FPGA SpiNNaker – eDVS connection User guide

Key 0 – RST

Key 1 is broken

Key 2 - Start

LEDG 1 – dumping packets for spinnaker

LEDG 2 – SpiNNaker ready

LEDG 0 – packet ready

LEDR 0 – transmitting to eDVS

LEDR 1 – receiving from eDVS

SW 1 send data to MATLAB

RS 232 send data to MATLAB