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Transformerless high voltage pulse generators for bipolar drive of Dielectric Barrier Discharges

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Abstract

Dielectric barrier discharge (DBD) lamps are capacitive loads that require pulsed operation to provide a homogeneous discharge distribution and consequently high lamp efficiency. As DBDs have a low Power Factor (PF) and almost dirac-like power consumption, resonant mode driving circuits are advantageous. In order to avoid restrictions of transformer-equipped topologies, such as high volume, high complexity and reliability issues due to the occurrence of a parasitic parallel resonance, this paper presents High Voltage Supplied Sinusoidal Pulse (HVS-SP) topologies that operate from high input voltage and do not require a transformer. As a main benefit, the transformer-less design also permits higher pulse frequency. By using the energy that remains stored in the DBD capacitance, voltage amplification of the circuit is higher compared to transformer-equipped variants. The topologies are rated against competing approaches and problems are discussed. Experiments show an electrical efficiency of 80 %.

1. Introduction

Dielectric Barrier Discharges (DBD) are used in applications as ozone synthesis, pollution control and surface treatment. The DBD principle can be utilized to excite rare gases in order to form excimers which emit ultraviolet (UV) light. These UV radiation sources feature long lifetime and instant UV output without any run-up time. The high energy radiation can cure lacquer coatings and could prospectively be utilized in water purification processes. In order to transform the UV wavelengths into visible light, a phosphor coating can be applied. Resulting DBD lamps are used as instant reliable light source in scanners and in architectural lighting applications.

Several topologies are known to drive DBD loads in pulsed mode. However, many require a transformer or coupled inductor to step-up the supply voltage in order to achieve the ignition voltage of the DBD, which is typically in the range of several kilovolts. The approach given in [1] uses a high voltage supplied full-bridge and thereby omits the transformer. Although an electrical efficiency of 89.4 % is claimed, the continuous square wave excitation of the DBD is less beneficial. Because the rms-voltage across the lamp connections is high compared to the lamp peak voltages, compliance with safety standards is aggravated. Furthermore, because the rising and falling edges of the lamp voltage have the same relative amplitude, beneficial bipolar excitation schemes [2] are not possible. The principle of a resonant up-swing as suggested in [3] generates high voltage sinusoidal pulses from low input voltage, but the necessary oscillations prior to ignition may deteriorate lamp efficiency [4].

This paper presents circuits that use high voltage Silicon Carbide (SiC) normally-on JFETs and MOSFETs to generate a sinusoidal pulse from a high voltage source without the use of a transformer. A flat Planilum® DBD lamp with a capacitance of 3 nF and an typical ignition voltage of 1.9 kV is oper-

ated with pulses of up to 1 MHz frequency. Even higher pulse frequencies are possible as the effective DBD capacitance is not enhanced by a transformer.

2. Circuit set-up and operation mode

The proposed circuit is based on the resonant principle. It utilizes the capacitance of the DBD to form a resonant tank in cooperation with an additional inductor. In contrast to continuously operating inverters, the resonant tank is excited and damped discontinuously.
The circuits presented here are high voltage supplied transformer-less topologies. Therefore, no parasitic parallel resonance [5] occurs and no DC-blocking capacitors are required. Furthermore, the voltage level of the DBD in idle time is no longer controlled by transformer freewheel action and therefore stays constant. The circuits presented benefit from the possibility to utilize the energy stored in the DBD capacitance for the following pulse. As the transformer ratio no longer enhances the effective DBD capacitance, the highest possible pulse frequency is increased by a factor of this ratio.
Drawbacks of these topologies include the requirement of a high voltage source and probably higher electromagnetic interference generated during fast switch transitions.
The schematic of the basic transformer-less High Voltage Supplied Sinusoidal Pulse (HVS-SP) topology is depicted in Figure 1A. The resonance circuit containing the DBD capacitance C_{DBD} and the series inductor L is excited by a half-bridge configuration consisting of two SiC-JFETs. As the JFETs do not contain body diodes, the additional SiC-Schottky diodes D1 and D2 are beneficially connected anti-parallel in order to support ZVS turn-on of the low switch LS and energy recovery at pulse termination. A pulse is initialized by enabling high switch HS with ZCS transition.

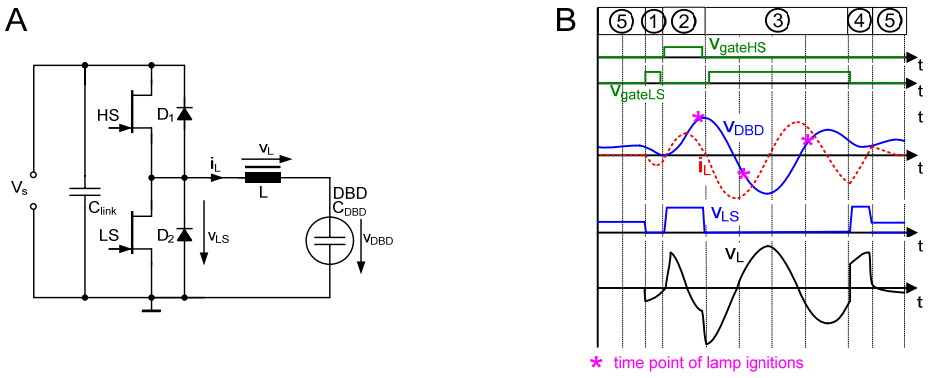


Figure 1: Schematic (A) and waveforms (B) of the HVS-SP topology equipped with SiC JFET switches.

The L-C circuit reacts with a voltage overshoot which follows a negative cosine wave shape as depicted in time range 2 of Figure 1B. During the last part of this positive voltage slope, the lamp ignites for the first-time. By soon initiating current transition from HS to LS, ZVS turn-on of LS is achieved. During time range 3, driven by a negative current, v_{DBD} swings back and leads to a beneficial [2] second ignition of the DBD. After a third voltage half wave, energy recovery is initiated in time range 4 by opening LS. This turn-off occurs under high current and therefore, fast switching is important to handle switching loss. C_{DBD} is almost discharged by the negative current i_L during one energy recovery cycle. This is in contrast to topologies that feature an inductor pre-charge as presented in [6] and require multiple recovery cycles.
However, an amount of energy equal to (1) is left in the circuit which concentrates in terms of a positive voltage offset of v_{DBD} and v_{LS}. A unique turn-on of LS in advance of pulse initialization utilizes the energy left in the DBD capacitance in order to store it in inductor L during time range 1. With this, ZVS

turn-on of HS is supported as suggested in [5]. Time range 5 in Figure 1B is the idle time in which no pulse is generated.
An important design criterion is the energy handling capability of the inductor that is approximately equal to maximum DBD capacitor energy (2). The peak resonant current of the not damped circuit is also depending on pulse frequency (3) and is mainly restricted by the maximum switch current. Another restriction occurs because of the necessary quality factor Q that has to be achieved in order to benefit from sufficient voltage amplification.

$$E_{left,rec} = \frac{1}{2}\left[V_s^{\,2}\left(C_{DBD} + C_{LS,oss}\right) + i_L^{\,2} L\right] \quad (1) \qquad E_L \approx \frac{1}{2} C_{DBD} \cdot V_{ign}^{\,2} \quad (2) \qquad I_{L,pk} \approx 2\pi C_{DBD} \cdot f_s \cdot V_{ign} \quad (3)$$

Beside the half-bridge configuration, a second half-bridge can be attached as shown in Figure 2A. This High Voltage Supplied Single Period Sinusoidal Pulse (HVS-SPSP) topology makes it possible to recover energy from the DBD immediately after the second ignition. This prevents a third ignition [7], which is less efficient. That is because also positive inductor current can recover energy through D_{ER}. A sketch of time-dependent waveforms is given in Figure 2B. Low switch LS and energy recovery switch ERS must be enabled shortly in advance of the pulse in order to maximize the step amplitude of v_{DBD}. By enabling LS, a negative i_L allows a partial ZVS turn-on of ERS. The pulse is then initialized by disabling LS and enabling HS with ZCS-condition in time range (2).

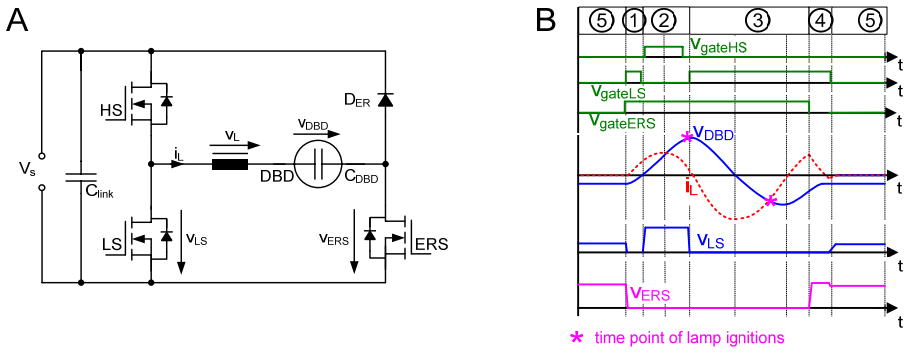


Figure 2: A: Schematic of the proposed HVS-SPSP topology; B: respective ideal waveforms.

Then, in time range (3), after the current i_L returns to being positive, energy recovery through diode DER is initiated by turning off energy recovery switch ERS. Depending on the time point at which ERS turns off, a certain amount of energy remains in the capacitances C_{DBD} and C_{OSS} of ERS:
This is roughly one quarter of maximum C_{DBD} energy. The resulting voltage offset dramatically reduces the relative amplitude of the negative voltage half-wave of the pulse. Thereby, current through the DBD is cut off shortly after the second ignition. Furthermore, the offset reduces the required supply voltage amplitude as the maximum voltage amplification is enhanced.
Although D_{ER} is made of SiC SBDs, a small reverse current flows through L after energy recovery. As $C_{DBD} >> C_{oss}$, V_{DBD} stays unaffected by this current. The negative i_L slightly rises V_{LS} above zero, while V_{ERS} falls. During idle time (5), V_{DBD} is equal to V_{LS} - V_{ERS} and, due to the full bridge configuration, is restricted to $-V_s$. In contrast to the HVS-SP topology and resonant up-swing techniques [3], absolutely no excitation by changes of V_{DBD} occurs in advance of the generated pulses. This is beneficial as it prevents any pre-ionization of the gas inside the DBD. Therefore, ignition voltage is kept low and homogeneity as well as lamp efficiency do not suffer [4].

3. Gate Drive Circuits for SiC Switches

In order to minimize conduction and switching losses of the power semiconductors, high voltage SiC-diodes and transistors have been used. As SiC switches require unique driving voltage levels, special

drivers, which are depicted in Figure 3, were designed that provide fast switching and maximum noise immunity. Both drivers get the driving signal through an optical link and are supplied by a high voltage transformer with symmetric voltage while the source of the respective power transistor is connected to circuit ground.

As the JFET contains a forward biased diode between gate and source, during the on-time, the driver has to act as current source. The circuit in Figure 3A provides two current levels to drive the gate. In low-state, during switching and shortly after turn-on, the driver provides high current through R_{HC}. In permanent on-state, the current is restricted by R_{LC}. The low impedance provided during the switch-off transition is especially crucial in order to restrict turn-off losses of the low switch in the half-bridge configuration. The origin of the negative spike that occurs during the transition from high current to low current is not yet clear. It does not appear if the transistor is replaced by a resistor. As no turn-off behavior is detectable, the transistor stays nevertheless in conducting state.

SiC MOSFETs are beneficially used in the HVS-SPSP topology as the reverse recovery time of their body diodes is not relevant for energy recovery. This is because energy recovery is performed by the extra SiC diode S_{PC}. These devices require operation with +22 V > V_{gate} > -5 V. Based on the symmetrical supply, a level-shift circuit containing ZD1-3 and C1 is implemented in the drive circuit shown in Figure 3B.

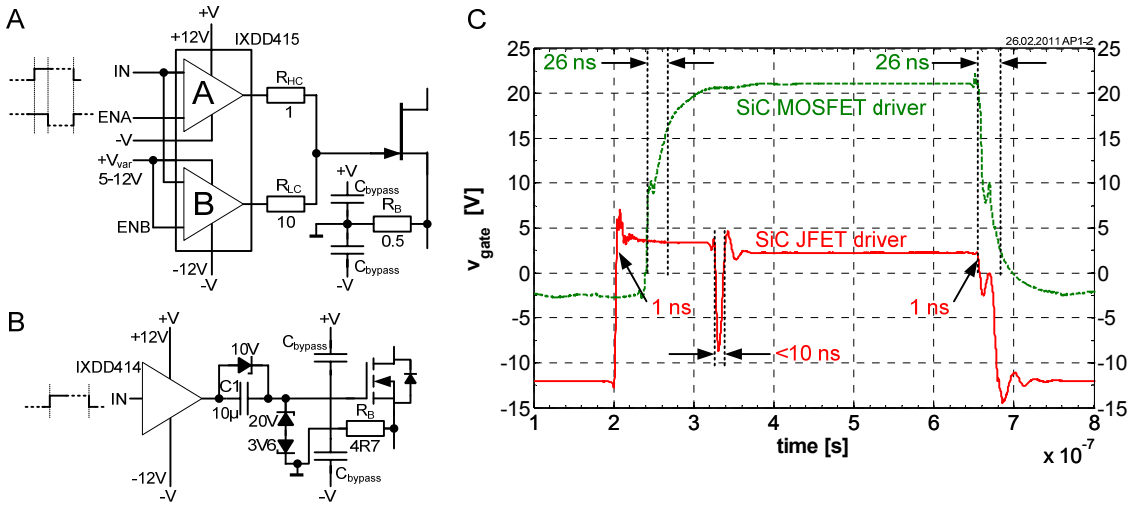


Figure 3: Gate drive circuits for SiC JFET SJEP120R063 (A) and SiC MOSFET CMF20120D (B); A: Delay of ENA is generated by monovibrator logic. C: Experimental results. JFET driver and MOSFET driver each attached with one switch.

4. Experimental Results

The two topology variations presented were evaluated by experiment. The measurement of input power has been performed using a high accuracy power meter. However, because of the high frequency, high voltage pulse, the measurement of DBD power has to be performed with an oscilloscope and respective probes. All probes were DC-calibrated, AC-compensated and deskewed. In order to isolate the circuit efficiency, lamp power is calculated across the repetition period f_{rep} and only across the pulse itself. The measured output power was evaluated twice: thermal loss measurement of heatsink and inductor yielded $P_{loss,therm}$ and calculation of the semiconductor loss procured $P_{loss,\,calc}$.

Figure 4 shows the results of the experimental operation of the suggested HVS-SP topology with a pulse frequency of 580 kHz. The supply voltage V_s has been adjusted to 1.15 kV. As can be seen in Figure 4A, the resonant circuit generated a peak voltage of 2 kV. This gives an overshoot factor of 1.74, which corresponds to an effective quality factor Q_{res} during the first voltage slope of 7. Also given

is Q_{res} gained by logarithmic decrement calculation. Three ignitions of the DBD are indicated by infrared radiation shown in Figure 4A. After energy recovery, which is finished at time point 2.84 µs, only 4 % of the C_{DBD} peak energy remains in the circuit. This energy leads to a parasitic series resonance of the switch output capacitances and L, which is damped by the resistive components of the circuit. The maximum current during the pulse occurs during the maximum negative slope of DBD voltage at time point 2.63 µs. The amplitude of approximately 23 A corresponds well with formula (3). Although the efficiency is electrically measured to be 70 %, the thermal verification yields up to 88 % efficiency.

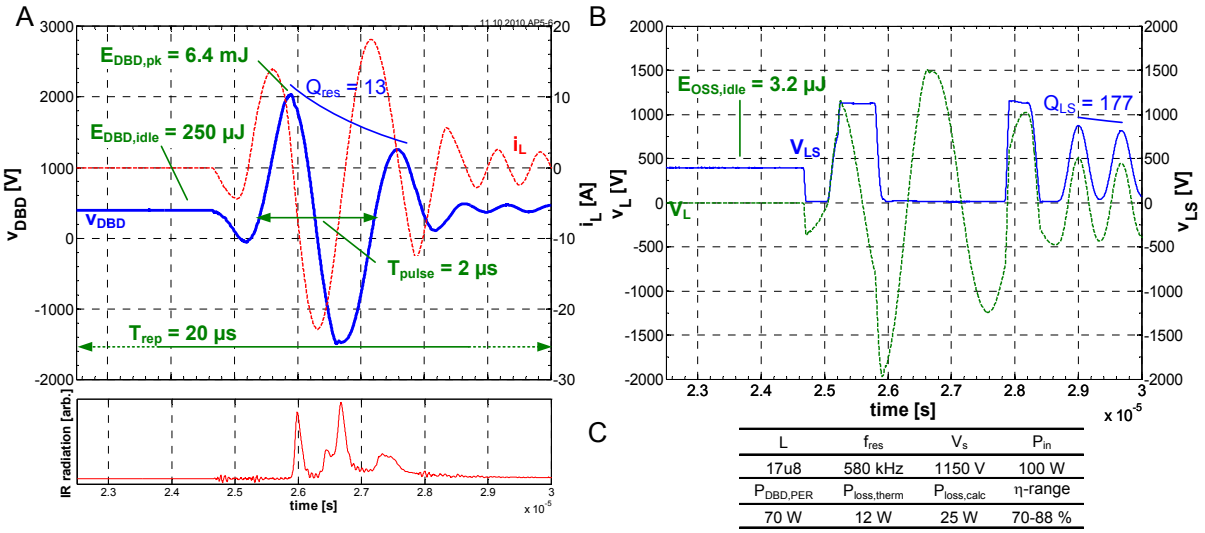


Figure 4: Experimental results. A: DBD voltage v_{DBD}, inductor current i_L and corresponding IR radiation; B: low switch voltage v_{LS} and inductor voltage v_L; C: key parameters.

The results for the experimental operation of the supposed HVS-SPSP topology are given in Figure 5. In this case, voltage measurement accuracy becomes even worse. This is because both DBD potentials float and therefore a differential measurement with two voltage probes needs to be performed. Only two sinusoidal half-waves are generated that beneficially lead to two ignitions per pulse. As indicated, PF of the first ignition is much higher compared to the second.

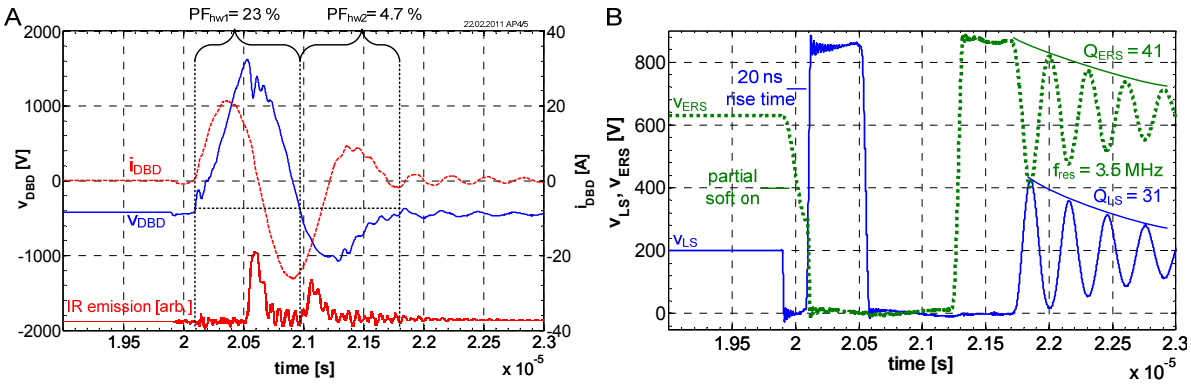
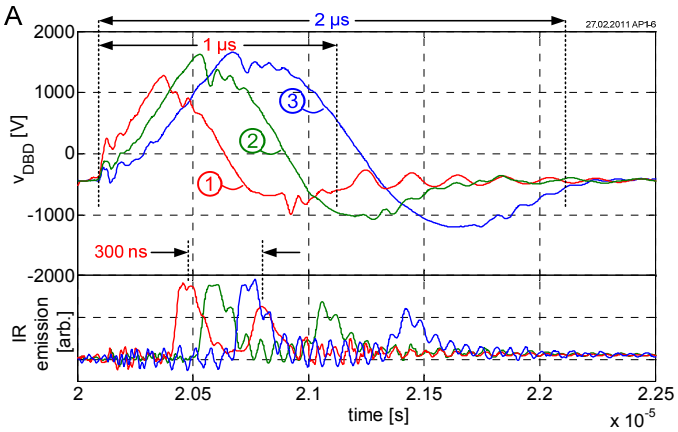


Figure 5: Experimental data of HVS-SPSP topology operation, V_s = 860 V, P_{in} = 107 W, f_{res} =25 kHz. A: DBD voltage V_{DBD}, DBD current i_{DBD}, infrared radiation; B: energy recovery switch voltage v_{ERS} and low switch voltage v_{LS}.

The SiC MOSFETs switch with up to 43 kV/µs. After pulse termination, the v_{LS} and v_{ERS} approach voltage levels determined by the different output capacitances of the respective bridge leg. The short turn-on of LS in advance of the pulse permits an partial soft turn-on of ERS. The DBD voltage v_{DBD} is constant beyond the actual pulse.

A variation of pulse frequency is depicted in Figure 6. As pulse frequency rises, the power fed into the first ignition also rises and outer ignition voltage shrinks by several hundred volts. However, due to the higher peak current, the electrical efficiency of the circuit is slightly lessened. The shrinking of the outer ignition voltage indicates a lower pre-ionization of the gas inside the DBD.

A



B

	③	②	①
L	17u8	8u	2u6
f_{res} [kHz]	500	670	1000
V_s [V]	900	860	860
P_{in} [W]	100	106.7	110
$P_{DBD,PER}$ [W]	61.3	51.9	45
$P_{DBD,PULSE}$ [W]	80	79	75
$PF_{DBD,1st\ half\text{-}wave}$ [W]	18%	23%	35%
$P_{loss,therm}$ [W]	16	14	22
$P_{loss,calc}$ [W]	19.3		26.3
η-range [%]	61-84	49-86	41-78

f_{rep} = 25 kHz

Figure 6: Comparison of different pulse widths achieved by different values for series inductance L. At pulse frequency of 1 MHz, delay between first and secondary ignition is as short as 300 ns.

5. Conclusion

This paper proved the possibility to drive DBD with a sinusoidal bipolar pulse without the use of a transformer. This omits parallel parasitic resonance and permits generation of high frequency pulses. The circuit is supplied by a high voltage source and contains Silicon Carbide (SiC) high voltage switches. For SiC MOSFETs and SiC JFETs, tailored gate drive circuits were presented. Further development of the excitation scheme led to the High Voltage Supplied Single Period Sinusoidal Pulse (HVS-SPSP) topology. With this, the used DBD flat lamp with a capacitance of 3 nF was operated at a pulse frequency of 1 MHz. The efficiency measurements were cross-checked by thermal loss measurements. The electrical efficiency of the topologies is in the range of 80 %.

Future work will include the verification of enhanced homogeneity and efficiency of the discharge at high frequency single period sinusoidal pulse excitation. This will be investigated by high speed imaging. Precise luminous flux measurements will prove the higher DBD efficiency achieved.

6. Literature

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