Agenda

- LPC1768 overview
- LPC1768 GPIO
- GPIO programming
    - LED
    - Buzzer
    - LCD

LPC1768 overview

- ARM Cortex-M3 (ARMv7-M)
- Flash 512KB
- SRAM 64KB
- (Boot) ROM 8 KB
- DMA Controller
    - Transfer data from RAM to IO device and vice-versa without intervention of CPU. CPU can spend more time in executing main code (rather than ISR for data transfer).
- Clock & Power circuit
- Fast GPIO
- Ethernet
- USB
- AHB to APB Bridge 0 & 1
- SSP (Synchronous Serial Port) & SPI
- I2C & I2S
- UART
- CAN
- Timers & RIT
- Watchdog Timer
- RTC
- PWM & Encoder
- ADC & DAC
- External Interrupts

Memory Mapped IO

- Flash:
- RAM:
- Boot ROM:
- GPIO: 0x2009C000 - 0x2009FFFF
- Peripherals:

LPC1768 GPIO

- There are 5 ports, each of 32 pins. But not all pins are in use.

LPC1768 Registers

- FIODIR (FIODIR0 to FIODIR4)
    - FIO2DIR : 0x2009C040
    - To change direction of GPIO port pin
        - 1: Output (Write on port pin)
        - 0: Input (Read from port pin)
- FIOSET (FIOSET0 to FIOSET4)
    - FIO2SET : 0x2009C058
    - To write on port pin
        - 1: Makes port pin high
        - 0: No effect
    - Its value (1) is latched.
- FIOCLR (FIOCLR0 to FIOCLR4)
    - FIO2CLR : 0x2009C05C
    - To write on port pin
        - 1: Makes port pin low
        - 0: No effect
    - Its value (1) is latched.
- FIOPIN (FIOPIN0 to FIOPIN4)
    - FIO2PIN : 0x2009C054
    - To read from port pin
        - High: reads as 1
        - Low: reads as 0
    - To write on port pin (without latching)
        - 1: Makes port pin high
        - 0: Makes port pin low
- FIOMASK (FIOMASK0 to FIOMASK4)
    - Avoids accidental changes in port pins.
    - 0: changes on port pins are allowed via SET, CLR or PIN registers.
    - 1: changes on port pins are not allowed via SET, CLR or PIN registers.

Buzzer Programming

- Buzzer --> ~~P2.12~~ --> P2.11
    - 0: beep/on

        - 1: off

LCD (HD44780) Programming

- HD44780
    - MPU interface
        - 4-bit: DB4 to DB7
        - 8-bit: DB0 to DB7
        - Busy Flag: DB7 (read)
            - 1: LCD is busy (in executing last Instruction)
            - 0: LCD is available
        - RS: Register Select
            - Select between Instruction Register (0) or Data Register (1)
        - RW: Read/Write
            - Read(1) or Write(0)
        - EN: Enable
            - Data on data lines will be latched (into LCD) when there is falling edge on EN.
    - DDRAM
        - Line1 address: 00
        - Line2 address: 40
- To write instruction (4-bit mode)
    - RS=0
    - RW=0
    - Send high nibble (of instruction)
    - Falling edge on EN
    - Send lower nibble (of instruction)
    - Falling edge on EN
    - Wait for busy flag
- To write data/ascii (4-bit mode)
    - RS=1
    - RW=0
    - Send high nibble (of data)
    - Falling edge on EN
    - Send lower nibble (of data)
    - Falling edge on EN
    - Wait for busy flag
- Wait for busy flag
    - RS=0

    - RW=1
    - EN=1
    - Read data
    - Repeat read if DB7=1
    - EN=0

- When reset, by default HD44780 does following:
    - Clear display
    - Function set: 8-bit mode, single line display, 5x8 font
    - Display control: Display off, Cursor off, Blinking off
    - Entry mode: Addr Incr, No shift

- HD44780 instructions (for our cct)
    - Clear display: 0x01
    - Entry mode: Addr Incr, No shift: 0x06
    - Display control: Display on, Cursor off, Blinking off: 0x0C
    - Function set: 4-bit mode, 2-line, 5x8: 0x28
    - Line1 DDRAM Address: 0x80
    - Line2 DDRAM Address: 0xC0

- BlueBoard HD44780 connections
    - 4-bit mode
    - LCD_RS --> ~~P2.16~~ --> P1.24
    - LCD_RW --> ~~P3.4~~ --> P1.23
    - LCD_EN --> ~~P3.8~~ --> P1.22
    - LCD_D4 --> ~~P3.3~~ --> P2.4
    - LCD_D5 --> ~~P3.5~~ --> P2.5
    - LCD_D6 --> ~~P3.6~~ --> P2.6
    - LCD_D7 --> ~~P3.7~~ --> P2.7

Fast GPIO vs Legacy GPIO

- LPC1768 (CM3) have only Fast GPIO. LPC2148 (ARM7) have Fast as well as Legacy GPIO.
- Legacy GPIO is connected to Peripheral bus, while Fast GPIO is connected to ARM High-speed bus.
- Legacy GPIO work with speed of Peripheral (slower), while Fast GPIO work with speed of ARM core (faster).
- Legacy GPIO can be accessed only as word registers, while Fast GPIO can be accessed as word, half-word or byte registers.
- Fast GPIO also have Mask Register, while Legacy GPIO doesn't have such feature.

Bit Banging vs Bit Banding

- Changing bits of GPIO to 1 and 0 is called as Bit banging. This is done on appropriate timing for implentation of protols like UART, SPI or I2C in software. This mainly reduce cost of hardware.
- Bit Banding is feature of ARM Cortex architecture. Maps one bit of IO Register or RAM to one word in address space. Any change in bit will reflect into that word and vice-versa.

This eliminates need of bitwise operators for manipulating the bit. This change operation is done in single bus cycle.