ATMEGA32 GPIO

- ATMEGA32 have 4 ports each of 8 pins -- PA, PB, PC, PD.
- For each port there are 3 registers
    - DDRx -- Data Direction Register
        - DDRx.n = 0 --> Input pin
        - DDRx.n = 1 --> Output pin
    - PORTx -- To write on port pin
        - PORTx.n = 1 --> Pin voltage HIGH
        - PORTx.n = 0 --> Pin voltage LOW
    - PINx -- To read from port pin
        - Pin voltage HIGH --> PINx.n = 1
        - Pin voltage LOW --> PINx.n = 0
- If port pin is configured as input and is not connected to external cct, its state cannot be determined (tri-state). To avoid this, pull up resistor is connected to each port pin, which is activated using PORTx Register.

AVR instructions

- LD & ST instructions
    - LDS instruction load data from data space into the GPR, while STS store data from GPR into the data space. These instructions are of 4 bytes and take 2 cycles.
    - LD instruction load data from data space into the GPR, , while ST store data from GPR into the data space. The address of data space location is given using address registers X, Y & Z. These instructions are of 2 bytes and take 2 cycles.

Addressing modes

- Single register mode (Immediate mode)
    - LDI R16, 5
    - CPI R17, 0
    - INC R0
- Register mode
    - MOV R0, R1
    - ADD R3, R4
- Direct addressing mode
    - LDS R0, 0x0060

    - STS 0x0060, R0
    - IN R0, PINA
    - OUT PORTA, R1

- Register indirect addressing mode
    - LD R0, X

- Flash indirect mode
    - LPM R0, Z

AVR Assembly programming

- demo.asm --> Assembler --> demo.obj --> Linker --> demo.hex
- .asm --> Assembly code
- .obj --> Object code (COFF format)
- .hex --> Hexadecimal (Binary) code (Intel Hex format)
- .lis/.lst --> Listing file
    - Contains instruction address/location, Machine level code and Assembly code in text format.

- .map --> Map file
    - Contains symbols info in text format i.e. Segment, Name of Symbol, Address of Symbol.

ATMEGA32 Timers

- Timer0, Timer1 and Timer2
- Timer0 is 8-bit timers.
    - 0-255. Interrupt can be generated when overflow.
    - Can be used as timer (CLK) or counter (edges on T0 pin).
    - One match register (OCR0). Interrupt can be generated when matched.
    - Normal mode, CTC mode, PWM mode, Fast PWM mode.
    - max delay of 65.536 ms (on 4 MHz clock and 1024 prescalar).

- Timer2 is 8-bit timers.
    - 0-255. Interrupt can be generated when overflow.
    - Can be used as timer on CPU clock or external clock.
    - One match register (OCR2). Interrupt can be generated when matched.
    - Normal mode, CTC mode, PWM mode, Fast PWM mode.
    - max delay of 65.536 ms (on 4 MHz clock and 1024 prescalar).

- Timer1 is 16-bit timers.
    - 0-65535. Interrupt can be generated when overflow.
    - Can be used as timer (CLK) or counter (edges on T1 pin).
    - Two match registers (OCR1A & OCR1B). Interrupt can be generated when matched.

    - Normal mode, CTC mode, PWM mode, Fast PWM mode, ... (15 modes)
    - max delay of 16.777216 sec (on 4 MHz clock and 1024 prescalar).

Timer modes

- Normal mode
    - Up counting
    - If matched with OCR, can generate interrupt. Then counting continues.
    - If overflow, can generate interrupt. Then counter restart counting from 0.
- CTC mode (Clear Timer on Compare)
    - Up counting
    - If matched with OCR, can generate interrupt. Then counting restart from 0.

Timer1 registers

- TCNT1 (H+L) -- Timer counter
- OCR1A (H+L) -- Output Compare Register1
- OCR1B (H+L) -- Output Compare Register2
- ICR1 (H+L) -- Input Capture Register
- TCCR1A
    - COM1A (10) -- Output compare mode -- Change pin level on match with OCR1A
    - COM1B (10) -- Output compare mode -- Change pin level on match with OCR1B
    - FOC1A & FOC1B -- Force Output Compare
    - WGM1 (10) -- Waveform Generation Mode bits
- TCCR1B
    - WGM1 (23) -- Waveform Generation Mode bits
    - CS1 (2:0) -- Clock Selector
        - 101 -- prescalar=1024
- WGM1 (3:0)
    - Normal mode : 0000
    - CTC : 0100
- TIFR
    - TOV1
    - OCF1A
    - OCF1B
    - ICF1
- TIMSK -- to enable interrupt
    - TOIE1
    - OCIE1B
    - OCIE1A
    - TICIE1

AVR Interrupts

- AVR controllers have interrupt unit/controller.
- The interrupts have fixed priority.
- Each peripheral can generate one or more interrupts and hence have one or more ISRs in vector table.
- Vector table is located at address 0x0000 in flash ROM.
- Each slot in vector table is 2 locations (4 bytes) long. Typically vector table contains JMP instructions.
- ATMEGA32 have 21 interrupt sources.
    - slot0: (0000h) Reset
    - slot1: (0002h) EINT0
    - ...
    - slot7: (000Eh) Timer1 Compare OCR1A (OCF1A flag)
    - ...
- Typically interrupt flag is automatically cleared when ISR is executed.
- When interrupt occur in AVR:
    - Current instruction is completed.
    - Interrupts are disabled (I=0) and return address is pushed on stack.
    - The ISR address is loaded in PC and then ISR executes.
    - While return (RETI), return address is popped from stack into PC and interrupts are reenabled (I=1).