RealDigital

Project 8 Arithmetic circuits

Introduction

In this project, we consider combinational logic circuits that act on **busses**, rather than individual signals. Recall that busses are groups of related signals that are regarded as a single logical unit transporting **a binary number**, instead of a collection of independent signals. Even though we will regard the input signals as bits in a binary number, they are nevertheless **logic signals**, and we know how to design **logic circuits that operate on logic signals**. In this case, the circuits we will design **combine input signals** to produce **output signals** that are in accordance with the rules of **addition** and **comparison**.

Before you begin, you should:

- Be confident in implementing combinational and sequential circuits in Vivado;
- Be confident in using the Xilinx simulator.

After you're done, you should:

- Understand the operation of adders and comparators;
- Be comfortable designing circuits using structural Verilog.

Requirements

1. 4-bit CLA

Define a **4-bit Carry Look-ahead Adder (CLA)** using structural Verilog (i.e., define a module for the **bit-slice component** and a module for the **Carry Propagate Generate Network (CPGN)**, and then connect **four bit-slice modules to the CPGN**).

Simulate your circuit to verify its function, and then program it into the Boolean Board. Use the **8 slide switches** to define the inputs, and display the **output** on **two digits of the seven-segment display**.

2. Comparator

Define a **4-bit bitwise comparator** in Verilog. Connect the **LT, EQ, and GT comparator outputs to three LEDs**, and verify your comparator's function.