Moore_FSM_Traffi_Light_Controller - [D:/Moore_FSM_Traffi_Light_Controller/Moore_FSM_Traffi_Light_Controller.xpr] - Vivado 2018.2

File Edit Flow Tools Reports Window Layout View Run Help Quick Access Ready

9000 s Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Desig

SYNTHESIS
- Run Synthesis
- Open Synthesized Desi

IMPLEMENTATION
- Run Implementation
- Open Implemented Des

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manage

SIMULATION - Behavioral Simulation - Functional - sim_1 - traffic_light_controller_tb

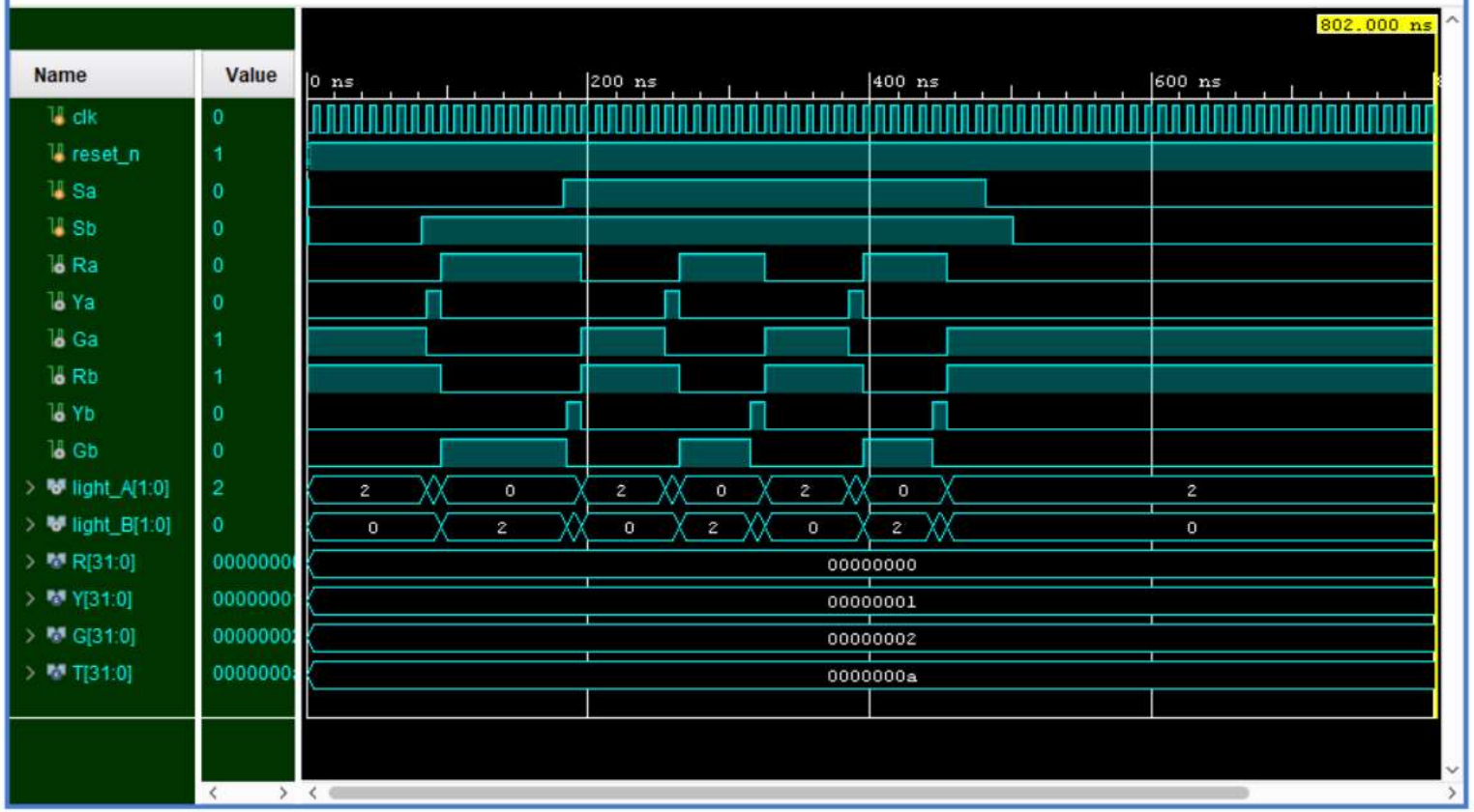
Scop | Sources

	Design U...	Block Type
traf...	traffic_lig...	Verilog M...
...	traffic_lig...	Verilog M...
glbl	glbl	Verilog M...

Objects

Name	Value	Data
clk	0	Logic
res...	1	Logic
Sa	0	Logic
Sb	0	Logic
Ra	0	Logic
Ya	0	Logic
Ga	1	Logic
Rb	1	Logic
Yb	0	Logic
Gb	0	Logic
lig...	2	Array
lig...	0	Array
R[3...	0	Array
Y[3...	1	Array
G[3...	2	Array
T[3...	10	Array

traffic_light_controller.v | traffic_light_controller_tb.v | Untitled 1



Tcl Console | Messages | Log

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'traffic_light_controller_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
```

Type a Tcl command here

Sim Time: 802 ns

Moore_FSM_Traffi_Light_Controller - [D:/Moore_FSM_Traffi_Light_Controller/Moore_FSM_Traffi_Light_Controller.xpr] - Vivado 2018.2

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Default Layout

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- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Open Elaborated Desig
- Report Methodology
- Report DRC
- Report Noise
- Schematic

SYNTHESIS
- Run Synthesis
- Open Synthesized Desi

IMPLEMENTATION
- Run Implementation
- Open Implemented Des

ELABORATED DESIGN - xc7vx690tffg1157-2 (active)

Sources | Netlist

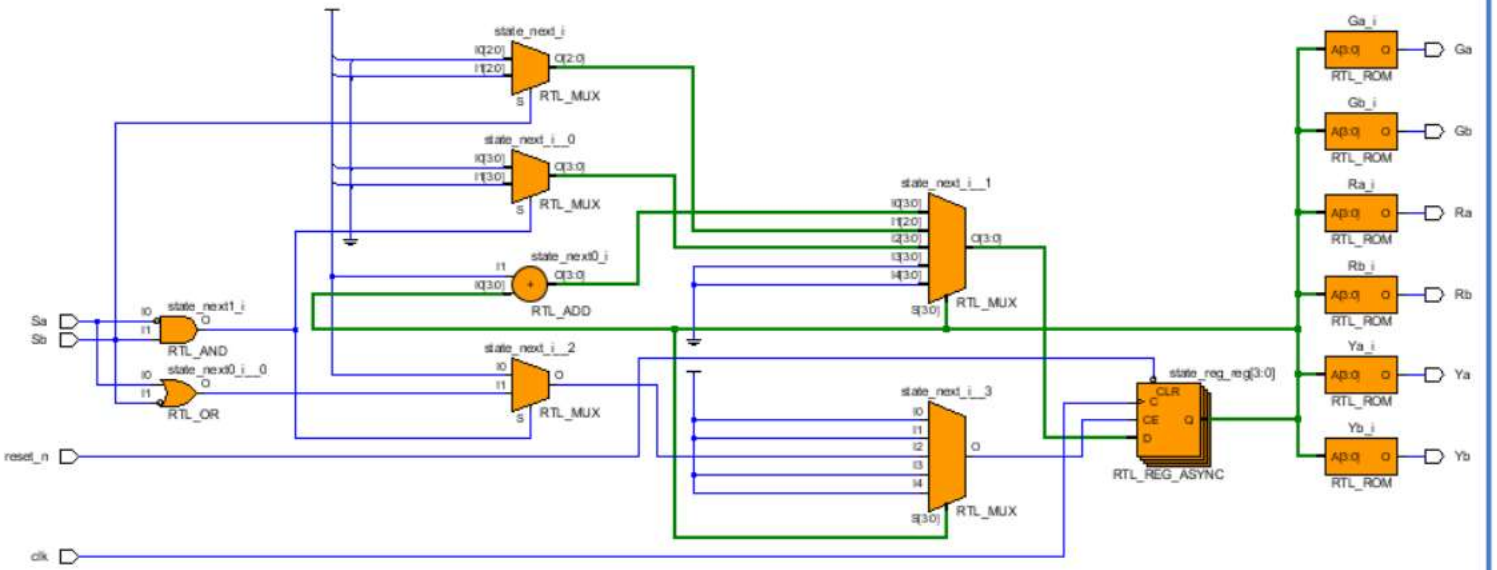
R traffic_light_controller
- Nets (35)
- Leaf Cells (20)

Source File Properties

Select an object to see properties

Project Summary | Schematic | traffic_light_controller.v | traffic_light_controller_tb.v

18 Cells 10 I/O Ports 35 Nets



Tcl Console | Messages | Log | Reports | Design Runs

```
7 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
```

Type a Tcl command here

Moore_FSM_Traffi_Light_Controller - [D:/Moore_FSM_Traffi_Light_Controller/Moore_FSM_Traffi_Light_Controller.xpr] - Vivado 2018.2

File Edit Flow Tools Reports Window Layout View Help Quick Access

Synthesis Complete

Default Layout

Flow Navigator

Language Templates
IP Catalog

IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design

SIMULATION
Run Simulation

RTL ANALYSIS
Open Elaborated Desig
Report Methodology
Report DRC
Report Noise
Schematic

SYNTHESIS
Run Synthesis
Open Synthesized Desi
Constraints Wizard
Edit Timing Constra
Set Up Debug
Report Timing Sumi
Report Clock Netwo
Report Clock Interac

SYNTHESIZED DESIGN - xc7vx690tffg1157-2 (active)

Sources Netlist

traffic_light_controller
Nets (31)
Leaf Cells (27)

Properties

Select an object to see properties

Project Summary Device traffic_light_controller.v traffic_light_controller_tb.v

Tcl Console Messages Log Reports Design Runs

```
INFO: [Project 1-479] Netlist was created with Vivado 2018.2
INFO: [Project 1-570] Preparing netlist for logic optimization
```

Type a Tcl command here