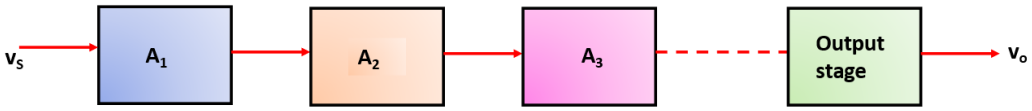
3.7 Introduction to output stage:



The output stage has to supply large power to the load. Hence it must satisfy the following requirements:

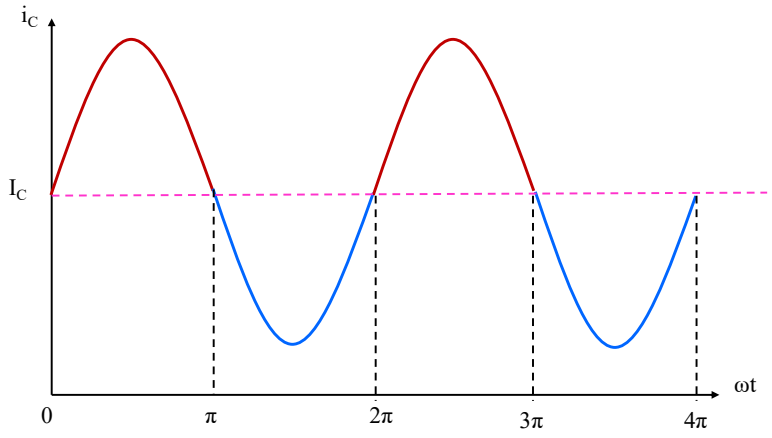
- It should have low output resistance so that power is not dissipated in the output resistance.
- The reduced power dissipation is required to ensure that the transistor is not heated due to excessive power dissipation.
- The power dissipation can be evaluated from the conversion efficiency. This requires that the output stage should have high efficiency.
- Therefore, the output stage evaluation is more concentrated on the efficiency of the amplifier rather than the voltage gain and current gain.

3.8 Classification of Output Stages:

(a) Class – A amplifier

In this type of amplifier, the transistor conducts for 360° That is the transistor conducts both during positive and negative half cycle of the input signal.

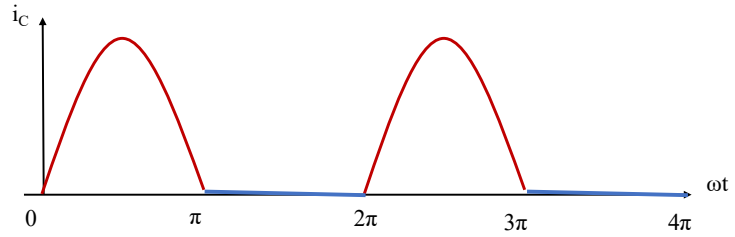
That is, the output current is a complete sine wave



(b) Class – B amplifier

In this type of amplifier, the transistor conducts for only 180^0. That is the transistor conducts only during positive and during negative half cycle of the input signal the transistor doesn't conduct.

That is, the output current is a half sine wave.

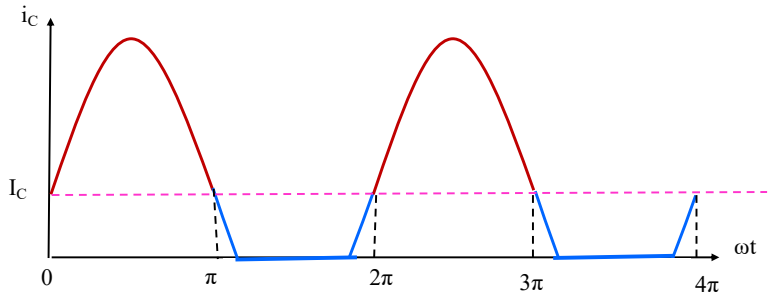


As seen in the above wave form, the output current is present only during positive half cycle and during negative half cycle the output current is zero.

(c) Class – AB amplifier

In this type of amplifier, the transistor conducts more than 180^0 but less than 360^0. That is the transistor doesn't conduct during a part of negative half cycle.

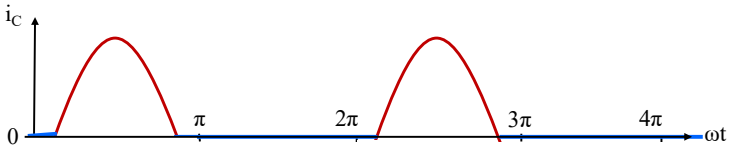
The output current waveform is as shown below.



(d) Class – C amplifier

In this type of amplifier, the transistor conducts less than 180^0. That is the transistor conducts for part of the positive half cycle and doesn't conduct in the negative half cycle.

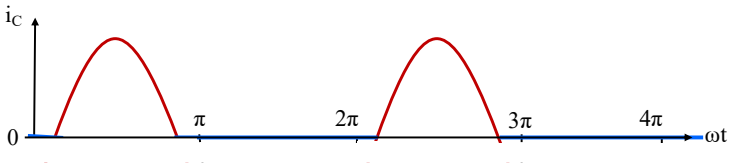
The output current waveform is as shown below.



(d) Class – C amplifier

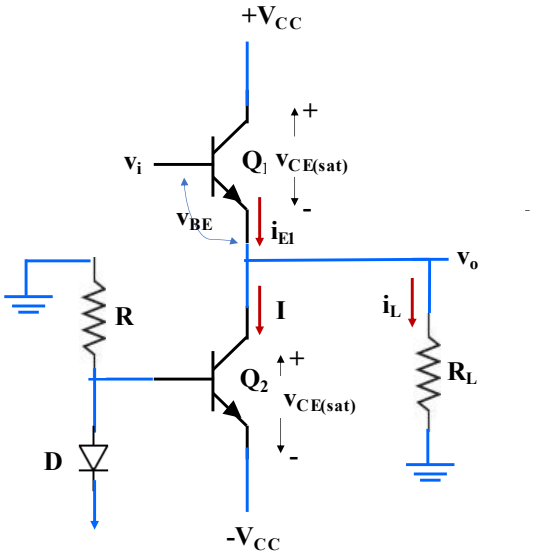
In this type of amplifier, the transistor conducts less than 180^0. That is the transistor conducts for part of the positive half cycle and doesn't conduct in the negative half cycle.

The output current waveform is as shown below.



3.9 Class-A output stage

(1) Transfer Characteristics



Circuit connections:

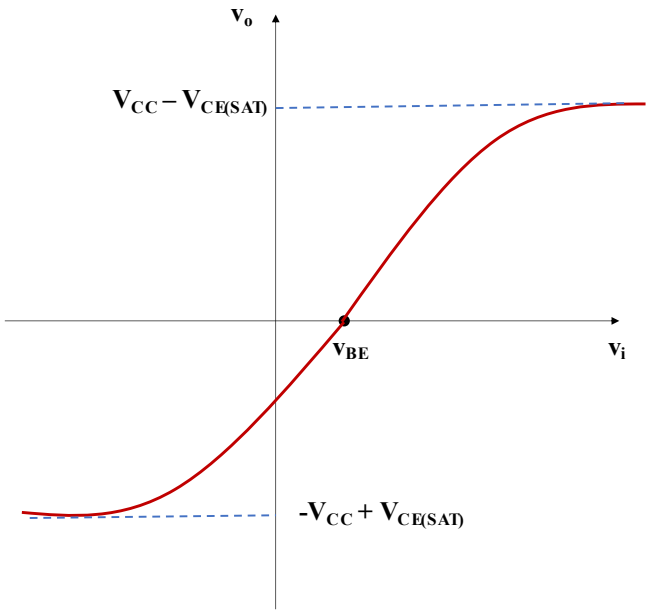
- The circuit consists of two transistors connected as shown in the figure.
- For the transistor Q_2, the resistor R and the diode D provides biasing. The resulting collector current I is constant.
- This current I of transistor Q_2 provides constant current biasing for the transistor Q_1.
- The input voltage is applied to base of Q_1.

Operation:

- The output voltage $v_o = v_i - V_{BE}$
- When the input voltage is equal to V_{BE}, the output voltage is '0'. If the input voltage is increases above V_{BE}, the output voltage increases as shown in the following graph. After a certain value, the output voltage saturates when Q_1 enters into saturation. In saturation, the volage $V_{CE(SAT)}$ is constant (around 0.2V). The corresponding output voltage is

  $V_{CC} - V_{CE(SAT)}$

- For all input voltages less than V_{BE}, the output voltage becomes negative and the load current flows through Q_2.
- As v_i increases in the negative direction, the output voltage also increases in the negative direction as shown in the figure. The extreme voltage in the negative direction is
  $-V_{CC} + V_{CE(SAT)}$



Thus, the variation of output voltage is from $(-V_{CC} + V_{CE(SAT)})$ to $(V_{CC} - V_{CE(SAT)})$

The maximum load current is $I_{L(max)} = [V_{CC} - V_{CE(SAT)}] / R_L$

The bias current in $Q_2 = [V_{CC} - V_{CE(SAT)}] / R_L$

The emitter current of Q1 varies between 0 and $2[V_{CC} - V_{CE(SAT)}] / R_L$.

(2) Power Dissipation:

Consider the case of zero load current.

$$I_L = 0$$

Then,

$$I_{E1} = I$$

Power dissipated in Q$_1$ $= V_{CC} I_{E1}$

$= V_{CC} I$

Power dissipated in Q$_2$ $= V_{CC} I$

Total Power dissipated $= 2\, V_{CC} I$

Output power = 0 (Since $I_L = 0$)

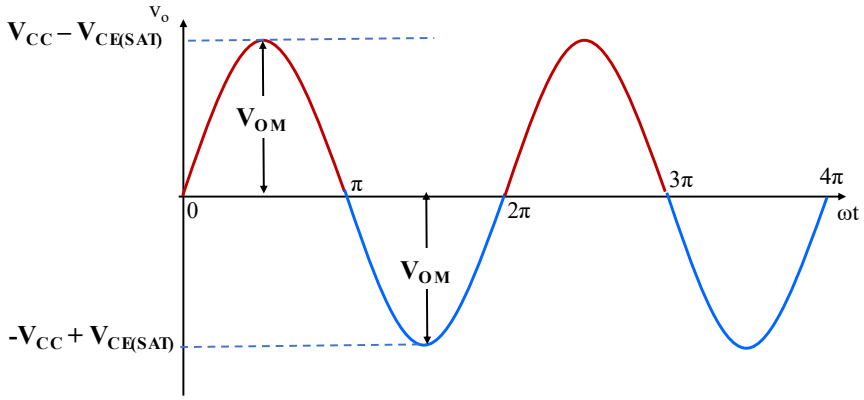
We know:

Input power = Output power + Total Power dissipated

Input power = $2\, V_{CC} I$

(3) Conversion Efficiency:

The output waveform of the circuit is as shown below. The peak value of the output voltage is: $V_{CC} - V_{CE(SAT)}$.



$$V_{OM} = V_{CC} - V_{CE(SAT)}$$

$$V_{OM} \cong V_{CC}$$

$$V_{ORMS} = \frac{V_{CC}}{\sqrt{2}}$$

AC Output power:

$$P_{oac} = \frac{(V_{ORMS})^2}{R_L}$$

$$P_{oac} = \frac{(\frac{V_{om}}{\sqrt{2}})^2}{R_L} = \frac{(V_{CC})^2}{2\,R_L}$$

$$\eta = \frac{\text{Output power}}{\text{Input power}}$$

$$\eta = \frac{\frac{V_{CC}^2}{2R_L}}{2\,V_{CC}\,I}$$

$$\eta = \frac{V_{CC}}{4\,(I\,R_L)}$$

$$\eta = \frac{1}{4}$$

$$\eta = 25\%$$

Prob:12A class-A output stage has supply voltage of V_{CC} =10V, load resistance of R_L = 100Ω. The DC bias current is constant at I = 100mA. The voltage across the load resistance has peak value of 8V. I output AC power, DC input power, efficiency and the power dissipated in the amplifier.

$$\text{Output power} = P_{oac} = \frac{(V_{ORMS})^2}{R_L}$$

$$P_{oac} = \frac{(\frac{V_{om}}{\sqrt{2}})^2}{R_L} = \frac{(V_{om})^2}{2\,R_L} = \frac{(8)^2}{2 \times 100} = \boxed{0.32\ W}$$

$$\text{Input power} = 2\,V_{CC}\,I = 2 \times V_{CC} \times I = 2 \times 10 \times 100 = \boxed{2\ W}$$

$$\eta = \frac{\text{Output power}}{\text{Input power}} = \frac{0.32}{2} = 0.16 = \boxed{16\%}$$

$$\text{Power dissipation} = \text{Input power} - \text{Output power} = 2\ W - 0.32\ W = \boxed{1.68\ W}$$

Prob: 13 A class-A output stage has supply voltage of V_{CC} =20V. The DC bias current is held constant at I = 100mA. The load resistance is adjusted to get maximum output power, find the maximum output AC power and the corresponding load resistance .

$$\text{Input power} = 2\,V_{CC}\,I = 2 \times V_{CC} \times I = 2 \times 20 \times 100 = \boxed{4\ W}$$

$$\text{Output power} = \eta \times \text{Input power}$$

$$= 0.25 \times 4 = \boxed{1\ W}$$

We know:

$$P_{oac} = \frac{(V_{ORMS})^2}{R_L} = \frac{(\frac{V_{om}}{\sqrt{2}})^2}{R_L} = \frac{(V_{om})^2}{2\,R_L} = \frac{(V_{CC})^2}{2\,R_L}$$

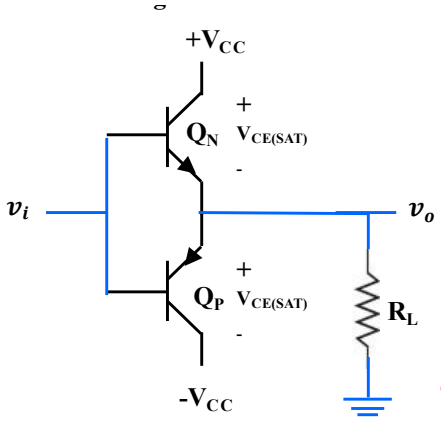
$$1 = \frac{(10)^2}{2\,R_L}$$

$$R_L = \boxed{50\ \Omega}$$

3.9 Class-A output stage

(1) Transfer Characteristics

Consider the following circuit diagram:



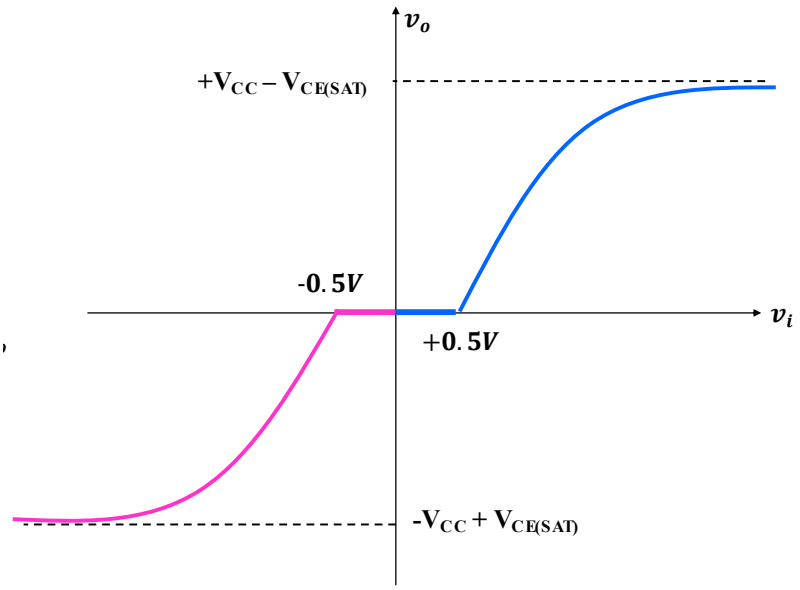
Circuit connections:

- One n-p-n transistor and another p-n-p transistor is connected together as shown in the figure. The emitters of the transistors are connected together and DC supply is connected to the collector terminal. Positive supply is used for n-p-n transistor and for the p-n-p transistor is connected negative DC supply is connected.
- The base terminals of the two transistors are connected together to the input signal v_i.
- The load resistor R_L is connected to the emitter terminal.
- The transistors are not provided with biasing arrangement. Therefore, there is no bias current is zero.

Circuit operation:

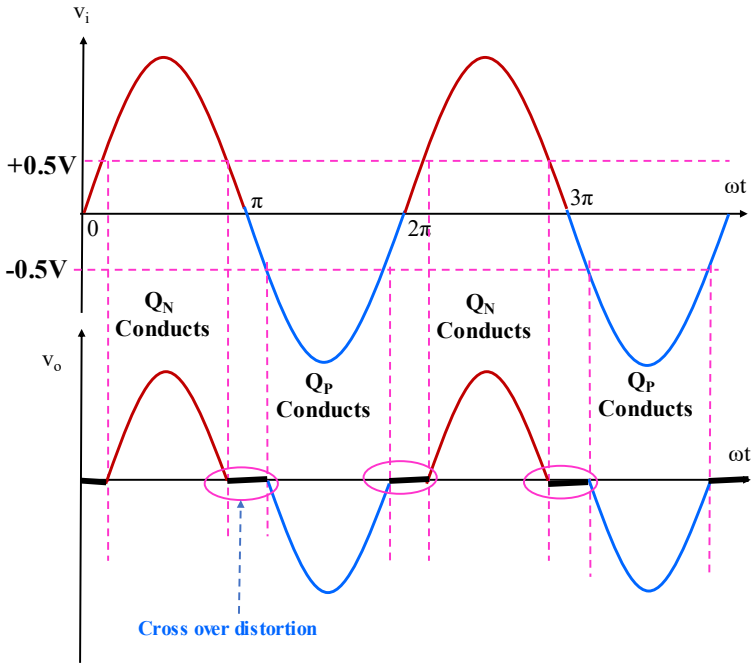
- Since the input is connected to the base terminal and output is connected to the emitter terminal, each transistor operates like "emitter follower". For an emitter follower, the voltage gain is unity. Therefore, the output voltage is equal to the input voltage.
- During positive half cycle of the input voltage, the transistor Q_N will conduct when the input voltage exceeds 0.5V which is the minimum voltage required to forward bias the base to emitter junction.
    - ❖ When Q_N is conducting, the positive input voltage appears at the output voltage.
    - ❖ As the input voltage increases, the output voltage is limited to $V_{CC} - V_{CE(SAT)}$ when transistor enters into saturation.
    - ❖ Thus, we get positive output voltage when Q_N conducts.
- During negative half cycle of the input voltage, the transistor Q_P will conduct when the input voltage exceeds - 0.5V which is the minimum voltage required to forward bias the base to emitter junction.
    - ❖ When Q_P is conducting, the negative input voltage appears at the output voltage.
    - ❖ As the input voltage increases, the output voltage is limited to $-V_{CC} + V_{CE(SAT)}$ when transistor enters into saturation.
    - ❖ Thus, we get negative output voltage when Q_P conducts.

Transfer characteristics:



(2) Conversion efficiency:

Based on the transfer characteristics, the output voltage waveform can be drawn as shown below. Each transistor conducts only when the input voltage exceeds 0.5V. When the input voltage is in between -0.5V and +0.5V, both the transistors will not conduct. Therefore, the output voltage is zero. This results in distorted output waveform. This is called “crossover distortion”.



Output power:

$$P_{OAC} = V_{ORMS}\, I_{ORMS}$$

$$P_{OAC} = \frac{V_{OM}}{\sqrt{2}} \frac{I_{OM}}{\sqrt{2}}$$

$$P_{OAC} = \frac{V_{OM}\, I_{OM}}{2}$$

Input power:

$$P_{I\,DC} = V_{CC} \times I_{O\,DC}$$

$$P_{I\,DC} = V_{CC} \times \frac{2I_{OM}}{\pi}$$

$$P_{I\,DC} = \frac{2\, V_{CC} I_{OM}}{\pi}$$

Efficiency:

$$\eta = \frac{P_{OAC}}{P_{I\,DC}}$$

$$\eta = \frac{\frac{V_{OM}\, I_{OM}}{2}}{\frac{2\, V_{CC} I_{OM}}{\pi}}$$

$$\eta = \frac{\pi}{4} \frac{V_{OM}}{V_{CC}}$$

To find maximum efficiency:

Put $V_{OM} = V_{CC}$ in the above equation.

$$\eta = \frac{\pi}{4} = 78.5\%$$

(3) Power dissipation:

The power dissipation is the difference between input DC power and the output AC power.

P_D = I/P power - O/P power

$P_D = P_{IDC} - P_{OAC}$

$$P_D = \frac{2 V_{CC} I_{OM}}{\pi} - \frac{V_{OM} I_{OM}}{2}$$

$$P_D = \frac{2 V_{CC} V_{OM}}{\pi R_L} - \frac{V_{OM} V_{OM}}{2 R_L}$$

$$P_D = \frac{2 V_{CC} V_{OM}}{\pi R_L} - \frac{V_{OM}^2}{2 R_L}$$

Maximum power can be found by differentiating wrt V_{OM} and equating to 0

$$P_{Dmax} = \frac{2 V_{CC}^2}{\pi^2 R_L}$$

Prob: 14 A class-B output stage has supply voltage which is about 5V greater than the peak output voltage. The load resistance is 8 Ω. The power delivered to the load is 20 W. Calculate the value of supply voltage, peak current drawn from the supply, the total supply power, and the conversion efficiency. Also calculate the maximum power dissipated

output power = 20 W

$$\frac{V_{OM}^2}{2 R_L} = 20 \text{ W}$$

$$\frac{V_{OM}^2}{2 \times 8} = 20 \text{ W}$$

$$V_{OM} = \sqrt{2 \times 8 \times 20}$$

$$V_{OM} = 17.9 \text{ V}$$

To find V_{CC}

$$V_{CC} = V_{OM} + 5 \text{ V}$$

$$V_{CC} = 23 \text{ V}$$

To find peak supply current

$$I_{OM} = \frac{V_{OM}}{R_L}$$

$$I_{OM} = \frac{17.9}{8}$$

$$I_{OM} = 2.24 \text{ A}$$

To find power drawn from supply

$$P_{IDC} = \frac{2 V_{CC} I_{OM}}{\pi}$$

$$P_{IDC} = \frac{2 \times 23 \times 2.24}{\pi}$$

$$P_{IDC} = 32.8 \text{ W}$$

To find maximum power dissipation

$$P_{Dmax} = \frac{2 V_{CC}^2}{\pi^2 R_L} = \frac{2 \times (23)^2}{\pi^2 \times 8}$$

$$P_{Dmax} = 13.4 \text{ W}$$

To find efficiency

$$\eta = \frac{\text{Output power}}{\text{Input power}} = \frac{20}{32.8}$$

$$\eta = 61 \%$$

Prob: 15 A class-B output stage has supply voltage of 50V. What is the load resistance for which maximum output power is delivered Also calculate the power dissipated in the circuit The peak current drawn from the DC supply is 10 mA

$$\text{Input power} = \frac{2V_{CC}I_{OM}}{\pi}$$

$$= \frac{2 \times 50 \times 10}{\pi}$$

$$\text{Input power} = 318 \text{ m W}$$

$$\eta = \frac{\text{output power}}{\text{input power}}$$

$$\text{Output power} = \eta \times \text{input power}$$

$$= 0.785 \times 318$$

$$\text{Output power} = 249.9 \text{ m W}$$

To find R_L

$$R_L = \frac{V_{OM}}{I_{OM}}$$

$$R_L = \frac{50}{10}$$

$$R_L = 5 \text{ K}\Omega$$

To find power dissipation

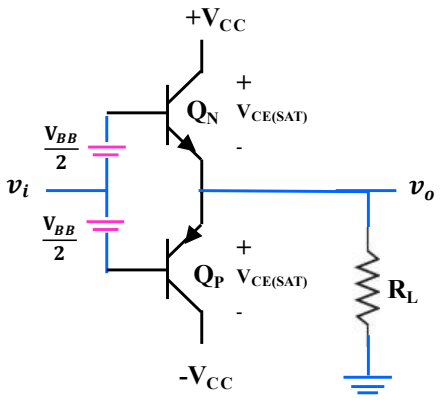
$$P_D = \text{Input power} - \text{Output power}$$

$$= 318 - 249.9$$

$$P_D = 68.1 \text{ m W}$$

3.10 Class- AB output stage

Circuit diagram:

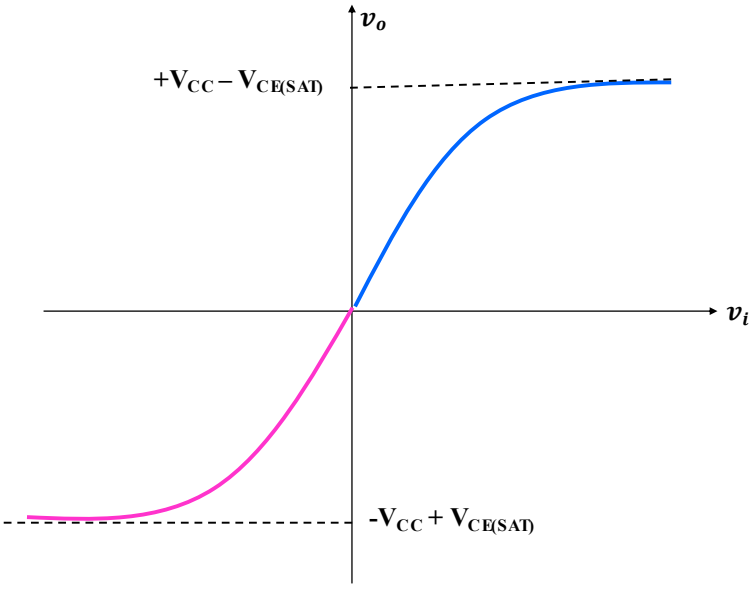


- One n-p-n transistor and another p-n-p transistor is connected together as shown in the figure. The emitters of the transistors are connected together and DC supply is connected to the collector terminal. Positive supply is used for n-p-n transistor and for the p-n-p transistor is connected negative DC supply is connected.
- The base terminals of the two transistors are connected together to the input signal v_i.
- The load resistor R_L is connected to the emitter terminal.
- Both the transistors are provided with biasing arrangement by connecting a DC supply $V_{BB}/2$ in the base of the transistors. The value of V_{BB} is adjusted to ensure the forward biasing of the base to emitter junction.

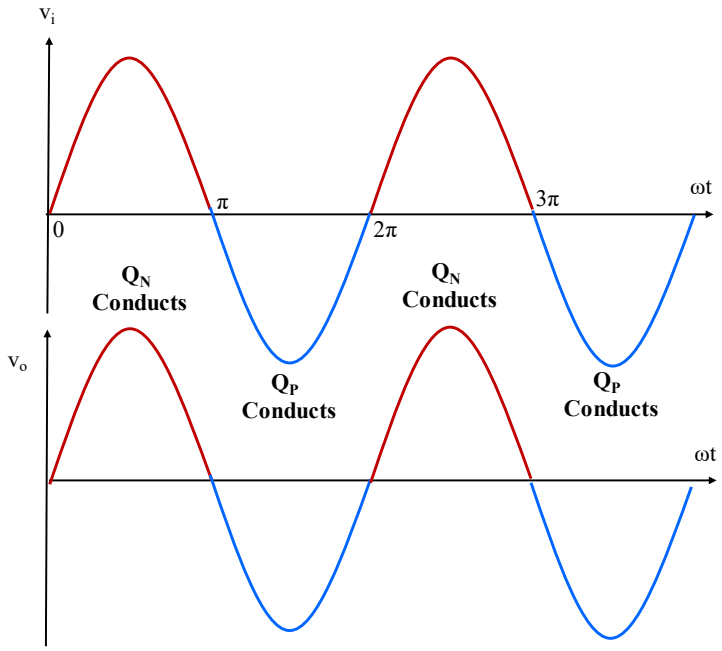
Circuit operation:

- Since the input is connected to the base terminal and output is connected to the emitter terminal, each transistor operates like "emitter follower". For an emitter follower, the voltage gain is unity. Therefore, the output voltage is equal to the input voltage.
- During positive half cycle of the input voltage, the transistor Q_N will conduct when the input voltage exceeds 0V.
  - ❖ When Q_N is conducting, the positive input voltage appears at the output voltage.
  - ❖ As the input voltage increases, the output voltage is limited to $V_{CC} - V_{CE(SAT)}$ when transistor enters into saturation.
  - ❖ Thus, we get positive output voltage when Q_N conducts.
- During negative half cycle of the input voltage, the transistor Q_P will conduct when the input voltage exceeds 0 V.
  - ❖ When Q_P is conducting, the negative input voltage appears at the output voltage.
  - ❖ As the input voltage increases, the output voltage is limited to $-V_{CC} + V_{CE(SAT)}$ when transistor enters into saturation.
  - ❖ Thus, we get negative output voltage when Q_P conducts.

Transfer characteristics:

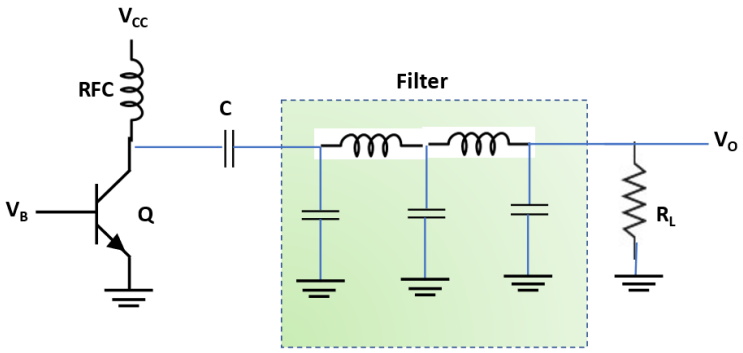


(2) Output waveform



As seen in the above waveform, the output waveform is free from "cross over distortion".

3.11 Class-C Tuned Amplifier



This circuit is used to get conversion efficiency greater than that of class B amplifier (78.5%). For this purpose, the transistor is operated either in cut-off or saturation.

In cut-off, the current through the transistor is zero. That is $I_C = 0$. Therefore, the power dissipated in the transistor is zero. The power dissipated can be found as product of voltage across the transistor and current through transistor. (Power dissipation = $V_{CE} \times I_C$)

In saturation, the voltage across the transistor is zero. That is $V_{CE} = 0$. Therefore, there is no power dissipation in the transistor.

Since the power dissipation is zero, the conversion efficiency will be very high.

Circuit connections:

The collector of the transistor is connected DC supply through an inductor called radio frequency coil (RFC). The collector is also connected to a filter circuit which removes harmonics to provide sinusoidal output of required frequency.

Operation:

During the positive half cycle of the input signal, the transistor is driven into saturation. Then the voltage across the transistor is zero. But current flows through RFC and the transistor.

During the negative half cycle of the input signal, the transistor is driven into cut-off and current through the transistor becomes zero. The inductor RFC develops the induced emf and this appears at the collector terminal. Due to the presence of inductor (RFC) and the capacitor at the collector, the collector voltage is sinusoidal.

The collector voltage is as follows: