DIGITAL SYSTEM DESIGN USING VERILOG

[SIMP] - TIE ECE REVIEW TEAM

Module - 01

01. Express the POS equations in a maxterms list form:

(i) $T = f(a,b,c) = (a+b'+c)(a'+b'+c)(a+b'+c)$

(ii) $J = f(a,b,c,d) = (a+b'+c+d)(a+b'+c+d')$
$(a'+b+c+d)(a'+b'+c+d)(a'+b'+c+d)$

02. Simplify the following expressions using K-map. Implement the simplified expression using basic gates:

(i) $f(a,b,c,d) = \sum m(2,3,4,5;13,15) + d(8,9,10,11)$

(ii) $f(a,b,c,d) = \Pi M(2,3,4,5,6,7,10,11,12)$

03. Using QM method and simplify the following function:

(i) $F1(a,b,c,d,e) = \sum m(0,2,8,10,16,18,24,26)$

(ii) $F2(a,b,c,d) = \sum m(0,1,2,3,6,7,8,9,14,15)$

(iii) $F3(a,b,c,d) = \sum m(2,3,4,5,6,7,10,11,12)$

(iv) $f(a,b,c,d) = \sum(1,3,4,5,6,9,11,12,13,14)$

04. Write the MEV K-map for the following Boolean functions:

(i) $F1(A,B,C,D) = \sum m(2,3,4,5,6,7,10,11,12)$

(ii) $F2(A,B,C,D) = \sum m(2,9,10,13,14,15)$

(iii) $F3(A,B,C,D) = \sum m(0,1,2,3,6,7,8,9,14,15)$

(iv) $Y = F(a,b,c,d,e) = \sum m(1,3,4,6,9,11,14,17,19,20,22,25,27,28,30) + \sum d(8,10,24,26)$

05. Define the following terms:

(i) Minterm (ii) Maxterm (iii) Combinational logic

(iv) Canonical sum of product (v) Canonical product of sum

06. Minimize the following multiple output functions using K-map:

(i) $F1 = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 4, 5, 14, 15)$

(ii) $F2 = \sum m(1, 2, 6, 7, 8, 13, 14, 15) + d(3, 5, 12)$

07. Show that $y = f(A, B, C, D) = \sum m(0, 2, 5, 7, 8, 10, 13, 15)$ is the complement of $y = f(A, B, C, D) = \pi(1, 3, 4, 6, 9, 11, 12, 14)$. Illustrate your answer using K-map to show the complement nature of the equations.

Module - 02

01. Implement full adder and full subtractor using decoder and write a truth table.

02. Design a logic circuit using a 3 to 8 logic decoder that has active low data inputs, an active high enable and active low data outputs. Use such a decoder to realize full adder circuit.

03. Implement the following function using 8:1 MUX:

$F1(A, B, C) = A'BD' + ACD + B'CD + A'C'D$

04. Design a combinational circuit to output the 2's complement of a 4 bit binary numbers: Construct the truth

table, simplify each output function using K-map and draw the logic diagram.

05. Design 2 bit comparator using logic gates.

06. Realize the following Boolean function $f(a,b,c) = \Sigma m(0,1,3,5,7)$ using 8:1 and 4:1 MUX.

07. Implement 16:1 MUX using 4:1 MUX.

Module-03

01. Explain the operation of a simple SR FlipFlop using NAND gates.

02. Explain how to use SR latch as a switch debouncer. Draw the timing diagram to support your explanation.

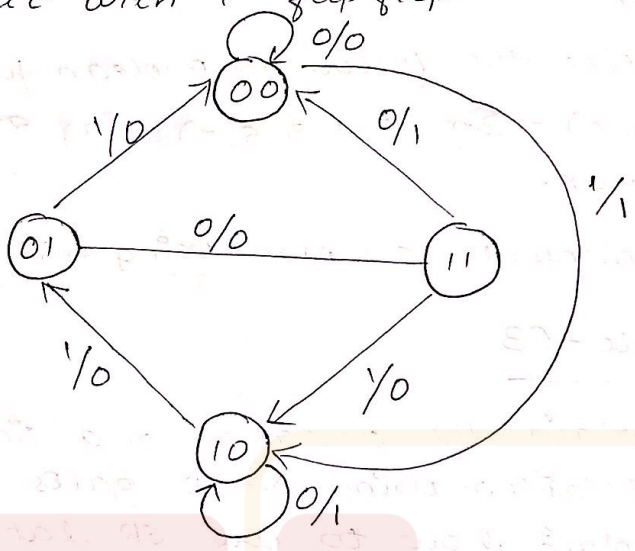
03. Explain the following:
(i) Switch debouncing and its elimination.
(ii) Race around problem and its elimination.

04. Design a block diagram of a mod 7 twisted ring counter and explain its operation.

05. Explain the following:
(i) 4 bit asynchronous counter
(ii) Johnson counter
(iii) Synchronous and asynchronous circuits.
(iv) Combinational and sequential circuits.

06. Compare between Moore and Mealy model with necessary block diagrams.

07. A sequential circuit has one input and one output. The state diagram is as shown below. Design a sequential circuit with 'T' flip flop.



Module - 04

01. What is Verilog? Differentiate between Verilog and VHDL.
02. What are the main differences between:
    (i) Task and Function in Verilog.
    (ii) Wire and Reg.
03. What are HDL simulators? Differentiate between blocking and non-blocking in Verilog.
04. What is the process to execute blocking and non-blocking assignments?
05. What do you understand by verilog full case statements and verilog parallel case statements?
06. What is repeat loop in verilog?
07. Describe data flow description in detail with examples.

Module – 05

01. Illustrate the structure of the HDL Behavioural description with necessary diagrams and programs.

02. Write the following:

(i) if statement syntax with expressions.

(ii) if else statement syntax with expressions.

(iii) case statement syntax with expressions.

(iv) loop statement syntax with expressions.

(v) Verilog Behavioral descriptions of MUX (2:1).

(vi) Structural descriptions of ripple carry adder.

03. What are sequential statements? Write the VHDL variable assignment statement.

04. Write the flow diagram of organization of structural description.