MODULE 4

Digital Voltmeter: Ramp Technique, Dual slope integrating Type DVM, Direct Compensation type and Successive Approximations type DVM. **Digital Multimeter:** Digital Frequency Meter and Digital Measurement of Time, Function Generator. **Bridges:** Measurement of resistance: Wheatstone's bridge, AC Bridges, Capacitance and Inductance Comparison bridge, Wien's bridge.

4.1 Digital Voltmeter: The digital voltmeters referred as DVM, converts the analog signals into digital and display the voltages to be measured as discrete numerals rather than pointer deflection, on the digital displays. DVMs can be used to measure ac and dc voltages and with proper transducer and signal conditioning circuit it can also measure parameters like pressure, temperature, stress etc. The output voltage is displayed on the digital display on the front panel.

These DVMs reduces the human reading and interpretation errors and parallax errors. The DVMs have various features and the advantages, over the conventional analog voltmeters having pointer deflection on the continuous scale.

There are different types of DVM which differ in number of digits, accuracy, speed of reading, size, power requirements and cost.

The important performance characteristics of DVM are as follows:

1. The input ranges from 1V to 1000V with provision for range selection and also indicates the overload condition.
2. Accuracy is high as ±0.005% of reading.
3. Resolution is 1ppm i.e. the meter can read 1μV on a 1V range.
4. Input impedance is around 10MΩ which helps in reducing loading effect.
5. Output is in BCD form and for other forms of output digital processing modules can be included.

4.2 Ramp Technique:

The operating principle is to measure the time that a linear ramp takes to change the input level to the ground level, or vice-versa. This time period is measured with an electronic time-interval counter and the count is displayed as a number of digits on an indicating tube or display. The operating principle and block diagram of a ramp type DVM are shown in Figs 4.1 and 4.2. The ramp may be positive or negative; in this case a negative ramp has been selected.

At the start of the measurement a ramp voltage is initiated (counter is reset to 0 and sampled rate multivibrator gives a pulse which initiates the ramp genera-tor). The ramp voltage is continuously compared with the voltage that is being measured. At the instant these two voltage become equal, a coincidence circuit generates a pulse which opens a gate,
i.e. the input comparator generates a start pulse. The ramp continues until the second

comparator circuit senses that the ramp has reached zero value. The ground comparator compares the ramp with ground. When the ramp voltage equals zero or reaches ground potential, the ground comparator generates a stop pulse. The output pulse from this comparator closes the gate. The time duration of the gate opening is proportional to the input voltage value.

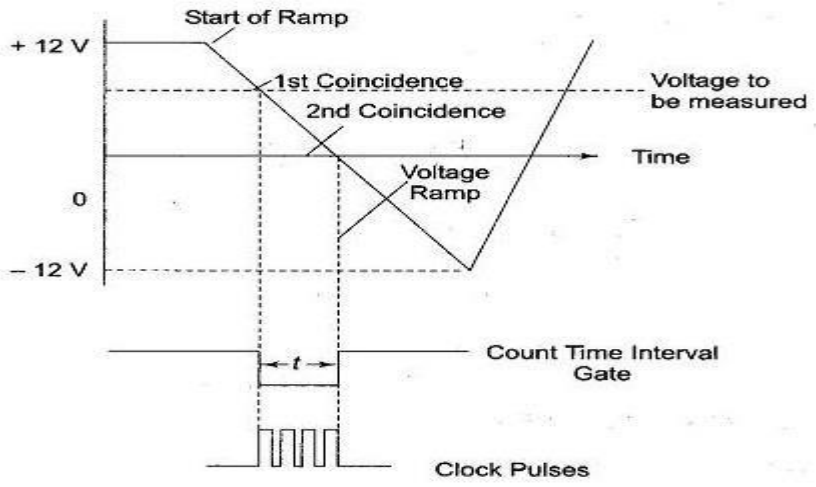

Figure 4.1: Voltage to time conversion

In the time interval between the start and stop pulses, the gate opens and the oscillator circuit drives the counter. The magnitude of the count indicates the magnitude of the input voltage, which is displayed by the readout. Therefore, the voltage is converted into time and the time count represents the magnitude of the voltage. The sample rate multivibrator determines the rate of cycle of measurement. A typical value is 5 measuring cycles per second, with an accuracy of ± 0.005% of the reading. The sample rate circuit provides an initiating pulse for the ramp generator to start its next ramp voltage. At the same time a reset pulse is generated, which resets the counter to the zero state.

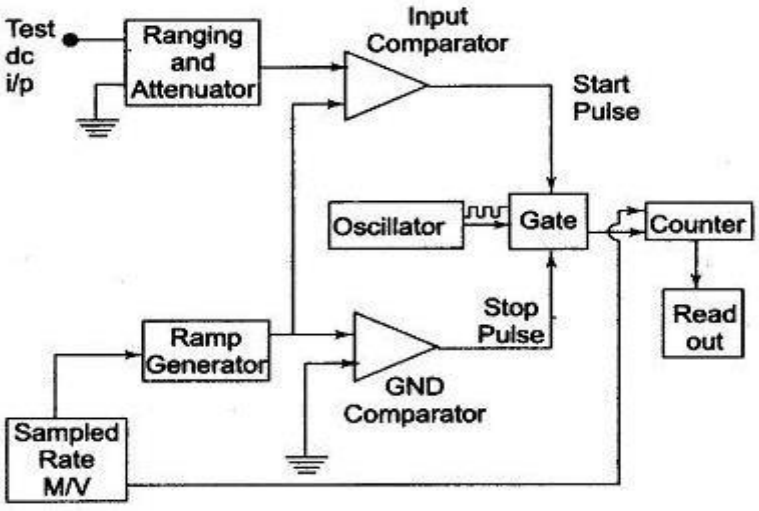

Figure 4.2: Block diagram of Ramp type DVM

4.2.1 Advantages and Disadvantages

The ramp technique circuit is easy to design and its cost is low. Also, the output pulse can be transmitted over long feeder lines. However, the single ramp requires excellent characteristics regarding linearity of the ramp and time measurement. Large errors are possible when noise is superimposed on the input signal. Input filters are usually required with this type of converter.

4.3 Dual Slope Integrating Type DVM (Voltage to Time Conversion):

Dual Slope Integrating Type DVM – In ramp techniques, superimposed noise can cause large errors. In the dual ramp technique, noise is averaged out by the positive and negative ramps using the process of integration.

Principle of Dual Slope Type DVM

As illustrated in Fig. 4.3, the input voltage 'e_i' is integrated, with the slope of the integrator output proportional to the test input voltage. After a fixed time, equal to t_1, the input voltage is disconnected and the integrator input is connected to a negative voltage — e_r. The integrator output will have a negative slope which is constant and proportional to the magnitude of the input voltage. The block diagram is given in Fig. 4.4.

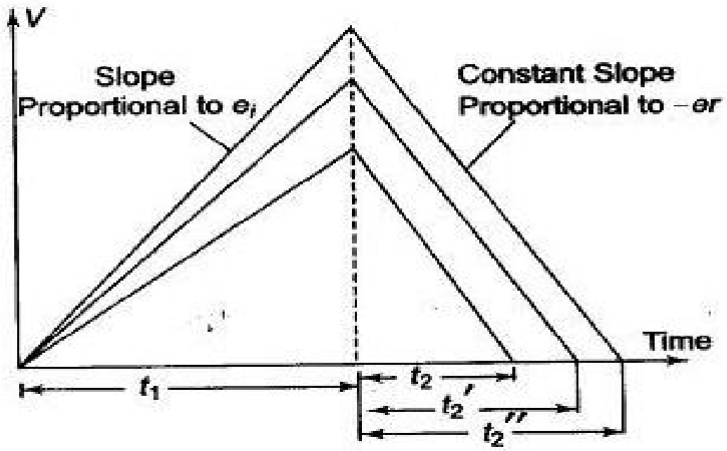

Figure 4.3: Basic principle of dual slope type DVM

At the start a pulse resets the counter and the F/F output to logic level '0'. S_i is closed and S_r is open. The capacitor begins to charge. As soon as the integrator output exceeds zero, the comparator output voltage changes state, which opens the gate so that the oscillator clock pulses are fed to the counter. (When the ramp voltage starts, the comparator goes to state 1, the gate opens and clock pulse drives the counter.) When the counter reaches maximum count, i.e. the counter is made to run for a time 't_1' in this case 9999, on the next clock pulse all digits go to 0000 and the counter activates the F/F to logic level '1'. This activates the switch drive, e_i is disconnected and $-e_r$ is connected to the integrator. The integrator output will have a negative slope which is constant, i.e. integrator output now decreases linearly to 0 volts. Comparator output state changes again and locks the gate. The

discharge time t_2 is now proportional to the input voltage. The counter indicates the count during time t_2. When the negative slope of the integrator reaches zero, the comparator switches to state 0 and the gate closes, i.e. the capacitor C is now discharged with a constant slope. As soon as the comparator input (zero detector) finds that e_0, is zero, the counter is stopped. The pulses counted by the counter thus have a direct relation with the input voltage.

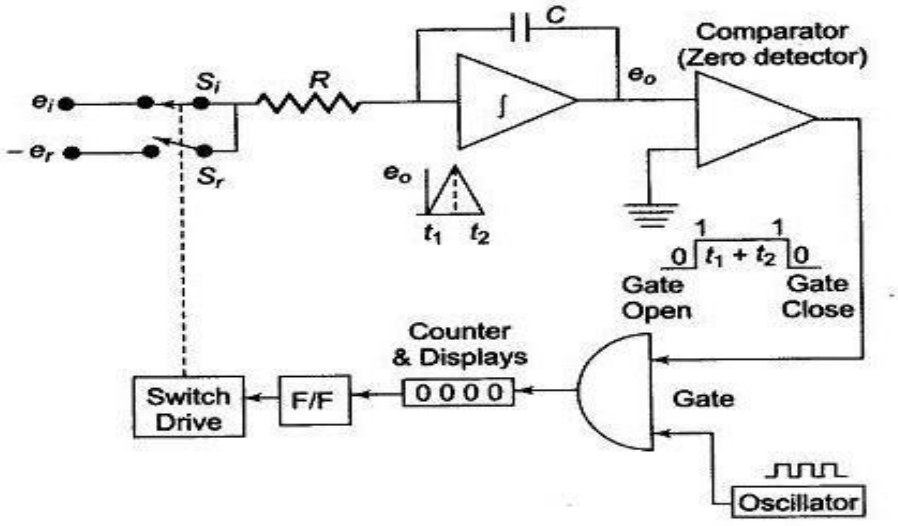

Figure 4.4: Block diagram of dual slope type DVM

During charging

$$e_o = -\frac{1}{RC}\int_0^{t_1} e_i\, dt = -\frac{e_i\, t_1}{RC} \tag{4.1}$$

During discharging

$$e_o = \frac{1}{RC}\int_0^{t_2} -e_r\, dt = -\frac{e_r\, t_2}{RC}$$

Subtracting Eqs 5.2 from 5.1 we have

$$e_o - e_o = \frac{-e_r t_2}{RC} - \left(\frac{-e_i t_1}{RC}\right)$$

$$0 = \frac{-e_r t_2}{RC} - \left(\frac{-e_i t_1}{RC}\right)$$

$$\frac{e_r t_2}{RC} = \frac{e_i t_1}{RC}$$

$$e_i = e_r \frac{t_2}{t_1}$$

If the oscillator period equals T and the digital counter indicates n_1 and n_2 counts respectively,

$$e_i = \frac{n_2 T}{n_1 T} e_r \quad \text{i.e.} \quad e_i = \frac{n_2}{n_1} e_r$$

Now, n_1 and e_r are constants.

$$\text{Let } K_1 = \frac{e_r}{n_1}. \text{ Then } e_i = K_1 n_2 \tag{4.4}$$

From Eq. 4.3 it is evident that the accuracy of the measured voltage is independent of the integrator time constant. The times t_1 and t_2 are measured by the count of the clock given by the numbers n_1 and n_2 respectively. The clock oscillator period equals T and if n_1 and e_r are constants, then Eq. 5.4 indicates that the accuracy of the method is also independent of the oscillator frequency.

The dual slope technique has excellent noise rejection because noise and superimposed ac are averaged out in the process of integration. The speed and accuracy are readily varied according to specific requirements; also an accuracy of ± 0.05% in 100 ms is available.

4.4 Successive Approximations

The successive approximations principle can be easily understood using a simple example; the determination of the weight of an object. By using a balance and placing the object on one side and an approximate weight on the other side, the weight of the object is determined.

If the weight placed is more than the unknown weight, the weight is removed and another weight of smaller value is placed and again the measurement is performed. Now if it is found that the weight placed is less than that of the object, another weight of smaller value is added

to the weight already present, and the measurement is performed. If it is found to be greater than the unknown weight the added weight is removed and another weight of smaller value is added. In this manner by adding and removing the appropriate weight, the weight of the unknown object is determined.

The successive approximation DVM works on the same principle. Its basic block diagram is shown in Fig. 4.5. When the start pulse signal activates the control circuit, the successive approximation register (SAR) is cleared. The output of the SAR is 00000000. V_{out} of the D/A converter is 0. Now, if $V_{in} > V_{out}$ the comparator output is positive. During the first clock pulse, the control circuit sets the D_7 to 1, and V_{out} jumps to the half reference voltage. The SAR output is 10000000. If V_{out} is greater than V_{in} the comparator output is negative and the control circuit resets D_7. However, if V_{in} is greater than V_{out} the comparator output is positive and the control circuits keep D_7 set. Similarly the rest of the bits beginning from D_7 to D_0 are set and tested. Therefore, the measurement is completed in 8 clock pulses.

Table 4.1

V_{in} = 1 V	Operation	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Compare	Output	Voltage
00110011	D_7 Set	1	0	0	0	0	0	0	0	$V_{in} < V_{out}$	D_7 Reset	2.5
"	D_6 Set	0	1	0	0	0	0	0	0	$V_{in} < V_{out}$	D_6 Reset	1.25
"	D_5 Set	0	0	1	0	0	0	0	0	$V_{in} > V_{out}$	D_5 Set	0.625
"	D_4 Set	0	0	1	1	0	0	0	0	$V_{in} > V_{out}$	D_4 Set	0.9375
"	D_3 Set	0	0	1	1	1	0	0	0	$V_{in} < V_{out}$	D_3 Reset	0.9375
"	D_2 Set	0	0	1	1	0	1	0	0	$V_{in} < V_{out}$	D_2 Reset	0.9375
"	D_1 Set	0	0	1	1	0	0	1	0	$V_{in} > V_{out}$	D_1 Set	0.97725
"	D_0 Set	0	0	1	1	0	0	1	1	$V_{in} > V_{out}$	D_0 Set	0.99785

At the beginning of the measurement cycle, a start pulse is applied to the start-stop multivibrator. This sets a 1 in the MSB of the control register and a 0 in all bits (assuming an 8-bit control) its reading would be 10000000. This initial setting of the register causes the output of the D/A converter to be half the reference voltage, i.e. 1/2 V. This converter output is compared to the unknown input by the comparator. If the input voltage is greater than the converter reference voltage, the comparator output produces an output that causes the control register to retain the 1 setting in its MSB and the converter continues to supply its reference output voltage of 1/2 V_{ref}.

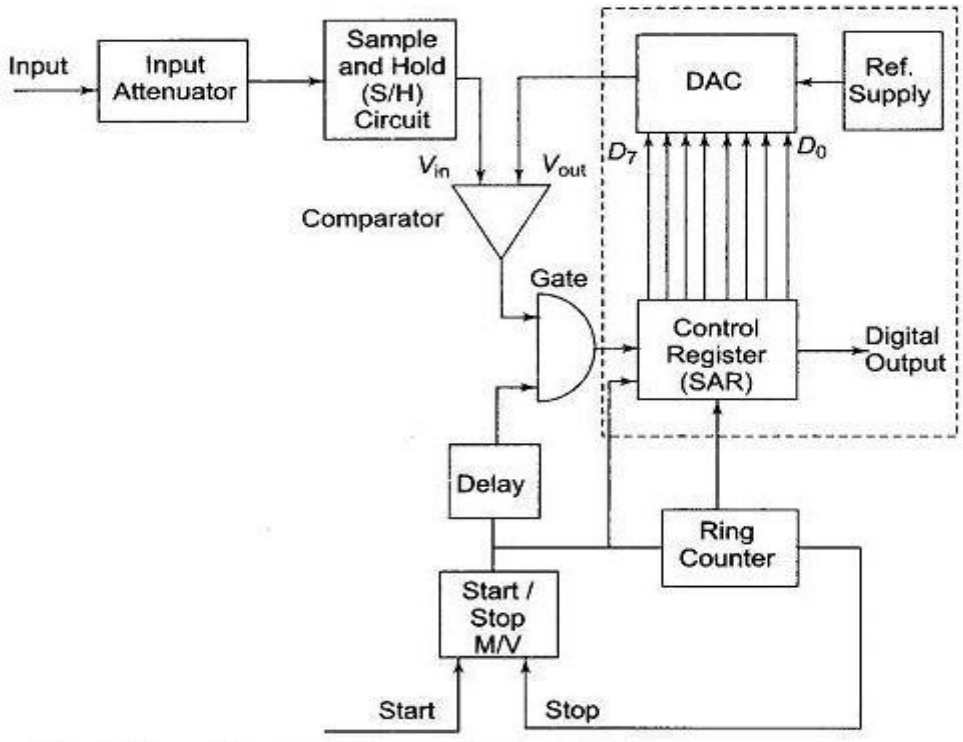

Figure 4.5: Successive approximation DVM

The ring counter then advances one count, shifting a 1 in the second MSB of the control register and its reading becomes 11000000. This causes the D/A converter to increase its reference output by 1 increment to 1/4 V, i.e. 1/2 V + 1/4 V, and again it is compared with the unknown input. If in this case the total reference voltage exceeds the unknown voltage, the comparator produces an output that causes the control register to reset its second MSB to 0. The converter output then returns to its previous value of 1/2 V and awaits another input from the SAR. When the ring counter advances by 1, the third MSB is set to 1 and the converter output rises by the next increment of 1/2 V + 1/8 V. The measurement cycle thus proceeds through a series of successive approximations. Finally, when the ring counter reaches its final count, the measurement cycle stops and the digital output of the control register represents the final approximation of the unknown input voltage.

4.5 Digital Multimeter Principles:

Analog meters require no power supply, they give a better visual indication of changes and suffer less from electric noise and isolation problems. These meters are simple and inexpensive. Digital meters, on the other hand, offer high accuracy, have a high input impedance and are smaller in size. They gives an unambiguous reading at greater viewing distances. The output available is electrical (for interfacing with external equipment), in addition to a visual readout. The three major classes of Digital Multimeter Principles are panel meters, bench type meters and system meters.

All Digital Multimeter Principles employ some kind of analog to digital (A/D) converters

(often dual slope integrating type) and have a visible readout display at the converter output.

Panel meters are usually placed at one location (and perhaps even a fixed range), while bench meters and system meters are often multimeters, i.e. they can read ac and dc voltage currents and resistances over several ranges.

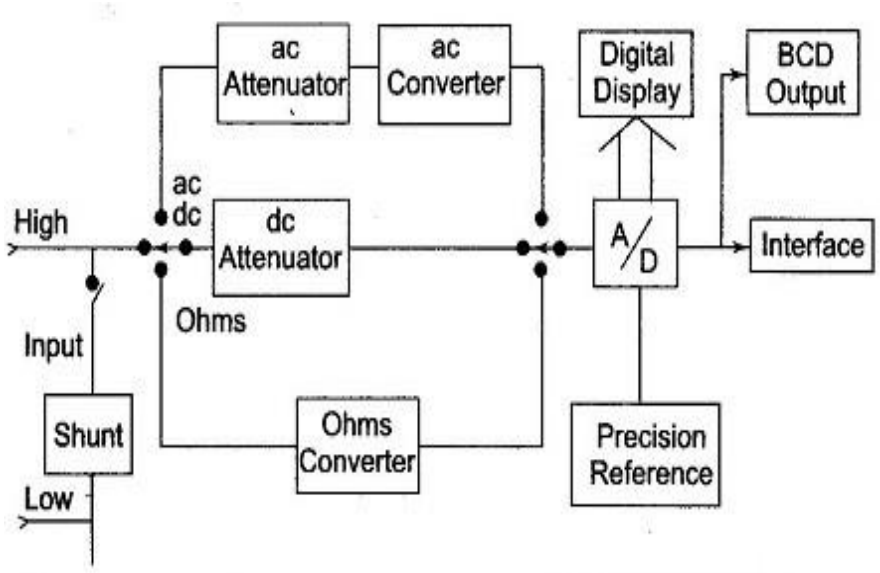

Figure 4.6: (a) Digital Multimeter

The basic circuit shown in Fig. 4.6(a) is always a dc voltmeter. Current is converted to voltage by passing it through a precision low shunt resistance while alternating current is converted into dc by employing rectifiers and filters. For resistance measurement, the meter includes a precision low current source that is applied across the unknown resistance; again this gives a dc voltage which is digitized and readout as ohms.

Bench meters are intended mainly for stand-alone operation and visual operation reading, while system meters provide at least an electrical binary coded decimal output (in parallel with the usual display), and perhaps sophisticated interconnection and control capabilities, or even microprocessor based computing power.

A basic Digital Multimeter Principles (DMM) is made up of several A/D converters, circuitry for counting and an attenuation circuit. A basic Digital Multimeter Block Diagram is shown in Fig. 4.6 (b). The current to voltage converter shown in the block diagram of Fig. 4.6 (b) can be implemented with the circuit shown in Fig. 4.6 (c).

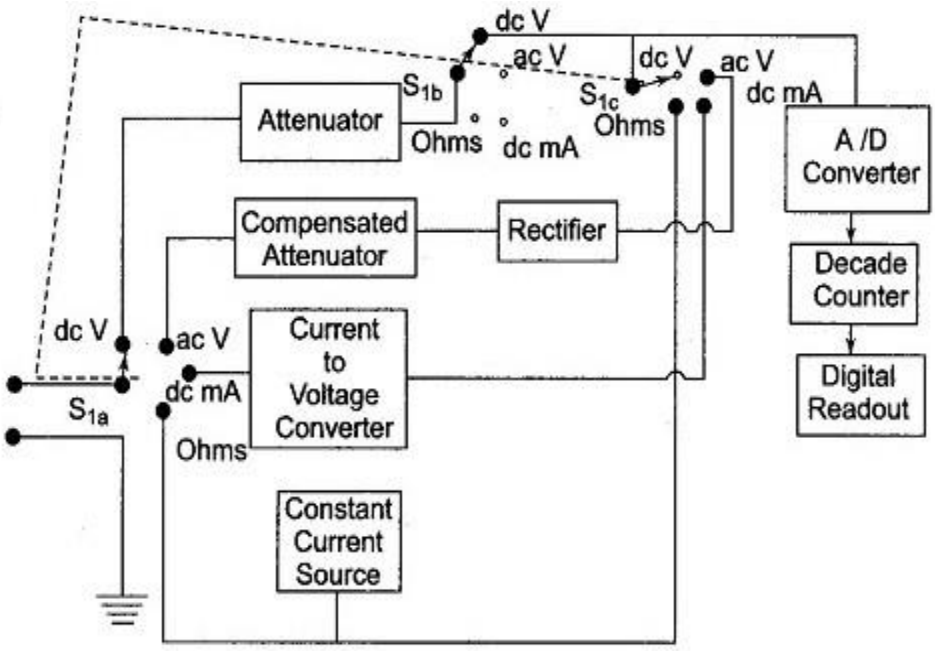

Figure 4.6: (b) Block diagram of a basic digital multimeter

The current to be measured is applied to the summing junction (Σi) at the input of the opamp. Since the current at the input of the amplifier is close to zero because of the very high input impedance of the amplifier, the current I_R is very nearly equal to I_i, the current I_R causes a voltage drop which is proportional to the current, to be developed across the resistors. This voltage drop is the input to the A/D converter, thereby providing a reading that is proportional to the unknown current.

Resistance is measured by passing a known current, from a constant current source, through an unknown resistance. The voltage drop across the resistor is applied to the A/D converter, thereby producing an indication of the value of the unknown resistance.

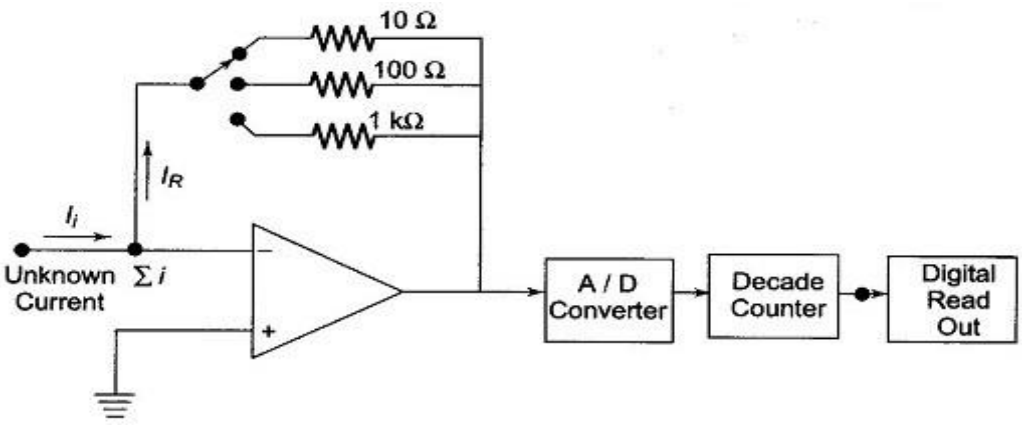

Figure 4.6: (c) Current to Voltage Converter

4.6 Digital Frequency Meter:

The Principle of Operation: The signal waveform is converted to trigger pulses and applied continuously to an AND gate, as shown in Fig. 4.7. A pulse of 1 s is applied to the other terminal, and the number of pulses counted during this period indicates the frequency.

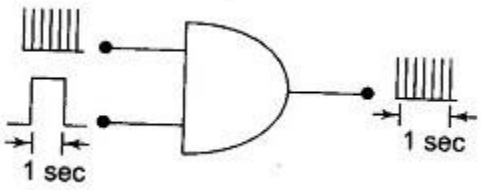

Figure 4.7: Principle of digital frequency meter

The signal whose frequency is to be measured is converted into a train of pulses, one pulse for each cycle of the signal. The number of pulses occurring in a definite interval of time is then counted by an electronic counter. Since each pulse represents the cycle of the unknown signal, the number of counts is a direct indication of the frequency of the signal (unknown). Since electronic counters have a high speed of operation, high frequency signals can be measured.

4.6.1 Basic Circuit of a Digital Frequency Meter:

The block diagram of a basic circuit of a digital frequency meter is shown in Fig. 4.8.

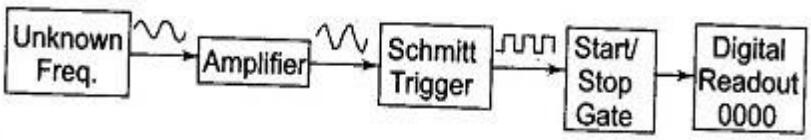

Figure 4.8: Basic circuit of a digital frequency meter

The signal may be amplified before being applied to the Schmitt trigger. The Schmitt trigger converts the input signal into a square wave with fast rise and fall times, which is

then differentiated and clipped. As a result, the output from the Schmitt trigger is a train of pulses, one pulse for each cycle of the signal.

The output pulses from the Schmitt trigger are fed to a START/STOP gate. When this gate is enabled, the input pulses pass through this gate and are fed directly to the electronic counter, which counts the number of pulses.

When this gate is disabled, the counter stops counting the incoming pulses. The counter displays the number of pulses that have passed through it in the time interval between start and stop. If this interval is known, the unknown frequency can be measured.

4.6.2 Basic Circuit for Frequency Measurement:

The basic circuit for frequency measurement is as shown in Fig. 4.9. The output of the unknown frequency is applied to a Schmitt trigger, producing positive pulses at the output. These pulses are called the counter signals and are present at point A of the main gate. Positive pulses from the time base selector are present at point B of the START gate and at point B of the STOP gate.

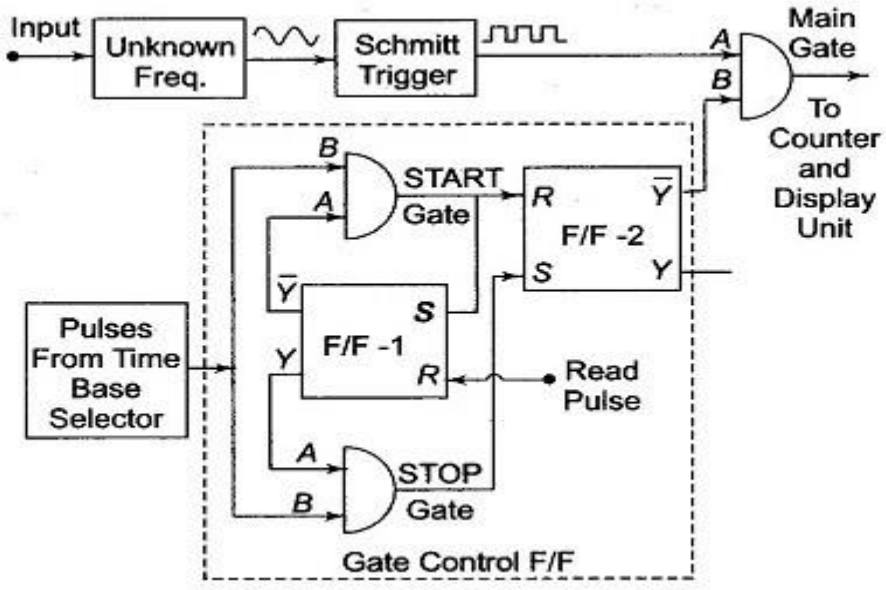

Figure 4.9: Basic circuit for measurement of frequency showing gate control flip-flop

Initially the Flip-Flop (F/F-1) is at its logic 1 state. The resulting voltage from output Y is applied to point A of the STOP gate and enables this gate. The logic 0 stage at the output Y of the F/F-1 is applied to the input A of the START gate and disables the gate.

As the STOP gate is enabled, the positive pulses from the time base pass through the STOP gate to the Set (S) input of the F/F-2 thereby setting F/F-2 to the 1 state and keeping it there.

The resulting 0 output level from Y of F/F-2 is applied to terminal B of the main gate. Hence no pulses from the unknown frequency source can pass through the main gate.

In order to start the operation, a positive pulse is applied to (read input) reset input of F/F-1, thereby causing its state to change. Hence Y = 1, Y= 0, and as a result the STOP gate is disabled and the START gate enabled. This same read pulse is simultaneously applied to the reset input of all decade counters, so that they are reset to 0 and the counting can start.

When the next pulse from the time base arrives, it is able to pass through the START gate to reset F/F-2, therefore, the F/F-2 output changes state from 0 to 1, hence Y changes from 0 to 1. This resulting positive voltage from Y called the gating signal, is applied to input B of the main gate thereby enabling the gate.

Now the pulses from the unknown frequency source pass through the main gate to the counter and the counter starts counting. This same pulse from the START gate is applied to the set input of F/F-1, changing its state from 0 to 1. This disables the START gate and enables the STOP gate. However, till the main gate is enabled, pulses from the unknown frequency continue to pass through the main gate to the counter.

The next pulse from the time base selector passes through the enabled STOP gate to the set input terminal of F/F-2, changing its output back to 1 and fi = 0. Therefore the main gate is disabled, disconnecting the unknown frequency signal from the counter. The counter counts the number of pulses occurring between two successive pulses from the time base selector. If the time interval between this two successive pulses from the time base selector is 1 second, then the number of pulses counted within this interval is the frequency of the unknown frequency source, in Hertz.

The assembly consisting of two F/Fs and two gates is called a gate control F/F. The block diagram of a digital frequency meter is shown in Fig. 4.10.

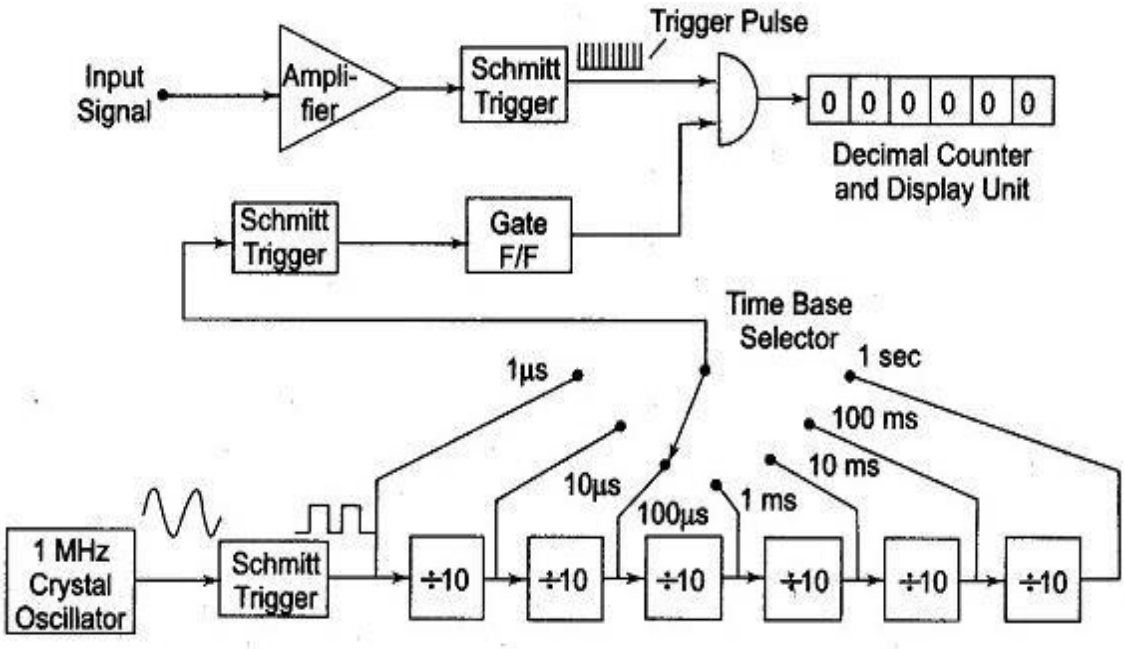

Figure 4.10: Block diagram of a digital frequency meter

The input signal is amplified and converted to a square wave by a Schmitt trigger circuit. In this diagram, the square wave is differentiated and clipped to produce a train of pulses, each pulse separated by the period of the input signal. The time base selector output is obtained from an oscillator and is similarly converted into positive pulses.

The first pulse activates the gate control F/F. This gate control F/F provides an enable signal to the AND gate. The trigger pulses of the input signal are allowed to pass through the gate for a selected time period and counted. The second pulse from the decade frequency divider changes the state of the control F/F and removes the enable signal from the AND gate, thereby closing it. The decimal counter and display unit output corresponds to the number of input pulses received during a precise time interval; hence the counter display corresponds to the frequency.

4.7 Digital Measurement of Time:

Principle of Operation: The beginning of the time period is the start pulse originating from input 1, and the end of the time period is the stop pulse coming from input 2.

The oscillator runs continuously, but the oscillator pulses reach the output only during the period when the control F/F is in the 1 state. The number of output pulses counted is a measure of the time period.

4.7.1 Time Base Selector:

It is clear that in order to know the value of frequency of the input signal, the time interval between the start and stop of the gate must be accurately known. This is called time base.

The time base consist of a fixed frequency crystal oscillator, called a clock oscillator, which has to be very accurate. In order to ensure its accuracy, the crystal is enclosed in a constant temperature oven. The output of this constant frequency oscillator is fed to a Schmitt trigger, which converts the input sine wave to an output consisting of a train of pulses at a rate equal to the frequency of the clock oscillator. The train of pulses then passes through a series of frequency divider decade assemblies connected in cascade. Each decade divider consists of a decade counter and divides the frequency by ten. Outputs are taken from each decade frequency divider by means of a selector switch; any output may be selected.

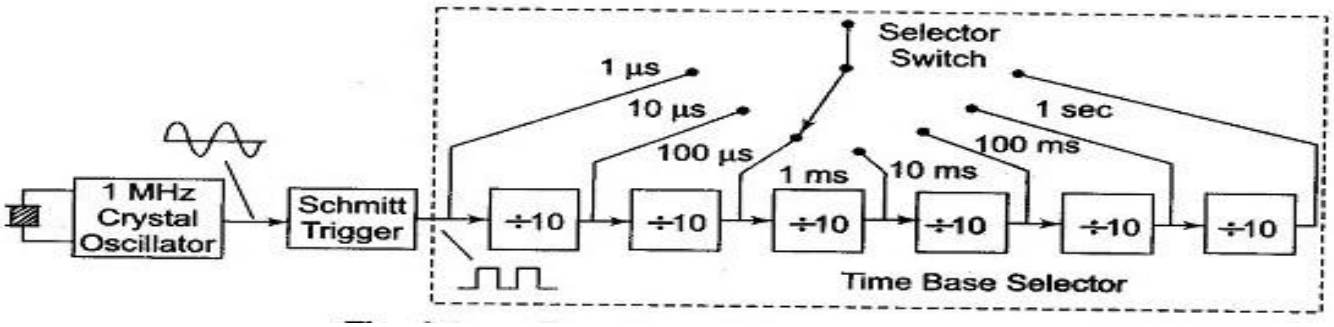

Figure 4.11: Time Base Selector

The circuit of Fig. 4.11 consists of a clock oscillator having a 1 MHz frequency. The output of the Schmitt trigger is 10^6 pulses per second and this point corresponds to a time of 1 microsecond. Hence by using a 6 decade frequency divider, a time base with a range of 1μs—10μs—100μs —1ms—10ms—100ms—1s can be selected using a selector switch.

4.7.2 Measurement of Time (Period Measurement):

In some cases it is necessary to measure the time period rather than the frequency. This is especially true in the measurement of frequency in the low frequency range. To obtain good accuracy at low frequency, we should take measurements of the period, rather than make direct frequency measurements. The circuit used for measuring frequency (Fig. 4.10) can be used for the measurement of time period if the counted signal and gating signal are interchanged.

Figure 4.12 shows the circuit for measurement of time period. The gating signal is derived from the unknown input signal, which now controls the enabling and disabling of the main gate. The number of pulses which occur during one period of the unknown signal are counted and displayed by the decade counting assemblies. The only disadvantage is that for measuring the frequency in the low frequency range, the operator has to calculate the frequency from the time by using the equation f = 1/T.

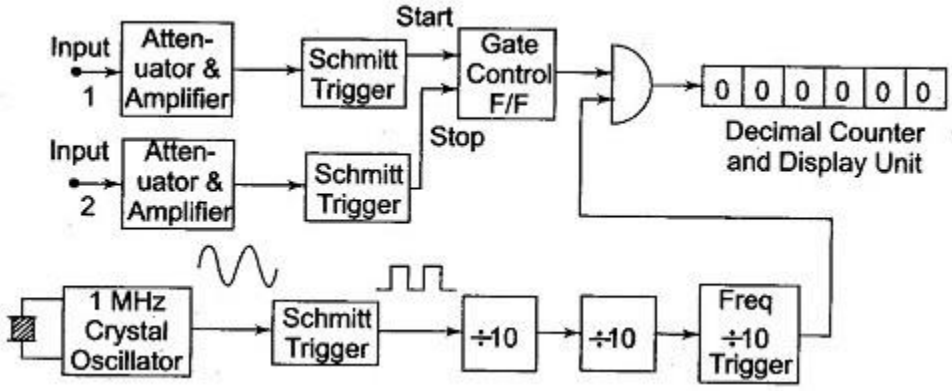

Figure 4.12: Basic Block diagram of time measurement

For example, when measuring the period of a 60 Hz frequency, the electronic counter might display 16.6673 ms, whence the frequency is

$$f = 1/T = \frac{1}{16.6673 \times 10^{-3}} = 59.9977 \text{ Hz}$$

The accuracy of the period measurement and hence of frequency can be greatly increased by using the multiple period average mode of operation. In this mode, the main gate is enabled for more than one period of the unknown signal. This is obtained by passing the unknown signal through one or more decade divider assemblies (DDAs) so that the period is extended by a factor of 10,000 or more.

Hence the digital display shows more digital of information, thus increasing accuracy. However, the decimal point location and measurement units are usually changed each time an additional decade divider is added, so that the display is always in terms of the period of one cycle of the input signal, even though the measurements may have lasted for 10,100 or more cycles.

Figure 4.13 show the multiple average mode of operation. In this circuit, five more decade dividing assemblies are added so that the gate is now enabled for a much longer interval of time than it was with single DDA.

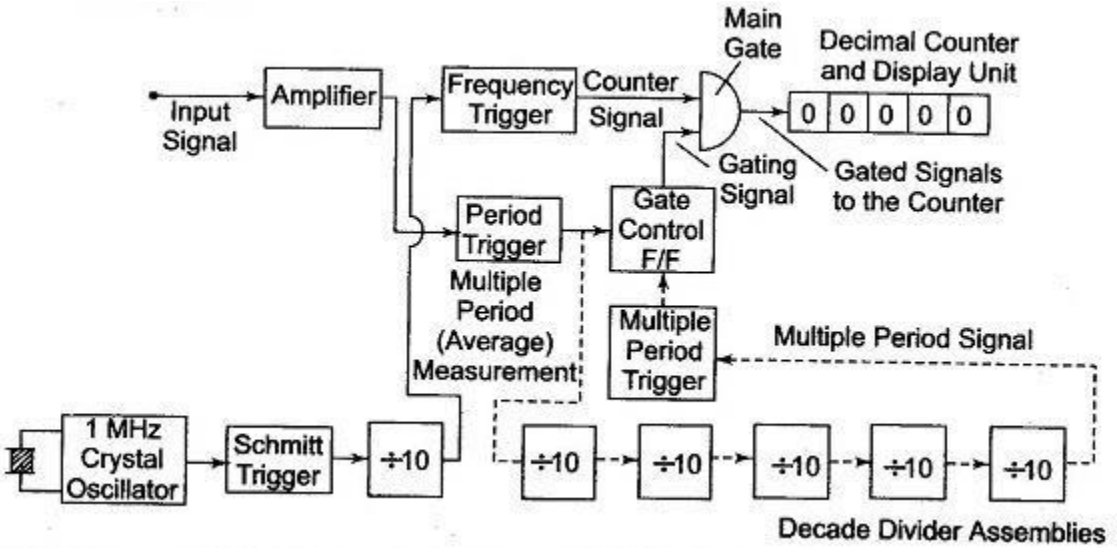

Figure 4.13: Block diagram of a single and multiple period (average) measurement.

4.8 Function Generator

A Function Generator Block Diagram produces different waveforms of adjustable frequency. The common output waveforms are the sine, square, triangular and sawtooth waves. The frequency may be adjusted, from a fraction of a Hertz to several hundred kHz.

The various outputs of the generator can be made available at the same time. For example, the generator can provide a square wave to test the linearity of an amplifier and simultaneously provide a sawtooth to drive the horizontal deflection amplifier of the CRO to provide a visual display.

Capability of Phase Lock: The function generator can be phase locked to an external source. One function generator can be used to lock a second function generator, and the two output signals can be displaced in phase by adjustable amount.

In addition, the fundamental frequency of one generator can be phase locked to a harmonic of another generator, by adjusting the amplitude and phase of the harmonic, almost any waveform can be generated by addition. The function generator can also be phase locked to a frequency standard and all its output waveforms will then have the same accuracy and stability as the standard source.

The Function Generator Block Diagram is illustrated in Fig. 4.14. Usually the frequency is controlled by varying the capacitor in the LC or RC circuit. In this instrument the frequency is controlled by varying the magnitude of current which drives the integrator. The instrument produces sine, triangular and square waves with a frequency range of 0.01 Hz to 100 kHz.

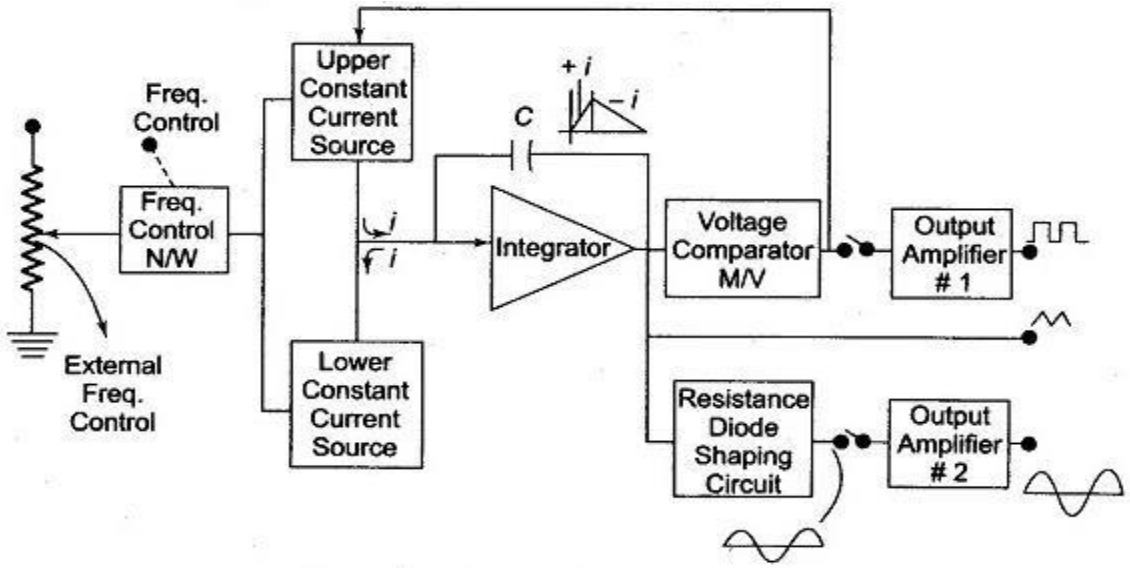

Figure 4.14: Function generator

The frequency-controlled voltage regulates two current sources. The upper current source supplies constant current to the integrator whose output voltage increases linearly with time, according to the equation of the output signal voltage.

$$e_{out} = -\frac{1}{C}\int_0^t i\,dt$$

An increase or decrease in the current increases or decreases the slope of the output voltage and hence controls the frequency. The voltage comparator multivibrator changes states at a pre-determined maximum level of the integrator output voltage. This change cuts off the upper current supply and switches on the lower current supply.

The lower current source supplies a reverse current to the integrator, so that its output decreases linearly with time. When the output reaches a predetermined minimum level, the voltage comparator again changes state and switches on the upper current source.

The output of the integrator is a triangular waveform whose frequency is determined by the magnitude of the current supplied by the constant current sources.

The comparator output delivers a square wave voltage of the same frequency. The resistance diode network alters the slope of the triangular wave as its amplitude changes and produces a sine wave with less than 1% distortion.

4.9 Wheatstone Bridge:

Introduction: A Bridge Circuit in its simplest form consists of a network of four resistance arms forming a closed circuit, with a dc source of current applied to two opposite junctions and a current detector connected to the other two junctions, as shown in Fig. 4.15.

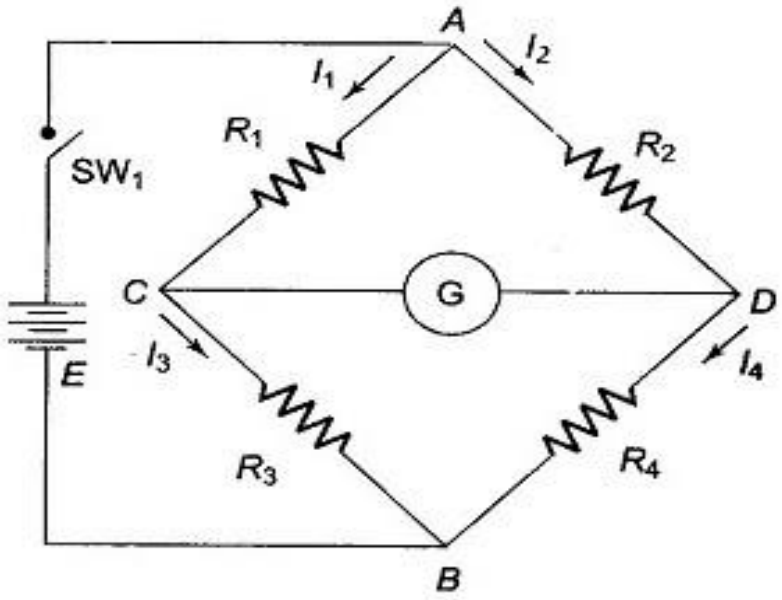

Figure 4.15: Wheatstone bridge

Wheatstone Bridge Circuit are extensively used for measuring component values such as R, L and C. Since the bridge circuit merely compares the value of an unknown component with that of an accurately known component (a standard), its measurement accuracy can be very high. This is because the readout of this comparison is based on the null indication at bridge balance, and is essentially independent of the characteristics of the null detector. The measurement accuracy is therefore directly related to the accuracy of the bridge component and not to that of the null indicator used.

The basic dc bridge is used for accurate measurement of resistance and is called Wheatstone's bridge.

4.9.1 Wheatstone Bridge Circuit (Measurement of Resistance):

Wheatstone's bridge is the most accurate method available for measuring resistances and is popular for laboratory use. The circuit diagram of a typical Wheatstone Bridge Circuit is given in Fig. 4.15. The source of emf and switch is connected to points A and B, while a sensitive current indicating meter, the galvanometer, is connected to points C and D. The galvanometer is a sensitive microammeter, with a zero centre scale. When there is no current through the meter, the galvanometer pointer rests at 0, i.e. mid-scale. Current in one direction causes the pointer to deflect on one side and current in the opposite direction to the other side.

When SW_1 is closed, current flows and divides into the two arms at point A, i.e. I_1 and I_2. The bridge is balanced when there is no current through the galvanometer, or when the potential difference at points C and D is equal, i.e. the potential across the galvanometer is zero.
To obtain the bridge balance equation, we have from the Fig. 4.15.

$$I_1R_1 = I_2R_2 \tag{4.5}$$

For the galvanometer current to be zero, the following conditions should be satisfied.

$$I_1 = I_3 = \frac{E}{R_1 + R_3} \tag{4.6}$$

$$I_2 = I_4 = \frac{E}{R_2 + R_4} \tag{4.7}$$

Substituting in Eq. (4.2)

$$\frac{E \times R_1}{R_1 + R_3} = \frac{E \times R_2}{R_2 + R_4}$$

$$R_1 \times (R_2 + R_4) = (R_1 + R_3) \times R_2$$

$$R_1 R_2 + R_1 R_4 = R_1 R_2 + R_3 R_2$$

$$R_4 = \frac{R_2 R_3}{R_1}$$

This is the equation for the bridge to be balanced.

In a practical Wheatstone Bridge Circuit, at least one of the resistance is made adjustable, to permit balancing. When the bridge is balanced, the unknown resistance (normally connected at R_4) may be determined from the setting of the adjustable resistor, which is called a standard resistor because it is a precision device having very small tolerance.
Hence

$$R_x = \frac{R_2 R_3}{R_1} \tag{4.8}$$

4.9.2 Sensitivity of a Wheatstone Bridge

When the bridge is in an unbalanced condition, current flows through the galvanometer, causing a deflection of its pointer. The amount of deflection is a function of the sensitivity of the galvanometer. Sensitivity can be thought of as deflection per unit current. A more sensitive galvanometer deflects by a greater amount for the same current. Deflection may be

expressed in linear or angular units of measure, and sensitivity can be expressed in units of S = mm/μA or degree/μA or radians/μA.

Therefore it follows that the total deflection D is D = S x I, where S is defined above and I is the current in microamperes.

4.9.3 Unbalanced Wheatstone's Bridge

To determine the amount of deflection that would result for a particular degree of unbalance, general circuit analysis can be applied, but we shall use Thevenin's theorem.

Since we are interested in determining the current through the galvanometer, we wish to find the Thevenin's equivalent, as seen by the galvanometer.

Thevenin's equivalent voltage is found by disconnecting the galvanometer from the Wheatstone Bridge Circuit, as shown in Fig. 4.16, and determining the open-circuit voltage between terminals a and b.

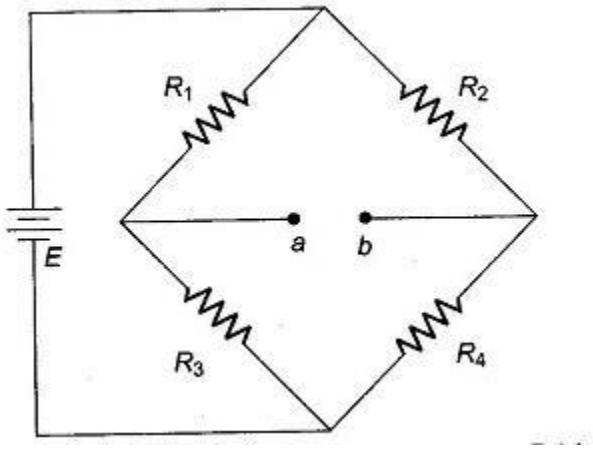

Figure 4.16: Unbalanced Wheatstone's bridge

Applying the voltage divider equation, the voltage at point a can be determined as follows

$$E_a = \frac{E \times R_3}{R_1 + R_3} \quad \text{and at point } b, \quad E_b = \frac{E \times R_4}{R_2 + R_4}$$

Therefore, the voltage between a and b is the difference between E_a and E_b, which represents Thevenin's equivalent voltage.

$$E_{th} = E_{ab} = E_a - E_b = \frac{E \times R_3}{R_1 + R_3} - \frac{E \times R_4}{R_2 + R_4}$$

Therefore

$$E_{ab} = E\left(\frac{R_3}{R_1 + R_3} - \frac{R_4}{R_2 + R_4}\right)$$

Thevenin's equivalent resistance can be determined by replacing the voltage source E with its internal impedance or otherwise short-circuited and calculating the resistance looking into terminals a and b. Since the internal resistance is assumed to be very low, we treat it as 0 Ω. Thevenin's equivalent resistance circuit is shown in Fig. 4.17.

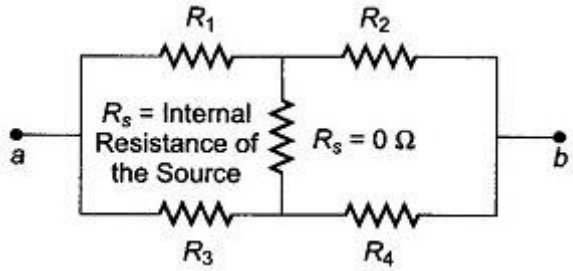

Figure 4.17: Thevenin's resistance

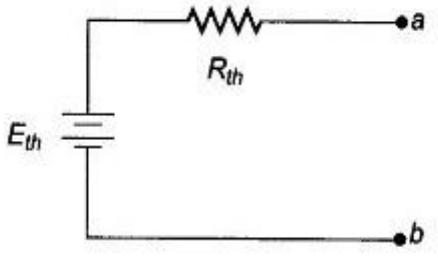

Figure 4.18: Thevenin's equivalent

The equivalent resistance of the circuit is $R_1//R_3$ in series with $R_2//R_4$ i.e. $R_1//R_3 + R_2//R_4$.

$$R_{th} = \frac{R_1 R_3}{R_1 + R_3} + \frac{R_2 R_4}{R_2 + R_4}$$

Therefore, Thevenin's equivalent circuit is given in Fig. 4.18. Thevenin's equivalent circuit for the bridge, as seen looking back at terminals a and b in Fig. 4.16, is shown in Fig. 4.18.

If a galvanometer is connected across the terminals a and b of Fig.4.16, or its Thevenin equivalent Fig. 4.18 it will experience the same deflection at the output of the bridge. The magnitude of current is limited by both Thevenin's equivalent resistance and any resistance connected between a and b. The resistance between a and b consists only of the galvanometer resistance R_g. The deflection current in the galvanometer is therefore given by

$$I_g = \frac{E_{th}}{R_{th} + R_g} \qquad (4.9)$$

4.9.4 Slightly Unbalanced Wheatstone's Bridge

If three of the four resistor in a bridge are equal to R and the fourth differs by 5% or less, we can develop an approximate but accurate expression for Thevenin's equivalent voltage and resistance.

Consider the circuit in Fig. 4.19.

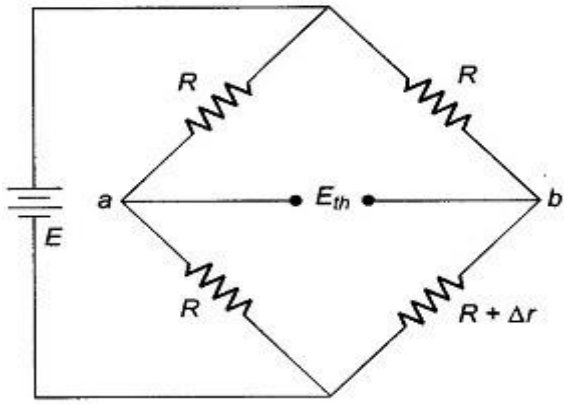

Figure 4.19: Slightly unbalanced Wheatstone's bridge

The voltage at point a is

$$E_a = \frac{E \times R}{R+R} = \frac{E \times R}{2R} = \frac{E}{2}$$

The voltage at point b is

$$E_b = \frac{R+\Delta r \times E}{R+R+\Delta r} = \frac{E(R+\Delta r)}{2R+\Delta r}$$

Thevenin's equivalent voltage between a and b is the difference between these voltages.

$$E_{th} = E_a - E_b = E\left(\frac{(R+\Delta r)}{2R+\Delta r} - \frac{1}{2}\right)$$

$$= E\left(\frac{2(R+\Delta r)-(2R+\Delta r)}{2(2R+\Delta r)}\right)$$

$$= E\left(\frac{2R+2\Delta r-2R-\Delta r}{4R+2\Delta r}\right)$$

$$= E\left(\frac{\Delta r}{4R+2\Delta r}\right)$$

Therefore

If Δ r is 5% of R or less, Δ r in the denominator can be neglected without introducing appreciable error. Therefore, Thevenin's voltage is

$$E_{th} = \frac{E \times \Delta r}{4R} = E\left(\frac{\Delta r}{4R}\right)$$

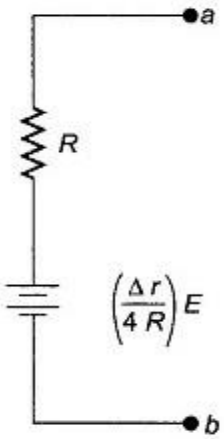

Figure 4.20: Thevenin's equivalent of slightly unbalanced Wheatstone's bridge

The equivalent resistance can be calculated by replacing the voltage source with its internal impedance (for all practical purpose short-circuit). The Thevenin's equivalent resistance is given by

$$R_{th} = \frac{R \times R}{R+R} + \frac{R(R+\Delta r)}{R+R+\Delta r}$$

$$= \frac{R}{2} + \frac{R(R+\Delta r)}{2R+\Delta r}$$

Again, if Δr is small compared to R, Δ r can be neglected. Therefore, R R

$$R_{th} = \frac{R}{2} + \frac{R}{2} = R$$

Using these approximations, the Thevenin's equivalent circuit is as shown in Fig. 4.20. These approximate equations are about 98% accurate if Δr ≤ 0.05 R.

4.9.5 Application of Wheatstone's Bridge

A Wheatstone bridge may be used to measure the dc resistance of various types of wire, either for the purpose of quality control of the wire itself, or of some assembly in which it is used. For example, the resistance of motor windings, transformers, solenoids, and relay coils can be measured.

Wheatstone Bridge Circuit is also used extensively by telephone companies and others to locate cable faults. The fault may be two lines shorted together, or a single line shorted to ground.

4.9.6 Limitations of Wheatstone's Bridge

For low resistance measurement, the resistance of the leads and contacts becomes significant and introduces an error. This can be eliminated by Kelvin's Double bridge.

For high resistance measurements, the resistance presented by the bridge becomes so large that the galvanometer is insensitive to imbalance. Therefore, a power supply has to replace the battery and a dc VTVM replaces the galvanometer. In the case of high resistance measurements in mega ohms, the Wheatstone's bridge cannot be used.

Another difficulty in Wheatstone Bridge Circuit is the change in resistance of the bridge arms due to the heating effect of current through the resistance. The rise in temperature causes a change in the value of the resistance, and excessive current may cause a permanent change in value.

4.10 Comparison Bridge:

There are two types of Comparison Bridge:

- **Capacitance Comparison Bridge**
- **Inductance Comparison Bridge**

4.10.1 Capacitance Comparison Bridge

Figure 4.21 shows the circuit of a capacitance comparison bridge. The ratio arms R_1, R_2 are resistive. The known standard capacitor C_3 is in series with R_3. R_3 may also include an added variable resistance needed to balance the bridge. C_x is the unknown capacitor and R_x is the small leakage resistance of the capacitor. In this case an unknown capacitor is compared with a standard capacitor and the value of the former, along with its leakage resistance, is obtained.

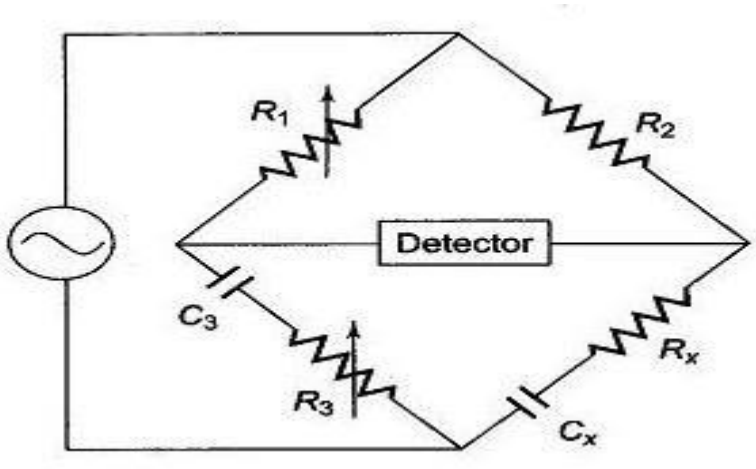

Figure 4.21: Capacitance comparison bridge

Hence,

$$Z_1 = R_1$$
$$Z_2 = R_2$$
$$Z_3 = R_3 \text{ in series with } C_3 = R_3 - j/\omega C_3$$
$$Z_x = R_x \text{ in series with } C_x = R_x - j/\omega C_x$$

The condition for balance of the bridge is

$$Z_1 Z_x = Z_2 Z_3$$

$$\text{i.e.} \qquad R_1\left(R_x - \frac{j}{\omega C_x}\right) = R_2\left(R_3 - \frac{j}{\omega C_3}\right)$$

$$\therefore \qquad R_1 R_x - \frac{j R_1}{\omega C_x} = R_2 R_3 - \frac{j R_2}{\omega C_3}$$

Two complex quantities are equal when both their real and their imaginary terms are equal. Therefore,

$$\text{i.e.} \qquad R_1 R_x = R_2 R_3 \qquad \therefore R_x = \frac{R_2 R_3}{R_1} \tag{4.10}$$

$$\text{and} \qquad \frac{R_1}{\omega C_x} = \frac{R_2}{\omega C_3} \qquad C_x = \frac{C_3 R_1}{R_2} \tag{4.11}$$

Since R_3 does not appear in the expression for C_x, as a variable element it is an obvious choice to eliminate any interaction between the two balance controls.

4.10.2 Inductance Comparison Bridge

Figure 4.22 gives a schematic diagram of an inductance comparison bridge. In this, values of the unknown inductance L_x and its internal resistance R_x are obtained by comparison with the standard inductor and resistance, i.e. L_3 and R_3.

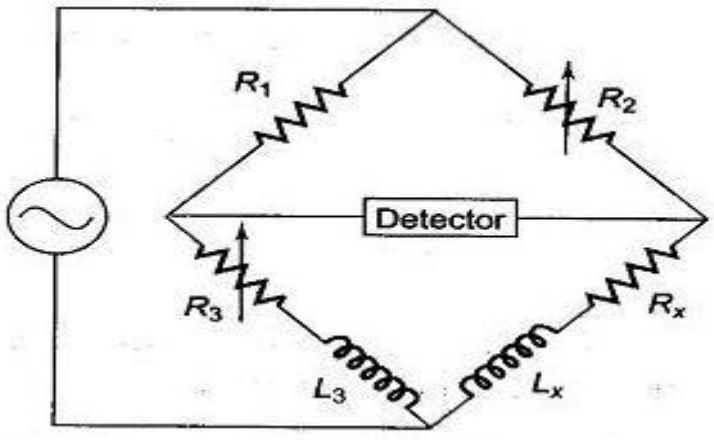

Figure 4.22: Inductance comparison bridge

The equation for balance condition is

$$Z_1 Z_x = Z_2 Z_3$$

The inductive balance equation yields

$$L_x = \frac{L_3 R_2}{R_1} \tag{4.12}$$

and resistive balance equations yields

$$R_x = \frac{R_2 R_3}{R_1} \tag{4.13}$$

In this bridge R_2 is chosen as the inductive balance control and R_3 as the resistance balance control. (It is advisable to use a fixed resistance ratio and variable standards). Balance is obtained by alternately varying L_3 or R_3. If the Q of the unknown reactance is greater than the standard Q, it is necessary to place a variable resistance in series with the unknown reactance to obtain balance.

If the unknown inductance has a high Q, it is permissible to vary the resistance ratio when a variable standard inductor is not available.

4.11 Wien's Bridge:

The Wien Bridge Circuit Diagram shown in Fig. 4.23 has a series RC combination in one arm and a parallel combination in the adjoining arm. Wien's bridge in its basic form, is designed to measure frequency. It can also be used for the measurement of an unknown capacitor with great accuracy.

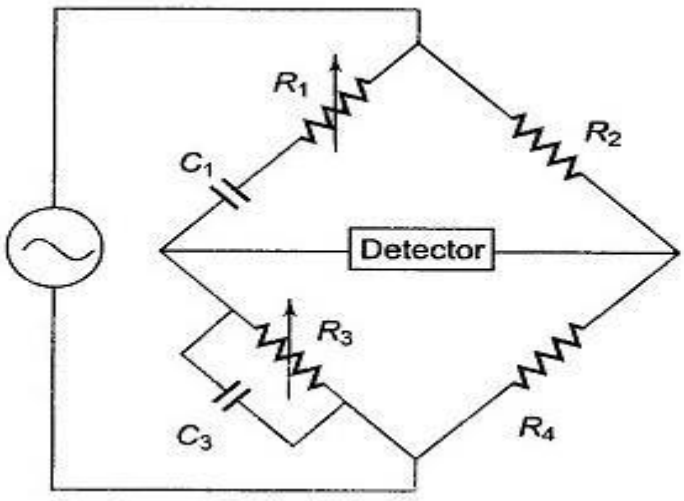

Figure 4.23: Wien's bridge

The impedance of one arm is

$$Z_1 = R_1 - j/\omega C_1$$

The admittance of the parallel arm is

$$Y_3 = 1/R_3 + j\,\omega\,C_3$$

Using the bridge balance equation,

we have

$$Z_1\,Z_4 = Z_2\,Z_3$$

Therefore,

$$Z_1\,Z_4 = Z_2/Y_3, \text{ i.e. } Z_2 = Z_1\,Z_4\,Y_3$$

$$R_2 = R_4\left(R_1 - \frac{j}{\omega C_1}\right)\left(\frac{1}{R_3} + j\omega C_3\right)$$

$$R_2 = \frac{R_1 R_4}{R_3} - \frac{j R_4}{\omega C_1 R_3} + j\,\omega\,C_3 R_1 R_4 + \frac{C_3 R_4}{C_1}$$

$$R_2 = \left(\frac{R_1 R_4}{R_3} + \frac{C_3 R_4}{C_1}\right) - j\left(\frac{R_4}{\omega C_1 R_3} - \omega C_3 R_1 R_4\right)$$

Equating the real and imaginary terms we have

$$R_2 = \frac{R_1 R_4}{R_3} + \frac{C_3 R_4}{C_1} \text{ and } \frac{R_4}{\omega C_1 R_3} - \omega\,C_3 R_1 R_4 = 0$$

Therefore $$\frac{R_2}{R_4} = \frac{R_1}{R_3} + \frac{C_3}{C_1} \qquad (4.14)$$

and $$\frac{1}{\omega C_1 R_3} = \omega\,C_3 R_1 \qquad (4.15)$$

$$\therefore \quad \omega^2 = \frac{1}{C_1 R_1 R_3 C_3}$$

$$\omega = \frac{1}{\sqrt{C_1 R_1 C_3 R_3}}$$

as $$\omega = 2\,\pi f$$

$$\therefore \quad f = \frac{1}{2\pi\sqrt{C_1 R_1 C_3 R_3}} \qquad (4.16)$$

The two conditions for bridge balance, (4.14) and (4.16), result in an expression determining the required resistance ratio R_2/R_4 and another expression determining the

frequency of the applied voltage. If we satisfy Eq. (4.14) and also excite the bridge with the frequency of Eq. (4.16), the bridge will be balanced.

In most Wien Bridge Circuit Diagram, the components are chosen such that $R_1 = R_3 = R$ and $C_1 = C_3 = C$. Equation (4.14) therefore reduces to $R_2/R_4 = 2$ and Eq. (4.16) to $f=1/2\pi RC$, which is the general equation for the frequency of the bridge circuit.

The bridge is used for measuring frequency in the audio range. Resistances R_1 and R_3 can be ganged together to have identical values. Capacitors C_1 and C_3 are normally of fixed values.

The audio range is normally divided into 20 — 200 — 2 k — 20 kHz ranges. In this case, the resistances can be used for range changing and capacitors C_1 and C3 for fine frequency control within the range. The Wien Bridge Circuit Diagram can also be used for measuring capacitances. In that case, the frequency of operation must be known.

The bridge is also used in a harmonic distortion analyzer, as a Notch filter, and in audio frequency and radio frequency oscillators as a frequency determining element. An accuracy of 0.5% — 1% can be readily obtained using this bridge. Because it is frequency sensitive, it is difficult to balance unless the waveform of the applied voltage is purely sinusoidal.