EAST POINT COLLEGE OF ENGINEERING & TECHNOLOGY

Department of Electronics and Communication Engineering

Question bank

Sem/Sec: III (A & B) **Subject: DSD** **Subject Code: BEC302**

Module-1

1. Define Quine McClusky method and solve the following Boolean expression using Quine-McClusky

i) D = f(a,b,c,d) = ∑m(0,1,2,3,6,7,8,9,14,15)

ii) K = f(w,x,y,z) = ∑m(1,3,13,15)+∑d(8,9,10,11)

2. Simplify the following Boolean expression using K-map

i) X= f(a,b,c,d) = πM(1,2,3,4,9,10) + πd(0,14,15)

ii) Y = f(w,x,y,z) = ∑m(6,7,9,10,13) + ∑d(1,4,5,11,15)

3. Define canonical form representation and solve the following equation using canonical form

i) P = f(a,b,c) = ab'+ac'+bc

ii) G = f(w,x,y,z) = w'x+yz'

iii) H = f(a,b,c,d) = (a+b'+c)(a'+d)

4. Simplify the Boolean expression and identify the prime implicants and essential prime implicants

i) Y = f(a,b,c,d) = ∑m(1,5,7,8,9,10,11,13,15)

ii) Z = f(a,b,c,d) = πM(0,2,3,8,9,10,12,14)

5. Simplify (A,B,C,D) = ∑m(1,2,3,5,6,7,9,10,11) using K – map to get minimum SOP expression as well as minimum POS expression. Among the two expressions, find out which one requires lesser number of gates implementation?

6. What are combinational circuits? Give an example. Explain combinational circuit with block Diagram.

Module-2

1. Explain binary adders with k-map and logical representation of equations for sum and carry.
2. Explain carry look ahead adder with general and sigma block. Also explain working of decimal adder with neat block diagram (take example of BCD addition).
3. What are comparator circuits? Design 2-bit magnitude comparator.
4. Implement a full adder using PAL. Implement f1(a b c d)= ∑m(0 1 2 5 7), f2(a b c d) = ∑m(1 2 4 6) using a PROM.
5. Realize the boolean expression using 3:8 decoder and two OR gates
   a) f(a b c) = ∑m(1 2 4 5)
   b) f(x y z) = ∑m(1 5 7)
6. Implement Q= (w x y z) = ∑m(0 2 4 5 7 9 10 14) using two 4:1 MUX with variable w, z connected to their select lines in the first level and 2:1 MUX with y variable connected to its select lines in the second level .

Module-3

1. What are registers? Explain any two classification of registers with neat diagram.
2. Explain the master-slave JK flip-flop with help of circuit diagram and waveforms.
3. Design a 4-bit binary ripple-up counter using positive-edge triggered JK flip-flop.
4. Explain positive edge triggered D flip-flop with help of circuit diagram and waveforms.
5. Design 3 bit synchronous up counter using JK flip-flop.
6. Obtain characteristics equation for the following flip-flop

    a) JK
    b) SR
    c) T
    d) D
7. Design a synchronous mod-6 counter using clocked JK flip-flop for the sequence 0 2 3 6 5 1.

Module-4

1. Explain the structure of Verilog module using example.
2. Explain the different styles of descriptions in Verilog.
3. Write a note on Verilog data types.
4. Write a Verilog code using Structural, data flow and behavioral style of description for-
    a) Full adder
    b) 8:1 Mux
5. Write a note on Arithmetic and shift, rotate and logical relational operators with example.

Module-5

1. Write a note on Signal assignment and variable assignment with example.
2. Write a note on constant declaration and constant assignment statement with example.
3. Explain sequential statements using example.
4. Explain different loop statements used in behavioral style of description.
5. Write a verilog code for 2:1 Mux using
    a) if- else statement.
    b) Conditional operator
6. Write a verilog code for
    a) ripple carry adder in structural description.
    b) 4- bit counter