EPC M2

Electronic and communication (Visvesvaraya Technological University)

2.1Biasing in MOSFET Amplifiers

Biasing: Establishing the desired DC voltages (V_{DS}) and currents (I_D) for the operation of the MOS amplifier.

MOSFET Regions of Operation

There are three regions of operation in the MOSFET

– When $V_{GS} < V_T$, no conductive channel is present and $I_D = 0$, this is said to be *cutoff region.*

– If $V_{GS} < V_T$ and $V_{DS} < V_{DS,sat}$, the device is in the *triode region* of operation. Increasing V_{DS} increases the lateral field in the channel, and hence the current. Increasing V_{GS} increases the transverse field and hence the inversion layer density, which also increases the current.

– If $V_{GS} < V_T$ and $V_{DS} > V_{DS,sat}$, the device is in the *saturation region* of operation. Since the drain end channel density has become small, the current is much less dependent on V_{DS}, but is still dependent on V_{GS}, since increased V_{GS} still increases the inversion layer density.

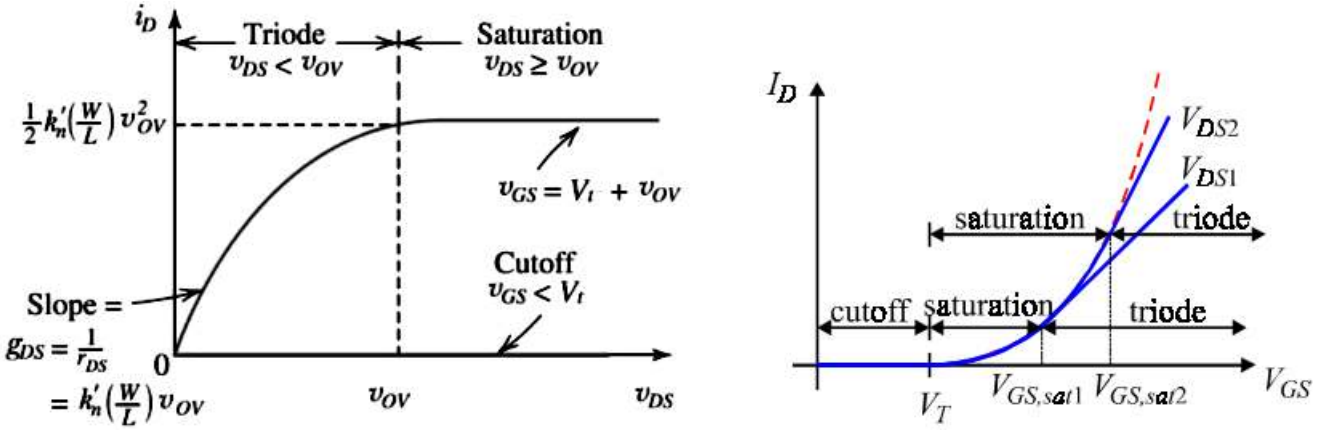


Fig.1 MOSFET Characteristic curves

As I_D is increased at fixed V_{DS}, no current flows until the inversion layer is established. For V_{GS} slightly above threshold, the device is in saturation since there is little inversion layer density (the drain end is pinched off). As V_{GS} increases, a point is reached where the drain end is no longer pinched off, and the device is in the triode region. A larger V_{DS} value postpones the point of transition to triode.

Common ways of biasing

1. Biasing by fixing VGS
2. Biasing by fixing VG and connecting a resistance in the Source
3. Biasing using a Drain-to-Gate Feedback Resistor

2.1.1 Biasing by fixing VGS

In this biasing technique, a suitable voltage supply is applied between gate and source as shown in the circuit diagram Fig. 2(a).

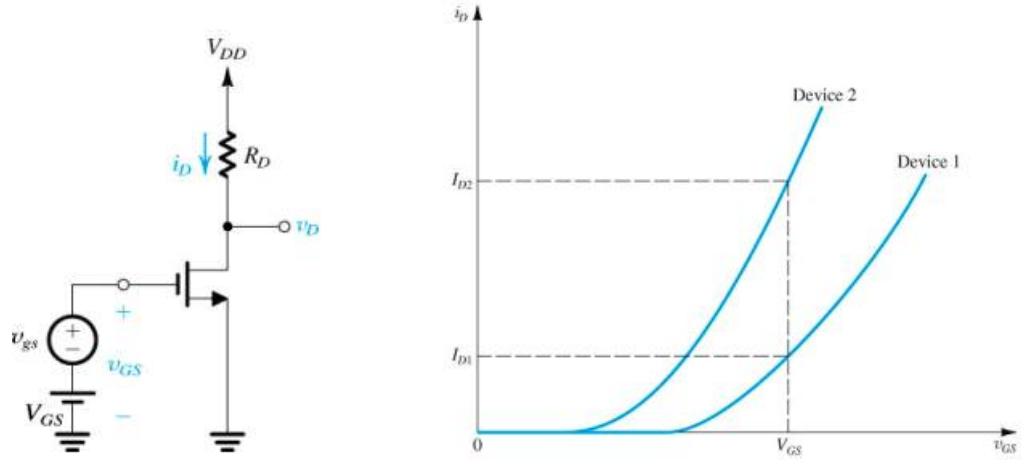


Fig.2 (a) Fixing V_{GS} circuit **(b) graph showing large variability in I_D values**

Bias point (i.e., I_D and V_{DS}) should be stable irrespective to variations in parameter values like, μ_n, Cox, (W/L), V_t due to temperature and/or manufacturing variability.

I_D in saturation region is given by

$$I_D = 0.5\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Where, W = Width of channel, L = Length of the channel, μ_n = Mobility of electrons in the conduction channel, Cox = capacitance of oxide layer and V_t = threshold voltage

This method is NOT desirable as μ_n, Cox, (W/L) and V_t are drastically change due to temperature and/or manufacturing variability.

When the MOSFET device is changed (even using the same supplier), this method can result in a large variability in the value of ID. Devices 1 and 2 represent extremes among units of the same type. See Fig.2(b).

2.1.2 Biasing by fixing V_G and connecting a resistance in the Source

In this biasing technique, a suitable voltage supply V_G is applied to gate by connecting R_S between source and ground as shown in the fig.3(a).

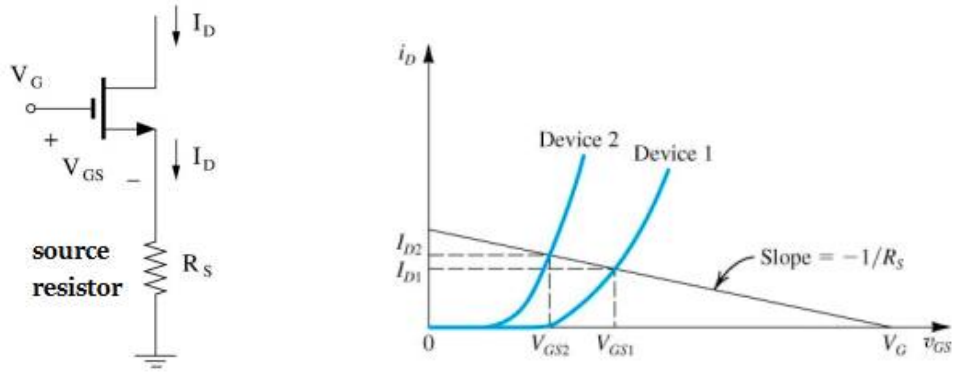


Fig.3 (a) Fixing V_G circuit **(b) graph showing small variability in I_D values**

Voltage drop across resistance R_S provides the biasing voltage V_G and no external source is required for biasing and this is the reason that it is called self-biasing.

$$V_G = V_{GS} + I_D R_S$$

Normally, V_G is much smaller than V_{GS}. In this case, R_S value creates *negative feedback* and it stabilizes the I_D current, hence it is called as *degenerative resistance*.

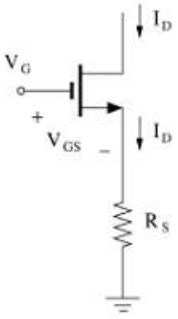
Even if V_G is larger than V_{GS}, I_D current value is determined by neglecting V_{GS}

$$V_{GS} - V_G + R_S I_D = 0 \Rightarrow I_D \approx V_G / R_S$$

From the fig. 3(b) it is illustrated that intersection of i_D and V_{GS} characteristic curve provide coordinates I_D and V_{GS} of bias point. It is observe that as in the case of fixed V_{GS}, variation of I_D (see difference between I_{D1} and I_{D2}) is much smaller.

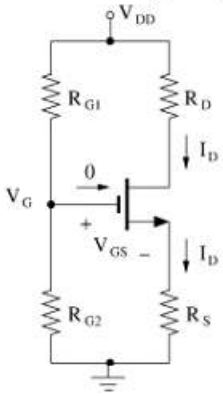
Examples of Bias with Source Degeneration

Basic Arrangement



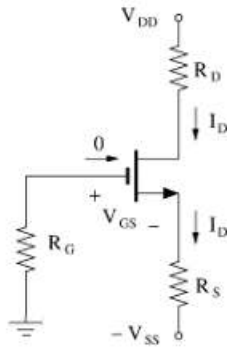
$$V_{GS} = V_G - R_S I_D$$

Bias with single supply



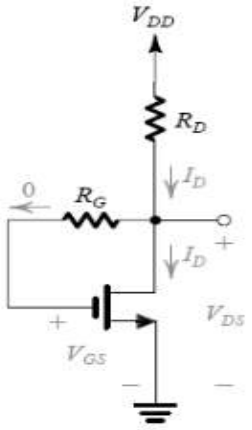
$$V_{GS} = V_G - R_S I_D$$

Bias with two supply



$$V_{GS} = V_{SS} - R_S I_D$$

2.1.3 Biasing using a Drain-to-Gate Feedback Resistor



A simple and effective biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in figure.

Here the large feedback resistance R_G *(usually in the M Ω range) forces the dc voltage at the gate to be equal to that at* the drain (because $I_G = 0$).

Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

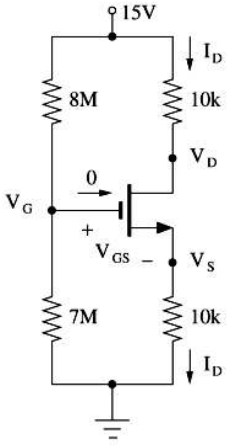
Which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D$$

In this case, R_G works just like the R_S which is to stabilize the bias current I_D in the event of changing V_{GS}. i,e, Note that there is no voltage dropped across R_G.

If I_D increases due to any reason, then V_{GS} *must decrease. The decrease in* V_{GS} *in turn* causes a decrease in I_D. Thus the negative feedback or degeneration provided by R_G *works to keep the value of* I_D *as* constant as possible.

Example: Find Bias point for $V_t = 1$ V and $\mu_n C_{ox}(W/L) = 1.0$ mA/V^2 (Ignore channel-length modulation).



Voltage divider ($I_G = 0$)

$V_G = (7)/(7+8)\times 15 = 7$ V

$$I_D = 0.5\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

GS-KVL: $V_G = V_{GS} + R_S I_D = 7$

$V_{OV} + V_t + R_S I_D = 7$

$V_{OV} + 1 + 10^4 \times (0.5\times 10^{-3} V_{OV}^2) = 7$

$5V_{OV}^2 + V_{OV} - 6 = 0 \rightarrow V_{OV} = 1$ V

$V_{GS} = V_{OV} + 1 = 2$ V

$V_S = V_G - V_{GS} = 7 - 2 = 5$ V

$I_D = V_S / R_S = 0.5$ mA

2.2 Small signal Operation and Modeling

The small-signal analysis is a mathematical approximation that allows us to see the effect of incremental changes on the inputs of an electrical device on its output characteristics.

2.2.1 DC bias point

For dc bias point I_D, we set the signal V_{GS} to be zero. Thus,

$$I_D = \frac{1}{2}k_n(V_{GS} - V_t)^2 = \frac{1}{2}k_n V_{OV}^2$$

Where neglected channel length modulation.

Here, $V_{OV} = V_{GS} - V_t$ is the overdrive voltage at which MOS is biased to operate. The DC voltage at the drain will be

$$V_D = V_{DD} - I_D R_D$$

To ensure saturation region,

$$V_D >> V_{GS} - V_t$$

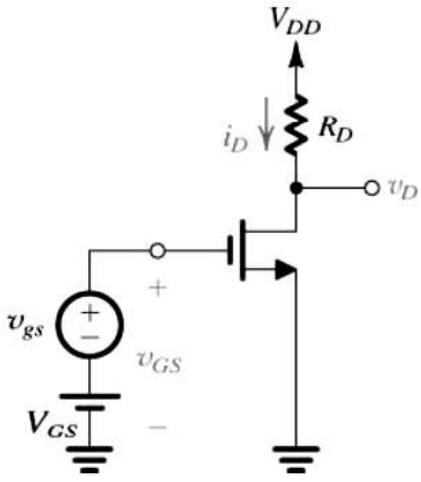


Fig. 4 Fixing V_{GS} circuit

2.2.2 Signal Current in Drain Terminal

Assume instantaneous input signal v_{gs} applied and total gate to source voltage is

$$v_{GS} = V_{GS} + v_{gs}$$

Resulting total instantaneous drain current is

$$i_D = \frac{1}{2}K_n'\left(\frac{W}{L}\right)(V_{GS} + v_{gs} - V_t)^2$$

$$i_D = \frac{1}{2}K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)^2 + K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)v_{gs} + \frac{1}{2}K_n'\left(\frac{W}{L}\right)v_{gs}^2$$

First component is the dc bias current, second is the current component directly proportional to the applied signal and last is proportional to square of input signal.

$$\frac{1}{2}K_n'\left(\frac{W}{L}\right)v_{gs}^2 \ll K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)v_{gs}$$

$$v_{gs} \ll 2(V_{GS} - V_t) \ll 2V_{OV}$$

$$i_D \approx I_D + i_d \quad \text{neglecting} \quad \text{last term.}$$

This is DC term plus a time-varying term, then from the above, one can see that the time-varying term is approximately given by

$$i_d = K_n'\left(\frac{W}{L}\right)(V_{GS} - V_t)v_{gs}$$

$$i_d \approx k_n(V_{GS} - V_t)v_{gs} = g_m v_{gs}$$

where quadratic term proportional to v_{gs}^2 has been ignored, and

$$g_m = k_n(V_{GS} - V_t) = k_n V_{OV} = \frac{i_d}{v_{gs}} = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{GS}=V_{GS}}$$

The above has the unit of conductance, and it is called the MOSFET trans-conductance.

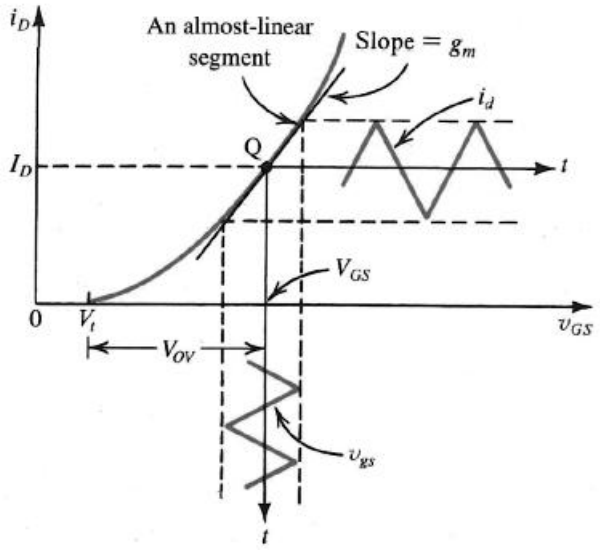


Fig. 5 Graphical depiction of the small signal analysis for MOSFET

2.2.3 Voltage Gain

From the fig. 4, the total instantaneous drain voltage v_D is

$$v_D = V_{DD} - R_D i_D$$

Under small signal condition:

$$v_D = V_{DD} - R_D(I_D + i_d)$$

$$v_D = V_D - R_D i_d$$

The signal component of this is

$$v_d = -i_d R_D = -g_m v_{gs} R_D$$

The voltage gain Av defined as

$$A_v \equiv \frac{v_d}{v_{gs}} = -g_m R_D$$

-ve sign indicates output is 180^o out of phase of applied input signal

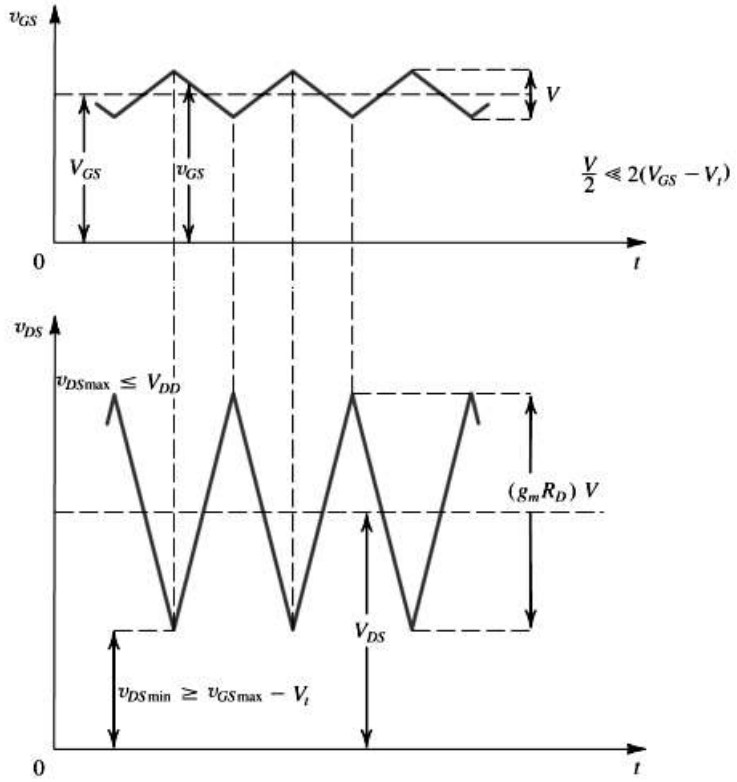


Fig. 6 Total instantaneous voltage v_{GS} and v_D

2.3 Small signal equivalent circuit models

By looking at the VI characteristic curve of the MOSFET, it is seen for incremental v_{ds}, the current i_d does not change. This relationship can be modeled by a current source. Moreover, the gate of the MOSFET is essentially an open circuit at DC. Hence, the small-signal equivalent-circuit model is presented in Figure 8(a).

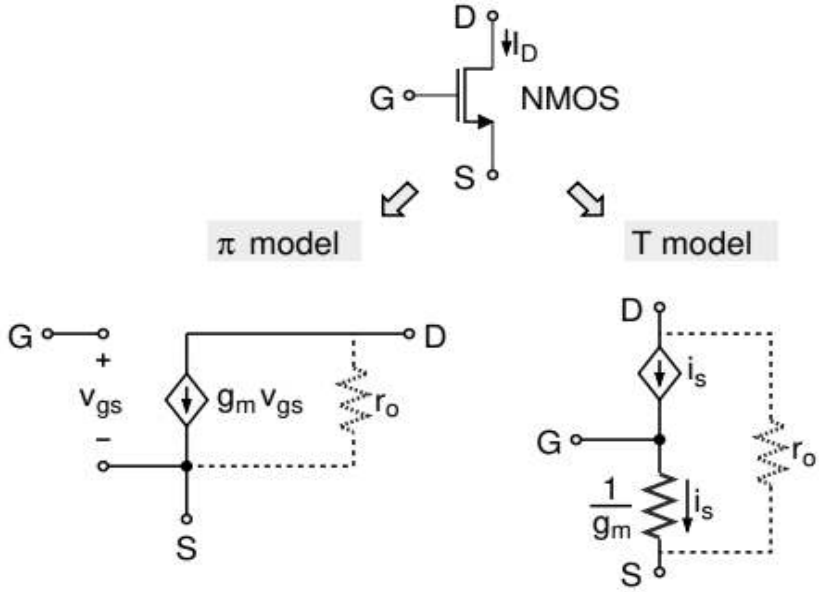


Fig. 7 MOS Symbol, Hybrid π- model and T model

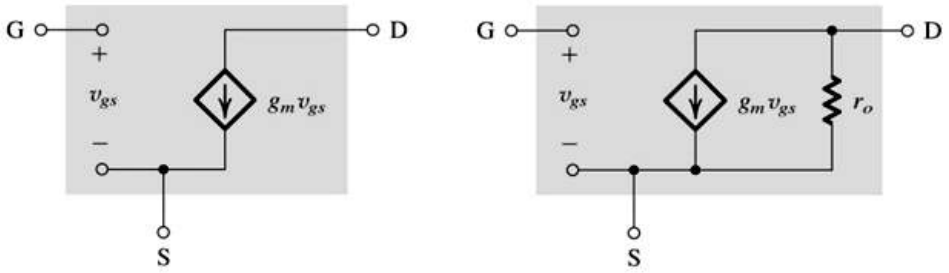


Fig.8 (a) neglecting the dependence of i_D on v_{DS} in the active region (b) including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A|/I_D$

$$I_D = \frac{1}{2} K_n' \left(\frac{W}{L}\right) v_{ov}^2$$

$$A_v = \frac{v_d}{v_{gs}} = -g_m (R_D \parallel r_o) \quad \{v_d = -i_d R_D = -g_m v_{gs} R_D\}$$

$$r_o = \frac{|V_A|}{I_D} \quad \text{where} \quad V_A = \frac{1}{\lambda}$$

r_o is introduced in parallel to controlled source is to improve small signal model shown in the Fig.(b).

2.4 Transconductance (g_m)

The transconductance can be looked at with more details by using

$$\begin{aligned} g_m &= k_n'(W/L)(V_{GS} - V_t) \\ &= k_n'(W/L)V_{OV} \\ &= \mu_n C_{ox}(W/L)V_{OV} \end{aligned}$$

The transconductance can be increased by increasing the W/L ratio, and also increasing the overdrive voltage V_{OV} . But increasing V_{OV} implies that the operating point for V_{DS} has to increase in order for the MOSFET to be in the saturation region. Also, by using the fact that,

$$I_D = \frac{1}{2} k_n V_{OV}^2 = \frac{1}{2} k_n' (W/L) V_{OV}^2 \qquad (1)$$

$$I_D = \frac{1}{2} k_n V_{OV}^2 = \frac{1}{2} k_n' (W/L) V_{OV}^2 \qquad (2)$$

or that $V_{OV} = \sqrt{2I_D/(k_n'(W/L))}$, then g_m inEq. (1)can be alternatively rewritten as

$$g_m = \sqrt{2k_n'(W/L)I_D} \qquad (3)$$

This implying that g_m is proportional to the square roots of the drain current I_D, and W/L.

At this point, note that

1. The trans-conductance g_m of a MOSFET is geometry dependent whereas that of the BJT is not.

2. The trans-conductance of a BJT is much larger than that of a MOSFET.

Since g_m is an incremental relationship, this can be shown graphically as in Figure 9.

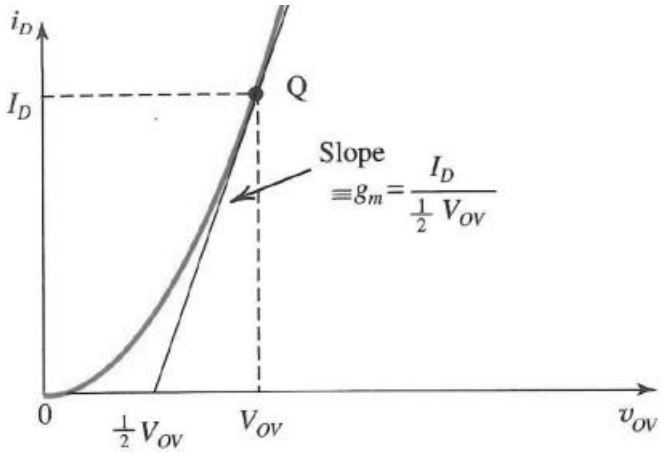


Fig. 9 incremental change in trans-conductance gm of a MOSFET

2.5 T- Equivalent circuit model

The hybrid-π equivalent-circuit model can be replaced by the T equivalent circuit model. The morphing of a hybrid-π model to the T model is shown in Figure.

1. The current source in the hybrid-π model can be split into two without affecting the branch current. This is seen from the morphing of Figure 10(a) to Figure 10(b).
2. Note that the gate current is zero. The point X can be connected to the gate input, and yet the gate current is zero because of KCL at X. This is indicated in Figure 10(c).
3. But the second voltage-controlled current source is just the voltage and current relation of a resistor whose resistance is $1/g_m$. Hence, it can be replaced by a resistor as shown in Figure 10(d).

Notice that in the T equivalent-circuit model, due to its construction, and KCL, the gate current is always zero, implying that its resistance is infinite.

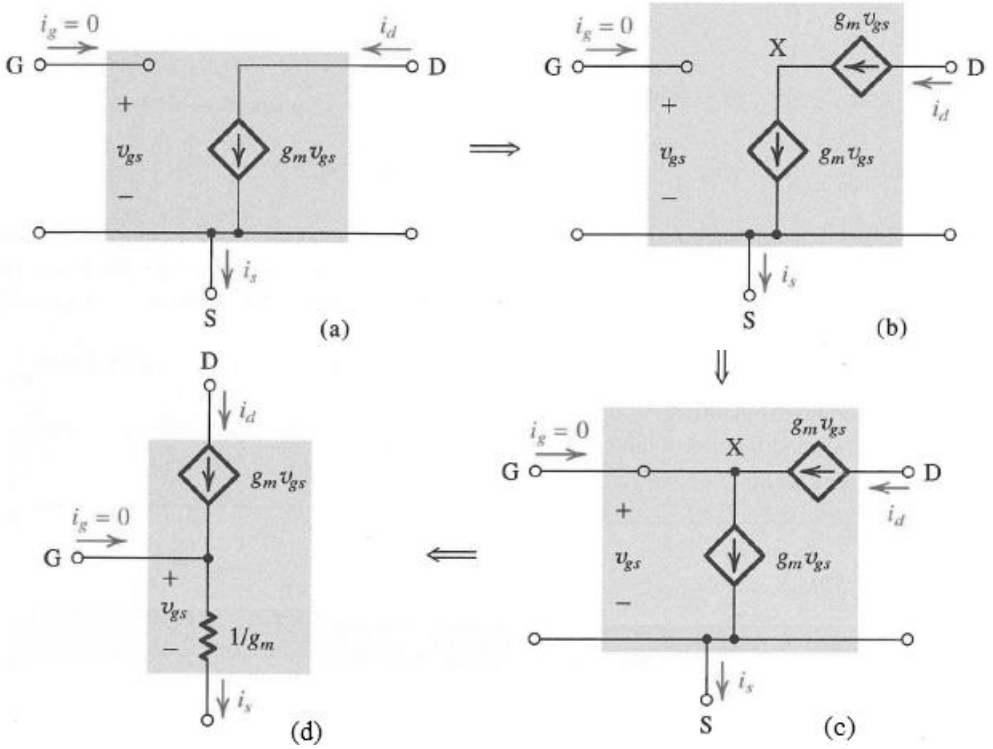


Figure 10 (a) and (b) early effect representing the T equivalent-circuit model

Also as the morphing of the hybrid-π equivalent-circuit model to the T equivalent-circuit model is unaffected by connecting a resistor between D and S, an r_o can be thus connected to account for the Early effect or the channel modulation effect as shown in Figure 10(a). Figure 10(b) is an alternative way of representing the T equivalent-circuit model, so that the gate current is always zero by KCL.

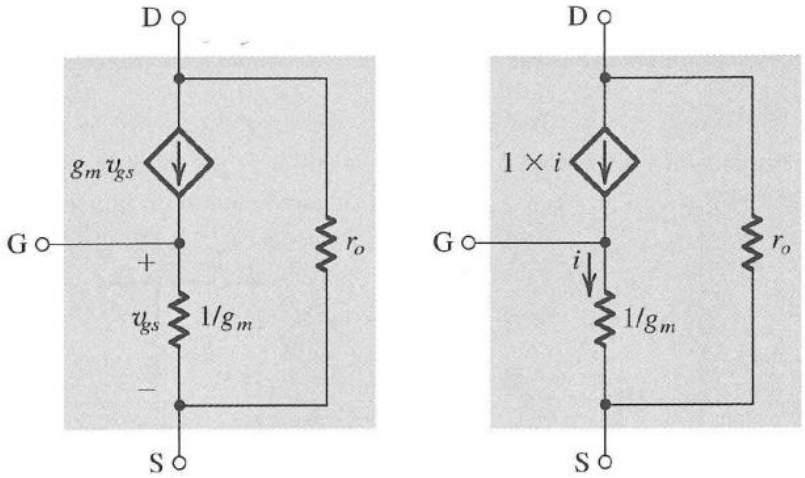


Fig.11 **(a)** **(b)**

The morphing of the π equivalent-circuit model to the T equivalent circuit model is still valid if a resistor is connected between the drain D and the source S. Hence, in fig11(a), r_o can be connected to account for the Early effect. Fig11(b) shows an alternative T model that is equivalent.

2.6 Single stage MOS amplifiers

2.6.1 Basic Configurations

Amplifier Configurations: 1) Common Source without source resistance 2) Common Source with a source resistance 3) Common gate 4) Common drain or source follower

Common Source (CS) Amplifier

- CS is most widely used configuration
- The source is grounded, making it common between input and output.
- We can use hybrid π model.
- In multistage amplifiers, the large gain is achieved from CS stage.

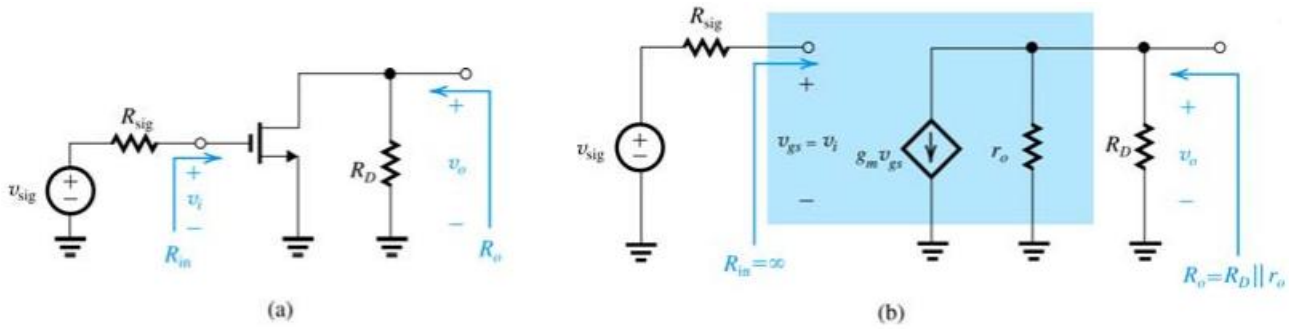


Fig.11 (a) NMOS Common-Source amplifier **(b) AC equivalent**

For R_o, set v_i=0

$$R_o = r_0 \| R_D$$

$$A_{vo} = -g_m(r_0 \| R_D)$$

$$R_i = \infty$$

Common Gate (CG) Amplifier

In CG Configuration, gate potential is at constant potential and the input signal is applied at the source terminal and the output is produced at the drain terminal. So that increase in input voltage V_{sig} in positive direction increases the negative gate source voltage. Due to I_D reduces, the drop I_DR_D also reduces.

Since $V_D = V_{DD} - I_DR_D$, the reduction in I_D results in an increase in output voltage

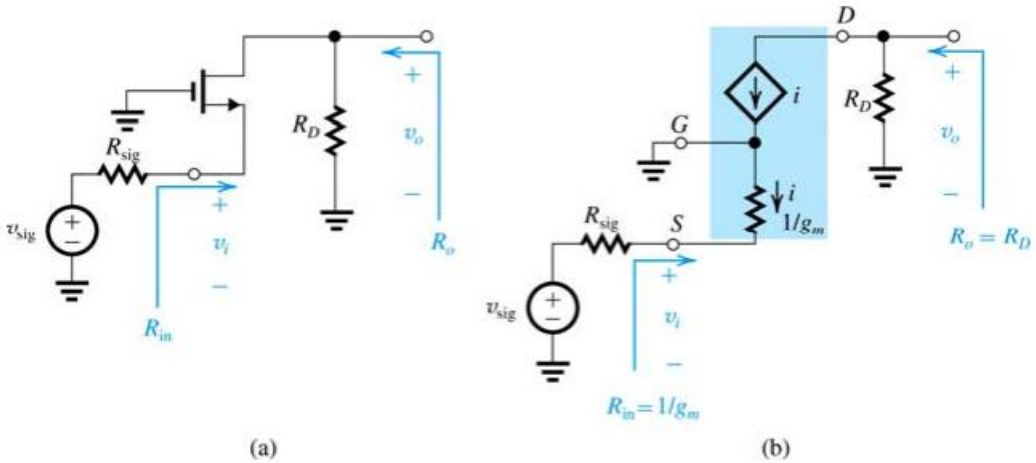


Figure 12(a) shows CG amplifier and figure (b) shows its small signal equivalent circuit.

By analizing the small signal equivalent circuit, the voltage gain of CG amplifier is given by,

$$A_v = g_m R_D$$

The input impedance of CG stage is relatively low only if the load resistance connected to the drain is small.

Common Drain (CD) Amplifier – Source Follower

In the CD Amplifier configuration, the drain terminal is at AC ground. The input is applied between the gate and drain terminals, while the output is measured between the source and drain terminal.

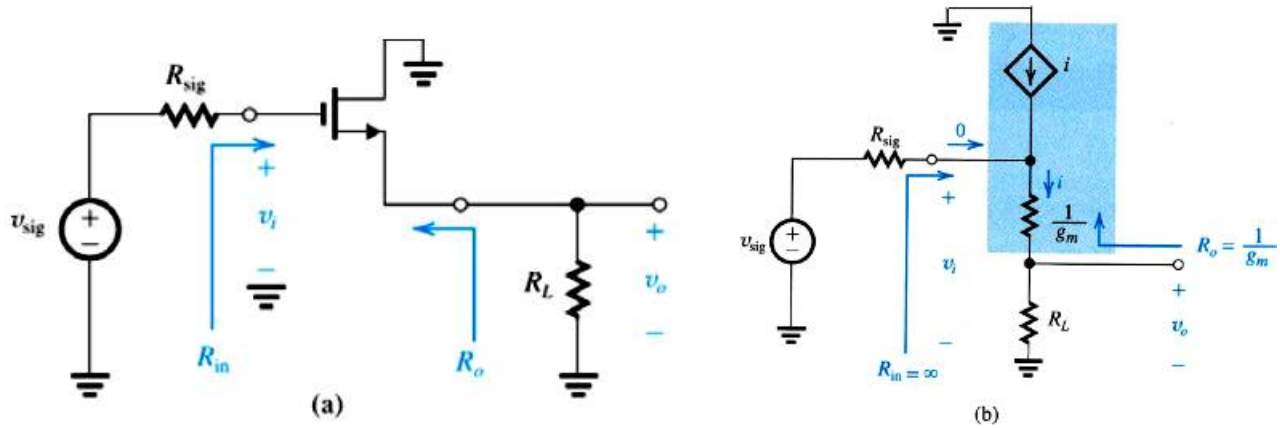


Figure 13(a) shows CD amplifier and figure (b) shows its small signal equivalent circuit.

The Common Drain Amplifier has

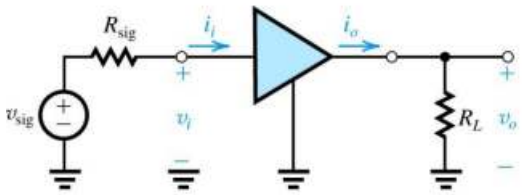
1) High Input Impedance
2) Low Output Impedance
3) Sub-unity voltage gain

Since the output at the source terminal is following the input signal, it is also known as Source Follower.

Because of its low output impedance, it is used as a buffer for driving the low output impedance load. Since there is a resistance RL connected to the source, it is easier to use the T-model

2.7 Characterizing amplifiers

An amplifier fed with a voltage signal v_{sig} having a source resistance R_{sig} and feeding a load resistance R_L. Here, R_L can be load or input resistance to the succeeding stages.



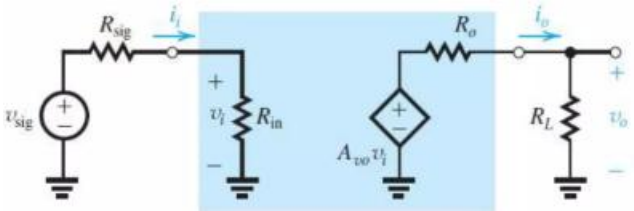
Input resistance with no load

The input resistance R_{in} *represents the loading effect of the amplifier* input on the signal source.

$$R_{in} \equiv \frac{v_i}{i_i}$$

R_{in} *and* R_{sig} *forms a voltage divider that reduces* v_{sig} *to the value* v_i

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig}$$



Open circuit voltage Gain:

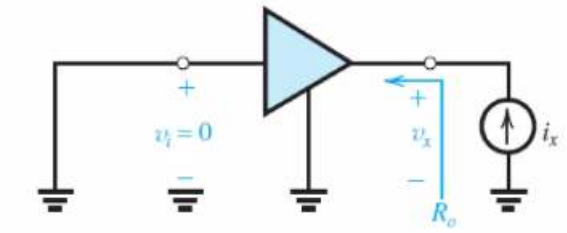
Open-circuit voltage gain A_{vo}, *defined as*

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

The last parameter is the output resistance R_o. *From figure, R_o is the resistance seen looking back into the amplifier output terminal with v_i set to zero.*

$$R_o = \frac{v_x}{i_x}$$

As R_o is determined with v_i = 0, the value of R_o does not depend on R_{sig}.



Output voltage v_o $$v_o = \frac{R_L}{R_L + R_o} A_{vo} v_i$$

Voltage gain of the amplifier, A_v $$A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o}$$

Overall voltage gain, G_v $$G_v \equiv \frac{v_o}{v_{sig}}$$

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_{vo} \frac{R_L}{R_L + R_o}$$

Input resistance with no load:

$$R_i \equiv \left.\frac{v_i}{i_i}\right|_{R_L=\infty}$$

Input resistance:

$$R_{in} \equiv \frac{v_i}{i_i}$$

Open-circuit voltage gain:

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

Voltage gain:

$$A_v \equiv \frac{v_o}{v_i}$$

Short-circuit current gain:

$$A_{is} \equiv \left.\frac{i_o}{i_i}\right|_{R_L=0}$$

Current gain:

$$A_i \equiv \frac{i_o}{i}$$

- Short-circuit transconductance:

$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{R_L=0}$$

- Output resistance of amplifier proper:

$$R_o \equiv \left.\frac{v_x}{i_x}\right|_{v_i=0}$$

- Output resistance:

$$R_{out} \equiv \left.\frac{v_x}{i_x}\right|_{v_{sig}=0}$$

- Open-circuit overall voltage gain:

$$G_{vo} \equiv \left.\frac{v_o}{v_{sig}}\right|_{R_L=\infty}$$

- Overall voltage gain:

$$G_v \equiv \frac{v_o}{v_{sig}}$$

2.8 Common-Source (CS) Amplifier without Source Resistance

The common-source (CS) amplifier for MOSFET is the analogue of the common emitter amplifier for BJT. Its popularity arises from its high gain, and that by cascading a number of them, larger amplification of the signal can be achieved. Fig. 14(a) shows the small-signal model for the CS amplifier. Here, R_D is considered part of the amplifier and is the resistance that one measures between the drain and the ground. The small-signal model can be replaced by its hybrid-π model as shown in Fig. 14(b). Then the current induced in the output port is $i = -g_m v_{gs}$ as indicated by the current source. Thus

$$v_o = -g_m v_{gs} R_D \qquad (1)$$

By inspection, one sees that

$$R_{\text{in}} = \infty, \quad v_i = v_{\text{sig}}, \quad v_{gs} = v_i \qquad (2)$$

Thus the open-circuit voltage gain is

$$A_{vo} = \frac{v_o}{v_i} = -g_m R_D \qquad (3)$$

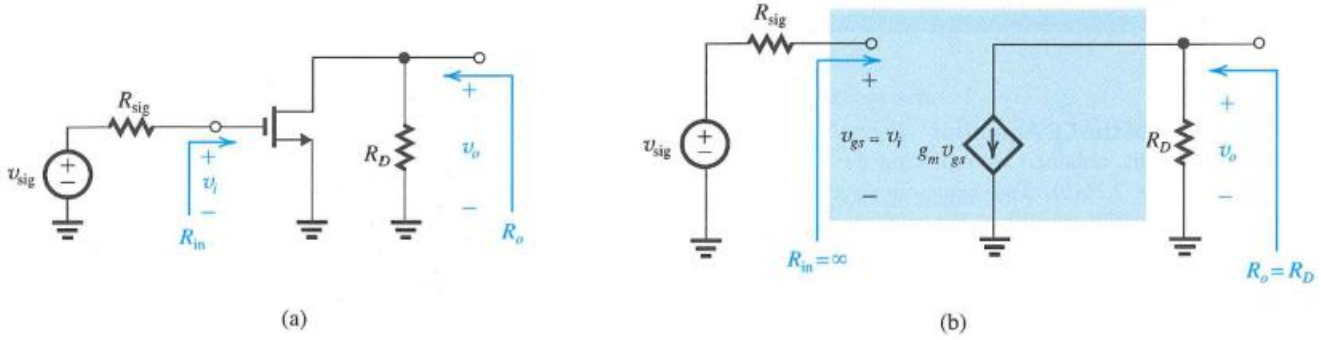


Figure 14(a) shows CV amplifier withot R_S and figure (b) shows its small signal equivalent circuit.

To find the Norton equivalence resistance, one sets vi = 0, which will make the current source an open circuit with zero current. And by the test-current method, the output resistance is

$$R_o = R_D \qquad (4)$$

From the fact that $R_{in} = \infty$, then $vi = v_{sig}$. The overall voltage gain, G_v, is the same as the voltage gain proper, A_v, namely,

$$A_v = A_{vo}\frac{R_L}{R_L + R_o} = -g_m \frac{R_D R_L}{R_L + R_D} = -g_m(R_D \parallel R_L) \qquad (5)$$

$$G_v = \frac{v_o}{v_{\text{sig}}} = -g_m(R_D \parallel R_L) \qquad (6)$$

Final Remarks on CS Amplifier

1. The CS amplifiers has infinite input impedance (draws no current at DC), and a moderately high output resistance (easier to match for maximum power transfer), and a high voltage gain (a desirable feature of an amplifier).
2. Reducing R_D reduces the output resistance of a CS amplifier, but unfortunately, the voltage gain is also reduced. Alternate design can be employed to reduce the output resistance.
3. A CS amplifier suffers from poor high frequency performance, as most transistor amplifiers do.

2.9 CS Amplifier with a Source Resistance

From fig.15(b), a T model is used for the equivalent circuit for simplicity. It is seen that the input resistance of the circuit is infinite because no gate current flows. As a consequence, $vi = v_{sig}$. However, because of the existence of the source resistance, less of the input voltage is divided to v_{gs}, by the voltage divider formula.

Thus

$$v_{gs} = v_i \frac{1/g_m}{1/g_m + R_s} = \frac{v_i}{1 + g_m R_s} \qquad (1)$$

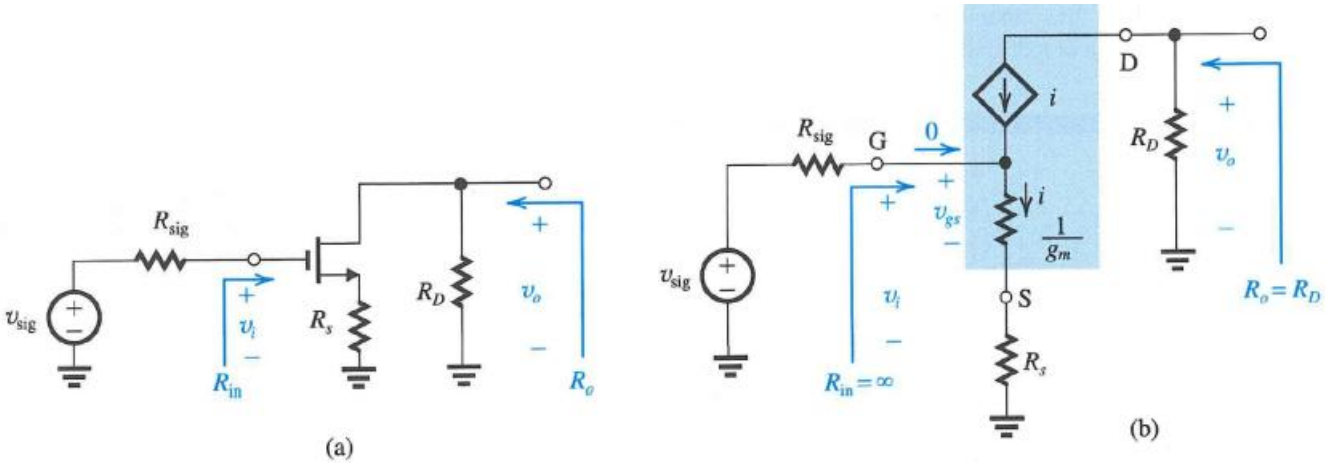


Figure 15(a) shows CG amplifier and figure (b) shows its small signal equivalent circuit.

It is seen that Rs can be used to make v_{gs} small so that there is less nonlinear distortion as the small-signal approximations will become better. The output voltage is generated by the controlled current source yielding

$$v_o = -iR_D \qquad (2)$$

The current i can be found by Ohm's law

$$i = \frac{v_i}{1/g_m + R_s} = \frac{g_m}{1 + g_m R_s} v_i \qquad (3)$$

Thus the open-circuit voltage gain (assume that R_D is part of the amplifier) is

$$A_{vo} = \frac{v_o}{v_i} = -\frac{g_m R_D}{1 + g_m R_s} = -\frac{R_D}{1/g_m + R_s} \qquad (4)$$

The above shows that including the source resistance reduces the amplifier gain by a factor of $(1 + g_m R_s)$ but linearity and bandwidth performance will improve. This is called negative feedback because when the input voltage v_i or v_{gs} attempts to increase, the voltage drop across Rs increases reducing v_{gs}. The source resistance is also called source-degeneration resistance.

The equivalent Thevenin's resistor is Ro which is just R_D in this case. When a load resistor R_L is added, then the voltage gain is

$$A_v = -\frac{g_m(R_D \parallel R_L)}{1 + g_m R_s} = -\frac{R_D \parallel R_L}{1/g_m + R_s} \qquad (5)$$

Because the input resistance is infinite, hence $v_i = v_{sig}$ and the overall voltage gain $G_v = A_v$.

Summary of the CS Amplifier with Source Resistance

1. The input resistance R_{in} is infinite.
2. The open-circuit voltage gain, A_{vo}, is reduced by a factor of $(1 + g_m R_s)$ as seen in Eq(4).
3. For the same nonlinear distortion, the input signal can be increased by a factor of $(1 + g_m R_s)$ compared to without Rs.
4. As shall be shown later, the high-frequency response of this design is improved. In general, the addition of the source resistance Rs gives rise to a "negative" feedback factor $(1 + g_m R_s)$ that reduces voltage gain, but improves linearity, and high-frequency response. Because of the negative-feedback action of Rs, it is also called the source-degenerate resistance.

2.10. Common-Gate (CG) Amplifier

The small-signal and a T-model equivalent-circuit common-gate (CG) amplifier is shown in Fig. 16(b). By inspection, the input resistance R_{in} is given by

$$R_{in} = \frac{1}{g_m} \qquad (1)$$

which is typically a few hundred ohms, a low input impedance. The output voltage is

$$v_o = -iR_D, \text{ where } i = -\frac{v_i}{1/g_m} = -g_m v_i \qquad (2)$$

Hence the open-circuit voltage gain is

$$A_{vo} = \frac{v_o}{v_i} = g_m R_D \qquad (3)$$

which is similar to that of the CS amplifier save for a sign change. The output resistance (or the Thévenin equivalent resistor) of the circuit is

$$R_o = R_D \qquad (4)$$

The smaller input impedance is deleterious to the amplifier gain, as by the voltage divider formula, one gets

$$\frac{v_i}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} = \frac{1/g_m}{1/g_m + R_{\text{sig}}} \qquad (5)$$

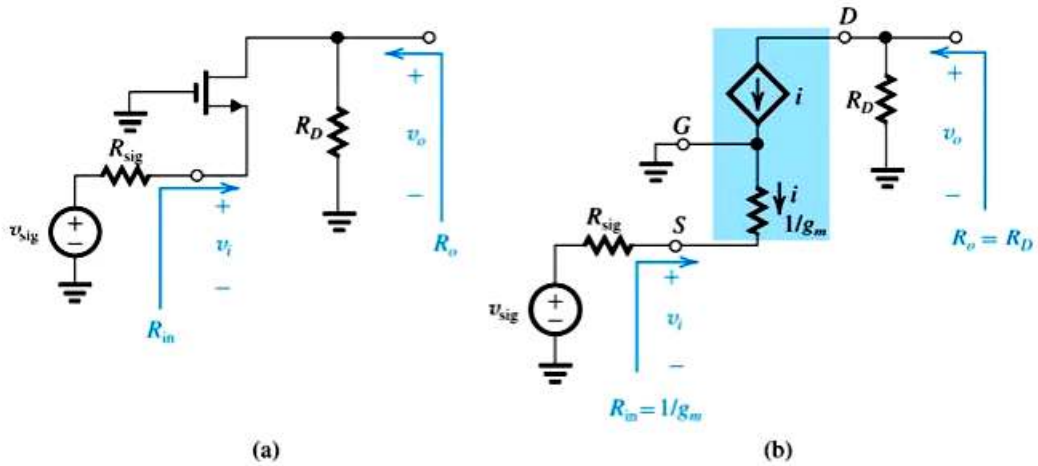


Figure 16(a) shows CG amplifier and figure (b) shows its small signal equivalent circuit.

Meaning that the v_i is attenuated compared to v_{sig}, since R_{sig} is typically larger than $1/g_m$. When a load resistor R_L is connected to the output, the voltage gain is

$$A_v = g_m R_D \parallel R_L \qquad (6)$$

Thus the overall voltage gain is

$$G_v = \frac{1/g_m}{R_{\text{sig}} + 1/g_m} g_m (R_D \parallel R_L) = \frac{R_D \parallel R_L}{R_{\text{sig}} + 1/g_m} \qquad (7)$$

As the input impedance is low, it is good for matching sources with a low input impedance due the the maximum power theorem, but it draws more current, implying high power consumption from the signal source.

Summary of the CG Amplifier

1. The CG amplifier has a low input resistance $1/g_m$. This is undesirable as it will draw large current when driven by a voltage input.
2. The voltage gain of the CG amplifier can be made similar in magnitude to that of the CS amplifier if $R_D \| R_L$ can be made large compared to $R_{sig} + 1/g_m$.
3. The output resistance can be made large since $Ro = R_D$.
4. The CG amplifier has good high frequency performance as shall be shown later.

2.11 The Source Follower (Common Drain Amplifier)

This is similar to the emitter follower for the BJT, which is used as a voltage buffer. It is a unit-gain amplifier with very large input impedance but smaller output impedance. Therefore it is good for matching a high-impedance circuit to a low-impedance circuit or to a circuit that needs a larger supply of current.

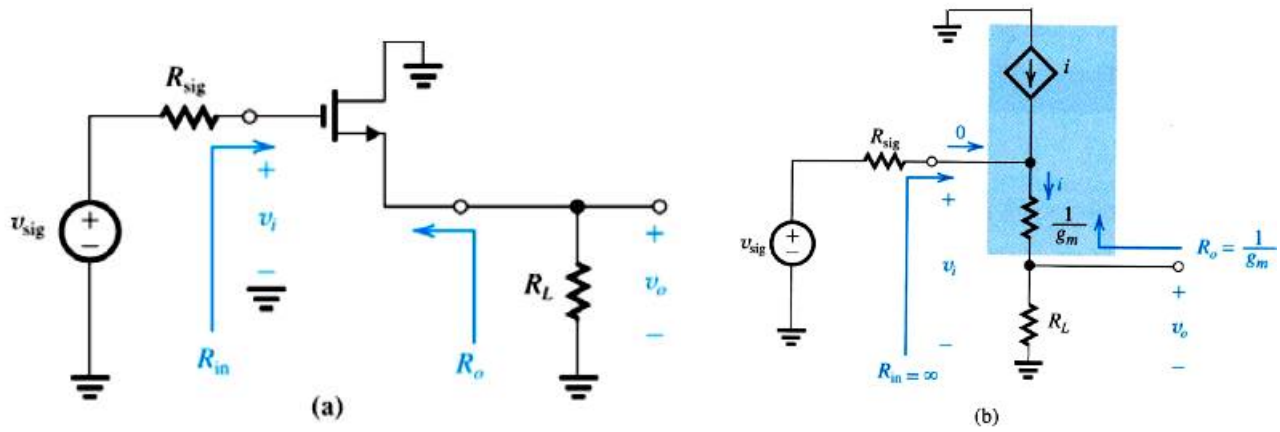


Figure 17(a) shows CD (source follower) amplifier and figure (b) shows its small signal equivalent circuit.

Figure 17(a) & (b) shows the small-signal circuit and a T-model equivalent circuit diagram for a source follower. The input source is represented by a Thevenin equivalent voltage v_{sig} and resistor R_{sig}. A load resistor is connected to the output between the source and ground. Since the gate current is zero for this circuit,

$$R_{in} = \infty \qquad (1)$$

Using the voltage divider formula, it is seen that voltage gain proper or terminal voltage gain is

$$A_v = \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m} \qquad (2)$$

For the open-circuit voltage gain, $R_L = \infty$ and

$$A_{vo} = 1 \qquad (3)$$

The output resistance is obtained by replacing the proper part of the amplifier with a Thévenin equivalence. To this end, with the use of the test-current method, one sets the value of $v_i = 0$, and thus

$$R_o = 1/g_m \qquad (4)$$

Because of the infinite input impedance R_{in}, then $v_i = v_{sig}$, and the overall voltage gain G_v (also called the total voltage gain) is the same as the voltage gain proper A_v (also called terminal voltage gain)

$$G_v = A_v = \frac{R_L}{R_L + 1/g_m} \qquad (5)$$

Since $1/g_m$ is typically small, with large R_L, the gain is less than unity, but is close to unity. Hence, this is a source follower, because the source voltage follows the input voltage, but yet, it can provide a larger current to the output than the input current.

Characteristics of MOSFET Amplifiers

Amplifier type	Characteristics				
	R_{in}	A_{vo}	R_o	A_v	G_v
Common source **without** R_s	∞	$-g_m R_D$	R_D	$-g_m(R_D \| R_L)$	$-g_m(R_D \| R_L)$
Common source with R_s	∞	$-\frac{g_m R_D}{1+g_m R_s}$	R_D	$\frac{-g_m(R_D \| R_L)}{1+g_m R_s}$ $-\frac{R_D \| R_L}{1/g_m + R_s}$	$-\frac{g_m(R_D \| R_L)}{1+g_m R_s}$ $-\frac{R_D \| R_L}{1/g_m + R_s}$
Common gate	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m(R_D \| R_L)$	$\frac{R_D \| R_L}{R_{sig} + 1/g_m}$
Source follower	∞	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$