Harsha Y

Physical Design Engineer Trainee

Profile

Recent B.E. Graduate offering a strong foundation in Physical Design and adept at its fundamentals like CMOS Technology; PnR flow, Parasitic Extraction, Static Timing Analysis; DRV, DRC & LVS Fixing.
Active interests in Design Signoff, FinFETs, FPGA Architecture and Physical aware Synthesis.

Key skills include:
- Quickly learning and mastering new technologies
- Working in both team and self-directed situations
- Critical thinking and Brainstorming for Problem solving
- Solid analytical, communication and presentation skills

Personal Information

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Technical skills

Logic Synthesis

Floorplan

Placement

Clock Tree Synthesis

Routing

Parasitic Extraction

Static Timing Analysis

Timing Closure

TCL Scripting

CMOS Technology

Digital Logic Design

Verilog HDL

C Programming

Experience & Core competencies

Physical Design Engineer Trainee, VLSIGuru Training Institute Aug 2022 - Feb 2023

- Incorporated necessary skill set of a PD Engineer through formal training, coaching or mentoring
- Hands on technical expertise in Block level physical design implementation
- Multi-voltage island-based floorplan design meeting power and timing requirements
- Capable of resolving placement and routing congestion issues
- Generated multiple TCL scripts to automate DRV fixing; cloning for fanout reduction; gather and analyze large volumes of multi-scenario timing data
- CTS implementation and Skew optimization
- Handled global and detail routing including LVS, DRC and Signal Integrity issue prevention
- Working knowledge in Static Timing Analysis, Timing ECO and Logic Synthesis
- Fundamental understanding of Transistors, CMOS Design, IC fabrication Process and Digital Electronics

FPGA Design and Verification Intern, Sandeepani School of Embedded System Design [CoreEL Technologies] Oct 2021 - Nov 2021

- Improved my knowledge in Verilog language concepts and coding for Synthesis
- Learnt about FPGA Architecture
- Hands-on execution of FPGA Design Flow using VIVADO Design Suite
- Used HDL Coding Techniques for Optimal FPGA Design
- Became versed in FSM Modeling
- Been introduced to STA and UART Design

Tools & Softwares

Synopsys ICC2,StarRC,PrimeTime,DC

Cadence Virtuoso, Assura, Genus

Xilinx Vivado, ISE

OS Unix, Windows

Volunteer work

GRAPHIC DESIGN ADMINISTRATOR,
International Conference on Forensics, Analytics, Big Data & Security
Oct 2021 - Jan 2022
IEEE Student Branch BMSIT&M

- Designed Brochure and category wise Certificates for the event
- Administered distribution of Certificates to respective Presenters, Participants, Chair Members and fellow Volunteers

Languages

English - written and verbal
Proficient

Kannada - written and verbal
Native

Hindi - written and verbal
Proficient

Certifications

VSD - Physical Design Flow
Online course - **Udemy**

Introduction to Embedded Systems Software and Development Environments
Online course - **Coursera**

Realization of Flight Control System and its Display
Internship - **HAL**

Overview of Export Manufacturing
Internship - **BEL**

Projects

32-BIT RISC CORE PROCESSOR [by SAED], VLSIGuru Training Institute Oct 2022 - Feb 2023

TITLE	ORCA_TOP
TECHNOLOGY NODE	TSMC 28nm
DESIGN TYPE	Multi-Voltage, Block level
METAL LAYERS	9 [H-V-H]
HARD MACROS	40 [4 Families]
FLAT CELLS	52,047
NUMBER OF PORTS	240
NUMBER OF CLOCKS	8 [3M + 3G + 2V]
TARGET CLOCK FREQUENCY	435 MHz

Objectives:

- Importing Verilog netlist, SDC and link libraries with proper sanity checks during each stage in PnR flow
- Creating timing aware Floorplan and Power plan
- Analyzing and resolving Congestion issues by reducing Cell density and Pin density at required regions during Placement stage
- Critical path grouping and placement optimization with nominal weightage
- Timing fixes (Setup and Hold); Pre-CTS and Post-CTS including DRV fixes
- Clearing up of DRCs and LVS errors Post-Route
- Parasitic Extraction for best and worst RC corners
- Implementing iterative STA ECOs for Timing Closure

Tools used: *Synopsys' IC Compiler II*, *Synopsys' StarRC*, *Synopsys' PrimeTime*

Smart Power Extender, BMSIT&M [VTU] 2021 - 2022
Academic

- IoT based Smart Power Extender with Timer feature controlled through a mobile app
- Worked as a 4-member team and designed an algorithm that facilitates real-time monitoring of appliance's time bound usage of the extender
- Set up Arduino based hardware required for accomplishing the same

Education

B.E. in Electronics and Communication Engineering, BMS Institute of Technology and Management 2018 - 2022

- CGPA : **8.34** • Percentage : **75.9%**

Pre-University Education, M.E.S Pre-University College of Arts, Commerce and Science 2016 - 2018

- Percentage : **91.83%**
- Achieved perfect score in ELECTRONICS

Matriculation, East West Public School 2015 - 2016

- Percentage : **96.64%**