Apeksha Chidanand Biradar

Contact Details

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Education

Bachelor of Engineering in Electronics and Communication
SKSVMACET,
Lakshmeshwar
CGPA-8.28
2018-2022

Jagadguru Tontadarya PU College
Gadag,Karnataka
Percentage-79%
2016-2018

Loyola High School
Gadag
Percentage-91.85%
2016

Career Objective

Seeking opportunity to work as Design and Verification engineer and wanting to discover every dimensions of VLSI with the ability of converting every problem into a possibility. I believe that positive approach makes the difference. And I want to implement that approach in my workplace and give my best for the growth of the organization.

Professional Training

Advanced VLSI Design and Verification Course

Maven Silicon VLSI Design and Training Centre, Bangalore
Sept 2022-till date.

Technical Project

Router 1x3 – RTL Design and Verification

HDL: Verilog

Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

Responsibilities:

- Architected the block level structure for the design.
- Implemented RTL using Verilog HDL.
- Synthesized the design.

Cuk Converter

Description:
Cuk converter is a type of DC\DC converter that has an output voltage magnitude that is either greater or less than the input voltage magnitude.

Responsibilities:
Simulated the circuit of Cuk converter using simulink tool of matlab software and analysed the output.

Behavioural Skills

- Good communication
- Optimistic
- Leadership quality

Hobbies

- Dancing
- Cooking
- Yoga

Languages

- English
- Kannada
- Hindi

Achievements

- Sonata scholarship for best performance in engineering academics (Twice).
  2021-2022

Technical Skills

VLSI Domain Skills

- **HDL**: Verilog
- **HVL**: System Verilog
- **Verification Methodologies**: Constraint Random Coverage Driven Verification
- **Digital Electronics:** Combinational & Sequential circuits, FSM, Memories.
- **Verilog Programming:** Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Synthesis issues, Races in simulation, pipelining RTL & TB Coding,
- **Advanced Verilog & Code Coverage:** Generate block, Continuous Procedural Assignments, Automatic Tasks, Named Events and Stratified Event Queue, Code Coverage: Statement and branch coverage, Condition & Expression Coverage, Toggle & FSM Coverage.

Verification Skills

System Verilog HVL

- Memories - Dynamic array, Queue, Associative array, Task & Function - Pass by reference
- Interface - Modport and clocking block.
- Basic and advanced object-oriented programming - Handle assignments, Copying the object contents, Inheritance, polymorphism, static properties and methods, virtual classes and parameterized classes.
- Constraint Randomization - constraint overriding and inheritance, Distribution and conditional constraints, Soft, static and inline constraints.
- Thread synchronization techniques - events, semaphores and Mailbox - built-in methods.
- Functional coverage - Cover groups, bins and cross-coverage, CRCDV and regression testing.

Declaration

I hereby declare that the information furnished above is true to the best of my knowledge and belief.

Place: Gadag, Karnataka, India Apeksha Chidanand Biradar

Date: