Mahesh Narbolikar

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Gulbarga-585101, Karnataka

Career Objective

A motivated individual seeking for a responsible position as an entry level Physical Design Engineer which will qualify me to bring the best out of my knowledge and experience in achieving growth and development of myself as well as the organization

Core Competancy

- Acquired extensive knowledge in ASIC PD Flow involving Floor Planning, Power Planning, Placement, Clock Tree Synthesis and Routing.
- Hands-on-experience on the industry tools such as Synopsys IC Compiler II for APR flow and Prime Time for Static Timing Analysis.
- Placement of macros based on data flow lines, ports and also providing with a required routing and placement blockages in the floorplan.
- Generated an optimized placement block with controlled congestion through various iterations of channel spacing and modifying floorplan.
- Knowledge in interpreting timing reports, fixing Setup and Hold violations and the concept of adjusting the clock skew in order to fix setup and hold violations.
- Dealing with Timing Paths of various PVT corners, Modes, Scenarios, concept of CRPR and also understanding of the constraints to define the False and Multi-Cycle Paths .
- Fair knowledge on Signal Integrity issues like Crosstalk, Reliability issues like Electromigration and Antenna effect.
- Analyzing and fixing of the DRC and DFM issues.
- Comprehensive knowledge on the concepts of STA, Logic Design and CMOS Theory .

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Instrumentation** **2022**

JSS Science and Technology University, Mysuru, with 8.12 CGPA

2018

SBR PU Composite College, Gulbarga, with 88.33 %

SSLC **2016**

SBR Residential Public School, Gulbarga, with 93.12 %

Domain Specific Project

RV-VLSI and Embedded systems Design Centre, Bengaluru

Physical Design Trainee Aug-2022 to Feb-2023

Block level Physical Design implementation

Description

A block level Implementation of a design at 40nm technology node with a list of 34 Macros, 40K+ Standard Cells, operating at a frequency of 833 MHz and a nominal supply voltage of 1.1V with a Target IR drop of 5% and an assigned Power Budget of 600mW

Tools

Synopsis Prime Time tool for STA, Synopsis IC compiler II for APR flow

Challenges

- Designing of a proper floorplan by ensuring a contiguous area between the macros and creating a good power routing such that it doesn't violates the IR drop and EM requirements.
- Overcoming congestion problem by keeping it under control with respect to global route congestion, also adding few partial blockages to control congestion at Standard cell area.
- Analyzing the timing reports and debugging the cause for setup and hold violations and working for the slack to be under control.
- Overcoming with the DFM Violations and providing them with a suitable fix with the help of Metal Jumpers and a Diode.

B.E / B.Tech Academic Project

JSS Science and Technology University, Mysuru

ARDUINO BASED VOICE CONTROLLED WHEELCHAIR

Description

Operating the wheel chair through an android app, usage of the voice-based system so that users voice acts as an input to control the mobility of wheelchair, Design and development of pulse and temperature monitoring system.

Tools

Arduino IDE, AMR Voice, Bluetooth RC controller app

Challenges

- Capturing of proper Voice command from the User as we had used an built in application called AMR Voice which was fluctuating to capture the User's command in the noisy environment.