KARTHIK Y
Course: M.Tech, VLSI Design, 21-23
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CGPA : 9.02

ACADEMIC DETAILS

COURSE	INSTITUTE/COLLEGE	BOARD/UNIVERSITY	SCORE	YEAR
PG (VLSI Design)	Vellore Institute of Technology	VIT University, Chennai	9.02 CGPA	2023
UG (Electronics & Communication Engineering)	R.N.S Institute of Technology	Visvesvaraya Technological University, Belagavi	7.5 CGPA	2019
INTERMEDIATE (Class XII)	K.L.E Society's Independent PU College	Department of Pre-University Education, Karnataka	86.83%	2015
MATRICULATE (Class X)	Vidyaniketan Public School	Central Board of Secondary Education, Delhi	9.4 CGPA	2013

WORK EXPERIENCE

Graduate Technical Intern, Intel Technology India Pvt Ltd. **Sept 2022- Present**

- Worked with a team which automates RTL-to-GDSII flow for design team, specifically in APR domain.
- Trained on APR flow design in Synopsys (Fusion Compiler) and Cadence (Genus & Innovus).
- Automated few of the existing problem statements in the APR flow using TCL and Shell scripting by reducing manual work in specific areas of regressions activities.
- Currently working with a team which develops scripts to construct, check and simulate the global clock distribution.
- Involved in modification of clock distribution scripts which were developed using ITCL format (legacy) and converted them to TCLOO.
- Certified from Cadence on "RTL-to-GDSII Flow v4.0" course.

Associate Application Developer, Accenture Solutions Pvt Ltd. **Jul 2019-Aug 2021**

- Experienced Cloud based frontend and backend application Developer involving in Assisting clients, process development and functional implementation.
- Hands-on Experience in developing Visualforce Pages and Lightning Components on Salesforce.com Platform (SFDC).

Subjects/Electives	ASIC Design, CAD for VLSI, Digital IC design, Digital Electronics, Verilog HDL, Python, TCL
Tools	Cadence (Genus, Innovus, Virtuoso), Synopsys (Fusion Compiler), Xilinx (ISE), Mentor Graphics (Tanner EDA)

PROJECTS

Design and Implementation of Advanced Array Multiplier using Compressors **Oct 2021-Nov 2021**

- Designed 4,5,6 and 7 inputs compressor by using Full Adders and Half Adders.
- Implemented Advanced Array multiplier using different compressor designs by replacing conventional utilisation of full adders.
- Analysis performed on low area consumption by Simulation and verification using *Xilinx ISE* tool.

Design of FinFET based Low Power SRAM Cell for portable Biomedical Applications **Nov 2021-Jan 2022**

- Designed 32nm FINFET based SRAM in 6T and 7T Configurations.
- Power Analysis was performed between the MOSFET and FINFET designs of SRAM.
- Self-Controllable Voltage logic (SVL) was applied in FINFET SRAM design to further reduce the power during read/write modes.
- Simulated and verified the design using the *Cadence Virtuoso* tool.

EXTRA CURRICULAR ACTIVITIES

Infy Campus Ambassador, RNSIT Sept-2017

- Selected as Infy Campus Champ for the year 2017 as a part of a program conducted by Infosys.
- Organized multiple workshops for students on industry-oriented topics and motivate them to be part of the industry in various activities.

Open House Project Expo Event Organizer

- Organized and involved in evaluation of best projects for "Open House Project Expo - 2018" in Department of ECE, RNSIT on 29th Sept 2018.