# YOGESH SUROSHE

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## Career Objective

A highly motivated, hardworking individual seeking an opportunity to learn and build upon skills that are essential within the industry.

## TECHNICAL SKILLS

- **Programming Languages:** Verilog HDL, System Verilog HVL SV)
- **Verification Technologies:** System Verilog( Assertions), Universal Verification Methodology (UVM)
- **Protocol** : AMBA- AXI- 4, AHB and APB.
- **Operating System** **:** Linux(ubuntu), Windows.
- **Tools** **:** Xilinx ISE , Xilinx Vivado and Mentor graphic modelsim.

## Work Experience

**Design Verification Engineer** **March 2022- Present**

**BitSilica Pvt. Ltd. Hyd.**

- Work on Mailbox Memory controller verification.
- Verified the AHB protocol features like Burst transfer, Aligned address, and pipelined operations.
- Worked on driver logic

**VLSI FOR ALL Pvt. Limited** **July 2022 – Present**

- Designed a pattern detector with the help of Moore and mealy FSM using System Verilog. Verified by waveform monitoring.
- Design a few sequences for AXI protocol by writing UVM testbench and verifying by assertion checker.

**Maven Silicon Pvt Ltd, Bangalore (DV)** **Dec. 2021 – July 2022**

[Digital Design, STA, Verilog, CMOS Design, System Verilog, UVM]

## Projects:

**Mailbox Memory controller verification.**

**Description**: MMU controller is responsible to communicate with 19 SRAM memory cuts. It is AHB interfaced device for internal register programming and supports simple burst operation.

**Roles and Responsibilities**

• Specification Readout
• Created vplan for features to be tested
• Vplan review with peers and other stake holders
• Update and modified test bench
• Created SV sequences to test the features.

**IP level Verification of AMBA-AHB protocol**

**Description:** The ARM Advanced Micro-controller Bus Architecture (AMBA) AHB is an open standard on-chip communication protocol. It supports features like pipelined operation, burst transfer and aligned transfers.

- Verified the AHB protocol features like Burst transfer, Aligned address, and pipelined operations
- Worked on driver logic

**IP level Verification of AMBA-AXI_4 based slave Duration**

**Description:** The AMBA_AXI_4 protocol is targeted at high-performance, high-frequency system and includes a number of features that make it suitable for a high-speed communication. AXI has five independent unidirectional channel.

**Roles and Responsibiliies**

- ·Detailed study of AMBA-AXI_4 protocol specification.
- ·Developed the test-cases for AXI for different scenarios.

**I2C (Inter integrated circuit) Protocol**

- I2C is Inter-Integrated Circuits. It is a bus interface connection protocol used for devices in serial communications. It is a widely used protocol for short-distance communication.
- ·Created C based testcase to check the integration of interrupt and data/control path

**SPI (Serial Peripheral Interface) Protocol**

- The Serial Peripheral Interface is a synchronous serial communication interface specification used for short-distance communication, primarily in embedded systems. The project was made using Verilog.

**UART (Universal Asynchronous Receiver Transmitter Communication) Protocol**

- UART project consisting three main sections The Transmitter, The Baud Rate generator (to synchronize transmitter and Receiver), and finally, the Receiver. The project was made using Verilog.

## Academic Qualification

| Course | College name | CGPA | Academic year |
|---|---|---|---|
| M.Tech | Indian Institute of Information technology, Gwalior | 8.22/10 | 2020-2022 |

## Achievements

- Qualified GATE (Electrical Engineering) in 2020. (422/1000)

## Personal details

**GENDER** **:** Male
**NATIONALITY** **:** INDIAN
**LANGUAGE KNOWN:** Marathi, Hindi and English
**DATE OF BIRTH** **:**14/02/1996

## Declaration

I hereby declare that all the information contained in this resume is in accordance with facts or truths to my knowledge. I take full authority for the correctness of the written information.

Banglore, India
Date: 05/04/2023

Yogesh Suroshe