ABHISHEK BM

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EDUCATION

MTECH in Digital Electronics and Communication

Skills

- Hands on PnR Netlist to GdsII.
- Strong Knowledge on Asic Design Flow.
- Familiar with Low power Design Techniques.
- Worked on 10nm, 16nm, 28nm Technologies.
- Hands on Icc2, Primetime, Innovus tools.
- Knowledge of Linux, TCL scripting.
- Exceptional communication skills.

CAREER OBJECTIVE

Seeking a challenging and responsible opportunity to utilize my technical skills and serve in the field of VLSI Physical Design while making a significant contribution to the success of the company.

WORK EXPERIENCE

1.5 Years of Experience in VLSI Physical Design in 28nm and 16,10nm technologies.

Working for G7N semiconductor Pvt Ltd (Sep 2021 – Present)

Project Summary

Project 1: Client-INTEL

Duration: 08Months

Tool Used: ICC2

Role: Handling of entire block level functions and ECO implementation with 600k inst count and 18 macros with 425MHz from Netlist to GDSII.

Technology: TSMC 10nm

Responsibilities:

- ECO cells implementation for timing improvement.
- Performed LVS cleanup.
- LEC and PTPX Checks.
- Done signoff checks and fixed caliber errors.

Project 2: Client-INTEL

Duration: 10months

Tool Used: Innovus

Role: Handling of block with 500k inst count and 18 macros with 625MHz from Netlist to GDSII.

Technology: TSMC 28nm

Responsibilities:

- Done multiple floorplan experiments for congestion control and timing improvement.
- Done multiple CTS experiments for reducing the insertion delay.
- Performed DRC and LVS cleanup.
- Cleaned the IR fixes given by IR Team.

Published techhnical Paper

Title: OFDMA FOR 4G/5G LTE BASED SYSTEM USING 16QAM TECHNIQUE
Paper Download Link:https://www.irjet.net/archives/V3/i7/IRJET-V3I7404.pdf

INTERNSHIP

- Worked as intern PD Trainee at NeoschipTechnologies Bangalore in 2019.
- Worked as intern Design Engineer Trainee (2015-16) in Centre Research Laboratory at Bharath Electronics Bangalore.

Place: Bangalore
Date: 05 APRIL 2023

Internship Projects

Soc Level

Technology: 45nm

Tool Used: Cadence innovus

Responsibilities: The RAK design is a SOC level design with 35K instances, 19 memories, and multi clock . The library used is a Cadence Generic 45nm library using 11 routing layers.

Full Chip- LOW POWER DESIGN [UPF]

Technology: 45nm

Tool Used: Cadence innovus with TCL scripting (45 nm)

Responsibilities**:** In this project our design is DMA MAC .The design consists of 2blocks with 30k instances, and 301 IO pins and using 11 routing layers. The design having multiple power domain and this is for to reduce the power consumption. It has power supply network , Level shifter, Retention cell etc. And all are implemented with TCL scripts. simple DMA design through the low power design flow by using UPF 2.0

Yours Faithfully
ABHISHEK B M