PRITIKA ROUT

Verification Engineer

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Objective

An enthusiastic and passionate VLSI Design and Verification Engineer looking for an opportunity to work in a reputed organization, which can provide good working environment to upgrade my skills and help me to deliver my best to meet the demand of the organization.

Experience

Verification Engineer Intern (Insemi Technology) *(1stth* Feb *2022 to 26* Oct*)*

Fault Management (FS04) (maverick semiconductor)

DESCRIPTION: This project deals with the Fault management .It will count the functional safety.The fault will be increment by one when an error occurred .It occurs on whenever a fault Generated it will be incremented by one .In the fail safe domain when an error is occuring
It will be count as error.

Design and Verification Training (Maven Silicon) *(28th Sep2021 to 28th Apr 2022)*

- Learned Verilog, System Verilog, Assertion and Coverage
- Learned UVM TB methodology
- Worked on FSM based design, Simulation, Synthesis, Assertions and Coverage
- Hands on experience on SPI, UART, I2C, APB, Protocols.
- Hands on experience with VCS .

Education

B.Tech. in Electronics Engineering 2017-2021
VEER SURENDRA SAI UNIVERSITY OF TECHNILOGY ,BURLA(ODISHA).
(*7.30 CGPA*).

Technical Skills

HDL: Verilog

HVL: System Verilog
Assertions & Coverage
TB Methodology: UVM
Protocols: SPI, I2C,UART, APB, AHB
Tools:VCS
Basics of soc verification flow.

Self Motivation	Hardworking	Decision Making
Adaptability	Process Oriented	

Languages

English	Hindi	odia