VISHAL SINGH

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CAREER OBJECTIVE

Seeking a rewarding career in VLSI design and verification, where I can utilize my knowledge and experience to contribute to the development of cutting-edge technologies.

TRAINING

JUNE 2022 – CURRENT

RTL DESIGN AND DESIGN VERIFICATION TRAINEE, MAVEN SILICON

- Completed intensive training in RTL design and design verification, gaining expertise in Verilog HDL, CDC, simulation, and verification methodologies.
- Learned industry-standard design methodologies, like UVM, and how to use advanced verification techniques to ensure design correctness and performance.
- Participated in project-based learning, where I applied the knowledge gained in the training to design and verify a complex digital circuit, which included writing RTL code, creating testbenches, and performing functional and timing simulations.

WORK EXPERIENCE

MAY 2021 –APR 2023

HARDWARE ENGINEER, L&T TECHNOLOGY SERVICES

Obsolescence Management and Super BOM management--- OTIS

- Component Engineering- Conducted extensive research and analysis to identify new electronic components that meet design specifications and comply with industry standards.
- Worked closely with suppliers to resolve component-related issues, including obsolescence, quality, and availability issues.
- Conducted component failure analysis and recommended design improvements to prevent future failures.
- Implemented continuous improvement initiatives to optimize the component selection process, reduce lead times, and increase cost savings.
- Generated and maintained accurate and up-to-date BOMs for multiple products, ensuring that all components were properly identified, sourced, and documented.
- Reviewed and analyzed engineering drawings, specifications, and other technical documentation to identify and select the appropriate components for the BOM.

Tools Experience: - MS Excel, PyCharm, KiCad, Silicon expert, Windchill.

EDUCATION

2017-21

BACHELOR OF TECHNOLOGY, UPES

Earned a bachelor's degree in Electronics and Communication Engineering, with a focus on digital circuit design, embedded systems, and communication systems. And secured 7.7/10 CGPA.

2015-16

INTERMEDIATE, GNPS

Pursued class 12th with Physics, Chemistry and Math's as main subject and scored 75%.

TECHNICAL SKILLS

- HDL: Verilog
- HDL Techniques: CDC
- HVL: System Verilog
- EDA Tool: Mentor Graphics - Questasim and Xilinx – ISE
- Programming Languages: C++ (Good understanding of OOPs concept, Class, Inheritance, Polymorphism)
- Verification Methodologies: Constraint Random Coverage Driven Verification
- TB Methodology: UVM
- Core Skills: RTL Coding using Synthesizable constructs of Verilog, FSM based design, Simulation, Synthesis, System Verilog Assertions.
- Familiarity with AMBA protocols (AHB, APB)

PROJECTS

1X3 ROUTER SOC DESIGN, MAVEN SILICON

- Designed a 1X3 Router SoC, which involved designing a complex system-on-chip architecture that incorporated multiple modules, such as the FSM, FIFOs, Registers, and I/O interface.
- Utilized Verilog HDL to design the RTL code for the various modules and used EDA tools such as Quartus Prime and ModelSim for simulation and synthesis.
- Tested and verified the design through simulation and formal verification using Verilog based test bench, ensuring that the design met the specifications and requirements.

MOD-15 UP/DOWN COUNTER VERIFICATION, MAVEN SILICON

- Verified the functionality of a MOD-15 Up/Down Counter design, which involved simulating the counter using testbenches and formal verification techniques using System Verilog based test bench.
- Designed and developed testbenches for the counter, which included generating various input stimulus to test the counter's functionality under different conditions, such as reset, load, and count operations.
- Successfully signed-off the verification process with 100% coverage.

1X3 ROUTER DESIGN VERIFICATION, MAVEN SILICON

- Successfully verified the functionality of a 1x3 Router design, which involved simulating the design using testbenches developed using UVM methodology.
- Developed a UVM-based testbench for the Router design, which included developing sequence items, Sequencer, Agents, drivers, monitors, and coverage collectors to ensure the design was verified thoroughly.
- Signed-off the verification process with 95% coverage.

SOFT SKILLS

- **Team Player**: - Worked with the team of 9 members from different technical backgrounds. Actively participated in team meetings and brainstorming sessions, contributing ideas and solutions that helped to drive the team's success.
- **Multitasker**: -Successfully managed office work and training simultaneously, ensuring that all deadlines and milestones were met in both the places.
- **Time Management**: - Set clear priorities and goals, focusing on the most important tasks, and ensuring that they were completed in a timely manner.

DECLARATION

I hereby declare that all the details provided above are true to the best of my knowledge.

Place- Mysore, Karnataka **Vishal Singh**
Date- 04-04-2023