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Career Objective

Eyes on a challenging and competitive environment where I can serve a reputed board like yours and earn a promising career for myself.

Core Competancy

- Good knowledge in ASIC PD Flow in Floor planning, Power planning, IR Drop Analysis, Automatic P&R, Clock Tree Synthesis & Routing.
- Hands on experience in STA, CRPR, Interpreting timing reports, fixing HOLD and SETUP violations.
- Generated and analysed timing reports of Pre-Layout and Post-Layout STA on Primetime and ICC2.
- worked on Floor plans for high utilization ratio and good contiguous core area, designed good power mesh to connect all macros and std-cells without any floating pins.
- Worked on placement with power budget and acceptable congestion ensuring good routability.
- Understood and modified Tcl scripts and have written Tcl scripts to extract information from the reports and to find the WNS & TNS.
- Analyzed and understood Design Constraints to specify PVT Corners, False paths, Half cycle, Multi Cycle path,Asynchronous Clocks, CRPR.
- Hands on experience in APR tools - ICC2 and STA tools- PrimeTime.
- Understood the Routing Flow and Fixed the DRC, LVS and Antenna violations.
- Good Knowledge in Logic Design Concepts, CMOS, MOSFET, Semiconductor Theory and Basic Electronic Devices.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2022**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2020**
kakatiya University College of engineering and technology, with 64 %

2015
Vidya Bharati junior college, sathupalli, with 96 %

SSLC **2013**
SDVR ZP High School , B.gangaram, with 8.7 %

Domain Specific Project

RV-SKILLS

Graduate Trainee Engineer May-2022 to Sep-2022

Designing of ASIC Block level Implementation

Description

Overview: 40mm design: Clock Frequency-1 GHZ, Shape -Rectilinear, Macro Count-34, Standard Cell Count-41k, Area-4.2 sq.mm, Supply Voltage-1.1V, Power Budget-600mWatts, IR Drop budget - 55Mv, Metal layers -7.

Tools

Synopsys ICC2

Challenges

- Understanding the design constraints and setup designing Floorplan as per Data Flow diagram and using Flylines to have contiguous Core area for std-cells.
- Building a good power plan to meet the It drop specified and ensuring that no floating pins missing vias in the design and no PC DRC errors after budding the power Network.
- To control congestion and DFT aware placement, tried different floorplan experiments and Implemented different strategies.
- Understanding tool's behavior while clock tree synthesis to meet target skew Min/Max latencies, fixing timing violations and understanding DBC and LVS errors

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RV-SKILLS

Graduate Trainee Engineer May-2022 to Sep-2022

Analysis of Timing Reports STA

Description

For Flip flops and latch based timing paths working at different operating conditions. Timing reports are analysed considering OCV, AOCV, uncertainty, CRPR Clock Skews and certain exceptions (Multi cycle paths) honoring the constraints file.

Tools

ICC2, PrimeTime.

Challenges

- Analysed all the timing paths different path groups at every stage of flow (floorplan placement & CTS) and how some violations are reduced in the later stages.
- Differentiating some violations which are based on timing exceptions such as false paths and multi-cycle paths and reporting about the same to change in the constraint file.
- Understood the effects of CRPR, OCV, AOCV and skew factors in timing analysis.

B.E / B.Tech Academic Project

kakatiya University College of engineering and technology

Password Based Circuit Breaker

Description

Password Based Circuit Breaker is design to protect a circuit from damage which is caused by over load or short circuit. It provides lineman safety by giving direct authorization of power lines to them,so they can turn on/off any time they want.

Tools

1)8051 micro controller. 2)Keypad,LCD ,Relay. 3)Power supply, Regulator. 4)Keil Cross Compiler.

Challenges

- we faced a problem of with it being totally wired and we hope to do a future version of this project with a GSM module so that it can receive a perticular message about which circuitto turn on or off.