MEKALATHOORI NITHISH

FRESHER

To seek a challenging position in an organization, which provides opportunities to personal growth and organizational growth as well.

nithinithish211@gmail.com | +91 7702970206 | Andhra Pradesh, India

EDUCATION

Bachelor of Engineering
Sree Rama Engineering College ,Tirupati.
2019 - 2022 *78%*
Electronics and Communication Engineering .

Diploma
Govt.Polytechnic college,Tirupati.
2016 - 2019 *79%*

S.S.C
S V High School,Renigunta.
2015 - 2016 *9.0*

TECHNICAL SKILLS

Design For Testability
- o Scan Insertion
- o Scan Compression (EDT)
- o ATPG Pattern Generation and Coverage Analysis
- o On-Chip Clock Controller
- o Scan Pattern Simulation
- o JTAG and Boundary Scan
- o MBIST Insertion

Digital Design
- Combinational and Sequential Circuit Design
- Basics of Verilog HDL

Basics of Static Timing Analysis

PROJECTS

(Final Year Project)
Comparative Analysis of Low Power Wallace Tree Encoders with Modified Full Adders

SOFTWARE SKILLS

Automation Languages : TCL

Operating Systems : Linux, MacOs | Text Editor : GVIM

DA Packages : Tessent (Scan, TestKompress, MBIST), ModelSim and DesignCompilers

INTERNSHIP

DFT Trainee
VLSIGuru Training Institute

PROJECTS (DFT RELATED)

MBIST and Scan Insertion on a small design
worked on small Hierarchical designs consisting of a Parent and multiple Child cores with flop count of ~4K. Performed MBIST Insertion, Scan Stitching and DRC Cleanup, EDT and OCC Insertion. Worked on ATPG Coverage analysis, Pattern generation and Serial & Parallel Scan pattern Simulation

CERTIFICATES

Completed “House Wiring” courses conducted by the SV University Tirupati.

Completed Workshop on “Printed Circuit Board Design & Fabrication” in “E-BLAZE” conducted by SV University Tirupati.

LANGUAGES

Telugu
Native or Bilingual Proficiency

English
Native or Bilingual Proficiency

INTERESTS

Design For Testability | Digital Design