ESWARAPRASAD PINNINTI
Mail id: eswarprasad054@gmail.com Ph no:7036389018

CAREER OBJECTIVE

I am seeking an opportunity that will allow me to contribute my skill in new environments, enhance my experience and broaden my horizons.

EDUCATIONAL DETAILS:

- Bachelor Of Technology (B-Tech) in Electrical & Electronics, with 62% (2019) at Satya institute of technology and management under JNTUK.
- State board of technical education & training (Diploma) in Electrical & Electronics, with 82% (2016) at Government polytechnic college.
- Board of secondary education (SSC) with 9.0 GPA (2013) at RCM St'Anthoys high school.
- I trained as Design and Verification engineer from the institute of **VLSIGURU** duration of 8 months.

PROFESSIONAL EXPERIENCE SUMMARY:

- Good understanding of ASIC verification flow.
- Good programming skills in **System Verilog and Verilog HDL.**
- Hands on experience with EDA tool (**Questa Sim, VCS)**.
- Good Understanding of HVL concepts. Able to code test scenario using existing given test plan. Knowledge of HVL test bench components, debugging HVL environment.
- Knowledge on Digital electronics.

Technical Skills:-

Hardware Description Language	: Verilog.
High-Level Verification Language	: System Verilog.
Methodology	: UVM.
EDA Tools	: Questa Sim.
Domain Knowledge	: AMBA-APB .
Operating Systems	: Linux, Windows.
Programming Languages	: Basic oops concepts.
Knowledge	: RTL Coding, Functional Verification , Constraint random verification and Assertion .

PROJECT'S :

PROJECT :1

Title : **MEMORY** .

HDL : VERILOG.

EDA Tool : MODELSIM.

Description :

Memory is a storage element that represents an array of vectors. Reg data type is used since we need to store the data. By using memory, we can do write and read operations. Memory elements are accessed using by index. All operations to memory happen only at the rising edge of the clock. 3 types of operations are possible at any rising edge of the clock.

1) Reset applied
2) Reset not applied
3) No transaction to the memory.

We can access memory in 2 ways. a) Front door access b) Back door access.

a) Front door access means accessing the memory contents by driving the design ports.
Front door takes time.

b) Backdoor access means accessing memory directly by hierarchy without driving the design ports. i.e., DUT. mem loading the values by memory hierarchy directly.

Backdoor access completes in zero time. In real chips there is no concept of backdoor access, it is only used for simulation purpose because it reduces simulation time.

- Implemented the TB using VERILOG.

PROJECT :2

Title **: FIFO** .

HDL : VERILOG .

EDA Tools : Modelsim, Questa Sim -- Verification Platform

Description :

FIFO is a design block that returns the data in First In First Out order. Chip operation is all about data transfers, data moving from one component to another component. One component giving the data and other one is taking the data. There is a possibility where one component generates data faster, another component consumes slower. This creates bottleneck in the chip operation. By using FIFO both components work at their own speeds. Functionality of FIFO is interfaces with a data producing component on one side, data consuming on the other side. It makes sure the producing and consuming happens independently at their own speed. FIFO is 2 types, 1) Synchronous FIFO

2) Asynchronous FIFO.

In Synchronous FIFO both write to FIFO and read from FIFO happens at same clock.

In Asynchronous FIFO the Write to FIFO and read from FIFO happens at different clock.

PROJECT :3

Tittle **: APB.**

METHODOLOGY : UVM

EDA Tools : Modelsim, Questa Sim -- Verification Platform

Description :

The APB is a part of AMBA 3 protocol family. APB is ADVANCED PERIPHERAL BUS protocol, It provides a low cost interface that is optimized for minimal power consumption and reduced interface complexity. The APB interface to any peripherals that are low bandwidth and do not require the high performance of a pipelined bus interface. Every transfer takes atleast 2 cycles. APB is a On-chip protocol i.e., communications for the blocks on the chip. It is also a Synchronous protocol; all the signal sampling happens at the positive edge of the clock. For APB transaction to complete psel, pready, penable should be 1 at +ve edge of the clock.

Self appraisal:

I hereby inform that the above information is true and best of my knowledge.

Place: VIZIANAGARAM

(P. Eswara prasad)