KIRAN BHUKYA

M. Tech (VLSI)
Indian Institute of Information Technology, Design and Manufacturing, Kancheepuram

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Looking for an opportunity to work in an organization to enhance my skills and knowledge along with contributing to the growth of organization.

WORK EXPERIENCE

- Advanced Physical Design Trainee at VLSI-guru training institute Bangalore
  Has hands-on experience with IC compiler 2-synopsys, I designed layouts for 14nm, 28nm and VLSI circuits.
  ICC2 was used to convert Netlist to GDS2

EDUCATION

- **B. Tech. Electronics and Communication Engineering with specialization in Design and Manufacturing + M. Tech. VLSI & Electronic System Design |2018-2023|**
  Indian Institute of Information Technology, Design, and Manufacturing, Kancheepuram |CGPA – 7.16|
- **Intermediate |2018|**
  T.T.W.J. College Mahbubnagar, Telangana | State Board |CGPA - 9.05|
- **High School |2016|**
  T. T. W. R. School, Yakub Pura, Warangal | State Board | CGPA – 8.5|

TECHNICAL STRENGTHS & LANGUAGES

• ICC2 (Synopsys) • Star RC • Primetime • TCL scripting • Linux	• Cadences virtuoso • Verilog • MATLAB • Multisim • Python	• PCB Designing • Cadence virtuoso Layout • LT Spice • ASIC Design Flow	• English • Telugu • Hindi

PROJECTS

1. Physical design implementation

Design specifications	Responsibility
• Processor: 32-bit RISC core • Process technology:28nm TSMC, • Operating frequency: 434 MHz • Memory: 40 macros • Number of ports:240 • Number of clocks: 6 • Complexity:0.52M std cells • Metal layers: 9 Routing • Voltage domain: Multi Voltage Domain (0.95V and 1.15V) • Tool used: Synopsys icc2, Star RC, Primetime	• **Input files:** Imported Read netlist, logical and physical library. Read the SDC and the techfile. • **Floorplan:** created rectilinear shape of the block made the design more complicated and placed macro family based on fly lines. • **Power Planning:** Read the UPF file, which had details on the voltage domain creation and addition of level shifters between the 2 voltage domains. Also draw the power • **Placement:** verifying the placement with respect to placement and routing congestion and verify if the timing looks good at placement stage. Creation of path grouping based on timing analysis at placement stage. • **CTS:** Defining the NDR's for clock routing and apply the same for clock nets, and specify the buffers/inverters to be used for CTS. Also define the clock latency and skew requirement. • **Routing:** Definition of layers to be used for routing and enable timing driven route optimization. • **DRC and LVS:** Check for LVS to make sure that there are no opens. Check for DRC and clean up all the shorts and spacing violations

2. Physical design implementation

Design specifications	Responsibility
• Processor: CHIPTOP • Process technology:14nm • Operating frequency: 860 MHz • Memory: 30 macros • Number of ports:392 • Number of clocks: 8 • Complexity:0.37M std cells • Metal layers: 10 Routing • Tool used: Synopsys icc2, Primetime	• **Input files**: Imported Verilog netlist, Read SDC, UPF, TLU+ files and .lib&. lef, technology file • **Floorplan:** Create the floorplan with different utilization possibility, pin placement and macro placement based on fly lines, applied blockages to macro to prevent congestion. • **Power plan:** Read the UPF file and make sure all devices get power in the design and fixed missing vias, floating wires and fixed DRC violations. • **Placement:** Did placement and applied various strategies to control congestion. Creation of bounce placement based on timing analysis at placement stage. • **CTS:** Fixed transition and timing violation across various corners • **Routing:** Definition of layers to be used for routing and enable timing driven route optimization. • **Sign off checks:** Check for LVS and ERC to make sure there are no shorts and opens. Check for DRC'S spacing, enclosure area violations and antenna check in design. Parasitic present in the nets extracted using Start RC and performed post layout STA using primetime.

3. Design and Analysis of Multibit Multiply and Accumulate (MAC) unit

Performed In-memory dot product operations without effecting regular processes in von Neumann architecture by using in-memory unit by conventional 6T SRAM cell at, 45nm, 28nm and 90nm technology nodes, which shows that migration of data between memory and processor is efficient way and observed low power dissipation, delay and improved Read and Write mode operation using current mirror techniques in a design and done layout.
Tool used: Cadence virtuoso

4. IMC: In-memory Boolean Computation using 8T SRAM

By modifying the conventional 6T SRAM to 8T SRAM in such a way that we can perform the basic Boolean logic operations such as NAND, NOR, XOR by using the In-Memory Computing Scheme. this project is implemented using at 28nm technology and done layout.
Tool used: Cadence virtuoso

COURSES DONE

Digital Logic Design |VLSI system Design |Solid state device |VLSI Technology |Analog Circuits |PCB Designing |Digital IC design |Analog IC design |TCL Scripting |Micro controllers and microprocessors |Electrical Drives |Control Systems | Embedded Systems |Python |Power electronics |Signal and systems |Digital system engineering.

CERTIFICATES & ACHIEVEMENTS

- Advance Physical Design Training from VLSIGURU, Bangalore
- NPTEL python certification
- MATLAB onramp Certificate
- Received 1st prize in tesla SCIENCE FAIR inschool.
- Selected for Mathematics Olympiad 2015 (District level)

PERSONALITY TRAITS

- Optimistic.
- Good Communication skills and good problem-solving skills.
- Flexible and dedicated.
- Strong motivational and leadership skills.

PERSONAL DETAILS

Name	Bhukya Kiran
Father's Name	Bhukya Kishan
Date of Birth	28 Nov 1999
Gender	Male
Nationality	Indian
Languages Known	English, Hindi, Telugu
Hobbies	Cycling, Watching Movies, swimming

DECLARATION

I hereby declare that the above-mentioned information is correct to the best of my knowledge and belief.

Signature

BHUKYA KIRAN