V.N.S.SAI SUBRAMANYAM

nagasivasai1915@gmail.com
+91 8179012294
https://www.linkedin.com/in/naga-siva-sai-subramanyanvinukondaa7243b1b2

CAREER OBJECTIVE

Dedicated Engineer striving to get the best possible results with my skills to develop and renovate something new. I believe learning is endless and will always help us to move forward, therefore I try to leverage as a competent person to contribute to the distinct goals and long term growth of the firm in the field of VLSI.

EDUCATIONAL QUALIFICATION

BACHELOR OF TECHNOLOGY **(2020 - 2023)**
Gayatri Vidya Parishad College of Engineering (A) (Visakhapatnam)
Electrionics and Communication Engineering - **9.15 (CGPA)** Till date

DIPLOMA **(2017 - 2020)**
Dr.B.R.Ambedkar G.M.R Polytechnic (Rajahmundry)
Electrionics and Communication Engineering - **96%**

SECONDARY HIGH SCHOOL **(2016 - 2017)**
Sri Maharshi Vidya Niketan E.M School (Anaparthi)
9.8 (CGPA)

PROFESSIONAL TRAINING

Advanced VLSI Design and Verification Course
Maven Silicon VLSI Design and Training Center, Bangalore August 2022 till date.

VLSI DESIGN USING EDA TOOLS Online Workshop
Conducted by Entuple Technologies,July 2022.

NPTEL Online Cerification On CMOS Digital VLSI Design
Instructor: Prof. Sudeb Dasgupta,IIT Roorkee, March 2022.

NPTEL Online Cerification On Hardware Modelling using Verilog
Instructor: Prof. Indranil Sengupta, IIT Kharagpur, September 2022.

TECHNICAL SKILLS

Programming Skills:

- Verilog, System Verilog, UVM, C Programming, Python Programming.

Subjects Expertise:

- Digital Electronics, Microprocessor and Microcontroller, Network Analysis.

Operating System:

- Linux

Tools:

- Xilinx ISE synthesis and simulator tool
- Quartus prime altera 19.1 synthesis tool
- Modelsim mentor graphics simulator tool
- Xilinix Vivado synthesis and simulator tool
- LT Spice (Spice Simulator).

Boards:

- Intel Altera's FPGA
- EDGE Artix 7 FPGA

PROJECTS

Router 1x3 - Design and Verification :

- The Design uses packet based protocol where it receives data serially byte wise from the source LAN and monitors the three destination LANs. When data reading is acknowledged,the router can send the data serially byte wise simultaneously to all three of them. It also does parity checking to verify the data packets received from the source LAN.

Soil Monitoring Bot Using FPGA in Verilog :

- Build a “Soil Monitoring Bot" for E-yantra robotics competition conducted by IIT-Bombay. The bot follows a line on the map and collects data through various sensors embedded to it Designed and interfaced UART,ADC,X-bee modules on FPGA using verilog.

IoT Based Project Smart Gas Stove

- Interfaced multiple modules to nodemcu to add smart and safe features to an LPG gas stove, where counting cooker whistles, timers and remote control through mobile app adds smartness. While gas leakage detection and sending alert sms to the user through mobile app adds safe feature.

INTERNSHIP

Trained on Cisco (CCNA) Modules:

- Introduction to the Networks, Routing and Switching concepts of the Networks which are simulated in the Packet Tracer software

ACHIEVEMENTS

- Best in academic grades and top scorer in VLSI Design, VLSI Testing and Testability, and IoT courses.
- Participated in District level school science fair and rewarded as cash prize for presenting the project.

EXTRA-CIRCULAR ACTIVIES

- Member and Volunteer in Yfs Club.
- Participated in several Cricket tournaments .
- Played a crucial role in organizing Tech-fest in college role.

BEHAVOURIAL SKILLS

- Adaptability.
- Patience.
- Quick learning.
- Leadership.

HOBBIES

- Playing Cricket.
- Spending time with family and friends.
- Cooking.

DECLARATION

I hereby declare that all the information furnished above is genuine to the best of my belief.

Date:

Place : Visakhapatnam

V.N.S SAI SUBRAMANYAM