Bodasakurthi Sekhar

Physical Design Engineer

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Block no 14 f-2 jnnurm colony kommadi village

Madhurwada Visakhapatnam 530048

physical design flow from RTL to GDS2 including input & output files, IR drop, Congestion, timingreports, timing paths. Have understanding of CMOS basic logic design & TCL

EDUCATION

- **VLSi physical design**
  VLSI guru Nov 2021 - April 2022
- **Masters of Sciences in Electronics**
  Gitam university Visakhapatnam
  June 2019 - Aug 2021
- **Bachelors of Sciences in Electronics**
  Presidency degree college
  June 2015 – May 2018
- **Inter**
  Sri Basara Junior College
  April 2013 – April 2015

EXPERIENCE

Physical design trainee
Bitsilica
May 2022 - present

Intern
Soroka soft india pvt ltd
March 2021-dec 2021

CERTIFICATES

VLSI Physical Design -VLSI GURU(11/2022)

SKILLS & TOOLS

Linux & windows | ICC2 | TCI | PD | PnR | STA | Floorplanning | Placement

PROJECTS

- VLSI - icc2 Block level engineer (Buffer)
  - Pd flow on 10nm with 1.2M std cells and 123 macro count
  - Applied NDR to avoid crosstalk
  - Added exclusive bounds to overcome timing issues
- VLSI - icc2 Block level engineer (Dec 2021 - April 2022).
  - pd flow on 40nm technology node with 200k std cell , 42 macros
  - 9 metal layers ,supply voltage 1.1V
- VLSI - High precision Multi Pulse Generation for EW ELINT Domain
  - it is a real time project by Bell Laboratories HYD
  - Xilinx spartan 6 FPGA Board, Xilinx ISE 13.1
  - Oscilloscope

LANGUAGES

English
Full Professional Proficiency

Telugu
Native or Bilingual Proficiency

Hindi
Full Professional Proficiency

INTERESTS

Cricket | To Watch Travelling vlogs