MOHAMMAD.SHANNU

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EDUCATION

- **M.Tech (VLSI Design): 78%**
  College: Sri Vahini Institute of Science andTechnology. JNTUK- 2016 March
- **B.Tech (ECE): 67%**
  College: Sri Sarathi Institute of Science andTechnology. JNTUK- 2013

TECHNICAL SKILLS

VLSI Design & Verification

- HDL: Verilog
- HVL: System Verilog
- Verification Methodologies: Constraint Random Coverage Driven Verification, Assertion Based Verification.
- TB Methodology: UVM
  Protocols: AXI, AHB, UART, I2C, SPI (Yet to be covered in course)
- EDA Tools: Modelsim & QuartusPrime
- Operating System: Linux
  Scripting Languages: Perl (Yet to be covered in course)
  Programming Languages: C &C++

CAREER OBJECTIVE

A relatively fresher in the field of VLSI, seeking full time employment in Design Verification roles. Quick to grasp new concepts, ideas and develop innovative solutions to problems. continuously demonstrating a high level of motivation and dedication that are required to meet deadlines.

PROFESSIONAL TRAINING

- **ADVANCED VLSI DESIGN AND VERIFICATION COURSE, MAVEN SILICON, Bengaluru, 27.07.2022 -Till now**

PROJECTS

-Maven Silicon

RAM SoC Verification – UVM

- The design includes four instances of 4096 x 64 RAM chips.
- Used four instances of both read & write agents for verification.
- HVL – System Verilog | Methodology - UVM | EDA Tool - QuestaSim

1 X 3 ROUTER RTL DESIGN AND VERIFICATION

- Description: The Router accepts data packets in a single 8-bit port and routes them to one of the three output channels channel0, channel1 or channel2. The main blocks within Router are Synchronizer, Controller (FSM), Register, FIFO Blocks.
- HDL -- Verilog | EDA Tools - ModelSim | Synthesis Tool –Quartus Prime.
- Verification done using Verilog testbenches

-Vahini college

An Efficient Design of Low-Power Booth Multiplier Design Using Fixed-Width (MTech)

- Tools: MAT Lab, Modelsim, Xilinix ISE Design Suit
- Description: An Efficient Design of Low power Booth Multiplier Design using Fixed-Width Replica Redundancy
  By adoptive algorithmic noise tolerant (ANT) architecture with the fixedwidth multiplier to build the reduced precision replica redundancy block (RPR)
- The postponed (ANT) architecture can meet the demand of High precision low power consumption, and area efficiency. We design the fixed-width RPR with error compensationcircuit via analyzing of probability and statistics.

Role: Team Leader

WORK EXPERIENCE

Five Years' Experience

- Worked as an Assistant. Professor in ASIST since 2021 june-2022july
- Worked as an Assistant. Professor in SVIST since 2018 june-2021May
- Worked as an Assistant. Professor in NRI IT since 2017 april-2018May

CORE SKILLS

Digital Electronics:
Combinational & Sequential circuits,
- FSM, Memories

Verilog Programming:
- Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end
- & fork join blocks,
  looping & branching construct, System tasks & Functions, compiler directives,
- FSM coding,
  Synthesis issues, Races in simulation,
- pipelining RTL & TB Coding,
  Advanced Verilog & Code
- Coverage: Generate block,
  Continuous Procedural Assignments,
- Self-checking testbench, Automatic Tasks,
- Named Events and Stratified Event Queue, Code Coverage: Statement and branch coverage,
- Condition & Expression Coverage, Toggle & FSM Coverage

POSISTIONS & RESPONSIBILITIES

- **M.TECH COORDINATER**: an institute of Amrutha Sai Engineering college.
- PROJECT GUIDE: on the period of teaching profession

EXTRA CURRICULAR ACTIVITIES

- Achieved One time Star Performer of the month in MavenSilicon during Training.
- State Player in Athletics'.
- Active participation in Paper-Postal Presentation &Workshops.

LANGUAGES KNOWN

- Telugu
- English
- Hindi

DECLARATION

I hereby declare that all the above information is true looking forward to serve your great esteemed organization and also, I will fulfill your expectations with my sincere efforts.

DATE:
PLACE: Mylavaram **(MOHAMMAD SHANNU)**