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Career Objective

To Pursue a Challenging Career in a high-level professional environment and to be a part of Progressive organization that gives a platform to utilize and enhance my skills and to work for the growth of organization.

Core Competancy

- Complete Understanding of ASIC Design Flow and Physical Design Flow.
- Good Knowledge and understanding of STA concepts.
- Fixing setup and hold violations. Understanding of timing reports.
- Worked on floor plan with high utilization and ensuring good contiguous core area for standard cells.
- Implemented power plan to connect power pins of all macros and standard cells to supply voltage without any PG DRC violations and achieved specified IR Drop limit.
- Good working knowledge of Verilog code, LINUX and scripting knowledge TCL.
- Hands On experience on Synopsys Prime Time and IC Compiler II, Cadence Virtuoso and Genus.
- Good Knowledge in Logic Design, CMOS and Basic Electronic devices.
- Good Communication and Managerial skills, Leadership quality, Quick Learner, Active listener.
- Adaptable to challenging environment, .Time Management, Problem analysis and Decision Making capability.

Education Details

Advanced Diploma in ASIC Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Global Academy Of Technology, with 8.6 CGPA

2018

RNS Pre University College, with 84.8 %

SSLC **2016**

VSS International Public School, with 9.4 %

Domain Specific Project

RV-SKILLS CENTER FOR EMERGING TECHNOLOGIES

Graduate Trainee Engineer Sep-2022 to Oct-2022

STATIC TIMING ANALYSIS (STA) and TCL Scripting

Description

Timing analysis on different path for registers and latch based designs having multi-cycle paths and half-cycle paths, considering OCV, CRPR, uncertainity, clock skew.

Tools

Synopsys Prime Time

Challenges

- Analysis of setup and hold slack violations, understand the cause for those violations.
- Understanding of derate factors,PVT corners, Global Variations, OCV and AOCV
- Analysis of different timing exceptions like false path, multi-cycle path and half-cycle paths.

RV-SKILLS CENTER FOR EMERGING TECHNOLOGIES

Graduate Trainee Engineer Oct-2022 to Jan-2023

FLOOR PLAN AND POWER PLAN

Description

TECHNOLOGY-40nm Macro Count -34 Standard cell count- 38887, Area- 4.2mm Supply- 1.1V Clock Frequency- 1GHz Number of metal layers- 7 Power Budget- 600mW IR Drop< 55mV

Tools

Synopsys IC Compiler II

Challenges

- Manually placing hard macros using data flow diagram in such a way that to provide the maximum contiguous core area and to make all pins of the macros are accessible.
- Implementing the power plan to meet the target IR drop and made power mesh DRC clean.
- Maintaining uniform orientation of hard macros and adding placement and routing blockages in required locations.

RV-SKILLS CENTER FOR EMERGING TECHNOLOGIES

Graduate Trainee Engineer Nov-2022 to Jan-2023

PLACEMENT AND CLOCK TREE SYNTHESIS

Description

Timing driven and congestion aware standard cell placement in Non-SPG flow is being done with optimum core utilization and building clock tree and routing all clock pins with optimized clock skew in both classic and CCD modes.

Tools

Synopsys IC compiler II

Challenges

- Performed timing driven and congestion driven placements and HFNS in order to minimize logical DRC's by thus improving timing QoR.
- Synthesizing clock tree by providing NDR rules and performed detailed routing for all clock nets with DRC clean in both classic and CCD modes.
- Performed sanity checks before and after each stage of physical design flow.

RV-SKILLS CENTER FOR EMERGING TECHNOLOGIES

Graduate Trainee Engineer Dec-2022 to Jan-2023

ROUTING AND DFM

Description

Routing all standard cell pins an d hard micro pins using metal layers, performing via optimization and post route optimization by taking into account of cross talk effects on timing.

Tools

Synopsys IC Compiler II

Challenges

- Fixing antenna violation using metal hopping and antenna diodes manually.
- Clearing all DRC violations and LVS violations in order to make sure that design can be manufacturable.
- Analyzing timing reports and other required reports in each stage.

B.E / B.Tech Academic Project

Global Academy Of Technology

OTP Based Electronic Lock System with Security Alert

Description

The main objective of this project is to develop a OTP based lock system with security alert features. It was done using GSM, interfacing it with Arduino. The OTP will be sent to registered mobile numbers and alert will also be sent if OTP is wrong.

Tools

Hardware- Arduino Board, GSM SIM800, Keyboard, LCD Display, Vibration Sensor, IR Sensor.
Software- Arduino IDE.

Challenges

- Developing the OTP based electronic system to unlock the door with security alert. To interface the GSM module with the microcontroller to transmit the OTP to authorized mobile.