Jaganath A

jaganath28101998@gmail.com, 8970307001

Kolar-563101, Karnataka

Career Objective

Seeking a challenging position in an organization to utilize my technical expertise and interpersonal skills thereby contributing towards organizational business goals and for self-development.

Core Competancy

- Hands on experience on IC COMPILER II involving FLOOR and POWER PLANNING , PLACEMENT , CLOCK TREE SYNTHESIS and ROUTING.
- Hands on experience on PRIMETIME for STATIC TIMING ANALYSIS and timing closure at block level by analyzing the timing reports at multiple modes (test,func) and scenarios.
- Worked on creating a Floorplan according to the macro placement guidelines with good contiguous area, and acceptable congestion between macros.
- Understanding Clock Tree Synthesis (CTS), types of clock trees, Non default routing (NDR) rules for clock routing. Understanding Routing, DFM and Antenna issues.
- Good knowledge on ASIC FLOW (RTL to GDSII), Digital electronics, Circuit Analysis, Basics of MOSFET theory.
- Analyzed and understood the constraints to specify the False paths, Multi Cycle paths, Asynchronous clocks, CRPR and PVT corners.
- Understood a bad floorplan leads to a various type of physical DRCs which are difficult to fix at routing stage.
- Have the knowledge of applying all the STA concepts and co-relating them to the app-options and Versatility with Recommended Methodology TCL scripts to automate design.
- Good knowledge on clock abnormalities - clock jitter, clock latency, clock skew, and the effect of clock skew on timing, Understanding Signal integrity, Xtalk.
- Worked on Placement plan and need for Physical cells, Tie cells, Clock gating cells, Spare cells in the design. Understanding DFT and scan chain reordering.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

JSS Academy Of Technical Education , Bengaluru, with 6.60 CGPA

2017

Chinmaya Independent Pu College, Chokkahalli, Kolar, with 69.33 %

SSLC **2015**

Vidya Jyothi Eng Medium High School , Basavanatha, Kolar, with 65.76 %

Domain Specific Project

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Aug-2022 to Feb-2023

Design of SOC Physical Design Block

Description

Implementation of block level chip in 40 nm technology with a frequency of 833MHZ.1.1V is the supply voltage. Block having five modules inside for data transfer, encryption and decryption. Used CCD to get good timings in the clock and data path.

Tools

IC Compiler II, Primetime from Synopsys.

Challenges

- Creating a good floorplan by ensuring a contiguous area between the macros. Meeting the IR drop by giving appropriate values of width and pitch for metal layers used for powerplan.
- Providing appropriate spacing between the macros to bring down the congestion. Providing keepout margin, routing blockage, and placement blockage t avoid DRC violations.
- Building a clock tree by achieving the clock skew with in the target. Post CTS got DRC error such as short and it's resolved by reroute the metal having shorts.
- Fixing Antenna violations by metal jumpers and by inserting antenna diode. Rerouting the existing nets manually while solving antenna issues to avoid new DRC's.

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Aug-2022 to Feb-2023

STATIC TIMING ANALYSIS

Description

Timing analysis for Flip Flop and latch based timing paths working under different operating conditions considering OCV , AOCV , CRPR, Uncertainty while honouring the constraints file.

Tools

Synopsys PrimeTime

Challenges

- Setting the constraints (SDC) like latency, transition, input and output delays for the given block needs good understanding of the STA concepts.
- Need to have the good knowledge on different timing paths like reg to reg, in to reg, reg to out, in to out and timing paths that are having Latches in them was challenging.
- Requires good attention while analysing the effects like Signal Integrity which deals with the Xtalk analysis.
- Analysing the timing reports for various timing paths that are having latches and flip flops and understanding difference between PBA and GBA was challenging.

B.E / B.Tech Academic Project

JSS Academy Of Technical Education , Bengaluru

Deep Learning Based Inventory Of Agriculture Crops and Organized Yield Production Using Satellite Images

Description

We provided a brief introduction to the research works which are applied in the agriculture domain for variety recognition, yield estimation, quality detection, crop mapping, organized production, and other tasks.

Tools

Software - Windows7, Colab. Hardware - PC with Intel i5, 8GB RAM, 128GB ROM

Challenges

- Getting the real time photos, categorizing the crops, estimating the duration of the crop through the satellite photos.