Vidya C N

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Career Objective

Seeking a position as a Physical Design Engineer with an opportunity for advancement to build a productive career for self and company.

Core Competancy

- Fundamentals of ASIC design flow.
- Comprehensive knowledge in concepts of Static Timing Analysis.
- Efficient in timing aware, congestion driven macro placement during the Floorplanning.
- Hands on experience with EDA Tools: APR: Synopsys ICC-2, STA: Synopsys PrimeTime.
- Examine and modifying Tcl -Script.
- Scripting Languages - Perl Scripting (Intermediate)
- Programming Languages: VHDL (Intermediate)
- Working with the Linux Environment.

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Rajarajeshwari college of engineering, with 9.04 CGPA

2018

Sri Aurobindo Composite PU College , with 87.33 %

SSLC **2016**

Kids international school, with 88.96 %

Domain Specific Project

RV-skills center for emerging technologies

Graduate Trainee Engineer Aug-2022 to Feb-2023

Lakshya

Description

Block-level Floorplanning and PowerPlanning: Implementing block-level design for Lakshya subsystem in 40nm technology. Supply voltage 1.1V, IR drop 5% of operating voltage, Standard cell count 38887 and Hard macros 34, Frequency of operation 833Mhz.

Tools

Synopsys IC Compiler 2

Challenges

- Placement of macros using appropriate data flow of blocks
- Creation of efficient power mesh within the IR drop limit.
- Fixing floating shapes for metal layer and fixing if any.

RV-skills center for emerging technologies

Graduate Trainee Engineer Aug-2022 to Feb-2023

Lakshya

Description

Block level Placement and CTS : A Timing driven and legalized placement of standard cells, ensuring good routability, building a Clock Tree to get an optimized skew, reducing timing violations, design rule violations checks, and minimum WNS,TNS.

Tools

Synopsys IC Compiler 2

Challenges

- Generation and analysis of Timing reports.
- Fan out synthesis during placement.
- Timing analysis after each stage.

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Graduate Trainee Engineer Aug-2022 to Feb-2023

Lakshya

Description

Static Timing Analysis for various Timing Paths: Setup and Hold analysis and interpreting timing reports, dealing with False Paths, Half cycle paths, Multi-Mode paths, and Reporting the violations in the logical DRCs.

Tools

Synopsys Prime Time

Challenges

- Generation and analysis of Timing reports with waveforms.
- Identifying and constraining timing paths, computing setup and hold slack .
- Understanding the concepts and the usage of timing exceptions.

B.E / B.Tech Academic Project

Rajarajeshwari college of engineering

A Novel Approach For Smart Indoor Farm

Description

A Smart indoor farm reduces plants' growth cycle by half and increases the yield per square meter by automation of irrigation, temperature control and aiding rapid photosynthesis by using RYB LEDs.

Tools

Arduino IDE, Arduino mega MCU board, ESP8266 , soil moisture sensor, water level sensor,DHT22,LED strip

Challenges

- Designing of system and blocks. Integration of all the blocks and searching for an erroneous part, if any. Learning how to program in Arduino IDE.