Y SHARMILA

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Hyderabad, Telangana, India.

OBJECTIVE

Aspire to secure a responsible career opportunity to utilize my skill and knowledge, and in the process of learning, make a significant contribution to the success of the organization.

TECHNICAL SKILLS

- Digital Design in Electronics
- Design For Testability (DFT)
- Verilog
- Advanced verilog and Code Coverage
- Static Timing Analysis
- FPGA (Field Programmable Gate Array)
- Tools:
  - Cadence-Virtuoso Platform,
  - Mentor Graphics-Questasim, QuartusPrime, Tessent tools.
- OS: Linux

MY EDUCATION

2017-2019

VELLORE INSTITUTE OF TECHNOLOGY, VELLORE

M.TECH

- Post Graduation in VLSI Design
- CGPA - 7.77

2012-2016

SAI VIDYA INSTITUTE OF TECHNOLOGY,BENGALURU

B.TECH

- Graduation in Electronics and Communication Engineering.
- Percentage - 69.7.

2010-2012

NARAYANA JR COLLEGE,HINDUPUR A.P

BOARD OF INTERMEDIATE EDUCATION

- Intermediate education in MPC(Maths, Physics and Chemistry).
- Percentage - 94.5.

2010

CHINMAYA VIDYALAYA, HINDUPUR,A.P

BOARD OF SECONDARY EDUCATION

- Secondary School Certificate(SSC).
- Percentage - 87.0

PROFESSIONAL TRAINING

- **Advanced VLSI Design and DFT** Course, Maven Silicon Design and Training Centre – Bangalore [Nov 2021– Oct 2022].

ACADEMIC ACTIVITIES

- Participated in IEEE workshop on “**RTL Verification using Verilog**”.
- Presented a seminar on “**People Detection and Tracking from Aerial Thermal Views**” in B.E.
- Attended IEEE International conferences on **Microelectronic Devices, Circuits and Systems on Low power verification and I/O Interface design** during M.Tech.
- Presented a project model of **"Student smart campus access management using RFID and NFC"** in B.E.
- Presented a paper on **"High Immune Electromagnetic Interference Filter"** in SET conference during M.Tech.

CO-CURRICULAR ACTIVITIES

- Volunteered BE college fest events and activities.
- Won 2nd prize in Inter-School Kabaddi competition during high school.
- Participated in Intra-School Volley ball competitions during high school.
- Served as a junior in NCC Kurnool Division
- Was a member of ceremonial marching band in high school.

KEY PROJECTS

RISC-V MICRO ARCHITECTURE IMPLEMENTATION

Maven Silicon, Bangalore, Jun'22-Aug'22(Post Academic)

- Synopsis:
  - Design: Designed RISC-V Micro Architecture with 3 stage pipelining. This includes design of (R,I,S,B,U,J) types of RV32I instructions. Each pipelining stage has various blocks such as PC MUX, Immediate adder, integer file, Machine control, CSR file etc.,
  - Verification: This design has been successfully implemented and verified using verilog and UVM.
  - Testing (DFT): ATPG, Boundary scan, Scan chain insertion and EDT IP insertion have been efficiently applied on RISC-V RTL. Improved test coverage and verified test patterns for any mismatches.
- Language Used (HDL): Verilog
- Tool: Model sim, Questasim and Mentor Graphics-Tessent tool.

ROUTER 1X3-RTL VERIFICATION

Maven Silicon, Bangalore, March 2022 (Post Academic)

- Synopsis: Designed a 1x 3 router that accepts data packets from source server and sends to three destination client networks where the packets follow TCP/IP Protocol. This design includes FIFO, Synchronizer, Controller, Register and Router top modules. These modules are successfully simulated and synthesized.
- HDL: Verilog
- EDA Tools: Model sim, Quartus Prime and Questasim.

DESIGN OF HIGH PERFORMANCE & LOW POWER SENSE AMPLIFIER FLIPFLOP (SAFF)

VIT, Vellore, Nov'18- Apr'19 (Academic-Master Thesis).

- Synopsis: Designed a novel SAFF on cadence virtuoso platform with 180nm and 90nm CMOS technology. This SAFF has an optimized design that yields better performance.
- The results show the clock to Q delay reduction of 38.4% and the power consumption reduction of 16.8%, which is observed as 50μW using load capacitance of 70fF at the output of the flip flop.
- Tool: Cadence virtuoso

PERSONAL TRAITS

- Eager to learn new things
- Aspire to contribute effectively and efficiently at work.
- Ability to work independently and in group as well.

HOBBIES

- Cooking
- Art
- Travel
- Reading
- Listening to music
- Volunteering

PERSONAL INFO

- **Date of Birth** : 30th Jan 1995.
- **Languages Known** : English, Telugu and Kannada.
- **Nationality** : Indian.

DECLARATION

- I do declare that the information furnished is true to the best of my knowledge and I take the responsibility for the correctness of the details given.

Date & Place:
11/04/2023,
Hyderabad.

Sharmila Y