PAVAN HEGDE

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CAREER OBJECTIVE

Trained VLSI Design Verification Engineer, looking forward to apply my Knowledge in the practical world to gain expertise in the domain. Hardworking Engineer to contribute to the world of VLSI technology to succeed in an environment of growth and excellence to get a job which provides me job satisfaction and self-development.

WORK EXPERIENCE AND COURSES

ADVANCED VLSI DESIGN AND VERIFICATION COURSE.

Maven Silicon VLSI Design and Training center, Banglore.
August -2022 to till date.

PROJECT ENGINEER.

Wipro Limited, Bangalore.
March-2021 to September-2022 (1.6 Years)
Domain: SAP HCM.
Key Responsibility:

- Analyzing the Client requirement and implementing the SAP HCM Personnel Administration, Organization Management changes
- Functional unit testing of the different Minor works changes

EDUCATION

COURSE	INSTITUTION	EXAMINATION BOARD	YEAR	% Or CGPA
B.E (ECE)	Banglore Institute of Technology,Banglore	VTU	2020	8.59
PUC	Sri Adichunchanagiri PU College, Shimoga.	Karnataka PU board	2016	94.66
SSLC	Basaveshwara High School, Ripponpete.	Karnataka state board	2014	89.12

FOUNDATION SKILLS

HDL: Verilog

HVL: System Verilog

Verification Methodologies: Constraint Random Driver Verification | Assertion based Verification

Protocol: APB | SPI

EDA Tool: Mentor Graphics – Questasim, Quartus Prime and Modelsim

Core skills: RTL coding using Verilog, CMOS Fundamentals, Functional and Code Coverage, STA, Test Bench creation using System Verilog and UVM Methodology.

Programming Languages: **C** [Datatype | Array | Pointers | Functions | Structure

DESIGN SKILLS

Digital Electronics: Combinational circuit | Sequential Circuits | FSM | Memories

Verilog Programming: Data types | Delays | Structured Procedure | Looping and Branching Construct | Tasks and Functions | FSM Coding | Code Coverage | Races in simulations | Compiler directive.

VERIFICATION SKILLS

Memories: Dynamic array | Queue | Associative array | Task and functions | pass by reference

Basic and advanced object -oriented programming: Handle assignments | Copying the object contents | Inheritance | Polymorphism | Statice properties | Virtual classes

Constraint Randomization: constraint overriding and inheritance | Distribution and conditional constraints | Soft and inline constraints | Assertions

Thread synchronization technique and Functional Coverage: Events | Semaphores | Mailbox | Cover groups | Cover bins | Cross-coverage| CRCDV

UVM: UVM Objects and Components | UVM Factory | Overriding Methods | Stimulus Modelling | UVM Phases | UVM Configuration | TLM | UVM Sequence, Virtual Sequence and Sequencer | Basics of RAL

Router 1x3 – RTL Design and Verification **- Maven Silicon.**

Description: The router accepts data packets on a single 8-bit port and routes them to one of the three channels, channel0 or channel1 or channel2

Responsibilities:

Design of FIFO, FSM, Register, Synchronizer blocks

- Verification of all sub blocks using Linear test bench
- Design of Router top module by instantiating the sub blocks
- Verification of the Router module using UVM Methodology
- Synthesis of the design

TECHNICAL PROJECTS

SPI Controller Core - Verification. **– Maven Silicon.**

Description: The SPI core provides serial communication capabilities with external device of variable length of transfer. This core is configured to connect with 32 slaves

Responsibilities:

- Architecture class based verification environment using UVM
- Define verification plan
- Verified the RTL module using System Verilog
- Generated function coverage for the RTL verification sign-off

CERTIFICATION

- SAP NetWeaver Certification issued by SAP
- Participated in KSHAMATHA soft skills training conducted by World Konkani Center
- Python Basics Certification issued by HackerRank

ACHIEVEMENTS

- 1st place in sub district level essay competition
- Alumni of Foundation for Excellence
- Star of the Month of a training batch in Maven Silicon from September-2022 to December-2022 and March-2023

HOBBIES

- Playing Cricket, Kabaddi
- Watching movies
- Participating in marathon

DECLARATION

I hereby declare that all the information furnished above is true to the best of my knowledge.

DATE:

PLACE: Bengaluru.

Pavan Hegde