MUNAPARTHI HIMA BINDU

ADVANCED PHYSICAL DESIGN & VERIFICATION TRAINEE

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Kancharapalem,VSPT,Andhra Pardesh

Career Objective

Looking for the position in Physical design engineer in a VLSI organization.Where my training experience and my innovative knowledge, technical skills can enhance me to change my career towards VLSI industry.

Work Experience

BITS VIZAG, AVANTHI &VISAKHA engineering colleges in Visakhapatnam.
Worked as Assistant professor.
June 2019 - Sep 2022
Subjects i expertise are : VLSI DESIGN, EDC, EMBEDDED SYSTEMS,
MPMC,STLD, EMI.
SKILLS:Xlinix ISE lab,EDC lab,STLD lab.

Professional Certification

PROFESSIONAL TRAINING MAVEN SILICON
July 2022 - Jan 2023
Advanced Physical Design & Verification

VLSI Domain Skills

HDL: Verilog
EDA Tool: Mentor Graphics -Quartus® Prime and Xlinix - ISE.
Domain: Tanner EDA, Physical Design flow including floor planning, Placement,STA,CTS & Routing and Signoff, Oasys, Aprisa and Calibre from Siemens ,static timing analysis using Synopsys Prime Time, Synopsys fusion compiler (rtl to gds-II flow).
Programming Languages:C-Language, Python,TCL.
Operating Systems: Working knowledge on Windows and Linux
Scripting Languages : TCL
Core Skills : RTL Coding using Synthesizable constructs of Verilog, FSM based design,Simulation, CMOS Fundamentals, Static Timing Analysis,Logic Synthesis, Floor planning, Placement, Routing, Signoff.

Education

2018
Master's in VLSI Design & Embedded Systems Engineering from GVP college of Engineering (A), Visakhapatnam with 75%.

2016
Bachelor's in Electronics and Communication Engineering from AIET College of engineering Visakhapatnam with 74.4 %.

2012
Intermediate from NRI Junior College,Visakhapatnam with 79.5%

2010
X Class from Visvodaya High School,Visakhapatnam with 63.3%

Subject Expertise

DigitalElectronics,VLSI,CMOS,EMI,Analog electronic, Microprocessors/ Microcontrollers

College Skills

Software languages: C, C++, PYTHON languages.
Tools used in Engineering

- MATLAB - Digital Signal Processing
- Keil MDK or Arduino IDE - Microcontroller Programming MASM or TASM - Assembly Language Programming (8085 or 8086).
- Boards-Having idea of Arduino UNO,Nano,Nodemcu, Raspberry PI.
- Cadence Virtuoso - Designing the layout and finding it parameters characterises,Custom IC design and package/PCB design/analysis.

Achivements

- **Star of The Month** for August, December and January at Maven Silicon VLSI Design and Training Center, Bangalore
- Secured more than 95% of marks in engineering chemistry in entire education career.
- I won 2nd topper in B.Tech 2nd year. Participation in Kho-kho district level at Sri Vasavi Engineering College, Tadepallegudem.
- Organized Freshers' and Farewell in college.
- Organized workshop on Poshan Abhiyaan

Hobbies

- Sketching
- Dancing
- Listening Music & Singing songs

Strengths

- Critical thinking
- Team motivator
- Easily adjustable in new environments
- Good team leader ability
- Quick learner

VLSI Design Skills:
Digital Electronics Combinational & Sequential circuits, FSM, Memories, CMOS implementation, Stick diagram.

STA: STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks Clock domain and Variations, Clock Distribution Networks, Fixing timing failure.

Verilog Programming: Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks, looping & branching construct, System tasks & Functions, compiler directives, FSM coding,Synthesis issues, Races in simulation, pipelining RTL & TB Coding.

Physical Design: Logic Synthesis, Floor planning, Placement, Routing, Clock Tree Synthesis and Timing Analysis using Aprisa, DRC, ERC, LVS and signoff using Calibre.

FPGA Design Tool Skill-set: Have worked on Xilinx-ISE 14.7 and have sound knowledge on converting RTL code to .bit file and download the same to the FPGA kit. Have worked on developing Testbench using Xilinx ISE.

WORKSHOPS

- Participated in a two day workshop on Advanced antenna technology and electromagnetic interference at DIET College with IEEE bodies in B.Tech.
- Participated in a two day workshop on “Fractional Order Modelling” conducted in G.V.P college of Engineering.
- Attended Electronics Knowledge in NSTL, Visakhapatnam.
- Attended Signaling System Knowledge in DD, INDIA.
- Participated in 1-week FDP on Python 3.4.3 organized by Vaagdevi College of Engineering during lockdown.

Major projects during Professional training

Physical Implementation of Project- Router 1x3

Description : The router accepts data packets on a single 8-bit port and routes them to one of the three (FIFO's) output channels channel 0, channel 1 and channel 2.

Responsibilities : Designed 1x3 router along with sub blocks and implemented RTL using Verilog HDL Simulated with Modelsim and Synthesized design with Quartus® Prime.

Taken Gate Level netlist after Oasys lab .

Implementing Floor Planning,Power Planning,Placement Implementing Clock Tree Synthesis, Routing process on the netlist.Performing timing analysis and achieve timing closure.Perform DRC, ERC and LVS for signoff Exporting the final GDS-II. Reduced setup and hold violations in router project.

Physical Implementation of RISC-V Design

Description : The RV32I Processor is designed to support all RV32I Base Integer Instructions (Total -39). It's a three stage
pipelined processor which executes 32 bit instructions in program order.

Responsibilities for Design:
Synthesizing the RISC-V RTL and generate the Gate Level netlist.Implementing floor planning,Placement and Routing process on the netlist.Implementing Clock Tree Synthesis. Performing timing analysis and achieve timing closure. Perform DRC, ERC and LVS for signoff Exporting the final GDS-II

M.TECH PROJ ECT

FAULT OBJ ECT DETECTION SYSTEM USING ULTRASONIC SENSORS

Description : Project aims at detecting the dimensions and weight of the object using sensors and sends fault object alert to end user through IoT.

Responsibilities : Learned coding of python,vpn,working of Arduino,Raspberry PI board interfacing with sensors.

DECLARATION

I here by declare that all the information provided in this resume is true .

D AT E : 3-3-2023

PLACE : Visakhapatnam

Munaparthi Hima Bindu