Yashasvi Suryavamshi .K.S

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OBJECTIVE

A fresher in the field of engineering, intended to build a career with commitment and dedication, which will help me realize my potential and enhance my skill set in the field of VLSI and embedded system and help with the growth of the organization.

PROFESSIONAL TRAINING

Advanced VLSI design and DFT course
Maven Silicon VLSI design and training center, Bangalore
August 2021 till date

EDUCATIONAL HISTORY

B.Tech in ECE

Vishveshwaraya technological university |2017-2022

- Global Academy of Technology
- Graduated with 7.65 (CGPA)
- From Karnataka

11th and 12th

Karnataka state board | 2015-2017

- Vidhya Vardhaka Sangha
- Graduated with 75%
- From Karnataka

10th

Karnataka state board | 2015

- Anupama English School
- Secured 90%
- From Karnataka

HOBBIES

- Driving
- Karaoke
- Cooking

PERSONAL TRAITS

- Quick Learner
- Hard Working
- People Person
- Independent
- Team Player

SKILLS

FOUNDATION SKILLS

- DESIGN SKILLS: Digital Electronics, Combinational and Sequential circuits, FSM, Memories, CMOS implementation, Stick diagrams.
- HDL: Verilog, VHDL
- OPERATING SYSTEM: Linux
- Scripting Language: Perl Scripting.
- Core Skills: RTL Coding using Synthesizable constructs of verilog, FSM based design, Simulation, CMOS Fundamentals, Code Coverage, Functional coverage, Synthesis, Static Timing Analysis, Assertion based verification using System Verilog Assertions.

DESIGN SKILLS

- DESIGN SKILLS: Digital Electronics, Combinational and Sequential circuits, FSM, Memories, CMOS implementation, Stick diagram
- VERILOG PROGRAMMING: Data types, operations, process delays in verilog, begin-end and fork join block, looping and branching constructs, system tasks and functions, compiler directives, FSM coding, Synthesis issuses, Races in simulation, pipeling RTL and TB coding
- ADVANCED VERILOG: Generate block, Continuous Procedural Assignments, Self checking testbench, Automatic Tasks, Named Events and Stratified Event Queue.
- CODE COVERAGE: Statement and branch coverage,Condition & Expression Coverage, Toggle & FSM Coverage
- STA: STA Basics, comparison with DTA, Timing path and constraints, different types of clocks, clock domain and variations, clock distribution networks, fixing timing failure.
- FPGA Design Tool Skill-set: Have worked on Xilinx-ISE 14.7 and have sound knowledge on converting RTL code to bit file and developing testbench.

DFT SKILLS

Experience with multiple aspects of the following:

- ATPG, Test coverage.
- JTAG, BSDL, IJTAG.
- Memory and logic BIST.
- Synthesis scan stitching.
- Memory BIST implementation.
- Scan/JTAG/Boundary-scan insertion and ATPG pattern generation.
- Test coverage and fault coverage analysis.
- Knowledge/experience with ATPG/DFT tools: Tessent, System Verilog, RTL.

VERIFICATION SKILLS

- System Verilog HVL: Memories, Functions, Interface, Basic and advanced object-oriented programming, Constraint Randomization, Thread synchronization techniques, Functional coverage, Interface and clocking block, Inheritance and Polymorphism, Constraint randomization - Inline, distribution, conditional, soft and static constraints. Mailbox and semaphores, Functional coverage, CRCDV and regression testing.
- System Verilog Assertions: Types of assertions, assertion building blocks, sequences with edge definitions and logical relationship. Sequences with different timing relationships. clock definitions, implication and repetition operators, different sequence compositions, inline and binding assertions, advanced SVA Features and assertion Coverage

COLLEGE SKILLS

Tools used in Engineering
MATLAB - Digital Signal Processing
Keil MDK or Arduino IDE - Microcontroller Programming
MASM or TASM - Assembly Language Programming (8085 or 8086) etc
NS2 - Network Simulator for Wireless communication.
Cadence Virtuoso - Custom IC design and package/PCB design/analysis

Subject Expertise
Digital electronics, Analog electronic, Network analysis, Analog & Digital Communications,
Signals & System, Signal Processing, Microprocessors/ Microcontrollers, Computer Organization, Wireless communication

PERSONAL SKILLS

- Internship on Design and Verification using Verilog in Entuple Technologies Pvt. Ltd.
- Introduction to Psychology from Yale University – Online (Coursera)
- Introduction to IOT & Embedded systems from University of California, Irvine- online (Coursera)
- Volunteer Teacher at “Volunteer For Cause”
- Languages Known: English, Kannada, Hindi, Konkani, French(Beginner)

PROJECTS

- RISC-V Design: The RV32I Processor is designed to support all RV32I Base Integer Instructions (Total -39). It’s a three stage pipelined processor which executes 32 bit instructions in program order.

Pipelined Stage I - The instructions are fetched from memory.

Pipelined Stage II - The instructions are decoded and the control signals for all units are generated. Branches, jumps and stores are executed in advance in this stage

Pipelined Stage III - Executes complete instruction and writes back the results in the register file

RESPONSIBILITIES:

Developed RTL codes for all modules of RISC V processor.

Verified individual modules with Linear TB code

The top module is synthesised and simulated

- Router 1x3 – RTL design and Verification

HDL: Verilog
HVL: SystemVerilog
TB Methodology: UVM
EDA Tools: Questasim and ISE

DESCRIPTION: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

RESPONSIBILITIES:

Architected the block level structure for the design

Implemented RTL using Verilog HDL.

Architected the class based verification environment using SystemVerilog

Verified the RTL model using SystemVerilog.

Generated functional and code coverage for the RTL verification sign-off

Synthesized the design.

- Design and verification of health monitoring system using CMOS 45nm technology

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DECLARATION

I hereby declare that all the information provided above are true to the best of my knowledge

Date: 11 April 2023
Place: Bangalore

YASHASVI SURYAVAMSHI