PARTH DANGI

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Physical Design Engineer having entry-level experience and looking forward to building a career in the domain by working in an organization. where my ability and skills will be utilized effectively for the betterment of myself and the Organization.

CORE COMPETENCIES

- Trained in Physical Design. Versed in ASIC Flow and Physical Design Flow.
- Implemented Projects based on 40nm and 28nm technology nodes.
- Trained in Floorplans, Powerplan, Placement, Clock Tree Synthesis, and Routing.
- Good knowledge and understanding of STA concepts: Fixing setup and hold violations, understanding of timing reports, CRPR, the effect of skew on timing, OCV, and latch concepts.
- Hands-on experience with VLSI tools: ICC2 Compiler, PrimeTime, Design Compiler.
- Good Understanding of Digital Logic Design, CMOS fundamentals, Hardware Design, and Microcontrollers.
- Basic Understanding of Physical Verification, DRCs, LVS .
- Good knowledge on Unix/Linux – Perl/TCL fundamentals/scripting.

TECHNICAL SKILLS

- ASIC: ASIC Flow | Physical Design Flow | Analog Design Flow
- Physical Design: Logic Synthesis | Floorplan | PowerPlan | PnR | Physical Verification
- EDA Tools: Design Compiler | IC Compiler | PrimeTime
- Scripting: Linux/UNIX | Perl | TCL
- Logic Design | Circuit Design| Hardware Design

WORK EXPERIENCE

ASSOCIATE ENGINEER A2 | SeviTech Systems, Bangalore (05/2022) – Present

- Worked with the team and implemented Physical Design flow on 2 Blocks
- Continually update manager and seniors with learnings and presentations.

Advance Diploma in ASIC Design |RV-VLSI Design Centre, Bangalore (12/2021) – (06/2022)

- Learned and Implemented Physical Design Flow on ASIC Block with 40nm technology node.

EDUCATION

B.TECH [Electronics and Communication] | Marwadi University, Rajkot (2018 –2022)

- Graduated with CGPA - 8.35
- Coordinator and Member of Aeromodelling Club, MU

DOMAIN SPECIFIC PROJECTS

1. Project Name: Block Level Design and Implementation of JBI subsystem
Tools used: Synopsys Design Compiler, IC Compiler II, StarRC, PrimeTime
Project Description: 28nm technology | Clock Frequency – 555.5 MHz | Voltage - 1.16 | Macro Count - 46 | Standard Cell Count - 43k+ | Shape - Square.

Challenges:

- Worked on Synthesis for the RTL code and generated SDC and Optimized Gate Level Netlist.
- Analysed Design Constraints and create floorplan of block using macro placement guidelines
- and worked for achieve higher core utilization ratio.
- Build a power plan to ensure about PG connectivity of macros and standard cells with meeting IR Drop and EM requirements.
- Performed timing driven and congestion driven placement to achieve design with optimized area usage and congestion.

2. Project Name : Block Level Design and Implementation of Falcon sub system
Tools used : Synopsys IC Compiler II, StarRC, PrimeTime
Project Description: 28nm technology | Clock Frequency - 500 MHz | Voltage - 1.16 | Macro Count - 16 | Standard Cell Count - 43k+ | Shape - Square.

Challenges:

- Analyzed Design Constraints and create floorplan of block using macro placement guidelines.
- Build a power plan by consume minimal routing resources, ensure that resolve all PG DRC.
- Performed timing driven and congestion driven placement to achieve design with optimized area usage and congestion.
- Doing CTS and analyzed the critical paths and fixing logical errors.
- Post CTS routability checks & fixing DRC & LVS issues and performed parasitic extraction on routed design.
- Run ECO flows to minimize DRV and timing violations and performed sign-off checks.

3. Project Name: ASIC Block Level Design and Implementation of Lakshya Block
Tools used: Synopsys ICC2, PrimeTime
Project Description: 40nm technology | Clock Frequency - 833 MHz | Shape - Rectilinear | Macro Count - 34 | Standard Cell Count - 38k+ | Area - 4.2 sq.mm | Supply Voltage - 1.1V | Power Budget - 600mWatts | IR Drop Budget - 55mV | Metal Layers - 7.

Challenges:

- Analyzed Design Constraints and create efficient floorplan. Place all groups of hard macros together using Data flow diagram and flylines for contiguous area for standard cells.
- Build a power plan to meet IR Drop goal and consume minimal routing resources, ensure that resolve all DRCs, Missing Vias, Floating Wires, Metal Spacings.
- Fixing congestion with performing experiments and tactics with Floorplan, providing channel, outing blockage where needed. Ensure Proper Insertion of Physical only cells.
- Performed timing driven placement to meet the goals of Setup & Hold timing with Zero LVS & DRC violations. Allow specific buffers & inverters for optimizing Data paths.
- Analyzed reports of Pre & Post Clock reports. Understand Classic CTS flow and CCD flow, Min/Max latencies and fixing timing violations, allow special cells to minimize skew.
- Understanding NDR rules for Clock nets, signal integrity, cross talk effects & antenna effects, analyzing timing reports after CTS with propagated clock, fixing setup & hold slack.
- Post CTS routability checks & fixing DRC violations for short, open nets, different net spacing, analyzing setup & hold violations, clock tree, latency & skew.
- Understanding routing flow & antenna effect. Fixing antenna violations by inserting antenna diodes and other DRC and LVS errors.

ACCOMPLISHMENTS

- Won 1st Price in “I’M 3D” ASIA Pacific 2020 for designing and manoeuvring a robust Drone.
- Qualified (Level-1) National Level Competition “Flipkart GRID 3.0” for Design Robots for Warehouse Applications.

INTERESTS

Aeromodelling | Pencil Sketches | Tech Gadgets