SiliConChip Technologies

Physical Design Course Details

What is VLSI?

Very Large-Scale Integration (VLSI) is a Solid Career Choice and offers Job opportunities for Electronics background graduates pursuing core employment. In India and overseas, VLSI provides a variety of job roles featuring outstanding professional growth and salary incentives. It is all about the design of integrated circuits which is usually referred to as a chip design. For those who are interested in pursuing a career in VLSI semiconductor sector and keep wondering if VLSI is a good career, let's take a closer look at the occupation and growth prospects available.

Career and Industry Scope of VLSI

There is lot of opportunities after completion of VLSI Program. Some of the job opportunities in this domain are RTL Design Engineer, Design Verification Engineer, Application Engineer, CAD Engineer, etc. With VLSI training, learners can give their career a new growth.

How does VLSI work?

Very large-scale integration is the process of making a microcircuit by combining many MOS transistors onto one chip. It is a microcircuit chips widely adopted, enabling complex semiconductor and telecommunication technologies to be developed.

What is Physical Design?

- Physical design is the process of turning a design into manufacturable geometries. It comprises a number of steps, including Floor planning, Placement, Clock tree synthesis, and Routing.
- Physical design begins with a netlist, which is synthesized from RTL. The netlist describes the components of a circuit and how they connect.
- Floor planning is the first major step. It involves identifying which structures should be placed near others, taking into account area restrictions, speed, and the various constraints required by components.

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Key Features:

- The Physical Design Course comprehensively covers Synthesis, Logical Equivalence Check (LEC), Physical Design Flow including Floor plan, Power plan, Clock Tree Synthesis, Routing, Static Timing Analysis, Physical Verification.
- Four Projects will be covered during the course using 45nm library. Labs are on Industry standard tool Synopsys DC Compiler, ICC2, Prime Time.

Course Delivery Model:

- Live Offline Class
- Each topic is followed by hands-on lab sessions with VLSI tools (Synopsys Tools).
- Soft Skill training.
- Mentoring sessions from Industry Experts
- Weekly mock interviews once eligible.

VLSI Tools and Lab

- **Synopsys Tools:**
    - Digital Design with Verilog: VCS.
    - Synthesis – Design Compiler Topographical
    - Static Timing Analysis (STA): Prime Time SI.
    - Physical Design: IC Compiler 2 (ICC2)
    - RC Extraction: Star RC
    - Physical Verification: IC Validator
    - Technology Libraries to Be Used: 45nm Libraries

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Eligibility for Attending this Internship/Training

- Internship applications are open for undergraduates (6th/7th/8th Semester), graduates, and postgraduates of the below-mentioned streams. BE/BTech in EEE/ECE/TE/CSE/IT/Instrumentation ME/MTech/MS in Electronics/MSc Electronics.
- Post – Graduate Freshers (MTech) with Specialization like VLSI/ Embedded/ Power Electronics/ Digital Communications/ Instrumentation etc.

Curriculum

- **Module 1: Essential of Linux**
  - Introduction to Linux
  - Command Line Operators
  - File Operations
  - Text Editors
  - Text Manipulation
  - Network Operations
  - Special Keystrokes
  - Assessment And Quizzes

- **Module 2: Digital Design**
  - Number System, Boolean Algebra, SOP and POS, K-Map
  - Combinational Circuit
  - Sequential Circuits
  - Finite State machines
  - Frequency Division
  - Setup and Hold time checks
  - Advance Design Issues: Metastability, Noise Margins, Power, Fan-out
  - Timing Consideration

- **Module 3: CMOS Devices and Technology**
  - Electronic Devices, Power Sources, Thevenin and Norton Theorem
  - Semiconductors Device Physics: Atomic Structure, Electronic
  - Configuration, Doping, Diode – Biasing and VI Characteristics
  - MOSFET: Region of operation, VL Characteristics
  - Function implementation using CMOS
  - Stick Diagram and Layout
  - Second order effect: Body Effect, Channel length modulation, Punch through, sub threshold conduction, DIBL
  - Process Technology: Clean Room, Wafer manufacturing, Oxidation, Diffusion, Ion implementation, Lithography.

- **Module 4: Verilog HDL**
  - Introduction of Verilog
  - Applications of Verilog HDL
  - Verilog HDL language Concepts
  - Data Types, Nets and registers, Arrays
  - Verilog Operators: Logical operators, Bitwise and Reduction operators, concatenation and conditional operators, Relational and arithmetic, Shift and Equity operators.
  - Types of Assignments: Continuous assignments, Inter/Intra assignments, Blocking and Non- blocking assignments, Execution branching, Task and Function
  - Finite State Machine (FSM): Basic FSM Structure, Moore Vs Mealy, Common FSM Coding styles, Registered outputs

- **Module 5: Synthesis**
  - ASIC Design flow and role of Synthesis
  - Synthesis flow
  - Writing timing constraints in SDC format
  - Constraining the design for timing
  - Power, area goals, set optimization techniques
  - Synthesize the design
  - Generate the analyse the reports, save the netlist and SDC

- **Module 6: Logic Equivalence Checking (LEC)**
  - Formal Verification
  - Understanding & Matching compare points
  - Debugging non-equivalent points

- **Module 7: TCL Scripting**
  - Features of TCL and Applications. TCL commands, Variable, arithmetic expressions, comments, identifiers, reserved wors, data type, decision, loops, arrays, strings, file, I/O and Procedures.

- **Module 8: Introduction of Physical Design, Data presentation and Sanity Check**
  - Introduction to Physical designed Physical Design Flow, Data Preparation: File required for PD (Netlist, SDC, Libraries, Technology files, TLU+)

- **Module 9: Floorplan**
  - Goals of floor planning, different aspects of floor planning, Rectangle /Rectilinear floor plans, Die Size estimation (Core Utilization, Aspect ratio), IO Placements, macro placement and guidelines.

- **Module 10: Power Routing**
  - Goals of power Routing, Power distribution structure (Ring, straps and follow-pin/std cell rail), Metal stack information, power planning methodology, IR drop analysis, types of power consumption

- **Module 11: Placement**
  - Goals of placement, types of placements, pre-place (End-cap, Tap & I/O buffer) cells, Placements optimization, congestion analysis, timing analysis, Tie-cells
  - High-Fan-out net synthesis, Scan chain re-order, path grouping and creating Bounds

- **Module 12: Timing Analysis (Pre-Layout) & Optimization**
  - STA overview and concepts, basic timing checks (setup, hold), Understanding timing constraint (SDC), timing corner, timing reports analysis
  - General optimization techniques, typical cause of timing violations and strategies for fixing the same, pre-CTS optimization to Fix Setup Violations

- **Module 13: Clock Tree Synthesis (CTS)**
  - Goals of CTS, Types of clock-tree, constraints for CTS, building clock tree, Analyse the result
  - Post-CTS optimization: Fixing setup and Hold Violations.

- **Module 14: Routing**
  - Goals of Routing, stage of routing: Global Routing, Track assignment and Detail Routing, Routing options, Fixing of routing violations (DRC, LVS), post route optimization, issues in routing and guidelines for optimum routing results.

- **Module 15: Post Layout STA**
  - Post Layout STA using SPEF, Multi moose multi corner STA, Derating factors, PVT, OCV variations

- **Module 16: ECO Flow:**
  - What is ECO, Types of ECO, Timing and Functional ECO, Performing the ECO placement and routing

- **Module 17: Sign-off Checks**
  - Physical Verification (DRC, LVS), IR drop analysis, Electro-Migration Analysis

Projects:

- Project will be given converging Netlist to GDS II flow. Various projects that will allow the students to understand the intricacies of implementation foe the minimum area, low power, high performance.
- The method of execution will be similar to typical block level physical design work/projects in the industry
- Block level input database will be given and the participants have to deliver GDS II, after clearing all the issues during sign-off checks.