Vijaya Kumar Muliki

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Career Objective

Seeking a position to work with a highly esteemed company which gives me a platform to use my skills for mutual growth and benefit of company and myself.

Core Competancy

- Hands on experience on IC COMPILER II TOOL.
- Very Good experience in physical Design Project involving FLOORPLAN, POWERPLANNING, PLACEMENT, CLOCK TREE SYNTHESIS and ROUTING.
- Good understanding of clock Abnormalities such as CLOCK JITTER, CLOCK LATENCY, CLOCK SKEW and understanding SIGNAL INTEGRITY and CROSS TALK.
- Good Understanding of STA concepts such as SETUP, HOLD VIOLATIONS, TIMING PATHS and DELAYS.
- Good knowledge on ASIC FLOW (Chip Specification, Design Functional Verification, RTL block level synthesis , Chip Partitioning, DFT,FLOORPLANNING, PLACEMENT, CTS).
- Worked on the SUPERPARTITION BLOCK with RECTILINEAR SHAPE and performed multiple floorplans to suit with the changes in shape and pin locations.
- Hands on experience on PRIMETIME for STATIC TIMING ANALYSIS and timing closure at block level by analyzing the TIMING REPORTS at multiple scenarios.
- Good knowledge on fundamentals in LOGIC DESIGN and Basics of MOSFET theory.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Krishna University College of Engineering and Technology , with 7.49 CGPA

2015

Andhra Polytechnic, with 63.85 %

SSLC **2012**

ZP High school , with 78 %

Domain Specific Project

RV-VLSI Institute

Graduate Trainee Engineer Nov-2022 to Dec-2022

FLOOR PLANNING AND PLACEMENT OPTIMIZATION

Description

Floorplanning is an essential design step, as it determines the size, shape and locations of modules in a chip and it estimates the total chip area, the interconnects and delay. Place_optimization meets timing,area and power specifications.

Tools

IC Complier II

Challenges

- Macro placement is a challenge for System on Chip with large number of cores and Memories.
- Accurate estimations of Timing, Power and Area.
- Timing and Congestion issues.

RV-VLSI Institute

Graduate Trainee Engineer Dec-2022 to Jan-2023

CLOCK TREE SYNTHESIS AND ROUTING

Description

CTS is a technique for distributing the clock equally among all sequential parts of VLSI design& balancing the clock delay to all clock inputs by inserting buffers/inverters. Routing Making physical connections between signal pins using metal layers.

Tools

IC Complier II

Challenges

- Automatic clock tree synthesis engine puts a lot of buffers across the chip that are not desired.
- Building clock tree separately with desired latency. This technique enabled meeting timing requirements for the mixed signal chip
- Macro Modeling Technique is to add insertion delay to the clock pins of specific registers in order to meet reg2reg timing paths.

B.E / B.Tech Academic Project

Krishna University College of Engineering and Technology

REMOTELY CONTROLLED ARMED SURVEILLANCE ROVER WITH WEAPON

Description

This remotely operated ground vehicle was designed and developed for use in COUNTER TERRORISM operations by the Indian army in difficult TERRAIN and SUSPICIOUS PLACES.

Tools

Embedded C software used in Arduino IDE And Bluetooth HC-05 Module.

Challenges

- 1.To drive the vehicle on difficult terrains. 2.Simultaneous use of vehicle and weapon. 3.Aligning the camera and the weapon in the same direction.