# **SNEHA G K**

Female/22/ English, Kannada, Hindi A Passionate Programmer and a VLSI Scholar Gejjagadahalli, Shivanapura post, Dasanapura Hobli, Bengaluru North Taluk 562123

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## **EDUCATION**

#### DR. AMBEDKAR INSTITUTE OF TECHNOLOGY

2019-2023, 8.8 CGPA

Bachelor of Engineering in Electronics and Communications

#### EXCELLENT SCIENCE AND COMMERCE PU COLLAGE

2017-2019, 93%

Science Domain-Physics, Chemistry, Mathematics, Computer Science

#### SREE BASAVESHWARA ENGLISH HIGH SCHOOL

97%

### SCHOLARSHIP

#### **KATALYST INDIA-** WINDS OF CHANGE

2019-2023

Women Empowerment Non-Profit NGO, selects the top talent and trains them with 600 proprietary and scientifically researched curriculum to groom the candidate for real world success.

CROSSROAD EMERGING LEADERSHIP PROGRAM: Semifinalist, selected from a pool of thousands of students across 135 countries.

CROSSROAD EMERGING LEADERSHIP PROGRAM, a Harvard Program is a prestigious and a fully funded career development opportunity for students from across the world, who are the first member of their family—or the first generation within their family—to attend university and facing challenges of financial and social circumstances. Following a rigorous multi-stage evaluation process, exceptional students are selected from a diverse applicant pool to take part in this unique educational experience

## **EXPERIENCE & PROJECTS**

### **Synopsys Technical Engineer Intern**

August 2022 – present

Revising and debugging the existing Backend design (Place and route) for customer projects Successfully reduced Global Skew from 360ns to 150ns by debugging the existing design, the missing CTS library cell. Also worked to improve PPA of A53 design (Timing, Area, Power and DRC).

## **MATLAB Developer Intern**

Oct 2021- Apr 2022

Developed MATLAB Code for more than 4 projects and also written Blog on each MATLAB Code.

### **Design a 16 Bit RISC Processor**

I have developed Verilog code based on the Harvard Architecture which supports 15 different Instructions. Synthesis of the Verilog code has been done in Xilinx Vivado. Physical Implementation of a design from RTL to Routing in Fusion Compiler with zero TNS and DRC.

## **Autonomous Self-Driving car**

In a team of three, I had taken up the leadership role leading the team though planning and execution of the project while I also significantly contributed to debugging, organizing parts, reporting and presentation.

### SKILL SETS

- ✓ Cadence Virtuoso
- ✓ PPA Push
- ✓ Synthesis
- ✓ Placement and Routing
- ✓ CTS
- ✓ Fusion Compiler
- ✓ Linux/ Unix Basics
- ✓ TCL Scripting

- ✓ C programming
- ✓ MATLAB
- ✓ Verilog
- ✓ Basic Python
- ✓ Microsoft word, PPT
- ✓ Public Speaking
- ✓ Team Player

## **CERTIFICATES**

- > C Programming by G-Tech Computer Education.
- > Career edge-Knockdown the lockdown by TCS.
- > The Fundamental of Digital Marketing by Google.
- > Probability and Statistics by HarvardVX.
- ➤ Basics of Machine Learning by Andrew.G in coursera (taken free course but not certified)

## **ACHIEVEMENTS**

- 1. **Gold Medalist:** Rewarded for academic excellence in 10<sup>th</sup> grade amongst 100 students.
- 2. **National Science Day Competition:** 3rd prize for Power Point Presentation on Big Bang Theory
- 3. **Morgan Stanley Competitive Assignment**: Claimed 1<sup>st</sup> position in 2 rounds out of 3, solved 16 programming problems efficiently