Bharath Reddy Palle
reddybharath1090@gmail.com, 7731891090
Hyderabad-508126, Telangana

Career Objective

Seeking a challenging and responsible position as a Physical Design Engineer with an opportunity for advancement.

Core Competancy

- Comprehensive knowledge and proficient in ASIC PD Flow involving Floor planning, Power planning, Automatic P&R, Clock Tree Synthesis & Routing.
- Better understanding and hands-on experience in STA, CRPR, Interpreting timing reports, fixing hold, and setup violations.
- Worked on a project with incorporates a 40nm Technology node with 7 Metal layers, 34 Macros, at 833 MHz frequency, 1.1 volts & power budget of 600 mW.
- Worked on Floorplan for high utilization ratio and good contiguous core area, designed good power mesh to connect all macros and std-cells without any floating pins.
- Worked on placement with power aware and acceptable congestion ensuring good routability.
- Familiar with TCL scripting and Perl scripting languages.
- Analyzed and understood Design Constraints to specify PVT Corners, False paths, Half cycle, Multi-Cycle paths, Asynchronous Clocks, and CRPR.
- Hands-on experience on Synopsys ICC2 and Prime Time.
- Good Knowledge of Logic Design Concepts, CMOS, MOSFET, Semiconductor Theory, and Basic Electronic Devices.
- Understood the Routing Flow and Fixed the DRC, LVS, and Antenna Violations.

Education Details

Advanced Diploma in ASIC Design **2022**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2020**
Anurag Group of Institutions, with 7.23 CGPA

2016
Narayana Junior College, with 94 %

SSLC **2014**
Vidya Kiran High School, with 90 %

Projects worked on

ACD Communications Pvt Ltd Client: IAF, Tata Nova

Engineer Mar-2021 to Feb-2022

MRSAM

Description

Participated in the manufacturing of low-power switches, high-power switches, control cards, couplers, and power supplies. Connectivity check of LPS and HPS. To maintain the Current and Voltage in the different Temperatures as per the requirements.

Tools

Regulator Power Supply, Amplifier, Signal Generator, Test Jig and RF Cables.

Challenges

- Working knowledge on RF testing equipment i.e. Signal Generators, Signal Analyzer, Oscilloscope, Network Analyzer, Power Supply, Amplifier
- Testing of LPS, HPS, ASU, and GSA.
- By consistently putting long hours for contributing work and performance to meet objectives and achieve team success
- I was involved in the Manufacturing of Ground System Antennas

---

Domain Specific Project

RV-VLSI Design Center

Graduate Trainee Engineer Jun-2022 to Sep-2022

Analysis of Timing Reports (STA)

Description

For Flip flops and latch based timing paths working at different operating conditions, Timing reports are analyzed considering OCV, AOCV, uncertainty, CRPR. Clock Skews and certain exceptions (Multi cycle, False paths) honoring the constraints file.

Tools

Synopsys PrimeTime, Synopsys ICC2.

Challenges

- Analyzed all the timing paths in different path groups at every stage of flow (floorplan, placement & CTS).
- Differentiating some violations which are based on timing exceptions such as false paths and multi-cycle paths and reporting about the same to change in the constraint file.
- Understood the effects of CRPR, OCV, AOCV and skew factors in timing analysis.

RV-VLSI Design Center

Graduate Trainee Engineer Jul-2022 to Aug-2022

Floorplan, Powerplan, and Placement implementation

Description

Worked on Floor plans for high utilization ratio and good contiguous core area, designed good power mesh to connect all macros without any floating pins. Worked on placement with power aware and acceptable congestion ensuring good routability.

Tools

Synopsys ICC2

Challenges

- Placing macros near to Die area with proper spacing during the Floorplan to improve congestion in further steps.
- Power Planning by providing Power connections to all the metal layers maintaining IR drop.
- Adding standard cells and physical only cells such that to have no DRC's and Congestion.

RV-VLSI Design Center

Graduate Trainee Engineer Aug-2022 to Sep-2022

CTS and Routing for Block level implementation

Description

Clock tree synthesis (CTS) is the automatic insertion of buffers/inverters along the clock paths of the ASIC design to balance the clock delay to all clock inputs. In the Routing stage, the tool routes all the signal nets with minimal physical DRCs.

Tools

Synopsys ICC2

Challenges

- Clock routes were created with the spacings according to the NDR.
- Generated Clock tree synthesis and worked on Classic and CCD flow and compared timing reports of both for better results.
- Rerouted the metals to solve the shorts and different net spacing errors.
- Understood the Routing Flow and Fixed the DRC,LVS and Antenna Violations. Cleared antenna violations by using Diode insertion method and Metal jumper method.

B.E / B.Tech Academic Project

Anurag Group of Institutions

Exclusive Furnace for Waste yard with Data Transmitter

Description

In this project we designed a special type of furnace to burn the waste in waste yard. In addition to the burning of waste, it also generates electric energy.The furnace is constructed with special mechanism which is aimed to generate Electric energy

Tools

Software: Arduino IDE, Thing Speak application. Hardware: Arduino UNO, WiFi Module ESP8266, LM35 (Temperature Sensor), Thermo Electric Generator, Heat Sink, Furnace with Mild Steel Sheets(3-side close & 1- side open).

Challenges

- Maintaining the temperature of the furnace when the waste burns. Generating power for maximum level using TEG. Converting output of sensors into digital for managing. Sending data to the concerned authority to maintain proper waste management.