Dr. Khadar Basha N

Physical Design Engineer

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SUMMARY

- 2+ Years of experience in VLSI Physical Design in latest technologies of 7nm, 10nm and 28nm with multi-million gate design tape outs.
- Strong fundamentals in physical design execution through handling diverse blocks in multiple projects (7nm-28nm). Expertise includes floor planning, PnR, CTS, RC-extraction, timing closure, physical and electrical verification.
- Hands on experience in Physical Design flow from Netlist to GDSII
- Familiarity with Unix, C, python and TCL script.
- Ability to work both independently and as part of a team.

SKILLS

Technical Skills	Physical Design | Static Timing Analysis
Programming Language	C | TCL | Python
Tools	IC CompilerII (ICC2) | PrimeTime (PT) | StarRC

WORK HISTORY

Physical Design Engineer **Spectrum digital, Hyderabad** **Feb 2021 - Present**

Project 1:

Client – Renesas - Network submodule (02/2023 to Still going on)

Block Details:

- Technology / Layers : 7nm/15M
- Block Name : Mem_cal_par
- Instance Count : 1.1M
- Macro Count : 84
- No. of Clocks : 17
- Clock Frequency : 2.6GHz
- Tools used : Fusion Compiler

Project 2:

Client – Renesas (05/2022 to 12/2022)

Block details:

- Technology / Layers : 10nm/12M
- Block Name : Vchinf_mcright
- Instance Count : 800K
- Macro Count : 24

- No. of Clocks : 12
- Clock Frequency : 2.05GHz
- Power Domain : Multi-VDD(2)
- Tools used : ICCII, Primetime

Task Handled in Design:

- Handled block implementation from floorplan to GDSII using a timing closure flow.
- Basically, this block is timing critical, achieving timing with different scenarios.
- Fixed DRCs, LVS and Electro Migration checks.

Project 3:

Client – Renesas (06/2021 to 02/2022)

Block details:

- Technology / Layers : 28nm/10M
- Block Name : Mdf_rcinf3
- Instance Count : 200K
- Macro Count : 18
- No. of Clocks : 6
- Clock Frequency : 930KHz
- Tools used : ICCII Compiler, PrimeTime and StarRC

Task Handled in Design:

- Handled block implementation from floorplan to GDSII.
- After multiple PnR trails with different congestion and timing options achieved best QoR.
- Performed Block level STA and resolved timing issues.

EDUCATION

Physical Design training	**VLSIGURU**	**Jul 2020 - Dec 2020**
PhD: Electronics	**Sri Venkateswara University**	**Jun 2014 - Oct 2019**
M.Tech: VLSI System Design	**JNTU Anantapur**	**Nov 2010 - Mar 2013**
B.Tech: ECE	**JNTU Hyderabad**	**Sep 2004 - May 2008**
Intermediate: MPC	**APR Junior College Gyarampalle**	**Aug 2002 - Apr 2004**
SSC: General	**APR School Srisailam**	**Jun 2001 - Apr 2002**

LANGUAGES

Telugu | English | Hindi

DECLARATION

I hereby declare that the statements made in this resume are true, complete and correct to the best of my knowledge and belief.

Place: Hyderabad.
Date:

Dr. Khadar Basha N.