BANDA SHIVA KUMAR

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Career Objective

To secure a challenging position in a reputed organization to utilize my knowledge, skills and abilities in the field of Physical Design and to be a part of a team that dynamically works towards the growth of the organization.

Core Competancy

- Experience in entire APR from floorplan, Placement, post placement timing closure, clock tree synthesis, Routing, Post route timing fixing and DRC fixing.
- Experience of working in APR of 40nm technology.
- Efficient in creating Power Mesh with strict IR drop and Power Budget.
- Hands-on experience on Synopsys IC Compiler2 and PrimeTime for STA.
- Routability analysis & post-route optimization and addressing routing DRC, Post-route timing closure. Fixed the DRC, LVS and Antenna Violations.
- Familiar with TCL scripting and Perl scripting languages, modified and extracted information from timing paths, finding WNS and TNS.
- Good Knowledge in Logic Design Concepts, CMOS, MOSFET, Semiconductor Theory and Basic Electronic Devices, Linux and Unix.
- Good knowledge of TCL, shell and PERL scripting.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2021**

CVSR college of Engineering and Technology, with 6.9 CGPA

2018

TKR college of Engineering and Technology, with 72.5 %

SSLC **2015**

Bhashyam High School, with 75 %

Domain Specific Project

RV -SKILLS CENTER FOR EMERGING TECHNOLOGIES

Graduate Trainee Engineer May-2022 to Jun-2022

Static Timing Analysis

Description

Acquired in-depth knowledge and proficient in STA involving Timing Reports. Analyzed and fixed the setup and hold violations by referring to Timing library and Timing Constraints.

Tools

Synopsis IC Compiler 2, Synopsys PrimeTime.

Challenges

- Analyzed all timing paths in different path groups at every stage of APR flow and observed how to fix those timing violations.
- Understood the effect of skew factors in Timing analysis. analyzed the timing reports of WNS, TNS, Min/Max timing reports and Latencies.
- Comparing the reports of single path group in each and every stage of APR flow- floorplan. Placement, Clock-tree synthesis and Routing.

RV -SKILLS CENTER FOR EMERGING TECHNOLOGIES

Graduate Trainee Engineer Jul-2022 to Aug-2022

Design of Floorplan, Powerplan & Placement

Description

Technology: 40nm, Clock Frequency is 833 MHz, Supply Voltage- 1.1V, Power Budget- 600mW, Max. IR drop (VDD+VSS) is 5.00%, Area 4.2 sq.mm, Macros- 34, standard cells- 38k, Shape: Rectilinear, Metal layers-7, Tap cells- 4k.

Tools

Synopsis IC Compiler 2

Challenges

- Understood the Design constraints & designed the floorplan as per Data Flow Diagram. placed the macros according to the guidelines to have contiguous core area for standard cells.
- Building a good Power plan to meet the IR drop specified and ensuring that no connectivity, missing vias issues in the design & no PG DRC errors after the building the power Mesh.
- Observed how the placement will be driven by different criteria like Timing driven, congestion driven & power optimization.
- Resolving the congestion by providing proper spacing between macros by formula method with multiple iterations and placement blockages.

RV -SKILLS CENTER FOR EMERGING TECHNOLOGIES

Graduate Trainee Engineer Aug-2022 to Sep-2022

Implementation of Clock Tree Synthesis & Routing

Description

Minimizing the congestion hotspots & reduction in cross-talk noise. Most of the IC's clock consumes 30- 40 % of total power. efficient clock architecture, clock gating helps to reduce power. clock buffers produces equal Rise & Fall time.

Tools

Synopsis IC Compiler 2

Challenges

- Identified and rectified the zroutes errors such as shorts, different var rule net spacing, spacing issues.
- Understood the effect of skew factors in Timing analysis.
- Resolving the antenna violations by using diode insertion and jumper insertion methods and fixed the DRC's and LVS.

B.E / B.Tech Academic Project

CVSR college of Engineering and Technology

Development of IOT enabled water quality monitoring for Aquaculture

Description

India's aquaculture industry has been growing at 7% per year. which results in a decline in aquaculture water quality & increase in the incidence of aquatic animal diseases. Using IoT, we can track the physio-chemical factors in pond water .

Tools

Software: Arduino programming and Image processing. Hardware: Arduino, Temperature Sensor, pH Sensor, Webcam and Stepper motor.

Challenges

- To alert farmers over abnormality in water quality parameters. To analyze water quality parameters over a period. To take subsequent actions to neutralize water parameters. maintaining water quality is essential.