DONE M.TECH IN VLSI AND HAVE EXPERIENCE OF 1 YEAR IN DESIGN VERIFICATION.

Jameel ahmed kustagi
jameelahmed5963@gmail.com
9663581514

SUMMARY

I have completedcompleted M.tech in vlsi and work for 1 year as a Asic design verification trainee.

CAREER OBJECTIVE

Looking for opportunities to incorporate my skills and training to help the company grow.
Specially in design verification.

SKILLS

Basics PHYTON	
CADENCE TOOL	Front end and back end design
QURTUS	Modelsim

EXPERIENCE

Feb-2022 - Apr-2023	**Sure trust group**
Vlsi course	Learn Verilog basic and testbench.
May-2022 - Mar-2023	**Radiant Semiconductors Bangalore**
Design verification engineer trainee	Verilog,SystemVerilog,UVM,Testbench, DDR protocol.

PROJECTS

Project Name: Design sequential circuit using Quantum dot cellular automation

Role: Design **Team Size:** 1 **Project Duration:** 3 Month

Project Detail Design of sequential circuit using QCA Design. Which is more effecient and less power consumption.

EDUCATION

Degree/Course	Institute/College	University/Board	Percentage/CGPA	Year of Passing
10	ACO SCHOOL ILKAL	KARNATAKA SECONDARY BOARD	84 %	2014
Puc	S.V.M COLLEGE ILKAL	Department of Pre-University karnataka	60 %	2016
B.E in Electrical and Electronic	SECAB INSTITUTE OF ENGINEERING AND TECHNOLOGY BIJAPUR	V.T.U BELGAUM	7.6	2020
M.Tech In VLSI AND EMBEDDED SYSTEMS	DAYANANDA SAGAR COLLEGE OF ENGINEERING BANG ALORE-560078	V.T.U BELGAUM	8.1	2022

STRENGTHS

Can learn and understand new thing.

AREAS OF INTERESTS

Vlsi, Asic design verification

HOBBIES

Reading and learning.

VLSI SURE TRUST GROUP

Vlsi course Taken vlsi training in which basics of verilog and testbench.

PERSONAL DETAILS

Address	Ward no.7 alampurpeth ilkal Ilkal, Bagalkot, Karnataka, 587125
Date of Birth	12-10-1997
Gender	Male
Nationality	Indian
Marital Status	Single
Languages Known	Kannada, Hindi, Urdu, English

DECLARATION

I hereby declare that all the above information is true to best of my knowledge

Jameel ahmed kustagi