Savirigana Mohini

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srikakulam-532213, Andra Pradesh

Career Objective

To be a part of an esteemed organization where I can rise to my highest potential by leveraging acquired knowledge along with utilizing my skills towards the growth of the organization.

Core Competancy

- Acquired in-depth knowledge in ASIC PD flow involving Floor planning, Power planning, IR Drop analysis, Automatic Place and Route, Clock tree synthesis and Routing.
- Good knowledge and hands-on experience in STA, CRPR, fix setup and hold violations.
- Analyzed and understood the design constraints to specify PVT corners, false paths, multi-cycle paths and CRPR.
- Worked on Floorplan and Power plan to meet specified IR drop and acceptable congestion.
- Hands-on experience in APR Tools-Synopsys ICC2 and STA Tools - PrimeTime.
- Understood and modified the TCL scripts, Hands-on experience with Linux commands.
- Generating and analyzing timing reports.
- Good knowledge of logic design concepts in CMOS, MOSFET, Semiconductor theory and Electronics Devices.
- Understood the routing flow and fixed the DRC, LVS, and Antenna violations.
- Hands-on experience RTL Design and Testbench.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electrical and Electronics** **2020**

GMR Institute of Technology, Rajam, with 7.31 CGPA

2017

GOVERMENT POLYTECHNIC , Srikakulam, with 72.75 %

SSLC **2014**

A.P.S.W.R School, with 65 %

Domain Specific Project

RV-Skills

Graduate Trainee Engineer Jun-2022 to Jun-2022

Analysis of Timing Reports STA

Description

Static timing analysis is the complete and exhaustive verification of all timing checks of a design. Timing reports are analyzed considering setup and hold violations, uncertainty, OCV, CRPR, noise handling and timing exceptions.

Tools

Synopsys PrimeTime, Synopsys IC Compiler 2

Challenges

- Identify violations that are based on timing exceptions such as false paths and multi-cycle paths and report changes in the constraint file.
- Understand the effects of CRPR, OCV, AOCV and skew factors in timing analysis.
- Analyze timing violations at all stages and fixed setup and hold violations.

RV-Skills

Graduate Trainee Engineer Jul-2022 to Aug-2022

Floorplan, Power plan and Placement

Description

Overview: 40nm design with Clock Frequency-1 GHZ, Rectilinear Shape, Macro Count-34, Standard Cell Count-41 K, Area-4.3 sq. mm, Supply Voltage-1.1V, Power Budget-600mWatts, IR-Drop Budget-55mV, Metal Layers-7.

Tools

Synopsys IC Compiler2

Challenges

- Understand the design constraints and design the floorplan as per the Data Flow diagram. Identify the illegal placement of macros and standard cells and legalize them.
- To build a good power plan by changing the width, spacing, pitch and offset to meet the IR drop specified and ensuring that there are no PG DRC errors after building the power net.
- Provide some keep-out margins around the macros, placement blockage, and routing blockages to rectify DRC like shorts, overlaps and metal spacing.
- To control congestion and DFT-aware placement, worked on different floorplan experiments and implemented different strategies.

RV-Skills

Graduate Trainee Engineer Aug-2022 to Sep-2022

Clock tree synthesis and Routing

Description

Performed pre-routing checks and setup and distribute the clock nets and signal nets to all elements in the design.

Tools

Synopsys IC Compiler2

Challenges

- Observe whether the clock reaches all the clock pins of sequential elements or not If shorts occur on the clock net, re-route that specific net.
- understand tool behavior while clock tree synthesis to meet target skew, Min/Max latencies, fix timing violations and understanding DRC and LVS errors.
- understand tool behavior while routing to meet Min/Max latencies, fanout understanding signal integrity.

B.E / B.Tech Academic Project

GMR Institute of Technology, Rajam

Analysis of electric power system using power world simulator

Description

Calculate the Power Transfer Distribution Factor(PTDFs), Line Outage Distribution Factors(LODFs) and find the critical line in the event of a fault, determine Post contingency analysis.

Tools

power world simulator

Challenges

- To provide and prioritize the impacts on an electric power system whenever typically unplanned problems or outages occur. Regions can be defined by zones, super areas, single buses, injection groups or the system slack.