Venkatalakshmitanuja Yenumala

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Vijayawada-521185, Karnataka

Career Objective

I intend to be a part of an organization where I can make best use of my skills in Physical Design Domain with an opportunity for advancement.

Core Competancy

- Knowledge on implementation of ASIC flow (netlist to GDS II) at block level with critical power, area & timing budget by giving the importance of each block in the flow.
- Knowledge on Logic Design Concepts and CMOS Structure.
- Comprehensive knowledge & hands on experience in STA, CRPR, Interpreting timing reports, fixing setup & hold violations.
- Worked on Floorplans for high utilization ratio, designed power mesh to meet IR drop and checked for pg connectivity errors.
- Worked on placement with power aware & acceptable congestion ensuring good routability.
- Performed analysis of reports at various stages of design to understand the sanity checks, place optimization & CTS.
- Understood the Routing flow & fixed the DRC, LVS, Antenna violations & the concept behind timing report analysis.
- Hands on experience in APR Tools- Synopsys IC Compiler II & STA Tools - PrimeTime and OS- Linux and Windows.
- Worked on a project in 40nm technology to implement a block level PD to meet required IR drop, congestion free placement & CTS for targeted skew.
- Knowledge in Verilog and TCL Scripting.

Education Details

Advanced Diploma in ASIC Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electrical and Electronics** **2021**

Lakireddy Balireddy College of Engineering, with 8 CGPA

2018

Gandhiji Institute of Science and Technology, with 76.49 %

SSLC **2015**

ZPHS, Lingalapadu, with 77.9 %

Domain Specific Project

RV Skills

Graduate Trainee Engineer Jul-2022 to Aug-2022

Block Level Implementation of ASIC

Description

Floorplan, Powerplan and Placement for Block Level with the specifications- Design- 40nm, Layers- 7, Supply Voltage- 1.1V, Area- 4.2 sq. mm, Clock frequency 833MHz, Power Consumption- 600mW, Max IR Drop- 5%, Standard cell count- 38403, Macros- 34.

Tools

Synopsys IC Compiler II

Challenges

- Designing the Floorplan by understanding the design specifications such that to have a contagious core area for placing a standard cell.
- Building a good power plan to meet the IR drop ensuring that no floating pins & missing vias in the design & also taking care about power budgets.
- Placement and Optimization of Physical only cells to meet the DRC violations and Congestion check.
- Analyzed the timing reports and understood how the violations can be reduced or increased in different stages.

RV Skills

Graduate Trainee Engineer Aug-2022 to Sep-2022

CTS & Routing on Block level design

Description

Floorplan, Powerplan and Placement for Block Level with the specifications- Design- 40nm, Layers- 7, Supply Voltage- 1.1V, Area- 4.2 sq. mm, Clock frequency 833MHz, Power Consumption- 600mW, Max IR Drop- 5%, Standard cell count- 38403, Macros- 34.

Tools

Synopsys IC Compiler II

Challenges

- Clock routes are routed using NDR. In CTS flow Synthesis is performed using CCD and Classic flows and compared for better timing reports.
- Reported for Timing Violations for different Timing Paths.
- At Routing stage, Signal routing was created and checked to meet the DRC's and congestion. Completing the connections without increasing total area of the block.
- Fixing of antenna violations by using two methods i.e, metal jumper and diode insertion.

RV Skills

Graduate Trainee Engineer Jun-2022 to Jul-2022

Static Timing Analysis(STA) on Block level design

Description

Timing analysis done for various flipflops and latches for various paths. Analyzed the Timing reports based on various conditions such as timing exceptions(False paths, Multi- cycle path), OCV, CRPR and Clock skews.

Tools

Synopsys PrimeTime

Challenges

- Understanding the timing reports of Pre-Layout STA on Prime Time and have a knowledge on resolving the timing violations.
- Analyzed the timing reports at different stages of APR flow for different path groups.
- Fixing hold violation without causing a setup violation or vice versa. Understood the effects of CRPR, OCV, AOCV and skew factors in timing analysis.
- Understood the time borrowing concept of level sensitive elements.

B.E / B.Tech Academic Project

Lakireddy Balireddy College of Engineering

Development of Power Balancing System Using Hybrid Microgrid

Description

This project helps about how to balance the power by using renewable resources (ex: solar& wind) which are abundant in nature. Along with the Battery storage system.

Tools

MATLAB

Challenges

- Main challenges are faced about power balancing issues due to renewable resources which does not deliver continuous power .For that reason we used Battery Storage System which stores the power and delivers the power when it is needed.