SUMER SAINI

Delhi Technological University, Delhi

@ sumersaini030@gmail.com (+91) 8239411433 https://www.linkedin.com/in/sumer-391024139

OBJECTIVE

Aspire to be in a leading organization with a dynamic and amiable work environment that will provide opportunities for growth. Willing to contribute towards growth of organization by utilizing my ability to adapt to new skills and being a team player. Passionate about VLSI and continuously improving myself in all its forte.

INTERNSHIP

INTERNSHIP at INTEL

August 2022 – May 2023 INTEL

Verification using UVM.

- Debugged some of existing issues in testbench.
- Analyzed the functional coverage of DUT.
- Added some new test cases to check some functionalities which were not exercised in existing test cases.
- Did some changes in monitor ,driver,agent to remove dependency on arguments passed in command while running test case.

ACADEMIC PROJECTS

M.Tech Project

AXI PROTOCOL USING VERILOG | TOOLS- Xilinx VIVADO

- Design of AXI protocol using verilog in which read and write operations are performed. The AXI protocol defines the signals and timing of the point-to-point connections between manager and subordinates. The AXI protocol is a point-to-point specification, not a bus specification. Therefore, it describes only the signals and timing between interfaces.

EXTENDING 8-BIT BOOTH MULTIPLIER TO IMPLEMENT CUBE,SQUARE,FACTORIAL- Xilinx VIVADO

- Design and extension of Booth multiplier to implement cube ,square and factorial. Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation.

DESIGN AND VERIFICATION OF FIFO USING SYSTEM VERILOG–Xilinx VIVADO

- Design FIFO and verified functional correctness using SYSTEMVERILOG.

EDUCATION

Pursuing M.tech in VLSI AND EMBEDDED SYSTEMS

Delhi Technological University, Delhi

August 2021-23 SGPA 8.45

B.Tech in Electronics and Communication Engineering

Compucom Institute of Technology and Managment,Jaipur

August 2016-2020 CGPA 8

Class XII

Vidhyasthali public school

May 2015 79.40%

Class X

Vidhyasthali public school

May 2013 85.5%

SKILLS

C++ | UVM | System VERILOG | SVA | VERILOG | C | Linux | Verdi

COURSEWORK

- Digital Electronics
- CMOS Digital IC Design
- Low Power VLSI Technique
- Physical design Flow
- Static Timing Analysis
- Clock Tree Synthesis
- UVM testbench for newbie (Udemy certificate)

ACHIEVEMENTS

- Qualified GATE-2021.