# NIVEDITA

## CONTACT


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## STRENTHS

- Self motivated and ready to tackle any challenge
- Having good communication and writing skills.

## TECHNICAL SKILLS

- Digital electronics
- **HDL**:VERILOG
- **HVL**:System verilog, UVM
- **EDA TOOLS**: Xilinx ISE, Mentor graphics, modelsim, Quartus Prime.

## PROFILE

As a graduate, I am Seeking a challenging position with a fast growing company where I can contribute to the growth of the organization as well as my professional career and to work in a team of dedicated and committed individuals who respect the way other works and help them work to their best potential.

## EDUCATION

**M.tech in VLSI and Embedded system**
Sharnbasva University Gulbarga (2020-2022)
CGPA:9.93

**B.E in Electronics and Communication Engineering**
PDA College Of Engineering Gulbarga (2015-2020)
CGPA:6.99

**P.U.C**
Nisarga pu science college Gulbarga (2013-2015)
PERCENTAGE:85.16%

**S.S.L.C**
Christa jyothi high school mudgal (2013)
PERCENTAGE:84.32%

## VERIFICATION SKILLS

**System Verilog HVL:** Interface and clocking block, Inheritance and Polymorphism, Constraint randomization – Inline, and semaphores, Functional coverage, CRCDV and regression testing.

**System Verilog Assertion:** Types of assertions, assertion building blocks, sequences with edge definition and logical relationship. Sequences with different timing relationships. Clock definitions, implication and repetition operators, different sequence compositions, inline and binding assertions, advanced SVA Features and assertion Coverage.

**UVM**: UVM Objects and components, UVM Factory and overriding methods, Stimulus Modeling, UVM Phases, UVM Configuration, TLM, UVM Sequence, virtual sequence and sequencer, introduction to RAL.

## ACADEMIC SKILLS

- Keilμvision
- LABVIEW
- LTESPICE IV

## ACHIVEMENTS

➢ **Presented a research paper entitled "Design of discrete cosine transform for H.265 using vedic algorithm"**
Participated in the Three Day National Conference during 1 to 3rd july 2022 on "Electronics Engineering Trends: The Future of the electronics and communication" organized by sharnbasva university, kalaburgi. got a first prize for presentation

➢ **Presented a search paper entitled "password based security lock system" .**
Participated in "National Research Conference on Engineering Business Management, Sciences, Humanitics & Social Sciences. Humanitics & Social Sciences – 2022"(NRCEBHS – 2022)held on 6th March 2022, organized by Godutai college of Engineering Kalaburgi.

## LANGUAGES

KANNADA ●●●●●
ENGLISH ●●●●●
HINDI ●●●●○

## HOBBIS

- Reading news paper
- Cooking
- Playing with kids

## PROFESSIONAL TRAINING

Maven Silicon VLSI Training Centre

- Dec 2021 till date

## PROJECTS

**Alarm clock based on fpga using verilog**

- **Description-** Project is based on HDL coding as we use fpga board**,** we can observe result in LCD also alarm buzzering.

**A novel approximate adder design using error reduced carry prediction and constant truncation employing parallel prefix adder**

- **Description-** Project is based on verilog coding, novel approximate adder the carry prediction strategy reduces error rate , and increases overall computation accuracy by reducing error distance.

**Router 1x3 RTL design and verification**

- **Description-** The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1,channel2.

## INTRENSHIP

Maven silicon VLSI Training Centre

Advance VLSI Design intrenship

26/mar/2022 to 26/jul/2022

## DECLARATION

I hereby declare all the above information is given true to the best of my knowledge and belief.

Thanking You…

NIVEDITA