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Executive Summary

- Working as the design verification Engineer since one year
- Possess the analytical skills necessary for engineering innovative approaches in VLSI field.
- Solid understanding of VLSI design and Verification environment.
- Good Knowledge of ASIC flow, HDL languages.
- Good working understanding of SV and UVM.

Skills Summary:

HDLs	: Verilog
HVL	: System Verilog
Verification Methodology	: Constraint Random Coverage Driven Verification (CRCDV), Assertion Based Verification (SVA).
TB Methodologies	: UVM
Programming Languages	: C.
EDA Tool	: Modelsim (Questa), Xilinx ISE Design
Operating Systems	: Linux, Windows
Protocols	: AMBA-APB, AHB, AXI (basic understanding),
Other	: Assembly Language.

Work Experience:

- Working as the design verification Engineer at Synapse Techno Design Innovations Pvt from May2022.

Project Details

VLSI Projects:

Project 1:
Project Title : AMBA APB
HDL : Verilog
HVL : System Verilog
EDA Tools : Questa
Description : The APB is part of the AMBA 3 protocol family. It provides a low-cost interface that is optimized for minimal power consumption and reduced interface complexity. The APB interfaces to any peripherals that are low-bandwidth and do not require the high performance of a pipelined bus interface.

Project 2:
Project Titlle. : Dual Port RAM
HDL : Verilog
HVL : System Verilog
Description : Dual Port RAM has separate ports for Write and Read .This project is Deals with understanding of Memory Behaviour with help of Sv TB architecture that is how Memory Behaves for Multiple reads and Multiple Writes at different memory locations .In this project have used constraints that helps to target specific memory locations according to the test .I have also used

Reference Model to mimic the original behaviour of the design and checker to check the functional correctness of the design and recording the status in the scoreboard.

Education:

Education	Institute	Year of Completion	Percentage (%)
B. Tech (EEE)	Rajiv Gandhi University of Knowledge Technologies(RGUKT) -Nuzvid	2021	86.6
PUC	RGUKT -Nuzvid	2017	92.3
SSC	ZPHS Kandlagunta	2015	9.5(GPA)

Leisure Time Activity

- Watching motivational video.
- Watching Movies.

Extra-Curricular Activities & Achievements

- Participated in NCSC(National Children Science Congress) -2013 and in finals secured B+grade
- In Grade VII got NMMS(National Means Merit Scholarship) .

Personal Details:

Father's Name. : SK Sara Saheb

Date of Birth : 25th may 2000
Languages : English, Telugu, Hindi
Nationality : Indian
Address : cheemalamarri,Guntur A.P-522615.