Atul Bhardwaj
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Career Objective

A motivated individual seeking for a responsible position as an entry level Physical Design Engineer which will qualify me to bring the best out of my knowledge and experience in achieving growth and development along with benefiting the organization

Core Competancy

- Acquired core knowledge in ASIC PD Flow involving Floor Planning, Power Planning, Placement, Clock Tree Synthesis and Routing.
- Hands-on-experience on the industry tools such as Synopsys IC Compiler II for APR flow and Prime Time for Static Timing Analysis.
- Placement of macros based on data flow lines, ports and also providing with a required routing and placement blockages in the floorplan.
- Generated an optimized placement block with controlled congestion through various iterations of channel spacing and modifying floorplan.
- Knowledge in interpreting timing reports, fixing Setup and Hold violations and the concept of adjusting the clock skew in order to fix setup and hold violations.
- Dealing with Timing Paths of various PVT corners, Modes, Scenarios, concept of CRPR and also understanding of the constraints to define the False and Multi-Cycle Paths.
- Analyzing and fixing of the DRC and DFM issues.
- Comprehensive knowledge on the concepts of STA, Logic Design.

Education Details

Advanced Diploma in ASIC Design **2022**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2021**
SEA College of Engineering and Technology, with 7.4 CGPA

2017
Narayana PU College, with 59.9 %

SSLC **2015**
SEA Internatinoal School, with 69 %

Domain Specific Project

RV-VLSI and Embedded systems Design Centre, Bengaluru

Graduate Trainee Engineer Sep-2022 to Feb-2023

Block level Physical Design implementation

Description

A block level Implementation of a design at 40nm technology node with a list of 34 Macros, 40K+ Standard Cells, operating at a frequency of 833 MHz and a nominal supply voltage of 1.1V with a Target IR drop of 5% and an assigned Power Budget of 600mW

Tools

Synopsis Prime Time tool for STA, Synopsis IC compiler II for APR flow

Challenges

- Designing of a proper floorplan by ensuring a contiguous area between the macros and creating a good power routing such that it doesn't violates the IR drop,
- Overcoming congestion problem by keeping it under control with respect to global route congestion, also adding few partial blockages to control congestion at Standard cell area.
- Analyzing the timing reports and debugging the cause for setup and hold violations and working for the slack to be under control.

B.E / B.Tech Academic Project

SEA College of Engineering and Technology

IoT based Accident detection system using ESP8266

Description

The basic concept which is emerged out from our project is to build an IoT based accident detection system with the help of Node MCU ESP8266 module and a vibration sensor

Tools

Language : Embedded C Tools Utilized : Node MCU

Challenges

- Implementing the hardware and software together simultaneously so it works in real world situations, so we had to add a base level Multisensor vibration sensor.