(+91)9356015654
shinisamal1996@gmail.com

Subhashini Samal

Summary

Seeking a challenging role as a DFT Engineer in an environment where I could learn, grow, and meaningfully contribute to the success of the company

Skill And Competency :

- Mentor Tessent – Fast scan,
- Tessent Questa Advanced simulator,
- Test Kompress & ModelSim Verilog Basic Knowledge.
- Linux Basics.

Additional Certification:

Completed six months of Professional training in DFT from Semicon technolabs Pvt Ltd, Bengaluru

- Digital Design Scan Insertion,
- scan DRC Violations and fixes
- Scan Compression
- Various Fault models and analyzing faults
- Stuck-at and at-speed ATPG
- Coverage Analysis for Test Coverage improvement
- Pattern Simulations

Knowledge in EDA tools:

- Tessent – FastScan, Test Kompress & MBIST Architect
- Tessent - ModelSim
- Xilinx ISE 14

Project Experience

Project And Design: Test Project 1- 1K flops
No Of Clocks: 1
Tools used: Tessent – Fastscan & ModelSim
3 months

- Performed Scan Insertion
- Checked for DRC violation
- Fixed DRC violations S1 & S2 by inserting test points
- Generated Patterns for Stuck-at
- Analyzed coverage drop Simulated Stuck-at patterns

Project And Design: Test Project 2- 2K Flops
No Of Clocks: 1
Tools used: Tessent– FastScan, TestKompress & ModelSim
3 months

- Inserted Scan circuitry
- Checked for DRC violation
- Fixed DRC violations
- Insertion of Compression Logic
- Stuck-at & at-speed pattern generation
- Coverage Analysis and improvement
- Simulation of Stuck-at patterns

EDUCATION

Bharati Vidyapeeth Deemed to be University, College of Engineering
2017 - 2020, Pune
Bachelor Of Technology, Electronics & Tele-Communication