Amal Chandra

Associate Engineer

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A passionate Physical Design Engineer with an objective to enhance career and gain professionalism within the VLSI industry by executing challenging duties continuously by learning new skills, and utilizing my knowledge towards organizational goals.

EMPLOYMENT HISTORY

Associate Engineer ► Techmahindra Cerium systems, Kochi **Sep 2020 - Apr 2023**

SKILLS

Unix | Tcl | Fusion Compiler, Prime Time, Design Compiler, ICC2 | Vim | Digital Design | C++, Python, Java | Static Timing Analysis | Place & Route | Shell scripting | ECO | Strong Communication | Critical Thinking | Problem Solving | Debugging | Situational Awareness | Teamwork | Customer Handling | Client Relationship Management | Punctuality | Quick understanding of new systems and processes

PROJECT EXPERIENCE

EPG_CNV_SDCOE (Dec 2020-April 2022)

Client: Intel
Technology: 7nm
Tools: DC, ICC2, PT
Responsibilities: Responsible for RTL2GDS2(Synthesis, floorplan, placement, CTS, Route)-Block level.
Floorplan done properly at partition level.
Resolved congestion issues by applying blockages and keepout margins.
Proper communication with clients to achieve better recipes.
Challenges: Handled multiple blocks throughout this project.
Floorplan done properly to reduce congestion with block consisting of 130 macros.
pin placement were done by using scripts for proper floorplanning.
Performed multiple iterations to achieve the goal within the specified time period.
Block gate count: 5 lakh
Block clock frequency: 3GHz
Block period: 340ps

GTCHE_D2G_SDCOE(May 2022-Dec 2022)

Client: Intel
Technology: 5nm
Tools: FC,PT
Responsibilities: Responsible for RTL2GDS2(Synthesis, floorplan, placement, CTS, Route)-Block level.
Performed multiple techniques to meet timing requirements.
Timing violations were fixed at FC and PT.
Proper communication with clients to achieve better recipes.
Challenges: Violations were fixed within time.
Timing script used to fix the timing violations since there were lot of violations and to meet the deadlines.
Performed multiple iterations and techniques to achieve the goal within the specified time period.
Repeaters were adjusted properly in multiple iterations to achieve timing improvement.
Extensive ECO to close the partition w.r.t Timing/DRC/DRV/LV/RV etc across all signoff corners.
Block gate count: 1 million
Block clock frequency: 3.125GHz
Block period: 320ps

IPG_PPC_SDCOE(Jan 2023-April 2023)

Client: Intel
Tools: PT,FC

Technology: 3nm
Responsibilities: Responsible for timing closure at top level.
Timing closure were done to tape-out the project.
Written ECO scripts to fix the timing issues.
Challenges: Top level consisted of multiple blocks. Effectively closed those timings.

CERTIFICATIONS

Digital warrior award for good performance in the project.
Tcl 1: Becoming a proficient user by Synopsys.
Become a Linux professional by Udemy.
IC Compiler II: Block level Implementation by Synopsys.

INTERNSHIPS

► Uniq Technologies **Jul 2019 - Jul 2019**

Learned about the basics of embedded systems.
Gained some knowledge about the role of embedded systems in robotics for building robots for some specific applications.

► BSNL **Jun 2017 - Jun 2017**

Learned about telecom technologies.

ACADEMIC PROJECTS

Final Year Project

An All-Terrain Electric Vehicle with pothole mapping using LIDAR.

Mini Project

Automatic slot assigning parking system.

EDUCATION

BTech ► Rajagiri School of Engineering and Technology, Kochi **2016 - 2020**

+2 ► St Joseph's Higher Secondary School, Thalassery **2014 - 2016**

DECLARATION

I hereby declare that the details provided above are best of my knowledge.

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Yours Sincerely
Amal Chandra