







# NUNAVATH KUMAR

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## ABOUT ME

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A Fresher in the area of VLSI, looking for full-time employment. Ability to grasp new concepts, ideas and come up with innovative solutions to problems. Demonstrate an ongoing high level of motivation and dedication required to meet deadlines.

## PROFESSIONAL QUALIFICATION

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### ADVANCED VLSI PHYSICAL DESIGN & VERIFICATION COURSE

Maven Silicon VLSI training center, Bangalore, Karnataka  
Sep 2022 till date

## EDUCATION

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### B.TECH IN ELECTRONICS AND COMMUNICATION ENGINEERING

JNTU University | 2022

- JNTUH College of engineering Hyderabad
- 1st class with 8.01 (CGPA)
- From Telangana

### DIPLOMA IN ELECTRONICS AND COMMUNICATION ENGINEERING

State Board Of Technical Education & Training | 2019

- T D R Polytechnic College Bibinagar
- 1st class with 90.20%
- From Telangana

### SECONDARY SCHOOL CERTIFICATE

Board of Secondary Education Telangana | 2016

- Z P P High School Battuguda, Yadadri Bhuvanagiri
- 7.3 (GPA)
- From Telangana



**HDL**

- Verilog 

**EDA TOOLS**

- Mentor Graphics- Quartus prime and Modelsim
- Siemens EDA- Oasys-RTL, Aprisa, Calibre
- Tanner tool- S-Edit, L-Edit
- Synopsys tool- Fusion Compiler

**PROGRAMMING LANGUAGES**

- Programming C 
- OOPs Java 
- Python 

**OPERATING SYSTEM**

- Working knowledge on Windows and Linux

**CORE SKILL**

- RTL Coding using Synthesizable constructs of Verilog, FSM based design, Simulation.

**DIGITAL ELECTRONICS**

- Digital Electronics, combinational & sequential circuit, FSM, Memories, Number System and Codes, Logic Circuits.

**CMOS**

- CMOS implementation, CMOS Inverter Design & Layout Design, Stick diagram.

**STATIC TIMING ANALYSIS**

- STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks Clock domain and Variations, Clock Distribution Networks, Fixing timing failure.

**VERILOG PROGRAMMING**

- Data types, Operators, Processes, Blocking assignment & Non Blocking assignment, begin - end & fork join blocks, looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Synthesis.

## PHYSICAL DESIGN SKILLS



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### PHYSICAL DESIGN

- Logic Synthesis, Floor Planning, Power Planning, Placement, Routing, Clock Tree Synthesis, Timing Analysis using Aprisa & Fusion Compiler.

### VERIFICATION

- DRC, ERC, LVS and Sign-Off using Calibre.

## PROJECTS



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### ROUTER 1X3 – RTL DESIGN AND VERIFICATION | MAVEN SILICON

- **Description:** The router accepts data packets on a single 8-bit port and routes them to one of the three (FIFO's) output channels channel 0, channel 1 and channel 2
- Technology-250nm, Frequency-20KHz, Metal layers- 4, Tool-Aprisa.

### AUTOMATIC FIRE ALARM SYSTEM | B.TECH

- **Description:** The project purposely is for house safety where the main point is to avoid the fire accidents occurred to the residents and the properties inside the house as well. It utilizes Arduino Uno board in conjunction with ATmega328 chip.

## INTERNSHIP



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### INTERNSHIP AT L&T TECHNOLOGY SERVICES

- From Jan | 2022 To May | 2022
- Automatic Door Light Sensor using Atmega 328p
- Car wiper System Using STM32F board

## STRENGTHS



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- Problem-solving and analytical thinking
- Team player and ability to work well with others
- Leadership abilities

## HOBBIES



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- Photography
- Playing cricket
- Cooking

## DECLARATION



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I hereby declare that all the details furnished above are true to the best of my knowledge and belief.

PLACE: Hyderabad  
DATE :

Nunavath Kumar