KADEMANE BASAVARAJU
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OBJECTIVE **:** To become a successful professional by working with dedication and commitment in an esteemed Organization where I can put up my knowledge as VLSI engineer for the growth of the organization and expand my potential to the maximum.

ACADEMIC QUALIFICATION:

Degree	*Institution*	*Board/ University*	*Year of Completion*	*CGPA/Percentage*
B.Tech(EEE)	*Sree Vidyanikethan Engineering College,Tirupati*	*JNTUA*	*2021*	*80.00%*
Higher Secondary	*Sri Chaitanya Jr.College, Vijayawada*	*Board of Intermediate Education of Andhra Pradesh*	*2017*	*95.5%*
Secondary School	*Z P HighSchool Govindawada*	*State Board ofSecondary Education*	*2015*	*9.7 CGPA*

Professional Experience : (1 YEAR)

- 1 year of experience working with DESIGN and VERIFICATION at **TECH MAHINDRA CERIUM Pvt. Ltd** ,Bangalore
- Trained on IP/SoC Verification

Professional knowledge:.

- Knowledge on Digital Electronics
- Knowledge on making Testbench in **VERILOG** and **UVM**.
- Hands on experience in **Verilog, SV, UVM**.
- Have knowledge on **AHB,APB**,**AXI** protocols
- Knowledge on Analog Electronics
- Familiar with RTL coding.
- Good knowledge on writing constraints and assertions.
- Basic knowledge on CMOS circuit design.

Technical Expertise:

- Tools : XILINX, Synopsys VCS, QuestaSIM
- HDL/ HVL : Verilog and System Verilog
- Methodologies : Universal Verification Methodology (UVM)
- IP Protocols : APB,AHB,AXI
- Operating Systems : LINUX and WINDOWS
- Terminal emulator : Putty , Xming (display server)

Project Summary:

1. Design and Verification of Synchronous and Asynchronous FIFO :

- Developed testcases in Verilog and System Verilog
- Verified the write and read operations at FIFO
- Asserted full and empty conditions

- Verified testbench with different test scenarios like single read, write and concurrent read and write operations.

Language	**:**	Verilog, System Verilog
EDA TOOL	**:**	QuestaSim

2. Design and Verification of AHB to APB Bridge:

- Developed testcases in UVM
- Verified the write and read operations for bridge
- Verified UVM testbench with different test scenarios like single read, write and burst read, write with different burst lengths.

Language	**:**	UVM
EDA TOOL	**:**	EDA playground

PROGRAMMING LANGUAGES:

- C
- Verilog
- System Verilog
- Basic knowledge on Python
- UVM
- MATLAB and SIMULATION

OPERATING SYTEM **:** **Linux**

SCRIPTING *LANGUAGES* **:** **Perl**

PERSONALITY TRAITS:

- *Creative Learner*
- *Willing to know about new technologies*
- *Team Management and Leadership*
- *Good Communication skills*

ACHIVEMENTS:

- *Certificate on Digital System Design by Tech Mahindra DEXT*
- *Certificate on Verilog by Tech Mahindra DEXT*
- Certificate on System Verilog by Tech Mahindra DEXT

DECLARATION:

I hereby declare that above given information is true to the best of my knowledge.

(K Basavaraju)