**LAXMI PATIL**
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**Objective :**

Seeking responsible carrier which provide me an opportunity to deliver my best and upgrade my skills in engineering and meet the demands of the organization.

**Professional training:**

Physical Design course, **VLSIGURU** training institute, Bangalore.

**JULY 2022–DEC 2022**

**Projects:**

**Project Title: ORCA TOP (multi voltage) (Block level)**

Worked At: VLSIGURU institute.

Description: Physical implementation of a block-level design (Netlist to GDSII)) at **28nm technology**, using 40 macros and standard cells 52k (approx..) ,I/O ports: 240, Number of clocks: 8 (3 Main clocks, 3 Generated clocks and 2 Virtual clocks), the clock frequency of 54MHZ, a supply voltage of 0.75V and 0.95V by using 9 metal layers.

**Tool Used: Synopsys IC Compiler (ICC2), Prime Time, StarRC**

**Responsibilities:**

1) Involved in creating Floor Planning, Power Planning
2) Running Placement, Clock tree synthesis and Routing.
3) Timing fixes (setup and Hold) pre-CTS and post-CTS including transition fixes.
4) Performing multiple floorplan iterations based on data flow to resolve congestion issues.
5) TNS under control, and acceptable standard cell utilization.
6) Fixing DRV/LVS, StarRC extraction
7) Physical verification, Static timing analysis.
8) Solved DRC, DFM, and LVS.

**Technical Skills:**

- Hands on experience in working with EDA tools: **ICC2, Prime Time, StarRC /Xtract**.
- Scripting languages **: TCL** (intermediate)
- Operating Systems: Basics of Linux and Windows
- Fundamental knowledge of digital electronics, Transistors, CMOS design
- Good knowledge of Floorplan, Placement, CTS, Routing, Physical verification, Static timing analysis and Timing ECO
- Good knowledge of Fixing DRV / LVS / Antenna, Crosstalk, Electro migration, Antenna effect, Latch-up for design.
- Good knowledge of STA using Prime Time.
- Good Knowledge in understanding of various timing reports during STA.

**Extra-curricular activities:**

- Student Member of from 2016-2020.
- Participated in **"AISYWC'17 and AISYWC'18– All India Student and young professional, Women in Engineering Congress"** organized in IIIT Allahabad and VVIT Mysore respectively.
- Attended the PCB workshop on "**Design and Fabrication of PCB**" conducted under IEEE-PES Student Branch Chapter (35261A) Organized by Department of Electrical and Electronics Engineering.

**Strengths:**

- Ability to work independently as well as a team member, Quick Learner .
- Problem-solving capability, responsibility, self-motivated.

**Soft Skills:**

punctual and disciplined
Team work
Volunteering
Presentation skills
Project Management
Social Networking

**Education:**

| Sl. No. | Qualification | YOP | Institution | Affiliated Board | C.G.P.A/ Percentage |
|---|---|---|---|---|---|
| 01. | Bachelor of Engineering (EEE) | 2020 | Basaveshwar Engineering College, Bagalkot | Visweshwaraiah Technological University(V.T.U) Belgaum. | **7.62** |
| 02. | PUC | 2016 | Tungal PU College,Jamkhandi. | Karnataka PU Board | **87%** |
| 03. | $10^{th}$ Grade | 2014 | G H S Vajjaramatti, Mudhol. | KSEEB | **91.52%** |

**Declaration:**

I hereby declare that information furbished above is correct to best of my knowledge.

(LAXMI PATIL)