Sindhu Mathy S

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Design for Testability Engineer/ Assistant Professor

Executive Summary

- Qualified trained professional with 8 months of experience in the field of Design for Testability using Mentor graphics tool.
- Proven ability in conducting subject related classes based in course curriculum as participating in curriculum co- ordination meetings with the staff.
- Proven ability in complex projects to effective completion aligned to specific requirements.
- Seasoned leader capable of providing direction to internal teams, managing cross-functional training, strengthening organizational diversity.

Key Skills

✦ Scan Insertion,EDT	✦ ATPG	✦ Simulation
✦ Verilog	✦ Unix/Linux	✦ Digital Electronics
✦ MBIST	✦ TCL	✦ JTAG
✦ Teaching & Academics	✦ Career Counselling	✦ Seminars & Workshops

Professional Training

Undergone Professional training in **Design for Testability (DFT)** from VLSI Guru, Bangalore. (Mar 2022 - Till Date).

➢ **Training Outline**

ASIC Flow, DFT Fundamentals, Scan Design, Scan DRC, Scan Insertion, Scan Compression, Boundary Scan (JTAG), ATPG, ATPG Fault Models, Simulation.

➢ **Tools Used in Training**

Tessent: Tessent Scan, Tessent TestKompress, Tessent FastScan. **Synopsys:** Synthesis.

Training & Internship Experience

Project 1: "Test_block"

Inserted scan for the design and analyzed the scenarios of bus contention, clock domain mixing, where to use the latch and black box. Inserted EDT for scan net list and generated EDT outputs and observed.ATPG pattern generation for Stuck-at and Transition fault models and also analyzed various ATPG fault classes, difference between transition and path delay tests, and necessity of defining black box. Achieved coverage of 98% for stuck at and 90% for transition.

Project 2: "Test_block-2"

This Test blocks consists of 3 clock domains with 22K flop count. Different test schemes like basic scan, compression mode for both DFT faults models like Stuck-at and At-Speed. The test coverage achieved was 99.1% and At-Speed coverage. Initial set up has been done for Scan and ATPG. Patterns are generated using Tessent Fastscan and validated using QuestaSim.

Assistant Professor (March 2017 – Feb 2022)
KIT-KalaignarKarunanidhi Institute of Technology,

Key Responsibility

- Prepared schedules for delivering course programs/ other assessments for students based on assigned syllabus and curriculum requirements
- Evaluated students using tutorials and formal evaluations, produced evaluation summaries and provided feedback to the institute management team.
- Designed / implemented tools to evaluate individual student's requirements based on identified weaknesses. Guided students in various projects and assignments including career development and other related issues.
- Functioned as Placement Coordinator, Teaching Coordinator. Represented the organization in FDP/Industrial Training/Short term Course/Research Seminars.

Research Project Details

Design of four way out of phase slot line power dividers: A compact two two-way out-of-phase slotline power divider operating at C-band using ADS.

IOT based automation for medical drug storage: To Monitor the drugs and medicines in the store and, their location by using IOT technology and RFID.

Education

ME (Communication Systems - ECE), Dr Mahalingam College of Engineering & Technology (MCET) ,Pollachi (2015) [CGPA-8.80 with Distinction]

BE (ECE), KIT-KalaignarKarunanidhi Institute of Technology, Anna University – Coimbatore (2013) [CGPA -8.10]

PROFESSIONAL DEVELOPMENT:

Certifications:

- Completed NPTEL Swayam certified course on **Digital Circuits**, Conducted by **IIT-Kharagpur**, July 19 to Oct 19.
- Completed NPTEL Swayam certified course on **Wireless and Cellular Communications**, Conducted by **IIT-Madras**, July 18 to Oct 18.
- Completed NPTEL Swayam certified course on **Basics of Software-defined radios & practical applications**, Conducted by **IIT-Roorkee**, Feb 18 to Mar 18.

Training courses and workshops:

- Faculty Development Training Program on "Control Systems & Sensors Technology" Bhilai Institute of Technology, Nov 2020.
- Faculty Development Training Program on "Emerging Trends and applications of Multiresolution Analysis Techniques in Wireless Communication", Pondicherry, September 2019.
- Attended Workshop on MATLAB Programming and Real-Time Simulation, Mathworks , Dec 2020
- Attended Workshop on 5G Technology and its Applications, March 2019.
- Attended Workshop on Artificial Intelligence and Signal Processing Using MATLAB, March 2019.

Publications:

- Analysis of Magnetic Resonance Image Segmentation using spatial fuzzy clustering algorithm, Published in **Journal of Global Pharma Technology** on Oct, 2018.

Personal Details

- Nationality : Indian
- Date of Birth: 01.08.1991
- Marital Status: Unmarried
- Hobbies and Interests: Gardening and Glass painting
- Languages: English, Tamil
- Address: 41, Ramachandra Nagar, Ondipudur, Coimbatore- 641 016.