Lingaraj K Hottin

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Professional Goals

To build a career in VLSI domain by working in an organization where my ability and skills will be utilized effectively for the betterment of myself and the Organization

Core Competency

- Trained in Sanity Check, Floorplan, Power plan, Placement, CTS, Routing and STA.
- Good knowledge and understanding of STA concepts: Fixing setup and hold violations, understanding oftiming reports, effect of skew on timing, OCV, latch concepts.
- Hands on experience on VLSI tools: ICC2 COMPILERGood.
- Understanding of Digital Logic Design, CMOS, MOSFET.
- Fundamentals Good knowledge on Unix/Linux, Synthesis flow Sign-off Checks and Physical Verification.
- Understanding of complete ASIC design flow and Physical Design flow.

Academic History

Advanced Diploma in ASIC Design - Physical Design, Takshila Institute of VLSI Technologies, Bangalore (January 2023)

Bachelor Degree in Electronics and Communication, SKSVMACET, Visvesvaraya Technological University (2018 –2022) (6.83 CGPA)

Pre-University PCMB, S A PU College Naregal,
Karnataka PU board (2016-2018) (62%)

Secondary School Leaving Certification (SSLC), P S S High School Naregal
KSEEB (2016) (72%)

Domain Specific Projects

Takshila Institute of VLSI design, VLSI Design Centre, Bangalore.

Physical Design Trainee

1) SOC Block level Implementation of ORCA_TOP_IO Project (28nm Technology node)

Tool: ICC2 compiler by Synopsys

Description:

- Technology: 28nm
- No.of macros: 30
- Layer: 9
- Std.cell count:50000
- No.of Clocks: 7 clocks
- Frequency: 400MHZ

Responsibilities

- Completed SOC Block level Physical design which involves implementation of Sanity Check, Design setup, Floorplaning ,Power planning, Placement and clock tree synthesis Routing.
- Physical Verification DRC, LVS, and DFM checks
- Sign-off checks and Tapeout

2) SOC Block level Implementation of ORCA_TOP Project (32nm Technology node)

Tool: ICC2 compiler by Synopsys

Description:

- Technology: 32nm
- No.of macros: 40
- Layer: 9
- Std.cell count: 56013
- No.of Clocks:7
- Frequency: 416MHz

Responsibilities:

- Completed SOC Block level Physical design which involves implementation of Sanity Check, Design setup, Iterative Floorplaning , Power planning, Place and CTS optimization
- Routing, Physical Verification, DRC, LVS, and DFM.
- Timing Closure and ECO Sign-off checks and Tapeout.

3) Static Time analysis

Description:

Complete analysis of different types of timing paths, setup and hold time, TCQ, latency, clock skew, uncertainty, maximum delay and minimum delay and derate factors.

Challenges:

- Computing setup slack and hold slack for different timing paths by using skew and delay tables finding worst
- slack and best slack for setup and hold
- Understanding the causes for setup violation and hold violation
- Understanding of derate factors, PVT, corners, OCV and AOCV

Academic Project

- Title: IOT Based Smart Ambulance
- Tool: Arduino IDE.
- Role: Team Lead
- In Smart Ambulance different type of sensors are used like Temperature, Pulse oximetry and Heart Rate,
- Simultaneously in traffic RF transmitter and RF receiver, both the results will be sent to near hospital.
- Helps: life saving of patient and time consumption.

Skills

- Physical Design
  - Sanity Checks
  - Floorplan & Power plan
  - P&R
  - DRC
- Static Timing Analysis
- Linux
- Synopsys IC Compiler (ICC2)

Certifications:

- **Takshila Institute of VLSI Technologies**

  Title: professional Training on physical design.

Personal Details

Date of Birth : 10/07/2000
Address : Kalakappa N Hottin, Near Veerabhadreshwara Temple Nidagundi Tq: Gajendragada
Dist: Gadag Karnatak 582114.
Languages Known : English, Kannada, Hindi.

Declaration:
I hereby declare that I would be glad to come for interview at any time that is convenient to you and assure you of my devoted service.

Date:
Place:

Lingaraj K Hottin