Pravallika Emani

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Guntur-522237, Andra Pradesh

Career Objective

To obtain a challenging and responsible position as a Physical Design Engineer with an opportunity of advancement.

Core Competancy

- Acquired good knowledge and proficiency in ASIC PD Flow involving Floor Planning, Power Planning, IR drop Analysis, Automatic P&R, CTS and Routing.
- Comprehensive Knowledge on STA, CRPR, Interpreting timing reports, fixing Setup and hold violations.
- Analysed timing reports of Pre-layout and Post-layout STA on PrimeTime and IC Compiler 2
- Hands on experience in APR tools-Synopsys ICC2 and STA tool- PrimeTime
- Good knowledge in Logic Design and Circuit Theory.
- Have knowledge in Applications of Semiconductor Devices and Basic Electronics.
- Have knowledge in TCL scripts, Linux for VLSI Engineer and Perl for VLSI Engineer.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2022**

RV-VLSI Design Center

Master Degree in **VLSI & ES** **2022**

University College of Engineering Kakinada, with 8.2 CGPA

Bachelor Degree in **Electronics and Communication** **2020**

Vignan's Nirula Institute of Technology and Science for Women,Guntur, with 8.01 CGPA

2016

Sri Chaitanya Junior College, Guntur, with 91.2 %

SSLC **2014**

Mary Matha English Medium HIgh School, Thullur, with 97 %

Domain Specific Project

RV-VLSI and Embedded Systems Design Center.

Graduate Trainee Engineer Jun-2022 to Sep-2022

Static Timing Analysis.

Description

Timing Reports are analyzed for Latches and Flipflops based timing paths at different environment conditions for timing violations considering Clock Skews, PVT variations, OCV(AOCV), CRPR and Signal Integrity by honoring the constraints file

Tools

Synopsys PrimeTime, Synopsys IC Compiler 2.

Challenges

- Analysed all the timing paths in different timing paths and observed the violations
- Understanding the Setup and Hold Violations.
- Understanding the effect of Clock Skew on Timing Slack and PVT variations on delay.
- Interpreting violations such as Recovery, Removal, No-change timing.

RV-VLSI and Embedded Systems Design Center.

Graduate Trainee Engineer Jul-2022 to Sep-2022

Floorplan and Placement for an ASIC block.

Description

Overview: Technology- 40nm, Supply voltage- 1.1V, Vt of transistors-svt, ltv, htv, Area- 4.2mm2, Clock frequency - 833MHz, Power Consumption -600mW, Max. IR drop(VDD + VSS)- 5%.

Tools

Synopsys IC Compiler 2

Challenges

- Understanding the setup and design constraints and designing the floorplan as per data flow diagram. Building the good Power plan to meet the IR drop requirement.
- Floorplan with high Utilization ratio and good contiguous core area. Designed good power mesh to connect all the macros and standard cells without any floating point.
- Controlling the congestion and checking for the timing violations.
- Rectifing the DRC errors in the Floorplan and Placement stages.

RV-VLSI and Embedded Systems Design Center.

Graduate Trainee Engineer Jul-2022 to Sep-2022

CTS and Routing of an ASIC block.

Description

Overview: Technology- 40nm, Supply voltage- 1.1V, Vt of transistors-svt, ltv, htv, Area- 4.2mm2, Clock frequency - 833MHz, Power Consumption -600mW, Max. IR drop(VDD + VSS)- 5%.

Tools

Synopsys IC Compiler 2

Challenges

- Understanding the Clock Tree Synthesis to meet the target Skew, Max/Min Latencies.
- Analyzing the differences between the Classic Flow and CCD.
- Fixing the timing violations, DRC and LVS errors.

B.E / B.Tech Academic Project

Vignan's Nirula Institute of Technology and Science for Women,Guntur

Automated Vehicle for Physically and Visually Challenged people

Description

Autonomous vehicle contains ARDUINO UNO as the core system having functionalities like Traffic light detection, vehicle detection, pedestrian detection, roadside lane detection to make the vehicle self-movable in autonomous mode.

Tools

Aurdino-UNO, HC-12 Module, Ultrasonic Sensor, LCD, LED, L298N Motor Driver, Motors, Switches and Battery.

Challenges

- Detection of Traffic light based on real world traffic system. Setting the range of Ultrasonic sensors to detect the Pedestrians, Road lane and Vehicles. Location tracking System is not inbuild in the Vehicle, so we need to use Separate GPS tracker.

M.E / M.Tech Academic Project

University College of Engineering Kakinada

Design of Imprecise Multiplier Using Dual stage Compressor with Reversable Logic.

Description

An Imprecise Multiplier with Dual stage 4:2 Compressors optimized for realization using reversible logic. Using the reversable logic gates the Dual stage 4:2 Compressors and PPA are designed. Area power and delay are reduced in this multiplier.

Tools

Xlinx Vivado 2018.3

Challenges

- Selection of the Dual stage 4:2 Compressor for the design. Designing the multiplier using adders and compressors with reversable logic. Reducing the delay of the multiplier using Parallel Prefix adder.