KOMMALA NAGASAI SRINIVAS

TRAINEE IN PHYSICAL DESIGN

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CAREER OBJECTIVE

Looking for challenging and diversified workplace where I can dedicate my work of theoretical knowledge and practically implementing those skills in a productive way, which would enable me to grow while fulfilling organization goals.

PROFESSIONAL TRAINING

MAVEN SILICON
APRIL 2022- Present

Physical Design

- Learnt synthesizing the netlist, implementing Physical design flow and physical verification using EDA & Synopsys tools.

EDUCATION

- **Master's in Communication Engineering & Signal Processing** from G.V.P college of Engineering (A), Visakhapatnam with 69.40%. (2016-2019)
- Bachelor's in Electronics and Communication Engineering from ANITS College of engineering Visakhapatnam with 65.60%. (2012-2016)
- Class XII from Sri Chaitanya Junior College, Srikakulam with 92.30%. (2010-2012)
- Class X from Gayatri Model High School Srikakulam with 81.83%. (2009-2010)

SKILL SET

VLSI DOMAIN SKILLS:

- **HDL :** Verilog
- **EDA Tool :** Mentor Graphics - Questasim , Xlinix - ISE, Xilinx – Vivado, APRISA and calibre.
- **SYNOPSYS Tool**: Fusion Compiler, Prime Time
- **Domain :** Physical Design flow including netlist extraction using Oasys tool. Floor plan, Placement, Clock tree synthesis, Routing , STA, Signoff using APRISA & Fusion Compiler tool. Physical Verification (PERC, DRC and LVS) using calibre tool.
- **Programming Languages :** C Language (based on the trainee's expertise)
- **Operating Systems :** Working knowledge on Windows and Linux
- **Version Control :** GIT
- **Scripting Languages :** TCL
- **Core Skills :** RTL Coding using Synthesizable constructs of Verilog, FSM based design & Simulation, CMOS Fundamentals, Physical design flow and Physical Verification (PERC, DRC & LVS)

COLLEGE SKILLS

- MATLAB - Digital Signal Processing
- MASM or TASM - Assembly Language Programming (8085 or 8086)
- HIGH FREQUENCY STRUCTURE SIMULATOR - Wireless communication.

ACHIEVEMENTS

•Stood as runners in the intra-department cricket tournament conducted by Anits communication engineers' society (ACES) in the year2016.

•Successfully completed ePROBE 2016 National Level Technical Fest as a coordinator of Hospitality & Accommodation organizedby ECE department of ANITS.

WORKSHOPS

- Participated in "**A three day Hand-on workshop on Design and Analysis of Antenna using HFSS**" held at MVGR college of engineering Vizianagaram.
- Participated in a two day national workshop on MATLAB "NATIONAL LEVEL STUDENT TECHNICAL PAPER CONTEST & EXHIBITION" held at GMR institute of technology & sciences Srikakulam.

HOBBIES

• Listening Music

•Playing Cricket

•Working out in the gym

Subject Expertise:

Digital electronics, Analog electronic, Network analysis, Analog & Digital Communications, Signals & System, Signal Processing, Microcontrollers, Wireless communication.

VLSI DESIGN

Digital Electronics :

Combinational & Sequential circuits, FSM, Memories, CMOS implementation, Stick diagram.

STA :

STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks, Clock domain and Variations, Clock Distribution Networks, Fixing timing failure.

Verilog Programming:

Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks, looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Synthesis issues, Races in simulation, pipelining RTL & TB Coding,

Physical Design :

Netlist Extraction using Oasys. Floor plan, Placement, Clock Tree Synthsis, Routing, STA, ECO and Sign off using Aprisa & Fusion compiler. Physical Verification (PERC, DRC, LVS) using Calibre.

Responsibilities for Design:

- Synthesizing the RTL code and generate the Gate Level netlist.
- Implementing floor plan, Placement, CTS, Routing, STA processes on the netlist
- Performed Timing Analysis and achieved timing closure.
- Performed DRC, PERC and LVS for Physical Verification
- Exporting the Design in GDS-II format.

STRENGTHS

- **Critical thinking**
- **Team motivator**
- **Adaptability to work in all kinds of situations**

CERTIFICATIONS

- **VSD - Physical Design Flow**

Credential: https://www.udemy.com/certificate/UC-29aee1c9-0968-4faa-9969-d41761b5196c/

- **VSD - Static Timing Analysis**

Credential: https://www.udemy.com/certificate/UC-53cfb164-37d0-4762-941e-48e325bd5753/

- **VSD - Timing ECO**

Credential: https://www.udemy.com/certificate/UC-259972b9-8ffd-40d7-96af-1a34880f1374/

- **VSD - TCL programming**

Credential: https://www.udemy.com/certificate/UC-b3f84151-115a-4276-a0f4-70b464f2a24c/

PROJECTS

1.RISCV-32bit – RTL design and Implementing Physical Design Flow
HDL: Verilog
EDA Tools: Model sim, Oasys, Aprisa & calibre
Description: RISCV is an open-source and reduced instruction set computing architecture used in microcontrollers and embedded systems that execute a large number of simple instructions to complete a task.

Responsibilities: Extracted the synthesized netlist from OASYS tool and performed the physical design flow using APRISA.

M.TECH PROJECT

2.Design and analysis of compact antenna using MIMO for wireless applications
Tools: HFSS
Description: Designed a compact MIMO antenna operating over a frequency range of 2.4GHz-5GHz with FR-4 epoxy as substrate obtained high gain with low mutual coupling by placing "SWASTIK" shaped slot between two dumbell patches.
Responsibilities: Designed and simulated MIMO antenna using HFSS.

DECLARATION:

I hereby declare that all the information provided in this resume is true.

DATE: 10-04-2023
PLACE: BANGALORE

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