Ram Bahadur Mahara

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PROJECTS

- 1. ORCA_TOP 28nm Physical Design project at VLSIGURU
 - Hard macros 40 | standard cells 62k | Metal Layers 9 | Max frequency 450MHz | No of clocks -5
 - Developed a block-level (RTL2GDS) multi-voltage design project at 28nm technology.
 - Imported design using NDM's
 - Conducted 4+ design iterations for creating core area and die area
 - Wrote a script in TCL to locate ports.
 - Placed macros according to guidelines to meet timing and reduced congestion
 - Understood UPF and created voltage area for power domains with VDDH 1.16v and VDD 0.75v
 - Carried out power planning and fixed issues after power planning
 - o Performed Placement and CTS with minimum congestion and timing violations
 - o Did routing and fixed shorts and DRC violations after routing
 - o Conducted timing ECO in ICC2, executed signoff RC extraction, and closed timing using Primetime

2. Volcano – 28nm Physical Design project at VLSIGURU

- Hard macros 34 | standard cells 44k | Metal Layers 9 | Max frequency 650MHz | No of clocks -5
 - Implemented floor planning to satisfy time, power, and other design condition after importing the design using NDM.
 - Performed Placement and CTS with minimum congestion and timing violations
 - Did routing and fixed shorts and DRC violations after routing

3. Smart Manhole management system – Final Year Project in B.E. at K.S INSTITUTE OF TECHNOLOGY

- ESP32 microcontroller and the Fast2sms SMS service were used to develop a real-time, intelligent Smart manhole management system.
- The proposed project could gather input from various sensors such as water level sensor, Gas sensor, and
 Tilt sensor and was able to notify the authorized individual.
- Project also had an LCD display that could be used to identify any malfunctioning sensors, and this
 information displayed can be used to correct/replace the component.
- o The tool used was Arduino IDE with C language
- We were able to secure funding of 7000rs from the Karnataka State Council for Science and Technology (KSCST)

EDUCATION

K.S INSTITUTE OF TECHNOLOGY | Bachelor of Engineering (B.E) | Bangalore | 2022

Concentrations: Electronics and communication (ECE) | CGPA: 6.6

RNS PU college | Bangalore | 2018
Pre-University College (PUC) | Percentage 61%

HILSIDE PUBLIC SCHOOL | Bangalore | 2016 SSLC (10th) | Percentage 70.04%

VLSIGURU | Apprenticeship | Bangalore | February 2023

Concentrations: Physical Design trainee

SKILLS & INTERESTS

Technical skills:

- o Good knowledge of Floorplan | Placement | CTS | Routing | Static Timing Analysis
- o Fundamental knowledge of digital electronics | Transistors | CMOS design | IC fabrication Process | Power planning
- o Good understanding of | various timing reports during STA| Global routing | detail routing | Synthesis that is RTL to Gate level conversion
- Hands-on experience in working with ICC2|Prime Time| StarRC/Xtract| Linux| TCL scripting & programming concept
- o Timing ECO | Fixing DRC / LVS
- social skills good at communicating and interacting with others | good at analyzing |
- Languages Fluent in English, Kannada, and Hindi