Jayanth D

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Career Objective

Seeking an opportunity with an esteemed organization for the role of a Physical Design Engineer where I can utilize my skills, enhance learning in the field of work and pave the way for achieving company's goal.

Core Competancy

- Thorough understanding of the ASIC PD flow including the significance of each design phase such as the Floorplan, Powerplan, IR Drop Analysis, Placement, CTS and Routing.
- Comprehensive knowledge of ASIC Netlist to GDSII, as well as practical experience.
- Creating an efficient floorplan with no macro-overlaps and a continuous core area along with placement and routing blockages to prevent congestion.
- Creating an efficient power mesh by choosing the proper metal width, spacing and pitch while taking the constraints into account and ensuring no PG connectivity issues.
- Effective standard cell placement and the construction of a clock tree that attempts to optimise all timing errors such clock skew and delay.
- Understanding signal routing and fixing all DRC, LVS and Antenna Violations.
- Performing Pre-STA and Post-STA and analysing the timing reports generated by them to fix timing violations.
- Consider implementing adjustments like OCV, AOCV, Multicycle Path, False path, Half Cycle path, X-talk, MCMM and PVT Corners after analysing the design restrictions.
- Good understanding and knowledge in logic design, CMOS and MOSFET.
- Basic knowledge on Verilog, Linux and TCL scripting.

Education Details

Advanced Diploma in ASIC Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Dr. Ambedkar Institute of Technology, with 8.48 CGPA

2018

Vidya Mandir Ind. PU College, with 88.5 %

SSLC **2016**

Presidency School, with 94.17 %

Domain Specific Project

RV - VLSI Design Center

Graduate Trainee Engineer Jul-2022 to Aug-2022

Design of Floorplan and Placement of Lakshya Block

Description

Technology : 40nm, Macro Count : 34, Standard cell count : 38403, Supply voltage : 1.1V, Power Budget : 600mW, Clock frequency : 833MHz, IR drop : <55mV, Max. IR drop (VDD+VSS) : 5%

Tools

Synopsys IC Compiler 2

Challenges

- The design constraints were looked at in order to have a continuous core area for standard cells and a floorplan based on a data flow diagram and flylines was constructed.
- In accordance with the IR drop limits, an appropriate power plan was constructed making sure that there were no floating pins, missing vias or PG DRCs.
- Standard cells were positioned and the spacing was gradually increased till the maximum congestion was +1 using an iterative approach.
- Analyzed the reports generated for different timing paths and compared the behaviour of each stage with respect to WNS,TNS and also identifying cause of violation.

RV - VLSI Design Center

Graduate Trainee Engineer Aug-2022 to Sep-2022

Design of CTS and Routing for Lakshya Block

Description

Technology : 40nm, Macro Count : 34, Standard cell count : 38403, Supply voltage : 1.1V, Power Budget : 600mW, Clock frequency : 833MHz, IR drop : <55mV, Max. IR drop (VDD+VSS) : 5%

Tools

Synopsys IC Compiler 2

Challenges

- Implemented two distinct CTS flows with clock propagation and analyzed reports for WNS, TNS, setup and hold for various timing paths.
- Buffers and inverters were added during optimization in order to reduce clock skew and latency.
- Signal routing was created by the tool and all DRC, LVS and antenna violations were fixed.
- Shorts and other DRC problems were corrected manually and antenna violations were resolved by inserting jumpers or diodes in place.

RV - VLSI Design Center

Graduate Trainee Engineer Jul-2022 to Jul-2022

Static Timing Analysis on Block Level Design

Description

In order to understand the setup and hold slack behaviour of flip-flops and latches, STA was performed on various timing paths with various test cases.

Tools

Synopsys IC Compiler 2, Prime Time tool

Challenges

- Timing reports on several APR flow stages were produced in order to make the required modifications to correct the violation and the outcomes of multiple timing paths are studied.
- To reduce output violations and shorten the run time, timing violations like false paths and multicycle paths were set using the tool commands.
- Using the reports produced for OCV, AOCV, MCMM and CRPR, the setup and hold violations were corrected.

B.E / B.Tech Academic Project

Dr. Ambedkar Institute of Technology

Multimedia Sentiment Analysis On Public Social Network Using NLP

Description

The major objective is to find hate speech on publicly social networks like Facebook, Twitter, etc. that may be reported and censored. The process was automated and conclusions were made based on significant amount of data.

Tools

Software Used : Python

Challenges

- 1. Gathering a sizable dataset and training it to produce correct results was the biggest obstacle. 2. It was impossible to perform it on real data since it requires lakhs of dataset and a powerful computer to run the calculations.