Hema Basavarajappa Gali

Personal Details

hemabgali@gmail.com

+91 8123749200

https://www.linkedin.com/in/hema-gali-053b8920b

Education Backround

Graduation
Bachelor of Engineering in Electronics and Communication in SKSVMACET, Lakshmeshwar
CGPA : 7.54
2018-2022

Intermediate
KLE Prerana PU College, Hubballi
Percentage : 77.7%
2016-2018

SSLC
Govt. Adarsha Vidyalya School Bidar
Percentage : 92%
2016

Career Objective

Aspiring for VLSI engineer role at an organization to utilize my skills that can contribute to the company's growth as well as enhance my knowledge by exploring new things in design and verification.

Professional Training

Advanced VLSI Design and Verification Course
Maven Silicon VLSI Design and Training Centre, Bangalore Sept 2022-till date

Technical Skills

VLSI Domain Skills

- **HDL**: Verilog
- **HVL**: System Verilog
- **Verification Methodologies**: Constraint Random Coverage Driven Verification
- **Digital Electronics**: Combinational & Sequential circuits, FSM, Memories, CMOS implementation.
- **Verilog Programming**: Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Synthesis issues, Races in simulation, pipelining RTL & TB Coding.
- **Advanced Verilog & Code Coverage**: Generate block, Continuous Procedural Assignments, Self-checking testbench, Automatic Tasks, Named Events and Stratified Event Queue, Code Coverage: Statement and branch coverage, Condition & Expression Coverage, Toggle & FSM Coverage.

Languages

- English
- Kannada
- Hindi

Behavioural Skills

- Team player
- Quick learner
- Good communication

Hobbies

- Drawing
- Painting
- Cooking
- Craft

Achievements

- Won the first prize in district level "Essay Competition".
- Secured third place in "Abacus Competition".

Verification Skills

System Verilog HVL

- Memories - Dynamic array, Queue, Associative array, Task & Function - Pass by reference
- Interface - Modport and clocking block.
- Basic and advanced object-oriented programming - Handle assignments, Copying the object contents, Inheritance, polymorphism, static properties and methods, virtual classes and parameterized classes.
- Constraint Randomization - constraint overriding and inheritance, Distribution and conditional constraints, Soft, static and inline constraints.
- Thread synchronization techniques - events, semaphores and Mailbox - built-in methods. Functional coverage - Cover groups, bins and cross-coverage, CRCDV and regression testing.

UVM

- UVM Objects & Components
- UVM Factory & overriding methods
- Stimulus Modelling
- UVM Phases
- UVM Configuration
- TLM
- UVM Sequence, virtual sequence & sequencer
- Introduction to RAL

Technical Project

Router 1x3 – RTL Design and Verification

HDL: Verilog
EDA Tools: Questasim and ISE
Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.
Responsibilities: Architected the block level structure for the design. Implemented RTL using Verilog HDL. Synthesized the design.

Cuk Converter

Description: Cuk converter is a type of DC\DC converter that has an output voltage magnitude that is either greater or less than the input voltage magnitude.

Responsibilities: Simulated the circuit of Cuk converter using simulink tool of matlab software and analysed the output.
Tools: MATLAB Simulink.

Declaration

I hereby declare that the information furnished above is true to the best of my knowledge and belief.

Date :

Hema Basavarajappa Gali

Place: Bidar, Karnataka, India