Dhanush S Gowda

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Career Objective

A physical design trainee to acquire advanced knowledge in my concern. Seeking a challenging career where my academic excellence will add value towards organization and personal.

Core Competancy

- Through understanding on ASIC flow and practical experience on APR flow that includes Floorplanning ,Powerplanning, placement ,CTS and Routing .
- Understanding in Various STA concepts such as Timing paths, Timing Arcs ,Slack, timing constraints, PVT corners, clock Skews, Fixing timing violations ,CRPR, AOCV.
- Developed a power network with no physical DRC errors and also made sure to meet the specified IR drop by varying the width ,Spacing and pitch of the metals.
- Developed an floorplan with contiguous core area, good utilization and required channel pacing with the help of flylines and data flow diagram.
- created a legalized placement block with minimal congestion, no DRC errors and no floating standard cells.
- Hands on experience on tools Synopsys IC compiler II , Synopsys Primetime.

Education Details

Advanced Diploma in ASIC Design **2025**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2021**

Don Bosco Institute Of Technology, with 7.76 CGPA

2017

Sri Chaitanya Pu College Nagarbhavi, with 77 %

SSLC **2015**

Shanti Dhama English Higher Primary School, with 79 %

Projects worked on

Accenture Client: Elevance Health

Associate Application Developer Jul-2022 to Dec-2022

Payroll Leave and absence

Description

Helped in developing payroll integrations using workday and Xml an Xslt. also analysed studio integrations

Tools

Workday, Workday Studio, Oxygen XML editor

Challenges

- Analysed studio integrations
- Got Certified in Workday HCM Course
- Got certified in Workday Integration

Domain Specific Project

RV-VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Oct-2022 to Feb-2023

Floorplan, Power plan and placement implementation

Description

Block level implementation of Lakshya subsystem: Technology 40nm, Supply Voltage 1.1V, Area 4.2 sq. mm, Power Budget-600nW, Max IR drop(VDD+VSS)-5%, No of standard cells 38403, No. of metal Layers 7

Tools

IC Compiler II Synopsys

Challenges

- Building Powerplan to maintain power network connectivity and IR Drop. Also ensuring that there were no missing vias, floating wire and power-ground DRC violations.
- Designing a Floorplan by determining Macroplacement as per the data flow diagram and using macro guidelines in order to achieve contagious core area and good utilization.
- Creating the placement block by inserting Pre placement cells, sufficient spaces in order to control the congestion and DRC violations obtained.

RV-VLSI AND EMBEDDDED SYSTEMS DESIGN CENTRE

Graduate Trainee Engineer Oct-2022 to Feb-2023

CTS & ROUTING Implementation

Description

Block level implementation of Lakshya subsystem:Technology-40nm ,supply voltage 1.1V, Area-4.2 sq. mm, Power budget-600nW, Max IR drop (VDD+VSS)-5%, No. of standard cells 38403, No. of metal layers 7.

Tools

IC Complier II- Synopsys

Challenges

- Analyzing clock tree to achieve minimum insertion delay and skew. Also checked rectified for the clock DRC errors.
- Analyzing and resolving the antenna violations by inserting the metal jumper and the diode into the layout .
- Performing clock tree synthesis and optimization using classic ,CCD flows and analyzing the tools behavior by comparing the timing reports in both the flows.

RV -VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Oct-2022 to Feb-2023

Analyzing the Timing Report by STA

Description

Generating of timing reports that include setup and hold slack calculations for flip flops and latch based paths working at various condition, reports and analyzed considering OCV, uncertainty CRPR, and timing exceptions (multicycle and flash paths).

Tools

Primetime by Synopsys, IC Compiler II -Synopsys

Challenges

- Understanding the primetime tool and commands related to the tool by analyzing their usage functionalities .
- Understanding the timing reports at every stage of PD flow, finding the cause of timing violations and how some of the violented paths are being reduced in later stages.
- Analyzing the effect of clock Skew, CRPR,OCV timing derates for all four different timing paths from the timing reports.

B.E / B.Tech Academic Project

Don Bosco Institute Of Technology

Autonomous robot navigation using LIDAR

Description

This project is all about autonomous ground vehicle with lidar mounted on it This vehicle maps the environment it is placed and navigates on its own to the destination by avoiding obstacle with the help of path planning and navigation module

Tools

RPLIDAR A1 360, Robotic operating system, Arduino UNO, RPI 3, DC motors, Python.

Challenges

- Inaccurate Path planning so had to optimize it using better algorithms.