

Geetha Rani Kadavakollu (Design Verification Engineer)



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PM Palem, Visakhapatnam, Andhra Pradesh. Pin - 530041

Name	Geetha Rani Kadavakollu
Designation/Role	Design Verification Engineer
Total Experience	9 months
Highest Education	B. Tech in Electronics & Communication Engineering
Key Skill Set	Languages : System Verilog, Verilog Tools : Xilinx Vivado, EDA Operating Systems: Unix OS Methodologies :UVM

Employment History

Role/designation	Employer	Duration	Years, Months
Verification Engineer	Cerium Systems	june 2022 to Till date	9 months

Profile Summary

- Having 9 months of experience in verification with the key skills of SV/Verilog.
- Strong knowledge in digital electronics and Digital System Design.
- Basic knowledge on Linux Commands.

PROJECTS

❖ ASYNCHRONOUS FIFO

We designed an Asynchronous FIFO of 16-bit depth and each data entry having width of 32-bit using Verilog in EDA Playground.

❖ DESIGN VERIFICATION OF ETHERNET PROTOCOL.

Started referring to ETHERNET protocol. Understand the testbench flow. setting up regressions and debugging the errors.

❖ UVM TEST BENCH FOR AHB LITE TO APB BRIDGE MODULE.

This Project is to verify the AHBlite2APB Bridge Module using UVM Testbench.

❖ UVM TEST BENCH FOR I2C PROTOCOL.

This Project is to verify the I2C Module using UVM Testbench.

Academic Profile

Degree	School/College/Institute	Board/University	CGPA/ Marks	Year of passing
B.Tech (Electronics Engineering)	Rajiv Gandhi University of Knowledge & Technologies, Nuzvid	RGUKT, Nuzvid	8.25	2022
12th	Rajiv Gandhi University of Knowledge & Technologies,Nuzvid	State Board	8.38	2018
10 th	ZP High School, Bhavadevarapalli.	State Board	9.8	2016

Personal Information:

DOB - 15-05-2001

Marital Status - Unmarried

Citizenship – Indian

DECLARATION: I do hereby declare that above particulars of information and facts stated are true, correct and complete to the best of my knowledge and belief.

Place: Visakhapatnam

Date: 01-03-2001

Signature: K.Geetha Rani