Vennela Raja Kuraganti

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CAREER OBJECTIVE

Seeking a position to utilize my skills and abilities in the field of VLSI Design and Verification offers professional growth while being sincere, resourceful, innovative and flexible.

EDUCATION

- M.tech (P.E) from CEC Chirala,(JNTUK) with 71.14% in the year 2018-2021
- B.tech (E.E.E) from CEC Chirala,(JNTUK) with 69.53% in the year 2013-2017
- Intermediate (M.P.C) from VBJC Chirala, with 85.00% in the year 2011-2013
- SSC from Board of Secondary Education, with 80.00% in the year 2010-2011

PROFESSIONAL SUMMARY

- Good knowledge on design verification using Verilog, System Verilog, UVM.
- Development, System Verilog Assertions, Code coverage and functional coverage.
- Exposure to different aspects of verification – including features listing, test plan development, test case
- Good knowledge on AMBA protocols - APB, AHB & AXI .
- Exposure to Verification of 10 GB Ethernet MAC IP core - specification, features listing, test-plan, and testcase.

TECHNICAL SKILLS

- HDL Known : Verilog programming
- HDVL Known : System verilog.
- Methodology : UVM
- Software Tools: EDA-playground, model-sim, Questa-sim, xilinx.
- Operating Systems : LINUX, windows.

ACADEMIC PROJECTS

- **MC-UPQC (Multiconverter Unified Power-Quality Conditioning System) –** [b.tech -2017]
  The aim of the MC-UPQC is to regulate the load voltage against sag/swell, interruption, and disturbances in the system to protect the Non-Linear/sensitive load. By using MC-UPQC results Improvement in Power Quality.
  Software : MATLAB

- **MIC BASED PV SYSTEM FOR STANDALONE AND MICRO GRID APPLICATIONS CONSIDERING VARIABLE IRRADIANCE AND TEMPERATURE –** [M.TECH - 2020]
  Software : MATLAB

SELF PROJECTS

1. Verification of 10 GB Ethernet MAC IP core

Description: The Ethernet IP core connects AXI interface on one side and Ethernet MAC interface on the other side. It is responsible for transmitting and receiving data frames. It can operate in Half or Full- Duplex Mode and is based on Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. MAC module performs several tasks such as CRC generation and checking, Pad generation, Generation of status signals.

Responsibilities:

- Understood – ethernet spec.
- Implemented the scenarios for different mode soft data transfer.
- Created the test cases to check the various interrupt conditions.
- Developed the test cases to verify all supported packet-based data transfers.
- Verified DUT with different test scenarios like data path, length-data mismatch.

2. Verification of Ethernet 10/100M IP

Description: 10/100M Ethernet-FIFO convertor IP core is an interface in charge of data conversion between the raw MAC frame and bit stream from one to the other. It works in full duplex mode. The bit stream's data rate depends on the input ff_clk's frequency. This convertor is used in a project to connect the GSM modulator/demodulator with PC. So the data form is conformed to the GSM standard. However, the structure of verilog code is very clear and easy to understand so that can be easily changed to be used in other situations.

Responsibilities:

- Understood the spec.
- Implemented the scenarios for different mode soft data transfer.
- Created the test cases to check the various interrupt conditions.
- Developed the test cases to verify all supported packet-based data transfers.

3. Verification IP Development for AXI Protocol

Description:The Advanced Extensible interface (AXI 4.0) is a part of the ARM Advanced Microcontroller Bus Architecture (AMBA) family. It supports high-performance, high-frequency system designs which isbackward-compatible with existing AHB and APB interfaces.

Responsibilities:

- Understood the AXI protocol Specification.
- Prepared the Verification Plan.
- UVM based testbench for Single master and Single Slave VIP
- Burst Mode Supported for Increment, Wrap and Fixed.
- Aligned and unaligned Data transfer supports.
- Backward compatible with AXI3.0.

ACTIVITIES

- **Actively participate** in NSS camps and events & Drawing competitions.
- Got Appreciations from my professors for giving Best Informative **Seminars**.
- Organizing events or activities & conducting conferences in our own TRUST.
- **Volunteer** participate in social, environmental groups & fundraising.

STRENGHTS

- Self-motivation and ability to take the initiative.
- Ability to work well under pressure.
- Quick learner, keen to learn and improves skills.
- Analyzation & Logical thinking.

HOBBIES & INTEREST

Drawing, photography.

PERSONAL INFORMATION

Date of Birth	3rd Jan 1996
Father	Madhusudhana Rao
Mother	K. Naga Siromani
Gender	male
languages	Telugu , English.

DECLARATION

I hereby declare that the information furnished above is true to the best of my Knowledge and belief.

K. Vennela Raja