Jagadish
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Contact No: +91-9731443756

Career Objective:

To be a part of organization that gives a scope to enhance my knowledge and utilizing my skills towards the growth of organization.

Professional Experience:

- Completed Physical Design Course from Takshila Institute of VLSI technologies in 6 months.
- Good Understanding of block level Physical design and verification concepts like **Floor planning, CTS, STA, DRC/LVS, DFM etc.**
- Practical exposure to Physical Design tools from **IC Compiler** tools.

Technical Skills:

- Strong understanding in the RTL to GDSII flow or design implementation.
- Good in concepts related to synthesis, place and route, CTS .
- Good knowledge and experience in Block-level Floor-planning and Physical verification.
- Working experience with tools like ICC.
- Strong knowledge in standard place and route flows ICC/Synopsys flows preferred.
- Well versed with timing constraints and STA.
- Good knowledge of Windows 7, 8 and Linux.

Academic Qualification:

Qualification	Name of Institution	Year of Passing	Percentage/ CGPA
B.Tech (ECE)	Shree Devi Institute of Technology, Mangalore Karnataka.	2022	**7.05 cgpa**
XII	Government PU College, Karkala Karnataka.	2018	**56%**
X	Jyothi High School Ajekar, Karkala	2016	**68 %**

Certifications:

- **Takshila Institute of VLSI Technologies Title:** Professional Training on Physical Design.

Project Worked On:

Title	**ORCA_TOP**
Tool used	IC Compiler
Description	• Technology: 32nm • No. of macros: 40 • Layer: 9 • Std. cell count: 56013 • No. of Clocks: 7 • Frequency: 416MHz
Responsibilities	Iterative Floorplan, IO ports placement, Power planning, Placement and CTS reviews, Routing and DRC checks.

Title	**ORCA_TOP_IO**
Tool used	IC Compiler
Description	Technology: 28nm No. of macros: 30 Layer: 9 Std. cell count: 50000 No. of Clocks: 7 Frequency: 400MHz
Responsibilities	Iterative Floor planning and Power-planning Placement and CTS optimization Physical Verification and manual optimization Timing Closure and ECO

Academic Project:

UVM Based Verification of CAN Protocol Controller Using System Verilog.

- CAN protocol is extensively used in Automotive Industry
- Helps in communicating between various ECU's Using Differential bus
- CAN is message based protocol.
- CAN bus is of Broadcast type.
- Message prioritization feature through identifier selection.

Personal Profile:

Date of Birth	:	20th June 2000
Languages Known	:	Kannada, English, and Hindi
Permanent Address	:	1-127 Neerkhana House Vagga, Kadabettu Post, Bantwal TQ Dakshina Kannada

Declaration:

I hereby declare that I would be glad to come for interview at any time that is convenient to you and assure you of my devoted service.

Date: **Jagadish**

Place: