Manish Chintala

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Career Objective

To obtain a career in VLSI Industry as a Physical Design Engineer, where I can contribute my skills for organization's success and improving my technical ability while being resourceful, innovative and flexible.

Core Competancy

- Good understanding on ASIC flow (RTL to GDSII).
- Designed a block level PnR flow, hands on experience on Floorplanning, Powerplanning, Placement, Clock tree synthesis, Routing.
- Knowledge on Static Timing Analysis concepts such as Timing paths, Setup and Hold timing, Clock skew, Timing arcs.
- Created a power ground network with no DRC errors with respect to the specified IR drop.
- Developed a floorplan with contiguous core region and provided channel spacing with the help of flylines and data flow diagram.
- Created a legalized placement block with minimal congestion, no floating standard cells.
- Generated timing reports at every stage of PnR flow and analyzed the WNS, TNS, and Delays.
- Hands on experience on Synopsys IC Compiler II, Synopsis Prime Time.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Teegala Krishna Reddy College of Engineering and Technology, with 7.20 CGPA

2018

Narayana Jr College, with 77 %

SSLC **2016**

Kakatiya High School, with 8.3 %

Domain Specific Project

RV-VLSI DESIGN CENTER

Graduate Trainee Engineer Sep-2022 to Jan-2023

Block level implementation of PnR

Description

Performed physical integration of block level PnR flow in 40nm technology to achieve power, performance and area along with the given constraints.

Tools

Synopsys IC Compiler II

Challenges

- Placement of macros according to the connectivity information in the core area.
- Creating an efficient power mesh within the IR drop limit.
- Understanding the clock tree synthesis to achieve minimal insertion delay and skew.
- Used various techniques to fix timing violations for critical blocks.

RV-VLSI DESIGN CENTER

Graduate Trainee Engineer Sep-2022 to Oct-2022

STA for various Timing Paths

Description

Validating the timing performance of a design by analyzing setup and hold timing reports for flip-flop and latch based design by considering uncertainty, CRPR, and dealing with timing exceptions such as false paths, multicycle paths.

Tools

Synopsys Prime Time

Challenges

- Analyzing setup and hold timing reports with waveforms.
- Analyzing the effect of clock insertion, OCV derates for various timing paths by understanding the timing reports.
- Identifying the violations based on timing exceptions such as multicycle and false paths.

B.E / B.Tech Academic Project

Teegala Krishna Reddy College of Engineering and Technology

Android military spying and bomb disposal robot

Description

This innovative system is made for operations which involve high risk for humans to enter, especially for some criminal case and may prove very beneficial for military area for spying purposes.

Tools

Keil micro, uc flash, proteus, Arduino, Ultrasonic and proximity sensor, L293D, LCD display

Challenges

- Implementation of Wireless sensor network ,processing the received input and providing the output signal for appropriate task.