PRAMODH H R

Contact No : +919141464819

Email id : pramodhhr2001@gmail.com

Objective

Willing to work in a challenging position with a growing organization, where I can utilize my technical, analytical and interpersonal skills to serve the organization.

Personal info

Address : Hodike hosahalli , channapatna (taluk) , ramanagar(district). pin code 562138

Gender :Male

Date of birth: 11-11-2001

Hobbies : swimming , cooking , travel, repair electronic gadgets , electronic device working analysis .

Language

English ●●●●○

Kannada ●●●●○

Technical skills

- C language ●●○○○
- Python ●●●●○
- Verilog HDL ●●●○○
- Cadence virtuoso ●●○○○
- physical design ●●○○○

Interpersonal skills

- Time management ●●●●○
- Problem solving ●●●●○
- Communication ●●●○○
- Creativity ●●●●○
- Leadership ●●●○○
- Quick learner ●●●●○

Packages and Operating Environment Familiarity:

- Windows , linux
- MATLAB , Xilinx ISE , Kiel microvision,
- pycharm ,anaconda
- Cadence Virtuoso ,NC launch, genus, innovus
- Arduino IDE and Multisim.

Education

Don Bosco Institute of Technology , Bangalore

Visvesvaraya Technological University **CGPA : 9.04**

Bachelor of engineering

Electronic and communication engineering | 2019- 2023

Concorde Mahesh Pre University College ,Mandya

Department Of Pre-University Education **Percentage - 74.83 %**

2nd pre university | 2018- 2019

Govt Adharsha Vidhyalaya (RMSA) , Mattikere

Board of Secondary Education **Percentage - 88.64 %**

10th standard | 2016 -2017

Workshops/Seminars

- Attended " **Leading Edge VLSI Physical Design using Modern Tools** " , 5 days FDP program , introduction to virtuoso , NC launch, genus , innovus , tempus , with hands on experience , held at S J B Institute of Technology, Bangalore.
- Attended a short term course by NATIONAL INSTITUTE OF TECHNOLOGY DELHI on "**Latest Trends in VLSI Devices, Circuits and Tools**" Organized by the Department of Electronics and Communication Engineering

Technical Experience

- **MINI PROJECT** : " design of 12 bit DAC using CMOS " , (analog) . where we have designed op-amp and R-2R ladder structure for 12 bit DAC design , simulated the design and obtained the power and delay value for the design using virtuoso .
- **PROJECT** : "Multiplier's comparision and its physical design " ,(ongoing) where we started with comparision of 4 multipliers in terms of power and area . that are booth ,vedhic ,dabba and russian peasent multiplier simulation using NC launch . area , timing , and power analysis using genus tool . Floorplan , physical design using innovus tool .
- **INTERNSHIP** : " VLSI design" , at R &D department of Don Boscho Institute of Technology . 4 week internship . introduction to virtuoso, NC launch , genus , innovus . With both analog and digital design methodology and understanding the need of EDA tool in physical design . with this during internship period we designed " 16 bit Vedic multiplier " , (digital) simulation using NC launch .area timing , and power analysis using genus tool . Floorplan , physical design using innovus tool .and done a comparision with other multipliers interms of power area delay parameter .
- **COURSE** : " VLSI Physical design " NPTEL course and got elite certificate in this course they coverd all the basic concepts of physical design , with florplan ,layout, routing , design methodology