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Career Objective

Aspiring to work as a SOC Physical Design engineer and utilize my skills with potential and contribute to company's growth.

Core Competancy

- Thorough understanding on ASIC flow and hands-on experience on APR flow that includes floorplanning, powerplanning, placement, routing(PnR) and CTS.
- Well-versed in various STA concepts such as Timing path, Arcs, slack, Timing Constraints, PVT corners, modes, skwes, Timing voilations,CRPR, OCV and AOCV.
- Having a technical exposure on DRC, LEC, ERC, LVS, SI analysyis, IR drop analysis, Timing closures ,Antenna violations using jumper and diodes.
- Hands on experience on EDA tools synopsys ICC-II compilier, Prime time, IC validator design compiler and star RC/XT.
- Good knowledge of digital Elctronics and logic designs.
- Working with the LINUX environment.
- Basic understanding of verilog HDL programming language and RTL designing.
- Good understanding in CMOS and MOSFET concepts.
- Valueable knowledge of TCL,Perl, shell and modifying of TCL scripts.
- Good knowledge of VLSI design flow - ASIC design flow (RTL to GDSII).

Education Details

Advanced Diploma in ASIC Design **2023**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**
Institute of engineering & science, IPS Academy, Indore, with 7.96 CGPA

2016
R.N.Y Inter College, Siwan, with 55 %

SSLC **2014**
C B H/S Ushari Dhanauti, Siwan, with 58 %

Domain Specific Project

RV-VLSI and Embedded Systems Design Center.

Graduate Trainee Engineer Aug-2022 to Feb-2023

Lakshya 40nm SOC Technology Subsystem.

Description

Technology-40nm, Supply voltage-1.1V,Area-4.2 sq. mm, Power budget-600mW, Frequency of operation-833MHz Max. IR drop (VDD+VSS)-5% , No. of Macros-34, No. of Standard cells-38887,No. of Metal layers-7, No. of Clocks-5.

Tools

PrimeTime, IC Compiler II - Synopsys

Challenges

- Designing a Floorplan by determining macro placement as per dataflow diagram, flylines and using the macro guidelines in order to achieve contiguous core area and good utilization.
- Building a Powerplan to maintain power network connectivity and IR drop. Also ensuring that there were no missing vias, floating wires and power-ground DRC violations .
- Creating a placement block by inserting pre-placement cells, placement constraints, sufficient spacings in order to control the congestion and DRC violations obtained.
- Rectifying the LVS errors like shorts which were obtained post routing by removing the overlapped routes and doing manual routing wherever necessary.

B.E / B.Tech Academic Project

Institute of engineering & science, IPS Academy, Indore

IoT based smart parking systems.

Description

Parking users will be able easily to find empty parking spots, saving time and fuel.They will have a lot of payment options to choose from. Parking users will not wait on queues entering or leaving the parking spot, because the system will be ticket.

Tools

RFID, IR Sensor, Servo Motor SG90, Node MCU-8266, Arduino IDE, Blynk Platform.

Challenges

- Cities must turn into gentle, smart and efficient places and evolve to become Smart Cities. Regarding mobility it should imply: Improve infrastructures and public transport flow.Availability if dynamic systems to guide the traffic towards its .