2023

## Aswin

### Objective

To be associated with an organization that provides career development opportunities and an environment to enable me to contribute in its growth with hard work and dedication

#### Education

### VLSIGURU Institute

VLSI (Physical design) -

#### A.V.L higher secondary school 2015-2016

SSLC - 74 %

#### Bharathi higher secondary school 2016-2018

HSC - 62%

#### S.A engineering college 2018-2022

B.E electronics and communication engineering - 80%

#### Skills

#### TOOLS AND LANGUAGES:

EDA Tools: synopsys ICC2 compiler

Programming language : C Scripting language : TCL

TECHNICAL SKILLS: \* Familiar with ASIC flow (netlist to

GDSII) Hands on experience in Floor Planning, Power Planning, Placement, CTS, Routing, STA and sign off

analysis. Have knowledge on Digital electronics, and CMOS design, & IC fabrication.

# ACADEMIC PROJECT

PROJECT TITLE: "PD ORCATOP MULTI VOLTAGE DESIGN"

TECHNOLOGY: 32nm HARD MACROS: 40 FREQUENCY:450Mhz

CLOCKS:4

TOOLS USED: synopsys ICC2 compiler

#### **ROLES & RESPONSIBILITY:**

block level physical design

Block level Floorplanning, Powerplanning, Decap insertion, Placement driven synthesis, global routing, Post placement, Timing closure, Clock tree synthesis, closk wiring, post clock timing closure, clock slew fixing, late mode and early mode optimization, timing driven and si driven routing, post route

timing fixing, Fixing DRC's

#### PROJECT 2

PROJECT TITLE: "VALCANO DESIGN"

TECHNOLOGY: 32nm HARD MACROS: 40 FREQUENCY:450Mhz

CLOCKS:4

TOOLS USED: synopsys ICC2 compiler

ROLES & RESPONSIBILITY: block level physical design

Block level Floorplanning, Powerplanning, Decap insertion, Placement driven synthesis, global routing, Post placement, Timing closure, Clock tree synthesis, closk wiring, post clock timing closure, clock slew fixing, late mode and early mode optimization, timing driven and si driven routing, post route timing fixing, Fixing DRC's

# Interpersonal skills

Good team player. Ability to balance and tackle any kind of situation.

## PERSONAL

FATHERS NAME k.subramani

DOB: 14/10/2000

LANGUAGE: Tamil,telugu,english

GENDER: Male

AGE: 22

## DECLARATION

I hereby declare that the above information are true to the best of my knowledge and own belief.