SUNKA PRASAD
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Summary:

- Good knowledge on System Verilog and UVM methodology.
- Worked on high-speed bus protocols like APB, AHB and AXI.
- Familiar with different aspects of VIP development, creating Test plan, write Test cases, Functional Coverage, Code coverage and regression.
- Experience in developing TB &TB components for block level
- Good coding skills for Verification and hands on with QuestaSim tool used in Verification and waveform-based debugging tools.
- Good Debugging skills.

Experience:

Designation	Organization	Duration
Verification Engineer	Softnautics	June 2022 – Feb 2023
Verification trainee	Maven Silicon Training Centre	Dec 2021 – May 2022

Academic Qualification:

Degree Name	College/University Name	Year	Percentage
B.Tech in Electronics and Communication Engineering	Gurunanak Institute of Technical Campus, Hyderabad	**2021**	**73.4%**
Diploma.(Electronics & Communication)	Govt. Institute of Electronics, Hyderabad	**2017**	**80.2%**
Secondary School Certificate(SSC)	Zilla Praja Parishath Secondary High School	**2014**	**93.0%**

Technical Skills:

• HDL/HVL	Verilog, System Verilog
• Verification Methodology	UVM
• Protocol Knowledge	PCIe,I2C,AHB, APB & AXI
• EDA Tools	Mentor Questa, ModelSim, Quartus Prime and vivado
• Scripting Knowledge	Perl ,Python,Linux and Unix

Projects Profile:

Project	Description
AHB to APB Bridge IP Core Verification **Role :** Verification using UVM	**Project Description:** An AHB to APB Bridge is an AHB slave which works as an interface between the high performance AHB bus and low performance APB bus. **Responsibilities** : As part of verification, • Understood AHB to APB Bridge Verification architecture document. • Architected the class based verification environment. • Defined Verification Plan • Verified the RTL module with UVM Test Bench with different test scenarios like single READ, WRITE, and Burst READ, WRITE with different burst lengths • Generated code coverage and functional coverage report for RTL Verification signoff Documented all Verification efforts
PROJECT DETAILS: (softnautics) **I2C SOFT IP - Verification Role :** Verification usingUVM	• • **I2C Soft IP Verification** • Understood IP Specification. • Developed test plan, testcases for coverage driven verification. • Verified the DUT with UVM Testbench with different constrained random test scenarios. • Found few RTL issues related to I2c master and slave. • Debugged the test cases failures and worked with designer to fix. • As a part of project python scripting was used to make environmental based logics simpler