#### Pallavi B H

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#### **Career Objective:**

To be a part of organization that gives a scope to enhance my knowledge and utilizing my skills towards the growth of organization.

## **Professional Experience:**

- Completed Physical Design Course from Takshila Institute of VLSI technologies in 6 months.
- Good Understanding of block level Physical design and verification concepts like Floor planning, CTS, STA, DRC/LVS, DFM etc.
- Practical exposure to Physical Design tools from IC Compiler tools.

#### **Technical Skills:**

- Strong understanding in the RTL to GDSII flow or design implementation.
- Good in concepts related to synthesis, place and route, CTS.
- Good knowledge and experience in Block-level Floor-planning and Physical verification.
- Working experience with tools like ICC.
- Strong knowledge in standard place and route flows ICC/Synopsys flows preferred.
- Well versed with timing constraints and STA.
- Good knowledge of Windows 7, 8 and Linux.

## **Academic Qualification:**

Qualification	Name of Institution	Year of Passing	Percentage/ CGPA
B.E (ECE)	Government Engineering College, k r pete	2022	7.95
Diploma	Government Polytechnic, k r pete	2019	86.54%
X11	Government Independent PU College , C R Patna	2016	62%
X	Shree Sharada high school , Byadarahalli	2014	80.80%

#### **Certifications:**

• Takshila Institute of VLSI Technologies

**Title:** Professional Training on Physical Design.

## **Project Worked on:**

Title	ORCA_TOP	
Tool used	IC Compiler	
Description	<ul> <li>Technology: 32nm</li> <li>No. of macros: 40</li> <li>Layer: 9</li> <li>Std. cell count: 56013</li> <li>No. of Clocks: 7</li> <li>Frequency: 416MHz</li> </ul>	
Responsibilities	Iterative Floorplan, IO ports placement, Power planning, Placement and CTS reviews, Routing and DRC checks.	

Title	ORCA_TOP_IO	
Tool used	IC Compiler	
Description	<ul> <li>Technology: 28nm</li> <li>No. of macros: 30</li> <li>Layer: 9</li> <li>Std. cell count: 50000</li> <li>No. of Clocks: 7</li> <li>Frequency: 400MHz</li> </ul>	
Responsibilities	Iterative Floor planning and Power-planning Placement and CTS optimization Physical Verification and manual optimization Timing Closure and ECO	

# **Academic Project:**

HUMAN ACTIVITY RECOGNITION USING MACHINE LEARNING: - it is used to identify the human activity like walking, dancing, yoga, driving etc.

## **Personal Profile:**

Date of Birth : 14 May 1999
Languages Known : English, Kannada

Permanent Address: Pallavi B H

D\O Huchegowda

Byadarahalli(V&P), C.R Patna(T), Hassan(D)-573111

## **Declaration:**

I hereby declare that I would be glad to come for interview at any time that is convenient to you and assure you of my devoted services.

Date: Pallavi B H

**Place: Bangalore**