Taha Perwaiz

Physical Design Engineer

+91-8368200359 | perwaizt@gmail.com | December 2nd, 1997 | linkedin.com/in/taha-perwaiz-902075189

Personal Profile

Highly motivated and results-driven SoC Design Engineer with experience in GPU design. Pursuing M.Tech in VLSI Design from VIT Vellore and set to complete in May 2023. Seeking a challenging role in the field of SoC design where I can utilize my skills and knowledge to make a meaningful contribution. Currently intern at Intel for 7 months with experience specialising in RTL to GDSII flow, Static Timing Analysis, Scripting and Synopsis tools. Primarily, looking for ASIC Design/Physical Design/Digital Design roles.

Education

Vellore Institute Of Technology *Vellore, Tamil Nadu*
VLSI Design - 8.3 CGPA *Current*

Jamia Millia Islamia *New Delhi, India*
BTech in Electronics and Commmunication - 9.93 SGPA *2021*

Chinmaya Vidyalaya *Jharkhand, India*
CBSE Class XII - 88.2% *2016*

Work Experience

Intel Technology *Bangalore, India*
Soc Design Intern *Sept 2022 - Current*

- Running complete RTL to GDSII implementation for large partition(s) meeting design goals.
- Worked rigorously under project lead for power optimization of multiple partitions through different recipes and floorplans.
- Collaborated with a four-person team to develop a model that could reduce the manual process and huge effort for timing classification.
- Automated and optimised the data extraction process, working with shell scripting, and employed other Linux tools.
- Other areas where I worked includes FC/SS Physical Verification, Unix, Scripting, etc.

University Projects

Implemented 16 bit RISC processor in Verilog *Vellore, Tamil Nadu*
Vellore Institute Of Technology *Feb 2022 - Apr 2022*

- Implemented RISC processor containing ALU, Shifter and Barrel Shifter as operational blocks. Data inputs were taken up randomly by creating lookup table.
- The project was carried on ModelSim(Mentor Graphics)

Comparison Of Dadda Multiplier and Wallace Tree Multiplier in Tanner EDA *Vellore, Tamil Nadu*
Vellore Institute Of Technology *Nov 2021 - Dec 2021*

- Circuit was made for both the Dadda and the Wallace Tree Multiplier and a comparison for the Power and Delay was made.

Output Characteristics Of NMOS and PMOS in Cadence Virtuoso *Vellore, Tamil Nadu*
Vellore Institute Of Technology *Nov 2021 - Dec 2021*

- The circuit for NMOS and PMOS was made and the Id vs Vgs with varying Vsb and Id vs Vds with varying Vgs was plotted.

Skills

Programming	Verilog, Perl, TcL, Python, C/C++., SV
Miscellaneous	Linux, Shell, Fusion Compiler, ICC/ICC2, PrimeTime,Tanner EDA Tool, Intel Quartus Prime, Microsoft Office.
Soft Skills	Time Management, Teamwork, Problem-solving, Documentation, Engaging Presentation.

Achievements

2022	Recieved cash prize for securing 2nd place in Inter VIT FPGA Hackathon.
2021	Qualified GATE 2021 in Electronics and Communications Engineering (AIR 2345)
2020	Received Scholarship for three consecutive years from 2017-2020 for Academic Excellence in B.Tech for securing Rank 2 in ECE Batch for three consecutive years.