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Career Objective

Seeking a challenging position in an organization to utilize my technical expertise and interposonal skills thereby contributing organizational business goals and for self-development..

Core Competancy

- Hands of experience on IC COMPILER involving FLOORPLAN and POWERPLANNING, PLACEMENT,CLOCKTREE SYNTHESIS and ROUTING.
- Worked on creating a Floorplan according to the macro placement guidelines with good contiguos area and acceptable congestion between the macros .
- Understanding Clock Tree Synthesis , types of clocktrees, Non default routing rules for clock routing.
- Good Knowledge on ASIC FLOW (RTL TO GDS) , Digital electronics, circuit analysis, basics of MOSFET theory
- Hands of experience on PRIME TIME for STATIC TIMING ANALYSIS and timing closure at block level by analysing the timing reports at multiple scenarios.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**
Sai Vidya Institute Of Technology, with 6.95 CGPA

2017
Yogananda Junior College, with 91.9 %

SSLC **2015**
Keshava Reddy EM High School, with 88 %

Domain Specific Project

RV VLSI and Embedded systems design center

Graduate Trainee Engineer Aug-2022 to Feb-2023

Implementation of ASIc block level design

Description

FLOOR PLAN and POWER PLAN Technology-40 nm,macro count- 34,supply 1.1V,Power budget 600wv , Number of metal layers -7

Tools

Synopsis IC compiler 2

Challenges

- manually placing hard macros using data floor diagram such way that to provide the maximum Core area and to make all pins of the macros are accessible.
- Implementing the Power plan to meet the target IR drop and made power mesh DRC clean.
- Maintaining the uniform orientation of hard macros and adding placement and routing blockages.

RV VLSI and Embedded systems design center

Graduate Trainee Engineer Aug-2022 to Feb-2023

Implementation of ASIC block level design

Description

PlACEMENT and CLOCK TREE SYNTHESIS Timing driven and conjunction aware standard cell placement in non-SPG flow is being done with optimum core utilisation.

Tools

Synopsis IC complier 2

Challenges

- Performed timing driven and conjunction driven placement and HFNS in order to minimize logical DRC by this improving timing QoR.
- Performed sanity check before and after each stage of physical design flow.
- Synthesising clock tree by providing NDR rules .

RV VLSI and Embedded systems design center

Graduate Trainee Engineer Aug-2022 to Feb-2023

Implementation of ASIC block level design

Description

Routing and DFM routing all standard cell pins and hard macros pins using metal layers, performing via optimization and post route optimization.

Tools

Synopsis IC complier 2

Challenges

- Fixing antenna vailotions using metal hopping and antenna diodes manually .
- Clearing alla DRC vialotions and LVS vialotions in order to make sure that design can be manufacturable.
- Analysing timing reports and other reports in each stage .

B.E / B.Tech Academic Project

Sai Vidya Institute Of Technology

Universal Tracking System

Description

Used for the wide purposes such as tracking,navigation and traffic management, To implement a data logging system on cloud, which can be used for telemetry..To show how systems can be combined for the purpose of telemetry. Install of mobile app.

Tools

Arduino I D E, C++ , Mobile APP(Blynk), / Node MCU (ESP8266) microcontroller, GPS&GSM modern, Motion Sensor(ADXL335), Buzzer,

Challenges

- To get the exact coordinates for tracking the device, Developing the program of using microcontroller,