TANVI MADARE

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ABOUT:

Looking for a challenging position in an organization, where I can utilize my knowledge and skills by contributing effectively towards the growth of the organization.

EXPERIENCE:

INTERN – Physical Design Engineer
Apex Semiconductor
Bangalore
(Sep 2022 – June 2023)

EDUCATION:

Master of Technology (VLSI)
VIT University
(2021-2023)

- CGPA: 8.2
- Main subjects: Digital IC Design, Digital Design with FPGA, ASIC Design, Design for testability.

Bachelor of Engineering (Electronics Engineering)
Yeshwantrao Chavhan college of Engineering Nagpur, Maharashtra
(2017 – 2021)
CGPA: 7.91

Higher Secondary Certificate (MH state board)
St. Paul Junior College Nagpur
(2016)
Marks: 72.22%

Secondary School Certificate (MH state board)
(2014)
Marks: 90.4%

TECHNICAL SKILLS:

- Tools: Cadence Virtuoso, Xilinx ISE
- Hardware Description Language: Verilog
- Operating Systems: Windows, Linux

PROJECTS:

- **VLSI Implementation of Convolutional Layer for CNN**
  Description: Designing Convolutional Layer using Verilog HDL. Efficient VLSI Implementation of CNN which includes Convolution, Maxpooling and ReLU layer. For Designing Convolutional Layer, Different adders are used and their area, power and delay are compared in order to define efficiency.

- **Design and Implementation of Single Precision Floating Point ALU using Verilog HDL**
  Description: Designing of Single Precision Floating Point ALU which can perform addition, Subtractions, Multiplication and Division Operations.