Name : Tarak Sai Kumar Gandham
E-mail : taraksai624@gmail.com
Mobile : +91 6301261163 www.se-minds.com

OBJECTIVE:

Seeking a responsible position as an entry level Physical Design Engineer which enables to bring the best out of my knowledge and experience in achieving organizational goals and personal growth.

PROFESSIONAL TRAINING:

An Industry Oriented Trainee in **VLSI ASIC PHYSICAL DESIGN** from **Se-minds Pvt. Ltd.**, Hyderabad from **August 2022 to January 2023.**

COURSE OUTLINE:

Basic Electronics, Digital fundamental concepts, MOSFET, CMOS design concepts, layout concepts, stick diagrams, fabrication, Basics of STA, Logic Synthesis fundamentals. Physical Design concepts: floor planning, PG planning, Low Power design techniques, CTS, Routing techniques, signal integrity. Advanced STA, vi editors, Basics of Unix.

TOOLS USED:

Experience in physical design of 90nm and 45nm technologies using Cadence tool

- Cadence Innovus : Place and Route
- Cadence Genus : Logic Synthesis

PROJECTS:

Project -1: Place and Route (Top level)

Design Name	: asic_entity
Objective	: Timing Driven layout.
Tools Used	: Cadence Innovus
Area	: 32187187.5 μm^2
Macros/Instance	: 29/53642
No. of Clocks	: 08
Frequency	: 125Mhz
Technology/Layers	: 90nm/9 Metal Layers

Role : Performing Audit checks, Floor plan, Placement, Trail route, Timing Analysis, CTS, Detailed Routing, Post Route Optimization, Sign Off Checks, Achieved 0% Congestion at Trail Route Stage.

Project -2: Place and Route (Block level)

Design Name	: eVITERBI_322
Objective	: To Observe I/O Pins Placement & Fixing DRV's & DRC's
Tools Used	: Innovus
Area	: 435.024 μm^2
Macros/Instances	: 0/113
No. of Clocks	: 01
Frequency	: 250Mhz
Technology/Layers	: 45nm/7 Metal Layers

Role: Performing Audit checks, performing normal PNR flow and done with foundation flow, Floor plan, Placement, Trail route, Timing Analysis, CTS, Detailed Routing, Post Route Optimization.

Name : Tarak Sai Kumar Gandham
E-mail : taraksai624@gmail.com
Mobile : +91 6301261163 www.se-minds.com

Project -3: Place and Route (Block level)

Design Name	: usb_wrapper
Objective	: To Meet Setup & Hold time, Fixing DRV's & DRC's
Tools Used	: Innovus
Area	: 1534651.6 μm^2
Macros/Instances	: 12/26956
No. of Clocks	: 17
Frequency	: 250Mhz
Technology/Layers	: 90nm/5 Metal Layers

Role: Performing Audit checks, performing normal PNR flow and done with foundation flow, Design Import, Floor plan, Placement, Trail route, Congestion Analysis, Timing Analysis, CTS, Detailed Routing, Post Route Optimization, Fixing Shorts & Opens.

Project -4: Logic Synthesis

Objective	: Perform ZWLM Synthesis & Obtained optimized Gate Level Netlist.
Tools Used	: Cadence Genus
Instances /Area	: 4131 / 236718 μm^2
No. of Clocks	: 07
Frequency	: 500Mhz
Technology/Layers	: 45nm/11 Metal Layers

Role : Check SDC and error correction, generating reports for Area, Timing and Power, different efforts for optimization (Generic, Mapping, Optimization), timing analysis and fixing.

ACADAMIC QUALIFICATIONS:

- B.Tech in Electronics and Electrical engineering from (2018-2021) in Usha Rama College of Engineering & Technology with 7.15 CGPA.
- Diploma: State Board of Technical Education & Training from (2015-2018) in Vikas College of Institution and Technology, Nunna,Vijayawada with 78.9 **%** aggregate.
- SSC from Board of Secondary Education (2015) in Sri Krishnaveni High School (Vijayawada) with 8.3 CGPA

SKILLS: Core Languages : VHDL, Verilog and TCL.

PERSONAL STRENGTHS:

- I can easily adopt to any technology
- I have good logical knowledge towards problem solving

DECLARATION:

I here by declare that the above-mentioned information is correct to the best of my Knowledge.

(TARAK SAI KUMAR GANDHAM)