CHAITRA R M
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Bangalore

Career Objective:

An enthusiastic and self-motivated Physical design engineer looking for a challenging and responsible position as Physical design engineer to apply my knowledge and skill with my hard work and patience and be world class in ASIC design.

Certification:

Completed physical design training from" QSOCS Institute of VLSI" training academy from(Aug-2019 to Feb-2020)

Education:

2019	8.75Cgpa BE - (Electronics and Communication) SJM Institute of Technology, Chitradurga.
2016	80% Diploma-(Electronics and Communication) SJM Polytechnic, Chitradurga.
2013	88.80% SSLC SSBHS English med school, Chitradurga.

Technical Skills:

- **Tools** : Synopsys ICC2, Fusion compiler, Cadence-encounter
- **Operating Systems** : Windows and Linux
- **Scripting** : Tcl

Summary:

- Good knowledge of terminologies, Design Constraints, Analyzing timing reports for all Timing paths in STA.
- Good Theorical knowledge of Signal integrity issues.
- Hands on Experience in PnR like Floor planning, Power planning, Placement, CTS,Routing.
- Knowledge of Linux operating system.
- Fixing congestion during various stages of PnR.

.Experience:

- Working as a **Physical design Engineer** in **Design2Signoff (D2S)** Semiconductor Pvt ltd (Mar 2022 to till date).

PROJECT DETAILS:

Project 1: Block level (Client:AMD)

- Technology node: 3nm
- Tool: Fusion compiler
- Metal layers: 18
- Macros/Instances: 14/22K
- Number of Clocks: 03
- Frequecy:69.735mHz

Responsibilities:

- Responsible for block level Floor planning, Placement, CTS, Routing & Timing Fixes.
- Created partial blockages, soft blockages in the channel to resolve congestion issues.
- Created bounds to resolve timing violations.
- Applied path groups to resolve timing violations.

Project 2: Block level(Client:AMD)

- Technology node: 5nm
- Tool: Fusion compiler
- Metal layers: 14
- Macros/Instances: 22/55K
- Number of Clocks: 04
- Frequecy:800MHz

Responsibilities:

- Responsible for block level Floor planning, Placement, CTS, Routing & Timing Fixes.
- Created partial blockages, soft blockages in the channel to resolve congestion issues.
- Created bounds to resolve timing violations.
- Applied path groups to resolve timing violations.

Personal Details:

- Date of Birth :26-04-1998
- Gender :Female
- Nationality :Indian
- Father's name :Mallikarjunappa
- Languages Known :English, Kannada

Declaration:

I do here by declare that the particulars of information and facts stated here in above are true, correct and complete to the best of my knowledge and belief.

CHAITRA R M
(SIGNATURE)