Thrihesh G

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Career Objective

To build a career in VLSI, pursue challenging and engaging opportunities with progressive organizations which allow me to improve my skillsets and contribute effectively towards personal and organizational growth.

Core Competancy

- Comprehensive knowledge on ASIC Flow and in-depth understanding of APR Flow involving Floor planning, Power planning, Placement, Clock Tree Synthesis and Routing.
- Gained knowledge in Static Timing Analysis, generating and analyzing timing reports of various paths, fixing setup and hold violations.
- Understood the concept of PVT variations and exposure to various Advanced STA concepts such as OCV, AOCV, PBA, CRPR, and the effect of clock skew on timing.
- Developed an effective Floorplan with a Contiguous core area, good Utilization, and required channel spacings with the help of a Data flow diagram and Fly line analysis.
- Developed a power network that met the IR drop target and ensured that there were no physical DRC errors, missing vias, and floating wires.
- Implemented a time-driven and legalized Placement to ensure good routability with minimal congestion and without DRC errors (by adding Placement Constraints).
- Implemented and compared two CTS flows Classic and CCD for better timing. Performed routing and fixed DRC errors, LVS Shorts, Antenna violations using Jumper and Diode.
- Generated the timing reports at every stage of the PD flow and analyzed the TNS, WNS, Delays of all paths, Clock Skew, Transition violations, Network and Source Latency.
- Hands-on experience on tools IC Compiler II - Synopsys, PrimeTime ?C Synopsys.
- Good understanding of logic design and CMOS concepts, understanding and modification of TCL scripts.

Education Details

Advanced Diploma in ASIC Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2021**

TKR College of Engineering and Technology, with 7.0 CGPA

2017

Sri Chaitanya Junior Kalasala, with 78 %

SSLC **2015**

Kendriya Vidyalaya No.1, Golconda, with 72 %

Domain Specific Project

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Jun-2022 to Sep-2022

Floorplan, Powerplan and Placement of 40nm block

Description

Technology: 40nm, Supply Voltage: 1.1V, No. of Macros: 34, Std cells: 38k, Clock Frequency: 833 MHz, Power Consumption: 600mw, IR Drop Budget: 55m, Area: 4.2 sq. mm, Transistors Used: HVT, SVT, LVT, Metal Layers: 7, Shape: Rectilinear.

Tools

Synopsys - IC Compiler 2

Challenges

- Development of a floorplan with the help of a data flow diagram and fly lines to achieve the required utilization and to have a contiguous Core area for standard cells.
- Development of an efficient power mesh by modifying Tcl scripts to meet the specified IR Drop and ensuring there are no physical DRCs, floating wires, and missing vias.
- Generation of a highly optimized placement block with controlled congestion through various iterations of channel spacing and modifying floorplan.
- Analyzing timing reports and identifying the cause in the timing path for which it's being violated and observing the WNS, and TNS at various stages of the flow.

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Jun-2022 to Sep-2022

Clock Tree Synthesis and Routing of 40nm block

Description

Technology: 40nm, Supply Voltage: 1.1V, No. of Macros: 34, Std cells: 38k, Clock Frequency: 833 MHz, Power Consumption: 600mw, IR Drop Budget: 55m, Area: 4.2 sq. mm, Transistors Used: HVT, SVT, LVT, Metal Layers: 7, Shape: Rectilinear.

Tools

Synopsys - IC Compiler 2

Challenges

- Implementing two distinct CTS flows Classic and CCD and comparing the timing reports of both flows.
- Analyzing the TNS, WNS, Delays, Clock Skew, Transitions violations, CRPR, Network, and Source Latency of different flows in CTS.
- Rectifying LVS errors such as shorts by removing overlapped routes and performing manual routing.
- Analyzing and resolving the antenna violations by inserting the metal jumper and the diode into the layout.

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Jun-2022 to Sep-2022

Analysis of Timing Reports (STA)

Description

Analysis of timing report includes setup and hold slack calculations for flip flops and latch-based timing paths working at various conditions, reports are analyzed considering OCV, uncertainty, CRPR, Clock Skews, and timing exceptions.

Tools

Synopsys - Prime Time tool Synopsys - IC Compiler 2

Challenges

- Understanding of various STA concepts Timing paths, Timing Arcs, Slack, Timing constraints, Clock abnormalities, Clock skews, Fixing timing violations, CRPR, AOCV, and PBA.
- Understanding of STA tool and Performing Static Timing Analysis by exploring the STA tool-related commands, and analyzing their usage and functionalities.
- Analyzing all the timing paths in different path groups at every stage of the flow APR flow and how some violations are being reduced in the later stages.
- Differentiating some violations which are based on timing exceptions such as false paths and multi-cycle paths and reporting about the same to change in the constraint file.

B.E / B.Tech Academic Project

TKR College of Engineering and Technology

Design of Flight Control System for Aerospace Application

Description

Design of Fight Control System for Aerospace application focused on familiarization development of various sub-systems, especially in the areas of Electronics and Communication, Assembly & Integration of Subsystems and Checkout.

Tools

Linux, VME device driver

Challenges

- Understanding of VME device driver. Complexity in building the code. Accessing the PCI interface.