NAMRATHA M

namrathamg21@gmail.com

7483150568

4th 'A' Cross, Near Ganesha Temple, Raja Kempegowda Badavane

linkedin.com/in/namratha-m-69a58b24b

PROFESSIONAL EXPERIENCE

INTERNSHIP PROJECT

- Design and Implementation of 32 Bit High Level Wallace Tree Multiplier Using 90nm Technology
- Physical Design and Implementation of 32 Bit High Level Wallace Tree Multiplier Using 90nm Technology

FINAL PROJECT

- Comparison of different types of SRAM T-Cells using cadence virtuoso &, Layout, DRC?LVS(on going)

COURSES

- Completed Short term course of VLSI by NIT Dehli
- Completed short term course of VLSI by SJBIT Bengaluru
- Completed intrenship at "DBIT R&D Bengaluru

SKILLS

python	●●●○○	Cadence virtuoso	●●●○○
VLSI Physical Design	●●●○○	Verilog HDL	●●●○○
Basic Electronics	●●●●○		

EDUCATION

Don Bosco Institute of Technology 2019 – 2023
Visvesvaraya Technological University
Bachelor of Engineering.
Electronics and Communications Engineering.
CGPA - 8.74

St.Anne's P U College for Girls Channapatna 2018 – 2019
State Board
percentage - 73.4%

St Joseph's English Medium High School Channapatna 2016 – 2017
State Board
percentage - 84.33%