RESUME

B. Dhavalika

Contact No. : 9676299440

E-Mail Id : Dhavalika.bathimurge@gmail.com

Present status of mine is getting training in an Institute for the course VLSI Design and Verification.

OBJECTIVES

Willing to work as a key player in challenging and creative environment for achieving organization goals in best possible way.

STRENGTHS

- Hardworking, Honest and Dedicated towards work.
- Team player with good leadership skills and also ability to excel as an individual.
- Good Communication Skills.
- Eager to learn new things.

ACADEMIC PROFILE

Education Stream	School/College/University	Passing Year	Percentage/Grade
B Tech ECE	BV Raju Institute of Technology, Narsapur	2020	8.79
Intermediate MPC	Sri Chaitanya Junior College	2016	91.2%
High School SSC 10th	Chigurupati Sri Krishnaveni Talent School	2014	9.3

TECHNICAL LANGUAGES KNOWN

- C and Data Structures, basics of python.
- Verilog HDL (Hardware Description Language), system Verilog.

COURSES AND INTERNSHIPS

COURSES:

- C-DAC Course in Digital System Design (Short term training for one month).
- System Design System on Chip (SDsoc) Training by Digilent (15 days duration).

INTERNSHIPS:

- At ECIL in EMBEDDED SYSTEMS (duration 1-month 2018 may-June).
- At DTDS Technology Pvt Ltd. (duration 10 months from 2019 June- 2020 March).

PROJECTS

TITLE: Cellphone detector

DESCRIPTION: The theme of this project is to prevent usage of mobile phones in prohibited areas.

TITLE: SUPER INTELLIGENT ROBOT

DESCRIPTION: The theme of this project to detect fire and smoke in the Emergency fields.

TITLE: Communication between FPGA using WIFI module.

DESCRIPTION: The theme of the project is to communicate the two FPGA's using WIFI module as wireless communication system with the help of AT commands and TCP/IP protocol.

TITLE: An FPGA Based Navigation Approach For Visually Impaired Individuals.

DESCRIPTION: The theme of the project is to use a navigation approach in a designed environment for visually challenged person and also to avoid the obstacles faced by the individuals and to give the directions. To share the status of the person like location for their cared ones using wireless technology (WI-FI).

TITLE: UP Down counter in SV environment.
DESCRIPTION: The theme of project is to count up down and contains internal register to get the behavior of counter. And the outputs indicates the whether it is up count or down count and at end of the count there is signal to raise count is ended. Here as a Design engineer we designed and as verification engineer implemented coverage and assertions. And verified in SV environment.

TITLE: MEMORY
DESCRIPTION: Memory is a Storage element used to store the data while writing into memory and can read from it when necessary. Verified the memory design in SV environment. Implemented functional coverage and assertions to check the functionality of design.

TITLE : FIFO
DESCRIPTION: The FIFO is a First in First out Design i.e. (Verilog) with FULL and EMPTY signals to indicate the FIFO. Verified the FIFO design in SV environment. Implemented functional coverage and assertions to check the functionality of design.

TITLE: APB protocol

DESCRIPTION: The AMBA APB Protocol supports low-performance, low-frequency system designs. The APB protocol is not pipelined. Used it to connect to low-bandwidth peripherals that do not require the high performance of the AXI protocol. Below mentioned points are done for this project

- Verified the protocol with a single master and single slave environment.
- Implemented Functional coverage model and implemented assertions.
- Understood the APB protocol specification.
- Developed slave logic to drive by the master.

EXPERIENCE

Job title: Jr. Design Engineer

Company: DTDS Technology Private limited.

Time Period: April 1st 2021 – October 31st 2022.

Job role: Worked as Jr. Design engineer. Testing LoRa modules, smart water meter, accelerometer. LoRa evaluation boards. Have knowledge of LoRa communication. Worked for designing of GUI application for our projects. Tested Lora module Node to Node communication.

PERSONAL DETAILS

- Nationality : Indian
- Date of birth : 26-10-1998
- Languages Known : Telugu, English and Hindi
- Current Location : Hyderabad
- Address : EWS-1233 KPHB colony JNTU Kukatpally, Hyderabad.

DECLARATION

I hereby **declare** that the information mentioned above is true to the best of my knowledge.

Signature

(B. Dhavalika)