TARRA NARENDRA

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Trained in Physical Design at Sumedha Institute of Technology (Hyderabad).

Career Objective:

Looking forward to an opportunity for working in a dynamic, challenging environment, where I can utilize my skills for developing my career and for the growth of the organization.

Academic Profile:

S.no	Name of the course	institution	Board/university	Year of pass	Percentage/ CGPA
1.	B.Tech(ECE)	Avanthi's Research and technological academy	JNTUK	2021	6.9
2.	12^{th}	Narayana junior college	Board of Intermediate Education	2017	9.24
3.	10^{th}	National Trinity High school	Board of Secondary Education	2015	8.2

Summary:

- Hands-on experience on EDA tools like DC SHELL ICC2 SHELL.
- Formulated 28nm technologies.
- Experience in debugging skills like DRC & setup and hold.

Projects:

- **Project : RP_TOP**
- Technology : 28nm
- Tools : Synopsys ICC2
- Frequency : 500 MHz
- Macros : 6
- Gate count : 67k
- No of Clocks :1 master clock

Responsibilities:

- Successfully implemented block level design from netlist to GDSII.
- Involved in Floor planning, Power Plan, Placement, CTS, Routing & Static timing analysis.
- Congestion analysis, Timing closure, DRC Fixes.

Projects 2:

- **Project : ALU**
- Technology : 28nm
- Tools : Design Compiler
- Frequency : 200 MHz
- Gate count : 485
- No of Clocks : 3 master clocks

Responsibilities:

- Successfully completed synthesis with 5ns time period.
- Design constraints like input and output delays, updating transition and load.
- Sanity checks and optimization to meet performance.

Technical Skills: -

- Hardware design tools: Design Compiler, IC Compiler ||
- Programming language: Basic C.
- Scripting languages: TCL, TCSH.
- VLSI Skills: Scripting, STA, PNR.

Declaration:

I hereby declare that the information given above is true to the best of my knowledge and belief.

PLACE: -VISAKHAPATNAM **Signature**: -

DATE: - Narendra