Syed Mahaboobsubhani

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SUMMARY

- ➤ Have knowledge on CMOS fundamentals, Digital electronics, and TCL scripting.
- Familiar with ASIC flow (RTL to GDSII).
- ➤ Hands on experience in synthesis, Floor Planning, Power Planning, Placement, CTS and Routing.

➤ Worked on 28nm technology.

ACADEMIC QUALIFICATIONS					
Qualification	Specialization	University/Board	Institute	Year	CGPA/Percentage
B.Tech	ECE	Lovely Professional University	Lovely Professional University	2020	8.06 CGPA
Intermediate	MPC	Board of Intermediate Education Andhra Pradesh	Sri Chaitanya Junior college	2016	94%
Matriculation	SSC	Board of Secondary Education Andhra Pradesh	Madhava Reddy e techno school	2014	9.3 CGPA

PROFESSIONAL TRAINING

6 months VLSI Physical design using Synopsys Tool training at Sumedha Design systems Pvt Ltd., Hyderabad.

TOOLS

Synthesis : Design Compiler
Timing Analysis : Prime Time
PNR : ICC2

REALTIME PHYSICAL DESIGN PROJECTS

i. RPTOPTOP

Description : Block Level Implementation

Duration : 2 months

Technology node: 28nm

Instance count: 76K

Frequency: 454 MHz

Macros : 6

Number of Clocks: 1

Metal Layers : 9

ii. ALU

Description : Block Level Implementation

Duration : 1 month

Technology node: 28nm

Instance count: 800

Frequency: 400 MHz

Number of Clocks: 3

Generated clock : 1

Metal Layers : 9

PERSONAL DETAILS

Date of Birth: 21 September, 1997

Nationality: Indian

Address: H.No 1-71, Malla Reddy Pally vill, Komarole Mandal, Prakasam Dist,

Andhra Pradesh, 523373.

DECLARATION

I do hereby declare that the above particulars of facts and information stated are true, correct, and complete to the best of my belief and knowledge.

Place: Hyderabad Signature

Date: 12 December, 2022 Syed Mahaboobsubhani