Kummari Upendra
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Career Objective

To obtain a challenging and responsible position as a Physical Design Engineer enabling me to utilize my Technical skills that offers growth and advancement opportunities.

Core Competancy

- Thorough understanding on ASIC flow and hands-on experience on APR flow that incudes Floorplanning, Powerplanning, Placement, CTS, and Routing.
- Well-versed in various STA concepts such as Timing Paths, Timing Arcs, Slack, Timing Constraints, PVT Corners, Modes, Clock Skews, fixing Timing Violations, CRPR, AOCV.
- Developed an Floorplan with Contiguous core area, good Utilization, good congestion and required Channel Spacings with the help of Flylines and Dataflow DIagram.
- Developed a Power network with no physical DRC errors and also made sure to meet the specified IR drop by varying the Width, Spacing and Pitch of the Metals.
- Created a Legalized Placement block with minimal Congestion, no DRC errors (by adding Placement Constraints like Blockages), and no floating standard cells.
- Implemented and compared two CTS flows Classic and CCD for better timing.
- Generated Timing Reports at every stage of PD flow and analyzed the TNS, WNS, delays, clock skew, transitions violations, CRPR, network latency and source latency.
- Hands on experience on tools Synopsys IC Compiler II, Synopsys PrimeTime.
- Good understanding in Logic Design, Network Analysis and CMOS concepts.
- Undertsanding and modifying of TCL scripts

Education Details

Advanced Diploma in ASIC Design **2023**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**
Sree Vidyanikethan Engineering College, with 78.89 %

2018
Narayana Junior College, with 97.3 %

SSLC **2016**
Ravindra Vidyanikethan School, with 92.15 %

Domain Specific Project

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Oct-2022 to Feb-2023

Design of a SOC physical design block on 40nm tech

Description

Design of SOC physical design block ready to be integrated into a full chip. Overview : 40nm design, Clock Frequency-1GHz, Area-4.2sq.mm, Supply-1.1v, Power Budget-600mW, IR-Drop-5% of VDD, Macros-34, Standard Cells-41k, Metal Layers-7.

Tools

Synopsys IC compiler2

Challenges

- Designing a Floorplan by determining macro placement as per dataflow diagram, flylines and using guidelines in order to achieve contiguous core area and good core utilization.
- Building a Powerplan to maintain power network connectivity and IR drop. Also ensuring that there were no missing vias, floating wires and PG DRC violations.
- Analyzing the route congestion map and tried different floorplan experiments to get the best congestion values.
- Understanding tool's behaviour while clock tree synthesis to meet target skew, Min/Max latencies, fixing timing violations and understanding DRC and LVS errors.

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Sep-2022 to Oct-2022

Analysis of Timing Reports (STA)

Description

Design of SOC physical design block ready to be integrated into a full chip. Overview : 40nm design, Clock Frequency-1GHz, Area-4.2sq.mm, Supply-1.1v, Power Budget-600mW, IR-Drop-5% of VDD, Macros-34, Standard Cells-41k, Metal Layers-7.

Tools

Synopsys Primetime, Synopsys IC compiler2

Challenges

- Exploring the PrimeTime tool and commands related to the tool by analyzing their usage and functionalities.
- Understanding the timing reports at every stage of PD flow, finding the cause of timing violations and how some of the violated paths are being reduced in later stages.
- Identifying the violations based on timing exceptions such as false paths, multi-cycle paths and reporting the same in the constraint file.
- Analyzing the effect of clock skew, CRPR, OCV timing derates for all four different timing paths from the timing reports.

B.E / B.Tech Academic Project

Sree Vidyanikethan Engineering College

Design of Quaternary Logic Gates and Circuits using Graphene Nanoribbon Field Effect Transistors

Description

Developed various circuits using GNRFET technology in Quaternary logic.

Tools

H-spice

Challenges

- GNRFETs are an attractive replacement for current transistors. However there are few challenges like Band Gap limitations, Fabrication cost and saturation.