RESUME

DARSHAN V
#373/C51 2nd main 2nd Cross
Teachers layout, Davangere

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CARRER OBJECTIVE:
To work in a challenging environment which inspires me to enhance myskills and explore.

Professional Training:
Advanced VLSI Design and Verification Course at Maven Silicon.
VLSI Design and Training Center , Bangalore
(Dec 2022 – present)

EDUCATION:

Year	Degree/Certificate	Institute / School	Aggregate
2022	MTech (VLSI Design and Embedded Systems)	Bangalore Institute of Technology(VTU)	8.33
2020	Bachelor of Engineering (Electronics and Communication)	Bapuji Institute of Engineering and Technology (VTU), Davangere	6.03
2016	Pre-University Course	Sir M Visvesaraya PU College , Davangere	70%
2014	Class 10th: SSLC Board	Siddganaga Composite High School , Davanagere	64%

TECHNICAL SKILLS:

Design Skill:

- **Digital Electronics:** Combinational & Sequential circuits, FSM, Memories, CMOS implementation, Stick diagram.
- **Static Timing Analysis(STA):** STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks, Clock domain and Variations, Clock Distribution Networks, Fixing timing failure.

- Advanced Verilog & Code Coverage: Generate block, Continuous Procedural Assignments,

- **Self-checking Testbench**, Automatic Tasks Named Events and Stratified Event Queue, Code Coverage: Statement and branch coverage, Condition & Expression Coverage, Toggle & FSMCoverage.

Verification Skill

- **System Verilog HVL**

  Memories - Dynamic array, Queue, Associative array, Task & Function - Pass by referenceInterface - Modport and clocking block.
  Basic and advanced object-oriented programming - Handle assignments, Copying the object
  contents, Inheritance, polymorphism, static properties and methods,
  virtual classes,and parameterized classes.
  Constraint Randomization - constraint overriding and inheritance, Distribution and conditionalconstraints, Soft, static and inline constraints.

Project:

Router 1x3 – RTL design and Verification
HDL: Verilog
HVL: SystemVerilog TB
EDA Tools: Questasim and ISE

Description: The routeraccepts data packetson a single 8-bit port and routesthem to one of the three output channels, channel0, channel1 and channel2.

INTERNSHIP :

- Completed One-Month Internship on Internet of Things and Embedded System in EDU Craft Techonology, Bangalore
- Completed One-Month Internship on Functional Verification Using System Verilog in CoreEL Technologies, Bangalore

ACADEMIC PROJECT:

1. Design and Verification of Ethernet Protocol using System Verilog
2. Design and Verification of APB Protocol using System Verilog.
3. IOT Based Industry Protection System Using Arduino
4. Design and Verification of Memory Controller Using System verilog
5. Development of Verification environment for a digital design from scratch and getting verifying the functionality of design

WORKSHOPS ATTENDED:

1. Participated in three days Workshop on IoT held at Bapuji Instituteof Engineering and Technology.
2. Participated in two days workshop on Mobile Communication held at Bapuji Institute of Engineering and Technology.

Publications:

1. Presented a paper entitled "Implementation and Verification of Memory Controller Using System Verilog" in International journal of Innovative research in technology

Personal Information:

Date of Birth: 5th of March 1998
Father's name: Veerabhadrappa B
Languages known: English, Kannada, Hindi,