Vellaluru Sai Bhargav
Email: sai77772554@gmail.com
Contact: 9392100161

Objective:

To succeed in an environment of growth and excellence and earn a job which provides me job satisfaction and self-development and help me achieve personal as well as organization goals.

Academic Details:

Graduation	College / School	Year Of Passing	Percentage/ CGPA
B.Tech (ECE)	Mekapati rajamohan reddy institute of technology and science, Nellore	2022	7.2 CGPA
Intermediate	Sri chaithanya junior academy college, kadapa	2018	91.4 %
SSC	Sri Sai Bharathi High School,Vontimitta, AP.	2016	9.3 CGPA

Professional Experience:

- Completed Physical Design Course 6 Months from Takshila Institute of VLSI technologies.
- Good Understanding of block level Physical design and verification concepts like **Floor planning, CTS, STA, DRC/LVS, DFM etc.**
- Practical exposure to Physical Design tools from **ICC-II/ICC Compiler, Design Compiler, Primetime, IC Validator** tools.
- Basic scripting to improve layout efficiency (Tcl).

Technical Skills:

- Strong understanding in the RTL to GDSII flow or design implementation.
- Good in concepts related to synthesis, place and route, CTS and timing convergence.
- Good knowledge and experience in Block-level Floor-planning and Physical verification.
- Working experience with tools like ICC/ICC2.
- Strong knowledge in standard place and route flows ICC/Synopsys flows preferred.
- Well versed with timing constraints and STA.
- Ability to multi-task and flexibility to work in global environment.
- Good knowledge of Windows 7, 8 and Linux.

Professional Projects:

Title	**ORCA_TOP_IO**
Tool used	IC Compiler
Description	• Technology: 28nm • No. of macros:30 • Layer:9 • Std. cell count:50000 • Frequency:400Mhz • No. of clocks :7clocks
Responsibilities	Iterative Floorplan, IO ports placement, Power planning, Placement and CTS reviews, Routing and DRC checks.

Title	ORCA_TOP
Tool used	IC Compiler
Description	• Technology: 32nm • No. of macros:40 • Layer:9 • Std. cell count:56013 • Frequency:416Mhz • No. of clocks :7clocks
Responsibilities	Iterative Floor plan, IO ports placement, Power planning, Placement and CTS reviews, Routing and DRC checks

Academic Project:

- Defence radar system for detecting, ranging and lauching.
  - Radar is a detecting system that uses the radio waves to determine the characteristics of moving objects, such as range, height, direction and the speed of the objects.

Personal Details:

Date of birth : 10-05-2000
Languages Known : Telugu, Hindi, English
Permanent Address : 6-1, seethapuram, vontimitta, kadapa, AP

Declaration:

I hereby declare that I would be glad to come for interview at any time that is convenient to you and assure you of my devoted service.

Date: **Vellaluru Sai Bhargav**
Place: