+91 9515040756

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EDUCATION

B.Tech | ECE | Aggregate: 72%
Tadipatri Engineering College
Andhra Pradesh
2012 – 2016

Class XII | MPC | Aggregate: 89.7%
Board of Intermediate Education
Andhra Pradesh
2010 - 2012

Class X | Aggregate: 87.8%
Board of Secondary Education
Andhra Pradesh
2009 - 2010

EXTRA CURRICULAR ACTIVITIES

- Achieved "Star of the month" thrice (September and February and March 2023) during the Advanced Physical Design and Verification Training Course at Maven Silicon.
- Participated in National level symposium at Sri Krishna Devaraya Institute Of Technology
- Participated in National level workshop at Tadipatri Engineering College Conducted by IIT Khanpur.
- Participated in National level symposium at JNTU, Pulivendula

JINKA GEETHAPRIYA

MAVEN SILICON
Centre of Excellence in VLSI

CAREER OBJECTIVE

To secure a challenging position in a reputable organization to expand my learnings, knowledge and skills. Secure a responsible career opportunity to fully utilize my training and skills, while making a significant contribution to the success of the company.

PROFESSIONAL TRAINING

Advanced Physical Design & Verification
07/2022 – Present | Maven Silicon

- Physical Design
- Floor planning, Placements & Routing
- Clock Tree Synthesis
- Static Timing Analysis
- Physical verification & Signoff

WORK EXPERIENCE

1. Hinduja Global Solutions
Customer Service Representative – 18-08-2016 to 05-03-2019
Quality Analysts – 06-03-2019 to 31-01-2020

2. Altruist Private Limited
Quality Analysts - 01-02-2020 to 31-03-2021

Responsibilities:

- Creating a Test plan
- Using the plan to access functionality, performance, reliability, stability and compatibility
- Gaurating against incorrect language usage and incorrect format used
- Ensuring the product is culturally compatible with the target market

VLSI DOMAIN SKILLS

HDL: Verilog
EDA Tools: Mentor Graphics – Modelsim, Intel Quartus Prime, Oasys, Aprisa and Calibre from Siemens EDA, Synopsys Prime Time and Fusion Compiler.
Programming Languages: C Language
Operating Systems: Window & Linux
Core Skills : RTL Coding using Synthesizable constructs of Verilog, FSM based design, Simulation, CMOS Fundamentals, Static Timing Analysis, Logic Synthesis, Floor planning, Placement, Routing, Signoff (ERC,DRC and LVS)

PERSONAL DETAILS

Father's Name: Rajagopal.J
Date of Birth: 05-01-1995.
Nationality: Indian.
Languages: English, Telugu, Kannada

STRENGTHS

- Positive Attitude
- Problem Solving
- Self Motivated
- Communication Skills
- Typing Speed (50WPM)

HOBBIES

- Classical Dancing
- Browsing
- Puzzle Solving

TOOLS

HDL used: Verilog.
RTL Design: ModelSim, Quartus Prime.
Physical Design: Aprisa, Oasys, Tanner.

B.TECH PROJECT

Main Project Name:
Video Object Tracking using threshold values and diffusion distance

Roll On Project: Leader

AIM: Provide security to the surveillance system

Description:
The Project is designed to provide security for surveillance. By using this tracking system we can track the moving objects by using threshold values of background objects and main object. By this we can provide high security in militaries etc.

VLSI DESIGN SKILLS

STA:

- STA basics, comparison with DTA, timing path and constraints.
- Different types of clocks, clock domain and variations, Clock Distribution Networks, Fixing Timing failure

Verilog Programming:
Data types, Operators, Processes, Blocking & Non Blocking Assignments, Delays in Verilog, begin end & fork-join blocks, looping and branching constructs, System tasks & Functions, compiler directives, Races in simulation, pipelining RTL & TB coding, generate block.

Physical Design:
Logic Synthesis, Floor Planning, Placement, Routing, Clock Tree Synthesis and Timing Analysis using Aprisa, DRC, ERC, LVS and signoff using Calibre.

PROJECTS

Physical Implementation of RISC-V Design
01/2023 - 02/2023 | Maven Silicon
The RV32I Processor is designed to support all RV32I Base Integer Instructions (Total-39). It's a three stage pipelined processor which executes 32 bit instructions in program order.
Pipelined Stage I - The instructions are fetched from the memory.
he control signals for all units

Responsibilities for the Design

- Synthesizing the RISC-V RTL and generate the Gate Level netlist.
- Implementing Floor Planning, Placement and Routing processes on the netlist.
- Implementing Clock Tree Synthesis.
- Performing Timing Analysis and achieve timing closure.
- Perform DRC, ERC, and LVS for signoff.
- Exporting the final GDS-II

Router 1x3
09/2022 - 10/2022 | Maven Silicon
The Router accepts data packets on the 8 bit data port and then routes to destination channels (channel-0/1/2).
The internal architecture consists of Register block, Synchronizer block, FSM block and three FIFO blocks (one for each output channel).

Responsibilities

- Architected block level structure for the design
- Implemented RTL using Verilog HDL
- Simulated and synthesized by using Modelsim and Quartus Prime.

Implemented RTL Design and Physical Design

Declaration

I hereby acknowledge and confirm that the information furnished above and complete to the best of my knowledge.

Date:
Place: Bangalore

J Geethapriya