SRIVIDYA SURAPARAJU

vidyasharma0014@gmail.com, 7981177662

HYDERABAD-501510, Telangana

Career Objective

To obtain responsible position in Semiconductor Industry as PD Engineer which is intellectually challenging and provides scope for advancement .

Core Competancy

- In-depth knowledge in PD flow involving Floorplanning , Powerplanning , IR drop analysis , Standard Cells Placement , Clock Tree Synthesis and Routing.
- Good knowledge in Logic Design and MOSFET concepts.
- Hands on experience in APR and STA tools such as IC Compiler2 and Prime Time from Synopsys.
- Fair knowledge and hands on experience in STA , CRPR , Interpreting timing reports , fixing Setup and Hold violations.
- Worked with different Floorplans to obtain High utilization ratio , good contiguous core area for Std-cells and designed powerplan to meet required IR Drop.
- Placed Standard Cells with acceptable Congestion ensuring good Routability.
- Generated and analysed timing reports of Pre-Layout and Post-layout STA and resolved timing violations.
- Knowledge in scripting PERL , TCL and well aware of different commands in Linux Operating System.
- Understood about various PVT Corners , False paths , Half-cycle paths , Multi-cycle paths and Asynchronous Clocks.
- Fixed various DRC , LVS and Antenna violations.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electrical and Electronics** **2021**

CVR COLLEGE OF ENGINEERING, with 9.13 CGPA

2017

SRI MEDHAVI JUNIOR COLLEGE, with 92.8 %

SSLC **2015**

D.A.V PUBLIC SCHOOL, with 91.2 %

Domain Specific Project

RV-VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Jul-2022 to Sep-2022

Designing of an ASIC at Block Level

Description

Overview : 40nm design, Clock Frequency: 1 GHz, Shape: Rectilinear, Macro count: 34, Standard cell count : 41k, Area : 4.2sq.mm, Supply Voltage: 1.1v , Power Budget: 600mwatts, Metal layers : 7.

Tools

IC Compiler2 from Synopsys

Challenges

- Block is timing and congestion critical. Performed so many floorplan experiments to arrive at a better floorplan.
- Understanding the design constraints and designing floorplan accordingly to create a contiguous core area for standard cells.
- Building a good powerplan to meet the specified IR drop and ensuring no missing vias , floating pin errors occur after building power network.

RV-VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Jul-2022 to Sep-2022

Fixing DRC violations

Description

Performed DRC check after every step ,resolved them using tool commands and Fixed Congestion using blockages and keep-out margins.

Tools

IC COMPILER2 from Synopsys

Challenges

- Fixed DRC issues like overlap , short and spacing of macro errors after completion of floorplan.
- Given Placement and Routing Blockages to resolve errors after placement.
- Fixed DRC's of metal manually and done manual route to fix timing.

RV-VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Jul-2022 to Sep-2022

Analysis of Timing Reports

Description

Generated Timing Reports and analysed them considering OCV, AOCV, CRPR, Uncertainity and exceptions like multi-cycle, false paths by referring to the constraints file.

Tools

IC COMPILER2 , Prime Time from Synopsys

Challenges

- Analysed all timing paths in various path groups at every stage of the PD flow.
- Differentiating violations which are based on timing exceptions such as false paths and multi-cycle paths.
- Understood the effects of OCV, AOCV, CRPR and Skew factors in timing analysis.

B.E / B.Tech Academic Project

CVR COLLEGE OF ENGINEERING

Speed control of single-phase Induction Motor using H-bridge Inverter

Description

H-bridge inverter is capable of providing desired alternating voltage level at output using DC voltages as input. The inverted output is applied to the induction motor . So by using H-bridge inverter, we can achieve speed control of induction motor.

Tools

Arduino UNO , Printed Circuit Board (PCB) , Induction Motor and have done the spice simulation to check integrity of circuit design and predict circuit behaviour.

Challenges

- 1. Analyzed working of the circuit with various values to achieve the desired output. 2. Soldering the required components such as capacitors, resistors, LED's, power diodes on PCB accurately to build electrical connection.