ACHUGATLA RAFATH

Physical Design Engineer

CONTACT ME

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CAREER OBJECTIVE

To work in a highly competitive environment with a perfect challenge by contributing the best for the growth of the organization while ensuring growth in my personal career.

PERSONAL PROFILE

Date of Birth : 03-07-2000
Place of Birth : Kurnool
Gender : Male
Nationality : Indian

LANGUAGES KNOWN

English
Telugu
Hindi
Urdu

EDUCATION

Bachelor of Technology - Electronics and communication Engineering
Sree Vidyanikethan Engineering College, Tirupati
2017 - 2021
CGPA : 7.13

Intermediate
Narayana Junior College, Kurnool
2015 - 2017
Percentage : 94.7

Secondary School Certificate
Sree Narayana Vidya Vihar High School, Atmakur
2015
CGPA : 9.3

Professional Training
Advanced Physical Design & Verification
Maven Silicon
April 2022 - Present

TECHNICAL SKILLS

Digital Design & Verilog programming

- **HDL :** Verilog
- **EDA Tools :** Modelsim & Questasim by Intel
- **Core Skills :** Combinational and Sequential Circuit, FSM, Memories, CMOS implementation, Stick diagram, Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin -end & fork join blocks, looping & branching construct, System tasks & Functions, compiler directions, FSM coding, Synthesis issues, Races in Simulation, pipelining RTL & TB Coding

VLSI Physical Design & Verification

- **EDA Tools :** Tanner, Oasys, Aprisa by Mentor Graphics, Synopsys Fusion Compiler,Calibre by Siemens
- **Domain :** Knowledge of MOSFET and their characteristic, Layout, Stick Diagram, Logic Synthesis, Floorplanning, Placement, Routing, Clock Tree Synthesis and Timing Analysis using Aprisa, DRC, ERC, LVS and signoff using Calibre

- **Operating systems :** Windows and Linux

PROJECT

- **Router Project - Maven Silicon**
  In this project we performed Physical Design flow for Router Design. Where we did the following things:
  - Synthesized RTL Scripts in OASYS RTL TOOL
  - Did Floor Planning and Power Planning, Placement and Optimization, Clock Tree Synthesis, Timing Analysis and Routing in APRISA TOOL & Synopsys Tool
  - Physical Verification: DRC, LVS, and PERC are executed in CALIBRE TOOL
- **Automatic Obstacle Avoiding Robot**
  The aim of this project is to design automatic obstacle avoiding robot.HC-SR04 ultrasonic sensor is used which triggers the pulses and receives the echo when the obstacle is near by. Based on this result Arduino instructs the LM298N motor driver module to navigate the wheels forward, backward, left or right. The application of this robot is not limited and it is mostly used in military organization now to carry out many risky jobs.

CERTIFICATION

- Certified in "**IOT-INTERNET OF THINGS"** internship held by **"INNOVIANS TECHNOLOGIES"** at hyderabad from 03 jun to 28 jun 2019
- Got Certificate of completion in **VSD - Physical Design Flow** by instructors Kunal Ghosh in **Udemy** platform on 09 Feb 2023

ACHIEVEMENTS

- Played role of class committee member
- Worked as Volunteer (Web Casting) in General Elections 2019 and Municipal Elections 2021
- Participated in "Student development program on EPICS" conducted by ACME(Association for Communication Majors & Enthusiasts) during the academic year 2018-2019 and got Certificate of Appreciation

DECLARATION

I hereby declared that the above – mentioned particulars are true and correct to the best of my knowledge and belief.

Date : 05-04-2023
Place : Nandyal A.Rafath

HOBBIES

Photography
Farming
Singing
Listening to Music
Watching Movies
Travelling
Playing Chess

STRENGTHS

Problem Solving
Technical Skills
Adaptability
Collaboration
Strong Work Ethic
Time Management
Critical Thinking
Handling Pressure