Anirban Dey

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Biswanath Chariali-784176, Assam

Career Objective

Seeking a challenging and performance-oriented career with an organization of distinction that recognizes my true potential and provides me professional growth in the industry.

Core Competancy

- Worked on various tasks using different commands in Static Timing Analysis (STA) with the help of given Netlist and Constraint Files.
- Worked on Block-Level Implementation of Design from Gate Level Netlist to GDSII using I/p files such as netlist, Constraints, Library, TLU+, UPF, Technology & DEF files.
- Worked on floorplan, power planning of a block in order to meet required IR drop and congestion at placement stage.
- Built the Clock Tree in CTS stage and resolved as well as fixed antenna violations in routing stage.
- Resolved and fixed DRC and LVS errors at every stage of the Physical Design Flow.
- Interpreted the timing report at every stage of APR Flow to understand the timing effects through STA and meet the hold and setup violations.
- Studied Data Flow Diagrams and Timing Models which basically represents its complete I/O characteristics without the need for a complete Gate Level Netlist of the block.
- Dealt with clock abnormalities i.e. Clock Uncertainty such as Jitter, Latency, Skew, margin, etc.
- Have a good grip on topics such as CMOS Fundamentals, Digital Electronics, Network Analysis, Semiconductor Devices, etc.
- Worked on tools such as Synopsys ICC2, Prime Time.

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

North Eastern Regional Institute of Science and Technology (NERIST), with 8.72 CGPA

2017

Little Star School, with 81 %

SSLC **2015**

Little Star School, with 78.5 %

Domain Specific Project

RV SKILLS: Center for Emerging Technologies

Trainee Nov-2022 to Feb-2023

Block Level Implementation of a 40 nm chip

Description

Block-Level Implementation of Design from Gate Level Netlist to GDSII in a 40 nm Technology with a supply voltage of 1.1V, Area = 4.2 sq. mm, power budget =600nW, 5 % Max IR Drop, No. of Standard Cells = 38403 and 7 metal Layers.

Tools

IC Compiler II- Synopsys

Challenges

- Placing Macros and Meeting the IR drop in the floor planning and power planning stages respectively.
- Fixing congestion Related Issues in the placement stage and performing CTS and routing in the layout.
- Analyzing and comparing timing reports in every stage of the PNR flow by checking the maximum transition, max capacitances, etc.
- Mitigating DRC, LVS, antenna violations related issues.

B.E / B.Tech Academic Project

North Eastern Regional Institute of Science and Technology (NERIST)

Analysis and Determination of Soil Parameters using Arduino.

Description

- To determine soil parameters like Humidity, Temperature, Soil-moisture and the presence of different gases such as smoke and CO2 in different soil samples and display them on LCD.

Tools

- Hardware: Arduino Uno, Humidity and Temperature Sensor (DHT 11), Soil-Moisture Sensor, Gas Sensor (MQ 135), LCD. - Software: Arduino IDE, Proteus Professional.

Challenges

- - Faced problems connecting different hardware with a microcontroller (Arduino Uno). - Faced a lot of problems writing code in Arduino IDE. - Sensors used are quite sensitive and get destroyed easily.