Shalini S

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Career Objective

To secure a challenging role with responsibility in the field of physical design in cutting-edge technology nodes, where I can effectively use my knowledge and talents for both organizational growth and personal development.

Core Competancy

- Practical knowledge of FLOOR and POWER PLANNING, PLACEMENT, CLOCK TREE SYNTHESIS, and ROUTING on the IC COMPILER II.
- Practical experience using PRIMETIME for STATIC TIMING ANALYSIS and timing closure at the block level by analyzing the timing reports at multiple modes and scenarios.
- Worked on designing a floorplan that adhered to macro placement guidelines, avoided small narrow channels between macros, good continuous area, with minimal congestion.
- Ensuring that there are no overlap cells, missing vias, floating wires, or cells, and adding routing or placement blockage accordingly so that it passes DRC and legality.
- Building CTS and analyzing reports for setup and hold violations and constraining False paths, Multicycle paths, I/O delay, Asynchronous clocks, CRPR, and PVT corners.
- Good knowledge of non-default routing, signal routing, DFM, and Antenna issues. ASIC FLOW, Digital electronics, Circuit Analysis, and Basics of MOSFET theory.
- Observed that a bad floorplan will result in a variety of physical DRCs such as an increase in routing congestion, increase in IR DROP, and waste-age of die area.
- Possess the ability to implement all STA concepts and relate them to app options to confine the design to satisfy desired specifications, analyzing and fixing DRC AND LVS
- Applying TCL scripts with the proper attributes to automate design and using the STA concept to correlate with app options to constrain the design.
- Understood the need for clock abnormalities, Physical cells, Tie cells, Clock gating cells, Spare cells, DFT, and scan chain reordering in the design.

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Presidency University , with 7.71 CGPA

2018

Narayana PU College , with 79.30 %

SSLC **2016**

M.M.E.T English High School, with 79.20 %

Domain Specific Project

RV-Skills Center for Emerging Technologies

Graduate Trainee Engineer Aug-2022 to Feb-2023

Design of a SOC physical design block on 40nm tech

Description

Designed an 833MHz block-level chip with a 1.1V supply voltage in 40 nm technology. having 38921 standard cells and 34 macros cells, used CCD flow to achieve accurate timings in the clock and data paths with a given power budget of 600 mW.

Tools

Synopsys Primetime tool for Static Timing Analysis, Synopsys IC complier II tool for APR flow

Challenges

- Ensuring that the macros are properly spaced to create a good layout. giving appropriate width, offset, and pitch values for the metal layers used to achieve the desired IR drop
- Separating the macros with enough space to ease congestion. By giving keepout margin, routing blockage, and placement blockage, to ensure there are no DRC violations.
- To ensure that there are no DRC violations in each step, Standard cells must be legally placed in their appropriate std cell rows. Routing CTS with NDR rules to avoid Xtalk and EM.
- Fixing Antenna violations by metal jumpers or by inserting antenna diode. Rerouting the existing nets manually while solving antenna issues to avoid new DRC's

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RV-Skills Center for Emerging Technologies

Graduate Trainee Engineer Aug-2022 to Feb-2023

STATIC TIMING ANALYSIS

Description

Timing analysis for latch and flip-flop having different timing paths operating under various operating conditions while considering PVT conditions OCV, AOCV, CRPR, and uncertainty while constraining them.

Tools

Synopsys PrimeTime

Challenges

- A thorough grasp of the STA is necessary to set the constraints, such as latency, uncertainty, transition, and input and output delays for the given block
- Must be knowledgeable about the timing paths. to decide the launch and capture paths to obtain the setup and hold slack information, as well as the timing of paths with latches.
- Requires careful consideration when analyzing impacts like Signal Integrity, which focuses on Xtalk analysis. knowing how to overcome these challenges .
- Analyzing the timing reports for various timing paths that are having latches and flip flops and understanding the difference between PBA and GBA was challenging.

B.E / B.Tech Academic Project

Presidency University

Vehicle-to-vehicle communication using LIFI

Description

A cutting-edge technology that can detect any breakdowns and the type of vehicle on the road. Li-Fi technology should be used to create vehicular communication to reduce traffic accidents and to give emergency vehicles priority.

Tools

Software: Embedded C, Arduino IDE Hardware: Arduino Uno,2*16 LCD, APR, selection sound recorder/reply IC experiment board, DC 12V 1×4 Key Switch Keypad, Light Fidelity-Receiver (Li-Fi Rx), Light Fidelity-Transmitter (Li-Fi Tx).power supply 5v or 12v.

Challenges

- Setting up the transmitter and receiver so they may readily communicate with one another, creating the suitable embedded C. transcribing the voice note to the keypad such that the output from the display, as well as the APR, are in accordance