Saurabh Bhivgade

Contact

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Khapri railway wardha road
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Skills

- Digital Electronics
- RTL coding using synthesizable constructs of Verilog
- FSM based design
- Static Timing Analysis
- System Verilog
- UVM

Expertise

- HDL: Verilog
- HVL: System Verilog
- EDA Tool: Quartusprime, Modelsim, Questasim
- DOMAIN: ASCI/FPGA front end design and verification
- OPERATING SYSTEM: LINUX
- PROGRAMMING: C++

Area of Interest

- Digital Electronics
- RTL Design
- VLSI
- Verification

Career Objective

A dedicated student and an individual who Believes in hard work with smart approach and giving hundred percent efforts to fulfill responsibility for the growth of organization.

Education

GH Raisoni college (RTMNU) — Nagpur, Maharashtra
Bachelors of Engineering (ECE) — 2016-2020 CGPA: 8.16

Santaji Mahavidyalayam — Nagpur, Maharashtra
12th — 2015 60.70%

Utkarsh Vidya Mandir — Nagpur, Maharashtra
10th — 2013 80.60%

Professional Training

Advanced VLSI Design and Verification Trainee
Maven Silicon VLSI Training center, Bengaluru — March 2022 - Till date

- Being trained in Digital Electronics, Verilog HDL for designing the hardware, System Verilog for verifying and UVM to develop efficient and reusable testbenches.

Projects

- **Router 1x3 RTL Design and Verification**
  HDL: Verilog
  HVL: System Verilog
  TB Methodology: UVM
  EDA Tool: Questasim

  DESCRIPTION:
  The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

  Responsibilities:
  - Architected the block level structure for the design
  - Implemented RTL using Verilog HDL.
  - Architected the class based verification environment using System Verilog
  - Verified the RTL model using System Verilog.
  - Generated functional and code coverage for the RTL verification sign-off
  - Synthesized the design.

- **Design and Verification of a 4-bit loadable up/down counter**
  Designed the counter in Verilog and verified it using CRCDV by developing the TB Architecture in System Verilog.

- **Advanced Peripheral Bus (APB) Protocol.**
  DESCRIPTION:
  The Advanced Peripheral Bus (APB) is part of the Advanced Microcontroller Bus Architecture (AMBA) protocol family. It defines a low-cost interface optimized for minimal power consumption and reduced interface complexity.

Achievements

- Maven Silicon STAR OF THE MONTH
- Achieved three times **Gold** medal incollege for securing 1st position
- Campus Ambassador of INTERNSHALA

Hobbies

- Meditation
- Pranayam

Soft skills

- Patience
- Team Person
- Quick learner

Languages

- English
- Hindi

VLSI Design Skills

Digital Electronics:
Combinational & Sequential circuits, FSM, Memories.

STA :
STA Basics, Comparison with DTA, **Timing Path and Constraints**, Different types of clocks, Clock domain and Variations, Clock Distribution Networks, Fixing timing failure.

Verilog Programming :
Data types, Operators, Processes, **BA & NBA**, Delays in Verilog, **begin - end & fork join blocks**, looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Synthesis issues, Races in simulation, pipelining RTL & TB Coding.

Advanced Verilog & Code Coverage:
Generate block, **Continuous Procedural Assignments**, Self-checking testbench, Automatic Tasks, Named Events and **Stratified Event Queue**,
Code Coverage: Statement and branch coverage, Condition & Expression Coverage, Toggle & FSM Coverage.

VLSI Verification Skills

System Verilog HVL:
Interface and clocking block, **Inheritance and Polymorphism**, **Constraint randomization** - Inline, distribution, conditional, soft and static constraints. **Mailbox and semaphores**, Functional coverage, **CRCDV** and regression testing.

System Verilog Assertions:
Types of assertions, assertion building blocks, sequences with edge definitions and logical relationship. **Sequences with different timing relationships**. Clock definitions, implication and repetition operators, different sequence compositions, inline and binding assertions, advanced SVA Features and assertion Coverage.

UVM:
UVM Objects & Components, UVM Factory & overriding methods, Stimulus Modelling, UVM Phases, **UVM Configuration**, TLM, UVM Sequence, **virtual sequence & sequencer.**

Declaration

I hereby declare that all the above information is true to the best of my knowledge.

DATE:
PLACE: Nagpur Maharashtra

Saurabh Bhivgade