# **RESUME**

Name: JHA PRAKASH AMARNATH Email id: jhaprakash209@gmail.com Mobile Number: +91 7698248928

# **EXPERINCE**:

• "Indicus Technology Ahmedabad" Training in VLSI Design and Verification Domain 6 month of Training.

# **PROFESSIONAL SUMMARY:**

- Working experience in writing UVM/SV test cases
- Very good experience in UVM and System Verilog
- Very good experience in RTL debugging
- Experience in writing System Verilog assertions/coverage
- Experience in verification architecture plan, test plan, coverage plan, and test case development of various testbench components
- Experience in coverage driver verification
- Very good debugging skills
- Strong Digital and Logic Design knowledge

#### **PROFESSIONAL SKILLS:**

Operating Systems	Windows, Linux
Programming Languages	Verilog, System Verilog
Methodology	UVM
VLSI EDA Tools	Questa Sim, Model Sim
Protocol Knowledge	АРВ, АНВ

# **EDUCATION QULIFICATION:**

Degree	Institute Name	Pass out Year	CGPA/Percentage
BE	L. J INSTITUTE OF ENGINEERING & TECHNOLOGY, AHMEDABAD	2020	6.91
DIPLOMA	L. J POLYTECHNIC, AHMEDABAD	2017	6.66
10 <sup>th</sup>	R. G YADAV ENGLISH Hr. Sec. SCHOOL, AHMEDABAD	2014	60 %

#### PROJECT: - 1

Project	Verification of DDR45 Controller unit
Methodology	UVM
End Client	No End Client
Responsibilities	<ul> <li>Developed intermediate Scoreboard to check data, address, and command propagation</li> <li>Developed User interface Driver and Monitor</li> <li>Developing feature testcases</li> <li>Developing functional cover points and assertions</li> <li>RTL Debugging of test failures and bug reporting</li> </ul>
Language and tools used	System Verilog, Questa Sim

# PROJECT: - 2

Project	Verification of 256-bit AES Engine block
Methodology	UVM
End Client	No End Client
Responsibilities	<ul> <li>Developed AES model</li> <li>Developed various testcases to verify the block</li> <li>RTL Debugging of test failures and bug reporting</li> </ul>
Language and tools used	System Verilog, Questa Sim

# **EXTRA CURRICULAR ACTIVITIES:**

- Attended a Three-day workshop on open-source controller board at L.J Polytechnic (11, july,2016).
- Attended a one-day workshop on Engineering's Day Celebration Navic & Gagan Application & Technologies (4, October, 2019).
- L.J. INNOVATION VILLAGE-2016 participated showcased a project making a LED bulb.
- L.J. INNOVATION VILLAGE-2019 participated showcased a project on making a Pani puri vending machine.
- Engineering day celebration-2018 at L.J. Institute of Engineering and Technology has been a second runner up for the event Bid-wars.
- National Level Edu tech Fest has participated in general Quiz at L.D college of Engineering.

# **DECLARATION:**

To obtain a position that will allow me to utilize my technical skills experience and willingness. To learn in making an organization successful.

**PRAKASH**