RESUME

NAGULA PRUTHVI RAJU

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CAREER OBJECTIVE:

To obtain a challenging position that offers opportunity for advancement and personality development and fully utilizes in an environment, where I would learn and improve myself and thus be an asset to the organization.

PROFESSIONAL SUMMARY:

- Trained in Physical Design domain from April-2022.
- Hands-on experience using Synopsys ICC2 for PNR implementation.
- Hands-on experience using Synopsys Design Compiler for Synthesis, Prime Time for STA.
- Involved in 2 block level design implementations (Netlist to GDSII), 1 block level design implementation (RTL to Gate-level netlist)
- Good knowledge in Floor plan, Power plan, Clock Tree Synthesis, Routing, Crosstalk analysis, EM/IR drop Analysis and Static Timing Analysis.
- Hands-on experience in complete backend flow – Logical Synthesis, Floor Planning, Placement, Clock Tree Synthesis and Routing, ECO.

EDA TOOLS:

IC Compiler-2	: Floor plan, Place and Route, Clock Tree Synthesis
Design Compiler	: Logic Synthesis
Prime Time	: Static Timing Analysis

PROJECT PROFILE:

Objective: Responsible for Synthesis using Synopsys design compiler.

Role: Import the design through specified libraries, read design, define design environment, set design constraints, optimize the design, analyze and resolve the design problems and report generation.

PNR PROJECT-1:

- Technology : 28nm
- Tool : IC Compiler 2.
- Std cell count : 550k
- Macros : 9
- No. of Clocks : 1
- Frequency : 1 MHz

Role:

Responsible for taking the design through floor planning, placement, CTS and Routing.

Challenges:

- To reduce Congestion, timing violations, EM/IR.
- Fixing Setup and hold violations.

PNR PROJECT-2:

- Technology : 28nm
- Tool : IC Compiler 2.
- Std cell count : 800k
- Macros : 26
- No. of Clocks : 1
- Frequency : 800 MHz

Role:

Responsible for taking the design through floor planning, power plan, placement, CTS and Routing.

Challenges:

- Changing the floorplan to check the congestion to its minimum value.
- Checking and fixing antenna violations and DRC violations.

SKILL SET:

Languages : TCL Scripting

EDA Tools : Synopsys (Design Compiler), IC Compiler 2, Prime time

Operating Systems : Windows, Linux.

ACADEMICS:

Course	Institution name	University/Board	Year of pass	Percentage
B. Tech (ECE)	Sree Chaitanya College of Engineering, Karimnagar.	JNTUH	2022	61%
Diploma (ECE)	Government Polytechnic, Nizamabad	SBTET	2018	76.6%
SSC	Surabhi High School, Gangadhara	SSC	2015	92%

DECLARATION:

I do hereby declare that the information and particulars furnished above are true to the best of my knowledge.

Place : Hyderabad

Date :

(**NAGULA PRUTHVI RAJU**)