Navya Vemula

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Career Objective

Seeking a career as a physical design engineer with the opportunity to work with teams on floor plan , place and route, Clock distribution and DRC/LVS Violations on the chip and contibuting to the significant growth of the organization.

Core Competancy

- Analyzing the Gate level Netlist through STA methodologies.
- Physical Implementation from Netlist to GDS, including floor planning, Placement, Clock Tree Synthesis, Placement, Optimization, Routing, Parasitic Extraction, STA.
- Create the floor plan from block diagram and minimize the IR drop voltage by changing the power grid values.
- Place and Route the Standard cells by APR tool and verifying the Optimization and Legalization of the design.
- Timing closure by adding the net parasitic of the design to meet the setup and hold violations.
- Familiar with scripting languages like TCL, perl, Linux and knowledge on digital logic design.
- Hands on experience on EDA tool from synopsys ICC shell to drive block PnR and timing closure.
- Good hands on experience with physical verification of DRC,LVS, Antenna, DFM and also other reliability check IR drop map and Congestion Map.
- Basic knowledge on CMOS, MOSFET and FINFET.

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2020**

Hyderabad Institute of Technology and Management, with 7 CGPA

2016

Narayana junior college, with 89.9 %

SSLC **2014**

Keshava Reddy concept school, with 9.8 %

Domain Specific Project

RV skills center for emerging technologies

Graduate Trainee Engineer Sep-2022 to Feb-2023

Lakshya design

Description

lakshya is a sub-system project where it helps to learn the real time problems that we face in the industry while doing floor plan, place and route , STA, Physical verification, DRC violations, analyze the timing reports and Antenna and Xtalk.

Tools

ICC2 shell from Synopsys. With the help of this tool we can run the TCL script and GUI of the design, analyze, modify, check the errors in the design with the help of icc2 commands

Challenges

- Design the floor plan such that all the macros meet the pin requirements. Power grids should be such that IR drop is minimum. Check the DRC errors and timing violations report
- Spare cells are added accordingly should to be checked. Legalization of the design have to be successful if not rerun. check the legality, Utility and timing violations.
- Check the standard cells placement sometimes the cells are not placed after placement. Check the DRC error and timing violations they may have reduced from floor plan to placement
- Check the congestion and reduce it to smaller values by calculating the overflow in the macros. In CTS run check the timing violations and fix it. In routing antenna and Xtalk.

B.E / B.Tech Academic Project

Hyderabad Institute of Technology and Management

IOT Based Smart Wheel Chair

Description

A smart wheel chair contains the connections between the sensors, tracking and detection. It includes multiple technologies and applications used to provide a easy life to the physically handicapped and old age people. Monitoring and tracking by GPS

Tools

Embedded C ,MPU6050, Raspberry Pi, IR sensor , GPS module, L293D Motor driver, DC motors

Challenges

- GPS module to interface with Raspberry pi to get the location of the wheel chair. To get the IOT page and the SMS to the mobile was the challenge. Configurating the motor driver directions and the distance it has to stop for obstacle.