Thejaswini Konda

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Career Objective

To excel as Physical Design Engineer and hold up a challenging position in semiconductor industry through dedication and ensure the success of personal as well as organizational goals.

Core Competancy

- Acquired in depth knowledge and hands on experience in working on different stages of Physical Design flow such as Floor plan, power plan, APR, CTS and Routing.
- Comprehensive understanding of Static Timing Analysis concepts such as Setup and Hold violations , AOCV and CRPR.
- Familiar with all the input files and library used for Physical design flow such as .lib, .tf, tluplus, .sdc and .lef.
- Hands on experience in working with Synopsys tools, IC Compiler 2 for APR and Prime Time for STA
- Performed Block level Physical design flow from Netlist to GDS2 for design with 34 macros and 38k Standard cell count.
- Decent knowledge in understanding TCL scripts.
- Comprehensive understanding of CMOS technology ,MOS device , digital and analog electronics.

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2017**

Vaagdevi Institute Of Technology & Science, with 70 %

Diploma **2014**

Govt Polytechnical College, with 76.04 %

SSLC **2011**

St.Joesph High School , with 76 %

Domain Specific Project

RV-VLSI Design Center

Graduate Trainee Engineer Aug-2022 to Nov-2022

FLOOR PLAN AND POWER PLAN

Description

Implemented Block level Physical design with the following specification. 4onm technology, clock frequency: 1GHz, Standard cell count:38k, Hard Macros:34,power Budget 600mW, Area:4.2Sq mm.

Tools

Synopsys IC Compiler II

Roles and Responsibilities

- Designing a good Floorplan by placing all macros along the core periphery as per the data flow diagram and using Fly lines, providing a contiguous core area for Standard cells.
- Building a good Power plan to meet specified IR drop of 5% for the supply of 1.1V. Understanding and fixing all the DRC and connectivity errors such as floating wire &missing vias
- Fixing congestion by providing channel spacing, creating proper placement and routing blockages by analyzing global route congestion map.
- Ensuring proper insertion of Physical only cells such as Boundary cells and Tap cells.

RV-VLSI Design Center

Graduate Trainee Engineer Aug-2022 to Feb-2023

CLOCK TREE SYNTHESIS AND ROUTING

Description

Building a clock tree for a block with placed standard cells for the minimum skew of 5-10% on clock period and analyzing pre & post-CTS clock reports Performed the last stage of PNR flow i.e Routing &insertion of antenna diode, DRC & LVS checks.

Tools

Synopsys IC Compiler II

Roles and Responsibilities

- Understanding Classic CTS flow and Concurrent clock and (CCD) flow , tools behavior while CTS to meet target slew , Min/Max latencies and fixing timing violations.
- Understanding NDR rules for clock nets , cross talk effects ,signal integrity & antenna effects. Analyzing timing reports after CTS with propagated clock , fixing setup &hold slack
- post CTS routability checks & fixing DRC violations for short, open nets , different net spacing .Analyzing setup & hold violations , clock tree ,latency & skew.
- Understanding routing flow & antenna effect. Fixing antenna violations by inserting antenna diodes and other DRC and LVS errors

B.E / B.Tech Academic Project

Vaagdevi Institute Of Technology & Science

Energy Efficient Design Of Novel Line Decoders in VLSI

Description

This work develops a mixed logic design methodology for line decoders .combining gates of different logic to the same circuits ,in an effort to obtain improved performance compared to single style design

Tools

MICROWIND ,DSCH

Challenges

- All these decoders have reduced transistor count and full swinging capability as compared to their conventional CMOS decoders . all the designed circuits present a significant decrement in power dissipation ,propagation delay ,area.