Kollu Bhumika
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Career Objective

Seeking a position of Physical Design Engineer enabling me to utilize my technical skills that offers mutual growth and advancement opportunities.

Core Competancy

- Worked on ASIC Physical Design flow involving Floorplan, Powerplan, IR drop analysis, Placement, Clock Tree Synthesis & Routing.
- Worked on Static Timing Analysis reports to analyze which timing path is failing or meeting the goal, setup & hold violation fixes.
- Analyzed timing reports of Pre-Layout STA and Post-Layout STA, fixed timing violations.
- Understood the design constraints and designing Floorplan using Flylines to have contiguous core area for standard cells.
- Designed a good power plan to meet the IR drop specified while ensuring no floating pins in the design.
- Building clock tree & data path optimization, connecting CLK pin of each sequential element to the clock nets such that clock skew is minimized.
- Tcl scripts have been understood, modified & also built to extract the timing path, WNS, TNS, number of total violations and core utilization.
- Hands on Experience in APR Tool: IC Compiler II - Synopsys and STA Tool: Prime time.
- Good knowledge in Logic Design Concepts, CMOS, Semiconductor Theory and Basic Electronic Devices.

Education Details

Advanced Diploma in ASIC Design **2022**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**
Sri Venakateswara Engineering College for Women, with 8.26 CGPA

2018
Sri Chaitanya Jr. College, with 94.6 %

SSLC **2016**
Rayalaseema Public School, with 93 %

Domain Specific Project

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Jun-2022 to Sep-2022

Analysis of Timing Reports (STA)

Description

Analyzed timing reports of pre-layout and post-layout STA stages for Flip flops and Latch based timing paths considering Cell Delays, Uncertainty, CRPR, Clock Skews, OCV while ensuring that the design satisifying specified timing constraints.

Tools

Synopsys PrimeTime, Synopsys IC Compiler II

Challenges

- As STA tool considers every path in design to be true, this might result in false timing paths being reported, to eliminate this false timing specific constraints were added.
- Applying timing exceptions for multicycle paths, minimum & maximum delay paths with caution, as true violations can get suppressed owing to incorrect constraints.
- Understood how parasitics have an effect on pre-layout and post-layout STA stages. Analyzed how some violations are reduced in later stages for the same timing paths.

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Jul-2022 to Sep-2022

Design of a SOC physical design block

Description

Planning and designing of SOC physical design block to be integrated into a full chip. Overview : 40nm technology, Supply-1.1v, Clock Frequency-833 MHz, Area-4.2 sq.mm, Macros-34, Standard Cells-41k, Power Budget-600mW, IR Drop-55mv, Metal layers-7.

Tools

Synopsys IC Compiler II

Challenges

- Designing Floorplan keeping one group of macros together without blocking any ports using Flylines, covering the edges of core boundary with the macros.
- Power plan to meet the IR drop required by fixing perfect values for parameters of metal layers, resolving DRC and connectivity errors.
- Performing multiple iterations of place opt, tried different floorplan expirements to control congestion, setting blockages for spacings between macros.
- Creating metal routes in the design, fixing max transition violations using buffers, antenna violations using metal jumpers and antenna diodes.

B.E / B.Tech Academic Project

Sri Venakateswara Engineering College for Women

Fingerprint Based Vehicle Starter

Description

Developing a model to increase the security level of vehicles from day-to-day threatens and provide a hassle free way to start/stop vehicle engine, which allows only authorized users.

Tools

Arduino UNO, GSM module, Fingerprint Sensor

Challenges

- Finding a way to alert the vehicle owner, when the vehicle is being theft.