SAYED KHAJA ALI MOHIDDIN

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CAREER OBJECTIVE:

To pursue a challenging career in an esteemed organization to enhance my knowledge and excel my skills for making successful contribution to the organization.

ACADEMIC QUALIFICATION:

ACADEMICS	UNIVERSITY/COLLEGE SCHOOL	ACADEMIC YEAR	PERCENTAGE
B. Tech (ECE)	**Gayatri vidya parishad college for degree and pg courses, Visakhapatnam**	**2019-2022**	**72.4%**
Diploma	**Sir c.r.reddy polytechnic, Vatluru**	**2016-2019**	**80.04%**
SSC/10th	**Sri chaitanya techno English medium school, Mandapeta**	**2015-2016**	**9.2**

SOFT SKILLS:

- Excellent written, presentation & verbal communication skill.
- Self-motivated to produce results in a fast and dynamic environment.
- Effective performer as an individual or in a team.
- Able to take proper and quick decision.

TECHNICAL SKILLS:

- Good understanding of **VLSI design flow** and **Physical Design Flow, CTS, Routing.**
- Knowledge of flows such as **Synthesis Flow**, **Floorplan** to **GDS-II Layout/ PNR** flow.
- Thorough knowledge of **Static Timing Analysis** and **Parasitic Extraction**.
- Good knowledge of **Digital Electronics, Basic Electronics, CMOS Fundamentals**. • Good awareness of **ASIC Flow** & Familiar with files like **.V, .lib, .sdc, .lef**
- Basic knowledge of understanding **TCL.**

TOOLS AND LANGUAGES

- Operating system : Linux, windows
- Scripting Language : TCL, TCSH
- Synthesis Tool : Design Compiler (Synopsys)
- PNR Tool : IC Compiler II(Synopsys)

TECHNICAL TRAINING: Sumedha IT Hyderabad

PROJECTS

Project-1: Details
Location: SUMEDHA IT (Hyderabad) Training
Project : ALU

Targets: Logic Synthesis and STA
Description:

- Technology : 28nm
- Operating conditions : 0.72v, -40c
- Wire load model : Zero wire load model
- Clock frequency : 500 MHz

Tools: Design Compiler (Synopsys) **Challenges:**

- Faced issues in analyses stage of RTL Files.
- Design constraints like clocks, input delay, output delay,clock uncertainty for design under analysis (DUA)
- Sanity checks performed after Synthesis.
- Optimizing the design with respect to performance. • Understanding the reasons for violations.

Project-2: Details
Location: SUMEDHA IT (Hyderabad) Training
Project: RP_TOP_TOP

Targets: Logic Synthesis and STA
Description:

- Technology : 28nm
- Operating conditions : 0.72v, -40c
- Wire load model : Zero wire load model
- Clock frequency : 400MHz

Tools: Design Compiler (Synopsys) **Challenges:**

- Faced issues in analyses stage of RTL Files.
- Design constraints like clocks, input delay, output delay,clock uncertainty for design under analysis (DUA)
- Sanity checks performed after Synthesis.
- Optimizing the design with respect to performance. • Understanding the reasons for violations.

Project-3: Details
Location: SUMEDHA IT (Hyderabad) Training
Project: RT_TOP_TOP

Targets: PNR (Floor planning & Power planning & Placement & CTS & Routing)

Description:

- Technology : 28nm
- Macro : 6
- Standard cell count :63853 (seq-11861, comb-51992)
- Area : 488097.792
- Supply voltage : 0.81v
- Metal layers : 9
- Number of ports 426
- Frequency : 430MHZ

Tools: IC Compiler II (Synopsys)

Challenges:

- Rectangle floorplan with lots of congestion and utilization of around 75%.
- Sufficient channel spacing provided around macro to avoid Routing issues.
- Resolved floating vias and shapes.
- Fixed timing violations after placement.

Role : Performing sanity checks, Design import , Floor Plan , Power Plan , Placement , Adding filler cells, Timing Analysis.

ACADEMIC PROJECT :

Title : Design of responsive website for ECE department.

Team Size : 4 members (Team Leader).

PERSONAL INFORMATION :

- Name : Sayed khaja ali mohiddin
- Father's Name : Sayed ahmed alisha
- Date of Birth : 12/08/2000
- Nationality : INDIAN
- Marital Status : Un-Married
- Languages known : Telugu, English.
- Address : 34-12-10 gandhi nagar 4th street Mandapeta-533308

DECLARATION:

I hereby declare that the above written particulars are true to the best of my Knowledge and belief

Place:Mandapeta

Date : 12/1/2023