KESHAV PRAKASH

SUMMARY OF QUALIFICATIONS:

- Overall 3.2 years of experience in VLSI -Design Verification.
- Good working knowledge on System Verilog- Design and development of re-usableverification environments, SV Assertions, Functional Coverage and Code Coverage Analysis.
- Good working knowledge on UVM verification methodology along with RAL modelcalculations.
- Gained Knowledge in Intel IOSF and SAOLA Environment.
- Good debugging skills in Functional based Verifications.
- Comprehensive Knowledge on scripting languages (PYTHON & PERL).
- Basic knowledge on Cache Coherency, Virtual Memory concepts, TLB (TranslationLookaside Buffer) and Pipelining in computer architecture.

EXPERIRNCE:

1. Name of the company : CGI information & systems

   Total experience : 01Aug2019-10OCt2021

2. Name of the company : Mobiveil technologies

   Total experience : 16Feb2022-

   29NOV2022

3. Name of the company: Excelmax technologies

   Total experience :5Dec2022-Till date

TECHNICAL SKILLS:

HDL/ HVL Skills	Verilog /System Verilog
Programming language	C
Scripting	Perl and Python
Verification Methodology	UVM (universal verification methodology)
Bus Protocols	USB.1/3.2, APB, AXI4-Lite, MIPI-Uni Pro 1.6 & 1.8.
Operating Systems	Windows and Linux
Tools	Synopsys VCS-Verdi, DVE, Mentor Graphics- Modelsim & Questasim

PROJECT EXPERIENCE:

Project Name: AMD USB	**Duration: JUN2022–TILL**

Role	**Verification Engineer**

Project Summary	The main aim of this project is to verify USB Caching Agent Test Card(CCAT) module which serves as application layer of Type 1 USB device. The verification is done to verify 'USB' and features of DUT for register write/read and data traffic respectively. The complete design consists of a USB IP (Physical, Data Link and Transaction Layers) integrated with CCAT.
Languages	UVM
Tools	Cadence Xcelium
Responsibilities	• Study of USB and CCAT (DUT) specifications. • Executed directed test cases which generates .Write and Read transactions with different opcodes from the DUT to Host. • Executed the directed tests cases generating snoop requests from Host and verify the response from the DUT.

Project Name: USB3.1/3.2	**Duration: AUG 2019– OCT 2021**
Role	**Verification Engineer**
Project Summary	The main aim of this project is to verify link and protocol layers of USB subsystem of PCH IPS.
Languages	OVM
Tools	VCS-VERDI, DVE
Responsibilities	• Generated the retro test cases of USB. • Validating Features of USB at SOC level. • Worked in USB3/3.1/3.2 as well both in XHCI &XDCI Controller • Debugging of failure across variants in 7nm and 10nm • Build USB SOIX Low power testcases • Reducing Simulation time in USB testcases.

Project Name: USB3.1/3.2	**Duration: Dec - 2020 to May - 2021**
Role	**Verification Engineer**
Client	Intel

Project Summary	The main aim of this project is to verify link and protocol layers of USB subsystem.
Languages	OVM
Tools	VCS-VERDI, DVE
Responsibilities	• Maintained weekly summary of regression. • Debugged RTL, BFM, Power management and various generatorissues related. • Debugged USB3/PIPE/TBT/MOAT Tracker and link level issues. • Involved in developing testcases and test sequences in XHCI • Worked closely with architects and design engineers to enhancethe environment. • Created focused and random test sequences as per the test plan. • Debugged feature regressions to find RTL bugs, filed and trackedbug fixes to ensure timely closures. • Analyzed Functional coverage to tweak constraint space and added New test to ensure proper regression coverage • Debugging of failure across variants in 7nm and 10nm • Reducing Simulation tie in USB testcases.

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Project Name: MIPI-UNIPRO	**Duration: January - 2020 to Nov - 2020**
Role	**Design and MATLAB Verification Engineer**
Project Summary	The main aim of this project is to verify stack layers of UniPro and DME (Device Management Entity).
Languages	System Verilog/ UVM
Tools	Verdi VCS
Responsibilities	• Generating sequences for stack layers (Transport layer & DatalinkLayer). • Generated test cases for Initiate, Hibernate, Power Mode and AFC(Acknowledge Frame Coding). • Successfully debugged error injection test cases using callback method.

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Project Name: APB On-Chip & Off-ChipCommunications	**Duration: November 2019 to December 2019**
Role	**Design and Verification**
Client	AMS

Project Summary	The main aim of this project is to verify APB On-Chip communication and Off-Chip communications.
Languages	System Verilog/ UVM
Responsibilities	• Generated Verification Plan for VIP based APB & SPI covering different control signals of APB along with PSLVRR and other corner cases. • Developed class-based Verification IP in UVM. • Developed RAL based sequences and sequencers for SPI. • Verified RTL module using System Verilog/UVM. • Achieved Functional coverage and Code coverage (97%).

ADVANCED TRAININGS/ DEVELOPMENT PROGRAM:

- Certification course on System Verilog and UVM (Universal Verification Methodology).

PERSONAL DETAILS:

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