Yoganand PNVSSP

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Tirupati-517507, Andra Pradesh

Career Objective

A passionate physical design trainee seeking a challenging, accountable role that allows me to use my technical expertise that provides the opportunity for my career advancement through making a significant contribution to the organization's mission

Core Competancy

- Comprehensive knowledge of the ASIC flow and practical expertise with the APR flow, which includes floor planning, power planning, placement, CTS, and routing
- Conversant with a variety of STA principles, including resolving Timing Violations, CRPR, AOCV, Slack, Timing Constraints, PVT Corners, Modes, and Clock Skews.
- Developed a Floorplan with Contiguous core area, good Utilization and appropriate Channel Spacings with the help of Flylines and Dataflow Diagram.
- Tweaked the width, spacing, and pitch of the metals to create a power network free of physical DRC errors?0?2while also making sure to achieve the required IR drop.
- A Legalized Placement block was created with minimal Congestion, no floating standard cells, no DRC errors by adding of Placement and Routing Blockages, Keepout margins
- Implemented and compared two CTS flows Classic and CCD for better timing. Performed routing and fixed DRC errors, LVS Shorts, Antenna violations using Jumper and Diode.
- Generated Timing Reports at every stage of PD flow and analyzed the TNS, WNS, delays, clock skew, transitions violations, CRPR, network latency and source latency
- Working knowledge of the Synopsys PrimeTime and IC Compiler II tools.
- Solid grasp of CMOS, Network Analysis, Basic electronics and Digital Logic Design concepts.
- Familiar with basic Linux, PERL, TCL and Verilog syntax and commands and has good analytical approach towards problem solving and troubleshooting

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electrical and Electronics** **2021**

Sree Vidyanikethan Engineering College, with 84.40 %

2017

Sri Chaitanya Academy Junior College, Tirupati, with 96.4 %

SSLC **2015**

Little Angels High School, Tirupati, with 98 %

Projects worked on

Cognizant Technology Solutions Client: CVS, British Telecommunications

Programmer Analyst Jul-2021 to Jul-2022

ServiceNow Development

Description

Worked as an integral and important member of the ServiceNow Developers team in the project. Handled Client instances single-handedly during upgrades to the latest versions and developed bug fixes to rectify anomalies in them.

Tools

ServiceNow

Challenges

- Has worked as the primary point of contact for the development of a new internal instance for the client
- Completely developed the UI Scripts, Client Scripts and Business rules for internal instance of the client
- Worked actively during the version and patch upgrades of ServiceNow and resolved upgrade issues

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Domain Specific Project

RV VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Oct-2022 to Feb-2023

Floorplan, Powerplan and Placement Implementation

Description

Block level implementation of Lakshya Subsystem: Technology-40nm, Supply voltage-1.1V, Area-4.2 sq. mm, Power budget-600mW, Max. IR drop (VDD+VSS)-5% , No. of macros-34, No. of Standard cells-38000 (approx), No. of Metal layers-7.

Tools

IC Compiler II - Synopsys

Challenges

- Designing a Floorplan by determining macro placement as per dataflow diagram, flylines and using the macro guidelines in order to achieve contiguous core area and good utilization.
- Building a Powerplan to maintain power network connectivity and IR drop. Also ensuring that there were no missing vias, floating wires and power-ground DRC violations.
- Creating a placement block by inserting pre-placement cells, placement constraints, sufficient spacings in order to control the congestion and DRC violations obtained.
- Analyzing of timing reports and identifying the cause in the timing path for which it's being violated and observing the WNS, TNS at various stages of the flow.

RV VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Oct-2022 to Feb-2023

CTS and Routing Implementation

Description

Block level implementation of Lakshya Subsystem: Technology-40nm, Supply voltage-1.1V, Area-4.2mm, Power budget-600mW, Max. IR drop (VDD+VSS)-5% , No. of macros-34, No. of Standard cells-38000 (approx), No. of Metal layers-7

Tools

IC Compiler II - Synopsys

Challenges

- Performing clock tree synthesis and optimization using classic, CCD flows and analyzing the tool's behavior by comparing the timing reports in both the flows.
- Analyzing clock tree to achieve minimum insertion delay and skew . Also checked and rectified for the clock DRC errors.
- Rectifying the LVS errors like shorts which were obtained post routing by removing the overlapped routes and doing manual routing wherever necessary
- Analyzing and resolving the antenna violations by inserting the metal jumper and the diode into the layout.

RV VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Sep-2022 to Oct-2022

Analysis of the Timing Reports (STA)

Description

Generation of timing reports that include setup and hold slack calculations for flip flops and latch-based paths working at various conditions, reports are analyzed considering OCV, uncertainty CRPR, and timing exceptions (multi-cycle, false paths)

Tools

Synopsys PrimeTime, IC Compiler II - Synopsys

Challenges

- Exploring the PrimeTime tool and commands related to the tool by analyzing their usage and functionalities
- Understanding the timing reports at every stage of PD flow, finding the cause of timing violations and how some of the violated paths are being reduced in later stages.
- Identifying the violations based on timing exceptions such as false paths, multi-cycle paths and specifying them in the SDC file.
- Analyzing the effect of clock skew, CRPR, OCV timing derates for all four different timing paths from the timing reports.

B.E / B.Tech Academic Project

Sree Vidyanikethan Engineering College

HOME AUTOMATION AND SECURITY SURVEILLANCE SYSTEM USING RASPBERRY PI

Description

Solution for residential security surveillance system and automation with monitoring the achievement of the following objectives: 1. Security solution for closing/opening the main entrance 2. IOT based Energy management solution for lighting load

Tools

Hardware: Raspberry PI 3 Chip, LDR, MCP3208, L293D Motor driver, AC Dimmer, Servo motor Software: Raspbian OS, VNC Viewer Language: Python 3

Challenges

- Getting familiar with the Raspberry PI technology and the Raspbian OS. Arriving at the accurate face detection algorithm for locking and unlocking the entrance. Precise control of the ambient lighting and security using affordable equipment.