Physical Design Trainee

Mahesh Narbolikar

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Career Objective

A motivated individual seeking for a responsible position as an entry level Physical Design Engineer which will qualify me to bring the best out of my knowledge and experience in achieving growth and development of myself as well as the organization.

Core Competency

- Acquired extensive knowledge in ASIC PD Flow involving Floor Planning, Power Planning, Placement, Clock Tree Synthesis and Routing.
- Hands-on-experience on the industry tools such as Synopsys IC Compiler II for APR flow and Prime Time for Static Timing Analysis.
- Placement of macros based on data flow lines, ports and also providing with a required routing and placement blockages in the floorplan.
- Generated an optimized placement block with controlled congestion through various iterations of channel spacing and modifying floorplan.
- Knowledge in interpreting timing reports, fixing Setup and Hold violations and the concept of adjusting the clock skew in order to fix setup and hold violations.
- Dealing with Timing Paths of various PVT corners, Modes, Scenarios, concept of CRPR and also understanding of the constraints to define the False and Multi-Cycle Paths.
- Fair knowledge on Signal Integrity issues like Crosstalk, Reliability issues like Electromigration and Antenna effect.
- Analysing and fixing of the DRC and DFM issues.
- Comprehensive knowledge on the concepts of STA, Logic Design and CMOS Theory.

Education

RV-VLSI and Embedded systems Design Centre, Bengaluru Sept 2022 - Feb 2023
ADVANCED DIPLOMA IN ASIC DESIGN - PHYSICAL DESIGN

JSS SCIENCE AND TECHNOLOGY UNIVERSITY, Mysuru Aug 2018 - July 2022
Bachelor of Electronics and Instrumentation Engineering
CGPA- 8.16

SBR PU College, Kalaburagi June 2016 - Mar 2018
Senior Secondary
Class 12th - 88.33%

SBR PUBLIC SCHOOL, Kalaburagi June 2015 - Apr 2016
Class 10th - 93.12%

Domain Specific Project

BLOCK LEVEL PHYSICAL DESIGN IMPLEMENTATION

Description

A block level Implementation of a design at 40nm technology node with a list of 34 Macros, 40K+ Standard Cells, operating at a frequency of 833 MHz and a nominal supply voltage of 1.1V with a Target IR drop of 5% and an assigned Power Budget of 600mW

Tools

- Synopsis IC compiler II for APR flow
- Synopsis Prime Time tool for STA

Roles and Responsibilities

- Understood the design specs and designed the efficient Floorplan by ensuring a contiguous area in between the macros, also added few Placement and Routing blockages through several iterations
- Built the Power plan to meet the IR drop, EM requirements and ensuring there are no floating wires, missing vias and no DRC violations
- Placement of standard cells and Congestion analysis over the design, also adding few partial blockages to control congestion at Standard cell area.
- Understood the essence of STA and analysed the Timing reports for effects of Clock skew, CRPR and OCV.
- Building a well-balanced clock tree, meeting the target skew and fixing of Setup and Hold violations.
- Performing signal routing and also fixing the DFM violations.

Challenges Faced during project

- Designing of a proper floorplan by considering its effects on the further steps of the PD flow
- Overcoming congestion problem by keeping it under control with respect to global route congestion.
- Analysing the timing reports and debugging the cause for setup and hold violations and working for the slack to be under control.
- Overcoming with the Antenna Violations and providing them with a suitable fix with the help of Metal Jumpers and a Diode.

Final Year Academic Project

ARDUINO BASED VOICE CONTROLLED WHEELCHAIR

- Operation of an android app through which we can operate a movement of wheel chair using android device.
- Implementation and usage of the voice-based system so that user's voice acts as an input to control the mobility of wheelchair.
- Design and development of pulse and temperature monitoring system

Tools

- Arduino IDE
- AMR Voice
- Bluetooth RC controller app

Internship and Certifications

Company – MITEL Jan 2022 – July 2022

INTERNSHIP

- Worked on the CMG Product.
- Hands on working with .NET Framework
- Trouble Shooting Techniques
- Analysed the root cause for few Bugs and tried reproducing them and gave them some appropriate fixes

Certification - Won the Fury Road event by CYBERIA (IEEE)