PORANKI MEGHANA poranki.meghana@gmail.com
(+91)8639469899

PROFESSIONAL TRAINING

ADVANCED VLSI DESIGN AND VERIFICATION course at Maven Silicon VLSI Design and Training center, Bangalore from November 2021 to June 2022

EMPLOYMENT DETAILS

Worked as **Design Verification Engineer** at BITSILICA PVT LTD, Hyderabad from ***JUNE 2022 t*o *APRIL 2023***

PROJECT DETAILS

1. **Design Verification Engineer BITSILICA PVT LTD June 2022– April 2023**
   Theoretical Knowledge on AMBA- [APB, AXI], UART, I2C
2. **Advanced VLSI Design Verification Training Maven Silicon March 2022-May 2022**
   Project: Router 1*3- RTL design and Verification
   - HDL: Verilog
   - HVL: System Verilog
   - TB Methodology: UVM
   - EDA Tools: Questasim

   Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.
   Responsibilities:
   - Architected the block level structure for the design
   - Implemented RTL using Verilog HDL.
   - Architected the class based verification environment using System Verilog
   - Verified the RTL model using System Verilog.
   - Generated functional and code coverage for the RTL verification sign-off
   - Synthesized the design.

TECHNICAL SKILLS

- Digital Electronics, Verilog [HDL], **System Verilog [HVL], System Verilog Assertions, UVM [Methodology]**.
- **Protocol** Knowledge **AMBA-APB, AXI, UART,I2C**
- Scripting Language: Perl
- EDA Tool: Mentor Graphics- QuestaSim
- Operating System: Linux
- Core Skills: RTL coding Using Synthesizable constructs of Verilog, FSM based design, and Assertion based verification using system Verilog Assertion

EDUCATION

Lingayas Institute of Management and Technology, Vijayawada 2021

- B-Tech in Electronics & Communication Engineering **(ECE) (CGPA: 7.31**

Sri Chaitanya Junior College 2017

- Board of Intermediate Education Certificate Examination **(Percentage: 83.5%)**

Sri Chaitanya School 2015

- Secondary School Certificate (AP) Examination **(CGPA: 7.5)**

ACHIEVEMENTS / EXTRA CURRICULAR ACTIVITIES

- Participated in circuitrix conducted by NRI Institute of Technology
- Participated in VLSI Technical online Quiz

PERSONAL INFORMATION

- Father's Name : P. V. Krishnam Raju
- Mother's Name : P. Prasanthi
- Date of Birth : 02 August 2000
- Languages known : Telugu, Hindi, English

DECLARATION:

I hereby declare that the details furnished above are true to the best of my knowledge.

(P. Meghana)