Shivam Gautam

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OBJECTIVE

I would like to work with a team in a challenging and competitive environment where I could improve my knowledge, capabilities and put them to use for the development of the organization.

EDUCATION

- **Motilal Nehru National Institute of Technology, Allahabad, Prayagraj** — Prayagraj
  Master of Technology - Microelectronics and VLSI Design : CPI: 8.6 — *2021-present*
- **Gautam Buddha University, Greater Noida , Uttar Pradesh** — Greater Noida
  integrated (B.Tech + M.Tech)-Electronics & Communication; CGPA: 8.6 — *2016 - 2021*
- **S.D Public School** — Muzaffarnagar, Uttar Pradesh
  12^{th} CBSE; Percentage: 86.6% — *April 2014 - May 2015*
- **S.D Public School** — Muzaffarnagar, Uttar Pradesh
  10^{th} CBSE; CGPA: 9.0 — *April 2012 - May 2013*

SKILLS

- **Languages** : C, Verilog, Tcl
- **Tools** : Cadence Virtuoso, Xilinx Vivado,Silvaco Atlas, EDEN(Intel specified)

PROJECTS

- **Internship Project:Timing and Power Optimization of Functional Unit Block in High Speed Core**: *Ongoing*
  - The core is periodically advancing towards new challenges with shrink in transistor size and progress of semiconductor industry . Transistor technology advancement has given the superior platform for fabricating high-performance multi-core processors with several innovative features . With every new generation core designing there comes the requirement to be developed to meet certain targets. From designer point of view, the new challenges in present day projects includes more stringent timing convergence and rigorous power reduction than in the previous studies.
  - Tools used: EDEN, TANGO and DUET.
- **Masters Project: Design and Simulation of junctionless vertical TFET used as transducer for sensing gases using Silvaco Atlas.**:
  - The objective of the project is to design and implement the junctionless vertical tunnel field-effect transistor (JL-VTFET) with catalytic metals as gate contacts is used for gas sensing applications.
  - An architecture for n-channel JL-VTFET with Palladium (Pd) as gate metal is analyzed for Hydrogen sensing, while Cobalt (Co) and Molybdenum (Mo) metals as gate contacts are analyzed for Ammonia sensing.
  - Characteristics of the proposed structure are studied considering the electric field, surface potential,and energy bandgap graphs concerning adsorption of gas molecules, using Silvaco ATLAS TCAD simulator. Simulation results of JL-VTFET with 50-nm gate length show good sensitivity calibrations and high Idon/Idoff ratio for Co, Mo and Pd as gate metals, respectively.
- **Masters Project: Design and simulation of a traffic light controller design using Mealy and Moore FSM technique.**: *Dec 2021-Dec 2021*
  - In this project we designed a traffic light controller using both the art of FSM technique via. Mealy and Moore's machine using module and testbench. It is used to determine the better PPA (power, performance, and area) of the particular design.
  - After finding the number of states for each of the machines, the state model is designed.
  - Tools used: Xilinx Vivado and Synopsys Design Compiler
- **Maters Project: Implementation of research paper of Analysis of Noise Immunity for Wide OR Footless Domino Circuit Using Keeper Controlling Network using cadence.**:
  - Due to high-speed and low area, domino circuits are used in a variety of applications such as comparator, adder,MUX, memory, microprocessor, and adder. In this project, a keeper controlling network is used to improve the noise immunity and performance for wide fan-in OR footless domino circuit. In this design, the keeper controlling network controls the keeper transistor. The network itself consists of an NMOS transistor, which acts as a switch and inverter chain. This network turns OFF the keeper transistor at the start of evaluation phase to enhance the speed of the domino circuit. Similarly, it turns ON the keeper transistor, when all inputs areat low voltage in the evaluation phase to enhance the noise immunity

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AREA OF INTEREST

- Backend Memory Circuit Design
- Understanding about Static Timing Analysis
- MOSFET's, CMOS Technology
- Physical design(Data Path)
- ASIC Flow

INDUSTRIAL EXPERIENCE

- Successfully completed a internship program at Intel Pvt. Ltd. India, a renowned company in the field of technology, gaining hands-on experience and valuable insights into the industry. *June 2022- May 2023*

ONLINE COURSE AND MTECH CURRICULUM

- Received certificate of completion of Verilog HDL from maven silicon *Oct 2021*

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RELEVANT COURSES

- VLSI Design
- Digital Integrated Circuits
- Digital Electronics
- VLSI Design Lab

PARTICIPATION

- Volunteer in Management team of National youth festival Hosted by Gautam Buddha university, Greater Noida (2018)

HOBBIES

- GYM
- Cooking

DECLARATION

- I hereby declare that the details furnished above are true and correct to best of my knowledge and belief