JITENDRA LODHI

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To develop my career as an engineer, contributing quality ideas and work for an organization where there is an ample scope for individual as well as organization growth in VLSI design verification domain.

ACADEMIC DETAILS

B.Tech (ECE)	Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal	8.01/10	2022
Class XII (MPBSE)	Maharana Pratap H.S.school,Gwalior.	77.6/100	2018
Class X (MPBSE)	D.K Public School, Gwalior	71.33/100	2014

PROJECT

- **Clock Generation For User Provided Frequency, Duty Cycle, Jitter and Phase .** **02/2022-02/2021**
  - This project involves the understanding of frequency, time period, duty cycle, jitter and mainly the understanding the waveforms generated through which the result is evaluated
  - Working tool: **Questasim, GVim**.
- **Design of Traffic Light Controller .** **02/2022-02/2022**
  - Designed a Verilog Model for Traffic signal Controller using State Machine Diagram, Implemented the project on Testbench using Verilog and Modelsim,
  - Working tool: **Questasim, GVim**.
- **Design and Verification of Synchronous and Asynchronous FIFO Using Verilog .** **02/2022-02/2022**
  - FIFO is a design component used for interfacing data transfer between two components either working on same frequency or a different frequency.
  - Both are implemented using Verilog and the RTL code verified using Verilog.
  - Working tool: **Questasim, GVim**.
- **Serial Peripheral Interface (SPI) Bus Protocol .** **01/2021-01/2021**
  - The Serial Peripheral Interface is a synchronous serial communication interface specification used for short distance communication, primarily in embedded systems. The project was made using Verilog
  - Working tool: **Questasim, GVim**.
- **APB Functionality Development Using Verilog .** **08/2019-08/2019**
  - In this project, we verified design functionality of APB slave. Developed design code for APB slave in verilog for basic functionality and developed Testbenchfor the same.
  - Working Tool**: Questasim** and **GVim**.

LANGUAGE AND TOOLS

Methodologies	: Verilog , SystemVerilog , Static Timing Analysis .
HDL language	: Verilog , SystemVerilog , Universal Verification Methodology (UVM) .
Tools	: ModelSim , QuestaSim , GVim editor , EDA Playground .
Operating System	: Linux (Commands), Windows .
Other skills	: PCB Designing , Soldering (SMD) .

RELEVANT COURSES

- Digital Electronics, UART, I2C, CMOS VLSI Design, Digital System Design, CDC, STA, Power Optimization.

EXTRA CURRICULAR ACTIVITIES

- Attend National Programme on Technology Enhanced Learning digital Circuits and got certificate with **72%** . 19/12/2020
- Qualified **GATE EXAM 2022** in my Final year**.** 08/02/2022
- VLSI FOR ALL | **Trainee** | Jun 2022 – Present | A Course Focusing On Digital, Verilog, SystemVerilog, UVM .