Jitendra MG

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Objective

To obtain a creative and challenging position in an organization that gives me an opportunity for self-improvement and leadership, while contributing to the symbolic growth of the organization with my technical, innovative, and logical skills.

Education

BE Electrical and Electronics
2016 -2020 Global Academy of Technology-Bengaluru. CGPA – 7.42

12th Pre-University -Science [PCME]
2014 -2016 ASC Independent PU College-Bengaluru. Percentage – 84.5

10th State Board -Karnataka
2014 The New Cambridge English School- Bengaluru. Percentage – 86.08

Academic Projects

Automated small Parts Counting Machine

EDA Tools: Arduino, Stepper Motor, LCD, Inductive Proximity sensor.
Description: To count small parts such as nuts, bolts, screws we came up with a design and control system to do it automatically by using proximity sensor, stepper motor and interfacing it with an Arduino.

Automation of Canal gates

EDA Tools: Hardware: Variable frequency drive, Programmable logic controller, Human Machine Interface, Induction Motor, PV cell, GSM module. Software: DOP & WPL Software
Description: To introduce canal automation in a concise manner without any human intervention by using PLC, HMI

Internships

- Worked as an **intern at Lakshmi Control and Instruments, based** on **PLC** for a period of 1 month.
  - Designed the **control system for mixing of raw materials.**
  - Designed the **gear system of a crane.**

Work Experience

- Worked in TCS for a duration of 14 months as an Assistant System Engineer in computer consultancy department.

Additional Course

Advance training on Physical Design

VLSIGURU Training Institute, Bengaluru
July 2022 to Feb 2023

VLSI Domain Skills

Technical Skills

- Basic Electronics
- Advanced digital Design
- GVIM, Linux
- Hands on technical expertise in Block level physical design implementation.
- Proper floor planning according to timing and power requirement.
- Resolving placement and routing congestion issues.
- Clock tree analysis and optimization
- Fixing timing and DRV violations.
- Good debugging skill in technical issues.
- Good knowledge and Understanding of Synthesis, Static Timing Analysis, Power and IR Analysis.

Tools

- Synthesis : Design compiler
- P&R : Synopsys ICCII
- STA : STARRC, Prime time
- LVS & DRC: IC Validator

Projects

1. ORCA_TOP

- Technology/Layers : 28nm / 9 Metal layers
- Macros : 40
- STD cells : 52k
- No. of clocks : 4
- Target clock Frequency: 450MHz

Role

- The tasks handled were Block level floor planning, End cap Insertion, Tap cell insertion, Placement, Post placement timing Closure, Clock tree synthesis, Post clock Timing closure, clock skew Fixing, Timing fixing & Fixing DRCs, Timing driven and SI driven Routing, Post Route.

Objectives

- Creating the floorplan with high importance for optimum performance.
- Place & route the design for meeting requirement.
- Fixing post route issues using ECO.

Roles and Responsibility

- Floorplan creation and checking and analysing.
- Fixing timing and congestion issues in placement stage using group path and bound creation.
- Critical path grouping and optimization with aggressive weightage.
- Reviewing timing and giving feedback on missing clock definitions, Missing I/O constraints
- CTS implementation and skew optimization.
- Exposure to timing and DRC fixing, Power and IR Analysis.

Achievements

- Participated in **National level techno exhibition** held at Ambedkar Institute of Technology
- Presented a paper on **Design and Development of metal parts counting machine** at oxford college of engineering under National Conference on Science Engineering and Management-2019

Hobbies

- Cricket, Badminton
- Travelling

Declaration

I hereby declare that the above-mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of above mentioned particulars.

Date:
Place: Bengaluru Jitendra MG