TEJASWINI P

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## EXPERIENCE:

Over all 2 Years of Experience in Physical Design.
**Worked as Physical Design engineer at Pozibility Technologies Pvt. Ltd. [Intel client]**

## Skill summary:

- Comprehensive knowledge to the complete digital P&R flow.
- Ability to work independently and develop quick engineering solutions for complex problems. Good experience of linux environment.
- Block level floor planning analysis .Hands On experience with ICC2, Prime Time, Fusion Compiler, Caliber
- Hands-on experience in block-level floor planning, placement optimizations, CTS and routing and signoff
- To effectively work within a team of other Physical Design Engineers and be responsible.

## Tools Used :

Fusion Compiler, Prime time, Caliber

## Roles and Responsibilities:

- Block level PNR [Floorplan, Placement, CTS and Routing], FEV, ECO Signoff
- Macro placement
- Analysis and debug knowledge on setup and hold violation timing fixes.
- Working on signoff stage which includes, Physical Verification, ECO implementation, DRC, LVS, RV fixes
- Performing FEV for block level
- Fixing caliber issues, opens, shorts and floating nets
- Done fixes for Big Wire Delay, slow slope, max cap, illegal cells, cell missing pg connection

## PROJECT DETAILS:

## Intel Client :

**Project 1:**

- Technology – 7nm
- Duration – 10 months
- Project description – 1.5 GHZ, 19 macros, 90k instance count

**Project 2 :**

- Technology - 40nm
- Duration – 9 months
- Project description – 100 MHZ, 65k instance count

**Project 3 :**

- Pozibility technologies pvt ltd internal bench project
- Technology – 32 nm
- Project description – 40 macros, 416 MHz

## ACADEMIC DETAILS:-

| COURSE | NAME OF INSTITUTION | BOARD/ UNIVERSITY | PERCENTAGE | YEAR OF PASSING |
|---|---|---|---|---|
| BE(ECE) | DON BOSCO INSTITUTE OF TECHNOLOGY | VISVESVARAYA TECHNOLOGICAL UNIVERSITY | 6.8(CGPA) | 2020 |
| PUC | MAHESH PU COLLEGE | PU BOARD | 82% | 2016 |
| SSLC | BEML COMPOSITE JUNIOUR COLLEGE | KARNATAKA STATE BOARD | 92% | 2014 |