Somashekhar Kumbar

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Professional Goals

To build a career in VLSI domain by working in an organization where my ability and skills will be utilized effectively for the betterment of myself and the Organization

Core Competency

- Trained in Floorplan, Power plan, Placement, CTS, and Routing
- Good knowledge and understanding of STA concepts: Fixing setup and hold violations, understanding of timing reports, CRPR, effect of skew on timing, OCV
- Hands on experience on VLSI tools: ICC COMPILER, PRIME TIME
- Good Understanding of Digital Logic Design, CMOS fundamentals Good knowledge
- Hands-on experience in Verilog programming and Test-bench based Verification
- Basic knowledge on IC fabrication process
- Understanding of complete ASIC design flow and Physical Design flow

Academic History

Designing of ASIC block using – Physical Design, ChipEdge Technologies Bangalore.

(August 2022 -- December 2022)

Bachelor Degree in Electronics and Communication, SKSVMACET,
Visvesvaraya Technological University (2018 –2021) (7 CGPA)

Intermediate in Diploma from Nalanda foundation Polytechnic , Hubli,
Department Of Technical Education (2015-2018) (67.46%)

Secondary School Leaving Certification (SSLC), Govt Junior Technical School, Hubli,
KSEEB (2015) (72.61%)

Domain Specific Projects

ChipEdge Technologies Pvt. Ltd Bangalore

Physical Design Trainee

1) **SOC Block level Implementation of Chiptop, J Bus Interface, Falcon Project (14nm, 28nm Technology node)**

Tool: ICC2 compiler by Synopsys

Description:

Currently working on SOC Block level Physical design which involves implementation of

- Design setup, Floorplaning
- Power planning, Place, and clock tree synthesis
- Routing, Physical Verification DRC, LVS, and DFM checks
- Signal Integrity and Back Annotation
- Sign-off checks and Tapeout

2) **Static Time analysis**

Tool: Synopsys Prime TimeDescription:
Complete analysis of different types of timing paths by using slew and delay tables for single clock & Multicycle clock by considering constraints such as clock skew, uncertainty, input delay and output delay and derate factors.

Challenges:

- Computing setup slack and hold slack for different timing paths by using skew and delay tables finding worst slack and best slack for setup and hold
- Understanding the causes for setup violation and hold violation
- Generating and analyzing timing reports in PT shell for the given timing paths
- Understanding of clock abnormalities and timing exceptions
- Understanding of derate factors, PVT corners, Global variations, OCV

Experience:

- Attented 4 Day's Hands on Session Workshop on "CMOS VLSI Design and Analysis of Combinational Circuits Using Cadence Design Environment" on gpdk180nm technology in Department of Electronics and Communication at SKSVMACET Laxmeshwar
- Creation of standard basic gates.
- Checked the PVT analysis.
- Creation of layout
- Checked the DRC & LVS

Academic Project

- ☐ Title: Design and analysis of 4TSRAM Cells in 45nm technology.
- ☐ Tool: Cadence Virtuoso Schematic Editor, Cadence
- ☐ Virtuoso Layout Editor, Assura, Analog Deign Environment (XL).
- ☐ Technology: 45nm
- ☐ Role: Responsible for Creation of Layout of Standard Basic Gates and Execution of
- ☐ DRC and LVS check.

Skills:

- Logic Design Physical Design
  - Floorplan & Power plan
  - P&R
  - DRC
- Static Timing Analysis
- Linux/Unix, Shell
- Synopsys IC Compiler (ICC), Primetime
- TCL Scripting

Personal Details:

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near idagunji ganapathi temple Hubli-580024

Languages Known : English, Kannada