Anju A N
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Career Objective

To obtain a position of Physical Design Engineer that will enable me to use my strong technical skills, educational background and ability to work well with the reputed organization.

Core Competancy

- Hands on experience on IC COMPILER II involving FLOOR and POWER PLANNING, PLACEMENT, CLOCK TREE SYNTHESIS and ROUTING.
- Hands on experience on PRIMETIME for STATIC TIMING ANALYSIS and timing closure at block level by analyzing the timing reports at multiple modes (test, func)and scenarios.
- Manual placement of macros based on data flow lines, Macro family and ports.
- Analyzing IR drop map and fixing the floorplan and power plan to solve the issue.
- Good knowledge on ASIC FLOW, Digital electronics.
- Analyzed and understood the constraints to specify the False paths, Multi Cycle paths, CRPR and PVT corners.
- Analyzing and fixing DRC issues.
- Analyzing routing congestion and fixing the floorplan.
- Good knowledge on clock abnormalities - clock jitter, clock latency, clock skew, and the effect of clock skew on timing, Understanding Signal integrity, Xtalk.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**
Vivekananda Institute Of Technology Bengaluru , with 8.42 CGPA

2018
G H College Haveri , with 69 %

SSLC **2016**
Morarji Desai Residential School Savanuru Haveri , with 91.52 %

Domain Specific Project

RV-VLSI DESIGN CENTRE

Graduate Trainee Engineer Aug-2022 to Feb-2023

Block level Physical Design Implementation

Description

A block level Implementation of a design at 40nm technology node with a list of 34 Macros, 40k+ Standard Cells, operating at a frequency of 833 MHz and a nominal supply Voltage of 1.1v with assigned power budget is 600mW with a Target IR drop of 5%.

Tools

Synopsis Prime Time tool for Static Timing Analysis, Synopsis IC compiler II tool for APR flow.

Challenges

- Creating a good floorplan by ensuring a contiguous area between the macros. Meeting the IR drop by giving appropriate values of width and pitch for metal layers used for powerplan.
- Providing appropriate spacing between the macros to bring down the congestion. Providing keep out margin, routing blockage, and placement blockage to avoid DRC violations.
- Ensuring proper placement of Standard cells in respective Standard cell rows, To make sure no DRC, short violations in each step. Routing CTS with NDR rules to avoid Xtalk and EM.
- Fixing Antenna violations by metal jumpers and by inserting antenna diode. Rerouting the existing nets manually while solving antenna issues to avoid new DRC's.

B.E / B.Tech Academic Project

Vivekananda Institute Of Technology Bengaluru

EFFICIENT TECHNIQUE FOR MEASUREMENT AND CONSERVATION OF ELECTRICITY USING SMART ENERGY METER

Description

The Current sensor is used to monitor units consumed, estimate cost. Measurement of voltage and power consumed will be displayed on the LED. In this way the user can observe the consumption of energy from anywhere of worldwide.

Tools

Thing speak, Arduino IDE.

Challenges

- Measurement of energy consumption in household need human intervention in calculation of energy consumed over a period of time. Due to variation in electricity consumption, the consumers are unable to set their electricity monthly budgets.