Jakanagari Uma Sanjana

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About Me

An electronics enthusiast, with bachelors in Electronics and Communication engineering. Creative and a motivated individual with a plethora of zeal to learn and explore. Punctual and disciplined in fulfilling the responsibilities and meeting deadlines. A team player with complimenting interpersonal and communication skills.

Professional Training

VLSI Trainee

Advanced VLSI Design and Verification course

Maven Silicon VLSI Design and Training, Bangalore.
September 2022 – Till date

Education

Graduation
2022

B.TECH in Electronics and Communication Engineering

- First Class with 8.6 CGPA
- From Sreenidhi Institute of Science and Technology, Hyderabad.

Higher Secondary Education
2018

Indian School Certificate Board

- First Class with 93%
- From St. Joseph's Public School, Hyderabad.

Secondary Education
2016

Indian Council for Secondary Education Board

- First Class with 94%
- From St. Joseph's Public School, Hyderabad.

Internships

Internship in Digital Design through Verilog
- from Krisemi Design Technologies
Design of FSM in Verilog, Synthesis and simulation in Xilinx Vivado .

Internship in Arduino boards and Programming
-from Microchip Academy

Internship in Electronics Machines, Converters and Propulsion control systems
-from South Central Railways.

Domain Skills

Design skills:
Combinational & Sequential circuits, FSM, Memories, CMOS implementation

EDA Tools: Mentor Graphics – Questasim, Quartus Prime and Xilinx - Vivado

HDL: Verilog

HVL: System Verilog

Verification Methodologies: Constraint Random Coverage Driven Verification, Assertion Based Verification – SVA

TB Methodology: UVM

Core Skills: RTL Coding using Synthesizable constructs of Verilog, FSM based design, Simulation, CMOS Fundamentals, Code Coverage, Functional Coverage, Synthesis, Assertion Based Verification using, System Verilog Assertions.

Operating System: Linux

Programing skills:

C [Data types , Array , Pointers , Memory Allocation ,Functions]

C++ [Good knowledge of OOPs concept, Class, Inheritance, Polymorphism]

Design skills

Digital Electronics:

Combinational & Sequential circuits, FSM, Memories

HDL: Verilog

- Data types, Operators, Processes, BA & NBA
- Delays in Verilog, begin - end & fork join blocks, looping & branching construct .
- System tasks & Functions, compiler directives, FSM coding
- Synthesis issues, Races in simulation, pipelining RTL & TB Coding
- Generate block, Continuous Procedural Assignments
- Self-checking test bench, Automatic Tasks
- Named Events and Stratified Event Queue

Code Coverage:

Statement and branch coverage, Condition & Expression Coverage, Toggle & FSM Coverage

Verification skills

HVL: System Verilog

- Memories - Dynamic array, Queue, Associative array, Task & Function - Pass by reference, Interface – Mod port and clocking block.
- Basic and advanced object-oriented programming
- Constraint Randomization
- Thread synchronization techniques
- Functional coverage

System Verilog Assertions:

- Types of assertions, assertion building blocks, sequences with edge definitions and logical relationship.
- Sequences with different timing relationships. clock definitions, implication and repetition operators, different sequence compositions, inline and binding assertions.
- Advanced SVA Features and assertion Coverage

Projects

Verification Methodology: UVM

UVM Objects & Components, UVM Factory & overriding methods, Stimulus Modeling, UVM Phases, UVM Configuration, TLM, UVM Sequence, virtual sequence & sequencer, Introduction to RAL

Router 1x3 – RTL design and Verification

The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

- Architected the block level structure for the bridge.
- Developed Verilog RTL for each block.
- Verified each block with different transfers like single READ, WRITE & Burst READ, WRITE and synthesized the design.
- Generated code coverage report for RTL Design signoff.

RFID Based ATM Security System

Designed a model to enhance the security of the existing ATM systems. The model uses three factor authentications to verify security.

Interpersonal Skills

- Confident
- Resilient
- Possess strong communication skills
- Good problem solving ability
- Good Team player

Achievements

- Published a research paper- RFID BASED ATM SECURITY SYSTEM published in IEEE approved in International Conference on Intelligent Controller and Computer for Smart Power (ICICCSP 2022).
- Best Innovation Idea winner in Research and Development programme at a MSME certified organization- Induce.
- Secured Bronze Medal in Basketball tournament conducted at National level by ICSE/ISC Sports association.

Hobbies and interests

- DIY Enthusiast
- Sports
- Journaling
- Fond of melodies
- Cooking

Declaration

I, hereby declare that all the information mentioned above is correct to the best of my knowledge and I shall hold the responsibility of its correctness of the information.

Place: Hyderabad

Signature:
Jakanagari Uma Sanjana