Name: Arigela Rajendra Kumar
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Objective:

Looking forward to establish my career to keep up with cutting edges of technology where my skills in the firm are best utilized for organizational goals and also to enrich my knowledge professionally and personally in order to excel in my path.

Core Competency:

- Worked on tools like ICCompilerII, IC Validator and Primetime
- Hands on experience on Block Level Signoff checks.
- Comprehensive knowledge of Physical Design implementation, Physical Design strategies – sanity checks, Floor Planning, Placement, CTS, Routing and Timing closure.
- Hands on dealing issues like LVS, DRCs.
- Experience on technology node like 40nm.

Project Details:

❖ **RV-VLSI &Embedded Systems Design Center, Bangalore**
Project: Block level implementation in 40nm technology
Description:

- Module: BLOCK I
- Technology Node: 40nm
- Tools used: ICC2,ICValidator

Role:

- Manual placement of macros at the periphery of the core to achieve maximum contiguous area for standard cells.
- Multiple iterations of adjusting the width and pitch of power straps to meet the IR drop target.
- Reducing congestion, avoiding floating nets, creation of blockages.
- Understanding the DRC, LVS and antenna violations.

❖ **RV-VLSI &Embedded Systems Design Center, Bangalore**
Project: Static Timing Analysis for various timing paths
Description:

- Module: BLOCK II
- Technology Node: 40nm

- Tools used: Primetime

Role:

- Interpreting and visualizing the circuit from timing reports.
- Proper understanding of setup time, hold time, min/max derate factor, CRPR which are all essential in analyzing the reports.
- Understanding Time-borrow concept and analyzing the reports for latch based designs. Understanding how the tool fixes the timing violations at each stage.

❖ **Rajeev Gandhi Memorial College of Engineering and Technology**

Project: Trespassers alerting control system using ESP32

Components:

ESP32, FDTI,
PIR sensor,
Buzzer.

Role:

- Designing the circuit on Breadboard
- Verifying the Connections to get desired output
- Team Leader

Education Details:

- Completed Advanced Diploma (Physical Design) in April 2023 from RV-VLSI Design Centre.
- Completed B.Tech. (Electronics and Communication Engineering) from Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal, Andhra Pradesh with *aggregate of 8.1 CGPA* in May-2022.
- Completed Intermediate from Sri Chaitanya Junior College, Vijayawada, Andhra Pradesh *with 95%* in April 2018.
- Completed SSC from Sri Chaitanya school, Kurnool, Andhra Pradesh *with 93%* in May 2016.

Declaration:

I hereby assure that, the information furnished above is true to the best of my knowledge.

Place: Bangalore Arigela Rajendra Kumar