Name : Ch Arunprakash
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Mobile : +91 9494316978

Objective

Looking for an opportunity to enhance my technical skills and knowledge in field of Digital Design and Verification.

Summary

- Knowledge on Digital Design Concepts and Verilog HDL.
- Knowledge in System Verilog concepts and UVM.
- Familiar with Editing tools like Notepad++

Professional Experience

- Worked as an Assistant professor in QIS College of Engineering and Technology, Ongole from 01-06-2018 to 30-10-2020.
- Worked as an Assistant professor in RISE Krishna Sai Prakasam Group of Institutions, Ongole from 01-11-2020 to 30-05-2022.

Technical Skills

HDLs	: Verilog
HVL	: System Verilog
Verification methodology	: UVM
EDA Tool	: Questa 10.7e
Operating System	: Windows 10 &11
Protocols	: AMBA AXI and APB

Certification Course

Certification Course : RTL design and verification.
Institute : VLSI First, Hyderabad India.

Project Details (During Training)

VLSI Project:

Project Title : Verification of APB

The AMBA APB protocol is targeted at low performancedevices that make suitable for a low peripheral interconnect with lesscomplexity & low-cost interface.

Role & Responsibilities:

- Understand the Specifications
- Developed the testbench component sequence, monitor and scoreboard
- Debugging

Education:

Education	Institution/University	Year of Passing	Percentage/CGPA
M.Tech (VLSI Design & ES)	Gayatri Vidya Parishad College of Engineering(A)	2015-2017	79.50%
B.Tech (ECE)	St.Ann's College of Engg. & Tech	2010-2014	67.34%
Inter	VBRJC	2008-2010	87.60%
SSC	BV & BN HS	2007-2008	83.30%

Personal Details :

Father's Name : Veeralingam
Date of Birth : 14-07-1993
Languages : English and Telugu
Nationality : Indian
Address : Chirala, Ap-523165

Declarations:

I hereby Declare that all the information provided above is accurate to best of my Knowledge.

Place:
Hyderabad

Signature:
Ch Arunprakash