Kotha Vijay Krishna

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Mancherial-504205, Telangana

Career Objective

To work in a firm with a professional work driven environment where I can utilize and apply my knowledge, skills which would enable me as a fresh graduate to grow while fulfilling organizational goals.

Core Competancy

- Obtained a good knowledge in ASIC PD flow
- Hands on experience in STA,and designing a circuit by ICC2 tool from synopsys
- Worked on Floor plans for high utilization ratio of the core amnd designed good power nets to connect all the macros
- Generated and analyzed the timing reports of pre and post layout STA on primetime
- Good knowledge in CMOS,Logic design concepts,Semiconductor theory,MOSFETs andf basic electronic devices
- Understood the routing flow
- Basic idea on the PERL

Education Details

Advanced Diploma in ASIC Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

SREENIDHI INSTITUTE OF SCIENCE AND TECHNOLOGY, with 7.48 CGPA

2018

NARAYANA JUNIOR COLLEGE, with 97 %

SSLC **2016**

SLATE HIGH SCHOOL, with 93 %

Domain Specific Project

RV-VLSI INSTITUTE

Graduate Trainee Engineer Jul-2022 to Sep-2022

LAKSHYA

Description

Designing of an ASIC Block level Implemenntation from the given design specifications and perform different optimization techniques to reduce power and obtain zero slack.

Tools

ICC2 tool from synopsys

Challenges

- In floor planning,macro(alignment and placement),placing the blockages and fixing dangling wires using power stripes
- Resolving the module density issue by changing floor plan and performing congestion and timing analysis
- Able to fix connectivity violations,Antenna violations.

RV-SKILLS

Graduate Trainee Engineer Jul-2022 to Sep-2022

STATIC TIMING ANALYSIS

Description

Analyzing the timing reports of Flipflops and latch based timing paths working at different conditions by considering OCV,AOCV,CRPR,uncertainity and certain exceptions(Multi cycle,False paths)

Tools

Synopsys prime time,ICC2 from synopsys

Challenges

- Analyzed all the timing paths in different path groupsat each and every stage of the flow and how some violations are reduced at the later stages
- Differentiating some violations such as false paths and multicycle paths and reporting about the same to change in the constraint file.
- Understood the effects of CPPR,OCV,AOCV and skew factors in timing analysis

B.E / B.Tech Academic Project

SREENIDHI INSTITUTE OF SCIENCE AND TECHNOLOGY

Virtual Voice Assistant

Description

A Virtual Voice Assistant is a software programm that can perform services of an individual based on the commands given to it.We are able to ask questions,place orders in zomato,send messages and personalize in the way want.

Tools

Pycharm,Web Browser

Challenges

- Background sounds which affects the voice recognition