Chandarayudu Kurra

Physical Design Engineer

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Career Objective:

Secure a responsible career opportunity to fully utilize my training and skills, while making a significant contribution to the success of the company.

Professional Experience:

I have completed six months of VLSI PHYSICAL DESIGN training at Takshila Institute of VLSI Technologies, Bangalore.

Technical Skills:

- Worked on different nodes like 28nm and 32nm technologies.
- Expertise in understanding of backend flow such as Floor-planning, Placement, CTS, Routing, STA and Sign-Off.
- Handled complex, hierarchical design which has more macros, participated in block level ECO phase.
- Tools: Synopsys-ICC1.
- Knowledge on Low power techniques like Clock gating, Power gating, Multi Voltage Domain, Level shifter, Power Switches, Multi Vt.
- Basics of DFT.
- TCL scripting.

Education:

SL.No	Degree	Name of the Institute	Board	Academic Year	CGPA
1.	B.Tech (E.C.E)	Mekapati Rajamohan Reddy Institute of Technology & Sciences	JNTUA	2019-22	7.9
2.	Diploma (E.C.E)	Government Polytechnic Collage, Proddatur	SBTET	2016-19	8.5
3.	S.S.C	Sri Vidyadhari High School, Proddatur	BSEAP	2015-16	8.2

Certification:

- Takshila Institute of VLSI Technologies

Title: Professional Training on Physical Design

Project 1:

Title	ORCA_TOP_IO
Tool used	IC Complier
Description	• Technology : 28nm • No. of macros : 30 • Layers : 9 • Std. cell count : 50000 • No. of Clocks : 7 • Frequency : 400MHz
Responsibilities	Iterative Floorplan, IO ports Placement, Power Planning and CTS reviews, Routing and DRC checks.

Challenges:

- Manual placement of macros around the periphery of the core by understanding the fly-lines.
- Achieving congestion-free placement by iteratively changed the floor plan for better routing and standard cell utilization.
- Analyzed the timing paths in different path groups for every session (Placement, CTS, Routing) and also analyzed violations and overcame them.
- Analyzed the open and shorts and resolve them.

Project 2:

Title	ORCA_TOP
Tool used	IC Complier
Description	• Technology : 32nm • No. of macros : 40 • Layers : 9 • Std. cell count : 56013 • No. of Clocks : 6 • Frequency : 416MHz
Responsibilities	Iterative Floorplan, IO ports Placement, Power Planning and CTS reviews, Routing and DRC checks.

Challenges:

- Manual placement of macros around the periphery of the core by understanding the fly-lines.
- Analyzed the timing paths in different path groups for every session (Placement, CTS, Routing) and also analyzed violations and overcame them.
- Reduce the latency in the CTS stage.
- Resolving the opens and shorts.

Declaration:

I hereby declare that I would be glad to come for interview at any time that is convenient to you and assure you of my devoted service.

Date: **Chandrayudu Kurra**

Place: