MeghanaGowda M P

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K.R.Pet-571426, Karnataka

Career Objective

I would love to work for an organization which provides me the opportunity to improve my skills and knowledge to growth along with organization objective.

Core Competancy

- Complete understanding of ASIC design flow from RTL to GSDII and Physical Design flow.
- Worked on floor plan with high utilization and ensuring good contiguous core area for standard cells.
- Implemented power plan to connect power pins of all macros and standard cells to the supply voltage without any PG DRC violations and achieved specified IR drop limit.
- Good knowledge and understanding of STA concepts: Fixing setup and hold violations, understanding of timing reports, effect of skew on timing, OCV, latch concepts.
- Good working knowledge of LINUX, Verilog code and scripting language TCL , perls.
- Hands on experience on Synopsys Prime Time and PnR tool IC Compiler II.
- Good knowledge in Logic Design, CMOS and Basic Electronic Devices.
- Quick learner, ability to work as a team as well as can plan and work in work independently and Good communication skills .

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2020**

G E C K.R.PET , with 6.36 CGPA

2017

Government Polytechnic K.R.PET , with 72.48 %

SSLC **2012**

B.R.P.M. HIGH SCHOOL BEERAVALLY, with 83.20 %

Domain Specific Project

RV -VLSI AND EMBEDDED SYSTEM DESIGN CENTER

Graduate Trainee Engineer Sep-2022 to Oct-2022

STATIC TIMING ANALYSIS (STA)

Description

Timing analysis on different path for registers and latch based designs having multi-cycle paths and half-cycle paths, considering OCV,CRPR, uncertainty, Latency, clock skew.

Tools

Synopsys Prime Time

Challenges

- Understand the causes for setup and hold slack violation.
- Analysis of different timing exceptions like false path, multi-cycle paths and half-cycle paths.
- Understanding of derate factors, PVT corners, Global variations, OCV and AOCV.

RV -VLSI AND EMBEDDED SYSTEM DESIGN CENTER

Graduate Trainee Engineer Oct-2022 to Nov-2022

FLOOR PLAN AND POWER PLAN

Description

Technology - 40nm, Macro count - 34, Standard cell count - 38887, Area - 4.2mm, Supply - 1.1V, Clock frequency - 833GHz, Number of metal layers - 7, Power Budget - 600mW, Max.IR drop (VDD+VSS) - 5% (<55mV).

Tools

Synopsys IC Compiler II

Challenges

- Manually placing hard macros using data flow diagram in such a way that to provide the maximum contiguous core area and to make all pins of the macros are accessible.
- Implementing power plan to meet the target IR drop and made power mesh DRC clean.
- Maintaining uniform orientation of hard macros and adding placement and routing blockages in required locations.

RV -VLSI AND EMBEDDED SYSTEM DESIGN CENTER

Graduate Trainee Engineer Nov-2022 to Dec-2022

PLACEMENT AND CLOCK TREE SYNTHESIS

Description

Timing driven and congestion aware standard cell placement in Non-SPG flow is being done with optimum core utilization and building clock tree and routing all clock pins with optimized clock skew in both classic and CCD modes.

Tools

Synopsys IC Compiler II

Challenges

- Performed timing driven and congestion driven placement and HFNS in order to minimize logical DRCs by thus improving timing QoR.
- Synthesizing clock tree by providing NDR rules and performed detailed routing for all clock nets with DRC clean in both classic and CCD modes.
- Performed sanity checks before and after each stage of physical design flow.

RV -VLSI AND EMBEDDED SYSTEM DESIGN CENTER

Graduate Trainee Engineer Jan-2023 to Jan-2023

ROUTING AND DFM

Description

Routing all standard cell pins and hard macro pins using metal layers, performing via optimization and post route optimization by taking into account of cross talk effects on timing.

Tools

Synopsys IC Compiler II

Challenges

- Fixing antenna violation using metal hopping and antenna diodes manually.
- Clearing all DRC violations and LVS violations in order to make sure that design can be manufacturable.
- Analyzing timing reports and other reports in each stage.

B.E / B.Tech Academic Project

G E C K.R.PET

Simulation of leakage power reduction technique in CMOS Circuits.

Description

To study and analyze the leakage components, a new enhanced leakage power reduction technique by the combination of sleepy stacked with LECTOR technique is applied.

Tools

Software: MATLAB 2018a/SIMULINK, SIMSCAPE, MATSPICE,

Challenges

- Transistors increases area and delay. Doesn't keep reasonable speed and depend upon temperature. Power calculation tools were rarely available and very costly.