SUMITH KUMAR K R

VLSI DESIGN & VERIFICATION TRAINEE

CONTACT ME

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EDUCATION

B.Tech (ECE) - 8.49 CGPA
AIT | Banglore
2017 - 2021

Intermediate - 88.6%
Hongirana Ind. PUC | Shimoga
2015 - 2017

High School (CBSE) - 9.4 CGPA
Hongirana School Of Excellence | Shimoga
2014 - 2015

SKILLS

- **Tools :** Modelsim, Questasim, Quartus Prime, Lint Knowledge, Opencv, TensorFlow, MATLAB, Microsoft Office
- **OS :** Windows, Linux
- **Technologies :** VLSI Design, VLSI Verification, I2C, AMBA, low power design, IoT, Digital Image Processing, Machine Learning, Digital Marketing.
- **Programming Language :** Verilog, System Verilog, C/C++, Python, PERL

ABOUT ME

I am a passionate engineering graduate, specialized in Electronics & Communication Engineering with consistent performance. Trainee in VLSI design and verification with both conceptual and practical knowledge. As I am highly fascinated towards how technology is changing & impacting the world of electronic. My aim is to achieve career excellence with sheer dedication and multifold learnings.

WORK EXPERIENCE

Student Intern
MedevPlus| Banglore
Worked in MedevPlus Banglore which is one of the prestigious medical device company as image processing engineer.

COURSES & WORKSHOPS

- **Mobile Making & IoT** | ATMECE | Mysore
- **Internet Of Things** | NIT | Suratkal
- **Python programming, Embedded systems & IoT Summer School** | Opencube Labs
- **Winter School: Practical Foundation for Machine Learning, OpenCV & Deep Learning** | AIT | Bangalore
- **Diploma in IT** | 84.8 |Manipal Institute of Computer Education
- **Samskrith Prathama** | 87.8% | Karnataka Samskrit University
- **Digital Marketing** | Mycaptain

SOFT SKILLS

- Presentation
- Team management
- Analytical thinking
- Scheduling

AWARDS

- IICDC - MyGov India IICDC - MyGov India Semifinalist (Jan 2020)
- Bharat Scouts and Guides - Zila Puraskar (Feb 2013)

HOBBIES

- Playing Cricket
- Evening long walk
- Trying new recipes
- Learning health tricks
- Personal finance
- Researching financials of different sectors

PROJECTS

- **AHB-to-APB Bridge verification using UVM**
  - Architected the class based verification environment using SystemVerilog
  - Verified the RTL model using SystemVerilog.
  - Generated functional and code coverage for the RTL verification sign-off
- **Router Design Verification using UVM**
  - Architected the block level structure for the design
  - Architected the class based verification environment using SystemVerilog
  - Verified the RTL model using SystemVerilog.
  - Generated functional and code coverage for the RTL verification sign-off
  - Synthesized the design.
- **1X3 Router Design**

  Router of 1 source and 3 destination is designed using Modelsim & Quartus Prime.
- **AI Driven Retail Video Analysis - Enhancing Customer Experience & Business**

  Object detection model & emotion detection model is used
- **Interner Of Underwater Things (IoUT)**

  Underwater wireless communication to reduce the latency in the existing systems

VLSI DESIGN

- **Digital electronics :**

  Combinational & Sequential circuits, FSM, Memories
  STA Basics, comparison with DTA, timing path and constraints, different types of clocks. Clock domain and variations, clock distribution networks, fixing timing failure
- **Verilog Programming :**

  Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks, looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Synthesis issues, Races in simulation, pipelining RTL & TB Coding.
- **Advanced Verilog & Code Coverage :**

  Generate block, continuous procedural assignments, self-checking testbench, automatic tasks, named events and stratified event queue, code coverage: Statement and branch coverage, condition & expression coverage, toggle & FSM Coverage.

VERIFICATION

- **System Verilog HVL**
  - Memories - Dynamic array, Queue, Associative array, Task & Function - Pass by reference
  - Interface - Modport and clocking block
  - Basic and advanced object-oriented programming - Handle assignments, Copying the object contents, Inheritance, polymorphism, static properties and methods, virtual classes and parameterized classes.
  - Constraint Randomization - constraint overriding and inheritance, Distribution and conditional constraints, Soft, static and inline constraints.
  - Thread synchronization techniques - events, semaphores and Mailbox-built-in methods
  - Functional coverage - Cover groups, bins and cross-coverage, CRCDV and regression testing

- **System Verilog Assertions**

  Types of assertions, assertion building blocks, sequences with edge definitions and logical relationship. Sequences with different timing relationships. clock definitions, implication and repetition operators, different sequence compositions, inline and binding assertions, advanced SVA features and assertion coverage.

- **UVM**
  - UVM Objects & Components
  - UVM Factory & overriding methods
  - Stimulus Modelling
  - UVM Phases
  - UVM Configuration
  - TLM
  - UVM Sequence, virtual sequence & sequencer

DECLARATION

I hereby declare that the details and information given above are complete and true to the best of my knowledge.

DATE : 07/02/2023

PLACE : Banglore **SUMITH KUMAR K R**