GUDE SHIVA KUMAR

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15 - 08 - 1999

My Goal

Intend to build a career with a leading cooperate of hi-tech environment with committed and dedicated people, which will help me explore myself fully and realize my potential.

EDUCATION

Master of Technology

- **National Institution of Technology Kurukshetra**
- Pursuing in Electrical engineering with specialization of control systems with 8.85 CGPA from 2021.

Bachelor of Technology

- Anil Neerukonda Institution of Technology and Sciences, Visakhapatnam.
- Graduated in Electrical and Electronics Engineering with 7.43 CGPA from 2016 to 2020.

EXPERIENCE

Product validation

- Working as an intern in Design for Testability in **Cadence Design systems, Noida** for 11 months from June 2022 to May 2023.
    - **Languages:** Verilog, UNIX.
    - **Tools:** Genus, Modus, xmvlog.
    - **Skills:** Digital Electronics, Analog Electronics.
    - **Description:** During internship, I have learnt on ATPG and MBIST. In ATPG, I learned on detecting of faults using scan path insertion. In MBIST, I gained knowledge on MBIST architecture and creation of auto solution groups.

SKILLS

- **HDL languages:** Verilog, System Verilog.
- **Programming Skills:** Python, UNIX.
- **Subject Skills:** Digital Electronics, Analog Electronics
- **Software Tools:** XILINX, Genus, Modus, xmvlog.

PROJECTS

- Testing different types of faults with scan chain insertion with and without compressor.
    - In this project, detected more than one lakh faults by inserting scan chain path to 30000 to 90000 flops with and without compressors.
    - Managed to create different types of SDC timing constraints for a counter with 10 flops.
- Testing of memories with different PMBIST insertion.
    - In this project, detected failure bits for different types of memory by adding solution group to PMBIST insertion.
    - Implementing and creating various types of SDC timing constraints to PMBIST clocks.
- Designing of ALU operations and BIST mechanism.
    - In this project, Created and verified arithmetic logical operations and Built in Self-Test mechanism by Verilog code.

CERTIFICATIONS

- Earned the UDEMY certificate on “System Verilog for verification part1: Fundamentals”
    - **Language**: System Veriolg.
    - **Tools**: XILINX Vivado, EDA playground.
    - **Skills**: Verilog, Basics of OOPS concepts.
    - **Description**: Describing about the fundamentals required for verification like generator, driver, monitor, scoreboard.
- Completed UDEMY certification on “Verilog for an FPGA engineer with Xilinx Vivado suite”.
    - **Languages:** Verilog
    - **Tools:** XILINX Vivado
    - **Skills:** Digital Electronics, Analog Electronics
    - **Description:** Designing of circuits with I/O planning and different types of modelling by HDL code.
- Completed COURSERA certification "Digital systems: From Logic Gates to processors".
    - **Tools**: Oracle VM virtual box
    - **Skills**: Digital Electronics
    - **Description**: Designing of various types of circuits and verifying circuit

ACHIEVEMENTS

- Got AIR 1167 through Instrumentation paper in gate 2021 conducted by IIT Delhi.
- Got AIR 8200 through electrical engineering in gate 2021 conducted by IIT Delhi.