ANAND NISHAD

My Contact

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Technical Skill

Programming Language

- Verilog(HDL)
- System Verilog(HVL)
- UVM(Methodology)
- C

Tools

- Mentor Graphics- Questasim
- Modelsim
- Quartuso prime
- LTSpice
- Matlab
- Xilinx ISE
- Cadence Virtuoso

Hardware

- 8086 Microcontroller

Academic Coursework

- Digital Electronics
- Analog Electronics
- Signal and System
- Digital Communication
- VLSI Design
- Network Theory
- IC fabrication Technology
- Microprocessor/Microcontroller

About Me

Dedicated and result-oriented **VLSI Design and Verification Trainee** with **2+ years** of experience as **system engineer**. Eager to apply proven-RTL Design and Verification skills for Semiconductor domain Company. Special interest in achieving the skillset goals.

Professional Training

Maven Silicon
Advanced VLSI Design and Verification Course
From April 2022 - Present

Work Experience

eCentric Solutions Private limited ,Delhi
Designation - System Engineer
From Jan 2018 - April 2020
Role and Responsibility: Manage and monitor all installed system and deal with logistic team co-ordination ,automatic machinery control, work process.

Education

- **Assam University, Silchar**

Bachelor of Technology in Electronics and Communication Engineering
From June 2013 - 2017
CGPA - 6.51

- **SVM Inter College Kanpur**

Senior Secondary(UPBOARD)
From May 2009 - 2011
Percentage - 79.20

- **SVM Inter College Kanpur**

Higher Secondary(UPBOARD)
From May 2008 - 2009
Percentage - 73.16

Specialization in Design Verification

Digital Electronics: Combinational and Sequential circuit, register ,counter, FSM , vending machine, memories FIFO etc..

Achievements

- Crack **JEE Main 2013** exam got government college

Certifications

- VLSI System on **Chip Design**
- **Analog Integrated Circuit Design** and ASIC implementation using **Cadence Design System.**
- Art and Challenging of **Writing Paper for IEEE Transactions** and High Impact Factor Journals
- Summer Technical Training (**Electronics Interconnections Techniques, Introduction to EMC and Calibration , PLC and Microcontroller**

Hobbies & Activities

- Travelling
- Running
- Reading Article and Books
- Listening music
- Coordinator in ASIC workshop
- Convener in Tech-fest
- Mess Manager in Hostel

STA basics: Comparison with DTA, Timing Path and Constraints, Different type of clocks, Clock domain and Variations, Clock Distribution Networks, Fixing timing failure.

Verilog Programming: Abstraction, Data type, Operators, sequential and Parallel block, Blocking and Non blocking assignment, Delays in Verilog, If else and case construct ,Looping-for ,repeat, forever, Task and Functions, Synthesis issue, Race in simulation, FSM coding, pipelining RTL and TB coding.

Advanced Verilog & Code Coverage: Generate block, Continuous Procedural Assignment, Self checking TB, Automatic Tasks, Named Events and Stratified Events Queue, Code Coverage , Toggle and FSM Coverage.

System Verilog HVL: Data type, Memories, Task and Functions, Interfaces, OOP Basics, Randomization, Constraints, Threads, Functional Coverage, Verification plan, RAM- TB Environment.

Universal Verification Methodology: UVM Factory, Stimulus Modeling, UVM Phases, Reporting Mechanism, TLM, UVM Configuration, Creating TB Components, UVM Sequence, Virtual Sequence and Virtual Sequencer, Creating Scoreboard, UVM Callbacks , UVM Events, Register Abstraction Layer.

VLSI Projects

Router 1x3n - RTL Design and Verification

HDL: Verilog
HVL: System Verilog
TB Methodology: UVM
EDA Tools: Questasim and ISE

Description: The router accepts data packets on a single 8-bit port and route to one of the three output channels , channel0, channel1, channel2.

Responsibility:

- Architected the block level structure for design
- Implemented RTL using Verilog HDL
- Architected the class based verification environment using System Verilog
- Verified the RTL model using System Verilog
- Generated functional and code coverage for RTL Verification sign-off
- Synthesized the design

Academic Projects

B.Tech Project: Study of Memristor and Its Application

Description: Theoretical approach to understand the memristor and its application in digital logic as well as analog electronics.

Responsibilities:

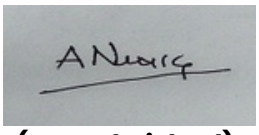
- Design the various model of memristor in the MATLAB environment.
- Investigated the behavior of memristor in direct current and alternating current.
- Simulate model of memristor in LTSPICE.
- Designed a oscillator using memristor.
- Analyzed the transient behavior of the Oscillator.

Declaration

I certify that foregoing information is correct and complete in all respect to the best of my knowledge and belief. If any information is found incorrect/ wrong, I shall be liable to action as decided by the authority.

Date:

Place: Bangalore



(Anand Nishad)