Resume

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Career objective

A dynamic, focused and dedicated student studied in **Electronics and Communications Engineering** at Gitam School of technology, who is constantly eager to refresh and enhance new technical skills in order to provide improved service as well as develop an inclusive mindset and thrive in this constantly evolving global market.

Education qualifications

- **O** Bachelors in **Electronic and Communication Engineering** from gitam school of technology with cgpa 6.87
- **O** Pre-university course in **PCMB** from st.joseph Indian composite pre-university in 2017
- SSLC from Vikasa high school with percentage 74.14

PROFESSIONAL TRAINING

Advanced VLSI Design and Verification

Futurewiz VLSI Training Institute Bangaluru

Technical skills

| 0 | HDL:- Verilog, Advanced Verilog | | | | |
|-------------|---|--|--|--|--|
| 0 | HVL :- System Verilog | | | | |
| 0 | TB Methodology :- UVM | | | | |
| 0 | Programming :- C | | | | |
| 0 | Domain:- FPGA front-end Design and Verification | | | | |
| | | | | | |
| EDA | TOOLS | | | | |
| | | | | | |
| 0 | Quartus Prima | | | | |
| O | Quartus Prime | | | | |
| 0 | Modelsim | | | | |
| 0 | Questasim | | | | |
| | | | | | |
| DD 0 | | | | | |
| DES. | IGN SKILLS | | | | |
| | | | | | |
| 0 | Digital Electronics | | | | |
| 0 | STA | | | | |
| 0 | Verilog programming | | | | |
| 0 | Advance Verilog & Code Coverage | | | | |

VERIFICATION SKILLS

- O System Verilog HVL
- O System Verilog Assertions
- O UVM

DECLARATION

I hereby declare that all the above information is true to the best of my knowledge And I bear the responsibility for the correctness of the mentioned particulars