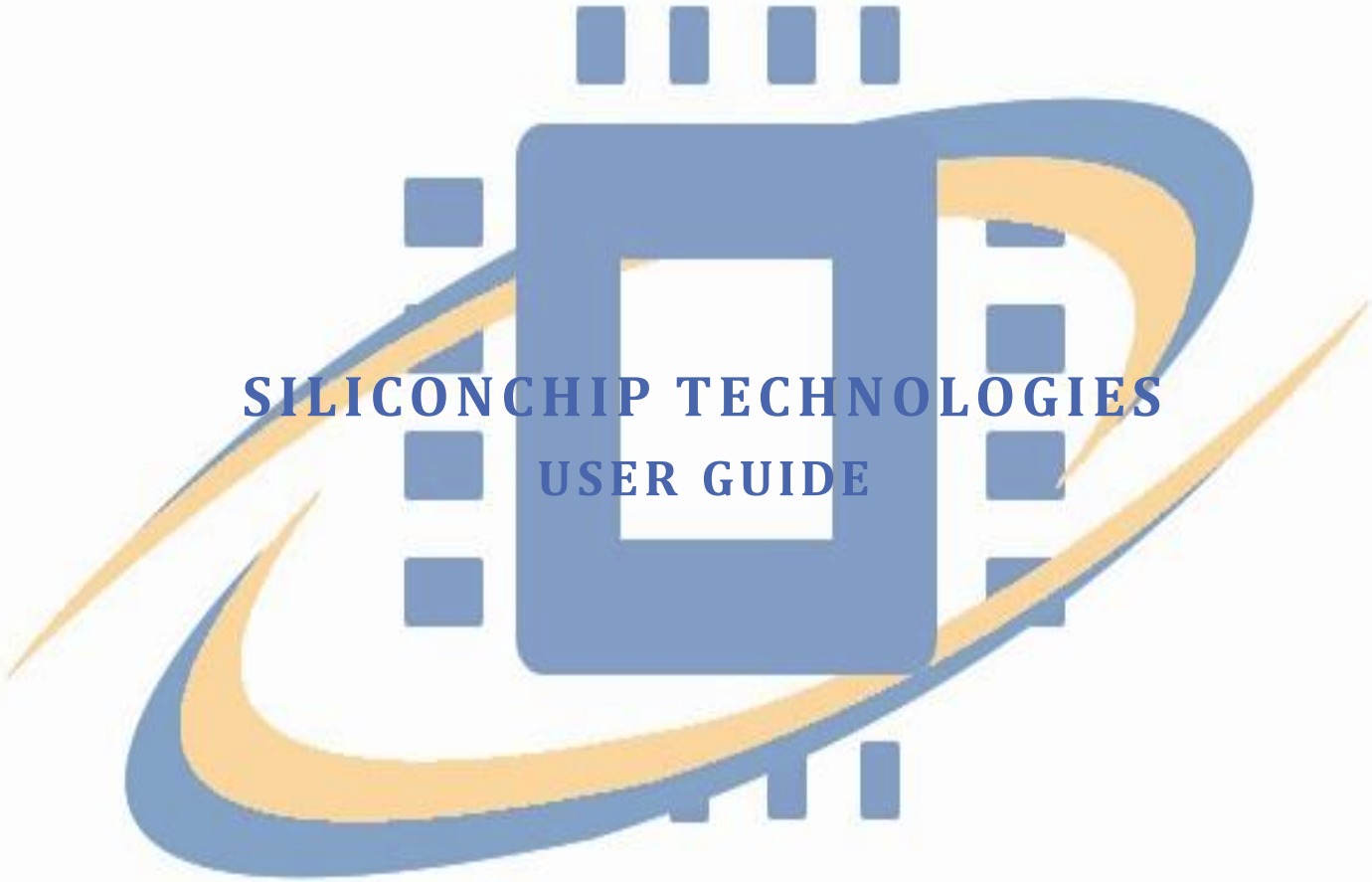


SILICONCHIP TECHNOLOGIES

USER GUIDE

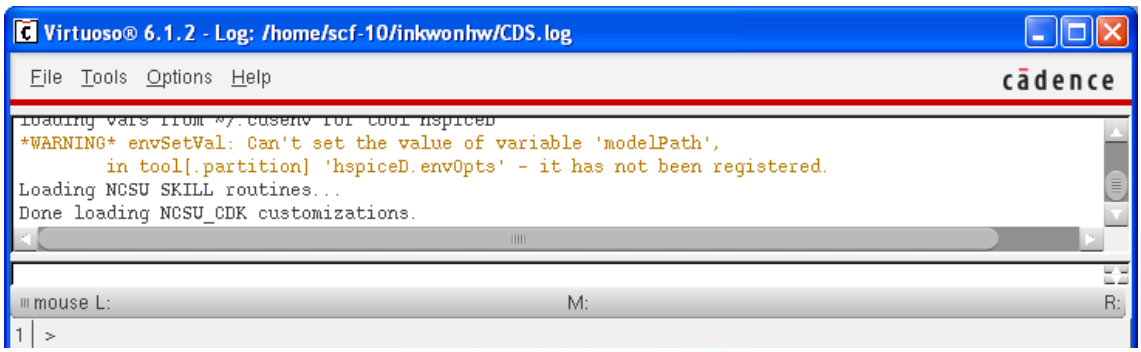
Cadence Tutorial

for Cadence version 6.1

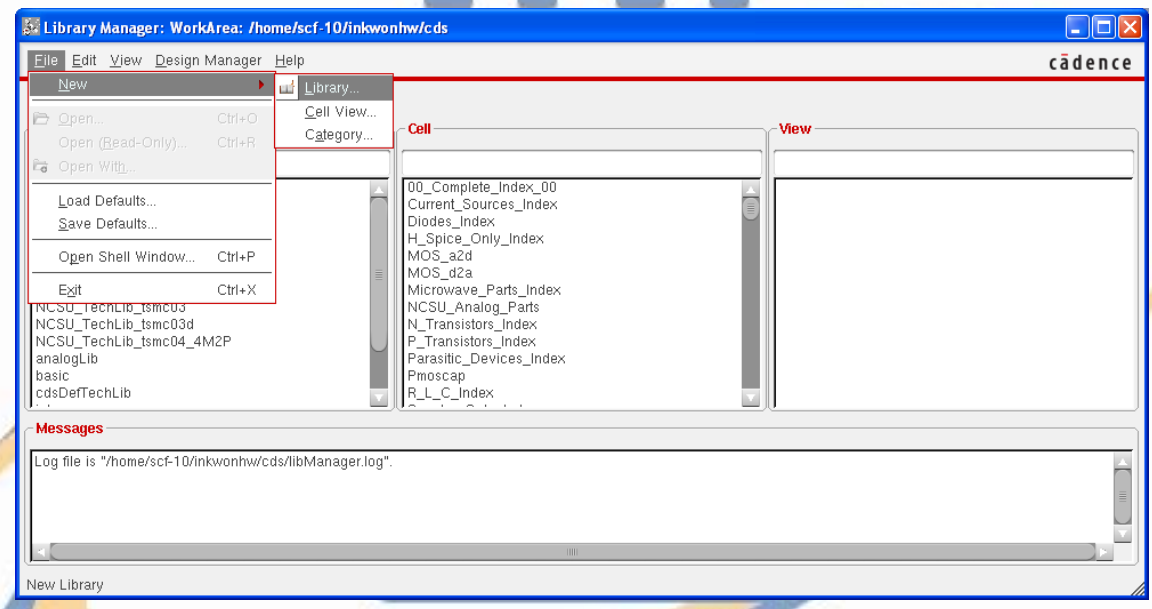
Inkwon Hwang
Feb, 2010

1. Create Library

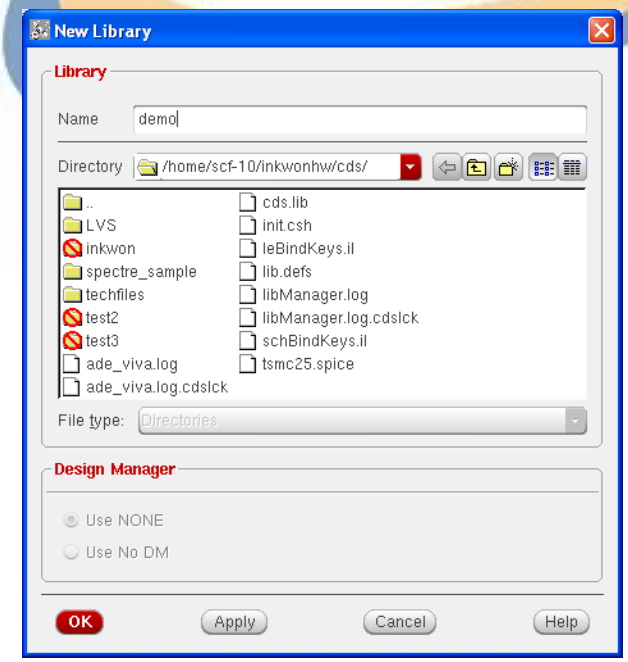
A. Tools → Library Manager

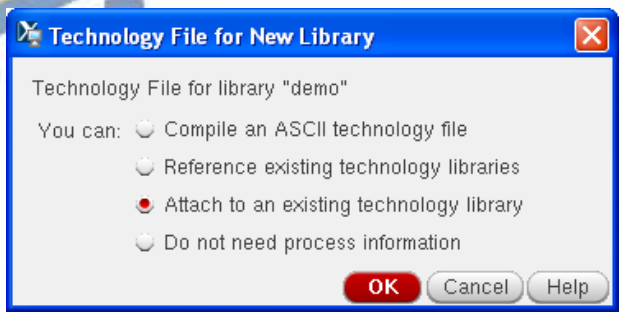


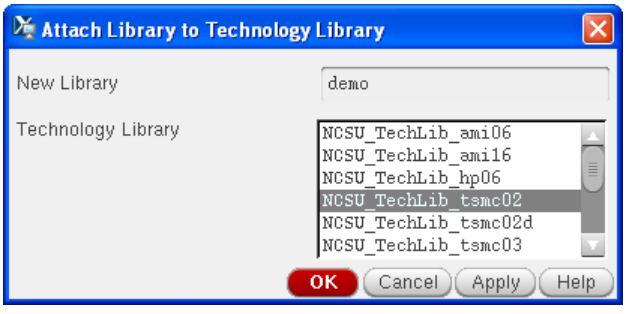
B. File → New → Library



C. Give a name and attach it to a technology library

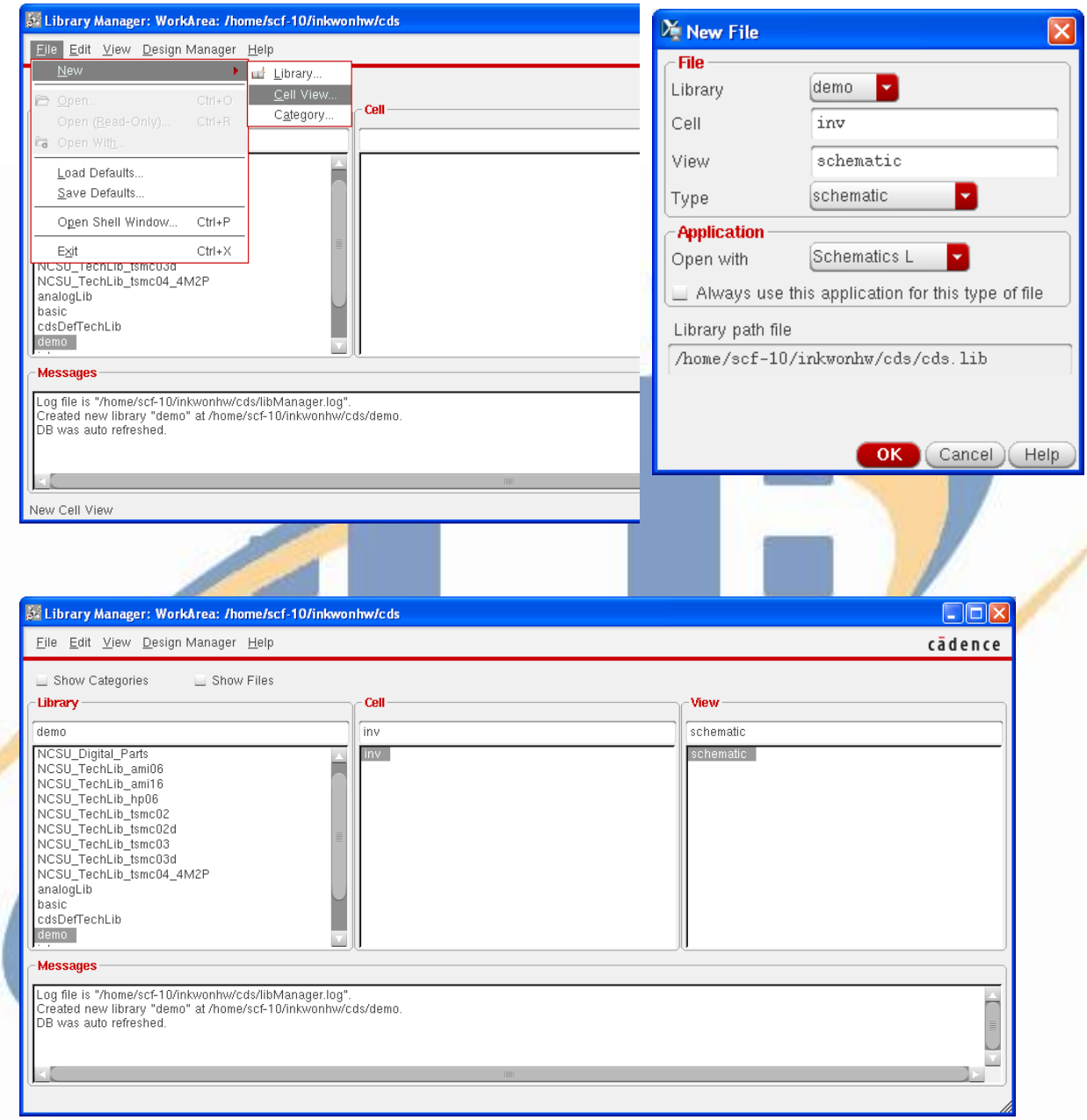






2. Schematic

A. Create a cell view

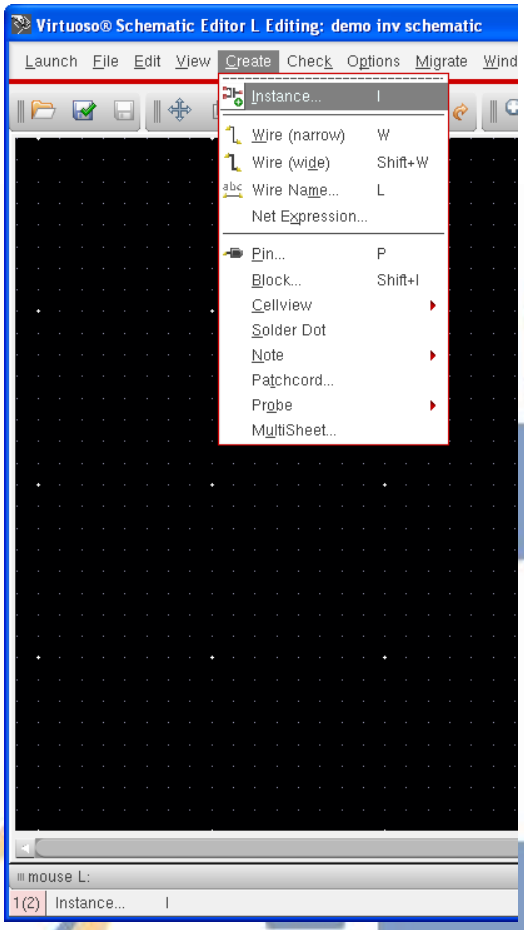


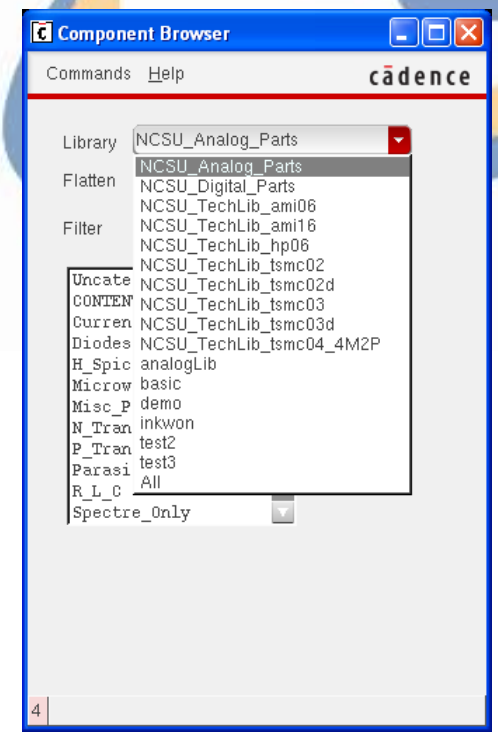
B. Draw a schematic

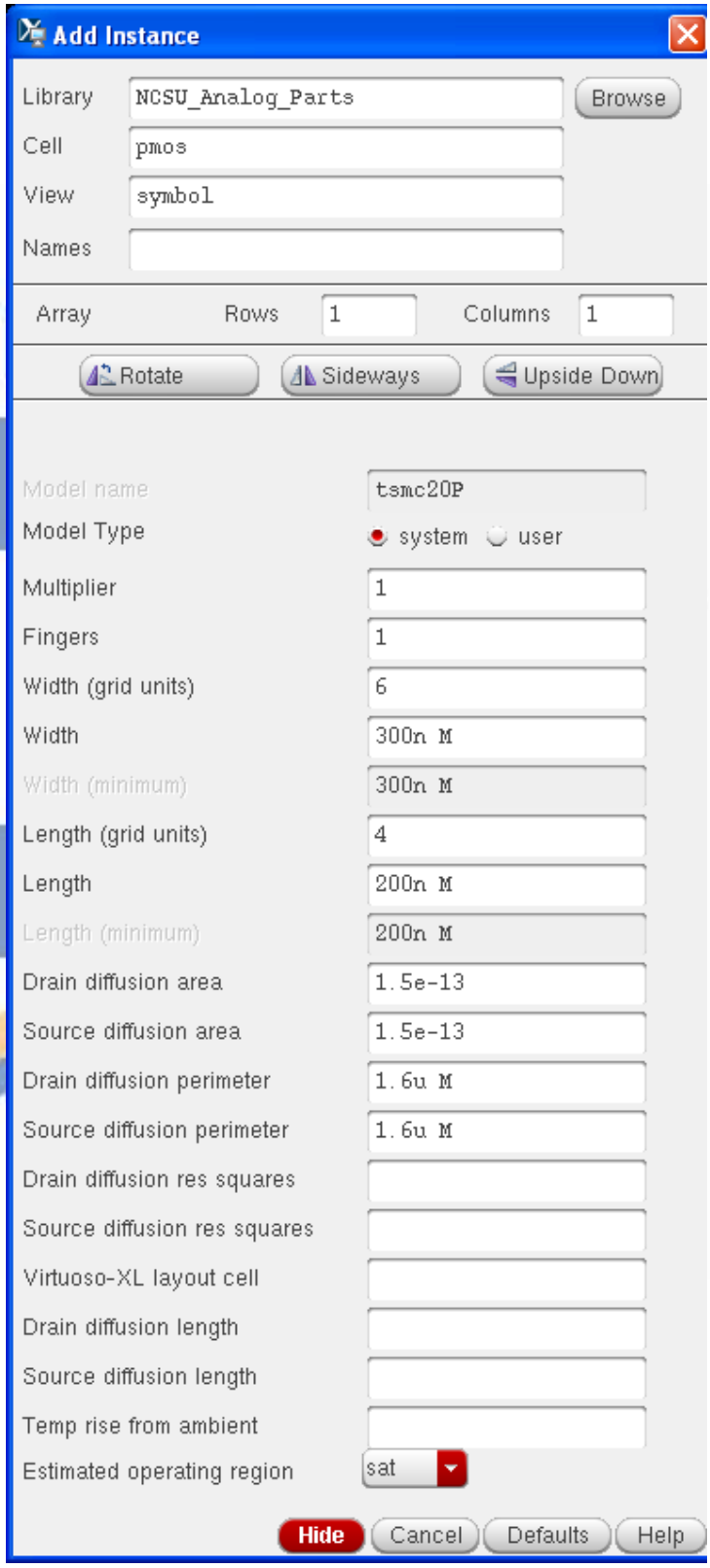
i. Add instances – pmos

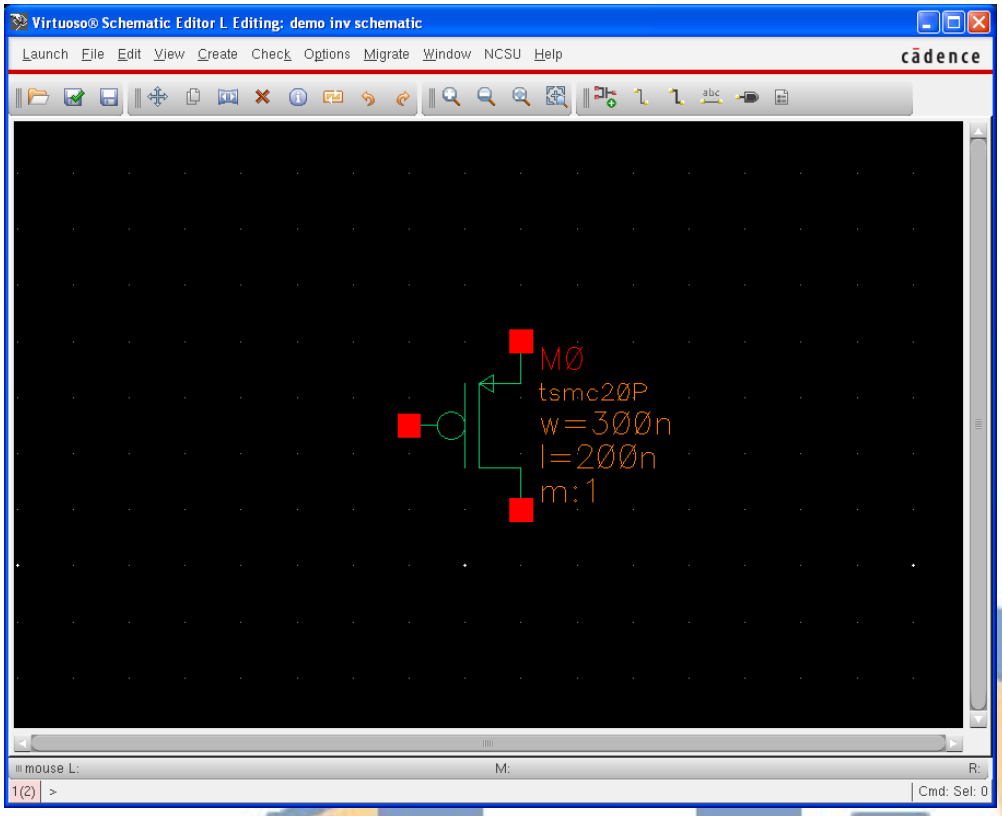
You can modify Width of transistors. Don't modify length unless you have a special purpose.

You should select a NCSU_Analog_Parts library.

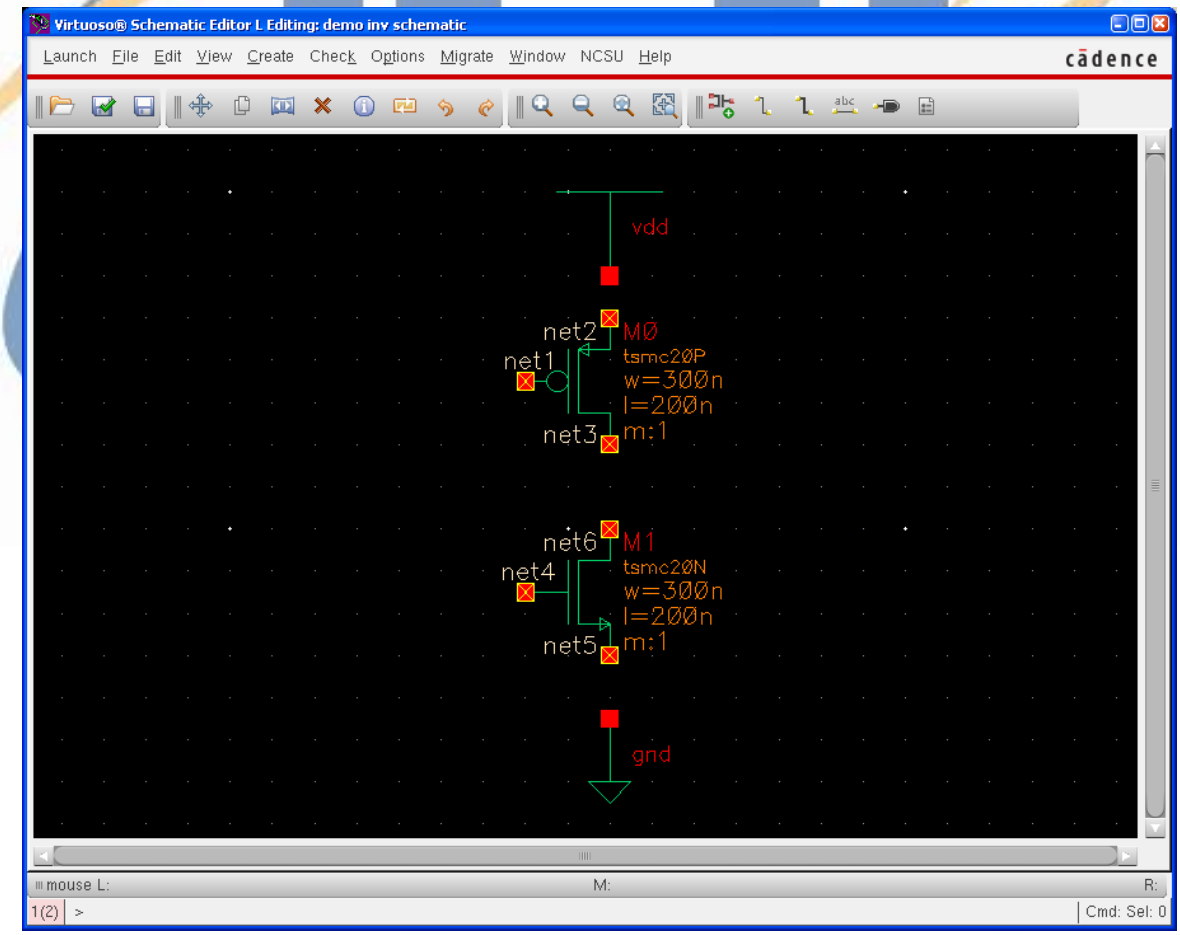




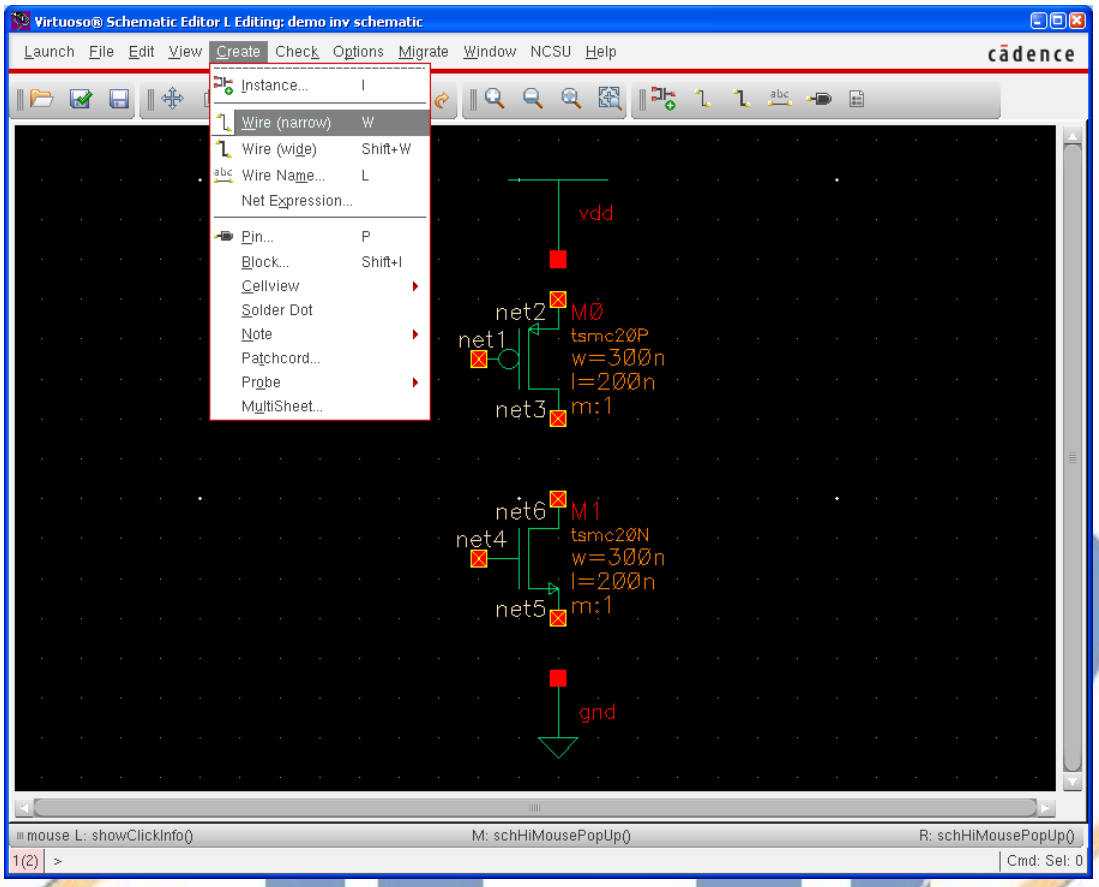


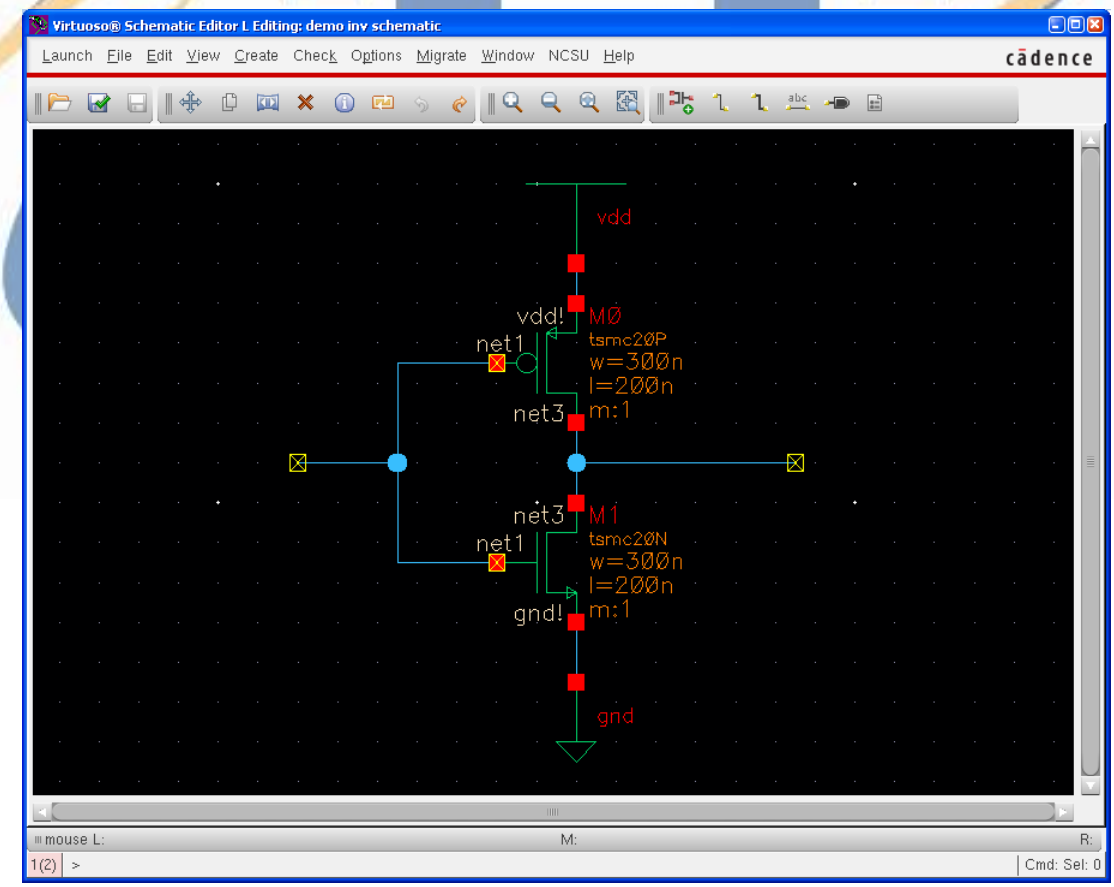


ii. Add instances – nmos, vdd, and gnd

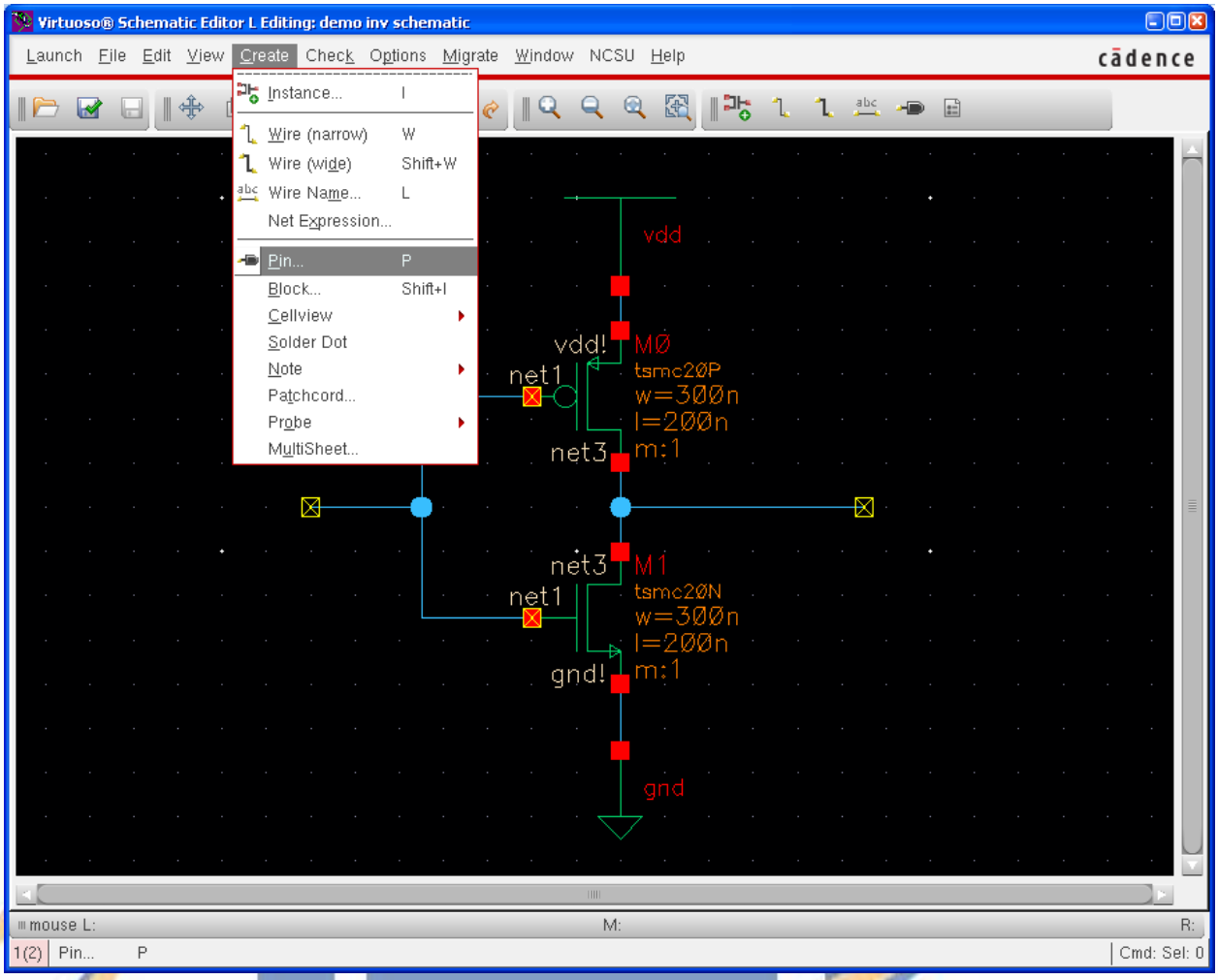


iii. Add wires: Create → Wire

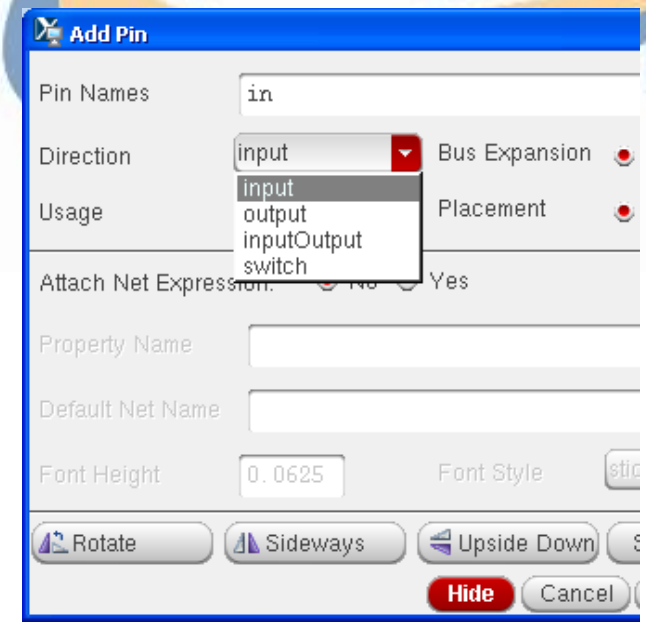


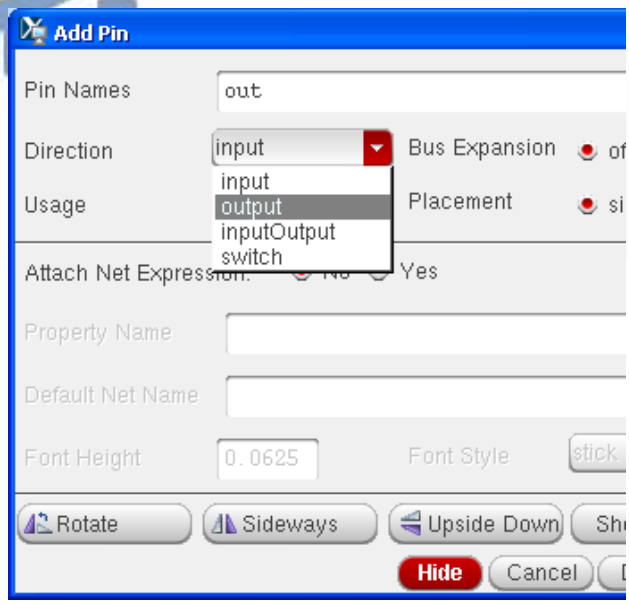


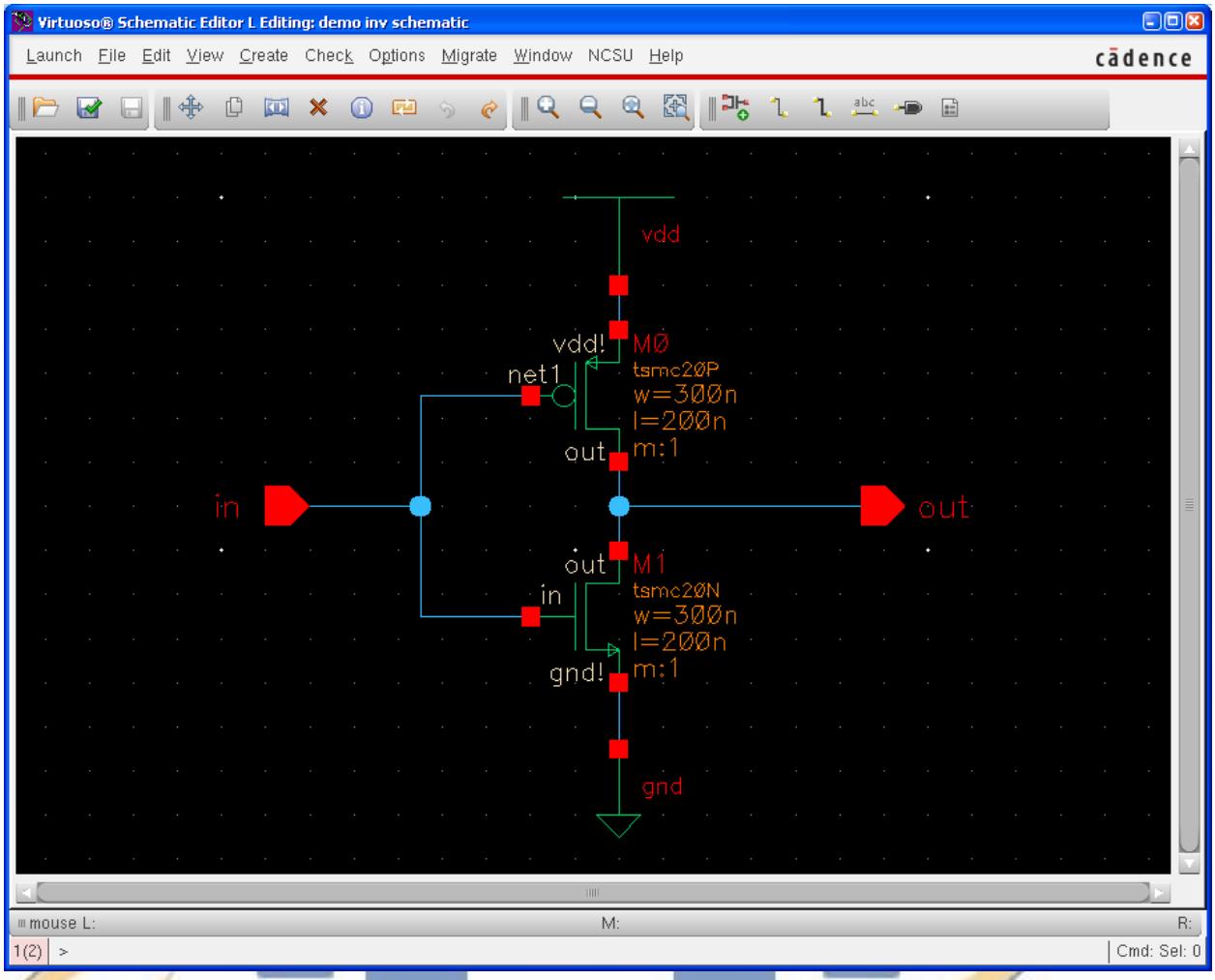
iv. Add pins: Create → Pin



We have for different types of direction. For schematics, we only use two types, input and output. InputOutput type is for supply changes, and it is necessary only for layout. We will discuss about this later.







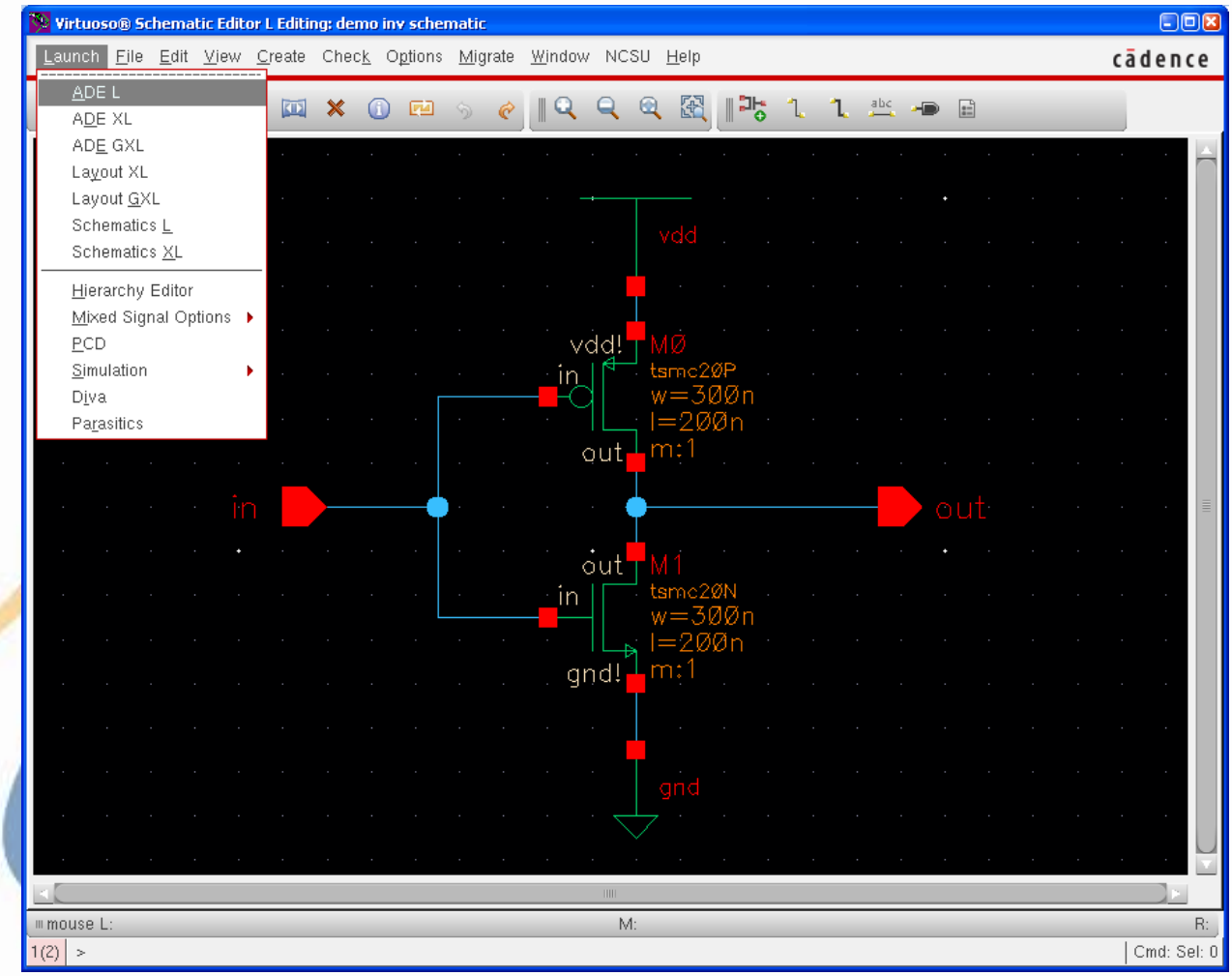
Now, we completed a schematic design. Let's move on the next phase.

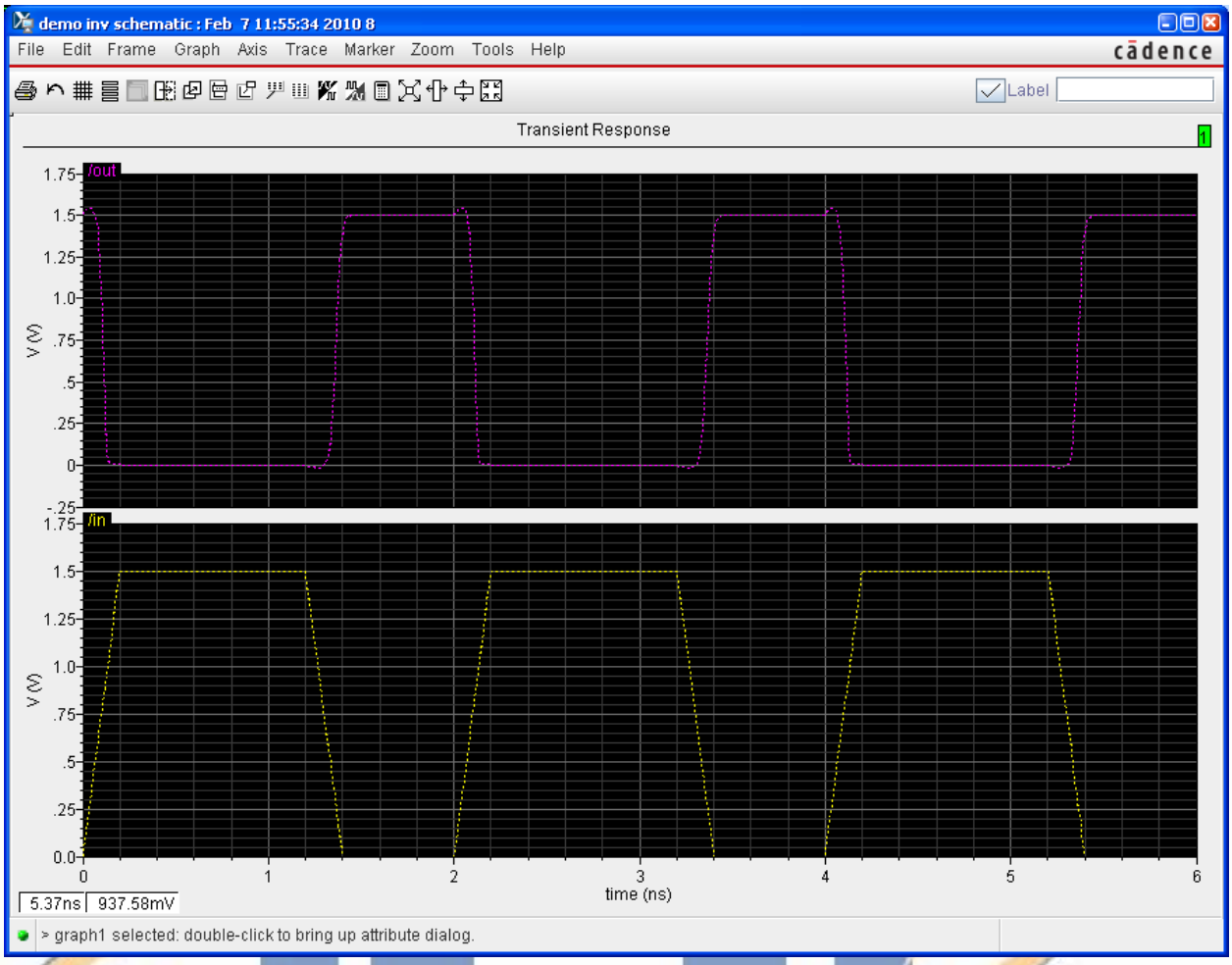
3. Run Spectre simulation

We will run spectre simulation. This section is for **both** schematics and layouts. I will show an example for a schematic. You can do the same thing for a layout.

A. Launch ADE (Analog Design Environment) L

Launch → ADE L





If you see a waveform like above picture, you followed every step properly.

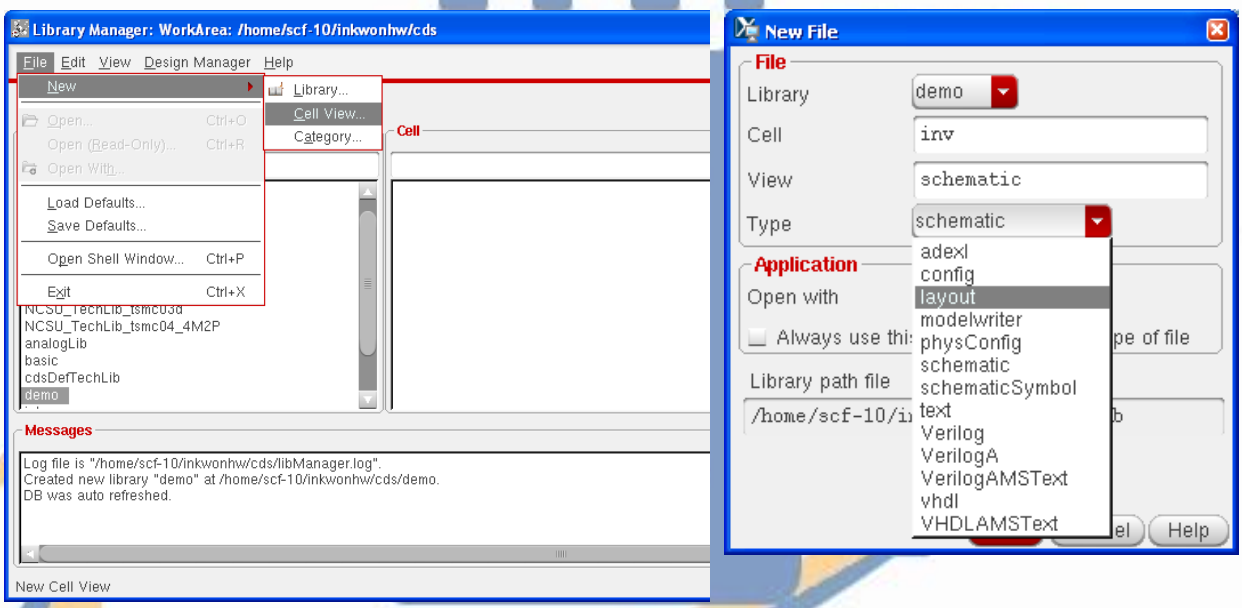
Good job!.

4. Layout

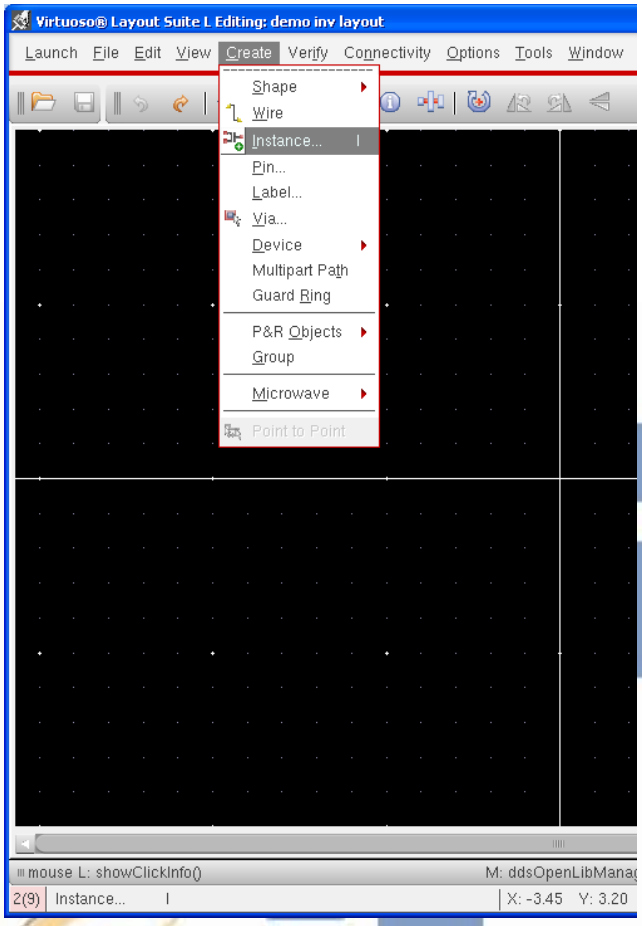
It’s time to draw layout. Schematics are for verifying your design very roughly. They don’t consider physical features like parasitic capacitances. After determining your design variables by schematics, you need to draw layouts.

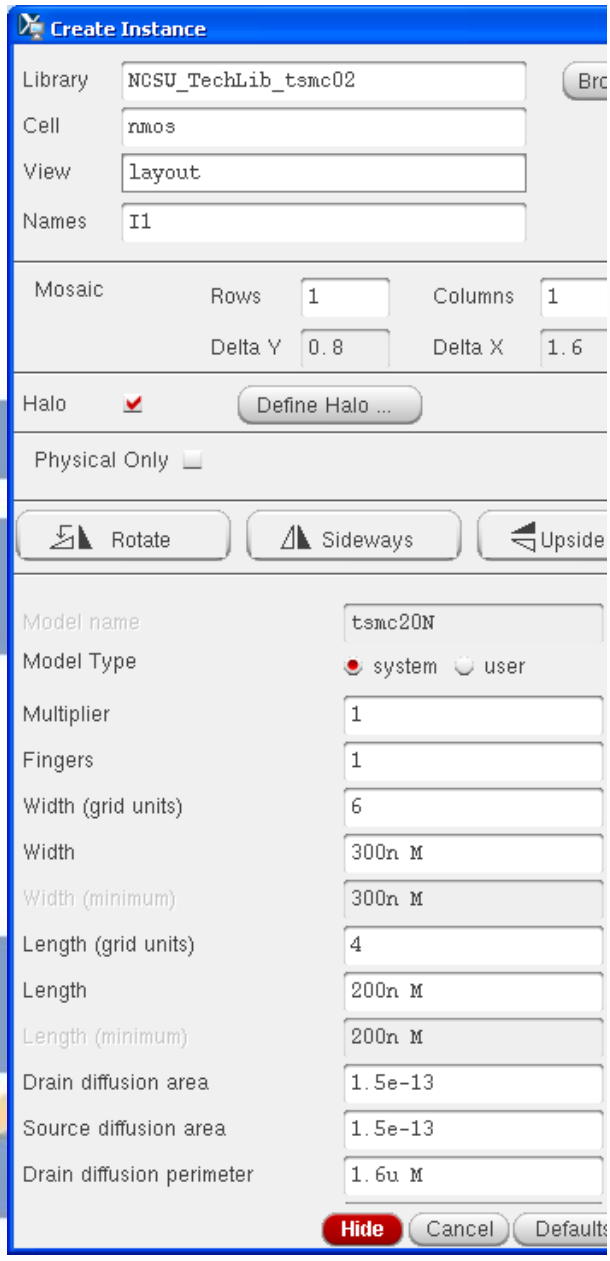
Design flow of layouts is very similar to one of schematics, but it has additional step which is LVS check. It is for check if your layout is identical to the schematic or not. Hence, this step is very important. If your logic doesn’t pass this step, you may lose significant points for that.

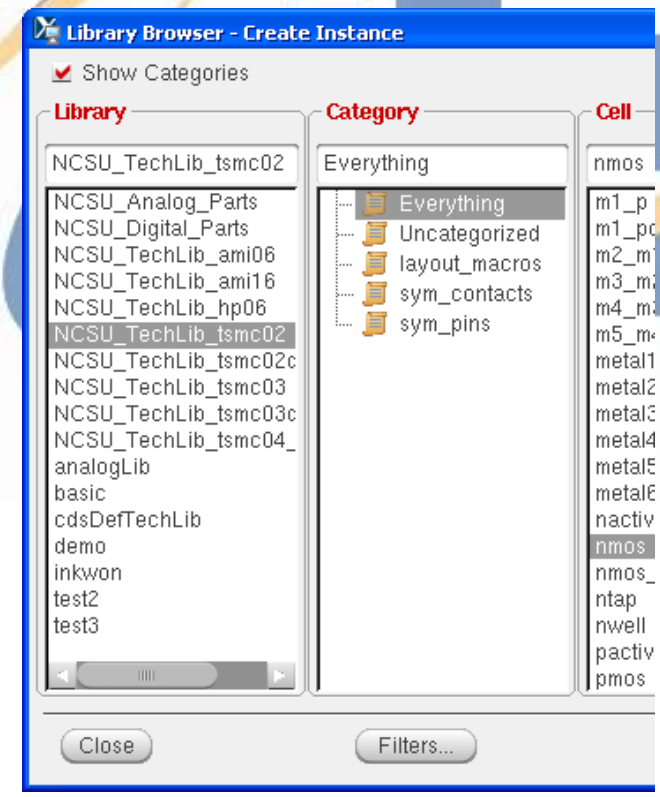
A. Create a layout



B. Add an instance - nmos

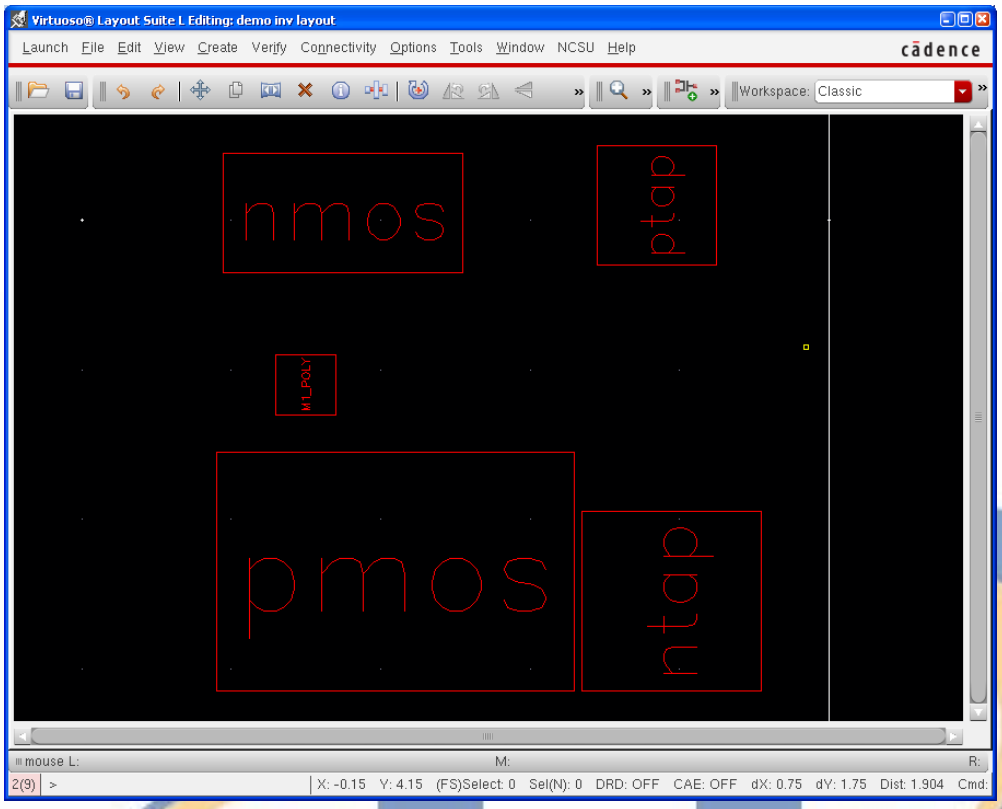




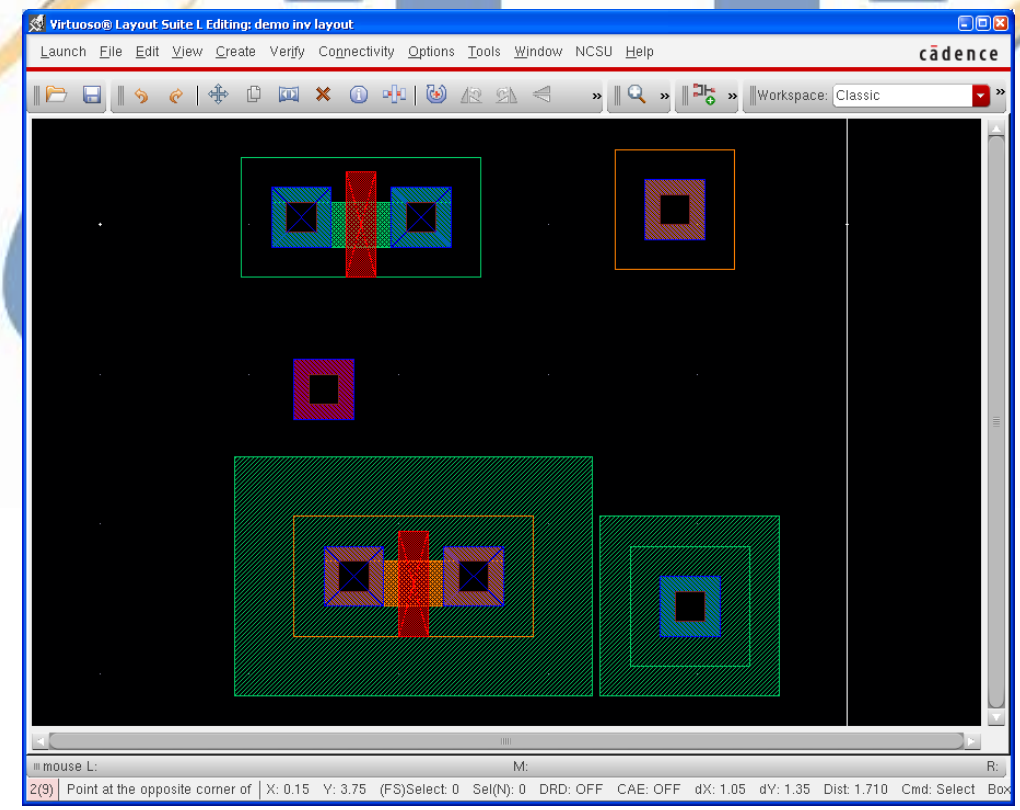


You can modify width of transistors.

C. Add more instances – pmos, ptap, ntap, and m1_ploy



You can select alternate view of a layout. Try 'Shift + f' and 'Ctrl + f'.

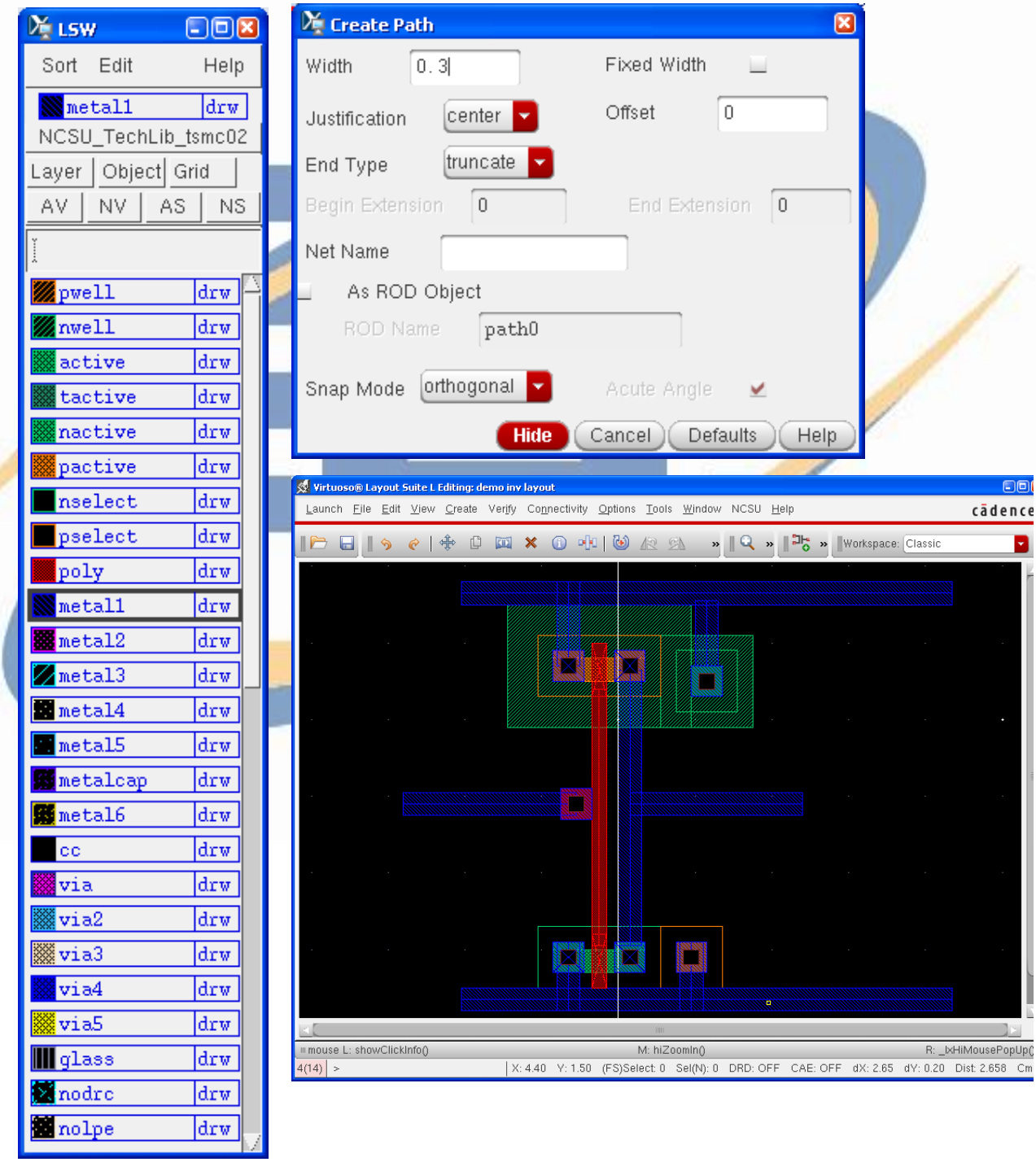


D. Draw metal1

There are few ways for drawing metal, but I recommend you use ‘path’. It’s quite convenience than others.

Create → Shape → Path

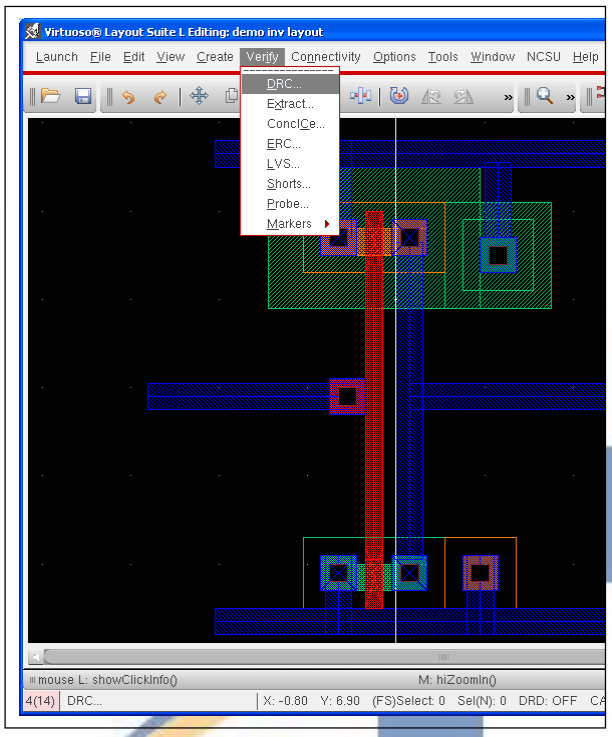
First of all, you should select metal1 on LSW window. Default width for metal1 is 0.3, which means 300nm (3 λ). You can draw metal layer simply by clicking

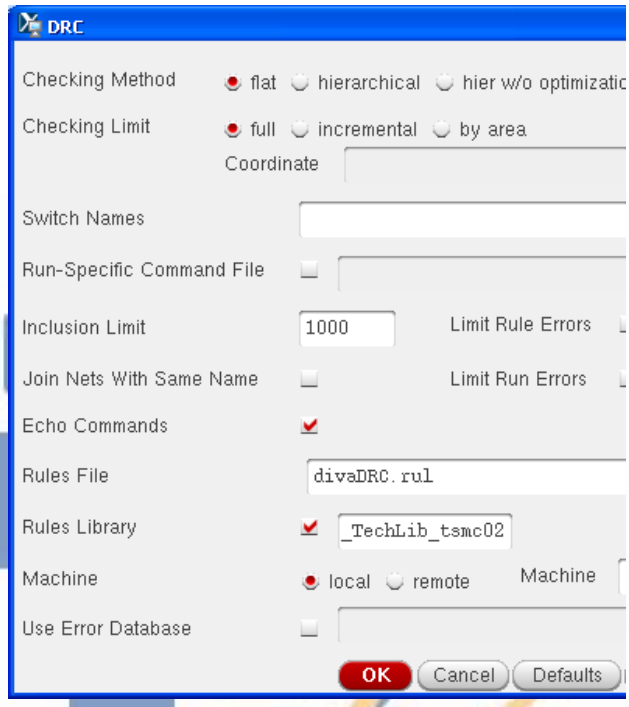


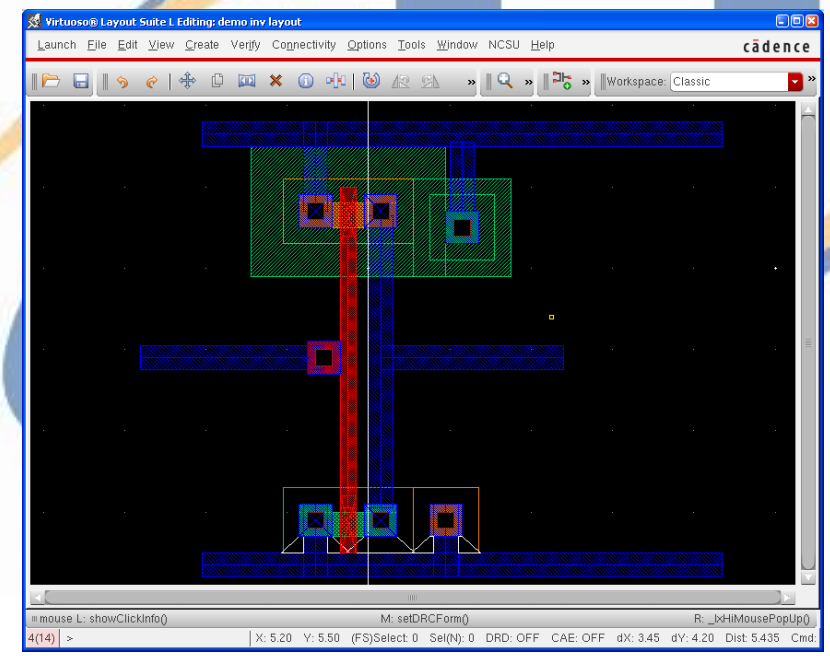
E. Run DRC

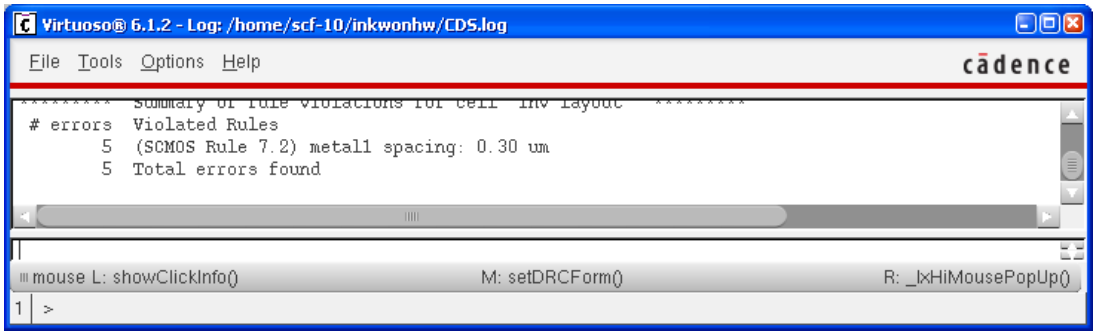
This step checks if your layout follows design rules.

Verify → DRC

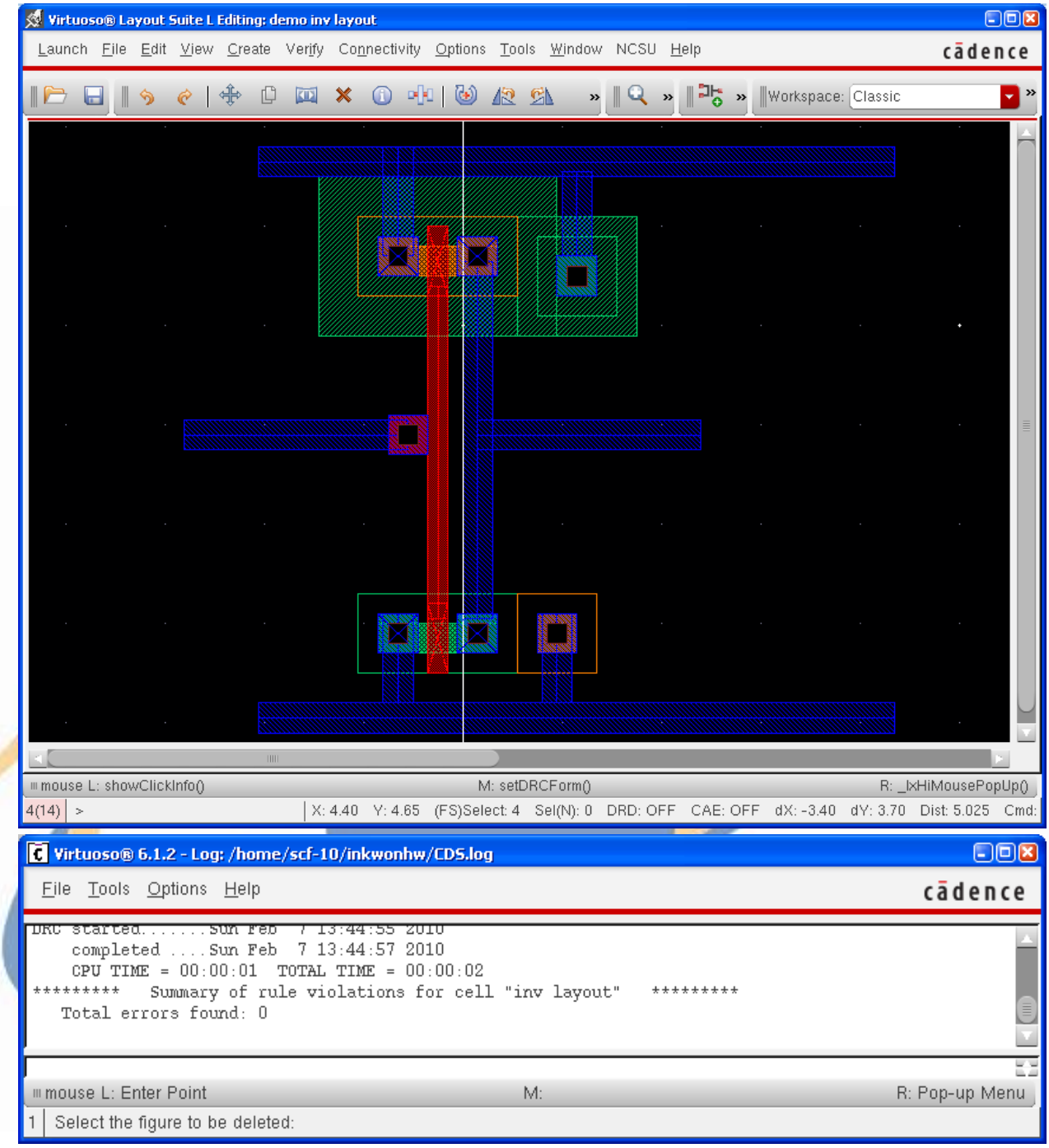








We have five errors. It is because a gnd metal layer is too close to an nmos transistor. After modifying layout, run DRC again.

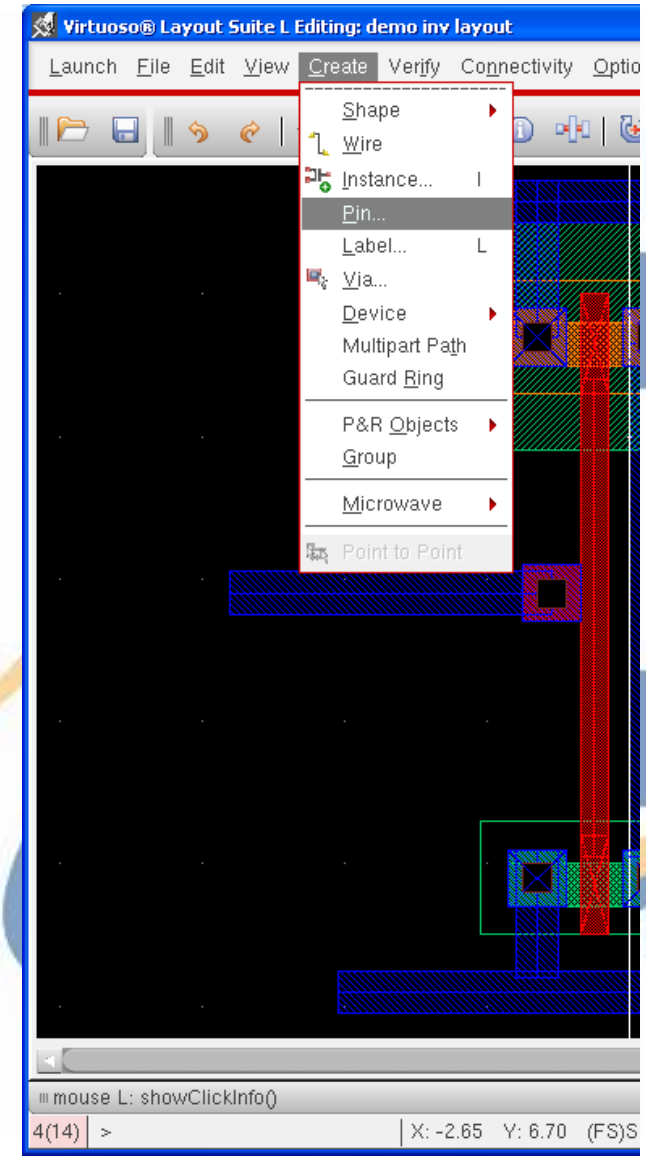


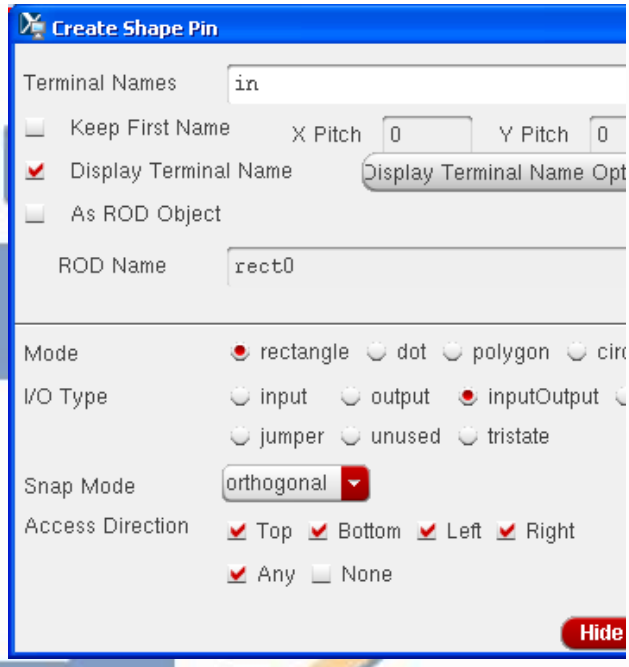
There is no error!!

F. Add pins

We had two pins on a schematic, which are ‘in’ and ‘out’. Pins are for assigning signals to physical device, so we assign voltage level of gnd and vdd by using pins. Hence, we have 4 pins for the layout, which are ‘in’, ‘out’, ‘gnd!’, and ‘vdd!’.

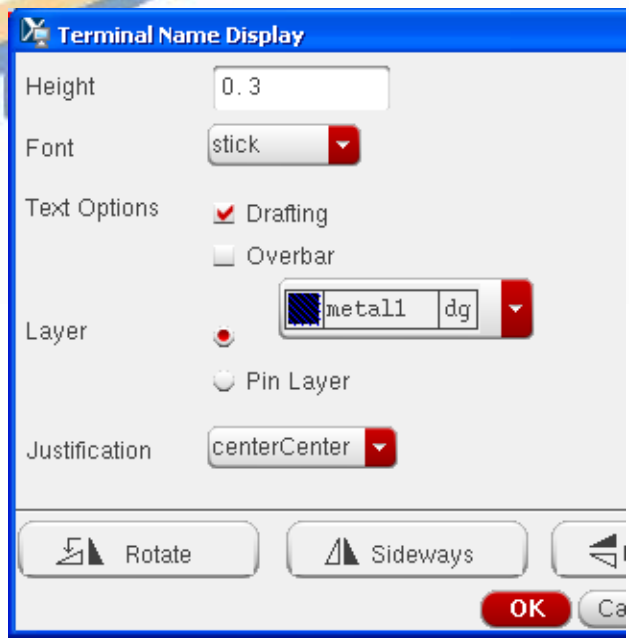
Create → Pin

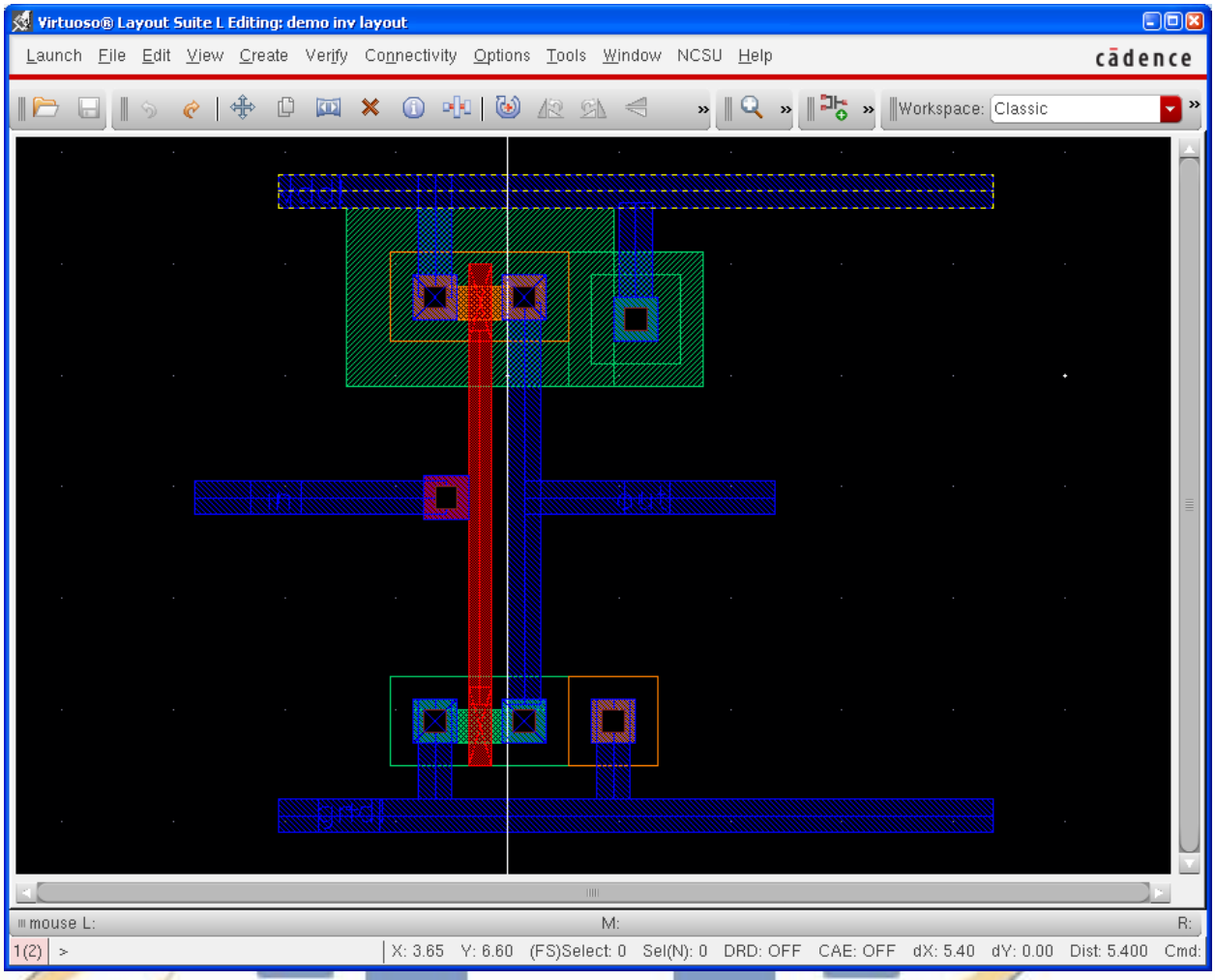




Check ‘Display Terminal Name’ if you want to see pin name on the layout.

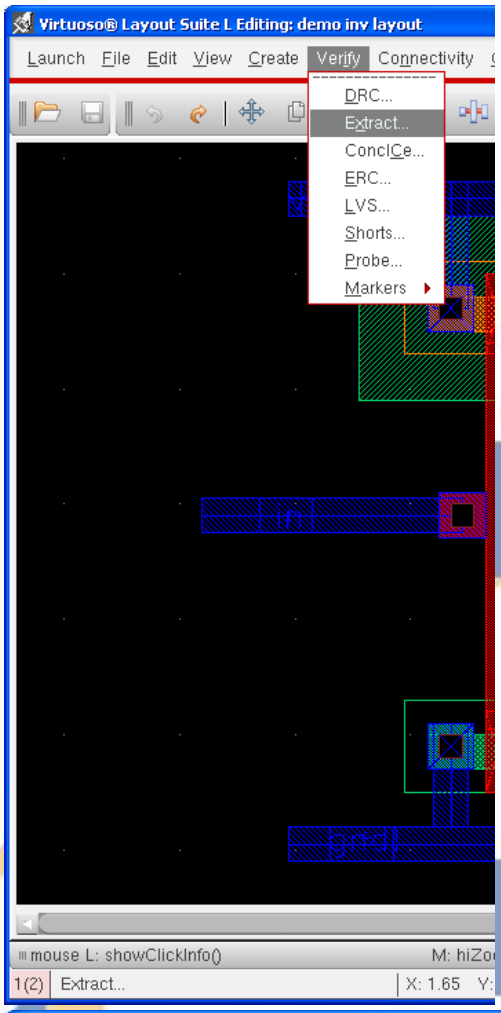
Click ‘Display Terminal Option

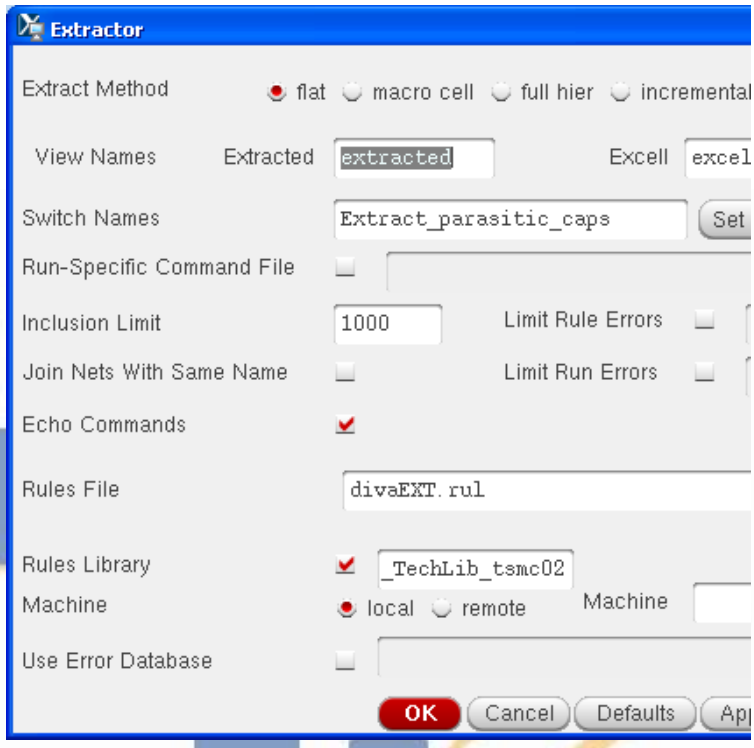



Virtuoso® Layout Suite L Editing: demo inv layout
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Workspace: Classic
vdd!
in
out
gnd!
mouse L:
M:
R:
1(2)
X: 3.65 Y: 6.60 (FS)Select: 0 Sel(N): 0 DRD: OFF CAE: OFF dX: 5.40 dY: 0.00 Dist: 5.400 Cmd:

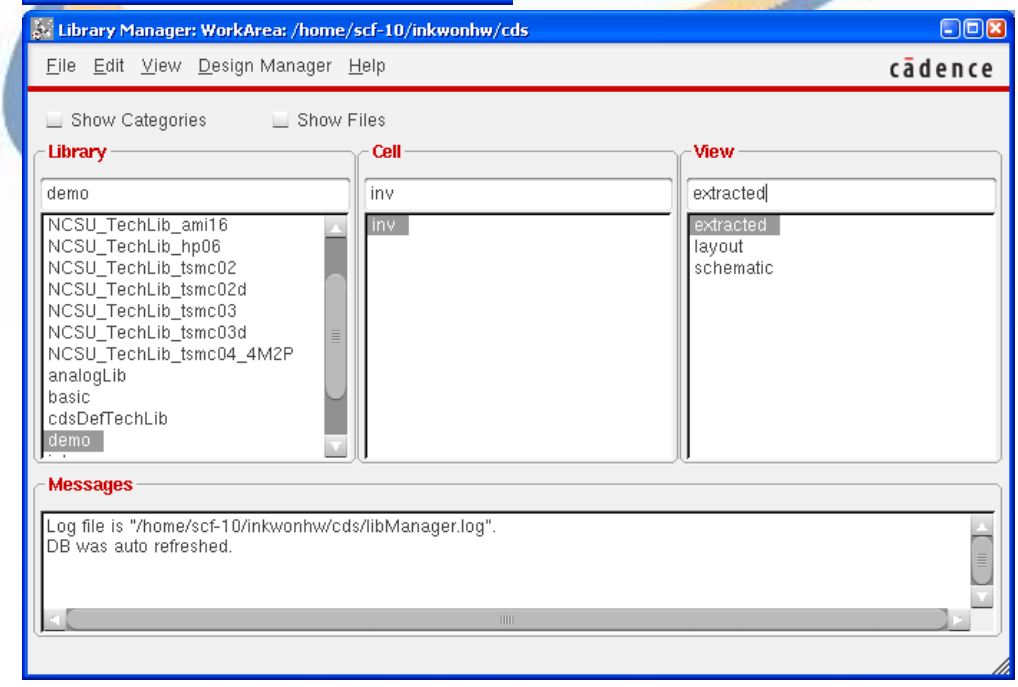
G. Extract

A layout is just a picture. If you need to run simulation using the layout, you should convert it to the other format. It is done by extracting. It's something like compiling a code.





Select 'Extract_parastic_cap' as a switch name, otherwise your extracted design won't have parasitic capacitances.

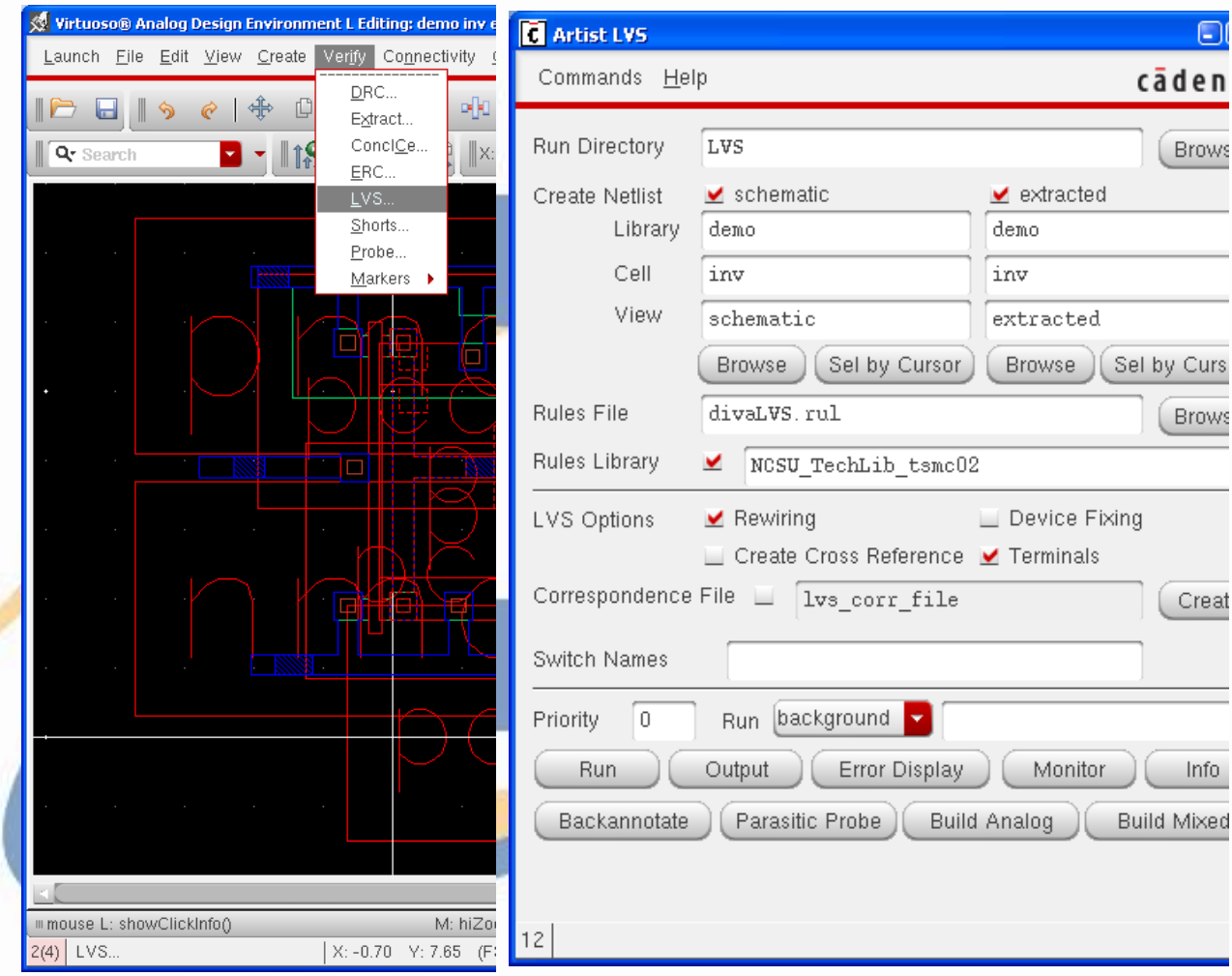


H. Run LVS

As I mentioned before, this step is very important for your grading. More complicated design, more time will be required for debugging LVS.

Verify → LVS

Keep in mind. You **SHOULD** compare your schematic with **EXTRACTED**.

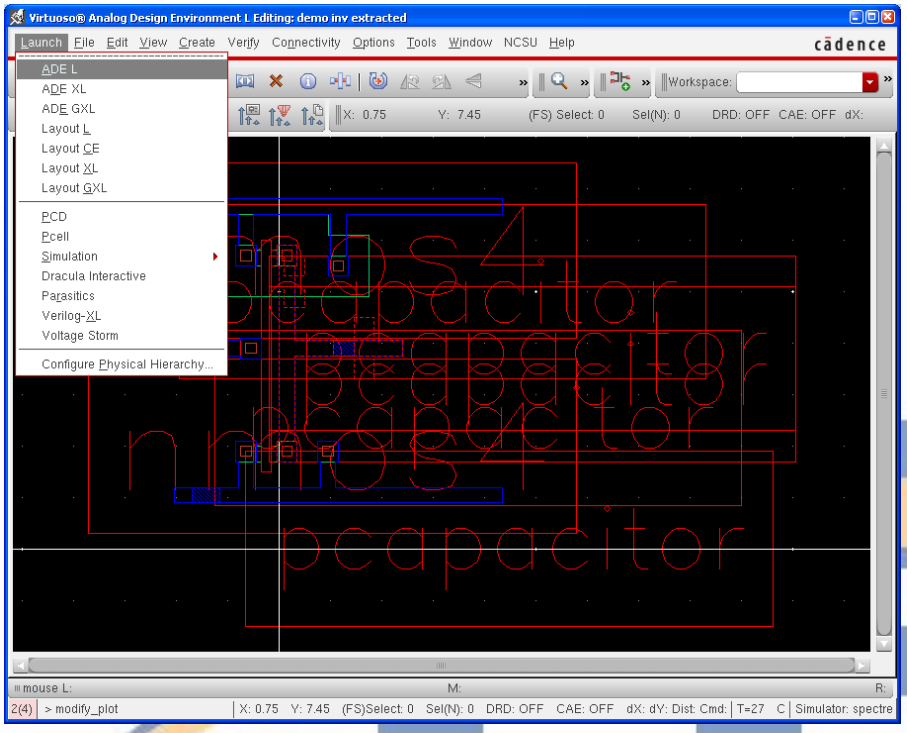


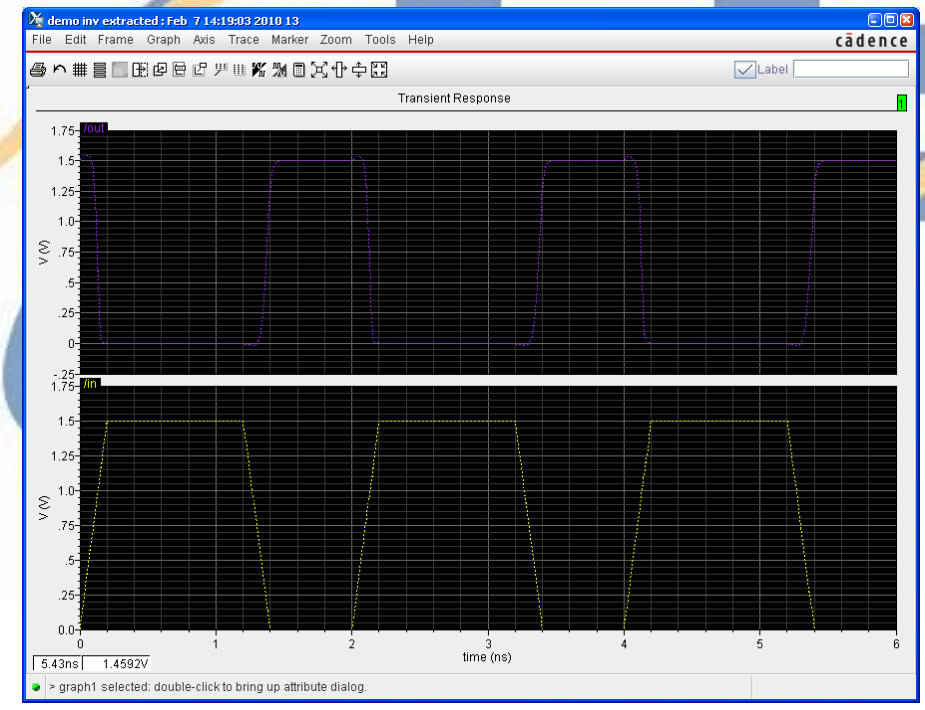
I hope all of you will see the following window.

If there are errors, you can check the results by clicking 'Output' button. 'Error Display' also might be helpful.

I. Run Spectre simulation

It is same as schematics. Go to step ‘4. Run Spectre simulation’.





Congratulations!!

You followed all steps I prepared. Let’s do the same thing for more complicated designs.