AJAY G. MISHRA

(PHYSICAL DESIGN ENGINEER)

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OBJECTIVES

To gain knowledge of all aspects of VLSI chip design and apply that knowledge in development & construction of leading edge products, IC, & chips. thereby adding value to the organization I Work for handling.

EDUCATION

ASIC Physical Design Trainee — **JAN 2023**
VLSI Guru Training Institute, **BENGALURU**

Bachelor of Engineering – Electronics and Telecommunication — **MAY 2020**
A.C Patil College Engineering & Technology**, MUMBAI** — C.G.P.A: **7.**87

12th Science (HSC) — **MAY 2016**
Model Collage Of Science & Arts,**MUMBAI** — Percentage: 66.33%

10th (SSC) — **MAY 2014**
NHHS, **MUMBAI** — Percentage: 88.80%

PROJECTS

- Hands on experience in Physical Design Flow of two projects on both S**ynopsys IC Compiler-II and IC Compiler-I tool,** 28nm technology in training at VLSI GURU Institute, Bengaluru (from July'22 to Jan'23).

TECHNICAL EXPOSURE & SKILL

EDA TOOL: SYNOPSYS IC COMPLIER, STAR RC, SYNOPSYS PRIME TIME, MATLAB, NETSIM, AUTOCAD, PACKET TRACER.

DOMAIN SPECIFIC PROJECT

VLSIGURU INSTITUTE, BENGALURU — **July to January 2023**

#1. Block Level Implementation of 32-bit RISC CORE Processor (Multi Voltage Design)

PROJECT: ORCA & VOLCANO

Design Specifications: Technology: 28nm
Standard Cells Count: 52007
Hard Macros: 40
Operating Frequency: 417 MHz
No. of Clocks: 8
Metal Layers: 9
Supply Voltage: 0.75 V and 0.95 V
IR drop: 5% of Supply Voltage
Total ports : 237(95 input ports & 142 output ports)

Tools: Synopsys IC Compiler, Star RC, Prime Time.

SUMMARY

- Hands on experience in Netlist to GDSII, floorplanning, placement, power planning, CTS(clock tree synthesis), routing, placement-optimizations, P&R/PnR, physical verification and ECO(engineering change order). asic and physical design & cad flow.
- Hands on experience on technology node like 28nm geometry & SOC(system-on-a-chip).
- Physical verification including drc(design rule checking), lvs(layout vs schematic), antenna effect, dfm(design for manufacturability).
- Aware about SI(signal integrity) issues like crosstalk, reliability issue like EM/IR drop.
- Static timing analysis (STA): experience in fixing setup & hold violation, identifying timing exceptions, and timing closure.
- Hands on experience in interpreting timing report at various stages of APR for different scenarios MCMM(multi-corner multi-mode), OCV(on chip variation) & CRPR.
- Familiar with various file formats: Netlist(.v), SDC, logical/timing library(.lib), Technology File(.tf) Physical library(.lef).
- Good Communication skills, Team player, & Problem solving / creativity skill.

ACADEMIC PROJECT

A.C Patil College Engineering & Technology, MUMBAI

1. IOT BASED SMART HOME **April 2020**

Description: The **Internet of Things** (or commonly referred to as IoT) based Home Automation system, as the name suggests aims to control all the devices of your smart home through internet protocols or cloud based computing.The IoT based Home Automation system offer a lot of flexibility over the wired systems s it comes with various advantages like ease-of-use, ease-of-installation, avoid complexity of running through wires or loose electrical connections, easy fault detection and triggering and above and all it even offers easy mobility.

2. Line Following Robot **Dec 2019**

3. Alcohol Detection With Vehicle Controlling **May 2019**

PERSONAL DETAILS

Date Of Birth	**:** 06 JUNE 1999
Languages Knows	**:** Hindi, English, & Marathi
Hobbies	**:** Playing video game, Traveling.
Nationality	**:** Indian
Permanent Address	**:** Mumbai, Maharashtra - 421306

DECLARATION

I hereby declare that above mentioned particulars are true to the best of my knowledge and belief.

PLACE :
DATE :

AJAY G. MISHRA