Akshay Wadinge

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Ichalkaranji-416115, Maharashtra

Career Objective

Seeking an opportunity to work as a Physical Design Engineer in various technology nodes to achieve best PPA(Power, Performance, Area) of an IC while contributing to the symbolic growth of organization.

Core Competancy

- Good knowledge of fundamentals of semicustom ASIC design flow (RTL to GDSII).
- Worked on designing of block level APR flow for 40nm technology.
- Hands-on experience in macro placement during Floorplaning, Powerplaning, Placement, Clock Tree Synthesis, Routing.
- Good understanding of Static Timing Analysis concepts-Setup Time, Hold Time, Transition, Delay, Skew, Jitter.
- Knowledge of estimation in minimum DRC'S, IR drop limits, minimum Congestions and Timing Closures.
- Understanding of Signal Integrity effects such as Xtalk Noise ,Xtalk Delay and issues like EM, Antenna, ESD.
- Generated and analyzed the timing reports on Prime Time and calculated various parameters-setup slack, hold slack, propagation delay.
- Hands-on experience with EDA Tools APR : Synopsys ICC-2, STA : Synopsys Prime Time. Examine and modifying Tcl-Script.
- Scripting Languages : Perl Scripting (Intermediate).
- Programming Languages : Verilog and VHDL (Intermediate). Working with the Linux Environment.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Shri Guru Gobind Singhji Institute of Engineering and Technology (SGGSIET), Nanded, with 8.67 CGPA

2018

Manere High school and Jr College, Ichalkaranji, with 81 %

SSLC **2016**

Marathi Medium High school, Narayan Mala, Ichalkaranji, with 95.40 %

Domain Specific Project

RV-VLSI DESIGN CENTER

Graduate Trainee Engineer Sep-2022 to Jan-2023

Block level Implementation of APR Flow

Description

Created optimized block level APR flow for “Lakshya sub-system” in 40nm technology to achieve the PPA — power, performance, area with respect to given constraints.

Tools

Synopsys — IC Compiler 2

Challenges

- Manual placement of macros in the core region with reducing the wire length and sufficient area available for standard cells and routing.
- Creation of efficient power mesh within the IR drop limit.
- Meeting the Clock tree DRC's — max transition delay, max load capacitance, minimum skew.
- Identifying and constraining the setup and hold slack for the timing paths in the design.

RV-VLSI DESIGN CENTER

Graduate Trainee Engineer Sep-2022 to Jan-2023

Static Timing analysis for various Timing Paths

Description

Interpreting the timing reports and analysis of setup and hold for the flip-flops and latch based designs considering uncertainty, CRPR, clock skew and dealing with timing exceptions such as multicycle paths, minimum maximum delay paths, false paths.

Tools

Synopsys — Prime Time

Challenges

- Understanding the concepts and different terms of STA for accurate analysis of timing reports.
- Generation and analysis of Timing reports with waveforms for different timing paths such as Input-Reg, Reg-Reg, Reg-output and Input-Output.
- Fixing the timing violations for setup and hold by using different techniques.

B.E / B.Tech Academic Project

Shri Guru Gobind Singhji Institute of Engineering and Technology (SGGSIET), Nanded

Wafer Fault Detection using Machine Learning

Description

Builded a classification methodology to predict the quality of wafer sensors based on the given training data, and it will give final result as wafer is faulty or not faulty.

Tools

PyCharm , Flask , Heroku

Challenges

- Collecting data from source and converting the data in user readable format. Tuning the data — finding the best parameters. Processing the data and finding patterns using machine learning algorithms.