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Career Objective

Seeking For an challenging positions to Utilize my skills and abilities in an organization that offers growth while being resourceful, Innovative anf Flexible

Core Competancy

- Hands On Experience on IC COMPILER II involving FLOORPLANNING, POWER PLANNING, PLACEMENT, CLOCK TREE SYNTHESIS AND ROUTING on 40nm technology node
- Worked on creating a floorplan according to the macro placement guidlines with good contiguous area and acceptable congestion between macros
- Analysing and verifying the DRC, LVS issues
- Understanding of Clock Tree Synthesis, types of clocks and non default routing rules of clock routing
- Good Knowledge in ASIC FLOW AND DIGITAL DESIGN and basics of MOSFET theory
- Familiar with usage of Synopsys IC COMPILER II
- Good Understanding Of STATIC TIMING ANALYSIS and timing closure at block level by analyzing the timing reports at multiple scenarios

Education Details

Advanced Diploma in ASIC Design **2023**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**
Krishna University College Of Engineering And Technology, with 6.7 CGPA

2018
Hyderabad Institute Of Excellence, with 93 %

SSLC **2016**
Bhaashyam Scientific High School, with 92 %

Domain Specific Project

RV-VLSI INSTITUTE

Graduate Trainee Engineer Nov-2022 to Dec-2022

FLOORPLANNING AND PLACEMENT OPTIMIZATION

Description

Floorplanning is an essential design step, it determines the size, shape and locations of modules in a chip and it estimates the total chip area, it interconnects and delays. place_optimization meets the timing, area and power specifications

Tools

IC COMPILER II

Challenges

- Macro Placement is challenge of system on Chip with large number of cores and memories
- Accurate Estimation of Power, Timing And Area
- Tining And Congestion Issues

RV-VLSI INSTITUTE

Graduate Trainee Engineer Dec-2022 to Jan-2023

CLOCK TREE SYNTHESIS AND ROUTING

Description

CTS is a technique for disturbing the clock equally among all sequential parts of VLSI design and balancing the clock delay to all clock inputs by inserting the buffers and inverters. routing makes physical connections between pins using metal layers

Tools

IC COMPILER II

Challenges

- Automatic clock tree synthesis engine puts a lot of buffers across the chip that are not desired
- Building clock tree separately with desired latency. This technique enabled meeting timing requirements for the mixed signal chip
- Macro Modelling Technique is to add insertion delay to the clock pins of specific registers in order to meet reg 2 reg timing paths

B.E / B.Tech Academic Project

Krishna University College Of Engineering And Technology

Hand Written Digit Recognition

Description

Hand Digit Recognition is used to recognize the Digits which are written by the Hand A handwritten digit recognition system is used to visualize artificial neural network

Tools

Python, CNN

Challenges

- Over Training