DEEKSHA R H

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To build a career in an environment that offers professional growth while being resourceful, innovative and flexible which helps to explore myself and realize my potential along with organizational growth.

Work Experience

1. Engineer – Design

Wipro Limited | June 2021 – present

Successful execution of ASICs from product definition to product release.

TSMC 5nm, Intel

- Automatic placement, CTS and routing with multi criteria optimization (power, area, timing).
- Timing closure support to maximize process node capability
- Analyzing and fixing RV issues.
- Writing eco's manually for some violations by analyzing section level STA sessions
- Worked on multiple blocks and provided RV, LV, caliber and timing clean database.

10nm, Intel

- Handled a block from synthesis to routing and did timing closure
- Took the design through first round of placement and then optimization
- Local hotspots were there for congestion, analyzed them, applied blockages.
- Written scripts to reduce LV violations
- Identified and fixed RV violations
- Supported other blocks to clear RV, LV and timing violations.

2. Trainee

Excel VLSI | July 2019 to March 2020

Worked on multiple projects to effectively understand advance concepts of ASIC flow.

Block Level Implementation of Leon Processor, 45nm

- Placement of macro cells with halos, placement and routing blockages and cell padding so that design is congestion free.
- Implementing power planning to make design floating pin free and ensure that all macro & standard cells are connected to VDD and VSS
- Debugging timing reports for different scenarios & fixing timing violations
- Fixing Physical & Logical DRVs
- Cleaning RV, LV and timing violations effectively

Block Level Implementation of ASIC Entity, 45nm

- Performed multiple iterations of floor plan and power plan to get the better placement of macros by avoiding notches and provided uniform area for placement of standard cells
- Tried and addressed congestion
- Fixing DRVs

Soft Skills

- Adaptable
- Team player

Industrial Skills

- Physical Design
- ASIC Design
- STA
- Tcl Scripting
- Reliability Verification

Tools/Platforms

- Synopsys: Fusion Compiler, ICC2, PrimeTime
- Cadence : Innovus, Genus, Tempus
- OS: Linux, Windows

Education

BE in Electronics and Communication – 7.3 CGPA
BIET Davanagere | 2015-2019

Class XII – 92.5%
Sir MV PU College Davanagere | 2013

Class X – 95.2%
STJHS Davanagere | 2011