ASHISH KUMAR
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PROFESSIONAL SUMMARY

- **11 months of** experience in **ASIC VERIFICATION** trainee**.**
- Proficient in writing **Verilog Codes, System Verilog Codes, UVM ,Testbench** and **Testcases**.
- Hands-on expertise of working on **Design** and **Testbench Development** in **Verilog, System Verilog and UVM Environment**.
- Good understanding of **UVM, System Verilog, Verilog, and Digital Circuits.**
- **Understanding of Protocols :AXI, APB , SPI.**

PROFESSIONAL EXPERIENCE

Role: ASIC Verification Engineer

PROJECT DETAILS:-

Project name: AXI Protocol TB Development in UVM.

Description: Build a Testbench for the AXI protocol.

Responsibilities and Roles:

- Using the AXI interface to connect the responder and the driver.
- Creating a setting with a master and slave agent.
- Reviewing the Scoreboard's outcome.
- Monitor and Coverage Port Interfacing.
- Driver sequencer and sequence port interface

Language: System Verilog

Methodology: UVM

Simulation Tool: QUESTASIM.

Project name: APB Protocol TB Development in UVM.

Description: Build a Testbench for the APB Protocol.

Responsibilities and Roles:

- Using the APB interface to connect the memory and the driver.
- Creating a setting with a master and slave agent.
- Reviewing the Scoreboard's outcome.
- Monitor and Coverage Port Interfacing.
- Driver sequencer and sequence port interface

Language: System Verilog

Methodology: UVM

Simulation Tool: QUESTASIM.

Project Name: Memory TB Development in System Verilog

Description: Design A code with the defined size (Width and Depth) for the required **Memory configuration**.

Roles & Responsibilities:

- Interfacing generator, bfm and mailbox.
- Developing an environment with configurable number of agents.
- Interfacing the testbench with design.

Language: System Verilog
Working Tool:MODELSIM, EDA Playground

Project Name: Design and Verification of Configurable Memory

Description:

Verilog Code for creating variable size memory and implementation of various Testcases.

Roles & Responsibilities:

- Implemented a memory which can be configured for user provided WIDTH and DEPTH.
- Implemented a testbench which supports the concept of **Front Door and Back Door Access**.
- Implemented **Testcases** for the verification of functionality as expected.

Working Tool: Modelsim, GVim

Project Name: SPI CONTROLLER

Description:

This project involves understanding of SPI Protocol and the external blocks it interfaces with.

Roles & Responsibilities:

- Implementation of design code for SPI Controller.
- Implementation of programming the registers and handling of SPI Protocol behaviour.
- Understanding the working of state transition of SPI Protocol from when it's in idle state till it has pending transactions to complete.
- Written testbench for the verification of the functionality as expected.

Language: Verilog
Working Tool: MODELSIM

Project Name: Interrupt Controller

Description:

Interrupt controller is a design used to collect interrupts from various peripheral controllers and forwards the interrupts to processor on priority basis. This continues till all interrupts are serviced by processor. It interfaces with processor on one side using APB interface and another side with peripheral controller. Interrupt controller has configuration registers for programming the various peripheral priority levels, interrupts are processed based on these values.

Roles & Responsibilities:

- Listing down **Design Features**.
- Generating design Verilog code.
- Creating **testcases** inside the testbench and writing **testbench coding in Verilog**.

Working Tool: Modelsim/Questasim/EDA playground, GVim

Project Name: Synchronous and Asynchronous FIFO

Description:

FIFO is a design component used for interfacing data transfer between two components eitherworking on same frequency or a different frequency. Implemented both Synchronous FIFO and Asynchronous FIFO using Verilog and testbench was also setup using Verilog. The design was implementedin such a way that there are no race or glitch conditions arise due to design working in two different clockdomains.

Roles & Responsibilities:

- Listing down **design features**.
- Generating design Verilog code.
- Creating **testcases** inside the testbench and writing **testbench coding in Verilog**.

Working Tool: Modelsim/Questasim/EDA playground, GVim

Project Name: Traffic Light Controller

Description:

Verilog Code for developing a simple **Traffic Light Controller** having four states using theconcept of FSM.

Roles&Responsibilities

- Implemented a TLC which can hold **Red-Yellow-Green states** using Up-counter.
- Implemented **testbench** for the same TLC to verify its functionality.

Working Tool: Modelsim/Questasim/EDA playground, GVim

Project Name:Pattern Detector.

Description:

This project involves understanding of state machines like Moore and Mealy.

Roles &Responsiblities:

- Understanding encoding styles, it's functioning and the most preferred style.
- Implementation of static and dynamic pattern detector.
- Implementation of design code to detect the desired pattern.
- Implementation of testbench with testcase like walking ones and zeroes, and seed concept.

Language: Verilog
Working Tool: MODELSIM

Project Name: Custom Clock Generation

Description:

Verilog Code for generation of clock for user provided frequency, duty cycle and jitter.

Roles & Responsibilities:

- Clock generation for **user provided frequency** by using **user specific time precision**.
- Clock generation for **user provided frequency, user provided duty cycle** and **user provided jitter**.

Language: **Verilog**
Working Tool: **Modelsim,Questasim,EDA playground, GVim**

TECHNICAL SKILLS

Languages:

- **Verilog,**
- **System Verilog,**
- **LINUX;**
- **Methodology:UVM**

Tools Used:

- **Modelsim,**
- **Questasim,**
- **GVim**

Protocols: **APB,AXI,SPI**

EDUCATION

- **M.Tech from NIT, Agartala in the year 2022 with 8.56 CGPA.**
- **Specialisation: VLSI Design**