

Nischay B S

nssr.nischay@gmail.com, 9632371606
Bengaluru-560079, Karnataka

Career Objective

Pursue a proactive career in the field of VLSI-PD and be part of an organization that gives me scope to continuously enhance my knowledge, skillsets and utilize the best of my technical and professional skills for organizational and personal growth.

Core Competancy

- Good familiarity with the flow of ASIC design, comprising Floor planning, Power planning and IR drop analysis, Placement, Clock-tree synthesis and Routing.
- Good exposure to concepts of STA, Signal Integrity, Physical Verification, Antenna violations and their fixation.
- Good hands-on experience with EDA tools like Synopsys Prime Time and IC compiler-2.
- Familiarity with working on 40nm technology nodes for flat designs.
- Experience in manual placement of macros looking into port and data flow lines to avoid routing congestions and fragmentation issues.
- Good understanding on DFT and scanchains.
- Familiar working in Linux environment and good hands-on with TCL and Perl scripting. Familiar with basics of C-language.
- Good understanding in analyzing the timing reports and fixing of setup and hold violations.
- Good basic knowledge on semiconductor device physics, CMOS working, logic design and Network analysis basics.
- Exposure to basic working of the FINFETs.

Education Details

Advanced Diploma in ASIC Design	2023
RV-VLSI Design Center	
Bachelor Degree in Electronics and Communication	2016
M S Ramaiah Institute of Technology, with 9.43 CGPA	
PUC	2012
VVS Sardar Patel Pre-University College, with 94.16 %	
SSLC	2010
Cordial High School, with 96.96 %	

Domain Specific Project

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer

Aug-2022 to Feb-2023

Lakshya Sub-system

Description

The project is an example created with an intent to understand the various aspects and challenges of VLSI Physical Design flow. It gives exposure to the real world complexities in the physical design.

Tools

IC Compiler-2 from Synopsys

Roles and Responsibilities

- Block level floor planning with manual placement of macros keeping in view the data flow lines, routing congestion and issues of fragmentation.
- Power plan with IR drop to be maintained well within the 5% threshold of the supply voltage, in addition to fixing of drc, missing vias and connectivity issues.
- Legalization issues at the placement stage. The drc and floating cells issues in the core region. The routing stage showed the blocked ports and antenna violations.
- The analysis of timing reports for setup violations in pre-cts, setup and hold violations in post-cts stages and further concluding on the possible reasons for its existence.

B.E / B.Tech Academic Project

M S Ramaiah Institute of Technology

Crowd Behavior Analysis using Optical Flow Method

Description

The optical flow methodology used in the project was helpful in overcoming the shortcomings of previously used methods for crowd behavior analysis, which failed in high density situations due to cluttering, partial occlusion and the computing costs.

Tools

Matlab

Challenges

- The need for sizeable quantum of data from the video feeds to arrive at the optimum value of optical threshold. The choice of the filter to be used to extract the details of the images. Implementation of foreground detection.