



Biki Teron

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*M.Tech, VLSI*

*Let's not get tired of doing good, because in time we'll have a  
harvest if we don't give up.  
Galatians 6:9*

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## Training

Institute : VLSI Guru (Bengaluru, Karnataka)  
Duration : July 2022 - February 2023  
Designation : Physical Design Trainee Engineer  
Trained : Yes

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## Work Experience

- Hands on technical expertise in Block level physical design implementation.
- Proper floor planning according to timing and power requirement.
- Resolving placement and routing congestion issues.
- Clock tree analysis and optimization
- Fixing timing and DRV violations.
- Good debugging skill in technical issues.
- Good knowledge and Understanding of Synthesis.
- Good knowledge on Static Timing Analysis.
- Good knowledge on Power IR Analysis.

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## Tool Used

Synthesis : Design compiler  
P & R : Synopsys IC Compiler II  
STA : Synopsys Prime Time  
RC Extraction : Synopsys StarRC  
IR Analysis : RedHawk

## Project Experience: Physical Implementaton of Multi Voltages 32-Bit RISC Processor (ORCA TOP)

Technology/Layers : 28nm / 9 Metal layers  
Foundry : TSMC  
Utilization : 75%  
Macros : 40  
STD cells : 52007  
No. of clocks : 3+3+2+1  
Low Power Design : Yes, PD\_RISC\_CORE = 0.95V & PD\_ORCA = 0.75V  
Target clock Frequency: 435MHz

### Objectives

- Performed sanity checks and did various iterations of floorplanning.
- Creating the floorplan with high importance for optimum performance.
- During Training, did various floorplanning with given Def and also by changing size of the block to get desired timing and congestion with reducing area.
- Pin placement was done with the help of guidelines given by top level.
- Place & route the design for meeting requirement.
- Applied various strategies to reduce skew and latency in cts stage.
- Fixed trans and timing violations and analyzed antenna violations and cross talk.
- Fixing post route issues using ECO.
- Performed sign-off for RC extraction and closed the timing.

### Award Achivement

- Karbi Langmet Amai.

### Extra-Curricular Activities

- Participated Cadence Tool Training Course for India-chip 2010 Tapeout at IIT Kanpur.
- Attended Short Course on Flexible Electronics, 2<sup>nd</sup>-7<sup>th</sup> July, 2018, IIT Kanpur.
- Attended short-term program on Modeling and Simulation of Nano-Transistors, 17<sup>th</sup> February - 7<sup>th</sup> March, 2021, IIT Kanpur.
- Attended Online Elementary FDP on "Modulation, Coding and Multiple Access Techniques for Wireless Communication and Storage Systems" from 15/11/2021 to 19/11/2021 at IIT Goa.
- Learning Silvaco for Semiconductor Simulation, Udemy, May 16, 2022.
- VSD - Physical Design Flow, Udemy, June 23, 2022.

### Education

2009–2011 **M.Tech.**, *IIT Guwahati*, North Guwahati, *CPI – 7.21*  
VLSI Design

2004–2008 **B.E.**, *Assam Engineering College*, Guwahati, Jalukbari, *Percentage – 63.03%*  
Electronics & Telecommunication Engineering

2002–2004 **Intermediate**, *Diphu Govt. College*, Diphu, *Percentage – 54.00%*  
Maths, Physics and Chemistry

2001–2002 **Xth Board**, *Kendriya Vidyalaya Diphu*, Diphu, *Percentage – 52.40%*  
Secondary School Certificate

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## Personal Details

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## Reference

1. Prof. Roy P. Paily  
Professor IIT Guwahati  
Head, Professor, Department of Electronics and Electrical Engineering  
IIT Guwahati

Homepage <https://www.iitg.ac.in/roypaily/>

2. Dr. Kuntal Deka  
Assistant Professor IIT Guwahati  
Department of Electronics and Electrical Engineering  
IIT Guwahati

Homepage <https://iitg.ac.in/eee/kuntald.html>

3. Dr. Chayan Bhawal  
Assistant Professor IIT Guwahati  
Department of Electronics and Electrical Engineering  
IIT Guwahati

Homepage <https://www.iitg.ac.in/eee/chayanb.html>

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## Declaration

I hereby declare that the above mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above mentioned particular.

Date: 27-3-2023

Place: Diphu

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