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Physical Design Engineer with 1+ years of hands of experience on different technology nodes(4nm, 5nm, 28nm, 45nm).

CAREER OBJECTIVE:

To secure a challenging position in a reputed company where I can have a penchant of learning and to play a key role in achieving company goals.

PROFESSIONAL SUMMARY:

- Strong Experience in Block-Level Implementation.
- Strong Experience in Floorplan, Powerplaning, Placement, CTS, Routing, STA, Physical Verification, and Synthesis.
- Hands-on Experience with EDA tools like ICC2,INNOVUS,PRIMETIME.
- Knowledge in digital design, CMOS, FINFET.
- Ability to work both as an individual and in a group.
- Undergone Physical Design training from GOLDENLIGHT SOLUTIONS, Bangalore . Duration: March 2021 –September 2021
- Currently working with **Aisemicon,Bengaluru.**

❖ **COURSE OUTLINE:**

Digital Design, CMOS & FINFET Fundamentals, Fabrication steps and process, Floor Planning, Power Planning, Placement, CTS, Routing, Static Timing Analysis, Physical Verification, and Synthesis.

Core Competency

Technical skills	
Linux commands	Working with files and directories
Physical Design	Knowledge of PNR flow and terminologies associated with Physical Design.
Static time analysis	Knowledge of terminologies related with STA
Tools	ICC, ICC2, Primetime, Design Compiler,. Innovus .
TCL	Working knowledge of TCL scripts which is used in EDA Tools.

Domain Specific Project

Project 1	**PHOENIX2 (AMD)**
Duration	**Live Project**
Technology	**5nm**
Tools	ICC2, PrimeTime
Project Description	This project was based on 5nm technology and PnR flow. Technology - 5nm, Macro Count - 63, Standard cell Count - 854372, Clocks – 8 ,Ports – 16020, Layers - 15
Responsibilities	Started the TileBuilder performed on the checks and reports of each stage in PnR and familiar with starting of TileBuilder, parallel and branch runs, updating the modified data of ICC2 to TileBuilder and updating tunables for a design. Manually placed macros, ports and keepout margins, blockages during floorplan, cleaned the Open and shorts in the design after routing, timing analysis in PrimeTime.

Project 2	**PHOENIX2(AMD)**
Duration	**Live Project**
Technology	**5nm**
Tools	ICC2 , PrimeTime
Project Description	This project was based on 5nm technology and PnR flow. Technology - 5nm, Macro Count - 39, Standard cell Count - 1594225, Clocks – 5,Ports – 18413, Layers - 15
Responsibilities	Performed analysis on report of each stage in PnR and familiar with starting of TileBuilder, parallel and branch runs, updating the modified data of ICC2 to TileBuilder and updating tunables for a design. Manually placed macro and keepout margins, blockages during floorplan. Analysis timing in PrimeTime and DRC analysis in Calibre.

Project 3	**LANAI - San Diego (QUALCOMM)**
Duration	**3 months**
Technology	**4nm**
Tools	PrimeTime
Project Description	Performed the Constraints ,Annotation and Link checks and also checked the input file Directories during Tag creation before starting PT Run.Familiar with the designshell,flowtracer,designview,Analysed the timing between start and end points,and resolved max path,min path Violations by increasing drive strength ,swapping between lnw6,ln6 , in Primetime session.
Responsibilities	Fv ,Clp in Aoss_wrapper and Accomplished floorplan manually for a Practice Design.

Project 4	**LEON (INSEMI)**
Duration	**2 Months**
Technology	**28nm**
Tools	Cadence Innovus , Tempus
Project Description	Technology - 28 nm, Macro Count - 4, Standard cell Count - 35614, Clocks - 6,Supply Voltage - 1.0V, I/O Pins - 1200 Metal Layers - 9
Responsibilities	● Manual placement of macros based on data flow lines, macro familyand ports. ● Iterations in adjusting the offset and number of power straps, pitch andtheir width to meet the IR drop target. ● Ensuring that design to be free from DRC violations, floating

	pins,floating wires by aligning the macros and giving placement and Routing blockages. ● Analyze design with acceptable congestion and distributed power withminimum timing. DRC's and building clock tree with optimized clock skew. ● Understanding the timing reports after each step of APR flow anddifferent placement switches for optimization. ● Design setup for CTS: cell purpose definition, clock buffers/inverters,don't touch cells. Understanding the tool behavior while Clock tree building and optimization of clock & data paths for fixing timing ● violations by balancing the skew.

Project 5	**Leon_Design (Training in GLS)**
Duration	**6 Months**
Technology	**32nm**
Tools	**ICC2, DC**
Project Description	Technology - 32 nm, Macro Count - 4, Standard cell Count - 251K, Clocks - 4 , I/O Pins - 1347, Metal Layers - 11
Responsibilities	Manually placed all the macros based on Hierarchy & Fly-line analysis.Perform Powerplan.Perform Pre-Placement & Std Cell Placement.Perform Timing & Congestion Analysis.Build Clock-Tree based on the specification.Performed Signal Routing.Perform Physical-Verification & Other Sign-Off checks. Performs Synthesis Flow i.e., Developing HDL file, Specify libraries, Read design, Define Design Environment, select compile strategy, Optimize the design, Analyze and Resolve Problems, Save the Design.

Certificates :

● Underwent an in-plant training at **DR NARLA TATA RAO THERMAL POWER STATION**, Vijayawada, Andhra Pradesh.
● Completed a 12- week online certification course in **Analog communication** from **NPTE**L, **IIT Kharagpur.**
● Completed **SIEMENS** courses of **BASICS OF PLC** and Process Instrumentation.
● Passed the **'C' certificate** examination in 'B' Grade held in 2019 under the authority of the **Ministry of Defence**, Government of India.
● Participated in **5-Day Entrepreneurship Awareness Programme** organized by start-up cell, SVU College of Engineering under **TEQUIP**, Sri Venkateswara University.
● Participated in Andhra Pradesh State Skill Development Corporation(APSSDC) for Internet of Things(IoT).
● Participated in the National Seminar for e-Learning and MOOC's in Higher Education.

Btech Project	**SMART IRRIGATION SYSTEM USING ARDUINO WITH GSM**
Project Description	A solution is proposed to automate the irrigation system using Arduino and the monitoring field by using photos captured by the camera.

Education

Course	University/college	Year	CGPA(%)
B.Tech (E.E.E)	Sri Venkateswara University College of Engineering, Tirupati	2020	7.44
Intermediate (M.P.C)	Sri Chaitanya Junior college, Vijayawada	2016	96.1 %
S.S.C	Keshava Reddy High School,Mamandur	2014	9.5 GPA

Declaration

I solemnly declare that all the above furnished information is free from error to the best of my knowledge and belief.

Dinesh.