LAVULURI DIVYA JYOTHI

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CAREER OBJECTIVE

Lavuluri Divya Jyothi here. I am a rookie with information that can help me advance my VLSI domain skills. I am seeking position which will provide an opportunity to explore, perform, excel in a competitive environment and to develop my skills and to put all my ideas on a proper platform to become a highly skilled professional.

PROFESSIONAL TRAINING

Advanced Physical Design and Verification Course
Maven Silicon VLSI Design and Training Center, Bangalore.
June 2022 till date.

EDUCATION

Qualification	Institution	Year of Passing	Aggregate (%)
M.Tech (VLSI & ES)	University College of Engineering ,Kakinada	2022	86
B. Tech (ECE)	St. Ann's College of Engineering & Technology	2019	82.84
Intermediate	Sri Vani Junior College	2015	94.9
SSC	Sri Vidya Bharathi Public School	2013	87.4

TECHNICAL SKILLS

VLSI Domain Skills

- HDL : Verilog
- EDA Tool : Mentor Graphics - Modelsim, Questasim and Siemens EDA - Tanner, Oasys, Aprisa.
- Operating Systems : Working knowledge on Windows and Linux
- Digital Electronics : Combinational & Sequential circuits, FSM, Memories.
- Verilog Programming : Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks, looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Races in simulation,
- Physical Design : Logic Synthesis, Floor planning, Placement, Routing, Clock Tree Synthesis and Timing Analysis using Aprisa, DRC, ERC, LVS and signoff using Calibre.
- STA : STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks, Clock domain and Variations, Clock Distribution Networks, Fixing timing failure.

PROJECT

Router 1*3

- Software : Model Sim, Quartus Prime
- Language : Verilog
- Modules : FIFO(4), FSM, Register, Synchronizer, Router Top.

Router is a device that transfers information in the form of packets based on address locations. I performed ASIC Design Flow on router project.

Reversible Logic Based Image Kernels for DIP Applications

- Software : Xilinx-ISE, Xilinx -Vivado
- Language : Verilog

Image kernels used for filtering and enhancing the images using reversible logic gates. The filter kernels implemented are Gaussian blur, Laplacian outline, Sobel, Emboss, Sharpen and Prewitt edge detection. The kernels are implemented individually using reversible logic gates and the designs are measured in terms of Area, delay and analysis the difference among the filter implementations and compare the parameter results among the six filters.

ACHIEVEMENTS

- I organized as a co-ordinator of 15th NATIONAL LEVELTECHNICAL SYMPOSIUM “VAIBHAV-2019” in St. Ann’s college of Engineering & Technology .
- I got 2nd price at “ Potti Sriramulu Chalavadi Mallikarjuna Rao College of Engineering And Technology” in technical quiz as part of JIGNASA-2018.
- I participated in “SITAR-2018” organized by Prasad V.Potluri Siddhartha Institute of Technology in paper presentation namely “LIGHT DECTION AND RANGING”.
- I published paper " Implementation of Hardware Efficient Reversible Logic Based Image Kernel for Image Processing Applications " in Journal of Emerging Technologies and Innovative Research.

STRENGTHS

- Adaptability and flexible to work
- Hardworking and quick leaner
- Well disciplined and punctual at work

DECLARATION

I hereby declare that the above said information is true to the best of my knowledge and as per record.

Place: Chinnaganjam, Andhra Pradesh

Date :

Signature