Yashwanth v

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Davanagere-577004, Karnataka

Career Objective

To obtain a career in Computer Hardware Industry as a Physical Design Engineer, where I can contribute my skills for organization's success and improving my technical ability while being resourceful, innovative and flexible.

Core Competancy

- Developed a power network with no physical DRC errors and also made sure to meet the specified IR drop by varying the width ,Spacing and pitch of the metals.
- Analyzing IR drop map and fixing the floorplan and power plan to solve the issue
- Hands on experience on tools Synopsys IC compiler II , Synopsys Primetime, cadence virtuoso,cadence innovas
- Manual placement of Macros based on data flow lines macros family and ports
- interpreting timing reports and fixing setup and hold violations
- Developed an floorplan with contiguous core area, good utilization and required channel pacing with the help of flylines and data flow diagram.
- Knowledge of static timing analysis -setup/hold concepts
- Hands on experience on technology nodes like 40nm ,90nm,180nm .
- Manual placement of macros based on macros family,ports and data lines
- Analyzing timing reports and fixing setup and hold violations

Education Details

Advanced Diploma in ASIC Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Alvas Institute of Engineering and Technology, with 6.8 CGPA

2018

Alvas pu college, with 82 %

SSLC **2016**

st johns convent, with 78 %

Domain Specific Project

RV vlsi Design center

Graduate Trainee Engineer Oct-2022 to Feb-2023

Implementation of PD flow

Description

operating frequency 833Mz ,operating voltage 1.1v, IR drom is 5% of operating voltage , staandard cells count 38887,macros count 38,metal layer 7

Tools

Synopsys IC Compiler II

Challenges

- Placement of macros according to the connectivity information in the core area
- Creating an efficient power mesh within the IR drop limit
- Meeting the CTS design Constraints, like maximum transition delay, maximum load, maximum fanout
- Analyzing the timing Reports and Fixing timing Violations

RV vlsi Design center

Graduate Trainee Engineer Sep-2022 to Oct-2022

STA for various Timing paths

Description

Validating the timing performance of a design by analyzing setup and hold timing reports for flip-flop and latch based design by considering uncertanity , CRPR, and dealing with timing exceptions such as false paths, multicycle paths.

Tools

Synopsys Prime Time

Challenges

- Analyzing setup and hold timing reports with waveforms.
- Analyzing the effect of clock insertion, OCV derates for various timing paths by undestanding the timing reports.
- Identifying the violations based on timing exceptions such as multicycle and false paths.

B.E / B.Tech Academic Project

Alvas Institute of Engineering and Technology

Buck Converter Using High Speed Processor

Description

Buck converter is a DC -DC converter which is used to convert 1.8 DC voltage to 0.9 DC voltage using VLSI in Cadence virtuoso. We have done the layout design of the Buck coverter

Tools

Cadence virtuoso

Challenges

- faced lot of problem in DRC and LVS check its rules while giving spaceing Transistor used in buck converter act as a switching device. Obtaining a continuous output is the main purpose of buck converter which can be achieved by using the energy store