MANU TYAGI

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A passionate engineer seeking to maintain a full-time position that offers professional challenges in the vlsi Front-end domain where I can utilize my extensive knowledge gained during my Training and professional courses.

Education

Bachelors of Technology: ECE
HMR Institute of Technology &Management.
2016-2020(September)
CGPA:7.58

Adarsh Public School,Vikas Puri
CGPA 7.8

Strength

Critical thinking
Accountability
Discipline

Languages Known

English
Hindi

Hobbies

Playing Baskeball.
Listening podcast
Writing Articles

Training

ADVANCED VLSI DESIGN & VERIFICAION
Maven Silicon | March'22- till date

Technical Skills

HDL*:* Verilog **HVL** : System Verilog
Verification Methodologies*:* Coverage Driven CRCDV, Assertion Base SVA
TB Methodology : UVM
EDA Tools *:* ModelSim - Intel FPGA Starter 10.5b, Mentor Graphics Questasim, Xilinx ISE Design Suite,Quartus prime 17.1.
Scripting language: perl. .
Protocols: SPI, UART,I2C , AXI, AHB.

Certificate

- **Enn Technologies Vlsi course : Design with Verilog**.
- **IEEE HMRITM General Secretary**
- IIT Delhi Ethical Hacking participant.
- IEEE IGDTU Modeling and simulation of TFET as Biosensor.
- MARC Springer volunteer.
- Defence Research and Development Organization **(DRDO)** Lastec lab
- WebTek Labs Pvt.Ltd**. Embedded And Robotics Using ARM**
- Kodding certified: Machine Learning Using Python
- NIIT Core Java certified.

Projects

Project#1

AMBA AHB2APB Bridge - RTL Design and Verification

HDL: Verilog, HVL: System Verilog, TB Methodology: UVM
EDA Tools: QuestaSim and Quartus-prime.

The AHB to APB bridge is designed as an AHB slave which converts AHB transactions to APB transactions by implementing pipelining at the AHB slave interface. Thus, the bridge supports AHB burst transfers.

Project#2

Router 1X3 – RTL Design and Verification

HDL: Verilog
EDA Tools:Modelsim, Quartus Prime and Questasim

Generated functional and code coverage for the RTL verification sign-off.

Project#3

RAM SOC RTL Design and Verification:

Verification - System Verilog
TB Methodology - UVM
EDA Tools - Questa Sim, Quartus Prime.

RAM SOC, is a chip consisting of 4 Memory modules each module is a 4096x64 memory unit, addressed using 12-bit addresses and data ports each of 64-bit, and is constructed using structural modeling.

Project#4

Synchronous and Asynchronous FIFO Design and verification:

EDA Tools - Model Sim, Quartus Prime
Design - Verilog HDL
Verification – Verilog.

Synchronous and Asynchronous FIFO, parameterized with Memory Depth and Width parameters, and performs parallel Read and Write operations.

Project#5 (B-tech)

1.Smart mirrors security with IOT connectivity
2.Drdo project – Design Instrumentation Amplifier
3.Using web cam as an alphanumeric detector

Declaration

I hereby declare that all the information contained in this resume is in accordance with facts or truths to my sense. I takefull authority for the correctness of the written information

Manu Tyagi