**Gottam Shiva prasad**
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## Career Objective

To excel as a Physical Design Engineer and hold up a challenging position in the semiconductor world through dedication and diligence and to ensure that I would work at mybest to do justice to an organization I work with.

## Core Competancy

- Good awareness of ASIC flow and know importance of each flow.
- Hands on experience in leading APR design tools like SYNOPSYS ICC II ad STA tool SYNOPSYS PRIME TIME.
- Analyzed and understood the design constraints to specify OCV, PVT corners, false paths, half cycle paths, CRPR.
- Good understanding of STA and timing constraints.
- Worked on placement with power aware and zero congestion, ensuring good routability
- Analyzed and understood the log files and reports of each stage in the PNR tool.
- Good knowledge in Logic Design, CMOS and Basic Electronic Devices.

## Education Details

**Advanced Diploma in ASIC Design** **2020**

RV-VLSI Design Center

**Bachelor Degree** in **Electronics and Communication** **2019**

Matrusri engineering college, with 68.3 %

**12th** **2015**

Sri Chaitanya jr college, with 91.4 %

**SSLC** **2013**

Srivani gurukulam , with 88 %

## Professional Experience:

- Working as Physical Design Engineer at TechMahindra from Mar-2021 till present.

## Technical Expertise:

- Synthesis : Synopsys DC, FC
- Place & Route : Synopsys ICC2, FC
- STA : Primetime
- Signoff Tools : Synopsys .
- ICC2 for DRC Fixing.

## Domain Specific Project:

Tools used: ICC2 , primetime

Technology node: 40nm

Challenges :

- Placement of macros by data flow diagram, creating blockages and optimal spacing between the macros to avoid congestion.
- Fixing setup and hold violations by minimizing skew using buffering techniques in clock and data paths.

| Project Profile | |
|---|---|
| **Project 1** | **Description** : 7 nm technology (Intel)<br>**Responsibilities:**<br>• Performed Floorplan, placement, CTS and routing to meet the timing/area/ congestion requirements and done incremental ECOs to meet all quality constraints.<br>• Implemented various challenges in PV and Sign-off flows for tape in Quality.<br>• Fixes all caliber (quality) violations<br>• Involved in various layout edits during ECO implementations, fixes like DRC, LVS mismatch, Antenna, DFM, signal route improvements, shielding and many other edits for PV or for timing/SI. |
| **Project 2** | **Description:** 5 nm technology (TSMC)<br>**Responsibilities:**<br>• Owned partition and converged from Netlist to GDSII, design was targeted to meet slack by various techniques which include floor planning, power planning, placement, CTS and detail routing.<br>• After analyzing the design, started reducing the routing congestion and placement congestion for obtaining better timing results.<br>• Fixed all DRV/caliber violations. |

## Self-appraisal:

I hereby declare that the above information furnished is true and correct to the best of my knowledge.

Place: Bangalore

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