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Career Objective

Willing to work as a Physical Design Engineer in a VLSI company and looking forward to take up challenging assignments in the related field of industry and to set new industry benchmarks in everything I endeavor

Core Competancy

- Basic Knowledge in ASIC design flow
- Good understanding of the inputs and outputs of all stages in the Physical Design (Floor Plan , Placement, CTS, Routing)
- Knowledge On Concepts of STA Analysis
- Analyzing IR drop and Fixing in the Floor Plan
- Hand on Experience on tool like PT shell and ICC shell
- Analyzing and Fixing the DRC Violations
- Manual Placement of Macros based on Fly-line analysis and ports
- Analyzing and Fixing the Congestion
- Knowledge on CMOS theory
- Generating and analyzing the Timing Reports of each step in Physical Design

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**
S R K INSTITUE OF TECHNOLOGY, with 6.48 CGPA

2019
SIR C.R.R. POLYTECHINIC , with 80.86 %

SSLC **2016**
SREE GANESH EM & TM HIGH SCHOOL, with 7.0 %

Domain Specific Project

RV-VLSI AND Embedded System Design Center

Graduate Trainee Engineer Oct-2022 to Feb-2023

Block Level Implementation Of APR Flow

Description

Block Level Implementation in 40nm technology ,Operating Frequency :833MHz, Voltage:1.1V,Voltage Drop is 5% of operating voltage ,Standard cells:38887 Macros:34, Metal layers:7

Tools

Synopsys ICC compiler

Challenges

- Providing (Space, Width, Pitch) according to IR drop
- Analyzing the timing reports and fix the timing violations
- Fixing Routing Congestion

RV-VLSI AND Embedded System Design Center

Graduate Trainee Engineer Sep-2022 to Jan-2023

Static Timing Analysis On Different Timings Paths

Description

Performed STA on Various Timing paths for both Flipflops and latches which comprise of setup and hold timing reports and there by understanding the slack

Tools

Synopsys Prime Time shell

Challenges

- Fixing setup and hold violations
- Knowledge on basic concepts and different terminologies used in STA for accurate analysis of timing reports.
- Generation and analysis of Timing paths with waveforms for various timing paths

B.E / B.Tech Academic Project

S R K INSTITUE OF TECHNOLOGY

A Reliable Routing Algorithm for Energy Efficient WSNs

Description

To Improve the life time of a network and reduceing the energy consumption of Network

Tools

MATLAB

Challenges

- Quality of Service , Reducing the Energy Consumption of a network , Average number of hops