Sampathirao Srihari Raju
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Career Objective

To contribute as STA/SoC Design Engineer for company's growth and advancements in technology by working on latest technology node.

Core Competancy

- Complete understanding of ASIC design flow from RTL to GDSII and PD flow involving Floor planning, Power planning, IR Drop Analysis, Automatic P&R, CTS and Routing.
- Good Knowledge of STA concepts like delay arc, fixing timing slack violations, CDC, SI, GBA, PBA, MCMM, OCV, AOCV, POCV, CRPR, time borrow, clock latency and useful skew.
- Good Knowledge of sign Off checks such as DRC, LVS, LEC, EM, IR Drop Analysis, ESD, ERC and antenna effects and methods of fixing them.
- Analyzing and interpreting timing reports for fixing timing violations.
- Good Knowledge of logical effort, DFT, low power implementation techniques and latest transistor technologies like Fin-FET.
- Good working knowledge of LINUX and scripting languages Perl/ TCL.
- Analyzed and understood Design Constraints to specify PVT Corners, False paths, Half cycle, Multi Cycle paths, Asynchronous Clocks, Clock gating.
- Hands on experience with Floor plan, power plan, IR drop analysis, Placement, CTS, Routing and DFM (DFY).
- Hands on experience on Synopsys Prime Time and PnR tool IC Compiler II, Mentor Graphics, Xilinx ISE and Tanner EDA.
- Good knowledge of Logic Design Concepts, CMOS, MOSFET, Semiconductor Theory, basic Electronic Devices, Verilog, Network Theory and Analog electronics.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2022**
RV-VLSI Design Center

Master Degree in **VLSI & ES** **2022**
Jawaharlal Nehru Technological University, Kakinada, with 8.67 CGPA

Bachelor Degree in **Electronics and Communication** **2020**
Rajiv Gandhi University of Knowledge and Technologies, Nuzvid, with 8.33 CGPA

2016
Rajiv Gandhi University of Knowledge Technologies, Nuzvid, with 84.5 %

SSLC **2014**
Kendriya vidyalaya vizianagram, with 93.3 %

Domain Specific Project

RV-VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Jul-2022 to Aug-2022

FLOOR PLAN AND POWER PLAN

Description

A design with 40nm Technology, 34 Macros, 41000 Standard Cells, 4.2mm sq. area, 1GHZ as Clock Frequency, Rectilinear shape, 1.1v as Operating Voltage, 600mw as power budget, Number of metal layers - 7, IR drop < 55mV.

Tools

Synopsys IC Compiler II

Challenges

- Manually placing hard macros using data flow diagram in such a way that to provide the maximum contiguous core area and to make all pins of the macros are accessible.
- Implementing power plan to meet the target IR drop and made power mesh DRC clean.
- Maintaining uniform orientation of hard macros and adding placement and routing blockages in required locations.
- Performing timing checks using Zero Wire Load Model in order to qualify Netlist.

RV-VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Jun-2022 to Jul-2022

Static Timing Analysis (STA)

Description

Timing Analysis on different path groups for register and latch based design, having multiple clocks, multi-cycle paths and half cycle paths.

Tools

Synopsys Prime Time

Challenges

- Generating the timing reports and analyzing them in order, understanding the concept of slack, useful skew.
- Understanding of delay tables in order to calculate delay across various timings arcs.
- Analysis of different timing exceptions like false path, multi-cycle paths and half cycle paths.
- Analyzing the report based on with and With-out Derate Factor to calculate CRPR.

RV-VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Aug-2022 to Sep-2022

PLACEMENT AND CLOCK TREE SYNTHESIS

Description

Timing driven and congestion aware standard cell placement in Non-SPG flow is being done with optimum core utilization and building clock tree and routing all clock pins with optimized clock skew in both classic and CCD modes.

Tools

Synopsys IC Compiler II

Challenges

- Performed timing driven and congestion driven placement and HFNS in order to minimize logical DRCs by thus improving timing QoR.
- Synthesizing clock tree by providing NDR rules and performed detailed routing for all clock nets with DRC clean in both classic and CCD modes.
- Performed sanity checks before and after each stage of physical design flow.

RV-VLSI AND EMBEDDED SYSTEMS DESIGN CENTER

Graduate Trainee Engineer Sep-2022 to Oct-2022

ROUTING AND DFM (DFY)

Description

Routing all standard cell pins and hard macro pins using metal layers, performing via optimization and post route optimization by taking into account of cross talk effects on timing.

Tools

Synopsys IC Compiler II

Challenges

- Fixing antenna violations using metal hopping and antenna diodes manually.
- Clearing all DRC violations and LVS violations in order to make sure that design can be manufacturable.
- Analyzing timing reports and other reports in each stage.

B.E / B.Tech Academic Project

Rajiv Gandhi University of Knowledge and Technologies, Nuzvid

Energy-Efficient Low-Latency Signed Multiplier for FPGA-based Hardware Accelerators

Description

Multiplication is one of the most extensively used arithmetic operations in a wide range of applications, such as multimedia processing for such applications, multiplier is one of the major contributors to the energy consumption, critical path delay and resource utilization.

Tools

Xilinx ISE 14.7

Challenges

- while designing signed multiplier we should increase the speed, decrease the area and we should get the accurate results.

M.E / M.Tech Academic Project

Jawaharlal Nehru Technological University, Kakinada

A low-Power Timing-Error-Tolerant Circuit by Controlling a clock

Description

In this project, we implemented timing error tolerant circuit and timing error tolerant circuit using time borrowing. By controlling clock, we are able to achieve low power. But, as the number of stages increases the power also increases.

Tools

Tanner EDA

Challenges

- To achieve power reduction in this project, we are implementing one of the low power techniques, clock gating technique. Here clock gating is applied to the D-flip-flop in timing error tolerant circuit.