Abhinand K P

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Education

Degree/Certificate	Institute/Board	CGPA/Percentage	Year
B.Tech. (EEE)	Mar Athanasius College of Engineering , Kothamangalam	7.38	2018-2022
Senior Secondary	Govt.Model Higher Secondary School, Mananchira	88.92%	2017
Secondary	Kendriya Vidyalaya No.1 Easthill, Calicut	8.2	2015

VLSI Projects

- **Design of Pattern Detector** *December 2022*
  Tools: Verilog,Questasim Remote
  – Pattern detector on a serial input is designed using Moore and Mealy FSM and noticed a change in the number of states.
  – It requires coding an FSM to detect each pattern until it reaches the final pattern.
  – Implemented testbench that randomly generates a series of 1s and 0s to check the pattern.

- **Design and Verification of FIFO** *December 2022*
  Tools:Verilog, Questasim Remote
  – FIFO is a design component used for interfacing data transfer between two components either working on the same frequency or at a different frequency.
  – Both Synchronous and Asynchronous FIFO are implemented using verilog and RTL code.
  – This project was verified for its functionality by writing testbench in verilog.

- **Single Port and Double Port RAM** *January 2023*
  Tools:Verilog, Questasim Remote
  – The Single Port RAM block models RAM that supports sequential read and writes operations but if you want simultaneous read and write operations then we can use Double Port RAM.
  – Both Single port and double port RAM were designed using verilog and are implemented using verilog RTL code.
  – This project was verified for its functionality by writing testbench in verilog and simulated using Questasim.

- **Design and Verification of APB Protocol** *January 2023*
  Tools: System Verilog, Questasim Remote
  – APB(Advanced Peripheral bus) is a non-pipelined protocol optimized for low power and low bandwidth peripherals.
  – This project consists of a master and a slave which has been designed using FSM in System Verilog.
  – The master and slave are then interconnected to each other in a top module by instantiating the master and slave module .
  – The project has been verified and tested for its functionality using system verilog.

- **Design and Verification of UART Using Verilog** *February 2023*
  Tools:Verilog, EDA Remote
  – UAR stands for universal asynchronous receiver transmitter is one of the most commonly used communication protocols.
  – This project consists of a master and a slave which has been designed using FSM in System Verilog.
  – UART consists of a baud rate generator which consists of a counter that helps us provide the timing information at the transfers .
  – It also consists of a transmitter and receiver which are used to transfer data.
  – The two modules were designed in verilog and interconnected by instantiating in the top module and were verified for their functionality by using testbench in verilog.

Academic Projects

- **Autonomous Bicycle - Obstacle Avoidance and Real-time Positioning** *May 2022*
  Tools: Arduino,Proteus Ernakulam
  – We developed an Autonomous Bicycle driven by a Rectangular geared DC motor and 12v battery.
  – The Aim of this Project is to provide an on-demand bicycle to promote a bicycle-sharing system (using obstacle avoidance and real-time positioning.
  – The obstacle Avoidance is done through a stepper motor fitted to the handle of the bicycle.

Key Courses Taken

- **RTL Design and Verification Course**: VLSI For All Pvt Ltd November 2022 - Ongoing

Skills Summary

•**Technical skills**: Digital Electronics, Analog Electronics, Electric Machines, Electric Vehicles
•**Protocols** : APB, SPI, I2C, UART
•**Languages** : Verilog, System Verilog, C Programming
•**Tools** : Gvim Editor, Questa Sim, Proteus, Solid Works
•**Soft Skills** : Leadership, Event Management, Listening, Problem-Solving, Time Management

Publications

- **Autonomous Bicycle: Obstacle Detection and Real-time Positioning** *June 2022*
  Research Article Ernakulam
  – Published by International Journal of Engineering Research and Applications(IJERA) ISSN:2248-9622, Vol.12, Issue 8, August 2022, pp. 27-33 (June 2022)

Awards and Certifications

- Winner Among Kerala Team in All India EBAJA Competition conducted by SAE India.
- NPTEL Certification on Digital circuits.
- Participated in MegaATV Competition Conducted by Autosports India
- Professional Certification in Electric Vehicle Design by Delft University.

Positions of Responsibility

- **Sports Club Secretary**: Students Senate Member, MACE *November 2021 - June 2022*
- **Administration Team Member**: Organized events, conducted workshops in College Cultural fest *May 2022*

Languages

- English
- Hindi
- Malayalam