A V Roshan Dev

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Bhopal-462047, Madhya Pradesh

Career Objective

As a dedicated Engineer, I am seeking a job which allows me to continue learning with new technologies and innovations by performing my improved skills and to encourage me to flourish as a Learner.

Core Competancy

- Fundamentals of ASIC design flow (RTL to GDSII).
- Extensive knowledge in concepts of Static Timing Analysis.
- Well experience with EDA Tools, APR: Synopsys ICC-2, STA: Synopsys
- Examine and modifying TCL script, Primetime tool.
- Perl scripting language.
- Basic knowledge of C, Verilog and VHDL.
- Compatible working with Linux system.
- Internet Of Things (IOT).

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Lakshmi Narain College of Technology, Bhopal, with 7.87 CGPA

2018

World Way International School, Bhopal, with 65.8 %

SSLC **2016**

World Way International School, Bhopal, with 64 %

Domain Specific Project

RV-VLSI DESIGN CENTER

Graduate Trainee Engineer Oct-2022 to Feb-2023

Static Timing Analysis for various timing paths

Description

Setup and Hold analysis and interpreting timing reports, dealing with False Paths, Half cycle paths, Multi-Mode paths, Reporting the violations in the logical DRC's

Tools

Synopsys Prime Time

Challenges

- Computing setup and hold slack.
- Analyzing the Timing Reports with generated waveforms
- Studying and understanding the usage of timing exceptions and it's concepts.
- Constraining the identified timing paths.

RV-VLSI DESIGN CENTER

Graduate Trainee Engineer Oct-2022 to Feb-2023

Block level Placement and Clock Tree Synthesis

Description

A Timing driven and legalized placement of standard cells thereby ensuring good routability. Building a Clock Tree to get an optimized skew, reduced timing violations, design rule violations and minimum WNS, TNS.

Tools

Synopsys IC Compiler 2

Challenges

- Analyzing timing delay after every step.
- constraining power consumption of Clock
- Analyzing Timing Reports.

RV-VLSI DESIGN CENTER

Graduate Trainee Engineer Oct-2022 to Feb-2023

Block level Floorplanning and Powerplanning

Description

Implementation of block level design for Lakshya subsystem in 40nm technology. Supply voltage: 1.1V, IR drop: 5% of operating voltage, Standard cell count: 38887 and Hard macros:34, Frequency of operation: 833MHz, 5 clocks, 7 Metal layer.

Tools

Synopsys IC Compiler 2

Challenges

- Putting together an efficient power mesh with in thr IR drop limit.
- Fixing floating shapes for metal layer and fixing if any.
- Placement of macros using appropriate data flow diagram of block.

B.E / B.Tech Academic Project

Lakshmi Narain College of Technology, Bhopal

Ultrasonic sensor Touchless Door Bell.

Description

We created a doorbell that detects object within given distance of 2-15cm and buzzer indoor with just a gesture which will be very usefull for social distancing at COVID like pandemic. It can also be used as motion detectors for security purposes.

Tools

ATMEGA328p microcontroller, ultrasonic sensor, pcb designing, IC 7805, a buzzer, 12v DC input, LEDs, 16MHz crystal oscillator, 1k ohm resistor, diode, a preset, filter capacitor.

Challenges

- - Designing and Making PCB. - Choosing and ordering components according to our circuit design. - Microcontroller programming. - Soldering components in the PCB to complete circuit board.