NIRAJ DUBEY

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CAREER OBJECTIVE:

Seeking a respectable position in a prominent organization that offers professional growth with mental satisfaction to utilize my skills and abilities while being **resourceful, innovative ,and flexible.**

EDUCATIONAL QUALIFICATION:

QUALIFICATIONS	INSTITUTIONS	YEAR	MARK
B.TECH (ECE)	TECHNOCRATS INSTITUTE OF TECHNOLOGY AND SCIENCE	2017-2021	8.7 CGPA
CLASS 12TH (UP BOARD)	GOVT ATS	2017	67.2%
CLASS 10TH (UP BOARD)	GOVT ATS	2015	83%

ACADEMIC PROJECTS:

Bluetooth Control Devices (Home Automation) using **ESP 8266 Micro Controller.** A setup is designed for controlling all the electrical appliances using Microcontroller Relays, Bluetooth Hc05 Module.

Core Competancy:

- Good knowledge of VLSI design flow - **ASIC design flow (RTL to GDS II)**

- Hands on experience in **synthesis, sanity checks.**

- Hands on experience in **PNR** flow using ICC2,Design Compiler tools by Synopsys.

- Having technical exposure on **Floor Planning, Place and route, Clock Tree Synthesis, Timing Analysis, DRC/LVS, Crosstalk analysis, IR drop analysis**

- Good knowledge of **MOSFET , CMOS** and its operation in different regions.

- Having technical exposure on **CMOS VLSI Digital Design**

TECHNICAL SKILLS:

Operating System	Windows XP /7/8/9/10, LINUX
Programming Language / Scripting Language	C, TCL
EDA Tools	**Synopsys** EDA Tools:(ASIC DESIGN) • Floor plan , PNR – IC COMPILER II • Synthesis – Design Compiler • Timing closure – Prime time • Physical verification – IC Validator • RC extraction – Star RC

PROFFESIONAL TRAINING:

Physical Design training from **ChipedgeTechnologies Pvt. Ltd, Banglore**

Using Synopsys IC Compiler II during August 2022 to December 2022.

PROJECT EXPERIENCE:

Project 1: **CHIPTOP**

Technology/ Metal layers	14nm/9 Metal Layers
Macros	4
Standard Cells	6108
No of Clock	1
Frequency	200 MHZ
Tools Used	Design Compiler, ICC **II** Compiler by **Synopsys**
Role	Synthesis, Design Import, Sanity checks, Floorplan, Powerplan,

	Placement, Timing Optimization, CTS , Routing, Timing Analysis, LVS and DRC

PROJECT 2: **JBI**

J –BUS Interface is one block in the open Sparc processor.

Technology/ Metal layers	28nm/9 Metal Layers
Macros	46
Standard Cells	47938
No of Clock	2
Frequency	0.263 GHZ
Tools Used	Design Compiler, ICC **II** Compiler, Star- RC, Prime time by **Synopsys**
Role	Design Import, Sanity checks, Floorplan, Powerplan, Placement, Timing Optimization, CTS , Routing, Timing Analysis, LVS and DRC, Design-Closure

JOB EXPERIENCE:

Currently Working as a PCB Test Engineer in **BHARAT ELECTRONICS LIMITED**

There I used to captured the waveform of various electric test of **BU ,CU & VVPAT**

INTEREST & HOBBIES:

Reading Books

Sports (Cricket, Badminton)

PERSONAL DETAILS:

Father Name : Dayashankar Dubey

Date of Birth : 21.07.1999

Language Known : Hindi , English

DECLARATION:

I hereby declare that all the particulars furnished above are authentic to best of my knowledge and belief.

Signature

Niraj kumar dubey