

Name: Patan Mansoor

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Career Objective:

To make a sound position in corporate world and work enthusiastically in team to achieve goal of the organization with devotion and hard work.

Training:

- Trained on SV, UVM& basic protocols in **EDIC SEMICON PVT.LTD, Hyderabad** .Working as DV engineer in EDIC SEMICON PVT.LTD.

Experience Summary:

- Knowledge on Verilog, VHDL and SystemVerilog
- Knowledge in C programming
- Expertise simulation tools such as Aldec Riviera Pro, Questa sim & cadence-Xcelium.
- Knowledge of UVM and SV Env.
- Knowledge on basic protocols and basic of pcie.

Technical Skills:

- HDL Known : Verilog HDL
- HDVL Known : System Verilog HDVL
- Methodology : UVM
- Tool : Cadence-(Xcelium), VManager & Questa sim.
- Operating systems : LINUX

Career History:

Company	Location	Years
BEL	Bangalore	2020(Feb)– 2021(Jun)

Project Handled:

Verification of AXI Protocol in system verilog and UVM.

Description: The AXI IP level verification is done by using SV, UVM environment by creating AXI agent. Different cases have been built to generate the stimulus in all the ways to cover the functionality.

Responsibilities:

- Understood the AXI protocol and its requirements. Developed the test plan.
- Verified all the response, transfer types and all supported burst operations.
- Implemented UVM components and created the sequences as per the specification.
- Worked on functional and code coverage (Toggle, FSM, Line, Expression and Condition etc).

Academic Profile:

- Bachelor of Technology (B.Tech) in Mechanical Engineering from Sree Venkateswara College in 2019.
- Diploma (Polytechnic) in Automobile Engineering from Government Polytechnic College in 2016.
- SSC from Srinivasa concept school in 2013.

Personal Details:

Gender	:	Male.
Nationality	:	Indian.
Date of Birth	:	16-Jan-1997.
Languages known	:	English, Hindi, Telugu, Urdu.

Declaration:

I Patan Mansoor, hereby declare that the information contained here is true and correct to the best of my knowledge and belief.

Patan Mansoor