Jataved Kambalimath

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Bagalkot-587102, Karnataka

Career Objective

To be part of Semiconductor workspace where I can utilize my knowledge and skills as a PD engineer and get opportunity to learn more. Be a part of Emerging technology and grow along with the Company.

Core Competancy

- Knowledge and skills on ASIC PD Flow involving floor plan, Powerplan, IR drop analysis, Automatic P&R, Clock Tree Synthesis and Routing.
- Worked on floorplan for high utilization ratio and designed good power Mesh to attain required IR drop.
- Worked on Automatic place and route to meet DRC's and Congestion with good routability.
- Worked on Classic and CCD synthesis flow on CTS and analyzing them for better timing reports.
- Understood routing flow and fixed DRC and LVS and Antenna violations.
- Knowledge and hands on experience on STA, CRPR, Interpreting Timing reports, Fixing Setup and Hold violations.
- Generated and analyzed timing reports for Pre-layout and Post-layout STA on Primetime and IC compiler 2 and resolved timing violations.
- Worked and modified TCL scripts and have written TCL scripts to extract information for timing paths, WNS and TNS.
- Hands on experience in APR tools Synopsys ICC2 and STA tools - Prime time
- Good knowledge in logic design concepts, CMOS, MOSFET and semiconductor theory.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2021**

Basaveshwar Engineering College, Bagalkot, with 6.1 CGPA

2015

Shree Guru Independent Pu College of Science, Gulbarga, with 63.16 %

SSLC **2013**

St Anne's Convent High School, Bagalkot, with 78 %

Domain Specific Project

RV-VLSI Design Center

Graduate Trainee Engineer Apr-2022 to Oct-2022

Designing of ASIC Flow Block Level Implementation

Description

Floorplan, Powerplan and Placement for Block Level. specifications are : Design- 40nm, Layers- 7, Supply Voltage- 1.1V, Area- 4.2 sq. mm, Clock frequency- 833MHz, Power Consumption- 600mW, Max IR Drop- 5%, Standard cell count- 38403, Macros - 34.

Tools

Synopsys IC Complier 2

Challenges

- Understanding specifications and designing Floorplan as per data flow diagram and making sure Flylines have adjoining area for Standard-cells.
- Setting up an efficient Powerplan to meet the IR-drop and eliminate DRC errors, Missing Vias and Floating pins.
- Understanding and Analyzing issues on Spare-cells, Tie-cells, Tap-cells and High Fanout errors during Place-opt and resolving them.
- Setting up NDR rules and Clearing all the Congestion by follow up Iterations.

RV-VLSI Design Center

Graduate Trainee Engineer Apr-2022 to Oct-2022

Analysis of STA

Description

Performing STA on various timing paths for flipflop and latches further generating timing reports. The reports are analyzed by factors such as OCV, AOCV, CRPR, Clock skew following the Constraint file.

Tools

Synopsys PrimeTime, Synopsys IC Compiler 2

Challenges

- Generating timing reports for all stages in APR flow further analyzing Setup and Hold violations.
- Understanding and analyzing Latency, Clock skew, OCV, CRPR in timing reports to eliminate Setup and Hold violations.
- Analyzing timing exceptions such as False path and Multi cycle path and reporting for changes in Constraint file

RV-VLSI Design Center

Graduate Trainee Engineer Apr-2022 to Oct-2022

CTS & Routing in Block Level Implementation

Description

During CTS and Routing stage, Buffers and Inverters are added to bring down the Skew and Latency hence meet the DRC regulations.

Tools

Synopsys IC Compiler 2

Challenges

- Understood and analyzed clock signal routing by Classic and CCD flow. thus comparing both timing reports.
- After CTS Optimization we manually fixed short errors, Net errors and multiple Via errors.
- Antenna violations was fixed by adding Jumper wires or Diode.

B.E / B.Tech Academic Project

Basaveshwar Engineering College, Bagalkot

UV-C Germs Disinfecting Machine

Description

An Automatic and Contactless Sanitizing machine. Capable of 360 degree disinfection. Entire process in monitored on LCD.

Tools

Hardware - Arduino UNO, Arduino WIFI 1010, UV-C lamp, Stepper motor, Servo motor, ultrasonic sensor, IR sensor, Enclosed Metal Chamber, LCD. Software - C++ (Arduino script).

Challenges

- Creating a harm free contained chamber for UV-C. Automatic time set for disinfection and emergency stop. Updating entire process on the LCD.