Name : BHANUSREE ANNAPAREDDY
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Phone no : 9491025879
www.se-minds.com

OBJECTIVE

Seeking a responsible position as an entry level Physical Design Engineer which enables to bring the best out of my knowledge and experience in achieving organizational goals and personal growth.

PROFESSIONAL TRAINING

An Industry Oriented Trainee in **VLSI ASIC PHYSICAL DESIGN** in **Se-minds Pvt, Ltd.**, Hyderabad from March 2022 to October 2022.

Course outline:

Digital fundamental concepts, MOSFET,CMOS design concepts, Basic of STA, Logic Synthesis fundamentals. Physical Design concepts: floor planning, PG planning, Low Power design techniques, CTS, Routing techniques, signal integrity. Experience on Static Timing Analysis and Good knowledge on Advanced STA, TCL Scripting, vi editors, Linux, dbGet commands.

Tools:

Experience in physical design of 90nmand 45nm technologies using Cadence tool

- ✓ Cadence Innovus : Floor Planning, Place & Route and clock tree synthesis
- ✓ Cadence Genus : Logic Synthesis

PROJECTS:

Project -1: Place and Route (Full Chip level – asic_entity)

Tools Used	: Cadence Innovus
Instance Count	: 31467
Macros	: 29
No.of Clocks	: 8
Frequency	: 125 MHz
Technology/Layers	: 90nm/9

Description: Perform Sanity Checks, performing normal PNR flow and done with foundation flow by reducing the block size with 100umm, Design import, Floor Planning, Power Planning, Placement, Trail Route, Congestion Analysis, Timing Analysis, Clock Tree Synthesis, Detail Routing, Timing Fixing.

Project -2: Place and Route (Block level - leon)

Tools Used	: Cadence Innovus - stylus
Instance Count	: 35601
Macros	: 4
No.of Clocks	: 5
Frequency	: 250 MHz
Technology/Layers	: 45nm/9

Description: Cleared DRC issues like parallel length spacing and timing is analyzed.

Project -3: Place and Route (Block level – eVITERBI_322)

Objective	: To Meet Setup Hold time, Fixing DRC's, DRV's
Tools Used	: Cadence Innovus
Macros/ Instance Count	: 0/100
No.of Clocks	: 1
Frequency	: 250 MHz
Technology/Layers	: 45nm/7

Description: Able to understand and generate Viewdefinition file. Cleared DRV and DRC , Connectivity issues. Generated a Flow scripts and automated the flow with "make" command by giving Plugin's at each stage.

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Project -4: Place and Route (Block level – usb_wrapper)

Objective	: Timing Driven Layout
Tools Used	: Cadence Innovus
Macros/Instance Count	: 12/28831
No.of Clocks	: 17
Frequency	: 208MHz
Technology/Layers	: 90nm/ 5

Description: Perform Sanity Checks, performing normal PNR flow. Automated the flow with "make" command.

Project -5 : Logic Synthesis (dtmf_receiver)

Objective	:Write SDC and TCL file and obtained Gate level netlist.
Tools Used	: Cadence Genus
Gate count	: 4131
Gate Area	: 231638.567um^2
No.of Clocks	: 7
Frequency	: 125MHz
Technology/Layers	: 45nm/ 11

Description: Check SDC & error correction, Generating reports for Area, Timing and Power, Different effort for optimization (generic, mapping, optimization) , Timing Analysis and Fixing.

ACADEMIC EDUCATION:

- Bachelor of Technology in Electronics and Communication from Rajiv Gandhi University of Knowledge and Technologies, Nuzvid in 2016-2020 with 8.41 CGPA
- Pre-University course from Rajiv Gandhi University of Knowledge and Technologies, Nuzvid in 2014-2016 with 9.8 CGPA
- Secondary School of education from Government High School in 2014 with 9.8 CGPA

PERSONAL STRENGTHS:

- ✓ Communication skills, Team-working, Volunteering, easily adopt to any technology.
- ✓ I have good logical knowledge towards problem solving.

DECLARATION:

I hereby declare that the above-mentioned information is correct to the best of my Knowledge.

(BHANUSREE ANNAPAREDDY)