Name : SAYANA KEERTHANA
E-mail : sayanakeerthi148@gmail.com
Mobile : +91 9391737771

Executive Summary

- Got certified as RTL Design and Verification Engineer from SUMEDHA IT.
- Possess the analytical skills necessary for engineering innovative approaches in VLSI field.
- Solid understanding of VLSI design and Verification environment.
- Good working understanding of SV and UVM.

Skills Summary:

HDLs	: Verilog
HVL	: System Verilog
Verification Methodology	: Constraint Random Coverage Driven Verification (CRCDV).
TB Methodologies	: UVM Programming
Tool	: Synopsis
Protocols	: AMBA - APB.

Certification Course

Certification Course: ASIC design and verification.
Institute : SUMEDHA IT, Hyderabad India.
Course Work : RTL Design and verification, Functional Coverage, Constraints, Randomization, Assertions , SV Environment, UVM testbench.

Project Details (During Training)

VLSI Projects:

Project 1:

Project Title : DPRAM.
Language : Verilog, System Verilog, UVM

- **Description**: Dual Port Random Access Memory (DPRAM) is a type of memory in which we can read and write simultaneously. We can send the addresses where we want to make write or read. In this project it consists of read enable and write enable input ports. If write enable is high we can write into the memory and if read enable is high we can read from the memory at specific address.
- Performed verification on DPRAM which supports both read and write operations at the same time

Project 2:

Project Title : FIFO.
Language : Verilog, System Verilog, UVM

- **Description:** FIFO is used to synchronize any two modules which have different bandwidth. If sender is sending data faster than the receiver then temporarily FIFO takes the data from the sender and stores it. Then receiver slowly takes the data from the FIFO.
- Designed a module which reads the data that is written first into it.

Project 3:

Project Title : AMBA-APB
Language : Verilog.

- **Description** : The AMBA APB protocol is targeted at low-performance, low-frequency system designs and includes a number of features that make it suitable for a low-speed submicron interconnect .

PROJECT : MAJOR
SMART ARMY JACKET

- **Description**: In this project explained about track the location of the soldiers with the help of GPS, and health parameters such as pulse rate and body temperature and also provided communication between the soldiers through the radio frequency channel. And using push buttons for emergency purposes, it will send an SMS alert to the officials who are in the military base station.
- Language: C Programming.

EDUCATION DETAILS:

COURSE	SPECIALIZATION	INSTITUTION	BOARD/ UNIVERSITY	SCORE	YEAR
UG	Electronics and Communication Engineering [E.C.E]	D.M.S.S.V.H College of Engineering	Jawaharlal Nehru Technological University Kakinada	7.56 CGPA	2022
XII	M.P.C	R.K Junior College	Andhra Pradesh State Board of Intermediate Education	94.8%	2018
X	SSC	Narayana E-Techno school	Andhra Pradesh State Board of Secondary Education	9.7 CGPA	2016

Interests

- Singing
- Badminton
- Carroms.

Extra Curricular Activities & Achievements & Internship

- Internship at Bharat Electronics Limited and Received Certificate
- Participate in online course of basics Geo-computation and Geo-web services conducted by Indian space research organization and received certification.
- Member in NSS (National Service Scheme).
- Coordinator in College Fest.
- Participated in Rangoli Competition.

Personal Details :

Father’s Name : Sayana Suresh

Date of Birth : 14 AUGUST 2000.

Languages : English, Telugu

Nationality : Indian

Address : Kokanarayanapalem , krishna district, Andhra Pradesh