PRAVEEN KUMAR MEDA

Physical design Engineer

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Nagayalanka, Krishna (Dist)

pin no: 521120

ABOUT ME:

To Build my career by acquiring a suitable position in a well established company and to work hard with high degree of commitment and sincerity in challenging and creative environment where my capabilities and technical skill are best utilized.

EDUCATION

B-Tech, Electrical and Electronics engineering
S.R.K.R Engineering college,Bhimavaram
CGPA: 6.88
2016-2019

Diploma, Electrical and Electronics engineering
Diviseema polytechnic college,Avanigadda
Percentage: 83.3%
2013-2016

S.S.C
Z.P.H. School, Nagayalanka
C.G.P.A: 8.5
2012-2013

PROFESSIONAL TRAINING

Maven Silicon VLSI Design and Training Canter, Bengaluru
Advanced Physical Design and Verification Course
May 2022 – Present
Currently, I am undergoing training at Maven Silicon to get hands on experience and develop the skill sets needed to get into VLSI Domain.

TECHNICAL SKILLS

CMOS Fundamentals: Working of Mosfet, Mos IV characteristics, second order effects Fabrication steps, Alternatives to CMOS, Layout and Stick diagrams.
Domain: Physical Design flow including floor planning, Placement & Routing, Clock Tree synthesis, Timing Analysis and Signoff using Oasys, Aprisa and Calibre from Siemens EDA.
EDA Tools: Tanner, Oasys, Aprisa
- Schematic creation, simulation, Analysis, Layout generation of digital circuits are performed on Tanner tool.
- Synthesis using Oasys tool.
- Floor planning, Placement, Clock Tree Synthesis, Routing and optimization using APRISA.

SKILLS

- Digital Design

- Physical Design

- EDA Tools

- Verilog

INTERPERSONAL SKILL

- Time management
- Problem solving
- Creativity
- Team work
- Decision-making
- Adaptability

HOBBIES

- Listening to music
- Drawing
- Painting
- Digital Arts

VLSI DOMAIN SKILLS

HDL: Verilog
EDA Tools: Modelsim, Quartus prime
Scripting Languages: TCL
Operating System: Working knowledge on Windows and Linux
Core Skills: RTL Coding, Simulation, CMOS Fundamentals, Static Timing Analysis, Logic Synthesis, floor planning, Placement, Routing, STA, Signoff (ERC, DRC, LVS)

VLSI DESIGN

Digital Electronics: Combinational & Sequential circuits, FSM, Memories, CMOS implementation, stick diagram
STA: STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks Clock domain and Validations, Clock Distribution Networks, Fixing timing failure

Verilog Programming: Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & folk join blocks, looping & branching constructs, System tasks & Functions, Synthesis issues, pipelining RTL & TB Coding

VLSI PROJECT 1

ROUTER 1X3 – RTL DESIGN AND VERIFICATION
HDL:

EDA Tools: Modelsim, Quartus prime, Tanner,Oasys, Aprisa
Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel
Responsibilities:
* Architected the design. Implemented RTL using Verilog HDL.
* Synthesized the design and generate the Gate Level netlist.
* Implementing floor planning, Placement and Routing processes on the netlist. Implementing Clock tree Synthesis.
* Performing Timing Analysis and achieve timing closure. Perform DRC, ERC and LVS for signoff.
* Exporting the final GDS-II

VLSI PROJECT 2

RISC-V Architecture
EDA Tools: Aprisa,
Description: Implemented RISC-V architecture from gate level netlist to GDSII file and verified using the Calibre tool

ACODEMIC PROJECT

* Power Generation from Locomotives Generating DC power from Alternative motors for locomotive to save power consumption project
* Automated Self-Cleaning Solar Panels Developed an automated self-cleaning system to improve the durability and performance of solar panels project

DECLARATION

I hereby declared that the above mentioned particulars are true and correct to the best of my knowledge and belief.

Date :

Place : M.Praveen Kumar