## NIKHIL KUMAR KASHA

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## Career Objective

To be a successful Physical Design engineer in an esteemed organization, where ample opportunity exists to reach professional and personal goals while working for the development of the organization to its highest potential.

## Core Competancy

- I know the basics of Perl ,TCL,Verilog languages and also have the knowledge of basic Linux commands.
- I have a complete understanding of STA and Logic Design.
- I can ensure an appropriate IR drop while varying the width, space, pitch and offset of metal during power plan which requires careful analysis and correction.
- I can correct DRC and LVS violations to reach the targeted IR Drop.
- I'am able to manually place macros during the floor planning without violating DRC's.
- I can reduce routing congestion during placement by fixing the floor plan. By ensuring there is enough space between macros, it will help to reduce traffic.
- I have an experience in analyzing timing paths and timing violations during CTS.

## Education Details

**Advanced Diploma in ASIC Design** **2023**

RV-VLSI Design Center

**Bachelor Degree** in **Electronics and Communication** **2022**

KG REDDY OF ENGINEERING & TECHNOLOGY, with 6.23 CGPA

**2018**

SRI CHAITANYA JUNIOR COLLEGE, with 86 %

**SSLC** **2016**

MARVEL HIGH SCHOOL, with 90 %

## Domain Specific Project

**RV Skills for Emerging Technologies, Bangalore, Karnataka, India.**

*Graduate Trainee Engineer* Sep-2022 to Jan-2023

**LAKSHYA**

**Description**

As an ASIC design engineer, I got an extensive experience in resolving DRC and LVS violations, reducing the congestion, in obtaining the targeted IR drop while Placement, Routing and CTS stages in order to design a good layout.

**Tools**

Synopsys ICC2

**Challenges**

- To reduce the congestion during and routing stages attempting number of iterations was the time taking process but works well with patience to achieve a good layout.
- Varying the width, space, pitch and offset values of the routing metals to achieve the targeted IR drop with no DRC violations during routing and placement stages .
- Rectifying timing violations during CTS stage which needs a deep understanding about timing paths.

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## B.E / B.Tech Academic Project

KG REDDY OF ENGINEERING & TECHNOLOGY

**POWER MONITORNIG AND ENERGY CONSERVATION IIOT SYSTEM**

**Description**

The aim of the project is to design a system for optimum energy usage by introducing motion-based sensors. IR sensors are used to sense an activity inside a room / a place where it is placed, which can turn ON/OFF.

**Tools**

Arduino Uno R3 , Node MCU , ESP8266 , ESP32 , Motion Sensor , IR sensor , Current transformer , Single / Multi Channel Relay Boards , Miscellaneous components : Bread board , Resistors , Capacitors .

**Challenges**

- With the help of blink IOT application, we combine both power monitoring and controlliing modules using Arduino and ESP 32. The data will be sent through Wi-Fi network and then control them through a mobile device.