SMEETA NAGANNAVAR

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1998-04-12 India

PROFILE

Mtech graduate. Looking forward to work in an organisation which provides me an opportunity as Design Verification Engineer to explore my technical skills towards organizational goals and be an ultimate resource to the organisation. It also helps to develop my personal skills with experience in the organisation.

EDUCATION

Mtech

MS Ramaiah university of applied science banglore

2020 – 2022 | banglore, india

Specialization-vlsi and nanotechnology

CGPA-7

Btech

REVA university banglore

2017 – 2020 | banglore, india

EEE

CGPA-7.1

Diploma

C B Kore polytechnic chikodi

2014 | chikodi, india

EEE

Percentage-68%

school

saraswati school ghataprabha

2014 | ghataprabha, india

percentage-87.84%

LANGUAGES

- Kannada
- English
- Hindi
- Marathi
- Telugu

PROJECTS

Efficient FIR Filter Design using BOOTH multiplier for vlsi application

Design and development of gain compensator module using FPGA radar application

SKILLS

CORE SKILLS

- RTL Coding using Synthesizable Constructs of Verilog
- FSM based Design
- Synthesis
- Simulation
- CMOS fundamental
- Code coverage
- Functional coverage
- Static Timing Analysis

DESIGN SKILLS

DIGITAL ELECTRONICS:

Combinational & Sequential circuits | FSM | Memories | CMOS implementation | stick diagram

STA:

STA basics | comparison with DTA | Timing Path and Constraints | Different types of clocks | Clock domain and Variations | Clock Distribution Networks| Fixing Timing failure

VERILOG PROGRAMMING:

Data types| Operators| Processes| Delays in Verilog| BA & NBA | begin - end & fork join block | looping & branching construct | System tasks & functions | Compiler directives | FSM coding | Synthesis issues | Races in simulation | pipelining RTL & TB Coding

ADVANCED VERILOG:

Generate block | Continuous Procedural Assignments | Self checking testbench | Automatic tasks | Named events and Stratified event Queue

VERIFICATION SKILLS

SYSTEM VERILOG HVL:

Dynamic and Multi-Dimensional arrays | Interface & Clocking block | inheritance & Polymorphism | Constraint Randomization - Inline distribution conditional soft & static constraint | Mailbox and Semaphores | Functional coverage | CRCDV and Regression testing

SYSTEM VERILOG ASSERATATION:

Types of assertation | assertation building blocks | sequence with edge definitions and logical relationships | clock definitions | implication and repetition operators

BASIC ADVANCED AND OBJECT ORIENTED PRIGRAMMING:

Handle assignments | copying object content | Inheritance | Polymorphism | static properties and methods | Virtual classes and parameterized classes

CONSTRAINT RANDOMIZATION:

Constraint overriding & Inheritance | Distribution and conditional constraints

THREADS SYNCRONIZATION TECHNIQUES:

Events | Semaphore | Maibox-buit-in methods

DECLARATION

I here by declare that all the information above is true to the best of my knowledge

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Belagavi