Rahul Bellad

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Belagavi-590006, Karnataka

Career Objective

To be a part of a dynamic workspace where I can utilize my knowledge and skills to work on emerging technologies with scope of learning and growth of the organization as well as self.

Core Competancy

- Hands on Experience in industry tools like Synopsys PrimeTime and Synopsys IC Compiler 2
- Analyzed and understood design constraints to specify PVT corners, False paths, Half cycle, Multicycle, CRPR, Signal Integrity.
- Knowledge and hands on experience in interpreting timing reports and fixing setup and hold violations.
- Through understanding of APR Flow in Block Level Implementation of ASIC from GLN to GDSII
- Worked on Floorplans for high utilization ratio, designed power mesh to meet IR drop and checked for pg connectivity errors.
- Worked on Automatic Place and Route to meet DRCs and congestion ensuring good routability.
- Worked and understood the Classic and CCD synthesis flow of CTS.
- Worked on routing flow and fixed the DRCs and LVS issues.
- Understood and modified TCL scripts for PD flow.
- Knowledge on Semiconductor theory, Logic Design and MOS structure.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2021**

KLE Dr M S Sheshgiri College of Engineering and Technology, with 8.42 CGPA

2017

MGVM PU College of Science and Commerce, Belagavi, with 76 %

SSLC **2015**

Amrita Vidyalayam School, Belagavi, with 8.8 %

Projects worked on

Accenture Solutions Pvt Ltd Client: British Telecom

Application Development Associate Oct-2021 to Jul-2022

Manual Testing of UI

Description

The job role was to find defects in the updated design of the UI that would be used by the client and update it to the development team for rectification.

Tools

JIRA, Micro Focus ALM

Challenges

- Compare previous versions of UI to the current UI and check for defects.
- Perform regression and end to end testing on the updated UI version to find defects and report to development team.
- Ensure all defects are identified before end of sprint

Domain Specific Project

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Sep-2022 to Jan-2023

Static Timing Analysis

Description

Timing analysis for flipflops and latches for various paths groups. Timing reports are analyzed considering various conditions such as OCV, Uncertainty, CRPR, Clock Skews and exceptions (Multi- cycle, False paths).

Tools

Synopsys PrimeTime, Synopsys IC Compiler 2

Challenges

- Constrained the given specifications in PT Shell to different path groups.
- Generated and analyzed the timing reports at different stages of APR flow for different path groups.
- Triaged the cause for violations based on timing exceptions such as false path and multicycle paths.
- Understood the effect of Clock Skew, CRPR, OCV and Crosstalk from the timing reports.

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Sep-2022 to Jan-2023

APR Flow of Block Level Implementation of ASIC

Description

Floorplan, Powerplan and Placement for Block Level with the following specs- Design- 40nm, Layers- 7, Supply Voltage- 1.1V, Area- 4.2 sq. mm, Clock frequency- 833MHz, Power Consumption- 600mW, Max IR Drop- 5%, Standard cell count- 38421, Macros- 34

Tools

Synopsys IC Compiler 2

Challenges

- Understanding the design specification and designing of Floorplan accordingly such that to have a contagious core area for standard cell placement.
- Building a Powerplan to meet the IR drop and ensuring that there are no floating wires, missing vias and DRC violations.
- Placement and Optimization of spare cells, tie cells, tap cells, boundary cells and standard cells to meet the DRC violations and Congestion check.
- Analyze the reports after each stage and try and rectify the errors.

RV-VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Dec-2022 to Jan-2023

APR Flow of Block Level Implementation of ASIC

Description

CTS and Routing for Block Level with the following specs- Design- 40nm, Layers- 7, Supply Voltage- 1.1V, Area- 4.2 sq. mm, Clock frequency- 833MHz, Power Consumption- 600mW, Max IR Drop- 5%, Standard cell count- 38421, Macros- 34

Tools

Synopsys IC Compiler 2

Challenges

- Clock routes are routed using NDR and CTS is built using H-Tree Algorithm. Synthesis is performed using Classic and CCD flow and compared for better timing reports.
- Reduce Clock Skew and Latency. Identified and rectified errors caused because of clock routing. Checked for clock exceptions and reported both setup and hold violations.
- Signal routing was done keeping DRCs and DRVs in mind. It was made sure that the interconnect wire length was minimal and congestion was in control.
- Fixing of Antenna violations was done using insertion of either jumper wires or diode. QOR reports were generated and proceed to signoff.

B.E / B.Tech Academic Project

KLE Dr M S Sheshgiri College of Engineering and Technology

Development of a 3D Printer

Description

The project was built using a 32-bit Controller and Stepper motors. The 3D printer enabled the user to convert his/her 3D Design to a .STL file and upload it to the 3D Printer which would convert the file to a geometric code(G-Code) and perform additive manufacturing process.

Tools

Hardware: SKR 1.4 Control Board, Nema-17 Stepper motors, Lead Screws and Belts, LCD Display, Filament for printing Firmware: Marlin

Challenges

- Create a printer that would be able to compete with other 3D printers in the market in terms of Print Speed and Print Quality. Creating a smaller footprint than an industrial 3D printer to make the printer a desk friendly device