PATEL AYUSH ASHOKBHAI

M.Tech – VLSI Design
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CAREER OBJECTIVE

- To succeed in an environment of growth and excellence and build an innovative career which provides self-development and help me to achieve the company goals.

EDUCATION

Degree	Institute/ Board	CGPA/ Percentage	Year
M.Tech in VLSI Design	Institute of Technology, Nirma University	9.20 (1st sem)	
		8.45 (2nd Sem)	2022
B. E. in Electronics and Communication Engineering	Vishwakarma Government Engineering College, Gujarat Technological University	9.08	2020
HSC	GSHSEB Board	79.33%	2016
SSC	GSHSEB Board	89.50%	2014

INTERNSHIP

Intel Technology Pvt. Ltd. **06 Jul, 2022 -12 May, 2023**

Design Verification Engineer

PROJECT : Low Power Checks and Power Estimation at RTL level using prime power .

- Main aim is to measure power using prime power tool .
- Setting up a prime power tool.
- We are providing six input files to the tool like UPF, gate – level netlist, constraints , SPEF , mapping , FSDB.
- UPF : Migrating UPF 2.0 to UPF 2.1 and perform low power checks and provide to prime power as an input.
- FUSION COMPILER : For other inputs like gate – level netlist, constraints , SPEF , mapping we are running FC.
- At last we have power numbers for actual test cases, and achieved annotation rate > 99.5% , and not facing any warnings.

PROJECTS

Implementation of 4x4 Sram Memory Array Using 180nm Technology Node.

- These Project includes the understanding of fundamentals of SRAM memory design aspects and layout design of 4x4 SRAM memory at 180nm technology using Cadence Virtuoso.

Design and Implementation of 2-Stage Op-Amp at 180nm Technology Node Using Cadence Virtuoso.

- This Project include Design and development of Two stage Op-Amp Schematic, (W/L) ratio's of all transistors, Gain analysis, Gain Bandwidth Product, Power Dissipation, Slew Rate, CMRR, Close Loop Gain, Integrator and Differentiatoras an application ,Layout (DRC,LVS,RCX) Layout using Cadence Virtuoso for given parameters.
- Secifications : Gain=60db, GBW= 30Mhz, Power=0.3mW, ICMR(+)=1.6V, ICMR(-)= 0.8V, Slew rate=20V/us, Cl=2pF .

Design and Simulate Different Types of Multipliers Using Verilog.

- Verilog Coding of Booth's multiplier, Modified Booth's multiplier, Brawn multiplier, Wallace Tree multiplier and test bench coding , Functional Verification and Synthesis.
- Comparision of all Multipliers in term of Area, Power, Speed.

Layout Design of a Boolean Equation Using Cadence Virtuoso.

- These project includes the optimization of a Boolean equation, Gate level representation, CMOS transistor level schematic, functional verification, stick diagram, Optimized layout design, Check DRC and LVS , RC Extraction, Post layout simulation in Cadence Virtuoso.

PERFORMANCE ANALYSIS OF HIGH SPEED VLSI ADDERS .

- Implementation of different types of 4-bit adder such as Ripple Carry Adder, Carry Look Ahead Adder, Carry Select Adder, Carry Save Adder, Kogge-Stone Adder using Verilog .

TECHNICAL PROFICIENCY

- **Programming Languages :** System Verilog , Verilog-HDL, Basics of Python,
- **Tools :** Prime Power , Prime Time , Fusion Compiler, Cadence Virtuoso , Cadence Encounter.

ACHIEVEMENTS

- GATE 2020 : AIR : 8984
- GATE 2021 : AIR : 6632
- UNIFIED CYBER OYMPIAD – 2012 : AIR : 7193.
- SHITO-RYU KARATE : Won Bronze Medal at National Level Champion Ship (4th kyu senior. Green Belt).

PERSONAL DETAILS

- **FULL NAME** : Patel Ayush Ashokbhai
- **GENDER** : Male.
- **NATIONALITY** : Indian.
- **MARITAL STATUS** : Unmarried.
- **LANGUAGE KNOWN** : English, Gujarati, Hindi.
- **LinkedIN ID** : http://linkedin.com/in/ayush-patel-749926221
- **HOBBIES** : Gymming, Cricket, Travelling, Reading.