MEGHANA S HARANAHALLI

RTL DESIGN AND VERIFICATION

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CAREER OBJECTIVE

Intend to build a career with committed and dedicated people, which will help me to realize mypotential, enhance my skill set in the field of VLSI and help the organization grow.

PROFILE SUMMARY

- Good understanding of the ASIC design flow.
- Attended training on "SOC Verification" and aware of its flow.
- Good knowledge in writing RTL models in Verilog HDL and Testbenches in SystemVerilog and UVM
- Good knowledge in verification methodologies.
- Good understanding in using industry standard EDA, Questasim and Modelsim, Verdi, VNC tools for the front-end design and verification.

PROFESSIONAL TRAINING

Advanced VLSI Design and Verification Course

Maven Silicon VLSI Design and Training Center, Bangalore — Jun 2021 – Jan2022

ACADEMIC CREDITIALS

Bachelor's of Engineering in Electronics and Communication
S T J Institute Of Technology Ranebennur, Karnataka
CGPA – 6.5 — 2017 - 2020

Diploma in Electronics and Communication
Government Polytechnic Bankapur, Karnataka
Percentage - 65% — 2013 - 2017

Central Board of Secondary Education
Om National PublicSchool, Ranebennur, Karnataka
CGPA – 6.8 — 2012 - 2013

TECHNICAL SKILLS

HDL: Verilog, SystemVerilog
Methodolgy: UVM
Scripting : Basic Perl
Operating System: Linux,Window
Tools : Questasim and Modelsim, Verdi, VNC
Protocols: AMBA APB, AHB-Lite, I2C

WORK EXPERIENCE

Junior Engineer(Intern) February 2022- October 2022

InSemi Technology Service Pvt. Ltd. Bangalore, Karnataka.

PROJECT DETAILS

Project1:KL15_TXFIFO

Tools & Language used: Verdi, VNC, Methodology UVM

Role and Responsibilities:

- Implemented UVM test-bench environment and components.
- Architected the class based verification environment using
- system Verilog Generated testcase and assertion for signal.
- Generated functional coverage for the verification.

Project Description:

The PHY enables symmetrical operation at for the downstream and upstream links. KL_8TO8_PLB_BYPS, an 8-bit simple FIFO with bypass path. This is based on the UVM methodology. The reset pin, when set high the circuit starts working,the bypass pin is set to a high state then input data directly read by the output data.

Project2: ROUTER 1X3 – RTL DESIGN AND VERIFICATION

HDL: Verilog

EDA Tools: Questasim and ISE

Description:

The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

DECLARATION

I hereby declare that all the above mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above mentioned particulars.

Place: Ranebennur Meghana S Haranahalli