PRAGYA SINGH
Course : M.TECH, VLSI, 2024
Email : pragyasinghanku@gmail.com
Mobile : 9752688338
CGPA : 8.3

ACADEMIC DETAILS					
COUSRE	SPECIALIZATION	INSTITUTE / COLLAGE	BOARD / UNIVERSITY	SCORE	YEAR
UG	ELECTRICAL	Shri Shankaracharya Group of Institutions	CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY	7.79	2021
PG	VLSI Design	VIT Bhopal University	Vellore Institute of Technology	8.3	2024
CLASS XII	SCIENCE	DAV,Public School Hudco	Central Board of Secondary Education	61.6%	2017
CLASS X		DAV Public School,Hudco, Bhilai.	Central Board of Secondary Education	8.4 CGPA	2015

Subject Knowledge	Digital Logic Design, Digital IC Design, CAD for VLSI, ASIC Design, Low Power IC, IC Technology,FPGA,STA,Physical design.
Skills	Verilog HDL, C Programming, Physical design(basic), STA, Perl
Tool and Technology	ModelSim, Quartus Prime, TCAD Synopsis, LTspice

Academic Projects

- **Designing of Digital Alarm Clock**

Tool used : Xilinx- VIVADO(FEB 23)

1) We are generating a clock with 7 output signals including Alarm signal, Hour, Minute, and seconds
2) The clock generated is in a 24 - hour format. We can give an initial time value to the system when reset signal=1 or by turning the signal LD_time=1

- **:Design & layout of 2 stage Operational Transconducatnce Amplifier**

Tool used : LTSPICE (DEC2022 – JAN2023)

1) Implemented the design of a 2-stage fully differential input & single-ended output.
2) Achieved tight specification on DC gain, phase&Gain margin.
3) Implemented its layout in Ltspice with scl 180nm technology.

INTENSHIP- MAVEN SILICON (JAN 203- FEB2023)
DESIGING AND VERIFICATION

- Application of digital electronics in chip designing
- Learnt how to design AHP to APB Bridge
- Learnt how to develop RTL synthesis, check the elaborated design and simulation to see the working of alarm clock specification and AHP TO APB Bridge protocol
- Tools – Xilinx- VIVADO

Languages known
ENGLISH, HINDI