ABHISHEK PANDEY

+91-8250821825 | mailbox.pandey.hitk@gmail.com |

EDUCATION

Indian Institute of Engineering Science & Technology(IIEST) Howrah , West Bengal

Master of Technology in VLSI Design (2021-2023) Agg.CGPA –8.64

Heritage Institute of Technology kOLKATA , West Bengal

Bachelor of Technology in Electronics & Communication (2015-2019) Agg.DGPA – 7.44

STD COLLEGE GHURAPALI Ghurapali ,Bihar

12th Grade (2014) *67%*

Jay Kay Nagar High School J K NAGAR,West Bengal

10th Grade (2012) *72.4 %*

SKILLS

HDL Language : Verilog HDL , System Verilog

PROTOCOL: UART,SPI,I2C,APB

Electronics: Digital Electronic , Static timing analysis

Methodology: UVM

Languages: English | Hindi

ACHIEVEMENTS

GATE 2022 | EC AIR - 2947

GATE 2021 | EC AIR - 6155

TRAINING

I have completed my six month training on Design verification profile from VLSI FOR ALL training institute.

PROJECT

DESIGN OF UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER USING VERILOG

* UART PROJECT consisting three main section the transmitter, the baud rate generator and Finally the receiver.

DESIGN OF SYNCHRONOUS FIFO USING VERILOG

* fifo is a design component used for interfacing data transfer between two component either Working on same frequency or different.

Declaration

I hereby declare that above furnished information and particular are true and correct to the best of my knowledge and belief.

DATE:13/02/23 ABHISHEK PANDEY