Girish K G

kg.girish91@gmail.com, 8722842040

Davangere-577001, Karnataka

Career Objective

I am a forward-thinking, passionate engineer motivated by the challenges to work on the optimized nm technology by fully utilizing my training, knowledge and right skills, thereby contributing my best to the company's growth.

Core Competancy

- Acquired knowledge and understood the Logic Design, basic Electronics, MOSFET and fundamentals of CMOS.
- Acquired knowledge about ASIC design and PD flow including Floor Plan, Power Plan, IR Drop Analysis, Automatic Place and Route, Clock Tree Synthesis and Routing.
- Good hands on experience of TCL, PT-Shell, ICC2 and familiar with the Linux Environment.
- Analyzed and understood design constraints to specify PVT corners, False paths, Half cycle, Multicycle, CRPR and Signal Integrity.
- Worked on Floorplans for high utilization ratio, designed power mesh to meet IR drop and checked for PG connectivity errors.
- Worked on Placement plan to have acceptable congestion to have good routabilitiy.
- Analyzed the generated timing reports of Pre-Layout and Post-Layout STA and the timing violations.
- Worked on Classic and CCD synthesis flow of CTS and compared both for better timing reports.
- Understood and modified some of the TCL scripts to fix Antenna violations using the Diode insertion method.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2020**

Bapuji Institute of Engineering and Technology, Davangere, with 6.0 CGPA

2016

Bapuji Polytechnic, Shabanur, Davangere , with 80.72 %

SSLC **2013**

Jain Vidyalaya High School, Davangere, with 74.40 %

Projects worked on

SHREE RENUKAMBA PRASANNA ENTERPRISES Client: Reliance Jio Infocomm Limited

Associate Field Engineer Oct-2019 to Jan-2022

OFC Blowing and Installation of 6.8KM

Description

12 Fiber OFC cable blowing from Kithane to Konthagondana Halli with route length of 6.77 meters with OTR of 6.45 meters and HDD of 328 meters.

Tools

ELGI SS 01 LB Compressor with 10KG Pressure along with Caterpillar BCA 9 and Honda 7.5 HP Blowing Machine.

Challenges

- Depth achievement of 1.65 meter from normal ground level by OTM and HDD methods.
- Planning of Man Hole Chambers and Hand Hole Chambers at every 4KM and 980 meters respectively.
- Rectification of Punch Points given by O&M team.
- Insertion of Warning tapes from 1.2 meter from bottom level after OFC Blowing.

Domain Specific Project

RV-VLSI Design Center

Graduate Trainee Engineer Jul-2022 to Aug-2022

Block Level Floor Plan & Placement for a 40nm Chip

Description

Floorplan, Powerplan and Placement for Block Level with the characteristics- Design- 40nm, Layers- 7, Supply Voltage- 1.1V, Area- 4.2 sq. mm, Clock frequency- 833MHz, Power Consumption- 600mW, Max IR Drop- 5%, Standard cell count- 38403, Macros - 34.

Tools

Synopsys IC Compiler 2

Challenges

- Designed Floorplan by understanding design constraints and data flow diagram to achieve optimized timing and to have contiguous core area for standard cells.
- Designing a Power Mesh to meet the acceptable IR Drops and ensuring there are no floating pins, missing vias and no PG DRC errors.
- Placement and Optimization of spare cells, tie cells, tap cells, boundary cells and standard cells to meet the DRC violations and Congestion check.
- Analyzed the Timing report and reported the cause of error for the timing violations.

RV-VLSI Design Center

Graduate Trainee Engineer Aug-2022 to Sep-2022

Designed CTS and Routing for 40nm Chip.

Description

Building CTS for Block Level with the characteristics- Design- 40nm, Layers- 7, Supply Voltage- 1.1V, Area- 4.2 sq. mm, Clock frequency- 833MHz, Power Consumption- 600mW, Max IR Drop- 5%, Standard cell count- 38403, Macros - 34

Tools

Synopsys IC Compiler 2

Challenges

- Addition of Buffers and Inverters to minimize the Clock Skew and Latency.
- Resolving the Antenna issue by Jumper methodology and diode insertion methodology.
- Analyzing the Reports of Placement, CTS and Routing to understand the Cell Counts, Utilization, WNS and TNS.
- Identified and rectified Short error caused because of clock routing. Checked for clock exception and also met the Congestion.

RV-VLSI Design Center

Graduate Trainee Engineer Jul-2022 to Sep-2022

Analysis of Timing Reports (STA)

Description

Timings analysis for flipflops and latches for various paths groups. Timing reports are analyzed considering various conditions such as OCV, uncertainty, CRPR, Clock skews and exceptions (Multi- cycle, False paths) honoring the constraints.

Tools

Synopsys Prime Time, Synopsys IC Complier 2

Challenges

- Constrained the given specifications in PT shell to understand the behavior of different path groups.
- Generated and analyzed the timing reports at different stages of APR flow for different path groups.
- Identified the cause for violations based on timing exceptions such as false path and multicycle paths and reported the same to change in constraint file.
- Understood the effect Clock skew, CRPR, OCV and Crosstalk from the timing reports.

B.E / B.Tech Academic Project

Bapuji Institute of Engineering and Technology, Davangere

Bus Ticket Automation

Description

The project is mainly aimed towards automation of the ticketing in the bus transportation. The circuit was established on the prototype bus model which can scan for the RFID tags or Biometrics and allow the passenger to travel by automatic payments.

Tools

Software Used are ARDUINO IDE, IOT THINGSPEAK. Hardware Used are Arduino Mega 2560, Wi-Fi Module, GSM Module, RFID Reader, IR Sensor, Display, Servo Motors, Motor Driving Circuit, wires, jumpers and Power Supply.

Challenges

- Selecting the suitable hardware which are compatible to our microcontroller was tough. The Distribution of power to the hardware in the circuit was challenging. Coding and Interfacing the hardware to meet the desired timing goals was stimulating.