DHONGA LAHARI

DESIGN VERIFICATION ENGINEER

CONTACT

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PERSONAL DETAILS

- Father name:D.Thirupathi Reddy
- Mother name: D. Divya
- Date of Birth: 04/02/2001

LANGUAGE

- English
- Telugu

HOBBIES

- Playing Badminton
- Listening Music

CAREER OBJECTIVE

Very passionate and enthusiastic to work in my dream career in VLSI Domain. Seeking a challenging workspace to apply the acquired knowledge for the overall growth of the organization and self Motivated to learn, grow and excel in the company

PROFESSIONAL TRAINING

Advanced VLSI Design and Verification Course
Maven Silicon, Bangalore
Duration: August 2022 - Present

EDUCATION

- **B.Tech | Electronics and Communication | 2018-22**
  JNTUH University, Hyderabad
  CGPA: 7.5
- **Intermediate(M.P.C.)| 2016-18**
  Narayana Junior College, Hyderabad
  Percentage: 95.5%
- **SSC | 2015-16**
  St Peters Foundation High School, Jangaon
  CGPA: 9.3

PROJECTS

- **AXI-AMBA AXI4 Protocol Verification**
  HVL: System Verilog |**TB Methodology**:UVM | **EDA Tools:**Mobaxterm
  Description: The AMBA AXI protocol is targeted at high-performance,high-frequency system and includes a number of features that make it suitable for a high-speed submicron interconnects.
- **AHBTOAPB Bridge IP Core Verification**
  HVL: System Verilog | **TB Methodology:**UVM |**EDA Tools:**Mobaxterm
  Description: The AHB to APB bridge is an AHB slave which works as an interface between the high speed AHB and low performance APB buses.
- **Router 1x3-RTL Design and Verification**
  EDA Tools: Mobaxterm | **HDL:**Verilog
  HVL: System Verilog | **TB Methodology:**UVM
  Description: The router accepts 8-bit data packets on input port and routes data onto one of the three output channels.
- **Implementation of prepaid electricity bill using Verilog**
  EDA Tools: Xilinx | **Language:** Verilog
  Description: In this Prepaid electricity billing system, when the system is on, it starts counting a number of units & reduces the balance on completion of the amount, and checks whether the backup is present or not. if there is a backup it continues counting units otherwise disconnects the line until the system is recharged again.

DESIGN SKILLS

Digital Electronics:
Number system, logic gates, Combinational & Sequential circuits, Finite State Machine, Memories.

STA :
STA Basics, Comparison with Dynamic Timing Analysis, Timing Path and Constraints, Different types of clocks Clock domain and Variations.

Verilog Programming :
Data types, Operators, Blocking Assignments& Non Blocking Assignments, Delays in Verilog, begin - end & fork-join blocks, System tasks & Functions, compiler directives, FSM coding.

Advanced Verilog & Code Coverage :
Generate block, Continuous Procedural Assignments, Self-checking testbench, Automatic Tasks, Named Events and Stratified Event Queue, Code Coverage: Statement and branch coverage, Condition & Expression Coverage, Toggle & FSM Coverage

VERIFICATION SKILLS

System Verilog HVL
Memories - Dynamic array, Queue, Associative array, Task & Function - Pass by reference Interface - Modport and clocking block, Basic and advanced object-oriented programming - Handle assignments, Copying the object contents, Inheritance, polymorphism, static properties and methods, virtual classes, and parameterized classes, Constraint Randomization - constraint overriding and inheritance, Distribution and conditional constraints, Soft, static and inline constraints. Thread synchronization techniques - events, semaphores, and Mailbox - built-in methods. Functional coverage - Cover groups, bins and cross-coverage, CRCDV, and regression testing.

System Verilog Assertions
Types of assertions, assertion building blocks, sequences with edge definitions and logical relationship. Sequences with different timing relationships. Clock definitions,implication and repetition operators, inline and binding assertions, advanced SVA Features and assertion Coverage

UVM
UVM Objects & Components, UVM Factory & overriding methods, Stimulus Modelling, UVM Phases, UVM Configuration, TLM, UVM Sequence, virtual sequence & sequencer, Introduction to RAL.

TECHNICAL EXPERTISE

- **HDL: Verilog**
- **HVL: SystemVerilog**
- **TB Methodology: UVM**
- **Operating System: Windows, Linux**
- **EDA Tools: Modelsim, Mobaxterm, Quartus Prime, Xilinx ISE**
- **Scripting Language: Perl Scripting**

ACHIEVEMENTS

- Secured 2nd prize in Paper Presentation with title of “3D INTERNET”.
- Maven Silicon STAR OF THE MONTH (Sept 2022).
- Secured Distinction in Secondary School.

STRENGTHS

- Creativity and Curiosity to learn new things.
- Hardworking sincere and confidence

DECLARATION

I hereby declare that all the details mentioned above are true to the best of my knowledge and belief.

Date :
Place : Hyderabad

Lahari Reddy