Nandan C R

nandancr06@gmail.com, 9902872774

Bengaluru-560091, Karnataka

Career Objective

To excel in the field of physical design and to work in an innovative and competitive world.

Core Competancy

- Implemention of block level design in 40nm technology
- Chip floor-planning, dealing with placement, clock tree synthesis, and routing, with multi criteria optimization (power, area, timings)
- knowledge on logic synthesis, constraints and Static timing analysis
- Efficient in power planning, congestion and IR Drop Analysis
- hand on experience on IC Complier II and primetime from Synopsys
- Understanding and modifying TCL scripts
- Scripting language - Perl and Linux scripting

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

Rajarajeswari College of Engineering , with 6.7 CGPA

2017

Alva's PU College, with 79.68 %

SSLC **2015**

Maria Sadana Public School, with 74.72 %

Domain Specific Project

RV-Skills center for emerging technologies

Graduate Trainee Engineer Aug-2022 to Feb-2023

Design implementation of floorplan

Description

Implementing block-level design for lakshya project. Floorplanning deals with the placement of I/O pads and macros as well as power and ground structure.

Tools

Synopsys (IC Compiler II)

Challenges

- Placement of macros with pin/ports of core, them near to core boundary
- Figure out routing congestion and fixing the floorplan and power plan to solve the issue
- Resolve IR drop map and fixing the DRC violations

RV-Skills center for emerging technologies

Graduate Trainee Engineer Aug-2022 to Feb-2023

Block level placement and Routing

Description

placement will be driven by different criteria like timing-driven congestion-driven, power optimization, and creating a physical connection based on logical connectivity

Tools

Synopsys (IC Compiler II)

Challenges

- Finding the factors which will influence setup violation
- Analyzing timing reports
- Figure out routing congestion

RV-Skills center for emerging technologies

Graduate Trainee Engineer Aug-2022 to Feb-2023

Clock tree synthesis

Description

The clocks get distributed evenly to all sequential elements in the design and building a clock tree to get design rule violation checks, optimized skew, and database with a properly build clock tree in the design

Tools

Synopsys (IC Compiler II)

Challenges

- analyzing timing reports
- reducing power consumption and crosstalk
- minimize clock latency

RV-Skills center for emerging technologies

Graduate Trainee Engineer Aug-2022 to Feb-2023

Static timing analysis

Description

STA breaks a design down into timing paths, calculates the signal propagation delay along each path, and checks for violations of timing constraints inside the design and at the input/output interface.

Tools

Synopsys (PrimeTime)

Challenges

- Finding the factors which will influence these setup and hold violation
- Analysis timing reports with waveform
- understanding the concepts related to timing exceptions

B.E / B.Tech Academic Project

Rajarajeswari College of Engineering

Detection of Railway Track Fault Using Raspberry PI

Description

This project discusses the critical safety techniques for high-speed train operation environments based on train control. The proposed system uses a continuity sensor for crack detection and gives us results and the ability to pinpoint the location

Tools

Python Programming Language, Thonny python IDE Raspberry PI, RFID, Ultrasonic sensor, Continuity sensor, Buzzer

Challenges

- Integration of blocks and learning coding was challenging.