ANAND VENKAT SESHU BABU PINNIBOYINA
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Career Objective

Seeking an opportunistic role in VLSI domain to build a career as a physical Design engineer, by working in an organization where my abilities and skills will be utilized effectively for the betterment of myself and the organization.

Core Competancy

- Complete understanding of ASIC design flow from RTL to GSDII and PD flow involving Floor planning, Power planning, IR Drop Analysis, Automatic P&R, CTS and Routing.
- Good Knowledge of STA concepts like delay arc, fixing timing slack violations, CDC, SI, GBA, PBA, MCMM, OCV, AOCV, POCV, CRPR, time borrow, clock latency and useful skew.
- Good Knowledge of sign Off checks such as DRC, LVS, LEC, EM, IR Drop Analysis, ESD, ERC and antenna effects and methods of fixing them.
- Generated and analyzed timing reports of Pre-Layout and Post-Layout STA on Prime time and IC Compiler II and resolving timing violations.
- Good Knowledge of logical effort, PDK, DFT, low power implementation techniques and latest transistor technologies like Fin-FET.
- Good working knowledge of LINUX and TCL. Proficiency in analyzing and customizingscripts for automating design flow and debugging flow related issues.
- Analyzed and understood Design Constraints to specify PVT Corners, False paths, Half cycle, Multi Cycle paths, Asynchronous Clocks, CRPR.
- Hands on experience with Floor plan, power plan, Placement, CTS, Routing.
- Hands on experience on Synopsys Prime Time and PnR tool IC Compiler II, Xilinx ISE .

Education Details

Advanced Diploma in ASIC Design - Physical Design

VLSI GURU Training Institution

Master Degree in **VLSI & ES**

Jawaharlal Nehru Technological University, Kakinada.

Bachelor Degree in **Electronics and Communication**

LAKI REDDY BALI REDDY COLLEGE OF ENGINEERING, MYLAVARAM

INTERMEDIATE

SRI CHAITANYA JUNIOR COLLEGE, BHAVANIPURUM

SSLC

ST. ANNE'S HIGH SCHOOL, GUNTUPALLI

Domain Specific Project

VLSI GURU INSTITUTION
Graduate Trainee Engineer

FLOOR PLAN AND POWER PLAN

Description

A design with 28nm(finfet) and 14nm(mosfet) Technology, 40 Macros, 52007 Standard Cells, 4.2mm sq. area, 413MHz as Frequency, 1.95v as Operating Voltage as power budget Number of metal layers - 9.

Tools

Synopsys IC Compiler II

Challenges

- Manually placing hard macros using data flow diagram in such a way that to provide the maximum contiguous core area and to make all pins of the macros are accessible.
- Implementing power plan to meet the target IR drop and made power mesh DRC clean.
- Maintaining uniform orientation of hard macros and adding placement and routing blockages in required locations.
- Peforming timing checks using Zero Wire Load Model in order to qualify Netlist.

VLSI GURU INSTITUTION
Graduate Trainee Engineer

PLACEMENT AND CLOCK TREE SYNTHESIS

Description

Timing driven and congestion aware standard cell placement in Non-SPG flow is being done with optimum core utilization and building clock tree and routing all clock pins with optimized clock skew in both classic and CCD modes.

Tools

Synopsys IC Compiler II

Challenges

- Performed timing driven and congestion driven placement and HFNS in order to minimize logical DRCs by thus improving timing QoR.
- Synthesizing clock tree by providing NDR rules and performed detailed routing for all clock nets with DRC clean in both classic and CCD modes.
- Performed sanity checks before and after each stage of physical design flow.

VLSI GURU INSTITUTION

Graduate Trainee Engineer

ROUTING

Description

Routing all standard cell pins and hard macro pins using metal layers, performing via optimization and post route optimization by taking into account of cross talk effects on timing.

Tools

Synopsys IC Compiler II

Challenges

- Fixing antenna violations using metal hopping and antenna diodes manually.
- Clearing all DRC violations and LVS violations in order to make sure that design can be manufacturable.
- Analyzing timing reports and other reports in each stage.

B.E / B.Tech Academic Project

My Project is entitled as **"HYBRID POWER GENERATION SYSTEM USING SOLAR AND WIND ENERGY" .**it is a real time application

M.E / M.Tech Academic Project

My Project is entitled as" **IMPLEMENTATION OF 24 BIT MULTIPLIER USING PARALLEL MULTIPLICATION WITH SORTING BASED BINARY COUNTERS FOR VLSI APPLICATIONS".**