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Career Objective

To obtain a challenging and responsible position as a Physical Design Engineer enabling me to utilize my Technical skills that offers growth and advancement opportunities.

Core Competancy

- Acquired in-depth knowledge and proficient in ASIC PD Flow involving Floor planning, Power planning, IR Drop Analysis, Automatic P&R, Clock Tree Synthesis & Routing.
- Comprehensive Knowledge and hands on experience in STA, Interpreting timing reports, fixing hold and setup violations.
- Generated and analyzed timing reports of Pre-Layout and Post-Layout STA on Primetime, IC Compiler II and resolving timing violations.
- Worked on Floor plans for high utilization ratio and good contiguous core area, designed good power mesh to connect all macros and std-cells without any floating pins.
- Worked on placement plan with power aware and acceptable congestion ensuring good routability.
- Understood and modified TCL script and have written TCL scripts to extract information from timing paths, finding WNS and TNS.
- Analyzed and understood Design Constraint to specify PVT Corners, False paths, Multi Cycle paths, asynchronus Clocks, CRPR.
- Hands on Experience in APR Tools - Synopsis ICC2 and STA Tools - Prime time.
- Good Knowledge in Logic Design Concepts, CMOS, Semiconductor Theory and Basic Electronic Devices.
- Understood the Routing Flow and Fixed the DRC and LVS and Antenna Violations.

Education Details

Advanced Diploma in ASIC Design **2023**
RV-VLSI Design Center

Bachelor Degree in **Electrical and Electronics** **2022**
sree vidyanikethan engineering college, with 69 %

2018
sree chaitanya junior college, with 95 %

SSLC **2016**
sri sai vijetha schol, with 88 %

Domain Specific Project

RV-VLSI AND Embedded Systems Design Center

Graduate Trainee Engineer Oct-2022 to Feb-2023

Design of a SoC physical design block on 40nm tech

Description

Design of a SoC physical design block ready to integrated into a full chip. Overview : 40nm design, Clock frequency : 1GHz, shape : L-shape, Macros : 34, Standard cells : 47k, area : 4.2sq.mm, supply voltage : 1.1v, IR-Drop : 55mv, Metal layers : 7

Tools

Synopsys IC Compiler2

Challenges

- Understanding the design constraints and designing floorplan as per Data Flow diagram and using flylines to have contiguous core area for std-cells.
- Building a good power plan to meet the IR drop specified and ensuring that no floating pins, missing vias in the design and no PG DRC errors after building the power Network.
- To control congestion and DFT aware placement, tried different floorplan experiments and implemented different strategies.
- Understanding tool's behavior while clock tree synthesis to meet target skew, Min/ MAX latencies, fixing timing violations and understanding DRC and LVS errors

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RV-VLSI and Embedded Systems Design center

Graduate Trainee Engineer Sep-2022 to Oct-2022

Analysis of the Timing Reports (STA)

Description

For Flip flops and latch based timing paths working at different operating conditions for different timing paths. Timing reports are analyzed considering Uncertainty, CRPR, clock skews while honoring the constraints file.

Tools

Synopsys Prime Time, Synopsys IC Compiler2

Challenges

- Analyzed all the timing paths in different path groups and how some violations are reduced in the later stages.
- Differentiating some violations which are based on timing exceptions such as false paths, multi-cycle paths and reporting about the same to change in the constraint file.
- Understood the effects of CRPR, OCV, AOCV and skew factors in timing analysis

B.E / B.Tech Academic Project

sree vidyanikethan engineering college

ANALYSIS OF ISLANDING DETECTION AT DISTRIBUTED NETWORK

Description

Load balancing, voltage regulation ,network reconfiguration

Tools

MATLAB

Challenges

- Finding out the optimal the switch combination for the given distribution network such that the losses are minimized, and the time taken for the algorithm is less. Improve their profit margins on one hand by reducing unnecessary operational cost.