Sima Kumari

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OBJECTIVE

I would like to work with a team in a challenging and competitive environment where I could improve my knowledge, capabilities and put them to use for the development of the organization.

EDUCATION

- **National Institute of Technology, Durgapur, West Bengal** — Durgapur
  Master of Technology - Telecommunication engineering: CGPA: 9.2 — *Sept 2021-present*
- **Oriental Institute of Science and Technology, Bhopal, Madhya Pradesh** — Bhopal
  Bachelor Of Technology-Electronics & Communication; CGPA: 9.02 — *July 2017 - Dec. 2021*
- **Kendriya Vidyalaya Adra** — Adra, West Bengal
  12^{th} AISSCE; Percentage: 76.2% — *July 2014 - June 2016*
- **Kendriya Vidyalaya Adra** — Adra, West Bengal
  10^{th} AISSE; Percentage: 81.7% — *July 2013 - June 2014*

SKILLS

- **Languages** : C, Verilog, Tcl
- **Tools** : ICC Compiler, Cadence Virtuoso, Xilinx Vivado, EDEN(Intel specified)

PROJECTS

- **Internship Project:Timing and Power Optimization of Functional Unit Block in High Speed Core**: *Ongoing*
  - The core is periodically advancing towards new challenges with shrink in transistor size and progress of semiconductor industry . Transistor technology advancement has given the superior platform for fabricating high-performance multi-core processors with several innovative features . With every new generation core designing there comes the requirement to be developed to meet certain targets. From designer point of view, the new challenges in present day projects includes more stringent timing convergence and rigorous power reduction than in the previous studies.
  - Tools used: EDEN, TANGO and DUET.
- **Masters Project: Design and implementation of Arithmetic Logic Unit(ALU) and ALU controller using Xilinx Vivado.**: *Feb 2022-Jun 2022*
  - The objective of the project is to design and implement the arithmetic logical unit and its controller part.
  - Processor is a RISC-based architecture that is designed to reduce the complexity of the instruction set and ultimately improve the performance.
  - It has various inputs such as data, function bits, and ALU opcode, and output we get as zero, negative, overflow, bad flag. The ALU control inputs are generated as the result of the decoding of opcode and function bits. According to the output of the data, the various flags are set to 0 or 1.
- **Masters Project: Design and simulation of a traffic light controller design using Mealy and Moore FSM technique.**: *Dec 2021-Dec 2021*
  - In this project we designed a traffic light controller using both the art of FSM technique via. Mealy and Moore's machine using module and testbench. It is used to determine the better PPA (power, performance, and area) of the particular design.
  - After finding the number of states for each of the machines, the state model is designed.
  - Tools used: Xilinx Vivado and Synopsys Design Compiler
- **Bachelors Project: IoT based water level indicator using NODEMCU which control the level of water in a tank and shows all the details of water level on the Blynk application and as per the requirement the pump is made on and off with the help of the Blynk app**: *Aug 2016-Dec 2017*
  - Tools used: Arduino IDE, Blynk application, PCB Wizard, NodeMCU.

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AREA OF INTEREST

- Backend Memory Circuit Design
- Understanding about Synthesis, STA analysis
- MOSFET's, CMOS Technology
- Placement, Floor planning, Routing, CTS
- ASIC Flow

INDUSTRIAL EXPERIENCE

- Successfully completed a internship program at Intel Pvt. Ltd. India, a renowned company in the field of technology, gaining hands-on experience and valuable insights into the industry. *Jul 2022-Jun 2023*

ONLINE COURSE AND MTECH CURRICULUM

- Verilog Language and Application(Online), 32 hours *20th Oct 2021 - 31th Nov 2021*
- Udemy RTL-to-GDSII Flow (Online), 12 hours *1st Jan 2021 – 15th Feb 2021*
- Title: Understanding CMOS Design by implementing the architecture using Cadence Virtuoso by analyzing the parameters.
    - The intent of the project is to get a deep-down understanding of CMOS logic with the help of the VTC curve and determine the design parameters like noise margin, rise time, fall time, propagation delay, electrical effort, and fanout capability.
    - Tools used: Cadence Virtuoso (180nm technology).
    - Challenges: To judge the symmetry of the VTC curve and determine the trip point of voltage and its impact with a different threshold voltage.
- Design and implementation of CMOS gates and doing hands-on placement, routing, floor planning, CTS.
    - Logic circuits are optimized in terms of area, speed, performance, and power.
    - Tools used: ICC Compiler and Cadence Virtuoso.

RELEVANT COURSES

- VLSI Design
- Electronic System Design
- Digital Integrated Circuits
- System On Chip Design
- VLSI Design Lab

PARTICIPATION

- Hold the position of CR (class representative) in NIT Durgapur.
- Participated in Tech acme 2018 of OIST Bhopal in Circuit designing event.
- Participated in Tech acme 2018 of OIST Bhopal in Robotics race event.
- Participated in CHIMERA-X 2018 of MANIT Bhopal.