Hema R

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Bangalore-560091, Karnataka

Career Objective

Seeking a position in Physical Design field to utilize my skills and abilities that encourages continuous learning and allows professional advancement while being creative , innovative and flexible.

Core Competancy

- Acquired working knowledge on ASIC PD flow, APR flow that involves Floorplan, Power plan, IR Drop Analysis, Placement, Clock Tree Synthesis and Routing.
- Hands on experience in industry-standard tools - Synopsys IC Complier, Prime time.
- Gained knowledge of ASIC Flow from Netlist to GDSII.
- Good understanding on fundamentals of Logic Design , CMOS and semiconductor theory.
- Good Knowledge of Linux and scripting languages like PERL, TCL and C programming.
- Experience in working on verification flows like DRC, LVS, IR drop, Antenna and Timing changes etc.
- Designed an ASIC Block in 40nm technology.
- Strong communication Skills.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**

JSSATEB, with 8.96 CGPA

2018

MES PU COLLEGE, with 94 %

SSLC **2016**

ANPS, with 95.36 %

Domain Specific Project

RV-VLSI Design Center

Graduate Trainee Engineer Oct-2022 to Feb-2023

Block level design -Sub system

Description

Physical design and Implementation of the block level design consist of 34 Macros and around 160 K core logic, with a supply voltage of 1.1v, 5% max IR drop, block was design to operate at 400MHZ and the design was implemented with 7 layers of metal.

Tools

Synopsys IC-Compiler, Prime Time

Challenges

- Developing a reliable floorplan with channel spacing to control the congestion throughout the PnR stage for the ease of routing and building clock tree.
- Generated timing reports at every stage of PD flow and analyzing the TNS, WNS, Delays, Clock Skew, Transitions violations, CRPR, Network and Source Latency.
- Developing an ASIC Block free from DRC,LVS,DFM, Setup, Hold and slew violations for final tape-out.

B.E / B.Tech Academic Project

JSSATEB

BATTERY AUTHENICATION FOR LI-ION BATTERIES

Description

With the use of a microcontroller-based authentication system that uses the UART protocol, the project goal is to protect leased batteries from physical counterfeiting while also verifying the charging process.

Tools

Hardware : Arduino uno and nano, Relay, BC547 transistor, LCD display Software : Embedded C, MATLAB, Arduino IDE

Challenges

- Debugging hardware faults. Improving code strength. Hardware synthesis using MATLAB.