ANNAPOORNA HM
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PROFESSIONAL SUMMARY

- **1 year** experience as **ASIC Verification Engineer.**
- Good experience in **debugging** and **analyzing** code.
- Proficient in writing **SV** and **UVC Testbench** from scratch.
- Experience and knowledge on **standard protocols** like **PCIe (5.0)**, **AXI**, **SPI** and **APB.**
- Hands-on expertise of working on **Design and Testbench development** in **Verilog, System Verilog and UVM** environment.
- Understanding of RTL **design/verification** concept.
- Possess knowledge in **Functional Coverage**, **Code Coverage**, and **Assertions**.
- Good knowledge in **Digital System, Verilog, System Verilog** and **UVM.**
- Excellent written and oral communications skills.
- Hands on experience on all standard **Simulation tools** like **Questa Sim, ModelSim, EDA Playground.**

EMPLOYMENT HISTORY

March 2022 – Present: Scaledge Technology, Bangalore Verification Engineer

PROFESSIONAL EXPERIENCE

PROJECT DETAILS

Project Name: PCIe 5.0 -Verification **3 months**

Description: In this project, we had to learn the working of PCIe protocol and its features. PCIe Gen-5 (**Peripheral Component Interconnect express**) is an interface standard that is used to connect motherboard with **High-speed Components** (GPU, WI-FI cards, SSD). PCIe is available in a different physical configuration which includes **x1, x8, x16, x32** depending upon the **Lanes**. It has mainly three layers called as **TL, DL** and **PL** that configured to transfer always a good packet.

Roles & Responsibilities:

- Understanding the **PCIe layers working**, and understanding the **protocol specification**.
- Develop **Test**, **Checker** & **Coverage** plan for its features.
- Installing and interfacing the back-to-back Synopsys VIP.
- Understand the **VIP environment** and run basic test cases to understand the flow of RC-EP.
- Working on the assertion plan and **development** of **test cases** as per test plan.

Working Tool: QuestaSim and GVim
Methodology: UVM
Language: System Verilog

Project Name: AXI Protocol Verification **1 month**

Description: AXI3 is an **AMBA protocol** used for high **performance.** Developed AXI UVC based testbench architecture and all the UVM component and **validated it** for various **AXI features.**

Roles & Responsibilities:

- Understanding the **AXI protocol Specifications.**
- Listing the **AXI features** and developing **Test plan**.
- Developing an environment with master agent and slave agent.
- Interfacing the **testbench** with **design**.
- Developed **Functional testcases,** developed **functional coverage** and **scoreboard**.

Working Tool: QuestaSim and GVim
Methodology: UVM

Project Name: APB Functionality Verification **15 days**

Description: **APB** is an **AMBA** protocol used for low performance applications. Worked on UVC development for APB. UVC was developed to work as both Master and Slave. Developed all the UVC components and validated UVC for various APB features.

Roles & Responsibilities:

- Reading and understanding **Specifications**.
- Developed the UVC **Architechure**.
- Developed the test bench using **UVM** to generate test case.
- Developed **functional coverage**.

Working Tool: **QuestaSim**

Methodology: **UVM**

Project Name: MEMORY TB development **5days**

Description: Developed design code for Memory Slave in Verilog for basic functionality and developed Testbench for the same. Checking basic memory write and read transactions with handshaking signals for understanding coding using System Verilog. This project also involved understanding of **OOPs concepts**.

Roles & Responsibilities:

- **Developing** the **RTL** code.
- Interfacing **generator**, **bfm** and **mailbox**.
- Interfacing the testbench with design.
- Checked Various features such as:
  - Number of agents we are adding based on our needs.
  - Developed concept so that our simulation end in smooth manner.
  - For avoiding meta-stability state, we add clocking block and mod-port concept.
- Developed **Functional** and **Code coverage.**

Working Tool: **ModelSim, Eda Playground**

Language: **System Verilog.**

Project Name: SPI Protocol **10 days**

Description: The Serial Peripheral Interface is a synchronous serial communication interface specification used for short-distance communication, primarily in embedded systems. This project involves understanding of **SPI Protocol and the external blocks it interfaces with**.

Roles & Responsibilities:

- Implementation of **design code** for SPI Controller.
- Implementation of **programming** the **registers** and handling of SPI Protocol behavior.
- Understanding the **working of state transition** of SPI Protocol from when it's in idle state till it has pending transactions to complete.
- Written **testbench** for the verification of the **functionality as expected.**

Working Tool: **ModelSim, GVim.**

Language: **Verilog**

TECHNICAL SKILLS

Languages:	**Verilog, System Verilog, UVM.**
Tools Used:	**QuestaSim, ModelSim, GVim, Xilinx ISE, EDA Playground.**
Methodologies:	**UVM.**
Operating System:	**Windows, Linux (Basics).**
Other Tools:	**Proteus, EasyEDA, KiCAD.**
Other Skills:	**PCB Designing.**
Protocols:	**PCIe, AXI, APB, SPI**

EDUCATION

- **B.E(Electronics and Communication) from Sri Venkateshwara College Of Engineering in the year 2022 with 8.78 CGPA/GPA.**
- **2nd PUC from Seshadripuram College (Main) in the year 2018 with 8.7 CGPA.**
- **10th from Army Public School, PRTC in the year 2016 with 8.5 CGPA.**