ANKIT KUMAR

8306757916 | akssm3009@gmail.com | linkedin.com/in/ankit-kumar-9992271b9

Objective

I intend to establish myself as a VLSI professional looking forward to an opportunity that will help me to realize my potential, enhance my skill set in the field of VLSI technology, and contribute to the organization growth.

Skills Summary

HDL & HVL	: Verilog, System Verilog, UVM
Protocol Known	: UART, PCI Express (Learning)
EDA Tools	: ModelSim, Quartus prime, Esim (Open-source EDA tool for circuit Simulation)
Hardware Tool	: Proteus, Ansys HFSS, Multisim, Simulink
Operating System	: Window, Linux (Beginner)

Certification Course

Certification course	Duration	Organization
Industrial Training in Advanced VLSI FRONT END	July 2022 - Present	FutureWiz (Truechip-Solution)
System Verilog for verification	Dec 2022 -Feb 2023	Udemy
VLSI System on Chip Design	Dec 2022	Maven Silicon

Awards and Reconigation

Project of the year in 3rd -year ECE department (1st prize) – Sensor Driving Using Thermoelectric generator.

Project Details

Project 1:

Project Title	**: Mixed-signal PLL (Phase lock loop) using google SKYwater pdk (130nm)**
HDL	: Verilog
EDA Tools	: Esim (Open-source EDA tool for circuit simulation)
Description	# Design and Simulation of wide tuning range and fast locking PLL using google skywater-pdk. # Design and verify different blocks of PLL using Verilator, Subcircuit builder, Kicad and Ngspice.

Project 2:

Project Title	**: Dual-Port Ram(DPRAM) Design and verification using System Verilog, UVM**
HDL	: Verilog, System Verilog,UVM
EDA Tools	: Quartus Prime, Modal Sim
Description	# Implemented the Dual Port Ram Using Verilog. # Architected the class-based verification environment using the system Verilog.

Project 3:

Project Title	**: Sequential D-Flip Flop Design and verification using System Verilog**
HDL	: Verilog, System Verilog
EDA Tools	: Quartus Prime, Modal Sim
Description	# The system design of a T intersection traffic light controller. # Design the RTL level code for the traffic light controller using a finite state machine and verify Its waveform by writing testbench code in Verilog.

Project 4:
Project Title : Traffic Light Controller using Verilog
HDL : Verilog
EDA Tools : Quartus Prime, Modal Sim
Description # The system design of a T intersection traffic light controller.
Design the RTL level code for the traffic light controller using a finite state machine and verify Its waveform by writing testbench code in Verilog.

Project 5:
Project Title : Sensor Driving using Energy Harvesting (Thermoelectric Generator)
Hardware Used: Arduino Mega 2560, Matrix Mercury Boost Converter Prototype kit
Description # Drive a low-power sensor by generating voltage with the help of a thermoelectric generator and stabilize its output using a DC-DC booster.
Developed a Hardware modal of a Thermoelectric generator on the aluminum sheet to generate Potential gradient.

Education

Education	Institution/ University	Year of Passing	Percentage
Industrial Training in Advanced VLSI	FutureWiz	2022-Present	-
Bachelor of Technology in Electrical & Electronics Engineering	Bennett University	2023	76.4%
XII	S.N. College Shamal Khaira, Bihar School Examination Board (BSEB)	2018	64.4%
X	DAV Public School Sasaram (CBSE)	2016	95%

Extra Circular Activities
Playing Cricket, Reading book

Personal Details

Father's Name: Hari Mohan Singh
Date of Birth: 05/05/2000
Languages Known: Hindi, English
Nationality: Indian

Declaration

I hereby declare that the above information is true and correct to the best of my knowledge and I have all the necessary documents for the same.
Place: Greater Noida
Date: 23-02-2023