Vineeth Raj R

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Career Objective

Seeking for a challenging position as a Physical Design Engineer where I can learn new skills, and expand my knowledge.

Core Competancy

- Comprehensive Knowledge and proficient in ASIC PD flow involving Floor Plan, Power Plan, IR-Drop analysis, Automatic Place and Route, Clock Tree Synthesis and Routing.
- Worked on Floorplan to have more core area and designed a good Power plan to connect all macros and standard cells with no DRC as well as meeting the IR-Drop.
- Worked on Placement plan to make the congestion acceptable.
- Worked on CTS and Routing Flow and Fixed all Possible DRC and LVS violations.
- Analyzed the timing paths in different path groups at every stage of flow (floorplan, placement and CTS).
- Understood and Modified Tcl scripts and have written Tcl scripts to extract information.
- Analyzed the timing reports of Pre-Layout and Post-Layout STA on PrimeTime and IC Compiler2 and Understood the effects of CRPR, OCV, AOCV, and skew factors.
- Analyzed and Understood Design Constrains to specify PVT corners, False path, Multicycle path, Asynchronous clocks.
- Hands on Experience in APR Tool - Synopsys ICC2 and STA Tool - PrimeTime.
- Good knowledge in Logic Design concepts, CMOS, MOSFET, Semiconductor Theory and Basic Electronic Devices.

Education Details

Advanced Diploma in ASIC Design **2022**

RV-VLSI Design Center

Bachelor Degree in **Mechatronics Engineering** **2021**

Kumaraguru College of Technology, with 7.64 CGPA

2017

Metro Matriculation Higher Secondary School, with 86 %

SSLC **2015**

Metro Matriculation Higher Secondary School, with 95.2 %

Domain Specific Project

RV-Skills

Graduate Trainee Engineer Jul-2022 to Sep-2022

Design of an ASIC Block

Description

This design is aimed for Floorplan, Power plan and Placement. The design block is from 40nm Technology, Clock Frequency -1 GHz, Supply Voltage-1.1V, Power consumption-600mWatts, IR-Drop Budget-55mV, Macros-34, Standard Cells-40k, Metal Layers-7.

Tools

Synopsys IC Compiler2

Challenges

- Understanding the design constrains and placing the Macros in such a way that makes the Floorplan good and having Core area to place the std-Cells, Boundary Cells, Tie Cells, etc.
- To make a good power plan and to meet the IR drop specified, gone through some iteration of values for width, spacing, pitch and offset of metal layers.
- To make a power plan that has no floating pins, missing vias in the design and no PG DRC errors after completing the power network.
- To Ensure that the congestion should be acceptable, gone through many iteration and tried with different floorplans to control the congestion.

RV-Skills

Graduate Trainee Engineer Jul-2022 to Sep-2022

Design of an ASIC Block for CTS and Routing

Description

This design is aimed for Clock Tree Synthesis and Routing. The design block is from 40nm Technology, Clock Frequency -1 GHz, Supply Voltage-1.1V, Power consumption-600mWatts, IR-Drop Budget-55mV, Macros-34, Standard Cells-40k, Metal Layers-7.

Tools

Synopsys IC Compiler2

Challenges

- Understanding and Modifying some app-options to analyze the Classic flow as well as the Concurrent Clock and Data optimization(CCD) flow to see the difference between them.
- Analyzed the DRC errors like Shorts, Spacing issues, Antenna Violations and Fixed them by Manually Routing some of the metal layers.
- Understanding the concepts of metal jumping, Diode Insertion and resolved the Antenna Violation in both of these methods.
- Analyzed and understood the timing reports that how the tool trying to meet the target skew, and decreasing the setup & hold violations.

RV-Skills

Graduate Trainee Engineer Jul-2022 to Sep-2022

Analysis of Timing Reports (STA)

Description

For Flip flop and latch based timing paths, analyzed the timing reports considering OCV, AOCV, uncertainty, CRPR, and certain exceptions like false path, multi cycle path.

Tools

Synopsys PrimeTime and Synopsys IC Compiler2.

Challenges

- Analyzed all the timing paths in different path groups at every stage of flow and observed how some violations are reduced in the later stages.
- Understanding and calculating the setup slack and hold slack for different timing paths which includes external input/output delays, CRPR.
- Differentiating some violations which are based on timing exceptions such as false paths, multi cycle paths, min./max. delay paths.

B.E / B.Tech Academic Project

Kumaraguru College of Technology

Secure Entrance for Covid-19

Description

This project is aimed and designed to maintain precautionary measures like social distancing, wearing of mask and monitoring body temperature.

Tools

Raspberry pi OS, Python, Raspberry pi 3, Raspberry pi camera and a Thermal Scanner.

Challenges

- Measuring the distance between people for social distancing was very challenging. Detecting people with and without mask was challenging.