JAGANNATH KUNDU

Completed MTech(2020-2022) in ECE at NIT Durgapur | E-mail –jagannathkundu2013@gmail.com

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Career Objective :

Currently looking for a job in VLSI industry in Frontend Domain. I am eager to learn and work as a Design Verification engineer & contribute to the growth of VLSI industry .

Academic Qualification:

Degree	Discipline	Institute	Board / University	Year of Passing	Aggregate % / CGPA
M. TECH	Electronics and Communicatio n Engineering	Nit Durgapur	NIT DGP	2022	9.1
B. TECH	Electronics and Communicatio n Engineering	Techno India, Salt Lake	MAKAUT	2020	7.71
Diploma	Electronics and Telecommunicati on Engineering	Contai Polytechnic	WBSCTE	2017	76.4
Secondary Education	All Subject	K.J.K.H.S	WBBSE	2011	62.3

TECHNICAL SKILLS :

- Hardware Description Language – **Verilog, System Verilog**
- Tools – **GVIM, Eda playground, Modelsim, Questasim**
- Programming & Scripting Language – C ,C++
- Software packages – MS office word , excel, power point, CST, Matlab
- Subject Knowledge –**Digital Design**, Electronics device & circuit , Control System

PROFESSIONAL VLSI TRAINING :

VLSI Design & Verification Trainee 15th Mar 2022 – Present

VLSI GURU Training Institute, Bangalore

AREA OF INTEREST :

- Design Verification, Functional Verification, RTL Design

TRAINING / PROJECTS :

Design and Verifications of Synchronous & Asynchronous FIFO *Verilog HDL*

- ***Description*** - In this design after releasing the reset , writes and reads happen to FIFO at the edge of the clock then generating Full and empty conditions. In testbench apply the testcases concurrent writes reads, FIFO full error, FIFO empty error, same for asynchronous FIFO but different is having write and read will clock domain.
- ***Observations*** - To understand the write, read toggle flag. Empty (synchronized write pointer to read clock domain) and Full (synchronized read pointer to write clock domain) generation is difficult for asynchronous FIFO. FIFO Full & Empty error will Depend on write, read delay and write, read clock time period.

Implementation of Different Size Memory *Verilog HDL*

- Reset all the memory content and read all the locations that we should get zero data, after releasing the reset ,write(when write enable high) and read(when read enable high) happen to the memory.
- Accessing memory contents by generating transactions on memory interface or by using memory hierarchy, In testbench apply the testcases front door write & read and back door write & read.

RTL coding and verification of Pattern Detector *Verilog HDL*

- It help to detect specific user defined pattern, when reset apply, reset all the reg variable else apply the state and next state will change based on current state and current input (change every position edge of the clock) whenever pattern detected output get 1 and count the pattern.

B. Tech project on :

Wi-Fi Control Home Automation System: We have remote controls for our television sets and other electronic system, which have made our real easy. We have come up with a new system called Arduino based home automation. The ESP8266 Wi-Fi module is a self-contained with integrated TCP/IP protocol stack that can give any microcontroller access to your Wi-Fi network.

M. Tech project on :

Isolation Enhancement of MIMO Antennas using Stub: Multiple-input multiple-output (MIMO) scheme refers to the technology where more than one antenna is used for transmitting and receiving the information packets. It enhances the channel capacity without more power. The system has a wide bandwidth range from 2–13.7 GHz.

Certifications and Achievements :

- Certificate in industrial trainings of Advanced IoT with Cloud Architecture.
- GATE 2020 Qualified in ECE specialization

Personal profile :

Name	:	Jagannath Kundu
D.O.B.	:	02/02/1996
Gender	:	Male
Permanent Address	:	Vill-Kantabari, P.S-Onda, Dist-Bankura, West Bengal-722122
Languages Known	:	Bengali, Hindi, English

Date –

Place – NIT Durgapur (Jagannath Kundu)