Kanthamani

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Professional Goals

To build a career in VLSI domain by working in an organization where my ability and skills will be utilized effectively for the betterment of myself and the Organization

Core Competency

- Trained in Sanity Check, Floorplan, Power plan, Placement, CTS, and Routing
- Good knowledge and understanding of STA concepts: Fixing setup and hold violations, understanding of timing reports, CRPR, effect of skew on timing, OCV, latch concepts
- Hands on experience on VLSI tools: ICC1 COMPILER
- Good Understanding of Digital Logic Design, Network Analysis, CMOS
- fundamentals Good knowledge on Unix/Linux –TCLfundamentals/scripting
- Hands-on experience in Verilog programming and Test-bench based
- Verification Basic knowledge on IC fabrication process
- Understanding of complete ASIC design flow and Physical Design flow

Academic History

Advanced Diploma in ASIC Design - Physical Design, Takshila Institute of VLSI Technologies, Bangalore (December 2022)

Bachelor Degree in Electronics and Communication, Government Engineering College K R Pete(2019-2022)(8.17 CGPA)

Diploma in electronics and Communication, JSS Polytechnic for women Mysore (2016-2019)(81.32%)

Pri-University PCMB, Govt PU College for Girls K R Nagara(2014-2016)(61.66%)

Secondary School Leaving Certification (SSLC), Government High School Thippuru (2014) (77.12%)

Domain Specific Projects

Takshila Institute of VLSI design, VLSI Design Centre, Bangalore.

Physical Design Trainee

1) SOC Block level Implementation of ORCA_TOP_IO Project (28nm Technology node)

Tool: ICC2 compiler by Synopsys

Description:

Currently working on SOC Block level Physical design which involves implementation of

- Sanity Check, Design setup, Floorplaning
- Power planning, Placement and clock tree synthesis
- Routing, Physical Verification DRC, LVS, and DFM checks
- Signal Integrity and Back Annotation
- Sign-off checks and Tapeout

2) SOC Block level Implementation of ORCA_TOP Project (32nm Technology node)

Tool: ICC2 compiler by Synopsys

Description:

Completed SOC Block level Physical design which involves implementation of

- Sanity Check, Design setup, Iterative Floorplaning , Power planning, Place and CTS optimisation
- Routing, Physical Verification , DRC, LVS, and DFM
- checks Signal Integrity and Back Annotation
- Timing Closure and ECO Sign-off checks and Tapeout,

3) Static Time analysis

Description:

Complete analysis of different types of timing paths by using slew and delay tables for single clock & Multicycle clock by considering constraints such as clock skew, uncertainty, input delay and output delay and derate factors.

Challenges:

- Computing setup slack and hold slack for different timing paths by using skew and delay tables finding worst slack and best slack for setup and hold
- Understanding the causes for setup violation and hold violation
- Generating and analyzing timing reports in PT shell for the given timing paths
- Understanding of clock abnormalities and timing exceptions
- Understanding of derate factors, PVT corners, Global variations, OCV and AOCV

Academic Project

- Title: Brain tumor separation from a brain tumor image using Python
- Tool: Anacoda software in Spyder 3.0

Skills

- Logic Design
- Physical Design
  - Sanity Checks
  - Floorplan & Power plan
  - P&R
  - DRC
- Static Timing Analysis
- Linux, Shell,TCL Scripting Fundamentals
- Synopsys IC Compiler (ICC)

Personal Details

Date of Birth : 05/01/1999

Address : D/O Kantharaju Thippuru(V&P), K R Nagara(T), Mysore(D)-571602

Languages Known :English, Kannada.

Declaration:

I hereby declare that I would be glad to come for interview at any time that is convenient to you and assure you of my devoted service.

Date: **Kanthamani**

Place:Bangalore