

Mahima Sanjay Tekale

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OBJECTIVE

To build my career in VLSI domain and looking for opportunity to improve my technical abilities in Physical Design which provides me self-development and help me achieve personal as well as organization goals.

PROFESSIONAL EXPERIENCE

INTERNSHIP, VLSI Guru Training Institute

Role : Trainee.

JULY 2022 - FEB 2023

A 7 months internship program includes,

Digital Electronic, Combination and Sequential circuits, FSM, Memories.

Basic PD, CMOS design, ASIC flow.

Advance PD, Floorplan, Powerplan, Placement, Clock Tree Synthesis, Routing.

STA, STA basics, Timing path and constraints, Different types of clocks.

EDUCATION

Course	College/ School	University/ Board	Aggregate
BE [E&TC]	NDMVP's Karmaveer Adv Baburao Ganpatrao Thakare College Of Engineering	Savitribai Phule Pune University	8.66 CGPA
Diploma	NDMVP's Rajarshi Shahu Maharaj Polytechinc	Maharashtra State Board Of Technical Education	79.53%
10th	Navarachana Vidyalaya	Maharashtra State Board Of Education	77.20%

INTERNSHIP PROJECTS (VLSI-Domain)

- **ORCA TOP (Multi Voltage, Block Level)**

Hard macros: 40
I/O Ports: 240
Frequency: 450MHZ
Number Of Clocks: 8(3 main clocks,3 generated clocks, 2 virtual clocks)
Process Technology: 28nm, 9 routing layers
Complexity: 52k gates (approx.)

ACADEMIC PROJECTS

- **Fog Based Handwash**
Cleaning of hands by using fog to save water.
- **Density Base Traffic Signal**
Aim of project is to control traffic using IR sensor and micro-controller.

SKILLS

- TCL Scripting language.
- Digital electronics and CMOS design.
- ASIC flow (RTL to GDSII).
- Floorplan, Powerplan, Placement, CTS, Routing and STA.
- Application Software: ICC2, GVIM, Cygwin.

PERSONAL DETAILS

- **DOB:** 03-09-2000
- **Gender:** Female
- **Nationality:** Indian
- **Location:** Nashik (Maharashtra)
- **Languages:** English, Hindi, Marathi.

DECLARATION

I hereby declare the above-furnished details are true to the best of my knowledge.

Date: 09-02-2023

Mahima Sanjay Tekale