Deepika Patil

Design And Verification Engineer at Mirafra Technologies Pvt. Ltd

Tel: +91-9611659693
Email id: deepikapatil2451@gmail.com
LinkedIn id: https://www.linkedin.com/in/deepika-patil-aa4292186

PROFFESSIONAL SUMMARY

Have been working as a Design and Verification Engineer close to 2 years .Have a good understanding of verification environments,knowledge on SV and UVM.

WORK EXPERIENCE

- Working as **Design and Verification** Engineer at **Mirafra Technologies Pvt. 2 years of experience**.
  - Develop UVM functional validation tests in System Verilog to verify design requirements are met at IP Level.
  - Architect highly modular verification collateral in the form of monitors, scoreboards, and checkers in simulation environments.
  - Analyzed coverage gaps and carried out strategies to achieve 100% coverage.

Project 1 : Subsystem Validation

1. **Company:** ARM (On Contract)
2. **Duration:** JULY 2022-NOV 2022
3. **Description:**
   - I worked on bring up of subsystem which covers integration , integration testing, Clock, Power and OS boot on Emulator
   - **Integration involves:**

     Connecting ARM IPs like Cluster with CMN Interconnect (CMN-600 ,CMN-7000, Interrupt controller (GIC),System Control Processor , ROM ,RAM, Network interconnects (NIC400) ,mMemory controller and Debug component using AMBA buses like AXI,APB and AEM low power interfaces.

   - **Validation involves**:

     Running C based test cases which covers most of part of Subsystem like System Boot Flow followed by payloads which covers CPU to Memory access through Interconnect, coherency based test cases, Interrupt controller initialization to check any unexpected interrupt occurring in system, System, CPU & Cluster Power Cycling involves different kind of power modes and clock frequency randomization to check across all clock domains to check any clock connectivity issues, different Reset scenarios validation at System level.

Project 2 : Pulpino SPI master Subsystem Verification

1. **Company:** Mirafra Technologies pvt,ltd
2. **Duration:** March 2022- April 2022
3. **Description:**
   - The pulpino subsystem uses AXI as its main interconnect with a bridge to APB for simple peripherals both the AXI and APB buses feature 32-bit wide data channels.
   - Developed Coverage plan according to RTL specification
   - With the help of submodules get the required SPI and AXI AVIPs collaterals
   - Examine functional and code coverage and generated coverage report

Project 3 : Verification of AXI-AVIP

1. **Company:** Mirafra Technologies Pvt. Ltd
2. **Duration:** *Jan 2022 – Feb 2022*
3. **Description:**
   - AXI4 is suitable for high bandwidth and low latency design. It provides high frequency and high throughput • It is a burst-based protocol which supports the features of blocking and outstanding transactions • Developed a accelerated vip architecture
   - Created the converted files on master slave to convert the transaction packets into struct packet and vice versa
   - Implemented the master monitor proxy and slave monitor proxy which passes the converted packets to hdl
   - Worked on scoreboard comparison and checked the address and data matched or not

Project 4 : Verification of SPI-AVIP

1. **Company:** Mirafra Technologies Pvt. Ltd
2. **Duration:** *Oct 2021 - Nov 2021*
3. **Description:**
   - The SPI is a full duplex interface both master and slave can send data at the same time via the MOSI AND MISO lines respectively. Accelerated VIP is used to increase the working frequency for the TB as it is working in an emulator where TB is having two top HDL/HVL
   - Testbench development of vip architecture
   - Developed a scoreboard, implemented an analysis fifo for checking
   - Created environment including components like agent on the hdl side which is using bus functional model consists of the slave and monitor diver BFM
   - Worked in Assertion and coverage.

- **Professional Development Training in VLSI** at **Sandeepani** – School of Embedded System Design, Authorized Training Partner **(ATP)** For **Xilinx**, from **2019-2020** Specializing in VLSI Design and Verification.

Skills

- HDL: Verilog.
- HVL: System Verilog.
- TB Methodology: UVM.
- SPI IP Verification, AMBA AXI IP Verification, AMBA APB IP Verification.
- ARM IP Verification : DSU(Cluster), CMN Interconnect, AXI, APB.
- Basic knowledge of C (Programming Language).
- Basic knowledge of Python.
- Works on EDA Tools like Model-Sim & Questa-Sim by Mentor Graphics, Vivado by Xilinx, Strato, Z1
- Basic knowledge of ASIC/FPGA Design Flow.

Summary

I am currently working on various internal projects. As a Design and Verification Engineer, my main task is to design Test Bench architecture and write test plans for both IP Level test benches. I am also responsible for integrating different components in a UVM-based architecture and analyzing the test result. I am skilled in Verilog, System Verilog, UVM, Digital Design, RTL Designs, C, and Python with a strong Engineering Background in Electronics and Communication.

EDUCATION

Bachelor of Engineering (BE) **2015-2019**

(Electronics and communication)

Godutai Engineering College of Women, Gulbarga

GPA 7.2/ 10

PUC **2013-2015**

Muktambika PU College for Science, Gulbarga

Percentage 74%

SSLC

Kannada Convent High School, Gulbarga **2012-2013**

Percentage 65%

Personal Details

Nationality: Indian

Father's Name: Revansiddappa Patil

Language: Kannada, Hindi, English

Declaration

I, hereby, declare that the above information is true, complete, and correct to the best of my knowledge. **Signature: Deepika Patil**