## Trisant Ray

trisant9@gmail.com, 8653974166

CHAKDAHA-741222, West Bengal


## Career Objective

A physical design trainee to acquire advanced knowledge in my concern. Seeking a challenging career where my academic excellence will add value towards organization and personal.

## Core Competancy

- Through understanding on ASIC flow and practical experience on APR flow that includes Floorplanning ,Powerplanning, placement ,CTS and Routing .
- Understanding in Various STA concepts such as Timing paths, Timing Arcs ,Slack, timing constraints, PVT corners, clock Skews, Fixing timing violations ,CRPR, AOCV.
- Developed a power network with no physical DRC errors and also made sure to meet the specified IR drop by varying the width ,Spacing and pitch of the metals.
- Developed an floorplan with contiguous core area, good utilization and required channel pacing with the help of flylines and data flow diagram.
- created a legalized placement block with minimal congestion, no DRC errors and no floating standard cells.
- Generated timing reports at every stage of PD flow and analyzed the TNS ,WNS, delays ,clock skew, transition violations, network latency and source latency.
- Hands on experience on tools Synopsys IC compiler II , Synopsys Primetime.

## Education Details

**Advanced Diploma in ASIC Design - Physical Design** **2023**

RV-VLSI Design Center

**Bachelor Degree** in **Electronics and Communication** **2022**

TECHNO MAIN SALT LAKE, with 78.54 %

**2019**

JIS SCHOOL OF POLYTECHNIC, with 74.2 %

**SSLC** **2016**

CHAKDAHA RAMLAL ACADEMY, with 72 %

## Domain Specific Project

**RV -VLSI AND EMBEDDED SYSTEMS DESIGN CENTER**

*Graduate Trainee Engineer* Oct-2022 to Feb-2023

**Floorplan, Powerplan and placement implementation**

**Description**

Block level implementation of Lakshya subsystem:Technology-40nm ,supply voltage 1.1V, Area-4.2 sq. mm, Power budget-600nW, Max IR drop (VDD+VSS)-5%, No. of standard cells 38403, No. of metal layers 7.

**Tools**

IC Complier II- Synopsys

**Challenges**

- Building a Powerplan to maintain power network connectivity and IR drop. Also ensuring that there were no missing vias,floating wires and power-ground DRC violations.
- Designing a Floorplan by determining Macro placement as per dataflow diagram and using the macro guidelines in order to achieve contiguous core area and good utilization.
- Creating a placement block by inserting Pre placement cells, sufficient spacings in order to control the congestion and DRC violations obtained.
- Analyzing of timing reports and identifying the cause in the timing path for which its being violated and overserving the WNS,TNS at various stages of the flow.

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**RV -VLSI AND EMBEDDED SYSTEMS DESIGN CENTER**

*Graduate Trainee Engineer* Oct-2022 to Feb-2023

**CTS & Routing Implementation**

**Description**

Block level implementation of Lakshya subsystem:Technology-40nm ,supply voltage 1.1V, Area-4.2 sq. mm, Power budget-600nW, Max IR drop (VDD+VSS)-5%, No. of standard cells 38403, No. of metal layers 7.

**Tools**

IC Complier II- Synopsys

**Challenges**

- Analyzing clock tree to achieve minimum insertion delay and skew. Also checked rectified for the clock DRC errors.
- Performing clock tree synthesis and optimization using classic ,CCD flows and analyzing the tools behavior by comparing the timing reports in both the flows.
- Analyzing and resolving the antenna violations by inserting the metal jumper and the diode into the layout .

**RV -VLSI AND EMBEDDED SYSTEMS DESIGN CENTER**

*Graduate Trainee Engineer* Sep-2022 to Feb-2023

**Analyzing the Timing Report by STA**

**Description**

Generating of timing reports that include setup and hold slack calculations for flip flops and latch based paths working at various condition, reports and analyzed considering OCV, uncertainty CRPR, and timing exceptions (multicycle and flash paths).

**Tools**

Primetime by Synopsys, IC Compiler II -Synopsys

**Challenges**

- Understanding the primetime tool and commands related to the tool by analyzing their usage functionalities .
- understanding the timing reports at every stage of PD flow, finding the cause of timing violations and how some of the violented paths are being reduced in later stages.
- Analyzing the effect of clock Skew, CRPR,OCV timing derates for all four different timing paths from the timing reports.
- Identifying the violations based on timing exceptions such as false paths, multi cycle paths and specifying them in the SDC file.

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**B.E / B.Tech Academic Project**

TECHNO MAIN SALT LAKE

**AI Virtual Keyboard using Machine learning**

**Description**

With the virtual keyboard, we can write on the real time images by combining the thumb and index fingers on the letter we want. At the same time, we can simultaneously write what we type on the virtual keyboard in the note application.

**Tools**

The programming language used in this project is Python, and the library used are OpenCV, Numpy.

**Challenges**

- The gathering of data in the experiments is based on pre-recorded videos and not real-time ones. The experiments don't take into consideration complex situations such as the possibility of using two or more fingers, other factors that are impractical