VLSI DOMAIN SKILLS

- **HDL:** Verilog
- **HVL:** SystemVerilog
- **Verification Methodologies:** Constraint Random Coverage Driven Verification Assertion Based Verification - SVA
- **EDA Tool:** Mentor Graphics - Questasim and Intel Quartus Prime
- **Domain:** ASIC / FPGA front-end Design and Verification
- **Programming Languages:** C [Datatype | Array | Pointers | Memory Allocation | List | Queues and stacks | Data structure, Functions]
- **Operating System:** Linux,Windows
- **Core Skills:** RTL Coding Verilog, FSM based design, Simulation, CMOS Fundamentals, Code Coverage, Functional Coverage, Synthesis, Static Timing Analysis

DESIGN SKILLS

- **Digital Electronics**: Combinational & Sequential circuits, FSM, Memories, CMOS implementation
- **STA**: STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks, Clock domain and Variations, Clock Distribution Networks, Fixing timing failure
- **Verilog Programming**: Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks, looping & branching construct, System tasks & Functions, compiler directives, FSM coding
- **Advanced Verilog & Code Coverage**: Generate block, Continuous Procedural Assignments, Self-checking testbench, Automatic Tasks, Named Events and Stratified Event Queue, Code Coverage: statement and branch coverage, Condition & Expression Coverage, Toggle & FSM Coverage.

TANNEERU SAI BHARGAV

Design & Verification Engineer

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SAI BHARGAV TANNEERU

CAREER OBJECTIVE

I am a B.Tech Graduate from K L UNIVERSITY. I am looking for a challenging job that helps me to learn new skills, enhance my general and technical knowledge in turn fulfilling the goals of the organisation.

CERTIFIED TRAINING

Advanced VLSI Design and Verification Course

2022/06 – Present

Maven Silicon VLSI Design and Verification Centre, Bangalore

EDUCATION

BACHELOR OF TECHNOLOGY

K L UNIVERSITY

2018 – 2022

CGPA : 8.36

INTERMEDIATE

VIGNAN COOPERATIVE JUNIOR COLLEGE

2016 – 2018

Percentage : 95.1%

SSC

SAINT JOSEPH'S SCHOOL

2016

GPA : 9.3

VERIFICATION SKILLS

System Verilog HVL:

- Memories: Dynamic array, Queue, Associative array, Task & Function - Pass by reference
- Interface: Modport and clocking block
- Basic and advanced object-oriented programming: Handle assignments, Copying the object contents,Inheritance, Polymorphism, Static Properties and Methods, Virtual Classes and Parameterized Classes
- Constraint Randomization: Constraint overriding , Distribution and Conditional Constraints, Soft, Static and Inline constraints.
- Thread synchronization techniques: Events, Semaphores and Mailbox - built-in methods
- Functional coverage: Cover groups, Bins and Cross Coverage, CRCDV.

System Verilog Assertions:

Types of assertions, assertion building blocks, sequences. Clock definitions, implication and repetition operators, different sequence compositions, Inline and Binding Assertions, advanced SVA Features and Assertion Coverage.

UVM :

- UVM Objects & Components
- UVM Factory & overriding methods
- Stimulus Modelling
- UVM Phases
- UVM Configuration
- TLM
- UVM Sequence, virtual sequence & sequencer
- Introduction to RAL

TECHNICAL SKILLS

- Digital Electronics
- Python
- Verilog
- System Verilog
- UVM

PROJECTS

AMBA AXI3/AXI4 Protocol Verification in UVM Environment

Description:

- Created a UVM Test Bench for verification of AMBA AXI.
- The AMBA AXI protocol is targeted at high-performance, high- frequency system and includes a number of features that makes it suitable for a high-speed submicron interconnect.
- AMBA AXI protocol is verified for a single master and single slave for write and read operation.
- For master write, aligned, unaligned transactions were verified for various burst size and burst length with single address transaction.
- For read, burst and overlapping burst transfers were verified.

Router 1x3 - RTL Design and Verification

Description**:** The router accepts data packets on a single 8-bit port and routes them to one of the three output channels: channel 0, channel 1 and channel 2.

Responsibilities:

- Architected the block level structure for the design
- Implemented RTL using Verilog HDL.
- Architected the class based verification environment using SystemVerilog.
- Verified the RTL model using SystemVerilog.
- Generated functional and code coverage for the RTL verification sign-off
- Synthesized the design.

Design, Analysis and Simulation of Low Noise Amplifier for IRNSS Applications

Description: In this project a Low Noise Amplifier(LNA) is designed with the constraints which include Low Power, High Gain, Low Noise Figure, Linearity, Stability. It has the ability to amplify weak input signals with better noise performance and gives better output than the normal Low Noise Amplifier(LNA).

COLLEGE SKILLS

- C Language
- NI LABVIEW
- NI MULTISIM

LANGUAGES

- Telugu
- Hindi
- English

STRENGTHS

- Optimistic
- Energetic
- Detail-Oriented
- Flexibility
- Adaptability

HOBBIES

- Listening Music
- Reading Books
- Playing Games in Android Smartphone and PC

CERTIFICATIONS

- VLSI Design, Embedded IoT Programming
- VLSI-Advanced Design & Verification-System Verilog and UVM

INTERNSHIP

Internship In PCB Design at Hex n bit, with industrial partner Tevatron Technologies PVT LTD

DECLARATION

I hereby declare that all the information given above is true and correct to the best of my knowledge.

Date:
Place: Bangalore TANNEERU SAI BHARGAV