# SiliconChip Technologies

## Design Verification Course Details

### What is VLSI?

Very Large-Scale Integration (VLSI) is a Solid Career Choice and offers Job opportunities for Electronics background graduates pursuing core employment. In India and overseas, VLSI provides a variety of job roles featuring outstanding professional growth and salary incentives. It is all about the design of integrated circuits which is usually referred to as a chip design. For those who are interested in pursuing a career in VLSI semiconductor sector and keep wondering if VLSI is a good career, let's take a closer look at the occupation and growth prospects available.

### Career and Industry Scope of VLSI

There is lot of opportunities after completion of VLSI Program. Some of the job opportunities in this domain are RTL Design Engineer, Design Verification Engineer, Application Engineer, CAD Engineer, etc. With VLSI training, learners can give their career a new growth.

### How does VLSI work?

Very large-scale integration is the process of making a microcircuit by combining many MOS transistors onto one chip. It is a microcircuit chips widely adopted, enabling complex semiconductor and telecommunication technologies to be developed.

### What is Design Verification?

Design verification is a crucial step in the VLSI (Very Large Scale Integration) design process. It is the process of validating and verifying that the design implementation meets its specifications and functional requirements.

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In VLSI design, verification is essential to ensure that the circuit or system behaves as expected and does not contain any functional bugs. It is a complex process that involves a combination of different techniques and methodologies to ensure the correctness of the design.

The main objective of design verification is to ensure that the design meets the following requirements:

1.Functional correctness: The circuit or system should perform its intended function accurately and consistently.

2.Timing constraints: The circuit or system should meet the timing requirements specified in the design.

3.Power consumption: The circuit or system should consume power within the specified limits.

4.Noise immunity: The circuit or system should be immune to noise and other external factors.

5.Physical design: The circuit or system should meet the physical design requirements, such as layout, routing, and placement.

To achieve these requirements, different techniques and methodologies are used in VLSI design verification, such as simulation, formal verification, and hardware emulation. These techniques help in identifying and eliminating design bugs before the actual manufacturing of the circuit or system.

Overall, design verification is a critical step in VLSI design, as it helps in ensuring the functionality, reliability, and performance of the final product.

**Module 1:**

**Introduction to VLSI**

Application of VLSI

Design Process of VLSI

Scope of VLSI

Introduction to VLSI Design flow

**Module 2:**

**Digital Electronics**

Number Systems - Review
Logic Minimization
Combinational Circuit Design
Understanding of a Logic Gate
Designing with Mux, Demux, Decoders, Encoders
Sequential Elements - D Latch, D Flop
Design of Sequential Systems - Registers and Counters
Finite State Machine

**Module 3:**

**Introduction to HDL**

History of Hard ware design
Benefits of HDL
HDL basics
Data Types and Operators
**HDL Programming**
Procedural and Continuous Assignments
Control flow statements
Blocking v/s Non-Blocking
Tasks and Functions
FSM Coding
Synthesizable Design

**Module 4:**

**System Verilog**

Compile Directive
System Tasks
File Management
OOP in System Verilog
Verilog Event Scheduling
Interface and Clocking
Process Synchronization
Program Blocks and Parameter
Functional Coverage
System Verilog Assertions

**Module 5:**

**UVM**

UVM Architecture
UVC Sequence items and Sequences
Basic concepts
Messaging
Stimulus Generation
Virtual Sequences
Virtual Sequencer
Communication between components
Drivers
Sequencers
Monitors
Subscribers

**Module 6:**

**Transaction Level Modelling (TLM)**

Concepts and Terminology
Simple uni-directional interfaces (put, get, peek)
More complex connections (transport, analysis)
TLM FIFOs and analysis FIFOs
Hierarchical connections with export
Analysis

**Module 7:**

**Register Layer**

Register layer architecture and features
Front door and back door access
Mirroring and updating
Address maps
Register adapters
Integrating registers into the environment
Register sequences
Built-in register test sequences

**Module 8:**

System Verilog and UVM Based Verification IP Project