Kishan Singhania

Design Engineer

To obtain a challenging position in VLSI engineering that will utilize my skills and experience for the growth of the organization.

ksinghania_mtech20@thapar.edu | +91 8961501229 | Gurugram, India

WORK EXPERIENCE

Research & Development Intern
Stryker Corporation

07/2021 - 06/2022 *Gurugram, India*

American multinational medical technologies corporation based in Kalamazoo, Michigan.

Achievements/Tasks

- Conduct research and development activities related to ASIC design and verification, including exploring new design methodologies, tools, and technologies.
- Responsible for creating and maintaining project documentation, including specifications, design documents, and test plans.
- Designed and Verified a decoder used in System Board of a Defibrillator using RTL Coding and simulating its behavior.

Design Engineer
Stryker Corporation

07/2022 - Present *Gurugram,India*

American multinational medical technologies corporation based in Kalamazoo, Michigan.

Achievements/Tasks

- Worked and integrated various RTL subsystems.
- Worked and created test bench for Advanced Peripheral Bus using System Verilog.
- Troubleshooted various systems written in Verilog independently.

EDUCATION

Master's of Technology
Thapar Institute of Engineering and Technology

09/2021 - 06/2022 *Patiala, India, GPA- 8.46*

Courses

- FPGA Design
- System Verilog
- Digital VLSI Design
- Embedded Systems
- Physical Design
- Device Physics
- Analog Electronics

Bachelor's of Technology
Calcutta Institute of Engineering and Management

08/2015 - 07/2019 *Kolkata, India, GPA- 7.82*

Courses

- Electrical Engineering

SKILLS

C Programming | Verilog | System Verilog | Python | Digital Design

PERSONAL PROJECTS

Designing Arithmetic Logic Unit using Verilog

- Implemented and verified various blocks of ALU using Verilog in Xilinx ISE Tool.
- Integrated all the sub-blocks using Verilog.
- Created testbench and verified the behavior of ALU through simulation.

Designing Moore and Mealy FSM Machine using Verilog

- Conducted research of FSM and implemented using Verilog.
- Debugged and verified FSM block through simulation.

RTL to GDSII Implementation of RISC V Processor using Open Source Tools

- Gained knowledge of RISC V Processor and its working.
- Gained knowledge of ASIC Design Flow.
- Solved various slacks issue between the two Flip Flops.

LANGUAGES

English
Full Professional Proficiency

Hindi
Native or Bilingual Proficiency

INTERESTS

Researching more on new VLSI Technologies

Watching Travel VLogs