Rajpurohit Rakesh

DESIGN AND VERIFICATION ENGINEER

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PROFILE SUMMARY

A fresher in the field of engineering seeking a full-time position in my field, where I can apply my knowledge and skills for continuous improvement with learning new concepts, ideas and develop innovative solutions to problems.

PROFESSIONAL TRAINING

MAVEN SILICON, CENTRE OF EXCELLENGE IN VLSI DESIGN | SEP2021-PRESENT

- Advanced VLSI Design and Verification Course

ACADEMIC CREDENTIALS

BACHELOR OF TECHNOLOGY | 2018-2021

Electronics and communication
Chirala Engineering College, A.P. | CGPA- 7.0

POLYTECHNIC | 2015-2018

Electronics and communication
Diviseema Polytechnic College | 80%

SSC | 2015

Government High School, A. P | CGPA-7.3

VLSI DOMAIN SKILLS

HDL: Verilog
HVL: System Verilog
Verification Methodologies: Constraint Random Coverage Driven Verification Assertion Based Verification - SVA
TB Methodology: UVM
Protocols: AXI, AHB, UART, I2C, SPI
EDA Tool: Mentor Graphics - Questasim and Xilinx - ISE, Xilinx - Vivado
Domain: ASIC/FPGA front-end Design and Verification
Programming Languages: C, Python, (Good knowledge of OOPs concept, Class, Inheritance, Polymorphism)
Operating System: Linux
Core Skills: RTL Coding using Synthesizable constructs of Verilog, FSM based design, simulation, Code Coverage, Functional Coverage, Synthesis, Static Timing Analysis, Assertion Based Verification using System Verilog Assertions.

VLSI DESIGN SKILLS

Digital Electronics: Combinational & Sequential circuits, FSM, Memories, CMOS implementation, Stick diagram.
STA: STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clocks Clock domain and Variations, Clock Distribution Networks, Fixing timing failure
Verilog Programming: Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks, looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Synthesis issues, Races in simulation, pipelining RTL & TB Coding,
Advanced Verilog & Code Coverage: Generate block, Continuous Procedural Assignments, Self-checking testbench, Automatic Tasks
Named Events and Stratified Event Queue, Code Coverage: Statement and branch coverage, Condition & Expression Coverage, Toggle & FSM Coverage

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DFT SKILLS

- ATPG, Test Coverage
- JTAG, BSDL, IJTAG
- Memory and Logic BIST
- Synthesis scan stitching
- Memory BIST implementation
- Scan/Jtag/boundary-scan insertion and ATPG pattern generation
- Test coverage and fault coverage analysis
- Knowledge/experience with ATPG / DFT tools: Tessent, System Verilog, RT

PROJECT

Project in Maven Training:
Router 1x3 – RTL design.
HDL: Verilog.
EDA Tools: Questasim and ISE.
Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1, and channel2.
Responsibilities:

- Architected the block level structure for the design
- Implemented RTL using Verilog HDL.
- Synthesized the design.

Project in BTech
Design and Implementation of Automatic door unlockingsystem using GSM and Arduino.
Components: Arduino, GSM & Keypad module, Motor driver, Buzzer.
Programming Language: C
Description: This system can monitor the users by using IOT and informs if there are any symptoms of covid-19 then this identifier will update us regarding some precautions to be taken care of.

STRENGTHS, HOBBIES & PERSONAL DETAILS

Strengths:

- Smart working
- Quick Learning
- Good Communication Skills
- Adaptive

Hobbies:

- Listening Music
- Watching Movies
- Helping people

Personal Details:
Date of birth : 25th May 1998
Languages : English, Hindi, Telugu

DECLARATION

I do hereby submit that all the information provided is true and correct to the best of my knowledge.

Place: Andhra Pradesh **Rajpurohit Rakesh**