BASAVARAJ

DESIGN AND VERIFICATION ENGINEER

CONTACT

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PERSONAL STRENGTHS

- Hard Working
- Good at Team Work
- People's person
- Timekeeper
- Self-learner and Adaptability

LANGUAGES KNOWN

- English - Professional Proficiency
- Kannada - Native Proficiency
- Hindi - Professional Proficiency
- Telugu - Limited Proficiency

HOBBIES

- Sports
- Volunteering
- Listening Music
- Travelling

1 CAREER OBJECTIVE

Seeking a position with an organization in the field of VLSI, where I can contribute my skills for organization's success and synchronize with new technology, while being resourceful, innovative and flexible.

2 PROFESSIONAL TRAINING

Advanced VLSI Design and Verification

>> Maven-Silicon VLSI Training Institute, Bengaluru.

[August 2022 - Present]

3 EDUCATION

Bachelor of Technology[B-Tech.] **[2019 - 2022]**

JAIN[Deemed-to-be University]

Electronics and Communication Engineering **CGPA - 8.4**

Diploma **[2016 - 2019]**

Nettur Technical Training Foundation[NTTF]

Diploma in Electronics **CGPA - 8.9**

SSLC **[2015 - 2016]**

Karnataka Secondary Education Examination Board

SSRHSS - Sree Siddaganga Math **Percentage - 63.52%**

EDA TOOLS

- Questasim
- Quartus Prime
- Modelsim
- Xilinx ISE
- DSCH
- Kiel uVision
- Arduino IDE
- EAGLE
- Proteus

DESIGN SKILLS

- Digital Electronics
- Verilog
- Advanced Verilog
- Code Coverage
- Static-Timing-Analysis[STA]

VERIFICATION SKILLS

- **System Verilog:**

Memories, Interface, Basics and advanced OOP's Constraint, Randomization, Thread Sync-Techniques .

- **Functional Coverage**
- **System Verilog Assertions**
- **UVM:**

UVM Objects & Components, UVM Factory and overriding methods, Stimulus Modelling, UVM Phases, UVM Configuration, TLM, UVM Sequence, virtual sequence, sequencer, introduction to RAL.

WORKSHOPS

- System-on-Chip [SoC] conducted by Jain[Deemed-to-be University].

4 TECHNICAL SKILLS

- HDL : Verilog, Advanced Verilog.
- HVL : System Verilog.
- TB Methodology : UVM.
- Protocols : UART, I2C, SPI.
- Programming Languages : C, Embedded C, Python.
- OS Platforms : Linux, Windows.
- Other Skills : CMOS VLSI Design, FPGA.
- Hardware Expertise : Spartan 6 FPGA Board[VLSI based System Design, 8051 [Embedded based System Design].

5 PROJECTS

1. Router 1x3 – RTL Design and Verification

HDL : Verilog
HVL : System Verilog
TB Methodology : UVM
EDA Tools : Questasim and Quartus prime

Description : The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel_0, channel_1 and channel_2.

Responsibilities :
i. Architected the block level structure for the design.
ii. Implemented RTL using Verilog HDL.
iii. Architected the Class based verification environment using System Verilog.
iv. Verified the RTL model using System Verilog.
v. Generated functional and code coverage for the RTL verification sign-off. Synthesized
the design.

2. WSN based Crop Recommender

Technologies Used : Embedded C, Python, STM32, Raspberry Pi, Ubuntu, Kotlin, Android Studio, MySQL, STM32 Cube IDE.

Description : A system that can recommend crops to farmers, based on their field parameters and display the data on an Android application. The cloud for this system was built using python and MySQL on Ubuntu VM.

ACHIEVEMENTS

- 2nd Best Project Award for 2021-2022 Academic Year, Department of Electronics and Communication Engineering, Jain[Deemed-to-be University].

6 PAPER PUBLICATION

- Presented paper with titled, "WSN based Crop Recommender", in Jnana Chilume 2022 organised by JAIN(Deemed-to-be University) on June-2022 – "ISBN-9789391131043".

7 EXTRA - CURRICULAR ACTIVITIES

- Presented in IEEE-BIT Mini Project Competition-2021 organized by IEEE Student Branch Bangalore on July 2021 and Presented on Medha (Online Test-Portal).

- Presented and Executed a project on "E-Waste Monitoring System" in Inter Zonal Quality Control Competition, organized by NTTF-NEC Bangalore.

8 CERTIFICATION

- System Design Through VERILOG from NPTEL - IIT -GUWAHATI.
- Learning Verilog for FPGA – LinkedIn Learning
- System Verilog – Udemy
- Python – LinkedIn Learning

9 DECLARATION

I, Basavaraj, hereby solemnly declare that all the information furnished in this resume is true to the best of my knowledge and belief.

Date :
Place : Bengaluru **[Basavaraj]**