Krishna Devagirikar

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Gadag-582103, Karnataka

Career Objective

Seeking for a Physical Design Engineer job to pursue a better career and healthy work environment where I can utilize my skills and knowledge efficiently for the organizational growth.

Core Competancy

- Expertise in Synopsys Prime Time and IC Compiler II
- Hands-on experience in Automatic Place and Route in 40nm technology with efficient floor planning.
- Hands-on experience in Manual placement of macros based on data flow lines.
- Analyzing IR drop map and fixing the floorplan to solve the IR drop issues by changing the powerplan in the design.
- Analyzing Routing congestion map report and solving it by changing a floorplan.
- Interpreting timing constraint reports and analyzing Setup and Hold violations and fixing the timing constraint.
- Knowledge of Static Timing Analysis concepts such as timing arcs, timing paths, PVT variations and PVT corners.
- Knowledge of Physical Design concepts such as Placement, Clock Tree Synthesis (CTS), Antenna errors.
- Analyzing QoR reports, DRC and LVS errors and fixing the errors.
- Knowledge of tcl scripting, interpreting the tcl scripts, perl scripting and Linux operating system.

Education Details

Advanced Diploma in ASIC Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electrical and Electronics** **2020**

Smt. Kamala and Sri Venkappa M. Agadi college of Engineering and Technolgy, Laxmeshwar, with 7.1 CGPA

2016

Govt. PU college, Gadag, with 70.3 %

SSLC **2014**

St. John's High school, Betageri - Gadag, with 85.44 %

Projects worked on

Pixel Controls Client: Hitachi Energy India Ltd.

PGGA testing engineer Jul-2021 to Aug-2022

Power Grid and Grid Automation

Description

Contributed by configuring and testing the IED's (Intelligent Electronic Devices) functionality and performance according to the client's specifications and integrating of IED's to the SCADA system.

Tools

MicroSCADA, PCM600

Challenges

- Testing of IED's function and performances according to the client's specifications
- Integrating IED's with the SCADA
- Configuration and Fault timing calculation

Domain Specific Project

RV-VLSI

Graduate Trainee Engineer Oct-2022 to Jan-2023

Lakshya

Description

Lakshya is a block-level design implemented in 40nm technology with around 31k cells and the frequency of operation is 833MHz.

Tools

Synopsys IC Compiler II

Challenges

- Finding efficient Floor plan, Manual macros placement, Power planning without any DRC violations and IR drop map analysis to fix the IR drop by changing the power plan.
- Using the routing congestion map to solve the congestion by manually changing the spacing of macro cells and placing the routing blockage to avoid standard cells placement.
- Analyzing timing reports, fixing the setup and hold violations, Clock Tree Synthesis (CTS).
- Antenna violations and solving the antenna errors.

B.E / B.Tech Academic Project

Smt. Kamala and Sri Venkappa M. Agadi college of Engineering and Technolgy, Laxmeshwar

Protection and Data acquisition of 3 phase asynchronous motor

Description

Project uses an IoT (Internet of Things) technology to collect a data of asynchronous motor and monitor the machine's health while performing a task and also to protect the machine from abnormal conditions and provides data of machine over internet.

Tools

Hardwares: Arduino ATmega328P Microcontroller, Digital voltage and current measuring meters, Thermal sensor, 16x2 LCD screen, Wi-Fi adapter Software: Arduino IDE

Challenges

- Establishing connection between an analog machine and the internet, Programming of Arduino ATmega328P