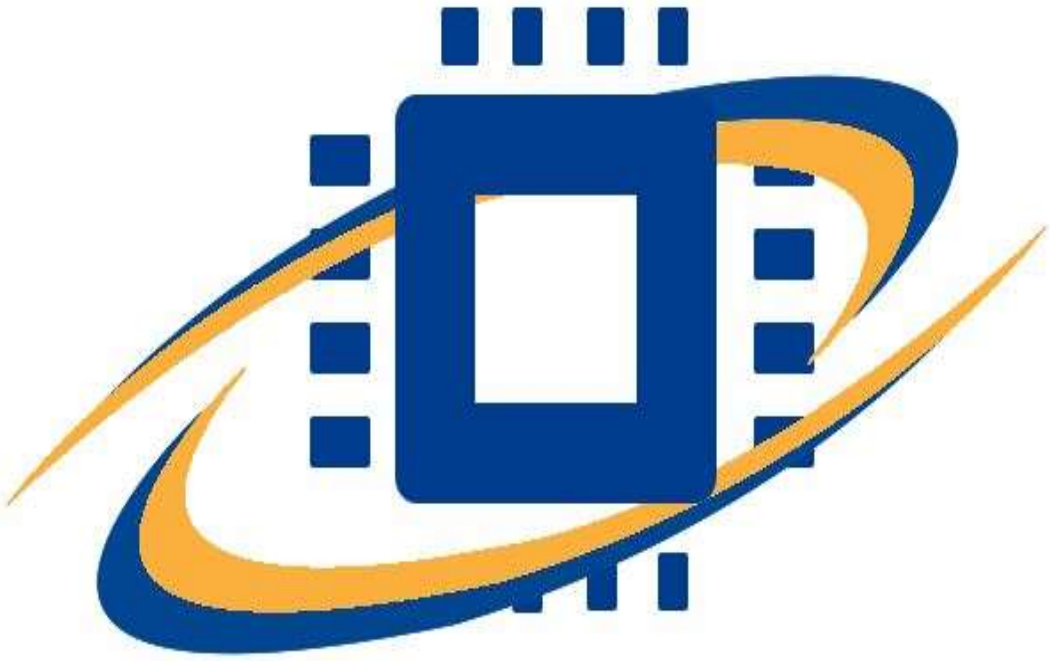
SiliconChip Technologies



Physical Design Internship

PHYSICAL DESIGN INTERNSHIP PROGRAM

Why Internship?

An internship is a period of work experience offered by an organization for a limited period of time. It is aimed at providing practical experience to the candidates when they implement their classroom learning in real-time work situations. It helps them learn the ways to understand and perform the desired duties and responsibilities in a particular role effectively. An internship is an amalgamation of theory and practice. Student interns equip themselves with practical skills in office settings. Internships also offer the benefit of creating professional recommendations, practical experience for your resume, and building networking opportunities.

What is VLSI?

Very Large-Scale Integration (VLSI) is a Solid Career Choice and offers Job opportunities for ECE fresher's pursuing core employment. In India and overseas, VLSI provides a variety of job roles featuring outstanding professional growth and salary incentives. It is all about the design of integrated circuits which is usually referred to as a chip design. For those who are interested in pursuing a career in VLSI semiconductor sector and keep wondering if VLSI a good career, let's take a closer look at the occupation and growth prospects available.

Career and Industry Scope of VLSI

There is lot of opportunities after completion of VLSI Program. Some of the job opportunities in this domain are Verification Engineer, Design Engineer, Application Engineer, CAD Engineer, etc. With VLSI training, learners can give their career a new growth.

How does VLSI work?

Very large-scale integration is the process of making a microcircuit by combining many MOS transistors onto one chip. It is a microcircuit chips widely adopted, enabling complex semiconductor and telecommunication technologies to be developed.

What is Physical Design?

- Physical design is the process of turning a design into manufacturable geometries. It comprises a number of steps, including floor planning, placement, clock tree synthesis, and routing.
- Physical design begins with a netlist, which is synthesized from RTL. The netlist describes the components of a circuit and how they connect.
- Floor planning is the first major step. It involves identifying which structures should be placed near others, taking into account area restrictions, speed, and the various constraints required by components.

About Physical Design Internship Program:

- VLSI Physical Design course, specially designed for fresh graduates to get comprehensive training to start a career in VLSI industry as a Physical Design Engineer. The course covers the latest industry requirements and is covered by trainer's experiences in Physical Design.
- The Course begins with introduction to Linux, Fundamentals to CMOS and Digital Electronic, Digital design using Verilog.

Key Features:

- The Physical Design Course comprehensively covers synthesis, Logical Equivalence Check (LEC), Physical Design Flow including Floor plan, Power plan, Clock Tree
- Synthesis & Routing, Static Timing Analysis, Physical Verification and VLSI Physical Design Automation.
- Four Projects will be covered during the course using 14nm/28nm library. Labs are on Industry standard tools synopsis like ICC2, Formality, StarRC, Prime Time and IC Validator.

Eligibility for Attending this Internship

- Internship applications are open for undergraduates (6th/7th/8th Semester), graduates, and postgraduates of the below mentioned streams. BE/BTech in EEE/ECE/TE/CSE/TT/Instrumentation/ ME/MTech/MS in Electronics/MSc Electronics
- Post – Graduate Freshers (MTech) with Specialization like VLSI/ Embedded/ Power Electronics/ Digital Communications/ Instrumentation etc.

Curriculum

- **Module 1: Essential of Linux**
  - Introduction to Linux
  - Command Line Operators
  - File Operations
  - Process
  - Text Editors
  - Text Manipulation
  - Network Operations
  - Special Keystrokes
  - Assessment And Quizzes
- **Module 2: Digital Design**
  - Number System, Boolean Algebra, SOP and POS, K-Map
  - Combinational Circuit
  - Sequential Circuits
  - Finite State machines
  - Frequency Division
  - Setup and Hold time checks
  - Advance Design Issues: Metastability, Noise Margins, Power, Fan-out
  - Timing Consideration

- **Module 3: CMOS Devices and Technology**
    - Electronic Devices, Power Sources, Thevenin and Norton Theorem
    - Semiconductors Device Physics: Atomic Structure, Electronic
    - Configuration, Doping, Diode – Biasing and VI Characteristics
    - MOSFET: Region of operation, VL Characteristics
    - Function implementation using CMOS
    - Stick Diagram and Layout
    - Second order effect: Body Effect, Channel length modulation, Punch through, sub threshold conduction, DIBL
    - Process Technology: Clean Room, Wafer manufacturing, Oxidation, Diffusion, Ion implementation, Lithography

- **Module4: Verilog HDL**
    - Introduction of Verilog
    - Applications of Verilog HDL
    - Verilog HDL language Concepts
    - Data Types, Nets and registers, Arrays
    - Verilog Operators: Logical operators, Bitwise and Reduction operators, concatenation and conditional operators, Relational and arithmetic, Shift and Equity operators.
    - Types of Assignments: Continuous assignments, Inter/Intra assignments, Blocking and Non- blocking assignments, Execution branching, Task and Function
    - Finite State Machine (FSM): Basic FSM Structure, Moore Vs Mealy, Common FSM Coding styles, Registered outputs

- **Module 5: Synthesis**
    - ASIC Design flow and role of Synthesis
    - Synthesis flow
    - Writing timing constraints in SDC format
    - Constraining the design for timing
    - Power, area goals, set optimization techniques
    - Synthesize the design
    - Generate the analyse the reports, save the netlist and SDC
- **Module 6: Logic Equivalence Checking (LEC)**
    - Formal Verification
    - Understanding & Matching compare points
    - Debugging non-equivalent points
- **Module 7: TCL Scripting**
    - Features of TCL and Applications. TCL commands, Variable, arithmetic expressions, comments, identifiers, reserved wors, data type, decision, loops, arrays, strings, file, I/O and Procedures.
- **Module 8: Introduction of Physical Design, Data presentation and Sanity Check**
    - Introduction to Physical designed Physical Design Flow, Data Preparation : File required for PD (Netlist, SDC, Libraries, Technology files, TLU+)
- **Module 9: Floorplan**
    - Goals of floor planning, different aspects of floor planning, Rectangle /Rectilinear floor plans, Die Size estimation (Core Utilization, Aspect ratio), IO Placements, macro placement and guidelines.
- **Module 10: Power Routing**
    - Goals of power Routing, Power distribution structure (Ring, straps and follow-pin/std cell rail), Metal stack information, power planning methodology, IR drop analysis, types of power consumption

- **Module 11: Placement**
    - Goals of placement, types of placements, pre-place (End-cap, Tap & I/O buffer) cells, Placements optimization, congestion analysis, timing analysis, Tie-cells
    - High-Fan-out net synthesis, Scan chain re-order, path grouping and creating Bounds
- **Module 12: Timing Analysis (Pre-Layout) & Optimization**
    - STA overview and concepts, basic timing checks (setup, hold), Understanding timing constraint (SDC) , timing corner, timing reports analysis
    - General optimization techniques, typical cause of timing violations and strategies for fixing the same, pre-CTS optimization to Fix Setup Violations
- **Module 13: Clock Tree Synthesis (CTS)**
    - Goals of CTS, Types of Clock-tree, constraints for CTS, building clock tree, Analyse the result
    - Post-CTS optimization: Fixing setup and Hold Violations.
- **Module 14: Routing**
    - Goals of Routing, stage of routing: Global Routing, Track assignment and Detail Routing, Routing options, Fixing of routing violations (DRC, LVS), post route optimization, issues in routing and guidelines for optimum routing results.
- **Module 15: Post Layout STA**
    - Post Layout STA using SPEF, Multi moose multi corner STA, Derating factors, PVT, OCV variations
- **Module 16: ECO Flow:**
    - What is ECO, Types of ECO, Timing and Functional ECO, Performing the ECO placement and routing
- **Module 17: Sign-off Checks**
    - Physical Verification (DRC, LVS), IR drop analysis, Electro-Migration Analysis

Projects:

- Project will be given converging Netlist to GDS II flow. Various projects that will allow the students to understand the intricacies of implementation foe the minimum area, low power, high performance.
- The method of execution will be similar to typical block level physical design work/projects in the industry

Course Delivery Model:

- Live Offline Class
- Each topic is followed by hands-on lab sessions with VLSI tools (Synopsys Tools).
- Soft Skill training.
- Mentoring sessions from Industry Experts
- Weekly mock interview assessments test

VLSI Tools and Lab

- **Synopsys Tools:**
    - Digital Design with Verilog: VCS.
    - Synthesis – Design Compiler Topographical
    - Static Timing Analysis (STA): Prime Time SI.
    - Physical Design: IC Compiler 2 (ICC2)
    - RC Extraction: Star RC
    - Physical Verification: IC Validator
    - Technology Libraries to be used: 14nm FINFET Libraries

Lab Timings

- **Timings:** 3 Hours (5 days a week – week days)

Key Features:

- Internship is offered in offline at office premises.
- 10+ years experienced Mentors.
- **Tool access:** Tool access will be given through VPN.

Duration: 12-15 weeks (4 - 5months

Training Contents:

The internship is split in to two phases: Basic Course + Advanced Course

Basics course:

- Advanced Digital electronics
- ASIC flow
- Physical design basics, keywords
- Linux OS
- TCL scripting
- BJT, CMOS, Fin FET and Semiconductor fundamentals

Advanced course

- Physical Design flow starting from Synthesis to Physical verification & 2 hands-on projects at 14nm and 28nm
- The course also includes dedicated sessions with students working on complete projects hands-on flow.

Course Outcome:

- Expertise with Industry Standard Projects, gives expertise on par of 2 years experienced engineer.
- **Tools:** Synopsys DC Compiler, Synopsys ICC II, Primetime.

Employment support:

- Once the student completes his internship work, evaluating his/her performance, the technical guidance will be provided till student gets a job.
- Regular mock interviews, evaluation tests and group discussion for interview preparation.

Other Details:

- Project will be given converging Netlist to GDS II flow. Various projects that will allow the students to understand the intricacies of implementation for the minimum area, low power, high performance.
- The method of execution will be similar to typical block level physical design work/projects in the industry
- Block level input database will be given and the participants have to deliver GDS II, after clearing all the issues during sign-off checks.

Note:

- **Fees:** 75,000 + GST = 88,500 INR
- **Note:** Instalment facility is available