SiliconChip Technologies Training Institute

Bangalore and Kalaburagi

Workshop Agenda

Day-1

Session 1

- Introduction to VLSI
- Why VLSI
- About Semiconductor Industry
- Growth of Semiconductor
- About SiliconChip Technologies
- Why SiliconChip Technologies ….?
- Career Growth
- Placement Details
- Discussion(Q&A)

Session 2

- Environment Setup and starting Cadence Virtuoso
- Starting Virtuoso layout editor
- Invertor Cell Layout and Schematic Design
- DRC and LVD Verification
- Parasitic Extraction and Post Layout Simulation

Workshop Agenda

Day-2

Session 3

Hands-on Cadence Virtuoso Tool

1. Create Library

A. Create a Invertor cell view

B. Draw a schematic

2. Schematic

3. Run Spectre simulation

4. Layout

5. Run Verification tool DRC and LVS

Session 4

1. Nand Gate Schematic and Layout

A. Create a Nand cell view

B. Draw a schematic

2. Schematic

3. Run Spectre simulation

4. Layout

5. Run Verification tool DRC and LVS