LALITHESH.D

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Career Objective:

Seeking a challenging position as a ASIC backend Engineer, where my skills and experience will greatly enhance the company's progress and my personal growth

Academic Details:

- **B.E** in **Electronics and Communication Engineering** from East West Institute of Technology, Bangalore with 6.00 CGPA in AUG 2020
- **Intermediate** in **PCME** from St. Claret Pre-University Collage, Bangalore with 65.33% in April 2015
- **SSLC** from Apollo High School, Bangalore with 70.00% in March 2013

Technical Skills:

- Complete understanding of ASIC flow and the stages involved in physical design flow such as **Netlist to GDSII**
- Hands on experience with Industry standard EDA tools like **Synopsys IC compiler (ICC/ICC2), DC Compiler**, **Primetime & StarRC**.
- Worked on block level of all aspects of Physical Design and verification including **Synthesis, Floor Planning, PG Planning, IR Drop analysis, Congestion free Placement, Clock Tree Synthesis, Timing Closure, Routing, DRC/LVS.**
- Understanding of reliability issues like Latch up, ESD, Antenna effect & EM
- Essential knowledge of **STA** & experience of fixing timing violations for Setup and Hold analysis under **OCV, MCMM & CRPR**
- Interpreting Timing reports and understanding all timing paths
- Working Knowledge of Linux/Unix operating system and **Tcl** to run physical design flow using Synopsys tools.
- Having a knowledge of CMOS concepts, Digital Electronics & semiconductors

Industrial Experience: - Physical design

Organization: Takshila institute of vlsi

Training Tools Used: IC complier and primetime

Description: Designing of ASIC block using Synopsys ICC for 32nm technology with macro count 40, std cell 56013, supply 0.75V, clock frequency 416 MHz and 9 metal layers and number of clocks 8. Complete physical design flow is carried out from netlist to Routing which includes floorplan, power plan, placement, CTS, Routing, DRC checks and GDSII report.

Challenges Faced:

- Placing of High-count macros in Floor plan stage.
- Placing of Soft, Hard & Partial Placement Blockages.
- Understanding the timing exception violations like False & Multi-cycle paths.
- Analyzing useful skew to optimize timing paths in CTS.
- Understand how the Cross-talk effects on timing paths & lead to violations.
- Fixing Setup, Hold & Maximum Transition violations.

Academic Project:

- **Title:** Automatic Detection and Notification of Potholes & Humps on Roads Using IOT.
- **Role:** Team leader
- **Software:** Arduino ide

One of the prime reasons for vehicular accidents is due to undetected Potholes and road Humps. Potholes force vehicle to slow down in place where the speed of vehicle may be expected to be higher, drivers do not expect to slow down and end up crashing into the other vehicle. Some Potholes go unattended for several weeks and get deeper with time, So much vehicular damage increases by just passing over the Pothole. Several lives are lost each year due to pavement distress, and it is high time for a cost-efficient solution to this problem so that it can be implemented This project Provides a prototype IOT based Pothole and hump detection system than can integrated with vehicle and hump detection system than can integrated with vehicle and provide timely information to maintenance authorities so that necessary steps can be taken for safety of drivers.

Personal Details:

Date of birth	: 23th AUG 1997
Languages Known	: Kannada, English, Telugu, Tamil and Hindi
Permanent Address	: NO 21-2nd main, Sanjeevini Nagar, Hegganahalli Cross, Bangalore-560091.

Declaration:

I hereby declare that the above stated details are correct to the best of my knowledge and belief

Date: (Signature)
Place: Bangalore