Chandrakanth Reddy Muddigari
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Career Objective

To excel as a Physical Design Engineer with hands on experience in nm technology and further contributing to the organization growth.

Core Competency

- Acquired in-depth knowledge of ASIC PD flow from floorplan to GDSII along with various inputs at each stage.
- Worked on floorplan with high utilization and ensuring good contiguous core area for standard cells.
- Implemented power plan to connect power pins of all macros and standard cells to the supply voltage with out any PG DRC violations and achieved specified IR drop limit..
- Worked on placement plan with power aware and zero congestion, ensuring good routability.
- Analyzed the Timing Reports, understood the cause of timing violations and possible solutions that could fix them.
- Analyzed and understood the design constraints to specify OCV, PVT Corners, false paths, halfcycle paths, CRPR.
- Hands on experience in industry standard EDA tools – Synopsys IC Compiler II and Prime Time.
- Good knowledge in Logic Design, CMOS and Basic Electronic Devices.

Professional Experience:

Worked as a **Physical Design Engineer** for **1 Year** in **Tech Mahindra Cerium Systems Pvt Ltd**

Education Details:

Course	Year Of Pass	Institution	Board/University	Result
PD Trained	2022	RV VLSI Banglore	RV VLSI	----
B.Tech	2021	REVA UNIVERSITY	Reva University	8 CGPA
Intermediate	2017	Narayana Junior College,Nellore	Board Of Intermediate Education	97%
S.S.C	2015	Narayana School Pulivendula	Board Of Secondary Education	9.3 CGPA

Domain Specific Project

RV- VLSI Design Center

Graduate Trainee Engineer Apr 2022

Designing of an ASIC block in 40nm Technlogy

Description

Technology-40nm, Macro Count- 34, Standard Cell Count- 41,946, Supply voltage-1.1V, Power Budget- 600mW, IR Drop budget- 55mV, Area- 4.2 sq. mm Clock Frequency- 1GHz, Metal layers- 7.

Tools

Synopsys IC Compiler II

Challenges

- Understanding the design setup, Tcl scripts and designing floorplan with macros according to the data flow diagram.
- ensuring that no floating pins or nets after power network.
- Getting congestion under control during placement along with an acceptable utilization.
- Efficient clock tree synthesis using NDR rules and optimization of clock and data path to fix the timing violations by balancing the skew.

B.E / B.Tech Academic Project

REVA UNIVERSITY

1.Devolopment of RF based Secure Coded Communication System

Project on radio frequency based communication system using Arduino Uno and Zigbee.

Tools

Arduino uno, Zigbee.

2.Devoloped a Humidity and temperature sensing device

Objective is to Sense humidity and temperature in any place using Arduino

STRENGTHS :

❖ Flexible to learn new skills

❖ Interested to learn new things and new technology

❖ Take Initiative and be independent when required.

❖ I have a ability to learn the things quicker

❖ Problem solving skills

DECLARATION:

I hereby declare that the information given above is true to the best of my knowledge.

Date : 01/03/2023 (Signature)

Place : Banglore M.Chandrakanth Reddy