Name : HARI SATYA PRASAD KANDREGULA
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www.se-minds.com

OBJECTIVE

Seeking a responsible position as an entry level Physical Design Engineer which enables to bring the best out of my knowledge and experience in achieving organizational goals and personal growth.

PROFESSIONAL TRAINING

An Industry Oriented Trainee in **VLSI ASIC PHYSICAL DESIGN** from **Se-minds Pvt. Ltd.,** Hyderabad from **August 2022 to January 2023.**

COURSE OUTLINE

Basic Electronics, Digital fundamental concepts, MOSFET, CMOS design concepts, layout concepts, stick diagrams, fabrication, Basics of STA, Logic Synthesis fundamentals. Physical Design concepts: floor planning, PG planning, Low Power design techniques, CTS, Routing techniques, signal integrity. Advanced STA, vi editors, Basics of Unix.

Tools:

Experience in physical design of 90nm and 45nm technologies using Cadence tool

- Cadence Innovus : Place & Route
- Cadence Genus : Logic Synthesis

PROJECTS:

Project -1: Place and Route (Top level)

Design Name : asic_entity
Objective : Timing Driven layout.
Tools Used : Cadence Innovus
Area : 31672192.5 μm^2
Macros/Instances : 29/53797
No. of Clocks : 08
Frequency : 125Mhz
Technology/Layers : 90nm/9 Metal Layers
Role **:** Performing Audit checks, Floor plan, Placement, Trail route, Timing Analysis, CTS, Detailed Routing, Post Route Optimization, Sign Off Checks, Achieved 0% Congestion at Trail Route Stage.

Project -2: Place and Route (Block level)

Design Name : eVITERBI_322
Objective : To Observe I/O Pins Placement and Fixing DRV's & DRC's
Tools Used : Cadence Innovus
Area : 435.024 μm^2
Macros/Instances : 0/113
No. of Clocks : 01
Frequency : 250Mhz
Technology/Layers : 45nm/7 Metal Layers
Role **:** Performing Audit checks, performing normal PNR flow and done with foundation flow, Floor plan, Placement, Trail route, Timing Analysis, CTS, Detailed Routing, Post Route Optimization.

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Project -3: Place and Route (Block level)

Design Name : usb_wrapper
Objective : To Meet Setup & Hold time, Fixing DRV's & DRC's
Tools Used : Cadence Innovus
Area : 1741021.4826 μm^2
Macros/Instances : 12/28104
No. of Clocks : 17
Frequency : 208.33Mhz
Technology/Layers : 90nm/5 Metal Layers
Role **:** Performing Audit checks, performing normal PNR flow and done with foundation flow, Design Import, Floor plan, Placement, Trail route, Congestion Analysis, Timing Analysis, CTS, Detailed Routing, Post Route Optimization, Fixing Shorts & Opens.

Project -4 : Logic Synthesis

Objective : Perform ZWLM Synthesis & Obtained optimized Gate Level Netlist.
Tools Used : Cadence Genus
Instances/Area : 4131/237011.129 μm^2
No. of Clocks : 07
Frequency : 500Mhz
Technology/Layers : 45nm/11 Metal Layers
Role **:** Check SDC and error correction, generating reports for Area, Timing and Power, different efforts for optimization (Generic, Mapping, Optimization), timing analysis and fixing.

ACADEMIC EDUCATION:

- B.Tech in Electronics and Communication engineering from (2017-2020) in Swarnandhra College Of Engineering & Technology Autonomous,Narsapuram with 7.51 CGPA.
- Diploma:State Board of Technical Education and Training from (2014-2017) in Smt. B.Seetha Polytechnic college,Bhimavaram with 78.26 **%** aggregate.
- SSC from Board of Secondary Education in Adithya Vidhya Nilayam School (visweswarayapuram) with 7.5 CGPA.

PERSONAL STRENGTHS

- I can easily adopt to any technology.
- I have good logical knowledge towards problem solving.

Declaration:

I hereby declare that the above-mentioned information is correct to the best of my Knowledge.

(HARI SATYA PRASAD KANDREGULA)