CHETANA MOTHUKURI

Email ID: chetanamothukuri@gmail.com

LinkedIn URL: https://www.linkedin.com/in/chetana-mothukuri/

Contact No: 9154020213

ABOUT ME:

- Extremely **motivated** to constantly develop my skills and grow professionally.
- To **learn** and to **apply** it through my actions is what makes me happy.
- To earn **your respect** and to meet **your expectations** is what I am willing to strive for.

EDUCATION:

- Master of Technology, Digital Systems and Computer Electronics, JNTUCEH (Kukatpally) [2020-2022] - 7.5 CGPA.
- Bachelor of Engineering, Electronics and Communication Engineering, University College of Engineering, Osmania University, Hyderabad [2015 – 2019] - 7.75 CGPA.
- Intermediate (MPC) Sri Chaitanya Junior Kalasala, Hyderabad [2015] - 96 %.
- High School (SSC) Sri Chaitanya Techno School, Kodad [2013] - 9.5 CGPA.

TECHNICAL SKILLS:

- **HDL** **:** Verilog
- **Scripting Languages :** TCL, TCSH
- **Subject Expertise** **:** Digital Electronics
- **Operating System** **:** Linux, Windows
- **Domain** **:** Physical Design
- **EDA Tools** **:** Mentor Graphics Model Sim, Xilinx Vivado, Synopsys Design Compiler, ICC2.
- Worked on RTL Synthesis, Physical Design flow stages like Floor Planning, Placement and Routing (PnR), CTS.

CORE SKILLS:

- CMOS Fundamentals.
- Static Timing Analysis (Basics).

PROFESSIONAL TRAINING

- 6 months VLSI Physical Design training at Sumedha Design systems Pvt.Ltd, Hyderabad.
- Worked on 28nm Technology (Synopsys Tools).

PROJECTS:

Academic Project:

Implementation of Low Power Approximate Multiplier Using High Order Compressors:

The need for low-power design is becoming a major issue in high-performance digital systems. Low-power multipliers are very important for reducing energy consumption of digital processing systems. In this work, approximate 8*8 multipliers are designed to reduce the power consumption. The design of approximate multiplier appears as a promising solution for many error-resilient applications.

Projects Undertaken at Sumedha IT:

ALU:

Technology node	: 28nm
Tools used	: Design Compiler
Frequency	: 400MHz
Clocks	: 2
Instance count	: 810
Roles & responsibilities	: RTL Synthesis

RPTOPTOP:

Technology node	: 28nm
Tools used	: Design Compiler, ICC2
Frequency	: 400MHz
Clocks	: 1
Instance count	: 76K
Roles & responsibilities	: RTL Synthesis, Physical Design

- RTL Synthesis, Physical Design flow stages like Floorplanning, Placement and Routing, Clock Tree Synthesis.

EXTRA CURRICULAR ACTIVITIES :

- Volunteered in “VLSID Conference 2023” held in Hyderabad.
- Volunteered in “GLOBAL ALUMNI MEET 2019” UCE, OU.
- Organizer for the event “FREESTYLE 2017” UCE, OU.

BEHAVIORAL SKILLS :

- Creative
- Empathetic
- Quick Learner
- Sophophilic

DECLARATION:

I Chetana, here by declare that the information mentioned above is true and correct to the best of my knowledge and belief.

Date:

Hyderabad. **CHETANA**