RESUME

Harsh Verman

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Career objective

Seek a position to utilize skills and abilities in the industry that offers professional growth while being resourceful and flexible.

Executive Summary

- Got certified as RTL Design and Verification Engineer from VLSI FIRST.
- Possess the analytical skills necessary for engineering innovative approaches in VLSI field.
- Good understanding of VLSI design and Verification environment.
- Good Knowledge of HDL languages.
- Good working understanding of SV and UVM.

Skills Summary

HDLs	: Verilog
HVL	: System Verilog
Verification Methodology	: Constraint Random Coverage Driven Verification (CRCDV).
TB Methodologies	: UVM
EDA Tool	: Modelsim (Questa), Xilinx ISE Design
Operating Systems	: Linux, Windows
Protocols	: AMBA- AXI 3.0,
Application	: Advanced Encryption Standard (AES)

Certification Course

Certification Course	**:** ASIC design and verification.
Institute	**:** VLSI First, Hyderabad India.
Course Work	: RTL Design and verification, Functional Coverage, Constraint-Randomization, SV Environment, UVM testbench.

Project Details (During Trining)

Project 1:

Project Title : **AES (Advanced Encryption Standard)**

HDL : Verilog

Description : AES is implemented in software and hardware throughout the world to encrypt sensitive data. It is essential for government computer security, cyber security and electronic data protection

Project 2:

Project Title : **AMBA AXI-3.0**

HVL : Universal Verification Methodology

Description : Advanced eXtensible Interface, or AXI, is part of ARM's AMBA specifications. The AXI is a point to point interconnect that designed for high performance, high speed microcontroller systems. The AXI protocol is based on a point to point interconnect to avoid bus sharing and therefore allow higher bandwidth and lower latency.

Educational Qualifications

Qualification	University	Name of the Institution	Year of Passing	Percentage obtained
B.Tech (ECE)	CSVTU	Shri Shankaracharya Group of Institute	2021	69.03
Intermediate	CGBSE	Good Shepherd English Medium School	2017	74.9
S.S.C	CBSE	Weidner Memorial Sr. Sec. School	2015	55

Co-Curricular activities

Workshops

- Attended to a workshop in collaboration with the **M Rise Educational Services on VLSI Front-End**

DECLARATION

I hereby declare that the above information given was true up to my knowledge.

Date: Signature

Place: Raipur (Harsh Verman)