KAMPA PRAVEEN KUMAR
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CAREER OBJECTIVE:

To contribute my skills and expertise to the overall document of the organization and to seek constantly sharpen my abilities and improve my efficiency.

TRAINED:

1) Physical design training at vlsiguru

Worked on physical design at block level for 14nm technology

TECHNICAL SKILLS :

a) Excellent in Unix commands/Used gvim commands in PD flow
b) Worked on TCl for PD applications
c) Worked in ASIC design flow (RTL to GDSII). Understanding of inputs and outputs of all the stages involved in physical design flow (APR).
d) Implementation of congestion driven macro placement during Floor planning, Power planning with IR drop, placement, CTS and routing.
e) Analyzed the complex timing reports and met timing closure on DSM technology.
f) dentifying and constraining timing paths, analyzing timing under various PVT corners, OCV, False Paths, Half cycle paths, MCMM, and CRPR.
e) Effect of Crosstalk, Electromigration, Antenna effect, Latch up and ESD for design.
f) Solved DRC, DFM, LVS .
g) Theory knowledge of SRAM bit cell and basic architecture. Scripting: fixing violation through Tcl scripts.
h) Aware of different files: .Lib, DEF, LEF, SDC and SPEF, .tf.
i) Expertise knowledge on CMOS theory, MOSFET's and Logic Design.

Tools Used

Synthesis : Design compiler
P&R : ICC2
STA : Prime time

Project 1 :

Traning project

Technology : 14nm or 28nm
Metal layers : 9 metal layers
standard cell count : 50k
Macros : 40
No of clocks : 5 clocks
Max frequency : 450 MHz
Number power domain : 2

Summary

a) Imported design using NDM methods
b) Performed sanity checks
c) Performed different iteraration for creating core area and die area
d) Written TCL script for port placements based locations
e) Placed macros according to guidelines to meet timing and to reduce congestion
f) Uderstood UPF and created voltage area for power domains
g) Done power planning and fixed issues after power planning
h) Done Placement and CTS with minimum congestion and timing violations

i)Done routing and fiixed shorts and DRC violations after routing
j) Performed signoff RC extraction and closed timing using Prime time
k) Performed timing ECO in ICC2

Project 2:

Traning project

Technology : 14nm or 28nm
Metal layers : 9 metal layers
standard cell count : 65k
Macros : 32
No of clocks : 5 clocks
Max frequency : 650 MHz

Summary

a) Imported design using and done floorplanning to meet timing , power and other design requirements
. b) Performed sanity checks
c) Performed different iteraration for creating core area and die area
d) Written TCL script for port placements based locations
e) Placed macros according to guidelines to meet timing and to reduce congestion
f) Uderstood UPF and created voltage area for power domains
g) Done power planning and fixed issues after power planning
h) Done Placement and CTS with minimum congestion and timing violations
i) Done routing and fiixed shorts and DRC violtions after routing
j) Performed signoff RC extraction and closed timing using Prime tim

Educational Qualition

i) B.TECH

College/University :Sri Vidyanikethan Engineering ,TIrupathy
Passout year : 2021
Aggreagate marks : 60.11%

ii) DIPLOMA

College/University:S.V Government Polytechnic college
Passout year : 2018
Aggreagate marks : 73.6

iii) SSC

school : V.R HIGH SCHOOL
Passout year : 2015
Aggreagate marks :7.7

Language Known : English, Telugu ,Hindi

Hobbies : Reading News Paper Listening music.

DECLARATION::

I here by declare that the above mentioned information is correct up to my knowledge and I bear the responsibility for the correctness of the above mentioned particulars.

PLACE:

DATE: (K.PRAVEEN KUMAR)