SHYLAJA REDDY

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I'm currently looking for design verification roles. I did my Masters in Microelectronic & communications engineering from Northumbria University, UK. I have about one and half years of overall work experience spanning ASIC Design Verification, FPGA and Optical Fibers. I am hard working, love bug hunting and am a fast learner.

EDUCATION

November 2021 TO PRESENT

ASIC DESIGN VERIFICATION TRAINEE, CHIPEDGE TECHNOLOGIES PVT. LTD.

- Development of Verification Environment for Memory Model using UVM
  This project is about building a verification environment for the given memory model design using UVM and check for correct functionality in accordance with the intent specified in the specifications of the device.
  Software tools: VCS
- Knowledge on AMBA AHB-lite and APB.
- Hands on experience on standard simulation tools like Synopsis VCS and EDA playground.
- Good experience in building verification environment from scratch.

Graduated in 2021

MSC IN MICROELECTRONIC & COMMUNICATIONS ENGINEERING, NORTHUMBRIA UNIVERISTY NEWCASTLE, UNITED KINGDOM.

- **Thesis - Analysis and Optimization of Single-Mode Optical Fibre Network**
  This project concentrates on designing, simulating and optimizing the performance of single mode optical fibre network with the EDFA (Erbium Doped Fibre Amplifier) employed in it using the optisystem software.
- Grade: Commendation (65%)

Graduated in 2019

B.E IN ELECTRONICS & COMMUNICATIONS ENGINEERING, DAYANANDA SAGAR ACADEMY OF TECHNOLOGY & MANAGEMENT.

- **Thesis – Design of FPGA-based digital sphygmomanometer**
  A patient's health monitoring device based on FPGA has been developed for monitoring parameters such as heartbeat, temperature, and blood pressure. Parallelism is achieved and information collected from the device may help in suggesting medication to overcome hypertension and lead a healthier life.

SKILLS

- Universal Verification Methodology
- System Verilog/Verilog
- Bus Protocols: AMBA AHB-lite, APB
- Knowledge on Etherenet protocol
- Xilinx Vivado
- Digital Logic Design
- PCB design software
- Opti-System Software

WORK EXPERIENCE

- Interned as a "**Research Assistant**" at IBM Watson, London [September 2020 to May 2021].
- Worked as an "**Application Support Engineer**" at Accenture Services Private Limited, Bengaluru [May 2019 to July 2019].
- Interned as a "**Product Design Engineer**" at e-Xcel Energy, Bengaluru [July 2018 to September 2018].

**References available upon request.