SIVA SATHEESH

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Experience Summary

Profile Brief	Total 1+ years of training experience in VLSIGURU INSTITUTE
Technology Node	28nm
Foundries	TSMC
EDA tools	ICC2, StarRC, Primetime.
Scripting	Basics of TCL
Others	Good knowledge on various aspects of physical design all the way from floorplanning to GDSII.

Education

- Bachelor of Technology in Electronics and Communications Engineering (ECE) from GVR&S college of Engineering and Technology **(2022)**
- Board of Intermediate from NARAYANA Jr college **(2017)**
- SSC from SKV high school **(2015)**

Professional Expertise

- Understanding of inputs and outputs of all the stages involved in physical design flow (APR).
- Implementation of congestion driven macro placement during Floor planning, Power planning with IR drop, CTS and Routing.
- Identifying and constraining timing paths, analyzing timing under various PVT corners.
- Effects of Crosstalk, Electromigration, Antenna effect, Latch up and ESD for design.
- Solved DRC, LVS and met PV clean.
- Scripting: fixing violations through TCL scripts.
- Aware of different files: .LIB, LEF, SDC, TF, TLU+ and SPEF.
- Knowledge on Digital electronics, CMOS theory and Basics of UNIX.

Project 1 details

Project Title : Block level implementation – ORCATOP 32-bit Multi voltage processor (ICC-2) 28nm.

Worked At : VLSIGURU institute.

Description : 28 nm technology node, 52k standard cells and 40 macros, clock frequency 54MHZ,Utilization 75%. Complete Flow Floor plan, Placement, CTS, Routing.

Duration: March to August 2022

Tool: Synopsys IC Compiler (ICC2)

CHALLENGES

- Performing multiple floorplan iterations based on data flow to resolve congestion issues, TNS under control and acceptable standard cell utilization
- Power planning with min number of P/G straps and width to meet the IR drops.
- Reducing logical DRC violations of clock tree and improving TNS by useful skew.
- Defining effective blockages to reduce global congestion.

Project 2 details

Project Title : Block level implementation – ORCATOP 64-bit Multi voltage processor (ICC-2) 28nm.

Worked At : VLSIGURU institute.

Description : 28 nm technology node, 60k standard cells and 50 macros, clock frequency 54MHZ, Utilization 75%. Complete Flow Floor plan, Placement, CTS, Routing.

Duration: September 2022 to February 2023

Tool: Synopsys IC Compiler (ICC2)

CHALLENGES

- Mainly concentrated on timing and congestion. And applied the blockages to reduce global congestion and timing as well.
- Fixing transition and hold violations by ECO routing and fix eco command.
- Timing analysis after each stage of APR flow to identify the type of violations and solved them by different fixing techniques.

Personal Details

Father Name	: Siva Armugam
Date of Birth	: 20-08-2000
Address	: D.No: 8/28, Kuchipudi, Pin code: 522313, Andhra Pradesh.
Country	: India
Languages Known	: English, Telugu, Tamil.

Declaration

I hereby declare that the above given information is true to the best of my knowledge and belief.

Place : Bangalore
Date : (Siva Satheesh)