Damodaram P

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Indian Single Male www.linkedin.com/in/damodaram-palichetty-b41059190

https://github.com/DhamuDynamic

Profile

To seek a creative career in a challenging environment so as to learn and improve continuously by enhancing my skill set.

Education

SSC (10th Class), Z.P.High School (Boys) 06/2016 – 04/2017 | Narayanavanam, India
I secured **9.8 CGPA** in my 10th class.

Pre University Course (Intermediate), 08/2017 – 04/2019 | Vempalli, India
Rajiv Gandhi University of Knowledge Technologies, R.K.Valley
I secured **9.0 CGPA** in my PUC.

B.Tech : Electronics and Communication Engineering, 06/2019 – present | Vempalli, India
Rajiv Gandhi University of Knowledge Technologies
I secured **9.2 CGPA**

Skills

C, MATLAB, Verilog, Digital Electronics, Digital System Design, Analog Electronics, Presentation Skills, Communication SKills, Team Player

Projects

Design of Low Power High Speed Full Adder using GDI Technology
Here we address a problem of delay and power consumption in digital circuits. We made our attempt to solve it by using GDI technology.

ALU using pipelining
In this project, I implemented and verified the functionality of ALU using pipelining in order to reduce the time taken to complete execution an instruction.

Simple Router Design
I implemented Simple 1x3 Router Design using verilog.
Router routes the data from source to one of the three destinations.
It includes some internal modules like Register, Finite state Machine, FIFO, Synchroniser.

Generation of 24 Hour Digital Clock
I implemented a 24-Hour Digital Clock using Verilog

Synchronous FIFO
I implemented a Synchronous FIFO which act as a buffer between a source and destination.

Automatic Audio Captioning

GCD Machine
I implemented a machine that computes GCD (Greatest Common Divisor) of two numbers. I implemented the Data path and designed Controller.

UART Protocol 11/2022 – 12/2022
UART : Universal Asynchronous Receiver Transmitter
In this project, I tried to implement and verify the functionality of the UART transmitter and Receiver.
It contains 3 sub-modules namely Baud Rate Generator, Transmitter and Receiver.

Courses

VLSI Design, SURE Trust 05/2022 – 08/2022 | India
I enhanced my VLSI skills and I dive deep into the VLSI in this course.
In this course, I learnt to design many Digital Circuits .

Certificates

- Certificate for completion of 4 months VLSI Training at SURE Trust
- Participation Certificate for District Level Inspire Seminar
- Paricipation Certificate for State Level Mathematics and Science Exhibition
- Participation Certificate for participating in Quiz held on National Mathematics Day
- Merit Certificate for winning Quiz competition conducted by ISRO

Interests

Meditation, Watching Movies

Organizations

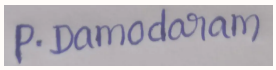
Helping Hands Organisation, Volunteer 08/2017 – present | India

Awards

Inspire Award, State govt. of Andhra Pradesh

Declaration

I solemnly declare that all the above information is correct to the best of my knowledge and belief.



P.Damodaram