Nived M Mutnal

+91 7338487203

Nivedmutnal8@gmail.com

www.linkedin.com/in/nived-mutnal-0a3946208

Career Objective

Constantly striving for the integrity of the company by putting genuine efforts, keeping honesty as a preference. Willing to obtain VLSI design engineer position which will utilize my creative thinking and knowledge about VLSI. I consider noble values as an important aspect, which reflects in my work and help me to grow individually and as a team.

Professional Training

Advanced VLSI Design and Verification Course

Maven Silicon VLSI Design and Training Centre, Bangalore
Sept 2022-till date

Education

Graduation **2018-2022**

Bachelor of Engineering in Electronics and Communication
SKSVMACET, Lakshmeshwar
CGPA-7.98

Intermediate **2016-2018**

Smt. Vidya P. Hanchinmani Independent Pre-University Science College. Dharwad
Percentage-78.5%

ICSE **2016**

Rainbow Residential Public School, Ranebennur,
Percentage-76%

Technical Skills

VLSI Domain Skills

- HDL: Verilog
- HVL: System Verilog
- Verification Methodologies: Constraint Random Coverage Driven Verification
- Digital Electronics: Combinational & Sequential circuits, FSM, Memories, CMOS implementation, Stick diagram.

- **STA**: STA Basics, Comparison with DTA, Timing Path and Constraints, Different types of clock Clock domain and Variations, Clock Distribution Networks, Fixing timing failure.
- **Verilog Programming**: Data types, Operators, Processes, BA & NBA, Delays in Verilog, begin - end & fork join blocks looping & branching construct, System tasks & Functions, compiler directives, FSM coding, Synthesis issues, Races in simulation, pipelining RTL & TB Coding,
- **Advanced Verilog & Code Coverage**: Generate block, Continuous Procedural Assignments, Self-checking testbench, Automatic Tasks, Named Events and Stratified Event Queue, Code Coverage: Statement and branch coverage, Condition & Expression Coverage, Toggle & FSM Coverage.

Verification Skills

System Verilog HVL

- Memories - Dynamic array, Queue, Associative array, Task & Function - Pass by reference
- Interface - Modport and clocking block.
- Basic and advanced object-oriented programming - Handle assignments, Copying the object contents, Inheritance, polymorphism, static properties and methods, virtual classes and parameterized classes.
- Constraint Randomization - constraint overriding and inheritance, Distribution and conditional constraints, Soft, static and inline constraints.
- Thread synchronization techniques - events, semaphores and Mailbox - built-in methods.
- Functional coverage - Cover groups, bins and cross-coverage, CRCDV and regression testing.

UVM

- UVM Objects & Components
- UVM Factory & overriding methods
- Stimulus Modelling
- UVM Phases
- UVM Configuration
- TLM
- UVM Sequence, virtual sequence & sequencer
- Introduction to RAL

Technical Project

Router 1x3 – RTL design and Verification

HDL: Verilog
Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

Responsibilities:

- Architected the block level structure for the design.
- Implemented RTL using Verilog HDL.
- Synthesized the design.

CAN Protocol Controller Using System Verilog

Description:
The CAN protocol is a standard designed to allow the microcontroller and the other device to communicate with each other without any host computer

Responsibilities:

- Implemented RTL using Verilog HDL
- Verified the working of bit arbitration and CRC checker component of CAN protocol.

Behavioral Skills

- Time Management
- Team Work
- Patience

Hobbies

- Dancing
- Playing volleyball
- Running
- Travelling

Declaration

I hereby declare that the information furnished above is true to the best of my knowledge and belief.

Date:

Place:Dharwad, Karnataka, India

Nived M Mutnal