DARSHAN B P (Available for Immediate joining)
S/O Putte Gowda B H, Majjigenahalli.
Bhadravathi Shivamogga 577229

+91 9513271428
darshanbp15@gmail.com

PROFILE:

Working as an Associate Physical Design Engineer at **Sevitech Systems Pvt Ltd [a UST Global Company]** since May 2022. Highly organized and detail-oriented postgraduate Diploma in **ASIC Design** from **RV-VLSI Design Centre, Bengaluru.**

EXPERIENCE:

1. **Sevitech Systems Pvt Ltd [a UST Global Company], Bengaluru [May 2022 – Till date]**
   - **Role: Associate Physical Design Engineer**
   - Worked on the two different projects of technology nodes **28**nm.
     - Worked on **28nm** technology node ,**500Mhz** Clock ,**9** Metal layer stack, **16** hard macros.
     - Worked on **28nm** technology node ,**500Mhz** Clock ,**9** Metal layer stack, **46** hard macros
   - Responsible for full block design from Netlist to GDS and Signoff checks.
   - Performed Floorplan, Placement, Cts, Routing and STA & ECO fixes.
   - Performed various optimization techniques in Placement and CTS like Partial Blockages, Cell padding, Placement bounds, Magnet Placement, Path Groups, and Skew Groups Etc.
   - Performed Classic & CCD methods of CTS to improve skew and timing performance of the design.
   - Performed various timing ECO optimizations like Cell sizing, Vt Swapping, Buffer insertion, DRV fixing and Congestion Reduction Techniques.
   - Reduced Crosstalk, glitch, Electromigration, IR drop and Signal Integrity issues with the Proper NDRs.

2. **RV-VLSI Design Centre, Bengaluru [Dec 2021- May-2022]**
   - **Role: Physical Design Trainee.**
   - Worked on **40nm** technology node ,**800Mhz** Clock **,7** Metal layer stack, **34** hard macros.
   - Responsible for full block design in Physical Design and STA.
   - Floor planning: Macro placement, channel estimation, Physical cell placement, Blockage definition.
   - Power planning: Inserting PG strap, Power hook-up.
   - Placement: Placement algorithm, In-place-optimization, DRC fixing, Timing and Congestion optimization.
   - Clock Tree synthesis: clock tree building & optimization, timing and Congestion fixing.
   - Routing: Global and detail routing, timing, Congestion and DRC fixing.
   - Performed various optimization techniques in Placement and CTS like Partial Blockages, Cell padding, Placement bounds, Magnet Placement, Path Groups, and Skew Groups Etc.
   - Have a Working knowledge to Reduce Crosstalk, glitch, Electromigration, IR drop and Signal Integrity issues.

TECHNICAL SKILLS:

- **Tool used** **:** Synopsys (ICC-II),
  Prime Time.
  StarRC.
  Design Compiler**.**

- **Scripting language:** Basics of TCL.
  Basics of Python**.**

- Basic knowledge of MOSFET, CMOS, COMBINATIONAL & SEQUENTIAL Circuits.
- Basic knowledge of ASIC Design flow.
- Basic knowledge of BACKEND DESIGN -Floorplan, Placement, CTS, Routing & STA.
- Basic working knowledge of SETUP, HOLD, DRVs, Crosstalk, Glitch analysis and fixes. SKEW & LATENCY reduction techniques.
- Basic working knowledge of DRC fixes & LVS flow.

EDUCATIONAL CHRONICLES:

BRANCH: ELECTRICAL AND ELECTRONICS ENGINEERING.

Degree	University/ Board	Institutions	Percentage	Year of Passing
PG Diploma in ASIC Design	RV Institutions	RV-VLSI Design Centre-Bengaluru	----------	2022
BE	VTU	SVCE Bengaluru	5.7	2020
DIPLOMA	DTE	VISSJ Govt Polytechnic, Bhadravathi	61.36	2016
SSLC	KSEEB	Navachethana English school. Bhadravathi	82.56	2013

CERTIFICATIONS:

- **Programmable logic controller (PLC)** and **SCADA** association with **IETE** at **PROLIFIC SYSTEMS AND TECHNOLOGIES PVT LTD**
- **Microcontroller and Internet of Things** at **PROLIFIC SYSTEMS AND TECHNOLOGIES PVT LTD**
- Workshop on **Renewable Energy and Energy Conservation for Sustainable Development** association with **INSTITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS.**
- SEMINOR ON **Indian Power System & Overview** ASSOCIATION WITH **POWER GRID CORPORATION INDIA LIMITED**
- My article published in **"Nyayanishta -a legal magazine**".
- **2nd Place** in **Quiz Competition** Which Was Organized By **KSTA.**

SPECIAL INTERESTS:

- Writing articles
- Teaching.
- Newspaper reading.
- Books reading.

DECLARATION:

I hereby declare that the above information is true to the best of my knowledge.

DARSHAN B P