Name : Venkata Sagarika Mamidi
Email Id : sagarikavm2001@gmail.com
Phone no : +91 9573310740

www.se-minds.com

OBJECTIVE

Seeking a responsible position as an entry level Physical Design Engineer which enables to bring the best out of my knowledge and experience in achieving organizational goals and personal growth.

PROFESSIONAL TRAINING

An Industry Oriented Trainee in **VLSI ASIC PHYSICAL DESIGN** from **Se-minds Pvt. Ltd**., Hyderabad from **August 2022 to January 2023.**

Course outline:

Basic Electronics, Digital fundamental concepts, MOSFET, CMOS design concepts, fabrication, Basics of STA, Logic Synthesis fundamentals. Physical Design concepts: floor planning, PG planning, Low Power design techniques, CTS, Routing techniques, signal integrity. Advanced STA, Basics of TCL, Basics of Unix.

Tools:

Experience in physical design of 90nm and 45nm technologies using Cadence tool

1. Cadence Innovus : Place &Route
2. Cadence Genus : Logic Synthesis

PROJECTS:

Project -1: Place and Route (Top level)

Design Name : asic_entity
Objective : Timing Driven layout.
Tools Used : Cadence Innovus
Area : 31672192.5 μm^2
Macros/Instance : 29 Macros, 62656
No. of Clocks : 08
Frequency : 125Mhz
Technology/Layers : 90nm/9 Metal Layers

Role : Performing Audit checks, Floor plan, Placement, Trail route, Timing Analysis, CTS, Detailed Routing, Post Route Optimization, Sign Off Checks, Achieved 0% Congestion at Trail Route Stage.

Project -2: Place and Route (Block level)

Design Name : eVITERBI_322
Objective : To Observe I/O Pins Place & Fixing DRV's & DRC's
Tools Used : Innovus
Area : 435.024 μm^2
Macros/Instances : 0/100
No. of Clocks : 01
Frequency : 250Mhz
Technology/Layers : 45nm/7 Metal Layers

Role : Performing Audit checks, performing normal PNR flow and done with foundation flow, Floor plan, Placement, Trail route, Timing Analysis, CTS, Detailed Routing, Post Route Optimization.

Name : Venkata Sagarika Mamidi
Email Id : sagarikavm2001@gmail.com
Phone no : +91 9573310740

www.se-minds.com

Project -3: Place and Route (Block level)

Design Name : usb_wrapper
Objective : To Meet Setup & Hold time, Fixing DRV's & DRC's
Tools Used : Innovus
Area : 1741021.4826 μm^2
Macros/Instances : 12 Macros/28831
No. of Clocks : 17
Frequency : 208Mhz
Technology/Layers : 90nm/5 Metal Layers

Role : Performing Audit checks, performing normal PNR flow and done with foundation flow, Design Import, Floor plan, Placement, Trail route, Congestion Analysis, Timing Analysis, CTS, Detailed Routing, Post Route Optimization, Fixing DRV's, DRC's.

Project -4 : Logic Synthesis

Objective : Perform ZWLM Synthesis & Obtained optimized Gate Level Netlist.
Tools Used : Cadence Genus
Area/Instances : 237011.129 μm^2 / 4131
No. of Clocks : 07
Frequency : 500Mhz
Technology/Layers : 45nm/11 Metal Layers

Role : Check SDC and error correction, generating reports for Area, Timing and Power, different efforts for optimization (Generic, Mapping, Optimization), timing analysis and fixing.

ACADEMIC EDUCATION:

1. B.Tech in the stream of Electrical and Electronics Engineering from Dadi Institute of Engineering Technology, Anakapalle in 2022 with 7.71 CGPA.
2. Diploma in the stream of Electrical and Electronics Engineering from Dadi Institute of Engineering Technology, Anakapalle in 2019 with 81.2%.
3. Secondary School Certificate from ZP High School, Aganampudi in 2016 with 8.3 CGPA.

PERSONAL STRENGTHS

1. I can easily adapt to any technology.
2. I have good logical knowledge towards problem solving.

DECLARATION:

I hereby declare that the above-mentioned information is correct to the best of my Knowledge.

(VENKATA SAGARIKA MAMIDI)