MAHANTAGOUDA SOMANAL

mahantagoud.patil@gmail.com +91-9880429463 in https://www.linkedin.com/in/mahantagouda-somanal-776363245

PROFILE

An Electrical and Electrical Engineer post graduate with good VLSI domain skills, looking forward to building a career in the VLSI field and enhancing my professional skills by seeking a challenging position in the organization and there by keeping the goals of the organization and self as the prime objective.

PROFESSIONAL TRAINING

Advanced VLSI Design and DFT

Maven Silicon Centre of Excellence in VLSI, Bangalore

LANGUAGES

- Kannada
- English

ACADEMIC QUALIFICATION

M.Tech

The National Institute of Engineering, Mysore

- *09/2018-08/2020, CGPA :-7.92*
- *Courses: -Power Systems Engineering*
- *Thesis:- A Dynamic voltage Restorer based interface scheme for Micro grid*

Bachelor of Engineering

Gogte Institute of Technology, Belagavi

- *06/2015-06/2018, percentage :- 63.18*
- *Courses:-Electrical and Electronics Engineering*

Diploma

K.H.K Institute of Engineering, dharawad

- *2010-2014, percentage :- 60.85*
- *Courses:-Electrical and Electronics Engineering*

S.S.L.C

VBHS High School, Talikoti

- *2005-2008, percentage : -76.16*
- *Courses:-General*

CERTIFICATES

- **ADVANCED VLSI DESIGN AND DFT**
  Course at Maven Silicon VLSI design and training center Bangalore
- Electric Power Grid Modernization: Trends, Challenges and Opportunities
- Power Electronics Application to Renewable Energy System and Energy Storage System
- Mitigation of Power Quality Issues in Distribution Generation System using Custom Power Devices

TECHNICAL SKILLS

operating system:

- Windows XP, Linux

MS Office:

- Microsoft Word, PPT, and MS Excel

VLSI domain skills:

- HDL: Verilog
- EDA Tool:

Mentor Graphics – Tessent Tool, Questasim and Xilinx

Domain:

ASIC/FPGA front-end Design and DFT

VLSI DFT Skill:

- Digital Electronics design
- DFT
- ATPG
- Scan Chain Insertion
- Test Kompress (EDT)
- Boundary scan
- IJTAG
- BIST
- Test coverage & Fault coverage analysis

PERSONAL DETAILS

Father Name : Tippanagouda somanal
Mother Name : Mudakamma somanal
Date of Birth : 22-07-1992
Gender : Male

PROJECT

DFT Insertion on RISC-V core

Role: DFT Trainee Engineer

EDA Tools

Test generation tools like Tessent Scan, Tessent Fast Scan, Tessent Boundary scan, test –kompress.

Description

The DFT design flow and implement the DFT logic on a RISC-V 32 I processor. This processor supports base integer instructions. It's a 3 stage pipelined processor which executes 32 bit instructions. In this project will insert boundary scan, scan chain, EDT IP core on this 32 bit processor design and implement the ATPG pattern generation using stuck-at-fault model. The design needs to be synthesized, and gate level netlist will be used for the DFT design flow

objectives

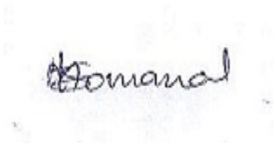
- Insert Boundary scan IJTAG components into the gate-level netlist.
- Insert scan chain into gate-level netlist.
- Insert EDT IP core to the scan chain netlist.
- ATPG flow to obtain test patterns using stuck-at-fault model.
- Report the fault coverage and test coverage.
- Improve the test coverage

DECLARATION

I hereby declare that the above-mentioned information is true to the best of my knowledge and I bear theresponsibility for the correctness of the above-mentioned particulars.

Date:

Place: Bangalore



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