Hemalatha Paruchuru
hemaparuchuru2109@gmail.com, 8074153422
Banglore-560076, Karnataka

Career Objective

Seeking a position as a Physical Design Engineer with an opportunity to work on advance design technologies where my ability and skills will be utilized effectively for the betterment of myself and the Organization.

Core Competancy

- Well versed with ASIC design flow. Understanding of inputs and outputs of all stages involved in Physical design flow.
- Good Knowledge and Understanding of STA concepts.
- Efficient in timing aware and congestion driven macro placement during Floor Planning & Power planning .
- Analyzing and understanding basics of Linux, Perl ,TCL & C programming.
- Aware of different files like .Lib, DEF, LEF, SDC and SPEF.
- Placement of macros using appropriate data flow and creation of efficient power mesh within IR drop limit.
- Hands on experience with EDA tool, Synopsys ICC2 Compiler & Synopsys Prime Time.
- Comprehensive Knowledge of Digital Logic Design, CMOS theory.

Education Details

Advanced Diploma in ASIC Design **2023**
RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2022**
Ramireddy Subba Ramireddy Engineering College, with 84 %

12th **2018**
Sri Srinivasa Junior College, with 97.6 %

SSLC **2016**
R R English Medium High School, with 98 %

Certifictaions

Got Certified by RV-VLSI Design Center in Advanced Studies in ASIC Design. **2023**

Domain Specific Project

RV VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Sep-2022 to Oct-2022

Static Timing Analysis for various Timing Paths

Description

Complete analysis of different timing paths by using slew and delay tables for single clock & Multicycle clock by considering constraints such as clock skew, uncertainty, input delay, output delay and derating factors.

Tools

Prime Time by Synopsys

Roles and Responsibilities

- Computing setup slack and hold slack for different timing paths by using skew and delay tables for finding worst slack and best slack for setup and hold.
- Understanding the cause for setup and hold violations and to find the ways to fix them.
- Generating and analyzing timing reports in PT shell for the given timing paths.
- Understanding of clock abnormalities and timing exceptions.
- Understanding of derate factors, PVT corners, Global variations, OCV and AOCV.

RV VLSI and Embedded Systems Design Center

Graduate Trainee Engineer Oct-2022 to Feb-2023

SoC Block Level Implementation of design block

Description

Implementation for Lakshya Subsystem using 40nm Technology node which contains 34 Macros and 43k Standard cell count and 7 metal Layers.

Specifications : Supply Voltage 1.1V, Area 4.2sqmm, Clock Freq. 833MHz, Power budget of 600mW, Max IR drop 5%.

Tools

ICC2 Compiler by Synopsys

Roles and Responsibilities

- Understanding the data flow among Macros with respect to ports, Channel spacing estimation between Macros.
- Building a good power plan to meet power budget (IR drop) by creating a mesh pattern and setting up suitable strategies to ensure that there are no floating errors & no DRC errors.
- Analyzing the global route Congestion map and determine where the hard and soft blockages to be added.
- Building a well-balanced clock tree meeting the target skew and fixing all setup and hold violations.

B.Tech Academic Project

Ramireddy Subba Ramireddy Engineering College 2022

Fast Binary Counters and Compressors generated by Sorting Network Description

In this project, fast saturated binary counters (7,3) , (15,4) and approximate (4,2) compressors based on sorting network are used to enhance the speed and performance of the process.

Tools

Xilinx Vivado, Verilog

Challenges

- Understanding the concepts of Counters, Compressors and Sorting Network. Generating and analyzing the RTL schematic and Technology schematic in Xilinx. Hands on experience with Verilog. Basic Understanding of VLSI Design Flow.