SHIJU N P

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Education

Degree/Certificate	Institute/Board	CGPA/Percentage	Year
B.Tech. (ECE)	Rajiv Gandhi institute of Technology Kottayam	7.39	2019-2022
Diploma	Govt Polytechnic College Chelakkara	7.4	2019
Senior Secondary	GHSS Valayam	73	2016
Secondary	GHSS Valayam	94	2014

VLSI Projects

- **Design of Pattern Detector** *December 2022*
  Tools: Verilog,Questasim Remote
  – Pattern detector on a serial input is designed using Moore and Mealy FSM and noticed a change in the number of states.
  – It requires coding an FSM to detect each pattern until it reaches the final pattern.
  – Implemented testbench that randomly generates a series of 1s and 0s to check the pattern.

- **Design and Verification of FIFO** *December 2022*
  Tools:Verilog, Questasim Remote
  – FIFO is a design component used for interfacing data transfer between two components either working on the same frequency or at a different frequency.
  – Both Synchronous and Asynchronous FIFO are implemented using verilog and RTL code.
  – This project was verified for its functionality by writing testbenchVerilog.

- **Single Port and Double Port RAM** *January 2023*
  Tools:Verilog, Questasim Remote
  – The Single Port RAM block models RAM that supports sequential read and writes operations but if you want simultaneous read and write operations then we can use Double Port RAM.
  – Both Single port and double port RAM were designed using Verilog and are implemented using Verilog RTL code.
  – This project was verified for its functionality by writing testbench in Verilog and simulated using Questasim.

- **Design and Verification of APB Protocol** *January 2023*
  Tools: System Verilog, Questasim Remote
  – APB(Advanced Peripheral bus) is a non-pipelined protocol optimized for low power and low bandwidth peripherals.
  – This project consists of a master and a slave which has been designed using FSM in System Verilog.
  – The master and slave are then interconnected to each other in a top module by instantiating the master and slave module .
  – The project has been verified and tested for its functionality using system verilog.

- **Design and Verification of UART Using Verilog** *February 2023*
  Tools:Verilog, EDA Remote
  – UAR stands for universal asynchronous receiver transmitter is one of the most commonly used communication protocols.
  – This project consists of a master and a slave which has been designed using FSM in System Verilog.
  – UART consists of a baud rate generator which consists of a counter that helps us provide the timing information at the transfers .
  – It also consists of a transmitter and receiver which are used to transfer data.
  – The two modules were designed in Verilog and interconnected by instantiating in the top module and were verified for their functionality by using testbench in Verilog.

- **Design and Verified Adder,Ram, FIFO Using system verilog test bench architcture** *February 2023*
  Tools:Verilog,System Verilog in EDA Remote
  – Wrote the RTL code for the full adder,Single port RAM,Dual port RAM and FIFO then verified using Complete Systemverilog Test bench architecture.
  – The test bench consist of Generator ,Driver,Monitor,Scoreboard and Referance model.
  – The communication between two component is make through the Mailbox And the Dut and test bench in connected via interface.

- **Design and Verified Basic Gates and combinational circuits by UVM Methodology** *February 2023*
  Tools: Verilog,System Verilog in EDA Remote
  – Wrote the RTL code for the gates and combinational circuits and verified using UVM(Universal verification method)
  – The verification is done in the EDA Playground. UVM 1.2 version is used for write the test bench and Synopsys VCS is used as a simulator

Academic Projects

- **Gesture-controlled wheel chair using mems** *march 2022*
  Tools: Arduino, mems, Motor Driver IC kottayam
  – Implemented the prototype of a wheel chair system controlled by the movement of hand palm with the help of mems(micro electro mechanical system) Accelerome te

- **Car automation system with seat belt and alcohol detection** *march 2021*
  Tools: Arduino, MQ3 kottayam
  – Implemented the prototype of a wheel chair system controlled by the movement of hand palm with the help of mems(micro electro mechanical system) Accelerome te

Key Courses Taken

- **RTL Design and Verification Course**: VLSI For All Pvt Ltd November 2022 - Ongoing

Skills Summary

•Technical skills : Digital Electronics, Analog Electronics, Basics of MOSFET Theory
•Protocols : APB, SPI, I2C, UART
•Languages : Verilog, System Verilog, UVM,Python
•Tools : Vivado,Questasim,EDA playground,GVim
•Soft Skills : Leadership ,Time management ,problem Solving

INTERSHIPS

- Doordarshan in 2018
- Attended training provided by mahendra private limited
- Data mining organized Revertech IT Solution

Awards and Certifications

- Digital circuits -NPTEL 2021
- Indroduction to IoT and Embedded System - coursera2020
- Crash Course on python - coursera 2021
- The arduino platform and C Programming
- Best performer of Mahendra private limited training
- Participate in State level athletic meet and earned 4th position
- Represended Distric level football 4 times

Positions of Responsibility

- NSS volounter Leader in Plus two
- Work IEDC Lead team in Diploma
- NSS volounter Leader in Plus two

Languages

- English
- Hindi
- Malayalam
- Tamil