VENUTURUPALLI SURYA NARASIMHA MEHAR

@ venuturupalli.mehar13@gmail.com 8639793510
in www.linkedin.com/in/mehar-venuturupalli-5a560a153

EDUCATION

POST GRADUATION :

M.Tech in VLSI Design, Amrita Vishwa Vidyapeetham

2021 – 2023 Coimbatore, Tamil Nadu

- Current CGPA - 8.36/10

GRADUATION :

B.Tech in Electronics and Communication Engineering, Amrita Vishwa Vidyapeetham

2017 – 2021 Amritapuri, Kerala

- Overall CGPA - 9.43/10

HIGHER SECONDARY EDUCATION:

Intermediate in MPC, Sri Chaitanya Junior Kalasala

2015 -2017 Vijayawada, Andhra Pradesh

- PERCENTAGE - 98.1%

SECONDARY EDUCATION:

Sri Chaitanya High School

2014 -2015 Vizianagaram, Andhra Pradesh

- CGPA - 9.8/10

TECHNICAL SKILLS

Programming Language

C

Hardware Description/Verification Languages

Verilog | System Verilog

Tools

Synopsys Verdi | Synopsys HWSW Verdi | Gcov | ModelSim | QuestaSim | Xilinx Vivado | Matlab | Cadence Virtuoso

Scripting Languages

Perl | Python | C Shell

PUBLICATION

IEEE Conference Paper

6-8 July 2021 IIT Kharagpur, India

V. S. Narasimha Mehar et al., "Covid-19 Prediction Through Chest X-Ray Image Datasets Using Deep Learning," 2021 12th International Conference on Computing Communication and Networking Technologies (ICCCNT), 2021, pp. 1-5, doi: 10.1109/ICCCNT51525.2021.9579985.

PROFILE SUMMARY

An enthusiastic, diligent and goal oriented person. Also, a good team player, who is open to learn and contribute to your esteemed organisation.

PROJECTS

RTL Design of Commutator through Memory Address Mapping and Input Scheduling Algorithm for Pipelined FFT Architectures

Aug 22 - Jan 23 ASE, Coimbatore

- In this M.Tech Final Year Project, a modified Input Scheduling Algorithm was introduced for the Multiple Delay Commutator(MDC) pipelined architecture of the FFT. Later, a comparitive analysis is made between the conventional MDC and the proposed MDC with respect to benchmarking parameters such as area, delay, inorder to observe the improved performance of the proposed design.

Covid-19 Prediction Through Chest X-Ray Image Datasets Using Deep Learning

Aug 20 - May 21 ASE, Amritapuri

- In this B.Tech Final Year Project, different Binary Classification models were developed to predict the existence of COVID in a Chest X-ray Image Dataset. These models were implemented through Pretrained CNN architectures. Finally, a comparitive study was made based on different bench marking parameters to find the efficient, reliable model among them.

INTERNSHIP

Design Verification(DV) Intern

Aug 22 - April 23 AMD, Bengaluru

- In this internship, I worked as a part of DDR DV Team, which is focusing on the Verification of DDR5/LPDDR5 IP.
- Primarly worked for the enablement of Firmware Coverage for the DV Testbench Environment, SV-UVM Testbench related DV tasks, enablement and usage of hardware-software debug tool for debugging Firmware versus DV Environment, Scripting for Automation.

ACHIEVEMENTS

-> GATE 2021 Qualified.

-> Published a Scopus Indexed IEEE Conference Paper on B.Tech Final Year Project in ICCCNT 2021 organised by IIT Kharagpur.

-> Won 2nd prize in Circuitrix Competition held at ASE, Amritapuri Campus in 2019. It was about designing the best circuit from it's output wave form in the least time possible.

-> Won 3rd prize in Fire Fighting Robot Competition held at ASE, Amritapuri Campus in 2018. It was about designing a bot which stops the fire in it's defined path.

AREAS OF INTEREST

Digital Design | Design Verification

STRENGTHS

Adaptability | Eye for Detail

LANGUAGES KNOWN

English | Telugu | Hindi