Alladi Supraja
Email id: suprajaalladi141@gmail.com
Contact No: +91 9573678772

Career Objective:

To be a part of organization that gives a scope to enhance my knowledge and utilizing my skills towards the growth of organization.

Professional Experience:

- Completed Physical Design Course completed from Takshila Institute of VLSI technologies in 6 months.
- Good Understanding of block level Physical design and verification concepts like **Floor planning, CTS, STA, DRC/LVS, DFM etc.**
- Practical exposure to Physical Design tools from **IC Compiler** tools.

Technical Skills:

- Strong understanding in the RTL to GDSII flow or design implementation.
- Good in concepts related to synthesis, place and route, CTS .
- Good knowledge and experience in Block-level Floor-planning and Physical verification.
- Working experience with tools like ICC.
- Strong knowledge in standard place and route flows ICC/Synopsys flows preferred.
- Well versed with timing constraints and STA.
- Good knowledge of Windows 7, 8 and Linux.

Academic Qualification:

Qualification	Name of Institution	Year of Passing	Percentage/ CGPA
B.Tech (ECE)	Mekapati Rajamohan Reddy Institute of Technology and Sciences, Udayagiri	2022	**72.56 %**
XII	Sri Chaitanya jr. College, Nellore	2018	**82.3 %**
X	Z.P.High school , survepalli	2016	**9.0**

Certifications:

- **Takshila Institute of VLSI Technologies**
  Title: Professional Training on Physical Design.

Project Worked On:

Title	**ORCA_TOP**
Tool used	IC Compiler
Description	• Technology: 32nm • No. of macros: 40 • Layer: 9 • Std. cell count: 56013 • No. of Clocks: 7 • Frequency: 416MHz
Responsibilities	Iterative Floorplan, IO ports placement, Powerplanning, Placement and CTS reviews, Routing and DRC checks.

Title	**ORCA_TOP_IO**
Tool used	IC Compiler
Description	• Technology: 28nm • No. of macros: 30 • Layer: 9 • Std. cell count: 50000 • No. of Clocks: 7 • Frequency: 400MHz
Responsibilities	Iterative Floorplanning and Power-planning Placement and CTS optimization Physical Verification and manual optimization Timing Closure and ECO

Academic Project:

- **Title : SMART CHILD RESCUE SYSTEM FROM BOREWELL**
- **Description:** To save the child from bore well by keeping the sensors at the top of the borewell which helps to sense the child if he/she fell inside the bore well.

Personal Profile:

Date of Birth : 22 August 2000
Languages Known : English, Telugu, and Hindi
Permanent Address : Alladi Supraja
D/o Alladi Venkata Ramanaiah, Thikkavarapadu, Survepalli bit-1, Venkatachalam, Nellore district, Andhra Pradesh - 524320

Date: **Alladi Supraja**
Place: Nellore