Saikumar kanakala

Ph:9985779290
Mail :kankalasaikumar0212@gmail.com
Address: Bondapalli village, Vizianagaram dist, 535260.
Linkedin: www.linkedin.com/in/kanakala-saikumar-03a512249

CAREER OBJECTIVE

As a job seeker, my intention and perspective towards career growth are to enhance myself in constant learning, I choose ultimately to be skilled, as per industry requirements and to be creative, and challenging, I always welcome problems with a positive attitude. So I select design verification engineer as a career path.

EXPERIENCE

Trainee engineer, POWERTECH SOLUTIONS, JAN2022-JUN2022

As a trainee electrical engineer supervising the AMC staff members, creating a safe environment in the field where heavy underground cables and overhead transmission lines maintenance should be done, as an engineer I should check the status of the equipment monthly and make a report on it. Attending fuse-off calls and faults on HV and UG cables rectified with modern techniques and checkups for hassle-free maintenance. Here I learned about supervising and gained knowledge in problem-solving skills, technical skills, and leadership qualities.

EDUCATION

Electrical and electronics engineering. 2015-2020

SATYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT 63%

Intermediate 2013-2015

NARAYANA JUNIOR COLLEGE 78.7%

PROJECTS

ADVANCED PERIPHERAL BUS

Tools used: Mentor Questa, EDA- playground.

Testbench developed: Verilog, System Verilog.

FIFO [FIRST IN FIRST OUT]

Tools used: Mentor Questa, EDA- playground.

Testbench developed: Verilog, System Verilog.

ADVANCED EXTENSIBLE INTERFACE

Tools used: Mentor Questa, EDA- playground.

Testbench developed: Verilog, System Verilog.

PRESENT

At present, I have done my VLSI training at the institute VLSIGURU, where I have gained knowledge in Verilog, system Verilog, universal verification methodology (UVM), and strong fundamental skills in digital electronics., also done major projects.

STRENGTHS

Flexible

Comfortable with ambiguity and able to thrive in a fast-paced environment

Self-motivated

being self-motivated I can be more productive.

ACHIEVEMENTS

- Created awareness in rural areas to ban plastic.
- Attended workshops on artificial intelligence in robotics and also MATLAB Simulink.

SKILLS

- Hardware description languages like Verilog, and System Verilog.
- UVM methodology
- Digital design fundamentals
- Good debugging skills
- Ability to work as a teammate
- Good verbal and written communication skills.

LANGUAGES

Telugu native

English advance

Hindi average

PASSIONS

- ♥ family
- cinematography
- music