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Career Objective

To secure a responsible career opportunity to fully utilize my knowledge and skills to work on cutting edge technologies, with the goal of fostering mutual progress between organization and self.

Core Competancy

- Hands on experience in STA Tool- PrimeTime, APR Tool- Synopsys IC Compiler 2 and OS- Linux and Windows.
- Knowledge in ASIC PD flow from GLN to GDS2.
- Knowledge and hands on experience in Pre-Layout STA, Interpretation of timing reports and fixing setup and hold violations.
- Analyzed and understood design constraints to specify PVT corners, False paths, Half cycle, Multicycle, CRPR, Signal Integrity.
- Worked on Floorplan for effecient planning and designed power mesh for minimal IR drop.
- Understood and modified TCL scripts for PD flow. Created TCL scripts to extract information of timing paths and finding WNS and TNS.
- Knowledge on Semiconductor theory, Logic Design and MOS structure.
- Worked on Transistor level Simulations for Research in low-power applications.

Education Details

Advanced Diploma in ASIC Design - Physical Design **2023**

RV-VLSI Design Center

Bachelor Degree in **Electronics and Communication** **2021**

Dayananda Sagar College of Engineering Bangalore, with 8.45 CGPA

2017

Alva's PU College Moodbidri, with 92.5 %

SSLC **2015**

KLE Society's School Gokak, with 79.8 %

Domain Specific Project

RV-VLSI Design Center

Graduate Trainee Engineer Nov-2022 to Feb-2023

Design of ASIC Block level Implementation

Description

The project was aimed to cover APR flow at 40nm, 1.1V over 4.2 sq. mm, operating at 833MHz, with 600mW. The key areas include: Floorplan, Powerplan, Placement, STA, CTS, Signal Routing, DRC check.

Tools

Synopsys PrimeTime, Syopsys IC Complier 2

Challenges

- Understood the design specs and designed the effecient Floorplan. Built the Powerplan to meet the IR drop with no floating wires, missing vias and no DRC violations.
- Placement of standard cells and Congestion analysis over the design. Spacing between macros to reduce congestion with Placement and Routing blockages through several iterations.
- Understood the essence of STA. Analysed the Timing reports for effects of Clock skew, CRPR, OCV, fanout. Traiged the cause for violations such as falsepaths and multicycle paths.
- CTS was performed for Class and CCD flow and comapred the timing reports. Signal routing was done and Antenna violations were fixed with metal jumper or diode.

B.E / B.Tech Academic Project

Dayananda Sagar College of Engineering Bangalore

Simulation and Modelling of Junctionless Surrounding Gate Tunnel FET

Description

To simulate a Tunnel FET with Junctionless phenomena for low-power applications. The nanodevice was designed for multi-gate operation using the Cylindrical gate all around device structure.

Tools

Silvaco TCAD, MATLAB

Challenges

- The exposure towards EDA tools for device level operation. Study and analysis of Junctionless Transistors and their working. Performance improvement of Junctionless devices in terms of ION/IOFF over conventional ones.