VIJAY VARMA PAKALAPATI

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CAREER OBJECTIVE:

To pursue a challenging career and be a part of progressive organization that gives a scope to enhance my knowledge and utilizing my skills towards the growth of the organization.

Professional Summary/ Work Experience:

I worked as a ASIC Physical Design Engineer at FRENUSTECH PVT LTD (JULY 2021-JANUARY 2023)

EXPERIENCE:

I have 1.7 years work of experience in Physical Design**.**

AREA(s) of Work:

Hands on experience in Synthesis,Floor Planing,Building CTS,Routing and STA Timing analysis, SI Analysis, OCV, LEC.

SKILLS (Tools/Languages/Methodologies):

Cadence EDA Tools:
Genus: Synthesis.
Innovus:Place and Route (PNR)
Tempus: STA and SI
Conformal: LEC
And Basics of TCL

PROJECTS AND DETAILS:

PROJECT 1 (Client United Microelectronics Corp.) (BLOCK LEVEL IMPLEMETATION)

Technology:	14nm
Gate count:	1.2M
Frequency:	800MHz
No. of clocks:	2

Role:

→Worked on Synthesis implementation and STA.
→Validating constraints for Synthesis and STA.
→Worked closely with PNR to resolve CTS issues by giving feedback to use NDR rules,clock buffers for building clock-tree and double-clocking,glitch and noise issues in CTS.
→Fixed Timing DRV.
→Encountered timing violations due to Crosstalk which were resolved.
→Manual ECO's were written to fix Setup and Hold violations.

Challenges:
→Writing ECO for the crosstalk issues.

PROJECT 2 (Harpoon -ALR) (BLOCK LEVEL IMPLEMETATION)

Technology:	TSMC 16nm
Gate count:	5.6M,47 macros
Size:	2000X1100 UM
Frequency:	1GHZ
No. of clocks:	1

Role:
→Floor planning to overcome the congestion and interface timings.
→Routed the design with the 9 metal layers including the power.
→Taken care of densely placed cells and congestion during placement.
→Fixed the DRV and DRC issues.
→Clock push and pull of timing critical paths.

Challenges:
→Initialized different Floorplans to avoid congestion.

Education:

Bachelor of Technology, Electrical and Electronics Engineering, Lendi Institute of Engineering and Technological,Andhra Pradesh, India, September 2020.

Declaration:
I hereby declare that the above information is true and correct to the best of my knowledge.

Place: Bangalore P.vijay varma