

openMSP430

Area and speed analysis

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Revision History

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1. AREA AND SPEED ANALYSIS	
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Area and Speed Analysis

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Notice: the results presented here might vary depending on the tool versions, applied timing constraints and exact configuration of the openMSP430 core.

The FPGA results were obtained using the free tool versions provided by the vendors (i.e ISE 11.1, QuartusII 9.1 & Libero 8.5).

The ASIC synthesis was run with Synopsys Design Compiler 2007.12 (without dc_ultra or any special feature).

1. Overview

1.1 FPGAs

				Utiliz	ation	
Manu- facturer	Devices	Info	Basic Config. (Core + Watchdog)	Hardware Multiplier	With debug interface (Software breakpoints)	Additional Hardware breakpoint unit
Xilinx	Spartan 3 Spartan 3E Spartan 3A Spartan 3A DSP Virtex 4	4-inputs LUTs	1 620	+ 200	+ 520	+ 80
	Spartan 6 Virtex 5 Virtex 6	6-inputs LUTs	1 240	+ 150	+ 350	+ 70
Altera	Cyclone II Cyclone III Cyclone IV GX Stratix	LEs	1 550	+ 210	+ 480	+ 110
Altera	Arria GX Arria II GX Stratix II Stratix III	ALUTs	1 030	+ 115	+ 380	+ 90
Actel	ProASIC3E ProASIC3L ProASIC3 Fusion IGLOOe	Tiles	3 550	+ 1 060	+ 1 200	+ 220
-	-	Registers	470	+ 75	+ 140	+ 45

(in	MHz, min and ma	Speed ax values across all speed grad	des)
Manufacturer	Devices	Basic Configuration (Core + Watchdog + HW Multiplier)	With debug interface
	Spartan 3 Spartan 3E Spartan 3A Spartan 3A DSP	30 - 40	25 - 35
Xilinx	Spartan 6	40 - 65	35 - 60
	Virtex 4	50 - 70	45 - 60
	Virtex 5	75 - 100	65 - 85
	Virtex 6	90 - 115	75 - 100
	Cyclone II	35 - 45	30 - 45
	Cyclone III Cyclone IV GX	40 - 55	35 - 50
Altera	Arria II GX	65 - 85	60 - 80
	Stratix II	55 - 75	50 - 65
	Stratix III	75 - 95	70 - 90
Actel	ProASIC3E ProASIC3L ProASIC3 Fusion IGLOOe	15 - 25	15 - 25

1.2 ASICs

			Area						
Process	Target Frequency	Info	Basic Config. (Core + Watchdog)	Hardware Multiplier	With debug interface (Software breakpoints)	Additional Hardware breakpoint unit			
180 nm	50 MHz	kGates	8	+ 2.5	+ 2	+ 0.8			
180 nm	100 MHz	kGates	10	+ 4.4	+ 2	+ 1.2			

2. Detailed results

2.1 FPGAs

2.1.1 Xilinx

	Speed Grade			oper	MSP430 Con	figura	tion			
FPGA Device		Info	No Debug	No Debug with HW multiplier	With debug interface (no HW breakpoints)	With debug interface (# hardware breakpoint units)				
				multiplici		1	2	3	4	
		4-LUTs	1 609	1 811	2 125	2 165	2 272	2 366	2 458	
	-4	Registers	458	533	594	637	679	721	763	
Snautan 2		Speed (MHz)	30.06	30.05	28.29	22.26	25.59	25.19	23.50	
Spartan 3		4-LUTs	1 609	1 811	2 127	2 166	2 276	2 367	2 459	
	-5	Registers	458	533	594	637	679	721	763	
		Speed (MHz)	32.69	34.11	32.63	27.09	28.90	27.68	27.63	
	-4	4-LUTs	1 615	1 816	2 131	2 185	2 298	2 383	2 474	
		Registers	458	533	594	637	679	721	763	
Spartan		Speed (MHz)	32.03	32.09	28.00	27.26	27.23	27.36	24.80	
3E		4-LUTs	1 615	1 816	2 131	2 184	2 295	2 383	2 474	
	-5	Registers	458	533	594	637	679	721	763	
		Speed (MHz)	37.27	37.71	32.51	32.34	29.51	30.26	29.29	
Spartan 3A		4-LUTs	1 629	1 832	2 139	2 191	2 304	2 396	2 489	
3A	-4	Registers	459	534	595	638	680	722	764	
		Speed (MHz)	31.23	31.05	29.08	26.45	26.39	24.87	24.47	
	-5	4-LUTs	1 622	1 827	2 138	2 187	2 302	2 388	2 483	
		Registers	459	534	595	638	680	722	764	
		Speed (MHz)	36.03	36.14	33.50	30.65	30.79	29.70	27.70	

		4-LUTs	1 628	1 831	2 140	2 197	2 310	2 402	2 497
	-4	Registers	459	534	595	638	680	722	764
Spartan		Speed (MHz)	31.18	31.26	29.51	26.61	26.48	24.30	24.56
3A DSP		4-LUTs	1 621	1 826	2 136	2 196	2 312	2 400	2 495
	-5	Registers	459	534	595	638	680	722	764
		Speed (MHz)	39.31	37.59	33.59	32.61	33.00	28.86	28.49
		6-LUTs	1 277	1 436	1 620	1 705	1 774	1 851	1 905
	-2	Registers	459	533	595	638	680	722	764
		Speed (MHz)	41.06	41.03	39.09	34.88	34.40	26.89	33.86
	-3	6-LUTs	1 271	1 425	1 603	1 685	1 753	1 829	1 876
Spartan 6		Registers	459	533	595	638	680	722	764
		Speed (MHz)	58.19	58.21	50.01	46.45	45.84	41.76	43.33
	-4	6-LUTs	1 267	1 424	1 603	1 681	1 750	1 828	1 873
		Registers	459	533	595	638	680	722	764
		Speed (MHz)	64.96	67.62	57.38	51.11	50.07	42.97	43.61
		4-LUTs	1 629	1 829	2 151	2 200	2 305	2 395	2 490
	-10	Registers	459	534	595	638	680	722	764
		Speed (MHz)	50.12	51.17	45.61	43.60	41.67	42.34	39.18
		4-LUTs	1 632	1 810	2 152	2 202	2 307	2 396	2 491
Virtex 4	-11	Registers	459	534	595	638	680	722	764
		Speed (MHz)	57.27	56.14	53.79	48.82	48.59	48.70	47.39
		4-LUTs	1 627	1 819	2 152	2 199	2 305	2 394	2 489
	-12	Registers	459	534	595	638	680	722	764
		Speed (MHz)	66.56	64.59	57.46	59.27	50.78	54.40	53.87

		6-LUTs	1 219	1 372	1 601	1 691	1 753	1 832	1 881
	-1	Registers	458	532	594	637	679	721	763
Virtex 5		Speed (MHz)	74.39	74.69	70.25	63.09	59.89	53.00	53.53
		6-LUTs	1 221	1 372	1 601	1 692	1 752	1 831	1 881
	-2	Registers	458	532	594	637	679	721	763
		Speed (MHz)	82.16	82.12	77.42	69.06	64.99	58.40	70.06
	-3	6-LUTs	1 215	1 367	1 602	1 692	1 751	1 831	1 882
		Registers	458	532	594	637	679	721	763
		Speed (MHz)	97.85	97.25	85.67	72.33	76.99	71.20	69.05
	-1	6-LUTs	1 237	1 390	1 585	1 673	1 746	1 818	1 866
		Registers	458	532	594	637	679	721	763
		Speed (MHz)	89.32	92.59	87.64	68.59	77.03	73.56	66.47
		6-LUTs	1 235	1 388	1 582	1 668	1 737	1 816	1 860
Virtex 6	-2	Registers	458	532	594	637	679	721	763
		Speed (MHz)	102.40	97.51	98.05	86.74	79.95	77.19	74.94
		6-LUTs	1 234	1 387	1 579	1 668	1 737	1 815	1 860
	-3	Registers	458	532	594	637	679	721	763
		Speed (MHz)	111.74	115.71	102.04	88.93	89.90	84.47	90.80

2.1.2 Altera

				ope	nMSP430 Co	nfigura	tion		
FPGA Device	Speed Grade	Info	No Debug	No Debug with HW multiplier	With debug interface (no HW breakpoints)	har	debug dware un		
						1	2	3	4
		LEs	1 552	1 785	2 040	2 179	2 286	2 418	2 507
	-6	Registers	467	537	610	653	695	737	779
		Speed (MHz)	45.10	47.32	42.79	43.81	41.57	42.10	40.71
		LEs	1 556	1 781	2 049	2 191	2 298	2 414	2 508
Cyclone II	-7	Registers	467	537	610	653	695	737	779
		Speed (MHz)	40.53	40.24	37.39	38.39	34.23	35.54	33.96
	-8	LEs	1 555	1 779	2 047	2 192	2 290	2 406	2 524
		Registers	467	537	610	653	695	737	779
		Speed (MHz)	33.07	32.97	32.00	30.62	29.78	29.63	26.38
	-6	LEs	1 539	1 752	2 021	2 148	2 251	2 357	2 450
		Registers	467	537	610	653	695	737	779
		Speed (MHz)	51.87	54.11	48.26	49.95	48.39	48.43	45.61
		LEs	1 539	1 750	2 022	2 147	2 244	2 363	2 443
Cyclone III	-7	Registers	467	537	610	653	695	737	779
		Speed (MHz)	46.25	43.88	44.28	41.64	39.18	40.59	40.86
		LEs	1 542	1 752	2 020	2 158	2 243	2 380	2 448
	-8	Registers	467	537	610	653	695	737	779
		Speed (MHz)	40.56	38.68	38.0	38.38	33.94	33.57	32.86
Cyclone IV GX	-6	LEs	1 541	1 750	2 024	2 148	2 246	2 364	2 459
GA		Registers	467	537	610	653	695	737	779

		Speed (MHz)	50.58	51.77	51.16	49.6	47.38	47.07	46.67
		LEs	1 540	1 749	2 024	2 148	2 247	2 366	2 448
	-7	Registers	467	537	610	653	695	737	779
		Speed (MHz)	47.09	44.19	44.43	42.63	42.49	41.6	39.03
		LEs	1 544	1 747	2 020	2 147	2 244	2 363	2 444
	-8	Registers	467	537	610	653	695	737	779
		Speed (MHz)	40.09	37.67	39.76	36.86	37.27	34.69	37.03
		ALUTs	1 044	1 160	1 414	1 525	1 588	1 675	1 765
Arria GX	-6	Registers	468	539	612	656	708	744	791
		Speed (MHz)	48.71	49.23	44.58	44.38	41.88	42.51	42.18
		ALUTs	1 031	1 146	1 407	1 507	1 577	1 668	1 754
	-4	Registers	469	540	611	654	706	749	793
		Speed (MHz)	84.37	83.22	78.81	75.19	75.75	76.3	79.81
		ALUTs	1 025	1 148	1 404	1 503	1 600	1 670	1 742
Arria II GX	-5	Registers	467	539	612	654	708	744	805
		Speed (MHz)	76.17	72.65	68.86	65.58	67.96	66.81	65.35
		ALUTs	1 032	1 143	1 403	1 506	1 590	1 677	1 755
	-6	Registers	469	539	611	659	704	753	793
		Speed (MHz)	62.63	61.59	59.66	57.2	55.76	59.04	57.41
Stratix		LEs	1 525	1 730	1 989	2 081	2 185	2 279	2 378
	-5	Registers	_	-	-	_	_	-	_
		Speed (MHz)	44.00	43.38	43.64	42.92	40.58	41.70	39.71
	-6	LEs	1 525	1 730	1 989	2 081	2 185	2 279	2 378
		Registers	-	-	-	_	_	_	-
		Speed (MHz)	39.88	40.74	39.82	37.18	37.42	36.97	36.81

		LEs	1 525	1 730	1 989	2 081	2 185	2 279	2 378
		DES		1 /30	1 707	2 001	2 103		2 370
	-7	Registers	_	-	-	_	-	_	-
		Speed (MHz)	32.97	34.67	33.27	32.83	33.06	31.54	30.66
		ALUTs	1 040	1 145	1 422	1 523	1 590	1 665	1 753
	-3	Registers	469	540	610	655	698	739	783
		Speed (MHz)	73.79	73.28	72.38	65.89	67.11	66.09	65.75
		ALUTs	1 039	1 157	1 424	1 529	1 601	1 671	1 762
Stratix II	-4	Registers	469	540	613	658	699	741	781
		Speed (MHz)	63.75	63.29	60.31	58.10	56.84	59.57	59.26
		ALUTs	1 039	1 155	1 419	1 527	1 592	1 678	1 763
	-5	Registers	469	541	617	655	698	741	783
		Speed (MHz)	54.04	54.82	51.89	50.81	49.89	50.02	49.31
		ALUTs	1 029	1 147	1 408	1 511	1 597	1 666	1 748
	-2	Registers	468	538	611	656	702	752	799
		Speed (MHz)	93.84	97.68	89.59	84.5	86.24	86.72	85.01
		ALUTs	1 033	1 142	1 414	1 506	1 588	1 675	1 754
Stratix III	-3	Registers	469	539	610	656	699	753	807
		Speed (MHz)	83.68	80.16	75.77	71.9	76.64	73.49	75.35
		ALUTs	1 030	1 147	1 411	1 505	1 587	1 670	1 760
	-4	Registers	469	539	614	654	700	754	803
		Speed (MHz)	73.17	72.42	72.63	66.91	68.49	65.19	68.43

2.1.3 Actel

				opei	nMSP430 Con	ıfigura	tion		
FPGA Device	Speed Grade	Info	No Debug	No Debug with HW multiplier	With debug interface (no HW breakpoints)		dware	g interf breakp its)	
				1 1		1	2	3	4
		Tiles	3 585	4 734	4 884	5 014	5 263	5 571	5 747
	Std	Registers	479	550	623	666	709	750	793
		Speed (MHz)	16.81	16.14	13.98	16.22	16.66	14.89	15.24
		Tiles	3 635	4 585	4 742	5 004	5 246	5 345	5 713
ProASIC3E	-1	Registers	479	552	624	667	708	750	793
		Speed (MHz)	18.01	18.97	17.92	16.03	19.03	19.08	18.29
	-2	Tiles	3 556	4 573	4 811	5 002	5 210	5 446	5 625
		Registers	479	553	623	666	707	750	792
		Speed (MHz)	22.45	20.84	21.42	21.24	24.01	22.85	19.45
		Tiles	3 549	4 665	4 774	5 012	5 183	5 453	5 638
	Std	Registers	480	552	623	667	709	750	792
ProASIC3L		Speed (MHz)	14.31	14.27	15.14	14.42	14.74	14.15	14.05
TIOASICSL		Tiles	3 535	4 595	4 776	5 032	5 174	5 418	5 706
	-1	Registers	479	551	623	666	708	750	793
		Speed (MHz)	18.13	17.31	15.90	18.34	17.14	17.69	16.27
ProASIC3		Tiles	3 585	4 734	4 884	5 014	5 263	5 571	5 747
	Std	Registers	479	550	623	666	709	750	793
		Speed (MHz)	16.47	15.62	15.03	16.55	16.00	14.63	15.38
	-1	Tiles	3 635	4 585	4 742	5 004	5 246	5 345	5 713
		Registers	479	552	624	667	708	750	793

		Speed (MHz)	18.03	19.21	18.39	18.40	18.95	17.13	18.59
		Tiles	3 556	4 573	4 811	5 002	5 210	5 446	5 625
	-2	Registers	479	553	623	666	707	750	792
		Speed (MHz)	22.80	21.97	21.67	21.24	22.57	23.27	20.75
		Tiles	3 646	4 844	4 857	5 016	5 214	5 467	5 739
IGLOOe	Std	Registers	479	552	623	666	709	751	791
		Speed (MHz)	14.01	14.51	13.61	13.85	14.29	14.44	14.10
		Tiles	3 585	4 734	4 884	5 014	5 263	5 571	5 747
Fusion	Std	Registers	479	550	623	666	709	750	793
		Speed (MHz)	16.65	15.84	14.25	15.60	15.62	15.20	15.50
	-1	Tiles	3 635	4 585	4 742	5 004	5 246	5 345	5 713
		Registers	479	552	624	667	708	750	793
		Speed (MHz)	17.90	18.46	17.79	17.86	17.81	18.69	17.98
	-2	Tiles	3 556	4 573	4 811	5 002	5 210	5 446	5 625
		Registers	479	553	623	666	707	750	792
		Speed (MHz)	22.30	21.34	20.58	20.27	21.48	21.39	20.59

2.2 ASICs

2.2.1 180nm

Target Frequency	Info	openMSP430 Configuration								
		No Debug	No Debug with HW multiplier	With debug interface (no HW	With debug interface (# hardware breakpoint units)					
				breakpoints)	1	2	3	4		
25 MHz	kgates	8 042	10 457	9 995	10 744	11 487	12 189	12 905		
	μm²	80 256	104 352	99 742	107 223	114 637	121 643	128 784		
	timing	clean	clean	clean	clean	clean	clean	clean		
33 MHz	kgates	8 039	10 458	9 976	10 839	11 584	12 293	13 022		
	μm²	80 226	104 365	99 552	108 164	115 602	122 677	129 956		
	timing	clean	clean	clean	clean	clean	clean	clean		
50 MHz	kgates	8 187	10 753	10 149	11 189	11 929	12 651	13 405		
	μm²	81 703	107 305	101 285	111 660	119 048	126 253	133 778		
	timing	clean	clean	clean	clean	clean	clean	clean		
66 MHz	kgates	8 535	11 837	10 591	12 042	12 873	13 489	14 299		
	μm²	85 172	118 130	105 693	120 176	128 465	134 606	142 692		
	timing	clean	clean	clean	clean	clean	clean	clean		
100 MHz	kgates	10 019	14 468	12 095	14 386	15 197	16 027	16 936		
	μm ²	99 988	144 382	120 698	143 560	151 660	159 936	169 014		
	timing	clean	-0.98 ns	clean	clean	clean	clean	clean		
125 MHz	kgates	11 851	16 142	13 838	16 502	17 209	17 660	18 718		
	μm²	118 270	161 087	138 095	164 676	171 738	176 229	186 793		
	timing	-0.75 ns	-2.85 ns	-0.62 ns	-1.46 ns	-1.66 ns	-1.81 ns	-1.81 ns		