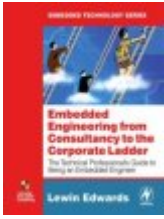




## Yamaha YM2203 FM Operator Type-N (OPN)



My **third book** is released! Learn what you'll need to know in order to become an embedded engineer.

The YM2203 is a chip of considerable interest to the arcade game emulator writer, because it's just about THE most common audio synth chip used on arcade boards.

This document was obtained from Yamaha Systems Technology's faxback service. To save everybody else in the world from calling the USA and requesting a 14-page fax, I have transcribed the text portions here. I have not reproduced the diagrams. Also note that the original document's tables were apparently drawn by hand; while I was typing it in, I had to estimate the bitfield widths in the register maps. I have also preserved the original English.

This information is just a datasheet, not a complete programmer's reference manual. Recommended reading to understand this document is the General Instruments datasheet for the AY-3-8910A. Tandy Electronics packaged the GI chip and retailed it with a very detailed application manual which is also good reading.

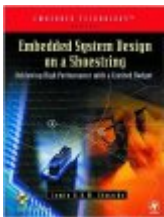


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### • OUTLINE

OPN (FM OPERATOR TYPE-N) is a new type synthesizer which can produce all sounds required owing to the FM sound source system. It is provided with a built-in register which can store sound information and be connected easily with a microprocessor or microcomputer. It also comprises a square wave sound source different from the sound source according to the FM system and a noise generator.



My **first book** gives you all the intro you need on developing 32-bit embedded systems on a hobbyist budget.

### • FEATURES

- The FM system sound source produce three different sounds simultaneously.
- One of the above three sounds can be set to the mode by which specific sound effects and composite sine wave sound are synthesized.
- Two programmable timers are incorporated.
- 8 bits general purpose input/output ports of two system are incorporated.
- Three square wave sounds and white noise can be produced in addition to the FM system sounds.
- Clock divider is built in so that wide operating frequency range is obtained.
- Input and output are compatible with TTL.
- Nch-Si gate MOS LSI is used.
- Single phase power source of 5V is used.
- This is compatible with software of YM2149 and AY-3-8910 and 8912 produced by GI.

### • TERMINAL DIAGRAM

GND	1	40	D0
D1	2	39	øS
D2	3	38	øM
D3	4	37	A0
D4	5	36	_RD
D5	6	35	_WR
D6	7	34	_CS
D7	8	33	IOB7
IOA7	9	32	IOB6
IOA6	10	31	IOB5

IOA5	11	30	IOB4
IOA4	12	29	IOB3
IOA3	13	28	IOB2
IOA2	14	27	IOB1
IOA1	15	26	IOB0
IOA0	16	25	_IRQ
AGND	17	24	_IC
ANALOG CHANNEL C	18	23	OP-O
ANALOG CHANNEL B	19	22	SH
ANALOG CHANNEL A	20	21	V <sub>DD</sub>

## • BLOCK DIAGRAM

Not available in online version.

## • DESCRIPTION OF TERMINAL FUNCTION

### 1. $\phi M$

This is the master clock of the OPN. The FM sound source and square wave sound source operate, based on this clock. The maximum input frequency up to 4.2MHz can be input by using a built-in 1/6 divider.

### 2. $\phi S$ , SH

These are the clock ( $\phi S$ ) and the synchronous signal (SH). They drive a D/A converter which converts digital output of the FM sound source into analog output.

### 3. D0 through D7

These 8-bit bi-directional bus exchange the data and address between the OPN and the micro-processor.

### 4. \_CS, \_RD, \_WR, A0

These signals control bi-directional bus of D0 through D7.

_CS	_RD	_WR	A0	
0	1	0	0	Writes address into the register of the OPN.
0	1	0	1	Writes the register content into the OPN.
0	0	1	0	Reads the OPN status.
0	0	1	1	Reads the content of the OPN register.
1	x	x	x	D0 through D7 bus line become high impedance.

\* Read enable register addresses 00 through 0F (16 bits).

### 5. \_IRQ

This is an interrupt signal sent from two timers. It can be masked by the program.

### 6. \_IC

This signal resets the system at low level. All the content of register array become "0".

### 7. OP-O

This outputs the FM modulated audio signal as 13-bit serial data. Accordingly, an external D/A converter is necessary.

### 8. Analog channel A, B and C

They are analog square wave audio signals. They can be mixed by setting resistance because of source follower.

### 9. IOA0 through IOA7, IOB0 through IOB7

They are two sets of 8-bit input/output ports. Each terminal incorporates pull up resistance.

### 10. AGND

This is analog ground terminal for the D/A converter which is built in the square wave sound source section.

### 11. V<sub>DD</sub>

This is a power terminal of +5V.

### 12. GND

This is a ground terminal.

## • DESCRIPTION OF FUNCTIONS

The OPN is controlled based on the data written into the register. Accordingly, a microprocessor is free from the sound control operation except sending the data to the register.

The FM sound source determines a sound by the combination (modulation) of full sine waves. All the modulation systems such as feedback FM, simple FM and multiple FM are possible. In respect to the square wave sound source, this is compatible with YM2149 (SSC) and AY-3-8910 and 8912 (PSG GI) in the use of the software. Therefore, function of the OPN can be improved by the exchange with the above LSI.

Each block of the OPN functions as follows.

- **Envelope generator (EG)**  
Determines the modulation index of the envelope and modulation wave of the FM sound source.
- **Phase generator (PG)**  
Determines the sine wave phase at each time step of the FM sound source.
- **Operator (OP)**  
Calculates the  $E \sin \theta$  value on the basis of the amplitude from the envelope generator and the phase from the phase generator.
- **Accumulator (ACC)**  
Accumulates and adds operator output of each channel to mix each sound of the FM sound source and matches with the D/A converter.
- **Square wave sound source/noise generator**  
Generates three different frequency square waves and pseudo-white noise. It can also mix noise and square wave. As for sound volume, it is possible to select either fixed sound volume (programmed value) or 10 pattern envelope producing mode. In this block, one D/A converter is provided for each sound.
- **Input/output port control**  
These are the general-purpose input/output ports to gets interface with external equipment.
- **Timer**  
Two types of timers are provided.

### Register content and address map

The OPN register is provided with the internal address as shown in the address map. The content of each register (address) is as follows.

(1)	\$00 ~ \$05	Generates frequency of the square wave sound source.
(2)	\$06	Generates frequency of noise source.
(3)	\$07	Controls the input and output of the input and output ports and the output of musical sound and noise.
(4)	\$08 ~ \$0A	Controls sound volume. It is possible to select the fixed sound volume system (programmable) or the variable sound volume system.
(5)	\$0B ~ \$0C	Controls the envelope cycle in the variable sound volume system.
(6)	\$0D	Specifies the envelope shape in the variable sound volume system.
(7)	\$0E ~ \$0F	8 bit general-purpose input and output ports.
(8)	\$21	Test information, always set to "0".
(9)	\$24 ~ \$26	Gives the set time of Timers A and B.
(10)	\$27	Controls the operation of Timers A and B, and sets the third channel mode of the FM sound source.
(11)	\$2D ~ \$2F	Specifies the dividing number of the input clock. The dividing numbers 2 through 6 are for the FM sound source, and the numbers 1 through 4 are for square wave sound source.
(12)	\$30 ~ \$3E	Controls Detune and Multiple. This is used to set tones. This controls the relationship between the fundamental wave and harmonic.

(13)	\$40 ~ \$4E	Gives the total level. This information becomes the modulation index of the sound volume and modulation wave of the modulated wave.
(14)	\$50 ~ \$5E	Key - Scale controls the rate of change of A - D - S and R according to the keyboard information. Attack rate gives the rate of change of the envelope at the time of attack.
(15)	\$60 ~ \$6E	Decay Rate shows the rate of change of the envelope at the time of decay.
(16)	\$70 ~ \$7E	Sustain Rate shows the rate of change of the envelope at the time of sustain.
(17)	\$80 ~ \$8E	Sustain level shows the level of the shift from decay to sustain. Release rate shows the rate of change of the envelope at the time of release.
(18)	\$90 ~ \$9E	Generates the envelope including the repeat pattern similar to that of square wave sound source.
(19)	\$A0 ~ \$A6	Gives key-code (F-number) of each channel.
(20)	\$A8 ~ \$AE	Gives the key-code (F-number) of three channels when set to the special mode.
(21)	\$B0 ~ \$B2	Gives the modulation system (connection) of the FM modulation and the modulation factor of the feedback FM (self-feedback).

### FM system

In the FM system, musical sounds are synthesized by controlling various high harmonic waves by use of the frequency modulation. The basic equation of the FM system is as follows.

$$\text{(Equation 1) } F = A \sin (\omega C t + I \sin \omega M t)$$

Where A is output amplitude, I is modulation index, and  $\omega C$  and  $\omega M$  are angular frequencies of carrier and modulator, respectively. This equation can also be expressed as follows.

$$\begin{aligned} \text{(Equation 2) } F = & A [J_0(I) \sin \omega C t + J_1(I) (\sin (\omega C + \omega M)t - \sin (\omega C - \omega M)t) \\ & + J_2(I) (\sin (\omega C + 2 \omega M)t - \sin (\omega C - 2 \omega M)t) \\ & + \dots ] \end{aligned}$$

Where,  $J_n(I)$  is the first class Bessel function of nth As shown in the above equation, the FM system contains various harmonics and can control them. The OPN provides the multiple FM modulation and feedback FM modulation shown in (3) and (4) in addition to the above FM modulation to produce every possible sound.

$$\text{(Equation 3) } F = A \sin [\omega C t + I_1 \sin (\omega M_1 t + I_2 \sin \omega M_2 t)]$$

$$\text{(Equation 4) } F = A \sin (\omega C t + \beta F)$$

### WRITE DATA

Address	Data Bits							Comment
21	TEST							LSI TEST DATA
24	TIMER-A							8 most significant bits of TIMER-A
25	not used					TIMER-A		2 least significant bits of TIMER-A
26	TIMER-B							TIMER-B data
27	MODE	RESET B	RESET A	ENABLE B	ENABLE A	LOAD B	LOAD A	TIMER-A/B control and 3 channel mode
28	SLOT			CH				Key-ON/OFF
2D	don't care							Set pre-scaler

2E	don't care			Selection of the dividing numbers of 1/3 and 1/6
2F	don't care			Set a divider to the dividing number of 1/2
30-3E	not used	DT	MULTI	Detune/Multiple (Addresses 33, 37, 3B are empty)
40-4E	not used	TL		Total Level (Addresses 43, 47, 4B are empty)
50-5E	KS	not used	AR	Key Scale/Attack Rate (Addresses 53, 57, 5B are empty)
60-6E	not used	DR		Decay Rate (Addresses 63, 67, 6B are empty)
70-7E	not used	SR		Sustain Rate (Addresses 73, 77, 7B are empty)
80-8E	SL		RR	Sustain Level/Release Rate (Addresses 83, 87, 8B are empty)
90-9E	not used		SSG-EG	SSG-Type Envelope Control (Addresses 93, 97, 9B are empty)
A0-A2	F-Num. 1			F-Numbers/BLOCK
A4-A6	not used	BLOCK	F-Num. 2	
A8-AA	3CH * F-Num. 1			3CH-3slot F-Numbers/BLOCK
AC-AE	not used	3CH * BLOCK	3CH * F-Num. 2	
B0-B2	not used	FB	CONNECT	Self-Feedback/Connection

**READ/WRITE DATA**

Address	Data Bits						Comment	
00	Fine Tune						Channel-A Tone Period	
01	not used			Coarse Tune				
02	Fine Tune						Channel-B Tone Period	
03	not used			Coarse Tune				
04	Fine Tune						Channel-C Tone Period	
05	not used			Coarse Tune				
06	not used			Period Control			Noise Period	
07	IN/OUT IOB	IN/OUT IOA	_NOISE	_TONE		_ENABLE		
08	not used		M	Level			Channel-A Amplitude	
09	not used		M	Level			Channel-B Amplitude	
0A	not used		M	Level			Channel-C Amplitude	
0B	Fine Tune						Envelope Period	
0C	Coarse Tune							
0D	not used			C	ATT	ALT	HLD	Envelope Shape/Cycle
0E	I/O Port-A						I/O Port Data	
0F	I/O Port-B							

**READ DATA**

Address	Data Bits	Comment
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xx	BUSY	not used	FLAG B	FLAG A	Status
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## • ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Rating

ITEM	RATING	UNIT
Terminal voltage	-0.3 ~ 7.0	V
Ambient operating temperature	0 ~ 70	°C
Storage temperature	-50 ~ 125	°C

### 2. Recommended Operation Conditions

ITEM	SYMBOL	MIN.	STD.	MAX.	UNIT
Supply voltage	Vdd	4.75	5.0	5.25	V
	Vss	0	0	0	V

### 3. DC Characteristics

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Input high level voltage	Total input	V <sub>IH</sub>		2.0		V <sub>DD</sub>	V
Input low level voltage	Total input	V <sub>IL</sub>		-0.3		0.8	V
Input leakage current	øM, _WR, _RD, A0	I <sub>L</sub>	V <sub>in</sub> = 0 ~ 5V	-10		10	µA
Three-state (off) input current	D0 ~ D7	I <sub>TSL</sub>	V <sub>in</sub> = 0 ~ 5V	-10		10	µA
Output high level voltage	Output except _IRQ	V <sub>OH1</sub>	I <sub>OH1</sub> = 0.4mA	2.4			V
		V <sub>OH2</sub>	I <sub>OH2</sub> = 40µA	3.3			V
Output leakage current (off)	_IRQ	I <sub>OL</sub>	V <sub>OH</sub> = 0 ~ 5V	-10		10	µA
Analog output voltage	ANALOG-CHA, B, C	V <sub>OA</sub>	Max. Sound volume, no mixing	0.95		1.35	V <sub>pp</sub>
Power current		I <sub>DD</sub>				120	mA
Pull-up resistance	IOA0 ~ IOA7, IOB0 ~ IOB7, _IC, _CS	R <sub>PU</sub>		60		600	k
Input capacitance	Total input	C <sub>i</sub>	f = 1MHz			10	pF
Output capacitance	Total output	C <sub>o</sub>				10	pF

### 4. AC Characteristics

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Input clock frequency	øM	f <sub>c</sub>	Pre-scaler function (Fig. A-1)	0.7		4.2	MHz
Input clock duty	øM			40	50	60	%
Input clock rise time	øM	T <sub>R</sub>	(Fig. A-1)			50	ns
Input clock breaking time	øM	T <sub>F</sub>	(Fig. A-1)			50	ns

### 5. Access to FM sound source

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Address set-up time	A0	T <sub>AS</sub>	(Figs. A-2 and A-3)	10			ns
Address hold time	A0	T <sub>AH</sub>	(Figs. A-2 and A-3)	10			ns
Chip select write width	_CS	T <sub>CSW</sub>	(Fig. A-2)	200			ns
Chip select read	_CS	T <sub>CSR</sub>	(Fig. A-3)	250			ns

width							
Write pulse write width	_WR	T <sub>WW</sub>	(Fig. A-2)	200			ns
Write data set-up time	D0 ~ D7	T <sub>WDS</sub>	(Fig. A-2)	100			ns
Write data hold time	D0 ~ D7	T <sub>WDH</sub>	(Fig. A-3)	20			ns
Read pulse width	_RD	T <sub>RW</sub>	(Fig. A-3)	250			ns
Read data access time	D0 ~ D7	T <sub>ACC</sub>	C <sub>L</sub> = 100pF (Fig. A-3)			250	ns
Read data hold time	D0 ~ D7	T <sub>RDH</sub>	(Fig. A-3)	10			ns
Output rise time	øS	T <sub>OR1</sub>	C <sub>L</sub> = 100pF (Fig. A-4)			200	ns
	OP-O, SH	T <sub>OR2</sub>	C <sub>L</sub> = 100pF (Fig. A-5)			300	ns
Output rise time	øS	T <sub>OF1</sub>	C <sub>L</sub> = 100pF (Fig. A-4)			200	ns
	OP-O, SH	T <sub>OF2</sub>	C <sub>L</sub> = 100pF (Fig. A-5)			300	ns

## 6. Access to SSG sound source

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Address set-up time	A0	T <sub>SAS</sub>	(Figs. A-7 and A-8)	10			ns
Address hold time	A0	T <sub>SAH</sub>	(Figs. A-7 and A-8)	10			ns
Chip select write width	_CS	T <sub>SCSW</sub>	(Fig. A-7)	250			ns
Chip select read width	_CS	T <sub>SCSR</sub>	(Fig. A-8)	400			ns
Write pulse write width	_WR	T <sub>SWW</sub>	(Fig. A-7)	250			ns
Write data set-up time	D0 ~ D7	T <sub>SWDS</sub>	(Fig. A-7)	0			ns
Write data hold time	D0 ~ D7	T <sub>SWDH</sub>	(Fig. A-7)	20			ns
Read pulse width	_RD	T <sub>SRW</sub>	(Fig. A-8)	400			ns
Read data access time	D0 ~ D7	T <sub>SACC</sub>	C <sub>L</sub> = 100pF (Fig. A-8)			400	ns
Read data hold time	D0 ~ D7	T <sub>SRDH</sub>	(Fig. A-8)	10			ns

ITEM		SYMBOL	CONDITIONS	MIN.	STD.	MAX.	UNIT
Reset pulse width	_IC	T <sub>ICW</sub>	(Fig. A-9)	73*			cycle

\* Depends on the dividing number of prescaler. Pulse width = (dividing number) x 12

## • TIMING DIAGRAM

(Timing is set on the basis of the values: V<sub>IH</sub> = 2.0V and V<sub>IL</sub> = 0.8V).

- **Fig. A-1 Clock Timing**  
(figure not available online)
- **Fig. A-2 FM section write timing**  
(figure not available online)  
**Note.** T<sub>CSW</sub>, T<sub>WW</sub> and T<sub>WDH</sub> are determined based on the time when either \_CS or \_WR goes to the high level.
- **Fig. A-3 FM section read timing**  
(figure not available online)  
**Note.** T<sub>AAC</sub> is determined based on the time when either \_CS or \_RD goes to the low level. T<sub>CSR</sub>, T<sub>RW</sub> and T<sub>RDH</sub> are determined based on the time when either \_CS or \_RD goes to the high level.
- **Fig. A-4 -a øM and øS (dividing numbers: 2 and 3)**  
(figure not available online)



- **Fig. A-4-b  $\phi$ M and  $\phi$ S (dividing number: 6)**  
(figure not available online)
- **Fig. A-5  $\phi$ M and SH . OP-O**  
(figure not available online)
- **Fig. A-6 Timing of  $\phi$ S and OP-O/CH at each dividing number**  
(figure not available online)
- **Fig. A-7 SSG section write timing**  
(figure not available online)  
**Note.** TSWDS is determined based on the time when either \_CS or \_WR goes to the low level. TSCW, TSWW and TSWDH are determined based on the time when either \_CS or \_WR goes to the high level.
- **Fig. A-8 SSG section read timing**  
(figure not available online)  
**Note.** TSACC is determined based on the time when either \_CS or \_RD goes to the low level. TSCSR, TSRW and TSRDH are determined based on the time when either \_CS or \_RD goes to the high level.
- **Fig. A-9 Reset pulse**  
(figure not available online)

## • OUTER DIMENSION DRAWING

(figure not available online)

The specifications of this product are subject to improvement changes without prior notice.

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