Version. 1.12

YAMAHA

LSI

YM2610

Application Manual

OPNB 6-ch,4-OP.FM + SSG + ADPCM sound generator

1995/1/20

YM2610

FM Operator Type-NB(OPNB)

■ Summary

OPNBは、FM音源方式を採用することにより、新しいタイプのシンセサイザーとしての威力をもち、あらゆる音に対応することができます。 Additionally, it can be easily connected to a microcomputer or microprocessor, and contains built-in registers for storing tone information.

さらにOPNBは、FM方式の音源とは異なった矩形波の音源およびnoise発生器に加えて
ADPCM音源部が内蔵されています。

■ Features

●FM方式の音源を採用し、4音同時発生が可能であり、4音をそれぞれ異色音にす
ることができる。

● 4 sounds, 1 of which can be complex sine wave speech synthesis

● Two built-in programmable timers

● Built-in LFO functionality

● In addition to FM synthesis and SSG (square wave generation), ADPCM output is possible.

●FM音源部及びADPCM-A音源と同B音源にLR出力制御機能あり

● Nch-Si Gate MOS LSI

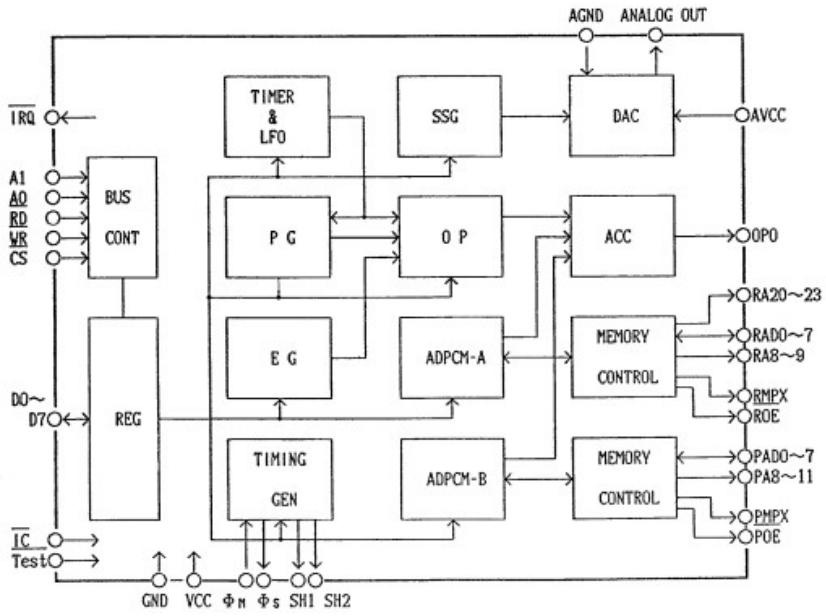
● 5V single power supply

● 64 pins

1. Summary

OPNB has two types of ADPCM output, LR出力を可能にしたものであり主な
Features:
1.FM tone generator 4 channels
2.Additional LFO functions
3.Left/Right Output
4.ADPCM-A tone generator ・6 channel polyphony
・External Memory Bankswitching up to 16 MB
5.ADPCM-B tone generator ・1 channel
・Variable Sampling Rate
(1.8KHz～55.5KHz)
・External Memory 最大連続16MBまで可能

2．ブロック図



3. Major Functions

(a) FM tone generator

Channels	:	4
Operators	:	4
Algorithms	:	8
LFO function	:	Amplitude, Frequency Modulation, Modulation Existence, LFO Freqency can be set.
複合 Sine Wave Speech Synthesis	:	4音中1音可能
Timers	:	Type A, Type B
LR Output Control	:	Can be controlled by On/Off
Compatible DAC	:	YM3016 (16 pins)

(B) SSG tone generator

Polyphony	:	3 Square Waves and White Noise
Analog Output	:	Converted to analog by built-in DAC, then the output is mixed to 1 terminal.

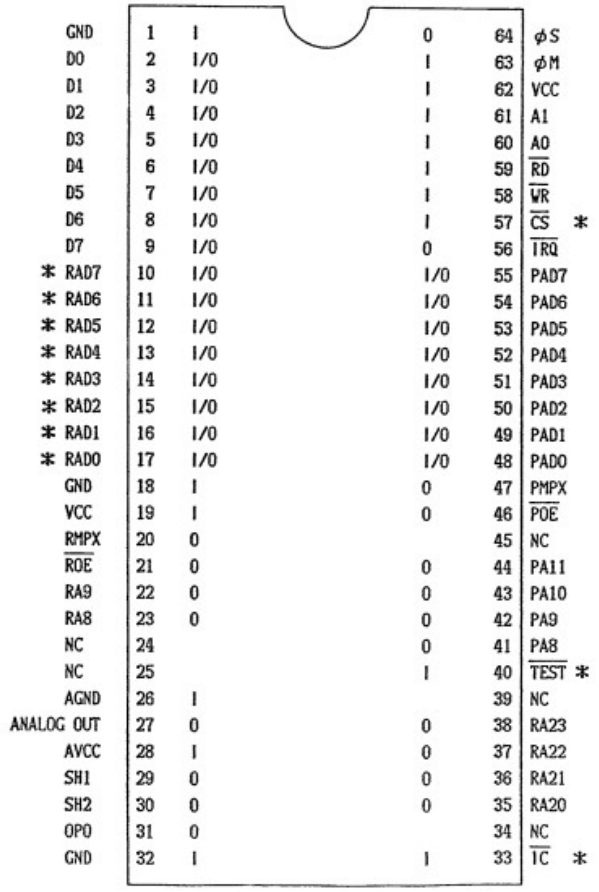
(c) ADPCM-A tone generator

ADPCM-A bit depth	:	4 bits
Channels	:	6
Sampling Rate	:	18.5KHz
Sound Data ROM	:	外部ROMにより最大連続1Mバイト/6音 Up to 16MB possible with bank switching
Start Address	:	外部より設定可能 Resolution 256 bytes
End Address	:	外部より設定可能 Resolution 256 bytes
Key On, Dump	:	Event-driven
Channel Level	:	Can be controlled for each channel
Output Level	:	Can control the level of all channels at the same time
LR Output Control	:	Can be controlled by On/Off

(B) ADPCM-B tone generator

ADPCM-B bit depth	:	4 bits
Channels	:	1
Sampling Rate	:	1.8～55.5KHz
Sound Data ROM	:	外部ROMにより最大連続16Mバイトまで可能
Start Address	:	外部より設定可能 Resolution 256 bytes
End Address	:	外部より設定可能 Resolution 256 bytes
Linear interpolation rate	:	55.5KHz
Output Level	:	Controllable
Repeat Play	:	Possible
LR Output Control	:	Can be controlled by On/Off

4．端子配置図



注：・本図はＴＯＰ　ＶＩＥＷ
・＊印の端子はプルアップ抵抗でVCCにプルアップされています。
・（ＮＣ）は無接続端子を示す。（無接続にてご使用ください）

5. Pin Description

Φm (I) : Master Clock. 8MHz.

Φs,SH1,SH2 (I) : DA Converter Clock (Φs) and Synchronization Signals (SH1,SH2).

OPO (I) : FM, ADPCM-A, ADPCM-B serial data output.

D0～D7 (I/O) : 8bit bi-directional data bus. プロセッサとデータのやり取りをします。

$\overline{CS}$,$\overline{RD}$,$\overline{WR}$,A1,A0(I) : D0～D7 data bus control. (See next page)

$\overline{IRQ}$ (O) : Interrupt signal. Open drain output.

ANALOG OUT (O) : SSG部のanalog出力です。ソースフォロワ出力。

RAD0～RAD7 (I/O) : ADPCM-A音源用ROMアドレス出力及びROMからのデータ入力です。

RA8～RA9 (O) : ADPCM-A sound ROM address output.

RA20～RA23 (O) : ADPCM-A sound ROM bankswitching.

RMPX (O) : ADPCM-A sound ROM address (lower 10 bits, upper 10 bits) latch.

$\overline{ROE}$ (O) : ADPCM-A音源用ROMのアウトプットイネーブル用です。

PAD0～PAD7 (I/O) : ADPCM-B音源用ROMのアドレス出力及びROMからのデータ入力です。

PA8～PA11 (O) : ADPCM-B音源用ROMのアドレス出力です。

PMPX (O) : ADPCM-B sound ROM address (lower 12 bits, upper 12 bits) latch.

$\overline{POE}$ (O) : ADPCM-B音源用ROMのアウトプットイネーブル用です。

$\overline{IC}$ (I) : Initialization input.

$\overline{TEST}$ (I) : Test input.

GND,AGND (I) : Ground pin.

VCC,AVCC (I) : +5V power supply pin.

■ Data Bus Control

レジスタのアドレスやデータのリード、ライトなどのデータバスコントロールは、$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A1 ,A0の各信号で行います。

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Addr.Range	Description
0	1	0	0	0	$00 - $28	SSG,Timer,ADPCM-B,etc. addr. write
					$30 - $B6	FM channel 1,2 address write
0	1	0	0	1	$00 - $28	SSG,Timer,ADPCM-B,etc. data write
					$30 - $B6	FM channel 1,2 data write
0	1	0	1	0	$00 - $2D	ADPCM-A address write
					$30 - $B6	FM channel 3,4 address write
0	1	0	1	1	$00 - $2D	ADPCM-A data write
					$30 - $B6	FM channel 3,4 data write
0	0	1	0	0	$XX	Status 0 data read
0	0	1	0	1	$00 - $0D	SSG data read
0	0	1	1	0	$XX	Status 1 data read
1	X	X	X	X	$XX	D0-D7 is high impedance

6. Electrical Characteristics

1. Absolute Maximum Rating

Item	Rated Value	Units
Terminal Voltage	-0.3～7.0	V
Operating Ambient Temp.	0～70	℃
Storage Temp.	-50.125	℃

2. Recommended operating conditions

Item	Symbol	Minimum	Standard	Maximum	Units
Power supply voltage	Vcc	4.75	5.0	5.25	V
	GND	0	0	0	V

3. DC Characteristics (Vcc＝5v±5%, Too＝0～70℃)

I t e m	Symbol	Conditions	Minimum	Maximum	Unit
Input High Level Voltage	All Inputs	VIH		2.0	Vcc	V
Input Low Level Voltage	All Inputs	VIL		-0.3	0.8	V
クロック入力 HighLevel電圧	φM	VCH		2.0	Vcc	V
クロック入力 LowLevel電圧	φM	VCL		-0.3	0.8	V
入力リーク電圧	φM, $\overline{WR}$, RD, A0, A1	IL	VIN=0～5V	-10	10	μA
スリーステート入力電源 (オフ状態)	D0～D7	ITSL	VIN=0～5V	-10	10	μA
出力HighLevel電圧	$\overline{IRQ}$を除く出力	VOH	IOH=0.4mA	2.4		V
出力LowLevel電圧	全出力	VOL	IOL=2mA		0.4	V
出力リーク電圧 (オフ状態)	$\overline{IRQ}$	IOL	VOH=0～5V	-10	10	V
アナログ出力電圧	ANALOG OUT	VOA	最大音量 3音同時 RL=470Ω	0.8	1.1	Vpp
電源電流		ICC			200	mA
プルアップ抵抗	RAD0～RAD7, TEST	RPU		60	600	kΩ

	$\overline{IC}$, $\overline{CS}$					
入力容量	全入力	CI	f=1MHz		10	PF
出力容量	全出力	CO			10	PF

4. AC Characteristics

項目	記号	条件	最小	標準	最大	単位
入力クロック周波数	φM	fc	(Fig.1)	7.5	8.0	8.5	MHz
入力クロックデューティ	φM			40	50	60	%
入力クロック立上り時間	φM	TCR	(Fig.1)			30	nS
入力クロック立下り時間	φM	TCF	(Fig.1)			30	nS
アドレスセットアップ時間	A0,A1	TAS	(Fig.2,3)	10			nS
アドレスホールド時間	A0,A1	TAH	(Fig.2,3)	10			nS
チップセレクトライト幅	$\overline{CS}$	TCSW	(Fig.2)	380			nS
チップセレクトリード幅	$\overline{CS}$	TCSR	(Fig.3)	380			nS
ライトパルス幅	$\overline{WR}$	TWW	(Fig.2)	380			nS
ライトデータセットアップ時間	D0～D7	TWDS	(Fig.2)	10			nS
ライトデータホールド時間	D0～D7	TWDH	(Fig.2)	30			nS
リードパルス幅	$\overline{RD}$	TRW	(Fig.3)	380			nS
リードデータアクセス時間	D0～D7	TACC	(Fig.3)			380	nS
リードデータホールド時間	D0～D7	TRDH	(Fig.3)	10			nS
リセットパルス幅	$\overline{IC}$	TICW	(Fig.4)	192			Cycle
メモリーデータセット時間	PAD0～PAD7 RAD0～RAD7	TMDS	(Fig.5,6)	70			nS

メモリーデータホールド時間	PAD0～PAD7 RAD0～RAD7	TMDH		10			nS
アウトプット立上り時間	SH1,SH2 OP0 ___ RMPX,ROE RA8,RA9 RA20～RA23 RAD0～RAD7 PMPX,POE PA8～PA11 PAD0～PAD7 φs	TOR	CL=100PF(Fig.7)			300	nS
アウトプット立下り時間	SH1,SH2 OP0 ___ RMPX,ROE RA8,RA9 RA20～RA23 RAD0～RAD7 PMPX,POE PA8～PA11 PAD0～PAD7 φs	TOF	CL=100PF(Fig.7)			300	nS

7. タイミング図

（タイミング図の設定は $V_H = 2.0V$, $V_L = 0.8V$ を基準とする。）

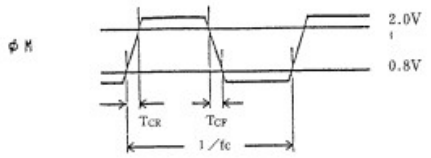
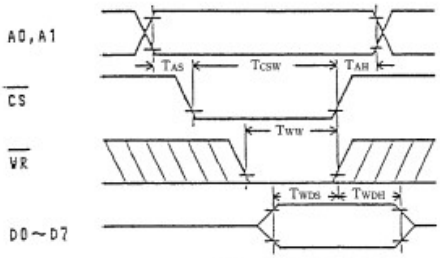
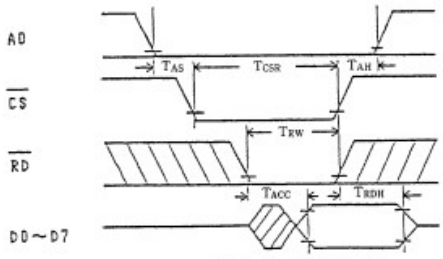


図1　クロックタイミング



(注)
TCSW, TWW, TWDS, TWDHは、CS, WRの何れかがHIGHレベルになる時を基準とする。

図2　ライトタイミング



(注)
TACCは、CS, WRの何れかが遅くLOWレベルになる時を基準とする。

TCSR, TRW, TRDHは、CS, WRの何れかがHIGHレベルになる時を基準とする。

図3　リードタイミング

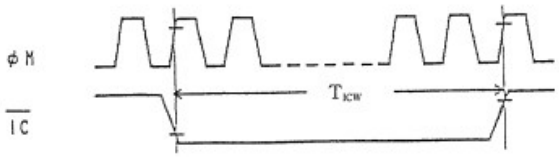
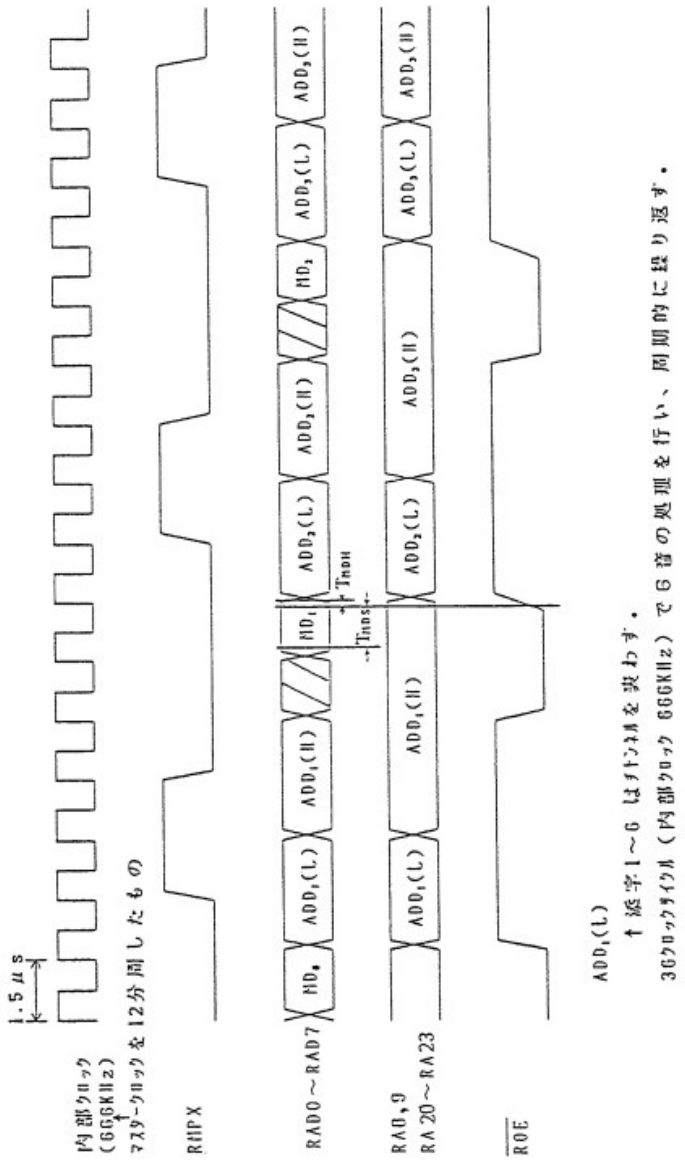


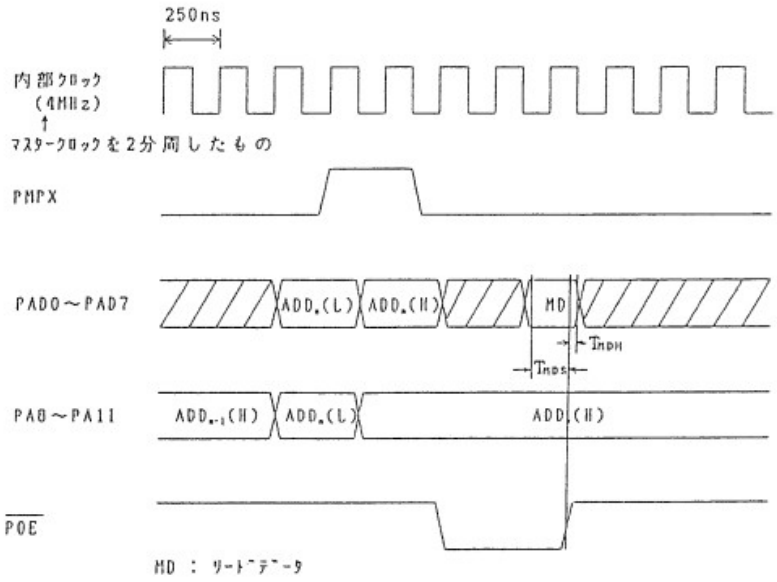
図4　リセットパルス幅

図5 ADPCM-A メモリーリードサイクル



ADD1(L)
↑終了1～6はチャンネルを表わす。
3Cクロックサイクル（内部クロック 666KHz）で6音の処理を行い、周期的に繰り返す。

図6 ADPCM-B メモリーリードサイクル



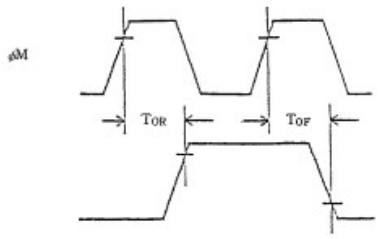
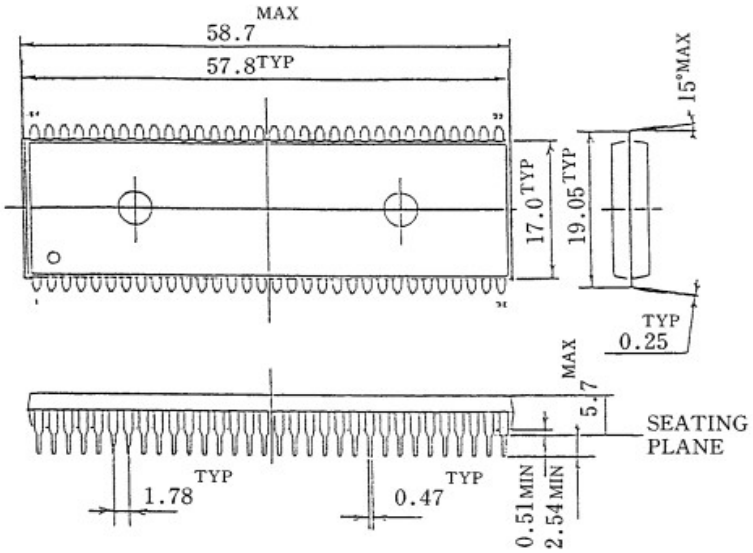


図 7 出力タイミング

8. 外 形 図



DIMMENSIONS IN MM

9. Functional Overview (1)

(a)Register Writing

When writing to the registers, first set the address, then send the data. (The order must always be address followed by data). However, if you're accessing the same address multiple times, you may write the address first and procceed to write the data register multiple times.

After writing to the address or data registers, you must wait before accessing them again. The wait time differs between address and data writes.

Wait Time

after addr. write	17 cycles
after data write	83 cycles

The number of cycles is based on the master clock.

(B)ADPCM Register Initial Values

Cleared at initialization time(IC="0"), register initial values are as follows:

ADPCM-A ADDRESS	REGISTER	Init.Value	ADPCM-B ADDRESS	REGISTER	Init.Value
00	DUMP/ADPCM-A ON	"00"	10	CONTROL 1	"00"

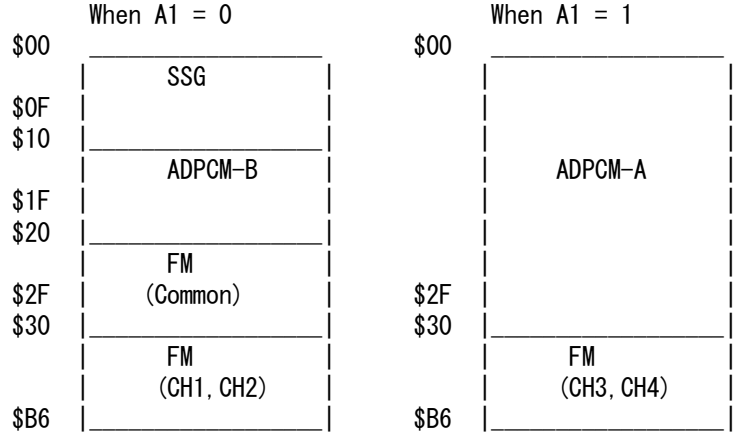
01	TOTAL LEVEL	"00"
02	TEST	"00"
08 0D	OUTPUT SELECT CHANNEL LEVEL	"00"
10 15	START ADR (L)	"00"
18 1D	START ADR (H)	"00"
20 25	END ADR (L)	"00"
28 2D	END ADR (H)	"00"

11	CONTROL 2	"00"
12	START ADR (L)	"XX"
13	START ADR (H)	"XX"
14	END ADR (L)	"XX"
15	END ADR (H)	"XX"
19	DELTA-N (L)	"XX"
1A	DELTA-N (H)	"XX"
1B	EG CONTROL	"XX"
1C	FLAG CONTROL	"00"

"XX" = undefined

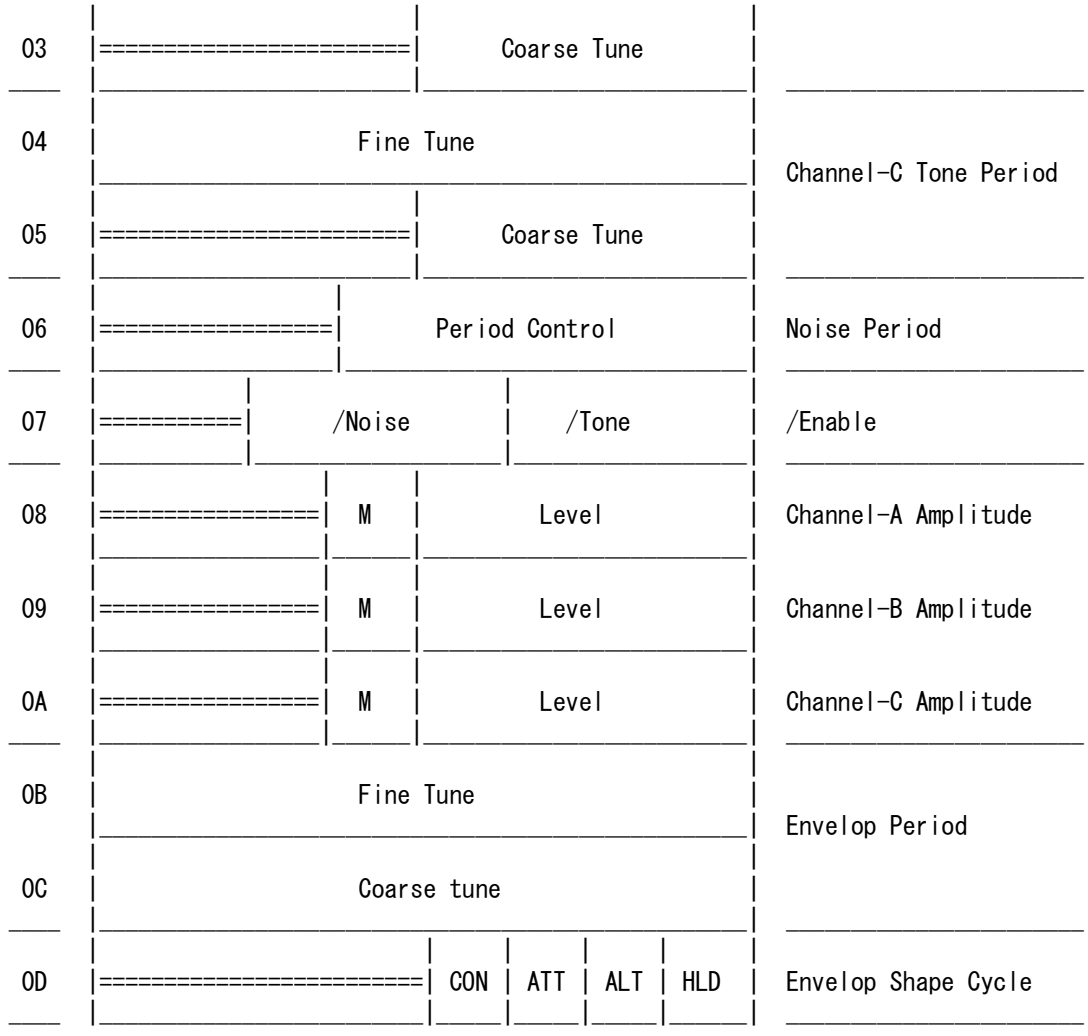
Functional Overview (2)

■ Register Address Allocation

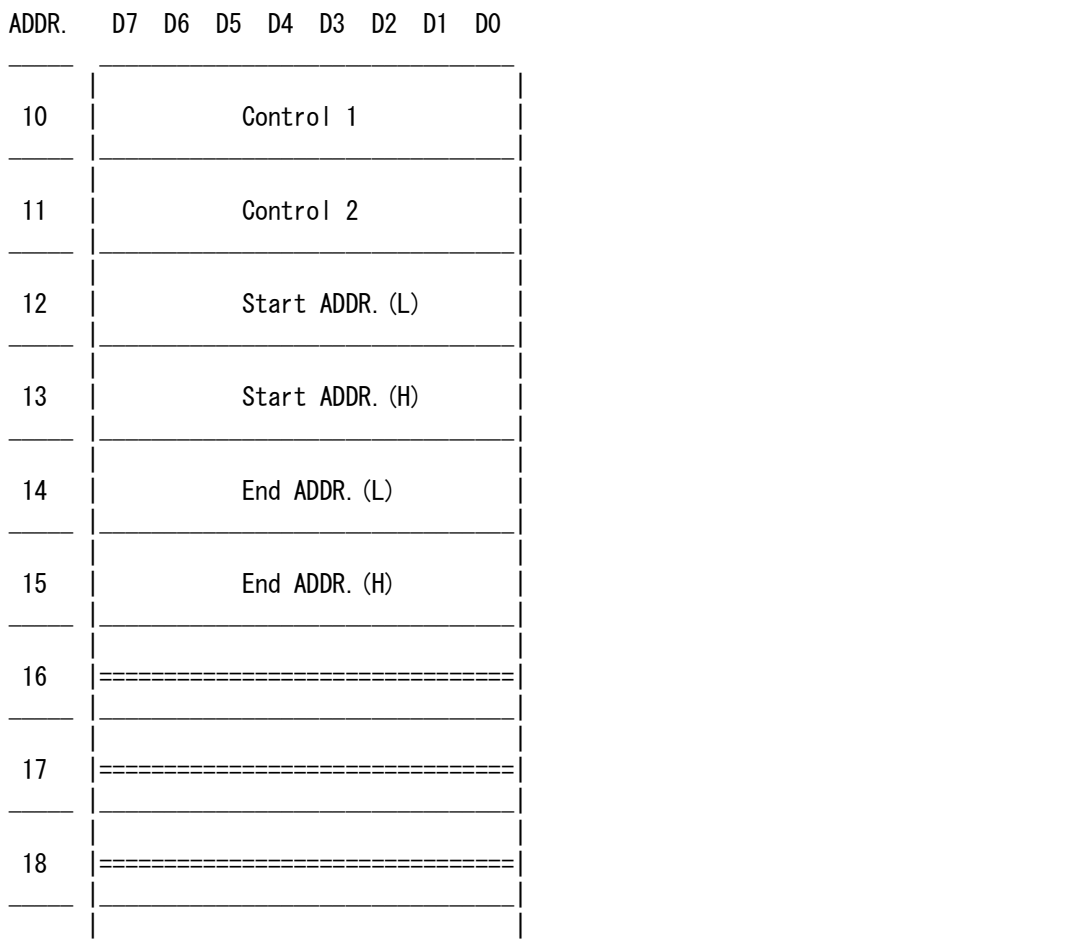


(a) Read/Write Data(SSG)

ADDR.	D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
00	Fine Tune								Channel-A Tone Period
01	Coarse Tune								
02	Fine Tune								Channel-B Tone Period



(B) Write Data (ADPCM-B)



19	Delta-N(L)	
1A	Delta-N(H)	
1B	EG Control	
1C	Flag Control	

(c) Write Data (FM)

ADDR.	D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
21	Test								LSI Test Data
22					LFO				LFO Freq Control
24	Timer-A								Timer-A upper 8 bits
25							Timer-A		Timer-A lower 2 bits
26	Timer-B								Timer-B Data
27	Mode		Reset		Enable		Load		Timer-A/B Control and 2 CH Mode
			B	A	B	A	B	A	
28	Slot					CH			Key-ON/OFF
29～2F									
31～3E		DT			MULTI				Detune/Multiple
41～4E					TL				Total Level
51～5E	KS				AR				Key Scale/Attack Rate
61～6E	AM				DR				AMON/Decay Rate
71～7E					SR				Sustain Rate
81～8E		SL				RR			Sustain Level/Release Rate
91～9E						SSG-EG			SSG-Type Envelop Control
A1,A2	F-Num 1								F-Numbers/Block

A5,A6	Block	F-Num 2		
A9,AA	2 CH * F-Num 1			2 CH - 2 Slot F-Numbers/Block
AD,AE	2CH*Block	2CH*F-Num2		
B1,B2	FB	Connect		Self Feedback/Connection
B5,B6	L / R	AMS	PMS	LR SEL./AM,PM SENS

※ Internal register address use

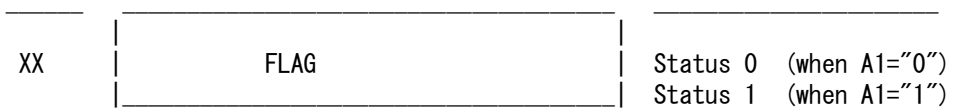
slot	1	2	3	4
ch1,ch3	*1	*5	*9	*D
ch2,ch4	*2	*6	*A	*E

(d) Write Data (ADPCM-A)

ADDR.	D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
00	DM		AON						Dump/ADPCM-A ON
01			ATL						ADPCM-A Total Level
02	Test								LSI Test Data
08 0D	L	R	AC L						Output Select Channel Level
10 15	Start ADDR.(L)								Start Address
18 1D	Start ADDR.(H)								
20 25	End ADDR.(L)								End Address
28 2D	End ADDR.(L)								

(e) Read Data

ADDR.	COMMENT



Functional Overview (3)

■ ADPCM-A Register Functions and Descriptions

DUMP/ADPCM-A ON ($00)

D7	D6	D5 D4 D3 D2 D1 D0
DM	--	AON

DM :"1"の時音をdump, produces a sound when "0".

AON : Specify ADPCM-A channel control bits.

ADPCM-A Total Level ($01)

D7	D6	D5 D4 D3 D2 D1 D0
--	--	ATL

ATL :ADPCM-A volume is set between 0 ～ -47.25dB in steps of 0.75dB.
all "1" equals 0 dB.

TEST ($02)

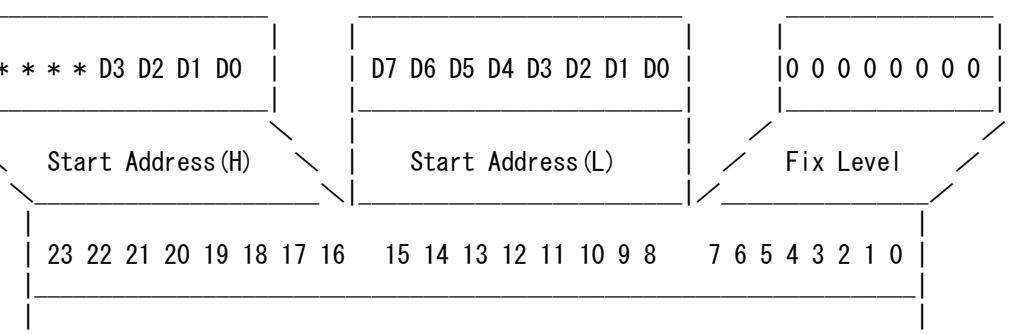
This address is provided to test the LSI.
Usually all "0".

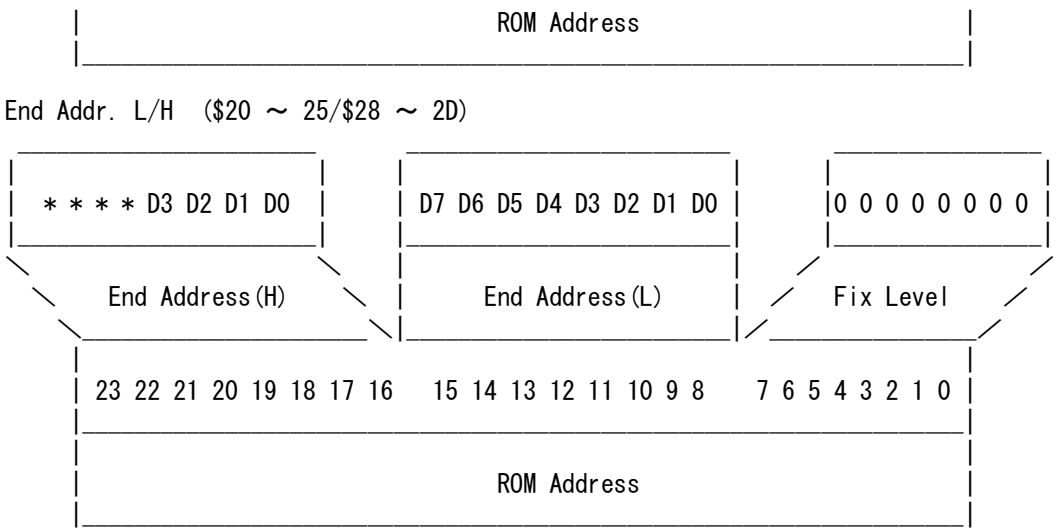
Output Select/Channel Level ($08-0D)

D7	D6	D5 D4 D3 D2 D1 D0
L	R	ACL

L : When "1", outputs to Left channel.
R : When "1", outputs to Right channel.
ACL :Each channel's level is 0 ～ -23.25dB in steps of 0.75dB.
all "1" = 0 dB

Start Addr. L/H ($10 ～ 15/$18 ～1D)





＊ $18 ～ 1D's D4 ～ D7 values and $28 ～ $2D's D4 ～ D7 values must be the same.

■ADPCM-A Synthesis Process

Address	Data	Comment
		Default
$1C	$3F	Mask Flags A0-A5 (flag reset)
$1C	$00	Enable flags
$01	$3F	Total Level setting (Maximum)
$08-$0D	$DF	Channel Level setting (Maximum)
$10-$15	$XX	Memory address start (L)
$18-$1D	$XX	Memory address start (H)
$20-$25	$XX	Memory address end (L)
$28-$2D	$XX	Memory address end (H)
Initalize Synthesis		
$00	$XX	AONビットが "1"になるのに同期して各チャンネルの合成開始(DM bit = "0")。 FLAG A0-A5が "1"となり、合成を指示するまで待機。 DMビットを "1"にして AONビットを "1"にすると、そのチャンネルは合成を中止する。 End of synthesis Synthesis ends when FLAG A0-A5 is "1".

■ADPCM-A Sound Source

Chan.	AON bit	Output Select	Start Address	End Address	End Synth.	Flag
1	D0	$08	$10/$18	$20/$28	FLAG	A0
2	D1	$09	$11/$19	$21/$29	FLAG	A1
3	D2	$0A	$12/$1A	$22/$2A	FLAG	A2
4	D3	$0B	$13/$1B	$23/$2B	FLAG	A3
5	D4	$0C	$14/$1C	$24/$2C	FLAG	A4
6	D5	$0D	$15/$1D	$25/$2D	FLAG	A5

Functional Overview (4)

■ADPCM-B Register Functions and Descriptions

Control 1 ($10)

D7 D6 D5 D4 D3 D2 D1 D0
START - - REPEAT - - - RESET

ADPCM-B Start, Control external memory access

RESET : 実行中に"1"とすると初期状態に戻る。但し、REPEATは"0"。
REPEAT : When "1", repeats ADPCM-B output from the same addresses.
START : When "1", ADPCM-B output begins.

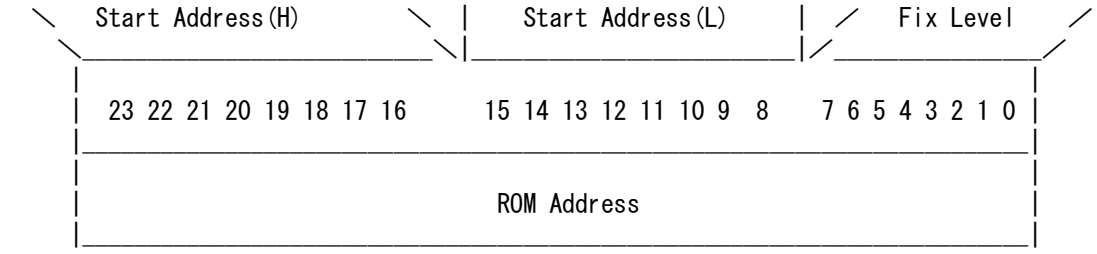
Control 2 ($11)

D7 D6 D5 D4 D3 D2 D1 D0
L R - - - - - -

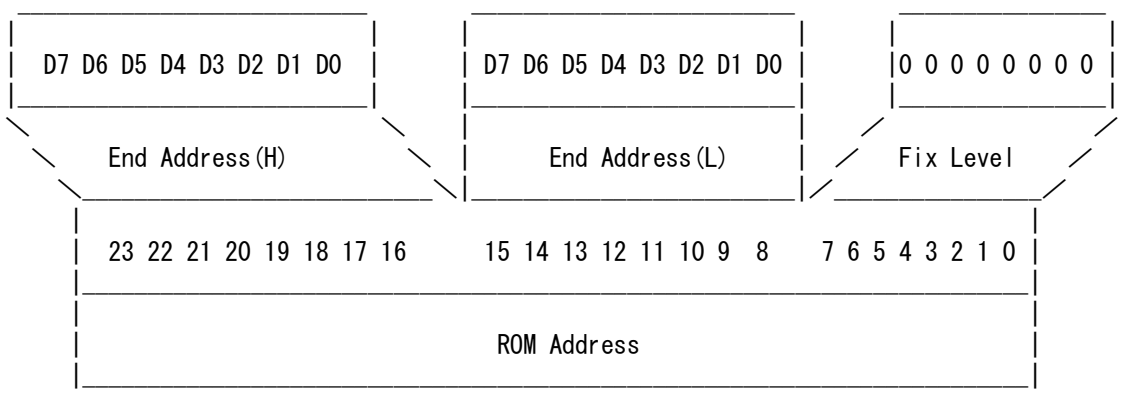
L : When "1", output to Left channel
R : When "1", output to Right channel

Start Address L/H ($12/$13)

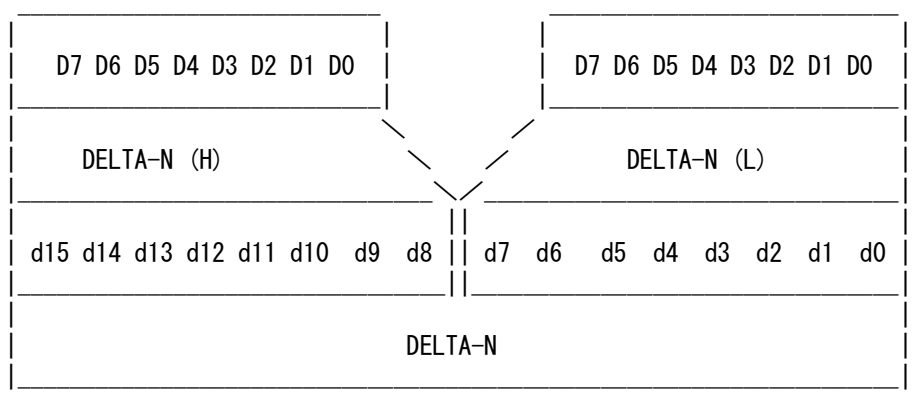
D7 D6 D5 D4 D3 D2 D1 D0		D7 D6 D5 D4 D3 D2 D1 D0		0 0 0 0 0 0 0 0



End Address L/H ($14/$15)



Delta-N L/H ($19/$1A)

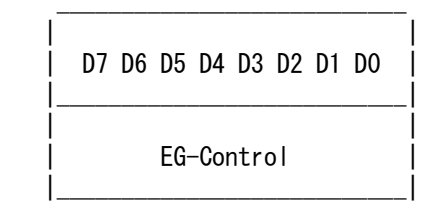


The sampling rate for ADPCM-B is specified like so:

$$f. = \frac{\triangle N}{256} * 55.5 \quad [KHz]$$

(Translator's note: The original document I translated had division by 216.)

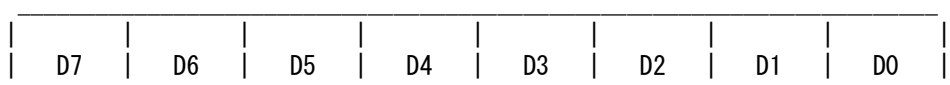
EG Control ($1B)



ADPCM-B Output Level Control

all "1" = max

Flag Control ($1C)



MSK B	_	MSK A5	MSK A4	MSK A3	MSK A2	MSK A1	MSK A0

ADPCM Flag Control

When MSK bit = "1", the corresponding flag in Status 1 is "0".

■ADPCM-B Synthesis Process

Addr.	Data	Comment
		Default
$1C	$80	Mask Flag B (Reset flags)
$1C	$00	Enable flags
$10	$00	Enable ADPCM-B output
$11	$C0	L and R channel output
$12	$XX	Memory start address (L)
$13	$XX	Memory start address (H)
$14	$XX	Memory end address (L)
$15	$XX	Memory end address (H)
$19	$BA	Sampling Rate 16 KHz (⊿N＝18874)
$1A	$49	
$1B	$FF	Set the output level (Maximum)
		Synthesis Initiation
$10	$80 (/$90)	Output begins when the START bit of register $10 is set to "1".
		Synthesis
		FLAG Bが "1"となり合成終了を指示するまで待機。
($10)	($80)	(Cancel repeat.)
($10)	($01)	(Force stop synthesis.)
		Synthesis End
$10	$00	Stop ADPCM-B output. Clear register $10

(Translator's note: The first entry in "Sampling Rate 16 KHz was "xx". 18874 = $49BA)

Functional Overview (5)

■ LFO Register Function and Description

LFO Frequency ($22)

D7	D6	D5	D4	D3	D2	D1	D0
				LFO ON	FREQ CONT		

FREQ CONT	0	1	2	3	4	5	6	7
freq (Hz)	3.98	5.56	6.02	6.37	6.88	9.63	48.1	72.2

FREQ CONT : Value is set based on the 8 values in the above table.
LFO ON : When "1", LFO is on.

PMS/AMS/LR ($B5 - $B6)

D7	D6	D5	D4	D3	D2	D1	D0
L	R	AMS			PMS		

PMS : Control phase modulation (based on table below).
AMS : Control amplitude modulation (based on table below).
L,R : Specify Left/Right channel output.

PMS	0	1	2	3	4	5	6	7
Diff.(Cents)	0	±3.4	±6.7	±10	±14	±20	±40	±80

AMS	0	1	2	3
Diff. (dB)	0	1.44	5.9	11.8

Decay Rate/AMON ($61 - $6E)

D7	D6	D5	D4	D3	D2	D1	D0
AMON			DR*				

*DR : Decay Rate
AMON : Control amplitude modulation for each slot. On when "1".

Functional Overview (6)

■ Status Read

Status 0 (Read) ($XX)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY						FLAG TB	FLAG TA

When D0,D1 are "1", $\overline{IRQ}$ is "0".

FLAG TA : Set to "1" when Timer A has finished/expired.
FLAG TB : Set to "1" when Timer B has finished/expired.
BUSY : データをレジスタにロード中 "1" になる。

Status 1 (Read) ($XX)

D7	D6	D5	D4	D3	D2	D1	D0
FLAG B		FLAG A5	FLAG A4	FLAG A3	FLAG A2	FLAG A1	FLAG A0

FLAG A0 ～ A5 : Set to "1" when each ADPCM-A channel reaches its end address.
FLAG B : Set to "1" when ADPCM-B has reached the end address.

● Additional Information from Others

・ADPCM-A部のADPCM音源は、YM2608に内蔵しているリズム音源部
に外付けROMのアドレス指定が、出来るようになったもののようで
音の出し方や、ボリュームのステップ等は、リズム音源と同等らしいです。

・ADPCM-B seems to be the same as the ADPCM in the YM2608.

・There is a second version of the YM2610, some call it the YM2610B.
The B version has 6 FM channels as opposed to 4.

[EOF]