



ARCHITECTURE SPECIFICATION

32-bit uDLX Core Processor

Universidade Federal da Bahia

Versão: 1.0

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Histórico de Revisões

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04/14/2014	Conception	João Carlos Bittencourt

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1. Introduction

1.1. Purpose

The main purpose of this document is to define specifications of a uDLX implementation and to provide a full overview of the design. This specifications defines all implementation parameters that composes the general uDLX requirements and specification. This definitions include processor operation modes, instruction set (ISA) and internal registers characteristics. This document also include detailed information of pipeline stages architecture, buses and other supplemental units.

1.2. Document Outline Description

This document is outlined as follow:

- Section :
- Section :

1.3. Acronyms and Abbreviations

Along this and other documents part of this project, it will be recurrent the usage of some acronyms and abbreviations. In order to keep track of this elements the Table 1 presents a set of abbreviations used and its corresponding meaning.

Table 1: Acronym and descriptions of elements in this document.

Acronym	Description
RISC	Reduced Instruction Set Computer
GPR	General Purpose Registers
FPGA	Field Gate Programmable Array
GPPU	General Purpose Processing Unit
SDRAM	Synchronous Dynamic Random Access Memory
HDL	Hardware Description Language
RAW	Read After Write
CPU	Central Processing Unit
ISA	Instruction Set Architecture
ALU	Arithmetic and Logic Unit
PC	Program Counter
RFlags	Flags Register
Const	Constant

2. Architecture Overview

2.1. Block Diagram

2.2. Pin/Port Definitions

Name	Length	Direction	Description

2.3. Parameters and Configurations

Name	Value	Description

3. Architecture Description

The data path developed to perform the synchronization is composed by:

3.1. Instructions Layout

3.2. Functional Data Path Description

3.2.1. Stage 1 - Instruction Fetch

3.2.2. Stage 2 - Instruction Decoding

3.2.3. Stage 3 - Execution

3.2.4. Stage 4 - Memory

3.2.5. Stage 5 - Write Back

3.3. Pipeline Register Description

3.4. Control Micro-instructions Description