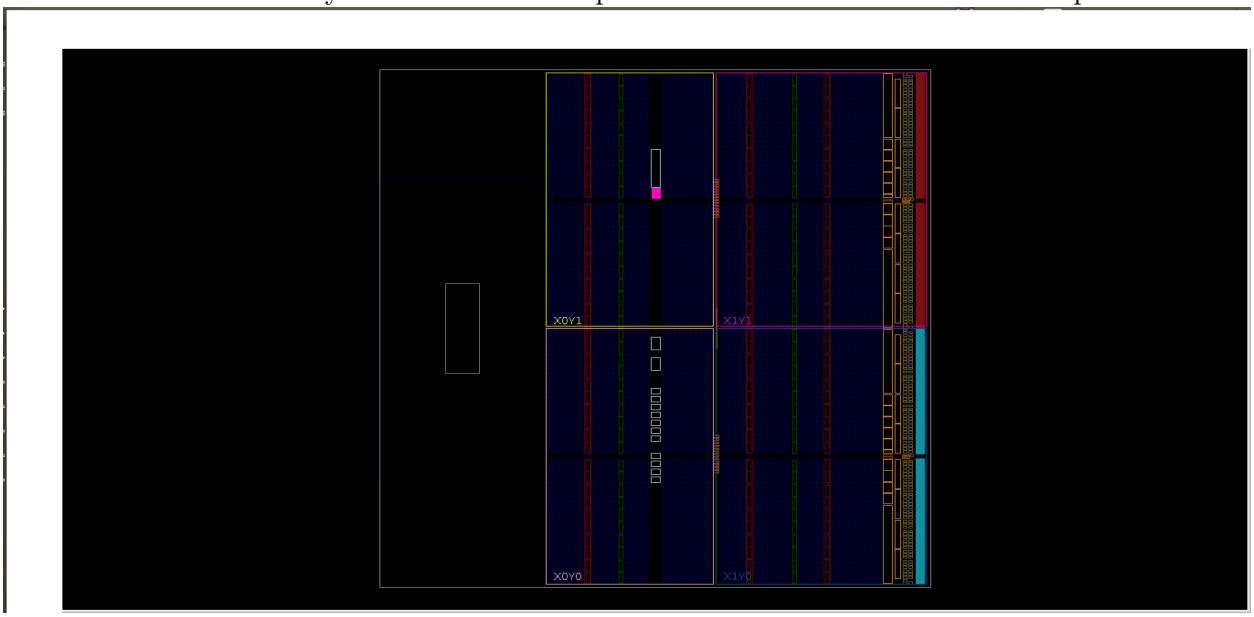
Notes for the FloorPlanning Paper

Let us consider a floorplanning example where we have to make a floorplan for two slots S_1 and S_2 on the FPGA fabric. Each slot has resource requirements denoted as $\{D_1, B_1, C_1\}$ and $\{D_2, B_2, C_2\}$ where D, B and C represent DSP, BRAM and CLB respectively.
Our proposed system takes as an input, the resource requirement of each slot and a description of the resource distribution of the FPGA fabric and it returns the placement coordinates of the slots. A slot is represented using 4 parameters i.e. the two bottom left coordinates and the width and the height of the slot. In our considered example the slots S_1 and S_2 are represented as (x_1, y_1, w_1, h_1) and (x_2, y_2, w_2, h_2).

Consider the resource layout in one of the quadrants of xc7z015 FPGA in the picture below



The number of BRAMs on the x axis of the FPGA fabric is expressed as

$$A(x) = \begin{cases} 0, & \mathbf{0}<\mathbf{x}<\mathbf{4}, \\ 1, & \mathbf{4}\leq\mathbf{x}<\mathbf{18}, \\ 2, & \mathbf{18}\leq\mathbf{x}<\mathbf{25}, \\ 3, & \mathbf{25}\leq\mathbf{x}<\mathbf{W}, \end{cases} \tag{1}$$

meanwhile the number of BRAMs on the y axis equals

$$B(y) = \begin{cases} y\%5, & \mathbf{0}\leq\mathbf{y}<\mathbf{H}, \end{cases} \tag{2}$$

The total number of BRAMs on the FPGA then equals to

$$BRAM(x,y) = A(x) * B(y) \tag{3}$$

The number of DSPs on the x axis of the FPGA fabric is expressed as

$$C(x) = \begin{cases} 0, & \mathbf{0<x<7}, \\ 1, & \mathbf{7\leq x<22}, \\ 2, & \mathbf{22\leq x<W}, \end{cases} \tag{4}$$

meanwhile the number of DSPs on the y axis equals

$$D(y) = \begin{cases} y\%5, & \mathbf{0\leq y<H}, \end{cases} \tag{5}$$

The total number of DSPs on the FPGA then equals to

$$DSP(x,y) = C(x) * D(y) \tag{6}$$

The number of CLB on the x axis is expressed

$$F(x) = \begin{cases} x, & \mathbf{0<x<4}, \\ (x-1), & \mathbf{4\leq x<7}, \\ (x-2), & \mathbf{7\leq x<10}, \\ (x-3), & \mathbf{10\leq x<15}, \\ (x-4), & \mathbf{15\leq x<18}, \\ (x-5), & \mathbf{18\leq x<22}, \\ (x-6), & \mathbf{22\leq x<25}, \\ (x-7), & \mathbf{25\leq x<W}, \end{cases} \tag{7}$$

The number of CLB on the y axis is expressed as

$$G(y) = \begin{cases} y, & \mathbf{0\leq y<H} \end{cases} \tag{8}$$

The total number of CLBs on the FPGA then equals to

$$CLB(x,y) = F(x) * G(y) \tag{9}$$

where

$$y \in \{0, H-1\} \quad and \quad x \in \{0, W-1\}$$

The total number of resources in a slot S(x, y, w, h) = (f(x+w, y+h) - f(x,y)) + (g(x+w, y+h) - g(x,y)) + (k(x+w, y+h) - k(x,y)) where f(x,y), g(x,y) and k(x,y) represent the number CLBs, DSP

and BRAM at (x,y) starting from the bottom left point i.e. (0,0) on the coordinate system of the fpga fabric.

(**to be included**: the position of the forbidden regions which are going to be used to formulate constraints)

The PR constraints used to generate the slot positions are

- there must be enough resources within the slots
- A frame can not be shared between two reconfigurable partitions (no interference)
- forbidden regions must not be included in the slots
- Left and right edges must be placed in proper positions
- the amount of wasted resources should be minimized (Wasting DSPs is more expensive than BRAMs which in turn is more expensive than CLBs)
- Other optimizations such as lower wire length between slots or lower length to I/O etc... can be added as constraints

constraint 1: This is fairly straight forward and needs no further elaboration
Constraint 2: A frame (tile) is the smallest reconfigurable physical region and it spans one clock region high and one resource wide. A Reconfigurable Frame cannot contain logic from more than one Reconfigurable Partition. This can be stated as two slots S_1 $\{x_1, y_1, w_1, h_1\}$ and $S_2\{ x_2, y_2, w_2, h_2 \}$ do not interfere if

$$x_1 + w_1 < x_2 \text{ or } y_1 + h_1 < y_2 : (x_1 < x_2 \text{ and } y_1 < y_2)$$

constraint 3: Global resources, clock resources (central clock column, BUFG, BUFR, MMCM etc...), static components (BSCAN, ICAP, XADC etc...) must not be included in the rectangles. The FPGA resource description must also include the location of these components to prohibit their inclusion in the rectangles

constraint 4: The left and right edges of the rectangles must be placed between CLB-CLB, CLB-BRAM or CLB-DSP and not between two interconnect columns (INT-INT).

constraint 5: This constraint has two parts. The first part states that the slots must be the smallest possible rectangles which contain the required amount of resources. The second part of the constraint states that the number of wasted resources should be kept to the minimum. Resources are considered wasted if they are included in a slot while not being used. All FPGA resources are not equally valuable. This means it is better to waste CLBs than BRAMs than DSPs. Hence there should be some kind of constraint to state the maximum amount of resources that can be wasted in search of an optimal slot. This constraint must also force the optimizer to start searching for slots from the columns of the most expensive resources.

constraint 6: Other constraints such as minimal wire length between slots (to reduce routing delay and power consumption) can be used as constraints to choose the optimal slots

Previous approaches of solving the floorplanning problem by other authors mostly involve two steps. First, all the possible slots are enumerated. This is done by starting a scan on the fpga fabric from the bottom left corner and lisitng all the possible rectangles which will contain all the necessary resources for the respective slots. Then some sort of heuristics/optimization is applied to choose the best ones from the set of possible slots.
Our approach instead focuses on using a mathemathical techniques to generate the slots first hand (without enumerating all possible slots) by using the proper constraints.

The system will finally return the parameters of S_1 $\{x_1, y_1, w_1, h_1\}$ and $S_2\{ x_2, y_2, w_2, h_2 \}$