ADAMAS UNIVERSITY PURSUE EXCELLENCE	**ADAMAS UNIVERSITY** **END (EVEN)SEMESTER EXAMINATION : MAY 2021** (Academic Session: 2020 – 21)		
Name of the Program: (B.Tech.)	B.Tech ECE	**Semester:** (I/III/ V/ VII/IX)	IV
Paper Title :	Digital Electronics	**Paper Code:**	EEC42102
Maximum Marks :	40	**Time duration:**	3 Hr
Total No of questions:	**8**	**Total No of Pages:**	2
(Any other information for the student may be mentioned here)			

Group A

Answer all the questions of the following **Marks (1 x 5=5)**

1. **a)** Design EX-OR Gate using NAND gate.
b) Reduce the following Boolean expression: $\bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + ABC$
c) Write and explain Truth table of 2:1 Multiplexer.
d) What is meant by race around condition in Flip-flop?
e) Write two difference between Combinational Circuit and Sequential Circuit.

GROUP –B

(**Short Answer Type Questions**)

Answer *any three* of the following $3 \times 5 = 15$

2. a) Simplify the following Boolean POS function using K-Map and realize the simplified expression using logic gates $f(A,B,C,D) = \pi M(6,7,8,9).D(12,13,14,15)$ [3]

b) Implement the Boolean function using 8:1 multiplexer

$f(A,B,C,D) = \sum m(1,2,4,5,9,11,12,13,14,15)$ [2]

3. a) Construct a D and JK Flip flop With Truth table and explain the operations. [3]

b) Design a 2:4 line Decoder. [2]

4. Obtain the set of prime implicants for the boolean expression

$f = \sum m(1,2,3,5,6,7,8,9,12,1315)$ using Quine-Mc-Cluskey method. [5]

5. Explain Serial in Parallel out shift register with suitable circuit diagram. [5]

GROUP –C

(**Long Answer Type Questions**)

Answer *any two* of the following $2 \times 10 = 20$

6. a) Design MOD-6 Asynchronous/Ripple up Counter using JK Flip-flop [4]

b) Design MOD-8 Synchronous Up Counter using T Flip-flop. [6]

7. a)) Design BCD Adder with suitable circuit diagram. [5]

b) How does a JK Flip flop differ from an SR flip flop in its operation? What is its advantage over an SR Flip flop?

c)Differentiate Truth table and Excitation Table? [3+2]

8. a) Design 8:1 multiplexer circuit using 4:1 multiplexer. [4]

b) Design CMOS inverter and CMOS NAND gate circuits. [3+3]