# ADAMAS UNIVERSITY
## END SEMESTER EXAMINATION
(Academic Session: 2020 – 21)

| Name of the Program: | BCA | Semester: | II |
|---|---|---|---|
| Paper Title: | DIGITAL ELECTRONICS | Paper Code: | ECE11501 |
| Maximum Marks: | 50 | Time Duration: | 3 Hrs |
| Total No. of Questions: | 17 | Total No of Pages: | 02 |
| *(Any other information for the student may be mentioned here)* | **1.** At top sheet, clearly mention Name, Univ. Roll No., Enrolment No., Paper Name & Code, Date of Exam. **2.** All parts of a Question should be answered consecutively. Each Answer should start from a fresh page. **3.** Assumptions made if any, should be stated clearly at the beginning of your answer. | | |

| Group A Answer All the Questions (5 x 1 = 5) | | | |
|---|---|---|---|
| **1** | **How** many two-inputs AND & OR gates are required to realize Y=CD+EF+G <br> **a)** 2,2      **b)** 2,3. <br> **c)** 3,3      **d)** none of these. | R | CO1 |
| **2** | **Solve** the Boolean expression $\overline{\overline{AB\overline{C}} + \overline{A}\overline{B}C}$ | AP | CO2 |
| **3** | In a 1:8 de-multiplexer, the number of select lines are <br> **a)** 4      **b)** 1 <br> **c)** 3      **d)** 2 | U | CO3 |
| **4** | **What** are the differences between ROM & RAM? | R | CO4 |
| **5** | The register that is loaded with parallel data with the stored data being available at the output serially one bit at a time is the type <br> **a)** SISO      **b)** SIPO <br> **c)** PISO      **d)** PIPO | R | CO5 |
| Group B Answer All the Questions (5 x 2 = 10) | | | |
| **6 a)** | **Design** and implement EX-OR gate using NOR gate. | C | CO2 |
| (OR) | | | |
| **6 b)** | On subtracting $(001100)_2$ from $(101001)_2$ using 2's complements, **construct** the value? | AP | CO1 |
| **7 a)** | **Simplify** and draw the logic diagram for the given expression $F = \overline{ABC} + \overline{A}BC + \overline{A}B\overline{C} + A\overline{BC} + A\overline{B}C$ | AN | CO2 |
| (OR) | | | |
| **7 b)** | **Construct** 16:1 MUX by using 4:1 MUX only. | AP | CO3 |
| **8 a)** | **Simplify** the expression $Y = \prod (0, 1, 4, 5, 6, 8, 9, 12, 13, 14)$ using the K-map method | AN | CO3 |
| (OR) | | | |
| **8 b)** | **Compare** between PROM, PLA & PAL. | E | CO4 |
| **9 a)** | **Determine** the initial clock frequency of 4-bit ripple counter, if the period of waveform at the last flip-flop is 64 microseconds. | E | CO5 |
| (OR) | | | |
| **9 b)** | **Explain** propagation delay in ripple counter. | U | CO5 |

| 10 a) | **Determine** the binary numbers represented by the following decimal numbers.<br>(i) 25.5 (ii) 10.625 | E | CO1 |
|---|---|---|---|
| | **(OR)** | | |
| 10 b) | **Define** Associative property of Boolean algebra. | R | CO2 |

**Group C**
**Answer All the Questions (7 x 5 = 35)**

| 11 a) | i) **Compare** between Weighted Binary Codes and Non-Weighted Binary Codes         **[2]**<br>ii) **Construct** the decimal number 82.67 to its binary, hexadecimal and octal equivalents.     **[3]** | AN, AP | CO1 |
|---|---|---|---|
| | **(OR)** | | |
| 11 b) | Draw the logic diagram of a full subtractor and **explain** its working with the help of a truth table. | U | CO2 |
| 12 a) | **Simplify** the expression using Karnaugh map $Y = \sum_m$ (0, 1, 4, 5, 8, 9, 12, 13, 14), d (2,3,6) and draw the equivalent circuit using logic gates. | AN | CO3 |
| | **(OR)** | | |
| 12 b) | Design and implement the circuit using 4-bit EXCESS-3 to BCD converter and simplify the expression using Karnaugh map. | C | CO2 |
| 13 a) | **What** is an Encoder? Draw the logic circuit of a 8-line to 3-line Encoder and explain its working. | R | CO3 |
| | **(OR)** | | |
| 13 b) | **Explain** the operation of master slave J-K flip flop and show how the race around condition is eliminated in it. | U | CO3 |
| 14 a) | **Design** 4x1 MUX using Boolean function $F(A,B,C,D) = \sum_m$ (1,4,5,7,9,12,13). | C | CO3 |
| | **(OR)** | | |
| 14 b) | Write the different conditions to check for **determining** the type of Decoder, number of AND gates and OR gates for realization of Boolean expression using PLDs. Realize the following set of logical expressions using ROM, PLA and PAL.<br>    $Y_1 = AC + \overline{A}B$<br>    $Y_2 = ABC + AB\overline{C} + \overline{A}BC$<br>    $Y_3 = A\overline{B}C + AB\overline{C} + A\overline{B}\overline{C}$ | E | CO4 |
| 15 a) | **Design** a 4-bit asynchronous up counter using negative edge triggered and show the timing diagram. | C | CO5 |
| | **(OR)** | | |
| 15 b) | **Design** PISO shift register and explain the data movement technique. | C, U | CO5 |
| 16 a) | i) Write down the differences between synchronous and asynchronous counters.<br>ii) **Design** Mod-6 Synchronous up counter using T flip flop**.** | R, C | CO5 |
| | **(OR)** | | |
| 16 b) | **Compare** between static and dynamic RAM. Draw the circuits of one cell of each and explain its working. | E | CO4 |
| 17 a) | **Construct** the D FF from JK FF using its corresponding characteristics & excitation table. | AP | CO3 |
| | **(OR)** | | |
| 17 b) | **Change** the S-R FF to D FF using its corresponding characteristics & excitation table. | C | CO3 |