	ADAMAS UNIVERSITY **END SEMESTER EXAMINATION** (Academic Session: 2020 – 21)		
Name of the Program:	BCA	**Semester:**	II
Paper Title:	Design of Logic Circuit	**Paper Code:**	CSE11405
Maximum Marks:	50	**Time Duration:**	3 Hrs
Total No. of Questions:	17	**Total No of Pages:**	2
(Any other information for the student may be mentioned here)	**1.** At top sheet, clearly mention Name, Univ. Roll No., Enrolment No., Paper Name & Code, Date of Exam. **2.** All parts of a Question should be answered consecutively. Each Answer should start from a fresh page. **3.** Assumptions made if any, should be stated clearly at the beginning of your answer.		

Group A **Answer All the Questions (5 x 1 = 5)**			
1	Convert $(110110100011)_2$ to $(\ )_{16}$.	**Ap**	**CO1**
2	What is the full form of CMOS?	**R**	**CO2**
3	Moore model uses only Entry Actions. True or False?	**U**	**CO3**
4	What is the full form of EEPROM?	**R**	**CO4**
5	ROMs are much faster than dedicated logic circuits. True or False?	**U**	**CO4**
Group B **Answer All the Questions (5 x 2 = 10)**			
6 a)	Using the Karnaugh map, obtain the Boolean expression for $F(A, B, C, D) = \sum_m(0,4,7,,9,13,15) + \sum_d(3,5)$	**Ap**	**CO1**
	(OR)		
6 b)	Draw the logic diagram and derive the Boolean expression of a half-subtractor.	**U**	**CO1**
7 a)	Define Fan-in and Fan-out.	**R**	**CO2**
	(OR)		
7 b)	What is the utility of CMOS?	**R**	**CO2**
8 a)	Define Mealy Machines.	**R**	**CO3**
	(OR)		
8 b)	Describe the universal logic gates.	**R**	**CO3**
9 a)	Describe the different laws of Boolean algebra.	**R**	**CO1**
	(OR)		
9 b)	Draw the logic circuit and truth table of a 2×4 decoder.	**Ap**	**CO1**
10 a)	Give the logic diagram and state transition table of a T F/F.	**U**	**CO4**
	(OR)		
10 b)	Give the logic diagram and state transition table of an S-R F/F.	**U**	**CO4**
Group C **Answer All the Questions (7 x 5 = 35)**			
11 a)	Using the Karnaugh map, minimise the following Boolean expression: $F(A, B, C, D) = \sum_m(1,2,3,8,9,10,11,14) + \sum_d(7, 15)$ and draw the logic circuit for the minimized expression	**Ap**	**CO1**
	(OR)		
11 b)	Draw the logic circuit diagram of a 2:1 MUX and by using it, design a 4:1 MUX.	**Ap**	**CO1**

12 a)	Briefly describe the family of logic gates	**R**	**CO2**
(OR)			
12 b)	Write short note on CMOS.	**R**	**CO2**
13 a)	Explain the functionality of Moore machine.	**U**	**CO3**
(OR)			
13 b)	Differentiate between Moore & Mealy machine.	**R**	**CO3**
14 a)	Write short note on ROM	**U**	**CO4**
(OR)			
14 b)	Explain how ROM is used as a PLD.	**Ap**	**CO4**
15 a)	Explain Full Adder with logic circuit diagram, truth table and Boolean expression	**U**	**CO1**
(OR)			
15 b)	Explain XOR and XNOR with logic diagrams and truth tables.	**U**	**CO1**
16 a)	Realize $f(A,B,C) = (a + bc)(b + c'a)$ using only NOR gates.	**Ap**	**CO1**
(OR)			
16 b)	Differentiate between K-map and Quine-McCluskey method	**R**	**CO1**
17 a)	Describe the different shift registers.	**U**	**CO4**
(OR)			
17 b)	Differentiate between S-R latch and S-R Flip-Flop	**U**	**CO4**

Note: The Sample prepared by assuming 5 COs in a course, considering one CO for one Module.

i) If the COs are higher in numbers that can be managed by equating sub-divisional questions

ii) If the COs are lower in numbers, the questions can be increased by equating the number of COs