ADAMAS UNIVERSITY PURSUE EXCELLENCE	**ADAMAS UNIVERSITY** **END-SEMESTER EXAMINATION : MAY 2021** (Academic Session: 2020 – 21)		
Name of the Program:	B.Tech	**Semester:**	IV
Paper Title :	Computer Architecture & Operating System	**Paper Code:**	ECS43120
Maximum Marks :	40	**Time duration:**	3 Hrs
Total No of questions:	8	**Total No of Pages:**	2
(Any other information for the student may be mentioned here)			

Answer all the Groups

Group A

Answer all the questions of the following $5 \times 1 = 5$

1. a) What are the advantages of booths Multiplication Algorithm?
   b) What do you understand by Instruction level parallelism?
   c)State the role of Cache memory.
   d)What is role of virtual memory in program execution?
   e)What do you understand by paging?

GROUP –B

Answer *any three* of the following $3 \times 5 = 15$

2. What do you understand by byte addressability. Discuss the basic functional units of a computer.

3. Let us assume that a complete execution of a program requires the execution of 100 machine language instruction. Some instructions may be executed more than once when they are inside loop, So we can assume that the average no of basic steps needed to execute one basic instruction is 7, such that each and every basic step completes in 1 clock cycle. If a 10 Hz – processor is used then calculate time required by the processor to execute the program. What is Processor clock?

4. Explain the working principle of a DMA Controller with example.

5. What do you understand by a fully associative cache explain with diagram. Calculate the hit ratio and miss ratio for LRU and FIFO replacement policy implemented on a fully associative cache with 8 cache blocks (0-7). The memory block requests are in the order-

   4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

   If LRU replacement policy is used, which cache block will have memory block 7?

GROUP –C

Answer *any two* of the following $2 \times 10 = 20$

6. Generate the3-Address 2-Address, 1-Address and Zero address Instruction sequence for the following expression $X = \frac{(a+b)}{4} + \frac{(c+5)\times d}{2}$

7. Write an Algorithm for division along with the flowchart. Represent each step for dividing 4 by 2.

8. What is Instruction Pipeline. What are the reasons for data hazard? Give a solution for data hazard.

   A Pipelined processor has 4 stages, Fetch, Decode, Execute, Write Back. Fetch, Decode and Write Back stage takes 1 clock cycle for each and every instructions and for Execution stage it depends on the Instruction. Addition and Subtraction instruction takes 1 clock cycle and Multiplication Instruction takes 3 clock cycles. The Instructions are

   $I_1: ADD R_2 R_1 R_0$

   I_2 : MUL $R_4 R_3 R_2$

   I_3 : SUB $R_5 R_4 R_2$

   Calculate the total number of clock cycles required to complete the execution of above Instruction sequence in- *Case1:* Without data forwarding and *Case2:* With data forwarding.
