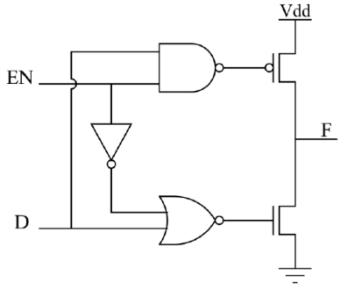
ADAMAS UNIVERSITY PURSUE EXCELLENCE	**ADAMAS UNIVERSITY** **END-SEMESTER EXAMINATION: MAY 2021** (Academic Session: 2020 – 21)		
Name of the Program:	B.Tech.	**Semester:**	VI
Paper Title:	VLSI System Design	**Paper Code:**	EEC43102
Maximum Marks:	40	**Time duration:**	3 Hours
Total No of questions:	08	**Total No of Pages:**	02
	Note: 1. Follow all the Instructions given on the cover page of the Answer Booklet Strictly. 2. All parts of a Question should be answered consecutively. 3. Each answer should start from a fresh page. 4. Assumptions made if any, should be stated clearly at the beginning of your answer.		

Answer all the Groups

Group A

Answer all the questions of the following $5 \times 1 = 5$

1. a) What is the difference between PLA and PAL?
b) State Moore's First law.
c) How does n-MOS oxide layer fabricate?
d) What are advantages of dynamic CMOS?
e) In the circuit shown, what are the values of F for EN= 0 and EN= 1 respectively



GROUP –B

Answer *any three* of the following $3 \times 5 = 15$

2. Design and explain the operation of the following using Transmission gates:
a) XOR gate
b) 4:1 MUX [3+2]

3. a) Design AND and XNOR gates using Pass transistor Logic.
b) Describe the Logic '0' and logic '1' transfer mechanism of a Pass transistor Logic. [3+2]

4. Draw and explain the operation of the NAND based SR flip flop circuit using CMOS AOI.

5. Draw the Stick Diagram and Schematic diagram of a static CMOS XOR gate and identify the corresponding components in the two drawing. [2+3]

GROUP –C

Answer *any two* of the following $2 \times 10 = 20$

6. a) Compare between static logic and dynamic logic.
b) Explain the operation of Domino logic to design CMOS circuits. What are the limitations of it?
c) Write down the operation of NORA logic. [2+4+1+3]

7. Explain the Voltage Transfer Characteristics (VTC) of CMOS inverter and calculate V_{OL} and V_{OH} [4+6]

8. a) Describe how MOS device use as non-volatile memory.
b) Write down the working principle of 6 transistors SRAM cell.
c) What are the main problems of pseudo n-MOS logic? [3+5+2]
