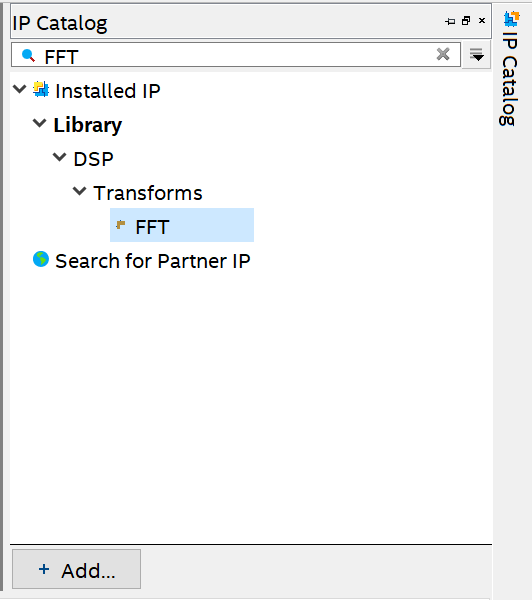
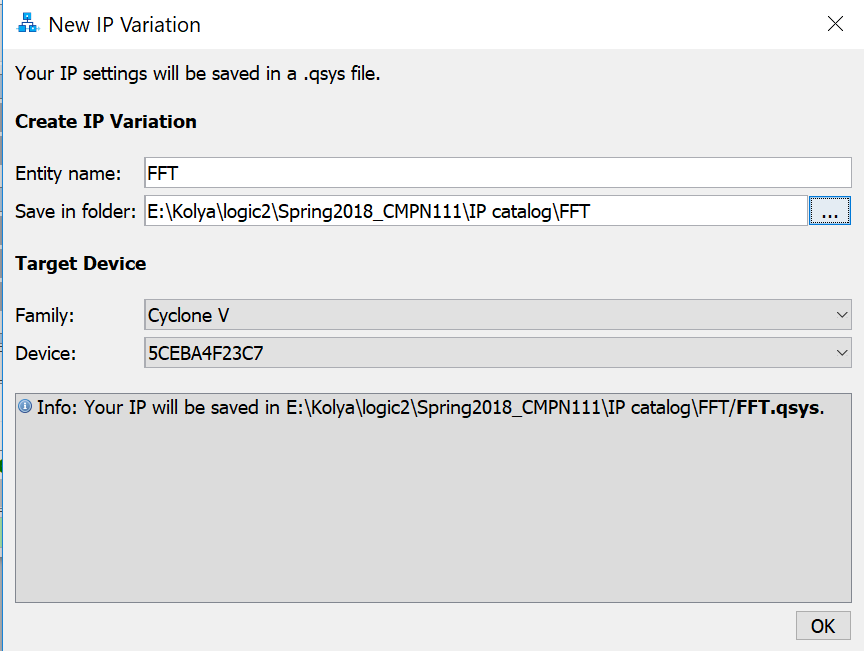
**FFT Generation**

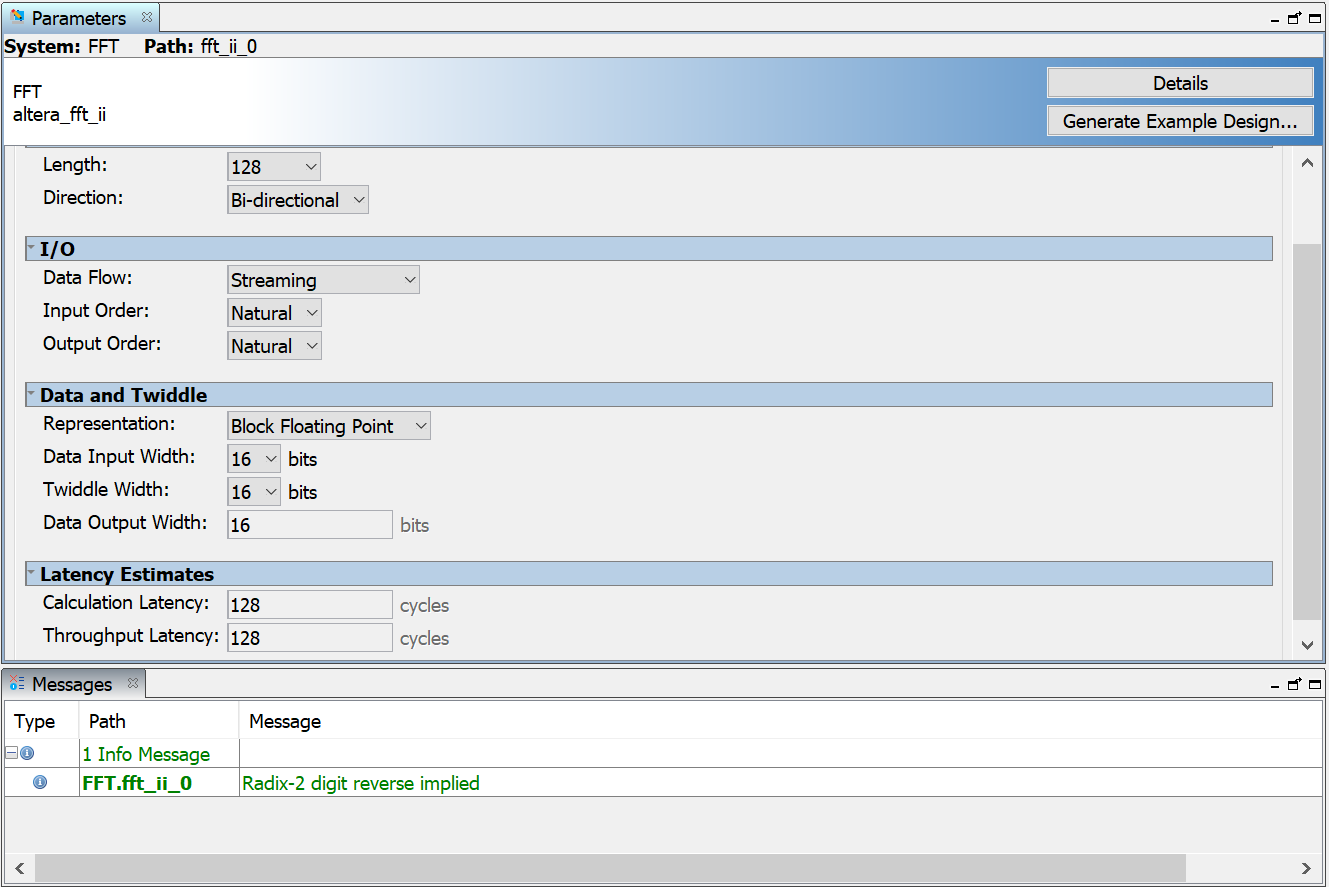
1. Tools🡪IP Catalog
2. Write FFT in search box and press Enter
3. Double click on FFT to open IP Parameter Editor



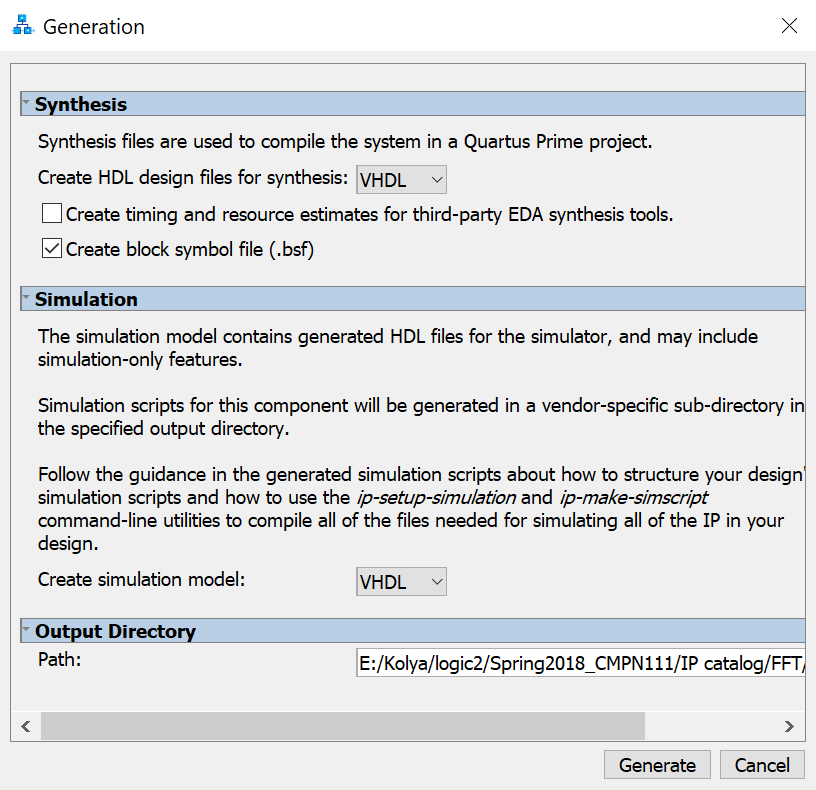
1. Enter the name of your entity as FFT and enter the path



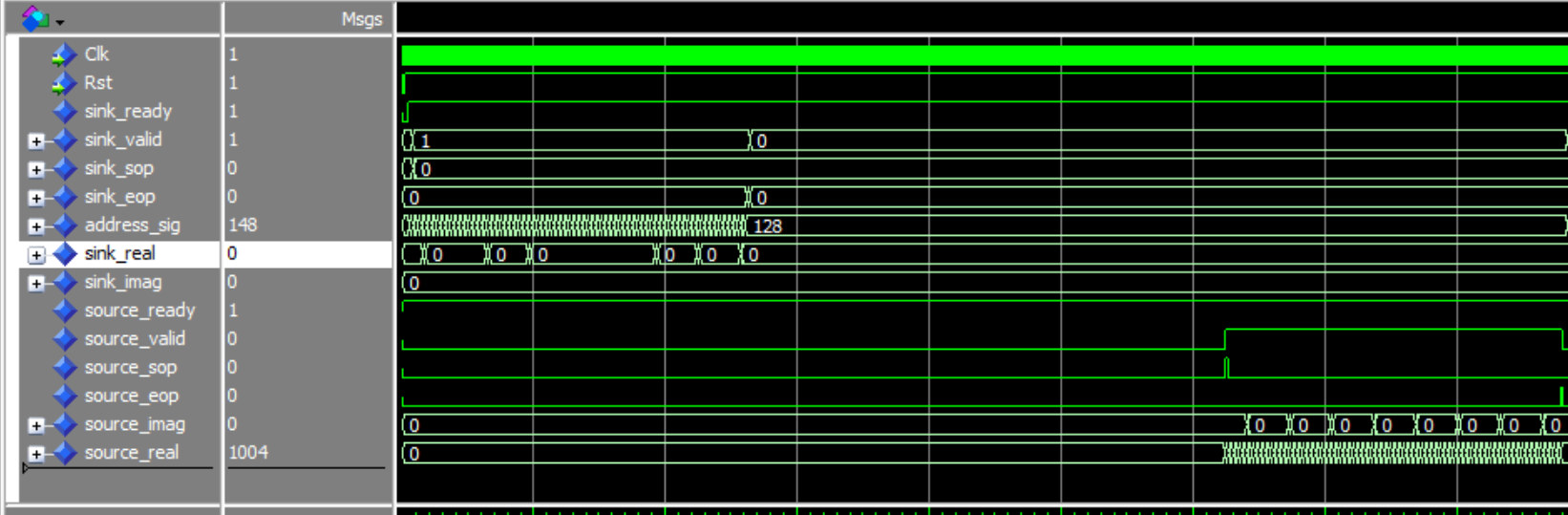
1. Enter the parameter as the following figure to configure the fft to work as 128 point and 16 bit data. (this parameter definition can be found at table 8 in ug\_fft.pdf page 37)



1. Click Generate HDL and enter the option as in the following figure Then click Generate



1. Add FFT.sip and FFT.qip to your project to add FFT IP to it.
2. The inputs and outputs port definition is found at table 10 in ug\_fft.pdf page 39)
3. You must write your testbench to simulate the FFT, Your testbench must generate the waveforms of FFT Streaming Data Flow which shown in figures 11, 12, 13 in ug\_fft.pdf page 30
4. To simulate the FFT you must simulate it from Quartus prime as following:
   1. Select Tools🡪Options🡪EDA Tool Options
   2. Enter in ModelSim-Altera the following path C:\intelFPGA\_lite\17.0\modelsim\_ase\win32aloem then press OK
   3. Select Assignments🡪Settings🡪Simulation
   4. Select Tool name: ModelSim-Altera
   5. Choose Compile test bench
   6. Press Test Benches button and add your test bench file (if you TB file is FFT128\_TB)
   7. Click New then enter FFT128\_TB in Test bench name and add your file by click the browsing button and click the add button
5. You TB file must wait first for sink\_ready to be “1” then assert sink\_valid
6. Put sink\_error = ‘00’
7. The inverse input determin the direction of transform. it make FFT if it equal to 0 otherwise it make IFFT
8. After that you will load the 128 real and imaginary input points.
9. The start of input transfer is noted by sink\_sop and the end of transfer is validated by sink\_eop
10. You must assert source\_ready to wait for output
11. The FFT will calculate the FFT and when it finished it will assert source\_valid
12. The 128 output (source\_real and source\_img) will generated between source\_sop and source\_eop



1. To run your TB chose RTL Simulation from Tasks panel then click RTL Simulation.