**Interactive Tool for the Simulation of**

**MOS Electrostatics**

Report for **Summer Research Internship of Gandhinagar (SRIP 2019)**

By

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Declaration

I, **Biswajeet Sahoo**, hereby declare that the presented report of summer internship entitled **“Interactive Tool for the Simulation of MOS Electrostatics”** is the result of work carried out by me at the nanoDC Laboratory, Department of Electrical Engineering, Indian Institute of Technology Gandhinagar, under the able supervision of **Dr. Nihar Ranjan Mohapatra**.

I also confirm that the information submitted in the report is true and original to the best of my knowledge.

IIT Gandhinagar **Biswajeet Sahoo**

May-June, 2019 SRIP Id- 201945640

**Acknowledgements**

The internship opportunity I had in the nanoDC Laboratory, Indian Institute of Technology Gandhinagar was a great experience for learning and research-professional development. I feel myself privileged for getting to meet and interact with many wonderful people and professionals who led me throughout this internship period.

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I choose this special space to gratefully acknowledge the immense cooperation and contribution of Mr. Mohit D Ganeriwala, PhD scholar at IITGN, who has made this journey a truly learning and joyful experience. His efforts in guiding me in every aspect to provide me a congenial working atmosphere are highly appreciated. Not only he guided me for the successful completion of the internship work but also shaped my vision as a budding research aspirant.

I would also like to thank all my friends and the students in the lab for bestowing their unforgettable love, warmth and support during my stay on the campus of IIT Gandhinagar.

IIT Gandhinagar Biswajeet Sahoo

May-June, 2019 SRIP Id- 201945640

**Abstract**

Nowadays, the development of VLSI technology is mainly directed towards the miniaturization of semiconductor devices which in turn heavily depend on the advancement in the MOSFET technology. The minimum dimension of a single device for present day technology is below 100nm in channel length. So with the advancement of the nanotechnology, it’s very important to study deeply the electrostatic properties of the MOSFET. In this project, an interactive tool is made for the simulation of *MOSFET Electrostatics*. The tool has been made for the simulation of MOS Cap (2 terminal), 3 terminal MOS and the complete whole 4 terminal MOS. The tool has options for both n type MOSFET as well as for the p type MOSFET. This tool is designed in which a way that it will be more user-friendly and easy to understand. It gives a proper visual representation of how a MOSFET would work under different scenarios as per the inputs given by the user and finally plotting the resulting graphs. It’s very useful for the research in Nanoelectronics and Semiconductor Device.

# Introduction

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a semiconductor device which is widely used for switching and amplifying electronics signals in most of the electronic devices. It is the heart of the integrated circuit and it can be designed and fabricated in a single chip because of the very small size of it. It is very far the most common transistor and can be used in both analog and digital circuits. It is a unipolar device i.e. conduction of current is either carried out by the movement of electrons or holes. It is much more faster than BJT since the majority carriers are the source of the current. So, comparatively BJT consumes more power. Thus with the increasing need of the MOS in this era, it’s necessary to study the operation of MOSFET by changing it’s structure, material, applied voltages, etc.

In this scenario, a simulation tool will play a pivotal role for the design engineers and researchers to analyse, characterize, and develop new devices. It saves time and lowers the cost of design when compared to the experimental approach. So a dynamic interactive tool is important for simulating devices.

It terms of construction and doping the MOSFET can be classified into 2 types:-

1. N-Channel MOSFET
2. P-Channel MOSFET

MOSFET is mainly available in 2 basic forms:-

1. Depletion Type - This is equivalent to a “Normally closed” switch. The device is normally ON at zero gate-source voltage. It can be used as load resistors in logic circuits
2. Enhancement Type – This is equivalent to a “Normally Open” switch. The transistor requires a Gate Source voltage (VGS) to switch the device “ON”. They will only conduct in the addition of positive voltage at the gate terminal. The device is normally OFF at zero gate-source voltage.

MOSFET mainly have 3 terminals: Gate, Source and Drain. The line between the drain and source connections represents the semi conductive channel. The channel width W and length L of individual transistor vary greatly, depending on circuit design needs. The centre part of the structure is covered by an insulator (typically Silicon dioxide, which is often referred to simply as oxide). The body interface to the oxide is often called the surface.

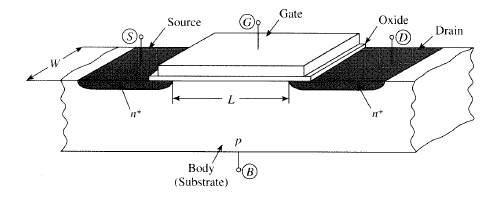


Figure 1: Simplified Structure of the n-channel MOS transistor

On basis of number of terminals MOS structure is classified into 3 types:-

1. 2 Terminal MOS/MOS Capacitor
2. 3 Terminal MOS
3. 4 Terminal MOS

The landing page of my software tool looks like the below picture. It has several buttons of matplotlib library of python. The user has to choose one of those which will open another window for plotting graphs. The whole software/tool doesn’t require python or any of its dependencies to be pre-installed in the user’s system. Every python file in converted to executable bundle file using the PyInstaller package and the executable files are called from this landing page. The whole folder is then converted to a single .exe file in case of Windows and a .zip file in case of Ubuntu. This single file can be given to any user for their use.

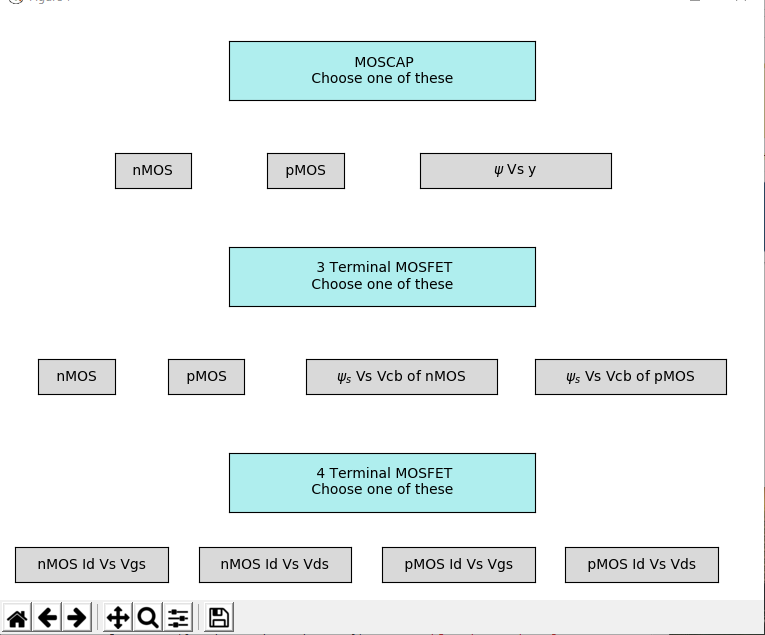


Figure 2: Main page of the tool

# 2 Terminal MOSFET Structure/MOS Capacitor

## 

## Introduction

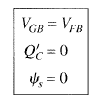
2 Terminal MOS is made gate, insulator and the body. This structure is also referred to as a MOS Capacitor. The acronym MOS, standing for metal-oxide semiconductor is used independently of whether the gate is actually made of metal or whether the insulator is Silicon dioxide. In early days gates were invariably considered as made of metal, the insulator made of Silicon dioxide and the semiconductor unambiguously referred as body. Extensive study of MOS Cap over the years have resulted in a detailed understanding of the structure and led to the development of better fabrication methods that greatly reduced the undesirable effects and that made the MOS transistors with high performance. In this we will consider the various potentials ,charges developed and the capacitance properties. A voltage at which there is no electrical charge in the semiconductor and hence no voltage drop, is called as Flatband voltage (VFB). The energy bands in the band diagram are horizontal (flat) in this case. Also we can define the surface potential ѱs as the total potential drop across the region, defined from the surface to a point in the bulk outside that region.

## Effect of Gate-Body Voltage on Surface Condition

Now let us consider the effect of Gate-Body Voltage (VGB) on the surface considering a p-type body.

1. Flatband Condition:

It is the case in which the Surface potential is zero, VGB = VFB and the charge in the semiconductor under the oxide QC =0.



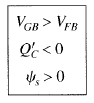
1. Accumulation:

It is the case where VGB decreases below VFB. The negative change of VGB will cause a negative change in the gate charge (QG) Thus the semiconductor charges will balance this change by providing a net positive charge. The negative change in VGB causes the negative change in Surface potential ѱs.



1. Depletion and Inversion:

In this case the VGB increases above VFB. The total charge on the gate QG will become more positive than the value at flatband(interface charge – QO). Thus QC balances the positive charge by providing the negative charges. Also the positive change in VGB will cause positive changes in ѱs.

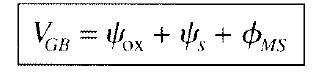


## Potential Balance and Charge Balance

Four kinds of potential drops are encountered in the loop:-

1. The voltage of the external source VGB.
2. The potential drop across the oxide ѱox
3. The surface potential ѱs
4. Sum of the contact potentials when going clockwise ΦMS.

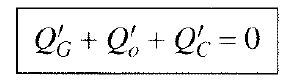
Thus, we can write ,



Now considering the charges in the system, they are of different types:-

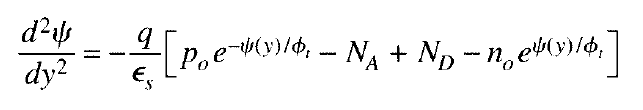
1. The charge on the gate QG
2. The effective interface charge QO
3. The charge in the semiconductor under the oxide QC

These charges must balance one another for overall charge neutral system:-

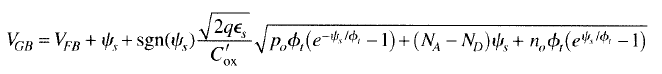


## General Analysis

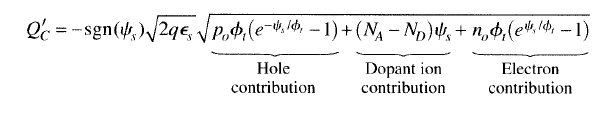
From the Poisson’s equation we get,



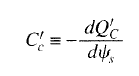
Double Integrating the equation, we can get the value of VGB :-

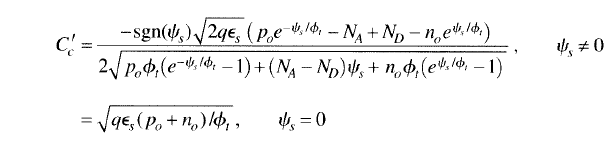


Similarly,We can also find the equation of the total semiconductor charge Q’c :-



If the potential across the semiconductor changes by ∆ѱs, the charge in that region will change by ∆Q’c. This additional charge must enter the region through it’s bottom, coming from the body terminal. Thus we can define the semiconductor capacitance C’c as





Using my python code i.e. I have used the matplotlib to plot the graphs of these equations and have got the following results :-

There are 4 graphs in each window for both nMOS and pMOS :-

1. Ѱs Vs VGB
2. Q’c Vs ѱs
3. Q’c Vs VGB
4. C’c Vs VGB

We can vary the shown parameters by moving the slider. Proper legends and labelling are also there for better information. The value of the slider in shown beside the slider bar. Also there is option for saving the graphs in matplotlib.

## n-type body MOS

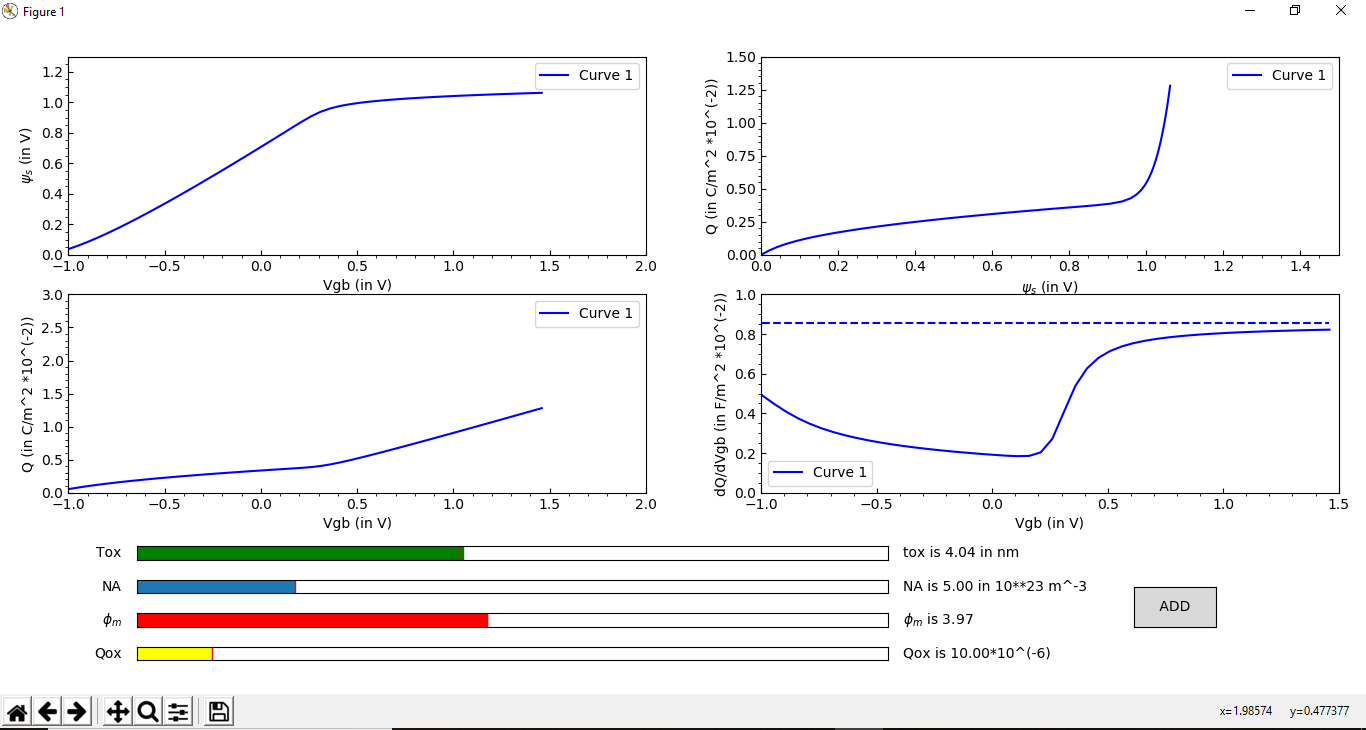


Figure 3: This shows the results of the n type body MOS Capacitor

## n-type body MOS

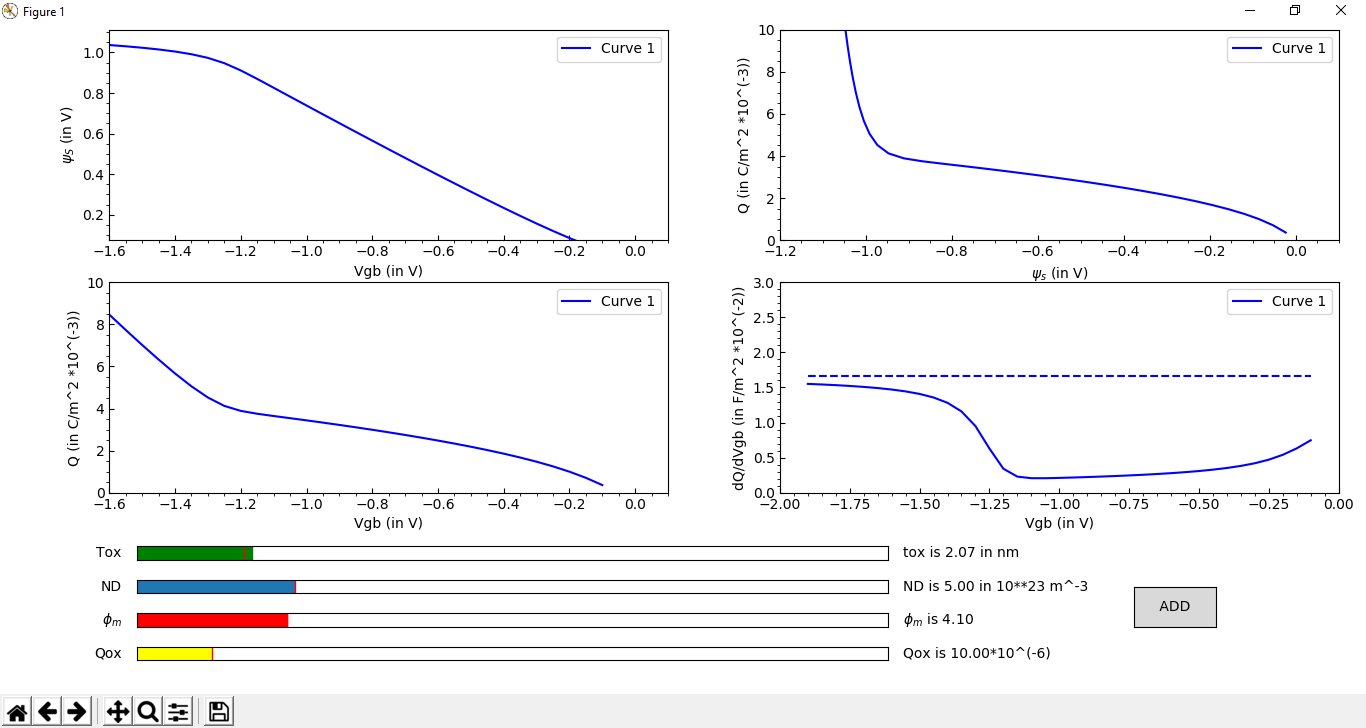


Figure 4: the results of the p type body MOS Capacitor

I have also solved the poison equation to get the equation of ѱ wrt to the distance y into the bulk material from the surface of semiconductor.

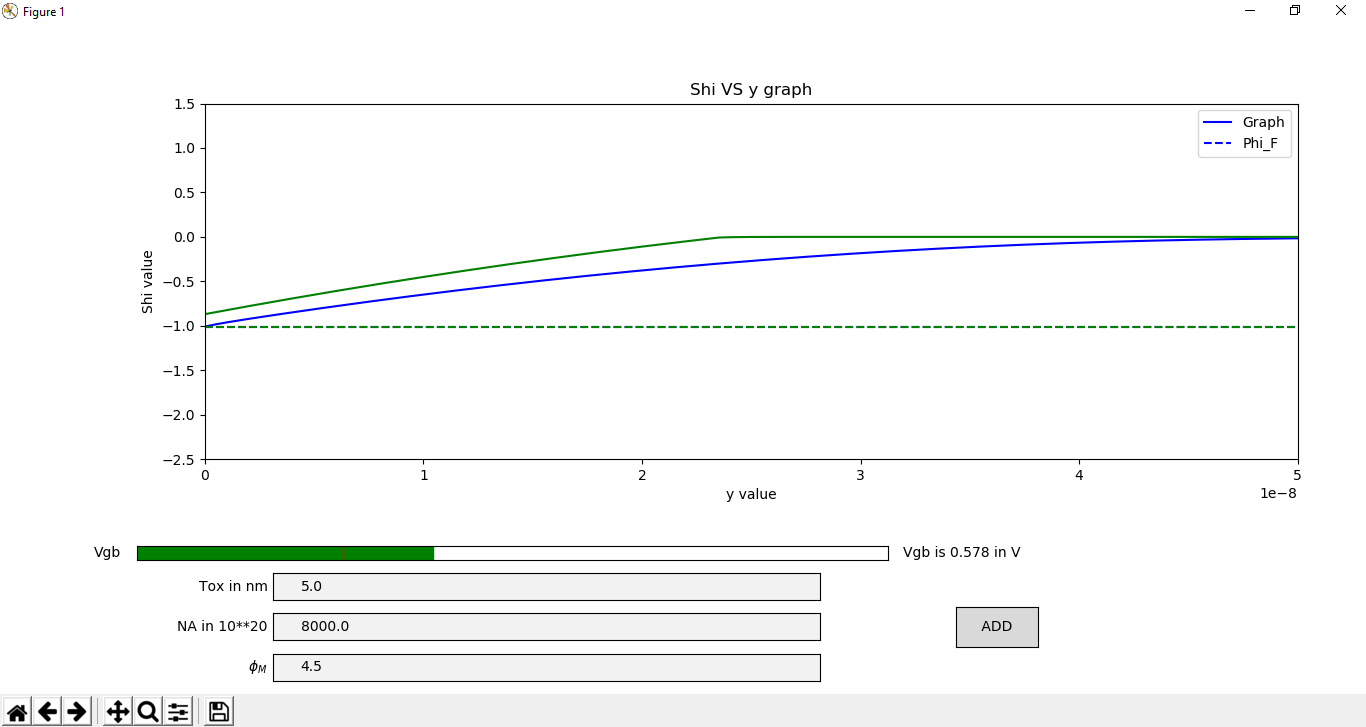


Figure 5: the results of the graph between ѱ wrt to the distance y

In my tool, the user can also add graphs by clicking on the ADD button given in the bottom right.

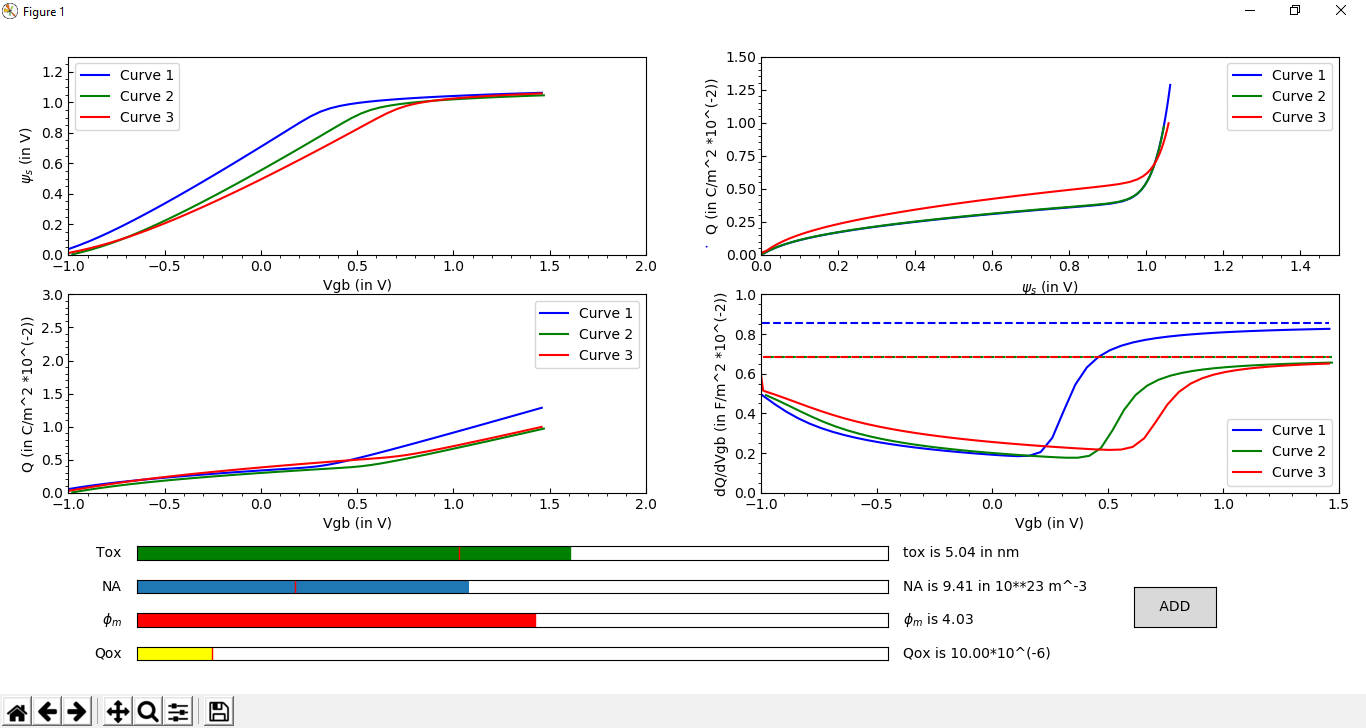
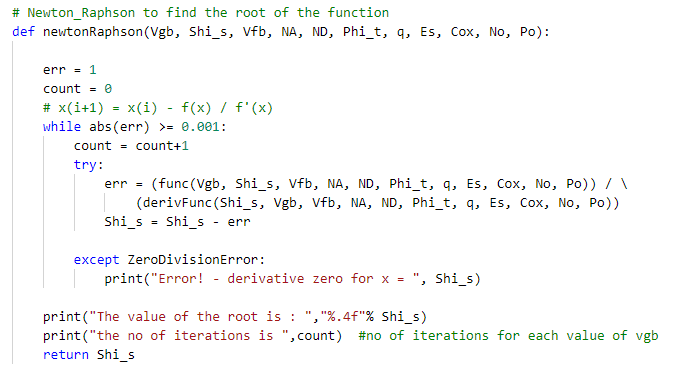
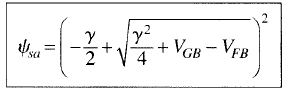


Figure 6: Addition of graphs for comparison purpose

The equation of VGB is not a linear function of ѱs . It’s a transcendental function of ѱ. It’s not easy to solve such equation. One of the ways of finding the root is using Newton Raphson method. It produces successively better approximations to the roots (or zeroes) of a real-valued function. The idea is to start with an initial guess which is reasonably close to the true root, then to approximate the function by its tangent line using calculus, and finally to compute the x-intercept of this tangent line by elementary algebra. This x-intercept will typically be a better approximation to the original function's root than the first guess, and the method can be iterated successively to find the approximate root. Now in Python,I have written the algorithm for the Newton Raphson method. From this, we can calculate the approximate values of the substrate potential in different regions (depletion, weak inversion, moderate inversion, strong inversion).



The approximate number of iterations of Newton Raphson for the VGB function varies from 2-5. This causes a little lag while changing the parameters and plotting graphs again. The number of iterations mostly depends on the initial value given to the Newton Raphson function. For finding the initial value I have considered the approximate value of ѱs in Depletion as well as Inversion region. The approximate value in the Depletion condition is :-



And, in the Inversion condition is :-



Where ∆Φ = 6\*ΦT , for uniform substrate.

The graph below shows the plot of the approximate solution

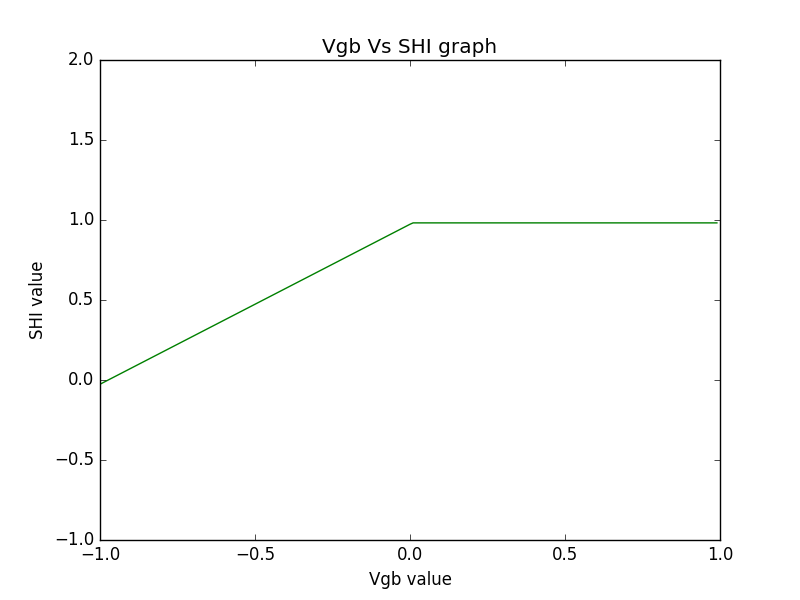


Figure 7: the approximate values for initial conditions of Newton Raphson method

I have also verified the graph of the Surface potential Vs Gate substrate potential from the (Gildenblat, Hailing Wang, Ten-Lon Chen, Xin Gu, & Xiaowen Cai, 2004) and got the data points from online WebPlotDigitizer App. The graph made by my tool matched completely with the graph made from the paper.

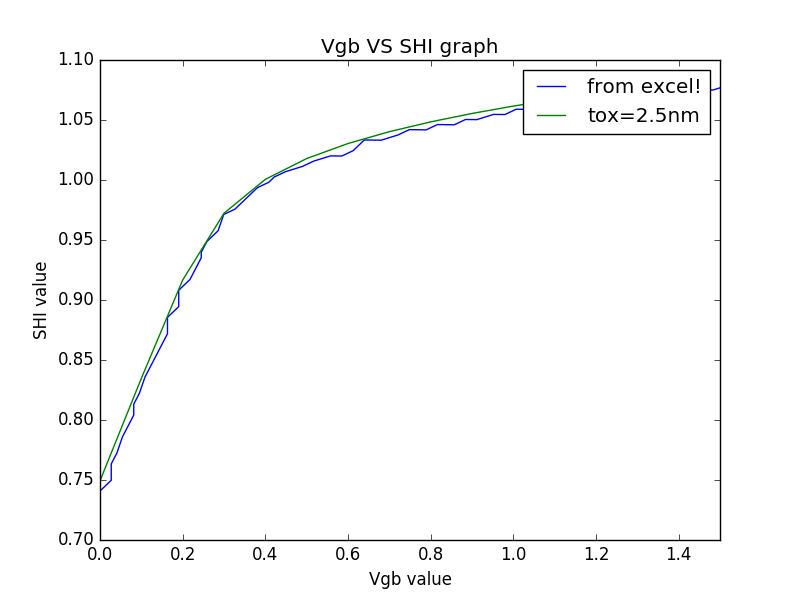


Figure 8: Verification of VGB Vs ѱs graph

# Terminal MOSFET Structure

## **Introduction**

A complete MOS transistor is formed by adding two more terminal to the basic MOS Capacitor structure to contact two opposite ends of the inversion layer. But properties that are not directly associated with the current can be studied by isolating the MOS and making a simpler structure called the 3 Terminal MOS. This is formed by contacting the inversion layer of the basic MOS structure at only one end. So now we can study the changes that take place in the charges and the potential distribution of the 3 terminal structure, caused by the application of an external voltage between this new terminal and the substrate. The 3rd terminal can be denoted by C as it is the contact to the inversion layer. It can be source or a drain terminal.

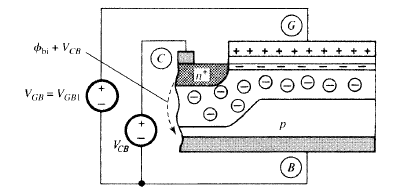


Figure 9: Basic 3 terminal MOS structure

## Changes with the variation of VCB

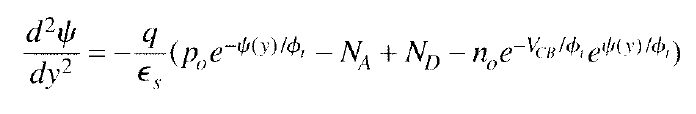
Considering n+ terminal and the p type body,

1. When VGB=VFB and the C terminal is short-circuited with the body terminal, no difference is obtained and the basic equations remains the same as the 2 terminal structure.
2. When VGB=VFB and still the C terminal is short-circuited, a narrow depletion region is formed in the body near the n+ terminal. The n+region is at a potential Φbi wrt the p region body, where Φbi is the built-in potential of the junction. The potential at the surface of the p region wrt deep in the body is 0. Thus the potential drop from the n+ region, along the surface, to the p region is Φbi.
3. When a potential V**CB** is applied to the C terminal, the total potential vertically across the n+ p region will increase to Φbi +Vcb. The electron density at the surface of the body will decrease. In fact if VCB is large enough, the inversion layer can disappear all together.

Total balance equations are given by :-

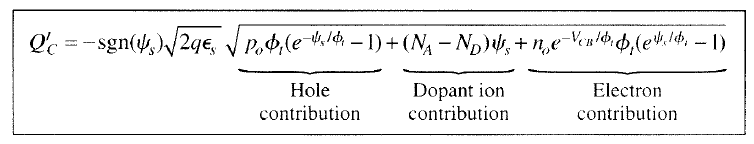
* Potential balance- V**CB** = ѱox + ѱs + ΦMS
* Charge equation- Q’g + Q’o + Q’c = 0
* The bulk charge potential relation Q’c = Q’c (ѱs, V**CB**)
* The gate charge potential relation Q’g= C’ox\* ѱox

Similar to the MOS Capacitor, the Poison equation for the 3 terminal MOS is given by

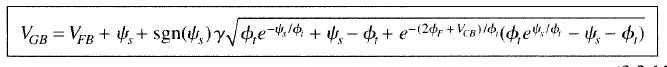


The difference in equation from the MOS Cap is here no is replaced by no\*e(-Vcb/Φt) where VCB is a constant independent of ѱ(y).

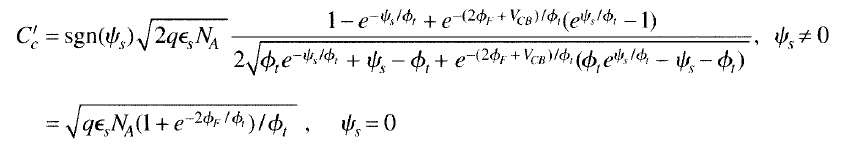
Solving the equation we can get,



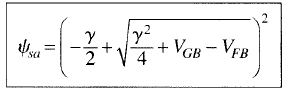
Finally, the equation for the Gate-Body Volatge is given by :-



Assuming that VCB is constant, the capacitance per unit area associated with the total semiconductor charge is defined by :-



Similarly, the roots of the equation is found out by using the Newton Raphson method. Only there is a change in the function equation as well as in the initial values given to the Newton Raphson method. In the depletion region, the initial value is given by :-



And in the inversion region is given by :-



Where , 

And ∆Φ = 6\*ΦT , for uniform substrate.

Using my python code i.e. I have used the matplotlib to plot the graphs of these equations. Similar to MOS Cap, there are 4 graphs in each window for both nMOS and pMOS :-

1. Ѱ­s Vs VGB
2. Q’c Vs Ѱ­s
3. Q’c Vs VGB
4. C’c Vs VGB

Also, similar features are present in this window.

I have got the following results :-

## N type body MOS

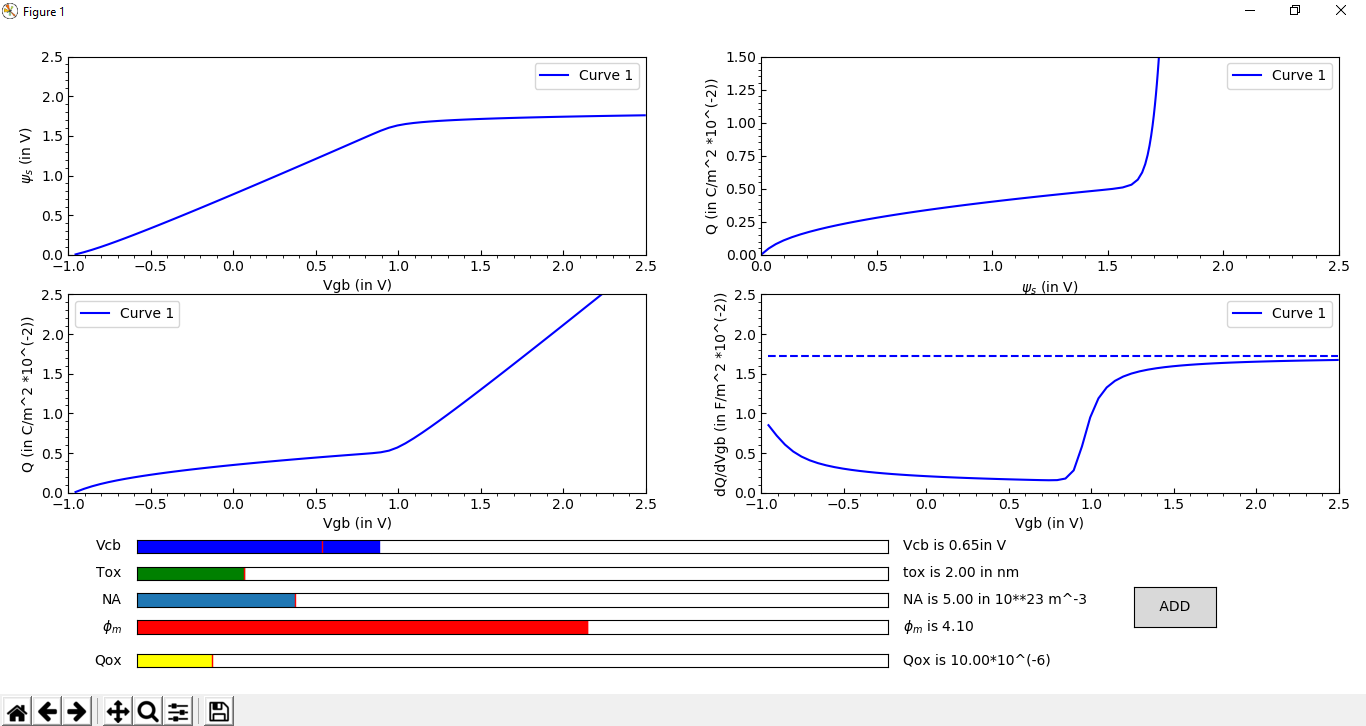


Figure 10: the results of the n type body 3 terminal structure

## P type body MOS

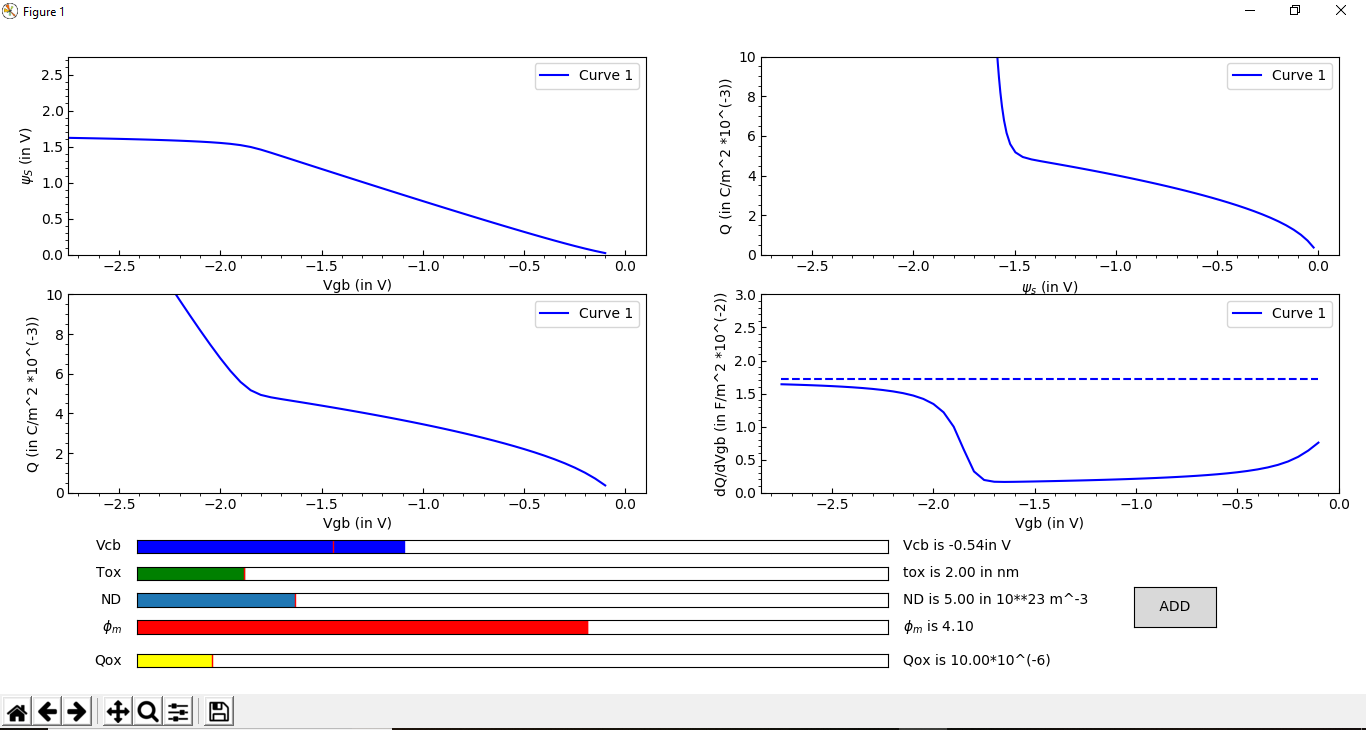


Figure 11: the results of the p type body 3 terminal structure

Now plotting the graph of ѱs Vs VCB, we get

## For nMOS:-

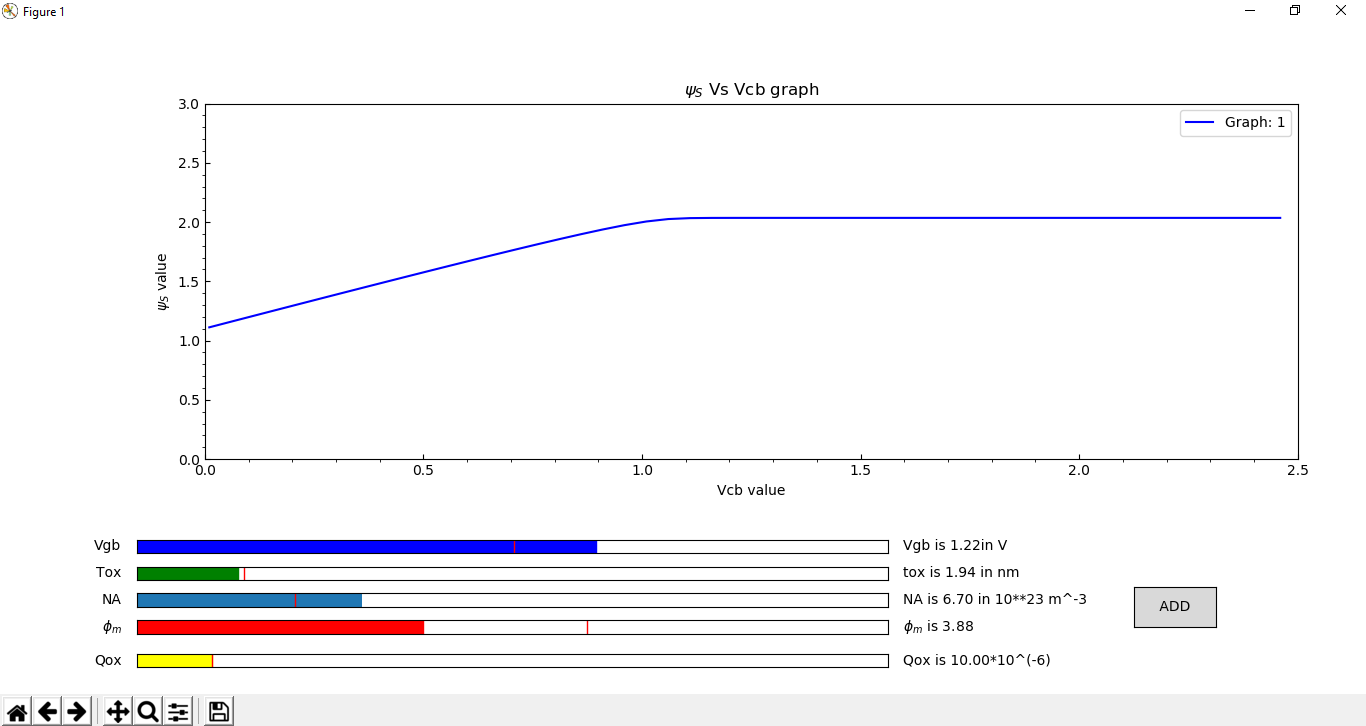


Figure 12: the graph of ѱs Vs VCB in nMOS

## For pMOS:-

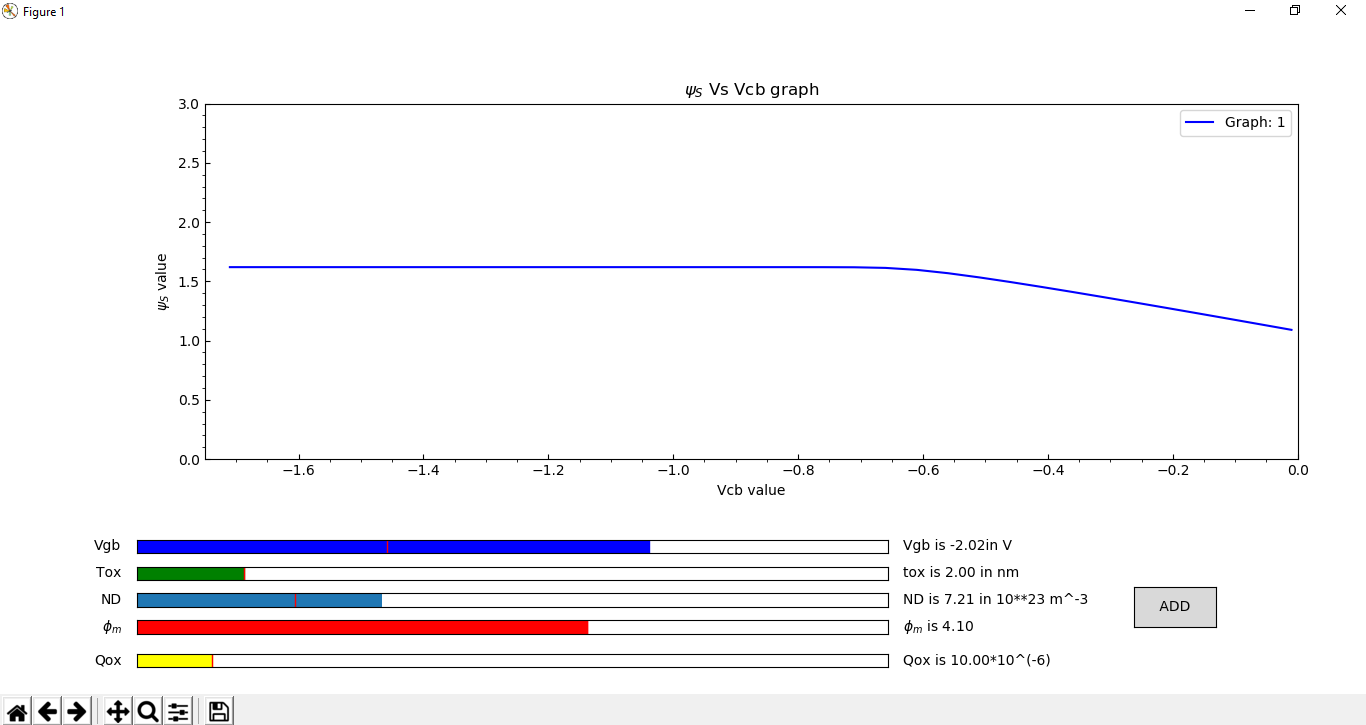


Figure 13: the graph of ѱs Vs VCB in pMOS

# Terminal MOS Structure

## Introduction

The whole complete MOS transistor is obtained by adding another terminal to the 3 terminal MOS Structure so that the inversion layer is contacted at two opposite ends. By applying a voltage between these ends, a current will flow in the inversion layer. Since the density of carrier available for conduction depends on the gate potential, the latter can be used to either create or eliminate the inversion layer. In this, our main goal will be to determine the drain current for any combination of dc terminal voltages. Throughout the work, we will assume the channel is sufficiently long and wide, so that edge effects are confined to a negligible part and the substrate is uniformly doped. Normal operation of a MOS transistor requires that both pn junctions be reverse biased. Now in this we will consider two voltages that are: VSB (Source-Body voltage) and VDB (Drain-Source voltage). Thus for normal operation, in case of a nMOS transistor both the voltages must be greater than equal to 0.

The current in the channel is caused by both the drift current and the diffusion current. Let x be the horizontal position in the channel, measured from the source end. If the inversion layer current at x is denoted by I(x), we will have



Drift current in MOS is because of the majority carriers. In case of MOS, the drift current increases with increase in the applied voltage till the Velocity saturation.

Diffusion current is a current in a semiconductor caused by the diffusion of the charge carriers (holes or electrons).This current is very small and also known as the leakage current.

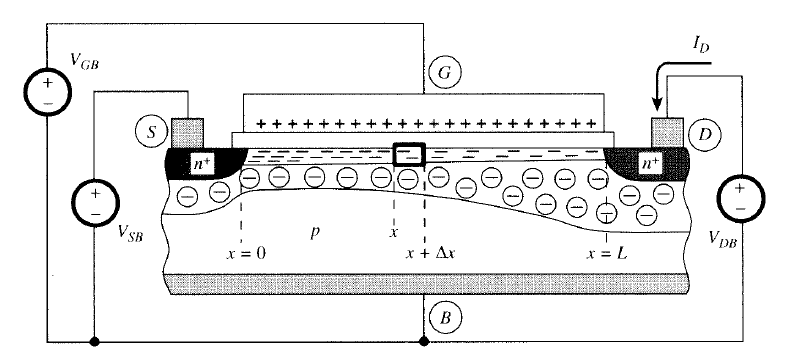
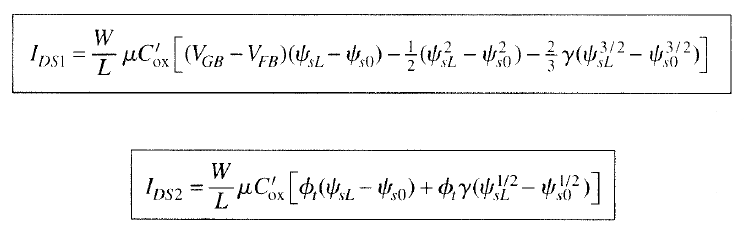


Figure 14: Basic 4 terminal MOSFET structure

So the total drain current can be written as the summation of Drift current Ids1 and Diffusion current Ids2.

The equations of these currents are :-

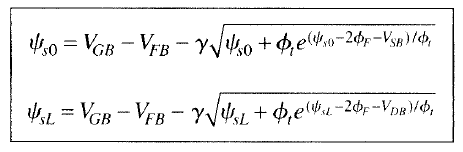


Where ѱs0 is the surface potential at the source end of the channel (x=0) and

ѱsL is the surface potential at the drain end of the channel (x=L).

## Evaluating ѱs0 and ѱsL

From the previous equation of Gate-body voltage from the 3 terminal MOS, we can get the value of ѱs0 at the source end and the value of ѱsL at the drain end. The equations are given below :-



Similarly, these equations can be solved by using the Newton Raphson method. The initial values to the Newton Raphson method is similar to the ones given in the 3 terminal MOS.

After evaluating the values, those are put in the equations of the drift and the diffusion current to find out the total current.

Now I have plotted four graphs, two each of pMOS and nMOS:-

## NMOS

Id Vs Vgs:-

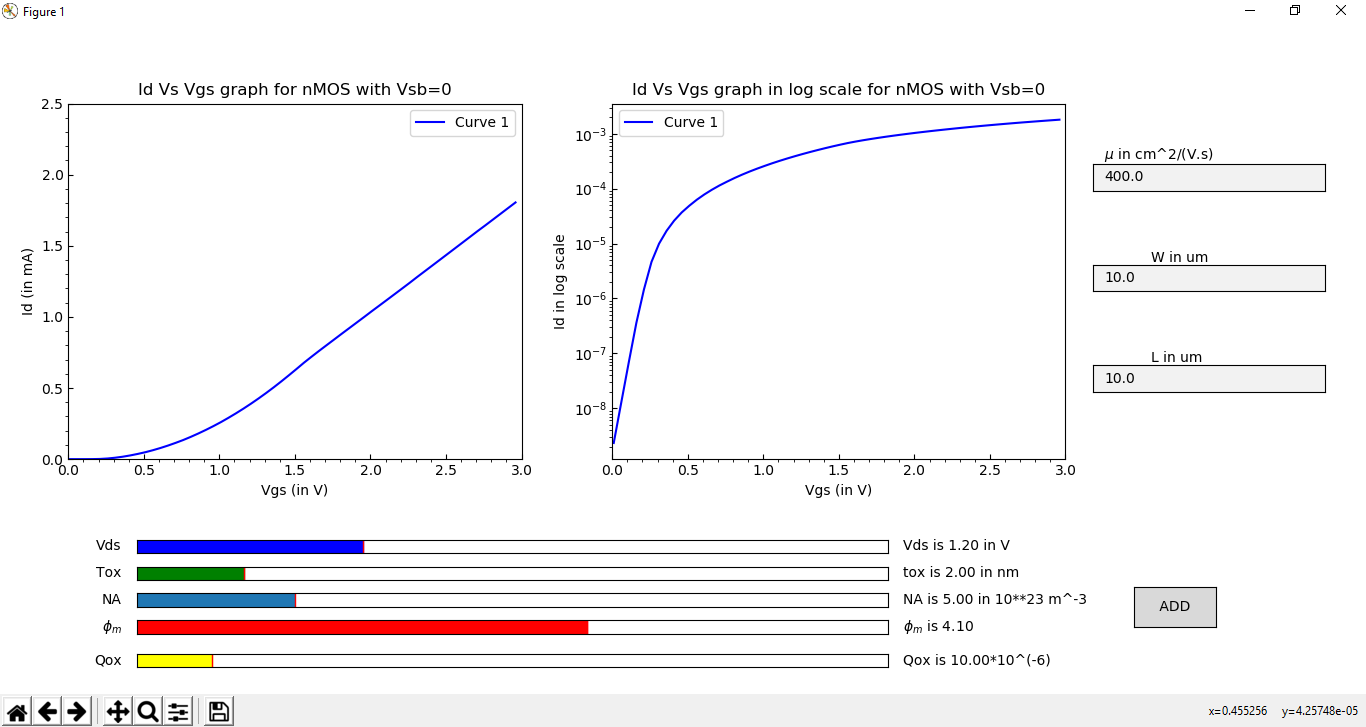


Figure 15: the graph of Ids Vs VGS in nMOS

Id Vs Vds:-

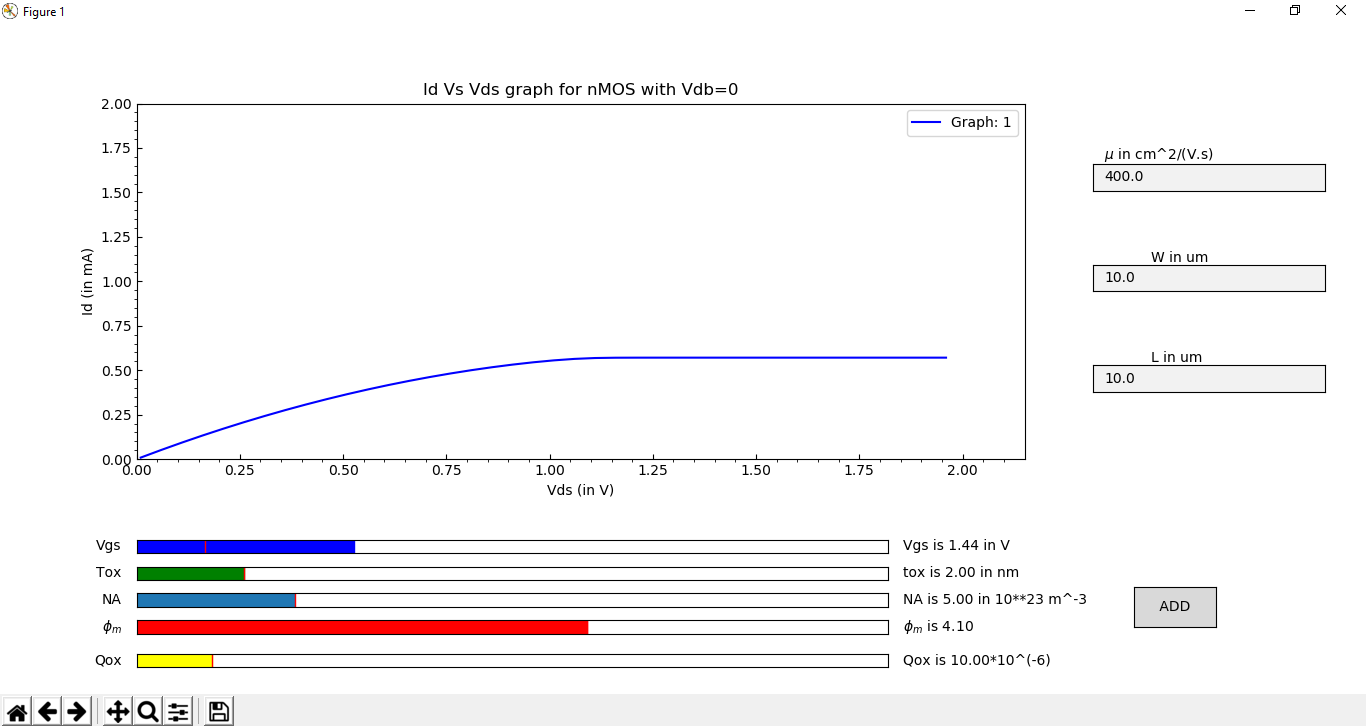


Figure 16: the graph of Ids Vs VDS in nMOS

## PMOS:-

Id Vs Vgs:-

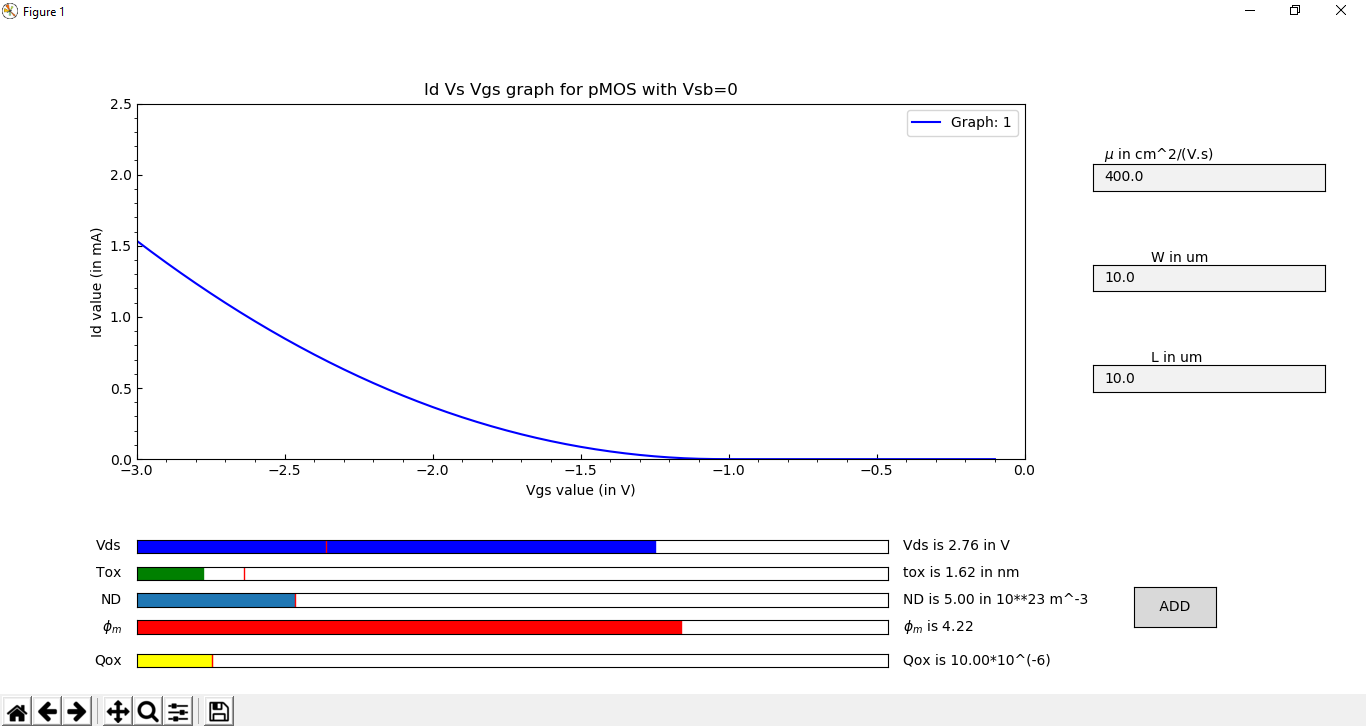


Figure 17: the graph of Ids Vs VGS in pMOS

Id Vs Vds:-

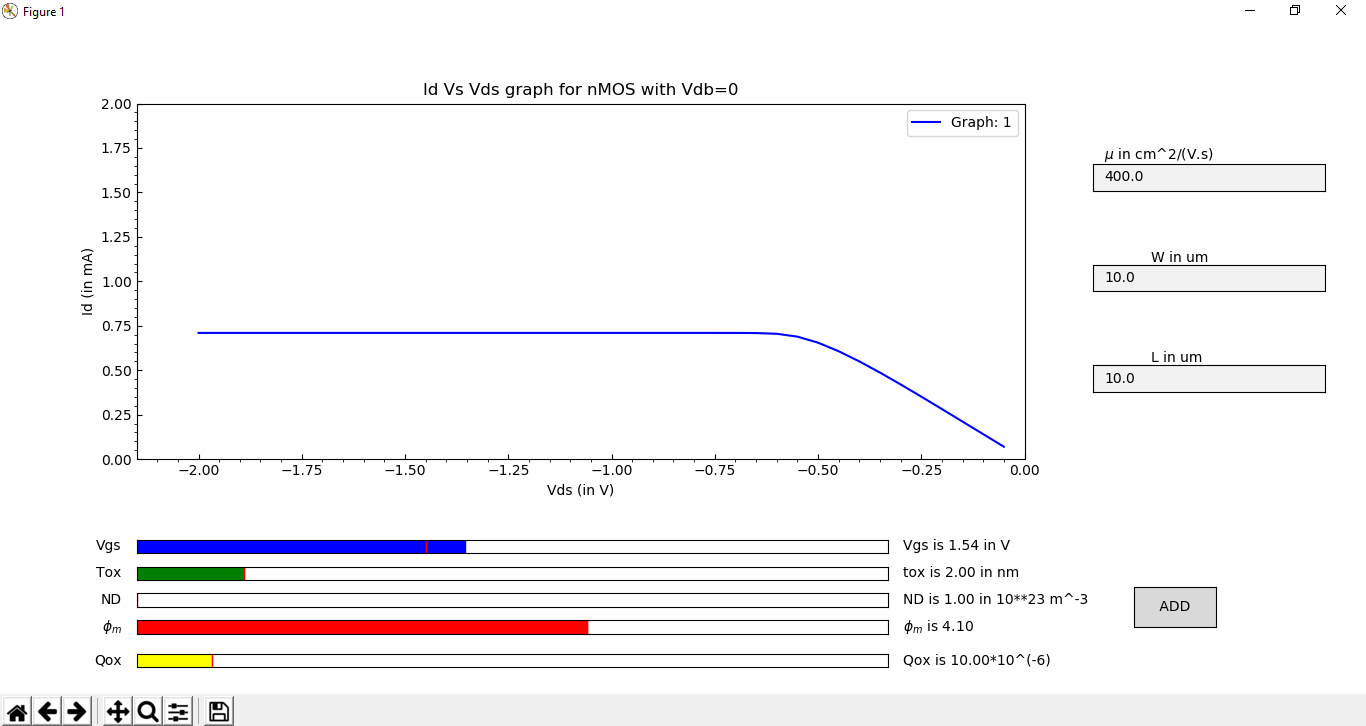


Figure 18: the graph of Ids Vs VDS in pMOS

Also I have verified the graph of Id Vs Vgs of nMOS with a IEEE journal paper (Taur, Liang, Wang, & Lu, 2004) and results almost matched.



Figure 19: the verification of graph of Ids Vs VGS in nMOS

Similarly, I have also verified the graph of Id Vs Vds of nMOS with the same IEEE paper (Taur et al., 2004) and the graph of my tool matched with that.

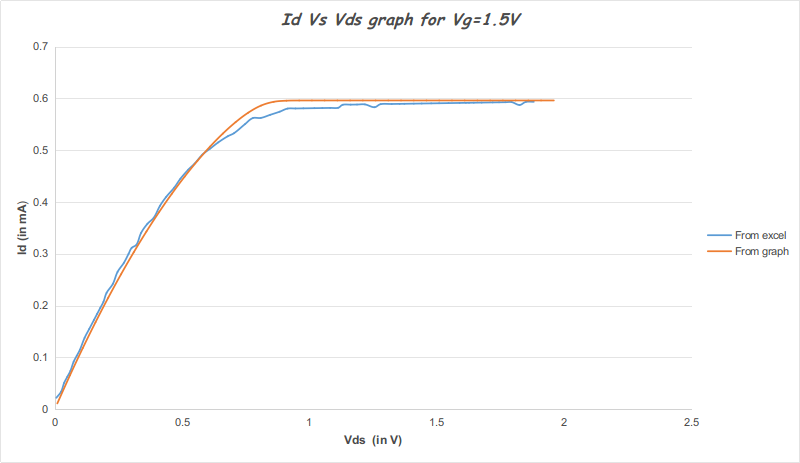


Figure 20: the verification of graph of Ids Vs VDS in nMOS

# Conclusion and Discussion

Overall from the project, I got a good programming knowledge of Python and using different libraries and packages of the Python. Also I learnt a lot more about the MOSFET electrostatics, getting more information about the different structures of the MOS and the result of variation of the different parameters. The advances in MOS technology have been obtained through continuous miniaturization of the devices. This has led to the development of the many analog and digital devices. The continuous aggressive downscaling for the higher density, the better performance and the low power consumption of MOSFETs leads to growth and development of the different devices. So my tool will be very helpful in the research work as well as in the demonstration purpose while learning the theories of the MOS. Visual demonstrations will give a better understanding of the MOSFET. This tool can also plot the graphs in much less time than simulating in other softwares like TCAD, etc . Well, this project can be extended more by plotting the graphs in the accumulation region also. Also the GUI can be more improved and attractive. The tool can also be extended to plot more graphs and making it more interactive for the user. Also one can add more features like saving the data points in an excel sheet.

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