

CHAPTER - 6

Bipolar Junction Transistor (BJT)

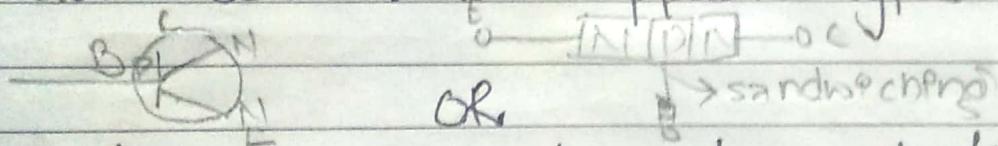
Transistor \rightarrow Transfer + Resistor

Current is due to both types of charge carriers

Light weight
Simple to construct
and long lasting

Definition:-

The transistor consist of two pn junctions (or two diodes) formed by sandwiching either p-type or n-type semiconductor between two opposite types.



A transistor is a three terminal, bipolar semiconductor device where current flows through a low resistance path to a high resistance path.

It is a bipolar devices because current conduction takes place due to both electrons and holes within the transistor

It is a current controlled devices where output current is controlled by input current.

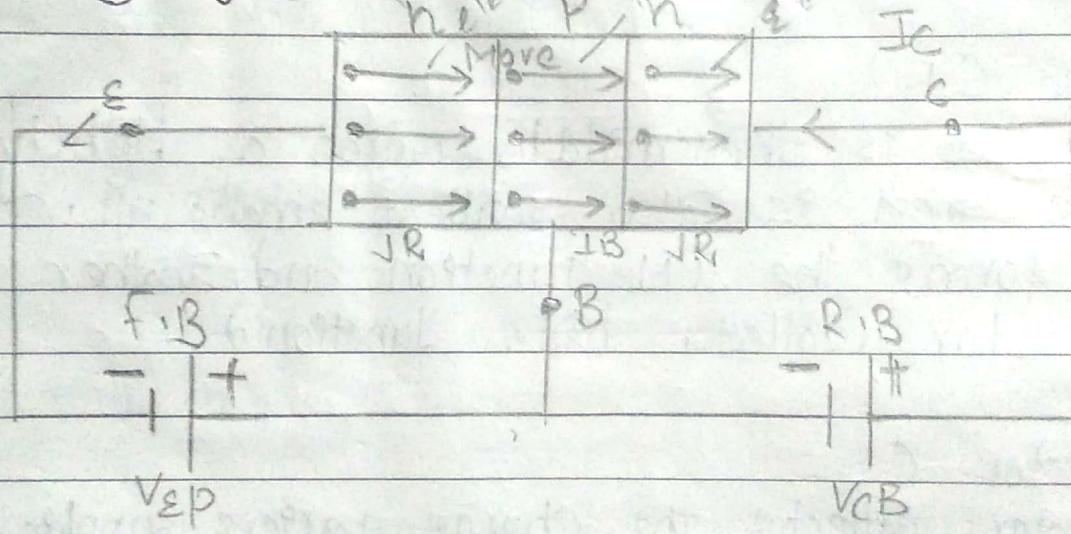
The arrow always goes from positive to negative.

↳ Transistor emits charge carriers and those charge carriers transfer from low-resistance path to a high-resistance path.

↳ Transistor action can be explained with its working principle.

Imp

Working of npn transistor



$$I_E = I_C + I_B$$

NPN transistor is a type of bipolar transistor that has 3 layers and is used for signal amplification. It is a current controlled device.

NPN is an abbreviation used for a negative positive negative transistor. This means a p-type semiconductor is used between 2 n-type semiconductor material.

Due to the variation in temp under no biased condition electrons in the emitter region starts moving towards the base region. But after a certain point of time a depletion region is created at emitter-base junction of transistor.

- ↳ Doping Concentration is responsible for thickness or thinness of depletion region. We achieve broader depletion width at the collector-base junction than the emitter base junction.
- ↳ When a voltage is applied to the terminals of transistor. The emitter base junction is forward provided forward dc voltage and the collector-base junction is supplied with a reverse dc voltage.
- ↳ Due to forward applied voltage the width of depletion region gets narrowed. As base region is very thin and lightly doped very few electrons gets combined with holes, And because of reverse voltage at collector base junction the electron start to drift at collector region because of strong electrostatic field.
- ↳ As electron start moving toward collector, a very small base current flows through the device

↳ This is why emitter current is the sum of sum of base current and collector current.

$$\text{ie. } I_E = I_C + I_B$$

~~Ans~~ Explain the Transistor as an amplifier

Transistor as an amplifier

Q) No transistor can used as amplifier

Amplifier :-

→ An amplifier is an electronic circuit which raises the strength of a weak signal.

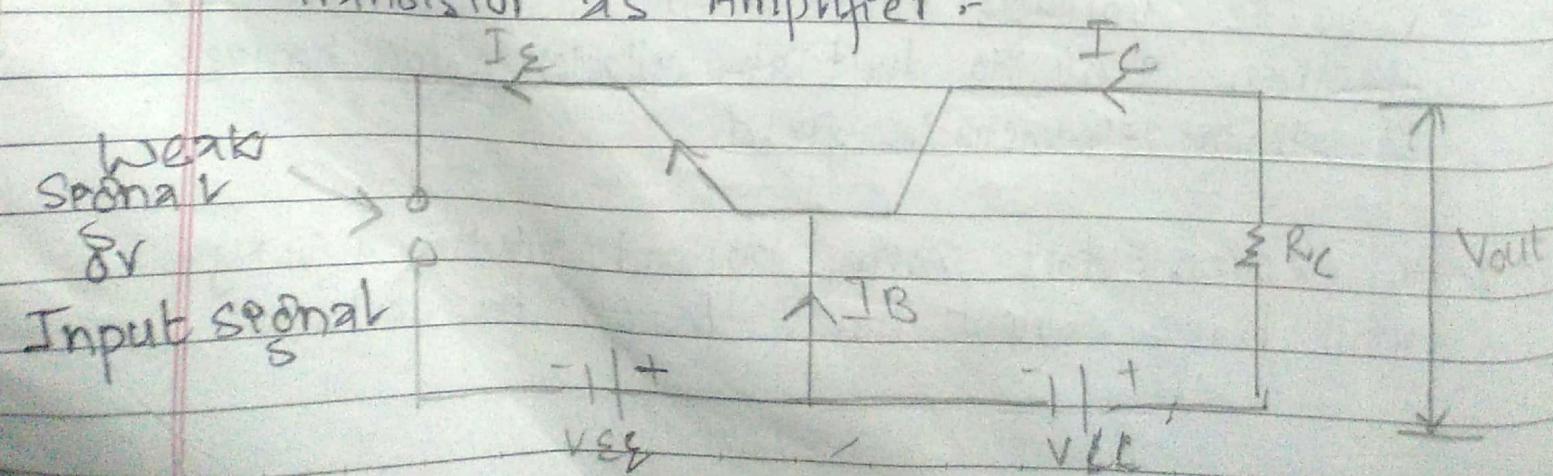
→ Transistor is used as an amplifier.

~~Ans~~ Transistor as Amplifier :-

- Faithfull amplification :-

If an amplifier amplifies the weak signal (input signal) such that the input-output waveform (or wave shape) does not change it is called faithful amplification.

Transistor as Amplifier :-





→ To use transistor as an amplifier, base, emitter junction must be forward biased, it is done by bias voltage V_{BE} . Similarly collector base junction must be reverse biased if it is done by bias voltage V_{BC} .

⇒ When an input signal (weak) is applied across the base emitter junction, it produces emitter current I_E . Since $I_E \approx I_C$ and I_C is the output current or collector current. Since the value of load resistance R_C is higher, then the output voltage which is the voltage drop across R_C having strength higher than input voltage.

∴ Hence, transistor can be used as an amplifier.

For example, let input voltage, $V_{IN} = 1mV$ input current, $I_E = 1mA$

$$\begin{aligned} \text{Since, } I_E &\approx I_C = 1mA \\ \therefore V_{OUT} &= I_C R_C \\ &= 1mA \times 2k\Omega \\ (\text{Here, } R_C &= 2k\Omega, \text{ assumed}) \\ \therefore V_{OUT} &= 2V \end{aligned}$$

→ To use transistor as an amplifier, base, emitter junction must be forward biased, it is done by bias voltage V_{BE} . Similarly collector base junction must be reverse biased if it is done by bias voltage V_{BC} .

⇒ When an input signal (weak) is applied across the base emitter junction, it produces emitter current I_E . Since $I_E \approx I_C$ and I_C is the output current or collector current. Since the value of load resistance R_C is higher, then the output voltage which is the voltage drop across R_C having strength higher than input voltage.

∴ Hence, transistor can be used as an amplifier.

for example, let input voltage, $V_{IN} = 1mV$
input current, $I_E = 1mA$

Since, $I_E \approx I_C = 1mA$

$$+ V_{OUT} = I_C R_C$$

$$= 1mA \times 2k\Omega$$

(Here, $R_C = 2k\Omega$; assumed)

$$\therefore V_{OUT} = 2V$$

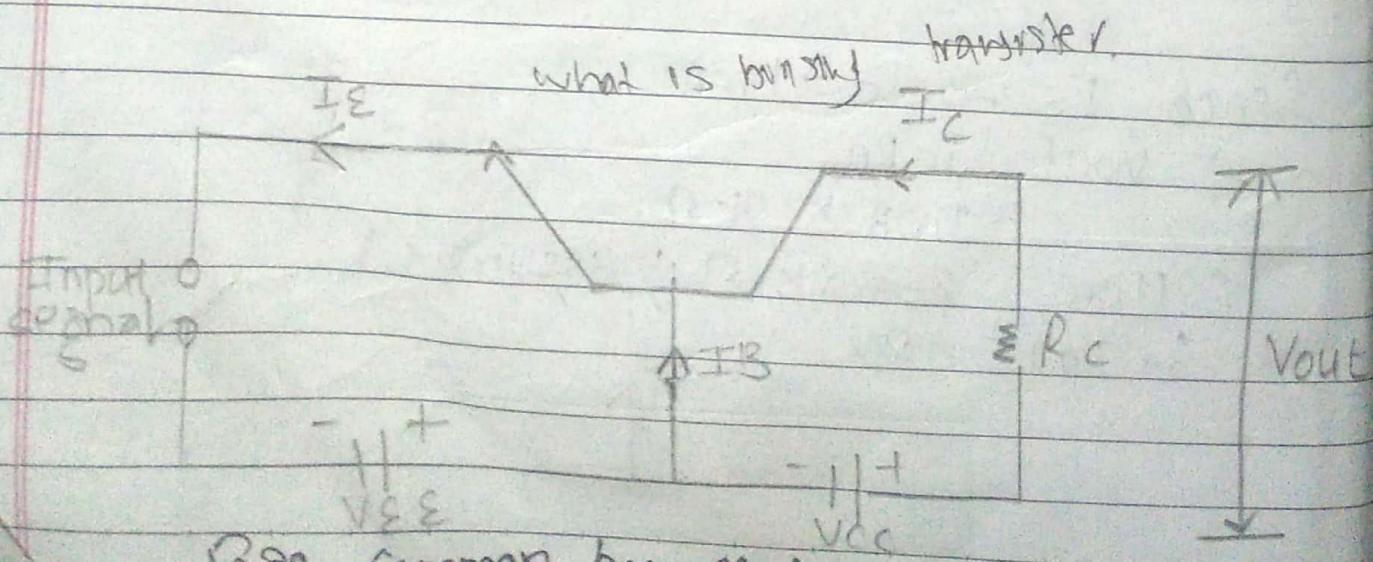
Therefore, for 1mv input voltage transistor produces 2v at the output. Hence transistor can be used as an amplifier.

Transistor Connection or Transistor Configuration.

→ A transistor is a three terminal device. But to operate it in electronic circuit, it needs four terminal common for input circuit and output circuit. Accordingly there are 3 transistor connections as:-

- ① Common Base (CB) connection
- ② Common Emitter (CE) connection - widely used.
- ③ Common collector (CC) connection

① Common Base (CB) transistor connection :-



Ans:- Common base (CB) transistor

↳ Here, base terminal is common for both input circuit for base-emitter circuit and output circuit (or collector-base circuit) hence the name CB connection.

→ The i/p signal is applied at the input circuit and o/p signal is obtained at output circuit R_C is the load resistance.

② Current amplification factor (α)

↳ Also called current gain.

↳ It is the ratio of output current (I_C) to the input current (I_E). Therefore,

$$\alpha = \frac{I_C}{I_E} - ①$$

(dc gain)

For simplicity,
dc gain is equal
to the ac gain.

$$\alpha = \frac{\Delta I_C}{\Delta I_E} - ②$$

(ac gain)

It is the ratio of change in collector current to the change in emitter current.

↳ Here, base terminal is common for both input circuit for base-emitter circuit and output circuit (or collector-base circuit) hence the name CB connection.

→ The ac signal is applied at the input circuit and ac signal is obtained at output circuit R_C is the load resistance.

② Current amplification factor (α)

↳ Also called current gain.

↳ It is the ratio of output current (I_C) to the input current (I_E). Therefore,

$$\alpha = \frac{I_C}{I_E} - ①$$

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dc gain is equal
to the ac gain.

$$\alpha = \frac{\Delta I_C}{\Delta I_E} - ②$$

(ac gain)

It is the ratio of change in collector current to the change in emitter current.

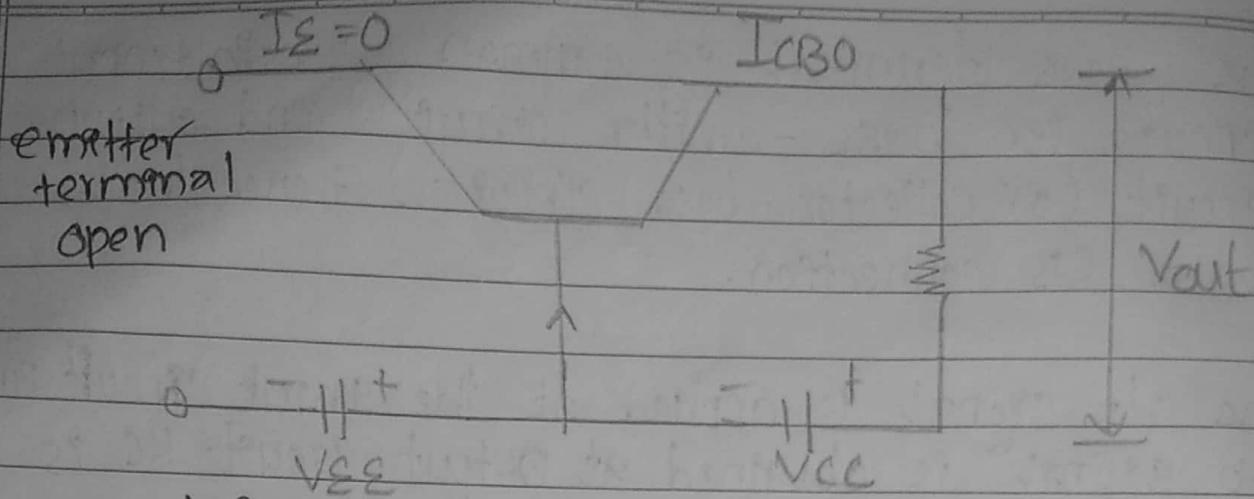


fig:- common Base (CB) transistor connection

(b) Expression for the collector current (I_{CBO}):-

- It is denoted by I_{CBO} which is the collector to base current with emitter open. This is due to the reverse bias collector base circuit.
- ∴ Therefore, the total collector current includes

① The part of emitter current which reaches the collector, ie. $I_c = \alpha I_E$, and

② The leakage current I_{CBO}

$$\text{∴ } I_c = \alpha I_E + I_{CBO}$$

$$\text{But } I_E = I_c + I_B$$

$$I_c = \alpha (I_c + I_B) + I_{CBO}$$

$$I_c - \alpha I_c = \alpha I_B + I_{CBO}$$

$$I_c (1 - \alpha) = \alpha I_B + I_{CBO}$$

$$\therefore I_c = \frac{\alpha}{1 - \alpha} I_B + \frac{I_{CBO}}{1 - \alpha}$$

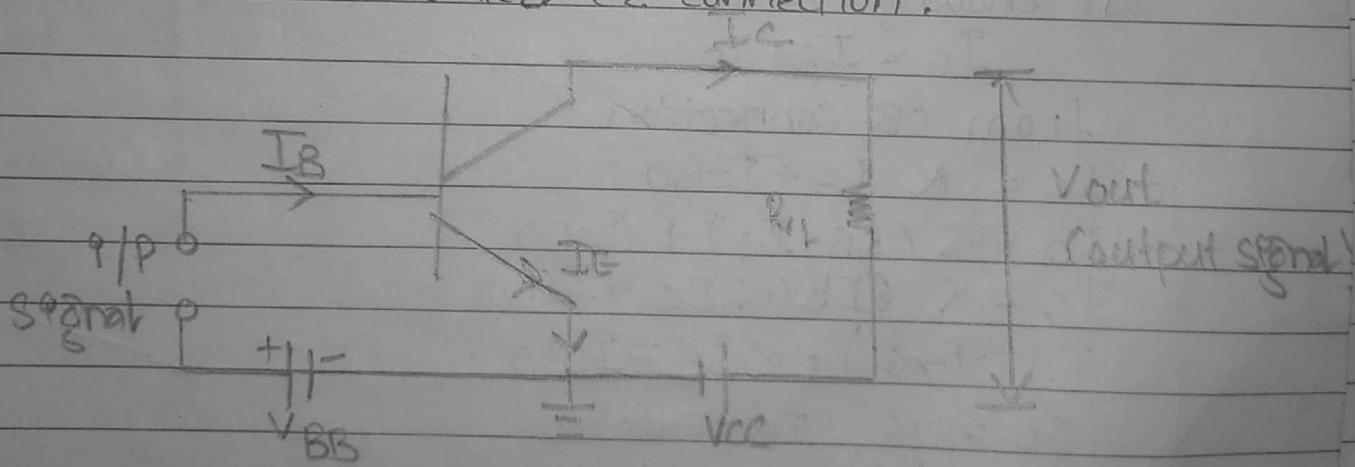
Which is the required expression for collector current.

(Q) Output resistance (r_o):-

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C} \quad | \quad I_S = \text{constant} \quad \left. \right\}$$

(Q) Common Emitter (CE) connection:-

Here Input is applied at base and emitter and output is taken from the collector and emitter. Since emitter is common for both i/p & o/p circuits, this connection is called CE connection.



(Q) Current amplification factor (β):-

It is the ratio of output current (I_C) to the input current (I_B)

$$\therefore \beta = \frac{I_C}{I_B} - ①$$

(dc gain)

$$\beta = \frac{\Delta I_C}{\Delta I_B} (\text{ac gain}) - ②$$

For simplicity:-

$$\text{dc gain} = \text{ac gain}$$

and $\beta > 1$ because $I_C \geq I_B$

(b) Expression for collector current :-

We know ;

$$I_S = I_B + I_C$$

from CB connection

$$I_C = \alpha I_S + I_{CBO}$$

$$I_C = \alpha (I_B + I_C) + I_{CBO}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C (1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + I_{CBO} - ③$$

(2) Common Emitter (C_E) connection:-

Imp. Where, $I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$

$I_{CEO} \rightarrow$ collector to emitter current with base open

$$I_C = \beta I_B + I_{CEO} - \textcircled{1}$$

where, $\beta = \frac{\alpha}{1-\alpha}$

(3) Relation Between α & β :- Explain relation.

We know;

$$I_E = I_C + I_B - \textcircled{1}$$

$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{I_C/I_E} = 1 + \frac{1}{I_C/I_B}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta} - \textcircled{2}$$

$$\frac{1}{\beta} = \frac{1}{\alpha} - 1$$

$$\frac{1}{\beta} = \frac{1-\alpha}{\alpha}$$

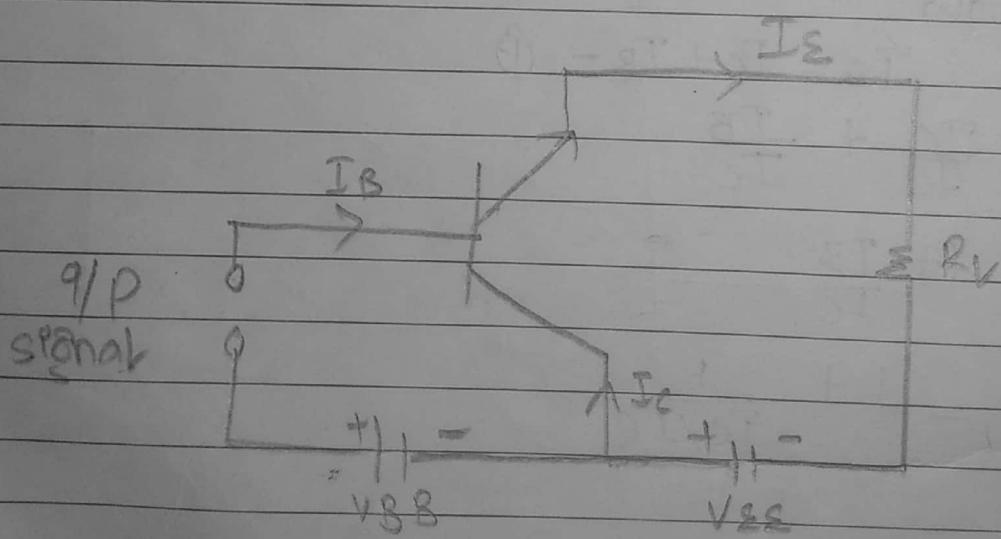
$$\beta = \frac{\alpha}{1-\alpha} - \textcircled{3}$$

Again from $\textcircled{2}$

$$\frac{1}{\alpha} = \frac{\beta + 1}{\beta}$$

$$\alpha = \frac{\beta}{\beta + 1} - \textcircled{4}$$

$\textcircled{5}$) CC connection :- (Common collector)



R_L = Load Resistance

$$Y = \frac{I_E}{I_B}$$

$$r >> 1$$

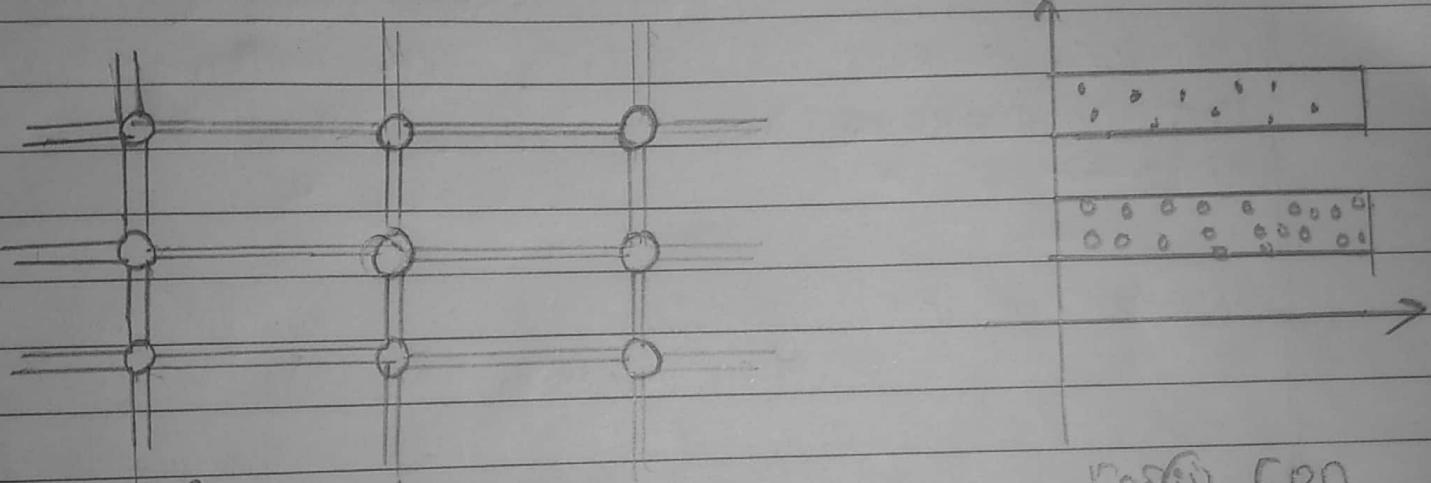
$$Y = \frac{I_C + I_B}{I_B}$$

$$r = B + 1$$

$$\therefore Y = \frac{K}{1+\alpha} + 1 \approx$$

p-type semiconductor

The extrinsic p-type semiconductor is formed when a trivalent impurity is added to pure semiconductor in a small amount, as a result, a large number of holes are created in it.



fig(i) Energy structure

Fig(ii) EBD

This type of semiconductor is obtained when traces of a trivalent impurity like Boron (B) are added to a pure silicon

The atoms with

BJT Biasing

Definition:-

- The proper flow of zero signal collector current (COP current) and the maintenance of the collector to emitter voltage COP voltage during the passage of the signal is called transistor biasing.

Biasing Circuit :-

- The circuit associated with transistor biasing is called biasing circuit.
- Biasing makes base-emitter junction always forward biased and collector-base junction always reverse biased. This is also called transistor 'turned on'.

~~Explain one~~

Method of Transistor Biasing:-

- (1) Fixed bias (or Base Resistor Bias)
- (2) Voltage Divider (or Potential divider Bias) *widely used.*
- (3) collector feedback bias *widely used.*
- (4) Emitter feedback bias

① Fixed bias (or Base Resistor Bias)

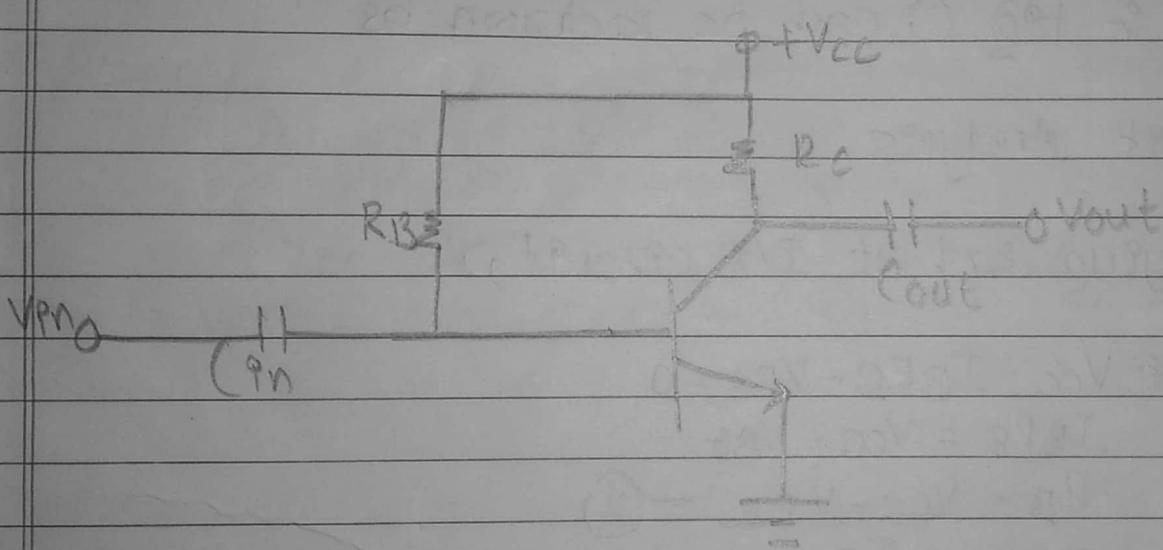


Fig:- circuit for fixed bias

For biasing, we use bc analysis.

To do this,

- (2) we remove ac signal sources, if any.
- (3) capacitors are open circuited, if any.

Relationship between α , β & γ in transistor

~~scribble~~

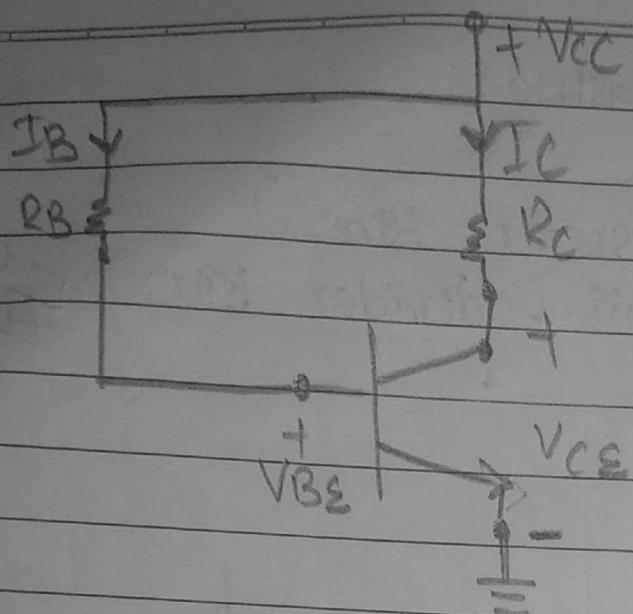


Fig ② :- Fig ① can be redrawn as

Circuit Analysis

Applying KVL at I/P circuit,

$$\text{V}_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad \text{--- (1)}$$

Since,

$$V_{CC} = \text{Fixed}$$

$$V_{BE} = 0.7V \text{ (fixed)}$$

then, this is called fixed bias because R_B is also fixed. Bias level established by base resistor, thus, also called base resistor bias.

Also,

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad (2)$$

But from CE connection,
we have,

$$\beta = \frac{I_C}{I_B}$$

$$\therefore I_C = \beta I_B \quad] - \quad (3)$$

Again,

Applying KVL at O/P circuit

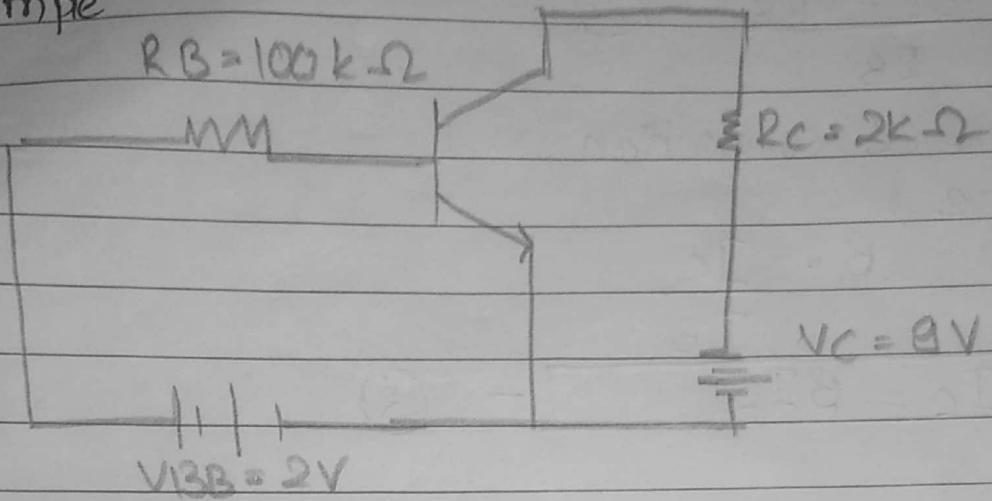
$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C - \quad (4)$$

Adv
dis

Q Example

$$R_B = 100\text{ k}\Omega$$

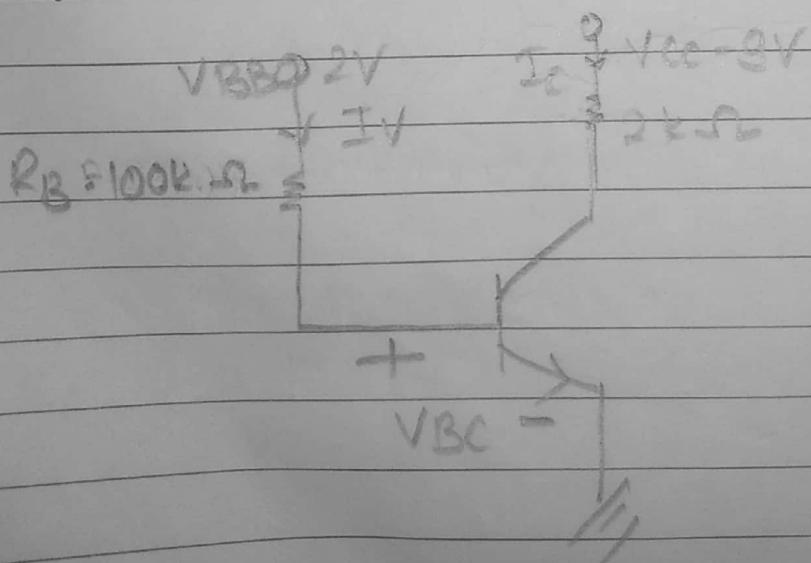


for above base biasing circuit

① Determine I_C if $V_{CE} = 8V$. Neglect small base-emitter voltage. Given $\beta = 50$

② If $R_B = 50\text{ k}\Omega$ find the new operating point.

Soln The circuit can be redrawn as;



Applying KVL at Q1P circuit

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$V_{BE} = 0$ (\because small + neglected, as given)

$$I_B = \frac{V_{BB}}{R_B} = \frac{2V}{100\text{k}\Omega} = 20\text{mA}$$

$$\begin{aligned} I_C &= \beta I_B = 50 \times 20\text{mA} \\ &= 1000\text{mA} \\ &= 1\text{mA} \end{aligned}$$

Applying KVL at Q1P circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_C R_C \\ &= 9 - 1\text{mA} \times 2\text{k}\Omega \\ &= 9 - 2 \\ &= 7\text{V} \end{aligned}$$

Ques.

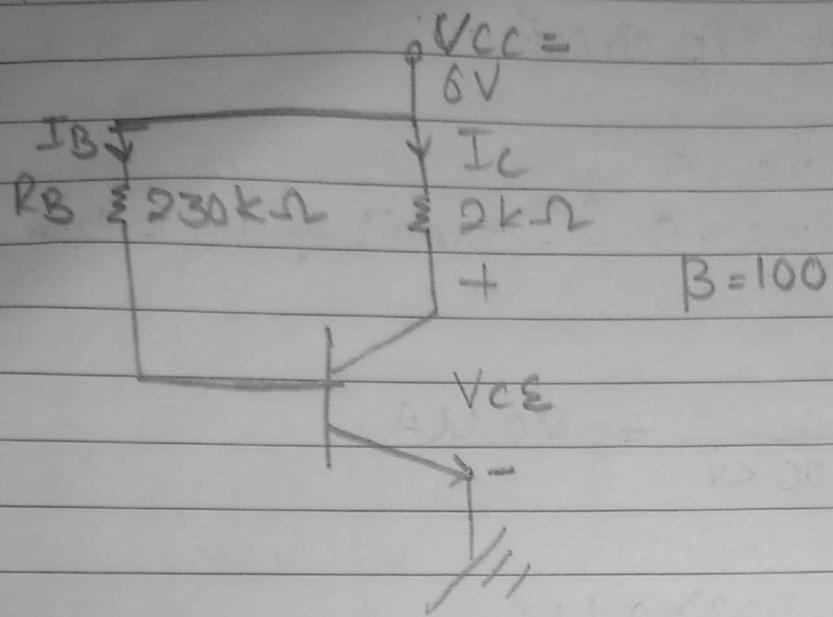


Fig shows the silicon transistor, is biased by base resistor method.

Draw dc load line and determine operating point

② Load line calculation:-

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C \quad (1)$$

Maximum current,

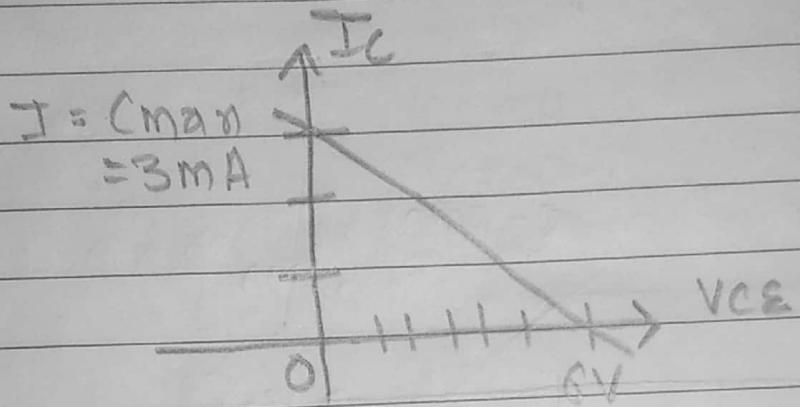
For this, make $V_{CE} = 0$

$$I_{C\max} = \frac{V_{CC}}{R_C} = \frac{6V}{2k\Omega} = 3mA$$

Maximum voltage V_{CE} max :-

for this,

$$\therefore V_{CE} \text{ max} = V_{CC} = 6V$$



Applying KVL at i/p circuit

$$V_{CC} - I_B R_C - V_{BE} = 0$$

But,

$V_{BE} = 0.7V$ for silicon transistor

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$= \frac{(6 - 0.7)}{530\text{k}\Omega} \text{V}$$

$$I_B = 10\text{nA}$$

$$\star I_C = \beta I_B$$

$$= 100 \times 10\text{nA} \quad I_C = 1\text{mA}$$

Principle of electronics

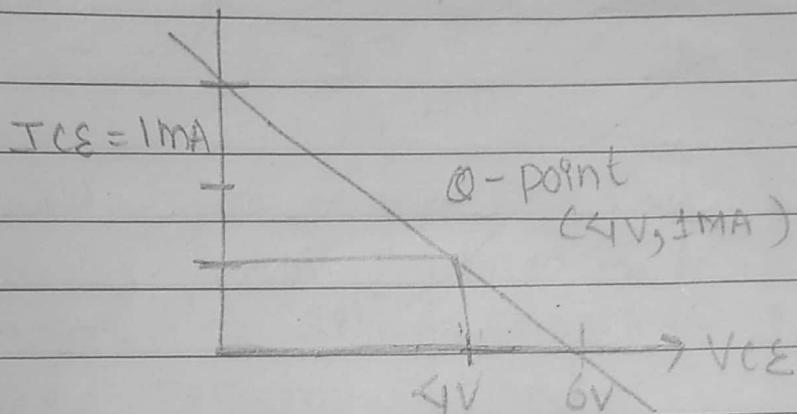
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Maximum Voltage, V_{CE} max :-

For this, $I_C = 0$

$$\therefore V_{CE} \text{ max} = V_{CC} = 6V$$



$V_{CE} < V_{CE} \text{ max}$.

b) operating point calculation:

* Applying KVL at i/p circuit.

$$V_{CC} = I_B R_B = V_{BE} = 0$$

But,

$V_{BE} = 0.7V$ for silicon transistor

$$\therefore I_B = \frac{V_{CC} - V_{BC}}{R_B}$$

$$= \frac{(6 - 0.7)V}{530k\Omega}$$

$$I_B = 10 \text{ nA}$$

$$I_C = \beta I_B$$

$$= 100 \times 10 \text{ nA}$$

$$I_C = 1 \text{ mA}$$

Applying KVL at o/p circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 6 - (1 \text{ mA} \times 2 \text{ k}\Omega)$$

$$= 6 - 2$$

$$= 4 \text{ V}$$

Operating point is (4V, 1mA)

~~②~~ Voltage divide (or potential divider bias method)

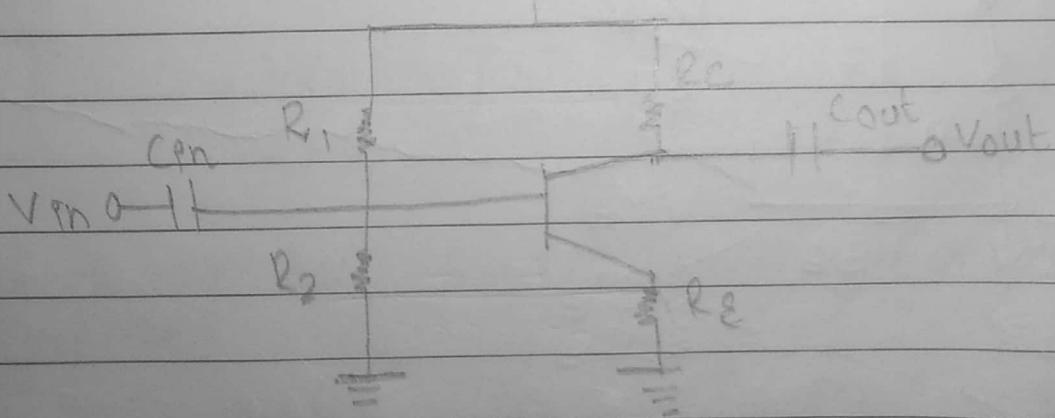
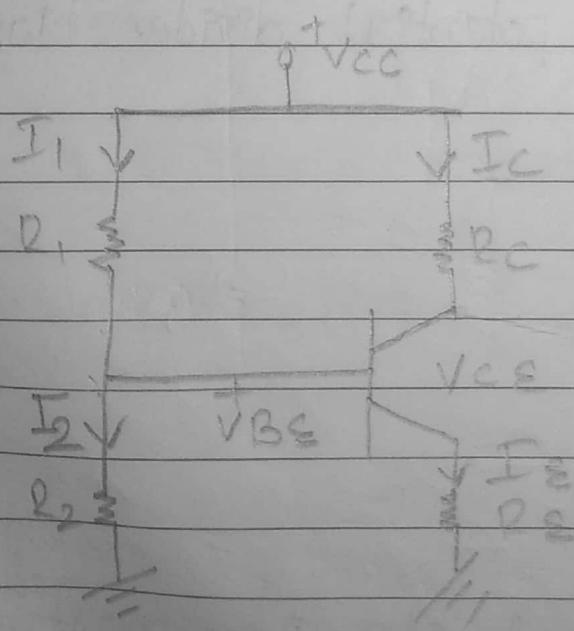


fig :- Voltage divider Bias circuit.

→ This biasing method is widely used and also called universal bias method.

- ↳ Transistor B is highly temperature dependent but this method is almost B independent hence widely used.
- ↳ Here, resistors R_1 & R_2 forms voltage divider circuit Resistor R_2 improves Stability.
- ↳ The voltage drop across R_2 (V_{R2}) forward biases the base-emitter junction.

This causes base current (I_B) and hence collector current (I_C) to flow during zero signal conditions.



$\delta\alpha$ analysis circuit.

Suppose current flowing through R_1 & I_1 . Since base current is very small, we can assume $I_1 \approx I_2$. In such condition, R_1 & R_2 forms Voltage divider network.

(1) Collector current I_c :-

We know;

$$V_{CC} - I_1 R_1 - I_2 R_2 = 0$$

$$\therefore I_1 = I_2$$

$$V_{CC} - I_1 R_1 - I_2 R_2 = 0$$

$$I_1 (R_1 + R_2) = V_{CC}$$

$$\therefore I_1 = I_2 = \frac{V_{CC}}{R_1 + R_2}$$

Now, voltage drop across R_2 is

$$V_{R_2} = I_2 R_2 = V_{CC} \frac{R_2}{R_1 + R_2} \quad \text{--- (1)}$$

Applying KVL to q/p circuit (or base-emitter circuit)

$$V_{R_2} - V_{BE} - I_S R_E = 0$$

$$\text{But, } I_S \approx I_C$$

$$\therefore V_{R_2} - V_{BE} = I_C R_E$$

$$\therefore I_C = \frac{V_{R_2} - V_{BE}}{R_E} \quad \text{--- (2)}$$

Since in eqn (2) I_c does not depend on β , this biasing method is called β independent method.

(ii) Collector-to-emitter voltage (V_{CE}):-

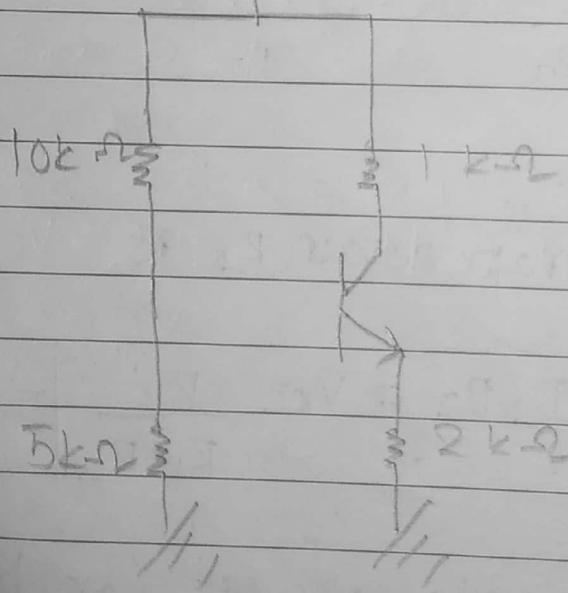
Applying KVL at collector circuit (or OIP circuit)

$$V_{CC} - I_c R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - V_{CE} - I_c R_C - I_c R_E = 0 \quad (\because I_E \approx I_c)$$

$$V_{CE} = V_{CC} - I_c (R_C + R_E) \quad \boxed{3}$$

$$+ V_{CC} = 15V$$



Draw the DC load line and determine the operating point of above circuit for the silicon transistor

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Voltage divider capacitor

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Soln

(a) Load line :-

$$V_{CG} = V_{CC} - I_C (R_C + R_S) \quad \text{---(1)}$$

(b) V_{CG} max :-

For this

$$I_C = 0, \text{ then } V_{CG \text{ max}} = V_{CC} = 15V$$

(c) I_C max

for the $V_{CG} = 0$ then,

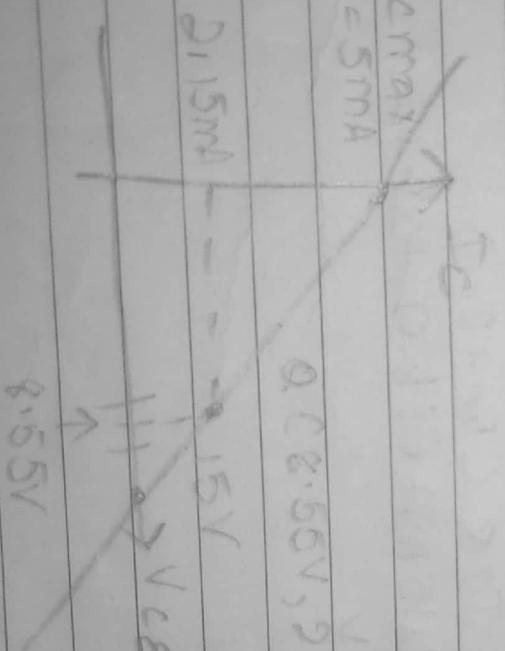
$$I_C \text{ max} = \frac{V_{CC}}{R_C + R_S}$$

$$= \frac{15V}{(1+2) k\Omega}$$

- 5mA

~~$I_{C \text{ max}}$~~
 $= 5 \text{ mA}$

~~$(Q, 8.56V, 2.15 \text{ mA})$~~



(b) operating point :-

$$(i) I_C = \frac{V_{R2} - V_{BE}}{R_E}$$

where,

$$\begin{aligned} V_{R2} &= V_{CC} \frac{R_2}{R_1 + R_2} \\ &= \frac{15 \times 5}{10 + 5} \\ &= 5V \end{aligned}$$

$$\therefore I_C = \frac{(5 - 0.7)V}{2k\Omega}$$

$$= 2.15mA$$

$$\therefore I_{CQ} = 2.15mA$$

(iv) ~~V_{CQ}~~ 8.55V

$$(vi) V_{CE} = V_{CC} - I_{CQ}(R_C + R_E)$$

$$= 15V - 2.15mA(1k\Omega + 2k\Omega)$$

$$= 8.55V$$

Chapter - 9: The operational Amplifier (Op-amp)

Definition of operational amplifier (Op-amp) :-

IMP

→ An operational amplifier (Op-amp) is a direct coupled, negative feedback, very high gain voltage amplifier used to amplify both dc as well as ac signals.

→ It is called operational amplifier (Op-amp) because primarily it is used in mathematical operations such as addition, subtraction, differentiation and integration.

→ Nowdays, op-amps are also used in ADC (Analog-to-digital converter), DAC (Digital-to-Analog converter), voltage-to-frequency converter, frequency-to-voltage converter, oscillators etc.

* Symbol of op-amp:-

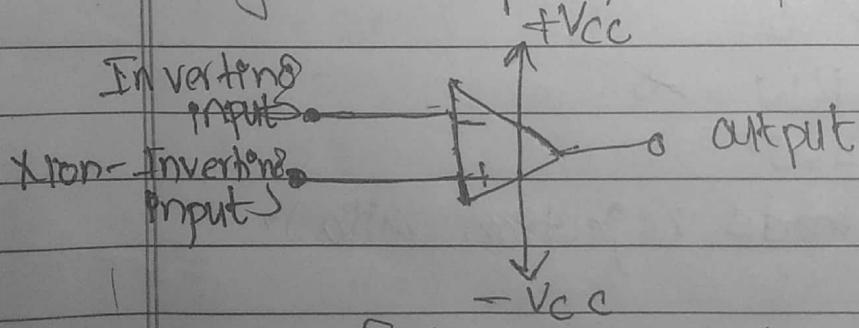
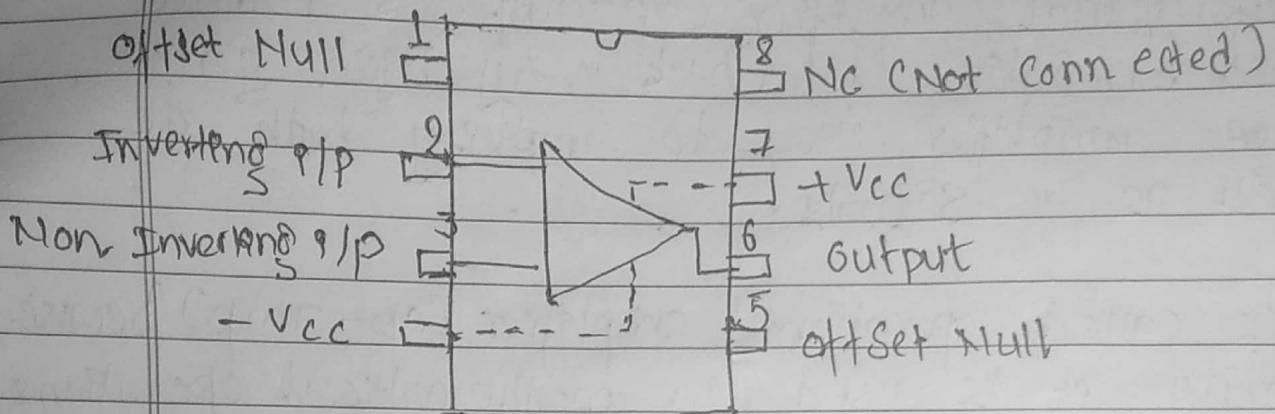


Fig :- Symbol

I_C op-amp (LM A741 op-amp)

↳ Available in 8-pin DIP (Dual Inline Pins)



Ideal Operational Amplifier and Its characteristics

Ideal characteristics :-

- ① The open loop gain is infinite, $A_o = \infty$.
- ② Input impedance or input resistance is infinite, $Z_{in} = \infty$ (or $R_{in} = \infty$)
- ③ Output impedance or output resistance is zero, $Z_{out} = 0$ (or $R_{out} = 0$)
- ④ Infinite bandwidth, $BW = \infty$.
- ⑤ Infinite CMRR, $f = \infty$ (CMRR \rightarrow common mode rejection ratio).
- ⑥ Zero offset voltage.
(P.S. If input voltage is zero, O/P voltage is also zero.)
- ⑦ Op-amp draws no current.

Equivalent circuit of an op-amp :-

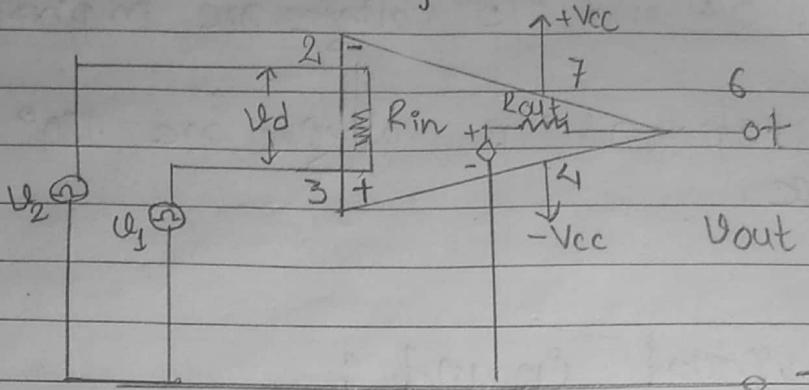


Fig:- equivalent circuit of an practical op-amp

→ The o/p voltage \$V_o\$ is directly proportional to a small difference i/p voltage \$V_d\$

$$V_d = V_1 - V_2$$

Then we can write

$$V_o \propto V_d$$

$$\text{or, } V_o = A_o V_d \quad \text{--- (1)}$$

$$\text{or, } V_o = A_o (V_1 - V_2) \quad \text{--- (2)}$$

where, \$A_o\$ = open loop gain

$$\begin{aligned} V_d &= \text{small signal differential i/p voltage} \\ &= V_1 - V_2 \end{aligned}$$

\$V_1\$ = small signal voltage at non-inverting terminal w.r.t ground.

\$V_2\$ = small signal voltage at inverting terminal w.r.t ground.

\$R_{in}\$ = i/p resistance.

\$R_{out}\$ = o/p resistance.

$$\left. \begin{cases} R_{in}(Z_{in}) = \infty \\ R_{out}(Z_{out}) = 0 \end{cases} \right\}$$

Note :-

- * If $V_1 > V_2$, O/P and I/p voltages are in phase
- + If $V_2 > V_1$, o/p and i/p voltages are 180° out of phase.

Concept of virtual ground :

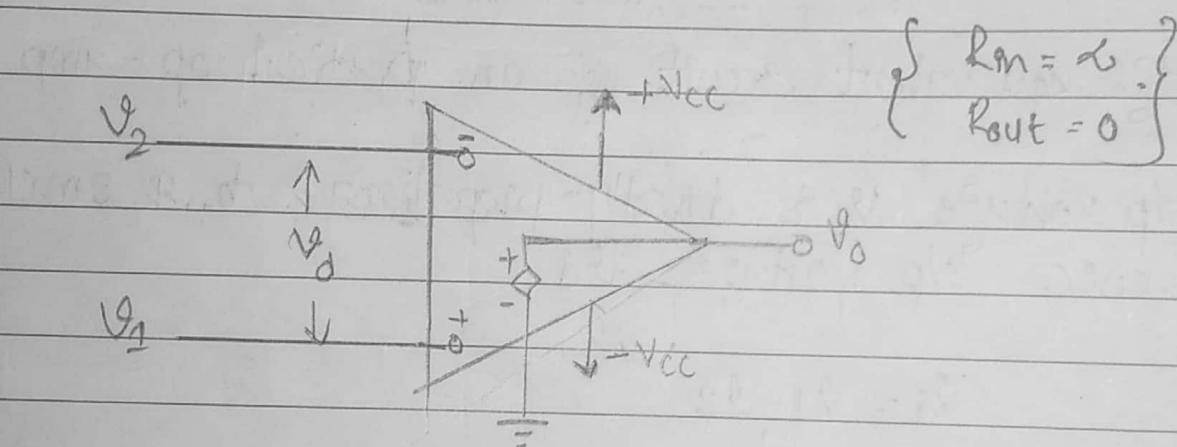


Fig:- Equivalent circuit of an ideal op-amp.

$$V_o = A_o V_d$$

$$V_d = \frac{V_2}{A_o}$$

$$V_d = \frac{V_2}{\infty} \quad [\because A_o = \infty \text{ for ideal case}]$$

$$V_d = 0$$

$$\text{But } V_d = V_1 - V_2 = 0$$

$$\therefore V_1 = V_2 - ①$$

→ ∵ $V_d = 0$, there exists a virtual short circuit between two o/p terminals and virtually no current flows from this short. This is called virtual ground because practically both o/p's V_1 and V_2 can not be same magnitude.

$$\left. \begin{aligned} i_{1n} - i_1 R_{in} - V_A &= 0 \\ i_1 R_{in} - V_{in} - V_A &= 0 \\ \therefore i_1 &= \frac{V_{in} - V_A}{R_{in}} \end{aligned} \right\}$$

Inverting op-amp :-

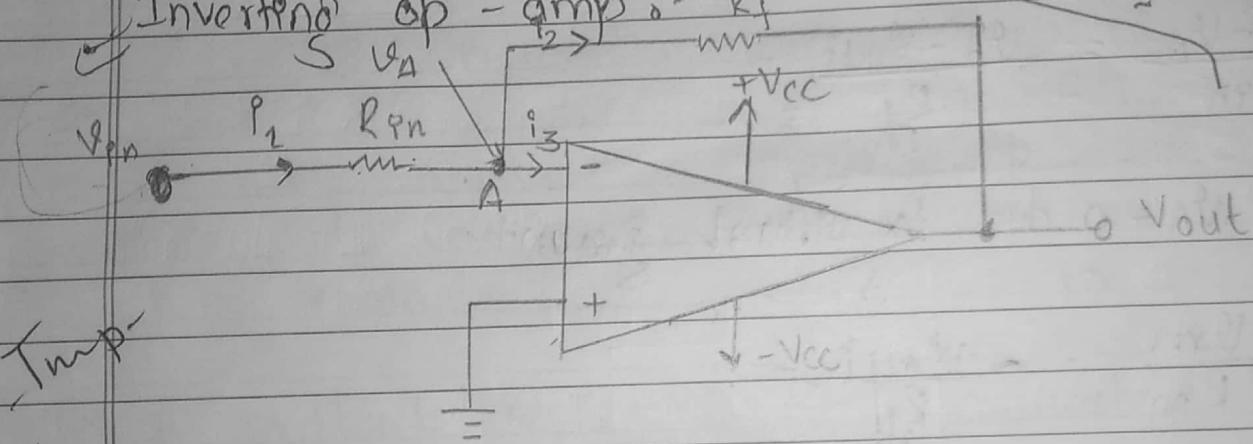


Fig :- Inverting op-amp circuit.

→ Fig above shows an inverting op-amp circuit. Here, o/p voltage is given to the inverting o/p terminal through resistor R_f .

→ A feedback resistor R_f is connected between o/p and inverting o/p terminal.

↳ This configuration is called inverting op-amp because there is 180° phase shift between o/p and o/p voltages.

Circuit Analysis :-

→ Applying K.C.L at node A.

$$i_1 = i_2 + i_3$$

But $i_3 = 0$ because op-amp draws no current.

$$\therefore i_1 = i_2$$

$$\frac{V_{in} - V_A}{R_{in}} = \frac{V_A - V_{out}}{R_f}$$

But $V_A = 0$ due to virtual ground.

$$\therefore \frac{V_{in}}{R_{in}} = -\frac{V_{out}}{R_f}$$

$$A_F = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}} \quad (1)$$

eqn 1 is the gain with feedback or close loop gain.
 The minus sign (-) indicated that there is 180° phase shift between input and output voltage.

(6 b)



Non-inverting op-amp :-

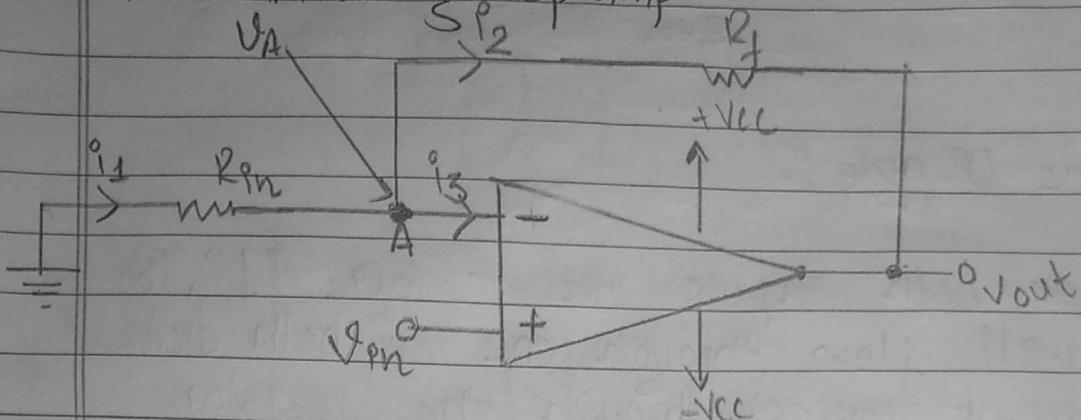


fig :- non-Inverting op-amp circuit.

→ fig above shows non-inverting op-amp circuit.
Here, o/p voltage is given to the non-inverting o/p terminal.

→ A feedback resistor R_F is connected between o/p and in o/p voltage

* Circuit analysis :-

↳ Applying KCL at node A.

$$i_1 = i_2 + i_3$$

But $i_3 = 0$ because op-amp draws no current.

$$\therefore i_1 = i_2$$

$$\frac{V_A - V_{in}}{R_{in}} = \frac{V_A - V_{out}}{R_F}$$

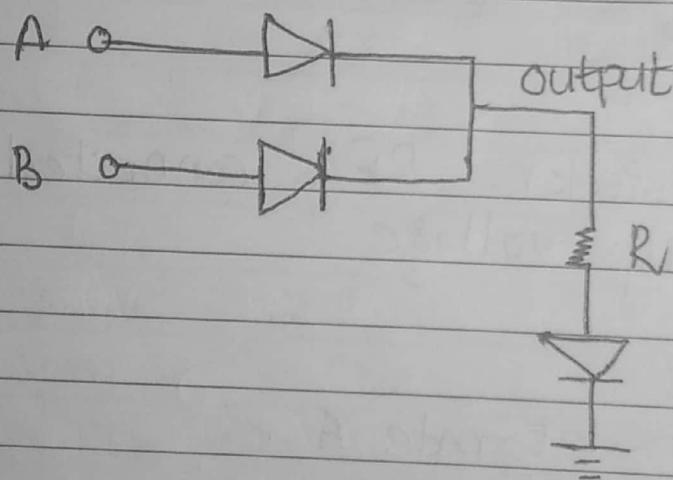
$$\text{or, } \frac{V_{out}}{R_F} = V_{in} \left(\frac{1}{R_F} + \frac{1}{R_{in}} \right)$$

$$\therefore \text{AF or (Acl)} : \frac{V_{out}}{V_{in}} = R_F \left(\frac{1}{R_F} + \frac{1}{R_{in}} \right)$$

$$\therefore A.F \text{ (or Acc)} = \frac{1 + R_F}{R_{in}} - ①$$

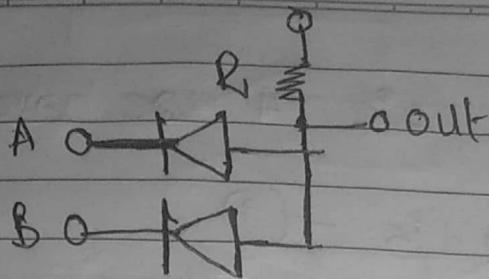
Diode as OR gate :-

→ If one or both inputs are at logic "1", the current will flow through one or both diodes. This current passes through the resistor and causes the appearance of a voltage across its terminals, thereby obtaining logic '1' on the output.



→ Diode as AND gate:-

↳ When both inputs are at logic "1", the two diodes are reverse biased and there is no current flowing to ground. Therefore the output is logic "1" because there is no voltage drop across the resistor R.



IMP

→ Summer (or Adder):

→ Summing amplifiers are mostly used in analog computers.

→ A summer (or adder) amplifier is a circuit whose output voltage is proportional to or equal to the algebraic sum of applied input voltages.

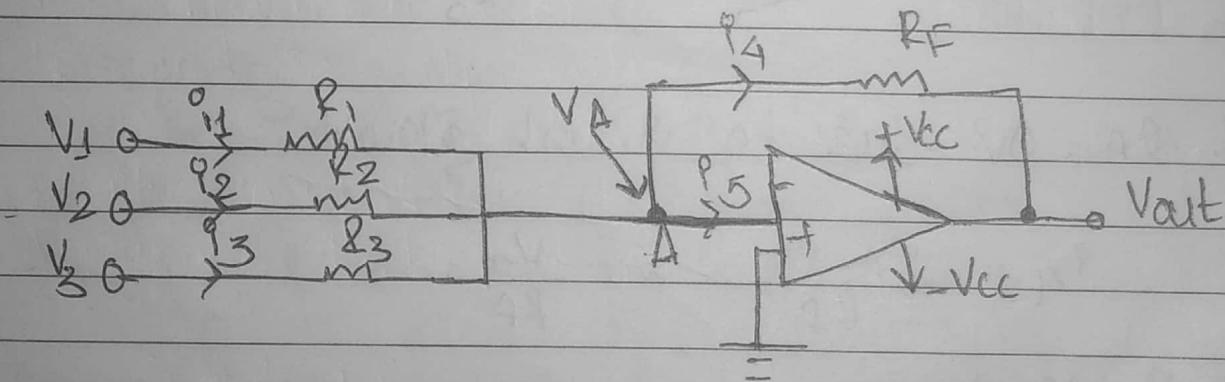


Fig :- op-amp summer (or adder circuit)

→ In the above circuit, V_1, V_2, V_3 are the i/p voltages applied and V_{out} is the o/p voltage.

Circuit analysis :-

Applying KCL at node 'A', we have

$$i_1 + i_2 + i_3 = i_4 + i_5 \quad \text{--- (1)}$$

But $i_5 = 0$ because op-amp does not draw current.

$$\therefore i_1 + i_2 + i_3 = i_4$$

where

$$i_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1}$$

$$i_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2}$$

$$i_3 = \frac{V_3 - V_A}{R_3} = \frac{V_3}{R_3}$$

$\therefore V_A = 0V$ due to virtual ground

and $i_4 = \frac{V_A - V_o}{R_f} = -\frac{V_o}{R_f}$

\therefore Eqn (1) becomes

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{V_o}{R_f} \quad \text{--- (2)}$$

$$\therefore V_o = \left(-\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right) \quad \text{--- (2)}$$

Q. If $V_o = -2V_1 + 3V_2 + 5V_3$

Design adder circuit.

classmate

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ie.

$$V_o \propto -(V_1 + V_2 + V_3) - \textcircled{3}$$

Case

* If $R_1 = R_2 = R_3 = R_f$, then

$$V_o = -(V_1 + V_2 + V_3) - \textcircled{4}$$

Q If $V_o = -2V_1 + 3V_2 + 5V_3$, Design adder circuit.

Soln:

$$V_o = -2V_1 + 3V_2 + 5V_3$$

$$= -(2V_1 - 3V_2 - 5V_3) - \textcircled{1} \quad \begin{array}{l} \text{Voltage may be} \\ + \text{ or } - \text{ but } \\ R_S \text{ not } (-) \end{array}$$

Comparing with

$$V_o = -\left(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3\right) - \textcircled{2}$$

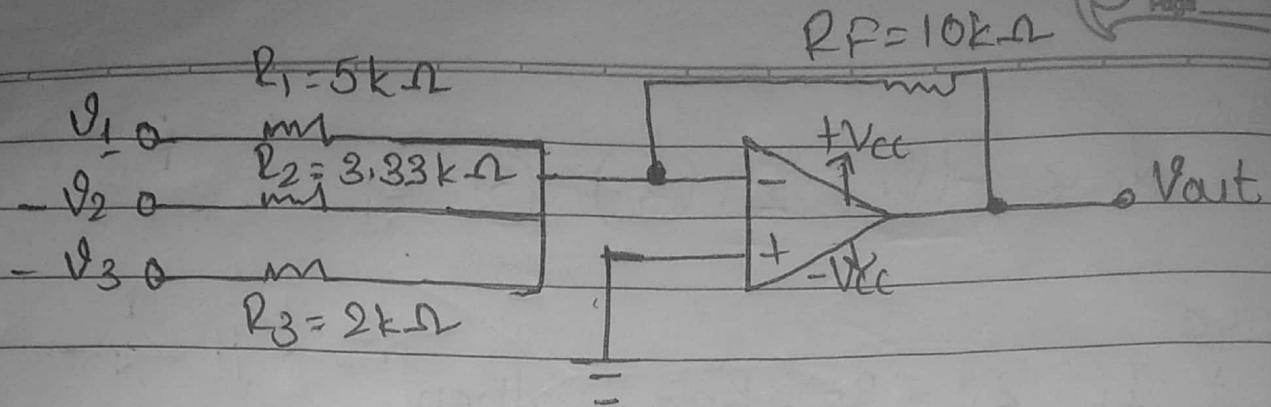
$$\frac{R_F}{R_1} = 2, \quad \frac{R_F}{R_2} = 3, \quad \frac{R_F}{R_3} = 5$$

Assume $R_F = 10k\Omega$ [always put $R_F = 10k\Omega$]

$$R_1 = 5k\Omega$$

$$R_2 = 3.33k\Omega$$

$$R_3 = 2k\Omega$$



Integration and Differentiating Amplifiers:-

① op-amp as Integrator.

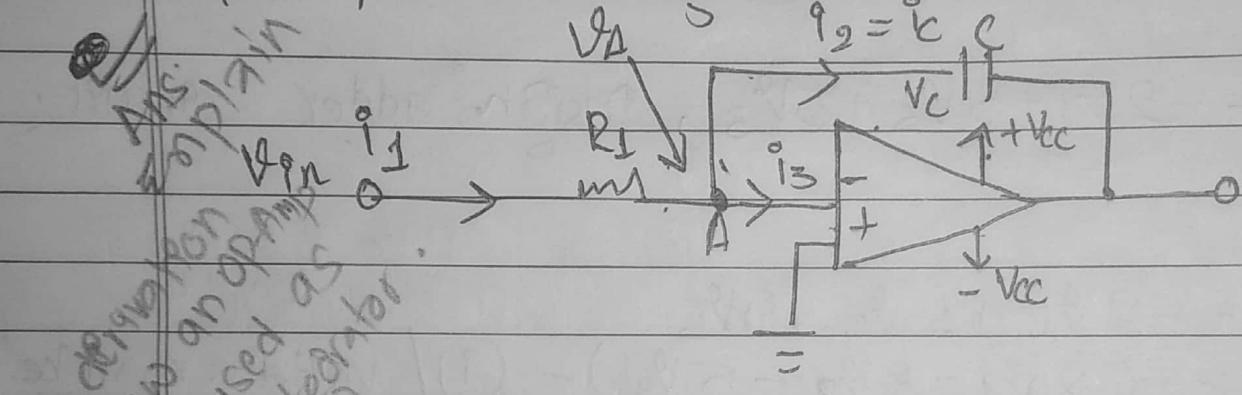


Fig = Op-amp as Integrator.

→ Op-amp Integrator is an electronic circuit which produces the o/p voltage (V_{out}) which is proportional to the integral of the i/p voltage (V_{in}).

→ In Fig, V_{in} = i/p voltage
 V_{out} = o/p "

V_C = Voltage across capacitor.

Circuit analysis :-

↪ Applying KCL at node 'A'

$$i_1 = i_2 + i_3 - (1)$$

$$\text{But } i_3 = 0$$

$$\therefore i_1 = i_2 - (1)$$

$$\text{But } i_2 = i_C \text{ then}$$

$$i_1 = \frac{V_{in} - V_A}{R_1} = V_{in} \quad [\because V_A = 0]$$

$$q = CV$$

$$i_C = \frac{dq}{dt}$$

$$= C \cdot \frac{dV_C}{dt}$$

$$= C \cdot \frac{d(V_A - V_{out})}{dt}$$

$$= C \cdot \frac{dV_{out}}{dt}$$

$$\Rightarrow i_2 = i_C = C \cdot \frac{dV_C}{dt} = C \cdot \frac{d(V_A - V_{out})}{dt}$$

$$= -C \cdot \frac{dV_{out}}{dt}$$

$$\therefore \frac{V_{in}}{R_1} = -C \cdot \frac{dV_{out}}{dt}$$

$$\therefore dV_{out} = -\frac{1}{R_1 C} \cdot V_{in} dt$$

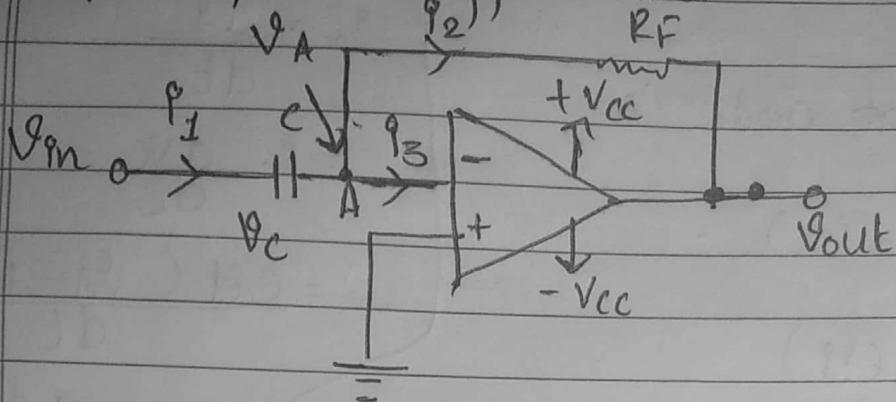
$$\left[\therefore V_{out} = -\frac{1}{R_1 C} \int V_{in} dt \right] \quad (i)$$

~~Vout \propto $\int V_{in} dt$~~

Now inversion ampli us -

Subtractional
amplifier
discrbe.

② Op-amp as Differentiator



$$. V_{in} - V_c - V_A = 0$$

$$V_{in} = V_c$$

fig :- Op-amp as differentiates.

↳ op-amp differentiator is an electronic circuit which produces the o/p voltage (V_{out}) which is proportional to the differentiation of the i/p voltage (V_{in})

⇒ In fig, V_{in} = i/p voltage.

V_{out} = o/p "

V_c = voltage across capacitor

Circuit analysis:-

Applying KCL at node 'A'

$$i_1 = i_2 + i_3 - (i)$$

But $i_3 = 0$

$$\therefore i_1 = i_c - (i)$$

$$i_1 = \frac{CdV_c}{dt}$$

$$i_1 = C \frac{d v_{in}}{dt}$$

$$i_2 = \frac{v_A - v_{out}}{R_f} = -\frac{v_{out}}{R_f} \quad [\because v_A = 0]$$

$$\therefore C \frac{d v_{in}}{dt} = -\frac{v_{out}}{R_f}$$

$$\left[\therefore v_{out} = R_f C \frac{d v_{in}}{dt} \right]$$

$$\text{or, } v_{out} \propto \frac{d v_{in}}{dt}$$

- ① In the op-amp integrator circuit, if the input voltage is sinusoidal (e.g., $v_{in} = V_m \sin \omega t$), obtain the expression for o/p voltage.

Solution:

(IF ask of 5 marks do from this, else do from differentiation)

$$V_o = -\frac{1}{R_f C} \int v_{in} dt - ①$$

$$\therefore v_{in} = V_m \sin \omega t \text{ then}$$

$$V_o = -\frac{1}{R_f C} \int V_m \sin \omega t dt$$

$$= -\frac{V_m}{R_f C} \left| \frac{-\cos \omega t}{\omega} \right|$$

$$= \frac{V_m}{R_i C W} \cos \omega t$$