



```

# run 100000ns
Time = 5000 | 0 0:00:00
Time = 15000 | 0 0:00:00
Time = 25000 | 0 0:00:01
Time = 35000 | 0 0:00:02
Time = 45000 | 0 0:00:03
Time = 55000 | 0 0:00:04
Time = 65000 | 0 0:00:05
Time = 75000 | 0 0:00:06
Time = 85000 | 0 0:00:07
Time = 95000 | 0 0:00:08
Time = 105000 | 0 0:00:09
Time = 115000 | 0 0:00:10
Time = 125000 | 0 0:00:11
Time = 135000 | 0 0:00:12
Time = 145000 | 0 0:00:13
Time = 155000 | 0 0:00:14
Time = 165000 | 0 0:00:15
Time = 175000 | 0 0:00:16
Time = 185000 | 0 0:00:17
Time = 195000 | 0 0:00:18
Time = 205000 | 0 0:00:19
Time = 215000 | 0 0:00:20
Time = 225000 | 0 0:00:21
Time = 235000 | 0 0:00:22
Time = 245000 | 0 0:00:23
Time = 255000 | 0 0:00:24
Time = 265000 | 0 0:00:25
Time = 275000 | 0 0:00:26
Time = 285000 | 0 0:00:27
Time = 295000 | 0 0:00:28
Time = 305000 | 0 0:00:29
Time = 315000 | 0 0:00:30
Time = 325000 | 0 0:00:31
Time = 335000 | 0 0:00:32

```

.....

Terminal output
For 10000 CLK Cycle
From 00:00:00
To 02:46:40



```
Time = 99685000 | 0 2:46:07
Time = 99695000 | 0 2:46:08
Time = 99705000 | 0 2:46:09
Time = 99715000 | 0 2:46:10
Time = 99725000 | 0 2:46:11
Time = 99735000 | 0 2:46:12
Time = 99745000 | 0 2:46:13
Time = 99755000 | 0 2:46:14
Time = 99765000 | 0 2:46:15
Time = 99775000 | 0 2:46:16
Time = 99785000 | 0 2:46:17
Time = 99795000 | 0 2:46:18
Time = 99805000 | 0 2:46:19
Time = 99815000 | 0 2:46:20
Time = 99825000 | 0 2:46:21
Time = 99835000 | 0 2:46:22
Time = 99845000 | 0 2:46:23
Time = 99855000 | 0 2:46:24
Time = 99865000 | 0 2:46:25
Time = 99875000 | 0 2:46:26
Time = 99885000 | 0 2:46:27
Time = 99895000 | 0 2:46:28
Time = 99905000 | 0 2:46:29
Time = 99915000 | 0 2:46:30
Time = 99925000 | 0 2:46:31
Time = 99935000 | 0 2:46:32
Time = 99945000 | 0 2:46:33
Time = 99955000 | 0 2:46:34
Time = 99965000 | 0 2:46:35
Time = 99975000 | 0 2:46:36
Time = 99985000 | 0 2:46:37
Time = 99995000 | 0 2:46:38
```

```
INFO: [USF-XSim-96] XSim completed. Design snapshot 'Digital_Clock_tb_behav' loaded.
```

```
INFO: [USF-XSim-97] XSim simulation ran for 100000ns
```

Same way the CLK running to end