ITE 聯陽半導體 ITE Tech. Inc.

IT9513/IT9517/IT9518

OFDM transmitter
for AirHD® & cchDTV®

V1.0

ITE Tech. Inc.

Easy HD Expressway

AirHD® cchDTV

This is a Preliminary document release. All specifications are subject to change without notice.
The material contained in this document supersedes all previous material issued for the products herein referenced. Please contact ITE Tech. Inc. for the latest document(s).

All sales are subject to ITE's Standard Terms and Conditions, a copy of which is included in the back of this document.

ITE, IT9510/IT9517/IT9513/IT9511/IT9518AirHD/cchDTV/DTV CAM are trademarks of ITE Tech. Inc.
All other trademarks are claimed by their respective owners.
All specifications are subject to change without notice.

Additional copies of this manual or other ITE literature may be obtained from:

ITE Tech. Inc.
Marketing & Sales Department
9F, No.233-1, Baociao Rd., Sindian City,
Taipei County 23145, Taiwan, ROC

Tel: 886-2-29126889
Fax: 886-2-8914-5970

If you have any marketing or sales questions, please contact our local sales representative nearest you on the ITE web site.

To find out more about ITE, visit our World Wide Web at:
http://www.ite.com.tw

Or e-mail itesupport@ite.com.tw for more product information/services

Revision History

Section	Revision	Page No.
1	• Feature of IT9510 series	
6	• Package 8x8 & Outline dimension	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	
	•	

CONTENTS

1. Features 3
2. General Description 3
3. Block Diagram 4
3.1 Analog Front-end 4
3.1.1 IT9511/IT9513/IT9517 4
3.1.2 IT9518 5
4. Ordering Information 7
5. Pin Diagram 8
6. Pin Description 11
7. Power Domains 14
8. Functional Descprition 15
8.1 Operation Modes 15
8.1.1 TS/I2C Mode 15
8.1.2 TS/USB Mode 15
8.1.3 I2S Mode 16
8.1.4 USB Mode 16
8.2 Analog Interface 16
8.2.1 Clocking 16
8.2.2 Clock Table 16
8.3 Initialization 16
8.4 LO, DAC, Mixer and Filter 16
8.5 DVB-T/ISDB-T COFDM Digital Signal Processing 17
8.5.1 Coding and Interleaving 17
8.5.2 Frequency-Domain Signal Processing 17
8.5.3 Time-Domain Signal Processing 17
8.6 2-Wire Interfaces 17
8.7 Host Interfaces 18
8.7.1 Transport Stream Interface 18
8.8 USB Interface 21
8.8.1 USB Descriptors 21
8.8.2 USB Control Protocol 21
8.9 IR Interface 22
8.9.1 The Function Keys and Alternative Keys 22
8.9.2 The External EEPROM 22
8.9.3 Boot Scheme (Provide EEPROM boot) 22
8.10 I2S Audio Interface Basic Operation: 22
8.11 GPIO Interface 23
9. Power Modes 25
9.1 Power Modes 25
9.2 Current Consumption 25
10. Register Descriptions 27
11. DC Characteristics 29
11.1 Absolute Maximum Ratings* 29
11.2 Operating Conditions 29
11.3 DC Electrical Characteristics 30
12. AC Characteristics 31
12.1 TS Input 31
12.2 2-Wire Bus Output Timing 31
12.3 2-Wire Bus Input Timing 32
12.4 I2S Bus Input Timing 32
13. Package 33
14. Top Marking Information 35

1. Features

- **Modulator**
  - ETSI, DVB-T/H (EN 300 744 V1.5.1) and ISDB-T (ARIB STD-B31 V1.6) Compliant transmitter for Digital Terrestrial Television
  - Configurable code rate: 1/2,2/3,3/4,5/6,7/8
  - Programmable QPSK, 16-QAM and 64-QAM Symbol Mapping
  - Configurable support for 2k, 4k, and 8k FFT
  - Programmable Guard Interval (1/4, 1/8, 1/16, 1/32)
  - Supports variable channel band width from 1 MHz to 8 MHz
  - RF output or Zero I/F complex base band I/Q output with integrated DAC and anti-aliasing filter
  - MER
    - > 40dB with external LO/Mixer
    - >30 dB with internal LO/Mixer
  - Carrier Suppression > 50dB
  - Spectrum Shoulders: 55 dB for perfect adjacent-channel operations
- On-chip voltage regulator:
  - Enables single supply 2.7V-3.6V operation.
  - May use 1.7V-2.0V supply for lower power.
- Integrated local oscillator and RF mixer with frequency tuning range 50MHz~950MHz.
- External local oscillator and external RF mixer supported
- 12MHz clock output to enable single-crystal system design.
- **MPEG2-TS** input interface
  - Both Serial and parallel supported
  - AES128 encryption
- 3x I^2S input interfaces
  - Support up to 31.6Mbps raw audio data rate which can deliver,
    - 2 ch, 384K, 32bits
    - 4 ch, 192K, 32bits
    - 6 ch, 192K, 24bits
  - Built-in TS encapsulation for transmission
- Integrated transport stream de-multiplexer (**PID filtering**) with bypass mode.
- Support PCR re-stamping for TS stream.
- Programmable SI/PSI table insertion
- **Control interfaces**
  - Embedded **USB 1.1** and **2.0** compatible interface supports with suspend mode.
  - UART
  - 1x IIC master and 1x IIC slave
- Infrared (**IR**) interface provided for remote control.
- Up to 8 independent GPIO pins
- MQFN-64 package, both commercial and **industrial** grades are available.

2. General Description

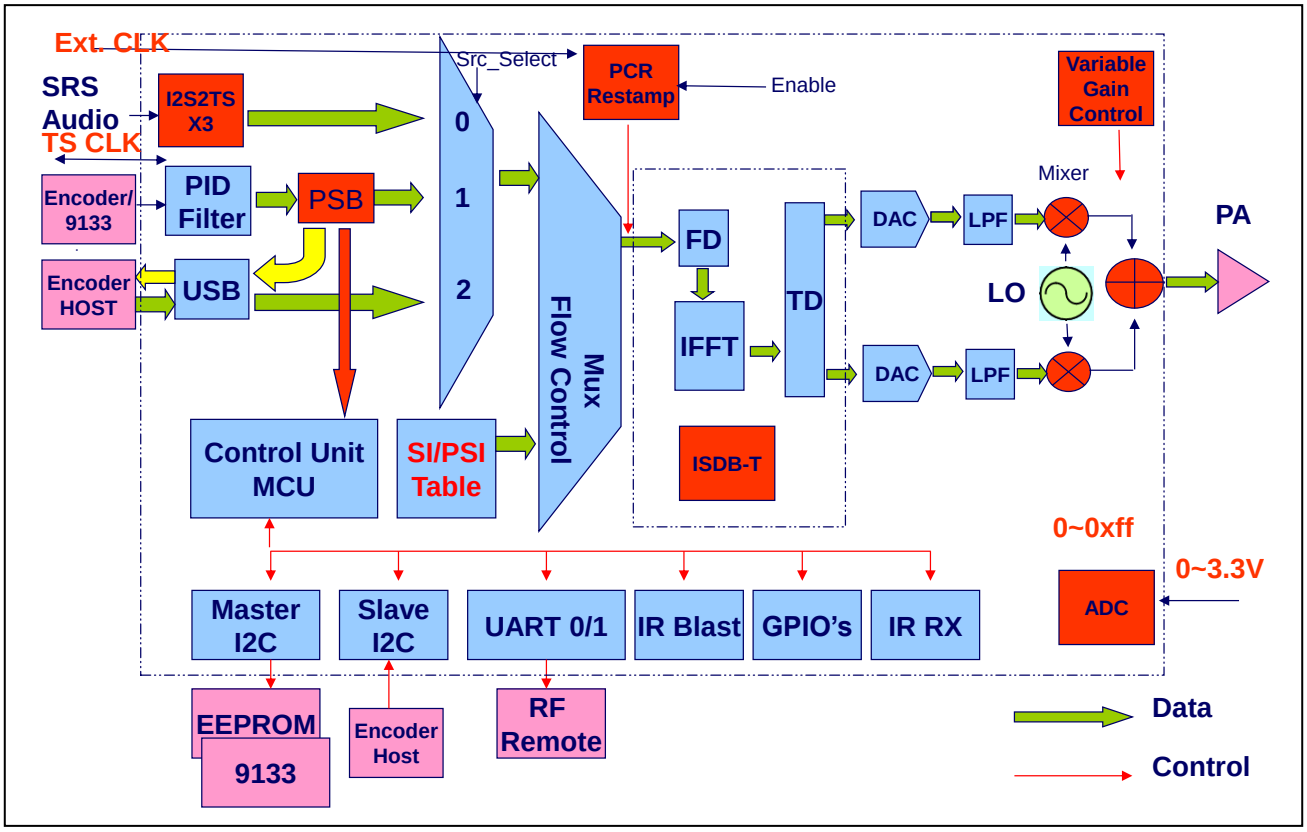
IT9510 is a series of highly integrated transmitter for AirHD, DTVCam, and other personal, community, or professional digital TV head-end applications. The core of IT9510 is a DVB-T and ISDB-TCOFDM modulator. The high level of integration of IT9510 significantly decreases the power consumption, board size and cost of modulators in digital TV transmitter. With IT9510, a low cost, low power, compact, reliable, high bandwidth and wireless (or wired) full HD delivery solution is easily achieved.

IT9510 offers very low total bill of materials (BOM) and high-integration-level system solutions. It includes processing units for forward error correction coding and digital modulation, D/A IQ converter, low-pass filters, embedded mixer, and local oscillator. IT9510 series also supports flexible input interfaces, including embedded USB 2.0 interface, and serial/parallel TS interface input with built-in de-multiplexer.

IT9510 series is compliant to the non-hierarchical transmission specified in DVB-T (ETSI EN 300 744) and ISDB-T (ARIB STD-B31 V1.6). A (204,188) Reed-Solomon encoder capable of correcting 8 error bytes is used to generate parity bytes for each input TS packet. The code rates of the punctured convolution encoder include 1/2, 2/3, 3/4, 5/6, and 7/8. Only native interleaving is used in IT9510. The output signal bandwidth is configurable from 1 MHz to 8 MHz for DVB-T and ISDB-T mode. The supported signal constellations include QPSK, 16-QAM, and 64-QAM. FFT modes of 2k, 4k, and 8k and guard intervals of 1/4, 1/8, 1/16, and 1/32 specified in EN 300 744 and STD-B31 V1.6 are supported. The transmission parameters are register-programmable, and are embedded in the Transmission Parameter Signaling (TPS) information as required by EN 300 744 and STD-B31 V1.6.

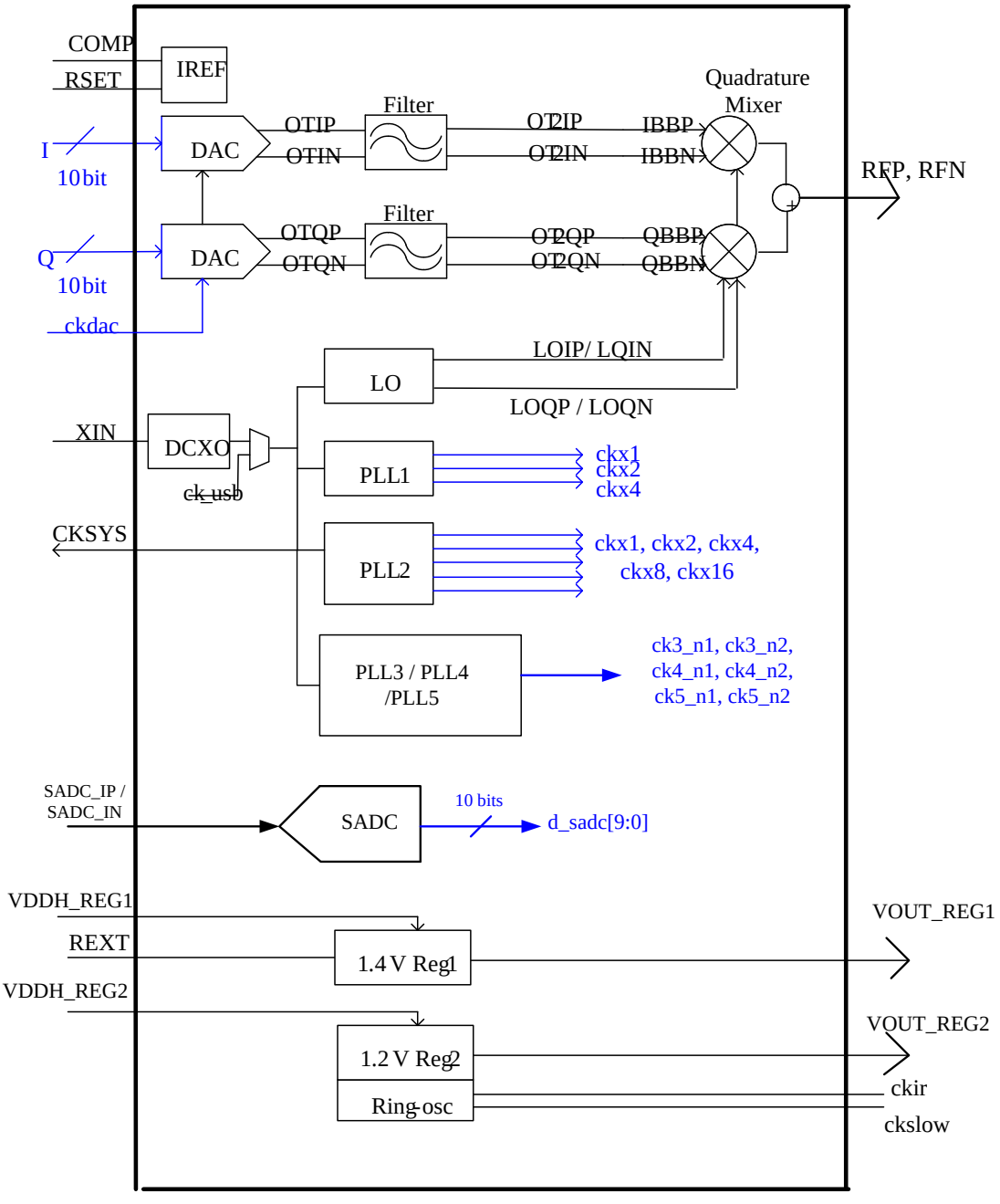
A complete set of application programming interface (API) is available, facilitating fast and easy integration into products on Windows Mobile, Windows CE, Windows 7, Windows XP, Vista, Linux, and many other operating systems. Furthermore, a complete set of USB drivers for Windows 7/XP/Vista, Windows Mobile/CE, and Linux are provided for IT9510.

3. Block Diagram

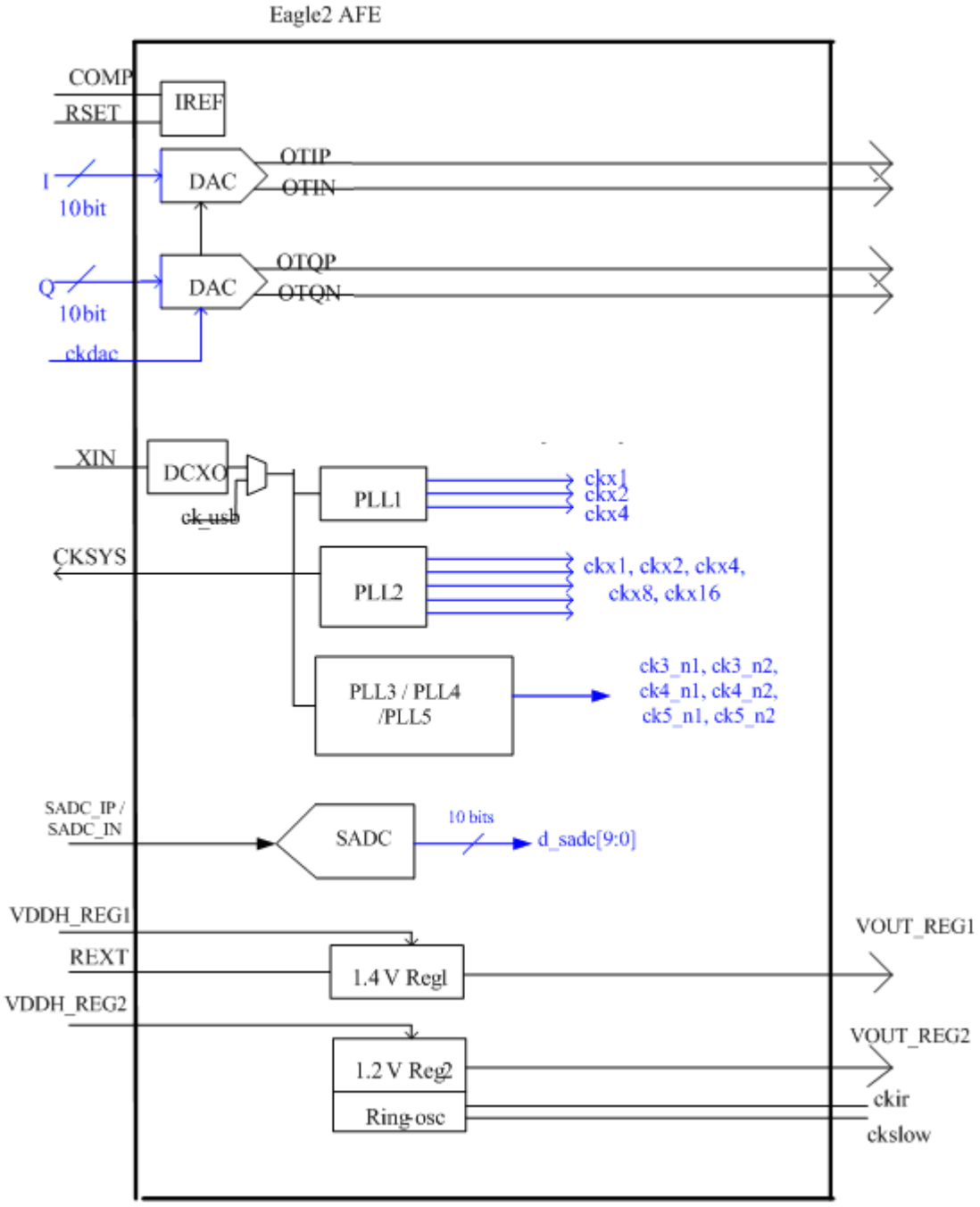


3.1 Analog Front-end

3.1.1 IT9511/IT9513/IT9517


COMP
RSET
IREF
I
10bit
DAC
OTIP
OTIN
Filter
OT2IP
OT2IN
IBBP
IBBN
Quadrature
Mixer
RFP, RFN
Q
10bit
DAC
OTQP
OTQN
Filter
OT2QP
OT2QN
QBBP
QBBN
ckdac
LOIP/ LQIN
LO
LOQP / LOQN
XIN
DCXO
ck_usb
PLL1
ckx1
ckx2
ckx4
CKSYS
PLL2
ckx1, ckx2, ckx4,
ckx8, ckx16
PLL3 / PLL4
/PLL5
ck3_n1, ck3_n2,
ck4_n1, ck4_n2,
ck5_n1, ck5_n2
SADC_IP /
SADC_IN
SADC
10 bits
d_sadc[9:0]
VDDH_REG1
REXT
1.4 V Reg1
VOUT_REG1
VDDH_REG2
1.2 V Reg2
VOUT_REG2
Ring-osc
ckir
ckslow

3.1.2 IT9518


Eagle2 AFE
COMP
RSET
IREF
I
10bit
DAC
OTIP
OTIN
Q
10bit
DAC
OTQP
OTQN
ckdac
XIN
DCXO
ck_usb
PLL1
ckx1
ckx2
ckx4
CKSYS
PLL2
ckx1, ckx2, ckx4,
ckx8, ckx16
PLL3 / PLL4
/PLL5
ck3_n1, ck3_n2,
ck4_n1, ck4_n2,
ck5_n1, ck5_n2
SADC_IP /
SADC_IN
SADC
10 bits
d_sadc[9:0]
VDDH_REG1
REXT
1.4 V Regl
VOUT_REG1
VDDH_REG2
1.2 V Reg2
Ring-osc
VOUT_REG2
ckir
ckslow

4. Ordering Information

Part Number	Description	Modulation	Package	Body Size
IT9517FN/AX	Commercial grade baseband transmitter for digital TV with USB and TS interfaces	16/64QAM, QPSK	64-pin MQFN	8mm × 8mm
IT9517FN-I/AX	Industrial specification of 9517	16/64QAM, QPSK	64-pin MQFN	8mm × 8mm
IT9513FN/AX	Commercial grade baseband transmitter for digital TV with USB and TS interfaces.	16QAM, 64QAM, 2K mode only	64-pin MQFN	8mm × 8mm
IT9513FN-I/AX	Industrial specification of 9513	16QAM, 64QAM, 2K mode only	64-pin MQFN	8mm × 8mm
IT9518FN/AX	Commercial grade baseband transmitter for digital TV with USB and TS (NOTE: without internal LO, mixer and LPF) interfaces	16/64QAM, QPSK	64-pin MQFN	8mm × 8mm

All ICs listed above are RoHS compliant component

5. Pin Diagram

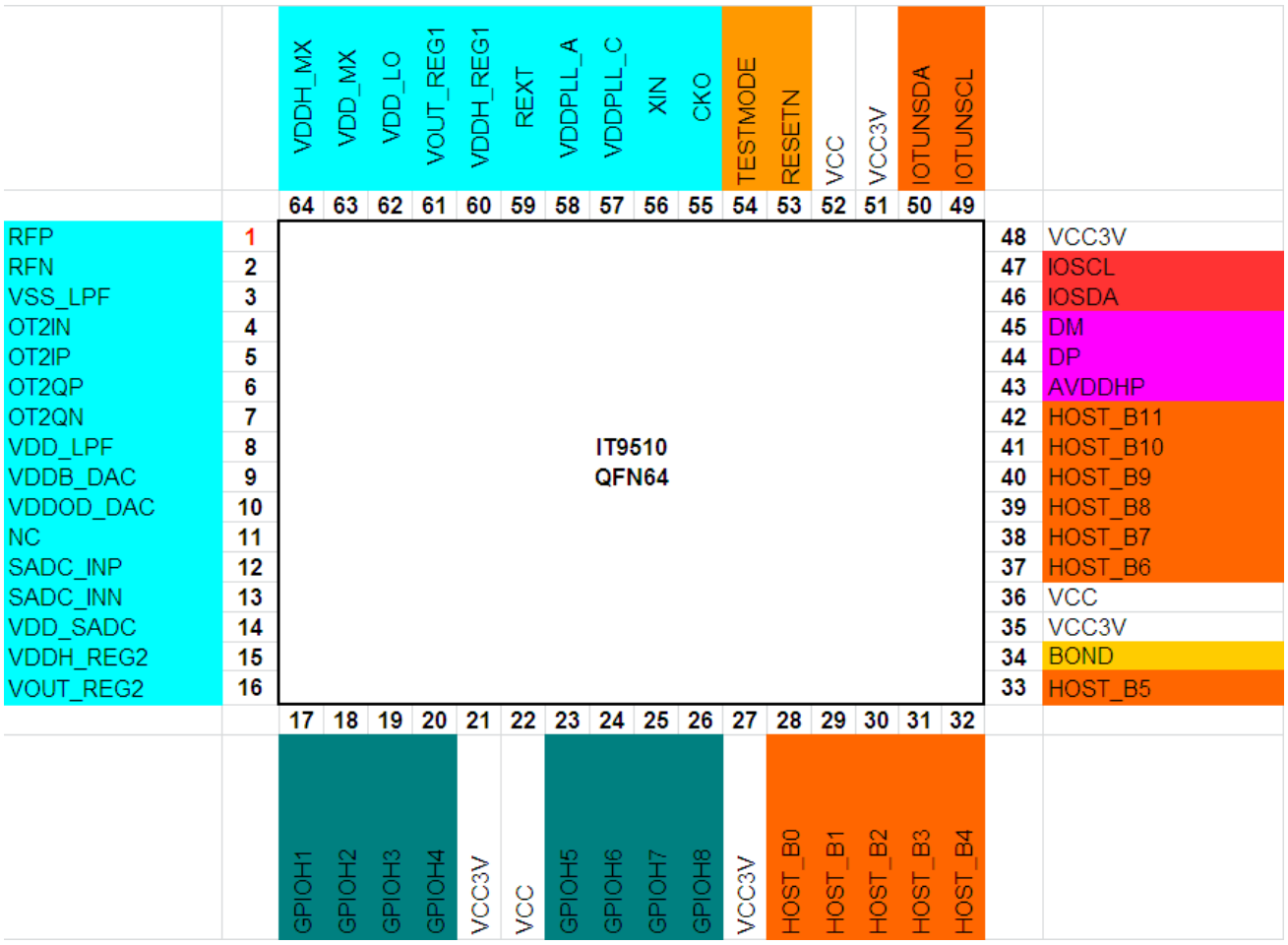


Table 5-1. IT9517/9513/9511/9518 pin listed in numeric order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	RFP (NC)	17	GPIOH1	33	HOST_B5	49	IOTUNSCL
2	RFN (NC)	18	GPIOH2	34	BOND	50	IOTUNSDA
3	VSS_LPF (NC)	19	GPIOH3	35	VCC3V	51	VCC3V
4	OT2IN	20	GPIOH4	36	VCC	52	VCC
5	OT2IP	21	VCC3V	37	HOST_B6	53	RESETN
6	OT2QP	22	VCC	38	HOST_B7	54	TESTMODE
7	OT2QN	23	GPIOH5	39	HOST_B8	55	CKO
8	VDD_LPF	24	GPIOH6	40	HOST_B9	56	XIN
9	VDDB_DAC	25	GPIOH7	41	HOST_B10	57	VDDPLL_C
10	VDDOD_DAC	26	GPIOH8	42	HOST_B11	58	VDDPLL_A
11	NC	27	VCC3V	43	AVDDHP	59	REXT
12	SADC_INP	28	HOST_B0	44	DP	60	VDDH_REG1
13	SADC_INN	29	HOST_B1	45	DM	61	VOUT_REG1
14	VDD_SADC	30	HOST_B2	46	IOSDA	62	VDD_LO
15	VDDH_REG2	31	HOST_B3	47	IOSCL	63	VDD_MX
16	VOUT_REG2	32	HOST_B4	48	VCC3V	64	VDDH_MX

6. Pin Description

Table 6-1. IT9517/9513/9511/9518 Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
8	VDD_LPF	PWR	-	+1.4V Analog Power Supply
9	VDDB_DAC	PWR	-	+1.4V Analog Power Supply
10	VDDOD_DAC	PWR	-	+1.4V Analog Power Supply
14	VDD_SDAC	PWR	-	+1.4V Analog Power Supply
57	VDDPLL_C	PWR	-	+1.4V Analog Power Supply
58	VDDPLL_A	PWR	-	+1.4V Analog Power Supply
62	VDD_LO	PWR	-	+1.4V Analog Power Supply
64	VDDH_MX (NC)	PWR	-	+3.3V Analog Power Supply
15	VDDH_REG2	PWR	-	+3.3V Analog Power Supply
60	VDDH_REG1	PWR	-	+3.3V Analog Power Supply
22,36,52	VCC	PWR	-	+1.2V Power Supply
21,27,35,48 ,51	VCC3V	PWR	-	+3.3V Power Supply
43	AVDDHP	PWR	-	+3.3V Power Supply for USB

Table 6-2. IT9517/9513/9511/9518 Pin Description of Analog I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1	RFP	AIO	-	Mixer out (Except IT9518)
2	RFN	AIO	-	Mixer out (Except IT9518)
12	SADC_INP	AIO	-	Slow ADC
13	SADC_INN	AIO	-	Slow ADC
4	OT2IN	AIO	-	LPF Output
5	OT2IP	AIO	-	LPF Output
6	OT2QP	AIO	-	LPF Output
7	OT2QN	AIO		LPF Output
16	VOUT_REG 2	AO	VCC	Internal LDO output (+1.2V)
44	DP	AIO	-	***Differential Positive signal for USB***
45	DM	AIO	-	***Differential Negative signal for USB***
56	XIN	AI		Xtal in
55	CKO	AO	-	Clock output for another device
59	REXT	AIO	-	External Resistor for DAC
61	VOUT_REG 1	AO	VDD_L O	Internal LDO output (+1.4V)

Table 6-3. IT9517/9513/9511/9518 Pin Description of Digital I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
53	RESETN	DI	VCC3V	***Power-on Reset (Low Active)***
54	TESTMODE	DI	VCC3 V	***Test mode selection; tied to ground for normal operation.***
17	GPIOH1	DIO	VCC3 V	***General purpose I/O***
18	GPIOH2	DIO	VCC3V	***General purpose I/O***
19	GPIOH3	DIO	VCC3V	***General purpose I/O***

Pin(s) No.	Symbol	Attribute	Power	Description
20	GPIOH4	DIO	VCC3V	***General purpose I/O***
23	GPIOH5	DO	VCC3V	***General purpose I/O***
24	GPIOH6	DIO	VCC3V	***General purpose I/O***
25	GPIOH7	DIO	VCC3V	***General purpose I/O***
26	GPIOH8	DIO	VCC3V	***General purpose I/O***
46	IOSDA	DIO	VCC3V	***Two-wire bus serial data line***
47	IOSCL	DO	VCC3V	***Two-wire bus serial clock line***
49	IOTUNSCL	DO	VCC3V	***Two-wire bus serialclock line (master)***
50	IOTUNSDA	DIO	VCC3V	***Two-wire bus serial data line (master)***
28	HOST_B0	DO	VCC3V	***Host interface***
29	HOST_B1	DO	VCC3V	***Host interface/I2S***
30	HOST_B2	DO	VCC3V	***Host interface/I2S***
31	HOST_B3	DO	VCC3V	***Host interface/I2S***
32	HOST_B4	DO	VCC3V	***Host interface/I2S***
33	HOST_B5	DO	VCC3V	***Host interface/I2S***
37	HOST_B6	DO	VCC3V	***Host interface/I2S***
38	HOST_B7	DO	VCC3V	***Host interface***
39	HOST_B8	DO	VCC3V	***Host interface***
40	HOST_B9	DO	VCC3V	***Host interface***
41	HOST_B10	DO	VCC3V	***Host interface***
42	HOST_B11	DO	VCC3V	***Host interface***
34	BOND	DI	VCC3V	***TS/I2S select***

NOTE: (NC) only for IT9518

Table 6-4. Pin description of GPIO and strapping

Name	Strapping	IO Functions	State after RESET
GPIOH1	Clock Select Bit 0	GPIO/ PWM/ Lock Indicator 1	High-Z
GPIOH2	Clock Select Bit 1	GPIO/ PWM/ Lock Indicator 2	High-Z
GPIOH3	Clock Select Bit 2	GPIO/ PWM/ Lock Indicator 3	High-Z
GPIOH4	N/A	GPIO/ PWM/ Lock Indicator 4/ UART-TxD	High-Z
GPIOH5	Mode Select Bit 0/ Two-wire bus address bit 0	GPIO/ Suspend Resume	High-Z
GPIOH6	Mode Select Bit 1 1: for AFE test 0: Two-wire bus	GPIO	High-Z
GPIOH7	Mode Select Bit 2/USB and TS mode switch	GPIO; IR receiving	High-Z
GPIOH8	Mode Select Bit 3	GPIO; UART-RxD	High-Z

Table 6-5. Strapping sampled at the rising edge of the RESET signal

Pin Name	Selection
{ GPIOH3,GPIOH2,GPIOH1}	Crystal frequency: 000 crystal = 12 MHz
{GPIOH8,GPIOH7,GPIOH6,GPIOH5}	Mode strapping and 2-wire bus address selection: (0,0,0,x) TS/I2C mode, { GPIOH5} = 2-wire address bit 1 (0,1,0,x) TS/USB mode (0,1,1,x) USB mode
BOND (pin 34)	(1) I2S mode

Table 6-6. Pin list of Host Interface

Pin \ Mode	TS Input Mode
HOST_B0	MPEG Data[7]
HOST_B1	MPEG Data[6]
HOST_B2	MPEG Data[5]
HOST_B3	MPEG Data[4]
HOST_B4	MPEG Data[3]
HOST_ B5	MPEG Data[2]
HOST_B6	MPEG Data[1]
HOST_B7	MPEG Data[0]
HOST_B8	MPEG Clock
HOST_B9	MPEG Valid
HOST_B10	MPEG Sync
HOST_B11	MPEG Fail

Notes: 1) These pins have no integrated pull up/down.
2) The state of these pins immediately after reset is high-Z.
3) The pads of these pins are of the CMOS type.
4) These pins are on I/O power domain

NOTE: Fail pin should be low if not used in some abnormal application.

7. Power Domains

IT9510 has four power domains: RF, Core, IO, and USB respectively.

The RF Domain is supplied by 3.3V±10% to provide power for analog functions. The external 3.3V should be connected to pin VDDH_MX, VDDH_REG1 and VDDH_REG2. The other analog power supply pins (1.4V) shall be connected to the pin VOUT_REG1 to be powered by the built-in voltage regulator.

The Core Domain is supplied by 1.2V±10% to provide power for the core circuits of IT9510. It can be provided by external 1.2V or using the internal voltage regulator from the pin VOUT_REG2.

The IO Domain provides power for the host interface, including the TS/I2S interface, 2-wire bus, UART and GPIOH1~GPIOH8. The supply voltage for IO Domain is 3.3V±10%.

The USB Power Domain is supplied by 3.3v±10% to power the USB interface under USB mode. Otherwise, the pin AVDDHP should be connected to ground.

8. Functional Descprition

8.1 Operation Modes

IT9510 supports four different operation modes, TS/I2C, TS/USB, I2S and USB depending on the data path and control path. The mode is determined by appropriately setting the strapping pins as specified in Table 6- and register programming after strapping.

The supported operation modes of IT9510 are summarized in Table 8-1 and the control and data paths in each operation mode are summarized in Table 8-2.

Table 8-1. Operation modes of IT9510

Mode / Part #	TS/I2C	TS/USB	USB	I2S
IT9517/IT9518	Yes	Yes	Yes	Yes
IT9513	Yes	Yes	Yes	Yes
IT9511	Yes	Yes	Yes	Yes

Table 8-2. Data path and contol paths at each output mode

Path / Mode	Data Path	Control Path
TS/I2C	TS	2-wire bus
TS/USB	TS	USB
USB	USB	USB
I2S	I2S	2-wire/USB

8.1.1 TS/I2C Mode

In the TS/I2C mode, the transport stream to be transmitted comes through either the parallel or serial TS input interface. IT9510 is controlled by an external host controller (CPU) via the 2-wire (I2C) bus as an I2C slave device. More details of the TS interface are given in Section 8.7.1.

8.1.2 TS/USB Mode

In the TS/USB mode, the transport stream to be transmitted comes through either the parallel or serial TS input interface. IT9510 is controlled by an external host controller (CPU) via the USB bus as a USB device. More details of the TS interface are given in Section 8.7.1.

8.1.3 I2S Mode

In the I2S mode, the transport stream interface is disabled and raw audio data is fed from the I2S interfaces. IT9510 is controlled by an external host controller (CPU) via 2-wire (I2C) bus as an I2C slave device or USB bus as a USB device. More details of the USB interface are given in Section 8.10

8.1.4 USB Mode

In the USB mode, IT9510 communicates with the host through the embedded USB 2.0 interface. The transport stream to be transmitted by IT9510 and control/status signals are all encapsulated in the USB frames. Besides, the host can access (read) the TS input thru USB EP5. More details of the USB interface are given in Section 8.8

8.2 Analog Interface

8.2.1 Clocking

IT9510 has on-chip crystal amplifiers for clock generation. Only single 12MHz crystal is required to generate all internal clocks.

IT9510 also provides a buffered clock output (CKO) which, for example, can be used to drive a second IT series receiver IC in TS/USB applications.

The IT9510 clocking circuit requires a stable reference clock. It can be provided by either of the following two methods:

1. Connect a crystal across the oscillator pin XTAL and ground, or
2. Connect an external clock source to the pin XTAL.

With programmable PLL, the supported reference clock frequency is 12MHz. This clock source can come from the crystal, other external clock source, or the buffered clock output (CKO) of another ITE receiver IC (in AirHD applications).

8.2.2 Clock Table

The programmable PLL default clock ratio is decided by pin strapping which is described in Table 6-. After the initial operation, it can also be re-programmed through register access. More details on programming the PLL ratio for different clock frequency selection can be found in *IT9510 Programming Guide*.

8.3 Initialization

Several important system parameters need to be programmed correctly in order to insure proper operations of IT9510. These include, among other things, the carrier frequency of the RF signal and DAC sampling frequency. More details on initializing IT9510 can be found in *IT9510 Programming Guide*.

8.4 LO, DAC, Mixer and Filter

The analog front end consists of a local oscillator (LO), a 10-bit high-speed IQ DAC, a low-pass filter (LPF), and a mixer.
The LO provides wide-range (covering VHF and UHF bands) differential clock outputs for data up-conversion.
The 10-bit IQ DAC converts the digital modulator output into analog baseband signal with an embedded clock source.

The LPF, located after the DAC, is an anti-aliasing filter for removing unwanted signal image and clock harmonics.
The mixer, with LO, up-converts the baseband signal to VHF or UHF band.
NOTE: For different application, IT9518 without internal mixer and LPF.

8.5 DVB-T/ISDB-T COFDM Digital Signal Processing

8.5.1 Coding and Interleaving

The input TS stream is first scrambled using a pseudo random sequence, and then encoded using a (204,188) shortened Reed-Solomon code with 8-byte error correcting ability. The output of the Reed-Solomon encoder then passes through a Forney-style convolutional interleaver, and the output is further encoded using a punctured convolutional encoder whose code rate can be 1/2, 2/3, 3/4, 5/6, or 7/8. Finally the output of the punctured convolutional encoder is interleaved using a bit-wise interleaving and symbol interleaving. The scrambler, encoders, and interleavers are specified in EN 300 744 and STD-B31 V1.6.

8.5.2 Frequency-Domain Signal Processing

The output of the symbol interleaver is mapped onto QPSK, 16-QAM, or 64-QAM constellations in accordance to EN 300 744 and STD-B31 V1.6. The resulting constellation points are then grouped into OFDM frames according to the DVB-T and ISDB-T frame structure. Each OFDM symbol is processed by the Fast Fourier Transformer (FFT) of IT9510, the core of which uses a 50-bit internal architecture to ensure excellent accuracy.

8.5.3 Time-Domain Signal Processing

The FFT output is re-sampled using a high quality rate converter. At the core of the rate converter are adaptively controlled low-order polynomial interpolators, so that multiple signal bandwidths can be supported at a low cost. The output of the rate converter is then directly applied to the DAC without further processing.

8.6 2-Wire Interfaces

IT9510 provides a 2-wire interface for communicating with the host. It is also used to communicate with the second IT9510 series receiver IC for TS/USB reception. The IT9510 2-wire Interface uses, respectively, pins IOSDA for the serial data and IOSCL for the serial clock. The bus address of the IT9510 2-wire Interface is determined by the strapping pins GPIOH6 and GPIOH5. When IT9510 is first powered on, the RESETN pin should be held low. Given the IT9510 is desired for USB mode or the slave device under TS TS/USB mode, as the RESETN pin transitions from low to high, the logic level of the strapping pins GPIOH6 and GPIOH5 are latched to determine the 2-wire bus address, as shown in Table 8-3. Note that the logic level of the strapping pins, GPIOH6 and GPIOH5, also determines its operation mode, as described in Table 6-.

Table 8-3. IT9510 2-wire bus address mapping table

{ GPIOH6,GPIOH5} at strapping	2-Wire Bus Address
{0,0}	0x38
(0,1)	0x3A

The IT9510 2-wire Interface supports both read and write operations. The circuit works as a slave transmitter in the read operation mode and slave receiver in the write operation mode to communicate with the Host. To communicate with the second ITE series IC, the independent master circuit works as a master transmitter in the write operation mode and master receiver in the read operation mode.

Details on using the 2-wire Interface can be found in IT9510 Programming Guide.

8.7 Host Interfaces

IT9517/9513/9511/9518 provides flexible interface, the so-called Host Interface, for connecting to the host in stand-alone applications, and for connecting to the master device, slave device, or the host in the TS/USB receiving mode. Depending on the application, this Host Interface can be configured into input interfaces. Host Interface comprises pins HOST_B0~HOST_B11.

IT9517/9513/9511/9518 Host Interface (HOST_B0~HOST_B11) is used for connecting to the host in stand-alone modes, or for connecting to the master/slave device or the host in the TS/USB mode. When connecting to the host, Host Interface (HOST_B0~HOST_B11) is configured into the TS mode with appropriate address selection by appropriate setting the strapping pins listed in Table 6-. When connecting to the slave device, Host Interface should be configured as the TS input interface for TS/USB receiving.
Details on how to configure the IT9510 host interfaces can be found in IT9510 Programming Guide.

8.7.1 Transport Stream Interface

The pin descriptions of Host Interface of IT9510 under TS mode are listed in Table 8-4.

Table 8-4. IT9510 TS interface pins

Pin Name	TS Input Interface (**IT9517**/9513/9511/9518)	
	Function	**Description**
HOST_B0	MPEG Data[7]	# MPEG transport stream data. # 8-bit in the parallel mode and 1-bit in the serial mode. # Data[0] or Data[7] can be the data pin in the serial mode
HOST_B1	MPEG Data[6]	
HOST_B2	MPEG Data[5]	
HOST_B3	MPEG Data[4]	
HOST_B4	MPEG Data[3]	
HOST_B5	MPEG Data[2]	
HOST_B6	MPEG Data[1]	
HOST_B7	MPEG Data[0]	
HOST_B8	MPEG Clock	MPEG clock
HOST_B9	MPEG Valid	MPEG data valid
HOST_B10	MPEG Sync	MPEG packet sync pulse
HOST_B11	MPEG Fail	MPEG uncorrectable

		packet indicator

The TS interface of IT9510 offers both parallel/serial input. For IT9510 (IT9517/9513/9511/9518) operating in the TS mode to communicate from the Host, the TS interface can operate in the parallel input mode, serial input mode, or be disabled. A timing diagram of the parallel input mode is shown in the example of Figure 8-1. For the serial input mode, the TS data can be configured to be input on Data[7] or Data[0]. On the other hand, for an IT9510 (IT9517/9513/9511/9518) operating in the standard USB2.0 mode, the transport stream interface is disable by strapping and should no input driving during operation. A table of IT9510 TS interface modes is given in Table 8-5.

The IT9510 transport stream interface is fully configurable. The list of configurable parameters is shown in Table 8-6. Details on configuring the IT9510 TS interface are available in IT9510 Programming Guide.

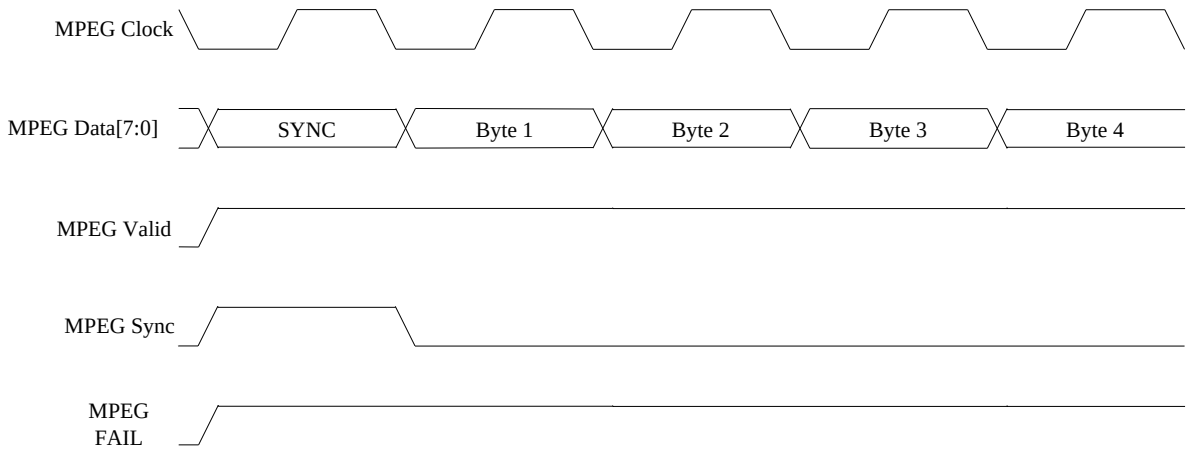


Figure 8-1. An example of TS parallel interface timing diagram

Table 8-5. The IT9510 TS interface mode selection

Part Number	Operation Mode	TS interface operation modes
IT9517/9513/9511	Standard USB2.0 mode	Serial Input. Data is on Data[7] or Data[0].
		Parallel Input

Table 8-6. Configurable parameters of the IT9510 TS interface

Parameter	Selections
Input Mode	Parallel Input Serial Input
Input data pin of serial mode.	Data[7] or Data[0]
Bit-Order	For Parallel Mode: Data[7] can be MSB or LSB For Serial Mode: Can be MSB first or LSB first.
Style of the MPEG-2 sync byte	MPEG-2 style or DVB-T style.
Signal polarity	Clock, Sync, Valid, and Fail can be independently configured to be active high or low.
The style of MPEG Valid	Continuous or gapped.
The gap between consecutive 188-byte payloads in units of byte times.	0 ~ 255
MPEG Sync assertion for the serial output mode, select whether MPEG Sync is asserted only for the first bit or for all bits of the first byte.	Asserted for all bits of the first byte or for the first bit only.
MPEG Clock frequency	Configurable
MPEG Sync pin for the serial input mode	Can be used or wired to ground.

8.7.1.1 Serial and Parallel Input Interface

The TS interface of IT9510 can become an input interface for accepting a TS stream and transmitted to receiver. Both parallel and serial data are supported for transmitted TS stream. An example timing diagram for the IT9510 TS serial input interface is shown in Fig 8-2.

MPEG Clock ccccccccccc:::ccccccccccccccc
MPEG Data[7] zmsssssssss:::ssssizzzmsssssss
MPEG Valid lkhhhhhhhhhh:::hhhhtlllkhhhhhhh
MP Sync (bit length) lktlllllllll:::llllllllktllllll

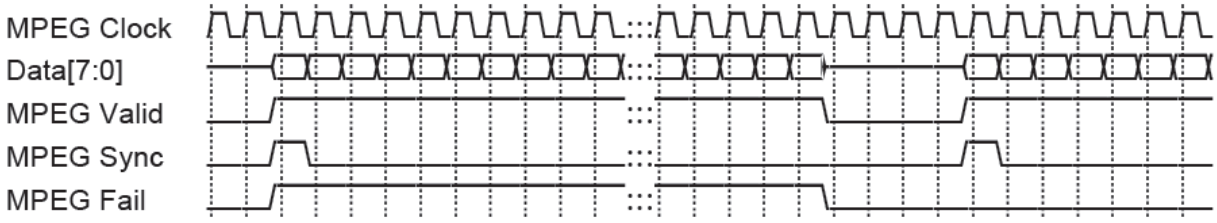


Figure 8-2. Timing diagram of the IT9510 TS serial input interface

MPEG Sync of IT9510 can be wired to the ground if MPEG Sync is not available from the TS stream provider.

8.7.1.2 PCR re-stamping

If a network or a Transport Stream re-multiplexor varies the delay in delivering the data stream from the encoder or storage system to the decoder, such variations tend to cause a difference between the values of the PCRs and the values that they should have when they are actually received. This is referred to as PCR jitter. Because of null packet insertion, IT9510 introduced PCR re-stamping mechanism to avoid PCR jitter. Although PCR jitter caused by null packet insertion is under one packet time, it still violates PCR requirement. In order to keep PCR accuracy, IT9510 provide several ways to reassign new PCR values to PCR packets for PCR accuracy.

8.8 USB Interface

IT9510 supports USB 2.0 standard with many configurable parameters in the Endpoint 0 descriptors.

8.8.1 USB Descriptors

Most strings and parameters in the descriptors are configurable in the external EEPROM, including:
Device descriptors: vender ID, product ID, device release number, manufacturer string index, product string index, serial number string index, configuration characteristics (self-powered, remote wake-up, …etc.), max power consumption, and interrupt endpoint (Endpoint 3) polling interval; and

Strings: the string description of the manufacturer and the product and the serial number. These strings are defined in USB 2.0 standard.

Please refer IT9510 Programming Guide for details on the external EEPROM.

8.8.2 USB Control Protocol

Basic USB transfer and control scenario detail as follow:

8.8.2.1 Default Endpoint (Endpoint 0)

Endpoint 0 is the same as defined in USB 2.0 standard.

8.8.2.2 Control Message

Proprietary control messages are sent through a request-and-reply model. Any request packet corresponds to a reply packet, unless the communication is malfunctioning. A sequence number field is employed in each control packet to resolve the late reply and duplicate request/reply problems.

The available control messages include those for getting the current configuration, downloading the firmware, computing firmware checksum, booting IT9510, copying the firmware to a slave device, reading and writing the IT9510 memory, as well as 2-wire bus control messages, software reset control messages, and Control Unit command control messages

8.8.2.3 Data Message

Data messages convey the transport streams received by IT9510.

8.9 IR Interface

IT9510 supports IR protocols such as NEC, RC5, and RC6. The IR function can be enabled or disabled and the IR protocol can be selected by appropriately setting the corresponding fields in the external EEPROM. For IT9510 operating in the standard USB 2.0 mode, it considered as a USB composite device with HID when the IR function is enabled. Otherwise it is a USB single device. More details on EEPROM settings are available in IT9510 Programming Guide. The IT9510 IR decoder decodes raw signals received from the IR photo-receiver. Then the demodulated signals are converted to HID (Human Interface Devices) format according to a translation table that is downloaded from the driver via the memory write protocol (See 8.8.2 for more details on USB control protocols). At last the USB host receives IR messages via USB Endpoint 3.

More details of the IT9510 IR interface are available in *IT9510 Programming Guide*.

8.9.1 The Function Keys and Alternative Keys

The function key (FN) is used to create alternative key sequences for a remote control. When FN of a remote control is pressed, an alternative key sequence is initiated, and any keys pressed are considered “alternative” if they are pressed within a predefined expiration time after the previous key press. This design enables a remote control with fewer keys (buttons) to almost double its “effective” number of keys. IT9510 will not send any key when only the function key is pressed

Alternative keys are supported in IT9510 as mentioned in *IT9510 Programming Guide.*

8.9.2 The External EEPROM

An external EEPROM can be used for storing USB related information and possibly other hardware related information in systems using IT9510. The content and format of the external EEPROM is given in detail in *IT9510 Programming Guide*.

8.9.3 Boot Scheme (Provide EEPROM boot)

Detailed boot scheme of IT9510 is described in *IT9510 Programming Guide.*

8.10 I2S Audio Interface Basic Operation:

The digital audio interface operates in slave mode and supports the following MSB first audio data formats: I2S, left justified and right justified. In I2S mode, the IT9510 transmit with data to clocks it receives over the digital audio interface. The interface has six pins which up audio data to six channels, ADC digital data input (DIN) by three, bit clock input (BCLK), master clock input (MCLK), and a L/R channel indicator (LRCLK).
In I2S mode, the MSB is available on the second rising edge of BCLK following a DFS transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency, and sample rate, there

may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

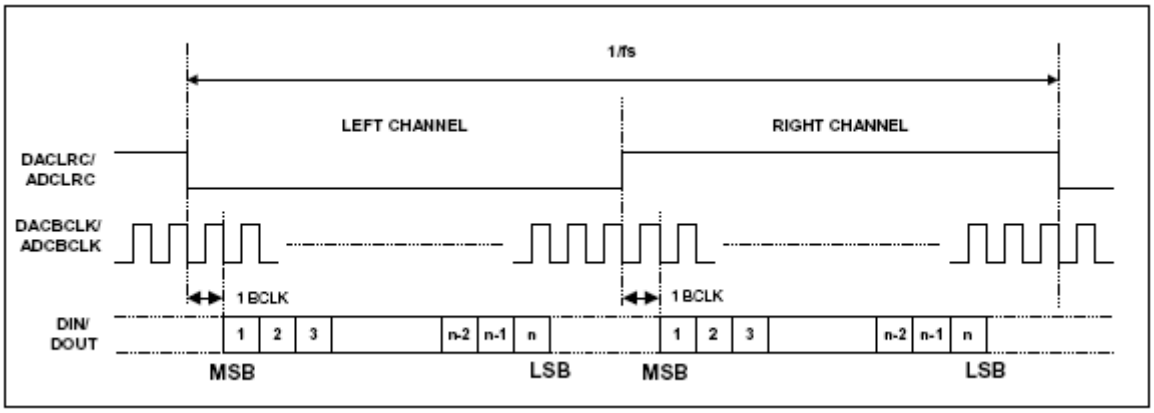


Figure 8.10-1 I2S Data Format and Protocal.

8.11 GPIO Interface

Please refer to *IT9510 GPIO User Manual* for application detail.

9. Power Modes

9.1 Power Modes

IT9510 supports the following power modes, as shown in Table 9-1:

1. Suspend – all functions are turned off except for one internal slow clock and the suspend control block. It could be initiated by USB suspend operation or by applying a high voltage on the GPIOH5 pin with appropriate parameters setting.

Table 9-1. Power mode table

States	Slow clock	IT9510	Host interface
Suspend	ON	OFF (Only USB PHY and control block active)	OFF

The transition time between each power state is listed in Table 9-2.

Table 9-2. IT9510 power state transition time

From \ To	Suspend mode
Suspend mode	N/A

9.2 Current Consumption

For the current consumption detail, please refer to *IT9510 Power Consumption Report.*

10. Register Descriptions

For register descriptions, please refer to *IT9510 Programming Guide*.

11. DC Characteristics

11.1 Absolute Maximum Ratings*

Table 11-1. IT9510 absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Core Power Voltage	VCC	-0.3	1.32	V
I/O Power Voltage	VCC3V	-0.3	3.6	V
USB Power Supply	AVDDHP	-0.3	3.6	V
Internal Regulator Power Voltage	VDDH_REG VCC3V	-0.3	3.6	V
Voltage on input pins	VI	-0.3	VCC3V+0.3	V
Voltage on output pins	VO	-0.3	VCC3V+0.3	V
Storage Temperature	Tstg	-40	150	ºC
Junction Temperature	Tj		125	ºC

MQFN64 Junction-Ambient Thermal Resistance (2-layer PCB)	Air Flow	0	1	2	3	m/s
	Rth(j-a)	63.1	50.5	45.5	43	ºC/W
MQFN64 Junction-Ambient Thermal Resistance (4-layer PCB)	Air Flow	0	1	2	3	m/s
	Rth(j-a)	24.4	21.4	20.2	19.7	ºC/W

***Comments**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

11.2 Operating Conditions

Table 11-2. IT9510 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
VHF band III frequency range	IN_VHF	50		300	MHz
UHF band frequency range	IN_UHF	300		950	MHz
Core Power	VCC	1.08	1.2	1.32	V

I/O Power Voltage	VCC3V	2.97	3.3	3.6	V
Power for USB	AVDDHP	2.97	3.3	3.6	V
Internal Regulator Power Supply	VDDAH_REG 1/2 VCC3V	3.0	3.3	3.6	V
Ambient Operating Temperature (Commercial)	Ta	0		70	ºC
Ambient Operating Temperature (Industrial)	Ta	-40		85	ºC

11.3 DC Electrical Characteristics

Table 11-3. IT9510 DC electrical characteristics

Note: RF_VDD=3.3V, VDD1=1.2V, VCC3V=3.3V, AVDDHP=3.3V, and Ta=25 ºC unless otherwise specified.

Parameter	Symbol	Test Condition	Min.	Typ	Max.	Unit
High Level Input Voltage for 3.3v IO	VIH		2.0			V
Low Level Input Voltage for 3.3v IO	VIL				0.8	V
Input Capacitance	Cin			3		pF
Power Consumption (Operating, with internal voltage regulator)	P_{op}*	USB mode		650		mW
		MPEG-TS mode		620		mW
Power Consumption (Suspend, with internal voltage regulator)	P_{sus}	Suspend (USB)				mW
		Suspend (by GPIOH5)				
High Level Output Voltage for 3.3v IO	VOH		3.0			V
Low Level Output Voltage for 3.3v IO	VOL				0.4	V
High/Low Level Output Current	IOH/IOL	Digital Output Pins	0		4	mA
High/Low Level Output Current	IOH/IOL	5V tolerant Open-Drain	0		2	mA
Operation Current for 3.3V (include internal voltage regulator)		USB mode		197		mA
		MPEG-TS mode		187		mA
Operation Current for 1.4V				65		mA
Operation Current for 1.2V				35		mA

Note: *Test signal: Mode 3, 64QAM, Code Rate 7/8, GI 1/32 for DVB-T.

12. AC Characteristics

12.1 TS Input

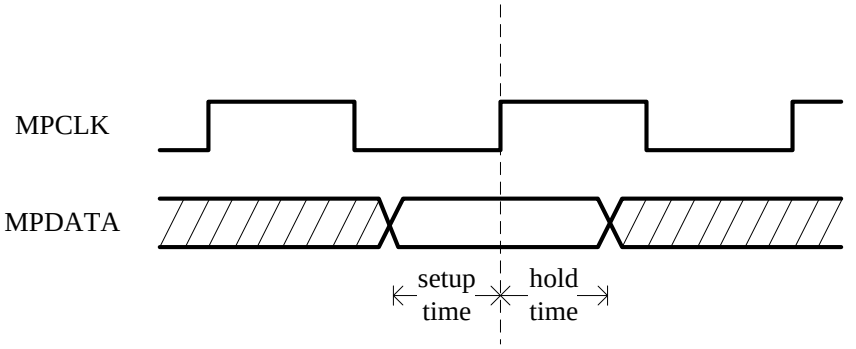


Figure 12-1. IT9510 TS input timing diagram

Table 12-1. IT9510 TS input timing

Parameter	Requirement	Unit
Input Set-up Time	8.29	ns
Input Hold Time	0.5	ns

12.2 2-Wire Bus Output Timing

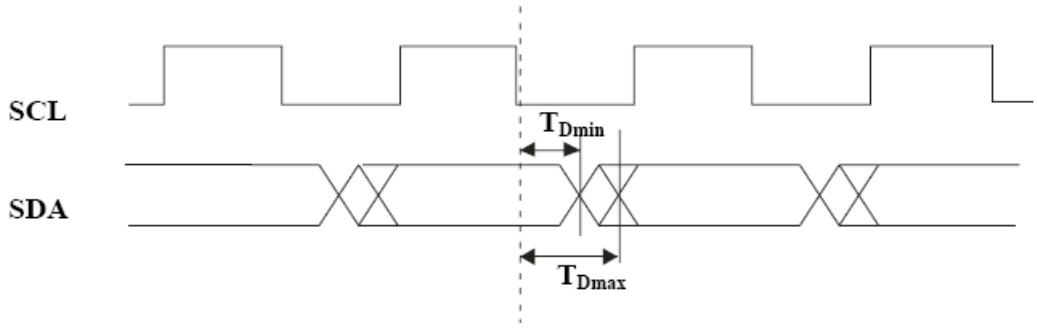


Figure 12-2. IT9510 2-wire bus output timing diagram.

Table 12-2. IT9510 2-wire bus output timing.

Parameter	Description	Min.	Max.	Unit

T_{Dmin}	Minimum valid delay of 2-wire bus output	T/2 + 2	NA	ns
T_{Dmax}	Maximum valid delay of 2-wire bus output	NA	T/2+6	ns

12.3 2-Wire Bus Input Timing

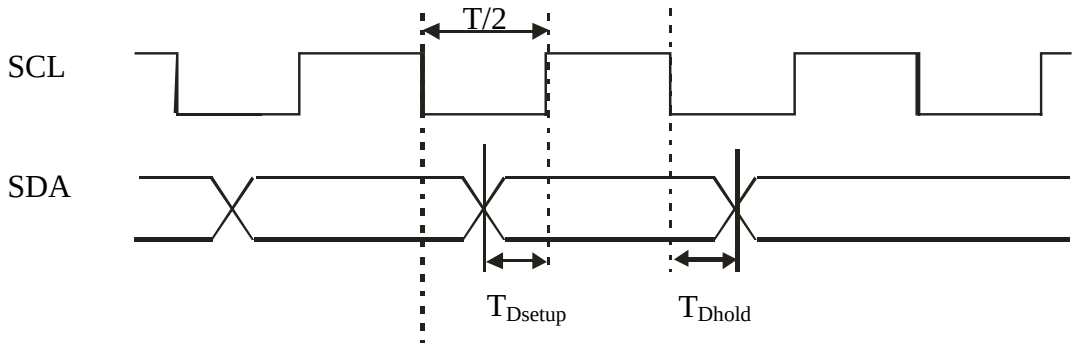
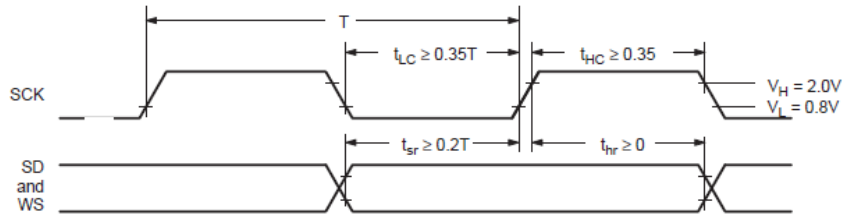


Figure 12-3. IT9510 2-wire bus input timing diagram.

Table 12-3. IT9510 2-wire bus input timing.

Parameter	Description	Min.	Max.	Unit
T_{Dsetup}	2-wire bus input setup time	2	T/2 -2	ns
T_{Dhold}	2-wire bus input hold time	2	T/2 -2	ns

12.4 I2S Bus Input Timing



T = clock period
T_r = minimum allowed clock period for transmitter
T > T_r

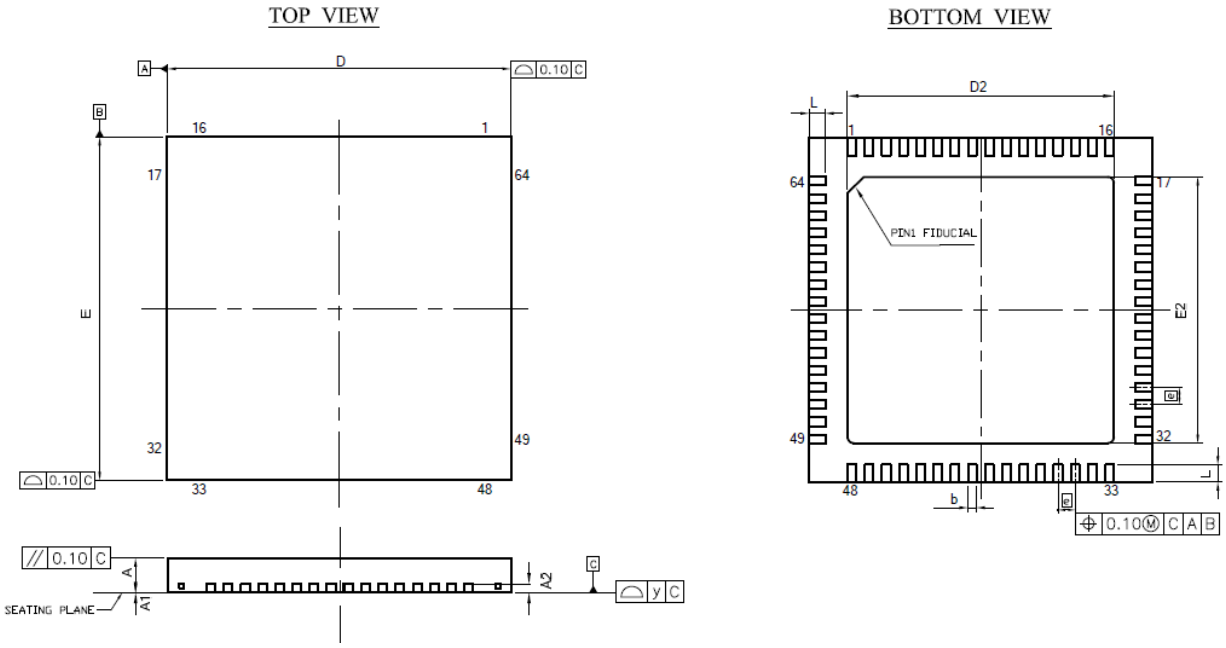
Figure 12-4. IT9510 I2S receiver timing diagram.

Table 12-4. IT9510 I2S receiver timing diagram.

Parameter	Description	Min.	Max.	Unit
T_{Dsetup}	I2S receiver timing diagram	2	T/2 -2	ns
T_{Dhold}	I2S receiver timing diagram	2	T/2 -2	ns

13. Package

MQFN 64 Package Outline Dimension (8mm*8mm)

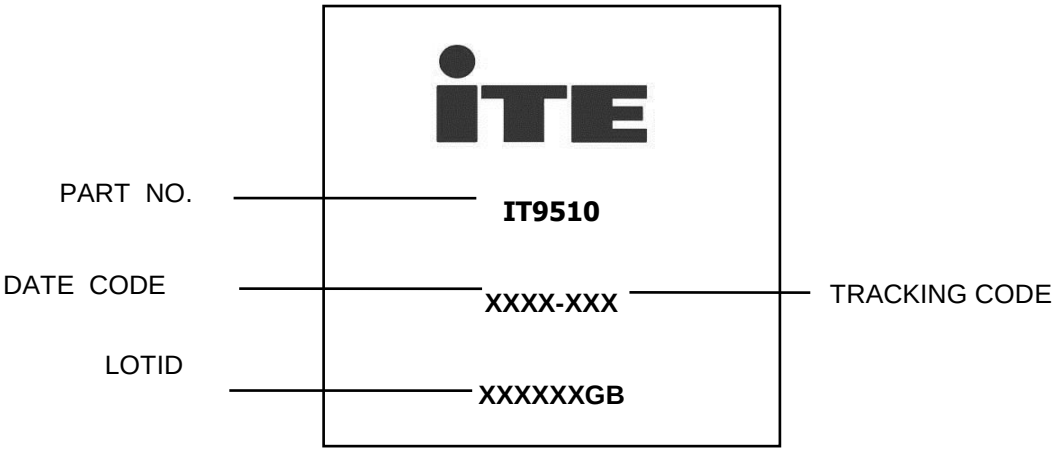


Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.028	0.030	0.031	0.70	0.75	0.80
A1	0.000	0.001	0.002	0.00	0.02	0.05
A3	0.008 REF			0.203 REF		
b	0.006	0.008	0.010	0.15	0.20	0.25
D	0.311	0.315	0.319	7.90	8.00	8.10
D2	0.240	---	0.260	6.10	---	6.60
E	0.311	0.315	0.319	7.90	8.00	8.10
E2	0.240	---	0.260	6.10	---	6.60
e	0.016 BSC			0.40 BSC		
L	0.014	0.016	0.018	0.35	0.40	0.45
y	--	--	0.003	--	--	0.08

Notes:

1. Controlling dimension：Millimeter
2. Reference document：Jedec Mo-220.
3. Take SMT into consideration, please use the minimum number of D2's and E2's dimensions.

14. Top Marking Information



ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.

(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.

(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.

(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.

(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).

(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.

(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.

(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.

(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.

(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.

(c) Buyer will not return any goods without first obtaining a customer return order number.

(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.

(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.

(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.