ITE 聯陽半導體 ITE Tech. Inc.

IT9500 (AX) series
IT9507/IT9503

Transmitter
for AirHD® & ccHDtv ®

Preliminary V1.1

ITE Tech. Inc.
Easy HD Expressway

airHD® ccHDtv®

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Revision History

Section	Revision	Page No.
	First release for IT9500 AX Series (IT9507FN/AX)	
5	Two wire bus descriptions updated	10

CONTENTS

FIGURES

TABLES

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1. Features

- **Modulator**
  - ETSI, DVB-T/H (EN 300 744 V1.5.1) Compliant baseband transmitter for Digital Terrestrial Television
  - Configurable code rate: 1/2,2/3,3/4,5/6,7/8
  - Programmable QPSK, 16-QAM and 64-QAM Symbol Mapping
  - Configurable support for 2k and 8k FFT
  - Programmable Guard Interval (1/4, 1/8, 1/16, 1/32)
  - Supports variable channel band width from 2 MHz to 8 MHz
  - Zero I/F complex base band I/Q output with integrated DAC and anti-aliasing filter
  - MER > 40dB
  - Carrier Suppression > 50dB
  - Spectrum Shoulders: 55 dB for perfect adjacent-channel operations
- On-chip voltage regulator:
  - Enables single supply 2.7V-3.6V operation.
  - May use 1.7V-2.0V supply for lower power.
- Integrated local oscillator for external RF mixer; frequency tuning range 50MHz~950MHz.
- 12MHz clock output to enable single-crystal system design.
- Serial and parallel **MPEG2-TS** input interface.
- Integrated transport stream de-multiplexer (**PID filtering**) with bypass mode.
- Programmable SI/PSI table insertion
- **Control interfaces**
  - Embedded **USB 1.1** and **2.0** compatible interface support with suspend mode.
  - UART
  - 1x IIC master and 1x IIC slave
- Infrared (**IR**) interface provided for remote control.
- Up to 8 independent GPIO pins
- MQFN-64 package, both commercial and **industrial** grades are available.
  -

2. General Description

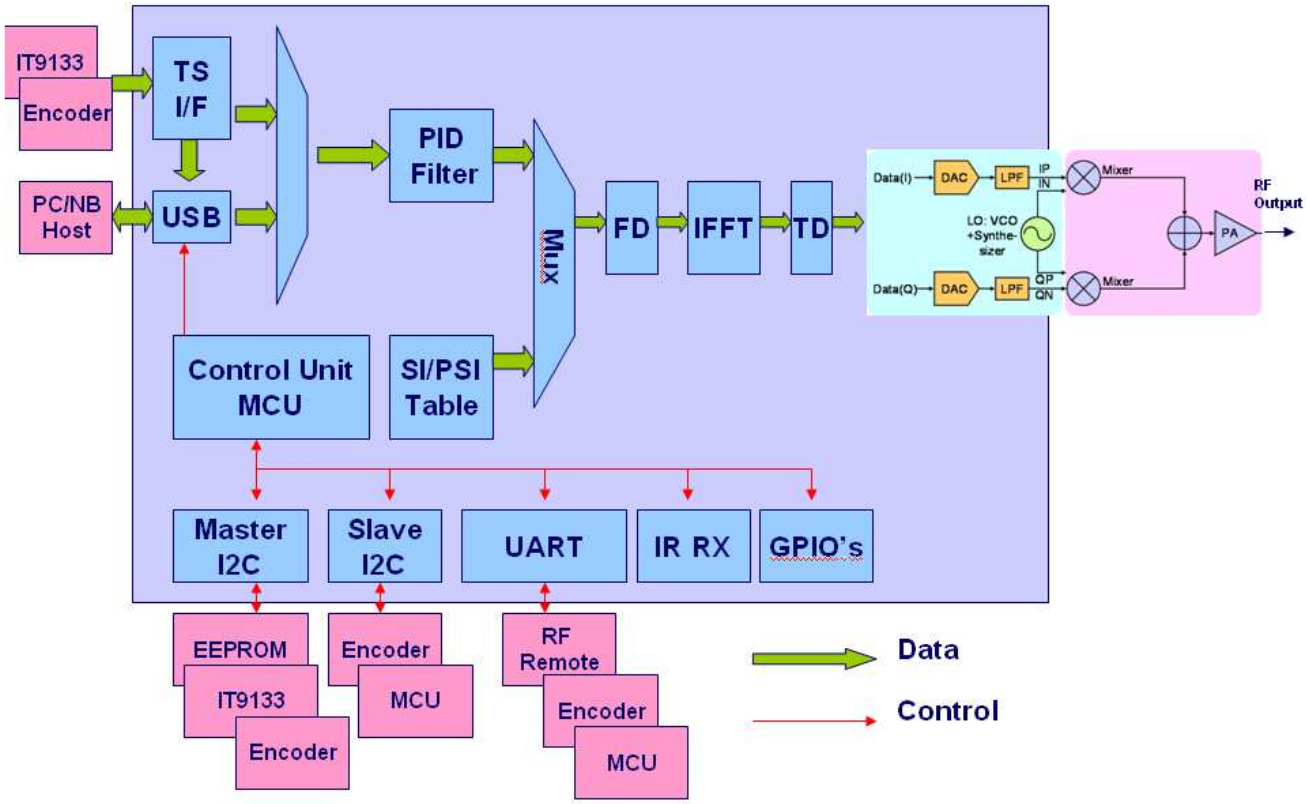
IT9500 is a series of highly integrated transmitter for AirHD, DTVCam, and other personal, community, or professional digital TV head-end applications. The core of IT9500 is a DVB-T COFDM modulator. The high level of integration of IT9500 significantly decreases the power consumption, board size and cost of modulators in digital TV transmitter. With IT9500, a low cost, low power, compact, reliable, high bandwidth and wireless (or wired) full HD delivery solution is easily achieved.

IT9500 offers very low total bill of materials (BOM) solutions. It includes processing units for forward error correction coding and digital modulation, D/A IQ converter, low-pass filters, and local oscillator for the external mixer. IT9500 series also supports flexible input interfaces, including embedded USB 2.0 interface, and serial/parallel TS interface input/output with built-in de-multiplexer.

IT9500 series is compliant to the non-hierarchical transmission specified in DVB-T (ETSI EN 300 744). A (204,188) Reed-Solomon encoder capable of correcting 8 error bytes is used to generate parity bytes for each input TS packet. The code rates of the punctured convolution encoder include 1/2, 2/3, 3/4, 5/6, and 7/8. Only native interleaving is used in IT9500. The output signal bandwidth is configurable from 2 MHz to 8 MHz. The supported signal constellations include QPSK, 16-QAM, and 64-QAM. FFT modes of 2k and 8k and guard intervals of 1/4, 1/8, 1/16, and 1/32 specified in EN 300 744 are supported. The transmission parameters are register-programmable, and are embedded in the Transmission Parameter Signaling (TPS) information as required by EN 300 744.

A complete set of application programming interface (API) is available, facilitating fast and easy integration into products on Windows Mobile, Windows CE, Windows 7, Windows XP, Vista, Linux, and many other operating systems. Furthermore, a complete set of USB drivers for Windows 7/XP/Vista, Windows Mobile/CE, and Linux are provided for IT9500.

3. Block Diagram



4. Pin Configuration (9503 only different in print)

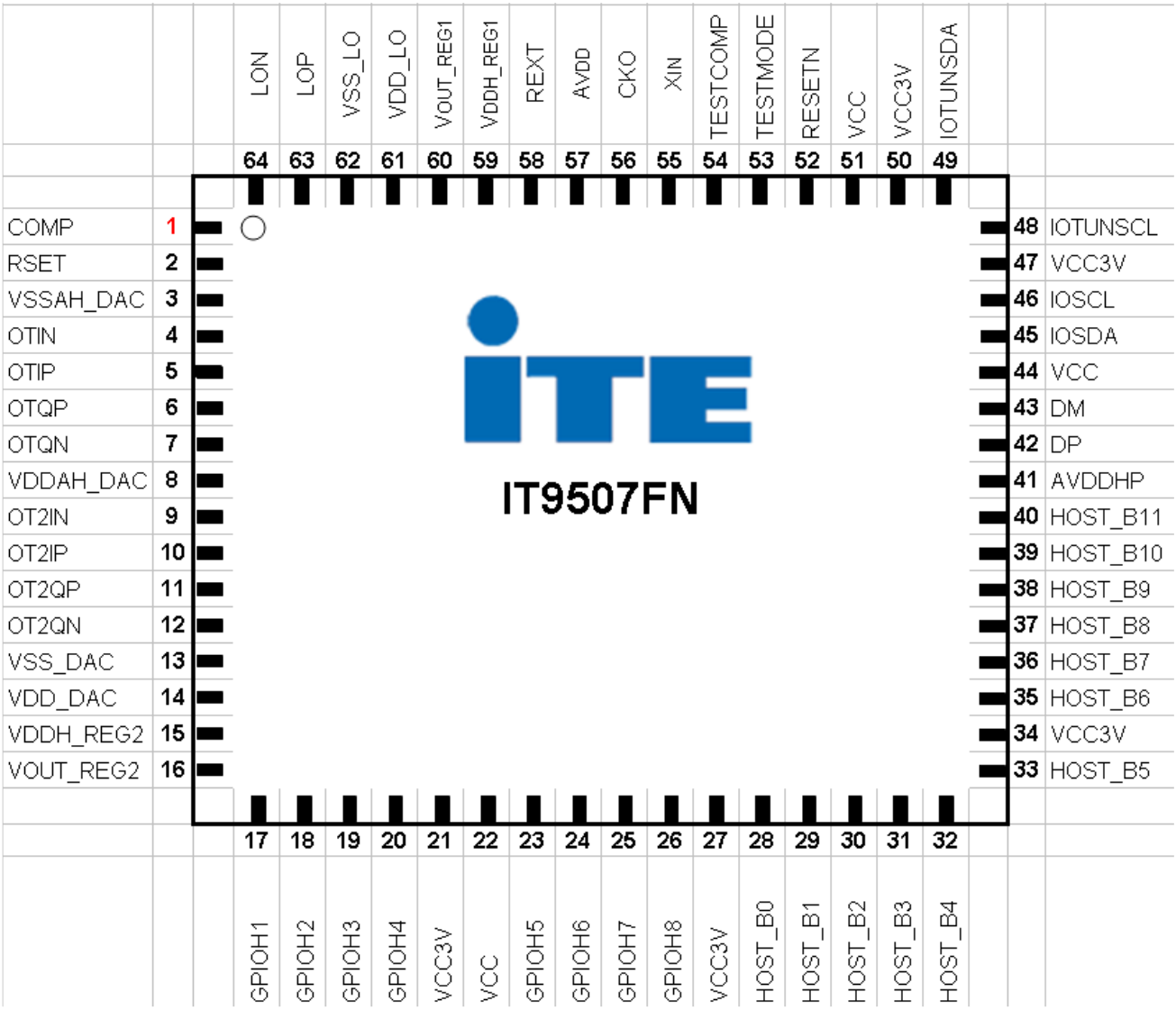


Table 4-1. IT9507/9503 pin listed in numeric order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	COMP	17	GPIOH1	33	HOST_B5	49	IOTUNSDA
2	RSET	18	GPIOH2	34	VCC3V	50	VCC3V
3	VSSAH_DAC	19	GPIOH3	35	HOST_B6	51	VCC
4	OTIN	20	GPIOH4	36	HOST_B7	52	RESETN
5	OTIP	21	VCC3V	37	HOST_B8	53	TESTMODE
6	OTQP	22	VCC	38	HOST_B9	54	TESTCOMP
7	OTQN	23	GPIOH5	39	HOST_B10	55	XIN
8	VDDAH_DAC	24	GPIOH6	40	HOST_B11	56	CKO
9	OT2IN	25	GPIOH7	41	AVDDHP	57	AVDD
10	OT2IP	26	GPIOH8	42	DP	58	REXT
11	OT2QP	27	VCC3V	43	DM	59	VDDH_REG1
12	OT2QN	28	HOST_B0	44	VCC	60	VOUT_REG1
13	VSS_DAC	29	HOST_B1	45	IOSDA	61	VDD_LO
14	VDD_DAC	30	HOST_B2	46	IOSCL	62	VSS_LO
15	VDDH_REG2	31	HOST_B3	47	VCC3V	63	LOP
16	VOUT_REG2	32	HOST_B4	48	IOTUNSCL	64	LON

5. Pin Description

Table 5-1. IT9507/9503 Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
14	VDD_DAC	PWR	-	***+1.4V Analog Power Supply***
8	VDDAH_DAC	PWR	-	***+3.3V Analog Power Supply***
15	VDDH_REG2	PWR	-	***+3.3V Analog Power Supply***
57	AVDD	PWR	-	***+1.4V Analog Power Supply***
59	VDDH_REG1	PWR	-	***+3.3V Analog Power Supply***
61	VDD_LO	PWR	-	***+1.4V Analog Power Supply***
22,44,51	VCC	PWR	-	***+1.2V Power Supply***
21,27,34,47,50	VCC3V	PWR	-	***+3.3V Power Supply***
41	AVDDHP	PWR	-	***+3.3V Power Supply for USB***

Table 5-2. IT9507/9503 Pin Description of Analog I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
1	COMP	AIO	-	***DAC External Cap***
2	RSET	AIO	-	***External Resistor for DAC***
4	OTIN	AIO	-	***DAC Output***
5	OTIP	AIO	-	***DAC Output***
6	OTQP	AIO	-	***DAC Output***
7	OTQN	AIO		***DAC Output***
9	OT2IN	AIO	-	***LPF Output***
10	OT2IP	AIO	-	***LPF Output***
11	OT2QP	AIO	-	***LPF Output***
12	OT2QN	AIO		***LPF Output***
16	VOUT_REG2	AO	VCC	***Internal LDO output (+1.2V)***
42	DP	AIO	-	***Differential Positive signal for USB***
43	DM	AIO	-	***Differential Negative signal for USB***
55	XIN	AI		***Xtal in***
56	CKO	AO	-	***Clock output for another device***
58	REXT	AIO	-	***External Resistor for DAC***
60	VOUT_REG1	AO	VDD_LO	***Internal LDO output (+1.4V)***
63	LOP	AIO		***LO output***
64	LON	AIO		***LO output***

Table 5-3. IT9507/9503 Pin Description of Digital I/O Signals

Pin(s) No.	Symbol	Attribute	Power	Description
52	RESETN	DI	VCC3V	***Power-on Reset (Low Active)***
53	TESTMODE	DI	VCC3V	***Test mode selection; tied to ground for normal operation.***
54	TESTCOMP	DI	VCC3V	***Test mode selection; tied to ground for normal operation./UART-RxD***
17	GPIOH1	DIO	VCC3V	***General purpose I/O***
18	GPIOH2	DIO	VCC3V	***General purpose I/O***
19	GPIOH3	DIO	VCC3V	***General purpose I/O***
20	GPIOH4	DIO	VCC3V	***General purpose I/O***

Pin(s) No.	Symbol	Attribute	Power	Description
23	GPIOH5	DO	VCC3V	***General purpose I/O***
24	GPIOH6	DIO	VCC3V	***General purpose I/O***
25	GPIOH7	DIO	VCC3V	***General purpose I/O***
26	GPIOH8	DIO	VCC3V	***General purpose I/O***
45	IOSDA	DIO	VCC3V	***Two-wire bus serial data line (It's slave mode for I2C/TS mode, but master mode for EEPROM access in USB mode)***
46	IOSCL	DO	VCC3V	***Two-wire bus serial clock line (It's slave mode for I2C/TS mode, but master mode for EEPROM access in USB mode)***
48	IOTUNSCL	DIO	VCC3V	***Two-wire bus serial clock line (master)***
49	IOTUNSDA	DO	VCC3V	***Two-wire bus serial data line (master)***
28	HOST_B0	DI	VCC3V	***Host interface***
29	HOST_B1	DI	VCC3V	***Host interface***
30	HOST_B2	DI	VCC3V	***Host interface***
31	HOST_B3	DI	VCC3V	***Host interface***
32	HOST_B4	DI	VCC3V	***Host interface***
33	HOST_B5	DI	VCC3V	***Host interface***
35	HOST_B6	DI	VCC3V	***Host interface***
36	HOST_B7	DI	VCC3V	***Host interface***
37	HOST_B8	DI	VCC3V	***Host interface***
38	HOST_B9	DI	VCC3V	***Host interface***
39	HOST_B10	DI	VCC3V	***Host interface***
40	HOST_B11	DI	VCC3V	***Host interface***

Table 5-4. Pin description of GPIO and strapping

Name	Strapping	IO Functions	State after RESET
GPIOH1	Clock Select Bit 0	GPIO/ PWM/ Lock Indicator 1	High-Z
GPIOH2	Clock Select Bit 1	GPIO/ PWM/ Lock Indicator 2	High-Z
GPIOH3	Clock Select Bit 2	GPIO/ PWM/ Lock Indicator 3	High-Z
GPIOH4	n/a	GPIO/ PWM/ Lock Indicator 4/ UART-TxD	High-Z
GPIOH5	Mode Select Bit 0/ Two-wire bus address bit 0	GPIO/ Suspend Resume	High-Z
GPIOH6	Mode Select Bit 1/ 1: Two-wire bus for AFE test 0: Two-wire bus normal mode	GPIO	High-Z
GPIOH7	Mode Select Bit 2/USB and TS	GPIO; IR receiving	High-Z

Name	Strapping	IO Functions	State after RESET
	mode switch		
GPIOH8	Mode Select Bit 3	GPIO	High-Z

Table 5-5. Strapping sampled at the rising edge of the RESET signal

Pin Name	Selection
{ GPIOH3,GPIOH2,GPIOH1}	Crystal frequency: 000 crystal = 12 MHz
{GPIOH8,GPIOH7,GPIOH6,GPIOH5}	Mode strapping and 2-wire bus address selection: (0,0,0,x) TS/I2C mode, { GPIOH5} = 2-wire address bit 1 (0,1,0,x) TS/USB mode (0,1,1,x) USB mode

Table 5-6. Pin list of Host Interface

Pin \ Mode	TS Input Mode
HOST_B0	MPEG Data[7]
HOST_B1	MPEG Data[6]
HOST_B2	MPEG Data[5]
HOST_B3	MPEG Data[4]
HOST_B4	MPEG Data[3]
HOST_ B5	MPEG Data[2]
HOST_B6	MPEG Data[1]
HOST_B7	MPEG Data[0]
HOST_B8	MPEG Clock
HOST_B9	MPEG Valid
HOST_B10	MPEG Sync
HOST_B11	MPEG Fail

Notes: 1) These pins have no integrated pull up/down.
2) The state of these pins immediately after reset is high-Z.
3) The pads of these pins are of the CMOS type.
4) These pins are on I/O power domain

6. Power Domains

IT9500 has four power domains: RF, Core, IO, and USB respectively.

The RF Domain is supplied by 3.3V±10% to provide power for analog functions. The external 3.3V should be connected to pin VDDAH_DAC and VDDH_REG2. The other analog power supply pins (1.4V) shall be connected to the pin VOUT_REG1 to be powered by the built-in voltage regulator.

The Core Domain is supplied by 1.2V±10% to provide power for the core circuits of IT9500. It can be provided by external 1.2V or using the internal voltage regulator from the pin VOUT_REG2.

The IO Domain provides power for the host interface, including the TS interface, 2-wire bus, UART and GPIOH1~GPIOH8. The supply voltage for IO Domain is 3.3V±10%.

The USB Power Domain is supplied by 3.3v±10% to power the USB interface under USB mode. Otherwise, the pin AVDDHP should be connected to ground.

7. Functional Descprition

7.1 Operation Modes

IT9500 supports three different operation modes, TS/I2C, TS/USB, and USB depending on the data path and control path. The mode is determined by appropriately setting the strapping pins as specified in Table 5- and register programming after strapping.

The supported operation modes of IT9500 are summarized in Table 7-1 and the control and data paths in each operation mode are summarized in Table 7-2.

Table 7-1. Operation modes of IT9500

Mode / Part #	TS/I2C	TS/USB	USB
IT9507	Yes	Yes	Yes
IT9503	Yes	Yes	Yes

Table 7-2. Data path and contol paths at each output mode

Path / Mode	Data Path	Control Path
TS/I2C	TS	2-wire bus
TS/USB	TS	USB
USB	USB	USB

7.1.1 TS/I2C Mode

In the TS/I2C mode, the transport stream to be transmitted comes through either the parallel or serial TS input interface. IT9500 is controlled by an external host controller (CPU) via the 2-wire (I2C) bus as an I2C slave device. More details of the TS interface are given in Section 7.7.1.

7.1.2 TS/USB Mode

In the TS/USB mode, the transport stream to be transmitted comes through either the parallel or serial TS input interface. IT9500 is controlled by an external host controller (CPU) via the USB bus as a USB device. More details of the TS interface are given in Section 7.7.1.

7.1.3 USB Mode

In the USB mode, IT9500 communicates with the host through the embedded USB 2.0 interface. The transport stream to be transmitted by IT9500 and control/status signals are all encapsulated in the USB frames. Besides, the host can access (read) the TS input thru USB EP5. More details of the USB interface are given in Section 7.8

7.2 Analog Interface

7.2.1 Clocking

IT9500 has on-chip crystal amplifiers for clock generation. Only single 12MHz crystal is required to generate all internal clocks.

IT9500 also provides a buffered clock output (CKO) which, for example, can be used to drive a second IT series receiver IC in TS/USB applications.

The IT9500 clocking circuit requires a stable reference clock. It can be provided by either of the following two methods:

1. Connect a crystal across the oscillator pin XTAL and ground, or
2. Connect an external clock source to the pin XTAL.

With programmable PLL, the supported reference clock frequency is 12MHz. This clock source can come from the crystal, other external clock source, or the buffered clock output (CKO) of another ITE receiver IC (in AirHD applications).

7.2.2 Clock Table

The programmable PLL default clock ratio is decided by pin strapping which is described in Table 5-. After the initial operation, it can also be re-programmed through register access. More details on programming the PLL ratio for different clock frequency selection can be found in *IT9500 Programming Guide*.

7.3 Initialization

Several important system parameters need to be programmed correctly in order to insure proper operations of IT9500. These include, among other things, the carrier frequency of the RF signal and DAC sampling frequency. More details on initializing IT9500 can be found in *IT9500 Programming Guide*.

7.4 LO, DAC and Filter

The analog front end consists of a local oscillator for VHF and UHF bands, a 16-bit high-speed IQ DAC, and a low pass filter.
The local oscillator provides wide-range differential clock outputs for external RF up-converter.
The 16-bit IQ DAC converts the digital modulator output into analog baseband signal using an embedded clock source.
The lowpass filter is an anti-aliasing filter for removing unwanted signal image and clock harmonics.

7.5 DVB-T COFDM Digital Signal Processing

7.5.1 Coding and Interleaving

The input TS stream is first scrambled using a pseudo random sequence, and then encoded using a (204,188) shortened Reed-Solomon code with 8-byte error correcting ability. The output of the Reed-Solomon encoder then passes through a Forney-style convolutional interleaver, and the output is further encoded using a punctured convolutional encoder whose code rate can be 1/2, 2/3, 3/4, 5/6, or 7/8. Finally the output of the

punctured convolutional encoder is interleaved using a bit-wise interleaving and symbol interleaving. The scrambler, encoders, and interleavers are specified in EN 300 744.

7.5.2 Frequency-Domain Signal Processing

The output of the symbol interleaver is mapped onto QPSK, 16-QAM, or 64-QAM constellations in accordance to EN 300 744. The resulting constellation points are then grouped into OFDM frames according to the DVB-T frame structure. Each OFDM symbol is processed by the Fast Fourier Transformer (FFT) of IT9500, the core of which uses a 50-bit internal architecture to ensure excellent accuracy.

7.5.3 Time-Domain Signal Processing

The FFT output is re-sampled using a high quality rate converter. At the core of the rate converter are adaptively controlled low-order polynomial interpolators, so that multiple signal bandwidths can be supported at a low cost. The output of the rate converter is then directly applied to the DAC without further processing.

7.6 2-Wire Interfaces

IT9500 provides a 2-wire interface for communicating with the host. It is also used to communicate with the second IT9500 series receiver IC for TS/USB reception. The IT9500 2-wire Interface uses, respectively, pins IOSDA for the serial data and IOSCL for the serial clock. The bus address of the IT9500 2-wire Interface is determined by the strapping pins GPIOH6 and GPIOH5. When IT9500 is first powered on, the RESETN pin should be held low. Given the IT9500 is desired for USB mode or the slave device under TS TS/USB mode, as the RESETN pin transitions from low to high, the logic level of the strapping pins GPIOH6 and GPIOH5 are latched to determine the 2-wire bus address, as shown in Table 7-3. Note that the logic level of the strapping pins, GPIOH6 and GPIOH5, also determines its operation mode, as described in Table 5-.

Table 7-3. IT9500 2-wire bus address mapping table

{GPIOH6, GPIOH5} at strapping	2-Wire Bus Address
{0,0}	0x38
{0,1}	0x3A

The IT9500 2-wire Interface supports both read and write operations. The circuit works as a slave transmitter in the read operation mode and slave receiver in the write operation mode to communicate with the Host. To communicate with the second ITE series IC, the independent master circuit works as a master transmitter in the write operation mode and master receiver in the read operation mode.

Details on using the 2-wire Interface can be found in IT9500 Programming Guide.

7.7 Host Interfaces

IT9507/9503 provides flexible interface, the so-called Host Interface, for connecting to the host in stand-alone applications, and for connecting to the master device, slave device, or the host in the TS/USB receiving mode. Depending on the application, this Host Interface can be configured into input interfaces. Host Interface comprises pins HOST_B0~HOST_B11.

IT9507/9503 Host Interface (HOST_B0~HOST_B11) is used for connecting to the host in stand-alone modes, or for connecting to the master/slave device or the host in the TS/USB mode. When connecting to the host,

Host Interface (HOST_B0~HOST_B11) is configured into the TS mode with appropriate address selection by appropriate setting the strapping pins listed in Table 5-. When connecting to the slave device, Host Interface should be configured as the TS input interface for TS/USB receiving.
Details on how to configure the IT9500 host interfaces can be found in IT9500 Programming Guide.

7.7.1 Transport Stream Interface

The pin descriptions of Host Interface of IT9500 under TS mode are listed in Table 7-4.

Table 7-4. IT9500 TS interface pins

Pin Name	TS Input Interface (IT9507/9503)	
	Function	Description
HOST_B0	MPEG Data[7]	# MPEG transport stream data. # 8-bit in the parallel mode and 1-bit in the serial mode. # Data[0] or Data[7] can be the data pin in the serial mode
HOST_B1	MPEG Data[6]	
HOST_B2	MPEG Data[5]	
HOST_B3	MPEG Data[4]	
HOST_B4	MPEG Data[3]	
HOST_B5	MPEG Data[2]	
HOST_B6	MPEG Data[1]	
HOST_B7	MPEG Data[0]	
HOST_B8	MPEG Clock	MPEG clock
HOST_B9	MPEG Valid	MPEG data valid
HOST_B10	MPEG Sync	MPEG packet sync pulse
HOST_B11	MPEG Fail	MPEG uncorrectable packet indicator

The TS interface of IT9500 offers both parallel/serial input. For IT9500 (IT9507/9503) operating in the TS mode to communicate from the Host, the TS interface can operate in the parallel input mode, serial input mode, or be disabled. A timing diagram of the parallel input mode is shown in the example of Figure 7-1. For the serial input mode, the TS data can be configured to be input on Data[7] or Data[0]. On the other hand, for an IT9500 (IT9507/9503) operating in the standard USB2.0 mode, the transport stream interface is disable by strapping and should no input driving during operation. A table of IT9500 TS interface modes is given in Table 7-5.

The IT9500 transport stream interface is fully configurable. The list of configurable parameters is shown in

Table 7-6. Details on configuring the IT9500 TS interface are available in IT9500 Programming Guide.

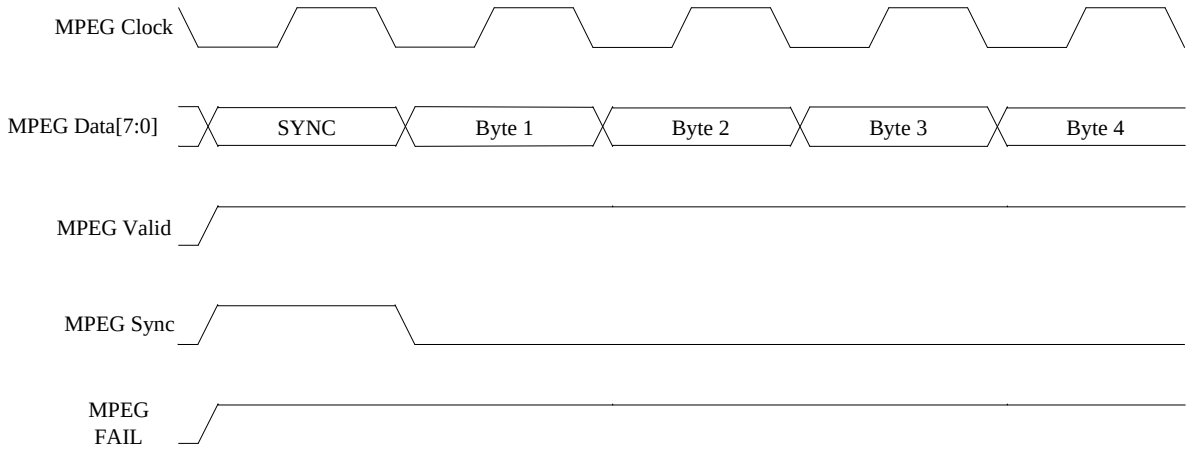


Figure 7-1. An example of TS parallel interface timing diagram

Table 7-5. The IT9500 TS interface mode selection

Part Number	Operation Mode	TS interface operation modes
IT9507/9503	Standard USB2.0 mode	Serial Input. Data is on Data[7] or Data[0].
		Parallel Input

Table 7-6. Configurable parameters of the IT9500 TS interface

Parameter	Selections
Input Mode	Parallel Input Serial Input
Input data pin of serial mode.	Data[7] or Data[0]
Bit-Order	For Parallel Mode: Data[7] can be MSB or LSB For Serial Mode: Can be MSB first or LSB first.
Style of the MPEG-2 sync byte	MPEG-2 style or DVB-T style.
Signal polarity	Clock, Sync, Valid, and Fail can be independently configured to be active high or low.
The style of MPEG Valid	Continuous or gapped.
The gap between consecutive 188-byte payloads in units of byte times.	0 ~ 255
MPEG Sync assertion for the serial output mode, select whether MPEG Sync is asserted only for the first bit or for all bits of the first byte.	Asserted for all bits of the first byte or for the first bit only.
MPEG Clock frequency	Configurable
MPEG Sync pin for the serial input mode	Can be used or wired to ground.

7.7.1.1 Serial and Parallel Input Interface

The TS interface of IT9500 can become an input interface for accepting a TS stream and transmitted to receiver. Both parallel and serial data are supported for transmitted TS stream. An example timing diagram for the IT9500 TS serial input interface is shown in Figure 7-2.

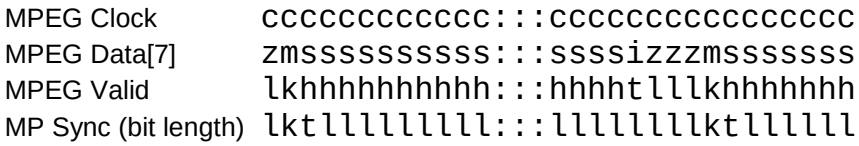


Figure 7-2. Timing diagram of the IT9500 TS serial input interface

MPEG Sync of IT9500 can be wired to the ground if MPEG Sync is not available from the TS stream provider.

7.8 USB Interface

IT9500 supports USB 2.0 standard with many configurable parameters in the Endpoint 0 descriptors.

7.8.1 USB Descriptors

Most strings and parameters in the descriptors are configurable in the external EEPROM, including:
Device descriptors: vender ID, product ID, device release number, manufacturer string index, product string index, serial number string index, configuration characteristics (self-powered, remote wake-up, …etc.), max power consumption, and interrupt endpoint (Endpoint 3) polling interval; and

Strings: the string description of the manufacturer and the product and the serial number. These strings are defined in USB 2.0 standard.

Please refer IT9500 Programming Guide for details on the external EEPROM.

7.8.2 USB Control Protocol

Basic USB transfer and control scenario detail as follow:

7.8.2.1 Default Endpoint (Endpoint 0)

Endpoint 0 is the same as defined in USB 2.0 standard.

7.8.2.2 Control Message

Proprietary control messages are sent through a request-and-reply model. Any request packet corresponds to a reply packet, unless the communication is malfunctioning. A sequence number field is employed in each control packet to resolve the late reply and duplicate request/reply problems.

The available control messages include those for getting the current configuration, downloading the firmware, computing firmware checksum, booting IT9500, copying the firmware to a slave device, reading and writing the IT9500 memory, as well as 2-wire bus control messages, software reset control messages, and Control Unit command control messages

7.8.2.3 Data Message

Data messages convey the transport streams received by IT9500.

7.9 IR Interface

IT9500 supports IR protocols such as NEC, RC5, and RC6. The IR function can be enabled or disabled and the IR protocol can be selected by appropriately setting the corresponding fields in the external EEPROM. For IT9500 operating in the standard USB 2.0 mode, it considered as a USB composite device with HID when the IR function is enabled. Otherwise it is a USB single device. More details on EEPROM settings are available in IT9500 Programming Guide. The IT9500 IR decoder decodes raw signals received from the IR photo-receiver. Then the demodulated signals are converted to HID (Human Interface Devices) format according to a translation table that is downloaded from the driver via the memory write protocol (See 7.8.2 for more details on USB control protocols). At last the USB host receives IR messages via USB Endpoint 3.

More details of the IT9500 IR interface are available in *IT9500 Programming Guide*.

7.9.1 The Function Keys and Alternative Keys

The function key (FN) is used to create alternative key sequences for a remote control. When FN of a remote

control is pressed, an alternative key sequence is initiated, and any keys pressed are considered “alternative” if they are pressed within a predefined expiration time after the previous key press. This design enables a remote control with fewer keys (buttons) to almost double its “effective” number of keys. IT9500 will not send any key when only the function key is pressed

Alternative keys are supported in IT9500 as mentioned in *IT9500 Programming Guide.*

7.9.2 The External EEPROM

An external EEPROM can be used for storing USB related information and possibly other hardware related information in systems using IT9500. The content and format of the external EEPROM is given in detail in *IT9500 Programming Guide*.

7.9.3 Boot Scheme

Detailed boot scheme of IT9500 is described in *IT9500 Programming Guide.*

7.10 GPIO Interface

Please refer to *IT9500 GPIO User Manual* for application detail.

8. Power Modes

8.1 Power Modes

IT9500 supports the following power modes, as shown in Table 8-1:

1. Suspend – all functions are turned off except for one internal slow clock and the suspend control block. It could be initiated by USB suspend operation or by applying a high voltage on the GPIOH5 pin with appropriate parameters setting.

Table 8-1. Power mode table

States	Slow clock	IT9500	Host interface
Suspend	ON	OFF (Only USB PHY and control block active)	OFF

The transition time between each power state is listed in Table 8-2.

Table 8-2. IT9500 power state transition time

To / From	Suspend mode
Suspend mode	N/A

8.2 Current Consumption

For the current consumption detail, please refer to *IT9500 Power Consumption Report.*

9. Register Descriptions

For register descriptions, please refer to *IT9500 Programming Guide*.

10. DC Characteristics

10.1 Absolute Maximum Ratings*

Table 10-1. IT9500 absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Core Power Voltage	VDD1	-0.3	1.32	V
I/O Power Voltage	VCC3V	-0.3	3.6	V
USB Power Supply	AVDDHP	-0.3	3.6	V
Internal Regulator Power Voltage	VDDAH_REG VCC3V	-0.3	3.6	V
Voltage on input pins	VI	-0.3	VCC3V+0.3	V
Voltage on output pins	VO	-0.3	VCC3V+0.3	V
Storage Temperature	Tstg	-40	150	ºC
Junction Temperature	Tj		125	ºC

MQFN64 Junction-Ambient Thermal Resistance (2-layer PCB)	Air Flow	0	1	2	3	m/s
	Rth(j-a)	63.1	50.5	45.5	43	ºC/W
MQFN64 Junction-Ambient Thermal Resistance (4-layer PCB)	Air Flow	0	1	2	3	m/s
	Rth(j-a)	24.4	21.4	20.2	19.7	ºC/W

***Comments**
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

10.2 Operating Conditions

Table 10-2. IT9500 operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
VHF band III frequency range	IN_VHF	50		300	MHz
UHF band frequency range	IN_UHF	300		950	MHz
Core Power	VCC	1.08	1.2	1.32	V

I/O Power Voltage	VCC3V	2.97	3.3	3.6	V
Power for USB	AVDDHP	2.97	3.3	3.6	V
Internal Regulator Power Supply	VDDAH_REG1 VCC3V	3.0	3.3	3.6	V
Ambient Operating Temperature (Commercial)	Ta	0		70	ºC
Ambient Operating Temperature (Industrial)	Ta	-40		85	ºC

10.3 DC Electrical Characteristics

Table 10-3. IT9500 DC electrical characteristics

Note: RF_VDD=3.3V, VDD1=1.2V, VCC3V=3.3V, AVDDHP=3.3V, and Ta=25 ºC unless otherwise specified.

Parameter	Symbol	Test Condition	Min.	Typ	Max.	Unit
High Level Input Voltage for 3.3v IO	VIH		2.0			V
Low Level Input Voltage for 3.3v IO	VIL				0.8	V
Input Capacitance	Cin			3		pF
Power Consumption (Operating, with internal voltage regulator)	P_{op}*	USB mode		380		mW
		MPEG-TS mode		350		mW
Power Consumption (Suspend, with internal voltage regulator)	P_{sus}	Suspend (USB)				mW
		Suspend (by GPIOH5)				
High Level Output Voltage for 3.3v IO	VOH		3.0			V
Low Level Output Voltage for 3.3v IO	VOL				0.4	V
High/Low Level Output Current	IOH/IOL	Digital Output Pins	0		4	mA
High/Low Level Output Current	IOH/IOL	5V tolerant Open-Drain	0		2	mA
Operation Current for 3.3V (include internal voltage regulator)		USB mode		115		mA
		MPEG-TS mode		105		mA
Operation Current for 1.4V				60		mA
Operation Current for 1.2V				30		mA

Note: *Test signal: Mode 3, 64QAM, Code Rate 7/8, GI 1/32 for DVB-T.

11. AC Characteristics

11.1 TS Input

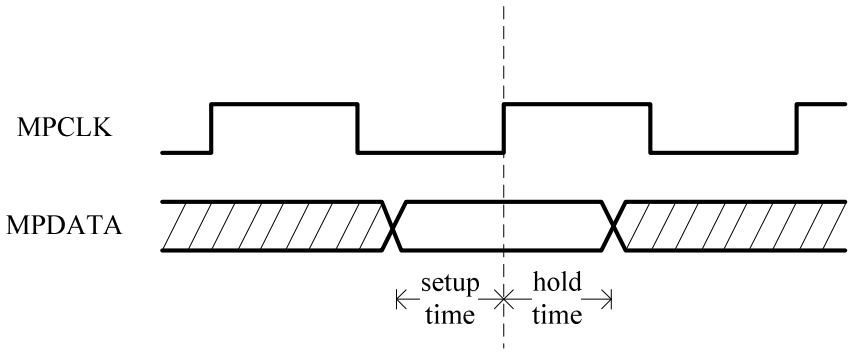


Figure 11-1. IT9500 TS input timing diagram

Table 11-1. IT9500 TS input timing

Parameter	Requirement	Unit
Input Set-up Time	8.29	ns
Input Hold Time	0.5	ns

11.2 2-Wire Bus Output Timing

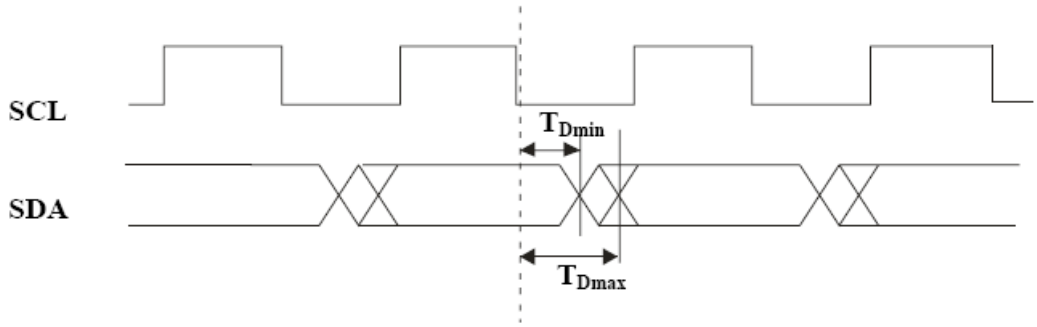


Figure 11-2. IT9500 2-wire bus output timing diagram.

Table 11-2. IT9500 2-wire bus output timing.

Parameter	Description	Min.	Max.	Unit
T_{Dmin}	Minimum valid delay of 2-wire bus output	T/2 + 2	NA	ns
T_{Dmax}	Maximum valid delay of 2-wire bus output	NA	T/2+6	ns

11.3 2-Wire Bus Input Timing

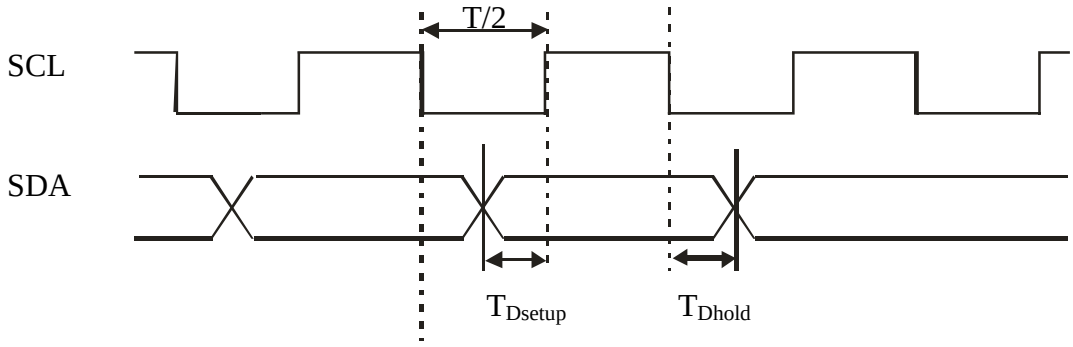


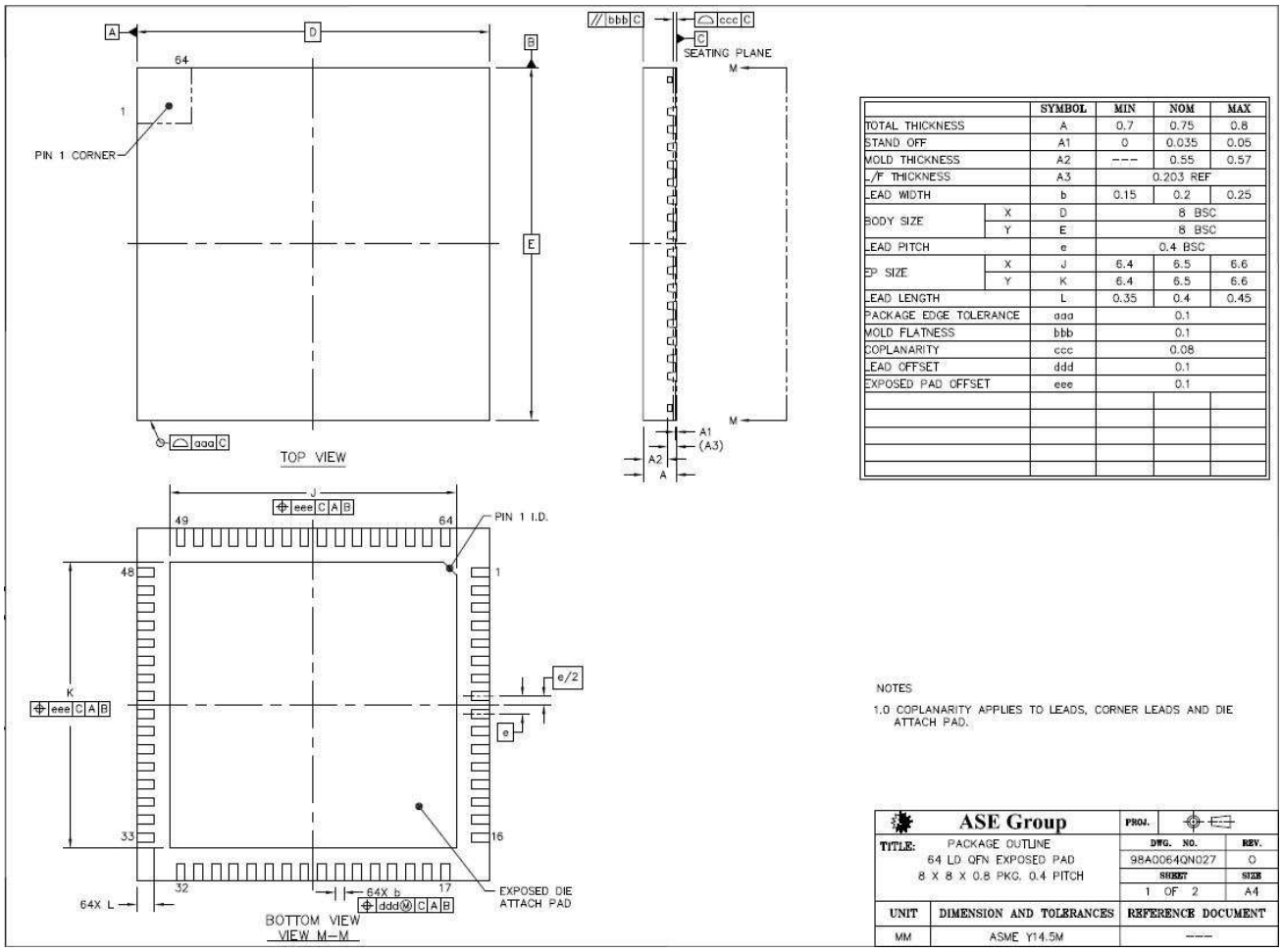
Figure 11-3. IT9500 2-wire bus input timing diagram.

Table 11-3. IT9500 2-wire bus input timing.

Parameter	Description	Min.	Max.	Unit
T_{Dsetup}	2-wire bus input setup time	2	T/2 -2	ns
T_{Dhold}	2-wire bus input hold time	2	T/2 -2	ns

12. Package Information

IT9507/9503FN – MQFN64



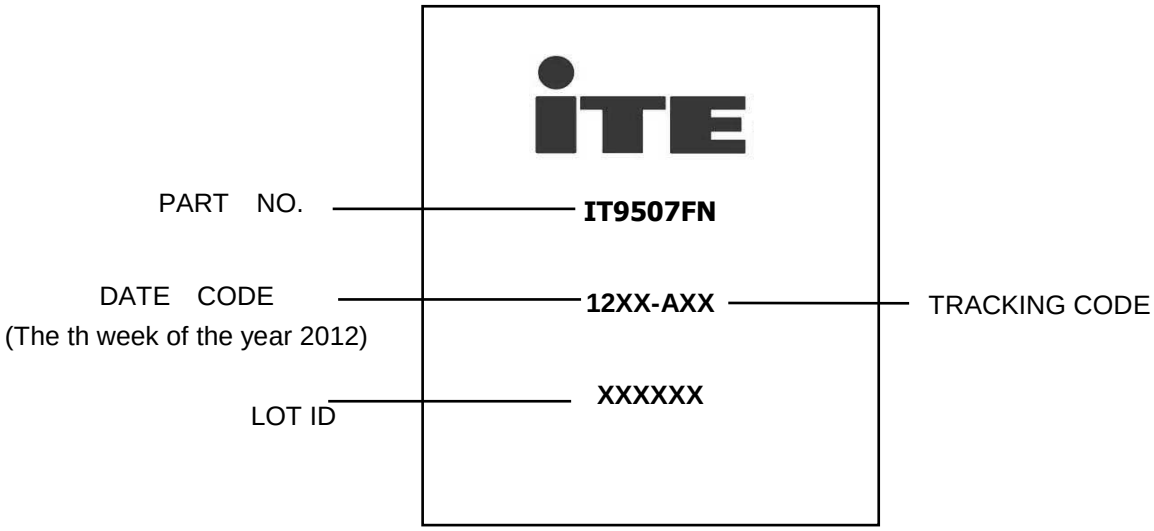
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	6.4	6.5	6.6
	Y	K	6.4	6.5	6.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

ASE Group		PROJ.	
TITLE: PACKAGE OUTLINE 64 LD QFN EXPOSED PAD 8 X 8 X 0.8 PKG, 0.4 PITCH		DWG. NO.	REV.
		98A0064QN027	O
		SHEET	SIZE
		1 OF 2	A4
UNIT	DIMENSION AND TOLERANCES	REFERENCE DOCUMENT	
MM	ASME Y14.5M	---	

13. Ordering Information

Part Number	Description	Package	Body Size
IT9507FN/AX	Commercial grade baseband transmitter for digital TV with USB and TS interfaces	64-pin MQFN	8mm × 8mm
IT9507FN-I/AX	Industrial specification of 9507	64-pin MQFN	8mm × 8mm
IT9503FN/AX	Commercial grade baseband transmitter for digital TV with USB and TS interfaces, Support QPSK/16QAM mode and guard Interval 1/4 & 1/8 only	64-pin MQFN	8mm × 8mm
IT9503FN-I/AX	Industrial specification of 9503	64-pin MQFN	8mm × 8mm

14. Top Marking Information



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