ITE 聯陽半導體 ITE Tech. Inc.

IT9917TE
IT9917TE-H / IT9919TE
IT9919TE-H / IT9919TE-N

High Performance A/V Encoder SOC

Specification V0.9.9.0

ITE TECH. INC.

This is a Preliminary document release. All specifications are subject to change without notice.
The material contained in this document supersedes all previous material issued for the products herein referenced. Please contact ITE Tech. Inc. for the latest document(s).

All sales are subject to ITE's Standard Terms and Conditions, a copy of which is included in the back of this document.

ITE, IT9919TE-H is a trademark of ITE Tech. Inc.
All other trademarks are claimed by their respective owners.
All specifications are subject to change without notice.

Additional copies of this manual or other ITE literature may be obtained from:

ITE Tech. Inc. Tel: 886-2-29126889
Marketing Department Fax: 886-2-2910-2551, 886-2-2910-2552
7F, No.233-1, Baociao Rd., Sindian City,
Taipei County 23145, Taiwan, ROC

You may also find the local sales representative nearest you on the ITE web site.

To find out more about ITE, visit our World Wide Web at:
http://www.ite.com.tw

Or e-mail itesupport@ite.com.tw for more product information/services

Revision History

Date	Revision	Page No.
-	Initial release.	-
2013/09/05	Modified table 4-30 and add table 4-31, 4-32 . Add power consumption table for recording YPbPr input.	26, 27, 60
2013/12/19	Add new IT9917 package	27, 35, 69
2014/04/15	Add new IT9917-H package	33, 36, 77

CONTENTS

FIGURES

TABLES

1. Features

- **Host Processor**
  - 200MHz 32-bit general purpose high performance RISC processor
  - Support separate 8K instruction and 8K data caches
  - DSP extension instruction for 32*32 MAC
  - Power saving

- **Audio Processor**
  - 200MHz 32-bit general purpose high performance RISC processor
  - Support separate 8K instruction and 8K data caches
  - DSP extension instruction for 32*32 MAC
  - Power saving
  - Support Audio Encoder
    - ADPCM
    - MPEG Audio
    - AAC-LC

- **Security Processor**
  - 200MHz 32-bit general purpose high performance RISC processor
  - Support separate 4K instruction and 8K data caches
  - DSP extension instruction for 32*32 MAC
  - Power saving

- **DMA Controller**
  - Provide 8 configurable DMA channels
  - Support chain transfer
  - Memory-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfer
  - Group round-robin arbitration scheme with 4 priority levels
  - Support 8-, 16-, and 32-bit wide data
  - Support big-endian and little-endian

- **Interrupt Controller**
  - Provides both edge and level-triggered interrupt sources with positive and negative directions
  - Provide de-bounce circuit for interrupt source

- **Timer with Pulse Width Modulation (PWM)**
  - Provide 2 independent 32-bit timer with PWM
  - Programmable duty cycle and frequency
  - Support external clock source
  - It can merge two timers as 64-bit timer
  - Support incrementing and decrementing mode

- **Remote Controller**
  - Hardware programmable to receive remote controller signal

- **General Purpose Input/output Ports**
  - Independent input, output and output enable buses for bi-directional I/O pins
  - Each port can separately trigger the GPIO interrupt when it programmed as input pin
  - Each port interrupt generation can be triggered by rising edge, falling edge, both edges, or high/low level when the interrupt option is set

- **UART**
  - Baud rate up to 6.25M bps
  - Firmware compatible with high-speed NS 16C550A UART
  - 128 bytes transmit/receive FIFOs
  - Internal diagnostic capabilities:
    - *Break, parity, overrun, framing error simulation for UART mode*

- **Watch Dog Timer**
  - During timeout, outputs are one or a combination of the following signals:
    - *System reset*
    - *System interrupt*
    - *External interrupt*
  - 32-bit down counter
  - A variable time-out period of reset
  - Access protection

- **IIC-Bus Interface**
  - Support stand, and fast mode through programming the clock division register
  - Support 7-bit, 10-bit and general call addressing mode

- Glitch suppression throughout the de-bounce circuit
- Programmable slave address
- Master-transmit, Master-receive, Slave-transmit and Slave-receive modes are provided
- Configurable multi-master mode supported
- Slave mode general call address detection

- **Synchronous Serial Port Controller**
  - Supports TI SSP, Motorola SPI, National Semiconductor Microwire
  - Supports master and slave modes
  - Internally or externally controlled serial bit clock
  - Internally or externally controlled frame/sync
  - Programmable frame/sync polarity
  - Programmable serial bit clock polarity, phase, and frequency
  - Programmable serial bit data sequence (MSB or LSB first)
  - Programmable threshold interrupt of transmit/receive FIFO
  - Independently programmable interrupt enable/disable
  - 16x32 transmit and receive data FIFO depth
  - Support 2nd SSP controller and include SPDIF function
    - SPDIF fully compliant with IEC958 standard
    - Support linear PCM and non-linear PCM (Compressed data)

- **USB Host/Device**
  - Provide one Host/Device controller, and one Host controller
  - Compliant with USB specification revision 2.0
  - Compatible with EHCI 1.0
  - Supports point-to-point communications with one HS/FS/LS device
  - Hardware configurable endpoints as HS/FS device
  - Both host and device support isochronous/ interrupt/ control/ bulk transfers
  - Compatible with EHCI data structures

- **Host Interface**
  - Supports addressing space up to 256MB
  - Supports SPI and IIC interface

- **Memory Interface**
  - Support maximum 256 MByte 16-bit DDR/DDR2
  - Support ping-pong bank with tilling memory access
  - Support different tilling mode

- **Ethernet MAC**
  - Compliant with the full IEEE 802.3-2002 specifications
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support of CSMA/CD Protocol for Half-Duplex operation
  - Supports IEEE 802.3x flow-control for Full-Duplex operation
  - Supports IEEE 1588-2002 Time stamping on the transmit and received frames
  - IEEE 802.3 compliant RMII PHY interface

- **Video Input Interface**
  - Support 24/30/36-bit RGB/YCbCr
  - Support BT601 : 16/20/24-bit YCbCr 4:2:2
  - Support BT656 : 8/10/12-bit YCbCr 4:2:2
  - Support HD BT1120 interface
  - BT656 like time multiplexed input with 54/108/144 MHz
  - Down sampling from YCbCr 4:4:4 to YCbCr 4:2:2 or 4:2:0
  - Dithering for conversion from 12-bit/10-bit component to 8-bit

- **Image Signal Processing**
  - Image and video scaling engine for scaling up and down
    - *4-Tap scaling filter*
    - *Configurable filter coefficients*
  - Color space conversion
  - De-interlace filter
    - *2D deinterlace filter*
    - *3D deinterlace filter*
  - High Color OSD

- **Audio Input Interface**

- Up to Four I2S interface, with sample rates of 32~192KHz and sample sizes of 16~24 bits
- SPDIF interface supporting PCM and non-PCM data

■ **H.264/AVC Encoder**
- Support Baseline profile, from level 1.0~ 4.0 up to 1080p@30fps
- Support CBR and VBR
- Programmable GOP structure

■ **JPEG Encoder**
- Compliant with Baseline JPEG standard ISO/IEC 10918
- Support 5M pixel still image encode
- Support 1080p@30fps Motion JPEG encode

■ **HDMI Receiver**
- Single-link HDMI 1.4 receiver
- Compliant with HDMI 1.3, HDCP 1.4 and DVI 1.0 specifications
- Integrated pre-programmed HDCP keys

■ **Cypher Engine**
- Compliant with the Publication 197 from NIST (AES) encryption/decryption with 128-bit key size
- Support DES/3DES encryption/decryption
- Support DVB-CSA decryption
- Support ECB, CBC, CFB, CTR and OFB operation mode
- Support RSA1024
- Support SHA256
- Support scrambler

■ **SD/MMC Controller**
- Two MMC/SD interface
- Fully compliant with MMCA v3.3
- Compliant with low-voltage support and 4 bits data of MMCA v4.0
- Compliant with SD/SDHC
- FAT16/FAT32 boot loader

■ **TSI**
- Support serial interface
- 32 PID filters
- Maximum bits rate up to 100 Mbits

■ **TSO**
- Support serial interface
- PCR Insertion
- Maximum bits rate up to 80 Mbits

■ **Boot Loader**
- Configurable booting device
- Serial NOR
- SD Card
- Co-operative mode
  - *SPI*
  - *IIC*
- Support de-compressed boot code

This page is intentionally left blank.

2. General Description

2.1 Introduction

IT9910 is a real-time and high performance A/V encoder SOC. It integrates a high performance H.264 Encoder, JPEG encoder, Audio encoder, 32-bit RISC CPU, USB, SD, Cypher Engine and versatile A/V input interfaces. It's easy to enable high quality and high performance video/audio recording.

IT9919 integrates 512Mbits DRAM in package to offer a small size, thus can help customer to design small size PCB board and also to shorten PCB board development cycle.

2.2 Multimedia Processor

2.2.1 Powerful Video Encoding Engine

IT9910 supports H.264 and JPEG encoder and encodes up to Full-HD 1920x1080 resolution. H.264 encoder is fully complies with ISO/IEC-14996-10 baseline profile. JPEG encoder is fully complies with ISO/IEC-10918 baseline profile. IT9919 also provides a video scaling engine for scaling up or down to the target encoding size.

2.2.2 Powerful Audio Encoding Solution

IT9910 embeds a 32-bit RISC CPU and a DSP engine. It can encode ADPCM, MPEG-1 and MPEG-2 layer 2 audio and AAC-LC streams.

2.2.3 High performance USB2.0 I/F

IT9910 supports a USB2.0 Host and a USB2.0 Device I/Fs. Users can have high speed data transfer experience through the USB2.0 I/F.

2.2.4 Flexible Storage Interface

IT9910 has MMC/SD cards I/F and NOR flash I/F. You can choose MMC/SD for multimedia contents storage space. If you want some other external cards I/F, IT9910 provides a USB host I/F allowing for an external card bus chip. Besides NOR and SD are the others solution for you to choose as a booting code storage space.

2.2.5 A/V Input Interface

IT9910 can accept BT.656, BT1120 and YCbCr 4:2:2 8/16 bits with separate H/V sync video. It is flexible to connect various external video A/D converters. The maximum resolution is up to 1920x1080.

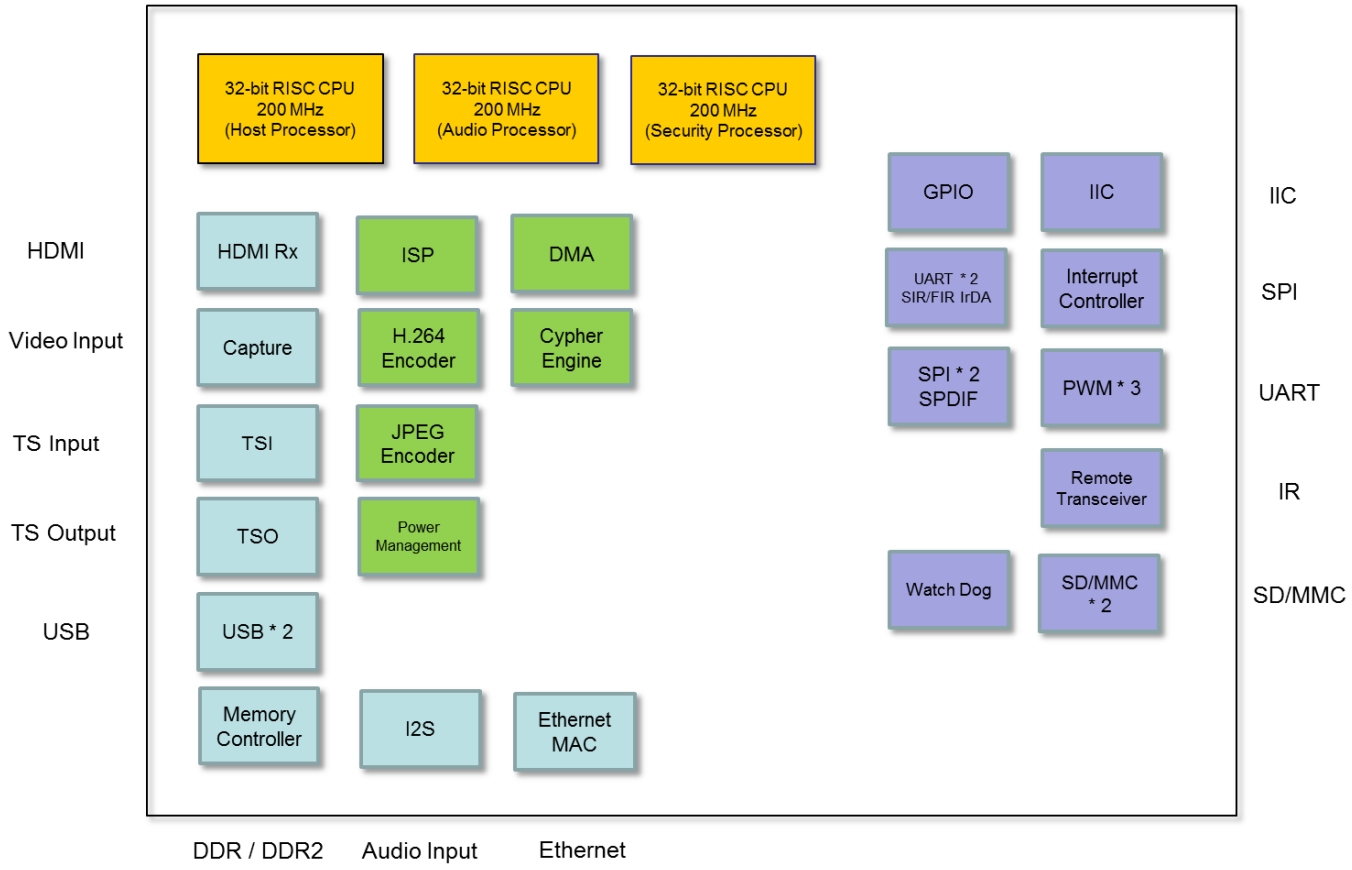
IT9910 supports I2S controller that can connect to various external A/D converters and can be configured as either master or slave mode..IT9919 also provides SPDIF interface supporting PCM and non-PCM data.

2.2.6 HDMI Receiver

The IT9919-H also provides high-performance and low-power single link HDMI receiver, fully compliant with HDMI 1.3, compliant HDMI 1.4a and HDCP 1.4 compliance and also backward compatible to DVI 1.0 specifications. IT9919-H can bypass HDMI digital signals and connect to external HDMI transmitter to achieve loop through function.

3. Block Diagram

Figure 3-1. Block Diagram of IT9910 Series



This page is intentionally left blank

4. Pin Configuration / Description

4.1 IT9919-H Pin Location

Figure 4-1. Pin Location of IT9919-H

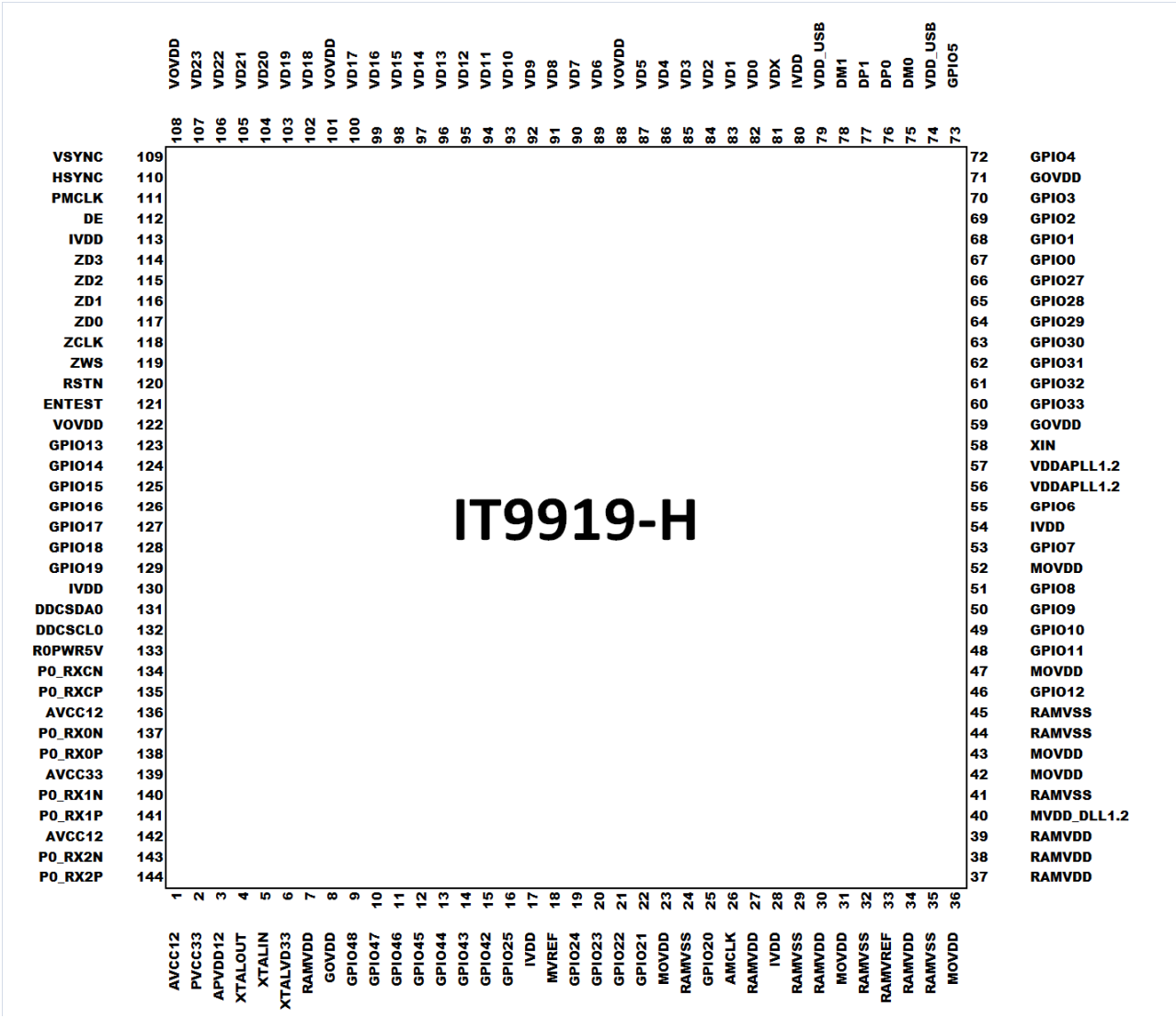


Table 4-1. Pins Listed in Numeric Order for IT9919-H

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AVCC12	37	RAMVDD	73	GPIO5	109	VSYNC
2	PVCC33	38	RAMVDD	74	VDD_USB	110	HSYNC
3	APVDD12	39	RAMVDD	75	DM0	111	PMCLK
4	XTALOUT	40	MVDD_DLL1.2	76	DP0	112	DE
5	XTALIN	41	RAMVSS	77	DP1	113	IVDD
6	XTALVD33	42	MOVDD	78	DM1	114	ZD3
7	RAMVDD	43	MOVDD	79	VDD_USB	115	ZD2
8	GOVDD	44	RAMVSS	80	IVDD	116	ZD1
9	GPIO48	45	RAMVSS	81	VDX	117	ZD0
10	GPIO47	46	GPIO12	82	VD0	118	ZCLK
11	GPIO46	47	MOVDD	83	VD1	119	ZWS
12	GPIO45	48	GPIO11	84	VD2	120	RSTN
13	GPIO44	49	GPIO10	85	VD3	121	ENTEST
14	GPIO43	50	GPIO9	86	VD4	122	VOVDD
15	GPIO42	51	GPIO8	87	VD5	123	GPIO13
16	GPIO25	52	MOVDD	88	VOVDD	124	GPIO14
17	IVDD	53	GPIO7	89	VD6	125	GPIO15
18	MVREF	54	IVDD	90	VD7	126	GPIO16
19	GPIO24	55	GPIO6	91	VD8	127	GPIO17
20	GPIO23	56	VDDAPLL1.2	92	VD9	128	GPIO18
21	GPIO22	57	VDDAPLL1.2	93	VD10	129	GPIO19
22	GPIO21	58	XIN	94	VD11	130	IVDD
23	MOVDD	59	GOVDD	95	VD12	131	DDCSDA0
24	RAMVSS	60	GPIO33	96	VD13	132	DDCSCL0
25	GPIO20	61	GPIO32	97	VD14	133	R0PWR5V
26	AMCLK	62	GPIO31	98	VD15	134	P0_RXCN
27	RAMVDD	63	GPIO30	99	VD16	135	P0_RXCP
28	IVDD	64	GPIO29	100	VD17	136	AVCC12
29	RAMVSS	65	GPIO28	101	VOVDD	137	P0_RX0N
30	RAMVDD	66	GPIO27	102	VD18	138	P0_RX0P
31	MOVDD	67	GPIO0	103	VD19	139	AVCC33
32	RAMVSS	68	GPIO1	104	VD20	140	P0_RX1N
33	RAMVREF	69	GPIO2	105	VD21	141	P0_RX1P
34	RAMVDD	70	GPIO3	106	VD22	142	AVCC12
35	RAMVSS	71	GOVDD	107	VD23	143	P0_RX2N
36	MOVDD	72	GPIO4	108	VOVDD	144	P0_RX2P

Table 4-2. Pins Listed in Alphabetical Order for IT9919-H

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AMCLK	26	GPIO19	129	MVREF	18	VD8	91
APVDD12	3	GPIO20	25	P0_RX0N	137	VD9	92
AVCC12	1	GPIO21	22	P0_RX0P	138	VD10	93
AVCC12	136	GPIO22	21	P0_RX1N	140	VD11	94
AVCC12	142	GPIO23	20	P0_RX1P	141	VD12	95
AVCC33	139	GPIO24	19	P0_RX2N	143	VD13	96
DM0	75	GPIO25	16	P0_RX2P	144	VD14	97
DP0	76	GPIO27	66	P0_RXCN	134	VD15	98
DP1	77	GPIO28	65	P0_RXCP	135	VD16	99
DM1	78	GPIO29	64	PMCLK	111	VD17	100
DE	112	GPIO30	63	PVCC33	2	VD18	102
DDCSDA0	131	GPIO31	62	R0PWR5V	133	VD19	103
DDCSCL0	132	GPIO32	61	RAMVDD	7	VD20	104
ENTEST	121	GPIO33	60	RAMVDD	27	VD21	105
GOVDD	8	GPIO42	15	RAMVDD	30	VD22	106
GOVDD	59	GPIO43	14	RAMVDD	34	VD23	107
GOVDD	71	GPIO44	13	RAMVDD	37	VDX	81
GPIO0	67	GPIO45	12	RAMVDD	38	VDDAPLL1.2	56
GPIO1	68	GPIO46	11	RAMVDD	39	VDDAPLL1.2	57
GPIO2	69	GPIO47	10	RAMVREF	33	VDD_USB	74
GPIO3	70	GPIO48	9	RAMVSS	24	VDD_USB	79
GPIO4	72	HSYNC	110	RAMVSS	29	VOVDD	88
GPIO5	73	IVDD	17	RAMVSS	32	VOVDD	101
GPIO6	55	IVDD	28	RAMVSS	35	VOVDD	108
GPIO7	53	IVDD	54	RAMVSS	41	VOVDD	122
GPIO8	51	IVDD	80	RAMVSS	44	VSYNC	109
GPIO9	50	IVDD	113	RAMVSS	45	XIN	58
GPIO10	49	IVDD	130	RSTN	120	XTALIN	5
GPIO11	48	MOVDD	23	VD0	82	XTALOUT	4
GPIO12	46	MOVDD	31	VD1	83	XTALVD33	6
GPIO13	123	MOVDD	36	VD2	84	ZCLK	118
GPIO14	124	MOVDD	42	VD3	85	ZD0	117
GPIO15	125	MOVDD	43	VD4	86	ZD1	116
GPIO16	126	MOVDD	47	VD5	87	ZD2	115
GPIO17	127	MOVDD	52	VD6	89	ZD3	114
GPIO18	128	MVDD_DLL1.2	40	VD7	90	ZWS	119

4.2 IT9919-H Pin Description

Table 4-3. IT9919-H Pin Description for Video Interface

Pin(s) No.	Symbol	Attribute	Description
111	PMCLK	O	Output pixel clock
110	HSYNC	I/O	Horizontal sync. signal
109	VSYNC	I/O	Vertical sync. signal
112	DE	I/O	Data enable
81	VDX	I/O	Video clock and data swap is supported by register setting.
107, 106, 105, 104, 103, 102, 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85, 84, 83, 82	VD[23:0]	I/O	Video clock and data swap is supported by register setting.

Output direction is for HDMI loop through.

Table 4-4. IT9919-H Pin Description for Audio Interface

Pin(s) No.	Symbol	Attribute	Description
26	AMCLK	I/O	Audio master clock
118	ZCLK	I/O	I2S serial clock
119	ZWS	I/O	I2S word select
114, 115, 116, 117	ZD[3:0]	I/O	I2S serial data

Output direction is for HDMI loop through.
Please see table 4-52 for Audio pin share.

Table 4-5. IT9919-H Pin Description for USB Interface

Pin(s) No.	Symbol	Attribute	Description
74, 79	VDD_USB	P	Analog supply voltage. 3.3V typical
76	DP0	I/O	Data Pins USB data in data positive pin terminal
75	DM0	I/O	Data Pins USB data in data negative pin terminal
77	DP1	I/O	Data Pins USB data in data positive pin terminal
78	DM1	I/O	Data Pins USB data in data negative pin terminal

Table 4-6. IT9919-H Pin Description for HDMI Interface

Pin(s) No.	Symbol	Attribute	Description
133	R0PWR5V	I	TMDS transmitter detection (5V-tolerant)
131	DDCSDA0	I/O	DDC I2C Data for HDMI Port (5V-tolerant)
132	DDCSCL0	I/O	DDC I2C Clock for HDMI Port (5V-tolerant)
137	P0_RX0N	I	HDMI Channel 0 negative input for HDMI Port
138	P0_RX0P	I	HDMI Channel 0 positive input for HDMI Port
140	P0_RX1N	I	HDMI Channel 1 negative input for HDMI Port
141	P0_RX1P	I	HDMI Channel 1 positive input for HDMI Port
143	P0_RX2N	I	HDMI Channel 2 negative input for HDMI Port
144	P0_RX2P	I	HDMI Channel 2 positive input for HDMI Port
134	P0_RXCN	I	HDMI Clock Channel negative input for HDMI Port
135	P0_RXCP	I	HDMI Clock Channel positive input for HDMI Port

Pin(s) No.	Symbol	Attribute	Description
5	XTALIN	I	Crystal clock input (for Audio PLL)
4	XTALOUT	O	Crystal clock output (for Audio PLL)
3	APVDD12	P	HDMI audio PLL power (1.35V)
1, 136, 142	AVCC12	P	HDMI analog frontend power (1.35V)
139	AVCC33	P	HDMI analog frontend power (3.3V)
2	PVCC33	P	HDMI receiver PLL power (3.3V)
6	XTALVD33	P	Power for crystal oscillator (3.3V)

Table 4-7. IT9919-H Pin Description for GPIO Interface

Pin(s) No.	Symbol	Attribute	Description
67	GPIO0	I/O	GPIO0
68	GPIO1	I/O	GPIO1
69	GPIO2	I/O	GPIO2
70	GPIO3	I/O	GPIO3
72	GPIO4	I/O	GPIO4
73	GPIO5	I/O	GPIO5
55	GPIO6	I/O	GPIO6
53	GPIO7	I/O	GPIO7
51	GPIO8	I/O	GPIO8
50	GPIO9	I/O	GPIO9
49	GPIO10	I/O	GPIO10
48	GPIO11	I/O	GPIO11
46	GPIO12	I/O	GPIO12
123	GPIO13	I/O	GPIO13
124	GPIO14	I/O	GPIO14
125	GPIO15	I/O	GPIO15
126	GPIO16	I/O	GPIO16
127	GPIO17	I/O	GPIO17
128	GPIO18	I/O	GPIO18
129	GPIO19	I/O	GPIO19
25	GPIO20	I/O	GPIO20
22	GPIO21	I/O	GPIO21
21	GPIO22	I/O	GPIO22
20	GPIO23	I/O	GPIO23
19	GPIO24	I/O	GPIO24
16	GPIO25	I/O	GPIO25
66	GPIO27	I/O	GPIO27
65	GPIO28	I/O	GPIO28
64	GPIO29	I/O	GPIO29
63	GPIO30	I/O	GPIO30
62	GPIO31	I/O	GPIO31
61	GPIO32	I/O	GPIO32
60	GPIO33	I/O	GPIO33
15	GPIO42	I/O	GPIO42
14	GPIO43	I/O	GPIO43
13	GPIO44	I/O	GPIO44
12	GPIO45	I/O	GPIO45
11	GPIO46	I/O	GPIO46
10	GPIO47	I/O	GPIO47
9	GPIO48	I/O	GPIO48

Please see table 4-49 for GPIO pin share.

Table 4-8. IT9919-H Pin Description for Memory Interface

Pin(s) No.	Symbol	Attribute	Description
23, 31, 36, 42, 43, 47, 52	MOVDD	P	Memory Supply 1.8 V
18	MVREFF	P	Memory Reference voltage (1/2 * MOVDD)
40	MVDD_DLL1.2	P	Memory DLL Supply 1.35 V
7, 27, 30, 34, 37, 38, 39	RAMVDD	P	Internal Stack Memory Supply 1.8 V
24, 29, 32, 35, 41, 44, 45	RAMVSS	P	Internal Stack Memory Ground
33	RAMVREF	P	Internal Stack Memory Reference voltage (1/2 * RAMVDD)

Table 4-9. IT9919-H Pin Description for Misc. Interface

Pin(s) No.	Symbol	Attribute	Description
121	ENTEST	I	Test Enable
120	RSTN	I	Reset
56, 57	VDDAPLL1.2	P	Crystal Supply 1.35V
58	XIN	I	Crystal 12MHz Input

Table 4-10. IT9919 Pin Description for Power/Ground Signal

Pin(s) No.	Symbol	Attribute	Description
17, 28, 54, 80, 113, 130	IVDD	P	Digital Core supply 1.35V
8, 59, 71	GOVDD	P	I/O Supply 3.3V
88, 101, 108, 122	VOVDD	P	I/O Supply 3.3V

4.3 IT9919-N Pin Location

Figure 4-2. Pin Location of IT9919-N

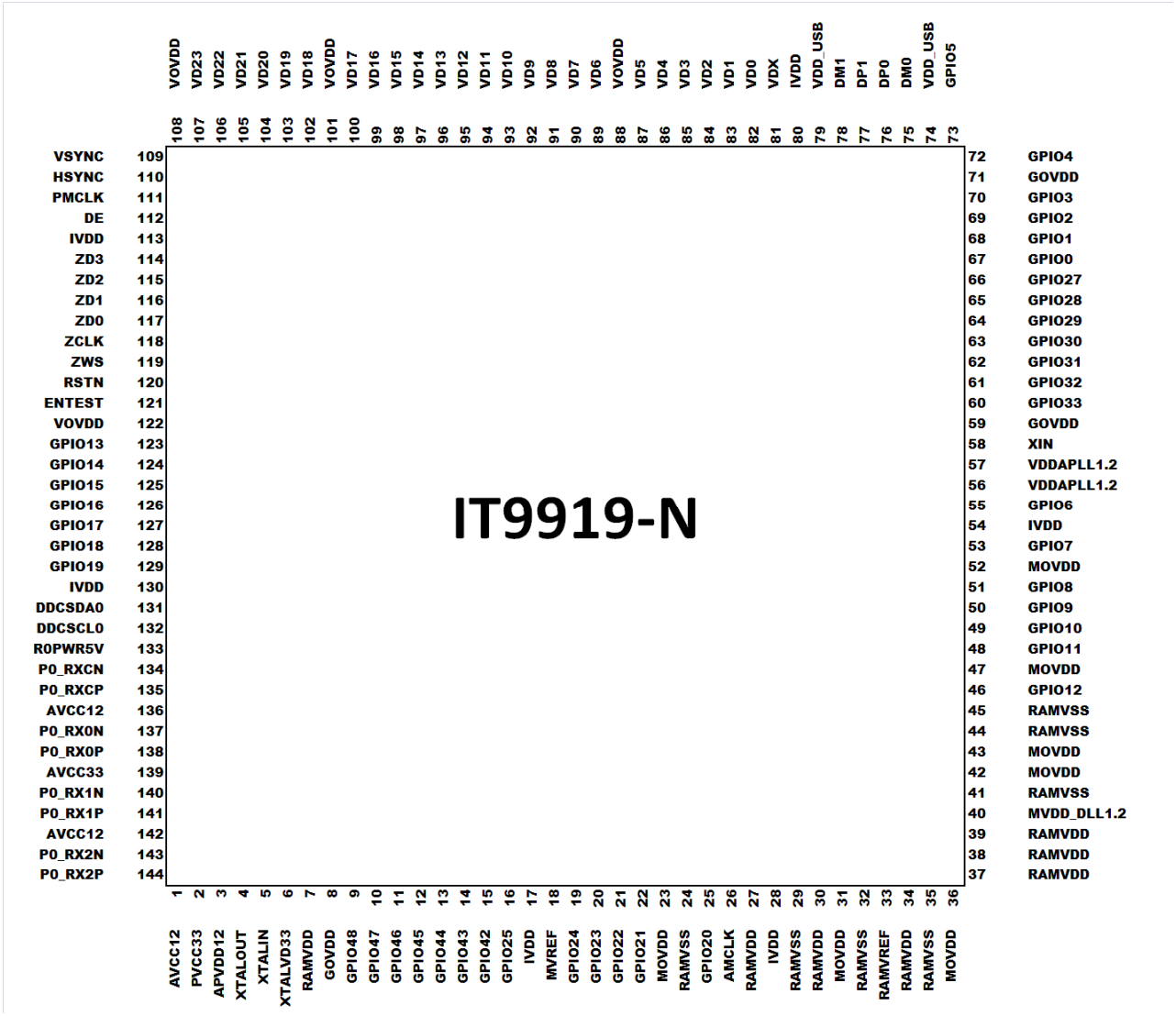


Table 4-21. Pins Listed in Numeric Order for IT9919-N

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AVCC12	37	RAMVDD	73	GPIO5	109	VSYNC
2	PVCC33	38	RAMVDD	74	VDD_USB	110	HSYNC
3	APVDD12	39	RAMVDD	75	DM0	111	PMCLK
4	XTALOUT	40	MVDD_DLL1.2	76	DP0	112	DE
5	XTALIN	41	RAMVSS	77	DP1	113	IVDD
6	XTALVD33	42	MOVDD	78	DM1	114	ZD3
7	RAMVDD	43	MOVDD	79	VDD_USB	115	ZD2
8	GOVDD	44	RAMVSS	80	IVDD	116	ZD1
9	GPIO48	45	RAMVSS	81	VDX	117	ZD0
10	GPIO47	46	GPIO12	82	VD0	118	ZCLK
11	GPIO46	47	MOVDD	83	VD1	119	ZWS
12	GPIO45	48	GPIO11	84	VD2	120	RSTN
13	GPIO44	49	GPIO10	85	VD3	121	ENTEST
14	GPIO43	50	GPIO9	86	VD4	122	VOVDD
15	GPIO42	51	GPIO8	87	VD5	123	GPIO13
16	GPIO25	52	MOVDD	88	VOVDD	124	GPIO14
17	IVDD	53	GPIO7	89	VD6	125	GPIO15
18	MVREF	54	IVDD	90	VD7	126	GPIO16
19	GPIO24	55	GPIO6	91	VD8	127	GPIO17
20	GPIO23	56	VDDAPLL1.2	92	VD9	128	GPIO18
21	GPIO22	57	VDDAPLL1.2	93	VD10	129	GPIO19
22	GPIO21	58	XIN	94	VD11	130	IVDD
23	MOVDD	59	GOVDD	95	VD12	131	DDCSDA0
24	RAMVSS	60	GPIO33	96	VD13	132	DDCSCL0
25	GPIO20	61	GPIO32	97	VD14	133	R0PWR5V
26	AMCLK	62	GPIO31	98	VD15	134	P0_RXCN
27	RAMVDD	63	GPIO30	99	VD16	135	P0_RXCP
28	IVDD	64	GPIO29	100	VD17	136	AVCC12
29	RAMVSS	65	GPIO28	101	VOVDD	137	P0_RX0N
30	RAMVDD	66	GPIO27	102	VD18	138	P0_RX0P
31	MOVDD	67	GPIO0	103	VD19	139	AVCC33
32	RAMVSS	68	GPIO1	104	VD20	140	P0_RX1N
33	RAMVREF	69	GPIO2	105	VD21	141	P0_RX1P
34	RAMVDD	70	GPIO3	106	VD22	142	AVCC12
35	RAMVSS	71	GOVDD	107	VD23	143	P0_RX2N
36	MOVDD	72	GPIO4	108	VOVDD	144	P0_RX2P

Table 4-12. Pins Listed in Alphabetical Order for IT9919-N

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AMCLK	26	GPIO19	129	MVREF	18	VD8	91
APVDD12	3	GPIO20	25	P0_RX0N	137	VD9	92
AVCC12	1	GPIO21	22	P0_RX0P	138	VD10	93
AVCC12	136	GPIO22	21	P0_RX1N	140	VD11	94
AVCC12	142	GPIO23	20	P0_RX1P	141	VD12	95
AVCC33	139	GPIO24	19	P0_RX2N	143	VD13	96
DM0	75	GPIO25	16	P0_RX2P	144	VD14	97
DP0	76	GPIO27	66	P0_RXCN	134	VD15	98
DP1	77	GPIO28	65	P0_RXCP	135	VD16	99
DM1	78	GPIO29	64	PMCLK	111	VD17	100
DE	112	GPIO30	63	PVCC33	2	VD18	102
DDCSDA0	131	GPIO31	62	R0PWR5V	133	VD19	103
DDCSCL0	132	GPIO32	61	RAMVDD	7	VD20	104
ENTEST	121	GPIO33	60	RAMVDD	27	VD21	105
GOVDD	8	GPIO42	15	RAMVDD	30	VD22	106
GOVDD	59	GPIO43	14	RAMVDD	34	VD23	107
GOVDD	71	GPIO44	13	RAMVDD	37	VDX	81
GPIO0	67	GPIO45	12	RAMVDD	38	VDDAPLL1.2	56
GPIO1	68	GPIO46	11	RAMVDD	39	VDDAPLL1.2	57
GPIO2	69	GPIO47	10	RAMVREF	33	VDD_USB	74
GPIO3	70	GPIO48	9	RAMVSS	24	VDD_USB	79
GPIO4	72	HSYNC	110	RAMVSS	29	VOVDD	88
GPIO5	73	IVDD	17	RAMVSS	32	VOVDD	101
GPIO6	55	IVDD	28	RAMVSS	35	VOVDD	108
GPIO7	53	IVDD	54	RAMVSS	41	VOVDD	122
GPIO8	51	IVDD	80	RAMVSS	44	VSYNC	109
GPIO9	50	IVDD	113	RAMVSS	45	XIN	58
GPIO10	49	IVDD	130	RSTN	120	XTALIN	5
GPIO11	48	MOVDD	23	VD0	82	XTALOUT	4
GPIO12	46	MOVDD	31	VD1	83	XTALVD33	6
GPIO13	123	MOVDD	36	VD2	84	ZCLK	118
GPIO14	124	MOVDD	42	VD3	85	ZD0	117
GPIO15	125	MOVDD	43	VD4	86	ZD1	116
GPIO16	126	MOVDD	47	VD5	87	ZD2	115
GPIO17	127	MOVDD	52	VD6	89	ZD3	114
GPIO18	128	MVDD_DLL1.2	40	VD7	90	ZWS	119

4.4 IT9919-N Pin Description

Table 4-13. IT9919-N Pin Description for Video Interface

Pin(s) No.	Symbol	Attribute	Description
111	PMCLK	O	Output pixel clock
110	HSYNC	I/O	Horizontal sync. signal
109	VSYNC	I/O	Vertical sync. signal
112	DE	I/O	Data enable
81	VDX	I/O	Video clock and data swap is supported by register setting.
107, 106, 105, 104, 103, 102, 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85, 84, 83, 82	VD[23:0]	I/O	Video clock and data swap is supported by register setting.

Output direction is for HDMI loop through.

Table 4-14. IT9919-N Pin Description for Audio Interface

Pin(s) No.	Symbol	Attribute	Description
26	AMCLK	I/O	Audio master clock
118	ZCLK	I/O	I2S serial clock
119	ZWS	I/O	I2S word select
114, 115, 116, 117	ZD[3:0]	I/O	I2S serial data

Output direction is for HDMI loop through.
Please see table 4-52 for Audio pin share.

Table 4-15. IT9919-N Pin Description for USB Interface

Pin(s) No.	Symbol	Attribute	Description
74, 79	VDD_USB	P	Analog supply voltage. 3.3V typical
76	DP0	I/O	Data Pins USB data in data positive pin terminal
75	DM0	I/O	Data Pins USB data in data negative pin terminal
77	DP1	I/O	Data Pins USB data in data positive pin terminal
78	DM1	I/O	Data Pins USB data in data negative pin terminal

Table 4-16. IT9919-N Pin Description for HDMI Interface

Pin(s) No.	Symbol	Attribute	Description
133	R0PWR5V	I	TMDS transmitter detection (5V-tolerant)
131	DDCSDA0	I/O	DDC I2C Data for HDMI Port (5V-tolerant)
132	DDCSCL0	I/O	DDC I2C Clock for HDMI Port (5V-tolerant)
137	P0_RX0N	I	HDMI Channel 0 negative input for HDMI Port
138	P0_RX0P	I	HDMI Channel 0 positive input for HDMI Port
140	P0_RX1N	I	HDMI Channel 1 negative input for HDMI Port
141	P0_RX1P	I	HDMI Channel 1 positive input for HDMI Port
143	P0_RX2N	I	HDMI Channel 2 negative input for HDMI Port
144	P0_RX2P	I	HDMI Channel 2 positive input for HDMI Port
134	P0_RXCN	I	HDMI Clock Channel negative input for HDMI Port
135	P0_RXCP	I	HDMI Clock Channel positive input for HDMI Port

Pin(s) No.	Symbol	Attribute	Description
5	XTALIN	I	Crystal clock input (for Audio PLL)
4	XTALOUT	O	Crystal clock output (for Audio PLL)
3	APVDD12	P	HDMI audio PLL power (1.35V)
1, 136, 142	AVCC12	P	HDMI analog frontend power (1.35V)
139	AVCC33	P	HDMI analog frontend power (3.3V)
2	PVCC33	P	HDMI receiver PLL power (3.3V)
6	XTALVD33	P	Power for crystal oscillator (3.3V)

Table 4-17. IT9919-N Pin Description for GPIO Interface

Pin(s) No.	Symbol	Attribute	Description
67	GPIO0	I/O	GPIO0
68	GPIO1	I/O	GPIO1
69	GPIO2	I/O	GPIO2
70	GPIO3	I/O	GPIO3
72	GPIO4	I/O	GPIO4
73	GPIO5	I/O	GPIO5
55	GPIO6	I/O	GPIO6
53	GPIO7	I/O	GPIO7
51	GPIO8	I/O	GPIO8
50	GPIO9	I/O	GPIO9
49	GPIO10	I/O	GPIO10
48	GPIO11	I/O	GPIO11
46	GPIO12	I/O	GPIO12
123	GPIO13	I/O	GPIO13
124	GPIO14	I/O	GPIO14
125	GPIO15	I/O	GPIO15
126	GPIO16	I/O	GPIO16
127	GPIO17	I/O	GPIO17
128	GPIO18	I/O	GPIO18
129	GPIO19	I/O	GPIO19
25	GPIO20	I/O	GPIO20
22	GPIO21	I/O	GPIO21
21	GPIO22	I/O	GPIO22
20	GPIO23	I/O	GPIO23
19	GPIO24	I/O	GPIO24
16	GPIO25	I/O	GPIO25
66	GPIO27	I/O	GPIO27
65	GPIO28	I/O	GPIO28
64	GPIO29	I/O	GPIO29
63	GPIO30	I/O	GPIO30
62	GPIO31	I/O	GPIO31
61	GPIO32	I/O	GPIO32
60	GPIO33	I/O	GPIO33
15	GPIO42	I/O	GPIO42
14	GPIO43	I/O	GPIO43
13	GPIO44	I/O	GPIO44
12	GPIO45	I/O	GPIO45
11	GPIO46	I/O	GPIO46
10	GPIO47	I/O	GPIO47
9	GPIO48	I/O	GPIO48

Please see table 4-49 for GPIO pin share.

Table 4-18. IT9919-N Pin Description for Memory Interface

Pin(s) No.	Symbol	Attribute	Description
23, 31, 36, 42, 43, 47, 52	MOVDD	P	Memory Supply 1.8 V
18	MVREFF	P	Memory Reference voltage (1/2 * MOVDD)
40	MVDD_DLL1.2	P	Memory DLL Supply 1.35V
7, 27, 30, 34, 37, 38, 39	RAMVDD	P	Internal Stack Memory Supply 1.8 V
24, 29, 32, 35, 41, 44, 45	RAMVSS	P	Internal Stack Memory Ground
33	RAMVREF	P	Internal Stack Memory Reference voltage (1/2 * RAMVDD)

Table 4-19. IT9919-N Pin Description for Misc. Interface

Pin(s) No.	Symbol	Attribute	Description
121	ENTEST	I	Test Enable
120	RSTN	I	Reset
56, 57	VDDAPLL1.2	P	Crystal Supply 1.35V
58	XIN	I	Crystal 12MHz Input

Table 4-20. IT9919-N Pin Description for Power/Ground Signal

Pin(s) No.	Symbol	Attribute	Description
17, 28, 54, 80, 113, 130	IVDD	P	Digital Core supply 1.35V
8, 59, 71	GOVDD	P	I/O Supply 3.3V
88, 101, 108, 122	VOVDD	P	I/O Supply 3.3V

4.5 IT9919 Pin Location

Figure 4-3. Pin Location of IT9919

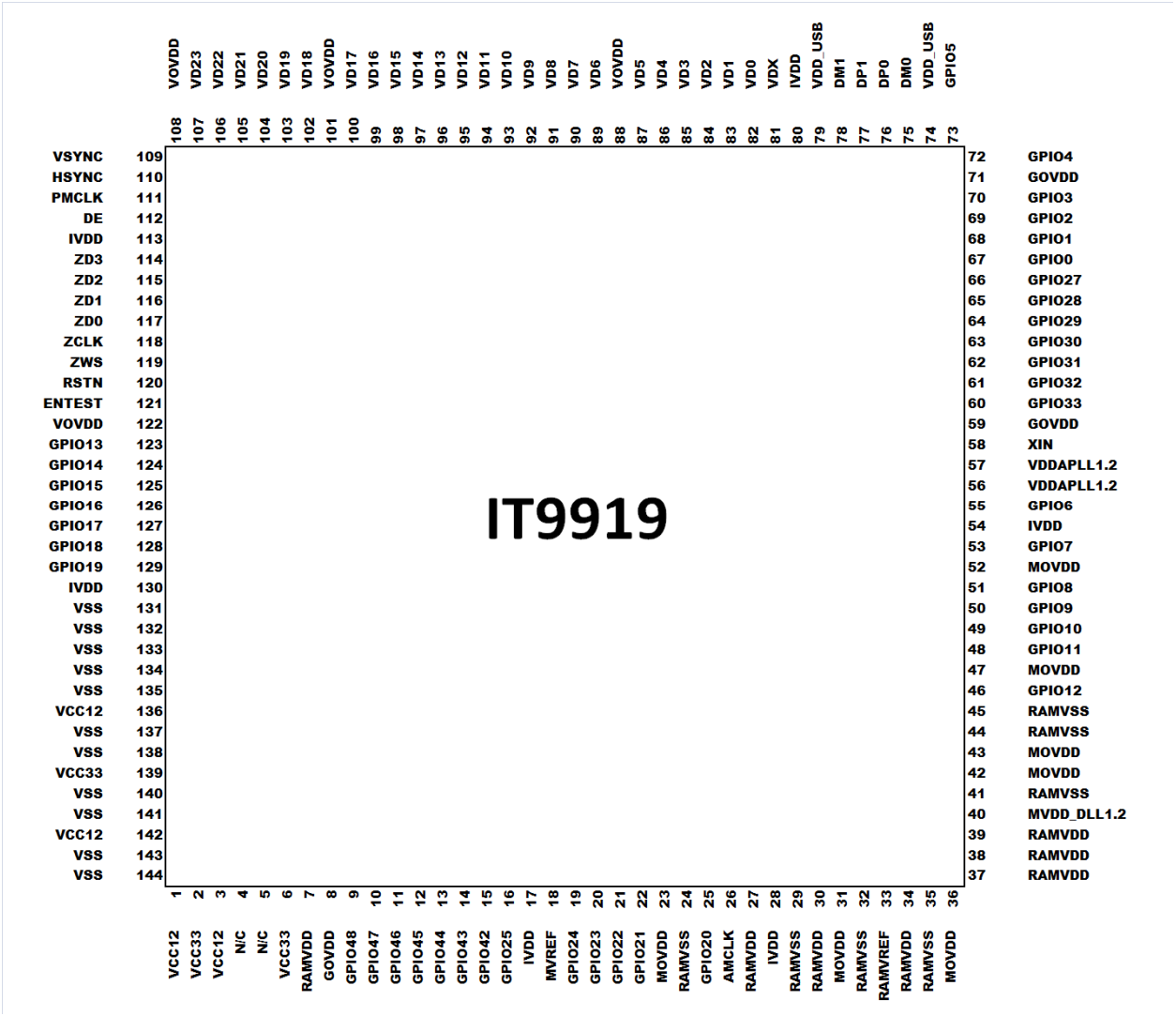


Table 4-21. Pins Listed in Numeric Order for IT9919

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC12	37	RAMVDD	73	GPIO5	109	VSYNC
2	VCC33	38	RAMVDD	74	VDD_USB	110	HSYNC
3	VCC12	39	RAMVDD	75	DM0	111	PMCLK
4	N/C	40	MVDD_DLL1.2	76	DP0	112	DE
5	N/C	41	RAMVSS	77	DP1	113	IVDD
6	VCC33	42	MOVDD	78	DM1	114	ZD3
7	RAMVDD	43	MOVDD	79	VDD_USB	115	ZD2
8	GOVDD	44	RAMVSS	80	IVDD	116	ZD1
9	GPIO48	45	RAMVSS	81	VDX	117	ZD0
10	GPIO47	46	GPIO12	82	VD0	118	ZCLK
11	GPIO46	47	MOVDD	83	VD1	119	ZWS
12	GPIO45	48	GPIO11	84	VD2	120	RSTN
13	GPIO44	49	GPIO10	85	VD3	121	ENTEST
14	GPIO43	50	GPIO9	86	VD4	122	VOVDD
15	GPIO42	51	GPIO8	87	VD5	123	GPIO13
16	GPIO25	52	MOVDD	88	VOVDD	124	GPIO14
17	IVDD	53	GPIO7	89	VD6	125	GPIO15
18	MVREF	54	IVDD	90	VD7	126	GPIO16
19	GPIO24	55	GPIO6	91	VD8	127	GPIO17
20	GPIO23	56	VDDAPLL1.2	92	VD9	128	GPIO18
21	GPIO22	57	VDDAPLL1.2	93	VD10	129	GPIO19
22	GPIO21	58	XIN	94	VD11	130	IVDD
23	MOVDD	59	GOVDD	95	VD12	131	VSS
24	RAMVSS	60	GPIO33	96	VD13	132	VSS
25	GPIO20	61	GPIO32	97	VD14	133	VSS
26	AMCLK	62	GPIO31	98	VD15	134	VSS
27	RAMVDD	63	GPIO30	99	VD16	135	VSS
28	IVDD	64	GPIO29	100	VD17	136	VCC12
29	RAMVSS	65	GPIO28	101	VOVDD	137	VSS
30	RAMVDD	66	GPIO27	102	VD18	138	VSS
31	MOVDD	67	GPIO0	103	VD19	139	VCC33
32	RAMVSS	68	GPIO1	104	VD20	140	VSS
33	RAMVREF	69	GPIO2	105	VD21	141	VSS
34	RAMVDD	70	GPIO3	106	VD22	142	VCC12
35	RAMVSS	71	GOVDD	107	VD23	143	VSS
36	MOVDD	72	GPIO4	108	VOVDD	144	VSS

Table 4-22. Pins Listed in Alphabetical Order for IT9919

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AMCLK	26	GPIO27	66	RAMVDD	34	VD5	87
DM0	75	GPIO28	65	RAMVDD	37	VD6	89
DP0	76	GPIO29	64	RAMVDD	38	VD7	90
DP1	77	GPIO30	63	RAMVDD	39	VD8	91
DM1	78	GPIO31	62	RAMVREF	33	VD9	92
DE	112	GPIO32	61	RAMVSS	24	VD10	93
ENTEST	121	GPIO33	60	RAMVSS	29	VD11	94
GOVDD	8	GPIO42	15	RAMVSS	32	VD12	95
GOVDD	59	GPIO43	14	RAMVSS	35	VD13	96
GOVDD	71	GPIO44	13	RAMVSS	41	VD14	97
GPIO0	67	GPIO45	12	RAMVSS	44	VD15	98
GPIO1	68	GPIO46	11	RAMVSS	45	VD16	99
GPIO2	69	GPIO47	10	RSTN	120	VD17	100
GPIO3	70	GPIO48	9	VCC12	1	VD18	102
GPIO4	72	HSYNC	110	VCC12	3	VD19	103
GPIO5	73	IVDD	17	VCC12	136	VD20	104
GPIO6	55	IVDD	28	VCC12	142	VD21	105
GPIO7	53	IVDD	54	VCC33	2	VD22	106
GPIO8	51	IVDD	80	VCC33	6	VD23	107
GPIO9	50	IVDD	113	VCC33	139	VDX	81
GPIO10	49	IVDD	130	VSS	131	VDDAPLL1.2	56
GPIO11	48	MOVDD	23	VSS	132	VDDAPLL1.2	57
GPIO12	46	MOVDD	31	VSS	133	VDD_USB	74
GPIO13	123	MOVDD	36	VSS	134	VDD_USB	79
GPIO14	124	MOVDD	42	VSS	135	VOVDD	88
GPIO15	125	MOVDD	43	VSS	137	VOVDD	101
GPIO16	126	MOVDD	47	VSS	138	VOVDD	108
GPIO17	127	MOVDD	52	VSS	140	VOVDD	122
GPIO18	128	MVDD_DLL1.2	40	VSS	141	VSYNC	109
GPIO19	129	MVREF	18	VSS	143	XIN	58
GPIO20	25	N/C	4	VSS	144	ZCLK	118
GPIO21	22	N/C	5	VD0	82	ZD0	117
GPIO22	21	PMCLK	111	VD1	83	ZD1	116
GPIO23	20	RAMVDD	7	VD2	84	ZD2	115
GPIO24	19	RAMVDD	27	VD3	85	ZD3	114
GPIO25	16	RAMVDD	30	VD4	86	ZWS	119

4.6 IT9919 Pin Description

Table 4-23. IT9919 Pin Description for Video Interface

Pin(s) No.	Symbol	Attribute	Description
111	PMCLK	O	Output pixel clock
110	HSYNC	I/O	Horizontal sync. signal
109	VSYNC	I/O	Vertical sync. signal
112	DE	I/O	Data enable
81	VDX	I/O	Video clock and data swap is supported by register setting.
107, 106, 105, 104, 103, 102, 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85, 84, 83, 82	VD[23:0]	I/O	Video clock and data swap is supported by register setting.

Output direction is for HDMI loop through.

Table 4-24. IT9919 Pin Description for Audio Interface

Pin(s) No.	Symbol	Attribute	Description
26	AMCLK	I/O	Audio master clock
118	ZCLK	I/O	I2S serial clock
119	ZWS	I/O	I2S word select
114, 115, 116, 117	ZD[3:0]	I/O	I2S serial data

Output direction is for HDMI loop through.
Please see table 4-52 for Audio pin share.

Table 4-25. IT9919 Pin Description for USB Interface

Pin(s) No.	Symbol	Attribute	Description
74, 79	VDD_USB	P	Analog supply voltage. 3.3V typical
76	DP0	I/O	Data Pins USB data in data positive pin terminal
75	DM0	I/O	Data Pins USB data in data negative pin terminal
77	DP1	I/O	Data Pins USB data in data positive pin terminal
78	DM1	I/O	Data Pins USB data in data negative pin terminal

Table 4-26. IT9919 Pin Description for GPIO Interface

Pin(s) No.	Symbol	Attribute	Description
67	GPIO0	I/O	GPIO0
68	GPIO1	I/O	GPIO1
69	GPIO2	I/O	GPIO2
70	GPIO3	I/O	GPIO3
72	GPIO4	I/O	GPIO4
73	GPIO5	I/O	GPIO5
55	GPIO6	I/O	GPIO6
53	GPIO7	I/O	GPIO7
51	GPIO8	I/O	GPIO8
50	GPIO9	I/O	GPIO9
49	GPIO10	I/O	GPIO10

Pin(s) No.	Symbol	Attribute	Description
48	GPIO11	I/O	GPIO11
46	GPIO12	I/O	GPIO12
123	GPIO13	I/O	GPIO13
124	GPIO14	I/O	GPIO14
125	GPIO15	I/O	GPIO15
126	GPIO16	I/O	GPIO16
127	GPIO17	I/O	GPIO17
128	GPIO18	I/O	GPIO18
129	GPIO19	I/O	GPIO19
25	GPIO20	I/O	GPIO20
22	GPIO21	I/O	GPIO21
21	GPIO22	I/O	GPIO22
20	GPIO23	I/O	GPIO23
19	GPIO24	I/O	GPIO24
16	GPIO25	I/O	GPIO25
66	GPIO27	I/O	GPIO27
65	GPIO28	I/O	GPIO28
64	GPIO29	I/O	GPIO29
63	GPIO30	I/O	GPIO30
62	GPIO31	I/O	GPIO31
61	GPIO32	I/O	GPIO32
60	GPIO33	I/O	GPIO33
15	GPIO42	I/O	GPIO42
14	GPIO43	I/O	GPIO43
13	GPIO44	I/O	GPIO44
12	GPIO45	I/O	GPIO45
11	GPIO46	I/O	GPIO46
10	GPIO47	I/O	GPIO47
9	GPIO48	I/O	GPIO48

Please see table 4-49 for GPIO pin share.

Table 4-27. IT9919 Pin Description for Memory Interface

Pin(s) No.	Symbol	Attribute	Description
23, 31, 36, 42, 43, 47, 52	MOVDD	P	Memory Supply 1.8 V
18	MVREFF	P	Memory Reference voltage (1/2 * MOVDD)
40	MVDD_DLL1.2	P	Memory DLL Supply 1.35V
7, 27, 30, 34, 37, 38, 39	RAMVDD	P	Internal Stack Memory Supply 1.8 V
24, 29, 32, 35, 41, 44, 45	RAMVSS	P	Internal Stack Memory Ground
33	RAMVREF	P	Internal Stack Memory Reference voltage (1/2 * RAMVDD)

Table 4-28. IT9919 Pin Description for Misc. Interface

Pin(s) No.	Symbol	Attribute	Description
121	ENTEST	I	Test Enable
120	RSTN	I	Reset
56, 57	VDDAPLL1.2	P	Crystal Supply 1.35V

Pin(s) No.	Symbol	Attribute	Description
58	XIN	I	Crystal 12MHz Input

Table 4-29. IT9919 Pin Description for Power/Ground Signal

Pin(s) No.	Symbol	Attribute	Description
17, 28, 54, 80, 113, 130	IVDD	P	Digital Core supply 1.35V
1, 3, 130, 142	VCC12	P	I/O Supply 1.35V
2, 6, 139	VCC33	P	I/O Supply 3.3V
8, 59, 71	GOVDD	P	I/O Supply 3.3V
88, 101, 108, 122	VOVDD	P	I/O Supply 3.3V
131, 132, 133, 134,135, 137, 138, 140, 141, 143, 144	VSS	G	I/O Ground

4.7 IT9917 Pin Location

Figure 4-4. Pin Location of IT9917

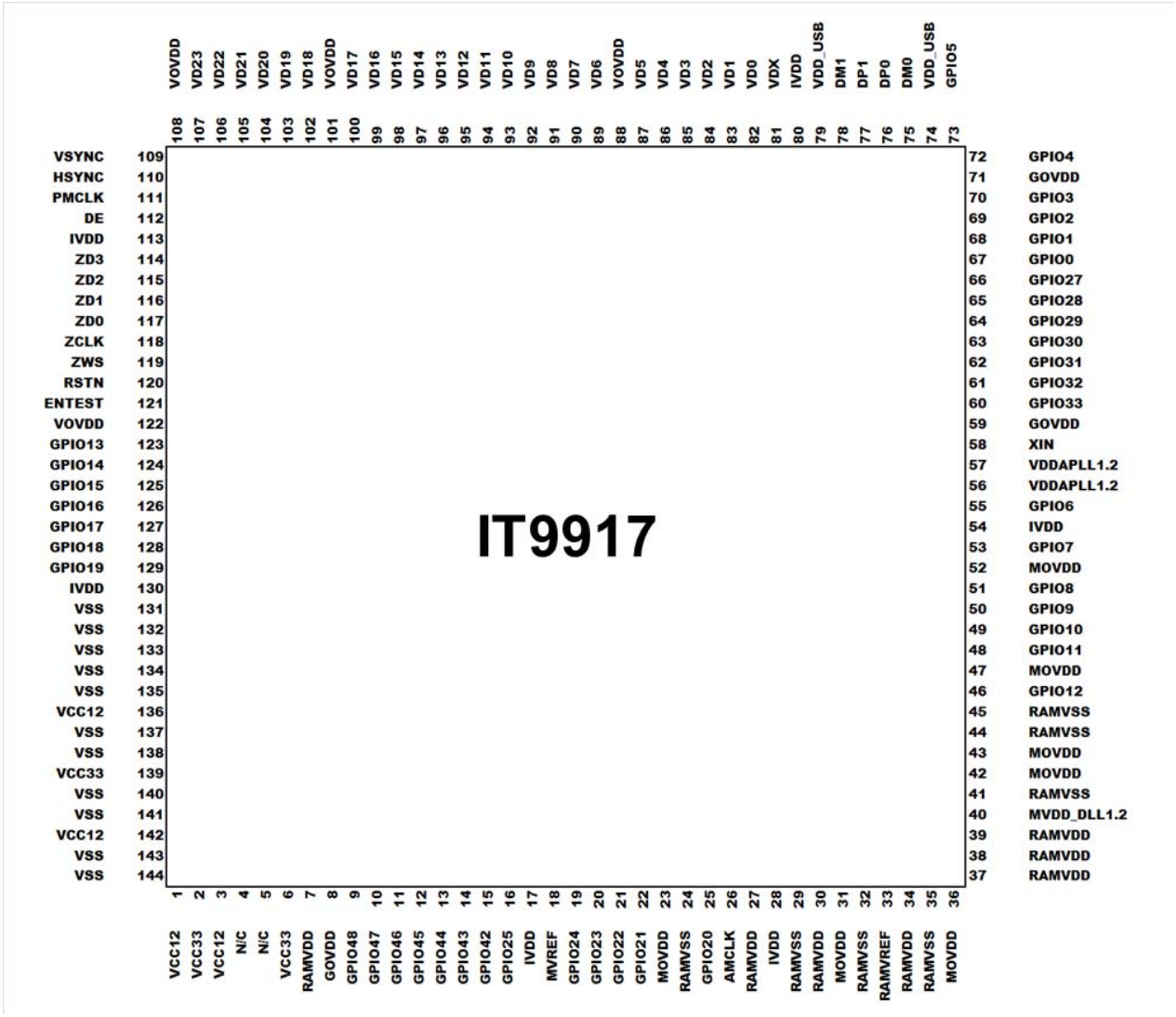


Table 4-30. Pins Listed in Numeric Order for IT9917

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC12	37	RAMVDD	73	GPIO5	109	VSYNC
2	VCC33	38	RAMVDD	74	VDD_USB	110	HSYNC
3	VCC12	39	RAMVDD	75	DM0	111	PMCLK
4	N/C	40	MVDD_DLL1.2	76	DP0	112	DE
5	N/C	41	RAMVSS	77	DP1	113	IVDD
6	VCC33	42	MOVDD	78	DM1	114	ZD3
7	RAMVDD	43	MOVDD	79	VDD_USB	115	ZD2
8	GOVDD	44	RAMVSS	80	IVDD	116	ZD1
9	GPIO48	45	RAMVSS	81	VDX	117	ZD0
10	GPIO47	46	GPIO12	82	VD0	118	ZCLK
11	GPIO46	47	MOVDD	83	VD1	119	ZWS
12	GPIO45	48	GPIO11	84	VD2	120	RSTN
13	GPIO44	49	GPIO10	85	VD3	121	ENTEST
14	GPIO43	50	GPIO9	86	VD4	122	VOVDD
15	GPIO42	51	GPIO8	87	VD5	123	GPIO13
16	GPIO25	52	MOVDD	88	VOVDD	124	GPIO14
17	IVDD	53	GPIO7	89	VD6	125	GPIO15
18	MVREF	54	IVDD	90	VD7	126	GPIO16
19	GPIO24	55	GPIO6	91	VD8	127	GPIO17
20	GPIO23	56	VDDAPLL1.2	92	VD9	128	GPIO18
21	GPIO22	57	VDDAPLL1.2	93	VD10	129	GPIO19
22	GPIO21	58	XIN	94	VD11	130	IVDD
23	MOVDD	59	GOVDD	95	VD12	131	VSS
24	RAMVSS	60	GPIO33	96	VD13	132	VSS
25	GPIO20	61	GPIO32	97	VD14	133	VSS
26	AMCLK	62	GPIO31	98	VD15	134	VSS
27	RAMVDD	63	GPIO30	99	VD16	135	VSS
28	IVDD	64	GPIO29	100	VD17	136	VCC12
29	RAMVSS	65	GPIO28	101	VOVDD	137	VSS
30	RAMVDD	66	GPIO27	102	VD18	138	VSS
31	MOVDD	67	GPIO0	103	VD19	139	VCC33
32	RAMVSS	68	GPIO1	104	VD20	140	VSS
33	RAMVREF	69	GPIO2	105	VD21	141	VSS
34	RAMVDD	70	GPIO3	106	VD22	142	VCC12
35	RAMVSS	71	GOVDD	107	VD23	143	VSS
36	MOVDD	72	GPIO4	108	VOVDD	144	VSS

Table 4-31. Pins Listed in Alphabetical Order for IT9917

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AMCLK	26	GPIO27	66	RAMVDD	34	VD5	87
DM0	75	GPIO28	65	RAMVDD	37	VD6	89
DP0	76	GPIO29	64	RAMVDD	38	VD7	90
DP1	77	GPIO30	63	RAMVDD	39	VD8	91
DM1	78	GPIO31	62	RAMVREF	33	VD9	92
DE	112	GPIO32	61	RAMVSS	24	VD10	93
ENTEST	121	GPIO33	60	RAMVSS	29	VD11	94
GOVDD	8	GPIO42	15	RAMVSS	32	VD12	95
GOVDD	59	GPIO43	14	RAMVSS	35	VD13	96
GOVDD	71	GPIO44	13	RAMVSS	41	VD14	97
GPIO0	67	GPIO45	12	RAMVSS	44	VD15	98
GPIO1	68	GPIO46	11	RAMVSS	45	VD16	99
GPIO2	69	GPIO47	10	RSTN	120	VD17	100
GPIO3	70	GPIO48	9	VCC12	1	VD18	102
GPIO4	72	HSYNC	110	VCC12	3	VD19	103
GPIO5	73	IVDD	17	VCC12	136	VD20	104
GPIO6	55	IVDD	28	VCC12	142	VD21	105
GPIO7	53	IVDD	54	VCC33	2	VD22	106
GPIO8	51	IVDD	80	VCC33	6	VD23	107
GPIO9	50	IVDD	113	VCC33	139	VDX	81
GPIO10	49	IVDD	130	VSS	131	VDDAPLL1.2	56
GPIO11	48	MOVDD	23	VSS	132	VDDAPLL1.2	57
GPIO12	46	MOVDD	31	VSS	133	VDD_USB	74
GPIO13	123	MOVDD	36	VSS	134	VDD_USB	79
GPIO14	124	MOVDD	42	VSS	135	VOVDD	88
GPIO15	125	MOVDD	43	VSS	137	VOVDD	101
GPIO16	126	MOVDD	47	VSS	138	VOVDD	108
GPIO17	127	MOVDD	52	VSS	140	VOVDD	122
GPIO18	128	MVDD_DLL1.2	40	VSS	141	VSYNC	109
GPIO19	129	MVREF	18	VSS	143	XIN	58
GPIO20	25	N/C	4	VSS	144	ZCLK	118
GPIO21	22	N/C	5	VD0	82	ZD0	117
GPIO22	21	PMCLK	111	VD1	83	ZD1	116
GPIO23	20	RAMVDD	7	VD2	84	ZD2	115
GPIO24	19	RAMVDD	27	VD3	85	ZD3	114
GPIO25	16	RAMVDD	30	VD4	86	ZWS	119

4.8 IT9917 Pin Description

Table 4-32. IT9917 Pin Description for Video Interface

Pin(s) No.	Symbol	Attribute	Description
111	PMCLK	O	Output pixel clock
110	HSYNC	I/O	Horizontal sync. signal
109	VSYNC	I/O	Vertical sync. signal
112	DE	I/O	Data enable
81	VDX	I/O	Video clock and data swap is supported by register setting.
107, 106, 105, 104, 103, 102, 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85, 84, 83, 82	VD[23:0]	I/O	Video clock and data swap is supported by register setting.

Output direction is for HDMI loop through.

Table 4-33. IT9917 Pin Description for Audio Interface

Pin(s) No.	Symbol	Attribute	Description
26	AMCLK	I/O	Audio master clock
118	ZCLK	I/O	I2S serial clock
119	ZWS	I/O	I2S word select
114, 115, 116, 117	ZD[3:0]	I/O	I2S serial data

Output direction is for HDMI loop through.
Please see table 4-52 for Audio pin share.

Table 4-34. IT9917 Pin Description for USB Interface

Pin(s) No.	Symbol	Attribute	Description
74, 79	VDD_USB	P	Analog supply voltage. 3.3V typical
76	DP0	I/O	Data Pins USB data in data positive pin terminal
75	DM0	I/O	Data Pins USB data in data negative pin terminal
77	DP1	I/O	Data Pins USB data in data positive pin terminal
78	DM1	I/O	Data Pins USB data in data negative pin terminal

Table 4-35. IT9917 Pin Description for GPIO Interface

Pin(s) No.	Symbol	Attribute	Description
67	GPIO0	I/O	GPIO0
68	GPIO1	I/O	GPIO1
69	GPIO2	I/O	GPIO2
70	GPIO3	I/O	GPIO3
72	GPIO4	I/O	GPIO4
73	GPIO5	I/O	GPIO5
55	GPIO6	I/O	GPIO6
53	GPIO7	I/O	GPIO7
51	GPIO8	I/O	GPIO8
50	GPIO9	I/O	GPIO9
49	GPIO10	I/O	GPIO10

Pin(s) No.	Symbol	Attribute	Description
48	GPIO11	I/O	GPIO11
46	GPIO12	I/O	GPIO12
123	GPIO13	I/O	GPIO13
124	GPIO14	I/O	GPIO14
125	GPIO15	I/O	GPIO15
126	GPIO16	I/O	GPIO16
127	GPIO17	I/O	GPIO17
128	GPIO18	I/O	GPIO18
129	GPIO19	I/O	GPIO19
25	GPIO20	I/O	GPIO20
22	GPIO21	I/O	GPIO21
21	GPIO22	I/O	GPIO22
20	GPIO23	I/O	GPIO23
19	GPIO24	I/O	GPIO24
16	GPIO25	I/O	GPIO25
66	GPIO27	I/O	GPIO27
65	GPIO28	I/O	GPIO28
64	GPIO29	I/O	GPIO29
63	GPIO30	I/O	GPIO30
62	GPIO31	I/O	GPIO31
61	GPIO32	I/O	GPIO32
60	GPIO33	I/O	GPIO33
15	GPIO42	I/O	GPIO42
14	GPIO43	I/O	GPIO43
13	GPIO44	I/O	GPIO44
12	GPIO45	I/O	GPIO45
11	GPIO46	I/O	GPIO46
10	GPIO47	I/O	GPIO47
9	GPIO48	I/O	GPIO48

Please see table 4-49 for GPIO pin share.

Table 4-36. IT9917 Pin Description for Memory Interface

Pin(s) No.	Symbol	Attribute	Description
23, 31, 36, 42, 43, 47, 52	MOVDD	P	Memory Supply 1.8 V
18	MVREFF	P	Memory Reference voltage (1/2 * MOVDD)
40	MVDD_DLL1.2	P	Memory DLL Supply 1.35V
7, 27, 30, 34, 37, 38, 39	RAMVDD	P	Internal Stack Memory Supply 1.8 V
24, 29, 32, 35, 41, 44, 45	RAMVSS	P	Internal Stack Memory Ground
33	RAMVREF	P	Internal Stack Memory Reference voltage (1/2 * RAMVDD)

Table 4-37. IT9917 Pin Description for Misc. Interface

Pin(s) No.	Symbol	Attribute	Description
121	ENTEST	I	Test Enable
120	RSTN	I	Reset
56, 57	VDDAPLL1.2	P	Crystal Supply 1.35V

Pin(s) No.	Symbol	Attribute	Description
58	XIN	I	Crystal 12MHz Input

Table 4-38. IT9917 Pin Description for Power/Ground Signal

Pin(s) No.	Symbol	Attribute	Description
17, 28, 54, 80, 113, 130	IVDD	P	Digital Core supply 1.35V
1, 3, 130, 142	VCC12	P	I/O Supply 1.35V
2, 6, 139	VCC33	P	I/O Supply 3.3V
8, 59, 71	GOVDD	P	I/O Supply 3.3V
88, 101, 108, 122	VOVDD	P	I/O Supply 3.3V
131, 132, 133, 134,135, 137, 138, 140, 141, 143, 144	VSS	G	I/O Ground

4.9 IT9917-H Pin Location

Figure 4-5. Pin Location of IT9917-H

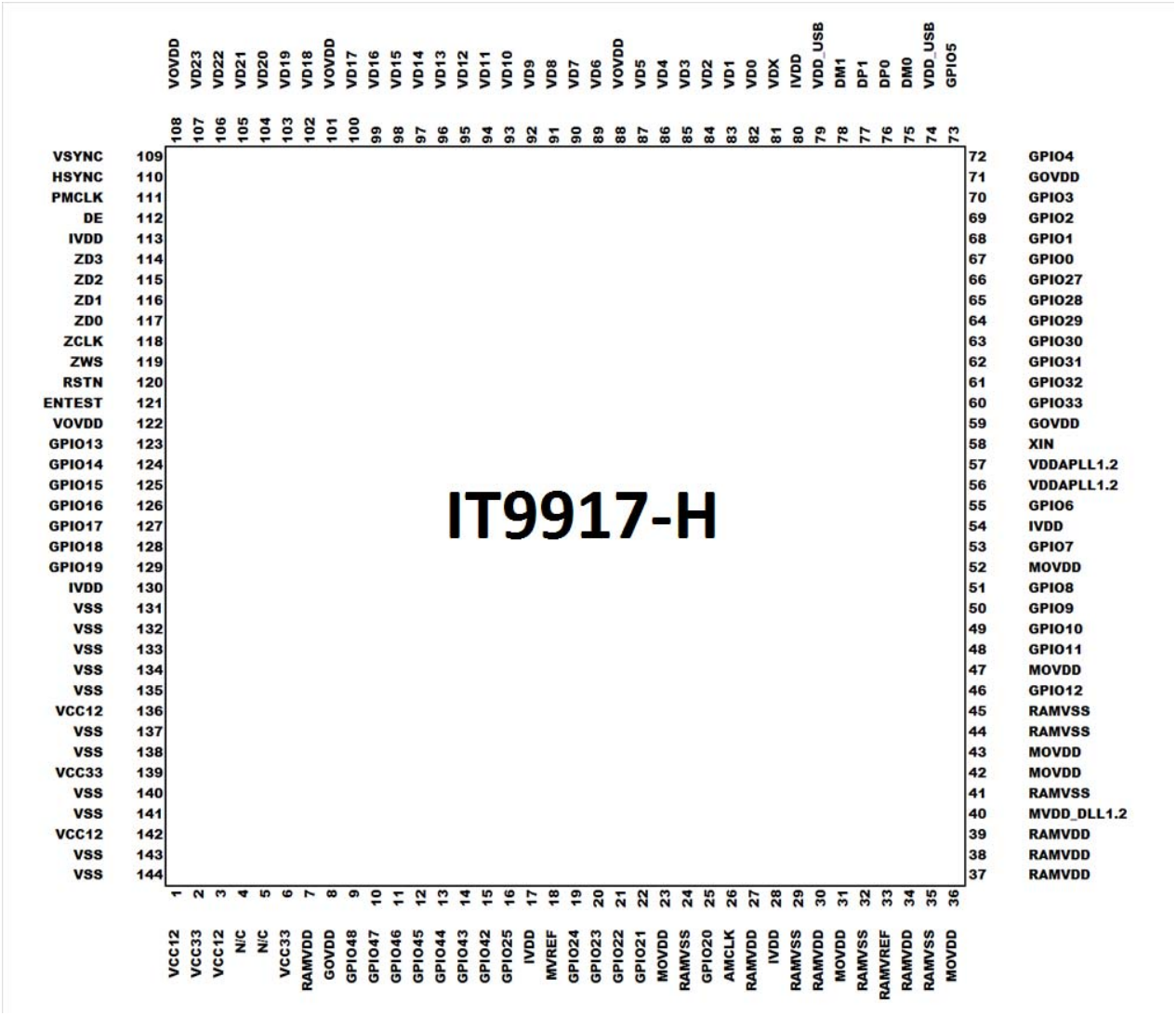


Table 4-39. Pins Listed in Numeric Order for IT9917-H

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	AVCC12	37	RAMVDD	73	GPIO5	109	VSYNC
2	PVCC33	38	RAMVDD	74	VDD_USB	110	HSYNC
3	APVDD12	39	RAMVDD	75	DM0	111	PMCLK
4	XTALOUT	40	MVDD_DLL1.2	76	DP0	112	DE
5	XTALIN	41	RAMVSS	77	DP1	113	IVDD
6	XTALVD33	42	MOVDD	78	DM1	114	ZD3
7	RAMVDD	43	MOVDD	79	VDD_USB	115	ZD2
8	GOVDD	44	RAMVSS	80	IVDD	116	ZD1
9	GPIO48	45	RAMVSS	81	VDX	117	ZD0
10	GPIO47	46	GPIO12	82	VD0	118	ZCLK
11	GPIO46	47	MOVDD	83	VD1	119	ZWS
12	GPIO45	48	GPIO11	84	VD2	120	RSTN
13	GPIO44	49	GPIO10	85	VD3	121	ENTEST
14	GPIO43	50	GPIO9	86	VD4	122	VOVDD
15	GPIO42	51	GPIO8	87	VD5	123	GPIO13
16	GPIO25	52	MOVDD	88	VOVDD	124	GPIO14
17	IVDD	53	GPIO7	89	VD6	125	GPIO15
18	MVREF	54	IVDD	90	VD7	126	GPIO16
19	GPIO24	55	GPIO6	91	VD8	127	GPIO17
20	GPIO23	56	VDDAPLL1.2	92	VD9	128	GPIO18
21	GPIO22	57	VDDAPLL1.2	93	VD10	129	GPIO19
22	GPIO21	58	XIN	94	VD11	130	IVDD
23	MOVDD	59	GOVDD	95	VD12	131	DDCSDA0
24	RAMVSS	60	GPIO33	96	VD13	132	DDCSCL0
25	GPIO20	61	GPIO32	97	VD14	133	R0PWR5V
26	AMCLK	62	GPIO31	98	VD15	134	P0_RXCN
27	RAMVDD	63	GPIO30	99	VD16	135	P0_RXCP
28	IVDD	64	GPIO29	100	VD17	136	AVCC12
29	RAMVSS	65	GPIO28	101	VOVDD	137	P0_RX0N
30	RAMVDD	66	GPIO27	102	VD18	138	P0_RX0P
31	MOVDD	67	GPIO0	103	VD19	139	AVCC33
32	RAMVSS	68	GPIO1	104	VD20	140	P0_RX1N
33	RAMVREF	69	GPIO2	105	VD21	141	P0_RX1P
34	RAMVDD	70	GPIO3	106	VD22	142	AVCC12
35	RAMVSS	71	GOVDD	107	VD23	143	P0_RX2N
36	MOVDD	72	GPIO4	108	VOVDD	144	P0_RX2P

Table 4-40. Pins Listed in Alphabetical Order for IT9917-H

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AMCLK	26	GPIO19	129	MVREF	18	VD8	91
APVDD12	3	GPIO20	25	P0_RX0N	137	VD9	92
AVCC12	1	GPIO21	22	P0_RX0P	138	VD10	93
AVCC12	136	GPIO22	21	P0_RX1N	140	VD11	94
AVCC12	142	GPIO23	20	P0_RX1P	141	VD12	95
AVCC33	139	GPIO24	19	P0_RX2N	143	VD13	96
DM0	75	GPIO25	16	P0_RX2P	144	VD14	97
DP0	76	GPIO27	66	P0_RXCN	134	VD15	98
DP1	77	GPIO28	65	P0_RXCP	135	VD16	99
DM1	78	GPIO29	64	PMCLK	111	VD17	100
DE	112	GPIO30	63	PVCC33	2	VD18	102
DDCSDA0	131	GPIO31	62	R0PWR5V	133	VD19	103
DDCSCL0	132	GPIO32	61	RAMVDD	7	VD20	104
ENTEST	121	GPIO33	60	RAMVDD	27	VD21	105
GOVDD	8	GPIO42	15	RAMVDD	30	VD22	106
GOVDD	59	GPIO43	14	RAMVDD	34	VD23	107
GOVDD	71	GPIO44	13	RAMVDD	37	VDX	81
GPIO0	67	GPIO45	12	RAMVDD	38	VDDAPLL1.2	56
GPIO1	68	GPIO46	11	RAMVDD	39	VDDAPLL1.2	57
GPIO2	69	GPIO47	10	RAMVREF	33	VDD_USB	74
GPIO3	70	GPIO48	9	RAMVSS	24	VDD_USB	79
GPIO4	72	HSYNC	110	RAMVSS	29	VOVDD	88
GPIO5	73	IVDD	17	RAMVSS	32	VOVDD	101
GPIO6	55	IVDD	28	RAMVSS	35	VOVDD	108
GPIO7	53	IVDD	54	RAMVSS	41	VOVDD	122
GPIO8	51	IVDD	80	RAMVSS	44	VSYNC	109
GPIO9	50	IVDD	113	RAMVSS	45	XIN	58
GPIO10	49	IVDD	130	RSTN	120	XTALIN	5
GPIO11	48	MOVDD	23	VD0	82	XTALOUT	4
GPIO12	46	MOVDD	31	VD1	83	XTALVD33	6
GPIO13	123	MOVDD	36	VD2	84	ZCLK	118
GPIO14	124	MOVDD	42	VD3	85	ZD0	117
GPIO15	125	MOVDD	43	VD4	86	ZD1	116
GPIO16	126	MOVDD	47	VD5	87	ZD2	115
GPIO17	127	MOVDD	52	VD6	89	ZD3	114
GPIO18	128	MVDD_DLL1.2	40	VD7	90	ZWS	119

4.10 IT9917-H Pin Description

Table 4-41. IT9917-H Pin Description for Video Interface

Pin(s) No.	Symbol	Attribute	Description
111	PMCLK	O	Output pixel clock
110	HSYNC	I/O	Horizontal sync. signal
109	VSYNC	I/O	Vertical sync. signal
112	DE	I/O	Data enable
81	VDX	I/O	Video clock and data swap is supported by register setting.
107, 106, 105, 104, 103, 102, 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85, 84, 83, 82	VD[23:0]	I/O	Video clock and data swap is supported by register setting.

Output direction is for HDMI loop through.

Table 4-42. IT9917-H Pin Description for Audio Interface

Pin(s) No.	Symbol	Attribute	Description
26	AMCLK	I/O	Audio master clock
118	ZCLK	I/O	I2S serial clock
119	ZWS	I/O	I2S word select
114, 115, 116, 117	ZD[3:0]	I/O	I2S serial data

Output direction is for HDMI loop through.
Please see table 4-52 for Audio pin share.

Table 4-43. IT9919-H Pin Description for USB Interface

Pin(s) No.	Symbol	Attribute	Description
74, 79	VDD_USB	P	Analog supply voltage. 3.3V typical
76	DP0	I/O	Data Pins USB data in data positive pin terminal
75	DM0	I/O	Data Pins USB data in data negative pin terminal
77	DP1	I/O	Data Pins USB data in data positive pin terminal
78	DM1	I/O	Data Pins USB data in data negative pin terminal

Table 4-44. IT9917-H Pin Description for HDMI Interface

Pin(s) No.	Symbol	Attribute	Description
133	R0PWR5V	I	TMDS transmitter detection (5V-tolerant)
131	DDCSDA0	I/O	DDC I2C Data for HDMI Port (5V-tolerant)
132	DDCSCL0	I/O	DDC I2C Clock for HDMI Port (5V-tolerant)
137	P0_RX0N	I	HDMI Channel 0 negative input for HDMI Port
138	P0_RX0P	I	HDMI Channel 0 positive input for HDMI Port
140	P0_RX1N	I	HDMI Channel 1 negative input for HDMI Port
141	P0_RX1P	I	HDMI Channel 1 positive input for HDMI Port
143	P0_RX2N	I	HDMI Channel 2 negative input for HDMI Port
144	P0_RX2P	I	HDMI Channel 2 positive input for HDMI Port
134	P0_RXCN	I	HDMI Clock Channel negative input for HDMI Port
135	P0_RXCP	I	HDMI Clock Channel positive input for HDMI Port

Pin(s) No.	Symbol	Attribute	Description
5	XTALIN	I	Crystal clock input (for Audio PLL)
4	XTALOUT	O	Crystal clock output (for Audio PLL)
3	APVDD12	P	HDMI audio PLL power (1.35V)
1, 136, 142	AVCC12	P	HDMI analog frontend power (1.35V)
139	AVCC33	P	HDMI analog frontend power (3.3V)
2	PVCC33	P	HDMI receiver PLL power (3.3V)
6	XTALVD33	P	Power for crystal oscillator (3.3V)

Table 4-45. IT9917-H Pin Description for GPIO Interface

Pin(s) No.	Symbol	Attribute	Description
67	GPIO0	I/O	GPIO0
68	GPIO1	I/O	GPIO1
69	GPIO2	I/O	GPIO2
70	GPIO3	I/O	GPIO3
72	GPIO4	I/O	GPIO4
73	GPIO5	I/O	GPIO5
55	GPIO6	I/O	GPIO6
53	GPIO7	I/O	GPIO7
51	GPIO8	I/O	GPIO8
50	GPIO9	I/O	GPIO9
49	GPIO10	I/O	GPIO10
48	GPIO11	I/O	GPIO11
46	GPIO12	I/O	GPIO12
123	GPIO13	I/O	GPIO13
124	GPIO14	I/O	GPIO14
125	GPIO15	I/O	GPIO15
126	GPIO16	I/O	GPIO16
127	GPIO17	I/O	GPIO17
128	GPIO18	I/O	GPIO18
129	GPIO19	I/O	GPIO19
25	GPIO20	I/O	GPIO20
22	GPIO21	I/O	GPIO21
21	GPIO22	I/O	GPIO22
20	GPIO23	I/O	GPIO23
19	GPIO24	I/O	GPIO24
16	GPIO25	I/O	GPIO25
66	GPIO27	I/O	GPIO27
65	GPIO28	I/O	GPIO28
64	GPIO29	I/O	GPIO29
63	GPIO30	I/O	GPIO30
62	GPIO31	I/O	GPIO31
61	GPIO32	I/O	GPIO32
60	GPIO33	I/O	GPIO33
15	GPIO42	I/O	GPIO42
14	GPIO43	I/O	GPIO43
13	GPIO44	I/O	GPIO44
12	GPIO45	I/O	GPIO45
11	GPIO46	I/O	GPIO46
10	GPIO47	I/O	GPIO47
9	GPIO48	I/O	GPIO48

Please see table 4-49 for GPIO pin share.

Table 4-46. IT9917-H Pin Description for Memory Interface

Pin(s) No.	Symbol	Attribute	Description
23, 31, 36, 42, 43, 47, 52	MOVDD	P	Memory Supply 1.8 V
18	MVREFF	P	Memory Reference voltage (1/2 * MOVDD)
40	MVDD_DLL1.2	P	Memory DLL Supply 1.35 V
7, 27, 30, 34, 37, 38, 39	RAMVDD	P	Internal Stack Memory Supply 1.8 V
24, 29, 32, 35, 41, 44, 45	RAMVSS	P	Internal Stack Memory Ground
33	RAMVREF	P	Internal Stack Memory Reference voltage (1/2 * RAMVDD)

Table 4-47. IT9917-H Pin Description for Misc. Interface

Pin(s) No.	Symbol	Attribute	Description
121	ENTEST	I	Test Enable
120	RSTN	I	Reset
56, 57	VDDAPLL1.2	P	Crystal Supply 1.35V
58	XIN	I	Crystal 12MHz Input

Table 4-48. IT9917-H Pin Description for Power/Ground Signal

Pin(s) No.	Symbol	Attribute	Description
17, 28, 54, 80, 113, 130	IVDD	P	Digital Core supply 1.35V
8, 59, 71	GOVDD	P	I/O Supply 3.3V
88, 101, 108, 122	VOVDD	P	I/O Supply 3.3V

4.11 GPIO Pin Share

Table 4-49. GPIO Pin Share Table

Pin	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
GPIO0	GPIO0	UART0 RX / IrDA_RXL	SPDIF_O	TSI_CSN	UART1 TX/RX
GPIO1	GPIO1	UART0 TX / IrDA_TX	PWM1	TSI_CLK	UART1 TX/RX
GPIO2	GPIO2	UART0 CTS / IrDA_RXH	IIC SDA	TSI_STR	UART1 TX/RX
GPIO3	GPIO3	UART0 RI	IIC SCL	TSI_DATA	UART1 TX/RX
GPIO4	GPIO4	USBID	Remote IR_T	LINK	UART1 TX/RX
GPIO5	GPIO5	XOUT	Remote IR_R	SD1CLK	UART1 TX/RX
GPIO6	GPIO6	UART0 DSR	SD0CLK	MDC	UART1 TX/RX
GPIO7	GPIO7	NR0CSN	SD1CLK		UART1 TX/RX
GPIO8	GPIO8	UART0 RI	SDCMD	MDIO	UART1 TX/RX
GPIO9	GPIO9	NRDO	SD_D0		UART1 TX/RX
GPIO10	GPIO10	NRDI	SD_D1		UART1 TX/RX
GPIO11	GPIO11	NRCLK	SD_D2		UART1 TX/RX
GPIO12	GPIO12	SPDIF_O	SD_D3	LINK	UART1 TX/RX
GPIO13	GPIO13	TSO_CSN	TSI_CSN	TXD0	UART1 TX/RX
GPIO14	GPIO14	TSO_CLK	TSI_CLK	TXD1	UART1 TX/RX
GPIO15	GPIO15	TSO_STR	TSI_STR	TX_EN	UART1 TX/RX
GPIO16	GPIO16	TSO_DATA	TSI_DATA	PWRDN	UART1 TX/RX
GPIO17	GPIO17	Remote IR_R	NR1CSN	REF_CLK	UART1 TX/RX
GPIO18	GPIO18	IIC SDA	KMICL	MDC	UART1 TX/RX
GPIO19	GPIO19	IIC SCL	KMIDA	MDIO	UART1 TX/RX
GPIO20	GPIO20	SPI_CLK	SD_D4	RXD0	UART1 TX/RX
GPIO21	GPIO21	SPI_CSN	SD_D5	RXD1	UART1 TX/RX
GPIO22	GPIO22	SPI_MOSI	SD_D6	RX_CRS_DV	UART1 TX/RX
GPIO23	GPIO23	SPI_MISO	SD_D7	RX_ER	UART1 TX/RX
GPIO24	GPIO24	UART0 RTS	PWM2		UART1 TX/RX
GPIO25	GPIO25	UART0 DTR	Remote IR_T		UART1 TX/RX
GPIO27	GPIO27	SPI_CLK	SD_D4	RXD0	UART1 TX/RX
GPIO28	GPIO28	SPI_CSN	SD_D5	RXD1	UART1 TX/RX
GPIO29	GPIO29	SPI_MOSI	SD_D6	RX_CRS_DV	UART1 TX/RX
GPIO30	GPIO30	SPI_MISO	SD_D7	RX_ER	UART1 TX/RX
GPIO31	GPIO31	UART0 RTS	PWM2		UART1 TX/RX
GPIO32	GPIO32	UART0 DTR	Remote IR_T		UART1 TX/RX
GPIO33	GPIO33	PWM0	Remote IR_R	MDIO	UART1 TX/RX
GPIO42	GPIO42	SPI_CLK	SD_D4	REF_CLK	UART1 TX/RX
GPIO43	GPIO43	SPI_CSN	SD_D5	TX_EN	UART1 TX/RX
GPIO44	GPIO44	SPI_MOSI	SD_D6	RX_CRS_DV	UART1 TX/RX
GPIO45	GPIO45	SPI_MISO	SD_D7	RX_ER	UART1 TX/RX
GPIO46	GPIO46	UART0 RTS	PWM2	MDC	UART1 TX/RX
GPIO47	GPIO47	UART0 DTR	Remote IR_T	MDIO	UART1 TX/RX
GPIO48	GPIO48	PWM0	Remote IR_R	PWRDN	UART1 TX/RX

Notes: GPIO14, GPIO15, GPIO16, GPIO17, GPIO24, GPIO25 is the hardware trap for IT9919-H. There is pull-high/low resistance on I/O. It cannot driving value on the external device when the system is resetting.

Table 4-50. SPI Host Interface when HOST_CFG == 01

Pin Name	Type	Default	Description
GPIO0	Input	HighZ	SPI Slave CLK
GPIO1	Input	HighZ	SPI Slave CS#
GPIO2	Input	HighZ	SPI Slave MOSI

Pin Name	Type	Default	Description
GPIO3	Output	0	SPI Slave MISO

Table 4-51. IIC Host Interface when HOST_CFG == 10

Pin Name	Type	Default	Description
GPIO0	I/O	HighZ	IIC SCL
GPIO1	I/O	HighZ	IIC SDA

4.12 Audio Pin Share

Table 4-52. Audio Pin Share Table

	Mode 1 (HDMI *)		Mode 2 (I2S & SPDIF input)		Mode 3 (I2S output)	
Pin	**Symbol**	**Attribute**	**Symbol**	**Attribute**	**Symbol**	**Attribute**
AMCLK	AMCLK	I/O	AMCLK	I/O	AMCLK	I/O
ZCLK	ZCLK	I/O	ZCLK	I/O	ZCLK	I/O
ZWS	ZWS	I/O	ZWS	I/O	ZWS	I/O
ZD0	ZD0	I/O	ZD0	I		
ZD1	ZD1	I/O				
ZD2	ZD2	I/O			ZD0	O
ZD3	ZD3	I/O				
DE			ZD0	I		
PMCLK			SPDIF	I		

Output is for HDMI loop through.

4.13 Function Comparism

Table 4-53. Function Comparism

Function	IT9917	IT9919	IT9917-H	IT9919-H	IT9919-N
Package	144 TQFP/EPAD	144 TQFP/EPAD	144 TQFP/EPAD	144 TQFP/EPAD	144 TQFP/EPAD
Memory	DDR2 64MB Embedded	DDR2 64MB Embedded	DDR2 64MB Embedded	DDR2 64MB Embedded	DDR2 64MB Embedded
HDMI RX	No	No	YES	YES	YES
HDCP	No	No	YES	YES	No
Encoder Power	1280x720x30P	1920x1080x30P	1280x720x30P	1920x1080x30P	1920x1080x30P

4.14 Hardware Trapping

Table 4-54. Hardware Trapping for IT9910

Pin Name	Symbol	Description
GPIO14	BOOT_CFG0	Boot Configuration 00: booting from SD/MMC 01: booting from NOR 10:Reserved 11: co-operative mode
GPIO15	BOOT_CFG1	
GPIO16	HOST_CFG0	Host Configuration 00: select JTAG interface 01: select SPI interface 10: select IIC interface 11: uses as DGPIO[0-3]
GPIO17	HOST_CFG1	
GPIO24	PLL_CFG	PLL Configuration 0: Normal 1: bypass PLL
GPIO25	DCXO_CFG	PLL DCXO Configuration 0: Normal 1: bypass DCXO

5. Function Decscription

5.1 Host Interface

5.1.1 General Description

A host processor can communicate with IT9910 through host interface. There are two types of bus protocol supported by host interface. By trapping DPGIO16 and DGPIO17 pins to decide the bus protocol of the host interface. The following table shows the setting.

Table 5-1. Host Bus Type

DGPIO17	DGPIO16	Host Bus Type Description
0	1	SPI-slave interface
1	0	IIC-slave interface

5.1.2 IIC-Slave Interface

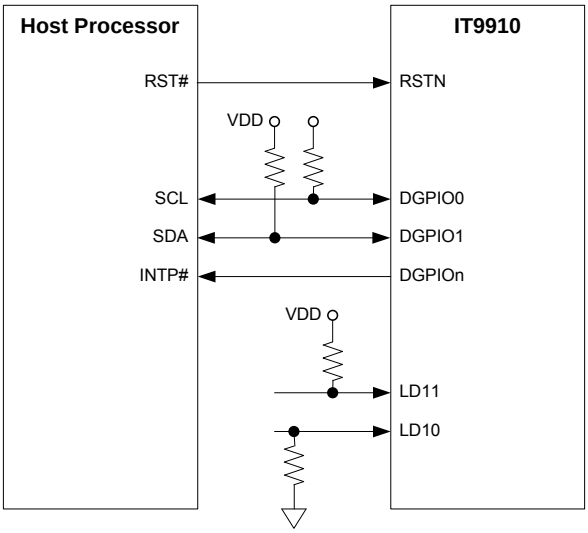


Figure 2 IIC-Slave Interface Implementation

IIC interface data transfer is starting with a START(S) condition and ending with STOP(P) condition. HOST starting a transfer should send a Slave_ID to slave firstly. The Slave_ID is 0x58 for write, and 0x59 for read. The following Address and Data is transferred in the unit of 16-bit, and low byte is before high byte. When transfer each byte, master and slave should return an acknowledgement (1-bit) in the 9th SCL, '0' is ack and '1' is non-ack. Write/Read transaction have separate format. The following figures and table show the details.

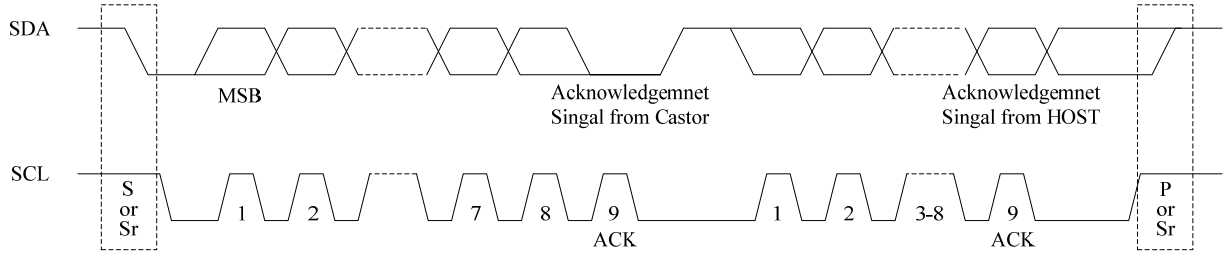


Figure 5-2. IIC Data Transfer

Write

S	Slave_ID_Wr	ACK-s	Address_L	ACK-s	Address_H	ACK-s	
			Data_Wr_L	ACK-s	Data_Wr_H	ACK-s	P

Data Transferred
(n bytes + acknowledge)

Read

S	Slave_ID_Wr	ACK-s	Address_L	ACK-s	Address_H	ACK-s	P
S	Slave_ID_Rd	ACK-s	Data_Rd_L	ACK-m	Data_Rd_H	(1) NACK-m	P

Data Transferred
(n bytes + acknowledge)

Note:
1. In reading cycles, the last data byte is followed by a "non-ack".

Figure 5-3. IIC-Slave Write/Read Transaction

Table 5-2. IIC-Slave Transaction Symbol Description

Symbol	Description
S or Sr	Start/Restart condition
Slave_ID_Wr	0x58
Slave_ID_Rd	0x59
ACK-s	Acknowledgement by Slave
ACK-m	Acknowledgement by Master

NACK-m	In IIC reading, the master device should “NACK” the last data byte to terminate the reading cycle.
Address_L	Address bits
Address_H	Address bits[16:9], MSB defines MMIO (= '0') or Memory (= '1')
Data_Wr_L	Write data bits[7:0]
Data_Wr_H	Write data bits[15:8]
Data_Rd_L	Read data bits[7:0]
Data_Rd_H	Read data bits[15:8]
P	Stop condition

.

5.1.3 SPI-Slave Interface

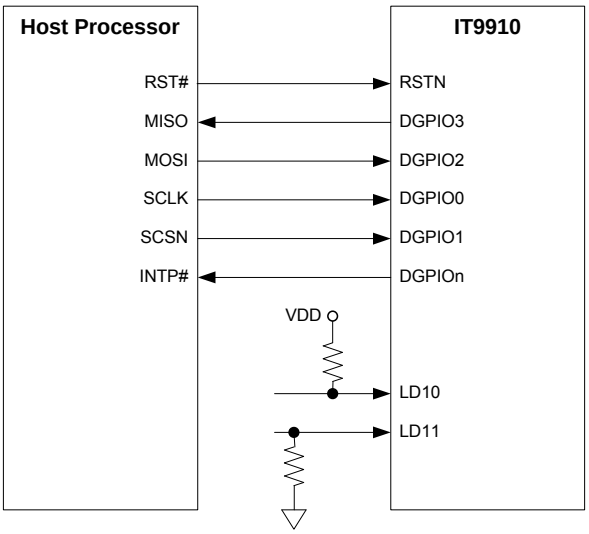


Figure 3 SPI-Slave Interface Implementation

SPI-Slave interface only supports SPI mode 0. Write/Read transaction is showed in the following figure. Its protocol is similar to IIC-slave interface. Address and Data is also 16-bit but acknowledgement is 8-bit. “FF” is ack and “00” is non-ack state.

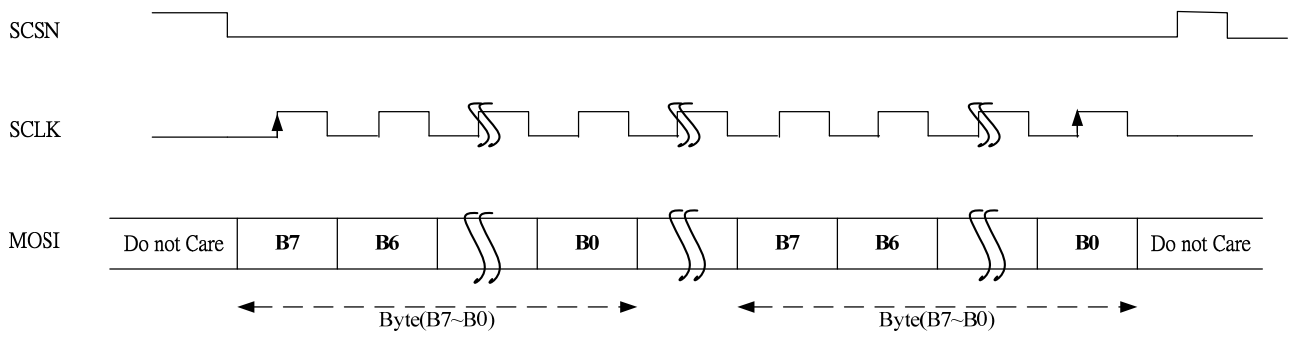


Figure 5-5. SPI Mode 0

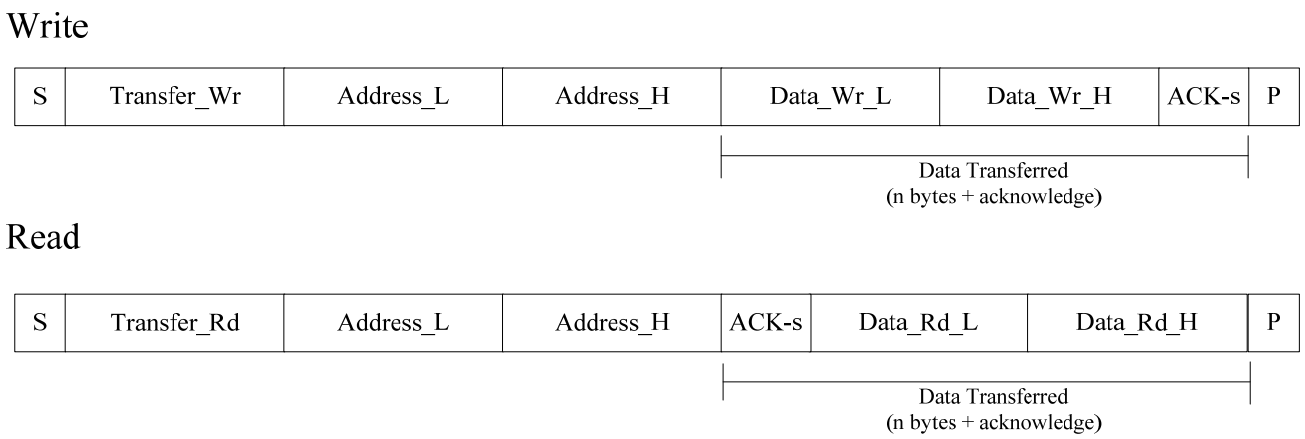


Figure 5-6. SPI-Slave Write/Read Transaction

Table 5-3. SPI-Slave Transaction Symbol Description

Symbol	Description
S	Start condition (SCSN falling edge)
Transfer_Wr	LSB= '0' is write transfer
Transfer_Rd	LSB= '1' is read transfer
ACK-s	Acknowledgement by Slave
Address_L	Address bits[8:1]
Address_H	Address bits[16:9], MSB defines MMIO (= '0') or Memory (= '1')
Data_Wr_L	Write data bits[7:0]
Data_Wr_H	Write data bits[15:8]
Data_Rd_L	Read data bits[7:0]
Data_ Rd_H	Read data bits[15:8]
P	Stop condition (SCSN rising edge)

5.2 HDMI Receiver Interface

The IT9910 provides high-performance and low-power single channel HDMI receiver, fully compliant with HDMI 1.3 and HDCP 1.4. Aside from the various video input formats supported, the IT9910 also supports 8 channels of I2S uncompressed digital audio, with sampling rate up to 192 kHz and sample size up to 24 bits. The figure is the functional block diagram of the IT9910 HDMI Receiver, which describes clearly the data flow.

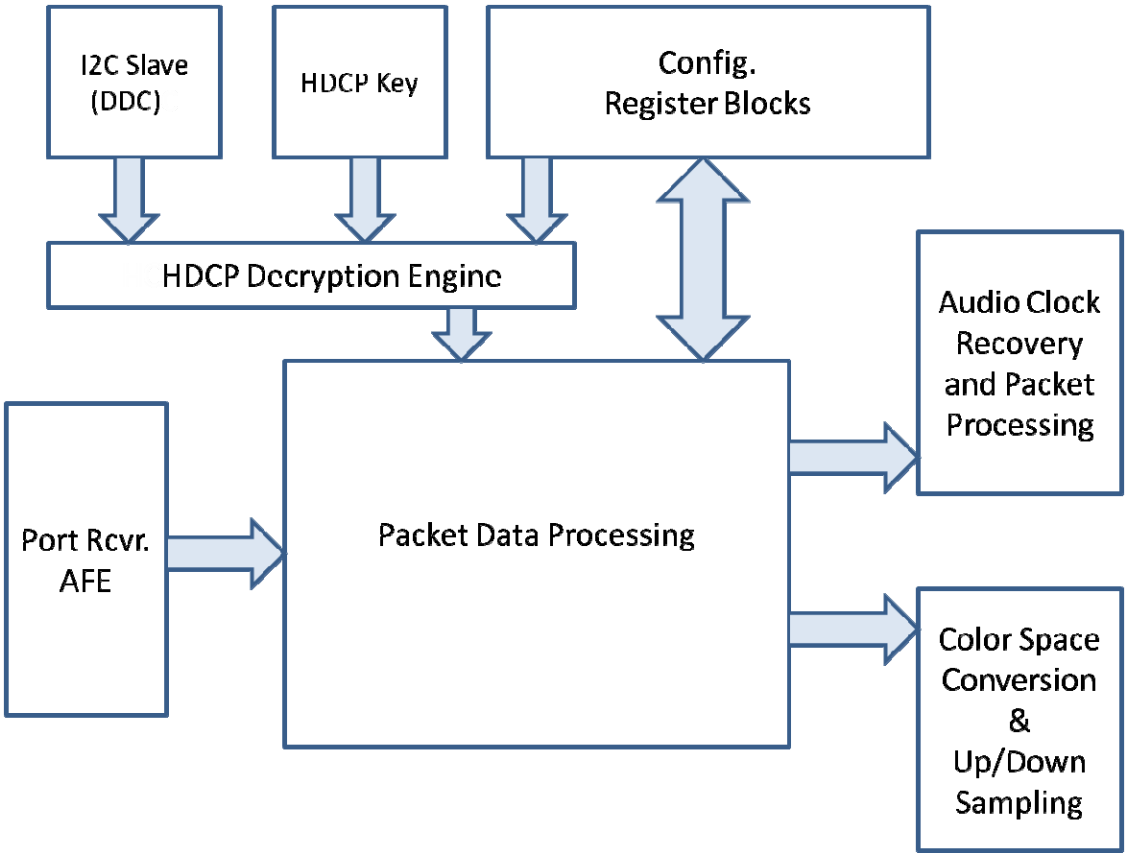


Figure 5-7. Functional block diagram of the HDMI Receiver

5.2.1 Receiver Analog Frontend (Rcvr. AFE)

The integrated TMDS receiver analog frontend macros is capable of receiving and decoding HDMI data at up to 2.25Gbps (with a TMDS clock of 225MHz). Adaptive equalization is employed to support long cables. The system firmware has total control over this through register settings.

5.2.2 Video Data Processing

IT9910 with its Deep Color capability ensures robust reception of high-quality uncompressed video content. Advanced processing algorithms are employed to optimize the performance of video processing such as color space conversion an up/down sampling.

Upsampling (YCbCr422 to YCbCr444)
In cases where input HDMI video data are in YCbCr 4:2:2 format and output is selected as 4:4:4, this block is enabled to do the upsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during upsampling.

Bi-directional Color Space Conversion (YCbCr ↔ RGB)
Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers bi-directional RGB ↔ YCbCr color space conversion (CSC). To provide maximum flexibility, the matrix coefficients of the CSC engine in the IT9910 are fully programmable. Users could elect to employ their preferred conversion formula.

Downsampling (YCbCr444 to YCbCr422)
In cases where input HDMI video data are in YCbCr 4:4:4 format and output is selected as YCbCr 4:2:2, this

block is enabled to do the downsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during downsampling.

Dithering (Dithering 12-to-10 or 12-to-8)
For outputing to the 10-bits / 8-bits-per-channel formats, decimation might be required depending on the exact input formats. This block performs the necessary dithering for decimation to prevent visible artifacts from appearing.

5.2.3 Audio Processing

The audio processing block in the HDMI Sink is crucial to the system performance since human hearing is susceptive to audio imperfection. The IT9910 prides itself in outstanding audio recovery performances. In addition, the audio clock recovery PLL uses an external crystal reference so as to provide stable and reliable audio clocks for all audio output formats.

Some previous HDMI Sink products were reported to generate unbearably harsh sounds during hot-plug / unplug as well as unspecified audio error. The IT9910 prides itself for detecting all kinds of audio error and soft-mutes the audio accordingly, therefore preventing unpleasant noise from outputting.

5.2.4 HDCP Engine and DDC Channel

The HDCP engine decrypts in incoming data. Preprogrammed HDCP keys are embedded in the IT9910. Users need not worry about the purchasing and management of the HDCP keys.

The DDC I2C interface is present at DDCSCL0 (Pin 131) & DDCSDA0 (Pin 132). With the interfaces, the IT9910 responds to the access of HDMI Sources via the DDC channels. HDMI Sources use the interfaces to perform HDCP authentication with the IT9910.

5.3 Video Input Interface

IT9910 can support various video input formats, including embedded sync and separated sync. The module captures the input video data and writes to memory or sends to Image Signal Processor module directly. The module also supports horizontal scaling down, down sampling and dithering.

The features of video input interface include :

- Support 24/30/36-bit RGB/YCbCr
- Support BT601 : 16/20/24-bit YCbCr 4:2:2
- Support BT656 : 8/10/12-bit YCbCr 4:2:2
- Support HD BT1120 interface
- BT656 like time multiplexed input with 54/108/144 MHz
- Down sampling from YCbCr 4:4:4 to YCbCr 4:2:2 or 4:2:0
- Dithering for conversion from 12-bit/10-bit component to 8-bit

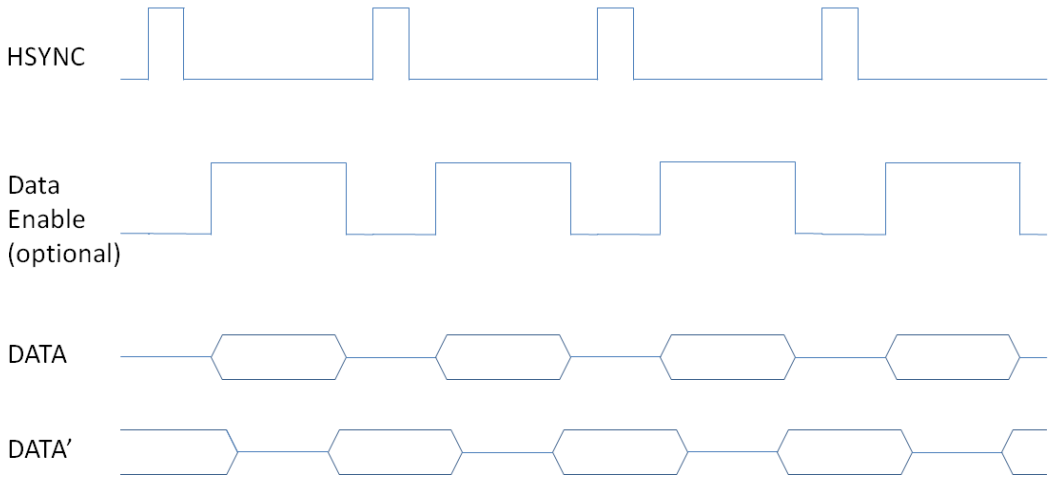


Figure 5-8. Active segment with Data Enable

IT9910 can receive parallel video signal with dedicated synchronous signals. It captures active segment of an active line via either indication of data enable or manual specification in registers. In manual mode, user is allowed to specify desired segment even across horizontal blanking.

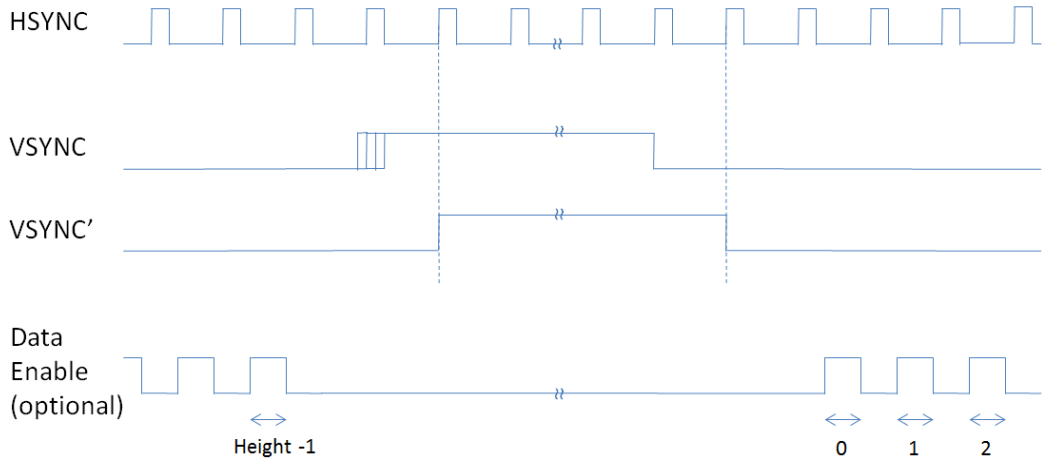


Figure 5-9. Realigns vertical sync

IT9910 accepts unstable vertical sync signal converted from analog source. It realigns vertical sync signal to horizontal sync signal for a stable frame start point.

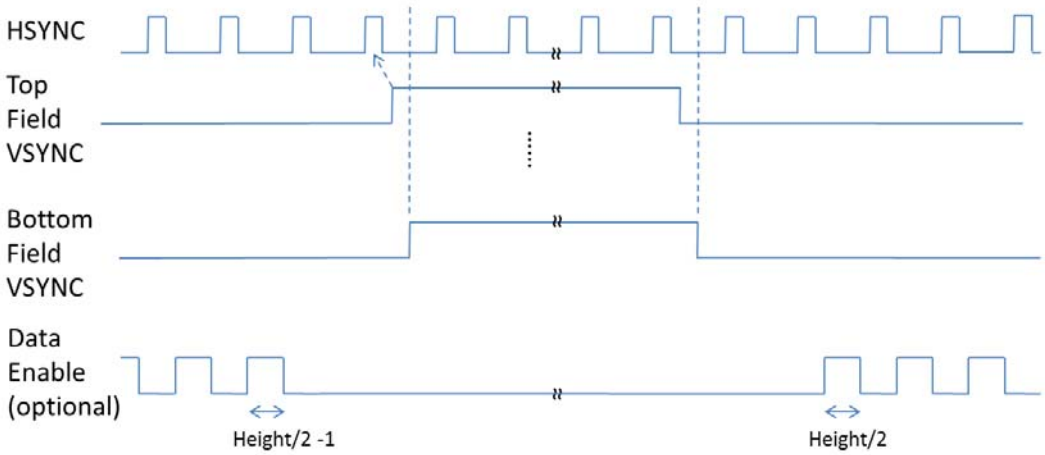
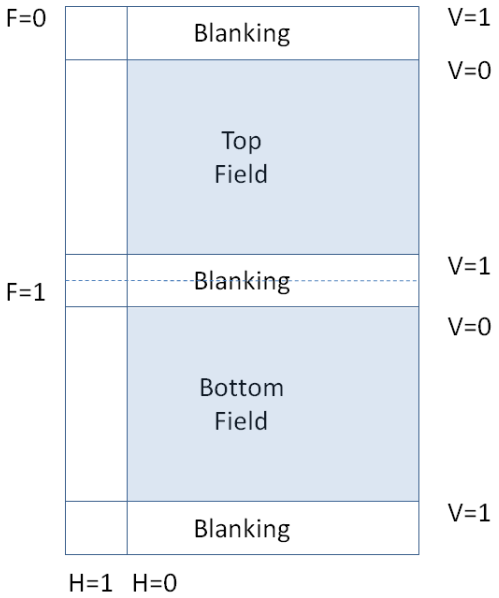


Figure 5-10. Interlaced signal timing waveform

The sync process for standard interlaced signal requires that VSYNC of bottom field toggles at around half line and VSYNC of top field toggles during horizontal blanking. IT9910, moreover, can manually handle top and bottom VSYNC both toggle during horizontal non-blanking, which could exist in digitized analog source.



	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Byte0	1	1	1	1	1	1	1	1
Byte1	0	0	0	0	0	0	0	0
Byte2	0	0	0	0	0	0	0	0
Byte3	1	F	V	H	-	-	-	-

Figure 5-11. BT656 sync codeword

IT9910 accept video signals with embedded syncs in conformance with BT.656 and BT.1120, as depicted in above diagram.

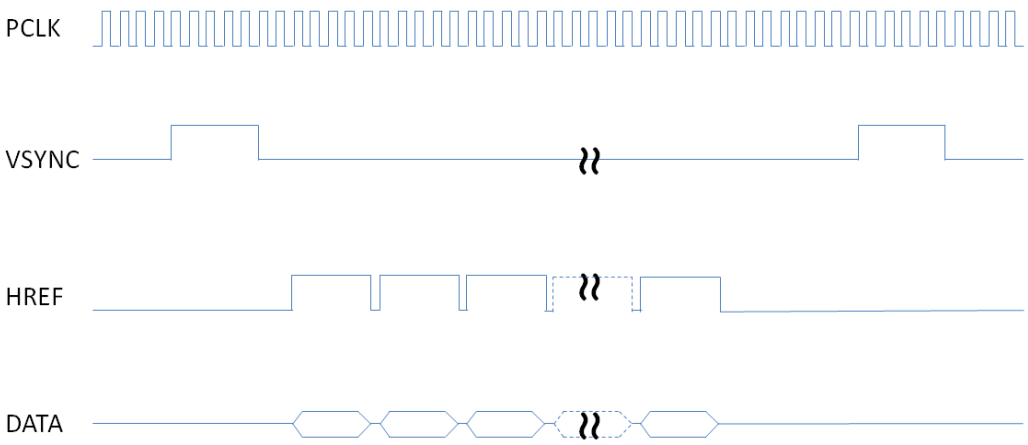


Figure 5-12. VSYNC and HREF timing diagram

When IT9910 works with frontend camera, it's common to expect sync signals: VSYNC and HREF, as shown in above. Since HREF functions as data enable instead of HSYNC, HREF needs to be connected to DE pin and sensor mode register shall be turned on to sync to this format.

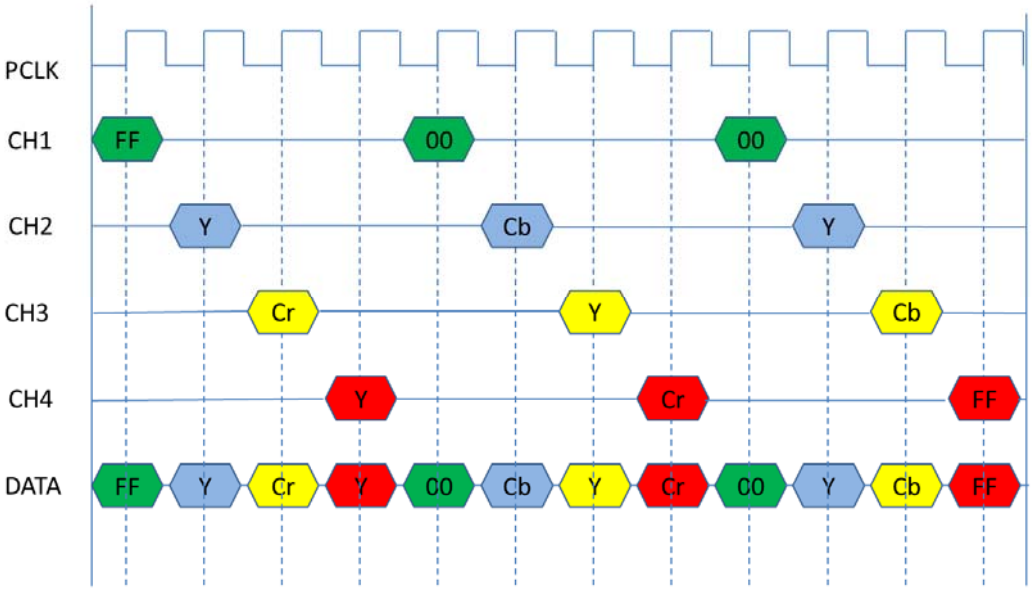


Figure 5-13. 4 channels of time-division-multiplexed

IT9910 captures up to 4 channels of time-division-multiplexed D1 BT.656 video. Each channel is byte level interleaved with separate sync signals.

5.4 H.264 Encoder

IT9919 supports high performance H.264 encoder and encodes up to Full-HD 1920x1080 resolution. H.264 encoder is fully complies with ISO/IEC-14996-10 baseline profile and from level 1.0 ~ 4.0 up to 1080p@30fps. The maximum encoding bit rate is 20Mbits.

Here are the features:

- Compatible with the ITU-T Recommendation H.264 specification.
- The encoder uses only one reference frame for the motion estimation.
- 1/4-pel accuracy motion estimation with programmable search range up to [+/-128, +/-64]
- Search range is reconfigurable by SW
  - Horizontal(-128 ~ 127), Vertical(-64 ~ 63)
  - Horizontal(-64 ~ 63), Vertical(-32 ~ 31)
  - Horizontal(-32 ~ 31), Vertical(-16 ~ 15)
  - Horizontal(-16 ~ 15), Vertical(-16 ~ 15)
- 16x16, 16x8, 8x16 and 8x8 block sizes are supported.
- Available block sizes can be configurable.
- Intra-prediction
  - Luma I4x4 Mode : 9 modes
  - Luma I16x16 Mode : 3 modes (Vertical, Horizon, DC)
  - Chroma Mode : 3 modes (Vertical, Horizon, DC)
- Minimum encoding image size is 96 pixels in horizontal and 16 pixels in vertical.
- The encoder supports the following error resilience tools
  - Video packet (fixed number of bits, and fixed number of macroblocks)
  - CIR (Cyclic intra Refresh)
  - Multi-slice structure
- FMO/ASO tool of H.264 is not supported.
- The encoder rate control is configurable
  - For low-delay and long-delay
  - Configurable from macroblock-level rate control to frame-level rate control
  - Support CBR and VBR

5.5 JPEG Encoder

The IT9910 JPEG encoder is based on the JPEG baseline standard and the arithmetic accuracy satisfies the requirement of the compatibility test of JPEG Part-2 (ISO/IEC10918-2). The parameters of luminance and chrominance quantization table are fully programmable. The Huffman tables are also fully programmable. The encoding process supports YUV 4:2:2 and 4:2:0 interleaved formats. The maximum encoding size of still image is 5M pixels. And motion JPEG is up to 1080p@30fps.

5.6 Image Signal Processor

IT9919 also provides a video scaling engine for scaling up or down to the target encoding size. Here are the features:

- Color filter effects
- Color space conversion
- Scaling engine for scaling up and down
- 2D and 3D de-interlace filter
- Sense change detection
- Motion detection
- 1 layer High color OSD

5.7 Memory Interface

The IT9910 supports 16-bit DDR and DDR2 SDRAM. The maximum memory size is 256 MB. For providing better performance, it also supports bank interleaving with tiling memory access.

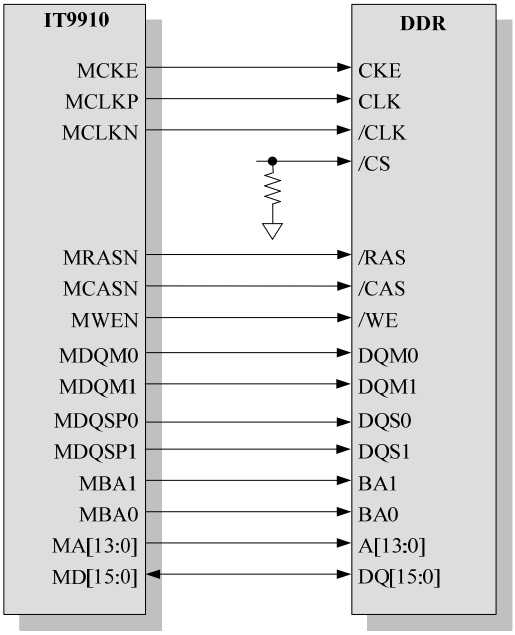


Figure 5-14. Connection of IT9910 to DDR

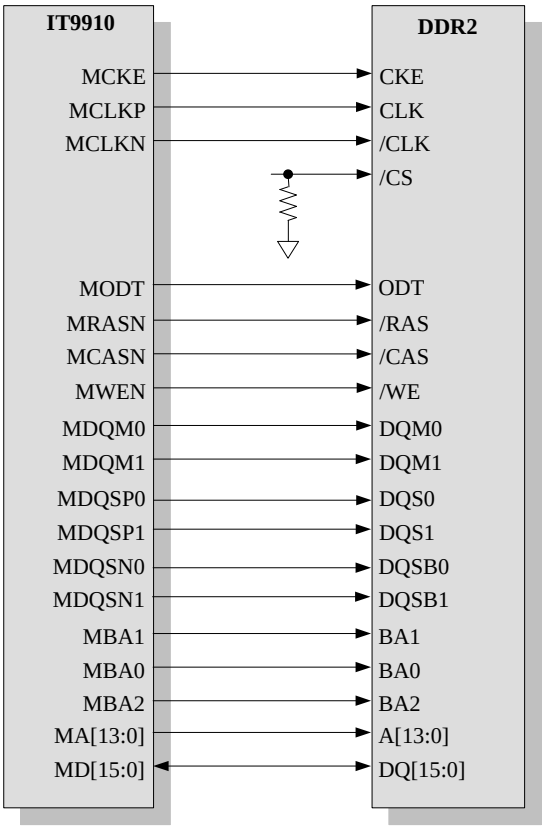


Figure 5-15. Connection of IT9910 to DDR2

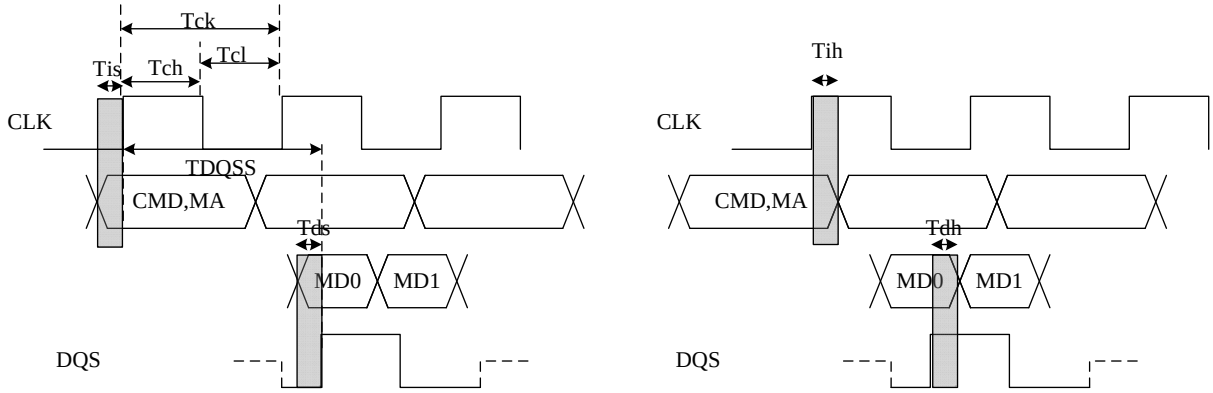


Figure 5-4. DDR Input/Output Timing

Table 5-1. DDR/DDR2 Timing Table

Symbol	Parameter	Min.	Max.	Unit
DDR				
Tck	Clock cycle Time with Latency 2,2.5,3			ns
Tch	CLK high level width			ns
Tcl	CLK low level width			ns
Tis	Address and Control input setup time			ns
Tih	Address and Control input hold time			ns
Tds	DQ and DM input hold time			ns
Tdh	DQ and DM input setup time			ns
TDQSS	Write command to first DQS latching transition			ns

5.8 Host/Device USB 2.0 Interface

This is a universal serial bus (USB) 2.0 On-The-Go (OTG) controller, which can play a dual role, either as a host or as a peripheral controller. There are two USB controllers. One is Host/Device selectable, the other is host only. For the Host/Device selectable controller, it controls which pin shares with GPIO4 on Table 4- by the ID pin. When it acts as a host, it contains a USB host controller that supports all-speed transactions. Without the software intervention, the host controller can deal with a transaction-based data structure to offload the CPU and automatically transmit and receive data on the USB bus. When it acts as a peripheral controller, each endpoint, except endpoint 0, accepts programmable HS/FS transfer types to provide a flexibility to suit all applications. In addition, complying with OTG standards means both the Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) are supported. The system bus can be a PVCI or AHB 32-bit bus interface. The transceiver interface is UTMI+ level 3, which supports the HS/FS/LS transfers and a HS/FS hub.

Table 5-5. Dynamic Characteristics of DP/DM

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
USB 2.0 transceiver (HS)						
Input levels (Differential receiver)						

V_{HSDIFF}	High-speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$ Measured at the connection as an application circuit	300	-	-	mV
V_{HSCM}	Voltage range of high-speed data signaling in the common mode		-50	-	500	mV
V_{HSSQ}	High-speed squelch detection threshold	Squelch is detected.	-	-	100	mV
		Squelch is not detected.	150	-	-	mV
V_{HSDSC}	High-speed disconnection detection threshold	Disconnection is detected.	625	-	-	mV
		Disconnection is not detected.	-	-	525	mV
Output levels						
V_{HSOI}	High-speed idle-level output voltage (Differential)		-10	-	10	mV
V_{HSOL}	High-speed low-level output voltage (Differential)		-10	-	10	mV
V_{HSOH}	High-speed high-level output voltage (Differential)		-360	-	400	mV
V_{CHIRPJ}	Chirp-J output voltage (Differential)		700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage (Differential)		-900	-	-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as the internal chip	40.5	45	49.5	Ω
Termination						
V_{TERM}	Termination voltage of the pull-up resistor on the RPU pin.		3.0	-	3.6	V
USB 1.1 transceiver (FS/LS)						
Input levels (Differential receiver)						
V_{DI}	Differential input voltage sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	Differential common-mode voltage		0.8	-	2.5	V
Input levels (single-ended receivers)						
V_{SE}	Single-ended receiver threshold		0.8	-	2.0	V
Output levels						
V_{OL}	Low-level output voltage		0	-	0.3	V
V_{HL}	High-level output voltage		2.8	-	3.6	V

Table 5-6. Static Characteristics of DP/DM

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics						

High-speed mode						
t_{HSR}	High-speed differential rise time		500	-	-	ps
t_{HSF}	High-speed differential fall time		500	-	-	ps
Full-speed mode						
t_{FR}	Rise time of DP/DM	C_L = 50 pF; 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FF}	Fall time of DP/DM	C_L = 50 pF; 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	4	-	20	ns
t_{FRMA}	Differential rise/fall time matching (t_{FR} / t_{FF})	Excluding the first transition from the idle mode	90	-	110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Low-speed mode						
t_{LR}	Rise time of DP/DM	CL = 200 pF ~ 600 pF; 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LF}	Fall time of DP/DM	CL = 200 pF ~ 600 pF; 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LRMA}	Differential rise/fall time matching (t_{LR}/t_{LF})	Excluding the first transition from the idle mode	80	-	125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from the idle mode	1.3	-	2.0	V
Driver timing						
High-speed mode						
	Driver waveform requirement	Please refer to the eye pattern of template 1 described in USB specification, Rev. 2.0.	Follow template 1			
Full-speed mode						
	Propagation delay (VI, FSE 0, OE to DP, DN)	For the detailed description of VI, FSE 0, and OE, please refer to the USB specification, Rev. 1.1.	-	-	15	ns
Low-speed mode						
Not specified: The low-speed delay time is dominated by the slow t_{LR} and t_{LF}.						
Receiver timing						
High-speed mode (Template 4, USB 2.0 spec.)						
	Data source jitter and receiver jitter tolerance	Please refer to the eye pattern of template 4 described in the USB rev	Follow template 4			

		2.0 specification.				
Full-speed mode						
$t_{PLH(rcv)}$ $t_{PHL(rcv)}$	Receiver propagation delay (DP; DM to RCV)	For the detailed description of RCV, please refer to the USB 1.1 specification.	-	-	15	ns
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to VOP, VON)		-	-	15	ns

5.9 MMC/SD Interface

5.9.1 General Description

The IT9910 support MMC/SD card for users to store the encoding A/V files. It is convenient for users to put these data to the computer or download data from the computer. The IT9910 is fully compliant with MMCA v3.3, low-voltage support, and 4-bit data of MMCA v4.0.

5.9.2 MMC/SD Interface Timing Diagram

The MMC/SD Interface Timing diagram is shown in Figure 5-5. The detailed timing description is shown in Table 5-.

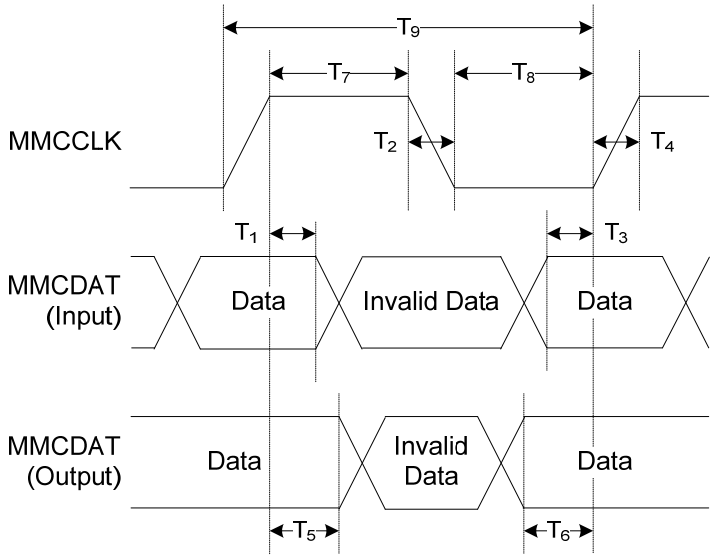


Figure 5-5. MMC/SD Interface Timing Diagram

Table 5-7. MMC/SD Interface Timing Table

Symbol	Parameter	Min	Max	Units
T1	Input Hold Time	5	-	ns
T2	Clock fall time	-	10	ns
T3	Input Setup Time	5	-	ns
T4	Clock Rise Time	-	10	ns
T5	Output Hold Time	3	-	ns

T6	Output Setup Time	3	-	ns
T7	Clock High Time	10	-	ns
T8	Clock Low Time	10	-	ns
T9	Clock Cycle Time	40	-	ns

5.10 Digital Audio Interface

5.10.1 General Description

IT9910 features a standard audio interface to support the transmission of mono or stereo data to and from the DAC or ADC. The standard audio interface support two data formats. One is standard IIS data format and the other is left justified data format. IT9910 audio interface may be configured as either master or slave. As a master interface mode, IT9910 generates the ACLK (ZCLK) and AWS (ZWS) and controls sequencing of the data transfer. In the slave mode, DAC or ADC generates the ACLK (ZCLK) and AWS (ZWS) and controls the sequencing of data transfer.

5.10.2 Digital Audio Interface Implementation

The audio interface in IT9910 has seven pins to support all the application implementation. The IT9910 can connect one DAC and one ADC. IT9910 also can connect on CODAC, it is dependents the application's purpose. There are three kinds of interface implementations, and all these can be configured as either master or slave mode.

- Implementation 1: IT9910 connect one ADC and one DAC. In this implementation, IT9910 audio interface may be configured as either master or slave. The figure below illustrates an example of this implementation in master mode.

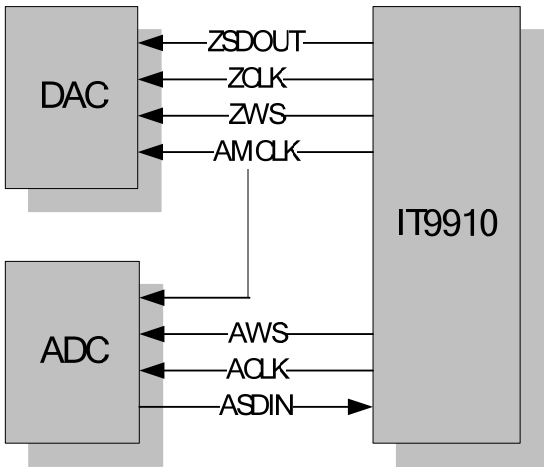


Figure 5-6. Audio Interface Implementation 1

- Implementation 2: IT9910 connect one CODEC. The CODEC only one bits clock (ACLK) and one sample clock (AWS). In this implementation, IT9910 audio interface may be configured as either master or slave. The figure below illustrates an example of this implementation in master mode.

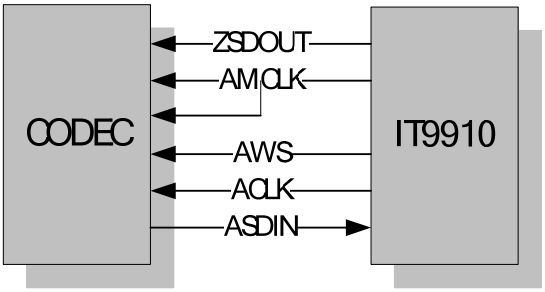


Figure 5-7. Audio Interface Implementation 2

- Implementation 3: IT9910 connect one CODEC. The CODEC only one bits clock (ACLK) and two sample clock (AWS, ZWS). In this implementation, IT9910 audio interface may be configured as either master or slave. The figure below illustrates an example of this implementation in master mode.

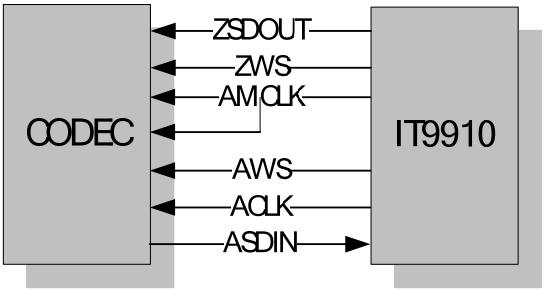


Figure 5-20. Audio Interface Implementation 3

5.10.3 Audio Interface Data Formats

IT9910 supports IIS and left justified audio interface data formats.

In IIS mode, The MSB is available on the second rising edge of ACLK following the AWS transition. The other bits up to LSB are then transmitted in order. The figure below illustrates the IIS interface.

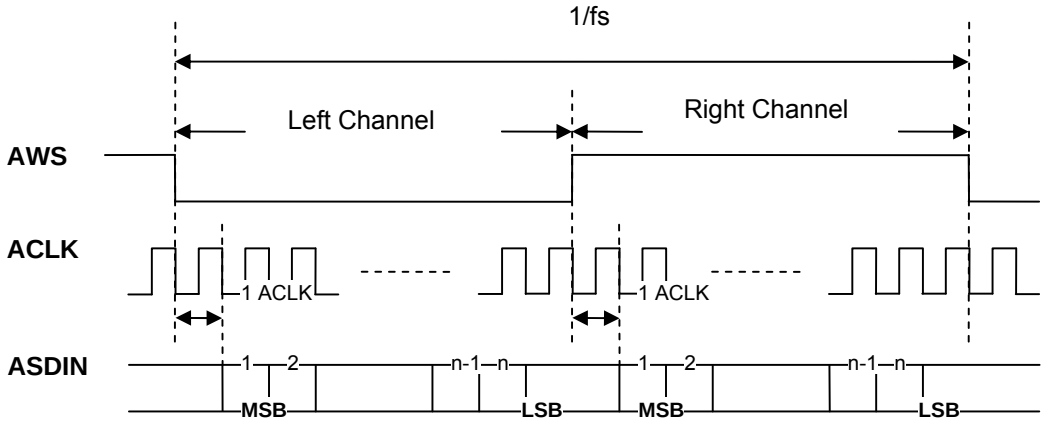


Figure 5-21. IIS Audio Interface

In Left justified mode, The MSB is available on the first rising edge of ACLK following the AWS transition. The others bits up to LSB are then transmitted in order. The figure below illustrates the IIS interface.

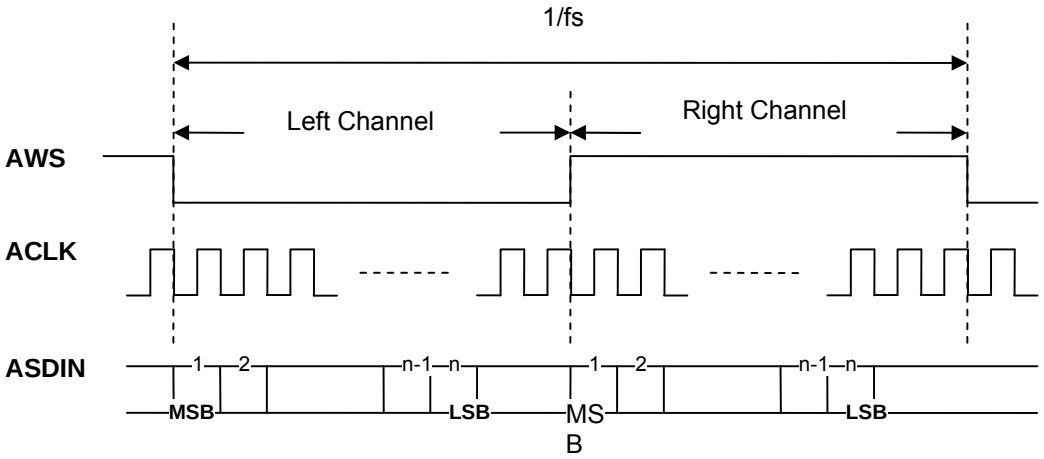


Figure 5-22. MSB Left Justified Interface

5.11 MPEG TS interface

For IT9910, the MPEG TS interface only can operate in serial mode. The payloads of transport stream will be serially output on MPEG Data pin. The output bit order can be MSB first or LSB first. MPEG Sync can be asserted at the first bit or first of the payload of the transport stream. And Clock, Sync, Valid can be independently configured to be active high or low. The timing diagrams of MPEG TS interface are shown in Figure 5-32 and Figure 5-24. Table 4- shows the pin share for MPEG TS interface pins.

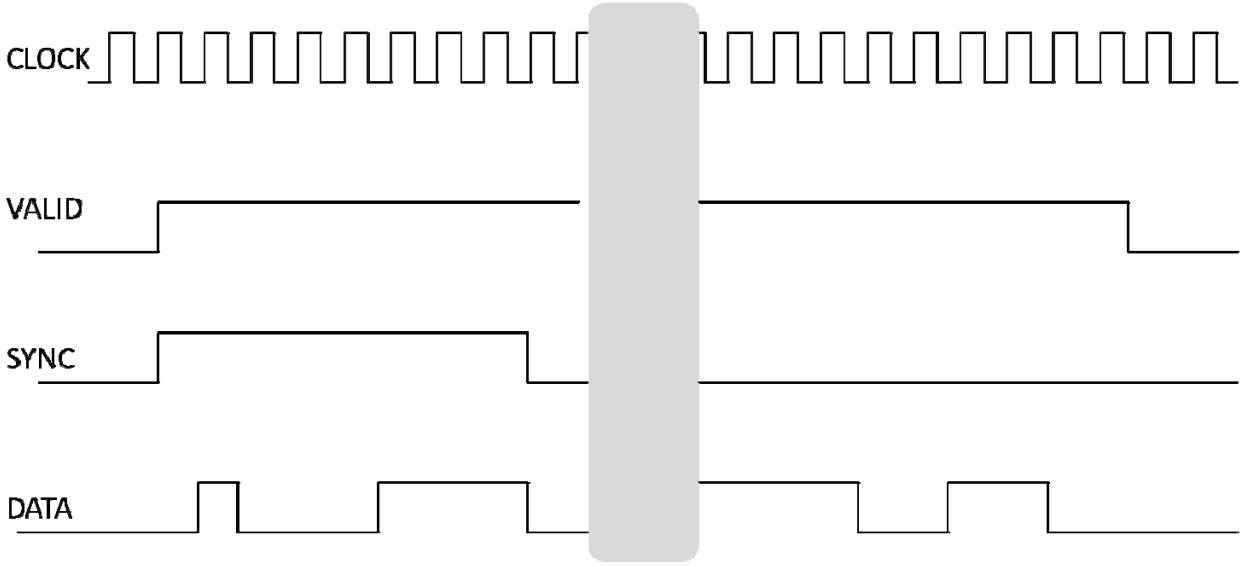


Figure 5-8. Timing Diagram of TS Interface when one Byte SYNC

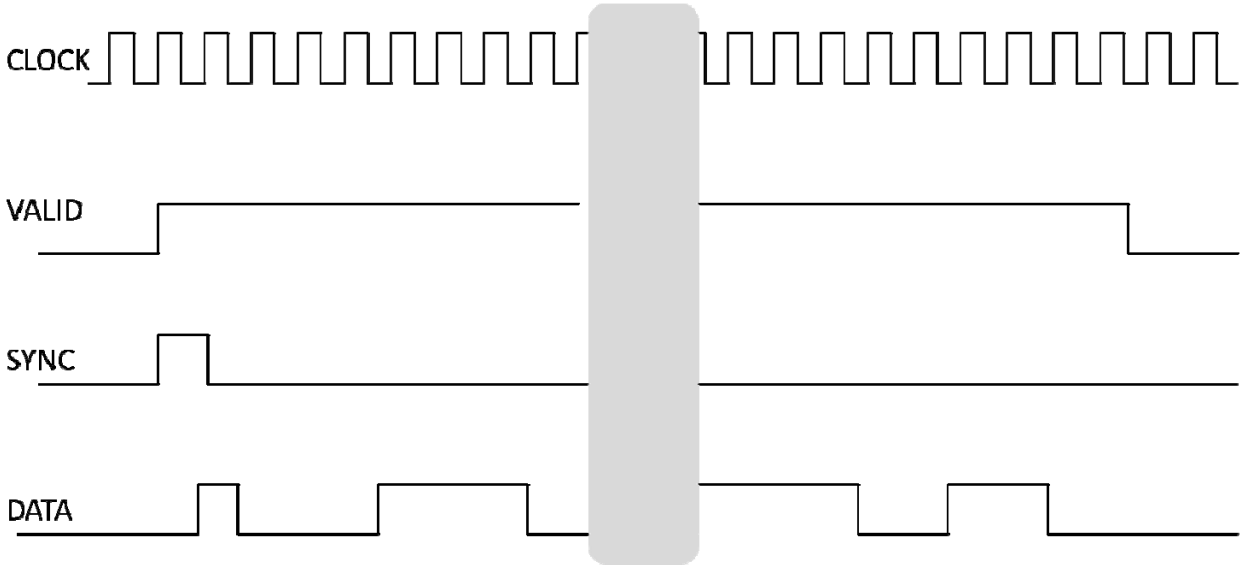


Figure 5-9. Timing Diagram of TS Interface when one Byte SYNC

5.12 UART and IrDA Interface

The UART and IrDA controller is a serial communication element that implements the most common infrared communication protocols. In addition to the infrared modes, the device also provides a UART mode of operation that is backward compatible to 16550 to support the existing communication software.

The following figure shows the block diagram of UART and IrDA communication controller.

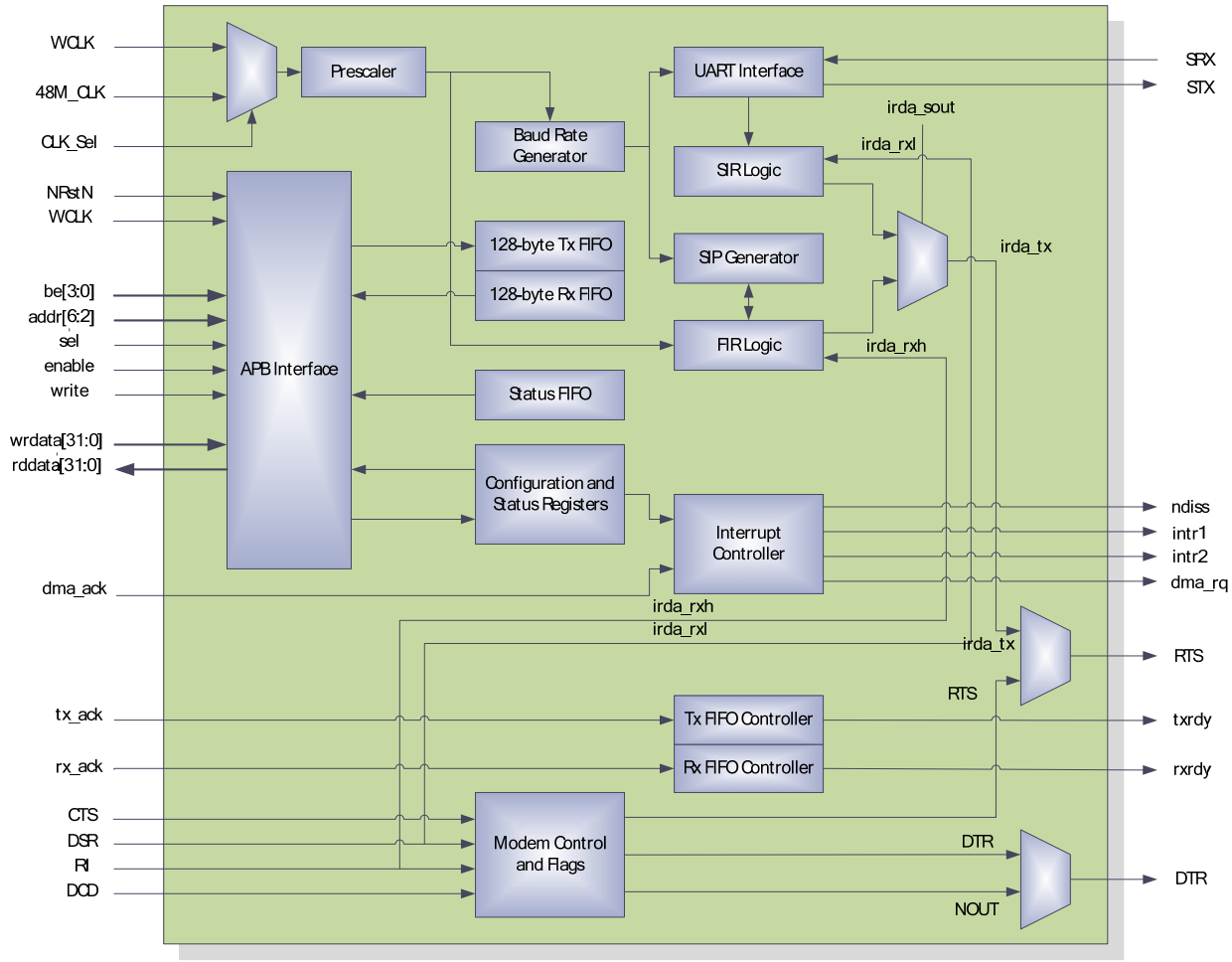


Figure 5-25. Block Diagram of UART and IrDA Controller

It provides the following features:

- Firmware compatible with the high-speed NS 16C550A UART
- IrDA 1.3 SIR with up to 115.2 kbps data rate
- SIR pulse width programmable as 1.6 µs or 3/16 of the baud-rate pulse width
- Supports IrDA 1.3 FIR
- Multi-frame transmission and reception in the FIR mode
- Back-to-back infrared frame transmission and reception in the FIR mode
- 32-bit IEEE 802 CRC32 hardware CRC generators and checkers for the FIR communications
- Break, parity, overrun, and framing error simulations in the UART mode
- CRC error and physical error simulation in the FIR mode

5.13 SPI Interface

SPI is a synchronous serial port interface that allows the host processors to serve as a master or a slave. It can

connect to various devices by using serial protocol. The SPI controller can directly use the on-chip DMA to transfer data between the external serial device and system memory without intervention from the processor. IT9910 has two SPI controller and one of SPI controller is connected to external NOR.

Table 5-8. NOR Interface AC Timing

Symbol	Alt	Parameter	Min	Typ	Max	Units
F_{clk}		Serial Clock Frequency	D.C.		40	MHz
t_{CH}		Serial Clock High Time	12.5			ns
t_{CL}		Serial Clock Low Time	12.5			ns
t_{CLCH}		Serial Clock Rise Time (Slew Rate)	0.2			V/ns
t_{CHCL}		Serial Clock Fall Time (Slew Rate)	0.2			V/ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time	5			ns
t_{CHSH}		CS# Active Hold Time	5			ns
t_{SHSL}	t_{CSH}	CS# High Time	100			ns
t_{CLQX}	t_{HO}	Input Hold Time	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	4			ns
t_{CHDX}	t_{DH}	Data In Hold Time	4			ns
t_{CLQV}		t_V Output Valid from SCK			6	ns

Notes: $t_{CLH} + t_{CLL}$ must greater than $1 / F_{CLK}$

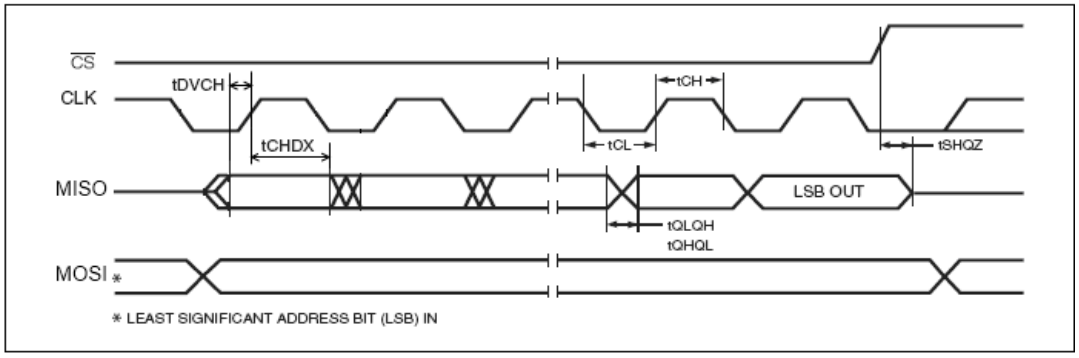


Figure 5-10. Serial Input Timing

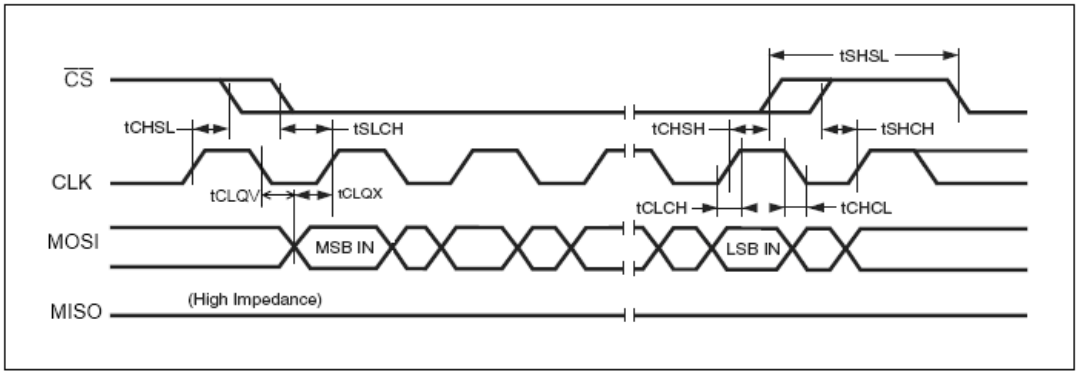


Figure 5-11. Serial Output Timing

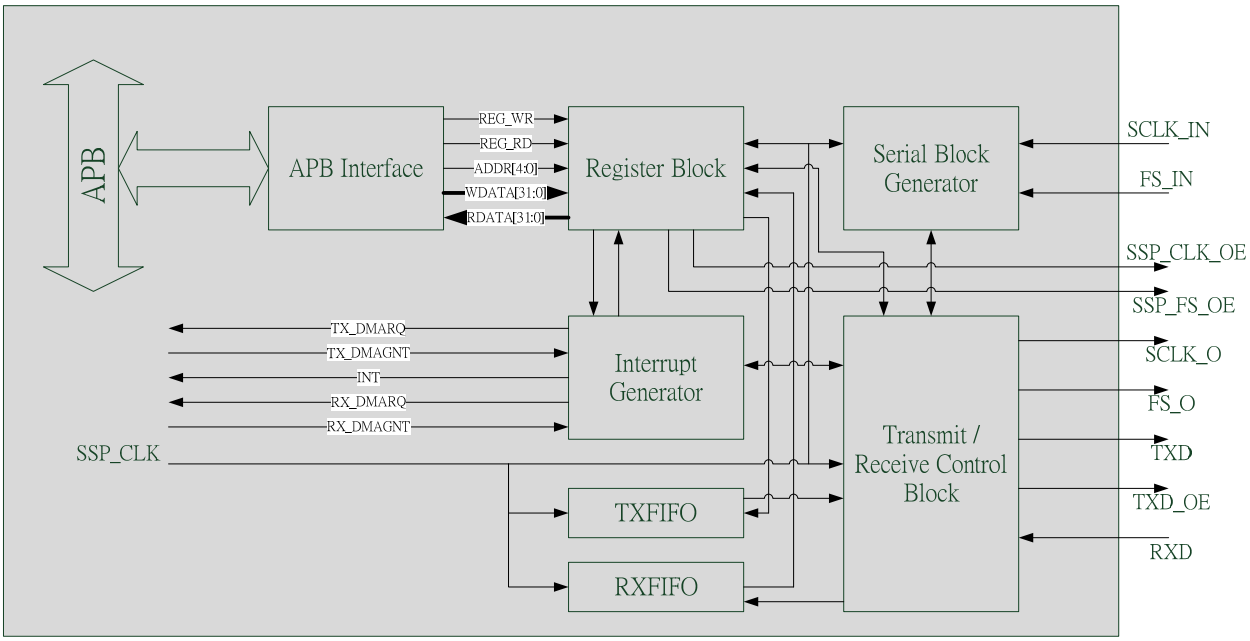


Figure 5-12. Block Diagram of NOR Interface

5.14 DMA Controller

IT9910 Direct Memory Access Controller is designed to enhance system performance and reduce processor-interrupt generation. System efficiency is improved by employing high-speed data transfers between the system and device. The DMA controller provides 8 channels for memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfer with a shared buffer.

The following figure illustrates the functional block diagram of the DMA controller.

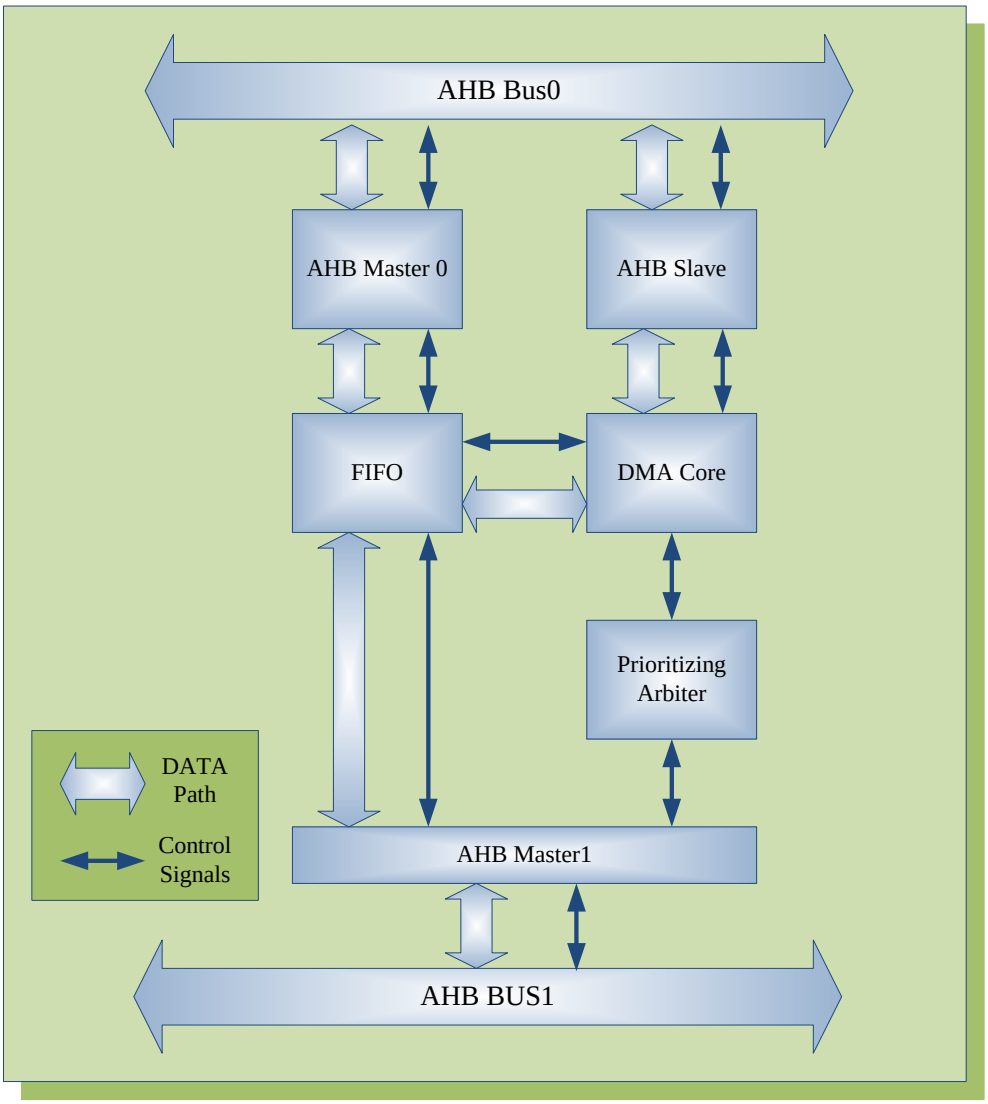


Figure 5-13. Block Diagram of DMA Controller

The main feature is :

- An AHB slave port for DMA controller configuration
- 2 AHB master interfaces for data transfer
- 8 configurable DMA channels
- Supports chain transfer
- Memory-to-memory, memory-to-peripheral, and peripheral-to-memory transfers
- Group round-robin arbitration scheme with 4 priority levels
- Supports 8-, 16-, and 32-bit wide data transaction
- Supports big-endian and little-endian

5.15 Ethernet MAC Interface

The IT9910 provides a high-quality 10/100 Ethernet controller with DMA function. It includes an AHB wrapper, DMA engine, on-chip memories (TX FIFO and RX FIFO), MAC, and RMII interface. It is an Ethernet controller

that provides AHB master capability and is fully compliant with the IEEE 802.3 100 Mbps and 10 Mbps specifications. The MAC DMA controller handles all data transfers between system memory and on-chip memories. The DMA engine supports the zero-copy data transfer that drastically improves the system performance. The DMA engine can be used to reduce the CPU loading, maximize the performance, and minimize the FIFO size. It has on-chip memories for buffering, which requires no external local buffer memory. The RMII interface can support two specific data rates, 10 Mbps and 100 Mbps. The functionality is identical at both data rates, and so is the signal timing relationship. The only difference between the 10 Mbps and 100 Mbps operations is the nominal clock frequency.

5.16 PLL Interface

IT9910 has three clock synthesizers to generate all of the internal clocks. The clock synthesizer can generate wide range of programmable frequencies up to 440MHz. The clock synthesizer accepts 12 MHz reference clock input. And system can even stop the reference clock after the PLL locked the target frequency and phase for power saving.

5.17 General-Purpose I/O

The GPIO controller is a user programmable general-purpose I/O controller. It is used to input/output data from the system and device. Each GPIO can be programmed as the input or output, pulled high or pulled low.

This GPIO can also be an interrupt input. It supports the rising edge, falling edge, both edge, and high/low level interrupt sense types. Each port can choose the pre-scale APB clock source as an interrupt source.

All the inputs are set to input upon the hardware reset.

The GPIO (general-purpose I/O) signals can be used to control and receive external devices or events. Table 4- shows the pin share for each GPIO pins.

6. Memory Mapping

There are two kinds of memory mapping. One is by host view, and other is by RISC view.

On the host view, the memory is divided into two parts. One is mapped to the IT9910 internal registers, which is so-called Memory Map IO (MMIO) space while the other is mapped to the external memory.

On the RISC view, all of address space (MMIO, and memory) is mapped by the linear address. On the base address 0xC000_0000, which is mapped to the MMP's engine, it should access by 16-bits data type in such address space. On the other address space, it should access by 32-bits data type. Please refer **Table 6-1**for the detailed memory mapping.

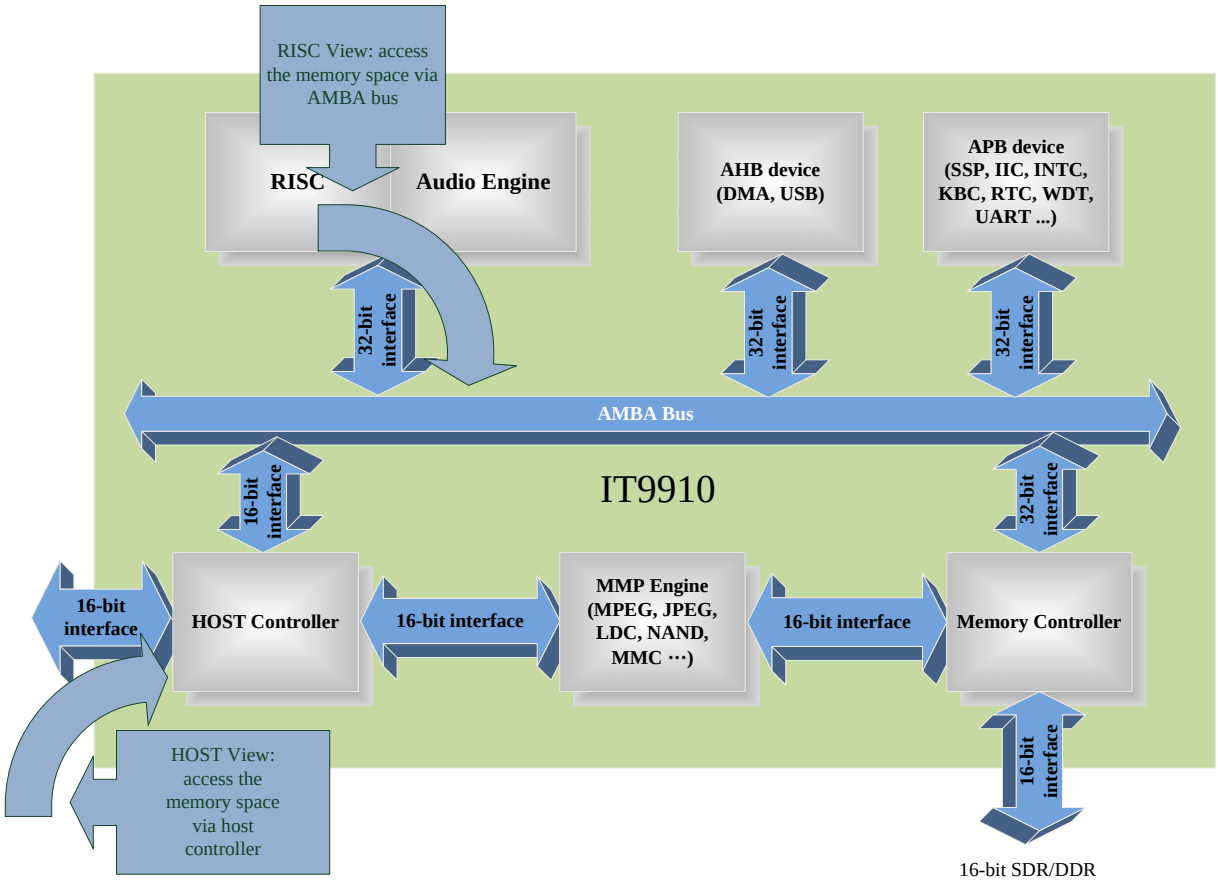


Figure 6-1. Architecture Memory View

Memory Map

APB Map	Host Map	Memory Map before booting	Memory Map after booting
0x0000_0000		NAND/ROM	Memory
0x8000_0000		Memory	ROM
0xC000_0000		MMP Engine	MMP Engine
0xC010_0000		SRAM on ISP (6144 bytes)	SRAM on ISP (6144 bytes)
0xC020_0000		SRAM (for audio) (8192 bytes)	SRAM (for audio) (8192 bytes)
0xD000_0000	0x5400	AHB layer 0	AHB layer 0
0xD010_0000	0x5800	AHB layer 1	AHB layer 1
0xD020_0000	0x5C00	DMA	DMA
0xD030_0000	0x6000	APB bridge	APB bridge
0xD040_0000	0x6400	USB 0	USB 0
0xD050_0000	0x6800	USB 1	USB 1
0xD060_0000	0x6C00	Reserved	Reserved
0xD070_0000	0x7000	Reserved	Reserved
0xD080_0000	0x7400	Ethernet	Ethernet
0xD090_0000	0x7800	DPU	DPU
0xD0A0_0000	(0xB800)	H.264 Encoder	H.264 Encoder
0xDE00_0000	0x7C00	GPIO	GPIO
0xDE10_0000	0x8000	I2C	I2C
0xDE20_0000	0x8400	Interrupt	Interrupt
0xDE30_0000	0x8800	Keypad/Mouse	Keypad/Mouse
0xDE40_0000	0x8C00	Reserved	Reserved
0xDE50_0000	0x9000	RTC	RTC
0xDE60_0000	0x9400	UART0	UART0
0xDE70_0000	0x9800	UART1	UART1
0xDE80_0000	0x9C00	SSP0	SSP0
0xDE90_0000	0xA000	SSP1	SSP1
0xDEA0_0000	0xA400	Timer	Timer
0xDEB0_0000	0xA800	Watch Dog	Watch Dog
0xDEC0_0000	0xAC00	Remote IR	Remote IR
0xDEE0_0000	0xB000	SD	SD

0xC000_0000 MMP Engine	
0x0000	General Setting
0x0100	Reserved
0x0200	Host
0x0300	DDR/DDR2
0x0400	ISP
0x0900	USB
0x0A00	JPEG
0x0C00	Reserved
0x1000	TSI
0x1080	Reserved
0x1100	Reserved
0x1400	Reserved
0x1500	Reserved
0x1600	IIS
0x1680	RISC0/RISC1
0x1700	RISC2
0x1A00	Reserved
0x1D00	Reserved
0x1F00	Reserved
0x2000	Capture
0x2100	TSM

Table 6-1. Memory Map

7. DC Characteristics

Absolute Maximum Ratings

Core Power (IVDD) ..... -0.3V to 2.0V
I/O Power (OVDD) ..... -0.3V to 4.0V
Input Voltage ... -0.3V to OVDD+10%
Output Voltage .. -0.3V to OVDD + 10%
Storage Temperature ..... -40°C to 125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Normal Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_{CORE}	Core Power (IVDD)	1.25	1.35	1.45	V
MOVDD	DDR1 Memory Power	2.3	2.5	2.7	V
	DDR2 Memory Power	1.7	1.8	1.9	V
OVDD	I/O Power	3.0	3.3	3.6	V
-	Operating Temperature	0	-	70	^0C

DC Electrical Characteristics

Symbol	Parameter	Condition.	Min.	Max.	Unit
V_{OL}	Output low voltage	Refer to I_{OL}	OVSS	OVSS+0.4	V
V_{OH}	Output high voltage	Refer to I_{OH}	OVDD-0.4	OVDD	V
I_{OH_S}	Output high current (with maximum driving strength)	OVDD = 3.3V V_{OH}= 2.9V	3.03	5.58	mA
I_{OL_S}	Output low current (with maximum driving strength)	OVDD = 3.3V V_{OL}= 0.4V	3.60	5.59	mA
I_{OH_W}	Output high current (with maximum driving strength)	OVDD = 3.3V V_{OH}= 2.9V	1.20	2.23	mA
I_{OL_W}	Output Low Current (with maximum driving strength)	OVDD = 3.3V V_{OL}= 2.9V	1.44	2.23	mA
I_{OZ}	Tri-state Leakage Current	-	-	± 10	uA
V_{IL}	Input Low Voltage	OVDD=3.3V	-	1.35	V
V_{IH}	Input High Voltage	OVDD=3.3V	1.95	-	V
I_{IN}	Input Leakage Current	-	-	± 10	uA
C_{IN}	Input Capacitance	-	-	3	pF

8. AC Characteristics

8.1 Reset Timing

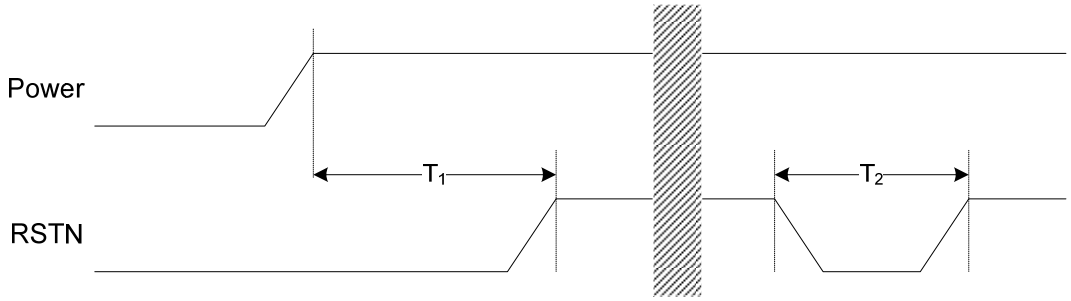


Figure 8-1. Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	Power valid to reset inactive	1	-	-	ms
T_2	Minimum reset pulse width	1	-	-	ms

Table 8-1. Reset Timing Table

Notes: The registers can be accessed 4 ms after the reset process is finished.

8.2 Power Sequence

Specific sequencing requirements shall be followed for all I/O power and core power.

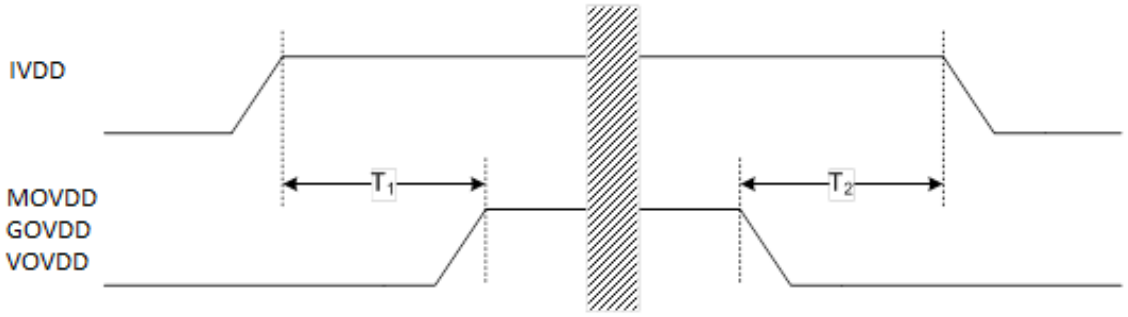


Figure 8-2. Power Sequence Timing

Table 8-2. Power Sequence Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_1	Core power valid to I/O power valid	10	-	-	us
T_2	I/O power invalid to core power invalid	10	-	-	us

9. Power Consumption

9.1 AV Sender

The current consumption in normal full operation mode while streaming A/V signal by DVB-T air signal is listed in Table 9-1.

The test conditions are:

1. Engine frequency is 200MHz and Memory frequency is 440MHz.
2. HDMI 1920x1080@60P input.
3. HDMI 1920x1080@60P pass through.
4. Video format is H.264 1920x1080@30P and bitrate is 18Mbits.
5. Audio format is MPEG Audio and bitrate is 256Kbits.
6. IT9057 is operated @64QAM, 7/8CR, 1/32 GI, 6MHz, 8K.

Table 9-1. AV sender operation mode power consumption

IT9057	HDMI Pass through	Video Format	IVDD 1.3V (mA)	MOVDD 1.8V (mA)	VDD 3.3V (mA)	VDD 5V (mA)	Total Power (mW)
ON	ON	1080i60	580	120	290	910	4550
		1080p60	620	130	330	960	4800
	OFF	1080i60	570	120	260	840	4200
		1080p60	610	130	270	880	4400
OFF	ON	1080i60	580	120	190	820	4100
		1080p60	590	120	210	880	4400
	OFF	1080i60	560	120	160	760	3800
		1080p60	580	120	170	800	4000

9.2 Grabber Box

The current consumption in normal full operation mode while recording A/V data to USB storage in Table 9-2. And Table 9-3.

The test conditions of Mode 1 are:

1. Engine frequency is 200MHz and Memory frequency is 440MHz.
2. HDMI 1920x1080@60P input.
3. HDMI 1920x1080@60P pass through.
4. Video format is H.264 1920x1080@30P and bitrate is 18Mbits.
5. Audio format is MPEG4 AAC-LC Audio and bitrate is 192Kbits.
6. File container is MP4 file format.

Table 9-2. Grabber box operation mode 1 power consumption

USB Storage	VDD 5V (mA)	Total Power (mW)
32G USB pen drive	750	3750
500G USB 3.0 Hard Disk	1100	5500

The test conditions of Mode 2 are:

1. Engine frequency is 200MHz and Memory frequency is 440MHz.
2. YPbPr 1920x1080@60P input and Analog audio input
3. HDMI 1920x1080@60P pass through.
4. Video format is H.264 1920x1080@30P and bitrate is 18Mbits.
5. Audio format is MPEG4 AAC-LC Audio and bitrate is 192Kbits.
6. File container is MP4 file format.
7. YPbPr A/D is CAT9883

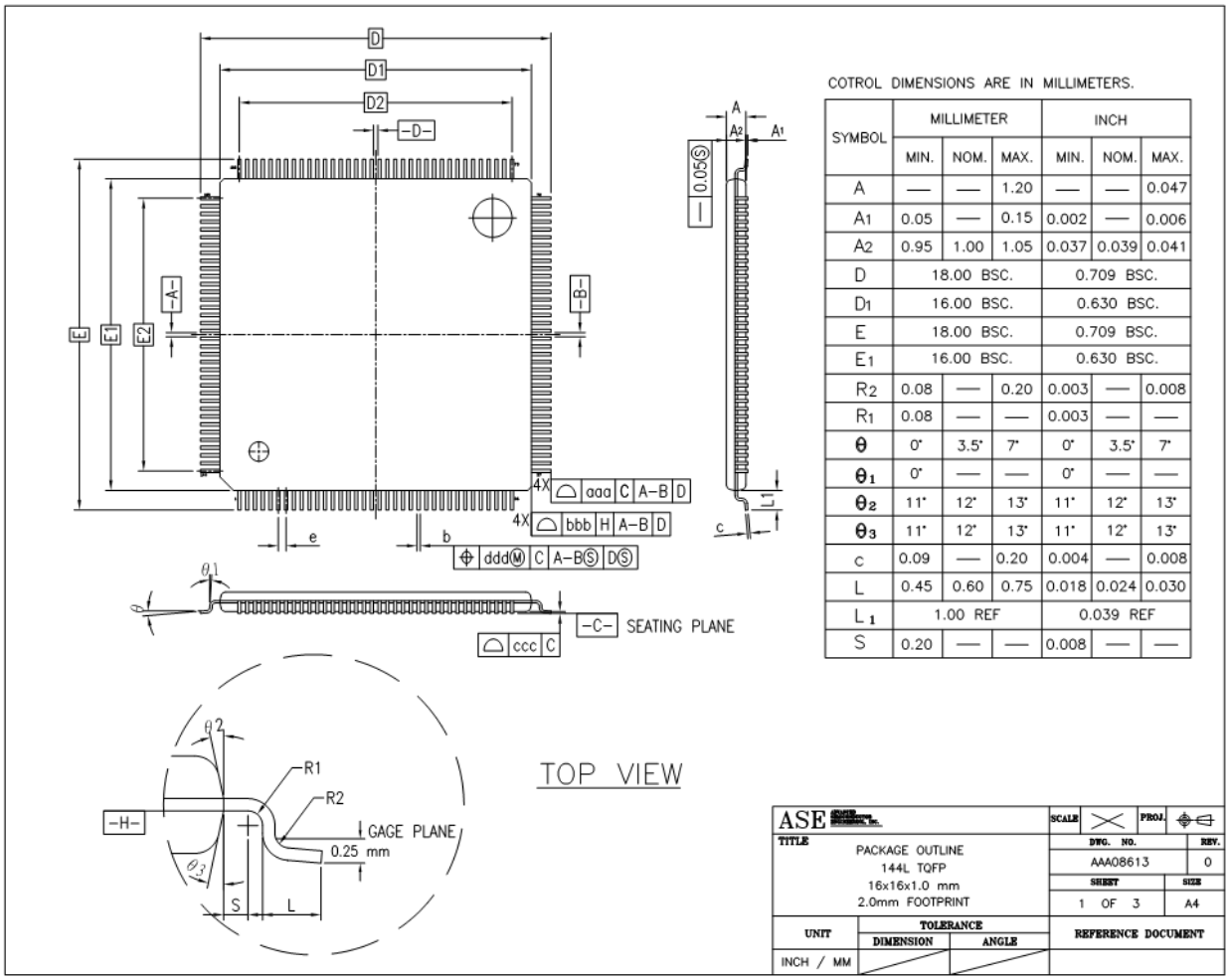
Table 9-3. Grabber box operation mode 2 power consumption

USB Storage	VDD 5V (mA)	Total Power (mW)
32G USB 2.0 pen drive	850	4250
32G USB 3.0 pen drive	950	4750

10. Package Information

IT9919 Package Information

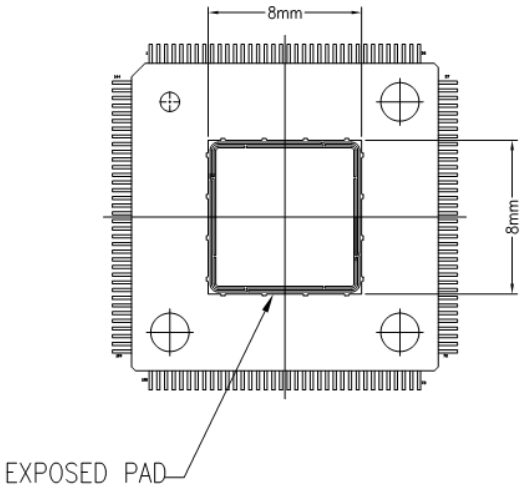
TQFP 144 Outline Dimensions unit: inches/mm



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.00 BSC.			0.709 BSC.		
D_1	16.00 BSC.			0.630 BSC.		
E	18.00 BSC.			0.709 BSC.		
E_1	16.00 BSC.			0.630 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

ASE		SCALE	PROJ.
TITLE: PACKAGE OUTLINE 144L TQFP 16x16x1.0 mm 2.0mm FOOTPRINT		DWG. NO.	REV.
		AAA08613	0
		SHEET 1 OF 3	SIZE A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE	REFERENCE DOCUMENT	



BOTTOM VIEW

SYMBOL	144L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	14.00			0.551		
E2	14.00			0.551		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

ASE	SCALE	PROJ.	
TITLE: PACKAGE OUTLINE 144L TQFP 16x16x1.0 mm 2.0mm FOOTPRINT	DWG. NO.		REV.
	AAA08613		0
	SHEET		SIZE
	2 OF 3		A4
UNIT: INCH / MM	TOLERANCE: DIMENSION / ANGLE		REFERENCE DOCUMENT

11. Ordering Information

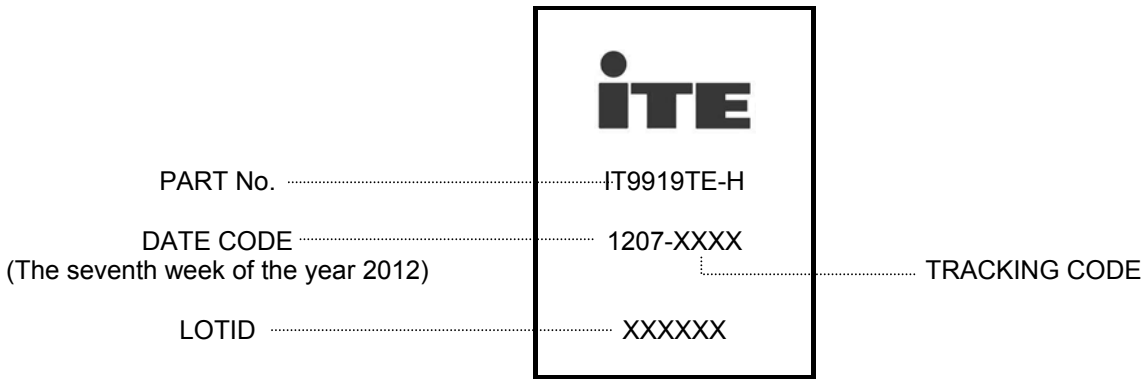
Part Number	Description	Package	Body Size
IT9919TE-H	High performance H.264 Encoder SOC w/ HDMI RX and HDCP Key	144 pins TQFP/EPAD	16*16 mm
IT9919TE-N	High performance H.264 Encoder SOC w/ HDMI RX	144 pins TQFP/EPAD	16*16 mm
IT9919TE	1080@30P High Performance H.264 Encoder SOC	144 pins TQFP/EPAD	16*16 mm
IT9917TE	720@30P High Performance H.264 Encoder SOC	144 pins TQFP/EPAD	16*16 mm
IT9917TE-H	720@30P High Performance H.264 Encoder SOC w/ HDMI RX and HDCP Key	144 pins TQFP/EPAD	16*16 mm

All components provided are RoHS-compliant (100% Green Available).

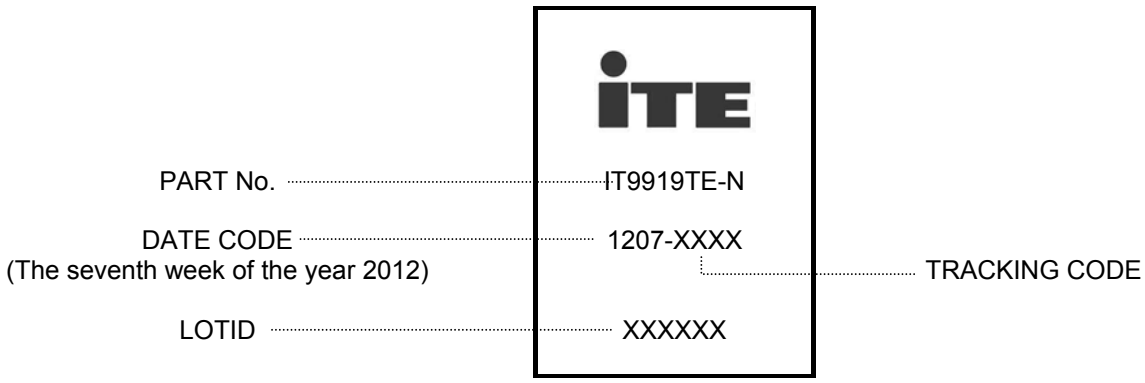
This page is intentionally left blank.

12. Top Marking Information

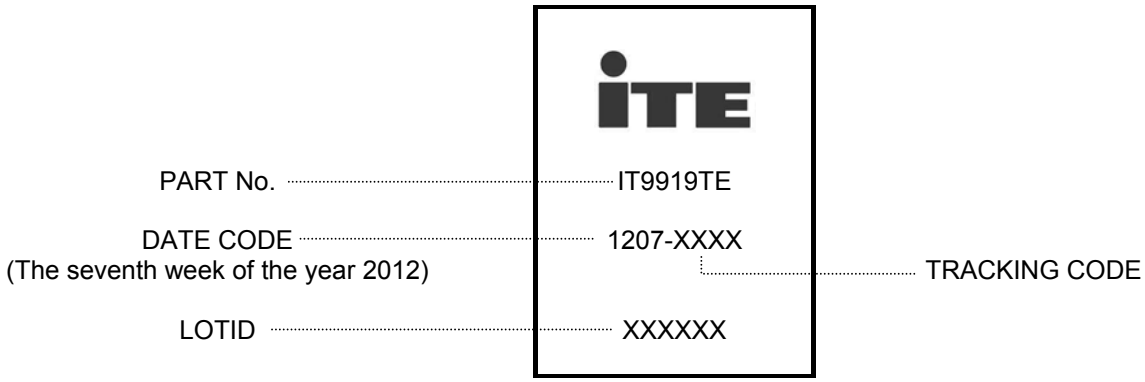
IT9919TE-H



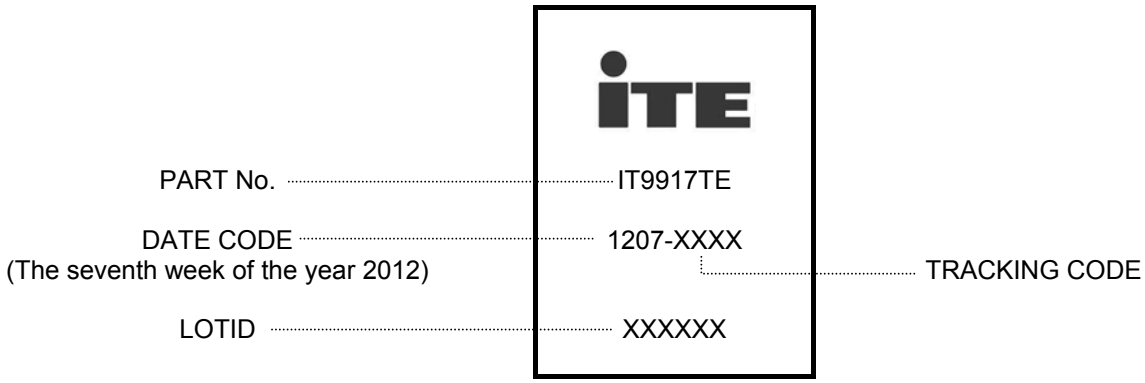
IT9919TE-N



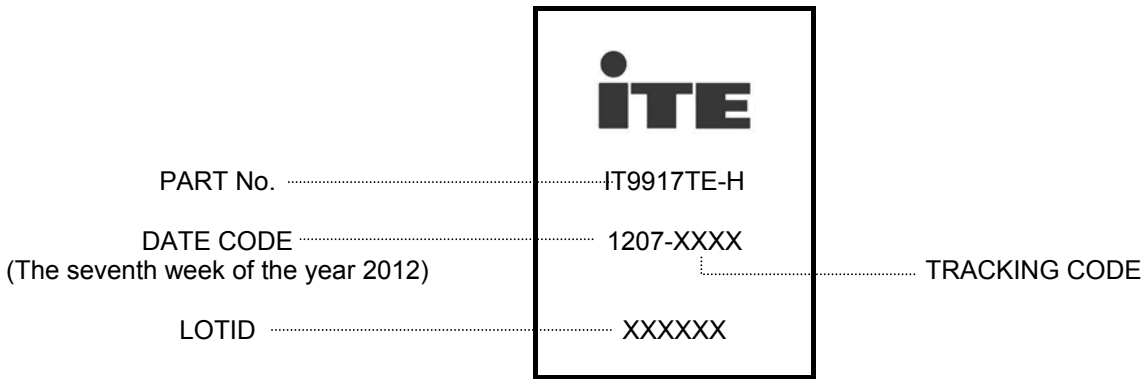
IT9919TE



IT9917TE



IT9917TE-H



ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.

(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.

(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.

(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.

(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).

(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.

(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.

(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.

(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.

(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.

(c) Buyer will not return any goods without first obtaining a customer return order number.

(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.

(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement.

Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.

(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.