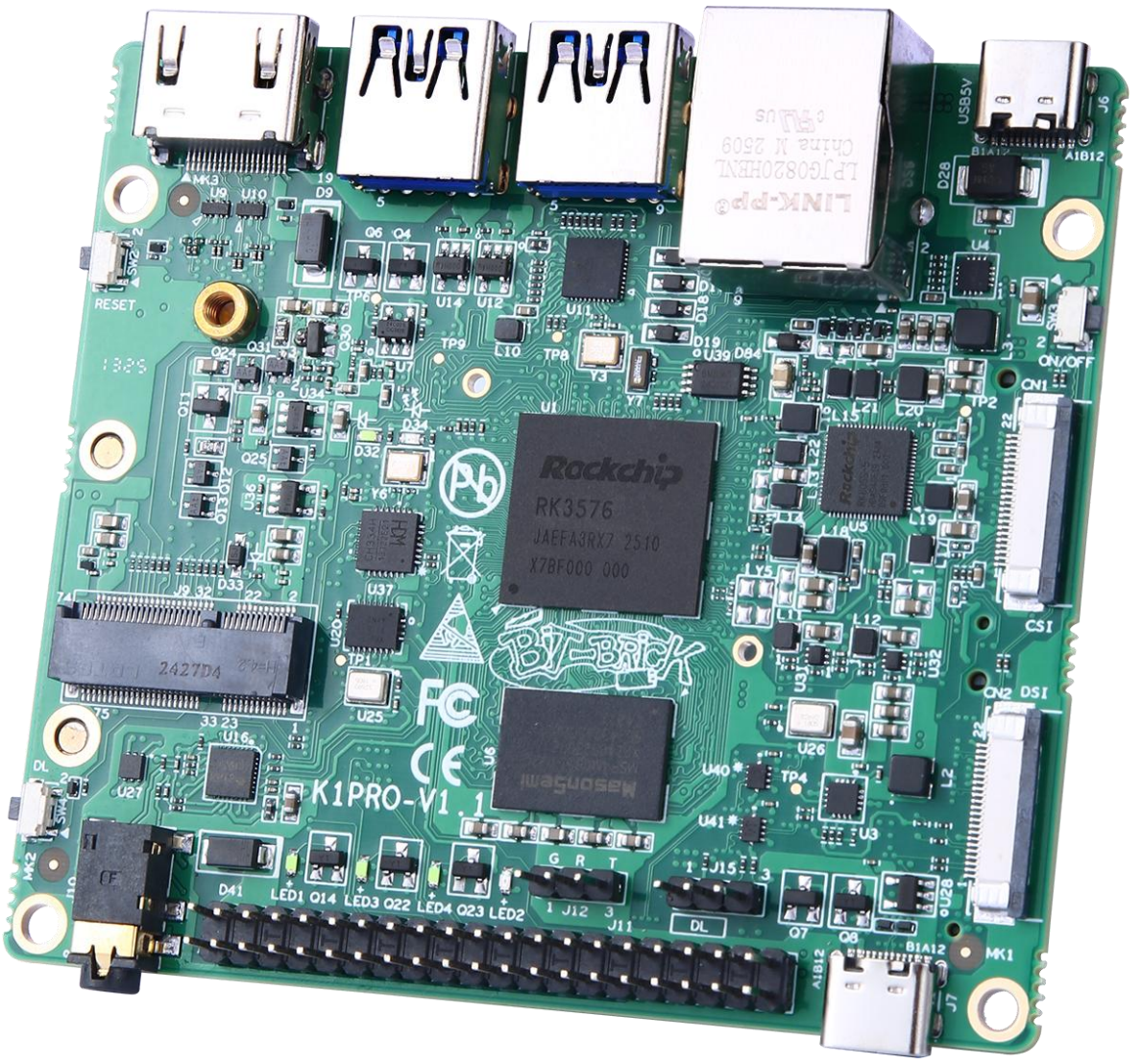
Bit-Brick K1 Pro
datasheet



Provisional version

V 1.0

Bit Brick Technology Corporation

March 5, 2025

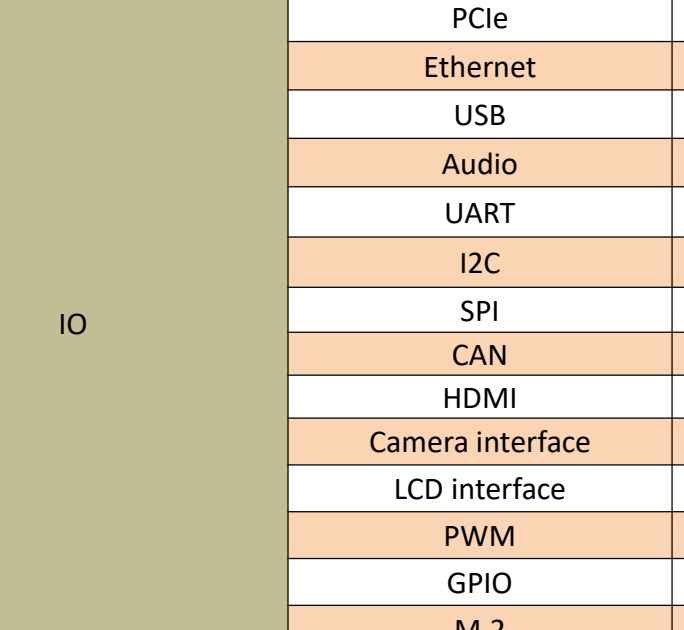
1. introduction

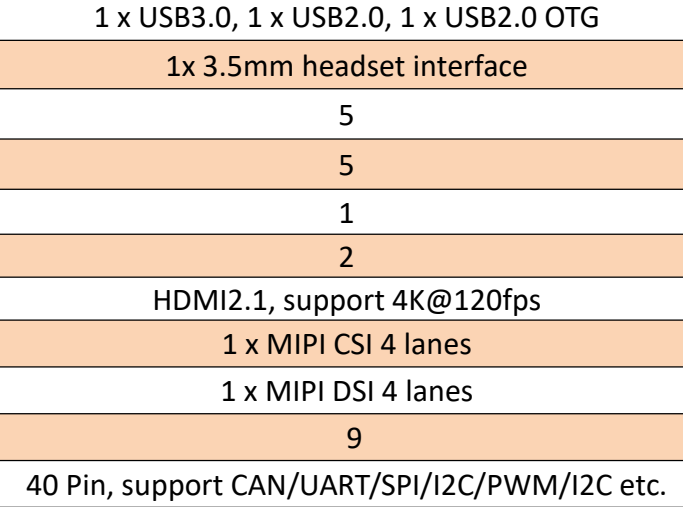
BIT-BRICK K1 Pro is a single-board computer based on the RK3576 application processor of Rockchip. The motherboard integrates large-capacity high-speed memory, eMMC Flash, Gigabit Ethernet, high-definition digital display interface, USB3.0 and USB2.0 interfaces, supports dual NVME solid-state drive interfaces, and supports a rich variety of bus interface expansions. K1 Pro is suitable for the different requirements of different people for learning computing technology.

2. Specifications

Form factor	Specification	
Processor	CPU	RK3576
	GPU	ARM Mali-G52 MC3
	NPU	6 TOPS@INT8,support INT4/INT8/INT16/FP16/BF16/TF32 hybrid operation
Memory	RAM	LPDDR4X SDRAM (4GB/8GB available)
	FLASH	eMMC flash ,maximum size up to 64GB
Graphic	Graph engine	ARM Mali-G52 MC3,Support OpenGL ES 1.1/ 2.0/3.2, OpenCL 2.0 and Vulkan 1.1
IO	PCIe	2 x PCIe 2.0 2 lanes for fast peripherals, support NVME SSD
	Ethernet	1 x Gigabit Ethernet
	USB	1 x USB3.0, 1 x USB2.0, 1 x USB2.0 OTG
	Audio	1x 3.5mm headset interface
	UART	5
	I2C	5
	SPI	1
	CAN	2
	HDMI	HDMI2.1, support 4K@120fps
	Camera interface	1 x MIPI CSI 4 lanes
	LCD interface	1 x MIPI DSI 4 lanes
	PWM	9
	GPIO	40 Pin, support CAN/UART/SPI/I2C/PWM/I2C etc.
	M.2	1 x M.2 KEY-E for modules, 2 x M.2 KEY-M
Power supply	Power Supply Voltage	Fixed 5V DC source
Environment	Operating Temperature	-40 ~ 85 °C
	Operating Humidity	95% relative humidity, non-condensing
Mechanical	Dimensions (W x D)	90 X 80 mm
Operation System		Linux/Android
Certifications		CE/FCC Class B

3. Functional Block Diagram





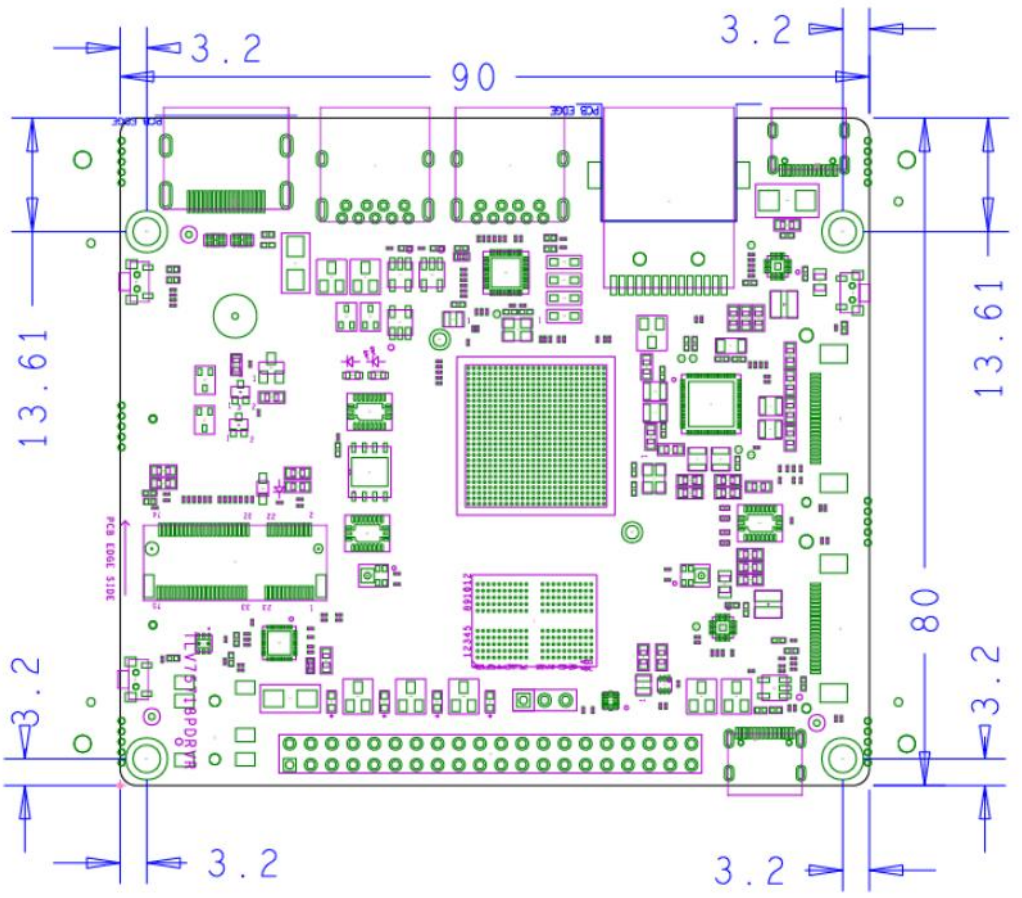
All product specifications are subject to change without notice.

Last updated: 5-Mar-2025

4. Dimension Specifications

Board Dimensions

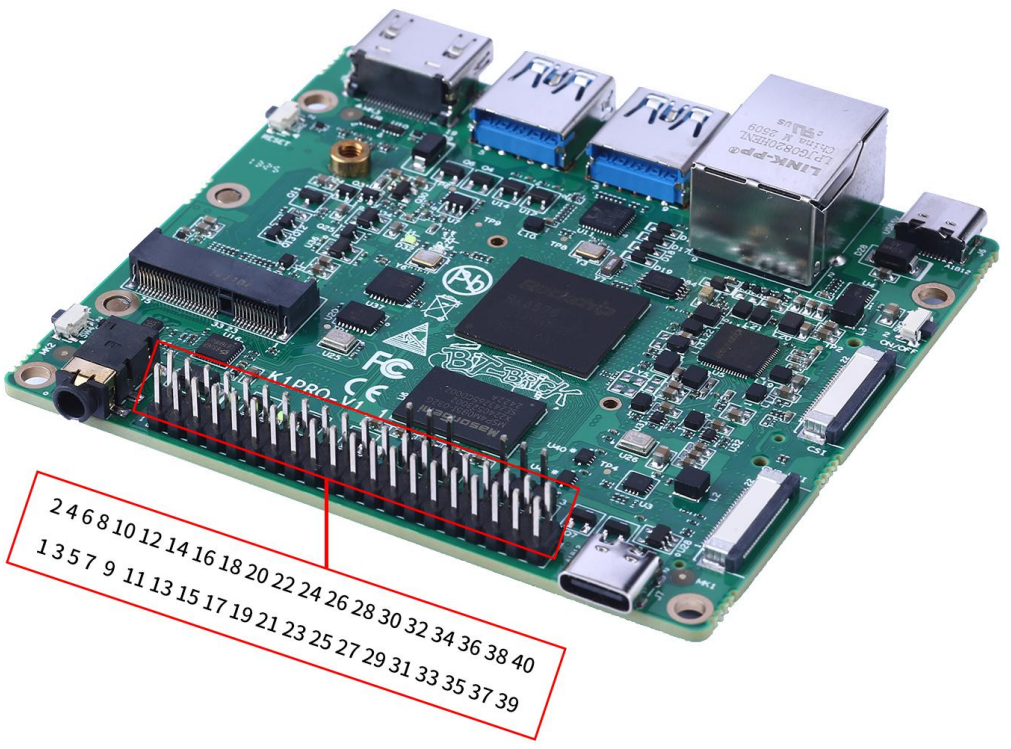
90.0mm X 80.0mm



5. GPIO Extension Interface

K1 Pro reserves a 40-pin GPIO extension interface, using a 2.54 double-row straight insertion socket, which is convenient for enthusiasts to connect peripherals according to their own needs and expand different functions. Our system will set these IOs to some specific functions by default, but users can reconfigure them through software to make these general-purpose IOs have some special functions, because these IOs are all multi-functional multiplexed pins.

Pin definations

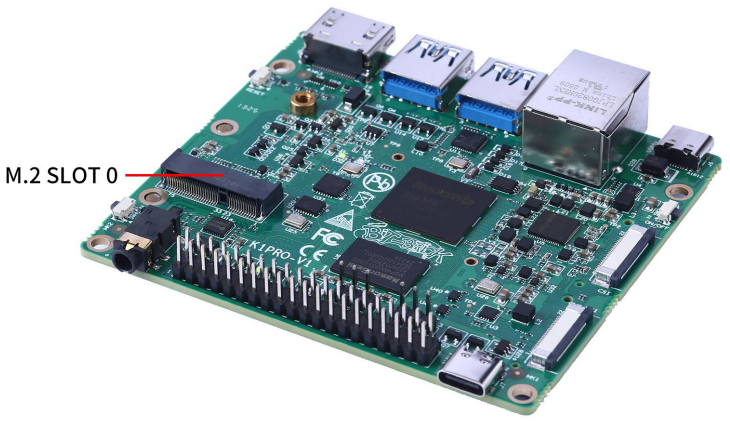


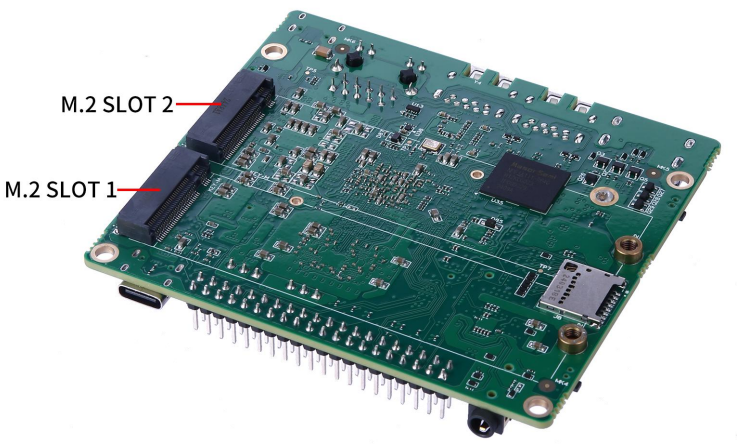
Pin Number	Pin Definition	Pin Number	Pin Definition
1	3.3V	2	5.0V
3	PWM2_CH1_M2/I2C6_SDA_M2/UART4_RX_M0/SAI4_SDO_M3/ETH1_RXD0_M0/ GPIO2_D1_d	4	5.0V
5	PWM2_CH0_M2/I2C6_SCL_M2/UART4_TX_M0/SAI4_SDI_M3/ETH1_TXCTL_M0/GPIO2_D0_d	6	GND
7	CAN0_TX_M2/I2C4_SCL_M1/UART6_TX_M0/SPI3_MOSI_M2/FLEXBUS0_D13_M1/PDM1_SDI3_M1/SAI4_SCLK_M0/GPIO4_A4_d	8	PWM2_CH2_M2/I3C1_SCL_M0/UART6_TX_M1/SAI4_MCLK_M3/ETH1_RXD1_M/CAM_CLK0_OUT_M1/GPIO2_D2_d
9	GND	10	PWM2_CH3_M2/I3C1_SDA_M0/UART6_RX_M1/ETH1_RXCTL_M0/GPIO2_D3_d
11	CAN0_RX_M2/I2C4_SDA_M1/UART6_RX_M0/SPI3_MISO_M2/FLEXBUS0_D14_M1/PDM1_CLK0_M1/SAI4_LRCK_M0/GPIO4_A6_	12	PWM2_CH4_M2/I2C9_SDA_M2/UART6_RTSN_M1/ETH1_MDC_M0/ISP_PRELIGHT_TRIG_M0/GPIO2_D4_d
13	PWM2_CH6_M0/SPI3_CLK_M2/SAI4_SDI_M0/SAI1_SDO0_M0/GPIO4_A7_d	14	GND
15	UART2_RTSN_M1/UART6_RTSN_M0/UART5_TX_M1/SPI4_CLK_M2/FLEXBUS1_D13_M1/PDM1_CLK1_M1/SAI1_SDI3_M0/SAI1_SDO1_M0/GPIO4_B0_d	16	PWM2_CH5_M2/I2C9_SCL_M2/UART6_CTSN_M1/ETH1_MDIO_M0/ISP_FLASH_TRIGOUT_M0/GPIO2_D5_d
17	3.3V	18	PWM2_CH6_M2/I3C1_SDA_PU_M0/UART9_RTSN_M0/SPDIF_RX0_M2/SAI3_MCLK_M2/ETH0_MCLK_M1/ETH_CLK1_25M_OUT_M0/CAM_CLK1_OUT_M1/GPIO2_D6_d
19	I2C7_SDA_M1/SPI3_MOSI_M0/UART3_RX_M0/SAI3_LRCK_M2/ETH0_MDC_M1/ETH1_PPSTRIG_M0/VI_CIF_VSYNC/GPIO3_A1_d	20	GND
21	MIPI_TE_M1/CAN1_TX_M3/SPI3_MISO_M0/UART3_CTSN_M0/SPDIF_RX1_M1/SAI3_SDO_M2/ETH0_RXCTL_M1/ETH1_PPSCLK_M0/VI_CIF_CLKO/GPIO3_A2_d	22	PWM1_CH0_M3/SPI2_CLK_M2/UART1_CTSN_M2/FLEXBUS0_CSN_M0/FLEXBUS1_D11/DSMC_RDYN/SAI4_SDI_M1/ETH_CLK0_25M_OUT_M0/VO_EBC_SDSHR/VO_LCDC_D23/GPIO3_A4_d
23	I2C7_SCL_M1/SPI3_CLK_M0/UART3_TX_M0/SAI3_SCLK_M2/ETH0_MDIO_M1/VI_CIF_HREF/GPIO3_A0_d	24	CAN1_RX_M3/SPI3_CSN0_M0/UART3_RTSN_M0/SPDIF_TX1_M1/SAI3_SDI_M2/ETH0_RXD1_M1/ETH1_PTP_REFCLK_M0/VI_CIF_CLKI/GPIO3_A3_d
25	GND	26	PWM0_CH0_M3/SPI2_MOSI_M2/UART10_RX_M0/FLEXBUS0_D8/DSMC_CSN1/SAI4_MCLK_M1/ETH0_MCLK_M0/VO_EBC_SDCE3/VO_LCDC_D19/GPIO3_B0_d
27	I2C7_SDA_M2/UART3_RX_M1/FLEXBUS0_CSN_M1/FLEXBUS1_D13_M0/FLEXBUS0_D14_M0/DSMC_INT2/SAI4_SDO_M1/CAM_CLK2_OUT_M0/SPDIF_TX0_M1/VO_POST_EMPTY/GPIO4_A1_d	28	MIPI_TE_M2/I2C7_SCL_M2/SPI1_CSN1_M2/UART3_TX_M1/FLEXBUS1_CSN_M3/FLEXBUS1_D14_M0/FLEXBUS0_D13_M0/DSMC_INT0/SAI4_LRCK_M1/CAM_CLK1_OUT_M0/SPDIF_RX0_M1/GPIO4_A0_d
29	MIPI_TE_M0/SPI4_MISO_M2/FLEXBUS1_D15_M1/PDM1_SDI1_M1/SAI1_SDI1_M0/SAI1_SDO3_M0/GPIO4_B2_d	30	GND
31	CAN1_RX_M2/I2C3_SDA_M0/UART2_RX_M1/FLEXBUS0_CSN_M4/SPDIF_RX0_M0/GPIO4_B4_d	32	PWM2_CH2_M3/SPI1_MISO_M2/UART8_RX_M0/FLEXBUS1_D6/DSMC_DATA4/SAI1_SDO0_M1/VO_EBC_SDDO6/VO_LCDC_D6/GPIO3_C5_d
33	CAN1_TX_M2/PCIE0_CLKREQN_M2/I2C3_SCL_M0/UART2_TX_M1/FLEXBUS0_D15_M1/SPDIF_TX0_M0/GPIO4_B5_d	34	GND
35	CAN0_TX_M3/I2C5_SCL_M3/SPI2_CSN0_M2/UART11_TX_M0/FLEXBUS1_D7/DSMC_DATA5/SAI1_SDO1_M1/VO_EBC_SDDO7/VO_LCDC_D7/GPIO3_C4_d	36	SPI1_MOSI_M2/UART8_TX_M0/FLEXBUS1_D5/DSMC_DATA3/SAI1_LRCK_M1/VO_EBC_SDDO5/VO_LCDC_D5/GPIO3_C6_d
37	PWM2_CH2_M3/SPI1_MISO_M2/UART8_RX_M0/FLEXBUS1_D6/DSMC_DATA4/SAI1_SDO0_M1/VO_EBC_SDDO6/VO_LCDC_D6/GPIO3_C5_d	38	PWM2_CH3_M3/SPI1_CSN0_M2/UART8_CTSN_M0/FLEXBUS1_D3/DSMC_DATA1/SAI1_MCLK_M1/VO_EBC_SDDO3/VO_LCDC_D3/GPIO3_D0_d
39	GND	40	PWM2_CH3_M1/CAN1_RX_M1/SPI4_CLK_M0/I2C6_SDA_M3/VP2_SYNC_OUT/SAI4_SCLK_M2/GPIO4_C7_d

6. M.2 Interface Description

M.2 Interface

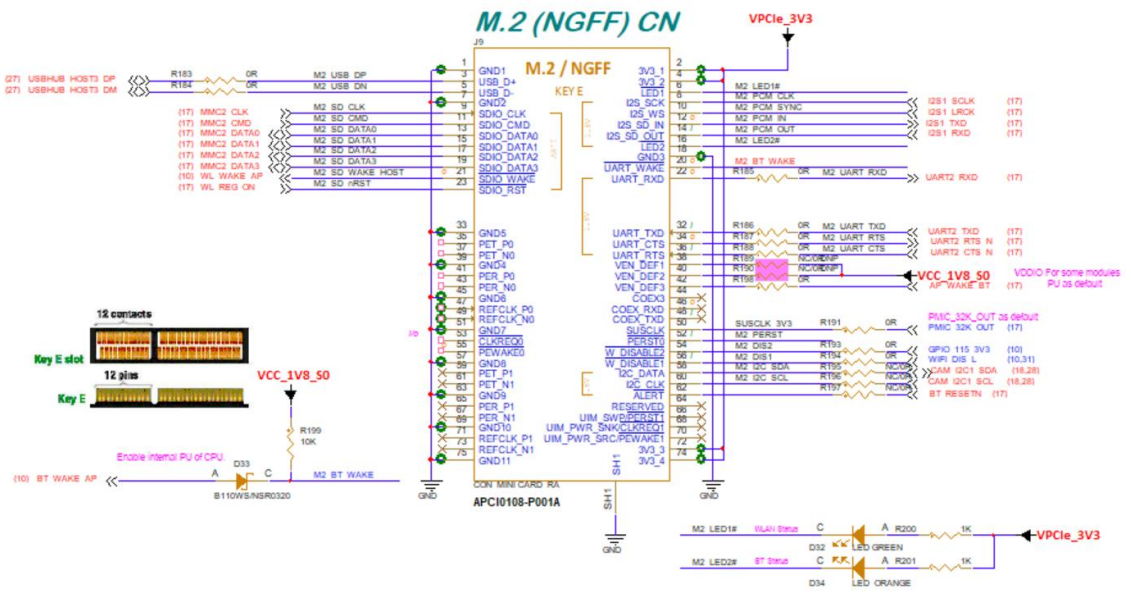
The K1 Pro board integrates three M.2 interfaces, as shown in the following figure:





Among them, M.2 SLOT 1 and 2 are standard M.2 KEY-M interface definitions, which can directly support solid-state drives with the NVME interface. The length of the solid-state drive can be 2280. Users can choose SSDs with the mainstream NVME interface.

The other M.2 SLOT 0 is the interface definition of KEY-E, with a length of 2230, which is mainly used to support various wireless modules. Since the processor only has three USB interfaces, the USB interface is not reserved for SLOT 0, and the PCIE interface compatible with NGFF is also removed, so modules with USB and PCIE interface definitions are not supported. The detailed description of the pin definition of the SLOT 0 interface is as follows:



7. Camera Interface Description

MIPI CSI2 Controlle

The RK3576 application processor of K1 Pro supports 5 CSI-2 interfaces:

- 4 ports support 2 D-PHY v1.2 data-lane with 2.5Gbps/lane
  These 4 ports may be bound as 2 ports with 4 data-lane per port
- 1 port supports 4 D-PHY data-lane or 3 C-PHY trios
  D-PHY is v2.0 which lane speed is 4.5Gbps
  C-PHY is v1.1 which trio speed is 2.5Gsps
- Each port supports 4 virtual channels

ISP Processor

The K1 Pro processor introduces a new generation 16-Megapixel ISP. It implements a lot of algorithm accelerators, such as HDR, 3A, CAC, 3DNR, 2DNR,Sharpening, Dehaze, Enhance, Debayer, Small Angle Lens-Distortion Correction and so on.
ISP V3.9

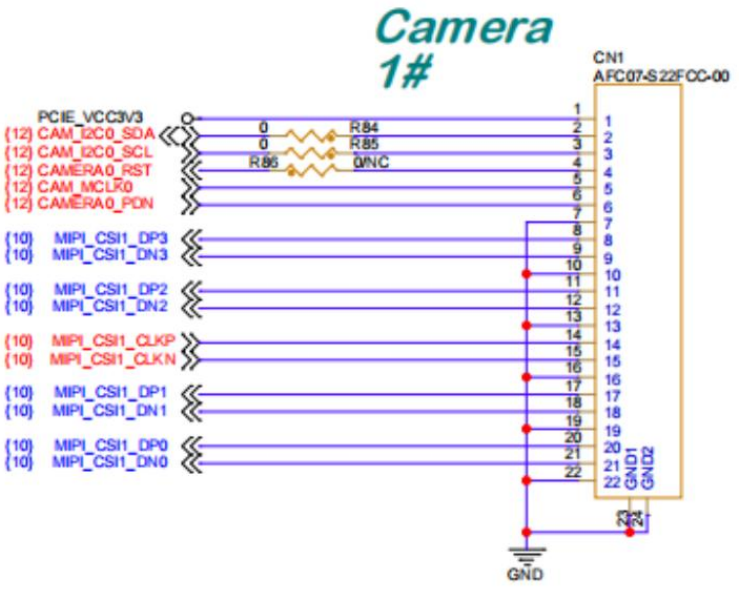
- Support video mode and picture mode
- One channel ISP, 16M pixels
- VICAP/DMA input: raw8/raw10/raw12/raw16
- RGB-IR sensor input
- 3A: include AE/Histogram, AF, AWB statistics output

- BLC: Black Level Correction
- PDAF: Phase Detection Auto Focus
- DPCC: Static/Dynamic defect pixel cluster correction
- LSC: Lens shading correction
- HDR: 2-Frame Merge into High-Dynamic Range
- DRC/TMO: Dynamic Range Compression, Tone mapping in RGB field
  - Supports up to 120dB HDR with 20-bit data width
- EXPANDER: Sensor expander
- GIC: Green Imbalance Correction
- Debayer: Advanced Adaptive Demosaic with Chromatic Aberration Correction(CAC)
- CCM/CSM: Color correction matrix; RGB2YUV etc
- Gamma: Gamma out correction
- Dehaze/Enhance: Automatic Dehaze and edge enhancement
- Bay3DNR: Advanced Temporal Noise reduce in RAW
- YUVME: Noise Motion Estimate and Motion Compensation in YUV
- 2DNR: Advanced Spatial Noise reduce in YUV
- Sharp: Picture Sharpening & Edge Enhance in YUV
- CGC: Color Gamut Compression, YUV full range/limit range convert
- 3DLUT: 3D-Lut Color Palette for Customer
- LDCH: Lens-distortion in the horizontal direction
- LDCV: Lens-distortion in the vertical direction
- Gain: Image local gain
- Output Scale*2: support scale down level

BIT - BRICK K1 Pro Camera

The BIT - BRICK K1 Pro board reserves a 4 - lane MIPI CSI2S camera interface

Its pin definition is as follows:



Users can design the camera according to their actual needs. The supported camera sensors are as follows:

序号	型号	像素	接口	位宽（bits）	帧率（fps）	已支持最大分辨率	厂家
1	GC2375	2M	MIPI CSI 1lane	10	30	1600x1200	格科微
2	S5K5E3YX	5M	MIPI CSI 2lane	10	30	2560x1920	三星
3	IMX135	13M	MIPI CSI 4lane	10	30	4208x3120	索尼
4	SC031GS	0.3M	MIPI CSI 1lane	10	30	640x480	思特威
5	GC5035	5M	MIPI CSI 2lane	10	30	2592x1944	格科微
6	OS05A10	2M	MIPI CSI 1lane	10	30	1920x1080	豪威
7	OV08D10	8M	MIPI CSI 2lane	10	30	3264x2448	豪威
8	OV13B10	13M	MIPI CSI 4lane	10	30	4208x3120	豪威
9	OV16A10	16M	MIPI CSI 4lane	10	30	3840x2160	豪威
10	OV8856	8M	MIPI CSI 4lane	10	30	2560x1440	豪威

It is recommended to choose the sensors in the above list to reduce the workload of software debugging.

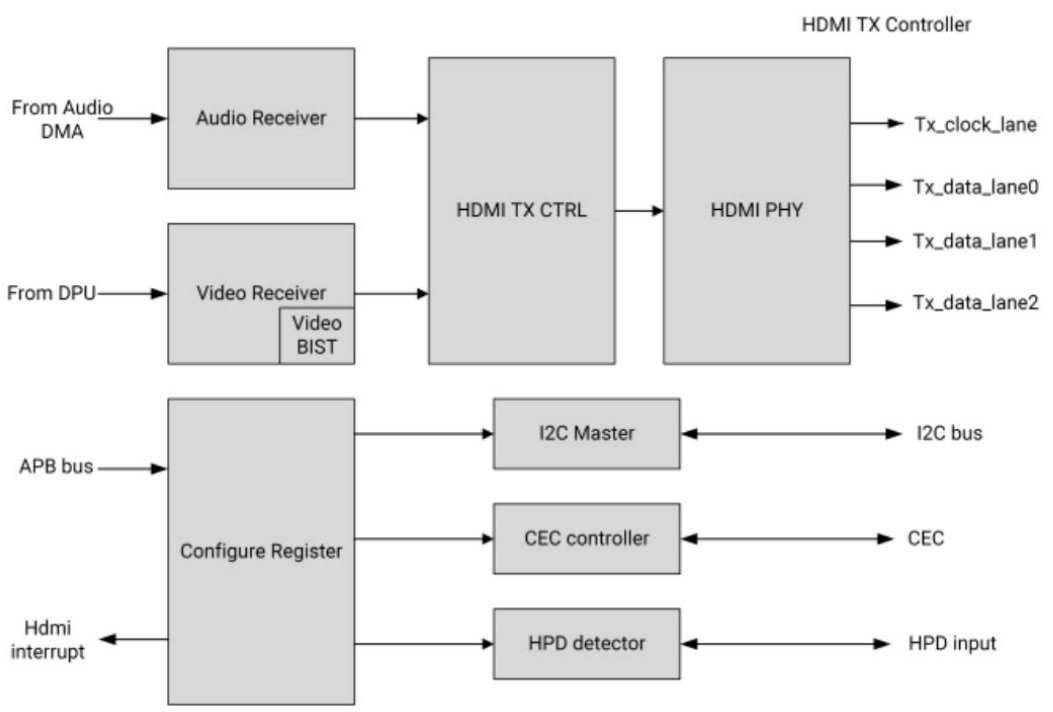
8. Display Interface Description

The K1 Pro motherboard supports HDMI and MIPI DSI2 interface-defined LCD displays as the graphical output interface.

HDMI

K1 Pro supports the HDMI2.1 version, and the maximum resolution supports 4K@120fps. The main features are as follows:

- Compliant with HDMI Specification v1.4
- HDMI v2.1
- Supports up to 4K@120Hz
- Output data format: RGB/YUV444/YUV422/YUV420 8/10-bit
- Supports CEC (Consumer Electronic Control) and ARC (Audio Return Channel)
- HDCP v2.3 and HDCP v1.4

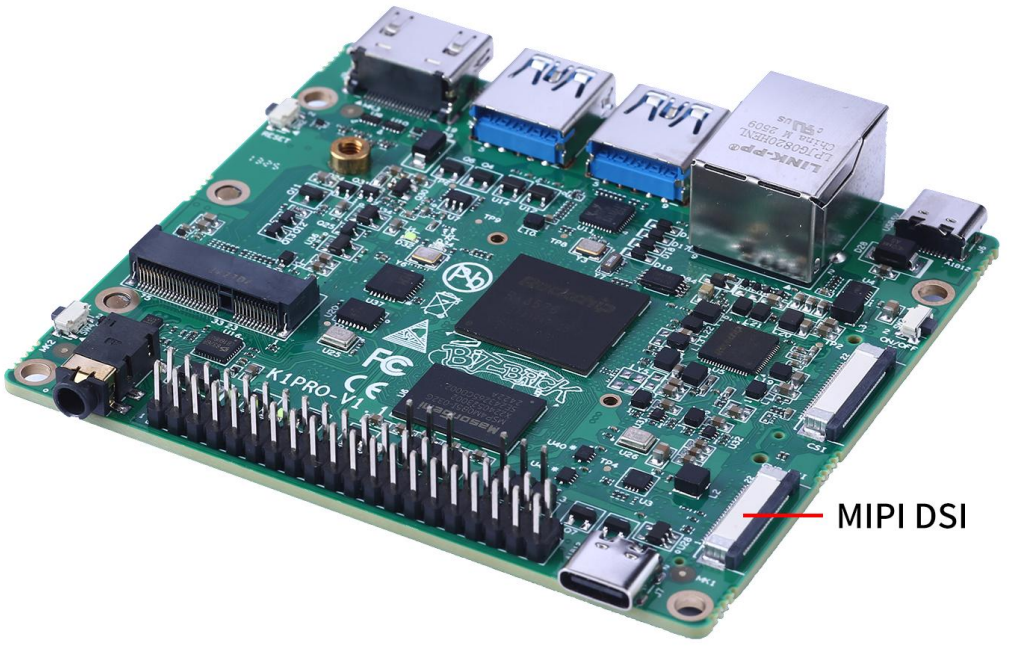


HDMI Transmission Block Diagram

You can directly connect K1 Pro and the display using a standard HDMI cable (if the display interface is not HDMI, you can purchase an HDMI converter, such as HDMI to DP, etc.)

MIPI DSI-2 TX interface

One MIPI DSI-2 v1.1 interface with D-PHY v2.0 or C-PHY v1.1
Supports 4 data lanes on D-PHY
Supports 3 data trios on C-PHY
Supports up to 2560x1600@60Hz
Supports RGB (up to 10bit) data format

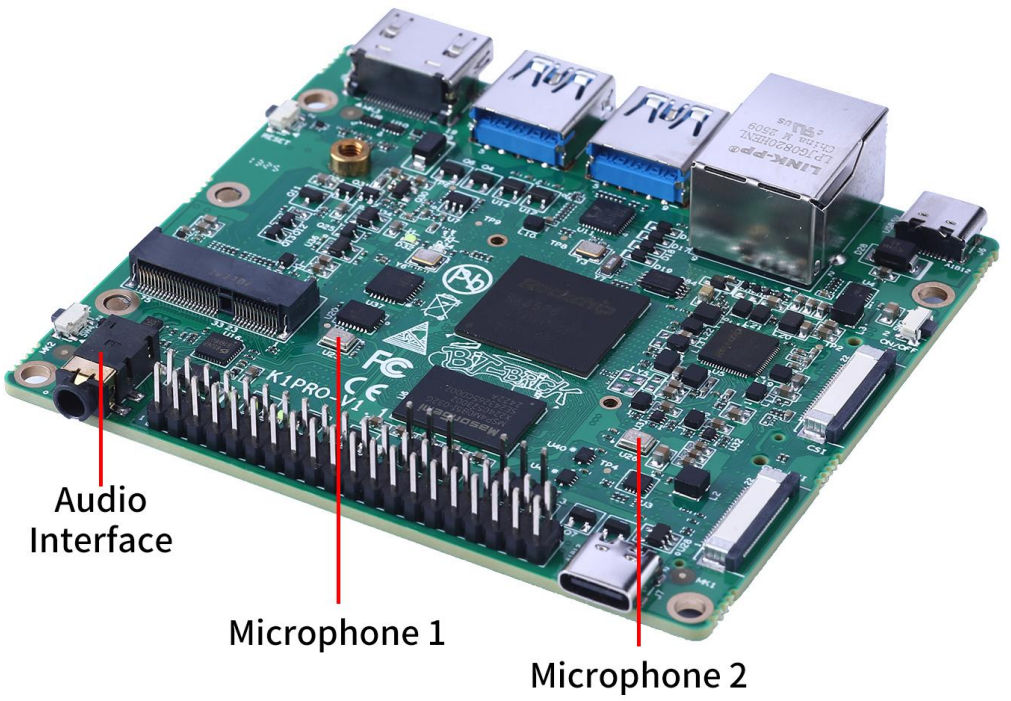


9. Audio Interface Description

Hardware Components

The audio part of K1 Pro is mainly composed of three aspects:

- HDMI audio output
- 3.5mm standard audio socket
- Left and right channel microphone input

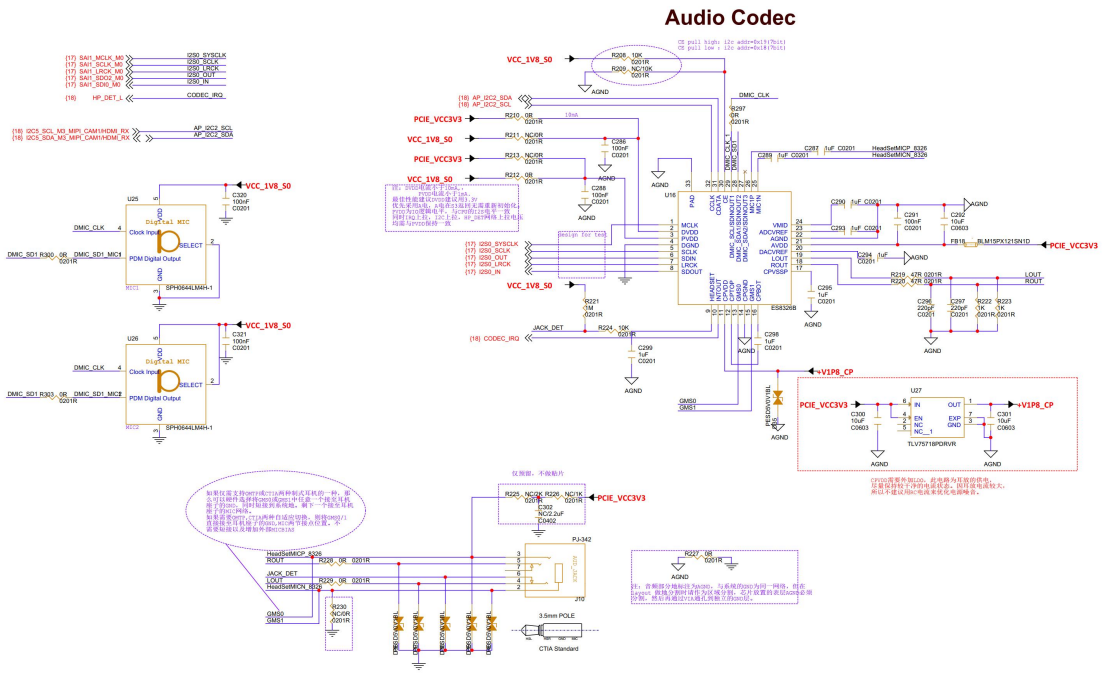


Schematic Diagram of the Audio Interface

Circuit

Although the processor internally integrates an audio Codec, K1 Pro still adopts the approach of an external Codec in the design. It connects to the ES8326B through the I2S interface to achieve audio input and output.

The ES8326B chip is an audio decoding chip, mainly used to convert digital audio signals into analog audio signals. It uses a high-performance digital signal processor and a low-power power amplifier to achieve a high-definition music experience and high-quality call requirements. For detailed specifications, refer to the ES8326B section in the data booklet.



Circuit of the Audio Part

10. Ordering Information

Part No.	CPU	Memory	Flash	Operating Temperature
Bit-Brick-K1 Pro-4320	RK3576	4GB	32GB	-40~85°C
Bit-Brick-K1 Pro-2160	RK3576	8GB	64GB	-40~85°C

11. Update History

Version Revision	Update Date	Content
Provisional V 1.0	2025-3-5	Initial the first version