Bit-Brick SSOM-IMX8MP
data sheet

Provisional version

V 1.0

Bit Brick Technology Corporation

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1 Summary

SSOM-IMX8MP-POC is an ultra-compact SoM equipped with NXP's i.MX8M Plus application processor. (System on Module).

The SoM contains LPDDR4 SDRAM, eMMC, NOR Flash, power monitoring IC (PMIC), and four board-toboard connectors as peripheral devices connected to the i.MX8M Plus.

Since most of the SoC (i.MX8M Plus) signals can be connected through the board-to-board connector, most of the SoC's functions are available.

Designed for compatibility with the development kit (i.MX 8M PLUS EVK) from NXP, the same functionality as the development kit can be achieved. This makes it easy to maintain compatibility with software provided by NXP.

1.1 Device

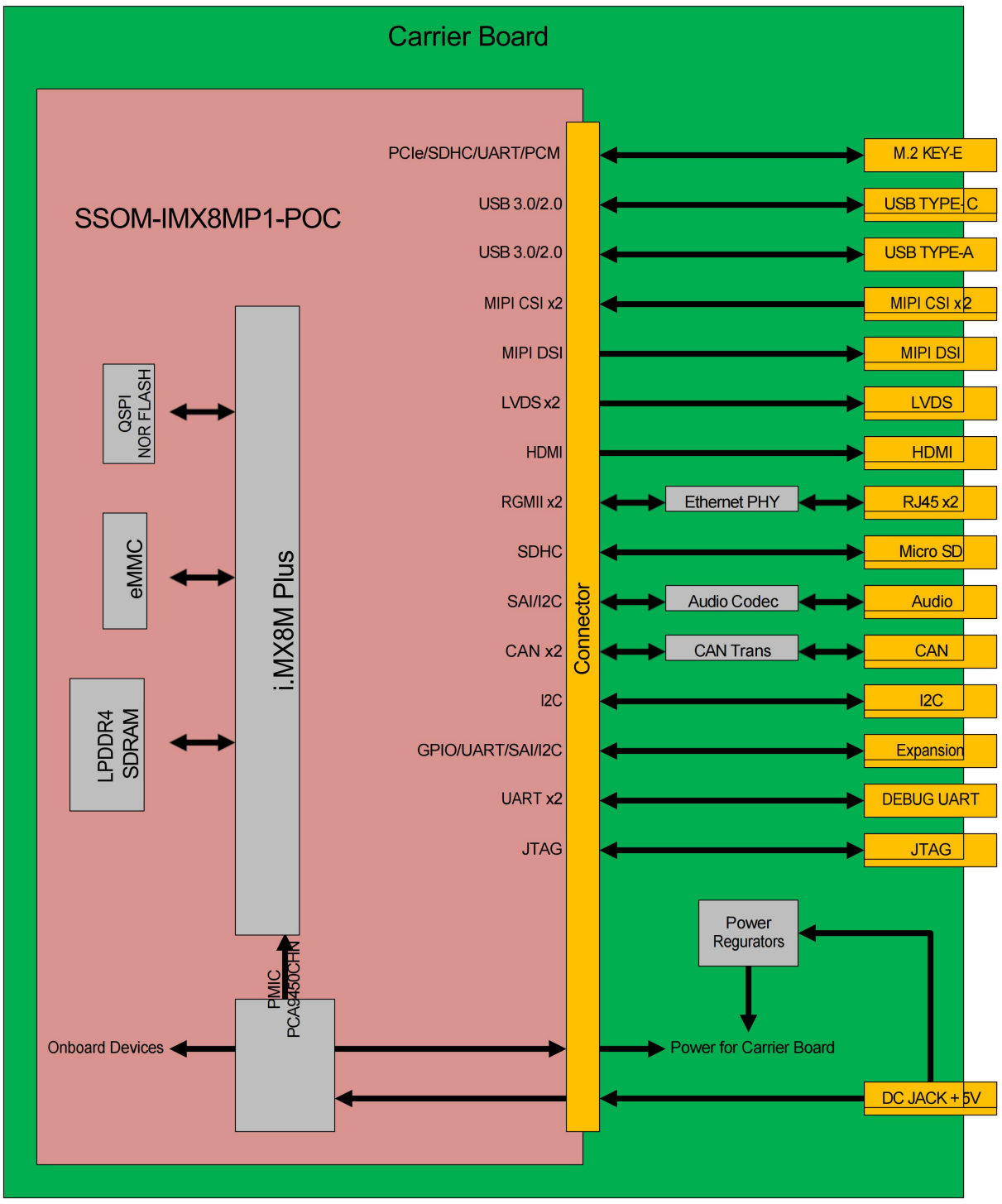
- ●SoC: i.MX8M Plus from NXP
  - Cortex A53 4 cores Maximum operating frequency 1.8 GHz
  - Cortex M7 1 core Maximum operating frequency 800MHz
  - NPU (Neural Processing Unit) Max. 2.3TOPS
- ● LPDDR4 SDRAM Up to 6GB
- ●eMMC up to 64GB
- ● QSPI NOR FLASH 32MB
- ● Power monitoring IC: PCA9450CHN from NXP
- ● Board-to-board connectors (4)
  - 100-pin connector (2 pcs)
  - 80-pin connector (2 pcs)

1.2 Feature

The following functions can be configured with the onboard SoC (i.MX8M Plus). (Not all functions are available at the same time.)

- ● PCI Express - 1 lane 1 channel
- ● USB 3.0 - Built-in PHY 2 channels
- ● USB 2.0 - Built-in PHY 2 channels
- ● HDMI interface
- ● LVDS display interface
  - 4 lanes 2 channels
- ● MIPI DSI Interface
  - 4 lanes 1 channel
- ● MIPI CSI interface
  - 4 lanes 2 channels
- ● Ethernet interface
  - RGMII interface 2 channels
- ● audio interface
  - Digital audio (SAI) Up to 5 channels
  - SPDIF interface 1 channel
- ● SD Card Interface
  - SDIO 2 channels
- ● Other
  - UART 4-channel
  - SPI 2 channel
  - I2C 3-channel
  - CAN 2 channel
  - GPIO

1.2.1 System Configuration Example



2 Signal Connection

All signals available on this SoM are compatible with those of the SoM in the NXP development kit (i.MX 8M PLUS EVK). The signal connections are equivalent to those of the SoM in the NXP development kit (i.MX 8M PLUS EVK), except for the signal pin assignments, which have been changed due to a connector change. Please refer to the schematic of the development kit (i.MX 8M PLUS EVK) from NXP for details.

2.1 Board-to-board connector and connection of each device

The board-to-board connector is connected to the i.MX8M Plus signal and the PMIC (PCA9450CHN) signal and power input/output.

The following shows the connection relationship between board-to-board connectors (J1 to J4) and each device on the SoM.

2.1.1 Connection relationship between J1 and each device

Table 2-1 shows the connection relationship between the board-to-board connector (J1) and each device on the SoM.

Table 2-1 Connection relationship between J1 and each device

Connector Pin Number	Connecior Pin Name	Connected Device	Device Pin Number	Device Pad Name
1(J1)	SAI1_TXC	i.MX8M Plus	AJ12	SAI1_TXC
3(J1)	SAI1_TXD0	i.MX8M Plus	AJ11	SAI1_TXD0
5(J1)	SAI1_TXD1	i.MX8M Plus	AJ10	SAI1_TXD1
7(J1)	SAI1_TXD2	i.MX8M Plus	AH11	SAI1_TXD2
9(J1)	SAI1_TXD3	i.MX8M Plus	AD12	SAI1_TXD3
11(J1)	GND			
13(J1)	SAI1_TXD4	i.MX8M Plus	AH13	SAI1_TXD4
15(J1)	SAI1_TXD5	i.MX8M Plus	AH14	SAI1_TXD5
17(J1)	SAI1_TXD6	i.MX8M Plus	AC12	SAI1_TXD6
19(J1)	SAI1_TXD7	i.MX8M Plus	AJ13	SAI1_TXD7
21(J1)	SAI1_TXFS	i.MX8M Plus	AF12	SAI1_TXFS
23(J1)	SAI1_MCLK	i.MX8M Plus	AE12	SAI1_MCLK
25(J1)	GND			
27(J1)	SAI1_RXFS	i.MX8M Plus	AJ9	SA1_RXFS
29(J1)	SAI1_RXC	i.MX8M Plus	AH8	SAI1_RXC
31(J1)	SAI1_RXD0	i.MX8M Plus	AC10	SAI1_RXD0
33(J1)	SAI1_RXD1	i.MX8M Plus	AF10	SAI1_RXD1
35(J1)	SAI1_RXD2	i.MX8M Plus	AH9	SAI1_RXD2
37(J1)	SAI1_RXD3	i.MX8M Plus	AJ8	SAI1_RXD3
39(J1)	GND			
41(J1)	SAI1_RXD4	i.MX8M Plus	AD10	SAI1_RXD4
43(J1)	SAI1_RXD5	i.MX8M Plus	AE10	SAI1_RXD5
45(J1)	SAI1_RXD6	i.MX8M Plus	AH10	SAI1_RXD6
47(J1)	SAI1_RXD7	i.MX8M Plus	AH12	SAI1_RXD7
49(J1)	GND			
51(J1)	SAI3_TXC	i.MX8M Plus	AH19	SAI3_TXC
53(J1)	SAI3_TXFS	i.MX8M Plus	AC16	SAI3_TXFS
55(J1)	SAI3_TXD	i.MX8M Plus	AH18	SAI3_TXD
57(J1)	SAI3_RXC	i.MX8M Plus	AJ18	SAI3_RXC
59(J1)	SAI3_RXFS	i.MX8M Plus	AJ19	SAI3_RXFS
61(J1)	SAI3_RXD	i.MX8M Plus	AF18	SAI3_RXD
63(J1)	SAI3_MCLK	i.MX8M Plus	AJ20	SAI3_MCLK
65(J1)	GND			
67(J1)	ECSPI2_MISO	i.MX8M Plus	AH20	ECSPI2_MISO
69(J1)	ECSPI2_MOSI	i.MX8M Plus	AJ21	ECSPI2_MOSI
71(J1)	ECSPI2_SCLK	i.MX8M Plus	AH21	ECSPI2_SCLK
73(J1)	ECSPI2_SS0	i.MX8MPlus	AJ22	ECSPI2_SS0
75(J1)	GND			
77(J1)	HDMI_TXCN	i.MX8M Plus	AJ24	HDMI_TXC_N
79(J1)	HDMI_TXCP	i.MX8M Plus	AH24	HDMI_TXC_P
81(J1)	GND			
83(J1)	HDMI_TXN0	i.MX8M Plus	AJ25	HDMI_TX0_N
85(J1)	HDMI_TXP0	i.MX8M Plus	AH25	HDMI_TX0_P
87(J1)	GND			
89(J1)	HDMI_TXN1	i.MX8M Plus	AJ26	HDMI_TX1_N

91(J1)	HDMI_TXP1	i.MX8M Plus	AH26	HDMI_TX1_P
93(J1)	GND			
95(J1)	HDM_TXN2	i.MX8M Plus	AJ27	HDMI_TX2_N
97(J1)	HDM_TXP2	i.MX8M Plus	AH27	HDMI_TX2_P
99(J1)	GND			
2(J1)	GND			
4(J1)	UART1_TXD	i.MX8M Plus	AJ3	UART1_TXD
6(J1)	UART1_RXD	i.MX8M Plus	AD6	UART1_RXD
8(J1)	UART1_CTS	i.MX8M Plus	AE6	UART3_RXD
10(J1)	UART1_RTS	i.MX8M Plus	AJ4	UART3_TXD
12(J1)	UART2_TXD	i.MX8M Plus	AH4	UART2_TXD
14(J1)	UART2_RXD	i.MX8M Plus	AF6	UART2_RXD
16(J1)	GND			
18(J1)	UART3_CTS	i.MX8M Plus	AD20	ECSPI1_MISO
20(J1)	UART3_RTS	i.MX8M Plus	AE20	ECSPI1_SS0
22(J1)	UART3_TXD	i.MX8M Plus	AC20	ECSPI1_MOSI
24(J1)	UART3_RXD	i.MX8M Plus	AF20	ECSPI1_SCLK
26(J1)	UART4_TXD	i.MX8M Plus	AH5	UART4_TXD
28(J1)	UART4_RXD	i.MX8M Plus	AJ5	UART4_RXD
30(J1)	GND			
32(J1)	I2C2_SCL*1	i.MX8M Plus	AH6	12C2_SCL
34(J1)	I2C2_SDA*1	i.MX8M Plus	AE8	I2C2_SDA
36(J1)	I2C3_SCL*1	i.MX8M Plus	AJ7	I2C3_SCL
38(J1)	I2C3_SDA*1	i.MX8M Plus	AJ6	I2C3_SDA
40(J1)	I2C4_SCL*1	i.MX8M Plus	AF8	12C4_SCL
42(J1)	12C4_SDA*1	i.MX8M Plus	AD8	12C4_SDA
44(J1)	GND			
46(J1)	SAI2_RXD	i.MX8M Plus	AJ14	SAI2_RXD0
48(J1)	SAI2_RXFS	i.MX8M Plus	AH17	SAI2_RXFS
50(J1)	SAI2_RXC	i.MX8M Plus	AJ16	SAI2_RXC
52(J1)	SAI2_MCLK	i.MX8M Plus	AJ15	SAI2_MCLK
54(J1)	GND			
56(J1)	SAI2_TXC	i.MX8M Plus	AH15	SAI2_TXC
58(J1)	SAI2_TXFS	i.MX8M Plus	AJ17	SAI2_TXFS
60(J1)	SAI2_TXD	i.MX8M Plus	AH16	SAI2_TXD0
62(J1)	GND			
64(J1)	SAI5_RXD0	i.MX8M Plus	AE16	SAI5_RXD0
66(J1)	SAI5_RXD1	i.MX8M Plus	AD16	SAI5_RXD1
68(J1)	SAI5_RXD2	i.MX8M Plus	AF16	SAI5_RXD2
70(J1)	SAI5_RXD3	i.MX8M Plus	AE14	SAI5_RXD3
72(J1)	SAI5_MCLK	i.MX8M Plus	AF14	SAI5_MCLK
74(J1)	SAI5_RXFS	i.MX8M Plus	AC-14	SAI5_RXFS
76(J1)	SAI5_RXC	i.MX8M Plus	AD14	SAI5_RXC
78(J1)	GND			
80(J1)	SPDIF_TX	i.MX8M Plus	AE18	SPDIF_TX
82(J1)	SPDIF_RX	i.MX8M Plus	AD18	SPDIF_RX
84(J1)	SPDIF_EXT_CLK	i.MX8M Plus	AC18	SPDIF_EXT_CLK
86(J1)	GND			
88(J1)	HDMI_HPD	i.MX8M Plus	AE22	HDMI_HPD
90(J1)	EARC_N_HPD	i.MX8M Plus	AH22	EARC_N_HPD
92(J1)	HDMI_DDC_SDA	i.MX8M Plus	AF22	HDMI_DDC_SDA
94(J1)	HDMI_DDC_SCL	i.MX8M Plus	AC22	HDMI_DDC_SCL
96(J1)	EARC_P_UTIL	i.MX8M Plus	AJ23	EARC_P_UTL
98(J1)	HDMI_CEC	i.MX8M Plus	AD22	HDMI_CEC
100(J1)	GND			

*1 **Pulled up to the power supply (VDD_1V8) on the SoM through a resistor 4.7KΩ.**

2.1.2 Connection relationship between J2 and each device

Table 2-2 shows the connection relationship between the board-to-board connector (J2) and each device on the SoM.

Table 2-2 Connection relationship between J2 and each device

Connector Pin Number	Connecior Pin Name	Connected Device	Device Pin Number	Device Pad Name

1(J2)	GND			
3(J2)	WDOG_B*2	i.MX8M Plus	B6	GPIO1_IO02
		PCA9450CHN	28	WDOG_B
5(J2)	GND			
7(J2)	GPIO1_IO11	i.MX8M Plus	D8	GPIO1_IO11
9(J2)	GPIO1_IO10	i.MX8M Plus	B7	GPIO1_IO10
11(J2)	GPIO1_IO09	i.MX8M Plus	B8	GPIO1_IO09
13(J2)	GPIO1_IO08	i.MX8M Plus	A8	GPIO1_IO08
15(J2)	GND			
17(J2)	GPIO1_IO07	i.MX8M Plus	F6	GPIO1_IO07
19(J2)	GPIO1_IO06	i.MX8M Plus	A3	GPIO1_IO06
21(J2)	GPIO1_IO05	i.MX8M Plus	B4	GPIO1_IO05
23(J2)	GPIO1_IO01	i.MX8M Plus	E8	GPIO1_IO01
25(J2)	GPIO1_IO00	i.MX8M Plus	A7	GPIO1_IO00
27(J2)	GND			
29(J2)	USB1_RXP	i.MX8M Plus	A9	USB1_RX_P
31(J2)	USB1_RXN	i.MX8M Plus	B9	USB1_RX_N
33(J2)	GND			
35(J2)	USB1_TXP	i.MX8M Plus	A10	USB1_TX_P
37(J2)	USB1_TXN	i.MX8M Plus	B10	USB1_TX_N
39(J2)	GND			
41(J2)	USB1_DN	i.MX8M Plus	E10	USB1_D_N
43(J2)	USB1_DP	i.MX8M Plus	D10	USB1_D_P
45(J2)	GND			
47(J2)	PCIE_RXN	i.MX8M Plus	B14	PCIE_RXN_N
49(J2)	PCIE_RXP	i.MX8M Plus	A14	PCIE_RXN_P
51(J2)	GND			
53(J2)	PCIE_TXN	i.MX8M Plus	B15	PCIE_TXN_N
55(J2)	PCIE_TXP	i.MX8M Plus	A15	PCIE_TXN_P
57(J2)	GND			
59(J2)	PCIE_CLKN	i.MX8M Plus	E16	PCIE_REF_PAD_CLK_N
61(J2)	PCIE_CLKP	i.MX8M Plus	D16	PCIE_REF_PAD_CLK_P
63(J2)	GND			
65(J2)	USB2_DP	i.MX8M Plus	D14	USB2_D_P
67(J2)	USB2_DN	i.MX8M Plus	E14	USB2_D_N
69(J2)	GND			
71(J2)	CSI1_DPO	i.MX8M Plus	D18	MIPI_CSI1_D0_P
73(J2)	CSI_DNO	i.MX8M Plus	E18	MIPI_CSI1_D0_N
75(J2)	GND			
77(J2)	CSI1_DP1	i.MX8M Plus	D20	MIPI_CSI1_D1_P
79(J2)	CSI1_DN1	i.MX8M Plus	E20	MIPI_CSI1_D1_N
81(J2)	GND			
83(J2)	CSI1_CKP	i.MX8M Plus	D22	MIPI_CSI1_CLK_P
85(J2)	CSI1_CKN	i.MX8M Plus	E22	MIPI_CSI1_CLK_N
87(J2)	GND			
89(J2)	CSI1_DP2	i.MX8M Plus	D24	MIPI_CSI1_D2_P
91(J2)	CSI1_DN2	i.MX8M Plus	E24	MIPI_CSI1_D2_N
93(J2)	GND			
95(J2)	CSI1_DP3	i.MX8M Plus	D26	MIPI_CSI1_D3_P
97(J2)	CSI1_DN3	i.MX8M Plus	E26	MIPI_CSI1_D3_N
99(J2)	GND			
2(J2)	GND			
4(J2)	GPIO1_IO15	i.MX8M Plus	B5	GPIO1_IO15
6(J2)	GPIO1_IO14	i.MX8M Plus	A4	GPIO1_IO14
8(J2)	GPIO1_IO13	i.MX8M Plus	A6	GPIO1_IO13
10(J2)	GPIO1_IO12	i.MX8M Plus	A5	GPIO1_IO12
12(J2)	GND			
14(J2)	BOOT_MODE0	i.MX8M Plus	Group of Ten	BOOT_MODE0
16(J2)	BOOT_MODE1	i.MX8M Plus	F8	BOOT_MODE1
18(J2)	BOOT_MODE2	i.MX8M Plus	G8	BOOT_MODE2
20(J2)	BOOT_MODE3	i.MX8M Plus	G12	BOOT_MODE3
22(J2)	GND			
24(J2)	USB2_VBUS_3V3	i.MX8M Plus	D12	USB2_VBUS

26(J2)	USB1_VBUS_3V3	i.MX8M Plus	A11	USB1_VBUS
28(J2)	GND			
30(J2)	USB2_RXN	i.MX8M Plus	B12	USB2_RX_N
32(J2)	USB2_RXP	i.MX8M Plus	A12	USB2_RX_P
34(J2)	GND			
36(J2)	USB2_TXN	i.MX8M Plus	B13	USB2_TX_N
38(J2)	USB2_TXP	i.MX8M Plus	A13	USB2_TX_P
40(J2)	GND			
42(J2)	DSI_DP0	i.MX8M Plus	A16	MIPI_DSI1_D0_P
44(J2)	DSI_DN0	i.MX8M Plus	B16	MIPI_DSI1_D0_N
46(J2)	GND			
48(J2)	DSI_DP1	i.MX8M Plus	A17	MIPI_DSI1_D1_P
50(J2)	DSI_DN1	i.MX8M Plus	B17	MIPI_DSI1_D1_N
52(J2)	GND			
54(J2)	DSI_CKP	i.MX8M Plus	A18	MIPI_DSI1_CLK_P
56(J2)	DSI_CKN	i.MX8M Plus	B18	MIPI_DSI1_CLK_N
58(J2)	GND			
60(J2)	DSI_DP2	i.MX8M Plus	A19	MIPI_DSI1_D2_P
62(J2)	DSI_DN2	i.MX8M Plus	B19	MIPI_DSI1_D2_N
64(J2)	GND			
66(J2)	DSI_DP3	i.MX8M Plus	A20	MIPI_DSI1_D3_P
68(J2)	DSI_DN3	i.MX8M Plus	B20	MIPI_DS1_D3_N
70(J2)	GND			
72(J2)	CSI2_DP3	i.MX8M Plus	A21	MIPI_CSI2_D3_P
74(J2)	CSI2_DN3	i.MX8M Plus	B21	MIPI_CSI2_D3_N
76(J2)	GND			
78(J2)	CSI2_DP2	i.MX8M Plus	A22	MIPI_CSI2_D2_P
80(J2)	CSI2_DN2	i.MX8M Plus	B22	MIPI_CSI2_D2_N
82(J2)	GND			
84(J2)	CSI2_CKP	i.MX8M Plus	A23	MIPI_CSI2_CLK_P
86(J2)	CSI2_CKN	i.MX8M Plus	B23	MIPI_CSI2_CLK_N
88(J2)	GND			
90(J2)	CSI2_DP1	i.MX8M Plus	A24	MIPI_CSI2_D1_P
92(J2)	CSI2_DN1	i.MX8M Plus	B24	MIPI_CSI2_D1_N
94(J2)	GND			
96(J2)	CSI2_DPO	i.MX8M Plus	A25	MIPI_CSI2_D0_P
98(J2)	CSI2_DNO	i.MX8M Plus	B25	MIPI_CSI2_D0_N
100(J2)	GND			

[*2] Pulled up to the power supply (VDD_1V8) on the SoM via a 100KΩ resistor.

2.1.3 Connection relationship between J3 and each device

Table 2-3 shows the connection relationship between the board-to-board connector (J3) and each device on the SoM.

Table 2-3 Connection relationship between J3 and each device

Connector Pin Number	Connecior Pin Name	Connected Device	Device Pin Number	Device Pad Name
1(J3)	ENET_RD0	i.MX8M Plus	AG29	ENET_RD0
3(J3)	ENET_RD1	i.MX8M Plus	AG28	ENET RD1
5(J3)	ENET_RD2	i.MX8M Plus	AF29	ENET RD2
7(J3)	ENET_RD3	i.MX8M Plus	AF28	ENET_RD3
9(J3)	ENET_RXC	i.MX8M Plus	AE29	ENET_RXC
11(J3)	ENET_RX_CTL	i.MX8M Plus	AE28	ENET_RX_CTL
13(J3)	GND			
15(J3)	SD2_RESET_B*3	i.MX8M Plus	AD28	SD2_RESET_B
		PCA9450CHN	12	SW_EN
17(J3)	SD2_nCD	i.MX8M Plus	AD29	SD2_CD_B
19(J3)	SD2_WP	i.MX8M Plus	AC26	SD2_WP
21(J3)	SD2_CMD	i.MX8M Plus	AB28	SD2_CMD
23(J3)	SD2_CLK	i.MX8M Plus	AB29	SD2 CLK
25(J3)	SD2_DATA0	i.MX8M Plus	AC28	SD2_DATA0
27(J3)	SD2_DATA1	i.MX8M Plus	AC29	SD2_DATA1
29(J3)	SD2_DATA2	i.MX8M Plus	AA26	SD2_DATA2
31(J3)	SD2_DATA3	i.MX8M Plus	AA25	SD2_DATA3
33(J3)	GND			

35(J3)	SD1_RESET_B	i.MX8M Plus	W25	SD1_RESET_B
37(J3)	SD1_STROBE	i.MX8M Plus	W26	SD1_STROBE
39(J3)	SD1_CLK	i.MX8M Plus	W28	SD1_CLK
41(J3)	SD1_CMD	i.MX8M Plus	W29	SD1_CMD
43(J3)	GND			
45(J3)	CLKOUT1	i.MX8M Plus	K29	CLKOUT1
47(J3)	CLKIN1	i.MX8M Plus	K28	CLKIN1
49(J3)	GND			
51(J3)	LVDS0_TX3_N	i.MX8M Plus	J28	LVDS0_D3_N
53(J3)	LVDS0_TX3_P	i.MX8M Plus	H29	LVDS0_D3_P
55(J3)	GND			
57(J3)	LVDS0_TX2_N	i.MX8M Plus	H28	LVDS0_D2_N
59(J3)	LVDS0_TX2_P	i.MX8M Plus	G29	LVDS0_D2_P
61(J3)	GND			
63(J3)	LVDS0_CLK_N	i.MX8M Plus	G28	LVDS0_CLK_N
65(J3)	LVDS0_CLK_P	i.MX8M Plus	F29	LVDS0_CLK_P
67(J3)	GND			
69(J3)	LVDS0_TX1N	i.MX8M Plus	F28	LVDS0_D1_N
71(J3)	LVDS0_TX1P	i.MX8M Plus	E29	LVDS0_D1_P
73(J3)	GND			
75(J3)	LVDS0TX0_N	i.MX8M Plus	E28	LVDS0_D0_N
77(J3)	LVDS0 TX0_P	i.MX8M Plus	D29	LVDS0_D0_P
79(J3)	GND			
2(J3)	ENET_MDC	i.MX8M Plus	AH28	ENET_MDC
4(J3)	ENET_MDIO	i.MX8M Plus	AH29	ENET_MDIO
6(J3)	GND			
8(J3)	ENET_TX_CTL	i.MX8M Plus	AF24	ENET_TX_CTL
10(J3)	ENET_TXC	i.MX8M Plus	AE24	ENET_TXC
12(J3)	ENET_TD0	i.MX8M Plus	AC25	ENET_TD0
14(J3)	ENET_TD1	i.MX8M Plus	AE26	ENET_TD1
16(J3)	ENET_TD2	i.MX8M Plus	AF26	ENET_TD2
18(J3)	ENET_TD3	i.MX8M Plus	AD24	ENET_TD3
20(J3)	GND			
22(J3)	SD1_DATA0	i.MX8M Plus	Y29	SD1_DATA0
24(J3)	SD1_DATA1	i.MX8M Plus	Y28	SD1_DATA1
26(J3)	SD1_DATA2	i.MX8M Plus	V29	SD1_DATA2
28(J3)	SD1_DATA3	i.MX8M Plus	V28	SD1_DATA3
30(J3)	GND			
32(J3)	SD1_DATA4	i.MX8M Plus	U26	SD1_DATA4
34(J3)	SD1_DATA5	i.MX8M Plus	AA29	SD1_DATA5
36(J3)	SD1_DATAG	i.MX8M Plus	AA28	SD1_DATA6
38(J3)	SD1_DATA7	i.MX8MPlus	U25	SD1_DATA7
40(J3)	GND			
42(J3)	NAND_DQS	i.MX8M Plus	R26	NAND_DQS
44(J3)	GND			
46(J3)	CLKOUT2	i.MX8M Plus	L29	CLKOUT2
48(J3)	CLKIN2	i.MX8M Plus	L28	CLKIN2
50(J3)	GND			
52(J3)	LVDS1_TX3_N	i.MX8M Plus	D28	LVDS1_D3_N
54(J3)	LVDS1_TX3_P	i.MX8M Plus	C29	LVDS1_D3_P
56(J3)	GND			
58(J3)	LVDS1_TX2_N	i.MX8M Plus	C28	LVDS1_D2_N
60(J3)	LVDS1_TX2_P	i.MX8M Plus	B29	LVDS1_D2_P
62(J3)	GND			
64(J3)	LVDS1_CLK_N	i.MX8M Plus	B28	LVDS1_CLK_N
66(J3)	LVDS1_CLK_P	i.MX8M Plus	A28	LVDS1_CLK_P
68(J3)	GND			
70(J3)	LVDS1_TX1_N	i.MX8M Plus	B27	LVDS1_D1_N
72(J3)	LVDS1_TX1_P	i.MX8M Plus	A27	LVDS1_D1_P
74(J3)	GND			
76(J3)	LVDS1_TX0_N	i.MX8M Plus	B26	LVDS1_D0_N
78(J3)	LVDS1_TX0_P	i.MX8M Plus	A26	LVDS1_D0_P
80(J3)	GND			

*3 **Pulled up to the power supply (LDO5 of PCA9450PCN) on the SoM via a resistor 4.7KΩ.**

2.1.4 Connection relationship between J4 and each device

Table 2-4 shows the connection relationship between the board-to-board connector (J4) and each device on the SoM.

Table 2-4 Connection relationship between J4 and each device

Connector Pin Number	Connecior Pin Name	Connected Device	Device Pin Number	Device Pad Name
1(J4)	VSYS_5V (+5.0V)	PCA9450CHN		
3(J4)				
5(J4)				
7(J4)				
9(J4)				
11(J4)				
13(J4)				
15(J4)				
17(J4)				
19(J4)				
21(J4)				
23(J4)				
25(J4)	ONOFF	i.MX8M Plus	G22	ONOFF
27(J4)	GND			
29(J4)				
31(J4)				
33(J4)				
35(J4)				
37(J4)	PMIC_32K_OUT	PCA9450CHN	7	CLK_32K_OUT
39(J4)	GND			
41(J4)	SYS_nRST	PCA9450CHN	8	PMIC_RST_B
43(J4)	POR_B*4	i.MX8M Plus	J29	POR_B
		PCA9450CHN	9	POR_B
45(J4)	GND			
47(J4)				
49(J4)				
51(J4)				
53(J4)				
55(J4)				
57(J4)				
59(J4)	JTAG_TMS	i.MX8M Plus	G-14	JTAG_TMS
61(J4)	JTAG_TDO	i.MX8M Plus	F-14	JTAG_TDO
63(J4)	JTAG_TDI	i.MX8M Plus	G16	JTAG_TDI
65(J4)	JTAG_MOD*5	i.MX8M Plus	G20	JTAG_MOD
67(J4)	JTAG_TCK	i.MX8M Plus	G18	JTAG_TCK
69(J4)	VDD_1V8 (+1.8V)	PCA9450CHN i.MX8M Plus LPDDR4 SDRAM QSPIFash eMMC		
71(J4)				
73(J4)				
75(J4)				
77(J4)				
79(J4)				
2(J4)	PMIC_ON_REQ	i.MX8M Plus	F22	PMIC_ON_REQ
		PCA9450CHN	39	PMIC_ON_REQ
4(J4)	NC			
6(J4)				
8(J4)				
10(J4)				
12(J4)				
14(J4)				
16(J4)				
18(J4)				
20(J4)				
22(J4)				
24(J4)				
26(J4)	GND			

28(J4)				
30(J4)				
32(J4)				
34(J4)				
36(J4)				
38(J4)				
40(J4)				
42(J4)				
44(J4)				
46(J4)				
48(J4)				
50(J4)				
52(J4)				
54(J4)	PMIC_SCLL	PCA9450CHN	27	SCLL
56(J4)	PMIC_SDAL	PCA9450CHN	26	SDAL
58(J4)	PMIC_SCLH	PCA9450CHN	25	SCLH
60(J4)	PMIC_SDAH	PCA9450CHN	24	SDAH
62(J4)	GND			
64(J4)	VSD_3V3 (+3.3V)	PCA9450CHN		
66(J4)				
68(J4)				
70(J4)	VDD_3V3 (+3.3V)	PCA9450CHN i.MX8M Plus eMMC		
72(J4)				
74(J4)				
76(J4)				
78(J4)				
80(J4)				

[*4] Pulled up to the power supply (LDO1 of PCA9450PCN) on the SoM through a resistor 4.7KΩ.

[*5] Pulled down through a resistor 10KΩ to ground (GND) on the SoM.

2.2 Connecting i.MX8M Plus to individual devices

LPDDR4 SDRAM, eMMC, NOR Flash, PMIC, and board-to-board connector are connected to t h e i.MX8M Plus.

The connection relationship between i.MX8M Plus and each device on the SoM is shown below.

2.2.1 Connection with LPDDR4 SDRAM

i.Table 2-5 shows the connection relationship between MX8M Plus and LPDDR4 SDRAM.

Table 2-5 Connection relationship between i . MX8M Plus and LPDDR4 SDRAM

i.MX8M Plus		LPDDR4 SDRAM	
Device Pad Name	**Pin Number**	**Pin Name**	**Pin Number**
DRAM_AC08/CA0_AA12	L6	CA0_B	R2
DRAM_AC09/CA1_A/A11	L4	CA1_B	P2
DRAM_AC10/CA2_A/A7	E4	CA2_B	R9
DRAM_AC11/CA3_A/A8	D4	CA3_B	R10
DRAM_AC12/CA4_A/A6	N4	CA4_B	R11
DRAM_AC13/CA5_A/A5	N5	CA5_B	P11
DRAM_AC02/CS0_A/CS0_n	N6	CS0_B	R4
DRAM_AC03/CS1_A/C0	J4	CS1_B	R3
DRAM_AC00/CKE0_A/CKE0	J6	CKE0_B	P4
DRAM_AC01/CKE1_A/CKE1	G5	CKE1_B	P5
DRAM_ACD4/CK_t_A/BG0	M1	CK_t_B	P8
DRAM_AC05/CK_c_A/BG1	Mega2	CK_c_B	P9
DRAM_DQ00	B3	DQ8_B	AA11
DRAM_DQ01	A2	DQ9_B	Y11
DRAM DQ02	E1	DQ10_B	V11
DRAM_DQ03	F2	DQ11_B	U11
DRAM_DQ04	E2	DQ12_B	U9
DRAM DQ05	C1	DQ13_B	V9
DRAM_DQ06	C2	DQ14_B	Y9

DRAM_DQ07	B1	DQ15_B	AA9
DRAM_DQ08	G1	DQ0_B	AA2
DRAM_DQ09	H1	DQ1_B	Y2
DRAM_DQ10	K1	DQ5_B	V4
DRAM DQ11	K2	DQ2_B	V2
DRAM_DQ12	L2	DQ3_B	U2
DRAM_DQ13	L1	DQ4_B	U4
DRAM_DQ14	G2	DQ7_B	AA4
DRAM_DQ15	F1	DQ6_B	Y4
DRAM_DM0	B2	DMI1_B	Y10
DRAM_DM1	H2	DM10_B	Y3
DRAM_DQSO_P	D2	DQS1_t_B	W10
DRAM_DQSO_N	D1	DQS1_c_B	V10
DRAM_DQS1_P	J2	DQS0_t_B	W3
DRAM_DQS1_N	J1	DQS0_c_B	V3
DRAM_AC28/CA0_B/A13	W4	CA0_A	H2
DRAM_AC29/CA1_B/BA0	W5	CA1_A	J2
DRAM_AC30/CA2_B/A10(AP)	AE4	CA2_A	H9
DRAM_AC31/CA3_B/A0	AF4	CA3_A	H10
DRAM_AC32/CA4_B/C2	U5	CA4_A	H11
DRAM_AC33/CA5B/CAS_n(A15)	U6	CA5_A	J11
DRAM_AC23/CS0_B/-	U4	CS0_A	H4
DRAM AC22/CS1_B/-	AA6	CS1_A	H3
DRAM_AC20/CKE0_BCK_t_B	AA4	CKE0_A	J4
DRAM_AC21/CKE1_BCK_c_B	AA5	CKE1_A	J5
DRAM_AC24/CK_t_B/A2	V2	CK_t_A	J8
DRAM_AC25/CK_c_B/A1	V1	CK_c_A	J9
DRAM_DQ16	AC1	DQ0_A	B2
DRAM_DQ17	AB1	DQ1_A	C2
DRAM_DQ18	W2	DQ3_A	F2
DRAM DQ19	Y2	DQ2_A	E2
DRAM_DQ20	Y1	DQ5_A	E4
DRAM DQ21	W	DQ4_A	F4
DRAM DQ22	AC2	DQ7_A	B4
DRAM_DQ23	AD1	DQ6_A	C4
DRAM_DQ24	AH3	DQ8_A	B11
DRAM_DQ25	AJ2	DQ9_A	C11
DRAM_DQ26	AE1	DQ10_A	E11
DRAM_DQ27	AD2	DQ11_A	F11
DRAM_DQ28	AE2	DQ12_A	F9
DRAM_DQ29	AG1	DQ13_A	E9
DRAM_DQ30	AG2	DQ14_A	C9
DRAM_DQ31	AH1	DQ15_A	B9
DRAM_DM2	AB2	DMI0_A	C3
DRAM_DM3	AH2	DMI1_A	C10
DRAM_DQS2_P	AA2	DQS0_t_A	D3
DRAM_DQS2_N	AA1	DQS0_c_A	E3
DRAM_DQS3_P	AF2	DQS1_t_A	D10
DRAM_DQS3_N	AF1	DQS1_c_A	E10

2.2.2 Connection with eMMC

i.Table 2-6 shows the connection relationship between MX8M Plus and eMMC.

Table 2-6 Connection relationship between i.MX8M Plus and eMMC

I.MX8M Plus		eMMC	
Pin Name	Pin Number	Pin Name	Pin Number
NAND_WE_B	U28	CLK	M6
NAND_WP_B	U29	CMD	M5
NAND_DATA04	P29	DAT0	A3
NAND_DATA05	N29	DAT1	A4
NAND_DATA06	M29	DAT2	A5
NAND_DATA07	R29	DAT3	B2
NAND_RE_B	R28	DAT4	B3
NAND_CE2_B	P28	DAT5	B4
NAND_CE3_B	N28	DAT6	B5
NAND_CLE	M28	DAT7	BG

2.2.3 Connection with SPI NOR Flash

i.Table 2-7 shows the connection relationship between the MX8M Plus and SPI NOR Flash.

Table 2-7 Connection relationship between i . MX8M Plus and SPI NOR Flash

I.MX8M Plus		SPI Flash	
Pin Name	Pin Number	Pin Name	Pin Number
NAND_ALE	N25	C	6
NAND_CE0_B	L26	sadist	1
NAND_DATA00	R25	DQ0	5
NAND_DATA01	L25	DQ1	2
NAND_DATA02	L24	DQ2	3
NAND_DATA03	N24	DQ3	7

2.2.4 Connection with PMIC (PCA9450CHN)

i.Table 2-8 shows the connection relationship between MX8M Plus and PMIC (PCA9450CHN).

Table 2-8 Connection relationship between i.MX8M Plus and PMIC (PCA9450CHN)

i.MX8M Plus		PMIC	
Pin Name	Pin Number	Pin Name	Pin Number
PMIC_ON_REQ	F22	PMIC_ON_REQ	39
PMIC_STBY_REQ	J24	PMIC_STBY_REQ	40
GPI01_IO02	B6	WDOG_B	28
POR_B	J29	POR_B	9
GPIO1_IO03	D6	IRQ_B	13
I2C1_SCL	AC8	SCL	41
I2C1_SDA	AH7	SDA	42
GPIO1_IO04	E6	SD_VSEL	29
SD2_RESET_B	AD28	SW_EN	12

2.2.5 Connection to other devices

i.Table 2-9 shows the connection relationship between MX8M Plus and other devices.

Table 2-9 Connections between i.MX8M Plus and other devices

i.MX8M Plus		Device	
Pin Name	Pin Number	Device	Pin(e.g. hairpin, bowling pin, etc.)
RTC_XTALI	J25	crystal oscillator 32.768KHz	
RTC_XTALO	J26		
XTALI_24M	G25	crystal oscillator 24MHz	
XTALO_24M	G26		
NAND_READY_B	T28	LED[*6]	gate pin

[*6] Setting NAND_READY_B to High level turns on the LED.

2.3 Connection between PMIC (PCA9450CHN) and each device

Table 2-10 shows the connection relationship between the PMIC (PCA9450CHN) and each device.

Table 2-10 Connection relationship between PMIC (PCA9450CHN) and each device

PMIC(PDN9450CHN)		Destination Device	Pin Name	Pin Number
Pin Name	Pin Number			
PMIC_RST_B	8	Connector J4	SYS_nRST	41

PMIC_ON_REQ	39	i.MX8M Plus	PMIC_ON_REQ	F22
		Connector J4	PMIC_ON_REQ	2
PMIC_STBY_REQ	40	i.MX8M Plus	PMIC_STBY_REQ	J24
WDOG_B	28	i.MX8M Plus	GPIO1_IO02	B6
		Connector J2	WDOG_B	3
POR_B	9	i.MX8M Plus	POR_B	J29
		Connector J4	POR_B	43
IRQ_B	13	i.MX8M Plus	GPIO1_IO03*1	D6
SCL	41	i.MX8M Plus	12C1_SCL	AC8
SDA	42	i.MX8M Plus	12C1_SDA	AH7
SCLL	27	Connector J4	PMIC_SCLL	54
SDAL	26	Connector J4	PMIC_SDAL	56
SCLH	25	Connector J4	PMIC_SCLH	58
SDAH	24	Connector J4	PMIC_SDAH	60
SD_VSEL	29	i.MX8M Plus	GPIO1_IO04	E6
SW_EN	12	i.MX8M Plus	SD2_RESET_B	AD28
		Connector J3	SD2_RESET_B	15
CLK_32K_OUT	7	Connector J4	PMIC_32K_OUT	37
XTAL_IN	10	crystal oscillator 32.768kHz		
XTAL_OUT	11			

[*1] OD output signal on the PMIC side. internal pull-up should be enabled in the i.MX8M Plus settings.

2.4 Functional connections

2.4.1 boot mode

At SoC startup, the state of the BOOT_MODE[3:0] pins is detected to determine how to boot the SoC.

On the SoM, since it is directly connected to the board-to-board connector, the boot method selection must be set from the carrier board by pull-up/pull-down or other means.

Connector Pin Number	Connecior Pin Name	i.MX8M Plus Pin Number	Device Pad Number
14(J2)	BOOT_MODE0	Group of Ten	BOOT_MODE0
16(J2)	BOOT_MODE1	F8	BOOT_MODE1
18(J2)	BOOT_MODE2	G8	BOOT_MODE2
20(J2)	BOOT_MODE3	G12	BOOT_MODE3

3 Electrical Specifications

3.1 power (button on TV, etc.)

The power input to the SoM is a single power input from the board-to-board connector, and three types of power generated from the power input are output from the board-to-board connector on the SoM.

All power outputs from the SoM are connected to the PMIC (PCN9450CHN) mounted on the SoM.

All power supplies used on the SoM are connected to the PMIC (PCA9450CHN).

3.2 SoM power input/output

- Power input: VSYS_5V (+5V)
- Power supply output: VDD_3V3 (+3.3V)
  VSD_3V3 (+3.3V) VDD_1V8 (+1.8V)

The voltage values for each power supply output in parentheses ( ) above are the voltage values when standard settings are made for the PMIC, and will vary depending on the values set. The allowable power supply input voltage also varies depending on the value set in the PMIC. For details, refer to the PCN9450CHN data sheet or other documents.

3.2.1 Power supply block diagram

All power inputs from the board-to-board connector are fed into the PMIC, which generates the respective power supplies and outputs them from the board-to-board connector.

The power supply dependencies between each device are shown in Figure 3-1.

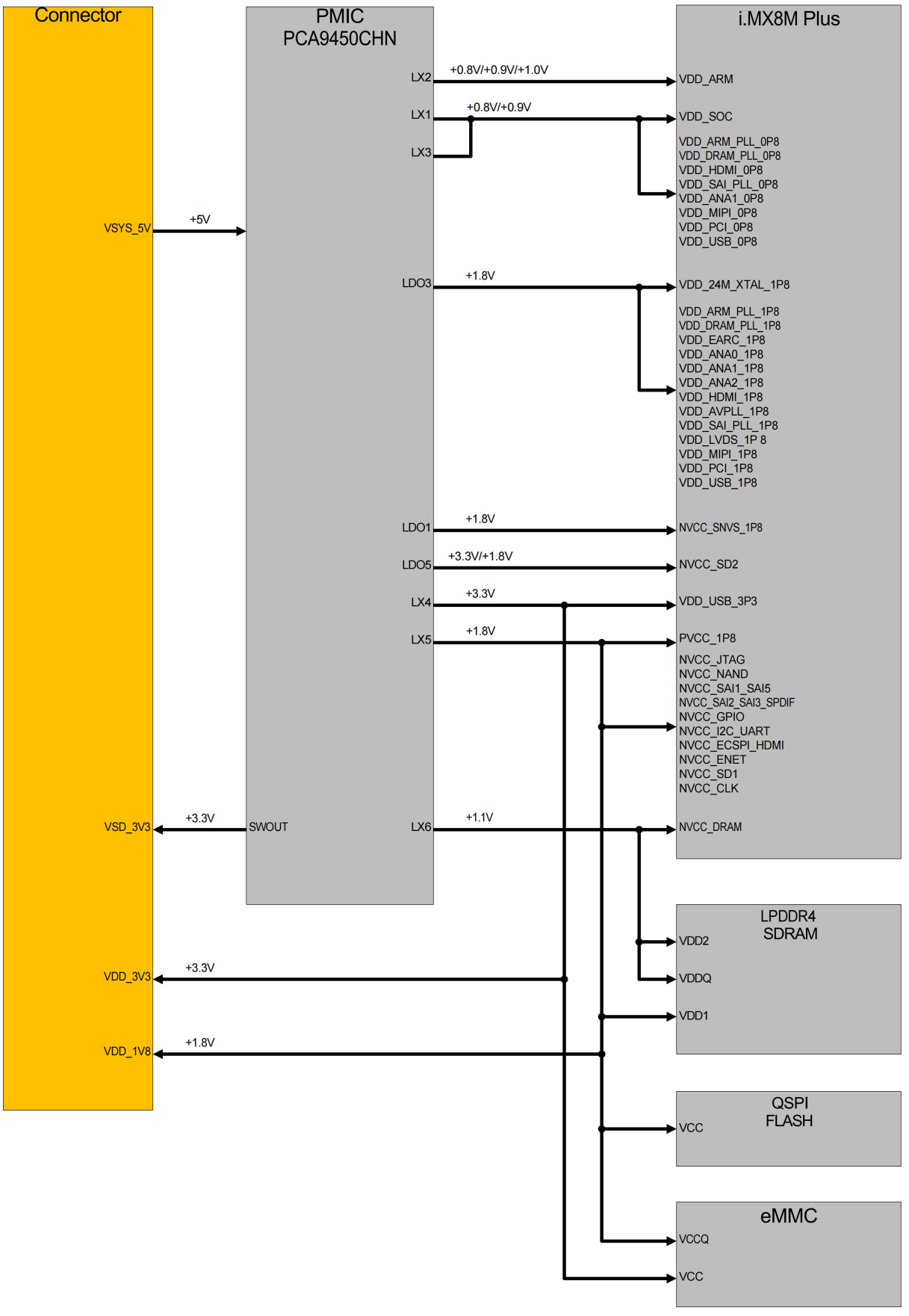


Figure 3-1 Power supply block diagram

3.2.2 Output current

The maximum current of each power supply output generated from the PMIC (PCA9450CHN) and the connection relationship between each power supply output and each device on the SoM are shown in the table below.

Table 3-1 Maximum current of each power supply output and connection relationship

PMIC(PCA9450CHN)			Destination Device	Connection Pin Name
Pin-Outs	**Operating Voltage**	**Maximum Curent**		
LX1 LX3	+0.8V /+0.9V	6.0A	i.MX8M Plus	VDD_SOC VDD_ARM_PLL_0P8 VDD_DRAM_PLL_0P8 VDD_HDMI_0P8 VDD_SALPLL_0P8 VDD_ANA1_0P8 VDD_MIPI_0P8 VDD_PCI_0P8 VDD_US_0P8
LX2	+0.8V /+0.9V /+1.0V	3.0A	i.MX8M Plus	VDD_ARM
LX4	+3.3V	3.0A	i.MX8M Plus	VDD_USB_3P3

			eMMC	VCC
			Connector J4	VDD_3V3
LX5	+1.8V	2.0A	i.MX8M Plus	PVCC_1P8 NVCC_JTAG NVCC_NAND NVCC_SAI1_SAI5 NVCC_SAI2_SAI3_SPDIF NVCC_GPIO NVCC_I2C_UART NVCC_ECSPL_HDMI NVCC_ENET NVCC_SD1 NVCC_CLK
			LPDDR4 SDRAM	VDD1
			QSPIFLASH	VCC
			eMMC	VCCQ
			ConnectorJ4	VDD_1V8
LX6	+1.1V	2.0A	i.MX8M Plus	NVCC_DRAM
			LPDDR4 SDRAM	VDD2 VDDQ
LDO1	+1.8V	10mA	I.MX8M Plus	NVCC_SNVS_1P8
LDO3	+1.8V	300mA	i.MX8M Plus	VDD_24M_XTAL_1P8 VDD_ARM_PLL_1P8 VDD_[DRAM_PLL_1P8 VDD_EARC_1P8 VDD_ANA0_1P8 VDD_ANA1_1P8 VDD_ANA2_1P8 VDD_HDML_1P8 VDD_AVPLL_1P8 VDD_SAI_PLL_1P8 VDD_IVDS_1P8 VDD_MIPI_1P8 VDD_PCI_1P8 VDD_USB_1P8
LDO5	+3.3V /+1.8V	150mA	i.MX8M Plus	NVCC_SD2
SWOUT	+3.3V	400mA	Connector J4	VSD_3V3

For each power supply output from the PMIC (PCA9450CHN), check the operating conditions of the device to be connected and set the appropriate operating voltage before use.

As for the power output from the connector, some power supplies are used concurrently by devices on the SoM, so please consider the maximum current before using them.

3.3 signal

Please design the SoM in consideration of the specifications of each device on the SoM and the settings made by the software, and observe the signal levels, signal timing, etc.

4 mechanical specification

4.1 board

- Board Dimensions
  50mm x 21mm x 3.4mm
- Component mounting surface
  Maximum height: 1.48mm (SoC part)
- connector surface
  Maximum height: 1.2mm (inductor part)

4.2 Holes for fixing substrates

4.2.1 connection

- Ground (signal name: GND) connection

4.2.2 Hole size

- Hole diameter: 1.6mm
- Pad outer diameter: 3.15mm

4.2.3 Hole position

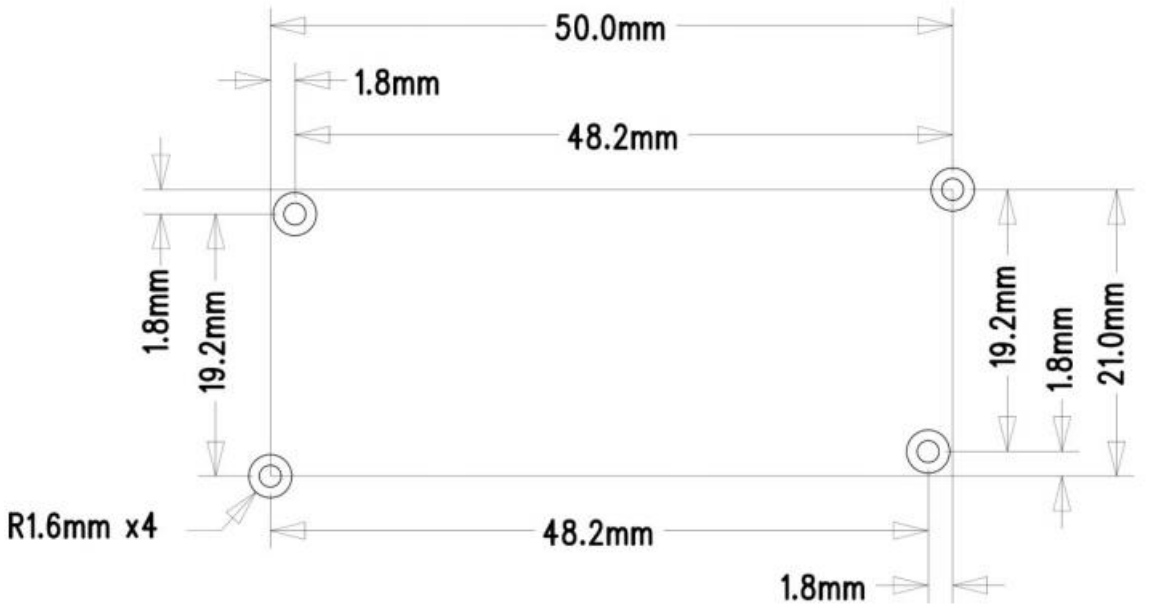


Figure 4-1 Hole Position Dimensions

4.3 Board to Board Connector

4.3.1 Connector Model No.

- J1, J2: 100-pole header connector DF40C-100DP-0.4V(51) manufactured by Hirose Electric Co.
  - Mating compatible connector model number
    Mating height 1.5mm: DF40C-100DS-0.4V(51)
- J3, J4: Hirose 80-pole header connector DF40C-80DP-0.4V(51)
  - Mating compatible connector model number
    Mating height 1.5mm: DF40C-80DS-0.4V(51)

4.3.2 Connector position

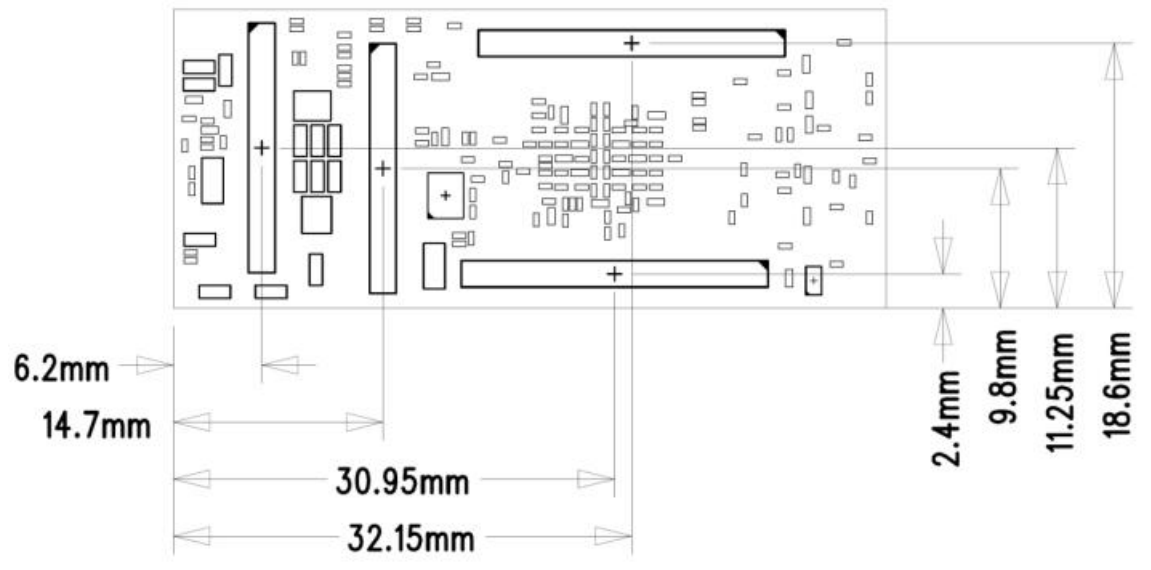


Figure 4-2 Connector Position Dimensions (Bottom View)

4.4 main components

4.4.1 Part Location

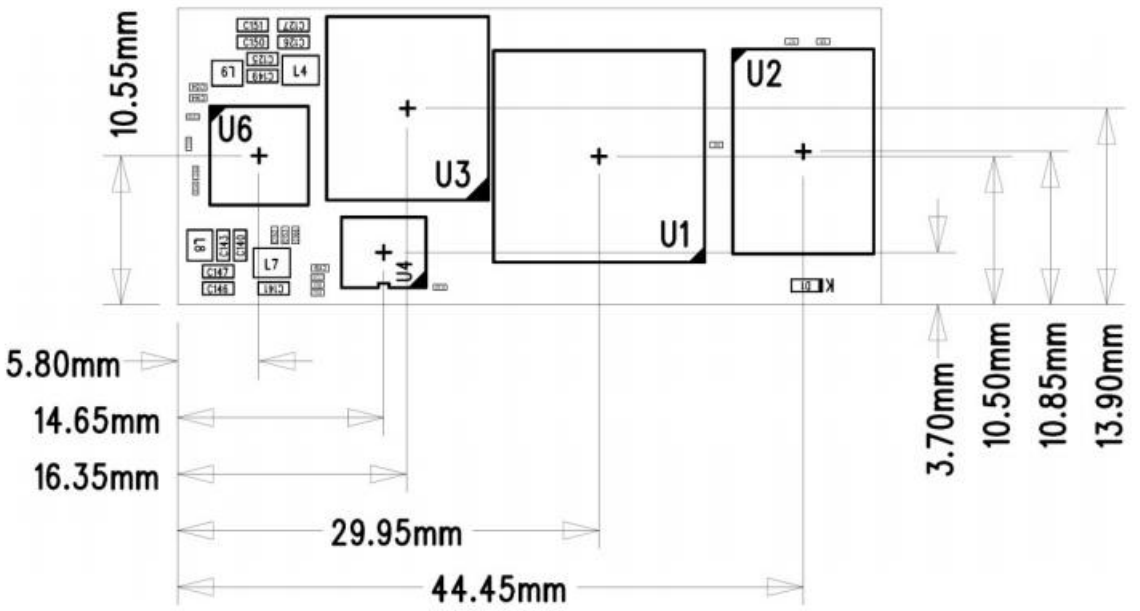


Figure 4-3 Part position dimensions (Top View)

4.4.2 Part height

U1: 1.1mm to 1.4mm
U2: 0.5mm to 0.7mm
U3: 0.5mm to 0.7mm
U4: 0.7mm to 0.8mm
U6: 0.8mm to 1.0mm
L4, L7, L8, L9: ~1.2mm

4.5 Precautions for mounting components on the carrier board side

To avoid interference with components on the SoM side, design the SoM so that no components are mounted on the carrier board side where it faces the SoM.

5 Notes on carrier board design

In this SoM, most signals are directly connected from each device on the SoM to the board-to-board connector. (Some signals are processed by pull-ups, pull-downs, etc.) It is recommended that the design be based on the i.MX8M Plus Hardware Developer's Guide provided by NXP Semiconductors.

5.1 Wiring Design

Signals connected to board-to-board connectors contain high-speed signals. When wiring high-speed signals, design with impedance control and wiring length in mind

5.1.1 differential signal

For wiring of differential signals, impedance control between pairs is required. On the carrier board, design the wiring in consideration of impedance as shown in the table below.

Table 5-1 Impedance of differential signals

i.MX8M Plus Instance	Target Impedance	Differenial Pair	Connector Pin Name	Connector Pin Number	i.MX8M Plus Pad Name
PCIE1	85Ω	PCIE_RX	PCIE_RXP	49(J2)	PCIE_RXN_P
			PCIE_RXN	47(J2)	PCIE_RXN_N
		PCIE_TX	PCIE_TXP	55(J2)	PCIE_TXN_P
			PCIE TXN	53(J2)	PCIE_TXN_N
		PCIE_CLK	PCIE_CLKP	61(J2)	PCIE_REF_PAD_CLK_P
			PCIE_CLKN	59(J2)	PCIE_REF_PAD_CLK_N
USB1	90Ω	USB2.0	USB1_DP	43(J2)	USB1_D_P
			USB1_DN	41(J2)	USB1_D_N
	85Ω	USB3.0 RX	USB1_RXP	29(J2)	USB1_RX_P
			USB1_RXN	31(J2)	USB1_RX_N
		USB3.0 TX	USB1 TXP	35(J2)	USB1_TX_P
			USB1_TXN	37(J2)	USB1_TX_N
USB2	90Ω	USB2.0	USB2_DP	65(J2)	USB2_D_P
			USB2_DN	67(J2)	USB2_D_N
	85Ω	USB3.0 RX	USB2_RXP	30(J2)	USB2_RX_P
			USB2_RXN	28(J2)	USB2_RX_N
		USB3.0 TX	USB2_TXP	36(J2)	USB2_TX_P
			USB2_TXN	34(J2)	USB2_TX_N
HDMI	100Ω	HDMI_TXC	HDMI TXCP	79(J1)	HDMI_TXC_P
			HDMI TXCN	77(J1)	HDMI_TXC_N
		HDMI_TX0	HDMI_TXP0	85(J1)	HDMI_TX0_P
			HDMI_TXN0	83(J1)	HDMI_TX0_N
		HDMI_TX1	HDMI_TXP1	91(J1)	HDMI_TX1_P
			HDMI_TXN1	89(J1)	HDMI_TX1_N
		HDMI_TX2	HDMI TXP2	97(J1)	HDMI_TX2_P
			HDMI_TXN2	95(J1)	HDMI_TX2_N
MIPI CSI1	100Ω	CSI1_CLK	CSI1_CKP	83(J2)	MIPI_CSI1_CLK_P
			CSI1_CKN	85(J2)	MIPI_CSI1_CLK_N
		CSI1_D0	CSI1_DP0	71(J2)	MIPI_CSI1_D0_P
			CSI1_DN0	73(J2)	MIPI_CSI1_D0_N
		CSI1_D1	CSI1_DP1	77(J2)	MIPI_CSI1_D1
			CS1_DN1	79(J2)	MIPI_CSI1_D1_N
		CSI1_D2	CSI1_DP2	89(J2)	MIPI_CSI1_D2_P
			CSI1_DN2	91(J2)	MIPI_CSI1_D2_N
		CSI1_D3	CSI1_DP3	95(J2)	MIPI_CSI1_D3_P
			CSI1_DN3	97(J2)	MIPI_CSI1_D3_N
MIPI CSI2	100Ω	CSI2_CLK	CSI2_CKP	82(J2)	MIPI_CSI2_CLK_P
			CSI2_CKN	84(J2)	MIPI_CSI2_CLK_N
		CSI2_D0	CSI2_DP0	94(J2)	MIPI_CSI2_D0_P
			CSI2_DN0	96(J2)	MIPI_CSI2_D0_N
		CSI2_D1	CSI2 DP1	88(J2)	MIPI_CSI2_D1_P
			CSI2 DN1	90(J2)	MIPI_CSI2_D1_N
		CSI2_D2	CSI2_DP2	76(J2)	MIPI_CSI2_D2_P
			CSI2_DN2	78(J2)	MIPI_CSI2_D2_N
		CSI2_D3	CSI2_DP3	70(J2)	MIPI_CSI2_D3_P
			CSI2_DN3	72(J2)	MIPI_CSI2_D3_N

MIPI DSI1	100Ω	DSI_CLK	DSI_CKP	52(J2)	MIPI_DSI1_CLK_P
			DSL_CKN	54(J2)	MIPI_DSI1_CLK_N
		DSI_D0	DSI_DP0	40(J2)	MIPI_DSI1_D0_P
			DSI_DN0	42(J2)	MIPI_DSI1_D0_N
		DSI_D1	DSI_DP1	46(J2)	MIPI_DSI1_D1_P
			DSLDN1	48(J2)	MIPI_DSI1_D1_N
		DSI_D2	DSI_DP2	58(J2)	MIPI_DSI1_D2_P
			DSI_DN2	60(J2)	MIPI_DSI1_D2_N
		DSI_D3	DSI_DP3	64(J2)	MIPI_DSI1_D3_P
			DSI_DN3	66(J2)	MIPI_DSI1_D3_N
LVDS0	100Ω	LVDS0_CLK	LVDSO_CLK_P	63(J3)	LVDS0_CLK_P
			LVDSO_CLK_N	61(J3)	LVDS0_CLK_N
		LVDS0_TX0	LVDS0_TX0_P	75(J3)	LVDS0_D0_P
			LVDS0_TX0_N	73(J3)	LVDS0_D0_N
		LVDS0_TX1	LVDS0_TX1_P	69(J3)	LVDS0_D1_P
			LVDS0_TX1_N	67(J3)	LVDS0_D1_N
		LVDS0_TX2	LVDS0_TX2_P	57(J3)	LVDS0_D2_P
			LVDS0_TX2_N	55(J3)	LVDS0_D2_N
		LVDS0_TX3	LVDS0_TX3_P	51(J3)	LVDS0_D3_P
			LVDS0_TX3_N	49(J3)	LVDS0_D3_N
LVDS1	100Ω	LVDS1_CLK	LVDS1_CLK_P	64(J3)	LVDS1_CLK_P
			LVDS1_CLK_N	62(J3)	LVDS1_CLK_N
		LVDS1_TX0	LVDS1_TX0_P	76(J3)	LVDS1_D0_P
			LVDS1_TX0_N	74(J3)	LVDS1_D0_N
		LVDS1_TX1	LVDS1_TX1_P	70(J3)	LVDS1_D1_P
			LVDS1_TX1_N	68(J3)	LVDS1_D1_N
		LVDS1_TX2	LVDS1_TX2_P	58(J3)	LVDS1_D2_P
			LVDS1_TX2_N	56(J3)	LVDS1_D2_N
		LVDS1_TX3	LVDS1_TX3_P	52(J3)	LVDS1_D3_P
			LVDS1_TX3_N	50(J3)	LVDS1_D3_N

5.1.2 single-ended signal

All single-ended signals other than differential signals should be wired with an impedance of 50Ω.

5.1.3 isometric line

Since signals such as Ethernet (RGMII), SDHC, HDMI, MIPI CSI, MIPI DSI, and LVDS operate at high speeds in synchronization with kick signals, care should be taken to wire them as equally long as possible.

6 Update History

Version Revision	Update Date	Contents
Provisional Rev1.0	30/6/2025	Creation of a provisional version