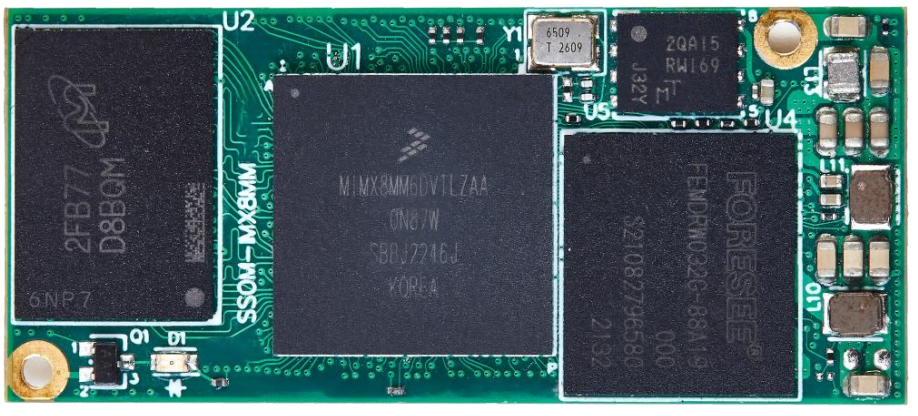
Bit-Brick SSOM-IMX8MM datasheet



Provisional version

V 1.0

Bit Brick Technology Corporation

June 30, 2025

1 Summary

SSOM-IMX8MM is an ultra-compact SoM (System on Module) with NXP's i.MX8M Mini application processor.

The SoM includes LPDDR4 SDRAM, eMMC, NOR Flash, power monitoring IC (PMIC), and three board-to- board connectors as peripheral devices connected to the i.MX8M Mini.

Since most of the SoC (i.MX 8M Mini) signals can be connected through the board-to-board connector, most of the SoC functions are available.

Designed for compatibility with NXP's development kit (i.MX 8M Mini EVK), the same functionality as the development kit can be achieved. This makes it easy to maintain compatibility with software provided by NXP.

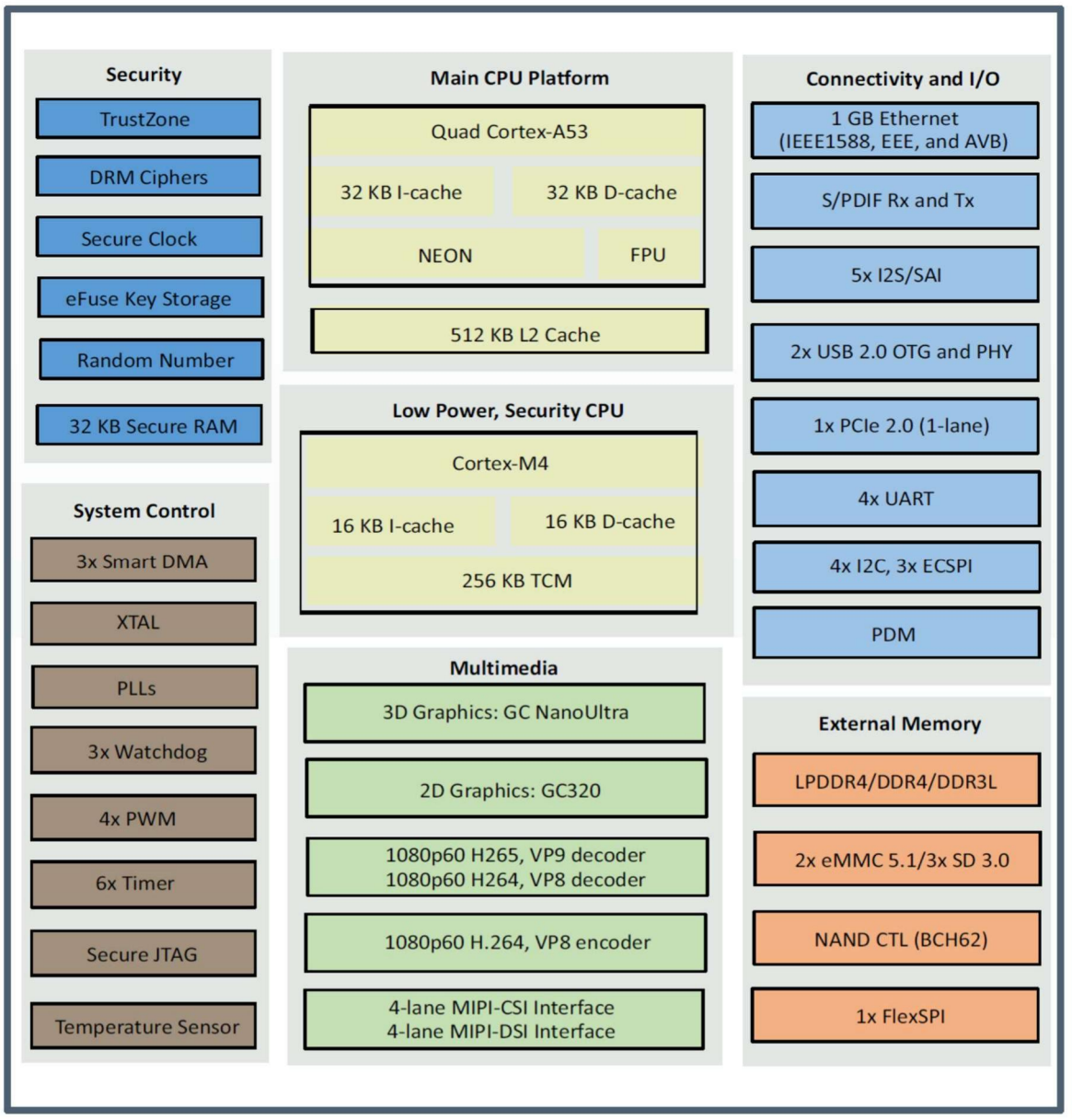
1.1 device

- SoC: NXP i.MX8M Mini
  - Cortex A53 4-core, maximum operating frequency 1.8 GHz
  - Cortex M4 1 core Maximum operating frequency 400MHz
- LPDDR4: SDRAM up to 4GB (to be determined)
- eMMC: up to 64 GB (to be determined)
- QSPI NOR FLASH: 32 MB (to be determined)
- Power monitoring IC: PCA9450AAHN from NXP (to be determined)
- Board-to-board connector (3 pcs)
  - 80-pin connector (3 pcs.)

1.2 Feature

The following functions can be configured with the on-board SoC (i.MX8M Mini). (Not all functions are available at the same time.)

- PCI Express
  - 1 lane 1 channel
- USB 2.0
  - Built-in PHY 2 channels
- MIPI DSI Interface
  - 4 lanes, 1 channel
- MIPI CSI Interface
  - 4 lanes, 1 channel
- Ethernet Interface
  - RGMII interface 1 channel
- audio interface
  - Digital audio (SAI) Up to 5 channels
  - SPDIF interface 1 channel
- SD Card Interface
  - SDIO 2 channels
- Other
  - UART 4 channels
  - SPI 3 channels
  - I2C 4 channels
  - GPIO



1.2.1 System Configuration Example

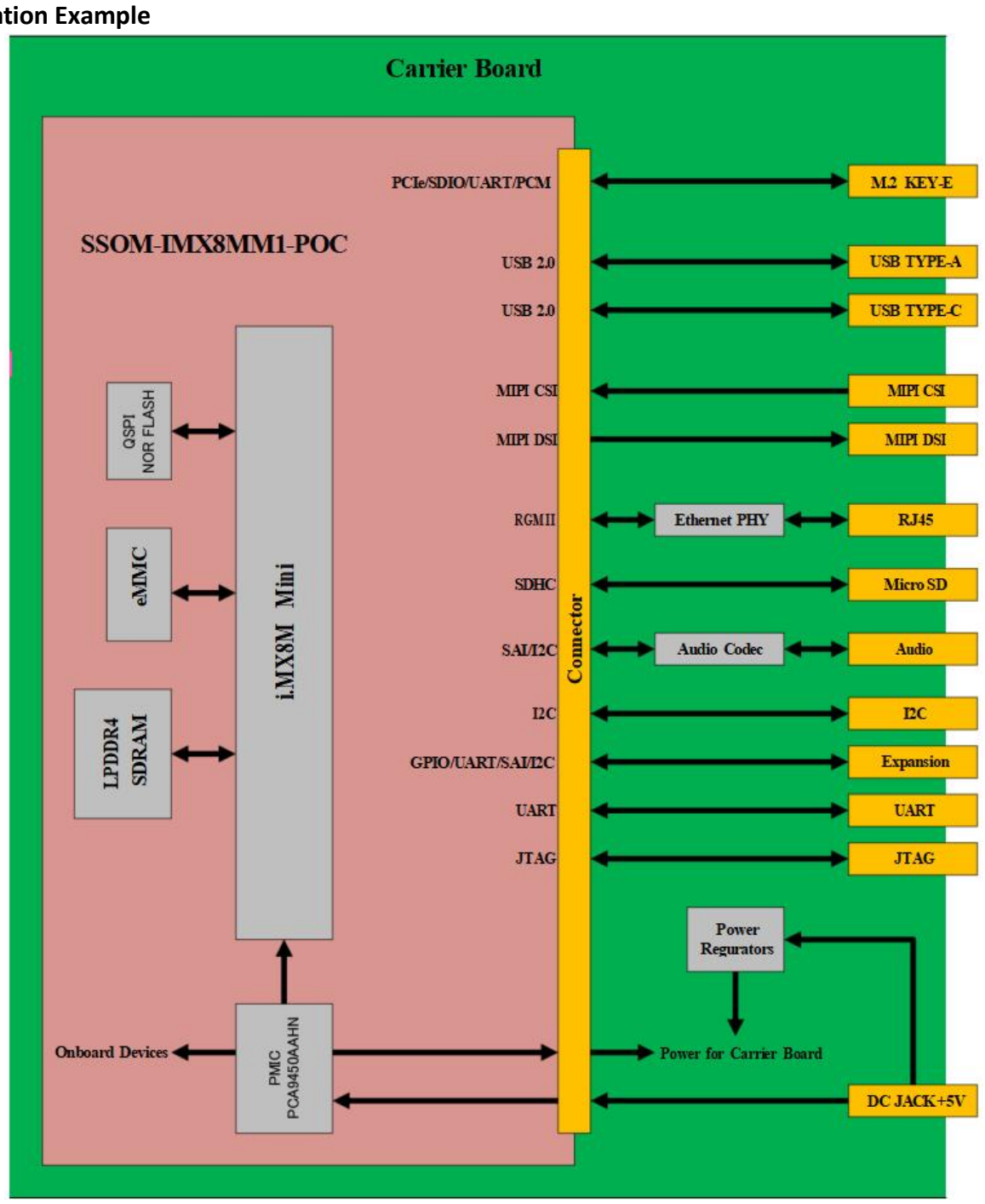


Fig.1-1 System Configuration Example

2 Signal Connection

All signals available from this SoM are compatible with those of the SoM in the NXP development kit (i.MX 8M Mini EVK). Signal connections are equivalent to those of the SoM in NXP's development kit (i.MX 8M Mini EVK), except for signal pin assignments due to connector changes. For details, please refer to the schematic of NXP's development kit (i.MX 8M Mini EVK).

2.1 Board-to-board connector and connection of each device

The board-to-board connector is connected to the i.MX8M Mini signals and the PMIC (PCA9450AAHN) signals and power input/output.

The following shows the connection relationship between board-to-board connectors (J1 to J3) and each device on the SoM.

2.1.1 Connection relationship between J1 and each device

Connection relationship between board-to-board connector (J1) and each device on the SoM Table 2-1 Table 21 shows the connection between the board-to-board connector (J1) and each device on the SoM.

Table 2-1 Connection relationship between J1 and each device

Connector Pin (e.g. hairpin, Bowling pin, etc.) Number	Connector Pin Name	Connected Device	Device Pin (e.g. hairpin, bowling pin, etc.) Number	Device Pad Name
1 (J1)	UART2_RXD	i.MX8M Mini	F15	UART2_RXD
3 (J1)	UART2_TXD	i.MX8M Mini	E15	UART2_TXD
5 (J1)	I2C4_SCL	i.MX8M Mini	D13	I2C4_SCL
7 (J1)	I2C4_SDA	i.MX8M Mini	E13	I2C4_SDA
9 (J1)	GND			
11 (J1)	I2C3_SCL *1	i.MX8M Mini	E10	I2C3_SCL
13 (J1)	I2C3_SDA *1	i.MX8M Mini	F10	I2C3_SDA
15 (J1)	I2C2_SCL *1	i.MX8M Mini	D10	I2C2_SCL
17 (J1)	I2C2_SDA *1	i.MX8M Mini	D9	I2C2_SDA
19 (J1)	GND			
21 (J1)	DSI_DN0	i.MX8M Mini	A9	MIPI_DSI_D0_N
23 (J1)	DSI_DP0	i.MX8M Mini	B9	MIPI_DSI_D0_P
25 (J1)	GND			
27 (J1)	DSI_DN1	i.MX8M Mini	A10	MIPI_DSI_D1_N
29 (J1)	DSI_DP1	i.MX8M Mini	B10	MIPI_DSI_D1_P
31 (J1)	GND			
33 (J1)	DSI_CKN	i.MX8M Mini	A11	MIPI_DSI_CLK_N
35 (J1)	DSI_CKP	i.MX8M Mini	B11	MIPI_DSI_CLK_P
37 (J1)	GND			
39 (J1)	DSI_DN2	i.MX8M Mini	A12	MIPI_DSI_D2_N
41 (J1)	DSI_DP2	i.MX8M Mini	B12	MIPI_DSI_D2_P
43 (J1)	GND			
45 (J1)	DSI_DN3	i.MX8M Mini	A13	MIPI_DSI_D3_N
47 (J1)	DSI_DP3	i.MX8M Mini	B13	MIPI_DSI_D3_P
49 (J1)	GND			
51 (J1)	UART1_TXD	i.MX8M Mini	F13	UART1_TXD
53 (J1)	UART1_RXD	i.MX8M Mini	E14	UART1_RXD
55 (J1)	UART1_RTS	i.MX8M Mini	D18	UART3_TXD
57 (J1)	UART1_CTS	i.MX8M Mini	E18	UART3_RXD
59 (J1)	GND			
61 (J1)	UART4_TXD	i.MX8M Mini	F18	UART4_TXD
63 (J1)	UART4_RXD	i.MX8M Mini	F19	UART4_RXD
65 (J1)	GND			
67 (J1)	USB1_ID	i.MX8M Mini	D22	USB1_ID
69 (J1)	USB2_ID	i.MX8M Mini	D23	USB2_ID
71 (J1)	USB1_VBUS *2	i.MX8M Mini	F22	USB1_VBUS
73 (J1)	USB2_VBUS *2	i.MX8M Mini	F23	USB2_VBUS
75 (J1)	GND			
77 (J1)	BOOT_MODE0	i.MX8M Mini	G26	BOOT_MODE0
79 (J1)	BOOT_MODE1	i.MX8M Mini	G27	BOOT_MODE1

2 (J1)	UART3_RTS	i.MX8M Mini	B6	ECSPI1_SS0
4 (J1)	UART3_CTS	i.MX8M Mini	A7	ECSPI1_MISO
6 (J1)	UART3_RXD	i.MX8M Mini	D6	ECSPI1_SCLK
8 (J1)	UART3_TXD	i.MX8M Mini	B7	ECSPI1_MOSI
10 (J1)	GND			
12 (J1)	ECSPI2_SS0	i.MX8M Mini	A6	ECSPI2_SS0
14 (J1)	ECSPI2_SCLK	i.MX8M Mini	E6	ECSPI2_SCLK
16 (J1)	ECSPI2_MISO	i.MX8M Mini	A8	ECSPI2_MISO
18 (J1)	ECSPI2_MOSI	i.MX8M Mini	B8	ECSPI2_MOSI
20 (J1)	GND			
22 (J1)	CSI_DN0	i.MX8M Mini	A14	MIPI_CSI_D0_N
24 (J1)	CSI_DP0	i.MX8M Mini	B14	MIPI_CSI_D0_P
26 (J1)	GND			
28 (J1)	CSI_DN1	i.MX8M Mini	A15	MIPI_CSI_D1_N
30 (J1)	CSI_DP1	i.MX8M Mini	B15	MIPI_CSI_D1_P
32 (J1)	GND			
34 (J1)	CSI_CKN	i.MX8M Mini	A16	MIPI_CSI_CLK_N
36 (J1)	CSI_CKP	i.MX8M Mini	B16	MIPI_CSI_CLK_P
38 (J1)	GND			
40 (J1)	CSI_DN2	i.MX8M Mini	A17	MIPI_CSI_D2_N
42 (J1)	CSI_DP2	i.MX8M Mini	B17	MIPI_CSI_D2_P
44 (J1)	GND			
46 (J1)	CSI_DN3	i.MX8M Mini	A18	MIPI_CSI_D3_N
48 (J1)	CSI_DP3	i.MX8M Mini	B18	MIPI_CSI_D3_P
50 (J1)	GND			
52 (J1)	PCIE_RXN	i.MX8M Mini	A19	PCIE_RXN_N
54 (J1)	PCIE_RXP	i.MX8M Mini	B19	PCIE_RXN_P
56 (J1)	GND			
58 (J1)	PCIE_TXN	i.MX8M Mini	A20	PCIE_TXN_N
60 (J1)	PCIE_TXP	i.MX8M Mini	B20	PCIE_TXN_P
62 (J1)	GND			
64 (J1)	PCIE_CLKN	i.MX8M Mini	A21	PCIE_CLK_N
66 (J1)	PCIE_CLKP	i.MX8M Mini	B21	PCIE_CLK_P
68 (J1)	GND			
70 (J1)	USB1_DN	i.MX8M Mini	A22	USB1_DN
72 (J1)	USB1_DP	i.MX8M Mini	B22	USB1_DP
74 (J1)	GND			
76 (J1)	USB2_DN	i.MX8M Mini	A23	USB2_DN
78 (J1)	USB2_DP	i.MX8M Mini	B23	USB2_DP
80 (J1)	GND			

***1 It is pulled up to the power supply (VDD_ 1V8) on the SoM through a resistor 4.7K Ω .**

***2 It is connected to the i.MX8M Mini via a 30K Ω resistor on the SoM.**

2.1.2 Connection relationship between J2 and each device

The connection relationship between the board-to-board connector (J2) and each device on the SoM is shown inTable 2-2 shows the connection between the board-to-board connector (J2) and each device on the SoM.

Table 2-2 Connection relationship between J2 and each device

Connector Pin (e.g. hairpin, Bowling pin, etc.) Number	Connector Pin Name	Connected Device	Device Pin (e.g. hairpin, bowling pin, etc.) Number	Device Pad Name
1 (J2)	SAI3_TXD	i.MX8M Mini	AF6	SAI3_TXD
3 (J2)	SAI3_TXC	i.MX8M Mini	AG6	SAI3_TXC
5 (J2)	SAI3_RXD	i.MX8M Mini	AF7	SAI3_RXD
7 (J2)	SAI3_RXC	i.MX8M Mini	AG7	SAI3_RXC
9 (J2)	SAI3_RXFS	i.MX8M Mini	AG8	SAI3_RXFS
11 (J2)	GND			
13 (J2)	SPDIF_EXT_CLK	i.MX8M Mini	AF8	SPDIF_EXT_CLK
15 (J2)	SPDIF_TX	i.MX8M Mini	AF9	SPDIF_TX
17 (J2)	SPDIF_RX	i.MX8M Mini	AG9	SPDIF_RX

19 (J2)	GND			
21 (J2)	GPIO1_IO07	i.MX8M Mini	AF11	GPIO1_IO07
23 (J2)	GPIO1_IO06	i.MX8M Mini	AG11	GPIO1_IO06
25 (J2)	GPIO1_IO05	i.MX8M Mini	AF12	GPIO1_IO05
27 (J2)	GPIO1_IO01	i.MX8M Mini	AF14	GPIO1_IO01
29 (J2)	GND			
31 (J2)	SAI1_RXFS	i.MX8M Mini	AG16	SAI1_RXFS
33 (J2)	SAI1_RXC	i.MX8M Mini	AF16	SAI1_RXC
35 (J2)	SAI1_RXD0	i.MX8M Mini	AG15	SAI1_RXD0
37 (J2)	SAI1_RXD1	i.MX8M Mini	AF15	SAI1_RXD1
39 (J2)	SAI1_RXD2	i.MX8M Mini	AG17	SAI1_RXD2
41 (J2)	GND			
43 (J2)	SAI1_RXD3	i.MX8M Mini	AF17	SAI1_RXD3
45 (J2)	SAI1_RXD4	i.MX8M Mini	AG18	SAI1_RXD4
47 (J2)	SAI1_RXD5	i.MX8M Mini	AF18	SAI1_RXD5
49 (J2)	SAI1_RXD6	i.MX8M Mini	AG19	SAI1_RXD6
51 (J2)	SAI1_RXD7	i.MX8M Mini	AF19	SAI1_RXD7
53 (J2)	GND			
55 (J2)	ENET_TX_CTL	i.MX8M Mini	AF24	ENET_TX_CTL
57 (J2)	ENET_TXC	i.MX8M Mini	AG24	ENET_TXC
59 (J2)	GND			
61 (J2)	ENET_TD3	i.MX8M Mini	AF25	ENET_TD3
63 (J2)	ENET_TD2	i.MX8M Mini	AG25	ENET_TD2
65 (J2)	ENET_TD1	i.MX8M Mini	AF26	ENET_TD1
67 (J2)	ENET_TD0	i.MX8M Mini	AG26	ENET_TD0
69 (J2)	GND			
71 (J2)	ENET_RXC	i.MX8M Mini	AE26	ENET_RXC
73 (J2)	ENET_RX_CTL	i.MX8M Mini	AF27	ENET_RX_CTL
75 (J2)	ENET_MDC	i.MX8M Mini	AC27	ENET_MDC
77 (J2)	ENET_MDIO	i.MX8M Mini	AB27	ENET_MDIO
79 (J2)	NVCC_ENET	i.MX8M Mini	W22	NVCC_ENET
2 (J2)	SAI3_TXFS	i.MX8M Mini	AC6	SAI3_TXFS
4 (J2)	SAI3_MCLK	i.MX8M Mini	AD6	SAI3_MCLK
6 (J2)	GND			
8 (J2)	GPIO1_IO15	i.MX8M Mini	AB9	GPIO1_IO15
10 (J2)	GPIO1_IO14	i.MX8M Mini	AC9	GPIO1_IO14
12 (J2)	GPIO1_IO13	i.MX8M Mini	AD9	GPIO1_IO13
14 (J2)	GPIO1_IO12	i.MX8M Mini	AB10 (former Soviet Union)	GPIO1_IO12
16 (J2)	GPIO1_IO11	i.MX8M Mini	AC10	GPIO1_IO11
18 (J2)	GPIO1_IO10	i.MX8M Mini	AD10	GPIO1_IO10
20 (J2)	GPIO1_IO09	i.MX8M Mini	AF10	GPIO1_IO09
22 (J2)	GPIO1_IO08	i.MX8M Mini	AG10	GPIO1_IO08
24 (J2)	GND			
26 (J2)	PDM_DATA3	i.MX8M Mini	AC13	SAI5_RXD3
28 (J2)	PDM_DATA2	i.MX8M Mini	AD13	SAI5_RXD2
30 (J2)	PDM_DATA1	i.MX8M Mini	AC-14	SAI5_RXD1
32 (J2)	PDM_DATA0	i.MX8M Mini	AD18	SAI5_RXD0
34 (J2)	PDM_CLK	i.MX8M Mini	AC15	SAI5_RXC
36 (J2)	GND			
38 (J2)	SAI5_MCLK	i.MX8M Mini	AD15	SAI5_MCLK
40 (J2)	SAI5_RXFS	i.MX8M Mini	AB15	SAI5_RXFS
42 (J2)	GND			
44 (J2)	SAI1_TXD0	i.MX8M Mini	AG20	SAI1_TXD0
46 (J2)	SAI1_TXD1	i.MX8M Mini	AF20	SAI1_TXD1
48 (J2)	SAI1_TXD2	i.MX8M Mini	AG21	SAI1_TXD2
50 (J2)	SAI1_TXD3	i.MX8M Mini	AF21	SAI1_TXD3
52 (J2)	GND			
54 (J2)	SAI1_TXD4	i.MX8M Mini	AG22	SAI1_TXD4
56 (J2)	SAI1_TXD5	i.MX8M Mini	AF22	SAI1_TXD5

58 (J2)	SAI1_TXD6	i.MX8M Mini	AG23	SAI1_TXD6
60 (J2)	SAI1_TXD7	i.MX8M Mini	AF23	SAI1_TXD7
62 (J2)	SAI1_TXC	i.MX8M Mini	AC18	SAI1_TXC
64 (J2)	GND			
66 (J2)	SAI1_TXFS	i.MX8M Mini	AB19.	SAI1_TXFS
68 (J2)	SAI1_MCLK	i.MX8M Mini	AB18	SAI1_MCLK
70 (J2)	GND			
72 (J2)	ENET_RD0	i.MX8M Mini	AE27	ENET_RD0
74 (J2)	ENET_RD1	i.MX8M Mini	AD27	ENET_RD1
76 (J2)	ENET_RD2	i.MX8M Mini	AD26	ENET_RD2
78 (J2)	ENET_RD3	i.MX8M Mini	AC26	ENET_RD3
80 (J2)	GND			

2.1.3 Connection relationship between J3 and each device

The connection relationship between the board-to-board connector (J3) and each device on the SoM is shown intable (e.g. Table 1) 2-3 shows the connection between the board-to-board connector (J3) and each device on the SoM.

table (e.g. Table 1) 2-3 Connection relationship between J3 and each device

Connector Pin (e.g. hairpin, Bowling pin, etc.) Number	Connector Pin Name	Connected Device	Device Pin (e.g. hairpin, bowling pin, etc.) Number	Device Pad Name
1 (J3)	ONOFF*3	i.MX8M Mini	A25	ONOFF
3 (J3)	PMIC_ON_REQ	i.MX8M Mini	A24	PMIC_ON_REQ
		PCA9450AAHN	39	PMIC_ON_REQ
5 (J3)	POR_B*3	i.MX8M Mini	B24	POR_B
		PCA9450AAHN	9	POR_B
7 (J3)	REF_CLK_32K	i.MX8M Mini	AG14	GPIO1_IO00
9 (J3)	SYS_nRST	PCA9450AAHN	8	PMIC_RST_B
11 (J3)	GND			
13 (J3)	GND			
15 (J3)	GND			
17 (J3)	GND			
19 (J3)	GND			
21 (J3)	GND			
23 (J3)	GND			
25 (J3)	GND			
27 (J3)	GND			
29 (J3)	JTAG_nTRST	i.MX8M Mini	C27	JTAG_TRST_B
31 (J3)	TEST_MODE *4	i.MX8M Mini	D26	TEST_MODE
33 (J3)	JTAG_TDO	i.MX8M Mini	E26	JTAG_TDO
35 (J3)	JTAG_TDI	i.MX8M Mini	E27	JTAG_TDI
37 (J3)	JTAG_TCK *5	i.MX8M Mini	F26	JTAG_TCK
39 (J3)	JTAG_TMS	i.MX8M Mini	F27	JTAG_TMS
41 (J3)	GND			
43 (J3)	CLKIN1	i.MX8M Mini	H27	CLKIN1
45 (J3)	CLKOUT1	i.MX8M Mini	H26	CLKOUT1
47 (J3)	CLKIN2	i.MX8M Mini	J27	CLKIN2
49 (J3)	CLKOUT2	i.MX8M Mini	J26	CLKOUT2
51 (J3)	GND			
53 (J3)	SD2_DATA2	i.MX8M Mini	V24	SD2_DATA2
55 (J3)	SD2_DATA3	i.MX8M Mini	V23	SD2_DATA3
57 (J3)	SD2_CLK	i.MX8M Mini	W23	SD2_CLK
59 (J3)	SD2_CMD	i.MX8M Mini	W24	SD2_CMD
61 (J3)	GND			
63 (J3)	SD2_nRST *6	i.MX8M Mini	AB26	SD2_RESET_B
65 (J3)	SD2_DATA1	i.MX8M Mini	AB24	SD2_DATA1
67 (J3)	SD2_DATA0	i.MX8M Mini	AB23	SD2_DATA0
69 (J3)	SD2_WP	i.MX8M Mini	AA27	SD2_WP
71 (J3)	SD2_nCD	i.MX8M Mini	AA26	SD2_CD_B
73 (J3)	GND			

75 (J3)	SAI2_TXC	i.MX8M Mini	AD22	SAI2_TXC
77 (J3)	SAI2_TXFS	i.MX8M Mini	AD23	SAI2_TXFS
79 (J3)	SAI2_TXD	i.MX8M Mini	AC22	SAI2_TXD0
2 (J3)	VDD_1V8			
4 (J3)	VDD_1V8			
6 (J3)	VDD_1V8			
8 (J3)	VDD_1V8			
10 (J3)	VDD_1V8			
12 (J3)	VDD_1V8			
14 (J3)	VDD_5V			
16 (J3)	VDD_5V			
18 (J3)	VDD_5V			
20 (J3)	VDD_5V			
22 (J3)	VDD_5V			
24 (J3)	VDD_5V			
26 (J3)	VDD_5V			
28 (J3)	VDD_5V			
30 (J3)	VDD_3V3			
32 (J3)	VDD_3V3			
34 (J3)	VDD_3V3			
36 (J3)	VDD_3V3			
38 (J3)	VDD_3V3			
40 (J3)	VDD_3V3			
42 (J3)	VDD_3V3			
44 (J3)	VDD_3V3			
46 (J3)	WL_REG_ON	i.MX8M Mini	R23	SD1_RESET_B
48 (J3)	SD1_STROBE	i.MX8M Mini	R24	SD1_STROBE
50 (J3)	SD1_DATA0	i.MX8M Mini	Y27	SD1_DATA0
52 (J3)	SD1_DATA1	i.MX8M Mini	Y26	SD1_DATA1
54 (J3)	SD1_DATA2	i.MX8M Mini	T27	SD1_DATA2
56 (J3)	SD1_DATA3	i.MX8M Mini	T26	SD1_DATA3
58 (J3)	GND			
60 (J3)	WL_WAKE_DEV	i.MX8M Mini	U27	SD1_DATA4
62 (J3)	BT_WAKE_DEV	i.MX8M Mini	U26	SD1_DATA5
64 (J3)	BT_WAKE_HOST	i.MX8M Mini	W27	SD1_DATA6
66 (J3)	WL_WAKE_HOST	i.MX8M Mini	W26	SD1_DATA7
68 (J3)	SD1_CMD	i.MX8M Mini	V27	SD1_CMD
70 (J3)	SD1_CLK	i.MX8M Mini	V26	SD1_CLK
72 (J3)	GND			
74 (J3)	SAI2_MCLK	i.MX8M Mini	AD19	SAI2_MCLK
76 (J3)	SAI2_RXC	i.MX8M Mini	AB22	SAI2_RXC
78 (J3)	SAI2_RXD	i.MX8M Mini	AC24	SAI2_RXD0
80 (J3)	SAI2_RXFS	i.MX8M Mini	AC19	SAI2_RXFS

***3 It is pulled up via a 100K Ω resistor to the power supply (NVCC_SNVS_ 1V8) on the SoM.**

***4 It is pulled down through a 100K Ω resistor to ground (GND) on the SoM.**

***5 It is pulled down through a 10K Ω resistor to ground (GND) on the SoM.**

***6 It is pulled up via a resistor 4.7K Ω to the power supply (NVCC_SD2) on the SoM.**

2.2 Connecting i.MX8M Mini to each device

The i.MX8M Mini has LPDDR4 SDRAM, eMMC, NOR Flash, PMIC, and board-to-board connectors connected.

The connection relationship between the i.MX8M Mini and each device on the SoM is shown below.

2.2.1 Connection with LPDDR4 SDRAM

The connection relationship between the i.MX8M Mini and LPDDR4 SDRAM is shown intable (e.g. Table 1) 2-4 shows the connection between the i.MX8M Mini and LPDDR4 SDRAM.

table (e.g. Table 1) 2-4 Connection relationship between i.MX8M Mini and LPDDR4 SDRAM

i.MX8M Mini		LPDDR4 SDRAM	
Device Pad Name	Pin Number	Pin Name	Pin Number
DRAM_AC08	J6	CA0_B	R2
DRAM_AC09	K6	CA1_B	P2
DRAM_AC10	E4	CA2_B	R9
DRAM_AC11	D5	CA3_B	R10
DRAM_AC12	N4	CA4_B	R11
DRAM_AC13	N5	CA5_B	P11
DRAM_AC02	K4	CS0_B	R4
DRAM_AC03	J4	CS1_B	R3
DRAM_AC00	F4	CKE0_B	P4
DRAM_AC01	F5	CKE1_B	P5
DRAM_AC04	L2	CK_t_B	P8
DRAM_AC05	L1	CK_c_B	P9
DRAM_DQ00	A5	DQ8_B	AA11
DRAM_DQ01	B5	DQ9_B	Y11
DRAM_DQ02	D2	DQ10_B	V11
DRAM_DQ03	D1	DQ11_B	U11
DRAM_DQ04	C1	DQ12_B	U9
DRAM_DQ05	B1	DQ13_B	V9
DRAM_DQ06	A3	DQ14_B	Y9
DRAM_DQ07	B4	DQ15_B	AA9
DRAM_DQ08	F2	DQ0_B	AA2
DRAM_DQ09	G2	DQ1_B	Y2
DRAM_DQ10	J1	DQ5_B	V4
DRAM_DQ11	J2	DQ2_B	V2
DRAM_DQ12	K2	DQ3_B	U2
DRAM_DQ13	K1	DQ4_B	U4
DRAM_DQ14	E1	DQ7_B	AA4
DRAM_DQ15	E2	DQ6_B	Y4
DRAM_DM0	A4	DMI1_B	Y10
DRAM_DM1	F1	DMI0_B	Y3
DRAM_DQS0_P	A2	DQS1_t_B	W10
DRAM_DQS0_N	B2	DQS1_c_B	V10
DRAM_DQS1_P	G1	DQS0_t_B	W3
DRAM_DQS1_N	H1	DQS0_c_B	V3
DRAM_AC28	W6	CA0_A	H2
DRAM_AC29	V6	CA1_A	J2
DRAM_AC30	AC4	CA2_A	H9
DRAM_AC31	AD5	CA3_A	H10
DRAM_AC32	R4	CA4_A	H11
DRAM_AC33	R5	CA5_A	J11
DRAM_AC23	V4	CS0_A	H4
DRAM_AC22	W4	CS1_A	H3
DRAM_AC20	AB4	CKE0_A	J4
DRAM_AC21	AB5	CKE1_A	J5
DRAM_AC24	U2	CK_t_A	J8
DRAM_AC25	U1	CK_c_A	J9
DRAM_DQ16	AB2	DQ0_A	B2
DRAM_DQ17	AA2	DQ1_A	C2
DRAM_DQ18	W1	DQ3_A	F2

DRAM_DQ19	W2	DQ2_A	E2
DRAM_DQ20	V2	DQ5_A	E4
DRAM_DQ21	V1	DQ4_A	F4
DRAM_DQ22	AC1	DQ7_A	B4
DRAM_DQ23	AC2	DQ6_A	C4
DRAM_DQ24	AG5	DQ8_A	B11
DRAM_DQ25	AF5	DQ9_A	C11
DRAM_DQ26	AD2	DQ10_A	E11
DRAM_DQ27	AD1	DQ11_A	F11
DRAM_DQ28	AE1	DQ12_A	F9
DRAM_DQ29	AF1	DQ13_A	E9
DRAM_DQ30	AG3	DQ14_A	C9
DRAM_DQ31	AF4	DQ15_A	B9
DRAM_DM2	AB1	DMI0_A	C3
DRAM_DM3	AG4	DMI1_A	C10
DRAM_DQS2_P	AA1	DQS0_t_A	D3
DRAM_DQS2_N	Y1	DQS0_c_A	E3
DRAM DQS3_P	AG2	DQS1_t_A	D10
DRAM DQS3_N	AF2	DQS1_c_A	E10

2.2.2 Connection with eMMC

The connection relationship between the i.MX8M Mini and eMMC is shown intable (e.g. Table 1) 2-5 shows the connection relationship between the i.MX8M Mini and eMMC.

table (e.g. Table 1) 2-5 Connection relationship between i.MX8M Mini and eMMC

i.MX8M Mini		eMMC	
Pin Name	**Pin Number**	**Pin Name**	**Pin Number**
NAND_WE_B	R26	CLK	M6
NAND_WP_B	R27	CMD	M5
NAND_DATA04	Mega 26	DAT0	A3
NAND_DATA05	L26	DAT1	A4
NAND_DATA06	K26	DAT2	A5
NAND_DATA07	N26	DAT3	B2
NAND_RE_B	N27	DAT4	B3
NAND_CE2_B	M27	DAT5	B4
NAND_CE3_B	L27	DAT6	B5
NAND_CLE	K27	DAT7	B6

2.2.3 Connection with SPI NOR Flash

The connection relationship between i.MX8M Mini and SPI NOR Flash is shown intable (e.g. Table 1) 2-6 shows the connection between the i.MX8M Mini and the SPI NOR Flash.

table (e.g. Table 1) 2-6 Connection relationship between i.MX8M Mini and SPI NOR Flash

i.MX8M Mini		SPI Flash	
Pin Name	**Pin Number**	**Pin Name**	**Pin Number**
NAND_ALE	N22	c	6
NAND_CE0_B	N24	S	1
NAND_DATA00	P23	DQ0	5
NAND_DATA01	K24	DQ1	2
NAND_DATA02	K23	DQ2	3
NAND_DATA03	N23	DQ3	7

2.2.4 Connection with PMIC (PCA9450CHN)

The connection relationship between the i.MX8M Mini and the PMIC (PCA9450CHN) is shown intable (e.g. Table 1) 2-7 shows the connection relationship between the i.MX8M Mini and the PMIC (PCA9450CHN).

table (e.g. Table 1) 2-7 Connection relationship between i.MX8M Mini and PMIC (PCA9450CHN)

i.MX8M Mini		PMIC	
Pin Name	Pin Number	Pin Name	Pin Number
PMIC_ON_REQ	A24	PMIC_ON_REQ	39
PMIC_STBY_REQ	E24	PMIC_STBY_REQ	40
GPIO1_IO02	AG13	WDOG_B	28
POR_B	B24	POR_B	9
GPIO1_IO03	AF13	IRQ_B	13
I2C1_SCL	E9	SCL	41
I2C1_SDA	F9	SDA	42
GPIO1_IO04	AG12	SD_VSEL	29

2.2.5 Connection to other devices

The connection relationship between the i.MX8M Mini and other devices is shown intable (e.g. Table 1) 2-8 shows the connections between the i.MX8M Mini and other devices.

table (e.g. Table 1) 2-8 Connections between i.MX8M Mini and other devices

i.MX8M Mini		Device	
Pin Name	Pin Number	Device	Pin (e.g. hairpin, bowling pin, etc.)
RTC_XTALI	A26	PCA9450AAHN	CLK_32K_OUT
XTALI_24M	B27	crystal oscillator 24MHz	
XTALO_24M	C26		
NAND_READY_B	P26	LED *7	gate pin

***7 The LED is turned on by setting NAND_READY_B to High level.**

2.3 Connection between PMIC (PCA9450CHN) and each device

The connection relationship between the PMIC (PCA9450CHN) and each device is shown intable (e.g. Table 1) 2-9 shows the connection between the PMIC (PCA9450CHN) and each device.

table (e.g. Table 1) 2-9 Connection relationship between PMIC (PCA9450CHN) and each device

PMIC (PDN9450CHN)		Destination Device	Pin Name	Pin Number
Pin Name	Pin Number			
PMIC_RST_B	8	Connector J3	SYS_nRST	9
PMIC_ON_REQ	39	i.MX8M Mini	PMIC_ON_REQ	A24
		Connector J3	PMIC_ON_REQ	3
PMIC_STBY_REQ	40	i.MX8M Mini	PMIC_STBY_REQ	E24
WDOG_B	28	i.MX8M Mini	GPIO1_IO02	AG13
		Connector J3	WDOG_B	
POR_B	9	i.MX8M Mini	POR_B	B24
		Connector J3	POR_B	5
IRQ_B	13	i.MX8M Mini	GPIO1_IO03*8	AF24
SCL	41	i.MX8M Mini	I2C1_SCL	E9
SDA	42	i.MX8M Mini	I2C1_SDA	F9
SCLL	27	unconnected		
SDAL	26	unconnected		
SCLH	25	unconnected		
SDAH	24	unconnected		
SD_VSEL	29	i.MX8M Mini	GPIO1_IO04	AG12
SW_EN	12	VDD_3V3	3.3V power supply	
CLK_32K_OUT	7	i.MX8M Mini	RTC_XTALI	A26
XTAL_IN	10	crystal oscillator 32.768kHz		
XTAL_OUT	11			

***8 OD output signal on the PMIC side; internal pull-up should be enabled in the i.MX8M Mini settings.**

2.4 Functional connections

2.4.1 boot mode

The status of the BOOT_MODE[1:0], SAI_RXD[7:0], and SAI_TXD[7:0] pins are detected at SoC startup to determine how to boot the SoC.

On the SoM, since it is directly connected to the board-to-board connector, the choice of boot method must be set from the carrier board by pull-up/pull-down or other means.

Connector Pin (e.g. hairpin, bowling pin, etc.) Number	Connector Pin Name	i.MX8M Mini Pin (e.g. hairpin, bowling pin, etc.) Number	Device Pad Name
77 (J1)	BOOT_MODE0	G26	BOOT_MODE0
79 (J1)	BOOT_MODE1	G27	BOOT_MODE1
35 (J2)	SAI1_RXD0	AG15	SAI1_RXD0
37 (J2)	SAI1_RXD1	AF15	SAI1_RXD1
39 (J2)	SAI1_RXD2	AG17	SAI1_RXD2
43 (J2)	SAI1_RXD3	AF17	SAI1_RXD3
45 (J2)	SAI1_RXD4	AG18	SAI1_RXD4
47 (J2)	SAI1_RXD5	AF18	SAI1_RXD5
49 (J2)	SAI1_RXD6	AG19	SAI1_RXD6
51 (J2)	SAI1_RXD7	AF19	SAI1_RXD7
44 (J2)	SAI1_TXD0	AG20	SAI1_TXD0
46 (J2)	SAI1_TXD1	AF20	SAI1_TXD1
48 (J2)	SAI1_TXD2	AG21	SAI1_TXD2
50 (J2)	SAI1_TXD3	AF21	SAI1_TXD3
54 (J2)	SAI1_TXD4	AG22	SAI1_TXD4
56 (J2)	SAI1_TXD5	AF22	SAI1_TXD5
58 (J2)	SAI1_TXD6	AG23	SAI1_TXD6
60 (J2)	SAI1_TXD7	AF23	SAI1_TXD7

3 Electrical Specifications

3.1 power (button on TV, etc.)

The main power input to the SoM is a single power input from the board-to-board connector, and two types of power generated from the power input are output from the board-to-board connector on the SoM. Other IO power input for Ethenet is required.

For power output from the SoM, all power supply outputs are connected to the PMIC (PCN9450AAHN) mounted on the SoM.

All power supplies used on the SoM are connected to the PMIC (PCA9450AAHN).

3.2 SoM power input/output

- Power input: VSYS_5V (+5V)
  ENET_NVCC (+1.8V/+3.3V)
- Power supply output: VDD_3V3 (+3.3V)
  VDD_ 1V8 (+1.8V)

The voltage values for each power supply output in parentheses ( ) above are the voltage values when standard settings are made for the PMIC, and will vary depending on the values set. The allowable value for the power input voltage also varies depending on the value set for the PMIC. For details, refer to the PCN9450AAHN data sheet and other documents.

3.2.1 Power supply block diagram

All power inputs from the board-to-board connector are input to the PMIC, which generates each power supply and outputs it from the board-to-board connector; each power output generated by the PMIC is also connected to each device.

The power supply dependencies between each device are,Figure 3. 3-1 The power supply dependencies between devices are as shown in Figure 31.

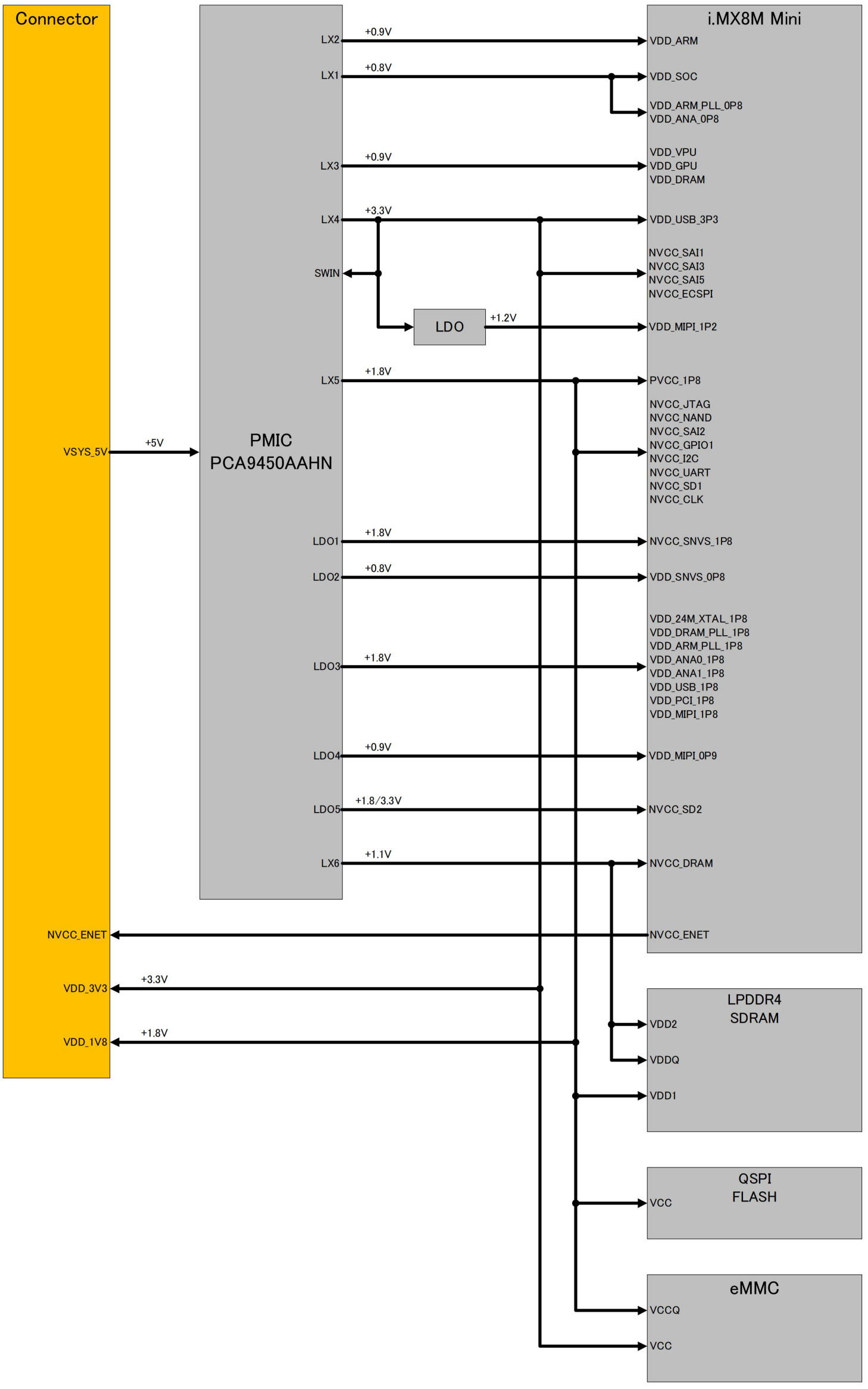


Figure 3. 3-1 Power Supply Block Diagram

3.2.2 Output current

The maximum current of each power output generated from the PMIC (PCA9450AAHN) and the connection relationship between each power output and each device on the SoM are shown in the table below.

table (e.g. Table 1) 3-1 Maximum current for each power supply output and connection relationship

PMIC (PCA9450AAHN)			Destination Device	Connection P in Name
Pin-outs	Operating Voltage	Maximum Current		
LX1	+0.95V	3.0A	i.MX8M Mini	VDD_SOC VDD_ARM_PLL_0P8 VDD_ANA_0P8
LX2	+0.85V	3.0A	i.MX8M Mini	VDD_ARM
LX3	+0.9V	3.0A	i.MX8M Mini	VDD_VPU VDD_GPU VDD_DRAM
LX4	+3.3V	3.0A	i.MX8M Mini	VDD_USB_3P3 NVCC_SAI1 NVCC_SAI3 NVCC_SAI5 NVCC_ECSPI
			eMMC	VCC
			Connector J3	VDD_3V3
LX5	+1.8V	2.0A	i.MX8M Mini	PVCC_1P8 NVCC_JTAG NVCC_NAND NVCC_SAI2 NVCC_GPIO1 NVCC_I2C NVCC_UART NVCC_SD1 NVCC_CLK
			LPDDR4 SDRAM	VDD1
			QSPI FLASH	VCC
			eMMC	VCCQ
			Connector J3	VDD_1V8
LX6	+1.1V	2.0A	i.MX8M Mini	NVCC_DRAM
			LPDDR4 SDRAM	VDD2 VDDQ
LDO1	+1.8V	10mA	i.MX8M Mini	NVCC_SNVS_1P8
LDO2	+0.85V	10mA	i.MX8M Mini	VDD_SNVS_0P8
LDO3	+1.8V	300mA	i.MX8M Mini	VDD_24M_XTAL_1P8 VDD_DRAM_PLL_1P8 VDD_ARM_PLL_1P8 VDD_ANA0_ 1P8 VDD_ANA1_ 1P8 VDD_USB_1P8 VDD_PCI_1P8 VDD_MIPI_1P8
LDO5	+3.3V/+1.8V	150mA	i.MX8M Mini	NVCC_SD2

For each power supply output from the PMIC (PCA9450AAHN), check the operating conditions of the device to be connected and set the appropriate operating voltage before use.

As for the power output from the connector, some power supplies are used concurrently by devices on the SoM, so please consider the maximum current before using them.

3.3 signal

Please design by considering the specifications of each device on this SoM and the settings made by software, and observe the signal level, signal timing, etc.

4 Mechanical Cpecification

4.1 board

- Board Dimensions
  45.5mm x 20mm x 3.8mm
- Component mounting surface
  Maximum height: 1.25mm (SoC section)
- connector surface
  Maximum height: 1.2mm (inductor part)

4.2 Holes for fixing substrates

4.2.1 connection

- Ground (signal name: GND) connection

4.2.2 Hole size

- Hole diameter: 1.6mm
- Pad outer diameter: 3.15mm

4.2.3 Hole position

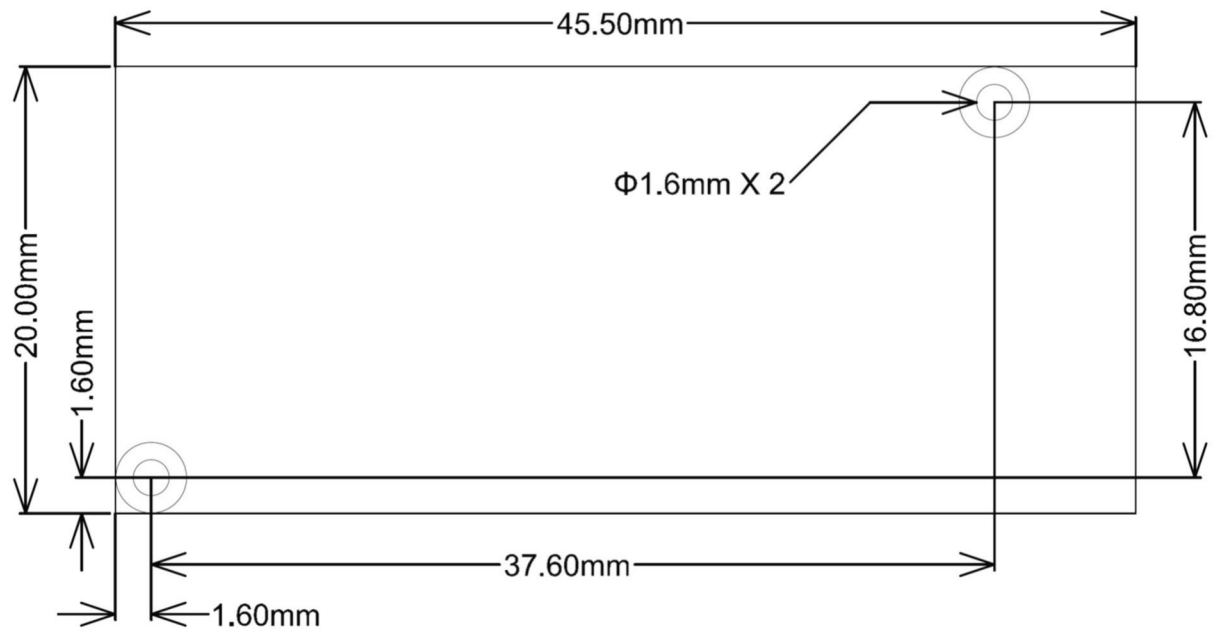


Figure 4-1 Hole Position Dimensions (Top View)

4.3 Board to Board Connector

4.3.1 Connector Model No.

- J1, J2, J3: 100-pin header connector DF40C-80DP-0.4V(51) manufactured by Hirose Electric Co.
  - Mating compatible connector model number Mating height 1.5mm: DF40C-80DS-0.4V(51)

4.3.2 Connector position

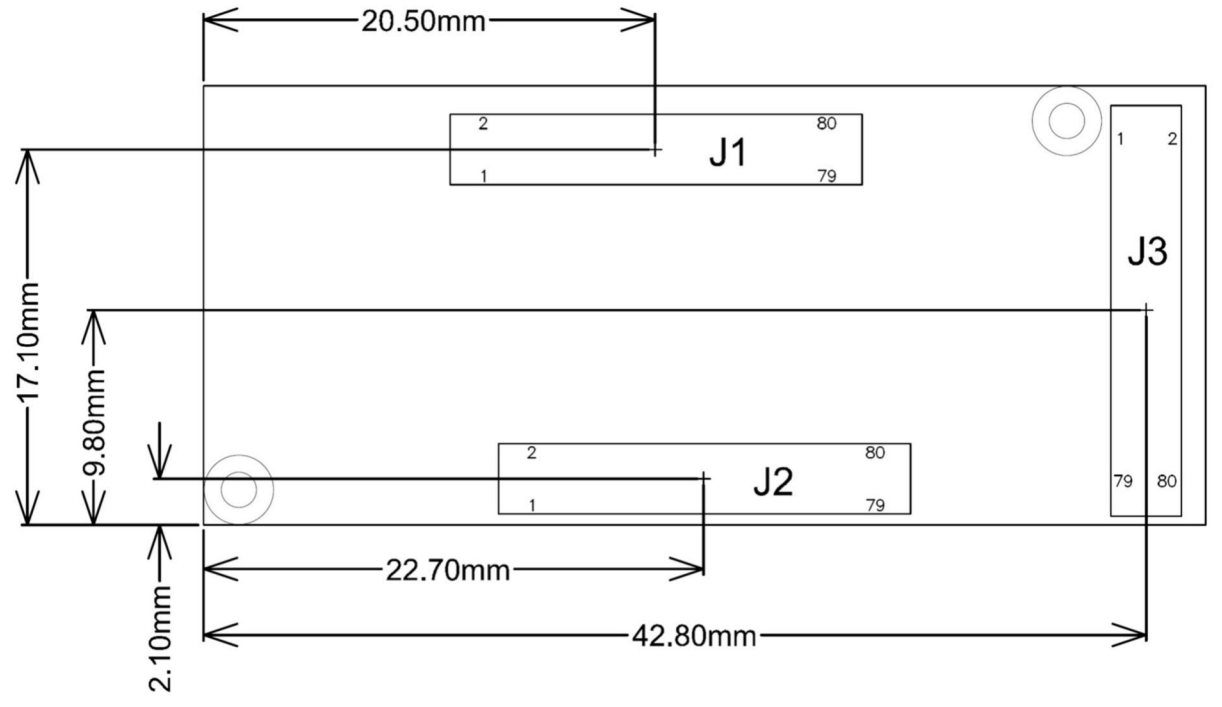


Figure 4-2 Connector Position Dimensions (Top View)

4.4 main components

4.4.1 Part Location

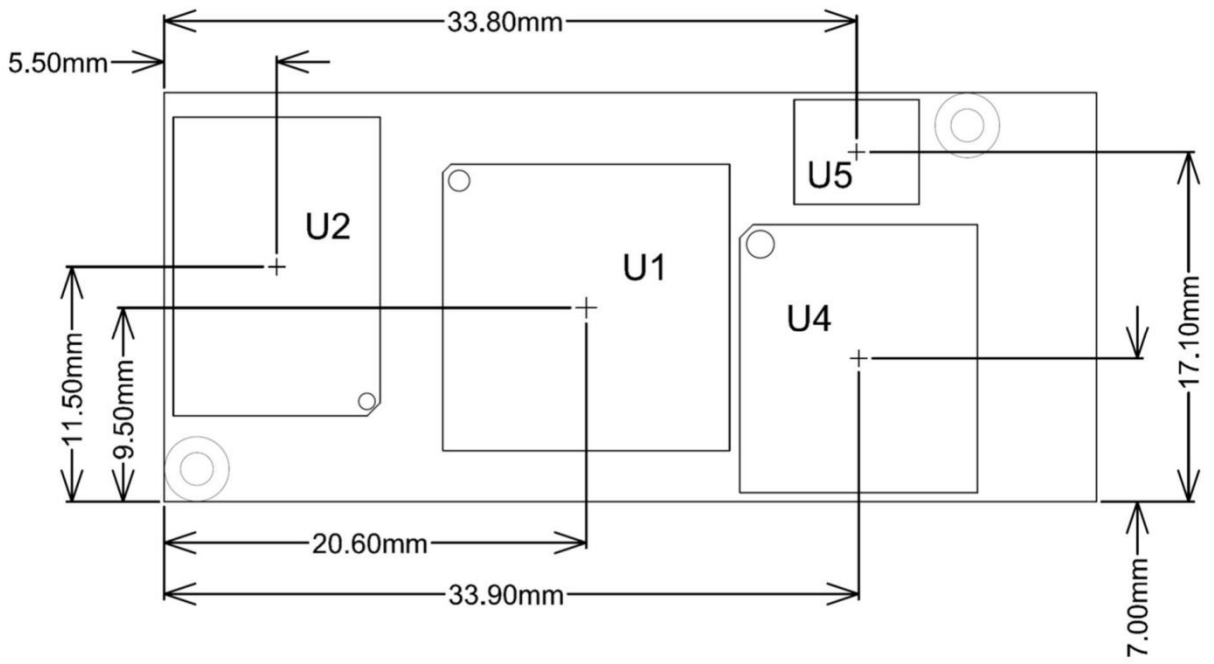


Figure 4-3 Part Position Dimensions (Top View)

4.4.2 Part height

U1: 1.05mm to 1.25mm
U2: 0.5mm to 0.7mm
U4: 0.5mm to 0.7mm
U5: 0.7mm to 0.8mm

4.5 Precautions for mounting components on the carrier board side

To avoid interference with components on the SoM side, design the carrier board so that no components are mounted on the carrier board side where it faces the SoM.

5 Notes on carrier board design

In this SoM, most signals are directly connected from each device on the SoM to the board-to-board connector. (Some signals are processed by pull-ups, pull-downs, etc.)

It is recommended that the design be based on the i.MX8M Mini Hardware Developer's Guide provided by NXP Semiconductors.

5.1 Wiring Design

Signals connected to board-to-board connectors contain high-speed signals.
When wiring high-speed signals, design with impedance control and wiring length in mind.

5.1.1 differential signal

For wiring of differential signals, impedance control between pairs is required.
On the carrier board, design the wiring in consideration of impedance as shown in the table below.

table (e.g. Table 1) 5-1 Impedance of Differential Signals

i.MX8M Mini Instance	Target. Impedance	Differential Pair	Connector Pin Name	Connector pin (e.g. hairpin, bowling pin, etc.) Number	i.MX8M Mini Pad Name
PCIE1	85Ω	PCIE_RX	PCIE_RXP	54 (J1)	PCIE_RXN_P
			PCIE_RXN	52 (J1)	PCIE_RXN_N
		PCIE_TX	PCIE_TXP	60 (J1)	PCIE_TXN_P
			PCIE_TXN	58 (J1)	PCIE_TXN_N
		PCIE_CLK	PCIE_CLKP	66 (J1)	PCIE_REF_PAD_CLK_P
			PCIE_CLKN	64 (J1)	PCIE_REF_PAD_CLK_N
USB1	90Ω	USB2.0	USB1_DP	72 (J1)	USB1_D_P
			USB1_DN	70 (J1)	USB1_D_N
USB2	90Ω	USB2.0	USB2_DP	78 (J1)	USB2_D_P
			USB2_DN	76 (J1)	USB2_D_N
MIPI CSI	100Ω	CSI_CLK	CSI_CKP	36 (J1)	MIPI_CSI1_CLK_P
			CSI_CKN	34 (J1)	MIPI_CSI1_CLK_N
		CSI_D0	CSI_DP0	24 (J1)	MIPI_CSI1_D0_P
			CSI_DN0	22 (J1)	MIPI_CSI1_D0_N
		CSI_D1	CSI_DP1	30 (J1)	MIPI_CSI1_D1_P
			CSI_DN1	28 (J1)	MIPI_CSI1_D1_N
		CSI_D2	CSI_DP2	42 (J1)	MIPI_CSI1_D2_P
			CSI_DN2	40 (J1)	MIPI_CSI1_D2_N
		CSI_D3	CSI_DP3	48 (J1)	MIPI_CSI1_D3_P
			CSI_DN3	46 (J1)	MIPI_CSI1_D3_N
MIPI DSI	100Ω	DSI_CLK	DSI_CKP	35 (J1)	MIPI_DSI1_CLK_P
			DSI_CKN	33 (J1)	MIPI_DSI1_CLK_N
		DSI_D0	DSI_DP0	23 (J1)	MIPI_DSI1_D0_P
			DSI_DN0	21 (J1)	MIPI_DSI1_D0_N
		DSI_D1	DSI_DP1	29 (J1)	MIPI_DSI1_D1_P
			DSI_DN1	27 (J1)	MIPI_DSI1_D1_N
		DSI_D2	DSI_DP2	41 (J1)	MIPI_DSI1_D2_P
			DSI_DN2	39 (J1)	MIPI_DSI1_D2_N
		DSI_D3	DSI_DP3	47 (J1)	MIPI_DSI1_D3_P
			DSI_DN3	45 (J1)	MIPI_DSI1_D3_N

5.1.2 single-ended signal

All single-ended signals other than differential signals should be wired with an impedance of 50 Ω .

5.1.3 isometric line

Since signals such as Ethernet (RGMII), SDHC, MIPI CSI, and MIPI DSI operate at high speeds in synchronization with clock signals, care should be taken to wire them at equal lengths whenever possible.

6 Update History

Version Revision	Update Date	Contents
Provisional Rev1.0	30/6/2025	Creation of a provisional version