RK3588 SMARC V2.1

Main Functions Introduction

1) PMIC: 1xRK806-1+DiscretePower
2) RAM: 2xLPDDR4/4X_32bi
3) ROM: eMMC5.1(Default) or SPI Flash
4) Support: 1xSDMMC3.0 Card
5) Support: 1 x TYPEC3.0(With DP TX)+1 x USB3.0 HOST+ 1 x USB20 HOST or USB3.0/2.0 HUB
6) Support: 3 x SATA3.0 Connector (7pin) or SATA PM
7) Support: 1 x 4Lane PCIe3.0 Connector (Dual Mode)
8) Support: 2 x 4Lanes MIPI DPHY RX Camera
9) Support: 2 x 4Lanes MIPI D/CPHY RX Camera
10) Support: 1 x HDMI2.0 RX
11) Support: 2 x HDMI2.1 TX or 2 x eDP1.3 TX
12) Support: 2 x 4Lanes MIPI D/CHY-TX
13) Support: 1xVGA Connector(DP to VGA)
14) Support: 1x4Lanes DP Port
15) Support: a/b/g/n/ac/ax 2T2R WIFI 6/5(PCIE/SDIO) +BT5.0
16) Support: 1x 10/100/1000 RJ45 Port(RGMII)
17) Support: 1x 10/100/1000 RJ45 Port(PCIE)
18) Support: 4G Module
19) Support: PCIE M.2
20) Support: 1xHeadphone+2xSPK+1xAnalog MIC

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Note

The power suffix S0 or S3 means:

S3: Keep power On during sleeping

S0:Power off during sleeping

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Description

Note

Option

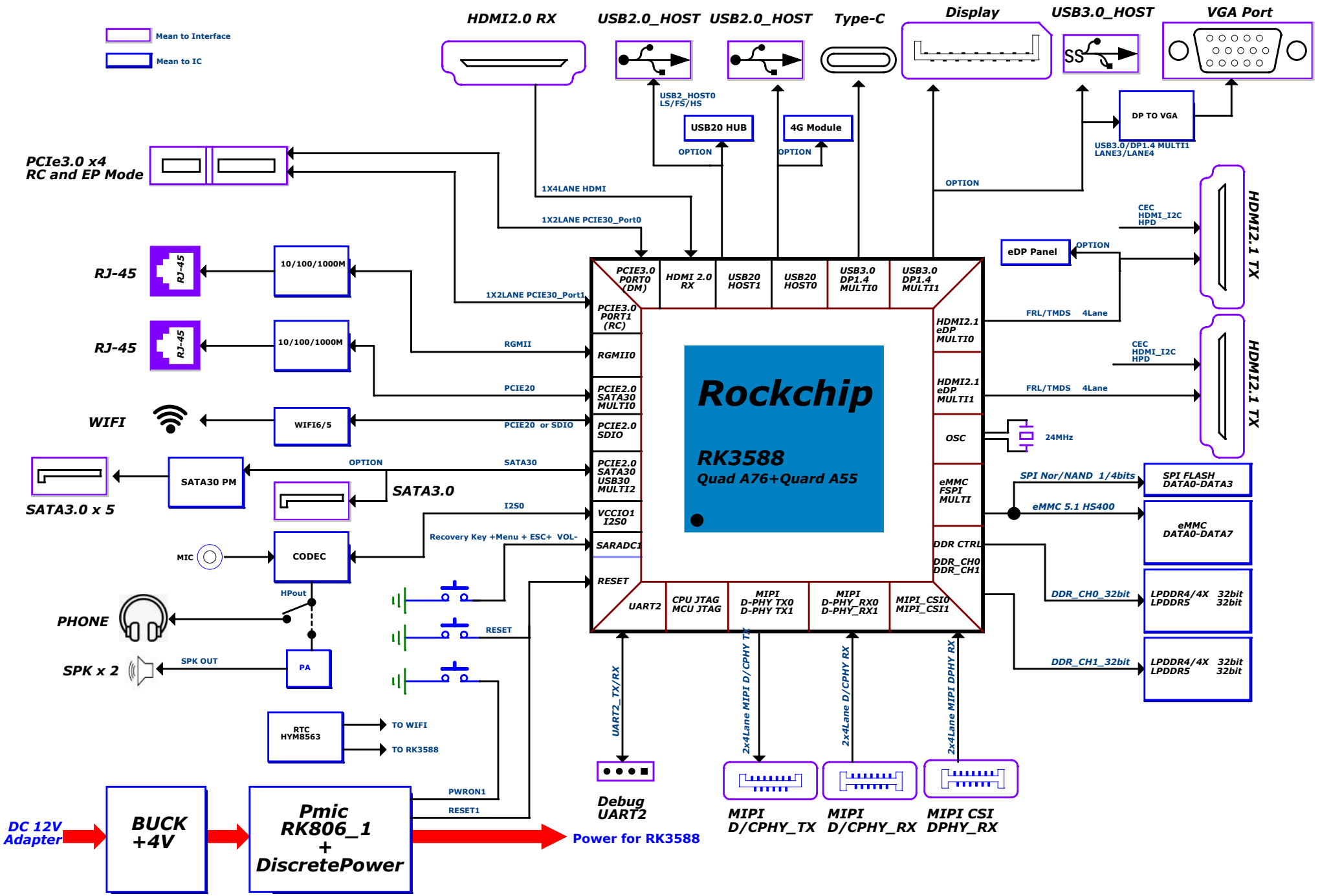
Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2025-03-18	Bzliu	1:Revision preliminary version	



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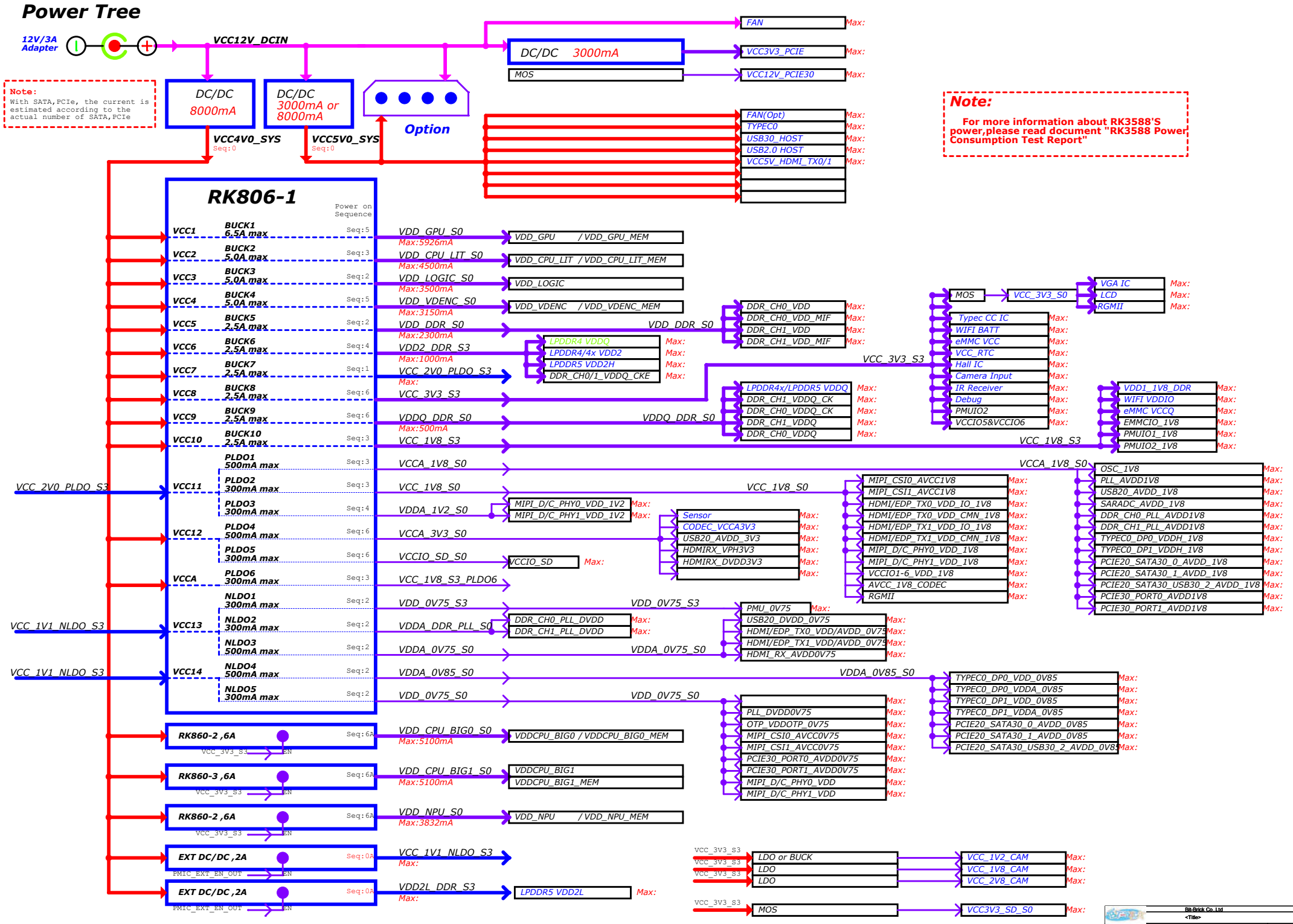
Power Tree



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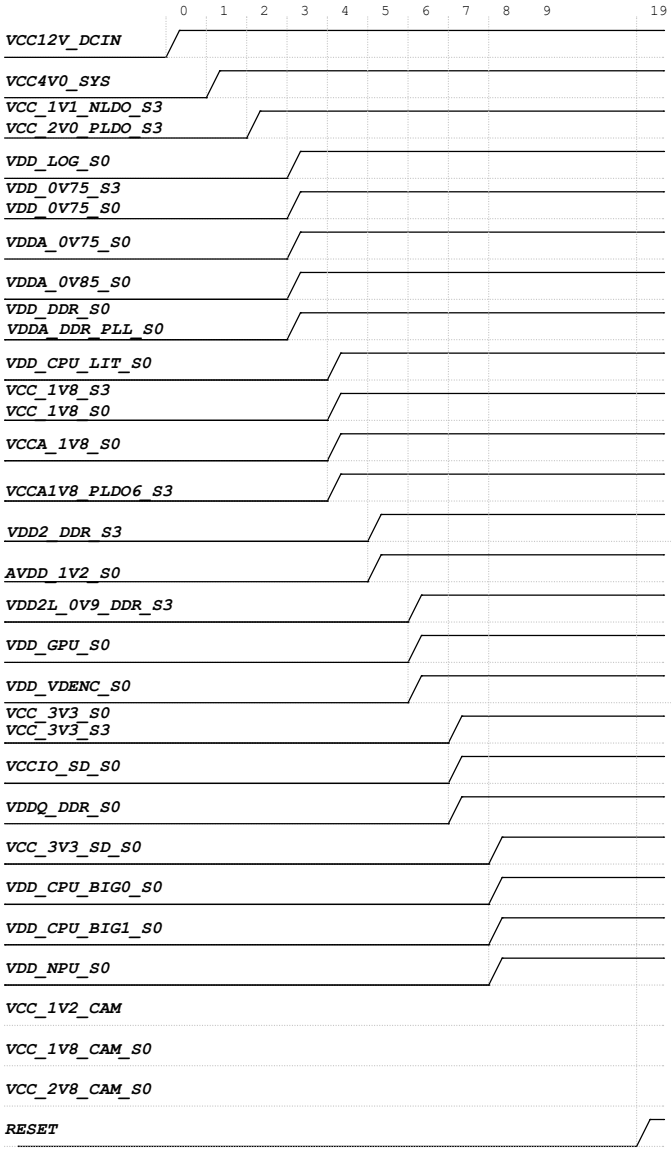
Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

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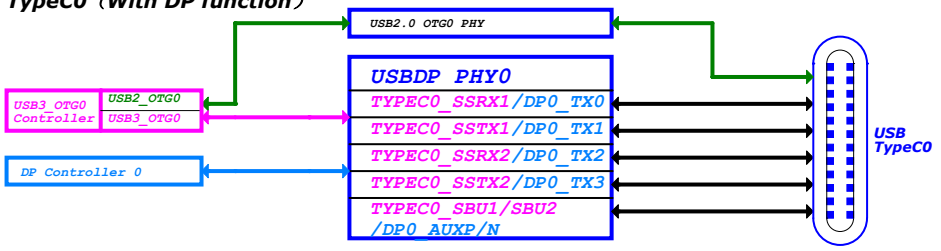
USB Controller Configure Table

Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1N/DP0_TX1N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1N/DP1_TX1N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

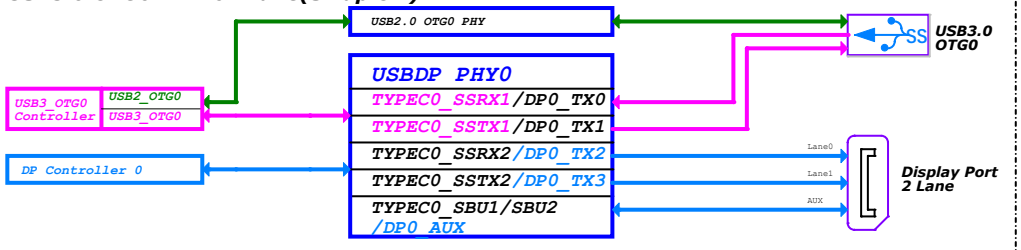
			OPTION1 USB30 HOST	OPTION2 USB30 HOST	OPTION3 USB30 HOST
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM		
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM			USB20_HOST1_DP USB20_HOST1_DM	
					TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

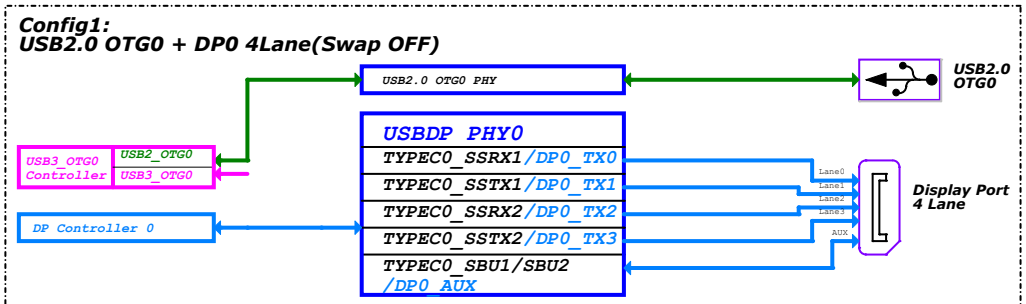
Config0:
TypeC0（With DP function）



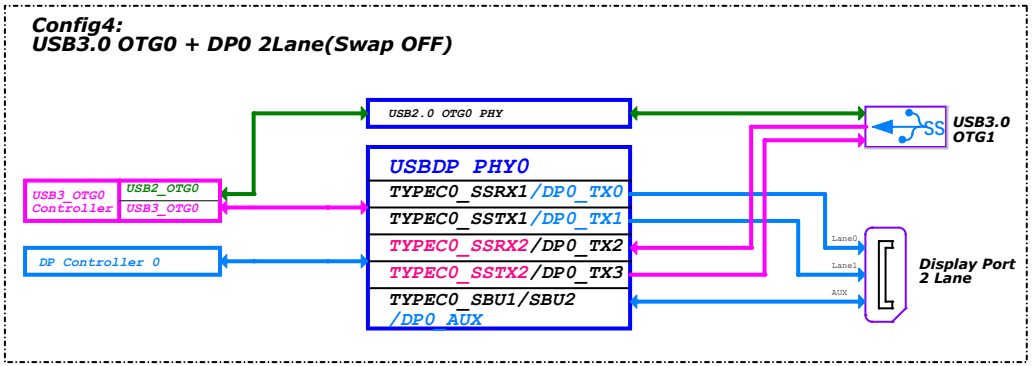
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



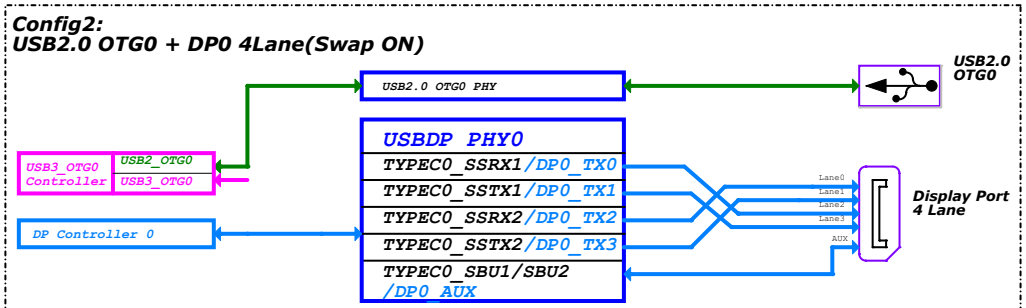
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



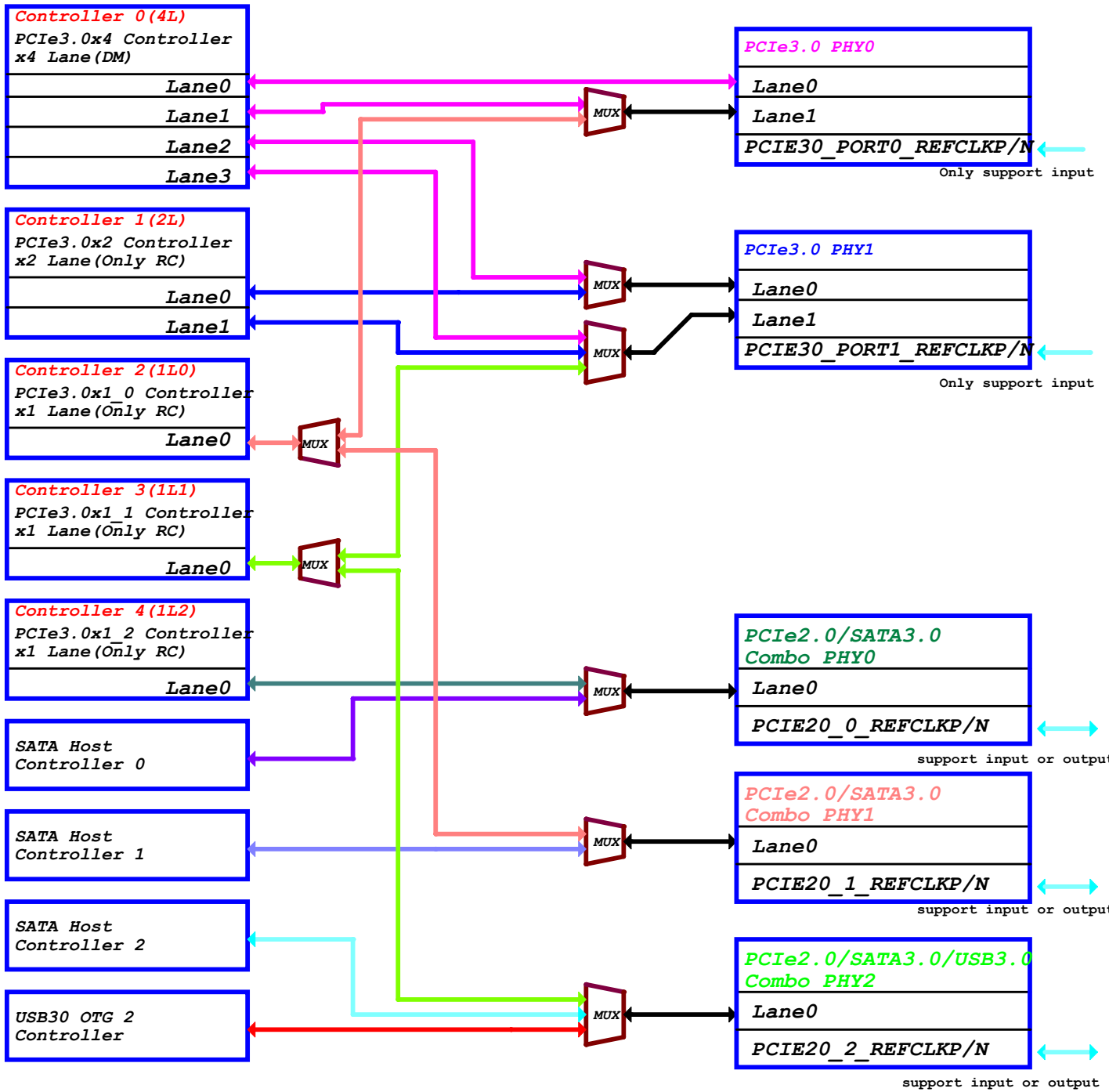
Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M*
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M*
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

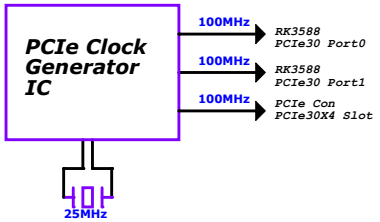
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

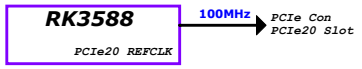
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



PCIe2.0 REFCLK



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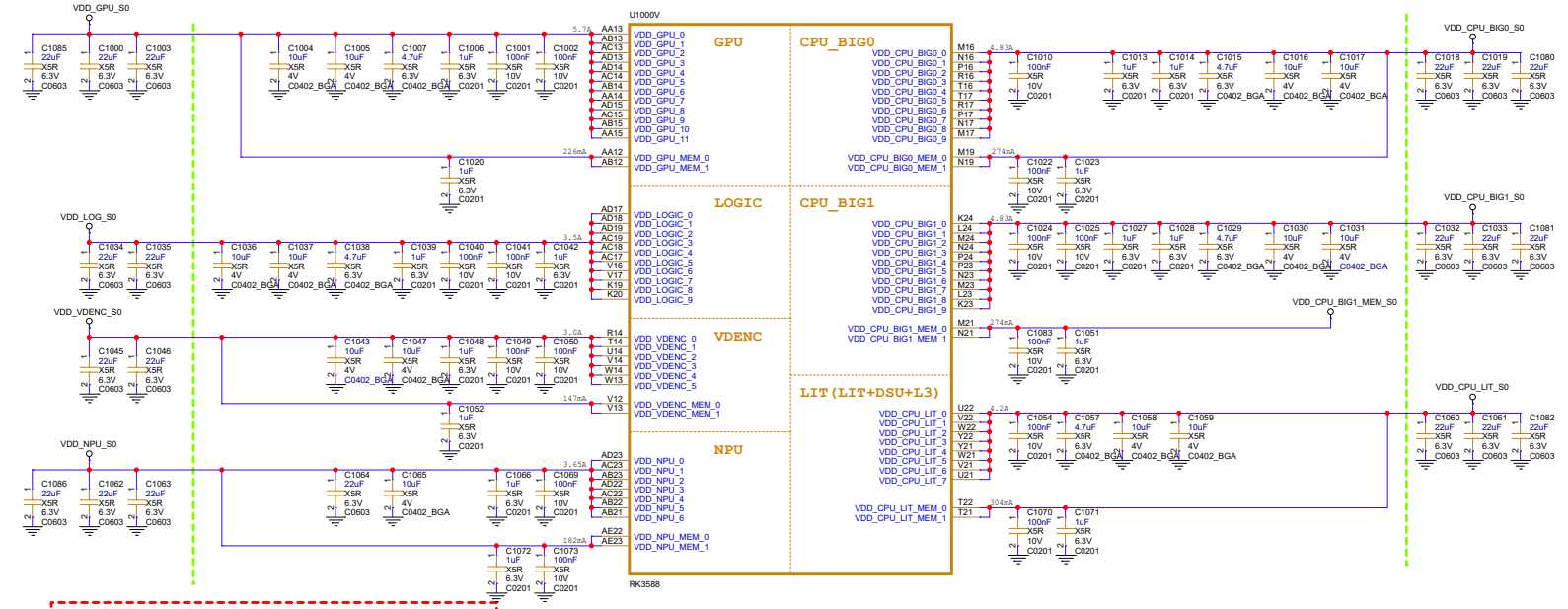
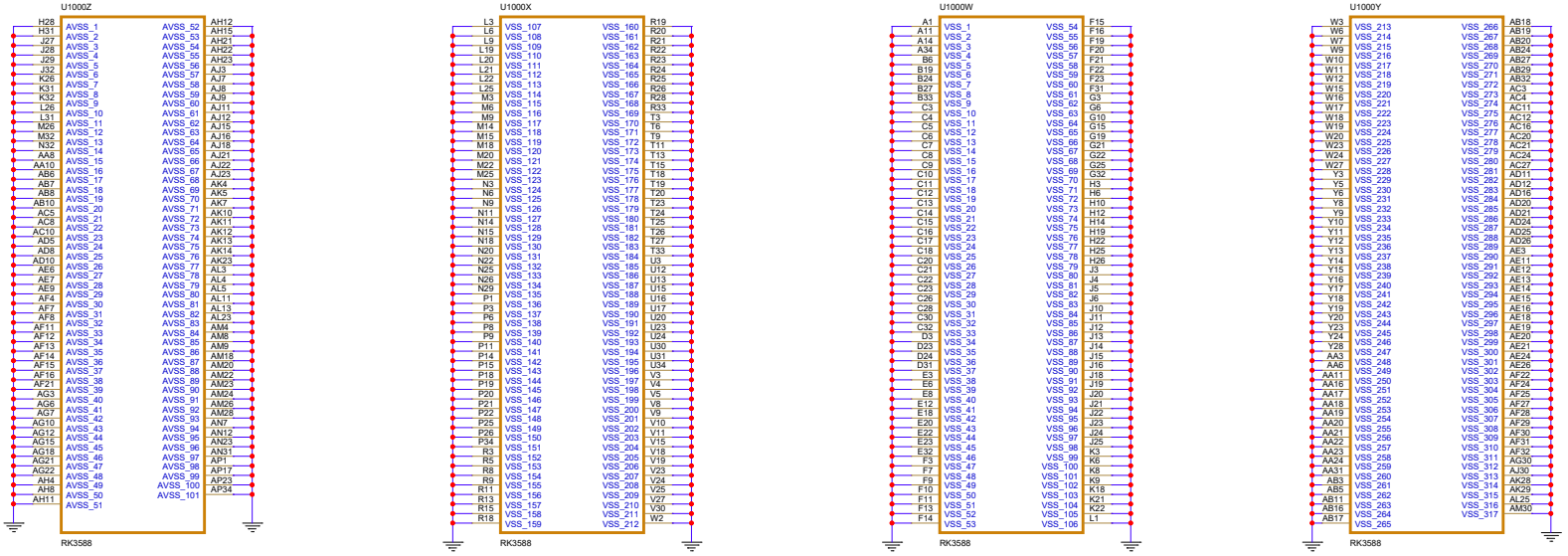
RK3588_V(POWER)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



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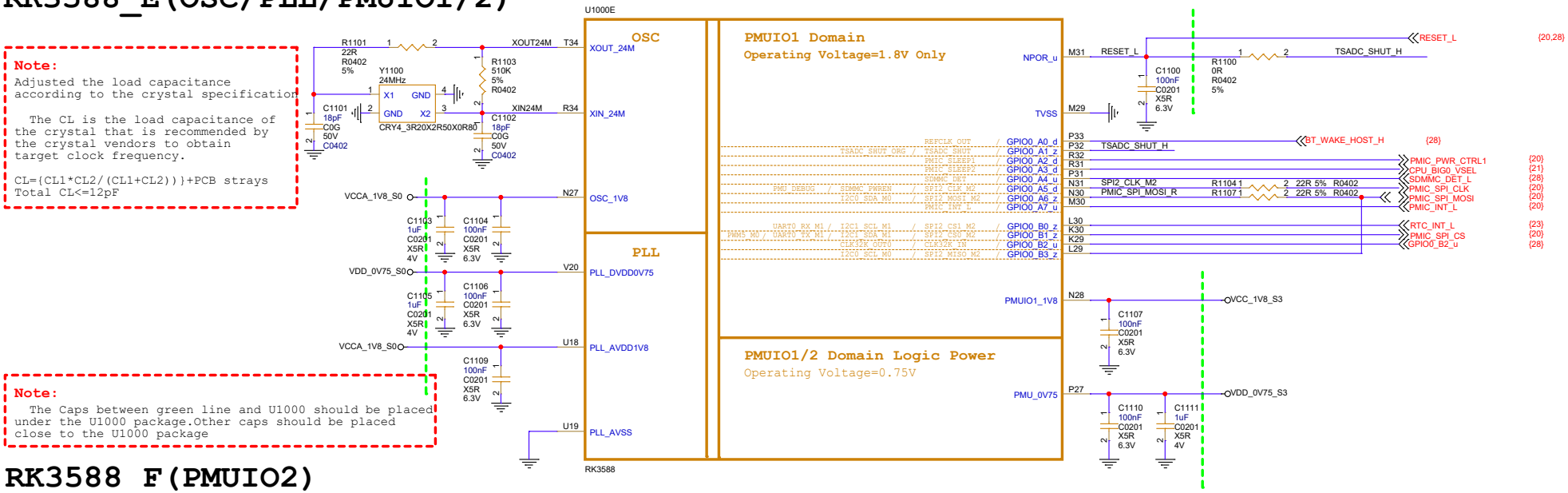
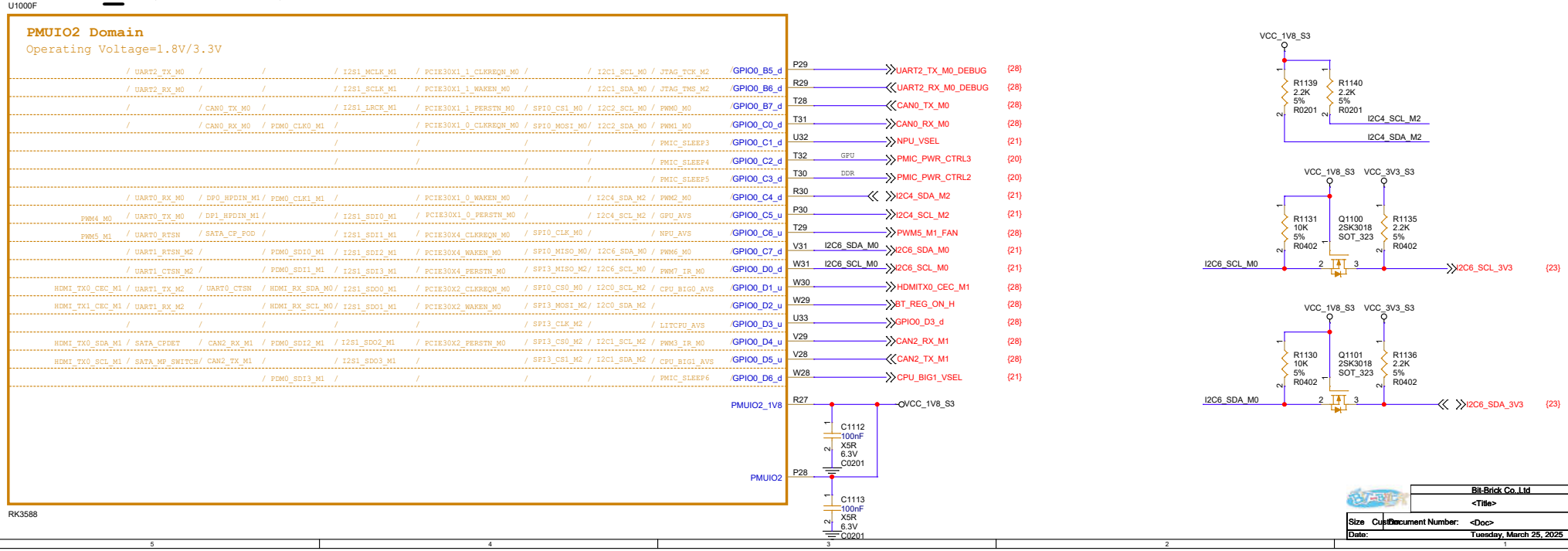
RK3588_E(OSC/PLL/PMUIO1/2)



RK3588_F(PMUIO2)



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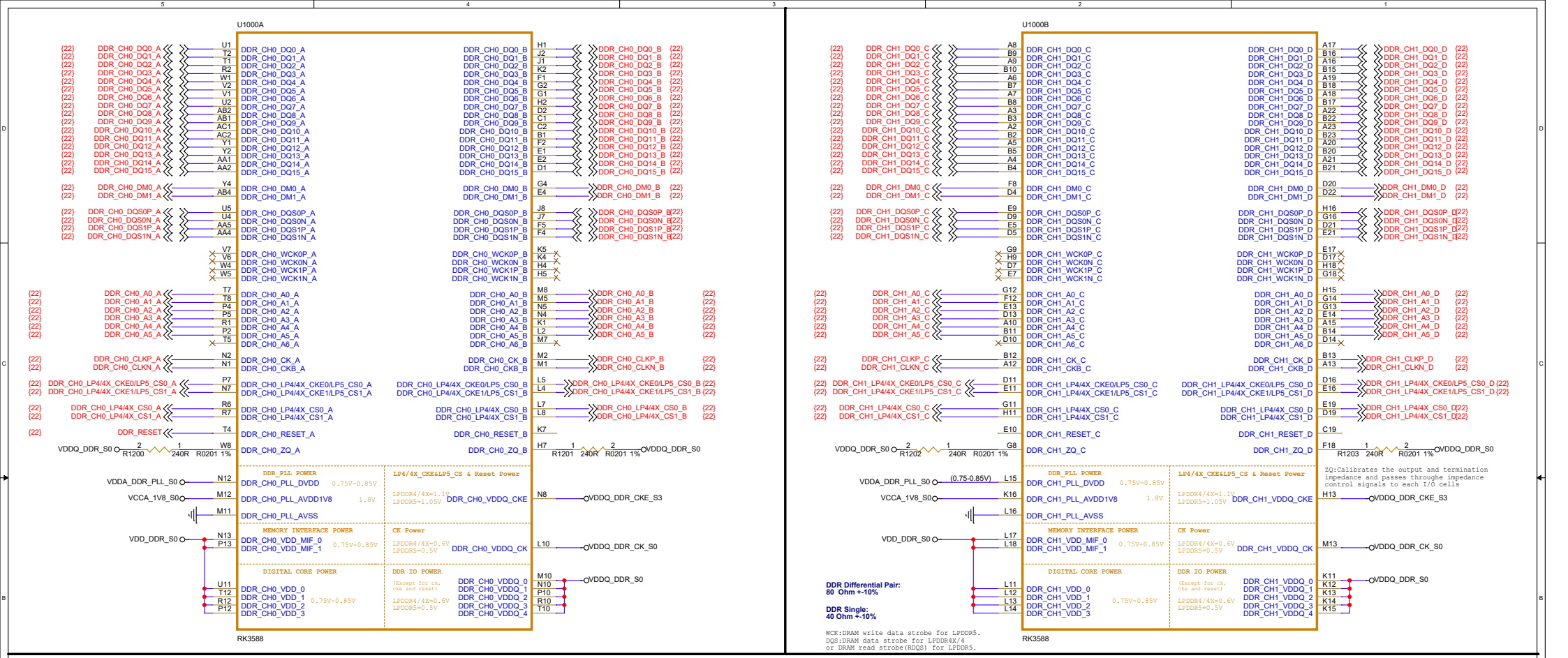

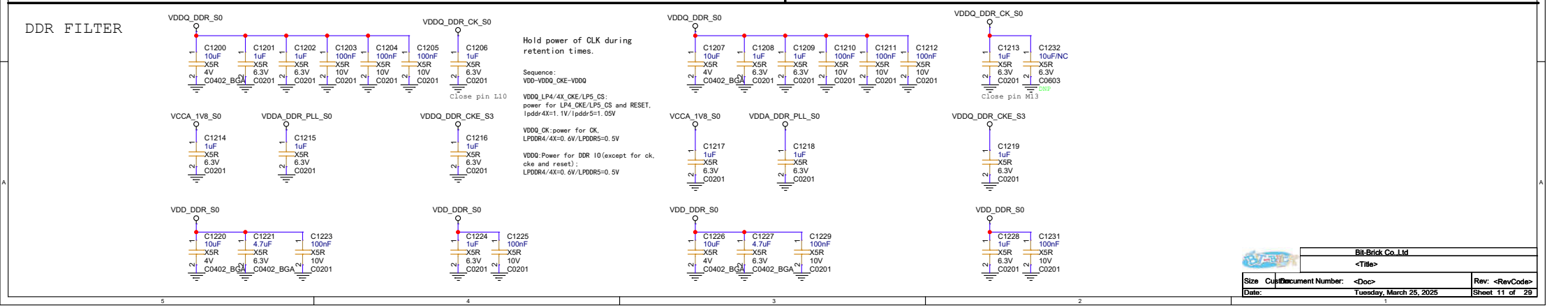

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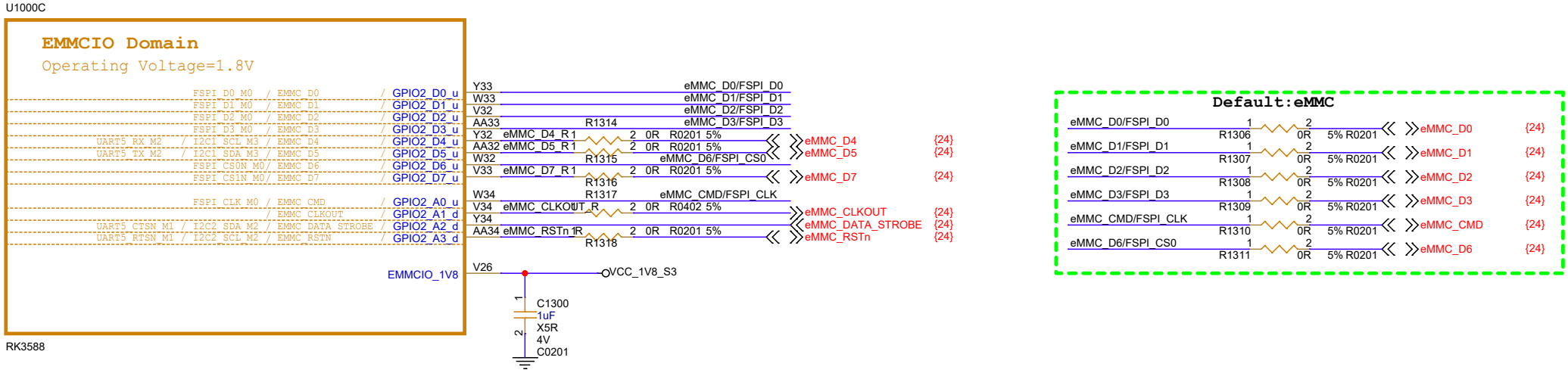
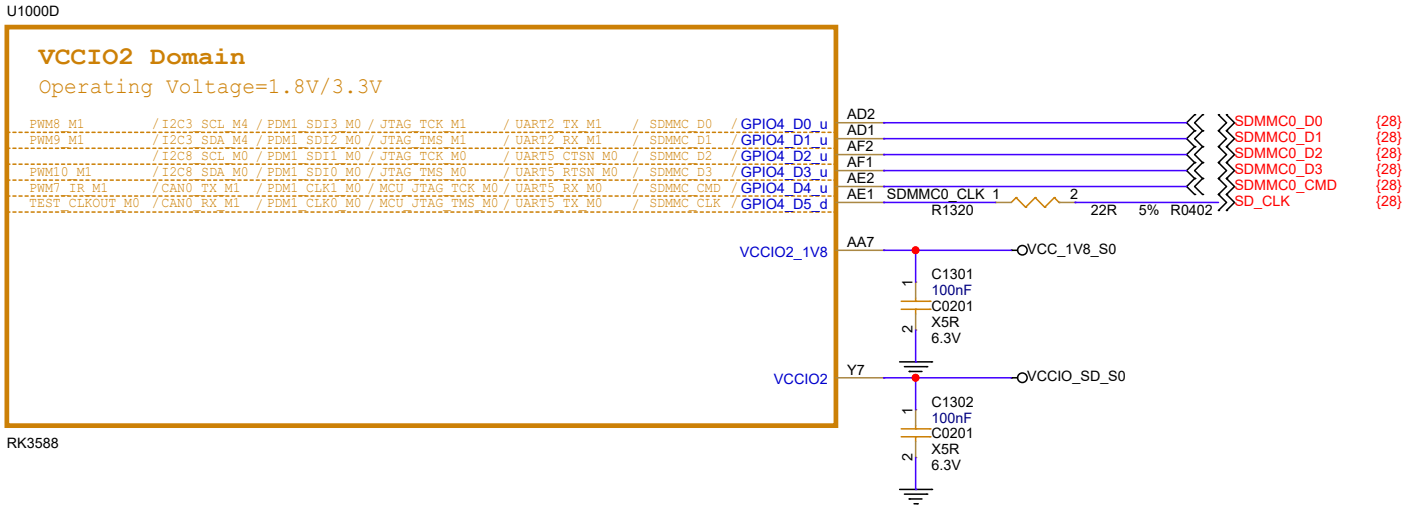
RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)



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RK3588_M(TYPEC/DP)

U1000M

Note:
If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1----Controller0
DP:RBR/HBR/HBR2/HBR3

TYPEC0_SBU1/DP0_AUXP
TYPEC0_SBU2/DP0_AUXN
TYPEC0_SSRX1P/DP0_TX0P
TYPEC0_SSRX1N/DP0_TX0N
TYPEC0_SSTX1P/DP0_TX1P
TYPEC0_SSTX1N/DP0_TX1N
TYPEC0_SSRX2P/DP0_TX2P
TYPEC0_SSRX2N/DP0_TX2N
TYPEC0_SSTX2P/DP0_TX3P
TYPEC0_SSTX2N/DP0_TX3N

AL15 TYPEC0_SBU1 {28}
AM15 TYPEC0_SBU2 {28}
AN13 TYPEC0_SSRX1P {28}
AP13 TYPEC0_SSRX1N {28}
AP14 TYPEC0_SSTX1P {28}
AN14 TYPEC0_SSTX1N {28}
AN15 TYPEC0_SSRX2P {28}
AP15 TYPEC0_SSRX2N {28}
AP16 TYPEC0_SSTX2P {28}
AN16 TYPEC0_SSTX2N {28}

TYPEC0_DP0_REXT — AH16 TYPEC0_REXT — R1402 8.2K R0201 1%

TYPEC0_DP0_VDD_0V85 / TYPEC0_DP0_VDDA_0V85 — AJ14 / AH14 — VDDA_0V85_S0
C1400 1uF X5R 6.3V C0201
C1401 100nF X5R 6.3V C0201

TYPEC0_DP0_VDDH_1V8 — AG14 — VCCA_1V8_S0
C1402 1uF X5R 6.3V C0201
C1403 100nF X5R 6.3V C0201

Do not delete!!!

TYPEC&DP MUX Differential Pair:
DATE:95 Ohm +-10%
For Typec

USB30 Differential Pair: **DATE:90 Ohm +-10%**
For USB30

DP Differential Pair: **DATE:100 Ohm +-10%**
For DP

USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1----Controller1
DP:RBR/HBR/HBR2/HBR3

TYPEC1_SBU1/DP1_AUXP
TYPEC1_SBU2/DP1_AUXN
TYPEC1_SSRX1P/DP1_TX0P
TYPEC1_SSRX1N/DP1_TX0N
TYPEC1_SSTX1P/DP1_TX1P
TYPEC1_SSTX1N/DP1_TX1N
TYPEC1_SSRX2P/DP1_TX2P
TYPEC1_SSRX2N/DP1_TX2N
TYPEC1_SSTX2P/DP1_TX3P
TYPEC1_SSTX2N/DP1_TX3N

AL10 DP1_AUXP
AM10 DP1_AUXN
AN8 DP1_TX0P/TYPEC1_SSRX1P
AP8 DP1_TX0N/TYPEC1_SSRX1N
AP9 DP1_TX1P/TYPEC1_SSTX1P
AN9 DP1_TX1N/TYPEC1_SSTX1N
AN10 DP1_TX2P
AP10 DP1_TX2N
AP11 DP1_TX3P
AN11 DP1_TX3N

Option

DP TX(4Lane)

DP1_AUXP / DP1_AUXN → DP1_AUXP {28} / DP1_AUXN {28}
DP1_TX0P/TYPEC1_SSRX1P / DP1_TX0N/TYPEC1_SSRX1N → DP1_TX0P {28} / DP1_TX0N {28}
DP1_TX1P/TYPEC1_SSTX1P / DP1_TX1N/TYPEC1_SSTX1N → DP1_TX1P {28} / DP1_TX1N {28}
DP1_TX2P → DP1_TX2P {28} / DP1_TX2N {28}
DP1_TX3P → DP1_TX3P {28} / DP1_TX3N {28}

TYPEC1_DP1_REXT — AG16 TYPEC1_REXT — R1410 8.2K R0201 1%

TYPEC1_DP1_VDD_0V85 / TYPEC1_DP1_VDDA_0V85 — AH13 / AJ13 — VDDA_0V85_S0
C1404 1uF X5R 6.3V C0201
C1405 100nF X5R 6.3V C0201

TYPEC1_DP1_VDDH_1V8 — AG13 — VCCA_1V8_S0
C1406 1uF X5R 6.3V C0201
C1407 100nF X5R 6.3V C0201

Note:
If need full function of Typec1
(With DP funtion)
please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

RK3588

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)

U1000L

USB2.0 of TYPEC0 (OTG/HOST/DEVICE)

HS/FS/LS

Download Port

TYPEC0_USB20_OTG_DP / TYPEC0_USB20_OTG_DM
TYPEC0_USB20_OTG_ID
TYPEC0_USB20_VBUSDET
TYPEC0_USB20_OTG0_REXT

AL12 AM12 → TYPEC0_OTG_DP {28} / TYPEC0_OTG_DM {28}
AL14 =1.8V → TYPEC0_USB20_OTG_ID {28}
AM14 <=3.3V → TYPEC0_USB20_VBUSDET {28}
AP12 OTG0_REXT — R1405 200R R0201 1%

USB20 Differential Pair:
DATE:90 Ohm +-10%

USB2.0 of TYPEC1 (OTG/HOST/DEVICE)

HS/FS/LS

TYPEC1_USB20_OTG_DP / TYPEC1_USB20_OTG_DM
TYPEC1_USB20_OTG_ID
TYPEC1_USB20_VBUSDET
TYPEC1_USB20_OTG1_REXT

AK9 AL9 → TYPEC1_OTG_DP {28} / TYPEC1_OTG_DM {28}
AK8 → TYPEC1_USB20_OTG_ID {28}
AL8 → TYPEC1_USB20_VBUSDET {28}
AP7 OTG1_REXT — R1406 200R R0201 1%

USB2.0 HOST0

HS/FS/LS

USB20_HOST0_DP / USB20_HOST0_DM
USB20_HOST0_REXT

AK6 AL6 → USB20_HOST0_DP {28} / USB20_HOST0_DM {28}
AG9 HOST0_REXT — R1400 200R R0201 1%

USB2.0 HOST1

HS/FS/LS

USB20_HOST1_DP / USB20_HOST1_DM
USB20_HOST1_REXT

AL7 AM7 → USB20_HOST1_DP {28} / USB20_HOST1_DM {28}
AH9 HOST1_REXT — R1401 200R R0201 1%

USB2.0 POWER

USB20_DVDD_0V75 — AH10 — VDDA_0V75_S0
C1408 100nF X5R 6.3V C0201

USB20_AVDD_1V8 — AG11 — VCCA_1V8_S0
C1409 100nF X5R 6.3V C0201

USB20_AVDD_3V3 — AJ10 — VCCA_3V3_S0
C1410 100nF X5R 6.3V C0201

RK3588

Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

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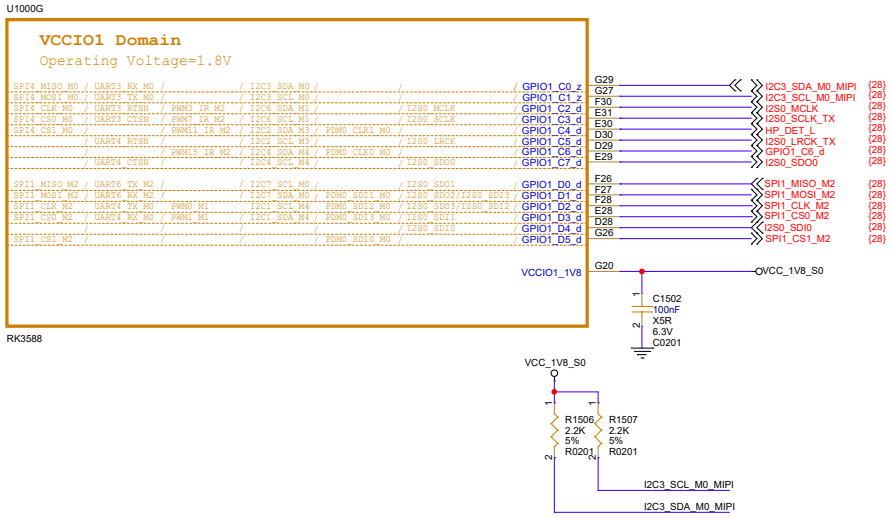
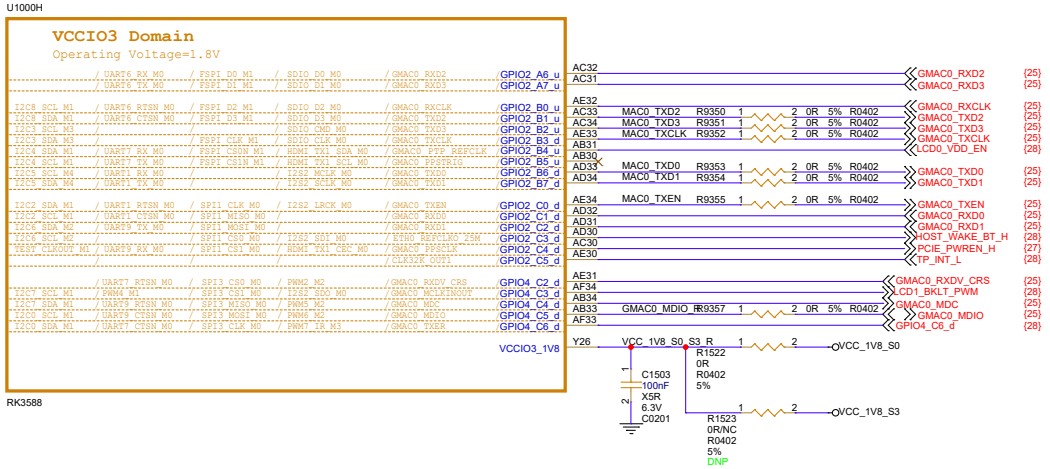
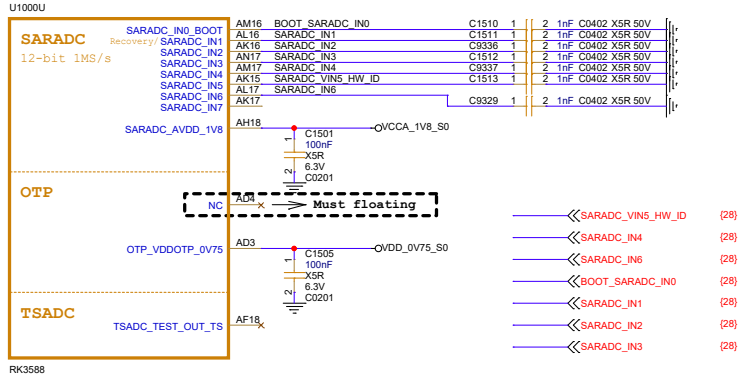
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

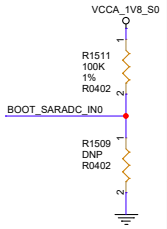


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

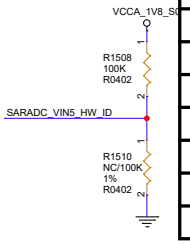


TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	51K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

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RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26 — MIPI_DPHY0_TX_CLKP {28}
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26 — MIPI_DPHY0_TX_CLKN {28}
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24 — MIPI_DPHY0_TX_D0P {28}
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24 — MIPI_DPHY0_TX_D0N {28}
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25 — MIPI_DPHY0_TX_D1P {28}
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25 — MIPI_DPHY0_TX_D1N {28}
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27 — MIPI_DPHY0_TX_D2P {28}
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27 — MIPI_DPHY0_TX_D2N {28}
MIPI_DPHY0_TX_D3P/NO_USE — AN28 — MIPI_DPHY0_TX_D3P {28}
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28 — MIPI_DPHY0_TX_D3N {28}

MIPI_DPHY Differential Pair: 100 Ohm +-10%
MIPI_CPHY Single: 50 Ohm +-10%

MIPI D/C-PHY CSI_RX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP31
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP32
MIPI_DPHY0_RX_D3P/NO_USE — AN34
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP33

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C1600 1uF — C0201 X5R 4V
MIPI_D/C_PHY0_VDD — AG20 — VDD_0V75_S0
C1602 100nF X5R 6.3V C0201
C1601 1uF X5R 6.3V C0201 D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V
MIPI_D/C_PHY0_VDD_1V2 — AH20 — VDDA_1V2_S0
C1603 1uF X5R 6.3V C0201
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — VCC_1V8_S0
C1605 1uF X5R 6.3V C0201

RK3588

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20 — MIPI_DPHY1_TX_CLKP {28}
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20 — MIPI_DPHY1_TX_CLKN {28}
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18 — MIPI_DPHY1_TX_D0P {28}
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18 — MIPI_DPHY1_TX_D0N {28}
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19 — MIPI_DPHY1_TX_D1P {28}
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19 — MIPI_DPHY1_TX_D1N {28}
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21 — MIPI_DPHY1_TX_D2P {28}
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A — AP21 — MIPI_DPHY1_TX_D2N {28}
MIPI_DPHY1_TX_D3P/NO_USE — AN22 — MIPI_DPHY1_TX_D3P {28}
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C — AP22 — MIPI_DPHY1_TX_D3N {28}

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21
MIPI_DPHY1_RX_D3P/NO_USE — AK22
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C1608 1uF — C0201 X5R 4V
MIPI_D/C_PHY1_VDD — AG19 — VDD_0V75_S0
C1609 1uF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V2 — AH19 — VDDA_1V2_S0
C1611 100nF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — VCC_1V8_S0
C1613 1uF X5R 6.3V C0201

RK3588

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N — AJ33/AJ34 — MIPI_CSI0_RX_CLK0P/MIPI_CSI0_RX_CLK0N {28}
MIPI_CSI0_D0P/MIPI_CSI0_D0N — AG33/AG34 — MIPI_CSI0_RX_D0P/MIPI_CSI0_RX_D0N {28}
MIPI_CSI0_D1P/MIPI_CSI0_D1N — AH33/AH34 — MIPI_CSI0_RX_D1P/MIPI_CSI0_RX_D1N {28}
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N — AM33/AM34
MIPI_CSI0_D2P/MIPI_CSI0_D2N — AK33/AK34 — MIPI_CSI0_RX_D2P/MIPI_CSI0_RX_D2N {28}
MIPI_CSI0_D3P/MIPI_CSI0_D3N — AL33/AL34 — MIPI_CSI0_RX_D3P/MIPI_CSI0_RX_D3N {28}

MIPI CSI Differential Pair: 100 Ohm +-10%

MIPI_CSI0_AVCC0V75 — AB25 — VDD_0V75_S0
C1616 100nF X5R 6.3V C0201
C1615 1uF X5R 6.3V C0201
MIPI_CSI0_AVCC1V8 — AB26 — VCC_1V8_S0
C1617 1uF X5R 6.3V C0201

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N — AJ31/AJ32 — MIPI_CSI1_RX_CLK0P/MIPI_CSI1_RX_CLK0N {28}
MIPI_CSI1_D0P/MIPI_CSI1_D0N — AG31/AG32 — MIPI_CSI1_RX_D0P/MIPI_CSI1_RX_D0N {28}
MIPI_CSI1_D1P/MIPI_CSI1_D1N — AH31/AH32 — MIPI_CSI1_RX_D1P/MIPI_CSI1_RX_D1N {28}
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N — AM31/AM32
MIPI_CSI1_D2P/MIPI_CSI1_D2N — AK31/AK32
MIPI_CSI1_D3P/MIPI_CSI1_D3N — AL31/AL32

MIPI_CSI1_AVCC0V75 — AA25 — VDD_0V75_S0
C1619 1uF X5R 6.3V C0201
MIPI_CSI1_AVCC1V8 — AA26 — VCC_1V8_S0
C1621 100nF X5R 6.3V C0201

RK3588

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

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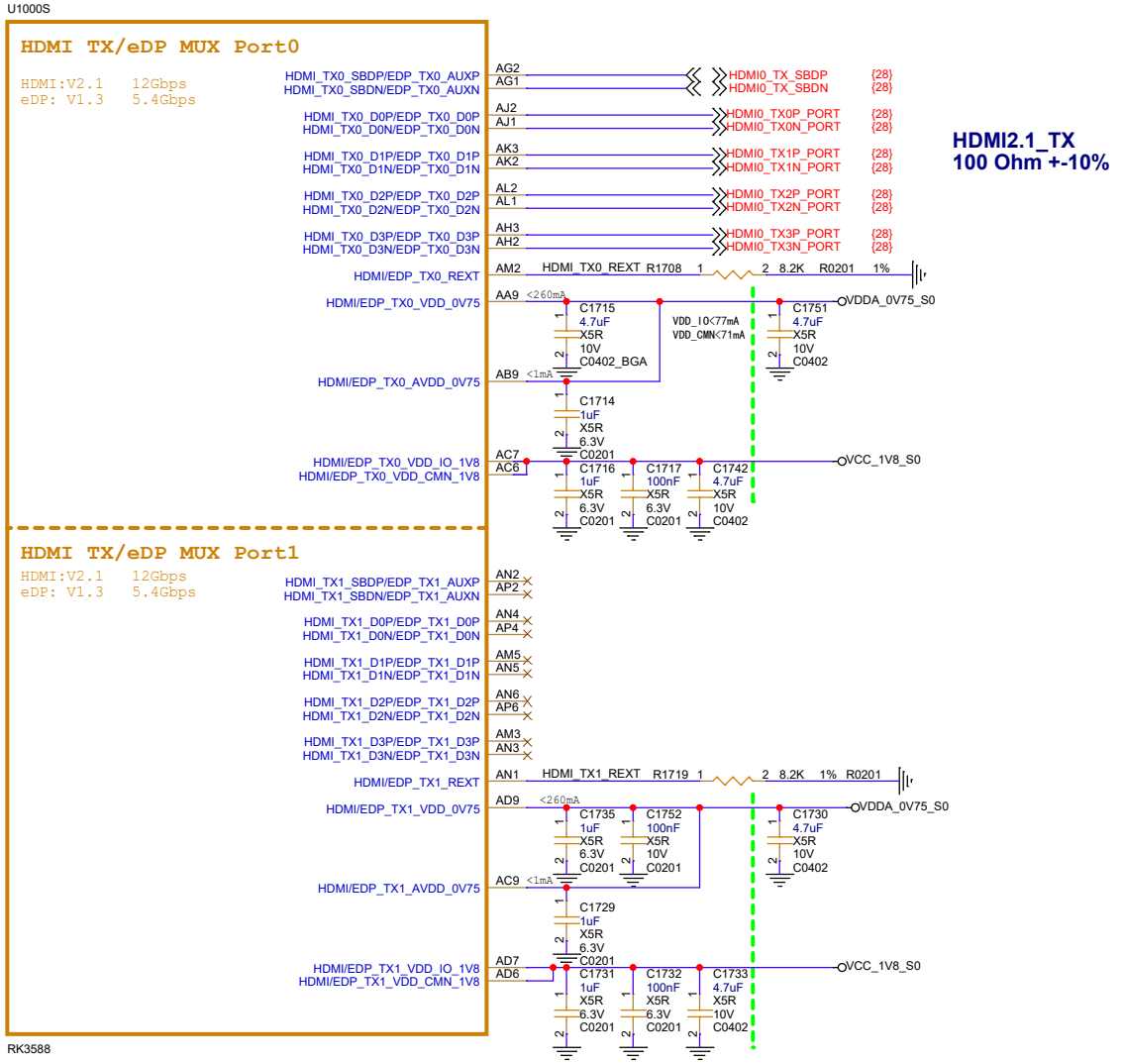
RK3588_S(HDMI2.1 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

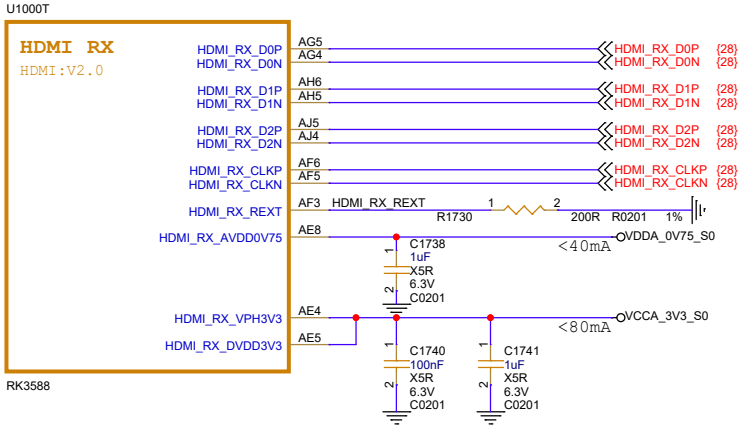


HDMI2.1_TX
100 Ohm +-10%

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



HDMI20_RX
100 Ohm +-10%

Note:
If not used:
Signal:leave floating
Power: Floating

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RK3588_N(PCIE20)

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2 1Lane(RC)--4(1L2)

SATA30 HOST Controller0

MUX

input or output

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN — L32 / L33 — PCIE20_0_REFCLKP {28} / PCIE20_0_REFCLKN {28}

PCIE20_0_TXP/SATA30_0_TXP / PCIE20_0_TXN/SATA30_0_TXN — M34 / M33 — PCIE20_0_TXP/SATA30_0_TXP {28} / PCIE20_0_TXN/SATA30_0_TXN {28}

PCIE20_0_RXP/SATA30_0_RXP / PCIE20_0_RXN/SATA30_0_RXN — N33 / N34 — PCIE20_0_RXP/SATA30_0_RXP{28} / PCIE20_0_RXN/SATA30_0_RXN{28}

PCIE20_SATA30_0_AVDD_0V85 — M28 — VDDA_0V85_S0
- C1810 10uF X5R 4V C0402

PCIE20_SATA30_0_AVDD_1V8 — M27 — VCCA_1V8_S0
- C1808 1uF X5R 4V C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0 1Lane(RC)--2(1L0)

SATA30 HOST Controller1

MUX

input or output

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN — H32 / H33

PCIE20_1_TXP/SATA30_1_TXP / PCIE20_1_TXN/SATA30_1_TXN — K33 / K34 — SATA30_1_TXP {28} / SATA30_1_TXN {28}

PCIE20_1_RXP/SATA30_1_RXP / PCIE20_1_RXN/SATA30_1_RXN — J33 / J34 — SATA30_1_RXP {28} / SATA30_1_RXN {28}

PCIE20_SATA30_1_AVDD_0V85 — L28 — VDDA_0V85_S0
- C1818 100nF X5R 6.3V C0201

PCIE20_SATA30_1_AVDD_1V8 — L27 — VCCA_1V8_S0
- C1816 100nF X5R 6.3V C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1 1Lane(RC)--3(1L1)

SATA30 HOST Controller2

USB30 HOST Controller2

MUX

input or output

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN — G31 / G30

PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP / PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN — H30 / H29 — USB30_2_SSTXP {28} / USB30_2_SSTXN {28}

PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP / PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN — J31 / J30 — USB30_2_SSRXP {28} / USB30_2_SSRXN {28}

PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 — VDDA_0V85_S0
- C1806 1uF X5R 4V C0201

PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 — VCCA_1V8_S0
- C1804 1uF X5R 4V C0201

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
If not used:
Signal:leave floating
Power: Floating

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4 4Lane(DM)--0(4L)

PCIe30x1_0 1Lane(RC)--2(1L0)

PCIE20/SATA30 MUX1

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIe30x2 2Lane(RC)--1(2L)

PCIe30x1_1 1Lane(RC)--3(1L1)

PCIE20/SATA30/USB30 MUX2

PCIE30 PORT0

input PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN — E33 / E34 — PCIE30_PORT0_REFCLKP_IN {27} / PCIE30_PORT0_REFCLKN_IN {27}

Lane0
- PCIE30_PORT0_TX0P / PCIE30_PORT0_TX0N — D32 / D33 — PCIE30_PORT0_TX0P {28} / PCIE30_PORT0_TX0N {28}
- PCIE30_PORT0_RX0P / PCIE30_PORT0_RX0N — G33 / G34 — PCIE30_PORT0_RX0P {28} / PCIE30_PORT0_RX0N {28}

Lane1
- PCIE30_PORT0_TX1P / PCIE30_PORT0_TX1N — C33 / C34 — PCIE30_PORT0_TX1P {28} / PCIE30_PORT0_TX1N {28}
- PCIE30_PORT0_RX1P / PCIE30_PORT0_RX1N — F32 / F33 — PCIE30_PORT0_RX1P {28} / PCIE30_PORT0_RX1N {28}

PCIE30_PORT0_RESREF — B34 — PCIE30_0_REF — R1801 1 2 200R 1% R0201

PCIE30_PORT0_AVDD0V75 — G24 — VDD_0V75_S0
- C1802 1uF X5R 6.3V C0201
- C1803 4.7uF X5R 10V C0402

PCIE30_PORT0_AVDD1V8 — G23 — VCCA_1V8_S0
- C1800 1uF X5R 6.3V C0201
- C1801 4.7uF X5R 10V C0402

PCIE30 PORT1

input PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN — A28 / B28 — PCIE30_PORT1_REFCLKP_IN {27} / PCIE30_PORT1_REFCLKN_IN {27}

Lane0
- PCIE30_PORT1_TX0P / PCIE30_PORT1_TX0N — B30 / A30
- PCIE30_PORT1_RX0P / PCIE30_PORT1_RX0N — B32 / A32

Lane1
- PCIE30_PORT1_TX1P / PCIE30_PORT1_TX1N — C29 / B29 — PCIE30_PORT1_TX1P {28} / PCIE30_PORT1_TX1N {28}
- PCIE30_PORT1_RX1P / PCIE30_PORT1_RX1N — C31 / B31 — PCIE30_PORT1_RX1P {28} / PCIE30_PORT1_RX1N {28}

PCIE30_PORT1_RESREF — A33 — PCIE30_1_REF — R1807 1 2 200R 1% R0201

PCIE30_PORT1_AVDD0V75 — H24 — VDD_0V75_S0
- C1814 1uF X5R 6.3V C0201
- C1815 4.7uF X5R C0402 10V

PCIE30_PORT1_AVDD1V8 — H23 — VCCA_1V8_S0
- C1812 100nF X5R 6.3V C0201
- C1813 4.7uF X5R 10V C0402

RK3588

CLK Differential Pair:
100 Ohm ±10%
DATA Differential Pair:
PCIE30: 85 Ohm ±10%

Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

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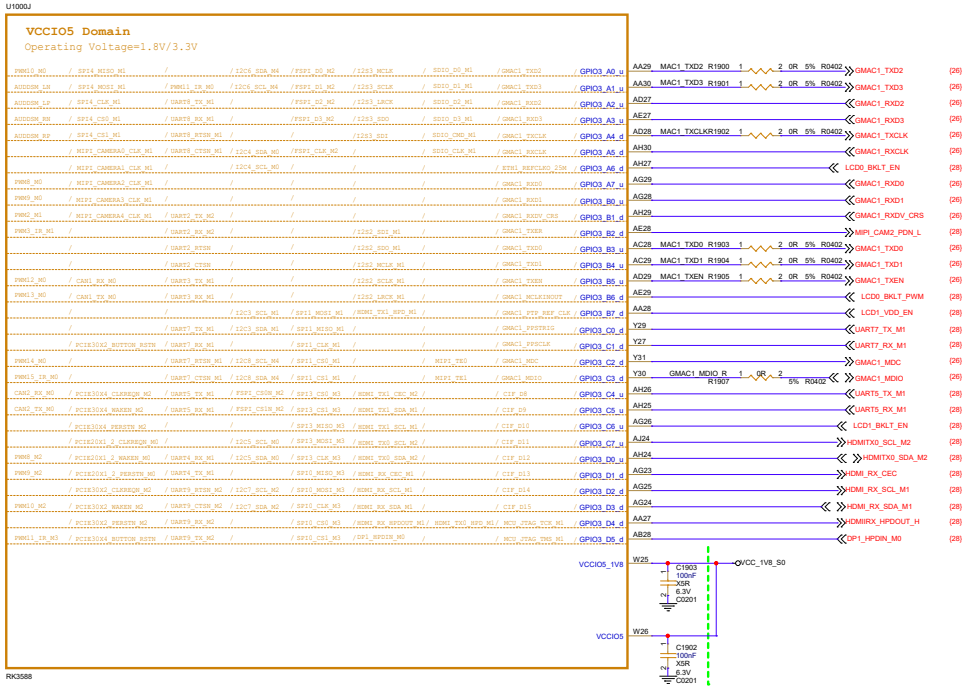
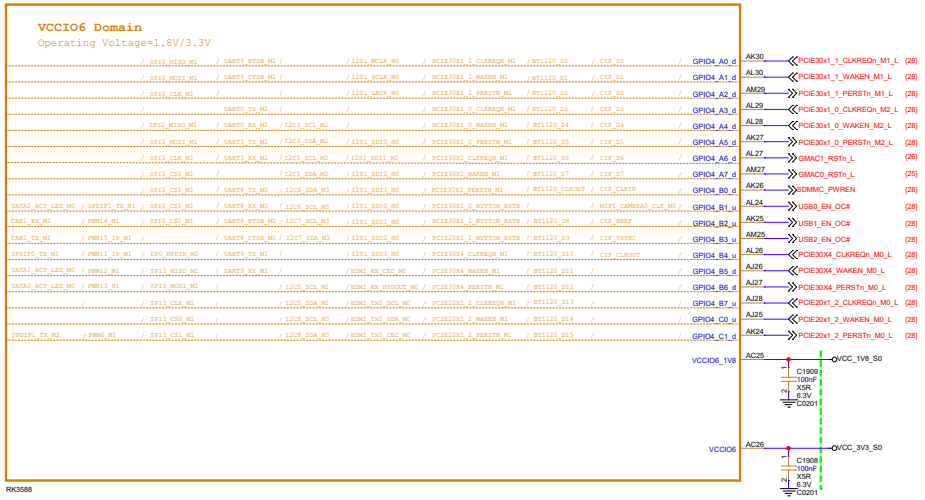
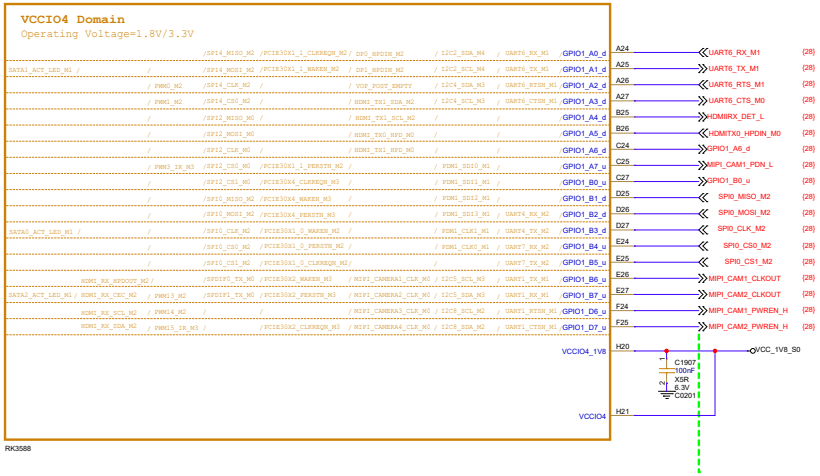
RK3588_J(VCCIO5 Domain)



RK3588_K(VCCIO6 Domain)



RK3588_I(VCCIO4 Domain)



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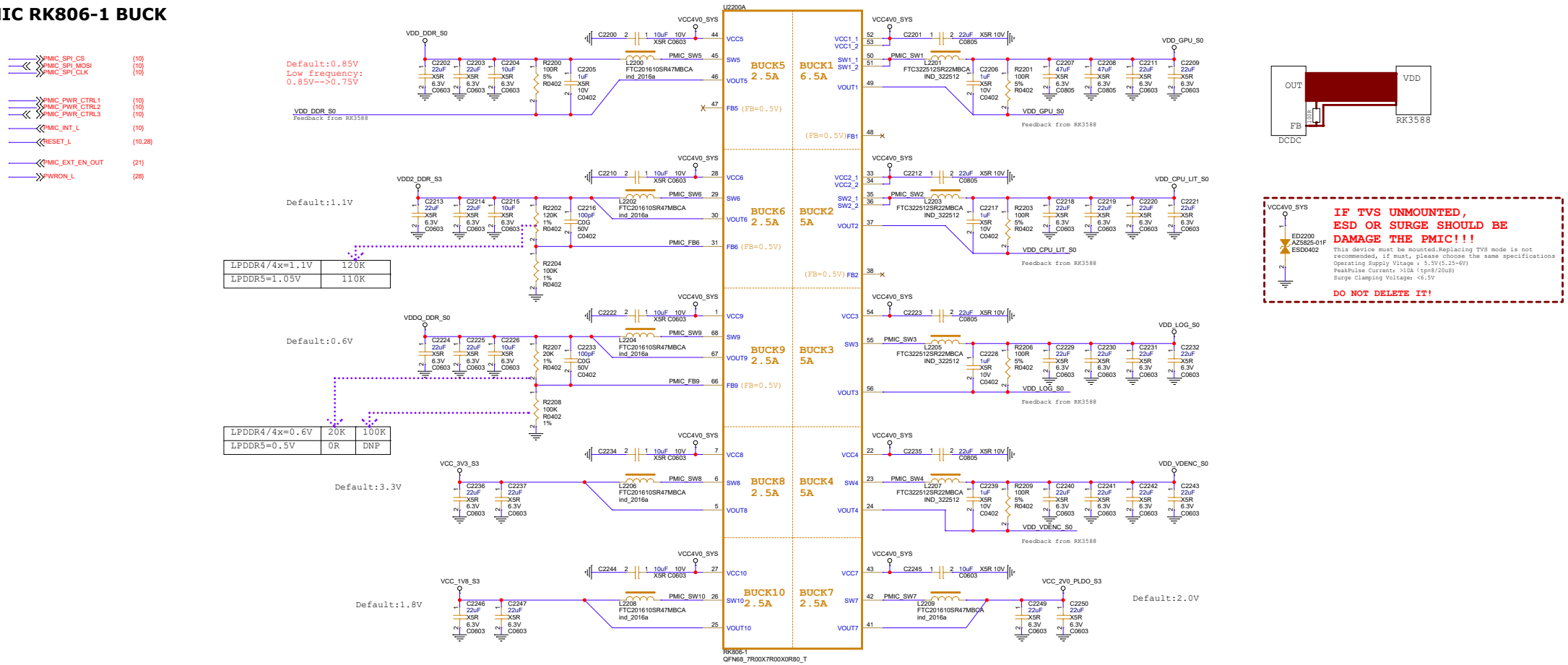
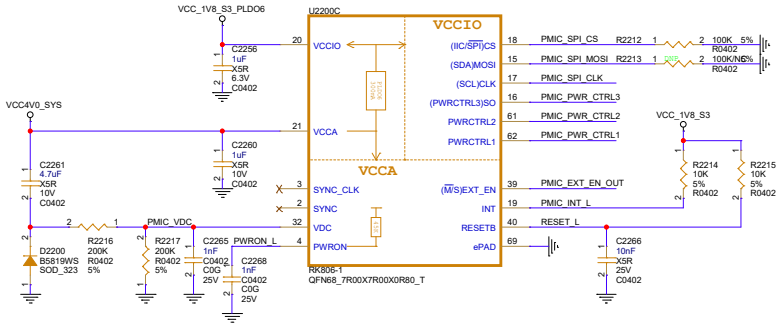
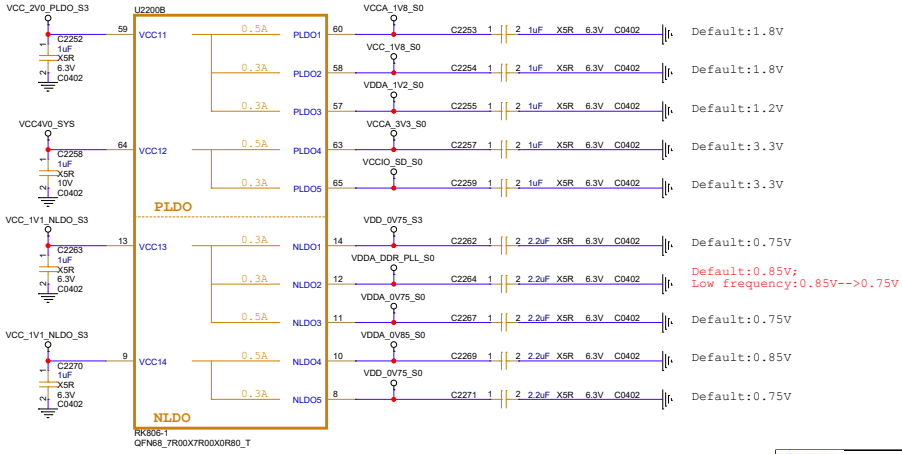
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



PMIC RK806-1 LDO



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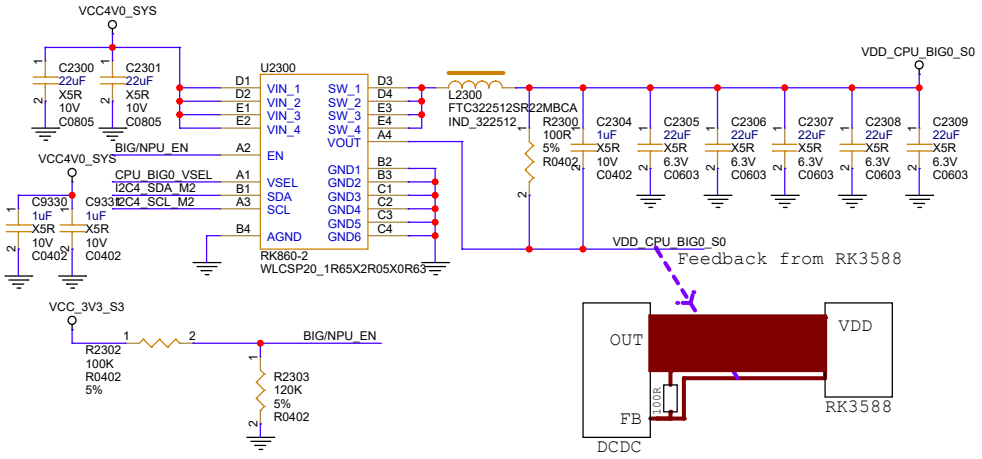
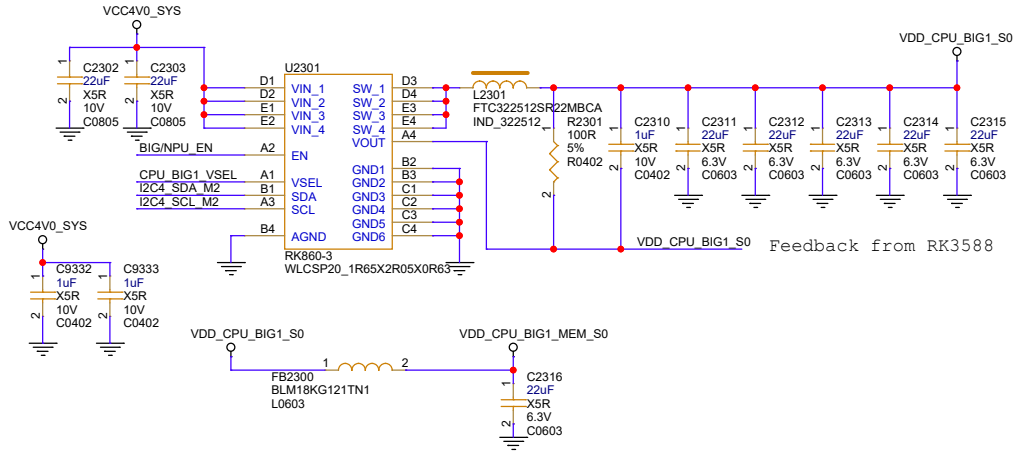
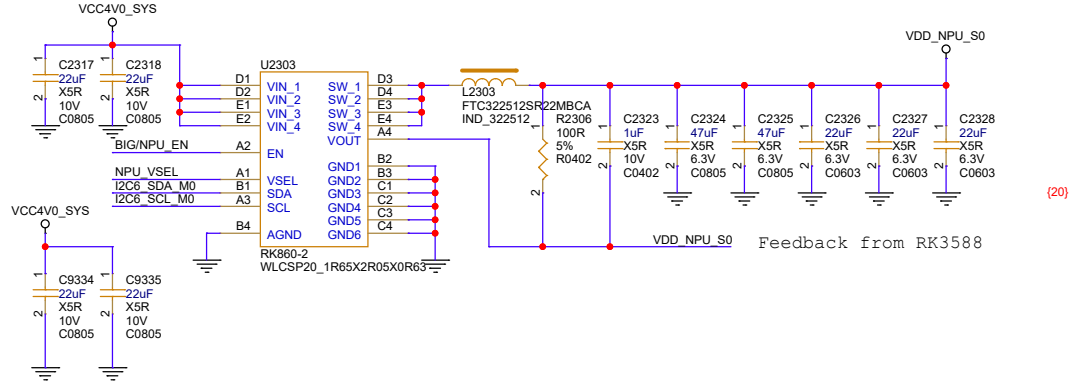
VDD_CPU_BIG0



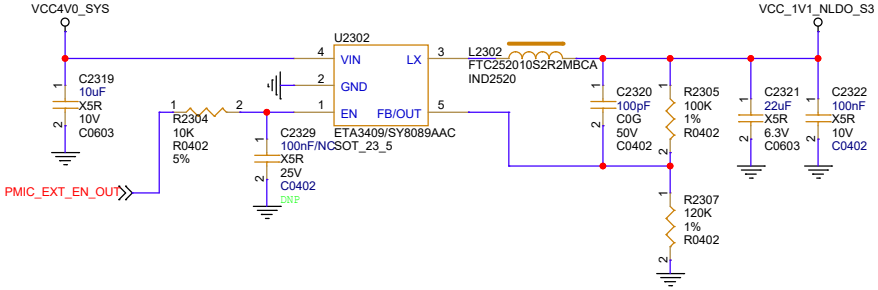
VDD_CPU_BIG1

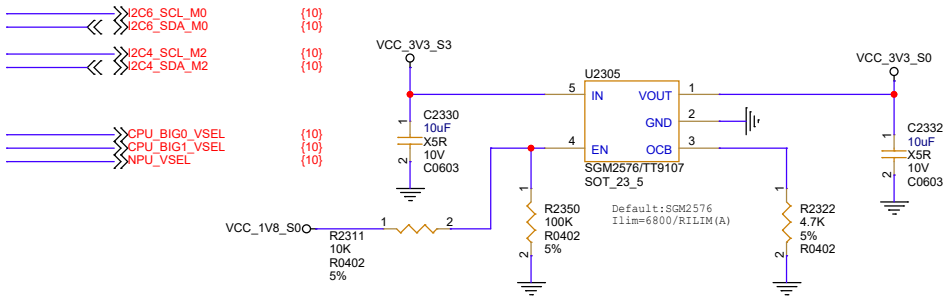


VDD_NPU



VCC_1V1_NLDO_S3





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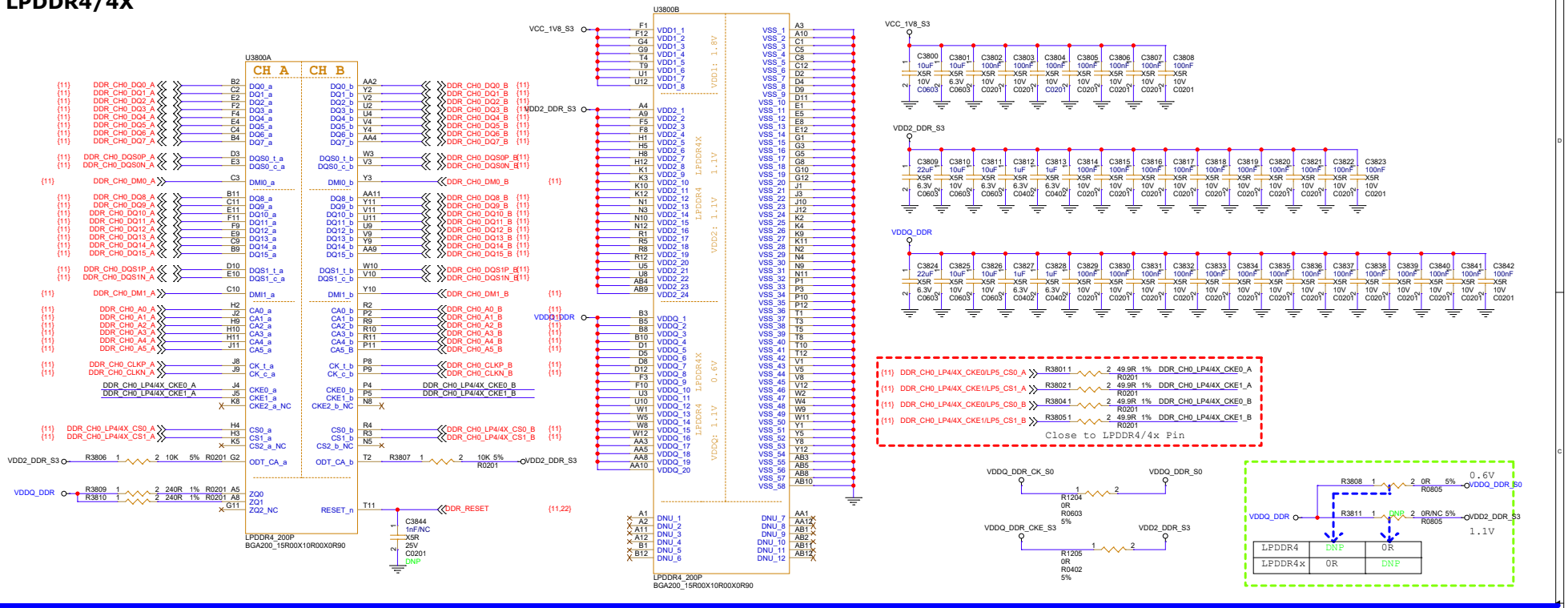
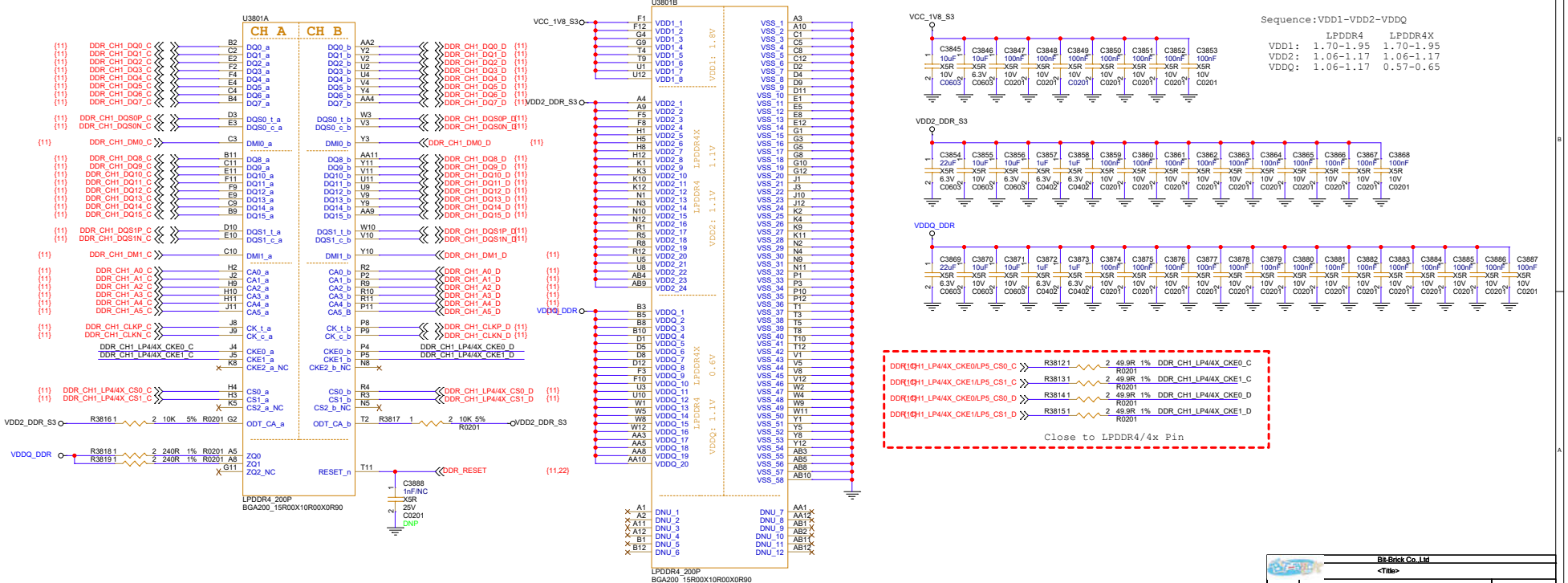
LPDDR4/4X





Sequence:VDD1-VDD2-VDDQ

	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

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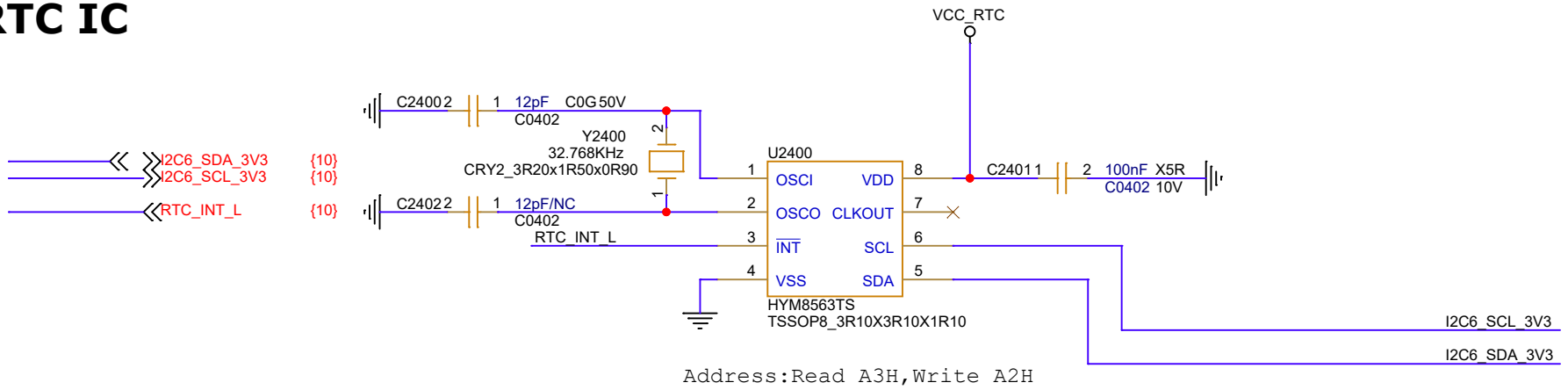
RTC IC



Address:Read A3H,Write A2H

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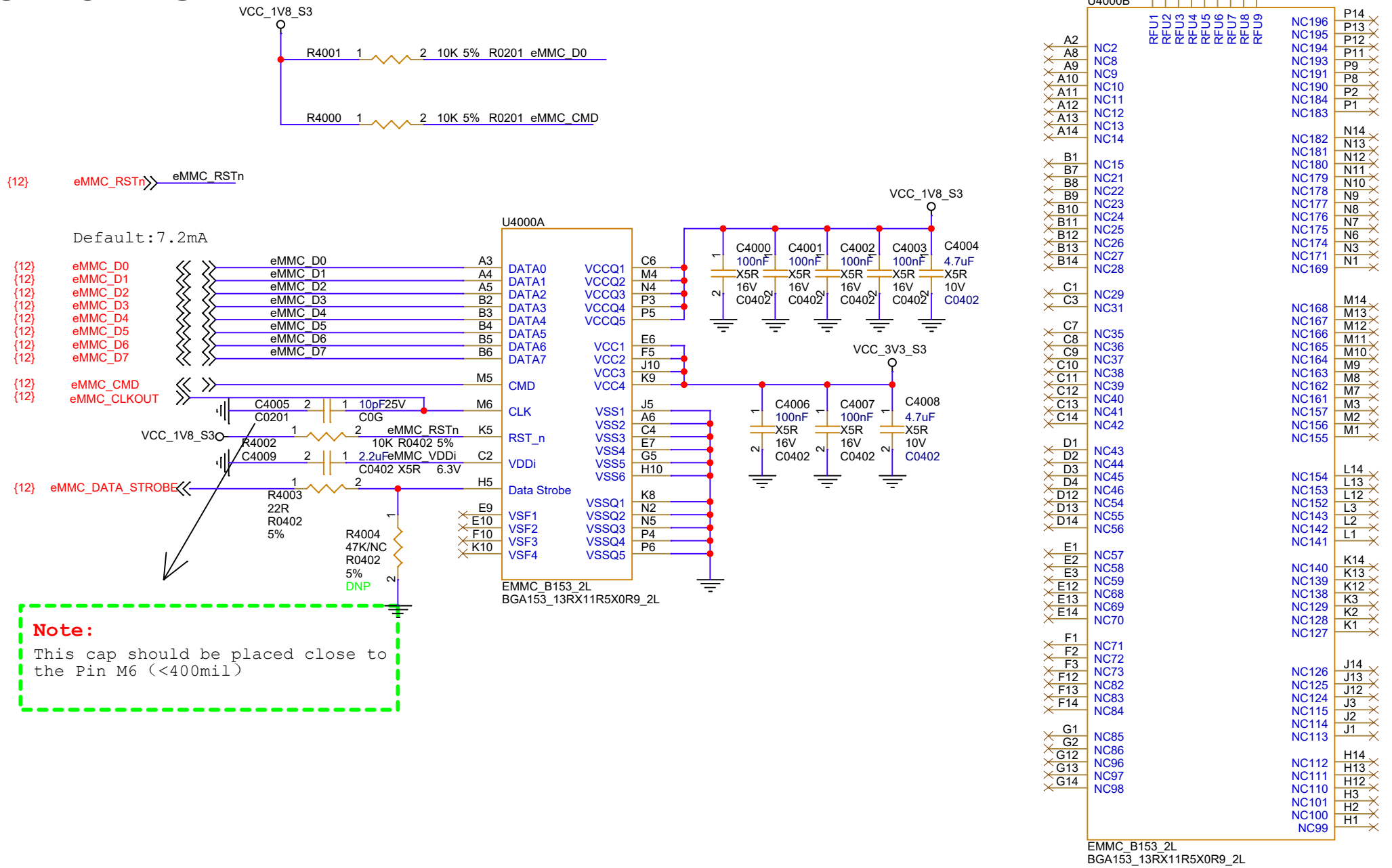
eMMC FLASH



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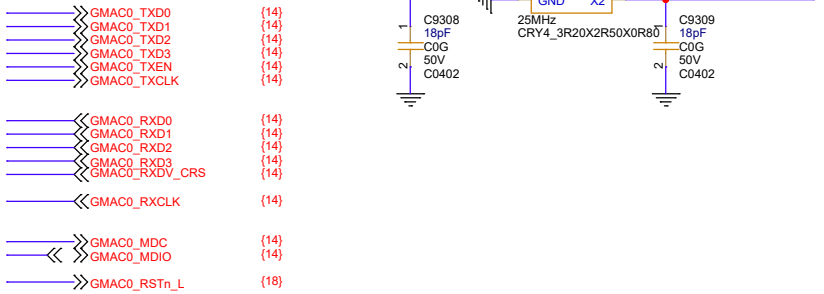
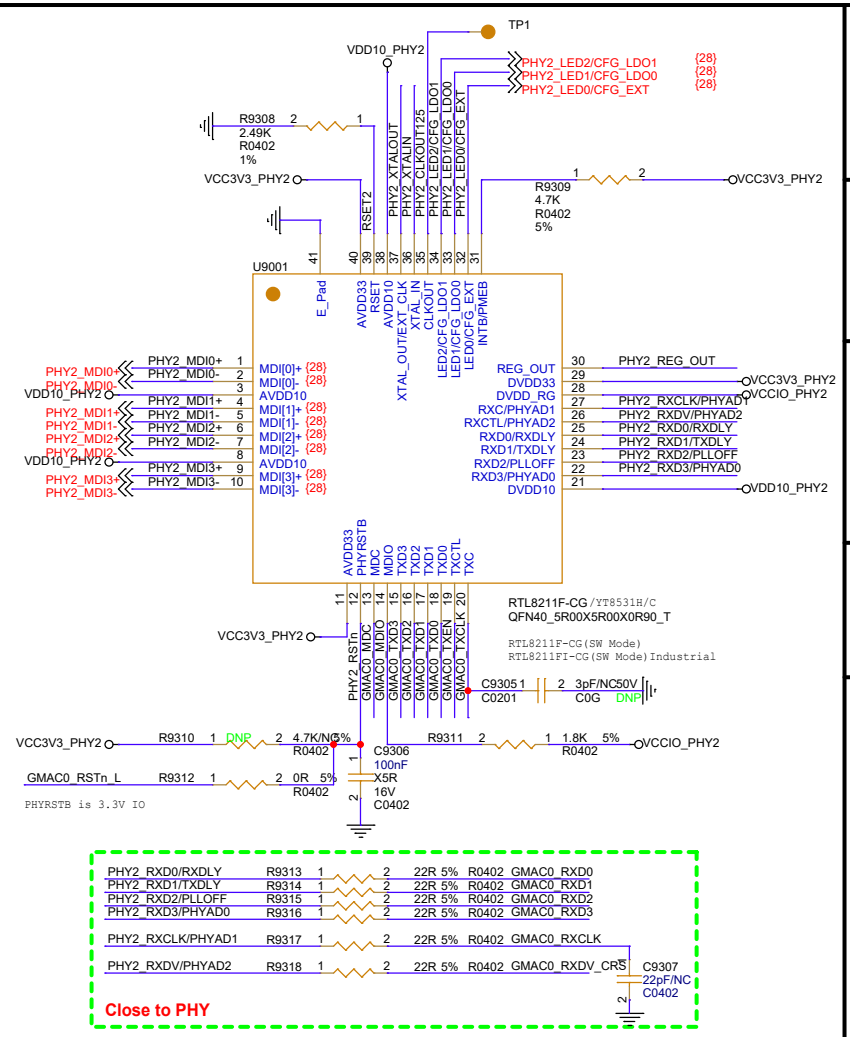
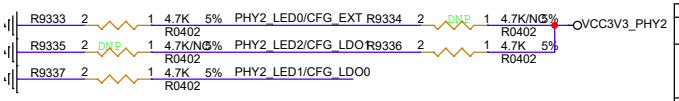
RGMII TO RJ45







VCC_PHY0_IO Voltage Config

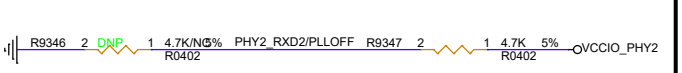
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	

PHY Address Config

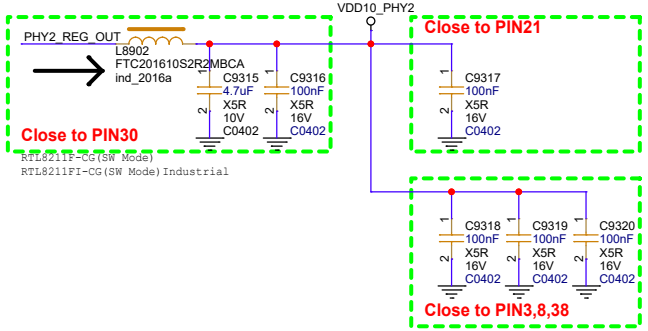
PHY Address	PHYAD[2:0]
1 (default)	3'b001

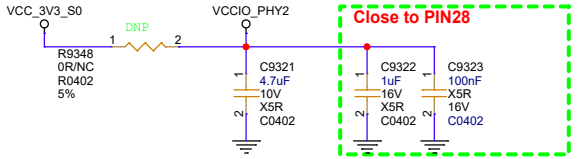
Pull-up for additional 2ns delay to RXC for data latching

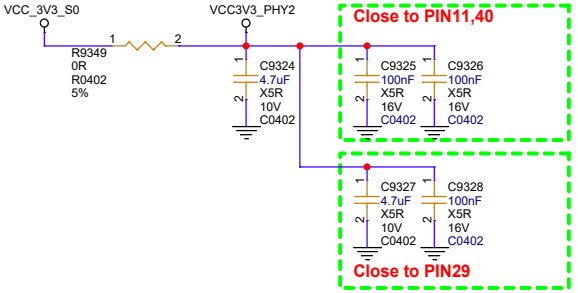
Pull-up for additional 2ns delay to TXC for data latching



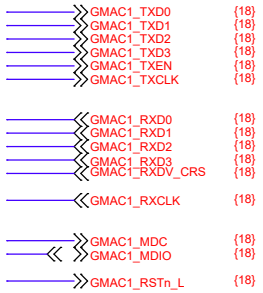
Pull-up to disable PLL @ ALDPS mode(Low power mode)

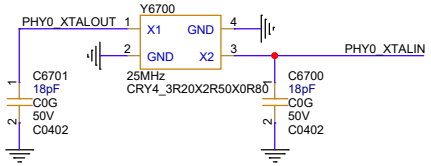


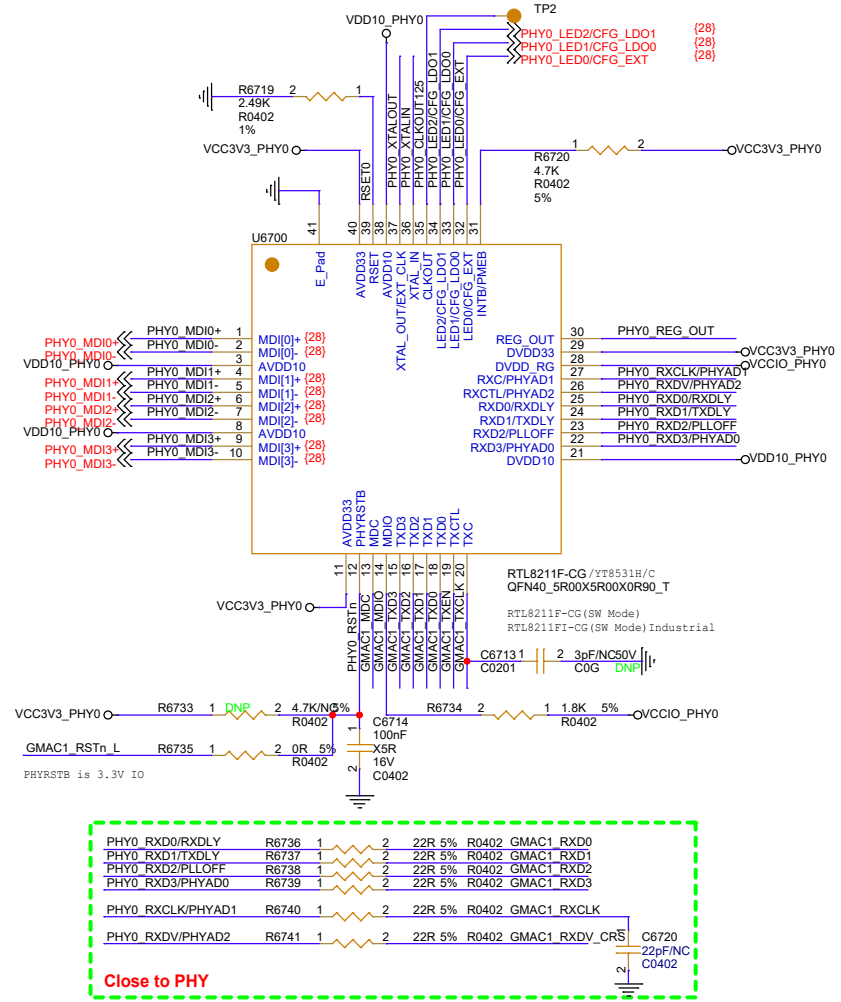


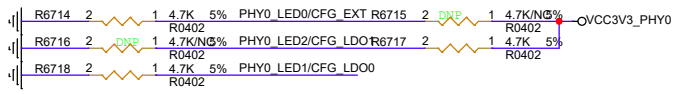


RGMII TO RJ45

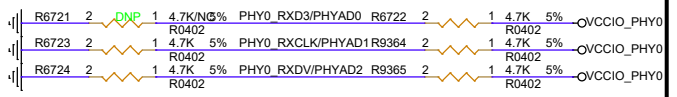


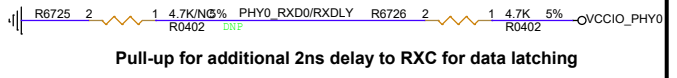


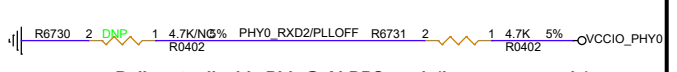


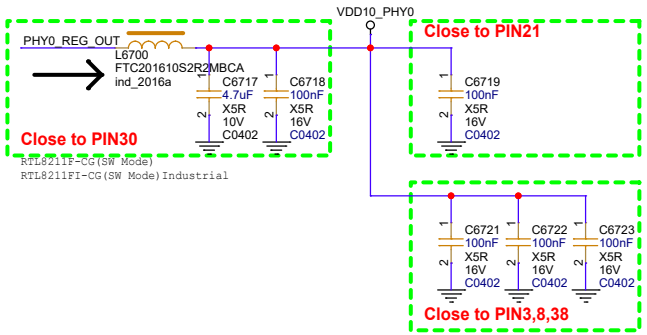


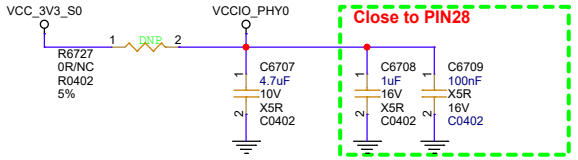
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V (default)	1'b0	2'b10	

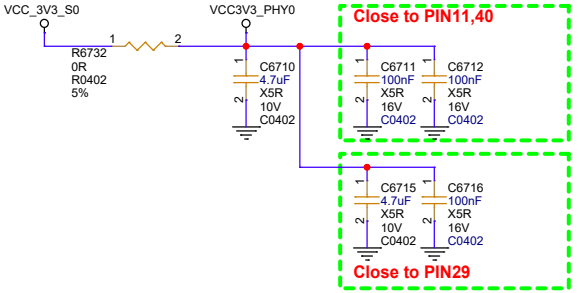












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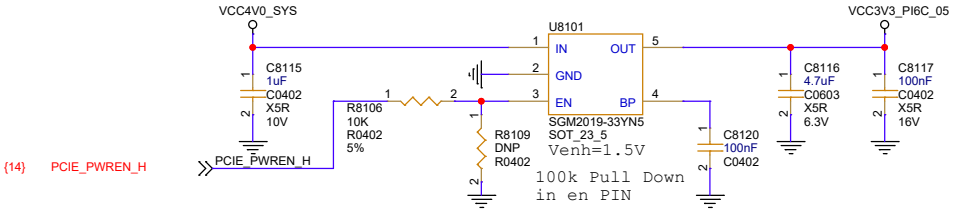
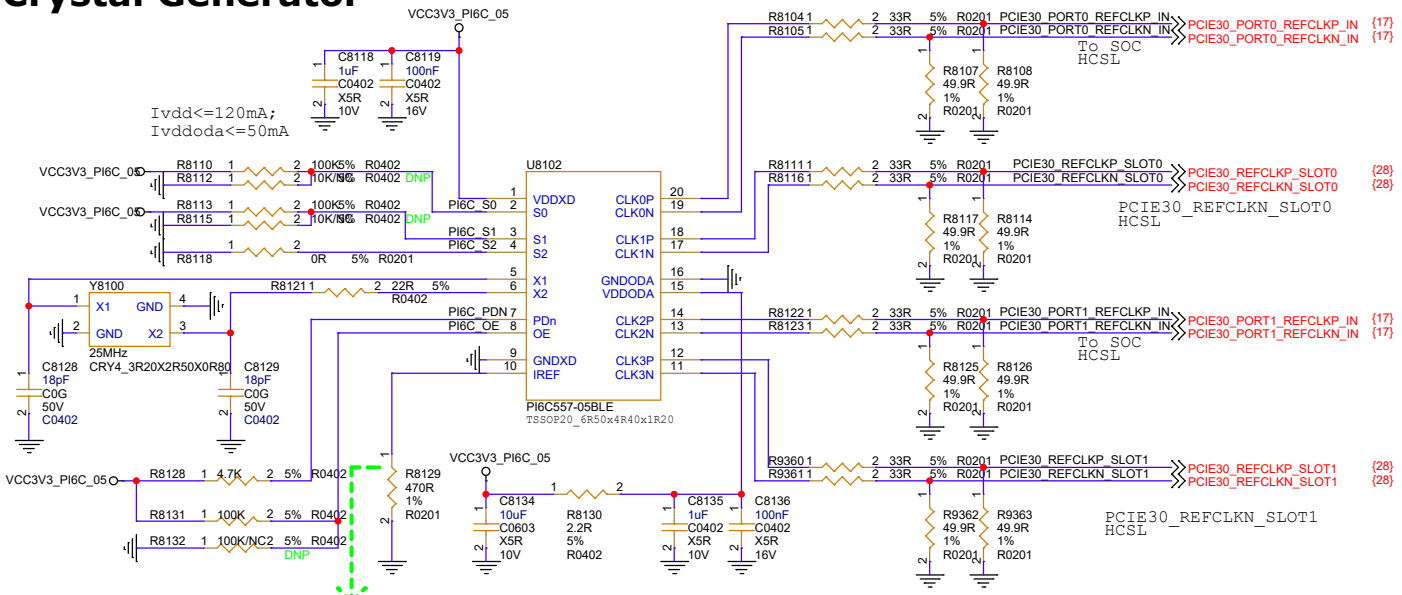
PCIe3.0 x 4 Slot



Crystal Generator



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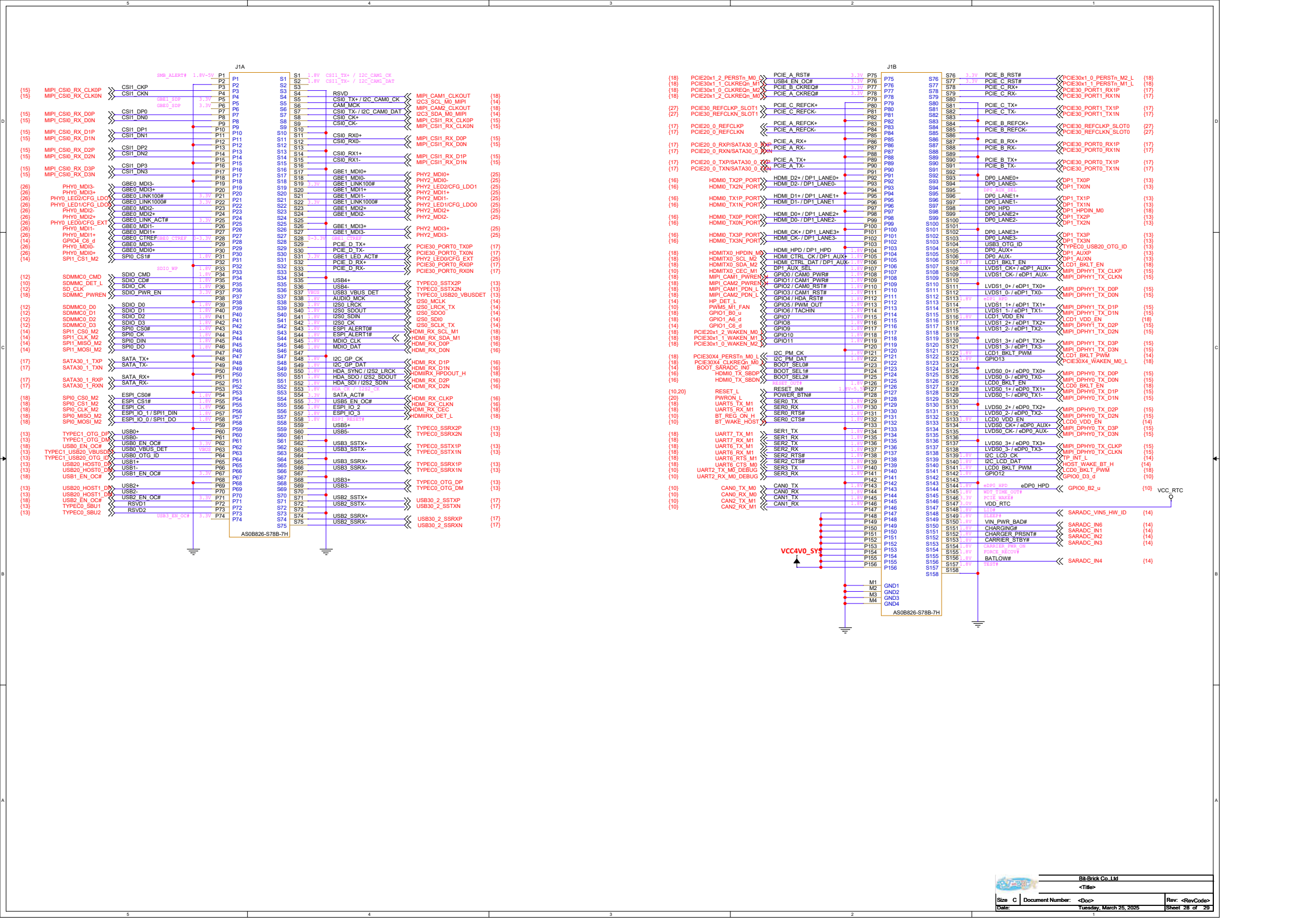
J1A
J1B
AS0B826-S78B-7H
AS0B826-S78B-7H
VCC4V0_SYS
VCC_RTC
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Mark

HOLE

HEATSINK

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