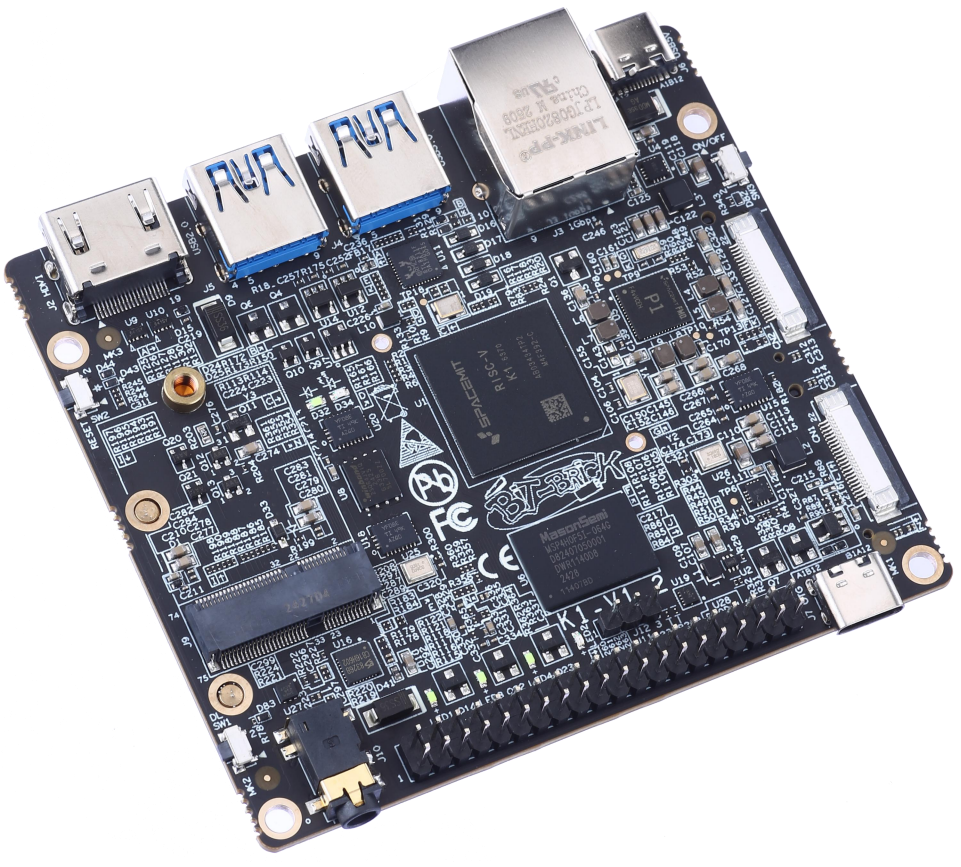
Bit-Brick K1
datasheet



Provisional version

V 1.0

Bit Brick Technology Corporation

February 26, 2025

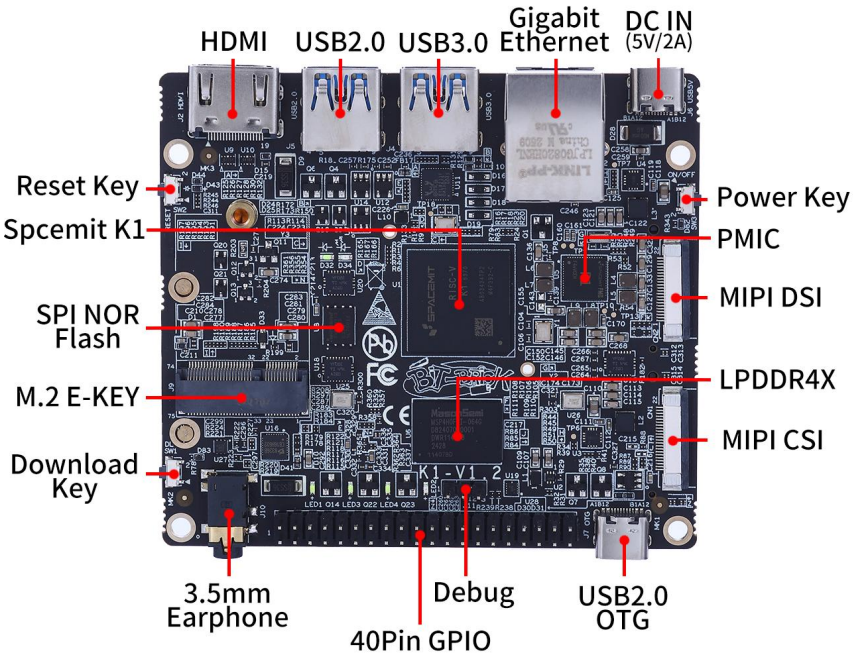
1. introduction

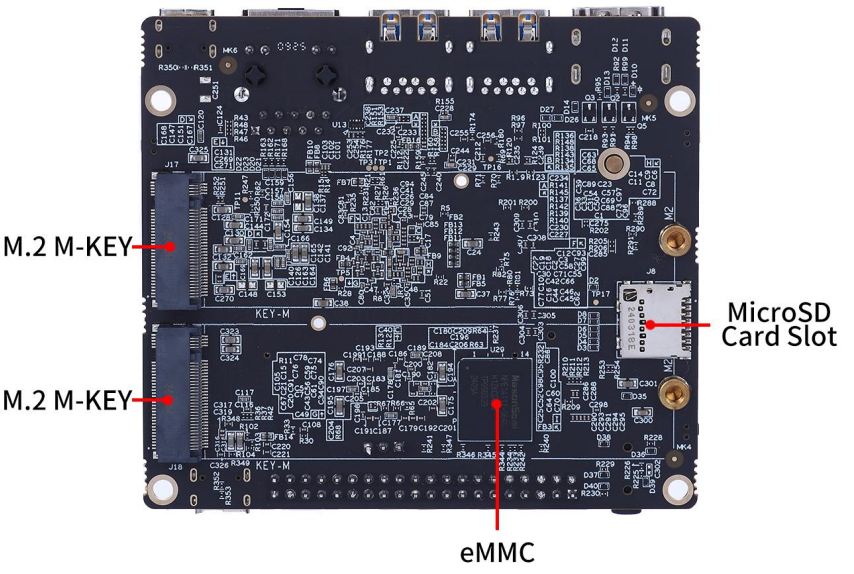
BIT-BRICK K1 is a single-board computer based on the RISC-V application processor of SpacemiT. The motherboard integrates large-capacity high-speed memory, Gigabit Ethernet, high-definition digital display interface, USB3.0 and USB2.0 interfaces, supports dual NVME solid-state drive interfaces, and supports a rich variety of bus interface expansions. K1 is suitable for the different requirements of different people for learning computing technology.

2. Specifications

Form factor	Specification	
Processor	CPU	RISC-V SpacemiT® X60™ Dual-Cluster Octa-core processors, adhere to the RISC-V 64GCVB architecture and RVA22 standard
	GPU	IMG BXE-2-32@819MHz, 32KB SLC, support OpenCL3.0/OpenGL ES 3.2/Vulkan1.3
	AI Performance	2 TOPS
Memory	RAM	LPDDR4X SDRAM (4GB/8GB available)
Graphic	Graph engine	IMG BXE-2-32@819MHz, 32KB SLC, support OpenCL3.0/OpenGL ES 3.2/Vulkan1.3
IO	PCIe	2 x PCIe 2.0 2 lanes for fast peripherals, support NVME SSD
	Ethernet	1 x Gigabit Ethernet
	USB	1 x USB3.0, 1 x USB2.0, 1 x USB2.0 OTG
	Audio	1x 3.5mm headset interface
	SDIO	1
	UART	6
	I2C	4
	SPI	4
	CAN	1
	HDMI	HDMI1.4, support 1920*1080@60fps
	Camera interface	1 x MIPI CSI 4 lanes
	LCD interface	1 x MIPI DSI 4 lanes
	PWM	12
	GPIO	40 Pin, support CAN/UART/SPI/I2C/PWM/I2S etc.
	M.2	1 x M.2 KEY-E for modules, 2 x M.2 KEY-M
Power supply	Power Supply Voltage	Fixed 5V DC source
Environment	Operating Temperature	-40 ~ 85 °C
	Operating Humidity	95% relative humidity, non-condensing
Mechanical	Dimensions (W x D)	90 X 80 mm
Operation System		Bianbu OS/Linux/Open Harmony
Certifications		CE/FCC Class B

3. Functional Block Diagram

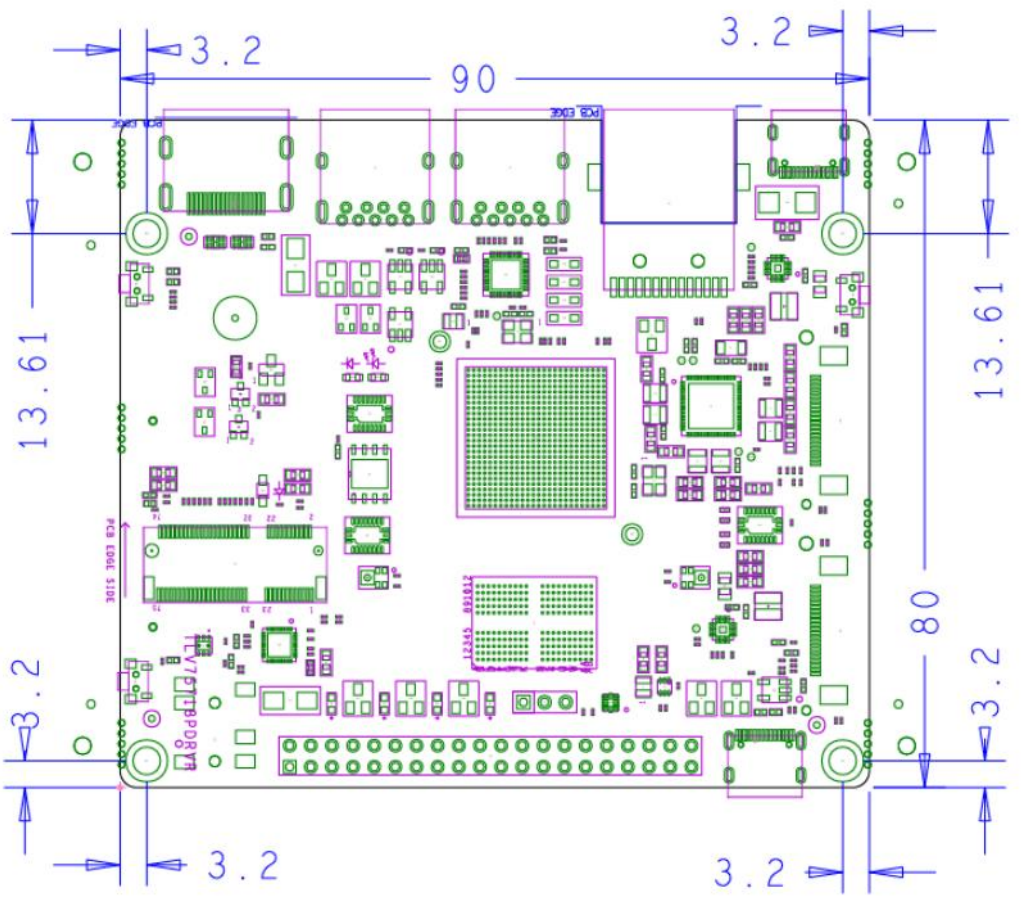




4. Dimension Specifications

Board Dimensions

90.0mm X 80.0mm



5. Application Processor

Product Introduction

SpacemiT® Key Stone™ K1 is a high-performance and ultra low-power SOC that integrates Octa RISC-V CPU cores with SpacemiT® Daoyi ™ AI computing power deployment. K1 has the following features:

- Integrates SpacemiT® self-innovate X60™ RISC-V processor core which adheres to the RISC-V 64GCVB architecture and RVA22 standard.
- Extends 2.0TOPS AI computing power by exploring RISC-V customized instructions to realize CPU AI fusion computing power, and mainstream AI inference frameworks such as TensorFlow Lite, TensorFlow, and ONNX RunTime are supported.
- Achieves ultra low power consumption by implementing different granularities of power islands and various levels of power states to make K1 more competitive and the leading edge.
- Supports full-feature interfaces to enrich more innovatative applications and products.

- Compatible with mainstream OS to meet the needs of various application scenarios.
- Meets Industrial grade reliability standards

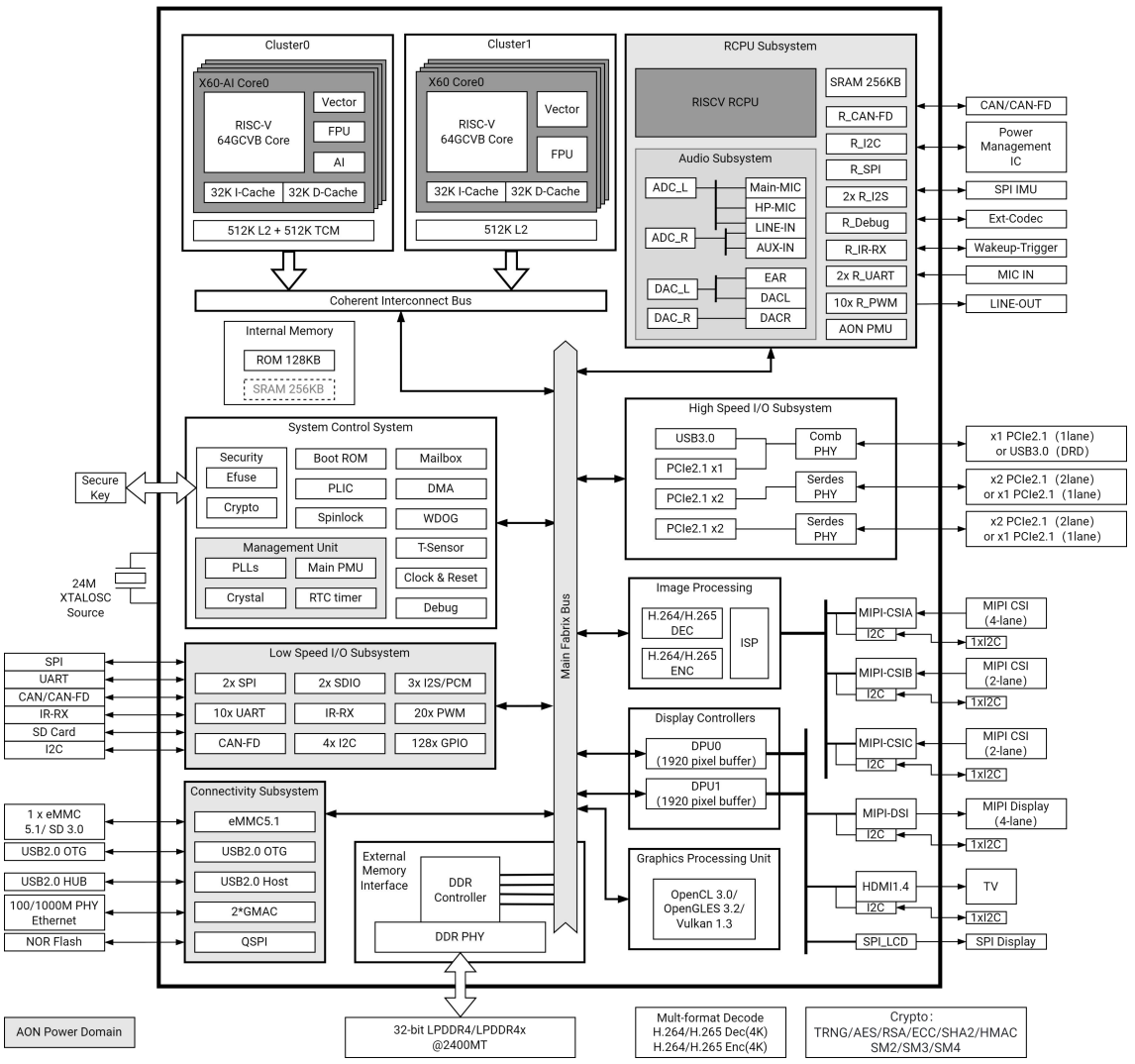
Feature Overview

Application Processor

- RISC-V SpacemiT® X60™ Dual-Cluster Octa-core processors
- Adhere to the RISC-V 64GCVB architecture and RVA22 standard
- Cluster0
  - Quad-Core with 2.0TOPS AI-Power
  - 32K L1-Cache per core
  - 512K L2-Cache
  - 512KB TCM
  - Vector-256bit
- Cluster1
  - Quad-Core
  - 32K L1-Cache per core
  - 512K L2-Cache
  - Vector-256bit
- DVFS with adaptive operating voltage from 0.6V to 1.05V DDR Memory
- Dual chip select 32-bit LPDDR4/LPDDR4x SDRAM with 2666Mbps operation and a total of up to 16GB of RAM
- Dual chip select 32-bit LPDDR3 SDRAM with 1866Mbps operation and a total of up to 4GB of RAM RCPU(Real-Time CPU)
- R-I2C (×1)
- R-I2S (×2)
- R-UART (×2)
- R-CAN_FD (×1)
- R-IR_RX (×1)
- R-PWM (×10)
- R-SPI (×1) Peripheral Controller
- GPIO (×128)
  - 128 pins
  - Pull-up/pull-down programmable
  - 104x 1.8V IO8
  - 24x 1.8V/3.3V IO
- UART (×10)
  - AP/BT/print
- I2C (×10)
  - for camera, G-Sensor/ E-COMPASS/ Proximit-Sensor/ Light-Sensor/Gyro and Fingerprint/NFC, PMIC, touch etc.
  - 8x AP_I2C(AP I2C0/1/7 only for camera)+1x HDMI I2C+1x PWR I2C
- SPI (×4)
  - To support both master and slave mode
  - For IMU, codec etc.
  - Platform has 4 SPI (1x QSPI, 1x SPI LCD, 2x SPI)
- USB (×3)
  - USB 2.0 OTG
  - USB 2.0 Host
  - USB 3.0 (combo PCIE PortA)
- PCIE (×3)
  - PCIE PortA Gen2x1
  - PCIE PortB Gen2x2
  - PCIE PortC Gen2x2
- GMAC (×2)
  - 10/100/1000 Mbps
  - RGMII
- SDIO (×1 for WIFI)
  - compatible for 4-bit SDIO 3.0 UHS-I protocol, up to SDR104 (208MHz)
- SD (×1 for TF card)
  - compatible for 4-bit SD 3.0 UHS-I protocol, up to SDR104 (208MHz)
- eMMC (×1)
  - compatible for 8bit eMMC5.1, up to HS400 (200MHz)
- MIPI CSI (CSI-2 v1.1) 4 lane(×2)
  - 4 Lane + 4 Lane mode
  - 4 Lane + 2 Lane mode
  - 4 Lane + 2 Lane + 2 Lane mode (triple sensor)
- MIPI DSI (DSI v1.1) (×1)

    - 4 Lane DSI
- PWM (×20)
- CAN-FD (×1)
- IR-RX (×1) Security System
- RISC-V PMP Security
- Secure Boot
- Secure eFuse 4K bits
- Cryptographic engine (TRNG/AES/SM2/SM3/SM4/RSA/ECC/SHA2/HMAC) Debug System
- Two JTAGs for both CPU and MCU subsystem
- UARTs
- CPU/IO register snapshot after watchdog reboot Boot System
- Initial AP boot from SPI-Nand/SPI-NorFlash/eMMC/SD
- 128KB boot-ROM size Aided System
- Watchdog design for each CPU/MCU subsystem Multimedia Features GPU
- IMG BXE-2-32@819MHz, 32KB SLC
- Support OpenCL3.0/OpenGL ES 3.2/Vulkan1.3 VPU (video processing unit)
- H.265/H.264/VP8/VP9/MPEG4/MPEG2 decoder 4K@60fps
- H.265/H.264/VP8/VP9 encoder 4K@30fps
- Support simultaneously processing encoding 1080P@60fps and decoding 1080P@60fps
- Support simultaneously processing H264/H265 encoding 1080P@30fps and H264/H265 decoding 4K@30fps Display
- 1 MIPI DSI-4lane or SPI interface
- Support up to HD + (1920x1080@60fps)
- Support up to 4-full-size-layer composer and maximum 8 layer composer by up-down layer reuse in rdma channel
- Support cmdlist mechanism, which can configure register parameters by HW
- Support concurrent write back, with both raw and afbc format, also support dither/crop/rotation in write back path
- Support advanced mmu (virtual address) mechanism, with nearly no page missing in 90/270 degree rotation
- Support color key and solid color
- Support both advanced error diffusion and pattern based dither for panel
- Support both afbc/raw format image source
- Color saturation/contrast enhancement
- Support both video mode and cmd mode for panel
- Support ddr frequency dynamic changing with embedded dfc buffer HDMI 1.4 Camera
- Dual-ISP
    - 16M (max.) 30fps Dual ISP
    - One 4 Lane CSI + one 4 Lane CSI or 4 Lane + 2 lane + 2 lane
    - RAW sensor, output YUV data to DRAM
    - Hardware JPEG encoder(hardware, up to 23M is supported)
    - Support YUV/EXIF/JFIF format
    - AF/AE/AWB
    - Face detection
    - Digital zoom, panorama view
    - PDAF
    - PIP (picture in picture)
    - Continuous video AF
    - HW 3D denoise Audio
- Integrated high quality audio codec and audio front-end
- ADC: 90dB SNR@20~20kHz
- DAC: 95dB SNR@20~20kHz
- Class-G: 95dB SNR@20~20kHz, 31mW@32-ohm, THD -90dB
- ClassAB: 95dB SNR@20~20kHz, 75mW@32-ohm, THD-90dB
- Line-out to support external Class-D audio amplifier (Class-D in PMIC: 95dB SNR@20 ~ 20kHz, 1W@4.2Vbat 10%THD + N, 8-ohm speaker)
- Three MICs input
- Stereo inputs path for noise cancellation
- Stereo headphone output
- Audio content sampling rates: 8kHz to 48kHz
- Microphone bias for headphone plug-in and hook-key detection
- Quad vocoders for adaptive multi-rate (AMR)
- Noise suppression and echo cancellation General
- Operation temperature: -40 ~ 85° C

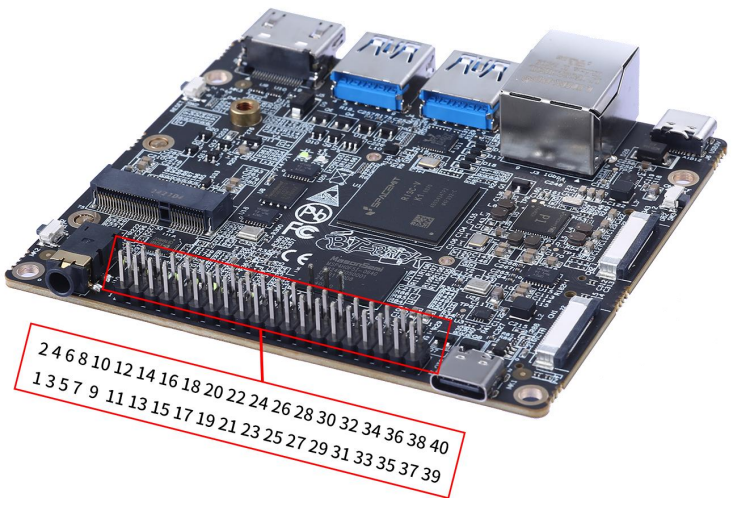
Block Diagram

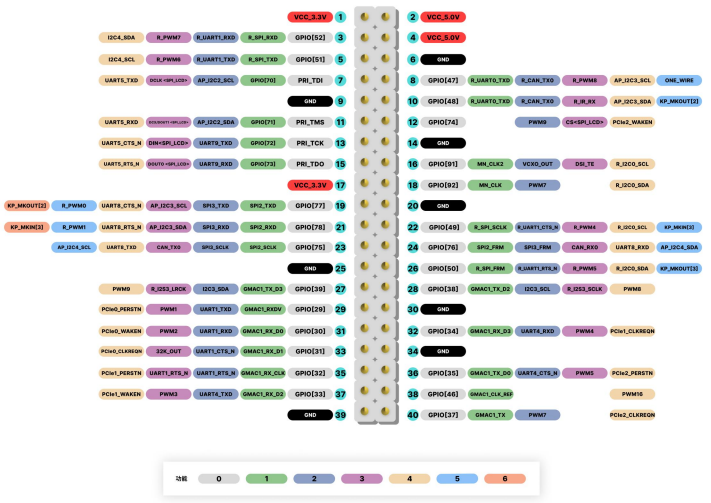


6. GPIO Extension Interface

K1 reserves a 40-pin GPIO extension interface, using a 2.54 double-row straight insertion socket, which is convenient for enthusiasts to connect peripherals according to their own needs and expand different functions. Our system will set these IOs to some specific functions by default, but users can reconfigure them through software to make these general-purpose IOs have some special functions, because these IOs are all multi-functional multiplexed pins.

Pin definations

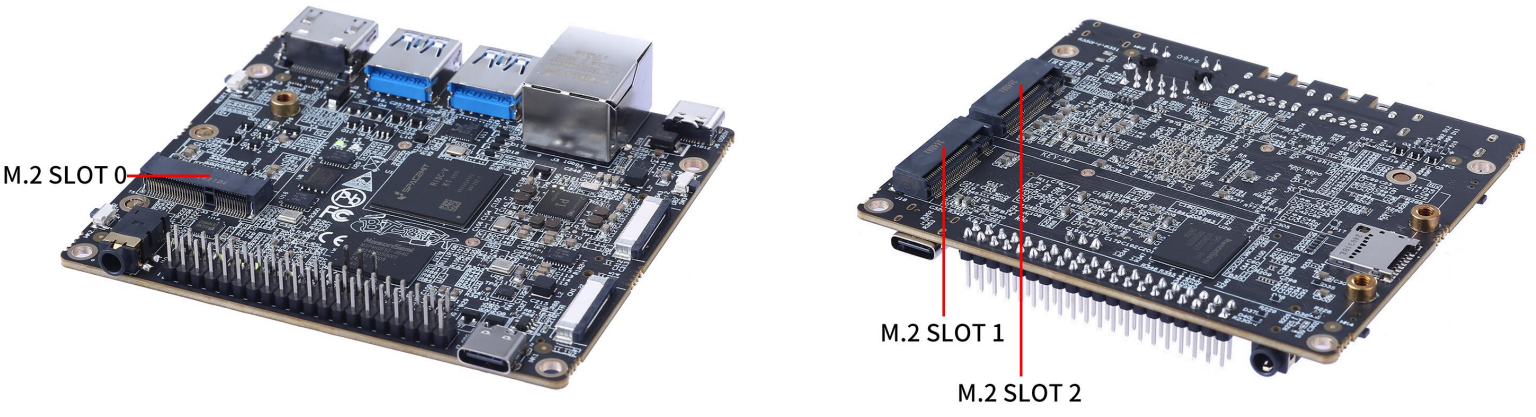




7. M.2 Interface Description

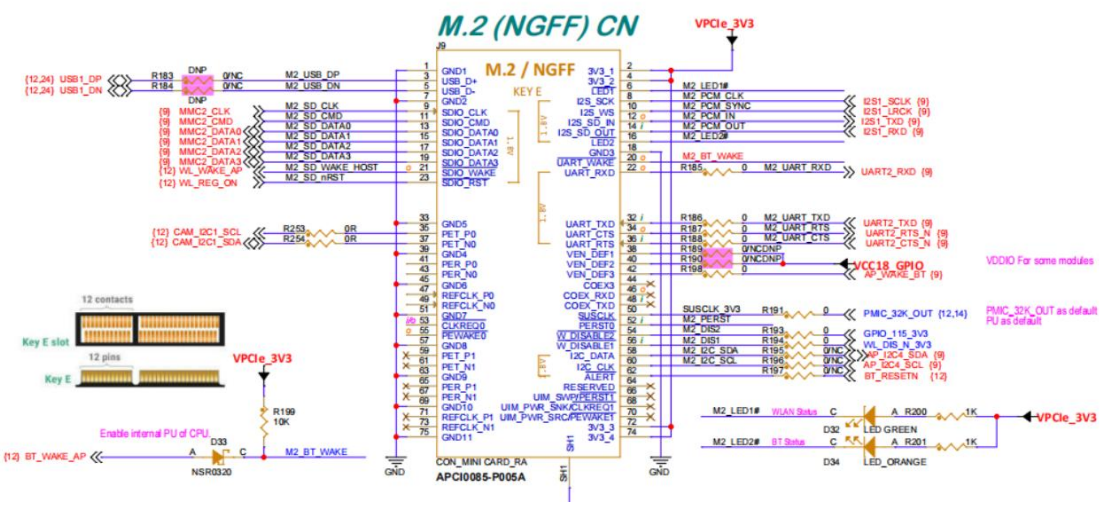
M.2 Interface

M.2 is the physical size and pin electrical interface specification for internal expansion cards and related connectors in computers. It adopts a new physical layout and connector to replace the PCI Express (PCIE) and mSATA interface standards. M.2 has flexible physical specifications, allowing for more types of module widths and lengths, and is compatible with more advanced interfaces, making M.2 more suitable for daily applications than mSATA, especially for solid-state drives in devices such as ultrabooks or tablets.
The K1 board integrates three M.2 interfaces, as shown in the following figure:



Among them, M.2 SLOT 1 and 2 are standard M.2 KEY-M interface definitions, which can directly support solid-state drives with the NVME interface. The length of the solid-state drive can be 2280. Users can choose SSDs with the mainstream NVME interface.

The other M.2 SLOT 0 is the interface definition of KEY-E, with a length of 2230, which is mainly used to support various wireless modules. Since the processor only has three USB interfaces, the USB interface is not reserved for SLOT 0, and the PCIE interface compatible with NGFF is also removed, so modules with USB and PCIE interface definitions are not supported. The detailed description of the pin definition of the SLOT 0 interface is as follows:



8. Camera Interface Description

MIPI CSI2 Controlle

The RISC - V application processor of K1 integrates two MIPI - CSI2 v1.1 controllers, each supporting 4 lanes with a maximum transmission rate of 1.5Gbps per lane. The supported data formats are as follows:

- Legacy YUV420 8 - bit
- YUV420 8 - bit
- RAW8
- RAW10
- RAW12
- RAW14
- Embed data type And it supports the following two data interleaving formats:
  1. Data type interleaving
  2. Virtual channel interleaving

ISP Processor

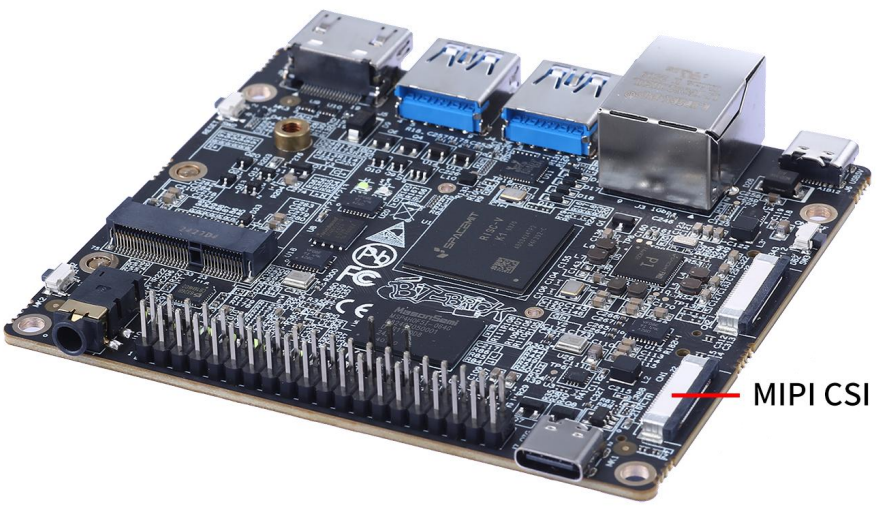
The K1 processor integrates a high - performance image processor that can simultaneously support two channels of raw data video streams, with a maximum processing capability of 16M@30fps. The main features of the ISP processor are as follows:

- Support video mode and picture mode
- RAW sensor, output YUV data to DRAM
- Hardware JPEG encoder/decoder (hardware, up to 23M is supported)
- Support YUV/EXIF/JFIF format
- AF/AE/AWB
- Face detection
- Digital zoom, panorama view
- PDAF
- PIP (picture in picture)

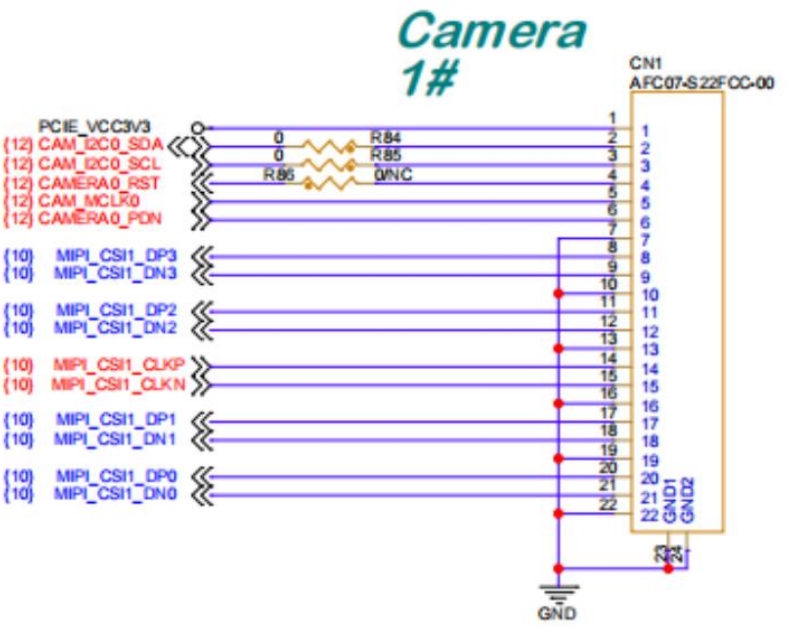
- Continuous video AF
- HW 3D denoise
- Multi - layer 2D YUV denoise
- Post Porcess of Lens Shading Correction
- Edge enhancement For more detailed information, you can read the chip specification: ISP Processor Specifications

BIT - BRICK K1 Camera

The BIT - BRICK K1 board reserves a 4 - lane MIPI CSI2S camera interface



Its pin definition is as follows:



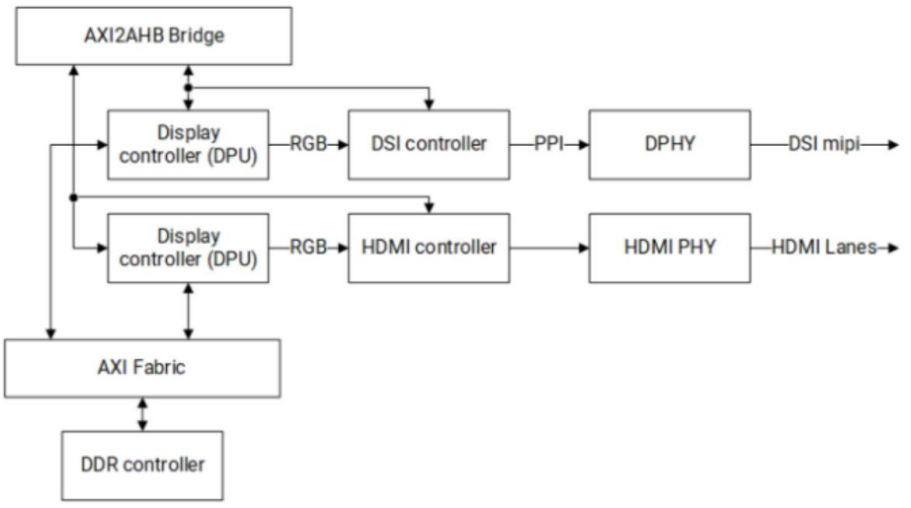
Users can design the camera according to their actual needs. The supported camera sensors are as follows:

序号	型号	像素	接口	位宽（bits）	帧率（fps）	已支持最大分辨率	厂家
1	GC2375	2M	MIPI CSI 1lane	10	30	1600x1200	格科微
2	S5K5E3YX	5M	MIPI CSI 2lane	10	30	2560x1920	三星
3	IMX135	13M	MIPI CSI 4lane	10	30	4208x3120	索尼
4	SC031GS	0.3M	MIPI CSI 1lane	10	30	640x480	思特威
5	GC5035	5M	MIPI CSI 2lane	10	30	2592x1944	格科微
6	OS05A10	2M	MIPI CSI 1lane	10	30	1920x1080	豪威
7	OV08D10	8M	MIPI CSI 2lane	10	30	3264x2448	豪威
8	OV13B10	13M	MIPI CSI 4lane	10	30	4208x3120	豪威
9	OV16A10	16M	MIPI CSI 4lane	10	30	3840x2160	豪威
10	OV8856	8M	MIPI CSI 4lane	10	30	2560x1440	豪威

It is recommended to choose the sensors in the above list to reduce the workload of software debugging.

9. Display Interface Description

The K1 motherboard supports HDMI and MIPI DSI2 interface-defined LCD displays as the graphical output interface.

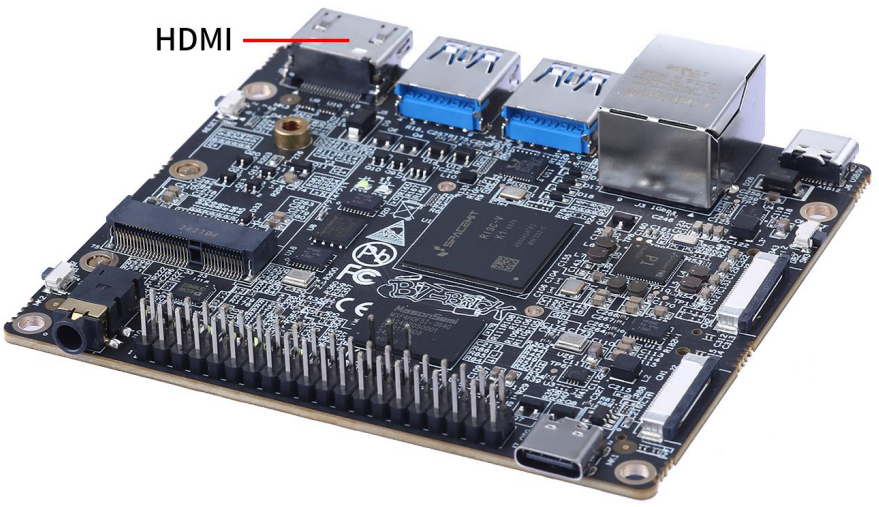


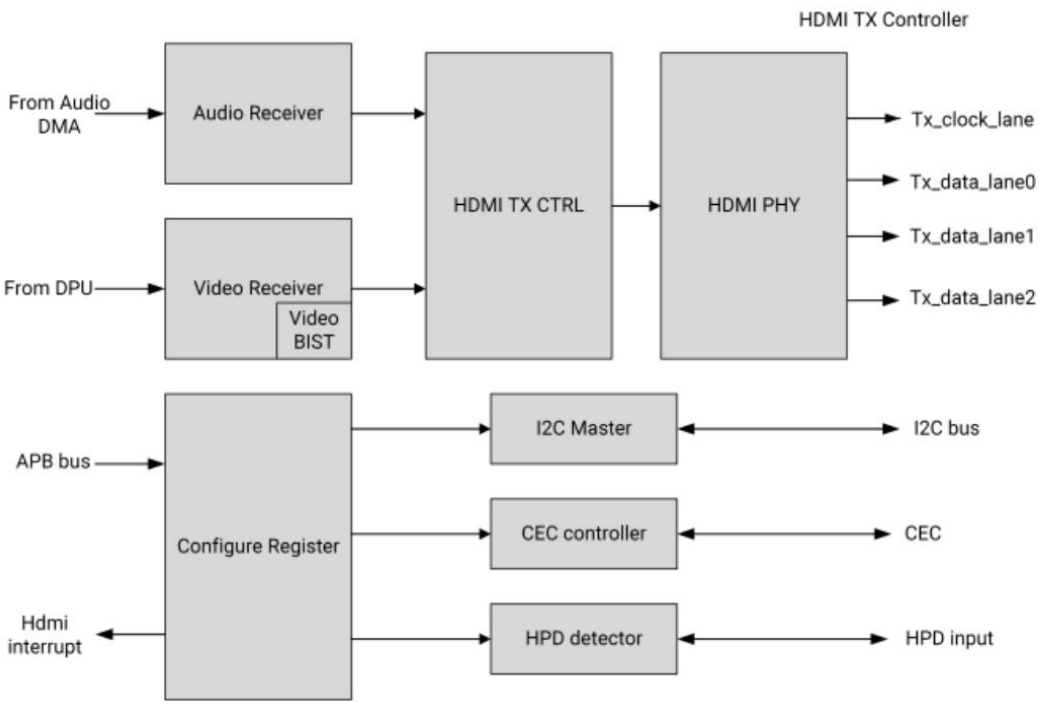
Block Diagram of the Processor Display Subsystem

HDMI

K1 supports the HDMI1.4a version, and the maximum resolution supports 1920*1080@60fps. The main features are as follows:

- Compliant with HDMI Specification v1.4
- Physical lane speed: up to 2.4Gbps/lane × 3lane
- Support resolution: up to 1920*1440@60Hz
- Support RGB, YcbCr4: 2: 2/4: 4: 4 input video
- Support RGB, YcbCr4: 2: 2/4: 4: 4 output video
- Support 8bpc/10bpc/12bpc input and output color depth
- Support EIA/CEA-861-F video timing and InfoFrame structure
- Support L-PCM (IEC 60958), 32KHz ~ 192KHz dual channel audio data
- Support Consumer Electronic Control (CEC)
- Internal I2C Master, support 100Kbps ~ 400Kbps





HDMI Transmission Block Diagram

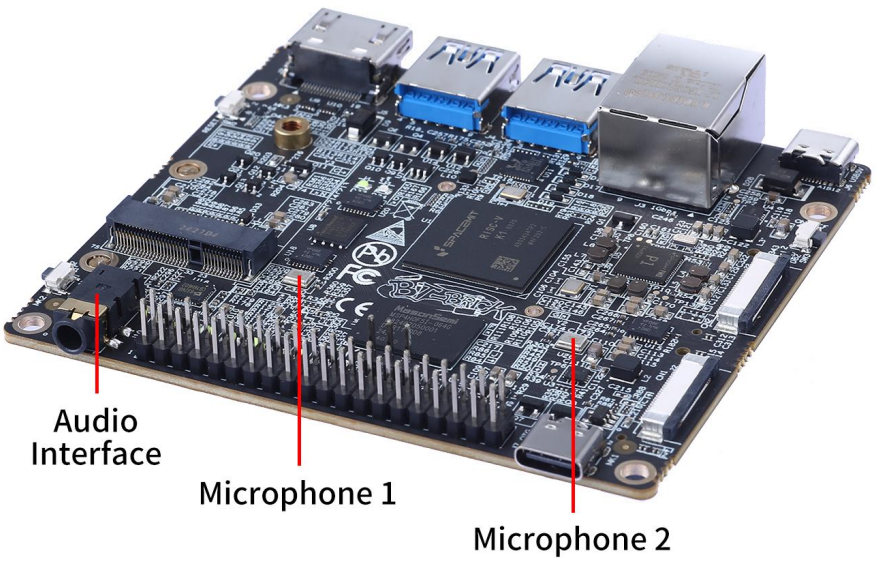
You can directly connect K1 and the display using a standard HDMI cable (if the display interface is not HDMI, you can purchase an HDMI converter, such as HDMI to DP, etc.)

10. Audio Interface Description

Hardware Components

The audio part of K1 is mainly composed of three aspects:

- HDMI audio output
- 3.5mm standard audio socket
- Left and right channel microphone input

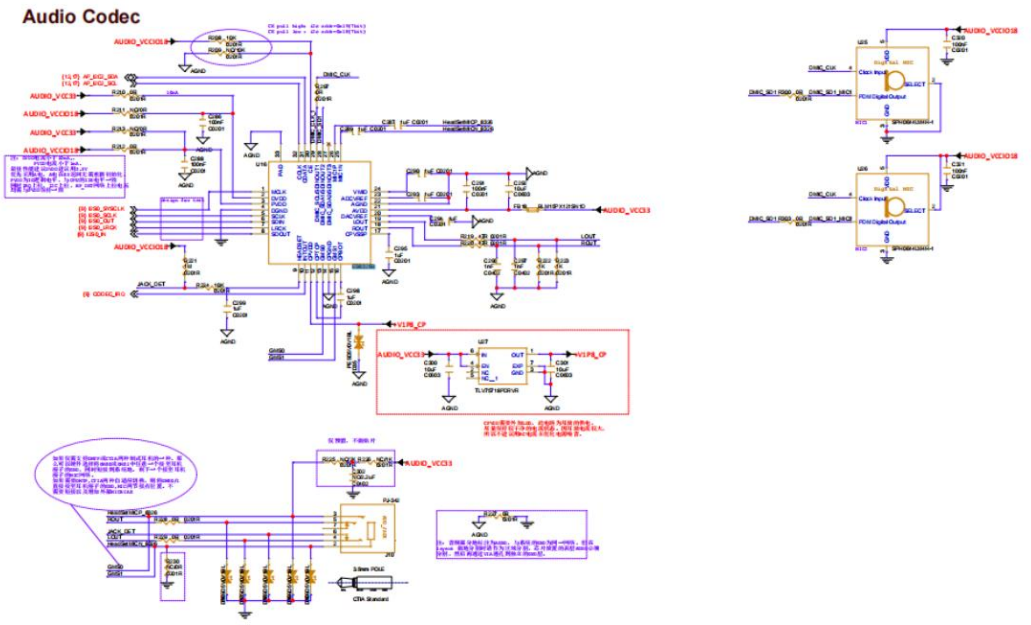


Schematic Diagram of the Audio Interface

Circuit

Although the processor internally integrates an audio Codec, K1 still adopts the approach of an external Codec in the design. It connects to the ES8326B through the I2S interface to achieve audio input and output.

The ES8326B chip is an audio decoding chip, mainly used to convert digital audio signals into analog audio signals. It uses a high-performance digital signal processor and a low-power power amplifier to achieve a high-definition music experience and high-quality call requirements. For detailed specifications, refer to the ES8326B section in the data booklet.



Circuit of the Audio Part

11. Ordering Information

Part No.	CPU	Memory	Operating Temperature
Bit-Brick-K1-4320	K1	4GB	-40~85°C
Bit-Brick-K1-2160	K1	8GB	-40~85°C

12. Update History

Version Revision	Update Date	Content
Provisional V 1.0	2025-2-26	Initial the first version