K1_DVP_BOARD

Revision History

Rev. Code	Date	By	Description
V1.0	2024-08-01	Bzliu	Initial version

INDEX/NOTES

Bit-Brick Co.,Ltd			
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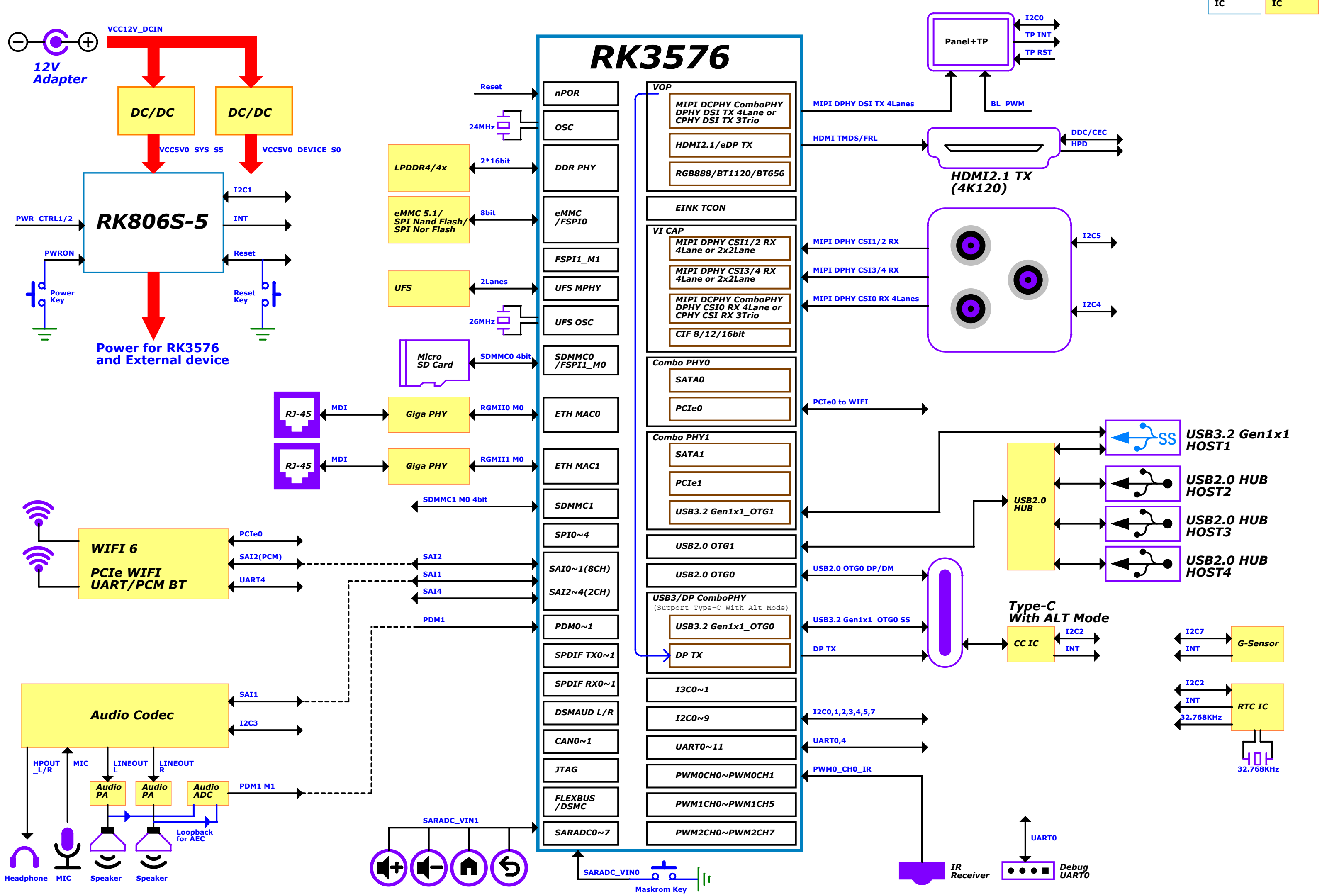
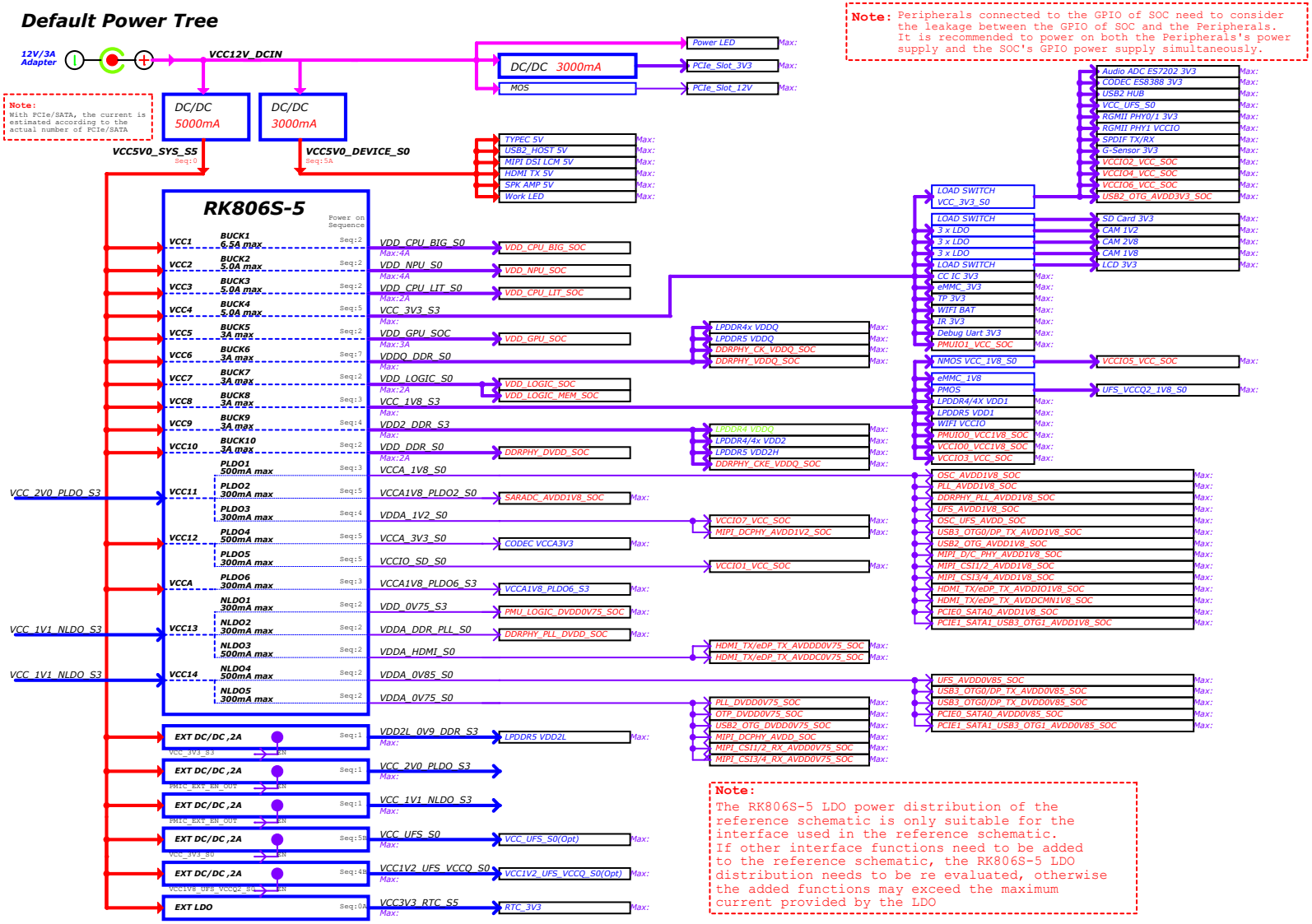
BLOCK

RK3576 Ref Block Diagram(Typical Application Case)



Default Power Tree



Rockchip	RK Rock Co. Ltd		
	K1_DVP_BOARD		
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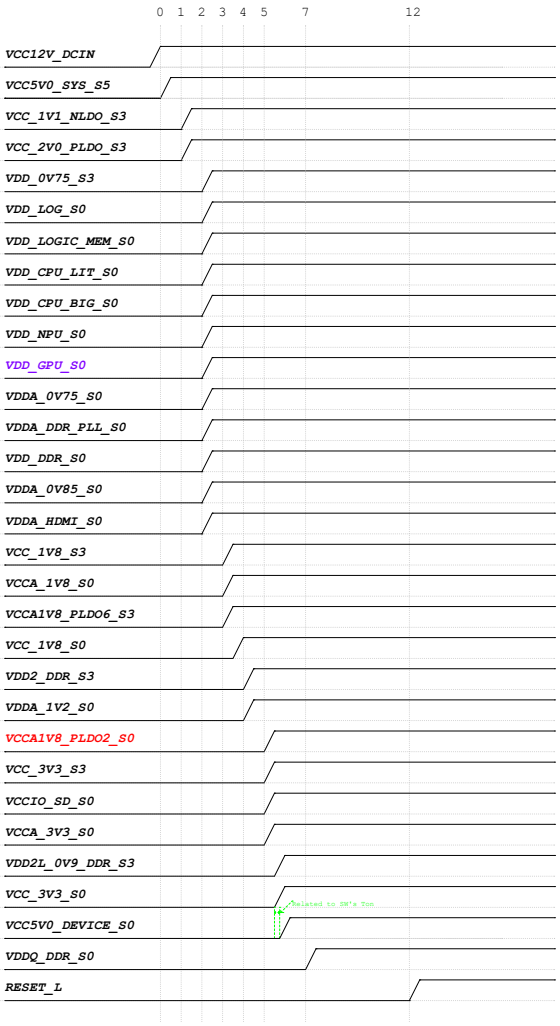
Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5A	0.9V	ON	0.9V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:

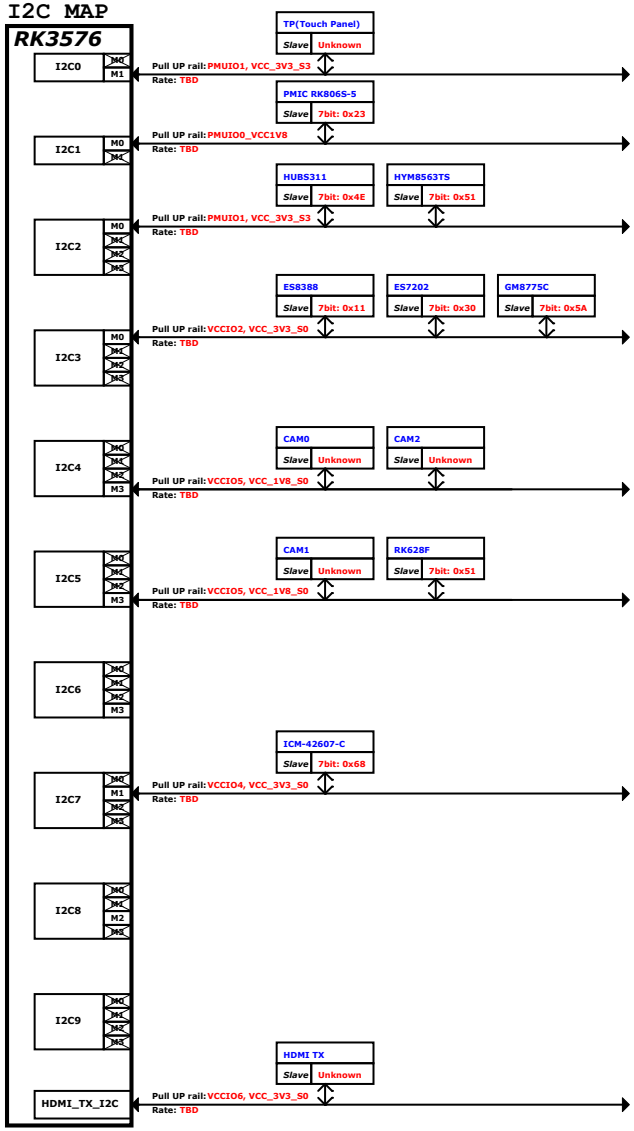
Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

IO Power Domain Map

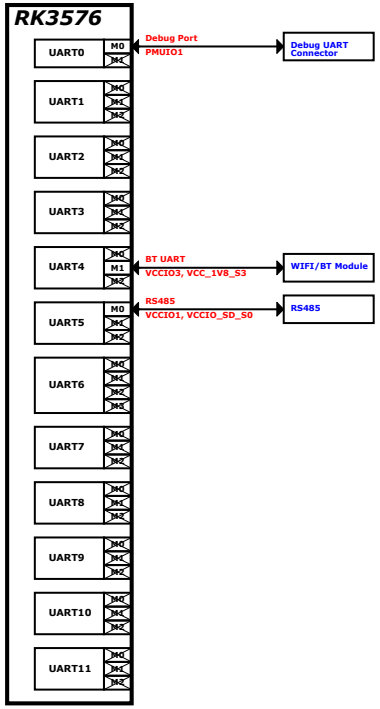
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

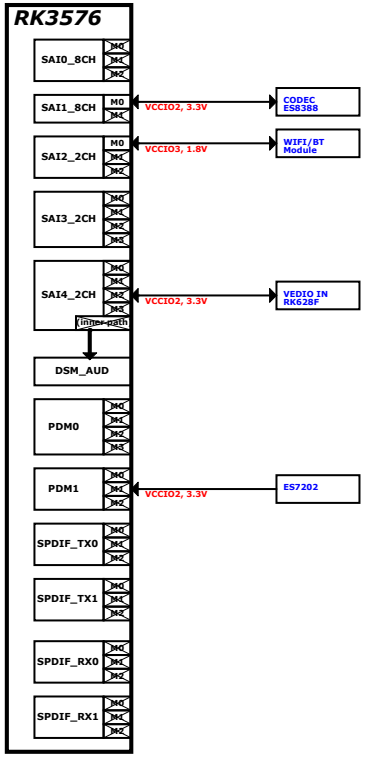
I2C MAP



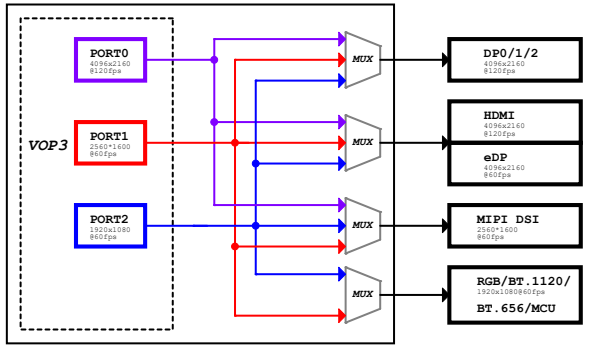
UART MAP



Audio MAP



VO MAP



Note:

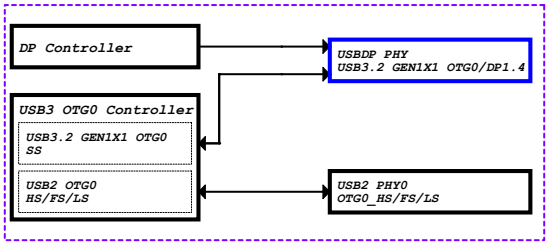
M0 Unselected IOmux path

M1 IOmux path in use

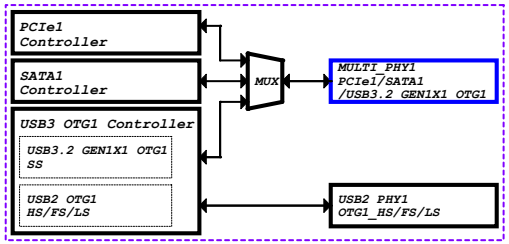
At the same time, only one path can be selected.

MULTI_PHY Path Map

USBDP PHY--USB3.2 GEN1X1 OTG0/DP1.4



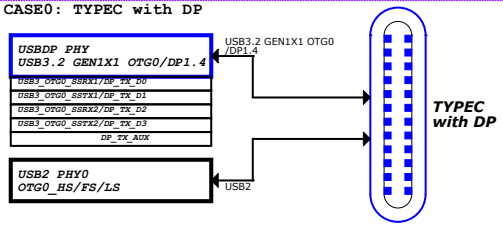
PCIe Combo PHY1-- PCIe1/SATA1/USB3.2 GEN1X1 OTG1



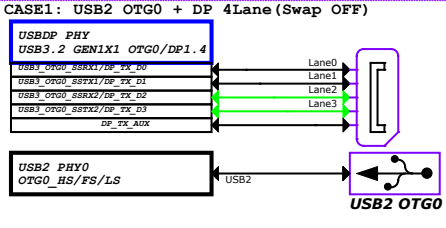
Note:
USB2 PHY1 can only be used when PCIE1/SATA1 is not in use!!!

USB OTG0/DP Application

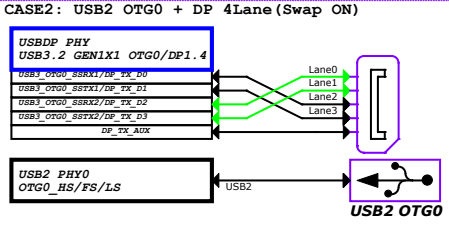
CASE0: TYPEC with DP



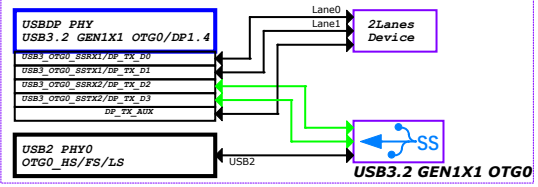
CASE1: USB2 OTG0 + DP 4Lane(Swap OFF)



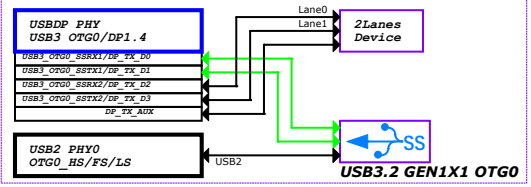
CASE2: USB2 OTG0 + DP 4Lane(Swap ON)



CASE3: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap OFF)



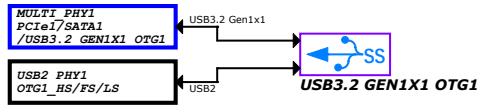
CASE4: USB3.2 GEN1X1 OTG0 + DP 2Lane(Swap ON)



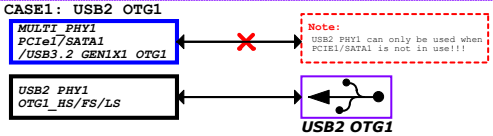
Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3_TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1_TXDP/N

USB OTG1 Application

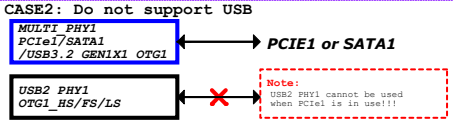
CASE0: USB3.2 GEN1X1 OTG1



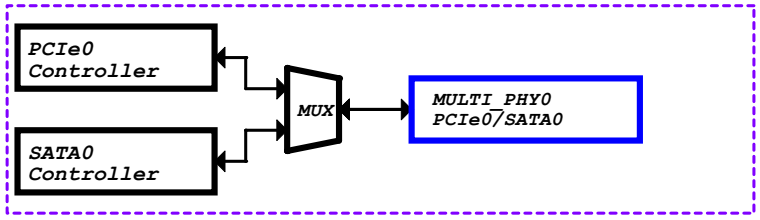
CASE1: USB2 OTG1

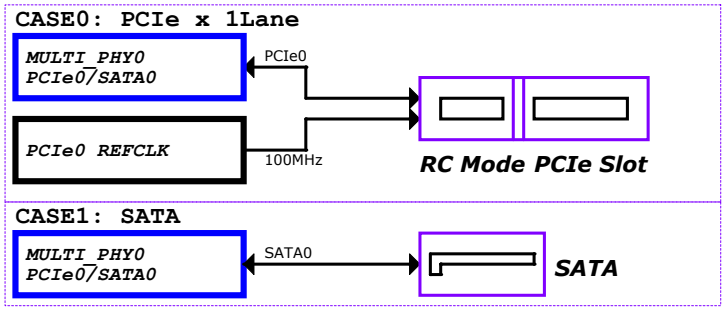


CASE2: Do not support USB

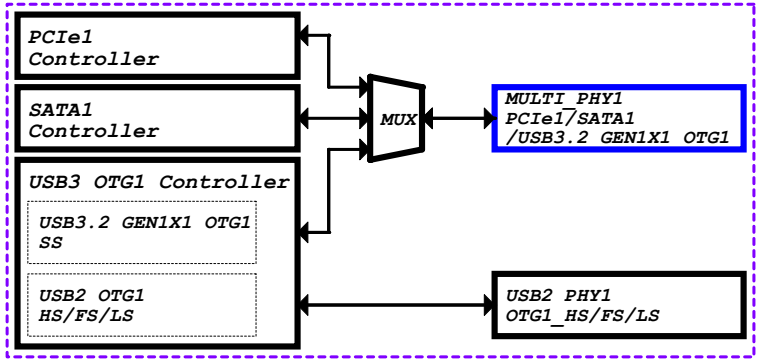


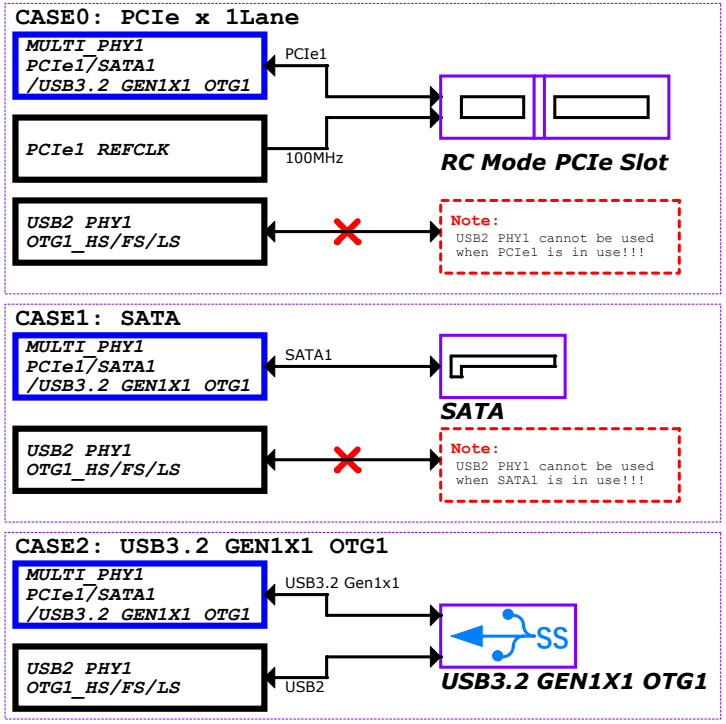
PCIe Combo PHY0--PCIe0/SATA0





PCIe Combo PHY1--
PCIe1/SATA1/USB3.2 GEN1X1 OTG1





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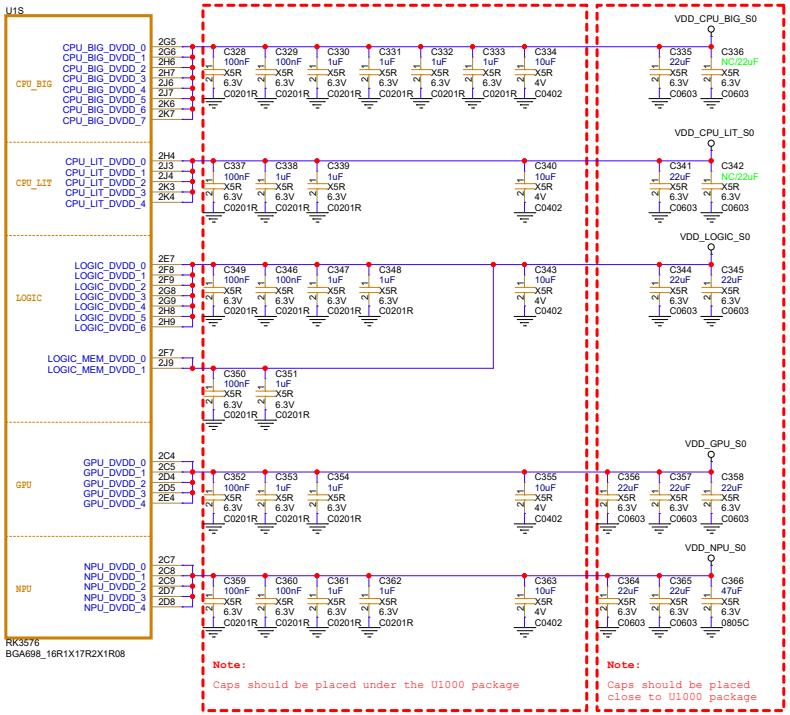
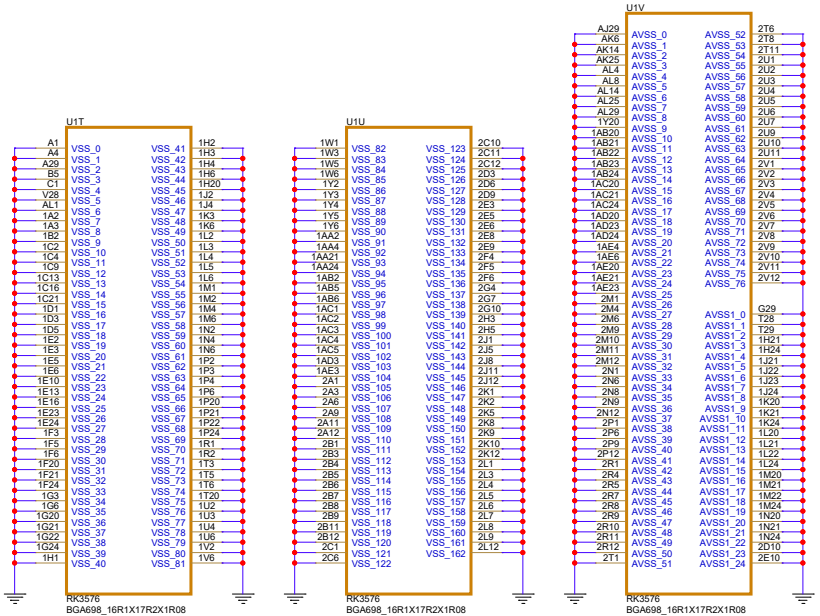
RK3576_S (Power)



RK3576_T/U/V (GND)



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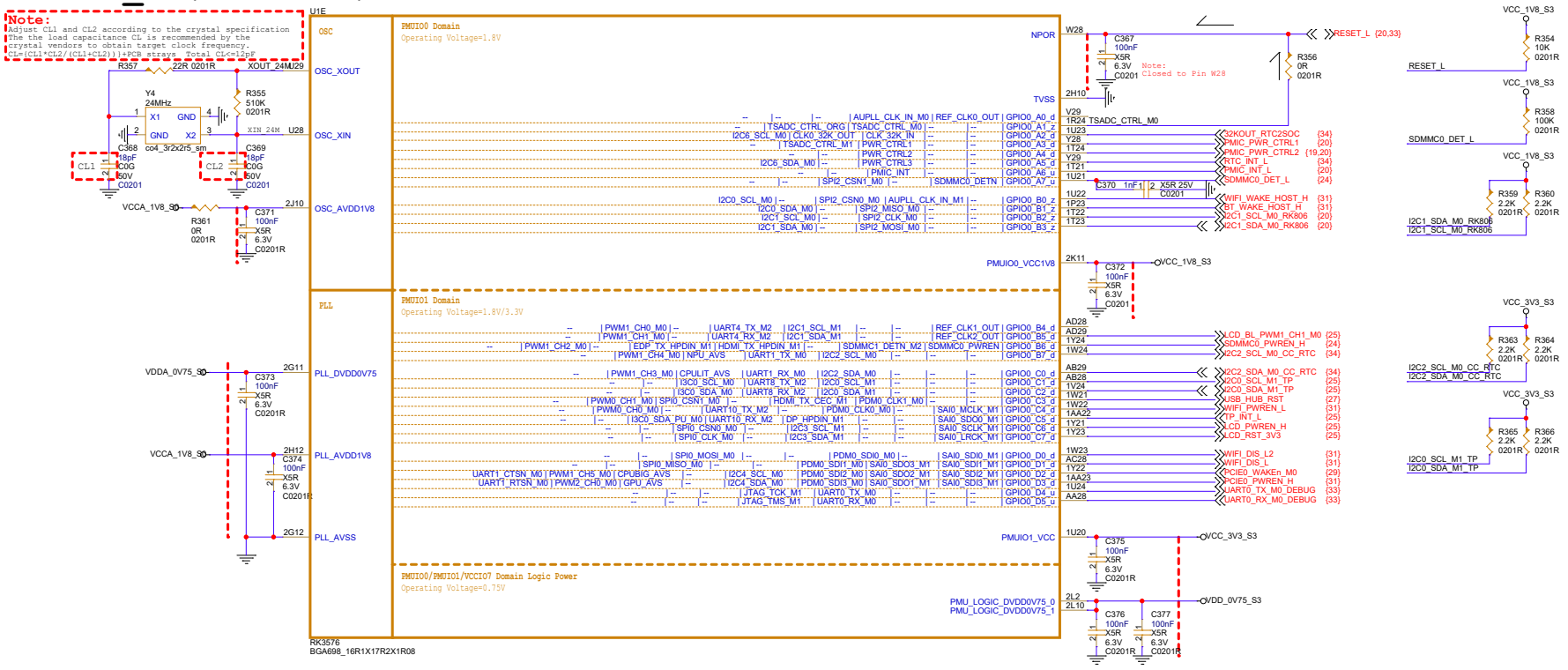
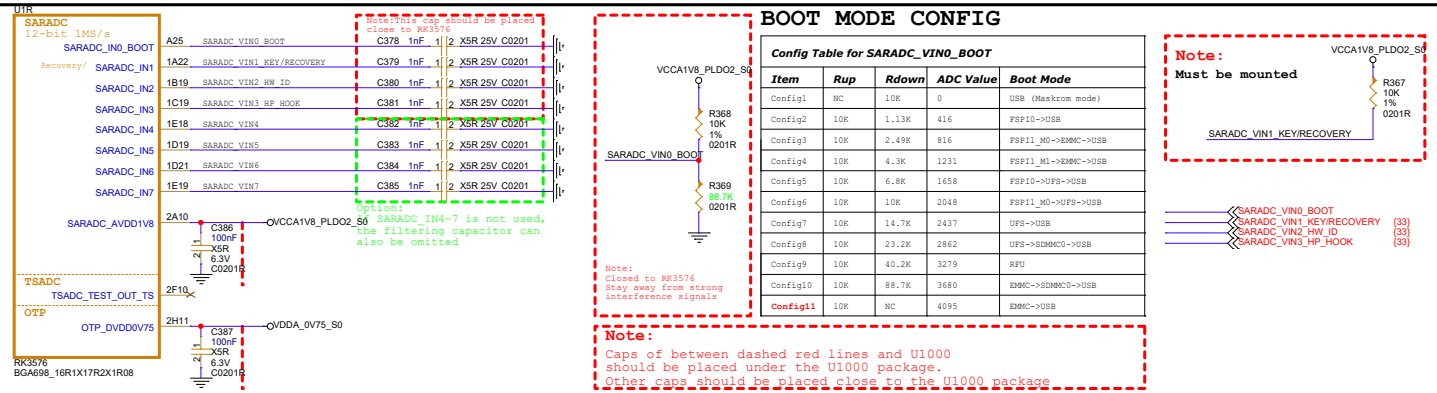
RK3576_E (PMUIO0/1)



RK3576_R (SARADC)



BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	10K	1.13K	416	FSPI0->USB
Config3	10K	2.49K	816	FSPI1_M0->EMMC->USB
Config4	10K	4.3K	1231	FSPI1_M1->EMMC->USB
Config5	10K	6.8K	1658	FSPI0->UFS->USB
Config6	10K	10K	2048	FSPI1_M0->UFS->USB
Config7	10K	14.7K	2437	UFS->USB
Config8	10K	23.2K	2862	UFS->SDMMC0->USB
Config9	10K	40.2K	3279	RFU
Config10	10K	88.7K	3680	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

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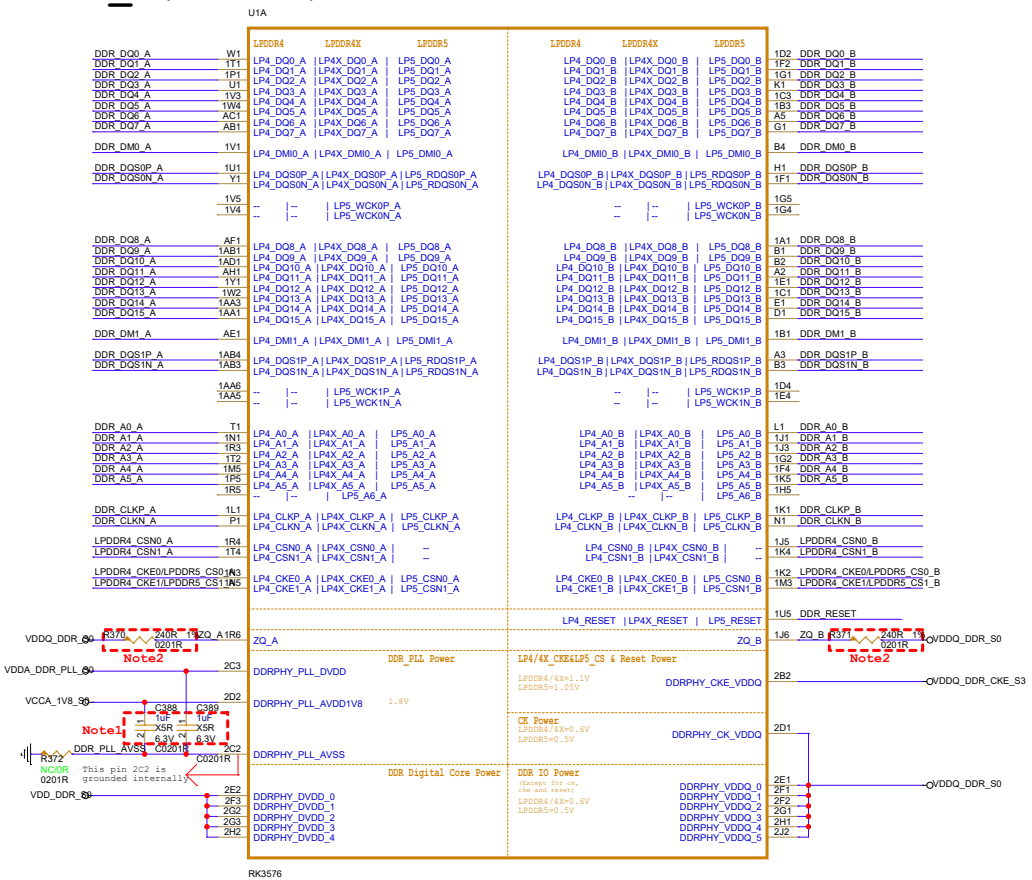
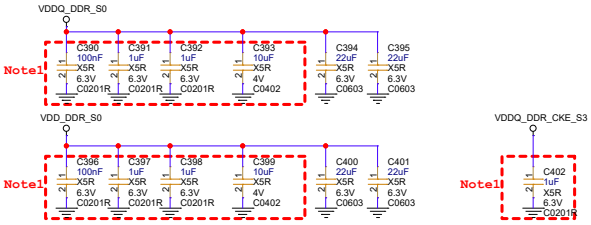
RK3576_A(DDRPHY)



DDR FILTER

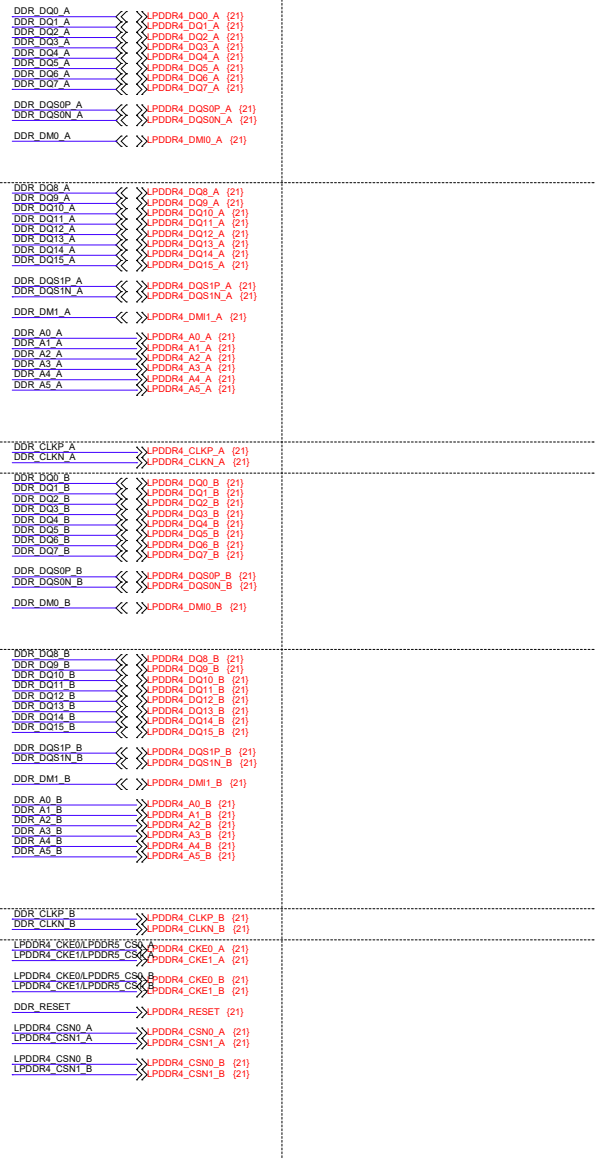


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1000 package

Note2:
Resistors in the red line dotted box should be placed under the U1000 package

LPDDR4/4X



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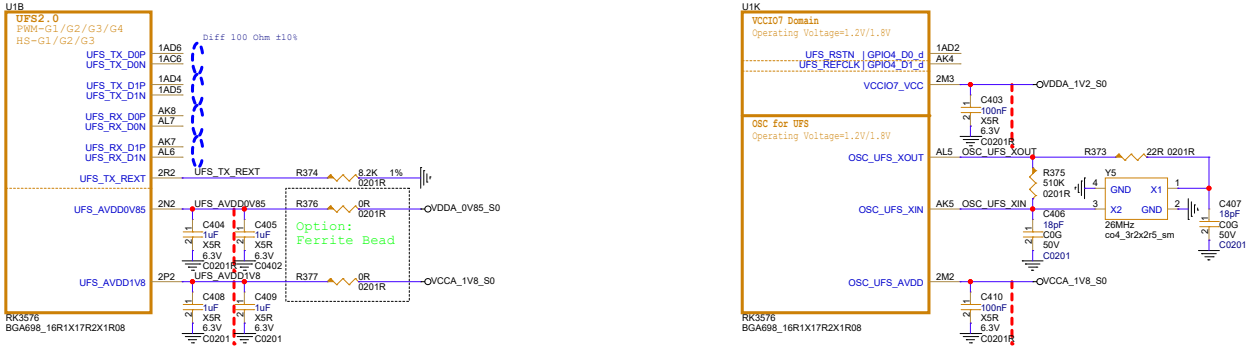
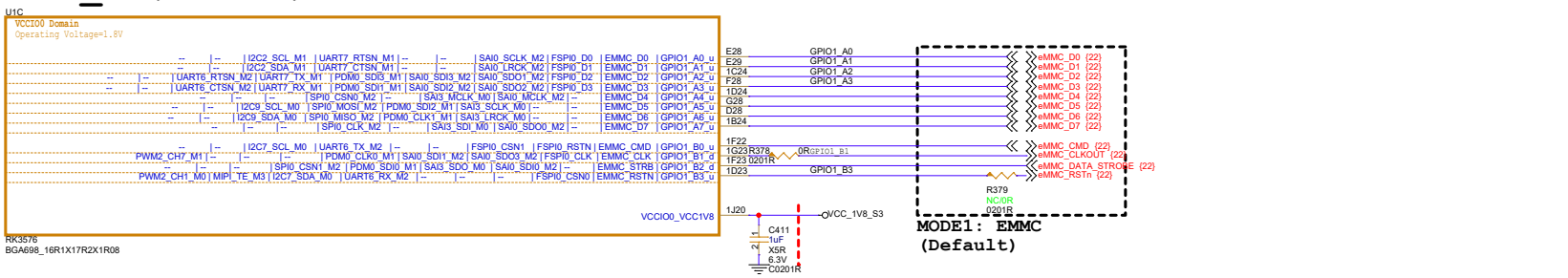
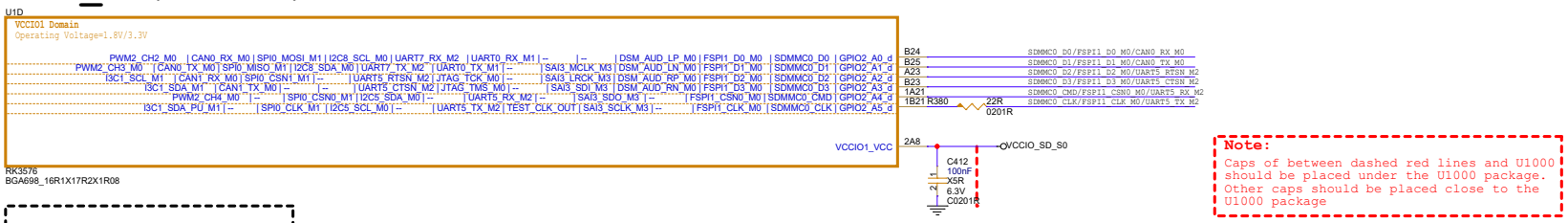
RK3576_B (UFS2.0)



RK3576_C (VCCIO0)



RK3576_D (VCCIO1)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

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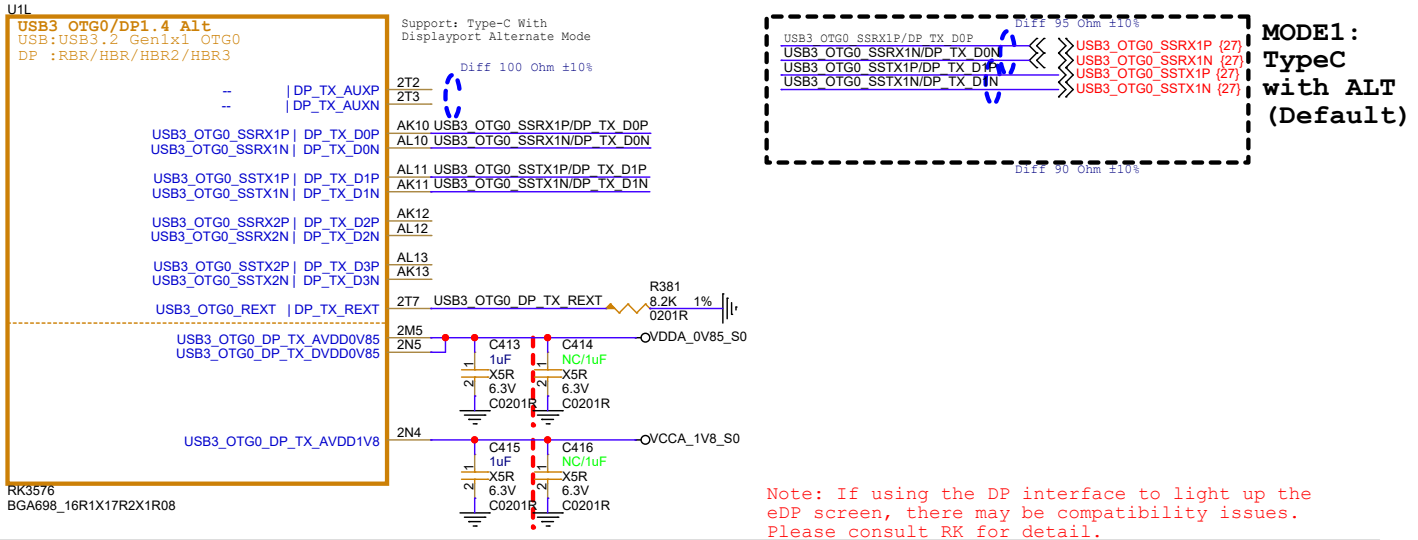
RK3576_L (USB3/DP)

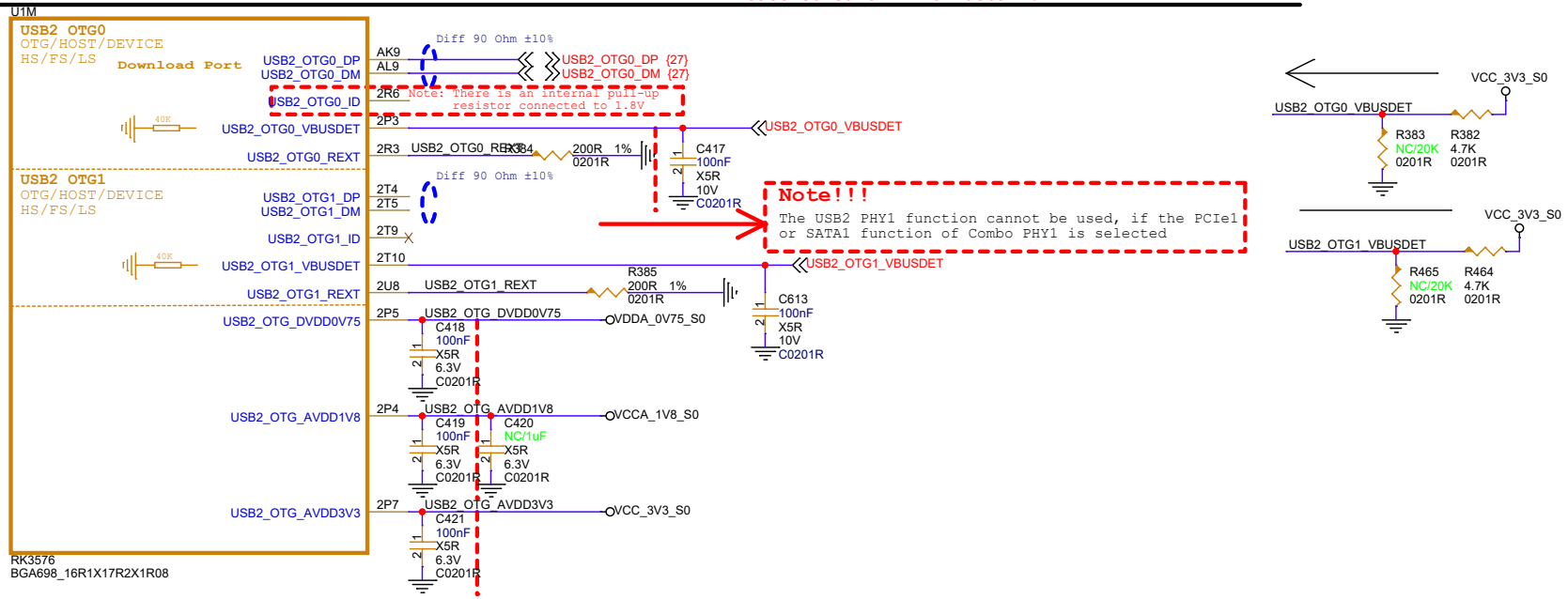


MODE1: TypeC with ALT (Default)

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Note: If using the DP interface to light up the eDP screen, there may be compatibility issues. Please consult RK for detail.

RK3576_M (USB2)



Note!!!
The USB2 PHY1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Bit-Brick Co.,Ltd			
K1_DVP_BOARD			
Size B	Document Number: CPU USB		Rev: V1.0
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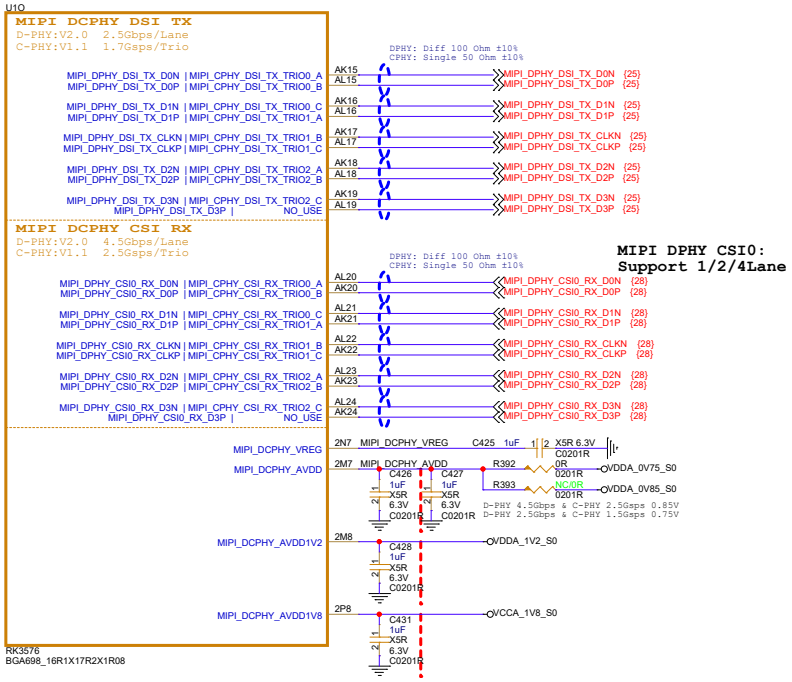
RK3576_O(MIPI DCPHY)

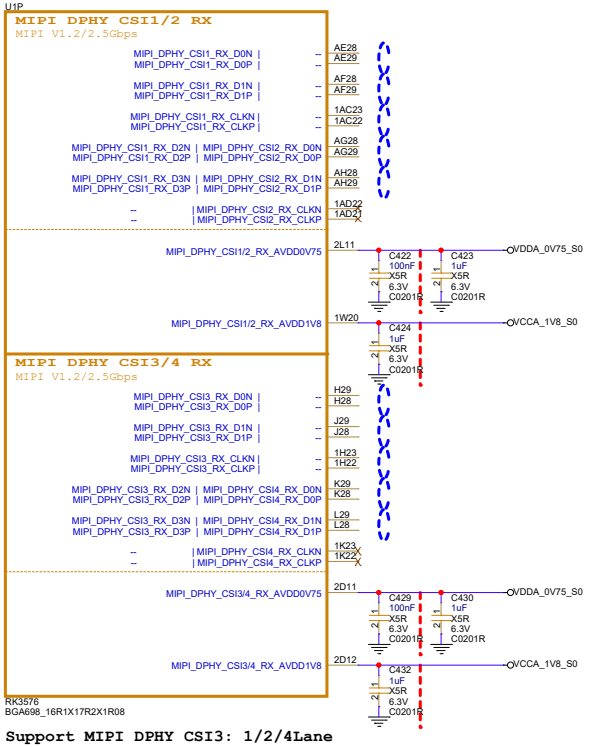


MIPI DPHY CSI0:
Support 1/2/4Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

Support MIPI DPHY CSI1: 1/2/4Lane
Support MIPI DPHY CSI2: 1/2Lane
Support: MIPI DPHY CSI1 2Lane + MIPI DPHY CSI2 2Lane



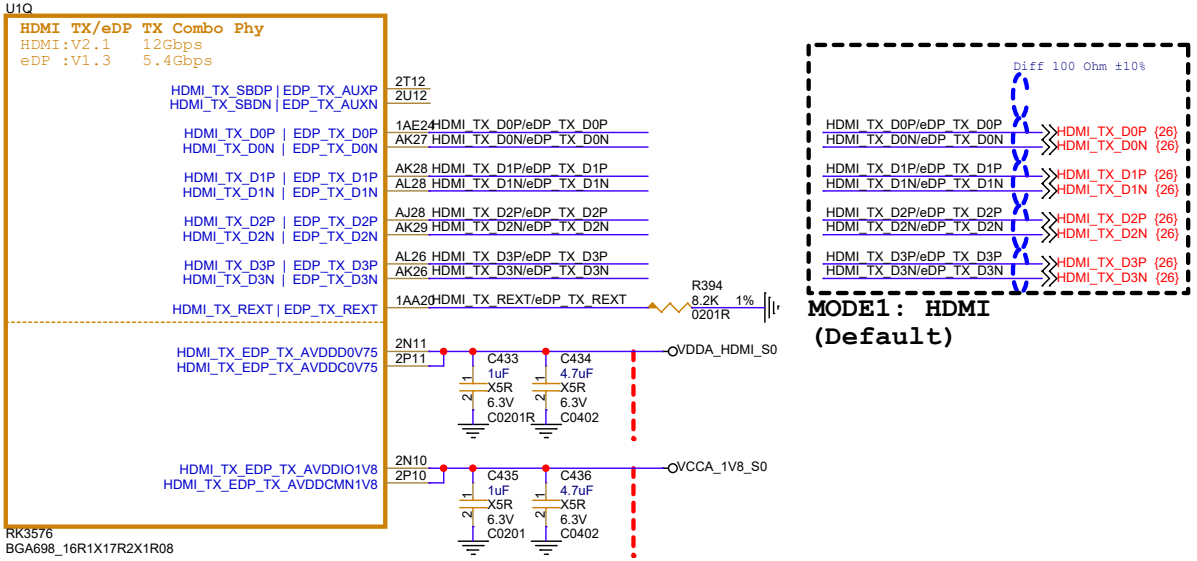
Support MIPI DPHY CSI3: 1/2/4Lane
Support MIPI DPHY CSI4: 1/2Lane
Support MIPI DPHY CSI3 2Lane + MIPI DPHY CSI4 2Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Bit-Brick Co.,Ltd			
K1_DVP_BOARD			
Size C	Document Number: CPU MIPI		Rev: V1.0
Date: Wednesday, March 05, 2025			Sheet 14 of 35

RK3576_Q(HDMI/eDP)

Note:
HDMI 2.1 supports up to 4Kx2K@120Hz

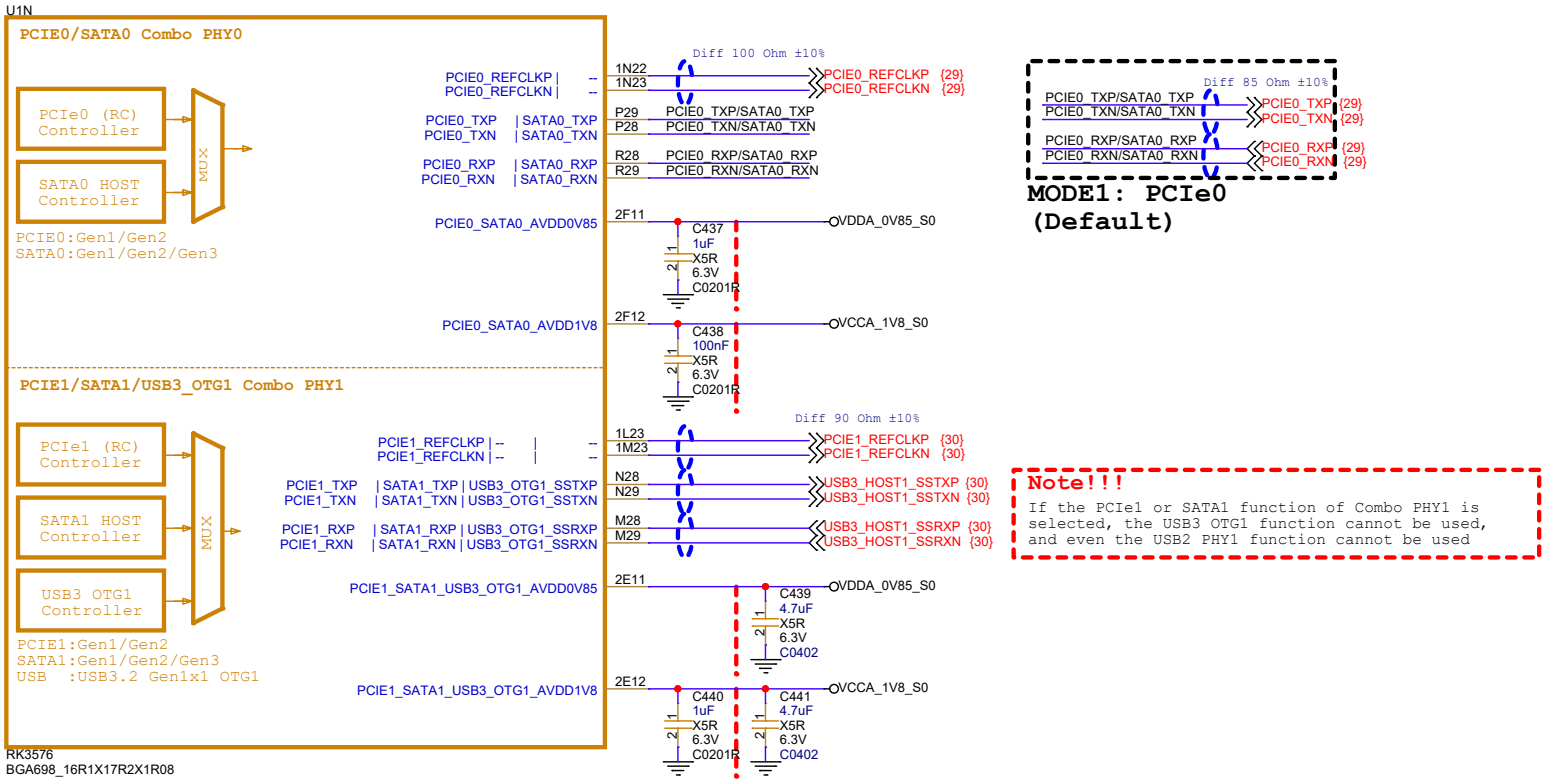


MODE1: HDMI (Default)

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Bit-Brick Co.,Ltd			
K1_DVP_BOARD			
Size B	Document Number: CPU HMDI&eDP		Rev: V1.0
Date:	Wednesday, March 05, 2025		Sheet 15 of 35

RK3576_N(PCIe/SATA/USB3)



MODE1: PCIe0 (Default)

Note!!!

If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG1 function cannot be used, and even the USB2 PHY1 function cannot be used

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

Bit-Brick Co.,Ltd		
K1_DVP_BOARD		
Size B	Document Number: CPU PCIE	Rev: V1.0
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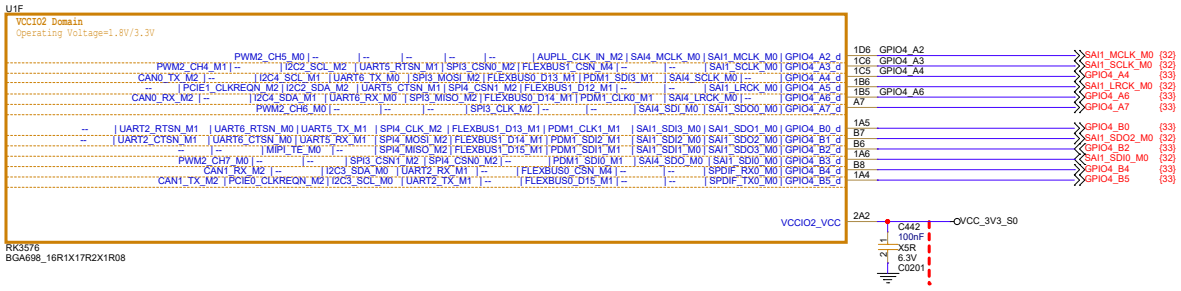
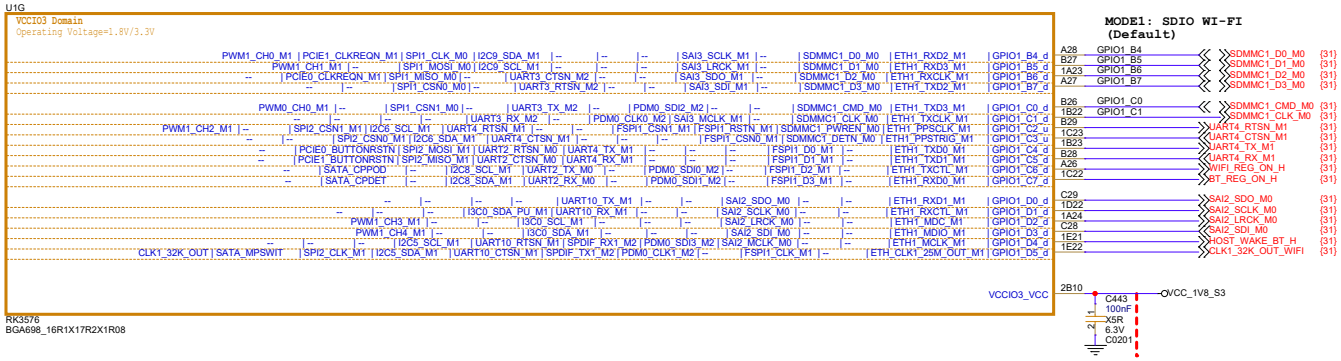
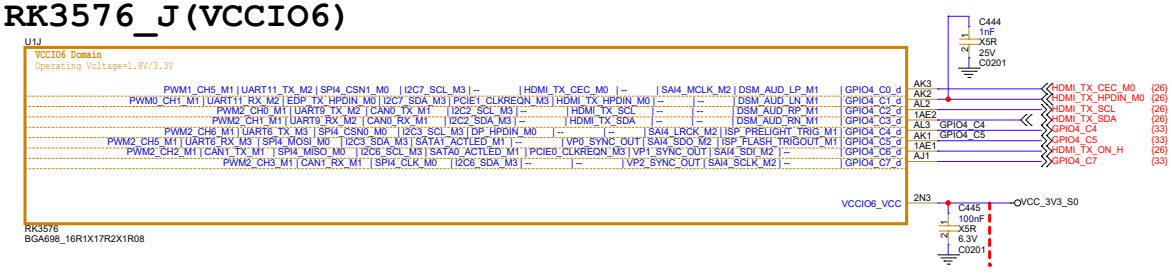
RK3576_F(VCCIO2)



RK3576_G(VCCIO3)



RK3576_J(VCCIO6)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Bit-Brick Co.,Ltd		
K1_DVP_BOARD		
Size C	Document Number: CPU GPIO236	Rev: V1.0
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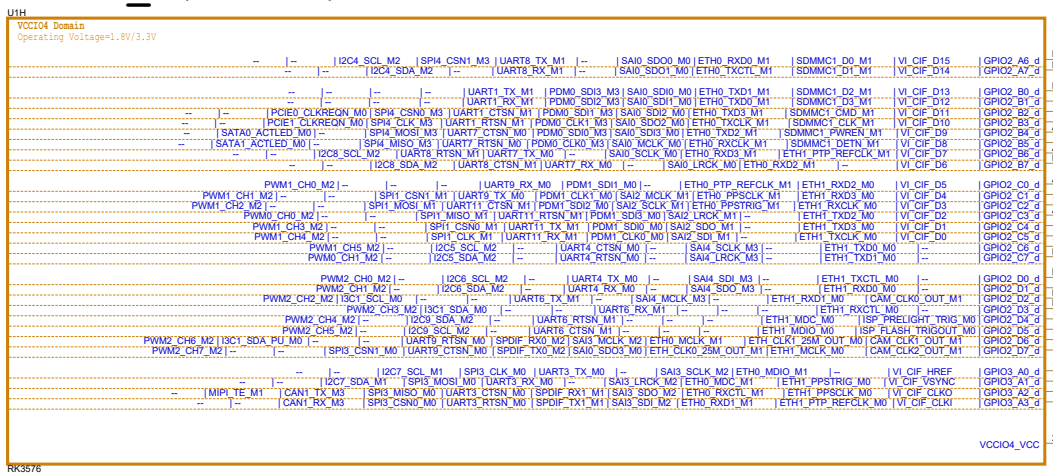
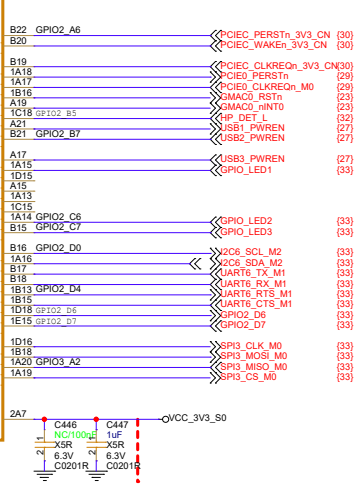
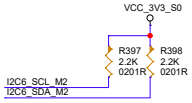
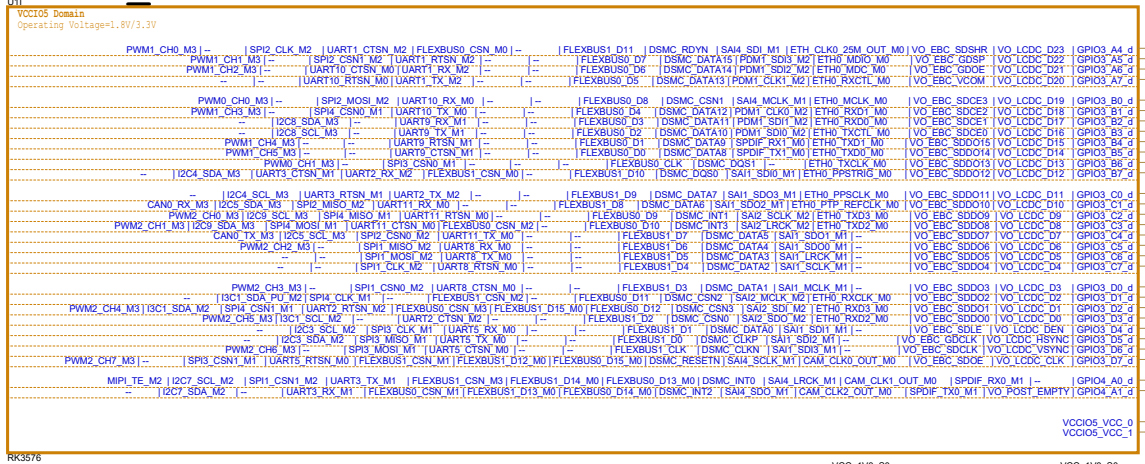
RK3576_H(VCCIO4)



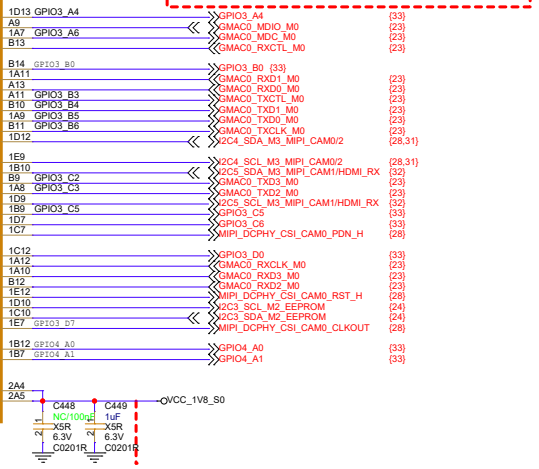


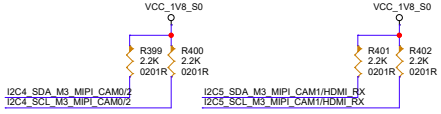


RK3576_I(VCCIO5)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package





Bit-Brick Co.,Ltd	
K1_DVP_BOARD	
Size C	Document Number: CPU GPIO45 Rev: V1.0
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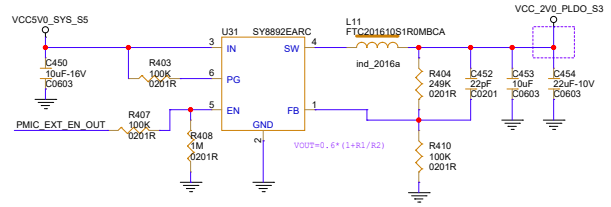
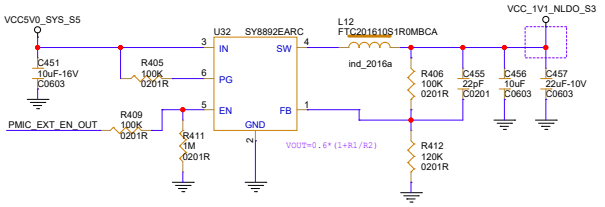
VCC_2V0_PLDO_S3



{20} PMIC_EXT_EN_OUT

{10,20} PMIC_PWR_CTRL2

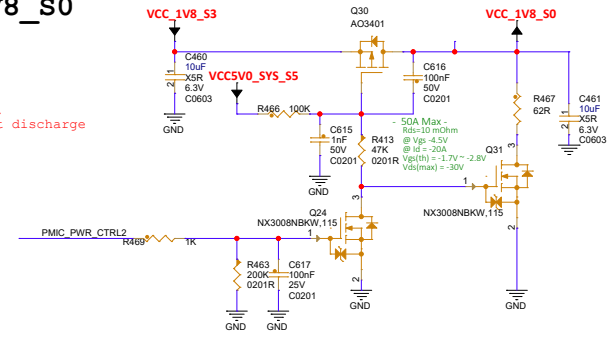
VCC_1V1_NLDO_S3



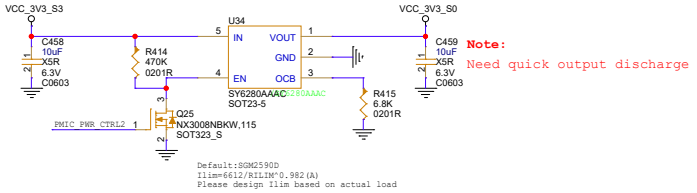
VCC_1V8_S0

Note:
1.8V Load switch.
Need quick output discharge

M.2 PWR



VCC_3V3_S0



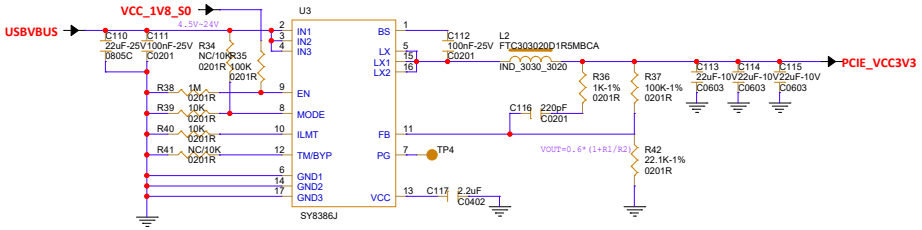
Note:
Need quick output discharge

Audio Power

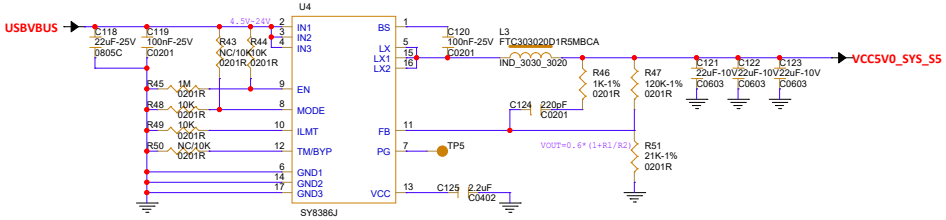
Note:
The voltage of VCCIO_CODEC is consistent with the voltage of VCCIO2

PCIE_VCC3V3

USBVBUS → VCC5V0_SYS



VCC5V0_SYS_S5



WIFI/BT Power

Bit-Brick Co.,Ltd			
K1_DVP_BOARD			
Size C	Document Number: EXT POWER		Rev: V1.0
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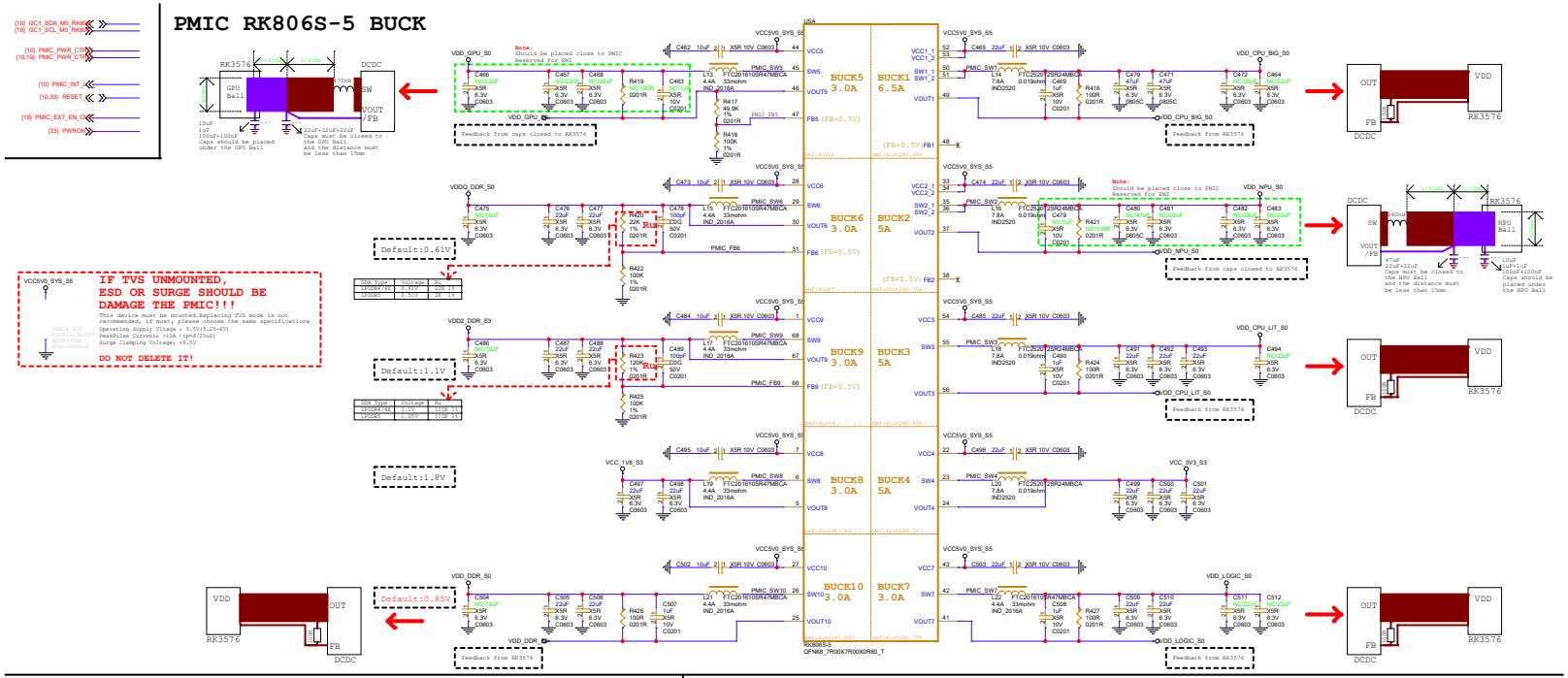
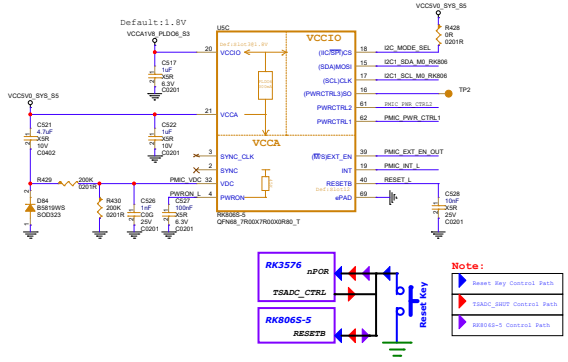
PMIC RK806S-5 BUCK

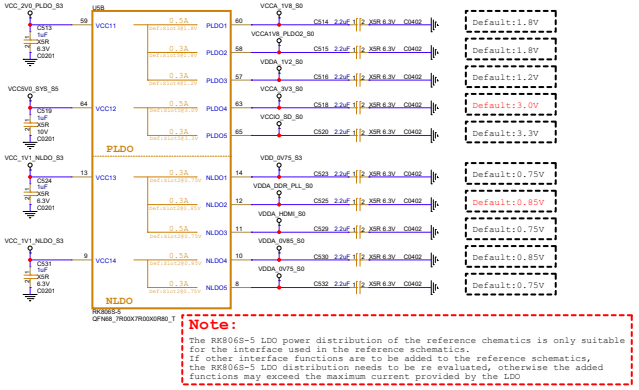


PMIC RK806S-5 Managerment

Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



PMIC RK806S-5 LDO



Note:
The RK806S-5 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

RK-Stick Co. Ltd			
K1_DVP_BOARD			
Size: D	Document Number: PMIC RK806S		Rev: V1.0
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LPDDR4/4X

{11} LPDDR4_DQ0_A
{11} LPDDR4_DQ1_A
{11} LPDDR4_DQ2_A
{11} LPDDR4_DQ3_A
{11} LPDDR4_DQ4_A
{11} LPDDR4_DQ5_A
{11} LPDDR4_DQ6_A
{11} LPDDR4_DQ7_A

{11} LPDDR4_DQS0P_A
{11} LPDDR4_DQS0N_A

{11} LPDDR4_DMI0_A

{11} LPDDR4_DQ8_A
{11} LPDDR4_DQ9_A
{11} LPDDR4_DQ10_A
{11} LPDDR4_DQ11_A
{11} LPDDR4_DQ12_A
{11} LPDDR4_DQ13_A
{11} LPDDR4_DQ14_A
{11} LPDDR4_DQ15_A

{11} LPDDR4_DQS1P_A
{11} LPDDR4_DQS1N_A

{11} LPDDR4_DMI1_A

{11} LPDDR4_A0_A
{11} LPDDR4_A1_A
{11} LPDDR4_A2_A
{11} LPDDR4_A3_A
{11} LPDDR4_A4_A
{11} LPDDR4_A5_A

{11} LPDDR4_CLKP_A
{11} LPDDR4_CLKN_A

{11} LPDDR4_CSN0_A
{11} LPDDR4_CSN1_A

{11} LPDDR4_CKE0_A
{11} LPDDR4_CKE1_A

{11} LPDDR4_RESET

{11} LPDDR4_DQ0_B
{11} LPDDR4_DQ1_B
{11} LPDDR4_DQ2_B
{11} LPDDR4_DQ3_B
{11} LPDDR4_DQ4_B
{11} LPDDR4_DQ5_B
{11} LPDDR4_DQ6_B
{11} LPDDR4_DQ7_B

{11} LPDDR4_DQS0P_B
{11} LPDDR4_DQS0N_B

{11} LPDDR4_DMI0_B

{11} LPDDR4_DQ8_B
{11} LPDDR4_DQ9_B
{11} LPDDR4_DQ10_B
{11} LPDDR4_DQ11_B
{11} LPDDR4_DQ12_B
{11} LPDDR4_DQ13_B
{11} LPDDR4_DQ14_B
{11} LPDDR4_DQ15_B

{11} LPDDR4_DQS1P_B
{11} LPDDR4_DQS1N_B

{11} LPDDR4_DMI1_B

{11} LPDDR4_A0_B
{11} LPDDR4_A1_B
{11} LPDDR4_A2_B
{11} LPDDR4_A3_B
{11} LPDDR4_A4_B
{11} LPDDR4_A5_B

{11} LPDDR4_CLKP_B
{11} LPDDR4_CLKN_B

{11} LPDDR4_CSN0_B
{11} LPDDR4_CSN1_B

{11} LPDDR4_CKE0_B
{11} LPDDR4_CKE1_B

U6A

CH A / CH B

LPDDR4_DQ0_A	B2	DQ0_A	DQ0_B	AA2	LPDDR4_DQ0_B
LPDDR4_DQ1_A	C2	DQ1_A	DQ1_B	Y2	LPDDR4_DQ1_B
LPDDR4_DQ2_A	E2	DQ2_A	DQ2_B	V2	LPDDR4_DQ2_B
LPDDR4_DQ3_A	F2	DQ3_A	DQ3_B	U2	LPDDR4_DQ3_B
LPDDR4_DQ4_A	F4	DQ4_A	DQ4_B	U4	LPDDR4_DQ4_B
LPDDR4_DQ5_A	E4	DQ5_A	DQ5_B	V4	LPDDR4_DQ5_B
LPDDR4_DQ6_A	C4	DQ6_A	DQ6_B	Y4	LPDDR4_DQ6_B
LPDDR4_DQ7_A	B4	DQ7_A	DQ7_B	AA4	LPDDR4_DQ7_B
LPDDR4_DQS0P_A	D3	DQS0_T_A	DQS0_T_B	W3	LPDDR4_DQS0P_B
LPDDR4_DQS0N_A	E3	DQS0_C_A	DQS0_C_B	V3	LPDDR4_DQS0N_B
LPDDR4_DMI0_A	C3	DMI0_A	DMI0_B	Y3	LPDDR4_DMI0_B
LPDDR4_DQ8_A	B11	DQ8_A	DQ8_B	AA11	LPDDR4_DQ8_B
LPDDR4_DQ9_A	C11	DQ9_A	DQ9_B	Y11	LPDDR4_DQ9_B
LPDDR4_DQ10_A	E11	DQ10_A	DQ10_B	V11	LPDDR4_DQ10_B
LPDDR4_DQ11_A	F11	DQ11_A	DQ11_B	U11	LPDDR4_DQ11_B
LPDDR4_DQ12_A	F9	DQ12_A	DQ12_B	U9	LPDDR4_DQ12_B
LPDDR4_DQ13_A	E9	DQ13_A	DQ13_B	V9	LPDDR4_DQ13_B
LPDDR4_DQ14_A	C9	DQ14_A	DQ14_B	Y9	LPDDR4_DQ14_B
LPDDR4_DQ15_A	B9	DQ15_A	DQ15_B	AA9	LPDDR4_DQ15_B
LPDDR4_DQS1P_A	D10	DQS1_T_A	DQS1_T_B	W10	LPDDR4_DQS1P_B
LPDDR4_DQS1N_A	E10	DQS1_C_A	DQS1_C_B	V10	LPDDR4_DQS1N_B
LPDDR4_DMI1_A	C10	DMI1_A	DMI1_B	Y10	LPDDR4_DMI1_B
LPDDR4_A0_A	H2	CA0_A	CA0_B	R2	LPDDR4_A0_B
LPDDR4_A1_A	J2	CA1_A	CA1_B	P2	LPDDR4_A1_B
LPDDR4_A2_A	H9	CA2_A	CA2_B	R9	LPDDR4_A2_B
LPDDR4_A3_A	H10	CA3_A	CA3_B	R10	LPDDR4_A3_B
LPDDR4_A4_A	H11	CA4_A	CA4_B	R11	LPDDR4_A4_B
LPDDR4_A5_A	J11	CA5_A	CA5_B	P11	LPDDR4_A5_B
LPDDR4_CLKP_A	J8	CK_T_A	CK_T_B	P8	LPDDR4_CLKP_B
LPDDR4_CLKN_A	J9	CK_C_A	CK_C_B	P9	LPDDR4_CLKN_B
LPDDR4_CKE0_A	J4	CKE0_A	CKE0_B	P4	LPDDR4_CKE0_B
LPDDR4_CKE1_A	J5	CKE1_A	CKE1_B	P5	LPDDR4_CKE1_B
	K8	CKE2_A_NC	CKE2_B_NC	N8	
LPDDR4_CSN0_A	H4	CS0_A	CS0_B	R4	LPDDR4_CSN0_B
LPDDR4_CSN1_A	H3	CS1_A	CS1_B	R3	LPDDR4_CSN1_B
	K5	CS2_A_NC	CS2_B_NC	N5	
VDD2_DDR_S3	G2	ODT_CA_A	ODT_CA_B	T2	VDD2_DDR_S3
		ZQ0			
VDDQ_DRAM_S0 R431 240R 1% 0201R	A5	ZQ1			
R432 240R 1% 0201R	A8	ZQ2_NC	RESET_n	T11	LPDDR4_RESET
	G11				

C533 NC/1nF X5R 25V C0201

LPDDR4_200P
BGA200_15R00X10R00X0R90

U6B

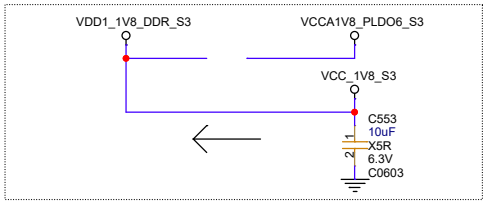
VDD1_1V8_DDR_S3	F1	VDD1_1	VDD1	VSS_1	A3
	F12	VDD1_2		VSS_2	A10
	G4	VDD1_3		VSS_3	C1
	G9	VDD1_4	1.8V	VSS_4	C5
	T4	VDD1_5		VSS_5	C8
	T9	VDD1_6		VSS_6	C12
	U1	VDD1_7		VSS_7	D2
	U12	VDD1_8		VSS_8	D4
				VSS_9	D9
VDD2_DDR_S3	A4	VDD2_1	VDD2	VSS_10	D11
	A9	VDD2_2		VSS_11	E1
	F5	VDD2_3		VSS_12	E5
	F8	VDD2_4	1.1V	VSS_13	E8
	H1	VDD2_5		VSS_14	E12
	H5	VDD2_6		VSS_15	G1
	H8	VDD2_7		VSS_16	G3
	H12	VDD2_8		VSS_17	G5
	K1	VDD2_9		VSS_18	G8
	K3	VDD2_10		VSS_19	G10
	K10	VDD2_11		VSS_20	G12
	K12	VDD2_12		VSS_21	J1
	N1	VDD2_13		VSS_22	J3
	N3	VDD2_14		VSS_23	J10
	N10	VDD2_15		VSS_24	J12
	N12	VDD2_16		VSS_25	K2
	R1	VDD2_17		VSS_26	K4
	R5	VDD2_18		VSS_27	K9
	R8	VDD2_19		VSS_28	K11
	R12	VDD2_20		VSS_29	N2
	U5	VDD2_21		VSS_30	N4
	U8	VDD2_22		VSS_31	N9
	AB4	VDD2_23		VSS_32	N11
	AB9	VDD2_24		VSS_33	P1
				VSS_34	P3
VDDQ_DRAM_S0	B3	VDDQ_1	VDDQ	VSS_35	P10
	B5	VDDQ_2		VSS_36	P12
	B8	VDDQ_3		VSS_37	T1
	B10	VDDQ_4	LP4	VSS_38	T3
	D1	VDDQ_5	1.1V	VSS_39	T5
	D5	VDDQ_6		VSS_40	T8
	D8	VDDQ_7		VSS_41	T10
	D12	VDDQ_8		VSS_42	T12
	F3	VDDQ_9	LP4x	VSS_43	V1
	F10	VDDQ_10	0.6V	VSS_44	V5
	U3	VDDQ_11		VSS_45	V8
	U10	VDDQ_12		VSS_46	V12
	W1	VDDQ_13		VSS_47	W2
	W5	VDDQ_14		VSS_48	W4
	W8	VDDQ_15		VSS_49	W9
	W12	VDDQ_16		VSS_50	W11
	AA3	VDDQ_17		VSS_51	Y1
	AA5	VDDQ_18		VSS_52	Y5
	AA8	VDDQ_19		VSS_53	Y8
	AA10	VDDQ_20		VSS_54	Y12
				VSS_55	AB3
				VSS_56	AB5
				VSS_57	AB8
				VSS_58	AB10
	A1	DNU_1		DNU_7	AA1
	A2	DNU_2		DNU_8	AA12
	A11	DNU_3		DNU_9	AB1
	A12	DNU_4		DNU_10	AB2
	B1	DNU_5		DNU_11	AB11
	B12	DNU_6		DNU_12	AB12

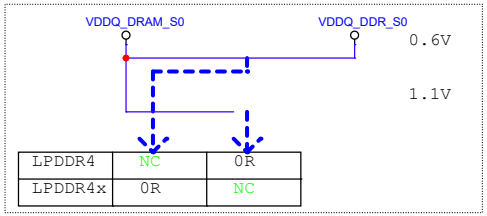
LPDDR4_200P
BGA200_15R00X10R00X0R90

Note:

Sequence:VDD1-VDD2-VDDQ

	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65





LPDDR4	NC	0R
LPDDR4x	0R	NC

VDDQ_DDR_CKE_S3
VDD2_DDR_S3

VDDQ_DRAM_S0

C534 22uF X5R 6.3V C0603
C535 10uF X5R 6.3V C0603
C536 10uF X5R 6.3V C0603
C537 1uF X5R 6.3V C0201
C538 1uF X5R 6.3V C0201
C539 100nF X5R 6.3V C0201
C540 100nF X5R 6.3V C0201
C541 100nF X5R 6.3V C0201
C542 100nF X5R 6.3V C0201
C543 100nF X5R 6.3V C0201
C544 100nF X5R 6.3V C0201
C545 100nF X5R 6.3V C0201
C546 100nF X5R 6.3V C0201
C547 100nF X5R 6.3V C0201
C548 100nF X5R 6.3V C0201
C549 100nF X5R 6.3V C0201
C550 100nF X5R 6.3V C0201
C551 100nF X5R 6.3V C0201
C552 100nF X5R 6.3V C0201

VDD2_DDR_S3

C554 22uF X5R 6.3V C0603
C555 10uF X5R 6.3V C0603
C556 10uF X5R 6.3V C0603
C557 1uF X5R 6.3V C0201
C558 1uF X5R 6.3V C0201
C559 100nF X5R 6.3V C0201
C560 100nF X5R 6.3V C0201
C561 100nF X5R 6.3V C0201
C562 100nF X5R 6.3V C0201
C563 100nF X5R 6.3V C0201
C564 100nF X5R 6.3V C0201
C565 100nF X5R 6.3V C0201
C566 100nF X5R 6.3V C0201
C567 100nF X5R 6.3V C0201
C568 100nF X5R 6.3V C0201

VDD1_1V8_DDR_S3

C569 10uF X5R 6.3V C0603
C570 100nF X5R 6.3V C0201
C571 100nF X5R 6.3V C0201
C572 100nF X5R 6.3V C0201
C573 100nF X5R 6.3V C0201
C574 100nF X5R 6.3V C0201
C575 100nF X5R 6.3V C0201
C576 100nF X5R 6.3V C0201
C577 100nF X5R 6.3V C0201

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K1_DVP_BOARD

Size A3	Document Number: LPDDR4X		Rev: V1.0
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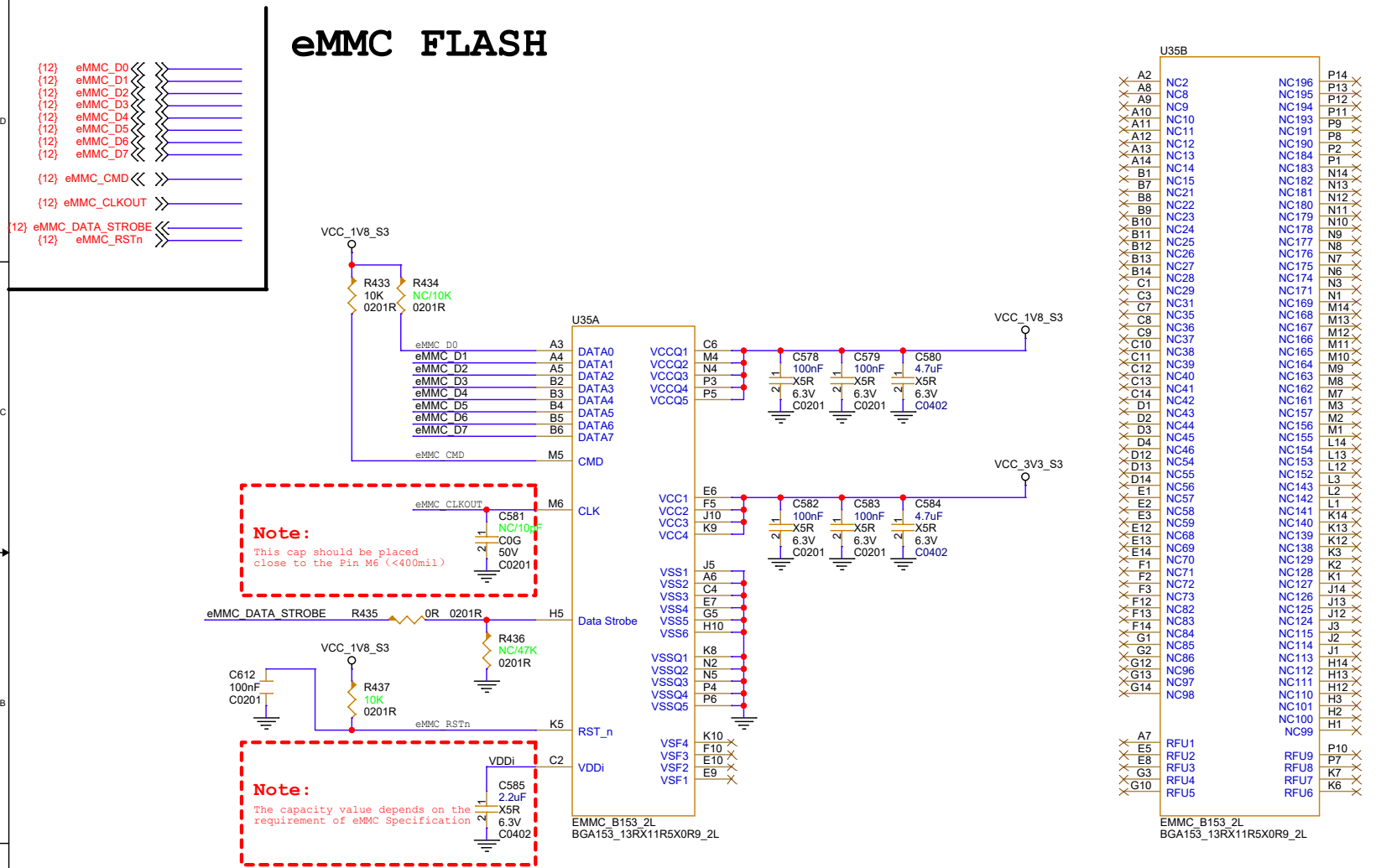
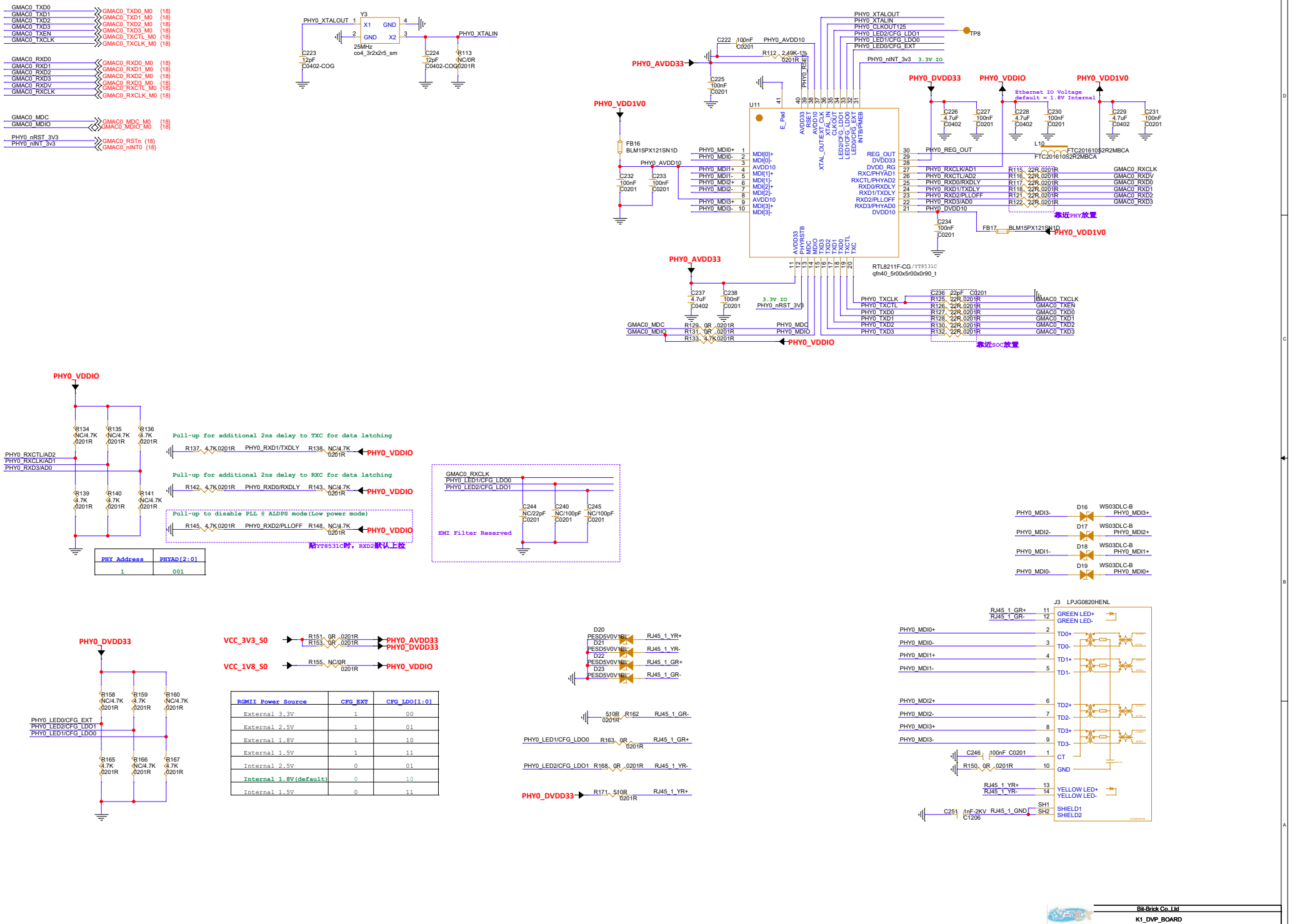
eMMC FLASH



Bit-Brick Co.,Ltd		
K1_DVP_BOARD		
Size B	Document Number: eMMC	Rev: V1.0
Date: Wednesday, March 05, 2025		Sheet 22 of 35

GMAC Ethernet0



PHY Address	PHYAD[2:0]
1	001

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1	00
External 2.5V	1	01
External 1.8V	1	10
External 1.5V	1	11
Internal 2.5V	0	01
Internal 1.8V(default)	0	10
Internal 1.5V	0	11

Bit-Brick Co.,Ltd	
K1_DVP_BOARD	
Size C	Document Number: ETHERNET GMAC0
Rev: V1.0	
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{18} I2C3_SCL_M2_EEPROM
{18} I2C3_SDA_M2_EEPROM
EEPROM_SCL
EEPROM_SDA

EEPROM

read: i2c addr=10100001
write: i2c addr=10100000

U7
EEPROM_SCL 1 SCL
EEPROM_SDA 2 GND
3 SDA
WP 5
VCC 4
GT24C02B-2TFLI-TR

TP6
R69 10K/NC 0201R
VCC_1V8_S0
C212 1uF C0201

VCC_1V8_S0
R70 4.7K 0201R
R71 4.7K 0201R
EEPROM_SCL
EEPROM_SDA

Micro SD Connector

VCC3V3_SD_S0
C210 4.7uF C0402
C211 100nF C0201
PESD5V0V1BL

TP7

{12} SDMMC0_D2
{12} SDMMC0_D3
{12} SDMMC0_CMD
{12} SDMMC0_CLK
{12} SDMMC0_D0
{12} SDMMC0_D1
{10} SDMMC0_DET_L

PESD5V0V1BL D2
PESD5V0V1BL D3
PESD5V0V1BL D4
PESD5V0V1BL D5
PESD5V0V1BL D6
PESD5V0V1BL D7
PESD5V0V1BL D8

J8
1 DATA2
2 CD/DATA3
3 CMD
4 VDD
5 CLK
6 VSS
7 DATA0
8 DATA1
9 CD
10 G1
11 G2
12 G3
13 G4
14 G5
1040310811

VCC_3V3_S3
VCC3V3_SD_S0
{10} SDMMC0_PWREN_H
U36
2A
5 IN
4 EN
GND 2
OUT 1 2A
ISET 3
MT9700
SOT23-5
C587 1uF C0201
R438 100K 0201R
R439 3.4K-1% 0201R
C586 1uF C0201
Ilim (A)=6800/Rset (ohm)

Bit-Brick Co.,Ltd			
K1_DVP_BOARD			
Size A3	Document Number: TF FLASH EEPROM		Rev: V1.0
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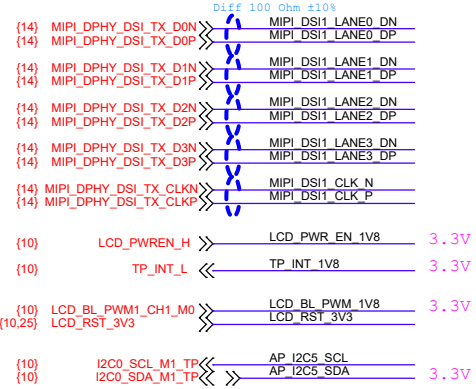
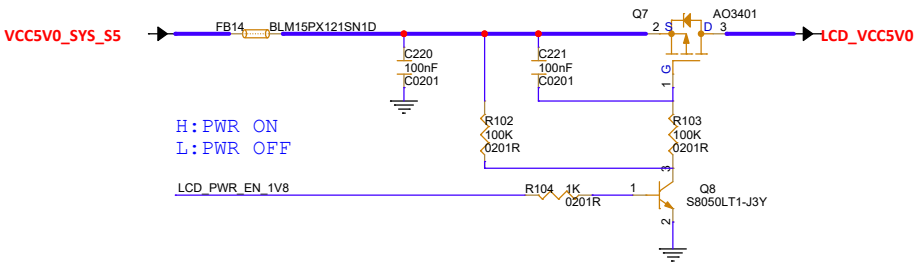
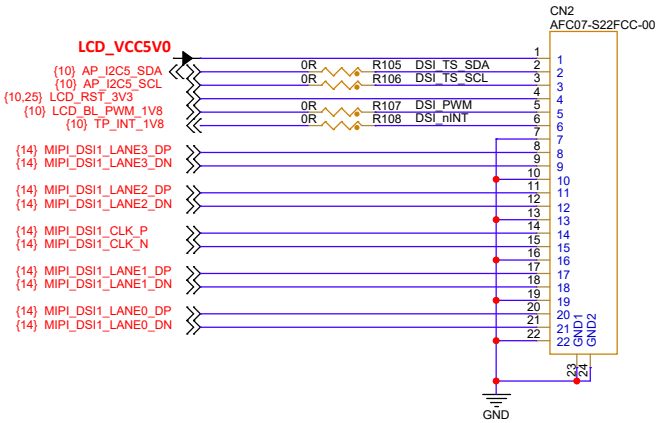
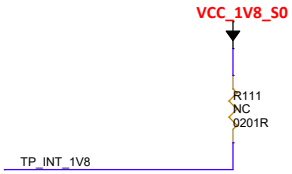
MIPI-DSI



DSI Display







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K1_DVP_BOARD			
Size A3	Document Number: DSI		Rev: V1.0
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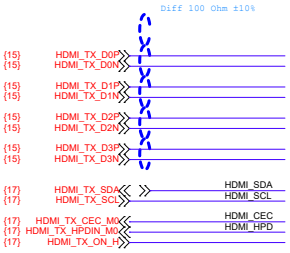
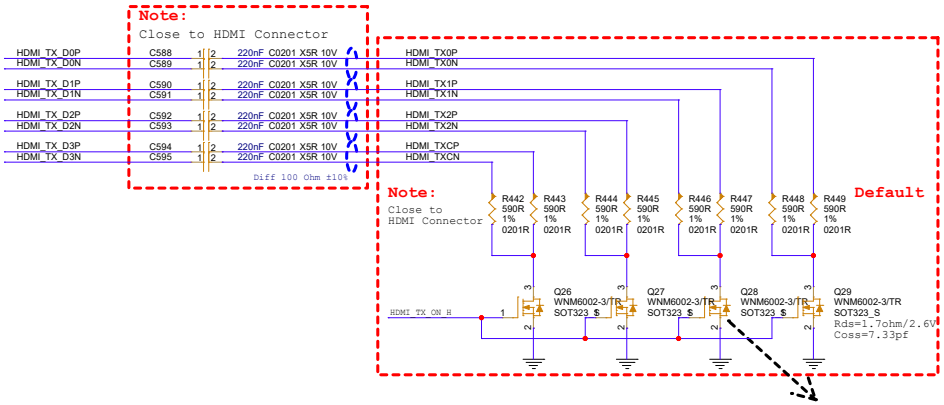
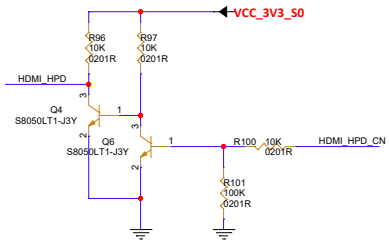
HDMI



HDMI 2.1 Support video output up to 4Kx2K@120Hz

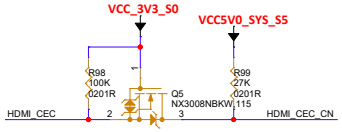


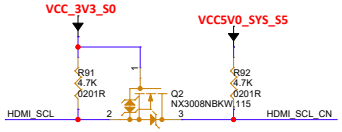


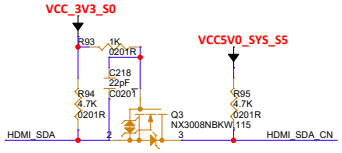
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

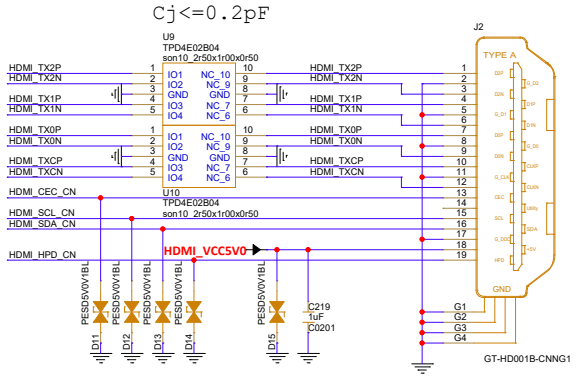
Note:
The controller only support AC coupled link.
In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.









Bit-Brick Co.,Ltd			
K1_DVP_BOARD			
Size C	Document Number: HDMI		Rev: V1.0
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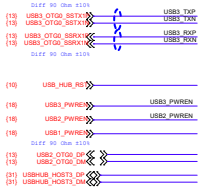
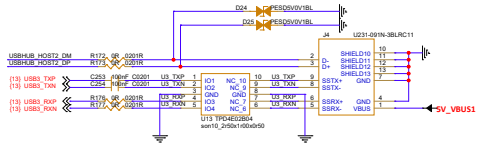
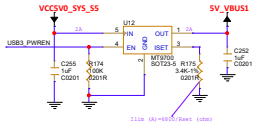
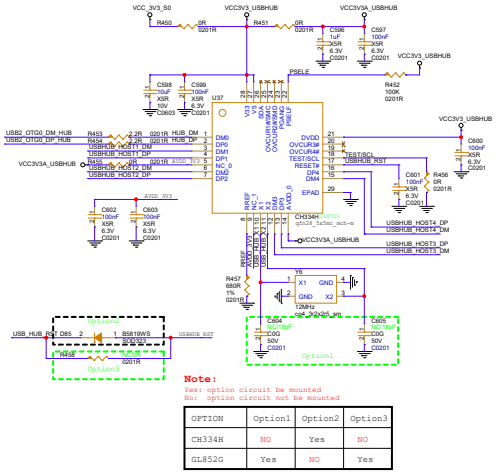


USB3.0 TYPEA



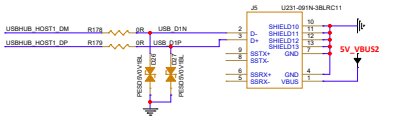


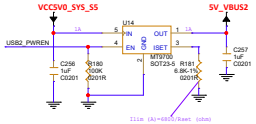
USB20_HUB+USB3.0 HOST



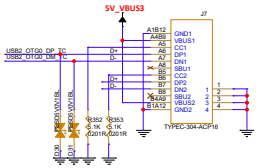
OPTION	Option1	Option2	Option3
CH334H	NO	Yes	NO
GL852G	Yes	NO	Yes

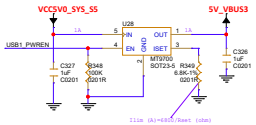
USB2.0 TYPEA-HOST



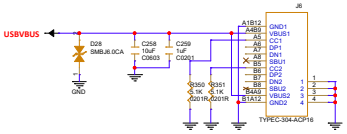


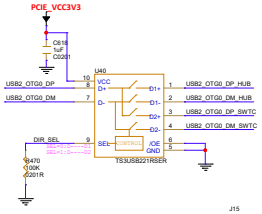
DOWNLOAD TYPEC

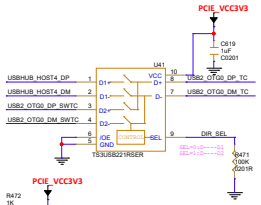


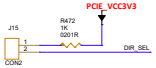


TYPEC POWER









BitBrick Co. Ltd			
K1_DVP_BOARD			
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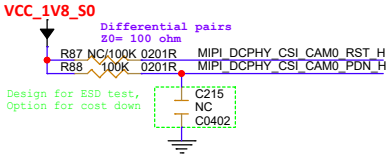
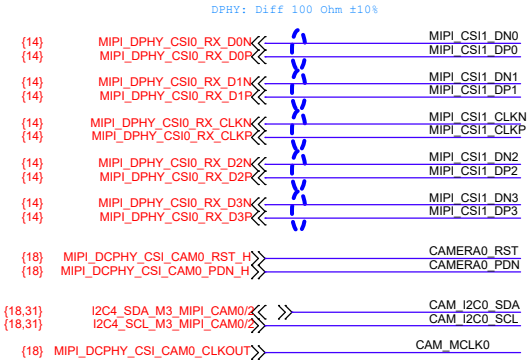
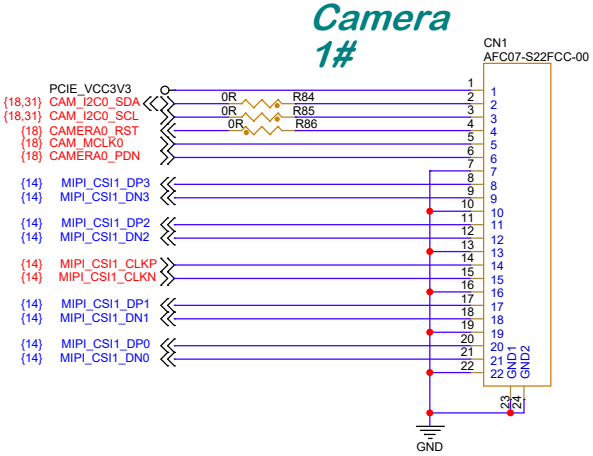
CAMERA

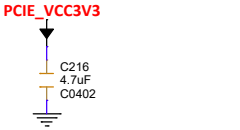


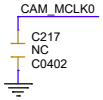




		信号	时钟	I2C	RST&PDN
4+2+2	CSI1	MIPI_CSI1_D0 MIPI_CSI1_D1 MIPI_CSI1_D2 MIPI_CSI1_D3	CAM_MCLK0 MIPI_CSI1_CLK	CAM_I2C0	CAMERA0_PDN CAMERA0_RST
	CSI2	MIPI_CSI3_D2 MIPI_CSI3_D3	CAM_MCLK1 MIPI_CSI2_CLK	CAM_I2C1	CAMERA1_PDN CAMERA1_RST
	CSI3	MIPI_CSI3_D0 MIPI_CSI3_D1	CAM_MCLK2 MIPI_CSI3_CLK	CAM_I2C2	CAMERA2_PDN CAMERA2_RST

		信号线		I2C	RST&PDN
4+4	CSI1	MIPI_CSI1_D0 MIPI_CSI1_D1 MIPI_CSI1_D2 MIPI_CSI1_D3	CAM_MCLK0 MIPI_CSI1_CLK	CAM_I2C0	CAMERA0_PDN CAMERA0_RST
	CSI2	MIPI_CSI3_D0 MIPI_CSI3_D1 MIPI_CSI3_D2 MIPI_CSI3_D3	CAM_MCLK1 MIPI_CSI3CLK	CAM_I2C1	CAMERA1_PDN CAMERA1_RST





NOTE:

1.The working voltage and current of power need determine according to the peripheral specification.

2.AFVCC-CSI has timing requirements, don't share the same power with DOVDD-CSI.

3.The front and rear cameras need to consider the compatibility of DVDD-CSI voltage.

Bit-Brick Co.,Ltd			
K1_DVP_BOARD			
Size A3	Document Number: CSI		Rev: V1.0
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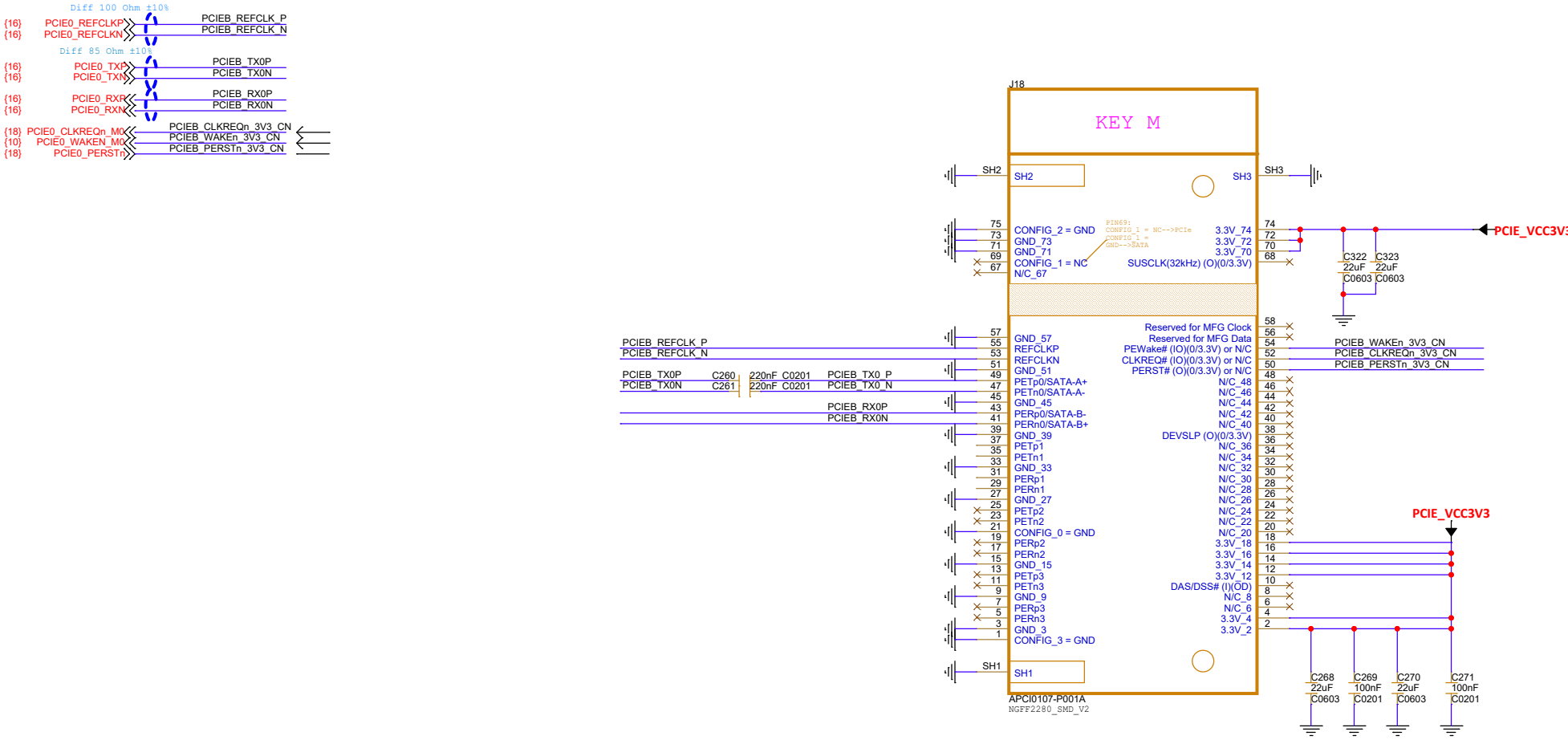
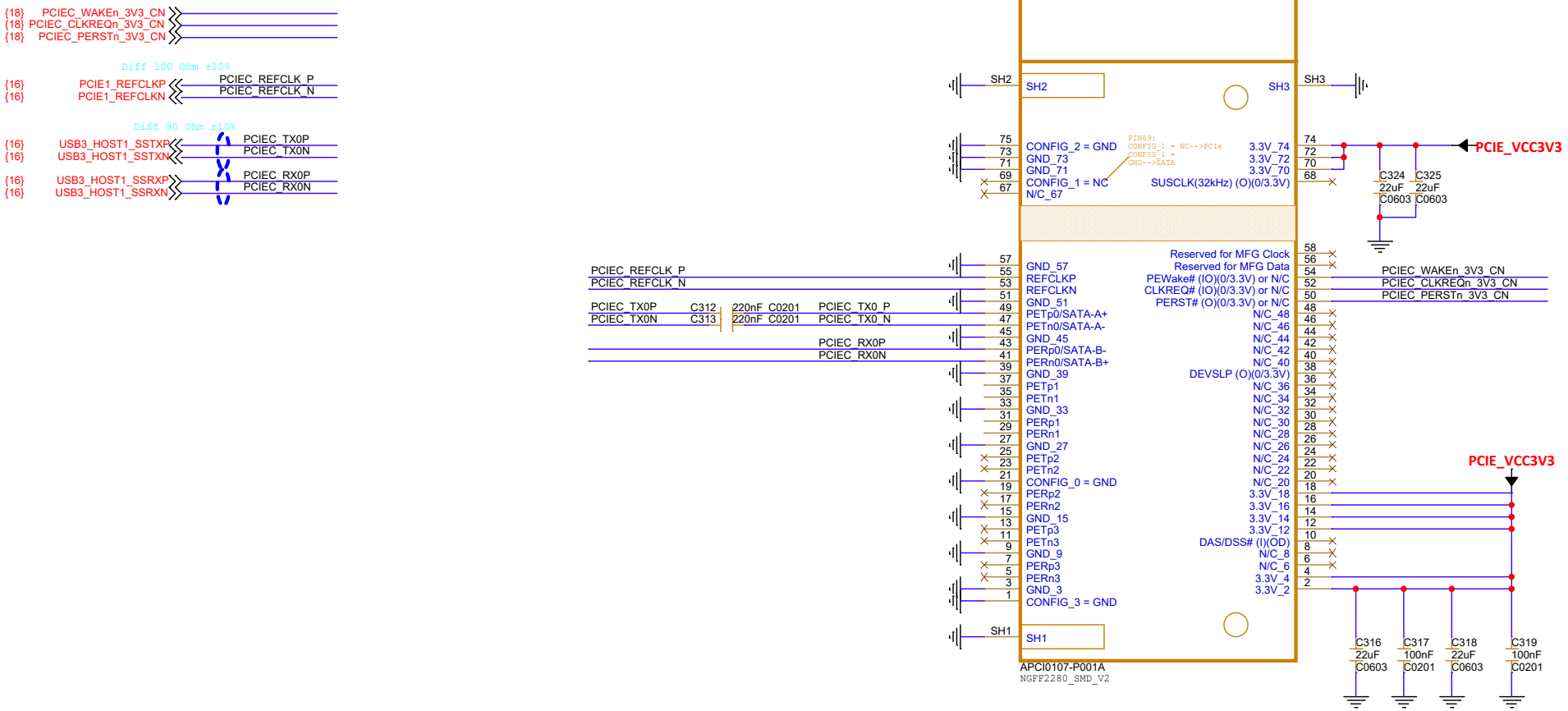
PCIEB



Bit-Brick Co.,Ltd			
K1_DVP_BOARD			
Size A3	Document Number: PCIEB M.2 KEY M		Rev: V1.0
Date: Wednesday, March 05, 2025			Sheet 29 of 35

PCIE1



Bit-Brick Co.,Ltd		
K1_DVP_BOARD		
Size B	Document Number: PCIEC M.2 KEY M	Rev: V1.0
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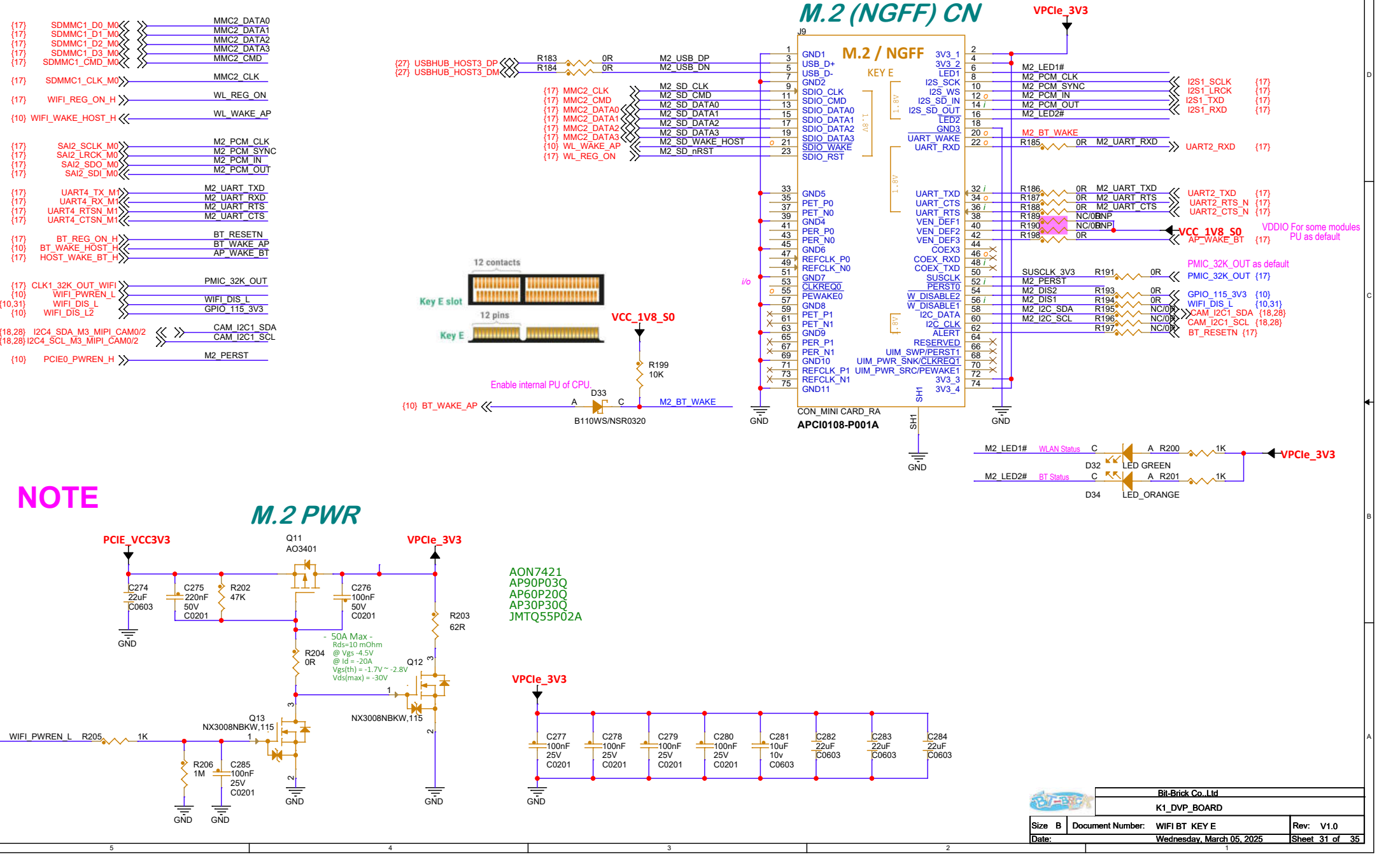

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K1_DVP_BOARD		
Size B	Document Number: WIFI BT KEY E	Rev: V1.0
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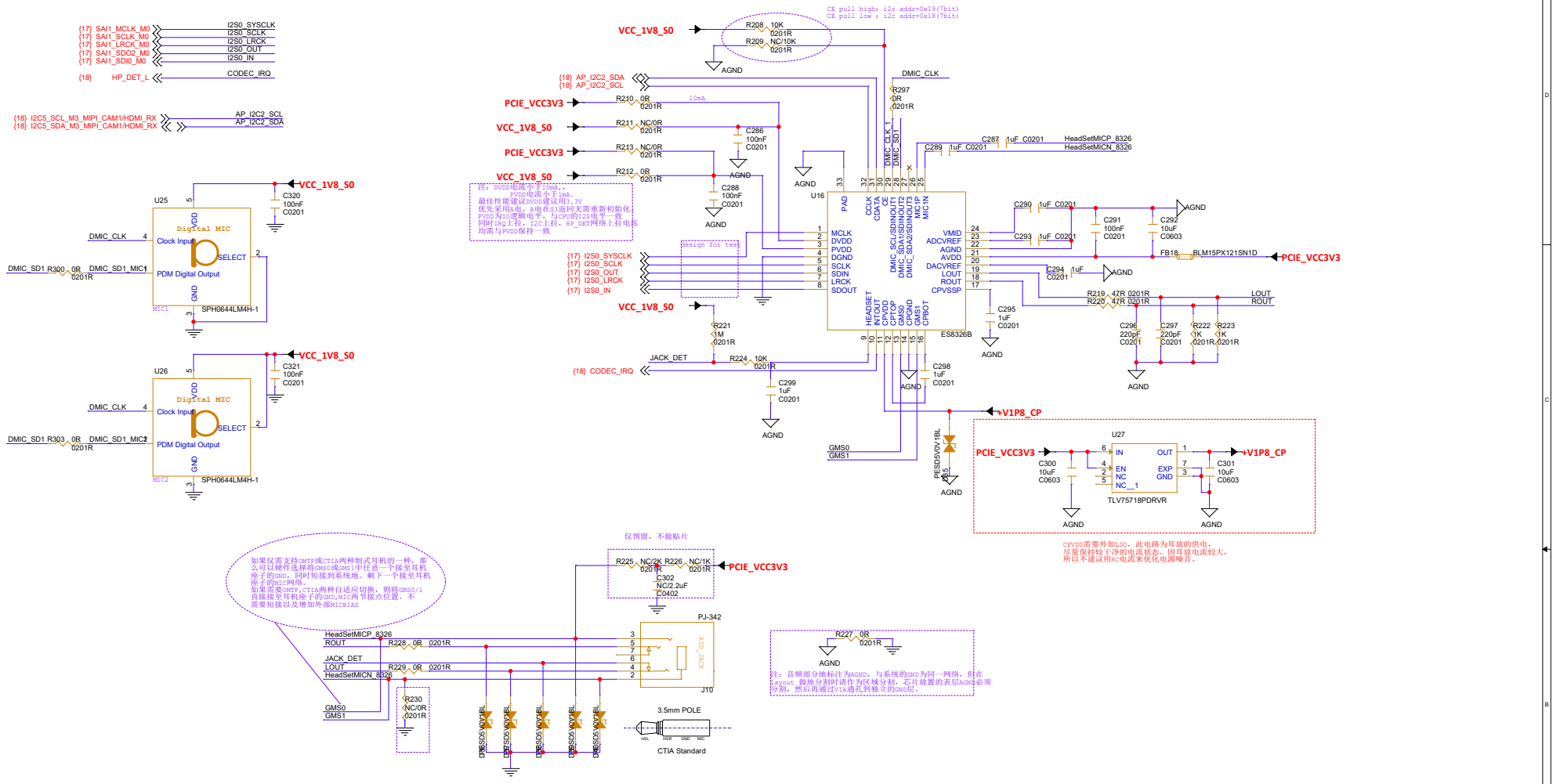
Audio Codec



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K1_DVP_BOARD			
Size C	Document Number: AUDIO ES8326B		Rev: V1.0
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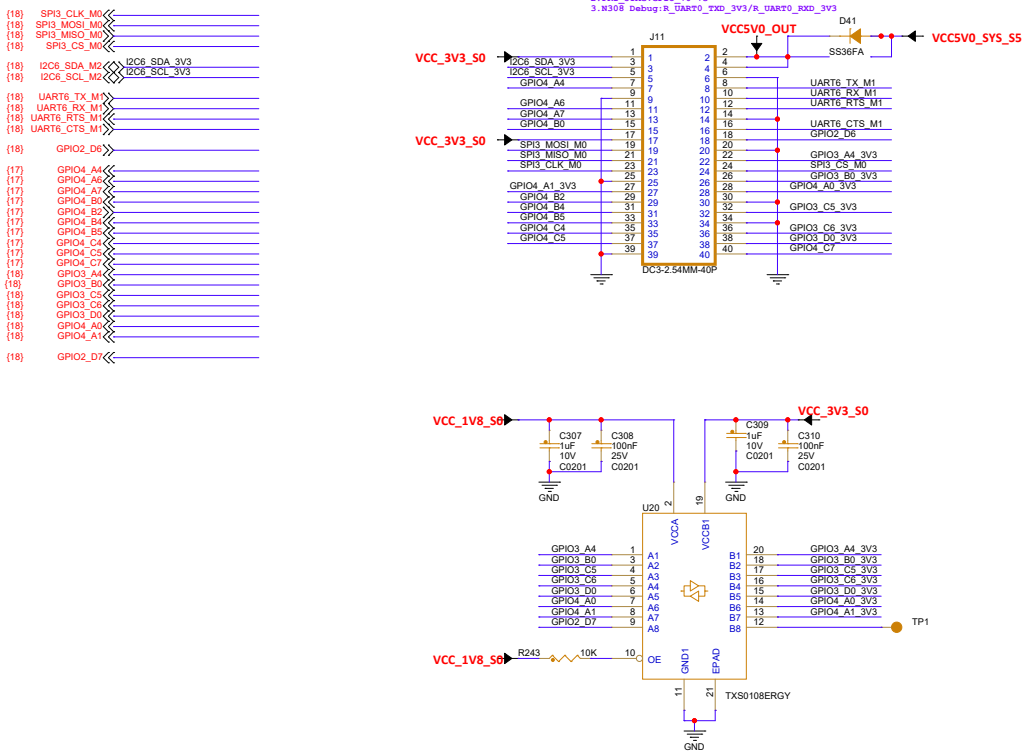
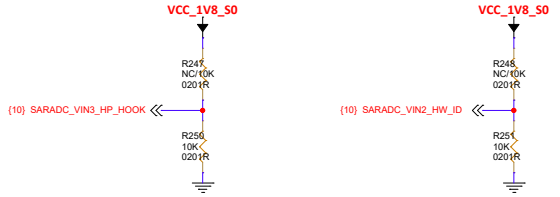
40 pin GPIO

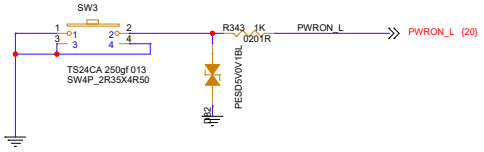
1.SPI_LCD:GPIO_70~74+GPIO_91+GPIO_92
2.PRI_JTAG:GPIO_70~73
3.N308 Debug:R_UART0_TXD_3V3/R_UART0_RXD_3V3



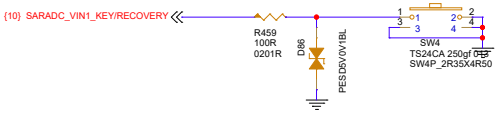
ADC



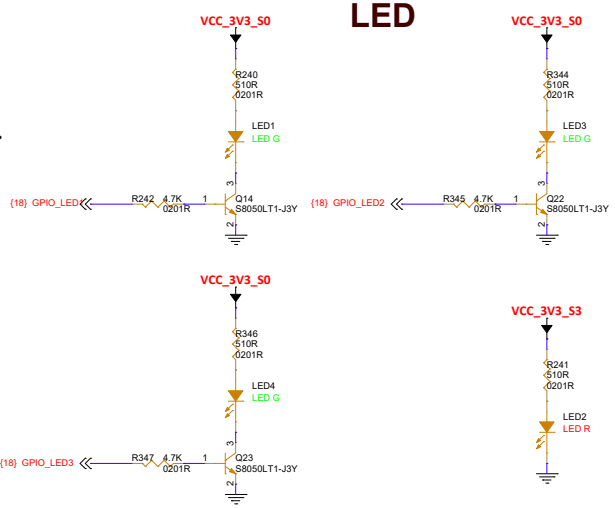
PowerON



V+/RECOVERY_Key

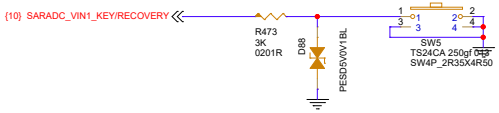


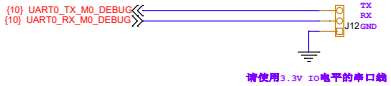
LED



REST

V-_Key





请使用3.3V IO电平的串口线

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K1_DVP_BOARD			
Size C	Document Number: EXT GPIO KEY LED		Rev: V1.0
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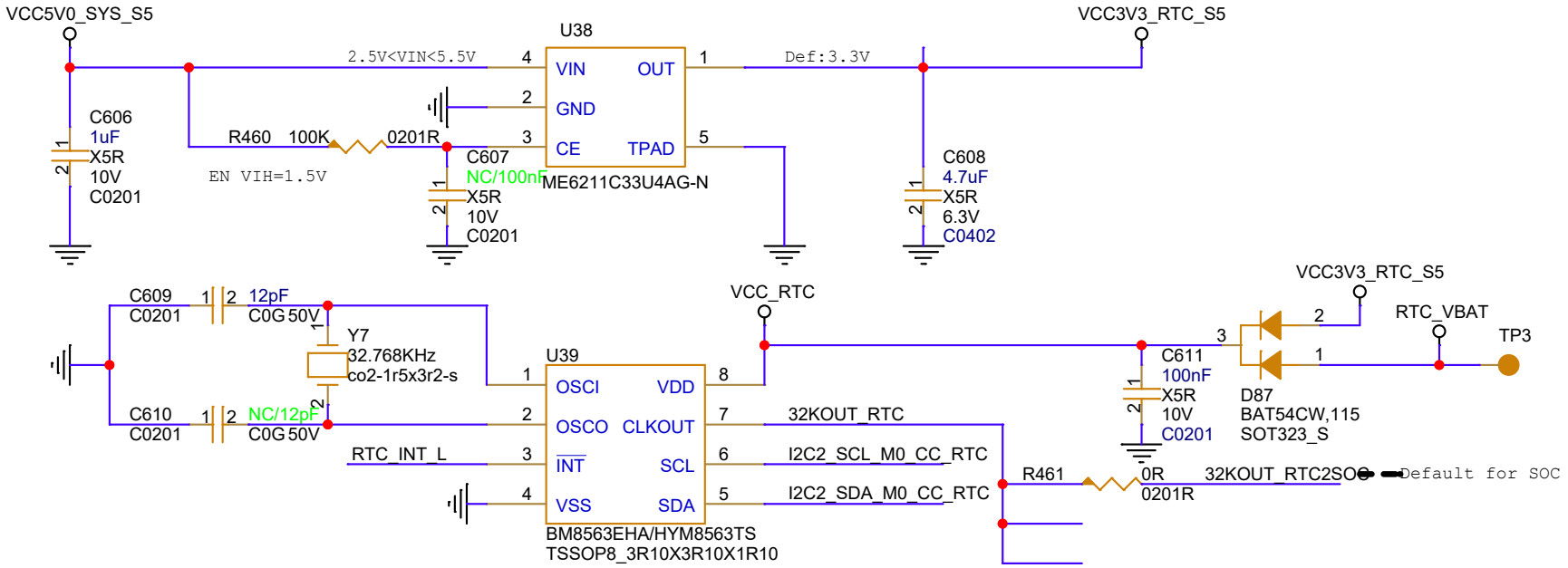
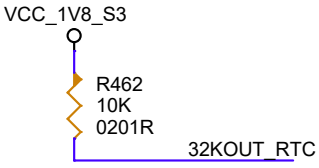
RTC

{10} I2C2_SCL_M0_CC_RTC
{10} I2C2_SDA_M0_CC_RTC
{10} RTC_INT_L
{10} 32KOUT_RTC2SOC





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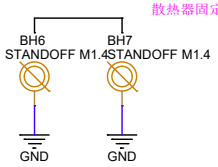
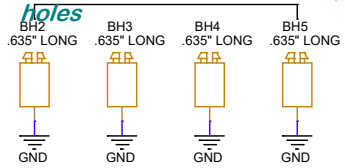
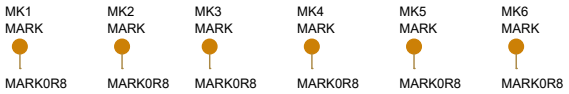
散热器固定孔



Base board screw holes

PCB四个角固定孔





Bit-Brick Co.,Ltd		
K1_DVP_BOARD		
Size B	Document Number: MECHANICAL	Rev: V1.0
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