

Fusion-Core ISA Definition: Revision 0.1

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1 Changelog

Version 0.1 Initial Definition of the Instruction Set Architecture

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2.2 Goals

2.3 Conventions

3 Register File Defintions

3.1 General Purpose Registers

3.1.1 Definition

3.1.2 Usage

3.2 Speial Registers

3.2.1 Control Registers

3.2.2 Supervisor Registers

4 Instruction Defintions

4.1 Instruction Types

4.1.1 Integer

4.1.2 Immediate

4.1.3 LoadStore

4.1.4 BranchJump

4.1.5 Floating Point

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4.1.8 Co-Processor

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4.2 List of Instructons

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4.2.2 Immediate

4.2.3 LoadStore

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5 Exceptions and Interrupts

5.1 Exceptions

5.2 Interrupts

5.2.1 User Level

5.2.2 Supervisor Level

7 Programming Conventions

7.1 Register Usage

7.2 Memory Locations for Vector Table

7.2.1 Interrupt Vector Table

7.2.2 Exception Vector Table