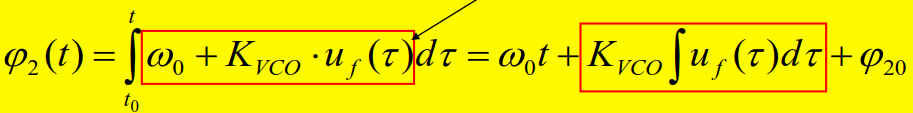


“spurs”

PLL

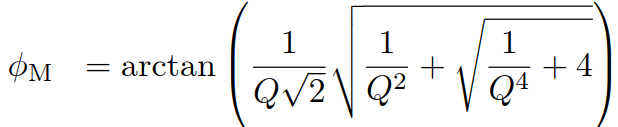
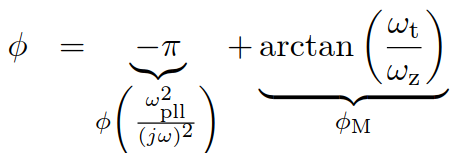
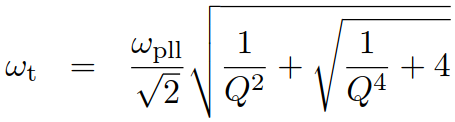
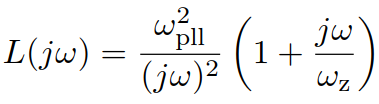
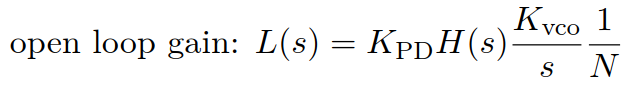
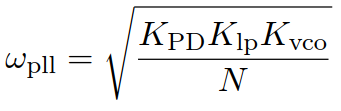
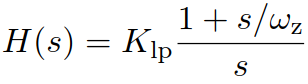
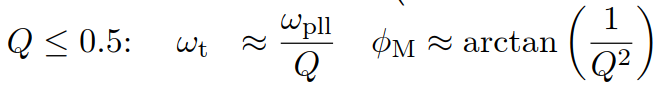
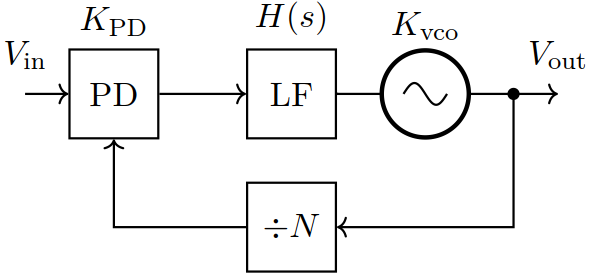
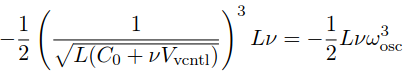
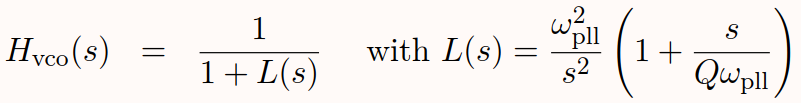
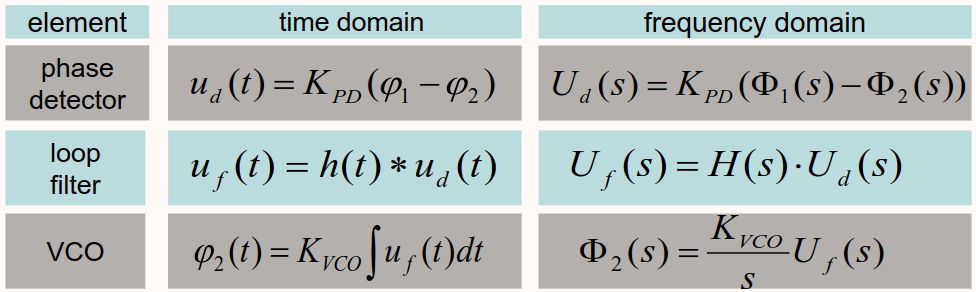
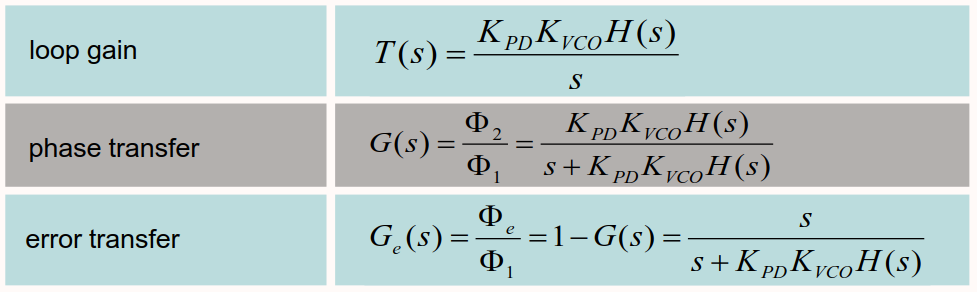
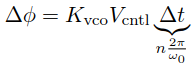
**Oscillator**



A VCO has a free-running frequency of **f0** with **Vcntl** = 0. Its output is applied to a frequency divider with **N**. When a pulse of amplitude **Up** and duration **tp** is applied to Vcntl, the phase of the f0/N clock at the output of the divider is observed to change by **Δφ** (in rad). Estimate **KVCO**

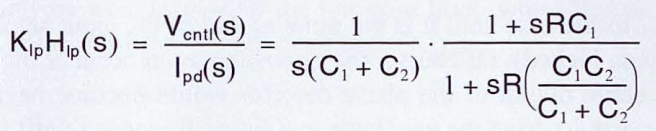
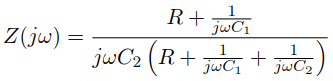
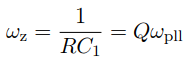
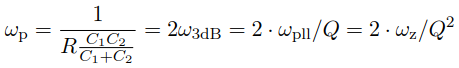
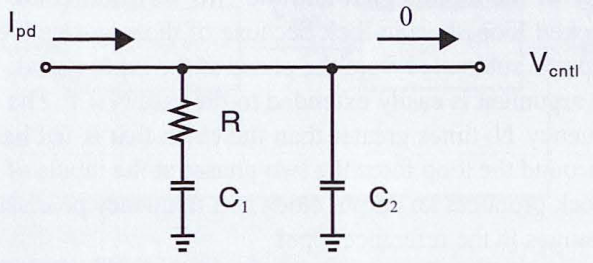
s /V.

**VCO**

S 

\* 1/N

How many cycles are required in order to change the output phase by **Δφ** with **Vcntl** and **KVCO**.



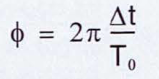
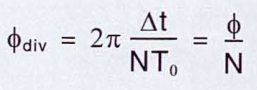
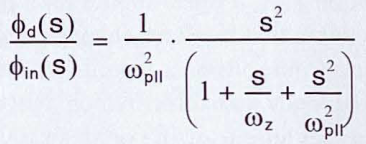
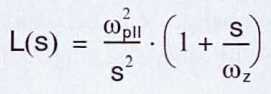
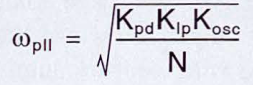
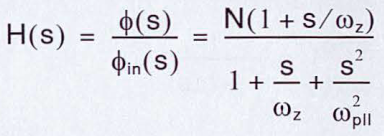
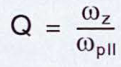
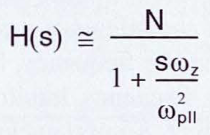
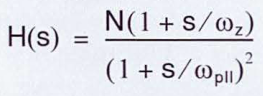
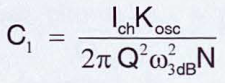
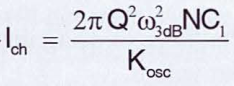
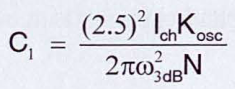
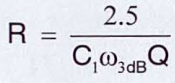
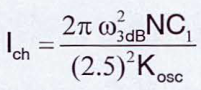
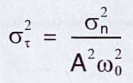
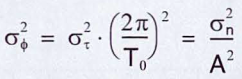
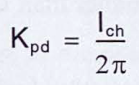
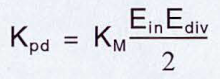
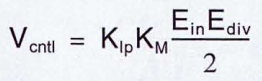
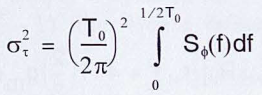
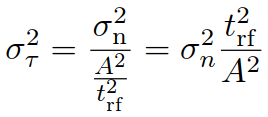
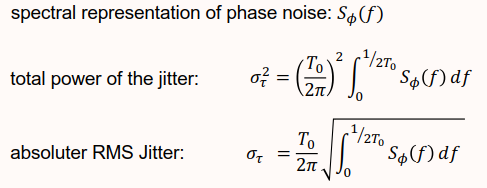
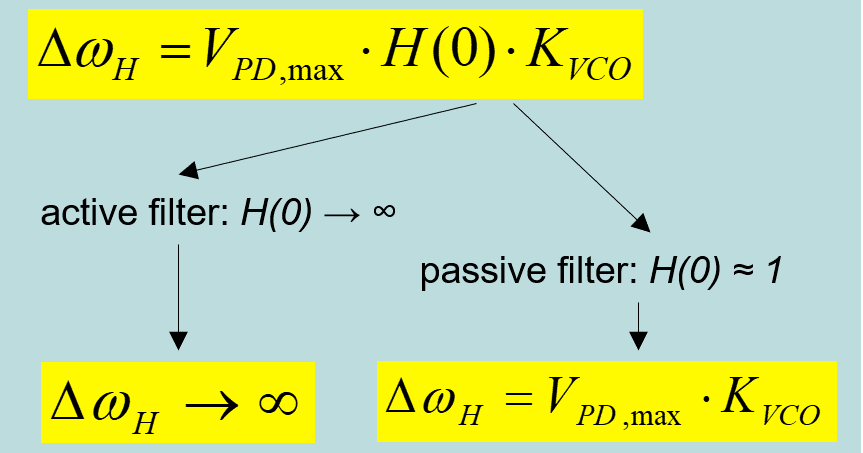
**for Q = 0.5 🡪 2.5**

**for Q << 0.5**

Find the new values of Q when the output frequency is changed?

What value of N results in the worst case loop bandwidth?

A PLL is to operate with a reference clock frequency **fref** = [MHz] and an output frequency **fout** = [MHz]. Design a loop ﬁlter (R, C1) for the charge-pump phase comparator so that the loop bandwidth is approximately **[1/15]th** of the reference clock frequency and **Q** = []. Assume the VCO has **Kvco** = [rad/s /V] and the charge-pump current is **Icp** = [µA].



**= maximum frequency deviation in the lock range**

**Static Hold Range**

**power**

***trf*** = rise / fall time of digital signal

