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CONFIDENTIAL

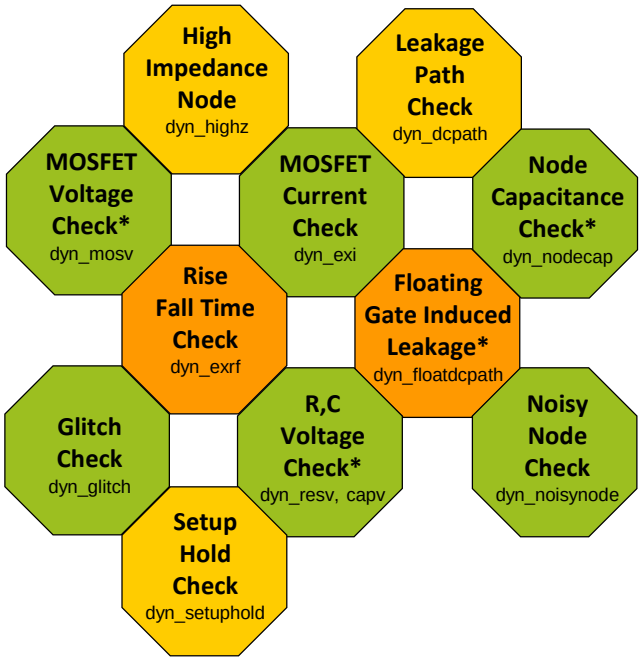
INVENTIVE

XPS Design Checks Introduction

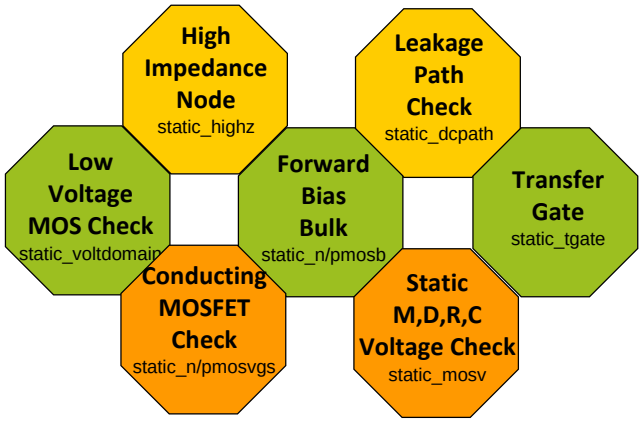
04/03/2015

XPS Design Check Overview

Dynamic Checks



Static Checks



尽早发现 topology/function/timing 问题

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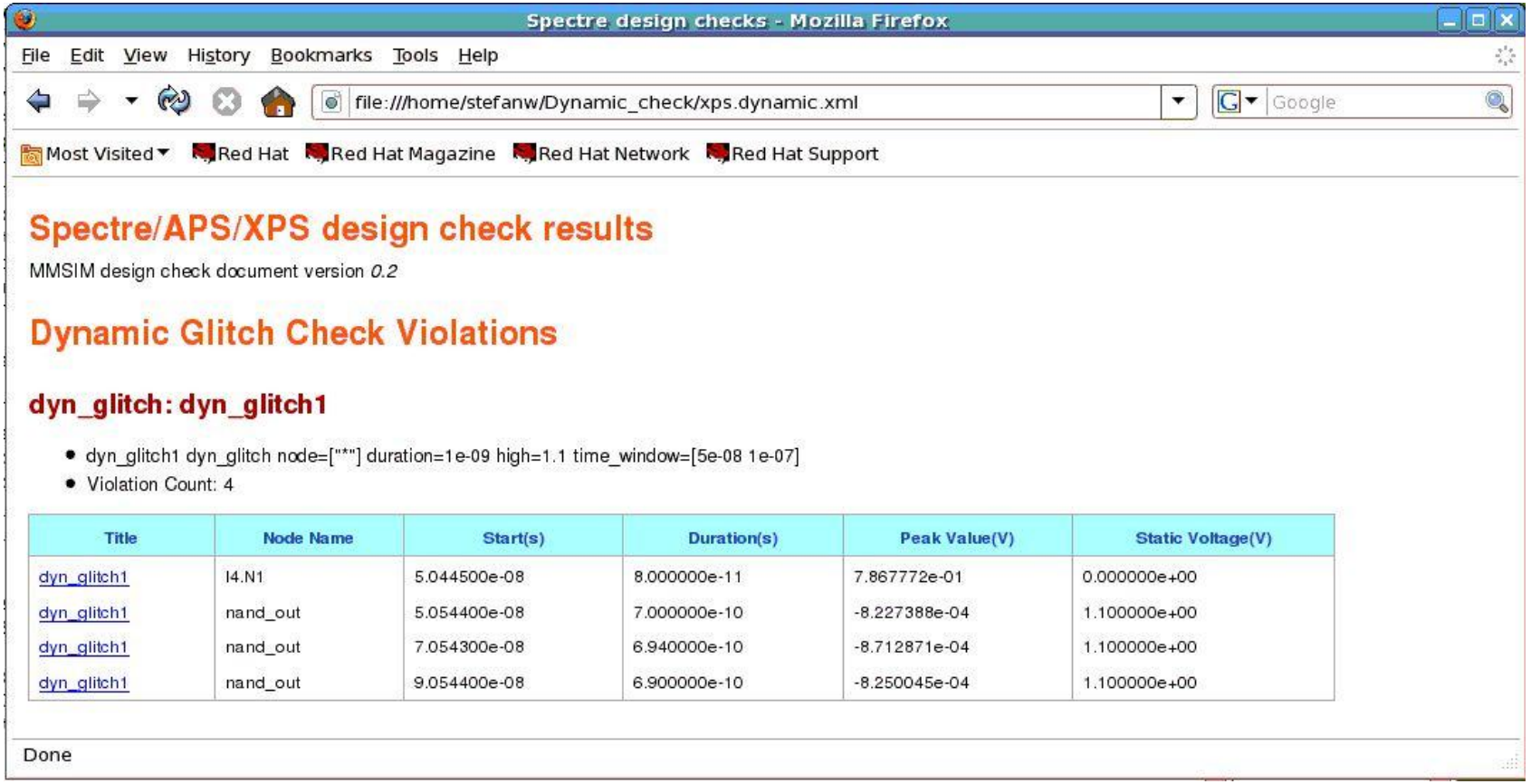
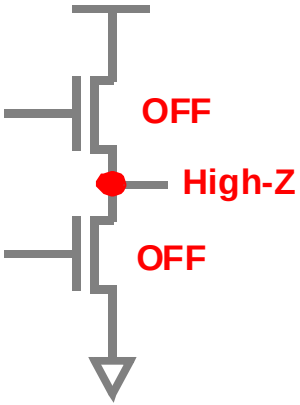
Design Check Output

可输出成文本、网页格式。



Dynamic High Impedance Node Check (dyn_highz)




```
hz1 dyn_highz  node=[*] duration=2n time_window=[1n 10n]
```

Dynamic HighZ Node Check Violations

dyn_highz: hz1

- hz1 dyn_highz node=["*"] duration=2e-09 time_window=[1e-09 1e-08]
- Violation Count: 1

Title	Node Name	Start(s)	Duration(s)
hz1	out	1.000000e-09	9.000000e-09

- Title Node Name Start(s) Duration(s)
- highz_cck XPRE1.XI7.C 1.000000e-10 4.990000e-08
- highz_cck XPRE1.XI7.B 1.000000e-10 4.990000e-08
- highz_cck XPRE1.XI7.A 1.000000e-10 4.990000e-08
- highz_cck XPRE1.XI6.C 1.000000e-10 4.990000e-08
- highz_cck XPRE1.XI6.B 1.000000e-10 4.990000e-08
- highz_cck XPRE1.XI6.A 1.000000e-10 4.990000e-08

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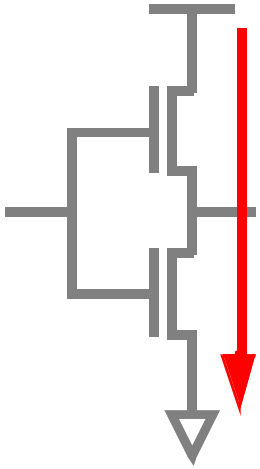
Dynamic DC Leakage Current Path (dyn_dcpath)



```
dyn_dcpath1 dyn_dcpath ith=1u duration=1n node=[vdd gnd]
time_window=[5n 10n]
```

Dynamic DC Leakage Path Check Violations

dyn_dcpath: dyn_dcpath1

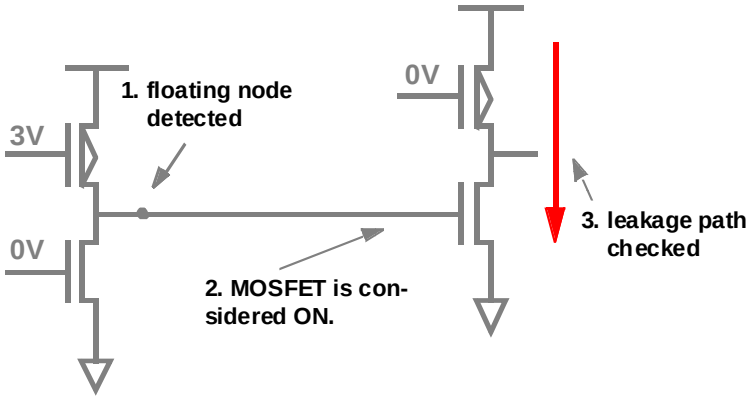
- dyn_dcpath1 dyn_dcpath ith=1e-06 duration=1e-09 node=["vdd" "gnd"] time_window=[5e-09 1e-08]
- Violation Count: 1

Title	From Node	To Node	Start(s)	Duration(s)
dyn_dcpath1	vdd	gnd	5.000000e-09	5.000000e-09

Path Elements:

- mp1
- mn2

Floating Gate Induced Leakage Check (dyn_floatdcpath)



dyn1 dyn_floatdcpath node=[vdd gnd] leaki_times=[1.1m]

Dynamic Floating Node Induced DC Leakage Path Check Violations

dyn_floatdcpath: dyn1

- dyn1 dyn_floatdcpath node=["vdd" "gnd"]
- Violation Count: 1

Title	From Node	To Node	Violation Time(s)
dyn1	vdd	gnd	7.976000e-09

Path Elements:

- mp1
- mn2

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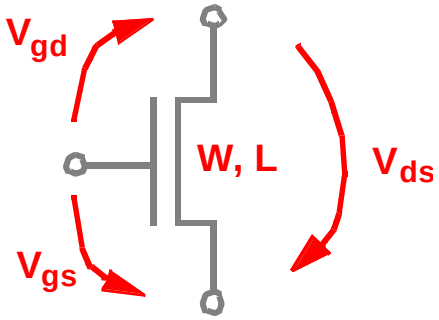
Dynamic MOSFET Voltage Check (dyn_mosv)




```
mosv dyn_mosv model=nmos cond=" v(g,s)>2&&I<2e-6"
duration=1n
```

Dynamic MOSFET Voltage Check Violations

dyn_mosv: mosv

- mosv dyn_mosv model=["nmos"] cond="v(g,s)>2&&I<2e-6" duration=1e-09
- Violation Count: 1

Title	Instance Name	Start(s)	Duration(s)
mosv	mn2	3.146000e-09	2.897000e-09

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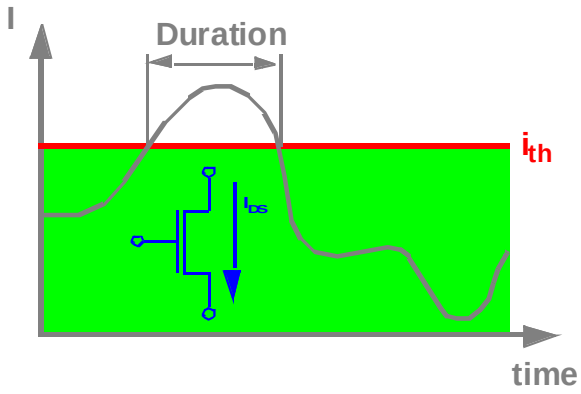
Dynamic Excessive Element Current Check (dyn_exi)




```
exi1 dyn_exi dev=[*] ith=1u duration=1n
exi2 dyn_exi dev=[*] ith=1u duration=1n inst=x1
exi3 dyn_exi dev=[*] ith=1u duration=1n subckt=res_exi
```

Dynamic Excessive Element Current Check Violations

dyn_exi: exi1

- exi1 dyn_exi dev=["*"] ith=1e-06 duration=1e-09
- Violation Count: 2

Title	Instance Name	Start(s)	Duration(s)	Max Current(A)
exi1	x1.mn1	4.923000e-09	5.077000e-09	2.320818e-03
exi1	x2.r1	1.280000e-10	9.872000e-09	3.000000e-03

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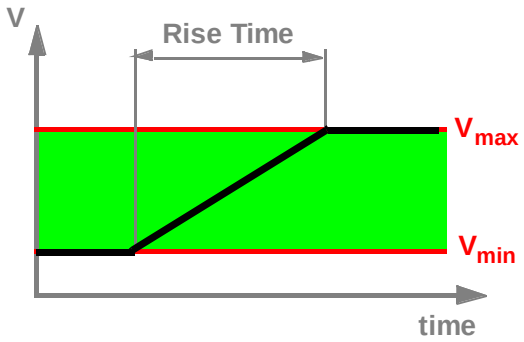
Dynamic Excessive Rise and Fall Time Check (dyn_exrf)



exrf1 dyn_exrf node=[*] rise=500p fall=500p vlth=0.3 vhth=2.7 time_window=[1n 9n]

Dynamic Excessive Rise, Fall, Undefined State Time Check Violations

dyn_exrf: exrf1

- exrf1 dyn_exrf node=["*"] rise=5e-10 fall=5e-10 utime=1e-09 vlth=0.3 vhth=2.7 time_window=[1e-09 9e-09]
- Violation Count: 5

Title	Node Name	Type	Start(s)	Duration(s)
exrf1	out	fall	1.390000e-09	1.288000e-09
exrf1	out1	utime	1.440000e-09	7.560000e-09
exrf1	t1	rise	4.838000e-09	8.270000e-10
exrf1	t2	fall	5.596000e-09	8.870000e-10
exrf1	out	rise	6.374000e-09	1.336000e-09

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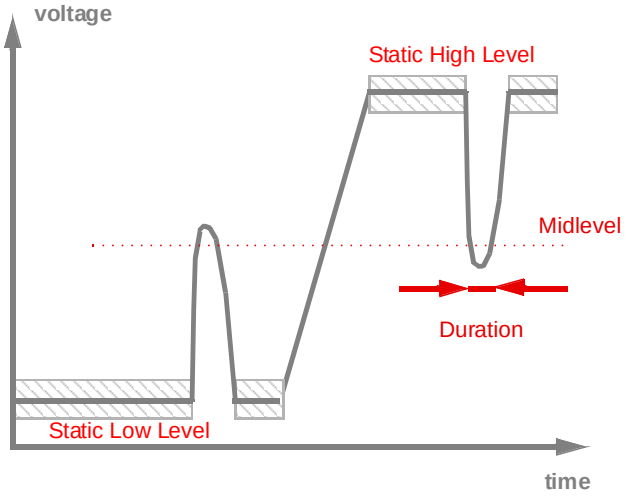
Dynamic Glitch Check (dyn_glitch)



dyn_glitch1 dyn_glitch node=[*] duration=1n high=1.2

Dynamic Glitch Check Violations

dyn_glitch: dyn_glitch1

- dyn_glitch1 dyn_glitch node=["*"] duration=1e-09 high=1.2
- Violation Count: 4

Title	Node Name	Start(s)	Duration(s)	Peak Value(V)	Static Voltage(V)
dyn_glitch1	XIL6.A1	2.064000e-09	2.940000e-10	-1.588217e-03	1.200000e+00
dyn_glitch1	OUT	2.089000e-09	3.050000e-10	1.197951e+00	0.000000e+00
dyn_glitch1	XIL6.A1	1.207800e-08	1.330000e-10	1.162371e+00	0.000000e+00
dyn_glitch1	OUT	1.210600e-08	1.320000e-10	-6.177051e-03	1.200000e+00

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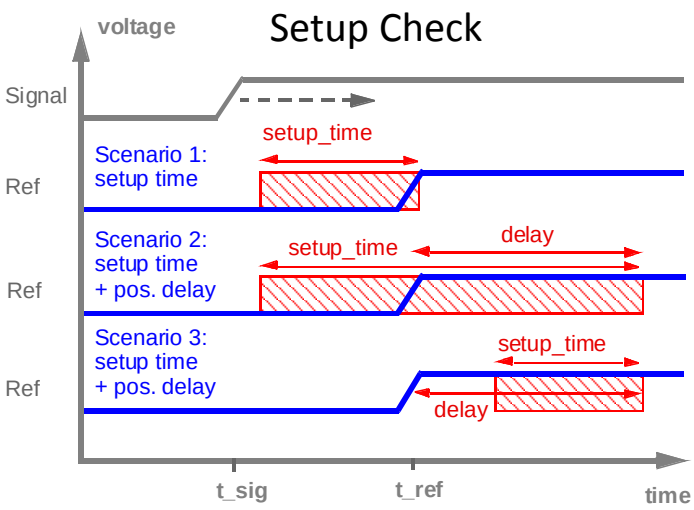
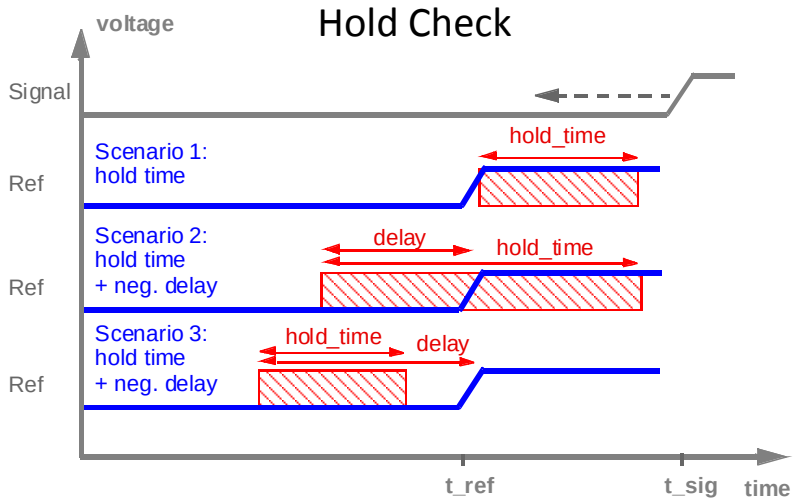
Dynamic Setup and Hold Check (dyn_setuphold)

- A setup or hold error is reported if the signal net transition occurs in the red marked area.






```
d1 dyn_setuphold node=data edge=both ref_node=clk ref_edge=rise setup_time=10n
d2 dyn_setuphold node=data edge=both ref_node=clk ref_edge=rise hold_time=10n
```

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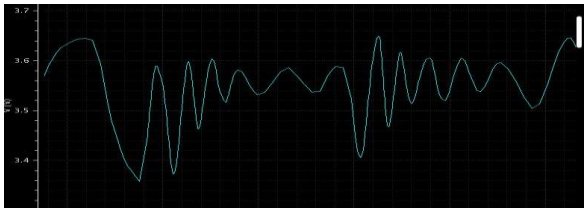
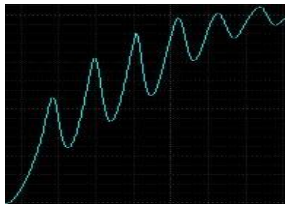
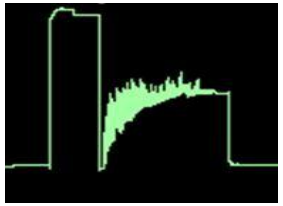
Dynamic Unstable Node Check (dyn_noisynode)







u1 dyn_noisynode node=["*"] duration=1e-08 skip=1.5e-10 time_window=[0 20n]

Dynamic Noisy Node Check Violations

dyn_noisynode: u1

- u1 dyn_noisynode node=["*"] duration=1e-08 skip=1.5e-10
- Violation Count: 5

Title	Node Name	Start(s)	Duration(s)
u1	2	8.333333e-12	1.998472e-08
u1	3	8.333333e-12	1.998472e-08

Dynamic Node Capacitor Check (dyn_nodecap)

```
n1 dyn_nodecap node=[*]
```

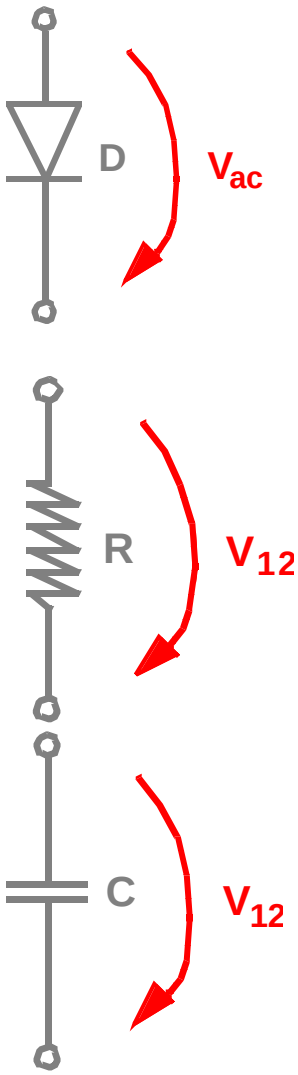
Dynamic Node Capacitance Check

dyn_nodecap: n1

- n1 dyn_nodecap node=["*"]
- Violation Count: 5

Title	Node Name	Capacitance(F) ▲
n1	mid	3.231565e-13
n1	out	1.033802e-13

Dynamic Device Terminal Voltage Check




```
dv1 dyn_diodev model=diode1 cond="v(a,c)>1.9“ duration=1n
```

```
resv dyn_resv cond="v(1,2)>1.2" duration=2n
```

```
capv dyn_capv cond="v(1,2)>1.2" duration=2n
```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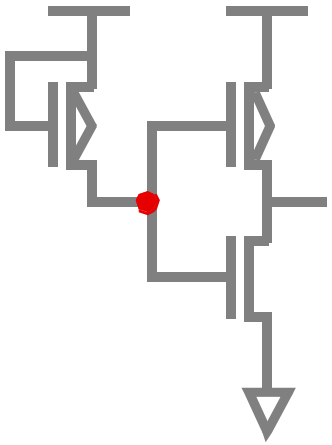
Static High Impedance Node Check (static_highz)



static_hz1 static_highz node=[*] vlth=0.3 vhth=1.8

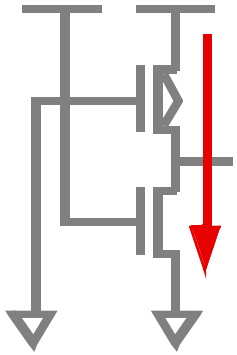
Static HighZ Node Check Violations

static_highz: static_hz1

- static_hz1 static_highz node=["*"] vlth=0.3 vhth=1.8
- Violation Count: 1

Title	Node Name
static_hz1	in

Static DC Leakage Path Check (static_dcpath)



dc1 static_dcpath node=[vdd gnd] vlth=0.7 vhth=1.0

Static DC Leakage Path Check Violations

static_dcpath: dc1

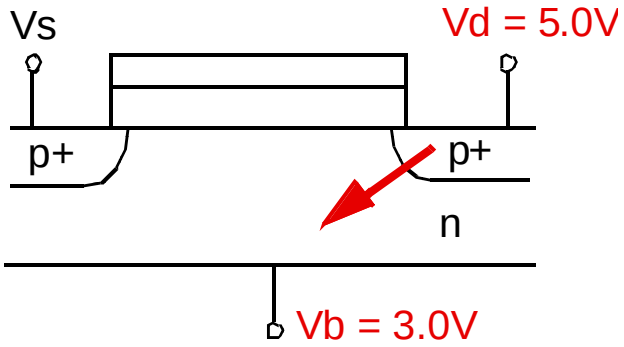
- dc1 static_dcpath node=["vdd" "gnd"] vlth=0.7 vhth=1
- Violation Count: 1

Title	From Node	To Node
dc1	vdd	gnd

Path Elements:

- x3.mp1
- x3.mn2

Forward Bias Bulk Check (static_nmosb, static_pmosb)




```
nmosb1 static_nmosb model=nmos vlth=0.3 vhth=0.7
```

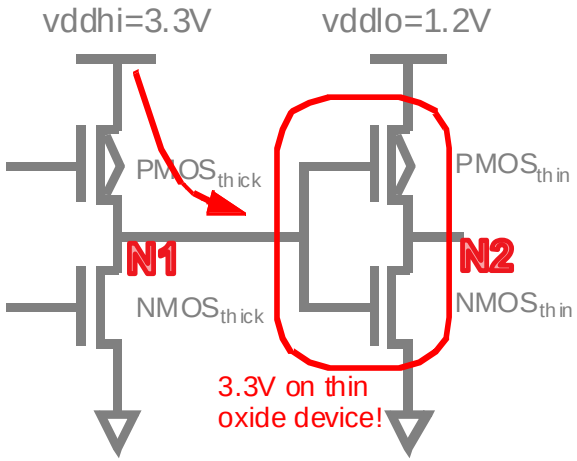
Static Forward Bias Bulk Check Violations

static_nmosb: nmosb1

- nmosb1 static_nmosb model=["nmos"] vlth=0.3 vhth=0.7
- Violation Count: 1

Title	Instance Name
nmosb1	X1.MN1

Static Voltage Domain Device Check (static_voltdomain)




```
Chk_domain1 static_voltdomain model=[LVNMOS] inst=[x1 x2.x3 x4.x5.*]
Chk_domain2 static_voltdomain subckt=[pump regulator inv]
Chk_domain3 static_voltdomain subckt=[*]
```

Static Voltage Domain Device Check Violations

static_voltdomain: mos1

- mos1 static_voltdomain model=["nmos"] vlth=2 vhth=10
- Violation Count: 1

Title	Node Name	Instance Name
mos1	mid	x2.mn2

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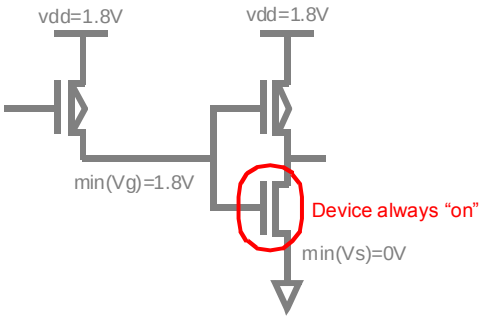
Static Always Conducting MOSFET (static_n(p)mosvgs)



mos1 static_nmosvgs model=nmos vt=0.5 vhth=0.8 vlth=0.2

Static Always Conducting MOSFET Check Violations

static_nmosvgs: mos1

- mos1 static_nmosvgs model=["nmos"] vt=0.5 vlth=0.2 vhth=0.8
- Violation Count: 1

Title	Instance Name
mos1	x2.mn2

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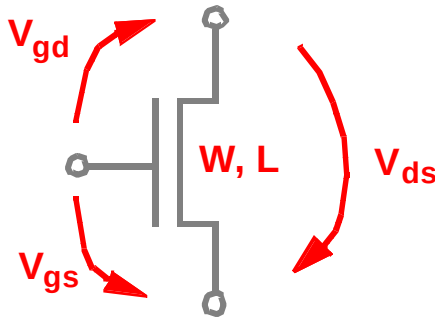
Static MOSFET Voltage Check (static_mosv)



mos1 static_mosv model=["nmos"] cond="v(g,s)>1.9"

Static MOSFET Voltage Check Violations

static_mosv: mos1

- mos1 static_mosv model=["nmos"] cond="v(g,s)>1.9"
- Violation Count: 1

Title	Instance Name
mos1	x2.mn2

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Static ERC Check (static_erc)

```
chk1 static_erc floatgate=all
```

- Perform ERC checks and reports errors into file with extension ‘static.xml’.
- Priority for 13.1 and following ISR’s: hotwell, floatbulk, floatgate, dangle
- Parameters
  - hotwell=off|on : **report MOSFET with bulk not connected to VDD or GND**.
  - dangle=off|all|notop : **dangling node check**
  - floatgate=off|all|no_top: **floating gate check**

    floatbulk=off|all|no_top: **floating bulk check**

Dynamic Subckt Port Power Check (dyn_subcktpwr)

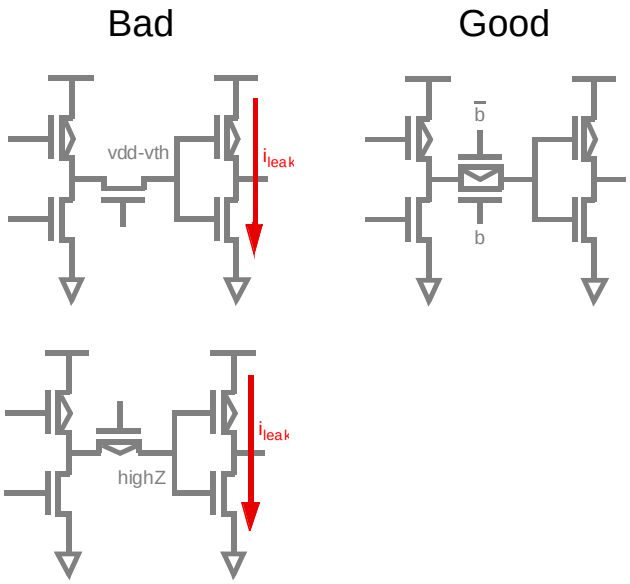
```
p1 dyn_subcktpwr inst=x1 port=[*] depth=4 time_window=[1u 10u]
```

```
Time: from 10n to 50n
*** Port Current Summary ********************
Max(A) Avg (A) RMS(A) Max Time
x1.B 600e-3 600e-3 500e-3 15e-9
x1.x2.x3.b 550e-3 300e-3 300e-3 12e-9

*** Port Power Summary **********
Max(w) Avg (w) RMS (w) Max time
x1.B 40e-3 50e-3 60e-3 25e-9
x1.x1.in2 32e-3 40e-3 5e-3 40e-9

*** Subckt Power Summary ******
Max(w) Avg (w) RMS (w) Max time
x1 60e-3 50e-3 0e-3 10e-9
x1.x1 30e-3 30e-3 10e-3 20e-9
```

Static Transmission Gate Check (static_tgate)




```
tgate1 static_tgate node=[*]
```

Static Transmission Gate Check Violations

static_tgate: tgate1

tgate1 static_tgate node=["*"]

Violation Count: 2

Title	Node Name
tgate1	in2
tgate1	in4

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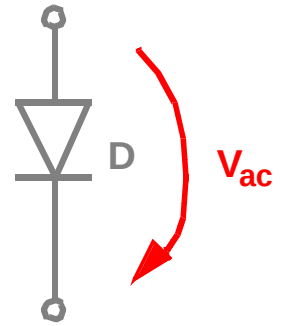
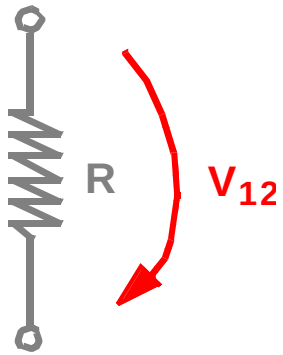
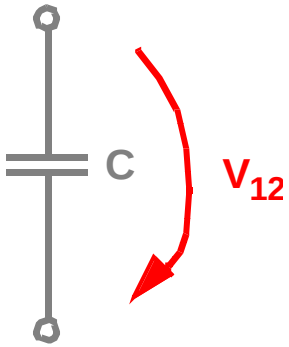
Static Device Terminal Voltage Check




```
dv1 static_diodev model=diode1 cond="v(a,c)>1.9"
```




```
resv1 static_resv cond="v(1,2)>1.2"
```




```
capv1 static_capv cond="v(1,2)>1.2"
```

Static Resistor/Capacitor Value Check

```
chk1 static_resistor type=distr rmin=0 rmax=1000G
```

```
chk1 static_capacitor type=distr cmin=0 cmax=1p
```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