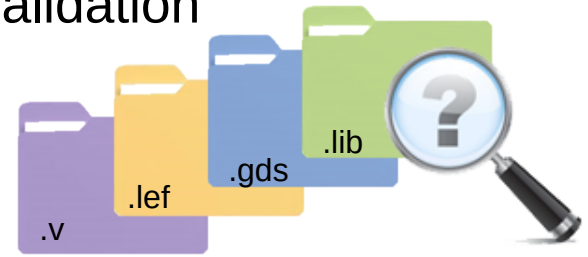
Qualib™ Introduction

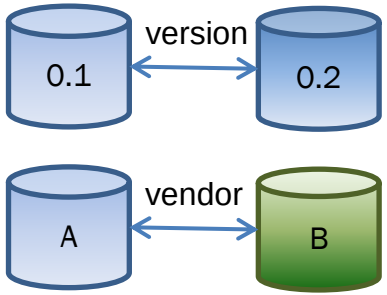
2015.12

Problems & Challenges

- More and more IPs and libraries to do validation
- So many views of each IP or std cell to do validation
  - Netlist
  - LEF/GDS
  - Timing lib
  - …



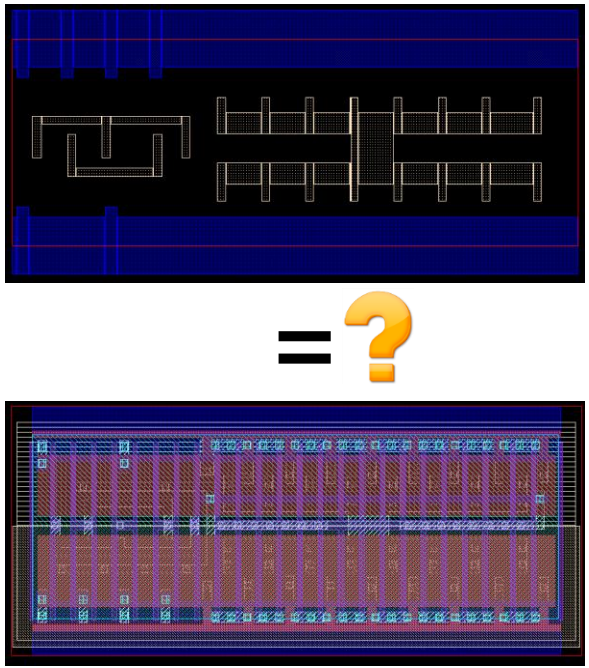
- Difficult to compare the performance of IPs or libraries from different vendors, or different versions…



Case Analysis A

Just before a tape-out, it was found that the LEF and GDS of an IP were not matching.

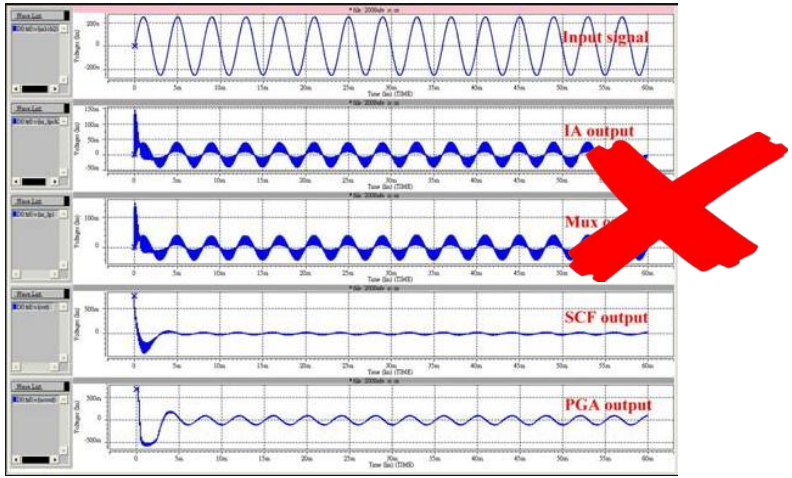
It took **days** to find out the difference and cause TO more than **2 weeks** delay.

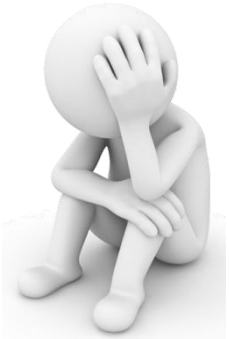


Case Analysis B

The timing liberty of an IP was not matching with netlist.

It caused **BIG** trouble for post simulation.

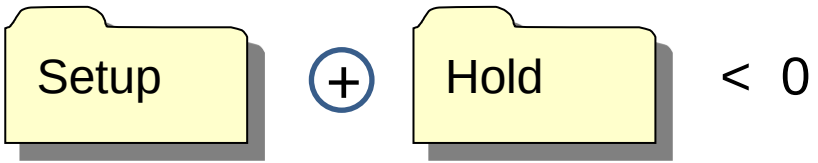




Case Analysis C

There was a timing closure problem in the design.

After **weeks** of debugging and many iterations,
it turned out to be the setup and hold constraint conflict of a Memory.



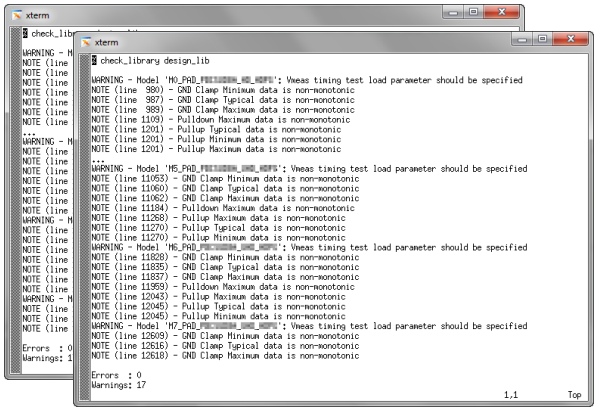
Qualib

"A Comprehensive IP/Library QA and Debugging Platform"

- Integrity checking
  - Layout
  - Timing
  - …
- Consistency checking
  - GDS vs. LEF
  - Verilog vs. Timing
  - …
- Comparison
  - Version control
  - Performance comparison

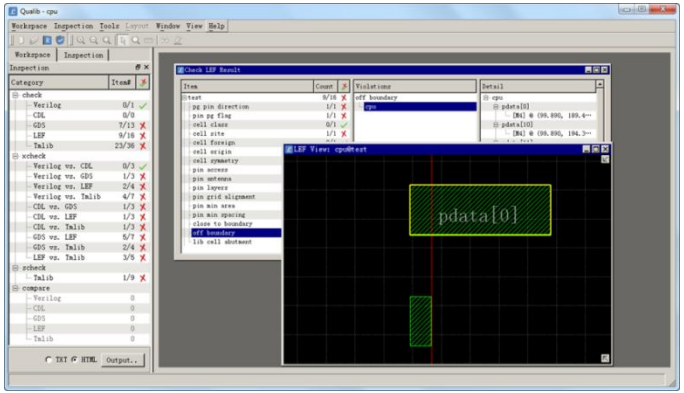
Improve QA Quality & Efficiency

Traditional Flow



- Based on experience; NO overall picture
- NO complete checking; poor IP/STD quality
- Difficult to maintain and expand

Qualib Flow

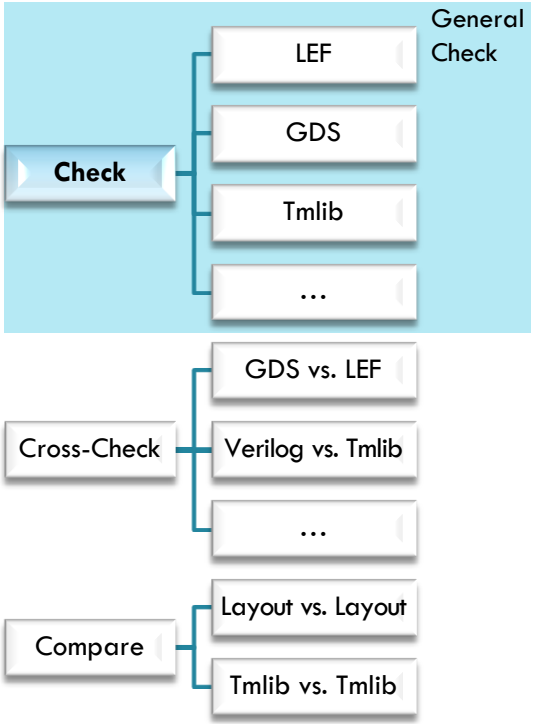


- Comprehensive check; combined with design flow
- Automatic flow; easy to probe the problem
- Shorter runtime and better design quality

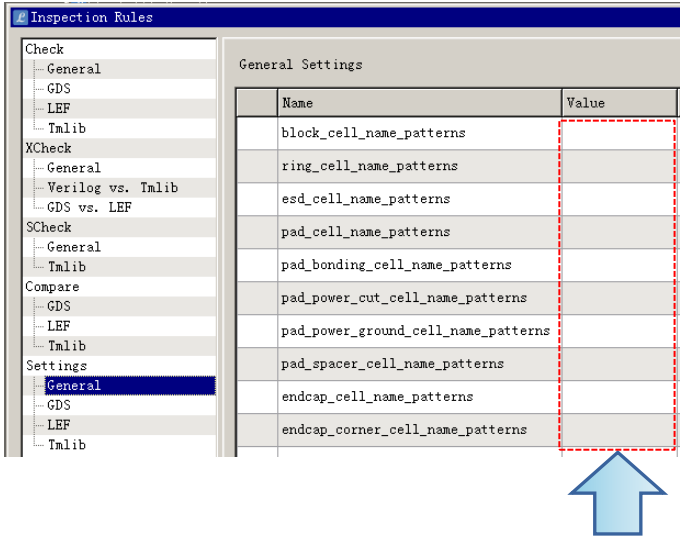
Application Scenarios

- Quality check during daily design
  - Front-end and back-end designer check DK view (interactive or batch mode)
- IP/STD regression check
  - Regression verification to all or specified DK view
- IP/STD Sign-off
  - Comprehensive examination before release, generate quality inspection reports
- Quality Sign-in before using libraries
  - P&R designers analyze and verify library quality, ensure ready and good to use

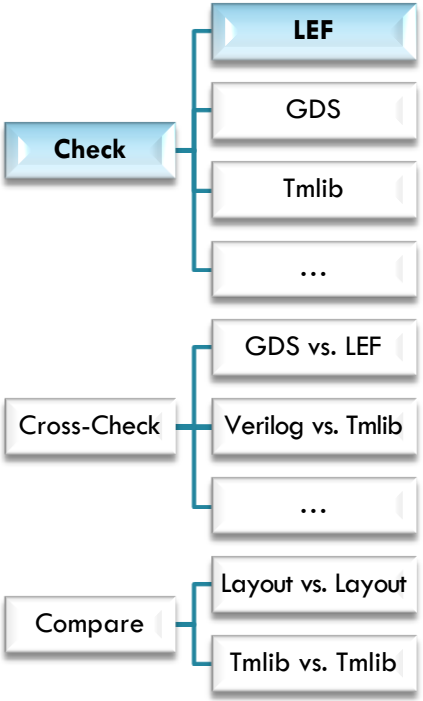
General Check



- Extra cells
- Missing cells
- Pin name
- P/G pin direction
- Pin P/G flag
- Cell class



LEF Check

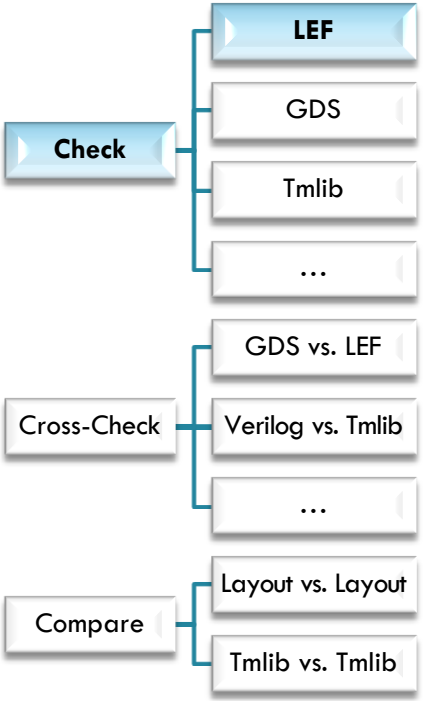


- Cell property
  - Cell class
  - Cell foreign
  - Cell origin
  - Cell symmetry
  - Cell site

LEF

```
MACRO cpu
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN cpu 0 0 ;
  SIZE 200.1 BY 200 ;
  SYMMETRY X Y ;
  PIN paddr[8]
    DIRECTION OUTPUT ;
    USE SIGNAL ;
    ANTENNAPARTIALMETALAREA 0.1484 LAYER M4 ;
    ANTENNAPARTIALMETALAREA 4.4604 LAYER M5 ;
    ANTENNAPARTIALMETALAREA 0.2916 LAYER M3 ;
    ANTENNAPARTIALCUTAREA 0.0392 LAYER VIA3 ;
    ANTENNAPARTIALCUTAREA 0.0392 LAYER VIA4 ;
    PORT
      LAYER M3 ;
        RECT 100.465 129.93 100.535 130 ;
    END
  END paddr[8]
  ...
  OBS
    LAYER M1 ;
      RECT 0.25 0.25 199.75 129.26 ;
      RECT 0.25 0.25 102.34 129.75 ;
      RECT 103.18 0.25 199.75 129.75 ;
      RECT 0.25 0.25 99.925 131.945 ;
      RECT 0.25 0.25 99.75 199.75 ;
    LAYER M2 ;
    ...
  END
END cpu
```

LEF Check



- Pin property
  - Pin antenna
  - Pin direction
  - Pin layer
  - P/G direction
  - Use Power/Ground

LEF

```
MACRO cpu
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN cpu 0 0 ;
  SIZE 200.1 BY 200 ;
  SYMMETRY X Y ;
  PIN paddr[8]
    DIRECTION OUTPUT ;
    USE SIGNAL ;
    ANTENNAPARTIALMETALAREA 0.1484 LAYER M4 ;
    ANTENNAPARTIALMETALAREA 4.4604 LAYER M5 ;
    ANTENNAPARTIALMETALAREA 0.2916 LAYER M3 ;
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    PORT
      LAYER M3 ;
        RECT 100.465 129.93 100.535 130 ;
    END
  END paddr[8]
  ...
  OBS
    LAYER M1 ;
      RECT 0.25 0.25 199.75 129.26 ;
      RECT 0.25 0.25 102.34 129.75 ;
      RECT 103.18 0.25 199.75 129.75 ;
      RECT 0.25 0.25 99.925 131.945 ;
      RECT 0.25 0.25 99.75 199.75 ;
    LAYER M2 ;
    ...
  END
END cpu
```
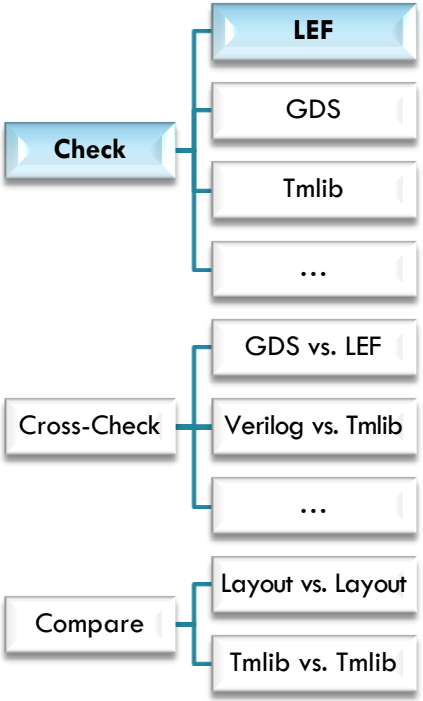

LEF Check



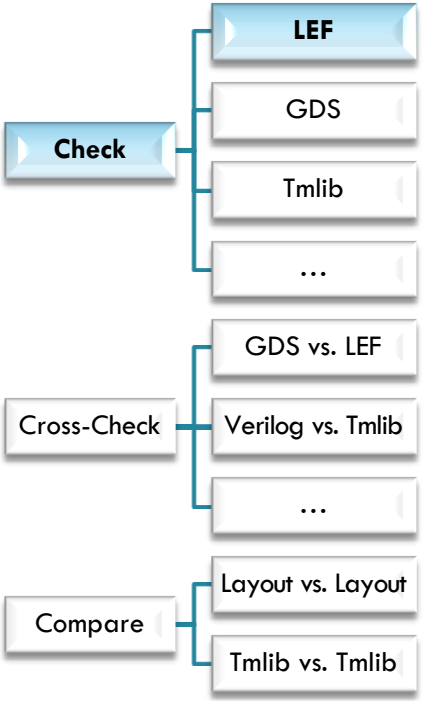
- **DRC**
  - **Pin off grid**
  - Out of boundary
  - Close to boundary
  - Min_area/spacing/width
- **Routability**
  - Pin access
  - Routing congestion
  - Routing flexibility

LEF

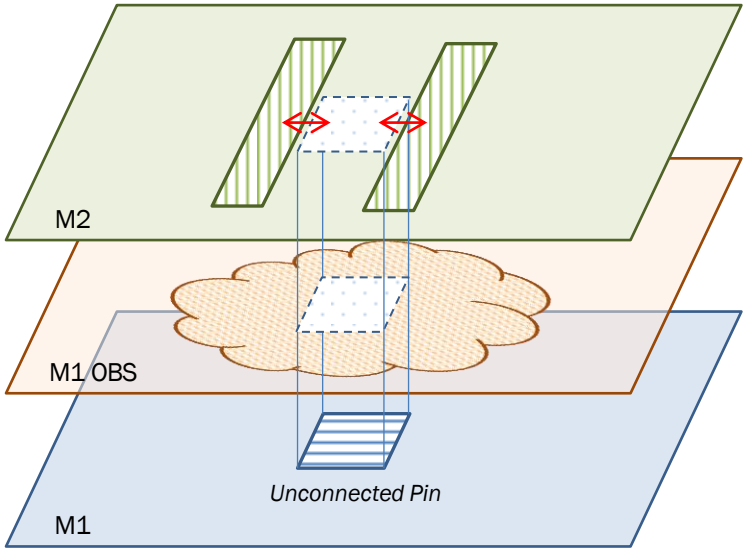
```
UNITS
  CAPACITANCE PICOFARADS 1 ;
  CURRENT MILLIAMPS 1 ;
  VOLTAGE VOLTS 1 ;
  DATABASE MICRONS 2000 ;
  FREQUENCY MEGAHERTZ 1 ;
END UNITS

MANUFACTURINGGRID 0.005 ;
```

```
MACRO cpu
  CLASS CORE ;
  ORIGIN 0 0 ;
  FOREIGN cpu 0 0 ;
  SIZE 200.1 BY 200 ;
  SYMMETRY X Y ;
  ...
  PIN portain[4]
    DIRECTION INPUT ;
    USE SIGNAL ;
    ANTENNAPARTIALMETALAREA 2.2134 LAYER M4 ;
    PORT
      LAYER M4 ;
        RECT 99.891 187.335 100 187.585 ;
    END
  END portain[4]
```

LEF Check

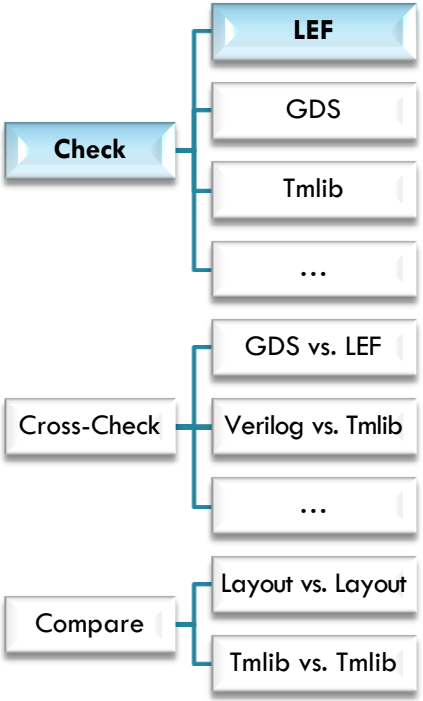


- **DRC**
  - Pin off grid
  - Out of boundary
  - Close to boundary
  - Min_area/spacing/width
- **Routability**
  - **Pin access**
  - Routing congestion
  - Routing flexibility

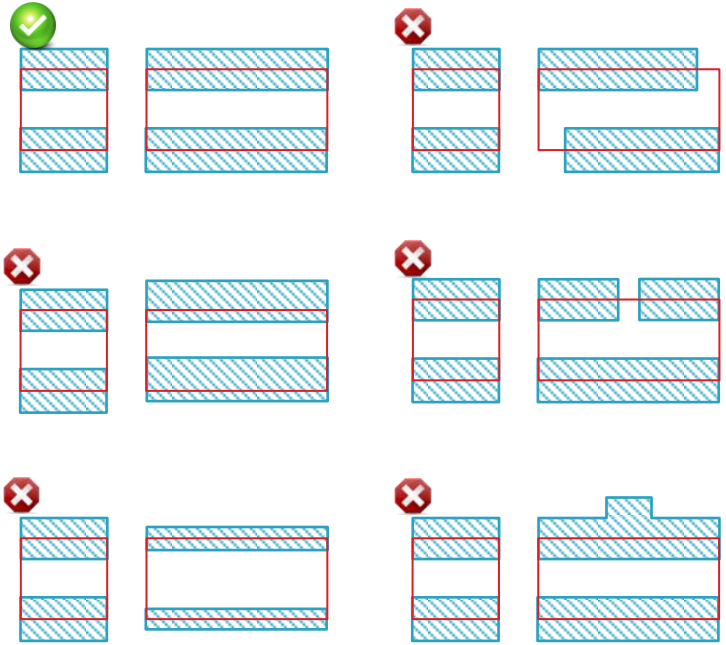


Pin shape cannon be routed due to blockage or DRC violation.

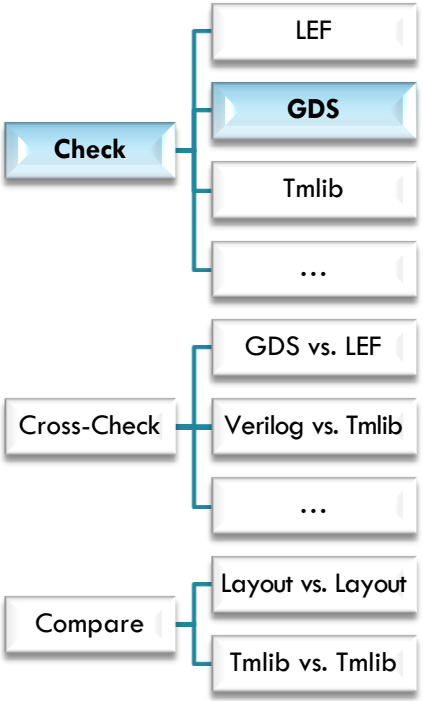
LEF Check



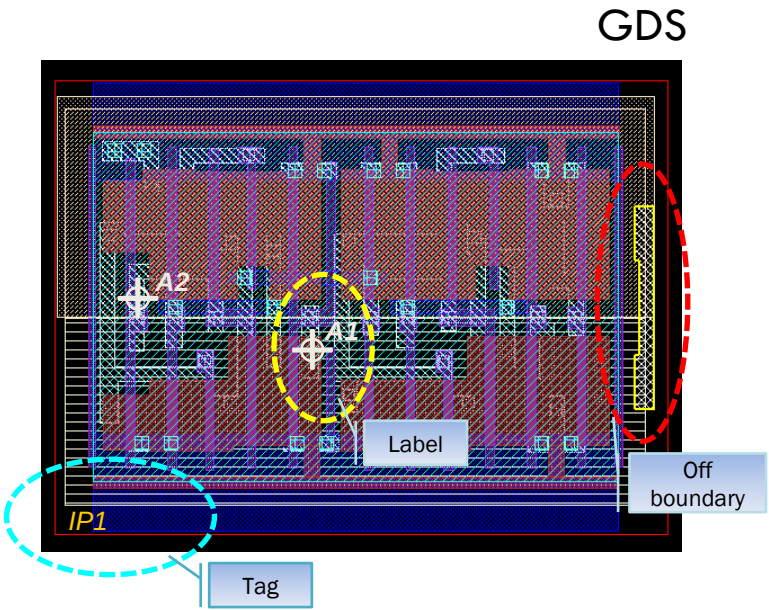
- Cell Abutment



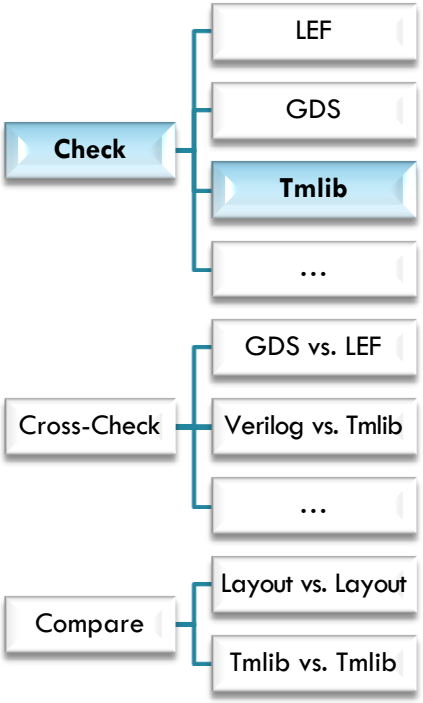
GDS Check



- **Label**
  - Label height
  - Label redundancy
  - Label layer
- **Tag**
  - Tag layer
  - Tag content
- **DRC**
  - Off grid
  - Out of boundary
  - Close to boundary



Timing Lib Check



- **Checking items**
  - Presence
  - Symmetry
  - Integrity
  - Outliers
  - Redundancy
  - Confliction
  - Trend
  - Desired/preferred value
  - CCS-NLDM correlation
  - …

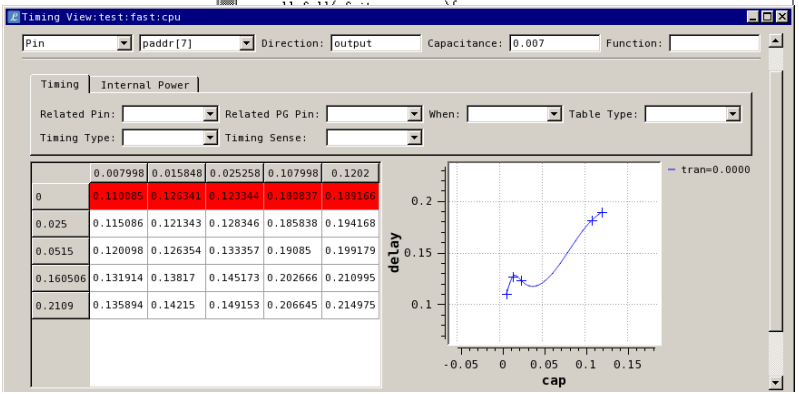
Timing/Internal power Arc	…
Timing/Internal power Table	Table value
	Table index
Leakage power	…
Cell attribute	Area
	Footprint
Pin attribute	Capacitance
	Max transition
	Max/min capacitance
Library definition	Operating condition
	Unit
	Slew/delay definition
Power/Ground attributes	Voltage_map
	Power down function
…	…

Timing Lib Check

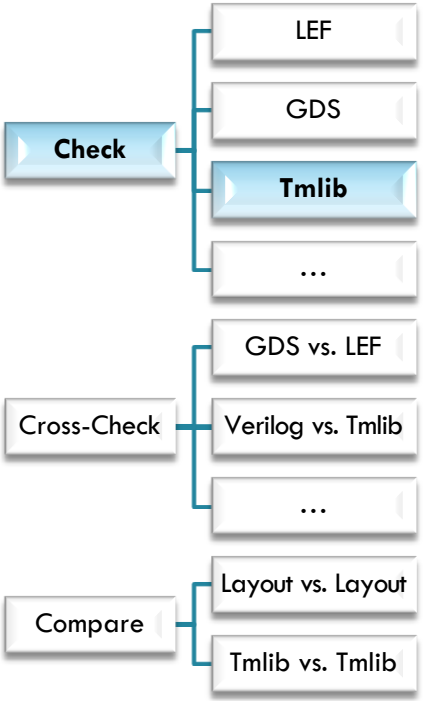
- **Check**
  - LEF
  - GDS
  - **Tmlib**
  - …
- **Cross-Check**
  - GDS vs. LEF
  - Verilog vs. Tmlib
  - …
- **Compare**
  - Layout vs. Layout
  - Tmlib vs. Tmlib

- Timing constraint conflict
  - setup_const + hold_const < 0
- Timing table monotonicity

```
pin("paddr[7]") {
  direction : output ;
  ...

  timing () {
    related_pin : "debugpc[3]" ;
    timing_type : combinational ;
    timing_sense : positive_unate ;

    cell_rise( f_itrans_ocap ){
      index_1 ( "0.000000, 0.025000, 0.051500, 0.160506, 0.210900");
      index_2 ( "0.007998, 0.015848, 0.025258, 0.107998, 0.120200");
      values ( "0.110085, 0.126341, 0.123344, 0.180837, 0.189166",\
           "0.115086, 0.121343, 0.128346, 0.185838, 0.194168",\
           "0.120098, 0.126354, 0.133357, 0.190850, 0.199179",\
           "0.131914, 0.138170, 0.145173, 0.202666, 0.210995",\
           "0.135894, 0.142150, 0.149153, 0.206645, 0.214975");
    }
    rise_transition( f_itrans_ocap ){
      ...
    }
```



Timing Lib Check

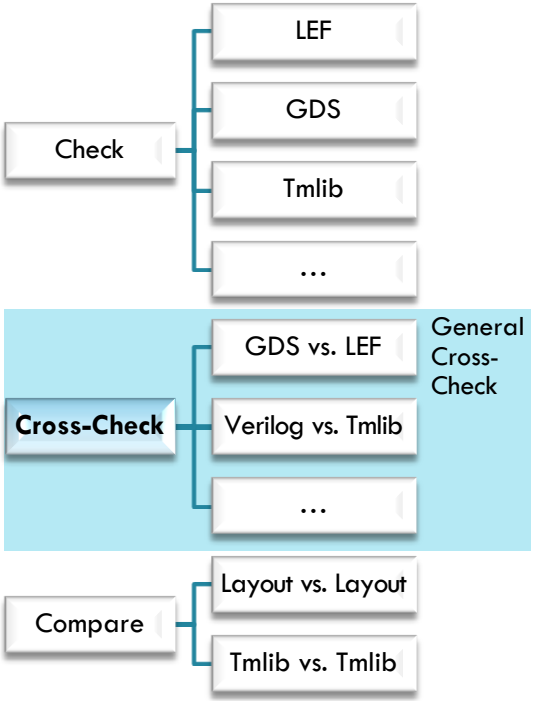


- Operating condition check
  -- process
  -- temperature
  -- voltage
  -- tree_type

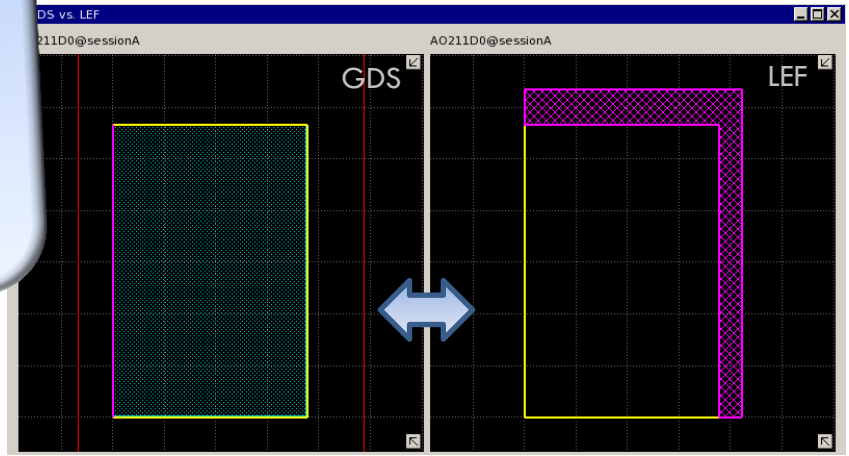
```
library (lib0p99v0cbc) {
        technology (cmos) ;
    delay_model : table_lookup ;
    revision    : 120 ;
    simulation  : true ;
    nom_process : 1 ;
    nom_temperature : 0;
    nom_voltage : 0.99;
    voltage_map(COREVDD1, 0.99);
    voltage_map(CORESNM1, 0.0);
    operating_conditions("0p99v0cbc"){
        process : 1;
        temperature : 0;
        voltage : 0.99;
        tree_type : "balanced_tree";
    }
    default_operating_conditions : 0p99v0cbc ;
    capacitive_load_unit (1,pf) ;
    voltage_unit : "1V" ;
    current_unit : "1mA" ;
```

icexplorer> **create_tmlib_corner** *-session* A {scc40nll_hs_lvt_ss_1_0.99_0}
-nominal_keyword {scc40nll_hs_lvt_ss}
-tree_type {balanced_tree}
-process {1} *-temperature* {0} *-voltage* {0.99}

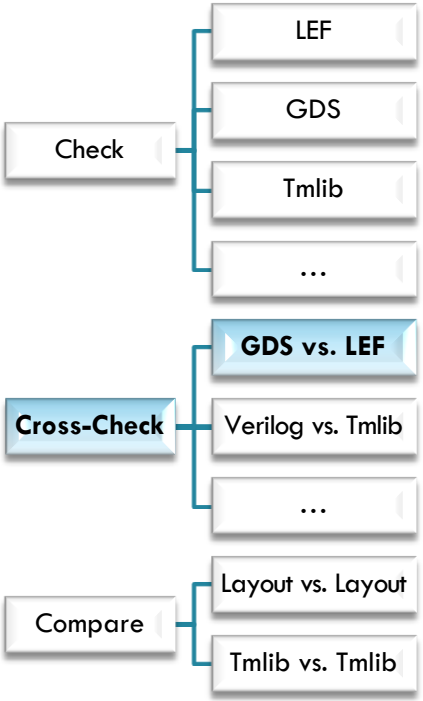
General Cross-Check



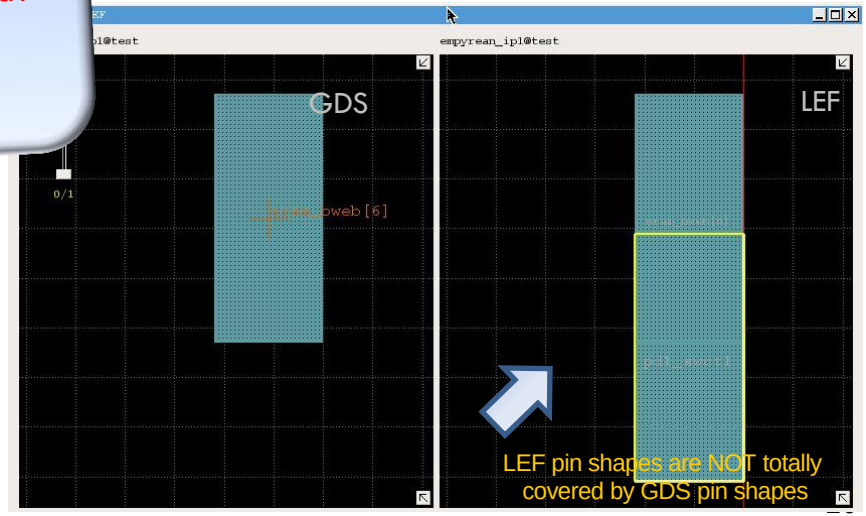
- Extra cells
- Missing cells
- Cell area
- Cell boundary
- Pin name
- Pin direction



GDS vs. LEF Cross-Check



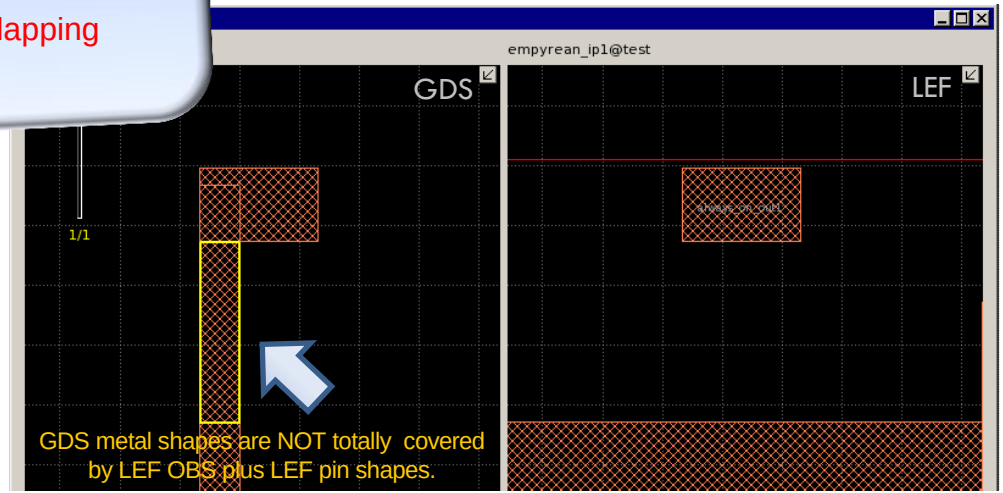
- Pin layer matched?
- Pin shape matched?
- OBS overlapping



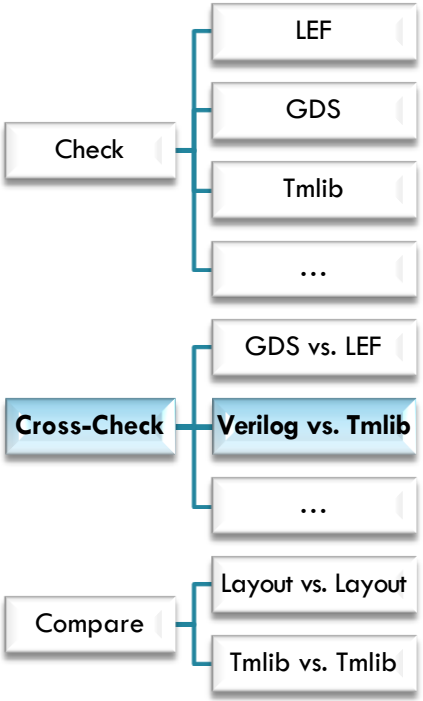
GDS vs. LEF Cross-Check

- Check
  - LEF
  - GDS
  - Tmlib
  - …
- **Cross-Check**
  - **GDS vs. LEF**
  - Verilog vs. Tmlib
  - …
- Compare
  - Layout vs. Layout
  - Tmlib vs. Tmlib

- Pin layer matched?
- Pin shape matched?
- OBS overlapping



Verilog vs. Tmlib Cross-Check



- Pin function
- Arc and sdf_cond
- Timing check

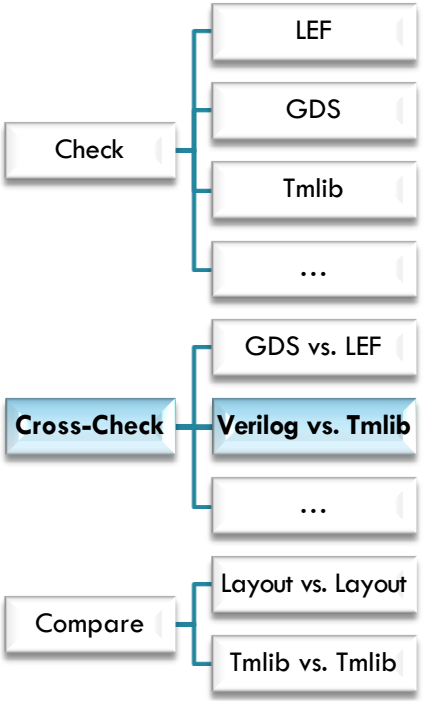
Timing .lib

```
cell (XNR3D1) {
  area : 4.2338;
  cell_footprint : "xnr3d1";

  pin(Z) {
    direction : output;
    function : "(!((A1^A2)^A3))";
    max_capacitance : 0.07452;
    timing () {
      related_pin : "A1";
      sdf_cond : "A2 == 1'b1 && A3 == 1'b0";
      timing_sense : positive_unate;
      timing_type : combinational;
      when : "A2&!A3";
      cell_rise (delay_template_7x7_0) {
        index_1 ("0.0017, 0.005, 0.0117, 0.025, 0.0515, 0.1047, 0.2109");
        index_2 ("0.00079, 0.00196, 0.0043, 0.00898, 0.01834, 0.03707, 0.07452");
        values ( \
```

Verilog

```
module XNR3D1 (A1, A2, A3, ZN, VDD, VSS);
    inout VDD;
    inout VSS;
    input A1, A2, A3;
    output ZN;
    xor (I0_out, A1, A2);
    xor (I1_out, I0_out, A3);
    not (ZN_pwr_net, I1_out);
    u_power_down_sum iZN (ZN, ZN_pwr_net, Vsum);
    not (nVSS, VSS);
    and (Vsum, VDD, nVSS);

  specify
    if (A2 == 1'b1 && A3 == 1'b0)
    (A1 => ZN) = (0, 0);
    if (A2 == 1'b0 && A3 == 1'b1)
    (A1 => ZN) = (0, 0);
    ...
  endspecify
endmodule
```

Verilog vs. Tmlib Cross-Check



- Pin function
- Arc and sdf_cond
- Timing check

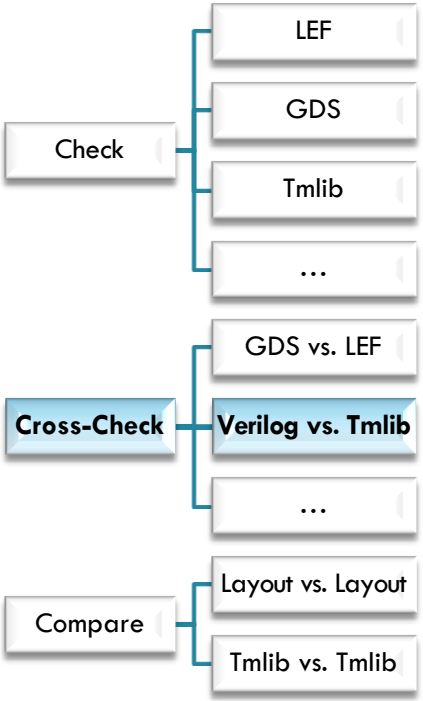
Timing .lib

```
cell (XNR3D1) {
  area : 4.2338;
  cell_footprint : "xnr3d1";

  pin(Z) {
    direction : output;
    function : "(!((A1^A2)^A3))";
    max_capacitance : 0.07452;
    timing () {
      related_pin : "A1";
      sdf_cond : "A2 == 1'b1 && A3 == 1'b0";
      timing_sense : positive_unate;
      timing_type : combinational;
      when : "A2&!A3";
      cell_rise (delay_template_7x7_0) {
        index_1 ("0.0017, 0.005, 0.0117, 0.025, 0.0515, 0.1047, 0.2109");
        index_2 ("0.00079, 0.00196, 0.0043, 0.00898, 0.01834, 0.03707, 0.07452");
        values ( \
```

Verilog

```
module XNR3D1 (A1, A2, A3, ZN, VDD, VSS);
    inout VDD;
    inout VSS;
    input A1, A2, A3;
    output ZN;
    xor (I0_out, A1, A2);
    xor (I1_out, I0_out, A3);
    not (ZN_pwr_net, I1_out);
    u_power_down_sum iZN (ZN, ZN_pwr_net, Vsum);
    not (nVSS, VSS);
    and (Vsum, VDD, nVSS);

  specify
    if (A2 == 1'b1 && A3 == 1'b0)
    (A1 => ZN) = (0, 0);
    if (A2 == 1'b0 && A3 == 1'b1)
    (A1 => ZN) = (0, 0);
    ...
  endspecify
endmodule
```

Verilog vs. Tmlib Cross-Check



- Pin function
- Arc and sdf_cond
- Timing check

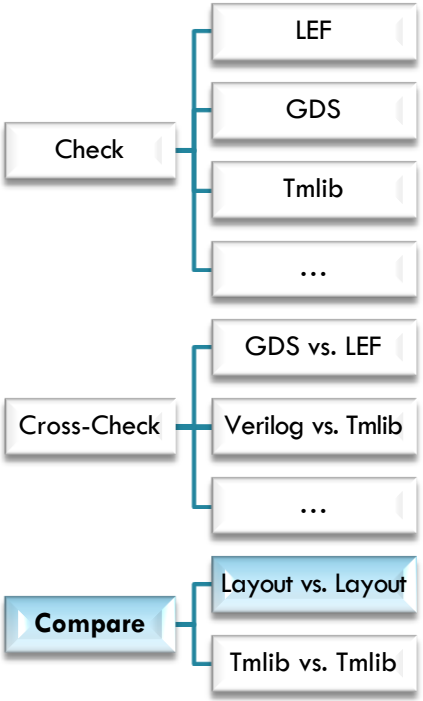
Timing .lib

```
cell (CKLNQD12) {
  ...
  pin(CP) {
    ...
    timing () {
      related_pin : "CP";
      sdf_cond : "E_NTE_SDFCHK";
      timing_type : min_pulse_width;
      when : "E&TE";
      rise_constraint (mpw_constraint_template_3x3) {
        index_1 ("0.0017, 0.025, 0.2109");
        values ( "0.01221, 0.03174, 0.2612" );
      }
      fall_constraint (mpw_constraint_template_3x3) {
        index_1 ("0.0017, 0.025, 0.2109");
        values ( "0.01221, 0.03174, 0.2612" );
      }
    }
```

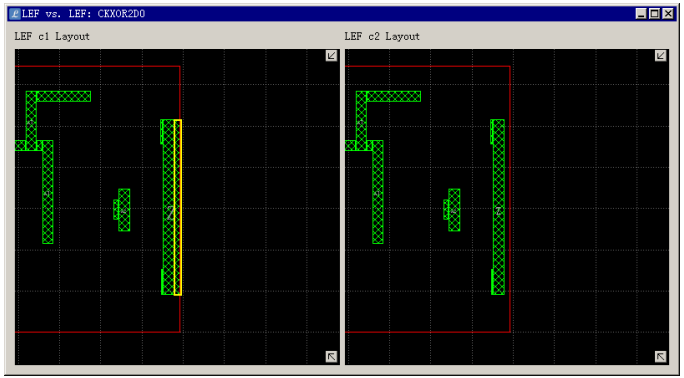
Verilog

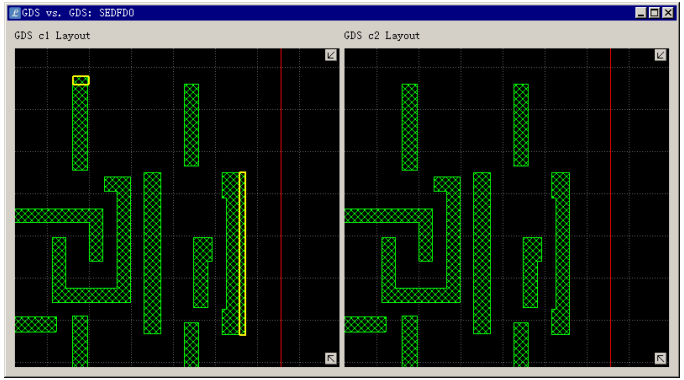
```
module CKLNQD12 (TE, E, CP, Q);
    input TE, E, CP;
    output Q;
    reg notifier;
    ...
  specify
    if (E == 1'b1 && TE == 1'b1)
    (CP => Q) = (0, 0);
    if (E == 1'b1 && TE == 1'b0)
    (CP => Q) = (0, 0);
    if (E == 1'b0 && TE == 1'b1)
    (CP => Q) = (0, 0);
    if (E == 1'b0 && TE == 1'b0)
    (negedge CP => (Q+:1'b0)) = (0, 0);

    $width (posedge CP &&& E_nTE_SDFCHK, 0, 0, notifier);
    $width (negedge CP &&& E_nTE_SDFCHK, 0, 0, notifier);
```

Compare Layout

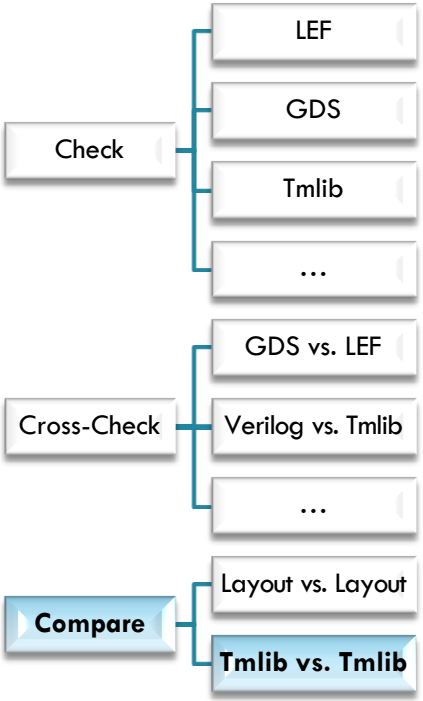


- Compare LEF
- Compare GDS

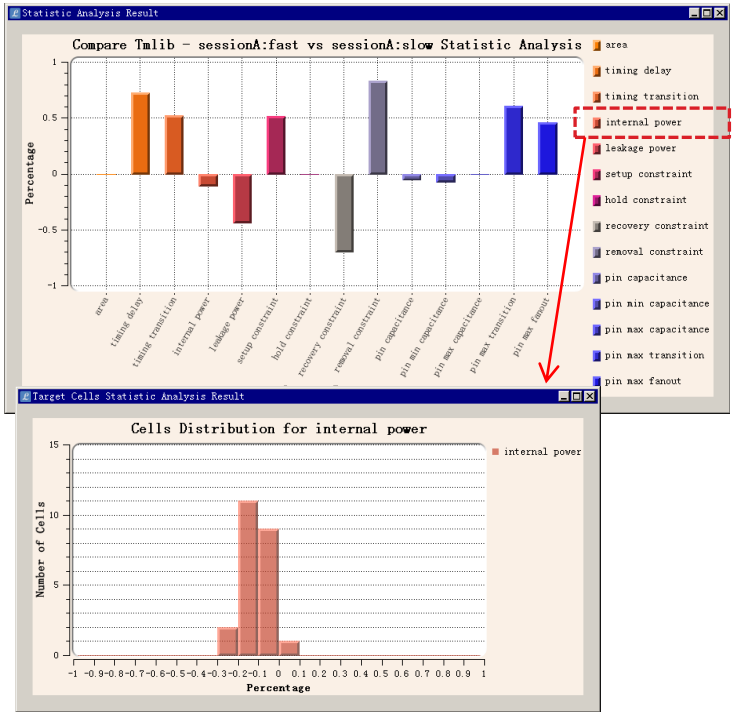




Compare Timing Lib

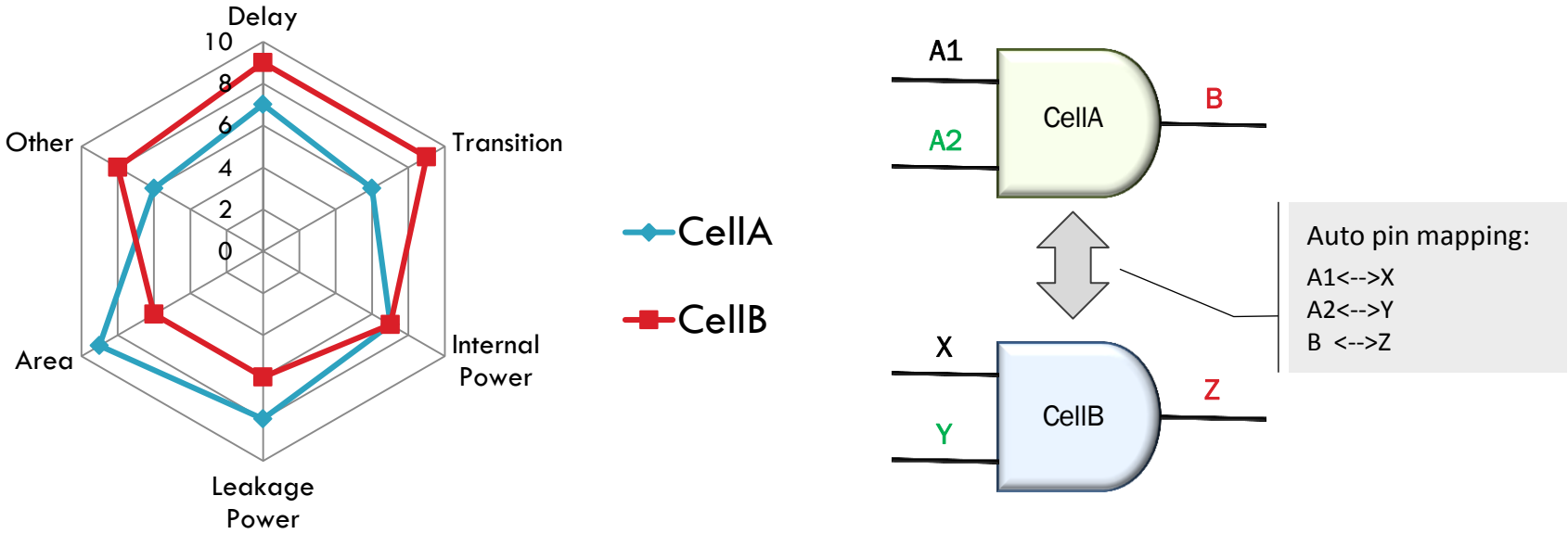


- Session vs. Session
  - Different vendors
  - Different versions
- Corner vs. Corner
- Cell vs. Cell

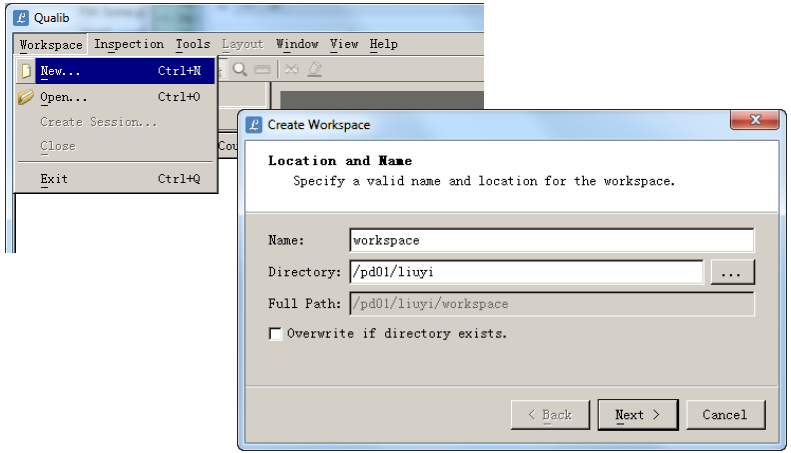


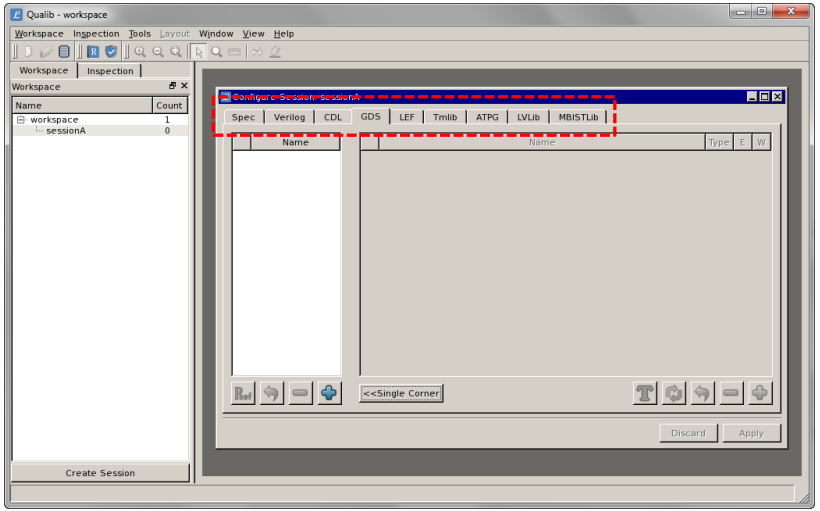
Intelligent Cell Comparison

- Cell PPA comparison between different vendors or versions

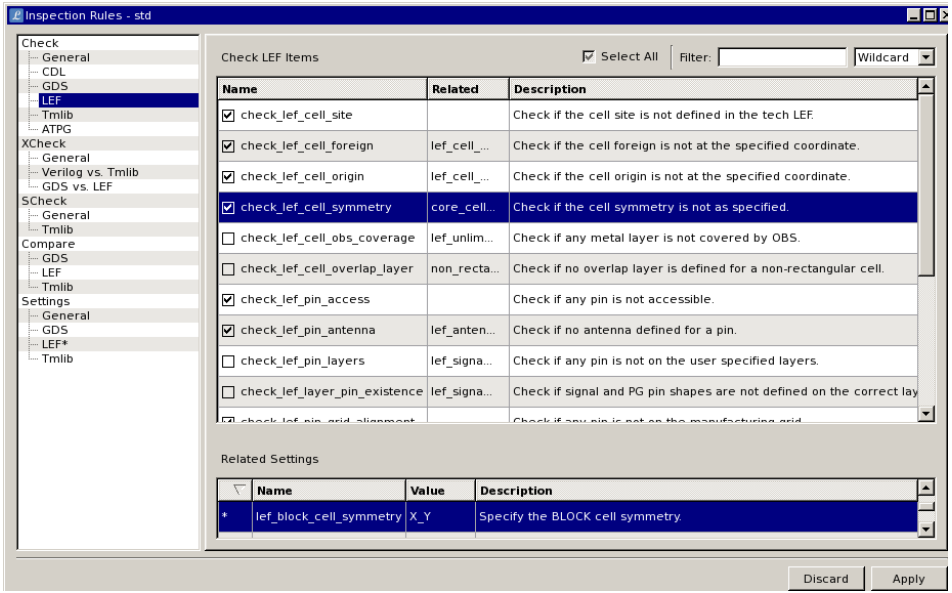


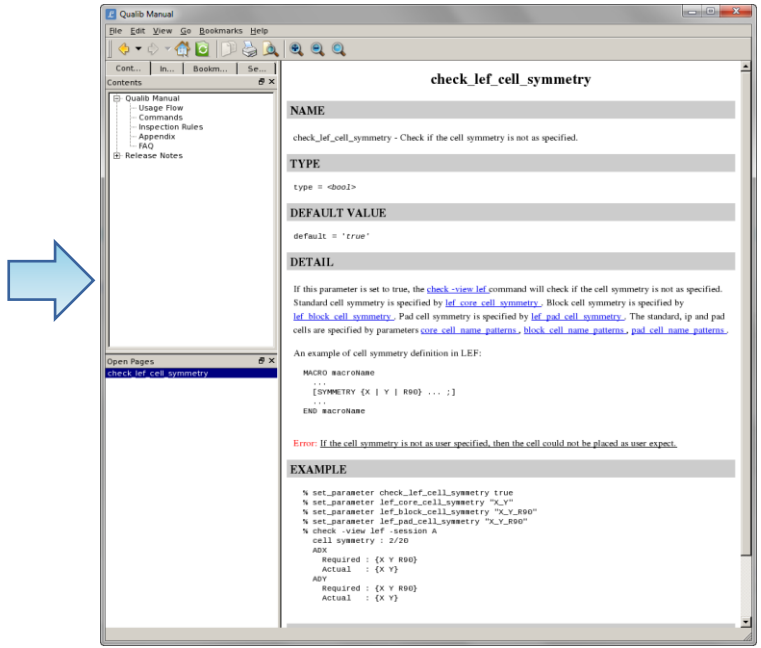
Usage Flow — *Input Files*



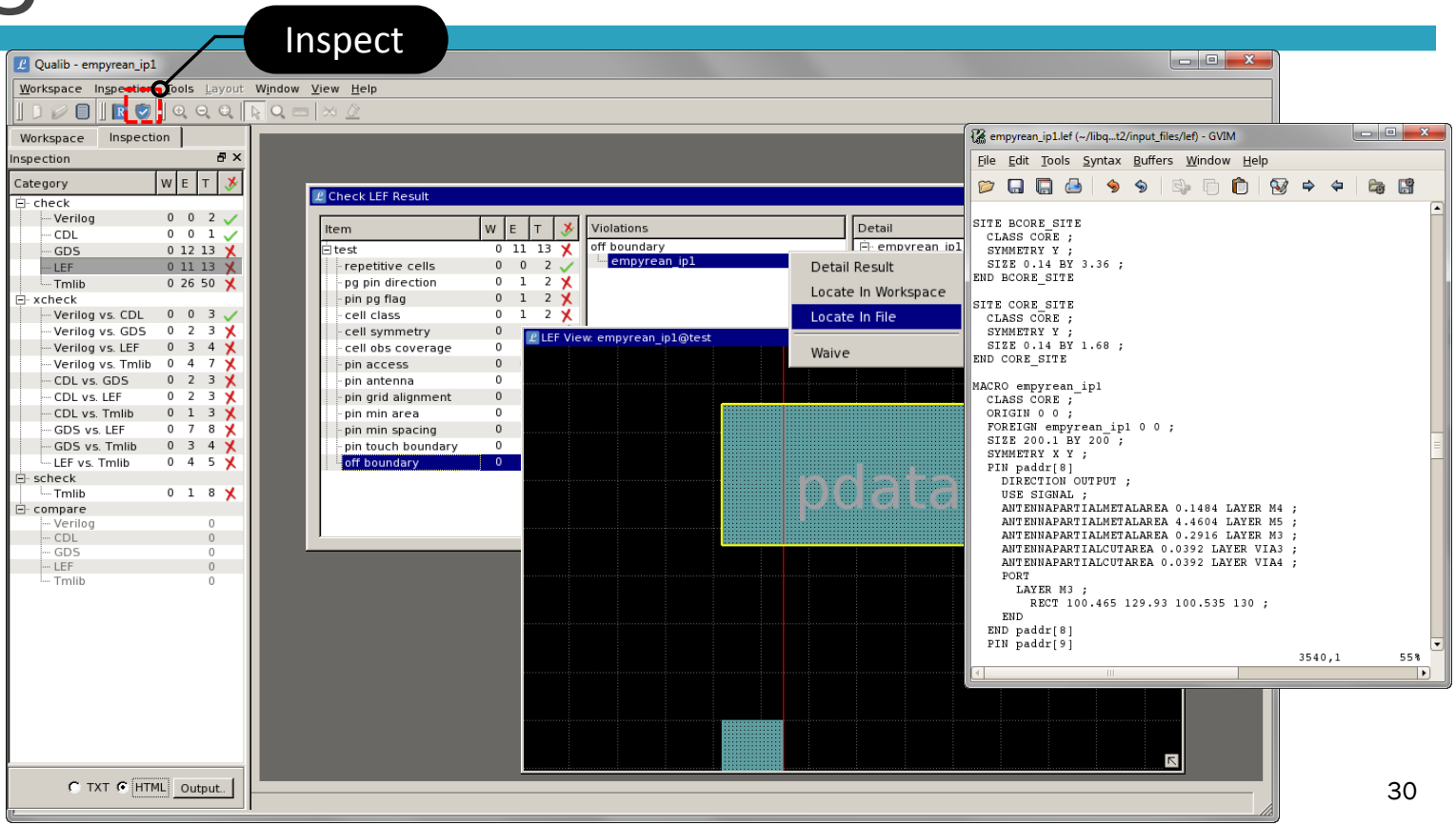


Usage Flow — *Configure Rules*

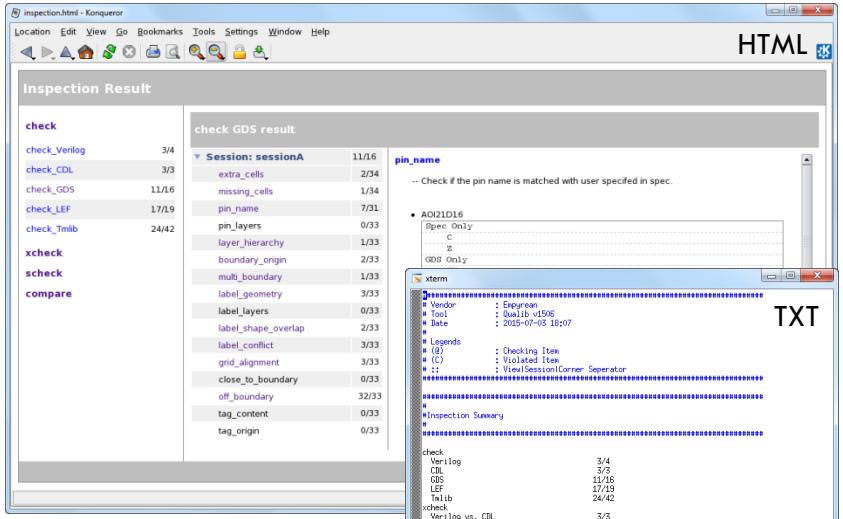


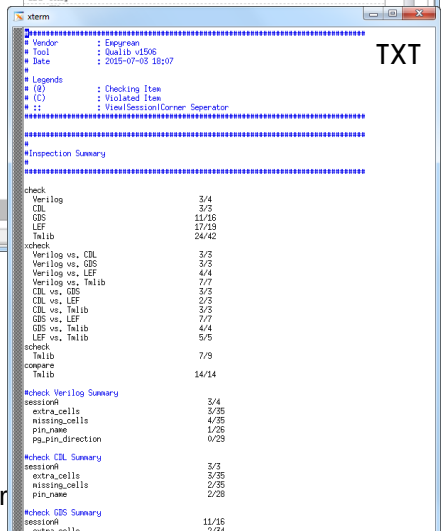


Usage Flow — *One-Click Check*

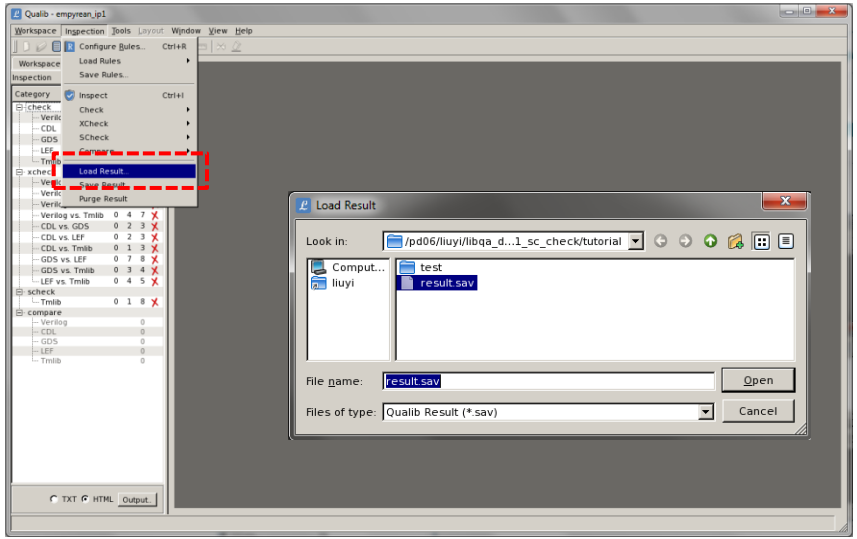


Usage Flow — *Reports*





- Restore the inspection result for further analysis



Qualib Updates

- V1512 Release
  - More library views integrated (ATPG, Mbist, lvlib …)
  - Support waive/unwaive check item and violated cell
  - Enhanced pin_access checking, avoid IP routablity problem
  - Added conflicting cell checking in GDS, avoid cell conflict due to IP merge
  - Added GDS precision uniqueness checking, avoid IP merge dbUnit conflict
  - Added more .lib checking items, such as power_down_function, noise table presence for ccs lib …

Summary

- A comprehensive platform to qualify IPs & standard cells
- Powerful interactive debugging functions for the source of problems
- Advanced analysis features for better IP & standard cell quality
- Flexible usage model and comprehensive reports

Thank You!