SRAM Stability Analysis Considering Gate Oxide SBD, NBTI and HCI

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ABSTRACT

For ultrathin gate oxide, soft breakdown (SBD) has been extensively studied but not fully integrated into circuit reliability simulation. Using a 6T SRAM cell as a generic circuit example, the time-dependent SBD was incorporated into circuit degradation analysis based on the exponential defect current growth model [1]. SRAM cell stability degradation due to individual failure mechanism was characterized. Multiple failure mechanisms degradation effect was also studied in regard of SRAM cell operation. Simulation results showed that gate oxide SBD is the dominating failure mechanism which causes SRAM stability and operation degradation, NBTI and HCI have much less effect.

Introduction

Soft breakdown (SBD) has acquired a great importance in the study of ultrathin gate oxides reliability. Previous SBD studies have been focused on understanding the physics and statistics [2]-[5], and the degradation effect at device level [6], [7]. As circuit reliability becomes more important, several works have been carried out to analyze the impact of SBD on circuit functionality [8]-[10]. However, without considering the circuit operation and correlating the SBD with stress time, those circuit level SBD degradation analyses only provided a static understanding of circuit functional degradation, which is not enough for circuit reliability modeling and prediction. Furthermore, two other prominent failure mechanisms, negative bias temperature instability (NBTI) and hot carrier injection (HCI) should also be considered in circuit reliability analysis, especially for advanced technologies.

To demonstrate the time-dependent SBD and multiple failure mechanisms degradation effect at circuit level, equivalent circuits are used to represent the degradation effect of each failure mechanisms in the circuit. Instance parameters of the equivalent circuits are correlated with the corresponding failure mechanism. Circuit functional degradation can be characterized through SPICE simulation.

SRAM was chosen as an example in this investigation because of its significant fraction in microprocessors, and its usage as a test vehicle in process development. A 6T SRAM cell was designed with 90nm technology. With a given application profile, multiple failure mechanisms degradations are estimated, and the SRAM cell stability and operation degradation are further characterized with regard to SBD, NBTI, HCI and their combined effect.

Failure Mechanism Equivalent Circuits

Various equivalent circuits have been proposed to represent the electrical effects of individual failure mechanism in circuit simulation. In this section, equivalent circuits used in our investigation will be mainly discussed.

Gate Oxide SBD

Gate current increase is one of the most important changes of device after gate oxide breakdown. Also, changes of threshold voltage and MOSFET transconductance have been observed for transistors with small width [6]. Most of the proposed SBD equivalent circuits are still focused on modeling of gate current increase. Kaczer et al. [11] constructed an equivalent circuit for an NFET with hard gate oxide breakdown by introducing one constant resistance R_{path} to represent the constant breakdown path, two adjacent NFETs, and two resistors R_{gs} and R_{gd} represent the resistance in the source and drain. For gate-to-diffusion breakdown, this equivalent circuit can be simplified to a circuit containing only R_{gs} (or R_{gd}) and the original transistor. Rodriguez et al. [12] developed an equivalent circuit which consists of voltage-dependent current sources between gate and drain or gate and source. The leakage current has a power law relationship with the stress voltage. Hosoi et al. [13] proposed another compact model by inserting two current sources I_{gc} and I_{gs} between the gate and the drain, and between the gate and the substrate, respectively. These gate oxide breakdown equivalent circuit models have been used for circuit function verifications at arbitrary breakdown levels and time.

A major problem of these previously proposed gate oxide breakdown equivalent circuits is they can not be used to simulate time dependent oxide degradation process as most commercial reliability simulators do for HCI and NBTI aging simulation. Inspired by the exponential I_g growth model recently proposed by Linder et al. [1], we proposed a new compact model which is poised to model the overall progress of oxide breakdown from the initial defect generation to SBD, and to final hard breakdown.

This new circuit model starts from the experimental observations of the exponential relation between defect current growth rate (GR) and gate stress voltage (V_g): GR increases exponentially with V_g at about 5 dec/V. This is mathematically equivalent to:

$$\ln(GR) = \alpha + \beta \cdot V_g \quad (1)$$

GR also scales with other device parameters including oxide thickness, channel length and substrate doping, while device area has no effect. Experimental results show GR increases one order of magnitude per 0.3 nm decrease of T_{ox}, so θ is about 1/0.3 with oxide thickness (T_{ox}) in nm. Here the equation:

$$\log_{10}(GR) = \gamma - \theta \cdot T_{ox} \quad (2)$$

Combing Equ. (1) and (2) together, GR can be generalized as

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$$GR = k_1 \cdot \exp(\beta \cdot V_g - \theta_1 \cdot T_{ox}) \quad (3)$$

where $\theta_1 = \ln(10) \cdot \theta$. The prefactor k_1 can be quantified by the time for the gate leakage current to grow from the initial oxide tunnel current I_0 (i.e. FN tunneling current I_{FN} for thick oxide, but direct tunneling current I_{DT} for ultra-thin oxide) to the gate current I_F at which circuit functions start to fail. I_F can be determined from circuit simulation by increasing gate leakage until circuit fails proper functionality. An arbitrary value of 100 uA is often used for I_F. I_0 can be determined from circuit fresh SPICE simulation at time 0 or by the classic FN tunneling equation for I_{FN} and the direct tunneling current model proposed in [14].

Experimental data shows defect current grows exponentially with stress time [1]. Put this in a mathematical formula, one can get:

$$I_g(t) = I_0 \cdot \exp(t \cdot GR) \quad (4)$$

With this I_g model (a function of stress voltage and stress time), it is easy to build a compact model for gate oxide SBD aging simulation. For the current source model, a simple voltage and time dependent current source can be added between MOSFET gate and drain (or source). The value of this current source is determined by the above I_g model and changes with stress time and voltage. Also, for the resistor equivalent circuit, the resistance can also be correlated with stress time. As a result, one can simulate oxide degradation process together with other MOSFET aging mechanisms to characterize the function and performance shift from MOSFET wearout effects.

For the 6T SRAM cell, there are three possible breakdown locations, pull-up PFET source, pull-down NFET source and PFET/NFET drain [8]. NFET source breakdown causes more severe cell stability degradation compared with breakdown at other locations. Experimental data showed that pull-down NFET transistor defects are the main cause of SRAM voltage sensitive failures [15]. Considering the facts above, we only model and simulate the pull-down NFET transistor gate-to-source SBD in this work. In order to provide a quick and good simulation, the resistor equivalent circuit is chosen and the circuit schematic is shown in Fig. 1.

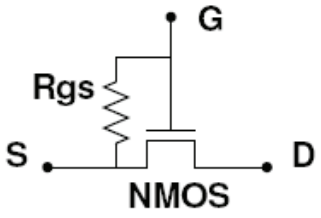


Fig. 1: NFET transistor SBD equivalent circuit.

The time dependent equivalent resistance R_{gs} can be expressed as:

$$R_{gs}(t) = \frac{V_{dd}}{I_0} \cdot \exp(-t \cdot GR) \quad (5)$$

where V_{dd} is the operating voltage, GR is the defect current growth rate under V_{dd} which can be estimated by Equ. (3).

HCI

Several HCI failure equivalent circuits have been developed, such as the parallel voltage-controlled current source for NFET in BERT [16], the two-transistor circuit in iSMILE [17] and the drain-side series resistance (ΔR_d model) in HISREM [18]. Among those equivalent circuits, the ΔR_d model provides a simple and efficient approach by requiring only one parameter (ΔN_{it}) for reliability simulation. In this model, based on the fact that the increase of HCI-induced series drain resistance is due to the injection of hot carriers close to the drain edge, a series resistance ΔR_d can be added to the drain of the NFET to emulate the process of hot carrier induced interface trap generation, the channel mobility reduction and threshold voltage drifts.

In this work, we applied the ΔR_d model to emulate the NFET HCI effect. The schematic of the equivalent circuit is shown in Fig. 2.

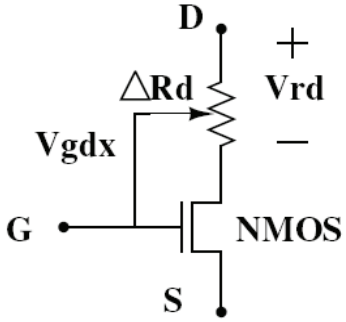


Fig. 2: NFET transistor HCI equivalent circuit.

Based on the derivation in [18], we used the saturation region equivalent resistance ΔR_d, which represents the worst case degradation effect.

$$\Delta R_d = \frac{1 + \alpha \Delta N_{it}}{I_{ds0}} \sqrt{\frac{V_{ds}^2 \alpha \Delta N_{it}}{1 + \alpha \Delta N_{it}} + \frac{2 V_{ds} \Delta N_{it} q}{C_{ox}}} \quad (6)$$

where α is a process dependent constant (~ 2.4E-12 cm^2 [19]), I_{ds0} is the drain current without HCI degradation. ΔN_{it} is the interface trapped charge.

$$\Delta N_{it} = B \cdot \exp(-\frac{\gamma_h}{V_{dd}}) \cdot t^{n_{hci}} \quad (7)$$

where B is a technology related constant, γ_h is the voltage acceleration parameter and n_{hci} is a constant.

NBTI

Although NBTI has been widely studied in recent years, little has been done to understand the circuit NBTI degradation effect through equivalent circuit. Considering the most obvious NBTI induced device degradation is the threshold voltage shift, a DC voltage source is utilized to represent the PMOS NBTI degradation. The equivalent circuit schematic is shown in Fig. 3.

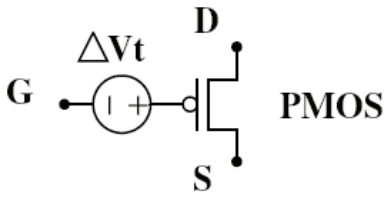


Fig. 3: PFET transistor NBTI equivalent circuit.

The threshold voltage degradation ΔV_{th} can be estimated by [20],

$$\Delta V_{th} = K_0 \cdot V_g^{\gamma_n} \cdot \exp(\frac{-E_a}{kT}) \cdot t^{n_{nbti}} \quad (8)$$

where K_0 is the prefactor, γ_n is the voltage acceleration parameter, E_a is the activation energy and n_{nbti} is the power law constant.

SRAM Cell Reliability Simulation

A single-bit 6T SRAM cell and its operation control circuits were designed with 90nm technology [21]. The gate oxide thickness is 1.4 nm and the power supply voltage is 1.2 V. The transfer ratio (width ratio of NFET M1 to pass-gate M5) of the SRAM cell is around 1.5. The function of the SRAM cell is simulated in SPICE to perform a set of sequential "write 0, read 0, write 1, read 1" operations. The duration of each operation is 2ns, and the cell is simulated for 8ns with an operation speed of 500MHz. Operation temperature is set to 27 ˚C. The cell is assumed to run the above operation sequential without stop.

With the given application profile, cell transistor stresses were characterized through SPICE simulation. Although transistors from M1 to M6 all suffer gate oxide breakdown stress, only the pull-down NFET transistor M1 was assumed to have gate oxide defect and the gate oxide SBD conduction was modeled by R1. This assumption is based on experiment results which showed most gate oxide defects can be attributed to defects on the pull-down transistors [15], and the ultra low probability of gate oxide defects of single transistor. Two pass-gate NFET transistors, M5 and M6, suffer bi-directional HCI stress during cell read and write. The degradation effect was modeled by resistors at both the drain and source side (R51 and R52 for M5, R61 and R62 for M6). For the two pull-up transistors, M3 and M4, the NBTI degradations are modeled by V3 and V4, respectively. Cell schematic with failure mechanism equivalent circuits is shown in Fig. 4.

For each cell transistor, the dynamic voltage stress profile was extracted from SPICE simulation output in order to characterize the degradations. With the given physics-of-failure models, stress duty factors (DFs) were estimated and the results are: 0.48 for M1 SBD, 0.48 for M3/M4 NBTI and 0.004 for M5/M6 HCI. Given the operation time, SBD, NBTI and HCI degradations can be estimated with Equ. (5), Equ. (8) and Equ. (6), respectively. For M1 SBD, the initial defect current I_0 was the direct tunneling current obtained from SPICE with a value of 1.1 nA. And the growth rate GR was assumed to be 9.0E-8/s based on the experimental results [1]. Other parameters were obtained from [21].

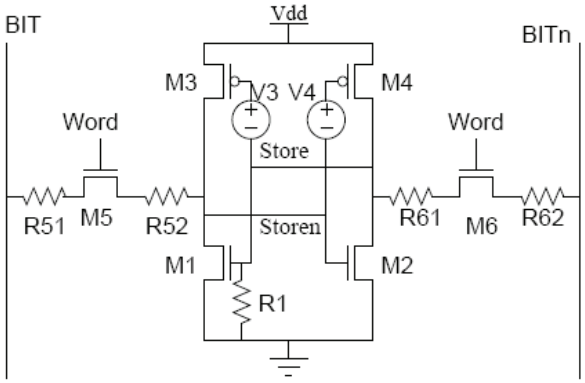


Fig. 4: Schematic of 1-bit 6T SRAM cell with failure mechanisms equivalent circuits. Store/Storen represents cell state. WORD line enables the two pass transistors M5 and M6.

SRAM Cell Stability Degradation: SBD and NBTI Effect

Static noise margin (SNM) [22] is often used to characterize the SRAM cell stability by drawing and mirroring the inverter characteristics and finding the maximum possible square between them. SNM degradations caused by SBD and NBTI are shown in Fig. 5 and Fig. 6, respectively.

For gate oxide SBD, SNM reduces from 384 mV at the fresh condition to 376 mV, 259 mV and 41 mV after 6, 8, 9 years operation, respectively. The SNM approaches zero at around 9.1 years, R1=15.0K for SBD degradation only.

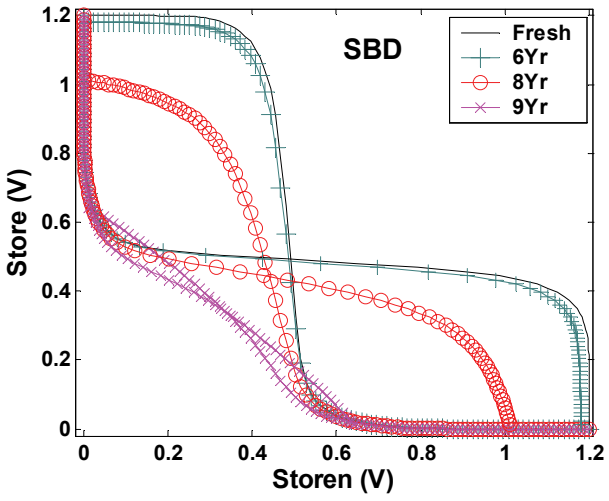


Fig. 5: SNM degradation caused by gate oxide SBD.

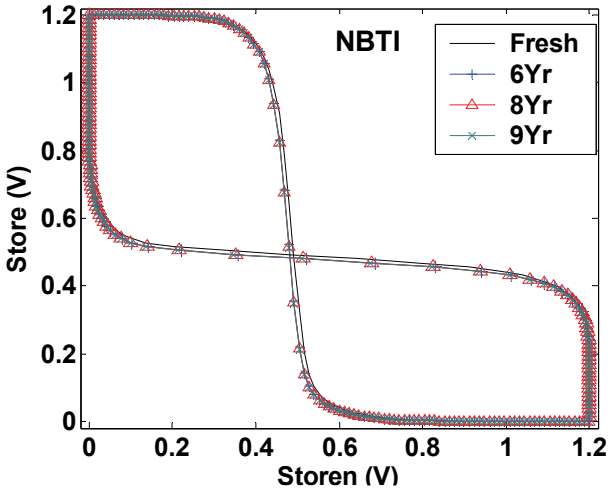


Fig. 6: SNM degradation caused by NBTI.

Compared Fig.5 with Fig. 6, we can see that SBD causes more detrimental degradation than NBTI in this investigation. Fig. 7 shows the SNM under SBD, NBTI and their combined effect, normalized to the SNM of the cell at fresh condition. It clearly shows that NBTI only causes very small SNM degradation. This is because threshold voltage shift is small in this case, and the shift slows down as time runs up. For M1 SBD only, the SNM degrades 33% and 90% after 8 and 9 years operation, respectively. These percentages change to 35% and 91% for the combined SBD and NBTI effect.

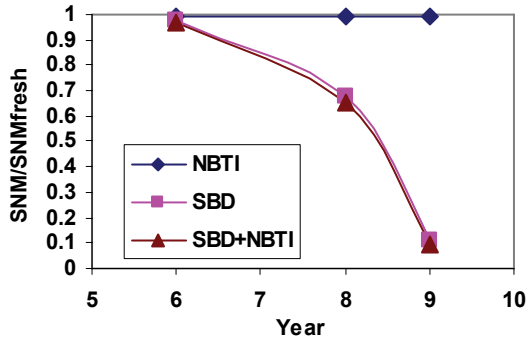
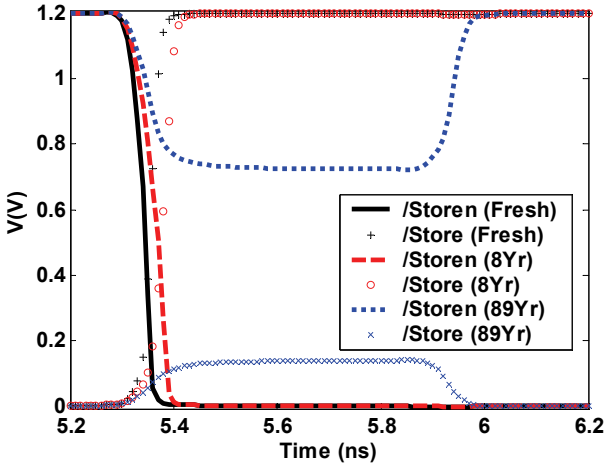


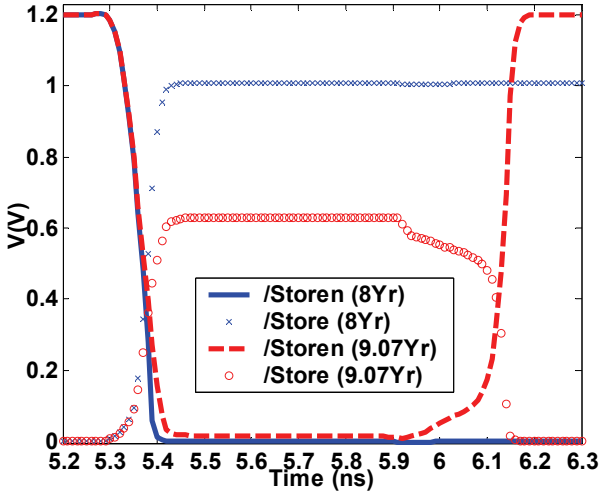
Fig. 7: Normalized SNM for SBD, NBTI and their combined effect.

Cell Operation Failure Caused By SBD, NBTI and HCI

Two pass-gate transistors, M5 and M6, suffer HCI the most because of the bi-directional stresses during read and write operation. Simulation results showed that HCI degradation affects the cell "write 1" operation, and it takes about 89 years to cause the failure as shown in Fig. 8 (a). Simulation results of the combined effect of SBD, NBTI and HCI is shown in Fig. 8 (b). "Write 1" operation failure happened at 9.07 years, which is a little bit earlier than the time SNM approaches zero due to SBD. From the simulation results, we can see that gate oxide SBD is still the dominating failure mechanism of SRAM cell stability and operation degradation.



(a) HCI



(b) SBD, NBTI and HCI

Fig. 8: "Store" and "Storen" during SRAM cell operation "Write 1". "Store" should be high after the operation. (a) HCI degradation effect. Simulation showed that operation fails after 89 years. (b) SBD, NBTI and HCI combined degradation effect. Simulation showed that operation fails at 9.07 years.

Summary

In this paper, SRAM cell reliability simulation is carried out by integrating the gate oxide SBD, NBTI and HCI through failure mechanism equivalent circuits. Gate oxide SBD is introduced into the circuit ageing simulation by modeling the defect current increase with an exponential growth model. Individual failure mechanism's effect on SRAM stability was simulated and compared. Multiple failure mechanisms degradation effect was also investigated through SRAM cell operation degradation analysis. Simulation results showed that SRAM cell stability and operation degradation is mostly caused by gate oxide SBD, NBTI and HCI play minor roles.

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Questions and Answers

Q: What did you assume for pull-up vs. pull-down strength?
A: 1.5X pull-down to pull-up so the bitcell is more write-limited. This could make it less susceptible to NBTI.

Q: The NBTI does not seem to realistic, have you verified on silicon?
A: Yes. The simulation was based on models and parameters provided by foundry. It could be different in other cases.

Q: What did you use for resistance after SBD?
A: The resistance is assumed to increase exponentially after SBD (Linder, IRPS 2003).

Q: Will your n and p assumptions impact your susceptibility to SBD and NBTI?
A: Yes.

Q: What are the values of the resistance you have been using in the SRAM cell for the 6 or 8 year?
A: R1 = 570Kohm at the 6 year, R1 = 55.8Kohm at the 8 year