Ver	Eff_Date	ECN No.	Author	Change Description
1.0P2	11-23-16	E120201647283	K. C. Huang (EMPED)	Merge T-N16-CL-CL-022 SHD/SHC document & Update SRAM ver 1.0 demo array (add alignment mark)
1.0P1	05-24-16	E120201621128	K. C. Huang (EMPED)	Release ver 1.0 SRAM SPICE model
0.9P1	11-14-15	E120201546247	K. C. Huang (EMPED)	Original (Release ver 0.9_2p1 SRAM SPICE model card and SRAM ver 1.0 demo array)

Approvals :

Please refer EDW workflow to see detail approval records

Title

TSMC 16 NM CMOS LOGIC FINFET COMPACT 1P13M HKMG CU_ELK LL 0.85V SP/2P8T/DP/SHD/SHC SRAM CELL LAYOUT & MODEL 16FFC-LL

Document No. : T-N16-CL-CL-021

Contents : 27
Attach. : 0
Total : 27

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TSMC 16 NM CMOS LOGIC FINFET COMPACT 1P13M HKMG CU_ELK LL 0.85V SP/2P8T/DP/SHD/SHC SRAM CELL LAYOUT & MODEL 16FFC-LL

It includes:

1. Introduction:

Here are the SRAM bit cells, which are listed in table 1, offered by TSMC for customer's design. The corresponding process is 16nm (CLN16FFC-LL) 1P13M embedded SRAM. The description and requirement of all SRAM cell and related strap/edge cells are shown here. No layout change is allowed because process margin are very sensitive and strongly layout dependent.

Bit Cell Type	Drawn cell size (um ^2)*	Operation Voltage(V)	Bit cell version	Model Version	Demo Array GDS Filename
6T single port SRAM	0.0734	0.85	1.0	1.0_2p1	16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020_AM.gds
	0.0907	0.85	1.0	1.0_2p1	
	0.108	0.85	1.0	1.0_2p1	
6T SP SHD	0.0690	0.85	1.0	1.0_2p1	
6T SP SHC	0.0864	0.85	1.0	1.0_2p1	
2 port 8T SRAM	0.130	0.85	1.0	1.0_2p1	
	0.138	0.85	1.0	1.0_2p1	
	0.147	0.85	1.0	1.0_2p1	
dual port 8T SRAM	0.194	0.85	1.0	1.0_2p1	

*Notice: The cell size showed in the table is drawn size.

[Table.1] Summary of SRAM cells included in this document

1.1 Change list

The updated demo array (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds, 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020_AM.gds) including one additional layer DUMMY0_18 (83;18) as alignment mark layer for placement check. The others are the same as original gds.

	Original gds	Update gds
GDS file name	16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016.gds 16FF_demo_arrays_v1d0_with_BL_tracking_for_T_N16_CL015_016.gds 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020.gds	16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds 16FF_demo_arrays_v1d0_with_BL_tracking_for_T_N16_CL015_016_AM.gds 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020_AM.gds
CAD Layer different		DUMMY0_18(83;18)

[Table.2] GDS list of SRAM cells included in this document

Customers should sign "**License Agreement**" to apply for this document.

These layouts are GDS format database.

v1d0 demo arrays are the same with v0d2 demo arrays.

2. Special concern for SRAM

(1) All SRAM unit cells are split-word-line (SWL) type SRAM.

(2) General and special purpose layers and their usages are listed in section 6. These layers must be included inside relative SRAM cells.

(3) For Pwell, Nwell pickup, TSMC suggests the distance between straps is within 60um.

(4) For BL loading, it is requested putting no more than 256 bits per bit line except SP & DP. The BL loading is 8~256.

(5) Customers are requested to consider WL resistance when deciding cell numbers per WL.

(6) There are different SRAM strap cell designs in standard offering. Please refer to SRAM cell summary table in [3-3].

(7) In Metal-2/Via-1, TSMC standard offering gds is Mxa/Vxa process. Customer needs to change Metal-2/Via-1 datatype 70 to datatype 0 if using Mx/Vx process.

(8) Customers must be responsible to check and use the latest version of SRAM to tape out.

3. Layout Guideline:

[3-1] Guideline for cell array architecture

To avoid error during cell array construction, customers must follow the rules below.

1. All Layers, in bitcell and accessory cells cannot be modified or removed.
2. The hierarchy and orientation of every bitcell and sub cells must be kept the same. Cell name needs to be kept the same as tsmc offered leaf cells.
3. For test line purpose, all BEOL OPC layers (Layer 159 data type 102~103, Layer 31 data type 102~103, Layer 51 data type 102~103, Layer 32 data type 102~103) have to be removed when the related main BEOL layers (Layer 159 data type 0, Layer 31 data type 0, Layer 51 data type 70, Layer 32 data type 70) are modified/added/deleted in a single SRAM array. For example, when a Via0 is removed, all of the Via0 OPC layers have to be removed in the array.

[3-2] Guideline for cell layout at edge of cell array

Because unit cell doesn't fulfill layout requirement along cell boundary, dedicated edge/strap corner cells must be used around SRAM bitcell. Customers are reminded not to violate design rules (Document No.T-N16-CL-DR-002) at cell array edge. Please refer to example attached in GDS format and relative cell names are listed in the following tables, taking 4x4 demo array for example. It is requested to use TSMC standard dummy cells and strap cells because they are strongly process related. The IP tag is for TSMC SRAM version control. Any modification of the IP tags or additional tags start with the same prefix are not allowed.

For SP-HD (0.0734um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds, array name: 16FF_d0734_v1d0_array_4x4_sep_wells_and_Vss_AM, cell name: 16FF_d0734_v1d0_x4, strapping cell name: 16FF_d0734_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_d0734_v1d0_strap_dummy_sep_wells_x1_r_AM, X edge cell name: 16FF_d0734_v1d0_row_edge_sep_Vss_x2_l_AM and 16FF_d0734_v1d0_row_edge_sep_Vss_x2_r_AM, edge strapping cell name: 16FF_d0734_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_d0734_v1d0_strap_dummy_sep_wells_x1_r_AM, and the corner dummy cell name: 16FF_d0734_v1d0_corner_dummy_sep_wells_x1_l_AM and 16FF_d0734_v1d0_corner_dummy_sep_wells_x1_r_AM).

For SP-HC (0.0907um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds, array name: 16FF_d0907_v1d0_array_4x4_sep_wells_and_Vss_AM, cell name: 16FF_d0907_v1d0_x4_AM, strapping cell name: 16FF_d0907_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_d0907_v1d0_strap_dummy_sep_wells_x1_r_AM, X edge cell name: 16FF_d0907_v1d0_row_edge_sep_Vss_x2_l_AM and 16FF_d0907_v1d0_row_edge_sep_Vss_x2_r_AM, edge strapping cell name: 16FF_d0907_v1d0_strap_dummy_sep_wells_x1_l_AM and

16FF_d0907_v1d0_strap_dummy_sep_wells_x1_r_AM, and the corner dummy cell name:
16FF_d0907_v1d0_corner_dummy_sep_wells_x1_l_AM and
16FF_d0907_v1d0_corner_dummy_sep_wells_x1_r_AM).

For SP-HP (0.108um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds, array name: 16FF_d108_v1d0_array_4x4_sep_wells_AM, cell name: 16FF_d108_v1d0_x4_AM, strapping cell name: 16FF_d108_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_d108_v1d0_strap_dummy_sep_wells_x1_r_AM, X edge cell name: 16FF_d108_v1d0_row_edge_sep_Vss_x2_l_AM and 16FF_d108_v1d0_row_edge_sep_Vss_x2_r_AM, edge strapping cell name: 16FF_d108_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_d108_v1d0_strap_dummy_sep_wells_x1_r_AM, and the corner dummy cell name: 16FF_d108_v1d0_corner_dummy_sep_wells_x1_l_AM and 16FF_d108_v1d0_corner_dummy_sep_wells_x1_r_AM).

For 2P_8T MUXN (0.130 um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds, array name: 16FF_2P_d130_v1d0_array_4x4_sep_wells_AM, cell name: 16FF_2P_d130_v1d0_x4_AM, strapping cell name: 16FF_2P_d130_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_2P_d130_v1d0_strap_dummy_sep_wells_x1_r_AM, X edge cell name: 16FF_2P_d130_v1d0_row_edge_sep_Vss_x2_l_AM and 16FF_2P_d130_v1d0_row_edge_sep_Vss_x2_r_AM, edge strapping cell name: 16FF_2P_d130_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_2P_d130_v1d0_strap_dummy_sep_wells_x1_r_AM, and the corner dummy cell name: 16FF_2P_d130_v1d0_corner_dummy_sep_wells_x1_l_AM and 16FF_2P_d130_v1d0_corner_dummy_sep_wells_x1_r_AM).

For 2P_8T HC MUXN (0.138 um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds, array name: 16FF_2P_d138_v1d0_array_4x4_sep_wells_AM, cell name: 16FF_2P_d138_v1d0_x4_AM, strapping cell name: 16FF_2P_d138_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_2P_d138_v1d0_strap_dummy_sep_wells_x1_r_AM, X edge cell name: 16FF_2P_d138_v1d0_row_edge_sep_Vss_x2_l_AM and 16FF_2P_d138_v1d0_row_edge_sep_Vss_x2_r_AM, edge strapping cell name: 16FF_2P_d138_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_2P_d138_v1d0_strap_dummy_sep_wells_x1_r_AM, and the corner dummy cell name: 16FF_2P_d138_v1d0_corner_dummy_sep_wells_x1_l_AM and 16FF_2P_d138_v1d0_corner_dummy_sep_wells_x1_r_AM).

For 2P_8T HS MUXN (0.147 um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds, array name: 16FF_2P_d147_v1d0_array_4x4_sep_wells_AM, cell name: 16FF_2P_d147_v1d0_x4_AM, strapping cell name: 16FF_2P_d147_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_2P_d147_v1d0_strap_dummy_sep_wells_x1_r_AM, X edge cell name: 16FF_2P_d147_v1d0_row_edge_sep_Vss_x2_l_AM and 16FF_2P_d147_v1d0_row_edge_sep_Vss_x2_r_AM, edge strapping cell name: 16FF_2P_d147_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_2P_d147_v1d0_strap_dummy_sep_wells_x1_r_AM, and the corner dummy cell name: 16FF_2P_d147_v1d0_corner_dummy_sep_wells_x1_l_AM and 16FF_2P_d147_v1d0_corner_dummy_sep_wells_x1_r_AM).

For DP_HC (0.194 um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds, array name: 16FF_DP_F_d194_v1d0_array_4x4_sep_wells_AM, cell name: 16FF_DP_F_d194_v1d0_x4_AM, strapping cell name: 16FF_DP_F_d194_v1d0_BL_twist_and_sep_wells_strap_x2_AM, X edge cell name: 16FF_DP_F_d194_v1d0_row_edge_twist_x2_AM and 16FF_DP_F_d194_v1d0_row_edge_x2_AM, edge strapping cell name: 16FF_DP_F_d194_v1d0_sep_wells_strap_edge_twist_x2_AM and 16FF_DP_F_d194_v1d0_sep_wells_strap_edge_x2_AM, and the corner dummy cell name: 16FF_DP_F_d194_v1d0_corner_dummy_sep_wells_x1_AM).

For SP-SHD (0.069um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020_AM.gds, array name: 16FF_d0690_v1d0_array_4x4_sep_wells_and_Vss_AM, cell name: 16FF_d0690_v1d0_x4_AM, strapping cell name: 16FF_d0690_ v1d0_sep_wells_strap_x2_AM, strapping edge cell name: 16FF_d0690_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_d0690_v1d0_strap_dummy_sep_wells_x1_r_AM, X edge cell name: 16FF_d0690_v1d0_row_edge_sep_Vss_x2_l_AM and 16FF_d0690_v1d0_row_edge_sep_Vss_x2_r_AM, edge strapping cell name: 16FF_d0690_v1d0_ sep_wells_strap_edge_x2_AM, and the corner dummy cell name: 16FF_d0690_v1d0_corner_dummy_sep_wells_x1_l_AM and 16FF_d0690_v1d0_corner_dummy_sep_wells_x1_r_AM).

For SP-SHC (0.0864um^2) 1P2M (1 Poly with 2 metal layers) standard cell, please refer to example attached in GDS format (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020_AM.gds, array name: 16FF_d0864_v1d0_array_4x4_sep_wells_and_Vss_AM, cell name: 16FF_d0864_v1d0_x4_AM, strapping cell name: 16FF_d0864_v1d0_sep_wells_strap_x2_AM, strapping

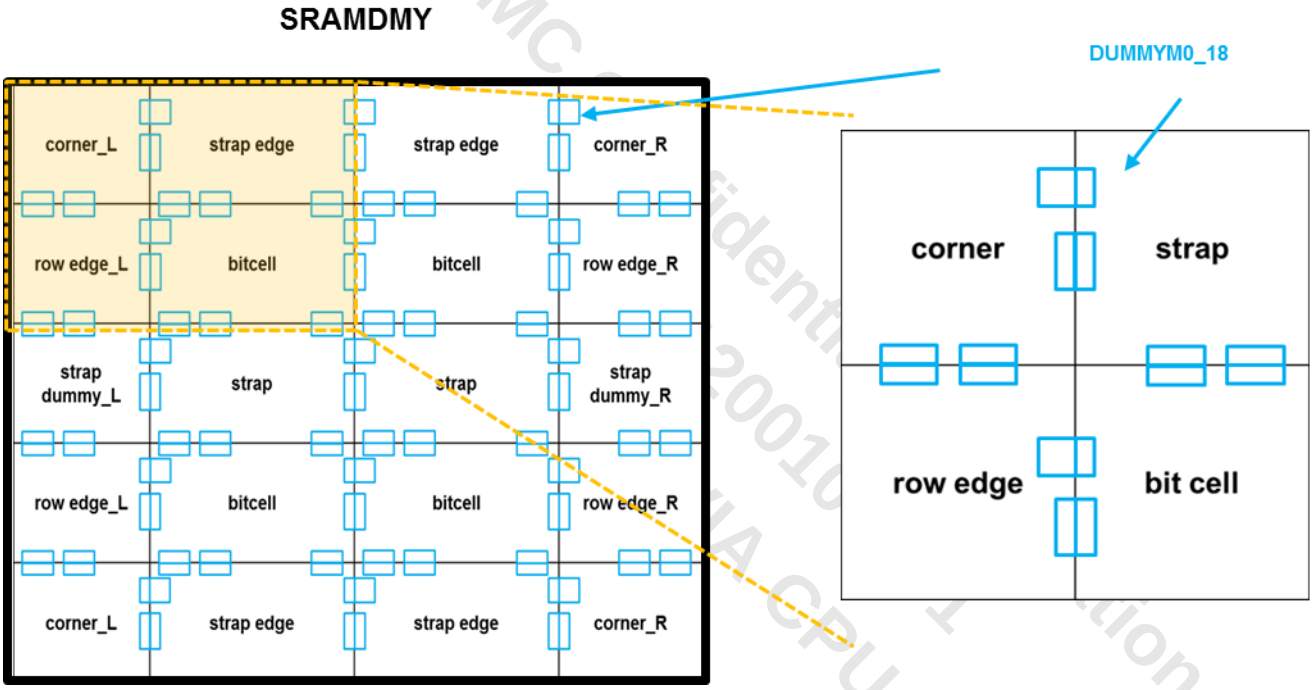
edge cell name: 16FF_d0864_v1d0_strap_dummy_sep_wells_x1_l_AM and 16FF_d0864_v1d0_strap_dummy_sep_wells_x1_r_AM, X edge cell name: 16FF_d0864_v1d0_row_edge_sep_Vss_x2_l_AM and 16FF_d0864_v1d0_row_edge_sep_Vss_x2_r_AM, edge strapping cell name: 16FF_d0864_v1d0_ sep_wells_strap_edge_x2_AM, and the corner dummy cell name: 16FF_d0864_v1d0_corner_dummy_sep_wells_x1_l_AM and 16FF_d0864_v1d0_corner_dummy_sep_wells_x1_r_AM).

For the other type cell metal routing, customers could refer to the below table and cell document package.

[3-3] Guideline for Strapping and Dummy Cell

(1) In corner edge, row edge and strap edge, please follow TSMC standard demo array method, any change is not allowed because they are strongly process related.

(2) With alignment mark array (GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds & 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020_AM.gds), DUMMY0_18 (layer 83 data type 18) is used to construct alignment mark and detection by DRC (ex: rule SRAM.R.49 and SRAM.R.49.1). Please refer to below plot.



(3) Recommend customer to create identical array configuration as TSMC demo array and do the LVL to confirm the correct usage.

(4) There are several well strap and power connection cell designs in standard offering. Please refer to below table for different design purpose.

(5) It is allowed to extend SP & DP cells Max bit line loading to 512 bits per BL, the other cells Max bit line loading please refer below table.

gds name: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016.gds & 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds

HD (16FF_d0734_v1d0_)	array_4x4 _common_power	array_4x4 _for_LCV	array_4x4 _sep_Nwell	array_4x4 _sep_wells_and_Vss	array_5Cx4R _common_power	array_5Cx4R _for_LCV	array_5Cx4R _sep_Nwell	array_5Cx4R _sep_wells_and_Vss
WL Metal Layer	M2	M2	M2	M2	M2	M2	M2	M2
BL Metal Layer	M1	M1	M1	M1	M1	M1	M1	M1
Vdd and Nwell Connection	Y	Separate	Separate	Separate	Y	Separate	Separate	Separate
Vbb and Vss Connection	Y	Y	Y	Separate	Y	Y	Y	Separate
Vdd tie together	Y	N	Y	N	Y	N	Y	N
Max bits per BL	512	512	512	512	512	512	512	512
HC (16FF_d0907_v1d0_)	array_4x4 _common_power	array_4x4 _for_LCV	array_4x4 _sep_Nwell	array_4x4 _sep_wells_and_Vss	array_5Cx4R _common_power	array_5Cx4R _for_LCV	array_5Cx4R _sep_Nwell	array_5Cx4R _sep_wells_and_Vss
WL Metal Layer	M2	M2	M2	M2	M2	M2	M2	M2
BL Metal Layer	M1	M1	M1	M1	M1	M1	M1	M1
Vdd and Nwell Connection	Y	Separate	Separate	Separate	Y	Separate	Separate	Separate
Vbb and Vss Connection	Y	Y	Y	Separate	Y	Y	Y	Separate
Vdd tie together	Y	N	Y	N	Y	N	Y	N
Max bits per BL	512	512	512	512	512	512	512	512
HP (16FF_d108_v1d0_)	array_4x4 _common_power	array_4x4 _for_LCV	array_4x4 _sep_Nwell	array_4x4 _sep_wells	array_5Cx4R _common_power	array_5Cx4R _for_LCV	array_5Cx4R _sep_Nwell	array_5Cx4R _sep_wells
WL Metal Layer	M2	M2	M2	M2	M2	M2	M2	M2
BL Metal Layer	M1	M1	M1	M1	M1	M1	M1	M1
Vdd and Nwell Connection	Y	Separate	Separate	Separate	Y	Separate	Separate	Separate
Vbb and Vss Connection	Y	Y	Y	Separate	Y	Y	Y	Separate
Vdd tie together	Y	N	Y	N	Y	N	Y	N
Max bits per BL	512	512	512	512	512	512	512	512
8T2P_2FIN (16FF_2P_d130_v1d0_)	array_4x4 _common_power	array_4x4 _separate_RBL	array_4x4 _sep_Nwell	array_4x4 _sep_wells	array_5Cx4R _common_power	array_5Cx4R _sep_wells	array_5Cx4R _sep_Nwell	
WL Metal Layer	M2	M2	M2	M2	M2	M2	M2	
BL Metal Layer	M1	M1	M1	M1	M1	M1	M1	
Vdd and Nwell Connection	Y	Y	Separate	Separate	Y	Separate	Separate	
Vbb and Vss Connection	Y	Y	Y	Separate	Y	Separate	Y	
Vdd tie together	Y	Y	Y	N	Y	N	Y	
Max bits per BL (write)	256	256	256	256	256	256	256	
Max bits per BL (read)	32	32	32	32	32	32	32	
8T2P_3FIN (16FF_2P_d138_v1d0_)	array_4x4 _common_power	array_4x4 _separate_RBL	array_4x4 _sep_Nwell	array_4x4 _sep_wells	array_5Cx4R _common_power	array_4x4 _s_RVss	array_5Cx4R _sep_Nwell	array_5Cx4R _sep_wells
WL Metal Layer	M2	M2	M2	M2	M2	M2	M2	M2
BL Metal Layer	M1	M1	M1	M1	M1	M1	M1	M1
Vdd and Nwell Connection	Y	Y	Separate	Separate	Y	Y	Separate	Separate
Vbb and Vss Connection	Y	Y	Y	Separate	Y	Y	Y	Separate
Vdd tie together	Y	Y	Y	N	Y	Y	Y	N
Max bits per BL (write)	256	256	256	256	256	256	256	256
Max bits per BL (read)	32	32	32	32	32	32	32	32
8T2P_4FIN (16FF_2P_d147_v1d0_)	array_4x4 _common_power	array_4x4 _separate_RBL	array_4x4 _sep_Nwell	array_4x4 _sep_wells	array_5Cx4R _common_power	array_5Cx4R _sep_wells	array_5Cx4R _sep_Nwell	
WL Metal Layer	M2	M2	M2	M2	M2	M2	M2	
BL Metal Layer	M1	M1	M1	M1	M1	M1	M1	
Vdd and Nwell Connection	Y	Y	Separate	Separate	Y	Separate	Separate	
Vbb and Vss Connection	Y	Y	Y	Separate	Y	Separate	Y	
Vdd tie together	Y	Y	Y	N	Y	N	Y	
Max bits per BL (write)	256	256	256	256	256	256	256	
Max bits per BL (read)	32	32	32	32	32	32	32	
HCDP (16FF_DP_F_d194_v1d0_)	array_4x4 _common_power	array_4x4 _sep_Nwell	array_5Cx4R _sep_Nwell	array_4x4 _sep_wells	array_5Cx4R _common_power	array_5Cx4R _sep_wells		
WL Metal Layer	M2	M2	M2	M2	M2	M2		
BL Metal Layer	M1	M1	M1	M1	M1	M1		
Vdd and Nwell Connection	Y	Separate	Separate	Separate	Y	Separate		
Vbb and Vss Connection	Y	Y	Y	Separate	Y	Separate		
Vdd tie together	Y	Y	Y	Y	Y	Y		
Max bits per BL	512	512	512	512	512	512	512	512

SPSHD (16FF_d0690_v0d2_)	array_4x4_for_ LCV	array_4x4_sep_w ells_and_Vss	SPSHC (16FF_d0864_v0d2_)	array_4x4_for_ LCV	array_4x4_sep_w ells_and_Vss
WL Metal Layer	**M2**	**M2**	**WL Metal Layer**	**M2**	**M2**
BL Metal Layer	**M1**	**M1**	**BL Metal Layer**	**M1**	**M1**
Vdd and Nwell Connection	**Separate**	**Separate**	**Vdd and Nwell Connection**	**Separate**	**Separate**
Vbb and Vss Connection	**Y**	**Separate**	**Vbb and Vss Connection**	**Y**	**Separate**
Vdd Tie Together	**N**	**N**	**Vdd Tie Together**	**N**	**N**

(6) If there is any special requirement such as ultra high speed, chip size, customers can arrange strapping frequency and metal space that based on TSMC design rule and SPICE model.

(7) Some dummy devices are formed due to the overlap of dummy OD and dummy Poly. If the dummy device has only one source/drain, there is no leakage path concern. Then the device is covered by RODMY (49;0) to waive this device in LVS check. If the dummy device has complete 4 terminals, leakage path may be created. So RODMY is not covered on these devices to allow LVS check. Customers should include those devices into netlist description.

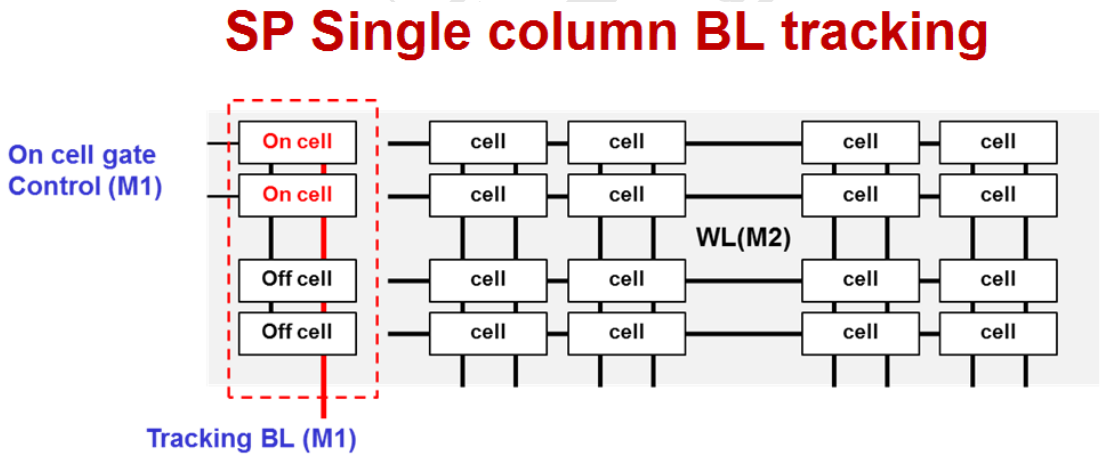
[3-4] Guideline for Tracking Circuit (Reference layout)

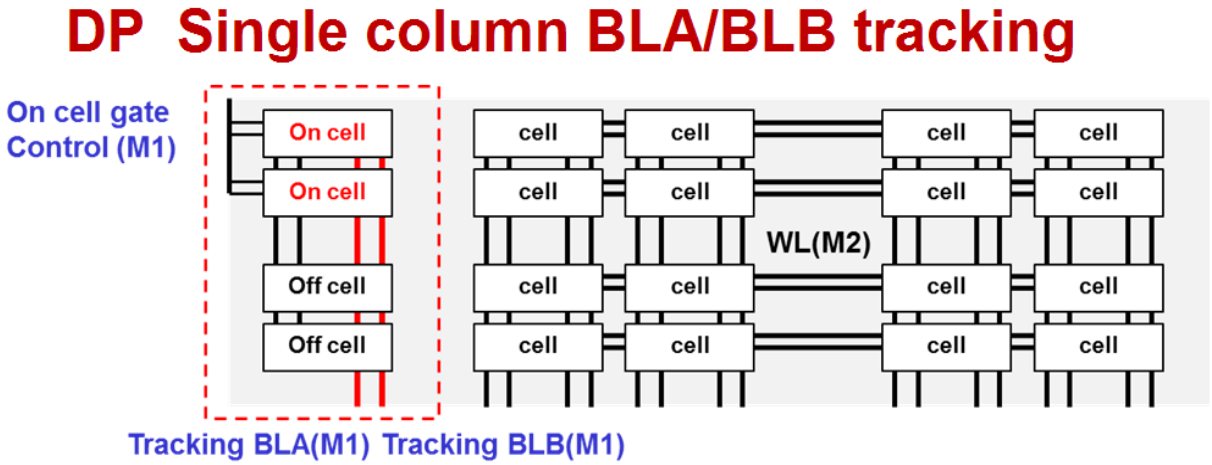
Tracking circuit is a tuning design to optimize speed performance.

(1) Any tracking circuit design not using SRAM cell layout must fully comply with standard logic rules (T-N16-CL-DR-002). Tracking circuit design must be reviewed by TSMC before tape out. Customers must take care of the performance difference between logic-rule-based tracking circuit and real SRAM.

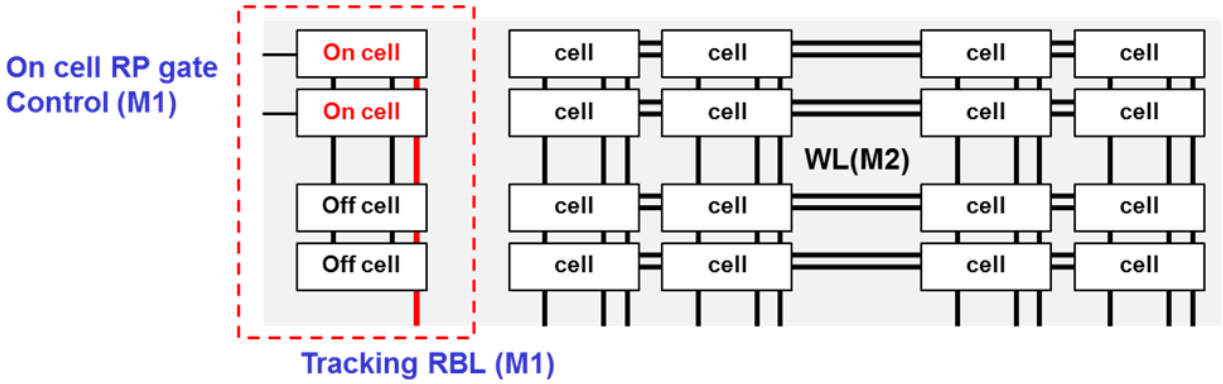
(2) For tracking circuit design with pure SRAM cell, please refer to TSMC tracking circuit demo array. Gds file : 16FF_demo_arrays_v1d0_with_BL_tracking_for_T_N16_CL015_016.gds
v1d0 demo array with BL tracking gds is the same with vd2 demo array with BL tracking gds.

(3) Brief BL tracking circuit plot





2P_8T Single column RBL tracking



4. Design Guideline

(1) Customers need to consider process variation into design margin to get stable yield in production.

(2) The logic and SRAM device variations have to be taken into consideration to reserve enough design margin (such as bitline differential voltage). It is especially important for the design using logic delay to generate sense amplifier timing control signal. Silicon validation with skewed logic/SRAM split is suggested.

(3) For single-ended read design, the access time should consider the minimum cell current (Icell) on the worst bit depending on SRAM bit-cell total density.

(4) Recommend to turn off pre-charge circuits on dummy read (columns) bit lines because it would create additional DC leakage path, worsen IR drop and degrade cell read stability.

(5) SRAM bitcell spec is verified based on the same array supply voltage, Wordline voltage, and Bitline precharge level in TSMC. Customers need to pay attention to cell margin degradation due to split voltage rails and signal coupling (such as WL voltage undershoot/overshoot) at design phase and validate with Si characterization.

(6) For HD 0.0734um2 single port SRAM ,customers must use design assist to provide over 250mV SRAM Vmin improvement at worse case SFG-6s, -40C for write operation regardless the size and configuration of SRAM instances. Write assist SPEC can be generated from V1.0 SRAM spice model but it subjects to change with silicon learning and spice model revised.

(7) HC-SP and 2P-8T don't need assist.

(8) For Dual port SRAM

(a.) Cell current (Icell) simulation should consider simultaneous read of both ports because Icell will be lower than only one port is turned on.

(b.) Longer write pulse, and write pulse >= read pulse is suggested to minimize the write margin degradation from insufficient write time when dummy read WLP overlap with write WLP. If dummy read pulse totally covers write pulse, write margin will severely degrade. TSMC also suggests customers to implement bit-line clamp scheme to enlarge write disturb window.

(c.) Silicon Vccmin characterization/test should cover the read/write with both ports accessing the same row. If the asynchronous clocking is allowed, the test should cover the offset of different clock

(9) For SHD 0.0690um2 single port SRAM ,customers must use design assist to provide over 250mV SRAM Vmin improvement at worse case SFG-6s, -40C for write operation regardless the size and configuration of SRAM instances. Write assist SPEC can be generated from V1.0 SRAM spice model but it subjects to change with silicon learning and spice model revised.

(10) SHC-SP doesn't need assist.

(11) Lower Vmin and DVFS offering table:

16FFC/LL		SRAM Offering		Usage Condition*
		HD/SHD with WAS	HC/HP/2P/DP/SHC	
STD	V_nom	0.85		>10yr, 125C
	V_min	0.765		
	V_max	0.935		
Lower Vmin	V_nom	0.75~0.85		10yr, 125C
	V_min	0.675		
	V_max	0.935		
DVFS	V_nom	0.75~1.0		10yr, 85C
	V_min	0.675		
	V_max	1.05		

*Definition of SRAM lifetime of tsmc SRAM vehicle based on HTOL Vccmin result of AF calculation with 10% reliability guardband of lowest Vnom. Customers need to consider reliability guardband for their own product use condition

5. Basic Information:

TSMC 6T cell IP: SP-HD with separate wells(for single port high density application)		
1. Unit cell size	0.0734 μm² (X: 0.408 μm; Y: 0.18 μm);	
2. Configuration	6T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds (Version 1.0)	Unit cell	16FF_d0734_v1d0_x4_AM
	X Edge cell	16FF_d0734_v1d0_row_edge_sep_Vss_x2_l_AM 16FF_d0734_v1d0_row_edge_sep_Vss_x2_r_AM
	Corner cell	16FF_d0734_v1d0_corner_dummy_sep_wells_x1_l_AM 16FF_d0734_v1d0_corner_dummy_sep_wells_x1_r_AM
	Y Edge cell and well strapping cell	16FF_d0734_v1d0_strap_dummy_sep_wells_x1_l_AM 16FF_d0734_v1d0_strap_dummy_sep_wells_x1_r_AM 16FF_d0734_v1d0_sep_wells_strap_edge_x2_AM 16FF_d0734_v1d0_sep_wells_strap_x2_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 10 /20 nm	
	Pull Down: 10 /20 nm	
	Pull Up: 10 /20 nm	
5. Cell SPICE model	**Version 1.0p1**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sr_v1d0_2p1_usage_guide.pdf"

TSMC 6T cell IP: SP-HC with separate wells (for single port high density application)		
1. Unit cell size	0.0907 μm² (X: 0.504 μm; Y: 0.18 μm);	
2. Configuration	6T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds (Version 1.0)	Unit cell	16FF_d0907_v1d0_x4_AM
	X Edge cell	16FF_d0907_v1d0_row_edge_sep_Vss_x2_l_AM 16FF_d0907_v1d0_row_edge_sep_Vss_x2_r_AM
	Corner cell	16FF_d0907_v1d0_corner_dummy_sep_wells_x1_l_AM 16FF_d0907_v1d0_corner_dummy_sep_wells_x1_r_AM
	Y Edge cell and well strapping cell	16FF_d0907_v1d0_strap_dummy_sep_wells_x1_l_AM 16FF_d0907_v1d0_strap_dummy_sep_wells_x1_r_AM 16FF_d0907_v1d0_sep_wells_strap_edge_x2_AM 16FF_d0907_v1d0_sep_wells_strap_x2_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 58 /20 nm	
	Pull Down: 58 /20 nm	
	Pull Up: 10 /20 nm	
5. Cell SPICE model	**Version 1.0p1**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sr_v1d0_2p1_usage_guide.pdf"

TSMC 6T cell IP: SP-HP with separate wells (for single port high density application)		
1. Unit cell size	0.108 μm² (X: 0.6 μm; Y: 0.18 μm);	
2. Configuration	6T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds (Version 1.0)	Unit cell	16FF_d108_v1d0_x4_AM
	X Edge cell	16FF_d108_v1d0_row_edge_sep_Vss_x2_l_AM 16FF_d108_v1d0_row_edge_sep_Vss_x2_r_AM
	Corner cell	16FF_d108_v1d0_corner_dummy_sep_wells_x1_l_AM 16FF_d108_v1d0_corner_dummy_sep_wells_x1_r_AM
	Y Edge cell and well strapping cell	16FF_d108_v1d0_strap_dummy_sep_wells_x1_l_AM 16FF_d108_v1d0_strap_dummy_sep_wells_x1_r_AM 16FF_d108_v1d0_sep_wells_strap_edge_x2_AM 16FF_d108_v1d0_sep_wells_strap_x2_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 106 /20 nm	
	Pull Down: 106 /20 nm	
	Pull Up: 10 /20 nm	
5. Cell SPICE model	**Version 1.0p1**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sr_v1d0_2p1_usage_guide.pdf"

TSMC 8T cell IP: 2P-8T with separate wells (RP 2fins)		
1. Unit cell size	0.130 μm² (X: 0.72 μm; Y: 0.18 μm)	
2. Configuration	8T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds (Version 1.0)	Unit cell	16FF_2P_d130_v1d0_x4_AM
	X Edge cell	16FF_2P_d130_v1d0_row_edge _x2_l_AM 16FF_2P_d130_v1d0_row_edge _x2_r_AM
	Corner cell	16FF_2P_d130_v1d0_corner_dummy_sep_wells_x1_l_AM 16FF_2P_d130_v1d0_corner_dummy_sep_wells_x1_r_AM
	Y Edge cell and well strapping cell	16FF_2P_d130_v1d0_strap_dummy_sep_wells_x1_l_AM 16FF_2P_d130_v1d0_strap_dummy_sep_wells_x1_r_AM 16FF_2P_d130_v1d0_sep_wells_strap_edge_x2_AM 16FF_2P_d130_v1d0_sep_wells_strap_x2_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 58 /20 nm	
	Pull Down: 58 /20 nm	
	Pull Up: 10 /20 nm	
	Read Port Pass Gate: 58 /20 nm	
	Read Port Pull Down: 58 /20 nm	
5. Cell SPICE model	**Version 1.0p1**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sr_v1d0_2p1_usage_guide.pdf"

TSMC 8T cell IP: 2P-8THC with separate wells (RP 3fins)		
1. Unit cell size	0.138 μm² (X: 0.768 μm; Y: 0.18 μm)	
2. Configuration	8T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds (Version 1.0)	Unit cell	16FF_2P_d138_v1d0_x4_AM
	X Edge cell	16FF_2P_d138_v1d0_row_edge _x2_l_AM 16FF_2P_d138_v1d0_row_edge _x2_r_AM
	Corner cell	16FF_2P_d138_v1d0_corner_dummy_sep_wells_x1_l_AM 16FF_2P_d138_v1d0_corner_dummy_sep_wells_x1_r_AM
	Y Edge cell and well strapping cell	16FF_2P_d138_v1d0_strap_dummy_sep_wells_x1_l_AM 16FF_2P_d138_v1d0_strap_dummy_sep_wells_x1_r_AM 16FF_2P_d138_v1d0_sep_wells_strap_edge_x2_AM 16FF_2P_d138_v1d0_sep_wells_strap_x2_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 58 /20 nm	
	Pull Down: 58 /20 nm	
	Pull Up: 10 /20 nm	
	Read Port Pass Gate: 106 /20 nm	
	Read Port Pull Down: 106 /20 nm	
5. Cell SPICE model	**Version 1.0p1**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sr_v1d0_2p1_usage_guide.pdf"

TSMC 8T cell IP: 2P-8THS with separate wells (RP 4fins)		
1. Unit cell size	0.147 μm² (X: 0.816 μm; Y: 0.18 μm)	
2. Configuration	8T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds (Version 1.0)	Unit cell	16FF_2P_d147_v1d0_x4_AM
	X Edge cell	16FF_2P_d147_v1d0_row_edge _x2_l_AM 16FF_2P_d147_v1d0_row_edge _x2_r_AM
	Corner cell	16FF_2P_d147_v1d0_corner_dummy_sep_wells_x1_l_AM 16FF_2P_d147_v1d0_corner_dummy_sep_wells_x1_r_AM
	Y Edge cell and well strapping cell	16FF_2P_d147_v1d0_strap_dummy_sep_wells_x1_l_AM 16FF_2P_d147_v1d0_strap_dummy_sep_wells_x1_r_AM 16FF_2P_d147_v1d0_sep_wells_strap_edge_x2_AM 16FF_2P_d147_v1d0_sep_wells_strap_x2_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 58 /20 nm	
	Pull Down: 58 /20 nm	
	Pull Up: 10 /20 nm	
	Read Port Pass Gate: 154 /20 nm	
	Read Port Pull Down: 154 /20 nm	
5. Cell SPICE model	**Version 1.0p1**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sr_v1d0_2p1_usage_guide.pdf"

TSMC 8T cell IP: DP-HC with separate wells (for single port high density application)		
1. Unit cell size	0.194 μm² (X: 1.08 μm; Y: 0.18 μm);	
2. Configuration	6T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_015_016_AM.gds (Version 1.0)	Unit cell	16FF_DP_F_d194_v1d0_x4_AM
	X Edge cell	16FF_DP_F_d194_v1d0_row_edge_twist_x2_AM 16FF_DP_F_d194_v1d0_row_edge_x2_AM
	Corner cell	16FF_DP_F_d194_v1d0_BL_twist_and_sep_wells_strap_x2_AM 16FF_DP_F_d194_v1d0_corner_dummy_sep_wells_x1_AM
	Y Edge cell and well strapping cell	16FF_DP_F_d194_v1d0_sep_wells_strap_edge_twist_x2_AM 16FF_DP_F_d194_v1d0_sep_wells_strap_edge_x2_AM 16FF_DP_F_d194_v1d0_strap_dummy_sep_wells_x1_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 58 /20 nm	
	Pull Down: 154 /20 nm	
	Pull Up: 10 /20 nm	
5. Cell SPICE model	**Version 1.0p1**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sr_v1d0_2p1_usage_guide.pdf"

TSMC 6T cell IP: SP-SHD with separate wells(for single port small high density application)		
1. Unit cell size	0.0690 μm² (X: 0.384 μm; Y: 0.18 μm);	
2. Configuration	6T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020_AM.gds (Version 1.0)	Unit cell	16FF_d0690_v1d0_x4_AM
	X Edge cell	16FF_d0690_v1d0_row_edge_sep_Vss_x2_l_AM 16FF_d0690_v1d0_row_edge_sep_Vss_x2_r_AM
	Corner cell	16FF_d0690_v1d0_corner_dummy_sep_wells_x1_l_AM 16FF_d0690_v1d0_corner_dummy_sep_wells_x1_r_AM
	Y Edge cell and well strapping cell	16FF_d0690_v1d0_strap_dummy_sep_wells_x1_l_AM 16FF_d0690_v1d0_strap_dummy_sep_wells_x1_r_AM 16FF_d0690_v1d0_sep_wells_strap_edge_x2_AM 16FF_d0690_v1d0_sep_wells_strap_x2_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 10 /20 nm	
	Pull Down: 10 /20 nm	
	Pull Up: 10 /20 nm	
5. Cell SPICE model	**Version 1.0**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sbcsr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sbcsr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sbcsr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sbcsr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sbcsr_v1d0_2p1_usage_guide.pdf"

TSMC 6T cell IP: SP-SHC with separate wells (for single port small high density application)		
1. Unit cell size	0.0864 μm² (X: 0.48 μm; Y: 0.18 μm);	
2. Configuration	6T; 1P2M	
	M1 as BL and Vcc	
	M2 as WL and Vss	
3. GDS file: 16FF_demo_arrays_v1d0_for_T_N16_CL_CL_019_020_AM.gds (Version 1.0)	Unit cell	16FF_d0864_v1d0_x4_AM
	X Edge cell	16FF_d0864_v1d0_row_edge_sep_Vss_x2_l_AM 16FF_d0864_v1d0_row_edge_sep_Vss_x2_r_AM
	Corner cell	16FF_d0864_v1d0_corner_dummy_sep_wells_x1_l_AM 16FF_d0864_v1d0_corner_dummy_sep_wells_x1_r_AM
	Y Edge cell and well strapping cell	16FF_d0864_v1d0_strap_dummy_sep_wells_x1_l_AM 16FF_d0864_v1d0_strap_dummy_sep_wells_x1_r_AM 16FF_d0864_v1d0_sep_wells_strap_edge_x2_AM 16FF_d0864_v1d0_sep_wells_strap_x2_AM
4. Cell transistors	Layout size (on simulation scheme)	
	Pass Gate: 58 /20 nm	
	Pull Down: 58 /20 nm	
	Pull Up: 10 /20 nm	
5. Cell SPICE model	**Version 1.0**	
HSPICE (H-2013.03-SP2)	cln16ffcll_sbcsr_v1d0_2p1.l	
SPECTRE (MMSIM12.1_ISR16)	cln16ffcll_sbcsr_v1d0_2p1.scs	
ELDO (13.1)	cln16ffcll_sbcsr_v1d0_2p1.l	

(**)For detailed model information, please refer to
"cln16ffcll_sbcsr_v1d0_2p1_release_note.pdf" and
"cln16ffcll_sbcsr_v1d0_2p1_usage_guide.pdf"

6. CAD Layer Mapping:

CAD layer mapping for TSMC SRAM cell-IP as follows:

Masking Layer	Mask Code	CAD Layer Mapping	Digitized tone (**D**ark/**C**lear)
N well (0.85V)	192	3	C
OD	120	6;15	D
COD_V	12P	6;18	C
COD_H	12M	6;17	C
Poly-1	130	17	D
PO2	139	17;12	C
M0OD	156	84;0	C
M0PO	159	84;2	C
CMD	158	84;20	D
NN	198	26	C
PP	197	25	C
VIA0-b	770	159;0 159;102	C
VIA0-c	870	159;0 159;103	C
Metal-1b	760	31;0 31;102	C
Metal-1c	860	31;0 31;103	C
Via1	378	51;70	C
Metal-2b	780	32;70 32;102	C
Metal-2c	880	32;70 32;103	C
LVS diffusion dummy layer		49	Exclude “gate” from LVS
SRAM OD for device		6;0	SRAM LVS purpose
SRAM FIN merge for device		6;11	SRAM LVS purpose
SRAM array dummy layer (SRM)		50;0	SRM is to cover the SRAM cell array. The edge of the SRM layer should be aligned to the boundary of the SRAM cell array, which may include storage, strapping, and dummy edge cells.
SRAM array dummy layer (SRM) for SHD cell		50;10	SRM_10 is used to cover the SHD SRAM cell array (0.0690um^2)
SRAM array dummy layer (SRM) for HD cell		50;11	SRM_11 is used to cover the HD SRAM cell array (0.0734um^2)
SRAM array dummy layer (SRM) for SHC cell		50;12	SRM_12 is used to cover the SHC SRAM cell array (0.0864um^2)
SRAM array dummy layer (SRM) for HC cell		50;13	SRM_13 is used to cover the HC SRAM cell array (0.0907um^2)
SRAM array dummy layer (SRM) for HP cell		50;14	SRM_14 is used to cover the HP SRAM cell array (0.108um^2)
SRAM array dummy layer (SRM) for 8T2P_2FIN cell		50;15	SRM_15 is used to cover the 8T2P_2FIN SRAM cell array (0.130um^2)
SRAM array dummy layer (SRM) for 8T2P_3FIN cell		50;16	SRM_16 is used to cover the 8T2P_3FIN cell array (0.138um^2)
SRAM array dummy layer (SRM) for 8T2P_4FIN cell		50;19	SRM_19 is used to cover the 8T2P_4FIN cell array (0.147um^2)
SRAM array dummy layer (SRM) for HCDP cell		50;18	SRM_18 is used to cover the HCDP cell array (0.194um^2)

IP	63;63	IP TAG
Cell boundary dummy layer	108	Define unit cell boundary
SRAM bit cell contact dummy layer	30;11	To cover SRAM bit cell contact
SRAM WL MP dummy layer	30;16	To cover SRAM cell word-line MP
SRAM BTC MP dummy layer	30;17	To cover SRAM cell BTC MP
SRAM alignment mark layer	83;18	Define alignment mark
SRAM DRC waive layer	186;0	Excluded from DRC
DRC dummy layer	186;1	SRAM pass gate device

7. Backup