DRAM: Architectures, Interfaces, and Systems

A Tutorial

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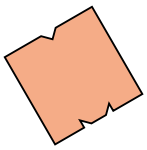
`http://www.ece.umd.edu/~blj/DRAM/`



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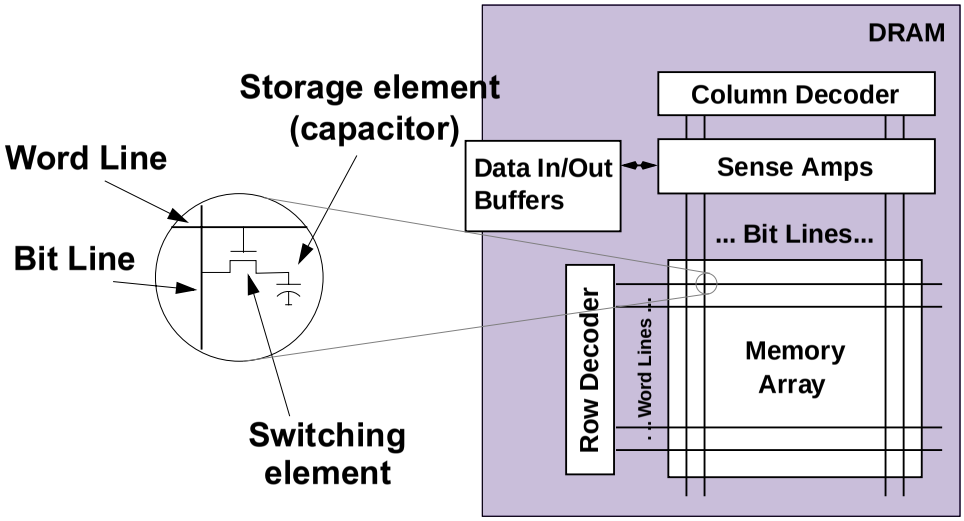
Outline

- **Basics**
- **DRAM Evolution: *Structural Path***
- **Advanced Basics**
- **DRAM Evolution: *Interface Path***
- **Future Interface Trends & Research Areas**
- **Performance Modeling:**
  Architectures, Systems, Embedded

Break at 10 a.m. — Stop us or starve

Basics

DRAM ORGANIZATION



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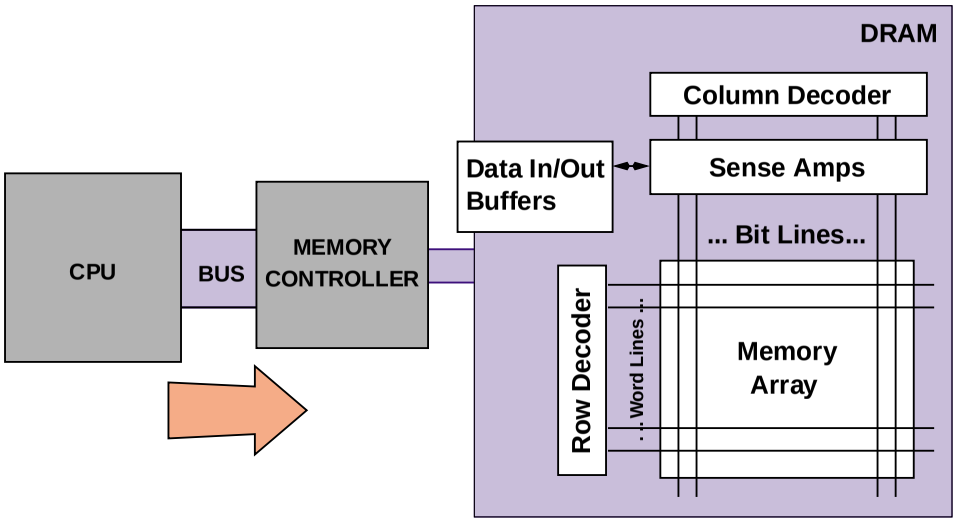
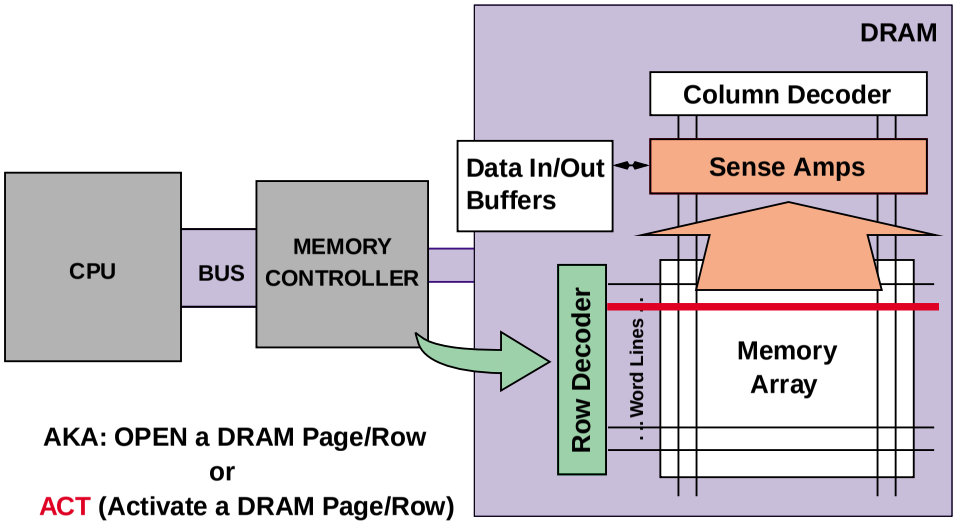
Basics

BUS TRANSMISSION



Basics

[PRECHARGE and] ROW ACCESS



AKA: OPEN a DRAM Page/Row
or
ACT (Activate a DRAM Page/Row)
or
RAS (Row Address Strobe)

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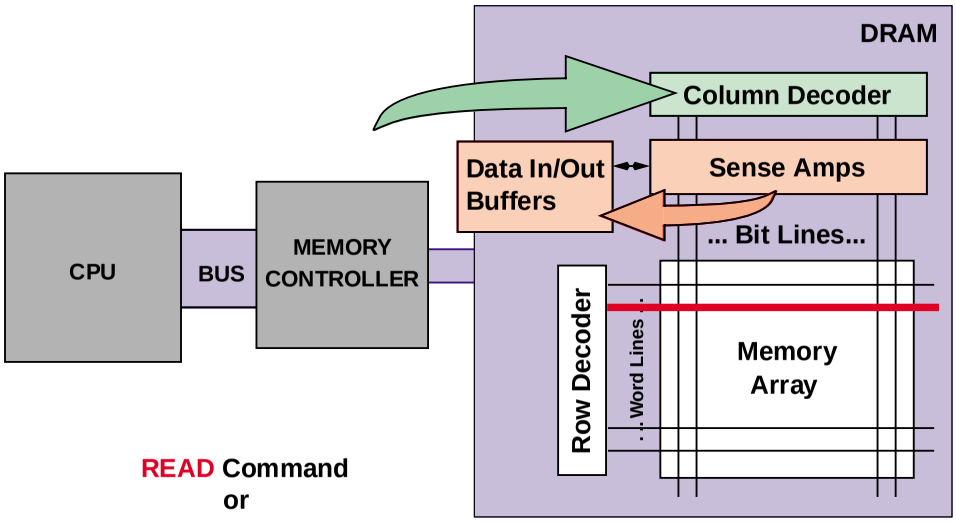
Basics

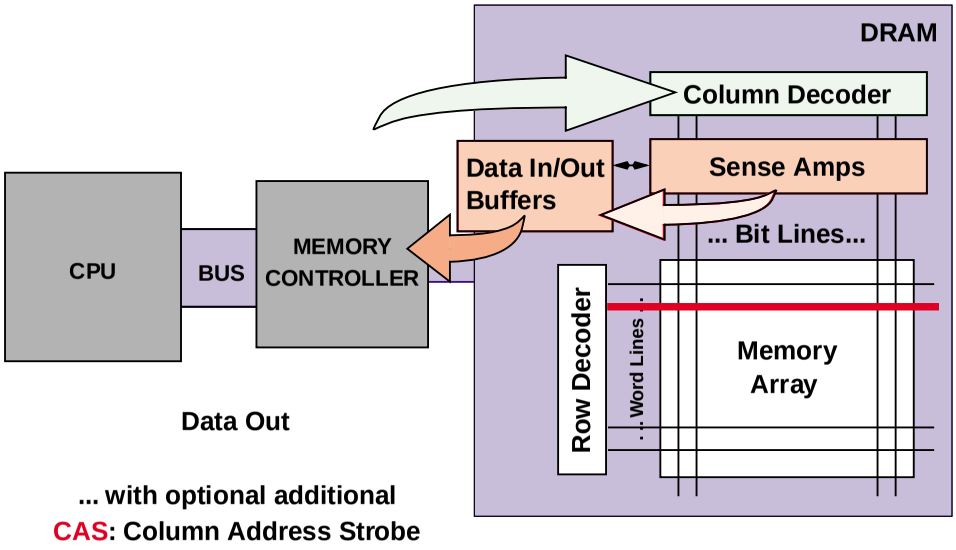
COLUMN ACCESS



READ Command
or
CAS: Column Address Strobe

Basics

DATA TRANSFER



note: page mode enables overlap with CAS

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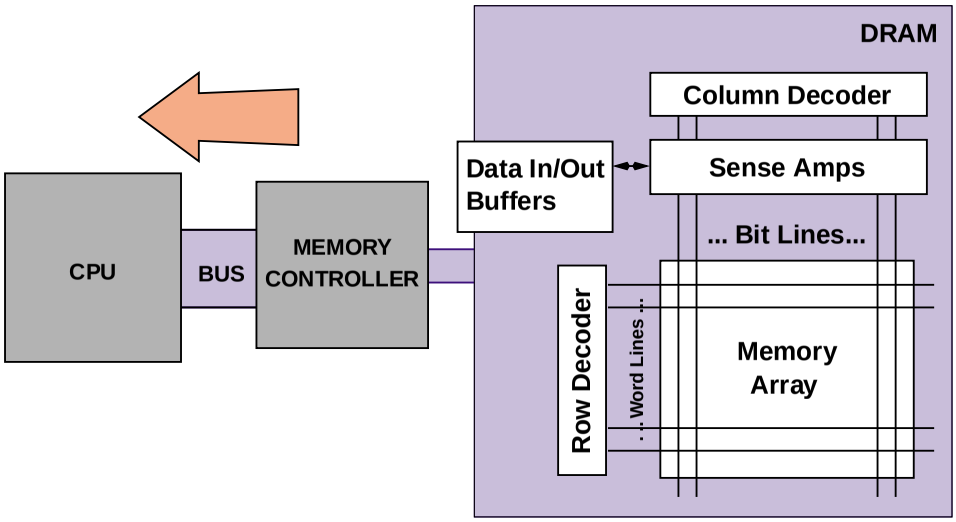
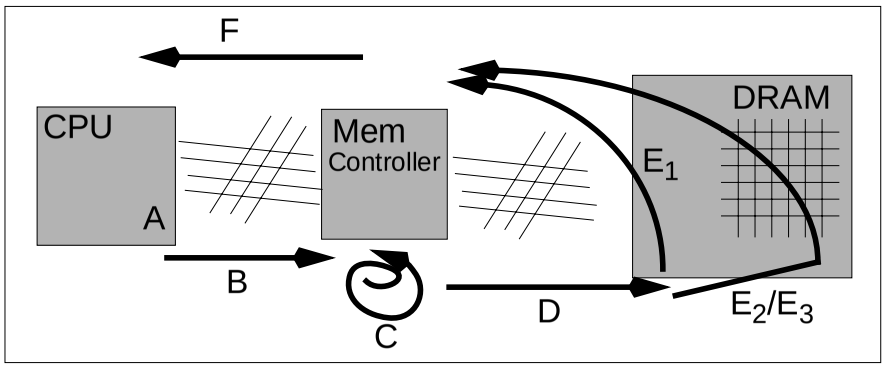
Basics

BUS TRANSMISSION



Basics



A: Transaction request may be delayed in Queue
B: Transaction request sent to Memory Controller
C: Transaction converted to Command Sequences
(may be queued)
D: Command/s Sent to DRAM
E_1: Requires only a **CAS** or
E_2: Requires **RAS + CAS** or
E_3: Requires **PRE + RAS + CAS**
F: Transaction sent back to CPU

"DRAM Latency" = A + B + C + D + E + F

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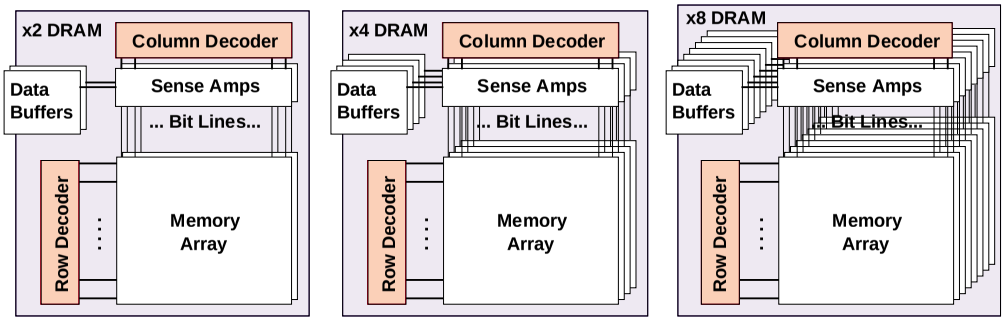
Basics

PHYSICAL ORGANIZATION

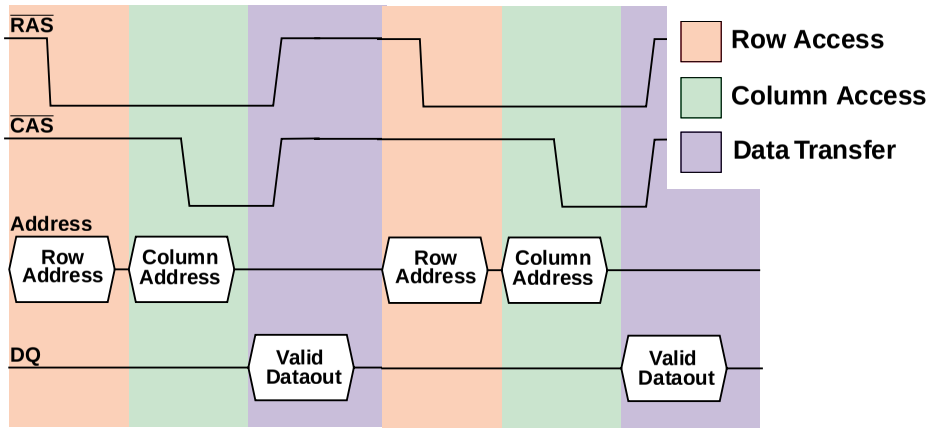


x2 DRAM **x4 DRAM** **x8 DRAM**

This is per bank …
Typical DRAMs have 2+ banks

Basics

Read Timing for Conventional DRAM



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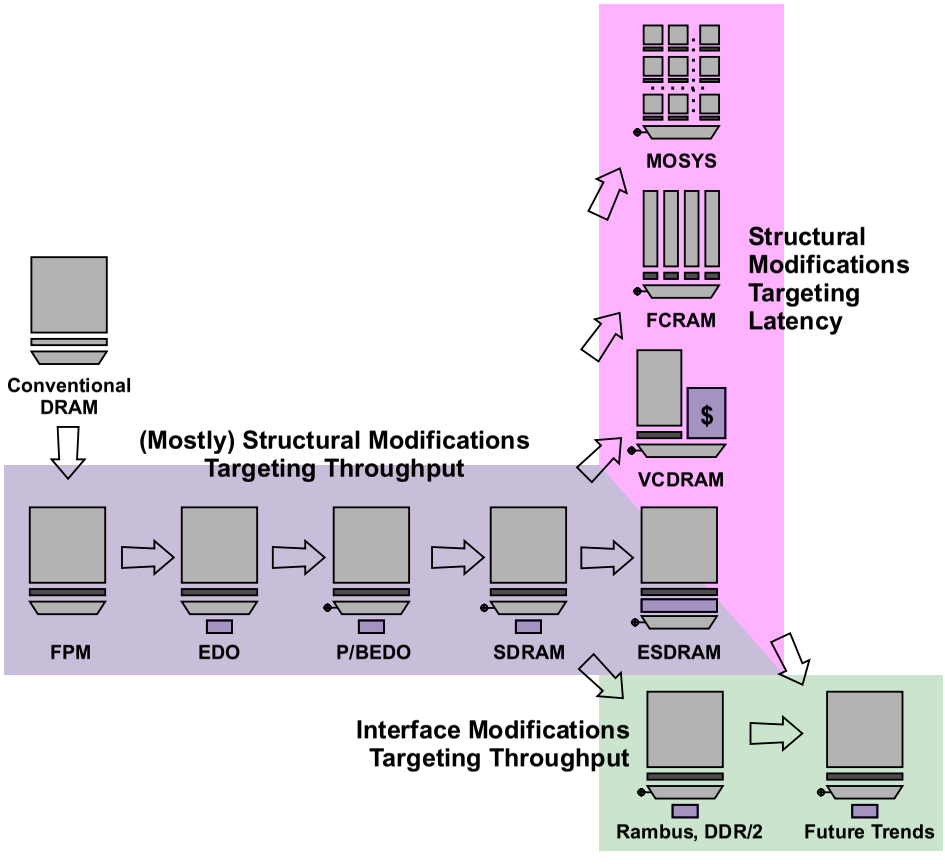
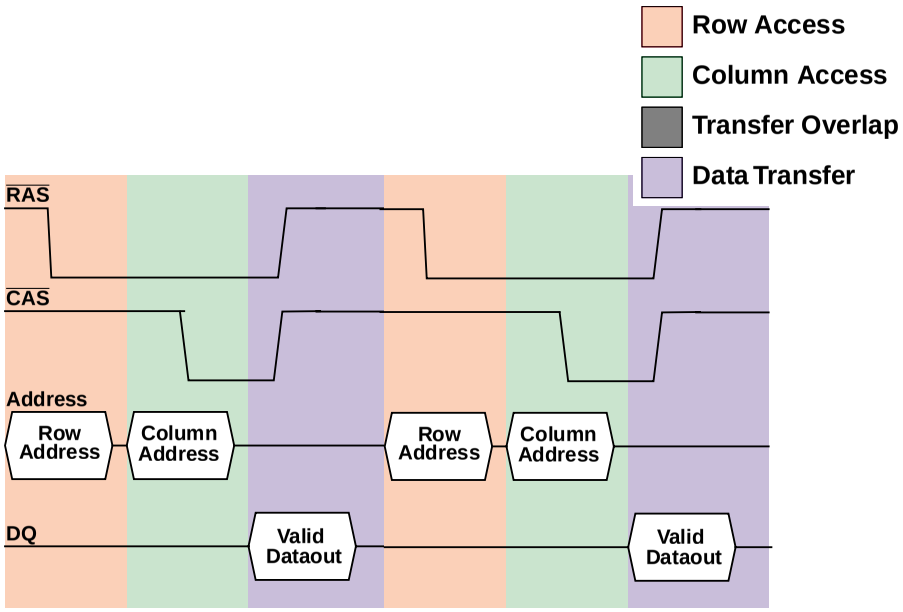
DRAM Evolutionary Tree



DRAM Evolution

Read Timing for Conventional DRAM



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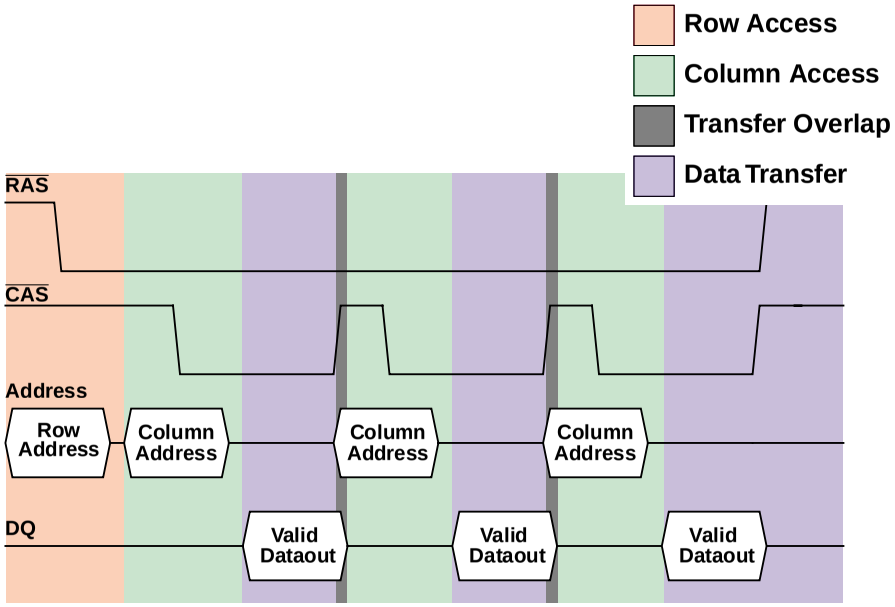
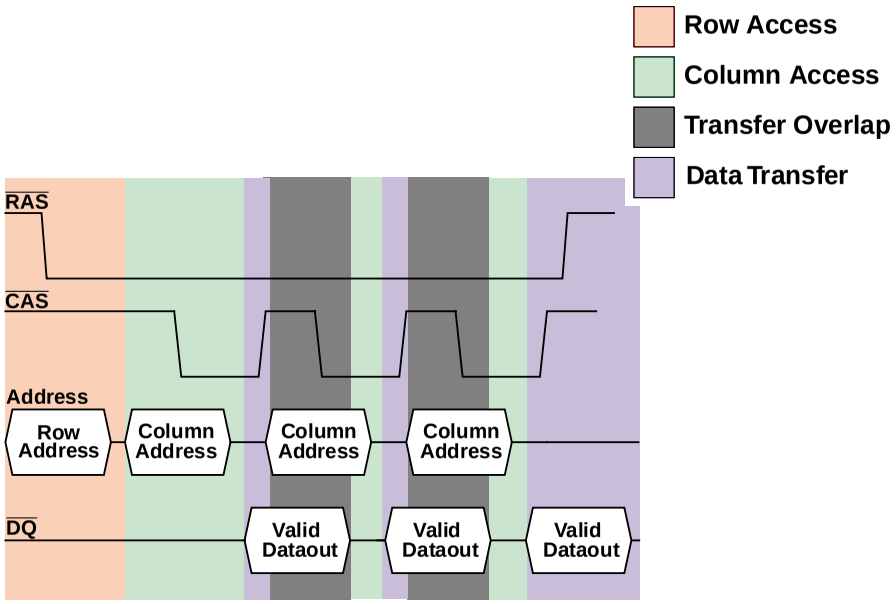
DRAM Evolution

Read Timing for Fast Page Mode



DRAM Evolution

Read Timing for Extended Data Out



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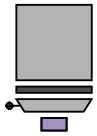
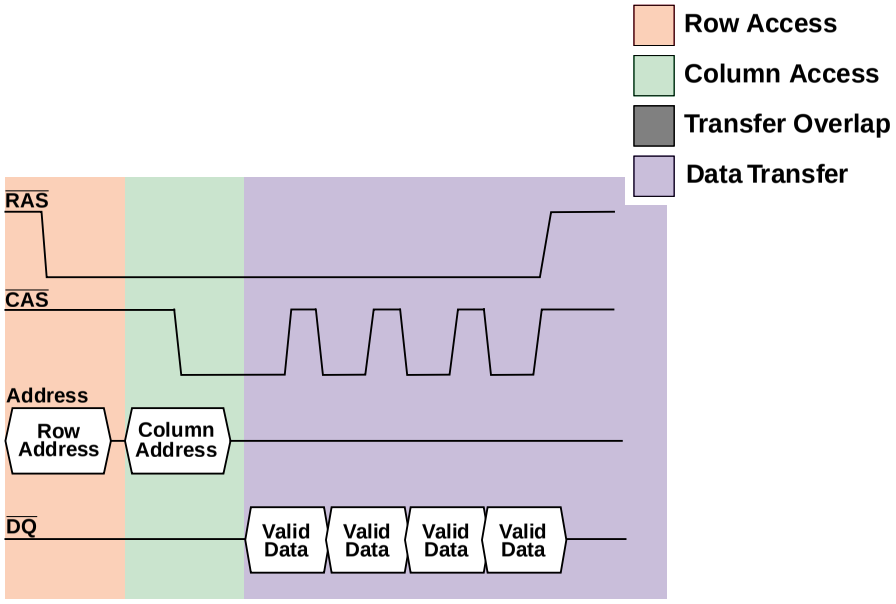
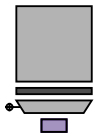
DRAM Evolution



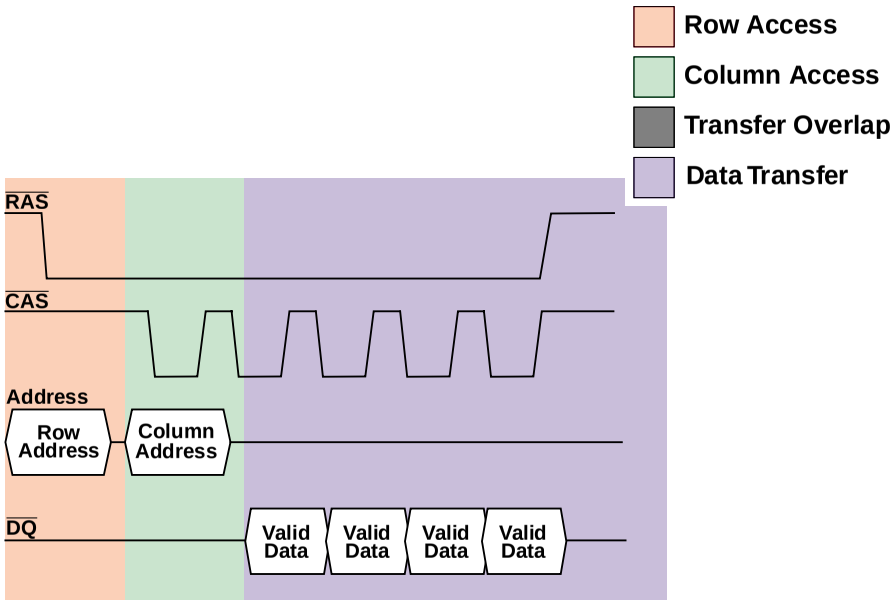
Read Timing for Burst EDO



DRAM Evolution



Read Timing for Pipeline Burst EDO



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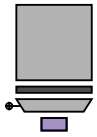
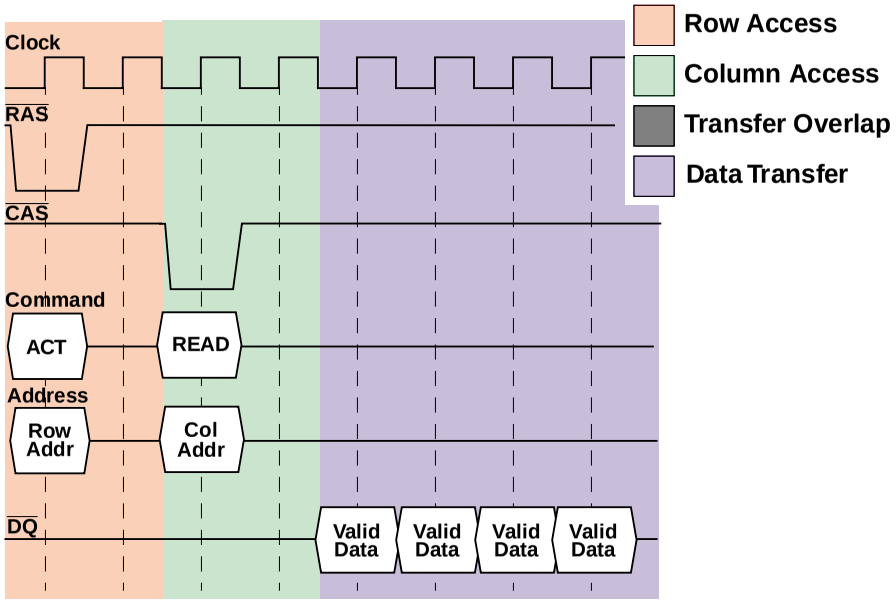
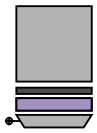


Read Timing for Synchronous DRAM



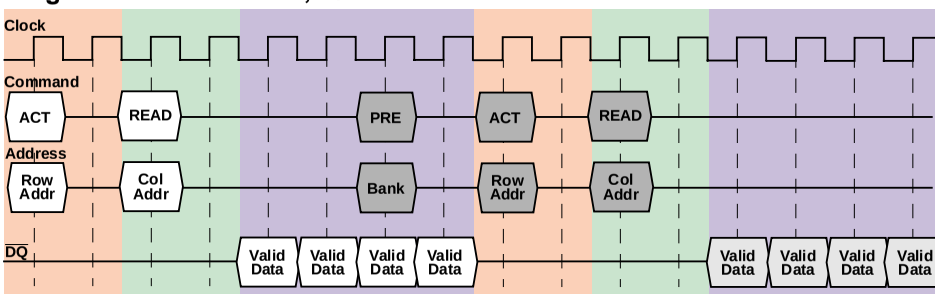
($\overline{RAS}$ + $\overline{CAS}$ + $\overline{OE}$ ... == Command Bus)

DRAM Evolution

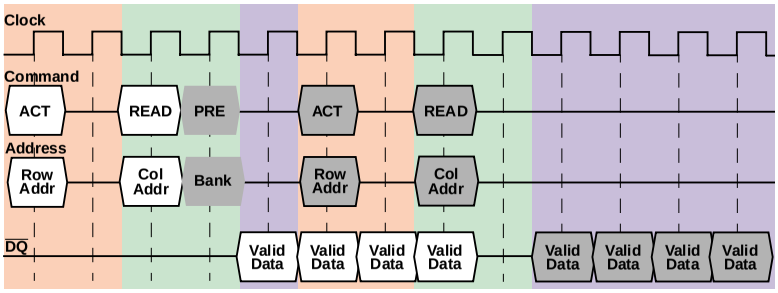


Inter-Row Read Timing for ESDRAM

Regular CAS-2 SDRAM, R/R to same bank



ESDRAM, R/R to same bank



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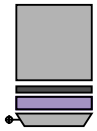
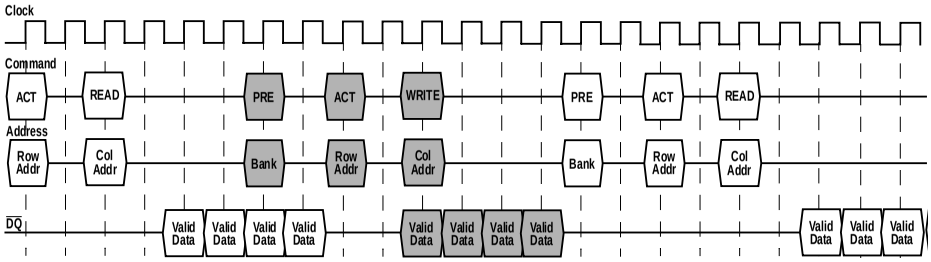
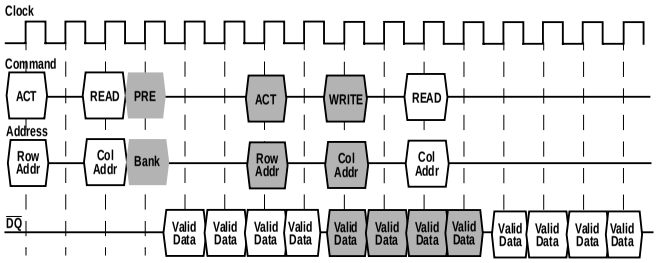


Write-Around in ESDRAM

Regular CAS-2 SDRAM, R/W/R to same bank, rows 0/1/0

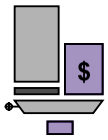


ESDRAM, R/W/R to same bank, rows 0/1/0

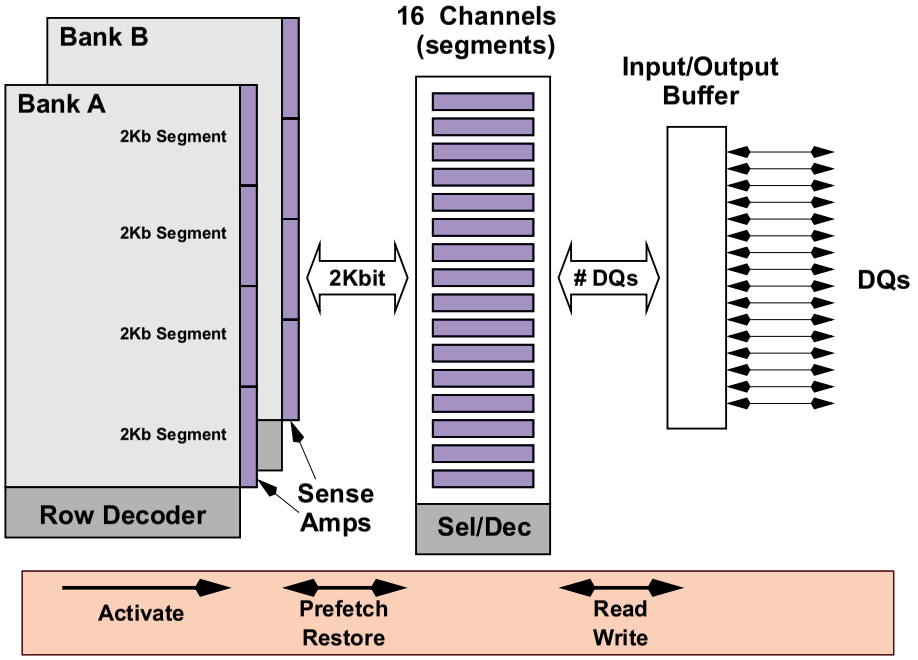


(can second READ be this aggressive?)

DRAM Evolution



Internal Structure of Virtual Channel



Segment cache is software-managed, reduces energy

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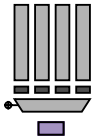
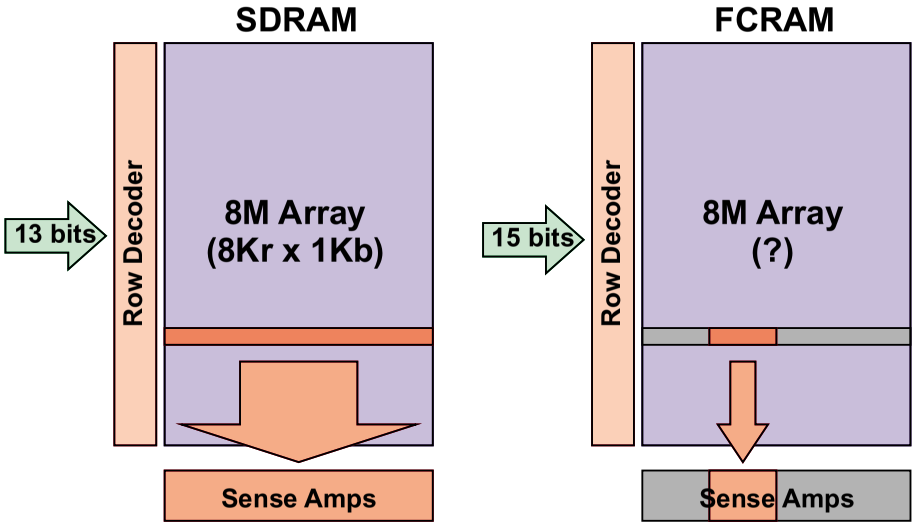


Internal Structure of Fast Cycle RAM

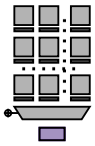


t_{RCD} = 15ns (two clocks)

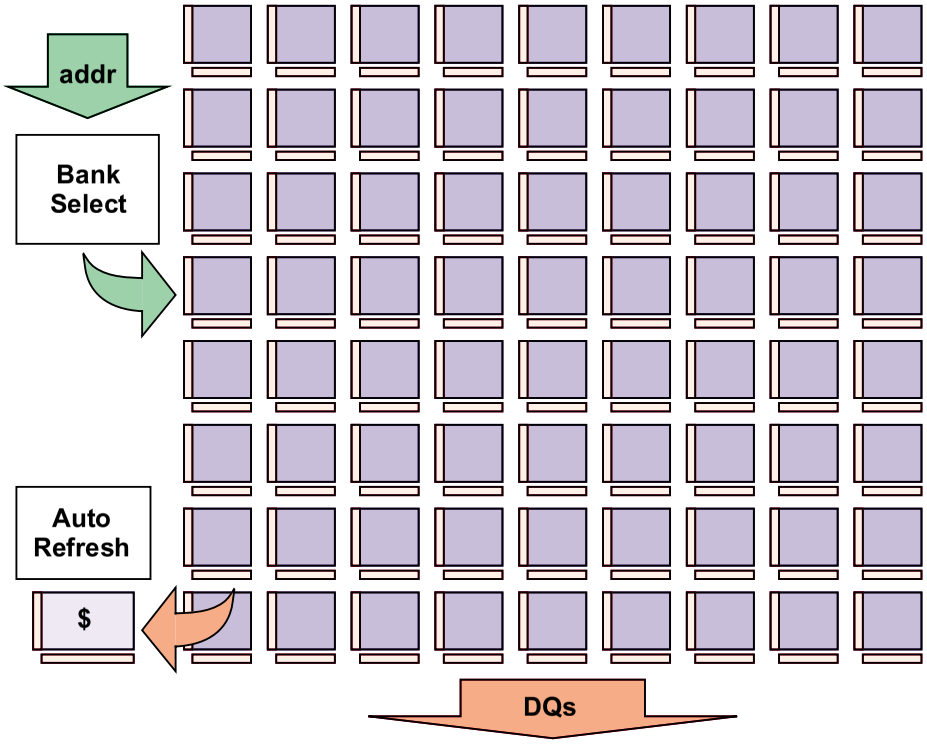
t_{RCD} = 5ns (one clock)

Reduces access time and energy/access

DRAM Evolution



Internal Structure of MoSys 1T-SRAM



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DRAM Evolution

Comparison of Low-Latency DRAM Cores

DRAM Type	Data Bus Speed	Bus Width (per chip)	Peak BW (per Chip)	RAS–CAS (t_{RCD})	RAS–DQ (t_{RAC})
PC133 SDRAM	133	16	266 MB/s	15 ns	30 ns
VCDRAM	133	16	266 MB/s	30 ns	45 ns
FCRAM	200 * 2	16	800 MB/s	5 ns	22 ns
1T-SRAM	200	32	800 MB/s	—	10 ns
DDR 266	133 * 2	16	532 MB/s	20 ns	45 ns
DRDRAM	400 * 2	16	1.6 GB/s	22.5 ns	60 ns
RLDRAM	300 * 2	32	2.4 GB/s	???	25 ns

Outline

- **Basics**
- **DRAM Evolution: *Structural Path***
- **Advanced Basics**
- **Memory System Details (Lots)**
- **DRAM Evolution: *Interface Path***
- **Future Interface Trends & Research Areas**
- **Performance Modeling: *Architectures, Systems, Embedded***

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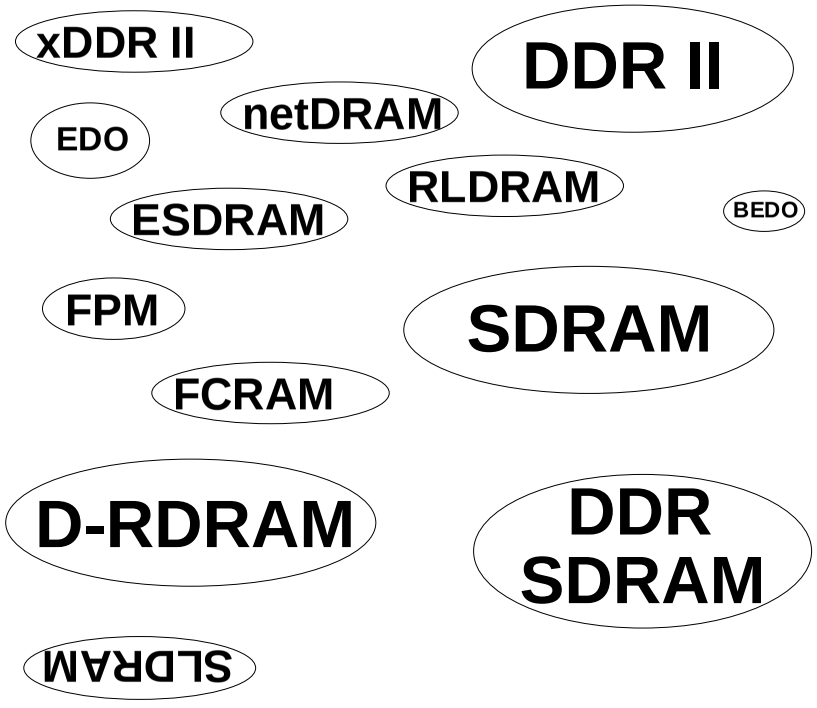
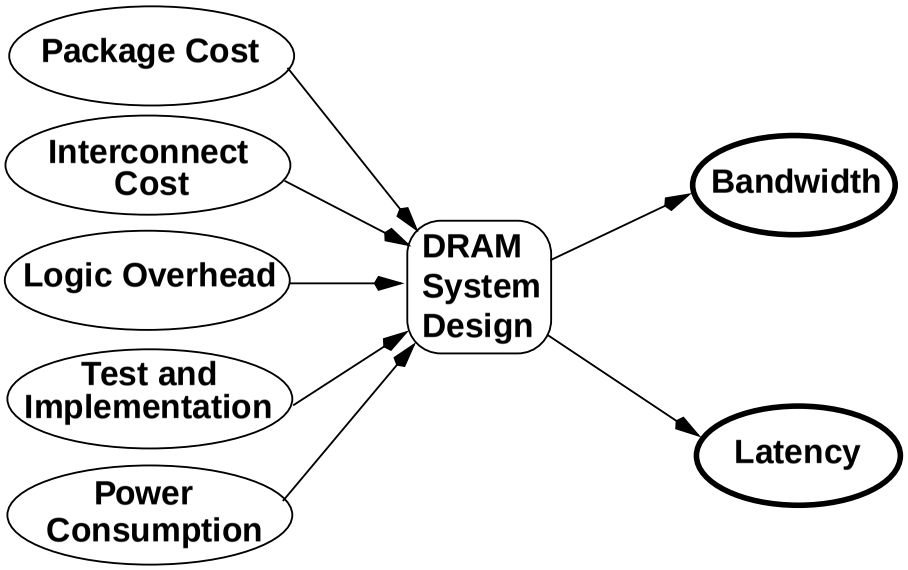
What Does This All Mean?



Cost - Benefit Criterion



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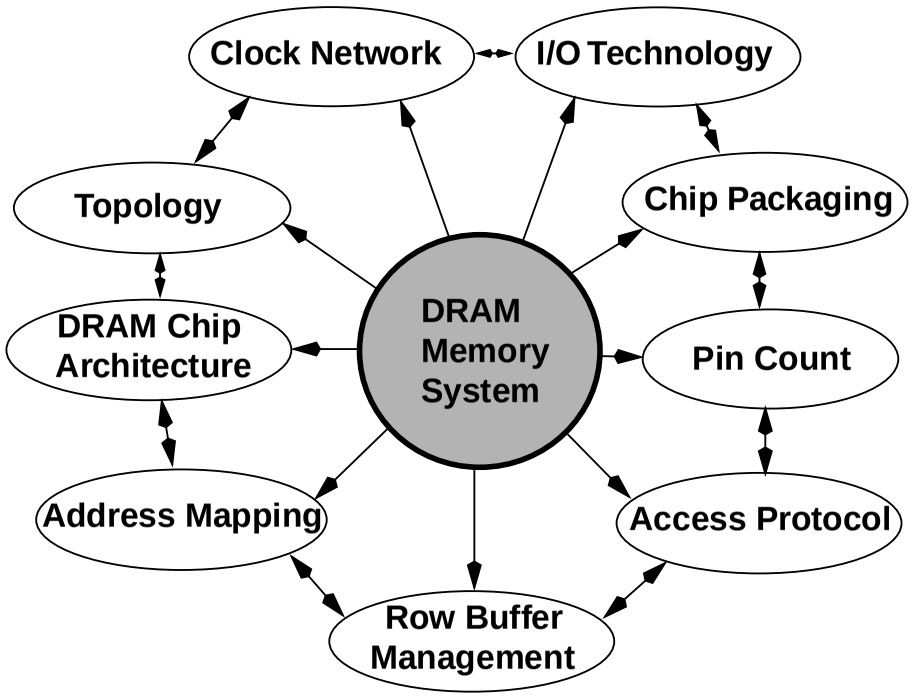
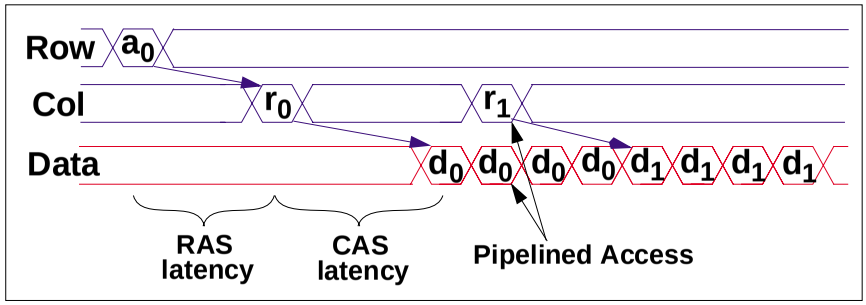
Memory System Design



DRAM Interfaces

The Digital Fantasy



Pretend that the world looks like this

But...

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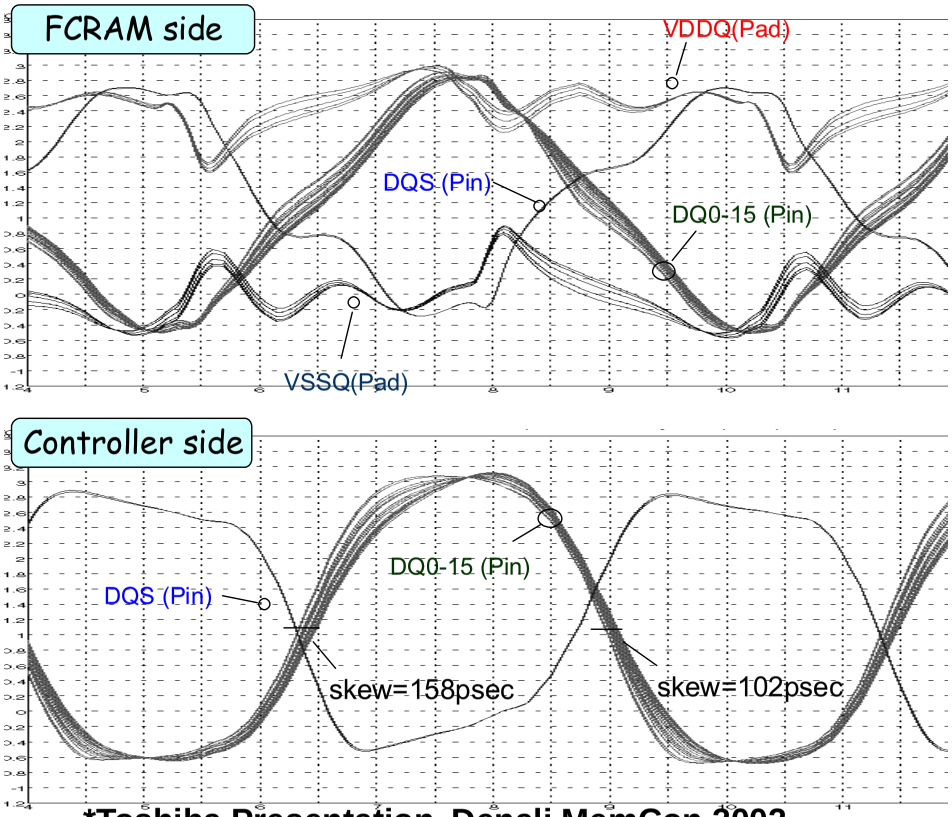
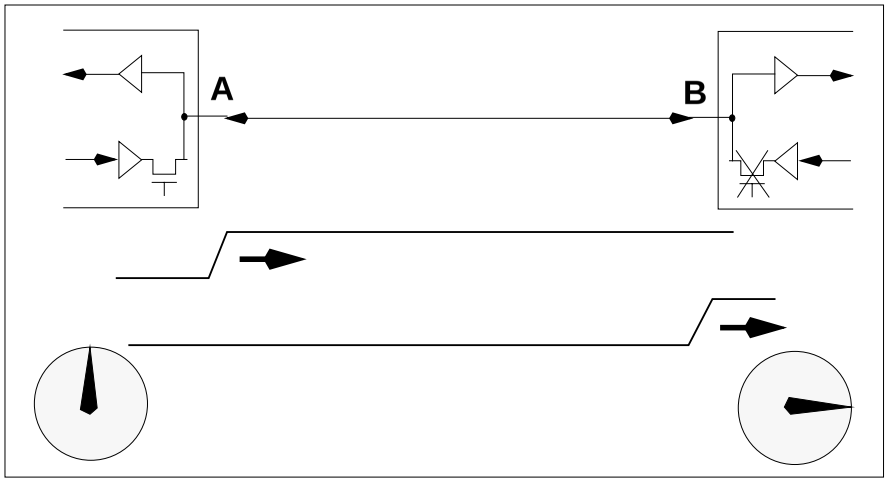
The Real World



***Toshiba Presentation, Denali MemCon 2002**

Signal Propagation



Ideal Transmission Line

~ 0.66c = 20 cm/ns

PC Board + Module Connectors + Varying Electrical Loads

= Rather non-Ideal Transmission Line

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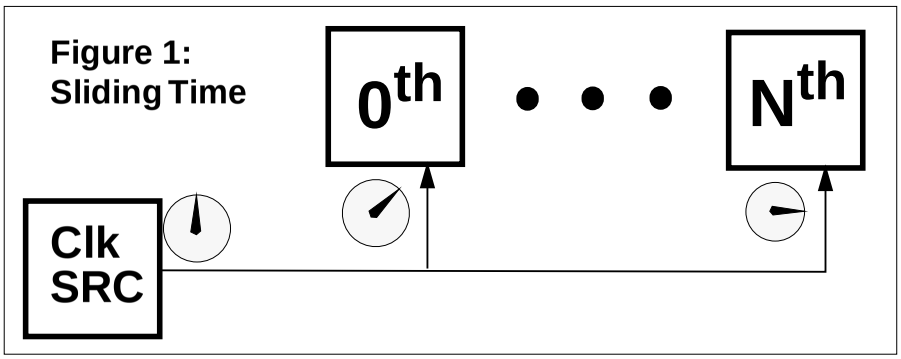
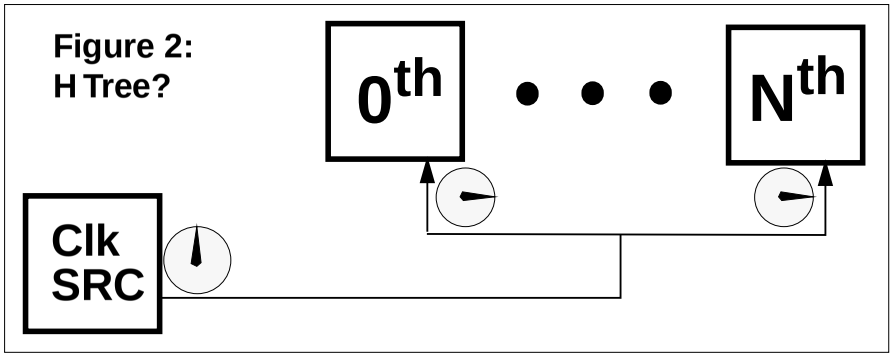
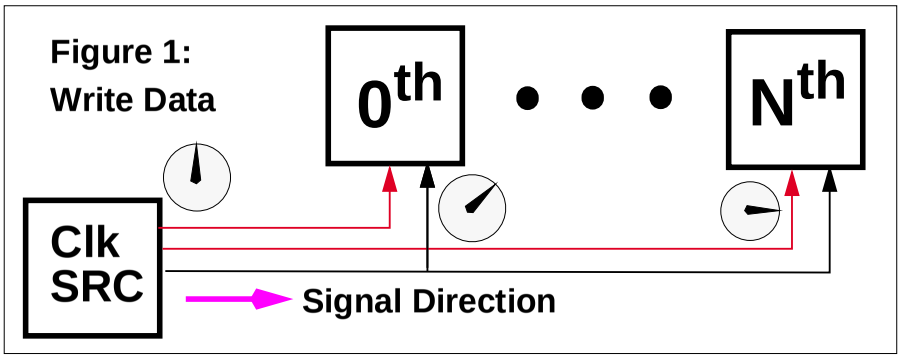
Clocking Issues

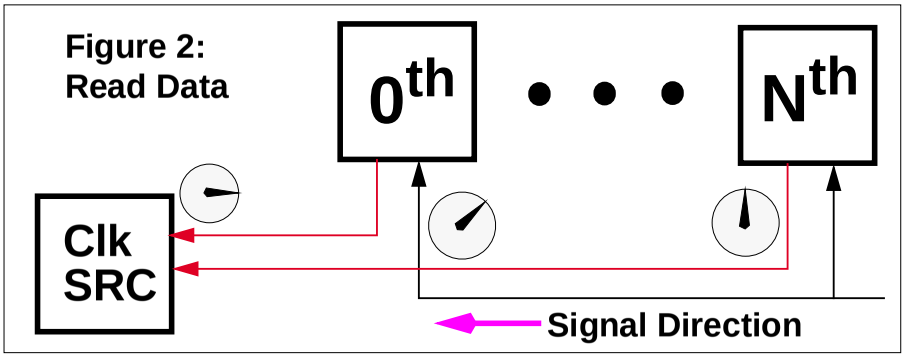




What Kind of Clocking System?

Clocking Issues





We need different "clocks" for R/W

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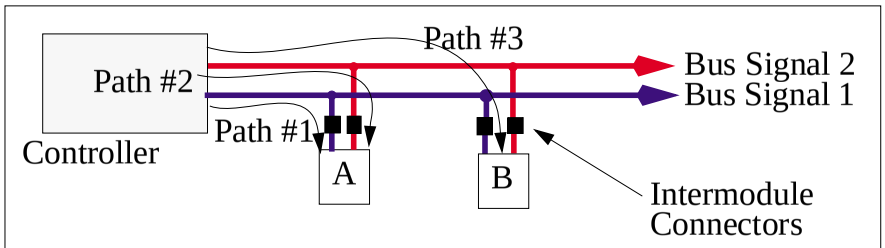
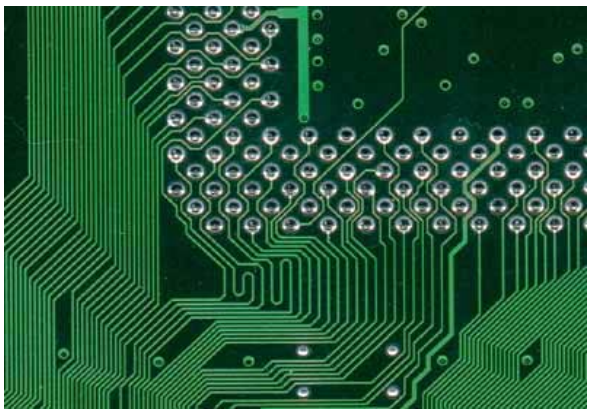
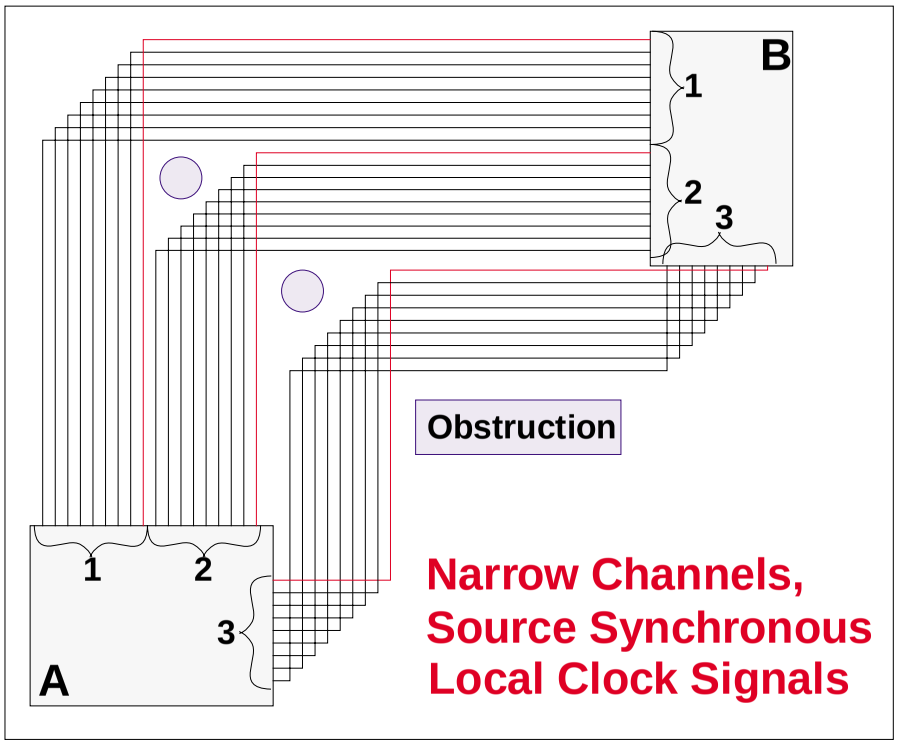
Path Length Differential





High Frequency AND Wide Parallel Busses are Difficult to Implement

Subdividing Wide Busses



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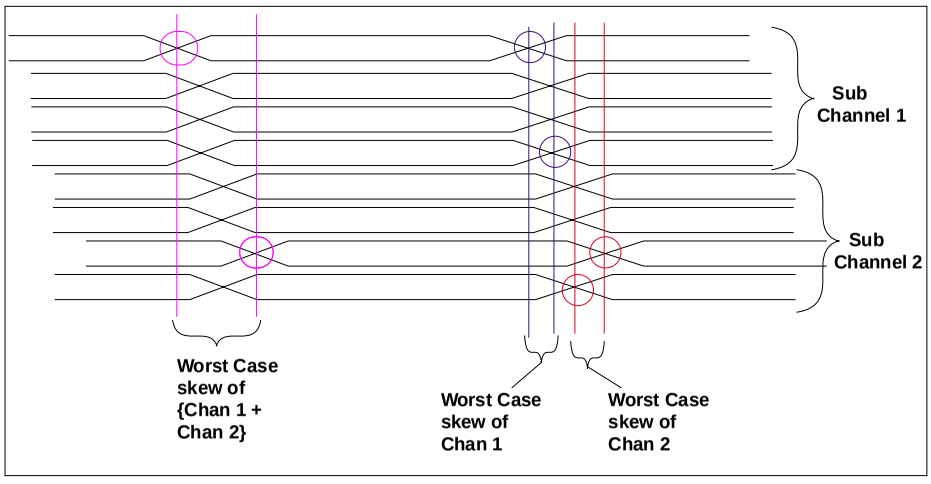
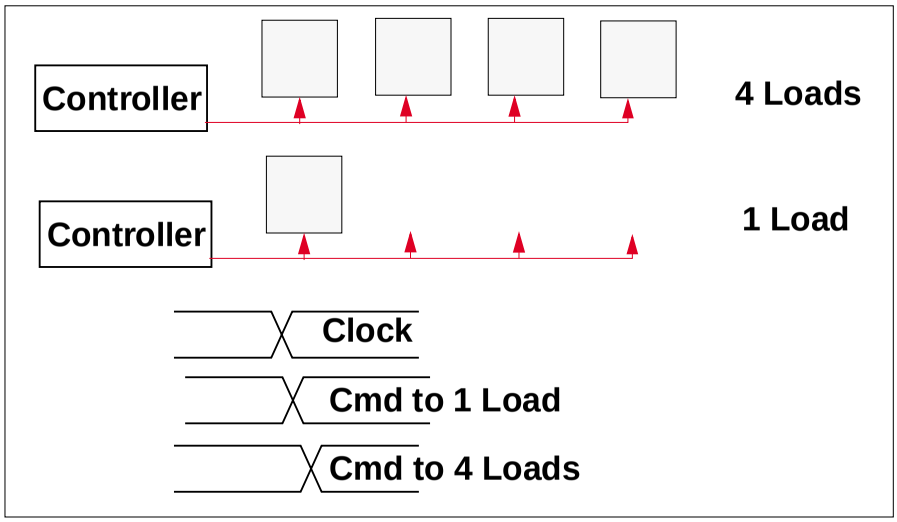
Why Subdivision Helps



Worst Case Skew must be Considered in System Timing

Timing Variations



How many DIMMs in System?

How many devices on each DIMM?

Who built the memory module?

Infinite variations on timing!

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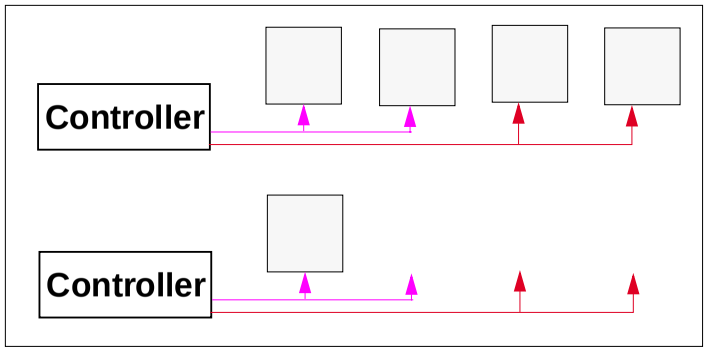
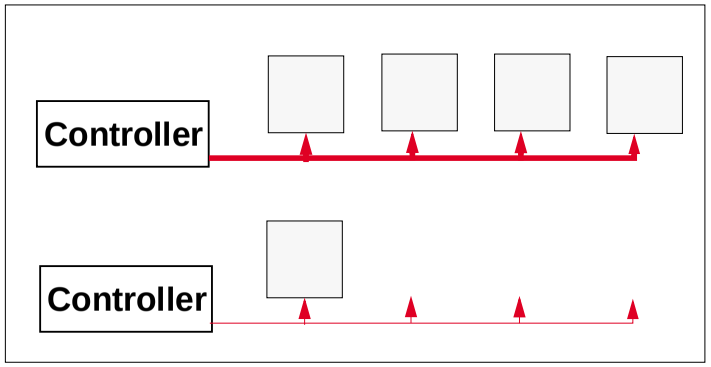
Loading Balance

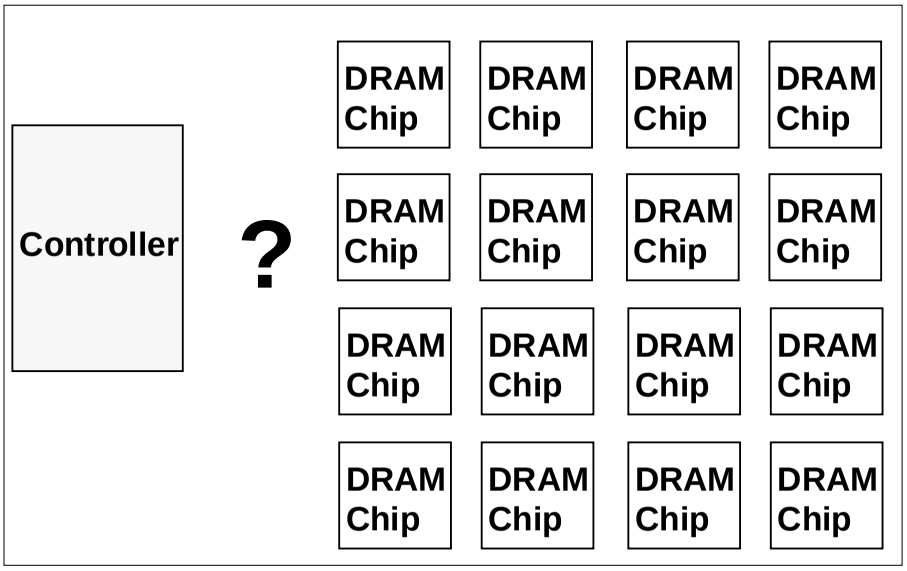


Duplicate Signal Lines



Variable Signal Drive Strength

Topology



DRAM System Topology Determines
Electrical Loading Conditions
and Signal Propagation Lengths

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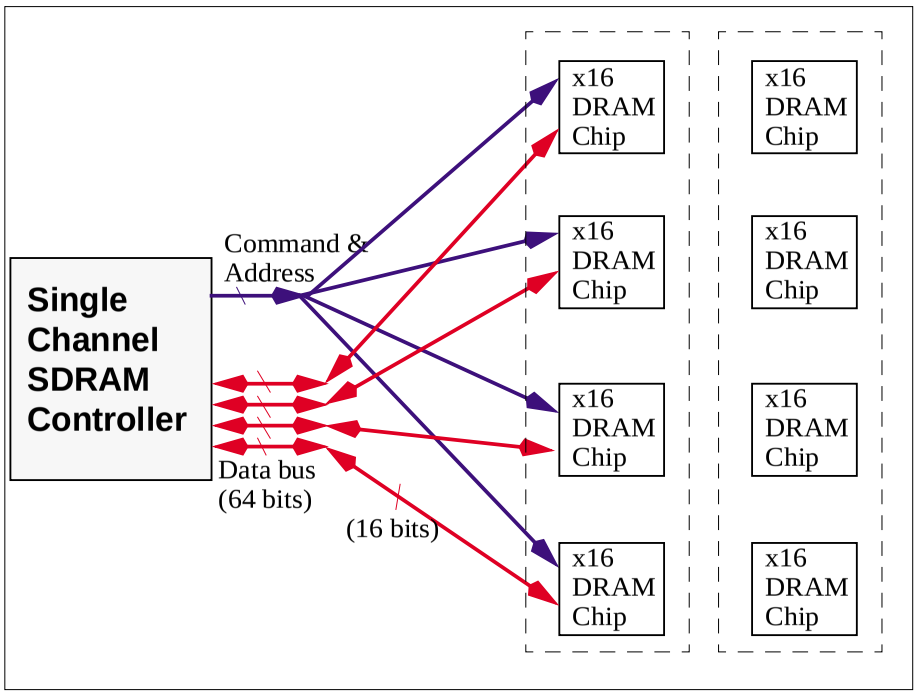
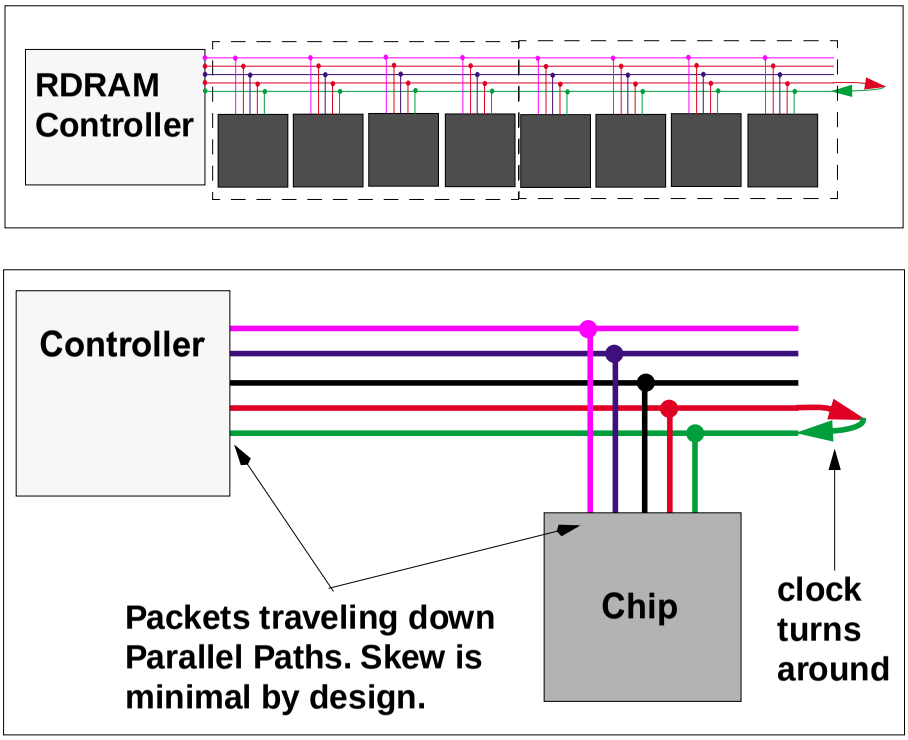
SDRAM Topology Example



Loading Imbalance

RDRAM Topology Example



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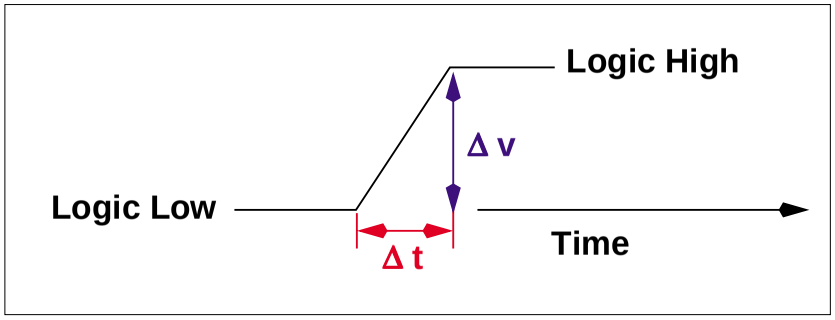
I/O Technology

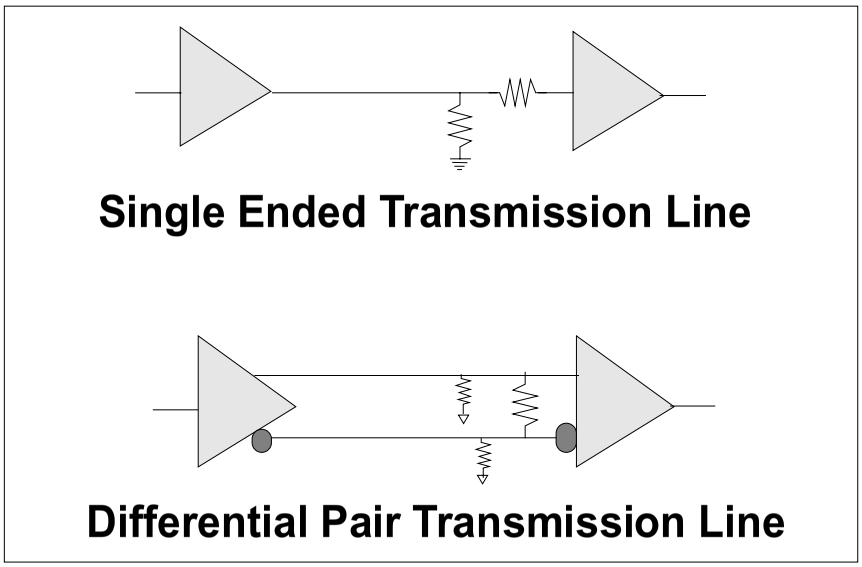


$$\text{Slew Rate} = \frac{\Delta v}{\Delta t}$$

Smaller Δ v =
Smaller Δ t at same slew rate

Increase Rate of bits/s/pin

I/O - Differential Pair



Increase Rate of bits/s/pin ?

Cost Per Pin?

Pin Count?

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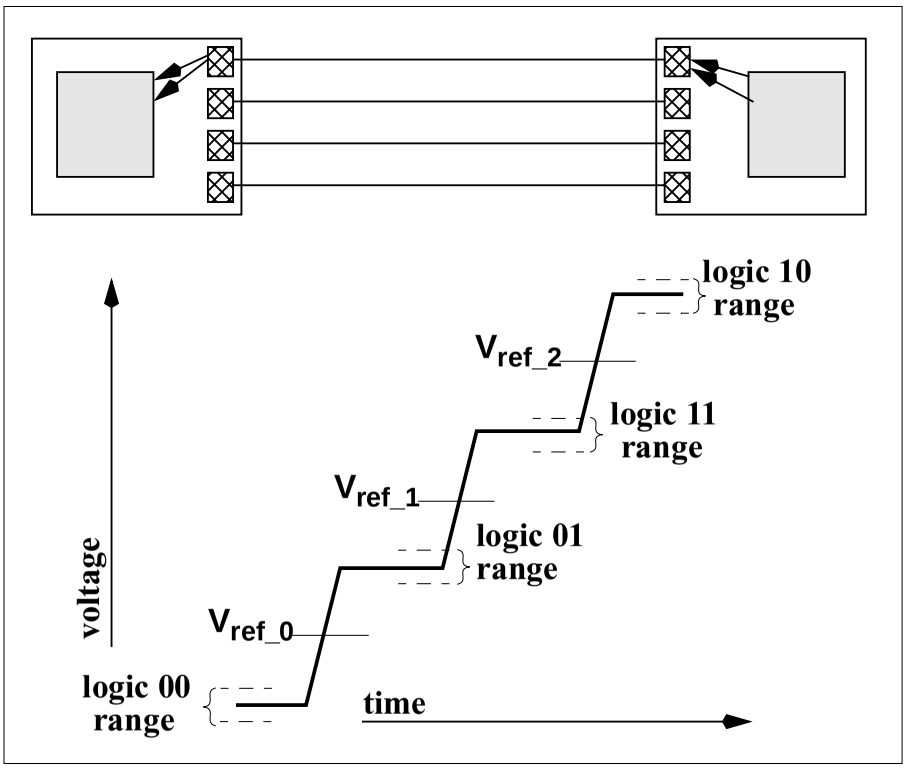
I/O - Multi Level Logic

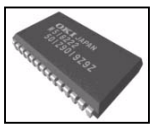


Increase Rate of bits/s/pin

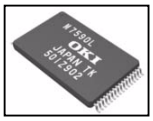
Packaging

DIP
"good old days"

SOJ
Small Outline J-lead

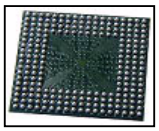


TSOP
Thin Small Outline Package



LQFP
Low Profile Quad Flat Package

FBGA
Fine Ball Grid Array



Features	Target Specification	
Package	FBGA	LQFP
Speed	800MBp	550Mbps
Vdd/Vddq	2.5V/2.5V (1.8V)	
Interface	SSTL_2	
Row Cycle Time t_{RC}	35ns	

Memory Roadmap for Hynix NetDDR II

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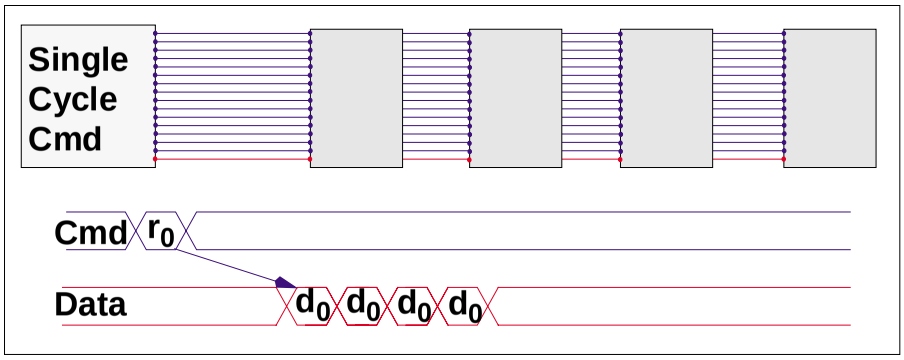
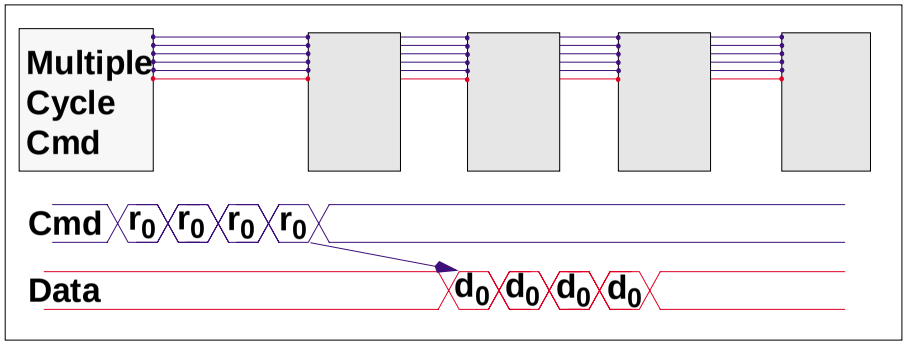
Access Protocol

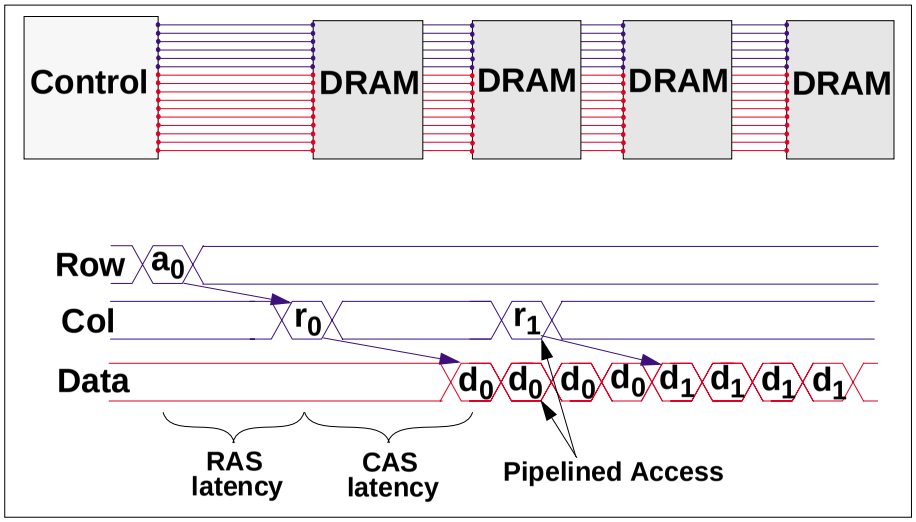


Single Cycle Command



Multiple Cycle Command

Access Protocol (r/r)



Consecutive Cache Line Read Requests to Same DRAM Row

Command

Data

a = Active (open page)
r = Read (Column Read)
d = Data (Data chunk)

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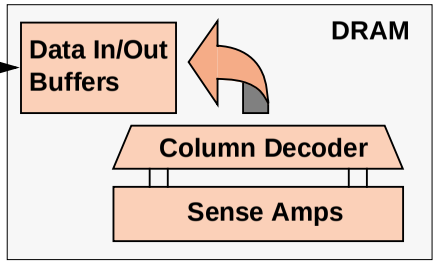
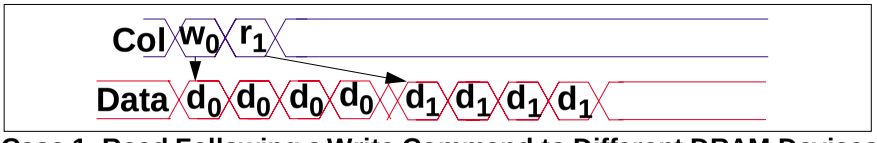
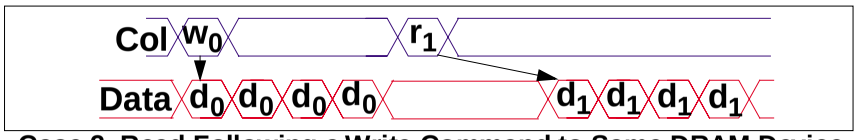
Access Protocol (r/w)

One Datapath - Two Commands

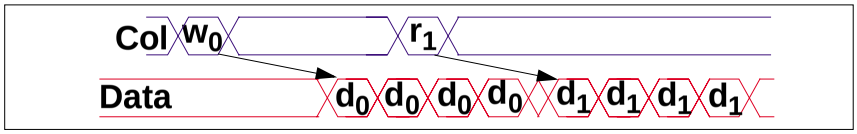




Case 1: Read Following a Write Command to Different DRAM Devices

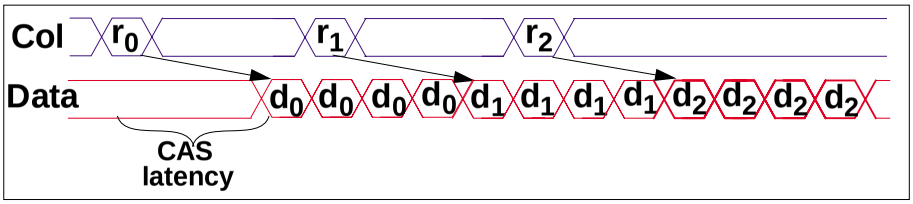


Case 2: Read Following a Write Command to Same DRAM Device

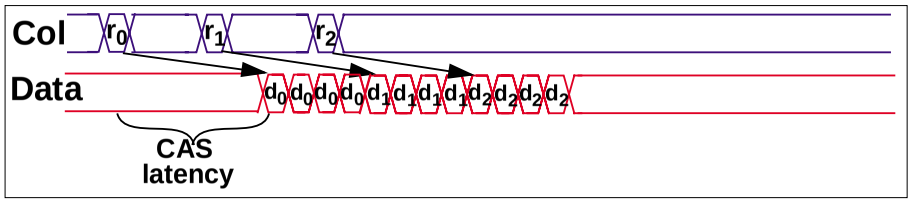


Soln: Delay Data of Write Command to match Read Latency

Access Protocol (pipelines)



Three Back-to-Back Pipelined Read Commands



"Same" Latency, 2X pin frequency, Deeper Pipeline

When pin frequency increases, chips must either

reduce "real latency", or
support longer bursts, or
pipeline more commands.

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David Wang
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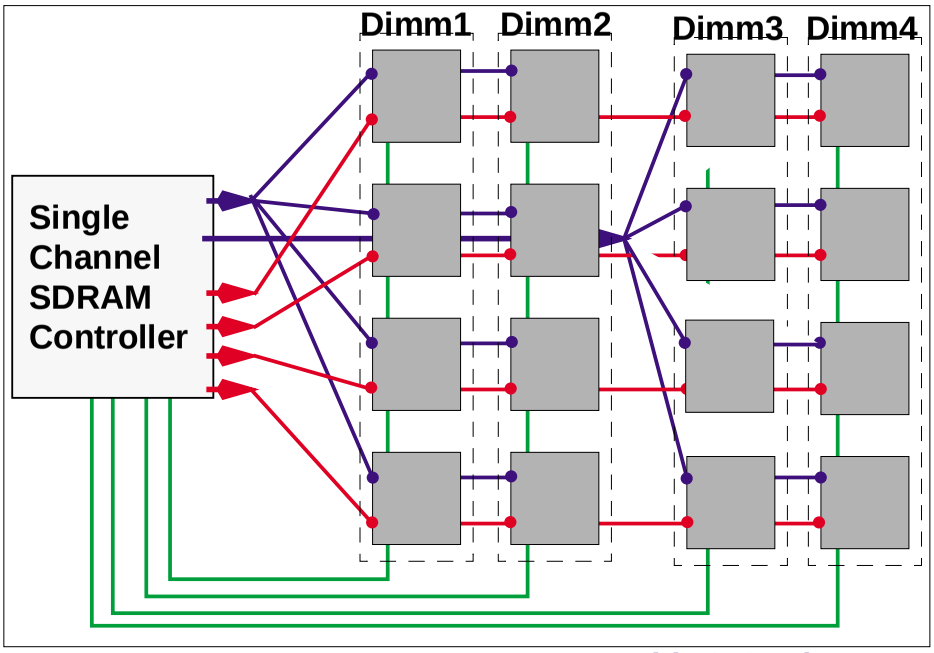
Outline

- **Basics**
- **DRAM Evolution: *Structural Path***
- **Advanced Basics**
- **DRAM Evolution: *Interface Path***
- **SDRAM, DDR SDRAM, RDRAM Memory System Comparisons**
- **Processor-Memory System Trends**
- **RLDRAM, FCRAM, DDR II Memory Systems Summary**
- **Future Interface Trends & Research Areas**
- **Performance Modeling: *Architectures, Systems, Embedded***

SDRAM System In Detail



"Mesh Topology"

Addr & Cmd
Data Bus
Chip (DIMM) Select

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SDRAM Chip

133 MHz (7.5ns cycle time)

Multiplexed Command/Address Bus

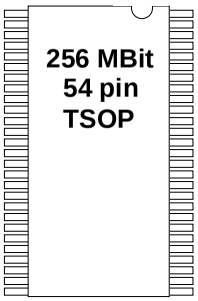
Programmable Burst Length, 1,2,4 or 8

Quad Banks Internally

Supply Voltage of 3.3V

Low Latency, CAS = 2 , 3

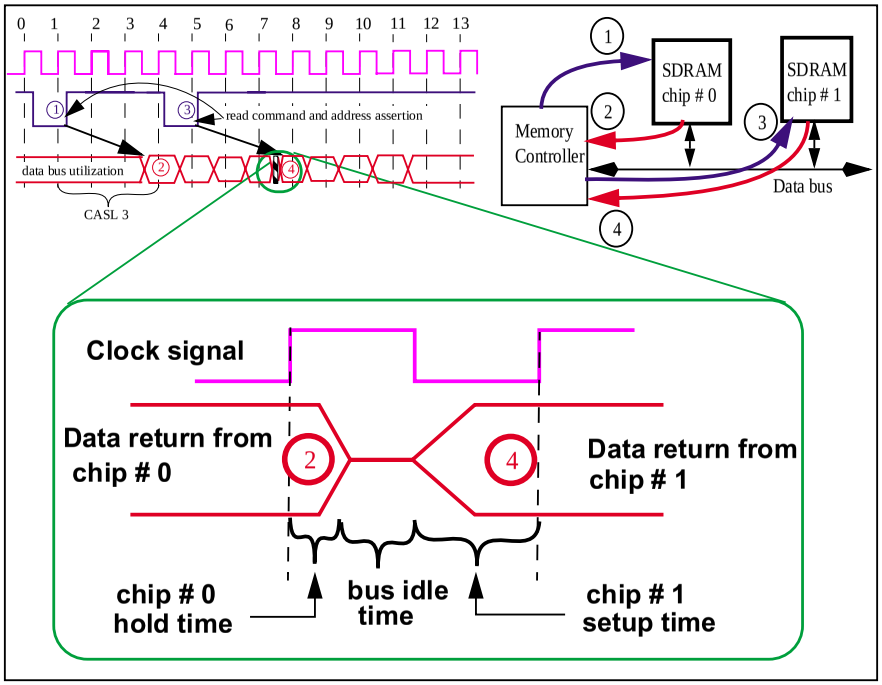
LVTTL Signaling (0.8V to 2.0V)
(0 to 3.3V rail to rail.)



14 Pwr/Gnd
16 Data
15 Addr
7 Cmd
1 Clk
1 NC

Condition Specification	Cur.	Pwr
Operating (Active) Burst = Continous	300mA	1W
Operating (Active) Burst = 2	170mA	560mW
Standby (Active) All banks active	60mA	200mW
Standby (powerdown) All banks inactive	2mA	6.6mW

SDRAM Access Protocol (r/r)



Back-to-back Memory Read Accesses to Different Chips in SDRAM

Clock Cycles are still long enough to allow for pipelined back-to-back Reads

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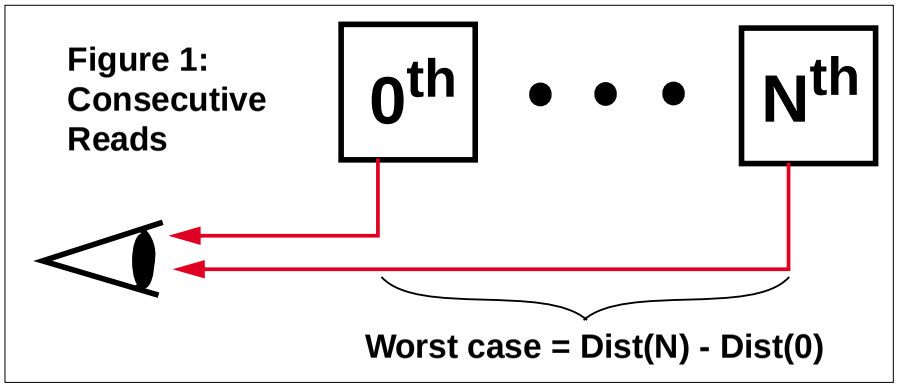
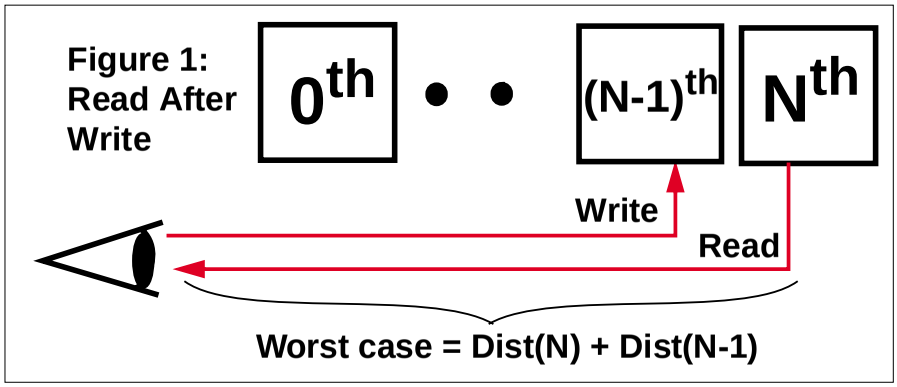
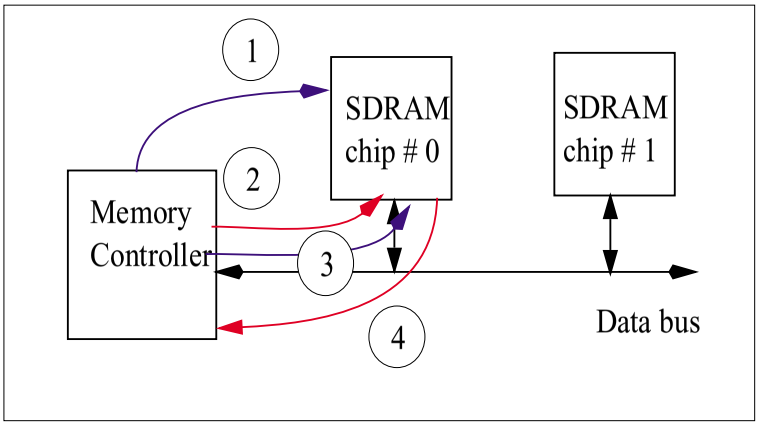
SDRAM Access Protocol (w/r)

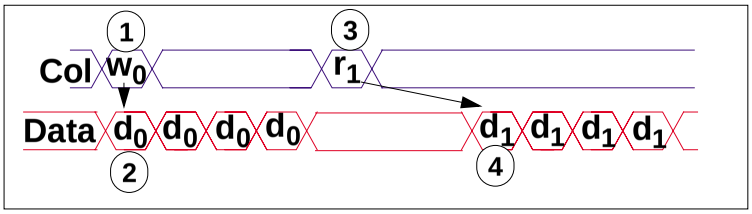




Bus Turn Around

SDRAM Access Protocol (w/r)





Read Following a Write Command to Same SDRAM Device

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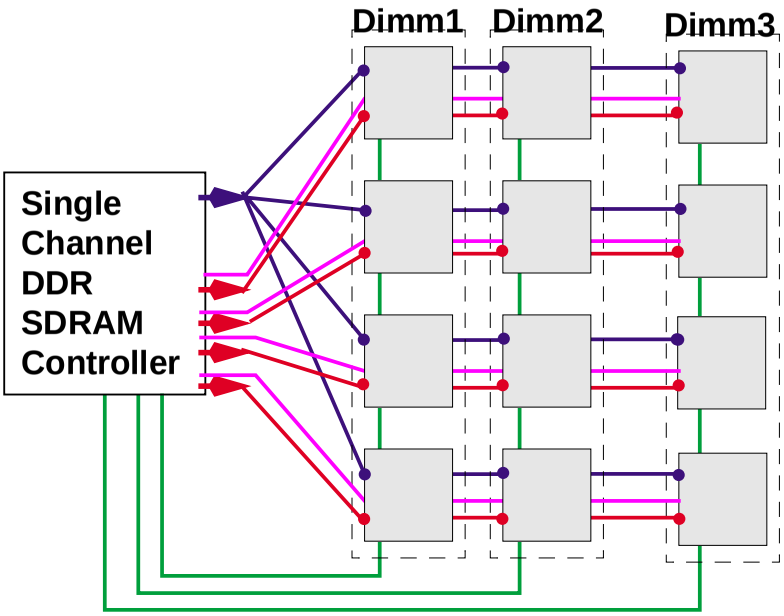
DDR SDRAM System



Same Topology as SDRAM

- Addr & Cmd
- Data Bus
- DQS (Data Strobe)
- Chip (DIMM) Select

DDR SDRAM Chip

133 MHz (7.5ns cycle time)

Multiplexed Command/Address Bus

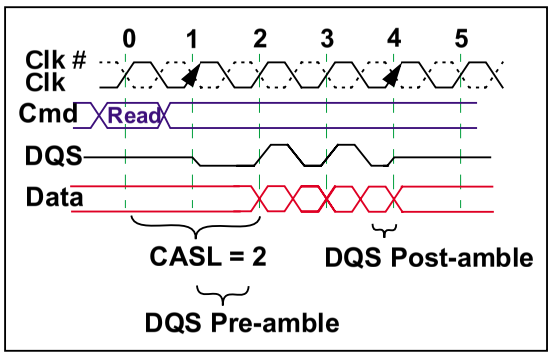
Programmable Burst Lengths, 2, 4 or 8*

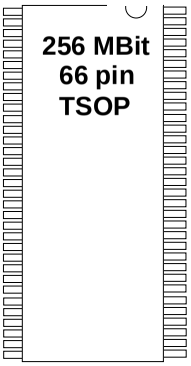
Quad Banks Internally

Supply Voltage of 2.5V*

Low Latency, CAS = 2 , 2.5, 3 *

SSTL-2 Signaling (Vref +/- 0.15V)
(0 to 2.5V rail to rail)





16 Pwr/Gnd*
16 Data
15 Addr
7 Cmd
2 Clk *
7 NC *
2 DQS *
1 Vref *

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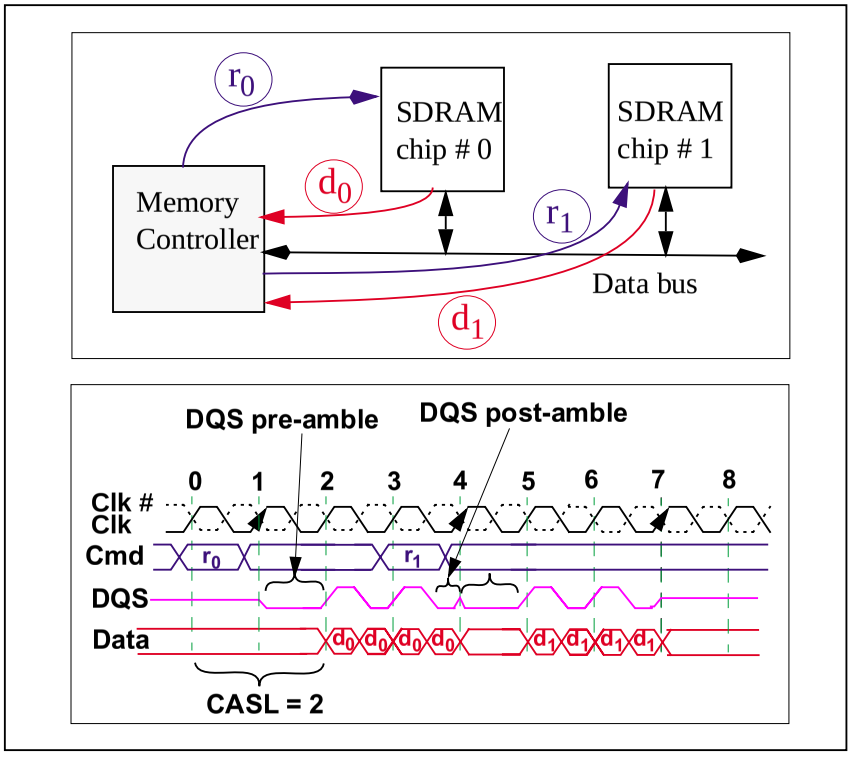
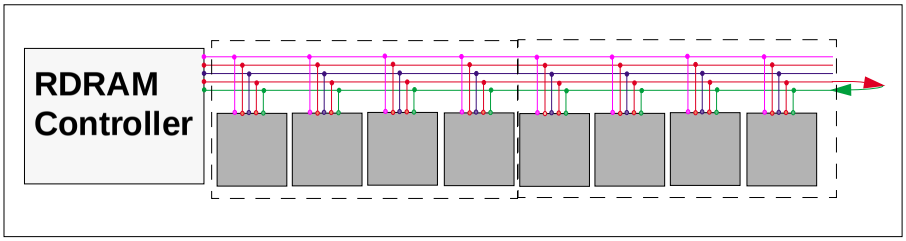
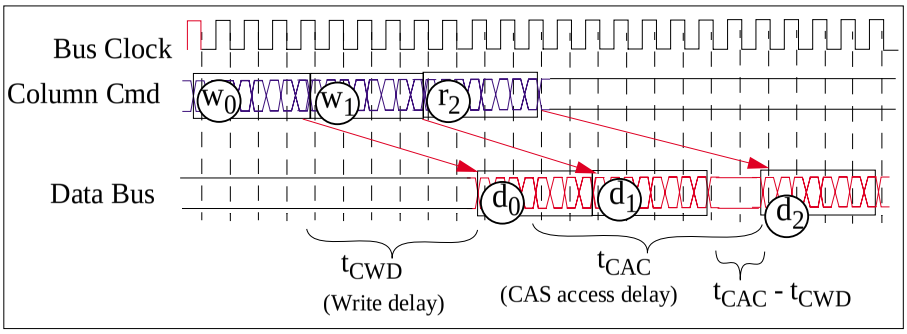
DDR SDRAM Protocol (r/r)



Back-to-back Memory Read Accesses to Different Chips in DDR SDRAM

RDRAM System





Two Write Commands Followed by a Read Command

Packet Protocol : Everything in 8 (half) cycle packets

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Direct RDRAM Chip

400 MHz (2.5ns cycle time)

Separate Row-Col Command Busses

Burst Length = 8*

4/16/32 Banks Internally*

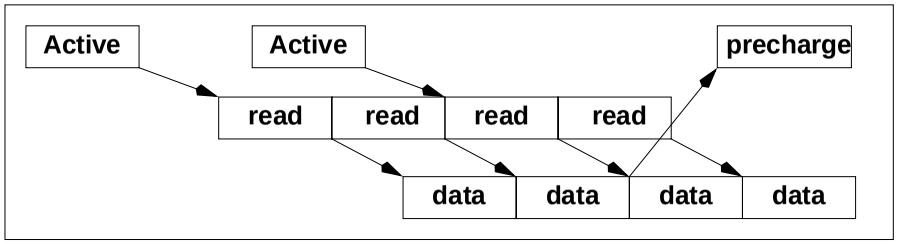
Supply Voltage of 2.5V*

Low Latency, CAS = 4 to 6 full cycles*

RSL Signaling (Vref +/- 0.2V)
(800 mV rail to rail)

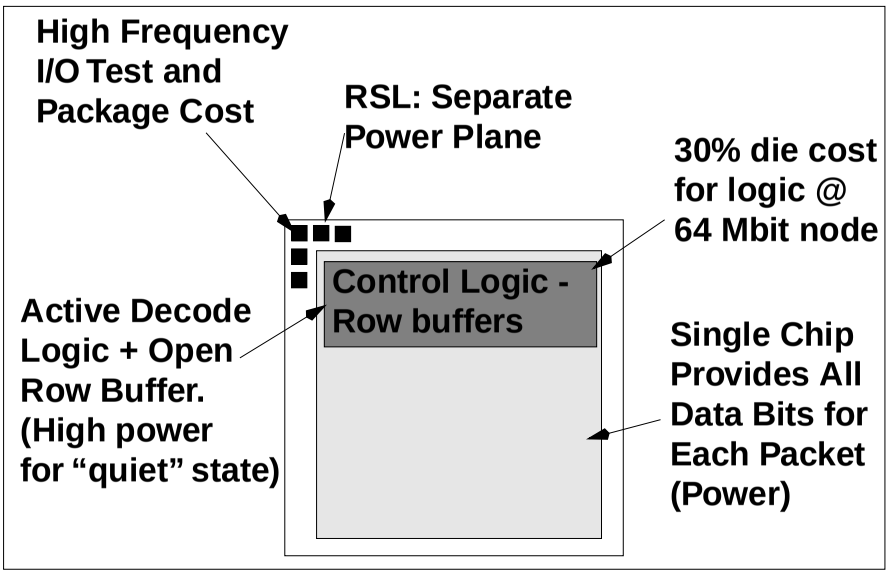
256 MBit
86 pin
FBGA

49 Pwr/Gnd*
16 Data
8 Addr/Cmd
4 Clk*
6 CTL *
2 NC
1 Vref *



All packets are 8 (half) cycles in length, the protocol allows near 100% bandwidth utilization on all channels. (Addr/Cmd/Data)

RDRAM Drawbacks



Significant Cost Delta for First Generation

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System Comparison

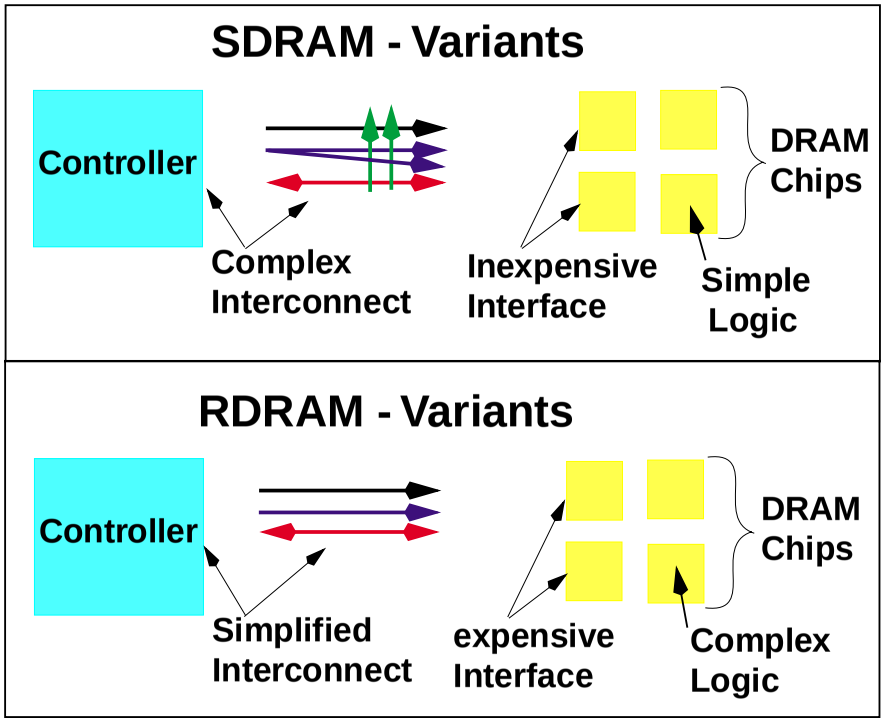
	SDRAM	DDR	RDRAM
Frequency (MHz)	133	133*2	400*2
Pin Count (Data Bus)	64	64	16
Pin Count (Controller)	102	101	33
Theoretical Bandwidth (MB/s)	1064	2128	1600
Theoretical Efficiency (data bits/cycle/pin)	0.63	0.63	0.48
Sustained BW (MB/s)*	655	986	1072
Sustained Efficiency* (data bits/cycle/pin)	0.39	0.29	0.32
RAS + CAS (t_{RAC}) (ns)	45 ~ 50	45 ~ 50	57 ~ 67
CAS Latency (ns)**	22 ~ 30	22 ~ 30	40 ~ 50

133 MHz P6 Chipset + SDRAM CAS Latency ~ 80 ns

*StreamAdd

**Load to use latency

Differences of Philosophy



Complexity Moved to DRAM

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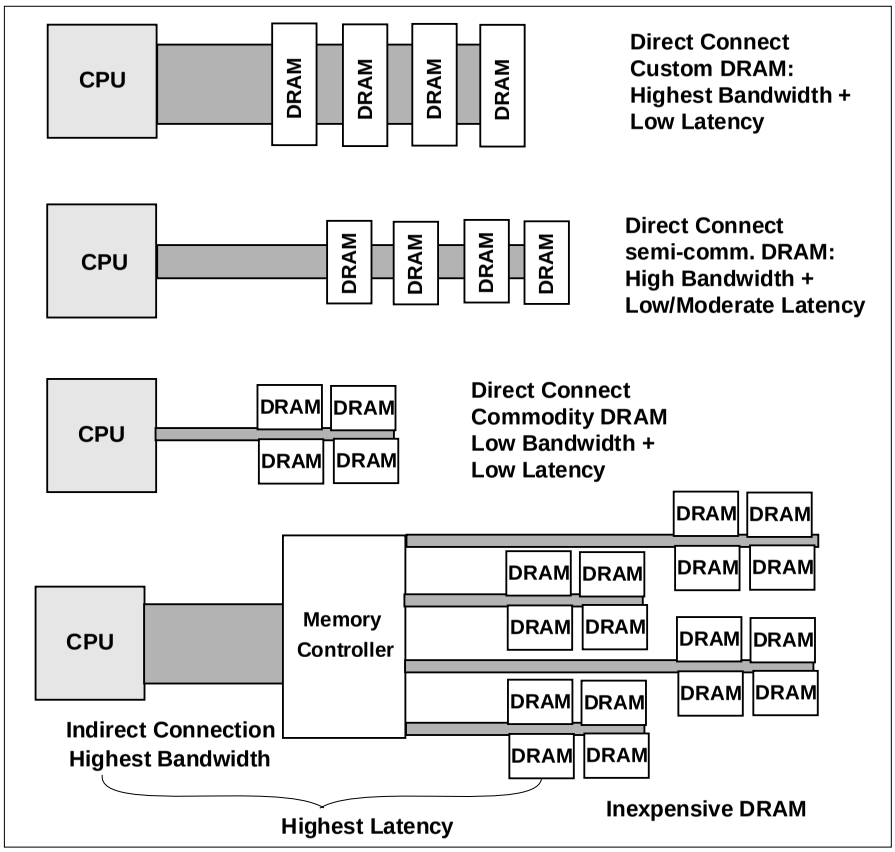
Technology Roadmap (ITRS)

	2004	2007	2010	2013	2016
Semi Generation (nm)	90	65	45	32	22
CPU MHz	3990	6740	12000	19000	29000
MLogicTransistors/ cm^2	77.2	154.3	309	617	1235
High Perf chip pin count	2263	3012	4009	5335	7100
High Performance chip cost (cents/pin)	1.88	1.61	1.68	1.44	1.22
Memory pin cost (cents/pin)	0.34 - 1.39	0.27 - 0.84	0.22 - 0.34	0.19 - 0.39	0.19 - 0.33
Memory pin count	48-160	48-160	62-208	81-270	105-351

Trend: **Free Transistors & Costly Interconnects**

Choices for Future



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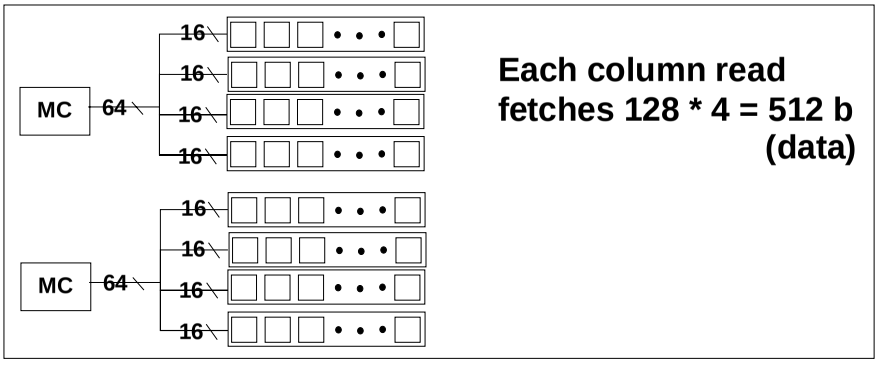
EV7 + RDRAM (Compaq/HP)

- RDRAM Memory (2 Controllers)
- Direct Connection to processor
- 75ns Load to use latency
- 12.8 GB/s Peak bandwidth
- 6 GB/s read or write bandwidth
- 2048 open pages (2 * 32 * 32)



What if EV7 Used DDR?

- **Peak Bandwidth 12.8 GB/s**
- **6 Channels of 133*2 MHz DDR SDRAM ==**
- **6 Controllers of 6 64 bit wide channels, or**
- **3 Controllers of 3 128 bit wide channels**

System	EV7 + RDRAM	EV7 + 6 controller DDR SDRAM	EV7 + 3 controller DDR SDRAM
Latency	75 ns	~ 50 ns*	~ 50 ns*
Pin count	~265** + Pwr/Gnd	~ 600** + Pwr/Gnd	~ 600** + Pwr/Gnd
Controller Count	2	6***	3***
Open pages	2048	144	72

* page hit CAS + memory controller latency.
** including all signals, address, command, data, clock, not including ECC or parity
*** 3 controller design is less bandwidth efficient.

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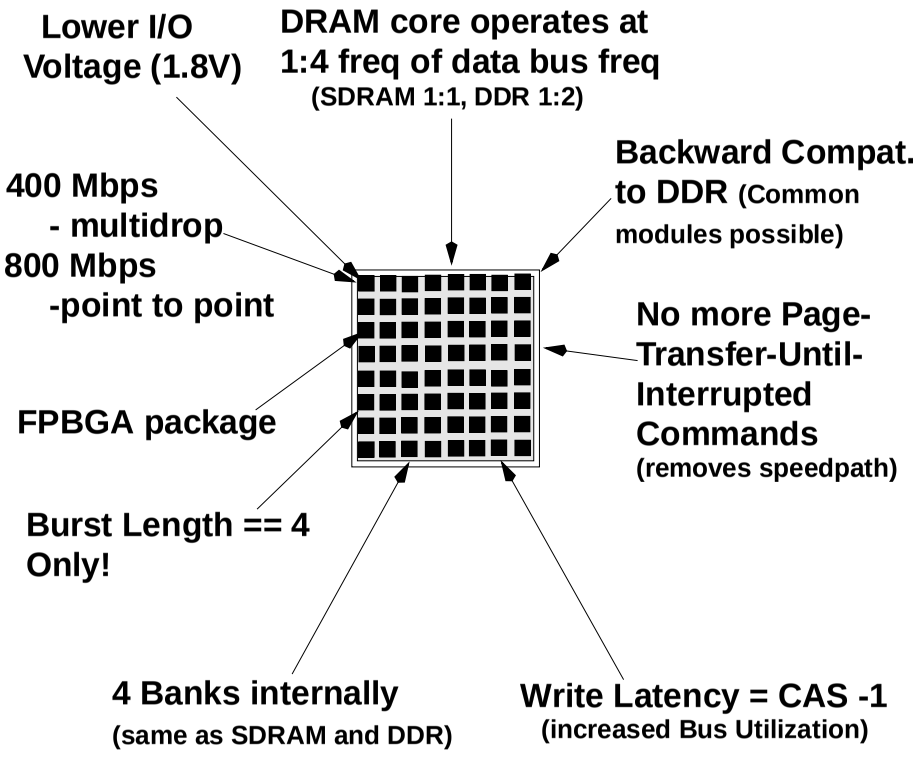
What's Next?

- **DDR II**
- **FCRAM**
- **RLDRAM**
- **RDRAM (Yellowstone etc)**
- **Kentron QBM**

DDR II - DDR Next Gen



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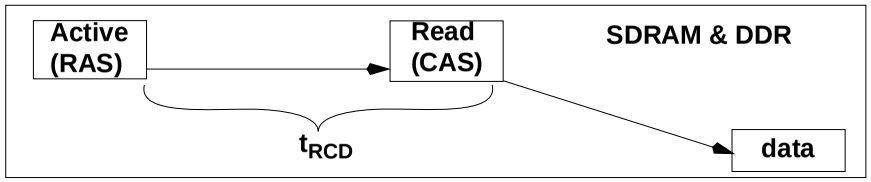
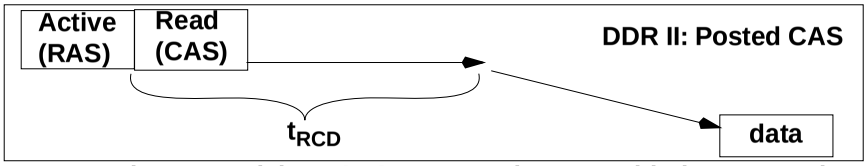
DDR II - Continued

Posted Commands



SDRAM & DDR SDRAM relies on memory controller to know t_{RCD} and issue CAS after t_{RCD} for lowest latency.



Internal counter delays CAS command, DRAM chip issues “real” command after t_{RCD} for lowest latency.

FCRAM

Fast Cycle RAM (aka Network-DRAM)

Features	DDR SDRAM	FCRAM/Network-DRAM
Vdd, Vddq	2.5 +/- 0.2V	2.5 +/- 0.15
Electrical Interface	SSTL-2	SSTL-2
Clock Frequency	100~167 MHz	154~200 MHz
t_{RAC}	~40ns	22~26ns
t_{RC}	~60ns	25~30ns
# Banks	4	4
Burst Length	2,4,8	2,4
Write Latency	1 Clock	CASL -1

FCRAM/Network-DRAM looks like DDR+

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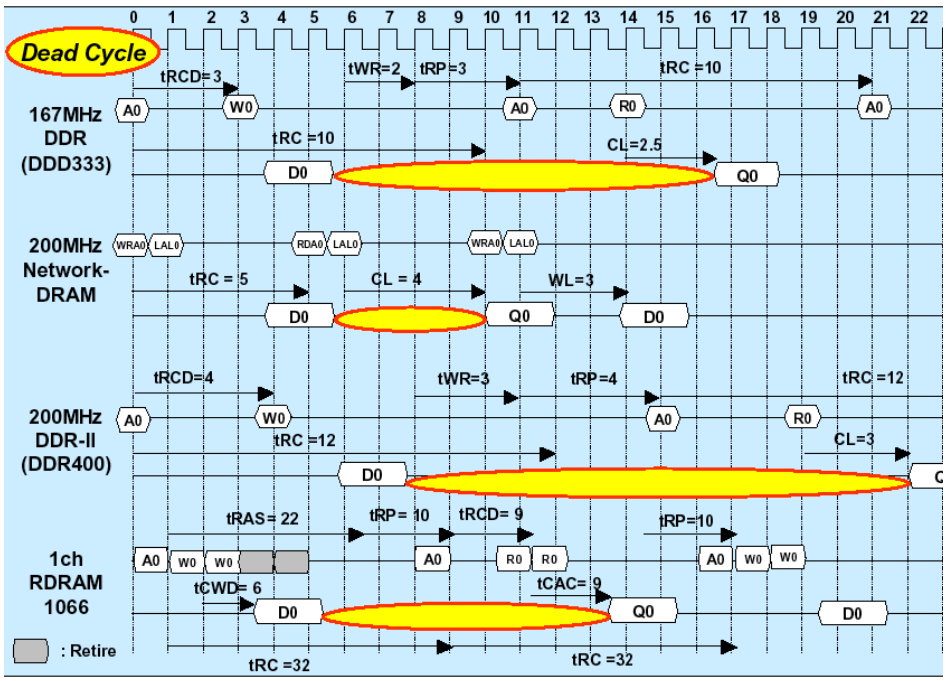
FCRAM Continued



Faster t_{RC} allows Samsung to claim higher bus efficiency

*** Samsung Electronics, Denali MemCon 2002**

RLDRAM

DRAM Type	Frequency	Bus Width (per chip)	Peak Bandwidth (per Chip)	Random Access Time (t_{RAC})	Row Cycle Time (t_{RC})
PC133 SDRAM	133	16	200 MB/s	45 ns	60 ns
DDR 266	133 * 2	16	532 MB/s	45 ns	60 ns
PC800 RDRAM	400 * 2	16	1.6 GB/s	60 ns	70 ns
FCRAM	200 * 2	16	0.8 GB/s	25 ns	25 ns
RLDRAM	300 * 2	32	2.4 GB/s	25 ns	25 ns

Comparable to FCRAM in latency
Higher Frequency (No Connectors)
non-Multiplexed Address (SRAM like)

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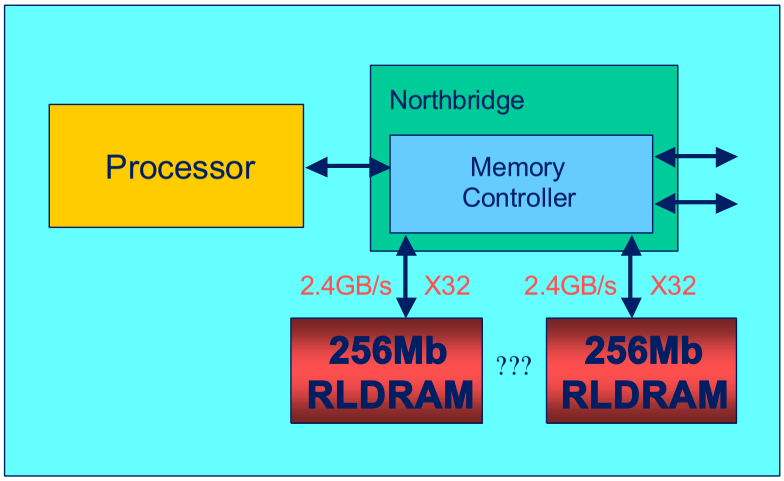
RLDRAM Continued

High-end PC and Server

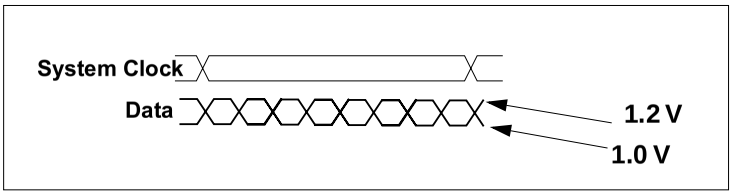


RLDRAM is a great replacement to SRAM in L3 cache applications because of its high density, low power and low cost

*Infineon Presentation, Denali MemCon 2002

RAMBUS Yellowstone

- Bi-Directional Differential Signals
- Ultra low 200mV p-p signal swings
- 8 data bits transferred per clock
- 400 MHz system clock
- 3.2 GHz effective data frequency
- Cheap 4 layer PCB
- Commodity packaging



Octal Data Rate (ODR) Signaling

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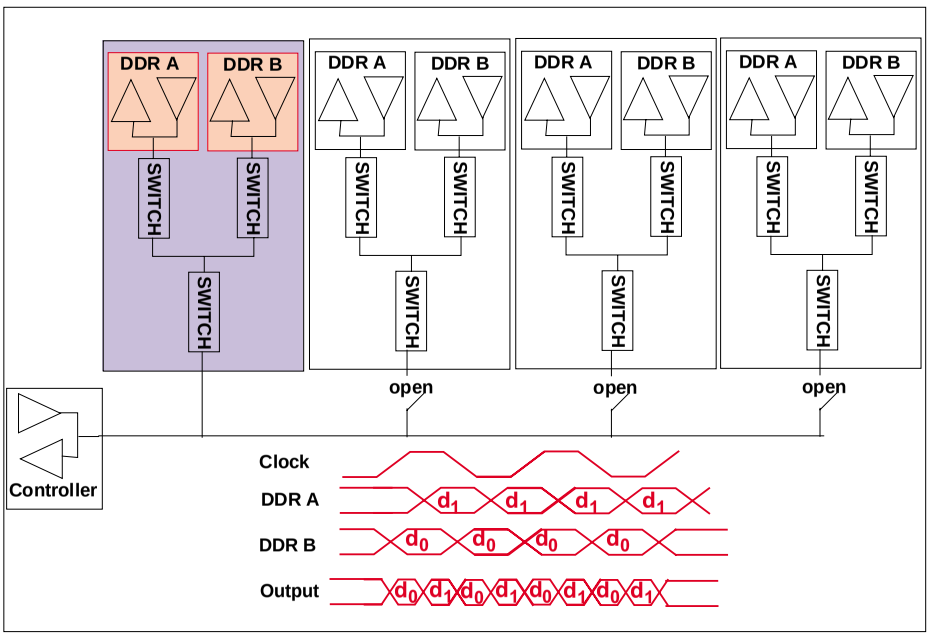
Kentron QBM™



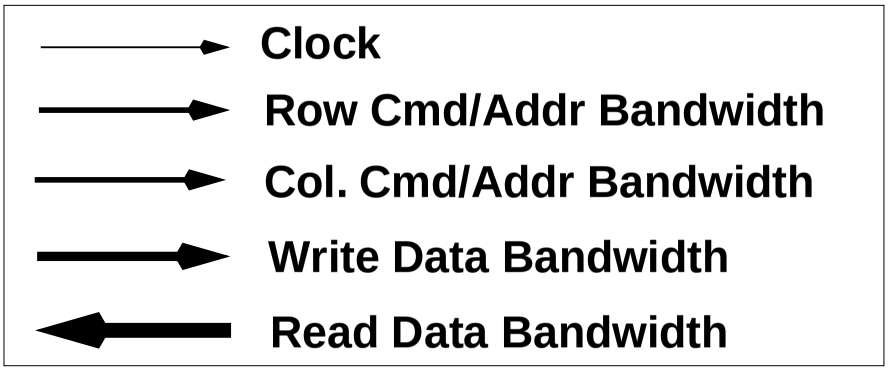
"Wrapper Electronics around DDR memory"

Generates 4 data bits per cycle instead of 2.

Quad Band Memory

A Different Perspective

Everything is bandwidth



Latency and Bandwidth

Pin-bandwidth and

Pin-transition *Efficiency (bits/cycle/sec)

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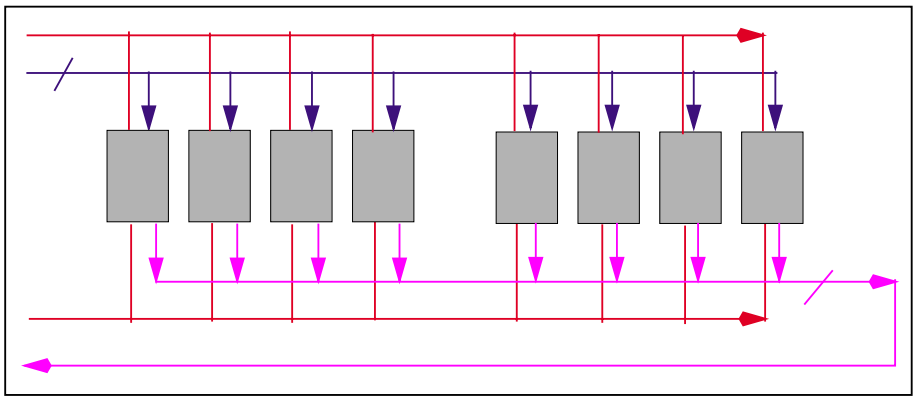
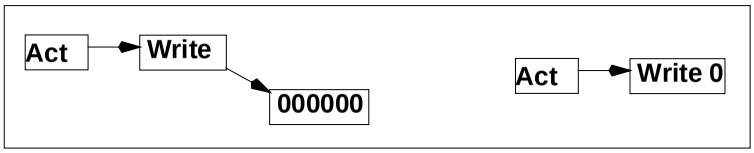
Research Areas: Topology



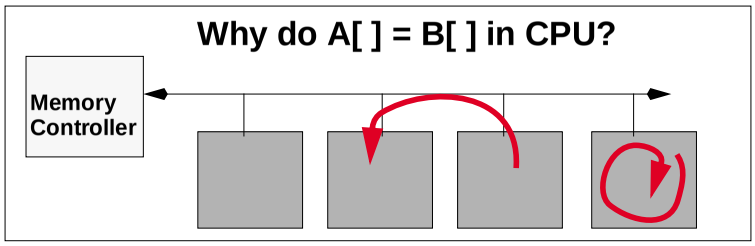
Unidirectional Topology:

- **Write Packets sent on Command Bus**
- **Pins used for Command/Address/Data**
- **Further Increase of Logic on DRAM chips**

Memory Commands?



Instead of A[ ] = 0; Do “write 0”



Move Data inside of DRAM or between DRAMs.

Why do STREAMadd in CPU?

A[ ] = B[ ] + C[ ]

Active Pages *(Chong et. al. ISCA ‘98)

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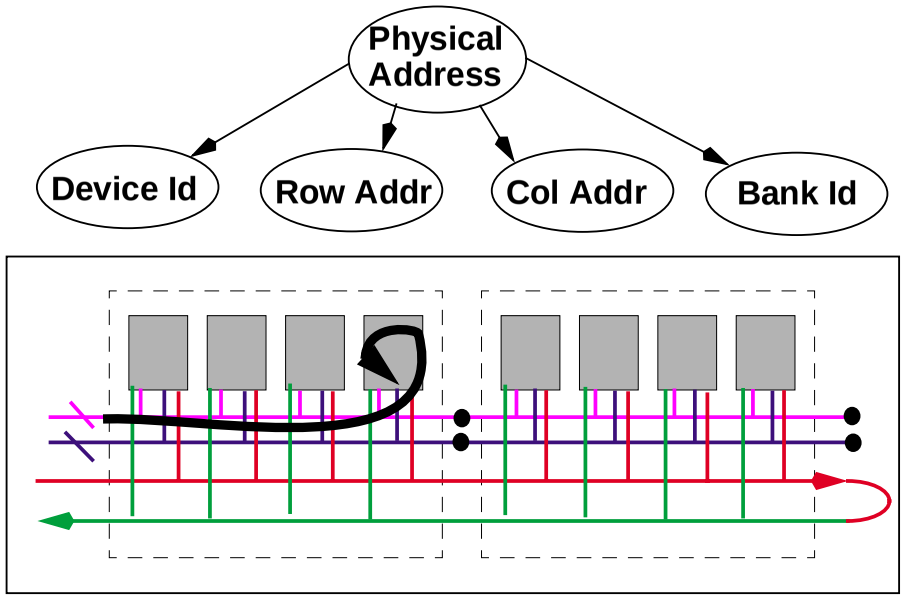
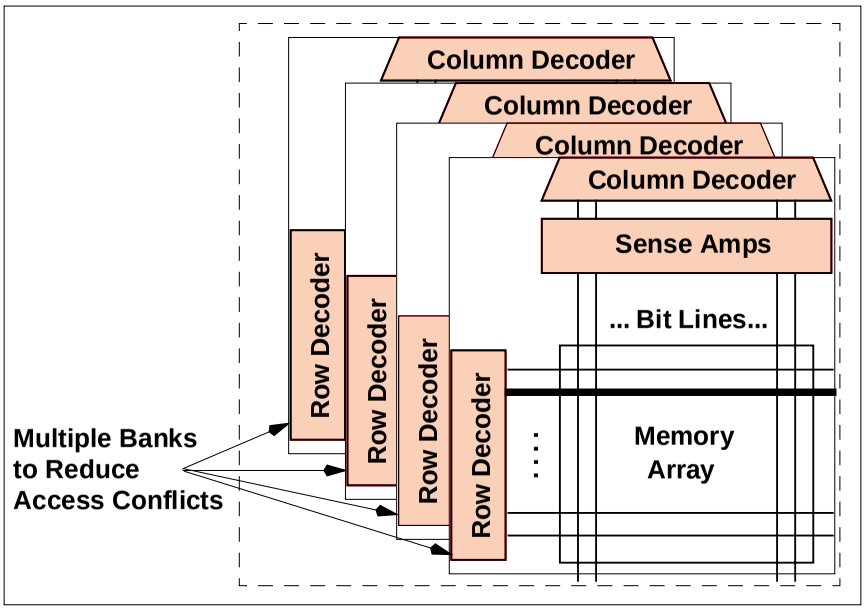
Address Mapping



Access Distribution for Temp Control
Avoid Bank Conflicts
Access Reordering for performance

Example: Bank Conflicts



Read 05AE5700 → Device id 3, Row id 266, Bank id 0
Read 023BB880 → Device id 3, Row id 1BA, Bank id 0
Read 05AE5780 → Device id 3, Row id 266, Bank id 0
Read 00CBA2C0 → Device id 3, Row id 052, Bank id 1

More Banks per Chip == Performance == Logic Overhead

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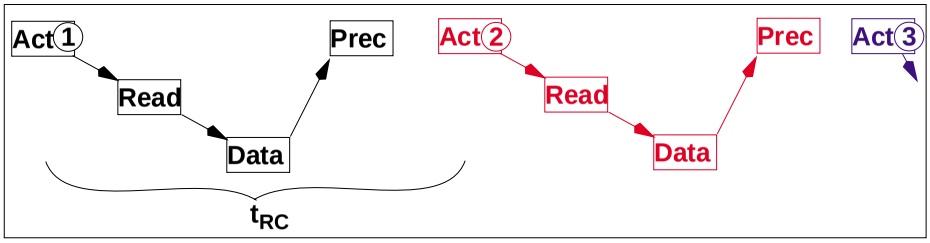
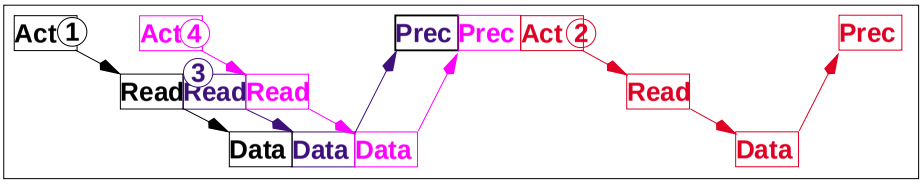
Example: Access Reordering

1 Read 05AE5700 → Device id 3, Row id 266, Bank id 0
2 Read 023BB880 → Device id 3, Row id 1BA, Bank id 0
3 Read 05AE5780 → Device id 3, Row id 266, Bank id 0
4 Read 00CBA2C0 → Device id 1, Row id 052, Bank id 1



Strict Ordering



Memory Access Re-ordered

Act = Activate Page (Data moved from DRAM cells to row buffer)
Read = Read Data (Data moved from row buffer to memory controller)
Prec = Precharge (close page/evict data in row buffer/sense amp)

Outline

- **Basics**
- **DRAM Evolution: *Structural Path***
- **Advanced Basics**
- **DRAM Evolution: *Interface Path***
- **Future Interface Trends & Research Areas**
- **Performance Modeling:**
  Architectures*, *Systems*, *Embedded

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Simulator Overview

CPU: SimpleScalar v3.0a

- **8-way out-of-order**
- **L1 cache: split 64K/64K, lockup free x32**
- **L2 cache: unified 1MB, lockup free x1**
- **L2 blocksize: 128 bytes**

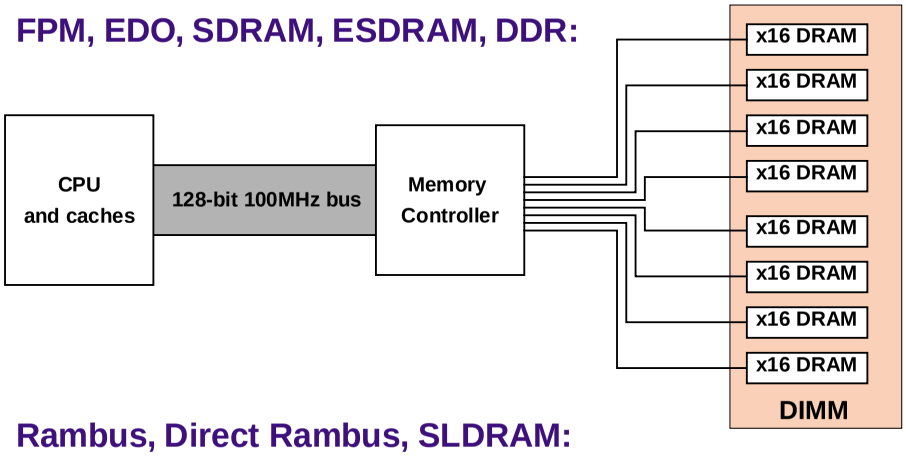
Main Memory: 8 64Mb DRAMs

- **100MHz/128-bit memory bus**
- **Optimistic *open-page* policy**

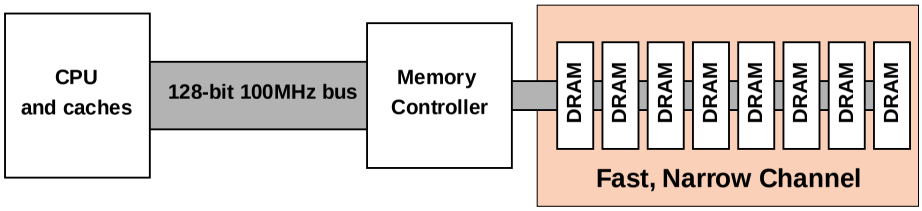
Benchmarks: SPEC ’95

DRAM Configurations

FPM, EDO, SDRAM, ESDRAM, DDR:



Rambus, Direct Rambus, SLDRAM:



Note: TRANSFER WIDTH of Direct Rambus Channel

- **equals that of ganged FPM, EDO, etc.**
- **is 2x that of Rambus & SLDRAM**

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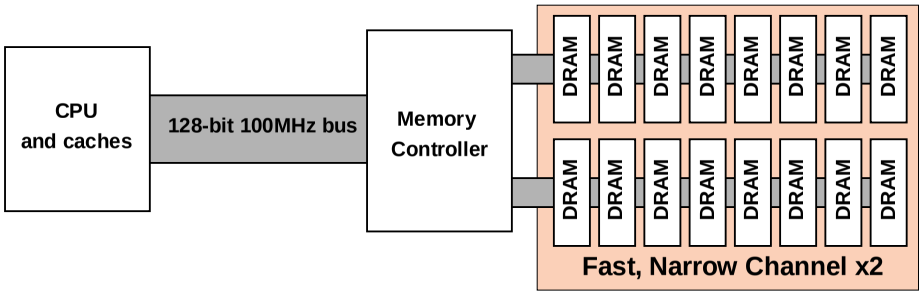
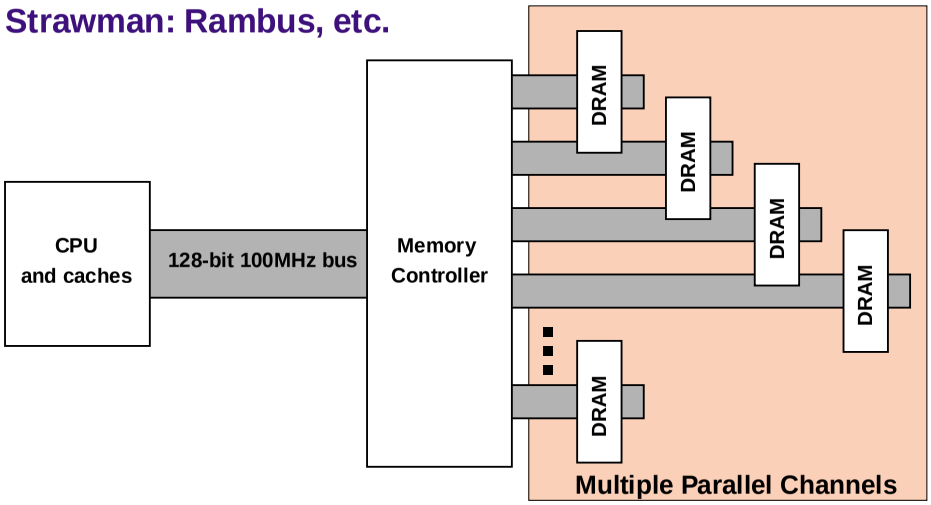
DRAM Configurations

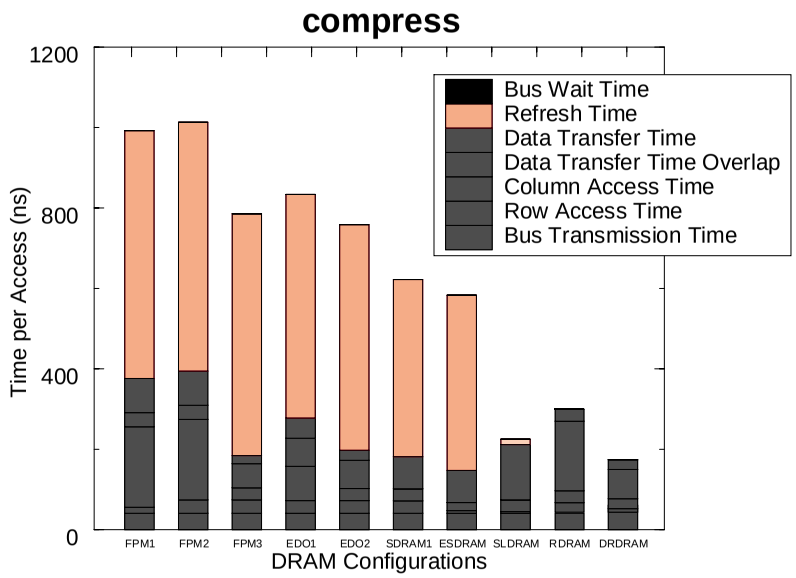
Rambus & SLDRAM dual-channel:



Strawman: Rambus, etc.



First … Refresh Matters



Assumes refresh of each bank every 64ms

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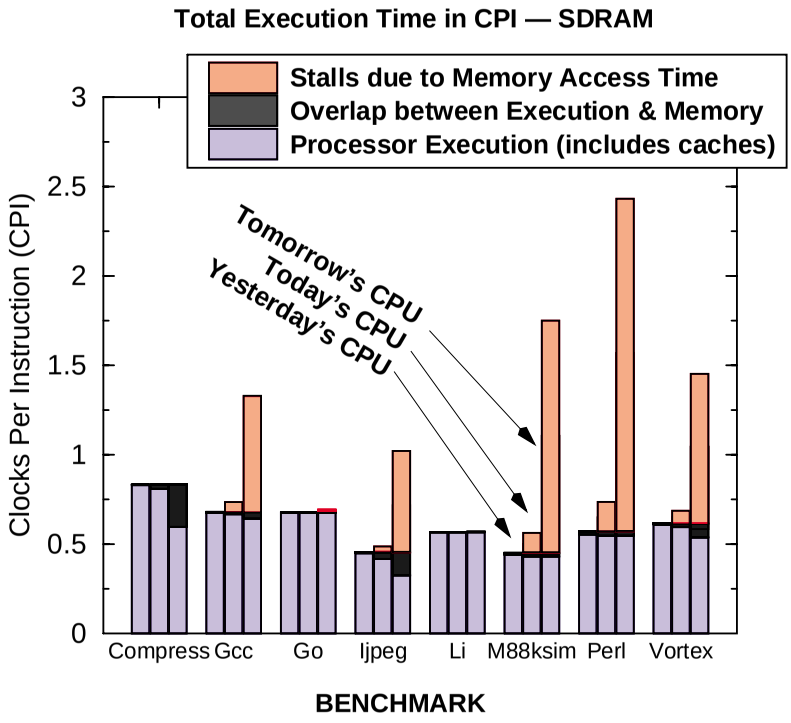
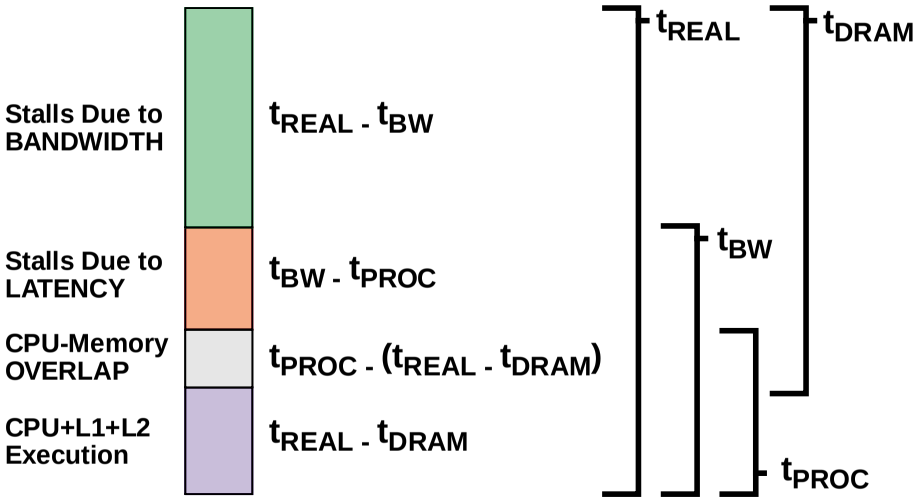
Overhead: Memory vs. CPU



Variable: speed of processor & caches

Definitions (var. on Burger, et al)

- t_{PROC} — processor with perfect memory
- t_{REAL} — realistic configuration
- t_{BW} — CPU with wide memory paths
- t_{DRAM} — time seen by DRAM system



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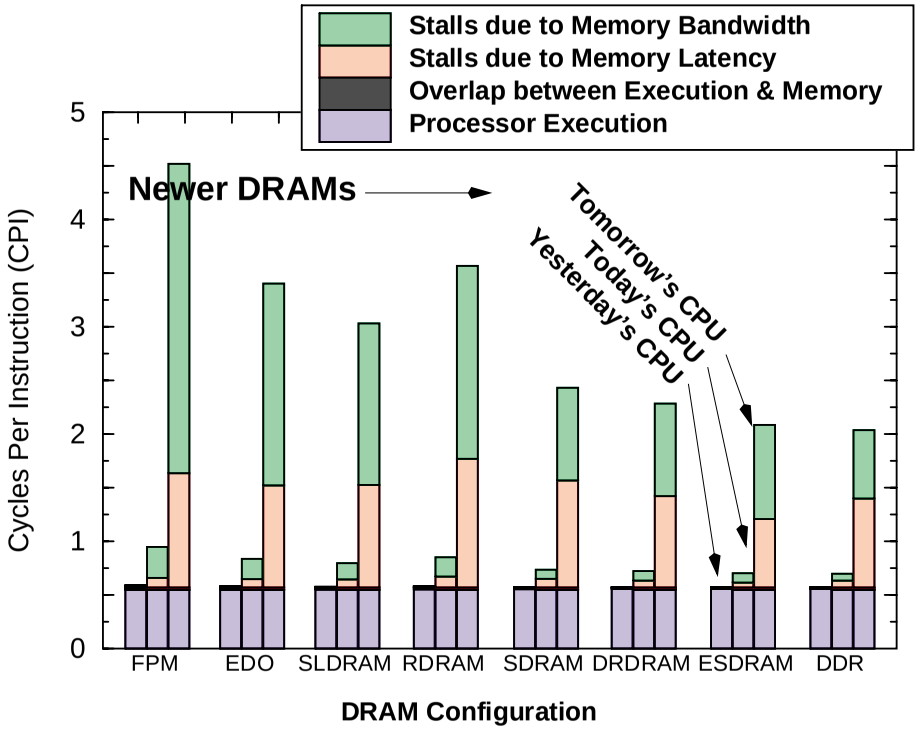
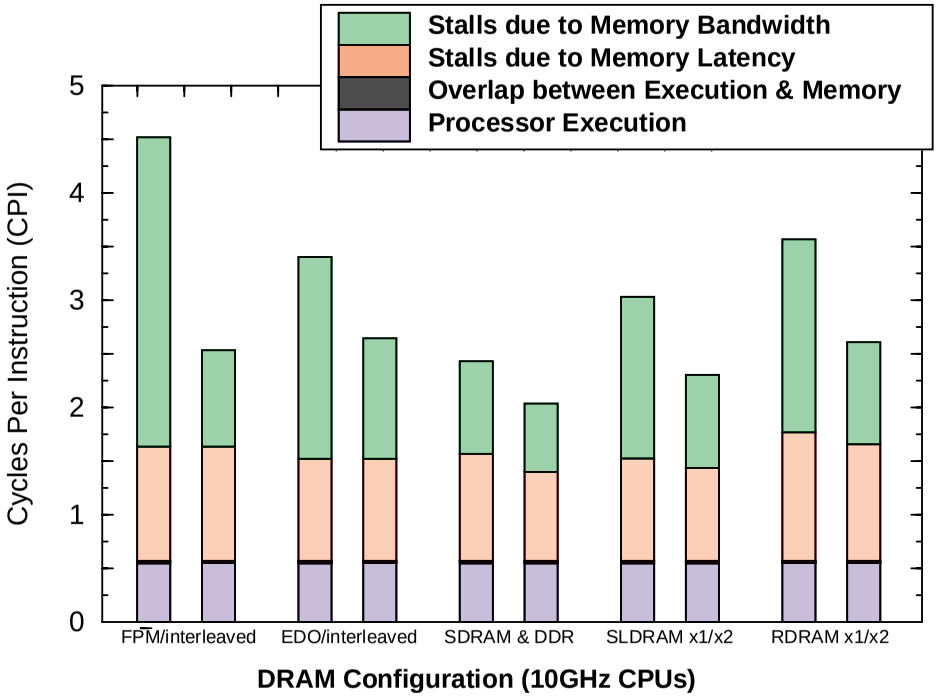
Memory & CPU — PERL

Bandwidth-Enhancing Techniques I:



Memory & CPU — PERL

Bandwidth-Enhancing Techniques II:



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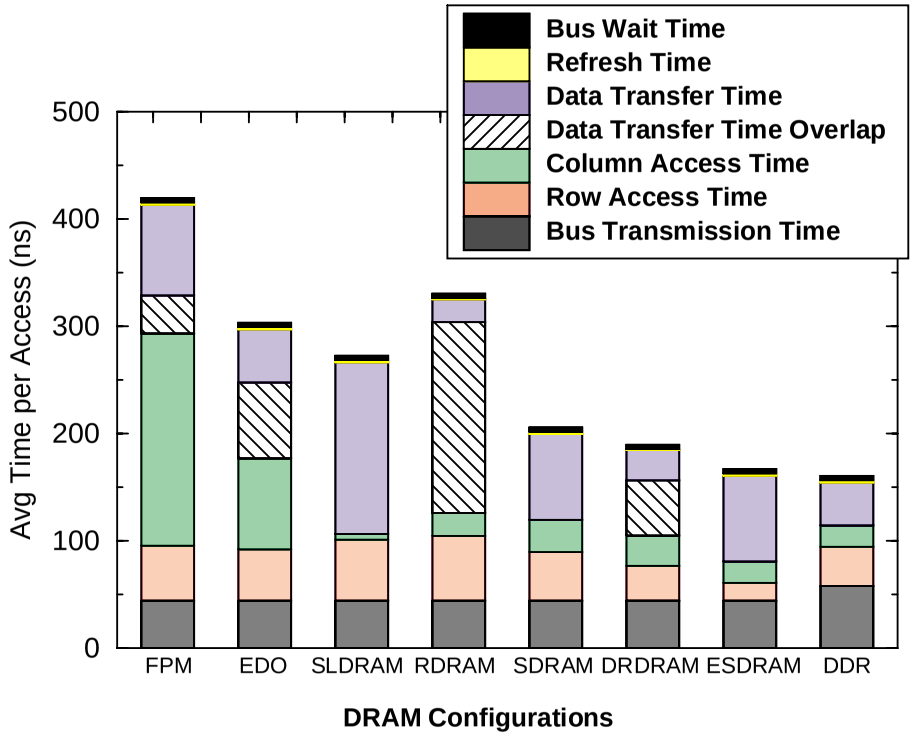
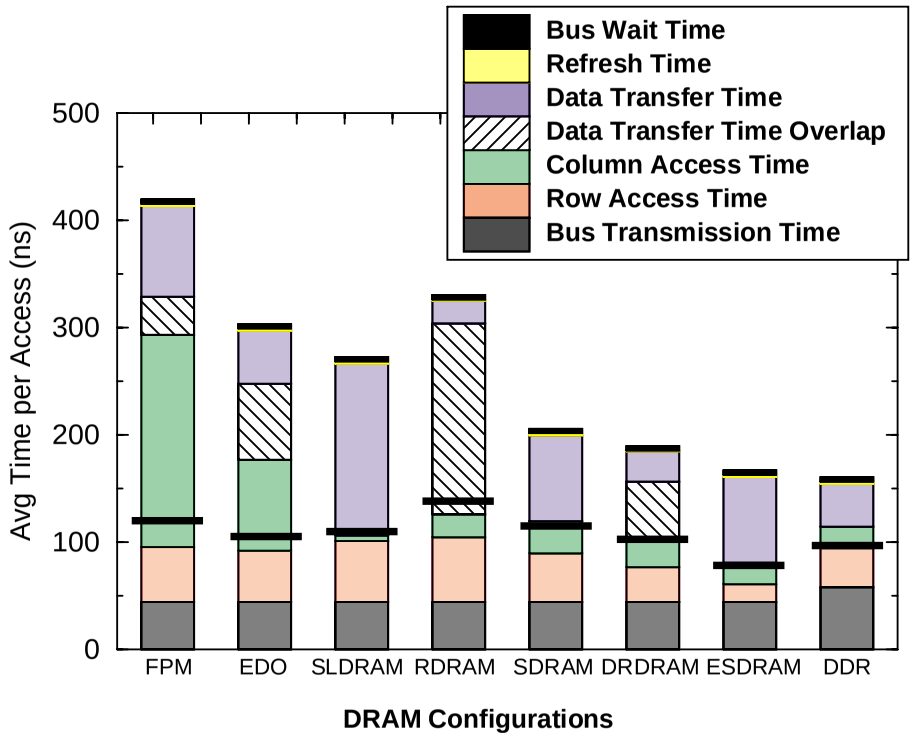
Average Latency of DRAMs



note: SLDRAM & RDRAM 2x data transfers

Average Latency of DRAMs



note: SLDRAM & RDRAM 2x data transfers

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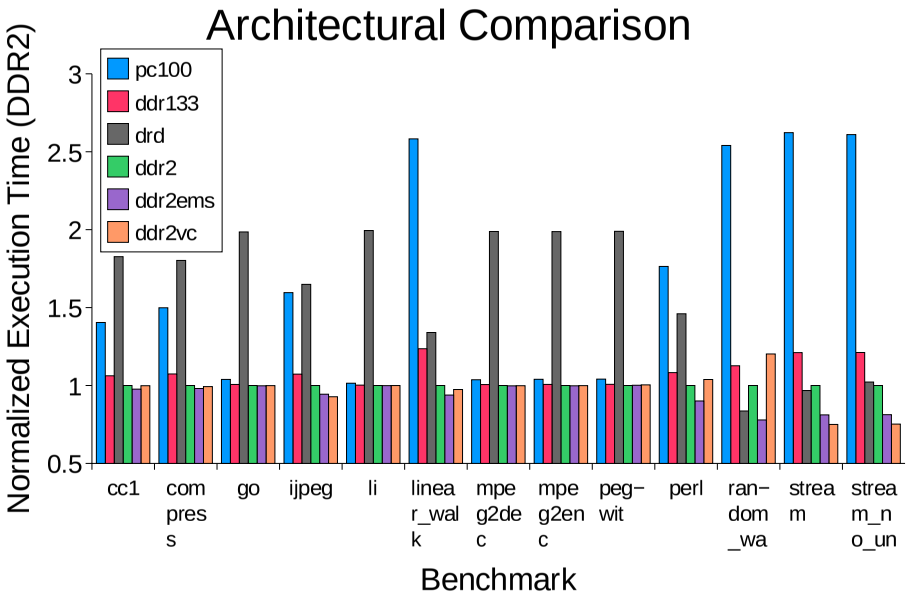
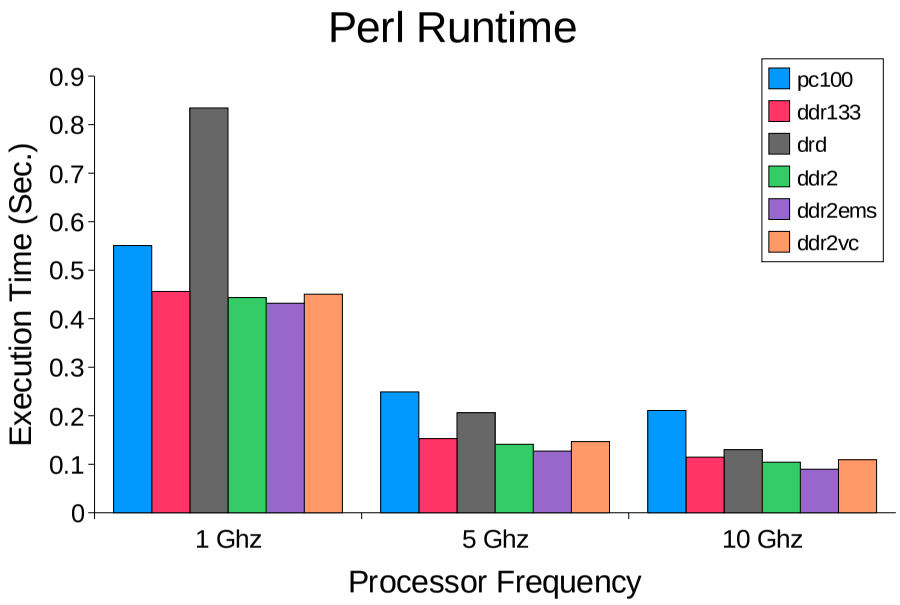
DDR2 Study Results



DDR2 Study Results



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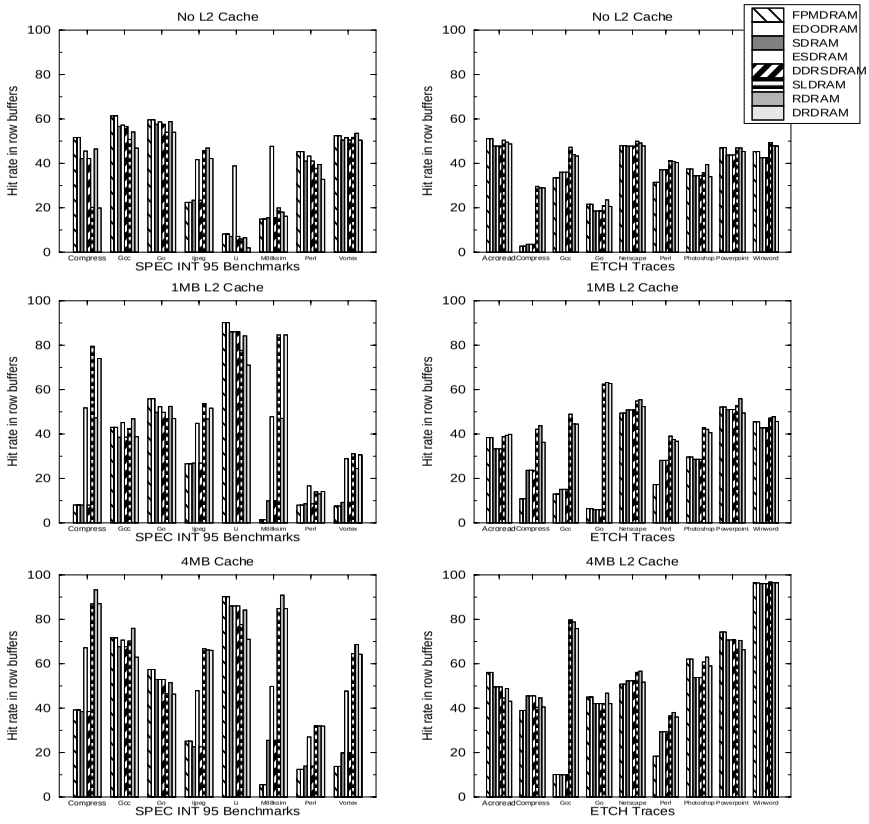
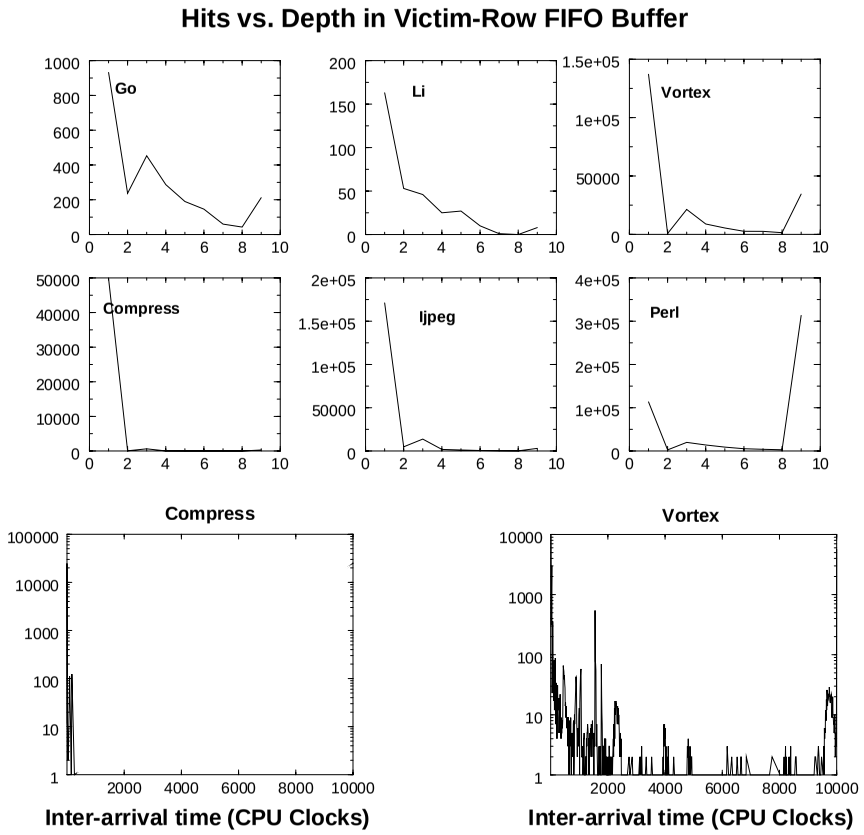
Row-Buffer Hit Rates



Row-Buffer Hit Rates



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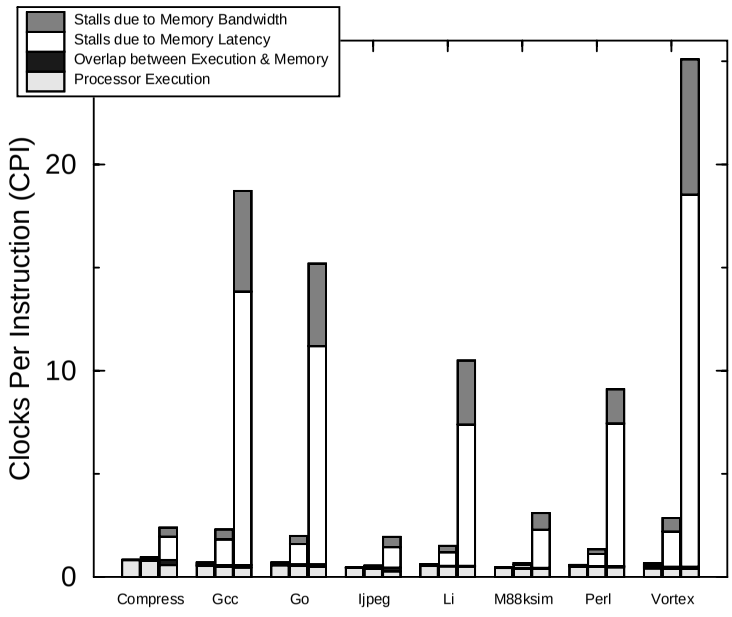
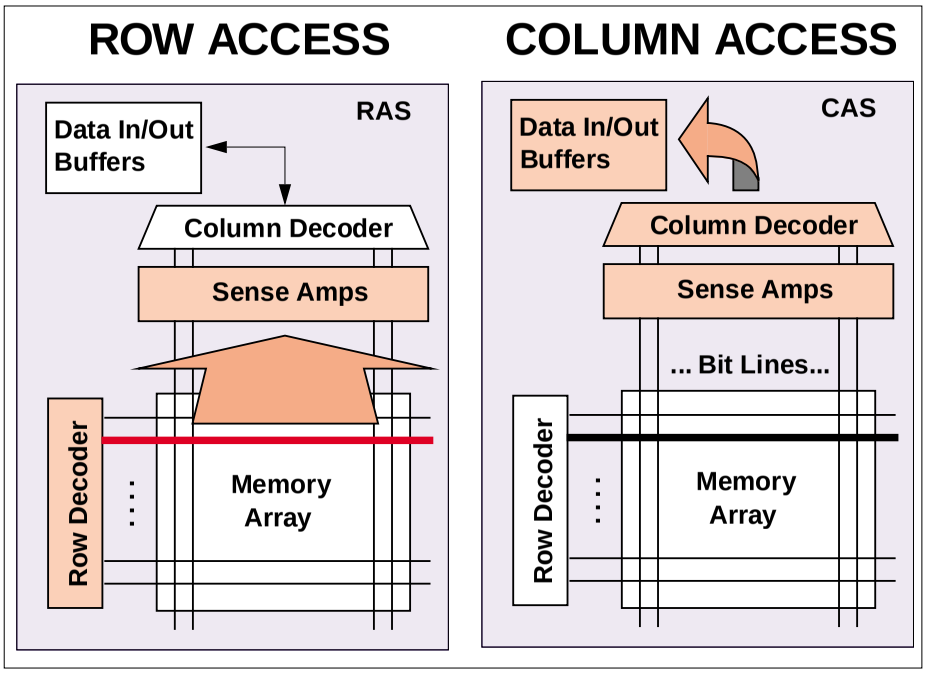
Row Buffers as L2 Cache



Row Buffer Management



RAS is like Cache Access
Why not Speculate?

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Cost-Performance

FPM, EDO, SDRAM, ESDRAM:

- **Lower Latency => Wide/Fast Bus**
- **Increase Capacity => Decrease Latency**
- **Low System Cost**

Rambus, Direct Rambus, SLDRAM:

- **Lower Latency => Multiple Channels**
- **Increase Capacity => Increase Capacity**
- **High System Cost**

However, 1 DRDRAM = Multiple SDRAM

Conclusions

100MHz/128-bit Bus is Current Bottleneck

- **Solution: Fast Bus/es & MC on CPU (*e.g.* Alpha 21364, Emotion Engine, …)**

Current DRAMs Solving Bandwidth Problem (but not Latency Problem)

- **Solution: New cores with on-chip SRAM (*e.g.* ESDRAM, VCDRAM, …)**
- **Solution: New cores with smaller banks (*e.g.* MoSys "SRAM", FCRAM, …)**

Direct Rambus seems to scale best for future high-speed CPUs

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Outline

- **Basics**
- **DRAM Evolution: *Structural Path***
- **Advanced Basics**
- **DRAM Evolution: *Interface Path***
- **Future Interface Trends & Research Areas**
- **Performance Modeling: *Architectures, Systems, Embedded***

Motivation

Even when we restrict our focus …

SYSTEM-LEVEL PARAMETERS

- Number of channels
- Channel latency
- Banks per channel
- Request-queue size
- Row-access
- DRAM precharge
- DRAM buffering
- Number of MSHRs

- Width of channels
- Channel bandwidth
- Turnaround time
- Request reordering
- Column-access
- CAS-to-CAS latency
- L2 cache blocksize
- Bus protocol

Fully | partially | not independent (this study)

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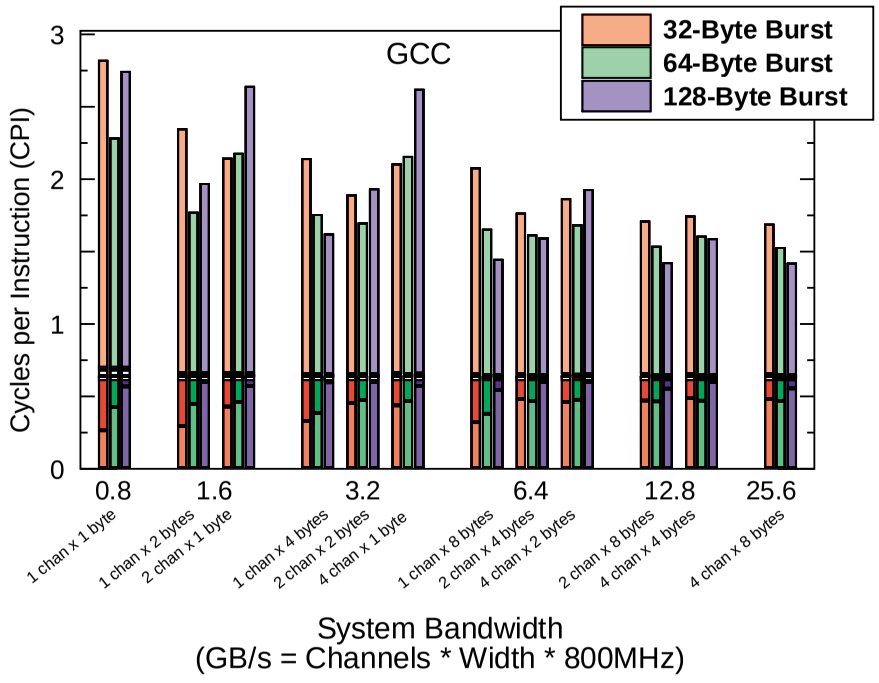
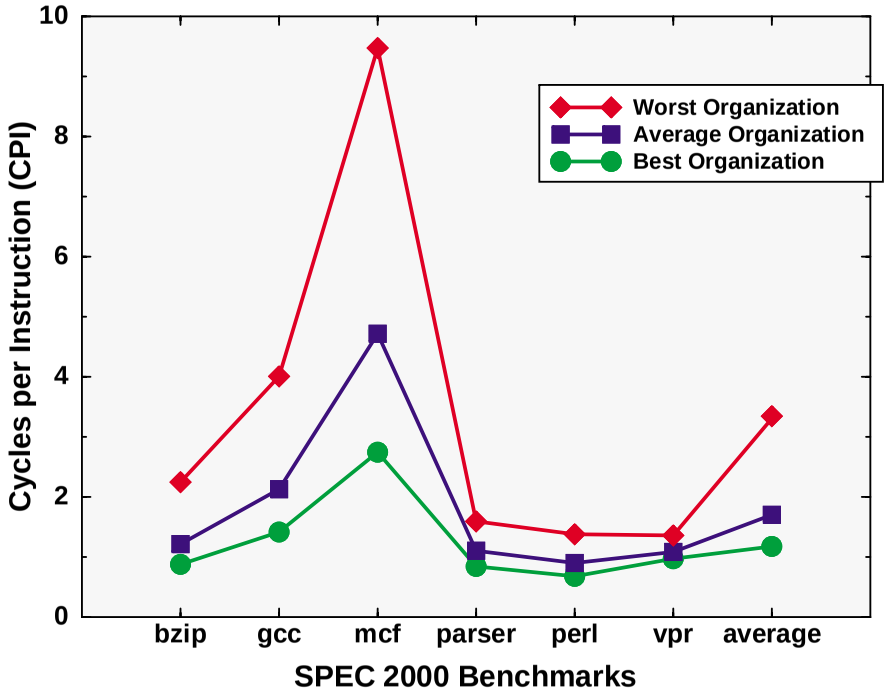
Motivation

... the design space is highly non-linear …



Motivation

... and the cost of poor judgment is high.



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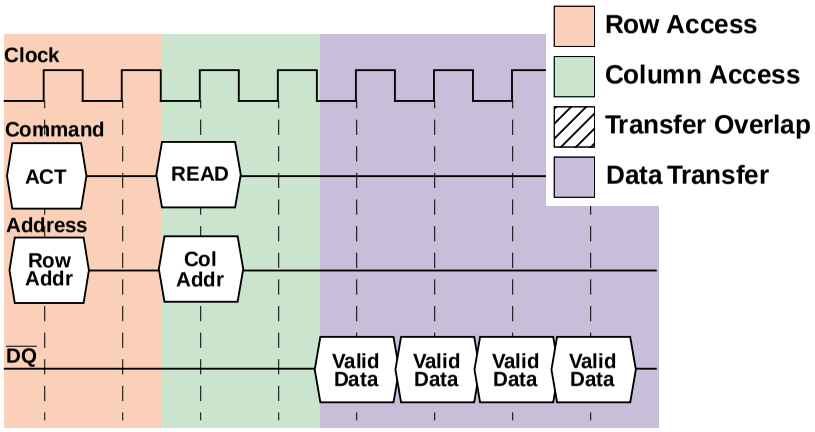
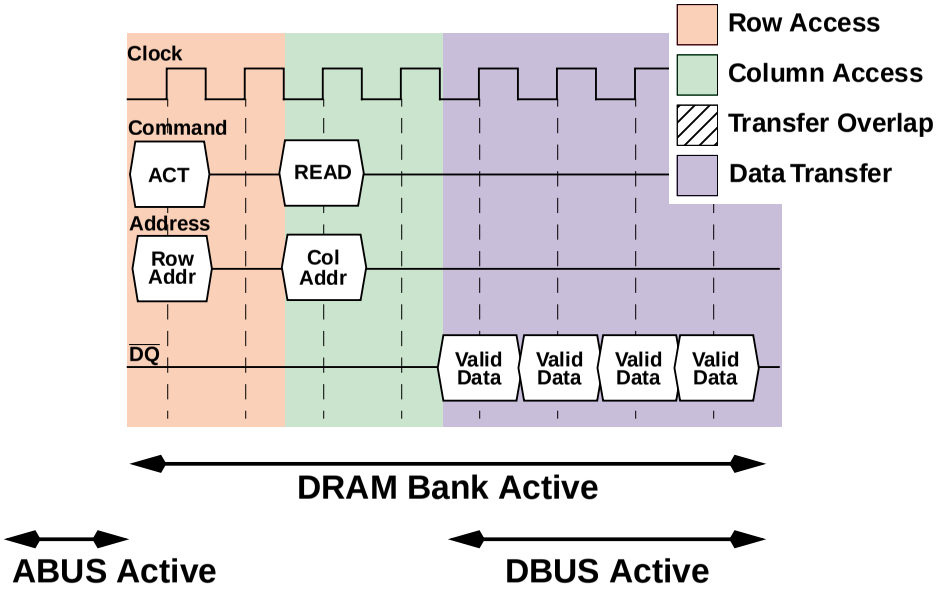
System-Level Model

SDRAM Timing



System-Level Model

Timing diagrams are at the DRAM level … not the system level



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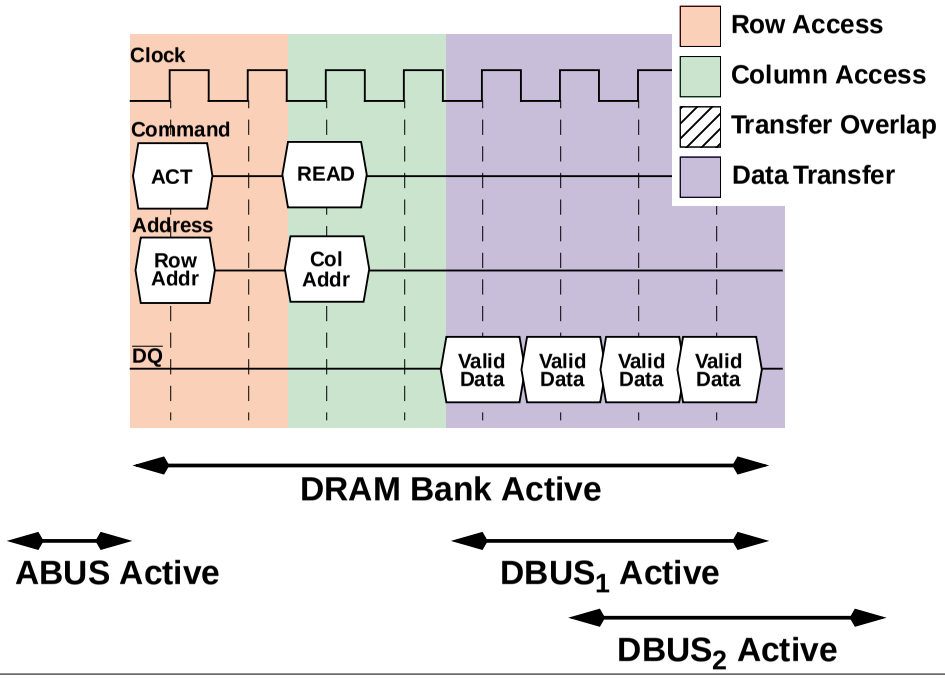
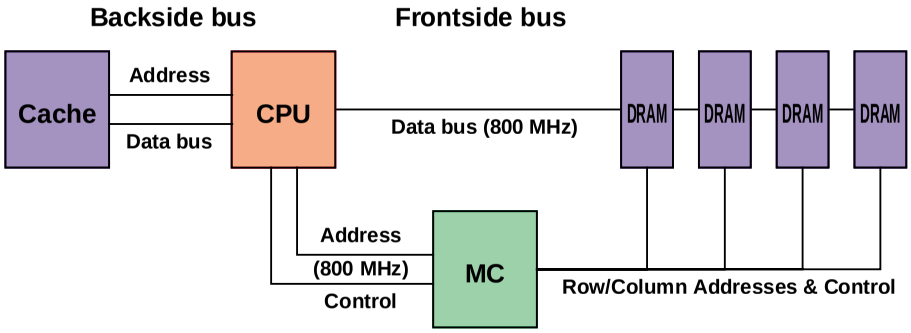
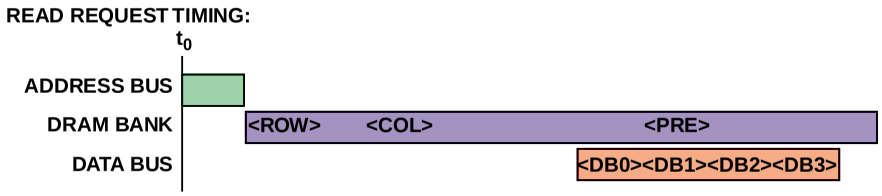
System-Level Model

Timing diagrams are at the DRAM level … not the system level



Request Timing





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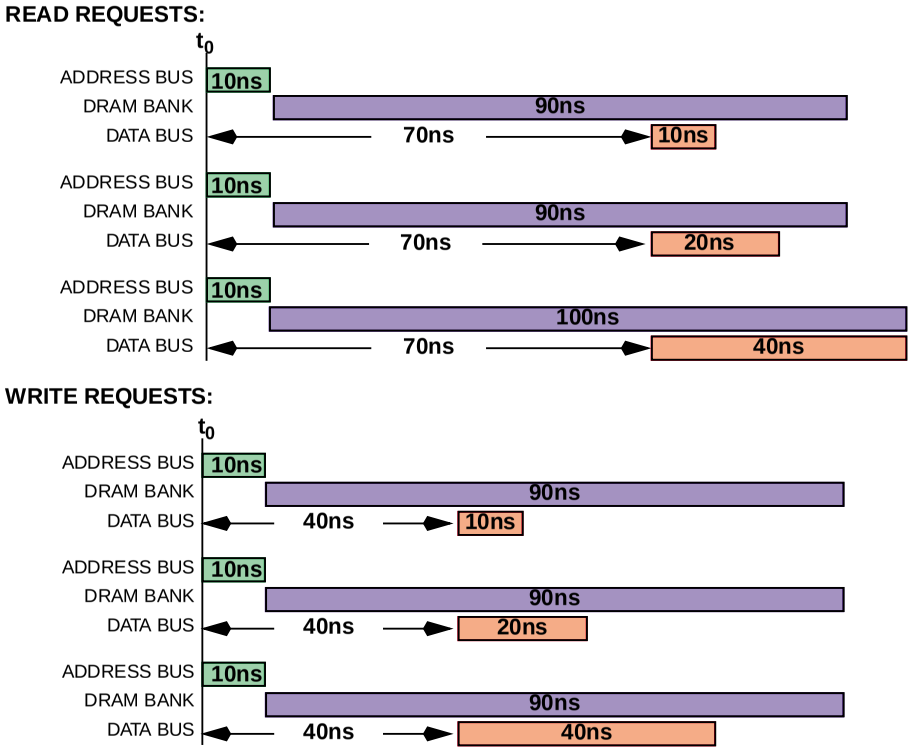
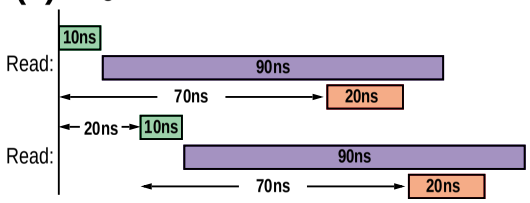
Read/Write Request Shapes



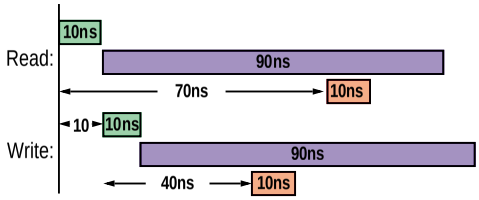
Pipelined/Split Transactions

(a) Legal if R/R to different banks:

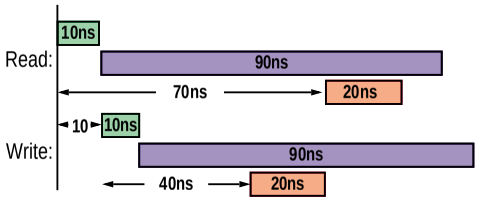


(b) Nestling of writes inside reads is legal if R/W to different banks:

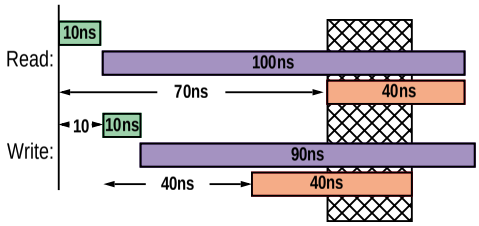
Legal if turnaround <= 10ns:



Legal if no turnaround:



(c) Back-to-back R/W pair that cannot be nestled:



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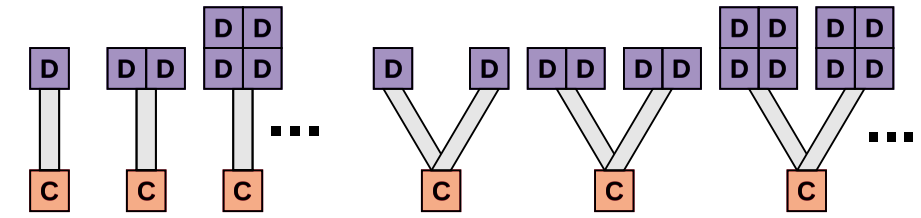
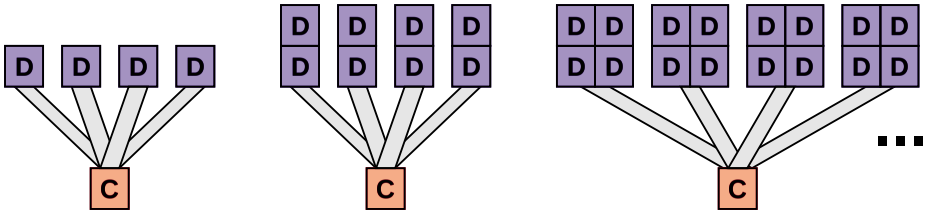
Channels & Banks



One independent channel
Banking degrees of 1, 2, 4, ...

Two independent channels
Banking degrees of 1, 2, 4, ...

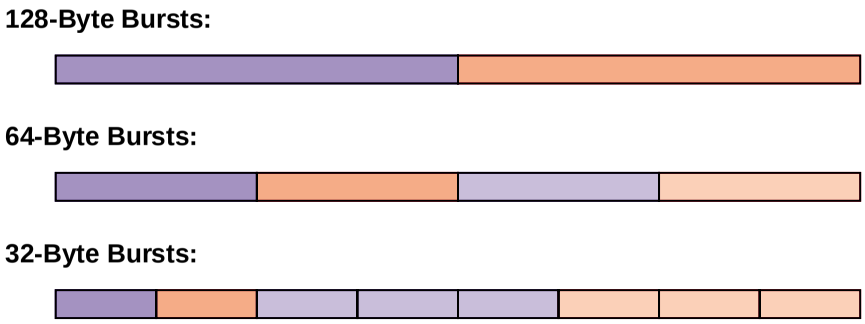


Four independent channels
Banking degrees of 1, 2, 4, ...

1, 2, 4	800 MHz Channels
8, 16, 32, 64	Data Bits per Channel
1, 2, 4, 8	Banks per Channel (Indep.)
32, 64, 128	Bytes per Burst

Burst Scheduling

(Back-to-Back Read Requests)



- Critical-burst-first
- Non-critical bursts are promoted
- Writes have lowest priority
  (tend back up in request queue …)
- Tension between large & small bursts:
  amortization vs. faster time to data

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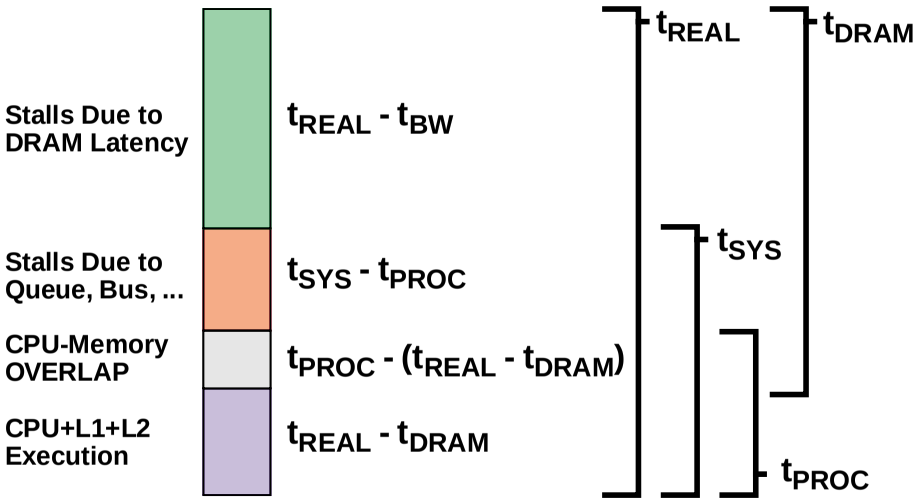
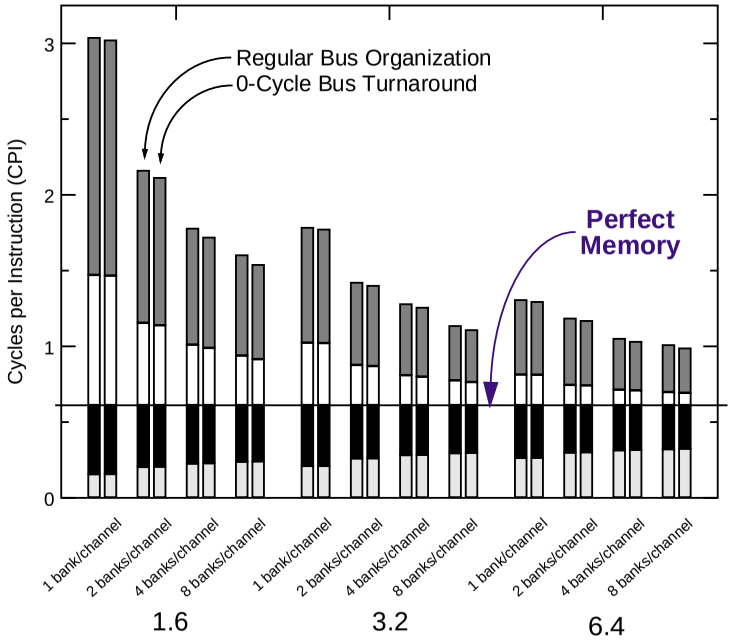
New Bar-Chart Definition



- t_{PROC} — CPU with 1-cycle L2 miss
- t_{REAL} — realistic CPU/DRAM config
- t_{SYS} — CPU with 1-cycle DRAM latency
- t_{DRAM} — time seen by DRAM system

System Overhead



Benchmark = BZIP (SPEC 2000), 32-byte burst, 16-bit bus

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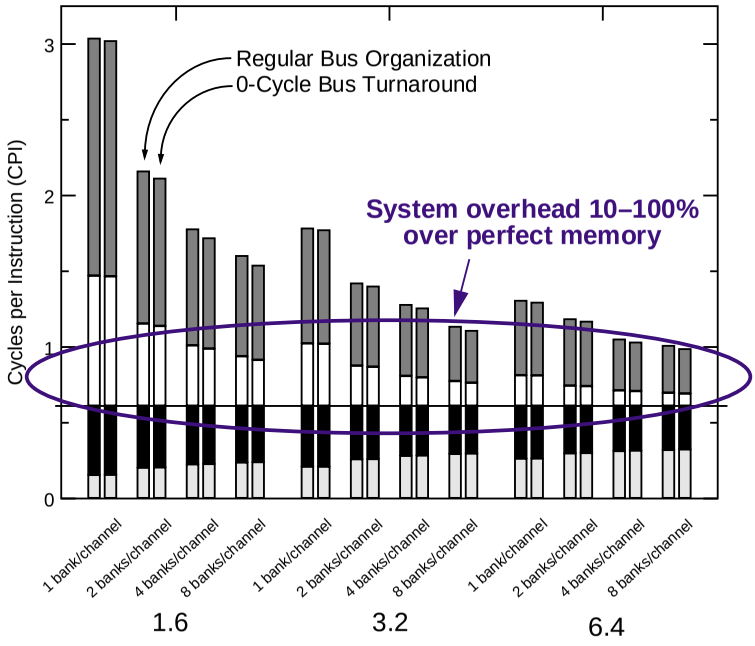
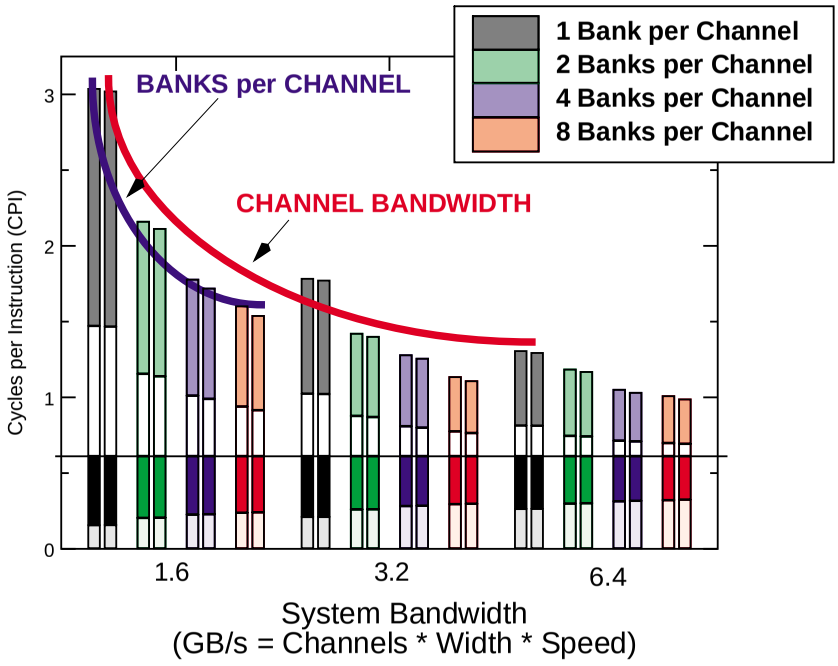
System Overhead



Benchmark = BZIP (SPEC 2000), 32-byte burst, 16-bit bus

Concurrency Effects



Benchmark = BZIP (SPEC 2000), 32-byte burst, 16-bit bus

Banks/channel as significant as channel BW

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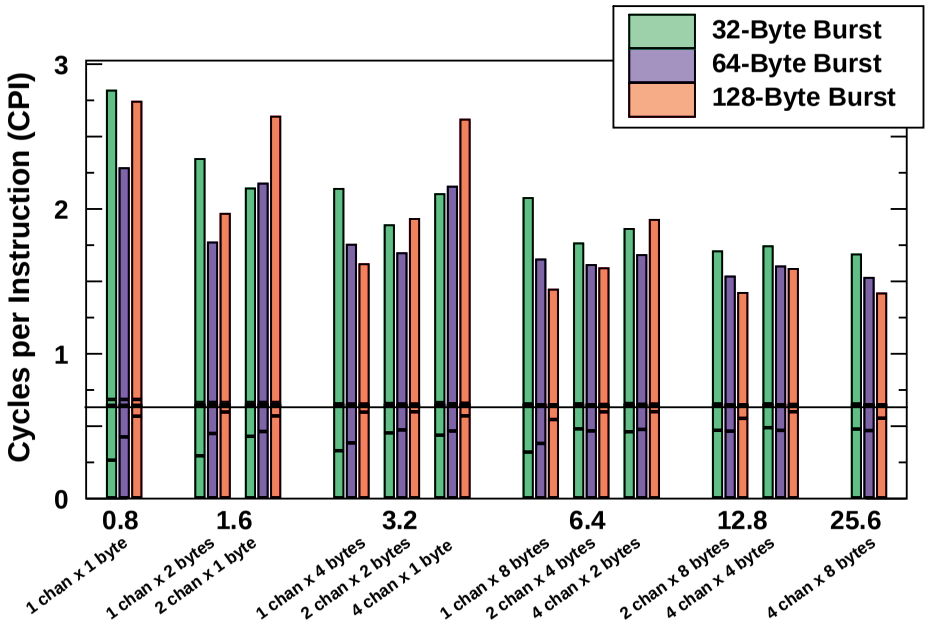
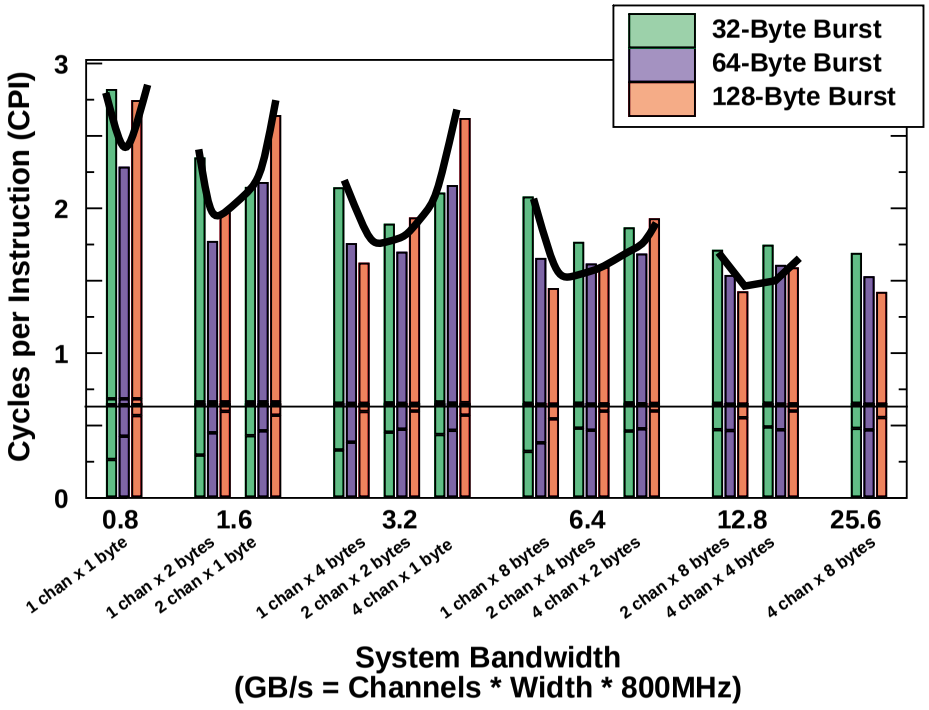
Bandwidth vs. Burst Width



Benchmark = GCC (SPEC 2000), 2 banks/channel

Bandwidth vs. Burst Width



Benchmark = GCC (SPEC 2000), 2 banks/channel

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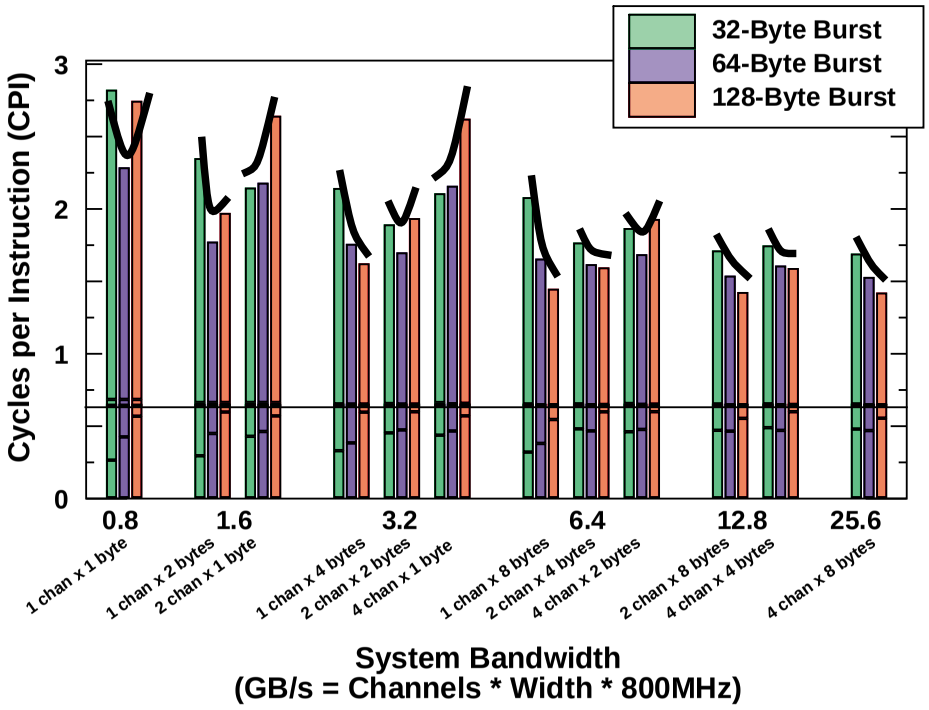
Bandwidth vs. Burst Width



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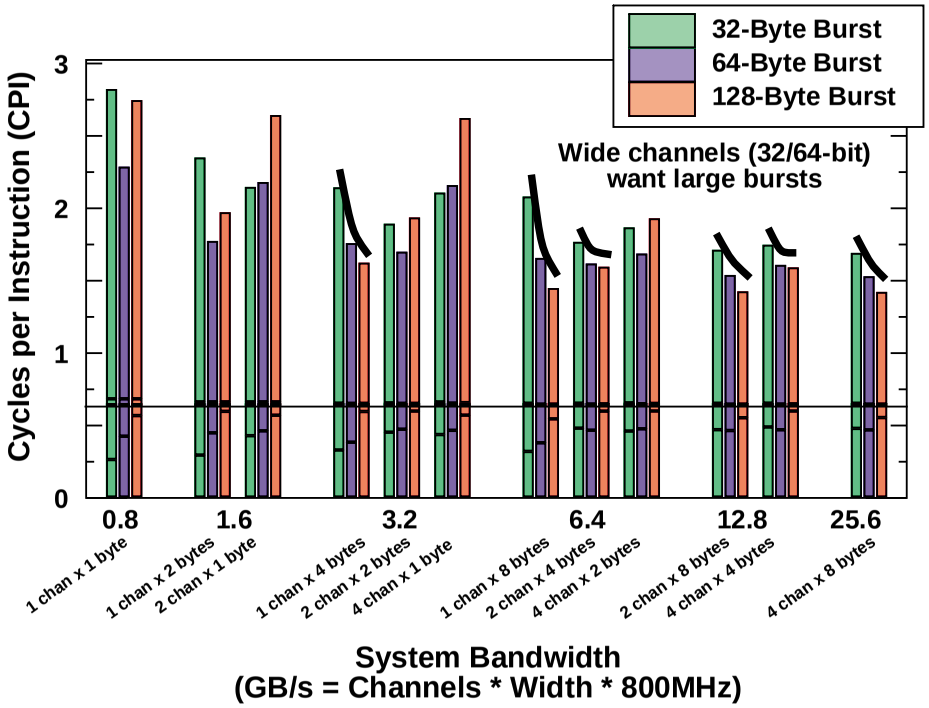
Bandwidth vs. Burst Width



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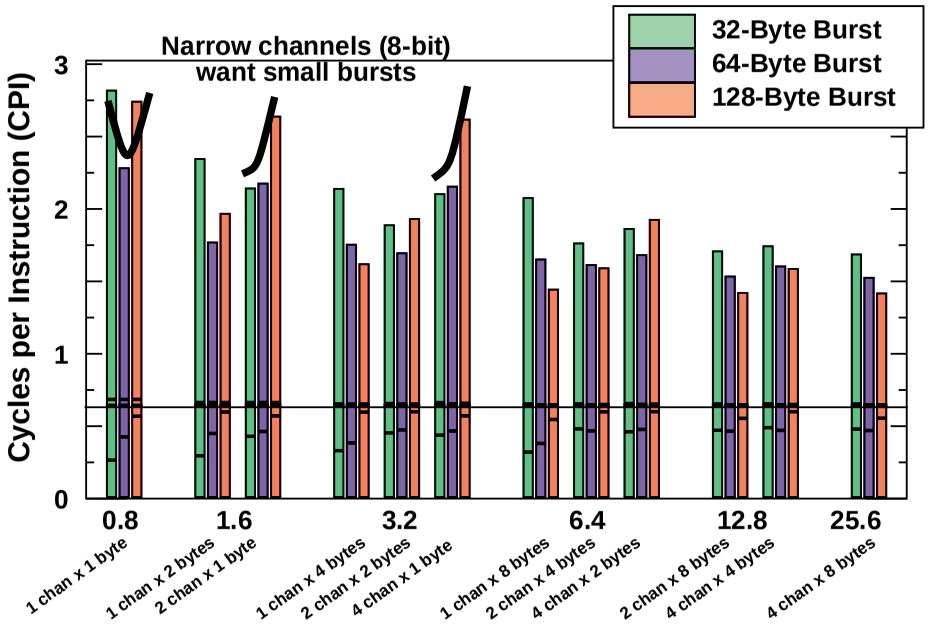
Bandwidth vs. Burst Width



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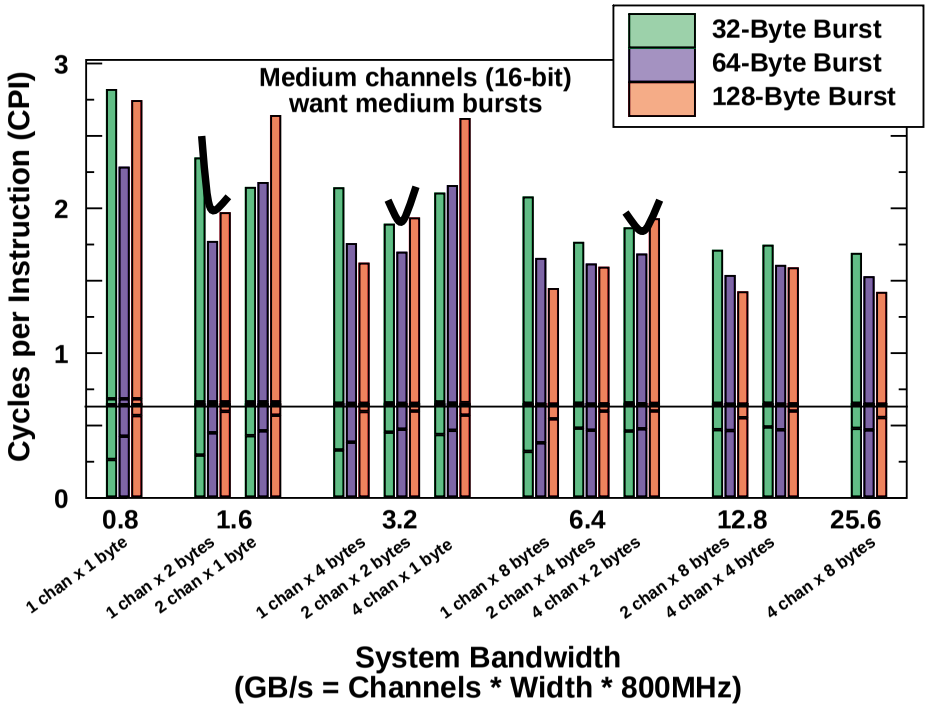
Bandwidth vs. Burst Width



Benchmark = GCC (SPEC 2000), 2 banks/channel

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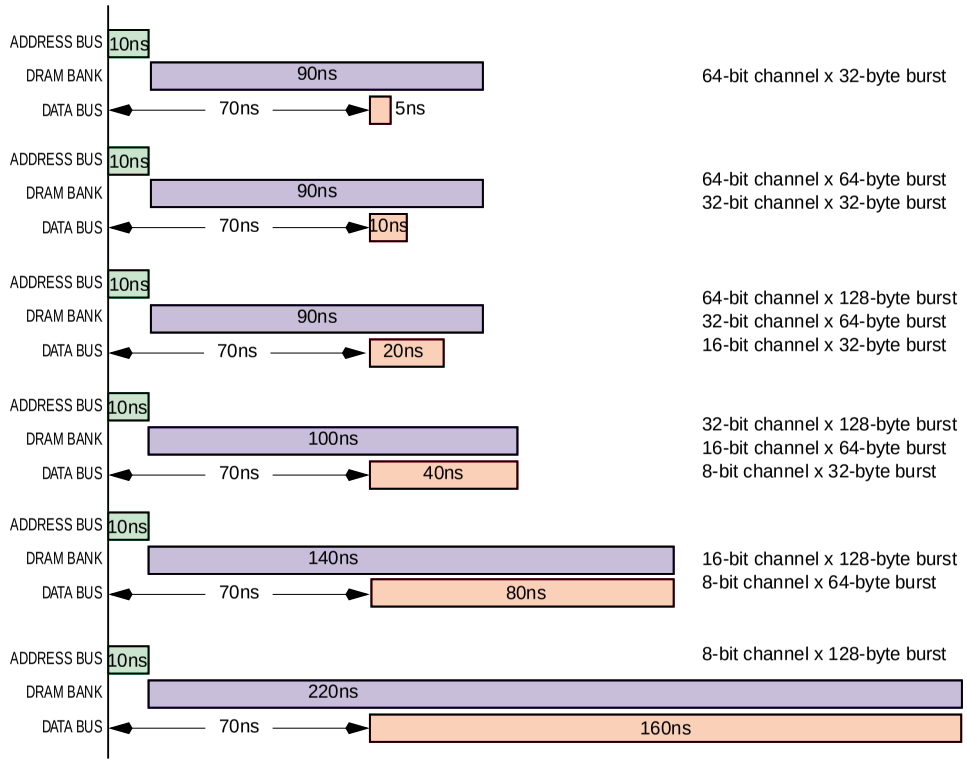
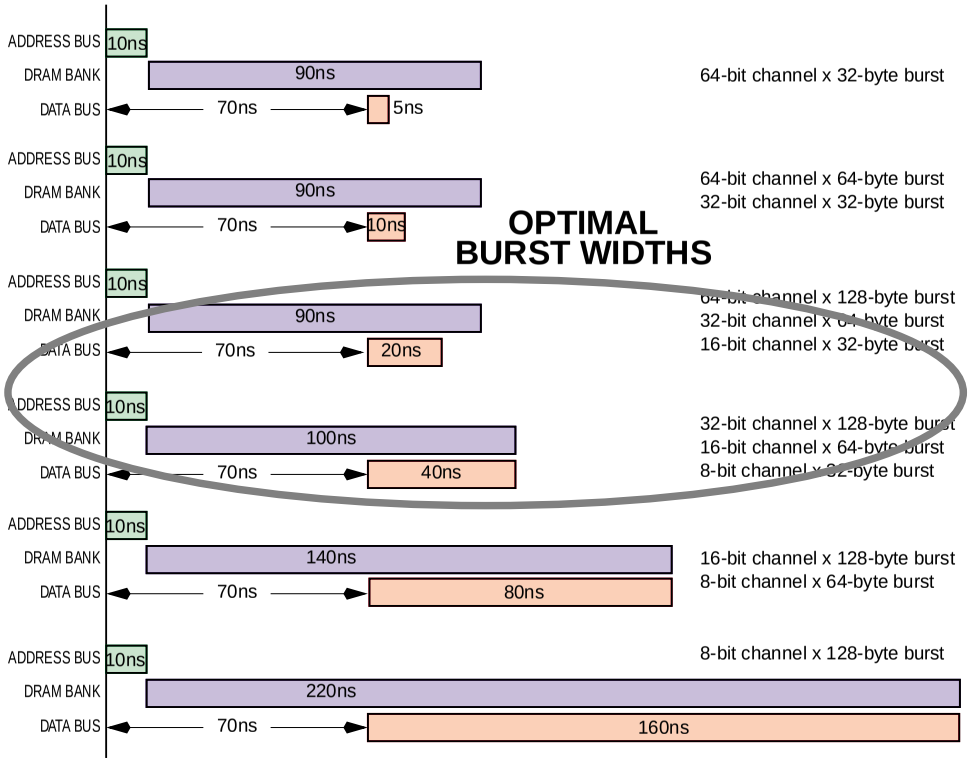
Burst Width Scales with Bus

Range of Burst-Widths Modeled



Burst Width Scales with Bus

Range of Burst-Widths Modeled



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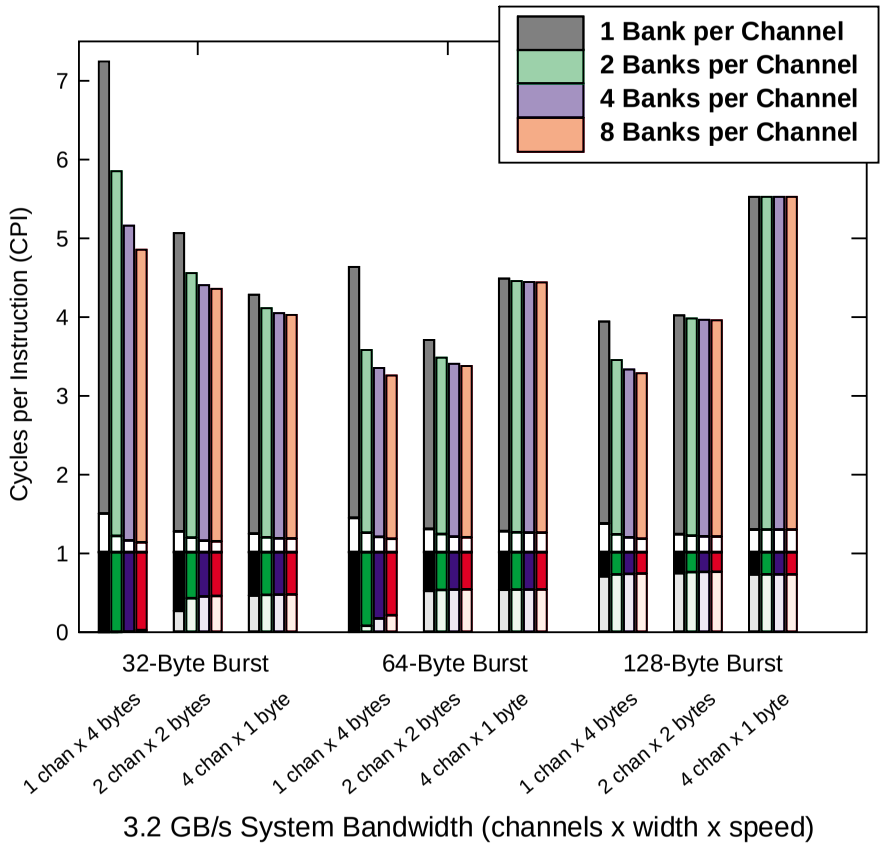
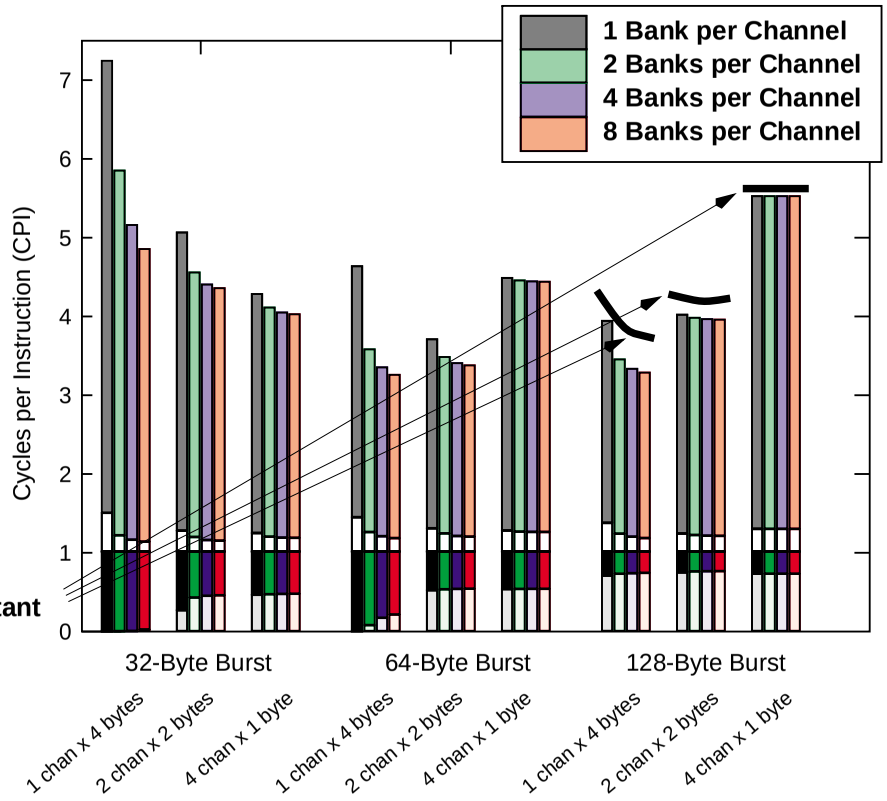
Focus on 3.2 GB/s — MCF



Focus on 3.2 GB/s — MCF



#Banks not particularly important given large burst sizes ...

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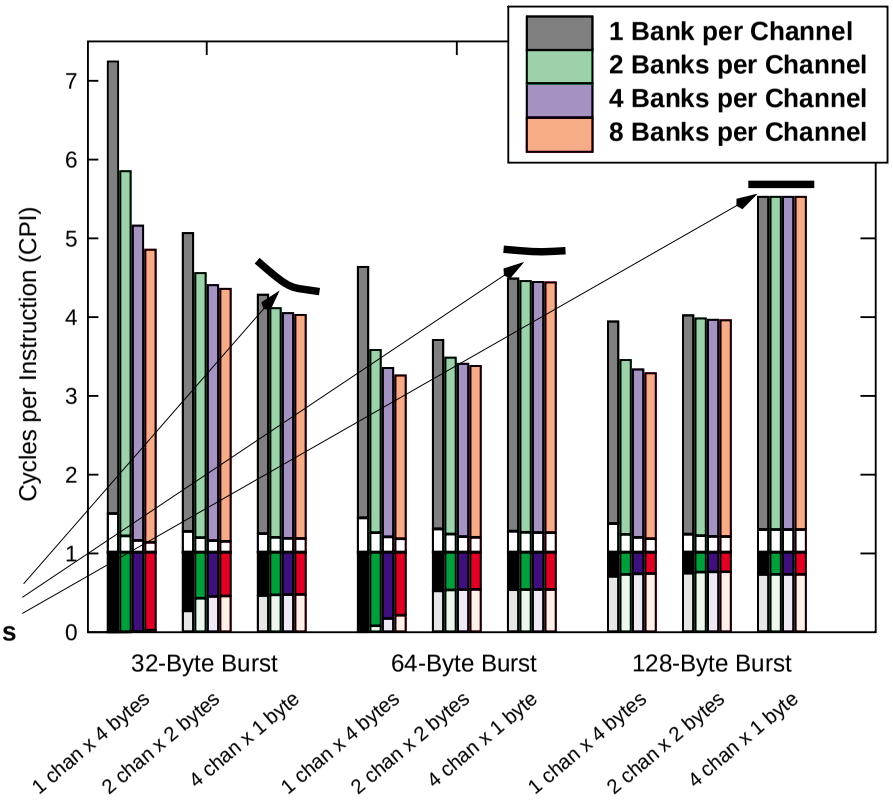
Focus on 3.2 GB/s — MCF



... even less so with multi-channel systems

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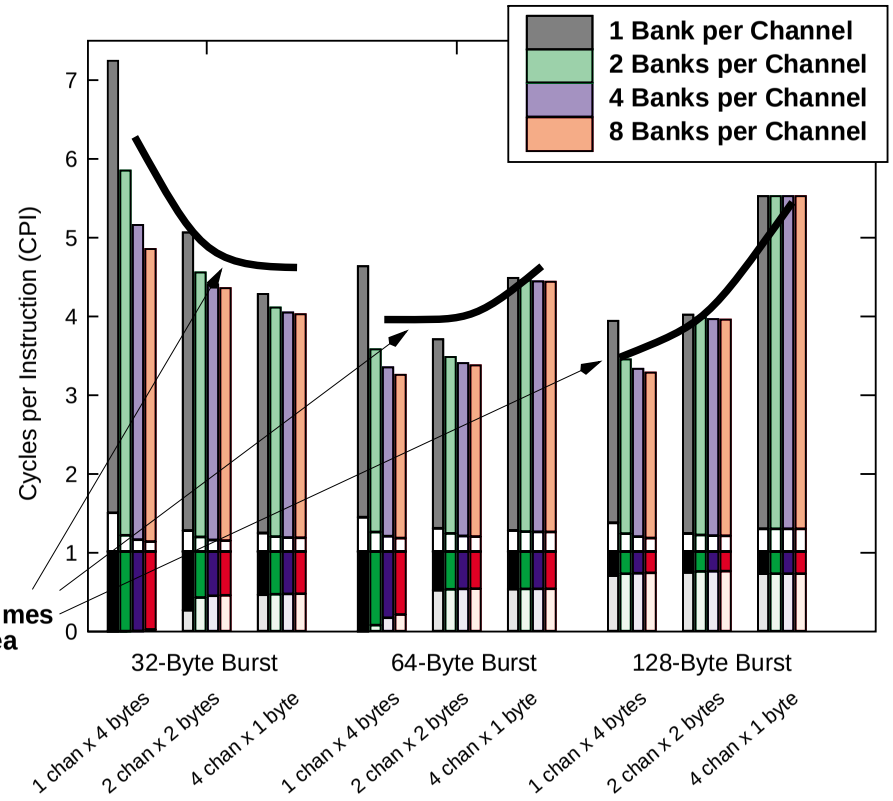
Focus on 3.2 GB/s — MCF



Multi-channel systems sometimes (but not always) a good idea

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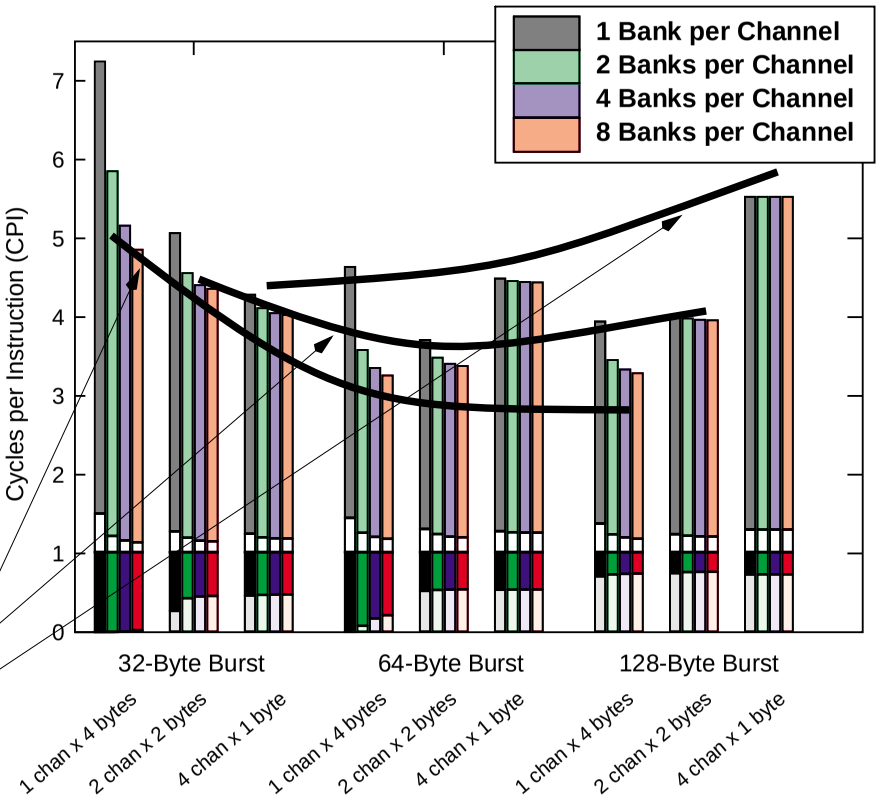
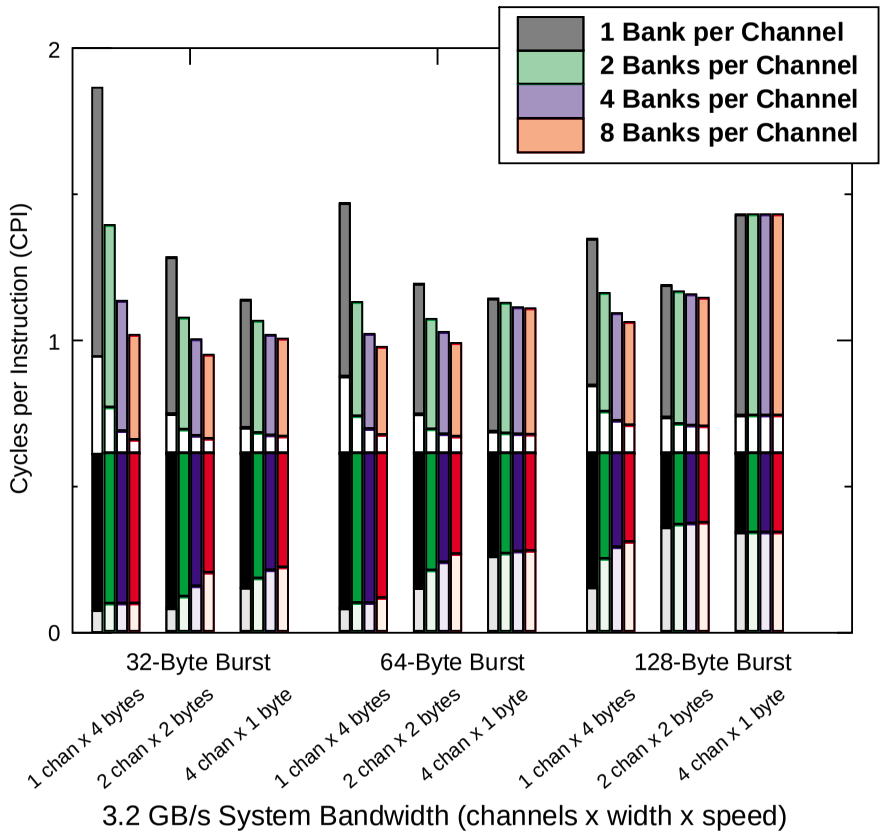
Focus on 3.2 GB/s — MCF



4x 1-byte channels
2x 2-byte channels
1x 4-byte channels

Focus on 3.2 GB/s — BZIP



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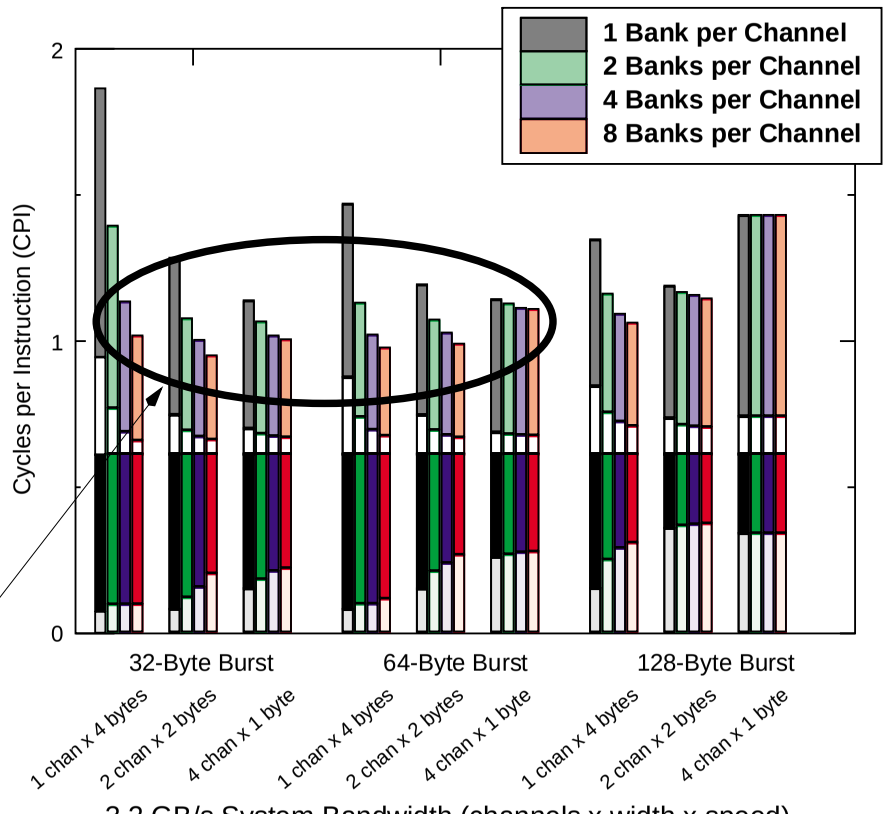
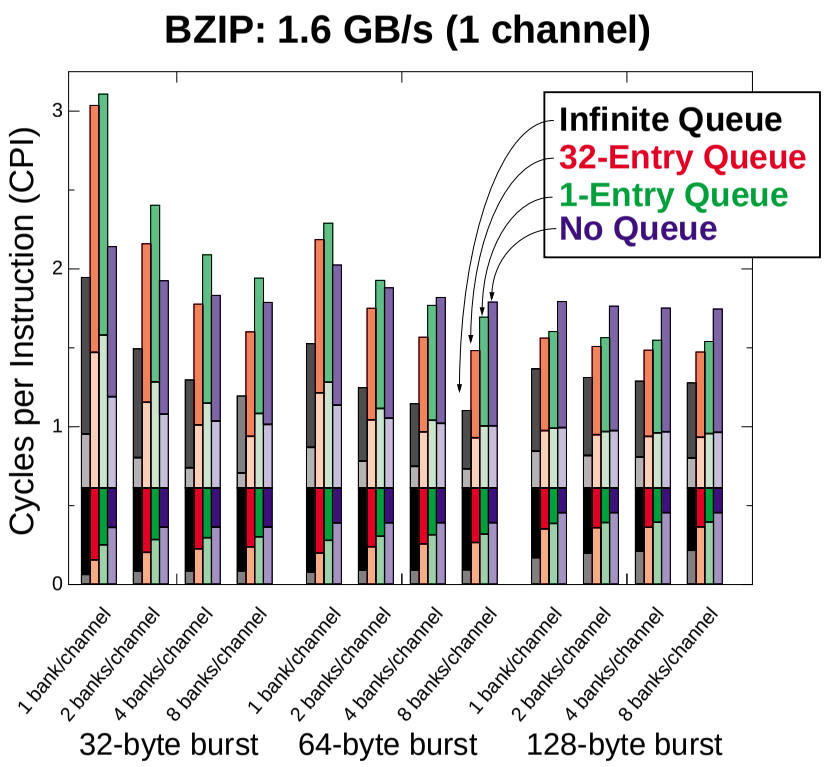
Focus on 3.2 GB/s — BZIP



BEST CONFIGS are at SMALLER BURST SIZES

Queue Size & Reordering



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Conclusions

DESIGN SPACE is NON-LINEAR,
COST of MISJUDGING is HIGH

CAREFUL TUNING YIELDS 30–40% GAIN

MORE CONCURRENCY == BETTER
(but not at expense of LATENCY)

- **Via Channels** → **NOT w/ LARGE BURSTS**
- **Via Banks** → **ALWAYS SAFE**
- **Via Bursts** → **DOESN'T PAY OFF**
- **Via MSHRs** → **NECESSARY**

BURSTS AMORTIZE COST OF PRECHARGE

- **Typical Systems: 32 bytes (even DDR2)**
  → THIS IS NOT ENOUGH

Outline

- **Basics**
- **DRAM Evolution: *Structural Path***
- **Advanced Basics**
- **DRAM Evolution: *Interface Path***
- **Future Interface Trends & Research Areas**
- **Performance Modeling:**
  Architectures, Systems, Embedded

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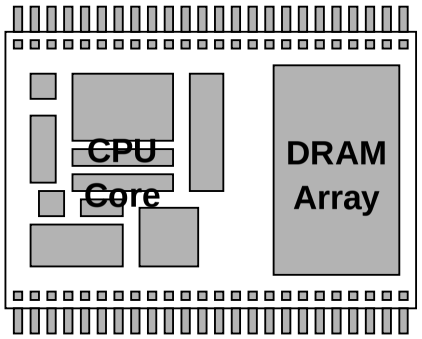
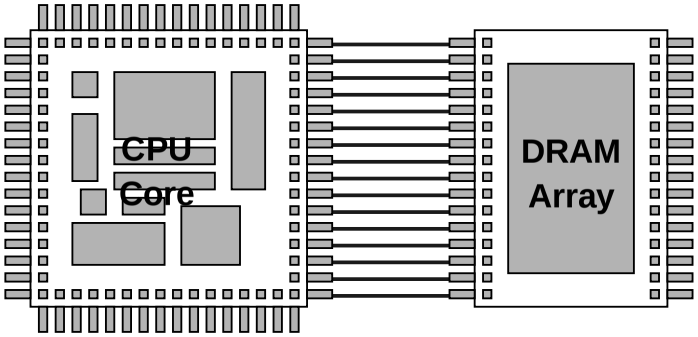
Embedded DRAM Primer



Embedded



Not Embedded

Whither Embedded DRAM?

***Microprocessor Report*, August 1996: "[Five] Architects Look to Processors of Future"**

- **Two predict imminent merger of CPU and DRAM**
- **Another states we cannot keep cramming more data over the pins at faster rates (implication: embedded DRAM)**
- **A fourth wants gigantic on-chip L3 cache (perhaps DRAM L3 implementation?)**

SO WHAT HAPPENED?

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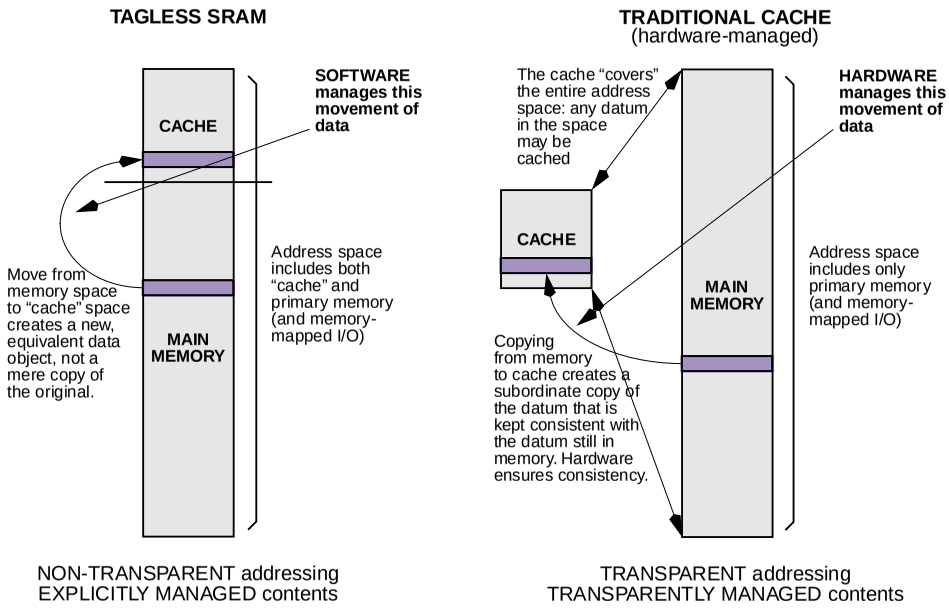
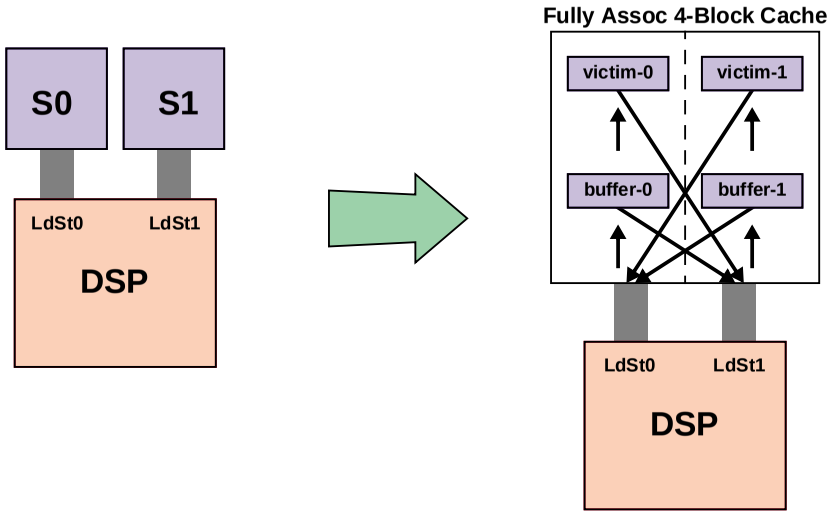
Embedded DRAM for DSPs

MOTIVATION



DSP Compilers => Transparent Cache Model

DSP Buffer Organization Used for Study



Bandwidth vs. Die-Area Trade-Off for DSP Performance

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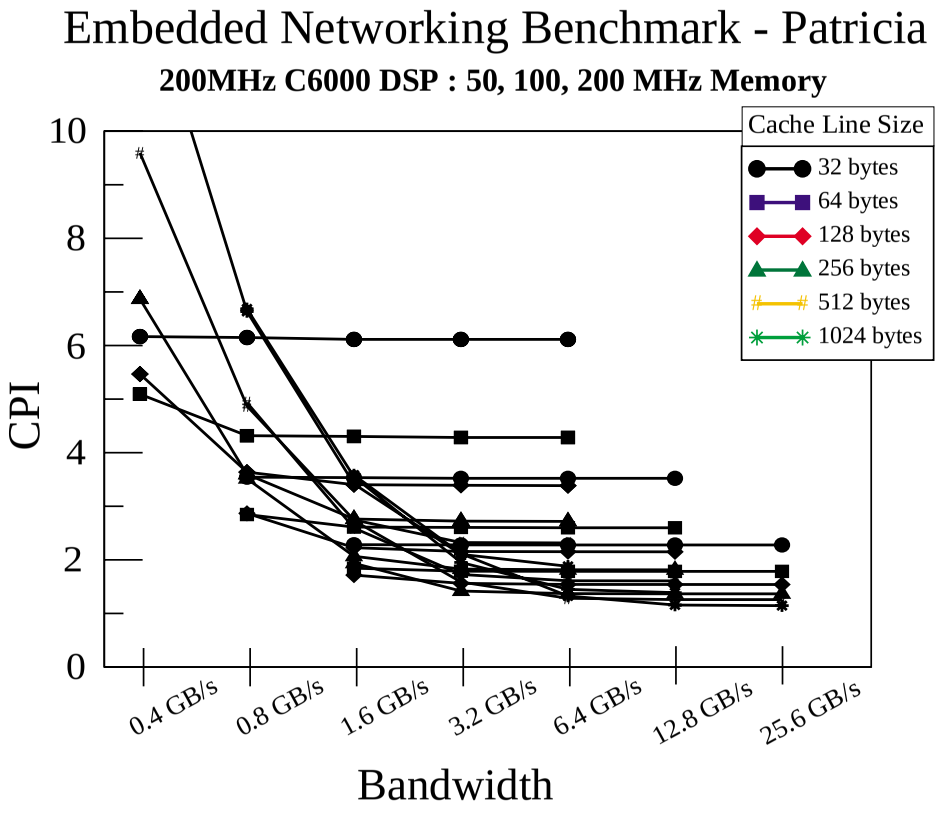
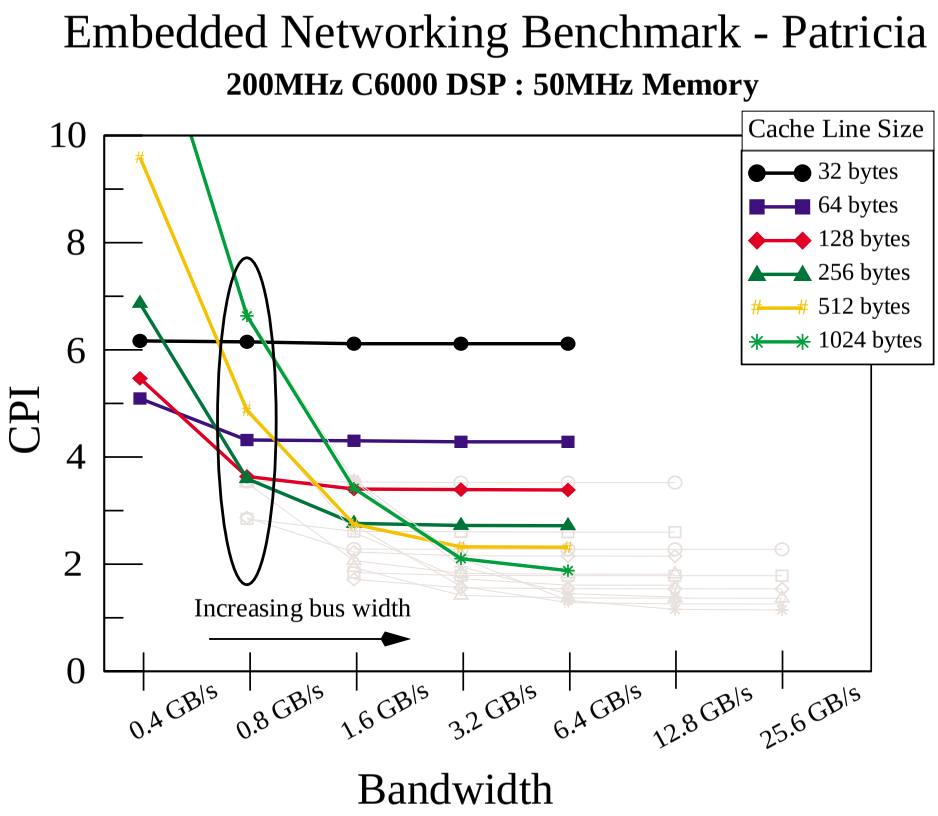
E-DRAM Performance



E-DRAM Performance



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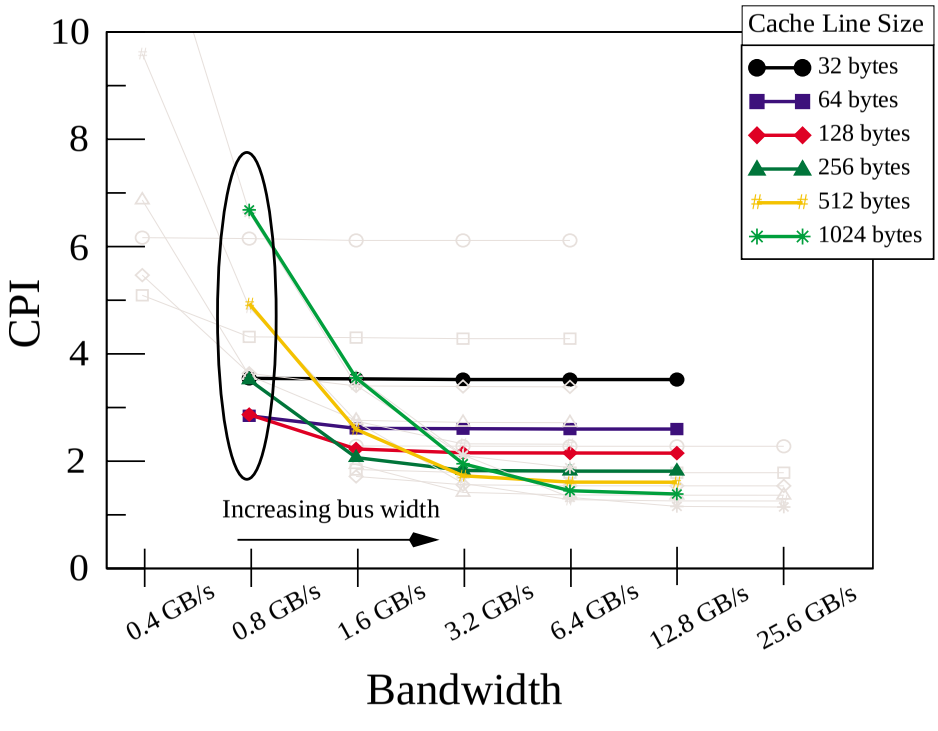
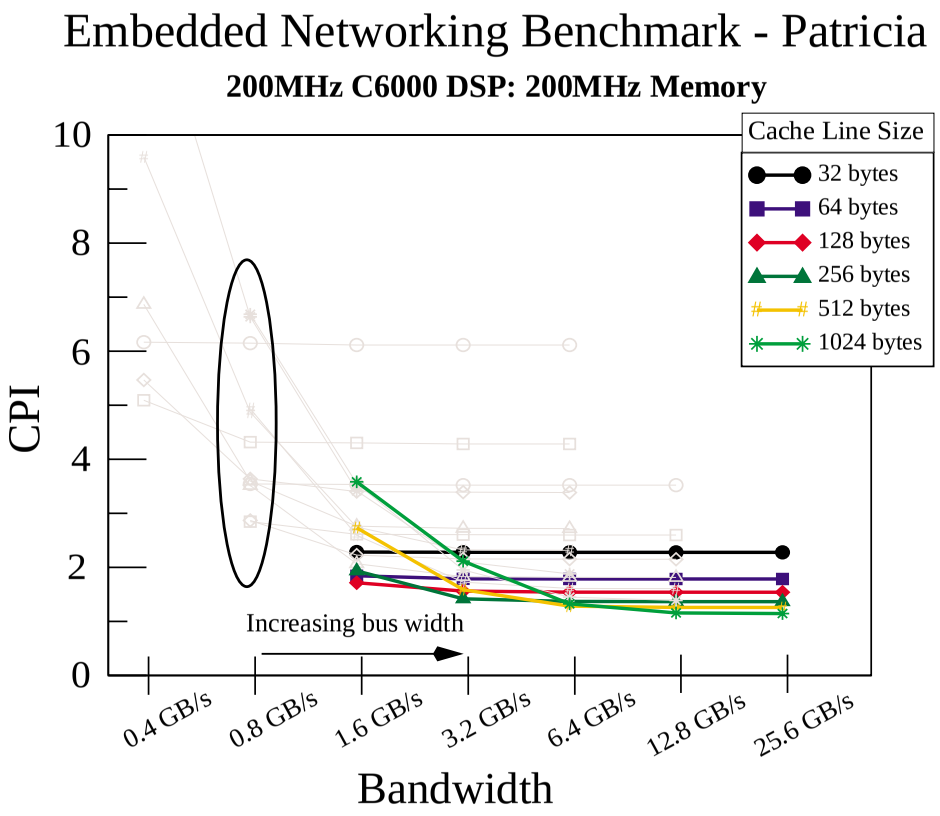
E-DRAM Performance



E-DRAM Performance



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Performance-Data Sources

"A Performance Study of Contemporary DRAM Architectures," *Proc. ISCA '99.* V. Cuppu, B. Jacob, B. Davis, and T. Mudge.

"Organizational Design Trade-Offs at the DRAM, Memory Bus, and Memory Controller Level: Initial Results," University of Maryland Technical Report UMD-SCA-TR-1999-2. V. Cuppu and B. Jacob.

"DDR2 and Low Latency Variants," *Memory Wall Workshop 2000*, in conjunction w/ ISCA '00. B. Davis, T. Mudge, V. Cuppu, and B. Jacob.

"Concurrency, Latency, or System Overhead: Which Has the Largest Impact on DRAM-System Performance?" *Proc. ISCA '01*. V. Cuppu and B. Jacob.

"Transparent Data-Memory Organizations for Digital Signal Processors," *Proc. CASES '01*. S. Srinivasan, V. Cuppu, and B. Jacob.

"High Performance DRAMs in Workstation Environments," *IEEE Transactions on Computers*, November 2001. V. Cuppu, B. Jacob, B. Davis, and T. Mudge.

Recent experiments by Sadagopan Srinivasan, Ph.D. student at University of Maryland.

Acknowledgments

The preceding work was supported in part by the following sources:

- **NSF CAREER Award CCR-9983618**
- **NSF grant EIA-9806645**
- **NSF grant EIA-0000439**
- **DOD award AFOSR-F496200110374**
- **… and by Compaq and IBM.**

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