cadence

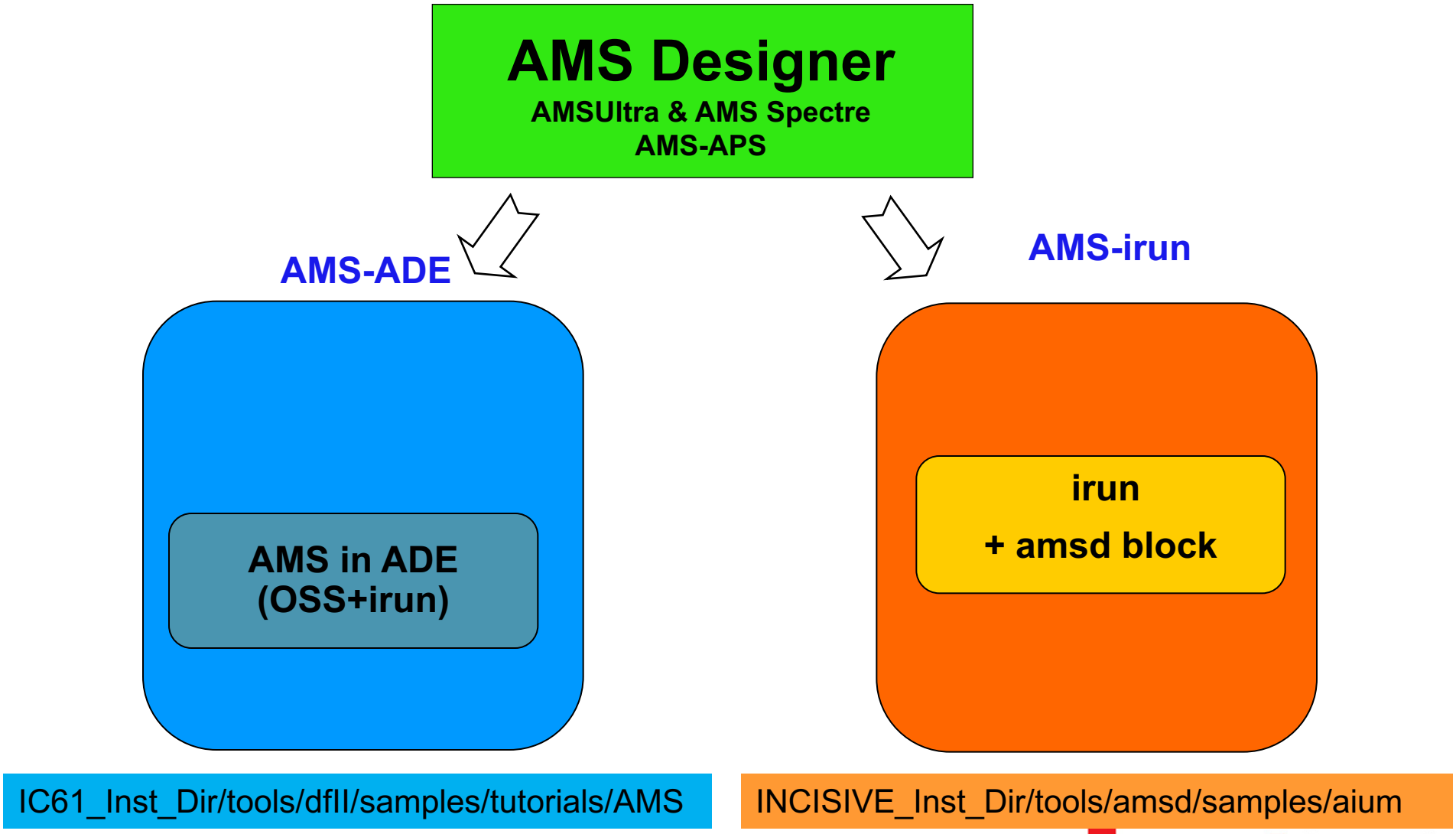
CONFIDENTIAL

INVENTIVE

Co-Sim

March, 2017

Use Mode


AMS Designer
AMSUltra & AMS Spectre
AMS-APS
AMS-ADE
AMS-irun
AMS in ADE
(OSS+irun)
irun
+ amsd block
IC61_Inst_Dir/tools/dfII/samples/tutorials/AMS
INCISIVE_Inst_Dir/tools/amsd/samples/aium

AMS-ADE

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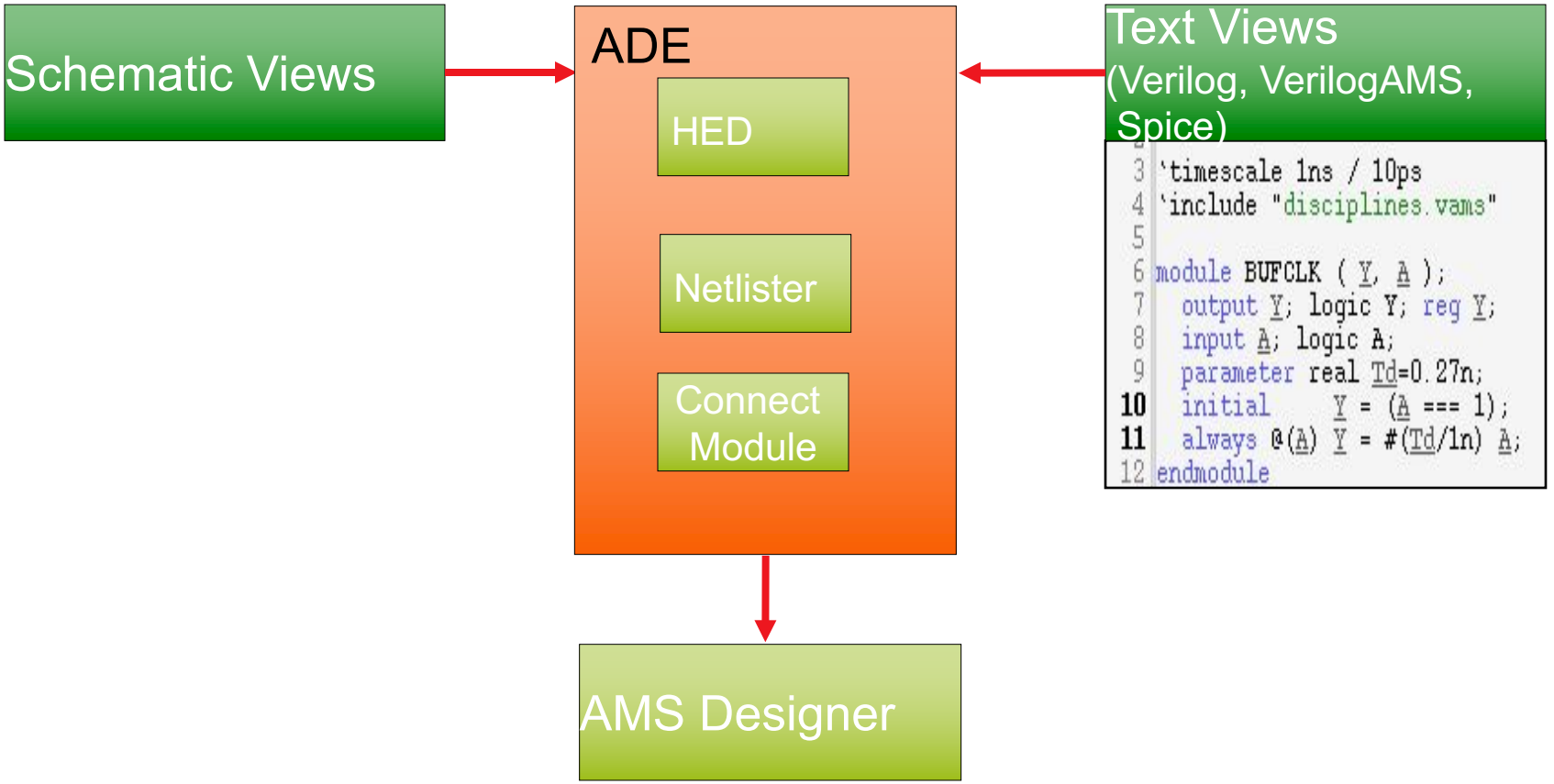
AMS-ADE Flow



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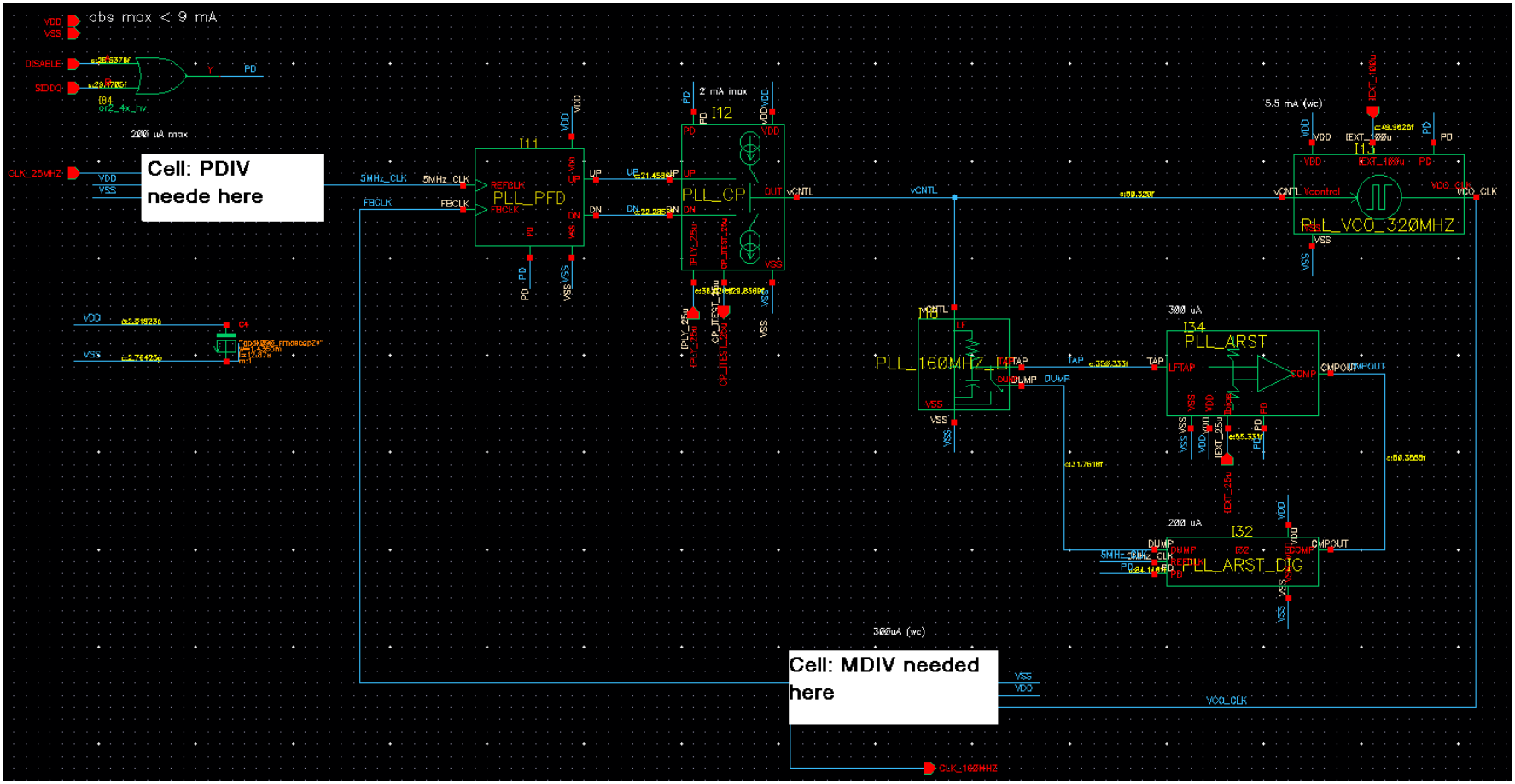
Example:PLL_160MHz



PLL_160MHZ_PDIV & PLL_160MHZ_MDIV are verilog description.

VerilogIn/VHDL In

- From the CIW, File->Import->Verilog… (or VHDL)

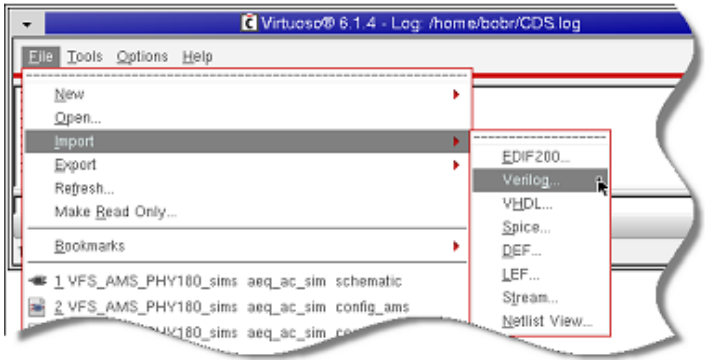
```
module PLL_160MHZ_MDIV (CLK160, CLKFB, CLKVCO, VDD, VSS);
    output CLK160;
    output CLKFB;
    input CLKVCO;
    input VDD;
    input VSS;

    integer i;
    reg CLKFB, CLK160;

    initial
        begin
                CLKFB=0;
                CLK160=0;
                i=0;
        end

    always @( posedge CLKVCO)
        begin
                CLK160 = ~ CLK160;
           if (i==0)
                CLKFB = 1;
           else
                CLKFB = 0;
           i=i+1;
           if (i==64)  i=0;
        end

endmodule
```




```
module PLL_160MHZ_PDIV (DIV, CLK, VDD, VSS);
    output DIV;
    input CLK;
    input VDD;
    input VSS;

    reg DIV;
    integer i;

    initial
        begin
           DIV=0;
           i=0;
        end

    always @( posedge CLK)
        begin
           if (i==0)
                DIV = 1;
           else
                DIV = 0;

           i=i+1;

           if (i==5)  i=0;
        end
endmodule
```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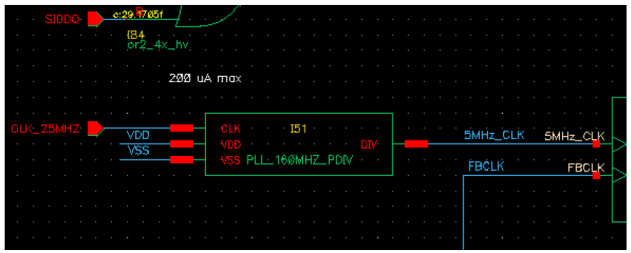
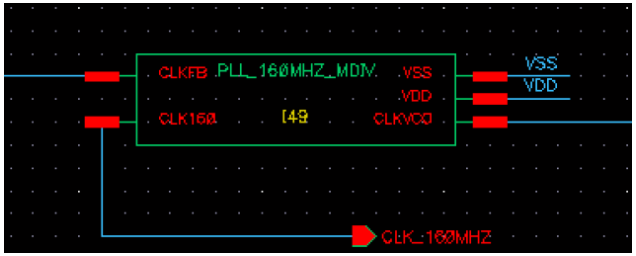
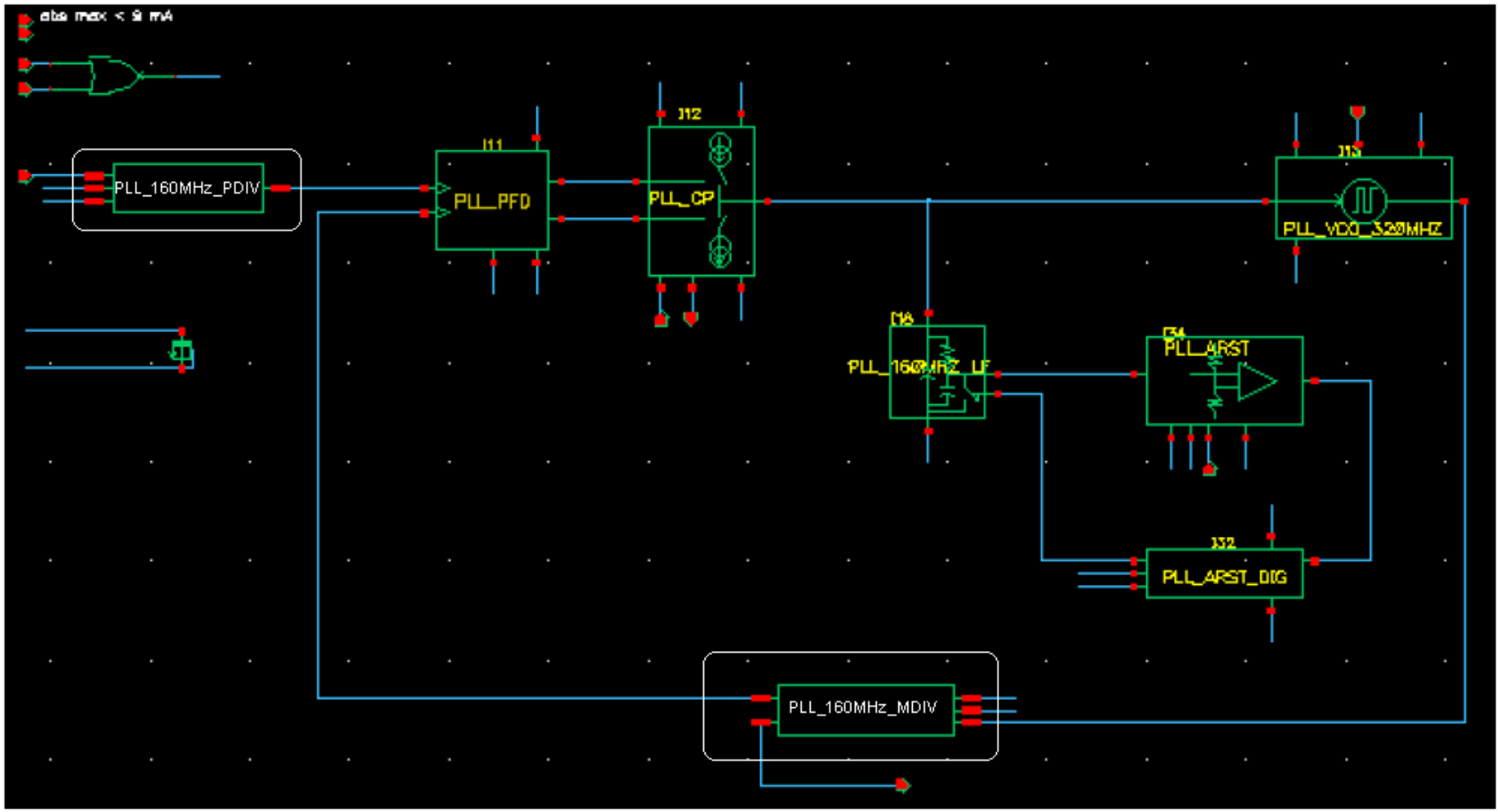
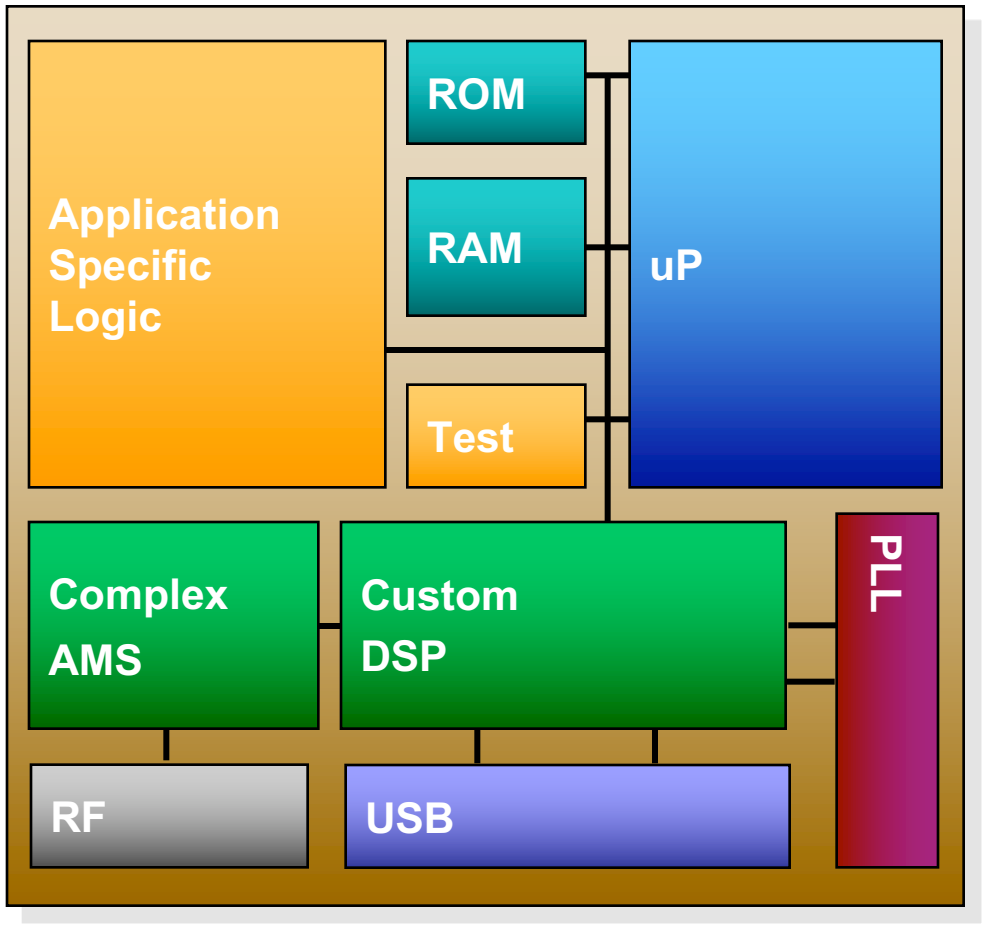
Complete mix-signal design in schematic

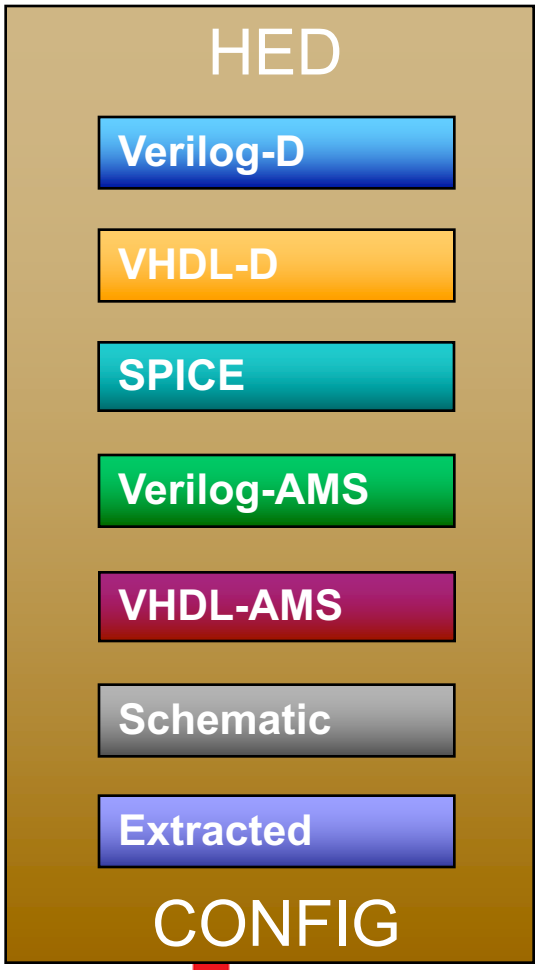






Configed Schematic





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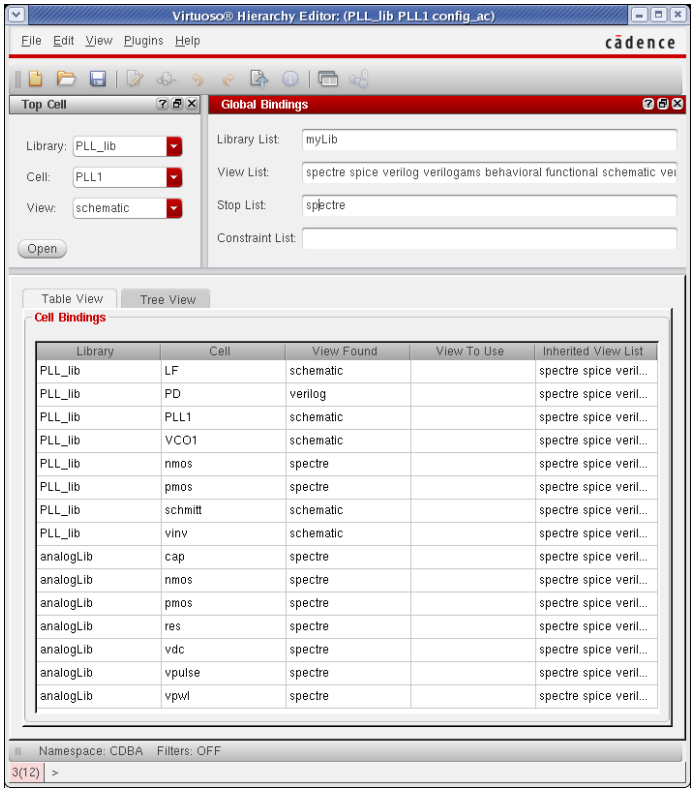
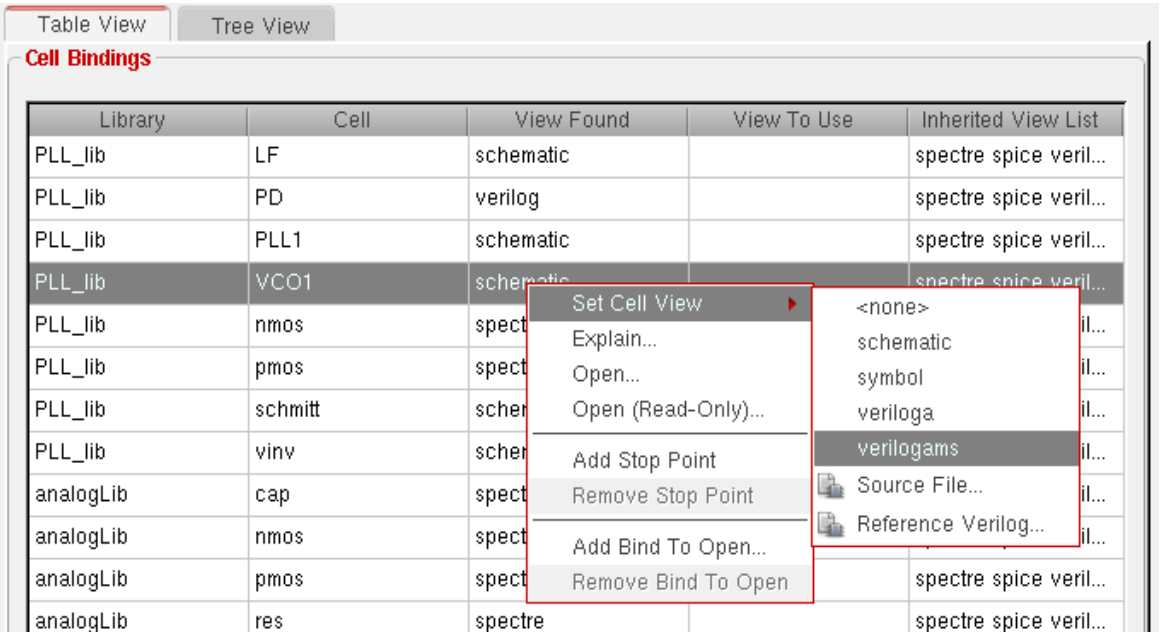
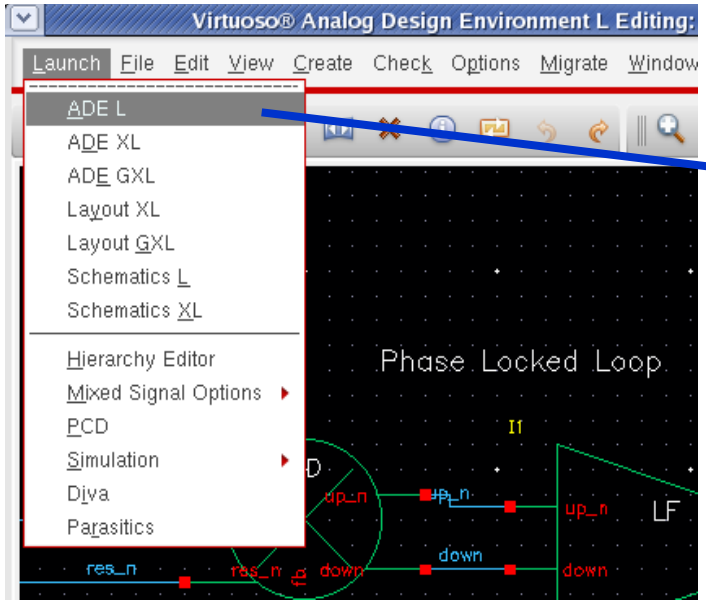
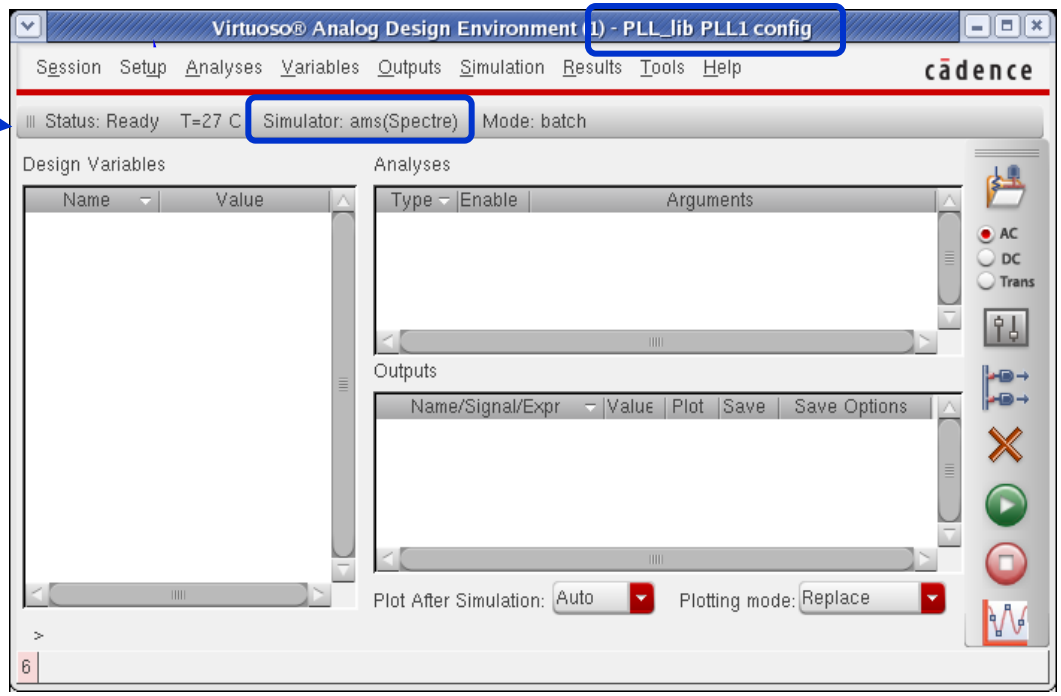
Hierarchy Editor



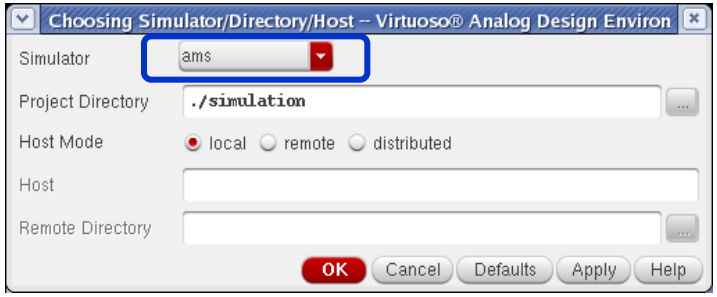


AMS in ADE

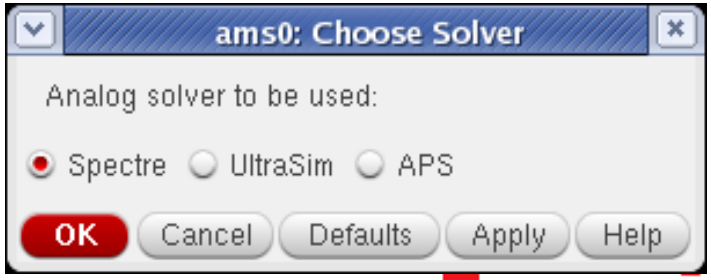




ADE->Simulator/Directory/Host …



ADE->Simulation->Solver



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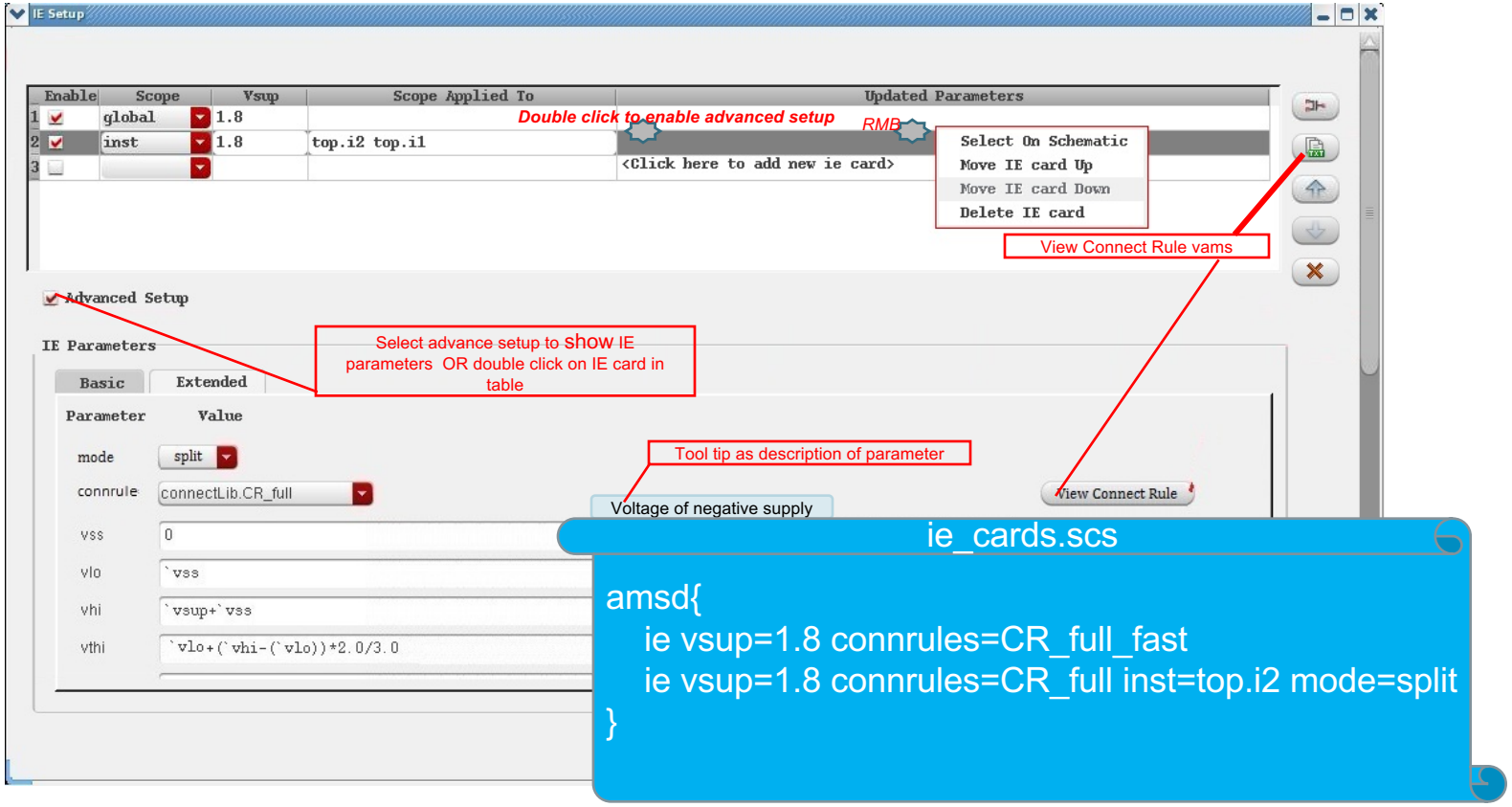
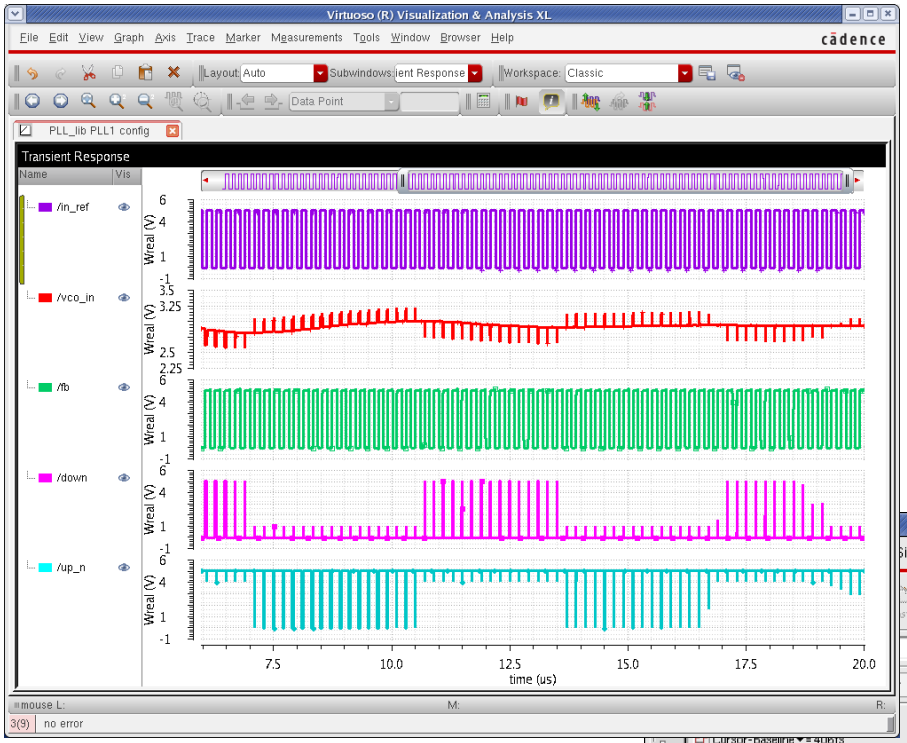
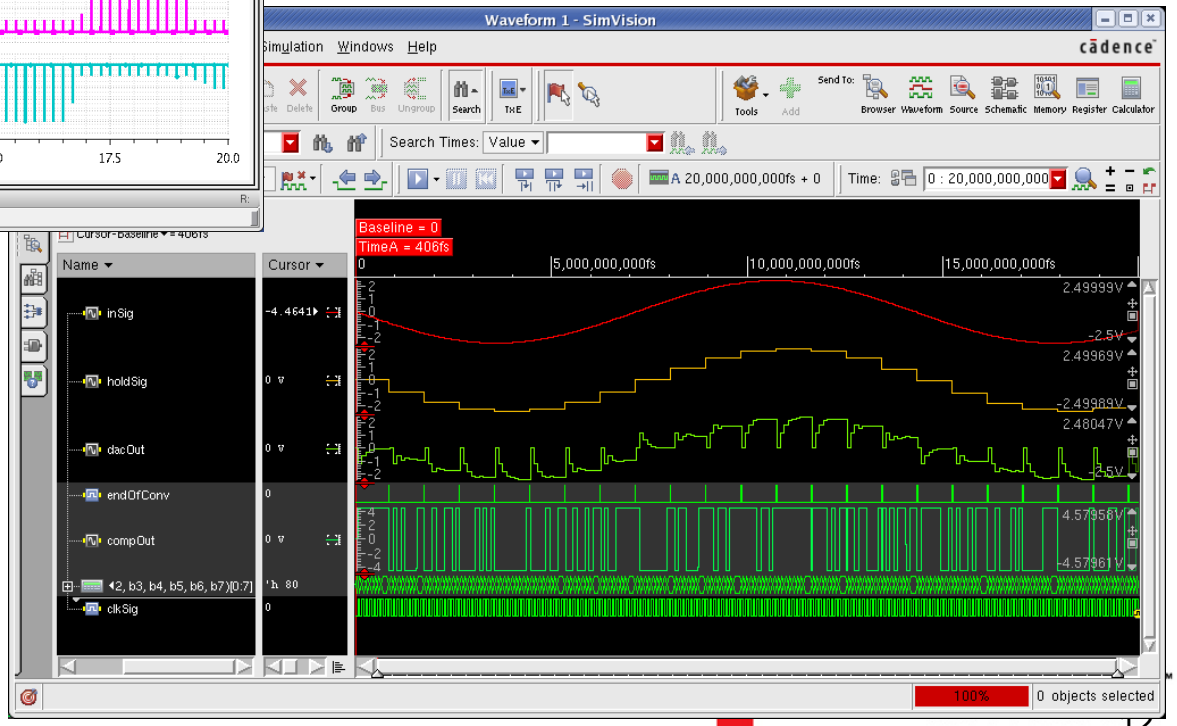
Easily Multi Voltage Setup

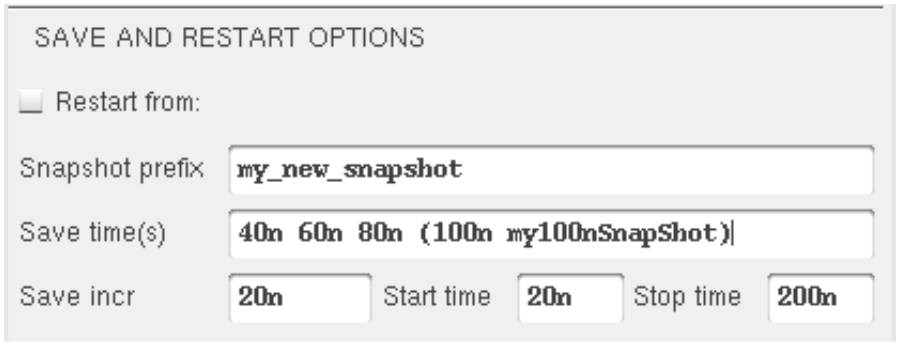


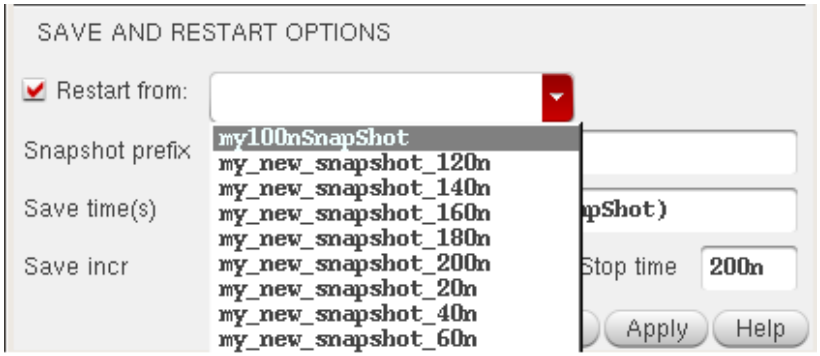
Waveform Display





Save and Restart





AMS-IRUN

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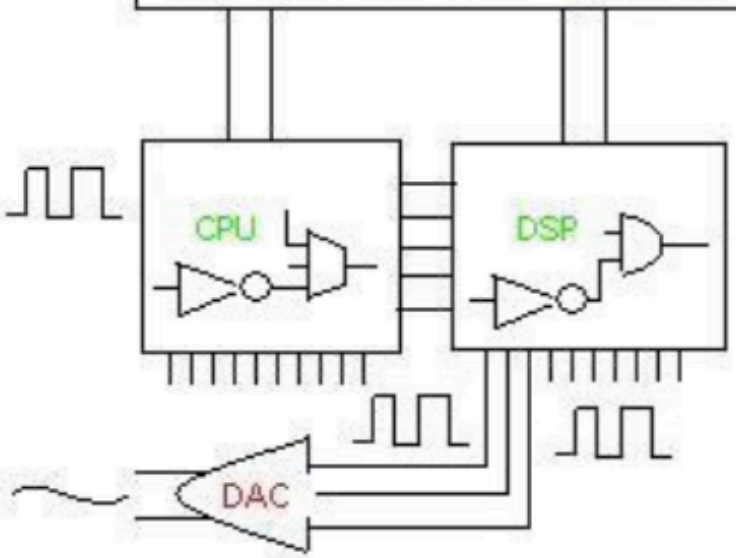
AMS-irun flow

Verilog(ams) on Top

Test Vector Generation
Signal Initialization
Function/Task
Monitor/Display
Verification/Comparision

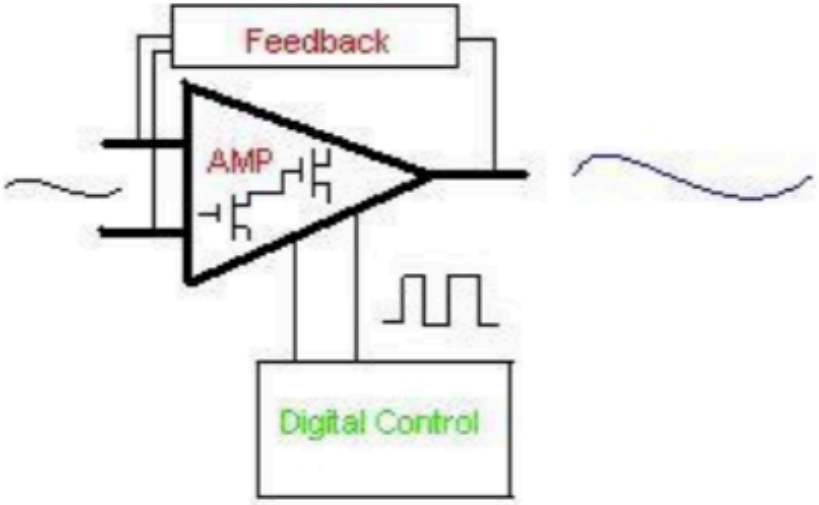
```
module top;
...
initial
  in1=1;..
always...
```



SPICE on Top

SPICE netlist
Power/ground Sources
External Components
Dummy Transistors

```
Vin in 0 5V
Gnd Agnd 0 0
Cout out 0 0.2p
Xamp inp inn....
.....
```



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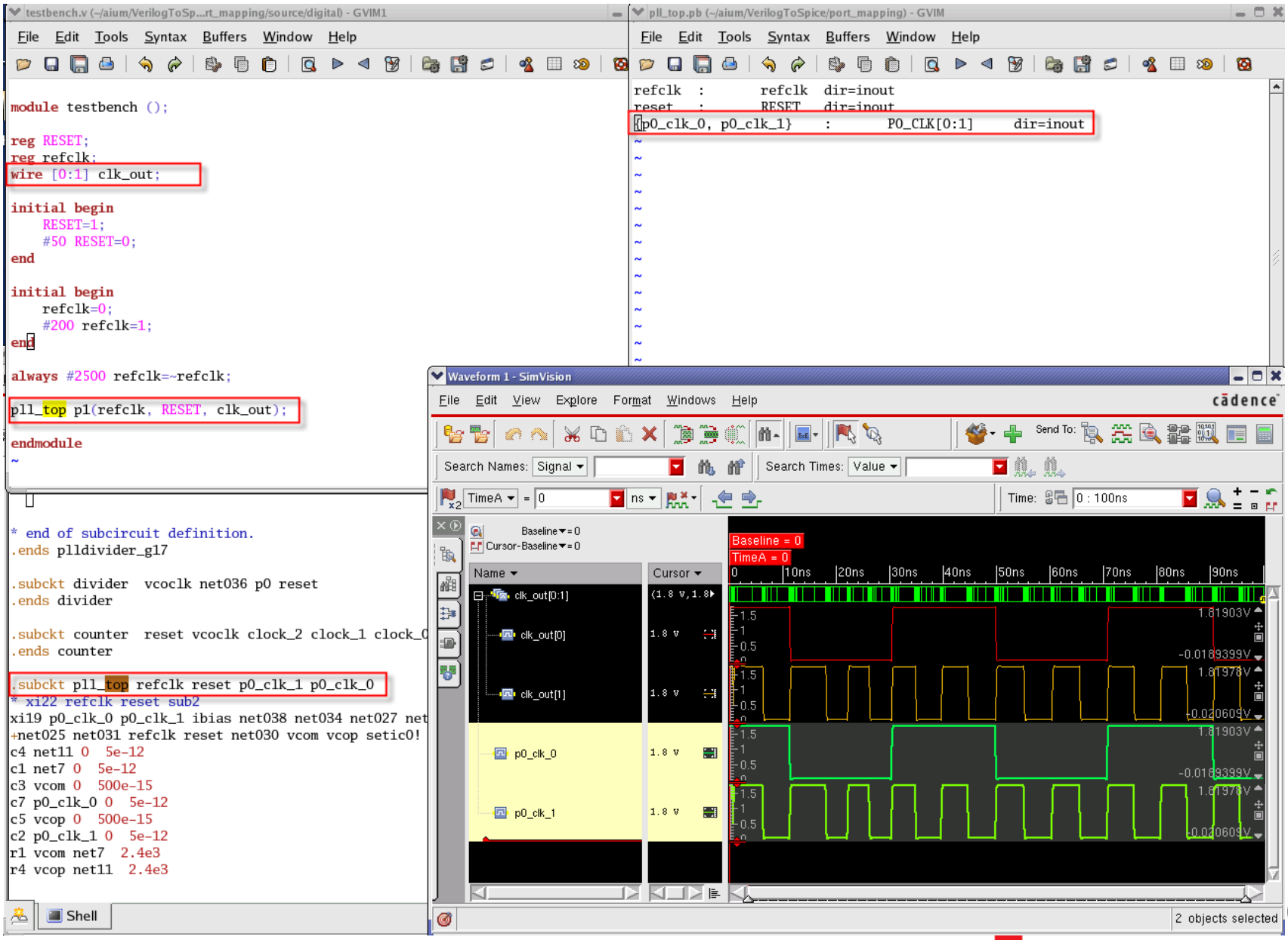
Port_map example



irun Use Model

```
irun  ./source/digital/*.v \
      ./amscf.scs \
      -solver aps \
      -timescale 1ns/100ps \
      -input probe.tcl
```

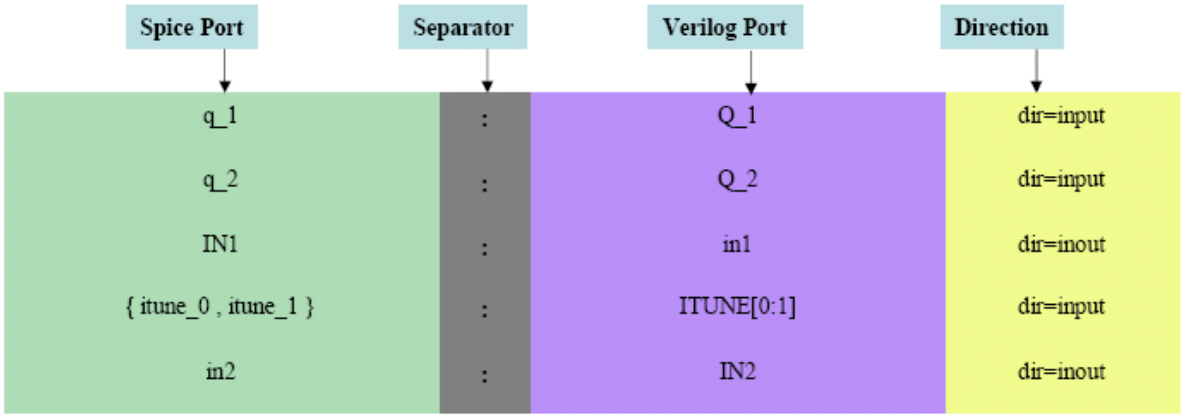
```
************
** amscf.scs
************
include "./source/analog/PLL.sp"
include "./models/gpdk_model.scs" section=tt

include "acf.scs"

amsd {
      portmap subckt=pll_top file="pll_top.pb"
      config cell="pll_top" use=spice
      ie vsup=1.8
       }
```

```
**********
** acf.scs
**********


.tran 1ns 400ns

.probe v(testbench.pll_top.vcom)
```

Verilog and spice interoperation

Port Mapping--- port_map file

Use model(Two Steps)
Firstly build mapping file between spice and verilog ports(file name: analog_top.pb)



Port Mapping--- port_map file

Then point to the mapping file in AMS control block/or prop.cfg

```
include "analog_top.sp"
amsd{
    portmap file="analog_top.pb"
    config cell=analog_top use=spice
  }
```

Analog Control Block

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AMS-XPS-MS

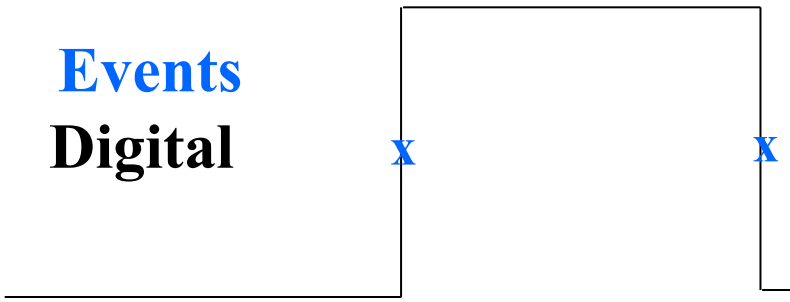
Use Model (AIUM Command-line Flow)

Enable AMS-XPS-MS post-layout flow

- Add irun command line option:
  - `-spectre_args "+ms +postlayout +speed=(1|2)"`
- Using +speed=3 is not recommended
- All the APS post-layout simulation techniques are also enabled with "+postlayout" for transistor analog partition

WREAL

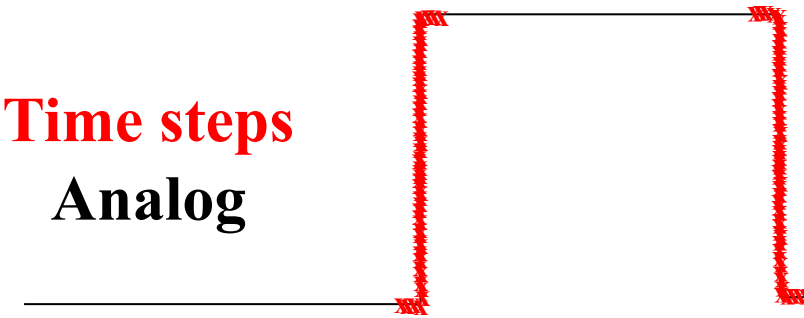
Analog vs. Digital simulation – Root cause of Performance Gap



- Digital solver solves logical expressions in a sequential manner based on triggering events
- Time and values are discrete

One computation per clock edge

vs



- The analog simulator must solve the entire analog system matrix at every simulation step
- Time and values are continuous

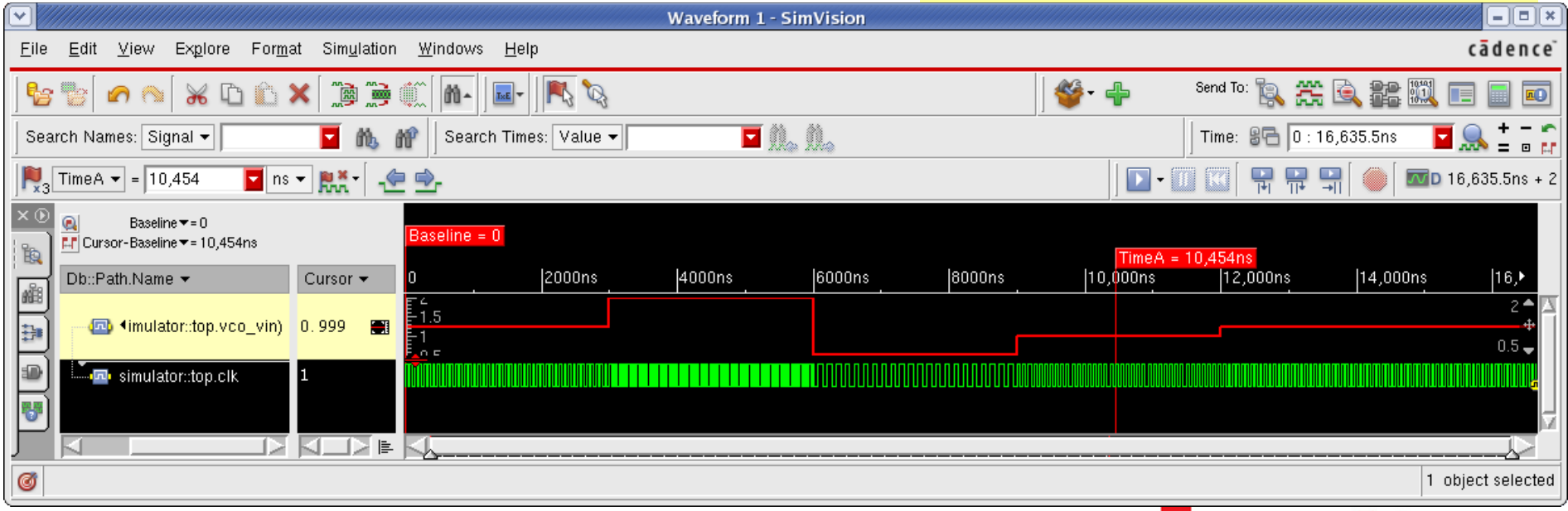
Many computations per clock edge

The wreal data type in Verilog-AMS

- Wreal data type declares a real net that has a real-valued connection
  - Wreal is time-discrete (event based)
  - Wreal wires can be used as ports
  - Infinite number of values – real

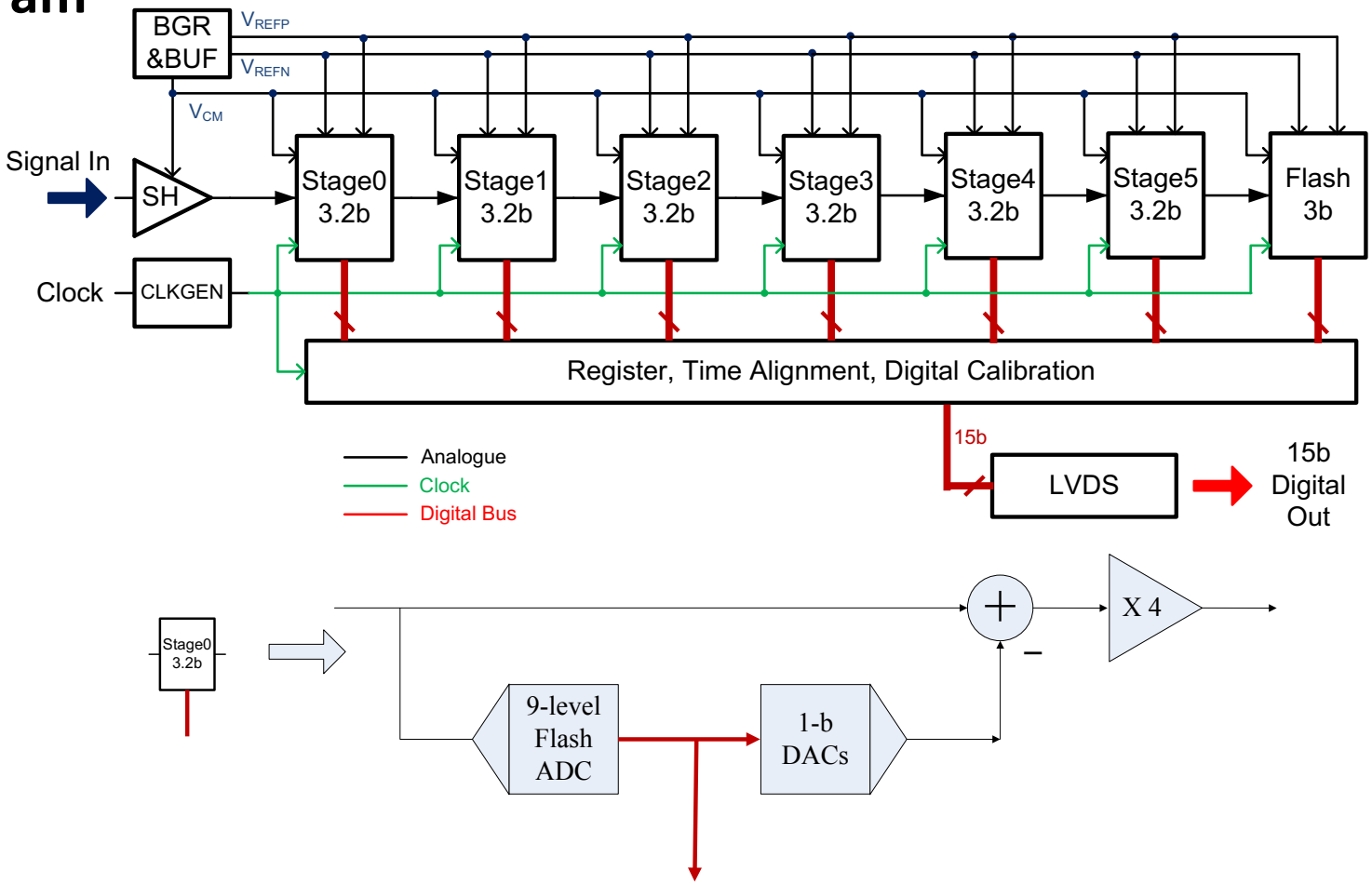
```
`timescale 1ns/1ps
module vco(vin, clk);
input vin; wreal vin;
output clk;
reg clk=0;

parameter real center_freq=1M,
    vco_gain=center_freq*0.3;
real freq,
```



Design Project: 15-bit CMOS Pipelined ADC

Diagram



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15-bit PADC: Traditional Design Flow

- Models for top level verification:
  - Clock generator: verilogA
  - Sample and Hold: verilogA
  - 9-level flash ADC: verilogA
  - MDAC0 (single stage): transistors/passive components
  - Ideal 16bit DAC: verilogA
  - Rest standard modules: verilogA

- Verification performance

  1 hour / 1 us

15-bit PADC: Traditional Design Flow

- Verification Targets:
  - Full-cycle functional verification (30M+ steps)including calibration
  - Timing control between stages is critical to get correct functionality

- Verification Challenges:
  - Pure digital simulation will take about 12 hours
  - Analog design and testbench in verilogA (simplified digital part)
    - 1us transient simulation takes 1 hour
    - For total 250ms+ simulation (30M+ steps):

    250000 hours=10416 days=28.54 years

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15-bit PADC: Real Number Modeling

- Models changed:
  - Clock generator: wreal
  - Sample and Hold: wreal
  - 9-level flash ADC: wreal
  - MDAC0 (single stage): wreal
  - Ideal 16bit DAC: wreal
  - Rest standard modules: Verilog
- Modeling effort: 7-day man work
  - Understand the design specs
  - Convert/build wreal models from scratch
  - Debug/Verify wreal models with schematics/specs

15-bit PADC: Real Number Modeling

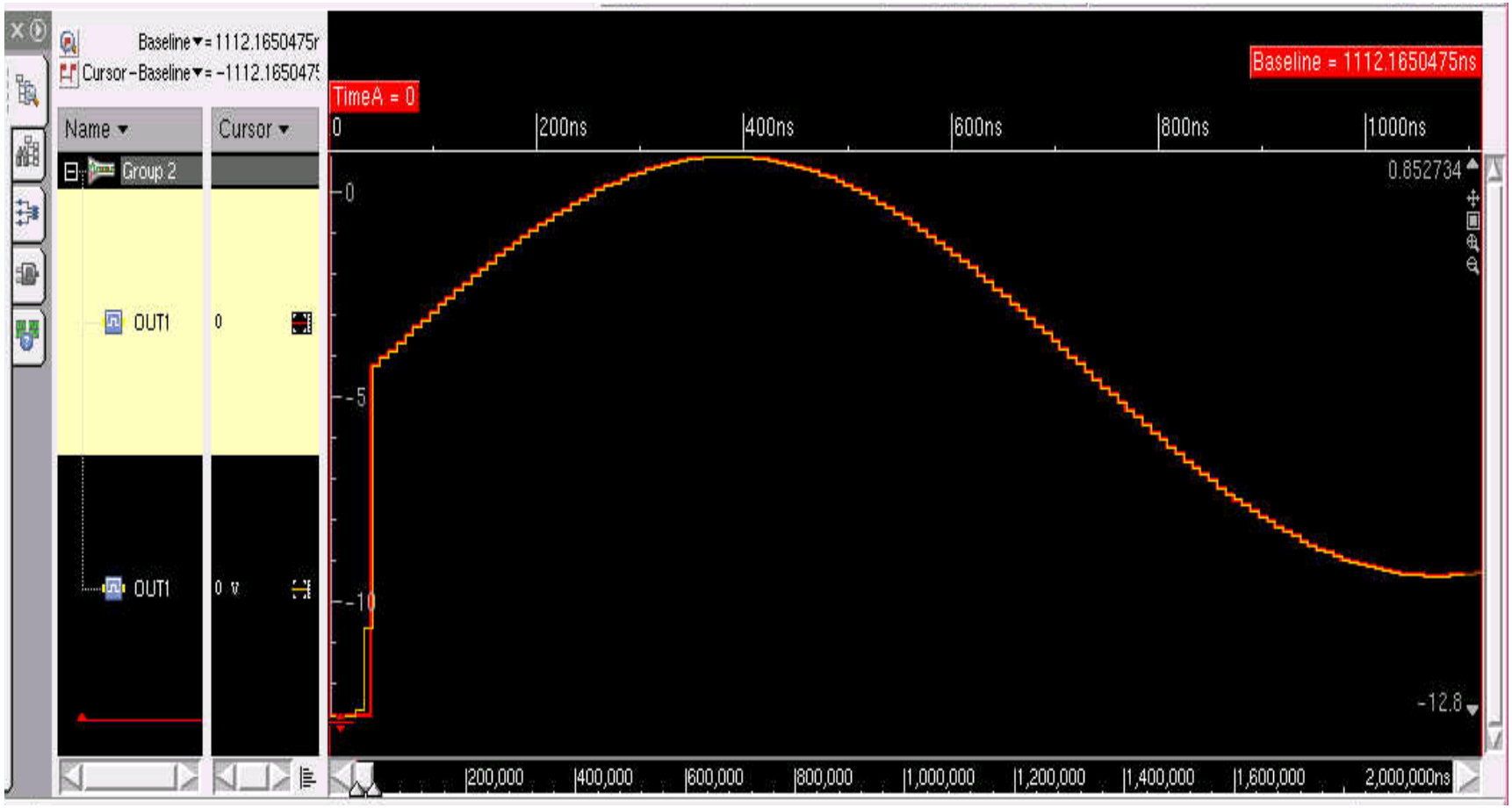
Performance: Wreal models vs. VerilogA models

- Seven-stage simulation (2us/2ms simulation)

	Seven-stage ADC with Peripheral (coder and ideal 16bit DAC)						
	2us simulation			2ms simulation			
	performance	Analog Step	Simulator Profile	performance	Analog Step	Simulator Profile	Note
VerilogA models	33m32s	214911	Analog 99.8% Digital 0.2%	too slow	N/A	N/A	Peripheral in VerilogA
Wreal models	89.437ms	54	Digital 100%	1m21s	54	Digital 100%	Peripheral in Verilog/Wreal
Speed up	**22496.3X**						

Note: optimized verilogA model makes 1us/16m

15-bit PADC: Real Number Modeling



16-bit ideal DAC output overlay

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