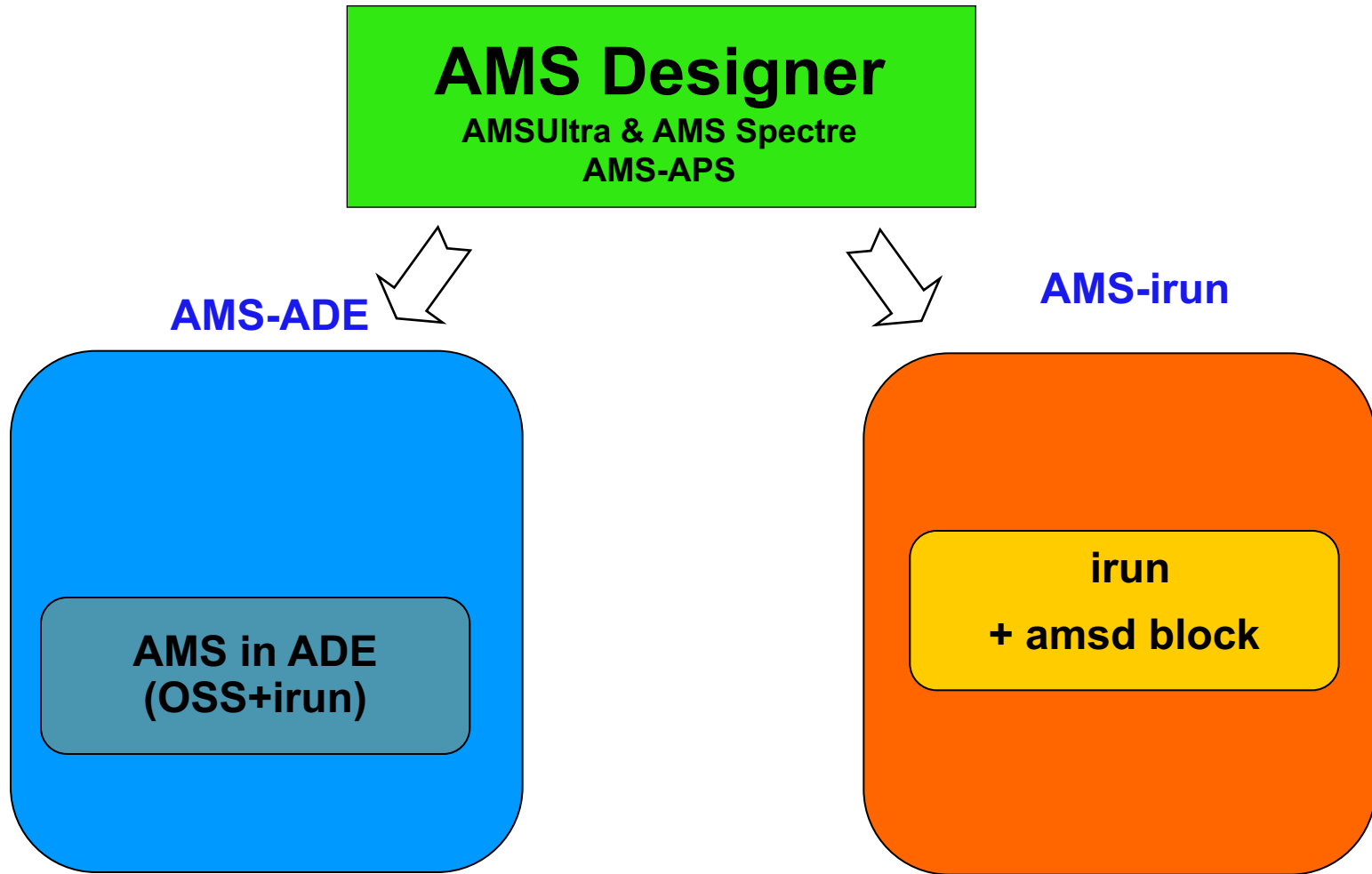


Co-Sim

March, 2017



Use Mode

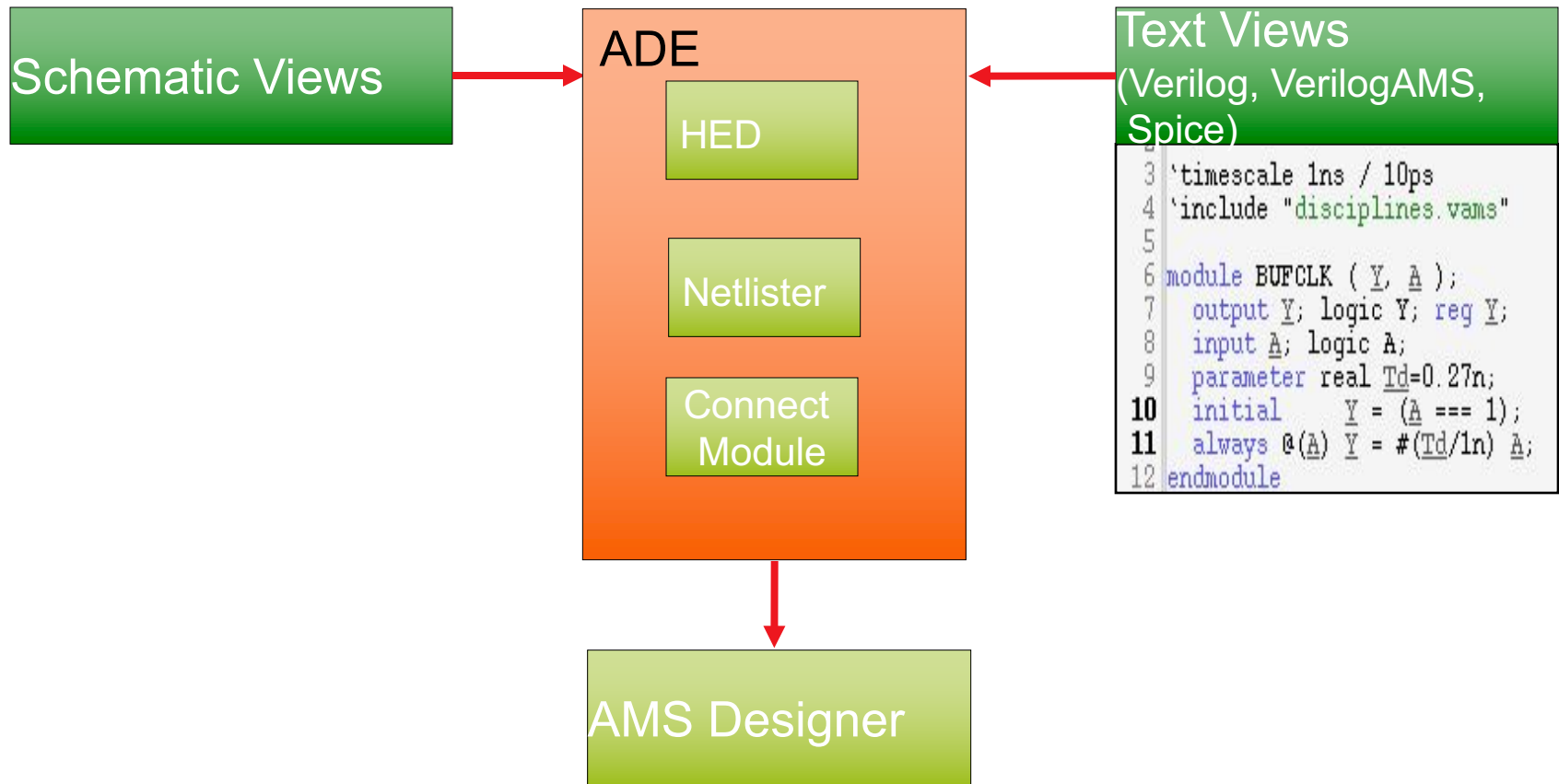


IC61_Inst_Dir/tools/dfll/samples/tutorials/AMS

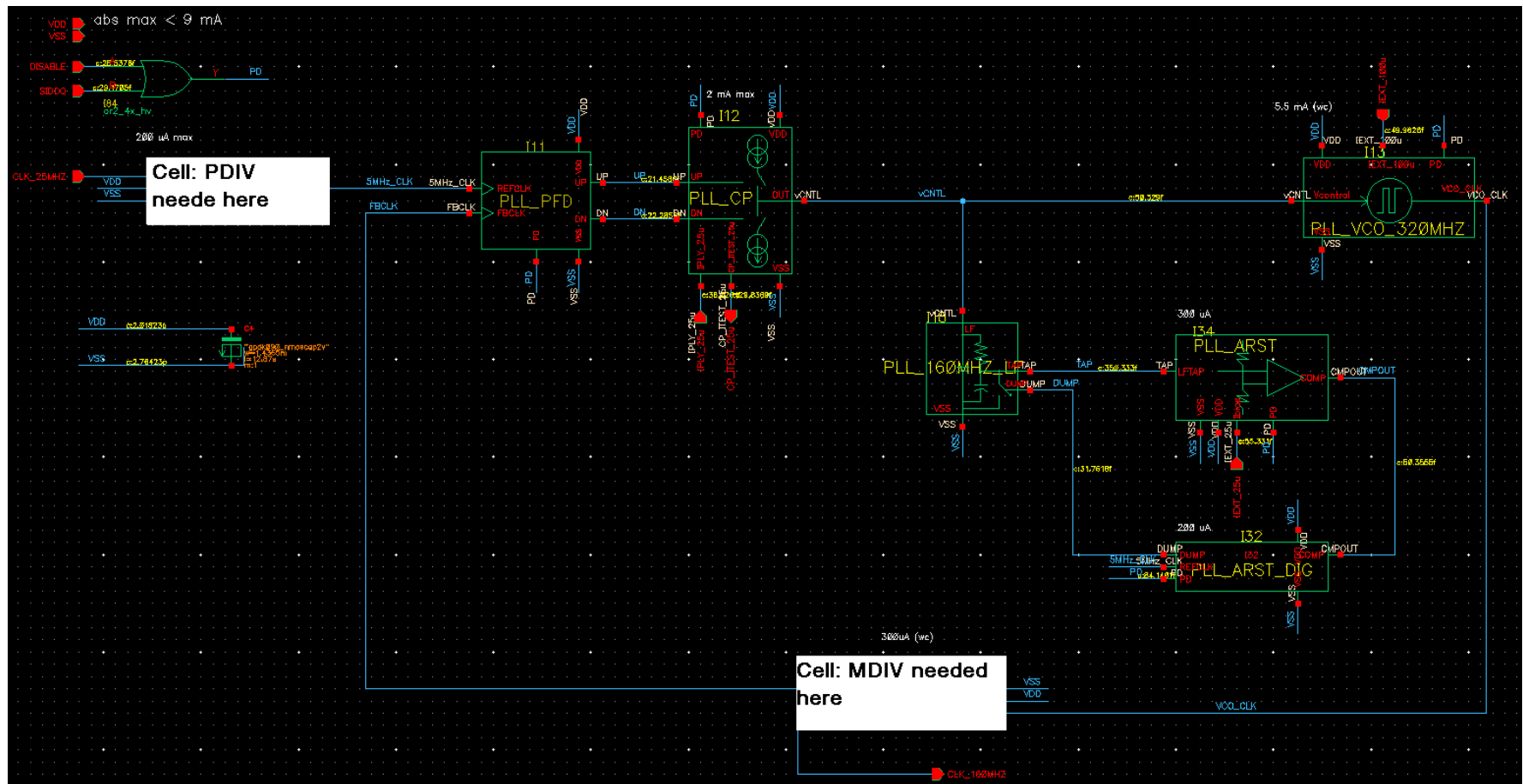
INCISIVE_Inst_Dir/tools/amsd/samples/aium

AMS-ADE

AMS-ADE Flow



Example:PLL_160MHz

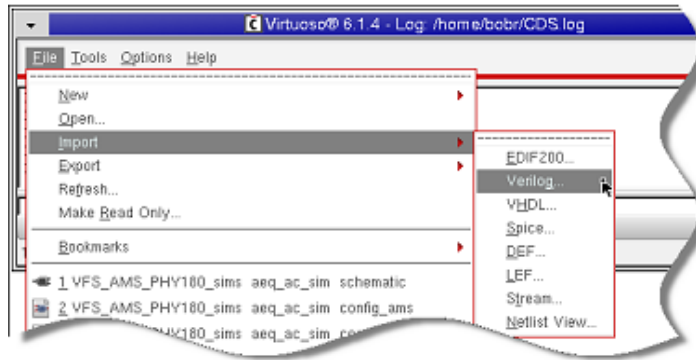


PLL_160MHZ_PDIV & PLL_160MHZ_MDIV are verilog description.

VerilogIn/VHDL In

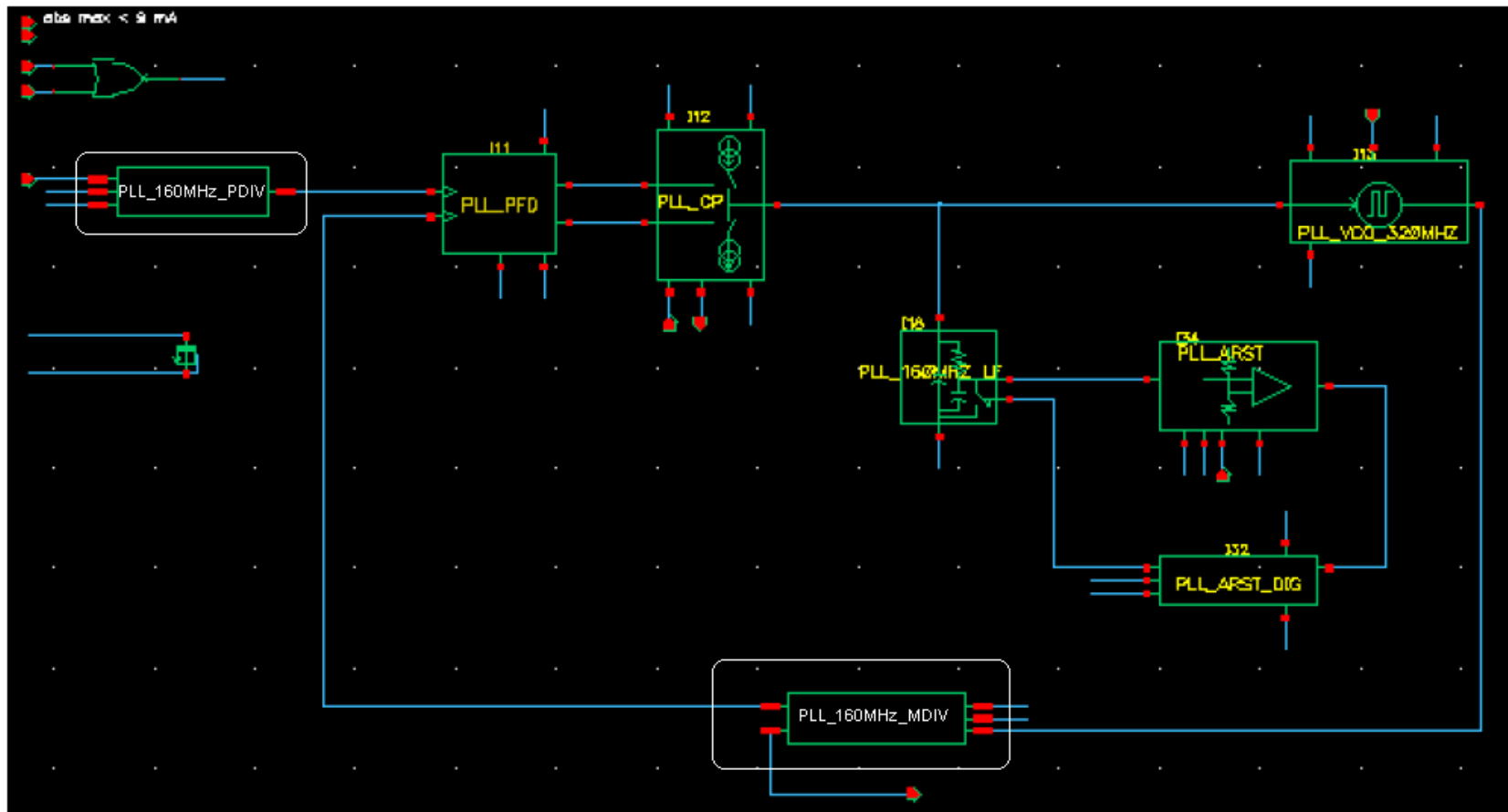
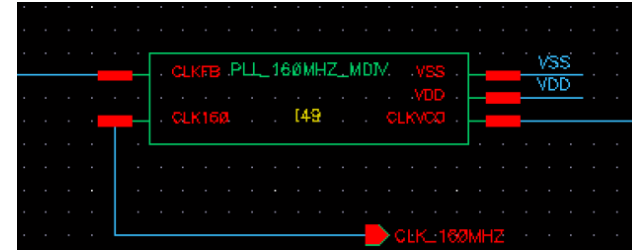
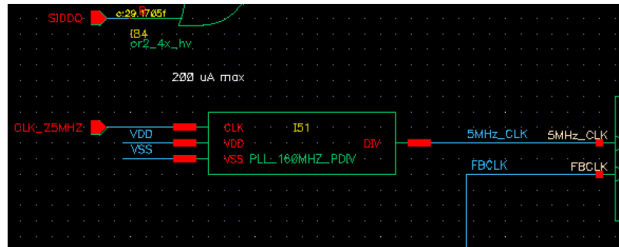
- From the CIW, File->Import->Verilog... (or VHDL)

```
module PLL_160MHZ_MDIV (CLK160, CLKFB, CLKVCO, VDD, VSS);  
    output CLK160;  
    output CLKFB;  
    input CLKVCO;  
    input VDD;  
    input VSS;  
  
    integer i;  
    reg CLKFB, CLK160;  
  
    initial  
        begin  
            CLKFB=0;  
            CLK160=0;  
            i=0;  
        end  
  
    always @( posedge CLKVCO)  
        begin  
            CLK160 = ~ CLK160;  
            if (i==0)  
                CLKFB = 1;  
            else  
                CLKFB = 0;  
            i=i+1;  
            if (i==64) i=0;  
        end  
  
endmodule
```

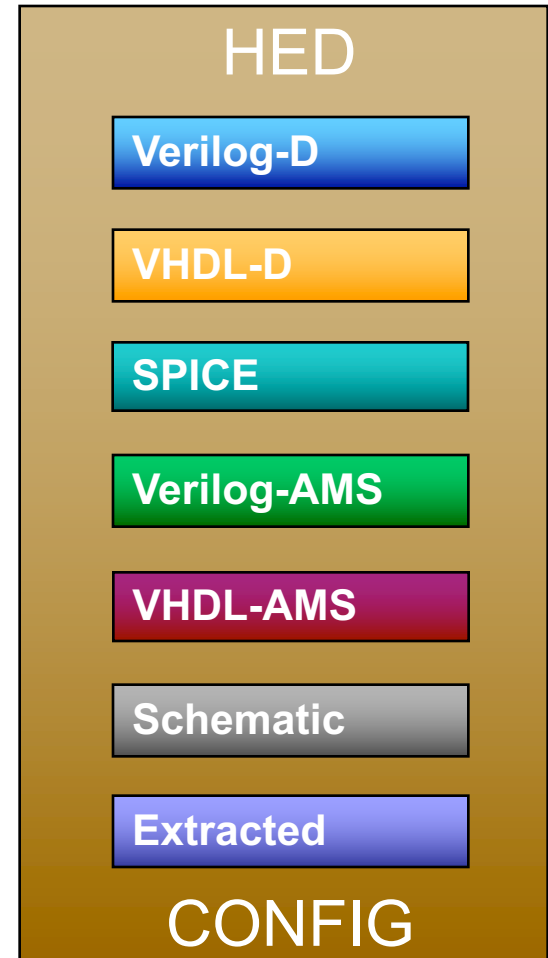
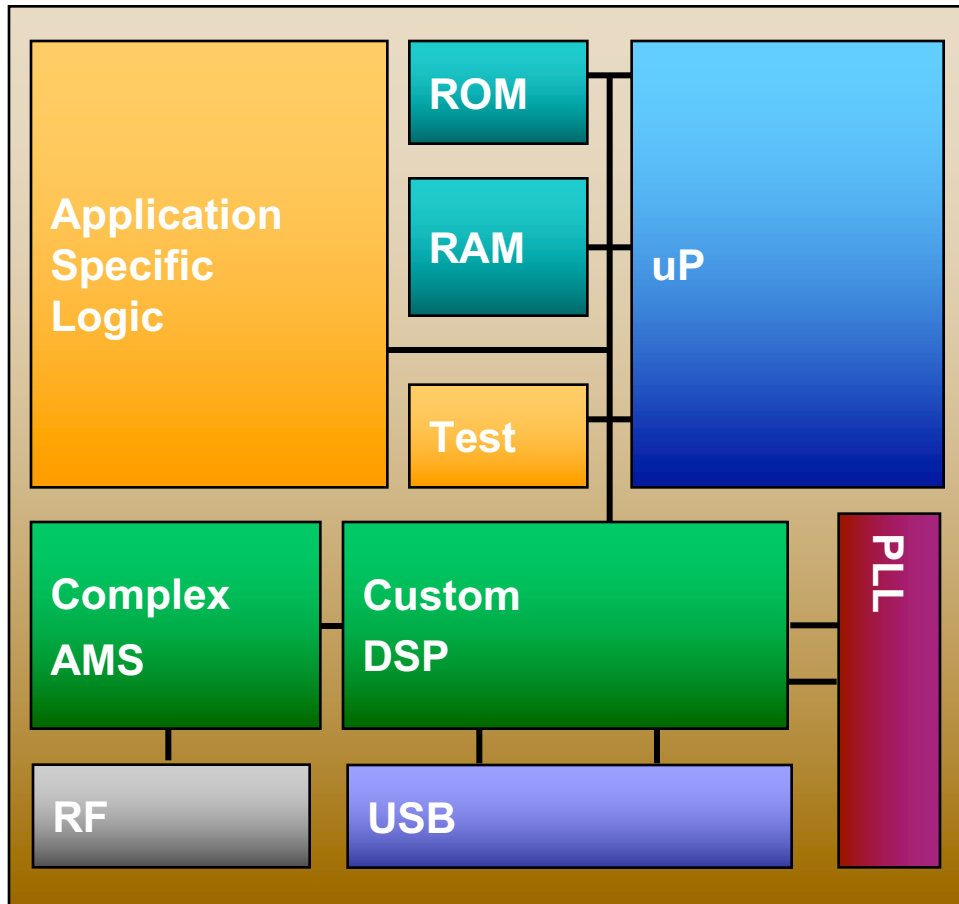


```
module PLL_160MHZ_PDIV (DIV, CLK, VDD, VSS);  
    output DIV;  
    input CLK;  
    input VDD;  
    input VSS;  
  
    reg DIV;  
    integer i;  
  
    initial  
        begin  
            DIV=0;  
            i=0;  
        end  
  
    always @( posedge CLK)  
        begin  
            if (i==0)  
                DIV = 1;  
            else  
                DIV = 0;  
  
            i=i+1;  
  
            if (i==5) i=0;  
        end  
  
endmodule
```

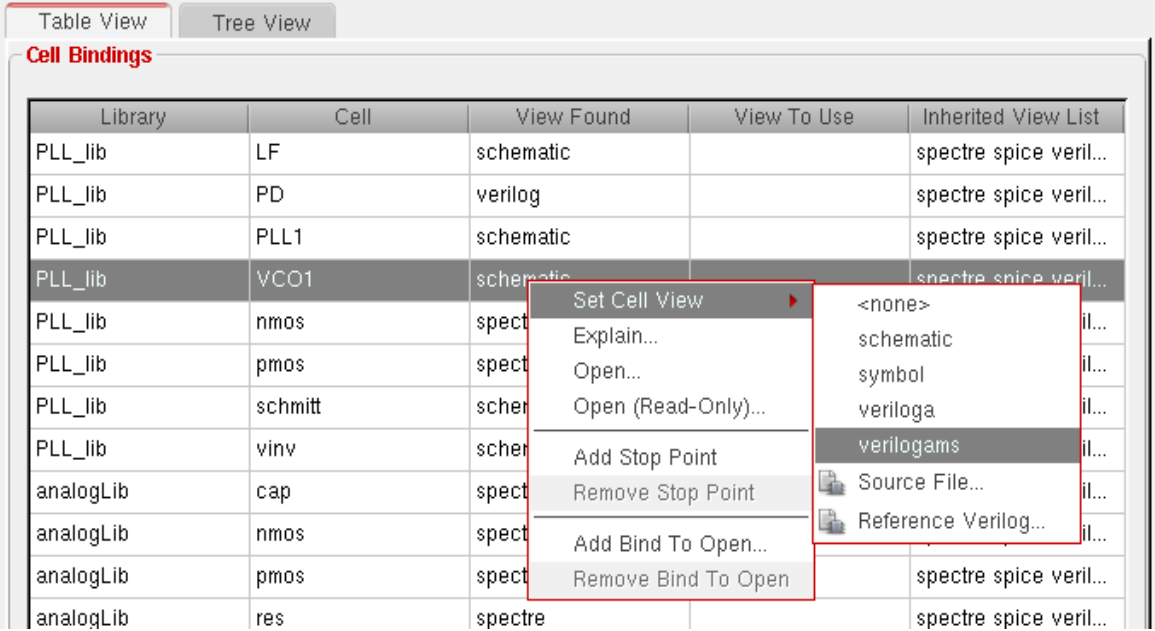
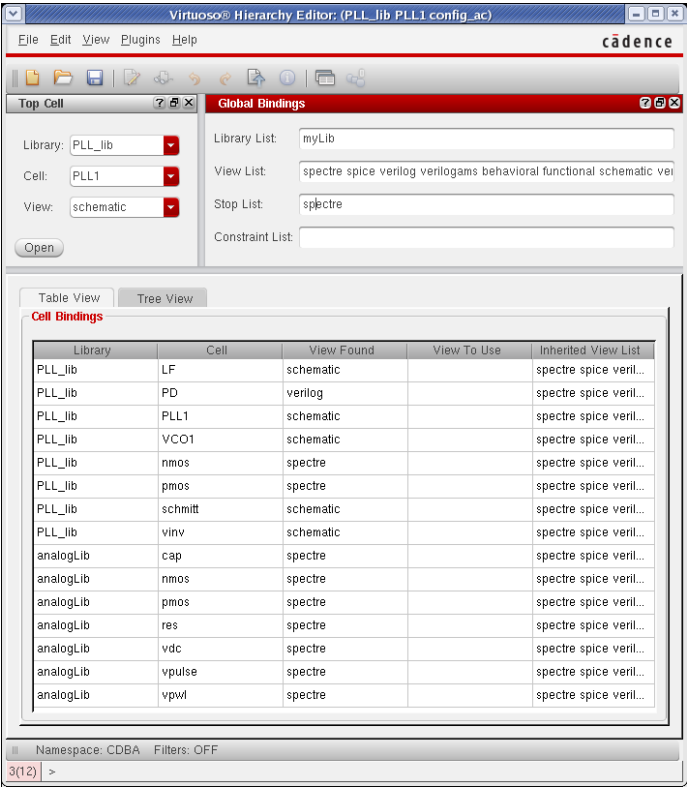
Complete mix-signal design in schematic



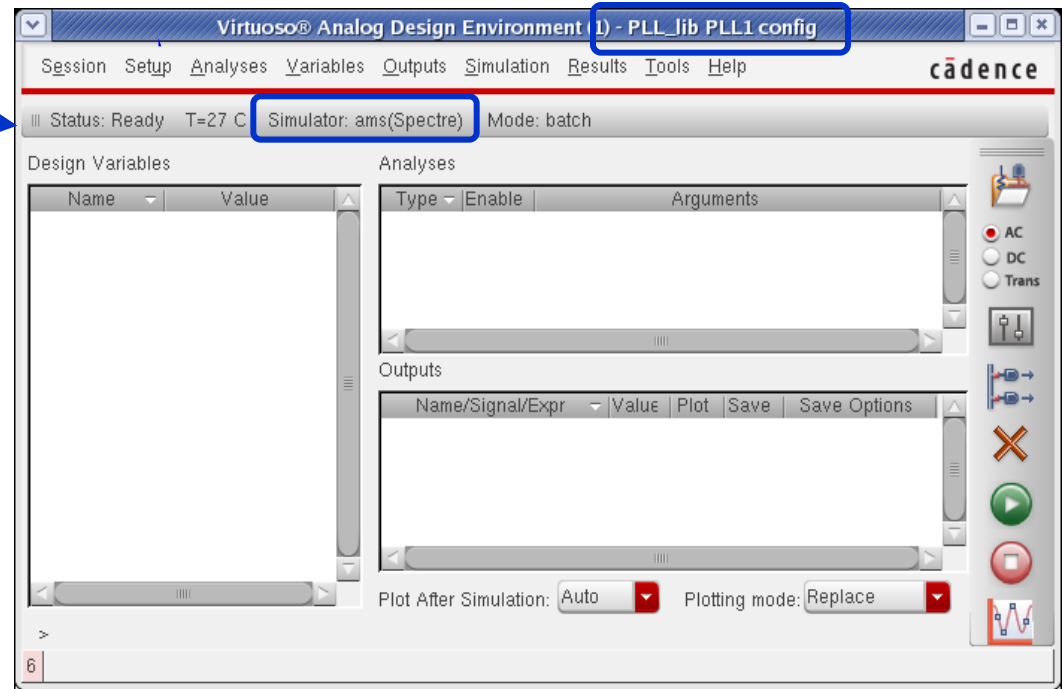
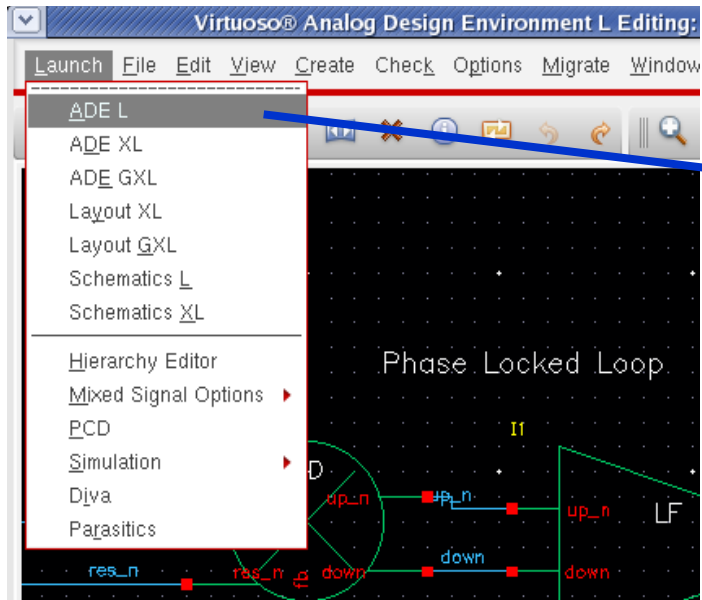
Configured Schematic



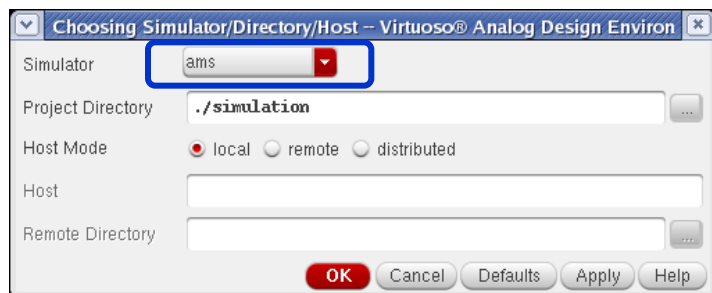
Hierarchy Editor



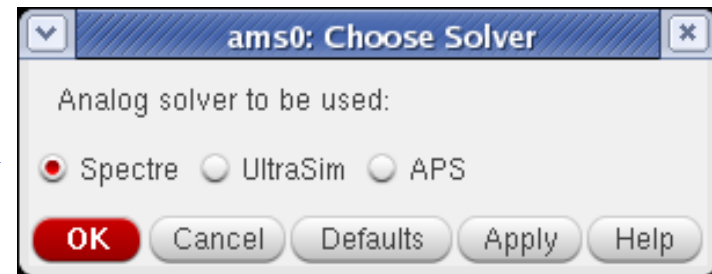
AMS in ADE



ADE->Simulator/Directory/Host ...



ADE->Simulation->Solver



Easily Multi Voltage Setup

IE Setup

Enable	Scope	Vsup	Scope Applied To	Updated Parameters
<input checked="" type="checkbox"/>	global	1.8		
<input checked="" type="checkbox"/>	inst	1.8	top.i2 top.i1	
<input type="checkbox"/>				<Click here to add new ie card>

Double click to enable advanced setup

Advanced Setup

IE Parameters

Basic | **Extended**

Parameter	Value
mode	split
connrule	connectLib.CR_full
vss	0
vlo	`vss
vhi	`vsup+`vss
vthi	`vlo+(`vhi-(`vlo`))*2.0/3.0

Select advance setup to show IE parameters OR double click on IE card in table

Tool tip as description of parameter

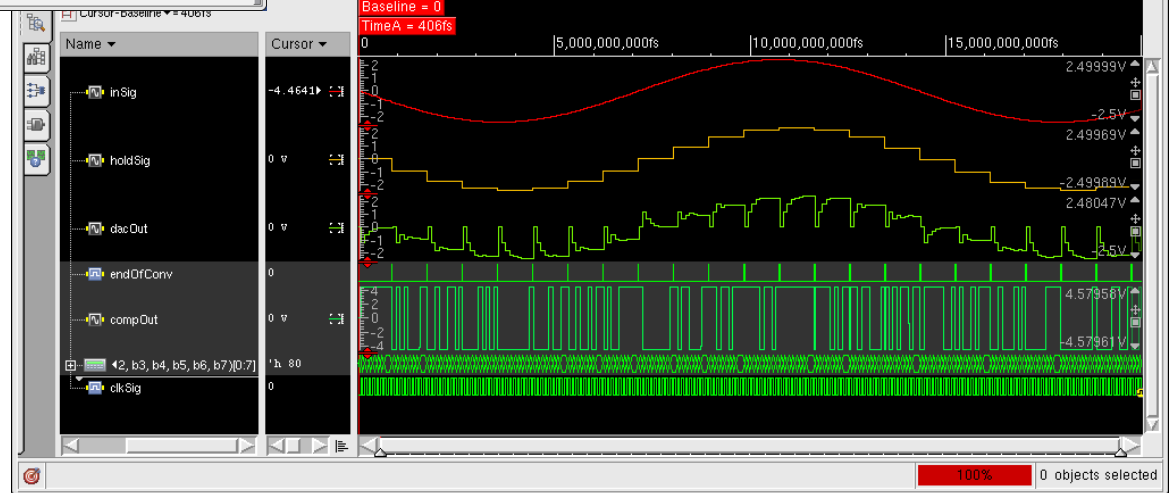
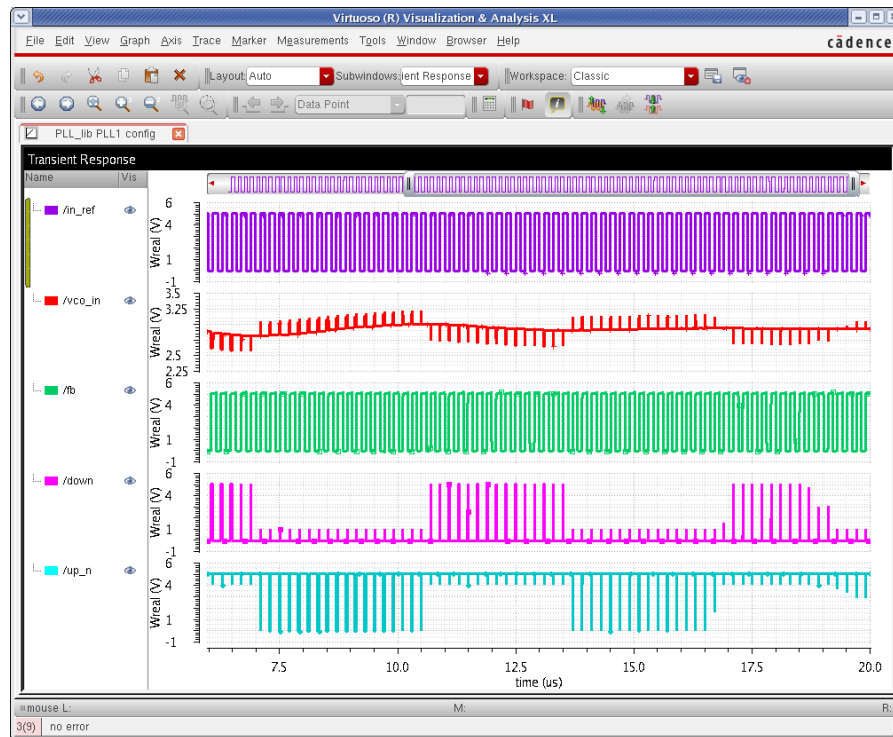
ie_cards.scs

```
amsd{
  ie vsup=1.8 connrules=CR_full_fast
  ie vsup=1.8 connrules=CR_full inst=top.i2 mode=split
}
```

View Connect Rule vams

View Connect Rule

Waveform Display



Save and Restart

SAVE AND RESTART OPTIONS

☐ Restart from:

Snapshot prefix

Save time(s)

Save incr Start time Stop time

SAVE AND RESTART OPTIONS

☒ Restart from:

Snapshot prefix

Save time(s)

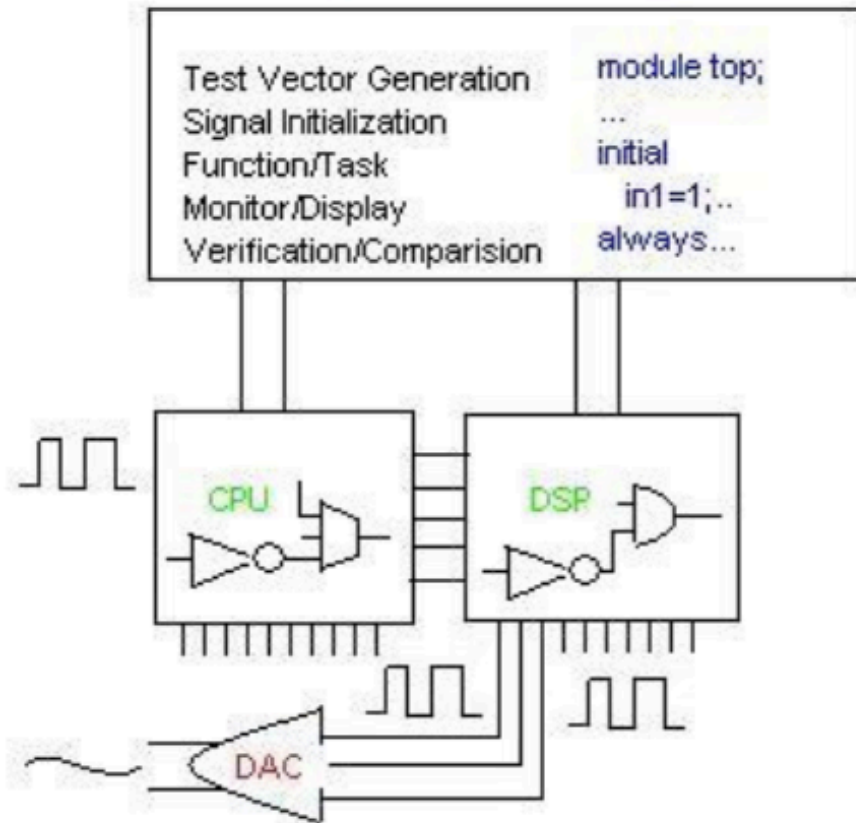
Save incr

Stop time

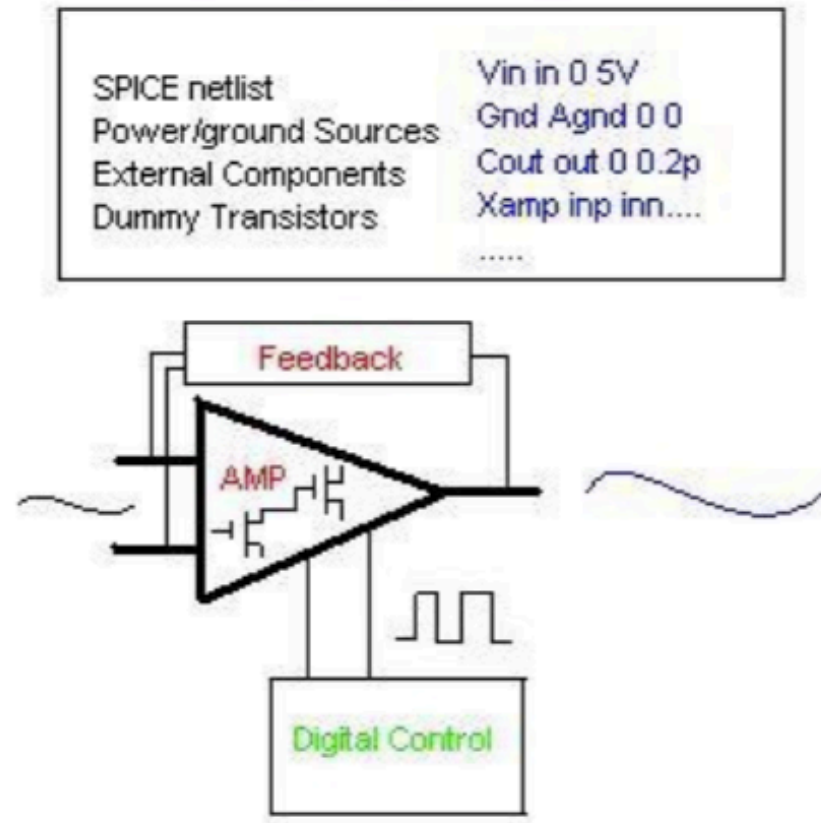
AMS-IRUN

AMS-irun flow

Verilog(ams) on Top



SPICE on Top



Port_map example

The image displays a Verilog testbench and its corresponding simulation waveform. The testbench is named `testbench.v` and is located at `~/aium/VerilogToSpice/port_mapping/source/digital`. The waveform viewer, titled `Waveform 1 - SimVision`, shows the simulation results for the `p1l_top` module.

Testbench Code:

```
module testbench ();
reg RESET;
reg refclk;
wire [0:1] clk_out;

initial begin
    RESET=1;
    #50 RESET=0;
end

initial begin
    refclk=0;
    #200 refclk=1;
end

always #2500 refclk==refclk;

p1l_top p1(refclk, RESET, clk_out);
endmodule
```

Waveform Details:

- Signals:** The waveform shows three signals: `clk_out[0:1]`, `p0_clk_0`, and `p0_clk_1`.
- Time Scale:** The time scale is set to 0 to 100ns.
- Signal Levels:** The signals are shown with voltage levels ranging from -0.0189399V to 1.81903V.
- Cursor:** A cursor is positioned at TimeA = 0 ns.

Simulation Results:

- The `clk_out[0:1]` signal is a square wave with a period of approximately 20ns.
- The `p0_clk_0` and `p0_clk_1` signals are square waves with a period of approximately 20ns.

irun Use Model

```
irun ./source/digital/*.v \  
    ./amscf.scs \  
    -solver aps \  
    -timescale 1ns/100ps \  
    -input probe.tcl
```

```
*****  
**  amscf.scs  
*****  
include "./source/analog/PLL.sp"  
include "./models/gpdk_model.scs" section=tt  
  
include "acf.scs"  
  
amsd {  
    portmap subckt=pll_top file="pll_top.pb"  
    config cell="pll_top" use=spice  
    ie vsup=1.8  
}
```

```
*****  
**  acf.scs  
*****  
  
.tran 1ns 400ns  
  
.probe v(testbench.pll_top.vcom)
```

Verilog and spice interoperation

Port Mapping--- port_map file

Use model(Two Steps)

Firstly build mapping file between spice and verilog ports(file name: analog_top.pb)

Spice Port	Separator	Verilog Port	Direction
q_1	:	Q_1	dir=input
q_2	:	Q_2	dir=input
IN1	:	in1	dir=inout
{ itune_0 , itune_1 }	:	ITUNE[0:1]	dir=input
in2	:	IN2	dir=inout

Port Mapping--- port_map file

Then point to the mapping file in AMS control block/or prop.cfg

```
include "analog_top.sp"  
amsd{  
    portmap file="analog_top.pb"  
    config cell=analog_top use=spice  
}
```

Analog Control Block

AMS-XPS-MS

Use Model (AIUM Command-line Flow)

Enable AMS-XPS-MS post-layout flow

- Add irun command line option:
 - `-spectre_args "+ms +postlayout +speed=(1|2)"`
- Using +speed=3 is not recommended
- All the APS post-layout simulation techniques are also enabled with “+postlayout” for transistor analog partition



WREAL

Analog vs. Digital simulation – Root cause of Performance Gap

Events
Digital

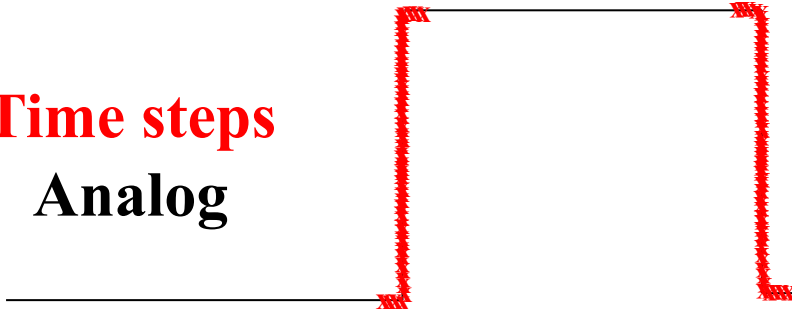


- Digital solver solves logical expressions in a sequential manner based on triggering events
- Time and values are discrete

One computation per clock edge

VS

Time steps
Analog



- The analog simulator must solve the entire analog system matrix at every simulation step
- Time and values are continuous

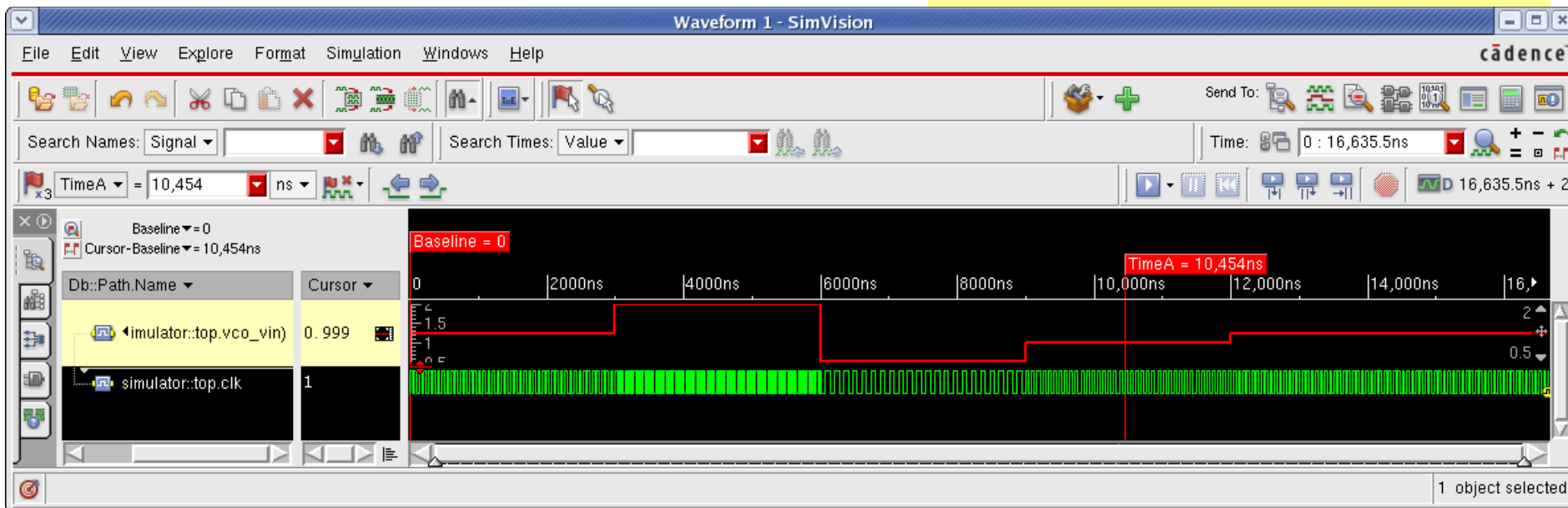
Many computations per clock edge

The wreal data type in Verilog-AMS

- Wreal data type declares a real net that has a real-valued connection
 - Wreal is time-discrete (event based)
 - Wreal wires can be used as ports
 - Infinite number of values – real

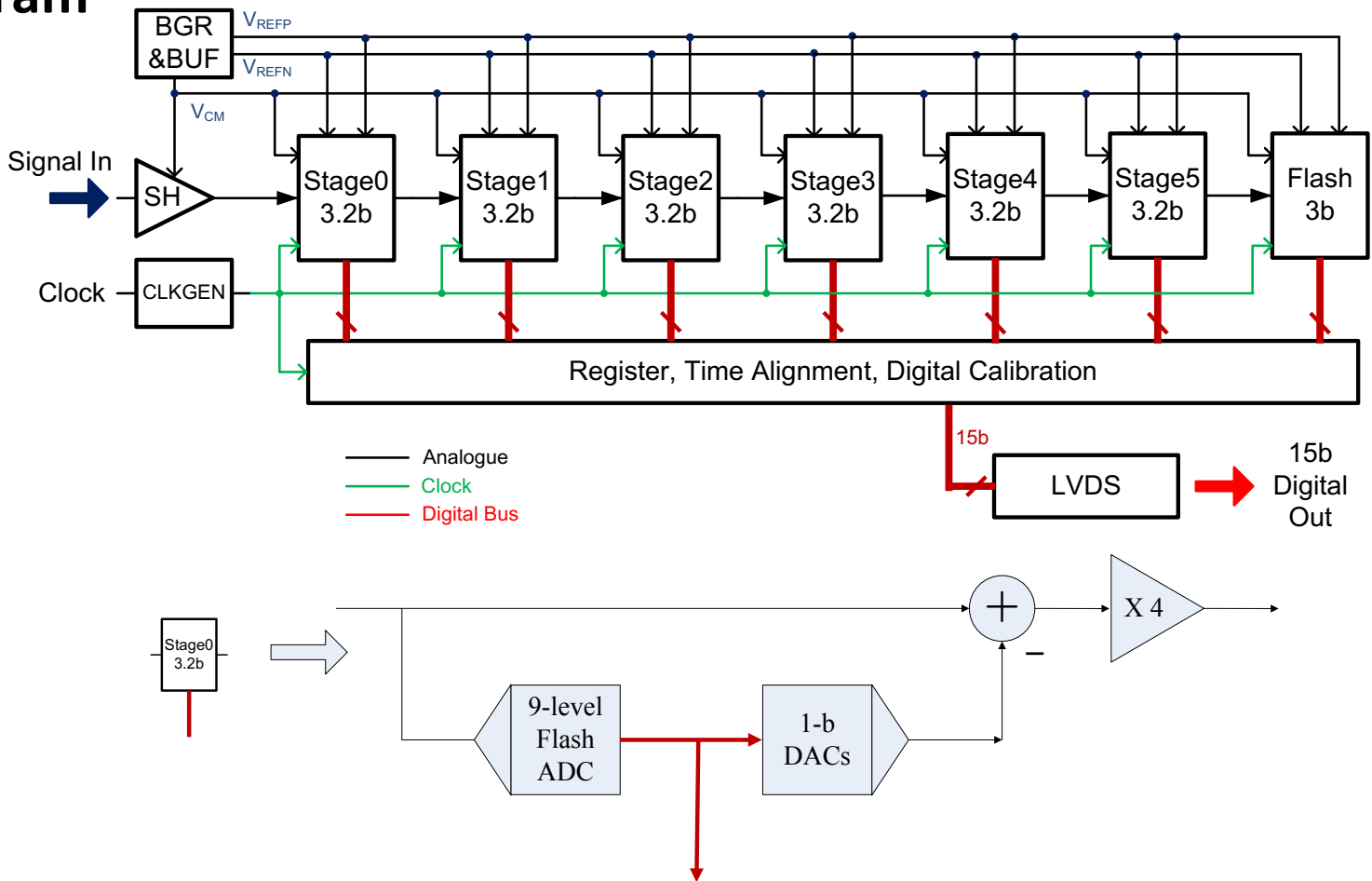
```
`timescale 1ns/1ps
module vco(vin, clk);
input vin; wreal vin;
output clk;
reg clk=0;

parameter real center_freq=1M,
            vco_gain=center_freq*0.3;
real freq,
```



Design Project: 15-bit CMOS Pipelined ADC

Diagram



15-bit PADC: Traditional Design Flow

- Models for top level verification:
 - Clock generator: verilogA
 - Sample and Hold: verilogA
 - 9-level flash ADC: verilogA
 - MDAC0 (single stage): transistors/passive components
 - Ideal 16bit DAC: verilogA
 - Rest standard modules: verilogA
- Verification performance
1 hour / 1 us

15-bit PADC: Traditional Design Flow

- Verification Targets:
 - Full-cycle functional verification (30M+ steps)including calibration
 - Timing control between stages is critical to get correct functionality
- Verification Challenges:
 - Pure digital simulation will take about 12 hours
 - Analog design and testbench in verilogA (simplified digital part)
 - 1us transient simulation takes 1 hour
 - For total 250ms+ simulation (30M+ steps):
250000 hours=10416 days=28.54 years



Can we wait?

15-bit PADC: Real Number Modeling

- Models changed:
 - Clock generator: **wreal**
 - Sample and Hold: **wreal**
 - 9-level flash ADC: **wreal**
 - MDAC0 (single stage): **wreal**
 - Ideal 16bit DAC: **wreal**
 - Rest standard modules: **Verilog**
- Modeling effort: 7-day man work
 - Understand the design specs
 - Convert/build **wreal** models from scratch
 - Debug/Verify **wreal** models with schematics/specs

15-bit PADC: Real Number Modeling

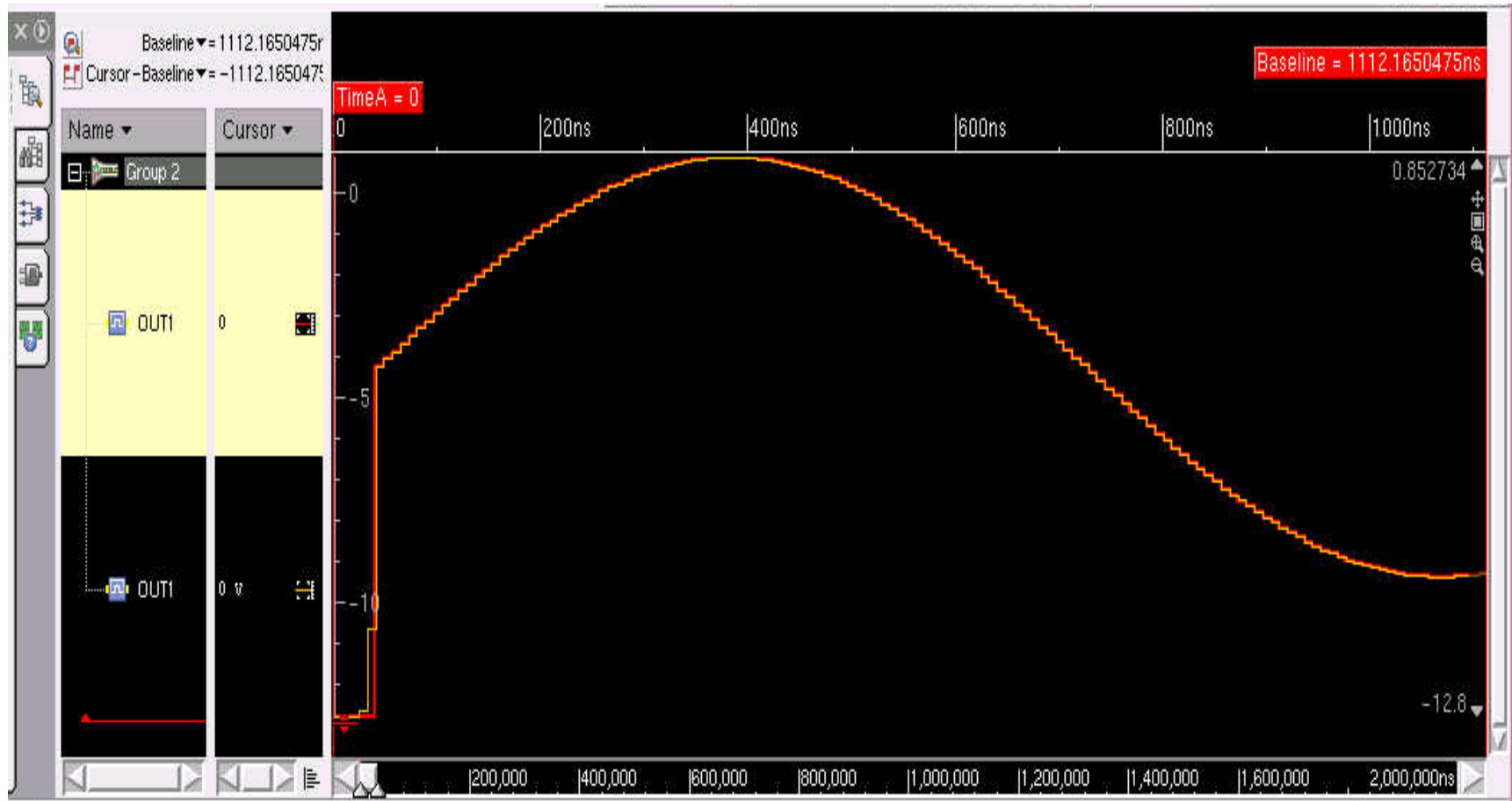
Performance: Wreal models vs. VerilogA models

- Seven-stage simulation (2us/2ms simulation)

	Seven-stage ADC with Peripheral (coder and ideal 16bit DAC)						
	2us simulation			2ms simulation			
	performance	Analog Step	Simulator Profile	performance	Analog Step	Simulator Profile	Note
VerilogA models	33m32s	214911	Analog 99.8% Digital 0.2%	too slow	N/A	N/A	Peripheral in VerilogA
Wreal models	89.437ms	54	Digital 100%	1m21s	54	Digital 100%	Peripheral in Verilog/Wreal
Speed up	22496.3X						

Note: optimized verilogA model makes 1us/16m

15-bit PADC: Real Number Modeling



16-bit ideal DAC output overlay



cā dence™

