12.2 A 7nm FinFET SRAM Macro Using EUV Lithography for Peripheral Repair Analysis

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Conventional patterning techniques, such as self-aligned double patterning (SADP) and litho-etch-litho-etch (LELE), have paved the way for the extreme ultraviolet (EUV) technology that aims to reduce the photomask steps [1,2]. EUV adds the extreme scaling to the high-performance of FinFET technology, thus opening up new opportunities for system-on-chip designers: delivering power, performance, and area (PPA) competitiveness. In terms of area, peripheral logic has scaled down aggressively in comparison to the bitcell given the intense design-rule shrinkage. Figure 12.2.1 shows the bitcell scaling trend and the peripheral logic unit area across different process nodes. Compared to the 10nm process node, the peripheral logic unit area is closer to the bitcell area in a 7nm process node aided by EUV, which allows bi-directional metal lines for scaling. Complex patterns and intensive scaling induce defective elements in the SRAM peripheral logic. Therefore, the probability of yield-loss due to defects is high, which necessitates the need for a repair scheme for the peripheral logic in addition to the SRAM bitcell. Despite the varied literature on bitcell repair, such as the built-in self-repair that analyzes the faulty bitcells to allocate the repair efficiently for a higher repairable rate [3], literature that discusses peripheral logic repair is sparse. Early literature [4] discusses the usage of a sense-amplifier, designed with redundancy, to address the sense-amplifier offset. Nevertheless, it is not related to the peripheral logic repair for yield improvement. This paper exclusively addresses the peripheral logic repair issue to achieve a higher repairable rate. A separate analysis of SRAM macro defect failures, in the bitcell and peripheral logic, provides a deeper understanding so as to increase the maximum repairable rate under random defect conditions.

Figure 12.2.2 shows a conventional column and peripheral repair approach; in which a bitcell defect (*B*) or a peripheral-defect (*P)* is repaired using a bitcell and peripheral tie. As such, it is possible to create a wasted resource (*W*) that could be, instead, used for additional repairs. Otherwise, an additional defect (*AU*) becomes irreparable due to the lack of redundancy in the conventional column repair; specifically, once all redundancies (*R*) are used. We propose finer grain redundancy control to provide a higher coverage of additional defects (AR). Figure 12.2.3 illustrates the repair decision diagram for the conventional and proposed methods. The conventional method begins by checking for a bitcell or peripheral defect, and uses available array redundancy to replace the whole of the defective column: bitcell and peripheral logic regardless of where the actual defect is located. In contrast, in this work a defect in the peripheral logic is replaced using the available peripheral redundancy, and the bitcell is addressed for additional repair independently. Handling the bitcell array and the peripheral separately helps increase the repairable rate using the peripheral repair method. Figure 12.2.3 compares the maximum repairable rate versus the available redundancy. The peripheral repair method can achieve up to a 2× higher maximum repairable rate compared to the conventional method.

An SRAM macro is designed to validate the failure phenomena for the effectiveness of the peripheral repair. Fig. 12.2.4 illustrates the SRAM test-chip with the peripheral repair analysis circuit. The efficiency of the peripheral repair scheme is assessed by analyzing the failure map for the test-chip. Using the divide and conquer rule, detour logic is implemented between the array and the peripheral logic to validate the possible failure spots. Figure 12.2.5 illustrates the SRAM macro functional blocks: sense amplifier, write-driver, and the detour logic. An SRAM write-assist scheme is implemented using WL overdrive (WLOD) and negative BL (NBL). WL underdrive (WLUD) is also implemented for read-assist.

The detour logic, Fig. 12.2.4, bypasses the internal signals to detect the defective failure spot. DETOUR-I checks the functionality of the SRAM data in and out (DQ) block. Similarly, DETOUR-II and DETOUR-III check the functionality of the peripheral logic and the bitcell. When the detour mode is enabled, the detour logic (Fig. 12.2.5c) disconnects the IN_{orig_B}-OUT_{orig_B} path and then configures IN_{orig_A}-OUT_{orig_B} path as shown in Fig. 12.2.5(c), which helps to validate the failure between the bitcell array and peripheral logic.

A 512kb SRAM macro is designed in a 7nm FinFET technology using EUV lithography. The 6T high-density (HD) SRAM bitcell is designed with a PU:PG:PD=1:1:1 fin number. As shown in Fig. 12.2.1, the 7nm FinFET 6T-HD SRAM bitcell exhibits the best scaling (smallest bitcell) published thus far.

Figure 12.2.6 shows the measured results of the macro using the detour test. Various failure maps are obtained by applying the detour test-modes. This helps to analyze the defective and the repairable failures. Silicon test results have shown that DETOUR-I skips the bitcell array and the peripheral logic without any failures. DETOUR-II skips the bitcell array by highlighting the entire column failure in a certain column array, and the DETOUR-III highlights a mix of bitcell and peripheral logic failures. According to silicon results, we have proved that there is a higher probablilty to increase SRAM yield with peripheral logic repair in 7nm technology. By extension, this probability increases as the area of SRAM peripheral logic shrinks, and thus probability of failure increases, with EUV technology.

Since 16Kb of redundancy was designed for the 512kb of bitcells, there is a 3% maximum repairable rate using the conventional repair scheme, and a 6% repairable rate using the proposed peripheral repair scheme, as shown in Fig. 12.2.6. This increase in the repairable rate, when applied to bitcell failures under a reduced supply-voltage, improves V_{MIN} by 39.9mV. The peripheral repair scheme also requires an additional multiplexer between the bitcell array and the peripheral logic to bypass the column-to-peripheral signals. However, the 1% area overhead for the peripheral repair method is negligible when compared to the additional number of repair columns needed to achieve a similar repairable rate. A 3% latency overhead is also observed, which is attributed to the switch logic between the bitcell array and the sense amplifier. Although the SRAM peripheral repair scheme has an additional latency overhead, the increasing defective yield-loss for a 7nm technology aided by EUV necessitates the need for an SRAM repair scheme. The 7nm FinFET 6T-HD SRAM is also evaluated for V_{MIN} improvement using assist. Experimental results show that the write-assist of NBL and read-assist of WLUD improves V_{MIN} by 150mV. Fig. 12.2.7 shows a die micrograph of a 7nm FinFET 512Kb SRAM test-chip with standard cell and I/O, which are designed with EUV lithography.

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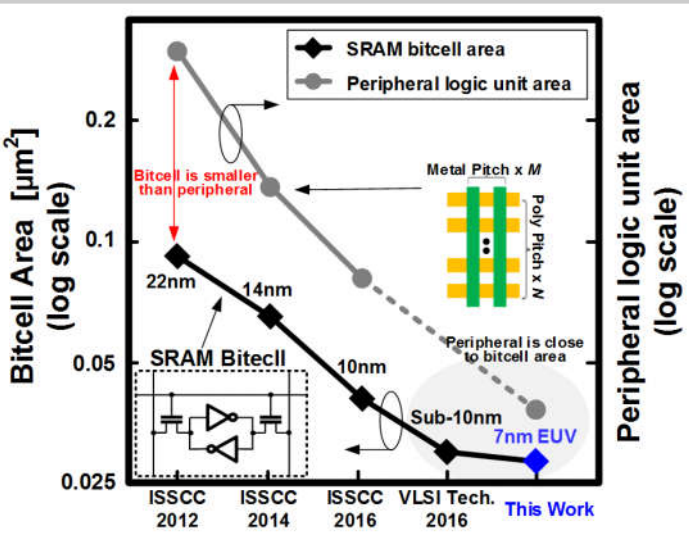

Figure 12.2.1: SRAM bitcell and peripheral logic unit area for different technology nodes.

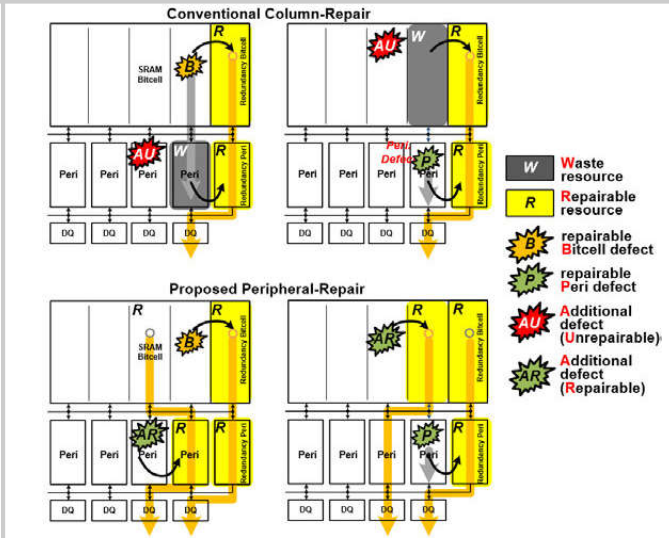

Figure 12.2.2: Conceptual behavior of the conventional column repair and the proposed peripheral repair.

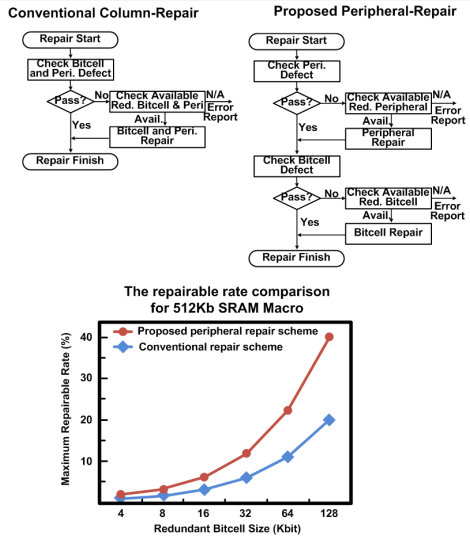

Figure 12.2.3: (a) Comparison of repair flow between the two schemes, and (b) a comparison of the maximum repairable rate.

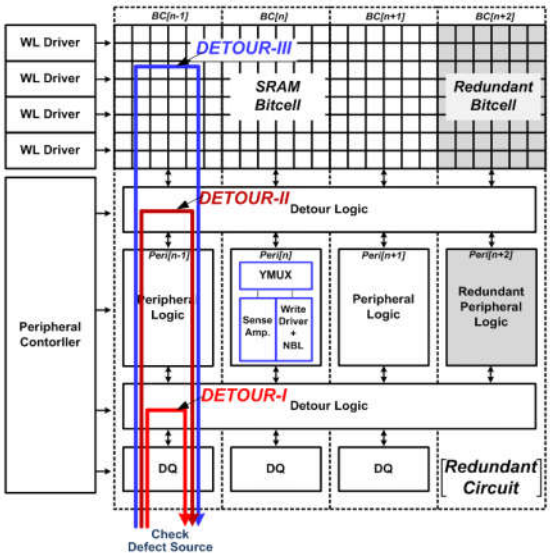

Figure 12.2.4: The SRAM test-chip for peripheral repair analysis.

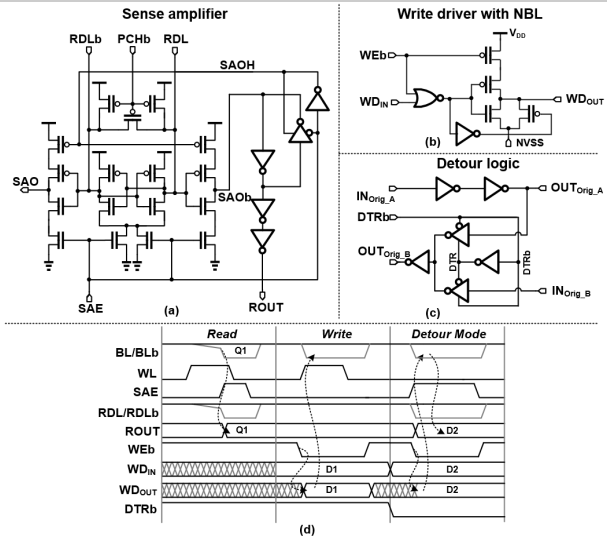

Figure 12.2.5: Circuits used: (a) sense amplifier, (b) write driver with NBL, and (c) detour logic. (d) timing diagram of the SRAM-chip.

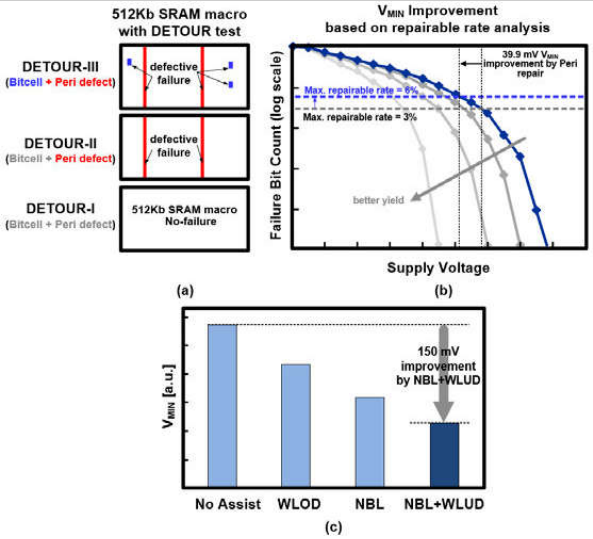

Figure 12.2.6: Silicon results: (a) DETOUR test, (b) V_{MIN} improvement with peripheral repair, and (c) V_{MIN} improvement with SRAM assists.

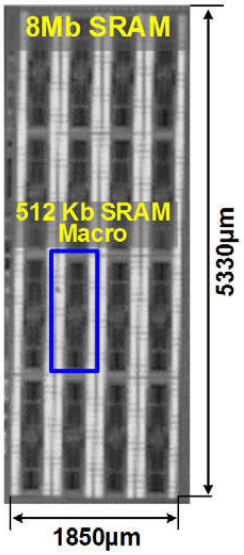

Figure 12.2.7: 7nm FinFET SRAM test-chip micrograph.

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