



Voltus-Fi EMIR Analysis Workshop

**Tool versions:
MMSIM131 ISR3
IC6.1.6 ISR6**

Voltus-Fi EMIR Analysis Workshop

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1. Introduction to Voltus-Fi EMIR Analysis Workshop

Welcome to Voltus-Fi EMIR Analysis Workshop. This workshop will take you through IR-drop and electromigration analysis flow utilizing our patent-pending technology in MMSIM (APS/XPS) followed by visualization of results in Virtuoso Layout Editor.

This workshop is designed to work with IC616 ISR6 and MMSIM131ISR3 or later. If you are interested in running LVS and extraction, then PVE121 and EXT131 are also required. There are no prerequisites for this workshop, although the ADE XL workshop is highly recommended. Some familiarity with physical design and the concepts of IR-drop and electromigration will be helpful.

In this section...

You will learn about the EMIR solver methods in MMSIM.

Voltus-Fi is new EMIR solution which comes integrated with the Spectre APS/XPS simulators for high capacity and accuracy, supporting electromigration for both power and signal nets along with IR-drop. This new dynamic power EMIR and signal EM capability uses a new patent pending technology, and is designed to provide very high capacity and performance. Within this flow, Spectre® APS can be used for high accuracy EMIR analyses; while Spectre® XPS can be deployed for high performance and high capacity EMIR simulation of memories. Voltus-Fi can provide a very well integrated visualization experience inside Virtuoso environment. Voltus-Fi EM engine is N20/N28 certified and supports all length and width based rules.

In an EMIR flow, a circuit is evaluated together with the parasitic resistor and capacitor network which models the IR drop and EM effect. The parasitic information comes from a transistor-level and unreduced DSPF or SPEF, which contains additional information about width, length, and XY coordinates of parasitic resistors. There are two general approaches in APS/XPS EMIR solution – Direct and Iterated.

Direct Mode

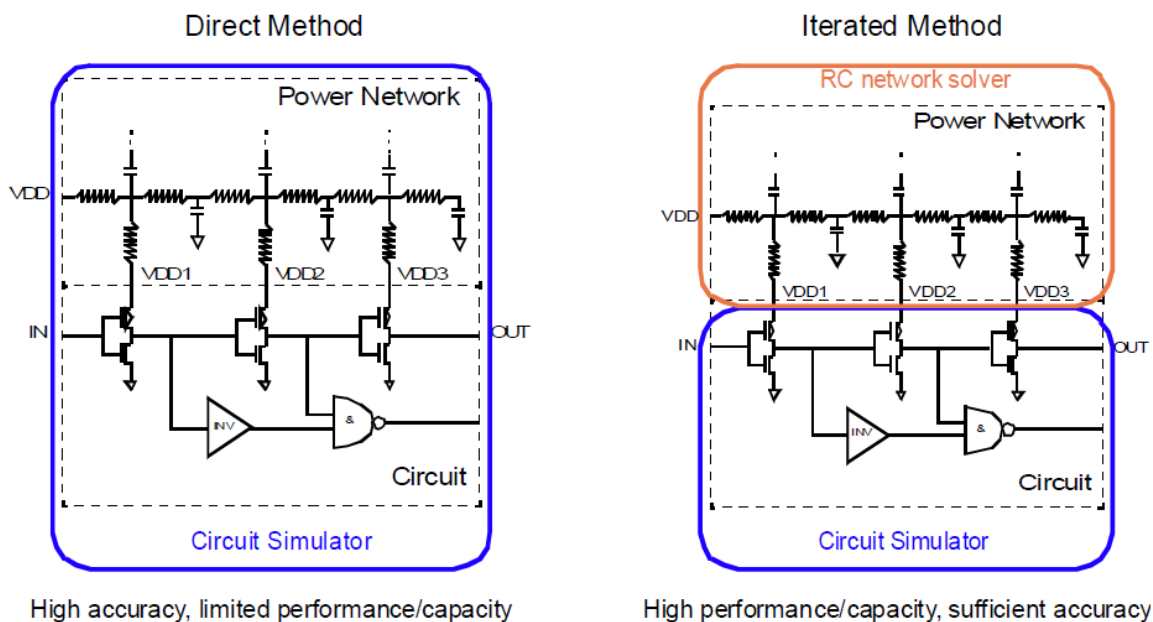
When high accuracy is required, flat simulation of the entire system - circuit and parasitic R's and C's – can be performed to accurately calculate EM/IR of any nets. This approach is often referred to as “one-step” or “direct” method, where the EMIR simulation performance and capacity is subject to the limitation of the circuit simulator being used. For high accuracy EMIR analysis of small design blocks, or designs with smaller numbers of RC nets, the direct EMIR analysis method is recommended.

Iterated Mode

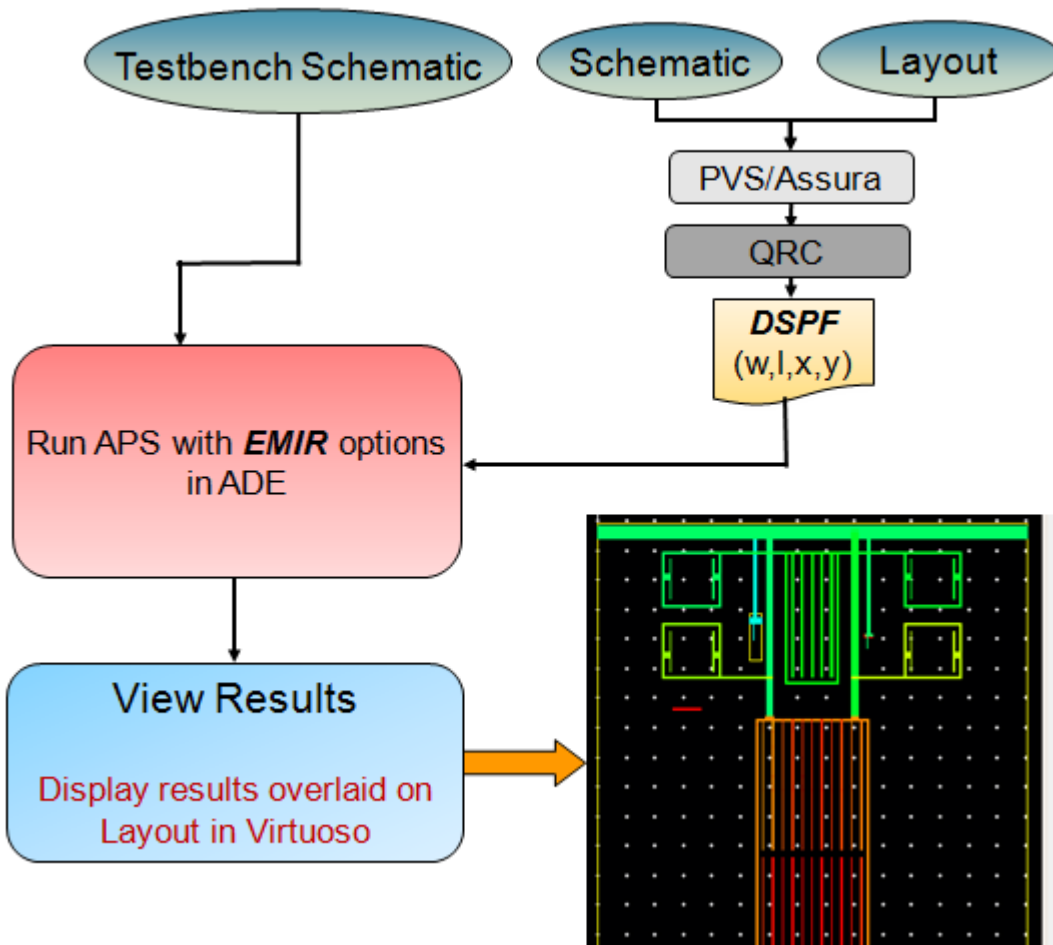
In order to conduct EMIR simulation on circuits with much larger power and signal nets in reasonable time, an alternative is to decouple the nonlinear circuit simulation from the linear RC net analysis. User can iterate over only the linear RC net analysis by modifying the layout, however the nonlinear circuit simulation may be done only once (the assumption is that the circuit doesn't change over iterations). This approach is often referenced as "two-step" or "iterated" method. The decoupling of the linear RC nets from the non-linear circuit is not mathematically equivalent to the original design and certain inaccuracy is introduced; however the user receives a significant benefit of simulation performance and capacity.

To gain higher performance and higher capacity on medium to large designs, the iterated EMIR analysis method is recommended. Both Spectre® APS and Spectre® XPS support the iterated EMIR analysis.

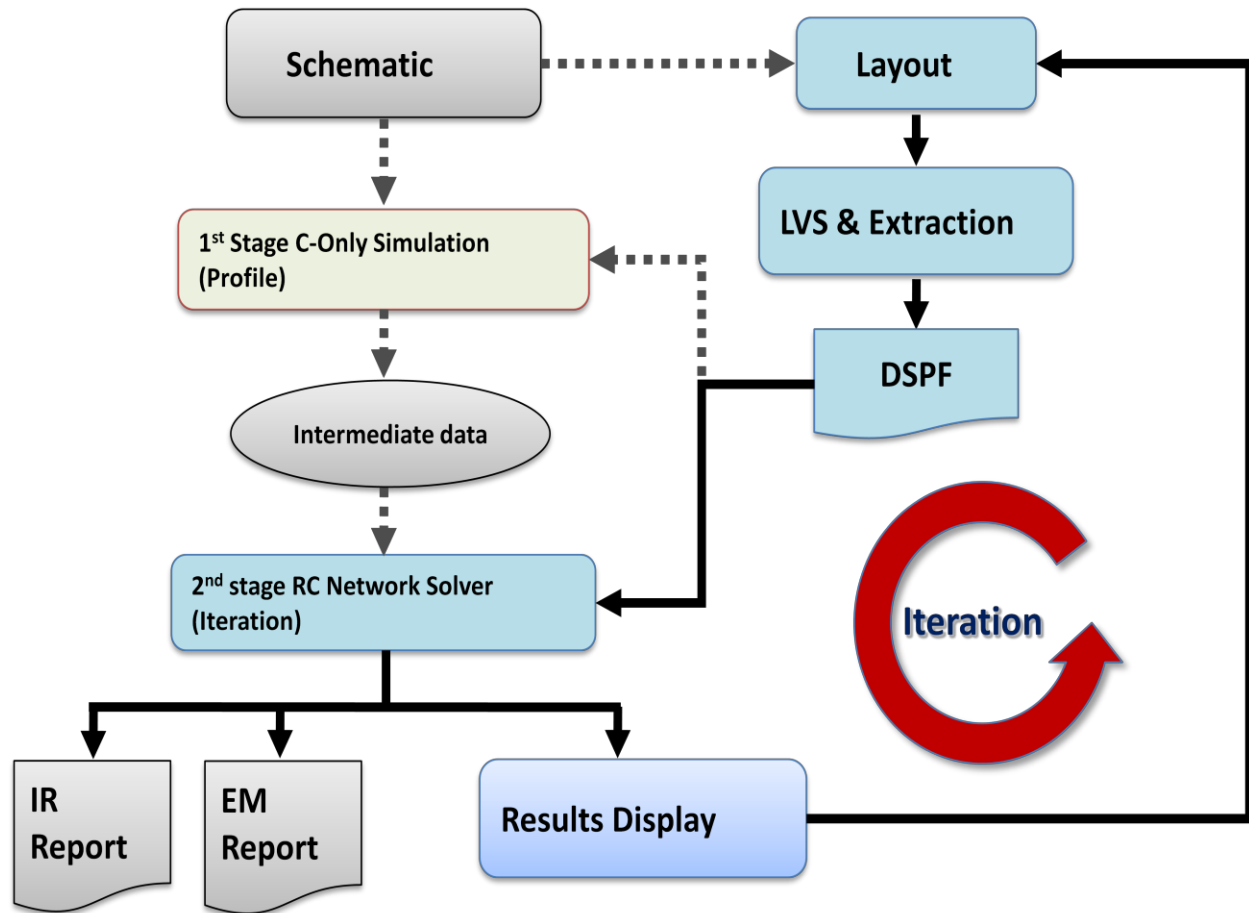
The snapshot below compares Direct and Iterated solving methods.



Voltus-Fi EMIR flow diagram is as below.



Voltus-Fi EMIR flow diagram for **Iterated** method looks as below.



2. Enabling EMIR in Analog Design Environment

In this section...

You will learn how to setup the EMIR flow in ADE-L/XL. For actions which relevant particularly to ADE-L and XL users, it has been clearly stated. You will start with looking at the testbench schematic and the nets to analyse.

Action 1: `tar xvzf VoltusFi_workshop.tar.gz`

Action 2: `cd VoltusFi_workshop`

Action 3: Open file 'sourceme' for editing. If your environment sets up all tool installations and licenses correctly, comment out lines 5 to 14 first, and then:

```
source sourceme
```

Else, update the paths for software installations in the same section, and then source the file.

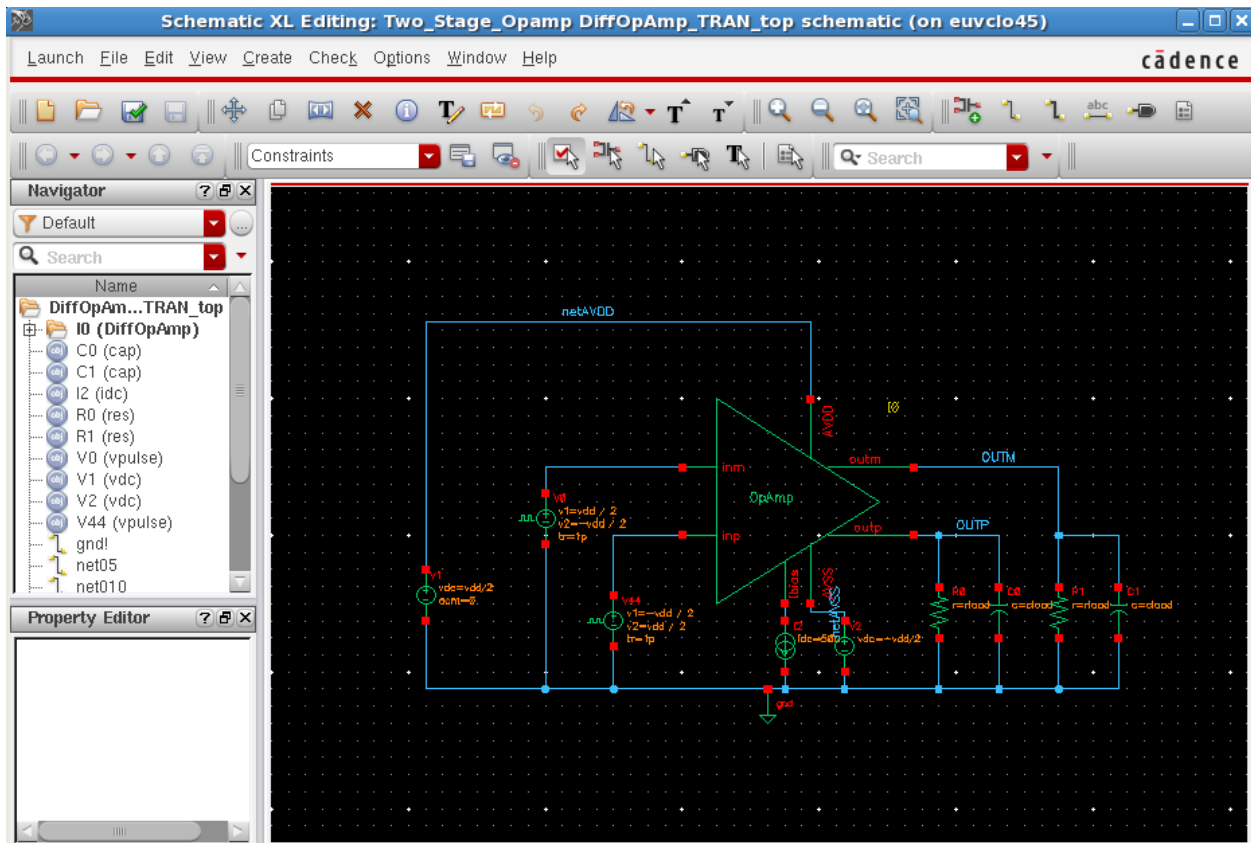
Action 4: `virtuoso &`

The CIW alongwith Library Manager will appear.

Action 5: In the Library Manager, select and open:

- Library: Two_Stage_Opamp
- Cell: DiffOpAmp_TRAN_top
- View: schematic

The testbench schematic can be seen below.



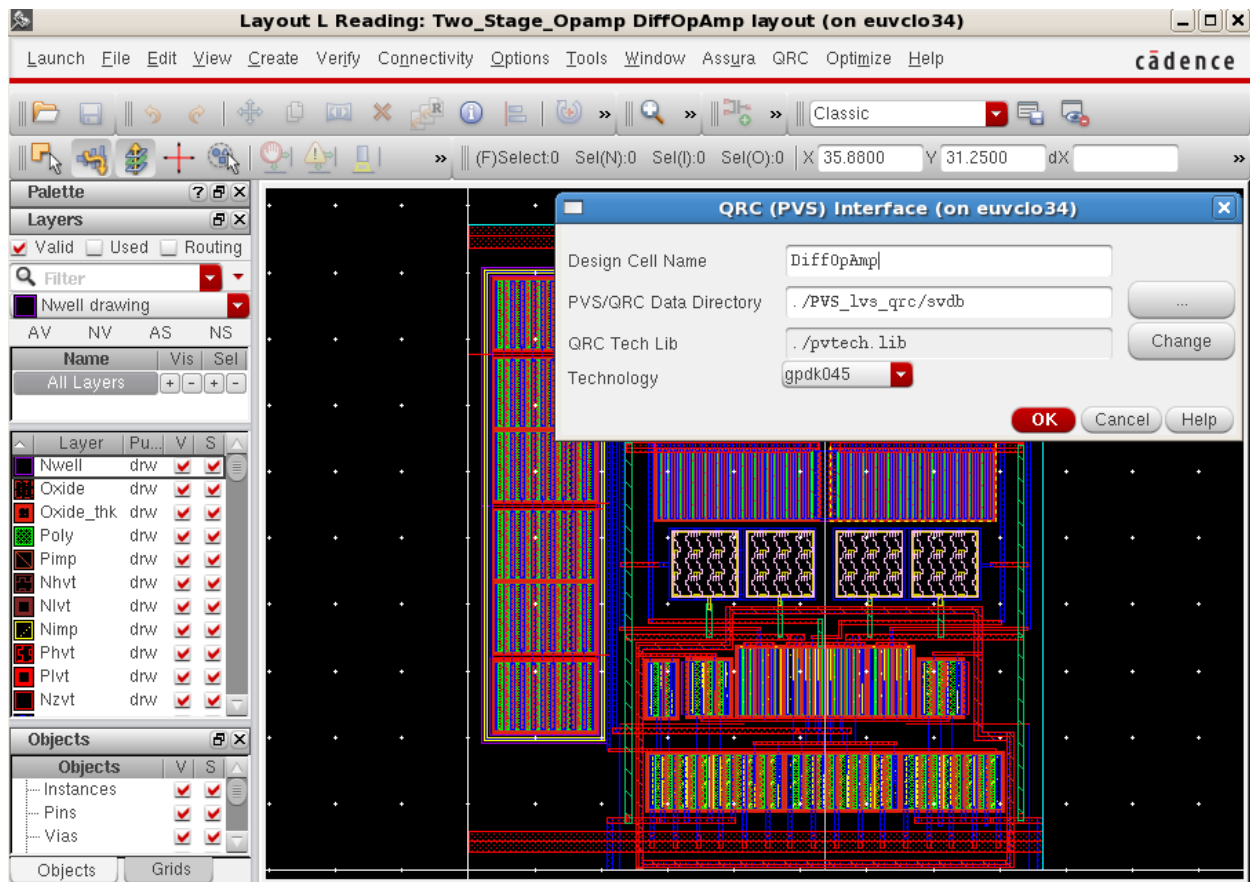
In this workshop, we will simulate and analyse for EMIR a differential op amp (instance name: I0). Descend into I0 schematic or layout to take a look at DUT implementation.

We will analyse supply net **AVDD** for IR-drop, and signal net **outm** for EM.

Action 6 (optional): Let's look at QRC setup for running extraction. You can choose to skip this step and directly use DSPF "DiffOpAmp.dspf" in the next step.

Open DUT layout and bring up QRC form through QRC -> Run PVS-QRC menu. LVS has already been run using PVS and the results are stored in directory 'PVS_lvs_qrc'.

- Library: Two_Stage_Opamp
- Cell: DiffOpAmp
- View: layout



Once QRC form comes up, load state “**EMIR**”. This should set the required options for running EMIR flow. Pay close attention to ‘Netlisting’ tab. Make sure your setup matches the snapshot below to generate a good DSPF required for EMIR analysis. This includes:

- Metal layer information for parasitic resistors
- Width of parasitic resistors
- Length of parasitic resistors
- X,Y coordinates of parasitic resistors
- Vias to be netlisted explicitly (and not merged with metal layers)
- Avoid false EM violations being flagged for stack vias

The setup shown below addresses all of the above.

QRC (PVS) Parasitic Extraction Run Form (on euvclo45)

Setup Extraction Filtering **Netlisting** Run Details Substrate

Design Resistor Models: Do Not Include

Parasitic Resistor Models: Include As Comment

Netlist With Names From: Schematic EM Analysis: ☐

Enable Virtual Metal Fill: ☐ Fine Shape: ☒ Save Fill Shapes: ☐

Sub Node Character: # Bus Bit: []

Hierarchy Delimiter: / Device Finger Delimiter: @

Import Globals: ☐ Force Globals: ☐

Parasitic Resistance Width: Silicon Parasitic Resistance Length: ☒

Parasitic Resistance Temperature Coefficient: ☐

XY Coordinates: R ☐ C ☐ r ☒ c ☐ D ☐ M ☐ Q ☐ X ☐

Ignore Vias: Layers: Nets:

Auto Substrate Stamping Off: ☐

Add Explicit Vias: ☒

Via Effect Off: ☐

Gate Diffusion Fringing Cap Off: ☐

Instance Off: ☐

Netlist Coupling Values: Single

Layer Name Printing: ☐

Stacked Via Metal Width: EM

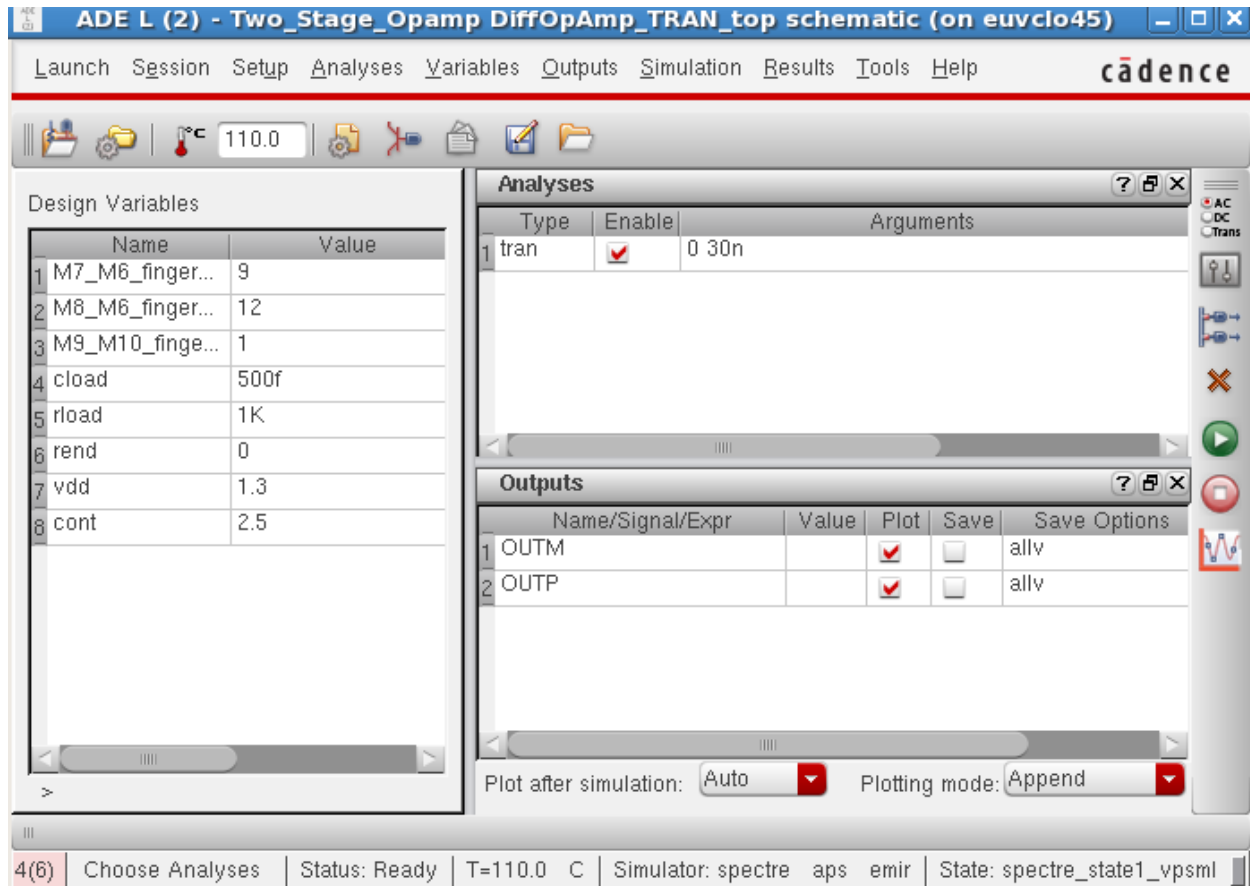
If you hit 'OK' button on QRC form, it should (re) generate a DSPF for the DUT. You can use your new DSPF, or the original one included in the workshop in subsequent steps (as mentioned earlier).

DSPF file 'DiffOpAmp.dspf.golden' has been provided as a back-up in case you overwrite DiffOpAmp.dspf and wish to retrieve it.

Action 7a (for ADE-L users): Open the testbench schematic:

- Library: Two_Stage_Opamp
- Cell: DiffOpAmp_TRAN_top
- View: schematic

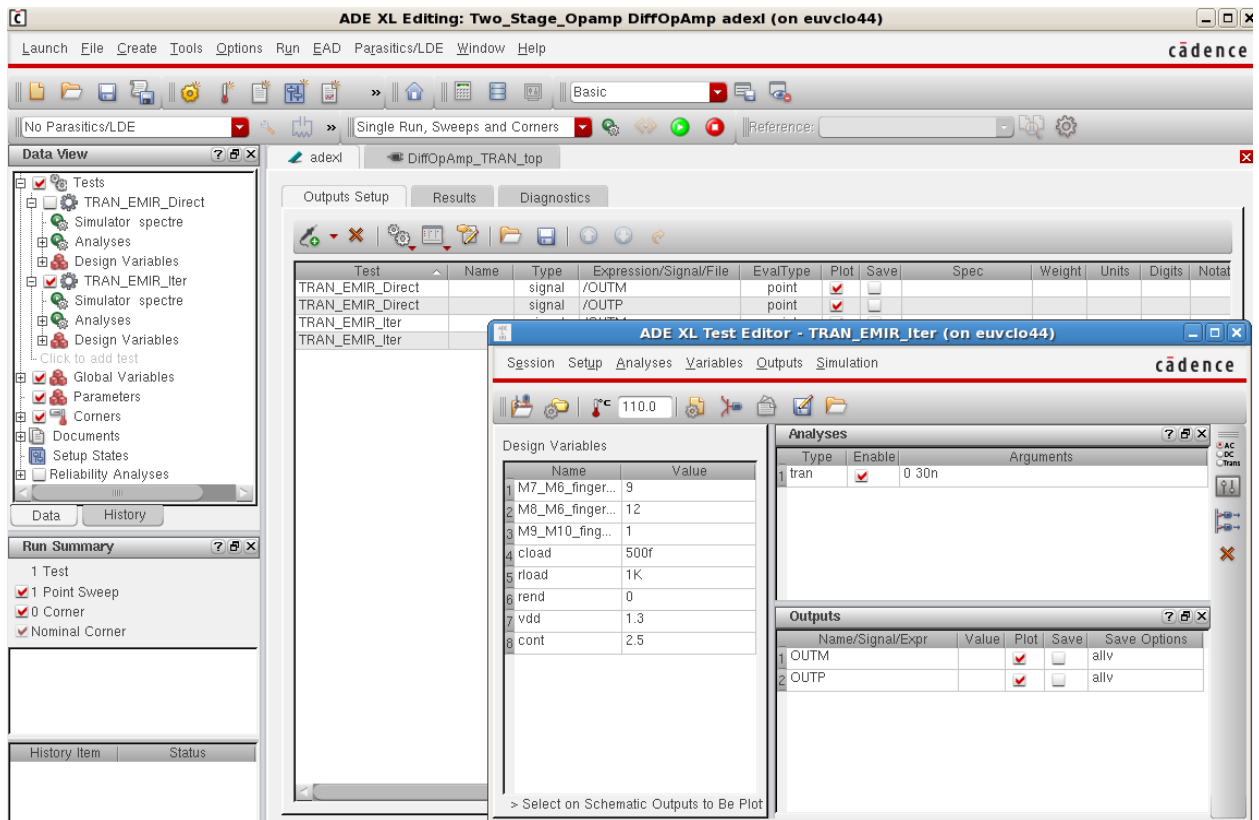
Launch ADE L from schematic and load state '**spectre_state1_emir**' from cellview. There is another state '**spectre_state1_emir_direct**' provided for reference EMIR setup using Direct solver method.



Action 7b (for ADEXL users): Open 'adexl' view for DUT

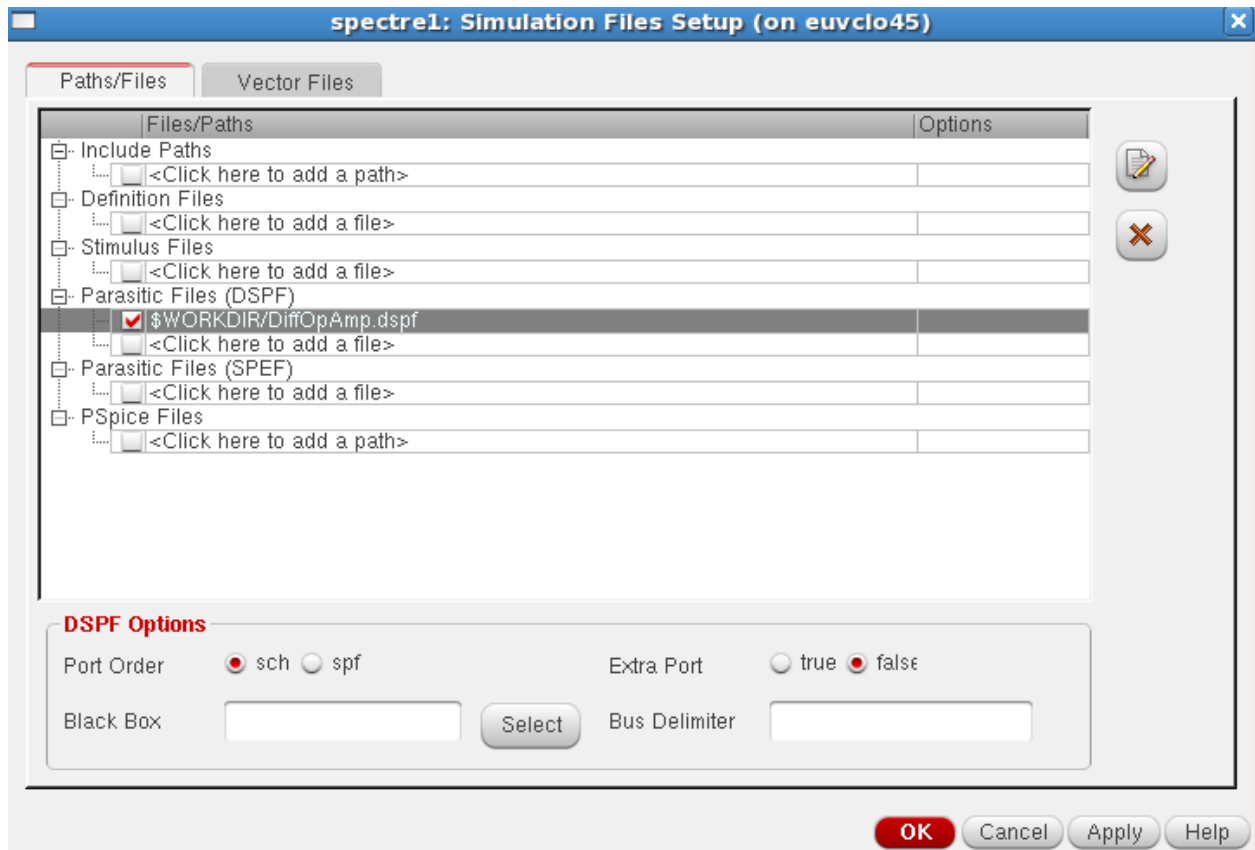
- Library: Two_Stage_Opamp
- Cell: DiffOpAmp
- View: adexl

Double-click on the test '**TRAN_EMIR_iter**' to open ADE XL test editor as shown below. Test '**TRAN_EMIR_Direct**' (disabled) has been created in adexl view for reference EMIR setup.



Action 8: Enable the EMIR related options mentioned as below (For ADE-XL users, these menus are available through <testname> -> RMB as well).

- Setup -> High-Performance Simulation
 - Enable **APS**
- Setup -> Simulation Files
 - This option has new fields to include the DUT DSPF or SPEF (snapshot below). Point to your parasitic file here (the path doesn't have to use any environment variable).



- Setup -> EM/IR Analysis
 - A form will pop-up allowing you to specify EMIR options

The EM/IR Analysis Setup form will come up as below for a **new** state/test. You will see the complete path to your EM rule file without involving variable \$WORKDIR.

The workshop uses file 'emDataFile.txt' for EM analysis. You can also explore the use of ICT file or qrcTechFile formats instead if you wish to. An example ICT file with EM rules can be found at the location below:

- ./pvs_qrc_decks/qrc/typical/ictfile

spectre2: EM/IR Analysis Setup (on euvclo45)

Net Selection

Net Name:

Select

Clear

Analysis:

☐ imax
☐ iavg
☐ irms
☐ iavgabs
☐ vmax
☐ vavg

Advanced Analysis:

☐ Signal Net IR Drop
☐ Power Gate

Add

Time Window Setup

Start

Stop

0

30n

×

☒ Full Transient
☐ Time Window

Add

Emirutil Setup

EM Tech File

\$WORKDIR/emDataFile.txt

...

Advanced Option:

autorun

▼

☒ true
☐ false

i

Additional Option:
Additional Value:

Add

Solver Method

☒ auto
☐ direct
☐ iterated
☐ profonly
☐ iteronly

Speed

default

▼

inputwvf

...

Add

DSPF File Checking

DSPF File

\$WORKDIR/DiffOpAmp.dspf

...

Run

Summary Information

Options	Value

Import

Export

Below is a brief description of each section of the form:

- Net Selection → Specify the nets to be analysed in the schematic, choose one or more analysis, and then click 'Add'. You will find the Summary Information

section at the bottom gets populated. A pink info-balloon is displayed when you hover over Net Name field to aid the users to select nets for analysis.

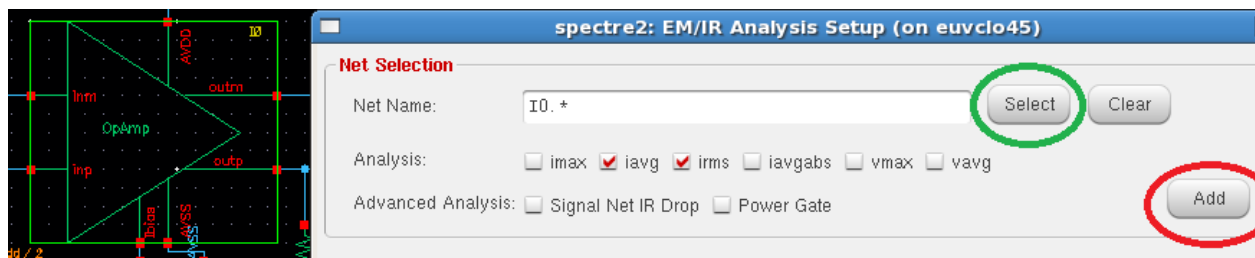
- Time Window Setup -> By default, for a transient analysis, EMIR analysis is run for the entire simulation period. You can choose to provide a different time window by enabling "Time window" and adding the new start/stop times (and click 'Add').
- Emirutil Setup -> EM Tech File field is populated automatically by setting an environment variable EMTECHFILE before launching Virtuoso. EM rules can be in any of the 3 supported formats – emDataFile, ICT file or qrcTechFile. Apart from EM file, there is a list of advanced options to choose from alongwith a value as required.
- Solver Method -> The default EMIR method is Auto (Direct), and different methods like iterated, profonly, iteronly can be selected as needed. Method "iteronly" is particularly relevant if the first EMIR simulation was run using iterated, and then the layout was modified to address any violations. The next simulation will benefit from using 'iteronly' because it will solve only the R/RC parasitics again, but not the circuit, thereby saving significant time.
- DSPF File Checking -> The DSPF file included through Simulation files is automatically populated in this field. Clicking 'Run' will invoke spfchecker which checks the syntax of the DSPF/SPEF followed by opening spfchecker output log. Spfchecker also compares the terminal names in DSPF and device models and populates the Summary Section with spf alias term statements.
- Summary Information -> This section contains the final set of commands that will be used by APS for performing EMIR analysis.
- The checkbox at the bottom of the form indicates that EMIR analysis has been enabled.

Action 9: Now, let's see how you enter the required options in the form.

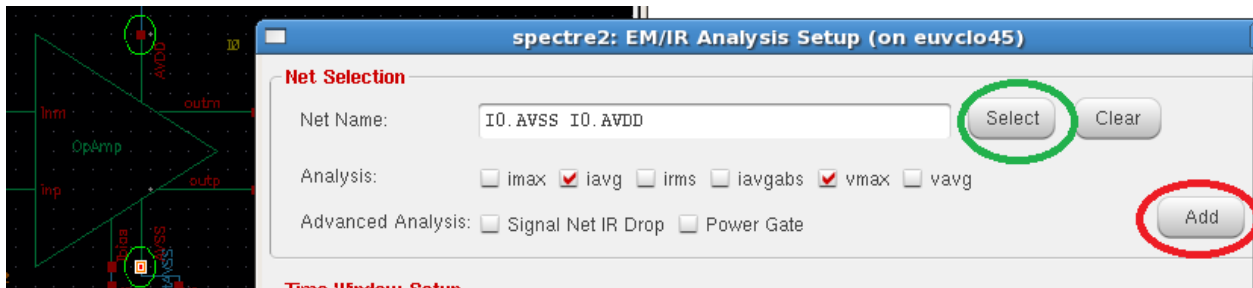
Net Selection

Press 'Select', this should bring up the testbench schematic prompting you to select the nets for analysis.

- To analyse all nets in the block for EM, select the instance, choose analysis and click 'Add'.

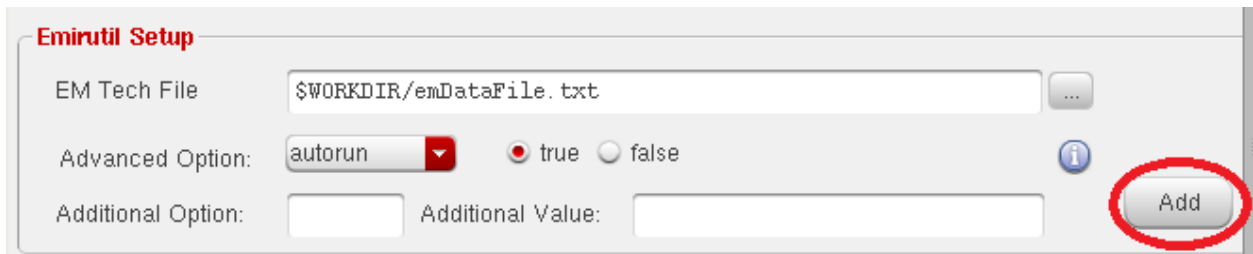


- Press 'Clear' to remove the net names
- To analyse a particular supply/ground net for IR-drop and/or EM, select the instance port(s) in testbench schematic



Emirutil Setup

- Path to EM rule will be automatically populated if EMTECHFILE variable is defined. You can point to a different EM rule file if required in this field.
- Explore the 'Advanced Option' to see if any settings apply to your design. More details can be found about these options in Spectre/APS user Guide under 'EMIR Analysis'.
- Remember to press 'Add' to include the EM rule file and any other options you may have selected



Solver Method

- Select 'iterated' method and press Add. The ADE L or XL reference setups included in workshop use method 'direct' or 'auto'.



DSPF File Checking

- When you click 'Run', a utility called 'spfchecker' is invoked in batch-mode to parse the DSPF. A log file will come up after spfchecker run has completed.

DSPF File Checking

DSPF File

 ...

Run

Summary Information

- The summary section should look as below. The options visible here will be translated into a file called emir.conf, and passed on to APS during simulation.

Summary Information

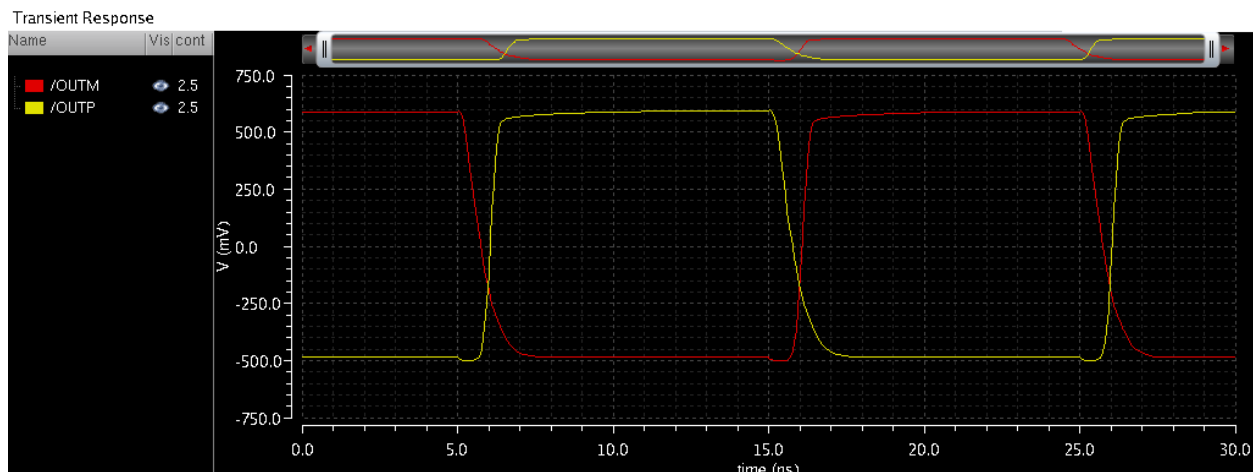
Options	Value
net	name=[I0.] analysis=[iavg irms]
net	name=[I0.AVSS I0.AVDD] analysis=[iavg vmax]
emirutil	techfile=\$WORKDIR/emDataFile.txt
emirutil	autorun=[true]
solver	method=[iterated]
spf	aliasterm = "capacitor 1=PLUS 2=MINUS"
spf	aliasterm = "g45n2svt 1=d 2=g 3=s"
spf	aliasterm = "g45p2svt 1=d 2=g 3=s"

Import
 Export
 Delete
 Clear

☒ Enable EMIR Analysis in Transient or DC Simulation

Press OK on the form and your EMIR setup is ready.

Action 10: Run the simulation, the simulation output should look as below.



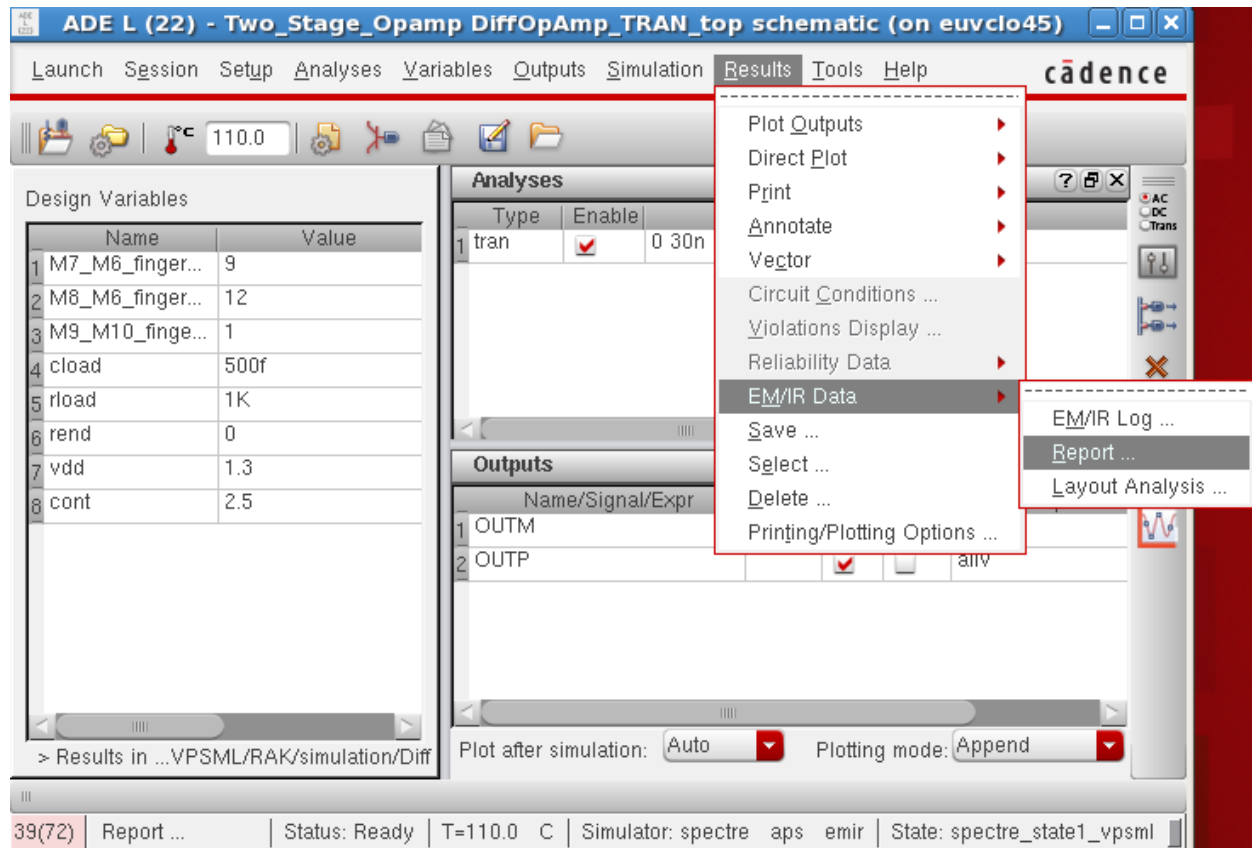
3. Analysing EMIR analysis outputs

In this section...

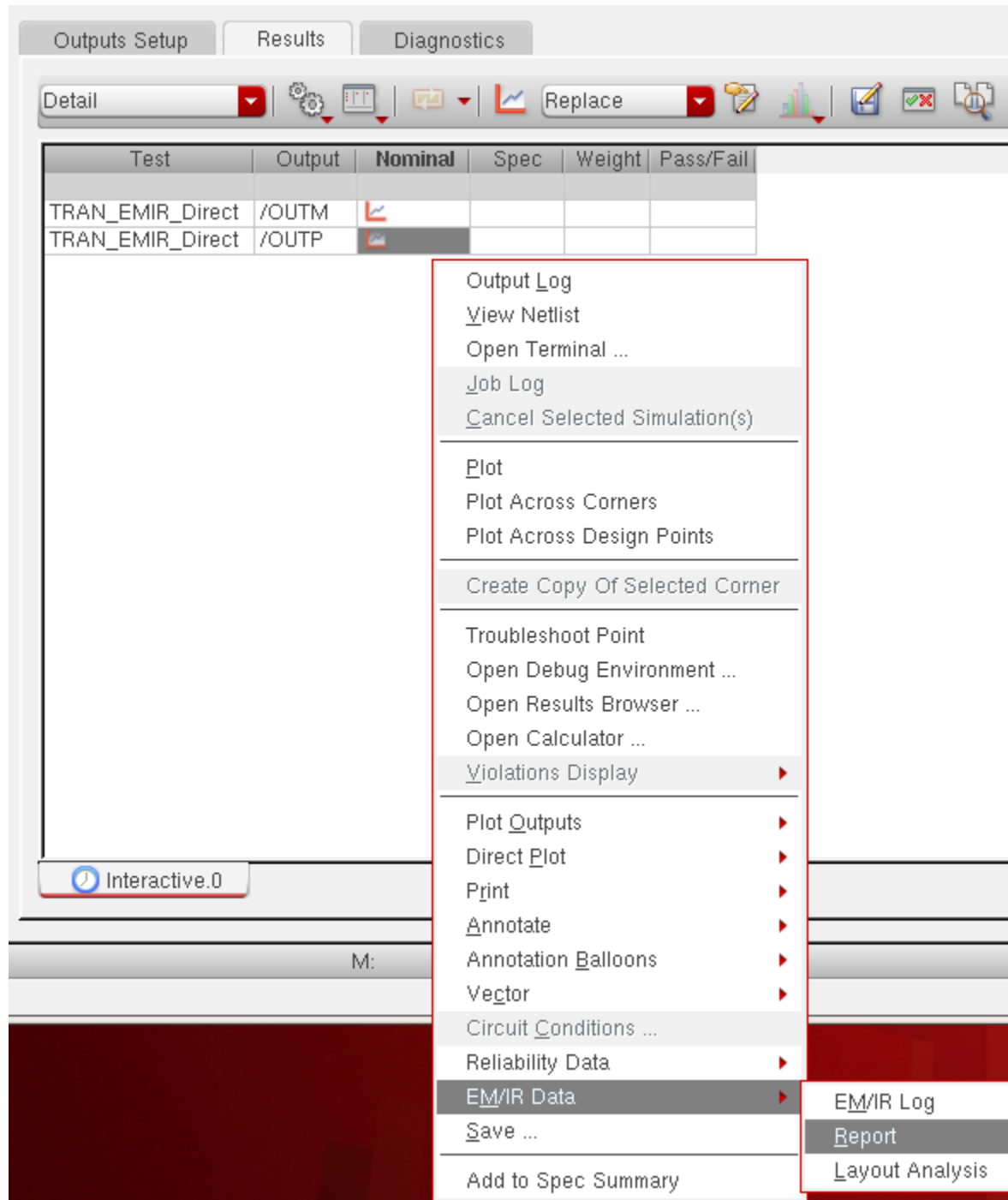
We analyse the different kinds of outputs of EMIR analysis i.e. output log, text and HTML reports, and finally the visualization of results overlaid on DUT layout.

Action 1: Explore the new menu called EM/IR Data added to view EMIR results.

For ADE-L users, this can be found as below.



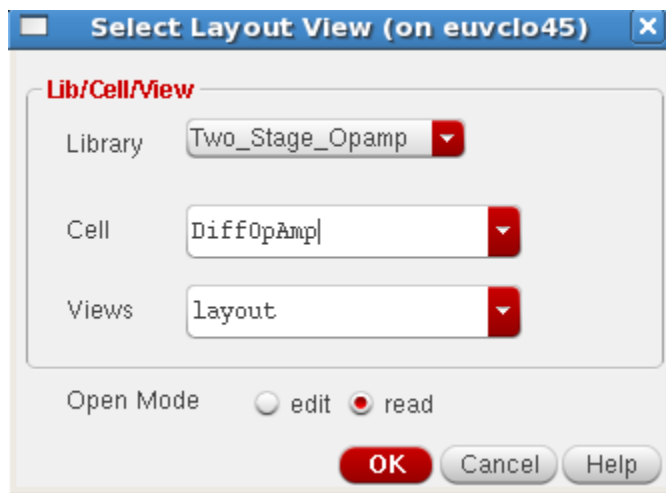
For ADE-XL users, the option is available through Results tab.



Action 2: Investigate EM/IR reports by selecting EM/IR Data -> Report. From the pop-up that follows, you can choose to view IR-drop reports (input.*.rpt_ir) and EM reports (input.*.rpt_em) in text or HTML formats. 'mozilla' browser will be invoked automatically (if found in the user's setup) to display the HTML reports.

Action 3: Prepare for visualizing the results in Layout Editor by selecting EM/IR Data -> Layout Analysis

A pop-up will come up prompting you to choose the DUT Layout view being analysed. This should be the same view for which you ran LVS and extraction to generate a DSPF. We auto-detect the DUT based on EMIR setup, but you may have to choose the correct view name if the block had multiple layout views.

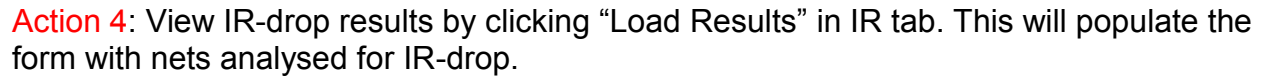


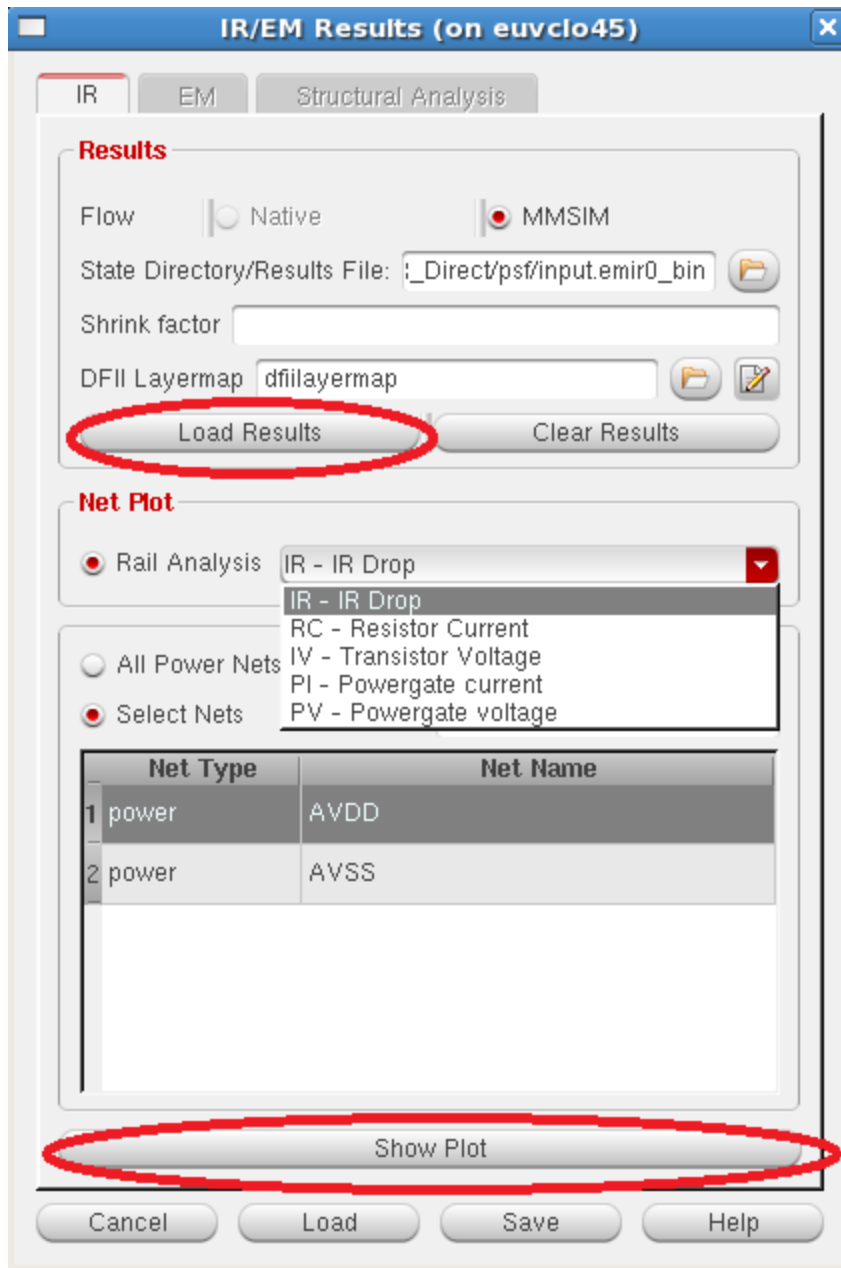
Pressing OK will open up the layout alongwith a form titled "**IR/EM Results**". The form contains three tabs called IR, EM and Structural Analysis.

A few fields are automatically populated in IR and EM tabs.

- State Directory/Results File: Points to the simulation results generated by APS.
- DFII Layermap: Points to a text file called "dfiilayermap" included in workshop. This file maps the extraction layer names in DSPF to DFII layer names.
- Tech File (EM tab only): Points to the EM rule file specified in ADE setup

See a snapshot of the form below.





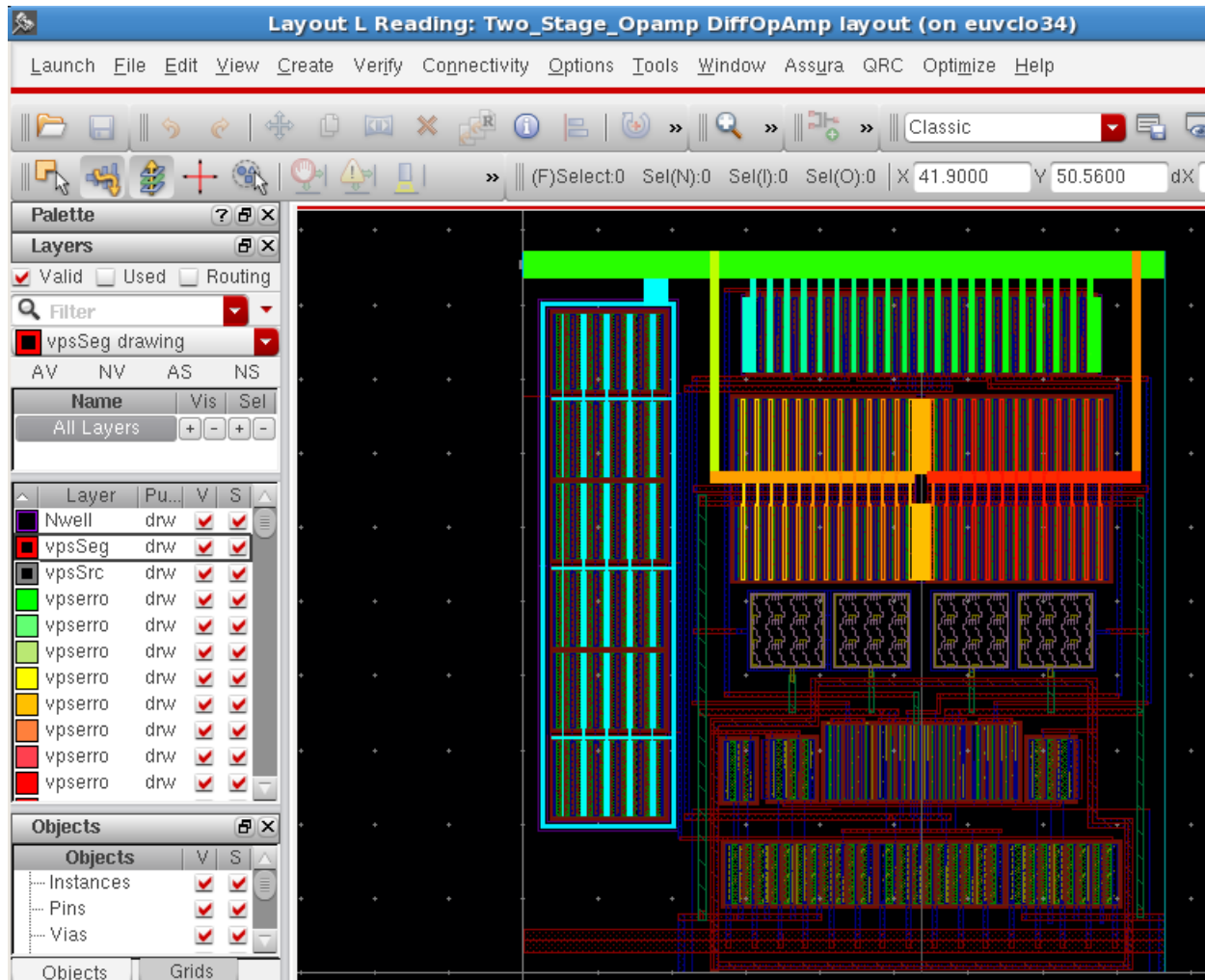
You can now select any net, alongwith Rail Analysis (plot types) as shown in the drop-down list.

Available plot types are:

- IR - This is an IR analysis plot (this is the default plot type)
- RC - This is resistor current plot showing how the current is flowing in the grid
- IV - This is transistor voltage plot showing the drop on the nodes connecting to devices
- PI - Power gate current plot
- PV - Voltage drop across power gates plot

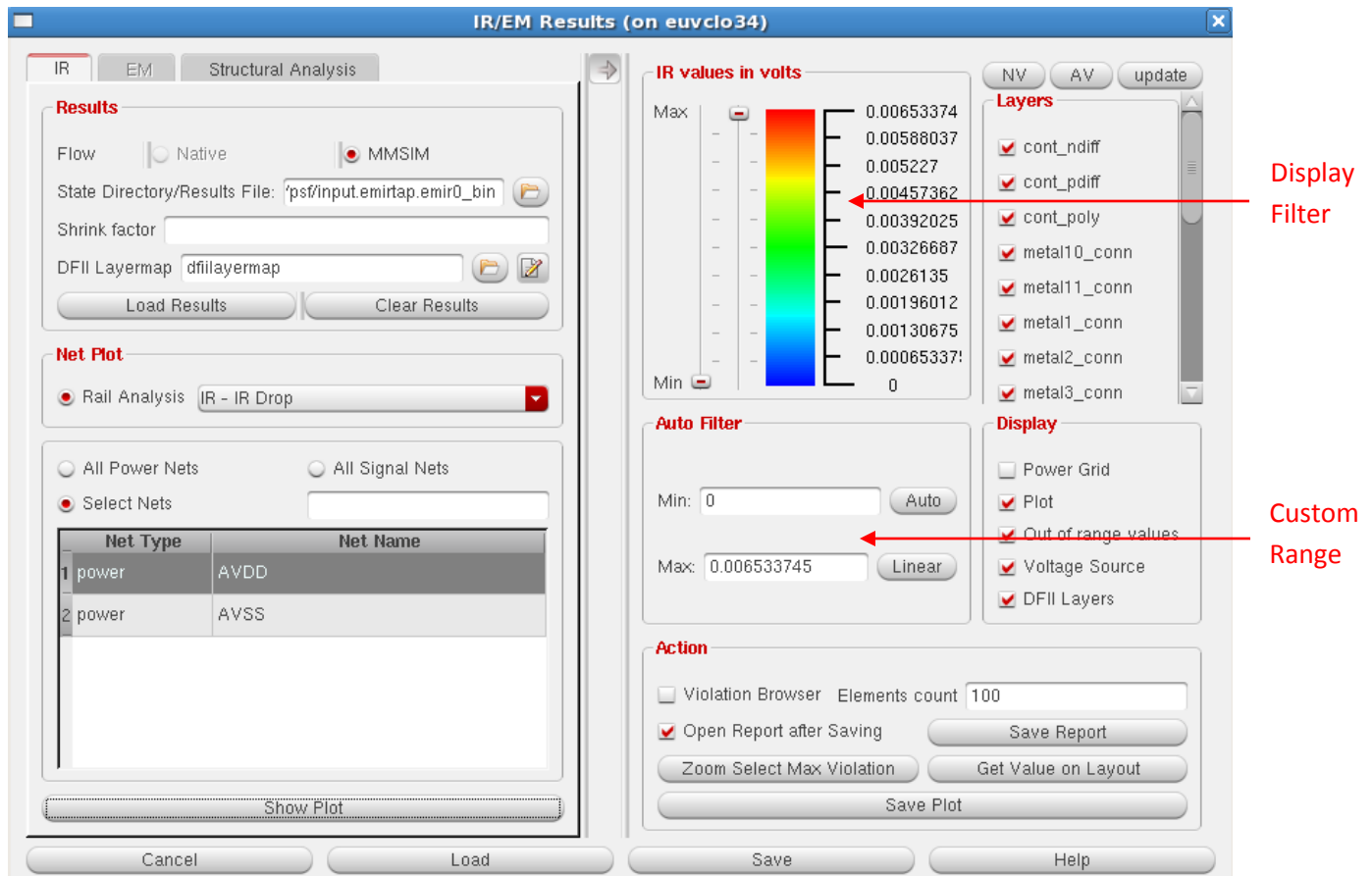
Select IR plot and power net AVDD from the net selection browser, and click on “Show Plot”.

This will overlay the plot on top of the layout as below (you may want to enable dimming in Layout Options -> Display to see the highlighting better).



At the same time, you will find more details in IR/EM Results form as a new form section is appended to its right.

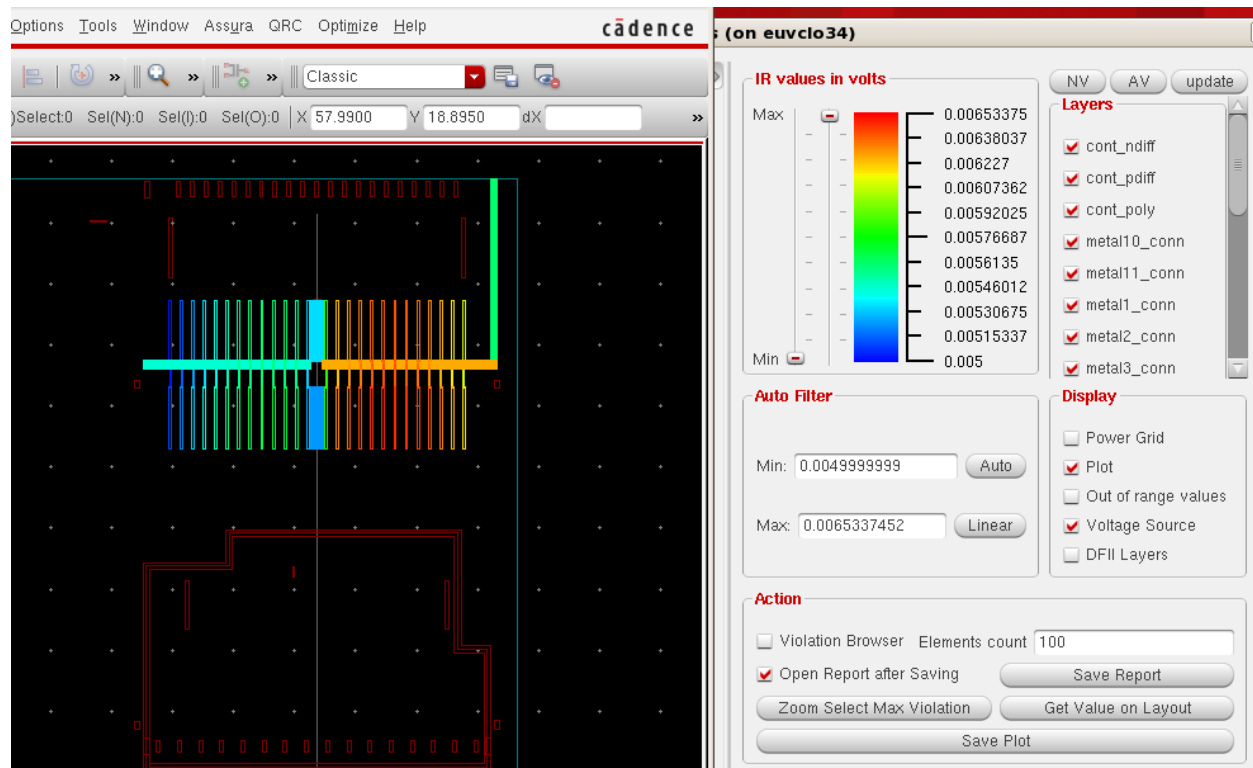
The worst drop on supply net AVDD is around 6.5mV – there will be a slight difference in results based on the solver method you chose while running APS (direct or iterated).



The important fields/features of the IR/EM Results form are:

- You can select to show plot of one net/all power nets/all signal nets or selected nets.
- The display filters are continuous filters; you can move the **Min** and **Max** sliders up or down to change the range of IR-drop being shown in the layout. Values lying outside the filter range will take deep blue or deep red color depending on which side of range it is.
- You can also write the custom range in **Auto Filter** field, and press 'Linear'.
- You can toggle displaying of out of range values, voltage sources, color Plot and DFII layers under '**Display**' settings.
- You can customize the results layers to view in Layout Editor from '**Layers**' section.

Try to display results with drop > 0.005V showing only the violations within range and no DFII layers. Layout Editor display will look as below (the plot below corresponds to *Iterated* method).



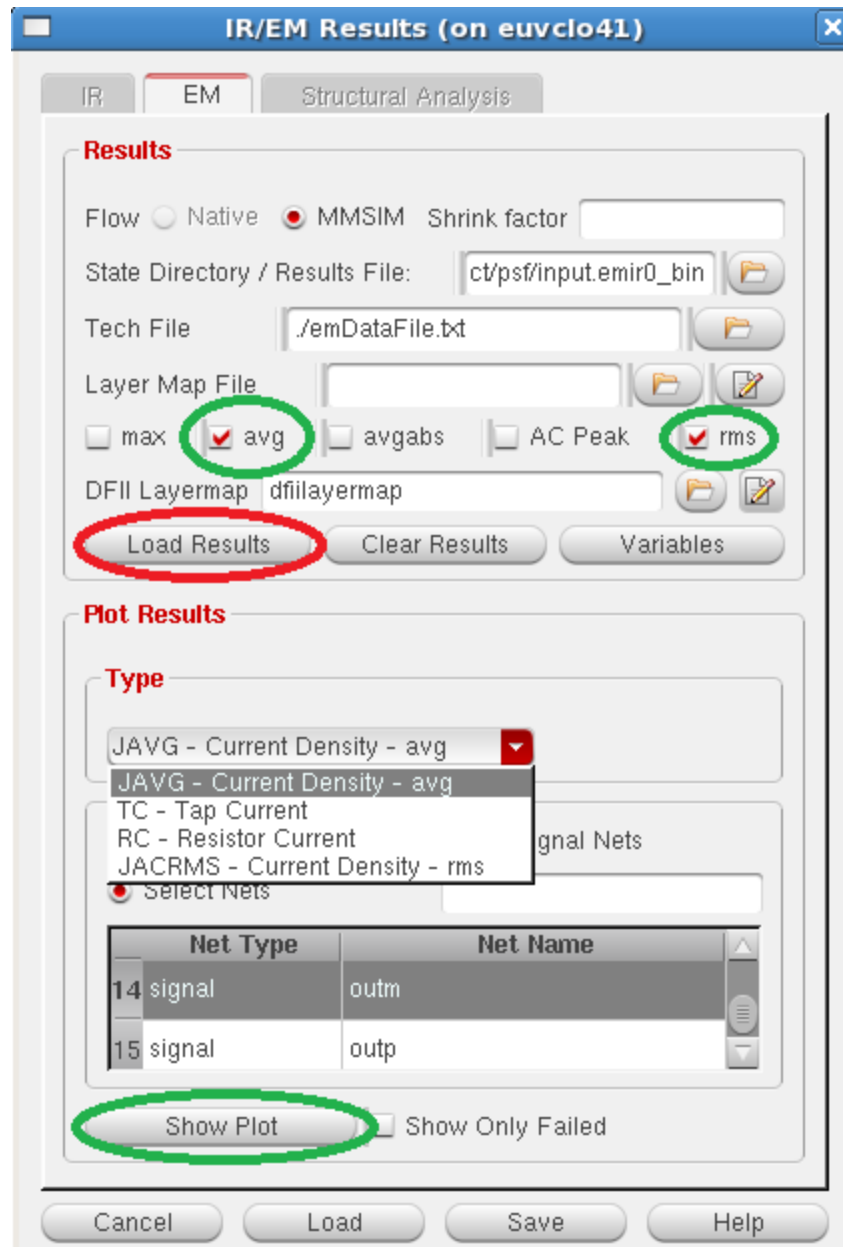
Action 5: We will now perform EM analysis. First, press “Clear Results” on IR tab, and then switch to EM.

Choose analysis names – avg, and rms, and click ‘Load Results’.

The new browser below is populated with all the nets analysed for EM.

Under **Plot Results**, you will see different types of plots to choose from:

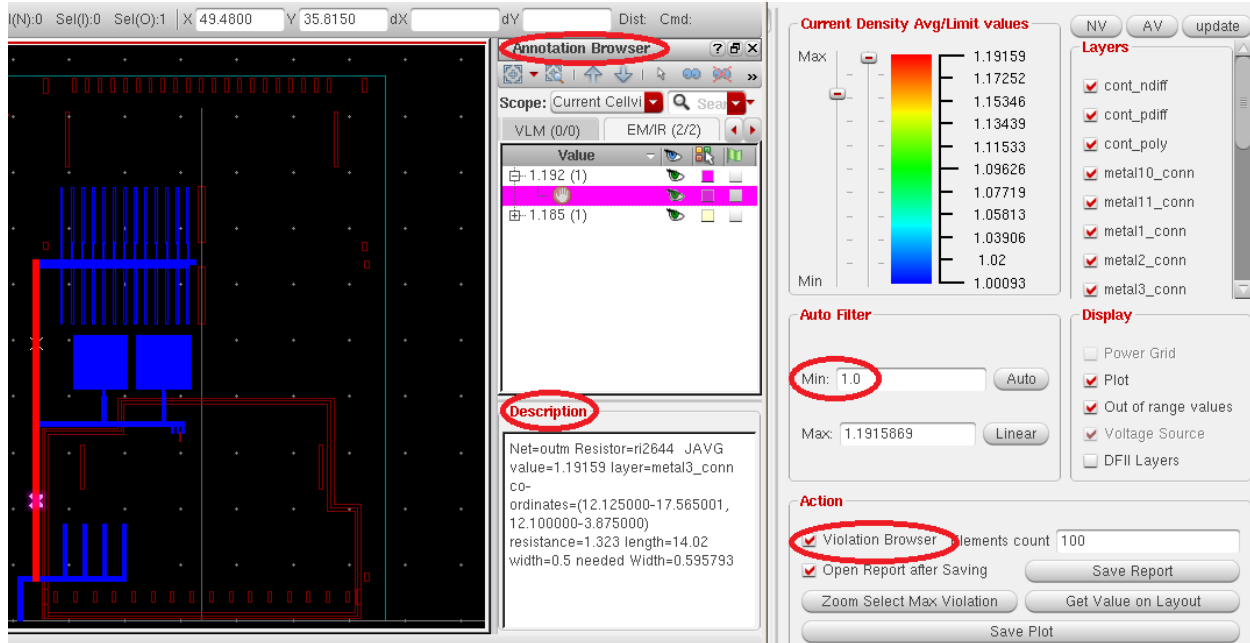
- JAVG - Plot showing average EM results (default)
- TC – Plot showing current flowing through net taps i.e. connected device terminals.
- RC – Plot showing current flowing through resistor segments
- JRMS – Plot showing RMS EM results



Let's look at JAVG EM results of signal net '**outm**' by choosing the net and clicking 'Show Plot'.

We will now explore another feature of the GUI by enabling "**Violation Browser**" in results form (see it highlighted below). This brings up a docked **Annotation Browser** assistant in Layout Editor with the top 100 EM results. This feature works in IR analysis as well.

The EM plot shows a ratio of (actual current density) to (allowed density limit) as defined in EM rule file. Therefore, a ratio ≥ 1 implies an EM failure. Move the Min slider value to 1 so that you see only the actual violations in Annotation Browser.



When you select a particular violation in Annotation Browser, the Description section below provides details about the violation e.g. layer, needed width.

In Annotation Browser, you can customize violation display by RMB -> View By, and then choose from the drop-down menu options.

More features

It is also possible to query the layout and back-annotate the corresponding violation(s) in Annotation Browser. There are two buttons in the form to help you achieve the same:

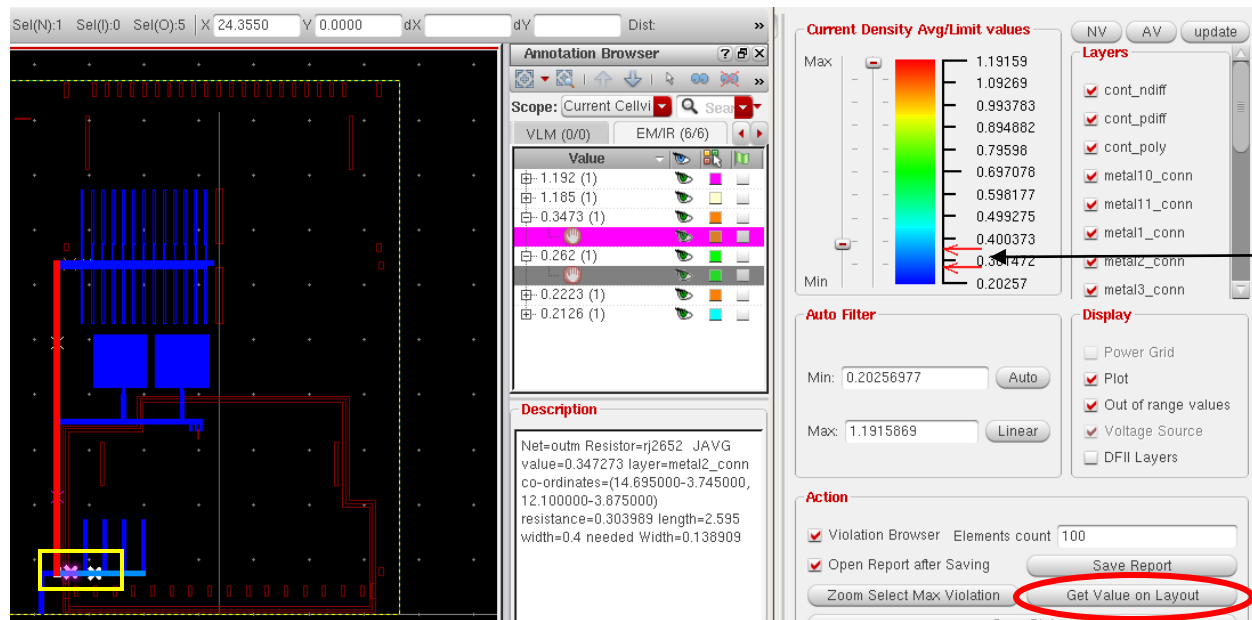
- Zoom Select Max Violation
- Get Value on Layout

Let's set the Min filter value to ~0.2 to bring more violations in Annotation Browser.

Now, if you click '**Get Value on Layout**', you will be prompted to draw a selection box in the layout. Once you draw the bbox, the violations enclosed in your box will be highlighted in the Annotation Browser (AB). You will also find that arrows are added in the Display Filter range to indicate the values of the violations highlighted in AB.

The figure below shows the selection box created in the layout and the corresponding violations in AB.

Voltus-Fi EMIR Analysis



Arrows
in
display
filter

'Zoom Select Max Violation' works in the same way, where once you create the selection box, Layout editor will zoom into the maximum violation found in the selected region. The same violation will be selected in AB.

This concludes this workshop. We encourage you to explore the different tool features, and contact Cadence support for any queries.

THANK YOU !