

Ver	Eff_Date	ECN No.	Author	Change Description
1.0_2	09-11-18	E120201833058	S. Y. Huang (PDS)	Please refer to Appendix A.4 Revision History for the update
1.0_1	06-15-18	E120201824108	S. Y. Huang (PDS)	Please refer to Appendix A.3 Revision History for the update
1.0	06-12-18	E120201818059	S. Y. Huang (PDS)	Please refer to Appendix A.2 Revision History for the update
0.9	01-08-18	E120201743169	M. Y. Lin (N7TDCP)	Please refer to Appendix A.1 Revision History for the update
0.5	07-21-17	E120201718234	M. Y. Lin (N7TDCP)	Original
Approvals:				Title
Please refer EDW workflow to see detail approval records				TSMC 7 NM CMOS LOGIC FINFET PLUS (N7+) DESIGN RULES
				Document No. : T-N07-CL-DR-022
				Contents : 1153
				Attach. : 0
				Total : 1153

* * * TSMC * * *

TSMC 7 NM CMOS LOGIC FINFET PLUS (N7+) DESIGN RULES

TSMC 7 NM CMOS LOGIC FINFET PLUS (N7+) DESIGN RULES

Distribution of this design rule is restricted. This document is TSMC Confidential. Do Not Copy. This document may not be copied or transferred to anyone without permission from TSMC.

Table of Contents

1 INTRODUCTION	7
1.1 OVERVIEW.....	7
1.2 REFERENCE DOCUMENTATION.....	7
2 TECHNOLOGY OVERVIEW	9
2.1 SEMICONDUCTOR PROCESS	9
2.1.1 Back-End Features.....	9
2.1.2 Front-End Features	10
2.2 DEVICES.....	11
2.3 POWER SUPPLY AND OPERATION TEMPERATURE RANGES.....	12
2.4 CROSS-SECTION	13
2.5 METALLIZATION INFORMATION	14
3 GENERAL LAYOUT INFORMATION	17
3.1 MASK INFORMATION, KEY PROCESS SEQUENCE, AND CAD LAYERS.....	17
3.2 METAL/VIA CAD LAYER INFORMATION FOR METALLIZATION OPTIONS.....	21
3.3 DUMMY PATTERN FILL CAD LAYERS	23
3.4 SPECIAL RECOGNITION CAD LAYER SUMMARY	25
3.5 DEVICE TRUTH TABLES	30
3.5.1 CLN07: 0.75V Core Design	30
3.6 DESIGN GEOMETRY RESTRICTIONS	36
3.6.1 Design Grid Rules	36
3.6.2 OPC Recommendations and Guidelines	37
3.7 DESIGN HIERARCHY GUIDELINES	39
3.8 CHIP IMPLEMENTATION AND TAPE OUT CHECKLIST	40
3.9 DRC METHODOLOGY	41
3.9.1 Definition of Delta Voltage Calculation	41
3.9.2 Voltage recognition CAD Layer	42
3.9.3 Voltage Recognition Method of Connection NET	46
3.9.4 Suggestion Design Flow of Voltage in a Net	51
3.9.5 DRC methodology of density exclusion	52
4 LAYOUT RULES AND RECOMMENDATIONS	53
4.1 LAYOUT RULE CONVENTIONS	53
4.2 DERIVED GEOMETRIES USED IN PHYSICAL DESIGN RULES.....	54
4.2.1 Derived Geometries	54
4.2.2 Special Definition.....	55
4.2.3 Collective Layers	56
4.3 DEFINITION OF LAYOUT GEOMETRICAL TERMINOLOGY	57
4.4 MINIMUM PITCHES	74
4.5 LAYOUT RULES AND GUIDELINES	75
4.5.1 Chip Boundary Layout Rules	75
4.5.2 FinFET Boundary Layout Rules	77
4.5.3 Gate Oxide and Diffusion (OD) Layout Rules	83
4.5.4 Cut-OD (COD) Layout Rules.....	98
4.5.5 Deep N-Well (DNW) Layout Rules [Optional]	107
4.5.6 N-Well (NW) Layout Rules	110
4.5.7 N-Well Under STI (NWRSTI) Layout Rules	115
4.5.8 NT_N Layout Rules	117
4.5.9 OD2 Layout Rules	118

4.5.10	OD18_15 Layout Rules.....	120
4.5.11	OD18_12 Layout Rules.....	122
4.5.12	OD15_12 Layout Rules.....	123
4.5.13	Standard Cell Layout Rules	124
4.5.14	BV_FB Layout Rules.....	212
4.5.15	BPO_V Layout Rules	216
4.5.16	Poly on OD edge (PODE) Layout Rules	219
4.5.17	Connected PODE (CPODE) Layout Rules (72N, 82N)	225
4.5.18	Poly Pitch 0.063 μm (PO_P63) Layout Rules.....	233
4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules.....	237
4.5.20	Poly (PO) Layout Rules	239
4.5.21	Cut-Poly (CPO) Layout Rules	269
4.5.22	Trim PO (TPO) Layout Rules.....	281
4.5.23	PO_Boundary (POB) Layout Rules	286
4.5.24	Butted PO (BPO) Layout Rules	288
4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	292
4.5.26	P+ Source/Drain Ion Implantation (PP) Layout Rules	303
4.5.27	N+ Source/Drain Ion Implantation (NP) Layout Rules	309
4.5.28	Layout Rules for Strained S/D Mask Logical Operation	315
4.5.29	DIODMY Layout Rules.....	316
4.5.30	High R Resistor Layout Rules.....	318
4.5.31	Metal Resistor (RM) Layout Rules	326
4.5.32	MOS Varactor Layout Rules (VAR)	327
4.5.33	MD Layout Rules	329
4.5.34	Cut-MD (CMD) Layout Rules	354
4.5.35	Butted CMD (BCMD) Layout Rules	363
4.5.36	MP Layout Rules.....	366
4.5.37	VC Layout Rules	374
4.5.38	Butted VG (BVG) Layout Rules	384
4.5.39	M0 Layout Rules	386
4.5.40	Cut-M0 (CM0) Layout Rules	404
4.5.41	Butted CM0 (BCM0) Layout Rules	417
4.5.42	VIA0 Layout Rules	423
4.5.43	M1 Layout Rules	443
4.5.44	VIAxs Layout Rules.....	468
4.5.45	Mxs Layout Rules	489
4.5.46	VIAx Layout Rules	508
4.5.47	Mx Layout Rules	534
4.5.48	VIAxa Layout Rules	560
4.5.49	Mxa Layout Rules	579
4.5.50	VIAya Layout Rules	605
4.5.51	Mya Layout Rules	618
4.5.52	VIAy Layout Rules	639
4.5.53	My Layout Rules	649
4.5.54	VIAyy Layout Rules.....	667
4.5.55	Myy Layout Rules	672
4.5.56	VIAyx Layout Rules.....	677
4.5.57	Myx Layout Rules	681
4.5.58	VIAyz Layout Rules.....	683
4.5.59	Myz Layout Rules	686
4.5.60	VIAz Layout Rules	688
4.5.61	Mz Layout Rules	691
4.5.62	VIAr Layout Rules	693
4.5.63	Mr Layout Rules.....	696
4.5.64	MOM Layout Rules	698
4.5.65	INDDMY Layer Identified Inductor Layout Rules	703
4.5.66	Product Labels and Logo Layout Rules.....	705
4.5.67	SRAM Layout Rules.....	706
4.5.68	MetalFuse Layout Rules	728
4.5.69	Antenna Effect Prevention (A) Layout Rules	731
4.5.70	RV Layout Rules [optional]	736
4.5.71	AI Redistribution Layer (AP RDL) Layout Rules [optional]	737
4.5.72	Seal Ring Rules	739
4.5.73	Pattern Treatment (PT) Rules.....	777

4.5.74	HD MIM Layout Rules.....	787
4.5.75	Extensive Forbidden Pattern (EFP) Rules.....	813
5	LAYOUT RULES FOR THE DEVICE GEOMETRY EFFECT	814
5.1	LAYOUT GUIDELINES FOR THE WPE (WELL PROXIMITY EFFECT).....	814
5.2	LAYOUT GUIDELINES FOR THE CPO EFFECT	815
5.3	LAYOUT GUIDELINES FOR LOD (LENGTH OF THE OD REGION) EFFECT	816
5.3.1	What is LOD?	816
5.4	LAYOUT GUIDELINES FOR OSE (OD SPACE EFFECT)	817
5.4.1	What is OSE?	817
5.5	LAYOUT GUIDELINES FOR MBE (METAL BOUNDARY EFFECT).....	818
5.5.1	What is MBE?.....	818
6	DUMMY PATTERN RULE AND FILLING GUIDELINE	819
6.1	DUMMY CELL RULES.....	819
6.2	DUMMY METAL (DM) RULES	824
6.3	DUMMY VIA (DVIA) RULES	831
6.4	DUMMY CPODE (DCPODE) RULES	835
6.5	DUMMY TCD RULES AND FILLING GUIDELINE	838
6.5.1	Dummy TCD Rules	838
6.5.2	Dummy TCD Insertion Guideline	844
6.6	IN CHIP OVERLAY (ICOVL) RULE AND FILLING GUIDELINE	846
6.6.1	In Chip Overlay (ICOVL) Introduction	846
6.6.2	N7+ In-Chip OVL Insertion Methodology	861
6.7	IP DENSITY GUIDELINES.....	863
6.7.1	IP_TIGHTEN_DENSITY Switch.....	864
6.7.2	IP_TIGHTEN_BOUNDARY Switch.....	869
7	DESIGN FOR MANUFACTURING (DFM)	871
7.1	LAYOUT GUIDELINES FOR YIELD ENHANCEMENT	871
7.1.1	Guidelines for Optimal Electrical Model and Silicon Correlation.....	871
7.1.2	Layout Tips for Minimizing Critical Areas	876
7.2	DFM RECOMMENDATIONS AND GUIDELINES SUMMARY	877
7.2.1	Recommendations	877
7.2.2	Guidelines	882
7.2.3	Grouping Table of Recommendations	883
7.3	GUIDELINES FOR MASK MAKING EFFICIENCY.....	885
7.4	DIE SIZE OPTIMIZATION KIT (GDA AND MFU)	886
7.4.1	What is MFU?.....	886
7.4.2	How to simulate MFU?	887
7.4.3	Design Guidelines for Higher MFU	887
7.4.4	MFU DRC examination	888
8	LAYOUT RULES AND RECOMMENDATIONS FOR ANALOG CIRCUITS	889
8.1	USER GUIDES	889
8.2	LAYOUT RULES, RECOMMENDATIONS AND GUIDELINES FOR THE ANALOG DESIGNS	890
8.2.1	General Guidelines.....	890
8.2.2	MOS Recommendations	891
8.2.3	Bipolar Transistor (BJT) Rules and Recommendations	912
8.2.4	Bipolar Transistor (IBJT) Rules and Recommendations	913
8.2.5	MOS Capacitor and Varactor	914
8.2.6	RF Varactor Guidelines	915
8.2.7	MoM Guidelines	917
8.2.8	Hi-R Guidelines	919
8.2.9	Metal Routing Guidelines	921
8.3	NOISE	922
8.3.1	Power and Ground	922
8.3.2	Signal	924
8.4	BURN-IN GUIDELINES FOR ANALOG CIRCUITS	924
9	LAYOUT GUIDELINES FOR LATCH-UP AND I/O ESD	926
9.1	LAYOUT RULES AND GUIDELINES FOR LATCH-UP PREVENTION	927
9.1.1	Latch-up Introduction	927
9.1.2	Layout Rules and Guidelines for Latch-up Prevention.....	930

9.1.3	Test Specification and Requirements	980
9.2	I/O ESD PROTECTION CIRCUIT DESIGN, LAYOUT RULES AND GUIDELINES	981
9.2.1	ESD introduction	981
9.2.2	ESD Implant (ESDIMP) Layout Rules.....	982
9.2.3	SR_ESD device Layout Rules	982
9.2.4	SDI Dummy Layer	983
9.2.5	DRC methodology for ESD guidelines	985
9.2.6	ESD Guidelines	991
9.2.7	CDM Protection for Cross Domain Interface.....	1021
9.3	ESD BACK-END RELIABILITY GUIDELINE	1049
9.3.1	Test Methodology.....	1049
9.3.2	Failure Mechanism.....	1050
9.3.3	Maximum ESD Current Density for Resistor.....	1050
9.3.4	Maximum ESD current density for M0, Via, and Metal	1051
9.3.5	Minimum ESD Current for ESD device	1054
9.3.6	Min. metal width to meet ESD specification.....	1055
9.4	TIPS FOR THE ESD/LATCHUP DESIGN.....	1056
9.4.1	Tips for General Latchup Design	1056
9.4.2	Tips for General ESD Design	1056
9.4.3	Tips for Power-Ground ESD Protection	1057
9.5	ESD TEST METHODOLOGY.....	1059
9.5.1	Stress condition and Measurement condition	1059
9.5.2	Failure criteria.....	1059
10	RELIABILITY RULES.....	1060
10.1	TERMINOLOGY	1060
10.2	FRONT-END PROCESS RELIABILITY RULES AND MODELS	1060
10.3	BACK-END PROCESS RELIABILITY RULES.....	1061
10.3.1	Guidelines for Stress Migration(SM)	1061
10.3.2	Guidelines for Low-k Dielectric Integrity	1062
10.4	CURRENT DENSITY (EM) SPECIFICATIONS	1063
10.4.1	Electromigration Lifetime Prediction Model	1063
10.4.2	Failure Mechanism.....	1063
10.4.3	Failure Criteria	1063
10.4.4	Length and Width Definition in EM Section	1064
10.4.5	Cu Wire Current Density (EM) Specifications ($T_j = 105^\circ\text{C}$)	1065
10.4.6	AP RDL Current Density (EM) Specifications.....	1091
10.4.7	Cu & AP-RDL Metal AC Operation	1092
10.4.8	AP RDL AC Operation	1112
10.4.9	High R Resistor Current Density (EM) Specifications	1113
10.4.10	Metal-Gate Interconnect Current Density (EM) Specifications	1114
11	DESIGN INFORMATION.....	1115
11.1	N7+ UNIVERSAL FIN GRID	1115
11.1.1	Introduction	1115
11.1.2	Design Rule Requirement of Universal Fin Grid.....	1116
11.1.3	Guidelines of FinFET_Boundary in Standard Cells	1117
11.1.4	Guidelines of Design Blocks Contain Multiple Types of FinFET_Boundary	1117
11.1.5	Guidelines of Hierarchical Design Blocks	1118
11.1.6	Guidelines of Chip Integration	1119
11.2	MUST JOIN PIN	1120
11.2.1	Introduction	1120
11.2.2	Must-Join Pin Rules	1120
11.2.3	Guidelines of Marker Creation	1127
12	APPENDIX A REVISION HISTORY.....	1129
12.1	A.1 FROM VERSION 0.5 TO VERSION 0.9	1129
12.2	A.2 FROM VERSION 0.9 TO VERSION 1.0	1140
12.3	A.3 FROM VERSION 1.0 TO VERSION 1.0_1	1148
12.4	A.4 FROM VERSION 1.0_1 TO VERSION 1.0_2	1149

1 Introduction

This chapter has been divided into the following topics:

- 1.1 Overview
- 1.2 Reference documentation

1.1 Overview

This document provides all the rules and reference information for the design and layout of integration circuits using the TSMC 7 NM CMOS LOGIC 1P15M (single poly, 15 metal layers), salicide, Cu technology. These rules and information about other specifications apply to TSMC semiconductor process: CLN07.

- **CLN07** is FinFET base with a 0.75V core design, and with 1.8V or 1.5V capable I/O.

In this document, figures and tables are usually numbered with 3 digits. The first two digits indicate section number and the last one is sequence number. For example, Table 1.2.1 is the first table in the section 1.2 of Chapter 1.



Warning: All tape-outs MUST be DRC clean.

1.2 Reference Documentation

Table 1.2.1 Reference Documents

Content	Reference Documentation
Reference Flow	Please download it from TSMC on-line
GDS layer usage	T-N07-CL-LE-001 TSMC 7 NM FINFET GDS LAYER USAGE DESCRIPTION FILE
DRC deck	T-N07-CL-DR-022-X1 (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) TSMC 7 NM FINFET CMOS LOGIC DRC COMMAND FILE
Dummy pattern generation utility	T-N07-CL-DR-022-X2 (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) TSMC 7 NM CMOS LOGIC DUMMY OD/PO GENERATION UTILITY T-N07-CL-DR-022-X3 (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) TSMC 7 NM CMOS LOGIC DUMMY METAL GENERATION UTILITY
Flip Chip deck	T-N07-BP-DR-004 TSMC 7 NM CU BUMP ON PAD FLIP CHIP WITH BUILD UP SUBSTRATE (FCBGA, FLIP CHIP BALL GRID ARRAY) AND INTERCONNECTION DESIGN RULE N7
InFO DRM information	Contact TSMC
COWOS deck	T-000-TS-DR-001 TSMC INTERPOSER COWOS (CHIP ON WAFER ON SUBSTRATE) DESIGN RULE
Device formation examples and LVS properties	T-N07-CL-LS-001 TSMC 7NM CMOS LOGIC FIN FET 1P8M HKMG CU_ELK 0.75/1.8V DEVICE FORMATION
LVS	T-N07-CL-LS-001-X1 (<i>X</i> is the code of EDA tool. Please refer to TSMC-Online for the details.) TSMC 7NM CMOS LOGIC FIN FET 1P8M HKMG CU_ELK 0.75/1.8V LVS COMMAND FILE

Content	Reference Documentation
MFU Advisor	T-000-CL-RP-013 TSMC MFU ADVISOR
SPICE	T-N07-CL-SP-011 TSMC 7 NM CMOS LOGIC FINFET PLUS (N7+) 0.75/1.8V SPICE MODEL
RTO Guideline	T-N07-CL-DR-041 TSMC 7 NM PLUS (N7+) RTO GUIDELINE - FOR MASK REVISION IMPACT ANALYSIS
RTO deck	T-N07-CL-DR-041-X1 (X is the code of EDA tool, please refer to TSMC-Online for the details) TSMC 7 NM PLUS (N7+) RTO GUIDELINE - FOR MASK REVISION IMPACT ANALYSIS COMMAND FILE (CALIBRE)
Automotive	T-N07-CL-DR-043 TSMC 7 NM CMOS LOGIC FINFET PLUS (N7+) AUTOMOTIVE DESIGN RULE
SRAM sanity checker	T-N07-CL-DR-024 TSMC 7 NM CMOS LOGIC SRAM SANITY CHECKER FINFET PLUS (N7+) (FOR LIMITED OFFER ONLY)

VIAI Confidential Information
938214
10/05/2018

2 Technology Overview

This chapter provides information about the following:

- 2.1 Semiconductor process (including front-end and back-end features)
- 2.2 Devices
- 2.3 Power supply and operation temperature ranges
- 2.4 Cross-section
- 2.5 Metallization Information

2.1 Semiconductor Process

The process consists of the front-end features and the back-end features.

2.1.1 Back-End Features

- Eleven to fifteen Cu metal levels, plus last metal level in Al pad.
- AlCu pad layer can be used as a redistribution layer (AP RDL) option.
- One or two thick last (top) Cu metal layers at a relaxed pitch for power, clock, busses, and major interconnect signal distribution
- Tight pitch levels for routing on thin Cu for the other metal levels below the thick level
- Chemical mechanical polishing (CMP) for enhanced planarization
- Dual damascene copper interconnection, for metal-2 to the last (top) metal
- Wire bond or flip chip terminals

2.1.2 Front-End Features

- **Shallow trench isolation (STI)**
Used for active isolation to reduce active pitch (OD pitch)
- **Retrograde twin well CMOS technology**
For a low well sheet resistance and enhancement of latch-up behavior (compared with conventionally diffused wells). Also provides for a good control of short parasitic field transistors.
- **Triple well, Deep N-Well (optional)**
For isolating P-Well from the substrate
- **Dual gate oxide process**
CLN07: Core: 0.75V , IO: 1.5V/1.8V
- **N+/P+ metal gate**
Allows symmetrical design of NMOS and PMOS devices
- **Multiple V_t devices for high performance requirements**
These devices may be mixed on the same die.
- **SRAM cells offering**

Technology	N7+
Cell Size	HD = 0.0274 μm^2
	HC = 0.0342 μm^2
	DP = 0.0750 μm^2
	8T2P_2FIN = 0.0496 μm^2
	8T2P_3FIN = 0.0530 μm^2

- **Self-aligned silicided drain and source**
Silicide is necessary to short drain and source; furthermore, it drastically reduces S/D serial resistance.
- **NW resistors**
One kind of NW resistor: NW resistor under STI.
- **Varactors**
CLN07: MOS varactors provide 0.75V/1.8V NMOS-in-NW capacitor structures.

2.2 Devices

The technology provides multiple V_t devices.

Table 2.2.1 Available V_t in each technology

Core	Technology
	N7+(0.75V)
STD V_t	✓
Low V_t	✓
Ultra Low V_t	✓

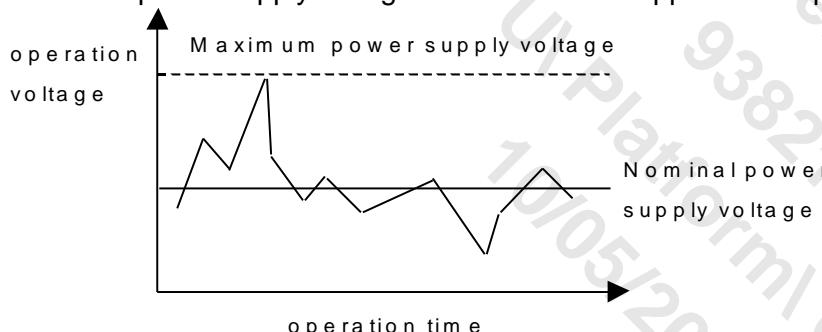
2.3 Power Supply and Operation Temperature Ranges

Table 2.3.1 Power Supplies

	Technology	
	N7+	
	Normal power supply	*Max power supply
Core (thin oxide)	0.75V	0.96V
I/O (thick oxide)	1.8V	1.98V
I/O (thick oxide)	1.5V	1.65V
1.8V underdrive to 1.5V	1.5V	1.65V
1.8V underdrive to 1.2V	1.2V	1.32V
1.5V underdrive to 1.2V	1.2V	1.32V

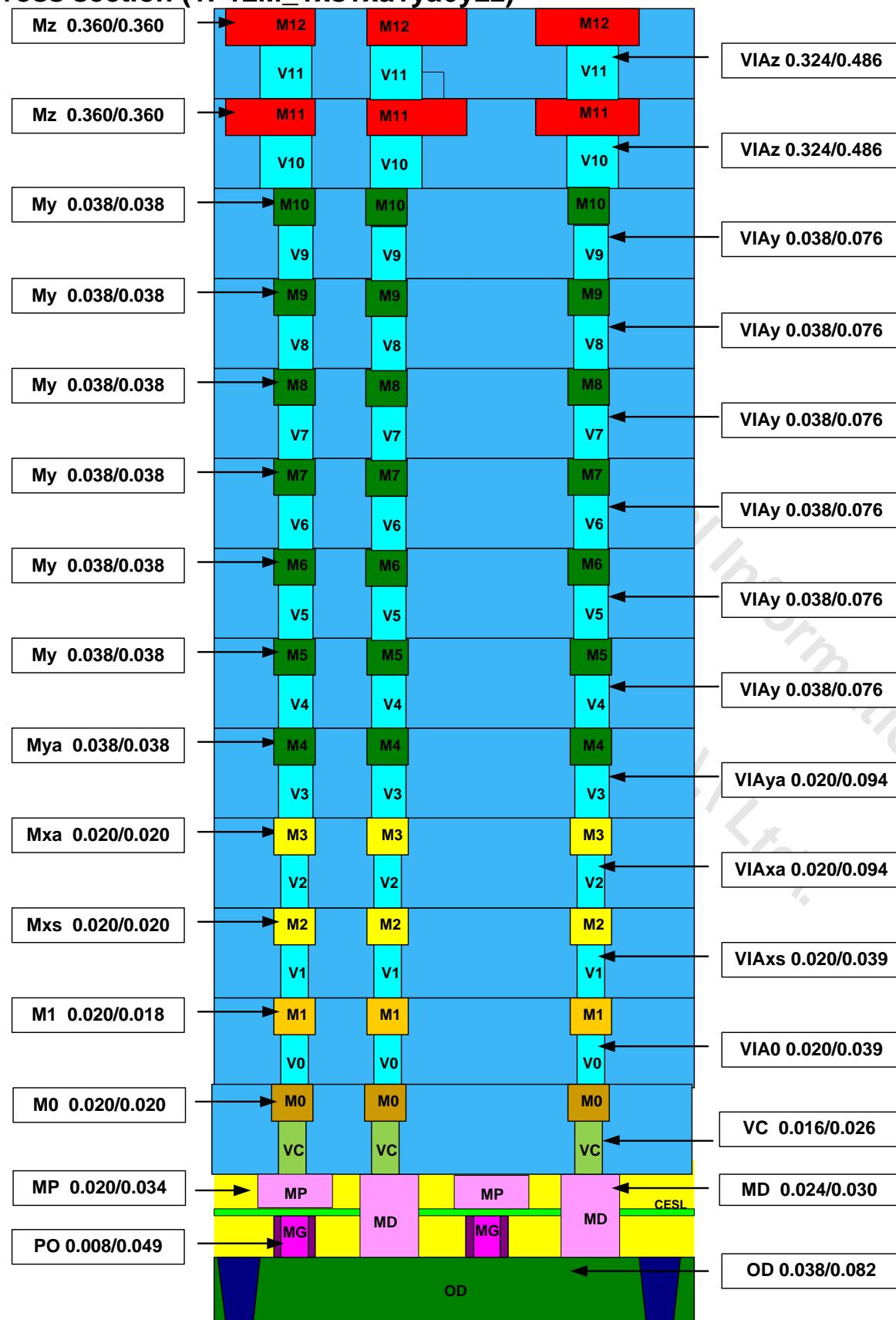
The operation temperature range is -40°C to 125°C (junction temperature).

Maximum power supply voltage means variation upper limit of product operation voltage.



2.4 Cross-section

Cross section (1P12M_1xs1xa1ya6y2z)



2.5 Metallization Information

The general N7+ logic process supports a single poly and fifteen metal layers (1P15M). Other metallization options are available and shown in the following table.

Table 2.5.1 Naming for Different Metal Types

Metal Type	Code	W/S (μm)
M0	M0	0.020/0.020
1.4X Metal	M1	0.020/0.018
1X Metal	Mxs	0.020/0.020
1X Metal	Mx	0.020/0.020
1X Metal	Mxa	0.020/0.020
2X Metal	Mya	0.038/0.038
2X Metal	My	0.038/0.038
3X Metal	Myy	0.062/0.064
6X Metal	Myx	0.126/0.126
9X Metal	Myz	0.18/0.18
18X Metal	Mz	0.36/0.36
22.5X Metal	Mr	0.45/0.45
Al RDL	AP	1.8/1.8

Table 2.5.2 Naming for Different Via Types

Via Type	Code	W/S (μm)
1X Via	VIA0	0.020/0.044 (square-square) 0.020/0.049 (square-rectangular) 0.020/0.049 (rectangular-rectangular)
1X Via	VIAxs	0.020/0.044 (square-square) 0.020/0.049 (square-rectangular) 0.020/0.049 (rectangular-rectangular)
1X Via	VIAx	0.020/0.044 (square-square) 0.020/0.049 (square-rectangular) 0.020/0.049 (rectangular-rectangular)
1X Via	VIAxa	0.020/0.094 (square-square) 0.020/0.095 (square-rectangular) 0.020/0.100 (rectangular-rectangular)
1X Via	VIAya	0.020/0.094 (square-square) 0.020/0.095 (square-rectangular) 0.020/0.100 (rectangular-rectangular)
2X Via	VIAy	0.038/0.076 (square-square) 0.038/0.082 (square-rectangular) 0.038/0.082 (rectangular-rectangular)
3X Via	VIAyy	0.062/0.064
6X Via	VIAyx	0.126/0.126
9X Via	VIAyz	0.180/0.180
16.2X Via	VIAz	0.324/0.486
20.7X Via	VIAr	0.414/0.594
Al Via	RV	2.7

Table 2.5.3

Metallization Options (Mz is used as top Metal)

Top Metal	Mz													
	M0	M0	M0	M0	M0	M0	M0	M0	M0	M0	M0	M0	M0	M0
V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0	V0
M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
VIA1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1
M2	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1
VIA2	Vxa1	Vx1	Vxa1	Vxa1	Vxa1	Vx1	Vxa1	Vxa1	Vx1	Vx1	Vxa1	Vxa1	Vx1	Vx1
M3	Mxa1	Mx1	Mxa1	Mxa1	Mxa1	Mx1	Mxa1	Mxa1	Mx1	Mx1	Mxa1	Mxa1	Mx1	Mx1
VIA3	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1	Vxa2	Vya1	Vya1
M4	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1	Mxa2	Mya1	Mya1
VIA4	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1	Vxa3	Vy1	Vy1
M5	My1	My1	My1	My1	My1	My1	My1	My1	My1	My1	My1	Mxa3	My1	My1
VIA5	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2	Vya1	Vy2	Vy2
M6	My2	My2	My2	My2	My2	My2	My2	My2	My2	My2	My2	Mya1	My2	My2
VIA6	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3	Vy1	Vy1	Vy3
M7	My3	My3	My3	My3	My3	My3	My3	My3	My3	My3	My3	My1	My3	My3
VIA7	Vy4	Vz1	Vy4	Vy2	Vy4	Vy4								
M8	My4	Mz1	My4	My2	My4									
VIA8	Vz1	Vz2	Vz1	Vy5	Vy5	Vy5	Vy5	Vyy1	Vy5	Vy5	Vy5	Vy3	Vyy1	Vyy1
M9	Mz1	Mz2	Mz1	My5	My5	My5	My5	Myy1	My5	My5	My5	My3	Myy1	Myy1
VIA9			Vz2	Vz1	Vz1	Vz1	Vy6	Vyy2	Vy6	Vy6	Vyy1	Vy4	Vyy2	Vyy2
M10			Mz2	Mz1	Mz1	Mz1	My6	Myy2	My6	My6	Myy1	My4	Myy2	Myy2
VIA10					Vz2	Vz2	Vz1	Vz1	Vz1	Vy7	Vyy2	Vy5	Vyy3	Vyy3
M11					Mz2	Mz2	Mz1	Mz1	Mz1	My7	Myy2	My5	Myy3	Myy3
VIA11							Vz2	Vz2	Vz2	Vz1	Vz1	Vy6	Vyx1	Vyx1
M12							Mz2	Mz2	Mz2	Mz1	Mz1	My6	Myx1	Myx1
VIA12										Vz2	Vz2	Vz1	Vyx2	Vyx2
M13										Mz2	Mz2	Mz1	Mzx2	Mzx2
VIA13												Vz2	Vz1	Vz1
M14												Mz2	Mz1	Mz1
VIA14													Vz2	Vz2
M15														Mz2
Wire bond (Au)	Contact TSMC													
EU Flip chip	Contact TSMC													
LF Flip chip	Contact TSMC													
InFO-POP	Contact TSMC													

Note:

1. The mark “————” in the above table stands for HD MIM layer

Table 2.5.4**Metallization Options (Mr is used as top Metal)**

Top Metal	Mr							
M0	M0	M0	M0	M0	M0	M0	M0	M0
V0	V0	V0	V0	V0	V0	V0	V0	V0
M1	M1	M1	M1	M1	M1	M1	M1	M1
VIA1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1	Vxs1
M2	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1	Mxs1
VIA2	Vxa1	Vx1	Vxa1	Vxa1	Vx1	Vx1	Vxa1	Vxa1
M3	Mxa1	Mx1	Mxa1	Mxa1	Mx1	Mx1	Mxa1	Mxa1
VIA3	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1	Vya1
M4	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1	Mya1
VIA4	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1	Vy1
M5	My1	My1	My1	My1	My1	My1	My1	My1
VIA5	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2	Vy2
M6	My2	My2	My2	My2	My2	My2	My2	My2
VIA6	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3	Vy3
M7	My3	My3	My3	My3	My3	My3	My3	My3
VIA7	Vy4	Vyy1	Vy4	Vy4	Vy4	Vy4	Vy4	Vy4
M8	My4	Myy1	My4	My4	My4	My4	My4	My4
VIA8	Vr1	Vyy2	Vyy1	Vy5	Vy5	Vy5	Vy5	Vy5
M9	Mr1	Myy2	Myy1	My5	My5	My5	My5	My5
VIA9	Vr2	Vr1	Vyy2	Vyy1	Vyy1	Vyy1	Vyy1	Vyy1
M10	Mr2	Mr1	Myy2	Myy1	Myy1	Myy1	Myy1	Myy1
VIA10		Vr2	Vr1	Vyy2	Vyy2	Vyy2	Vyy2	Vyy2
M11		Mr2	Mr1	Myy2	Myy2	Myy2	Myy2	Myy2
VIA11			Vr2	Vr1	Vr1	Vyx1	Vyx1	Vyx1
M12			Mr2	Mr1	Mr1	Myx1	Myx1	Myx1
VIA12				Vr2	Vr2	Vyx2	Vyx2	Vyx2
M13				Mr2	Mr2	Myx2	Myx2	Myx2
VIA13						Vr1	Vr1	Vr1
M14						Mr1	Mr1	Mr1
VIA14						Vr2	Vr2	Vr2
M15						Mr2	Mr2	Mr2
Wire bond (Au)	Contact TSMC							
EU Flip chip	Contact TSMC							
LF Flip chip	Contact TSMC							
InFO-POP	Contact TSMC							

Note:

1. The mark “————” in the above table stands for HD MIM layer

3 General Layout Information

This chapter provides the following general layout information:

- 3.1 Mask information, key process sequence, and CAD layers
- 3.2 Metal/via CAD layer information for metallization options
- 3.3 Dummy pattern fill CAD Layers
- 3.4 Special recognition CAD layer summary
- 3.5 Device truth tables
- 3.6 Design geometry restrictions
- 3.7 Design hierarchy guidelines
- 3.8 Chip Implementation and Tape Out Checklist
- 3.9 DRC methodology of net voltage recognition

3.1 Mask Information, Key Process Sequence, and CAD Layers

All tables list masks and corresponding masking steps.

- 1. The **VTC_N/VTC_P** masks are default masks for those customers who use certain SRAM cell IP.
- 2. TSMC uses NW and OD2 (OD_18 or OD_15) to generate **NW1V, NW2V, PW1V, and PW2V** masks by logical operations. Designers can draw NW only.
- 3. TSMC uses NP, PP, and other layers to generate **N1V, N2V, P1V, and P2V** masks by logical operations. Designers do not need to draw these masks.
- 4. **AI pad** is a reverse tone of CB with bias. However, in a flip-chip or InFO-POP product, AI pad is a drawn layer.

The **Mask Name column** lists names that are reserved for standard mask steps. These names should not be used for another purpose in tape out files without prior authorization from TSMC.

The **CAD Layer column** lists CAD layer numbers. To obtain all related CAD layer usage information, please refer to TSMC Document.

Table 3.1.1 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN07

It is not allowed for customers to change the digitized tone (Dark or Clear)

key Process Sequen ce * = Optiona l Mask	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Description
1	ZERO	12R	C	Derived	Zero layer
2*	DNW	119	C	1;0	Deep N-Well.
3	PW1V	191	D	Derived	Core device P-Well.
4	NW1V	192	C	Derived	Core device N-Well.
5	OD	120	D	Derived	Thin oxide for device.
6	COD_H	12M	C	Derived	FinFET patterning
7	TOD	12E	C	Derived	OD trim
8	OD_P	12L	D	Derived	OD process
9	COD_V	12P	C	Derived	FinFET patterning
10	PW2V	193	C	Derived	1.8V P-Well.
11	NW2V	194	C	Derived	1.8V N-Well.
12	PO	130,13G	D	Derived	Poly-Si.
13*	TPO2	13Q	C	Derived	PO trim2
14	TPO	13B	C	Derived	PO trim
15	N2V	116	C	Derived	1.8V NLDD implantation.
16	P2V	115	C	Derived	1.8V PLDD implantation.
17	N1V	19M	C	Derived	LDD implantation
18	NSSD	126	C	Derived	Strained S/D
19	SSD	123	C	Derived	Strained S/D
20	PFI	199	C	Derived	Pick up implantation
21	NP	198	C	Derived	N+ implantation.
22	PP	197	C	Derived	P+ implantation.
23	CPO	739, 839	D	17;11	Double PO patterning
24	CPODE	72N, 82N	D	Derived	Cut FinFET process
25	OD2	152	D	Derived	1.8V thick oxide for DGO process.
26	VT3	137	C	Derived	VT3 tuning
27	VT1	13D	C	Derived	VT1 tuning
28	PMET	13C	C	Derived	P+ metal gate
29	VT4	138	C	Derived	VT4 tuning
30	VT2	13E	C	Derived	VT2 tuning
31	CMD	A58, B58, C58	D	Derived	Cut MD
32	MD	756, 856	D	Derived	MD
33	PSI_P	19N	C	Derived	P+ PSI
34	MP	759, 859	D	Derived	MP
35*	HIGH_R	134	D	117;6	High R Resistor
36	VC	97A	C	179;400	Via hole between MD/MP and M0.
37	CM0	3AA, 7A0, 8A0	D	180	Cut M0
38	M0	750, 850	D	180	1st metal for interconnection.
39	V0	970	C	159	Via hole between M1 and M0.
40	M1	960	C	31	2nd metal for interconnection
41	VIA1	978	C	51	Via hole between M2 and M1.
42	M2	980	C	32	3rd metal for interconnection
43	VIA2	779, 879 379	D	52	Via hole between M3 and M2.
44	M3	781, 881	D	33	4th metal for interconnection
45	VIA3	773, 873 373	D	53	Via hole between M4 and M3.

key Process Sequence * = Optiona l Mask	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Description
		373	C		
46	M4	784, 884	D	34	5th metal for interconnection.
		384	C		
		774, 874	D		
47	VIA4	374	D	54	Via hole between M5 and M4.
		374	C		
		785, 885	D		
48	M5	385	C	35	6th metal for interconnection
		775, 875	D		
49	VIA5	375	D	55	Via hole between M6 and M5.
		375	C		
		786, 886	D		
50	M6	386	C	36	7th metal for interconnection.
		776, 876	D		
51	VIA6	376	D	56	Via hole between M7 and M6.
		376	C		
		787, 887	D		
52	M7	387	C	37	8th metal for interconnection.
		377	C		
53	VIA7	388	C	57	Via hole between M8 and M7.
54	M8	372	C	38	9th metal for interconnection.
55	VIA8	389	C	58	Via hole between M9 and M8.
56	M9	37A	C	39	10th metal for interconnection.
57	VIA9	38A	C	59	Via hole between M10 and M9.
58	M10	37B	C	40	11th metal for interconnection.
59	VIA10	38B	C	60	Via hole between M11 and M10.
60	M11	37C	C	41	12th metal for interconnection.
61	VIA11	38C	C	61	Via hole between M12 and M11.
62	M12	37D	C	42	13th metal for interconnection.
63	VIA12	38D	C	62	Via hole between M13 and M12.
64	M13	37E	C	43	14th metal for interconnection.
65	VIA13	38E	C	63	Via hole between M14 and M13.
66	M14	37F	C	44	15th metal for interconnection.
67	VIA14	38F	C	64	Via hole between M15 and M14
68	M15	182	D	45	16th metal for interconnection.
69*	CTM	183	D	77	Capacitor Top Metal used in HD MIM
70*	CBM	183	D	88	Capacitor Bottom Metal used in HD MIM

FBEOL option1 (Wire bond without AlCu RDL)

67	CB	107	C	76;0	Passivation-1 open for bond pad.
68	AP	307	D	Derived	AlCu pad.
69	CB2	308	C	86;20	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without AlCu RDL)

67	CB	107	C	169;0	Passivation-1 open for bond pad.
68	AP	307	D	74;0	AlCu pad.
69	CB2	308	C	86;0	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with AlCu RDL)

67	CB-VD	306	C	Derived	Passivation-1 open for bond pad, Al RDL via.
68	AP-MD	309	D	Derived	AlCu pad, Al RDL.
69	CB2	308	C	86;20	Passivation-2 open.

FBEOL option4 (Flip chip with AlCu RDL)

67	CB-VD	306	C	Derived	Passivation-1 open for bond pad, Al RDL via.
68	AP-MD	309	D	74;0	AlCu pad, Al RDL.
69	CB2	308	C	86;0	Passivation-2 open.

FBEOL option5 (InFO-POP with AlCu RDL)

67	CB-VD	306	C	85;0	Passivation -1 VIA hole for bump pad
68	AP-MD	309	D	74;0	AP RDL for bump pad
69	CB2	308	C	86;0	Passivation -2 pad opening for bump pad
70	PM	009	D	5;0	Polyimide opening

3.2 Metal/Via CAD Layer Information for Metallization Options

- Due to the complexity of metallization schemes, Table 3.2.1 is the summary of TSMC metal/via CAD layer number, name, and data type.

The labels "x", "xs", "xa", "ya", "y", "yy", "z", "r" denote different metal schemes and minimum pitches. "x" is first inter-layer metal (Mx) with minimum pitch 0.040 μm. "xs" is inter-layer metal (Mxs) with minimum pitch 0.040 μm. "xa" is inter-layer metal (Mxa) with minimum pitch 0.040 μm. "ya" is inter-layer metal (Mya) with minimum pitch 0.076 μm. "y" is inter-layer metal (My) with minimum pitch 0.076 μm. "yy" is inter-layer metal (Myy) with minimum pitch 0.126 μm. "z" using data type "40" is top layer metal (Mz) with minimum pitch 0.72 μm. "r" using data type "80" is top layer metal (Mr) with minimum pitch 0.900 μm. The via data type is the same as the metal right upon the via.

- For any metal combination, a marker $(1+A+B+C) M_AxByCz$ can be used to represent the metal combination of Mx, My and Mz.

The marker is interpreted as one layer of M1, A layers of Mx, B layers of My, C layers of Mz (Mz). The total metal layer number is $1 + A + B + C$. For example, a 7 metal layer process with one M1 layer, one Mx layers, two Mxa layer, one Mya layer, and one My layer and two Mz layers, can be denoted as 7M_1x2xa1ya1y1z.

Table 3.2.1 Metal CAD Layer Number, Name, and Data type

Layer	CAD	Data type									
		Name	Layer #	x	xs	xa	ya	y	yy	yx	z
M0	180	255,256	-	-	-	-	-	-	-	-	-
VIA0	159	-	420	-	-	-	-	-	-	-	-
M1	31	-	420	-	-	-	-	-	-	-	-
VIA1	51	-	400	-	-	-	-	-	-	-	-
M2	32	-	400	-	-	-	-	-	-	-	-
VIA2	52	250	-	290	-	-	-	-	-	-	-
M3	33	275,276	-	315,316	-	-	-	-	-	-	-
VIA3	53	-	-	-	330	-	-	-	-	-	-
M4	34	-	-	-	-	330	-	-	-	-	-
VIA4	54	-	-	-	-	-	350	-	-	-	-
M5	35	-	-	-	-	-	360	-	-	-	-
VIA5	55	-	-	-	-	-	350	-	-	-	-
M6	36	-	-	-	-	-	350	-	-	-	-
VIA6	56	-	-	-	-	-	350	-	-	-	-
M7	37	-	-	-	-	-	360	-	-	-	-
VIA7	57	-	-	-	-	-	350	-	-	40	-
M8	38	-	-	-	-	-	350	-	-	40	-
VIA8	58	-	-	-	-	-	350	-	-	40	-
M9	39	-	-	-	-	-	360	-	-	40	-
VIA9	59	-	-	-	-	-	350	90	-	40	-
M10	40	-	-	-	-	-	350	90	-	40	-
VIA10	60	-	-	-	-	-	-	90	-	40	-
M11	41	-	-	-	-	-	-	90	-	40	-
VIA11	61	-	-	-	-	-	-	-	370	40	-
M12	42	-	-	-	-	-	-	-	370	40	-
VIA12	62	-	-	-	-	-	-	-	370	40	-
M13	43	-	-	-	-	-	-	-	370	40	-
VIA13	63	-	-	-	-	-	-	-	-	-	80
M14	44	-	-	-	-	-	-	-	-	-	80
VIA14	64	-	-	-	-	-	-	-	-	-	80
M15	45	-	-	-	-	-	-	-	-	-	80

3.3 Dummy Pattern Fill CAD Layers

Table 3.3.1 Dummy Pattern Fill CAD Layers

Dummy Layer	CAD	Dummy Data type									
		FEOL/ MEOL	Metal type								
			x	1, xs	xa	ya	y	yy	yx	z	r
DmyM0	180	-	252,253, 258,259	-	-	-	-	-	-	-	-
DmyM1	31	-	-	421,427	-	-	-	-	-	-	-
DmyM2	32	-	-	401,407	-	-	-	-	-	-	-
DmyM3	33	-	272,273, 258,259	-	312,313, 318,319	-	-	-	-	-	-
DmyM4	34	-	-	-	-	331,337	-	-	-	-	-
DmyM5	35	-	-	-	-	-	361,367	-	-	-	-
DmyM6	36	-	-	-	-	-	351,357	-	-	-	-
DmyM7	37	-	-	-	-	-	361,367	-	-	-	-
DmyM8	38	-	-	-	-	-	351,357	91,97	-	41	-
DmyM9	39	-	-	-	-	-	361,367	91,97	-	41	-
DmyM10	40	-	-	-	-	-	351,357	91,97	-	41	-
DmyM11	41	-	-	-	-	-	-	91,97	-	41	-
DmyM12	42	-	-	-	-	-	-	-	371	41	-
DmyM13	43	-	-	-	-	-	-	-	371	41	-
DmyM14	44	-	-	-	-	-	-	-	-	-	81
DmyM15	45	-	-	-	-	-	-	-	-	-	81
DmyVIA0	159	-	-	427	-	-	-	-	-	-	-
DmyVIA1	51	-	-	407	-	-	-	-	-	-	-
DmyVIA2	52	-	252,253	-	297	-	-	-	-	-	-
DmyVIA3	53	-	-	-	-	331	-	-	-	-	-
DmyVIA4	54	-	-	-	-	-	351	-	-	-	-
DmyVIA5	55	-	-	-	-	-	351	-	-	-	-
DmyVIA6	56	-	-	-	-	-	351	-	-	-	-
DmyVIA7	57	-	-	-	-	-	351	91	-	-	-
DmyVIA8	58	-	-	-	-	-	351	91	-	-	-
DmyVIA9	59	-	-	-	-	-	351	91	-	-	-
DmyVIA10	60	-	-	-	-	-	-	91	-	-	-
DmyVIA11	61	-	-	-	-	-	-	-	-	-	-
DmyVIA12	62	-	-	-	-	-	-	-	-	-	-
DmyVIA13	63	-	-	-	-	-	-	-	-	-	-
DmyVIA14	64	-	-	-	-	-	-	-	-	-	-

Table notes:

1. Metal data types 258/259 (DM0), 421 (DM1), 401 (DMxs), 258/259/278/279 (DMx), 298/299/318/319 (DMxa), 331/341 (DMya), 351/361 (DMy), 91 (DMyy), 371 (DMyx), 41 (DMz), 81 (DMr) are the dummy metals without receiving OPC, where TSMC dummy metal utility will generate data types 258/259 (DM0), 258/259 (DM1), 258/259/278/279 (DMx), 298/299/318/319 (DMxa), 331/341 (DMya), 351/361 (DMy), 41 (DMz), 81 (DMr),.
2. Metal data types 252/253 (DM0_O), 427 (DM1_O), 407 (DMxs), 252/253/272/273 (DMx_O), 292/293/312/313 (DMxa_O), 337/347 (DMya_O), 357/367 (DMy_O) will receive OPC as well as main metal patterns, where TSMC dummy metal utility will generate data types 252/253 (DM0_O), 427 (DM1_O), 407 (DMxs_O), 252/253/272/273 (DMx_O), 292/293/312/313 (DMxa_O), 337/347 (DMya_O), 357/367 (DMy_O)
3. VIA data types 427 (DVIA0), 407 (DVIA1), 252/253 (DVIAx) & 297 (DVIAxa) are the dummy VIAs receiving OPC, where TSMC dummy via utility will generate data types 427 (DVIA0), 407 (DVIA1), 252/253 (DVIAx) & 297 (DVIAxa).
4. VIA data types 251/258/259 (DVIAx), 291 (DVIAxa), 331 (DVIAya), & 351 (DVIAy) & 91 (DVIAyy) are the dummy VIAs without receiving OPC, where TSMC dummy via utility will generate data types 252/253 (DVIAx), 290 (DVIAxa), 331 (DVIAya), 351 (DVIAy), & 91 (DVIAyy).

3.4 Special Recognition CAD Layer Summary

Table 3.4.1 lists special layers used in CLN07 design rules and in DRC command files. These layers are used for CAD device recognition, and DRC waivers. Some CAD layer designators include a GDS data type according to the GDS *layer; data type* format.

The column "Tape-out required layer" indicates that this layer must be noted on the mask tape-out form to provide information for mask making.

Table 3.4.1 Special Layer Summary

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape-out required layer
General					
Chip_Boundary	108;250	Chip area definition	Chip Boundary Layout Rules	✓	✓
FinFET_Boundary_1	250;0	Defines the FinFET area	FinFET_Boundary rule	✓	✓
FinFET_Boundary_9	250;28	Defines Cell Height H240 area	Cell Height 240 (H240) Layout Rules	✓	✓
FinFET_Boundary_8	250;8	Defines Cell Height H300 area	Cell Height 300 (H300) Layout Rules	✓	✓
CCP_9	98;1	CCP_9 (CAD layer: 98;1) is used to define Confined Compact Pattern inside FB_9	Cell Height 240 (H240) Layout Rules	✓	✓
CCP_8	98;8	CCP_8 (CAD layer: 98;8) is used to define Confined Compact Pattern inside FB_8	Cell Height 300 (H300) Layout Rules	✓	✓
HEADER_9	6;129	HEADER_9 (CAD layer: 6;129) is used to define HEADER cell inside FB_9	Cell Height 240 (H240) Layout Rules	✓	✓
HEADER_8	6;128	HEADER_8 (CAD layer: 6;128) is used to define HEADER cell inside FB_8	Cell Height 300 (H300) Layout Rules	✓	✓
prBoundary	108;0	P&R cell boundary layer for auto P&R purpose	OD rule	✓	✓
COD_H	6;17	COD_H (CAD layer: 6;17) is used for Horizontal Cut OD	Cut-OD Layout Rules	✓	✓
COD_V	6;18	COD_V (CAD layer: 6;18) is used for Vertical Cut OD	Cut-OD Layout Rules	✓	✓
DCOD_H	6;27	DCOD_H (CAD layer: 6;27) is used for Horizontal Cut OD	Cut-OD Layout Rules	✓	✓
DCOD_V	6;28	DCOD_V (CAD layer: 6;28) is used for Vertical Cut OD	Cut-OD Layout Rules	✓	✓
COD_BLOCK	6;22	Cut-OD blockage layer	Cut-OD Layout Rules		
NWDMY1	114;0	NWELL 2 terminal resistor dummy layer for DRC and LVS. The NW region covered by only NWDMY is the "NW under STI resistor."	NWRSTI rules	✓	
NWDMY2	114;1	NWELL 3 terminal resistor dummy layer for DRC and LVS. The NW region covered by only NWDMY is the "NW under STI resistor."	NWRSTI rules	✓	

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape-out required layer
RH_TN	117;6	This layer is for high R resistors	High R resistor rules	✓	✓
SR_DTN	117;7	This layer is for high R resistors	High R resistor rules	✓	✓
RH_TNB	117;8	This layer is for high R resistors	High R resistor rules	✓	
VAR	143;0	This layer is for MOS type varactors.	MOS varactor rules	✓	✓
LOGO	158;0	LOGO and product labels layer for DRC	Logo rules	✓	
IBJTD MY	110;3	Cover BJT device	Analog layout rule	✓	✓
BJTED MY	110;2	Cover BJT device emitter	Analog layout rule	✓	✓
RFDMY	161;0	For RF device DRC/LVS. Also serves as an exclusion layer for dummy feature insertion checks.		✓	
INDDMY	144;0	Dummy layer for inductor.	IND layout rule	✓	
DIODMY	119;0	Cover Diode layer	Diode dummy layer	✓	✓
RPDMY_1	115;1	OD resistors and Metal gate and high R resistors dummy layers for LVS and DRC	Metal gate and high R resistor rules	✓	
RPDMY_2	115;2	OD resistors and Metal gate and high R resistors dummy layers for LVS and DRC	Metal gate and high R resistor rules	✓	
PODE_GATE	206;28	PODE_GATE is used to define GATE abutting OD vertical edge for LVS recognize MOS diode and turn-off transistor.	PODE layout rule	✓	
PODE_TrGATE	206;29	PODE_TrGATE is used to define the Transistor (with S/D area) which gate abut PODE_GATE.	PODE layout rule	✓	
CPO	17;11	The PO;11 layer (17;11) is used for the Cut-Poly	Cut-Poly (CPO) layout Rules	✓	✓
DECAPDMY	129;0	Decoupling Capacitor dummy layer to cover DECAP	PO.DN.3	✓	
BVG	179;274	Butted two VC to one rectangular VC	BVG rules	✓	✓
PO_Boundary	108;17	PO_Boundary (CAD layer 108;17) for poly pitch = 0.057 µm on grid.	POB rules	✓	✓
PO_P63	105;5	Defines poly pitch 0.063 µm area	Poly Pitch 0.063 µm (PO_P63) Layout Rules	✓	✓
PO_P76	105;6	Defines poly pitch 0.076 µm area	Poly Pitch 0.076 µm (PO_P76) Layout Rules	✓	✓
BPO	17;50	Butted PO (CAD layer 17;50) is used for SRAM bit cell abut periphery cell.	BPO rules	✓	✓
BPO_2	17;51	BPO_2 (CAD layer 17;51) is used for SRAM bit cell abut periphery cell.	BPO rules	✓	✓
BPO_V	17;52	Vertical Butted PO mark layer	BPO_V	✓	✓
BV_FB	250;119	FinFET boundary vertical butted layer	BV_FB rules	✓	✓
BLK_WF	255;10	FEOL blocking layer for SRAM	SRAM rules	✓	✓
BLK_WB	255;11	BEOL blocking layer for SRAM	SRAM rules	✓	✓
BLK_M1	255;40	BEOL blocking layer for SRAM	SRAM rules	✓	✓
BLK_M2	255;32	BEOL blocking layer for SRAM	SRAM rules	✓	✓

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape-out required layer
BLK_M3	255;33	BEOL blocking layer for SRAM	SRAM rules	✓	✓
BLK_M4	255;34	BEOL blocking layer for SRAM	SRAM rules	✓	✓
BCWDMY	255;14	Boundary cell blocking layer	SRAM Layout Rules	✓	✓
MATCHING	205;8	Critical matching devices in analog circuit, e.g. DAC, Bandgap, current mirror, ADC, OPAMP, analog differential pair, analog filter, RF tuning circuit.	PO.DN.6, PO.R.18	✓	*
ANARRAY_H	255;20	To define sensitive analog N/P MOS array with high matching requirement, e.g. current DAC, ADC.	PO.DN.6, PO.R.18	✓	*
ANARRAY_M	255;21	To define sensitive analog N/P MOS array with medium matching requirement, e.g. Bandgap, OPAMP.	PO.DN.6, PO.R.18	✓	*
ANARRAY_HS	255;23	To define sensitive analog N/P MOS array with medium matching requirement, e.g. Bandgap, OPAMP.	PO.DN.6, PO.R.18	✓	*
ANARRAY_S	255;24	To define sensitive analog N/P MOS array with medium matching requirement, e.g. Bandgap, OPAMP.	PO.DN.6, PO.R.18	✓	*
EUV layers					
VC	179;400	VC	VC rule	✓	✓
VIA0	159;420	VIA0 main layer	VIA0 rule	✓	✓
DVIA0_O	159;427	VIA0 OPC layer	VIA0 rule	✓	✓
VIA1	51;400	VIA1 main layer	VIAxs rule	✓	✓
DVIA1_O	51;407	VIA1 OPC layer	VIAxs rule	✓	✓
M1	31;420	M1 main layer	M1 rule	✓	✓
DM1	31;421	M1 Non-OPC layer	M1 rule	✓	✓
DM1_O	31;427	M1 OPC layer	M1 rule	✓	✓
M2	32;400	M2 main layer	Mxs rule	✓	✓
DM2	32;401	M2 Non-OPC layer	Mxs rule	✓	✓
DM2_O	32;407	M2 OPC layer	Mxs rule	✓	✓
Coloring					
MOCA	180;255	M0 color A marker	M0 rule	✓	✓
MOCB	180;256	M0 color B marker	M0 rule	✓	✓
MxCA	Mx;275	Mx color A marker	Mx rule	✓	✓
MxCB	Mx;276	Mx color B marker	Mx rule	✓	✓
VxCA	VIAx;255	VIAx color A marker	VIAx rule	✓	✓
VxCB	VIAx;256	VIAx color B marker	VIAx rule	✓	✓
Mx;275	Mx;275	MxCA minimum pitch 0.040 µm direction in perpendicular to core PO direction	Mx rules	✓	✓
Mx;276	Mx;276	MxCB minimum pitch 0.040 µm direction in perpendicular to core PO direction	Mx rules	✓	✓
Mxa;295	Mxa;295	MxaCA minimum pitch 0.040 µm direction in parallel to core PO direction	Mxa rules	✓	✓
Mxa;296	Mxa;296	MxaCB minimum pitch 0.040 µm direction in parallel to core PO direction	Mxa rules	✓	✓
Mxa;315	Mxa;315	MxaCA minimum pitch 0.040 µm direction in perpendicular to core PO direction	Mxa rules	✓	✓
Mxa;316	Mxa;316	MxaCB minimum pitch 0.040 µm direction in perpendicular to core PO direction	Mxa rules	✓	✓

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape-out required layer
Mya;330	Mya;330	Mya minimum pitch 0.076 μm direction in parallel to core PO direction	Mya rules	✓	✓
Mya;340	Mya;340	Mya minimum pitch 0.076 μm direction in perpendicular to core PO direction	Mya rules	✓	✓
My;350	My;350	My minimum pitch 0.076 μm direction in parallel to core PO direction	My rules	✓	✓
My;360	My;360	My minimum pitch 0.076 μm direction in perpendicular to core PO direction	My rules	✓	✓
Dummy utility					
DMnEXCL	150;n	Dummy Mn exclusion marker layer	DMn rules	✓	
SR_DOD	6;7	SR_DOD (6;7) only can be used for dummy utility patterns.	OD rules	✓	✓
SR_DPO	17;7	SR_DPO (17;7) only can be used for dummy patterns.	PO layout rule	✓	✓
SR_DCPO	17;23	The PO;23 layer (17;23) is used for the dummy Cut-Poly	Cut-Poly (CPO) layout Rules	✓	✓
SR_DMD	84;7	SR_DMD (84;7) only can be used for dummy utility patterns.	MD rules	✓	✓
SR_DMP	84;47	SR_DMP (84;47) only can be used for dummy utility patterns.	MP rules	✓	✓
DC2_MANDREL	257;21	dummy waive layer	Dummy Cell Rules	✓	✓
DC2_CORE	257;22	dummy waive layer	Dummy Cell Rules	✓	✓
DC2_IO	257;23	dummy waive layer	Dummy Cell Rules	✓	✓
DC3	257;31	dummy waive layer	Dummy Cell Rules	✓	✓
DC4_CORE	257;42	dummy waive layer	Dummy Cell Rules	✓	✓
DC4_IO	257;43	dummy waive layer	Dummy Cell Rules	✓	✓
DC5_1	257;51	dummy waive layer	Dummy Cell Rules	✓	✓
DC5_2	257;52	dummy waive layer	Dummy Cell Rules	✓	✓
DC6_1	257;61	dummy waive layer	Dummy Cell Rules	✓	✓
DC6_2	257;62	dummy waive layer	Dummy Cell Rules	✓	✓
DC7	257;71	dummy waive layer	Dummy Cell Rules	✓	✓
DC8_1	257;81	dummy waive layer	Dummy Cell Rules	✓	✓
DC8_2	257;82	dummy waive layer	Dummy Cell Rules	✓	✓
DC9_1	257;91	dummy waive layer	Dummy Cell Rules	✓	✓
FEOLBLK	150;27	Dummy layer to avoid FEOL dummy insertion	ICOVL rules	✓	
BEOLBLK	150;28	Dummy layer to avoid BEOL dummy insertion	ICOVL rules	✓	
TCDDMY1	165;1	Dummy layer for FEOL/MEOL dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M0	165;180	Dummy layer for M0 dummy TCD pattern	DTCD rules	✓	✓

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape-out required layer
TCDDMY_M1	165;31	Dummy layer for M1 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M2	165;32	Dummy layer for M2 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M3	165;33	Dummy layer for M3 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M4	165;34	Dummy layer for M4 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M5	165;35	Dummy layer for M5 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M6	165;36	Dummy layer for M6 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M7	165;37	Dummy layer for M7 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M8	165;38	Dummy layer for M8 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M9	165;39	Dummy layer for M9 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M10	165;40	Dummy layer for M10 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M11	165;41	Dummy layer for M11 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M12	165;42	Dummy layer for M12 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M13	165;43	Dummy layer for M13 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M14	165;44	Dummy layer for M14 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_M15	165;45	Dummy layer for M15 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V0	165;159	Dummy layer for V0 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V1	165;51	Dummy layer for V1 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V2	165;52	Dummy layer for V2 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V3	165;53	Dummy layer for V3 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V4	165;54	Dummy layer for V4 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V5	165;55	Dummy layer for V5 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V6	165;56	Dummy layer for V6 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V7	165;57	Dummy layer for V7 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V8	165;58	Dummy layer for V8 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V9	165;59	Dummy layer for V9 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V10	165;60	Dummy layer for V10 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V11	165;61	Dummy layer for V11 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V12	165;62	Dummy layer for V12 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V13	165;63	Dummy layer for V13 dummy TCD pattern	DTCD rules	✓	✓
TCDDMY_V14	165;64	Dummy layer for V14 dummy TCD pattern	DTCD rules	✓	✓
ICOVL					
ICOVL_SINGLE	165;320	Dummy layer for ICOVL	ICOVL rules	✓	✓
ICOVL_A	165;70	Dummy layer for ICOVL	ICOVL rules	✓	✓
ICOVL_B	165;71	Dummy layer for ICOVL	ICOVL rules	✓	✓
ICOVL_C	165;72	Dummy layer for ICOVL	ICOVL rules	✓	✓
ICOVL_D	165;73	Dummy layer for ICOVL	ICOVL rules	✓	✓
ICOVL_E	165;74	Dummy layer for ICOVL	ICOVL rules	✓	✓
ICOVL_B1	165;521	Dummy layer for ICOVL	ICOVL rules	✓	✓
ICOVL_D1	165;523	Dummy layer for ICOVL	ICOVL rules	✓	✓
MFUSE					
MetalFuse	156;2	For metal fuse bitCell DRC error waive in N7+ process	MD and Mx/Mxa rules	✓	
MetalFuseLink	156;3	Metal fuse link DRC and LVS recognition layer	MetalFuse rules	✓	✓
MetalFuse_B1	156;8	Metal fuse DRC recognition layer	M1~VIAYA rules	✓	
MetalFuse_B2	156;9	Metal fuse DRC recognition layer for PGM device	M1~VIAYA rules	✓	

3.5 Device Truth Tables

This section contains the device truth tables for:
CLN07 CMOS Logic technology

The following provides a legend for the following device truth table.

- | | |
|---|-------------|
| 1 | Required |
| 0 | Not allowed |
| * | Don't care |

3.5.1 CLN07: 0.75V Core Design

Table 3.5.1 Device Truth Table for N07

Device	SPICE Name	Design Levels														Special Layer														
		DNW	FinFET-Boundary	OD	NW	NT_N	OD_18	OD_15	POLY	VTUL_N	VTUL_P	VTL_N	VTL_P	VTS_N	VTS_P	N+	P+	OD18_15	OD18_12	OD15_12	RH_TN	RPDMDY_1	RPDMDY_2	NWDMDY1	NWDMDY2	VAR	IBJTDMY	DIODMY	SR_ESD	SDI
NMOS (0.75V)	nch_svt_mac	*	1	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	*	0	0	
PMOS (0.75V)	pch_svt_mac	*	1	1	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	*	0	0	
Low Vt NMOS (0.75V)	nch_lvt_mac	*	1	1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	*	0	0	
Low Vt PMOS (0.75V)	pch_lvt_mac	*	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	*	0	0	
Ultra Low Vt NMOS (0.75V)	nch_ulvt_mac	*	1	1	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	*	0	0	
Ultra Low Vt PMOS (0.75V)	pch_ulvt_mac	*	1	1	1	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	*	0	0	
I/O NMOS(1.8V)	nch_18_mac	*	1	1	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	0	0
I/O PMOS(1.8V)	pch_18_mac	*	1	1	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	*	0	0	
I/O NMOS(1.8V underdrive 1.5V)	nch_18ud15_mac	*	1	1	0	0	1	0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	*	0	0	
I/O PMOS(1.8V underdrive 1.5V)	pch_18ud15_mac	*	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	*	0	0	
I/O NMOS(1.8V underdrive 1.2V)	nch_18ud12_mac	*	1	1	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	*	0	0	
I/O PMOS(1.8V underdrive 1.2V)	pch_18ud12_mac	*	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	*	0	0	
Low Vt I/O NMOS(1.5V)	nch_lvt15_mac	*	1	1	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	*	*	0	0
Low Vt I/O PMOS(1.5V)	pch_lvt15_mac	*	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	*	0	0	
Low Vt I/O NMOS(1.5V underdrive 1.2V)	nch_lvt15ud12_mac	*	1	1	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	*	0	0	
Low Vt I/O PMOS(1.5V underdrive 1.2V)	pch_lvt15ud12_mac	*	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	*	0	0	
iBJT PNP (P+/NW/Psub)	pnp_i1_mac	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0
iBJT NPN (N+/PW/DNW)	npn_i1_mac	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0
	npn_i2_mac																													

Device	SPICE Name	Design Levels																				
		DNW		FinFET_Boundary_1																		
		OD	NW	NT_N	OD_18	OD_15	PO	VTUL_N	VTUL_P	VTL_N	VTL_P	VTS_N	VTS_P	NP	PP	MD	MP	VC	M0	VIA0	M1	VIA1
RF Varactor(NMOS Capacitor) with DNW	moscap_rf	1	1	1	1	0	0	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1
1.8V RF Varactor(NMOS Capacitor) with DNW	moscap_rf18	1	1	1	1	0	1	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1
RF Varactor(NMOS Capacitor) without DNW	moscap_rf_nw	0	1	1	1	0	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1
1.8V RF Varactor(NMOS Capacitor) without DNW	moscap_rf18_nw	0	1	1	1	0	1	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1

Device	SPICE Name	Special Layer																		
		OD_18_12	OD_18_15	RH_TN	RPDMY	NWDMY	VAR	BJTDMY	IBJTDMY	DIODMY	SR_ESD	SDI	GATED	HIA_DUMMY	SDI_2	DM0EXCL	DM1EXCL	DM2EXCL	DM3EXCL	RFDMY
RF Varactor(NMOS Capacitor) with DNW	moscap_rf	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1
1.8V RF Varactor(NMOS Capacitor) with DNW	moscap_rf18	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1
RF Varactor(NMOS Capacitor) without DNW	moscap_rf_nw	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1
1.8V RF Varactor(NMOS Capacitor) without DNW	moscap_rf18_nw	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1

Device	SPICE Name	Special Layers																																				
		MOMDMY_0	MOMDMY_1	MOMDMY_2	MOMDMY_3	MOMDMY_4	MOMDMY_5	MOMDMY_6	MOMDMY_7	MOMDMY_8	MOMDMY_9	MOMDMY_10	MOMDMY(155;21)	MOMDMY_22	MOMDMY_23	MOMDMY_24	MOMDMY_25	MOMDMY_27	MOMDMY_28	MOMDMY_31	MOMDMY_32	MOMDMY_33	MOMDMY100-drawing1(155;101)	MOMDMY100-drawing3(155;103)	DM0EXCL	DM1EXCL	DM2EXCL	DM3EXCL	DM4EXCL	DM5EXCL	DM6EXCL	DM7EXCL	DM8EXCL	DM9EXCL	DM10EXCL	FEOLBLK	BEOLBLK	RFDMY
2T RTMOM	crtmom_2t	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	
4T MX RTMOM	crtmom_mx_4t	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0
3T RTMOM with NW shielding	crtmom_wo	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	
3T RTMOM with PW shielding		1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	
3T RTMOM with NTN shielding		1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	
5T MX RTMOM with NW shielding	crtmom_wo_mx	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	
5T MX RTMOM with PW shielding		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	
5T MX RTMOM with NTN shielding		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	
3T RTMOM with NW shielding	crtmom_wo_rf	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	
3T RTMOM with PW shielding		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	
3T RTMOM with NTN shielding		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	

Note:

- 1 MOMDMY(155;21): DRC dummy layer to recognize MOM for DRC check
- 2 MOMDMY(155;22): LVS dummy layer used to recognize MX MOM
- 3 MOMDMY(155;23): LVS dummy layer used to recognize pin plus 1, minus 1 for MX MOM
- 4 MOMDMY(155;24): LVS dummy layer used to recognize pin plus 2, minus 2 for MX MOM
- 5 MOMDMY(155;25): LVS dummy layer used to recognize cross-coupled MOM pin
- 6 MOMDMY(155;27): LVS dummy layer used to recognize 2T BB MOM
- 7 MOMDMY(155;28): LVS dummy layer used to recognize 3T MOM without guardring
- 8 MOMDMY(155;31): LVS dummy layer used to recognize MOM devices with NW shield
- 9 MOMDMY(155;32): LVS dummy layer used to recognize MOM devices with PW shield
- 10 MOMDMY(155;33): LVS dummy layer used to recognize MOM devices with NTN shield
- 11 MOMDMY(155;101): LVS dummy layer for SPICE parameter n_mxa recognition
- 12 MOMDMY(155;103): LVS dummy layer for SPICE parameter vapmod recognition
- 13 RFDMY(161;0): dummy layer for RF devices

3.6 Design Geometry Restrictions

3.6.1 Design Grid Rules

Rule No.	Description	Label	Op.	Rule
G.1	The design grid must be an integer multiple of 0.0005 µm. 0.001 µm deviation is allowed for 45-degree polygon dimensions (Except UBM, AP, or following conditions: 1. CBD [in UBM], 2. CB2_FC [in UBM], 3. PM [in UBM])		=	0.0005
G.2	Shapes with acute angles between line segments are not allowed			
G.3	Only shapes that are orthogonal or on a 45-degree angle are allowed (Except UBM, AP, or following conditions: 1. CBD [in UBM], 2. CB2_FC [in UBM], 3. PM [in UBM])			
G.4	For the OPC layers, any edge of length < 1.0 x minimum width cannot have another adjacent edge of length < 1.0 x minimum width. (Figure 3.6.1) The OPC layers: OD, OD2, PO, CPO, TPO, NW, VTL_N, VTL_P, VTUL_N, VTUL_P, VTS_N, VTS_P, NP, PP, MD, CMD, MP, VC, M0, CM0, VIA0, M1, VIAxs, Mxs, VIAx, Mx, VIAxa, Mxa, VIAya, Mya, VIAy, My, VIAyy, Myy, VIAyx, Myx			
G.5	Layers must be inside Chip_Boundary in chip level (Cut is not allowed) (Except NP, PP, COD_V, M0~AP, LUP_015U, LUP_075U, LUP_150U, or following conditions: 1. patterns [INSIDE SEALRING_ALL])			
G.6g ^U	For DNW, NW, NP, PP, Mn (n = 0, 1, x, xa, ya, y, yy, yx, yz, z, r) all vertices and intersections of 45-degree polygon must be on an integer multiple of 0.0005 µm.			

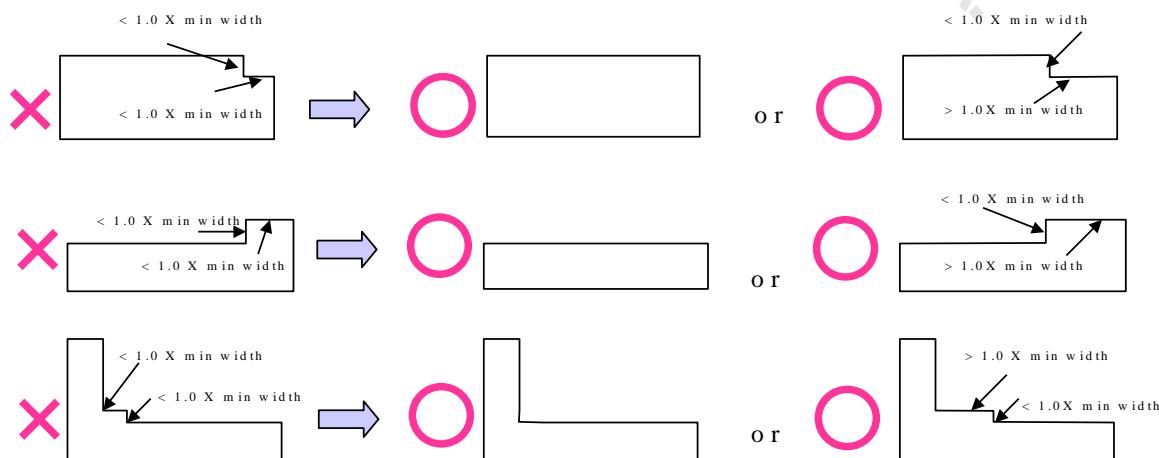


Figure 3.6.1 Illustration for G.4.

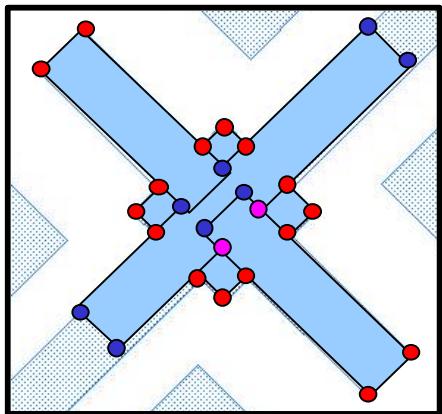


Figure 3.6.2 Illustration for G.6g^U.

3.6.1.1 DBU guideline

Recommend to use 0.5 nm as layout database unit (DBU) when streaming out GDS. TSMC's technology files adopt 0.5 nm DBU by default.

If different DBU setting is considered, please consult it with TSMC for guidelines to modify default setting of TSMC's technology files to prevent from potential failure, for example, job may be terminated.

3.6.2 OPC Recommendations and Guidelines

The following OPC recommendations are very important tips to reduce OPC and mask-making cycle time (or physical verification) and ensure the best silicon performance:

- **Make certain that the design is DRC clean (free of all DRC violations).**
- **Do not use circles, oval shapes, or logos of arbitrary geometry (Figure 3.6.3).** Use rectangular or 45-degree polygons to write words, logos, and other marks that are not part of the circuit.
- **Verify that all line-ends are rectangular.**
- **Limit cell names to 127 or fewer characters.**
- **Use a well-organized, hierarchical layout structure.**
- **Avoid redundant or excessive overlaps of polygons from two, or more than two, different cells or cell placements.** For example, avoid forming a straight line from numerous cell placements, with each one contributing a little piece. Refer to the "Design Hierarchy Guidelines" section in this chapter.
- **Avoid small jogs (Figure 3.6.4).** It is recommended to use greater than, or equal to, half of the minimum width of each layer for each segment of a jog.

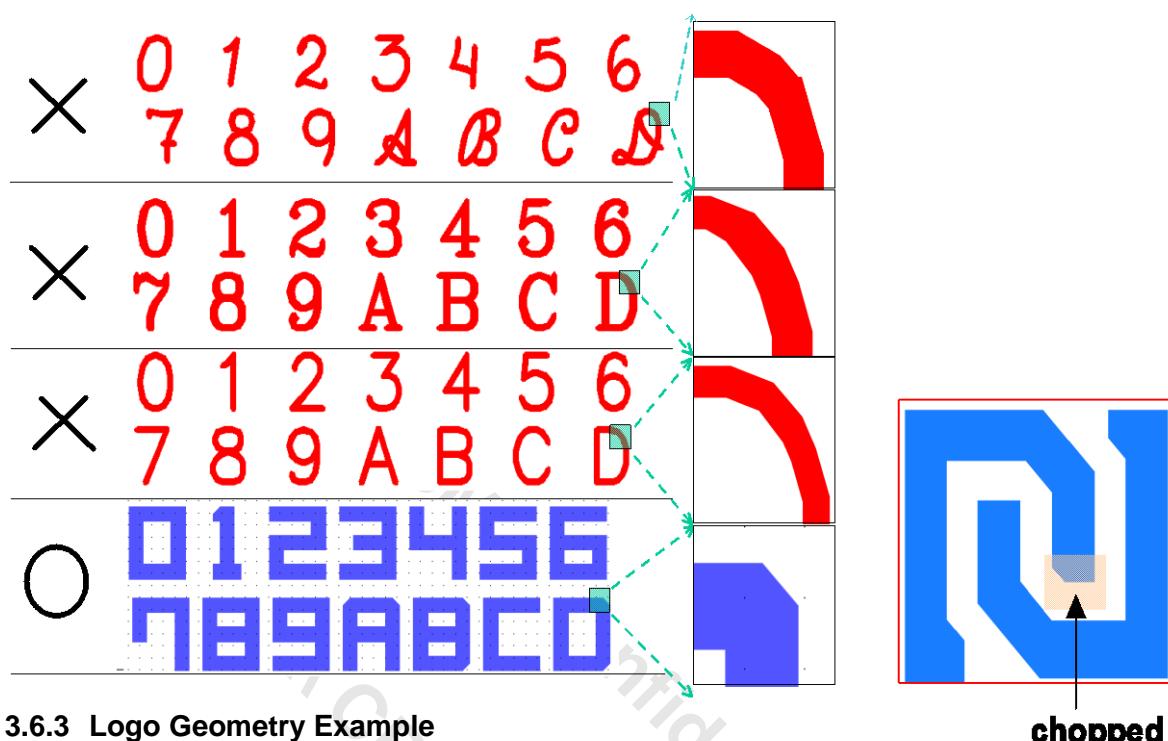


Figure 3.6.3 Logo Geometry Example

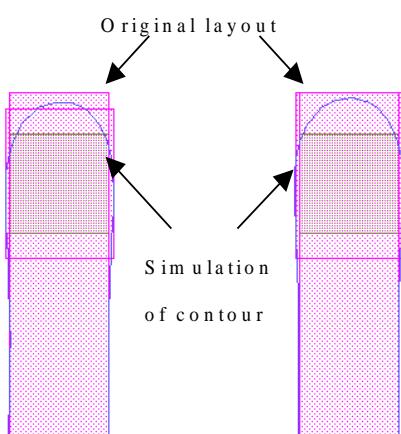


Figure 3.6.4 Simulation contour for the layout with and without small jog/zigzag -- metal line example and can not have well mask database treatment due to small jog/zigzag, and cause smaller overlap on via hole.

3.7 Design Hierarchy Guidelines

The style of the cell hierarchy in a design can significantly affect the following:

- OPC and mask-making cycle time
- Run time and memory usage of physical verification.

Following are the recommended practices:

- Re-use design blocks as much as possible. Do not create two different cells for the same device.
- Whenever possible, avoid using *L*, *U*, or *ring* shapes.
- For inevitable *ring* structures such as seal-rings and power rings, use cells for holding each ring segment instead of drawing the whole ring at once. The same method applies to the *L* and *U* shapes.
- Put everything as low in the cell hierarchy as possible. Here are some examples:
 - Put all shapes required for defining a device or circuit into the same cell. An inverter cell, for example, should include NW, OD, PO, NP, PP, MD, and MP as well as VC and M0 (for pins).
 - Avoid drawing a large shape to cover a whole circuit.
 - Place texts at the lowermost cell where devices can be formed.
 - For layout patches/revisions/ECOs, avoid changing device properties or metal connections at upper cells in the design hierarchy.
 - Draw within the cell the shapes required in TSMC's logic operations. Please consider all independent layers used in each rule logic operations and derived layer logic operations.
 - Make certain each cell is DRC clean in a bottom-up construction of the cell hierarchy. For example, when placing a MD, or MP in a cell, place M0 in that cell as well, with the required amount of M0.
 - Keep dummy fill geometry in a separate hierarchy from the main patterns and reduce the count of flattened dummy fill geometry as much as possible.

3.8 Chip Implementation and Tape Out Checklist

The following checklist is required to be completed prior to the tape out:

- IP are correctly utilized in the design
 - Pay attentions to the special orientation/direction (e.g. SRAM), guard ring or space keep-out requirements of placement.
 - Pay attentions to routing constrains in resistance matching, power net spacing, over block routing, allowed dummy fill layers and power connection/width.
 - To avoid using failed library and IP, please pay attentions to the available library/IP validation status from TSMC Online (Design Portal → Library/IP).
 - It is highly recommended that do not modify or remove the IP tags (CAD 63;63) in the design.
- The design passes signal/power/IR/ESD integrity analysis
 - Simulations of all CKTs in setup time, hold time, timing window reveal acceptable behavior overall operating corners.
 - Analyses in statistical leakage, total power consumption, power network robustness, static/dynamic IR, IO SSO meet design specifics overall operating corners.
 - Ensure all MDs/MPs/vias and metal lines meet EM lifetime requirement.
 - ESD/latch-up layout and design requirements have been met.
- The design passes DRC
 - Use the most update DRC command file version corresponding to the design rule document.
 - Need to choose the DRC options carefully & correctly.
 - Need to cover all the DRC, including latch-up, ESD, antenna, assembly check.
 - It is recommended to run full chip DRC if there is any layout change in cell level.
 - Any DRC violation needs to be reviewed by TSMC, to make sure no production concern.
- The design passes LVS/ERC checks
 - Use the most update LVS/ERC command file version corresponding to the SPICE document.
- Must use TSMC dummy generation utilities to insert dummy patterns to meet the minimum pattern density requirements. Don't change any dimensions and variables of TSMC utilities.
- DFM implementation is recommended
 - Adopt TSMC APR settings for DFM VIA replacement. Or, utilize TSMC redundant VIA utility on customized IP (non-APR routing) design.
 - RC extraction by DFM-LPE to have accurate SPICE simulations in IP design.
 - The section 3.7 Design Hierarchy Guidelines have been considered.
- Tape out information
 - Make sure to have every "tape out required CAD layer" filled correctly in the TSMC e-tapeout system. Additionally, to correctly fill DRC-only CAD layers of the design is welcome.

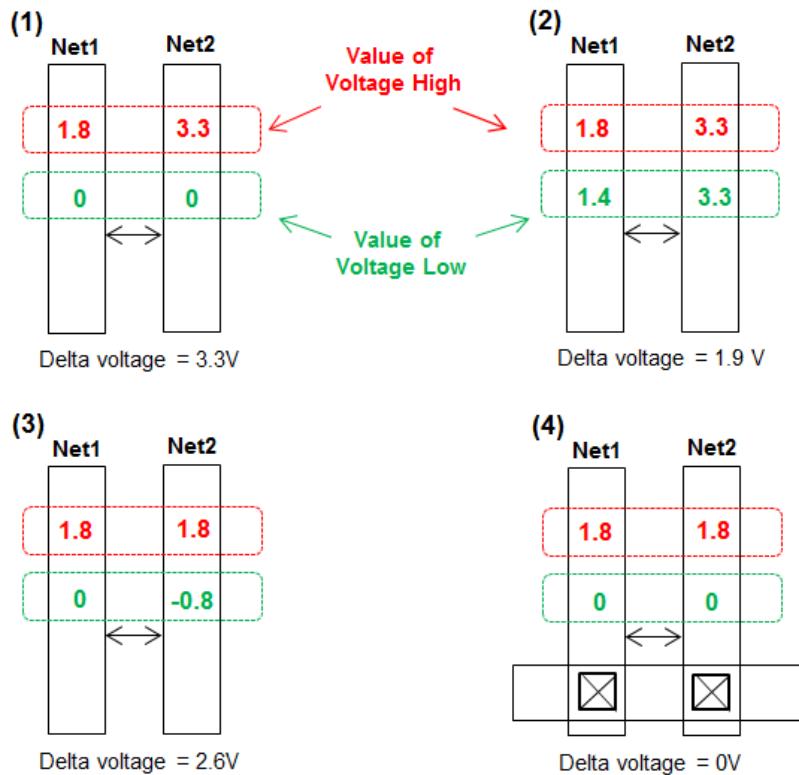
3.9 DRC methodology

This section illustrates the features of definition and methodology on doing the examination of the rules related to delta-voltage in tsmc DRC deck.

3.9.1 Definition of Delta Voltage Calculation

In tsmc DRC deck, it is based on the voltage recognition CAD layer and net connection to calculate the voltage difference between two neighboring nets by the following formula:

- **Delta V** = MAX (Net1 Voltage High – Net2 Voltage Low, Net2 Voltage High – Net1 Voltage Low)
- Voltage High** = the highest voltage on this net
- Voltage Low** = the lowest voltage on this net
- The Delta V will be 0 if two nets are connected as same potential.
- If “Voltage Low” > “Voltage High” on a net, DRC will report warning on this net.



3.9.2 Voltage recognition CAD Layer

In order to let DRC recognition of the net voltage precisely, it is important to place either “the voltage text layer” or “the voltage marker layer” into each net, which with maximum delta V > 0.96V in your design.

To place “the voltage text layer” (both **Voltage High** and **Voltage Low**) in a net is the firstly recommended. It’s the 1st priority of voltage recognition at tsmc DRC deck.

Please refer to sec.3.9.3.3 for the priority sequence of voltage recognition in DRC deck.

3.9.2.1 The usage of voltage text layer

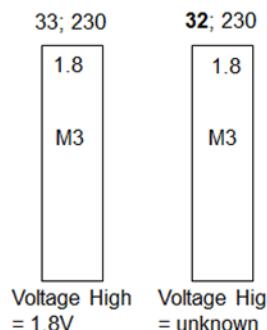
- TSMC only offers the “voltage text” layers of OD, PO, MP, MD, M0~M15 and AP layers for DRC doing the voltage recognition on each net. The definition and usage of these text layers are listed at Table 3.9.1.
- There are totally 4 types of voltage text layers: “Voltage High Top”, “Voltage High”, “Voltage Low Top” and “Voltage Low”.
- Each “voltage text” CAD layer MUST be placed to the corresponding process layer; otherwise, TSMC DRC cannot correctly recognize out the voltage value of the required net. e.g.:

The “Voltage High” will be recognized as “1.8V” if one M3 voltage text “1.8” (CAD layer 33;230) is put on M3 (CAD layer 33;255/33;256 for Mx & 33;295/33;296 for Mxa). But, it cannot be recognized as 1.8V if it’s placed on M2 (CAD layer 32;275/32;276). It has the same result for the recognition of “Voltage Low”. (refer Figure 3.9.2.1.1)
- If there are several “Voltage High” and “Voltage Low” text information in a net, the “Voltage High” will be recognized by the maximum value of these texts and “Voltage Low” will be recognized by the minimum one. e.g. (refer Figure 3.9.2.1.2)
 - The “Voltage High” will be recognized as 1.8V if there are “1.5” by M3 (33;230) and “1.8” by M2 (32;230).
 - The “Voltage Low” will be recognized as 1.2V if there are “1.2” by M3 (33;231) and “1.8” by M2 (32;231).
- “Voltage High Top” and “Voltage Low Top” (CAD layer datatypes 232 and 233, respectively) can be used in GDS top level and these layers are only supported for M1~M15 and AP layers. (refer Figure 3.9.2.1.3)
 1. DRC deck will use these layers to overwrite the original voltage texts in lower hierarchy. e.g.: the “Voltage High” will be recognized as “0V” if there are both M5 voltage text “0” (by CAD layer “35;232”) and “1.2” (by CAD layer “35;230”) put on the same M5. Same result for the recognition of “Voltage Low”.
 2. DRC will treat these layers at the upper metal layer with higher priority. e.g.: the “Voltage High” will be recognized as “0V” if M6 voltage text “0” (by CAD layer “36;232”) and M5 voltage text “1.2” (by CAD layer “35;232”) are put on the same connection net respectively. Same result for the recognition of “Voltage Low”.
 3. If an IP will be reduplication in chip level with several “Voltage High” text/marker layers, but some of them will tie to VSS by different connection. You can place a voltage text “0” by “Voltage High Top” at the topper metal layer of this net. (ex: add AP voltage text “0” by CAD layer 74;232, refer Figure 3.9.2.1.4). Same method is also valid for the case of “Voltage Low”.
- It is useless to assign the voltage text on dummy patterns. (refer Figure 3.9.2.1.1)
 1. DRC always recognizes OPC dummy patterns as 0V.
 2. DRC will not recognize delta V value on non-OPC dummy patterns.
- The content of the “voltage text” must be a “numeral”. Any “space” & “non-numeral string” in the voltage text is not allowed and DRC will ignore these incorrect texts during voltage recognitions with a warning message at DRC error report. (refer Figure 3.9.2.1.5)

Table 3.9.1 Four types of text layers definition

Process Layer	CAD Layer #	TSMC Default Data type			
		Voltage High	Voltage High Top (highest priority)	Voltage Low	Voltage Low Top (highest priority)
OD	6	230	Not support	231	Not support
PO	17	230	Not support	231	Not support
MP	84	230	Not support	231	Not support
MD	84	236	Not support	237	Not support
M0	180	230	Not support	231	Not support
M1~M15	31~45	230	232	231	233
AP	74	230	232	231	233

(1) "Voltage High" recognition



(2) "Voltage Low" recognition

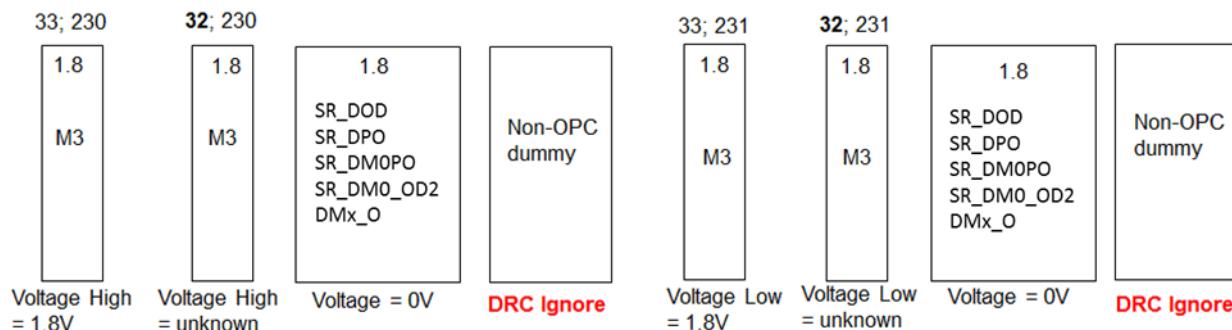


Figure 3.9.2.1.1

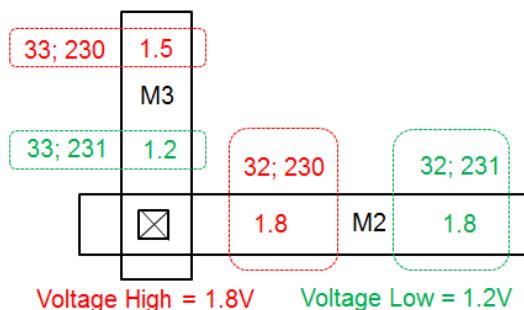


Figure 3.9.2.1.2

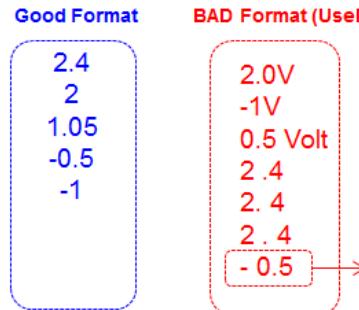
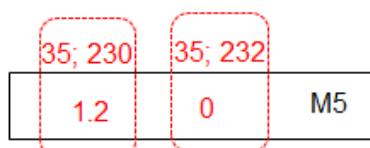
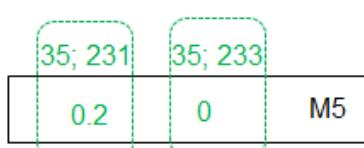


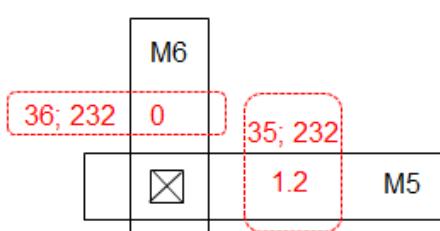
Figure 3.9.2.1.5



(a) Voltage High = 0V



(b) Voltage Low = 0V



(c) Voltage High = 0V

Figure 3.9.2.1.3

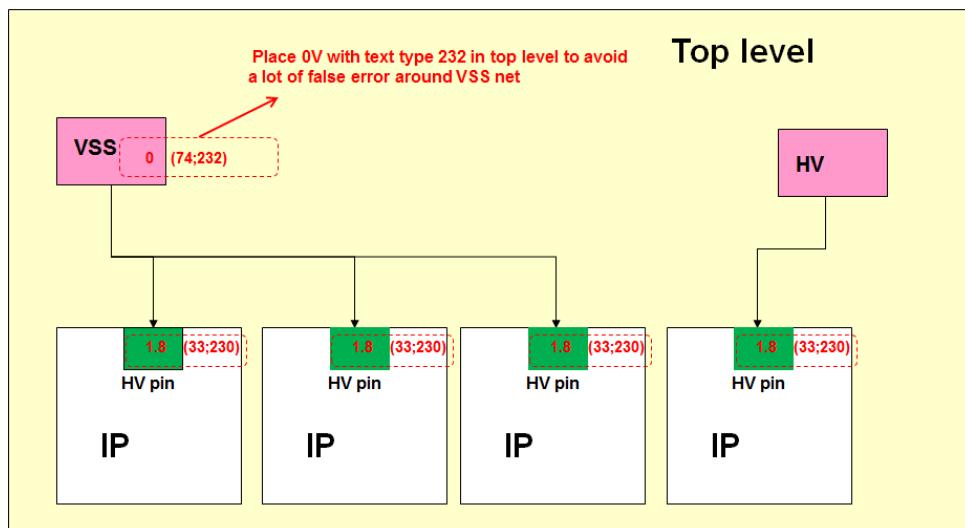


Figure 3.9.2.1.4

3.9.2.2 Usage of voltage marker layer

- Besides the usage of voltage text, to use the “voltage marker layer” of M0~M15 and MD layer is the second priority for tsmc DRC doing the voltage recognition on each net.
- The definition and usage of these voltage marker layers are listed at Table 3.9.2.
 - Only the “Voltage High” is defined with discrete voltage value in tsmc N7+ CAD layer usage. “Voltage Low” are NOT supported and not defined at tsmc N7+ CAD layer usage.
 - Each metal layer has the corresponding voltage marker layer. Each “voltage marker” layer MUST be placed on the correct corresponding layer, otherwise, DRC cannot correctly recognize the voltage markers.
e.g. if a M3 voltage marker (CAD layer: 33;218) is put on M3 (CAD layer 33;255/33;256 for Mx & 33;295/33;296 for Mxa), then this net will be recognized as 1.8V. But, it cannot be recognized correctly if it's placed on M2 (CAD layer, 32;275/32;276).
- If there are several voltage makers in a net, the maximum voltage marker layer will have higher priority for the definition of “Voltage High”, e.g. this net will be recognized as “1.8V” if there are (33;215, M3 1.5V marker) on M3 and (32;218, M2 1.8V maker) on M2.
- It is useless to draw voltage marker on OPC dummy metal. DRC always recognizes these dummy metals as 0V.

Table 3.9.2 “Voltage High” : each CAD layer has its specific voltage value.

M0~M15 (180,31~45):

DataType	200	201	202	203	204	205	206	207	208	209	210	211
Voltage	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1
DataType	212	213	214	215	216	217	218	219	220	221	222	
Voltage	1.2	1.3	1.4	1.5	1.6	1.7	1.8	2.5	3.3	5.0	7.0	

MD (84):

DataType	212	219	220
Voltage	1.2	2.5	3.3

3.9.3 Voltage Recognition Method of Connection NET

3.9.3.1 “Voltage High” recognition

Figure 3.9.3.1 is to illustrate the decision sequence of the “Voltage High” at tsmc DRC deck: the “voltage text” is the 1st priority. Therefore, to place both “Voltage High” and “Voltage Low” text layers in a net is strongly recommended.

- If there are several voltage text and voltage marker information in a net, the “Voltage High” will be recognized as the highest value of the voltage text layer. Then, if a net only has “voltage marker” information, the “Voltage High” will be recognized as the value of highest one. e.g.:
 - The “Voltage High” will be recognized as 1.5V if the net has “1.5” by M3 voltage text layer (33;230) and M3 1.8V marker layer (33;218).
 - The “Voltage High” will be recognized as 1.8V if the net only has “1.5” by M3 voltage text (33;230) and “1.8” by M2 voltage text (32;230).
 - The “Voltage High” will be recognized as 1.8V if the net only has 1.5V M3 marker (33;215) and 1.8V M2 marker (32;218).
- If your IP has multiple voltage applications, it is recommended to place the highest voltage text or marker layer on the nets. And, to follow the related delta voltage design rules to enlarge corresponding wire spaces in order to avoid unexpected DRC violations after chip implementation
- If a net is without any voltage high text/ marker layers, and connect to PW strap. The “Voltage High” will be recognized as 0.
- Once a net is without any recognitions above, DRC will check if the net connects to MOS/HV diode :
 - If not connect to any MOS/HV diode, the “Voltage High” will be recognized as 0.
 - If the net connect to MOS/HV diode, the “Voltage High” recognition will depend on the switch of
 - (1) “USE_SD_VOLTAGE_ON_CORE_TO_IO_NET”, and (2) “USE_IO_VOLTAGE_ON_CORE_TO_IO_NET”. (refer Table 3.9.3 in section 3.9.3.3)
 - (1) USE_SD_VOLTAGE_ON_CORE_TO_IO_NET: to recognize the priority of S/D and GATE since GATE’s potential is driven by other device’s S/D.
 - (a) Switch set “On”: the “Voltage High” will be the maximum operating voltage on this net by the priority (IO S/D/diode) > (core S/D) > (core GATE) > (IO GATE) > (core diode).
 - (b) Switch set “Off”: the “Voltage High” will depend on “USE_IO_VOLTAGE_ON_CORE_TO_IO_NET”
 - (2) USE_IO_VOLTAGE_ON_CORE_TO_IO_NET
 - (a) Switch set “Off”: the “Voltage High” will be the minimum operating voltage on this net.
 - (b) Switch set “On”: the “Voltage High” will be the maximum operating voltage on this net.

The examples of net voltage recognition by these two switches, and you could refer to table 3.9.3 for more details:

Connect to both core & IO MOS/Diode devices				Pre-definition for LV & HV net			
MOS*		Diode#		"USE_SD_VOLTAGE_ON_CORE_TO_IO_NET" option			
Core source (0.75V)	IO gate (1.8V)	IO drain (1.8V underdrive to 1.5V)	1.8VIO	Turn Off		Turn On	
				"USE_IO_VOLTAGE_ON_CORE_TO_IO_NET"	"USE_SD_VOLTAGE_ON_CORE_TO_IO_NET"	1.8V	1.8V
V		V	V	0.75V	0.75V	1.8V	0.75V
V	V			0.75V	0.75V	1.8V	1.8V

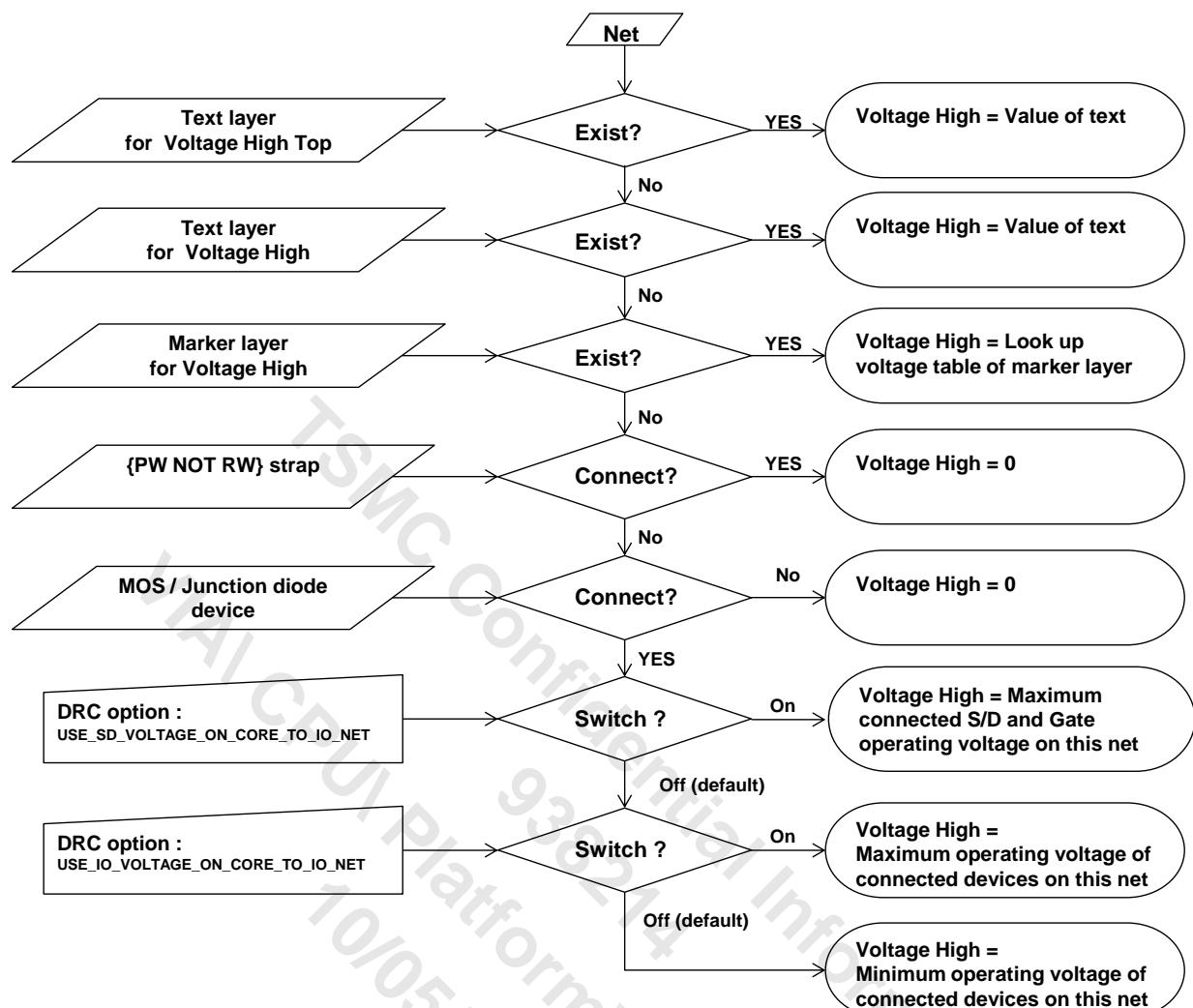


Figure 3.9.3.1 Flow of priority

3.9.3.2 “Voltage Low” recognition

- If several “Voltage Low” text layers exist in a net, the “Voltage Low” will be recognized as the lowest value of these texts.
- If the net is without “Voltage low” text layer, this net will be recognized as 0. (refer Figure 3.9.3.2)

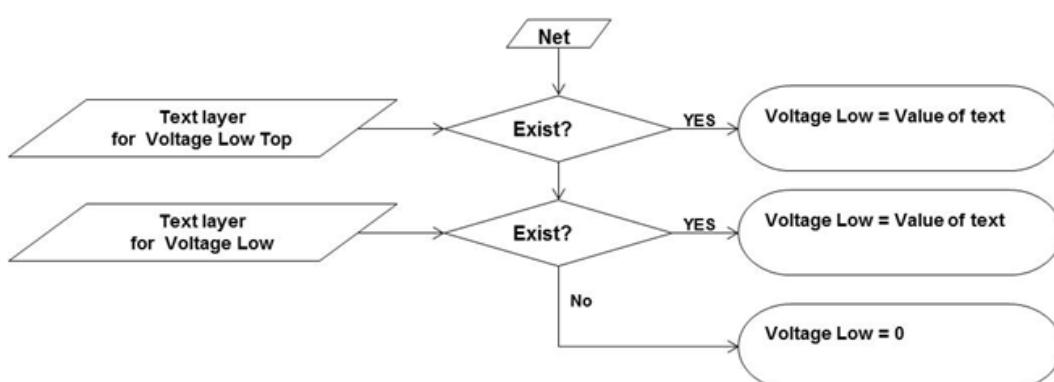


Figure 3.9.3.2 Flow of priority

3.9.3.3 Pre-definition for net without Voltage text/marker

- If a net is without any voltage high text/ marker layers, DRC will follow Table 3.9.3 to pre-define the “low voltage” and “high voltage” by the type of device component.
- Voltage text is a MUST for a net in the following two conditions: (1) the net’s intended voltage does not follow the pre-definition table, or (2) the net’s voltage range is outside RTL-compiled range (e.g., delta-V > 1.8V, like 2.5V, 3.3V...)

Table 3.9.3 Pre-defined High Voltage (HV)/ Low Voltage (LV) table by switch options:

No voltage text/marker on the net	Connection												Pre-definition for LV & HV net									
	MOS*						Diode#						"USE_SD_VOLTAGE_ON_CORE_TO_IO_NET" option				Turn ON					
	Core			IO			Core	IO	Turn off		Turn on											
	Source	Drain	Gate	Source	Drain	Gate			"USE_IO_VOLTAGE_ON_CORE_TO_IO_NET"	"USE_IO_VOLTAGE_ON_CORE_TO_IO_NET"	"USE_IO_VOLTAGE_ON_CORE_TO_IO_NET"	"USE_IO_VOLTAGE_ON_CORE_TO_IO_NET"										
Connect to core device only	V								LV		LV		LV		LV		LV					
		V							LV		LV		LV		LV		LV					
			V						LV		LV		LV		LV		LV					
						V			LV		LV		LV		LV		LV					
Connect to IO device only				V					HV		HV		HV		HV		HV					
					V				HV		HV		HV		HV		HV					
						V			HV		HV		HV		HV		HV					
							V		HV		HV		HV		HV		HV					
Connect to both core & IO MOS/Diode devices	V		V						LV		HV		HV		HV		HV					
	V			V					LV		HV		HV		HV		HV					
	V				V				LV		HV		HV		HV		HV					
		V				V			LV		HV		HV		HV		HV					
		V				V			LV		HV		HV		HV		HV					
			V			V			LV		HV		HV		HV		HV					
				V		V			LV		HV		HV		HV		HV					
				V		V			LV		HV		HV		HV		HV					
				V			V		LV		HV		HV		HV		HV					
					V		V		LV		HV		HV		HV		HV					
					V			V	LV		HV		HV		HV		HV					
						V		V	LV		HV		HV		HV		HV					
							V	V	HV		HV		HV		HV		HV					
							V	V	HV		HV		HV		HV		HV					
							V	V	HV		HV		HV		HV		HV					
							V	V	HV		HV		HV		HV		HV					
							V	V	HV		HV		HV		HV		HV					

Warnings:



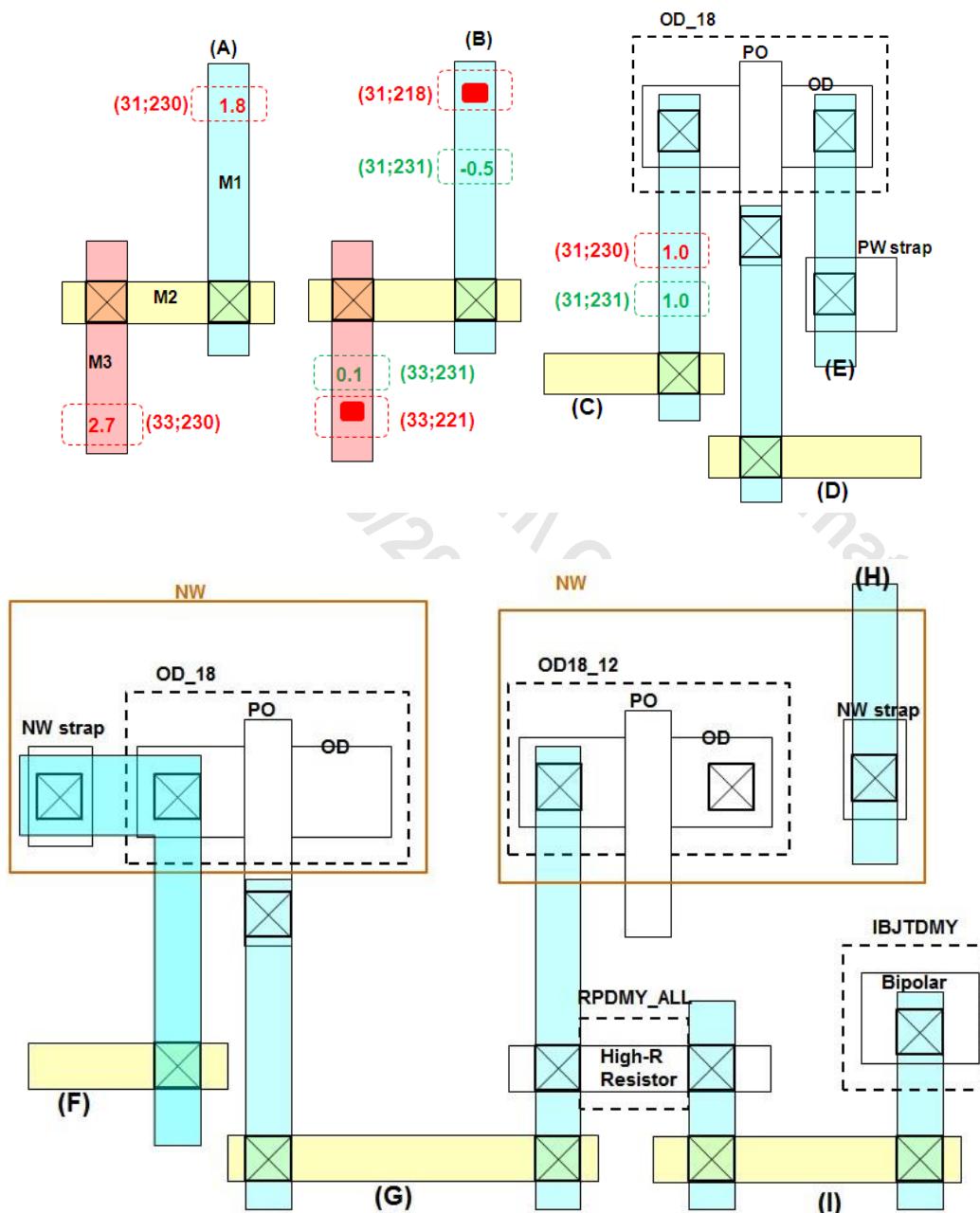
- (1) DRC LV/HV net pre-definition CANNOT correctly define voltage values for iBJT, MOM, MIM and Resistor. Voltage text is a MUST for these devices, otherwise, the nets will be defaulted as 0V
- (2) Voltage text is a MUST for a net in the following two conditions: (i) the net’s intended voltage does not follow the table’s pre-definition, or (ii) the net’s voltage range is outside RTL-compiled range (e.g., delta-V > 1.8V, like 2.5V, 3.3V...)
- (3) *: MOS include transistors, and VAR
- (4) #: Diode only include junction diode, Gated diode, and HIA diode

3.9.3.4 The examples of net voltage recognition

NET	A	B	C	D	E	F	G	H	I
Voltage High	2.7	5	1.0	1.8	0	1.8	1.2 (USE_IO_VOLTAGE_ON_CORE_TO_IO_NET option is OFF)	0*	0*
							1.8 (USE_IO_VOLTAGE_ON_CORE_TO_IO_NET option is ON)		
Voltage Low	0	-0.5	1.0	0	0	0	0	0	0

Note:

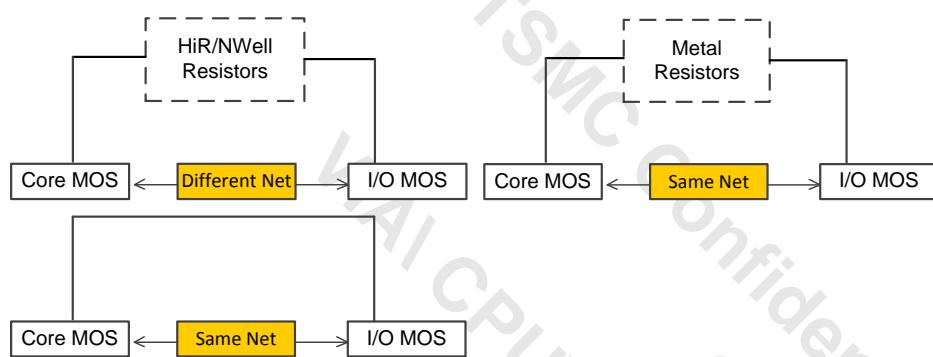
*: The Net H and Net I will be recognized as 0V , because these nets do not have any voltage text/ marker layer and do not connect to any MOS/ Junction diode.



3.9.3.5 Resistor recognition

The connection of tsmc delta voltage check will be recognized as broken by High R resistor with RPDMY_ALL and NWell resistor with {NWDMY OR NWDMY1} and not broken by metal resistor with RMDMYn (CAD layer 116;n , n = 0~15)

NET	High R Resistor	NWell Resistor	Metal Resistor
Connection of delta-V rule	Broken	Broken	Not Broken

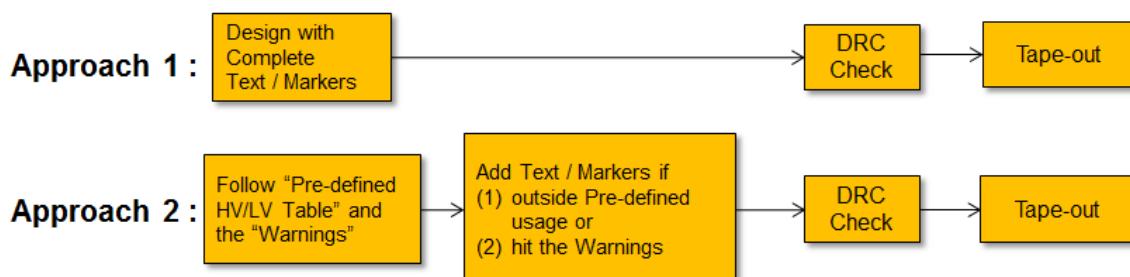


3.9.4 Suggestion Design Flow of Voltage in a Net

DRC CANNOT recognize voltage in a net correctly if no voltage text layer or voltage marker layers in it. In order to well manage your design, two approaches are recommended:

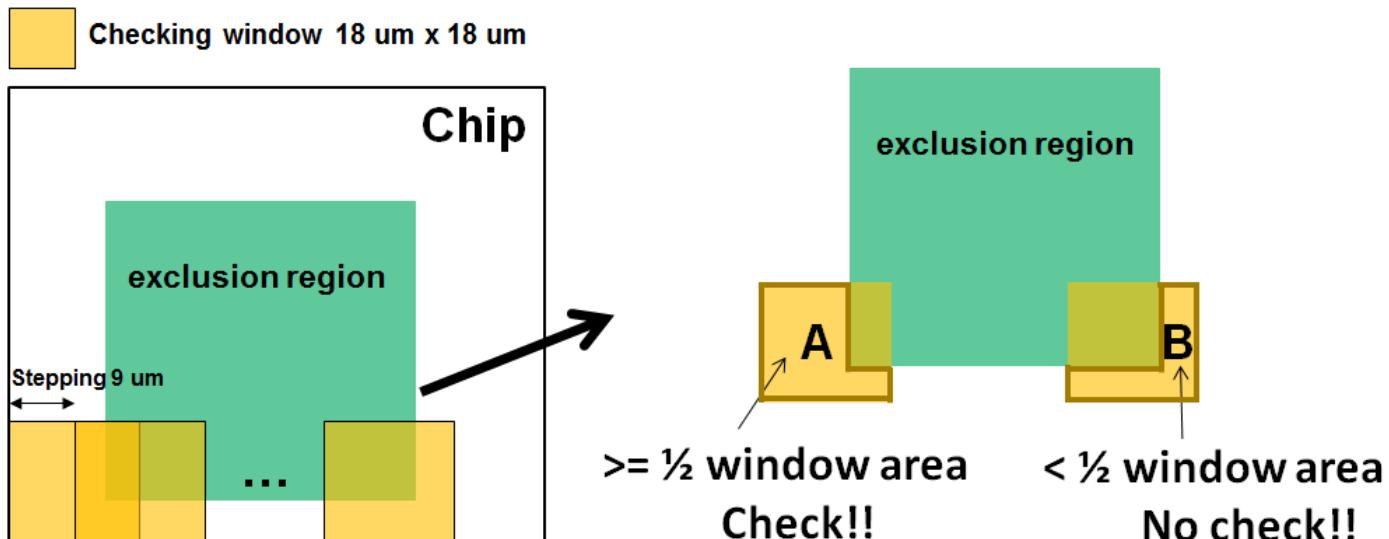
Approach-1: To make your design with complete voltage text or maker layers with DRC clean.

Approach-2: Follow table 3.9.3 pre-defined High Voltage (HV)/ Low Voltage (LV) definitions, then add voltage text/ marker layers on the net which hit the warnings. Finally, It could make the design with DRC clean.



3.9.5 DRC methodology of density exclusion

- Local density rule will be applied while the area of {checking window NOT exclusion region} $\geq 1/2$ window area.
- For example:
 - OD.DN.3.1 Minimum ALL_OD density in window 18 μm x 18 μm , stepping 9 μm (Except TCDDMY, ICOVL_SINGLE, BLK_WF, NWDMY, SEALRING_ALL)
→ DRC will have the local density check on "A". ($\geq \frac{1}{2}$ window area); while DRC will not have local density check on "B". ($< \frac{1}{2}$ window area)



4 Layout Rules and Recommendations

This chapter provides information about the following:

- 4.1 Layout Rule Conventions
- 4.2 Derived Geometries Used in Physical Design Rules
- 4.3 Definition of Layout Geometrical Terminology
- 4.4 Minimum Pitches
- 4.5 Layout Rules and Guidelines

4.1 Layout Rule Conventions

The TSMC layout rules follow these conventions:

- Unless otherwise specified, all rules specify minimum dimensions.
- The basic unit of measure is μm ; the basic unit of area is μm^2 .
- Process, product, and reliability yields should improve when designs are relaxed from minimum dimensions. Use the minimum dimensions shown only to shrink chip sizes or improve circuit performances.
- Design rules requiring exact dimensions (“=” in the rule tables) are not to be relaxed. Guidelines are grouped in a separate table.
- DFM recommendations and guidelines are designated by the symbol ® or the letter “g” after the rule numbers.
- When the letter U in superscript (U) is used after a rule number, the rule is not checked by the DRC.
- Different kinds of bracket punctuations are used in the rules for different purposes as follows:
 - Parentheses () are used for explanation.
 - Square brackets [] are used for certain conditions.
 - Curved brackets { } indicate that an operation is performed.
- Background color of rule table identifies ground rule within rule group and separates rule groups to help user reading.

4.2 Derived Geometries Used in Physical Design Rules

4.2.1 Derived Geometries

Term	Definition
NW1V	{NW OUTSIDE OD2} (Notes)
NW2V	{NW NOT OUTSIDE OD2} (Notes)
PW	{NOT NW}
FIELD	{NOT {OD OR SR_DOD}}
FIELD PO	{PO NOT {OD OR SR_DOD}}
ALL_OD	{OD OR SR_DOD}
N+OD	{NP AND OD}
P+OD	{PP AND OD}
ACTIVE	{N+ ACTIVE OR P+ ACTIVE}
N+ ACTIVE (NACT)	{NP AND OD} NOT NW}
P+ ACTIVE (PACT)	{PP AND OD} AND NW}
ACT (ACTIVE)	{NACT OR PACT}
CrtNACT	{ALL_OD AND NP} NOT NW}
CrtPACT	{ALL_OD AND PP} AND NW}
CrtACT	{CrtNACT OR CrtPACT}
SrNACT	{SR_DOD AND NP} NOT NW}
SrPACT	{SR_DOD AND PP} AND NW}
SrACT	{SrNACT OR SrPACT}
STRAP	{NWSTRAP OR PWSTRAP}
NWSTRAP	{NP AND OD} AND {NW NOT {NW INTERACT NWDMY}}}}
PWSTRAP	{PP AND OD} NOT NW}
OD2	{OD_18 OR OD_15}
NWRSTI	{NW INTERACT {{NW AND NWDMY} NOT OD}}
ALL_PO	{PO OR SR_DPO}
GATE	{PO AND OD}
TrGATE	{GATE NOT {PODE_GATE OR CPODE}}
NGATE	{PO AND OD} AND NP} NOT NW}
PGATE	{PO AND OD} AND PP} AND NW}
CrtNGATE	{CrtPO AND OD} AND NP} NOT NW}
CrtPGATE	{CrtPO AND OD} AND PP} AND NW}
CrtGATE	{CrtNGATE OR CrtPGATE}
SrNGATE	{SR_DPO AND OD} AND NP} NOT NW}
SrPGATE	{SR_DPO AND OD} AND PP} AND NW}
SrGATE	{SrNGATE OR SrPGATE}
VarNGATE	{PO AND OD} AND NP} AND NW} AND VAR}
VarPGATE	{PO AND OD} AND PP} NOT NW} AND VAR}
VarGATE	{VarNGATE OR VarPGATE}
ALL_MD	{MD OR SR_DMD}
ALL_CMD	{CMD OR SR_DCMD}
ALL_MP	{MP OR SR_DMP}
ALL_CPO	{CPO OR SR_DCPO}
TPO	TPO_2
TCDDMY	TCDDMY1
DmyVIAn	{DVIAn OR DVIAn_O}
DmyMn	{DMn OR DMn_O}
CTMFFINAL	{CTM NOT CTM_O}
CBMFFINAL	{CBM NOT CBM_O}

4.2.2 Special Definition

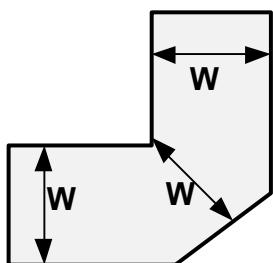
Term	Definition
NW	N-WELL
PW	P-WELL
RW	NW hole in DNW
MOS	Transistor structure consisting of a source, a drain, and a gate
NMOS	N type MOS
PMOS	P type MOS
SR_DOD	Dummy OD
SR_DPO	Dummy PO
DMn	Dummy Metal
DMn_O	OPC dummy metal. The rules of DMn_O are the same as real metal, Mn
CHIP	GDS EXTENT or GDS bounding box
Seal-ring enhanced zone	The region between the seal-ring and Chip_Boundary
ENDCAP	The PO extension of a transistor gate in the width direction onto the field
CB	Passivation opening for wire bond design
CBD	Passivation opening for flip chip design
RV	Redistribution VIA for connecting AP-MD with Mtop
CB2_FC	Passivation 2 opening for flip chip
CB2_WB	Passivation 2 opening for wire bond
AP	Al pad metal layer after CB or CBD in Cu process
AP RDL	Al pad redistribution layer
PM	Polyimide opening
UBM	Under bump metallurgy
A~B	A ≤ rule value ≤ B
PRL	Parallel run length
Line-end (end)	Layer edge width ≤ W µm [edge formed by 2 consecutive 90-90 degree convex corners] W value is defined in each layer
Run	Layer edge except Layer line-end edge
Lower_Metal/VIA	Intermediate under layer of metal/VIA EX: Lower_Metal of VIA3 is M3. Lower_VIA of VIA3 is VIA2.
Upper_Metal/VIA	Intermediate upper layer of metal/VIA EX: Upper_Metal of M2 is M3. Upper_VIA of M2 is VIA2.

4.2.3 Collective Layers

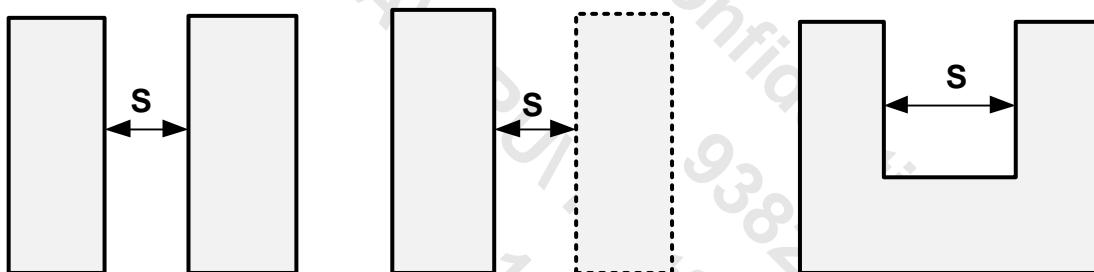
Term	Definition
VT	VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P
Dummy_Cell	DC3, DC2_MANDREL, DC2_CORE, DC4_CORE, DC6_1, DC2_IO, DC4_IO, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2
DC_Mandrel	DC3, DC2_MANDREL
DC_PO36	DC2_CORE, DC4_CORE, DC6_1
DC_Core	DC3, DC2_MANDREL, DC2_CORE, DC4_CORE, DC6_1
DC_IO	DC2_IO, DC4_IO
DC_WPO	DC6_2, DC5_1, DC5_2
DC_WO_IMP	DC2_MANDREL, DC2_CORE, DC4_CORE, DC6_1, DC2_IO, DC4_IO, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2
DC_PO	DC3, DC2_MANDREL, DC2_CORE, DC4_CORE, DC6_1, DC2_IO, DC4_IO, DC6_2, DC5_1, DC5_2
DC_OD_WONP	DC2_MANDREL, DC2_CORE, DC4_CORE, DC2_IO, DC4_IO, DC6_1, DC6_2
TCDDMY_Mn	TCDDMY_M0, TCDDMY_M1, TCDDMY_M2, TCDDMY_M3, TCDDMY_M4, TCDDMY_M5, TCDDMY_M6, TCDDMY_M7, TCDDMY_M8, TCDDMY_M9, TCDDMY_M10, TCDDMY_M11, TCDDMY_M12, TCDDMY_M13, TCDDMY_M14, TCDDMY_M15
TCDDMY_Vn	TCDDMY_V0, TCDDMY_V1, TCDDMY_V2, TCDDMY_V3, TCDDMY_V4, TCDDMY_V5, TCDDMY_V6, TCDDMY_V7, TCDDMY_V8, TCDDMY_V9, TCDDMY_V10, TCDDMY_V11, TCDDMY_V12, TCDDMY_V13, TCDDMY_V14
NWDMY	NWDMY1, NWDMY2

4.3 Definition of Layout Geometrical Terminology

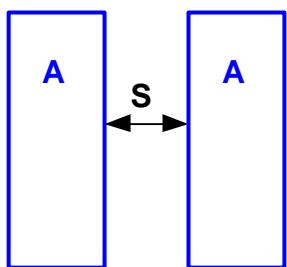
Width: Distance of interior-facing edge for single layer. (W)



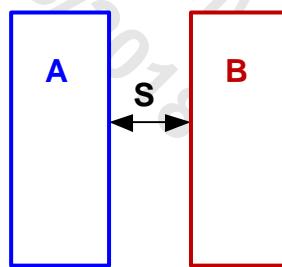
Space: Distance of exterior-facing edge for one or two layer (S)



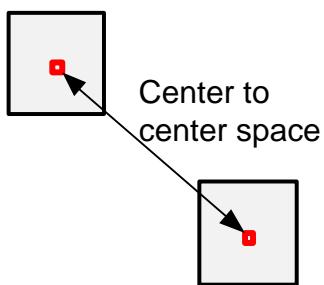
Space of A



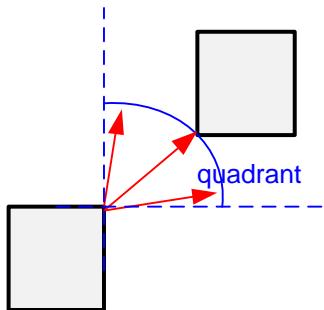
Space of A to B



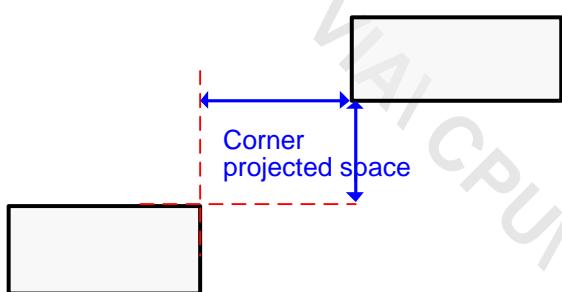
Center to center space: Distance of two centers of two square polygons



Corner space: Shortest distance of two square or rectangular polygons within quadrant

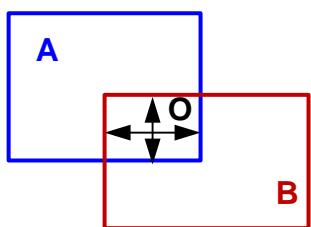


Corner projected space: Shortest distance between one corner and extended edges from other corner

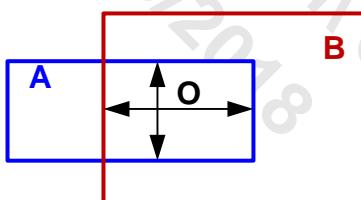


Overlap: Overlap of two layers (O)

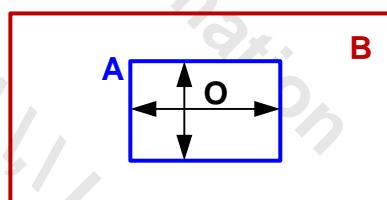
A overlap B



A overlap B

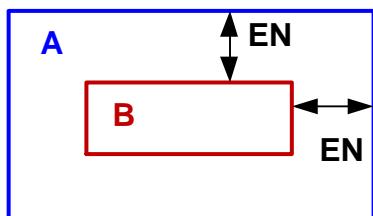


A overlap B

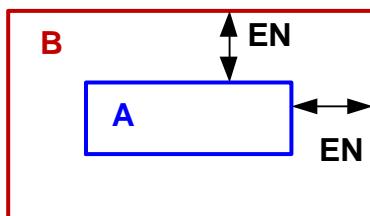


Enclosure: Distance of inside edge to outside edge (Fully inside) (EN)

A enclosure of B

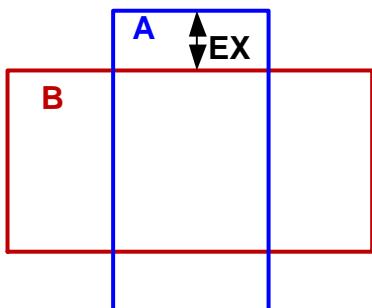


B enclosure of A

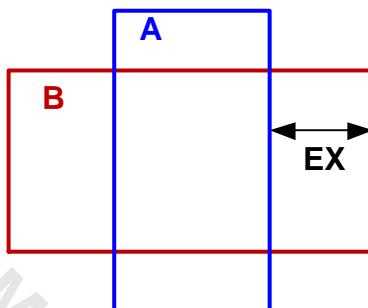


Extension: Distance of inside edge to outside edge (EX)

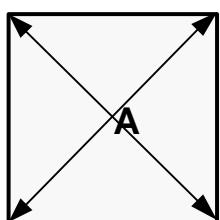
A extension on B



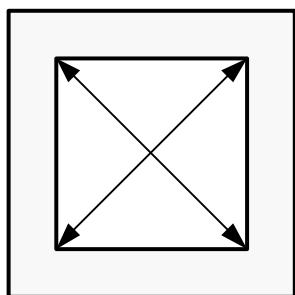
B extension on A



Area (A)

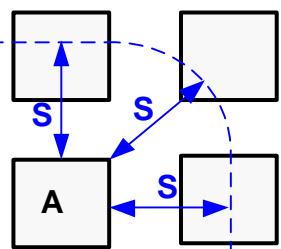


Enclosed Area

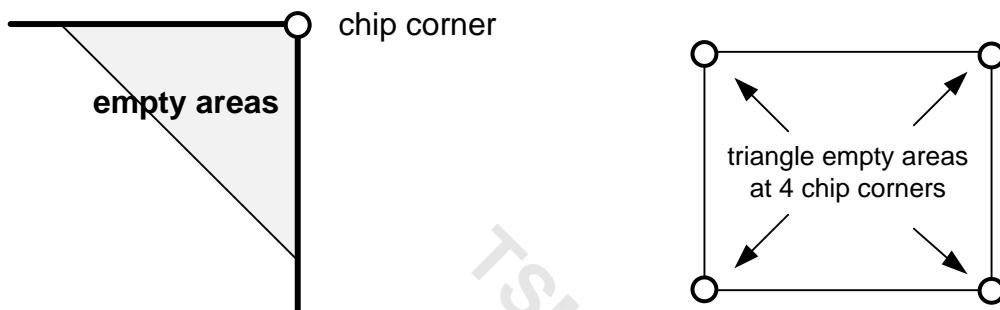


3-Neighboring

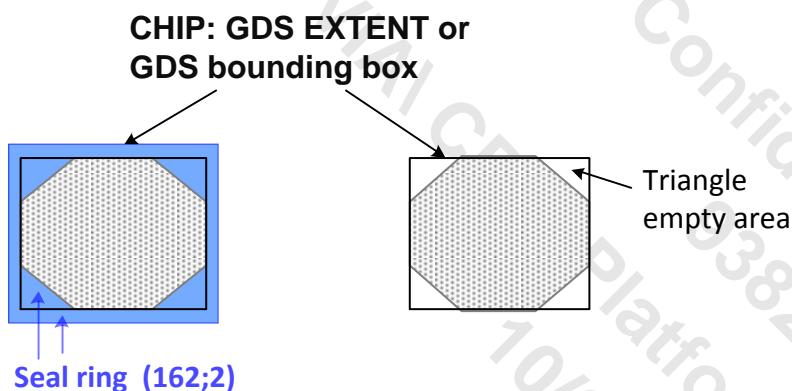
3- neighboring A (distance < S)



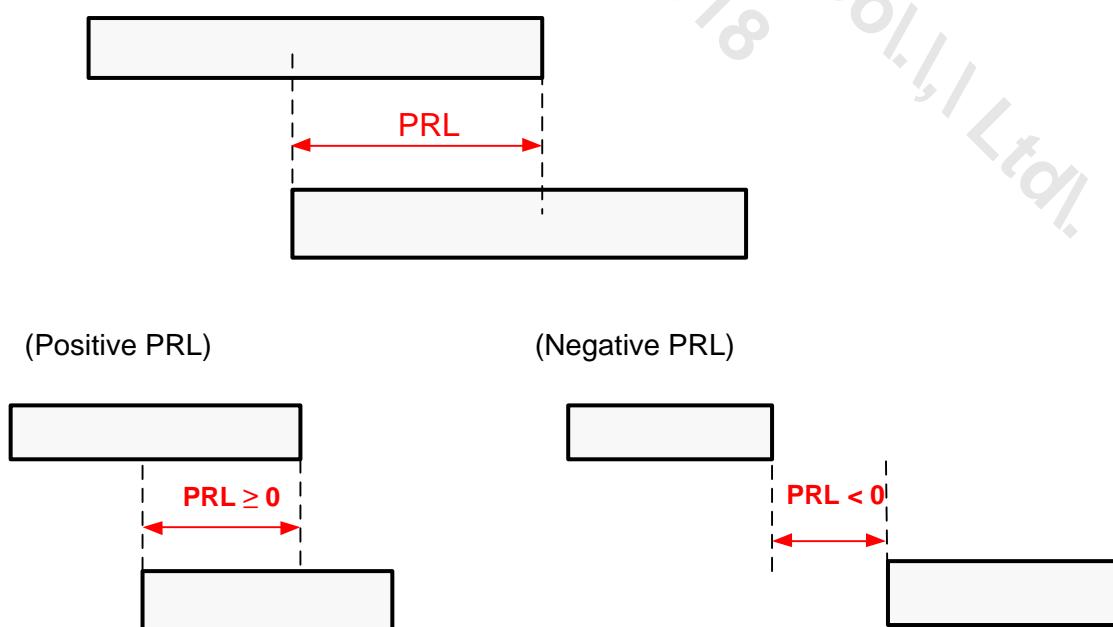
Chip corner triangle empty areas: triangle empty areas at 4 chip corners. If sealring is added by tsmc, these regions must be reserved and no layout is allowed inside

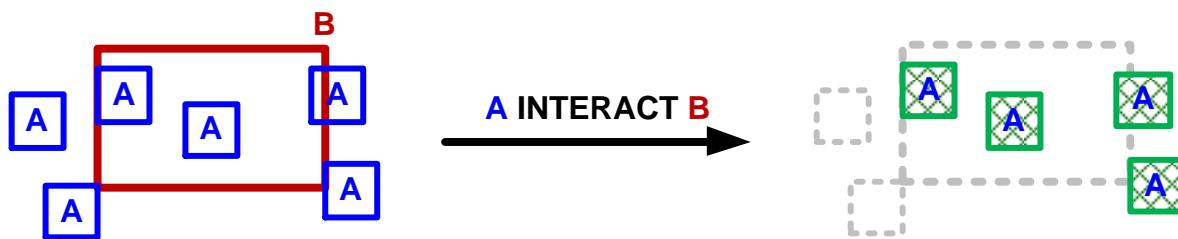
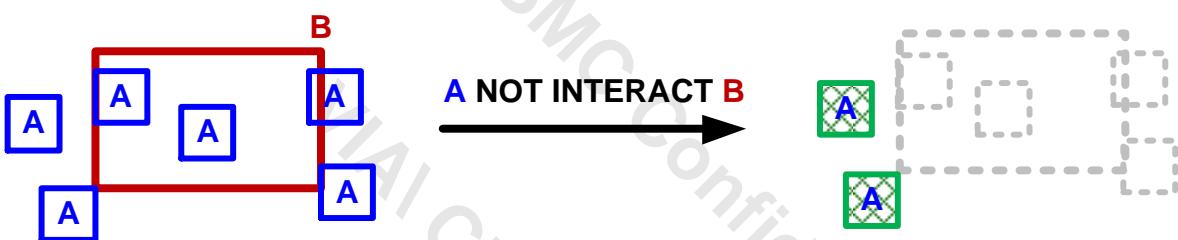
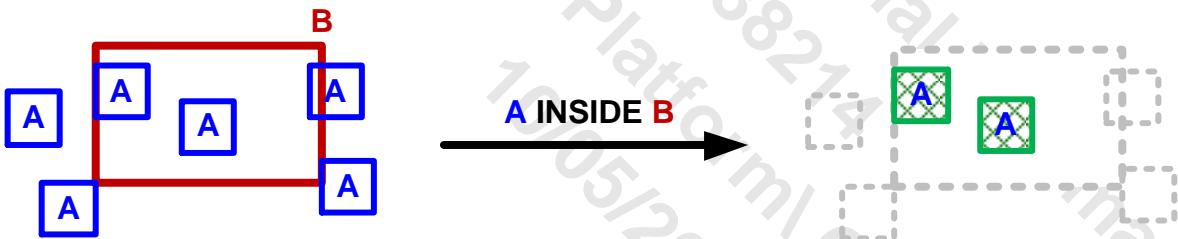
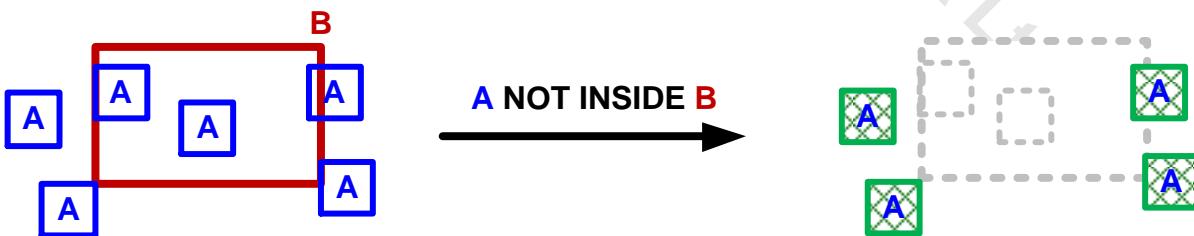


CHIP:

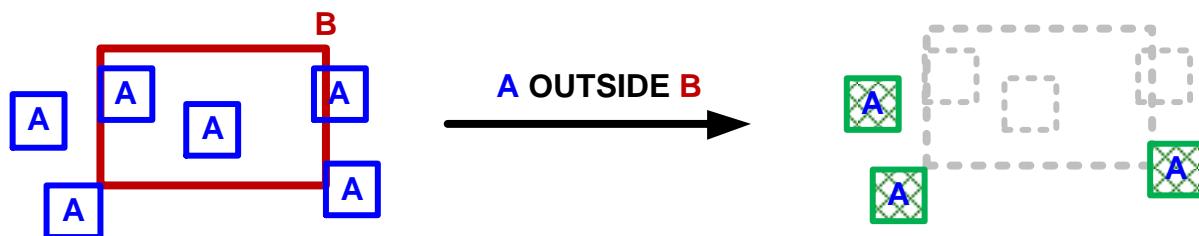


Parallel run length (PRL) : projection length between two polygon

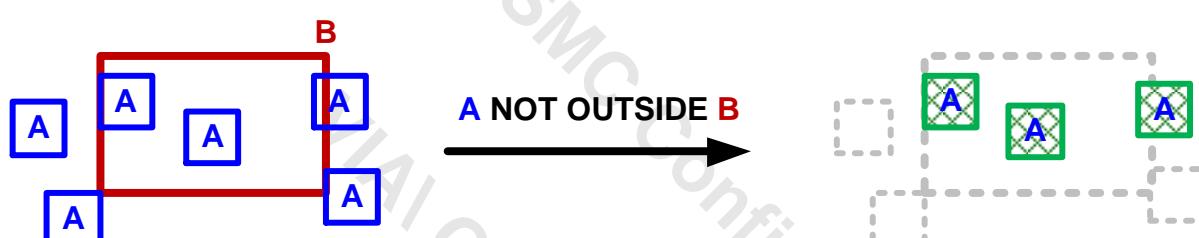


INTERACTNOT INTERACTINSIDENOT INSIDE

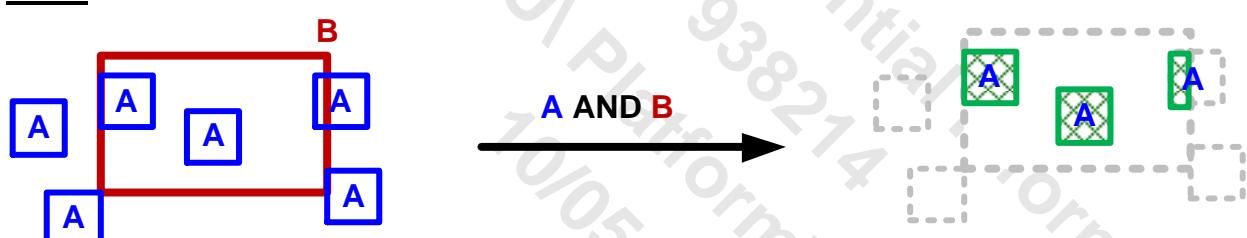
OUTSIDE



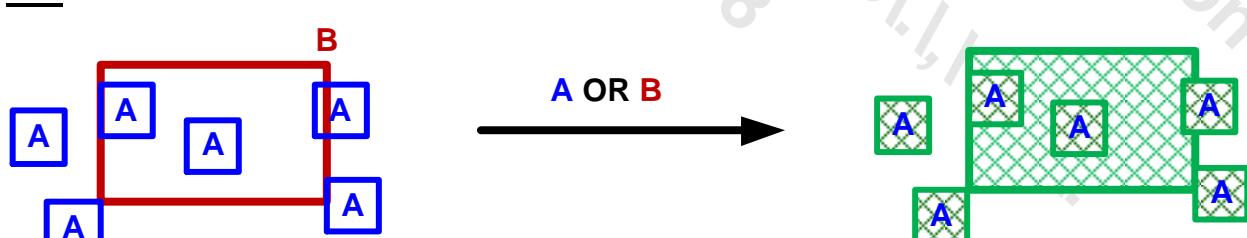
NOT OUTSIDE



AND

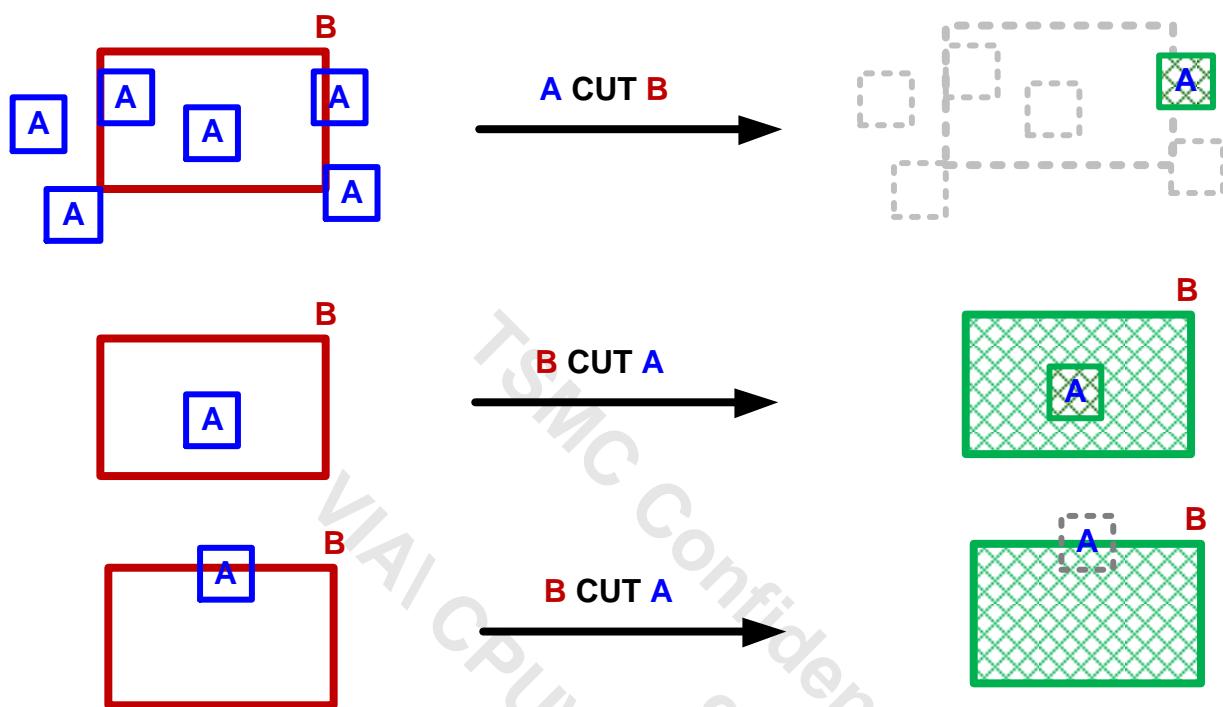
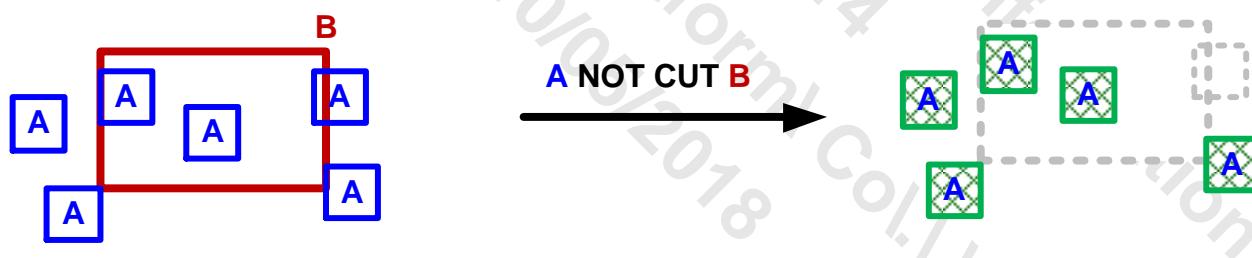
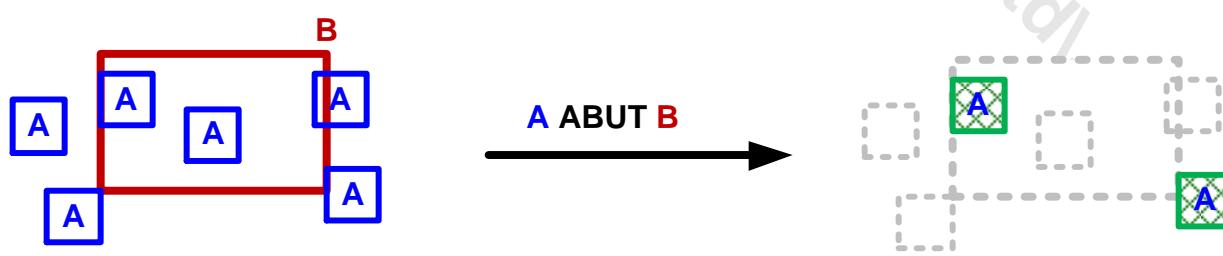


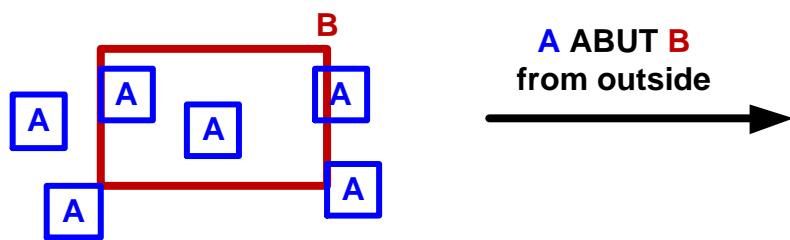
OR



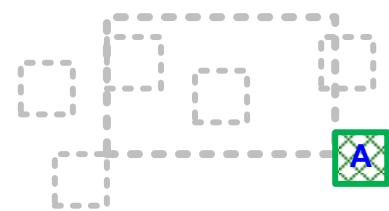
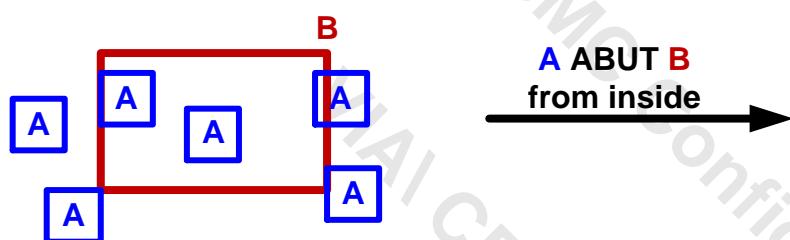
The information contained herein is the exclusive property of TSMC and shall not be distributed, copied, reproduced, or disclosed in whole or in part without prior written permission of TSMC.

62 of 1153

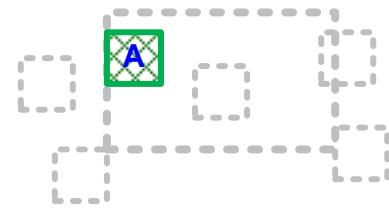
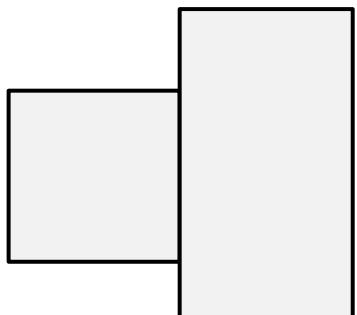
CUTNOT CUTABUT

ABUT from outside

A ABUT B
from outside

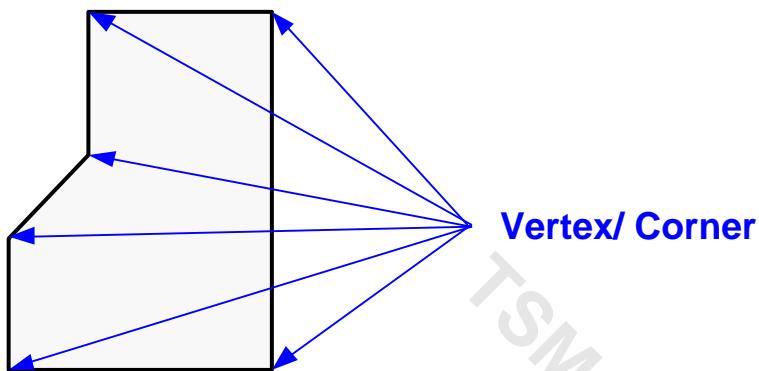
ABUT from inside

A ABUT B
from inside

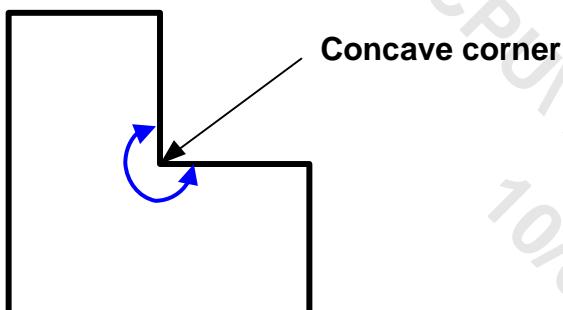
Butted

TSMC Confidential Information
938214
10/05/2018

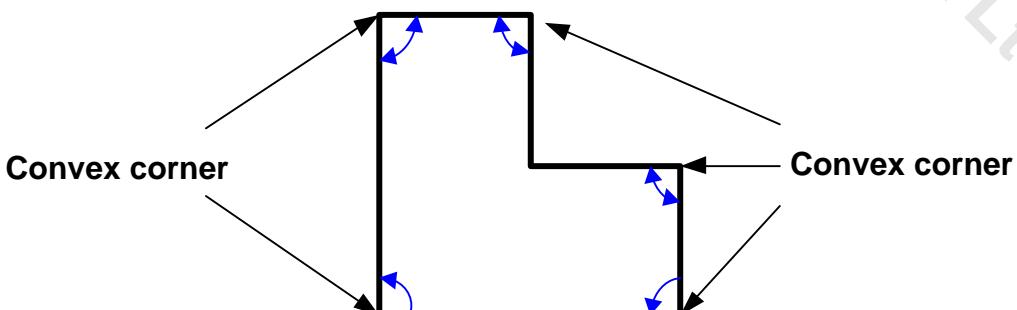
Vertex/ Corner: Polygon whose edge forms an angle, angle measured through the polygon interior

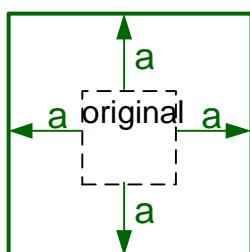
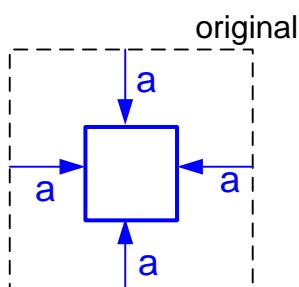
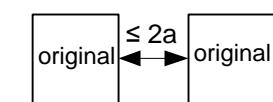


Concave corner: two edges join at corner and the angle between the edges, measured through the polygon interior, > 180 degrees

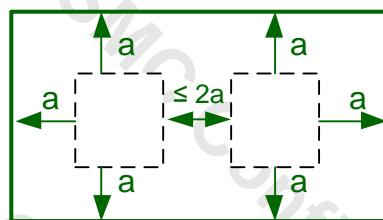


Convex corner: two edges join at corner and the angle between the edges, measured through the polygon interior, < 180 degrees

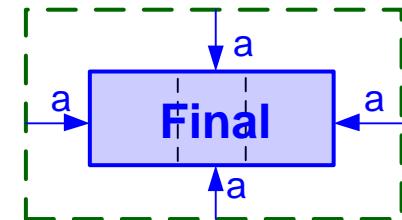
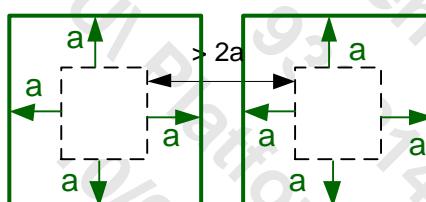
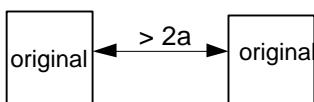
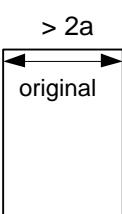


SIZING a**SIZING - a****SIZING up/down a**

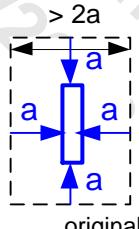
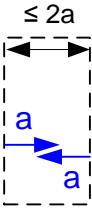
Sizing up a



Sizing down a

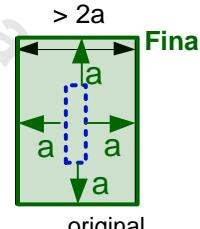
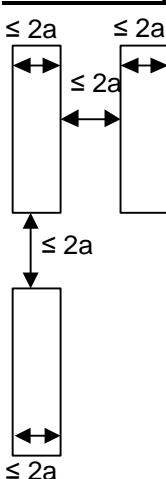
**SIZING down/up a**

Sizing down a

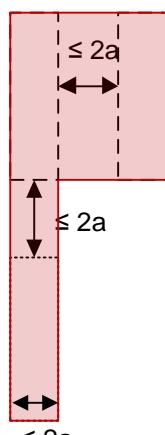


Sizing up a

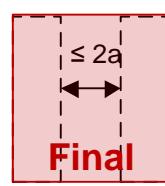
Empty

**SIZING up/down/down/up a**

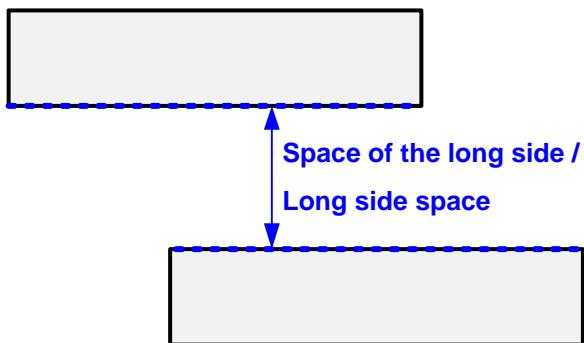
Sizing up/down a



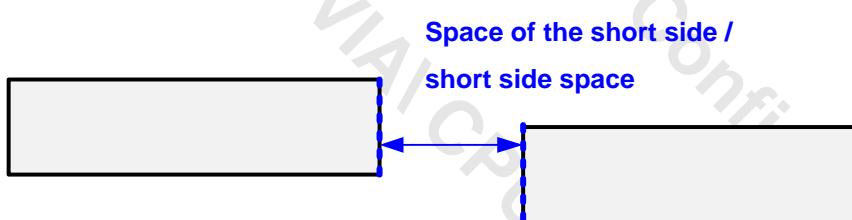
Sizing down/up a



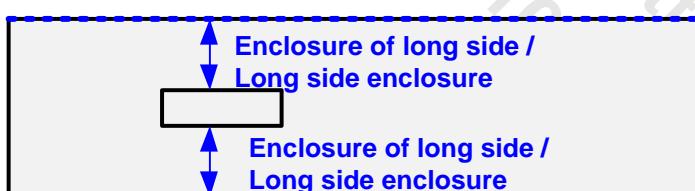
Space of long side / Long side space



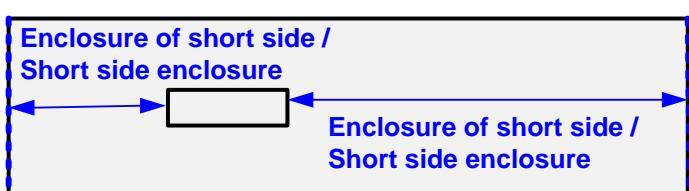
Space of short side / Short side space



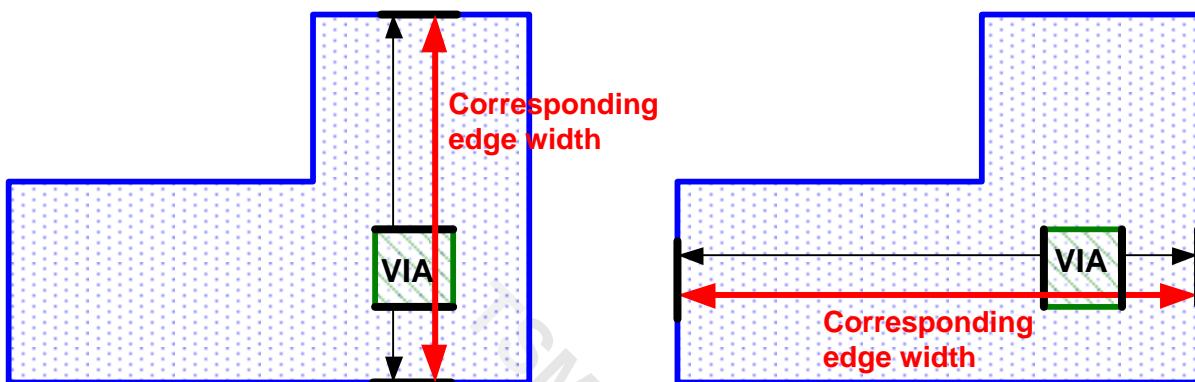
Enclosure of long side / Long side enclosure



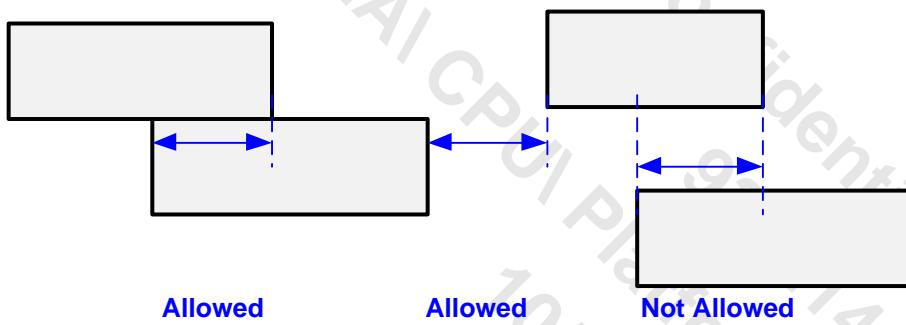
Enclosure of short side / Short side enclosure



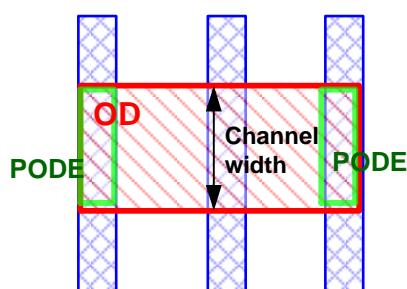
Corresponding edge width



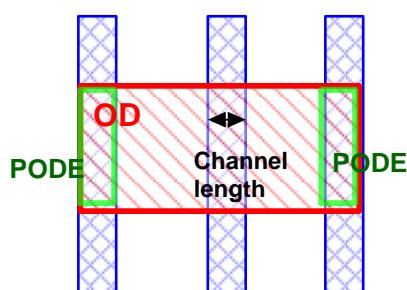
One track



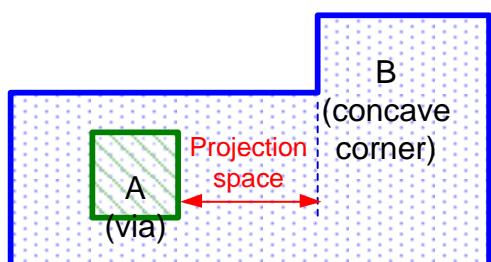
Channel width



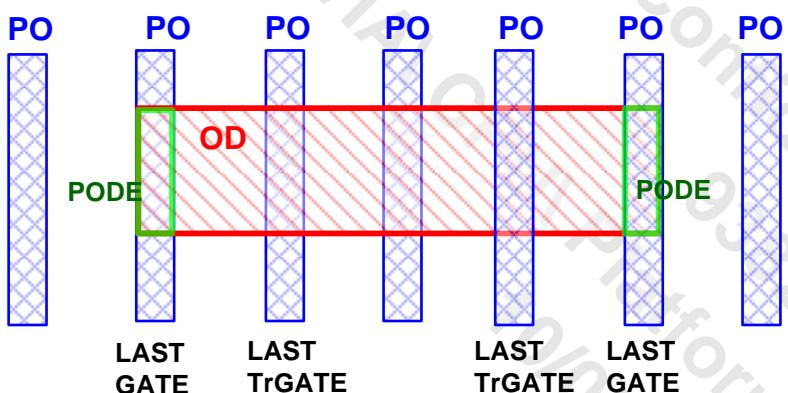
Channel length



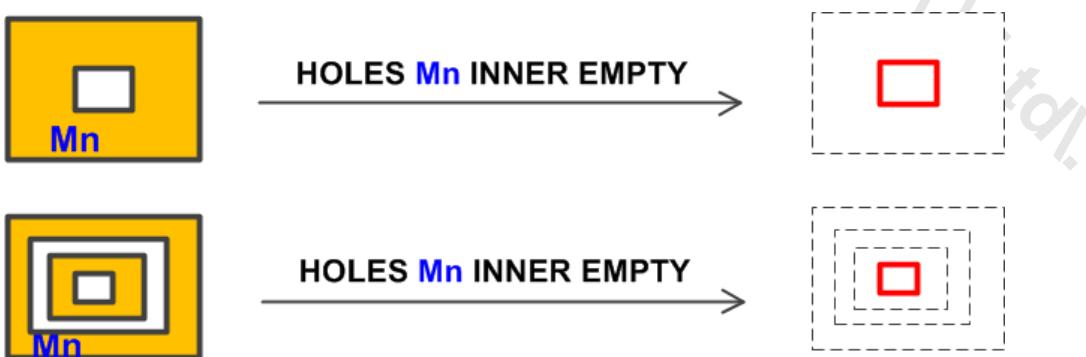
Projection space between A and B

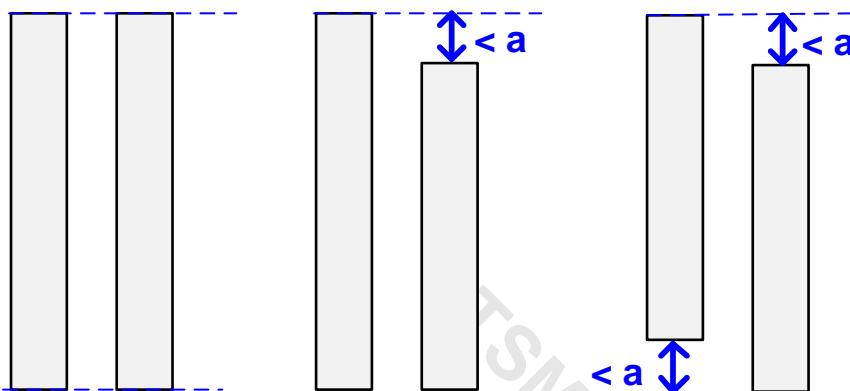
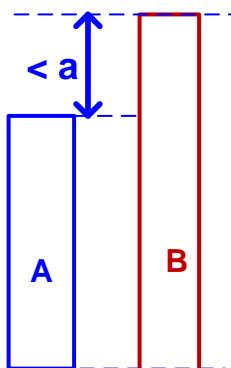
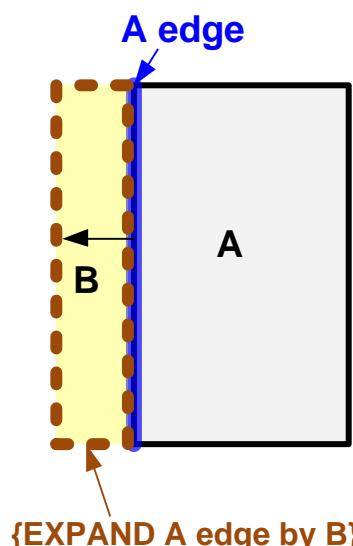


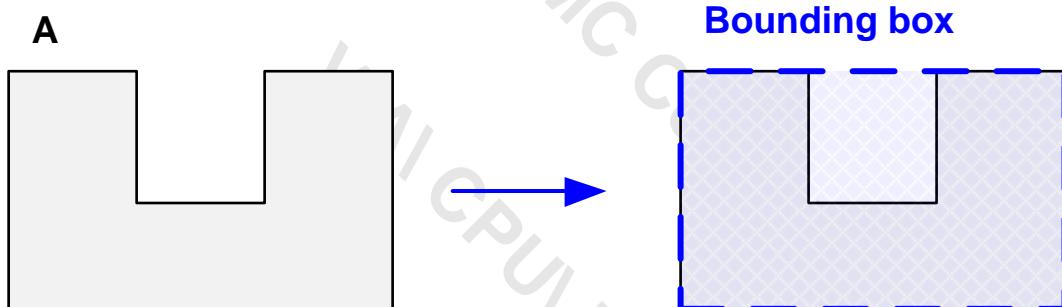
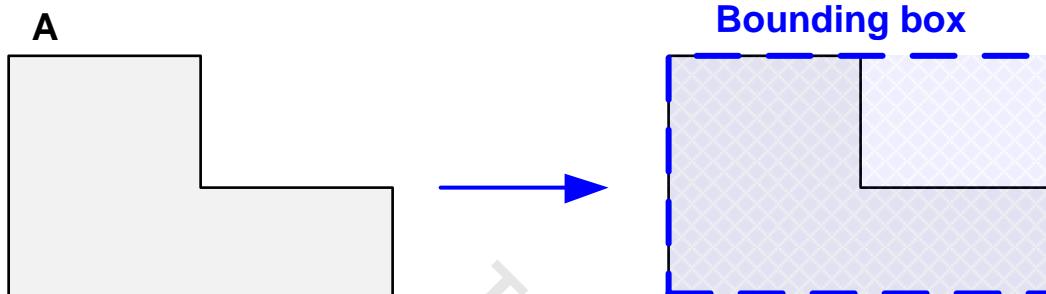
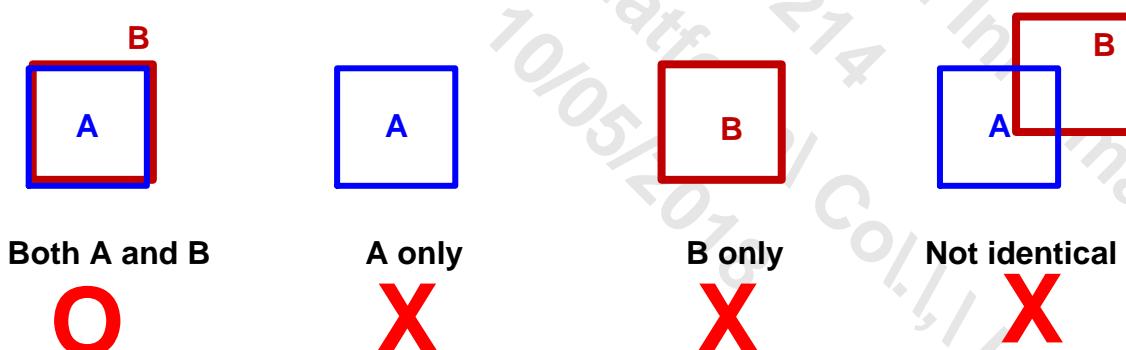
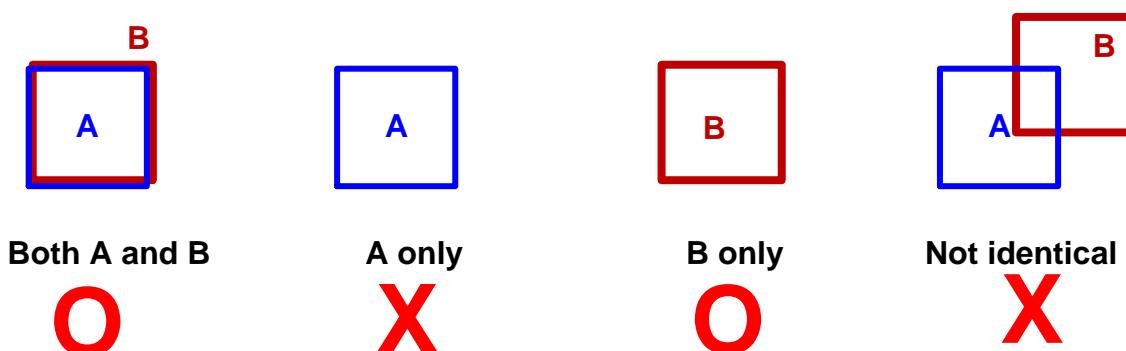
LAST GATE & LAST TrGATE

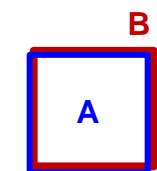


HOLES Mn INNER EMPTY



Projection-Length-Difference < aB Projection Length Difference on A < a (a must > 0)EXPAND A edge by B

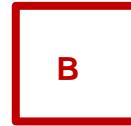
Bounding boxA and B must be drawn identicallyA must be drawn identically to B

A [INTERACT B] must be drawn identically to B

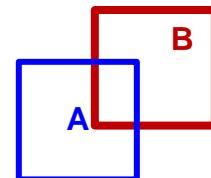
Both A and B



A only



B only

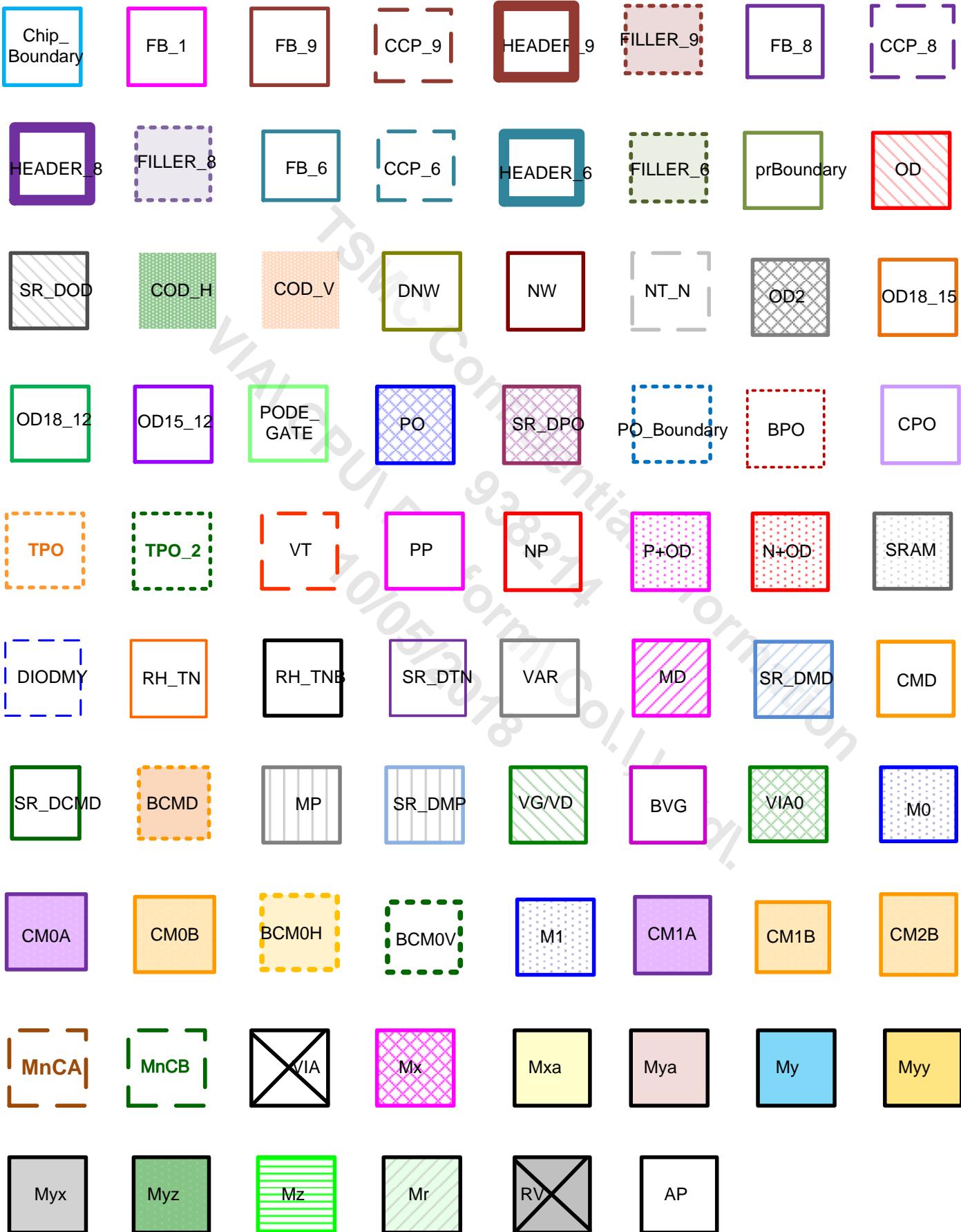


Not identical



VIAI CPU\Platform\ Col., I Ltd.
938214
10/05/2018

Pattern definitions of design layers



4.4 Minimum Pitches

Definition of Layout Geometrical Terminology

Layer	CLN07 (Unit: μm)
OD transistor pitch	0.120 (W/S=0.038/0.082)
PO interconnect pitch (on STI)	0.057 (W/S=0.008/0.049)
PO interconnect width	0.008
PO transistor pitch (on OD)	0.057 (W/S=0.008/0.049)
Minimum channel length of a transistor	0.008
Minimum channel width of a transistor	0.038
N+/P+ OD spacing	0.082
MD pitch	0.057 (W/S=0.024/0.033)
M0 pitch	0.040 (W/S=0.020/0.020)
M1 pitch	0.038 (W/S=0.020/0.018)
Mxs pitch (in MINP direction)	0.040 (W/S=0.020/0.020)
Mx pitch (in MINP direction)	0.040 (W/S=0.020/0.020)
Mxa pitch (in MINP direction)	0.040 (W/S=0.020/0.020)
Mya pitch (in MINP direction)	0.076 (W/S=0.038/0.038)
My pitch (in MINP direction)	0.076 (W/S=0.038/0.038)
Myy pitch	0.126 (W/S=0.062/0.064)
Myx pitch	0.252 (W/S=0.126/0.126)
Myz pitch	0.360 (W/S=0.180/0.180)
Mz pitch	0.720 (W/S=0.360/0.360)
Mr pitch	0.900 (W/S=0.450/0.450)
VIA0 pitch (square)	0.064 (W/S=0.020/0.044)
VIAxs pitch (square)	0.064 (W/S=0.020/0.044)
VIAx pitch (square)	0.064 (W/S=0.020/0.044)
VIAxa pitch (square)	0.114 (W/S=0.020/0.094)
VIAya pitch (square)	0.114 (W/S=0.020/0.094)
VIAy pitch (square)	0.114 (W/S=0.038/0.076)
VIAyy pitch	0.126 (W/S=0.062/0.064)
VIAyz pitch	0.360 (W/S=0.180/0.180)
VIAyx pitch	0.252 (W/S=0.126/0.126)
VIAz pitch	0.810 (W/S=0.324/0.486)
VIAr pitch	1.008 (W/S=0.414/0.594)

4.5 Layout Rules and Guidelines

4.5.1 Chip Boundary Layout Rules



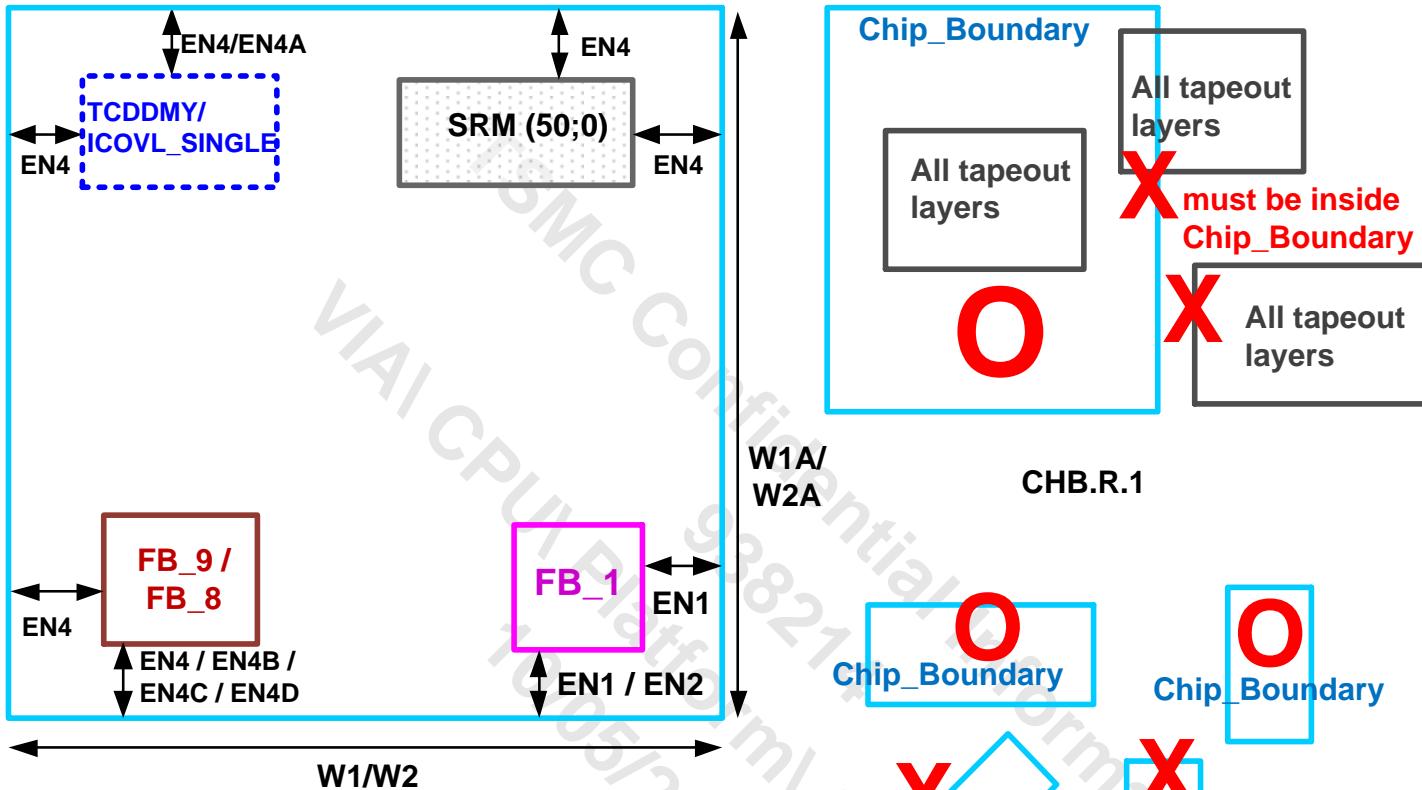
Warning: Please be notified that "window size" or "chip size" have to be (0.120^*n) μm in tsmc "iTapeout" system.

Chip_Boundary (CAD layer: 108;250) is used to define chip area without SEALRING_ALL (162;2).
DRC checks all CHB rules (exclude CHB.R.1.1) in chip level only. $n \geq 0$ and n is integer.

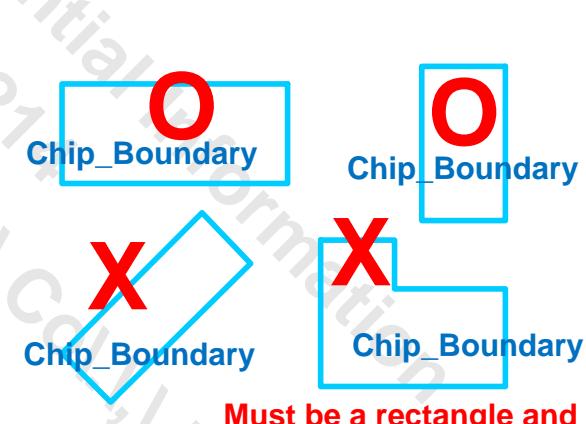
Rule No.	Description	Label	Op.	Rule
CHB.W.1	Width in chip level	W1	\geq	0.4000
CHB.W.1.1	Width in vertical direction in chip level	W1A	$=$	$0.4800+0.1200^*n$
CHB.W.2	Maximum width of Chip_Boundary with seal ring in horizontal direction Definition of Sx follows Chapter 6.5.1	W2	\leq	$26000-Sx^*2$
CHB.W.2.1	Maximum width of Chip_Boundary with seal ring in vertical direction Definition of Sy follows Chapter 6.5.1	W2A	\leq	$33000-Sy^*2$
CHB.EN.1	Enclosure of FB_1, prBoundary, PO_Boundary in chip level	EN1	\geq	0
CHB.EN.2	Enclosure of FB_1 in vertical direction in chip level	EN2	$=$	$0.1310+0.0300^*n$
CHB.EN.4	Enclosure of {{TCDDMY OR TCDDMY_Mn} OR ICOVL_SINGLE} OR SRM (50;0)} in chip level	EN4	\geq	2
CHB.EN.4.0	Enclosure of {FB_9 OR FB_8} in chip level	EN4	\geq	0.9000
CHB.EN.4.1	Enclosure of {TCDDMY OR ICOVL_SINGLE} in vertical direction in chip level	EN4A	$=$	$2.0100+0.0300^*n$
CHB.EN.4.2	Enclosure of FB_9 in vertical direction in chip level	EN4B	$=$	$0.9000+0.1200^*n$
CHB.EN.4.3	Enclosure of FB_8 in vertical direction in chip level	EN4C	$=$	$0.9300+0.1200^*n$
CHB.R.1	All tapeout layers must be inside Chip_Boundary in chip level (Except SEALRING_ALL) DRC flags {{CHIP NOT SEALRING_ALL} NOT Chip_Boundary}			
CHB.R.1.1	Following layers must be used accordingly 1. OD_SRAM1, CPO_SRAM, PO_SRAM2, PO_SRAM3, MD_A, MD_B, CO_SRAM, CO_SRAMn ($n = 11\sim60$), MP_A, MP_B, TPO_1, BLK_WF must be inside SRM. 2. CM0B_1, CM0B_2, BLK_WB, SRAMDMY_1, SRAMDMY_2, RODMY, SRM_1, SRM_2, SRM_n ($n = 5\sim25$) must be inside SRAMDMY. 3. OD_DA, COD_H, COD_V must be inside {SEALRING_ALL OR SRM}. 4. WPOM, POMM, LMARK must be inside SEALRING_ALL. 5. DCOD_H, DCOD_V must be inside Dummy_Cell. 6. ODMUO, POMUO, WPOUO, CPO_A, CPO_B, CMD_A, CMD_B, GCOD_H, GCOD_V is not allowed.			
CHB.R.2	Chip_Boundary must be a rectangle orthogonal to grid in chip level			
CHB.R.3	One and only one Chip_Boundary in a chip is a must in chip level			
CHB.R.4	SEALRING_ALL inner orthogonal edges must abut Chip_Boundary in chip level			

Chip_Boundary

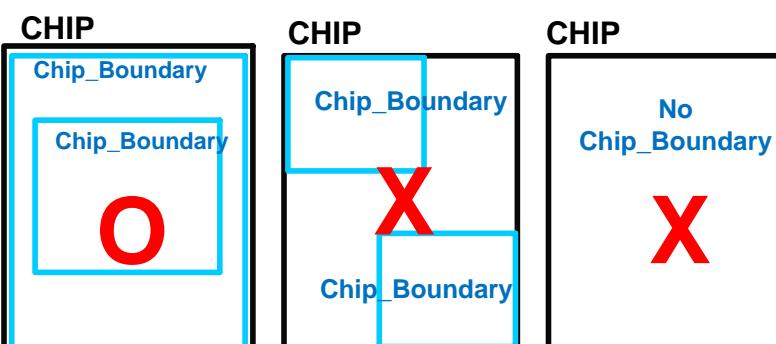
Chip_Boundary



CHB.W.1 / CHB.W.1.1 / CHB.W.2 / CHB.W.2.1 /
CHB.EN.1 / CHB.EN.2 / CHB.EN.4 / CHB.EN.4.1 /
CHB.EN.4.2 / CHB.EN.4.3

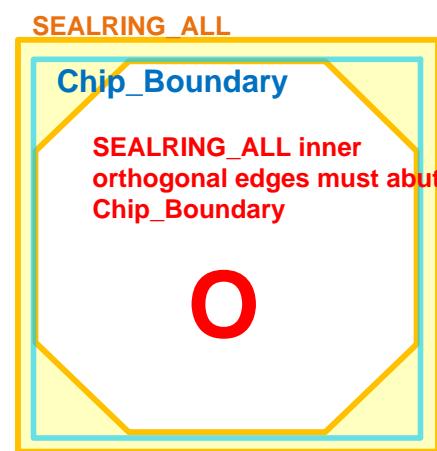


CHB.R.2



One and only one Chip_Boundary in a chip is must

CHB.R.3



CHB.R.4

4.5.2 FinFET Boundary Layout Rules

FinFET_Boundary_9 (CAD layer: 250;28, or FB_9) is used for standard cell height = 0.240 μm ($Lg \leq 0.011 \mu\text{m}$).

FinFET_Boundary_8 (CAD layer: 250;8, or FB_8) is used for standard cell height = 0.300 μm ($Lg \leq 0.011 \mu\text{m}$).

FinFET_Boundary_1 (CAD layer: 250;0, or FB_1) is used for FinFET device.

prBoundary (CAD layer: 108;0) is used as cell boundary layer for auto P&R purpose.

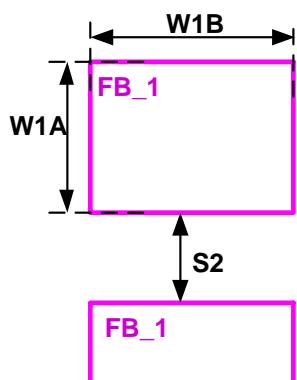
$n \geq 0$ and n is integer.

Rule No.	Description	Label	Op.	Rule
FB.W.1.1	Width of FB_1 in vertical direction	W1A	=	0.2180+0.0300*n
FB.W.1.2	Width of FB_1 in horizontal direction (Except DC6_1, DC4_CORE)	W1B	\geq	0.4000
FB.W.1.3	Vertical edge length of FB_1 between two consecutive 270-270 degree corners	W1C	=	0.0220+0.0300*n
FB.W.1.4	Vertical edge length of FB_1 between two consecutive 90-270 degree corners	W1D	=	0.0300+0.0300*n
FB.W.1.5	Concave corner to concave corner width of FB_1 in vertical direction	W1E	=	0.0080+0.0300*n
FB.S.2	Space of FB_1 in vertical direction [PRL > -0.030 μm] (Except Dummy_Cell)	S2	=	0.0820+0.0300*n
FB.S.2.2	Space of FB_1 to FB_9	S2B	\geq	0.1310
FB.S.2.2.1	Space of FB_1 to FB_9 in horizontal direction [PRL > -0.131 μm] (Overlap is not allowed)	S2Ba	\geq	0.1400
FB.S.2.3	Space of {SRM (50;0) OR {{FB_9 OR FB_8} OR BV_FB [width = 0.240/0.300 μm]}} in horizontal direction [PRL > -0.900 μm] (Overlap, abut is not allowed)	S2C	=	0.1400~0.2400, \geq 0.9000
FB.S.2.4	Space of {SRM (50;0) OR {{FB_9 OR FB_8} OR BV_FB [width = 0.240/0.300 μm]}} in vertical direction [PRL > -0.140 μm] (Overlap, abut is not allowed)	S2D	\geq	0.9000
FB.S.2.6	Space of FB_1 to SRM (50;0) (Overlap is not allowed)	S2F	\geq	0.1240
FB.S.2.7	Space of FB_1 to SRM (50;0) in vertical direction [PRL > -0.124 μm]	S2G	\geq	0.2300
FB.S.2.8	Space of FB_1 to FB_8 (Overlap is not allowed)	S2H	\geq	0.1400
FB.S.2.9	Space of FB_1 to FB_8 in vertical direction [PRL > -0.140 μm]	S2I	\geq	0.1610
FB.S.3	Space of {TCDDMY OR ICOVL_SINGLE} to {SRM (50;0) OR {FB_9 OR FB_8}} (Overlap is not allowed)	S3	\geq	2
FB.EN.1	FB_1 enclosure of ALL_OD in vertical direction	EN1	=	0.0600+0.0300*n
FB.EN.2	FB_1 enclosure of ALL_OD [PRL > -0.060 μm] in horizontal direction (Except Dummy_Cell)	EN2	\geq	0.0700
FB.EN.3	prBoundary enclosure of ALL_OD in vertical direction in cell level (Turn on DRC option: prBoundary_FIN, for global fin alignment after cell abutment) (Except FB_9, BLK_WF)	EN3	=	0.0410+0.0300*n
FB.EN.3.1	prBoundary enclosure of ALL_OD in vertical direction in cell level (Turn on DRC option: prBoundary_COD, for COD utility handling after cell abutment) (Except FB_9)	EN3A	\geq	0.1010

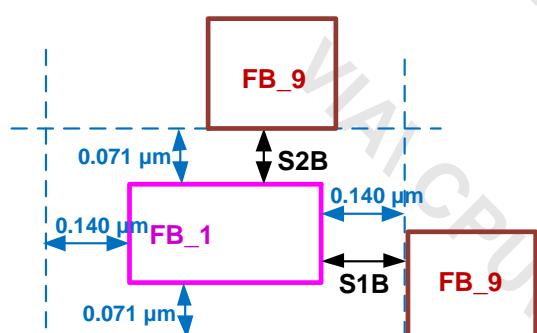
Rule No.	Description	Label	Op.	Rule
FB.EN.3.2	prBoundary enclosure of ALL_OD [length < 0.154 μm in horizontal direction] in vertical direction in cell level (Turn on DRC option: prBoundary_COD, for COD utility handling after cell abutment) (Except FB_9)	EN3B	≥	0.1310
FB.EN.7	prBoundary enclosure of FB_1 in vertical direction in cell level	EN7	=	0.0110+0.0300*n
FB.EN.7.1	prBoundary enclosure of TCDDMY in vertical direction in cell level	EN7A	=	0.0300*n
FB.R.1	ALL_OD must be inside {FB_1 OR {FB_9 OR FB_8}} (Except SEALRING_ALL, BLK_WF, TCDDMY)			
FB.R.3	{{{FB_1 OR {FB_9 OR FB_8}} OR BV_FB [width = 0.240/0.300 μm]}} OR SRM} point touch is not allowed			
FB.R.5	{FB_1 OR {FB_9 OR FB_8}} must be orthogonal to grid			

TSMC Confidential Information
938214
VIAI CPU Platform Col., Ltd.
10/05/2018

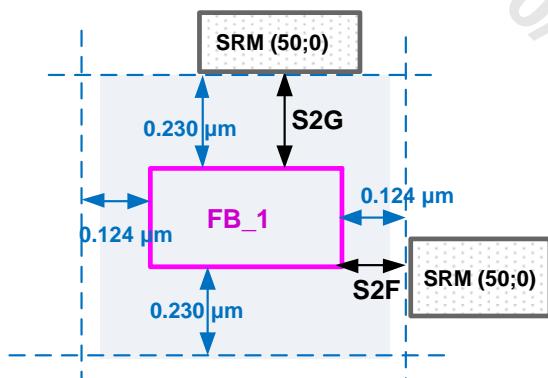
Fin Boundary



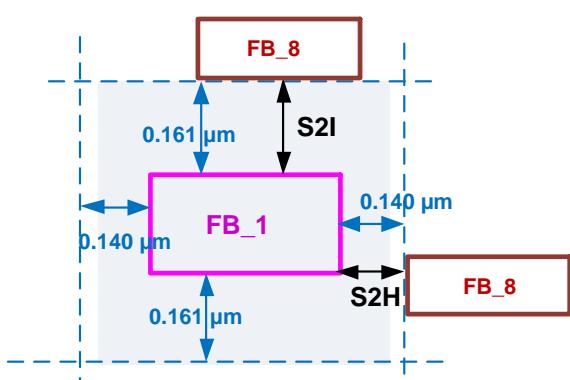
FB.W.1.1 / FB.W.1.2 / FB.S.2



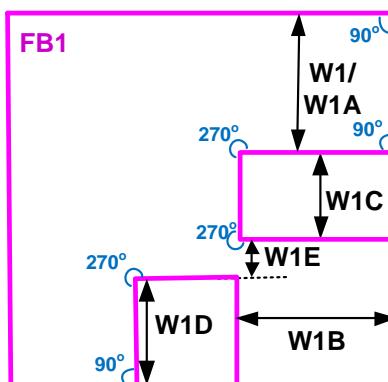
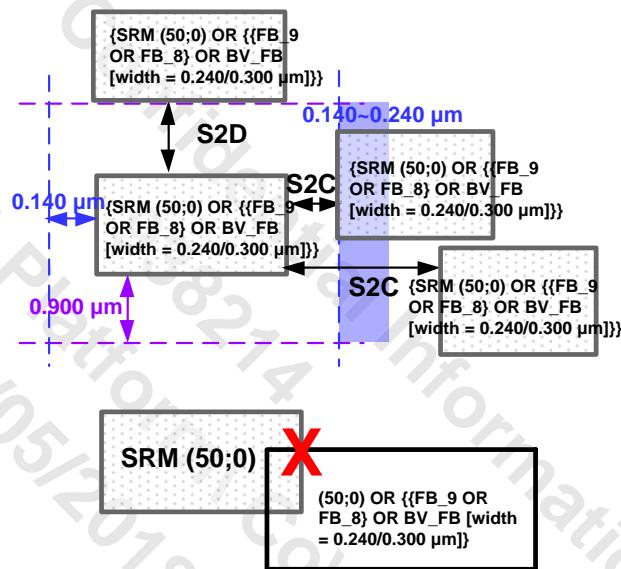
FB.S.2.2 / FB.S.2.2.1



FB.S.2.6 / FB.S.2.7



FB.S.2.8 / FB.S.2.9

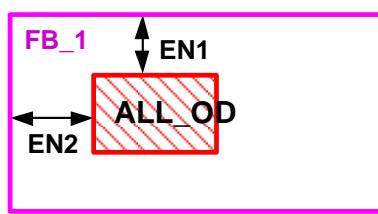
FB.W.1.1 / FB.W.1.2 / FB.W.1.3
FB.W.1.4 / FB.W.1.5

Overlap is not allowed

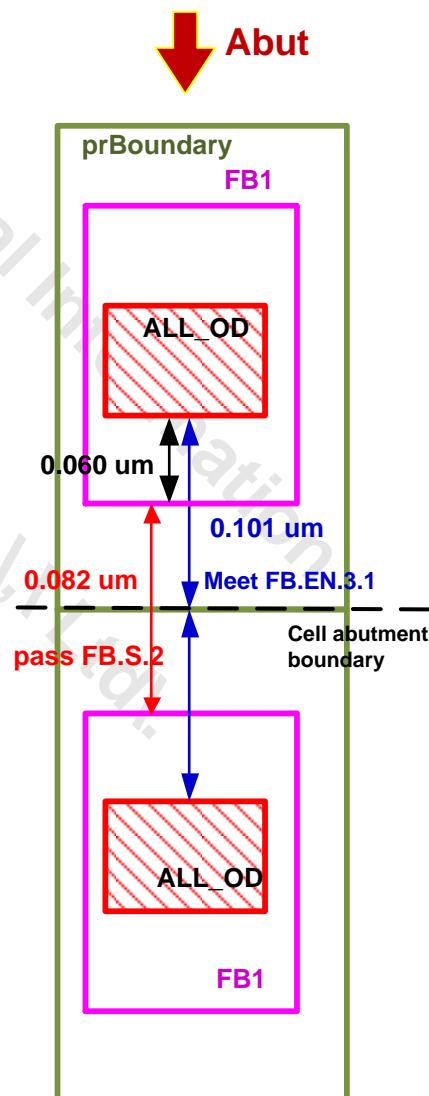
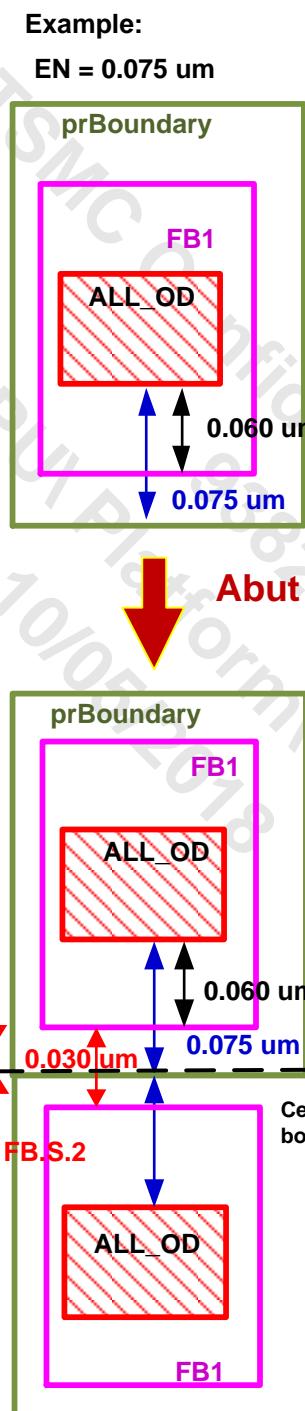
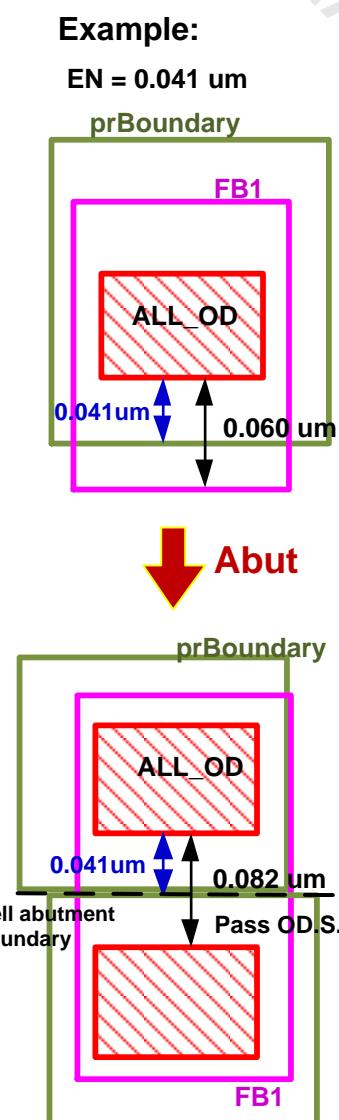
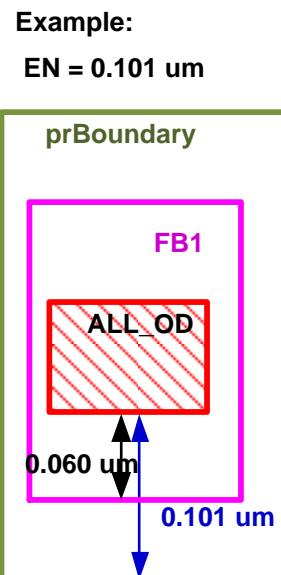
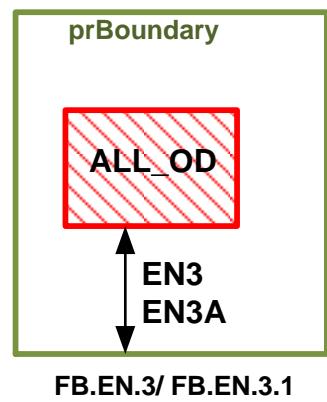
FB.S.2.3 / FB.S.2.4



FB.S.3



FB.EN.1 / FB.EN.2



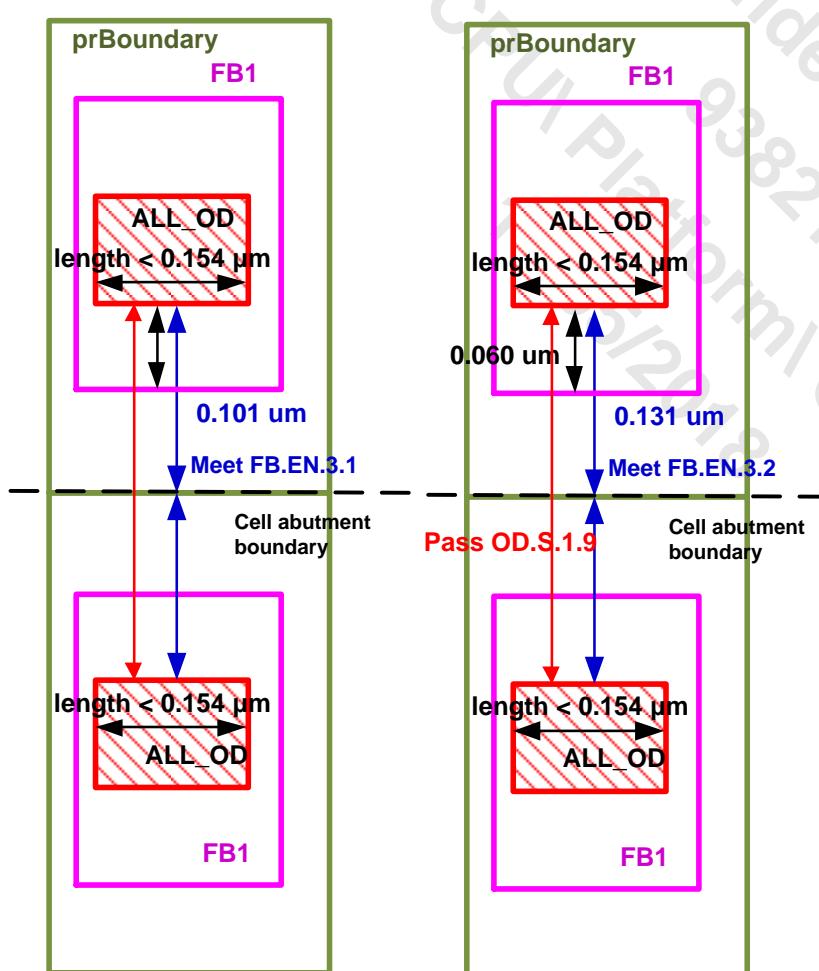
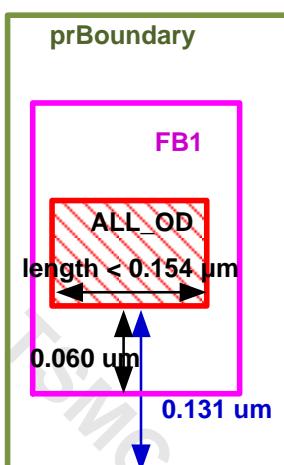
Example:

EN = 0.101 um

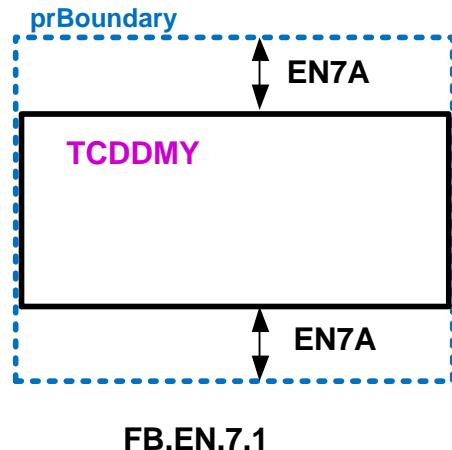
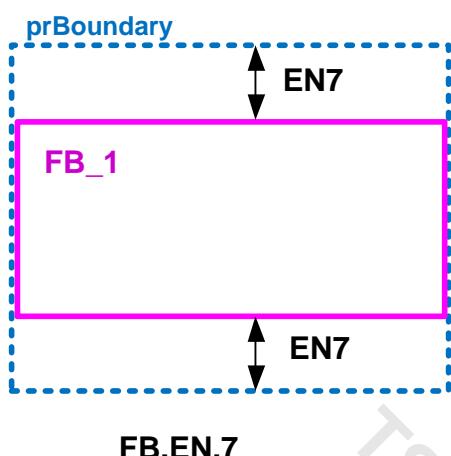


Example:

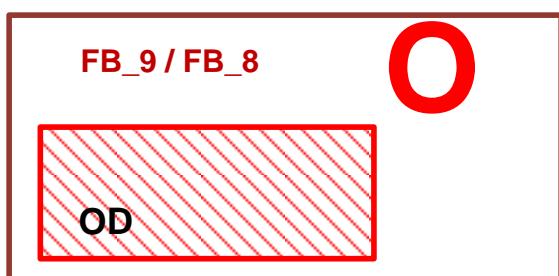
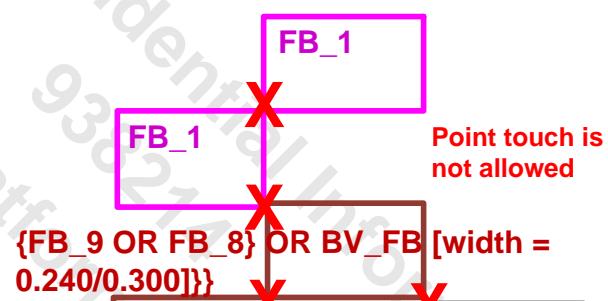
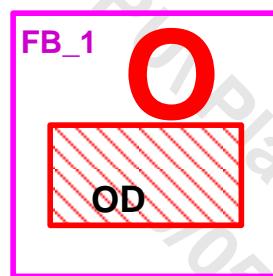
EN = 0.131 um



FB.EN.3.2

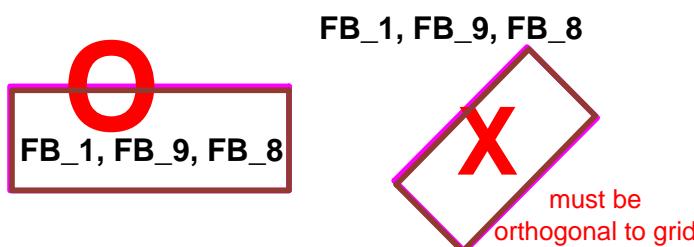


OD must be inside FB_1, FB_9, FB_8
ALL_OD must be inside FB_1 and {FB_9 OR FB_8}



FB.R.3

FB.R.1



FB.R.5

4.5.3 Gate Oxide and Diffusion (OD) Layout Rules

$n \geq 0$ and n is integer.

ALL_OD = {OD OR SR_DOD}

Rule No.	Description	Label	Op.	Rule
OD.W.1	Width of ALL_OD (Except BLK_WF)	W1	\geq	0.0380
OD.W.1.1	Width of ALL_OD in vertical direction (Except BLK_WF)	W1A	=	0.0380+0.0300*n
OD.W.1.2	Width of ALL_OD [INSIDE OD2] (Except DC6_2 (257;62))	W1B	\geq	0.0680
OD.W.1.3	Width of ALL_OD [INSIDE OD2] in vertical direction (Except DC6_2 (257;62))	W1C	=	0.0680+0.0300*n
OD.W.3	Maximum channel width of MOS device (Except HEADER_9)	W3	\leq	0.5780
OD.W.5	Channel width of MOS [I/O device] (Except following conditions: 1. {STRAP NOT VAR})	W5	=	0.0980+0.0300*n
OD.W.7	Maximum width of ALL_OD in vertical direction	W7	\leq	0.9680
OD.W.7.1	Maximum width of ALL_OD in vertical direction (Except HEADER_9, or following conditions: 1. {Dummy_Cell NOT {{DC5_1 OR DC5_2} OR DC7} OR {DC8_1 OR DC8_2}}})	W7A	\leq	0.5780
OD.S.1	Space of ALL_OD (Except BLK_WF)	S1	\geq	0.0460
OD.S.1.0.1	Space of ALL_OD [INSIDE PO_P63]	S1	\geq	0.0520
OD.S.1.0.2	Space of ALL_OD [INSIDE PO_P76]	S1	\geq	0.0650
OD.S.1.1	Space of ALL_OD in vertical direction (Except FB_9, BLK_WF)	S1A	=	0.0820+0.0300*n
OD.S.1.2	Space of STRAP to ACTIVE (Except FB_9, BLK_WF)	S1B	\geq	0.0820
OD.S.1.3	Space of ALL_OD [width \geq 0.308 μm] to ALL_OD in vertical direction [PRL > 0.011 μm] (Except HEADER_9, HEADER_8)	S1C	\geq	0.1120
OD.S.1.4	At least one side of Small_OD space to ALL_OD in vertical direction [PRL > 0.036 μm] (Except FB_9, FB_8) Definition of Small_OD: Small_OD = {ALL_OD [0.038 μm \leq width \leq 0.128 μm , length \leq 0.182 μm , area $<$ 0.0149 μm^2 (excluding 0.068 μm x 0.170 μm / 0.068 μm x 0.179 μm / 0.068 μm x 0.182 μm)]}	S1D	\leq	0.1720

Rule No.	Description	Label	Op.	Rule
OD.S.1.9	<p>Space of ALL_OD [length < 0.154 μm in horizontal direction] to ALL_OD in vertical direction (Except FB_9, FB_8, BLK_WF, or following conditions: 1. ALL_OD [length < 0.154 μm in horizontal direction] horizontal edge abut CONFINED_EDGE, 2. Space of ALL_OD [length < 0.154 μm in horizontal direction] to ALL_OD_MERGE_S120H [length ≥ 0.154 μm] in vertical direction = 0.082 μm [PRL > -0.063 μm], 3. Space of ALL_OD [length < 0.154 μm in horizontal direction] in vertical direction = 0.082 μm [0.114 μm > PRL > -0.063 μm])</p> <p>Definition of ALL_OD_MERGE_S120H: ALL_OD SIZING up/down 0.060 μm in horizontal direction</p> <p>Definition of CONFINED_EDGE: Horizontal edge of ALL_OD_MERGE_S120H meet one of following condition: 1. adjacent to vertical edge [edge length = 0.030 μm] 2. abut at least two ALL_OD</p>	S11	=	0.1120, 0.1420, 0.1720, ≥ 0.2620
OD.S.2	<p>Maximum vertical space of Functional_ACTIVE to OD_Merge (Except BLK_WF, or following conditions: 1. Horizontal edge of Functional_ACTIVE fully inside OD_Merge, 2. PRL ≥ 0.108 μm and violation length ≤ 0.386 μm)</p> <p>Definition of Functional_ACTIVE: {ACTIVE INTERACT {{PO NOT CPO} INTERACT MP}}</p> <p>Definition of OD_Merge: {ALL_OD SIZING up/down 0.240 μm in horizontal direction}</p>	S2	≤	0.5620
OD.S.3	Space of ALL_OD [INSIDE OD2]	S3	≥	0.0940
OD.S.3.1	Space of ALL_OD [INSIDE OD2] in vertical direction	S3A	=	0.1420+0.0300*n
OD.S.8	Space of SR_DOD to NWDMY (Overlap is not allowed)	S8	≥	0.4800
OD.S.11	Empty space of ALL_OD DRC flags {{CHIP NOT ALL_OD} SIZING down/up 2.5 μm} (Except TCDDMY, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)	S11	≤	5
OD.S.11.1	Empty space of ALL_OD DRC flags {{CHIP NOT ALL_OD} SIZING down/up 0.600 μm} (Except NWDMY, RH_TNB, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)	S11	≤	1.2
OD.S.12.2	Space to ALL_OD [maximum delta V > 1.32V] (1.2V + 10%)	S12	≥	0.0940
OD.S.12.3	Space to ALL_OD [maximum delta V > 1.65V] (1.5V + 10%)	S12	≥	0.1500
OD.S.18	Space of ALL_OD [0.008 μm ≥ PRL > -0.0525 μm] in horizontal direction (Except BLK_WF)	S18	≥	0.0940
OD.S.18.1	Space of ALL_OD [projection length difference = 0.060 μm] in horizontal direction (Except BLK_WF, or following conditions: 1. ALL_OD projection on Checked_OD = 0.060 μm with space ≤ 0.055 μm in horizontal direction) <p>Definition of Checked_OD: {{ALL_OD SIZING up/down 0.086 μm in vertical direction} NOT ALL_OD}</p>	S18A	≥	0.0940

Rule No.	Description	Label	Op.	Rule
OD.S.18.2	Space of ALL_OD [projection length difference = 0.090 μm] in horizontal direction (Except BLK_WF, or following conditions: 1. ALL_OD projection on Checked_OD = 0.090 μm with space ≤ 0.055 μm in horizontal direction) Definition of Checked_OD follows OD.S.18.1	S18B	≥	0.0940
OD.S.18.3	Space of ALL_OD [length < 0.154 μm in horizontal direction] to ALL_OD [projection length difference = 0.120 μm] in horizontal direction	S18C	≥	0.0940
OD.S.22.6	Forbidden vertical width of enclosed region within {rectangular ALL_OD merge its space ≤ 0.106 μm in horizontal direction} with [both adjacent space ≤ 0.172 μm in vertical direction] (Except FB_9, FB_8, PO_P63, or following conditions: 1. horizontal width ≤ 0.122 μm or > 0.334 μm) DRC flags the space causing COD utility problem or COD rule violation in certain of layout	S22F	=	0.2020
OD.S.22.7	Forbidden vertical width of enclosed region within {rectangular ALL_OD merge its space ≤ 0.118 μm in horizontal direction} with [both adjacent space ≤ 0.172 μm in vertical direction] [INSIDE PO_P63] (Except FB8, or following conditions: 1. horizontal width ≤ 0.118 μm or > 0.378 μm) DRC flags the space causing COD utility problem or COD rule violation in certain of layout	S22F	=	0.2020
OD.S.22.8	Forbidden vertical width of enclosed region within {{rectangular ALL_OD SIZING up/down 0.057 μm in horizontal direction} SIZING 0.025 μm in horizontal direction} with [both adjacent space = 0.172 μm in vertical direction] (Except FB_9, FB_8, PO_P63, or following conditions: 1. horizontal width ≤ 0.122 μm or > 0.342 μm) DRC flags the space causing COD utility problem or COD rule violation in certain of layout	S22G	=	0.2020
OD.S.22.8.1	Forbidden vertical width of enclosed region within {{rectangular ALL_OD SIZING up/down 0.063 μm in horizontal direction} SIZING 0.029 μm in horizontal direction} with [both adjacent space = 0.172 μm in vertical direction] [INSIDE PO_P63] (Except FB8, following conditions: 1. horizontal width ≤ 0.134 μm or > 0.378 μm) DRC flags the space causing COD utility problem or COD rule violation in certain of layout	S22G	=	0.2020
OD.S.22.9	Forbidden vertical width of enclosed region within {rectangular ALL_OD merge its space ≤ 0.118 μm in horizontal direction} with [1. both adjacent space = 0.202 μm in vertical direction, and 2. one adjacent space = 0.046~0.055 μm, the other adjacent space = 0.046~0.118 μm in horizontal direction] (Except FB_9, FB_8, or following conditions: 1. horizontal width < 0.103 μm or > 0.118 μm) DRC flags the space causing COD utility problem or COD rule violation in certain of layout	S22I	=	0.2320
OD.S.22.10	Forbidden vertical width of enclosed region within {rectangular ALL_OD merge its space ≤ 0.118 μm in horizontal direction} with [1. both adjacent space = 0.232 μm in vertical direction, and 2. one adjacent space = 0.046~0.055 μm, the other adjacent space = 0.046~0.118 μm in horizontal direction] (Except FB_9, FB_8, or following conditions: 1. horizontal width < 0.103 μm or > 0.118 μm) DRC flags the space causing COD utility problem or COD rule violation in certain of layout	S22J	=	0.2620

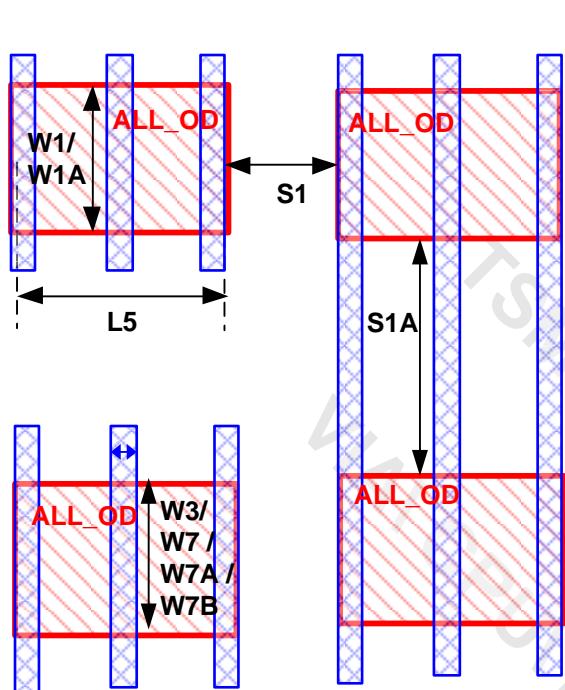
Rule No.	Description	Label	Op.	Rule
OD.S.25	Space of vertical edge [between 2 consecutive 90-90 degree corners] of {ACTIVE OR SR_DOD} [horizontal length > 1 μm , interact PO [width \leq 0.020 μm]] to ALL_OD in horizontal direction (a violation with a length ratio $<$ 83 % is allowed, the length ratio = violation length / device width)	S25	\leq	1
OD.L.2g ^U	It is strongly suggested to limit the max interconnect length to be as short as possible to avoid high Rs variation			
OD.L.5	Length of ALL_OD in horizontal direction (Except BLK_WF)	L5	\geq	0.1220
OD.L.5.0.1	Length of ALL_OD in horizontal direction [INSIDE PO_P63]	L5	\geq	0.1340
OD.L.5.0.2	Length of ALL_OD in horizontal direction [INSIDE PO_P76]	L5	\geq	0.1600
OD.L.5.1	Maximum length of OD in horizontal direction	L5A	\leq	204
OD.L.5.2	Maximum length of SR_DOD in horizontal direction (Except FB_9, FB_8)	L5B	\leq	61
OD.A.1	Area of ALL_OD (Except FB_9, FB_8, BLK_WF)	A1	\geq	0.00646
OD.A.1.2	Area of ALL_OD [INSIDE OD2] (Except following conditions: 1. {Dummy_Cell NOT {{DC5_1 OR DC5_2} OR DC7} OR {DC8_1 OR DC8_2}}})	A1B	\geq	0.01800
OD.A.2	Enclosed area of {ALL_OD SIZING up/down 0.086 μm in vertical direction} (Except FB_9, FB_8, BLK_WF, or following conditions: 1. rectangular enclosed area 0.046 μm x 0.382 μm , 0.049 μm x 0.382 μm , 0.052 μm x 0.382 μm , 0.055 μm x 0.382 μm)	A2	\geq	0.02300
OD.A.6	Maximum area sum of {ACTIVE NOT ALL_PO} in the same OD	A6	\leq	150
OD.A.7	Empty area of ALL_OD [ALL_OD space > 0.900 μm] DRC flags {{CHIP NOT {ALL_OD SIZING up/down 0.450 μm }} down/up 0.450 μm } can enclose a 5 μm x 0.900 μm orthogonal rectangle (Except SEALRING_ALL, NWDMY, RH_TNB, TCDDMY, ICOVL_SINGLE, IGBTDMY, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)	A7	$<$	4.5
OD.A.7.1	Empty area of ALL_OD [ALL_OD space > 1.2 μm] DRC flags {{CHIP NOT {ALL_OD SIZING up/down 0.6 μm }} down/up 0.6 μm } can enclose a 16 μm x 1.2 μm orthogonal rectangle (Except SEALRING_ALL, NWDMY, TCDDMY, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)	A7	$<$	19.2
OD.A.8	Empty area of ALL_OD within 1 μm from SRAM DRC flags {{{SRM SIZING 1 μm } NOT SRM} NOT ALL_OD} SIZING down/up 0.2965 μm } can enclose a 9 μm x 0.593 μm orthogonal rectangle	A8	$<$	5.337
OD.A.8.2	Empty area of ALL_OD [ALL_OD space > 3.5 μm] DRC flags {{CHIP NOT {ALL_OD SIZING up/down 1.75 μm }} down/up 1.75 μm } can enclose a 3.5 μm x 25 μm orthogonal rectangle (Except SEALRING_ALL, TCDDMY, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)	A8B	$<$	87.5
OD.A.9	Empty area of ALL_OD [INSIDE PO_Boundary] DRC flags {{PO_Boundary NOT ALL_OD} SIZING down/up 0.200 μm } can enclose a 10 μm x 0.400 μm (vertical x horizontal) orthogonal rectangle	A9	$<$	4
OD.DN.1	Minimum ALL_OD density across full chip (Except NWDMY, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	25%
OD.DN.2	Maximum ALL_OD density across full chip (Except NWDMY, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\leq	60%

Rule No.	Description	Label	Op.	Rule
OD.DN.3.1	Minimum ALL_OD density in window 18 μm x 18 μm, stepping 9 μm (Except TCDDMY, ICOVL_SINGLE, BLK_WF, NWDMY, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	12%
OD.DN.3.2	Minimum ALL_OD density of {{RH_TNB SIZING 10 μm} NOT RH_TNB} (Except NWDMY, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	20%
OD.DN.4	Maximum ALL_OD density in window 18 μm x 18 μm, stepping 9 μm (Except TCDDMY, ICOVL_SINGLE, NWDMY, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≤	65%
OD.DN.9	Minimum SR_DOD density inside {{{{{OD OR PO} INTERACT TrGATE [NOT INTERACT VAR]} SIZING 2.5 μm} NOT {{OD OR PO} SIZING 0.400 μm}} NOT SRM (50;0)} NOT OD2} NOT NWDMY} NOT SEALRING_ALL} (Except following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc) This rule is only checked on the whole chip, not on the IP level		≥	10%
OD.DN.10	ALL_OD density difference between any two neighboring checking windows [window 10 μm x 10 μm, stepping 5 μm] (Except TCDDMY, ICOVL_SINGLE, NWDMY, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≤	45%
OD.R.2	ALL_OD must be a rectangle orthogonal to grid			
OD.R.5	SR_DOD is a must in chip level. SR_DOD CAD layer (TSMC default, 6;7) must be different from OD CAD layer			
OD.R.5.1	{SR_DOD NOT CPODE_WAIVE} interact OD, PO is not allowed (Except following conditions: 1. SR_DOD interact {PO NOT CPO} [NOT INTERACT OD or MP]) Definition of CPODE_WAIVE: {{{SR_DOD AND OD} AND CPODE} SIZING 0.002 μm}			
OD.R.6	ALL_OD cut OD2 is not allowed			
OD.R.7	Maximum delta V > 3.63V is not allowed. DRC searching range of ALL_OD space to ALL_OD is < 2.5 μm			
OD.R.8	ALL_OD must be inside prBoundary in cell level			
OD.R.9	ALL_OD horizontal edge must be on fin grid (Except BLK_WF)			

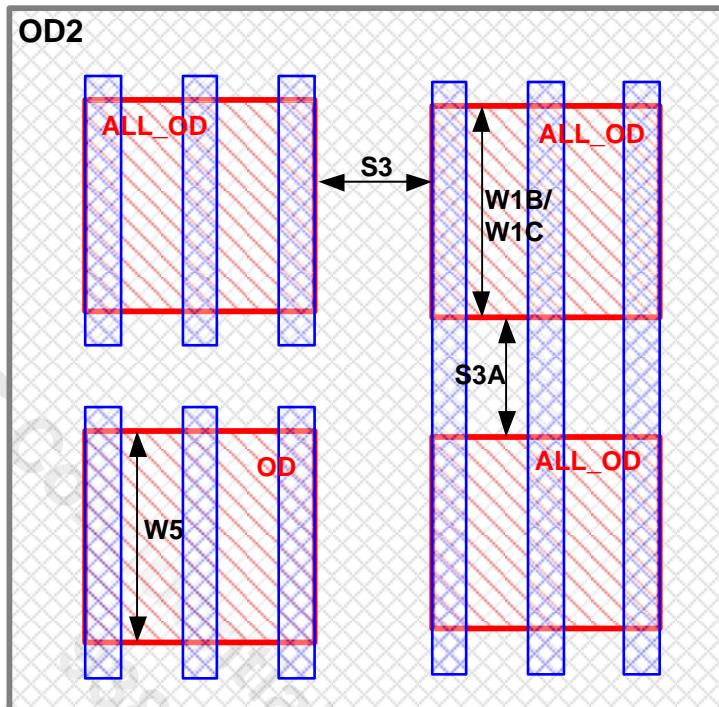
Table Notes:

- Delta Voltage Calculation in high voltage spacing rules please refer to section 3.9 DRC methodology of net voltage recognition.

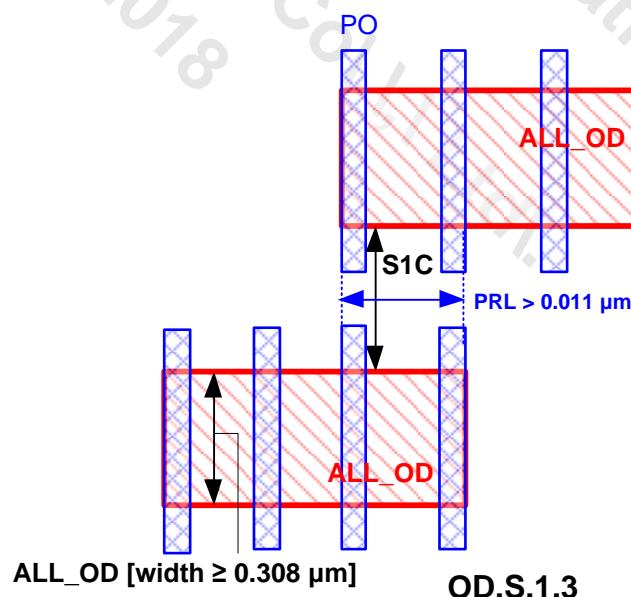
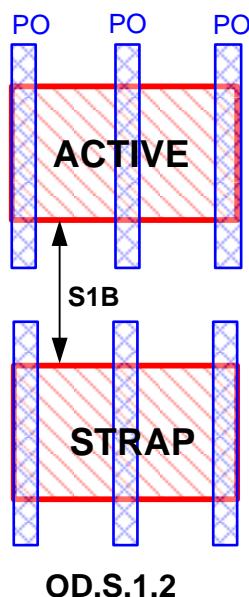
OD

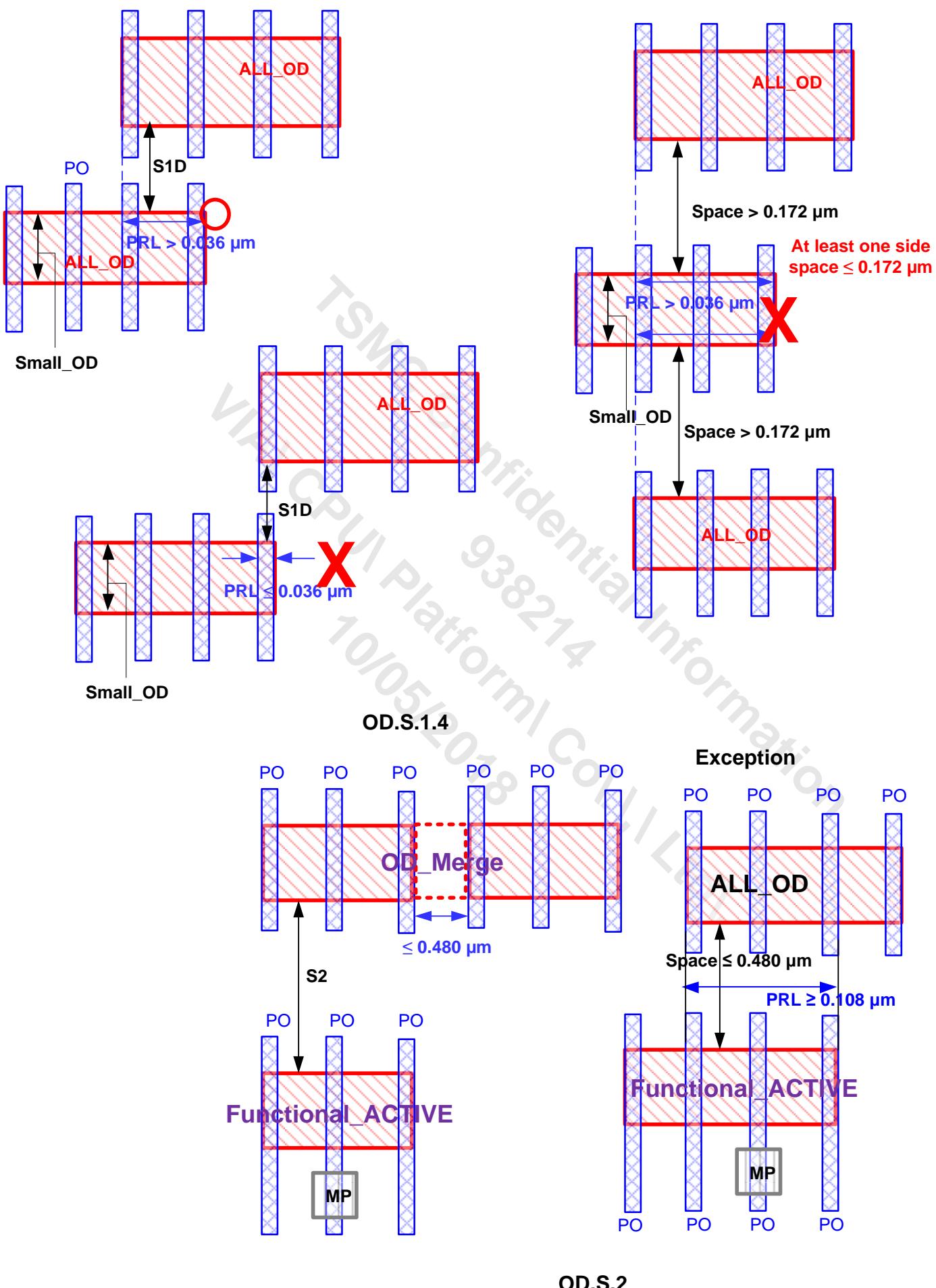


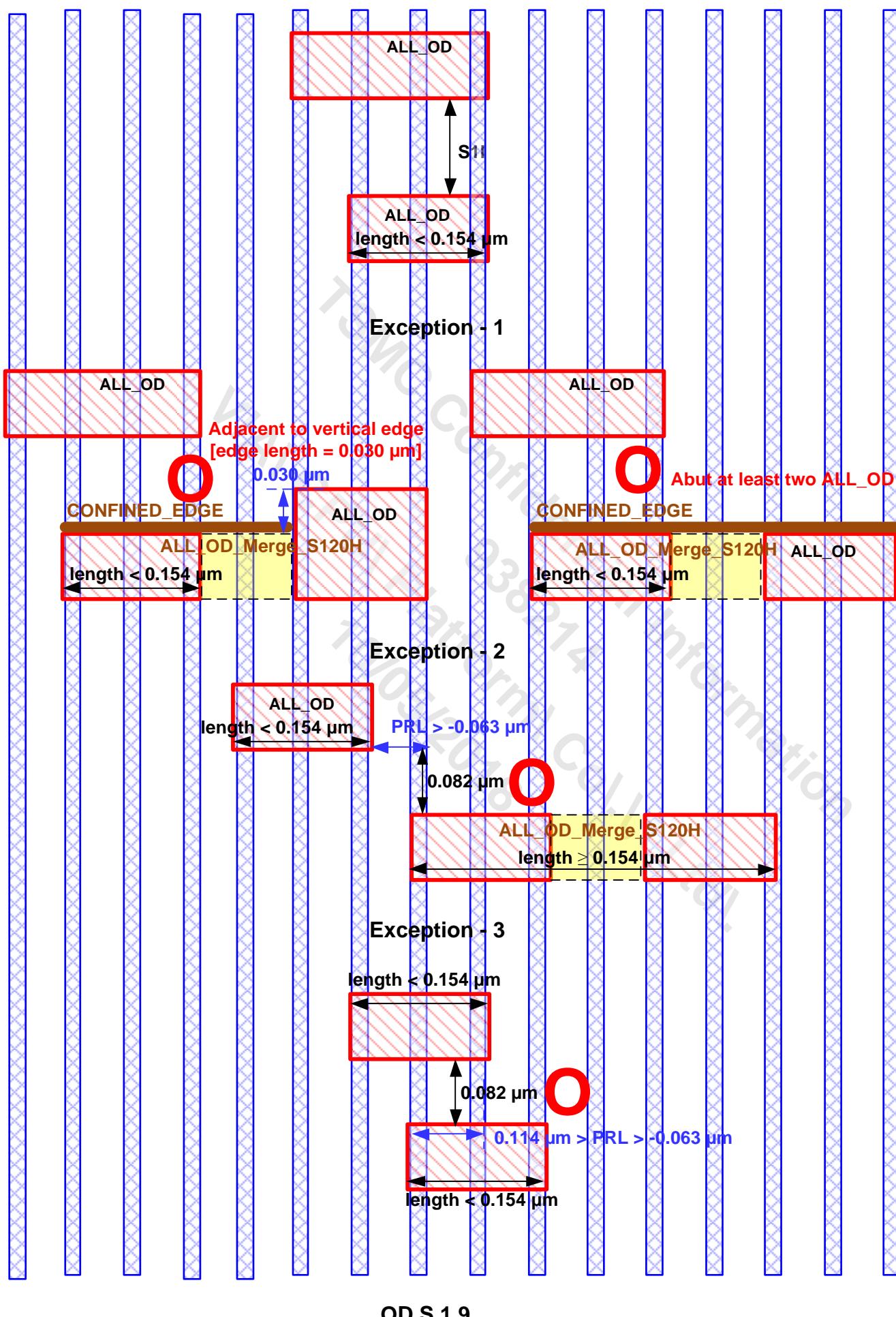
OD.W.1 / OD.W.1.1 / OD.W.3 / OD.W.7 /
OD.W.7.1 / OD.S.1 / OD.S.1.1 / OD.L.5 /
OD.S.1.0.1 / OD.L.5.0.1 / OD.S.1.0.2 /
OD.L.5.0.2

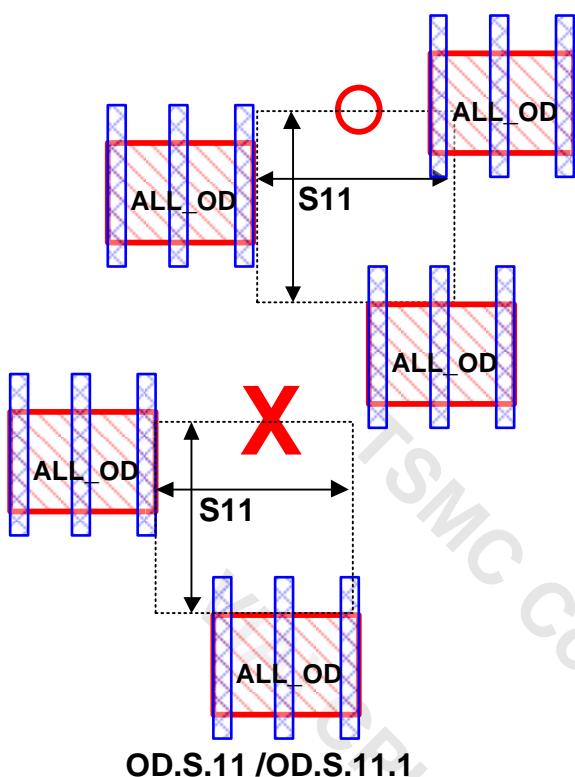


OD.W.1.2/ OD.W.1.3/ OD.W.5/ OD.S.3/
OD.S.3.1

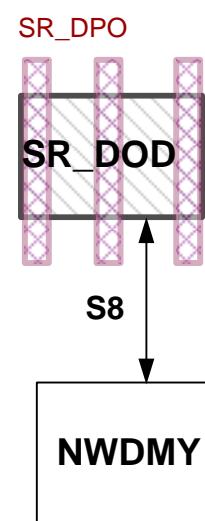




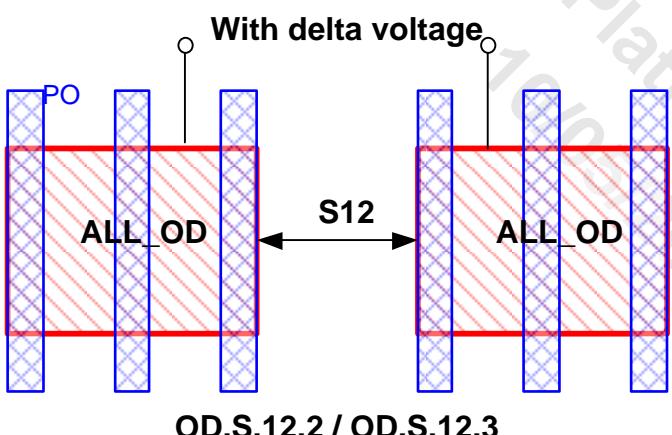




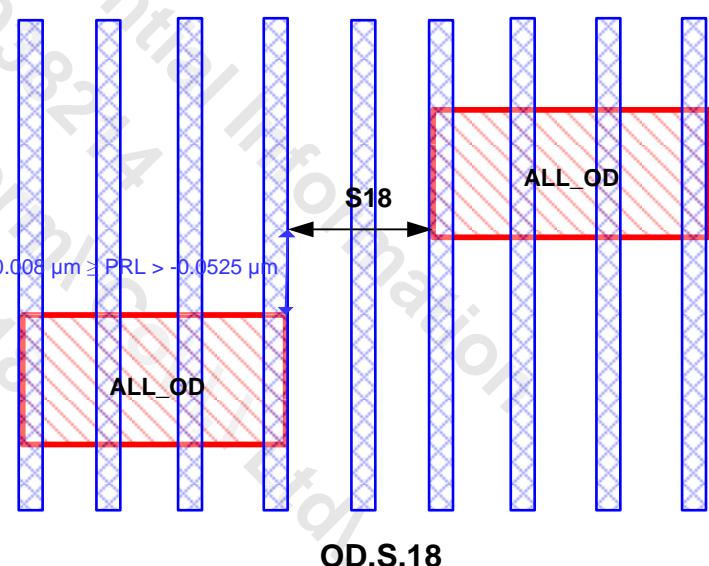
OD.S.11 / OD.S.11.1



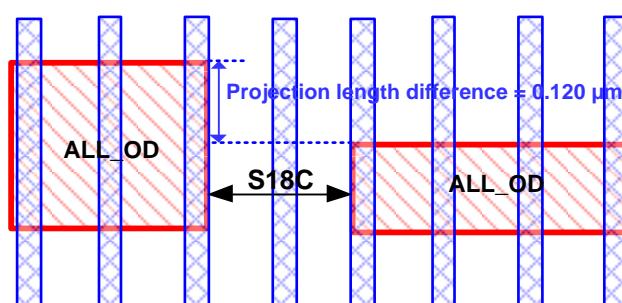
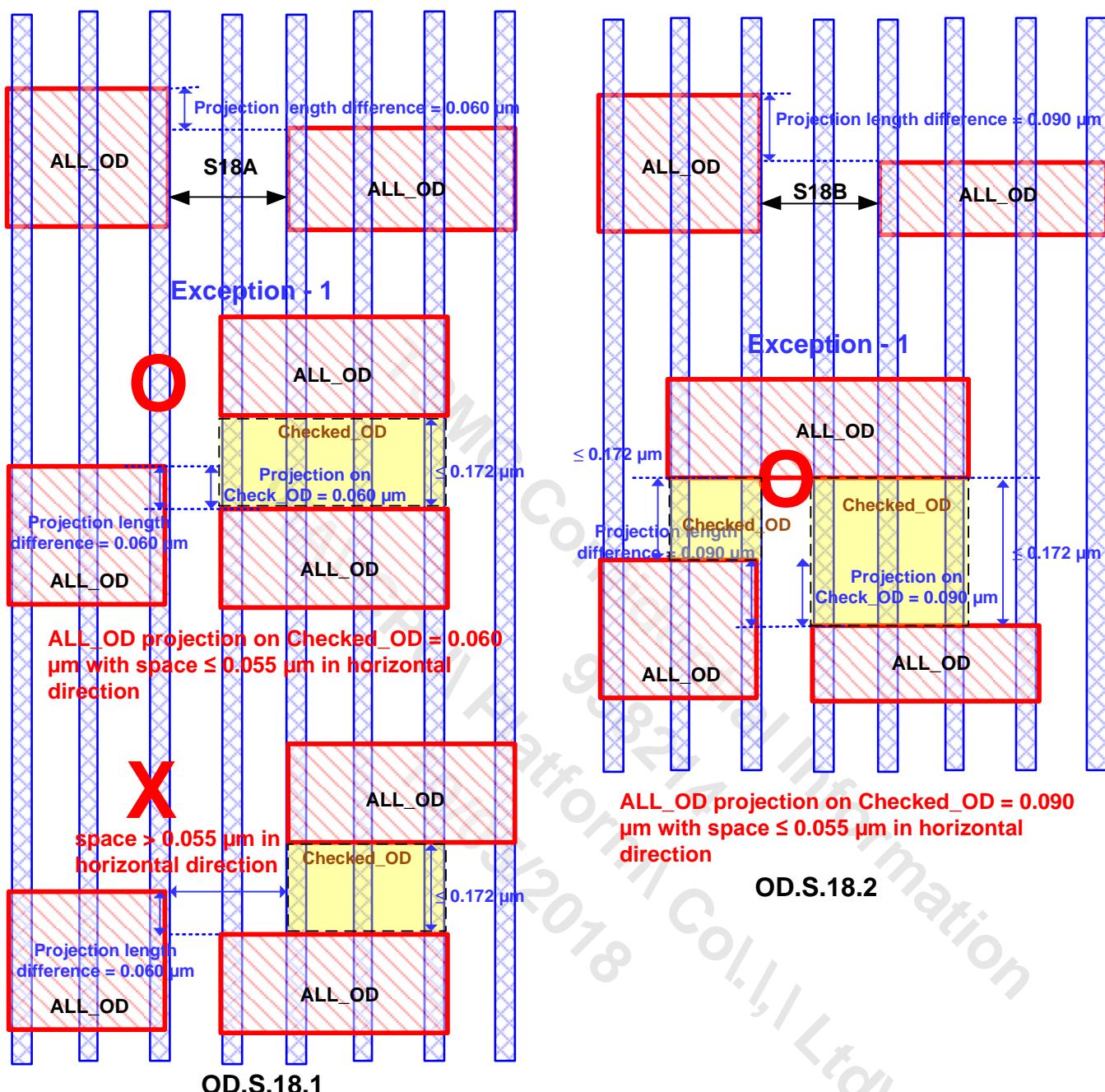
OD.S.8

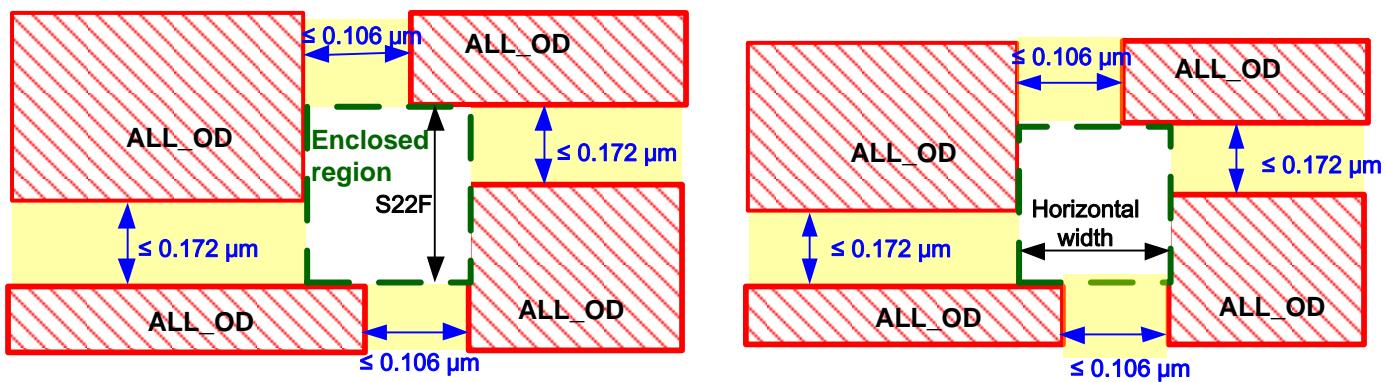


OD.S.12.2 / OD.S.12.3

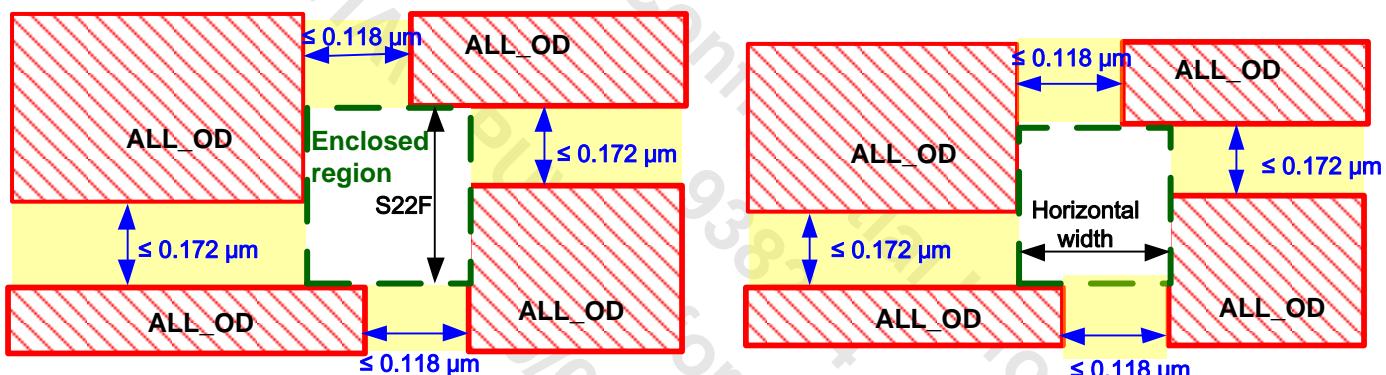


OD.S.18

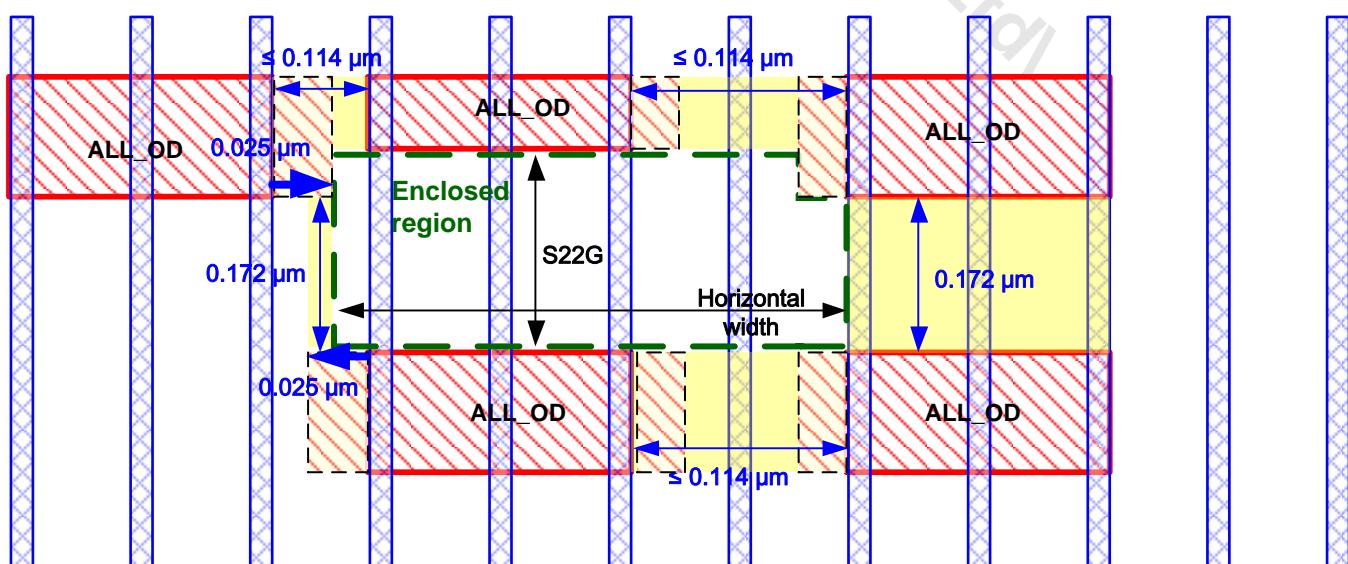




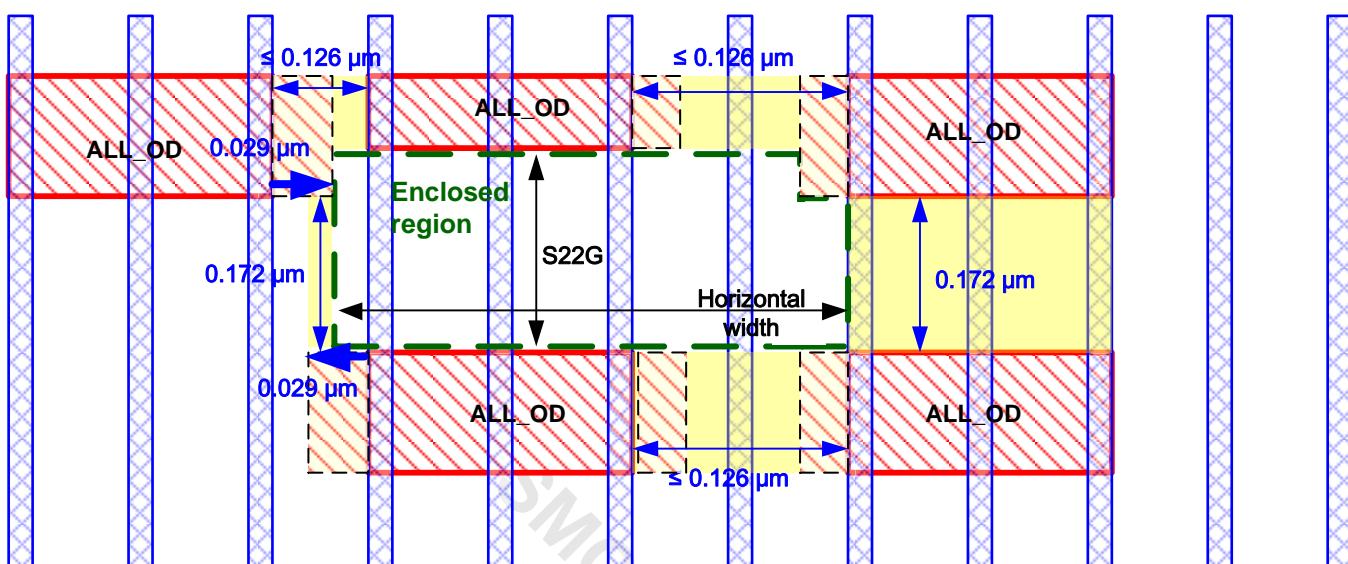
OD.S.22.6



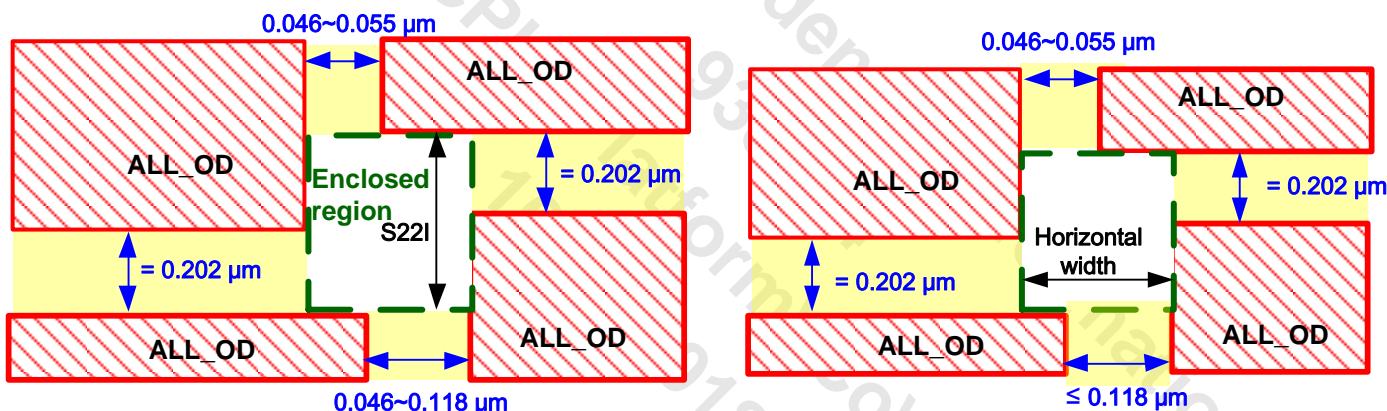
OD.S.22.7



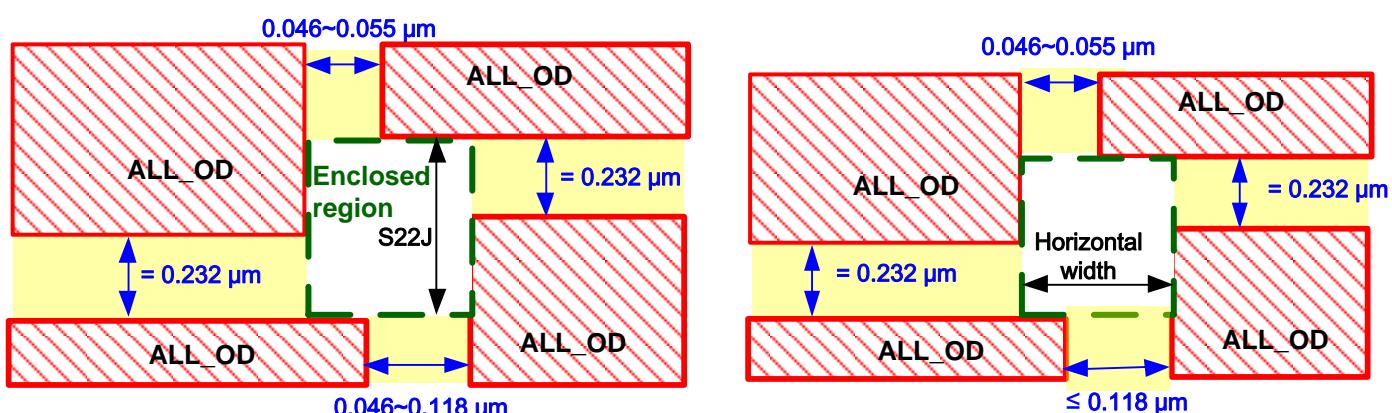
OD.S.22.8



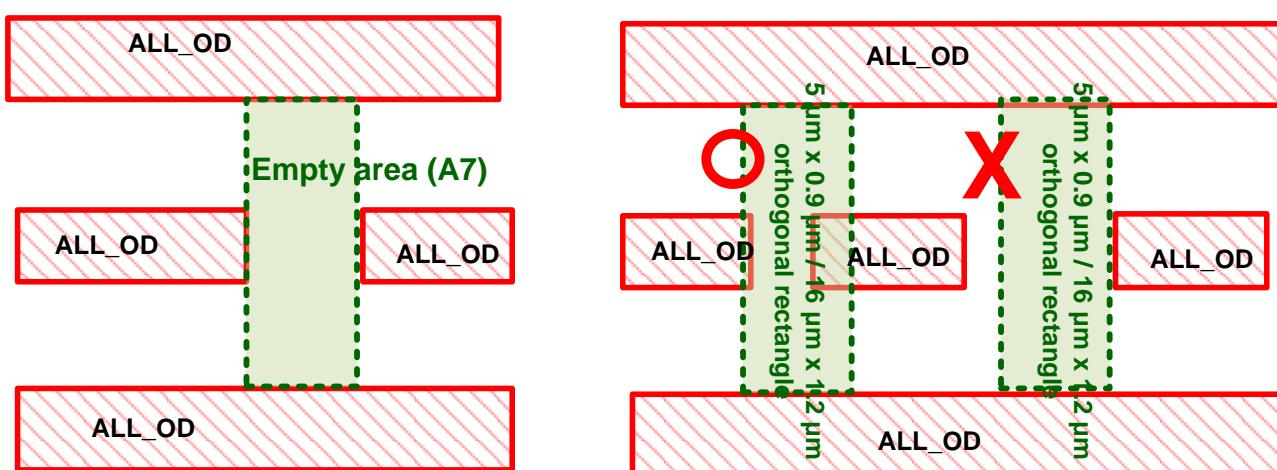
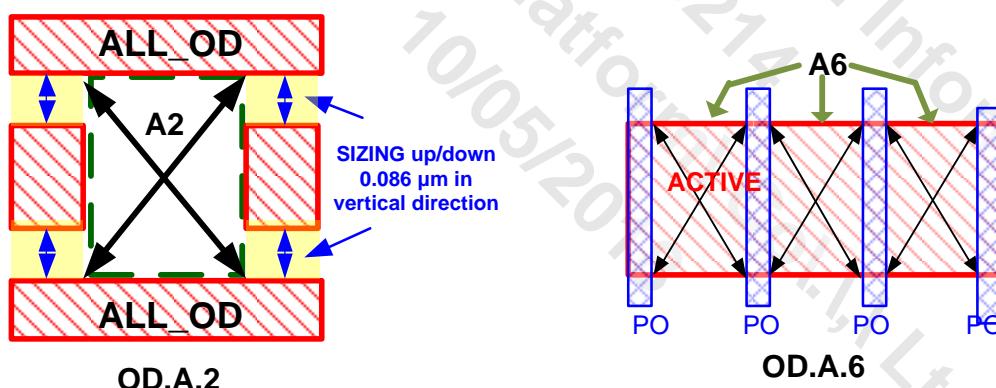
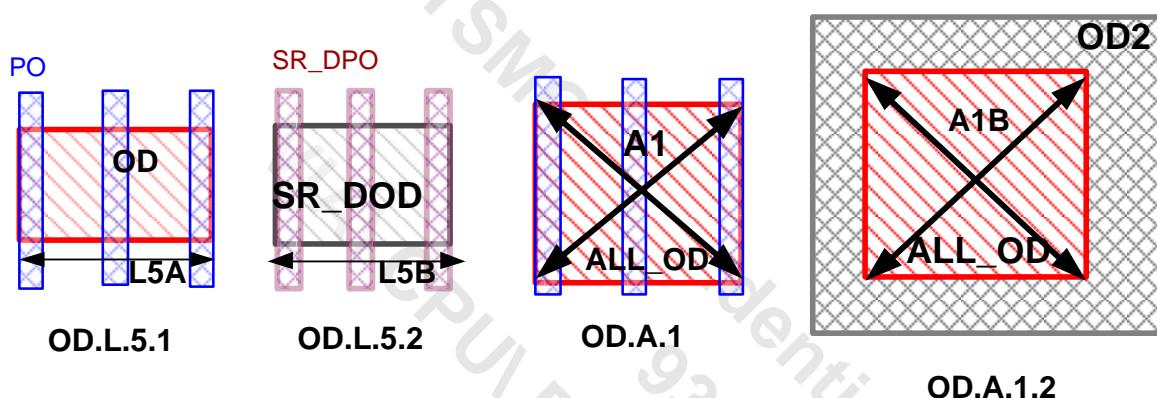
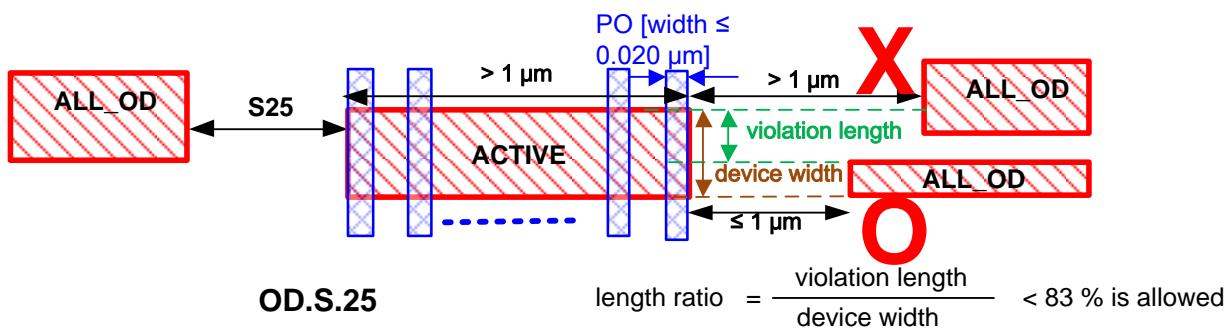
OD.S.22.8.1



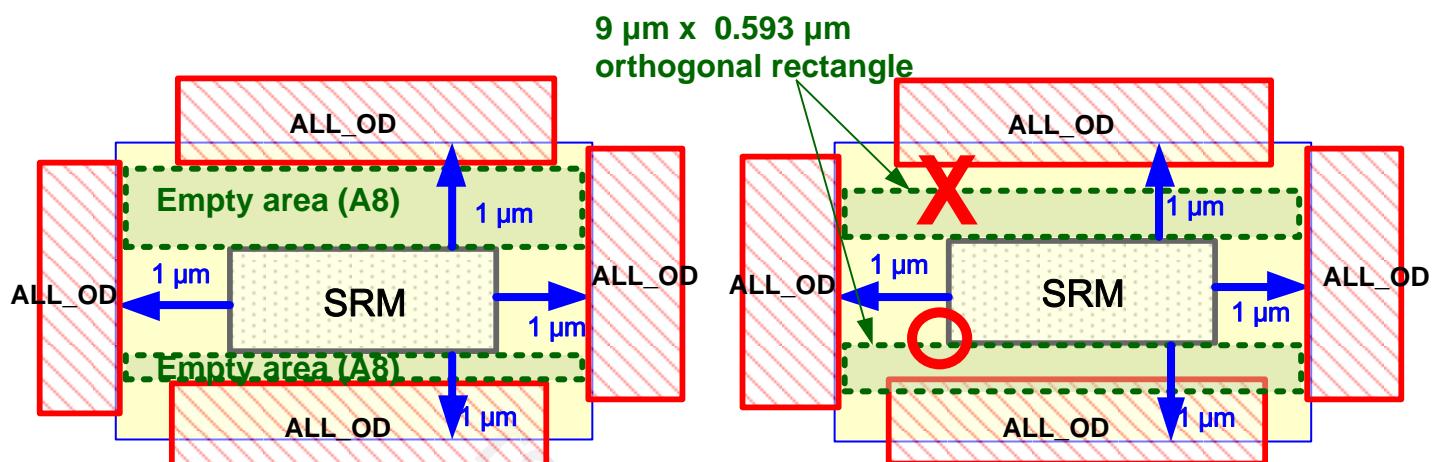
OD.S.22.9



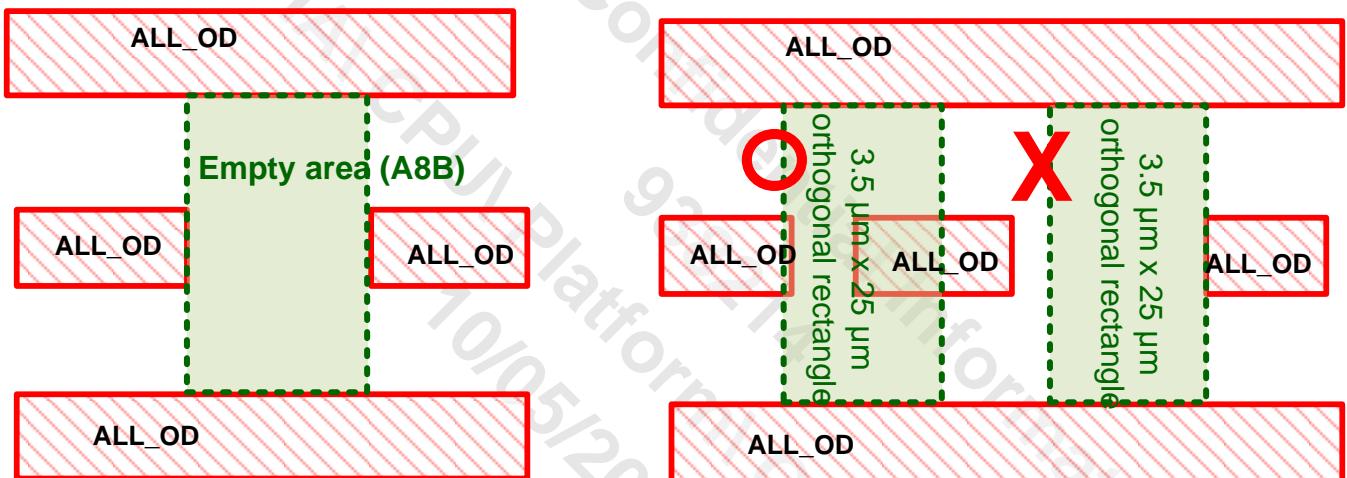
OD.S.22.10



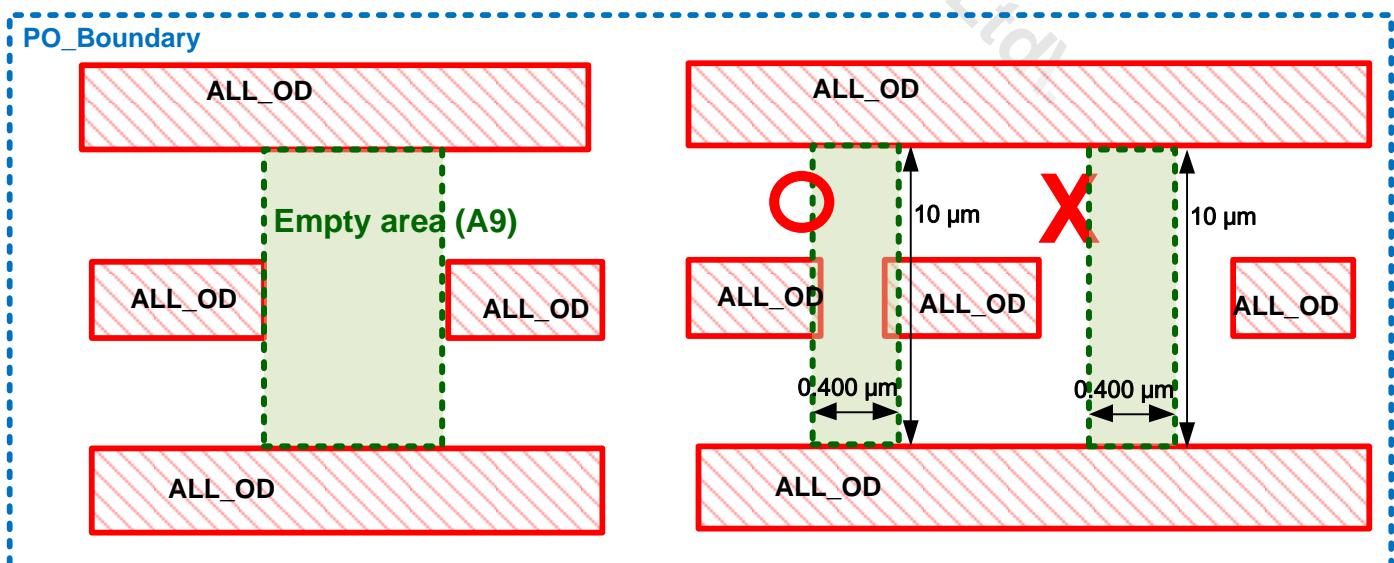
OD.A.7 / OD.A.7.1



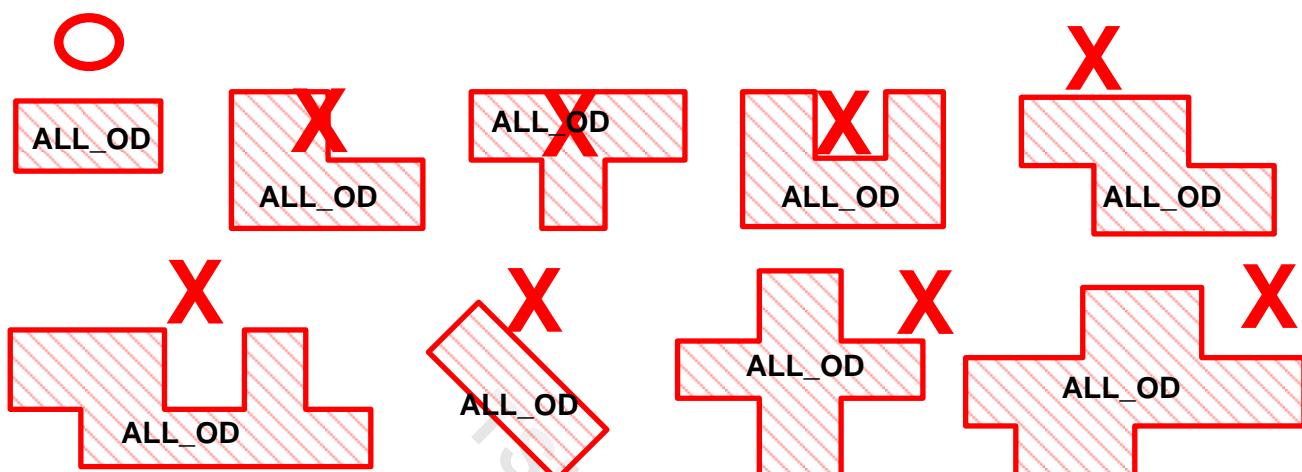
OD.A.8



OD.A.8.2

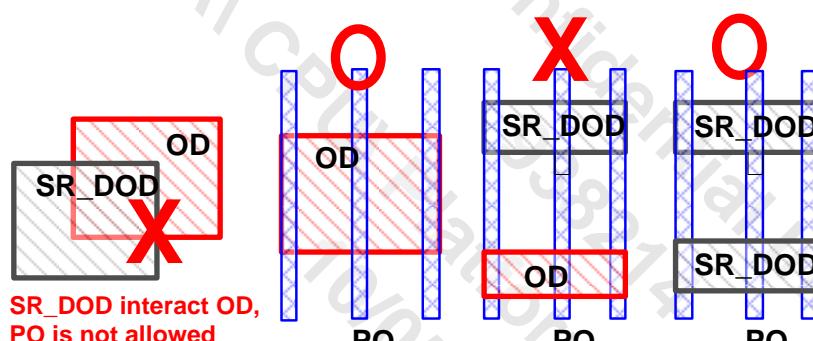


OD.A.9

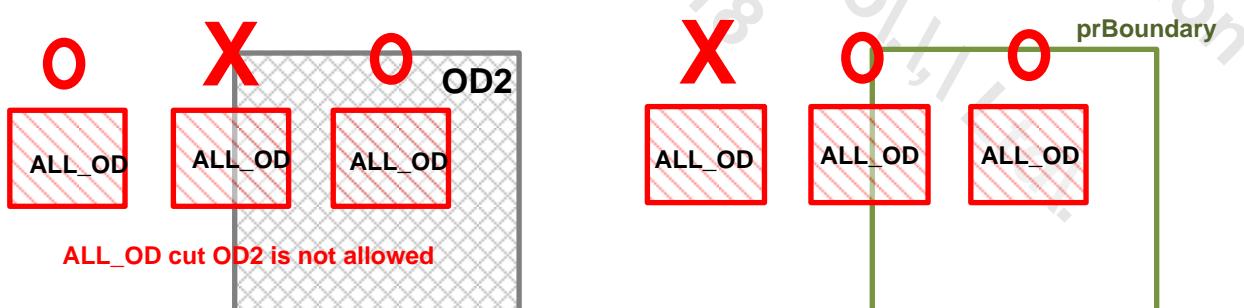


ALL_OD must be a rectangle orthogonal to grid

OD.R.2

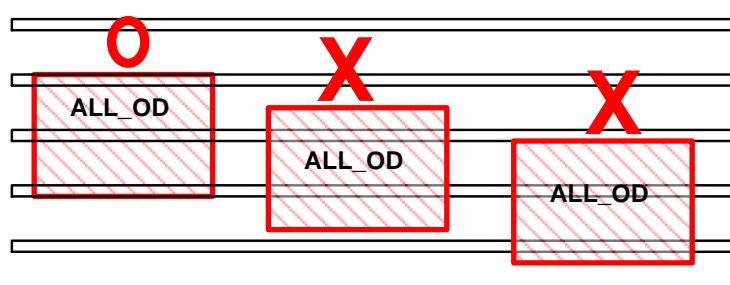


OD.R.5.1



OD.R.6

OD.R.8



OD.R.9

4.5.4 Cut-OD (COD) Layout Rules

COD_H (CAD layer: 6;17) is drawn inside SRAM and SEALRING_ALL for Horizontal Cut OD.

COD_V (CAD layer: 6;18) is drawn inside SRAM and SEALRING_ALL for Vertical Cut OD.

DCOD_H (CAD layer: 6;27) is generated from dummy utility for Horizontal Cut OD.

DCOD_V (CAD layer: 6;28) is generated from dummy utility for Vertical Cut OD.

All these layers are tapeout layers.

ALL_COD_H = {COD_H OR DCOD_H}

ALL_COD_V = {COD_V OR DCOD_V}

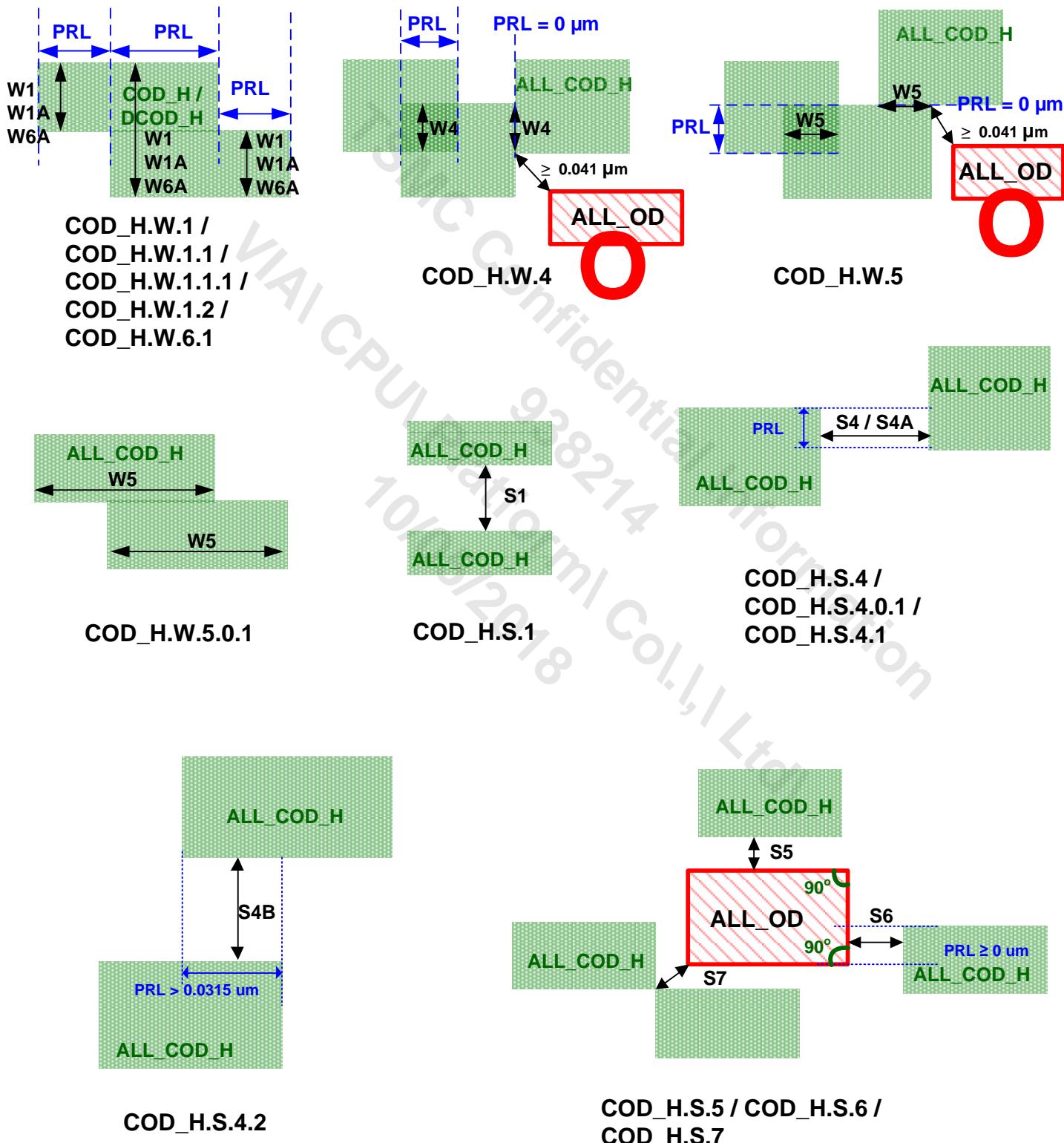
Rule No.	Description	Label	Op.	Rule
COD_H.W.1	Width in vertical direction DRC flags ALL_COD_H width between horizontal edges (Except BLK_WF, or following conditions: 1. {FB_9 SIZING 0.011 μm in vertical direction})	W1	≥	0.0600
COD_H.W.1.1	Width in vertical direction (Except BLK_WF, PO_P63, or following conditions: 1. {FB_9 SIZING 0.011 μm in vertical direction}) DRC flags COD_H width between horizontal edges [PRL > 0.060 μm]	W1A	=	0.0600, 0.0900, 0.1200, 0.1500
COD_H.W.1.1.1	Width in vertical direction [INSIDE PO_P63] (Except BLK_WF, or following conditions: 1. {FB_9 SIZING 0.011 μm in vertical direction}) DRC flags COD_H width between horizontal edges [PRL > 0.064 μm, INSIDE PO_P63]	W1A	=	0.0600, 0.0900, 0.1200, 0.1500
COD_H.W.1.2	Width in vertical direction DRC flags DCOD_H width between horizontal edges [PRL > 0.060 μm]	W1B	=	0.0600, 0.0900, 0.1200, 0.1500, 0.1800
COD_H.W.4	Concave corner to concave corner width in vertical direction [-0.054 μm < PRL ≤ 0 μm] (Except following conditions: 1. concave corner to ALL_OD space ≥ 0.041 μm)	W4	≥	0.0600
COD_H.W.5.0.1	Width in horizontal direction [PRL > 0 μm]	W5	≥	0.0530
COD_H.W.5	Concave corner to concave corner width in horizontal direction [-0.060 μm < PRL ≤ 0 μm] (Except following conditions: 1. concave corner to concave corner width ≤ 0.001 μm in horizontal direction, 2. concave corner to ALL_OD space ≥ 0.041 μm)	W5	≥	0.0540
COD_H.W.6.1	Maximum width in vertical direction (Except TCDDMY)	W6A	≤	0.2400
COD_H.S.1	Space (Point touch is allowed)	S1	≥	0.0300
COD_H.S.4	Space of ALL_COD_H [PRL > 0 μm] in horizontal direction (Except FB_9, FB_8)	S4	≥	0.0850
COD_H.S.4.0.1	Space of {ALL_COD_H NOT DCOD_H} [PRL > 0 μm] in horizontal direction (Except FB_9, FB_8)	S4	≥	0.1080
COD_H.S.4.1	Space of ALL_COD_H [-0.030 μm < PRL ≤ 0 μm] in horizontal direction	S4A	≥	0.0460
COD_H.S.4.2	Space of ALL_COD_H [PRL > 0.0315 μm] in vertical direction	S4B	≥	0.0600
COD_H.S.5	Space to ALL_OD in vertical direction (Except BLK_WF)	S5	≥	0.0110
COD_H.S.6	Space to ALL_OD edge [between two consecutive 90-90 degree corners] in horizontal direction [PRL ≥ 0 μm] (Except TCDDMY)	S6	≥	0.0230

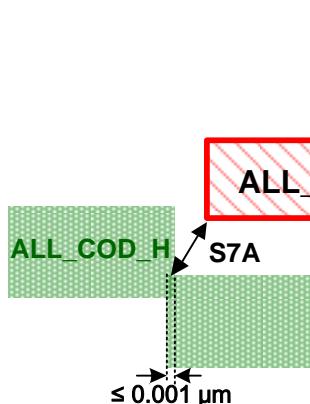
Rule No.	Description	Label	Op.	Rule
COD_H.S.7	Space of ALL_COD_H [point touch] to ALL_OD	S7	\geq	0.0510
COD_H.S.7.1	Space of Checked_COD_H to ALL_OD Definition of Checked_COD_H: ALL_COD_H [0 μm < concave corner to concave corner width ≤ 0.001 μm]	S7A	\geq	0.0510
COD_H.S.7.2	Space of Concave_COD_H to ALL_OD Definition of Concave_COD_H: Concave corner to concave corner width of ALL_COD_H in vertical direction < 0.060 μm [-0.054 μm < PRL ≤ 0 μm]	S7B	\geq	0.0410
COD_H.S.9.2	Space to SRM (50;0) in vertical direction [PRL > -0.106 μm] ({ALL_COD_H CUT SRM (50;0)} is not allowed)	S9B	\geq	0.2190
COD_H.S.9.3	Space to SRM (50;0) in horizontal direction [PRL > -0.189 μm]	S9C	\geq	0.1710
COD_H.S.10.4	Space of ALL_COD_H [NOT INSIDE SRM] to {{FB_9 OR FB_8} OR BV_FB [width = 0.240/0.300 μm]} [PRL > -0.122 μm] in vertical direction (Cut is not allowed)	S10D	\geq	0.1200
COD_H.S.10.4.1	Space of ALL_COD_H [NOT INSIDE SRM] to {{FB_9 OR FB_8} OR BV_FB [width = 0.240/0.300 μm]} in horizontal direction [PRL > -0.090 μm] (Cut is not allowed)	S10D1	\geq	0.1870
COD_H.EN.1	Enclosure by Chip_Boundary in vertical direction in chip level (Except BLK_WF, or following conditions: 1. ALL_COD_H inside {FB_9 SIZING 0.011 μm in vertical direction})	EN1	=	0.0300*n
COD_H.EN.1.1	Enclosure by prBoundary in vertical direction in cell level (Except BLK_WF, or following conditions: 1. ALL_COD_H inside {FB_9 SIZING 0.011 μm in vertical direction})	EN1	=	0.0300*n
COD_H.L.1	Horizontal edge length of rectangular ALL_COD_H	L1	\geq	0.1620
COD_H.L.2	For L-shape ALL_COD_H with jog height = 0.030 μm and short side width ≤ 0.060 μm, the jog length (horizontal edge length of 90-270 degree corners)	L2	\geq	0.0540
COD_H.L.3	Horizontal edge length between two consecutive 270-270 degree corners (U-shape ALL_COD_H)	L3	\geq	0.1080
COD_H.L.4	Horizontal edge length between two consecutive 270-90 degree corners (Stair-shape ALL_COD_H) (Except FB_8, or following conditions: 1. horizontal edge length ≤ 0.002 μm)	L4	\geq	0.0240
COD_H.A.1	Area	A1	\geq	0.01200
COD_H.A.2	Enclosed area (include surrounding by point-touch polygons)	A2	\geq	0.01300
COD_H.R.2	ALL_COD_H overlap ALL_OD is not allowed			
COD_H.R.4	ALL_COD_H must be orthogonal to grid			
COD_H.R.5	{ALL_OD {expanding horizontal edge by 0.011 μm}} horizontal edge must be fully projected to ALL_COD_H, and ALL_COD_H expanding from ALL_OD edge \geq 0.023 μm in horizontal direction (Except FB_9, FB_8, BLK_WF)			
COD_H.R.6	{Chip_Boundary NOT COD_S} must be fully covered by {ALL_COD_H OR ALL_COD_V} in chip level Definition of COD_S: {{{SRM OR FB_8} OR {{ALL_OD OR FB_9} OR TCDDMY} SIZING 0.011 μm in vertical direction}} OR {SEALRING_ALL OR {ICOVL_SINGLE SIZING 0.009 μm}}			

Rule No.	Description	Label	Op.	Rule
COD_H.R.6.1	{prBoundary NOT COD_S} must be fully covered by {ALL_COD_H OR ALL_COD_V} in cell level Definition of COD_S: {{{SRM OR FB_8} OR {{{ALL_OD OR FB_9} OR TCDDMY} SIZING 0.011 μm in vertical direction}} OR {SEALRING_ALL OR {ICOVL_SINGLE SIZING 0.009 μm}}}			

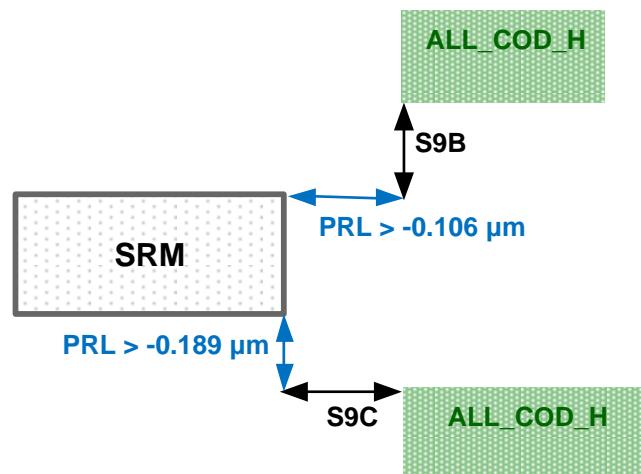
Rule No.	Description	Label	Op.	Rule
COD_V.W.1	Width of ALL_COD_V (Except FB_9)	W1	≥	0.0300
COD_V.W.2	Width of ALL_COD_V in vertical direction [PRL > 0.062 μm]	W2	≥	0.0600
COD_V.W.3	Width of ALL_COD_V in horizontal direction [PRL > 0.011 μm]	W3	≥	0.0460
COD_V.S.1	Space of ALL_COD_V	S1	≥	0.0080
COD_V.S.1.1	Space of ALL_COD_V in horizontal direction [PRL > 0.090 μm] (Except BLK_WF, SEALRING_ALL)	S1A	≥	0.1160
COD_V.S.1.2	Space of ALL_COD_V in vertical direction (Except FB_9, BLK_WF)	S1B	≥	0.1200
COD_V.S.3	Space of ALL_COD_V to ALL_OD in vertical direction (Except FB_9, BLK_WF)	S3	≥	0.0410
COD_V.O.1	ALL_COD_V overlap of ALL_COD_H in vertical direction (Overlap = 0 is allowed on BLK_WF boundary) (Except FB_9, FB_8)	O1	≥	0.0300
COD_V.L.1	Edge length of ALL_COD_V in vertical direction (Except BLK_WF)	L1	≥	0.0300
COD_V.A.1	Area of ALL_COD_V (Except BLK_WF, FB_9, FB_8)	A1	≥	0.01290
COD_V.A.2	Enclosed area of ALL_COD_V (Except FB_8, or following conditions: 1. Enclosed area [INTERACT FB_9])	A2	≥	0.02510
COD_V.R.2	ALL_COD_V overlap ALL_OD is not allowed			
COD_V.R.4	ALL_COD_V must be orthogonal to grid (Except SEALRING_ALL)			
COD_V.R.5	ALL_OD vertical edge must fully abut {ALL_COD_H OR ALL_COD_V} (Except following conditions: 1. {ALL_OD expanding horizontal edge 0.011 μm in vertical direction})			

COD_H

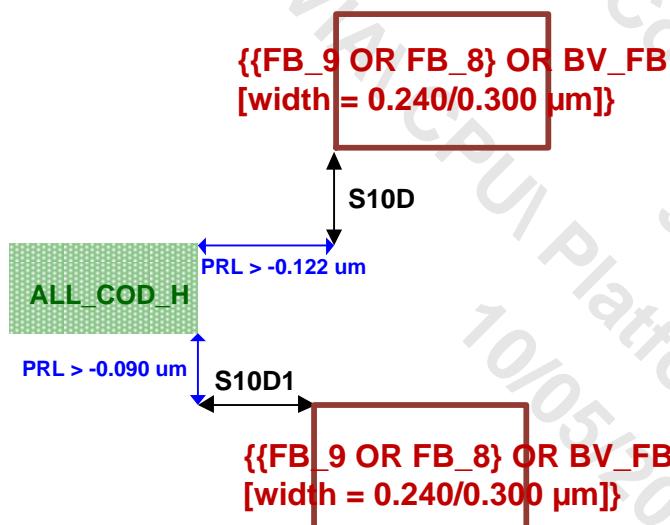




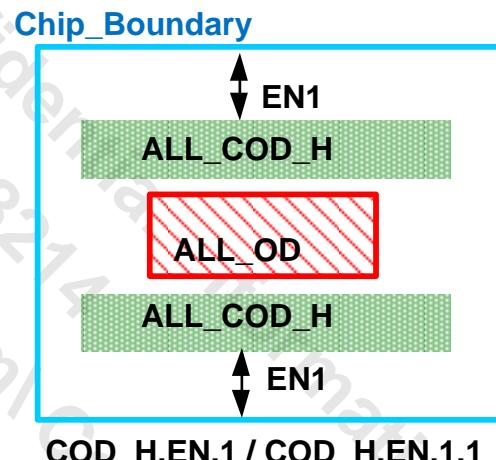
COD_H.S.7.1 / COD_H.S.7.2



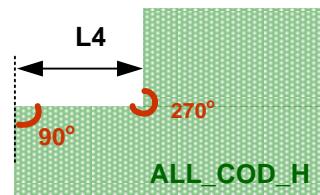
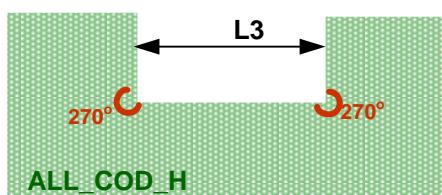
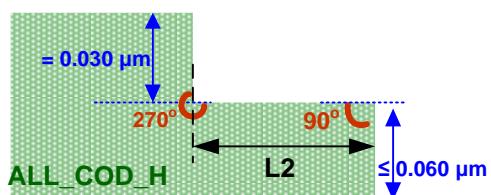
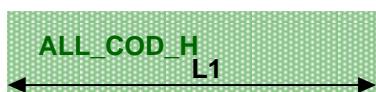
COD_H.S.9.2 / COD_H.S.9.3



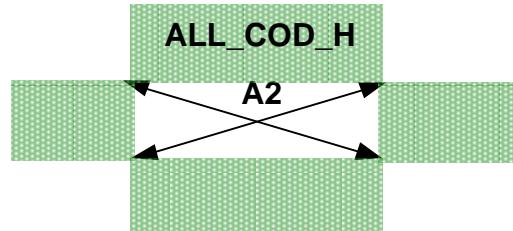
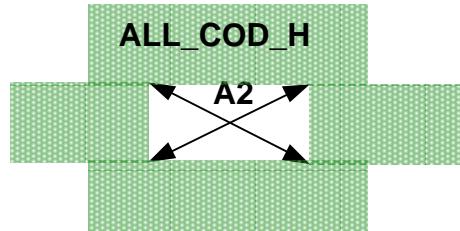
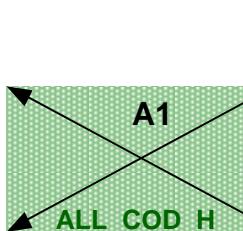
COD_H.S.10.4 / COD_H.S.10.4.1



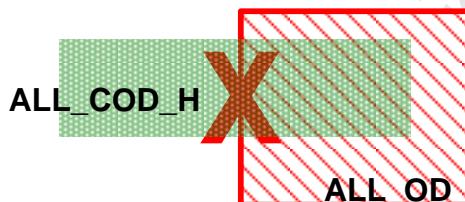
COD_H.EN.1 / COD_H.EN.1.1



COD_H.L.1 / COD_H.L.2/COD_H.L.3/COD_H.L.4

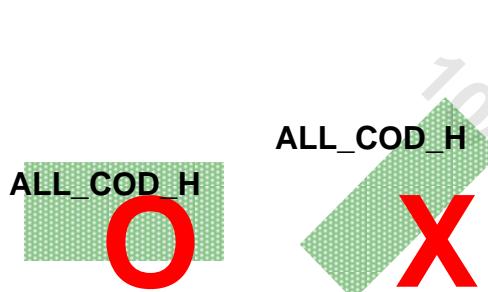


COD_H.A.1/COD_H.A.2

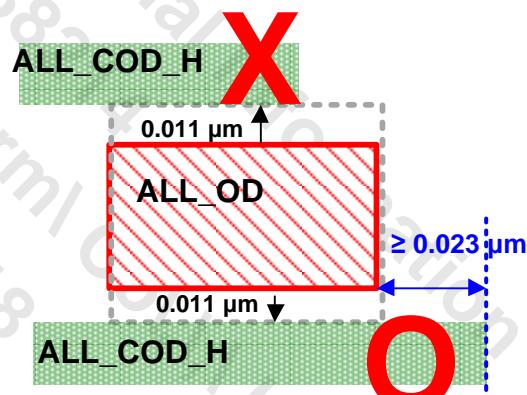


ALL_COD_H overlap ALL_OD is not allowed.

COD_H.R.2

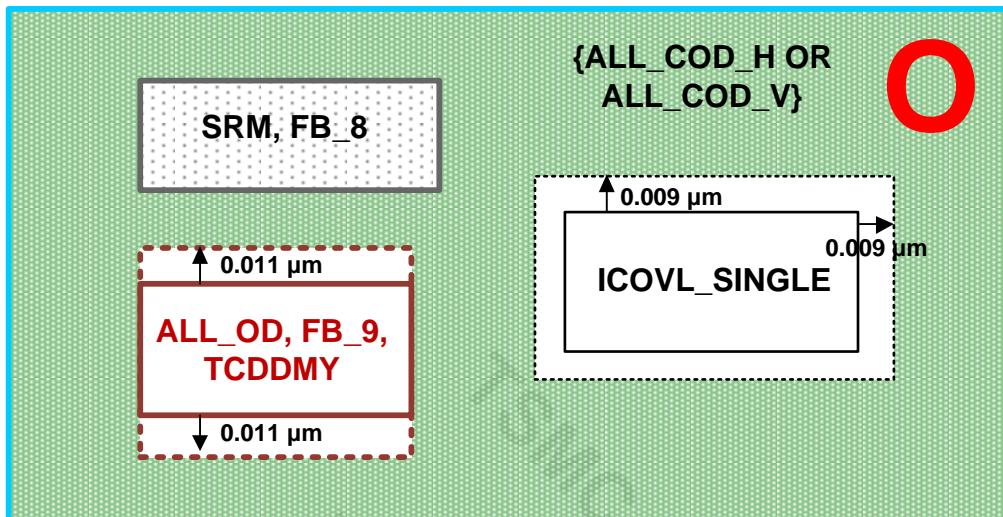


ALL_COD_H must be orthogonal to grid

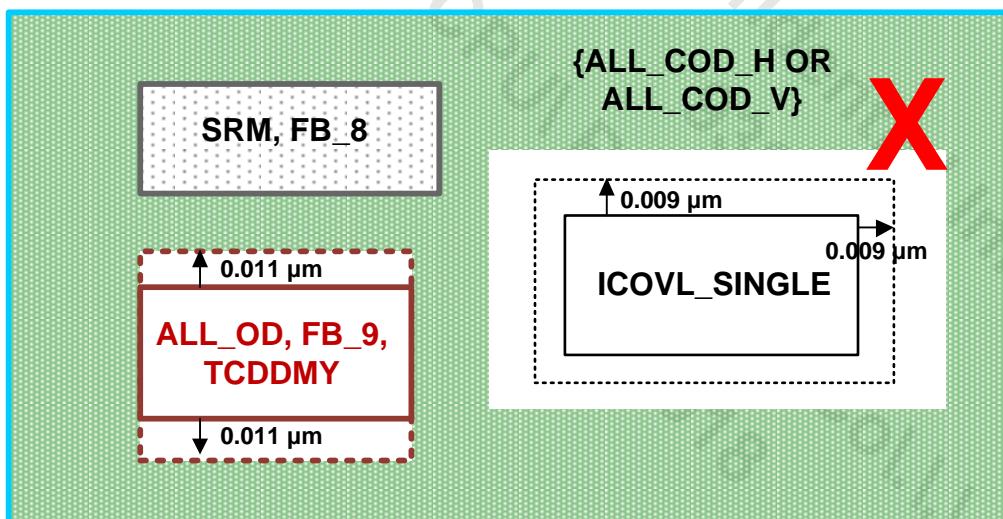


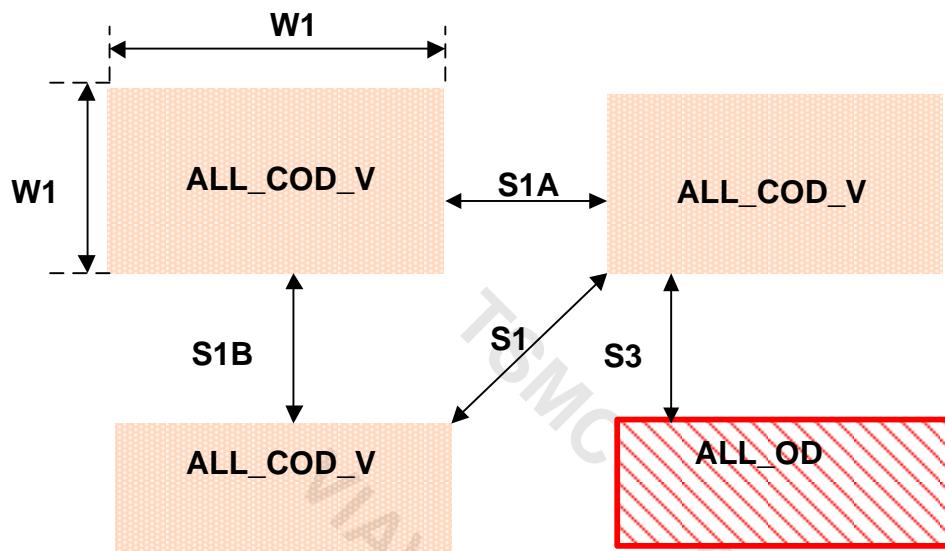
COD_H.R.4

COD_H.R.5

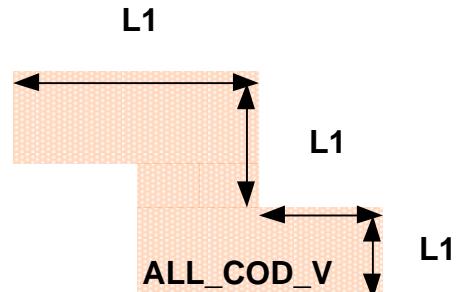
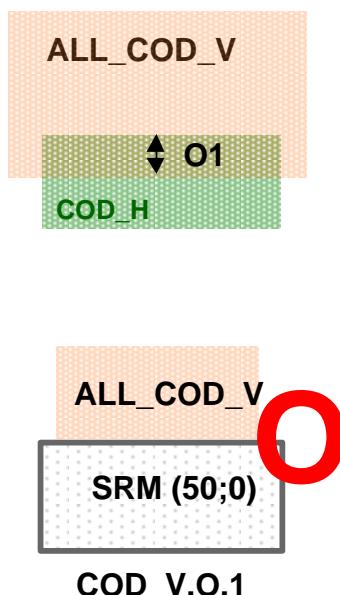
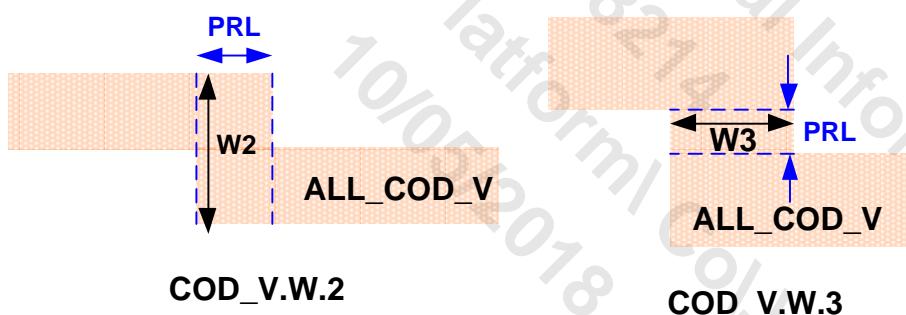
Chip_Boundary / prBoundary**Chip_Boundary / prBoundary**

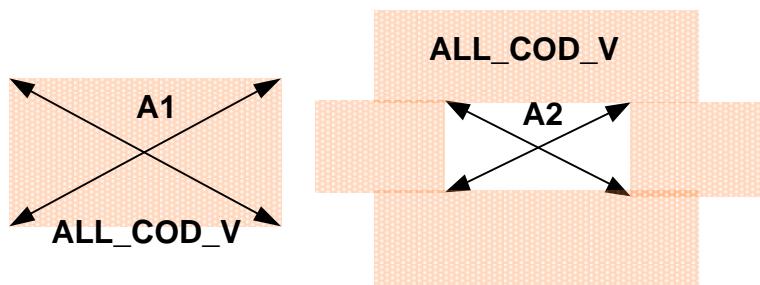
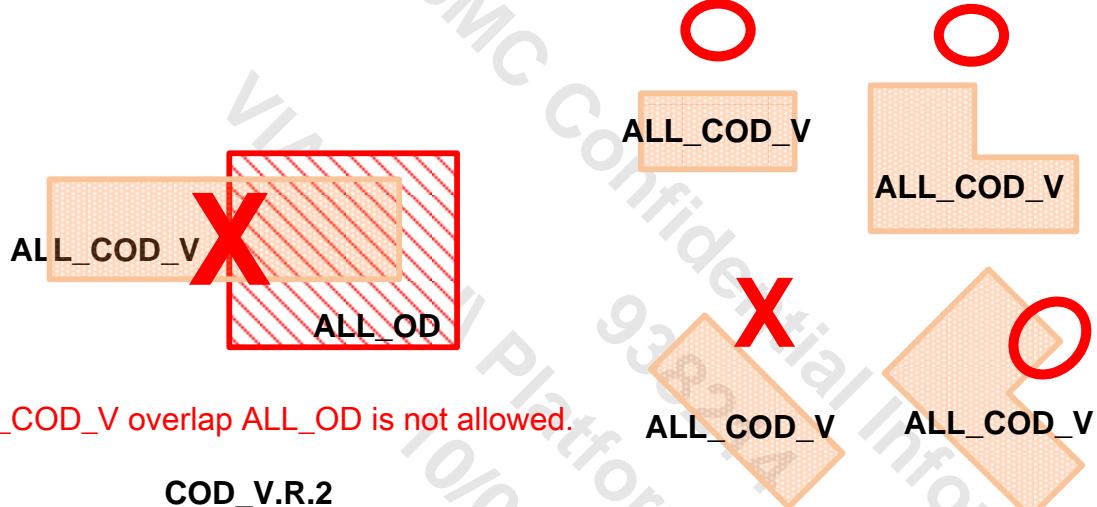
Must be fully covered

**COD_H.R.6 / COD_H.R.6.1**

COD_V

**COD_V.W.1 / COD_V.S.1 / COD_V.S.1.1 /
COD_V.S.1.2 / COD_V.S.3**

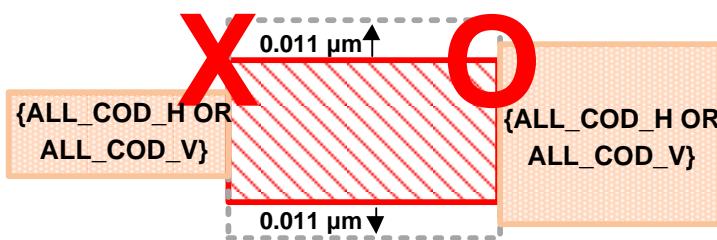
**COD_V.L.1**

**COD_V.A.1/COD_V.A.2**

ALL_COD_V overlap ALL_OD is not allowed.

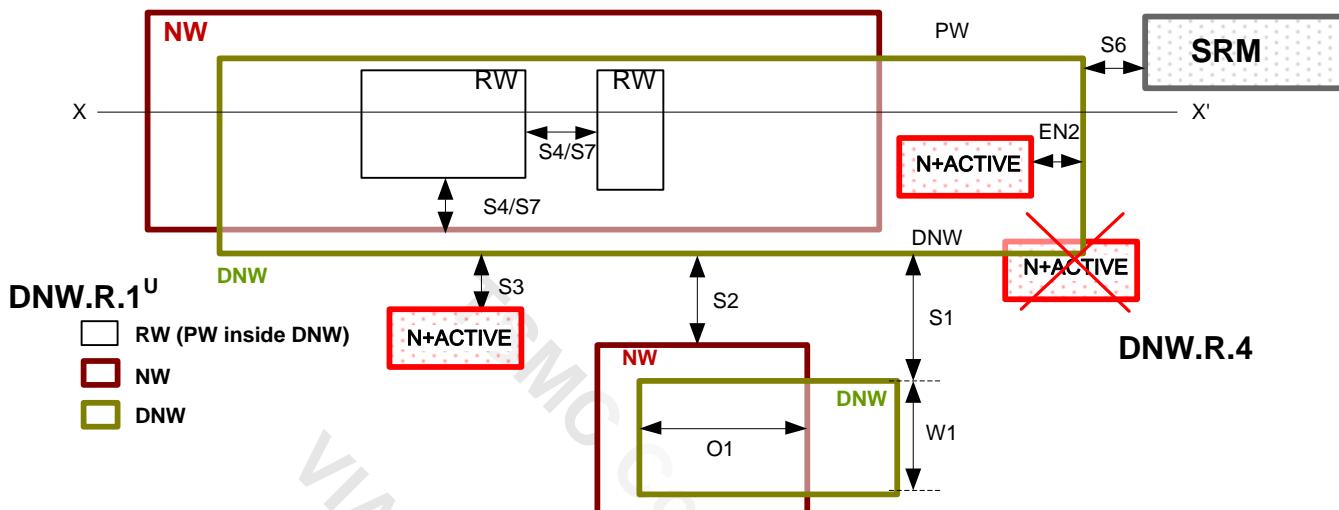
COD_V.R.2

ALL_COD_V must be orthogonal to grid

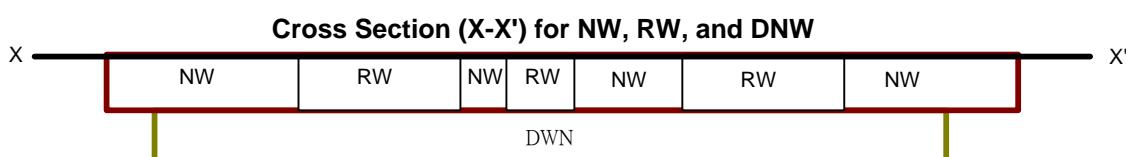
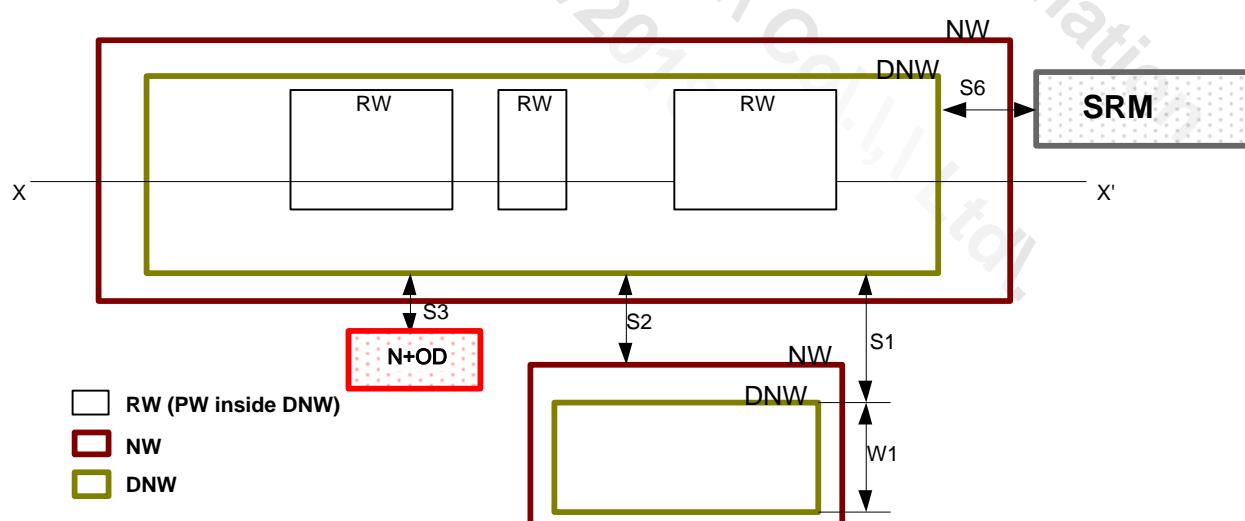
COD_V.R.4**COD_V.R.5**

4.5.5 Deep N-Well (DNW) Layout Rules [Optional]

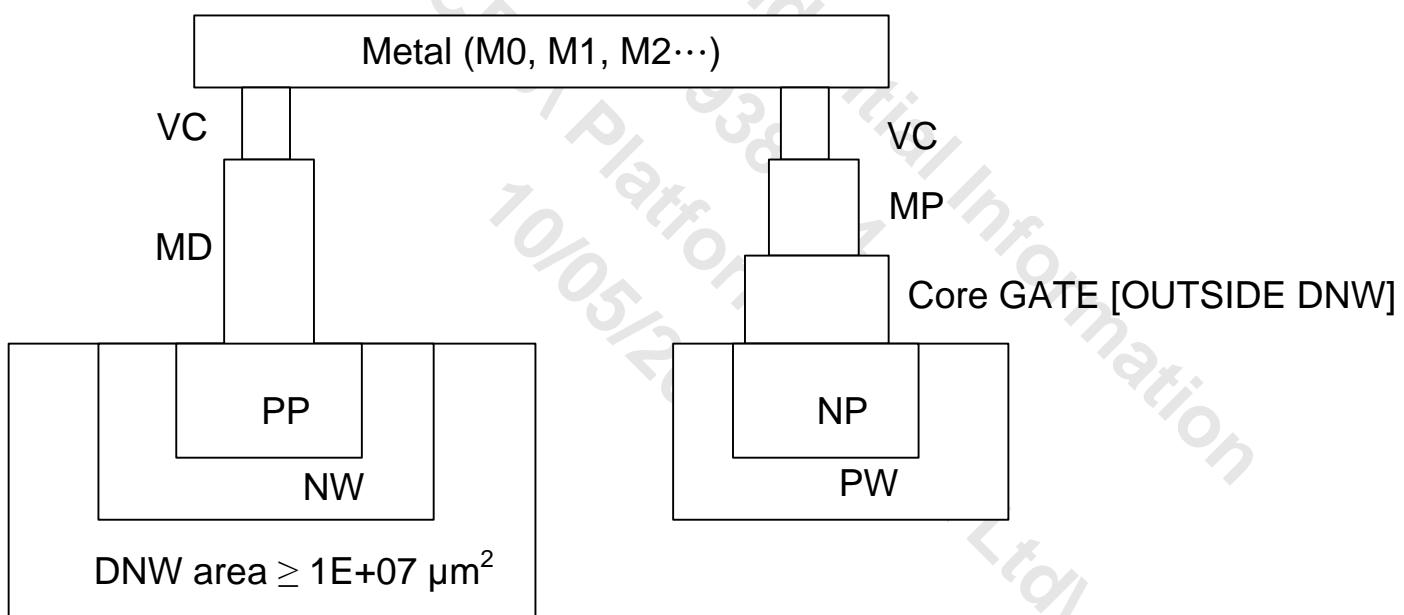
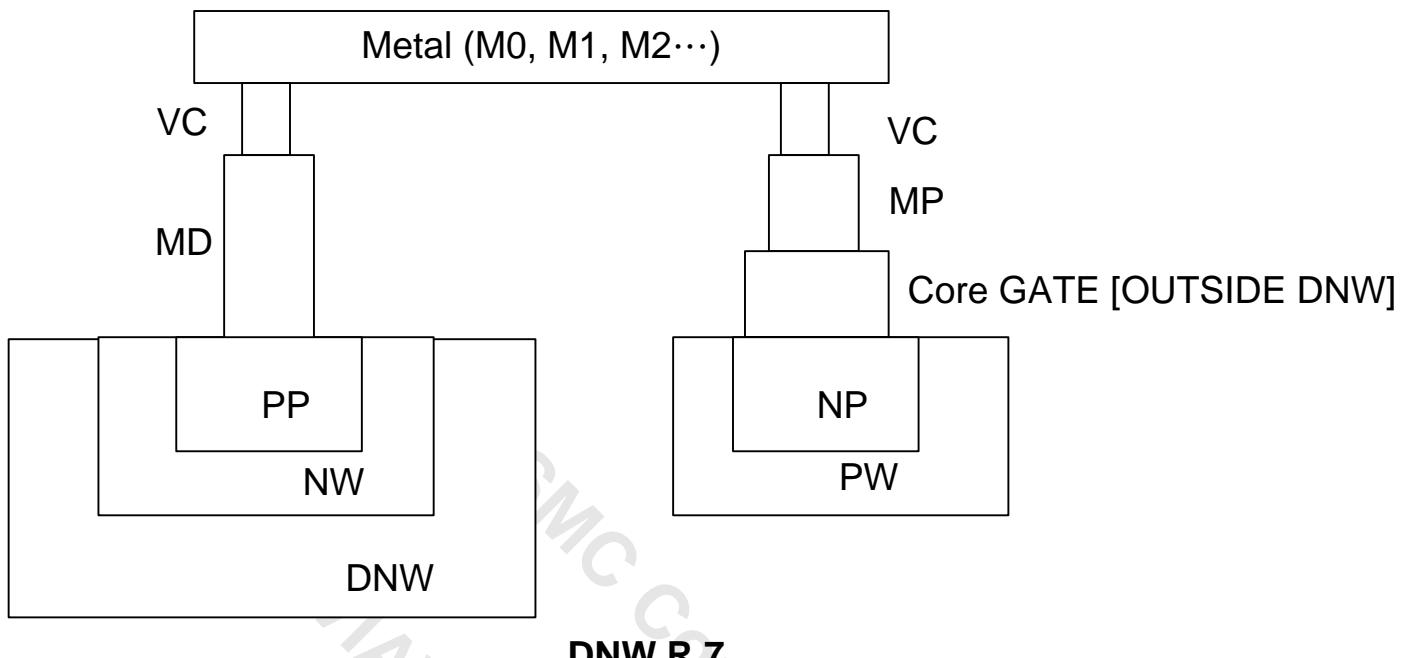
Rule No.	Description	Label	Op.	Rule
DNW.W.1	Width	W1	\geq	1.5
DNW.S.1	Space	S1	\geq	3.15
DNW.S.2	Space to NW with different potentials	S2	\geq	1.5
DNW.S.3	Space to {N+ ACTIVE OUTSIDE DNW}	S3	\geq	1.485
DNW.S.4	Space of RW to {RW OR PW} with different potential	S4	\geq	0.2400
DNW.S.6	Space to SRM (50;0) (Overlap is not allowed)	S6	\geq	1.5
DNW.S.7	Space of RW to {RW OR PW} [maximum delta V > 0.96V]	S7	\geq	0.5000
DNW.S.7.1	Space of RW to {RW OR PW} [maximum delta V > 1.32V] (1.2V + 10%) (Except IBJTDMY)	S7	\geq	0.7140
DNW.S.7.2	Space of RW to {RW OR PW} [maximum delta V > 1.65V] (1.5V + 10%) (Except IBJTDMY)	S7	\geq	0.9000
DNW.EN.2	Enclosure of N+ ACTIVE	EN2	\geq	0.4010
DNW.O.1	Overlap of NW	O1	\geq	0.3600
DNW.R.1 ^U	RW is the NW hole in DNW			
DNW.R.2 ^U	Keep {NW INTERACT DNW} and PW in reverse bias			
DNW.R.3 ^U	{NW INTERACT DNW} must be at the same potential			
DNW.R.4	{N+ ACTIVE CUT DNW} is not allowed			
DNW.R.5g ^U	Recommended not using floating RW unless necessary to avoid unstable device performance			
DNW.R.7	Maximum cumulative area ratio of DNW to {(NMOS core gates) OUTSIDE DNW} [connects to {P+ ACTIVE INSIDE {NW INTERACT DNW}}] (This rule is checked by the DRC command files in ANTENNA_DRC directory) Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	5.0E+06
DNW.R.7.1	Maximum cumulative area ratio of DNW [area \geq 1E+07 μm^2] to {(NMOS/P-VAR core gates) OUTSIDE DNW} [connects to {P+ ACTIVE INSIDE {NW INTERACT DNW}}, and does not connect to STRAP] (This rule is checked by the cumulative connections (from M0 to AP respectively) and the DRC command files in ANTENNA_DRC directory.) Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	5.0E+06
DNW.R.7.2	Maximum cumulative area ratio of DNW [area \geq 1E+07 μm^2] to {core_NMOS/P-VAR INSIDE DNW [area \leq 1E03 μm^2]} (This rule is checked by the cumulative connections (from M0 to AP respectively) and the DRC command files in ANTENNA_DRC directory.) Definition of core_NMOS/P-VAR: 1. NMOS and P-VAR gates do not inside OD2, and 2. Connect to {{PP AND OD} AND NW} INSIDE DNW [area \geq 1E+07 μm^2], and 3. Do not connect to STRAP Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	5.0E+06
DNW.R.8	Maximum delta V > 3.63V is not allowed. DRC searching range: 1. DNW space to DNW or NW is < 5 μm 2. RW space to RW or PW is < 5 μm			

DNW

DNW.W.1 / DNW.S.1 / DNW.S.2 / DNW.S.3 / DNW.S.4 / DNW.S.6 / DNW.S.7 / DNW.S.7.1 / DNW.S.7.2 / DNW.EN.2 / DNW.O.1 / DNW.R.1^U DNW.R.4



DNW.W.1 / DNW.S.1 / DNW.S.2 / DNW.S.3 / DNW.S.6



4.5.6 N-Well (NW) Layout Rules

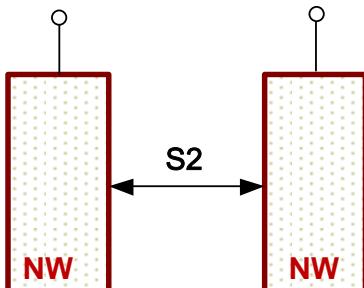
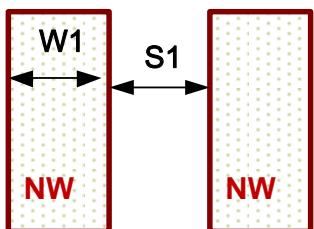
Rule No.	Description	Label	Op.	Rule
NW.W.1	Width (Except BLK_WF)	W1	\geq	0.1920
NW.W.1.1	Width [NW space < 0.224 μm]	W1A	\leq	0.3760
NW.W.1.3	{OD2 AND NW} width [{OD2 AND NW} space < 0.224 μm]	W1A	\leq	0.3760
NW.W.1.4	{OD2 NOT {NW OR NT_N}} width [{OD2 NOT {NW OR NT_N}} space < 0.224 μm]	W1A	\leq	0.3760
NW.S.1	Space (Except BLK_WF)	S1	\geq	0.1920
NW.S.1.1	Space of NW [width < 0.224 μm] (Except BLK_WF)	S1A	\leq	0.3760
NW.S.1.3	Space of {OD2 AND NW} [width < 0.224 μm]	S1A	\leq	0.3760
NW.S.1.4	Space of {OD2 NOT {NW OR NT_N}} [width < 0.224 μm]	S1A	\leq	0.3760
NW.S.2	Space to NW on different net	S2	\geq	0.2400
NW.S.5	Space to ALL_OD ({ALL_OD CUT NW} is not allowed) (Except BLK_WF, Dummy_Cell)	S5	\geq	0.0410
NW.S.5.1	Space to {ALL_OD INTERACT OD2} (Except Dummy_Cell)	S5A	\geq	0.1610
NW.S.7	Space of NW to ALL_OD [at least one edge at each corner] (Except Dummy_Cell)	S7	\geq	0.0710
NW.S.7.1	Space of NW to ALL_OD [at least one adjacent edge of NW space to ALL_OD < 0.050 μm] (Except Dummy_Cell)	S7A	\geq	0.0770
NW.S.8.1	Space of NW [edge length < 0.290 μm , PRL > 0 μm] to OD (Except Dummy_Cell)	S8A	\geq	0.0800
NW.S.9	Space to SRM (50;0) (Space = 0 μm is allowed)	S9	\geq	0.3600
NW.S.10	Space of NW [PRL > 0.250 μm] (Except BLK_WF)	S10	\geq	0.2400
NW.S.10.1	Space of {OD2 AND NW} [PRL > 0.250 μm]	S10A	\geq	0.2500
NW.S.11	Space to NW [maximum delta V > 0.96V]	S11	\geq	0.5000
NW.S.11.1	Space to NW [maximum delta V > 1.32V] (1.2V + 10%)	S11	\geq	0.7140
NW.S.11.2	Space to NW [maximum delta V > 1.65V] (1.5V + 10%)	S11	\geq	0.9000
NW.S.12	Space to OD [maximum delta V > 0.96V]	S12	\geq	0.0750
NW.S.12.1	Space to OD [maximum delta V > 1.32V] (1.2V + 10%)	S12	\geq	0.1390
NW.S.12.2	Space to OD [maximum delta V > 1.65V] (1.5V + 10%)	S12	\geq	0.1610
NW.S.13	Space of PW to OD [maximum delta V > 0.96V]	S13	\geq	0.0750
NW.S.13.1	Space of PW to OD [maximum delta V > 1.32V] (1.2V + 10%)	S13	\geq	0.1390
NW.S.13.2	Space of PW to OD [maximum delta V > 1.65V] (1.5V + 10%)	S13	\geq	0.1610
NW.EN.1	Enclosure of ALL_OD (Except BLK_WF, Dummy_Cell)	EN1	\geq	0.0410
NW.EN.1.1	Enclosure of {ALL_OD INTERACT OD2} (Except Dummy_Cell)	EN1A	\geq	0.1610
NW.EN.3	NW enclosure of ALL_OD [at least one edge at each corner] (Except Dummy_Cell)	EN3	\geq	0.0710
NW.EN.3.1	NW enclosure of ALL_OD [at least one adjacent edge of NW enclosure of ALL_OD < 0.050 μm] (Except Dummy_Cell)	EN3A	\geq	0.0770
NW.EN.5	NW [edge length < 0.290 μm , PRL > 0 μm] enclosure of OD (Except Dummy_Cell)	EN5	\geq	0.0800
NW.EN.6	NW [vertical edge length < 1.1 μm between 2 consecutive 90-90 degree corners, PRL > 0 μm] enclosure of ALL_OD in horizontal direction (Except BLK_WF, RH_TNB)	EN6	\leq	0.2000
NW.L.1	Length of 45-degree bent NW (minimum edge length)	L1	\geq	0.4500
NW.A.1	Area	A1	\geq	0.18800

Rule No.	Description	Label	Op.	Rule
NW.A.2	Area of {OD2 NOT {NW OR NT_N}}, and {OD2 AND NW}	A2	\geq	0.28800
NW.A.3	Enclosed area	A3	\geq	0.18800
NW.A.4	Enclosed area of {OD2 NOT {NW OR NT_N}}, and {OD2 AND NW}	A4	\geq	0.28800
NW.R.1g ^U	Recommend not using unintentional floating well to avoid unstable device performance			
NW.R.3	Maximum delta V > 3.63V is not allowed. DRC searching range: 1. NW space to NW is < 1.8 μ m 2. NW space to N+ ACTIVE or PWSTRAP is < 1.63 μ m 3. PW space to P+ ACTIVE or NWSTRAP is < 1.63 μ m			
NW.R.4	{SR_DOD NOT SR_DPO} [INSIDE Dummy_Cell and INTERACT DNW] intersecting NW forms \geq 2 SR_DOD is not allowed			

TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

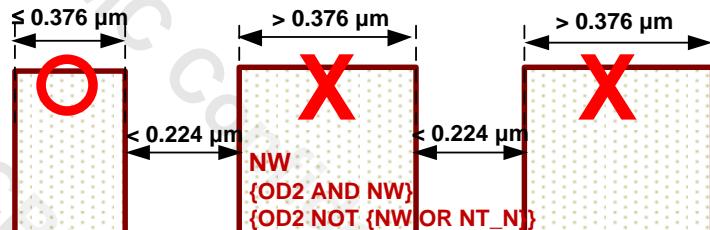
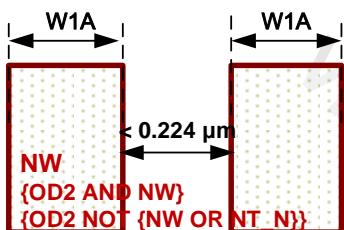
NW

With different potential

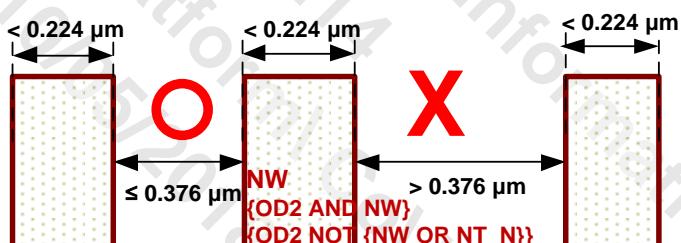
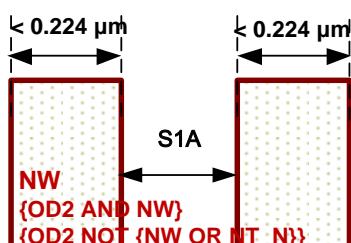


NW.W.1 / NW.S.1

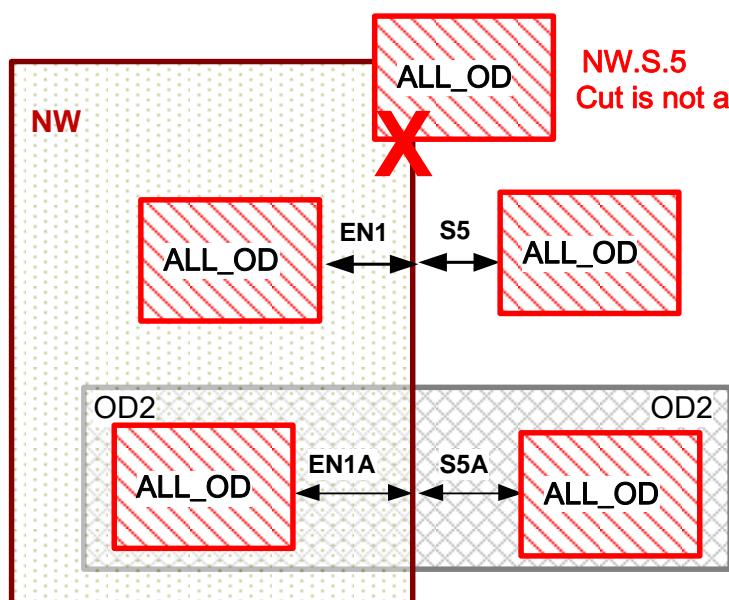
NW.S.2



NW.W.1.1 / NW.W.1.3 / NW.W.1.4

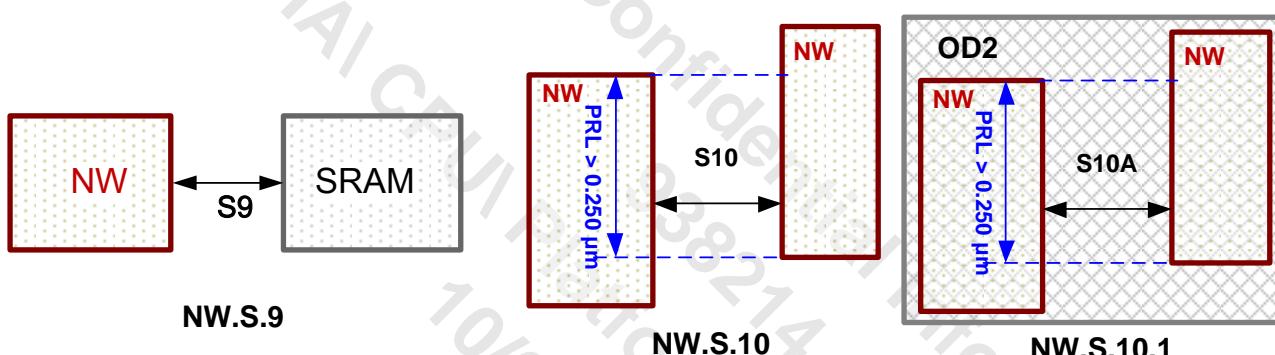
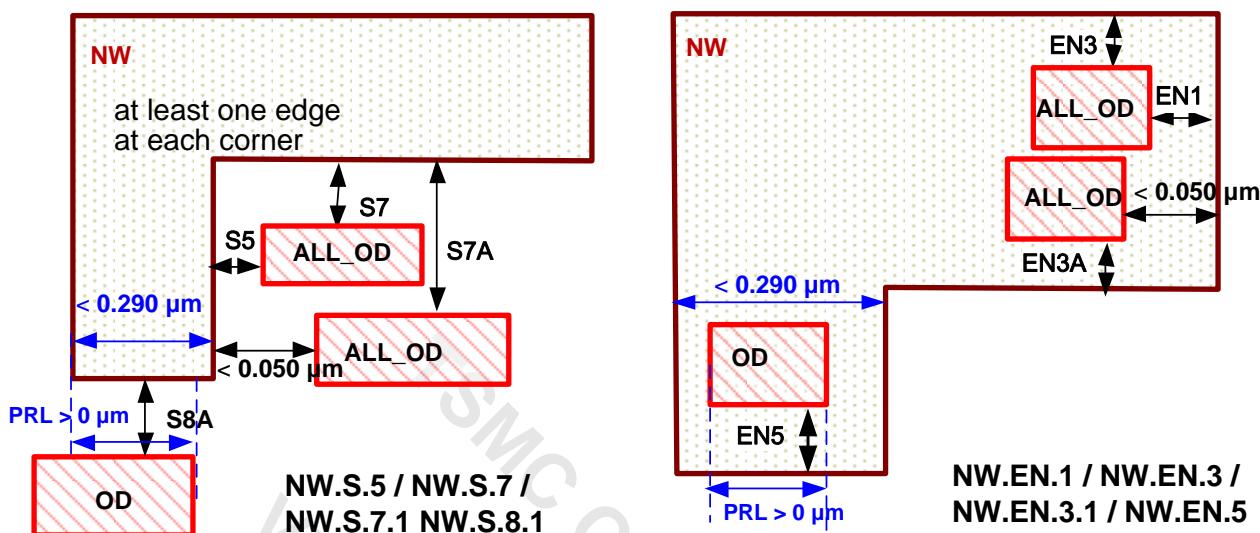


NW.S.1.1 / NW.S.1.3 / NW.S.1.4

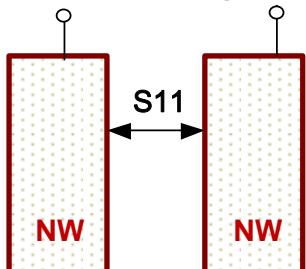


NW.S.5 / NW.S.5.1/ NW.EN.1/ NW.EN.1.1

at least one edge
at each corner

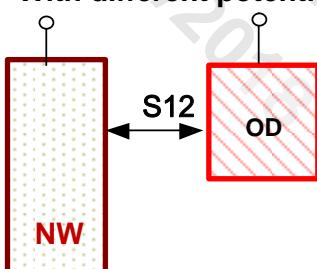


With different potential



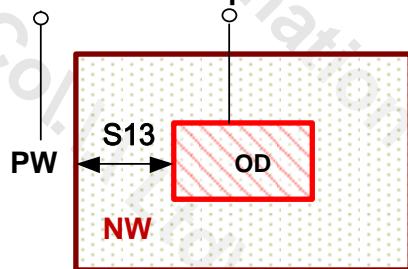
NW.S.11 / NW.S.11.1 / NW.S.11.2

With different potential

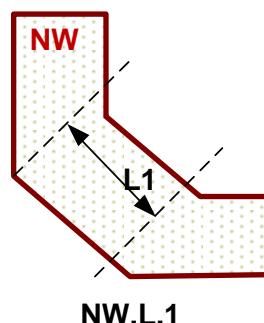
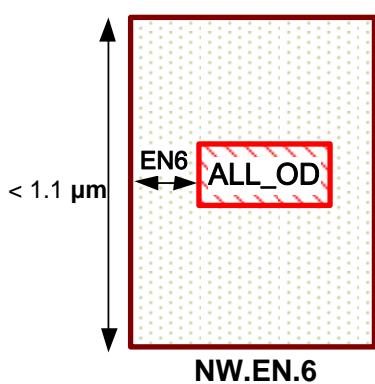


NW.S.12 / NW.S.12.1 / NW.S.12.2

With different potential



NW.S.13 / NW.S.13.1 / NW.S.13.2

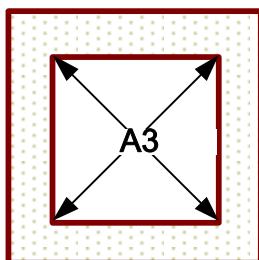


NW,
{OD2 NOT {NW OR NT_N}},
{OD2 AND NW}



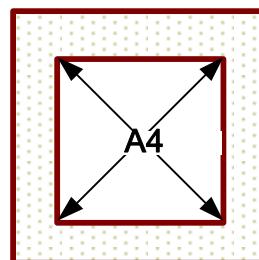
NW.A.1 / NW.A.2

NW

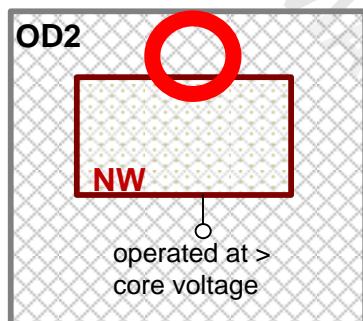


NW.A.3

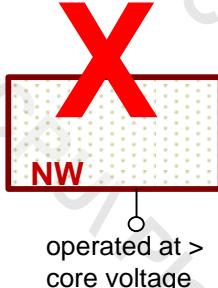
**{OD2 NOT {NW OR NT_N}},
{OD2 AND NW}**



NW.A.4



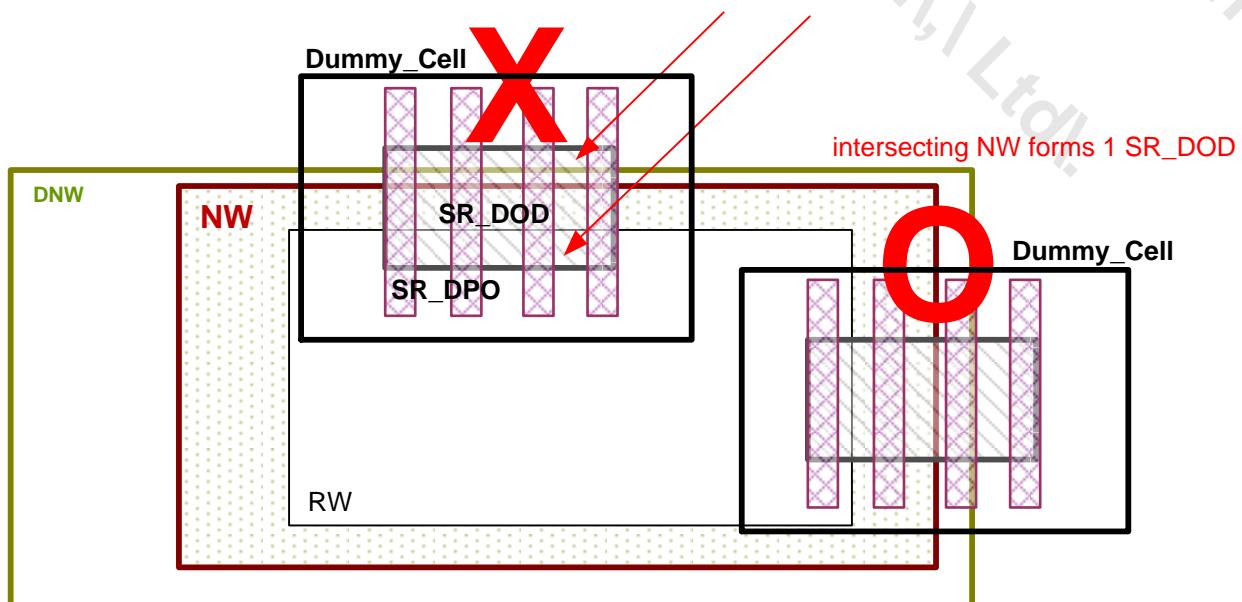
OD2 must cover NW [operated at > core voltage]



operated at >
core voltage

N.W.R.2^u

{SR_DOD NOT SR_DPO} [INSIDE Dummy_Cell and INTERACT DNW] intersecting NW forms ≥ 2
SR_DOD is not allowed



NW.R.4

4.5.7 N-Well Under STI (NWRSTI) Layout Rules

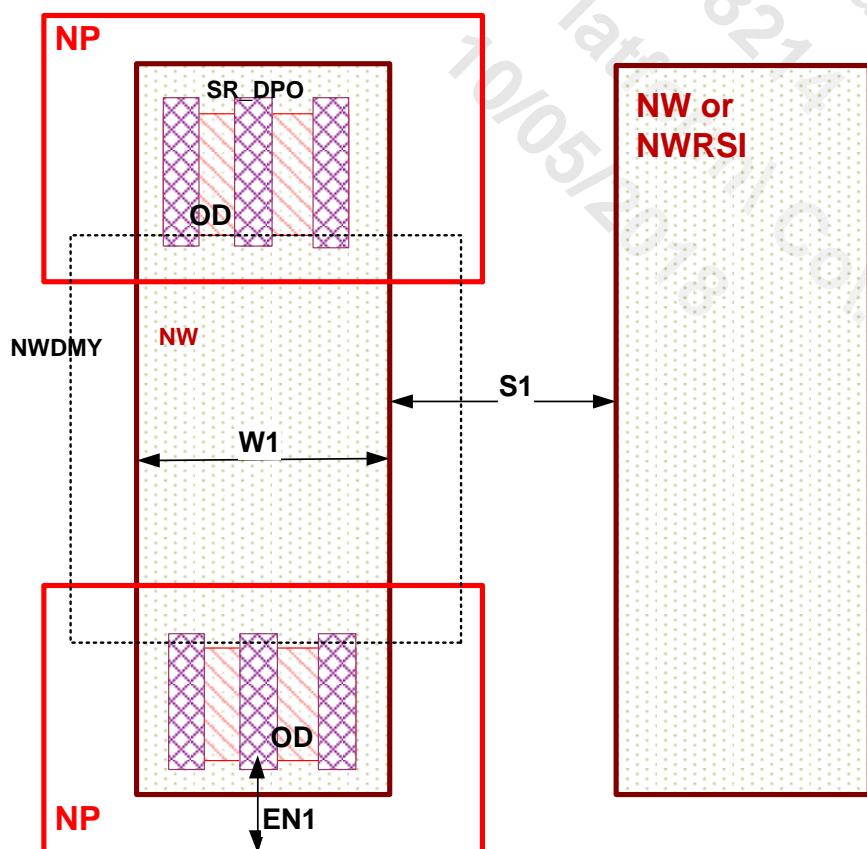
NWDMY1 (114;0) is required for NWELL 2 terminal resistor.

NWDMY2 (114;1) is required for NWELL 3 terminal resistor.

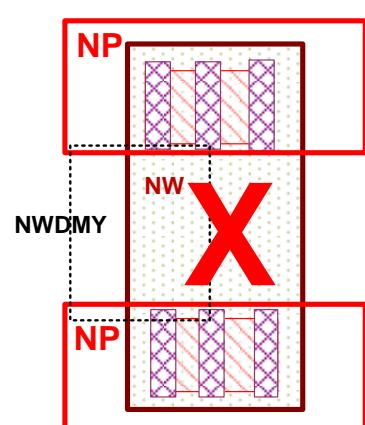
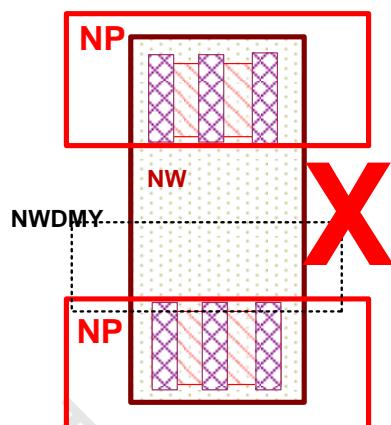
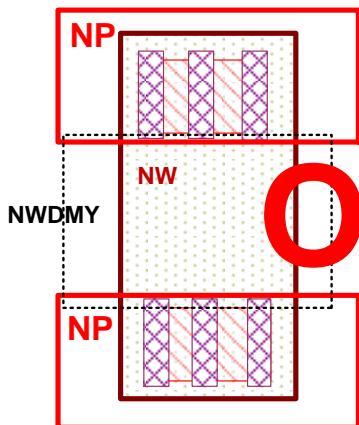
NWDMY = {NWDMY1 OR NWDMY2}

Rule No.	Description	Label	Op.	Rule
NWRSTI.W.1	Width	W1	\geq	1.388
NWRSTI.S.1	Space to NWRSTI or to NW	S1	\geq	0.9000
NWRSTI.EN.1	NP enclosure of {OD INTERACT NWRSTI}	EN1	\geq	0.3600
NWRSTI.R.1	NWDMY must abut OD			
NWRSTI.R.2	NWDMY intersecting NWRSTI must form two or more NWs			
NWRSTI.R.3g	Recommended to use rectangle shape resistor DRC flags {NWDMY AND NWRSTI} is not a rectangle			
NWRSTI.R.4	{NP INTERACT NWDMY} OR NWDMY overlap DNW, PP, OD2, VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P is not allowed (Except Dummy_Cell)			
NWRSTI.R.5	OD [INTERACT NWDMY] must be inside NW			
NWRSTI.R.7	NW [INTERACT NWDMY] overlap TrGATE is not allowed			
NWRSTI.R.8	NWDMY1 overlap NWDMY2 is not allowed			

NWRSTI



NWRSTI.W.1/ NWRSTI.S.1/ NWRSTI.EN.1

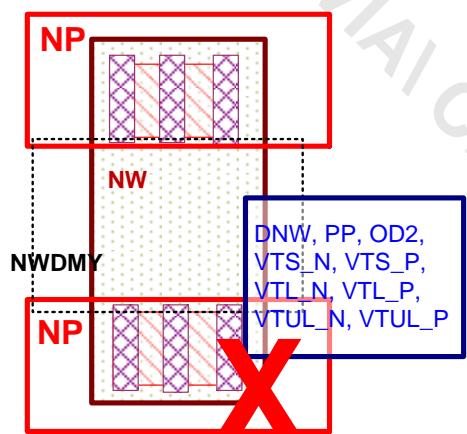


NWDMDY must abut with OD edge

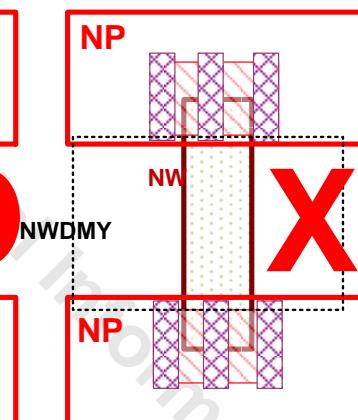
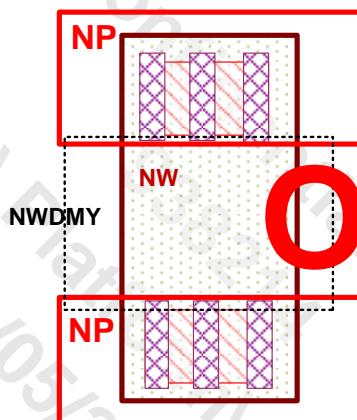
NWDMDY intersecting NWRSTI must form two or more NWs

NWRSTI.R.1

NWRSTI.R.2



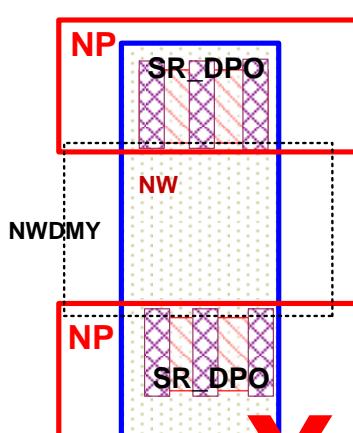
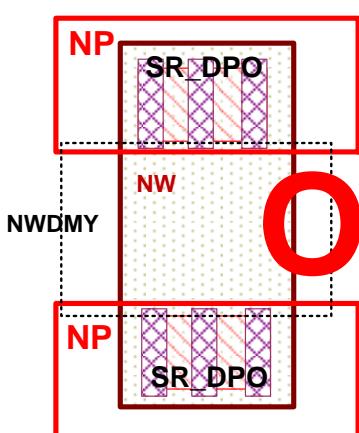
{NP INTERACT NWDMDY} OR NWDMDY overlap of DNW, PP, OD2, VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P is not allowed



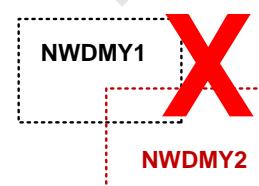
OD [INTERCAT NWDMDY] must fully inside NW

NWRSTI.R.4

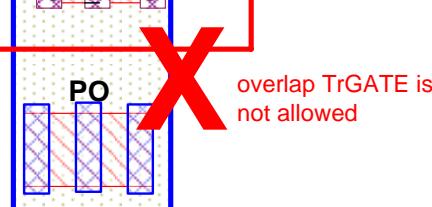
NWRSTI.R.5



Overlap is not allowed



NWRSTI.R.7



overlap TrGATE is not allowed

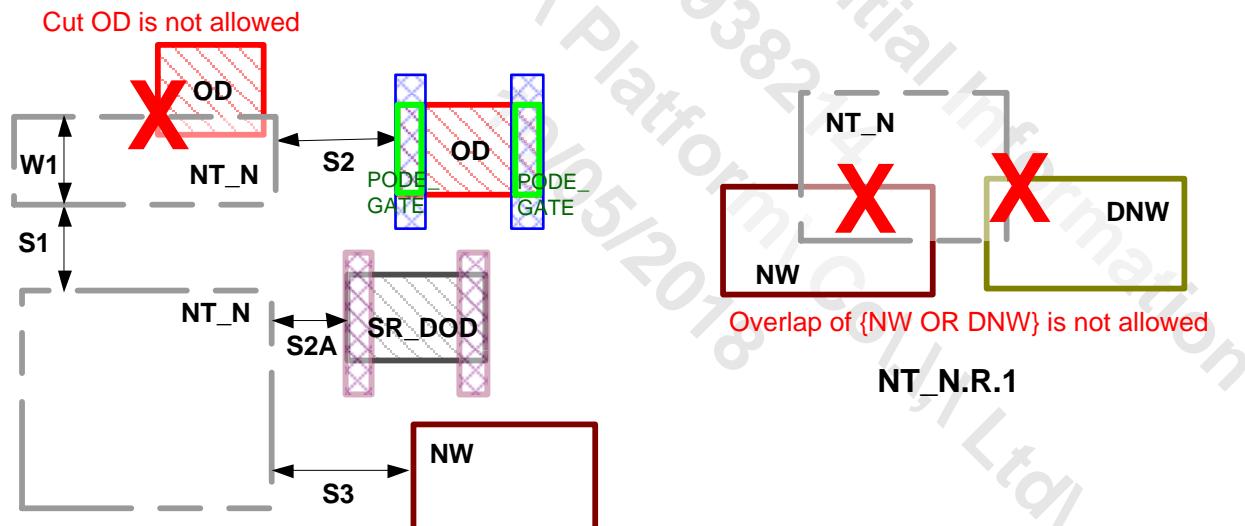
NWRSTI.R.8

4.5.8 NT_N Layout Rules

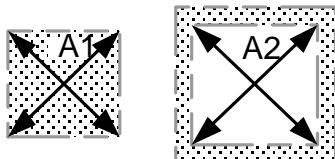
NT_N layer (CAD layer: 11;0) is only for Well implant blocking, and no native Vt NMOS devices offering. OD inside NT_N only can be used for NT_N potential pickup purpose, such as the guard-ring of MOM and inductor.

Rule No.	Description	Label	Op.	Rule
NT_N.W.1	Width	W1	\geq	0.2400
NT_N.S.1	Space	S1	\geq	0.2400
NT_N.S.2	Space to OD (Cut is not allowed)	S2	\geq	0.3420
NT_N.S.2.1	Space to SR_DOD	S2A	\geq	0.1260
NT_N.S.3	Space to NW	S3	\geq	0.7200
NT_N.A.1	Area	A1	\geq	0.32400
NT_N.A.2	Enclosed area	A2	\geq	0.32400
NT_N.R.1	Overlap {NW OR DNW} is not allowed			
NT_N.R.2	Overlap TrGATE is not allowed			

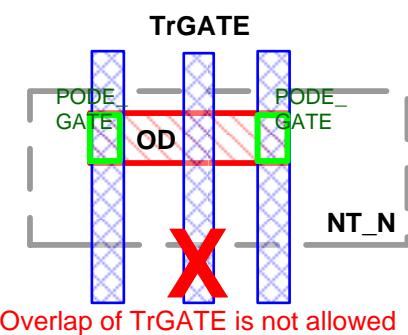
NT_N



NT_N.W.1 / NT_N.S.1 / NT_N.S.2
NT_N.S.2.1 / NT_N.S.3



NT_N.A.1 / NT_N.A.2



NT_N.R.2

4.5.9 OD2 Layout Rules

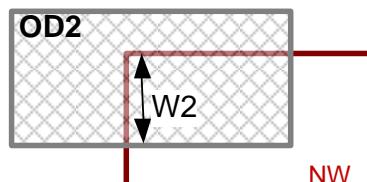
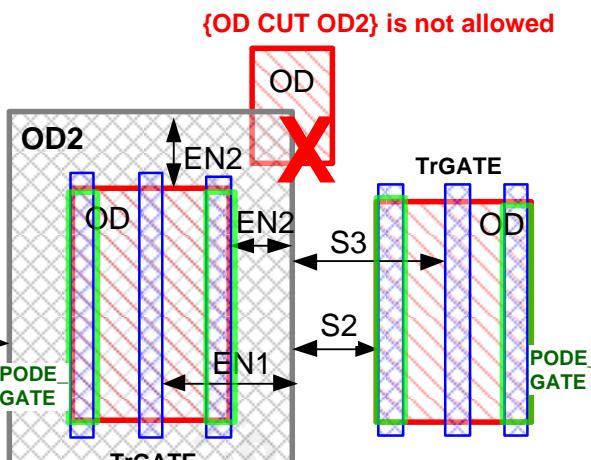
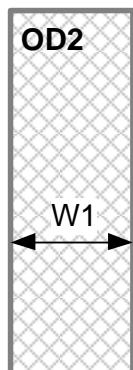
Define thick oxide area of 1.5V/1.8V I/O transistors.

The OD_18 layer (CAD layer: 16;0) is used for N7+ 1.8V gate oxide area.

The OD_15 layer (CAD layer: 21;0) is used for N7+ 1.5V gate oxide area.

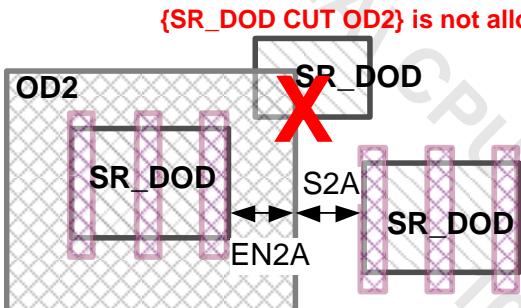
OD2 refers to any thick oxide device, for example, OD2 = {OD_18 OR OD_15}.

Rule No.	Description	Label	Op.	Rule
OD2.W.1	Width	W1	\wedge	0.2880
OD2.W.2	Width of {OD2 AND NW}	W2	\wedge	0.2400
OD2.W.3	Width of {OD2 NOT {NW OR NT_N}}	W3	\wedge	0.2400
OD2.S.1	Space	S1	\wedge	0.2880
OD2.S.2	Space to OD ({OD CUT OD2} is not allowed)	S2	\wedge	0.1170
OD2.S.2.1	Space to SR_DOD (SR_DOD cut OD2 is not allowed)	S2A	\wedge	0.0720
OD2.S.3	Space to core TrGATE in horizontal direction	S3	\wedge	0.1920
OD2.S.4	Space to NW (Space = 0 μ m is allowed)	S4	\wedge	0.2400
OD2.S.6	Space of {OD2 AND NW}	S6	\wedge	0.1920
OD2.S.7	Space of {OD2 NOT {NW OR NT_N}}	S7	\wedge	0.1920
OD2.EN.1	Enclosure of {OD2 AND TrGATE} in horizontal direction	EN1	\wedge	0.1920
OD2.EN.2	Enclosure of OD	EN2	\wedge	0.1170
OD2.EN.2.1	Enclosure of SR_DOD	EN2A	\wedge	0.0720
OD2.EX.1	NW extension on OD2 (Extension = 0 μ m is allowed)	EX1	\wedge	0.2400
OD2.EX.2	Extension on NW (Extension = 0 μ m is allowed)	EX2	\wedge	0.2400
OD2.O.1	Overlap of NW (Overlap = 0 μ m is allowed)	O1	\wedge	0.2400
OD2.A.1	Area	A1	\wedge	0.28800
OD2.A.2	Enclosed area	A2	\wedge	0.28800
OD2.R.1	OD2 must be orthogonal to grid			
OD2.R.2	OD_18 overlap OD_15 is not allowed			
OD2.R.3	OD_15 overlap VAR, IBJTDNY is not allowed			

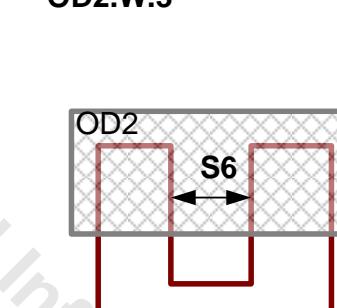
OD2

OD2.W.2

OD2.W.1 / OD2.S.1 / OD2.S.2
OD2.S.3 / OD2.EN.1 / OD2.EN.2



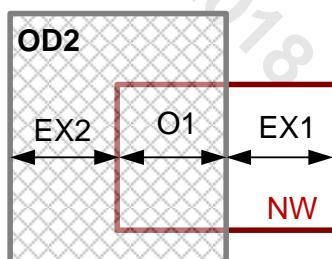
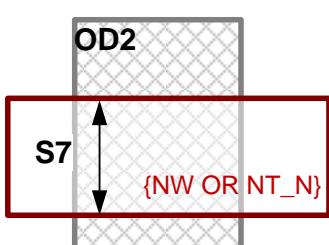
OD2.W.3



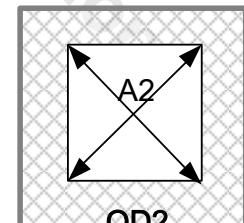
OD2.S.6

OD2.S.2.1 / OD2.EN.2.1

OD2.S.4



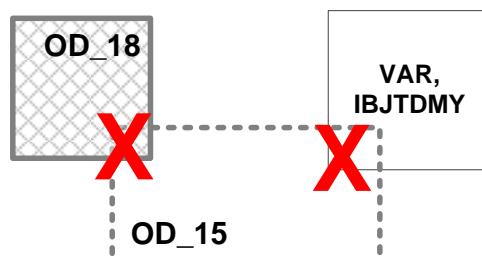
OD2.EX.1 / OD2.EX.2 /
OD2.O.1



OD2.A.1 / OD2.A.2



OD2.R.1



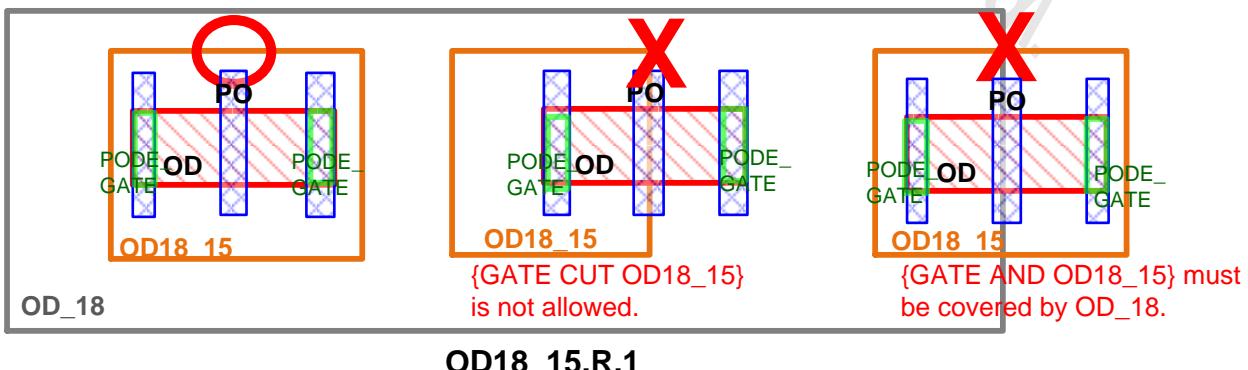
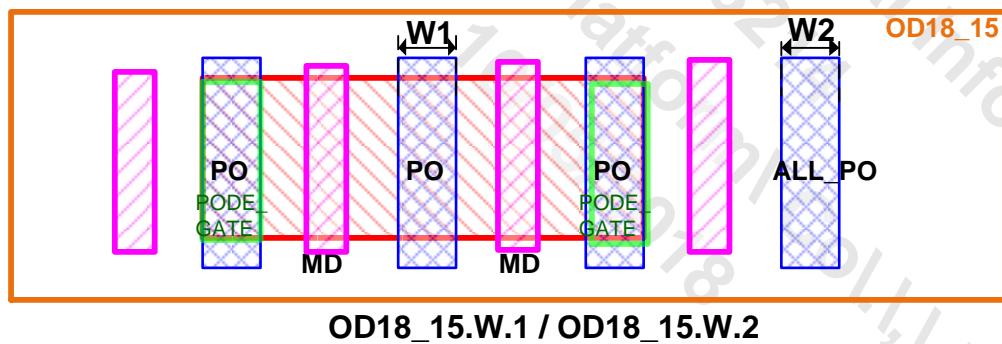
OD2.R.2 / OD2.R.3

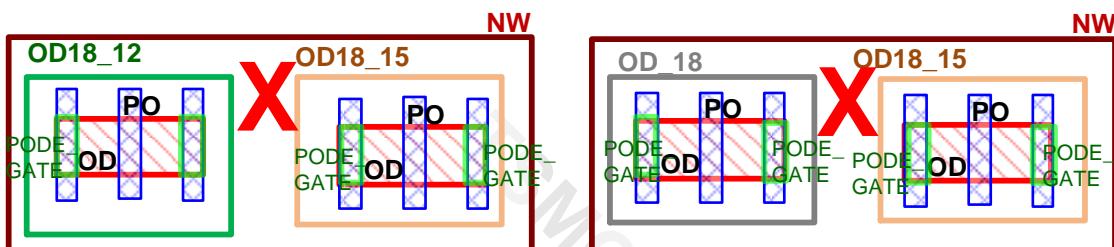
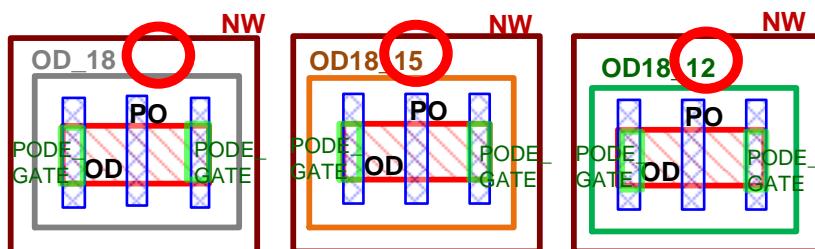
4.5.10 OD18_15 Layout Rules

OD18_15 (CAD layer:16;4) is only used for 1.8V underdrive to 1.5V in N7+ process. This is not a mask layer.

Rule No.	Description	Label	Op.	Rule
OD18_15.W.1	Channel length of 1.8V MOS underdrive to 1.5V {GATE AND OD18_15}	W1	=	0.0860~0.2400
OD18_15.W.2	ALL_PO width of 1.8V MOS underdrive to 1.5V {ALL_PO AND OD18_15} (Except following conditions: 1. {{DC_CORE OR DC_IO} OR DC_WPO})	W2	=	0.0860~0.2400
OD18_15.R.1	{GATE AND OD18_15} must be covered by OD_18. {GATE CUT OD18_15} is not allowed			
OD18_15.R.2	1.8V TrGATE, 1.5V TrGATE, 1.2V TrGATE cannot share the same NW			
OD18_15.R.3	OD18_15 must be orthogonal to grid			
OD18_15.R.5	{GATE AND OD18_15} can't overlap OD18_12			
OD18_15.R.5.1	{TrGATE AND OD18_15} can't overlap VAR			

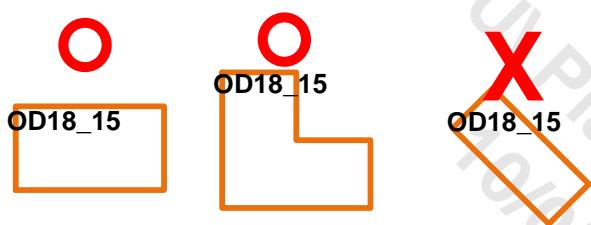
OD18_15





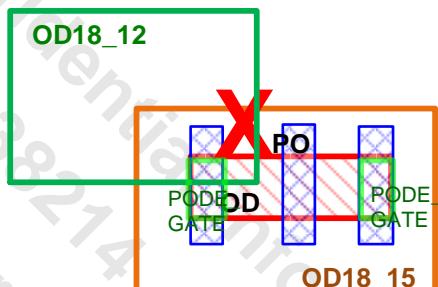
1.8V TrGATE, 1.5V TrGATE or 1.2V cannot share the same NW.

OD18_15.R.2



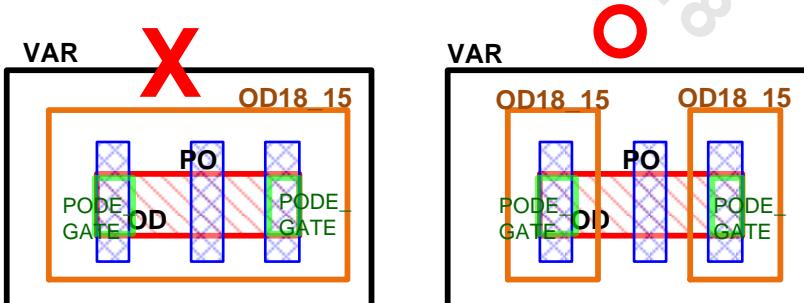
OD18_15 must be orthogonal to grid

OD18_15.R.3



{GATE AND OD18_15} can't overlap OD18_12

OD18_15.R.5



{TrGATE AND OD18_15} overlap VAR is not allowed

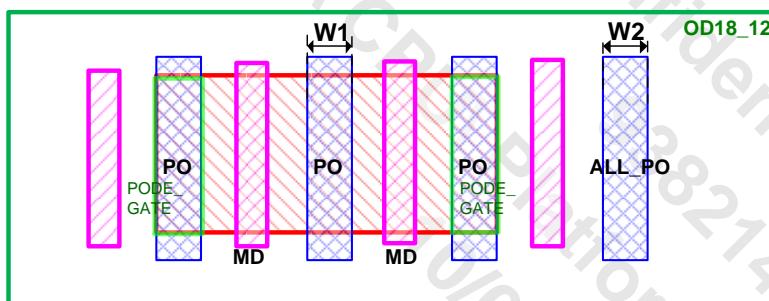
OD18_15.R.5.1

4.5.11 OD18_12 Layout Rules

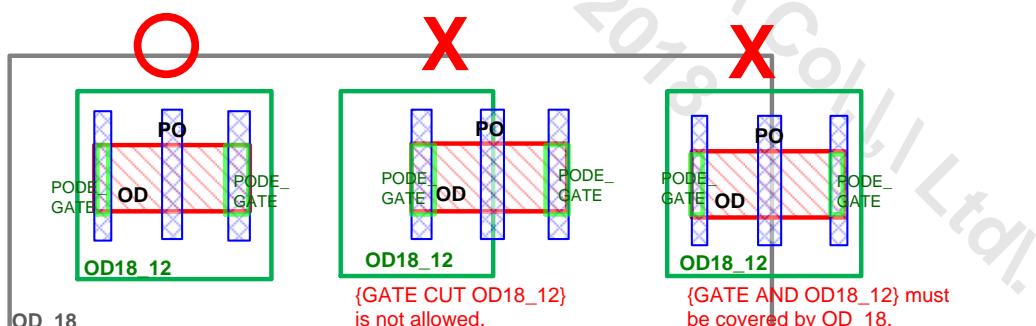
OD18_12 (CAD layer:16;1) is only used for 1.8V underdrive to 1.2V in N7+ process. This is not a mask layer.

Rule No.	Description	Label	Op.	Rule
OD18_12.W.1	Channel length of 1.8V MOS underdrive to 1.2V {GATE AND OD18_12}	W1	=	0.0720~0.2400
OD18_12.W.2	ALL_PO width of 1.8V MOS underdrive to 1.2V {ALL_PO AND OD18_12} (Except following conditions: 1. {{DC_CORE OR DC_IO} OR DC_WPO})	W2	=	0.0720~0.2400
OD18_12.R.1	{GATE AND OD18_12} must be covered by OD_18. {GATE CUT OD18_12} is not allowed			
OD18_12.R.3	OD18_12 must be orthogonal to grid			
OD18_12.R.5	{GATE AND OD18_12} can't overlap OD18_15 or VAR.			

OD18_12

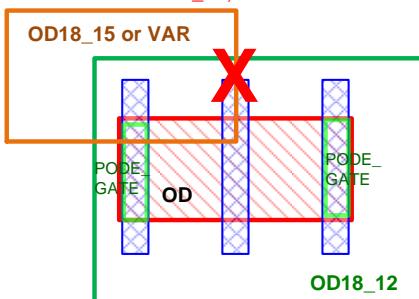


OD18_12.W.1 / OD18_12.W.2

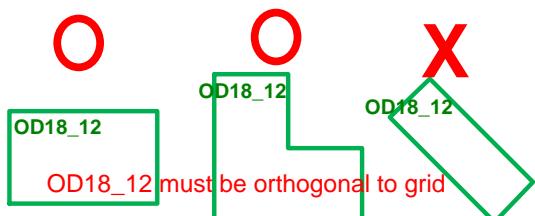


OD18_12.R.1

{GATE AND OD18_12} overlap
OD18_15, or VAR is not allowed.



OD18_12.R.3

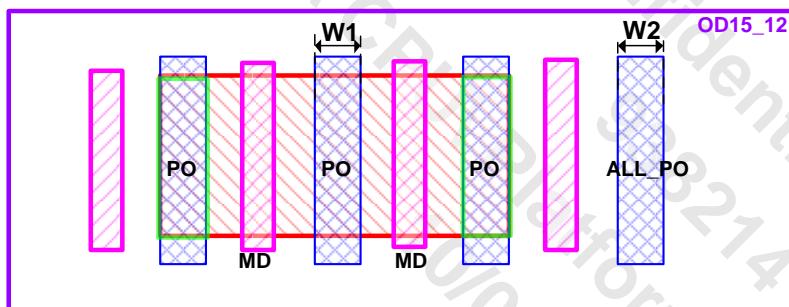


4.5.12 OD15_12 Layout Rules

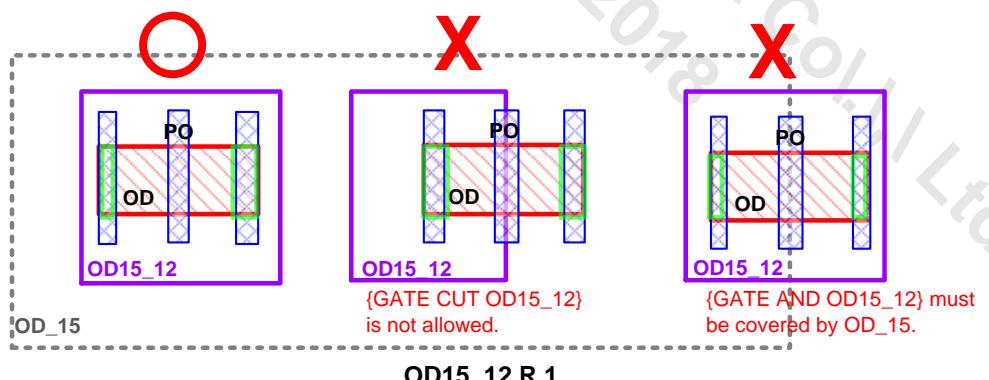
OD15_12 (CAD layer:21;4) is only used for 1.5V underdrive to 1.2V in N7+ process. This is not a mask layer.

Rule No.	Description	Label	Op.	Rule
OD15_12.W.1	Channel length of 1.5V MOS underdrive to 1.2V {GATE AND OD15_12}	W1	=	0.0720~0.2400
OD15_12.W.2	ALL_PO width of 1.5V MOS underdrive to 1.2V {ALL_PO AND OD15_12} (Except following conditions: 1. {{DC_CORE OR DC_IO} OR DC_WPO})	W2	=	0.0720~0.2400
OD15_12.R.1	{GATE AND OD15_12} must be covered by OD_15. {GATE CUT OD15_12} is not allowed			
OD15_12.R.3	OD15_12 must be orthogonal to grid			
OD15_12.R.5	{GATE AND OD15_12} can't overlap VAR.			

OD15_12

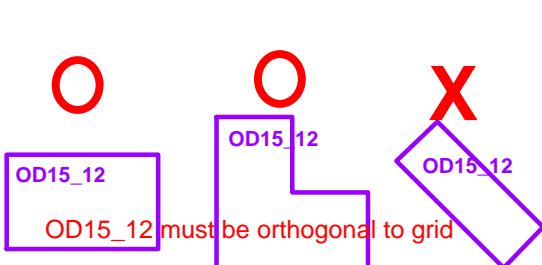


OD15_12.W.1 / OD15_12.W.2

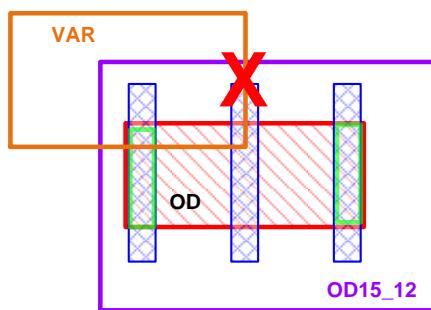


OD15_12.R.1

{GATE AND OD15_12} can't overlap VAR.



OD15_12.R.3



OD15_12.R.5

4.5.13 Standard Cell Layout Rules

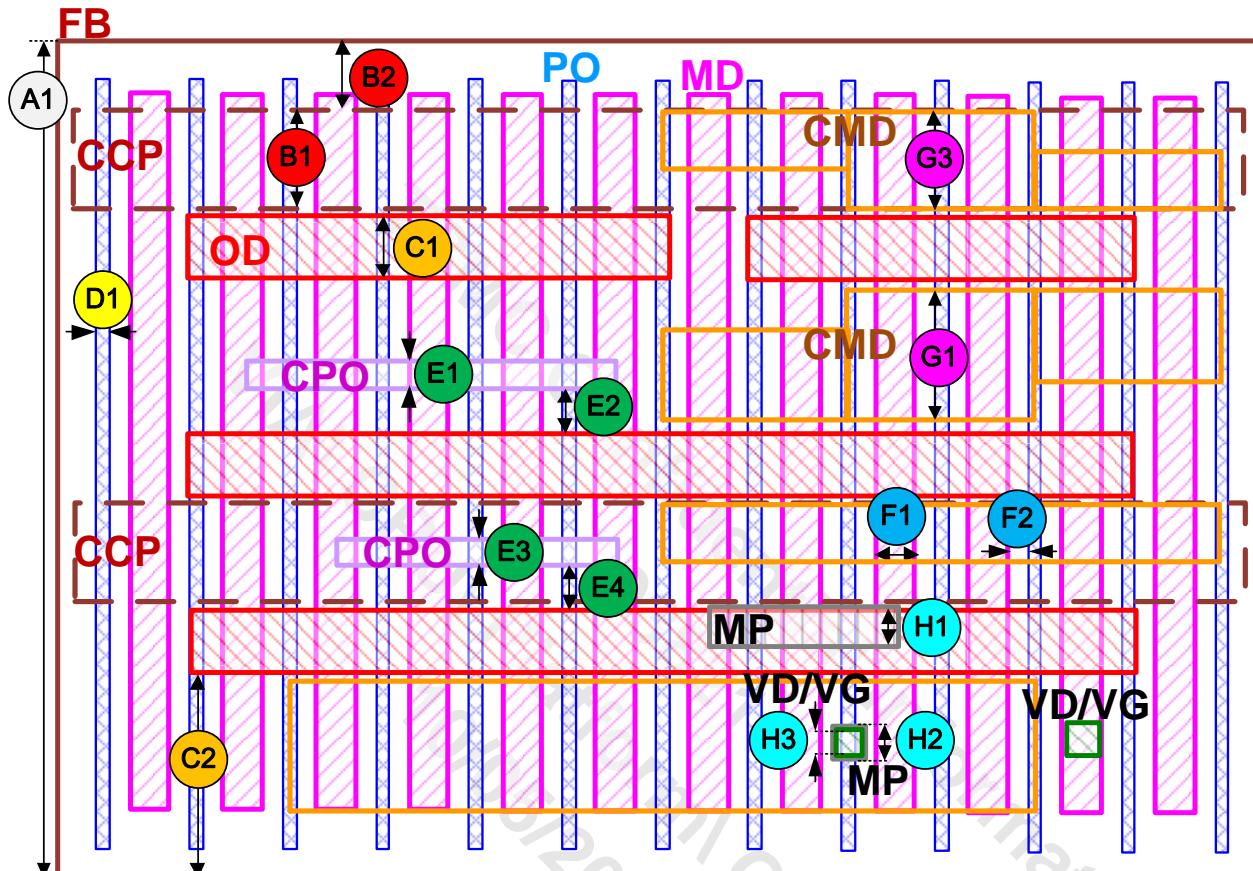
This section provides information about the following:

- 4.5.13.1 Standard Cell Quick Reference
- 4.5.13.2 Common Standard Cell (CELL) Layout Rules
- 4.5.13.3 Cell Height 240 (H240) Layout Rules ($L_g \leq 0.011 \mu m$)
- 4.5.13.4 Cell Height 300 (H300) Layout Rules ($L_g \leq 0.011 \mu m$)

TSMC Confidential Information
938214
VIAI CPU Platform\ Col. I Ltd.
10/05/2018

4.5.13.1 Standard Cell Quick Reference

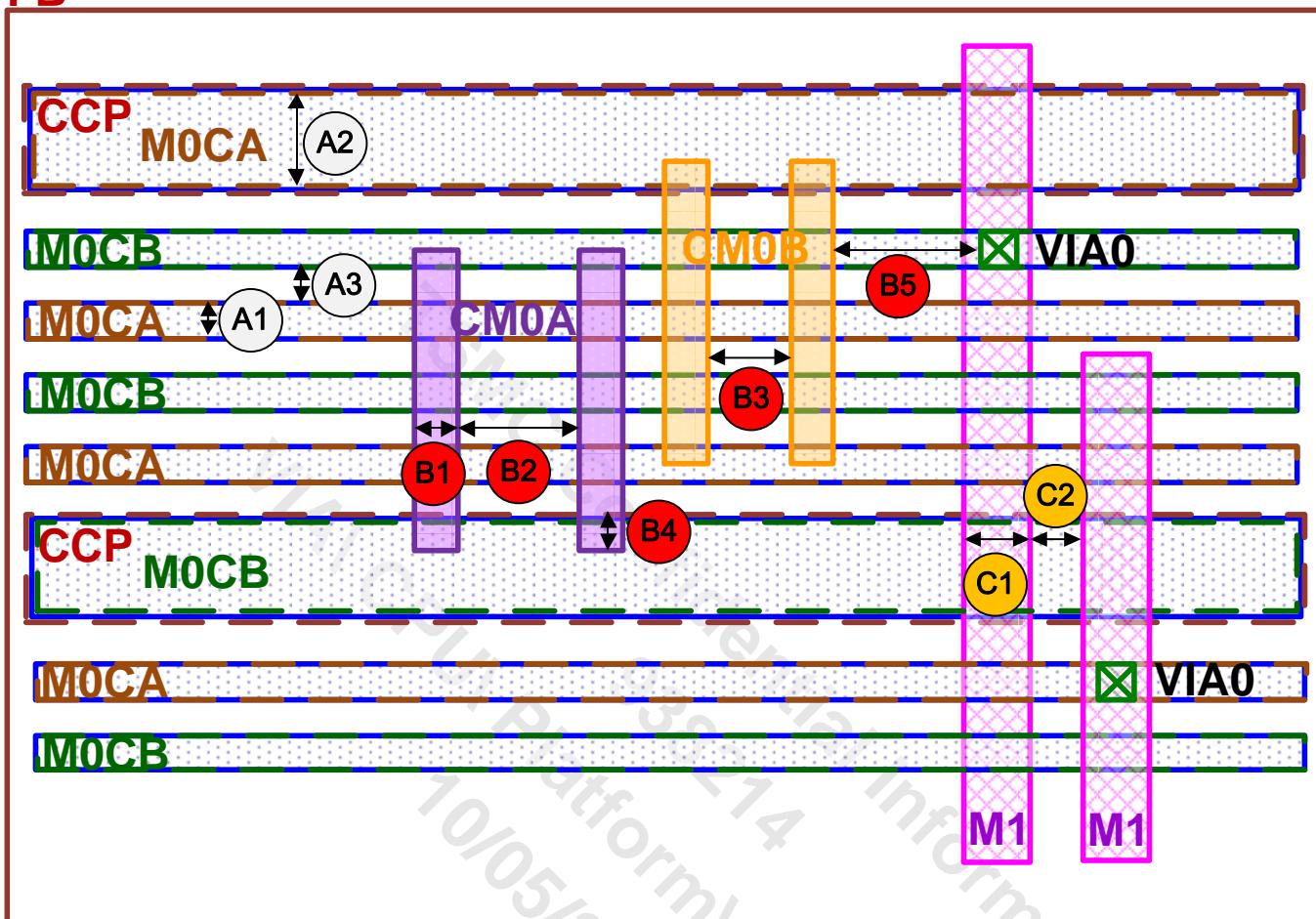
Standard Cell Quick Reference – FEOL/MEOL



Item	Description	H240 (FB_9)	H300 (FB_8)	Rule Number
A1	Width of FB	=0.4800+0.2400*n	=0.9000+0.6000*n	*.FB.W.1.1
B1	Width of CCP	=0.0600	=0.0800	*.CCP.R.1
B2	FB enclosure of CCP	=0.0900+0.2400*n	=0.1100+0.3000*n	*.FB.EN.5
C1	Width of OD	=0.0380	=0.0380, 0.0680	*.OD.W.1.1
C2	FB enclosure of OD	≥ 0.0500	≥ 0.0410	*.FB.EN.1
D1	Width of PO	=0.0080, 0.0110	=0.0080, 0.0110	*.PO.W.1.1
E1	Width of CPO [in-cell]	=0.0160	=0.0160	*.CPO.W.1
E2	PO End Cap [in-cell]	≥ 0.0230	≥ 0.0230	CPO.S.4
E3	Width of CPO [CCP]	=0.0160	=0.0300	*.CPO.W.1
E4	PO End Cap [CCP]	≥ 0.0240	≥ 0.0260	*.CPO.S.4.2
F1	Width of MD	=0.0240	=0.0240	MD.W.1
F2	Space of MD to PO	≥ 0.0110	≥ 0.0110	MD.S.6.1
F3	MD extension on OD	≥ 0.0100	≥ 0.0100	MD.EX.5.4
G1	Width of CMD [in-cell]	=0.0560, 0.0960	=0.0400, 0.0560, 0.0960	*.CMD.W.1
G2	Width of CMD [CCP]	=0.0350, 0.0600	=0.0540, 0.0780	*.CMD.W.1.1
H1	Width of rectangular MP	=0.0220	=0.0220	MP.W.1
H2	Width of square MP	=0.0200	=0.0200	MP.W.1
H3	Width of VC	=0.0160, 0.0200	=0.0160, 0.0200	VC.W.1

Standard Cell Quick Reference – BEOL

FB



Item	Description	H240 (FB_9)	H300 (FB_8)	Rule Number
A1	Width of M0 [in-cell]	=0.0200	=0.0200	*.M0.W.1.1
A2	Space of M0	=0.0200	=0.0200	*.M0.S.19
A3	Width of M0 [CCP]	=0.0600	=0.0800	*.M0.R.15.1
B1	Width of CM0A/CM0B	=0.0240	=0.0240	CM0A.W.1
B2	Space of CM0A	≥ 0.0840	≥ 0.0840	CELL.CM0A.S.1.2
B3	Space of CM0B	≥ 0.0615	≥ 0.0615	CELL.CM0B.S.1.3
B4	Overlap of CM0A/CM0B and CCP	=0.0100	=0.0100	CELL.CCP.O.1
B5	Space of CM0A/CM0B to VIA0	≥ 0.0065	≥ 0.0065	CELL.CM0A.S.5
C1	Width of VIA0	=0.0200	=0.0200	VIA0.W.1
D1	Width of M1	≥ 0.0200	≥ 0.0200	M1.W.1
D2	Space of M1	≥ 0.0180	≥ 0.0180	M1.S.1

4.5.13.2 Common Standard Cell (CELL) Layout Rules

Common and specific layout rules required in standard cells are summarized in this section. In addition to standard cells, rules might flag outside standard cells as a ground rule.

For example, M1.A.2 violation outside standard cells could also be flagged by CELL.M1.A.2. However, once M1.A.2 is followed, CELL.M1.A.2 flag is gone.

Rule No.	Description	Label	Op.	Rule
CELL.OD.R.16	ALL_OD [INSIDE {HEADER_9 OR HEADER_8}] must be fully covered by VTS_P or VTL_P			
CELL.COD_V.R.6	Horizontal edge of ALL_COD_V [INSIDE CCP_9, CCP_8,] must abut horizontal centerline of CCP_9, CCP_8			
CELL.COD_V.R.6.1	Horizontal edge of ALL_COD_V [INSIDE {FB_8 NOT CCP_8}] must abut horizontal centerline of {FB_8 NOT CCP_8}			
CELL.CPO.R.14	CPO [width = 0.030 μm] outside CCP_8 is not allowed			
CELL.MD.S.8.2	Space of short side of ALL_MD [short side NOT INTERACT CMD] to ALL_OD in vertical direction (Except BLK_WF)	S8B	\geq	0.0320
CELL.MD.EX.5.1	{ALL_MD NOT CMD} extension on ALL_OD in vertical direction (Extension < 0 μm is not allowed)	EX5A	\geq	0.0020
CELL.CMD.S.3	Space of ALL_CMD edge [INSIDE MD] to VC [width/length = 0.016 μm /0.016 μm , INTERACT MD] [PRL > 0 μm]	S3	\geq	0.0040
CELL.CMD.S.3.1	Space of ALL_CMD edge [INSIDE MD] to VC [width/length = 0.020 μm /0.020 μm , INTERACT MD] [PRL > 0 μm]	S3A	\geq	0.0020
CELL.CMD.DN.1	Maximum {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}} density in window 10 μm x 10 μm , stepping 5 μm		\leq	66%
CELL.MP.S.1.1	Space of ALL_MP to rectangular ALL_MP (Except BLK_WF)	S1A	\geq	0.0370
CELL.MP.S.1.1.1	Space of ALL_MP to rectangular ALL_MP [different net] (Except BLK_WF)	S1A1	\geq	0.0410
CELL.MP.S.5.1	Space of ALL_MP to ALL_OD (Except BLK_WF, or following conditions: 1. {Dummy_Cell NOT {{DC5_1 OR DC5_2} NOT DC7} NOT {DC8_1 OR DC8_2}}})	S5A	\geq	0.0200
CELL.MP.S.5.3	Space of ALL_MP to ALL_OD in horizontal direction [PRL > -0.020 μm] (Except BLK_WF, or following conditions: 1. {Dummy_Cell NOT {{DC5_1 OR DC5_2} NOT DC7} NOT {DC8_1 OR DC8_2}}})	S5C	\geq	0.0230
CELL.MP.S.5.10	Space of MP to CPO [INTERACT the same PO] in vertical direction	S5J	\geq	0.0100
CELL.MP.R.12	ALL_MP INTERACT {CCP_9 OR CCP_8} is not allowed			
CELL.VC.W.1	Width of VC [INSIDE CCP_9, CCP_8]	W1	=	0.0200
CELL.VC.R.19.6	VC [INSIDE CCP_9, CCP_8] must be fully covered by BVG			
CELL.M0.A.2	Area of M0_NOT_CM0 (Except BCM0H)	A2	\geq	0.00123
CELL.M0.A.2.1	Area of {M0CA NOT CM0A} [INTERACT one CM0A]	A2A	\geq	0.00168
CELL.M0.A.2.2	Area of {M0CB NOT CM0B} [INTERACT one CM0B]	A2B	\geq	0.00168
CELL.CM0A.S.1.2	Space of long side of CM0A [PRL \geq 0 μm , INSIDE {FB_9 OR FB_8}] (Except BCM0H)	S1B	\geq	0.0840
CELL.CM0A.S.4	Space of CM0A edge [INSIDE M0CA] to VC [PRL > 0 μm]	S4	\geq	0.0065
CELL.CM0A.S.5	Space of CM0A edge [INSIDE M0CA] to VIA0 [PRL > 0 μm] (Except BLK_WB)	S5	\geq	0.0065

Rule No.	Description	Label	Op.	Rule
CELL.CM0A.S.5.1	Space of CM0A edge [INSIDE M0CA] to VIA0 [INTERACT {M1 NOT M1 [width = 0.020/0.037 μm]}] [PRL > 0 μm] (Except BLK_WB)	S5A	≥	0.0095
CELL.CM0A.R.8	CM0A vertical centerline must abut vertical centerline of ALL_PO [width ≤ 0.011 μm] or space to vertical centerline of ALL_PO [width ≤ 0.011 μm] = 0.0285 μm [INSIDE FB_9, FB_8] (Except PO_P63)			
CELL.CM0A.R.8.1	CM0A vertical centerline must abut vertical centerline of ALL_PO [width ≤ 0.011 μm] or space to vertical centerline of ALL_PO [width ≤ 0.011 μm] = 0.0315 μm [INSIDE {FB_9 OR FB_8} [INTERACT PO_P63]]			
CELL.CM0B.S.1	Space (Except BLK_WB, or following conditions: 1. Both CM0B interact BCM0VB or BCM0H, 2. Two CM0B space = 0.0615 μm [both CM0B length ≥ 0.160 μm, PRL > -0.079 μm])	S1	≥	0.0840
CELL.CM0B.S.1.2	Space to long side of CM0B [length < 0.160 μm, PRL > -0.079 μm, INSIDE {{FB_9 OR FB_8} NOT {{CCP_9 OR CCP_8} SIZING -0.010 μm}}]	S1B	≥	0.0840
CELL.CM0B.S.1.3	Space of long side of CM0B [PRL ≥ 0 μm, INSIDE {FB_9 OR FB_8}] (Except BCM0H)	S1C	≥	0.0615
CELL.CM0B.S.1.4	Space to long side of CM0B [length < 0.160 μm] [PRL ≥ 0 μm, INSIDE {FB_9 OR FB_8}] (Except BCM0H)	S1D	≥	0.0840
CELL.CM0B.S.4	Space of CM0B edge [INSIDE M0CB] to VC [PRL > 0 μm] (Except BLK_WB)	S4	≥	0.0065
CELL.CM0B.S.5	Space of CM0B edge [INSIDE M0CB] to VIA0 [PRL > 0 μm] (Except BLK_WB)	S5	≥	0.0065
CELL.CM0B.S.5.1	Space of CM0B edge [INSIDE M0CB] to VIA0 [INTERACT {M1 NOT M1 [width = 0.020/0.037 μm]}] [PRL > 0 μm] (Except BLK_WB)	S5A	≥	0.0095
CELL.CM0B.R.7.3	P114_Group width in horizontal direction > 0.936 μm is not allowed Definition of P114_Space: Space region = 0.090 μm in horizontal direction formed by CM0B [length > 0.240 μm, PRL > 0.240 μm] Definition of P114_Group: {P114_Space SIZING 0.024 μm in horizontal direction}			
CELL.CM0B.R.8	CM0B vertical centerline must abut vertical centerline of ALL_PO [width ≤ 0.011 μm] or space to vertical centerline of ALL_PO [width ≤ 0.011 μm] = 0.0285 μm [INSIDE FB_9, FB_8] (Except PO_P63)			
CELL.CM0B.R.8.1	CM0B vertical centerline must abut vertical centerline of ALL_PO [width ≤ 0.011 μm] or space to vertical centerline of ALL_PO [width ≤ 0.011 μm] = 0.0315 μm [INSIDE {FB_9 OR FB_8} [INTERACT PO_P63]]			
CELL.VIA0.S.31.1.T	Space of VIA0 [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μm]	S31AT	≥	0.0370
CELL.VIA0.S.31.2.T	Space of VIA0 [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 μm in horizontal/vertical direction] in vertical direction [PRL > -0.018 μm]	S31BT	≥	0.0370

Rule No.	Description	Label	Op.	Rule
CELL.VIA0.S.31.3.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S31CT	≥	0.0650
CELL.VIA0.S.31.4.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S31DT	≥	0.0440
CELL.VIA0.S.31.5.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S31ET	≥	0.0370
CELL.VIA0.S.31.6.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except BLK_WB)	S31FT	≥	0.0440
CELL.VIA0.S.31.7.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S31GT	≥	0.0650
CELL.VIA0.S.31.8.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S31HT	≥	0.0370
CELL.VIA0.S.31.9.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S31IT	≥	0.0650
CELL.VIA0.S.31.10.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S31JT	≥	0.0440
CELL.VIA0.S.31.11.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S31KT	≥	0.0370
CELL.VIA0.S.31.12.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.025 µm]	S31LT	≥	0.0440
CELL.VIA0.S.31.13.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except BLK_WB)	S31MT	≥	0.0650
CELL.VIA0.S.31.14.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S31NT	≥	0.0370
CELL.VIA0.S.31.15.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S31OT	≥	0.0370
CELL.VIA0.S.31.16.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S31PT	≥	0.0600
CELL.VIA0.S.31.17.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction]	S31QT	≥	0.0265
CELL.VIA0.S.32.1.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32AT	≥	0.0650

Rule No.	Description	Label	Op.	Rule
CELL.VIA0.S.32.2.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32BT	≥	0.0440
CELL.VIA0.S.32.3.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S32CT	≥	0.0370
CELL.VIA0.S.32.4.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32DT	≥	0.0650
CELL.VIA0.S.32.5.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32ET	≥	0.0440
CELL.VIA0.S.32.6.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S32FT	≥	0.0370
CELL.VIA0.S.32.7.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32GT	≥	0.0650
CELL.VIA0.S.32.8.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32HT	≥	0.0650
CELL.VIA0.S.32.9.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S32IT	≥	0.0370
CELL.VIA0.S.32.10.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32JT	≥	0.0650
CELL.VIA0.S.32.11.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32KT	≥	0.0440
CELL.VIA0.S.32.12.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S32LT	≥	0.0370
CELL.VIA0.S.32.13.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32MT	≥	0.0650
CELL.VIA0.S.32.14.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32NT	≥	0.0650
CELL.VIA0.S.32.15.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S32OT	≥	0.0370
CELL.VIA0.S.32.16.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32PT	≥	0.0740
CELL.VIA0.S.32.17.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32QT	≥	0.0740

Rule No.	Description	Label	Op.	Rule
CELL.VIA0.S.32.18.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction]	S32RT	≥	0.0370
CELL.VIA0.S.33.1.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except BLK_WB)	S33AT	≥	0.0440
CELL.VIA0.S.33.2.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S33BT	≥	0.0650
CELL.VIA0.S.33.3.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S33CT	≤	0.0370
CELL.VIA0.S.33.4.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S33DT	≤	0.0650
CELL.VIA0.S.33.5.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S33ET	≤	0.0650
CELL.VIA0.S.33.6.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S33FT	≤	0.0370
CELL.VIA0.S.33.7.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S33GT	≤	0.0370
CELL.VIA0.S.33.8.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S33HT	≤	0.0650
CELL.VIA0.S.33.9.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S33IT	≥	0.0370
CELL.VIA0.S.33.10.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S33JT	≥	0.0650
CELL.VIA0.S.33.11.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S33KT	≥	0.0650
CELL.VIA0.S.33.12.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S33LT	≥	0.0370
CELL.VIA0.S.33.13.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S33MT	≥	0.0440
CELL.VIA0.S.33.14.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S33NT	≤	0.0650
CELL.VIA0.S.33.15.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S33OT	≥	0.0370

Rule No.	Description	Label	Op.	Rule
CELL.VIA0.S.33.16.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S33PT	≥	0.0560
CELL.VIA0.S.33.17.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S33QT	≥	0.0740
CELL.VIA0.S.33.18.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction]	S33RT	≥	0.0370
CELL.VIA0.S.34.1.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S34AT	≥	0.0650
CELL.VIA0.S.34.2.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S34BT	≥	0.0440
CELL.VIA0.S.34.3.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S34CT	≥	0.0370
CELL.VIA0.S.34.4.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S34DT	≥	0.0650
CELL.VIA0.S.34.5.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S34ET	≥	0.0440
CELL.VIA0.S.34.6.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S34FT	≥	0.0370
CELL.VIA0.S.34.7.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S34GT	≥	0.0650
CELL.VIA0.S.34.8.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S34HT	≥	0.0650
CELL.VIA0.S.34.9.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S34IT	≥	0.0370
CELL.VIA0.S.34.10.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S34JT	≥	0.0650
CELL.VIA0.S.34.11.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S34KT	≥	0.0440
CELL.VIA0.S.34.12.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S34LT	≥	0.0370
CELL.VIA0.S.34.13.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S34MT	≥	0.0650

Rule No.	Description	Label	Op.	Rule
CELL.VIA0.S.34.14.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S34NT	≥	0.0650
CELL.VIA0.S.34.15.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S34OT	≥	0.0370
CELL.VIA0.S.34.16.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S34PT	≥	0.0740
CELL.VIA0.S.34.17.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S34QT	≥	0.0740
CELL.VIA0.S.34.18.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction]	S34RT	≥	0.0370
CELL.VIA0.S.35.1.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.025 µm]	S35AT	≥	0.0440
CELL.VIA0.S.35.2.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S35BT	≥	0.0650
CELL.VIA0.S.35.3.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S35CT	≥	0.0370
CELL.VIA0.S.35.4.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S35DT	≥	0.0650
CELL.VIA0.S.35.5.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S35ET	≥	0.0650
CELL.VIA0.S.35.6.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S35FT	≥	0.0370
CELL.VIA0.S.35.7.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S35GT	≥	0.0440
CELL.VIA0.S.35.8.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S35HT	≥	0.0650
CELL.VIA0.S.35.9.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S35IT	≥	0.0370
CELL.VIA0.S.35.10.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S35JT	≥	0.0650
CELL.VIA0.S.35.11.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S35KT	≥	0.0650

Rule No.	Description	Label	Op.	Rule
CELL.VIA0.S.35.12.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S35LT	≥	0.0370
CELL.VIA0.S.35.13.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S35MT	≥	0.0370
CELL.VIA0.S.35.14.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S35NT	≥	0.0650
CELL.VIA0.S.35.15.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S35OT	≥	0.0370
CELL.VIA0.S.35.16.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S35PT	≥	0.0560
CELL.VIA0.S.35.17.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S35QT	≥	0.0740
CELL.VIA0.S.35.18.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction]	S35RT	≥	0.0370
CELL.VIA0.S.37.1.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S37AT	≥	0.0370
CELL.VIA0.S.37.2.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S37BT	≥	0.0600
CELL.VIA0.S.37.3.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S37CT	≥	0.0265
CELL.VIA0.S.37.4.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S37DT	≥	0.0740
CELL.VIA0.S.37.5.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S37ET	≥	0.0740
CELL.VIA0.S.37.6.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S37FT	≥	0.0370
CELL.VIA0.S.37.7.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S37GT	≥	0.0560
CELL.VIA0.S.37.8.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S37HT	≥	0.0740
CELL.VIA0.S.37.9.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S37IT	≥	0.0370

Rule No.	Description	Label	Op.	Rule
CELL.VIA0.S.37.10.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S37JT	≥	0.0740
CELL.VIA0.S.37.11.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S37KT	≥	0.0740
CELL.VIA0.S.37.12.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S37LT	≥	0.0370
CELL.VIA0.S.37.13.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S37MT	≥	0.0560
CELL.VIA0.S.37.14.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S37NT	≥	0.0740
CELL.VIA0.S.37.15.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S37OT	≥	0.0370
CELL.VIA0.S.37.16.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S37PT	≥	0.0560
CELL.VIA0.S.37.17.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S37QT	≥	0.0740
CELL.VIA0.S.37.18.T	Space of VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.060 µm in horizontal/vertical direction]	S37RT	≥	0.0370
CELL.VIA0.L.1	Length of VIA0 [width = 0.020 µm]	L1	=	0.0200, 0.0340, 0.0500, 0.0600
CELL.M1.W.1.1	Width of M1 (31;420) [INTERACT FB_9, FB_8] in MINP direction	W1A	=	0.0200, 0.0220, 0.0370, 0.0400, 0.0600
CELL.VIAxs.S.31.1.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S31AT	≥	0.0370
CELL.VIAxs.S.31.2.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S31BT	≥	0.0370
CELL.VIAxs.S.31.3.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S31CT	≥	0.0740
CELL.VIAxs.S.31.4.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S31DT	≥	0.0440
CELL.VIAxs.S.31.5.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S31ET	≥	0.0370
CELL.VIAxs.S.31.6.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S31FT	≥	0.0440

Rule No.	Description	Label	Op.	Rule
CELL.VIAxs.S.31.7.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S31GT	≥	0.0740
CELL.VIAxs.S.31.8.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S31HT	≥	0.0370
CELL.VIAxs.S.31.9.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S31IT	≥	0.0740
CELL.VIAxs.S.31.10.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S31JT	≥	0.0440
CELL.VIAxs.S.31.11.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S31KT	≥	0.0370
CELL.VIAxs.S.31.12.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S31LT	≥	0.0440
CELL.VIAxs.S.31.13.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S31MT	≥	0.0740
CELL.VIAxs.S.31.14.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S31NT	≥	0.0370
CELL.VIAxs.S.32.1.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32AT	≥	0.0740
CELL.VIAxs.S.32.2.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32BT	≥	0.0440
CELL.VIAxs.S.32.3.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S32CT	≥	0.0370
CELL.VIAxs.S.32.4.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32DT	≥	0.0740
CELL.VIAxs.S.32.5.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32ET	≥	0.0440
CELL.VIAxs.S.32.6.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S32FT	≥	0.0370
CELL.VIAxs.S.32.7.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32GT	≥	0.0740
CELL.VIAxs.S.32.8.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32HT	≥	0.0740

Rule No.	Description	Label	Op.	Rule
CELL.VIAxs.S.32.9.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S32IT	≥	0.0370
CELL.VIAxs.S.32.10.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32JT	≥	0.0740
CELL.VIAxs.S.32.11.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32KT	≥	0.0440
CELL.VIAxs.S.32.12.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S32LT	≥	0.0370
CELL.VIAxs.S.32.13.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S32MT	≥	0.0740
CELL.VIAxs.S.32.14.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S32NT	≥	0.0740
CELL.VIAxs.S.32.15.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S32OT	≥	0.0370
CELL.VIAxs.S.33.1.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S33AT	≥	0.0440
CELL.VIAxs.S.33.2.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S33BT	≥	0.0740
CELL.VIAxs.S.33.3.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S33CT	≥	0.0370
CELL.VIAxs.S.33.4.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S33DT	≥	0.0740
CELL.VIAxs.S.33.5.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S33ET	≥	0.0740
CELL.VIAxs.S.33.6.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S33FT	≥	0.0370
CELL.VIAxs.S.33.7.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S33GT	≥	0.0440
CELL.VIAxs.S.33.8.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S33HT	≥	0.0740
CELL.VIAxs.S.33.9.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S33IT	≥	0.0370

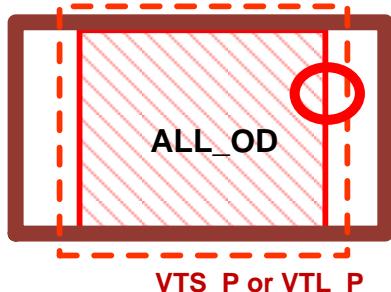
Rule No.	Description	Label	Op.	Rule
CELL.VIAxs.S.33.10.T	Space of VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μm]	S33JT	≥	0.0740
CELL.VIAxs.S.33.11.T	Space of VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] in vertical direction [PRL > -0.020 μm]	S33KT	≥	0.0740
CELL.VIAxs.S.33.12.T	Space of VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction]	S33LT	≥	0.0370
CELL.VIAxs.S.33.13.T	Space of VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 μm]	S33MT	≥	0.0440
CELL.VIAxs.S.33.14.T	Space of VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] in vertical direction [PRL > -0.018 μm]	S33NT	≥	0.0740
CELL.VIAxs.S.33.15.T	Space of VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction]	S33OT	≥	0.0370
CELL.VIAxs.S.34.1.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μm]	S34AT	≥	0.0740
CELL.VIAxs.S.34.2.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] in vertical direction [PRL > -0.020 μm]	S34BT	≥	0.0440
CELL.VIAxs.S.34.3.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction]	S34CT	≥	0.0370
CELL.VIAxs.S.34.4.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μm]	S34DT	≥	0.0740
CELL.VIAxs.S.34.5.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 μm in horizontal/vertical direction] in vertical direction [PRL > -0.020 μm]	S34ET	≥	0.0440
CELL.VIAxs.S.34.6.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 μm in horizontal/vertical direction]	S34FT	≥	0.0370
CELL.VIAxs.S.34.7.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μm]	S34GT	≥	0.0740
CELL.VIAxs.S.34.8.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction] in vertical direction [PRL > -0.020 μm]	S34HT	≥	0.0740
CELL.VIAxs.S.34.9.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 μm in horizontal/vertical direction]	S34IT	≥	0.0370
CELL.VIAxs.S.34.10.T	Space of VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μm]	S34JT	≥	0.0740

Rule No.	Description	Label	Op.	Rule
CELL.VIAxs.S.34.11.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S34KT	≥	0.0440
CELL.VIAxs.S.34.12.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction]	S34LT	≥	0.0370
CELL.VIAxs.S.34.13.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S34MT	≥	0.0740
CELL.VIAxs.S.34.14.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S34NT	≥	0.0740
CELL.VIAxs.S.34.15.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction]	S34OT	≥	0.0370
CELL.VIAxs.S.35.1.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S35AT	≥	0.0440
CELL.VIAxs.S.35.2.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S35BT	≥	0.0740
CELL.VIAxs.S.35.3.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S35CT	≥	0.0370
CELL.VIAxs.S.35.4.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S35DT	≥	0.0740
CELL.VIAxs.S.35.5.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S35ET	≥	0.0740
CELL.VIAxs.S.35.6.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction]	S35FT	≥	0.0370
CELL.VIAxs.S.35.7.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S35GT	≥	0.0440
CELL.VIAxs.S.35.8.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm]	S35HT	≥	0.0740
CELL.VIAxs.S.35.9.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction]	S35IT	≥	0.0370
CELL.VIAxs.S.35.10.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm]	S35JT	≥	0.0740
CELL.VIAxs.S.35.11.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm]	S35KT	≥	0.0740

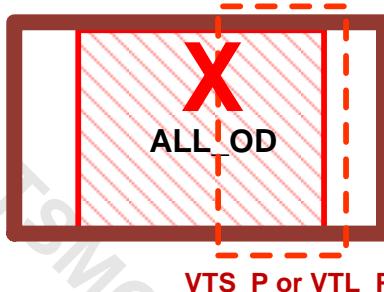
Rule No.	Description	Label	Op.	Rule
CELL.VIAxs.S.35.12.T	Space of VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 μm in horizontal/vertical direction]	S35LT	≥	0.0370
CELL.VIAxs.S.35.13.T	Space of VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 μm]	S35MT	≥	0.0440
CELL.VIAxs.S.35.14.T	Space of VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] in vertical direction [PRL > -0.018 μm]	S35NT	≥	0.0740
CELL.VIAxs.S.35.15.T	Space of VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction]	S35OT	≥	0.0370
CELL.Mx.S.4.1	Space to Mx line-end in NMINP direction [PRL > -0.020 μm] (Except BLK_WB)	S4A	≥	0.1160
CELL.Mx.A.1	Area of Mx	A1	≥	0.00368
CELL.Mx.CS.5.1	Mx end-end/end-run space [PRL > -0.060 μm] in NMINP direction (Except BLK_WB)	CS5A	≥	0.1160
CELL.CCP.EN.1	ALL_CMD enclosure by {CCP_9 OR CCP_8} in horizontal direction	EN1	≥	0.0285
CELL.CCP.O.1	{CCP_9 OR CCP_8} [INTERACT M0CA] overlap CM0B in vertical direction	O1	=	0.0100
CELL.CCP.O.1.1	{CCP_9 OR CCP_8} [INTERACT M0CB] overlap CM0A in vertical direction	O1A	=	0.0100
CELL.CCP.R.1	Any vertex of {CCP_9 OR CCP_8} inside ALL_MD is not allowed			
CELL.CCP.R.2	Vertical edge of CCP_9, CCP_8 must abut {FB_9 OR BV_FB [width = 0.120/0.240 μm]}, {FB_8 OR BV_FB [width = 0.150/0.300 μm]}, respectively			

CELL-OD/COD/CPO/MD/CMD

HEADER_9, HEADER_8



HEADER_9, HEADER_8

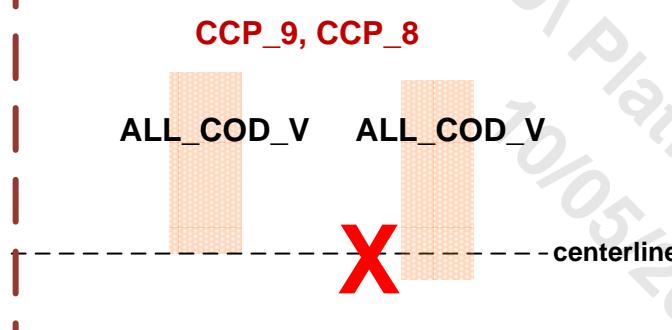


HEADER_9, HEADER_8

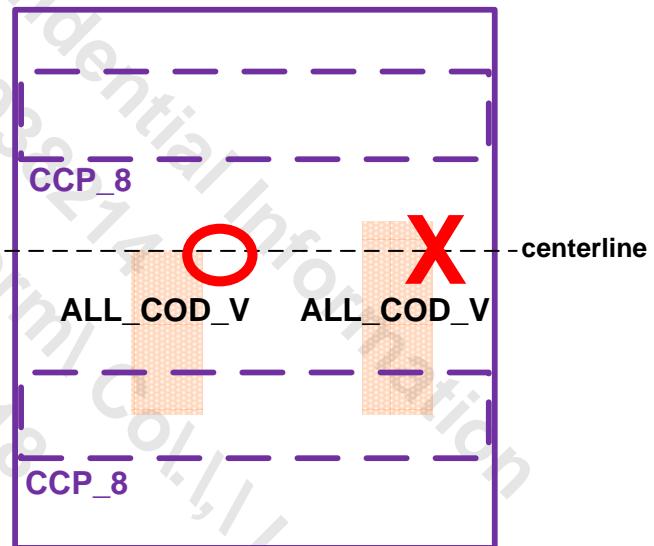


ALL_OD [INSIDE {HEADER_9 OR HEADER_8}] must be fully covered by VTS_P or VTL_P

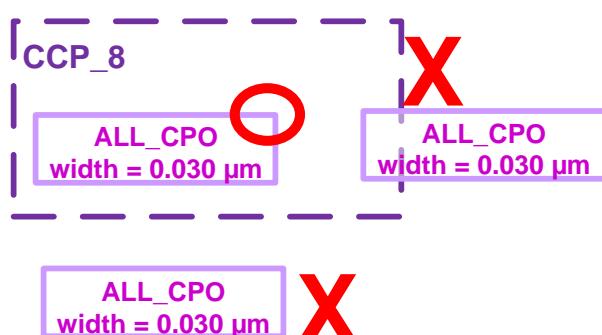
CELL.OD.R.16



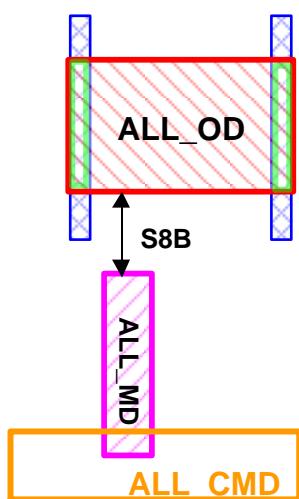
CELL.COD_V.R.6



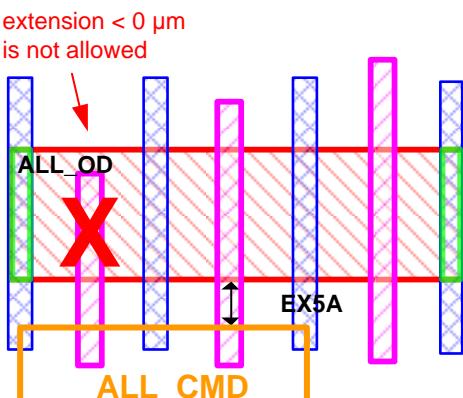
CELL.COD_V.R.6.1



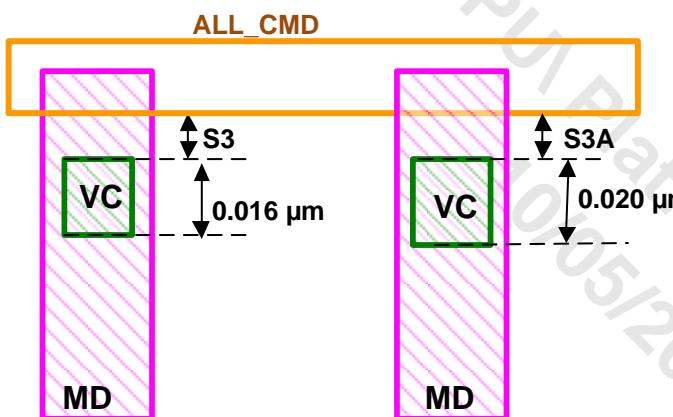
CELL.CPO.R.14



CELL.MD.S.8.2

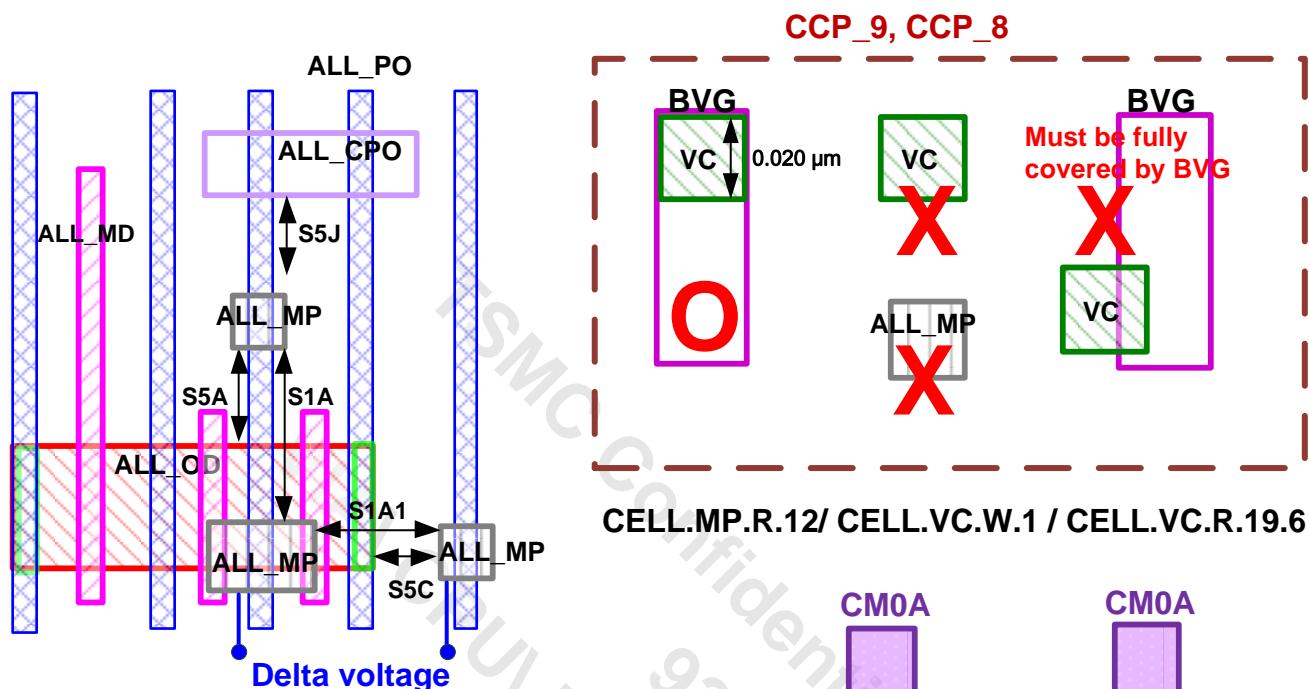


CELL.MD.EX.5.1

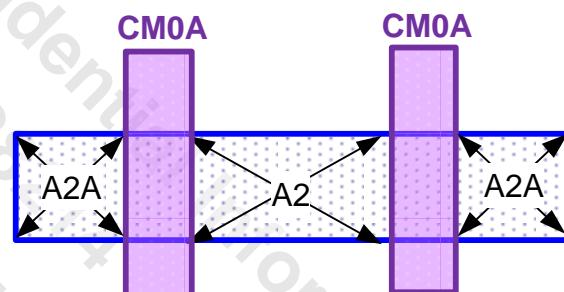


CELL.CMD.S.3 / CELL.CMD.S.3.1

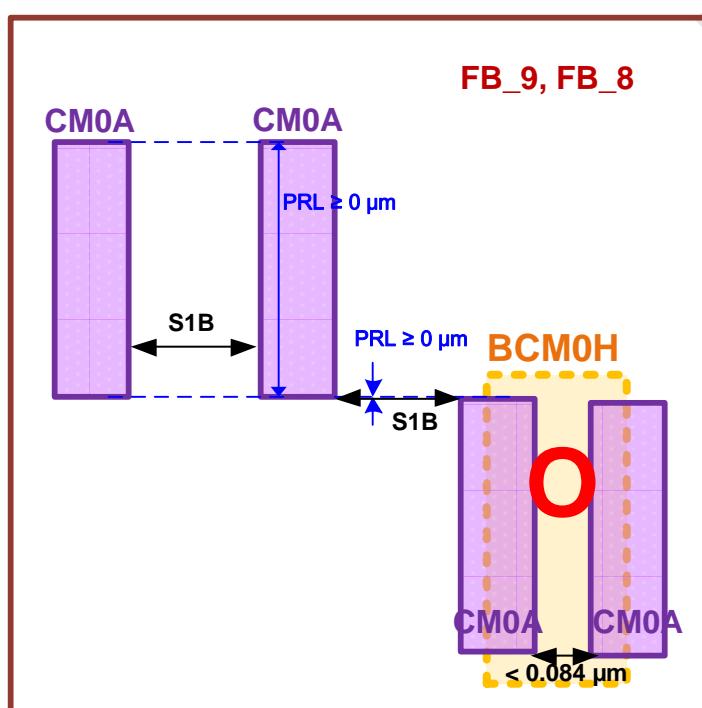
CELL-MP/VC/M0/CM0A/CM0B/VIA0



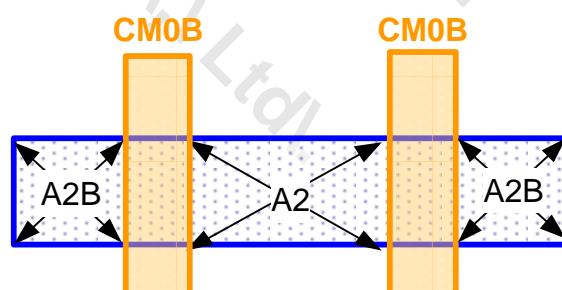
CELL.MP.S.1.1 / CELL.MP.S.1.1.1 /
CELL.MP.S.5.1 / CELL.MP.S.5.3 /
CELL.MP.S.5.10



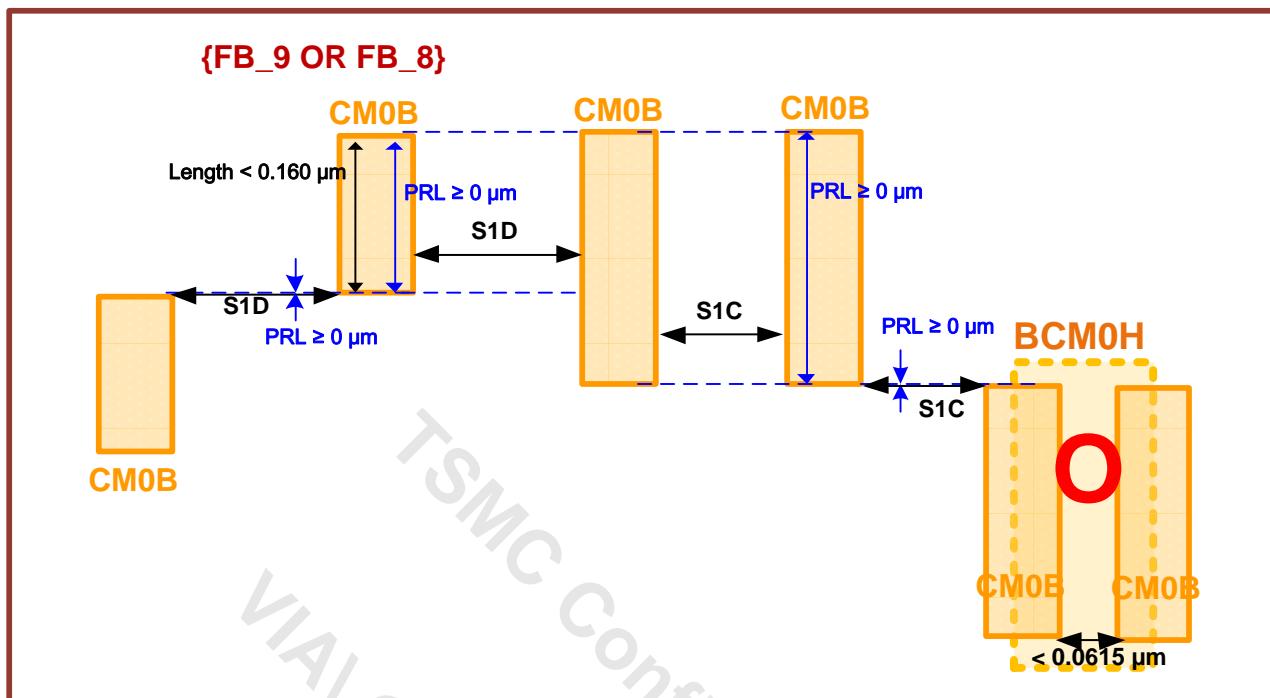
CELL.M0.A.2 / CELL.M0.A.2.1



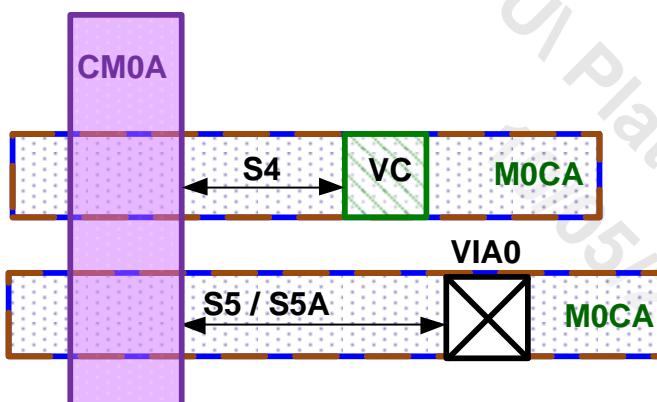
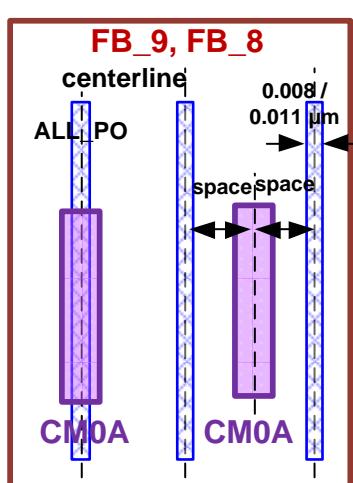
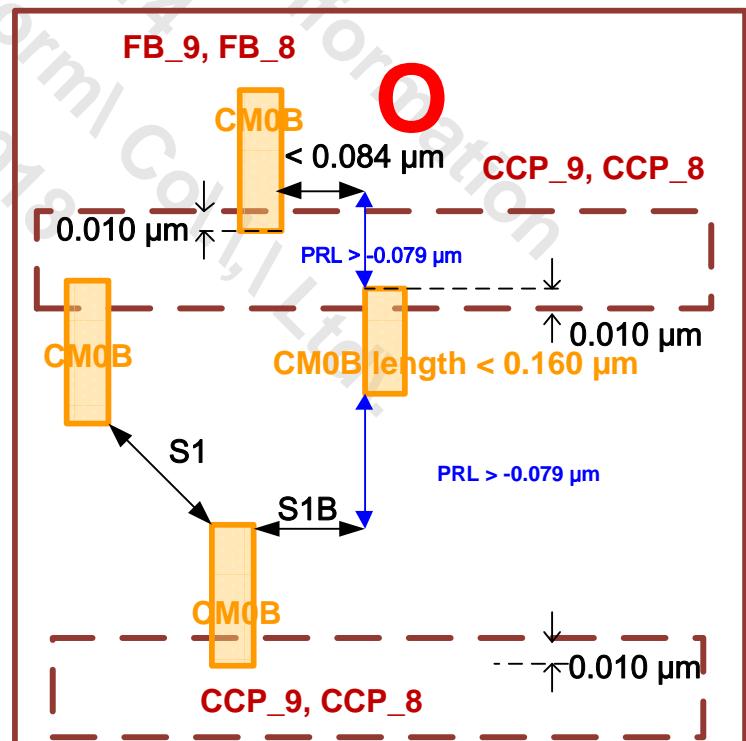
CELL.CM0A.S.1.2



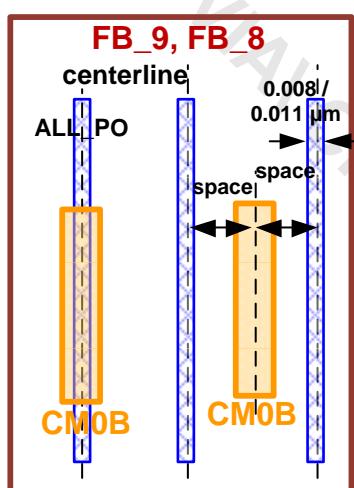
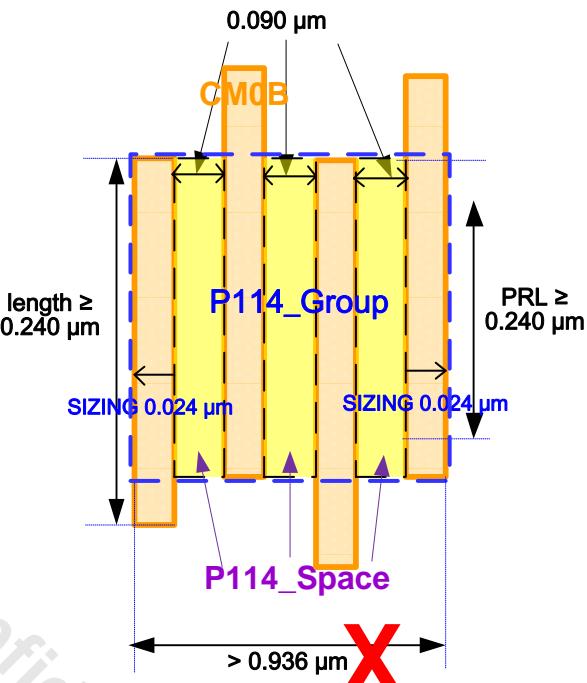
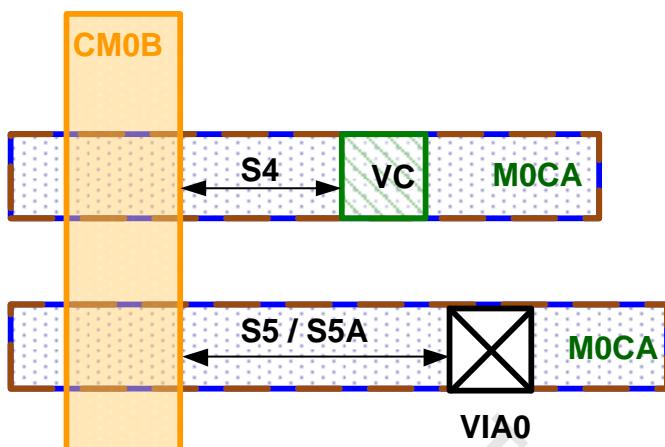
CELL.M0.A.2.2



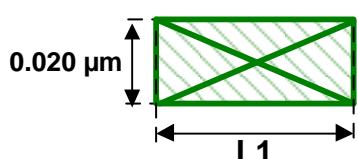
CELL.CM0B.S.1.3 / CELL.CM0B.S.1.4

CELL.CM0A.S.4 /
CELL.CM0A.S.5 / CELL.CM0A.S.5.1CELL.CM0A.R.8 /
CELL.CM0A.R.8.1

CELL.CM0B.S.1 / CELL.CM0B.S.1.2

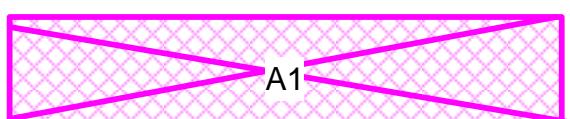
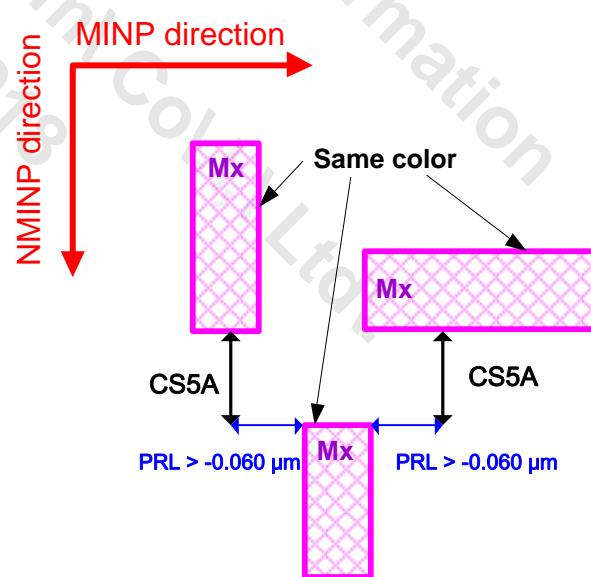
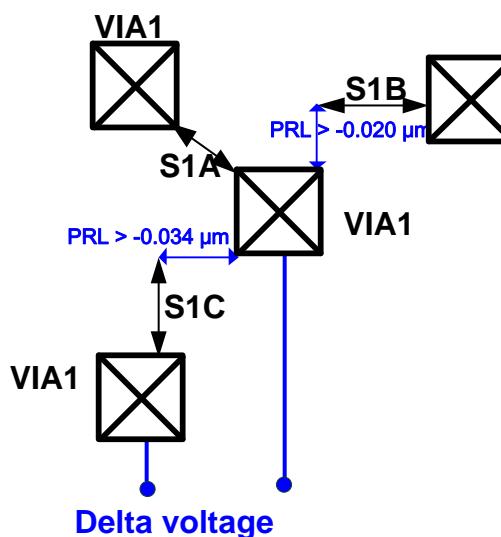
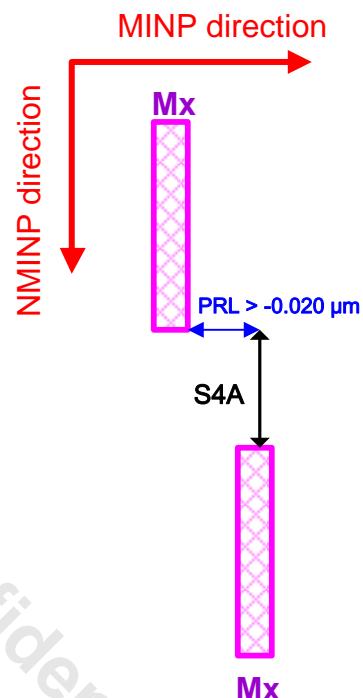
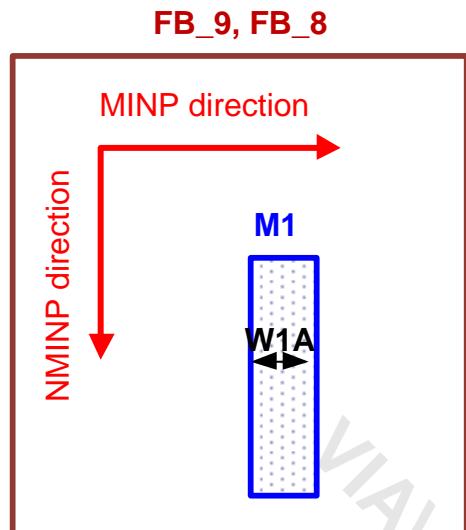


CELL.CM0B.R.7.3

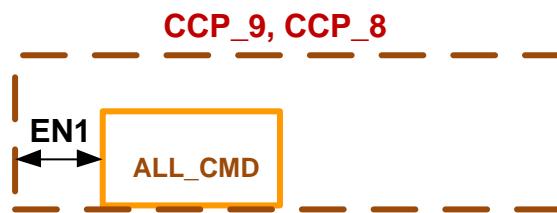


CELL.VIA0.L.1

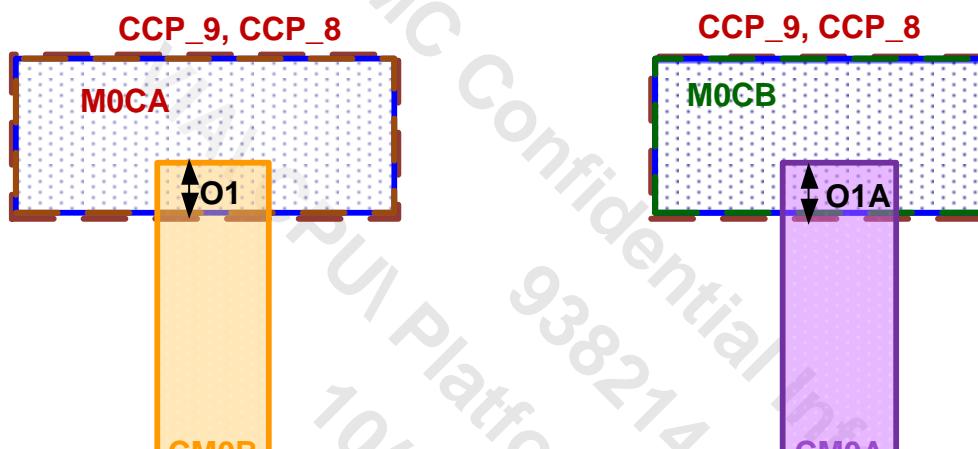
CELL-M1/VIAx/Mx



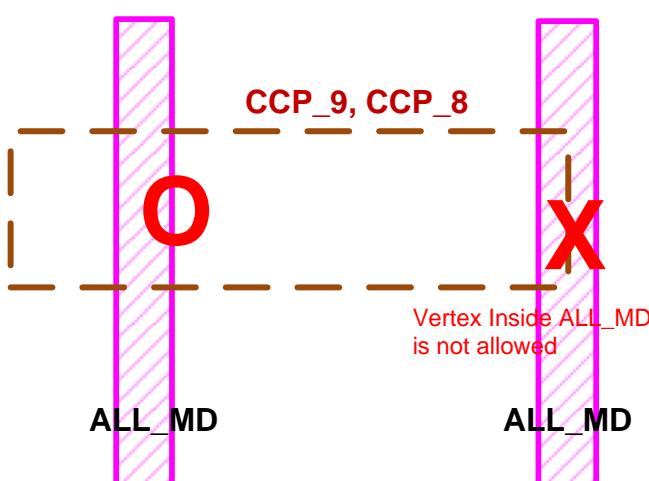
CELL - CCP



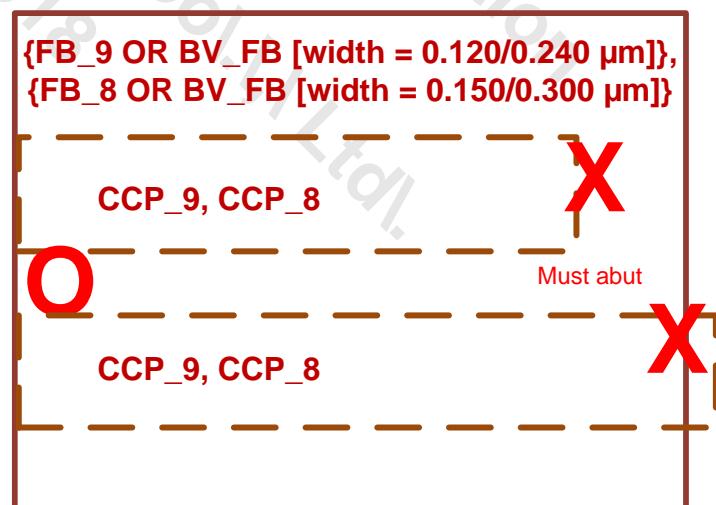
CELL.CCP.EN.1



CELL.CCP.O.1 / CELL.CCP.O.1.1



CELL.CCP.R.1



CELL.CCP.R.2

4.5.13.3 Cell Height 240 (H240) Layout Rules

FinFET_Boundary_9 (CAD layer: 250;28, or FB_9) is used for cell with cell height = 0.240 μm , $Lg \leq 0.011 \mu\text{m}$. CCP_9 (CAD layer: 98;1) is used to define Confined Compact Pattern inside FB_9.

HEADER_9 (CAD layer: 6;129) is used to define HEADER cell inside FB_9

Rule No.	Description	Label	Op.	Rule
H240.FB.W.1	Width of {FB_9 OR BV_FBF [width = 0.240 μm] in horizontal direction	W1	\geq	0.6610
H240.FB.W.1.1	Width of FB_9 in vertical direction	W1A	=	0.4800+0.2400*n
H240.FB.W.1.3	Vertical edge length of {FB_9 OR BV_FBF [width = 0.240 μm] between two consecutive 270-270 degree corners	W1C	=	0.4800+0.2400*n
H240.FB.W.1.4	Vertical edge length of {FB_9 OR BV_FBF [width = 0.240 μm] between two consecutive 90-270 degree corners	W1D	=	0.4800+0.2400*n
H240.FB.W.1.5	Concave corner to concave corner width of FB_9 in vertical direction	W1E	=	0.2400+0.2400*n
H240.FB.W.1.6®	Recommended width of FB_9 in vertical direction	W1F	=	1.2000+0.2400*n
H240.FB.EN.1	FB_9 enclosure of ALL_OD	EN1	\geq	0.0500
H240.FB.EN.1.1	Maximum enclosure of ALL_OD by FB_9	EN1A	\leq	0.2100
H240.FB.EN.2	FB_9 enclosure of ALL_OD in horizontal direction	EN2	\geq	0.0700
H240.FB.EN.5	FB_9 enclosure of CCP_9 in vertical direction	EN5	=	0.0900+0.2400*n
H240.FB.EN.6	FB_9 enclosure of TPO, VT, NP, PP in vertical direction	EN6	=	0.1200*n
H240.FB.EN.7	prBoundary enclosure of FB_9 in vertical direction in cell level	EN7	=	0.1200+0.1200*n
H240.FB.R.10	ALL_OD need to be placed in pre-defined 2-fin-grid position inside FB_9 (Except HEADER_9) Pre-defined 2-fin-grid configuration: 1. Each fin in 2-fin group has fin width = 0.008 μm with 0.022 μm apart 2. 2-fin group is 0.050 μm from top or bottom FB_9 boundary 3. 2-fin groups are separated by 0.064 μm with CCP_9 (N+OD to N+OD, or P+OD to P+OD) 4. 2-fin groups are separated by 0.100 μm without CCP_9 (N+OD to P+OD)			
H240.FB.R.11	Horizontal edge of {FB_9 SIZING -0.050 μm in vertical direction} must abut at least one ALL_OD			
H240.OD.W.1.1	Width of ALL_OD [INSIDE FB_9] in vertical direction (Except HEADER_9)	W1A	=	0.0380
H240.OD.W.1.5	Width of rectangular ALL_OD [INSIDE FB_9] in vertical direction (Except HEADER_9)	W1E	=	0.0380
H240.OD.S.1.10	Maximum space of ALL_OD in horizontal direction [INSIDE FB_9] (Except HEADER_9)	S1J	\leq	0.2770
H240.OD.S.1.11	PODE_GATE_1CPP space to ALL_OD in horizontal direction Definition of H240_OD_1CPP_SPACE: Space region of OD [space to another OD = 0.100 μm in vertical direction, 0 μm < PRL \leq 0.011 μm , INSIDE {FB_9 NOT CCP_9}] Definition of PODE_GATE_1CPP: H240_OD_1CPP_SPACE SIZING 0.019 μm in vertical direction	S1K	\leq	0.1630

Rule No.	Description	Label	Op.	Rule
H240.OD.S.1.12	Either one long side of PODE_GATE_1CPP space to ALL_OD in horizontal direction H240_OD_1CPP, PODE_GATE_1CPP definition follow H240.OD.S.1.11	S1L	\leq	0.0490
H240.OD.S.4	Space of STRAP [INSIDE FB_9] to ALL_OD in horizontal direction	S4	\geq	0.1000
H240.OD.S.4.1	Space of NWSTRAP to PWSTRAP [INSIDE FB_9]	S4A	\geq	0.1830
H240.OD.S.29	Horizontal edge of H240_OD [edge length > 0.278 μm] space to SR_DOD [width = 0.038 μm] in vertical direction (Except following conditions: 1. violation length \leq 0.278 μm and interact H240_OD concave corner) Definition of H240_OD: { {OD [INSIDE FB_9] SIZING up/down 0.139 μm in horizontal direction} SIZING up/down 0.050 μm in vertical direction }	S29	$=$	0.0640
H240.OD.A.1	Area of ALL_OD [INSIDE FB_9]	A1	\geq	0.00463
H240.OD.R.8	STRAP [INSIDE FB_9] must be a rectangle orthogonal to grid, and vertical width = 0.038 μm			
H240.COD_V.S.1.2	Space of ALL_COD_V in vertical direction [INSIDE FB_9]	S1B	\geq	0.1110
H240.COD_V.W.1	Width of ALL_COD_V [INSIDE FB_9]	W1	\geq	0.0180
H240.COD_V.S.4	Space of ALL_COD_V to ALL_OD in vertical direction [INSIDE {FB_9 NOT CCP_9}] (Except following conditions: 1. ALL_COD_V edge outside abut FB_9)	S4	$=$	0.0410, 0.0590
H240.COD_V.O.1	ALL_COD_V overlap of ALL_COD_H in vertical direction [INSIDE FB_9]	O1	\geq	0.0120
H240.COD_V.A.1	Area of ALL_COD_V [INSIDE FB_9]	A1	\geq	0.00510
H240.COD_V.A.2	Enclosed area of ALL_COD_V [Enclosure area INTERACT FB_9]	A2	\geq	0.01490
H240.PO.W.1.1	Width of ALL_PO [INSIDE FB_9]	W1A	$=$	0.0080, 0.0110
H240.PO.S.25.5	Empty space of ALL_PO [INSIDE FB_9] in horizontal direction DRC flags {{FB_9 NOT ALL_PO} SIZING down/up 0.0245 μm in horizontal direction}	S25	\leq	0.0490
H240.CPO.W.1	Width of ALL_CPO [INTERACT FB_9] in vertical direction	W1	$=$	0.0160, 0.1000
H240.CPO.S.4.2	Space of ALL_CPO [INSIDE CCP_9] to ALL_OD [INTERACT ALL_PO] in vertical direction (Overlap is not allowed)	S4B	\geq	0.0240
H240.CPO.O.3	CPO [width = 0.016 μm , INSIDE {FB_9 NOT CCP_9}] overlap NW in vertical direction		$=$	0, 0.0080, 0.0160
H240.CPO.R.12	CPO [INSIDE CCP_9] must be at the centerline of CCP_9 in vertical direction			
H240.CPO.R.15	ALL_CPO overlap {{OD [INTERACT MOS] SIZING 0.024 μm in vertical direction} SIZING 0.057 μm in horizontal direction} [INSIDE FB_9] is not allowed.			
H240.CPO.R.16.1	CPO [width = 0.016 μm , INSIDE {{FB_9 NOT CCP_9} AND NW}] must abut NW horizontal edge			
H240.TPO.W.1	Width [INSIDE FB_9] (Except following conditions: 1. Point touch of corners, 2. One track overlap = 0.057/0.114 μm in horizontal direction)	W1	\geq	0.1710
H240.TPO.S.1	Space [INSIDE FB_9] (Except following conditions: 1. Point touch of corners, 2. One track space = 0.057/0.114 μm in horizontal direction)	S1	\geq	0.1710
H240.TPO.S.2.1	Space to ALL_OD [INSIDE FB_9] in vertical direction	S2A	\geq	0.0320

Rule No.	Description	Label	Op.	Rule
H240.TPO.EN.1.1	Enclosure of ALL_OD [INSIDE FB_9] in vertical direction	EN1A	\geq	0.0320
H240.TPO.A.1	Area [INSIDE FB_9]	A1	\geq	0.04104
H240.TPO.A.2	Enclosed area (include surrounding by point-touch polygons) [INSIDE FB_9]	A2	\geq	0.04104
H240.VT.W.2	Width of VT in horizontal direction [INSIDE FB_9] (Except following conditions: 1. Point touch of corners, 2. One track overlap = 0.057/0.100/0.114 μm in horizontal direction) DRC flags width between vertical edges [PRL \geq 0 μm]	W2	\geq	0.1710
H240.VT.W.2.2	Width of {{VTL_N OR VTUL_N} OR VTS_P}, {VTL_P OR VTS_N} in horizontal direction [INSIDE FB_9] (Except following conditions: 1. Point touch of corners, 2. One track overlap = 0.057/0.100/0.114 μm in horizontal direction) DRC flags width between vertical edges [PRL \geq 0 μm]	W2B	\geq	0.1710
H240.VT.S.2	Space of VT in horizontal direction [PRL \geq 0 μm , INSIDE FB_9] (Except following conditions: 1. Point touch of corners, 2. One track space = 0.057/0.100/0.114 μm in horizontal direction)	S2	\geq	0.1710
H240.VT.S.2.2	Space of {{VTL_N OR VTUL_N} OR VTS_P} in horizontal direction [PRL \geq 0 μm , INSIDE FB_9] (Except following conditions: 1. Point touch of corners, 2. One track space = 0.057/0.100/0.114 μm in horizontal direction)	S2B	\geq	0.1710
H240.VT.S.2.4	Space of {VTL_P OR VTS_N} in horizontal direction [PRL \geq 0 μm , INSIDE FB_9] (Except following conditions: 1. Point touch of corners, 2. One track space = 0.057/0.100/0.114 μm in horizontal direction)	S2D	\geq	0.1710
H240.VT.S.4.1	Space of VT to ALL_OD [INSIDE FB_9] in vertical direction	S4A	\geq	0.0320
H240.VT.EX.1	{PO NOT CPO} extension on VT in vertical direction [INSIDE FB_9] (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	EX1	=	0, \geq 0.0430
H240.VT.EX.4.1	Extension on ALL_OD [INSIDE FB_9] in vertical direction	EX4A	\geq	0.0320
H240.VT.O.1	VT overlap of {ALL_PO NOT CPO} in vertical direction [INSIDE FB_9] (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	O1	=	0.0300, \geq 0.0430
H240.VT.A.1	Area of VT [INSIDE FB_9]	A1	\geq	0.02052
H240.VT.A.2	Enclosed area of VT (include surrounding by point-touch polygons) [INSIDE FB_9]	A2	\geq	0.02052
H240.VT.A.2.2	Enclosed area of {{VTL_N OR VTUL_N} OR VTS_P} [INSIDE FB_9] (include surrounding by point-touch polygons)	A2B	\geq	0.02052
H240.VT.A.2.4	Enclosed area of {VTS_N OR VTL_P} [INSIDE FB_9] (include surrounding by point-touch polygons)	A2D	\geq	0.02052
H240.VT.A.3	Area of {{ALL_PO NOT CPO} AND VT} [INTERACT FB_9] (Except Dummy_Cell)	A3	=	0.00024, \geq 0.00034
H240.VT.R.12	VTUL_P horizontal edge interact VTS_N, VTL_N is not allowed [INSIDE FB_9]			
H240.PP.W.1	Width [INSIDE FB_9]	W1	\geq	0.1200

Rule No.	Description	Label	Op.	Rule
H240.PP.W.1.1	Width [space < 0.192 μm, INSIDE FB_9] (DRC flags opposite side)	W1A	=	0.1200, ≥ 0.1920
H240.PP.S.1	Space [INSIDE FB_9]	S1	≥	0.1200
H240.PP.S.1.2	Space [width < 0.192 μm, INSIDE FB_9] (DRC flags opposite side)	S1B	=	0.1200, ≥ 0.1920
H240.PP.S.3	Space to ALL_OD [INSIDE FB_9]	S3	≥	0.0320
H240.PP.EN.1	Enclosure of ALL_OD [INSIDE FB_9]	EN1	≥	0.0320
H240.PP.EN.1.1	Enclosure of ALL_OD in vertical direction [INSIDE {FB_9 NOT {CCP_9 SIZING 0.002 μm in vertical direction}}, PRL > -0.062 μm]	EN1A	≥	0.0500
H240.PP.R.1	PP must fully cover {Core PMOS TrGATE SIZING 0.032 μm} (R1) [INSIDE FB_9]			
H240.NP.W.1	Width [INSIDE FB_9]	W1	≥	0.1200
H240.NP.W.1.1	Width [space < 0.192 μm, INSIDE FB_9] (DRC flags opposite side)	W1A	=	0.1200, ≥ 0.1920
H240.NP.S.1	Space [INSIDE FB_9]	S1	≥	0.1200
H240.NP.S.1.2	Space [width < 0.192 μm, INSIDE FB_9] (DRC flags opposite side)	S1B	=	0.1200, ≥ 0.1920
H240.NP.S.3	Space to ALL_OD [INSIDE FB_9]	S3	≥	0.0320
H240.NP.EN.1	Enclosure of ALL_OD [INSIDE FB_9]	EN1	≥	0.0320
H240.NP.EN.1.1	Enclosure of ALL_OD in vertical direction [INSIDE {FB_9 NOT {CCP_9 SIZING 0.002 μm in vertical direction}}, PRL > -0.062 μm]	EN1A	≥	0.0500
H240.NP.R.1	NP must fully cover {Core NMOS TrGATE SIZING 0.032 μm} (R1) [INSIDE FB_9]			
H240.MD.S.1.1	Space of short side of ALL_MD [width = 0.024 μm] to ALL_MD_Checked short side [INTERACT CCP_9, PRL > -0.030 μm] Definition of ALL_MD_Checked: 1. ALL_MD [width = 0.024 μm] length < 0.130 μm, or 2. ALL_CMD extension on ALL_MD [width = 0.024 μm] in vertical direction ≥ 0.030 μm	S1A	≥	0.1070
H240.MD.EX.6	{ALL_MD NOT CMD} extension on ALL_OD edge [INTERACT {CCP_9 SIZING 0.002 μm in vertical direction}] in vertical direction [INSIDE {CCP_9 SIZING 0.002 μm in vertical direction}] (Extension < 0 μm is not allowed)	EX6	=	0.0020, 0.0270
H240.MD.EX.6.1	{ALL_MD NOT CMD} extension on ALL_OD in vertical direction [INSIDE {FB_9 NOT {CCP_9 SIZING 0.002 μm in vertical direction}}] (Extension < 0 μm is not allowed)	EX6A	≥	0.0020
H240.MD.L.1.1	Length of ALL_MD [width = 0.024 μm, INSIDE FB_9] in vertical direction (Except Dummy_Cell)	L1A	≥	0.1080
H240.MD.R.1	MD [width = 0.024 μm, INSIDE FB_9] short side must interact CMD			
H240.CMD.W.1	Width of CMD [INSIDE {FB_9 NOT CCP_9}] in vertical direction	W1	=	0.0560, 0.0960
H240.CMD.W.1.1	Width of CMD [INSIDE CCP_9] in vertical direction	W1A	=	0.0350, 0.0600
H240.CMD.W.2	Concave corner to concave corner width of ALL_CMD [INSIDE {FB_9 NOT CCP_9}] in vertical direction [PRL > -0.114 μm] DRC flags space between 2 horizontal ALL_CMD edge [INSIDE {FB_9 NOT CCP_9}] in vertical direction < 0.016 μm [PRL > -0.114 μm]	W2	=	0.0160
H240.CMD.W.2.1	Concave corner to concave corner width of ALL_CMD [INSIDE CCP_9] in vertical direction [PRL > -0.114 μm] DRC flags space between 2 horizontal ALL_CMD edge [INSIDE CCP_9] in vertical direction < 0.010 μm [PRL > -0.114 μm]	W2A	=	0.0100

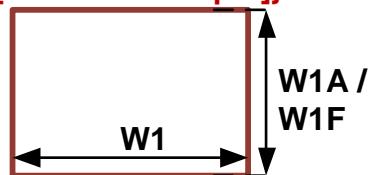
Rule No.	Description	Label	Op.	Rule
H240.CMD.S.1	Space of CMD in vertical direction [PRL > -0.057 μm, INSIDE FB_9]	S1	≥	0.0420
H240.CMD.S.1.1	Space of CMD in horizontal direction [PRL > -0.060 μm, INSIDE CCP_9]	S1A	=	0.0570, ≥ 0.1140
H240.CMD.S.1.2	Space of CMD to CCP_9 in vertical direction [INSIDE FB_9] (Cut is not allowed)	S1B	=	0.0420, 0.0820
H240.CMD.S.7	Space of CMD [Derived from BCMD, INSIDE {FB_9 NOT CCP_9}] in horizontal direction [PRL > -0.060 μm] (Except following conditions: 1. CMD horizontal direction space = 0.057 μm with PRL = 0.016 μm)	S7	≥	0.1080
H240.CMD.EN.1	ALL_CMD enclosure by CCP_9 in vertical direction	EN1	=	0, 0.0250
H240.CMD.EX.2	ALL_CMD extension on ALL_MD [width = 0.024 μm] in vertical direction [INSIDE FB_9]	EX2	≥	0.0200
H240.CMD.L.1	Length of CMD [INSIDE {FB_9 NOT CCP_9}] in horizontal direction	L1	≥	0.1140
H240.CMD.L.1.1	Length of CMD [INSIDE CCP_9] in horizontal direction	L1A	=	0.0570, ≥ 0.1140
H240.CMD.L.2	Horizontal edge length of ALL_CMD [INSIDE FB_9] between two consecutive 270-270 degree corners (U-shape), or two consecutive 90-90 degree corners (T-shape), or two consecutive 90-270 degree corners (L-shape)	L2	=	0.0570, ≥ 0.1140
H240.CMD.R.6.3	SR_DCMD overlap FB_9 is not allowed			
H240.MP.R.7	MP [width = 0.022 μm, INSIDE FB_9] either one vertical edge must be at the centerline of MD [width = 0.024 μm] in horizontal direction			
H240.MP.R.9	{ALL_MP [width = 0.022 μm, INSIDE FB_9] SIZING 0.001 μm} must abut CCP_9			
H240.VC.EN.1	Square VC [width = 0.016 μm, INTERACT MD [width = 0.024 μm]] enclosure by MD [width = 0.024 μm] for two opposite sides with the other two sides = 0.004 μm [INSIDE {FB_9 NOT CCP_9}]	EN1	≥	0.0190
H240.VC.EN.1.1	Square VC [width = 0.020 μm, INTERACT MD [width = 0.024 μm]] enclosure by MD [width = 0.024 μm] for two opposite sides with the other two sides = 0.002 μm [INSIDE {FB_9 NOT CCP_9}]	EN1A	≥	0.0170
H240.VC.EN.1.3	Square VC [width = 0.020 μm, INTERACT MD [width = 0.024 μm]] enclosure by MD [width = 0.024 μm] for two opposite sides with the other two sides = 0.002 μm [INSIDE CCP_9]	EN1C	≥	0.0070
H240.M0.W.1.1	Width in MINP direction [INSIDE {FB_9 NOT CCP_9}]	W1A	=	0.0200
H240.M0.S.2.3	Space of M0 [width = 0.060 μm] to M0 [width = 0.020 μm] in MINP direction [PRL > -0.040 μm, INSIDE {{FB_9 OR BV_FB [width = 0.120/0.240 μm]} SIZING 0.040 μm in horizontal direction}]	SM	≥	0.0200
H240.M0.S.3	Space of M0 [INTERACT CCP_9] in NMINP direction [PRL > 0 μm]	S3	≥	0.1360
H240.M0.S.19	Empty space of M0 [INSIDE {FB_9 OR BV_FB [width = 0.120/0.240 μm]}] DRC flags {{{{FB_9 OR BV_FB [width = 0.120/0.240 μm]}} SIZING -0.010 μm in vertical direction} NOT {M0 OR CCP_9}} SIZING down/up 0.010 μm}	S19	≤	0.0200
H240.M0.EN.2.7	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.060 μm] for two opposite sides with the other two sides ≥ 0.003 μm [INSIDE CCP_9]	EN2G	≥	0.0600
H240.M0.R.15.1	CCP_9 must be drawn identically to {M0CA [INTERACT {FB_9 OR BV_FB [width = 0.120/0.240 μm]}] SIZING up/down 0.068 μm in horizontal direction} or M0CB [INTERACT {FB_9 OR BV_FB [width = 0.120/0.240 μm]}]			

Rule No.	Description	Label	Op.	Rule
H240.M0.R.20	{M0 AND {FB_9 NOT {{FB_9 SIZING -0.090 μm in vertical direction} SIZING -0.080 μm in horizontal direction}}} interact VC, VIA0 is not allowed			
H240.M0.CS.1.1	Space to M0 [width = 0.020 μm] in MINP direction [same color, PRL > -0.124 μm, INSIDE {{FB_9 OR BV_FB [width = 0.120/0.240 μm]} SIZING 0.124 μm in horizontal direction}] (Except following conditions: 1. {DM0_DO1 OR DM0_DO2} space to M0 [width = 0.020 μm] ≥ 0.120 μm, PRL > -0.124 μm)	SM	=	0.0600, 0.0620, 0.0640, 0.0660, 0.1000, ≥ 0.1400
H240.M0.CS.1.2.1	Space of M0 [width = 0.060 μm] to M0 [width = 0.020 μm] in MINP direction [same color, PRL > -0.060 μm, INSIDE {{FB_9 OR BV_FB [width = 0.120/0.240 μm]} SIZING 0.060 μm in horizontal direction}]	SM	=	0.0600, ≥ 0.1000
H240.CM0A.W.3	Width of CM0A_Group in horizontal direction Definition of CM0A_Checked: {CM0A [INTERACT CCP_9, length < 0.160 μm, space = 0.090 μm in horizontal direction, PRL > 0 μm]} Definition of CM0A_Group: {{{{short side of CM0A_Checked} INTERACT CCP_9} expanding edge 0.070 μm in vertical direction} OR CM0A_Checked} SIZING up/down 0.017 μm in horizontal direction} AND CCP_9}	W3	≤	0.3090
H240.CM0A.S.1.1	Space of long side of CM0A [PRL > -0.079 μm, INSIDE {FB_9 NOT {CCP_9 SIZING -0.010 μm}}] (Except BCM0H)	S1A	≥	0.0840
H240.CM0A.S.2	Space of short side of CM0A [PRL > -0.044 μm, INSIDE FB_9] (Except following conditions: 1. short side space of CM0A [INTERACT BCM0VA] = 0.040 μm [PRL > -0.044 μm] inside CCP_9)	S2	≥	0.1200
H240.CM0A.R.7	CM0A overlap CCP_9 [INTERACT M0CA] is not allowed			
H240.CM0B.W.3	Width of CM0B_Group in horizontal direction Definition of CM0B_Checked: {CM0B [INTERACT CCP_9, length < 0.160 μm, space = 0.090 μm in horizontal direction, PRL > 0 μm]} Definition of CM0B_Group: {{{{short side of CM0B_Checked} INTERACT CCP_9} expanding edge 0.070 μm in vertical direction} OR CM0B_Checked} SIZING up/down 0.017 μm in horizontal direction} AND CCP_9}	W3	≤	0.3090

Rule No.	Description	Label	Op.	Rule
H240.CM0B.W.4	<p>Width of CM0B_Checked_Group in horizontal direction</p> <p>Definition of CM0B_Checked_Group: $\{\{\text{short side of CM0B_Checked [INTERACT CCP_9] SIZING }0.070 \mu\text{m in vertical direction}\} \text{ SIZING up/down } 0.017 \mu\text{m in horizontal direction}\} \text{ AND CCP_9\}}$</p> <p>Definition of CM0B_Checked: CM0B interact P855_Group_W</p> <p>Definition of P855_Space_W: Space region = $0.0615 \mu\text{m}$ in horizontal direction formed by $\{\text{CM0B NOT CM0B_BCM0H}\} [\text{length } \geq 0.160 \mu\text{m, PRL } \geq 0.160 \mu\text{m}]$</p> <p>Definition of P855_Group_W: Length of $\{P855_Space_W \text{ SIZING } 0.024 \mu\text{m in horizontal direction}\}$ in horizontal direction $\geq 0.195 \mu\text{m}$</p> <p>Definition of CM0B_BCM0H Both vertical edge of $\{\text{CM0B [INTERACT BCM0H] SIZING up/down } 0.017 \mu\text{m in horizontal direction}\}$ space to CM0B = $0.0615 \mu\text{m}$ in horizontal direction with PRL $\geq 0.160 \mu\text{m}$</p>	W4	\leq	0.1950
H240.CM0B.S.1.1	Space of long side of CM0B [PRL > -0.079 μm , INSIDE {FB_9 NOT {CCP_9 SIZING -0.010 $\mu\text{m}\}}}](Except BCM0H)$	S1A	=	0.0615, 0.0840, 0.0900, 0.0960, 0.1110, ≥ 0.1160
H240.CM0B.S.2	Space of short side of CM0B [PRL > -0.056 μm , INSIDE FB_9] (Except following conditions: 1. short side space of CM0B [INTERACT BCM0VB] = $0.040 \mu\text{m}$ [PRL > -0.056 μm] inside CCP_9)	S2	\geq	0.1200
H240.VIA0.EN.21.9	Short side enclosure of rectangular VIA0 by M0_NOT_CM0 [width = $0.060 \mu\text{m}$] with the other two long side enclosure $\geq 0.020 \mu\text{m}$ [INSIDE CCP_9]	EN21I	\geq	0.0600
H240.VIA0.EN.21.10	Short side enclosure of rectangular VIA0 by M0_NOT_CM0 [width = $0.060 \mu\text{m}$] with the other two long side enclosure $\geq 0.060 \mu\text{m}$ [INSIDE CCP_9]	EN21J	\geq	0.0050

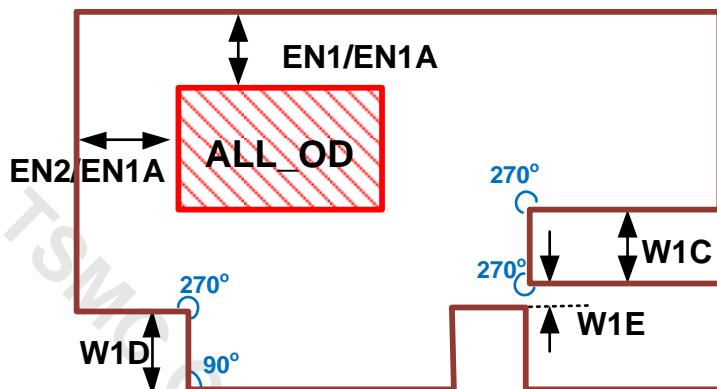
H240-FB

{FB_9 OR BV_FBF
[width = 0.240 μm]}

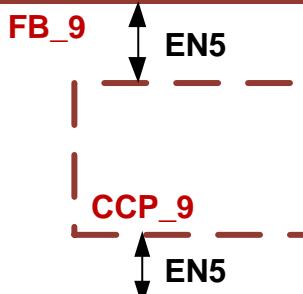


H240.FB.W.1 /
H240.FB.W.1.1 /
H240.FB.W.1.6®

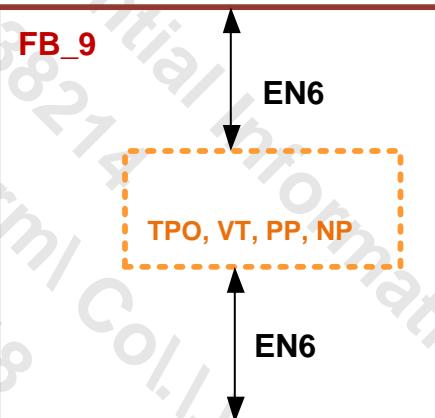
{FB_9 OR BV_FBF [width = 0.240 μm]}



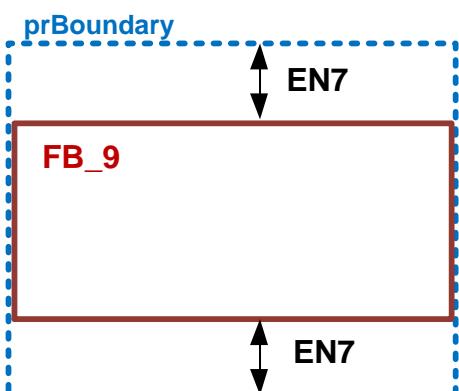
H240.FB.W.1.3 / H240.FB.W.1.4 /
H240.FB.W.1.5 / H240.FB.EN.1 /
H240.FB.EN.1.1 / H240.FB.EN.2



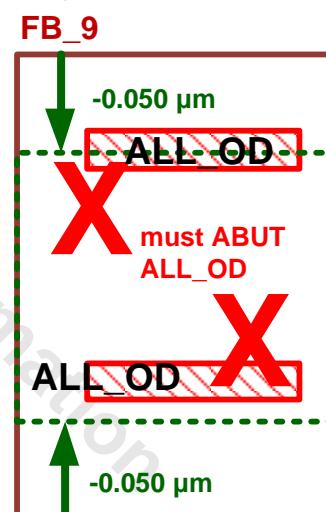
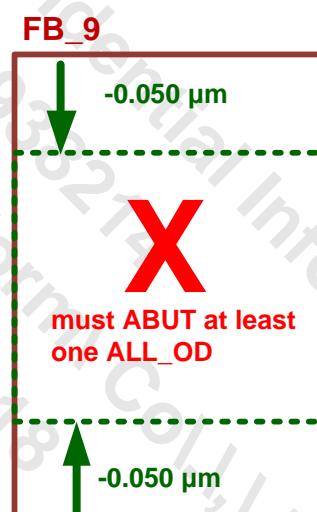
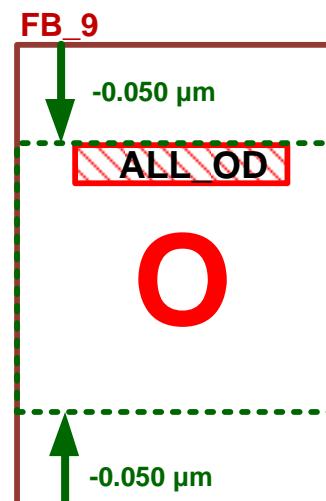
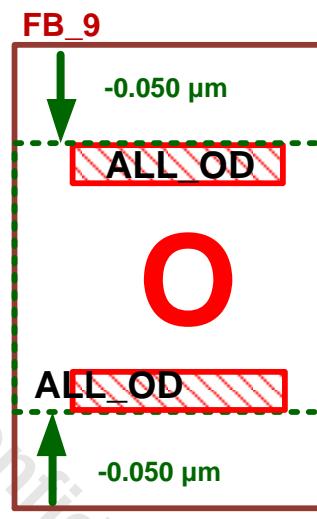
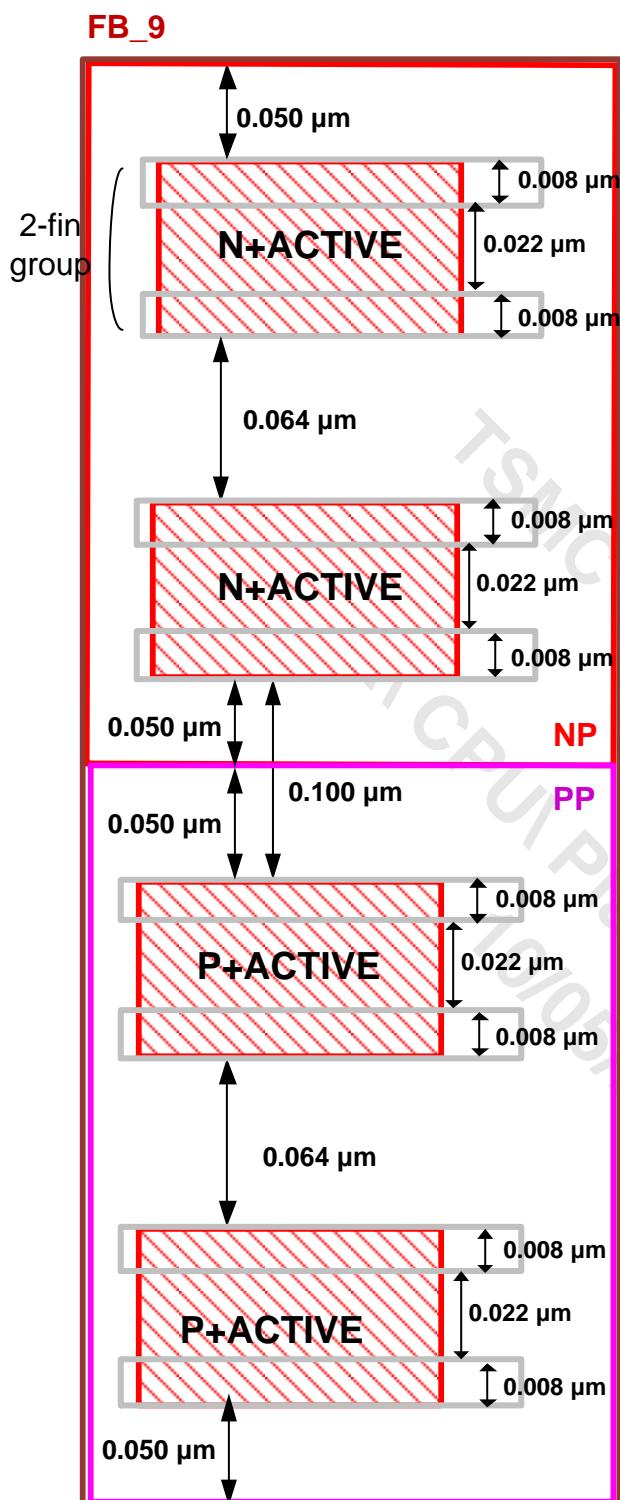
H240.FB.EN.5



H240.FB.EN.6



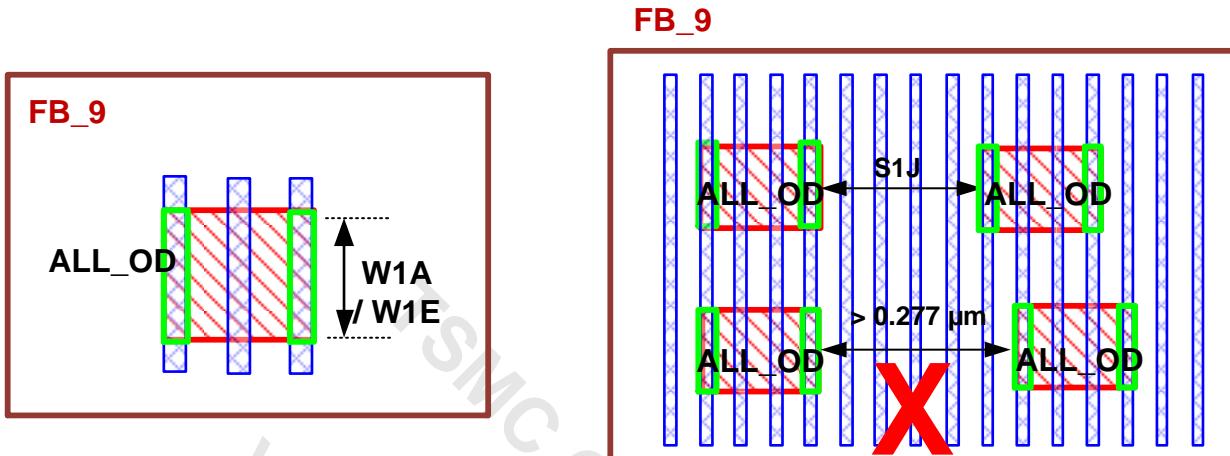
H240.FB.EN.7



H240.FB.R.11

H240.FB.R.10

H240-OD



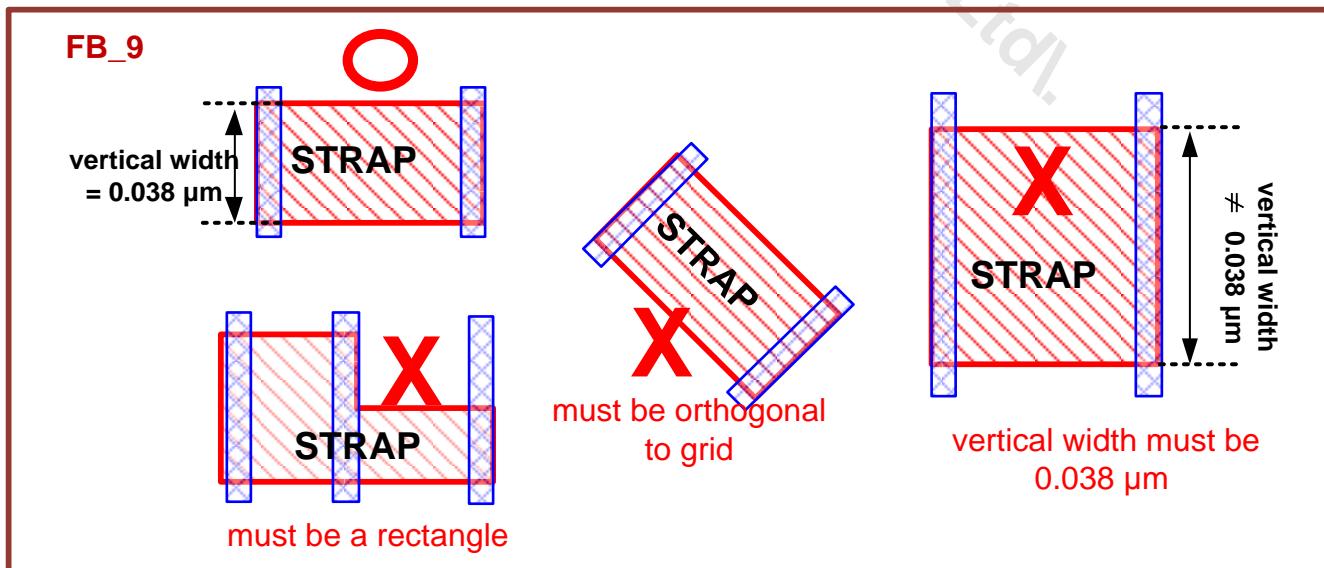
H240.OD.W.1.1 / H240.OD.W.1.5

H240.OD.S.1.10

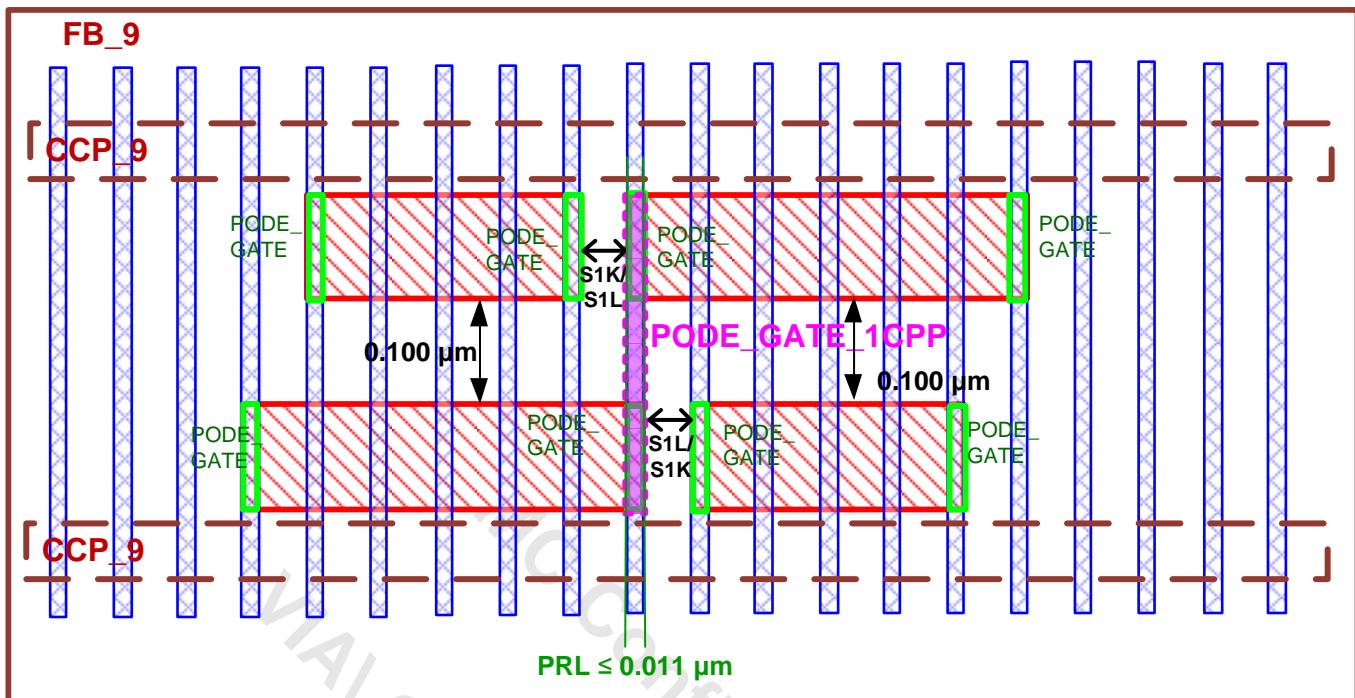


H240.OD.S.4 / H240.OD.S.4.1

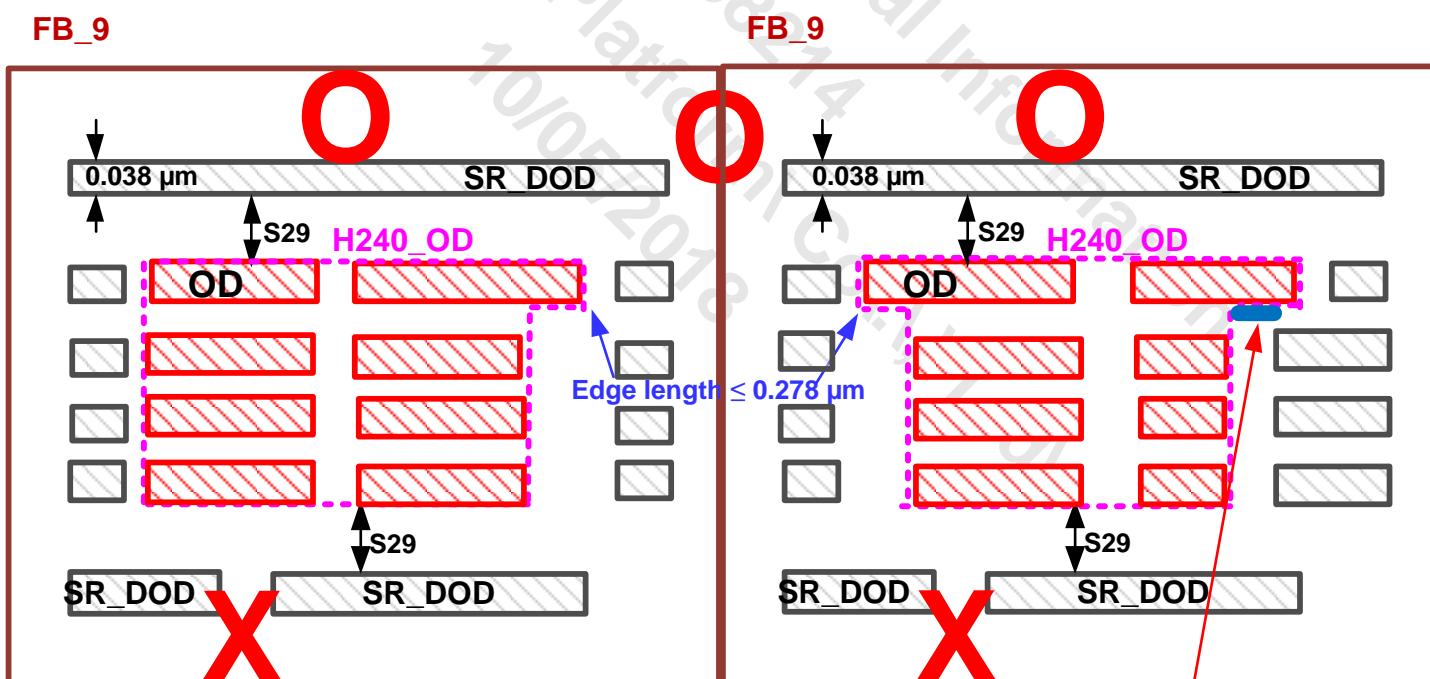
H240.OD.A.1



H240.OD.R.8



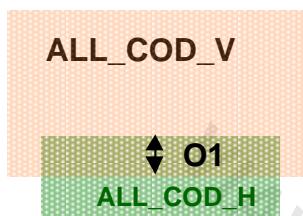
H240.OD.S.1.11/H240.OD.S.1.12



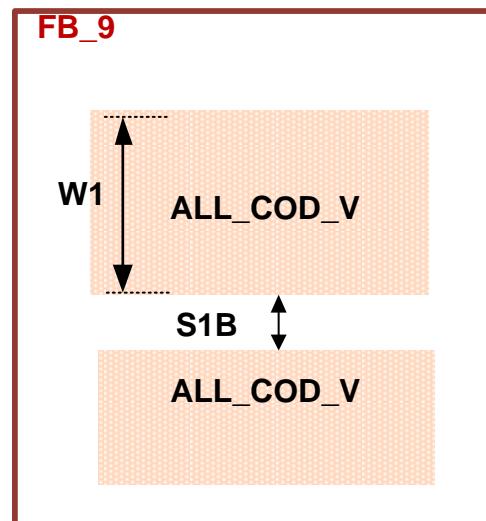
H240.OD.S.29

H240-COD

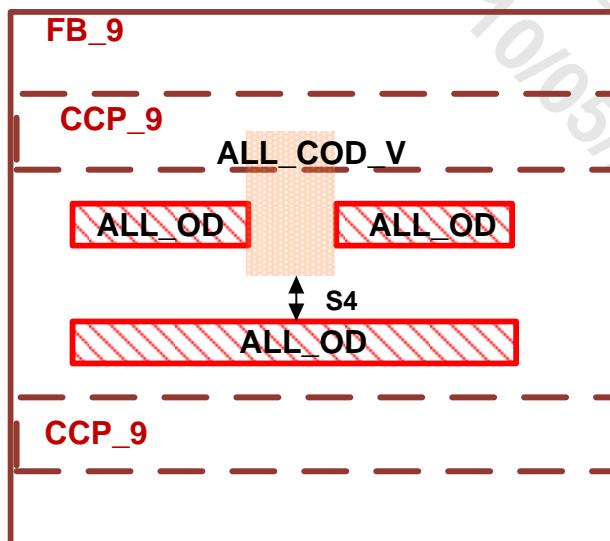
FB_9



H240.COD_V.O.1

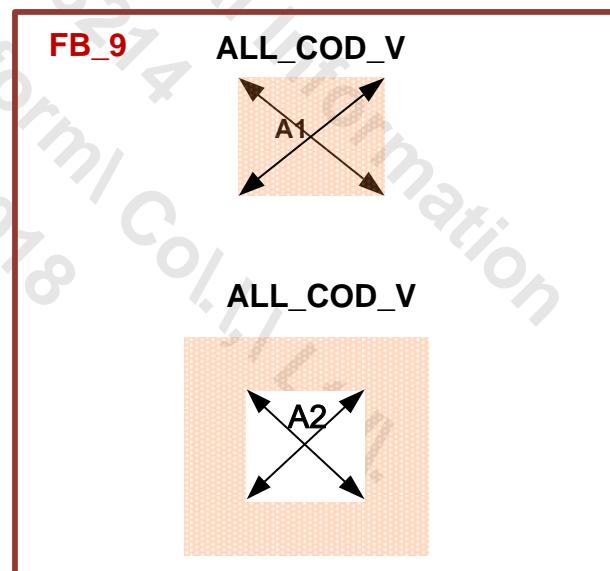
H240.COD_V.W.1
H240.COD_V.S.1.2

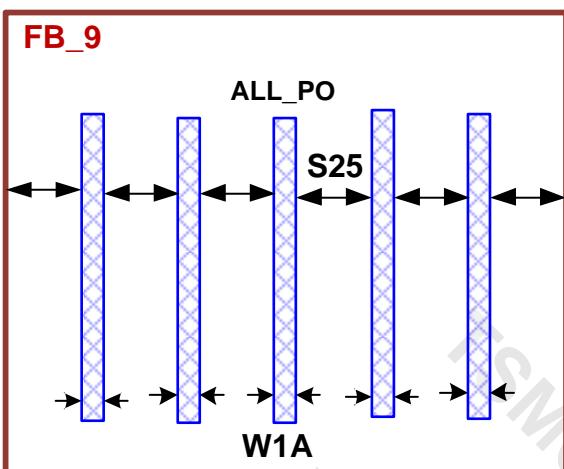
FB_9



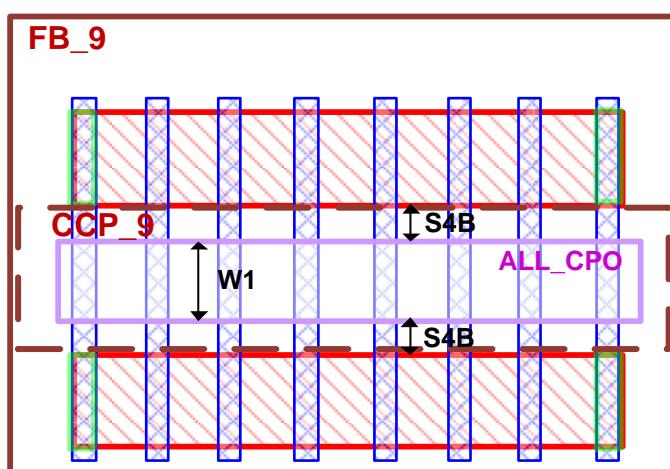
H240.COD_V.S.4

FB_9

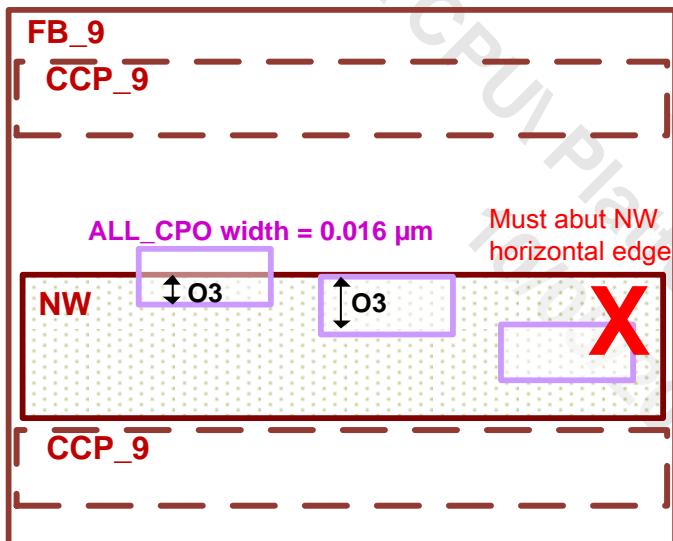
H240.COD_V.A.1 /
H240.COD_V.A.2

H240-PO/CPO/TPO

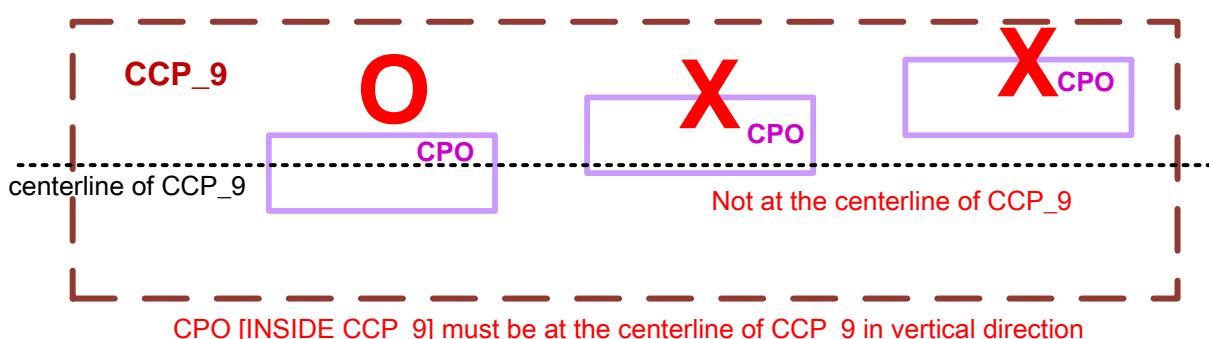
H240.PO.W.1.1 / H240.PO.S.25.5



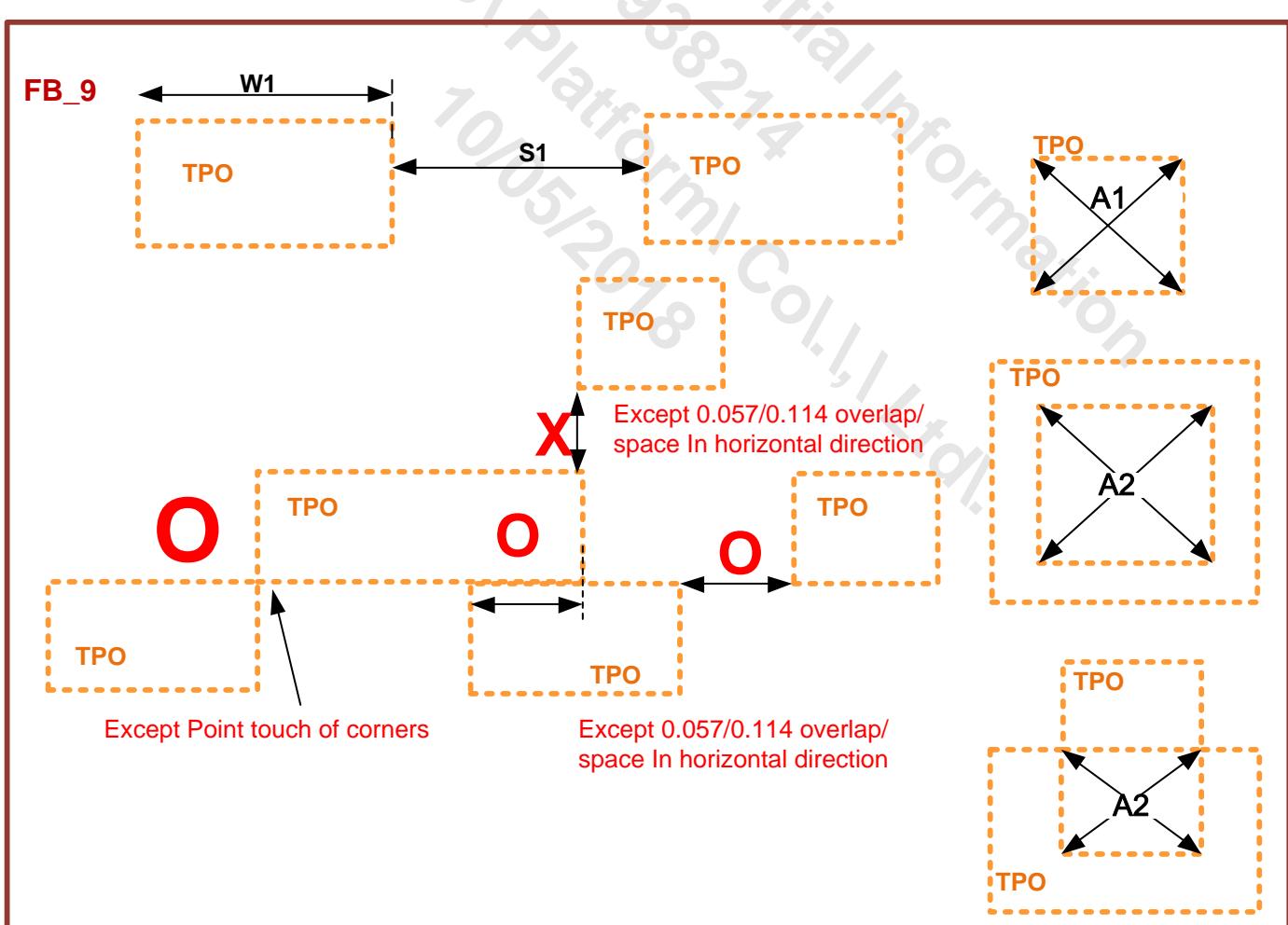
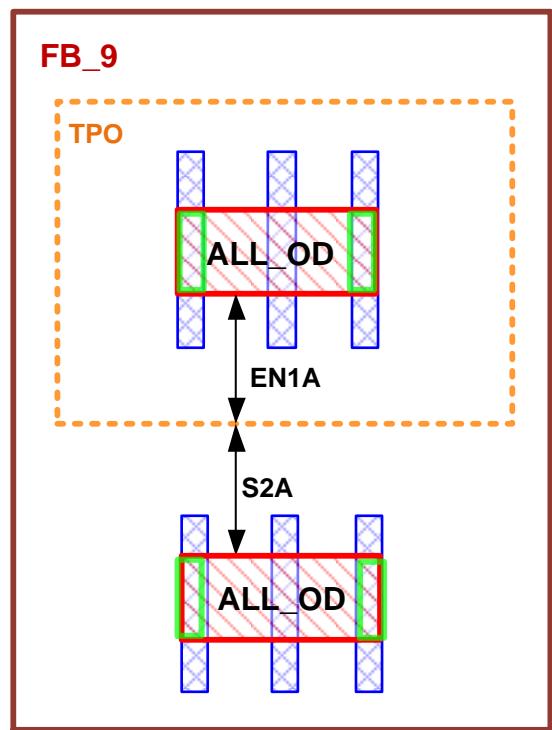
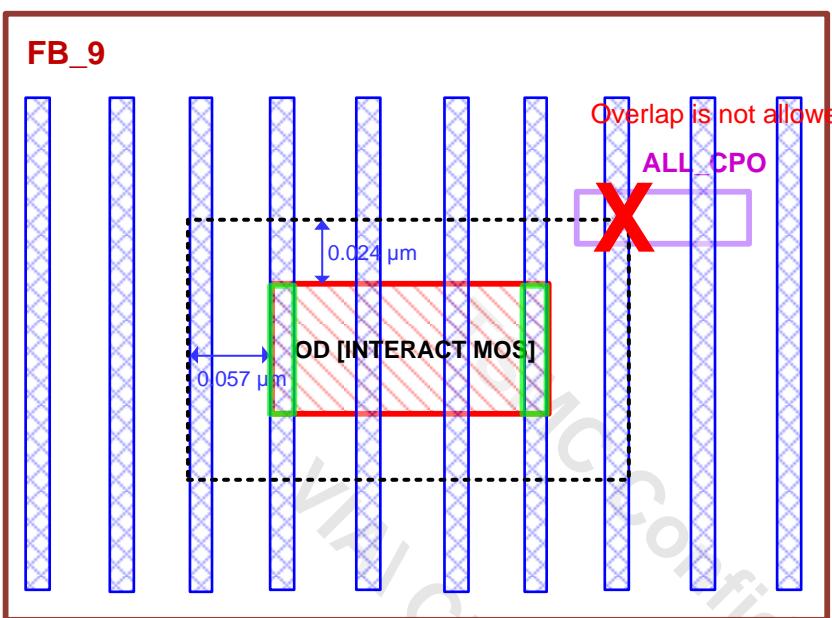
H240.CPO.W.1 / H240.CPO.S.4.2



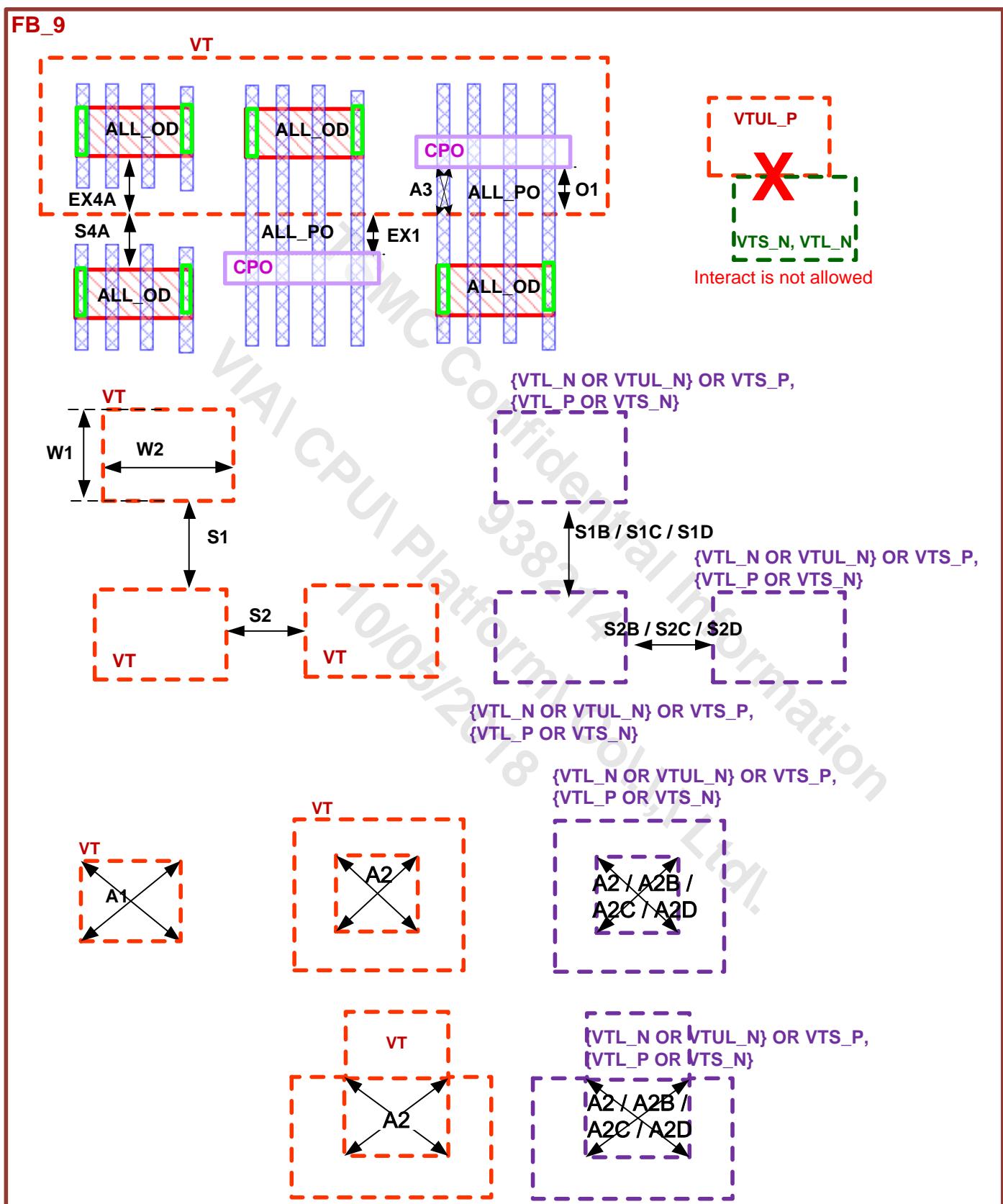
H240.CPO.O.3 / H240.CPO.R.16.1



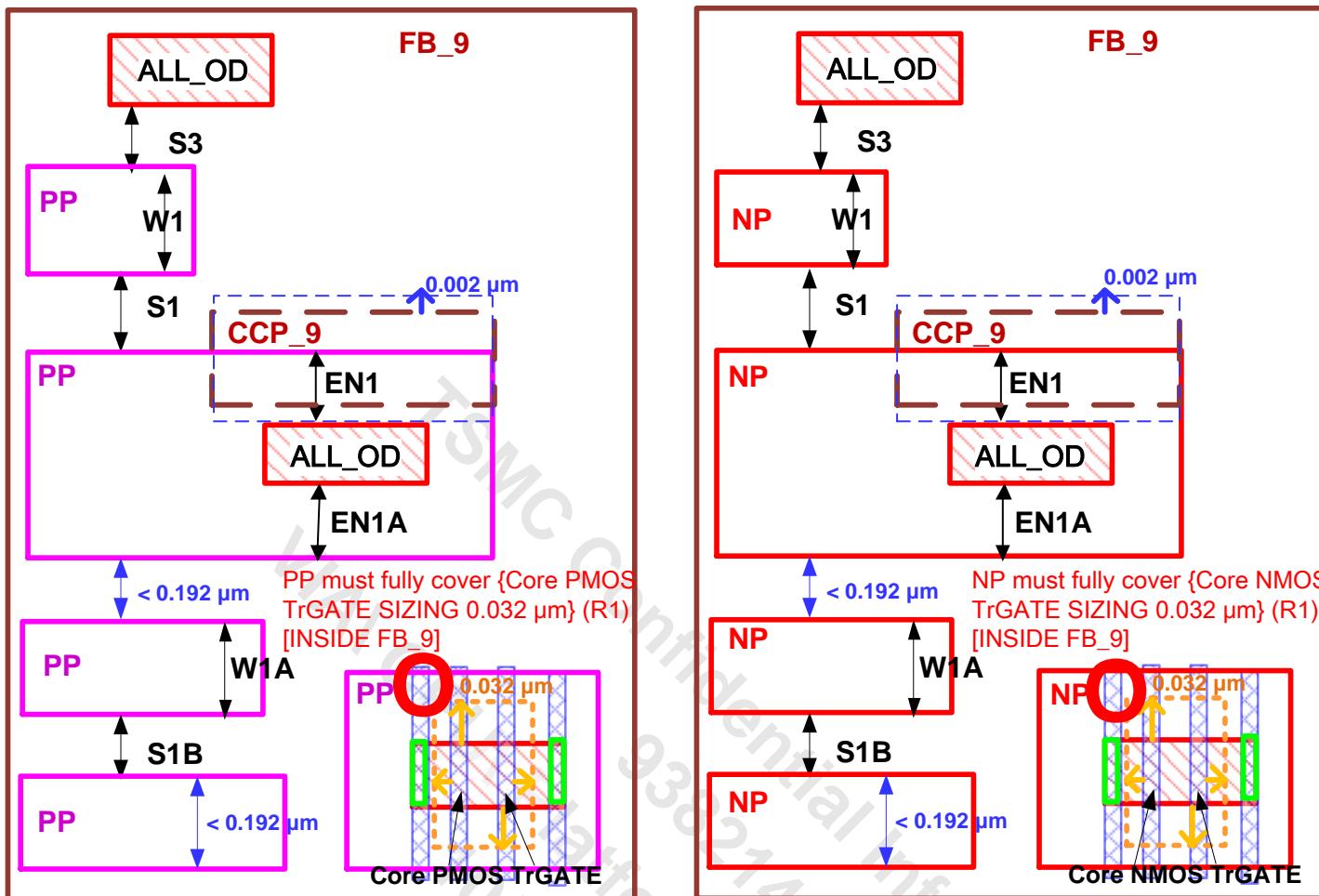
H240.CPO.R.12



H240-VT/PP/NP

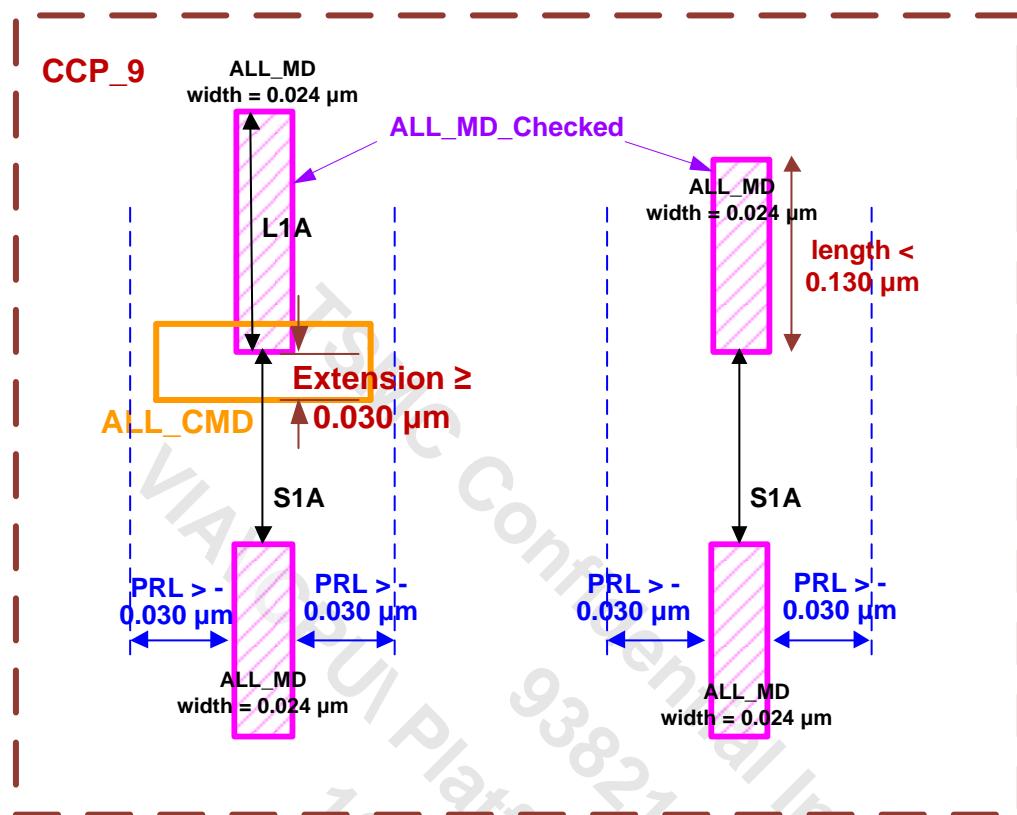
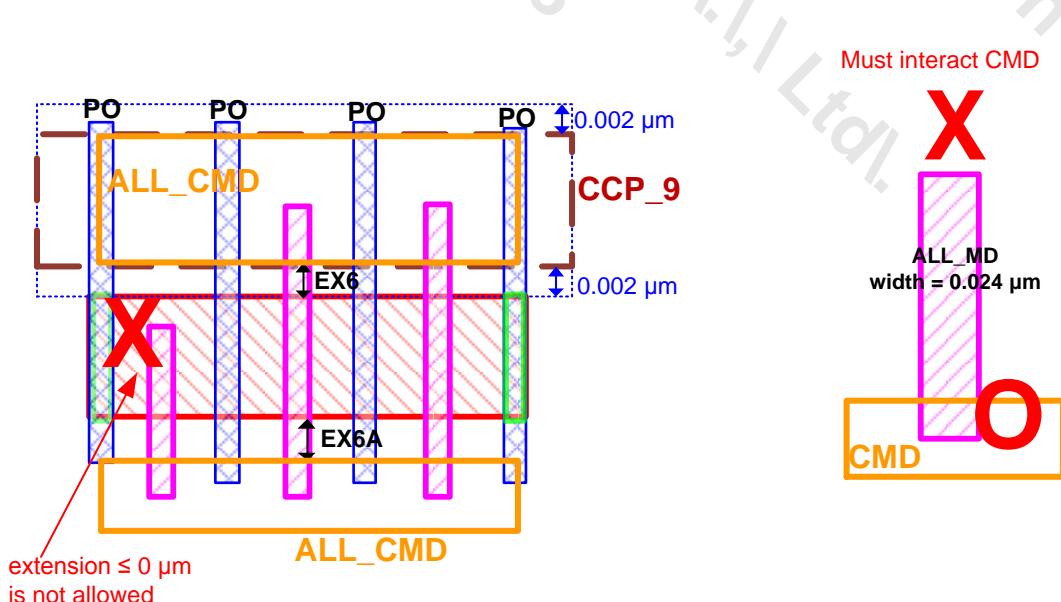


**H240.VT.W.2 / H240.VT.W.2.2 / H240.VT.S.2 / H240.VT.S.2.2 /
H240.VT.S.2.4 / H240.VT.S.4.1 / H240.VT.EX.1 / H240.VT.EX.4.1 /
H240.VT.O.1 / H240.VT.A.1 / H240.VT.A.2 / H240.VT.A.2.2 /
H240.VT.A.2.4 / H240.VT.A.3 / H240.VT.R.12**

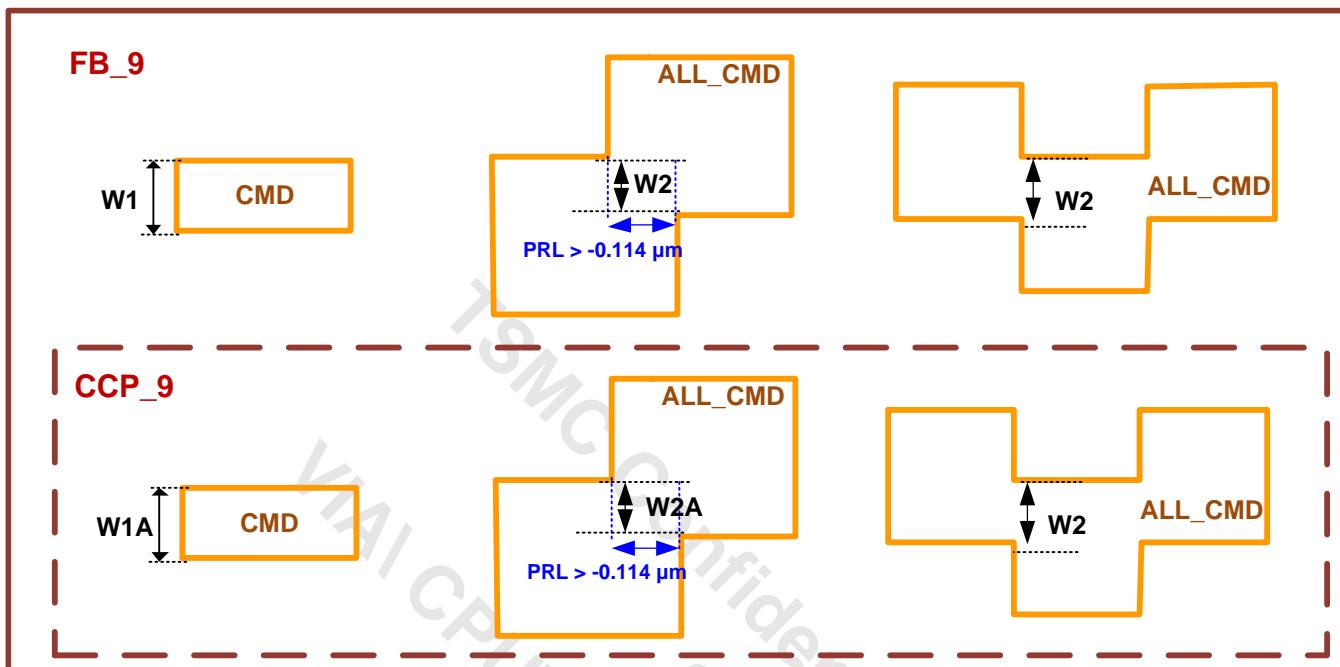


H240.PP.W.1 / H240.PP.W.1.1 /
 H240.PP.S.1 / H240.PP.S.1.2 /
 H240.PP.S.3 / H240.PP.EN.1 /
 H240.PP.EN.1.1 / H240.PP.R.1

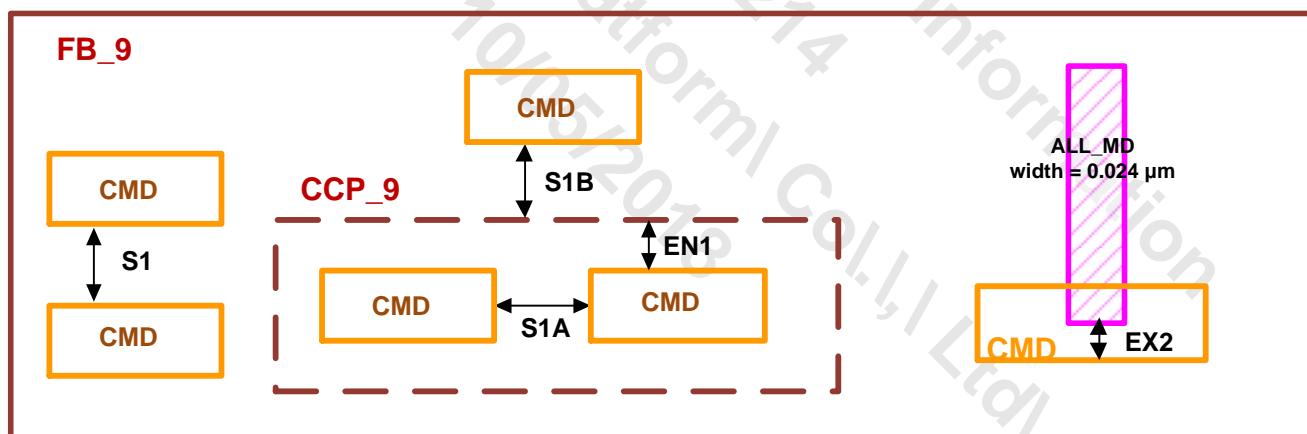
H240.NP.W.1 / H240.NP.W.1.1 /
 H240.NP.S.1 / H240.NP.S.1.2 /
 H240.NP.S.3 / H240.NP.EN.1 /
 H240.NP.EN.1.1 / H240.NP.R.1

H240-MD**H240.MD.S.1.1 / H240.MD.L.1.1****FB_9****H240.MD.EX.6 / H240.MD.EX.6.1 / H240.MD.R.1**

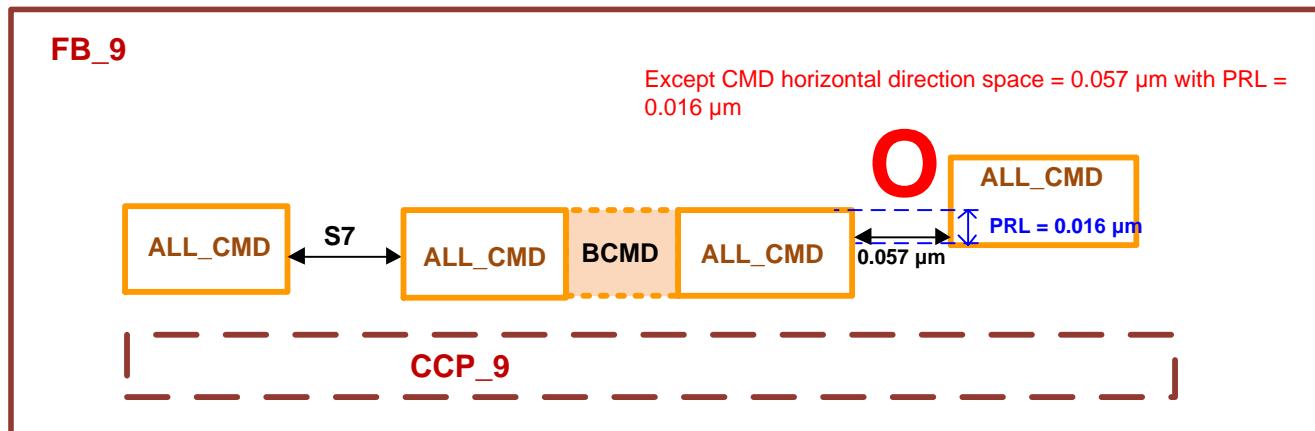
H240-CMD



H240.CMD.W.1 / H240.CMD.W.1.1 /
H240.CMD.W.2 / H240.CMD.W.2.1

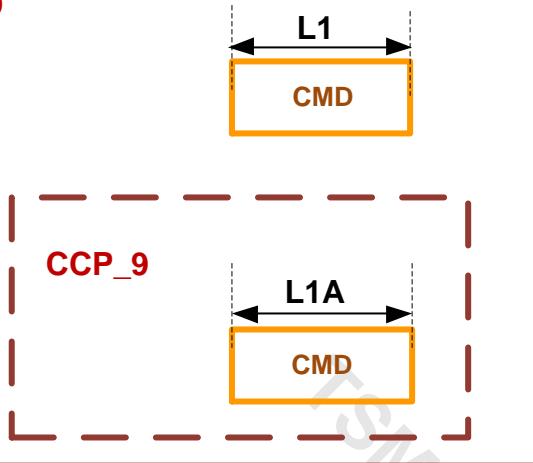


H240.CMD.S.1 / H240.CMD.S.1.1 / H240.CMD.S.1.2 /
H240.CMD.EN.1 / H240.CMD.EX.2



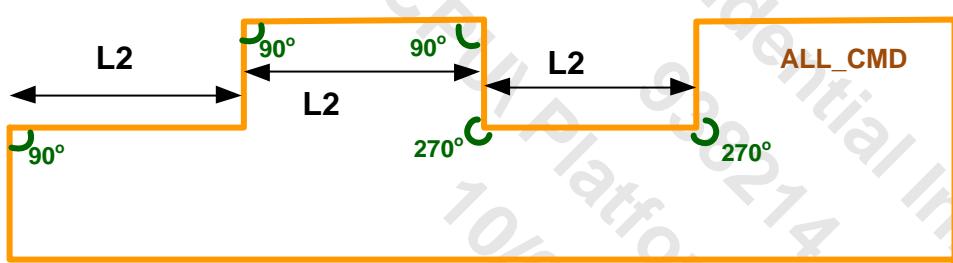
H240.CMD.S.7

FB_9



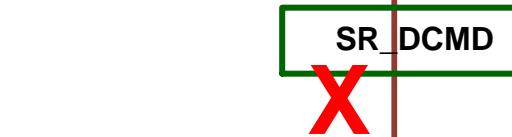
H240.CMD.L.1 / H240.CMD.L.1.1

FB_9



H240.CMD.L.2

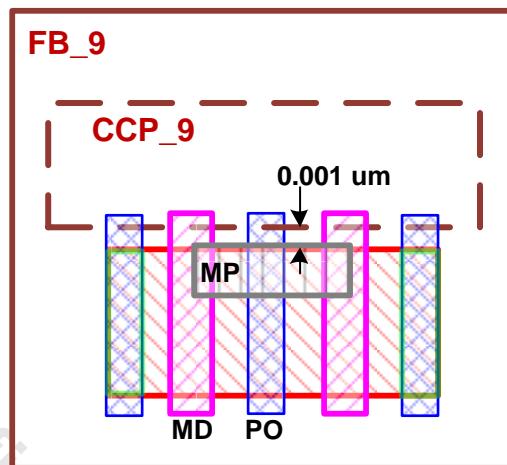
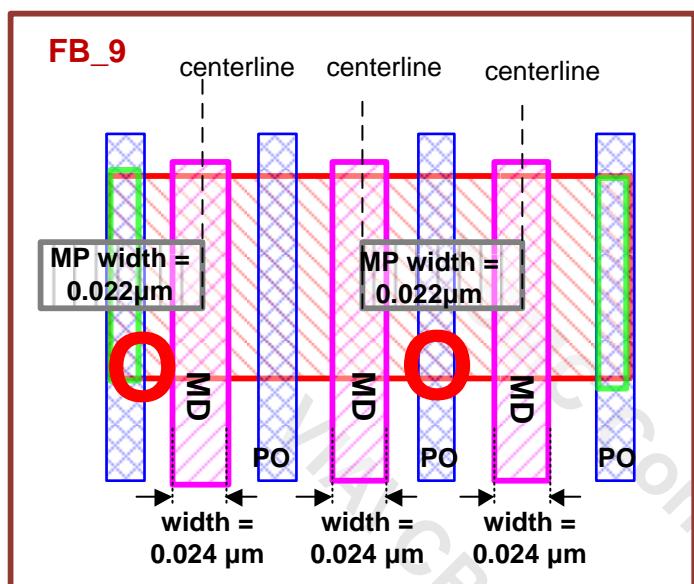
FB_9



Overlap is not allowed

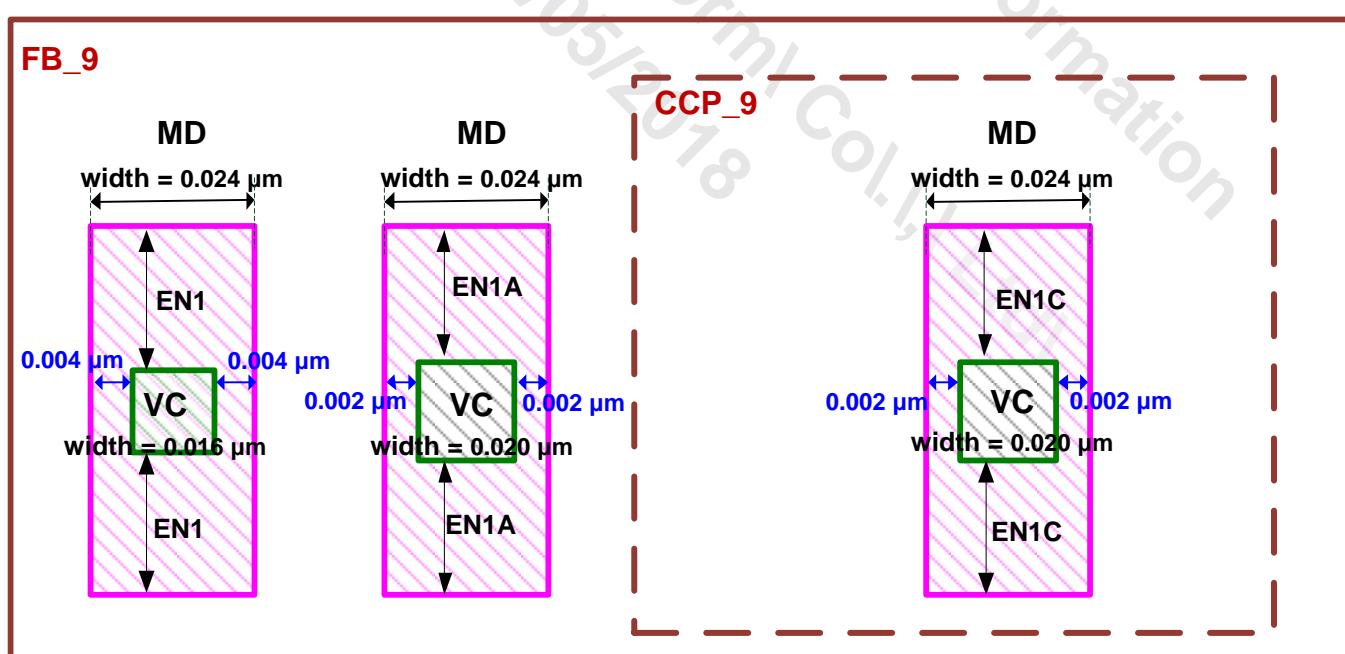
H240.CMD.R.6.3

H240-MP/VC



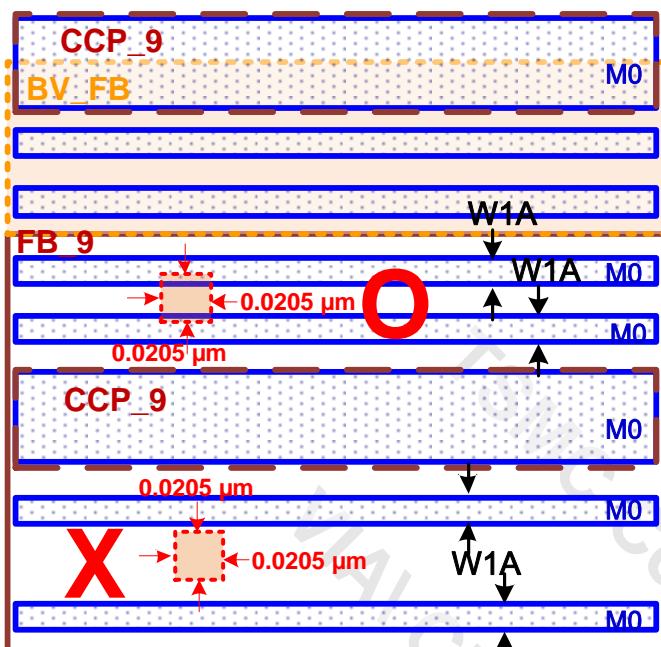
H240.MP.R.7

H240.MP.R.9



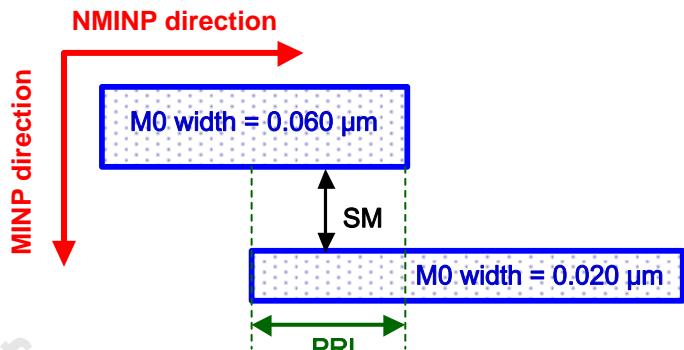
H240.VC.EN.1 / H240.VC.EN.1.1 / H240.VC.EN.1.3

H240-M0/CM0/VIA0

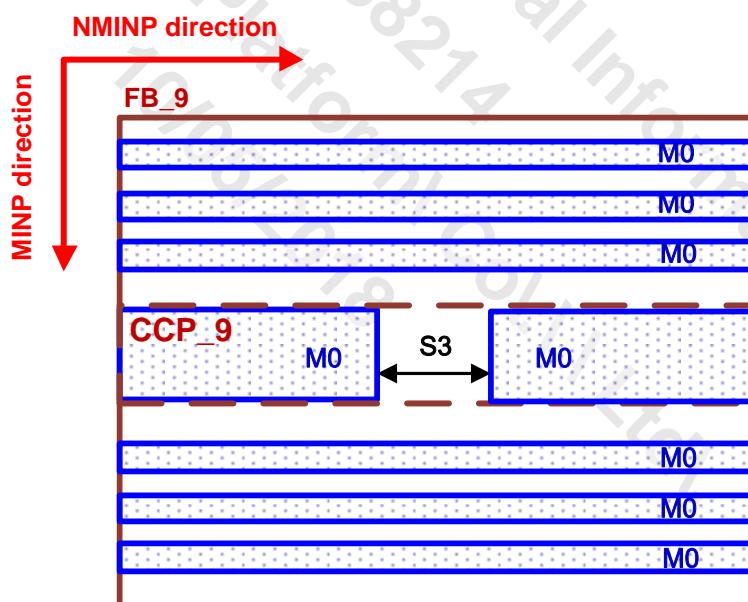


H240.M0.W.1.1 / H240.M0.S.19

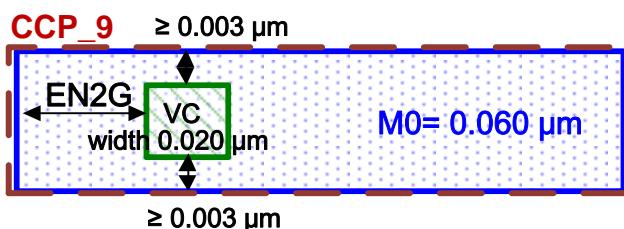
{}{FB_9 OR BV_FB [width = 0.120/0.240 μm]}
SIZING 0.090 μm in vertical direction



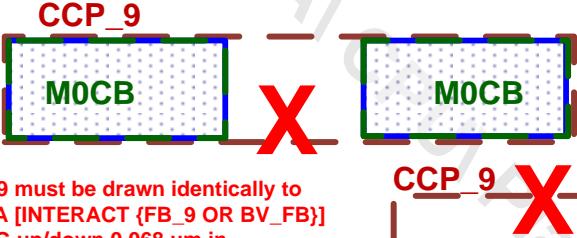
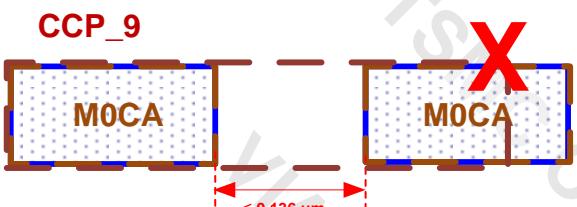
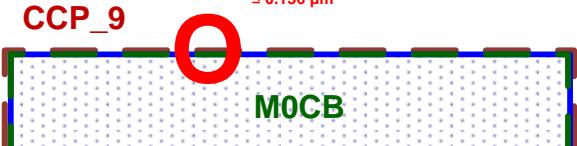
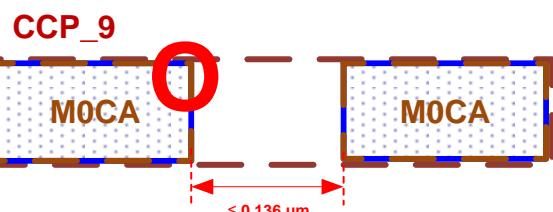
H240.M0.S.2.3



H240.M0.S.3

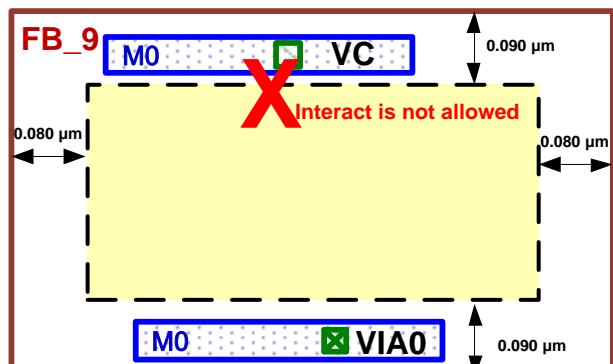


H240.M0.EN.2.7



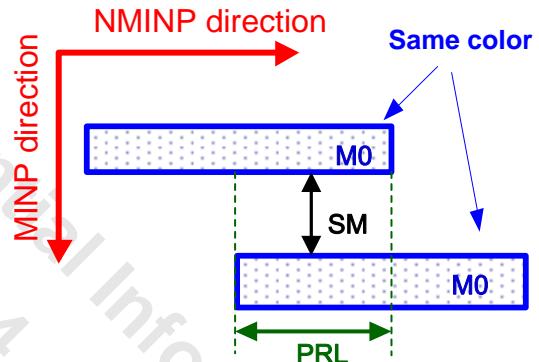
CCP_9 must be drawn identically to
(M0CA [INTERACT {FB_9 OR BV_FB}]
SIZING up/down 0.068 μm in
horizontal direction} or M0CB
[INTERACT {FB_9 OR BV_FB}])

H240.M0.R.15.1



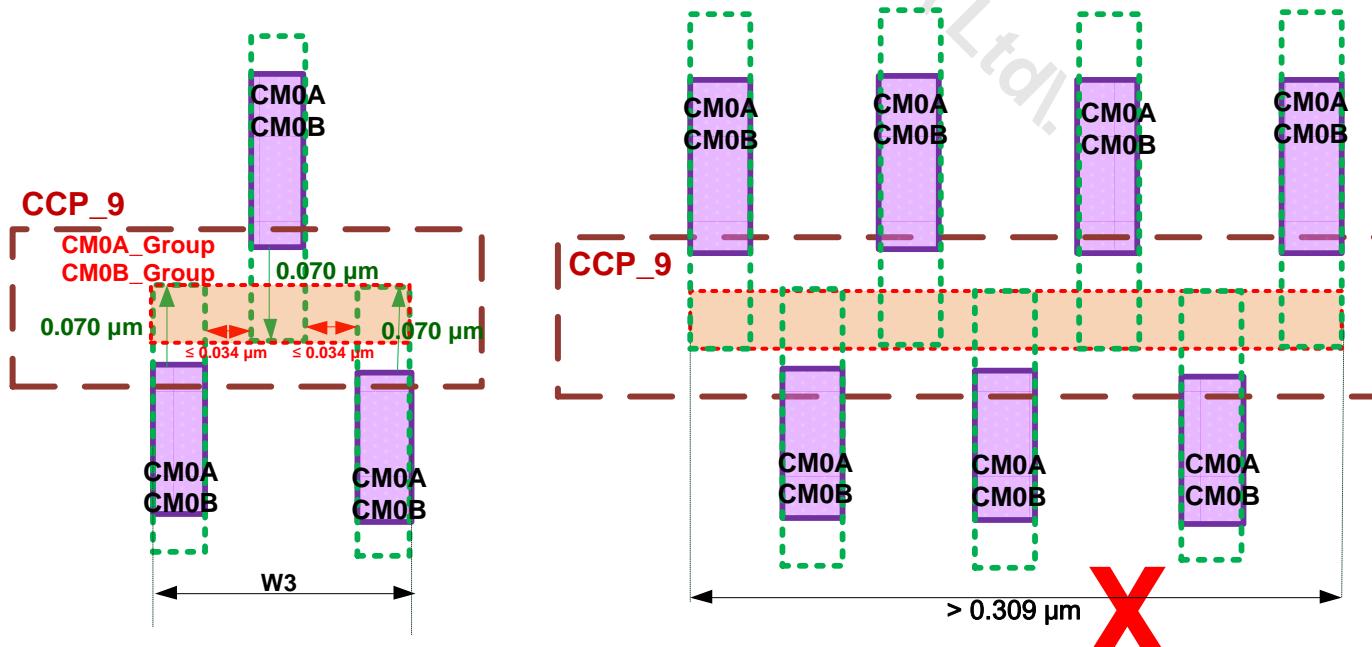
H240.M0.R.20

{(FB_9 OR BV_FB [width = 0.120/0.240 μm])
SIZING 0.124 μm in horizontal direction}



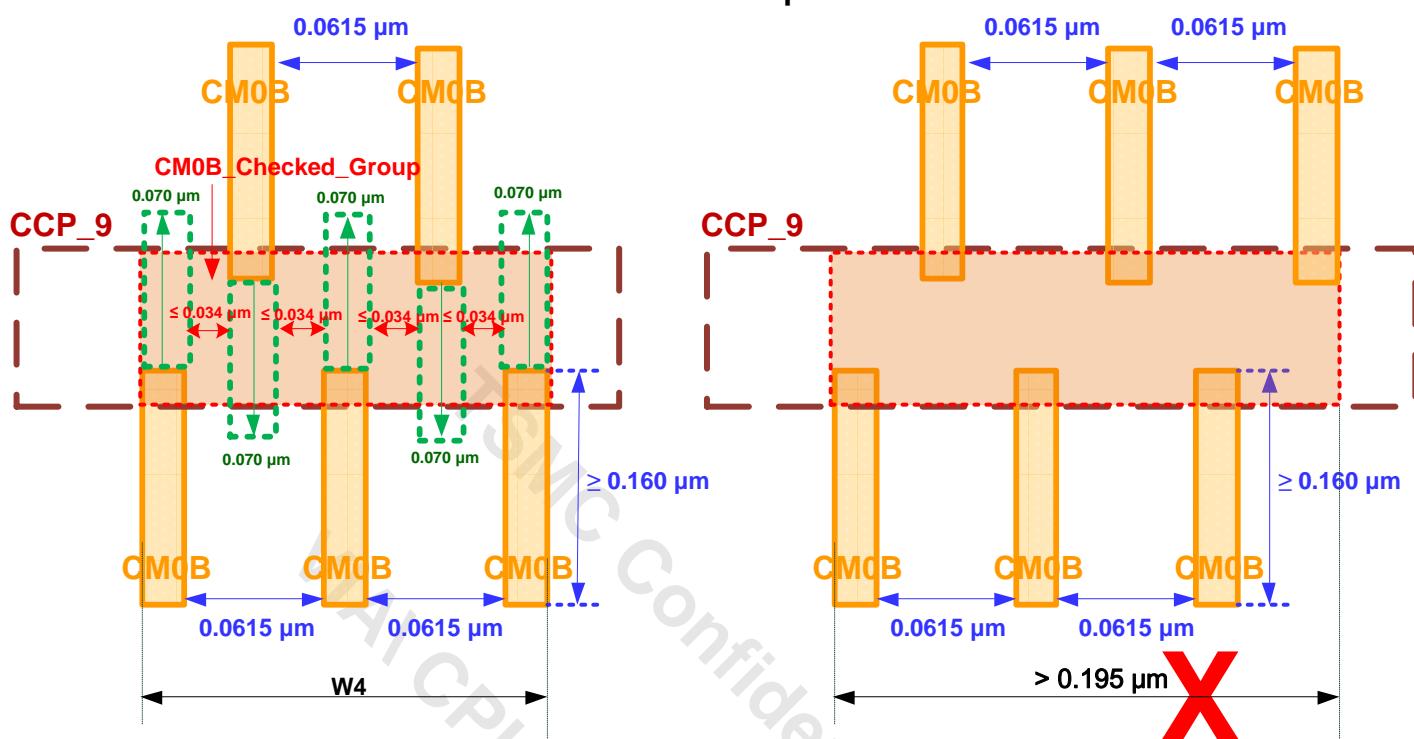
H240.M0.CS.1.1 / H240.M0.CS.1.2.1

Example:

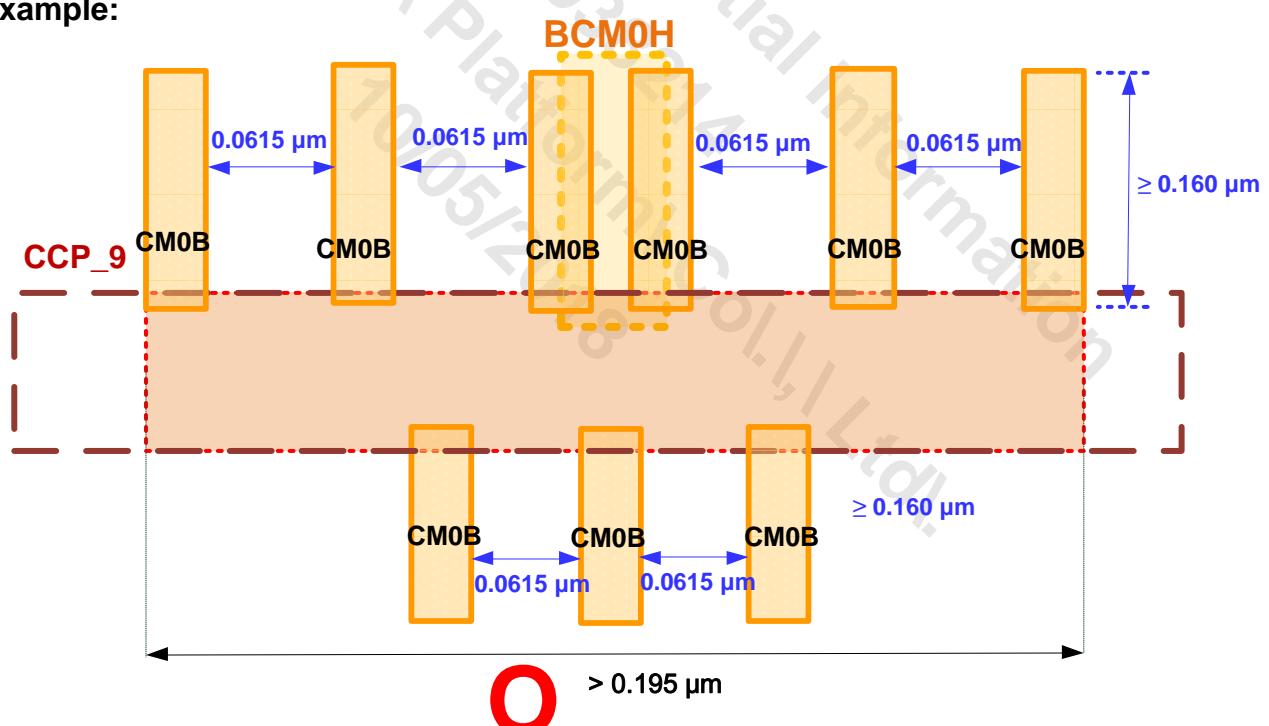


H240.CM0A.W.3 / H240.CM0B.W.3

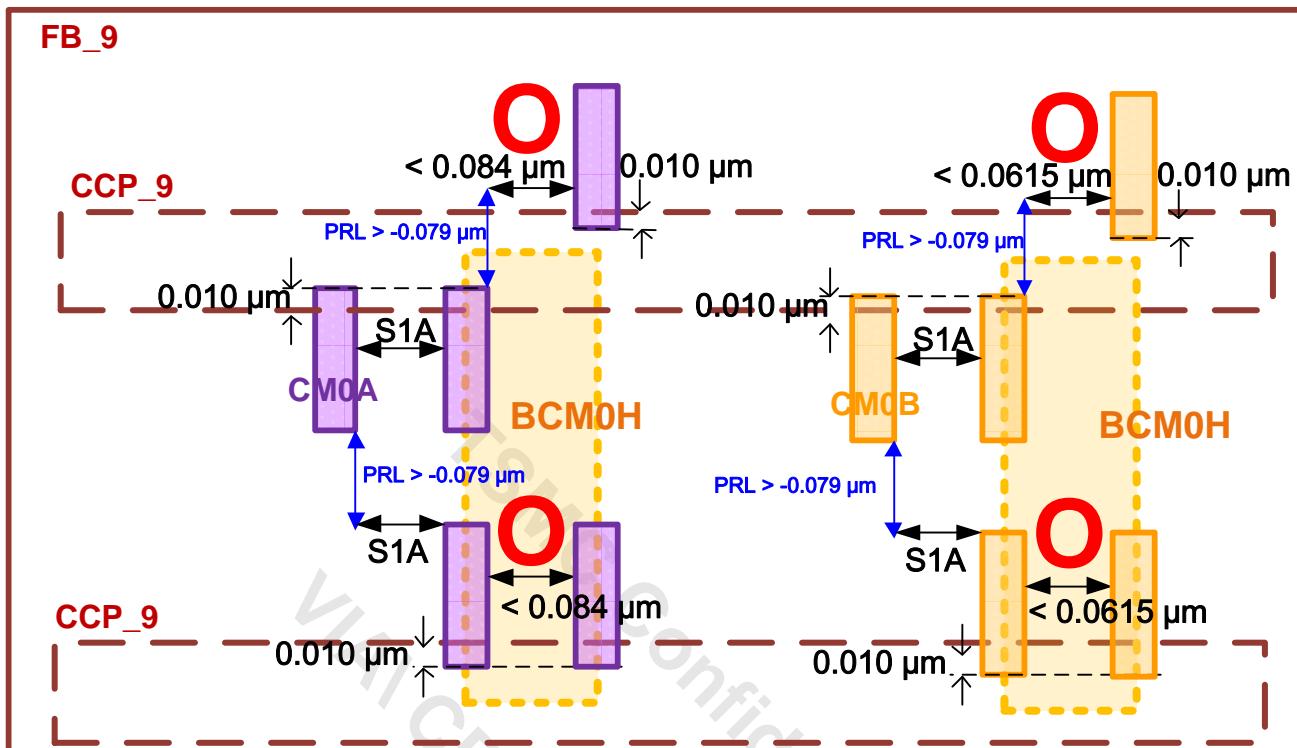
Example:



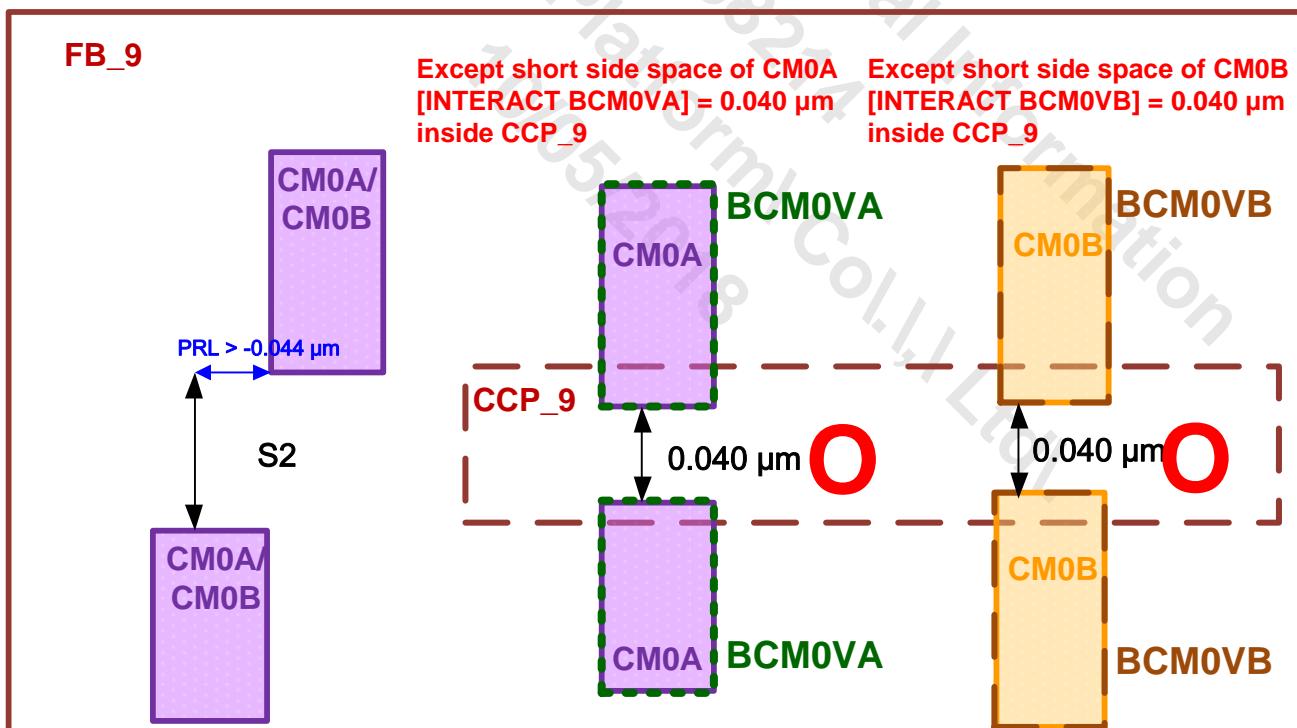
Example:



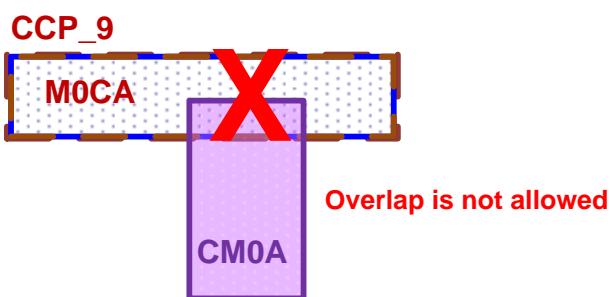
H240.CM0B.W.4



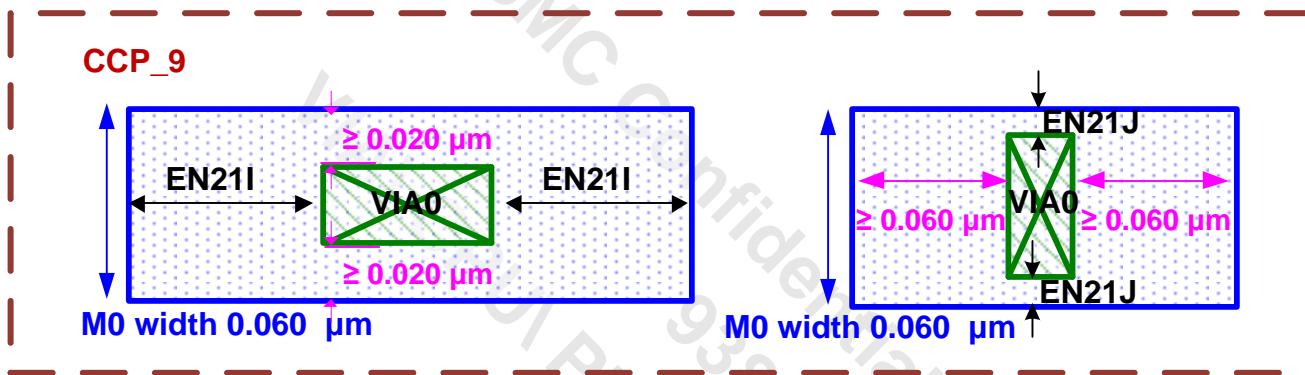
H240.CM0A.S.1.1 / H240.CM0B.S.1.1



H240.CM0A.S.2 / H240.CM0B.S.2



H240.CM0A.R.7



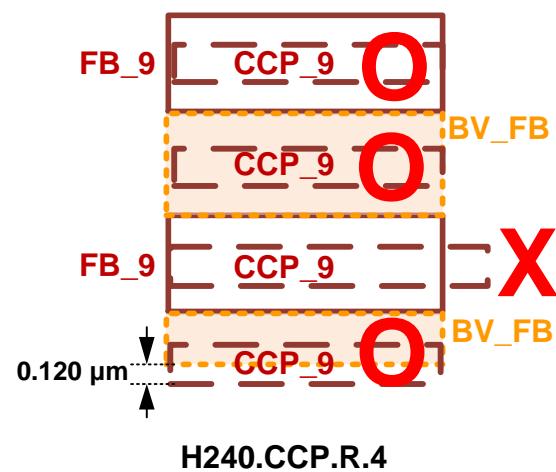
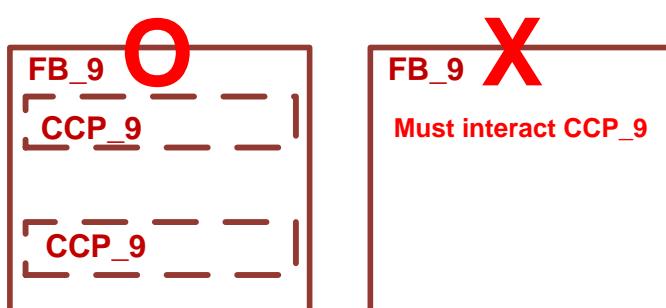
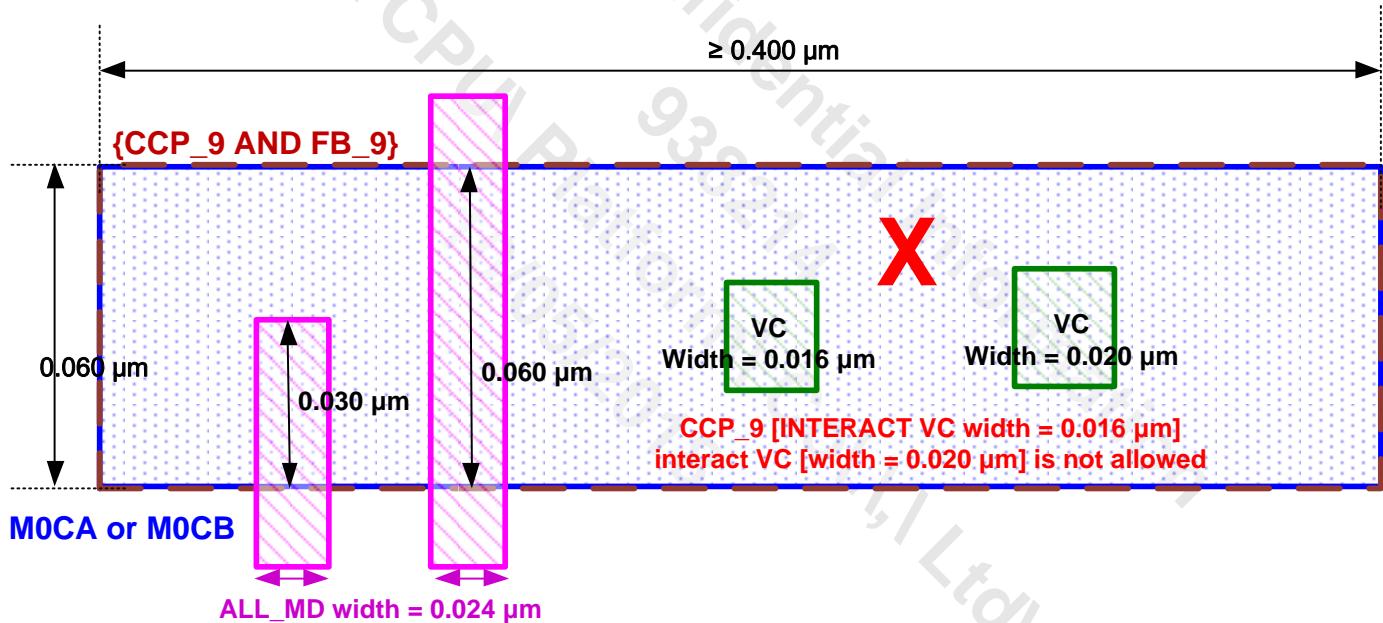
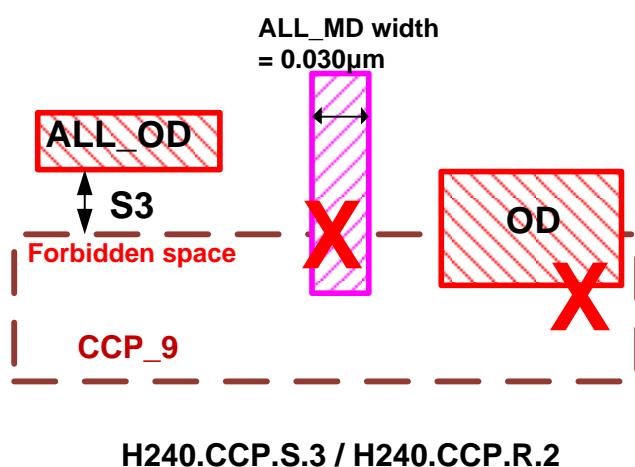
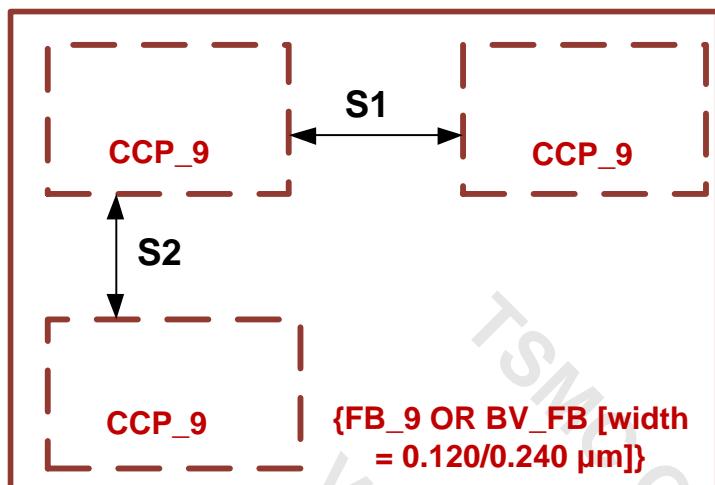
H240.VIA0.EN.21.9 / H240.VIA0.EN.21.10

4.5.13.3.1 H240 Confined Compact Pattern (CCP) Layout Rules for Power Rail

CCP_9 (CAD layer: 98;1) is used to define Confined Compact Pattern inside FB_9.

Rule No.	Description	Label	Op.	Rule
H240.CCP.S.1	Space	S1	\geq	0.1800
H240.CCP.S.2	Space in vertical direction [INSIDE {FB_9 OR BV_FBF [width = 0.120/0.240 $\mu\text{m}]]}]$	S2	=	0.1800
H240.CCP.S.3	Forbidden space of CCP_9 to ALL_OD in vertical direction	S3	=	0.0320
H240.CCP.R.1	Confined Compact Pattern 9 (CCP_9) must be a rectangle [width = 0.060 μm , length \geq 0.400 μm] and coincident to M0CA or M0CB			
H240.CCP.R.1.1	{CCP_9 AND FB_9} must interact ALL_MD [width = 0.024 μm], and overlap ALL_MD [width = 0.024 μm] must be 0.030 μm or 0.060 μm in vertical direction			
H240.CCP.R.1.3	CCP_9 [INTERACT VC width = 0.016 μm] interact VC [width = 0.020 μm] is not allowed			
H240.CCP.R.2	CCP_9 overlap ALL_MD [width = 0.030 μm] or OD is not allowed (Except HEADER_9)			
H240.CCP.R.3	FB_9 must interact CCP_9			
H240.CCP.R.4	CCP_9 must be inside {FB_9 OR {BV_FBF [width = 0.120/0.240 $\mu\text{m}]]} SIZING 0.120 \mu\text{m} in vertical direction}}$			

TSMC Confidential Information 938214
10/05/2018

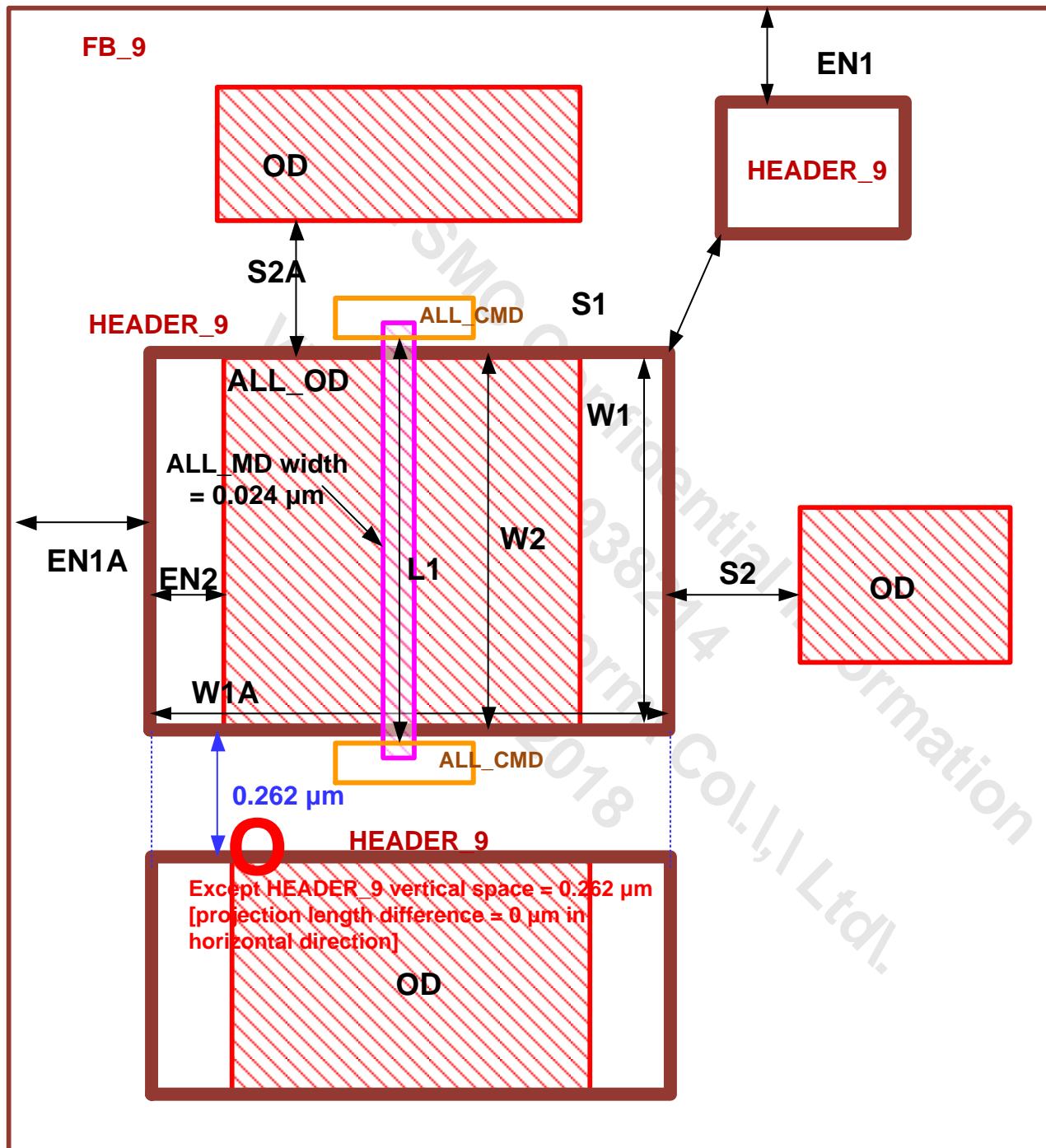
H240-CCP_9

4.5.13.3.2 H240 Header Cell Layout Rules

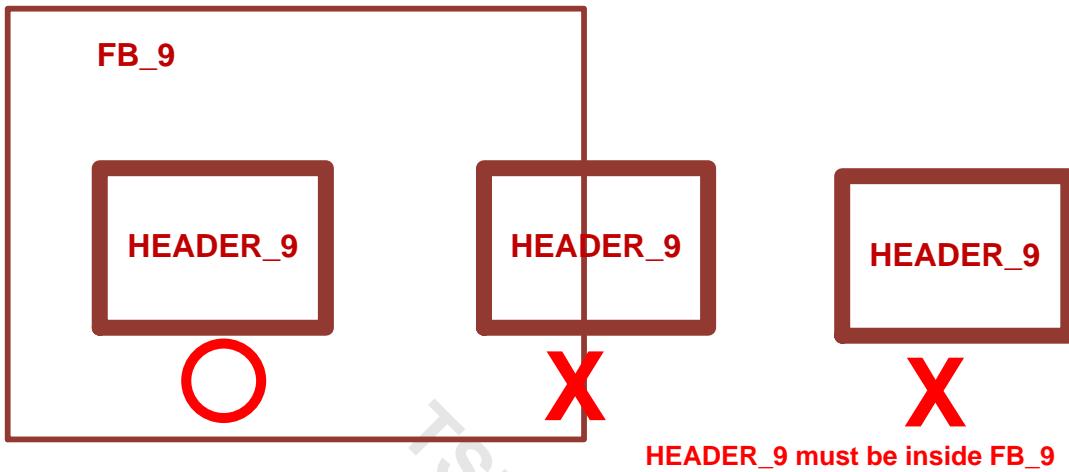
HEADER_9 (CAD layer: 6;129) is used to define HEADER cell inside FB_9

Rule No.	Description	Label	Op.	Rule
H240.HEADER.W.1	Width of HEADER_9 in vertical direction	W1	=	0.2180, 0.4580, 0.6980
H240.HEADER.W.1.1	Width of HEADER_9 in horizontal direction	W1A	≥	0.8100
H240.HEADER.W.2	Width of ALL_OD [INSIDE HEADER_9] in vertical direction	W2	=	0.2180, 0.4580, 0.6980
H240.HEADER.S.1	Space of HEADER_9 (Except following conditions: 1. HEADER_9 vertical space = 0.262 μm [projection length difference = 0 μm in horizontal direction])	S1	≥	0.6000
H240.HEADER.S.2	Space of HEADER_9 to OD in horizontal direction [PRL > -0.061 μm]	S2	≥	0.1040
H240.HEADER.S.2.1	Space of HEADER_9 to OD in vertical direction [PRL > -0.104 μm]	S2A	≥	0.0610
H240.HEADER.EN.1	Enclosure by FB_9 in vertical direction	EN1	=	0.2510+0.2400*n
H240.HEADER.EN.1.1	Enclosure by FB_9 in horizontal direction	EN1A	≥	0.5985
H240.HEADER.EN.2	Enclosure of OD in horizontal direction (Cut is not allowed)	EN2	=	0.1085 ~ 0.1100
H240.HEADER.L.1	Length of {ALL_MD [width = 0.024 μm, INTERACT HEADER_9] NOT ALL_CMD} in vertical direction	L1	=	0.0420 ~ 1.6640
H240.HEADER.R.1	HEADER_9 must be inside FB_9			
H240.HEADER.R.2	Horizontal edge of HEADER_9 must abut ALL_OD			
H240.HEADER.R.3	Horizontal edge of OD [INSIDE HEADER_9] must be fully projected by another OD with space = 0.061 μm.			
H240.HEADER.R.3.1	Horizontal edge of OD_Forbidden_Region interact OD is not allowed. OD_Forbidden_Region { {{HEADER_9 SIZING 0.104 μm in horizontal direction} NOT OD} SIZING 0.061 μm in vertical direction}			
H240.HEADER.R.4	HEADER_9 must be a rectangle orthogonal to grid			
H240.HEADER.R.5	Only one OD is allowed inside HEADER_9			

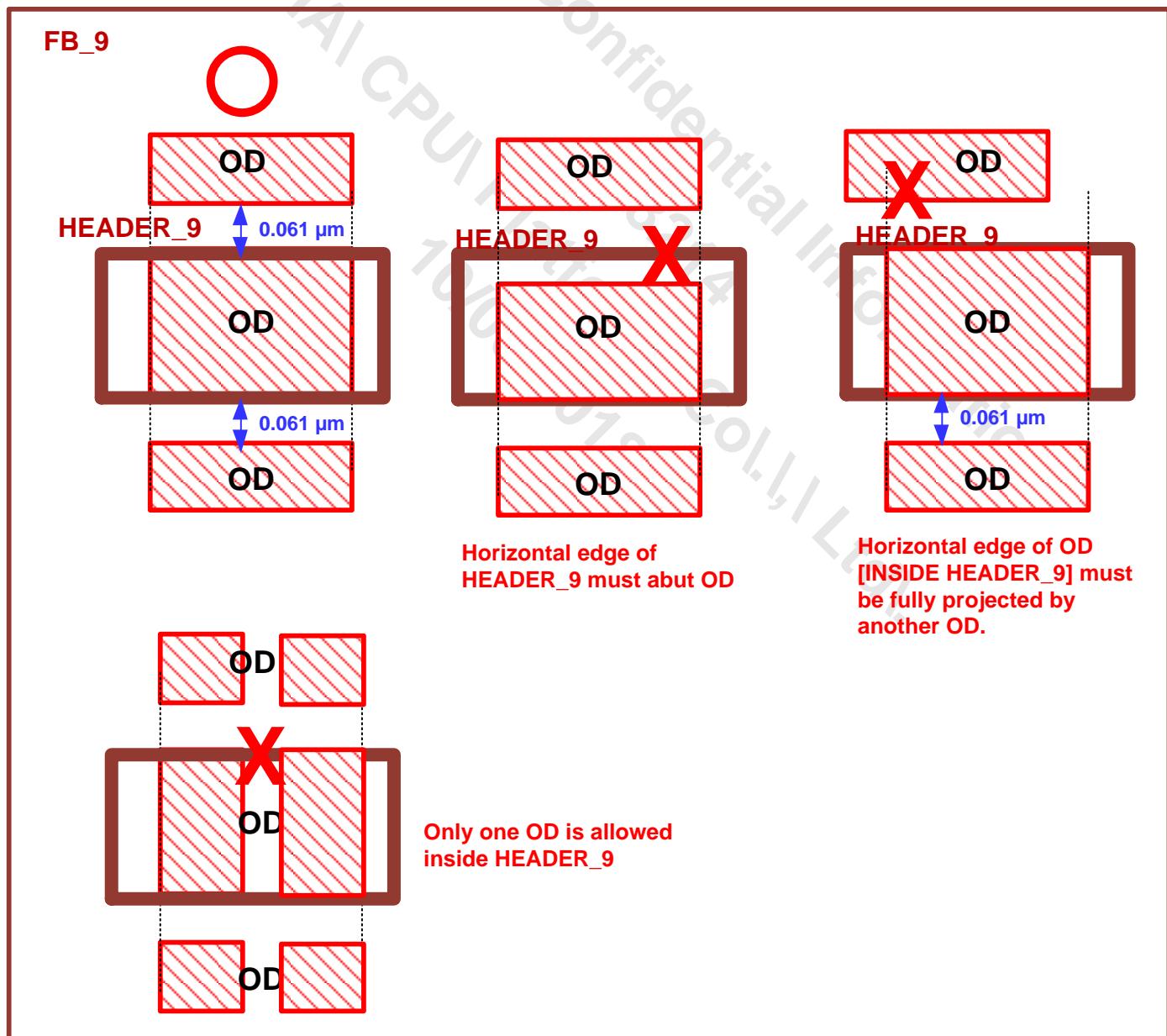
H240-HEADER



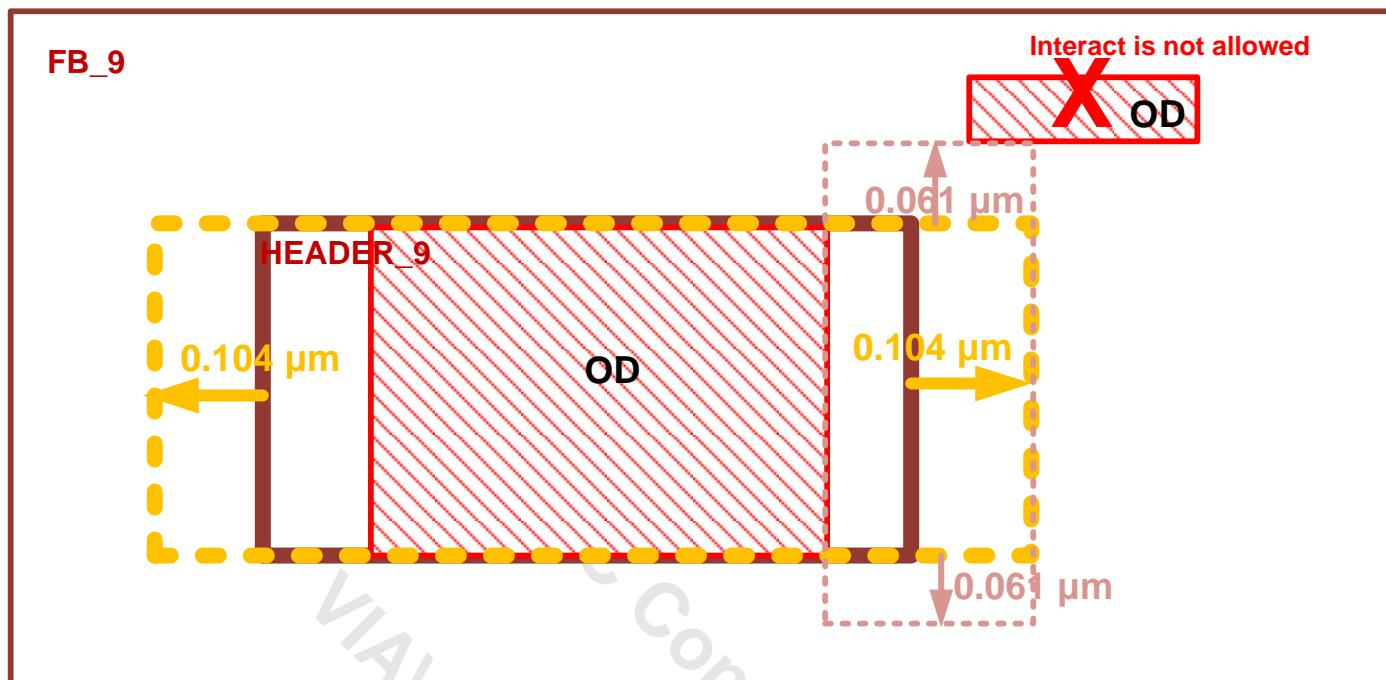
H240.HEADER.W.1 / H240.HEADER.W.1.1 /
H240.HEADER.W.2 / H240.HEADER.S.1 /
H240.HEADER.S.2 / H240.HEADER.S.2.1 /
H240.HEADER.EN.1 / H240.HEADER.EN.1.1 /
H240.HEADER.EN.2 / H240.HEADER.L.1



H240.HEADER.R.1



H240.HEADER.R.2 / H240.HEADER.R.3 / H240.HEADER.R.5



H240.HEADER.R.3.1



H240.HEADER.R.4

4.5.13.4 Cell Height 300 (H300) Layout Rules

FinFET_Boundary_8 (CAD layer: 250;8, or FB_8) is used for cell with cell height = 0.300 μm , $Lg \leq 0.011 \mu\text{m}$. CCP_8 (CAD layer: 98;8) is used to define Confined Compact Pattern inside FB_8.

HEADER_8 (CAD layer: 6;128) is used to define HEADER cell inside FB_8

Rule No.	Description	Label	Op.	Rule
H300.FB.W.1	Width of {FB_8 OR BV_FBF [width = 0.300 μm] in horizontal direction	W1	\geq	0.6610
H300.FB.W.1.0.1	Width of {FB_8 OR BV_FBF [width = 0.300 μm] [INTERACT PO_P63] in horizontal direction	W1	\geq	0.7150
H300.FB.W.1.1	Width of FB_8 in vertical direction	W1A	=	0.9000+0.6000*n
H300.FB.W.1.3	Vertical edge length of {FB_8 OR BV_FBF [width = 0.300 μm] between two consecutive 270-270 degree corners	W1C	=	0.9000+0.6000*n
H300.FB.W.1.4	Vertical edge length of {FB_8 OR BV_FBF [width = 0.300 μm] between two consecutive 90-270 degree corners	W1D	=	0.6000+0.6000*n
H300.FB.W.1.5	Concave corner to concave corner width of {FB_8 OR BV_FBF [width = 0.300 μm] in vertical direction	W1E	=	0.9000+0.6000*n
H300.FB.W.1.6®	Recommended width of {FB_8 OR BV_FBF [width = 0.300 μm] in vertical direction	W1F	=	1.5000+0.6000*n
H300.FB.EN.1	FB_8 enclosure of ALL_OD	EN1	\geq	0.0410
H300.FB.EN.1.1	Maximum enclosure of ALL_OD by FB_8	EN1A	\leq	0.2100
H300.FB.EN.1.2	Maximum enclosure of ALL_OD by FB_8 [INTERACT PO_P63]	EN1B	\leq	0.0905
H300.FB.EN.2	FB_8 enclosure of ALL_OD in horizontal direction	EN2	\geq	0.0700
H300.FB.EN.5	FB_8 enclosure of CCP_8 in vertical direction	EN5	=	0.1100+0.3000*n
H300.FB.EN.6	FB_8 enclosure of TPO, VT, NP, PP in vertical direction	EN6	=	0.1500*n
H300.FB.EN.7	prBoundary enclosure of FB_8 in vertical direction in cell level	EN7	=	0.1500+0.1200*n
H300.FB.R.11	Horizontal edge of {FB_8 SIZING -0.041 μm in vertical direction} must abut at least one ALL_OD			
H300.OD.W.1.1	Width of ALL_OD [INSIDE FB_8] in vertical direction (Except HEADER_8)	W1A	=	0.0380, 0.0680
H300.OD.W.1.5	Width of ALL_OD [INSIDE FB_8] in vertical direction (Except following conditions: 1. {ACTIVE INTERACT TrGATE})	W1E	=	0.0680
H300.OD.S.4	Space of STRAP [INSIDE FB_8] to ALL_OD in horizontal direction	S4	\geq	0.1000
H300.OD.S.4.1	Space of NWSTRAP to PWSTRAP [INSIDE FB_8]	S4A	\geq	0.1740
H300.OD.S.29	Horizontal edge of H300_OD [edge length > 0.278 μm] space to SR_DOD [width = 0.068 μm] in vertical direction (Except PO_P63, or following conditions: 1. violation length $\leq 0.278 \mu\text{m}$ and interact H300_OD concave corner) Definition of H300_OD: {OD [INSIDE FB_8] SIZING up/down 0.139 μm in horizontal direction} SIZING up/down 0.071 μm in vertical direction}	S29	=	0.0820
H300.OD.S.29.1	Horizontal edge of H300_OD_PO_P63 [edge length > 0.307 μm] space to SR_DOD [width = 0.068 μm] in vertical direction (Except following conditions: 1. violation length $\leq 0.307 \mu\text{m}$ and interact H300_OD_PO_P63 concave corner) Definition of H300_OD_PO_P63: {OD [INSIDE FB_8 [INTERACT PO_P63]] SIZING up/down 0.1535 μm in horizontal direction} SIZING up/down 0.071 μm in vertical direction}	S29A	=	0.0820

Rule No.	Description	Label	Op.	Rule
H300.OD.L.6.1	Horizontal edge length between two consecutive 90-90 degree corners [INSIDE FB_8]	L6A	\geq	0.1220
H300.OD.A.1	Area of ALL_OD [INSIDE FB_8]	A1	\geq	0.00440
H300.OD.R.8	STRAP [INSIDE FB_8] must be a rectangle orthogonal to grid, and vertical width = 0.068 μm			
H300.COD_H.W.1	Width [INSIDE {FB_8 SIZING 0.011 μm in vertical direction}] in vertical direction	W1	=	0.0600, 0.0900, 0.1200
H300.COD_H.W.1.1	Width [INSIDE {FB_8 SIZING 0.011 μm in vertical direction}] in vertical direction (Except CCP_8) DRC flags ALL_COD_H width between horizontal edges [PRL > 0.085 μm]	W1A	=	0.0900, 0.1200
H300.COD_H.W.1.2	Concave corner to concave corner width in vertical direction [INSIDE {FB_8 SIZING 0.011 μm in vertical direction}] [-0.085 μm < PRL \leq 0 μm]	W1B	=	0.0600
H300.COD_H.S.4	Space of ALL_COD_H in horizontal direction [PRL > -0.001 μm , INSIDE FB_8]	S4	\geq	0.0540
H300.COD_H.S.4.0.1	Space of ALL_COD_H in horizontal direction [PRL > -0.001 μm , INSIDE FB_8 [INTERACT PO_P63]]	S4	\geq	0.0630
H300.COD_H.S.4.1	Space of ALL_COD_H in horizontal direction [PRL > 0.029 μm , INSIDE FB_8]	S4A	\geq	0.0850
H300.COD_H.S.4.1.1	Space of ALL_COD_H in horizontal direction [PRL > 0.029 μm , INSIDE FB_8 [INTERACT PO_P63]]	S4A	\geq	0.1000
H300.COD_H.S.4.2	Space to ALL_COD_H vertical edge [INTERACT ALL_OD] in horizontal direction [INSIDE FB_8, PRL > -0.001 μm]	S4B	\geq	0.0850
H300.COD_H.S.4.2.1	Space to ALL_COD_H vertical edge [INTERACT ALL_OD] in horizontal direction [INSIDE FB_8 [INTERACT PO_P63], PRL > -0.001 μm]	S4B	\geq	0.1000
H300.COD_H.R.10	COD_H [INTERACT {FB_8 OR BV_FB [width = 0.300 μm }]} must be inside {{FB_8 OR BV_FB [width = 0.300 μm]}} expanding horizontal edge by 0.011 μm (Except Dummy_Cell)			
H300.COD_H.R.12	ALL_COD_H cut {CCP_8 SIZING -0.010 μm in vertical direction} is not allowed			
H300.COD_V.A.1	Area of ALL_COD_V [INSIDE FB_8]	A1	\geq	0.00690
H300.COD_V.A.2	Enclosed area of ALL_COD_V [INSIDE FB_8]	A2	\geq	0.01740
H300.PO.W.1.1	Width of ALL_PO [INSIDE FB_8]	W1A	=	0.0080, 0.0110
H300.PO.S.25.5	Empty space of ALL_PO [INSIDE FB_8 [NOT INTERACT PO_P63]] in horizontal direction DRC flags {{FB_8 [NOT INTERACT PO_P63] NOT ALL_PO} SIZING down/up 0.0245 μm in horizontal direction}	S25	\leq	0.0490
H300.PO.S.25.5.1	Empty space of ALL_PO [INSIDE FB_8 [INTERACT PO_P63]] in horizontal direction DRC flags {{FB_8 [INTERACT PO_P63] NOT ALL_PO} SIZING down/up 0.0275 μm in horizontal direction}	S25	\leq	0.0550
H300.CPO.W.1	Width of ALL_CPO [INTERACT FB_8] in vertical direction	W1	=	0.0160, 0.0300, 0.1000
H300.CPO.W.2.2	Maximum width of {{ALL_PO INTERACT CPO [width = 0.016/0.030 μm] NOT OD2} [INSIDE FB_8]}	W2B	\leq	0.0110
H300.CPO.S.4.2	Space of ALL_CPO [INSIDE CCP_8] to ALL_OD [INTERACT ALL_PO] in vertical direction (Overlap is not allowed)	S4B	\geq	0.0260
H300.CPO.EX.4	ALL_PO extension on ALL_CPO [width = 0.016/0.030 μm]	EX4	\geq	0.0900
H300.CPO.EN.7	CPO [width = 0.016 μm , INSIDE NW] enclosure by NW in vertical direction [INSIDE {FB_8 NOT CCP_8}]	EN7	=	0.0200

Rule No.	Description	Label	Op.	Rule
H300.CPO.O.3	CPO [width = 0.016 μm, INSIDE {FB_8 NOT CCP_8}] overlap NW in vertical direction	O3	=	0.0080, 0.0160
H300.CPO.R.9.1	ALL_CPO width [INSIDE FB_8, INTERACT neighboring two ALL_PO of TrGATE [{SIZING 0.010 μm} AND PO], in horizontal and outside OD direction], and the ALL_CPO number must be only one		=	0.0160, 0.0300
H300.CPO.R.12	CPO [INSIDE CCP_8] must be at the centerline of CCP_8 in vertical direction			
H300.VT.EX.1	{PO NOT CPO} extension on VT in vertical direction [INSIDE FB_8] (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	EX1	=	0.0200, ≥ 0.0430
H300.VT.O.1	VT overlap of {ALL_PO NOT CPO} in vertical direction [INSIDE FB_8] (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	O1	=	0.0200, ≥ 0.0430
H300.VT.A.1	Area of VT [INSIDE FB_8]	A1	≥	0.03420
H300.VT.A.2	Enclosed area of VT (include surrounding by point-touch polygons) [INSIDE FB_8]	A2	≥	0.03420
H300.VT.A.2.2	Enclosed area of {{VTL_N OR VTUL_N} OR VTS_P} [INSIDE FB_8] (include surrounding by point-touch polygons)	A2B	≥	0.03420
H300.VT.A.2.4	Enclosed area of {VTS_N OR VTL_P} [INSIDE FB_8] (include surrounding by point-touch polygons)	A2D	≥	0.03420
H300.VT.A.3	Area of {{ALL_PO NOT CPO} AND VT} [INTERACT FB_8] (Except Dummy_Cell)	A3	=	0.00016, 0.00022, ≥ 0.00034
H300.PP.W.1	Width [INSIDE FB_8]	W1	≥	0.1500
H300.PP.W.1.1	Width [space < 0.192 μm, INSIDE FB_8] (DRC flags opposite side)	W1A	=	0.1500, ≥ 0.1920
H300.PP.S.1	Space [INSIDE FB_8]	S1	≥	0.1500
H300.PP.S.1.2	Space [width < 0.192 μm, INSIDE FB_8] (DRC flags opposite side)	S1B	=	0.1500, ≥ 0.1920
H300.NP.W.1	Width [INSIDE FB_8]	W1	≥	0.1500
H300.NP.W.1.1	Width [space < 0.192 μm, INSIDE FB_8] (DRC flags opposite side)	W1A	=	0.1500, ≥ 0.1920
H300.NP.S.1	Space [INSIDE FB_8]	S1	≥	0.1500
H300.NP.S.1.2	Space [width < 0.192 μm, INSIDE FB_8] (DRC flags opposite side)	S1B	=	0.1500, ≥ 0.1920
H300.MD.S.8.2.1	Space of short side of ALL_MD [short side NOT INTERACT CMD] to ALL_OD in vertical direction [INSIDE {FB_8 NOT CCP_8}]	S8B1	≥	0.0370
H300.MD.S.23.2	MD [INTERACT OD] to 1st MD space rule: Space of Checked_MD_S1 to {ALL_MD NOT ALL_CMD} in horizontal direction [INSIDE FB_8] (Except PO_P63) Definition of Checked_MD_S1: {{MD [width = 0.024 μm] NOT CMD} AND {OD [width = 0.038 μm]} OR {OD [width = 0.068 μm] SIZING -0.027 μm in vertical direction}}}}	S23B	=	0.0330
H300.MD.S.23.2.1	MD [INTERACT OD] to 1st MD space rule: Space of Checked_MD_S1 to {ALL_MD NOT ALL_CMD} in horizontal direction [INSIDE FB_8 [INTERACT PO_P63]] Definition of Checked_MD_S1: {{MD [width = 0.024 μm] NOT CMD} AND {OD [width = 0.038 μm]} OR {OD [width = 0.068 μm] SIZING -0.027 μm in vertical direction}}}}	S23B	=	0.0390

Rule No.	Description	Label	Op.	Rule
H300.MD.EX.6	{ALL_MD NOT CMD} extension on ALL_OD edge [INTERACT {CCP_8 SIZING 0.001 μm in vertical direction}] in vertical direction [INSIDE {CCP_8 SIZING 0.001 μm in vertical direction}] (Extension < 0 μm is not allowed)	EX6	=	0.0020, 0.0260
H300.MD.EX.6.1	{ALL_MD NOT CMD} extension on ALL_OD in vertical direction [INSIDE {FB_8 NOT {CCP_8 SIZING 0.001 μm in vertical direction}}] (Extension < 0 μm is not allowed)	EX6A	≥	0.0020
H300.CMD.W.1	Width of CMD [INSIDE {FB_8 NOT CCP_8}] in vertical direction	W1	=	0.0400, 0.0560, 0.0960
H300.CMD.W.1.1	Width of CMD [INSIDE CCP_8] in vertical direction	W1A	=	0.0540, 0.0780
H300.CMD.W.2	Concave corner to concave corner width of ALL_CMD [INSIDE {FB_8 NOT CCP_8}] in vertical direction [PRL > -0.114 μm] DRC flags space between 2 horizontal ALL_CMD edge [INSIDE {FB_8 NOT CCP_8}] in vertical direction < 0.056 μm [PRL > -0.114 μm]	W2	=	0, 0.0560
H300.CMD.W.2.1	Concave corner to concave corner width of ALL_CMD [INSIDE CCP_8] in vertical direction [PRL > -0.114 μm] DRC flags space between 2 horizontal ALL_CMD edge [INSIDE CCP_8] in vertical direction < 0.030 μm [PRL > -0.114 μm]	W2A	=	0.0300
H300.CMD.S.1	Space of CMD in vertical direction [PRL > -0.057 μm, INSIDE FB_8]	S1	≥	0.0430
H300.CMD.S.1.1	Space of CMD [NOT INTERACT PO_P63] in horizontal direction [PRL > -0.060 μm, INSIDE CCP_8]	S1A	=	0.0570, ≥ 0.1140
H300.CMD.S.1.1.1	Space of CMD [INTERACT PO_P63] in horizontal direction [PRL > -0.060 μm, INSIDE CCP_8]	S1A	=	0.0630, ≥ 0.1260
H300.CMD.S.1.2	Space of CMD to CCP_8 in vertical direction [INSIDE FB_8] (Cut is not allowed)	S1B	=	0.0420, 0.0820, 0.1380
H300.CMD.S.2	Space of CMD [width = 0.040 μm] to CMD in vertical direction [PRL > -0.057 μm, INSIDE FB_8]	S2	=	0.0430, 0.0560, ≥ 0.0670
H300.CMD.S.2.1	Space of CMD [width = 0.056 μm] to CMD in vertical direction [PRL > -0.057 μm, INSIDE FB_8]	S2A	=	0.0830, ≥ 0.1070
H300.CMD.S.2.2	Space of CMD [width = 0.096 μm] to CMD in vertical direction [PRL > -0.057 μm, INSIDE FB_8]	S2B	=	0.0430, 0.0670, 0.0830, ≥ 0.1070
H300.CMD.S.2.4	Space of CMD [width = 0.054 μm] to CMD in vertical direction [PRL > -0.057 μm, INSIDE FB_8]	S2D	=	0.0430, 0.0670, 0.0830, ≥ 0.1070
H300.CMD.S.2.5	Space of CMD [width = 0.078 μm] to CMD in vertical direction [PRL > -0.057 μm, INSIDE FB_8]	S2E	=	0.0430, ≥ 0.0830
H300.CMD.S.7	Space of CMD [Derived from BCMD, INSIDE {FB_8 NOT CCP_8}] in horizontal direction [PRL > 0 μm]	S7	≥	0.1080
H300.CMD.EN.1	ALL_CMD enclosure by CCP_8 in vertical direction	EN1	=	0.0010, 0.0250
H300.CMD.EX.2	ALL_CMD extension on ALL_MD [width = 0.024 μm] in vertical direction [INSIDE FB_8]	EX2	≥	0.0200
H300.CMD.L.1	Length of CMD [INSIDE {FB_8 NOT CCP_8}] in horizontal direction	L1	≥	0.1140
H300.CMD.L.1.1	Length of CMD [NOT INTERACT PO_P63, INSIDE CCP_8] in horizontal direction	L1A	=	0.0570, ≥ 0.1140
H300.CMD.L.1.1.1	Length of CMD [INTERACT PO_P63, INSIDE CCP_8] in horizontal direction	L1A	=	0.0630, ≥ 0.1260
H300.CMD.L.2	Horizontal edge length of ALL_CMD [NOT INTERACT PO_P63, INSIDE FB_8] between two consecutive 270-270 degree corners (U-shape), or two consecutive 90-90 degree corners (T-shape), or two consecutive 90-270 degree corners (L-shape)	L2	=	0.0570, ≥ 0.1140
H300.CMD.L.2.1	Horizontal edge length of ALL_CMD [INTERACT PO_P63, INSIDE FB_8] between two consecutive 270-270 degree corners (U-shape), or two consecutive 90-90 degree corners (T-shape), or two consecutive 90-270 degree corners (L-shape)	L2	=	0.0630, ≥ 0.1260

Rule No.	Description	Label	Op.	Rule
H300.CMD.L.3	Z-shape ALL_CMD [NOT INTERACT PO_P63, INSIDE FB_8] length in horizontal direction DRC flags space between 2 vertical CMD edge between 90-270 degree corners in horizontal direction < 0.1140 μm [PRL > -0.126 μm]	L3	=	0.0570, ≥ 0.1140
H300.CMD.L.3.1	Z-shape ALL_CMD [INTERACT PO_P63, INSIDE FB_8] length in horizontal direction DRC flags space between 2 vertical CMD edge between 90-270 degree corners in horizontal direction < 0.1260 μm [PRL > -0.126 μm]	L3	=	0.0630, ≥ 0.1260
H300.CMD.R.6.3	SR_DCMD overlap FB_8 is not allowed			
H300.CMD.R.10	ALL_MD overlap Checked_CMD_Region [INSIDE FB_8] is not allowed Definition of Check_CMD_Region: {{CMD [width = 0.040 μm] SIZING up/down 0.028 μm in vertical direction} NOT CMD [width = 0.040 μm]}			
H300.MP.S.2.5	Space of ALL_MP to ALL_MD [short side INTERACT CCP_8 and NOT INTERACT ALL_CMD]	S2E	≥	0.0490
H300.MP.R.9	{ALL_MP [width = 0.022 μm, INSIDE FB_8] SIZING 0.001 μm} must abut CCP_8			
H300.VC.EN.1	Square VC [width = 0.016 μm, INTERACT MD [width = 0.024 μm]] enclosure by MD [width = 0.024 μm] for two opposite sides with the other two sides = 0.004 μm [INSIDE {FB_8 NOT CCP_8}]	EN1	≥	0.0190
H300.VC.EN.1.1	Square VC [width = 0.020 μm, INTERACT MD [width = 0.024 μm]] enclosure by MD [width = 0.024 μm] for two opposite sides with the other two sides = 0.002 μm [INSIDE {FB_8 NOT CCP_8}]	EN1A	≥	0.0170
H300.VC.EN.1.3	Square VC [width = 0.020 μm, INTERACT MD [width = 0.024 μm]] enclosure by MD [width = 0.024 μm] for two opposite sides with the other two sides = 0.002 μm [INSIDE CCP_8]	EN1C	≥	0.0070
H300.M0.W.1.1	Width in MINP direction [INSIDE {{FB_8 OR BV_FB [width = 0.150/0.300 μm]} NOT CCP_8}]	W1A	=	0.0200
H300.M0.S.2.3.1	Space of M0 [width = 0.080 μm] to M0 [width = 0.020 μm] in MINP direction [PRL > -0.040 μm, INSIDE {{FB_8 OR BV_FB [width = 0.150/0.300 μm]} SIZING 0.040 μm in horizontal direction}]	SM	≥	0.0200
H300.M0.S.3	Space of M0 [INTERACT CCP_8] in NMINP direction [PRL > 0 μm]	S3	≥	0.1800
H300.M0.S.19	Empty space of M0 [INSIDE {FB_8 OR BV_FB [width = 0.150/0.300 μm]}] DRC flags {{{{FB_8 OR BV_FB [width = 0.150/0.300 μm]} SIZING -0.030 μm in vertical direction} NOT {M0 OR CCP_8}} SIZING down/up 0.010 μm}	S19	≤	0.0200
H300.M0.EN.2.8	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.080 μm] for two opposite sides with the other two sides ≥ 0.003 μm [INSIDE CCP_8]	EN2H	≥	0.0600
H300.M0.R.15.1	CCP_8 must be drawn identically to {M0CA [INTERACT {FB_8 OR BV_FB [width = 0.150/0.300 μm]}] SIZING up/down 0.090 μm in horizontal direction}			
H300.M0.R.20	{M0 AND {FB_8 NOT {{FB_8 SIZING -0.110 μm in vertical direction} SIZING -0.080 μm in horizontal direction}}} interact VC, VIA0 is not allowed			

Rule No.	Description	Label	Op.	Rule
H300.M0.CS.1.1	Space to M0 [width = 0.020 μm] in MINP direction [same color, PRL > -0.124 μm , INSIDE {{FB_8 OR BV_FBFB [width = 0.150/0.300 μm]}} SIZING 0.124 μm in horizontal direction] (Except following conditions: 1. {DM0_DO1 OR DM0_DO2} space to M0 [width = 0.020 μm] \geq 0.120 μm , PRL > -0.124 μm)	SM	=	0.0600, 0.0620, 0.0640, 0.0660, 0.1200, \geq 0.1400
H300.M0.CS.1.3	Space of M0 [width = 0.080 μm with edge length > 0.060 μm in NMNP direction] to M0 [width = 0.020 μm] in MINP direction [same color, PRL > -0.060 μm , INSIDE {{FB_8 OR BV_FBFB [width = 0.150/0.300 μm]}} SIZING 0.060 μm in horizontal direction]	SM	=	0.0600, \geq 0.1200
H300.CM0A.S.1.1	Space of long side of CM0A [PRL > -0.079 μm , INSIDE {FB_8 NOT {CCP_8 SIZING -0.010 μm } }] (Except BCM0H)	S1A	\geq	0.0840
H300.CM0A.S.2	Space of short side of CM0A [PRL > -0.044 μm , INSIDE FB_8] (Except following conditions: 1. short side space of CM0A [INTERACT BCM0VA] = 0.060 μm [PRL > -0.044 μm] inside CCP_8)	S2	\geq	0.1200
H300.CM0B.W.3	Width of CM0B_Group_8 in horizontal direction (Except PO_P63) Definition of CM0B_Checked: {CM0B [INTERACT CCP_8, length < 0.160 μm , space = 0.090 μm in horizontal direction, PRL > 0 μm]} Definition of CM0B_Group_8: { {{{{{short side of CM0B_Checked}}} INTERACT CCP_8}} expanding edge 0.070 μm in vertical direction} OR CM0B_Checked } SIZING up/down 0.017 μm in horizontal direction} AND CCP_8}	W3	\leq	0.3090
H300.CM0B.W.3.1	Width of CM0B_Group_P63 in horizontal direction Definition of CM0B_Checked: {CM0B [INTERACT CCP_8, length < 0.160 μm , space = 0.102 μm in horizontal direction, PRL > 0 μm]} Definition of CM0B_Group_P63: { {{{{{short side of CM0B_Checked}}} INTERACT CCP_8}} expanding edge 0.070 μm in vertical direction} OR CM0B_Checked } SIZING up/down 0.0195 μm in horizontal direction} AND CCP_8}	W3	\leq	0.3390

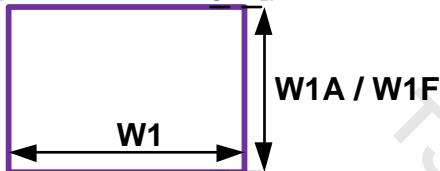
Rule No.	Description	Label	Op.	Rule
H300.CM0B.W.4	<p>Width of P855_CM0B_Checked_Group in horizontal direction (Except PO_P63)</p> <p>Definition of P855_CM0B_Checked_Group: $\{\{ \text{short side P855_CM0B_Checked [INTERACT CCP_8] SIZING } 0.070 \mu\text{m in vertical direction} \} \text{ SIZING up/down } 0.017 \mu\text{m in horizontal direction} \} \text{ AND CCP_8}$</p> <p>Definition of P855_CM0B_Checked: CM0B interact P855_Group_W</p> <p>Definition of P855_Space_W: Space region = $0.0615 \mu\text{m}$ in horizontal direction formed by $\{\text{CM0B NOT P855_CM0B_BCM0H}\} [\text{length} \geq 0.160 \mu\text{m}, \text{PRL} \geq 0.160 \mu\text{m}]$</p> <p>Definition of P855_Group_W: Length of $\{\text{P855_Space_W SIZING } 0.024 \mu\text{m in horizontal direction}\}$ in horizontal direction $\geq 0.195 \mu\text{m}$</p> <p>Definition of P855_CM0B_BCM0H Both vertical edge of $\{\text{CM0B [INTERACT BCM0H] SIZING up/down } 0.017 \mu\text{m in horizontal direction}\}$ space to CM0B = $0.0615 \mu\text{m}$ in horizontal direction with PRL $\geq 0.160 \mu\text{m}$</p>	W4	\leq	0.1950
H300.CM0B.W.4.1	<p>Width of P945_CM0B_Checked_Group in horizontal direction [INSIDE PO_P63]</p> <p>Definition of P945_CM0B_Checked_Group: $\{\{ \text{short side P945_CM0B_Checked [INTERACT CCP_8] SIZING } 0.070 \mu\text{m in vertical direction} \} \text{ SIZING up/down } 0.0195 \mu\text{m in horizontal direction} \} \text{ AND CCP_8}$</p> <p>Definition of P945_CM0B_Checked: CM0B interact P945_Group_W</p> <p>Definition of P945_Space_W: Space region = $0.0705 \mu\text{m}$ in horizontal direction formed by $\{\text{CM0B NOT P945_CM0B_BCM0H}\} [\text{length} \geq 0.160 \mu\text{m}, \text{PRL} \geq 0.160 \mu\text{m}]$</p> <p>Definition of P945_Group_W: Length of $\{\text{P945_Space_W SIZING } 0.024 \mu\text{m in horizontal direction}\}$ in horizontal direction $\geq 0.213 \mu\text{m}$</p> <p>Definition of P945_CM0B_BCM0H Both vertical edge of $\{\text{CM0B [INTERACT BCM0H] SIZING up/down } 0.0195 \mu\text{m in horizontal direction}\}$ space to CM0B = $0.0705 \mu\text{m}$ in horizontal direction with PRL $\geq 0.160 \mu\text{m}$</p>	W4A	\leq	0.2130
H300.CM0B.S.1.1	Space of long side of CM0B [PRL > -0.079 μm , INSIDE {FB_8 NOT {CCP_8 SIZING -0.010 $\mu\text{m}\}}}] (Except BCM0H, PO_P63)$	S1A	=	0.0615, 0.0840, 0.0900, 0.0960, 0.1110, ≥ 0.1160
H300.CM0B.S.1.2	Space of long side of CM0B [PRL > -0.079 μm , INSIDE {FB_8 [INTERACT PO_P63] NOT {CCP_8 SIZING -0.010 $\mu\text{m}\}}}] (Except BCM0H)$	S1B	\geq	0.0705
H300.CM0B.S.2	Space of short side of CM0B [PRL > -0.056 μm , INSIDE FB_8] (Except following conditions: 1. short side space of CM0B [INTERACT BCM0VB] = $0.060 \mu\text{m}$ [PRL > -0.056 μm] inside CCP_8)	S2	\geq	0.1200

Rule No.	Description	Label	Op.	Rule
H300.VIA0.EN.22	Short side enclosure of rectangular VIA0 by M0_NOT_CM0 [width = 0.080 μm] with the other two long side enclosure \geq 0.030 μm [INSIDE CCP_8]	EN22	\geq	0.0600
H300.VIA0.EN.22.1	Short side enclosure of rectangular VIA0 by M0_NOT_CM0 [width = 0.080 μm] with the other two long side enclosure \geq 0.060 μm [INSIDE CCP_8]	EN22A	\geq	0.0150

TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

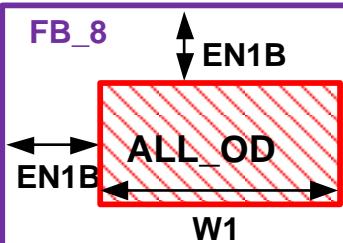
H300-FB

{FB_8 OR BV_FBF
[width = 0.300 μm]}



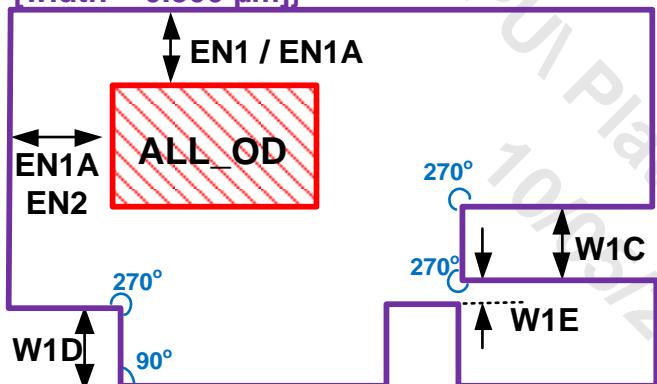
H300.FB.W.1 /
H300.FB.W.1.1 /
H300.FB.W.1.6®

PO_P63



H300.FB.W.1.0.1 / H300.FB.EN.1.2

{FB_8 OR BV_FBF
[width = 0.300 μm]}



H300.FB.W.1.3 / H300.FB.W.1.4 /
H300.FB.W.1.5 / H300.FB.EN.1 /
H300.FB.EN.1.1 / H300.FB.EN.2

FB_8

EN5

CCP_8

EN5

H300.FB.EN.5

FB_8

EN6

TPO, VT, PP, NP

EN6

H300.FB.EN.6

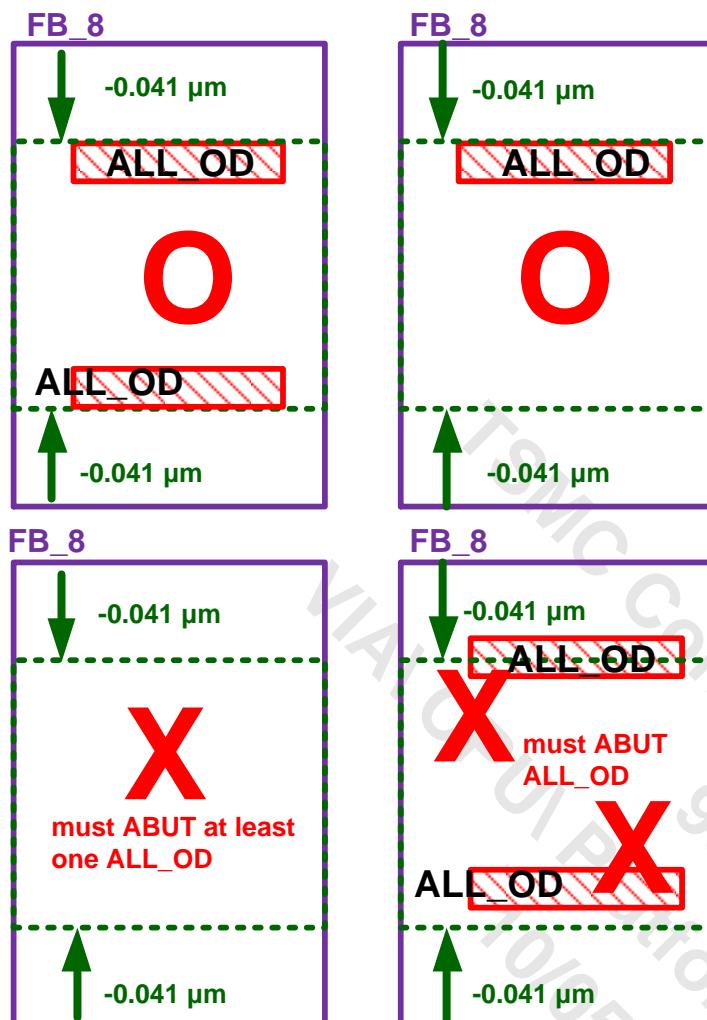
prBoundary

EN7

FB_8

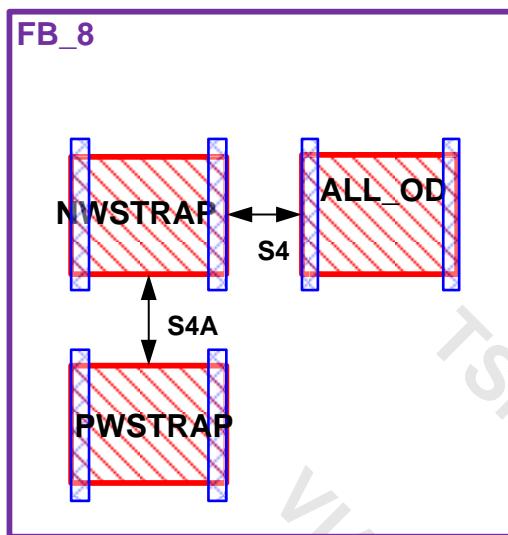
EN7

H300.FB.EN.7

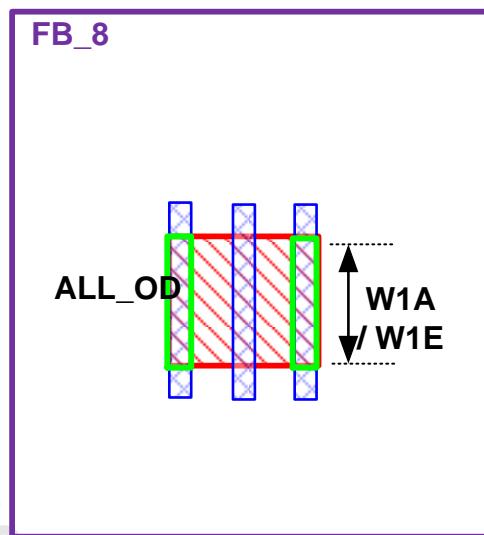


H300.FB.R.11

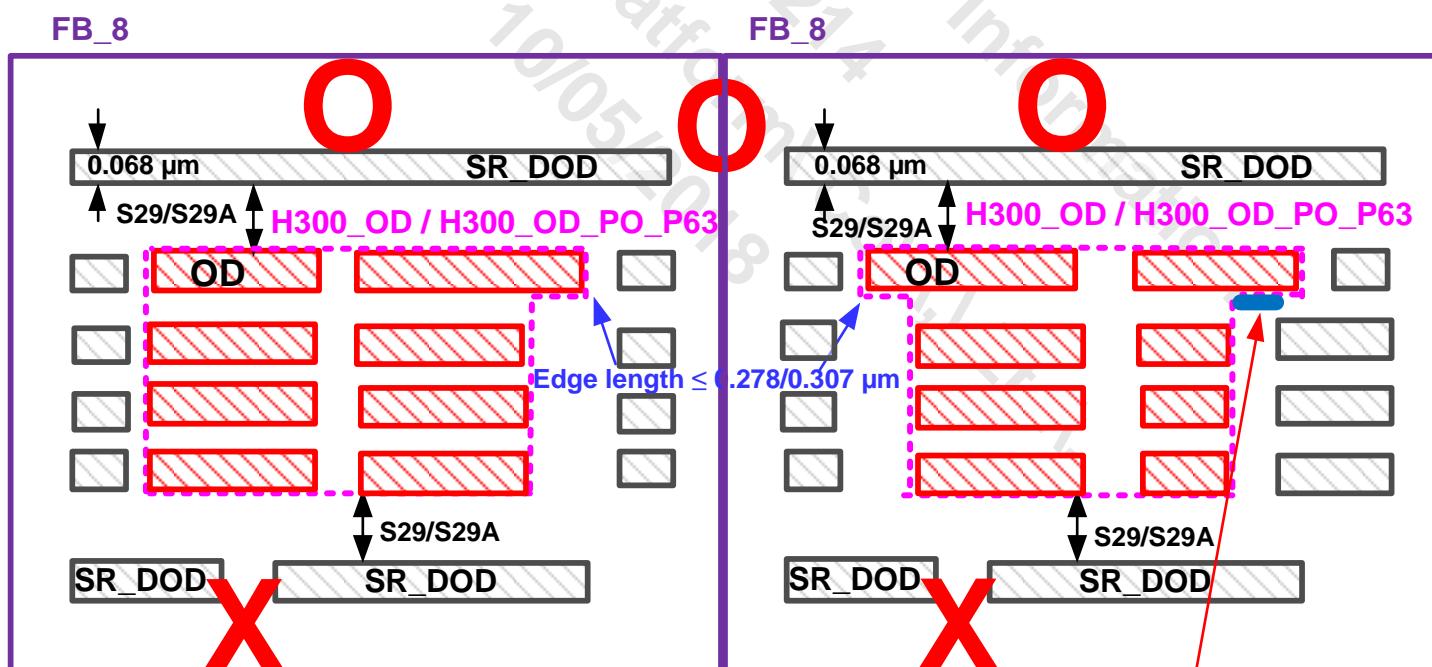
H300-OD



H300.OD.S.4 / H300.OD.S.4.1

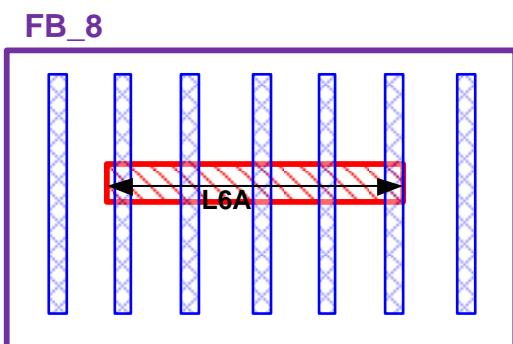


H300.OD.W.1.1 / H300.OD.W.1.5 /

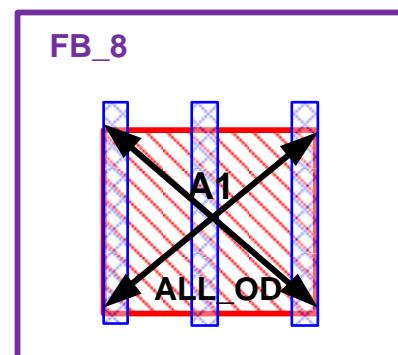


violation length $\leq 0.278/0.307 \mu\text{m}$ and
interact H300_OD/H300_OD_PO_P63
concave corner

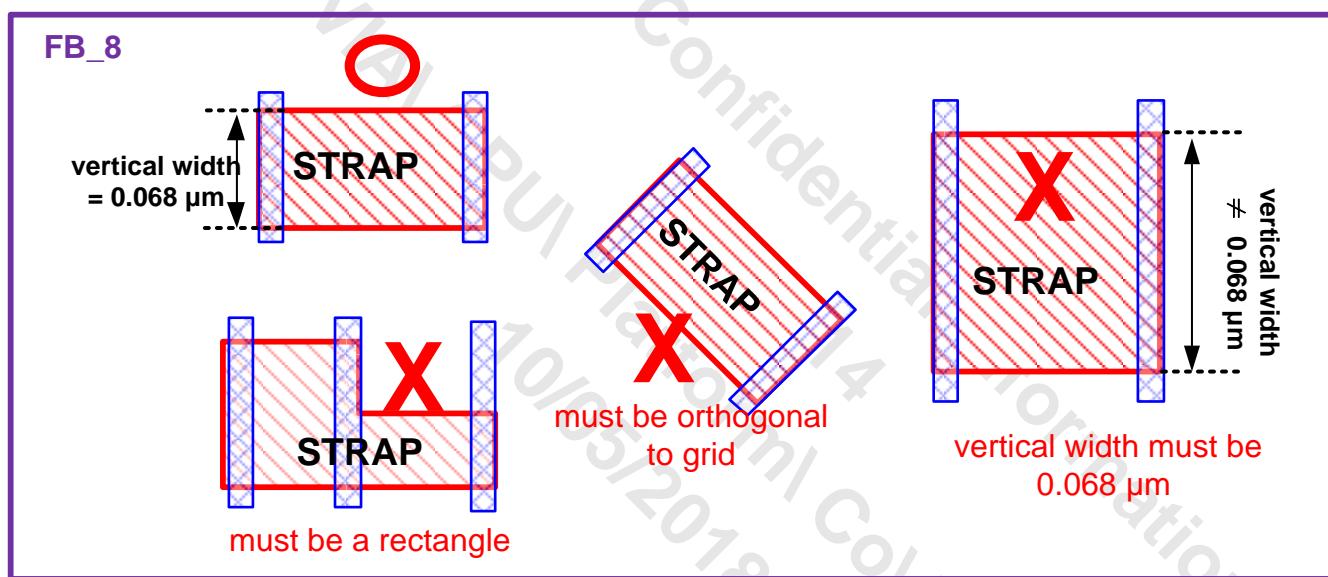
H300.OD.S.29 / H300.OD.S.29.1



H300.OD.L.6.1

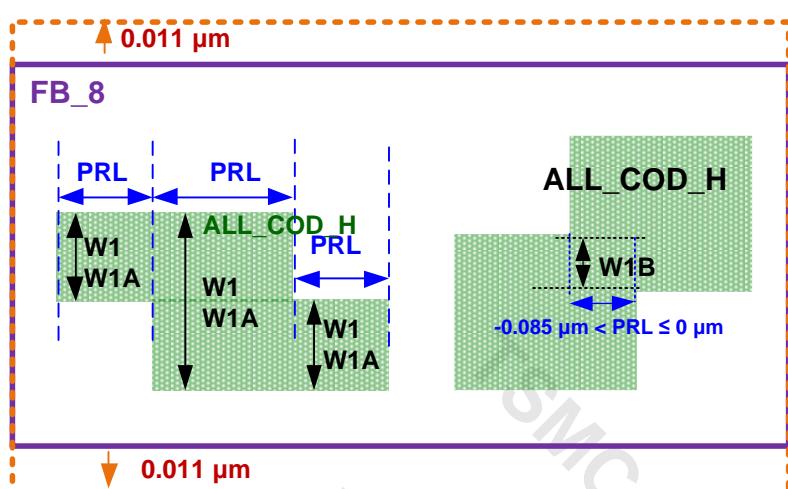


H300.OD.A.1

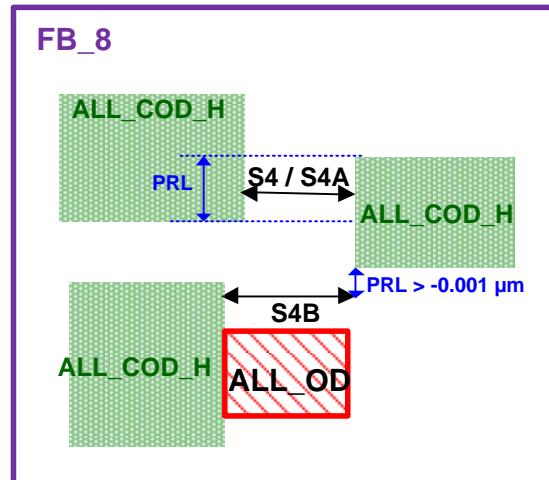


H300.OD.R.8

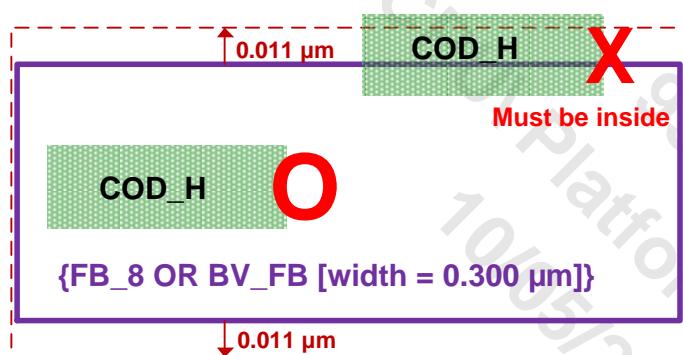
H300-COD



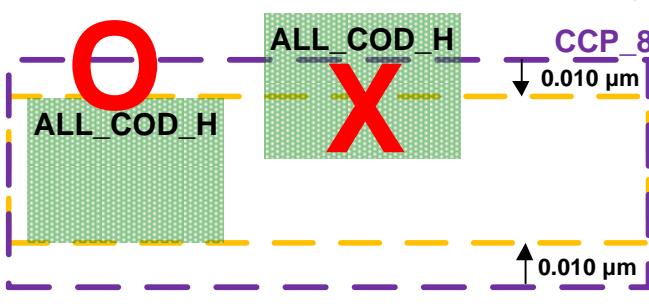
H300.COD_H.W.1
H300.COD_H.W.1.1
H300.COD_H.W.1.2



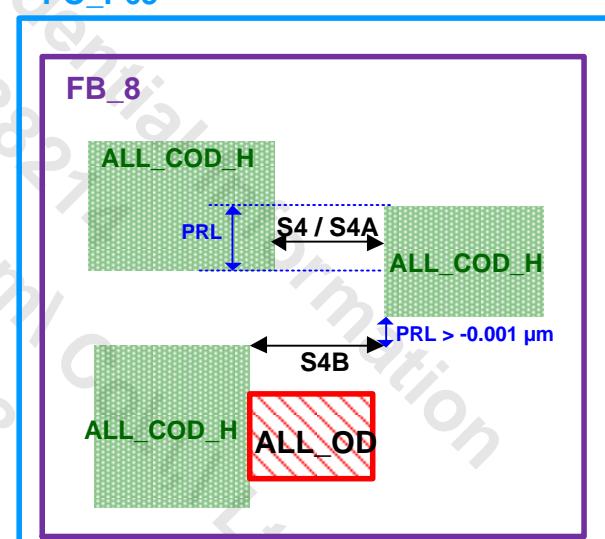
H300.COD_H.S.4
H300.COD_H.S.4.1
H300.COD_H.S.4.2



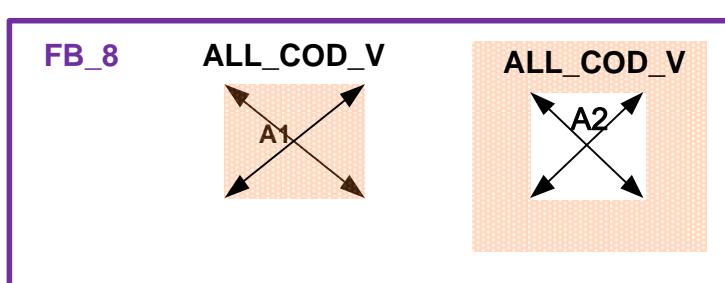
H300.COD_H.R.10



H300.COD_H.R.12

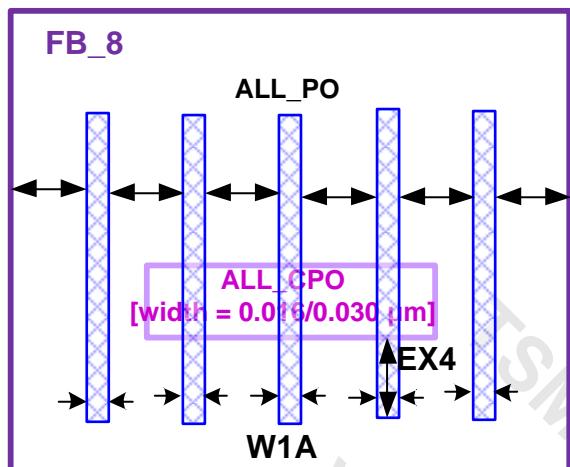


H300.COD_H.S.4.0.1 /
H300.COD_H.S.4.1.1 /
H300.COD_H.S.4.2.1

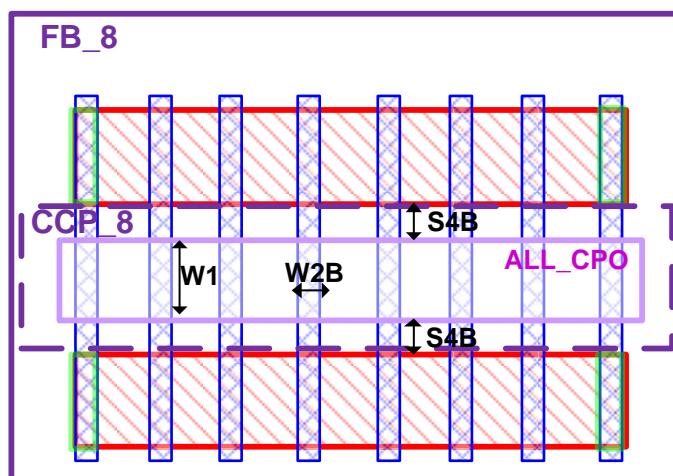
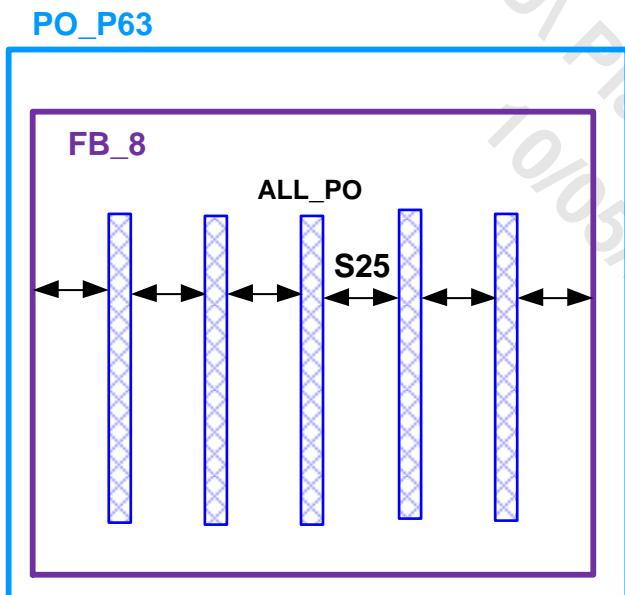


H300.COD_V.A.1 / H300.COD_V.A.2

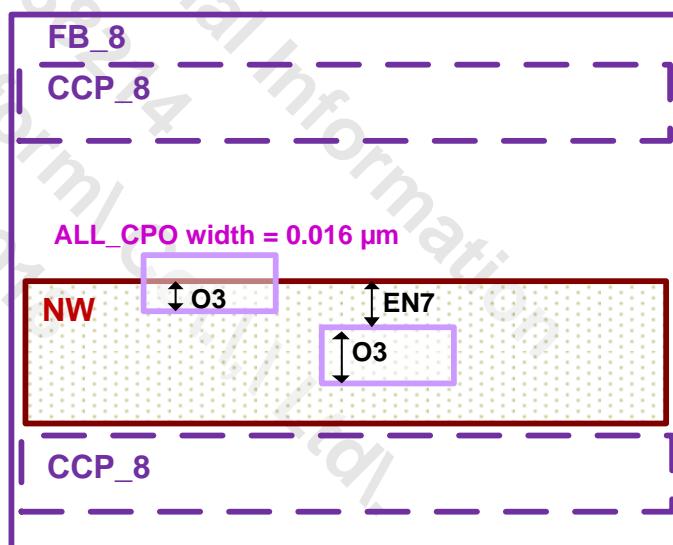
H300-PO/CPO



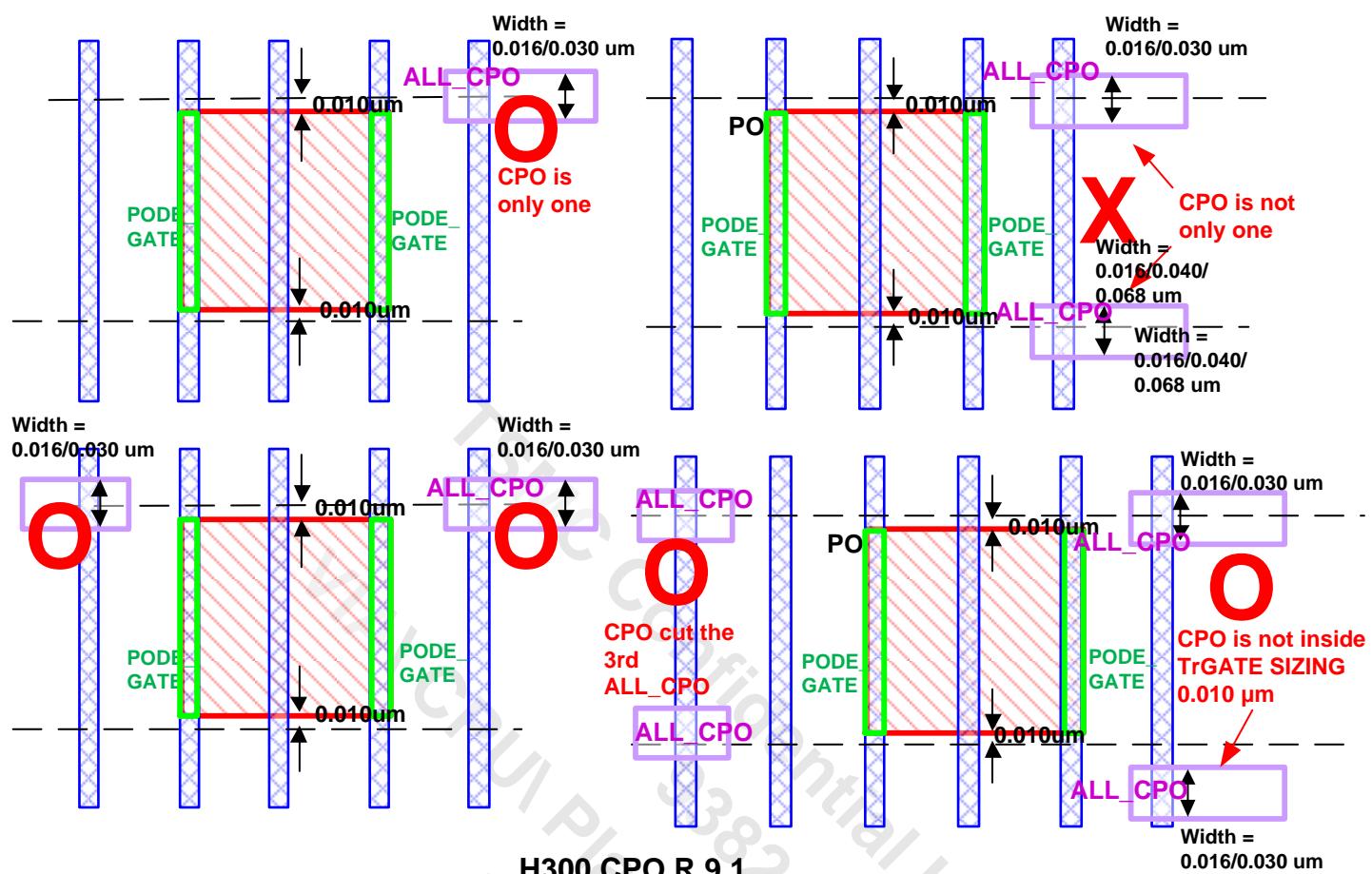
H300.PO.W.1.1 / H300.CPO.EX.4

H300.CPO.W.1 / H300.CPO.W.2.2 /
H300.CPO.S.4.2

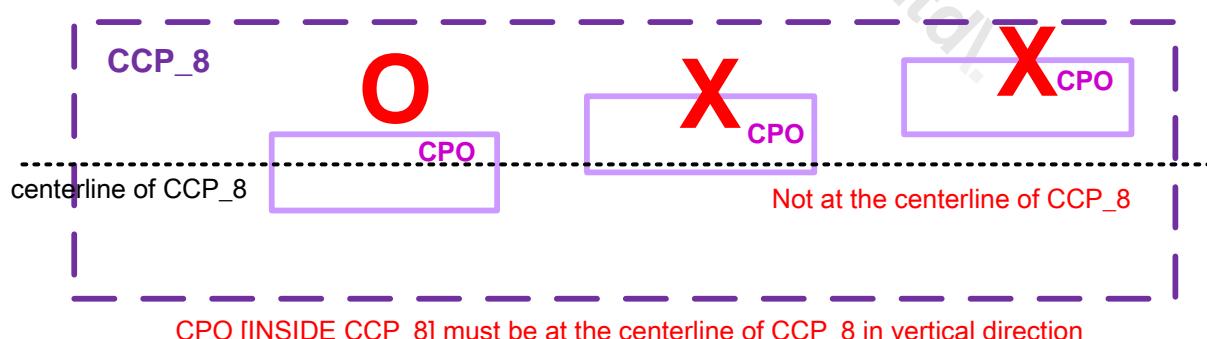
H300.PO.S.25.5 / H300.PO.S.25.5.1



H300.CPO.EN.7 / H300.CPO.O.3



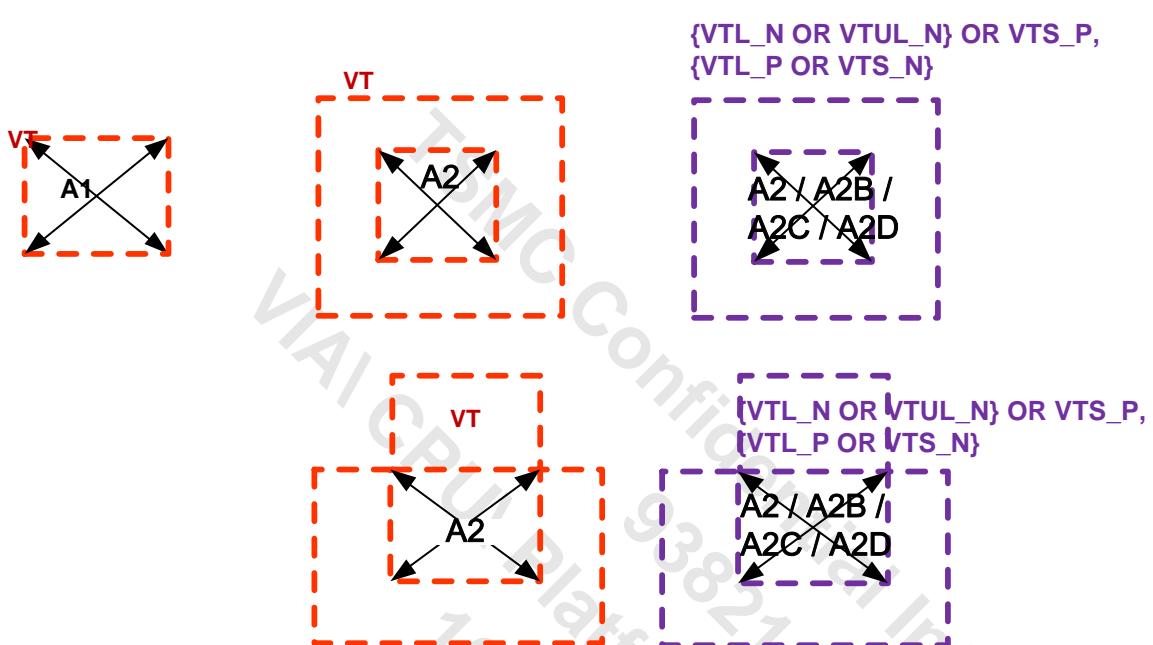
H300.CPO.R.9.1



H300.CPO.R.12

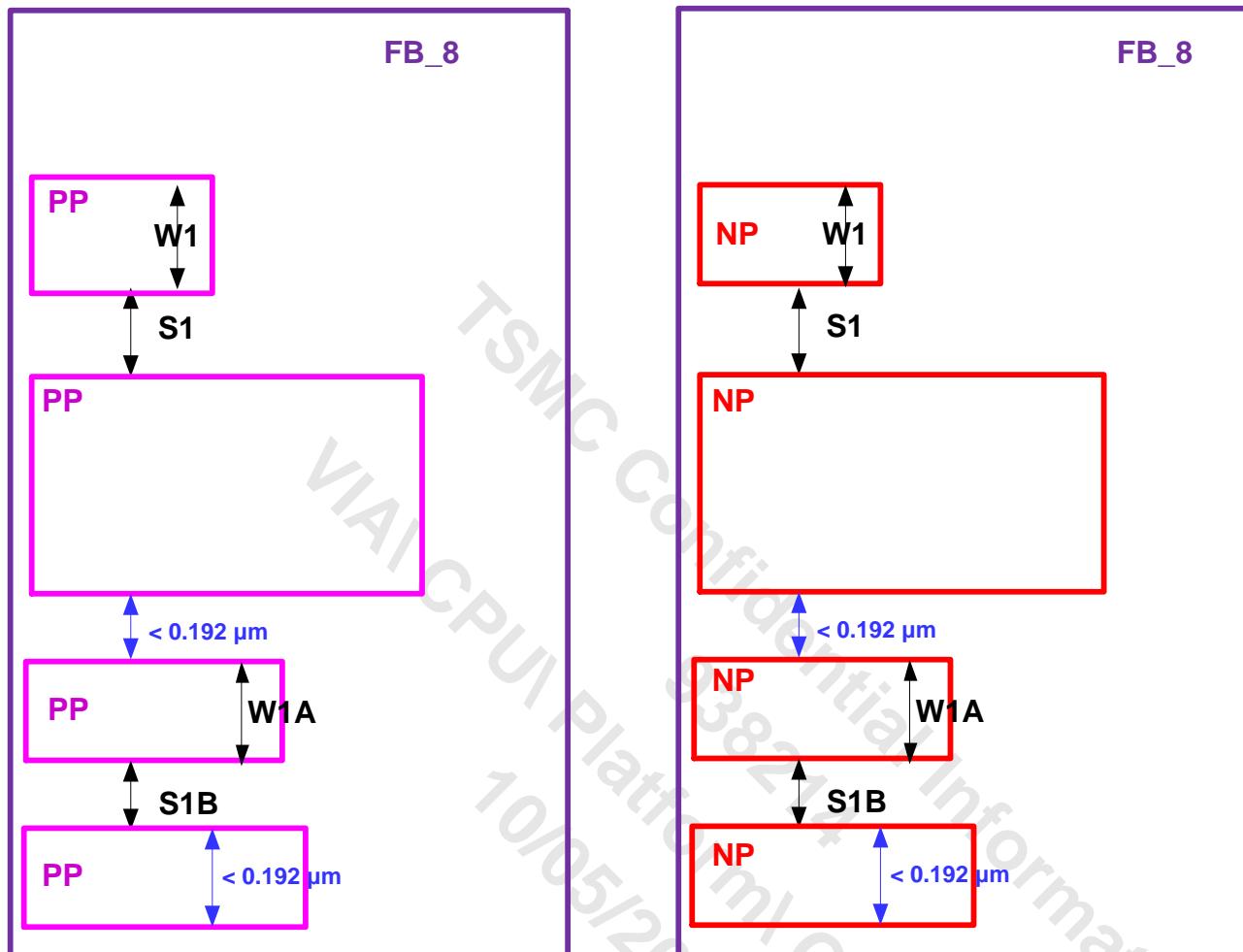
H300-VT

FB_8



H300.VT.A.1 / H300.VT.A.2 / H300.VT.A.2.2 / H300.VT.A.2.4 /
H300.VT.A.3

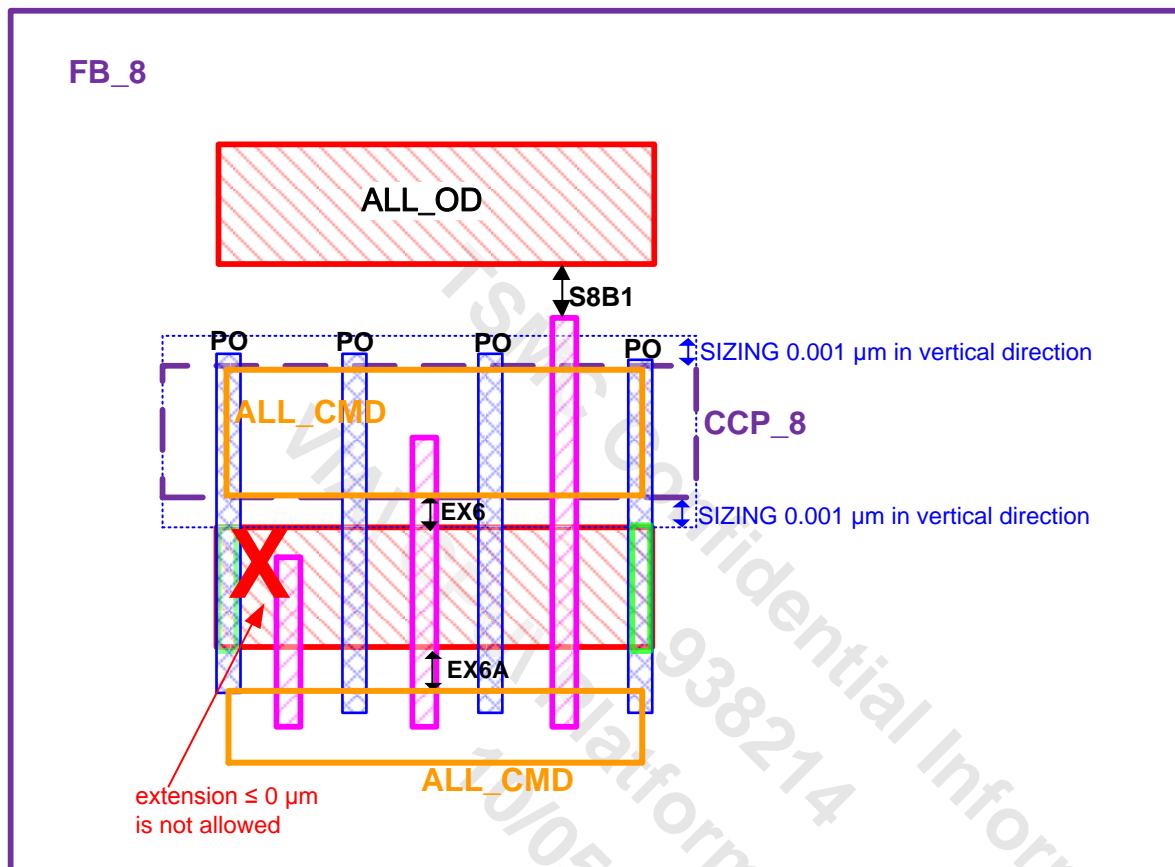
H300-PP/NP



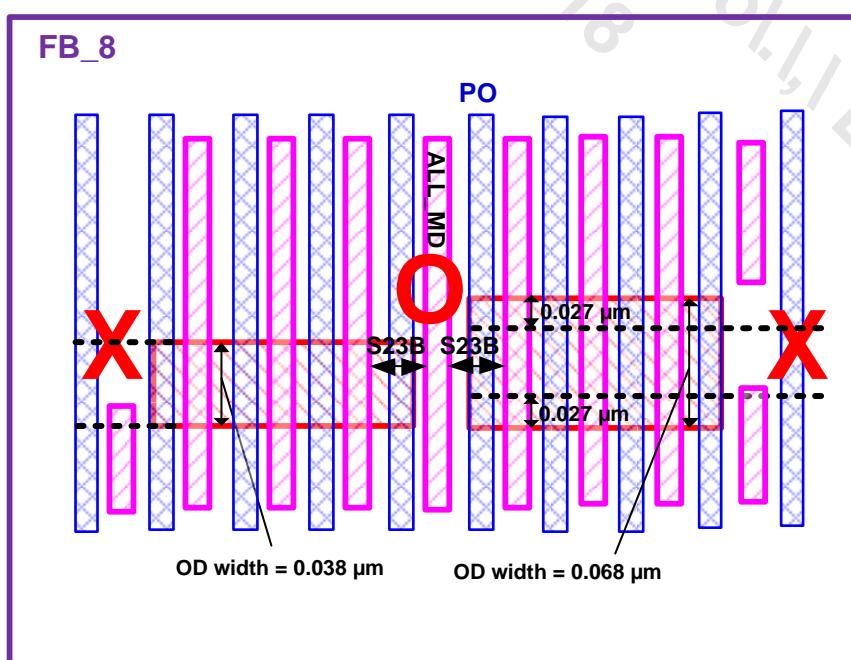
H300.PP.W.1 / H300.PP.W.1.1 /
H300.PP.S.1 / H300.PP.S.1.2

H300.NP.W.1 / H300.NP.W.1.1 /
H300.NP.S.1 / H300.NP.S.1.2

H300-MD

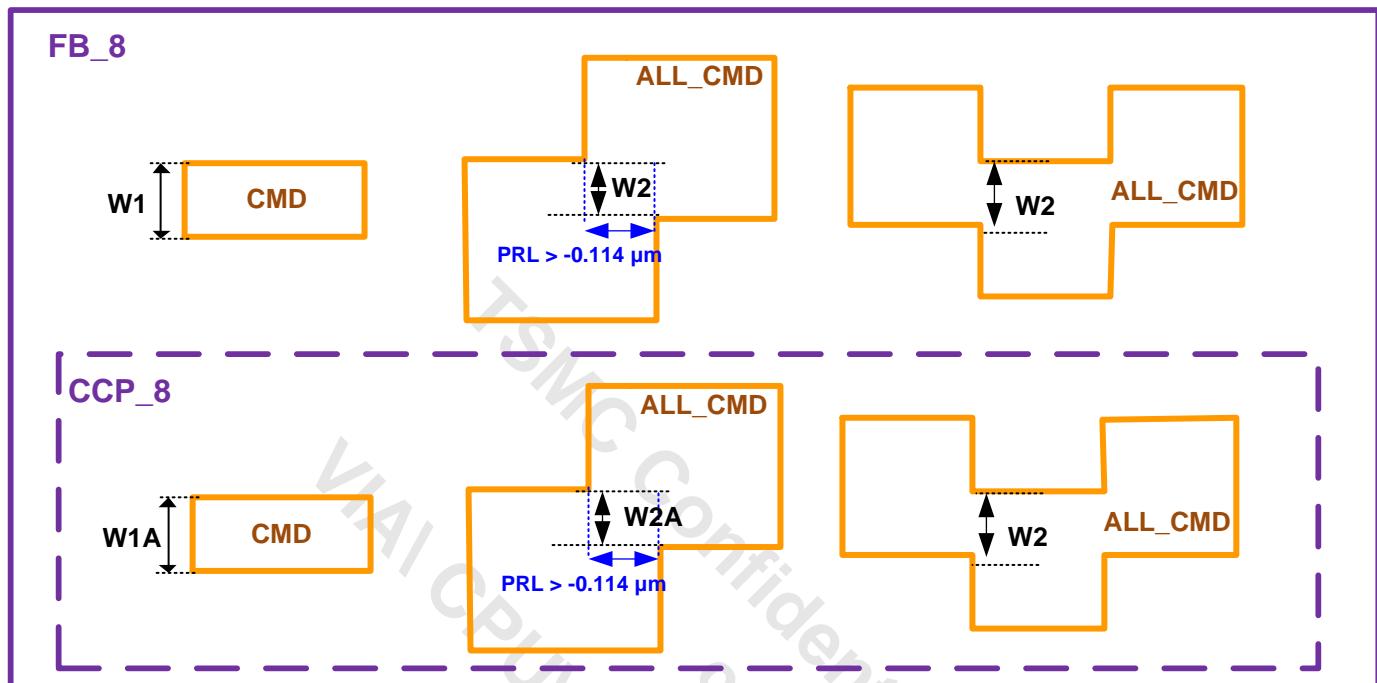


H300.MD.S.8.2.1 / H300.MD.EX.6 / H300.MD.EX.6.1

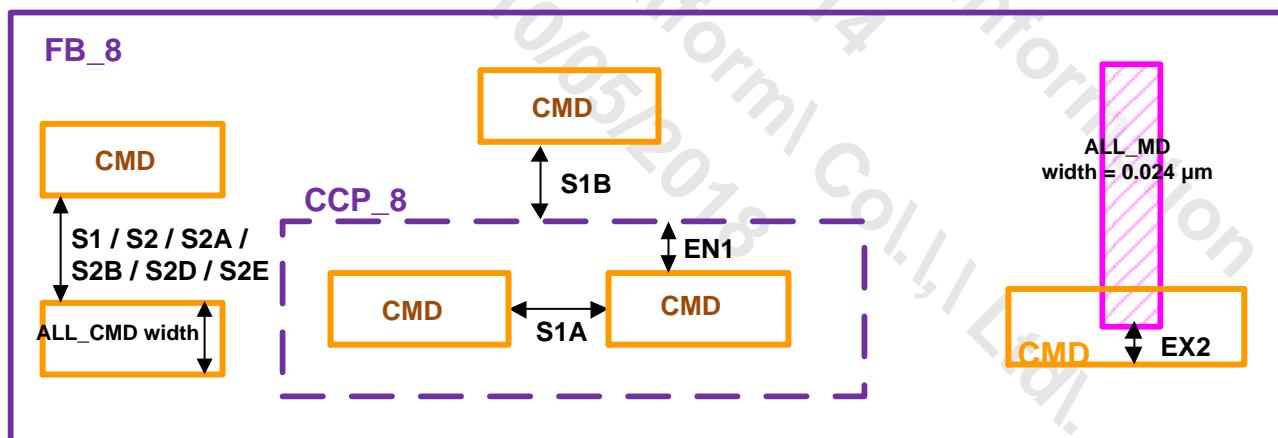


H300.MD.S.23.2 / H300.MD.S.23.2.1

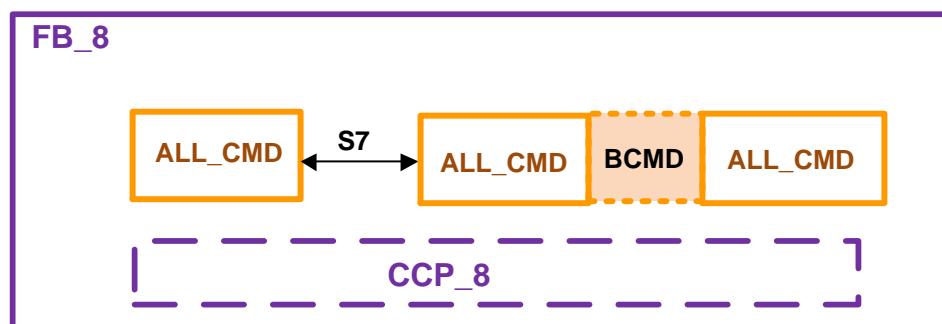
H300-CMD



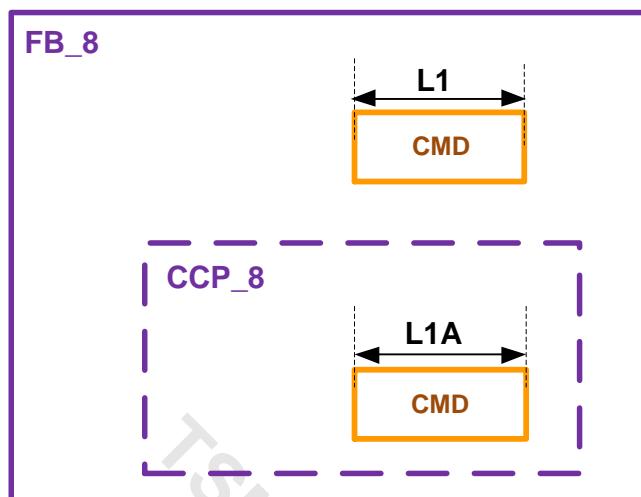
**H300.CMD.W.1 / H300.CMD.W.1.1 /
H300.CMD.W.2 / H300.CMD.W.2.1**



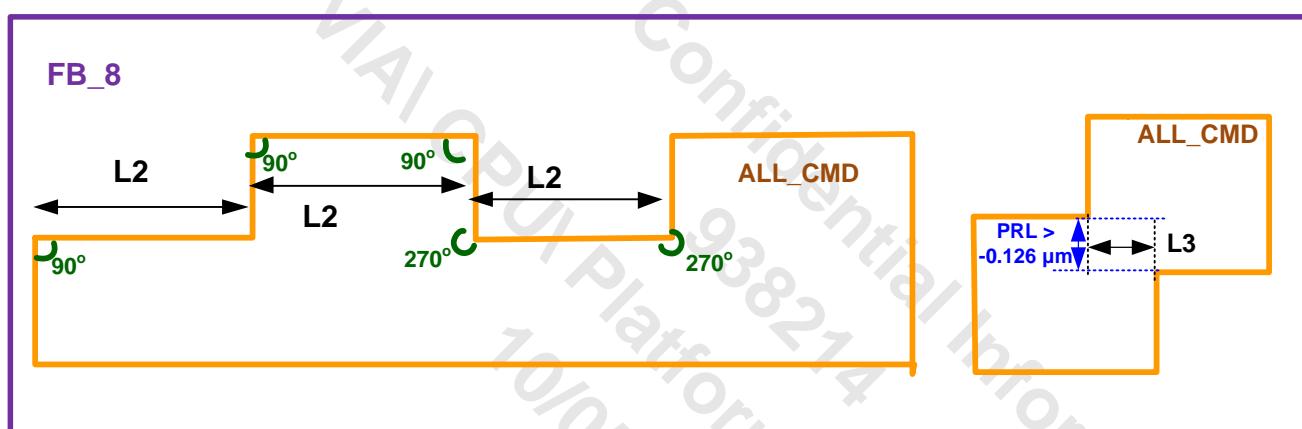
H300.CMD.S.1 / H300.CMD.S.1.1 / H300.CMD.S.1.1.1 / H300.CMD.S.1.2 /
H300.CMD.S.2 / H300.CMD.S.2.1 / H300.CMD.S.2.2 / H300.CMD.S.2.4 /
H300.CMD.S.2.5 / H300.CMD.EN.1 / H300.CMD.EX.2



H300.CMD.S.7



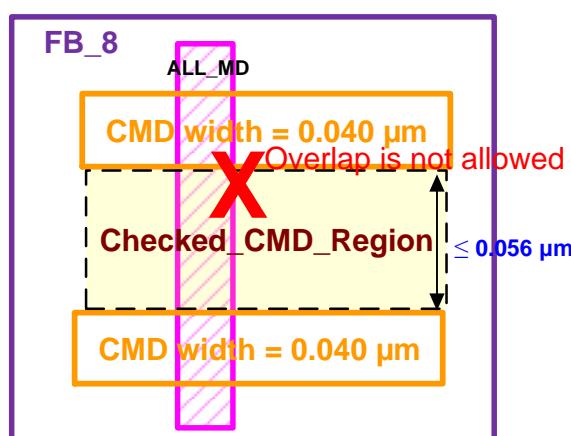
H300.CMD.L.1 / H300.CMD.L.1.1 /
H300.CMD.L.1.1.1



H300.CMD.L.2 / H300.CMD.L.2.1 /
H300.CMD.L.3 / H300.CMD.L.3.1

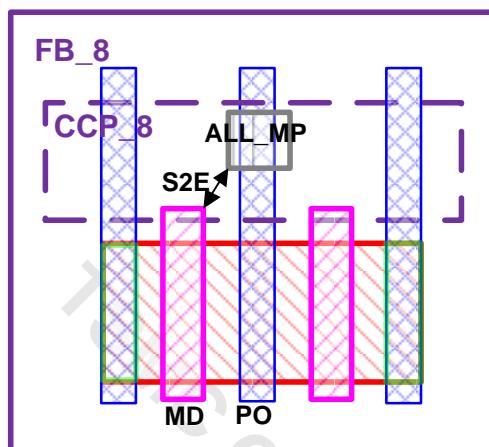


H300.CMD.R.6.3

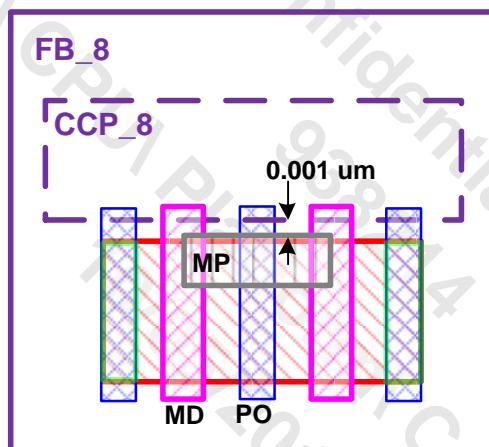


H300.CMD.R.10

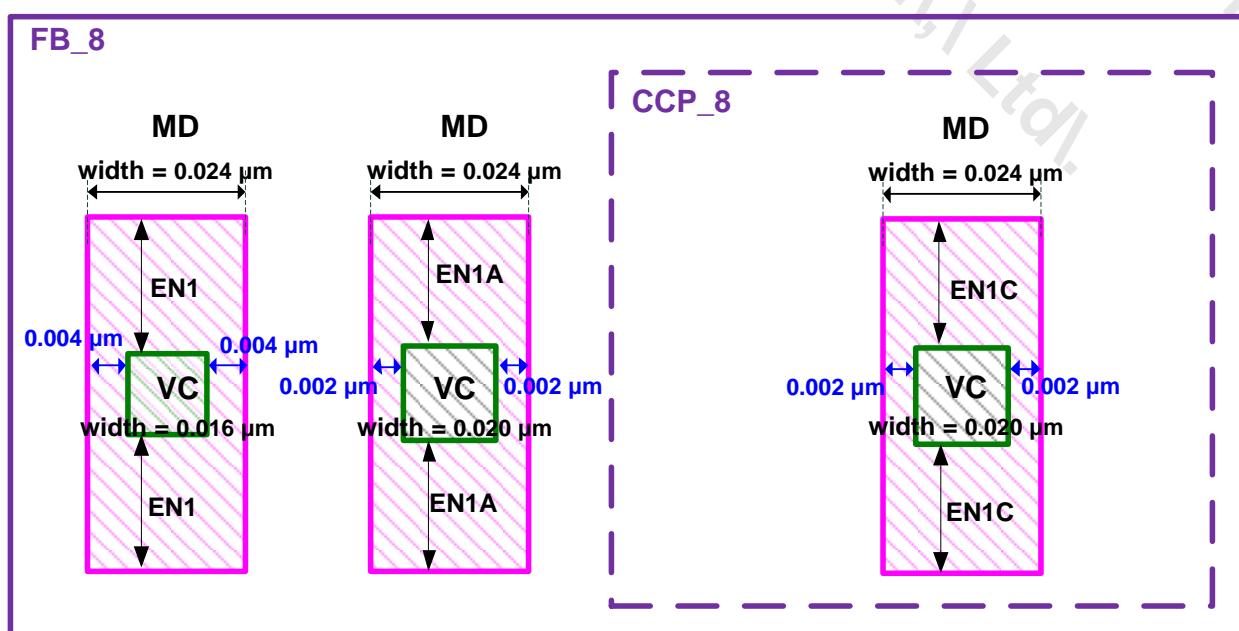
H300-MP/VC



H300.MP.S.2.5

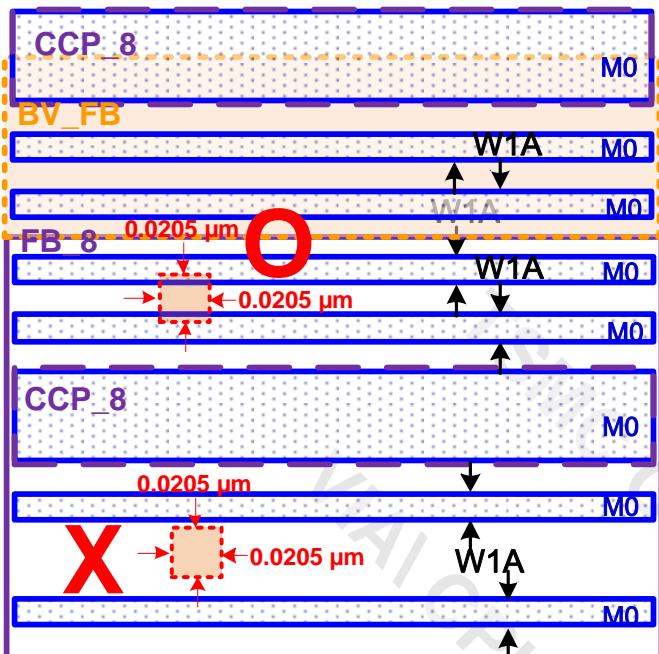


H300.MP.R.9

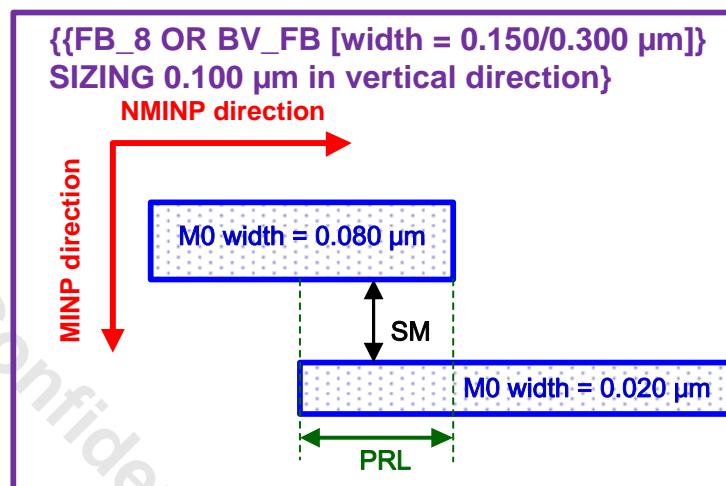


H300.VC.EN.1 / H300.VC.EN.1.1 / H300.VC.EN.1.3

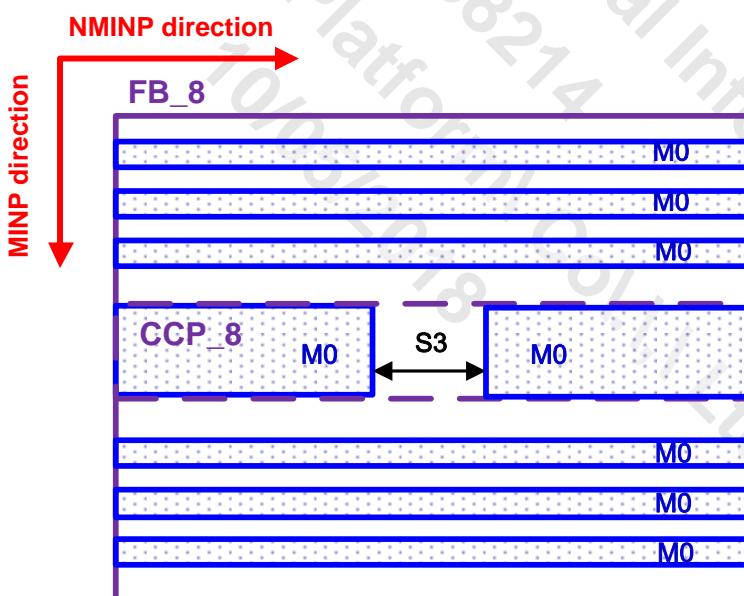
H300-M0/CM0



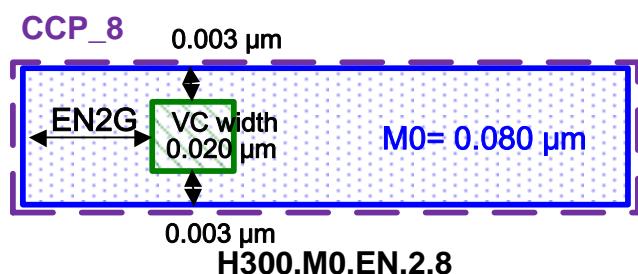
H300.M0.W.1.1 / H300.M0.S.19



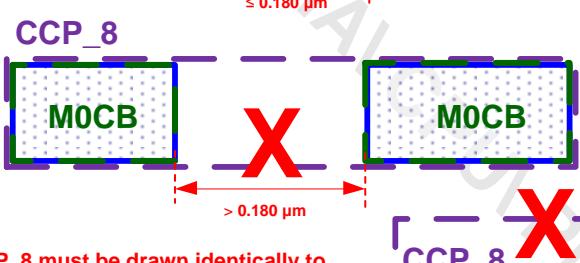
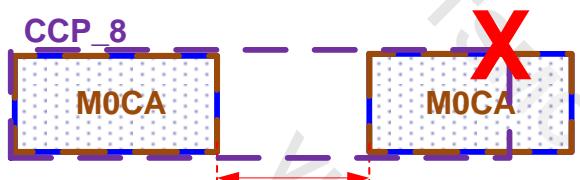
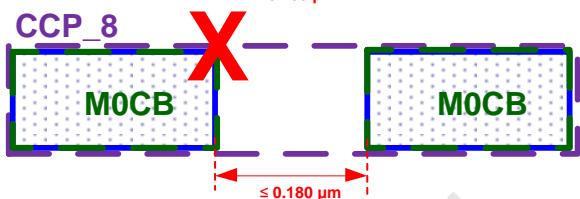
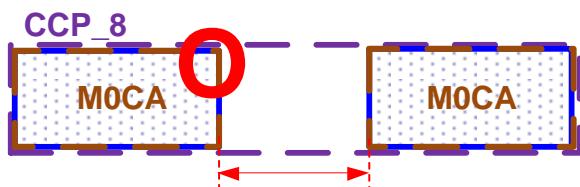
H300.M0.S.2.3.1



H300.M0.S.3

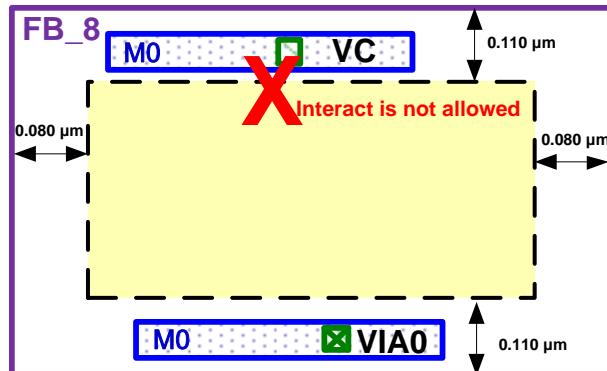


H300.M0.EN.2.8



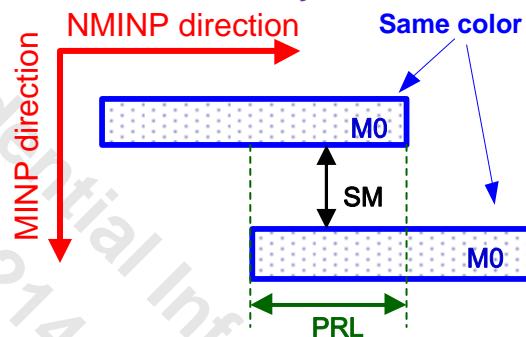
CCP_8 must be drawn identically to
{M0CA [INTERACT {FB_8 OR BV_FBFB}]
SIZING up/down 0.090 μm in
horizontal direction}

H300.M0.R.15.1



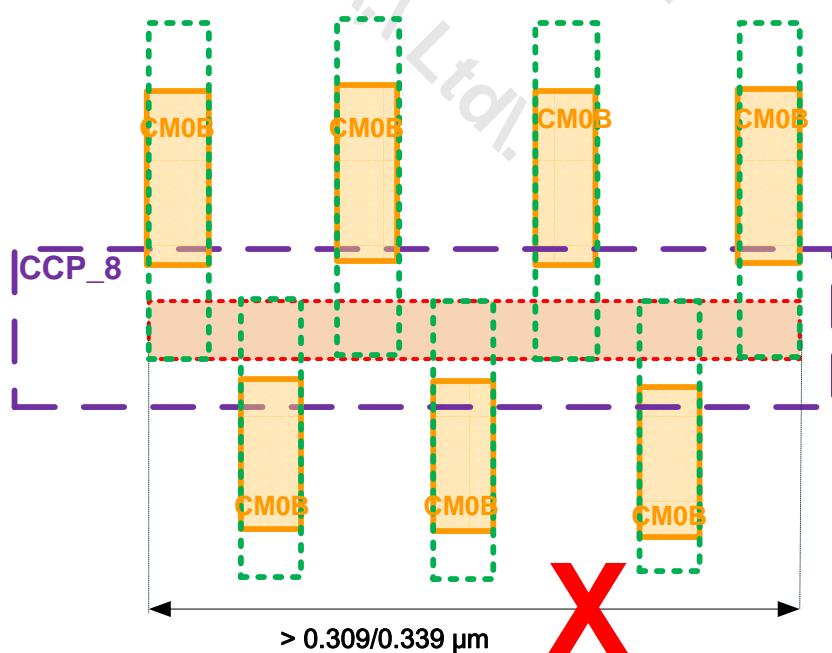
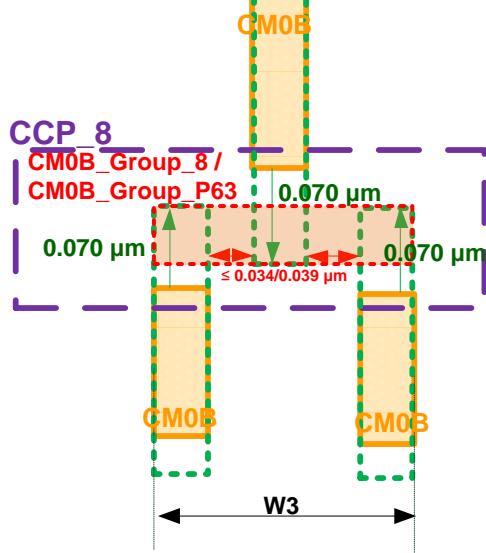
H300.M0.R.20

{ {FB_8 OR BV_FBFB} [width =
0.150/0.300 μm] SIZING 0.124 μm in
horizontal direction }

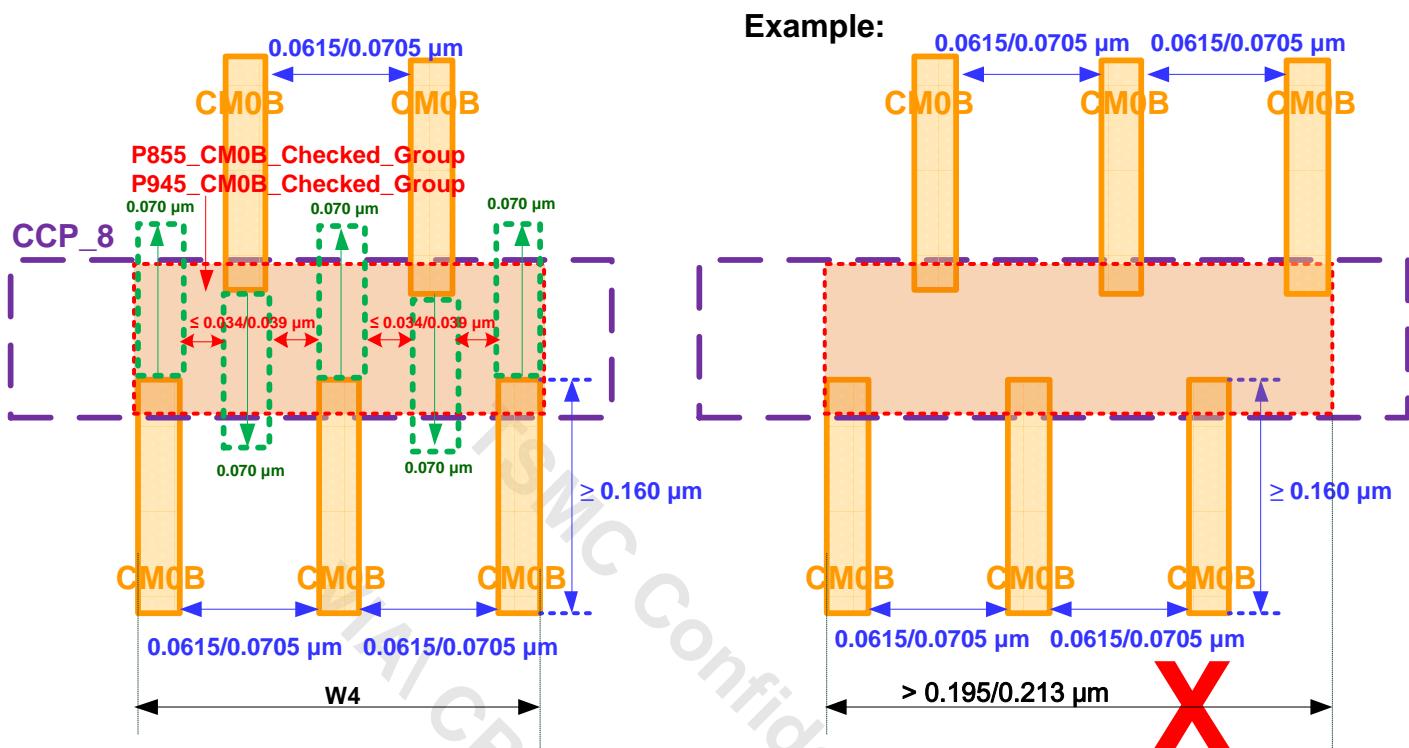


H300.M0.CS.1.1 / H300.M0.CS.1.3

Example:



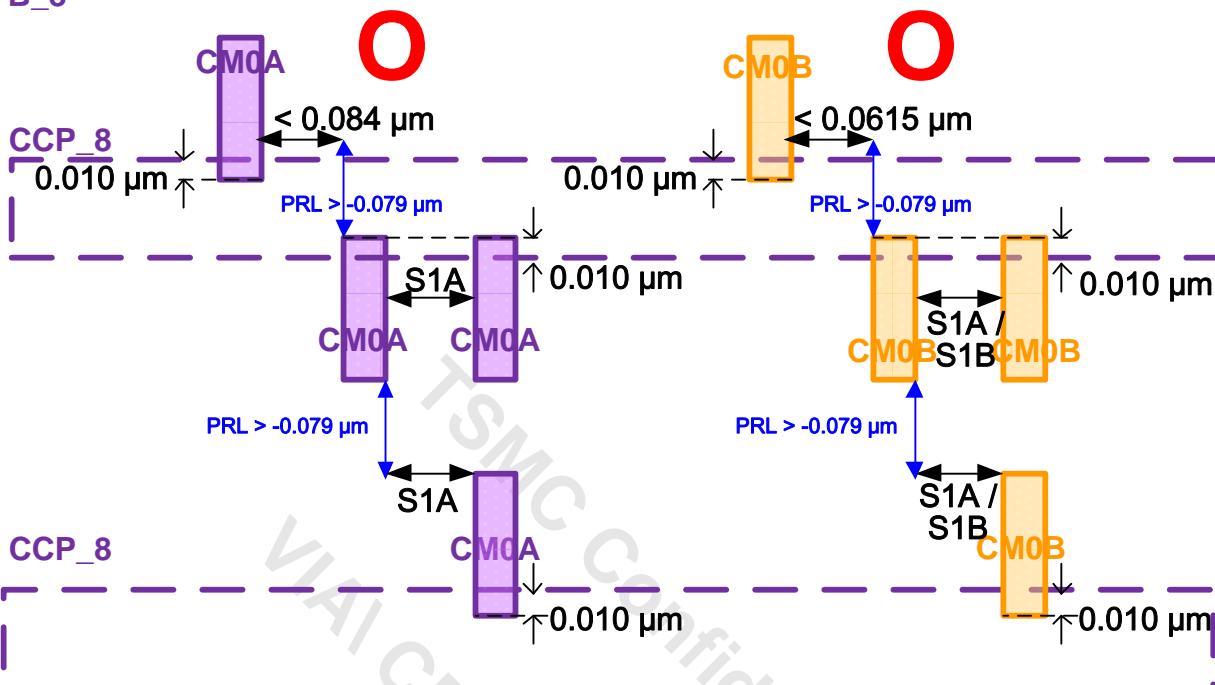
H300.CM0B.W.3 / H300.CM0B.W.3.1

**Example:**

The diagram shows a valid CM0B contact pattern. It consists of five vertical orange bars labeled 'CM0B'. The first two bars have a gap of $0.0615/0.0705 \mu\text{m}$. The next two bars are grouped together under a yellow dashed box labeled 'BCM0H' with a gap of $0.0615/0.0705 \mu\text{m}$. The final bar has a gap of $0.0615/0.0705 \mu\text{m}$ from the previous bar. The total width of the CCP_8 layer is indicated as $\geq 0.160 \mu\text{m}$. The total width of the pattern is labeled as $> 0.195/0.213 \mu\text{m}$, which is marked with a red circle.

H300.CM0B.W.4 / H300.CM0B.W.4.1

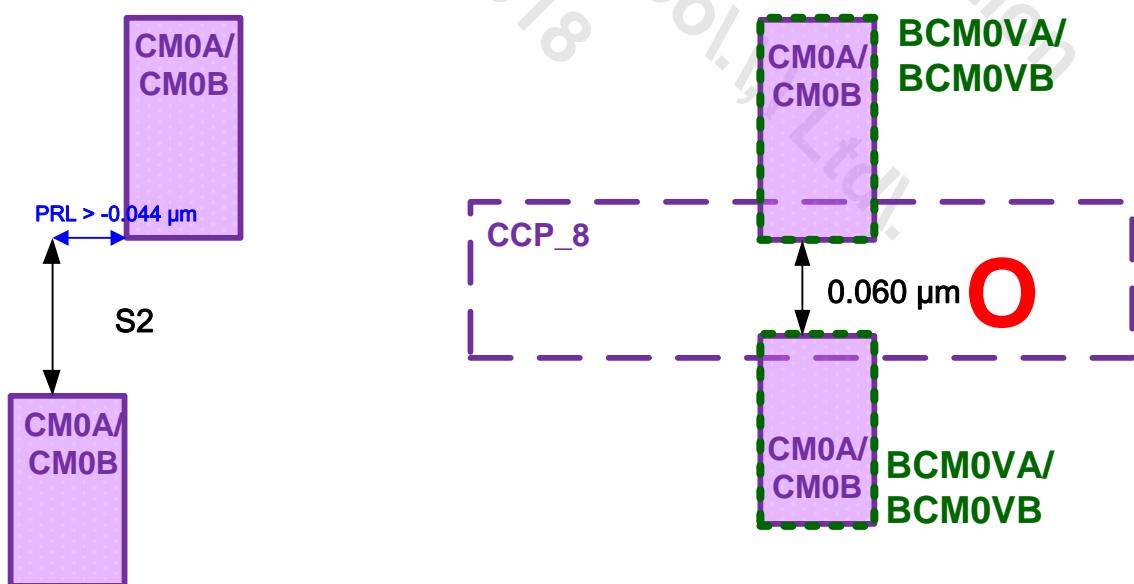
FB_8



H300.CM0A.S.1.1 /
H300.CM0B.S.1.1 / H300.CM0B.S.1.2

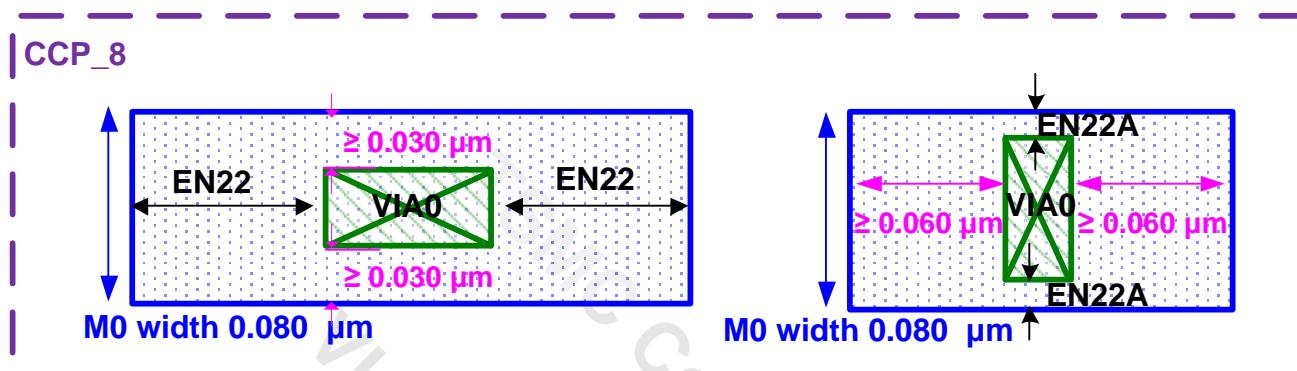
FB_8

Except short side space of CM0A [INTERACT
BCM0VA] = 0.060 μm inside CCP_8



H300.CM0A.S.2 / H300.CM0B.S.2

H300-VIA0



H300.VIA0.EN.22 / H300.VIA0.EN.22.1

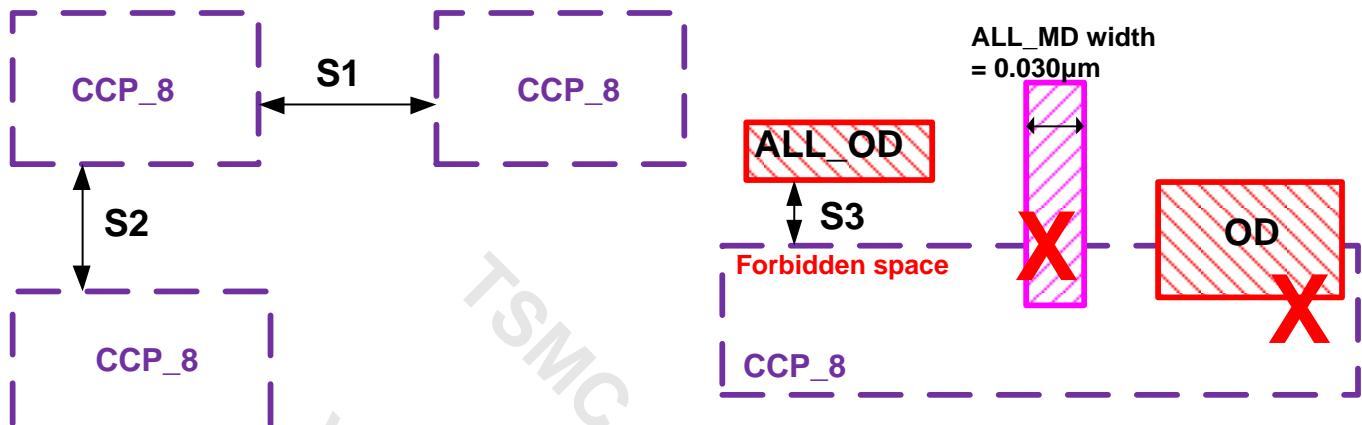
4.5.13.4.1 H300 Confined Compact Pattern (CCP) Layout Rules for Power Rail

CCP_8 (CAD layer: 98;8) is used to define Confined Compact Pattern inside FB_8.

Rule No.	Description	Label	Op.	Rule
H300.CCP.S.1	Space	S1	\geq	0.1800
H300.CCP.S.2	Space in vertical direction [INSIDE {FB_8 OR BV_FB [width = 0.150/0.300 $\mu\text{m}】}]$	S2	=	0.2200
H300.CCP.S.3	Forbidden space of CCP_8 to ALL_OD in vertical direction	S3	=	0.0310
H300.CCP.R.1	Confined Compact Pattern 8 (CCP_8) must be a rectangle [width = 0.080 μm , length \geq 0.400 μm] and coincident to M0CA or M0CB			
H300.CCP.R.1.1	{CCP_8 AND FB_8} must interact ALL_MD [width = 0.024 μm], and overlap ALL_MD [width = 0.024 μm] must be 0.080 μm in vertical direction			
H300.CCP.R.1.3	CCP_8 [INTERACT VC width = 0.016 μm] interact VC [width = 0.020 μm] is not allowed			
H300.CCP.R.2	CCP_8 overlap ALL_MD [width = 0.030 μm] or OD is not allowed (Except HEADER_8)			
H300.CCP.R.3	FB_8 must interact CCP_8			
H300.CCP.R.4	CCP_8 must be inside {FB_8 OR {BV_FB [width = 0.150/0.300 μm] SIZING 0.150 μm in vertical direction}}			

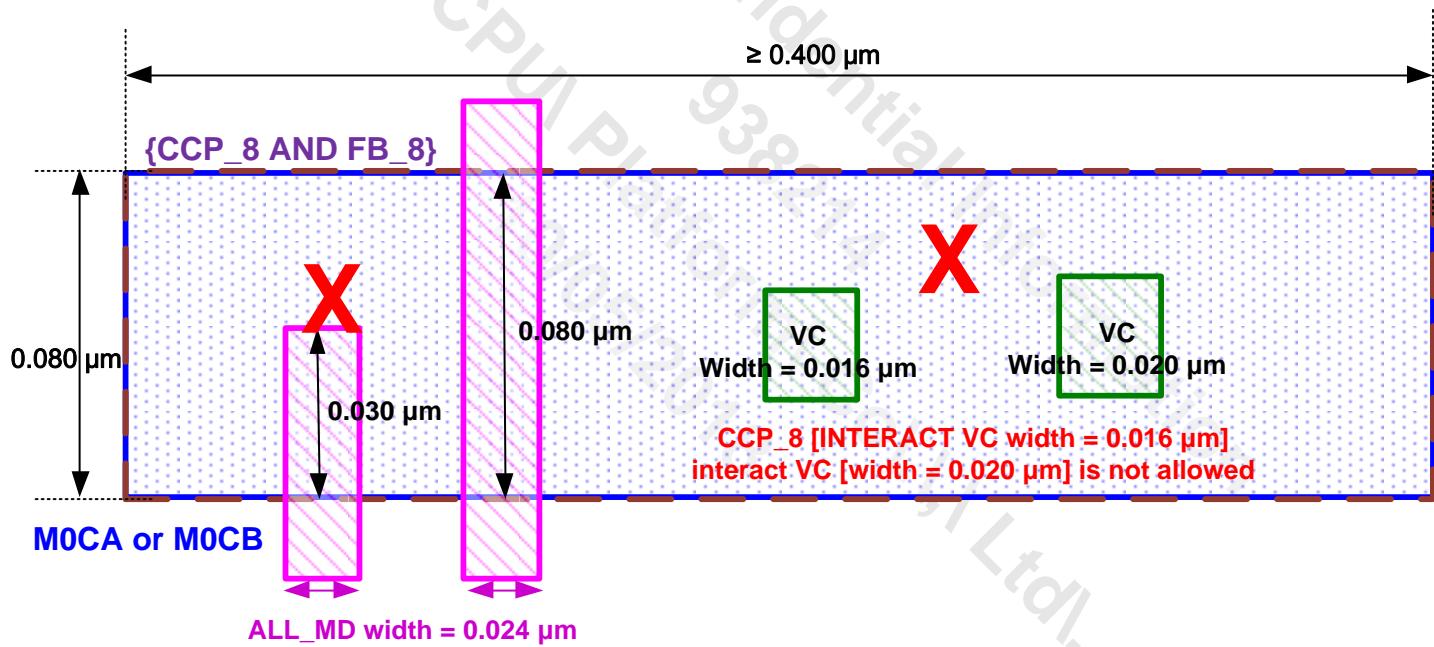
TSMC Confidential Information 938214
10/05/2018

H300-CCP

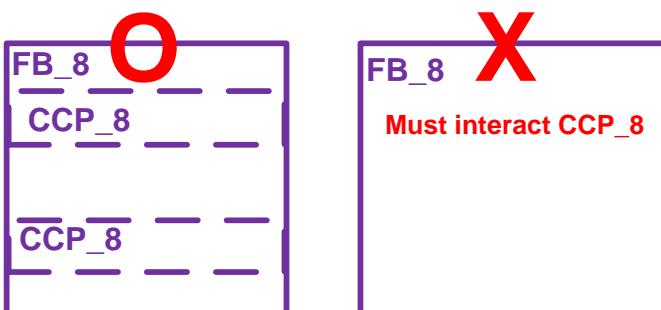


H300.CCP.S.1 / H300.CCP.S.2

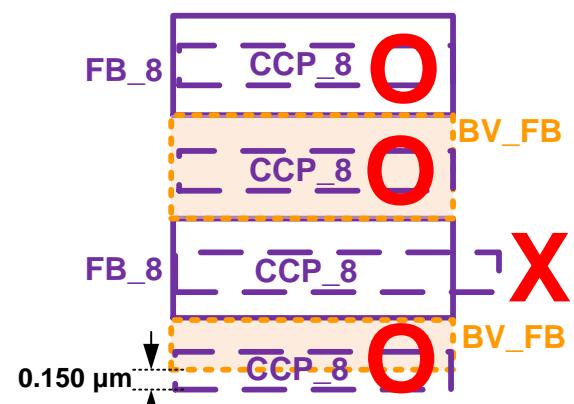
H300.CCP.S.3 / H300.CCP.R.2



H300.CCP.R.1 / H300.CCP.R.1.1 / H300.CCP.R.1.3



H300.CCP.R.3



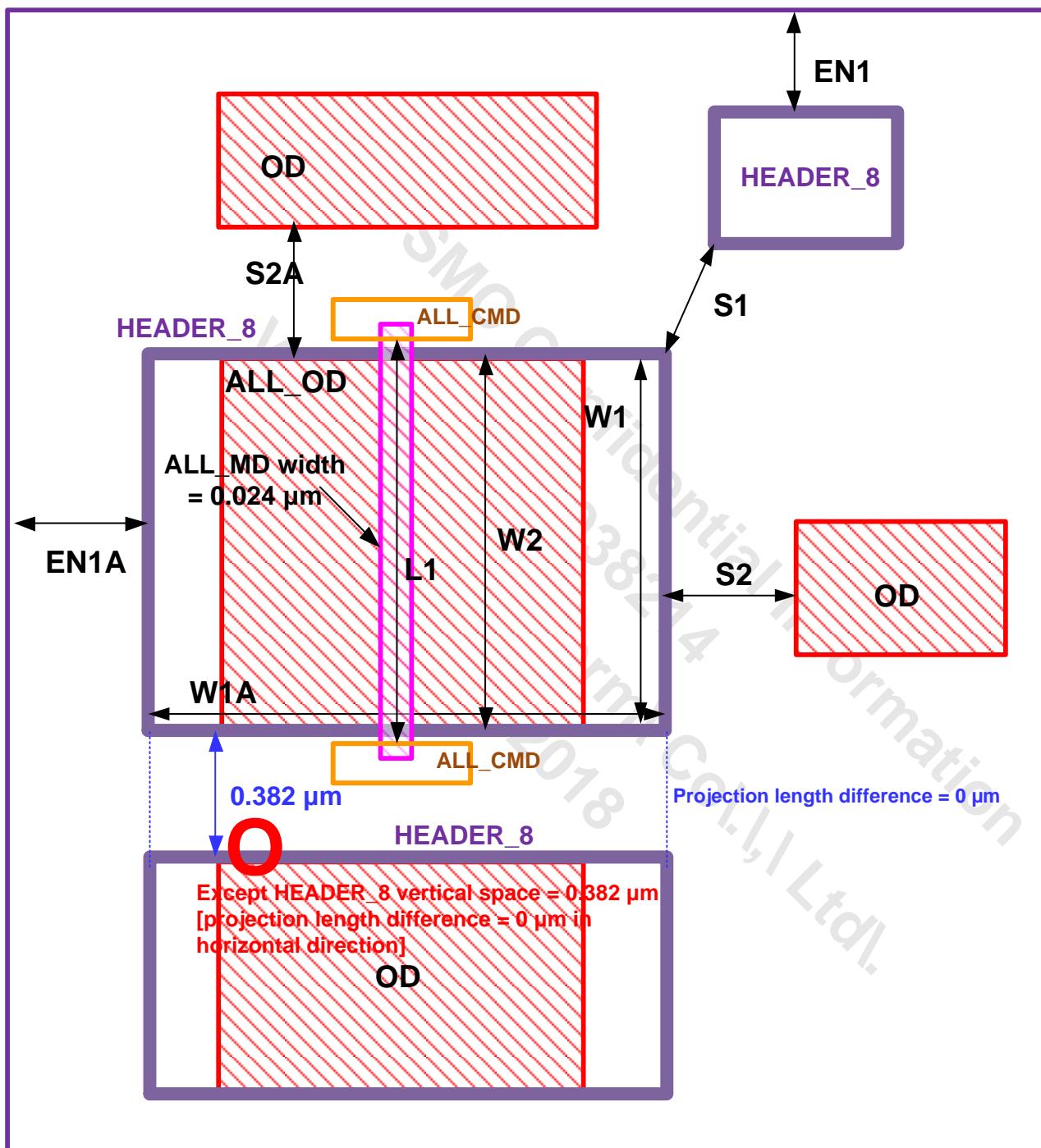
H300.CCP.R.4

4.5.13.4.2 H300 Header Cell Layout Rules

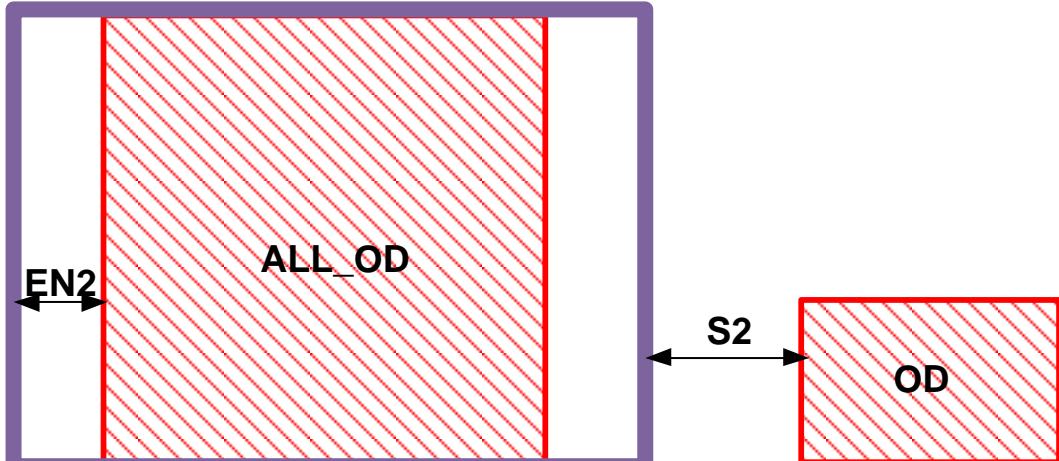
HEADER_8 (CAD layer: 6;128) is used to define HEADER cell inside FB_8

Rule No.	Description	Label	Op.	Rule
H300.HEADER.W.1	Width of HEADER_8 in vertical direction	W1	=	0.2180
H300.HEADER.W.1.1	Width of HEADER_8 in horizontal direction	W1A	\geq	0.8100
H300.HEADER.W.2	Width of ALL_OD [INSIDE HEADER_8] in vertical direction	W2	=	0.2180
H300.HEADER.S.1	Space of HEADER_8 (Except following conditions: 1. HEADER_8 vertical space = 0.382 μm [projection length difference = 0 μm in horizontal direction])	S1	\geq	0.6000
H300.HEADER.S.2	Space of HEADER_8 to OD in horizontal direction [PRL > -0.082 μm]	S2	\geq	0.0800
H300.HEADER.S.2.0.1	Space of HEADER_8 to OD in horizontal direction [PRL > -0.082 μm , INSIDE PO_P63]	S2	\geq	0.0890
H300.HEADER.S.2.1	Space of HEADER_8 to OD in vertical direction [PRL > -0.080 μm]	S2A	\geq	0.0820
H300.HEADER.EN.1	Enclosure by FB_8 in vertical direction	EN1	=	0.3410+0.3000*n
H300.HEADER.EN.1.1	Enclosure by FB_8 in horizontal direction	EN1A	\geq	0.5700
H300.HEADER.EN.2	Enclosure of OD in horizontal direction (Cut is not allowed) (Except PO_P63)	EN2	=	0.0800 ~ 0.0815
H300.HEADER.EN.2.1	Enclosure of OD in horizontal direction [INSIDE PO_P63] (Cut is not allowed)	EN2A	=	0.0890 ~ 0.0905
H300.HEADER.L.1	Length of {ALL_MD [width = 0.024 μm , INTERACT HEADER_8] NOT ALL_CMD} in vertical direction	L1	=	0.0420 ~ 0.8440
H300.HEADER.R.1	HEADER_8 must be inside FB_8			
H300.HEADER.R.2	Horizontal edge of HEADER_8 must abut ALL_OD			
H300.HEADER.R.3	Horizontal edge of OD [INSIDE HEADER_8] must be fully projected by another OD with space = 0.082 μm .			
H300.HEADER.R.3.1	Horizontal edge of OD_Forbidden_Region interact OD is not allowed. OD_Forbidden_Region { {{HEADER_8 SIZING 0.080 μm in horizontal direction} NOT OD} SIZING 0.082 μm in vertical direction}			
H300.HEADER.R.3.1.1	Horizontal edge of OD_Forbidden_Region [INTERACT PO_P63] interact OD is not allowed. OD_Forbidden_Region { {{HEADER_8 SIZING 0.089 μm in horizontal direction} NOT OD} SIZING 0.082 μm in vertical direction}			
H300.HEADER.R.4	HEADER_8 must be a rectangle orthogonal to grid			
H300.HEADER.R.5	Only one OD is allowed inside HEADER_8			

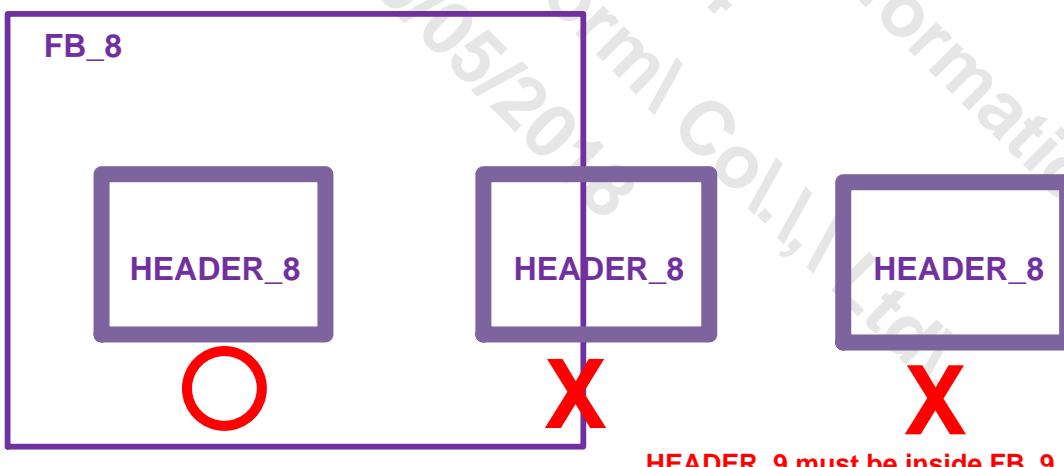
H300-HEADER



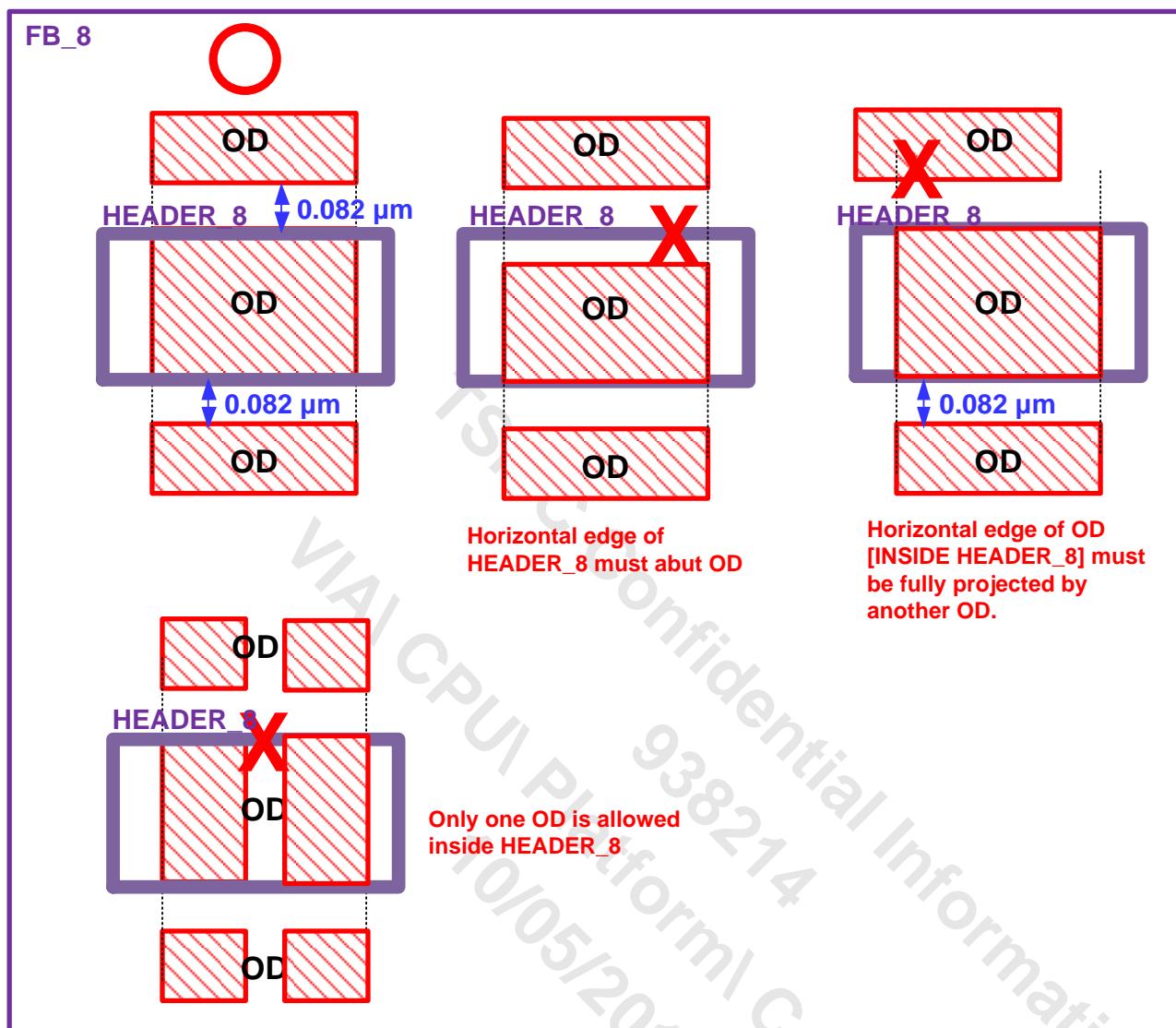
H300.HEADER.W.1 / H300.HEADER.W.1.1 /
H300.HEADER.W.2 / H300.HEADER.S.1 /
H300.HEADER.S.2 / H300.HEADER.S.2.1 /
H300.HEADER.EN.1 / H300.HEADER.EN.2 /
H300.HEADER.L.1

FB_8**PO_P63****HEADER_8**

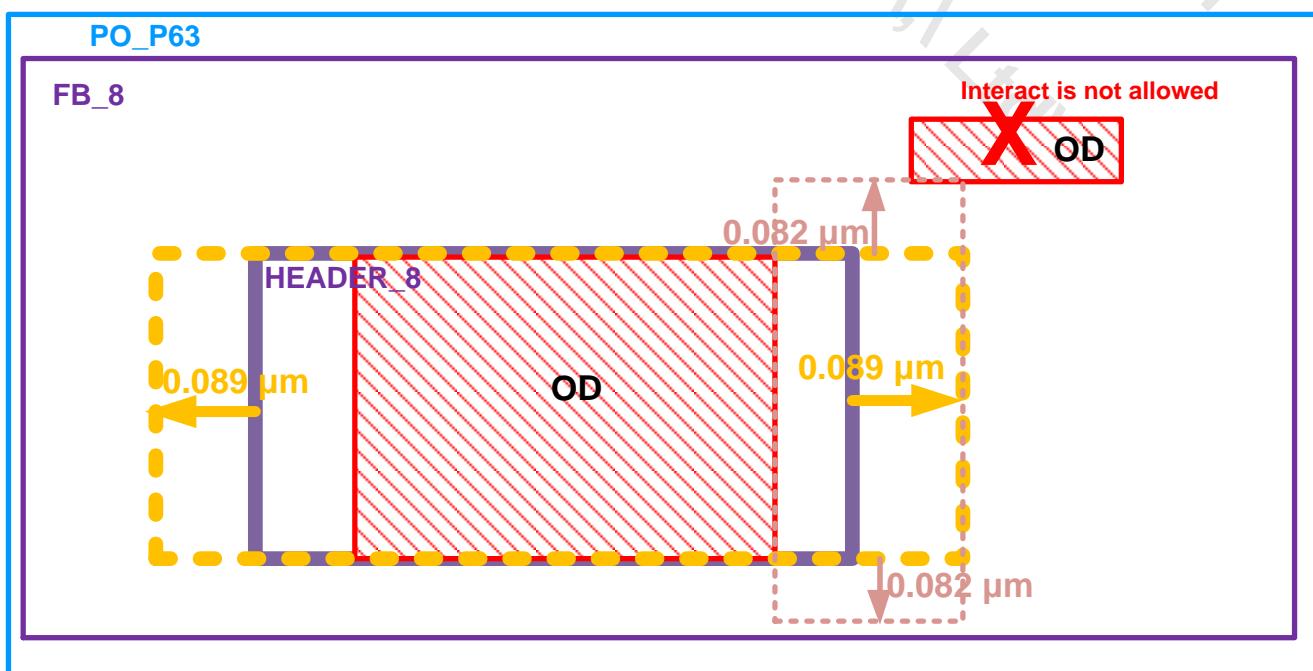
**H300.HEADER.S.2.0.1 / H300.HEADER.EN.2 /
H300.HEADER.EN.2.1**



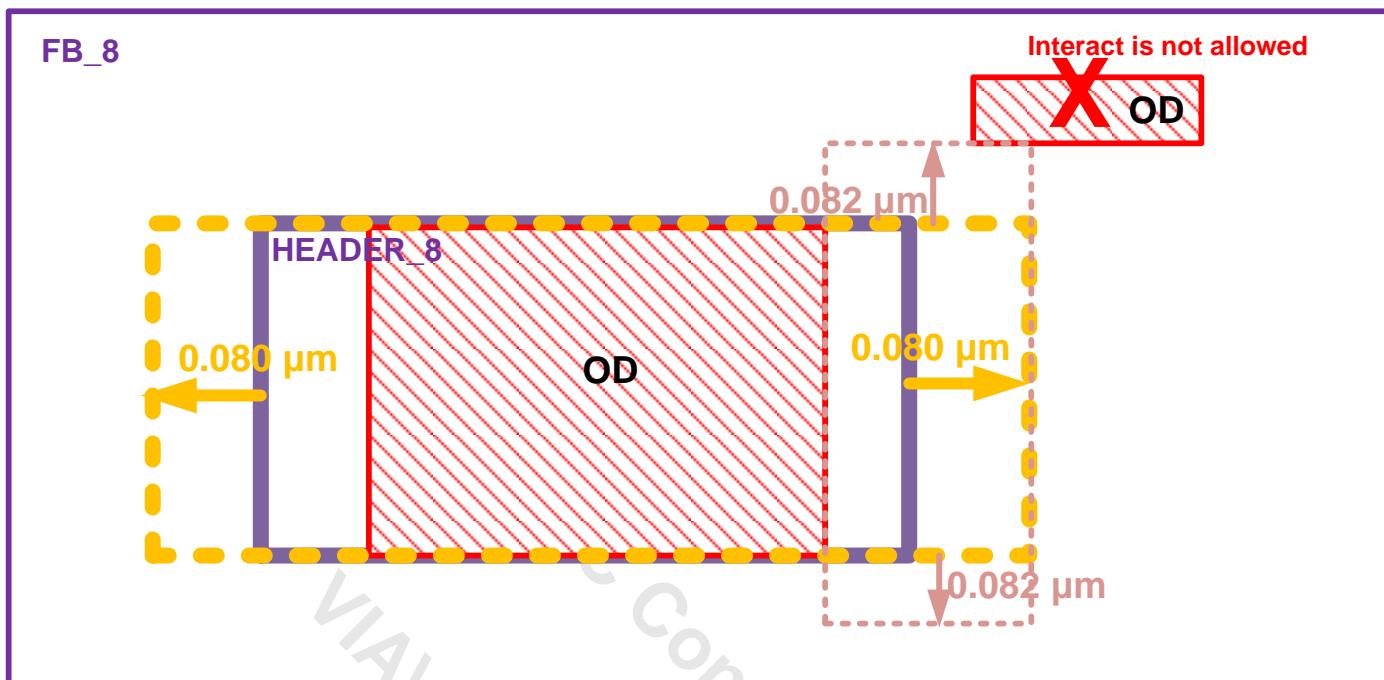
H300.HEADER.R.1



H300.HEADER.R.2 / H300.HEADER.R.3 / H300.HEADER.R.5



H300.HEADER.R.3.1.1



H300.HEADER.R.3.1



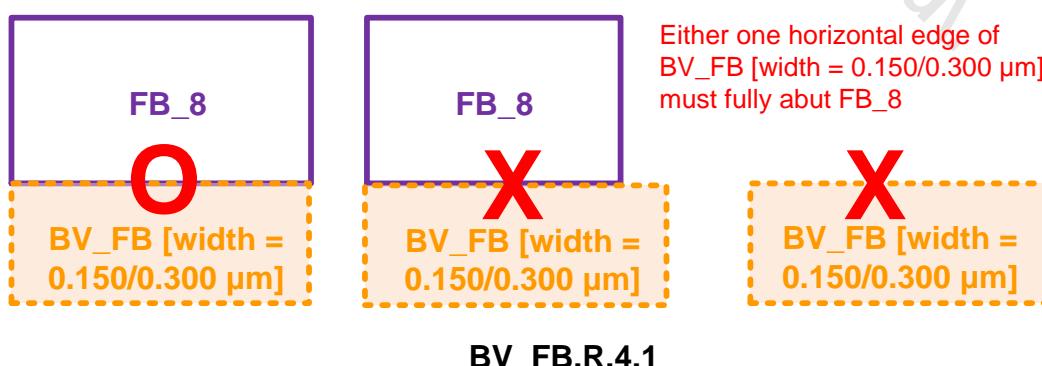
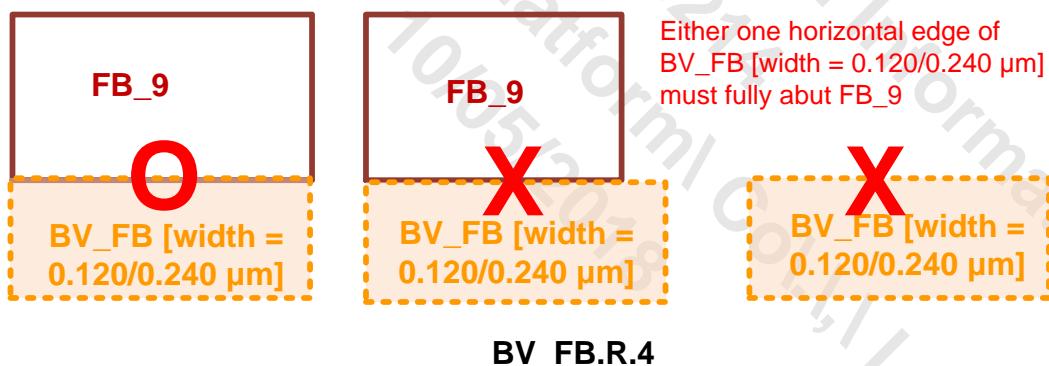
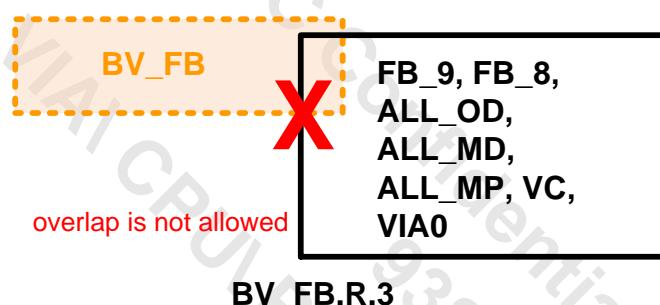
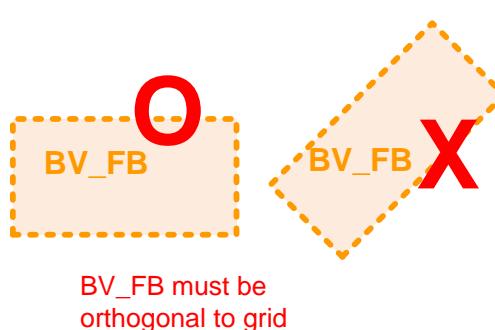
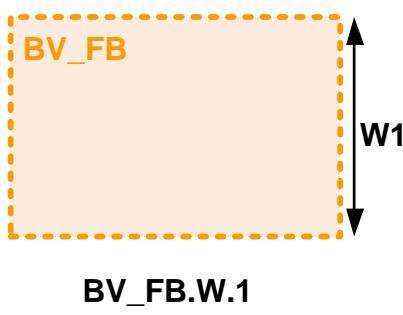
H300.HEADER.R.4

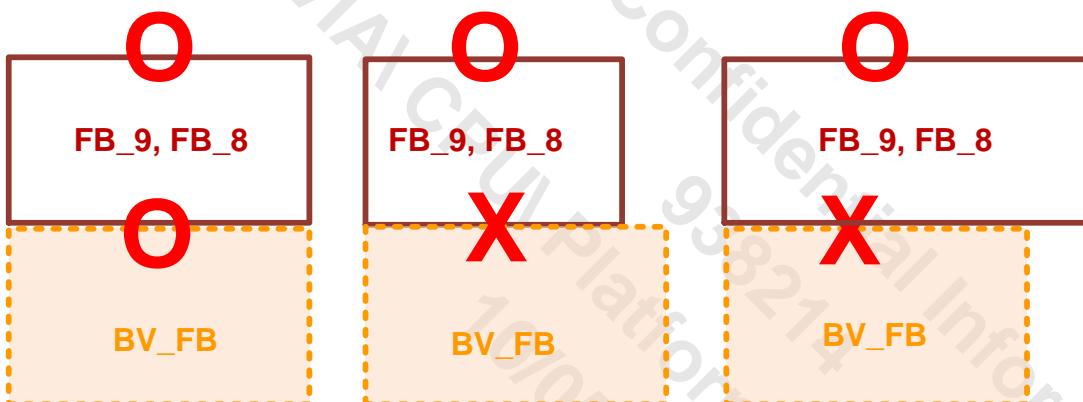
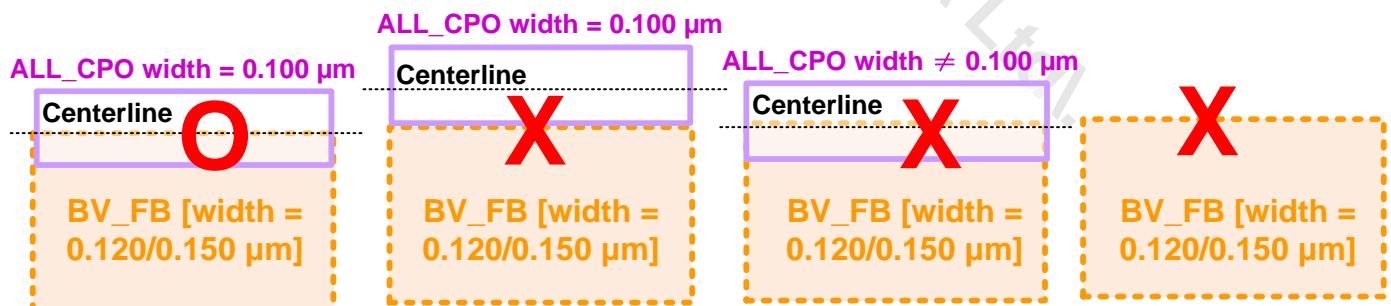
4.5.14 BV_FB Layout Rules

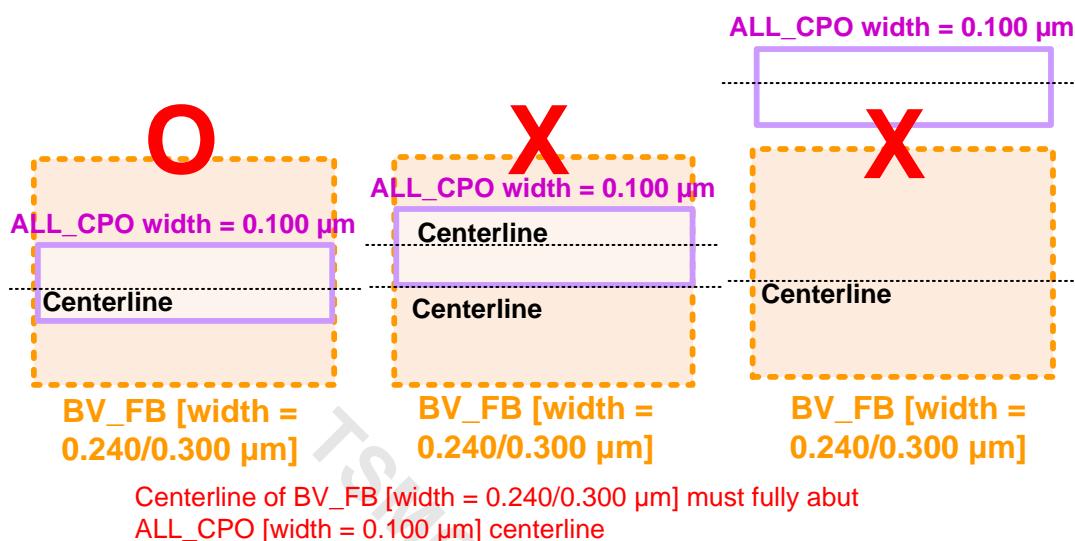
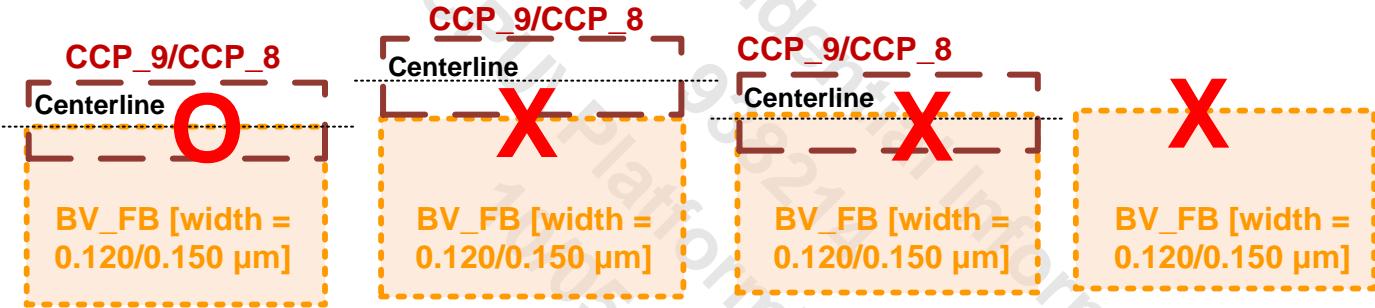
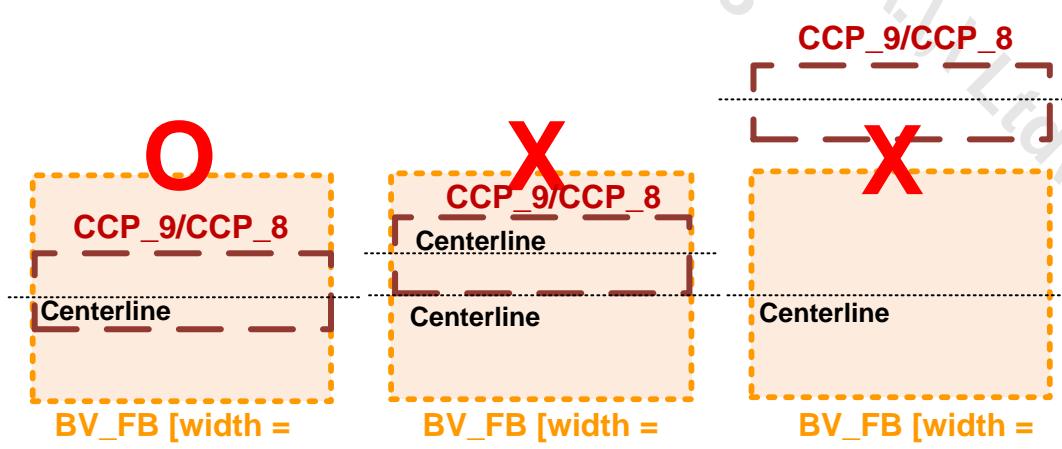
BV_FB (CAD layer 250;119) is used for STDCELL vertical abutment.

Rule No.	Description	Label	Op.	Rule
BV_FB.W.1	Width of BV_FB in vertical direction	W1	=	0.1200, 0.1500, 0.2400, 0.3000
BV_FB.R.1	BV_FB must be orthogonal to grid			
BV_FB.R.3	BV_FB overlap FB_9, FB_8, ALL_OD, ALL_MD, ALL_MP, VC, VIA0 is not allowed			
BV_FB.R.4	Either one horizontal edge of BV_FB [width = 0.120/0.240 µm] must fully abut FB_9			
BV_FB.R.4.1	Either one horizontal edge of BV_FB [width = 0.150/0.300 µm] must fully abut FB_8			
BV_FB.R.4.3	Horizontal edge of BV_FB [width = 0.240/0.300 µm] must fully abut FB_9/FB_8, respectively.			
BV_FB.R.5	Horizontal edge [INTERACT BV_FB] of {FB_9 OR FB_8} must fully abut BV_FB			
BV_FB.R.6	Either one horizontal edge of BV_FB [width = 0.120/0.150 µm] must fully abut ALL_CPO [width = 0.100 µm] centerline			
BV_FB.R.6.1	Centerline of BV_FB [width = 0.240/0.300 µm] must fully abut ALL_CPO [width = 0.100 µm] centerline			
BV_FB.R.7	Either one horizontal edge of BV_FB [width = 0.120/0.150 µm] must fully abut CCP_9/CCP_8 centerline, respectively.			
BV_FB.R.7.1	Centerline of BV_FB [width = 0.240/0.300 µm] must fully abut CCP_9/CCP_8 centerline, respectively.			

BV_FB



**BV_FB.R.4.3****BV_FB.R.5****BV_FB.R.6**

**BV_FB.R.6.1****BV_FB.R.7**

Centerline of BV_FB [width = 0.240/0.300 μm] must fully abut CCP_9/CCP_8 centerline

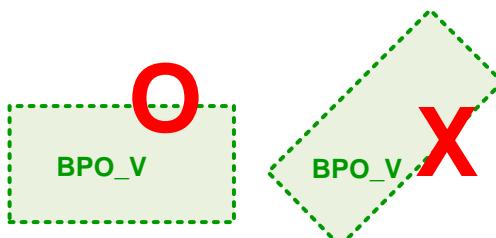
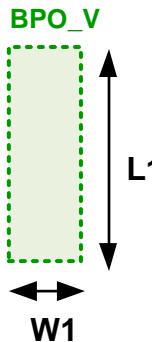
BV_FB.R.7.1

4.5.15 BPO_V Layout Rules

BPO_V (CAD layer 17;52) is used for STDCELL vertical abutment.

Rule No.	Description	Label	Op.	Rule
BPO_V.W.1	Width of BPO_V in horizontal direction	W1	=	0.0080
BPO_V.L.1	Length of BPO_V in vertical direction	L1	=	0.0500, 0.1000
BPO_V.R.1	BPO_V must be a rectangle orthogonal to grid			
BPO_V.R.2	BPO_V must be inside {ALL_CPO [width = 0.100 μm] AND BV_FB}			
BPO_V.R.4	Either one horizontal edge of BPO_V must fully abut SR_DPO			
BPO_V.R.5	SR_DPO horizontal edge abut CPO [INTERACT BV_FB] must fully abut BPO_V			
BPO_V.R.6	Horizontal edge of BPO_V [length = 0.100 μm] must fully abut SR_DPO			

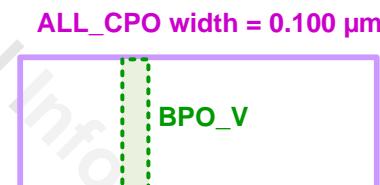
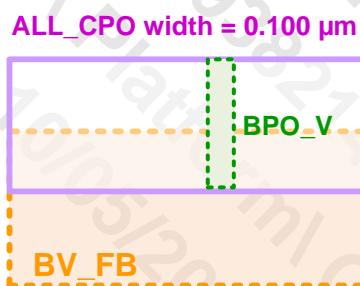
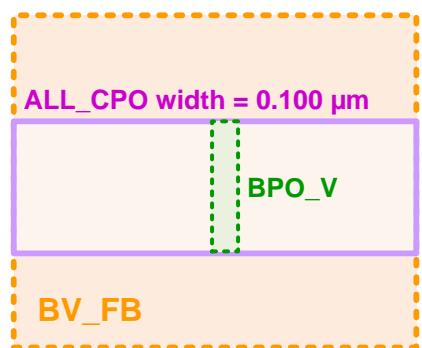
BPO_V



BPO_V must be a rectangle orthogonal to grid

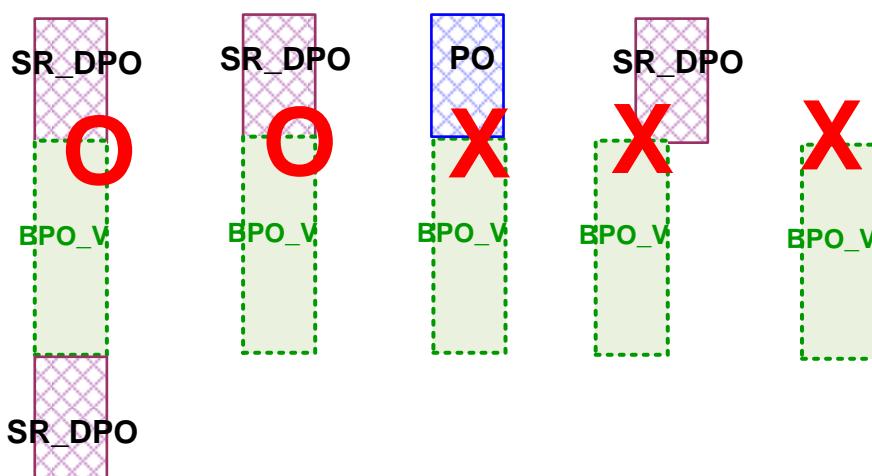
**BPO_V.W.1 /
BPO_V.L.1**

BPO_V.R.1

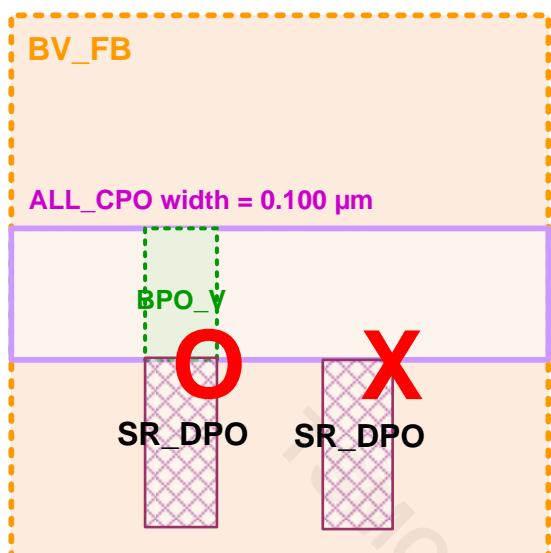


BPO_V must be inside {ALL_CPO [width = 0.100 μm] AND BV_FB}

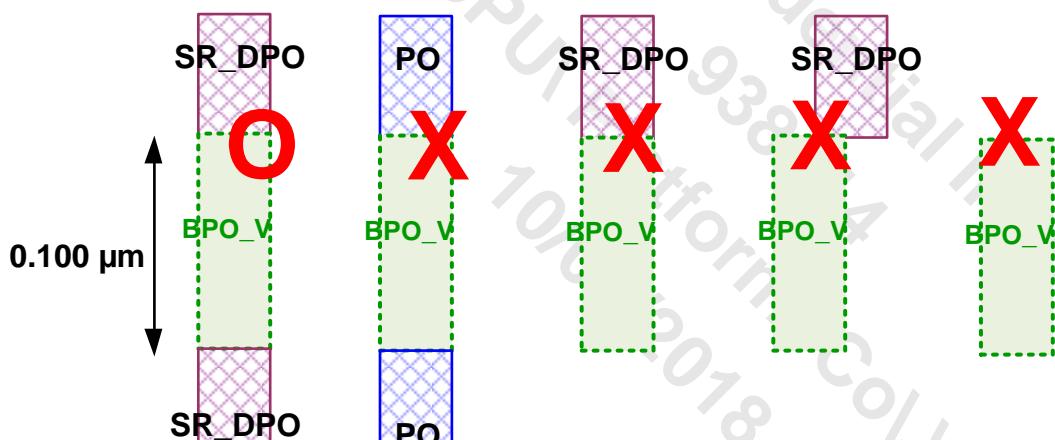
BPO_V.R.2



BPO_V.R.4



BPO_V.R.5



BPO_V.R.6

4.5.16 Poly on OD edge (PODE) Layout Rules

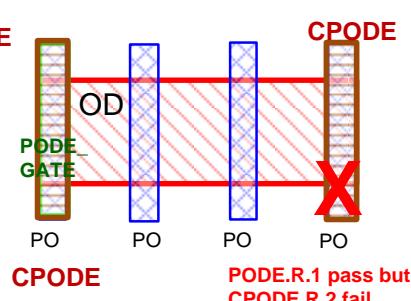
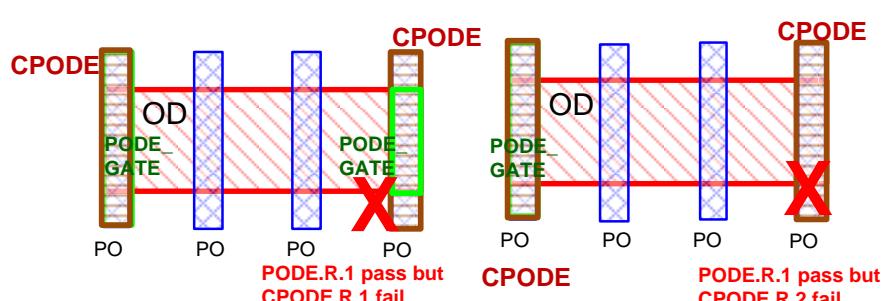
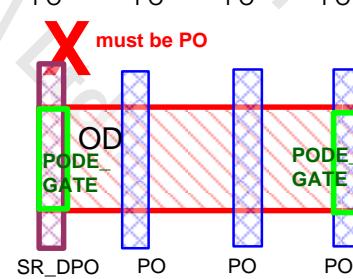
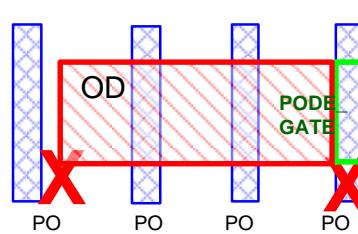
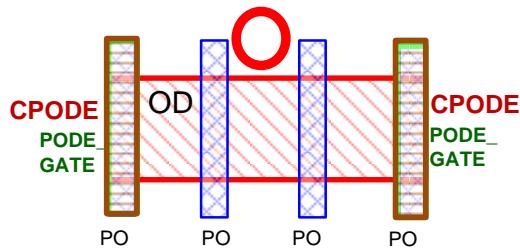
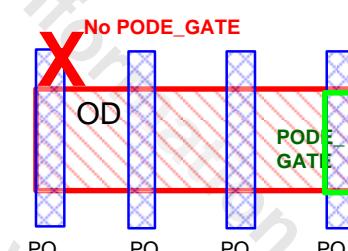
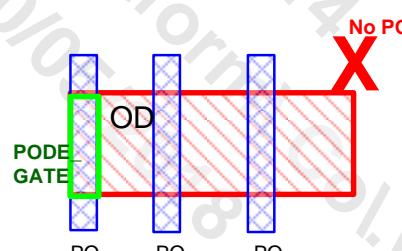
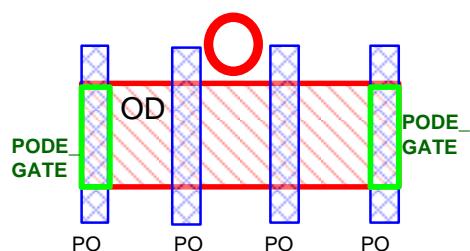
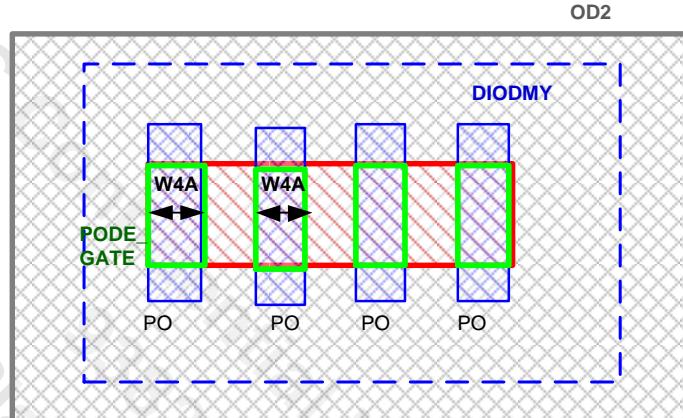
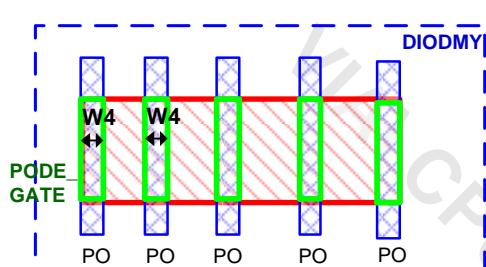
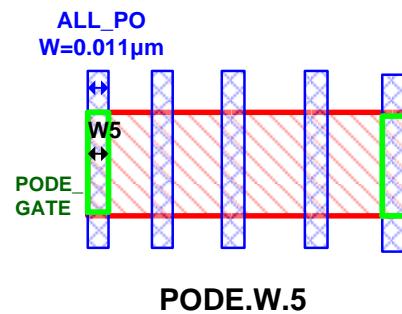
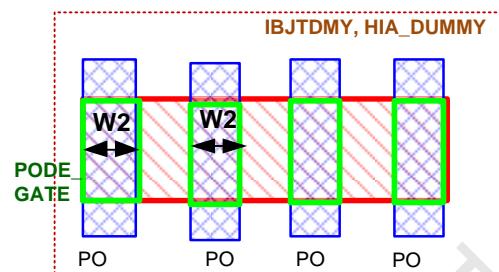
PODE_GATE (CAD layer: 206;28) is used to define GATE abutting OD vertical edge for LVS recognize 3-terminal MOS diode on OD edge.

TrGATE = {GATE NOT {PODE_GATE OR CPODE}}

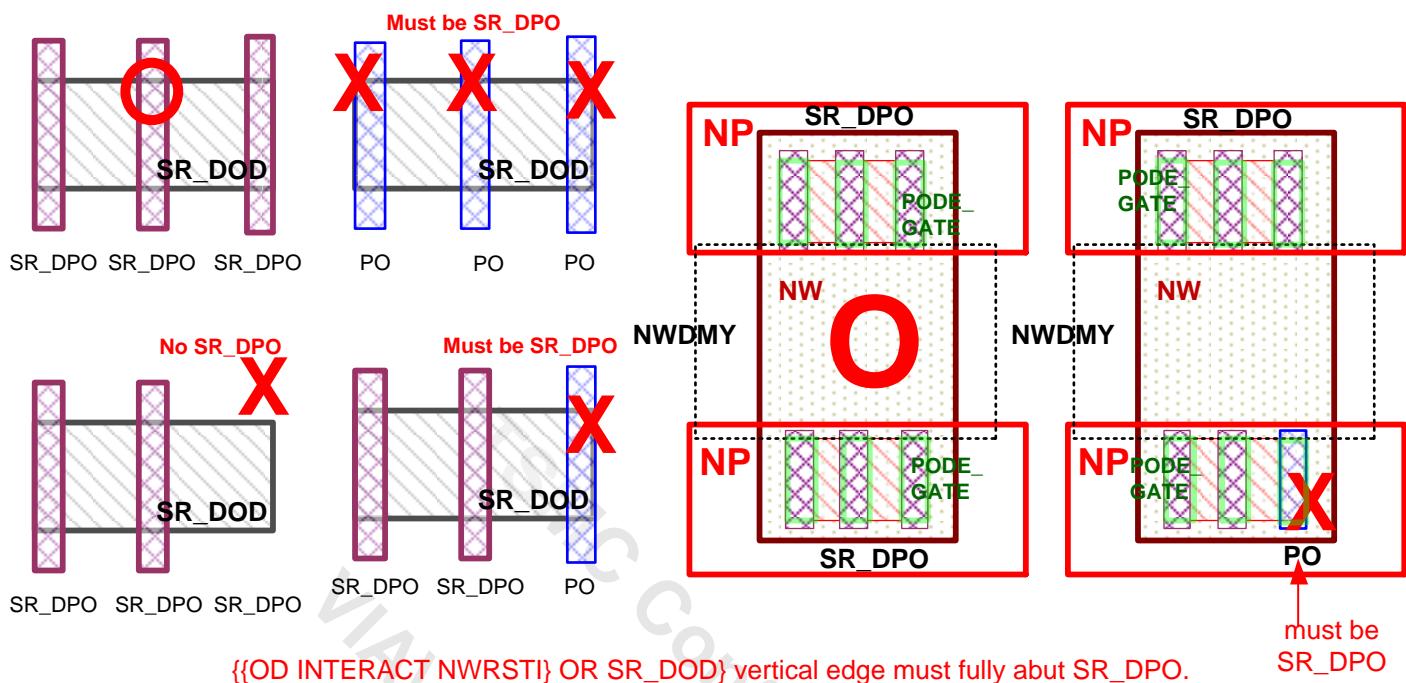
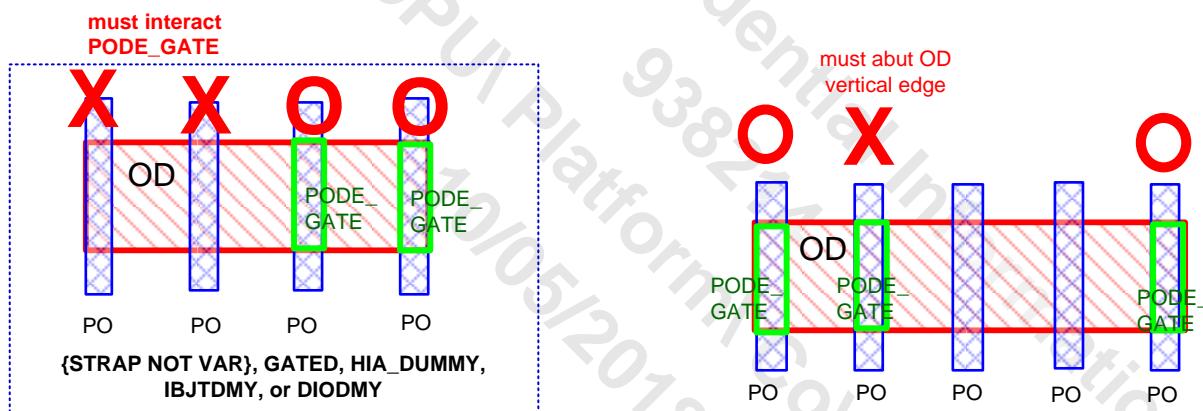
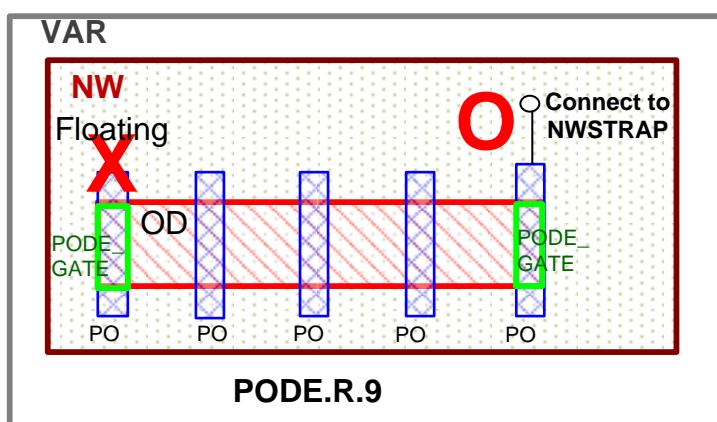
Rule No.	Description	Label	Op.	Rule
PODE.W.2	Width of {PO AND PODE_GATE} in horizontal direction [INSIDE IBJTD MY, HIA_DUMMY]	W2	=	0.0860
PODE.W.4	Width of {PO AND PODE_GATE} in horizontal direction [INSIDE {DIOD MY NOT OD2}]	W4	=	0.0200
PODE.W.4.1	Width of {PO AND PODE_GATE} in horizontal direction [INSIDE {DIOD MY AND OD2}]	W4A	=	0.0860
PODE.W.5	Width of PODE_GATE [NOT INTERACT CPODE [width = 0.011 μm], INTERACT ALL_PO [width = 0.011 μm]] (Except following conditions: 1. PODE_GATE_Region, 2. PODE_GATE [width = 0.008 μm] abut ALL_PO [width = 0.011 μm]) Definition of PODE_GATE_Region follows CPODE.R.9	W5	=	0.0110
PODE.R.1	OD vertical edge must fully abut both PO and {PODE_GATE OR CPODE} (Except SEALRING_ALL, NWRSTI, BLK_WF, or following conditions: 1. GATE [Lg < 0.011 μm] inside {PODE_GATE OR CPODE} [width = 0.011 μm], 2. OD edge abut CPODE [width = 0.011 μm, INTERACT PODE_GATE [width = 0.008 μm]])			
PODE.R.1.1	{{OD INTERACT NWRSTI} OR SR_DOD} vertical edge must fully abut SR_DPO (Except DC6_2 (257;62))			
PODE.R.2	GATE [INSIDE {STRAP NOT VAR}, HIA_DUMMY, IBJTD MY, or DIOD MY] must interact PODE_GATE (Except BLK_WF)			
PODE.R.2.1	Either one vertical edge of PODE_GATE must fully abut OD vertical edge (Except HIA_DUMMY, IBJTD MY, DIOD MY, or following conditions: 1. {STRAP NOT VAR}, 2. OD edge interact CPODE [width = 0.011 μm, INTERACT PODE_GATE [width = 0.008 μm]], 3. PODE_GATE_Region) Definition of PODE_GATE_Region follows CPODE.R.9			
PODE.R.3	PODE_GATE must be drawn identically to GATE (Except following conditions: 1. GATE [Lg = 0.008 μm] inside PODE_GATE [width = 0.011 μm], 2. OD edge interact CPODE [width = 0.011 μm, INTERACT PODE_GATE [width = 0.008 μm]], 3. PODE_GATE_Region) Definition of PODE_GATE_Region follows CPODE.R.9			
PODE.R.9	{{PO NOT CPO} INTERACT {PODE_GATE AND NW}} [INSIDE VAR] must connect to NWSTRAP			
PODE.R.12	Width of {PO AND PODE_GATE} in horizontal direction must be the same [0.020 μm ≤ TrGATE Lg ≤ 0.036 μm, INTERACT same OD]			

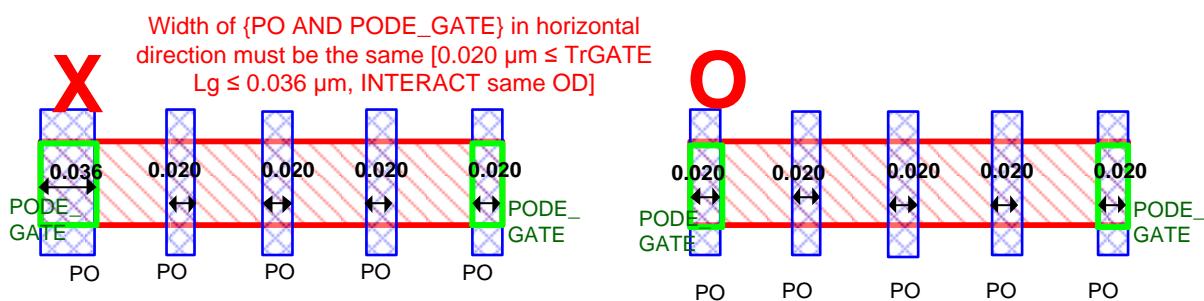
Rule No.	Description	Label	Op.	Rule
PODE.R.12.2	Width of {PO AND PODE_GATE} [in horizontal and outside OD direction] neighboring to LAST TrGATE [channel length $\geq 0.072 \mu\text{m}$, {PO AND PODE_GATE} to LAST TrGATE space = $0.094 \mu\text{m}$] must be the same as LAST TrGATE or $0.072 \mu\text{m}$ Definition of LAST TrGATE: TrGATE abut the same S/D with PODE_GATE [OD on LAST TrGATE extension $\leq 0.334 \mu\text{m}$] (Except OD2)			
PODE.R.12.3	Width of {PO AND PODE_GATE} [in horizontal and outside OD direction] neighboring to LAST TrGATE [INSIDE OD2, {PO AND PODE_GATE} to LAST TrGATE space = $0.094 \mu\text{m}$] must be the same as LAST TrGATE, or $0.086 \mu\text{m}$, or $0.135 \mu\text{m}$ Definition of LAST TrGATE: TrGATE abut the same S/D with PODE_GATE [OD on LAST TrGATE extension $\leq 0.334 \mu\text{m}$] (Except OD18_12, OD15_12)			
PODE.R.12.4	Width of {PO AND PODE_GATE} [in horizontal and outside OD direction] neighboring to LAST TrGATE [INSIDE {OD18_12 OR OD15_12}, {PO AND PODE_GATE} to LAST TrGATE space = $0.094 \mu\text{m}$] must be the same as LAST TrGATE, $0.072 \mu\text{m}$, or $0.086 \mu\text{m}$ or $0.135 \mu\text{m}$ Definition of LAST TrGATE: TrGATE abut the same S/D with PODE_GATE [OD on LAST TrGATE extension $\leq 0.334 \mu\text{m}$]			
PODE.R.13	Width of GATE [$0.020 \mu\text{m} \leq \text{Lg} \leq 0.036 \mu\text{m}$] on the same OD must be the same			
PODE.R.14	Width of TrGATE [width = $0.008/0.011 \mu\text{m}$, between two neighboring PODE_GATE, INTERACT same OD [NOT INTERACT CPODE]] must be the same (Except BLK_WF)			
PODE.R.15	Width of TrGATE [between both two neighboring PODE_GATE [width = $0.008 \mu\text{m}$], INTERACT same OD [NOT INTERACT CPODE]] must be $0.008 \mu\text{m}$			

PODE

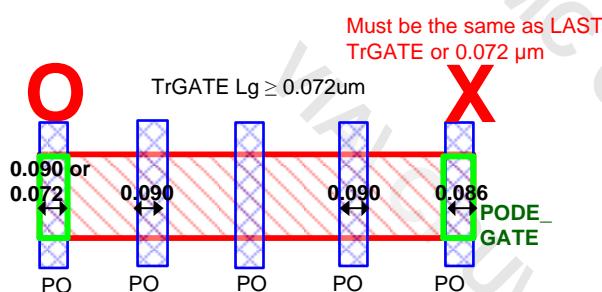


PODE.R.1

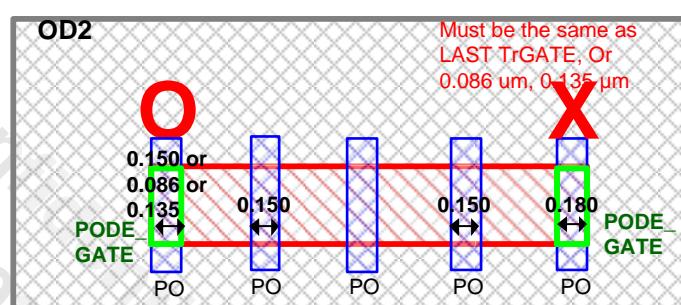
**PODE.R.1.1****PODE.R.2****PODE.R.2.1**



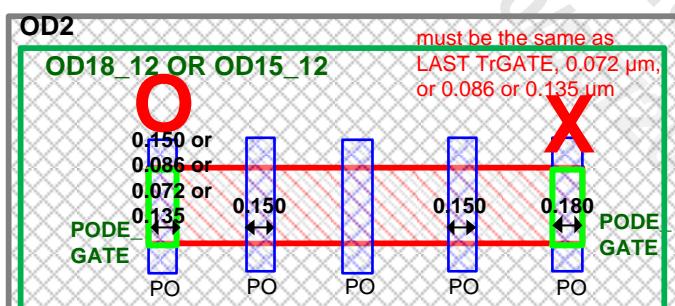
PODE.R.12



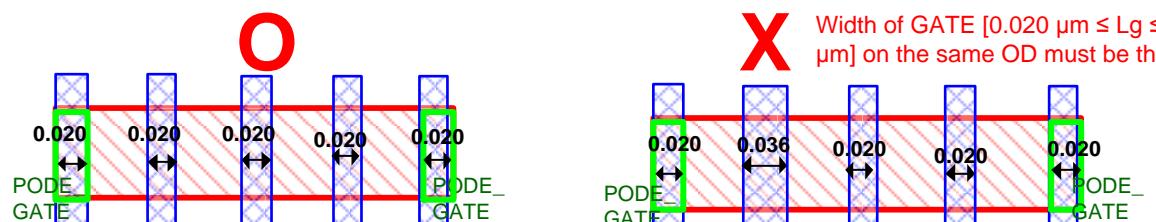
PODE.R.12.2



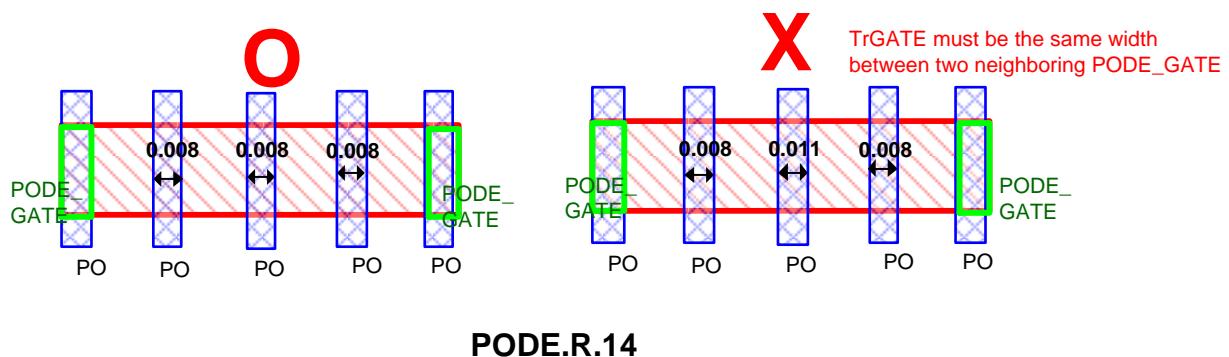
PODE.R.12.3



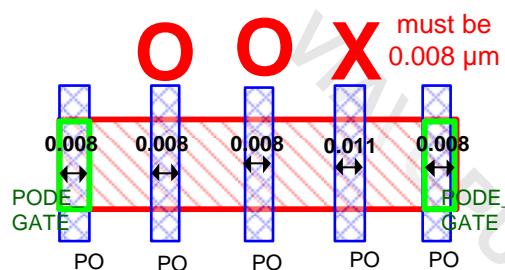
PODE.R.12.4



PODE.R.13



PODE.R.14



PODE.R.15

4.5.17 Connected PODE (CPODE) Layout Rules (72N, 82N)

CPODE (CAD layer: 206;32) is a tape-out layer and used to connect two PODE cells together, including drain-to-drain abutment in Std. cell. An OD related mask (72N, 82N) is generated accordingly for manufacture. In LVS, CPODE overlap PODE_GATE at OD edge, the GATE is still treated as 3-terminal MOS diode.

DCPODE (CAD layer: 206;33) is generated by dummy utility.

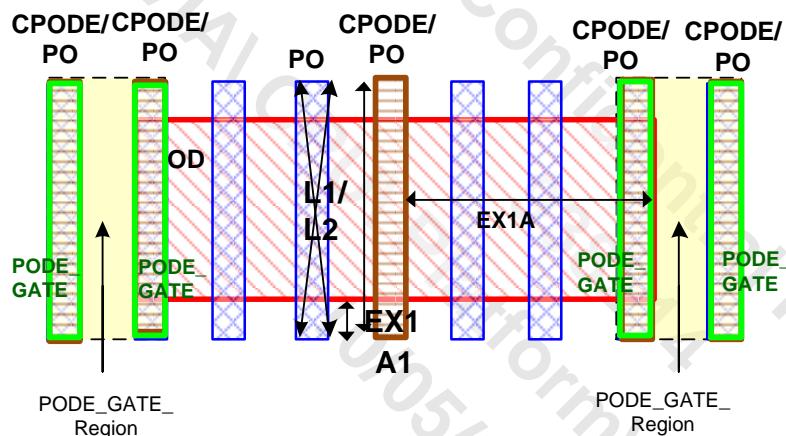
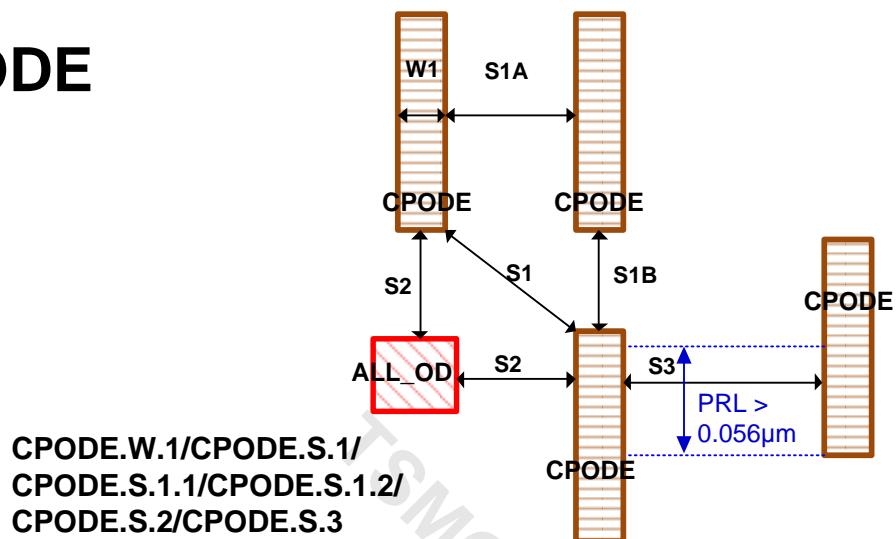
ALL CPODE = {CPODE OR DCPODE}

Rule No.	Description	Label	Op.	Rule
CPODE.W.1	Width in horizontal direction	W1	=	0.0080, 0.0110
CPODE.W.3	<p>Maximum width of CPODE_Group in horizontal direction</p> <p>(Except following conditions: 1. Rectangle {CPODE_Group SIZING down/up 0.070 µm in horizontal direction} [Width ≤ 0.182 µm in horizontal direction] with length ≤ 0.016 µm in vertical direction)</p> <p>Definition of CPODE_Group: $\{\{\{CPODE \text{ NOT Checked_PODE_GATE}\} \text{ SIZING up/down } 0.0275 \mu\text{m in horizontal direction}\} \text{ SIZING down/up } 0.0055 \mu\text{m in horizontal direction}\}$</p> <p>Definition of Checked_PODE_GATE follows CPODE.S.1.1</p>	L3	≤	0.1250
CPODE.S.1	Space	S1	≥	0.0460
CPODE.S.1.1	<p>Space {CPODE NOT Checked_PODE_GATE} in horizontal direction</p> <p>Definition of Checked_PODE_GATE: $\{\{PODE_GATE \text{ SIZING } 0.002 \mu\text{m in horizontal direction}\} \text{ AND }\{CPODE \text{ OR PODE_GATE}\}$</p>	S1A	≥	0.0460
CPODE.S.1.2	<p>Space of {CPODE NOT Checked_PODE_GATE} in vertical direction</p> <p>Definition of Checked_PODE_GATE follows CPODE.S.1.1</p>	S1B	≥	0.1120
CPODE.S.2	<p>{CPODE NOT Checked_PODE_GATE} space to ALL_OD</p> <p>Definition of Checked_PODE_GATE follows CPODE.S.1.1</p>	S2	≥	0.0320
CPODE.S.3	<p>Maximum space of Final CPODE in horizontal direction [PRL > 0.056 µm]</p> <p>(Except following conditions: 1. Final_CPODE enclosure by {FB_9 OR BV_FB} within 0.680 µm in horizontal direction)</p> <p>Definition of Final_CPODE: $\{\{\{Checked_CPODE \text{ NOT Checked_PODE_GATE}\} \text{ SIZING down/up } 0.001 \mu\text{m in horizontal direction}\} \text{ NOT CPO}\}$</p> <p>Definition of Checked_CPODE: $\{CPODE [\text{width} = 0.008 \mu\text{m}] \text{ SIZING } 0.0015 \mu\text{m in horizontal direction}\}$ $\text{OR } CPODE [\text{width} = 0.011 \mu\text{m}]$</p> <p>Definition of Checked_PODE_GATE follows CPODE.S.1.1</p>	S3	≤	1.3600

Rule No.	Description	Label	Op.	Rule
CPODE.EX.1	{CPODE NOT Checked_PODE_GATE} extension on ALL_OD in vertical direction Definition of Checked_PODE_GATE follows CPODE.S.1.1	EX1	\geq	0.0320
CPODE.EX.1.1	ALL_OD extension on CPODE in horizontal direction	EX1A	$=$	0, ≥ 0.1125
CPODE.L.1	Length of {CPODE NOT Checked_PODE_GATE} in vertical direction Definition of Checked_PODE_GATE follows CPODE.S.1.1	L1	\geq	0.1120
CPODE.L.2	Maximum length of {CPODE NOT Checked_PODE_GATE} in vertical direction Definition of Checked_PODE_GATE follows CPODE.S.1.1	L2	\leq	30
CPODE.A.1	Area of {CPODE NOT Checked_PODE_GATE} Definition of Checked_PODE_GATE follows CPODE.S.1.1	A	\geq	0.00089
CPODE.O.1	Horizontal edge of {CPODE NOT Checked_PODE_GATE} overlap of CPO [width = 0.016 μm] in vertical direction Definition of Checked_PODE_GATE follows CPODE.S.1.1	O1	$=$	0.0080
CPODE.DN.1	Minimum {{CPODE NOT Checked_PODE_GATE} OR DCPODE} density across full chip (Except following conditions: 1. CPODE does not exist in the chip) Definition of Checked_PODE_GATE follows CPODE.S.1.1		\geq	1%
CPODE.DN.2	Maximum {{CPODE NOT Checked_PODE_GATE} OR DCPODE} density across full chip Definition of Checked_PODE_GATE follows CPODE.S.1.1		\leq	10%
CPODE.DN.3	Maximum {{CPODE NOT Checked_PODE_GATE} OR DCPODE} density in window 15 μm x 15 μm, stepping 7.5 μm Definition of Checked_PODE_GATE follows CPODE.S.1.1		\leq	12%
CPODE.DN.4	Maximum {{ALL_CPO OR CPO_SRAM} OR {ALL_CPODE NOT Checked_PODE_GATE}} density in window 15 μm x 15 μm, stepping 7.5 μm Definition of Checked_PODE_GATE follows CPODE.S.1.1		\leq	20%
CPODE.R.1	{CPODE AND OD} must be drawn identically to GATE			
CPODE.R.2	CPODE abut OD vertical edge [between two consecutive 90-90 degree corners] is not allowed (Except following conditions: 1. PODE_GATE_Region, 2. Checked_PODE_GATE, 3. {CPODE AND {OD AND SR_DOD}}) Definition of Checked_PODE_GATE follows CPODE.S.1.1 Definition of PODE_GATE_Region follows CPODE.R.9			
CPODE.R.2.1	{{CPODE NOT CPO} AND PODE_GATE} must follow either one of the following conditions 1. Abut OD vertical edge [between two consecutive 90-90 degree corners], 2. OUTSIDE OD, 3. INSIDE CPODE [width = 0.011 μm] and abut the vertical edge of {OD SIZING 0.0015 μm in horizontal direction} [between two consecutive 90-90 degree corners]			

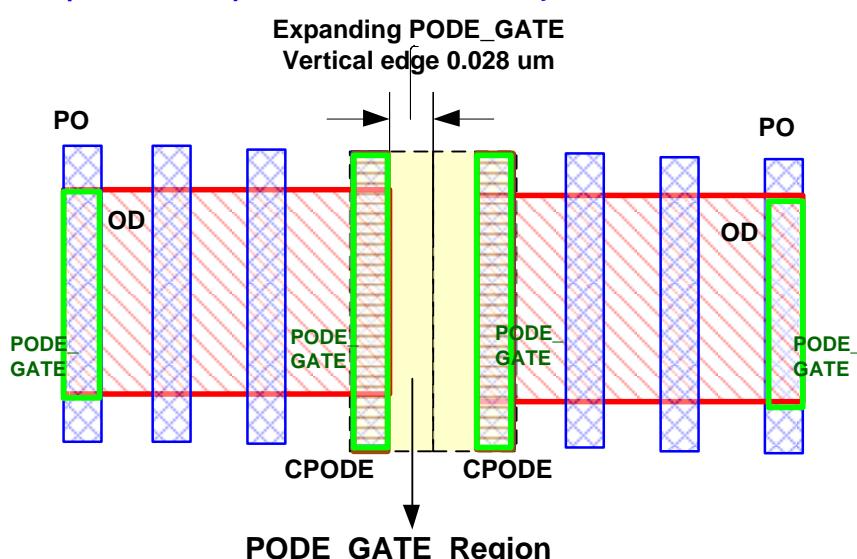
Rule No.	Description	Label	Op.	Rule
CPODE.R.3	{PO NOT CPO} [INTERACT CPODE] overlap MP is not allowed. (Except following conditions: 1. MP [Width = 0.022 μm] overlap {{PO NOT CPO} AND CPODE})			
CPODE.R.5	CPODE interact STRAP, {horizontal edge of PODE_TrGATE}, DIODMY, Dummy_Cell, OD2 or {SRM (50;0) OR SRAMDMY (186;0)} is not allowed			
CPODE.R.6	CPODE must be rectangular orthogonal to grid (Except following conditions: 1. CPODE [width = 0.011 μm] abut CPODE [width = 0.008 μm] in horizontal edge)			
CPODE.R.7	Maximum delta V > 0.98 V between 2 source/drain ACTIVE beside CPODE is not allowed			
CPODE.R.8	Vertical edge of PODE_GATE [INTERACT CPODE] must be coincident with CPODE vertical edge (Except following conditions: 1. {PODE_GATE [width = 0.008 μm] AND CPODE [width = 0.011 μm]})			
CPODE.R.8.1	Vertical edge of {Checked_CPODE NOT Checked_PODE_GATE} must be coincident with ALL_PO vertical edge Definition of Checked_CPODE: {CPODE [width = 0.008 μm] SIZING 0.0015 μm in horizontal direction} AND SR_DPO} OR CPODE Definition of Checked_PODE_GATE follows CPODE.S.1.1			
CPODE.R.9	Horizontal edge of PODE_GATE_Region cut OD vertical edge is not allowed. Definition of PODE_GATE_Region: A region formed by {PODE_GATE [INTERACT CPODE] SIZING up/down 0.028 μm in horizontal direction}			
CPODE.R.10	Horizontal edge of {CPODE NOT Checked_PODE_GATE} must inside CPO [width = 0.016 μm] or fully abut CPO [width = 0.100 μm] Definition of Checked_PODE_GATE follows CPODE.S.1.1			
CPODE.R.11	CPODE outside FB_9 is not allowed			
CPODE.R.13.1	CPODE_Group overlap Connected_MD or MP is not allowed Definition of Connected_MD: {MD NOT CMD} interact VC or MP Definition of CPODE_Group: {{{CPODE NOT Checked_PODE_GATE} SIZING up/down 0.0275 μm in horizontal direction} SIZING down/up 0.0055 μm in horizontal direction} Definition of Checked_PODE_GATE follows CPODE.S.1.1			

CPODE

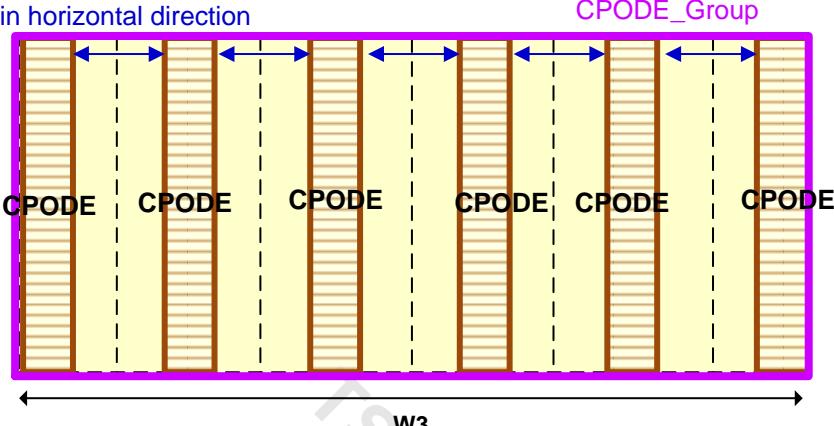


Definition of PODE_GATE_Region:

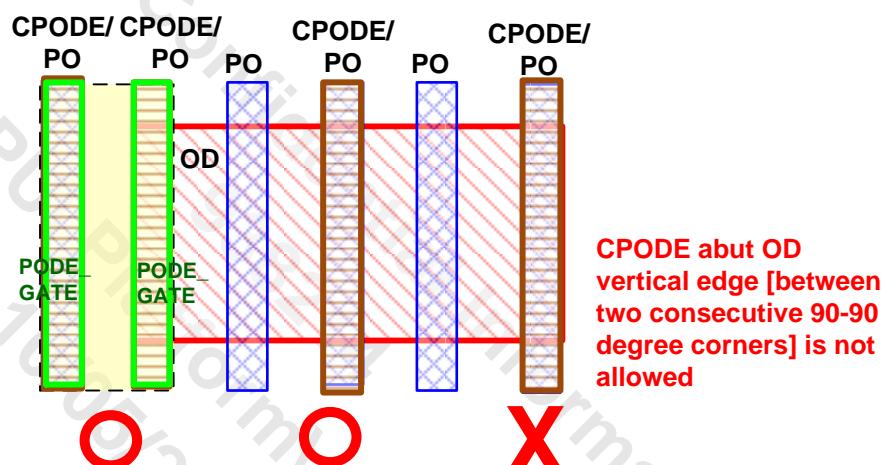
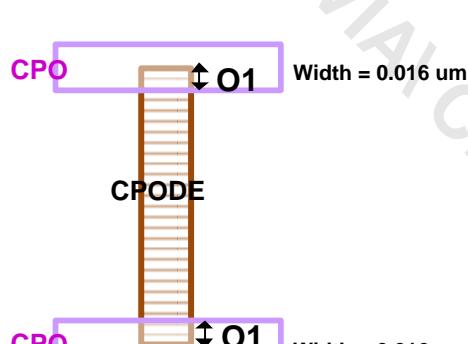
A region formed by {PODE_GATE [INTERACT CPODE] SIZING up/down 0.028 μm in horizontal direction}



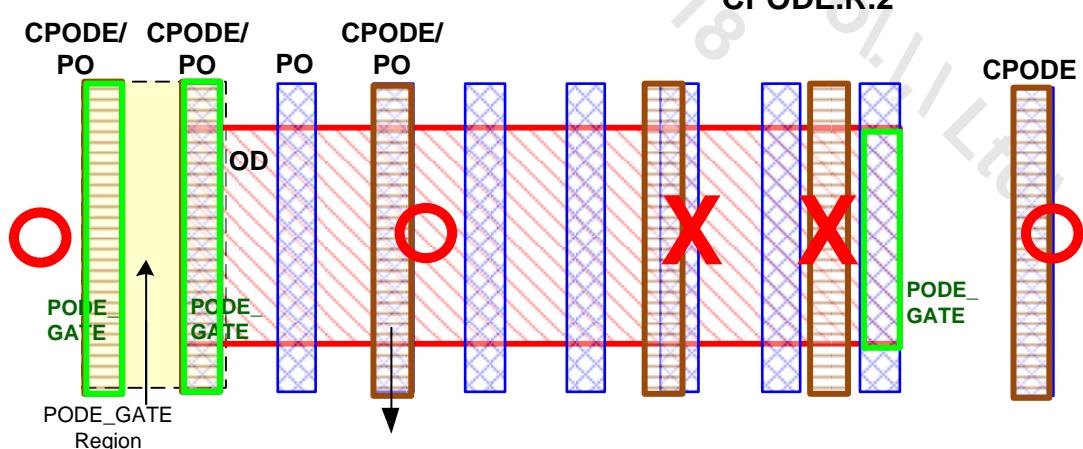
SIZING up/down 0.0245 μ m
in horizontal direction



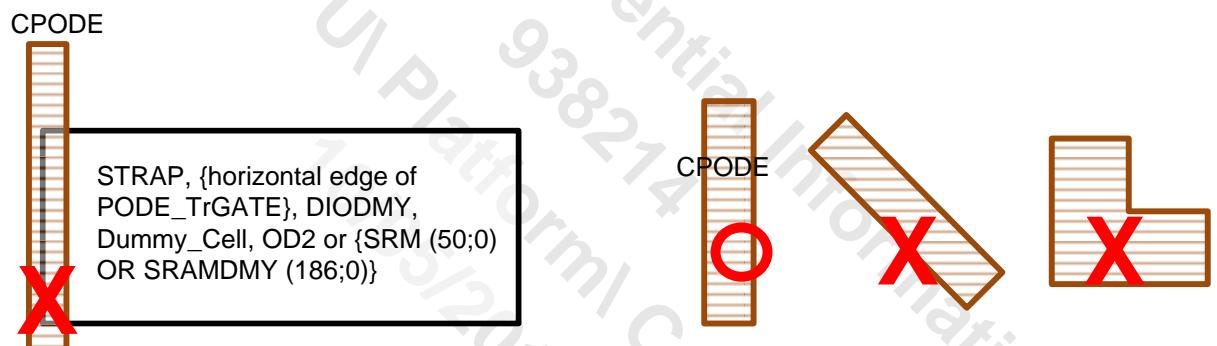
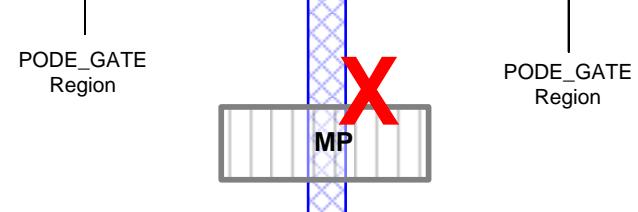
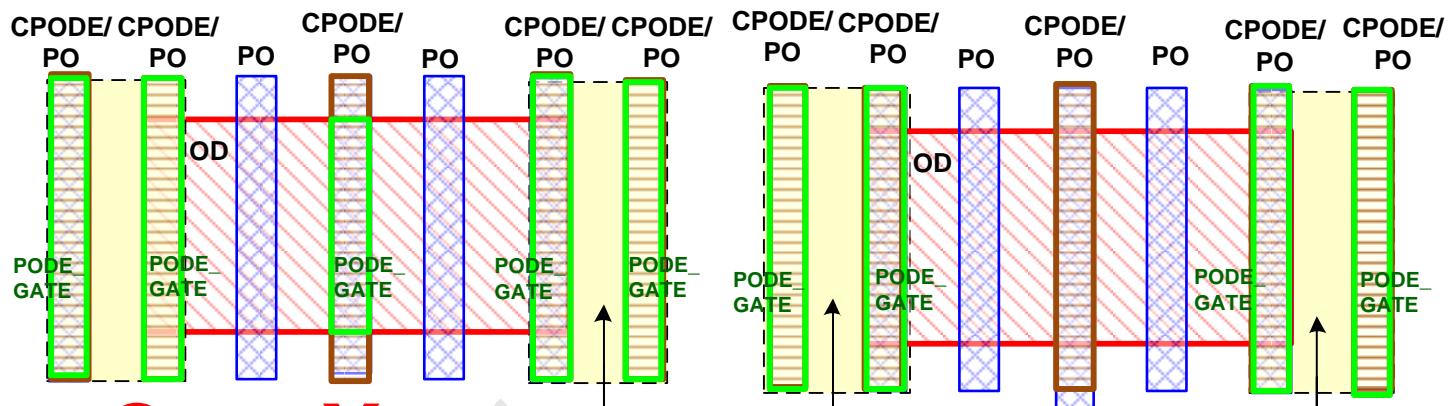
CPODE.W.3



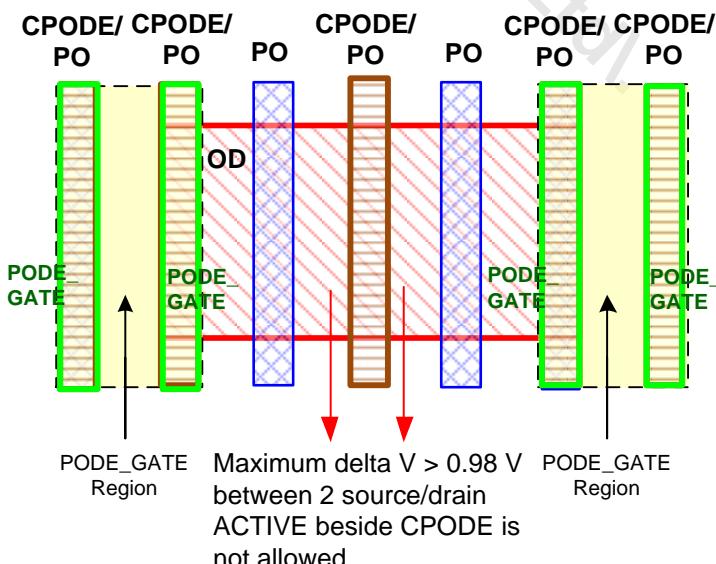
CPODE.R.2

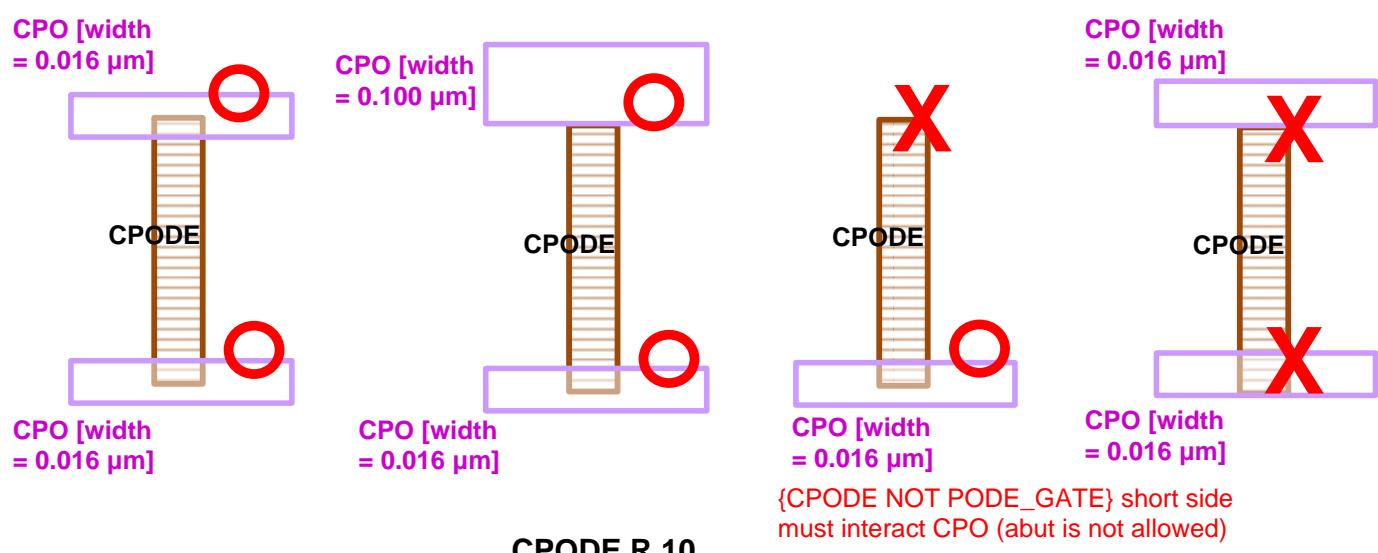
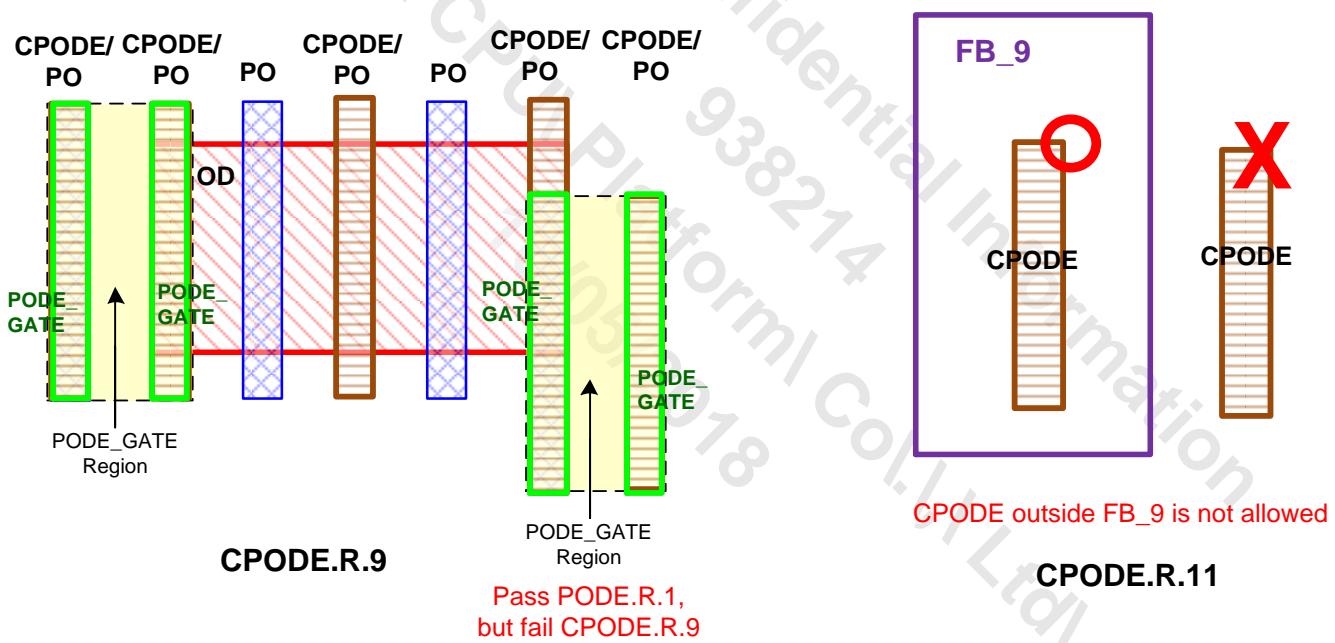
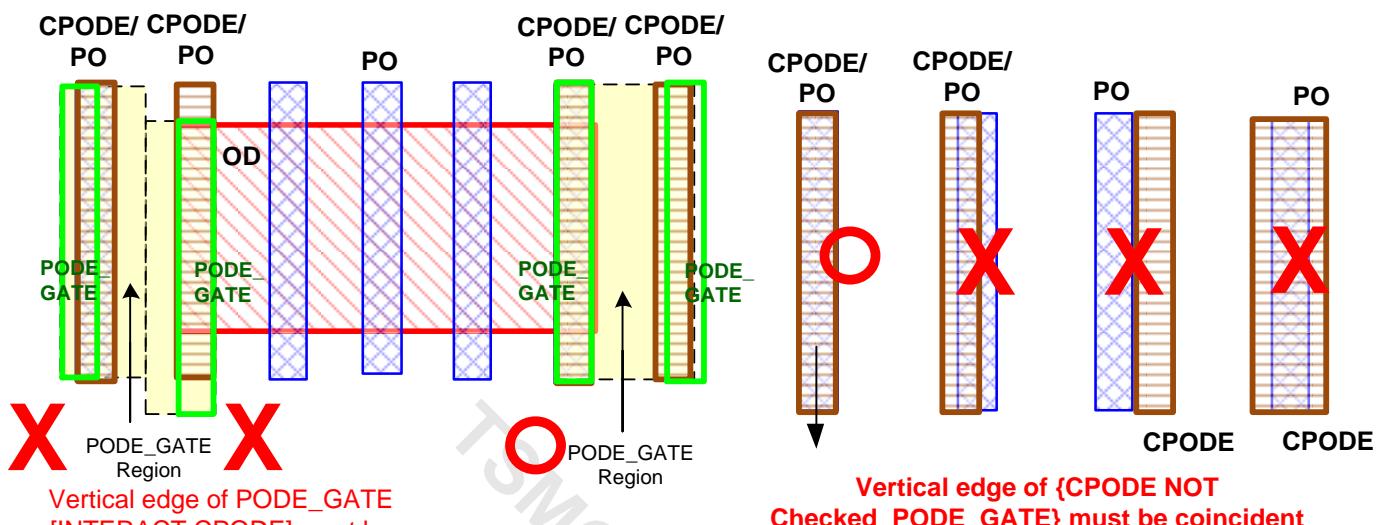


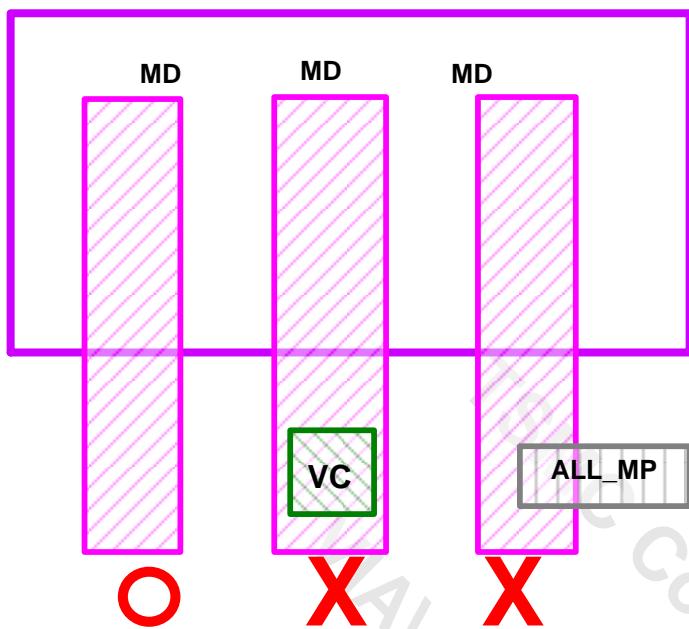
CPODE.R.1



Interact is not allowed.



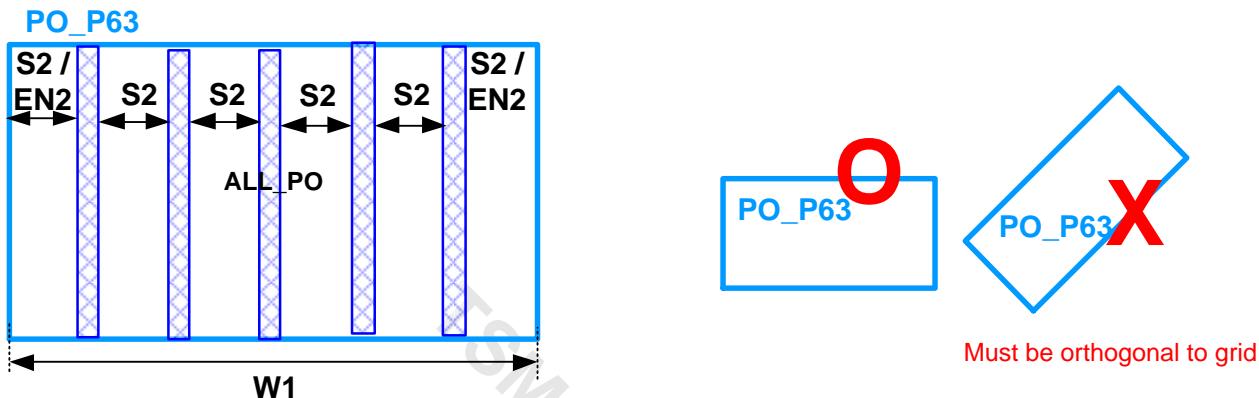


CPODE_Group**CPODE.R.13.1**

4.5.18 Poly Pitch 0.063 μm (PO_P63) Layout Rules

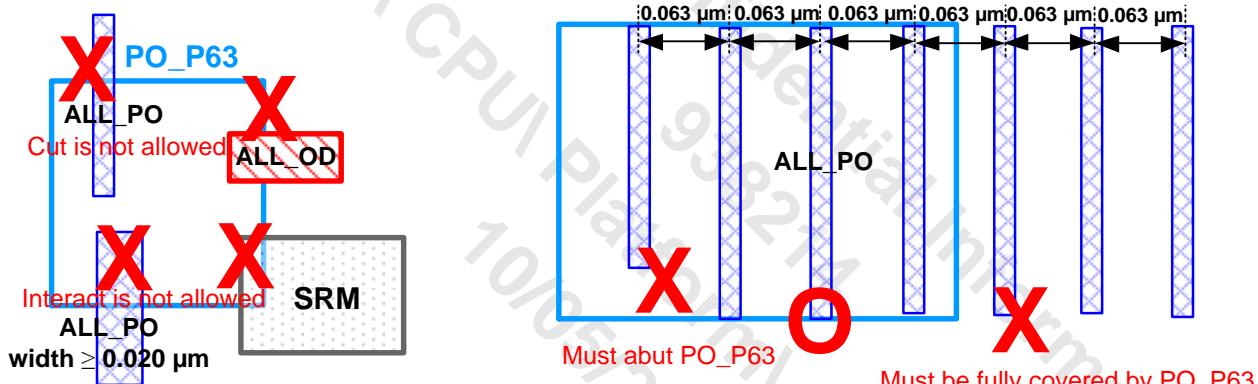
PO_P63 (CAD layer: 105;5) is a tape-out layers for poly pitch 0.063 μm layout.

Rule No.	Description	Label	Op.	Rule
PO_P63.W.1	Width in horizontal direction	W1	≥	0.6300
PO_P63.S.2	Empty space of ALL_PO [INSIDE PO_P63] DRC flags {{PO_P63 NOT ALL_PO} SIZING down/up 0.058 μm}	S2	≤	0.1160
PO_P63.EN.2	Enclosure of ALL_PO in horizontal direction	EN2	≈	0.0260
PO_P63.R.1	PO_P63 must be orthogonal to grid			
PO_P63.R.2	ALL_PO, ALL_OD cut PO_P63 is not allowed			
PO_P63.R.3	ALL_PO [width ≥ 0.020 μm], SRM interact PO_P63 is not allowed			
PO_P63.R.5	{ALL_PO OR BPO_V} [width ≤ 0.011 μm, centerline space = 0.063 μm] must be fully covered by PO_P63			
PO_P63.R.7	{ALL_PO OR BPO_V} [INSIDE PO_P63] line-end must abut PO_P63			
PO_P63.R.8	ALL_PO [INTERACT PO_P63] must be inside PO_P63			
PO_P63.R.9	PO_P63 [INTERACT FB_8] must be drawn identical to {FB_8 SIZING 0.100 μm in vertical direction} or {FB_8 SIZING 0.150 μm in vertical direction}			
PO_P63.R.10	PO_P63 must be inside FB_1 or {FB_8 SIZING 0.150 μm in vertical direction}			

PO_P63

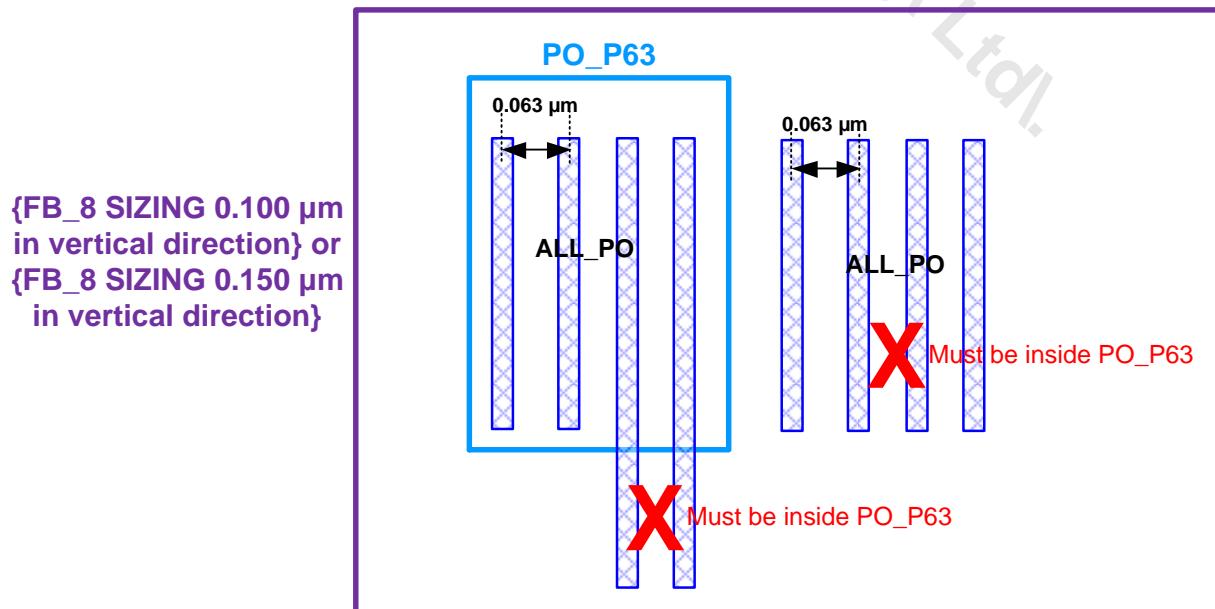
PO_P63.W.1 / PO_P63.S.2 / PO_P63.EN.2

PO_P63.R.1

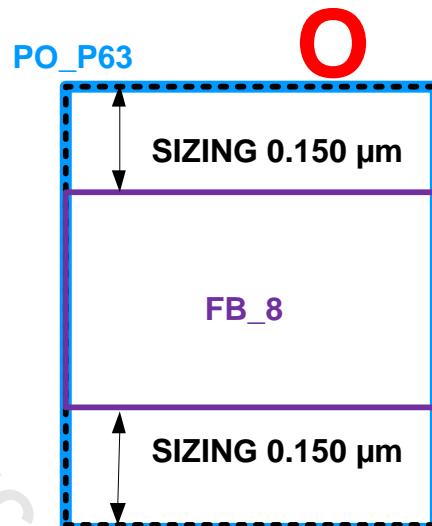
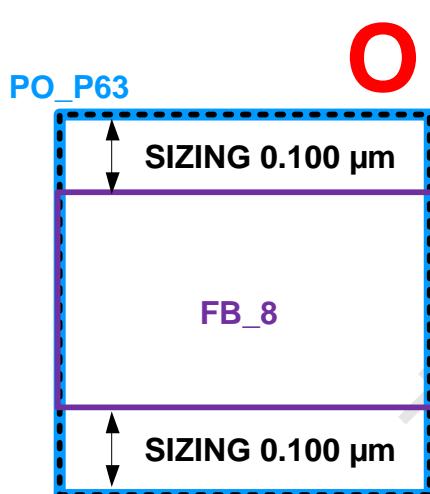


PO_P63.R.2 / PO_P63.R.3

PO_P63.R.5 / PO_P63.R.7

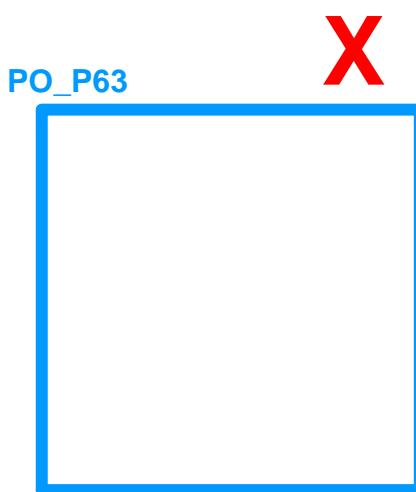
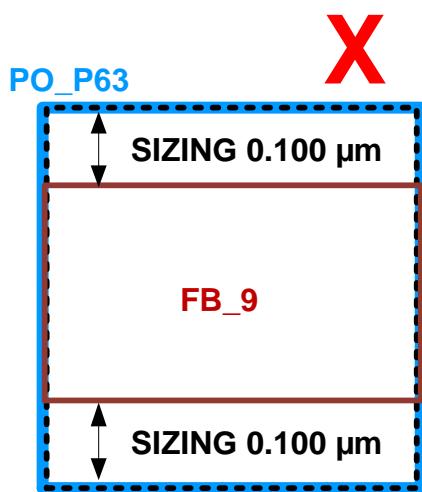
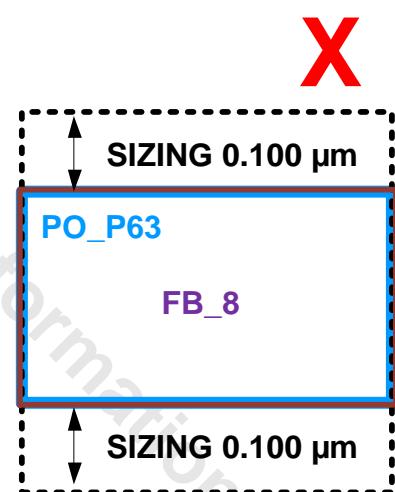
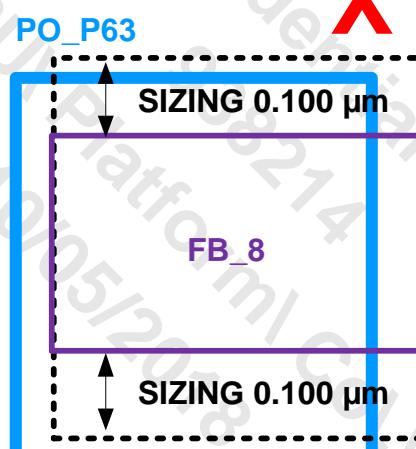
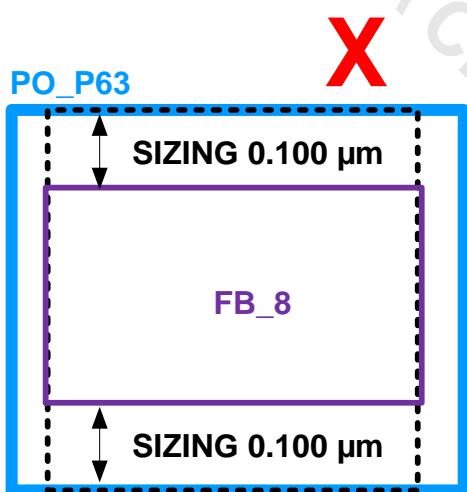


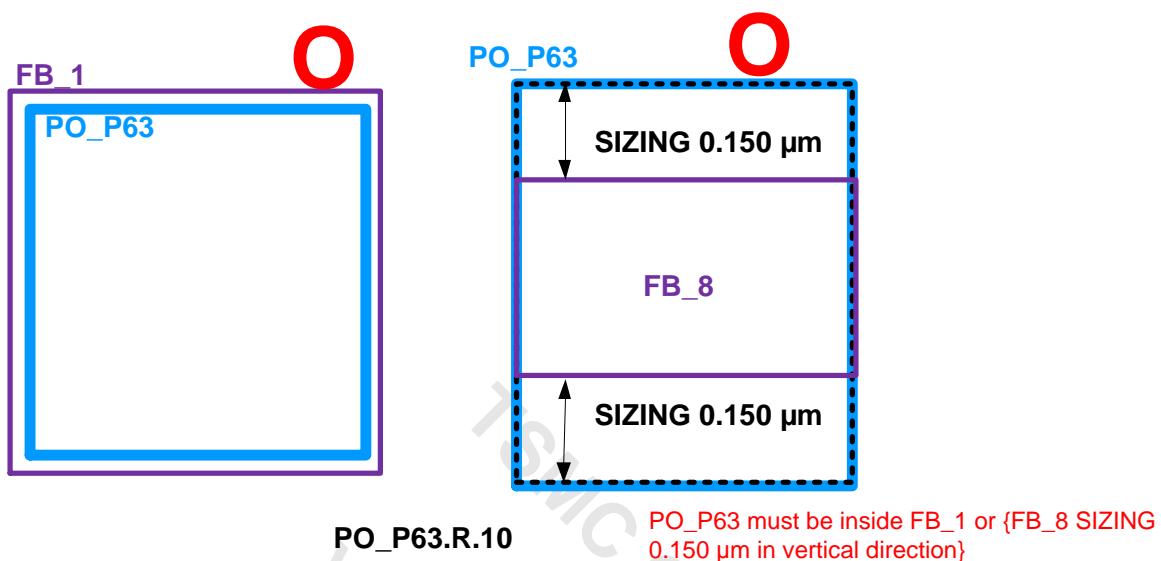
PO_P63.R.8



PO_P63.R.9

PO_P63 must be drawn identical to
{FB_8 SIZING 0.100 µm in vertical direction} or
{FB_8 SIZING 0.150 µm in vertical direction}

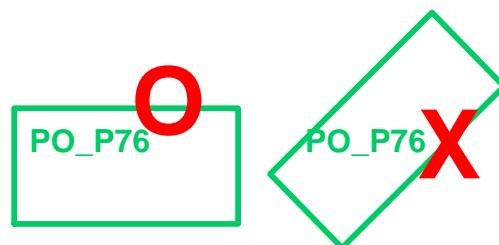
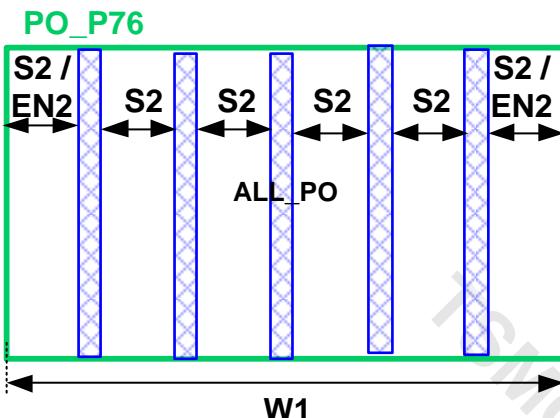




4.5.19 Poly Pitch 0.076 μm (PO_P76) Layout Rules

PO_P76 (CAD layer: 105;6) is a tape-out layers for poly pitch 0.076 μm layout.

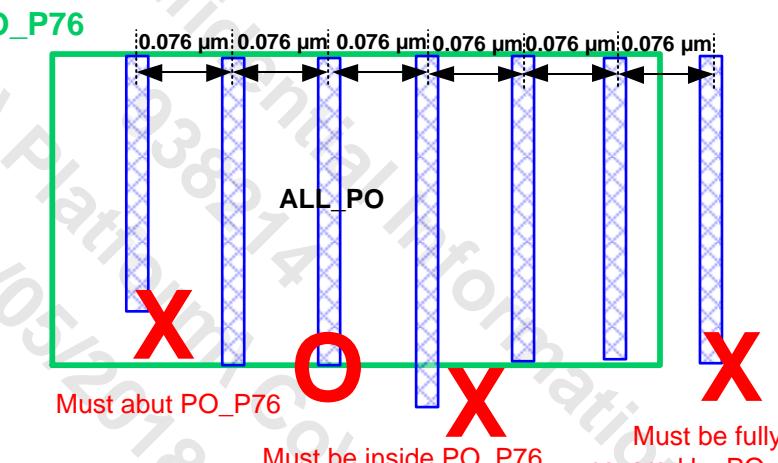
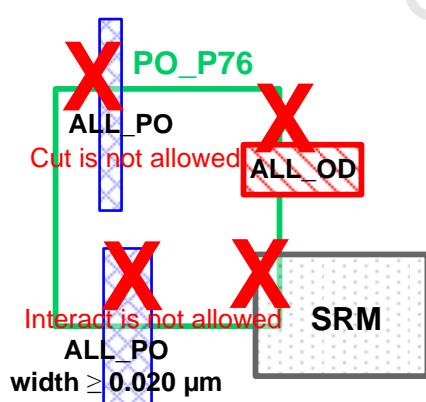
Rule No.	Description	Label	Op.	Rule
PO_P76.W.1	Width in horizontal direction	W1	\geq	0.7600
PO_P76.S.2	Empty space of ALL_PO [INSIDE PO_P76] DRC flags {{PO_P76 NOT ALL_PO} SIZING down/up 0.058 μm}	S2	\leq	0.1160
PO_P76.EN.2	Enclosure of ALL_PO in horizontal direction	EN2	\geq	0.0325
PO_P76.R.1	PO_P76 must be orthogonal to grid			
PO_P76.R.2	ALL_PO, ALL_OD cut PO_P76 is not allowed			
PO_P76.R.3	ALL_PO [width \geq 0.020 μm], SRM interact PO_P76 is not allowed			
PO_P76.R.5	ALL_PO [width \leq 0.011 μm, centerline space = 0.076 μm] must be fully covered by PO_P76			
PO_P76.R.7	ALL_PO [INSIDE PO_P76] line-end must abut PO_P76			
PO_P76.R.8	ALL_PO [INTERACT PO_P76] must be inside PO_P76			
PO_P76.R.9	PO_P76 must be inside FB_1			

PO_P76

Must be orthogonal to grid

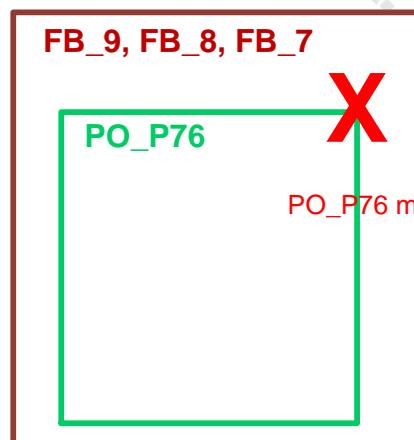
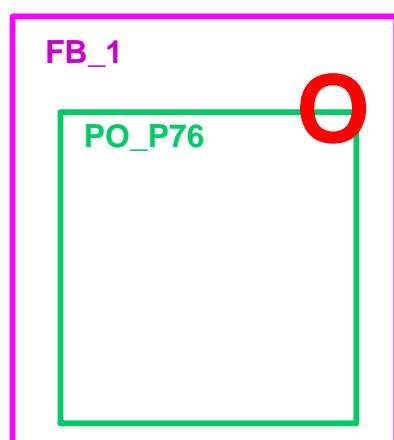
PO_P76.W.1 / PO_P76.S.2 / PO_P76.EN.2

PO_P76.R.1



PO_P76.R.2 / PO_P76.R.3

PO_P76.R.5 / PO_P76.R.7/PO_P76.R.8



PO_P76.R.9

4.5.20 Poly (PO) Layout Rules

ALL_PO = {PO OR SR_DPO}

Rule No.	Description	Label	Op.	Rule
PO.W.1	Width of ALL_PO	W1	\geq	0.0080
PO.W.1.1	Width of ALL_PO	W1A	=	0.0080, 0.0110, 0.0200, 0.0360, 0.0720 ~ 0.2400
PO.W.2	Width of ALL_PO [INTERACT OD2] (Except OD18_12, OD15_12, or following conditions: 1. {Dummy_Cell NOT DC_7})	W2	\geq	0.0860
PO.W.3	Channel length of core device (Except BLK_WF, or following conditions: 1. GATE [INTERACT CPODE])	W3	=	0.0080, 0.0110, 0.0200, 0.0360, 0.0720 ~ 0.2400
PO.W.4.1	Channel length of 1.8V MOS ({GATE AND {OD_18 NOT {OD18_15 OR OD18_12}}}) (Except HIA_DUMMY, IBJTDMY, DIODMY, or following conditions: 1. {STRAP NOT VAR})	W4A	=	0.1350 ~ 0.2400
PO.W.5	Maximum width of ALL_PO	W5	\leq	0.2400
PO.W.11	1st PO width rule (beside ALL_PO width = 0.008 μm): Width of ALL_PO neighboring to ALL_PO [width = 0.008 μm , space to ALL_PO < 0.070 μm]	W11	=	0.0080, 0.0110
PO.W.11.1	1st PO width rule (beside ALL_PO width = 0.011 μm): Width of ALL_PO neighboring to ALL_PO [width = 0.011 μm , space to ALL_PO < 0.070 μm]	W11	=	0.0080, 0.0110
PO.W.11.3	1st PO width rule (beside ALL_PO width = 0.020 μm): Width of ALL_PO neighboring to ALL_PO [width = 0.020 μm , space to ALL_PO < 0.094 μm]	W11	=	0.0200, 0.0360
PO.W.11.7	1st PO width rule (beside ALL_PO width = 0.036 μm): Width of ALL_PO neighboring to ALL_PO [width = 0.036 μm , space to ALL_PO < 0.094 μm]	W11	=	0.0200, 0.0360
PO.W.12	Width of ALL_PO [in horizontal and outside OD direction] neighboring to TrGATE [channel length = 0.008 μm , ALL_PO to TrGATE space < 0.070 μm]	W12	=	0.0080, 0.0110
PO.W.12.1	Width of ALL_PO [in horizontal and outside OD direction] neighboring to TrGATE [channel length = 0.011 μm , ALL_PO to TrGATE space < 0.070 μm]	W12	=	0.0110
PO.W.12.3	Width of ALL_PO [in horizontal and outside OD direction] neighboring to TrGATE [channel length = 0.020 μm , ALL_PO to TrGATE space < 0.094 μm]	W12	=	0.0200
PO.W.12.4	Width of ALL_PO [in horizontal and outside OD direction] neighboring to TrGATE [channel length = 0.036 μm , ALL_PO to TrGATE space < 0.094 μm]	W12	=	0.0360
PO.W.13	Width of ALL_PO [in horizontal and outside OD direction] neighboring to LAST TrGATE [channel length \geq 0.072 μm , ALL_PO to LAST TrGATE space = 0.094 μm] (Except SR_ESD, BLK_WF) Definition of LAST TrGATE: TrGATE abut the same S/D with PODE_GATE [OD on LAST TrGATE extension \leq 0.334 μm]	W13	\geq	0.0720

Rule No.	Description	Label	Op.	Rule
PO.W.13.1	Width of ALL_PO [in horizontal and outside OD direction] neighboring to LAST TrGATE [INSIDE OD2, ALL_PO to LAST TrGATE space = 0.094 μm] (Except SR_ESD, OD18_12, OD15_12) Definition of LAST TrGATE: TrGATE abut the same S/D with PODE_GATE [OD on LAST TrGATE extension ≤ 0.334 μm]	W13	≥	0.0860
PO.W.13.2	Width of ALL_PO [in horizontal and outside OD direction] neighboring to LAST TrGATE [INSIDE {OD18_12 OR OD15_12}, ALL_PO to LAST TrGATE space = 0.094 μm] (Except SR_ESD) Definition of LAST TrGATE: TrGATE abut the same S/D with PODE_GATE [OD on LAST TrGATE extension ≤ 0.334 μm]	W13	≥	0.0720
PO.W.14	Width of DRAW_Fine_PO_Group [INTERACT MOS] in horizontal direction Definition of DRAW_Fine_PO_Group: {Fine_PO_Group NOT DC_Mandrel} Definition of Fine_PO_Group: ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.035 μm as group	W14	≥	2
PO.W.14.1	Width of Fine_PO_Group_Region [INTERACT MOS] in vertical direction Definition of Fine_PO_Group_Region follows PO.A.7 DRC merged small inner holes (area < 0.5 μm ²) of Fine_PO_Group_Region	W14A	≥	2
PO.S.1	Space of ALL_PO	S1	≥	0.0460
PO.S.1.0.1	Space of ALL_PO [INSIDE PO_P63]	S1	≥	0.0520
PO.S.1.0.2	Space of ALL_PO [INSIDE PO_P76]	S1	≥	0.0650
PO.S.1.1	Space of ALL_PO [width ≥ 0.020 μm] to ALL_PO	S1A	≥	0.0800
PO.S.1.2	Centerline space of ALL_PO [width ≤ 0.011 μm] in horizontal direction (Except PO_P63, PO_P76, or following conditions: 1. centerline space > 0.100 μm)	S1B	=	0.0570
PO.S.1.2.2	Centerline space of ALL_PO [width ≤ 0.011 μm] in horizontal direction [INSIDE PO_P63] (Except following conditions: 1. centerline space > 0.100 μm)	S1B	=	0.0630
PO.S.1.2.3	Centerline space of ALL_PO [width ≤ 0.011 μm] in horizontal direction [INSIDE PO_P76] (Except following conditions: 1. centerline space > 0.100 μm)	S1B	=	0.0760
PO.S.1.3	Centerline space of ALL_PO [width = 0.020 μm] in horizontal direction (Except following conditions: 1. centerline space > 0.100 μm)	S1B	=	0.1000
PO.S.2	Space of ALL_PO [width ≥ 0.072 μm] to ALL_PO [PRL > -0.094 μm]	S2	≥	0.0940
PO.S.2.2	Space of ALL_PO [NOT OUTSIDE OD2] to ALL_PO (Except Dummy_Cell)	S2B	≥	0.0940
PO.S.3	Space of short side of {ALL_PO [width = 0.008/0.011 μm] OR BPO_V [length = 0.100 μm]} to {ALL_PO OR BPO_V [length = 0.100 μm]} [PRL > -0.150 μm]	S3	≥	0.2000
PO.S.3.1	Space of short side of {ALL_PO [width = 0.008/0.011 μm] OR BPO_V [length = 0.100 μm]} [PRL > -0.160 μm]	S3A	≥	0.2700

Rule No.	Description	Label	Op.	Rule
PO.S.3.2	Space of short side of PO [width = 0.008/0.011 μm] [PRL > -0.180 μm] (Except following conditions: 1. short side of PO fully abut SR_DPO, 2. PO [INTERACT SR_DPO_WAIVE] short side space = 0.240~0.269 μm) Definition of SR_DPO_WAIVE follows VT.R.5	S3B	\geq	0.2700
PO.S.4	Space of short side of ALL_PO [0.020 μm \leq width \leq 0.036 μm] to ALL_PO [PRL > -0.080 μm]	S4	\geq	0.1100
PO.S.5	Space of long side of ALL_PO [0.020 μm \leq width \leq 0.036 μm] to ALL_PO [PRL > -0.110 μm]	S5	\geq	0.0800
PO.S.13.1	TrGATE [NOT INSIDE {PO_P63 OR PO_P76}] to 1st PO space rule (Lg = 0.008 μm): Space of {{TrGATE [NOT INSIDE {PO_P63 OR PO_P76}] SIZING 0.036 μm } AND PO} to ALL_PO of core device [channel length = 0.008 μm in horizontal direction, centerline space = 0.057 μm]	S13	=	0.0475 ~ 0.0490
PO.S.13.2	TrGATE to 1st PO [NOT INSIDE {PO_P63 OR PO_P76}] space rule (Lg = 0.011 μm): Space of {{TrGATE [NOT INSIDE {PO_P63 OR PO_P76}] SIZING 0.036 μm } AND PO} to ALL_PO of core device [channel length = 0.011 μm , centerline space = 0.057 μm]	S13	=	0.0460 ~ 0.0475
PO.S.13.5	TrGATE to 1st PO space rule (Lg = 0.020 μm): Space of {{TrGATE SIZING 0.036 μm } AND PO} to ALL_PO of core device [channel length = 0.020 μm]	S13	=	0.0800
PO.S.13.6	TrGATE to 1st PO space rule (Lg = 0.036 μm): Space of {{TrGATE SIZING 0.036 μm } AND PO} to ALL_PO of core device [channel length = 0.036 μm]	S13	=	0.0800
PO.S.14	TrGATE to 1st PO space rule (Lg \geq 0.072 μm): Space of {{TrGATE SIZING 0.060 μm } AND PO} to poly at both sides ALL_PO [channel length \geq 0.072 μm] (Except SR_ESD)	S14	=	0.0940
PO.S.16	TrGATE to 2nd PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE of core device [0.008 μm \leq channel length \leq 0.011 μm] to the second ALL_PO in horizontal and outside OD direction (The second PO is required to be placed beside the TrGATE.) (Except PO_P63, and PO_P76)	S16	=	0.1030 ~ 0.1060
PO.S.16.1	TrGATE to 2nd PO space rule (0.020 μm \leq Lg \leq 0.036 μm): Space of TrGATE of core device [0.020 μm \leq channel length \leq 0.036 μm] to the second ALL_PO in horizontal and outside OD direction (The second PO is required to be placed beside the TrGATE.)	S16	\leq	0.1960
PO.S.16.2	TrGATE to 2nd PO space rule (Lg \geq 0.072 μm): Space of TrGATE of core device [channel length \geq 0.072 μm] to the second ALL_PO in horizontal and outside OD direction. (The second PO is required to be placed beside the TrGATE.) (Except SR_ESD)	S16	\leq	0.4280
PO.S.16.3	TrGATE to 3rd PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE of core device [0.008 μm \leq channel length \leq 0.011 μm] to the third ALL_PO in horizontal and outside OD direction (The third PO is required to be placed beside the TrGATE.) (Except PO_P63, and PO_P76)	S16C	=	0.1600 ~ 0.1630
PO.S.16.4	TrGATE to 3rd PO space rule (0.020 μm \leq Lg \leq 0.036 μm): Space of TrGATE of core device [0.020 μm \leq channel length \leq 0.036 μm] to the third ALL_PO in horizontal and outside OD direction (The third PO is required to be placed beside the TrGATE.)	S16C	\leq	0.3120
PO.S.16.5	TrGATE to 4th PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE of core device [0.008 μm \leq channel length \leq 0.011 μm] to the fourth ALL_PO in horizontal and outside OD direction (The fourth PO is required to be placed beside the TrGATE.) (Except PO_P63, and PO_P76)	S16E	=	0.2170 ~ 0.2200

Rule No.	Description	Label	Op.	Rule
PO.S.17	Space of FIELD ALL_PO to ALL_OD (Except following conditions: 1. poly jog \leq 0.002 μm)	S17	\geq	0.0460
PO.S.17.1	Space of FIELD ALL_PO [width \geq 0.020 μm] to ALL_OD	S17A	\geq	0.0530
PO.S.18.1	TrGATE [INSIDE PO_P63] to 1st PO space rule (Lg = 0.008 μm): Space of {{TrGATE [INSIDE PO_P63] SIZING 0.036 μm } AND PO} to ALL_PO of core device [channel length = 0.008 μm , centerline space = 0.063 μm]	S18A	=	0.0535 ~ 0.0550
PO.S.18.2	TrGATE [INSIDE PO_P63] to 1st PO space rule (Lg = 0.011 μm): Space of {{TrGATE [INSIDE PO_P63] SIZING 0.036 μm } AND PO} to ALL_PO of core device [channel length = 0.011 μm , centerline space = 0.063 μm]	S18B	=	0.0520 ~ 0.0535
PO.S.18.3	TrGATE [INSIDE PO_P63] to 2nd PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE [INSIDE PO_P63] of core device [0.008 μm \leq channel length \leq 0.011 μm] to the second ALL_PO in horizontal and outside OD direction (The second PO is required to be placed beside the TrGATE.)	S18C	=	0.1150 ~ 0.1180
PO.S.18.4	TrGATE [INSIDE PO_P63] to 3rd PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE [INSIDE PO_P63] of core device [0.008 μm \leq channel length \leq 0.011 μm] to the third ALL_PO in horizontal and outside OD direction (The third PO is required to be placed beside the TrGATE.)	S18D	=	0.1780 ~ 0.1810
PO.S.18.5	TrGATE [INSIDE PO_P63] to 4th PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE [INSIDE PO_P63] of core device [0.008 μm \leq channel length \leq 0.011 μm] to the fourth ALL_PO in horizontal and outside OD direction (The fourth PO is required to be placed beside the TrGATE.)	S18E	=	0.2410 ~ 0.2440
PO.S.19.1	TrGATE [INSIDE PO_P76] to 1st PO space rule (Lg = 0.008 μm): Space of {{TrGATE [INSIDE PO_P76] SIZING 0.036 μm } AND PO} to ALL_PO of core device [channel length = 0.008 μm , centerline space = 0.076 μm]	S19A	=	0.0665 ~ 0.0680
PO.S.19.2	TrGATE [INSIDE PO_P76] to 1st PO space rule (Lg = 0.011 μm): Space of {{TrGATE [INSIDE PO_P76] SIZING 0.036 μm } AND PO} to ALL_PO of core device [channel length = 0.011 μm , centerline space = 0.076 μm]	S19B	=	0.0650 ~ 0.0665
PO.S.19.3	TrGATE [INSIDE PO_P76] to 2nd PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE [INSIDE PO_P76] of core device [0.008 μm \leq channel length \leq 0.011 μm] to the second ALL_PO in horizontal and outside OD direction (The second PO is required to be placed beside the TrGATE.)	S19C	=	0.1410 ~ 0.1440
PO.S.19.4	TrGATE [INSIDE PO_P76] to 3rd PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE [INSIDE PO_P76] of core device [0.008 μm \leq channel length \leq 0.011 μm] to the third ALL_PO in horizontal and outside OD direction (The third PO is required to be placed beside the TrGATE.)	S19D	=	0.2170 ~ 0.2200
PO.S.19.5	TrGATE [INSIDE PO_P76] to 4th PO space rule (0.008 μm \leq Lg \leq 0.011 μm): Space of TrGATE [INSIDE PO_P76] of core device [0.008 μm \leq channel length \leq 0.011 μm] to the fourth ALL_PO in horizontal and outside OD direction (The fourth PO is required to be placed beside the TrGATE.)	S19E	=	0.2930 ~ 0.2960
PO.S.22.1.1	Forbidden space of ALL_PO [width = 0.008 μm , centerline space = 0.057 μm] to ALL_PO in horizontal direction (Except PO_P63, PO_P76, DC_PO36, DC_Mandrel)	S22	=	0.0480 ~ 0.0485, 0.0495 ~ 0.1795

Rule No.	Description	Label	Op.	Rule
PO.S.22.1.1.1	Forbidden space of ALL_PO [width = 0.008 μm, INSIDE PO_P63] to ALL_PO in horizontal direction	S22	=	0.0540 ~ 0.0545, 0.0555 ~ 0.1795
PO.S.22.1.1.2	Forbidden space of ALL_PO [width = 0.008 μm, INSIDE PO_P76] to ALL_PO in horizontal direction	S22	=	0.0670 ~ 0.0675, 0.0685 ~ 0.1795
PO.S.22.1.2	Forbidden space of ALL_PO [width = 0.011 μm, centerline space = 0.057 μm] to ALL_PO in horizontal direction (Except PO_P63, PO_P76, DC_PO36, DC_Mandrel)	S22	=	0.0465 ~ 0.0470, 0.0480 ~ 0.1795
PO.S.22.1.2.1	Forbidden space of ALL_PO [width = 0.011 μm, INSIDE PO_P63] to ALL_PO in horizontal direction	S22	=	0.0525 ~ 0.0530, 0.0540 ~ 0.1795
PO.S.22.1.2.2	Forbidden space of ALL_PO [width = 0.011 μm, INSIDE PO_P76] to ALL_PO in horizontal direction	S22	=	0.0655 ~ 0.0660, 0.0670 ~ 0.1795
PO.S.22.1.3	Forbidden space of DRAW_Fine_PO_Group in horizontal direction [PRL > 0.300 μm] (Except SEALRING_ALL) Definition of DRAW_Fine_PO_Group follows PO.W.14	S22A3	=	0.4010 ~ 0.5500
PO.S.22.1.4	Forbidden space of DRAW_Fine_PO_Group in vertical direction [PRL > 0.300 μm] (Except SEALRING_ALL) Definition of DRAW_Fine_PO_Group follows PO.W.14	S22A4	=	0.5000 ~ 0.6000
PO.S.22.2	Forbidden space of ALL_PO [width = 0.020 μm] to ALL_PO [width ≥ 0.020 μm] in horizontal direction	S22	=	0.0805 ~ 0.2060, 0.2460 ~ 0.2860
PO.S.23.3	Space of ALL_PO [width = 0.020 μm and one side poly space > 0.080 μm in horizontal direction] to ALL_PO in horizontal direction	S23	=	0.0800
PO.S.23.5	Space of ALL_PO [width = 0.036 μm and one side poly space > 0.080 μm in horizontal direction] to ALL_PO in horizontal direction	S23	=	0.0800
PO.S.23.7	Space of ALL_PO [0.072 μm ≤ width < 0.162 μm and one side poly space > 0.094 μm in horizontal direction] to ALL_PO in horizontal direction (Except SR_ESD)	S23	=	0.0940
PO.S.24	Space of ALL_PO jog [width ≤ 0.002 μm] to TrGATE in vertical direction [PRL > -0.049 μm]	S24	≥	0.0320
PO.S.25	Empty space of {ALL_PO NOT CPO} (Except RH_TNB, NWDMY, TCDDMY, ICOVL_SINGLE, or following conditions: 1. {SEALRING_ALL SIZING 0.500 μm}, 2. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags {{CHIP NOT {ALL_PO NOT CPO}} SIZING down/up 0.500 μm}	S25	≤	1
PO.S.25®	Empty space of {ALL_PO NOT CPO} (Except RH_TNB, NWDMY, TCDDMY, ICOVL_SINGLE, or following conditions: 1. {SEALRING_ALL SIZING 0.450 μm}, 2. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags {{CHIP NOT {ALL_PO NOT CPO}} SIZING down/up 0.450 μm}	S25	≤	0.9000
PO.S.25.3	Empty space of {ALL_PO NOT CPO} [INSIDE RH_TNB] DRC flags {{CHIP AND RH_TNB} NOT {ALL_PO NOT CPO}} SIZING down/up 1 μm	S25	≤	2
PO.S.25.4	Empty space of {ALL_PO NOT CPO} [INSIDE NWDMY] DRC flags {{Chip AND NWDMY} NOT {ALL_PO NOT CPO}} SIZING down/up 2.5 μm	S25	≤	5
PO.S.26	Maximum space of ALL_PO [INTERACT ALL_OD, in horizontal and inside OD direction] (Except SR_ESD)	S26	≤	0.0940
PO.S.27	Space of ALL_PO [width < 0.036 μm] to ALL_PO [width ≥ 0.100 μm] (Except Dummy_Cell)	S27	≥	0.2000

Rule No.	Description	Label	Op.	Rule
PO.EX.3	ALL_PO extension on ALL_OD in vertical direction (Extension < 0 μm is not allowed)	EX3	≥	0.0320
PO.EX.3.2	ALL_PO [width ≥ 0.020 μm] extension on ALL_OD in vertical direction (Except DC5_2 (257;52)) (Extension < 0 μm is not allowed)	EX3B	≥	0.0610
PO.EX.7	ALL_PO jog [width ≤ 0.002 μm] extension on TrGATE in vertical direction [PRL > -0.049 μm]	EX7	≥	0.0320
PO.EN.1	DRAW_Fine_PO_Group enclosure of OD [INTERACT MOS] (Except BLK_WF) Definition of DRAW_Fine_PO_Group follows PO.W.14	EN1	≥	0.2200
PO.EN.1.1	DRAW_Fine_PO_Group enclosure of OD [INTERACT MOS] in horizontal direction [PRL > - 0.220 μm] (Except BLK_WF) Definition of DRAW_Fine_PO_Group follows PO.W.14	EN1A	≥	0.2835
PO.EN.1.3	DRAW_Fine_PO_Group enclosure of OD [INTERACT MOS] in horizontal direction [PRL > - 0.220 μm, INSIDE PO_P63] Definition of DRAW_Fine_PO_Group: {Fine_PO_Group NOT DC_Mandrel} Definition of Fine_PO_Group: ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.030 μm as group	EN1C	≥	0.3135
PO.EN.1.4	DRAW_Fine_PO_Group enclosure of OD [INTERACT MOS] in horizontal direction [PRL > - 0.220 μm, INSIDE PO_P76] Definition of DRAW_Fine_PO_Group: {Fine_PO_Group NOT DC_Mandrel} Definition of Fine_PO_Group: ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.035 μm as group	EN1C	≥	0.3785
PO.L.2	Length of ALL_PO	L2	≥	0.2090
PO.L.2.1	Length of ALL_PO [width ≤ 0.011 μm]	L2A	≥	0.2200
PO.L.2.2	Length of ALL_PO [0.020 μm ≤ width ≤ 0.036 μm]	L2B	≥	0.2470
PO.L.2.3	Length of {SR_DPO NOT CPO [width = 0.100 μm]}	L2C	≥	0.1000
PO.L.3	Length of PO jog [jog width ≤ 0.002 μm and OUTSIDE CPO]	L3	≥	0.2020
PO.L.3.1	Length of SR_DPO jog [jog width ≤ 0.002 μm and OUTSIDE CPO]	L3A	≥	0.1460
PO.L.4	Maximum length of {PO NOT {CPO OR CPO_SRAM}} [INTERACT OD]	L4	≤	10
PO.L.4.1	Maximum length of {PO [width ≥ 0.072 μm] NOT CPO} [INTERACT OD] (Except IBJTDY)	L4A	≤	1.2
PO.L.4.3	Maximum length of {PO [width = 0.036 μm] NOT CPO} [INTERACT OD]	L4C	≤	1.5
PO.L.5	Horizontal edge length between two consecutive 270-270 degree corners of {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.0245 μm} (10 polys for merged U-shape) (Except PO_P63, PO_P76)	L5	≥	0.6160
PO.L.5.0.1	Horizontal edge length between two consecutive 270-270 degree corners of {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.0275 μm} [INSIDE PO_P63] (10 polys for merged U-shape)	L5	≥	0.6820
PO.L.5.0.2	Horizontal edge length between two consecutive 270-270 degree corners of {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.035 μm} [INSIDE PO_P76] (10 polys for merged U-shape)	L5	≥	0.8250

Rule No.	Description	Label	Op.	Rule
PO.L.5.1	Horizontal edge length between two consecutive 90-90 degree corners {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.0245 μm} (10 polys for merged T-shape) (Except PO_P63, PO_P76)	L5A	≥	0.5210
PO.L.5.1.1	Horizontal edge length between two consecutive 90-90 degree corners {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.0275 μm} [INSIDE PO_P63] (10 polys for merged T-shape)	L5A	≥	0.5750
PO.L.5.1.2	Horizontal edge length between two consecutive 90-90 degree corners {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.035 μm} [INSIDE PO_P76] (10 polys for merged T-shape)	L5A	≥	0.6920
PO.L.5.2	Horizontal edge length between two consecutive 90-270 degree corners {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.0245 μm} (10 polys for merged stair-shape) (Except PO_P63, PO_P76, or following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	L5B	≥	0.5670
PO.L.5.2.1	Horizontal edge length between two consecutive 90-270 degree corners {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.0275 μm} [INSIDE PO_P63] (10 polys for merged stair-shape) (Except following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	L5B	≥	0.6270
PO.L.5.2.2	Horizontal edge length between two consecutive 90-270 degree corners {ALL_PO [width ≤ 0.011 μm] SIZING up/down 0.035 μm} [INSIDE PO_P76] (10 polys for merged stair-shape) (Except following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	L5B	≥	0.7570
PO.A.1	Area of ALL_PO	A1	≥	0.00176
PO.A.3	Area of {ALL_PO NOT CPO} (Except Dummy_Cell, IBJTD MY, or following conditions: 1. {ALL_PO NOT CPO} [width ≤ 0.036 μm] enclosed in 10 μm x 10 μm window with poly density ≤ 50%, 2. {ALL_PO NOT CPO} [width = 0.100 μm ~ 0.240 μm, length ≤ 30 μm] enclosed in 10 μm x 10 μm window with poly density ≤ 50%) DRC methodology: Area of {ALL_PO NOT CPO} Definition of "High Density Region": {ALL_PO NOT CPO} density [10 μm x 10 μm window, stepping 5 μm] inside {{ALL_PO NOT CPO} [area > 2.43 μm²] SIZING 5 μm} is > 50% DRC won't flag: 1. IBJTD MY 2. {ALL_PO NOT CPO} [width ≤ 0.036 μm] NOT INTERACT "High Density Region" 3. {ALL_PO NOT CPO} [width = 0.100 μm ~ 0.240 μm, length ≤ 30 μm] NOT INTERACT "High Density Region"	A3	≤	2.43
PO.A.3.1	Area of {ALL_PO NOT CPO} [INSIDE IBJTD MY]	A3A	≤	4

Rule No.	Description	Label	Op.	Rule
PO.A.4	<p>Empty area of {ALL_PO NOT CPO} [ALL_PO space > 1.2 μm] (Except ICOVL_SINGLE, SEALRING_ALL, TCDDMY, or following conditions:</p> <ol style="list-style-type: none"> 1. Chip corner triangle empty areas if seal-ring is added by tsmc) <p>DRC flags {{CHIP NOT {{ALL_PO NOT CPO} SIZING up/down 0.600 <math>\mu\text{m}}}} SIZING down/up 0.600 <math>\mu\text{m}} can enclose a 16 $\mu\text{m} \times 1.2 \mu\text{m}$ orthogonal rectangle</math></math></p> <p>Warning: To avoid PO.A.4 violation from a high R resistor with large width (e.g. $W \geq 1.06 \mu\text{m}$), recommend to use the shorter length (e.g. $L < 15.2 \mu\text{m}$) of a high R resistor</p>	A4	<	19.2
PO.A.4.1	<p>Empty area of {ALL_PO NOT CPO} [ALL_PO space > 0.800 μm] (Except SEALRING_ALL, TCDDMY, ICOVL_SINGLE, NWDMY, RH_TNB, IBJTDMY, or following conditions:</p> <ol style="list-style-type: none"> 1. Chip corner triangle empty areas if seal-ring is added by tsmc) <p>DRC flags {{CHIP NOT {{ALL_PO NOT CPO} SIZING up/down 0.400 <math>\mu\text{m}}}} SIZING down/up 0.400 <math>\mu\text{m}} can enclose a 5 $\mu\text{m} \times 0.800 \mu\text{m}$ orthogonal rectangle</math></math></p>	A4A	<	4
PO.A.4.2	<p>Maximum empty area [abut {ALL_PO NOT CPO} width $\leq 0.020 \mu\text{m}$] of {ALL_PO NOT CPO} [$< 0.570 \mu\text{m} \times 7 \mu\text{m}$] (Except SEALRING_ALL, TCDDMY, ICOVL_SINGLE, NWDMY, RH_TNB, IBJTDMY, or following conditions:</p> <ol style="list-style-type: none"> 1. Chip corner triangle empty areas if seal-ring is added by tsmc) <p>DRC flags {{CHIP NOT {{ALL_PO NOT CPO} SIZING up/down 0.285 <math>\mu\text{m}}}} SIZING down/up 0.285 <math>\mu\text{m}} can enclose a 0.570 $\mu\text{m} \times 7 \mu\text{m}$ orthogonal rectangle and this orthogonal rectangle abut PO width $\leq 0.020 \mu\text{m}$</math></math></p>	A4B	<	4
PO.A.5	<p>Empty area of {ALL_PO NOT CPO} within 1 μm from SRAM (Except following conditions:</p> <ol style="list-style-type: none"> 1. SRM (50;0) space to {ALL_PO NOT CPO} [PRL > 0.250 μm] $\leq 0.400 \mu\text{m}$, 2. prBoundary enclosure SRM (50;0) $\leq 0.150 \mu\text{m}$ in cell level) <p>DRC flags {{{{SRM SIZING 1 μm} NOT SRM} NOT {ALL_PO NOT CPO}}} SIZING down/up 0.270 <math>\mu\text{m}} can enclose a 10 $\mu\text{m} \times 0.540 \mu\text{m}$ orthogonal rectangle</math></p>	A5	<	5.4
PO.A.7	<p>Area of Fine_PO_Group_Region [INTERACT MOS]</p> <p>Definition of Fine_PO_Group: ALL_PO [width $\leq 0.011 \mu\text{m}$] SIZING up/down 0.035 μm as group</p> <p>Definition of Fine_PO_Group_Region : Fine_PO_Group SIZING up/down 0.200 μm</p> <p>DRC merged small inner holes (area $< 0.5 \mu\text{m}^2$) of Fine_PO_Group_Region</p>	A7	\geq	36
PO.DN.1	Minimum {ALL_PO NOT CPO} density across full chip		\geq	14%
PO.DN.1.1	Maximum {ALL_PO NOT CPO} density across full chip		\leq	40%
PO.DN.2	<p>Minimum {ALL_PO NOT CPO} density in window 10 $\mu\text{m} \times 10 \mu\text{m}$, stepping 5 μm</p> <p>(Except TCDDMY, ICOVL_SINGLE, RH_TNB, or following conditions:</p> <ol style="list-style-type: none"> 1. {SEALRING_ALL SIZING 1 μm}, 2. {Chip corner triangle empty areas SIZING 1 μm} if seal-ring is added by tsmc) 		\geq	10%

Rule No.	Description	Label	Op.	Rule
PO.DN.2.1	Minimum {ALL_PO NOT CPO} density in window 10 μm x 10 μm, stepping 5 μm (Except TCDDMY, ICOVL_SINGLE, or following conditions: 1. {SEALRING_ALL SIZING 1 μm}, 2. {Chip corner triangle empty areas SIZING 1 μm} if seal-ring is added by tsmc)		≥	7%
PO.DN.3.1	Maximum {PO NOT CPO} density in window 10 μm x 10 μm, stepping 5 μm (Except OD2, TCDDMY, ICOVL_SINGLE, or following conditions: 1. DECAPDMY [width ≤ 35 μm and space > 10 μm])		≤	50%
PO.DN.3.2	Maximum {ALL_PO NOT CPO} density in window 150 μm x 150 μm, stepping 75 μm (Except TCDDMY, ICOVL_SINGLE)		≤	50%
PO.DN.3.4	Maximum {ALL_PO NOT CPO} density in window 10 μm x 10 μm, stepping 5 μm (Except TCDDMY, ICOVL_SINGLE)		≤	60%
PO.DN.3.6	Maximum {ALL_PO NOT CPO} density in window 10 μm x 10 μm, stepping 5 μm (Except DECAPDMY, OD2, TCDDMY, ICOVL_SINGLE)		≤	53%
PO.DN.6	Maximum {ALL_PO NOT CPO} density in {{{{MATCHING OR ANARRAY_H} OR ANARRAY_M} OR ANARRAY_S} SIZING 10 μm} in window 10 μm x 10 μm, stepping 5 μm Each MOS array for mis-match circuit must be covered by MATCHING (205;8), ANARRAY_H(255;20), ANARRAY_S (255;24), or ANARRAY_M (255;21) to check PO.DN.6, 3 times mis-match degradation will be occurred if they violate PO.DN.6		≤	50%
PO.DN.7	ALL_PO density difference between any two neighboring checking windows [window 10 μm x 10 μm, stepping 5 μm] (Except TCDDMY, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≤	35%
PO.R.1	ALL_PO [width ≥ 0.020 μm] must be a rectangle orthogonal to grid (Except SEALRING_ALL)			
PO.R.1.1	ALL_PO [0.008 μm ≤ width ≤ 0.011 μm] must be a rectangle orthogonal to grid (Except following conditions: 1. small jog ≤ 0.002 μm, and the jog width must be the same)			
PO.R.1.4	ALL_PO jog width must be the same			
PO.R.1.5	ALL_PO jog length [INSIDE CPO] must be the same			
PO.R.1.6	ALL_PO jog must be at the same height (on the same ALL_PO), Z-shape ALL_PO jog isn't allowed			
PO.R.1.7	ALL_PO jog [INTERACT {TrGATE SIZING 0.100 μm}] must be at the same height			
PO.R.2	SR_DPO overlap PO is not allowed (Except following conditions: 1. {SR_DPO AND PO} INSIDE CPO, 2. {SR_DPO AND {CPODE SIZING 0.002 μm in horizontal direction}})			
PO.R.2.1	{{{SR_DPO AND PO} AND CPODE} [width ≤ 0.011 μm] vertical centerline must abut vertical centerline of PO [width ≤ 0.011 μm]}			
PO.R.3 ^U	ALL_PO line-end must be rectangular			
PO.R.5	ALL_PO must be vertical direction (Except DC_WPO, SEALRING_ALL)			
PO.R.12.1	OD [INTERACT PO [width ≥ 0.020 μm]] must be a rectangle			

Rule No.	Description	Label	Op.	Rule
PO.R.15	<p>The number of {ALL_PO [width ≤ 0.011 μm] OR BPO_V [length = 0.100 μm]} in each PO_P57_Group_Even_NOPOB [poly space ≤ 0.049 μm] must be even.</p> <p>Definition of PO_P57_NOPOB: $\{\text{ALL_PO} [\text{width} \leq 0.011 \mu\text{m}] \text{ OR } \text{BPO_V} [\text{length} = 0.100 \mu\text{m}]\} \text{ NOT PO_Boundary}$</p> <p>Definition of PO_P57_Group_Even_NOPOB: Form PO_P57_NOPOB with same length with neighboring PO_P57_NOPOB (space = 0.046/0.0475/0.049 μm) as group</p>			
PO.R.15.1	<p>The number of {ALL_PO [width ≤ 0.011 μm] OR BPO_V [length = 0.100 μm]} in each PO_P63_Group_Even [poly space ≤ 0.055 μm] must be even.</p> <p>Definition of PO_P63_Group_Even: Form {ALL_PO OR BPO_V [length = 0.100 μm]} [INSIDE PO_P63] with same length with neighboring ALL_PO (space = 0.052/0.0535/0.055 μm) as group</p>			
PO.R.15.2	<p>{ALL_PO [width ≤ 0.011 μm] OR BPO_V [length = 0.100 μm]} number in each PO_P57_Group_Even_NOPOB must be ≥ 10, and adjacent ALL_PO number with same width in PO_P57_Group_Even_NOPOB must be ≥ 2 (Except Dummy_Cell, or following conditions: 1. the group [ALL_PO number is even] fully project at both side group [≥ 10 poly])</p> <p>Definition of PO_P57_Group_Even_NOPOB follows PO.R.15</p>			
PO.R.15.2.1	<p>{ALL_PO [width ≤ 0.011 μm] OR BPO_V [length = 0.100 μm]} number in each PO_P63_Group_Even must be ≥ 10, and adjacent ALL_PO number with same width in PO_P63_Group_Even must be ≥ 2 (Except Dummy_Cell, or following conditions: 1. the group [ALL_PO number is even] fully project at both side group [≥ 10 poly])</p> <p>Definition of PO_P63_Group_Even follows PO.R.15.1</p>			
PO.R.15.2.2	<p>ALL_PO [width ≤ 0.011 μm] number in each PO_P76_Group_Even must be ≥ 10, and adjacent ALL_PO number with same width in PO_P76_Group_Even must be ≥ 2 (Except Dummy_Cell, or following conditions: 1. the group [ALL_PO number is even] fully project at both side group [≥ 10 poly])</p> <p>Definition of PO_P76_Group_Even follows PO.R.15.7</p>			
PO.R.15.4	<p>The number of ALL_PO [width ≤ 0.011 μm] in each PO_P57_Group_Even_POB [poly space ≤ 0.049 μm] must be even.</p> <p>Definition of PO_P57_POB: {ALL_PO [width ≤ 0.011 μm] INSIDE PO_Boundary}</p> <p>Definition of PO_P57_Group_Even_POB: Form PO_P57_POB with same length with neighboring PO_P57_POB (space = 0.046/0.0475/0.049 μm) as group</p>			
PO.R.15.5	<p>ALL_PO number in each PO_P57_Group_Even_POB must be ≥ 10, and adjacent ALL_PO number with same width in PO_P57_Group_Even_POB must be ≥ 4 (Except Dummy_Cell)</p> <p>Definition of PO_P57_Group_Even_POB follows PO.R.15.4</p>			

Rule No.	Description	Label	Op.	Rule
PO.R.15.7	The number of ALL_PO [width ≤ 0.011 μm] in each PO_P76_Group_Even [poly space ≤ 0.068 μm] must be even. Definition of PO_P76_Group_Even: Form ALL_PO [{INSIDE PO_P76}] with same length with neighboring ALL_PO (space = 0.065/0.0665/0.068 μm) as group			
PO.R.16	The number of ALL_PO [width = 0.020 μm] in one group [poly space ≤ 0.080 μm] must be ≥ 7. (DRC flags width of {ALL_PO [width = 0.020 μm, space ≤ 0.080 μm] SIZING up/down 0.040 μm} < 0.620 μm in horizontal direction)			
PO.R.18	Maximum width and length of high {ALL_PO NOT CPO} density region ≥ 65% in {{{{MATCHING OR ANARRAY_H} OR ANARRAY_M} OR ANARRAY_S} SIZING 10 μm}, by checking window 3 μm x 10 μm, stepping 1.5 μm x 5 μm, and 10 μm x 3 μm, stepping 5 μm x 1.5 μm respectively		≤	60
PO.R.19	Floating gate is forbidden if the effective source/drain are not connected together. (Except BLK_WF) Floating gate in the DRC is as follows: (1) TrGATE without MP (2) TrGATE with MP but not connected to MOS OD, STRAP or PAD (3) It is not a floating gate if the TrGATE is connected to OD by butted MP in SRAM bit cell The effective source/drain in DRC is as follows: (1) Source/drain is connected to different {MOS OD NOT PO}, STRAP, Gate, or PAD This rule is only checked in chip level			
PO.R.22	{ALL_PO NOT CPO} cut {OD2 OR {{IBJTDMDY OR DIODMY} OR VAR}} is not allowed (Except Dummy_Cell)			
PO.R.24	SR_DPO abut with PO must be in the center of CPO [width ≤ 0.068 μm] in vertical direction			
PO.R.25	ALL_PO [width ≤ 0.036 μm] interact {{NWDMDY OR RH_TNB} SIZING 1 μm} is not allowed (Except SEALRING_ALL, Dummy_Cell, or following conditions: 1. ALL_PO interact STRAP)			
PO.R.29	Maximum delta V > 3.63V is not allowed. DRC searching range of {ALL_PO NOT CPO} space to ALL_OD is < 0.760 μm			
PO.R.30	ALL_PO number interact same ALL_OD must be ≥ 2 (Except Dummy_Cell)			
PO.R.33	Passive_Device_Forbidden_Region interact ALL_PO [width < 0.072 μm] is not allowed (Except SEALRING_ALL, Dummy_Cell, or following conditions: 1. ALL_PO interact STRAP) Passive_Device: {NWDMDY OR RH_TNB} OR IBJTDMDY Passive_Device_Forbidden_Region: {Passive_Device SIZING 0.6 μm} NOT Passive_Device}			
PO.R.34	Either one of {ALL_PO NOT CPO} [ALL_PO width = 0.072~0.090 μm, either one side poly space > 0.147 μm in horizontal direction, interact same ALL_CPO and same ALL_PO] interact MP is not allowed (Except following conditions: 1. {ALL_PO NOT ALL_CPO} is the same net [INTERACT the same ALL_CPO]) DRC only check ALL_PO cross ALL_CPO case			

Table Notes:

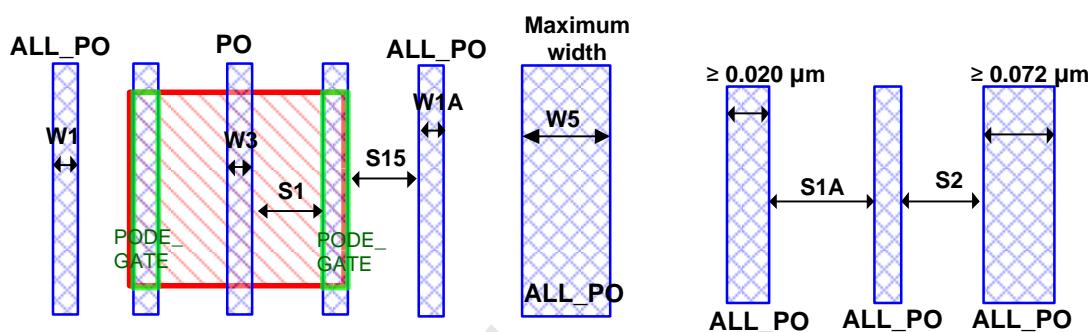
- It is recommended, either to follow the density DFM recommendations to design your IP layout, or

adopt “IP_TIGHTEN_DENSITY” in the DRC deck, to avoid high/low density violation while IP repeating or IP abutting with others. If you use dummy block to avoid dummy insertion after IP design, please make sure to insert dummy patterns before IP release, no matter by utility or manually. Do not leave white space arbitrarily.

- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

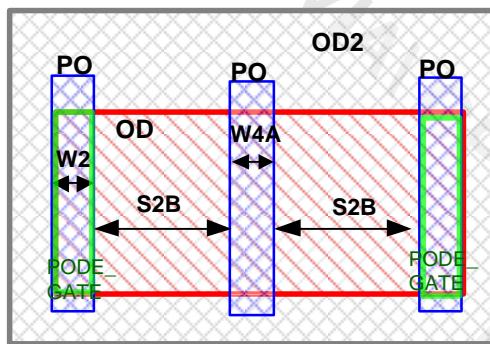
TSMC Confidential Information
VIAI CPU Platform\ Col., I Ltd.
938214
10/05/2018

PO

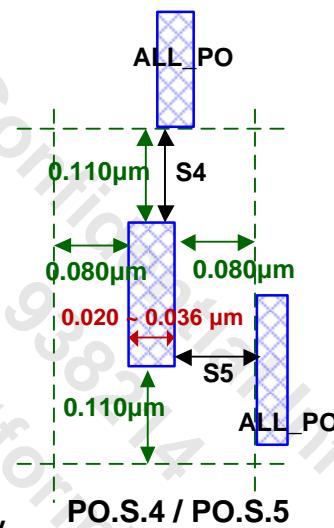


PO.W.1 / PO.W.1.1 /PO.W.3/ PO.W.5/ PO.S.1/PO.S.1.0.1/PO.S.1.0.2

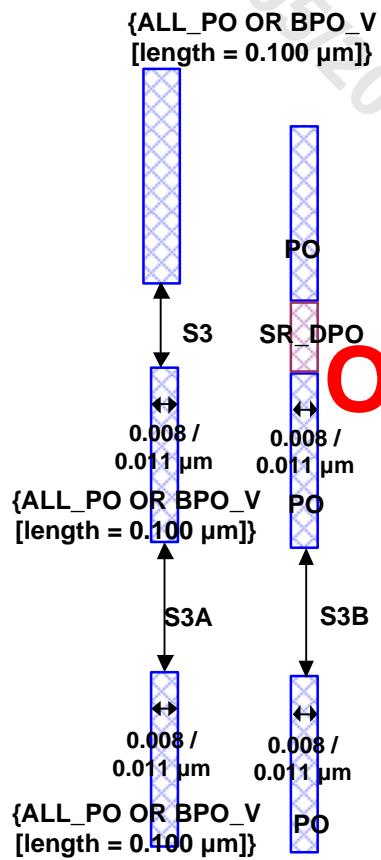
PO.S.1.1 / PO.S.2



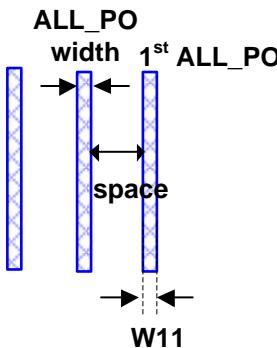
PO.W.2 / PO.W.4.1/ PO.S.2.2



PO.S.4 / PO.S.5



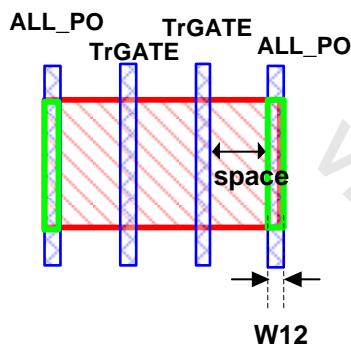
PO.S.3 / PO.S.3.1 / PO.S.3.2



1st PO width rule:

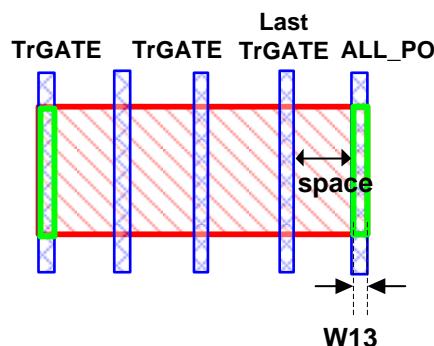
Rule	ALL_PO width	space	1st ALL_PO width
PO.W.11	0.008 μm	< 0.070 μm	0.008, 0011 μm
PO.W.11.1	0.011 μm	< 0.070 μm	0.008, 0011 μm
PO.W.11.3	0.020 μm	< 0.094 μm	0.020, 0036 μm
PO.W.11.7	0.036 μm	< 0.094 μm	0.020, 0036 μm

PO.W.11 / PO.W.11.1 / PO.W.11.3 / PO.W.11.7



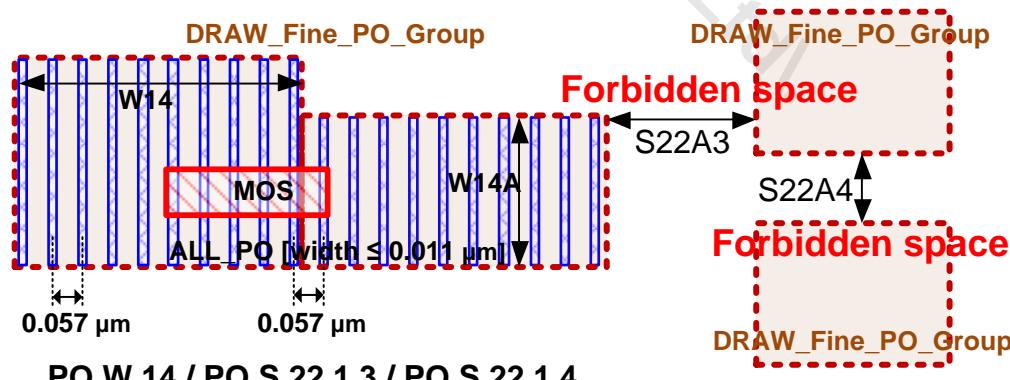
Rule	ALL_PO width	space	1st ALL_PO width
PO.W.12	0.008 μm	< 0.070 μm	0.008, 0011 μm
PO.W.12.1	0.011 μm	< 0.070 μm	0011 μm
PO.W.12.3	0.020 μm	< 0.094 μm	0.020 μm
PO.W.12.4	0.036 μm	< 0.094 μm	0036 μm

PO.W.12 / PO.W.12.1/ PO.W.12.3/ PO.W.12.4

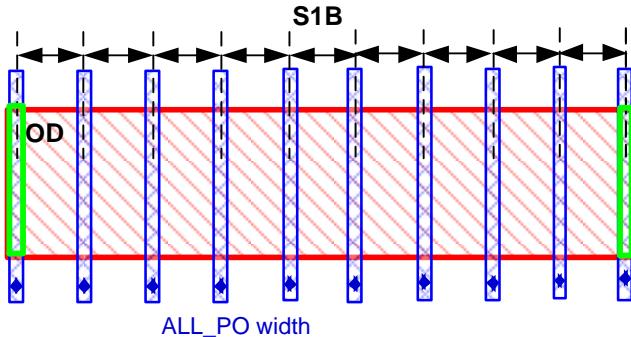


Rule	Last TrGATE condition	space	ALL_PO width
PO.W.13	$\geq 0.072 \mu\text{m}$	=0.094 μm	$\geq 0.072 \mu\text{m}$
PO.W.13.1	inside OD2	=0.094 μm	$\geq 0.086 \mu\text{m}$
PO.W.13.2	inside {OD18_12 OR OD15_12}	=0.094 μm	$\geq 0.072 \mu\text{m}$

PO.W.13 / PO.W.13.1 / PO.W.13.2

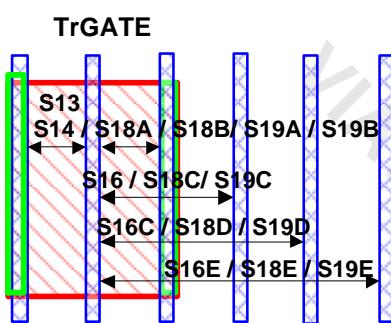


PO.W.14 / PO.S.22.1.3 / PO.S.22.1.4



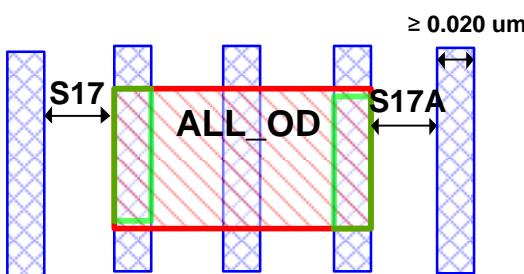
Rule	ALL_PO width	Centerline space(S1B)
PO.S.1.2	=0.008/0.011μm	0.057 μm
PO.S.1.2.2	=0.008/0.011μm	0.063 μm
PO.S.1.3	=0.020 μm	0.100 μm

PO.S.1.2 / PO.S.1.2.2 / PO.S.1.3

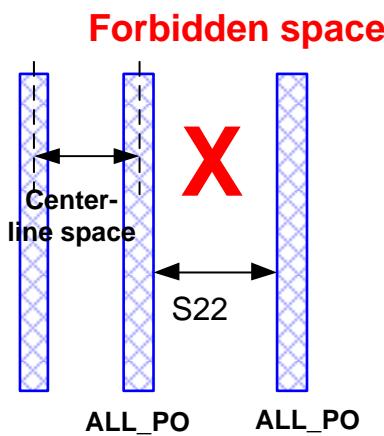


channel length	Centerline space	to 1st PO space (S13/S14/S18A/S18B/S19A/ S19B)	to 2nd PO space (S16/S18C/S19C)	to 3rd PO space (S16C/S18D/S19D)	to 4th PO space (S16E/S18E/S19E)
=0.008 μm	=0.057 μm	=0.0475~ 0.0490 μm PO.S.13.1	=0.103~ 0.106 μm PO.S.16	=0.160~ 0.163 μm PO.S.16.3	=0.217~ 0.220 μm PO.S.16.5
=0.011 μm	=0.057 μm	=0.0460~ 0.0475 μm PO.S.13.2			
=0.008 μm	=0.064 μm	=0.0545~ 0.0560 μm PO.S.18.1	=0.117~ 0.120 μm PO.S.18.3	=0.181~ 0.184 μm PO.S.18.4	=0.245~ 0.248 μm PO.S.18.5
=0.011 μm	=0.064 μm	=0.0530~ 0.0545 μm PO.S.18.2			
=0.008 μm	=0.076 μm	=0.0665~ 0.0680 μm PO.S.19.1	=0.1410 ~ 0.144 μm PO.S.19.3	=0.2170 ~ 0.220 μm PO.S.19.4	=0.2930 ~ 0.296 μm PO.S.19.5
=0.011 μm	=0.076 μm	=0.0650 ~ 0.0665 μm PO.S.19.2			
=0.020 μm	=0.100 μm	=0.0800 μm PO.S.13.5	≤ 0.196 μm PO.S.16.1	≤ 0.312 μm PO.S.16.4	X
=0.036 μm	X	=0.0800 μm PO.S.13.6	≤ 0.196 μm PO.S.16.1		
≥ 0.072 μm	X	=0.0940 μm PO.S.14	≤ 0.428 μm PO.S.16.2	X	X

PO.S.13.1 / PO.S.13.2 / PO.S.13.5 / PO.S.13.6 / PO.S.14 / PO.S.16 /
PO.S.16.1 / PO.S.16.2 / PO.S.16.3 / PO.S.16.4 / PO.S.16.5 /
PO.S.18.1 / PO.S.18.2 / PO.S.18.3 / PO.S.18.4 / PO.S.18.5 /
PO.S.19.1 / PO.S.19.2 / PO.S.19.3 / PO.S.19.4 / PO.S.19.5

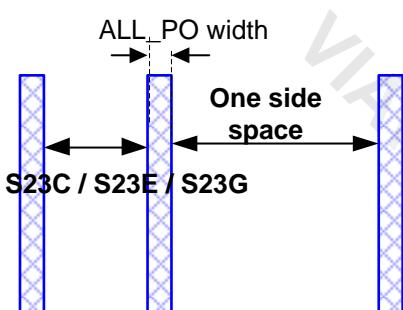


PO.S.17 / PO.S.17.1



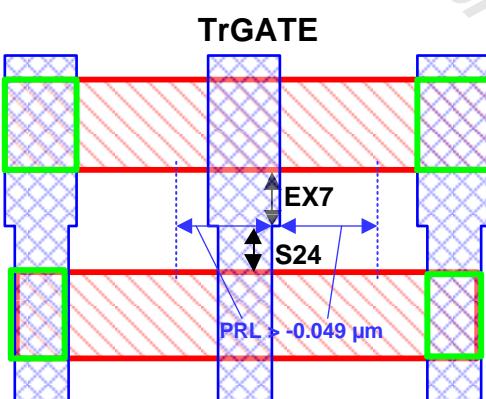
Rule	ALL_PO width	Centerline space	Forbidden space(S22)
PO.S.22.1.1	=0.008 μm	=0.057 μm	0.0480 ~ 0.0485, 0.0495 ~ 0.1795 μm
PO.S.22.1.2	=0.011 μm	=0.057 μm	0.0465 ~ 0.0470, 0.0480 ~ 0.1795 μm
PO.S.22.1.1.1	=0.008 μm	=0.063 μm	0.0550 ~ 0.0555, 0.0565 ~ 0.1795 μm
PO.S.22.1.1.2	=0.008 μm	=0.076 μm	0.0670 ~ 0.0675, 0.0685 ~ 0.1795 μm
PO.S.22.1.2.1	=0.011 μm	=0.063 μm	0.0535 ~ 0.0540, 0.0550 ~ 0.1795 μm
PO.S.22.1.2.2	=0.011 μm	=0.076 μm	0.0655 ~ 0.0660, 0.0670 ~ 0.1795 μm
PO.S.22.2	=0.020 μm	=0.100 μm	0.0805 ~ 0.2060 0.2460 ~ 0.2860 μm

PO.S.22.1.1 / PO.S.22.1.1.1 / PO.S.22.1.1.2 / PO.S.22.1.2 /
PO.S.22.1.2.1 / PO.S.22.1.2.2 / PO.S.22.2 /

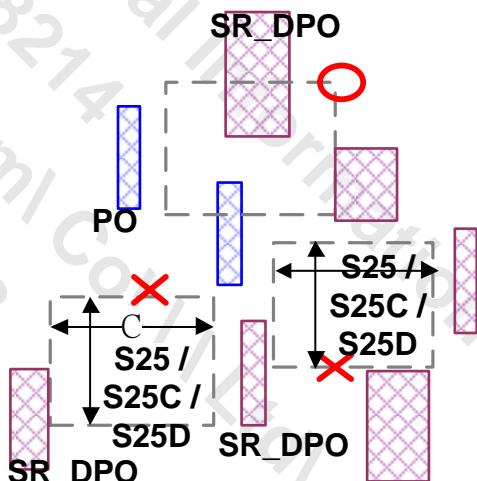


Rule	ALL_PO width	one side poly space	Space
PO.S.23.3	= 0.020 μm	> 0.080 μm	= 0.080 μm (S23C)
PO.S.23.5	= 0.036 μm	> 0.080 μm	= 0.080 μm (S23E)
PO.S.23.7	= 0.072~ 0.161 μm	> 0.094 μm	= 0.094 μm (S23G)

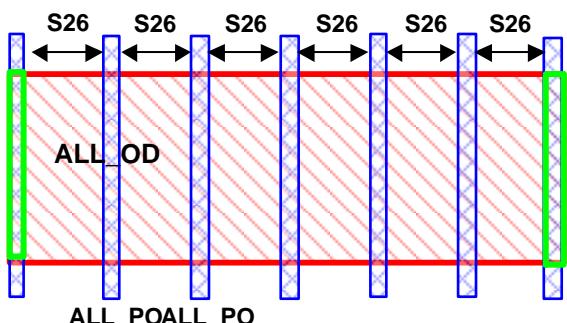
PO.S.23.3 / PO.S.23.5 / PO.S.23.7



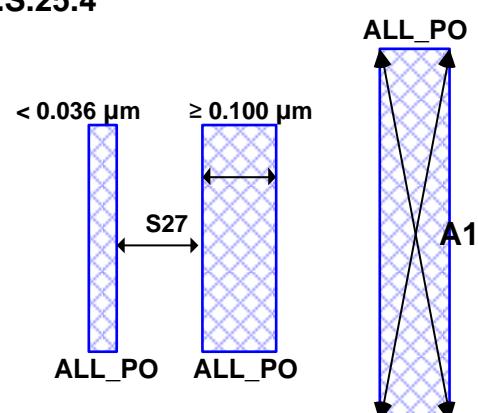
PO.S.24 / PO.EX.7



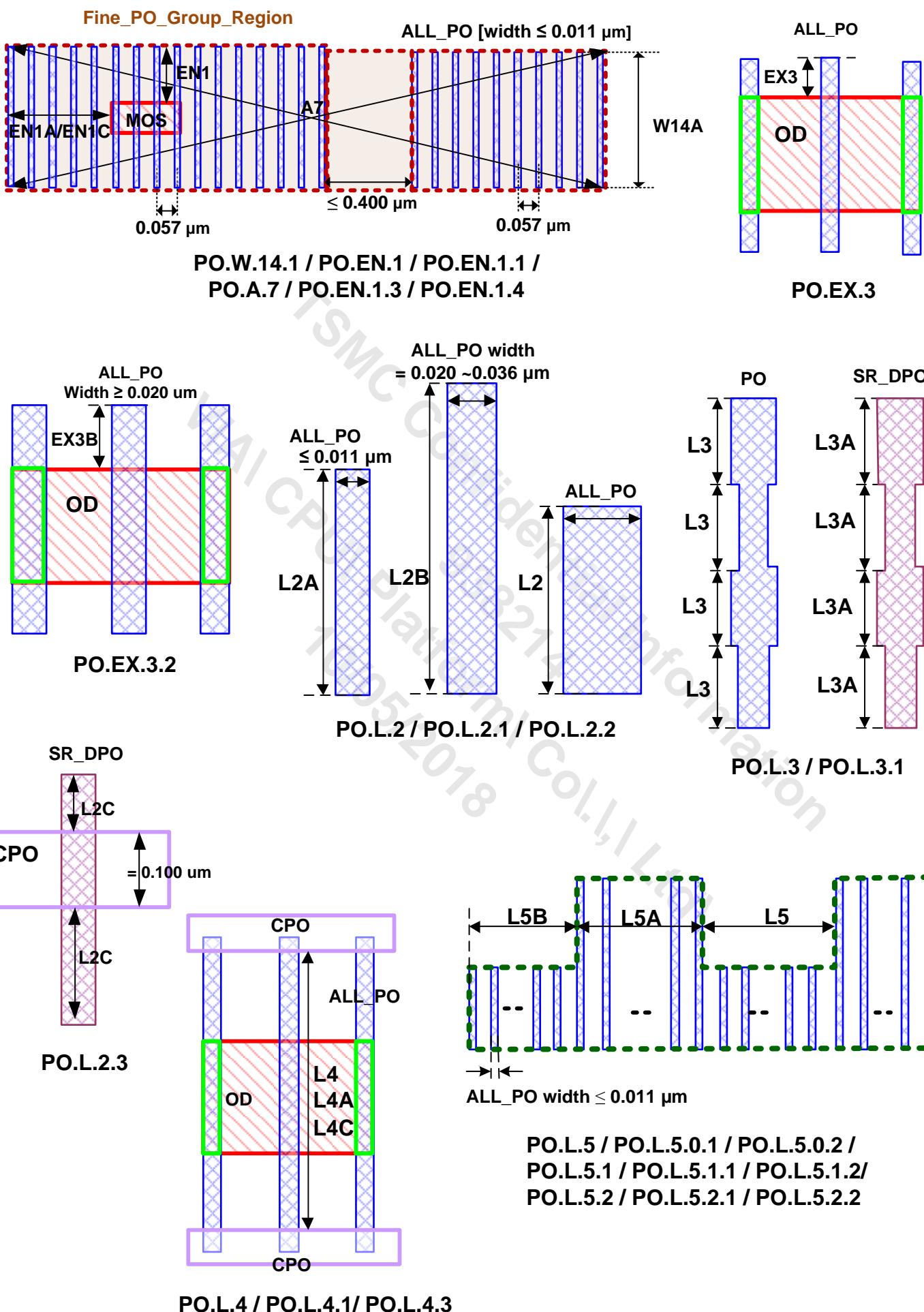
PO.S.25 / PO.S.25® / PO.S.25.3/
PO.S.25.4

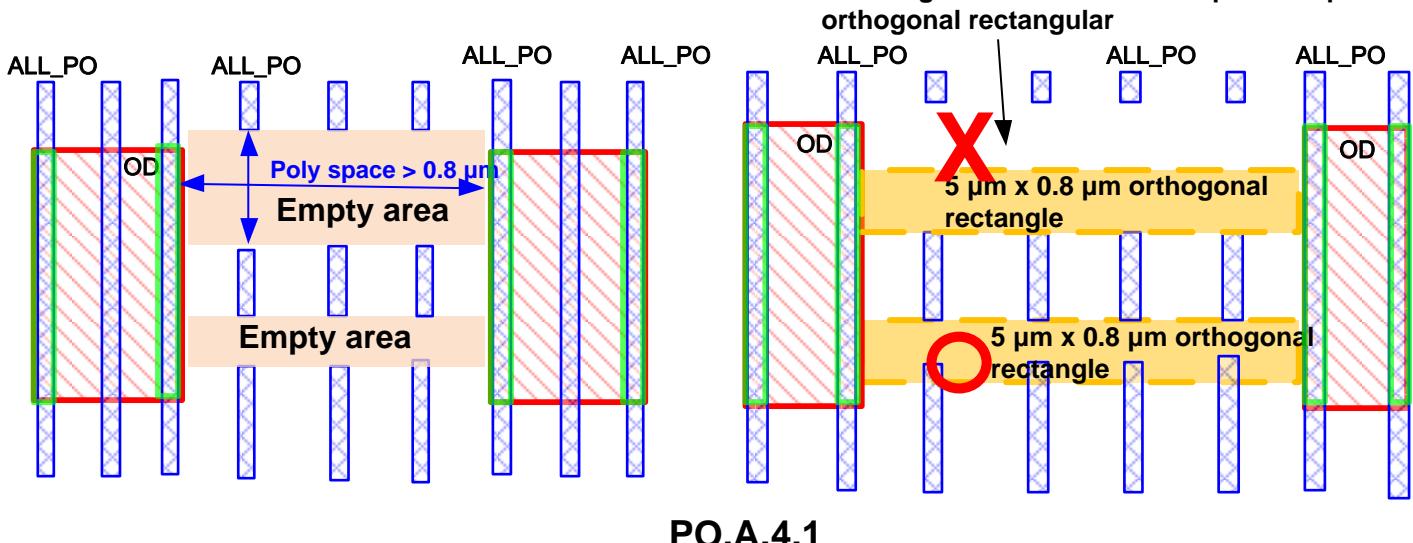
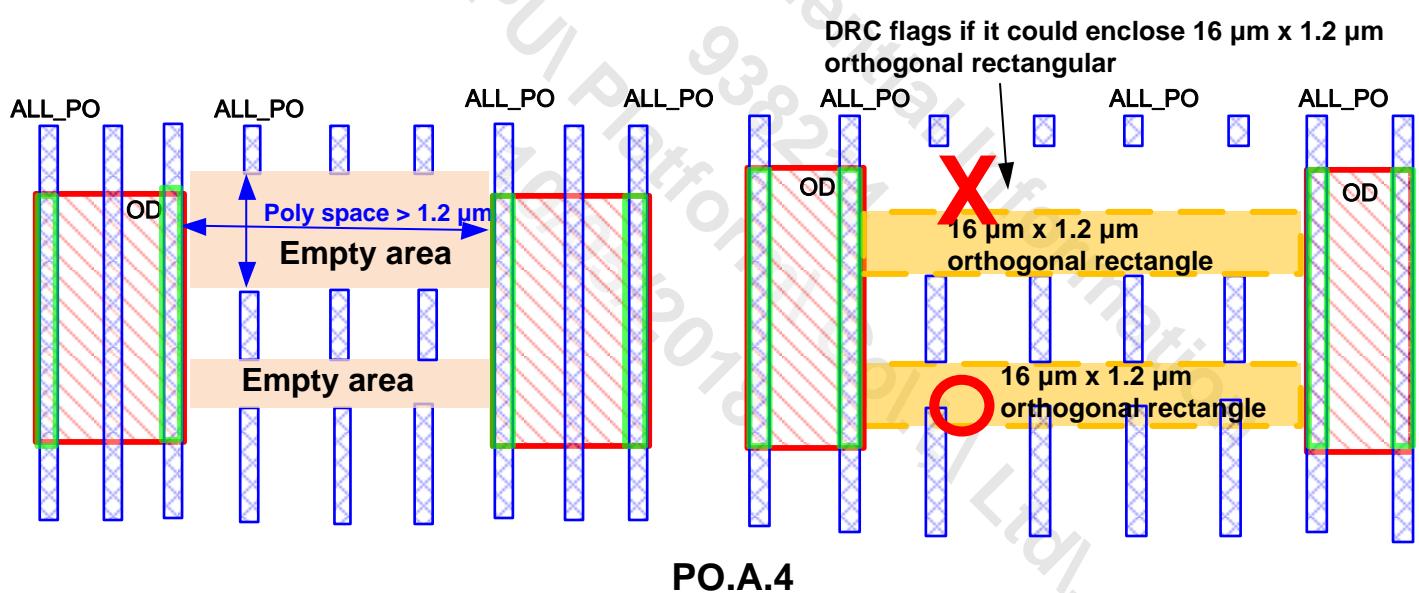
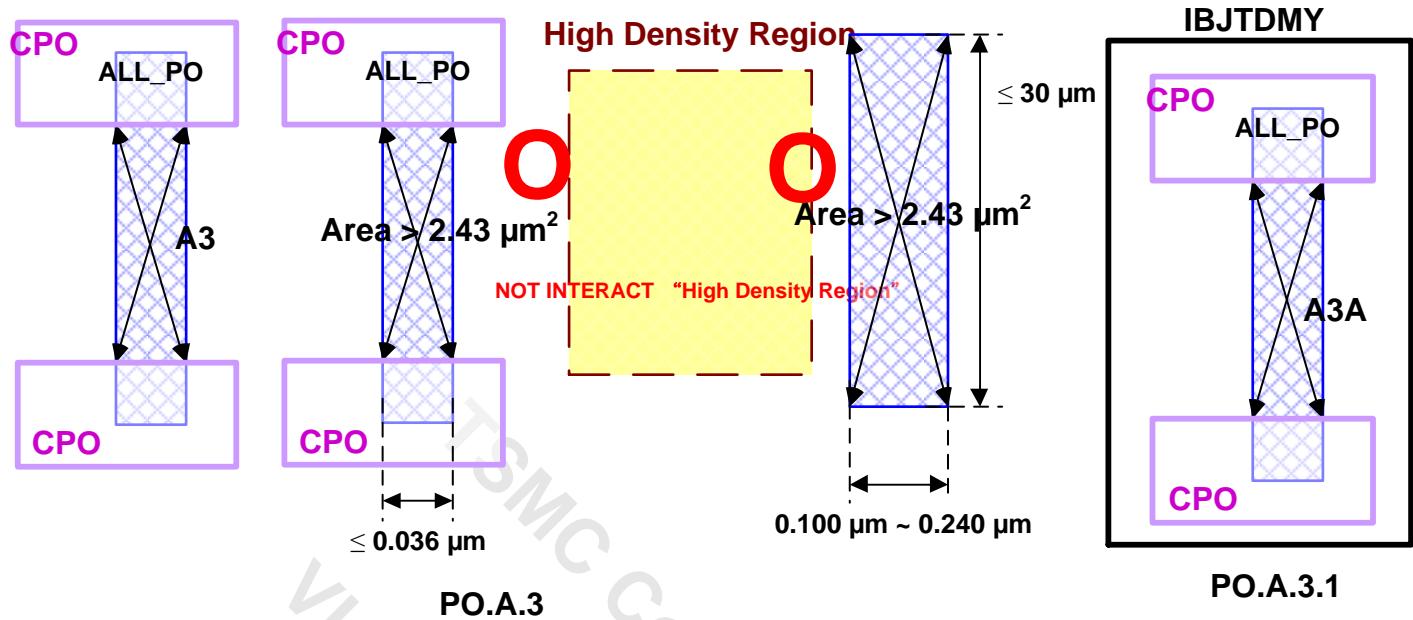


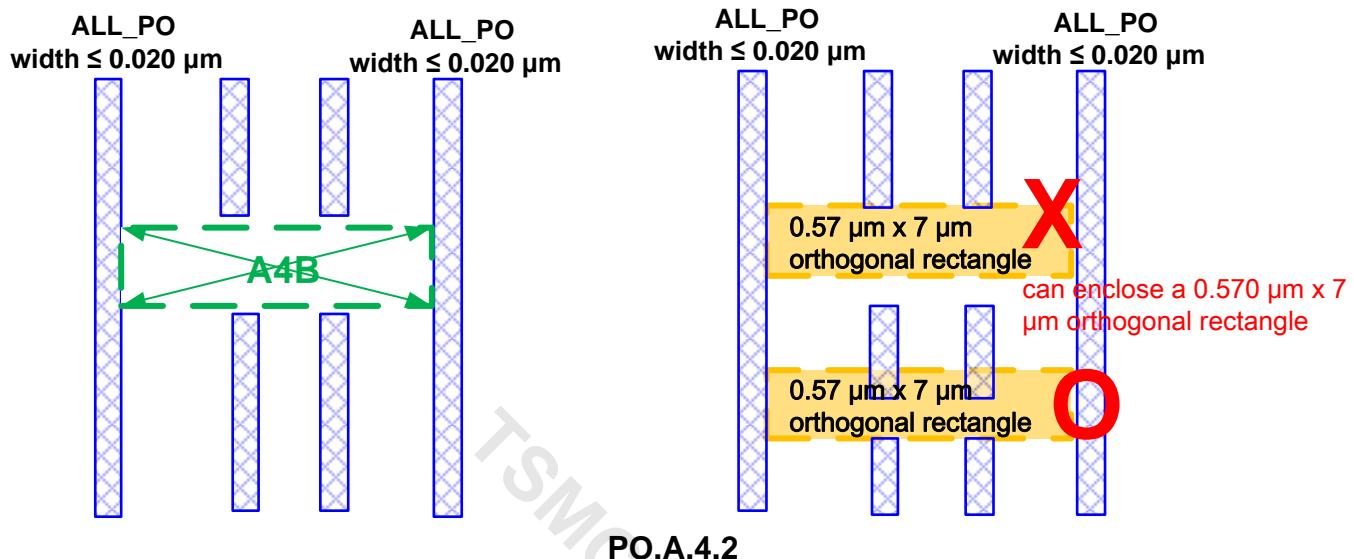
PO.S.26



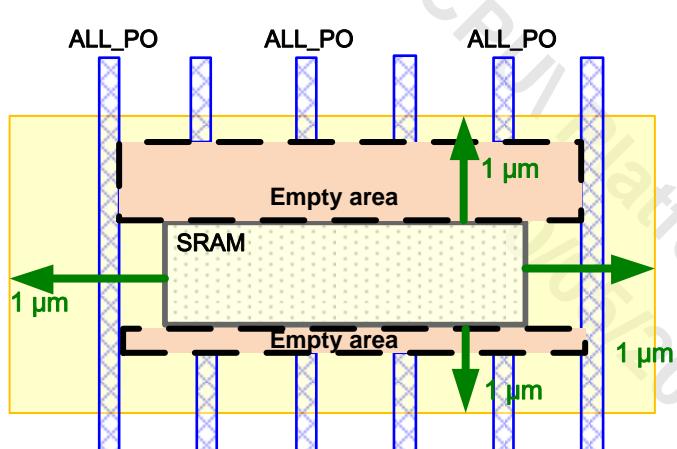
PO.A.1



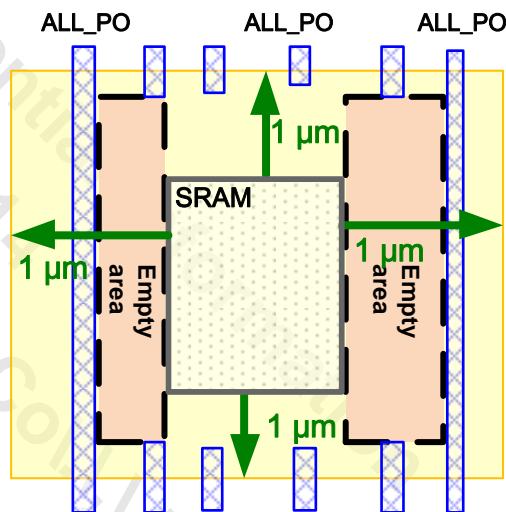




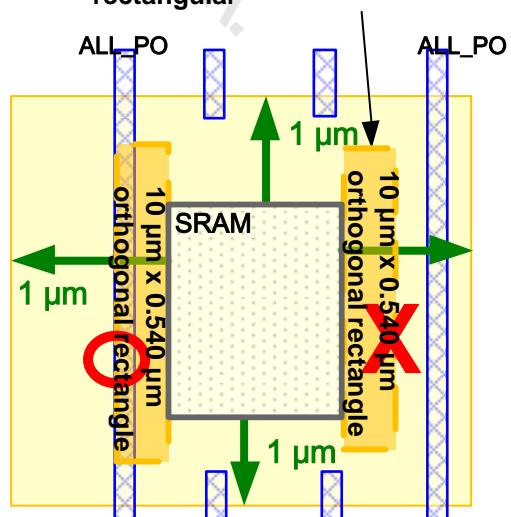
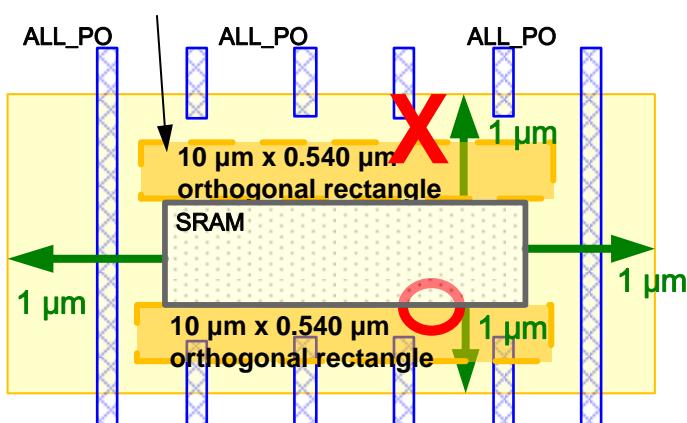
PO.A.4.2



DRC flags if it could enclose
10 μm x 0.540 μm orthogonal
rectangular

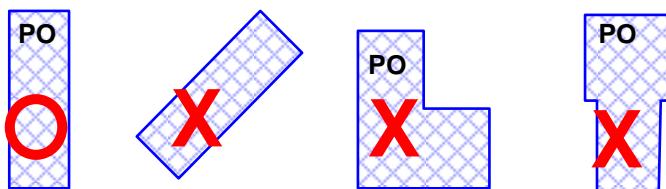


DRC flags if it could enclose
10 μm x 0.540 μm orthogonal
rectangular



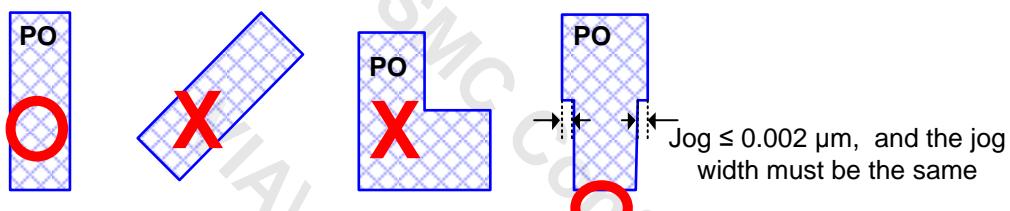
PO.A.5

- ALL_PO [width > 0.020 μm]



must be a rectangle orthogonal to grid

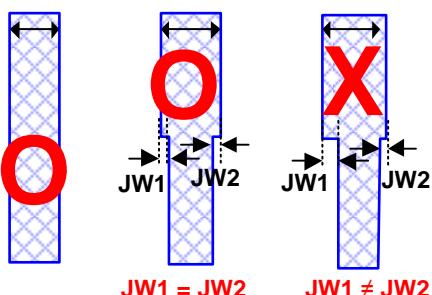
- ALL_PO [width = 0.008/0.011 μm with centerline space = 0.057 μm]



must be a rectangle orthogonal to grid

PO.R.1 / PO.R.1.1

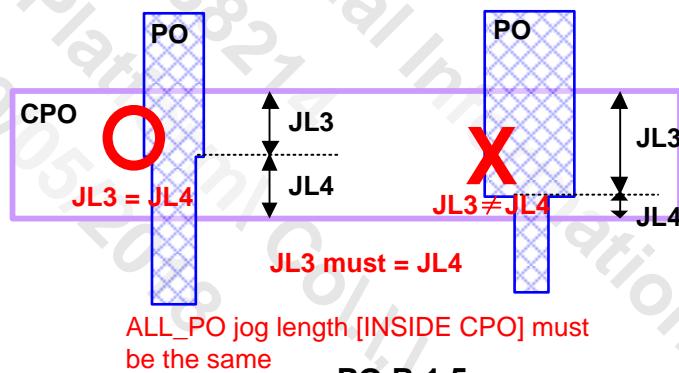
ALL_PO width = 0.008 ~ 0.011 μm



JW1 = JW2

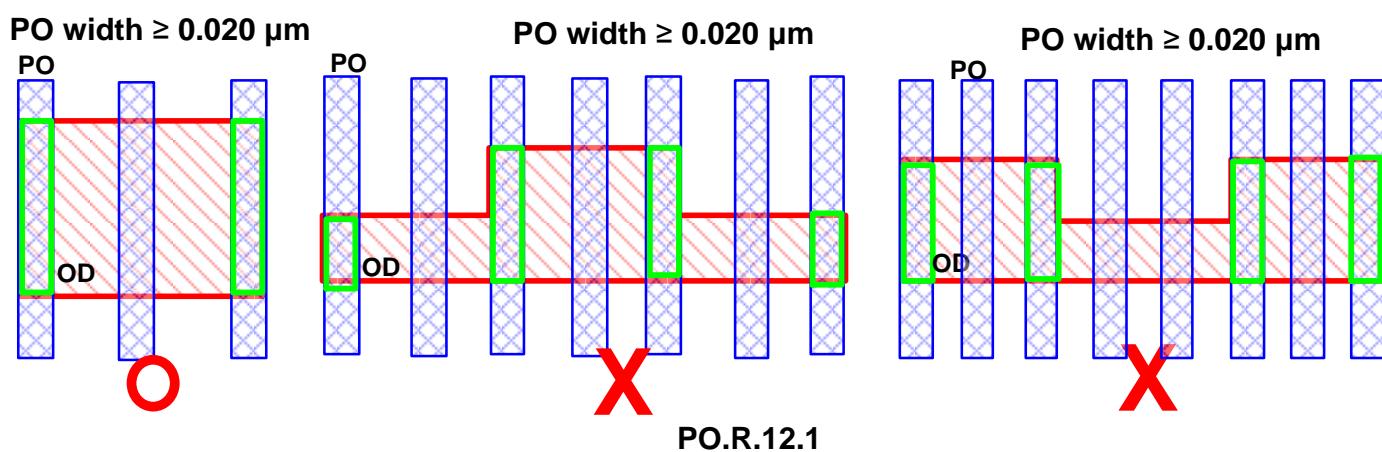
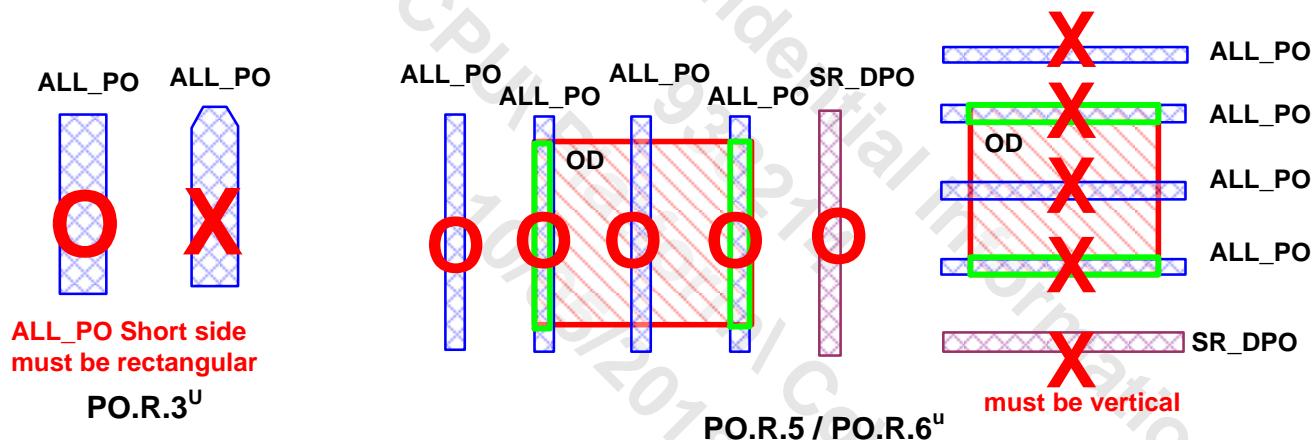
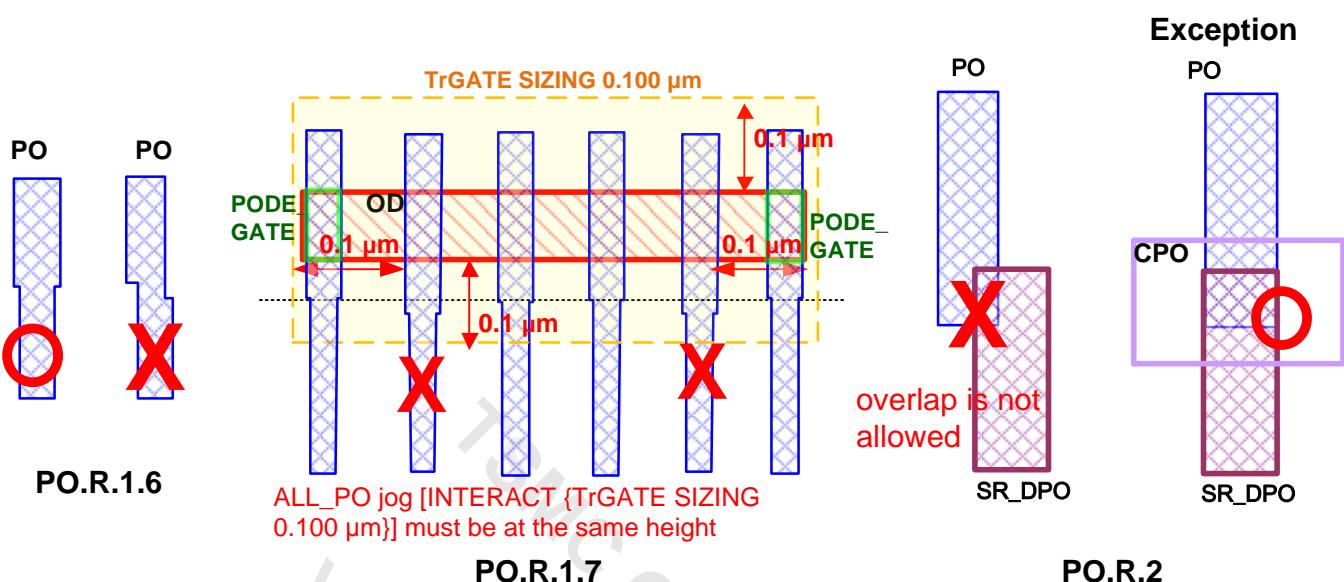
JW1 ≠ JW2

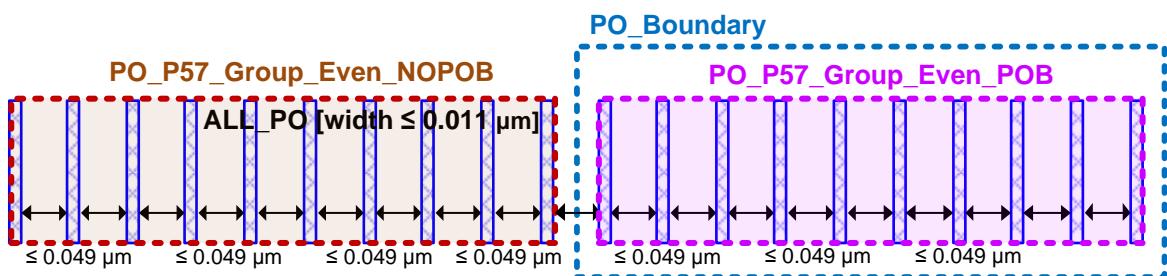
PO.R.1.4



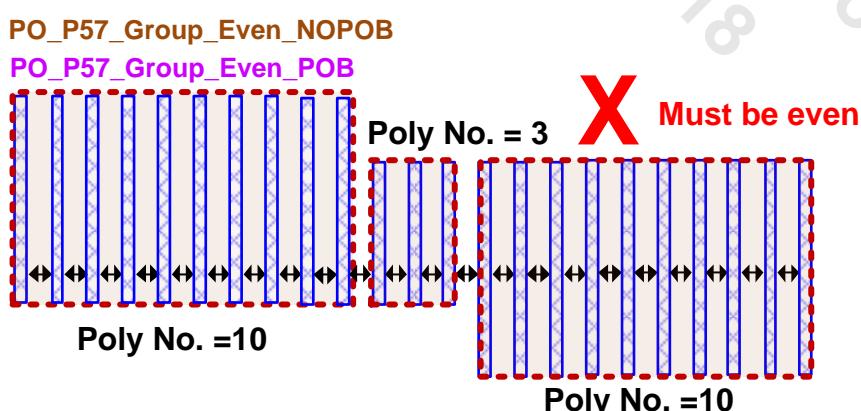
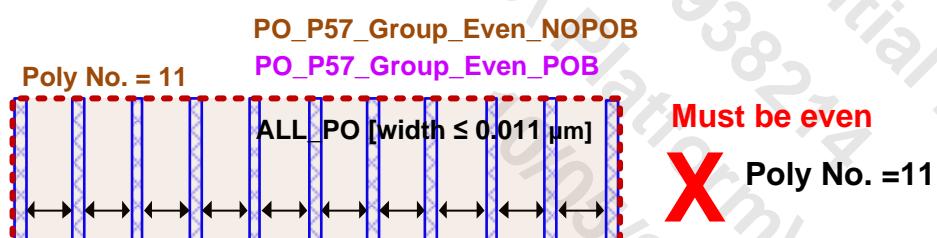
ALL_PO jog length [INSIDE CPO] must be the same

PO.R.1.5



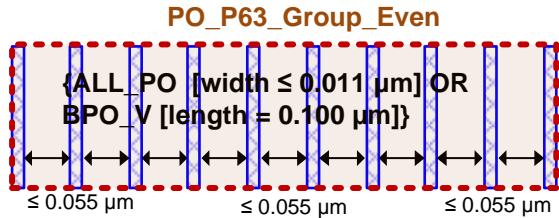


- The number of ALL_PO [width ≤ 0.011 μm] in each PO_P57_Group_Even_NOPOB [poly space ≤ 0.049 μm] must be even
 - The number of ALL_PO [width ≤ 0.011 μm] in each PO_P57_Group_Even_POB [poly space ≤ 0.049 μm] must be even

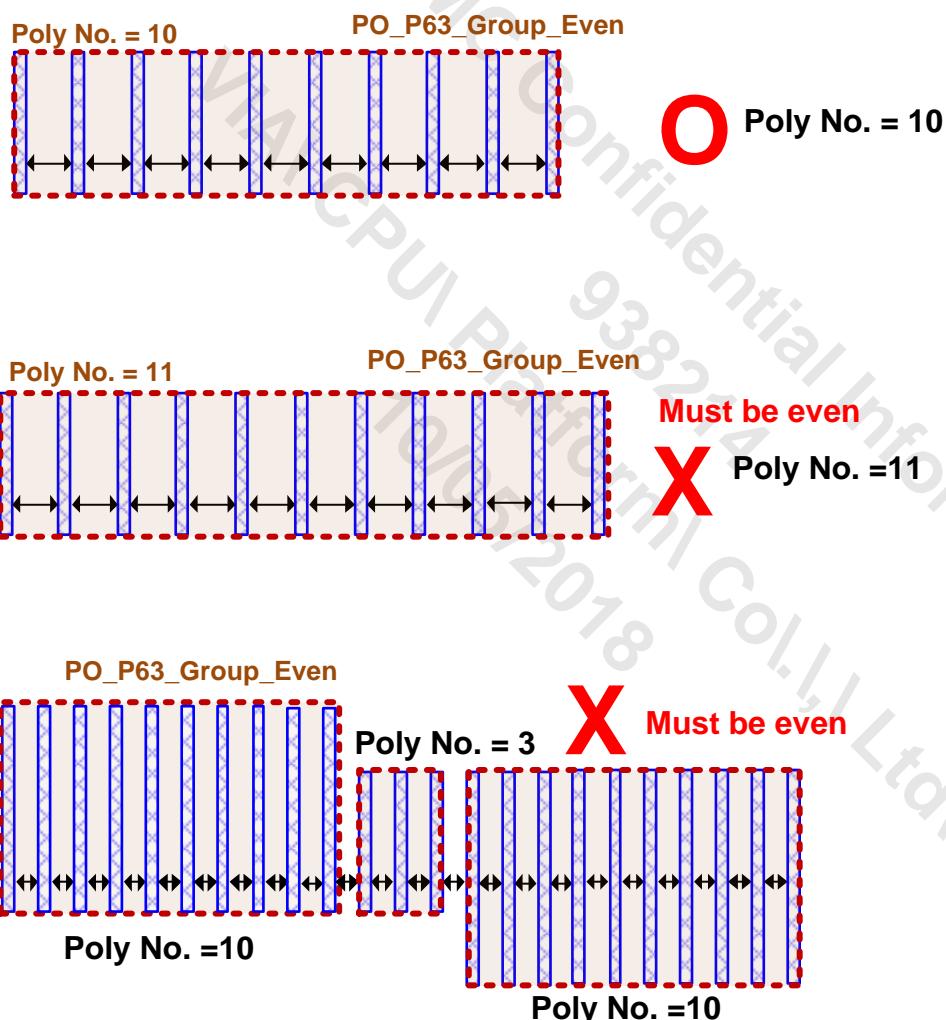


PO.R.15 / PO.R.15.4

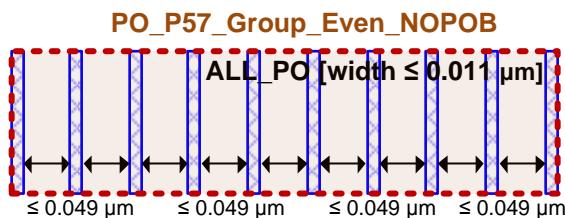
PO_P63



- The number of {ALL_PO [width $\leq 0.011 \mu\text{m}$] OR BPO_V [length = 0.100 μm] } in each PO_P63_Group_Even [poly space $\leq 0.055 \mu\text{m}$] must be even

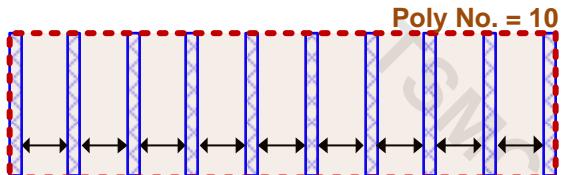


PO.R.15.1



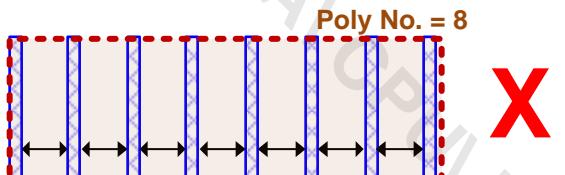
- ALL_PO number in each PO_P57_Group_Even_NOPOB must ≥ 10

PO_P57_Group_Even_NOPOB

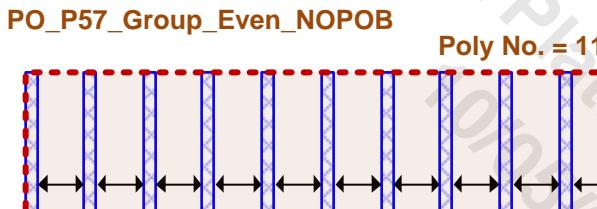


Poly No. ≥ 10 and even

PO_P57_Group_Even_NOPOB



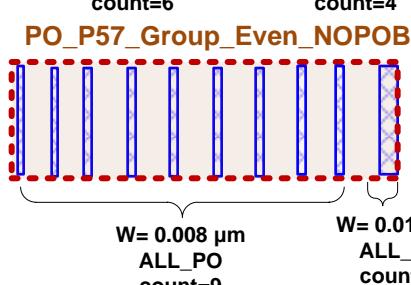
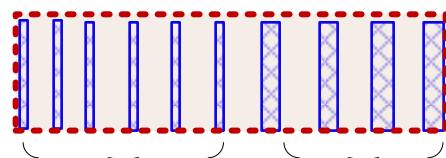
Must ≥ 10
Poly No. < 10



Violate PO.R.15
Poly No. = 11

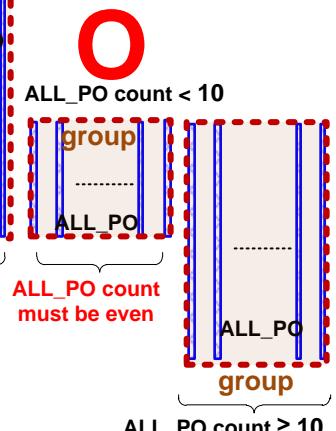
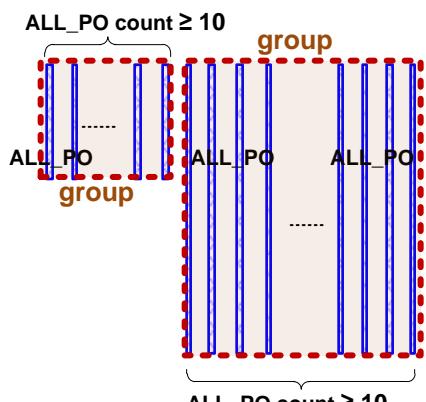
- adjacent ALL_PO number with same width in each PO_P57_Group_Even_NOPOB must be ≥ 4

PO_P57_Group_Even_NOPOB

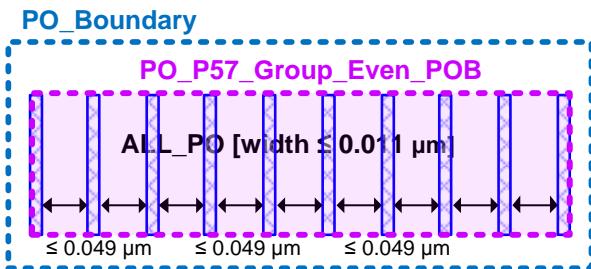


The number of adjacent {ALL_PO NOT CPO} with the same width must ≥ 2

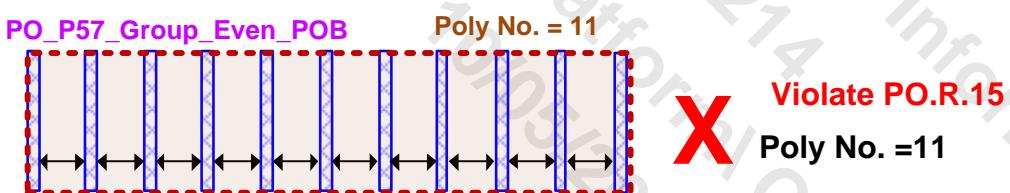
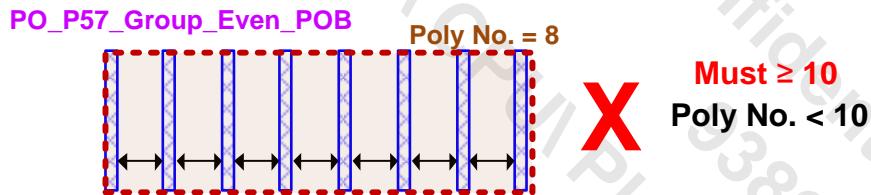
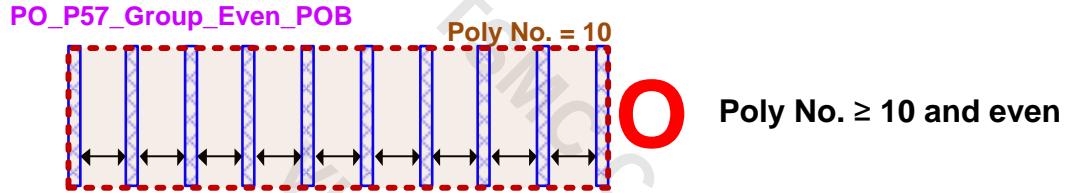
Example:



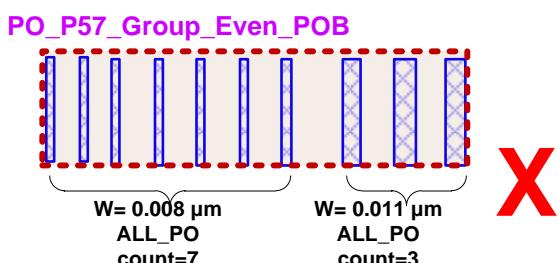
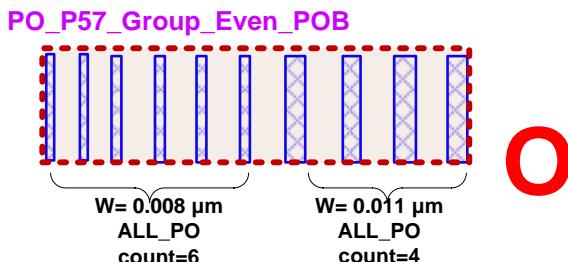
PO.R.15.2



- ALL_PO number in each PO_P57_Group_Even_POB must ≥ 10

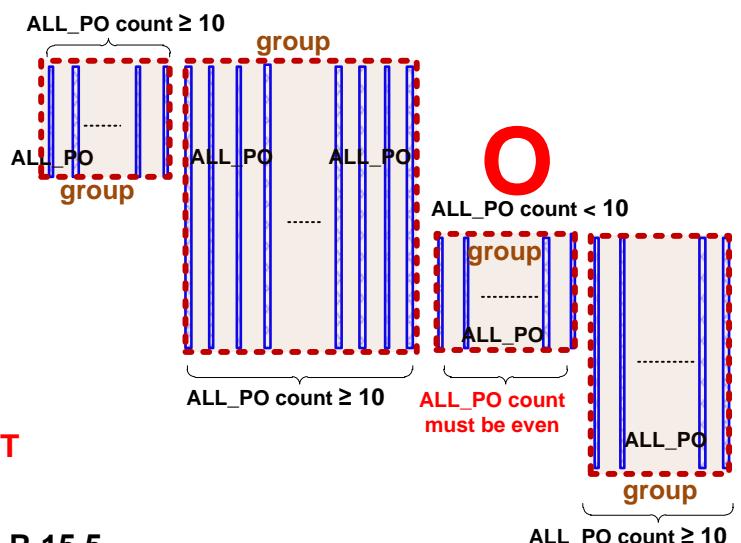


- adjacent ALL_PO number with same width in each PO_P57_Group_Even_POB must be ≥ 4

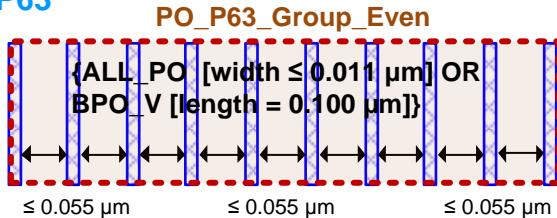


The number of adjacent {ALL_PO NOT CPO} with the same width must ≥ 4

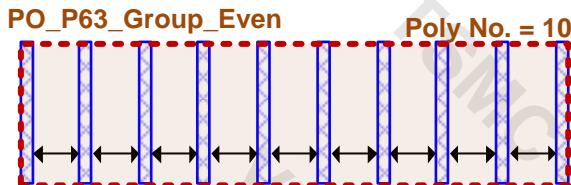
Example:



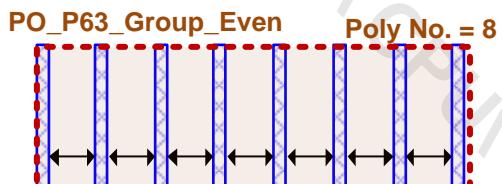
PO.R.15.5

PO_P63

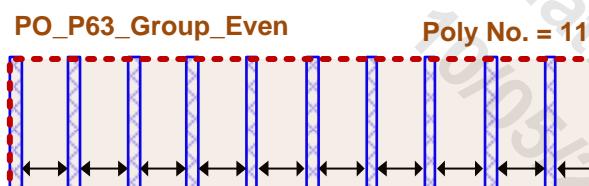
- {ALL_PO [width $\leq 0.011 \mu\text{m}$] OR BPO_V [length = 0.100 μm]} number in each PO_P63_Group_Even must ≥ 10



Poly No. ≥ 10 and even

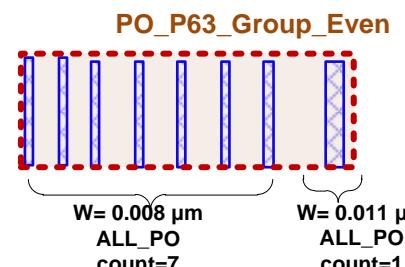
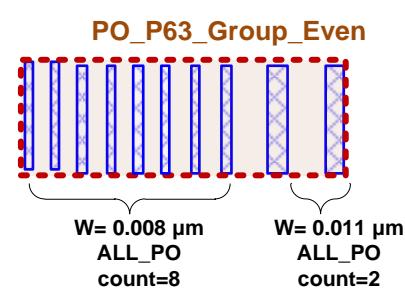


Must ≥ 10
Poly No. < 10



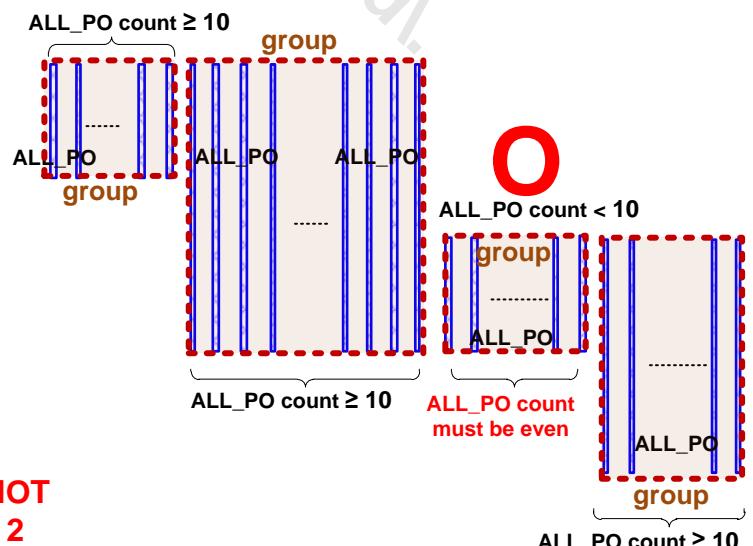
Violate PO.R.15.1
Poly No. = 11

- adjacent ALL_PO number with same width in each PO_P63_Group must be ≥ 2

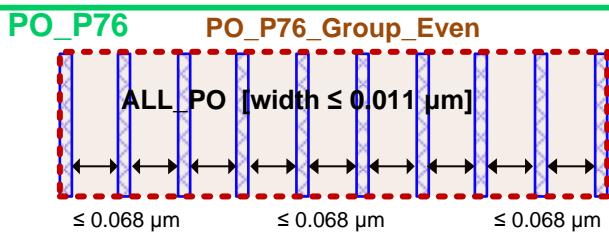


The number of adjacent {ALL_PO NOT CPO} with the same width must ≥ 2

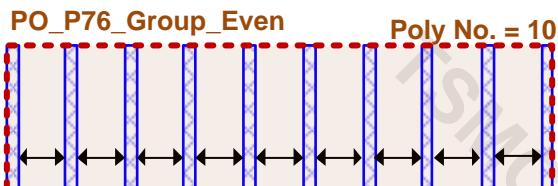
Example:



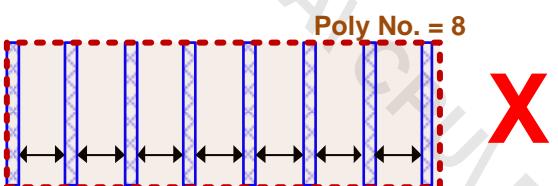
PO.R.15.2.1



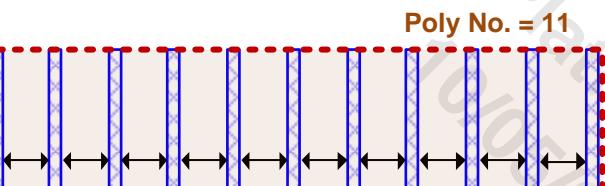
- ALL_PO [width $\leq 0.011 \mu\text{m}$] number in each PO_P76_Group_Even must ≥ 10



Poly No. ≥ 10 and even

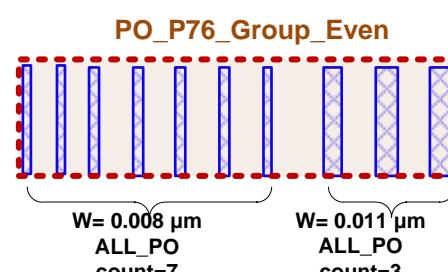
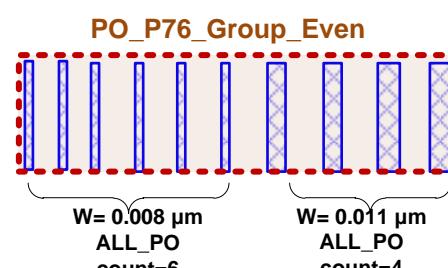


Must ≥ 10
Poly No. < 10



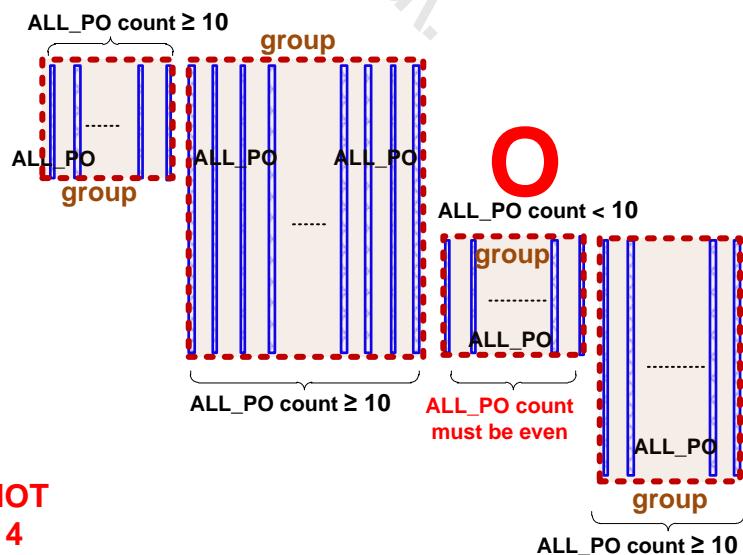
Must be even
Poly No. = 11

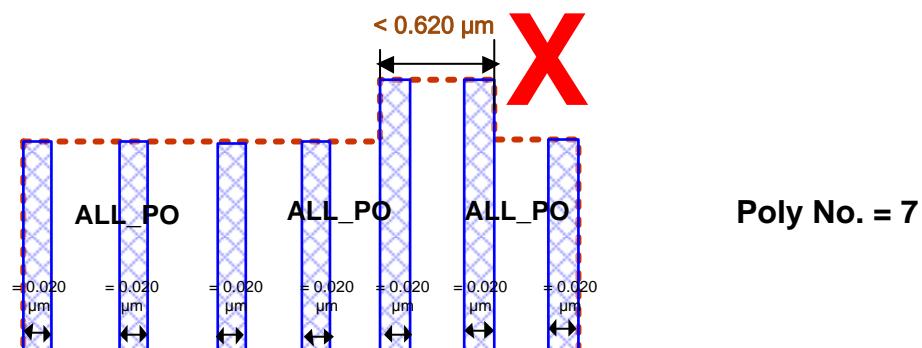
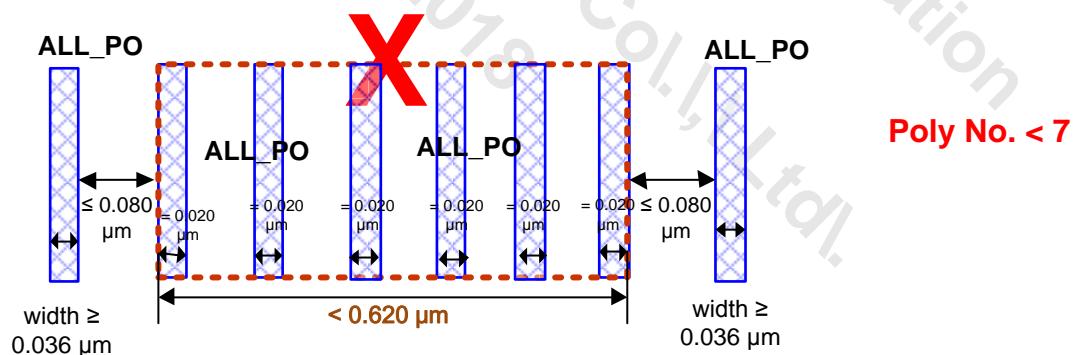
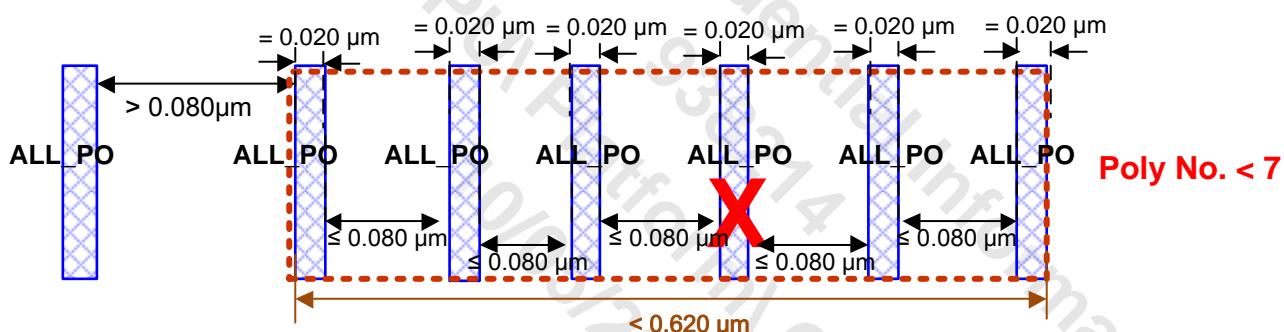
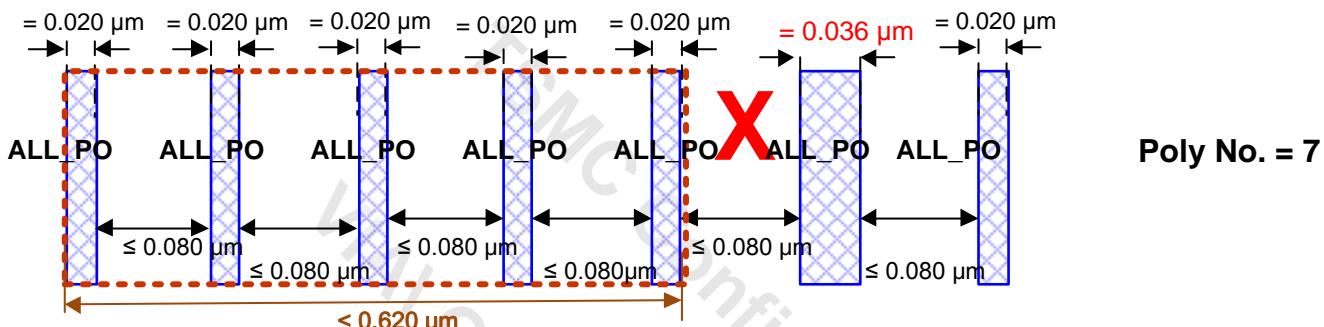
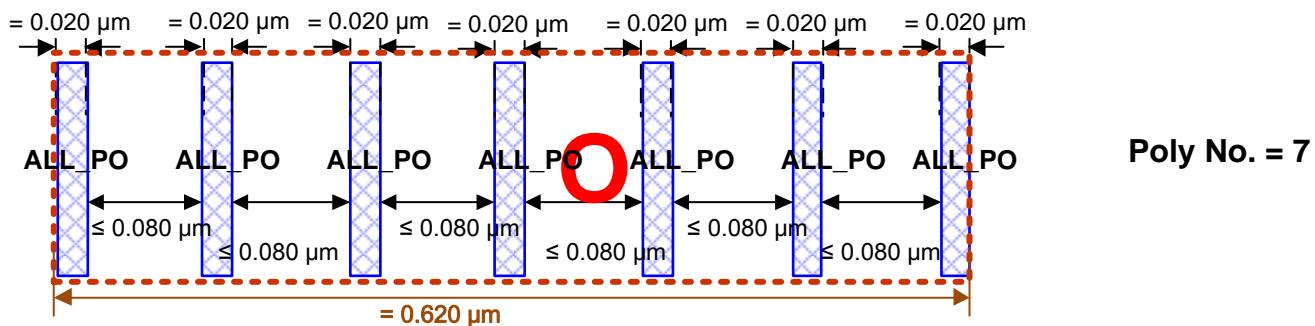
- adjacent ALL_PO number with same width in each PO_P76_Group must be ≥ 4



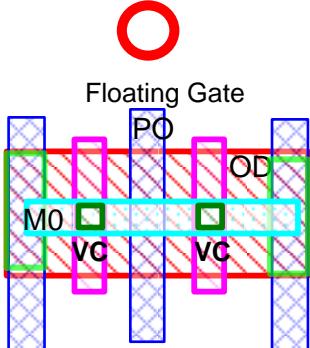
The number of adjacent {ALL_PO NOT CPO} with the same width must ≥ 4

Example:

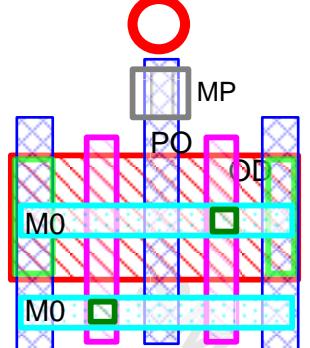




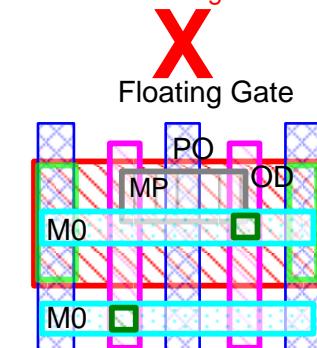
source/drain are connected together



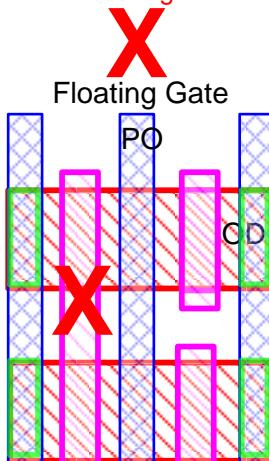
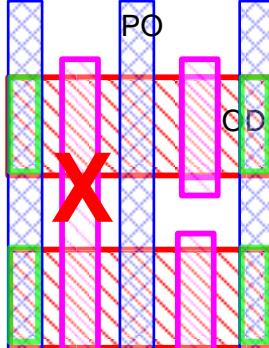
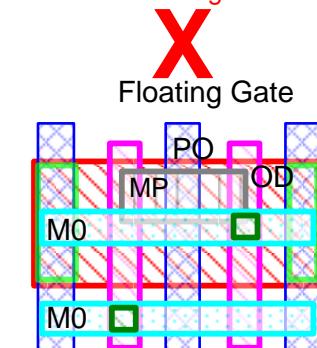
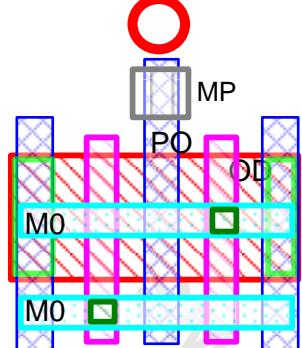
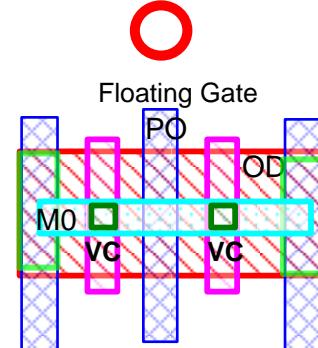
Connect to {MOS OD NOT PO}, STRAP, Gate, or PAD.



Floating gate is prohibited if the effective source/drain are not connected together.

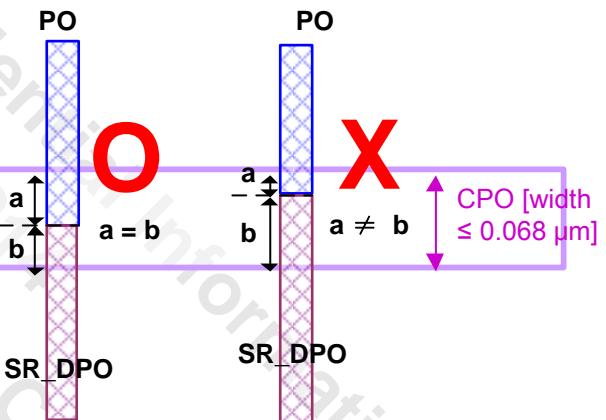
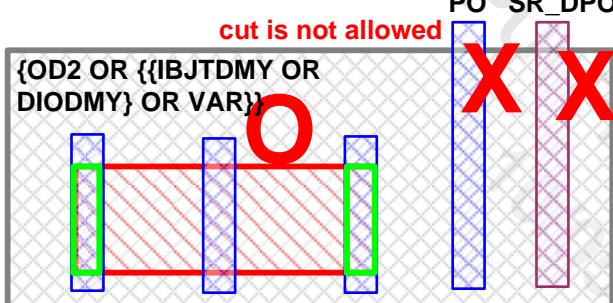


source/drain are not connected together

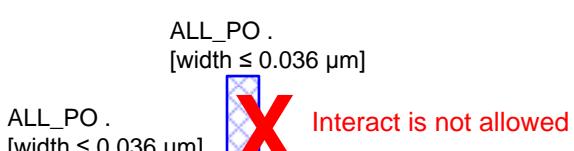



Source/drain is connected to different {MOS OD NOT PO}, STRAP, Gate, or PAD.

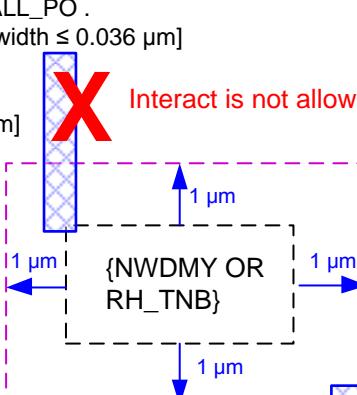
PO.R.19



PO.R.22

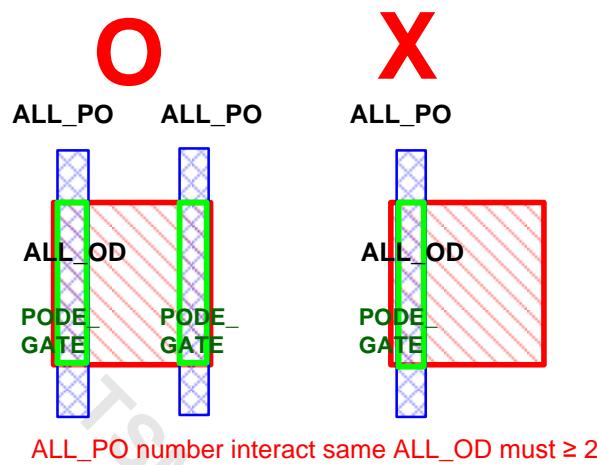


PO.R.24

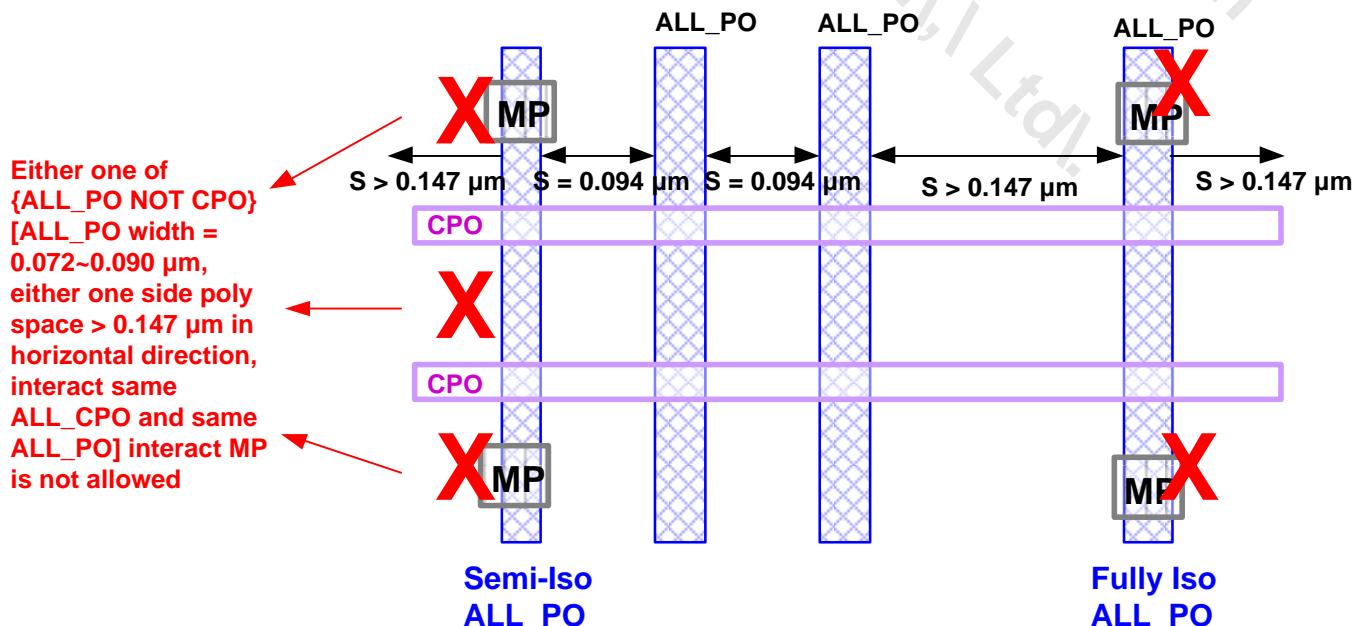
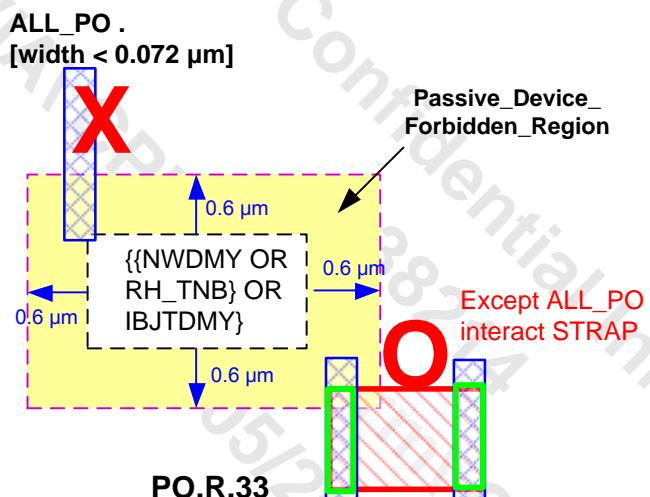


Except ALL_PO interact STRAP

PO.R.25



PO.R.30



PO.R.34

4.5.21 Cut-Poly (CPO) Layout Rules

CPO (CAD layer 17;11) is used to cut poly.

SR_DCPO (CAD layer 17;23) is used to cut poly inside Dummy_Cell.

ALL_CPO = {CPO OR SR_DCPO}

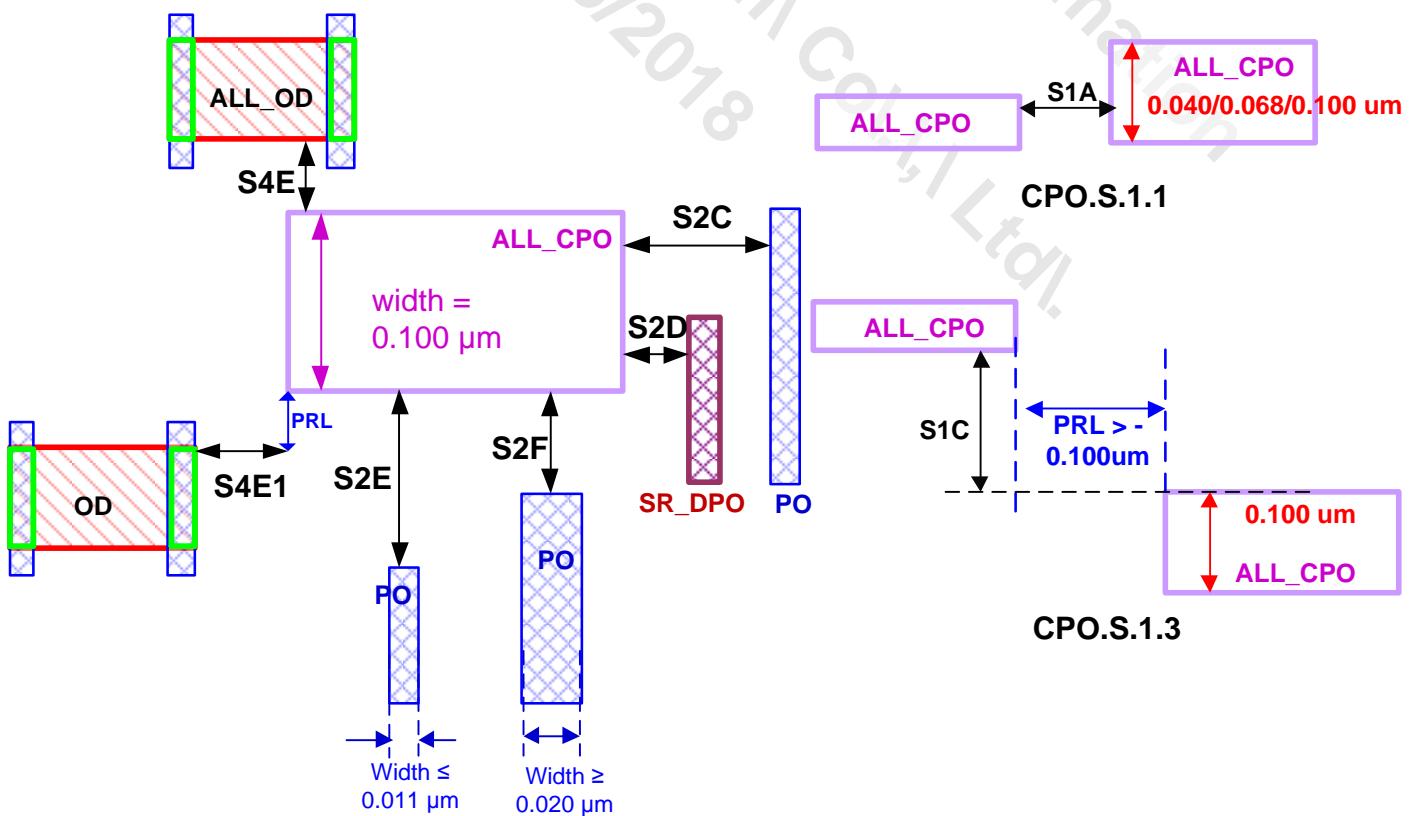
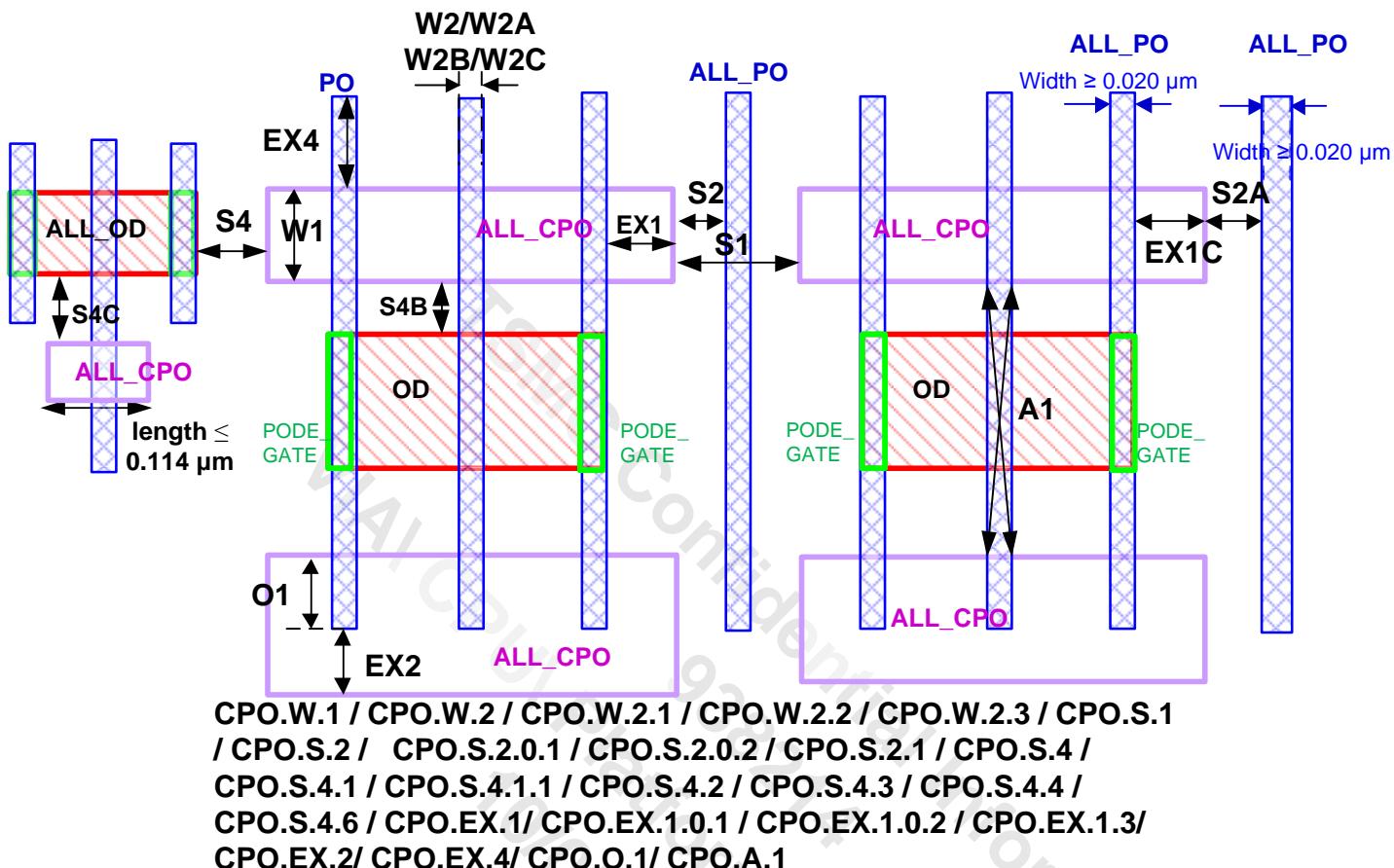
Rule No.	Description	Label	Op.	Rule
CPO.W.1	Width of ALL_CPO in vertical direction (Except FB_8)	W1	=	0.0160, 0.0400, 0.0680, 0.1000
CPO.W.2	Maximum width of {{ALL_PO INTERACT ALL_CPO} NOT OD2}	W2	\leq	0.0900
CPO.W.2.1	Maximum width of {{ALL_PO INTERACT ALL_CPO [width = 0.040 μm] NOT OD2}}	W2A	\leq	0.0360
CPO.W.2.2	Maximum width of {{ALL_PO INTERACT ALL_CPO [width = 0.016 μm] NOT OD2}}	W2B	\leq	0.0110
CPO.W.2.3	Width of {{ALL_PO INTERACT ALL_CPO [width = 0.040/0.068 μm] NOT OD2}}	W2C	\geq	0.0200
CPO.S.1	Space of ALL_CPO	S1	\geq	0.0540
CPO.S.1.1	Space of ALL_CPO to ALL_CPO [width = 0.040/0.068/0.100 μm]	S1A	\geq	0.0700
CPO.S.1.3	Space to ALL_CPO [width = 0.100 μm] in vertical direction [PRL > -0.100 μm]	S1C	\geq	0.0700
CPO.S.2	Space of ALL_CPO to ALL_PO (Except following conditions: 1. ALL_PO [width = 0.008/0.011 μm] abut ALL_CPO [width = 0.100 μm])	S2	\geq	0.0230
CPO.S.2.0.1	Space of ALL_CPO to ALL_PO [INSIDE PO_P63] (Except following conditions: 1. ALL_PO [width = 0.008/0.011 μm] abut ALL_CPO [width = 0.100 μm])	S2	\geq	0.0260
CPO.S.2.0.2	Space of ALL_CPO to ALL_PO [INSIDE PO_P76] (Except following conditions: 1. ALL_PO [width = 0.008/0.011 μm] abut ALL_CPO [width = 0.100 μm])	S2	\geq	0.0325
CPO.S.2.1	Space of ALL_CPO to ALL_PO [width \geq 0.020 μm]	S2A	\geq	0.0400
CPO.S.2.3	Space of ALL_CPO [width = 0.100 μm] to PO in horizontal direction	S2C	\geq	0.0770
CPO.S.2.4	Space of ALL_CPO [width = 0.100 μm] to SR_DPO in horizontal direction	S2D	\geq	0.0230
CPO.S.2.4.1	Space of ALL_CPO [width = 0.100 μm] to SR_DPO in horizontal direction [INSIDE PO_P63]	S2D	\geq	0.0260
CPO.S.2.4.2	Space of ALL_CPO [width = 0.100 μm] to SR_DPO in horizontal direction [INSIDE PO_P76]	S2D	\geq	0.0325
CPO.S.2.5	Space of ALL_CPO [width = 0.100 μm] to ALL_PO [width \leq 0.011 μm] in vertical direction [PRL > -0.077 μm] (Except following conditions: 1. ALL_PO [width = 0.008/0.011 μm] abut ALL_CPO [width = 0.100 μm], 2. small ALL_PO jog \leq 0.002 μm)	S2E	\geq	0.1700
CPO.S.2.6	Space of ALL_CPO [width = 0.100 μm] to ALL_PO [width \geq 0.020 μm] in vertical direction [PRL > -0.077 μm]	S2F	\geq	0.1000
CPO.S.4	Space of ALL_CPO to ALL_OD (Overlap is not allowed)	S4	\geq	0.0230
CPO.S.4.1	Space of ALL_CPO to ALL_OD in horizontal direction [INSIDE PO_P63]	S4	\geq	0.0260
CPO.S.4.1.1	Space of ALL_CPO to ALL_OD in horizontal direction [INSIDE PO_P76]	S4	\geq	0.0325
CPO.S.4.2	Space of ALL_CPO to ALL_OD [INTERACT ALL_PO] in vertical direction (Overlap is not allowed) (Except following conditions: 1. ALL_CPO [INSIDE {CCP_9 OR CCP_8}])	S4B	\geq	0.0300
CPO.S.4.3	Space of ALL_CPO [length \leq 0.114 μm] to ALL_OD [INTERACT ALL_PO] in vertical direction (Overlap is not allowed) (Except following conditions: 1. ALL_CPO [INSIDE {CCP_9 OR CCP_8}])	S4C	\geq	0.0330
CPO.S.4.4	Space of ALL_CPO [length \leq 0.126 μm] to ALL_OD [INTERACT ALL_PO] in vertical direction [INSIDE PO_P63] (Overlap is not allowed) (Except following conditions: 1. ALL_CPO [INSIDE {CCP_9 OR CCP_8}])	S4C	\geq	0.0330

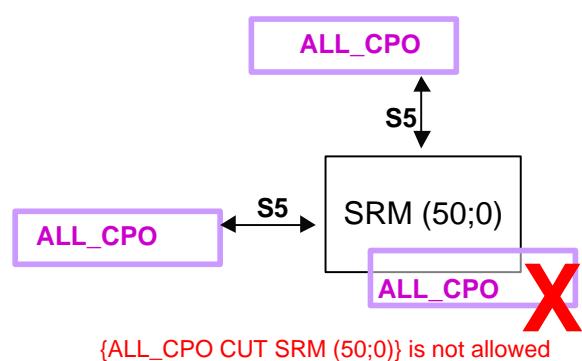
Rule No.	Description	Label	Op.	Rule
CPO.S.4.5	Space of ALL_CPO [width = 0.100 μm] to ALL_OD (Except Dummy_Cell)	S4E	≥	0.0420
CPO.S.4.5.1	Space of CPO [width = 0.100 μm] to OD in horizontal direction [PRL > -0.042 μm]	S4E1	≥	0.0800
CPO.S.4.6	Space of ALL_CPO [length ≤ 0.152 μm] to ALL_OD [INTERACT ALL_PO] in vertical direction [INSIDE PO_P76] (Overlap is not allowed)	S4C	≥	0.0330
CPO.S.5	Space of ALL_CPO to SRM (50;0) {ALL_CPO CUT SRM (50;0)} is not allowed	S5	≥	0.1080
CPO.EX.1	ALL_CPO extension on ALL_PO [width ≤ 0.011 μm] in CPO length direction (Except Dummy_Cell, PO_P63, PO_P76, or following conditions: 1. PO [edge space to ALL_PO following PO.S.1.2]) DRC checks {ALL_CPO NOT {ALL_CPO SIZING -0.046 μm in horizontal direction}} must interact ALL_PO	EX1	=	0.0230~0.0460
CPO.EX.1.0.1	ALL_CPO extension on ALL_PO [width ≤ 0.011 μm] in CPO length direction [INSIDE PO_P63] (Except Dummy_Cell, or following conditions: 1. PO [edge space to ALL_PO following PO.S.1.2.2]) DRC checks {ALL_CPO NOT {ALL_CPO SIZING -0.049 μm in horizontal direction}} must interact ALL_PO	EX1	=	0.0260~0.0490
CPO.EX.1.0.2	ALL_CPO extension on ALL_PO [width ≤ 0.011 μm] in CPO length direction [INSIDE PO_P76] (Except Dummy_Cell, or following conditions: 1. PO [edge space to ALL_PO following PO.S.1.2.3]) DRC checks {ALL_CPO NOT {ALL_CPO SIZING -0.0495 μm in horizontal direction}} must interact ALL_PO	EX1	=	0.0325~0.0495
CPO.EX.1.1	ALL_CPO extension on ALL_PO [one side poly space > 0.080 μm, width = 0.020 μm] in CPO length direction (Except following conditions: 1. ALL_CPO extension on SR_DPO [one side poly space > 0.080 μm, width = 0.020 μm] ≥ 0.040 μm)	EX1A	=	0.0510
CPO.EX.1.3	ALL_CPO extension on ALL_PO [width ≥ 0.020 μm] in CPO length direction (Except following conditions: 1. PO [edge space to ALL_PO following PO.S.1.3, or PO.S.2]) DRC checks {ALL_CPO NOT {ALL_CPO SIZING -0.051 μm in horizontal direction}} must interact ALL_PO	EX1C	=	0.0400~0.0510
CPO.EX.1.5	{ALL_CPO [width = 0.100 μm] SIZING 0.010 μm in CPO width direction} extension on ALL_PO in CPO length direction (Except following conditions: 1. PO [edge space to ALL_PO following PO.S.1.2, or PO.S.1.2.2, or PO.S.1.2.3], 2. ALL_CPO [width = 0.100 μm] extension on SR_DPO ≥ 0.023 μm)	EX1E	=	0.0500~0.0520
CPO.EX.2	ALL_CPO extension on ALL_PO in vertical direction [PRL > -0.040 μm] (Except following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	EX2	≥	0.0280
CPO.EX.4	ALL_PO extension on ALL_CPO [width = 0.016/0.040/0.068 μm]	EX4	≥	0.0900
CPO.O.1	Overlap of ALL_PO in ALL_CPO [width = 0.040/0.068 μm] width direction (Except DC2_CORE (257;22))	O1	≥	0.0400
CPO.O.2	ALL_CPO [width = 0.100 μm] overlap of PO [width = 0.008/0.011 μm] in CPO width direction	O2	=	0
CPO.O.2.1	ALL_CPO [width = 0.100 μm] overlap of SR_DPO [width = 0.008/0.011 μm] in CPO width direction	O2A	=	0, 0.1000
CPO.L.1	Length of ALL_CPO in horizontal direction	L1	≥	0.0570
CPO.L.1.1	Length of ALL_CPO [width = 0.040/0.068 μm] in horizontal direction	L1A	≥	0.1000
CPO.L.1.2	Length of ALL_CPO [width = 0.100 μm] in horizontal direction	L1B	≥	0.5700
CPO.A.1	Area of {ALL_PO NOT ALL_CPO}	A1	≥	0.00073

Rule No.	Description	Label	Op.	Rule
CPO.DN.1.1	Maximum {ALL_CPO OR CPO_SRAM} density in window 20 μm x 20 μm , stepping 10 μm (Except TCDDMY, ICOVL_SINGLE)		\leq	15%
CPO.DN.2	Maximum {ALL_CPO OR CPO_SRAM} density across full chip		\leq	12%
CPO.DN.3	Minimum {ALL_CPO OR CPO_SRAM} density across full chip (Except SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	5%
CPO.R.1	ALL_CPO must be a rectangle orthogonal to grid			
CPO.R.1.1	Short side of ALL_PO [width = 0.008/0.011 μm] must fully abut ALL_CPO [width = 0.100 μm] (Except BLK_WF)			
CPO.R.3	ALL_CPO [INTERACT OD2] is not allowed (Except following conditions: 1. {DC_Core OR DC_IO})			
CPO.R.3.1	{(ALL_PO INTERACT ALL_CPO) INTERACT OD2} is not allowed (Except following conditions: 1. {DC_Core OR DC_IO})			
CPO.R.4	ALL_CPO must interact ALL_PO (ALL_CPO abut ALL_PO is not allowed) (Except following conditions: 1. ALL_CPO [width = 0.100 μm] abut ALL_PO [width = 0.008/0.011 μm])			
CPO.R.6	Any vertex of ALL_CPO inside ALL_PO is not allowed			
CPO.R.7	Last ALL_PO [INTERACT ALL_CPO length \geq 3 μm] interact MP is not allowed (Except following conditions: 1. ALL_CPO inside CCP_9, CCP_8, 2. {ALL_PO NOT ALL_CPO} is the same net [INTERACT the same ALL_CPO]) Definition of Last ALL_PO: a set of {ALL_PO NOT ALL_CPO} [INTERACT ALL_CPO], and the Last ALL_PO is the one which most closest to ALL_CPO edge DRC only check ALL_PO cross ALL_CPO case			
CPO.R.8	Short side of ALL_PO [width = 0.020 μm] must interact ALL_CPO			
CPO.R.9.1	ALL_CPO width [INTERACT neighboring two ALL_PO of TrGATE [{SIZING 0.010 μm } AND PO], in horizontal and outside OD direction], and the ALL_CPO number must be only one (Except FB_8)		=	0.0160, 0.0400, 0.0680
CPO.R.10	ALL_PO [width \geq 0.020 μm] interact ALL_CPO [width = 0.100 μm] is not allowed			
CPO.R.13	SR_DCPO interact {PO OR CPO} is not allowed			
CPO.R.15	ALL_CPO overlap {{OD [INTERACT MOS] SIZING 0.030 μm in vertical direction} SIZING 0.057 μm in horizontal direction} is not allowed. (Except FB_9, FB_8)			
CPO.R.15.1	ALL_CPO overlap {{OD [INTERACT MOS] SIZING 0.030 μm in vertical direction} SIZING 0.063 μm in horizontal direction} is not allowed [INSIDE PO_P63] (Except FB_9, FB_8)			
CPO.R.15.2	ALL_CPO overlap {{OD [INTERACT MOS] SIZING 0.030 μm in vertical direction} SIZING 0.076 μm in horizontal direction} is not allowed [INSIDE PO_P76] (Except FB_9, FB_8)			

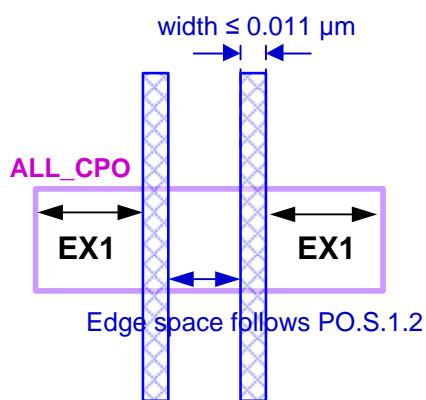
Rule No.	Description	Label	Op.	Rule
CPO.G0.0	<p>G0-SPACE definition:</p> <ol style="list-style-type: none"> 1. G0 X space (G0XS) of ALL_CPO [width = 0.016/0.030 μm] to ALL_CPO < 0.108 μm [PRL > -0.096 μm] 2. G0 Y space (G0YS) of ALL_CPO [width = 0.016/0.030 μm] to ALL_CPO < 0.096 μm [PRL > -0.108 μm] 3. G0 X space (G0XS) of ALL_CPO [width = 0.040/0.068 μm] to ALL_CPO < 0.108 μm [PRL > -0.128 μm] 4. G0 Y space (G0YS) of ALL_CPO [width = 0.040/0.068 μm] to ALL_CPO < 0.128 μm [PRL > -0.108 μm] 5. G0 X space (G0XS) of ALL_CPO [width = 0.100 μm] to ALL_CPO < 0.108 μm [PRL > -0.120 μm] 6. G0 Y space (G0YS) of ALL_CPO [width = 0.100 μm] to ALL_CPO < 0.120 μm [PRL > -0.108 μm] <p>G0-AREA definition:</p> <ol style="list-style-type: none"> 1. G0 run-run area (G0RA): The projection area between 2 edges with G0XS/G0YS 2. G0-AREA is independent to all other ones, even if they are overlapped or crossed <p>Loop:</p> <ol style="list-style-type: none"> 1. A loop is formed when ALL_CPO polygons are connected in a cyclic sequence with G0-AREA in between 2. A loop cannot contain any sub-loops which share one or more polygons with it 			
CPO.G0.1	G0-AREA cannot be formed by single polygon			
CPO.G0.2	G0-AREA count of the close loop formed by original polygons and G0-Areas cannot be odd number			

CPO

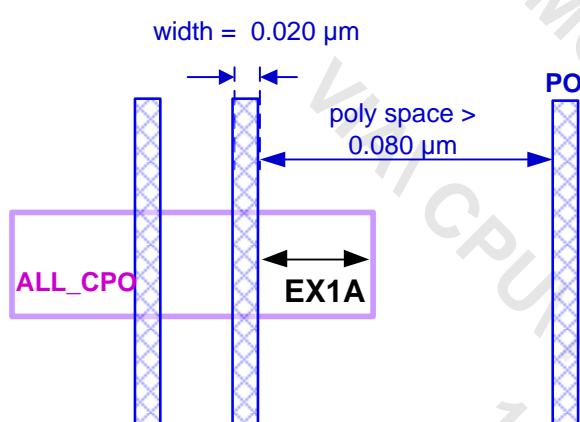




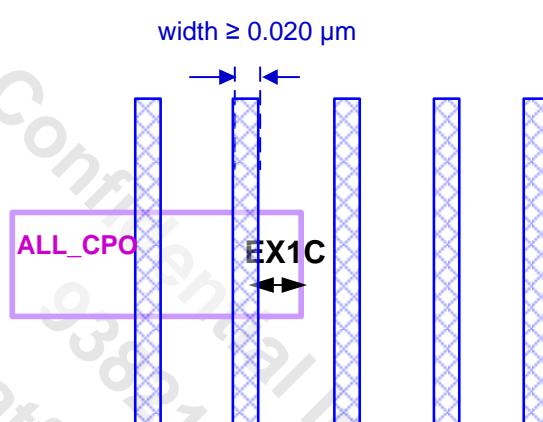
{ALL_CPO CUT SRM (50;0)} is not allowed



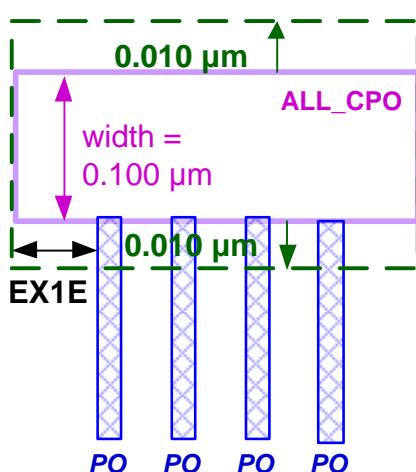
CPO.S.5



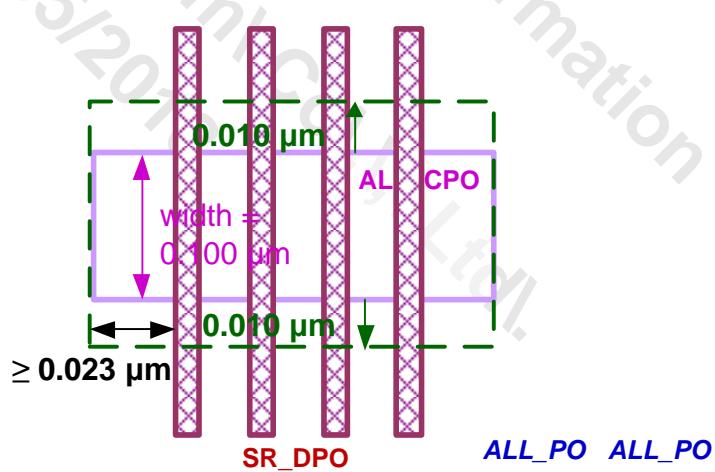
CPO.EX.1



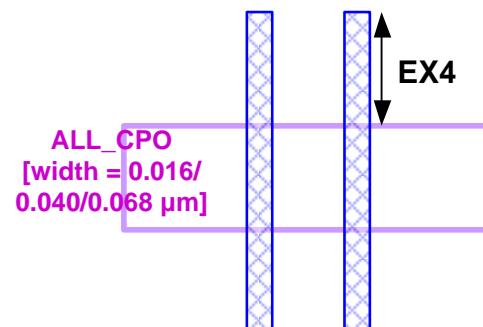
CPO-FX-1.1



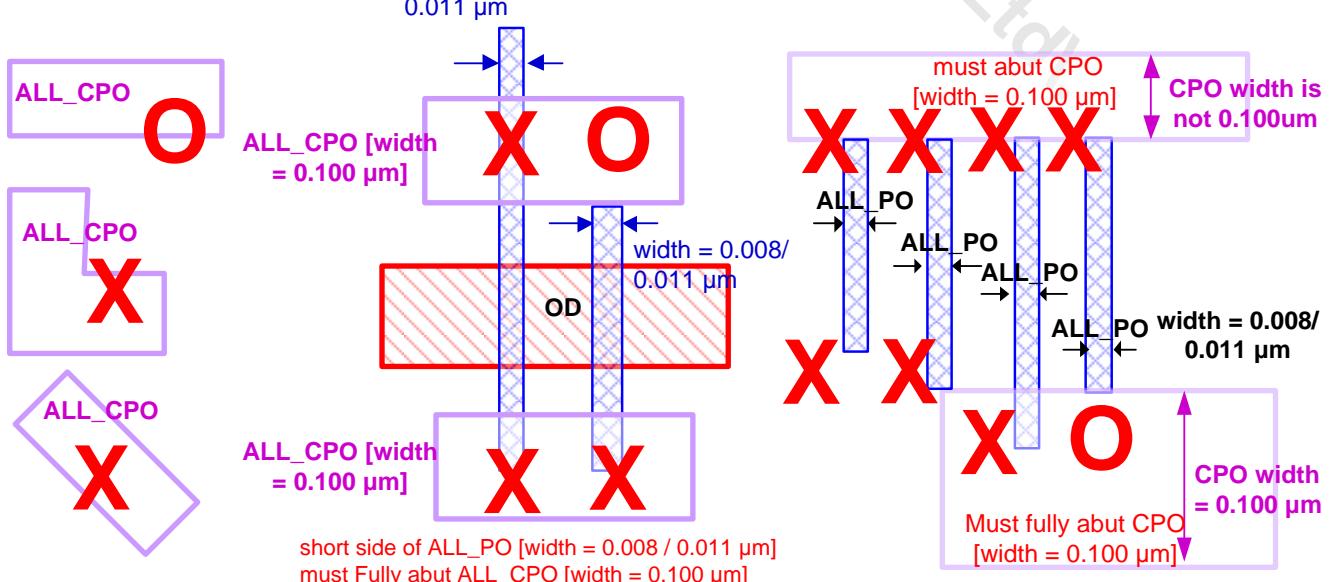
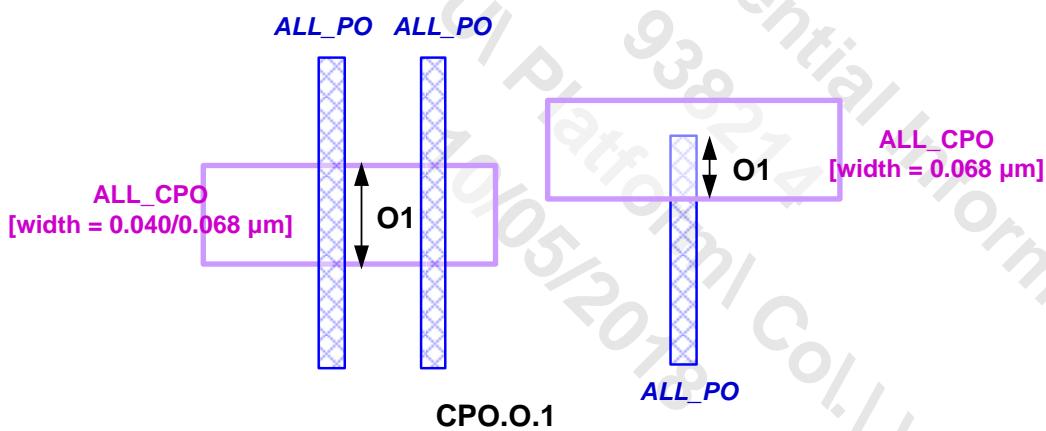
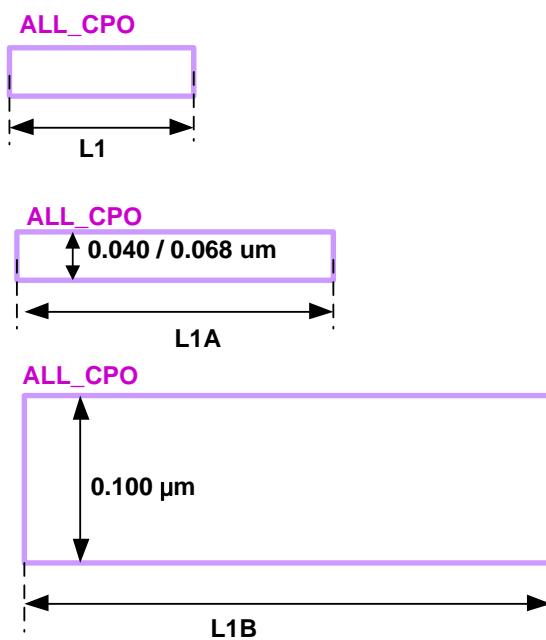
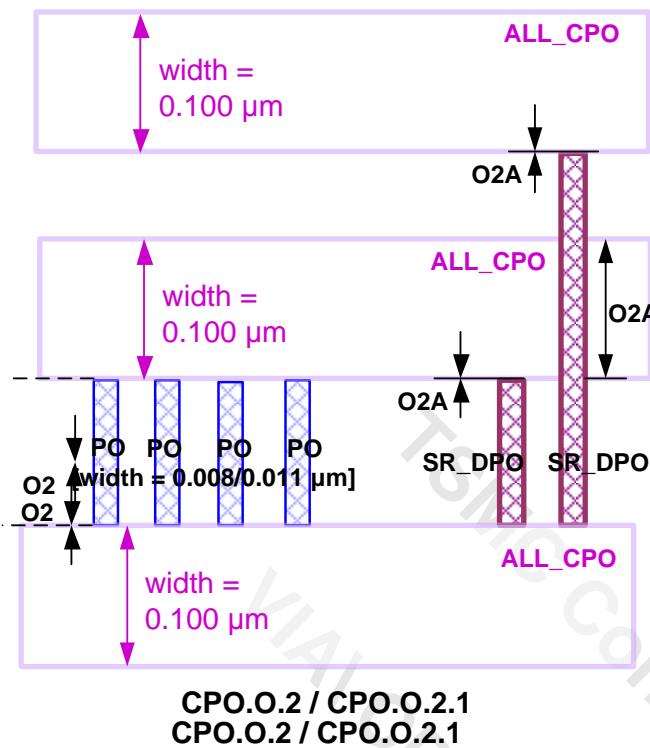
CPO FX 1.3

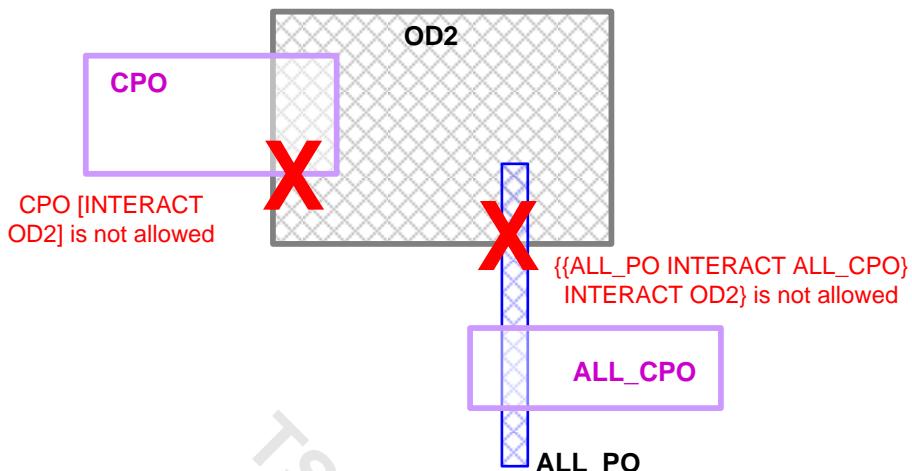


CPO.EX.1.5



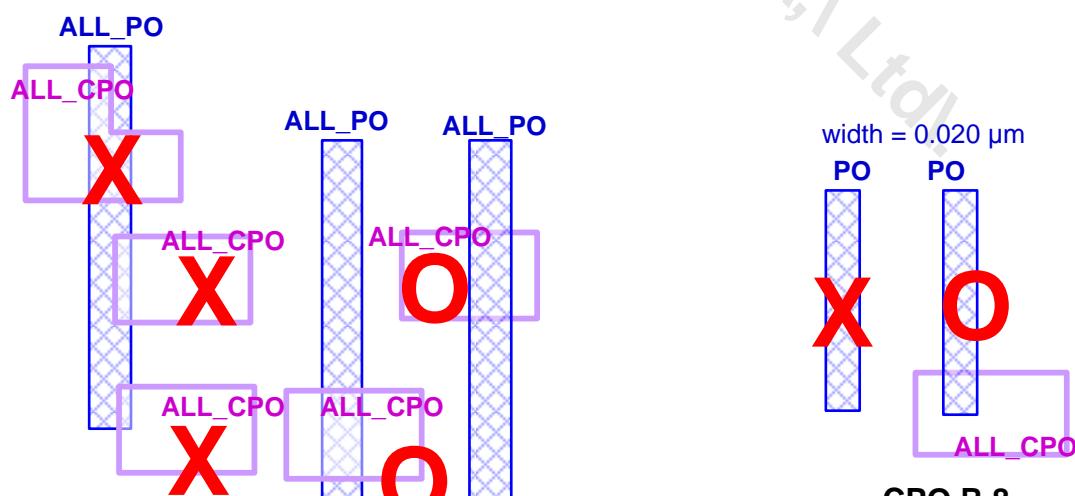
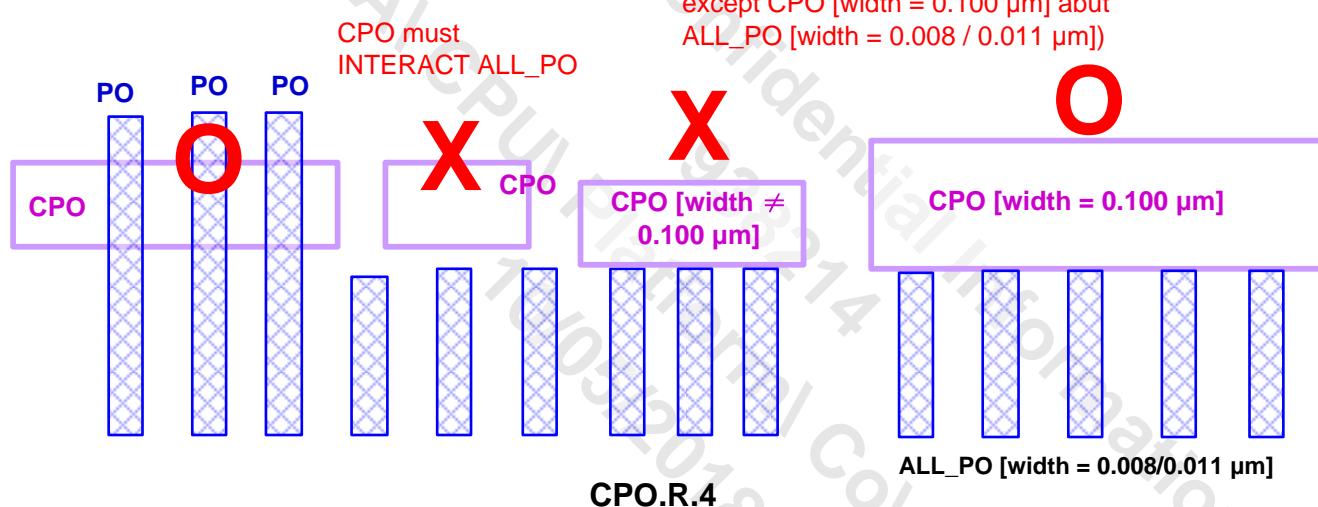
CPO.EX.4





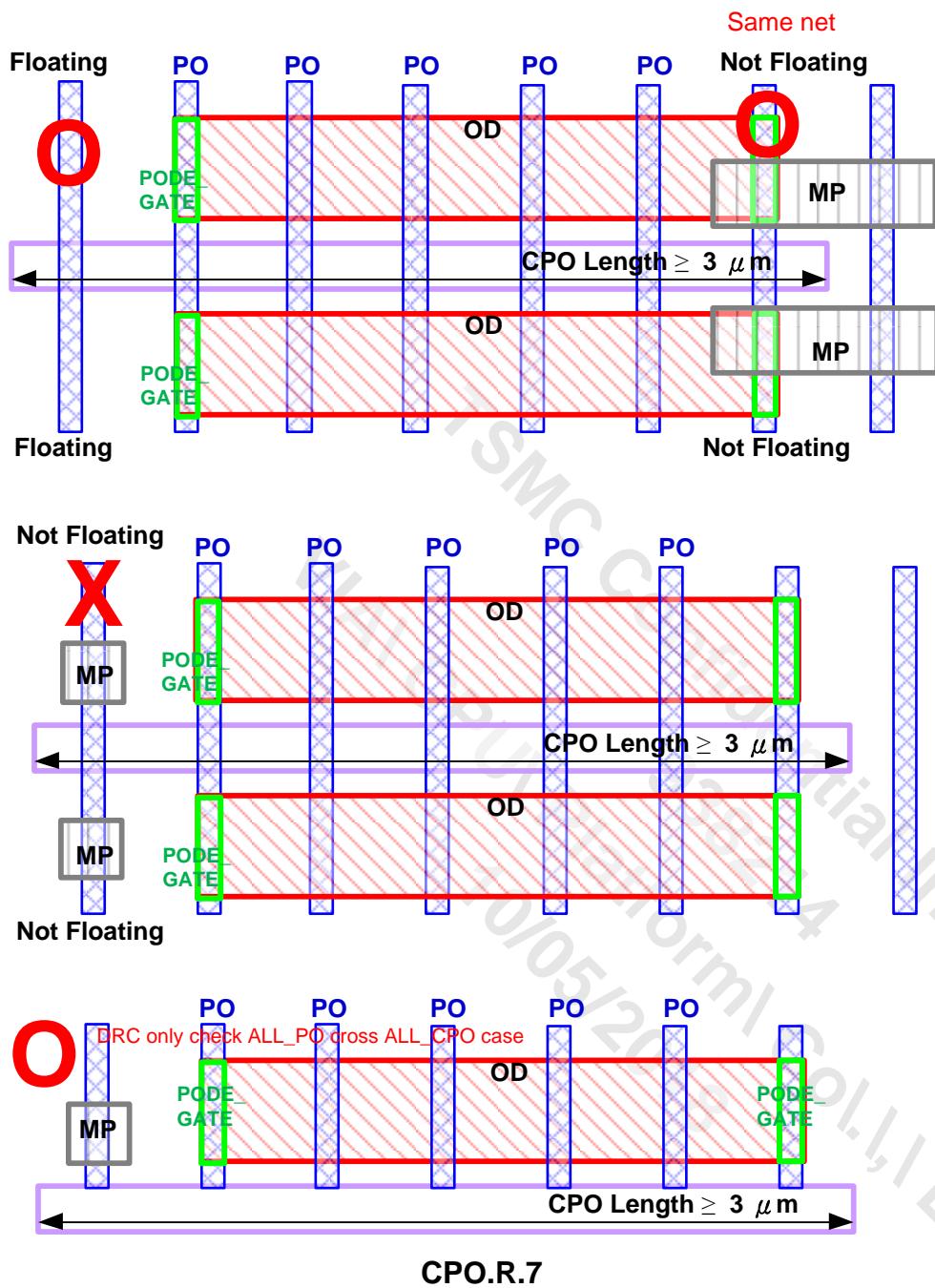
CPO.R.3/ CPO.R.3.1

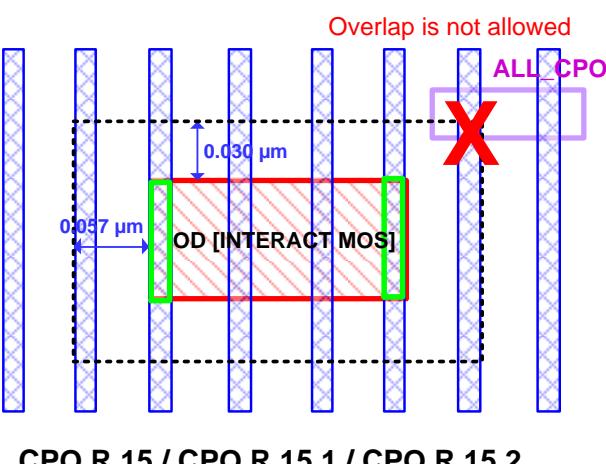
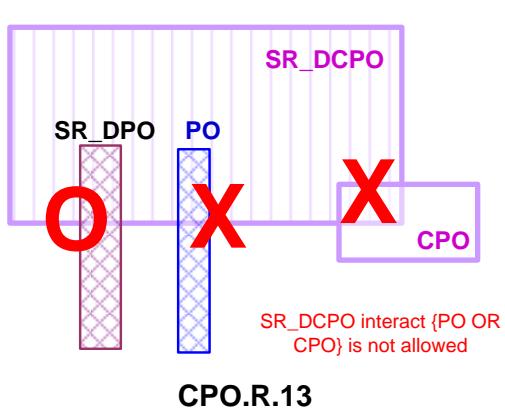
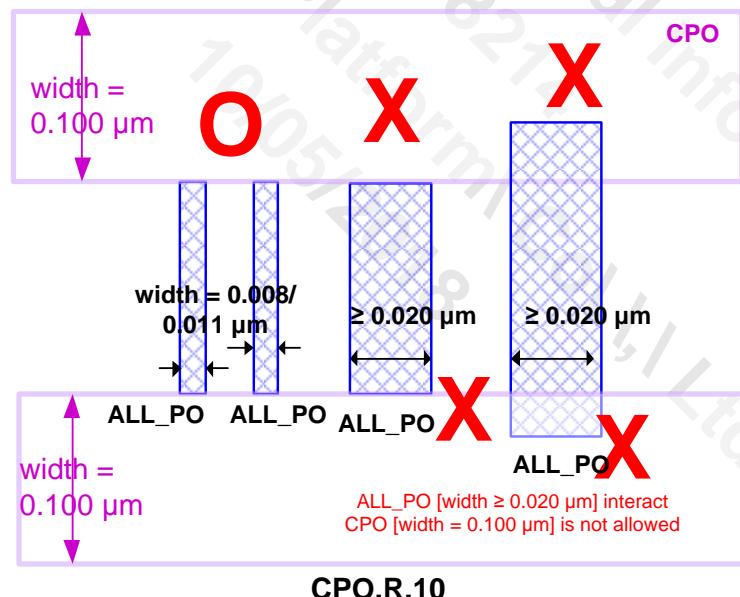
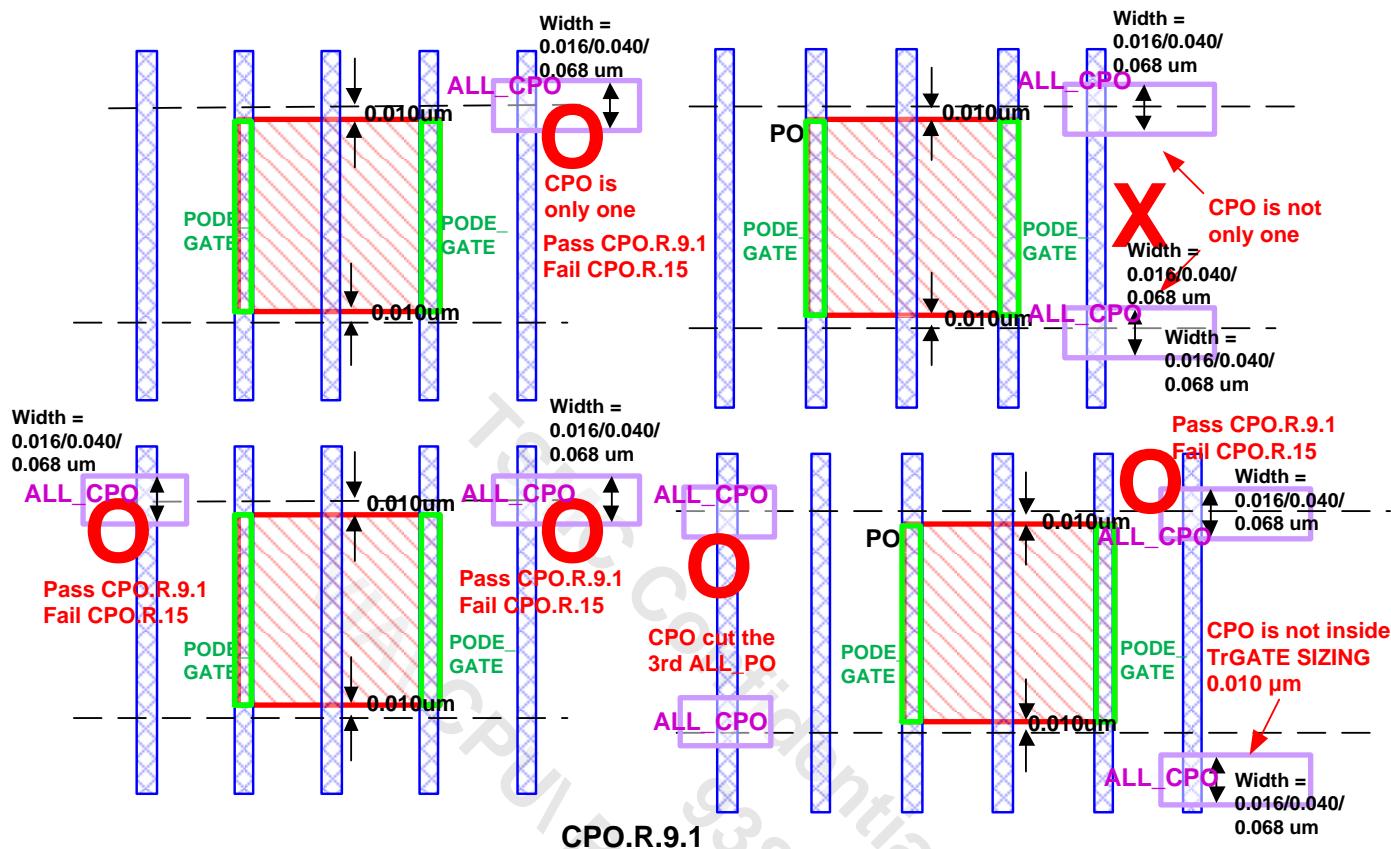
CPO abut ALL_PO is not allowed,
except CPO [width = 0.100 µm] abut
ALL_PO [width = 0.008 / 0.011 µm]

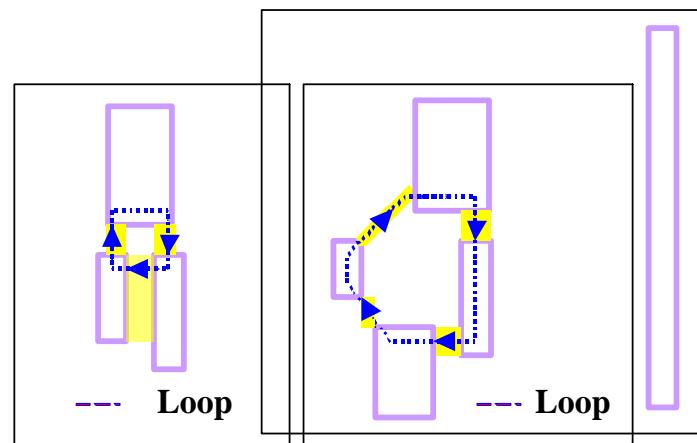
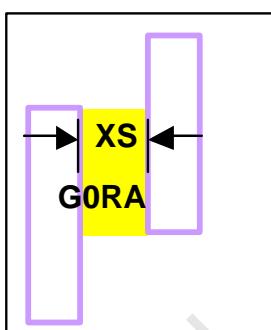
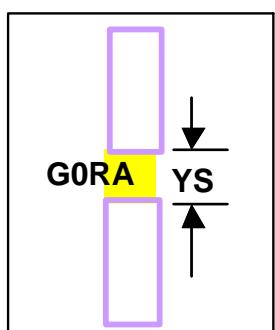


Any vertex of CPO inside
ALL_PO is not allowed

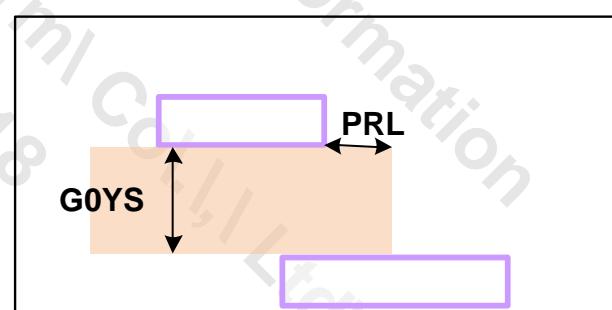
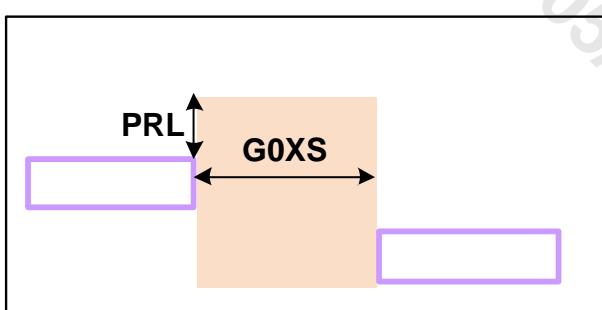
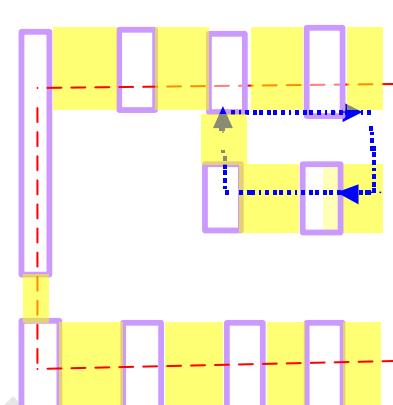
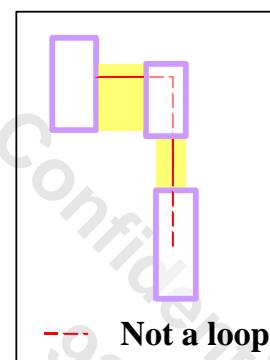
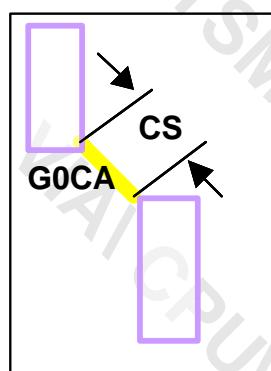
CPO.R.6



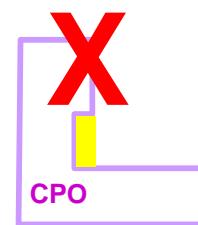
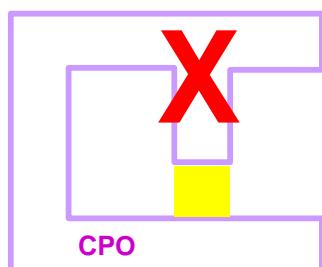




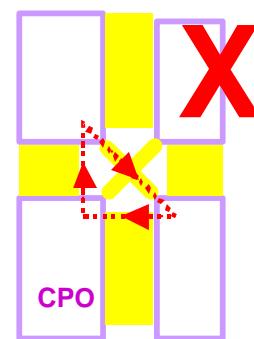
G0-AREA



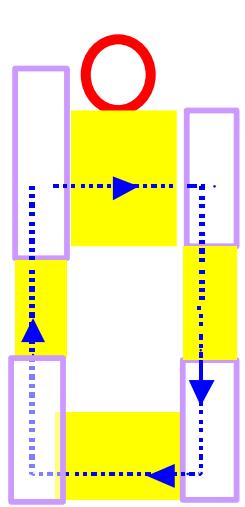
CPO.G0.0



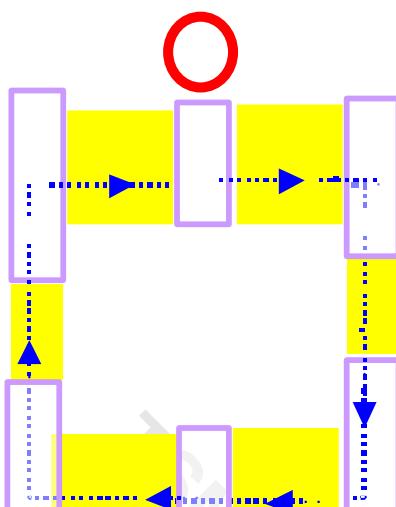
CPO.G0.1



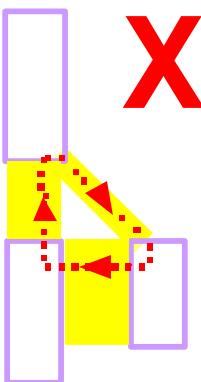
CPO.G0.2



Count = 4, even



Count = 6, even



Count = 3, odd

CPO.G0.2

4.5.22 Trim PO (TPO) Layout Rules

TPO_2 (CAD layer 17;17 for poly pitch = 0.057 µm) is used to trim poly.

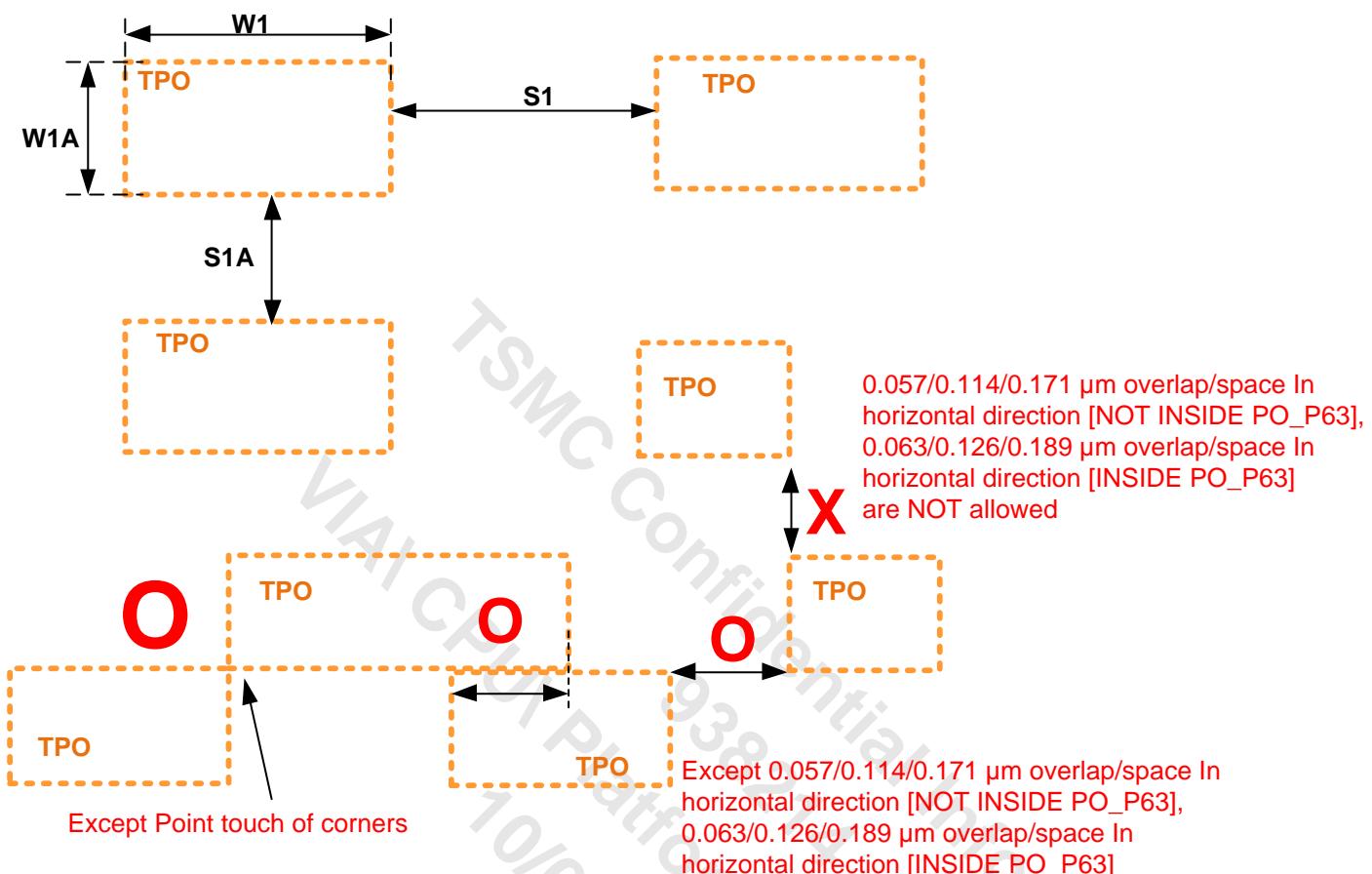
TPO = TPO_2

Rule No.	Description	Label	Op.	Rule
TPO.W.1	Width (Except following conditions: 1. Point touch of corners, 2. Concave corner to concave corner width = 0.057/0.063/0.114/0.126/ 0.171/0.189 µm in horizontal direction [PRL = 0 µm], 3. {FB_9 SIZING 0.120 µm in vertical direction})	W1	≥	0.2280
TPO.W.1.1	Width in vertical direction (Except BLK_WF)	W1A	≥	0.2400
TPO.W.1.2	Width [INSIDE PO_P76]	W1	≥	0.2280
TPO.W.2	Width of ALL_PO [both side centerline space = 0.057 µm, and INTERACT vertical edge of TPO_2]	W2	=	0.0110
TPO.W.2.1	Width of ALL_PO [both side centerline space = 0.063 µm, and INTERACT vertical edge of TPO_2, INSIDE PO_P63]	W2	=	0.0110
TPO.W.2.2	Width of ALL_PO [both side centerline space = 0.076 µm, and INTERACT vertical edge of TPO_2, INSIDE PO_P76]	W2	=	0.0110
TPO.S.1	Space (Except FB_9, or following conditions: 1. Point touch of corners, 2. Corner to corner space = 0.057/0.063/0.114/0.126/0.171/0.189 µm in horizontal direction [PRL = 0 µm])	S1	≥	0.2280
TPO.S.1.1	Space in vertical direction	S1A	≥	0.2400
TPO.S.1.2	Space [INSIDE PO_P76]	S1	≥	0.2280
TPO.S.2	Space to ALL_OD	S2	≥	0.0230
TPO.S.2.0.1	Space to ALL_OD [INSIDE PO_P63]	S2	≥	0.0260
TPO.S.2.0.2	Space to ALL_OD [INSIDE PO_P76]	S2	≥	0.0325
TPO.S.2.1	Space to ALL_OD in vertical direction (Except FB_9, BLK_WF)	S2A	≥	0.0410
TPO.S.3	Space to {{ALL_PO NOT CPO} OR BPO_V} in horizontal direction	S3	≥	0.0230
TPO.S.3.1	Space to {{ALL_PO NOT CPO} OR BPO_V} in horizontal direction [INSIDE PO_P63]	S3	≥	0.0260
TPO.S.3.2	Space to {ALL_PO NOT CPO} in horizontal direction [INSIDE PO_P76]	S3	≥	0.0325
TPO.S.4	Space to SRM (50;0) (Space = 0 µm is allowed)	S4	≥	0.2100
TPO.EN.1	Enclosure of ALL_OD	EN1	≥	0.0230
TPO.EN.1.0.1	Enclosure of ALL_OD [INSIDE PO_P63]	EN1	≥	0.0260
TPO.EN.1.0.2	Enclosure of ALL_OD [INSIDE PO_P76]	EN1	≥	0.0325
TPO.EN.1.1	Enclosure of ALL_OD in vertical direction (Except FB_9, BLK_WF)	EN1A	≥	0.0410
TPO.EN.1.3	Maximum enclosure of {ALL_PO OR BPO_V} by TPO	EN1C	≤	0.1160
TPO.EN.2	Enclosure of {{ALL_PO NOT CPO} OR BPO_V} in horizontal direction	EN2	≥	0.0230
TPO.EN.2.1	Enclosure of {{ALL_PO NOT CPO} OR BPO_V} in horizontal direction [INSIDE PO_P63]	EN2	≥	0.0260
TPO.EN.2.2	Enclosure of {ALL_PO NOT CPO} in horizontal direction [INSIDE PO_P76]	EN2	≥	0.0325
TPO.A.1	Area (Except FB_9)	A1	≥	0.05472
TPO.A.2	Enclosed area (include surrounding by point-touch polygons) (Except FB_9)	A2	≥	0.05472
TPO.R.1	TPO must fully cover {ALL_PO [width = 0.008 µm] OR BPO_V}			

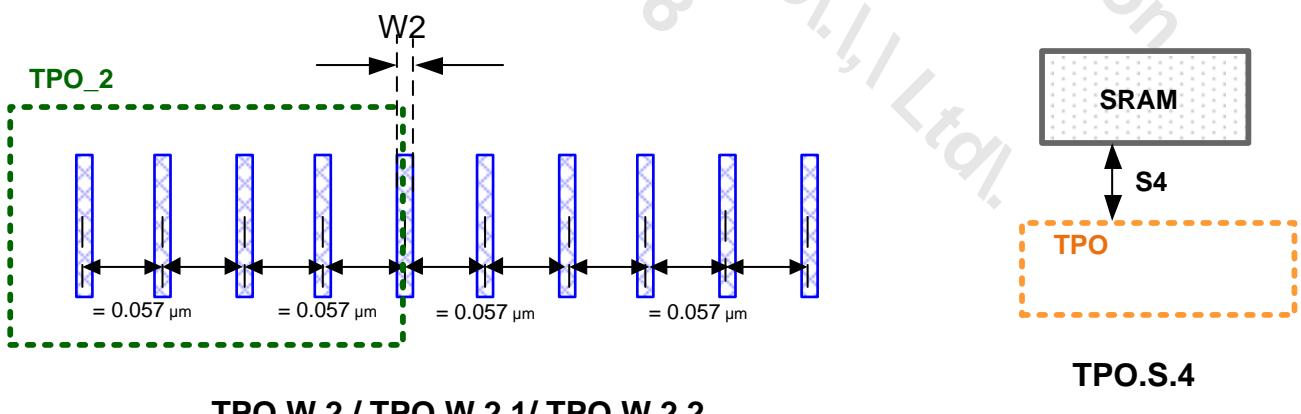
Rule No.	Description	Label	Op.	Rule
TPO.R.2	TPO overlap ALL_PO [width \geq 0.011 μm] is not allowed (Except BLK_WF, or following conditions: 1. ALL_PO [width = 0.011 μm , both sides centerline space = 0.057/0.063/0.076 μm , and TPO_2 edge on centerline of ALL_PO])			
TPO.R.5	PODE_GATE [NOT INTERACT CPODE [width = 0.011 μm], ABUT OD vertical edge between 90-90 degree convex corner] cut TPO vertical edge is not allowed			
TPO.R.6.1	$\{\{\text{TrGATE OR \{OD NOT PO\}} \text{ NOT CPODE}\} \text{ CUT TPO_2}\}$ is not allowed			
TPO.R.6.2	TPO_2 overlap SRM is not allowed			
TPO.R.7	TPO_2 must be orthogonal to grid			

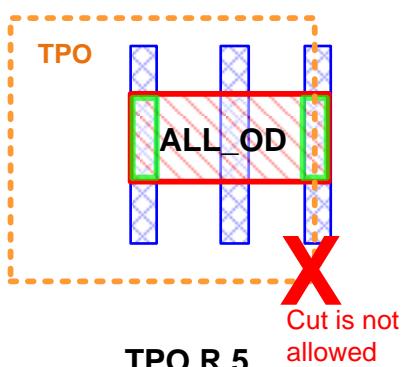
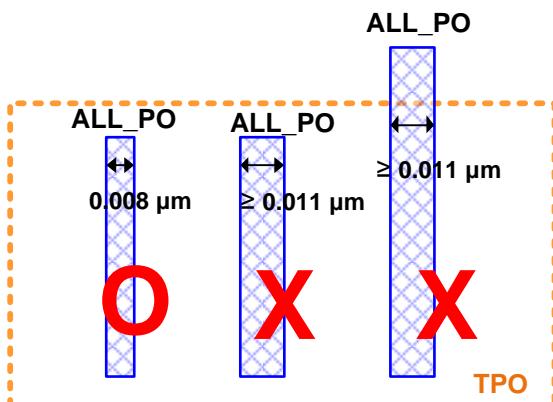
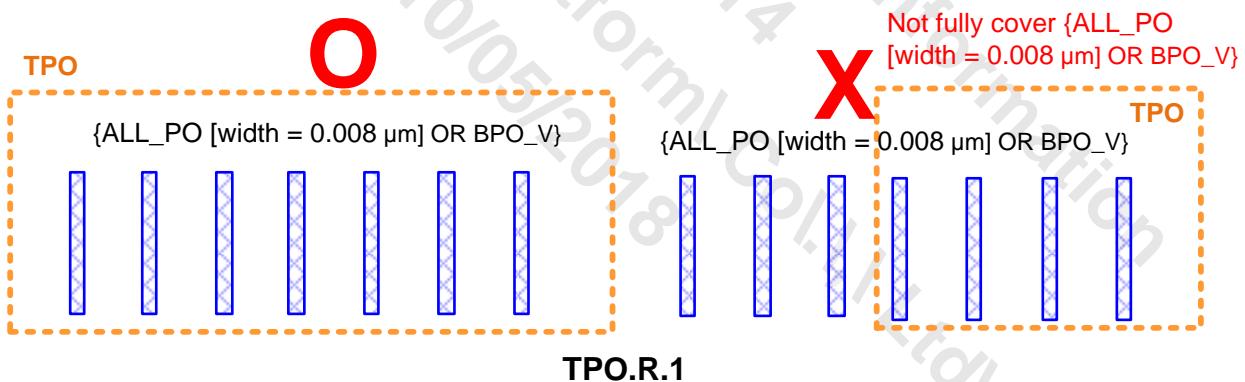
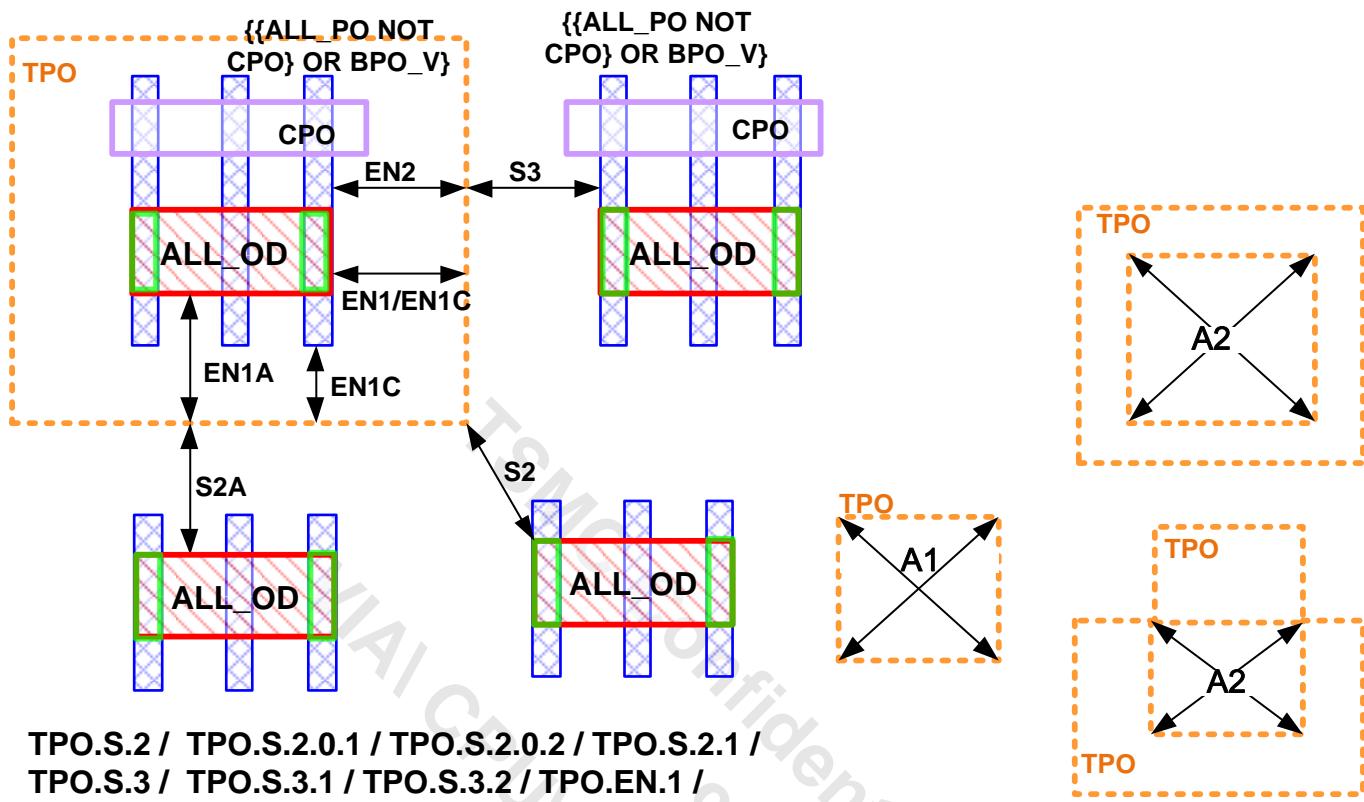
TSMC Confidential Information
VIAI CPU Platform Col., I Ltd.
938214
10/05/2018

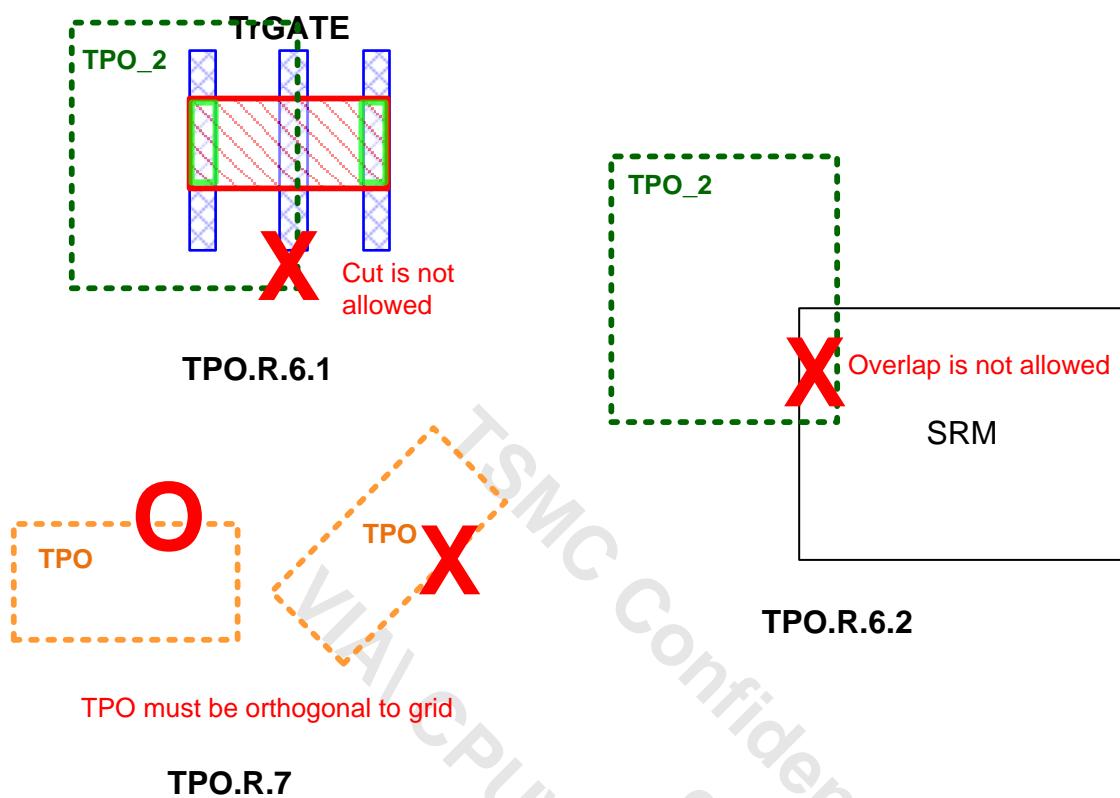
TPO



TPO.W.1 / TPO.W.1.1 / TPO.W.1.2 / TPO.S.1 / TPO.S.1.1 / TPO.S.1.2







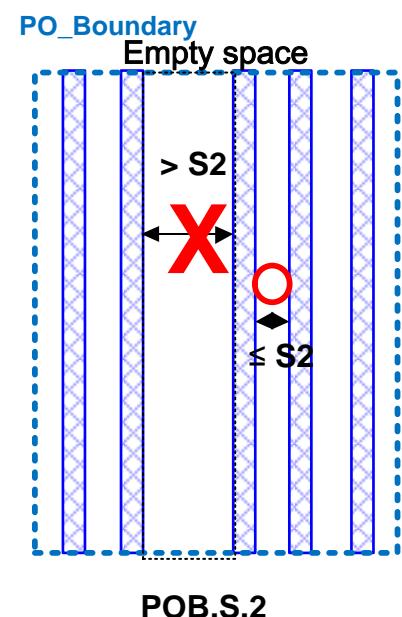
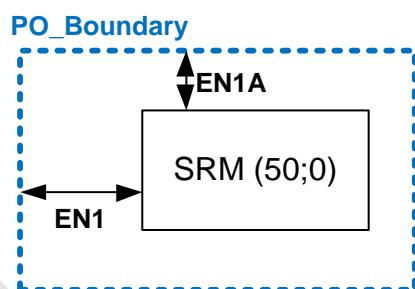
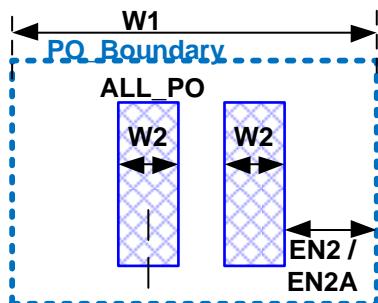
4.5.23 PO_Boundary (POB) Layout Rules

PO_Boundary (CAD layer 108;17) is used for poly pitch = 0.057 μm on grid.

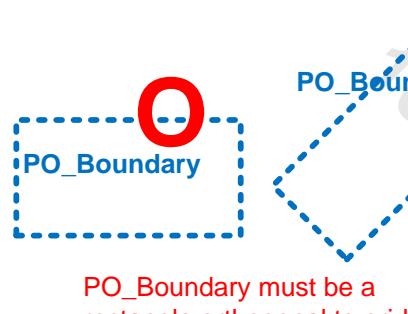
$n \geq 0$ and n is integer.

Rule No.	Description	Label	Op.	Rule
POB.W.1	Width of PO_Boundary in horizontal direction	W1	=	$0.5700+0.1140*n$
POB.W.2	Width of ALL_PO [INTERACT PO_Boundary]	W2	\leq	0.0110
POB.S.2	Empty space of ALL_PO [INSIDE PO_Boundary] DRC flags {{PO_Boundary NOT ALL_PO} SIZING down/up 0.0245 μm}	S2	\leq	0.0490
POB.EN.1	Enclosure of SRM in horizontal direction	EN1	=	$0.0570+0.1140*n$
POB.EN.1.1	Enclosure of SRM in vertical direction	EN1A	\geq	0.0610
POB.EN.2	Enclosure of ALL_PO [width = 0.008 μm, INSIDE PO_Boundary] in horizontal direction	EN2	=	0.0245
POB.EN.2.1	Enclosure of ALL_PO [width = 0.011 μm, INSIDE PO_Boundary] in horizontal direction	EN2A	=	0.0230
POB.R.1	PO_Boundary must be orthogonal to grid			
POB.R.2	{{SRM OR BPO (17;50)} OR BPO_2} must be inside PO_Boundary			
POB.R.3	OD, ALL_PO cut PO_Boundary is not allowed			
POB.R.4	ALL_PO [INSIDE PO_Boundary] line-end must abut PO_Boundary			

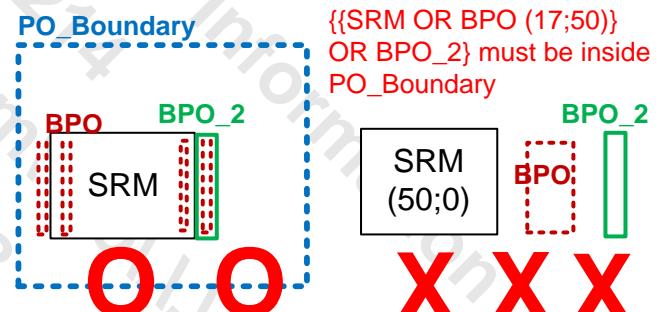
POB



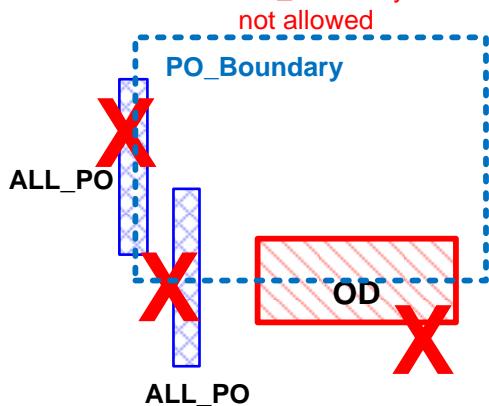
**POB.W.1 / POB.W.2 / POB.EN.1 /
POB.EN.1.1 / POB.EN.2 / POB.EN.2.1**



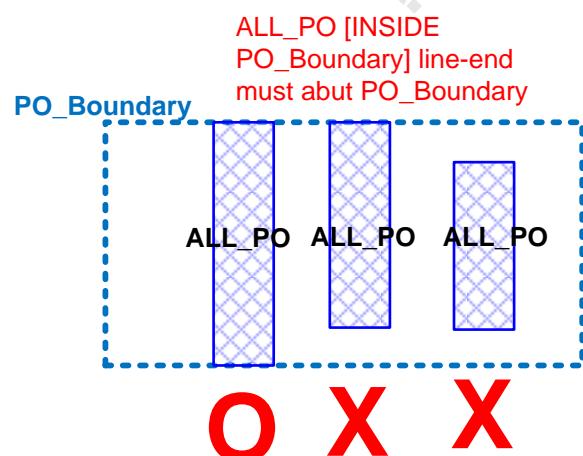
POB.R.1



POB.R.2



POB.R.3

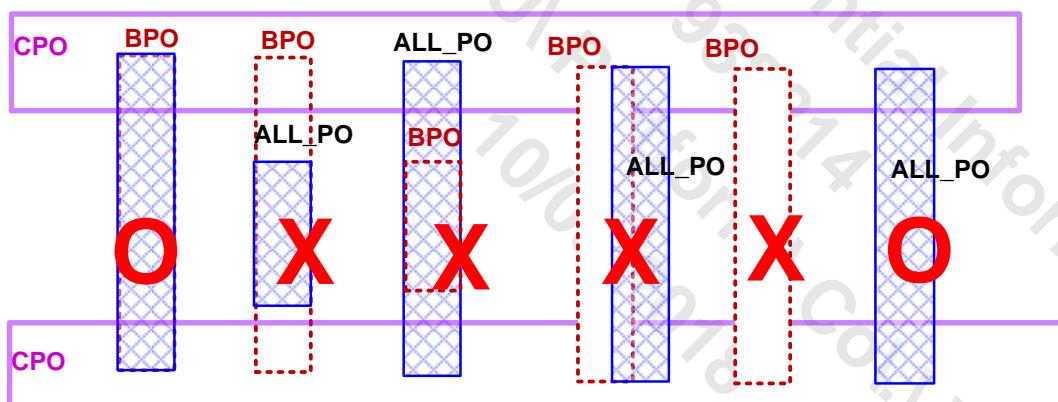
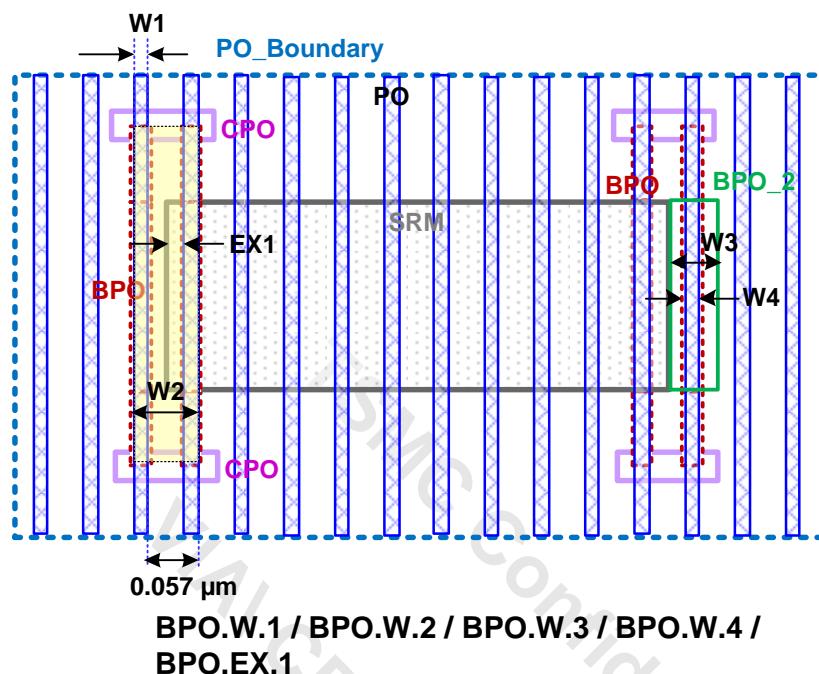


POB.R.4

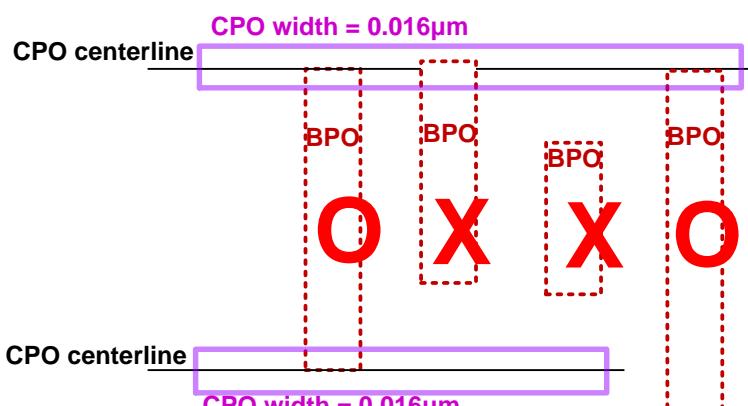
4.5.24 Butted PO (BPO) Layout Rules

Butted PO (CAD layer 17;50) is used for SRAM bit cell abut periphery cell.

Rule No.	Description	Label	Op.	Rule
BPO.W.1	Width of BPO (17;50) in horizontal direction	W1	\leq	0.0110
BPO.W.2	Width of {BPO (17;50) SIZING up/down 0.0245 μm in horizontal direction} in horizontal direction (Except BLK_WF , or following conditions: 1. BPO_SRAM) Definition of BPO_SRAM: {BPO SIZING up/down 0.137 μm in horizontal direction} [INTERACT {SRM SIZING -0.057 μm horizontal direction}]	W2	=	0.0650~0.0680
BPO.W.3	Width of BPO_2 in horizontal direction	W3	=	0.0570
BPO.W.4	Width of {ALL_PO AND BPO_2} in horizontal direction	W4	=	0.0110
BPO.EX.1	SRM extension on BPO (17;50) in horizontal direction	EX1	=	0.0230, 0.0245
BPO.R.1	{BPO (17;50) NOT CPO} must be drawn identically to {ALL_PO NOT CPO}			
BPO.R.2	BPO (17;50) line-end must abut CPO [width = 0.016 μm] centerline or abut CPO [width = 0.100 μm] horizontal edge from outside (Except BLK_WF)			
BPO.R.3	BPO (17;50) overlap ALL_OD, ALL_MP is not allowed			
BPO.R.5	{ALL_PO NOT CPO} [INTERACT {{SRM SIZING 0.057 μm in horizontal direction} NOT {SRM SIZING -0.057 μm horizontal direction}}] must interact BPO (17;50)			
BPO.R.5.1	{ALL_PO NOT CPO} [NOT INTERACT {SRM SIZING 0.057 μm in horizontal direction}] interact BPO (17;50) is not allowed			
BPO.R.6	BPO_2 must interact BPO			
BPO.R.6.1	BPO_2 must be centered at centerline of BPO in horizontal direction			
BPO.R.7	One of BPO_2 vertical edge must abut and coincident to SRM vertical edge from outside, the other one BPO_2 vertical edge must abut PO_Boundary vertical edge.			
BPO.R.8	BPO_2 overlap SRM is not allowed			
BPO.R.9	BPO_2 must be a rectangle orthogonal to grid			

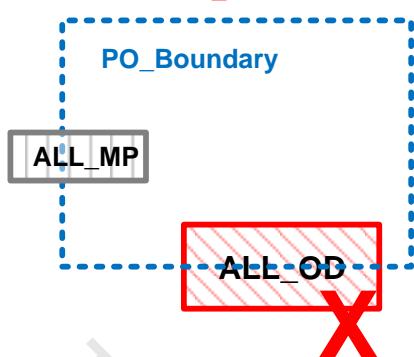
BPO

{BPO (17;50) NOT CPO} must be drawn identically to {ALL_PO NOT CPO}

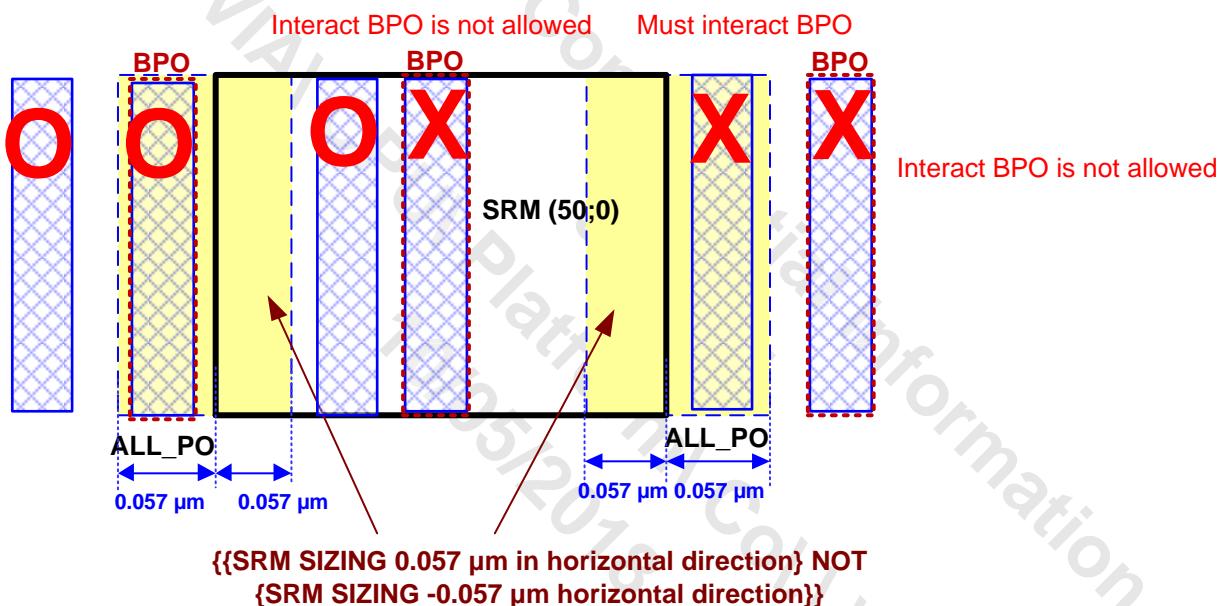
BPO.R.1**BPO.R.2**

CPO width = 0.100 μm

BPO (17;50) overlap ALL_OD,
ALL_MP is not allowed

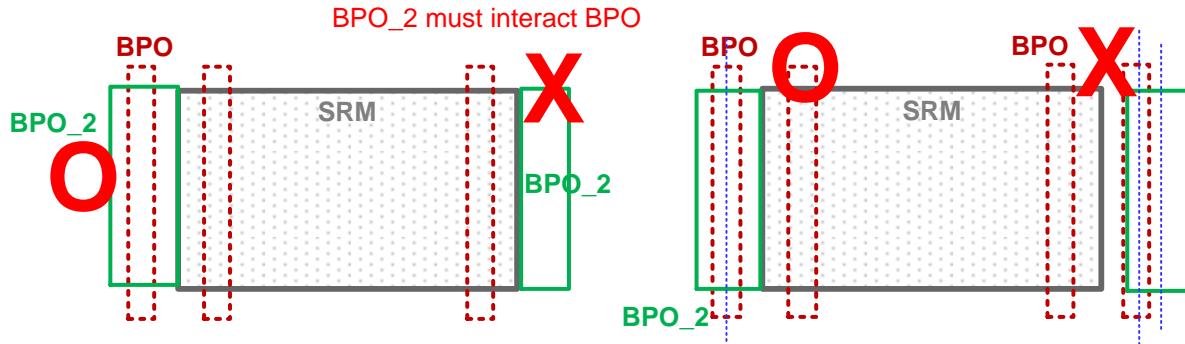


BPO.R.3



BPO.R.5 / BPO.R.5.1

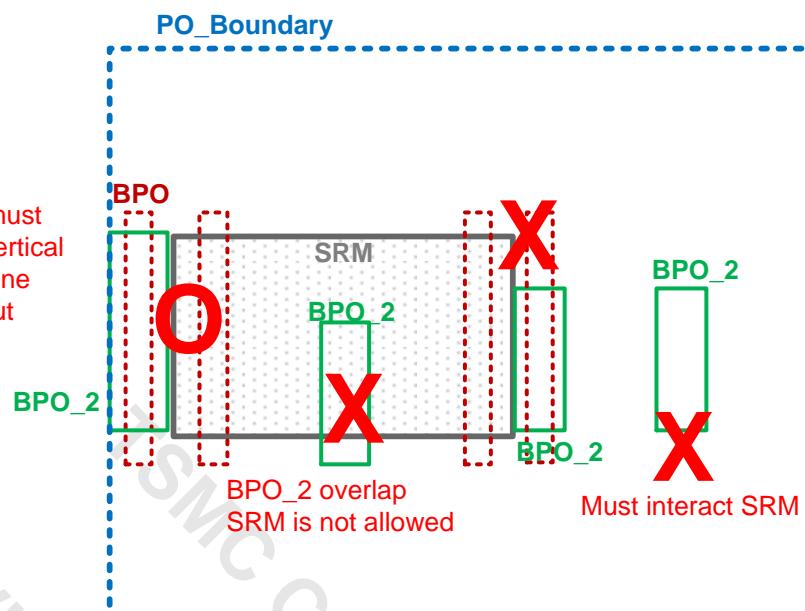
BPO_2 must be centered at centerline
of BPO in horizontal direction



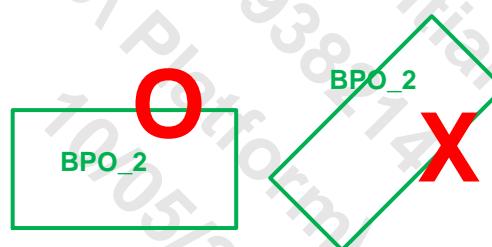
BPO.R.6

BPO.R.6.1

One of BPO_2 vertical edge must abut and coincident to SRM vertical edge from outside, the other one BPO_2 vertical edge must abut PO_Boundary vertical edge.



BPO.R.7 / BPO.R.8



BPO.R.9

4.5.25 VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]

VT = VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P 6 single layers

ALL_VT = {ALL_VT_N OR ALL_VT_P}

ALL_VT_N = {{VTS_N OR VTL_N} OR VTUL_N}

ALL_VT_P = {{VTS_P OR VTL_P} OR VTUL_P}

Rule No.	Description	Label	Op.	Rule
VT.W.1	Width of VT (Except BLK_WF, or following conditions: 1. Point touch of corners, 2. Concave corner to concave corner width = 0.057/0.063/0.100/ 0.114 µm in horizontal direction [PRL = 0 µm])	W1	≥	0.1200
VT.W.1.1	Width of VT [INSIDE PO_P76]	W1	≥	0.1200
VT.W.1.2	Width of {{VTL_N OR VTUL_N} OR VTS_P}, {VTL_P OR VTS_N} (Except BLK_WF, or following conditions: 1. Point touch of corners, 2. Concave corner to concave corner width = 0.057/0.063/0.100/0.114 µm in horizontal direction [PRL = 0 µm])	W1B	≥	0.1200
VT.W.1.2.1	Width of {{VTL_N OR VTUL_N} OR VTS_P}, {VTL_P OR VTS_N} [INSIDE PO_P76]	W1B	≥	0.1200
VT.W.2	Width of VT in horizontal direction (Except FB_9, or following conditions: 1. Point touch of corners, 2. Concave corner to concave corner width = 0.057/0.063/0.100/ 0.114/0.126/0.171/0.189/0.200 µm in horizontal direction [PRL = 0 µm]) DRC flags width between vertical edges [PRL ≥ 0 µm]	W2	≥	0.2280
VT.W.2.1	Width of VT in horizontal direction [INSIDE PO_P76]	W2	≥	0.2280
VT.W.2.2	Width of {{VTL_N OR VTUL_N} OR VTS_P}, {VTL_P OR VTS_N} in horizontal direction (Except FB_9, or following conditions: 1. Point touch of corners, 2. Concave corner to concave corner width = 0.057/0.063/0.100/ 0.114/0.126/0.171/0.189/0.200 µm in horizontal direction [PRL = 0 µm]) DRC flags width between vertical edges [PRL ≥ 0 µm]	W2B	≥	0.2280
VT.W.2.2.1	Width of {{VTL_N OR VTUL_N} OR VTS_P}, {VTL_P OR VTS_N} in horizontal direction [INSIDE PO_P76]	W2B	≥	0.2280
VT.S.1	Space of VT (Except BLK_WF, or following conditions: 1. Point touch of corners, 2. Corner to corner space = 0.057/0.063/0.100/ 0.114 µm in horizontal direction [PRL = 0 µm])	S1	≥	0.1200
VT.S.1.1	Space of VT [INSIDE PO_P76]	S1	≥	0.1200
VT.S.1.2	Space of {{VTL_N OR VTUL_N} OR VTS_P} (Except BLK_WF, or following conditions: 1. Point touch of corners, 2. Corner to corner space = 0.057/0.063/0.100/ 0.114 µm in horizontal direction [PRL = 0 µm])	S1B	≥	0.1200
VT.S.1.2.1	Space of {{VTL_N OR VTUL_N} OR VTS_P} [INSIDE PO_P76]	S1B	≥	0.1200

Rule No.	Description	Label	Op.	Rule
VT.S.1.4	Space of {VTL_P OR VTS_N} (Except BLK_WF, or following conditions: 1. Point touch of corners, 2. Corner to corner space = 0.057/0.063/0.100/ 0.114 µm in horizontal direction [PRL = 0 µm])	S1D	≥	0.1200
VT.S.1.4.1	Space of {VTL_P OR VTS_N} [INSIDE PO_P76]	S1D	≥	0.1200
VT.S.2	Space of VT in horizontal direction [PRL ≥ 0 µm] (Except FB_9, or following conditions: 1. Point touch of corners, 2. Corner to corner space = 0.057/0.063/0.100/ 0.114/0.126/0.171/ 0.189/0.200 µm in horizontal direction [PRL = 0 µm])	S2	≥	0.2280
VT.S.2.1	Space of VT in horizontal direction [PRL ≥ 0 µm, INSIDE PO_P76]	S2	≥	0.2280
VT.S.2.2	Space of {{VTL_N OR VTUL_N} OR VTS_P} in horizontal direction [PRL ≥ 0 µm] (Except FB_9, or following conditions: 1. Point touch of corners, 2. Corner to corner space = 0.057/0.063/0.100/ 0.114/0.126/0.171/ 0.189/0.200 µm in horizontal direction [PRL = 0 µm])	S2B	≥	0.2280
VT.S.2.2.1	Space of {{VTL_N OR VTUL_N} OR VTS_P} in horizontal direction [PRL ≥ 0 µm, INSIDE PO_P76]	S2B	≥	0.2280
VT.S.2.4	Space of {VTL_P OR VTS_N} in horizontal direction [PRL ≥ 0 µm] (Except FB_9, or following conditions: 1. Point touch of corners, 2. Corner to corner space = 0.057/0.063/0.100/ 0.114/0.126/0.171/ 0.189/0.200 µm in horizontal direction [PRL = 0 µm])	S2D	≥	0.2280
VT.S.2.4.1	Space of {VTL_P OR VTS_N} in horizontal direction [PRL ≥ 0 µm, INSIDE PO_P76]	S2D	≥	0.2280
VT.S.4	Space of VT to ALL_OD (Except Dummy_Cell)	S4	≥	0.0230
VT.S.4.0.1	Space of VT to ALL_OD [INSIDE PO_P63] (Except Dummy_Cell)	S4	≥	0.0260
VT.S.4.0.2	Space of VT to ALL_OD [INSIDE PO_P76] (Except Dummy_Cell)	S4	≥	0.0325
VT.S.4.1	Space of VT to ALL_OD in vertical direction (Except FB_9, Dummy_Cell, BLK_WF)	S4A	≥	0.0410
VT.S.5	Space of VT to ALL_PO (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog ≤ 0.002 µm)	S5	≥	0.0230
VT.S.5.0.1	Space of VT to {ALL_PO NOT CPO} in horizontal direction [INSIDE PO_P63] (Except Dummy_Cell)	S5	≥	0.0260
VT.S.5.0.2	Space of VT to {ALL_PO NOT CPO} in horizontal direction [INSIDE PO_P76] (Except Dummy_Cell)	S5	≥	0.0325
VT.S.5.0	Space of VT to {ALL_PO NOT CPO} in horizontal direction (Except Dummy_Cell)	S5	≥	0.0230
VT.S.5.1	Space of VT to {ALL_PO NOT CPO} [ALL_PO width = 0.008/0.011 µm, centerline space = 0.057 µm] in horizontal direction (Except Dummy_Cell)	S5A	≥	0.0245/0.0230
VT.S.5.1.1	Space of VT to {ALL_PO NOT CPO} [ALL_PO width = 0.008/0.011 µm, INSIDE PO_P63] in horizontal direction (Except Dummy_Cell)	S5A	≥	0.0275/0.0260
VT.S.5.1.2	Space of VT to {ALL_PO NOT CPO} [ALL_PO width = 0.008/0.011 µm, INSIDE PO_P76] in horizontal direction (Except Dummy_Cell)	S5A	≥	0.0340/0.0325
VT.S.5.2	Space of VT to {ALL_PO NOT CPO} [ALL_PO width = 0.020/0.036 µm] in horizontal direction (Except Dummy_Cell)	S5B	≥	0.0400

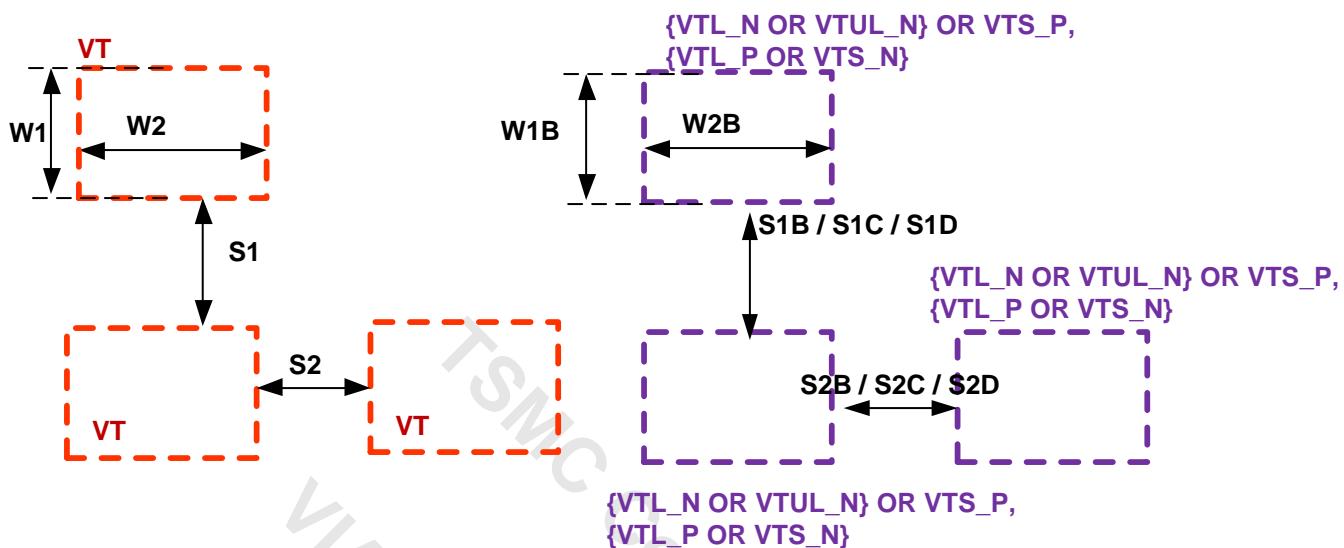
Rule No.	Description	Label	Op.	Rule
VT.S.5.3	Space of VT to {ALL_PO NOT CPO} [ALL_PO width \geq 0.072 μm] in horizontal direction (Except Dummy_Cell)	S5C	\geq	0.0470
VT.S.6.1	Space of VT to TrGATE [Lg = 0.008/0.011 μm , centerline space = 0.057 μm] in horizontal direction ({TrGATE CUT VT} is not allowed)	S6A	\geq	0.0530/0.0515
VT.S.6.2	Space of VT to TrGATE [Lg = 0.008/0.011 μm , INSIDE PO_P63] in horizontal direction	S6B	\geq	0.0590/0.0575
VT.S.6.3	Space of VT to TrGATE [Lg = 0.008/0.011 μm , INSIDE PO_P76] in horizontal direction	S6B	\geq	0.0720/0.0705
VT.S.7	Space of VT to SRM (50;0) (Space = 0 μm is allowed)	S7	\geq	0.2100
VT.S.9.1	Space of VT to ALL_PO [INSIDE PO_P63] (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	S9	\geq	0.0260
VT.S.9.2	Space of VT to ALL_PO [INSIDE PO_P76] (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	S9	\geq	0.0325
VT.S.11	Space of VT [PRL > 0.480 μm [excluding projection of ALL_OD on VT within 0.170 μm at both sides]]	S11	\geq	0.2400
VT.S.11.1	Space of {{VTL_N OR VTUL_N} OR VTS_P} [PRL > 0.480 μm [excluding projection of ALL_OD on {{VTL_N OR VTUL_N} OR VTS_P} within 0.170 μm at both sides]]	S11	\geq	0.2400
VT.S.11.3	Space of {VTL_P OR VTS_N} [PRL > 0.480 μm [excluding projection of ALL_OD on {VTL_P OR VTS_N} within 0.170 μm at both sides]]	S11	\geq	0.2400
VT.EN.1	TrGATE [Lg = 0.008/0.011 μm , centerline space = 0.057 μm] enclosure by VT in horizontal direction	EN1	\geq	0.0530/0.0515
VT.EN.1.2	TrGATE [Lg = 0.008/0.011 μm , INSIDE PO_P63] enclosure by VT in horizontal direction	EN1B	\geq	0.0590/0.0575
VT.EN.1.3	TrGATE [Lg = 0.008/0.011 μm , INSIDE PO_P76] enclosure by VT in horizontal direction	EN1C	\geq	0.0720/0.0705
VT.EN.2	ALL_OD enclosure by VT (Except Dummy_Cell)	EN2	\geq	0.0230
VT.EN.2.1	ALL_OD enclosure by VT [INSIDE PO_P63] (Except Dummy_Cell)	EN2A	\geq	0.0260
VT.EN.2.2	ALL_OD enclosure by VT [INSIDE PO_P76] (Except Dummy_Cell)	EN2B	\geq	0.0325
VT.EN.3	ALL_PO enclosure by VT in horizontal direction (Except Dummy_Cell)	EN3	\geq	0.0230
VT.EN.3.1	ALL_PO enclosure by VT in horizontal direction [INSIDE PO_P63] (Except Dummy_Cell)	EN3A	\geq	0.0260
VT.EN.3.2	ALL_PO enclosure by VT in horizontal direction [INSIDE PO_P76] (Except Dummy_Cell)	EN3B	\geq	0.0325
VT.EX.1	{ALL_PO NOT CPO} extension on VT in vertical direction (Except FB_9, FB_8, Dummy_Cell, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	EX1	\geq	0.0430
VT.EX.2	VT extension on {ALL_PO NOT CPO} in horizontal direction (Except Dummy_Cell)	EX2	\geq	0.0230
VT.EX.2.0.1	VT extension on {ALL_PO NOT CPO} in horizontal direction [INSIDE PO_P63] (Except Dummy_Cell)	EX2	\geq	0.0260
VT.EX.2.0.2	VT extension on {ALL_PO NOT CPO} in horizontal direction [INSIDE PO_P76] (Except Dummy_Cell)	EX2	\geq	0.0325
VT.EX.2.1	VT extension on {ALL_PO NOT CPO} [ALL_PO width = 0.008/0.011 μm , centerline space = 0.057 μm] in horizontal direction (Except Dummy_Cell)	EX2A	\geq	0.0245/0.0230

Rule No.	Description	Label	Op.	Rule
VT.EX.2.1.1	VT extension on {ALL_PO NOT CPO} [ALL_PO width = 0.008/0.011 μm, INSIDE PO_P63] in horizontal direction (Except Dummy_Cell)	EX2A	≥	0.0275/0.0260
VT.EX.2.1.2	VT extension on {ALL_PO NOT CPO} [ALL_PO width = 0.008/0.011 μm, INSIDE PO_P76] in horizontal direction (Except Dummy_Cell)	EX2A	≥	0.0340/0.0325
VT.EX.2.2	VT extension on {ALL_PO NOT CPO} [ALL_PO width = 0.020/0.036 μm] in horizontal direction (Except Dummy_Cell)	EX2B	≥	0.0400
VT.EX.2.3	VT extension on {ALL_PO NOT CPO} [ALL_PO width ≥ 0.072 μm] in horizontal direction (Except Dummy_Cell)	EX2C	≥	0.0470
VT.EX.3	CPO [width = 0.016/0.100 μm] extension on VT in vertical direction (Except following conditions: 1. CPO [width = 0.016 μm] abut VT horizontal edge [INSIDE FB_9])	EX3	≥	0.0080
VT.EX.3.1	CPO [width = 0.040/0.068 μm] extension on VT in vertical direction (Except Dummy_Cell)	EX3A	≥	0.0200
VT.EX.4.1	Extension on ALL_OD in vertical direction (Except FB_9, Dummy_Cell, BLK_WF)	EX4A	≥	0.0410
VT.O.1	VT overlap of {ALL_PO NOT CPO} in vertical direction (Except FB_9, FB_8, Dummy_Cell, or following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	O1	≥	0.0430
VT.O.2	VT overlap of CPO [width = 0.016/0.100 μm] in vertical direction (Except Dummy_Cell, or following conditions: 1. CPO [width = 0.016 μm] abut VT horizontal edge [INSIDE FB_9])	O2	≥	0.0080
VT.O.2.1	VT overlap of CPO [width = 0.040/0.068 μm] in vertical direction	O2A	≥	0.0200
VT.A.1	Area of VT (Except FB_9)	A1	≥	0.02736
VT.A.2	Enclosed area of VT (include surrounding by point-touch polygons) (Except FB_9, FB_8)	A2	≥	0.04000
VT.A.2.2	Enclosed area of {{VTL_N OR VTUL_N} OR VTS_P} (include surrounding by point-touch polygons) (Except FB_9, FB_8)	A2B	≥	0.04000
VT.A.2.4	Enclosed area of {VTL_P OR VTS_N} (include surrounding by point-touch polygons) (Except FB_9, FB_8)	A2D	≥	0.04000
VT.A.3	Area of {{ALL_PO NOT CPO} AND VT} (Except FB_9, FB_8, Dummy_Cell)	A3	≥	0.00034
VT.R.0	DRC check VT = VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P 6 single layers in this section			
VT.R.1	VT overlap each other is not allowed			
VT.R.1.1	ALL_VT overlap OD2 is not allowed (Except Dummy_Cell)			
VT.R.1.2	ALL_VT_N overlap P+ ACTIVE is not allowed			
VT.R.1.3	ALL_VT_P overlap N+ ACTIVE is not allowed			
VT.R.4	{PODE_GATE NOT CPODE} [ABUT OD vertical edge between 90-90 degree convex corner] cut vertical edge of VT is not allowed			
VT.R.5	{{ALL_OD NOT {CPODE OR SR_DPO_WAVE}} CUT VT} is not allowed (Except Dummy_Cell) Definition of SR_DPO_WAIVE: SR_DPO INTERACT SR_DOD [INTERACT CPODE]			
VT.R.6	ACTIVE must be covered by ALL_VT (Except RH_TNB, OD2, NWRSTI, VAR, IBJTDNY, DIODMY, BLK_WF)			

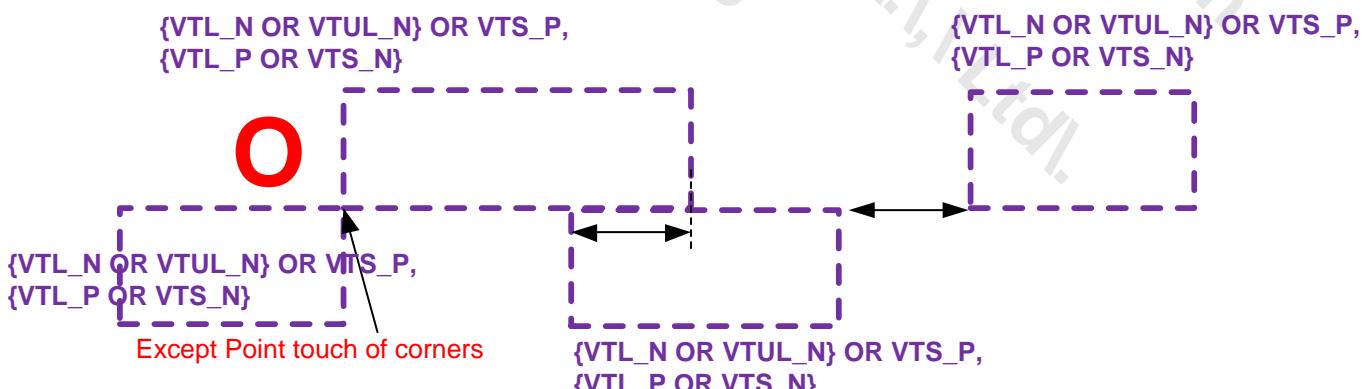
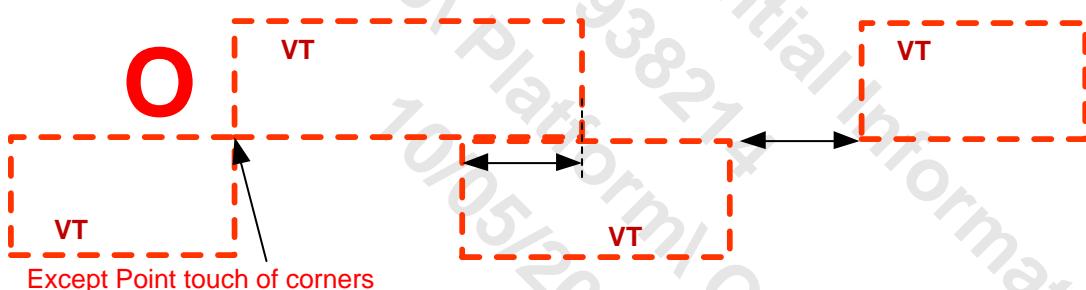
Rule No.	Description	Label	Op.	Rule
VT.R.6.1	ALL_PO must be covered by ALL_VT (Except RH_TNB, OD2, SEALRING_ALL, VAR, IBJTDMY, DIODMY, BLK_WF, Dummy_Cell, or following conditions: 1. ALL_PO [INTERACT NWDMY], 2. {ALL_PO AND BPO_2})			
VT.R.7	VT overlap SEALRING_ALL, TCDDMY, ICOVL_SINGLE is not allowed			
VT.R.8	VT must be orthogonal to grid			
VT.R.9	{PO NOT CPO} NOT CPODE cut vertical edge of VT is not allowed			
VT.R.9.1	More than one VT horizontal edge inside {{PO NOT CPO} INTERACT PODE_GATE} NOT OD} [INTERACT PODE_GATE, with VT vertical edge inside] is not allowed			
VT.R.10	Vertical edge of ALL_VT_N abut ALL_VT_P inside PO is not allowed			
VT.R.11	{SR_DOD [NOT INTERACT CPODE] or OD [INTERACT PO width ≥ 0.020 μm]} NOT INSIDE Dummy_Cell) cut VT is not allowed			

VIAI CPU Confidential Information
938214
10/05/2018

VT



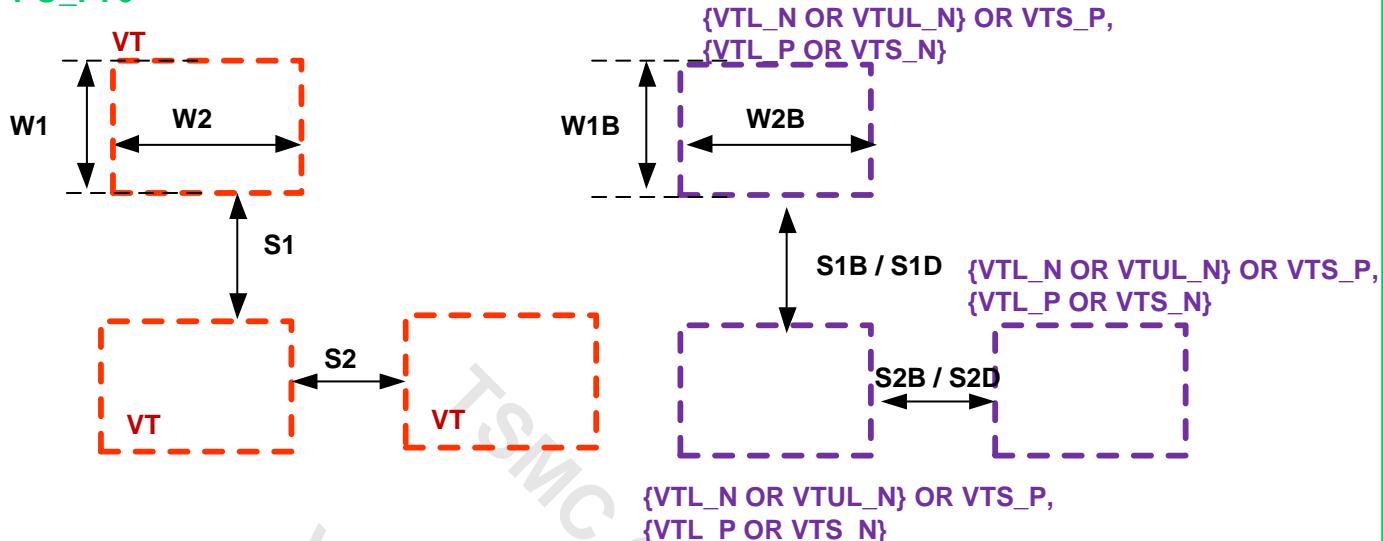
Except 0.057/0.100/0.114 μm overlap/space [NOT
INSIDE PO_P63] in horizontal direction
Except 0.063/0.126/0.189 μm overlap/space
[INSIDE PO_P63] in horizontal direction



Except 0.057/0.100/0.114 μm overlap/space [NOT
INSIDE PO_P63] in horizontal direction
Except 0.063/0.126/0.189 μm overlap/space
[INSIDE PO_P63] in horizontal direction

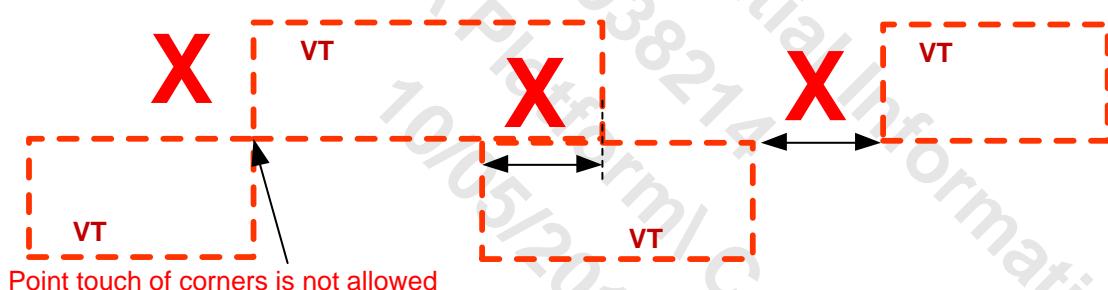
**VT.W.1 / VT.W.1.2 / VT.W.2 / VT.W.2.2 / VT.S.1 / VT.S.1.2 /
VT.S.1.4 / VT.S.2 / VT.S.2.2 / VT.S.2.4**

PO_P76



PO_P76

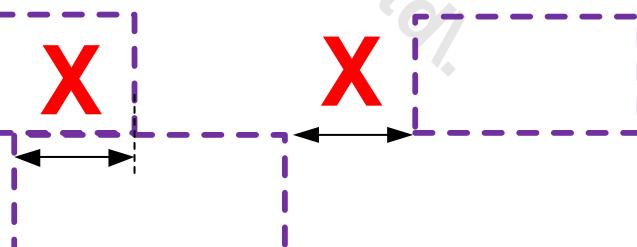
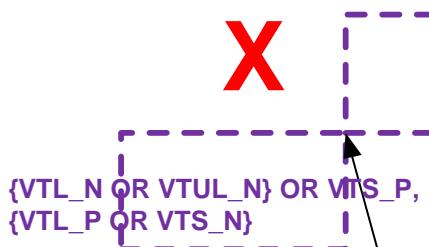
overlap/space < 0.228 μm [INSIDE PO_P76] in horizontal direction is not allowed



PO_P76

{VTL_N OR VTUL_N} OR VTS_P,
{VTL_P OR VTS_N}

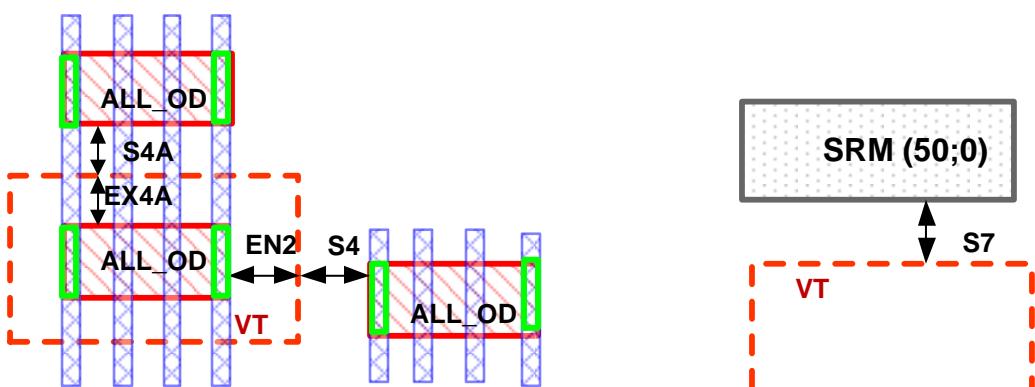
{VTL_N OR VTUL_N} OR VTS_P,
{VTL_P OR VTS_N}



Point touch of corners is not allowed

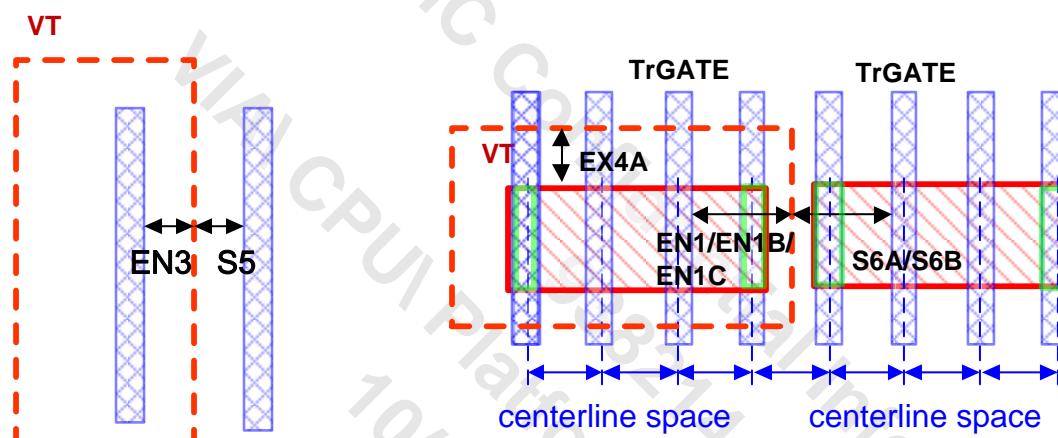
overlap/space < 0.228 μm [INSIDE PO_P76] in horizontal direction is not allowed

VT.W.1.1 / VT.W.1.2.1 / VT.W.2.1 / VT.W.2.2.1 / VT.S.1.1/
VT.S.1.2.1 / VT.S.1.4.1 / VT.S.2.1 / VT.S.2.2.1 / VT.S.2.4.1



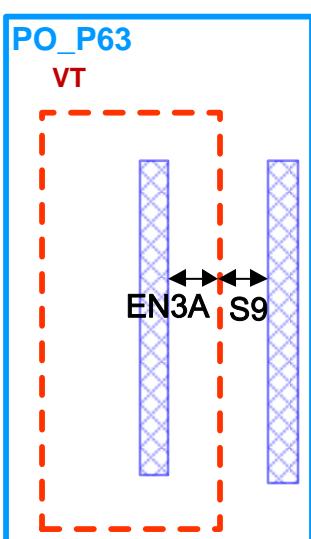
**VT.S.4 / VT.S.4.0.1 / VT.S.4.0.2 / VT.S.4.1
VT.EN.2 / VT.EN.2.1 / VT.EN.2.2 / VT.EX.4.1**

VT.S.7

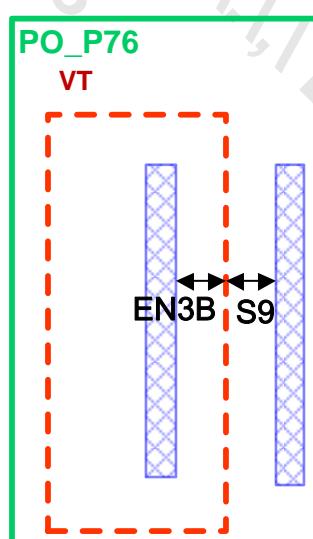


VT.S.5 / VT.EN.3 / VT.S.5.0.1/VT.S.5.0.2

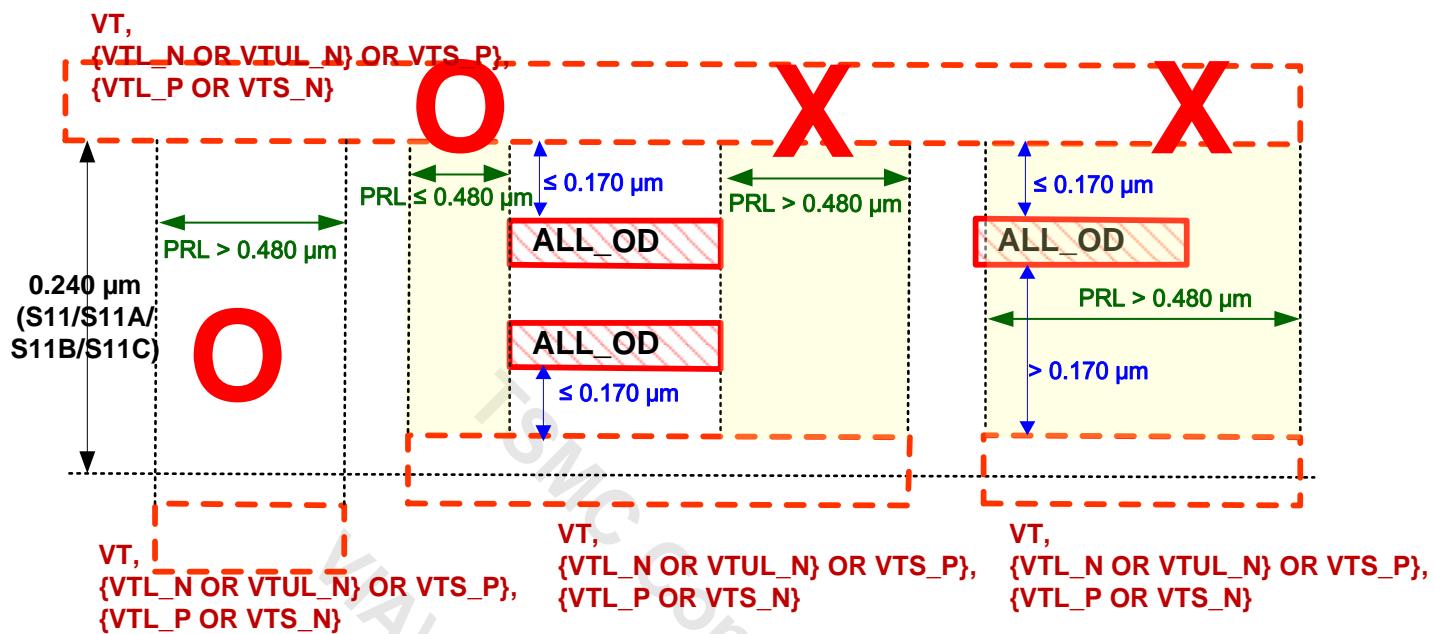
**VT.S.6.1 / VT.S.6.2 / VT.S.6.3 / VT.EN.1 /
VT.EN.1.2 / VT.EN.1.3 / VT.EX.4.1**



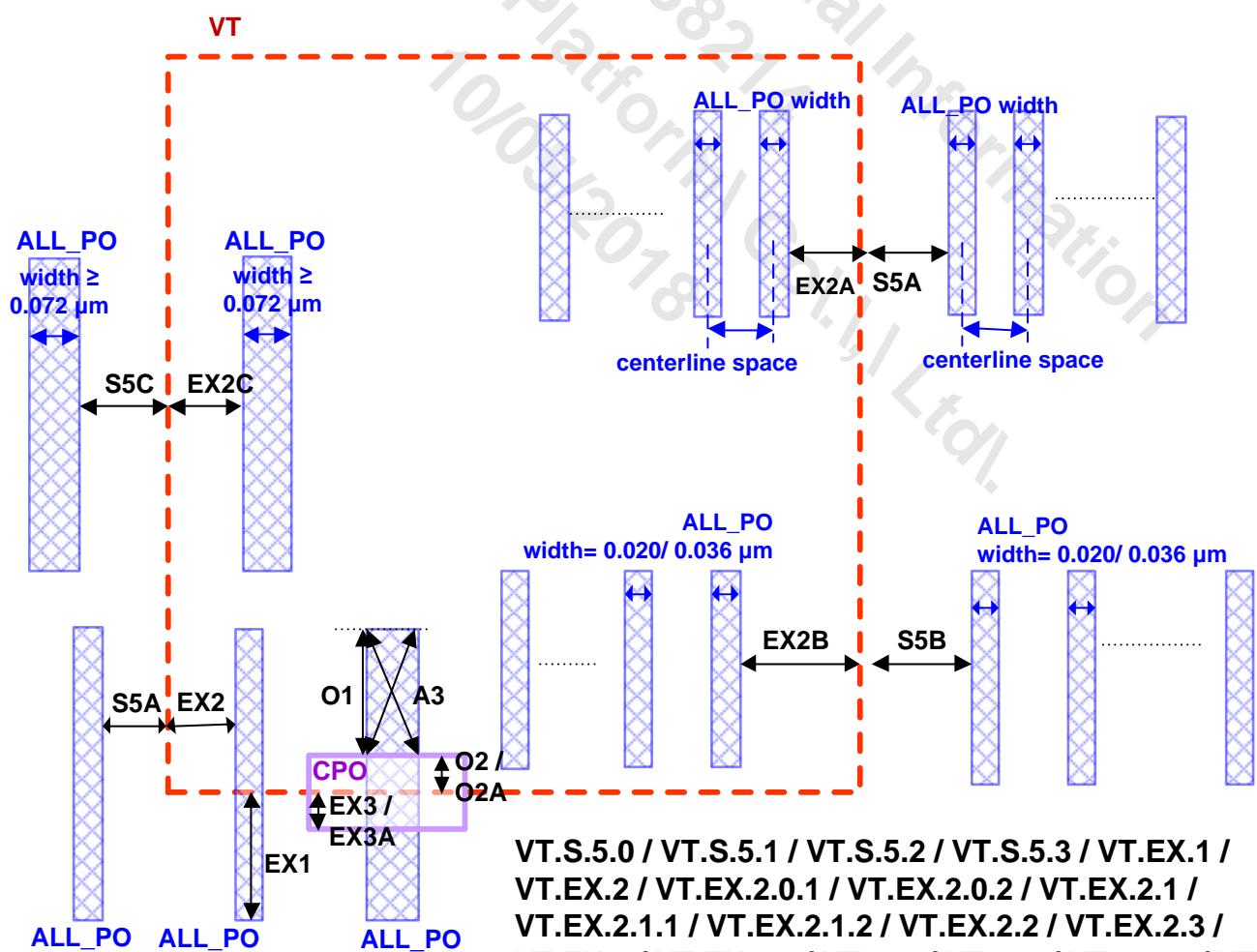
VT.S.9.1 / VT.EN.3.1

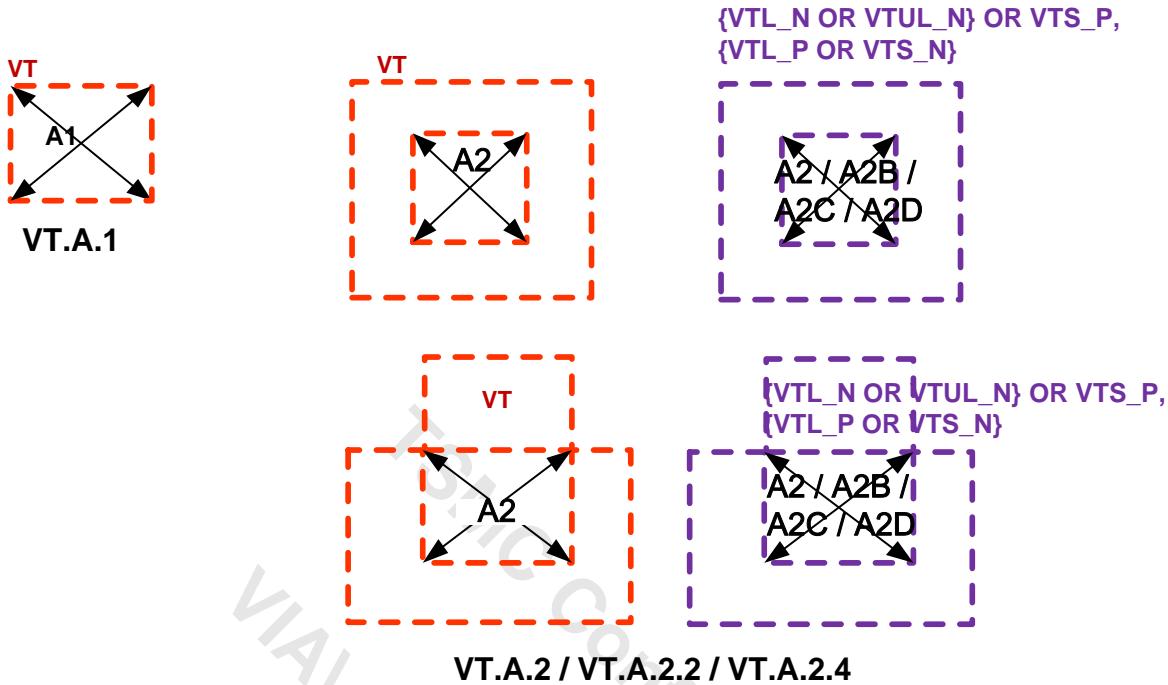


VT.S.9.2 / VT.EN.3.2



VT.S.11 / VT.S.11.1 / VT.S.11.3



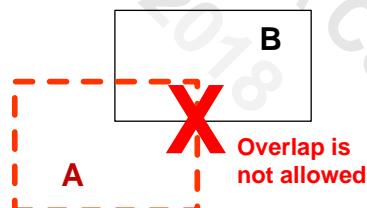


B

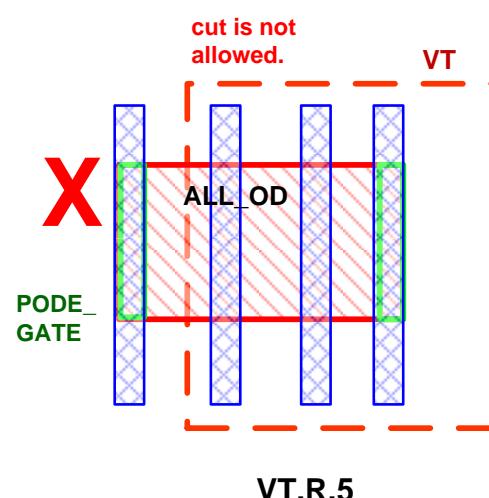
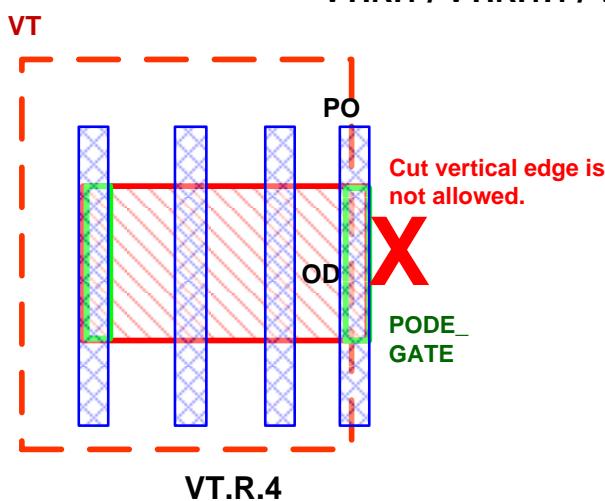
A

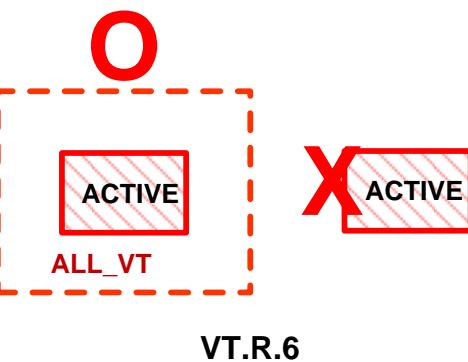
	N+ ACTIVE	P+ ACTIVE	VTS_N	VTS_P	VTL_N	VTL_P	VTUL_N	VTUL_P	OD2
VTS_N		X		X	X	X	X	X	X
VTS_P	X		X		X	X	X	X	X
VTL_N		X	X	X		X	X	X	X
VTL_P	X		X	X	X		X	X	X
VTUL_N		X	X	X	X	X		X	X
VTUL_P	X		X	X	X	X	X		X

"X" means overlap is not allowed

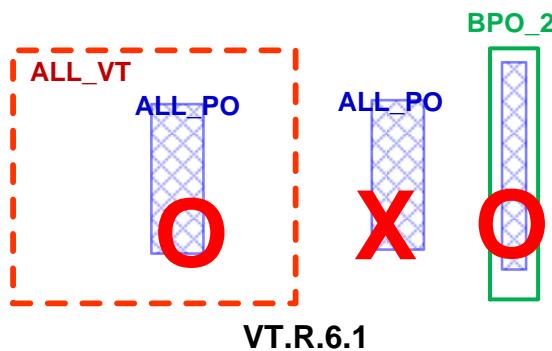


VT.R.1 / VT.R.1.1 / VT.R.1.2 / VT.R.1.3

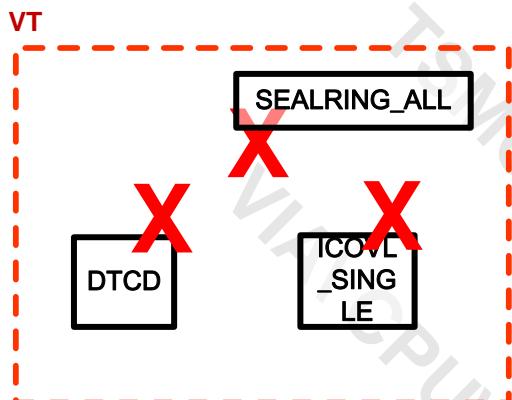




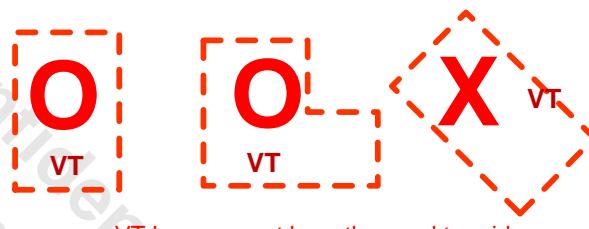
VT.R.6



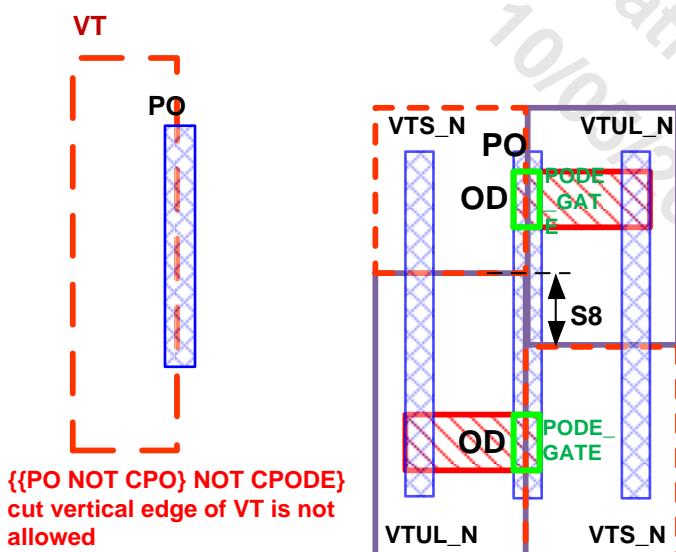
VT.R.6.1



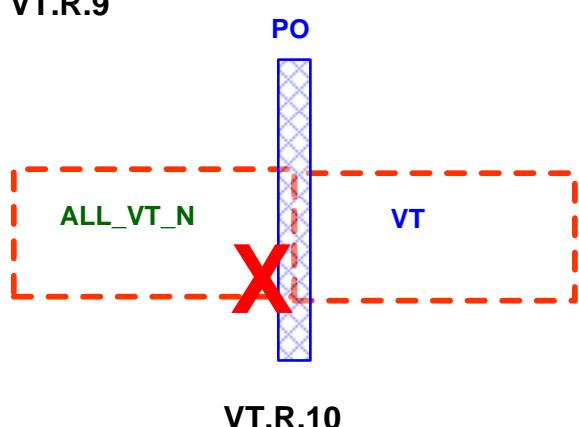
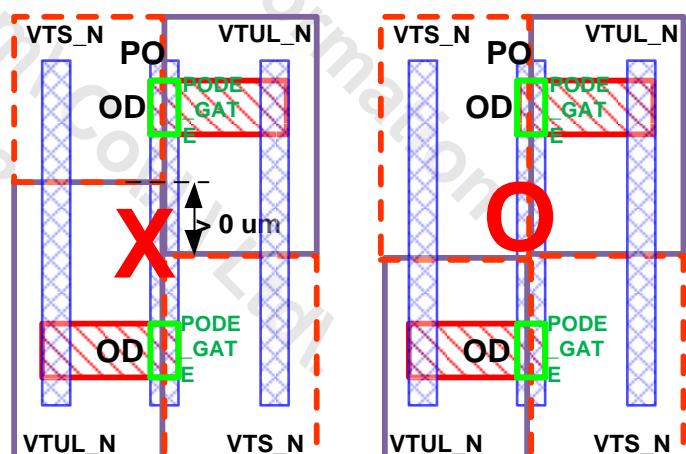
VT.R.7



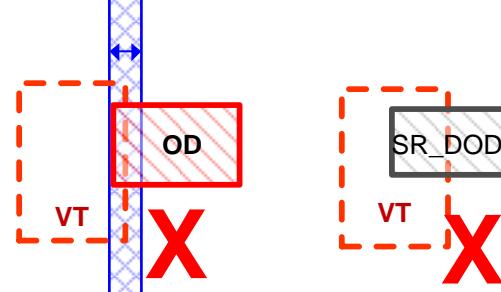
VT.R.8



VT.R.9



VT.R.10

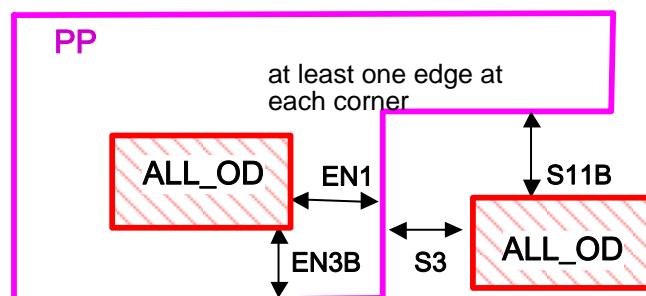
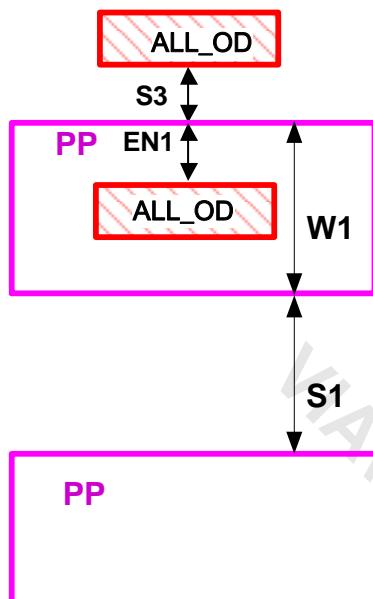


VT.R.11

4.5.26 P+ Source/Drain Ion Implantation (PP) Layout Rules

Rule No.	Description	Label	Op.	Rule
PP.W.1	Width (Except FB_9, FB_8, BLK_WF, SEALRING_ALL)	W1	\geq	0.1600
PP.W.1.1	Width [space < 0.192 μm] (Except FB_9, FB_8, BLK_WF) (DRC flags opposite side)	W1A	\geq	0.1920
PP.W.1.2	Width [edge space to PP < 0.180 μm] (Except BLK_WF) (DRC flags the edge formed by 2 consecutive 90-90 degree corners)	W1B	\geq	0.2000
PP.S.1	Space (Except FB_9, FB_8, BLK_WF)	S1	\geq	0.1600
PP.S.1.2	Space [width < 0.192 μm] (Except FB_9, FB_8, BLK_WF) (DRC flags opposite side)	S1B	\geq	0.1920
PP.S.1.3	Space to PP [edge length < 0.180 μm] (Except FB_9, FB_8, BLK_WF) (DRC flags the edge formed by 2 consecutive 90-90 degree corners)	S1C	\geq	0.2000
PP.S.1.4	Space [in horizontal direction for space PRL > 0.250 μm , or INSIDE OD2 for space PRL > 0.250 μm] (Except BLK_WF)	S1D	\geq	0.2000
PP.S.1.5	Space [PRL > 0.480 μm [excluding projection of ALL_OD on PP within 0.170 μm at both sides]]	S1E	\geq	0.2400
PP.S.3	Space to ALL_OD (Except FB_9, BLK_WF, Dummy_Cell)	S3	\geq	0.0410
PP.S.6	Space of PP [edge length < 0.276 μm] to N+ ACTIVE [PRL > 0 μm] (Except BLK_WF)	S6	\geq	0.0650
PP.S.11.2	Space to ALL_OD [at least one edge at each corner] (Except BLK_WF, Dummy_Cell)	S11B	\geq	0.0710
PP.S.11.3	Space of PP [edge length < 0.270 μm] to ALL_OD [NOT INSIDE Dummy_Cell] (Except BLK_WF)	S11C	\geq	0.0770
PP.S.12	Space to SRM (50;0) (Space = 0 μm is allowed)	S12	\geq	0.2100
PP.EN.1	Enclosure of ALL_OD (Except FB_9, BLK_WF, Dummy_Cell)	EN1	\geq	0.0410
PP.EN.3.2	Enclosure of ALL_OD [at least one edge at each corner] (Except BLK_WF, Dummy_Cell)	EN3B	\geq	0.0710
PP.EN.4	PP [edge length < 0.276 μm] enclosure of P+ ACTIVE [PRL > 0 μm] (Except BLK_WF)	EN4	\geq	0.0650
PP.EN.5.1	PP [edge length < 0.270 μm] enclosure of ALL_OD (Except BLK_WF, or following conditions: 1. DC_OD_WONP) Definition of DC_OD_WONP: {DC_Core NOT DC3} OR DC_IO OR DC6_2}	EN5A	\geq	0.0770
PP.EN.7	PP enclosure of ALL_PO (Except Dummy_Cell, BLK_WF, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	EN7	\geq	0.0050
PP.EN.7.1	PP enclosure of ALL_PO [width \leq 0.011 μm] in horizontal direction (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	EN7A	\geq	0.0050

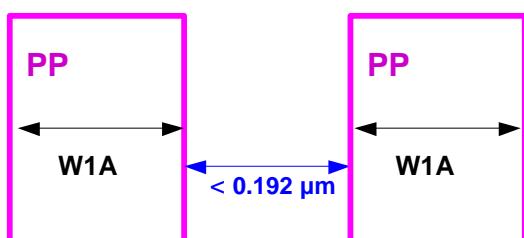
Rule No.	Description	Label	Op.	Rule
PP.EN.7.2	PP enclosure of ALL_PO [width \geq 0.020 μm] in horizontal direction (Except Dummy_Cell)	EN7B	\geq	0.0390
PP.EN.8	PP enclosure of ALL_PO in vertical direction (Except Dummy_Cell, BLK_WF, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	EN8	\geq	0.0400
PP.EN.8.1	PP enclosure of ALL_PO [width \leq 0.011 μm] in vertical direction (Except BLK_WF, Dummy_Cell, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	EN8A	\geq	0.1100
PP.EN.8.2	PP enclosure of ALL_PO [width \geq 0.020 μm] in vertical direction (Except IBJTDY, Dummy_Cell)	EN8B	\geq	0.0670
PP.L.1	45-degree edge length (Except SEALRING_ALL)	L1	\geq	0.4500
PP.A.1	Area (Except BLK_WF, SEALRING_ALL)	A1	\geq	0.07000
PP.A.1.1	Area of PP, {{{{{PP NOT OD2} AND NW} NOT IBJTDY} NOT VAR} NOT RH_TNB} SIZING up/down/down/up 0.054 μm , {{{{{PP AND OD2} AND NW} NOT IBJTDY} NOT VAR} NOT RH_TNB} SIZING up/down/down/up 0.054 μm (Except BLK_WF, SEALRING_ALL)	A1A	\geq	0.07000
PP.A.1.2	Area of {PP AND {PO_P63 OR PO_P76}}	A1B	\geq	0.07000
PP.A.3	Enclosed area	A3	\geq	0.07000
PP.A.3.2	Enclosed area of {PP AND {PO_P63 OR PO_P76}}	A3B	\geq	0.07000
PP.A.3.1	Enclosed area of PP, {{{{{PP NOT OD2} AND NW} NOT IBJTDY} NOT VAR} NOT RH_TNB} SIZING up/down/down/up 0.054 μm , {{{{{PP AND OD2} AND NW} NOT IBJTDY} NOT VAR} NOT RH_TNB} SIZING up/down/down/up 0.054 μm	A3A	\geq	0.07000
PP.R.1	PP must fully cover {Core PMOS TrGATE SIZING 0.041 μm } (R1) (Except FB_9, BLK_WF)			
PP.R.2	PP must fully cover {I/O PMOS TrGATE SIZING 0.075 μm } (R2)			
PP.R.3	Overlap NP is not allowed			
PP.R.4	ALL_OD must be fully covered by {NP OR PP} (Except Dummy_Cell, RH_TNB)			
PP.R.5	{{{ALL_PO [width \leq 0.011 μm] SIZING 0.110 μm in vertical direction} SIZING 0.023 μm in horizontal direction} must be fully covered by {NP OR PP} (Except RH_TNB, Dummy_Cell)}			
PP.R.6	PP and NP at the same ALL_OD is not allowed (Except Dummy_Cell)			
PP.R.7	{{{ALL_PO [width \geq 0.020 μm] SIZING 0.067 μm in vertical direction} SIZING 0.046 μm in horizontal direction} must be fully covered by {NP OR PP} (Except Dummy_Cell, IBJTDY, SEALRING_ALL)}			
PP.R.8	Vertical edge of NP or PP cut ALL_PO is not allowed (Except Dummy_Cell, SEALRING_ALL)			
PP.R.9	{PP NOT {PP SIZING -0.160 μm in vertical direction}} must interact at least one {ALL_PO NOT DC_PO} (Except SEALRING_ALL, DC3)			
PP.R.9.1	{PP NOT {PP SIZING -0.160 μm in horizontal direction}} must interact at least one {ALL_PO NOT DC_PO} (Except SEALRING_ALL, DC3)			
PP.R.9.2	Enclosure of {ALL_PO NOT DC_PO} line-end [ALL_PO width \geq 0.020 μm] in 0.1105 μm ~ 0.1600 μm region in vertical direction is not allowed (Except DC3)			

PP

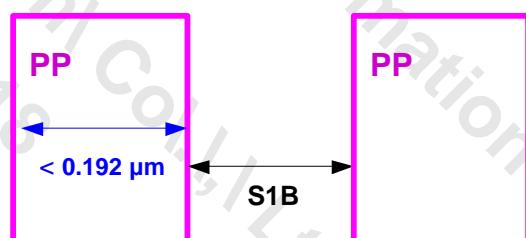
**PP.S.3/ PP.S.11.2/
PP.EN.1/PP.EN.3.2**



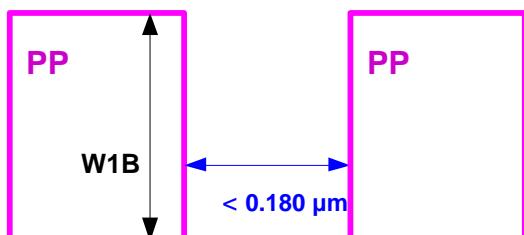
PP.S.6 /PP.EN.4



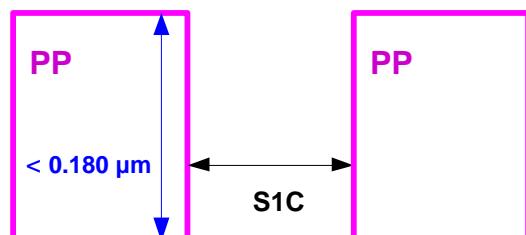
PP.W.1.1



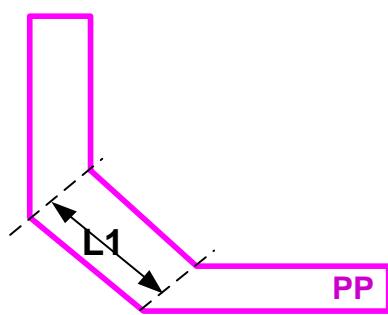
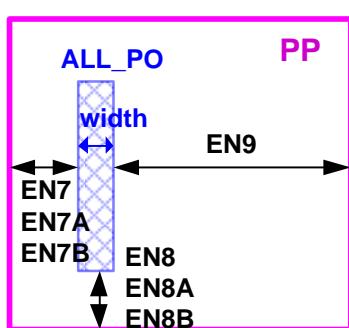
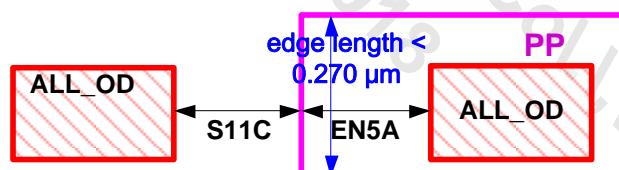
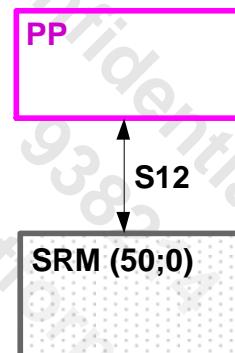
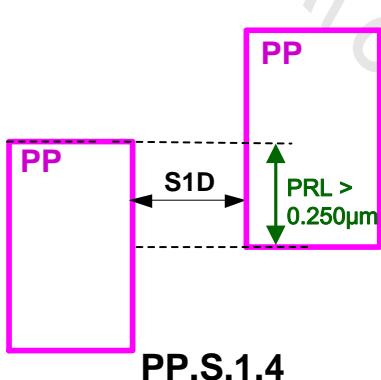
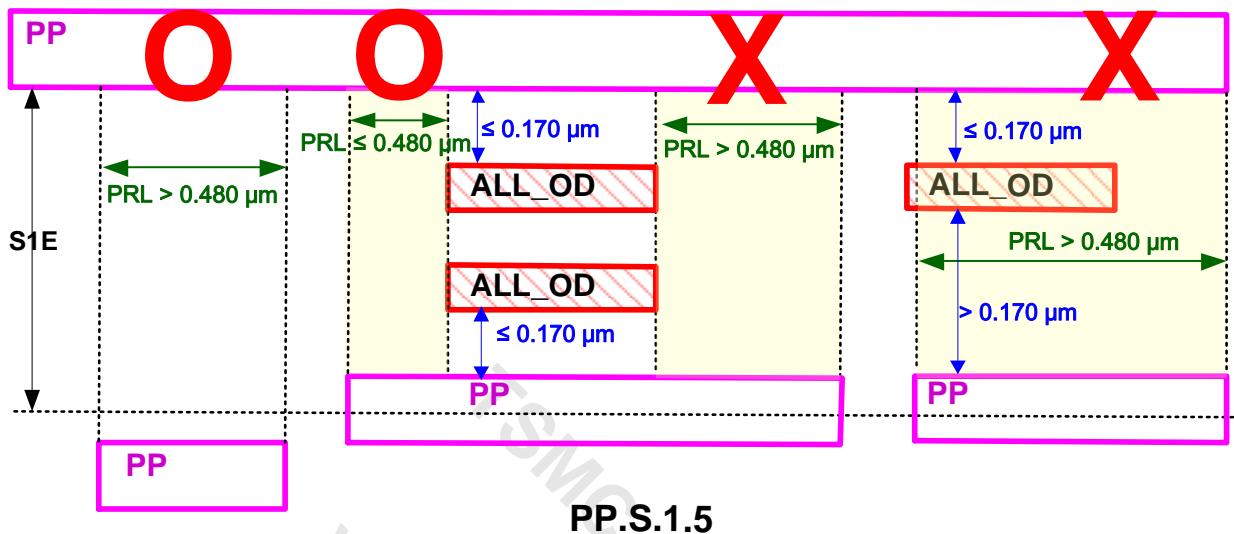
PP.S.1.2

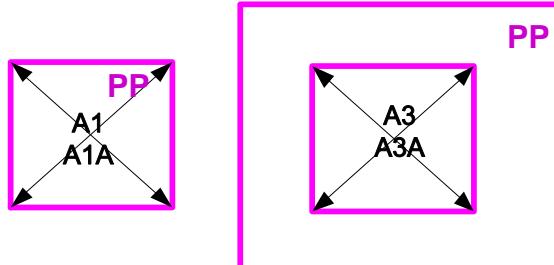


PP.W.1.2

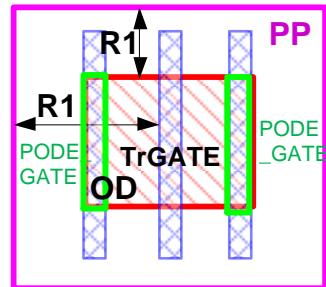


PP.S.1.3

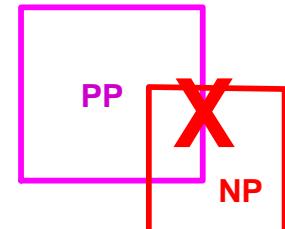




PP.A.1 / PP.A.1.1 / PP.A.1.2 /
PP.A.3 / PP.A.3.1 / PP.A.3.2

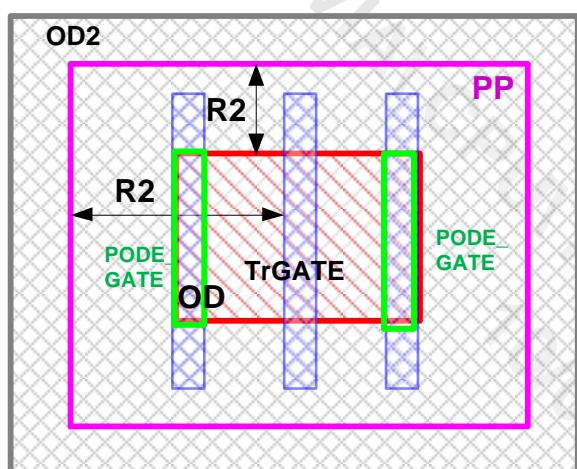


PP.R.1

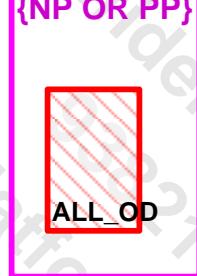


Overlap of NP is not allowed

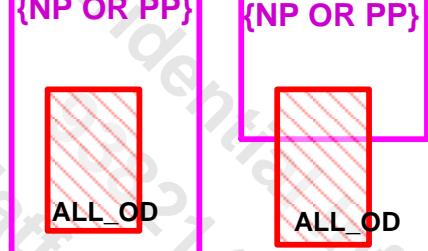
PP.R.3



PP.R.2

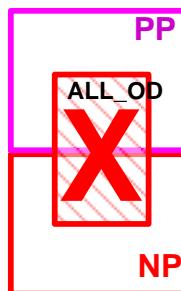


ALL_OD must be fully covered by {NP OR PP}

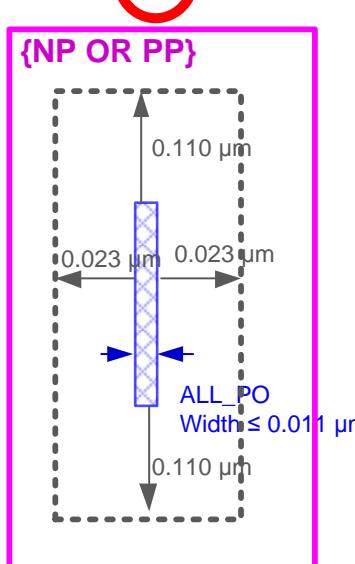


PP and NP at the same
ALL_OD is not allowed

PP.R.4

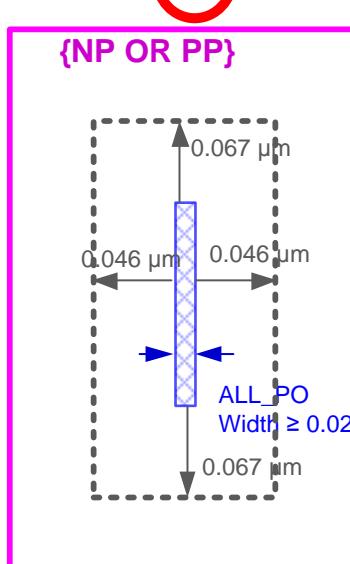


PP.R.6



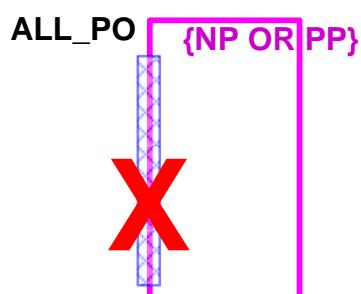
Must be fully covered by {NP OR PP}

PP.R.5

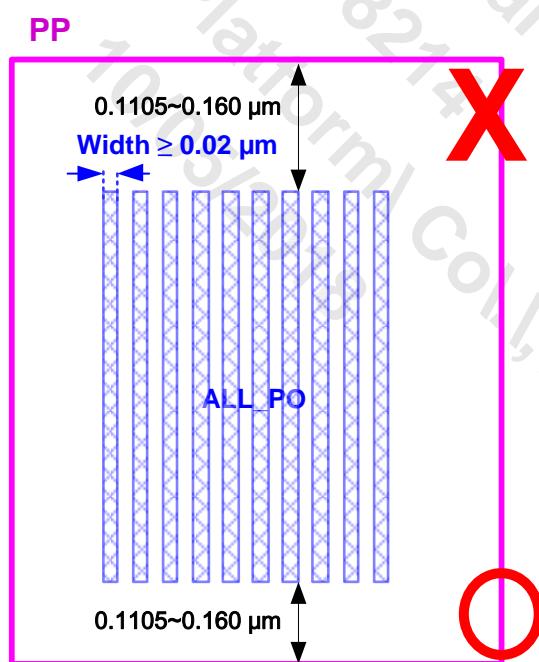
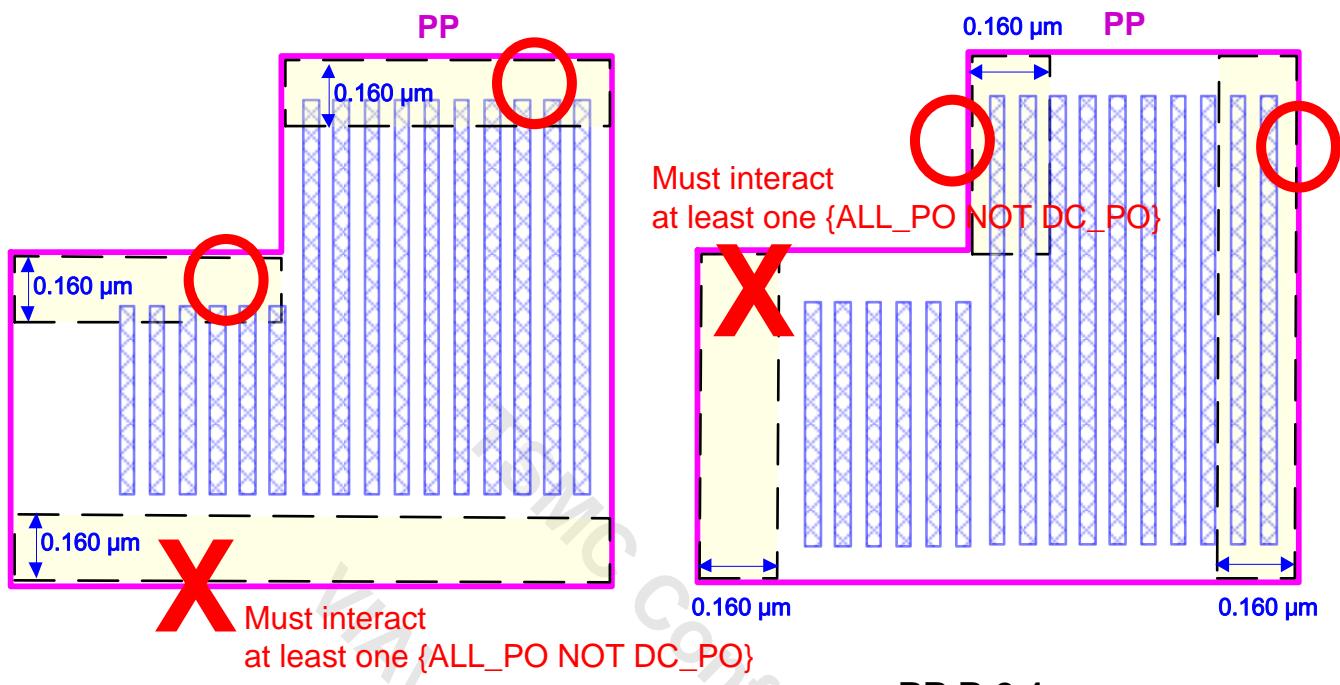


ALL_PO Width $\geq 0.020 \mu\text{m}$

PP.R.7



PP.R.8

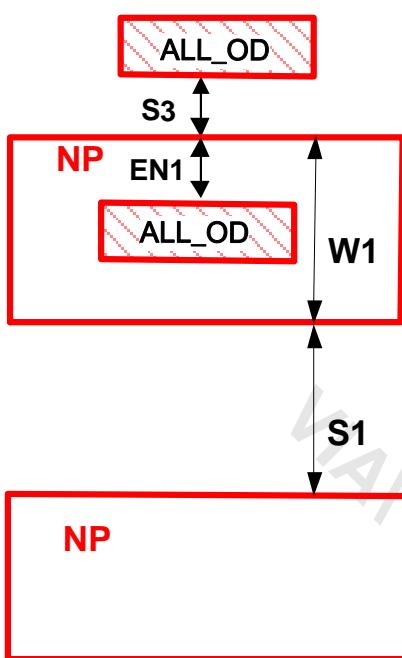


4.5.27 N+ Source/Drain Ion Implantation (NP) Layout Rules

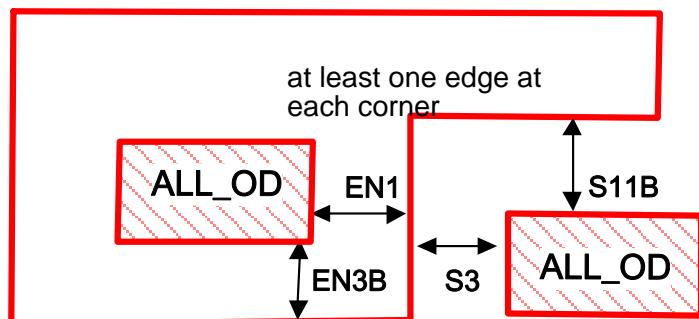
Rule No.	Description	Label	Op.	Rule
NP.W.1	Width (Except FB_9, FB_8, BLK_WF)	W1	\geq	0.1600
NP.W.1.1	Width [space < 0.192 μm] (Except FB_9, FB_8, BLK_WF) (DRC flags opposite side)	W1A	\geq	0.1920
NP.W.1.2	Width [edge space to NP < 0.180 μm] (Except BLK_WF) (DRC flags the edge formed by 2 consecutive 90-90 degree corners)	W1B	\geq	0.2000
NP.S.1	Space (Except FB_9, FB_8, BLK_WF, or following conditions: 1. Space of NP to NP [INTERACT SEALRING_ALL])	S1	\geq	0.1600
NP.S.1.2	Space [width < 0.192 μm] (Except FB_9, FB_8, BLK_WF) (DRC flags opposite side)	S1B	\geq	0.1920
NP.S.1.3	Space to NP [edge length < 0.180 μm] (Except FB_9, FB_8, BLK_WF) (DRC flags the edge formed by 2 consecutive 90-90 degree corners)	S1C	\geq	0.2000
NP.S.1.4	Space [in horizontal direction for space PRL > 0.250 μm , or INSIDE OD2 for space PRL > 0.250 μm] (Except BLK_WF, or following conditions: 1. Space of NP to NP [INTERACT SEALRING_ALL])	S1D	\geq	0.2000
NP.S.1.5	Space [PRL > 0.480 μm [excluding projection of ALL_OD on NP within 0.170 μm at both sides]] (Except following conditions: 1. Space of NP to NP [INTERACT SEALRING_ALL])	S1E	\geq	0.2400
NP.S.3	Space to ALL_OD (Except FB_9, BLK_WF, Dummy_Cell)	S3	\geq	0.0410
NP.S.6	Space of NP [edge length < 0.276 μm] to P+ ACTIVE [PRL > 0 μm] (Except BLK_WF)	S6	\geq	0.0650
NP.S.11.2	Space to ALL_OD [at least one edge at each corner] (Except BLK_WF, Dummy_Cell)	S11B	\geq	0.0710
NP.S.11.3	Space of NP [edge length < 0.270 μm] to ALL_OD [NOT INSIDE Dummy_Cell] (Except BLK_WF)	S11C	\geq	0.0770
NP.S.12	Space to SRM (50;0) (Space = 0 μm is allowed)	S12	\geq	0.2100
NP.EN.1	Enclosure of ALL_OD (Except FB_9, BLK_WF, Dummy_Cell)	EN1	\geq	0.0410
NP.EN.3.2	Enclosure of ALL_OD [at least one edge at each corner] (Except BLK_WF, Dummy_Cell)	EN3B	\geq	0.0710
NP.EN.4	NP [edge length < 0.276 μm] enclosure of N+ ACTIVE [PRL > 0 μm] (Except BLK_WF)	EN4	\geq	0.0650
NP.EN.5.1	NP [edge length < 0.270 μm] enclosure of ALL_OD (Except BLK_WF, or following conditions: 1. DC_OD_WONP) Definition of DC_OD_WONP: {DC_Core NOT DC3} OR DC_IO OR DC6_2}	EN5A	\geq	0.0770

Rule No.	Description	Label	Op.	Rule
NP.EN.7	NP enclosure of ALL_PO (Except Dummy_Cell, BLK_WF, or following conditions: 1. small ALL_PO jog $\leq 0.002 \mu\text{m}$)	EN7	\geq	0.0050
NP.EN.7.1	NP enclosure of ALL_PO [width $\leq 0.011 \mu\text{m}$] in horizontal direction (Except Dummy_Cell, or following conditions: 1. small ALL_PO jog $\leq 0.002 \mu\text{m}$)	EN7A	\geq	0.0050
NP.EN.7.2	NP enclosure of ALL_PO [width $\geq 0.020 \mu\text{m}$] in horizontal direction (Except Dummy_Cell)	EN7B	\geq	0.0390
NP.EN.8	NP enclosure of ALL_PO in vertical direction (Except Dummy_Cell, BLK_WF, or following conditions: 1. small ALL_PO jog $\leq 0.002 \mu\text{m}$)	EN8	\geq	0.0400
NP.EN.8.1	NP enclosure of ALL_PO [width $\leq 0.011 \mu\text{m}$] in vertical direction (Except BLK_WF, Dummy_Cell, or following conditions: 1. small ALL_PO jog $\leq 0.002 \mu\text{m}$)	EN8A	\geq	0.1100
NP.EN.8.2	NP enclosure of ALL_PO [width $\geq 0.020 \mu\text{m}$] in vertical direction (Except IBJTD MY, Dummy_Cell)	EN8B	\geq	0.0670
NP.L.1	45-degree edge length	L1	\geq	0.4500
NP.A.1	Area	A1	\geq	0.07000
NP.A.1.1	Area of NP, {{{{{NP NOT OD2} NOT {NW OR NT_N}}} NOT IBJTD MY} NOT VAR} NOT RH_TNB} SIZING up/down/down/up 0.054 μm , {{{{{NP AND OD2} NOT {NW NOT NT_N}}} NOT IBJTD MY} NOT VAR} NOT RH_TNB} SIZING up/down/down/up 0.054 μm	A1A	\geq	0.07000
NP.A.3	Enclosed area	A3	\geq	0.07000
NP.A.3.1	Enclosed area of NP, {{{{{NP NOT OD2} NOT {NW OR NT_N}}} NOT IBJTD MY} NOT VAR} NOT RH_TNB} SIZING up/down/down/up 0.054 μm , {{{{{NP AND OD2} NOT {NW NOT NT_N}}} NOT IBJTD MY} NOT VAR} NOT RH_TNB} SIZING up/down/down/up 0.054 μm	A3A	\geq	0.07000
NP.R.1	NP must fully cover {Core NMOS TrGATE SIZING 0.041 μm } (R1) (Except FB_9, BLK_WF)			
NP.R.2	NP must fully cover {I/O NMOS TrGATE SIZING 0.075 μm } (R2)			
NP.R.3	Overlap PP is not allowed			
NP.R.9	{NP NOT {NP SIZING -0.160 μm in vertical direction}} must interact at least one {ALL_PO NOT DC_PO} (Except SEALRING_ALL, DC3)			
NP.R.9.1	{NP NOT {NP SIZING -0.160 μm in horizontal direction}} must interact at least one {ALL_PO NOT DC_PO} (Except SEALRING_ALL, DC3, or following conditions: 1. NP interact NWDMY)			
NP.R.9.2	Enclosure of {ALL_PO NOT DC_PO} line-end [ALL_PO width $\geq 0.020 \mu\text{m}$] in 0.1105 μm ~ 0.1600 μm region in vertical direction is not allowed (Except DC3)			

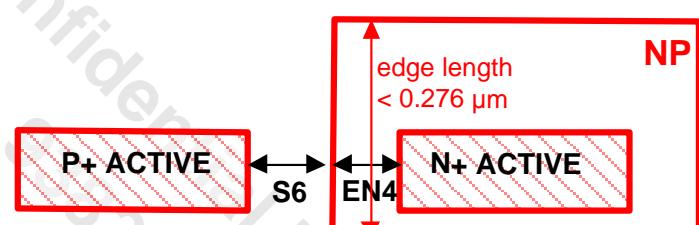
NP



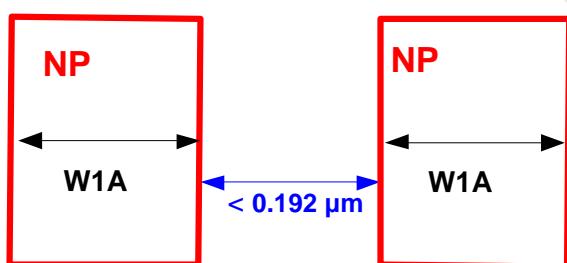
NP.W.1 / NP.S.1 / NP.S.3 / NP.EN.1



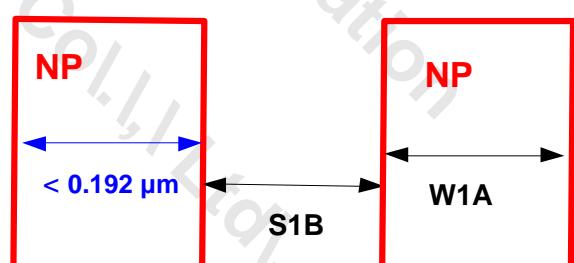
**NP.S.3/ NP.S.11.2/
NP.EN.1/NP.EN.3.2**



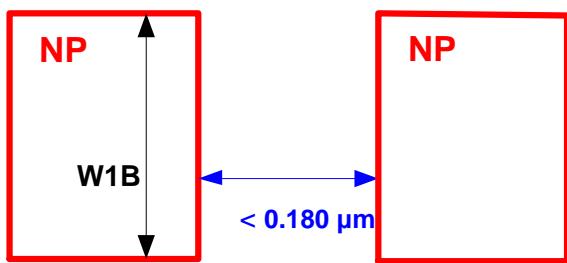
NP.S.6 /NP.EN.4



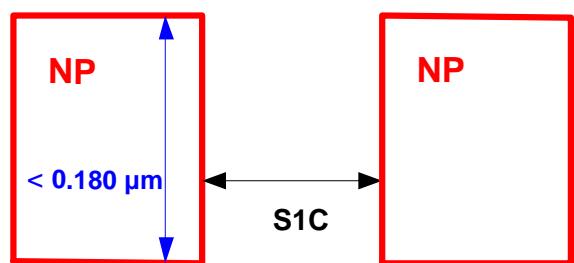
NP.W.1.1



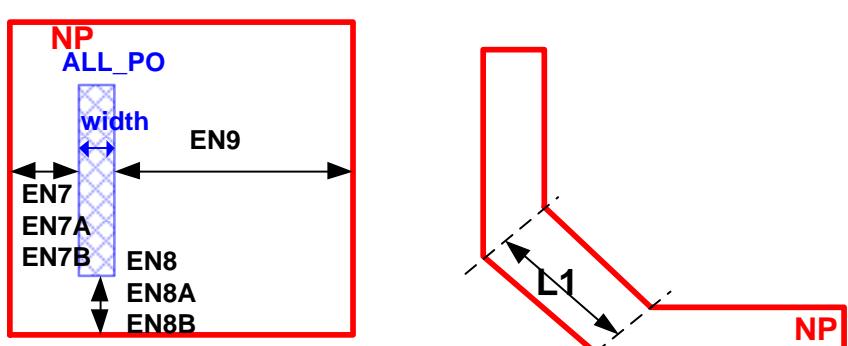
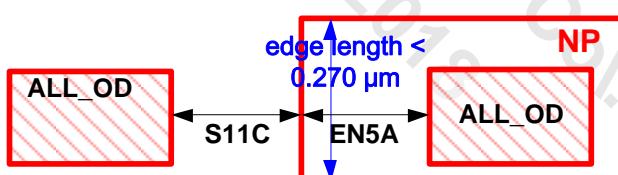
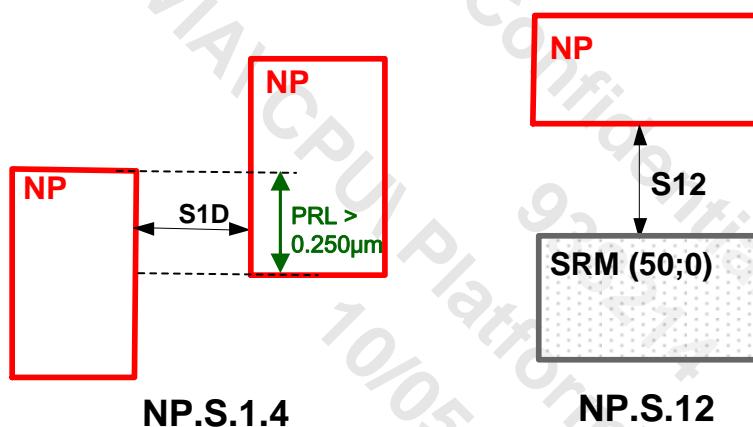
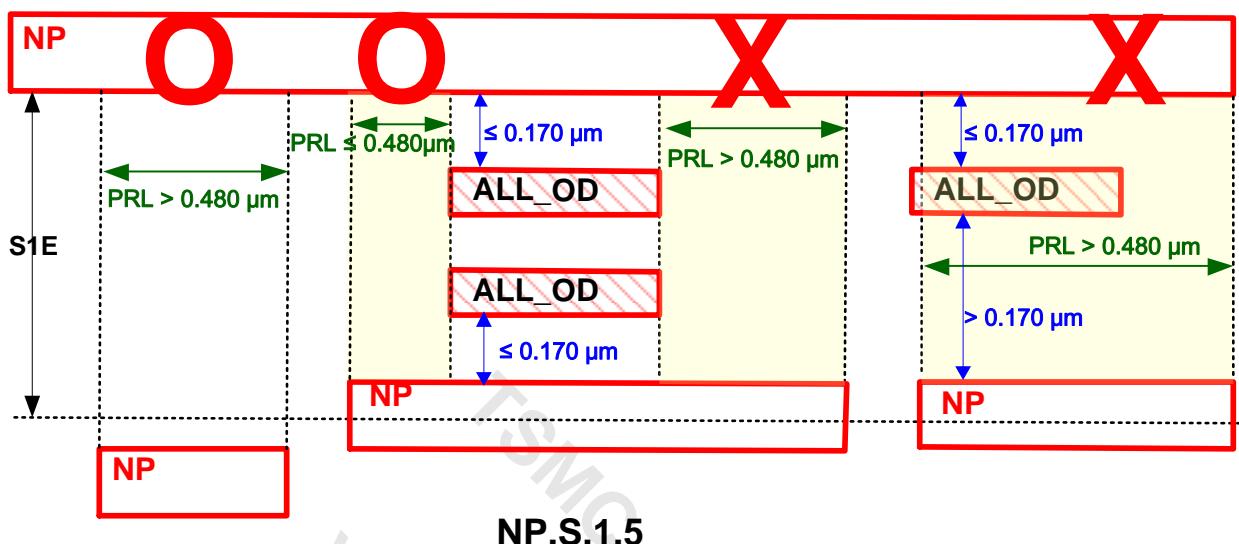
NP.S.1.2

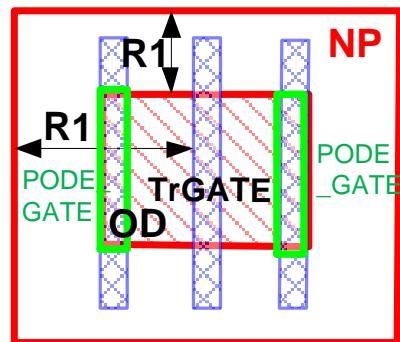
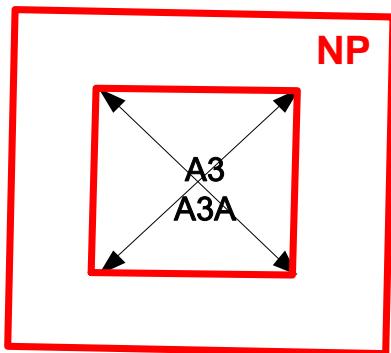
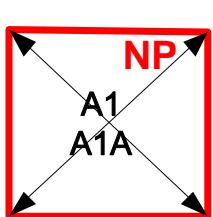


NP.W.1.2



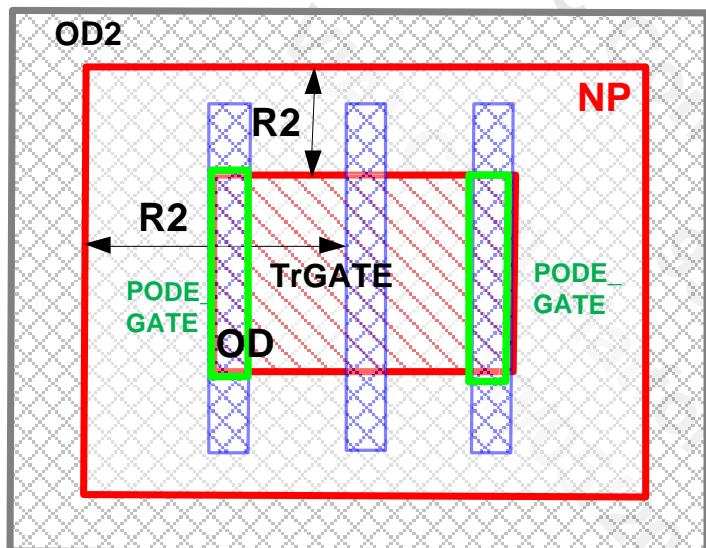
NP.S.1.3



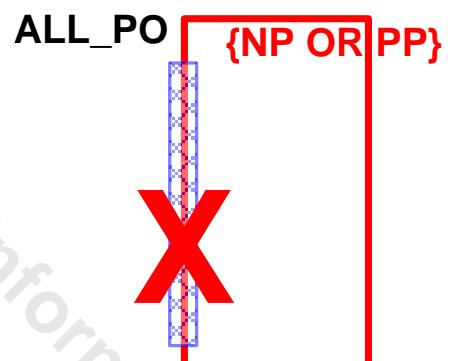


NP.A.1/ NP.A.1.1
NP.A.3 / NP.A.3.1

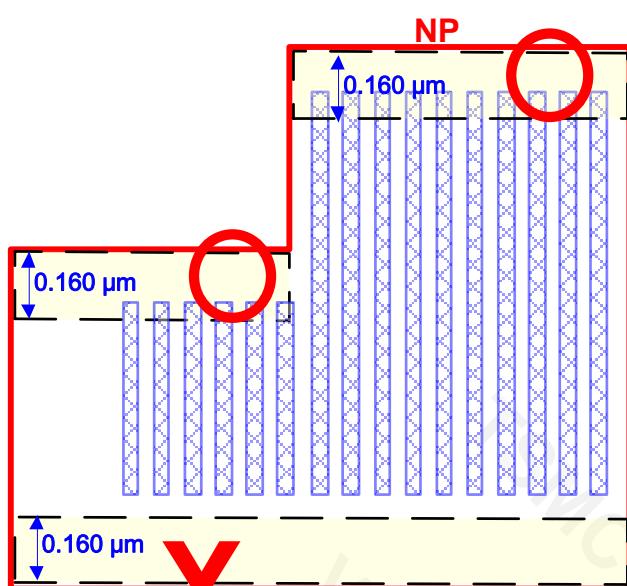
NP.R.1



NP.R.2

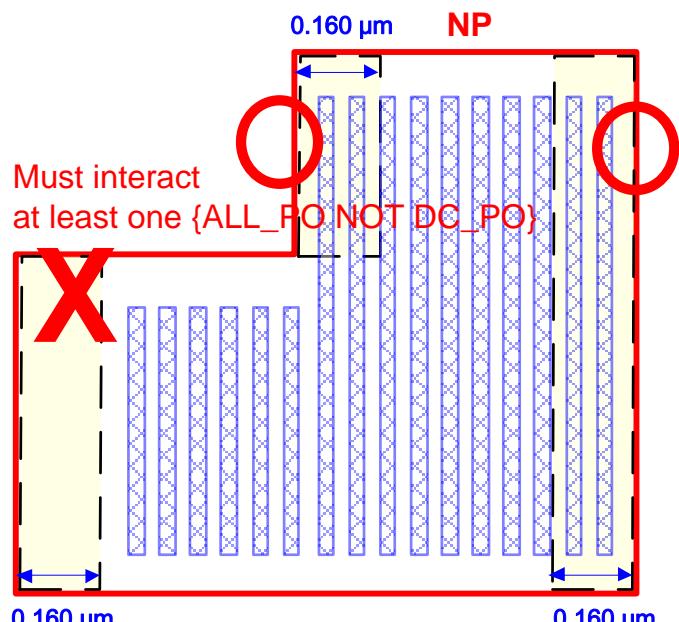


NP.R.3

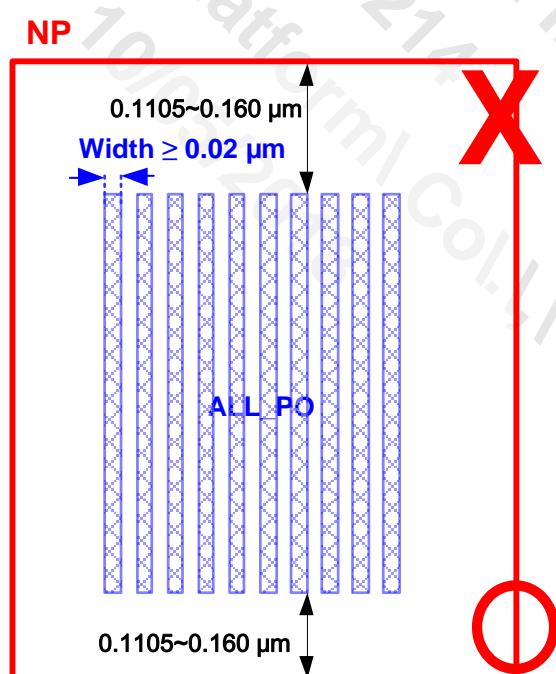


Must interact
at least one {ALL_PO NOT DC_PO}

NP.R.9



NP.R.9.1



NP.R.9.2

4.5.28 Layout Rules for Strained S/D Mask Logical Operation

Mask 123 and 126 are necessary in N7+ process.

Rule No.	Description	Label	Op.	Rule
SSD.DN.1	Strained S/D (mask ID: 123) open ratio should be $\geq 5\%$ and be as uniform as possible over the chip DRC methodology: Minimum $\{\{\{PP \text{ OR } DC_WO_IMP}\} \text{ AND } ALL_OD\} \text{ NOT } \{ALL_PO \text{ SIZING } 0.012 \mu\text{m}\}$ density across full chip $\geq 5\%$		\geq	5%
SSD.DN.2	Strained S/D (mask ID: 126) open ratio should be $\geq 4\%$ and be as uniform as possible over the chip DRC methodology: Minimum $\{\{\{NP \text{ NOT } DC_WO_IMP}\} \text{ AND } ALL_OD\} \text{ NOT } \{ALL_PO \text{ SIZING } 0.012 \mu\text{m}\}$ density across full chip $\geq 4\%$		\geq	4%
SSD.DN.3	Strained S/D (mask ID: 123) open ratio should be $\leq 17\%$ and be as uniform as possible over the chip DRC methodology: Maximum $\{\{\{PP \text{ OR } DC_WO_IMP}\} \text{ AND } ALL_OD\} \text{ NOT } \{ALL_PO \text{ SIZING } 0.012 \mu\text{m}\}$ density across full chip $\leq 17\%$		\leq	17%
SSD.DN.4	Strained S/D (mask ID: 126) open ratio should be $\leq 17\%$ and be as uniform as possible over the chip DRC methodology: Maximum $\{\{\{NP \text{ NOT } DC_WO_IMP}\} \text{ AND } ALL_OD\} \text{ NOT } \{ALL_PO \text{ SIZING } 0.012 \mu\text{m}\}$ density across full chip $\leq 17\%$		\leq	17%
SSD.DN.5	Strained S/D (mask ID: 123) open ratio in window $20 \mu\text{m} \times 20 \mu\text{m}$, stepping $10 \mu\text{m}$ should be $\leq 30\%$ and be as uniform as possible over the chip (Except TCDDMY, ICOVL_SINGLE) DRC methodology: Maximum $\{\{\{PP \text{ OR } DC_WO_IMP}\} \text{ AND } ALL_OD\} \text{ NOT } \{ALL_PO \text{ SIZING } 0.012 \mu\text{m}\}$ density $\leq 30\%$		\leq	30%
SSD.DN.6	Strained S/D (mask ID: 126) open ratio in window $20 \mu\text{m} \times 20 \mu\text{m}$, stepping $10 \mu\text{m}$ should be $\leq 30\%$ and be as uniform as possible over the chip (Except TCDDMY, ICOVL_SINGLE, SEALRING_ALL) DRC methodology: Maximum $\{\{\{NP \text{ NOT } DC_WO_IMP}\} \text{ AND } ALL_OD\} \text{ NOT } \{ALL_PO \text{ SIZING } 0.012 \mu\text{m}\}$ density $\leq 30\%$		\leq	30%



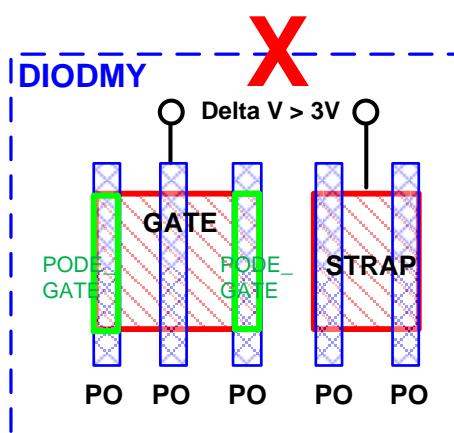
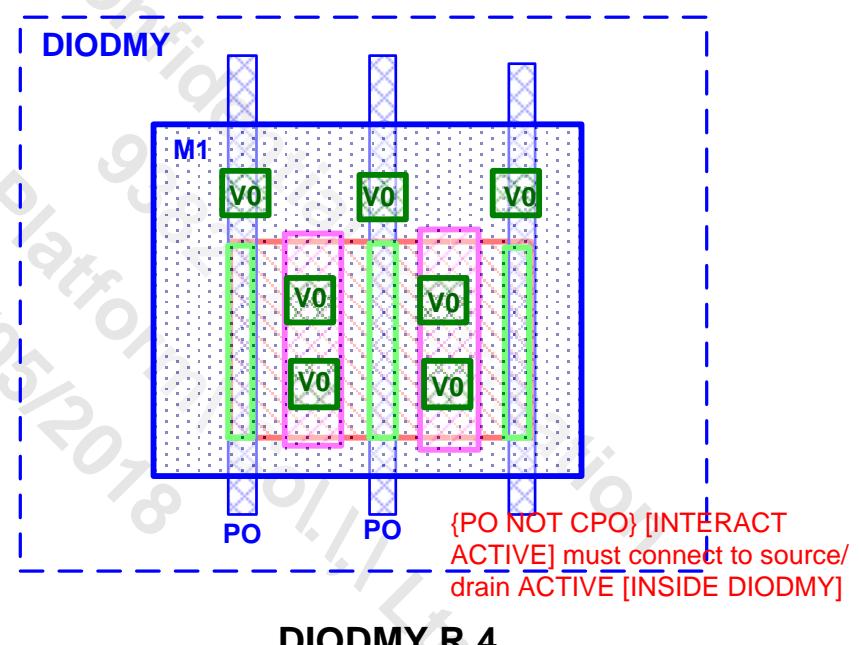
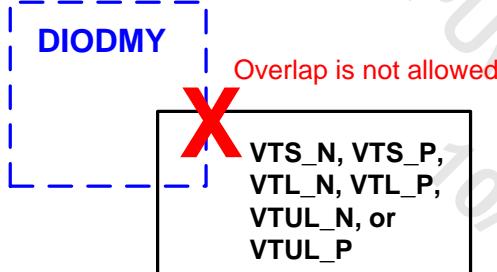
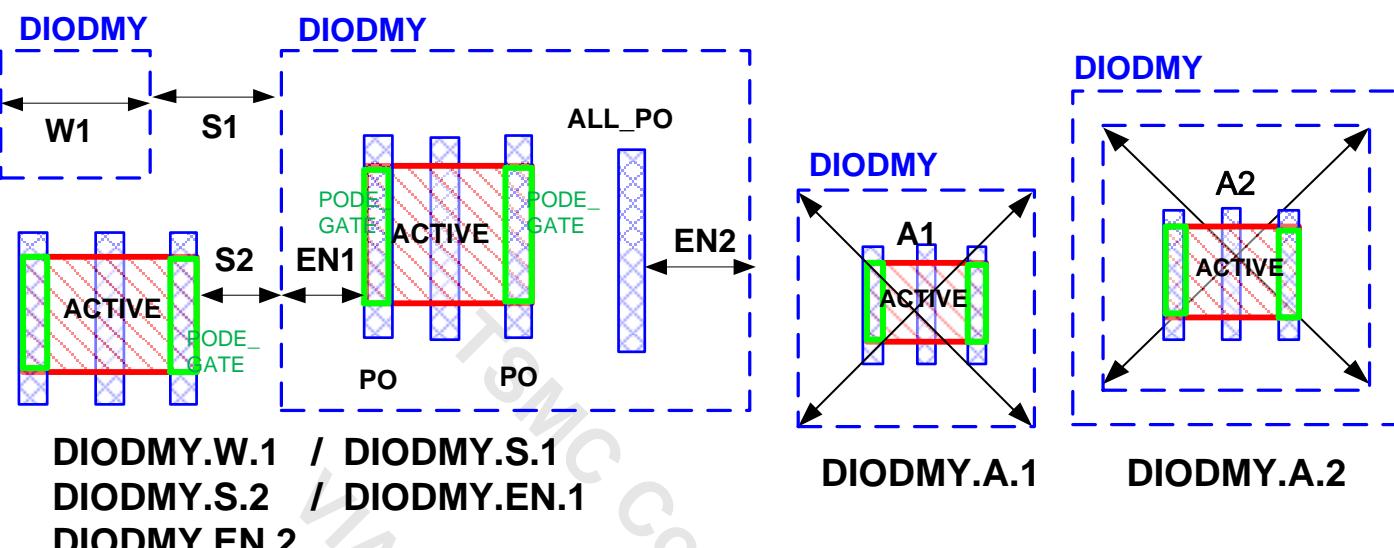
Warning: Using tsmc dummy utility is a must.
If the rules are not followed, the process will
be seriously impacted.

4.5.29 DIODMY Layout Rules

Both N+/P+ diodes need DIODMY for LVS purpose.

Rule No.	Description	Label	Op.	Rule
DIODMY.W.1	Width	W1	\approx	0.1920
DIODMY.S.1	Space	S1	\approx	0.1920
DIODMY.S.2	Space of DIODMY [INTERACT ACTIVE] to ACTIVE ({ACTIVE CUT DIODMY} is not allowed)	S2	\approx	0.0430
DIODMY.EN.1	Enclosure of ACTIVE	EN1	\approx	0.0430
DIODMY.EN.2	Enclosure of ALL_PO [NOT INSIDE Dummy_Cell]	EN2	\approx	0.0350
DIODMY.A.1	Area of DIODMY [INTERACT ACTIVE]	A1	\approx	0.07000
DIODMY.A.2	Enclosed area of DIODMY [INTERACT ACTIVE]	A2	\approx	0.07000
DIODMY.R.1	Overlap VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, or VTUL_P is not allowed			
DIODMY.R.4	{PO NOT CPO} [INTERACT ACTIVE] must connect to source/drain ACTIVE [INSIDE DIODMY]			
DIODMY.R.5	Delta V > 3V between core diode GATE and core diode bulk is not allowed			

DIODMY



4.5.30 High R Resistor Layout Rules

RH_TN (CAD layer 117;6) is used for High R Resistor

SR_DTN (CAD layer 117;7) is used for dummy High R Resistor

RH_TNB (CAD layer 117;8) is used for High R Resistor block layer

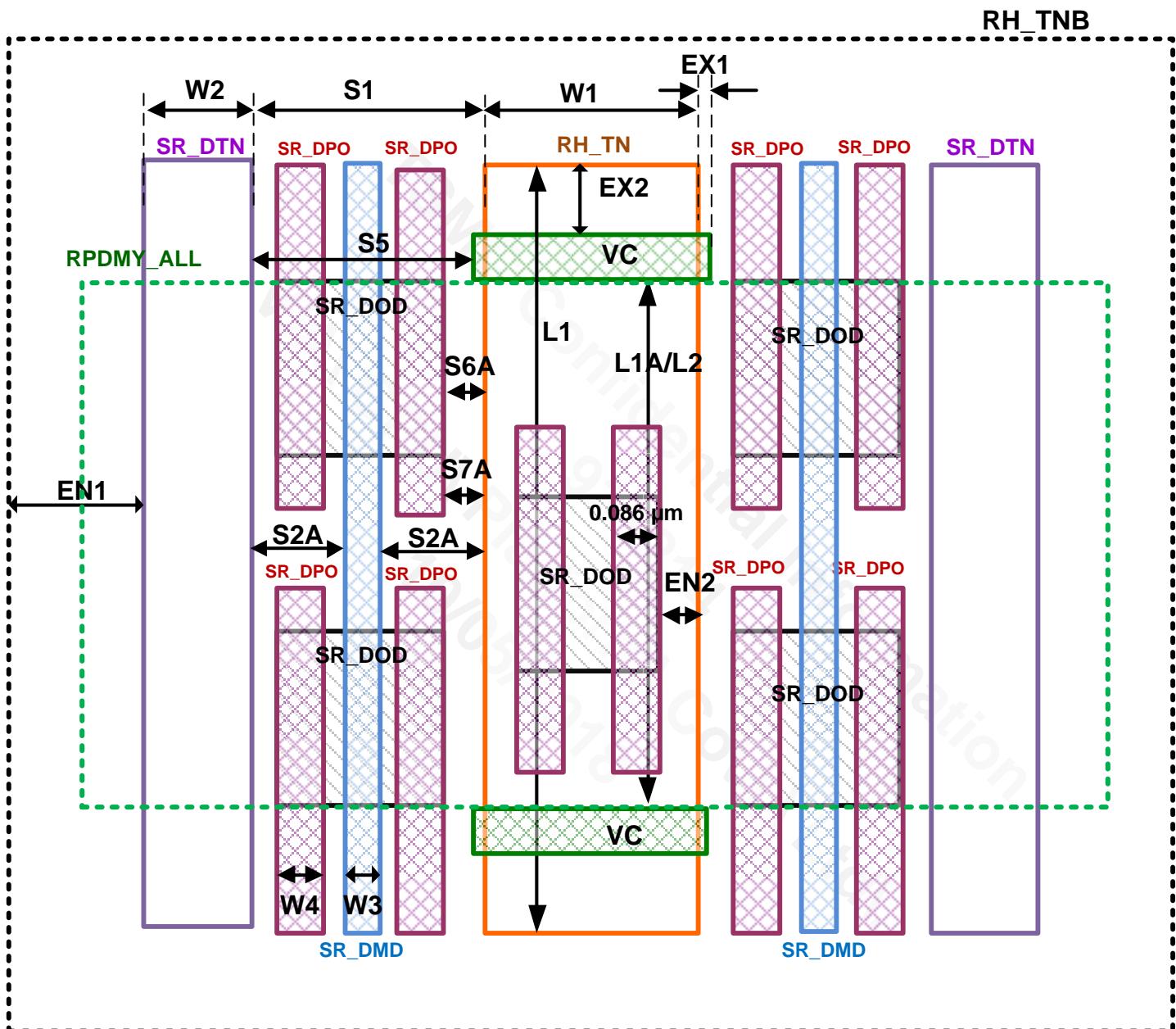
RPDMY_ALL = {RPDMY_1 OR RPDMY_2}

Rule No.	Description	Label	Op.	Rule
RH_TN.W.1	Width of RH_TN (117;6)	W1	=	0.3600~1.8
RH_TN.W.2	Width of SR_DTN (117;7)	W2	=	0.1980~1.8
RH_TN.W.3	Width of SR_DMD (inside RH_TNB)	W3	=	0.0300
RH_TN.W.4	Width of SR_DPO (inside RH_TNB) (Except following conditions: 1. {Dummy_Cell NOT DC_7})	W4	=	0.0860
RH_TN.S.1	Space of {RH_TN OR SR_DTN} (RH_TN overlap SR_DTN is not allowed)	S1	\geq	0.1600
RH_TN.S.1.1	Space of {RH_TN OR SR_DTN} in length direction [PRL \geq 0 μm]	S1A	\geq	0.1700
RH_TN.S.2	Space of {RH_TN OR SR_DTN} to {VC OR MD} (Overlap is not allowed) (Except following conditions: 1. VC [width = 0.080 μm , INTERACT RH_TN] space to {RH_TN OR SR_DTN})	S2	\geq	0.3500
RH_TN.S.2.1	Space of RH_TN to SR_DMD (RH_TN overlap with SR_DMD is not allowed)	S2A	\geq	0.1150
RH_TN.S.2.2	Space of RH_TN to M0 [NOT INTERACT VC [width = 0.080 μm]] (RH_TN interact M0 [NOT INTERACT VC [width = 0.080 μm]] is not allowed)	S2B	\geq	0.1080
RH_TN.S.5	Space of {RH_TN OR SR_DTN} to VC [width = 0.080 μm] (SR_DTN overlap VC is not allowed)	S5	\geq	0.1000
RH_TN.S.6.1	Space to ALL_OD (Overlap OD is not allowed)	S6A	\geq	0.0700
RH_TN.S.6.2	Space of SR_DTN to OD (SR_DTN overlap OD is not allowed)	S6B	\geq	0.0700
RH_TN.S.7.1	Space to {ALL_PO OR ALL_MD} (Overlap {PO OR ALL_MD} is not allowed)	S7A	\geq	0.0700
RH_TN.S.7.2	Space of SR_DTN to {PO OR MD} (SR_DTN overlap {PO OR MD} is not allowed)	S7B	\geq	0.0700
RH_TN.S.8	Space of RH_TNB to ALL_OD (Overlap OD, cut SR_DOD is not allowed)	S8	\geq	0.0650
RH_TN.S.10	Space of RH_TNB	S10	\geq	0.2880
RH_TN.S.11	Space of VC [width = 0.080 μm] line-end to line-end	S11	\geq	0.1320
RH_TN.S.11.1	Space of VC [width = 0.080 μm] run to run	S11A	\geq	0.1500
RH_TN.EX.1	VC [width = 0.080 μm] extension on RH_TN in width direction at both sides (Extension \leq 0 μm is not allowed)	EX1	=	0.0140
RH_TN.EX.2	RH_TN extension on VC [width = 0.080 μm] in RH_TN length direction (Extension \leq 0 μm is not allowed)	EX2	\geq	0.0650
RH_TN.EN.1	RH_TNB enclosure of {{SR_DOD OR SR_DTN} OR RH_TN}	EN1	\geq	0.0650
RH_TN.EN.2	RH_TN enclosure of SR_DOD in horizontal direction (SR_DOD cut RH_TN is not allowed)	EN2	=	0.0240~0.1135
RH_TN.L.1	Length of RH_TN, SR_DTN	L1	\geq	0.6500
RH_TN.L.1.1	Length of high R resistor ({RH_TN AND RPDMY_ALL})	L1A	\geq	0.3600
RH_TN.L.2	Maximum Length of high R resistor ({RH_TN AND RPDMY_ALL}) Warning: To avoid PO.A.4 violation from a high R resistor with large width (e.g. W \geq 1.060 μm), recommend to use the shorter length (e.g. L < 15.2)	L2	\leq	25

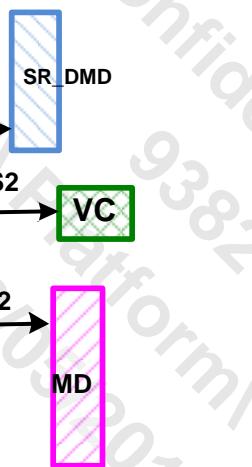
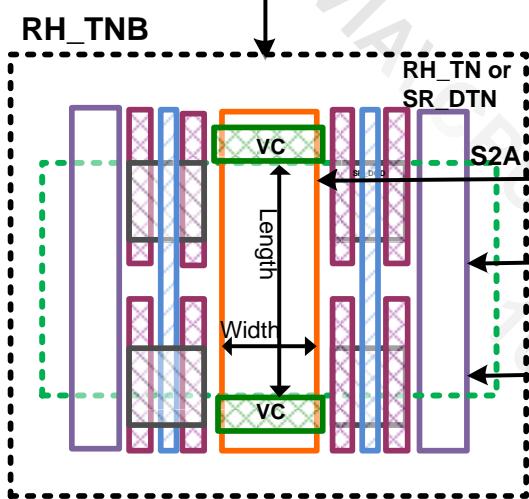
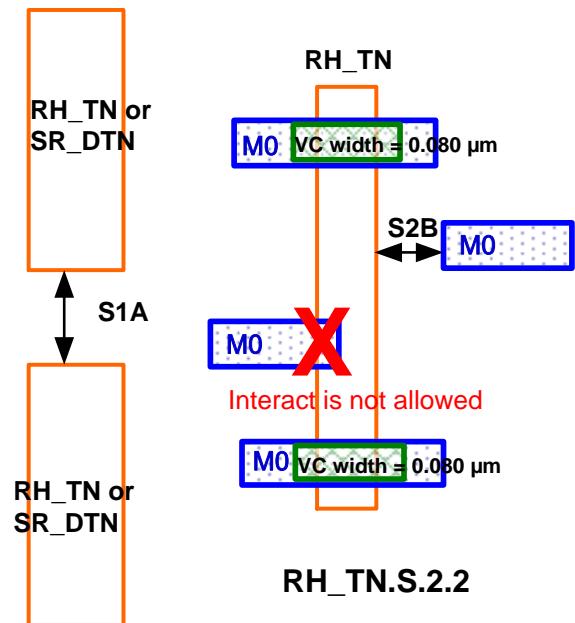
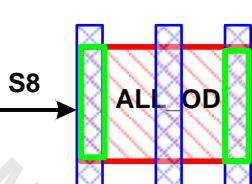
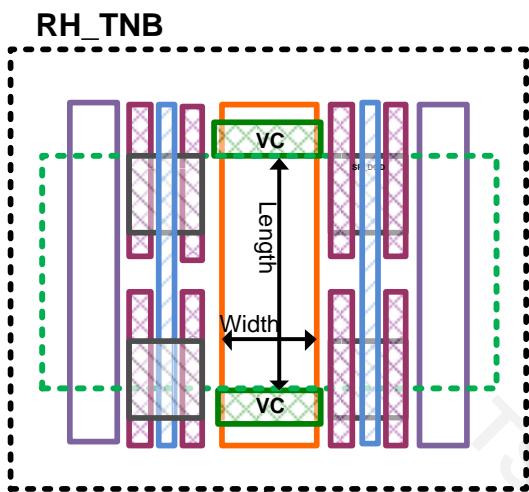
Rule No.	Description	Label	Op.	Rule
	μm) of a high R resistor			
RH_TN.A.1	Area of RH_TN, SR_DTN	A1	≥	0.12870
RH_TN.R.1	Square number (length/width) of high R resistor must be ≥ 1 (Except following conditions: 1. RPDMY (117;4) for non-precision usage)			
RH_TN.R.2	SR_DTN must be placed 2-side beside high R resistor (DRC flags no SR_DTN or other high R resistor within 2.2 μm in width direction and the number of SR_DTN [INTERACT RH_TNB] < 2)			
RH_TN.R.3	{RH_TN OR SR_DTN} OR RPDMY_ALL {INTERACT RH_TN} must be a rectangle orthogonal to grid			
RH_TN.R.4	RH_TN must interact VC [width = 0.080 μm]			
RH_TN.R.4.1	RH_TN must interact SR_DPO [width = 0.086 μm], SR_DOD			
RH_TN.R.4.2	VC [width = 0.080 μm] must interact RH_TN (Except SEALRING_ALL)			
RH_TN.R.5	RPDMY_ALL must abut VC [width = 0.080 μm] edge, RPDMY_ALL must interact 2 SR_DTN			
RH_TN.R.6	RPDMY_ALL intersecting RH_TN must form two or more RH_TNs			
RH_TN.R.7	RH_TN must be covered by RH_TNB, and must be uni-direction in the same RH_TNB			
RH_TN.R.8	RH_TNB must interact RH_TN			
RH_TN.R.10	Maximum delta V > 3.63V is not allowed. DRC searching range of 1. {{RH_TN NOT RPDMY_ALL} OR SR_DTN} space to {{RH_TN NOT RPDMY_ALL} OR SR_DTN} is < 1.5 μm; 2. {{RH_TN NOT RPDMY_ALL} space to {{RH_TN NOT RPDMY_ALL} OR SR_DTN} at length direction is < 1.7 μm; 3. {{RH_TN NOT RPDMY_ALL} OR SR_DTN} space to {ALL_MP OR {ALL_MD NOT ALL_CMD}} is < 3.5 μm; 4. {{RH_TN NOT RPDMY_ALL} space to ALL_OD is < 0.390 μm; 5. {{RH_TN NOT RPDMY_ALL} space to {ALL_PO NOT ALL_CPO} is < 0.700 μm			
RH_TN.R.11	{RPDMY_ALL AND RH_TN} overlap VC is not allowed			
RH_TN.R.12	RH_TN overlap DNW, PO, ALL_CPO, ALL_MD, ALL_CMD, ALL_MP is not allowed			
RH_TN.R.13	RH_TNB must be fully covered by NW and OD_18			
RH_TN.R.13.1	NW [INTERACT RH_TNB] must be drawn identically to RH_TNB (Except RPDMY_2)			
RH_TN.R.14	RPDMY_1, RPDMY_2 interact each other or same RH_TNB is not allowed			
RH_TN.DN.2	Maximum {RH_TN OR SR_DTN} density inside Chip_Boundary if Chip_Boundary has RH_TN in chip level		≤	30%
RH_TN.DN.4	Maximum {RH_TN OR SR_DTN} density in window 20 μm x 20 μm has RH_TN, stepping 10 μm		≤	50%

High R Resistor

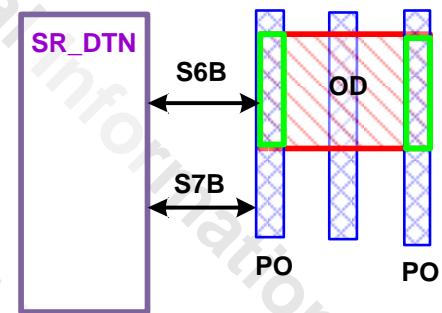
Width direction →
Length direction ↓



RH_TN.W.1 / RH_TN.W.2 / RH_TN.W.3 / RH_TN.W.4 / RH_TN.S.1 / RH_TN.S.2.1 /
 RH_TN.S.5 / RH_TN.S.6.1 / RH_TN.S.7.1 / RH_TN.EX.1 / RH_TN.EX.2 /
 RH_TN.EN.1 / RH_TN.EN.2 / RH_TN.L.1 / RH_TN.L.1.1 / RH_TN.L.2 / RH_TN.R.4.1

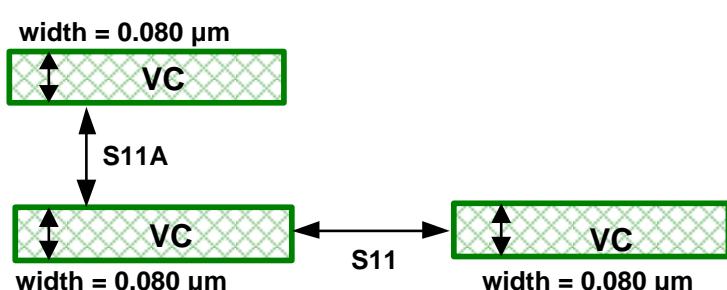


RH_TN.S.1.1

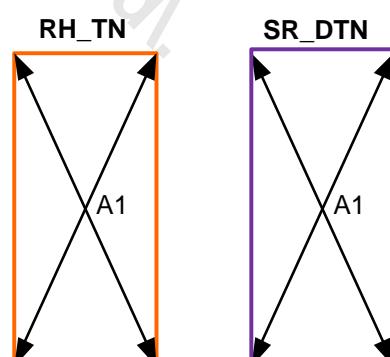


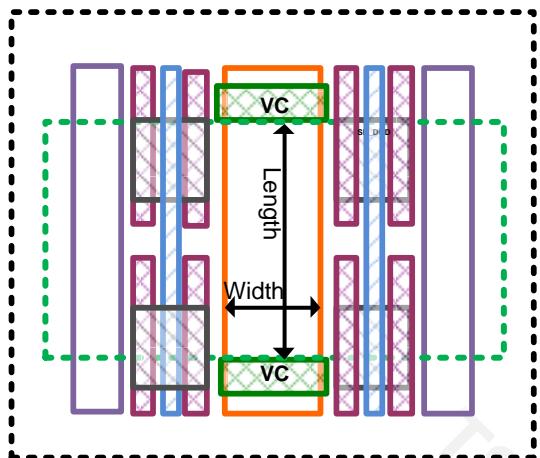
RH_TN.S.6.2 / RH_TN.S.7.2

RH_TN.S.2 / RH_TN.S.2.1
RH_TN.S.8 / RH_TN.S.10



RH_TN.S.11/ RH_TN.S.11.1

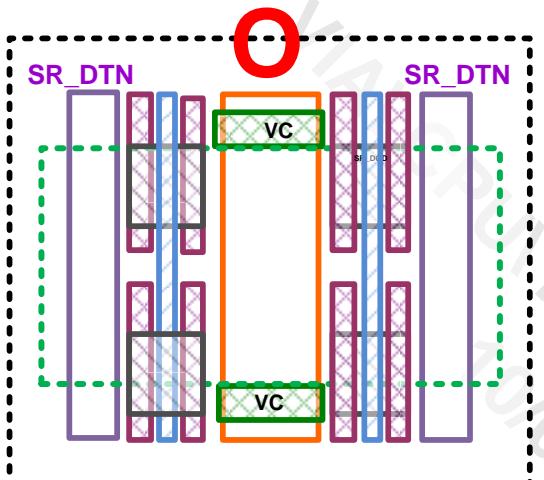




$\frac{\text{Length}}{\text{Width}}$ must be ≥ 1

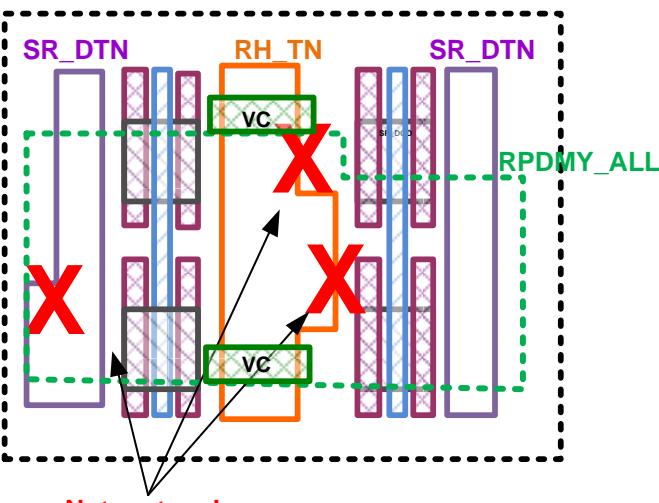
Square number (length/width) of high R resistor must be ≥ 1

RH_TN.R.1

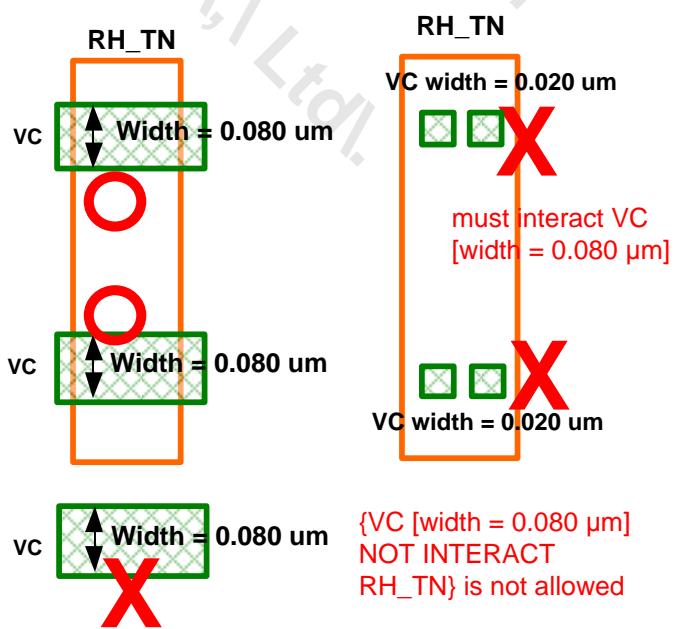


SR_DTN must be placed 2-side beside high R resistor

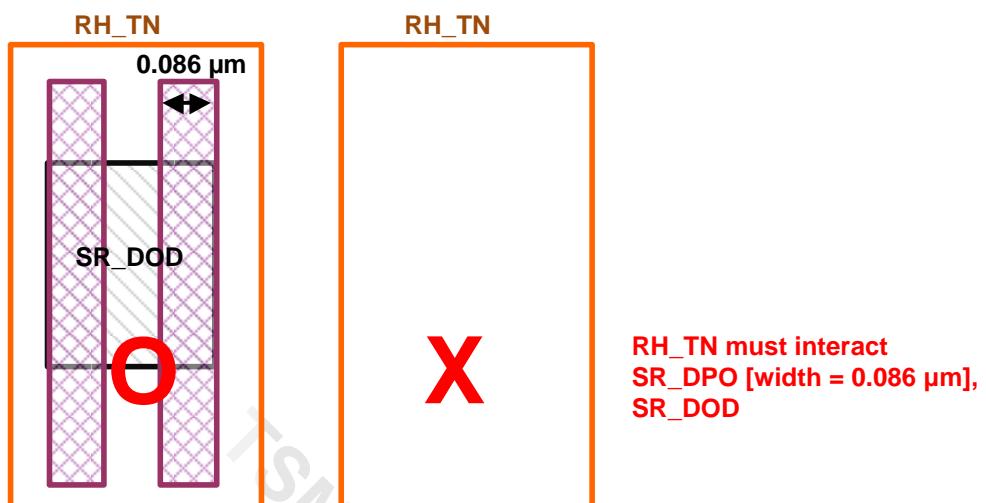
RH_TN.R.2



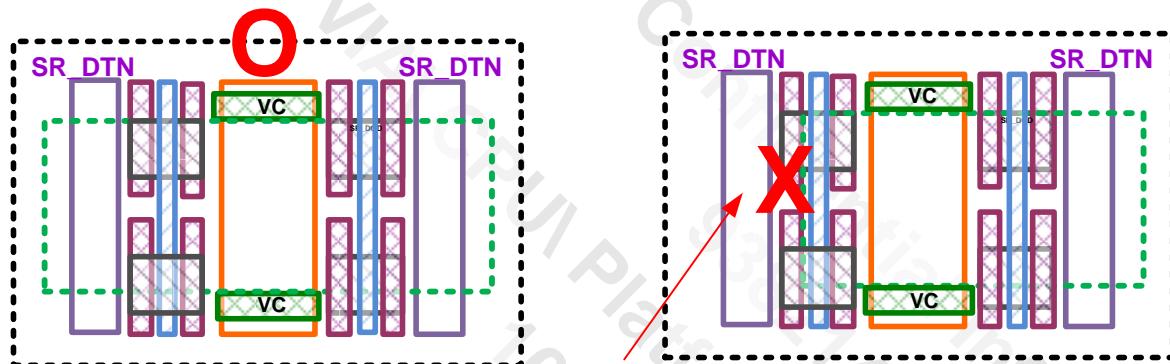
RH_TN.R.3



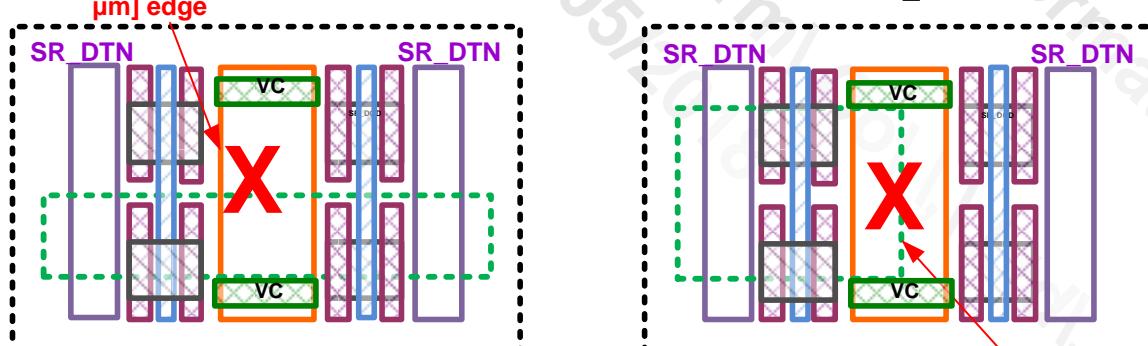
RH_TN.R.4 / RH_TN.R.4.2



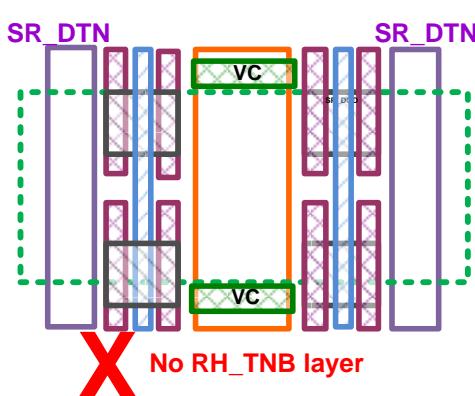
RH_TN.R.4.1



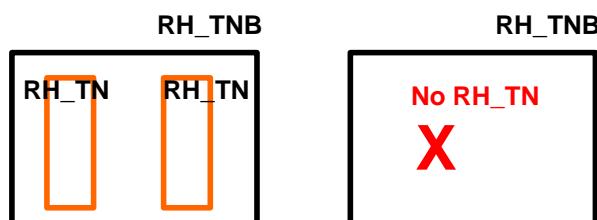
RH_TN.R.5



RH_TN.R.6

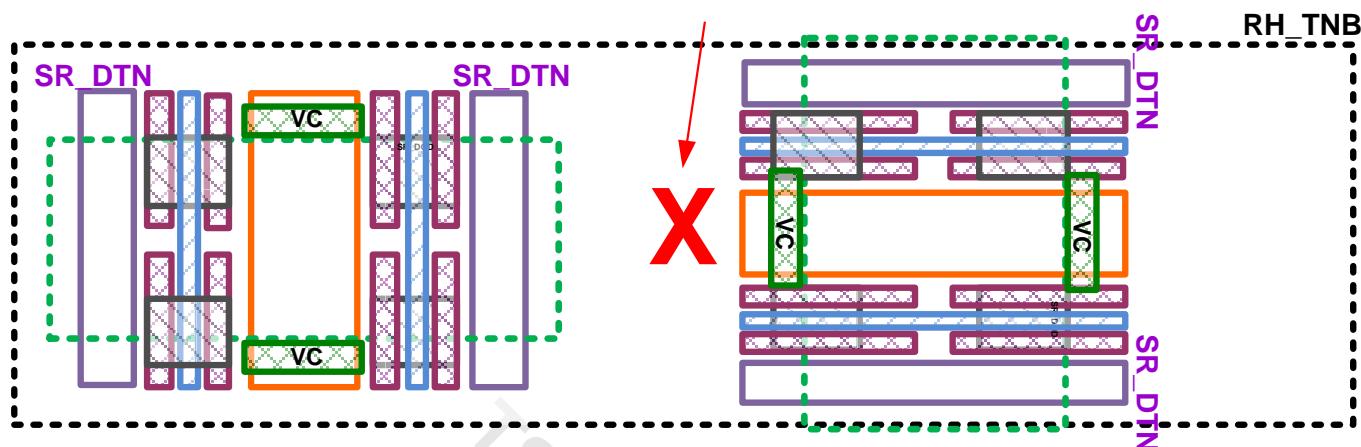


RH_TN.R.7



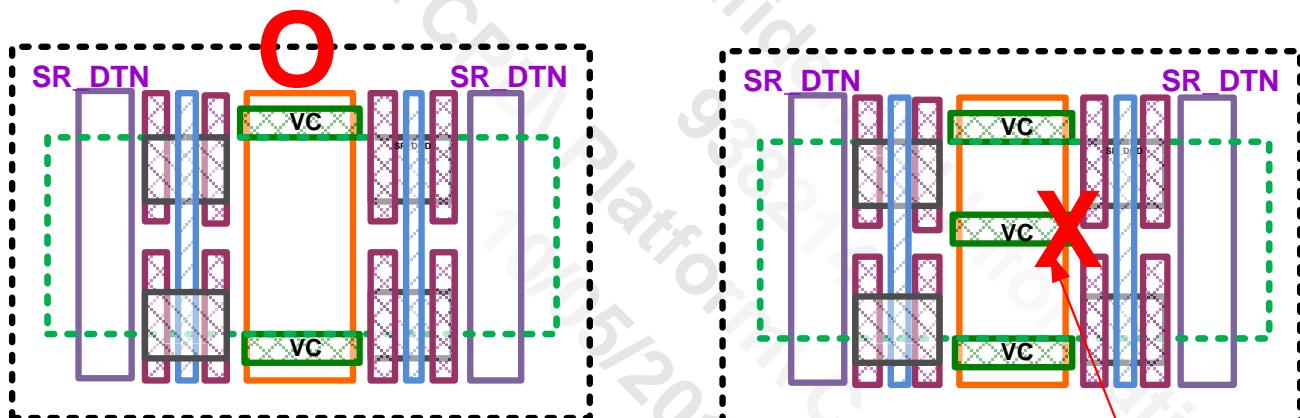
RH_TN.R.8

RH_TN are not same direction



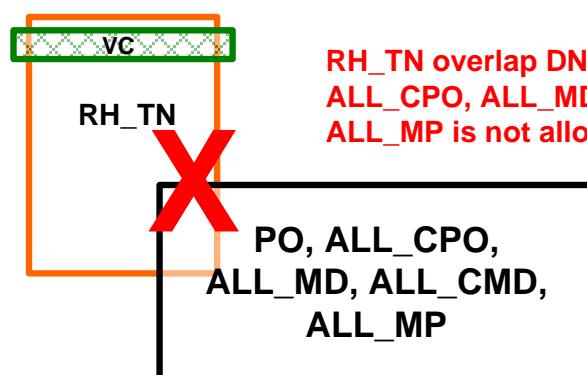
RH_TN must be uni-direction in the same RH_TNB

RH_TN.R.7

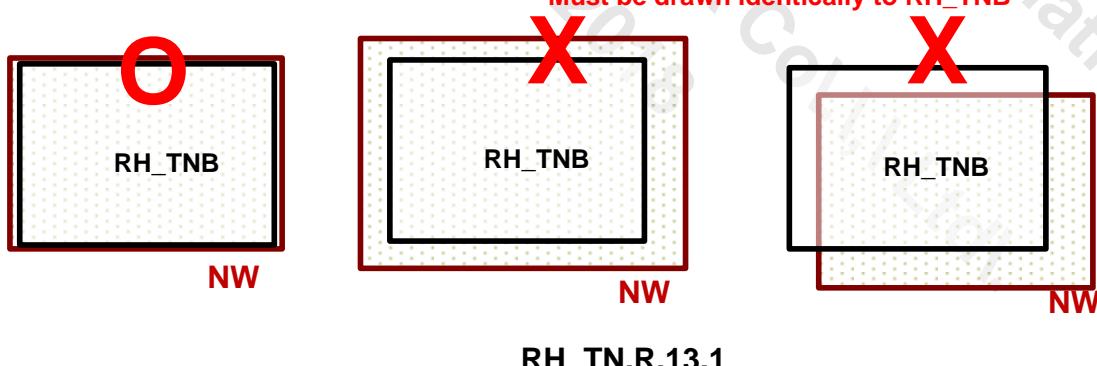
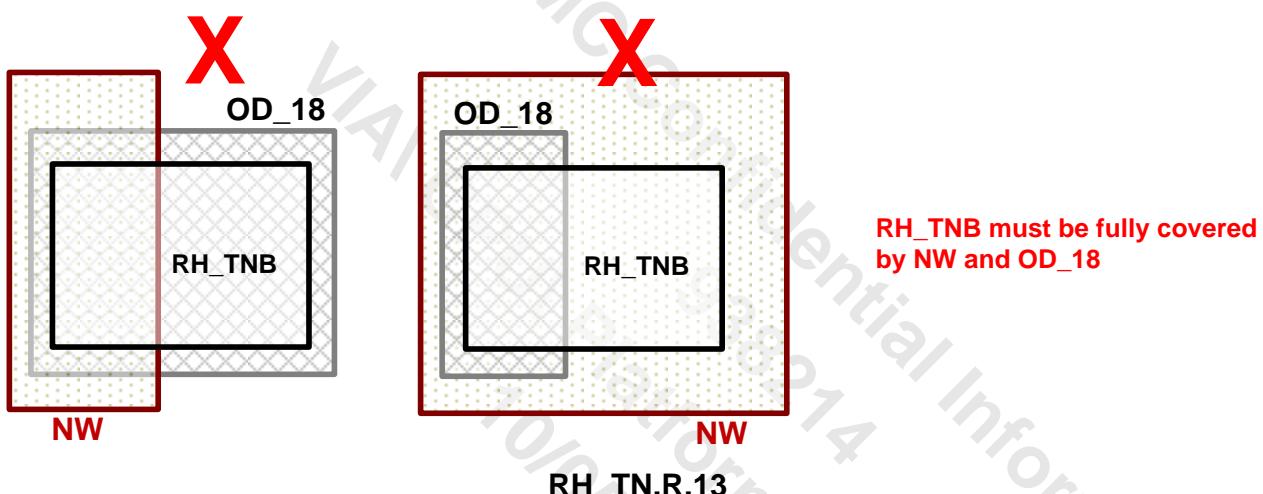
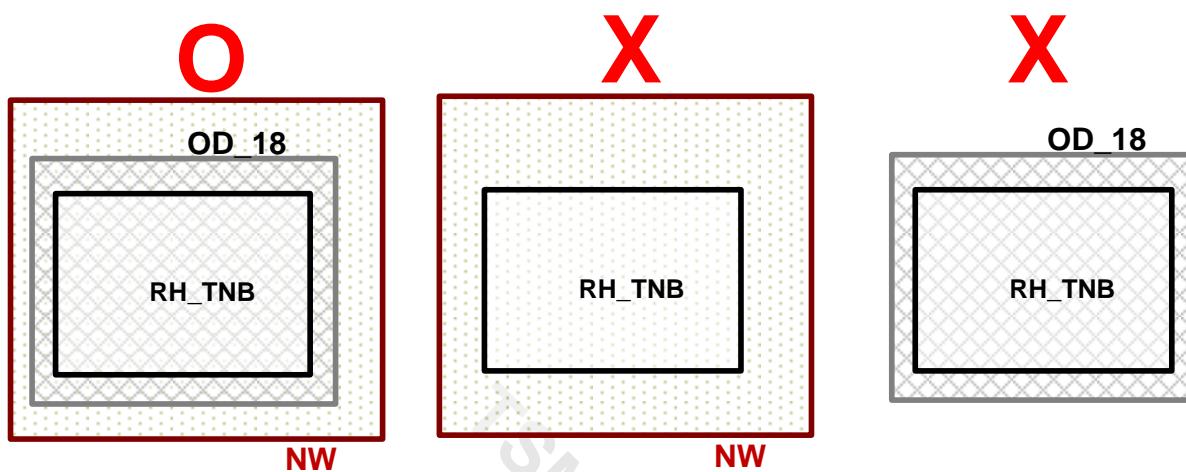


{RPDMY_ALL AND RH_TN}
[Overlap VC] is not allowed

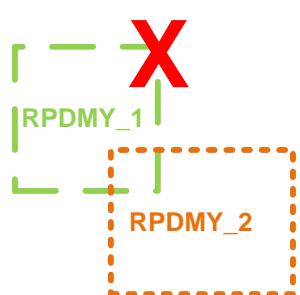
RH_TN.R.11



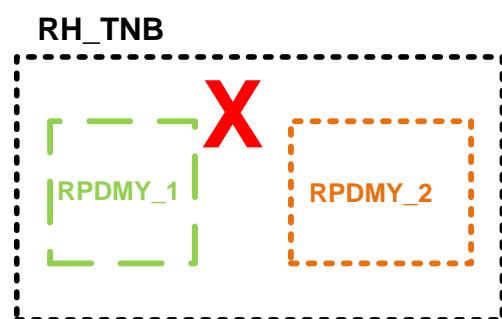
RH_TN.R.12



Interact each other is not allowed



Interact same **RH_TNB** is not allowed



RH_TN.R.14

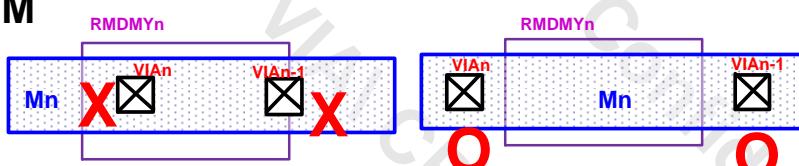
4.5.31 Metal Resistor (RM) Layout Rules

RMDMYn ($n=1\sim 15$) and RMDMYAP are used to define metal resistor and AP resistor for DRC/LVS device recognition.

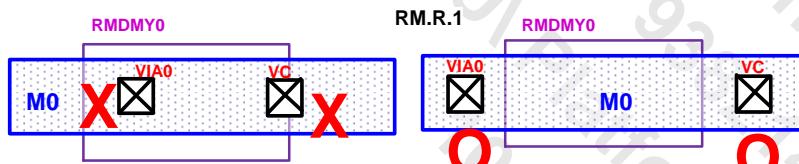
The connection of these nets will not be recognized as broken during DRC checks.

Rule No.	Description	Label	Op.	Rule
RM.R.1	{VIA n OR VIA $n-1$ } [Overlap {RMDMYn AND Mn}] is not allowed. ($n = 1\sim 15$)			
RM.R.1.1	{VIA0 OR VC} [Overlap {RMDMY0 AND M0}] is not allowed			
RM.R.2	RV [Overlap {{RMDMYAP AND AP} OR {RMDMYtop AND Mtop}}] is not allowed			
RM.R.3	RMDMYn intersecting Mn must form two or more Mns ($n = 1\sim 15$)			
RM.R.3.1	RMDMY0 intersecting M0 must form two or more M0s			
RM.R.4	RMDMYAP intersecting AP must form two or more APs			

RM

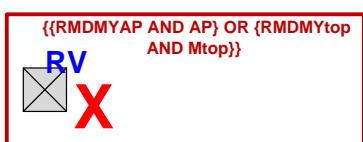


{VIA n OR VIA $n-1$ } [Overlap {RMDMYn AND Mn}] is not allowed. ($n = 1\sim 14$)



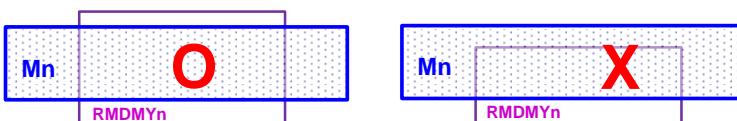
{VIA0 OR VC} [Overlap {RMDMY0 AND M0}] is not allowed

RM.R.1.1



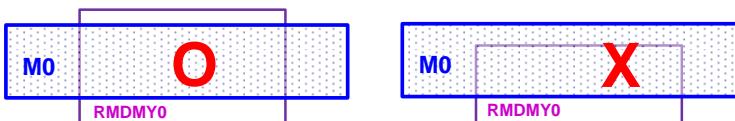
RV [Overlap {{RMDMYAP AND AP} OR {RMDMYtop AND Mtop}}] is not allowed

RM.R.2



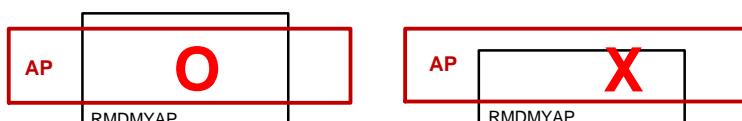
RMDMYn intersecting Mn must form two or more Mns

RM.R.3



RMDMY0 intersecting M0 must form two or more M0s

RM.R.3.1



RMDMYAP intersecting AP must form two or more APs

RM.R.4

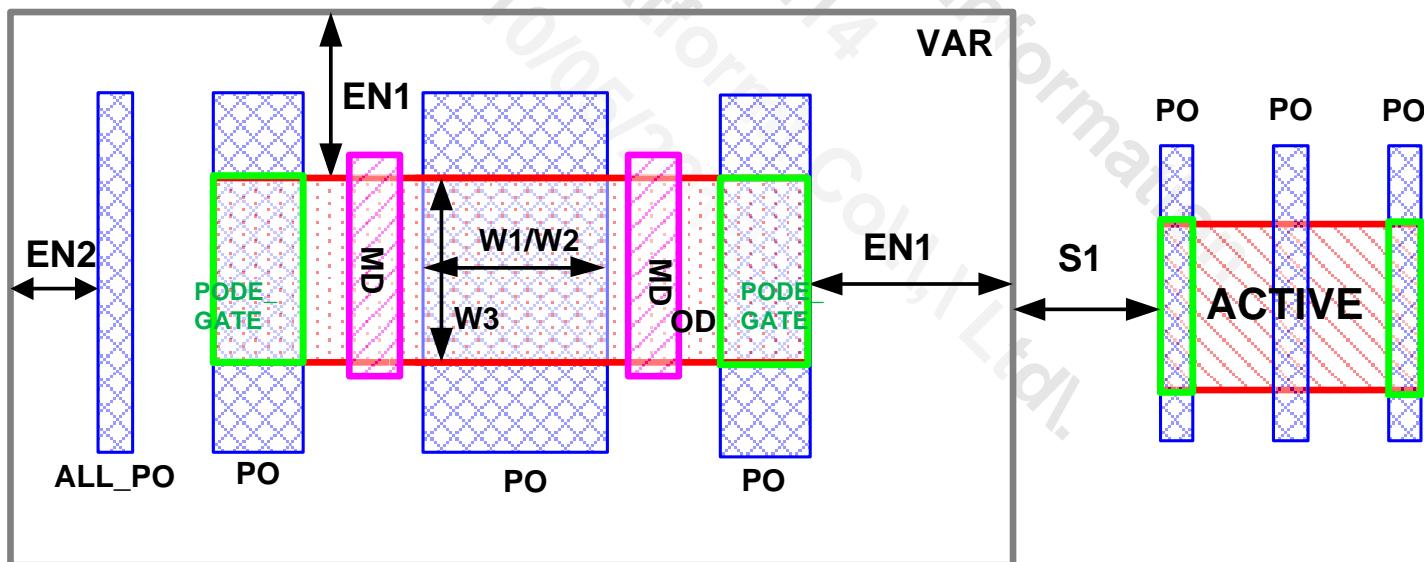
4.5.32 MOS Varactor Layout Rules (VAR)

NVAR: NMOS in NW.

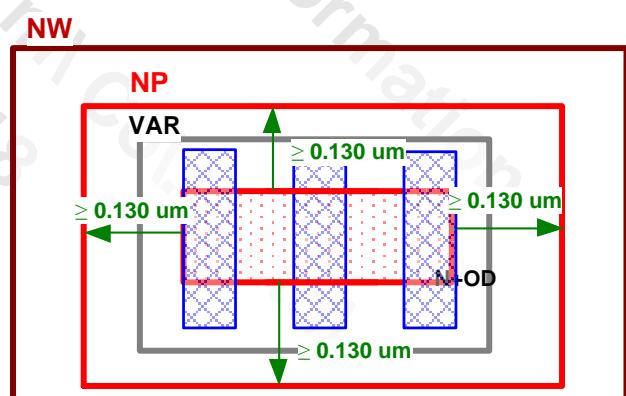
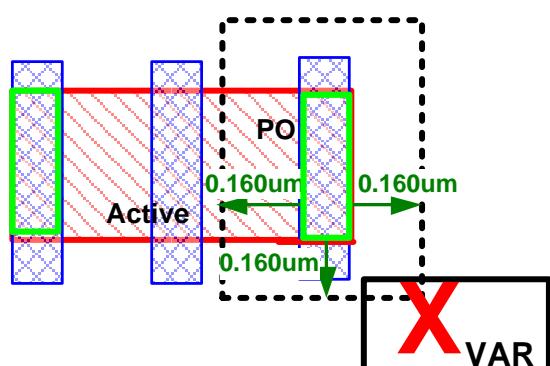
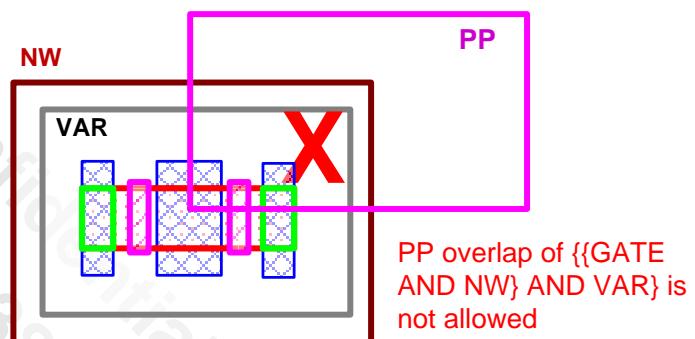
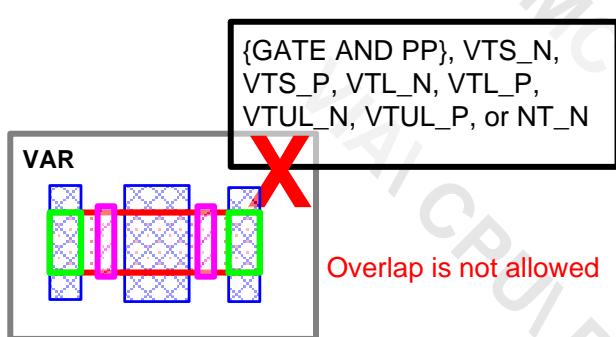
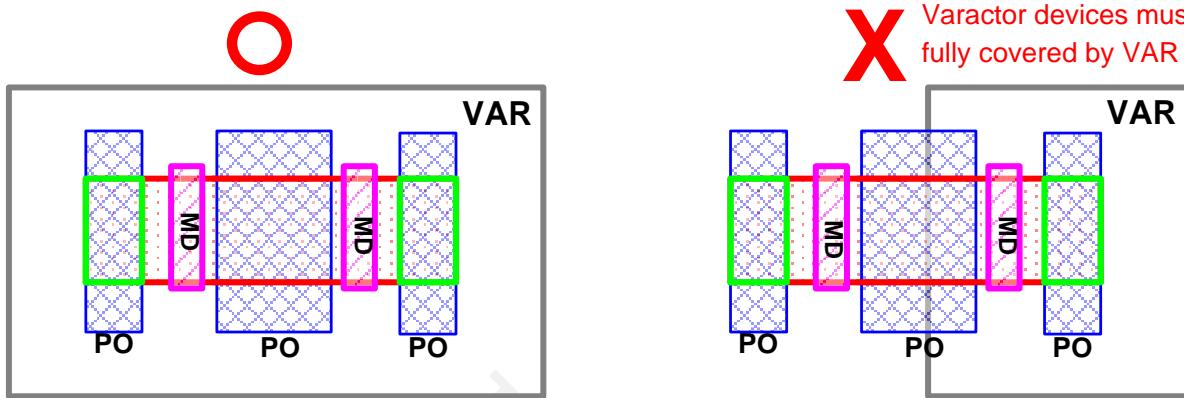
VAR: Customer must provide this layer (CAD layer: 143) to generate LDD logical operation, if the MOS varactor is used.

Rule No.	Description	Label	Op.	Rule
VAR.W.1	Channel length of {{TrGATE NOT OD2} AND VAR}	W1	=	0.0720~0.2400
VAR.W.2	Channel length of {{TrGATE AND OD2} AND VAR}	W2	=	0.1350~0.2400
VAR.W.3	Channel width of {GATE AND VAR}	W3	\geq	0.2180
VAR.S.1	Space to ACTIVE	S1	\geq	0.1170
VAR.EN.1	Enclosure of OD	EN1	\geq	0.1440
VAR.EN.2	Enclosure of ALL_PO (Except Dummy_Cell)	EN2	\geq	0.0350
VAR.R.1	Varactor devices must be fully covered by VAR layer			
VAR.R.2	Overlap {GATE AND PP}, VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P, or NT_N is not allowed			
VAR.R.3	PP overlap {{GATE AND NW} AND VAR} is not allowed			
VAR.R.4	Overlap {{PO AND ACTIVE} SIZING 0.160 μ m} is not allowed			
VAR.R.5	NP must fully cover {{{{VAR AND GATE} AND NW} SIZING 0.190 μ m} AND OD} SIZING 0.130 μ m}			

VAR



VAR.W.1 / VAR.W.2 / VAR.W.3 / VAR.S.1 / VAR.EN.1/ VAR.EN.2



4.5.33 MD Layout Rules

MD (CAD layer: 84;0) can be used as an interconnection layer between OD and VC.

ALL_MD = {MD OR SR_DMD}

Rule No.	Description	Label	Op.	Rule
MD.W.1	Width of ALL_MD in horizontal direction (Except SEALRING_ALL)	W1	=	0.0240, 0.0300
MD.W.1.1	Width of ALL_MD in horizontal direction [INSIDE PO_P76]	W1	=	0.0300
MD.W.2	Width of ALL_MD [INTERACT {ALL_OD INTERACT ALL_PO [width ≥ 0.020 μm]}]	W2	=	0.0300
MD.W.2.1	Width of ALL_MD [space to ALL_PO [width ≥ 0.020 μm] ≤ 0.037 μm]	W2A	=	0.0300
MD.S.1	Space of ALL_MD (SR_DMD overlap MD is not allowed)	S1	≥	0.0330
MD.S.1.1	Space of short side of ALL_MD [width = 0.024 μm, PRL > -0.030 μm]	S1A	≥	0.0960
MD.S.1.2	Space of long side of ALL_MD [width = 0.024 μm, PRL > -0.096 μm]	S1B	≥	0.0330
MD.S.2	Space of short side of ALL_MD [width = 0.030 μm] to ALL_MD [PRL > -0.070 μm] (EXCEPT PO_P76)	S2	≥	0.0860
MD.S.2.0.1	Space of short side of ALL_MD [width = 0.030 μm] to ALL_MD [PRL > -0.046 μm] [INSIDE PO_P76]	S2	≥	0.0860
MD.S.2.1	Space of long side of ALL_MD [width = 0.030 μm] to ALL_MD [PRL > -0.086 μm] (Except PO_P76)	S2A	≥	0.0700
MD.S.2.2	Space of long side of ALL_MD [width = 0.030 μm] to ALL_MD [PRL > -0.086 μm] [INSIDE PO_P76]	S2A	≥	0.0460
MD.S.6.1	Space of ALL_MD to ALL_PO	S6	≥	0.0110
MD.S.6.2	Space of ALL_MD to ALL_PO [width = 0.008/0.011 μm]	S6	≥	0.0110
MD.S.6.3	Space of ALL_MD to ALL_PO [width = 0.008/0.011 μm] [INSIDE PO_P76]	S6C	≥	0.0175
MD.S.6.4	Space of ALL_MD to ALL_PO [width = 0.020/0.036 μm]	S6	≥	0.0250
MD.S.6.5	Space of ALL_MD to ALL_PO [width ≥ 0.072 μm]	S6	≥	0.0320
MD.S.6.6	Space of ALL_MD to ALL_PO [width = 0.008 μm, centerline space = 0.057 μm] (Except following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	S6	≥	0.0125
MD.S.6.7	Space of ALL_MD to ALL_PO [width = 0.008 μm, centerline space = 0.076 μm] (Except following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	S6G	≥	0.0190
MD.S.7	Space of both long side of {ALL_MD [width = 0.024 μm] NOT ALL_CMD} to ALL_PO (Except PO_P63)	S7	≤	0.0125
MD.S.7.0.1	Space of both long side of {ALL_MD [width = 0.024 μm] NOT ALL_CMD} to ALL_PO [INSIDE PO_P63]	S7	≤	0.0155
MD.S.7.0.2	Space of both long side of {ALL_MD [width = 0.030 μm] NOT ALL_CMD} to ALL_PO [INSIDE PO_P76]	S7	≤	0.0190
MD.S.7.1	Space of ALL_MD to ALL_PO [INSIDE PO_P63]	S7	≥	0.0140
MD.S.7.2	Space of ALL_MD [width = 0.030 μm] to ALL_PO (Except PO_P76)	S7B	≥	0.0250
MD.S.7.2.1	Space of ALL_MD [width = 0.030 μm] to ALL_PO [INSIDE PO_P76]	S7B	≥	0.0175
MD.S.7.3	Space of {ALL_MD [width = 0.030 μm] NOT ALL_CMD} to {ALL_PO NOT CPO} [one side poly space > 0.080 μm in horizontal direction, width ≤ 0.036 μm] in horizontal direction	S7C	≥	0.0360

Rule No.	Description	Label	Op.	Rule
MD.S.7.3.1	Space of {ALL_MD [width = 0.030 μm] NOT ALL_CMD} to {ALL_PO NOT CPO} [one side poly space ≥ 0.120 μm in horizontal direction, width ≥ 0.072 μm] in horizontal direction	S7C1	≥	0.0420
MD.S.7.4	Space of FIELD {ALL_PO NOT CPO} to ALL_MD [FIELD {ALL_PO NOT CPO} width < 0.096 μm, one side space to {{GATE [INSIDE OD2] SIZING 0.060 μm} AND PO} = 0.094 μm in horizontal direction, the other side space to {ALL_PO NOT CPO} ≥ 0.150 μm in horizontal direction] in horizontal direction (Except following conditions: 1. the regions of only one MD space to SR_DPO < 0.055 μm, 2. SR_DPO space to SR_DMD)	S7D	≥	0.0550
MD.S.7.5	Space of short side of ALL_MD to ALL_PO (Except following conditions: 1. small ALL_PO jog ≤ 0.002 μm)	S7E	≥	0.0470
MD.S.7.6	Space of ALL_MD to short side of ALL_PO [width < 0.226 μm] (Except following conditions: 1. ALL_PO jog ≤ 0.002 μm)	S7F	≥	0.0470
MD.S.8.1	Space of ALL_MD to ALL_OD (SR_DMD overlap OD is not allowed, MD overlap SR_DOD is not allowed)	S8A	≥	0.0110
MD.S.8.1.1	Space of ALL_MD to ALL_OD [INSIDE PO_P63]	S8A	≥	0.0140
MD.S.8.1.2	Space of ALL_MD to ALL_OD [INSIDE PO_P76]	S8A	≥	0.0175
MD.S.8.2	Space of short side of ALL_MD [short side NOT INTERACT CMD] to ALL_OD in vertical direction [PRL > -0.030 μm] (Except FB_8, BLK_WF)	S8B	≥	0.0960
MD.S.20	Space of ALL_MD to SRM (50;0) (Cut is not allowed)	S20	≥	0.1120
MD.S.20.1	Space of ALL_MD [width = 0.030 μm] to SRM (50;0) [PRL > -0.144 μm] in horizontal direction ({ALL_MD CUT SRM (50;0)} is not allowed)	S20	≥	0.1500
MD.S.20.2	Space of ALL_MD [width = 0.024 μm] to SRM (50;0) [PRL > -0.112 μm] in vertical direction ({ALL_MD CUT SRM (50;0)} is not allowed)	S20B	≥	0.1440
MD.S.20.3	Space of ALL_MD [width = 0.030 μm] to SRM (50;0) [PRL > -0.150 μm] in vertical direction	S20B	≥	0.1440
MD.S.21.1	Space of {ALL_MD NOT ALL_CMD} to ALL_OD [maximum delta V > 0.96V]	S21	≥	0.0320
MD.S.21.3	Space of {ALL_MD NOT ALL_CMD} to ALL_OD [maximum delta V > 1.98V] (1.8V + 10%)	S21	≥	0.0490
MD.S.21.5	Space of {ALL_MD NOT ALL_CMD} to ALL_OD [maximum delta V > 2.75V] (2.5V + 10%)	S21	≥	0.0620
MD.S.22.1	Space of {ALL_MD NOT ALL_CMD} to {ALL_PO NOT CPO} [maximum delta V > 0.96V] (Except MetalFuse, or following conditions: 1. STRAP_With_Floating_PO [INSIDE MOMDMY]) Definition of STRAP_With_Floating_PO: {STRAP NOT INTERACT {ALL_PO NOT CPO} [INTERACT {MP OR ACTIVE}]}	S22	≥	0.0320
MD.S.22.2	Space of {ALL_MD NOT ALL_CMD} to {ALL_PO NOT CPO} [maximum delta V > 1.98V] (1.8V + 10%) (Except MetalFuse, or following conditions: 1. SR_DPO interact SDI_2) (Maximum delta V > 1.98V between MD and neighboring PO on same OD is not allowed)	S22	≥	0.0470
MD.S.22.5	Space of {ALL_MD NOT ALL_CMD} to {ALL_PO NOT CPO} [maximum delta V > 2.75V] (2.5V + 10%) (Except following conditions: 1. SR_DPO interact SDI_2) (Maximum delta V > 1.98V between MD and neighboring PO on same OD is not allowed)	S22	≥	0.0540

Rule No.	Description	Label	Op.	Rule
MD.S.23	MD [INTERACT OD] to 1st MD space rule: Space of Checked_MD to {ALL_MD NOT ALL_CMD} in horizontal direction (Except FB_9, FB_8, BLK_WF, PO_P63) Definition of Checked_MD: { {{MD [width = 0.024 μm] NOT CMD} AND OD [width < 0.188 μm]} SIZING 0.005 μm in vertical direction }	S23	=	0.0330
MD.S.23.1®	MD [INTERACT OD] to 2nd MD space rule: Space of Checked_MD to the second {ALL_MD NOT ALL_CMD} in horizontal direction (Except FB_9, FB_8, BLK_WF, PO_P63) Definition of Checked_MD: { {{MD [width = 0.024 μm] NOT CMD} AND OD [width < 0.188 μm]} SIZING 0.005 μm in vertical direction } (The second MD is required to be placed beside the MD [INTERACT OD])	S23A	=	0.0900
MD.S.24	MD [INTERACT OD] to 1st MD space rule: Space of Checked_MD to {ALL_MD NOT ALL_CMD} in horizontal direction [INSIDE PO_P63] (Except FB_9, FB_8, BLK_WF) Definition of Checked_MD follows MD.S.23	S24	=	0.0390
MD.S.24.1®	MD [INTERACT OD] to 2nd MD space rule: Space of Checked_MD to the second {ALL_MD NOT ALL_CMD} in horizontal direction [INSIDE PO_P63] (Except FB_9, FB_8, BLK_WF) Definition of Checked_MD follows MD.S.23 (The second MD is required to be placed beside the MD [INTERACT OD])	S23A	=	0.1020
MD.S.25	MD [INTERACT OD] to 1st MD space rule: Space of Checked_MD to {ALL_MD NOT ALL_CMD} in horizontal direction [INSIDE PO_P76] Definition of Checked_MD: { {{MD [width = 0.030 μm] NOT CMD} AND OD [width < 0.188 μm]} SIZING 0.005 μm in vertical direction }	S25	=	0.0460
MD.S.25.1®	MD [INTERACT OD] to 2nd MD space rule: Space of Checked_MD to the second {ALL_MD NOT ALL_CMD} in horizontal direction [INSIDE PO_P76] Definition of Checked_MD follows MD.S.25(The second MD is required to be placed beside the MD [INTERACT OD])	S25A	=	0.1220
MD.S.26	Space of ALL_MD [width = 0.030 μm, INSIDE PO_P76] to ALL_MD [NOT INSIDE PO_P76, PRL > -0.096 μm] in horizontal direction	S26	≥	0.1500
MD.S.26.1	Space of ALL_MD [width = 0.030 μm, INSIDE PO_P76] to ALL_MD [NOT INSIDE PO_P76, PRL > -0.150 μm] in vertical direction	S26A	≥	0.0960
MD.EX.1	ALL_OD extension on ALL_MD in horizontal direction (Extension ≤ 0 μm is not allowed) (Except BLK_WF)	EX1	≥	0.0205
MD.EX.1.1	ALL_OD extension on ALL_MD in horizontal direction [INSIDE PO_P63] (Except BLK_WF)	EX1	≥	0.0235

Rule No.	Description	Label	Op.	Rule
MD.EX.1.2	ALL_OD extension on ALL_MD in horizontal direction [INSIDE PO_P76] (Except BLK_WF)	EX1	\geq	0.0270
MD.EX.4	ALL_OD [INTERACT ALL_PO [0.020 $\mu\text{m} \leq \text{width} \leq 0.036 \mu\text{m}]]] extension on ALL_MD in horizontal direction (Extension \leq 0 \mu\text{m} is not allowed, DRC flags ALL_MD within ALL_PO and ALL_OD edge)$	EX4	\geq	0.0450
MD.EX.4.1	ALL_OD [INTERACT ALL_PO [width $\geq 0.072 \mu\text{m}$ and OUTSIDE OD2]] extension on ALL_MD in horizontal direction (Extension $\leq 0 \mu\text{m}$ is not allowed)	EX4A	\geq	0.1040
MD.EX.5.1	{ALL_MD NOT ALL_CMD} extension on ALL_OD in vertical direction (Extension $< 0 \mu\text{m}$ is not allowed) (Except FB_9, FB_8)	EX5A	\geq	0.0050
MD.EX.5.2	{ALL_MD [width = 0.030 $\mu\text{m}]]$ NOT ALL_CMD} extension on ALL_OD in vertical direction (Extension $< 0 \mu\text{m}$ is not allowed)	EX5B	\geq	0.0150
MD.EX.5.3	{ALL_MD NOT rectangular ALL_CMD [length $\leq 0.057 \mu\text{m}]]$ extension on ALL_OD in vertical direction (Extension $< 0 \mu\text{m}$ is not allowed) (Except FB_9, FB_8)	EX5C	\geq	0.0070
MD.EX.5.3.1	{ALL_MD NOT rectangular ALL_CMD [length $\leq 0.063 \mu\text{m}]]$ extension on ALL_OD in vertical direction [INSIDE PO_P63] (Extension $< 0 \mu\text{m}$ is not allowed) (Except FB_9, FB_8)	EX5C	\geq	0.0070
MD.EX.5.4	ALL_MD [short side NOT INTERACT ALL_CMD] extension on ALL_OD in vertical direction (Extension $< 0 \mu\text{m}$ is not allowed)	EX5D	\geq	0.0100
MD.EX.7	ALL_PO extension on projected edge of neighboring short side of {ALL_MD [width = 0.024 $\mu\text{m}]]$ NOT ALL_CMD} in vertical direction (Extension $< 0 \mu\text{m}$ is not allowed)	EX7	\geq	0
MD.EX.7.1	ALL_PO extension on projected edge of neighboring short side of {ALL_MD [width = 0.030 $\mu\text{m}]]$ NOT ALL_CMD} in vertical direction [INSIDE PO_P76] (Extension $< 0 \mu\text{m}$ is not allowed)	EX7	\geq	0
MD.L.1	Length of {ALL_MD [width = 0.024 $\mu\text{m}]]$ NOT ALL_CMD} in vertical direction (Except BLK_WF, Dummy_Cell, SEALRING_ALL, or following conditions: 1. {ALL_MD [INTERACT {HEADER_9 OR HEADER_8}]}))	L1	=	0.0420 ~ 0.6420
MD.L.1.1	Length of ALL_MD [width = 0.024 $\mu\text{m}]]$ in vertical direction (Except Dummy_Cell, FB_9)	L1A	\geq	0.1300
MD.L.2	Length of {ALL_MD [width = 0.030 $\mu\text{m}]]$ NOT ALL_CMD} in vertical direction (Except Dummy_Cell)	L2	=	0.1300 ~ 0.7300
MD.L.2.1	Length of ALL_MD [width = 0.030 $\mu\text{m}]]$ in vertical direction (Except Dummy_Cell)	L2A	\geq	0.1300
MD.A.1	Area of ALL_MD	A1	\geq	0.00240
MD.A.2	Area of {ALL_MD NOT ALL_CMD}	A2	\geq	0.00100
MD.DN.1	Minimum {ALL_MD NOT {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}} density in window 125 $\mu\text{m} \times 125 \mu\text{m}$, stepping 62.5 μm (Except NWDMY, LOGO, TCDDMY, ICOVL_SINGLE, RH_TNB, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	5%

Rule No.	Description	Label	Op.	Rule
MD.DN.1.1	Minimum {ALL_MD NOT {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}} density in window 20 μm x 20 μm has GATE, stepping 10 μm (Except NWDMDY, LOGO, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
MD.DN.2	Maximum {ALL_MD NOT {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}} density in window 20 μm x 20 μm, stepping 10 μm (Except TCDDMY, ICOVL_SINGLE)		≤	45%
MD.R.2	ALL_MD must be vertical direction (Except SEALRING_ALL)			
MD.R.5	ALL_MD [width = 0.024 μm] overlap {OD2 OR NWRSTI} is not allowed. (ALL_MD width must be = 0.030 μm) (Except Dummy_Cell)			
MD.R.6	ALL_MD must be a rectangle orthogonal to grid (Except SEALRING_ALL)			
MD.R.7	Only one ALL_MD [width = 0.024/0.030 μm] is allowed on individual S/D (Except SR_ESD)			
MD.R.8	ALL_MD overlap ALL_PO is not allowed			
MD.R.9	SR_DMD interact OD, MD, VC is not allowed (Except SEALRING_ALL, or following conditions: 1. {SR_DMD ABUT MD} INSIDE CMD)			
MD.R.10	MD overlap SR_DOD, SR_DMD, SR_DMP is not allowed			
MD.R.11	{OD INTERACT PO} NOT PO} must interact MD			
MD.R.11.1	{SR_DOD NOT ALL_PO} must interact SR_DMD (Except RH_TN)			
MD.R.12	ALL_MD [width = 0.024 μm and length ≤ 0.150 μm] must be coupled in one group with number of ALL_MD ≥ 10 (Except FB_9, SEALRING_ALL, PO_P63) DRC flags {ALL_MD SIZING up/down 0.052 μm in vertical direction} [length ≤ 0.150 μm, NOT INTERACT MD_Group] Definition of MD_Group: {{{ALL_MD [width = 0.024 μm] SIZING up/down 0.052 μm in vertical direction} SIZING up/down 0.0165 μm in horizontal direction} SIZING down/up 0.0225 μm in vertical direction} SIZING down/up 0.268 μm in horizontal direction}			
MD.R.12.1	ALL_MD [width = 0.024 μm and length ≤ 0.150 μm] must be coupled in one group with number of ALL_MD ≥ 10 [INSIDE PO_P63] (Except FB_9, SEALRING_ALL) DRC flags {ALL_MD SIZING up/down 0.052 μm in vertical direction} [length ≤ 0.150 μm, NOT INTERACT MD_Group_PO_P63, INSIDE PO_P63] Definition of MD_Group_PO_P63: {{{ALL_MD [width = 0.024 μm] SIZING up/down 0.052 μm in vertical direction} SIZING up/down 0.0195 μm in horizontal direction} SIZING down/up 0.0225 μm in vertical direction} SIZING down/up 0.295 μm in horizontal direction}			

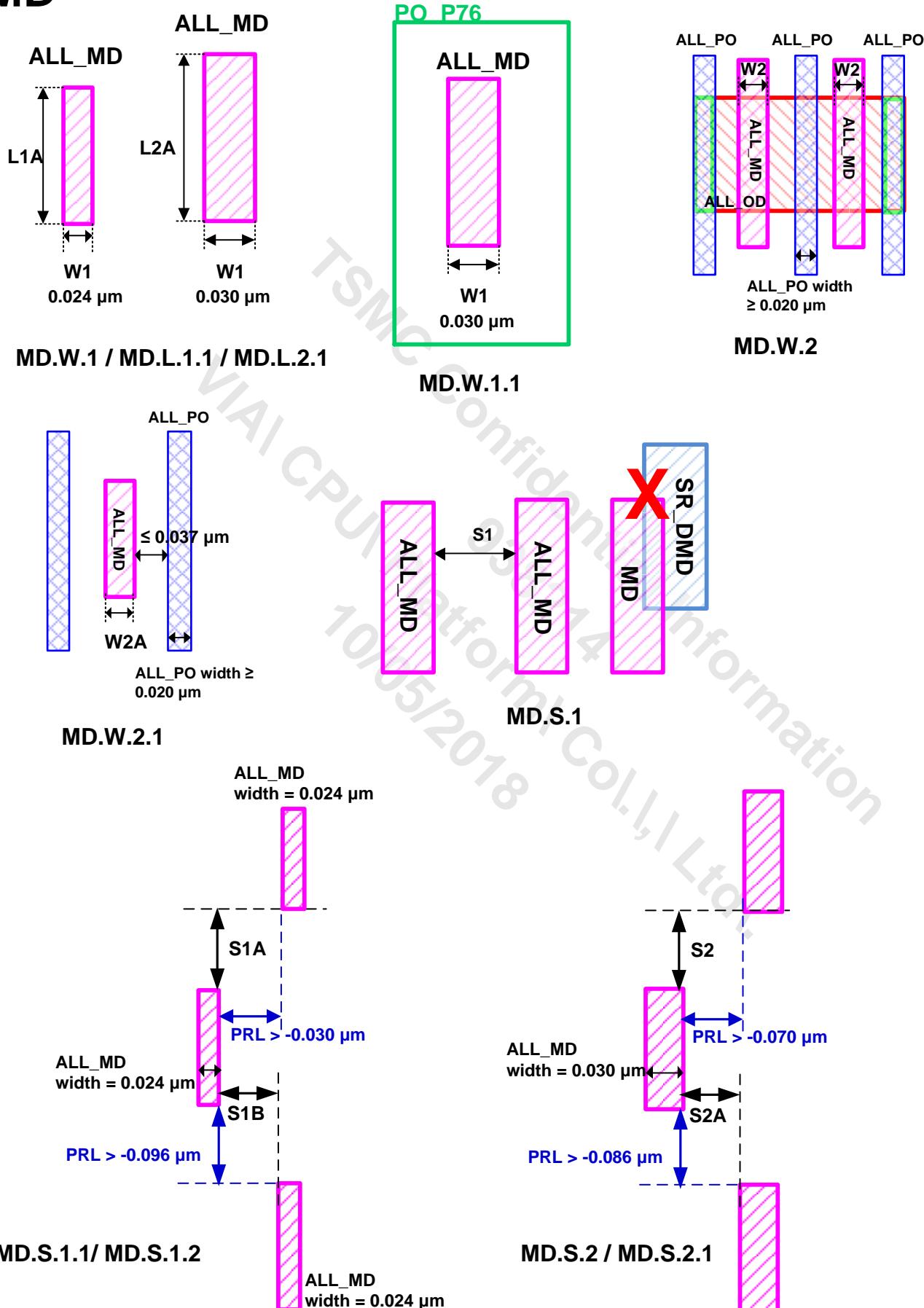
Rule No.	Description	Label	Op.	Rule
MD.R.13	<p>1st_STI_MD interact {{OD OR VC} OR MP} or space to 2 or more {Wide_OD OR ISO_Small_OD} $\leq 0.014 \mu\text{m}$ in horizontal direction [PRL > 0 μm] is not allowed (Except BLK_WF, SEALRING_ALL, PO_P63)</p> <p>STI_MD : {{{ALL_MD NOT Dummy_Cell} [width = 0.024 $\mu\text{m}】 NOT ALL_CMD [Derived from BCMD]} NOT ALL_OD}$</p> <p>Wide_OD : Length of ALL_OD vertical edge [between two consecutive 90-90 degree corners] $\geq 0.188 \mu\text{m}$</p> <p>Small_OD : Length of ALL_OD vertical edge [between two consecutive 90-90 degree corners] $\leq 0.158 \mu\text{m}$</p> <p>ISO_Small_OD : Small_OD space to ALL_OD > 0.292 μm [PRL > -0.120 μm] in horizontal direction</p> <p>1st_STI_MD : STI_MD space to {Wide_OD OR ISO_Small_OD} $\leq 0.014 \mu\text{m}$ in horizontal direction [PRL > 0 μm]</p>			
MD.R.13.1	<p>1st_STI_MD interact {{OD OR VC} OR MP} or space to 2 or more {Wide_OD OR ISO_Small_OD} $\leq 0.016 \mu\text{m}$ in horizontal direction [PRL > 0 μm, INSIDE PO_P63] is not allowed (Except BLK_WF)</p> <p>STI_MD : {ALL_MD [width = 0.024 $\mu\text{m}】 NOT ALL_CMD [Derived from BCMD]} NOT ALL_OD$</p> <p>Wide_OD : Length of ALL_OD vertical edge [between two consecutive 90-90 degree corners] $\geq 0.188 \mu\text{m}$</p> <p>Small_OD : Length of ALL_OD vertical edge [between two consecutive 90-90 degree corners] $\leq 0.158 \mu\text{m}$</p> <p>ISO_Small_OD : Small_OD space to ALL_OD > 0.307 μm [PRL > -0.120 μm] in horizontal direction</p> <p>1st_STI_MD : STI_MD space to {Wide_OD OR ISO_Small_OD} $\leq 0.016 \mu\text{m}$ in horizontal direction [PRL > 0 μm]</p>			
MD.R.13.2	<p>1st_STI_MD interact {{OD OR VC} OR MP} or space to 2 or more {Wide_OD OR ISO_Small_OD} $\leq 0.019 \mu\text{m}$ in horizontal direction [PRL > 0 μm, INSIDE PO_P76] is not allowed (Except BLK_WF)</p> <p>STI_MD : {ALL_MD [width = 0.030 $\mu\text{m}】 NOT ALL_CMD [Derived from BCMD]} NOT ALL_OD$</p> <p>Wide_OD : Length of ALL_OD vertical edge [between two consecutive 90-90 degree corners] $\geq 0.188 \mu\text{m}$</p> <p>Small_OD : Length of ALL_OD vertical edge [between two consecutive 90-90 degree corners] $\leq 0.158 \mu\text{m}$</p> <p>ISO_Small_OD : Small_OD space to ALL_OD > 0.372 μm [PRL > -0.120 μm] in horizontal direction</p> <p>1st_STI_MD : STI_MD space to {Wide_OD OR ISO_Small_OD} $\leq 0.019 \mu\text{m}$ in horizontal direction [PRL > 0 μm]</p>			

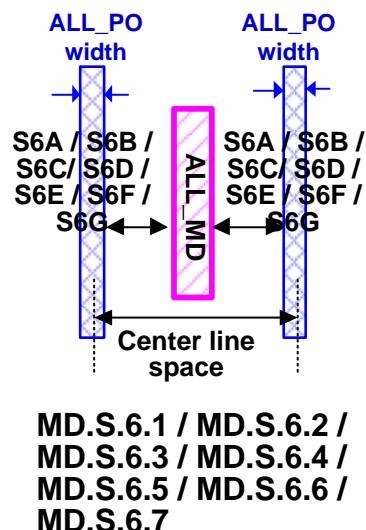
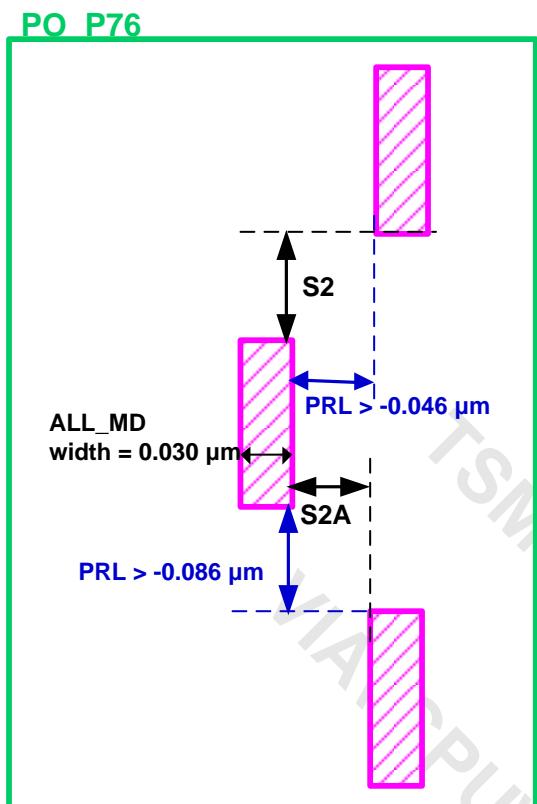
Rule No.	Description	Label	Op.	Rule
MD.R.15	<p>ALL_MD interact Edge_PO_P57 is not allowed (Except Dummy_Cell, BLK_WF, or following conditions:</p> <ol style="list-style-type: none"> 1. {ALL_MD NOT ALL_CMD} interact {STRAP NOT VAR} and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are floating (not interact MP) or same net to {ALL_MD NOT ALL_CMD}, 2. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are floating (not interact MP), 3. {ALL_MD NOT ALL_CMD} and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are same net, 4. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side are same net, 5. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on one side is floating and on the other side interact strap with same net.) <p>Definition of Edge_PO_P57: {PO_P57_Group NOT {PO_P57_Group SIZING -0.228 μm in horizontal direction}}</p> <p>Definition of PO_P57_Group: Form PO_P57 with neighboring PO_P57 (space = 0.046/0.0475/0.049 μm) as group</p> <p>Definition of PO_P57: ALL_PO [width ≤ 0.011 μm]</p>			
MD.R.15.1	<p>ALL_MD interact Edge_PO_P63 is not allowed (Except Dummy_Cell, or following conditions:</p> <ol style="list-style-type: none"> 1. {ALL_MD NOT ALL_CMD} interact {STRAP NOT VAR} and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are floating (not interact MP) or same net to {ALL_MD NOT ALL_CMD}, 2. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are floating (not interact MP), 3. {ALL_MD NOT ALL_CMD} and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are same net, 4. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side are same net, 5. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on one side is floating and on the other side interact strap with same net.) <p>Definition of Edge_PO_P63: {PO_P63_Group NOT {PO_P63_Group SIZING -0.252 μm in horizontal direction}}</p> <p>Definition of PO_P63_Group: Form ALL_PO [INSIDE PO_P63] with neighboring ALL_PO (space = 0.052/0.0535/0.055 μm) as group</p>			

Rule No.	Description	Label	Op.	Rule
MD.R.15.2	<p>ALL_MD interact Edge_PO_P76 is not allowed (Except Dummy_Cell, or following conditions:</p> <ol style="list-style-type: none"> 1. {ALL_MD NOT ALL_CMD} interact {STRAP NOT VAR} and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are floating (not interact MP) or same net to {ALL_MD NOT ALL_CMD}, 2. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are floating (not interact MP), 3. {ALL_MD NOT ALL_CMD} and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side in horizontal direction are same net, 4. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on both side are same net, 5. {ALL_MD NOT ALL_CMD} is floating (not interact {OD OR MP OR VC}) and its 1st neighboring {ALL_PO NOT ALL_CPO} on one side is floating and on the other side interact strap with same net.) <p>Definition of Edge_PO_P76: {PO_P76_Group NOT {PO_P76_Group SIZING -0.304 μm in horizontal direction}}</p> <p>Definition of PO_P76_Group: Form ALL_PO [INSIDE PO_P76] with neighboring ALL_PO (space = 0.0650/0.0665/0.0680 μm) as group</p>			
MD.R.23	<p>Maximum delta V > 3.63V is not allowed.</p> <p>DRC searching range of {ALL_MD NOT ALL_CMD} space to ALL_OD is < 0.750 μm; {ALL_MD NOT ALL_CMD} space to {ALL_PO NOT ALL_CPO} is < 0.700 μm; {ALL_MD NOT ALL_CMD} space to {ALL_MD NOT ALL_CMD} is < 0.700 μm</p>			
MD.R.24	<p>STI_PO_Floating space to 2 or more Short_STI_MD_Bias ≤ 0.016 μm in horizontal direction [PRL > 0 μm] is not allowed (Except following conditions:</p> <ol style="list-style-type: none"> 1. all Short_STI_MD_Bias beside same STI_PO_Floating are same net) <p>Definition of STI_PO_Floating: { {ALL_PO [width ≤ 0.011 μm] NOT ALL_CPO} [NOT INTERACT ALL_OD] } not interact MP</p> <p>Definition of STI_PO_Bias { {ALL_PO [width ≤ 0.011 μm] NOT ALL_CPO} [NOT INTERACT ALL_OD] } interact MP</p> <p>Definition of Short_STI_MD_Bias: { {ALL_MD [width = 0.024 μm] NOT ALL_CMD [Derived from BCMD]} [NOT INTERACT ALL_OD, length < 0.082 μm] } interact {MP OR VC}</p>			
MD.R.24.1	<p>STI_PO_Bias space to Short_STI_MD_Bias ≤ 0.016 μm in horizontal direction [PRL > 0 μm] is not allowed (Except following conditions:</p> <ol style="list-style-type: none"> 1. STI_PO_Bias and Short_STI_MD_Bias are same net) <p>Definition of STI_PO_Bias, Short_STI_MD_Bias follow MD.R.24</p>			

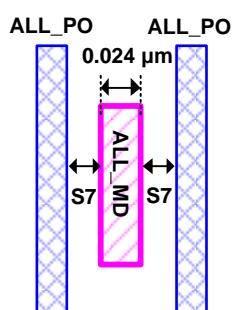
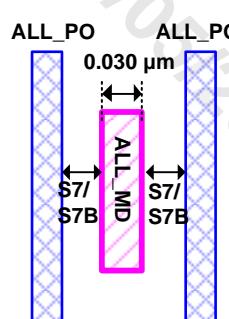
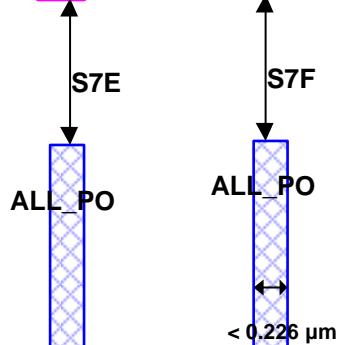
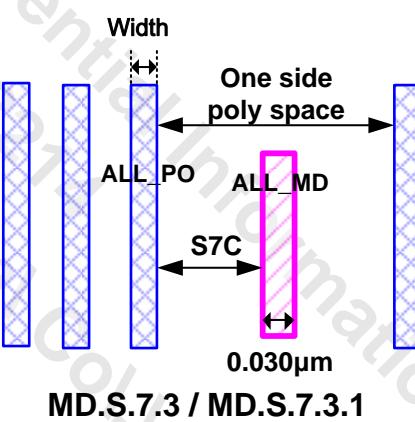
Rule No.	Description	Label	Op.	Rule
MD.R.25	<p>1st_STI_PO_Floating space to 2 or more {1st_Checked_MD OR MD_Bias} $\leq 0.019 \mu\text{m}$ in horizontal direction [PRL > 0 μm] is not allowed (Except following conditions: 1. Space region interact ALL_MP [width = 0.022 μm])</p> <p>Definition of 1st_STI_PO_Floating: {ALL_PO [width $\leq 0.011 \mu\text{m}$] NOT ALL_CPO} [space to OD_Iso_Edge $\leq 0.076 \mu\text{m}$ in horizontal direction, PRL > 0 μm] not interact ALL_MP</p> <p>Definition of 1st_STI_PO_Bias: {ALL_PO [width $\leq 0.011 \mu\text{m}$] NOT ALL_CPO} [space to OD_Iso_Edge $\leq 0.076 \mu\text{m}$ in horizontal direction, PRL > 0 μm] interact ALL_MP</p> <p>Definition of OD_Iso_Edge: ALL_OD vertical edge [INTERACT {{CHIP NOT {ALL_OD SIZING up/down 0.400 μm} down/up 0.400 μm} can enclose a 0.800 μm x 0.800 μm orthogonal rectangle}]</p> <p>Definition of 1st_Checked_MD: {{ALL_MD NOT Dummy_Cell} NOT ALL_CMD [Derived from BCMD]} space to ALL_OD $\leq 0.063 \mu\text{m}$ in horizontal direction [PRL > 0 μm]</p> <p>Definition of MD_Bias: {{ALL_MD NOT ALL_CMD [Derived from BCMD]} [INTERACT {ALL_MP OR VC}]} NOT ALL_OD}</p>			
MD.R.25.1	<p>1st_STI_PO_Bias space to {1st_Checked_MD OR MD_Bias} $\leq 0.019 \mu\text{m}$ in horizontal direction [PRL > 0 μm] is not allowed (Except following conditions: 1. Space region interact ALL_MP [width = 0.022 μm])</p> <p>Definition of 1st_STI_PO_Bias, OD_Iso_Edge, 1st_Checked_MD, MD_Bias follow MD.R.25</p>			

Rule No.	Description	Label	Op.	Rule
MD.G0.0	<p>G0-SPACE definition:</p> <ul style="list-style-type: none"> 1. G0 X space (G0XS) of ALL_MD [width = 0.024 μm] < 0.084 μm [PRL > -0.096 μm] 2. G0 Y space (G0YS) of ALL_MD [width = 0.024 μm] < 0.096 μm [PRL > -0.084 μm] 3. G0 X space (G0XS) of ALL_MD [width = 0.030 μm, NOT INSIDE PO_P76] to ALL_MD [NOT INSIDE PO_P76] < 0.150 μm [PRL > -0.096 μm] 4. G0 Y space (G0YS) of ALL_MD [width = 0.030 μm, NOT INSIDE PO_P76] to ALL_MD [NOT INSIDE PO_P76] < 0.096 μm [PRL > -0.150 μm] 5. G0 X space (G0XS) of ALL_MD [width = 0.030 μm, INSIDE PO_P76] to ALL_MD [INSIDE PO_P76] < 0.122 μm [PRL > -0.096 μm] 6. G0 Y space (G0YS) of ALL_MD [width = 0.030 μm, INSIDE PO_P76] to ALL_MD [INSIDE PO_P76] < 0.096 μm [PRL > -0.122 μm] <p>G0-AREA definition:</p> <ul style="list-style-type: none"> 1. G0 run-run area (G0RA): The projection area between 2 edges with G0XS/G0YS 2. G0-AREA is independent to all other ones, even if they are overlapped or crossed <p>Loop:</p> <ul style="list-style-type: none"> 1. A loop is formed when ALL_MD polygons are connected in a cyclic sequence with G0-AREA in between 2. A loop cannot contain any sub-loops which share one or more polygons with it 			
MD.G0.1	G0-AREA cannot be formed by single polygon			
MD.G0.2	G0-AREA count of the close loop formed by original polygons and G0-AREAs cannot be odd number			

MD

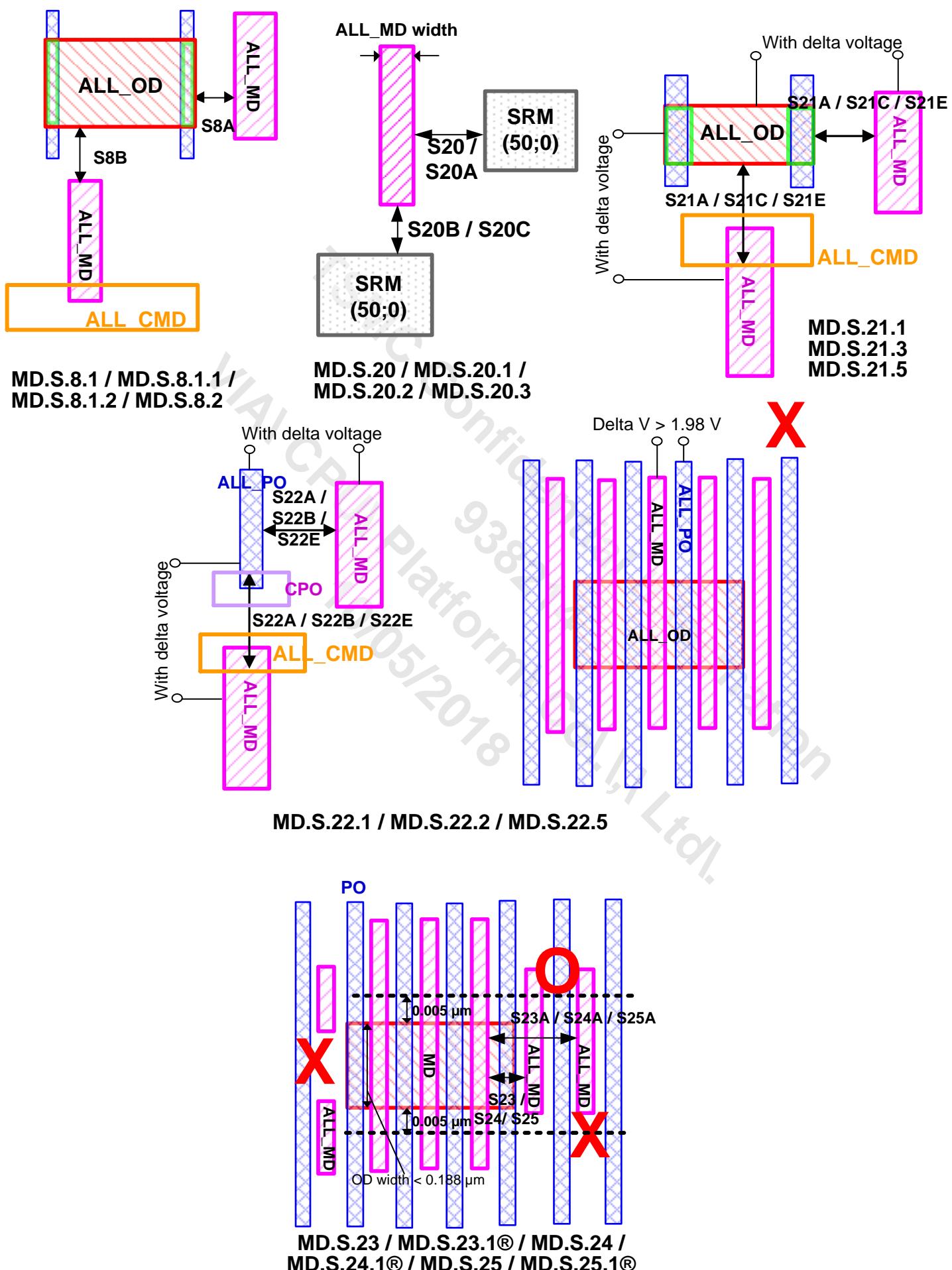


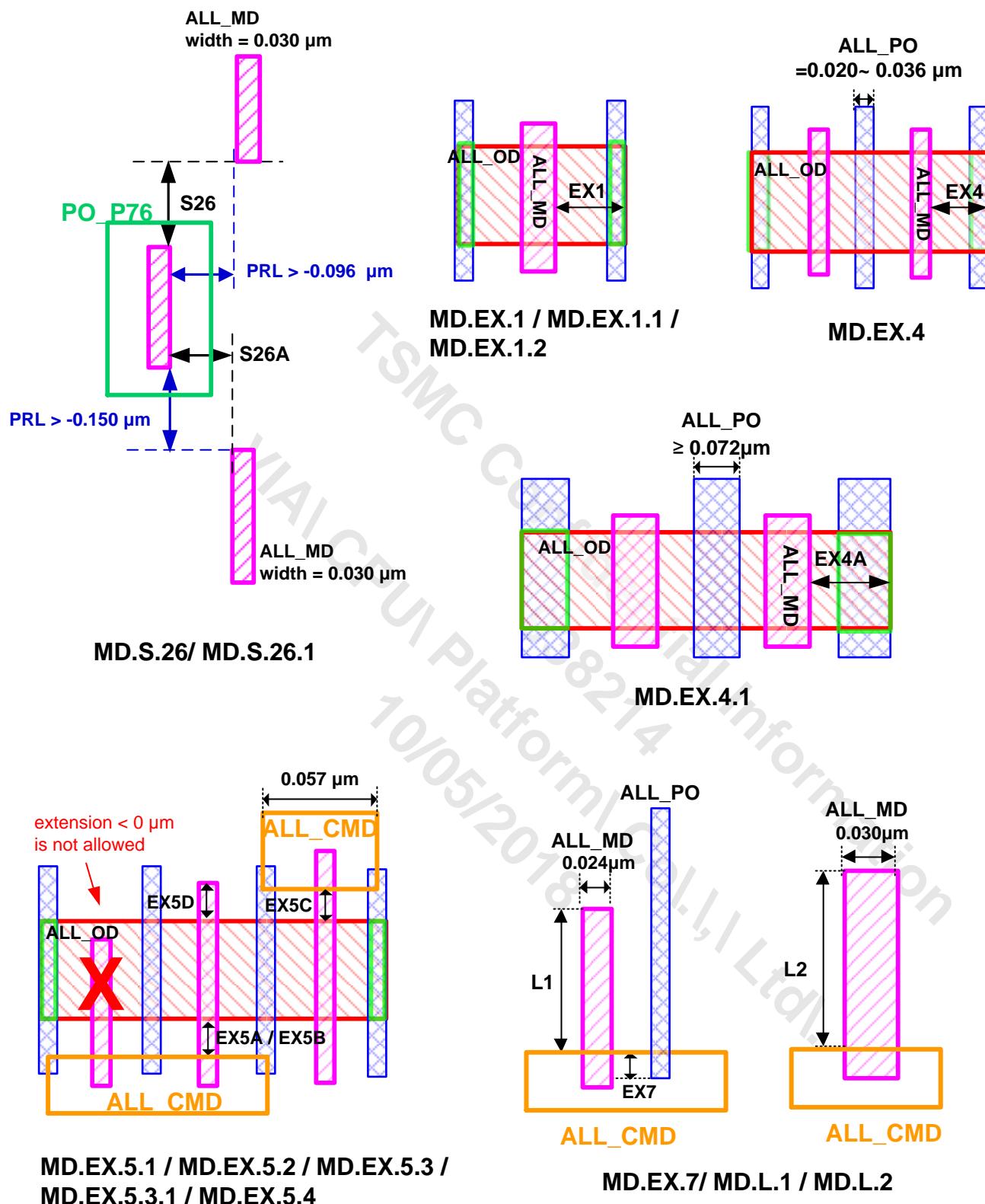
MD.S.2.0.1/ MD.S.2.2

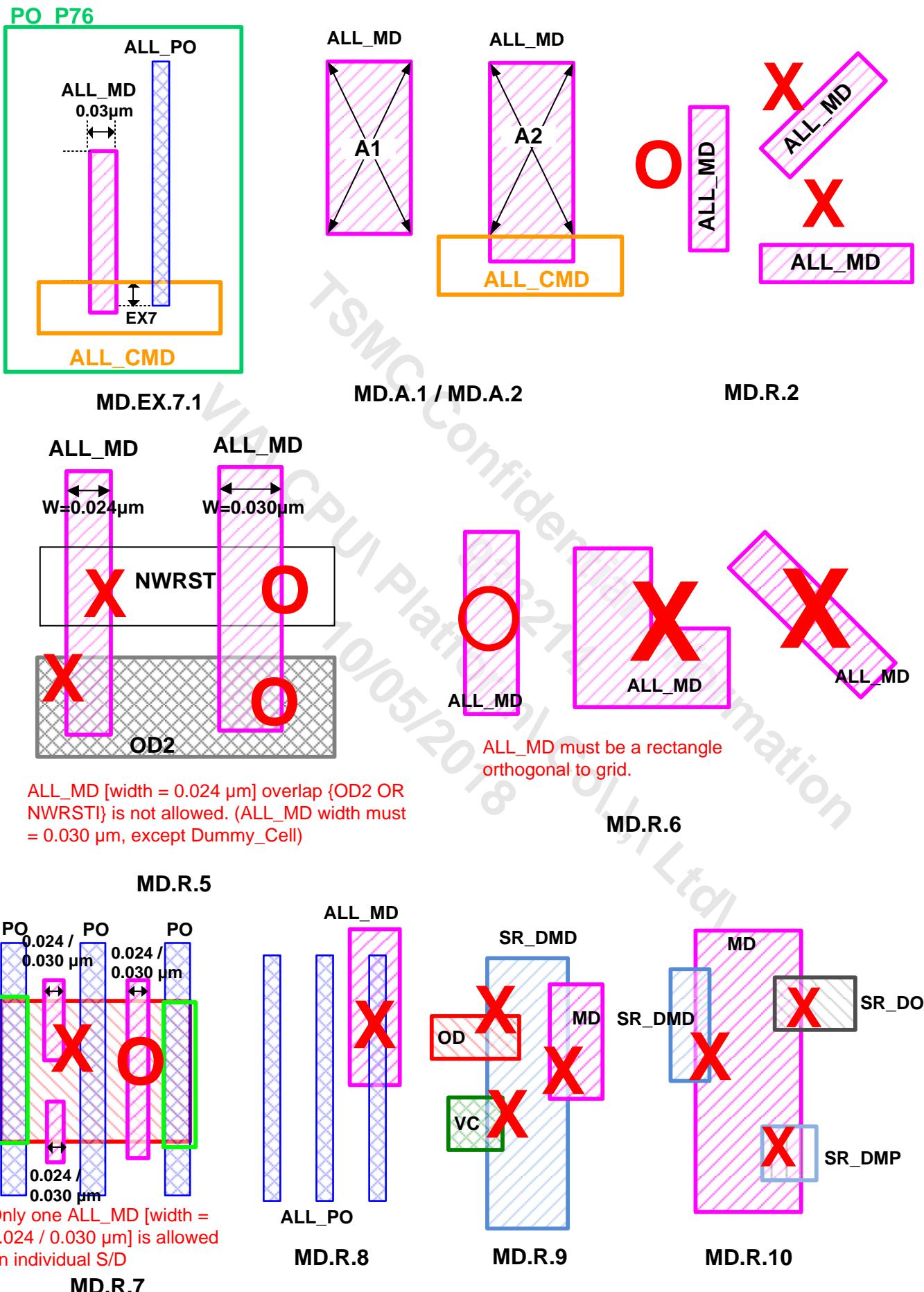
MD.S.7 /
MD.S.7.0.1 /
MD.S.7.1MD.S.7.2
MD.S.7.0.2/
MD.S.7.2.1

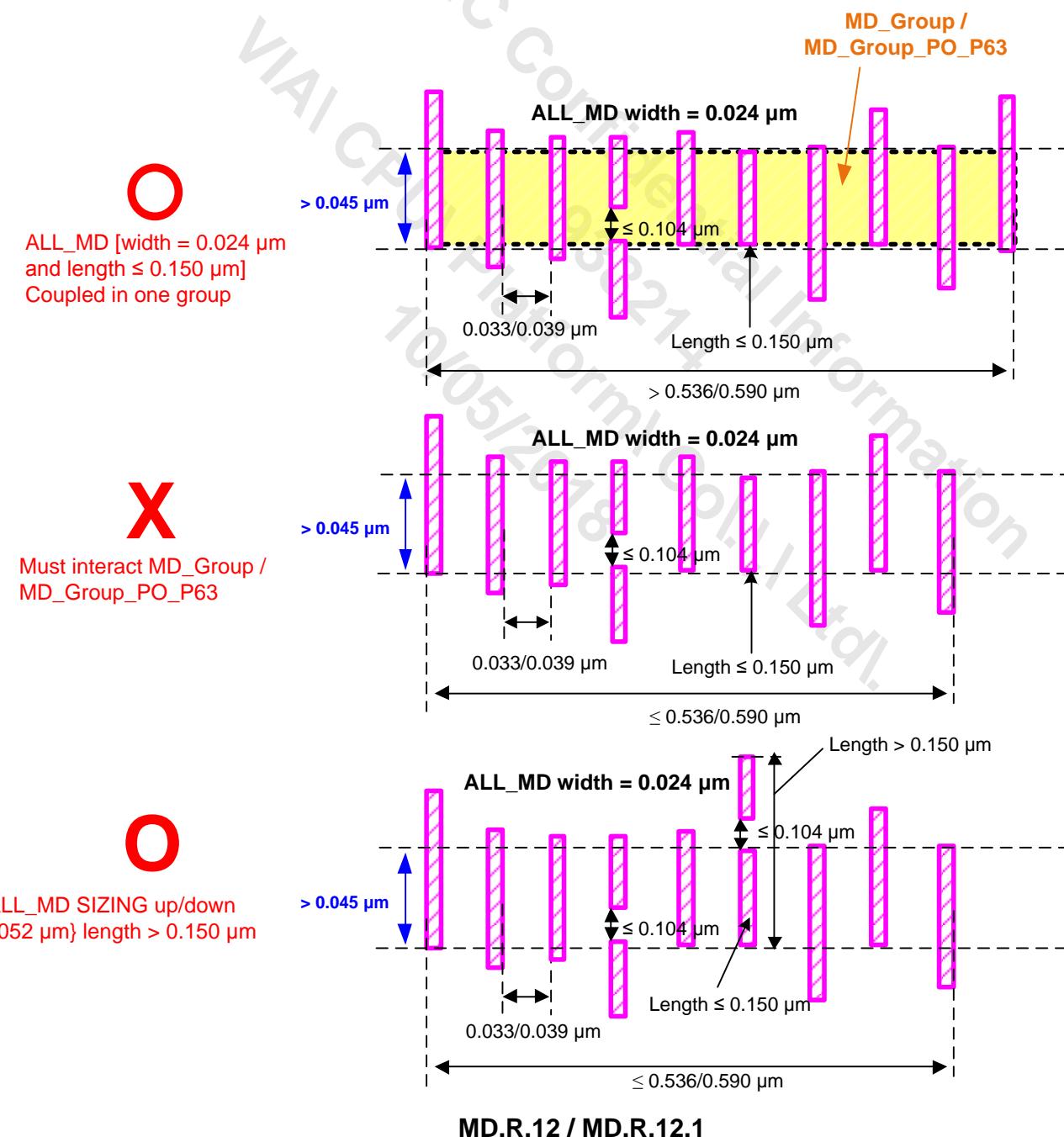
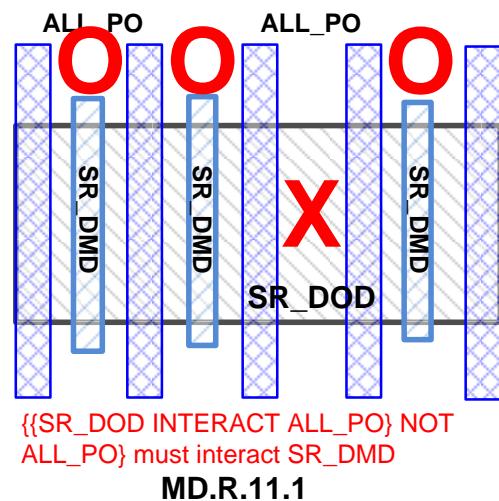
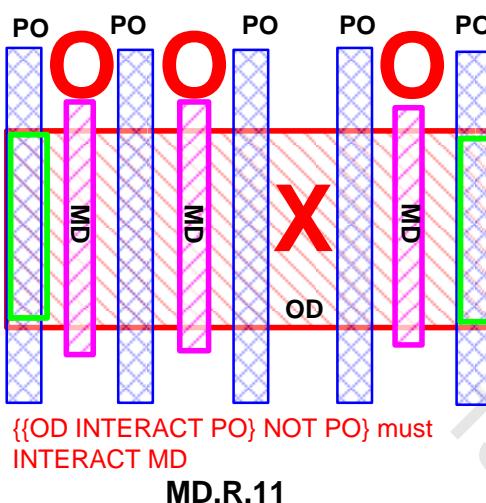
MD.S.7.4

MD.S.7.5 / MD.S.7.6





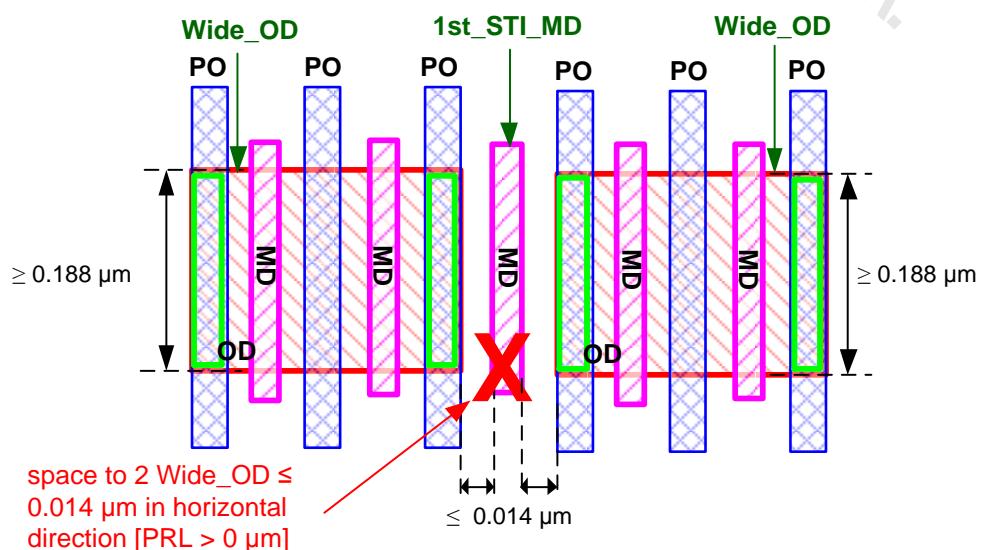
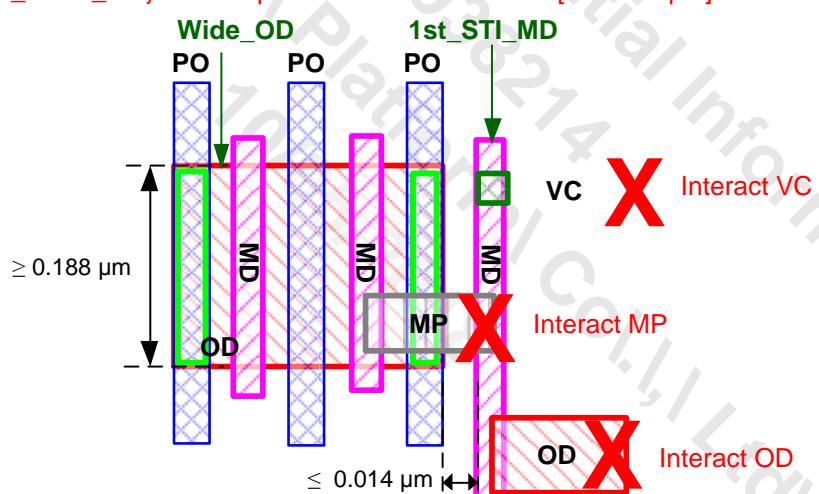
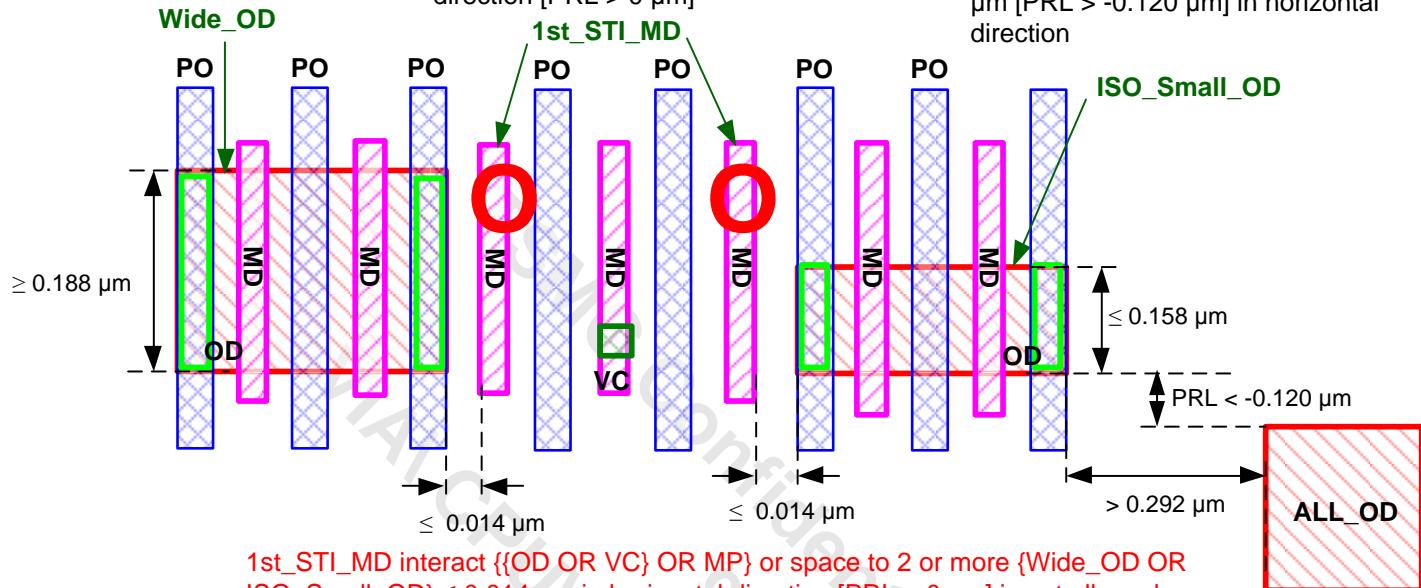




Wide_OD :
Length of ALL_OD vertical edge
[between two consecutive 90-90 degree corners] $\geq 0.188 \mu\text{m}$

STI_MD :
{ALL_MD [width = 0.024 μm] NOT
ALL_CMD} NOT ALL_OD
1st_STI_MD :
STI_MD space to {Wide_OD OR
ISO_Small_OD} $\leq 0.014 \mu\text{m}$ in horizontal
direction [PRL > 0 μm]

Small_OD :
Length of ALL_OD vertical edge
[between two consecutive 90-90 degree
corners] $\leq 0.158 \mu\text{m}$
ISO_Small_OD :
Small_OD space to ALL_OD > 0.292
 μm [PRL > -0.120 μm] in horizontal
direction

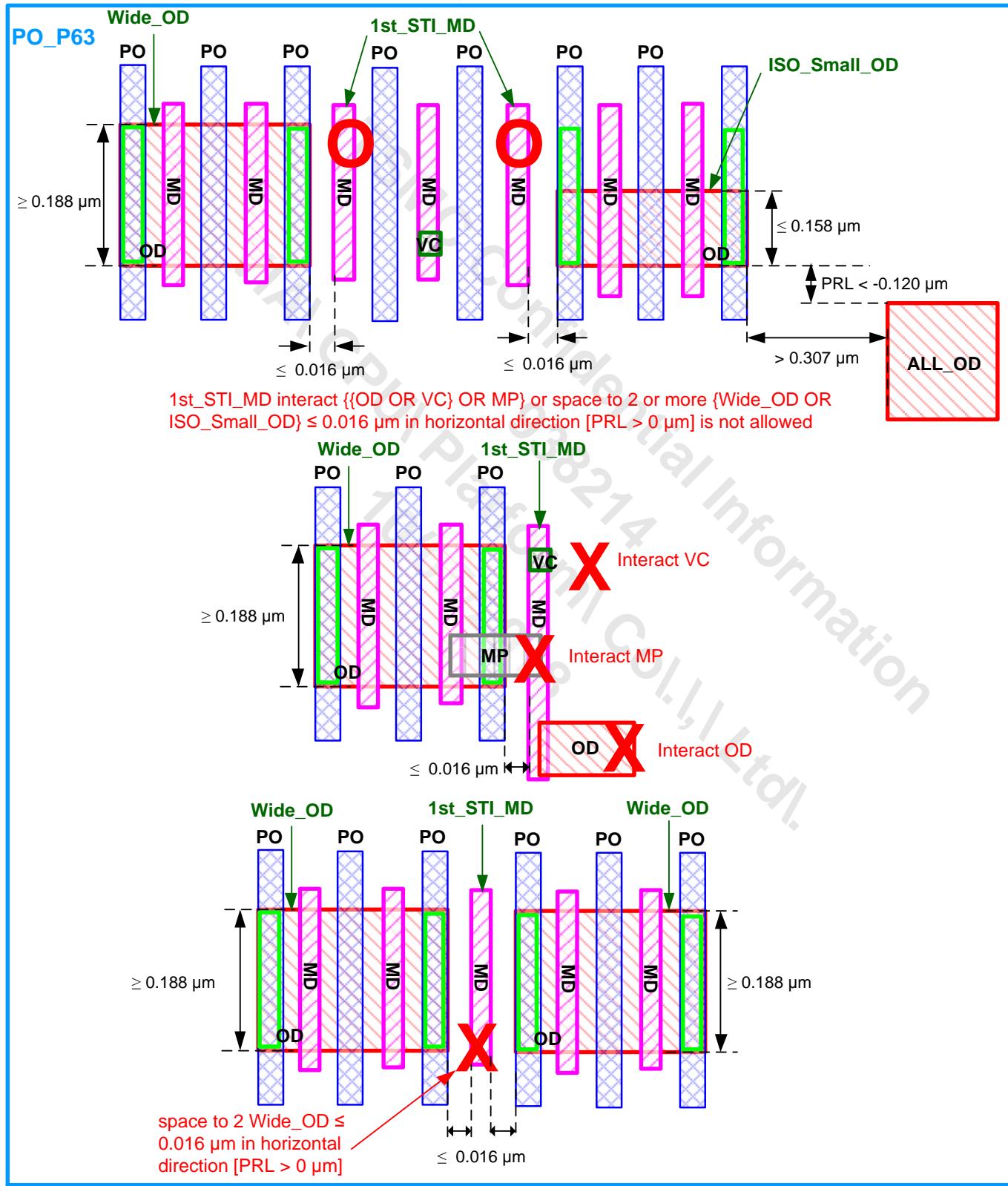


MD.R.13

Wide_OD :
Length of ALL_OD vertical edge
[between two consecutive 90-90 degree corners] $\geq 0.188 \mu\text{m}$

STI_MD :
{ALL_MD [width = 0.024 μm] NOT
ALL_CMD} NOT ALL_OD
1st_STI_MD :
STI_MD space to {Wide_OD OR
ISO_Small_OD} $\leq 0.016 \mu\text{m}$ in horizontal
direction [PRL > 0 μm]

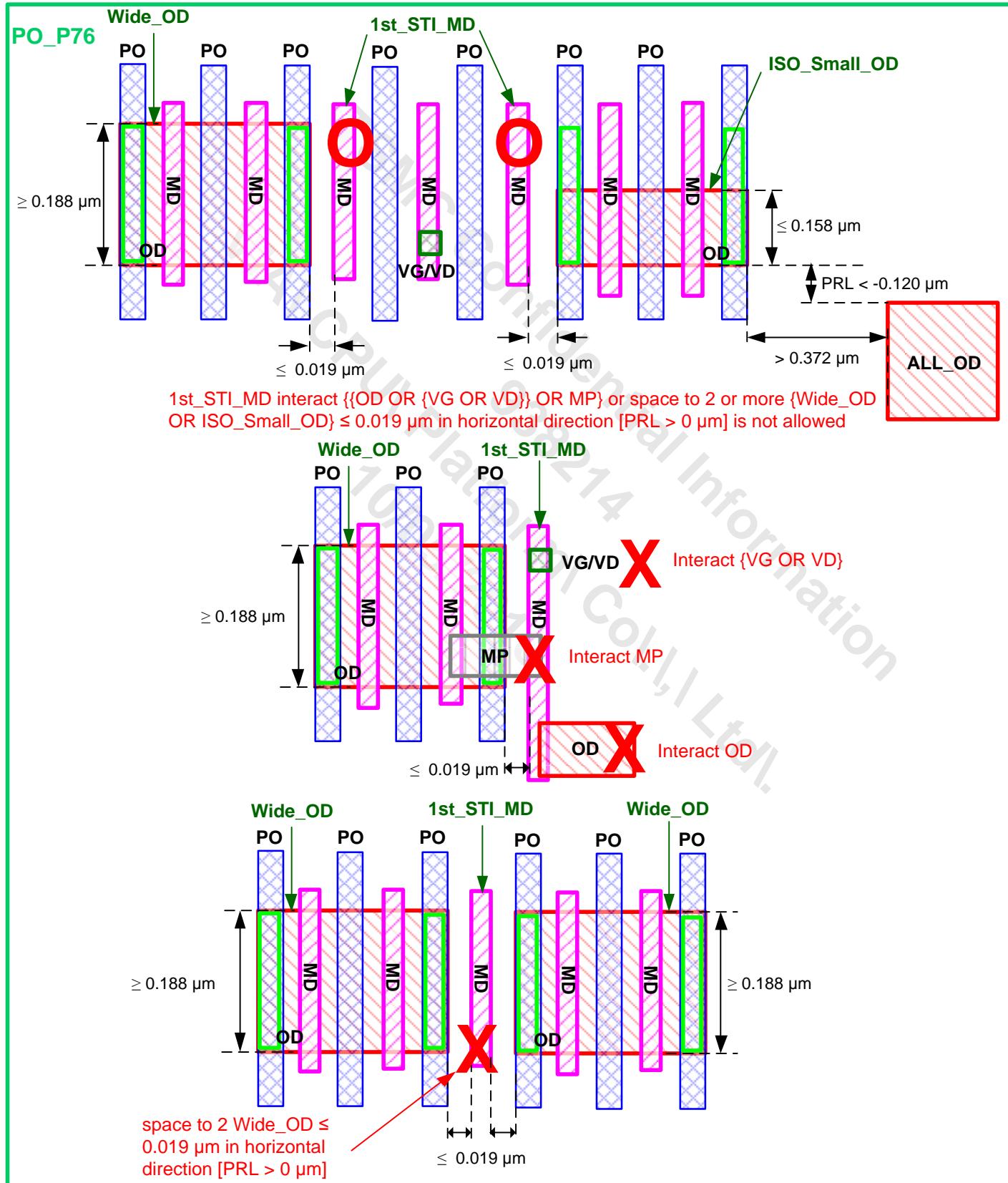
Small_OD :
Length of ALL_OD vertical edge
[between two consecutive 90-90 degree
corners] $\leq 0.158 \mu\text{m}$
ISO_Small_OD :
Small_OD space to ALL_OD > 0.307
 μm [PRL < -0.120 μm] in horizontal
direction



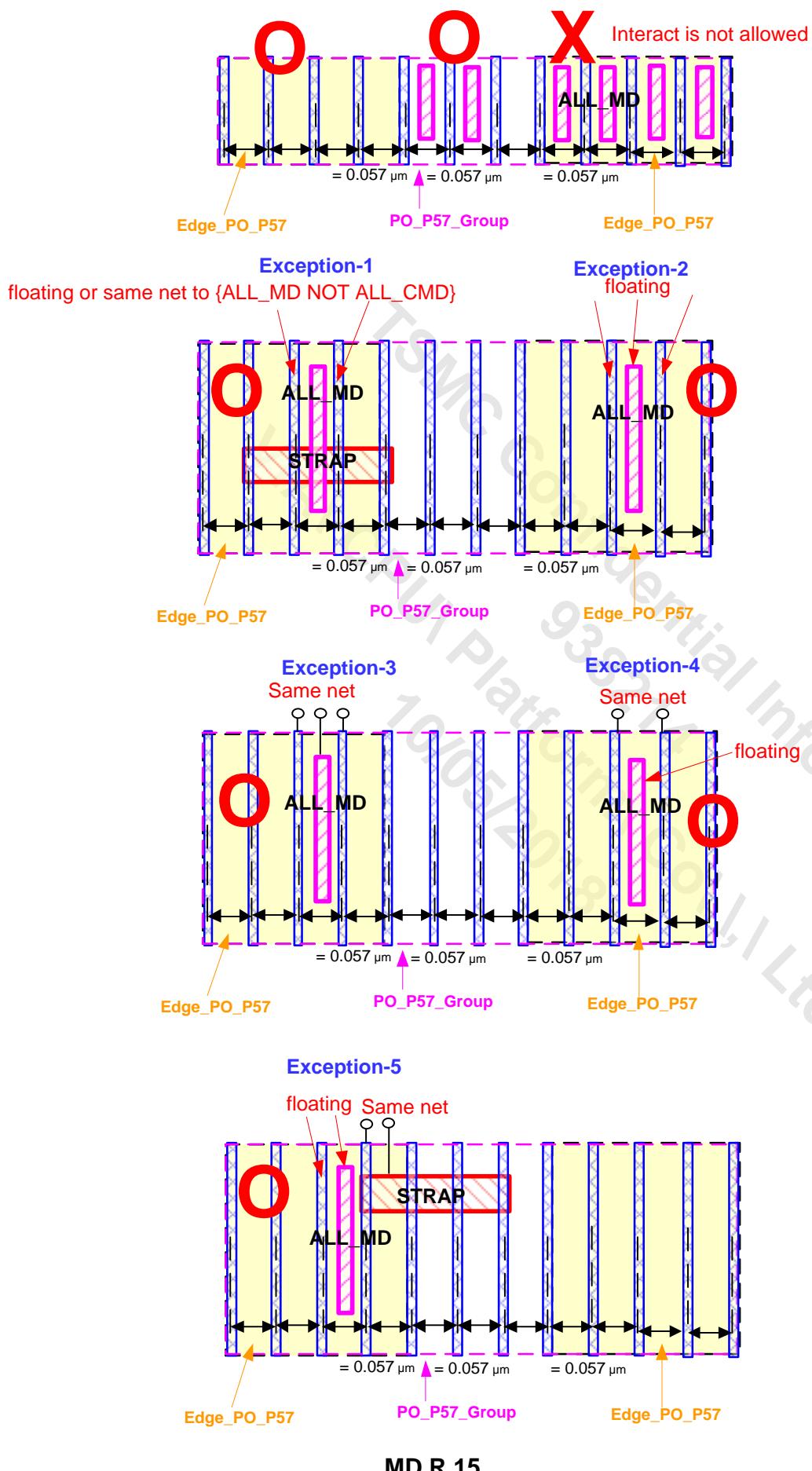
Wide_OD :
Length of ALL_OD vertical edge
[between two consecutive 90-90 degree corners] $\geq 0.188 \mu\text{m}$

STI_MD :
{ALL_MD [width = 0.030 μm] NOT
ALL_CMD} NOT ALL_OD
1st_STI_MD :
STI_MD space to {Wide_OD OR
ISO_Small_OD} $\leq 0.019 \mu\text{m}$ in horizontal
direction [PRL > 0 μm]

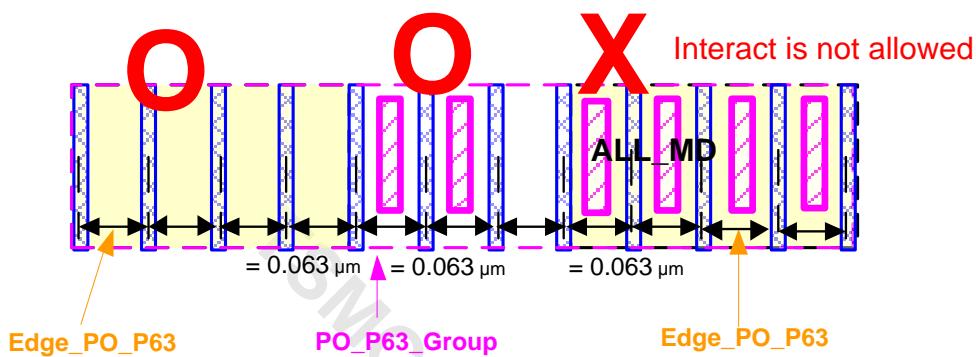
Small_OD :
Length of ALL_OD vertical edge
[between two consecutive 90-90 degree
corners] $\leq 0.158 \mu\text{m}$
ISO_Small_OD :
Small_OD space to ALL_OD $> 0.372 \mu\text{m}$ [PRL < -0.120 μm] in horizontal
direction



MD.R.13.2

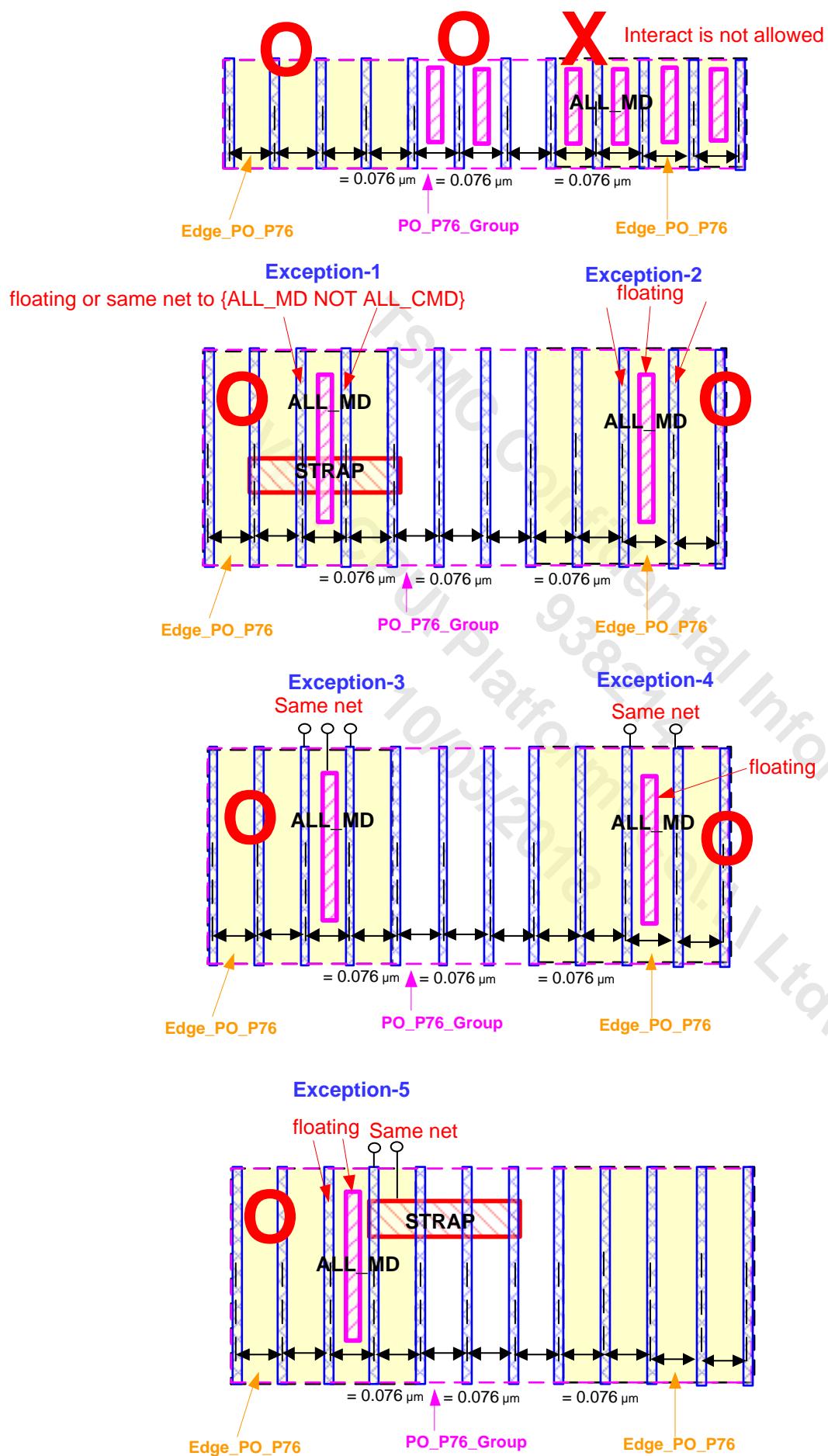


PO_P63



MD.R.15.1

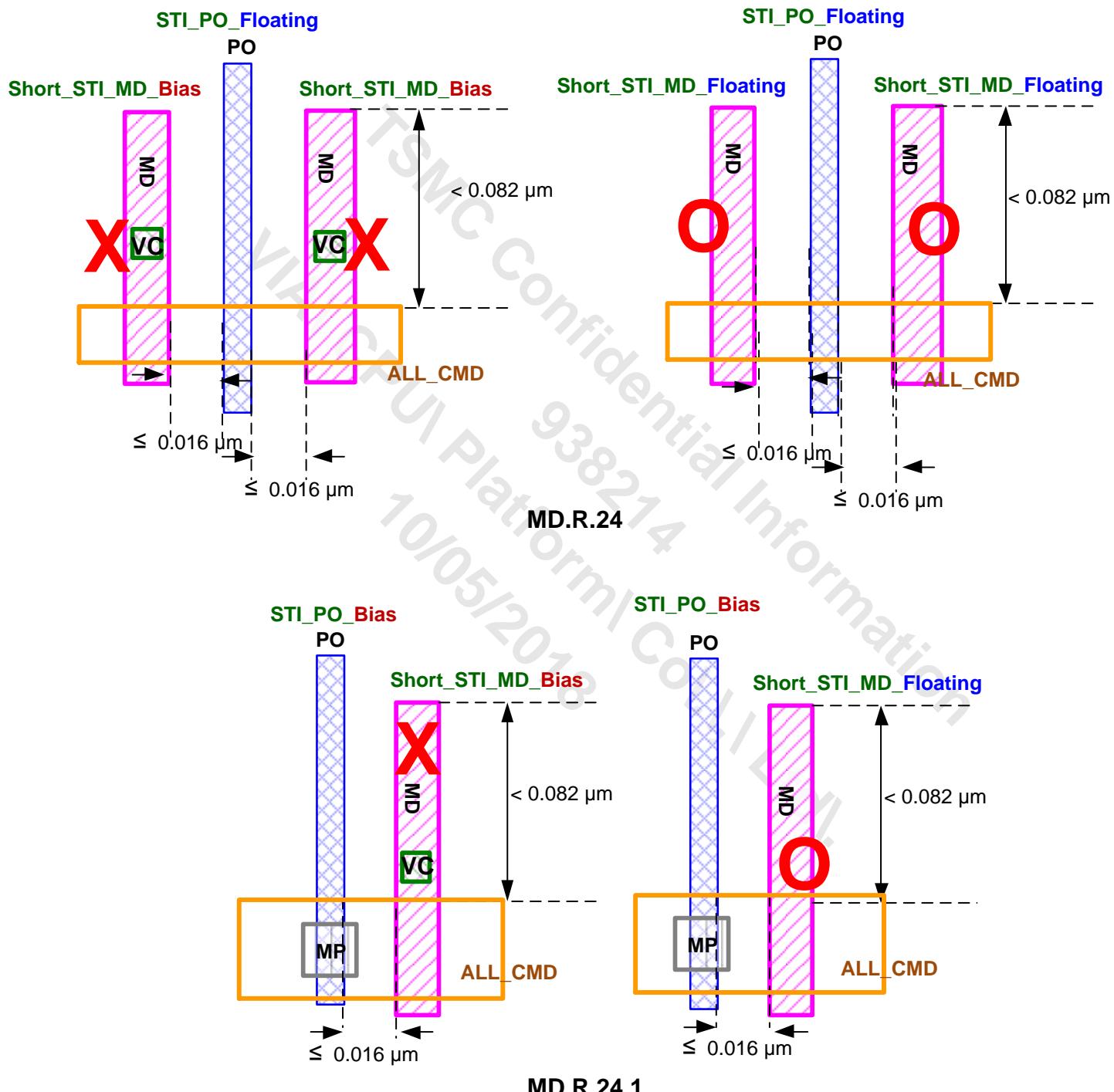
10/05/2018

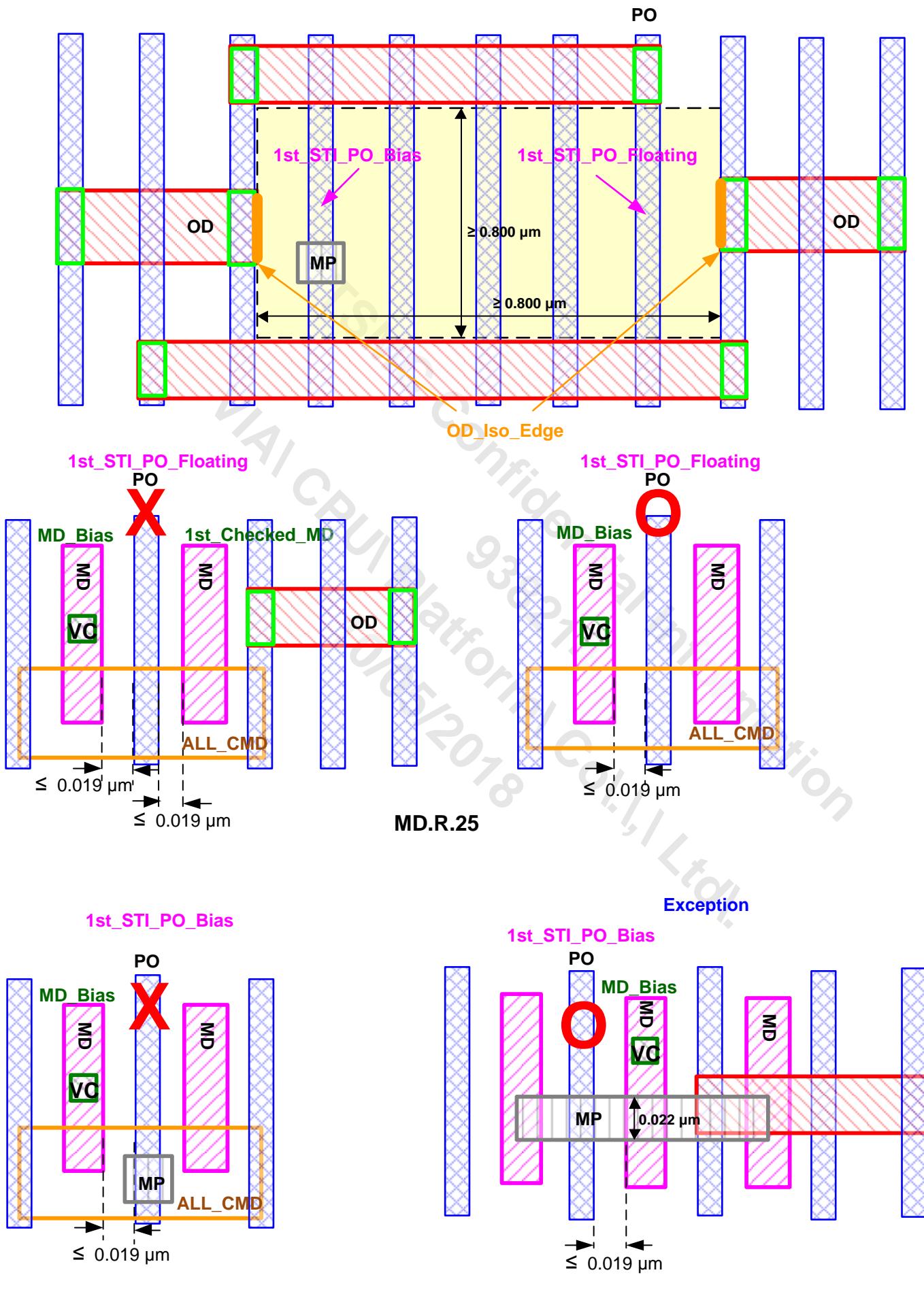


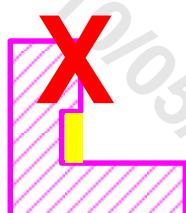
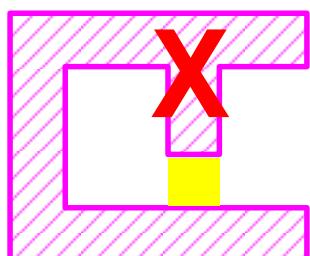
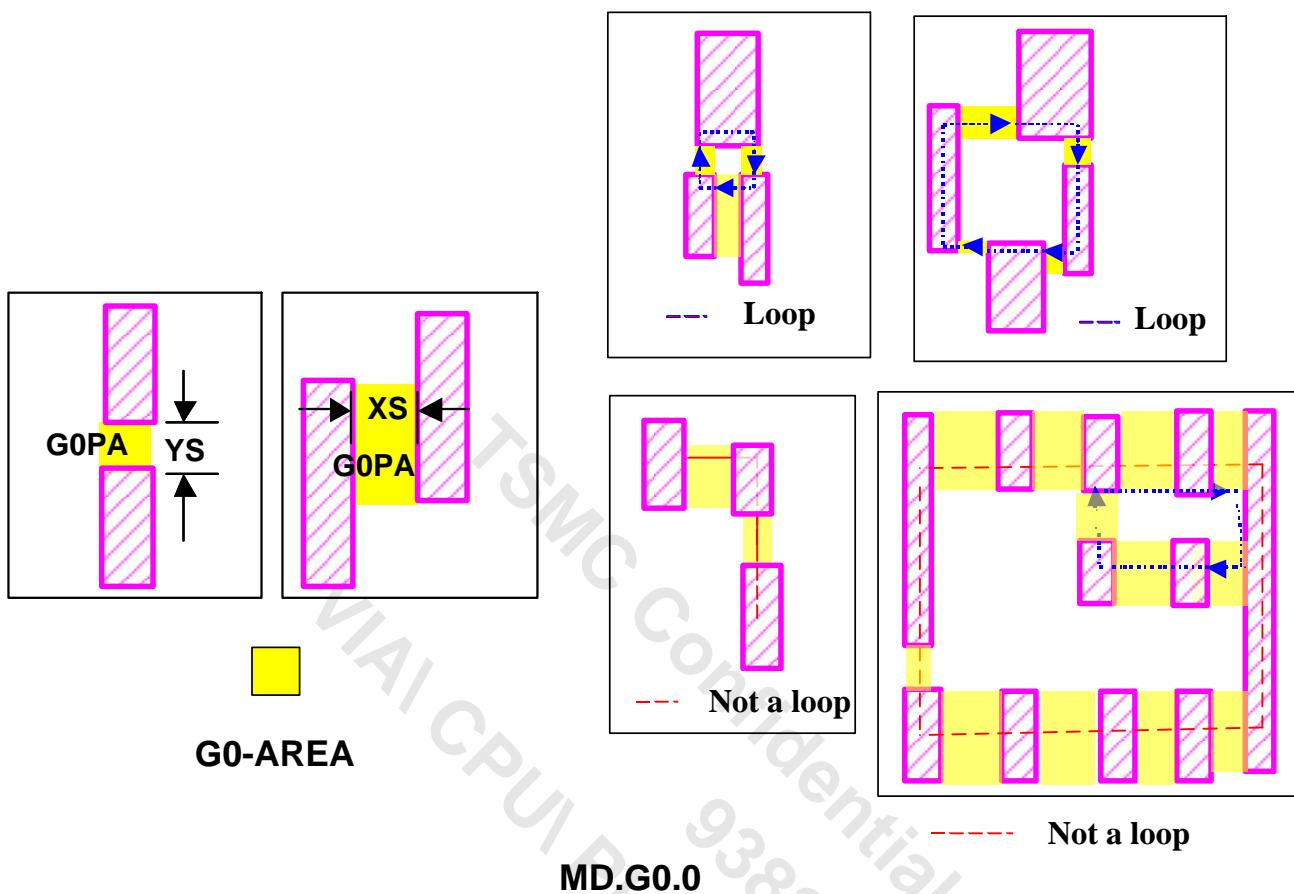
STI_PO_Floating:
 $\{\{ALL_PO [width \leq 0.011 \mu m]\}$
 $NOT ALL_CPO\} [NOT$
 $INTERACT ALL_OD]\} not$
 interact MP

Short_STI_MD_Bias:
 $\{\{ALL_MD [width = 0.024 \mu m]\} NOT$
 $ALL_CMD [Derived from BCMD]\} [NOT$
 $INTERACT ALL_OD, length < 0.082$
 $\mu m\} interact \{MP OR VC\}$

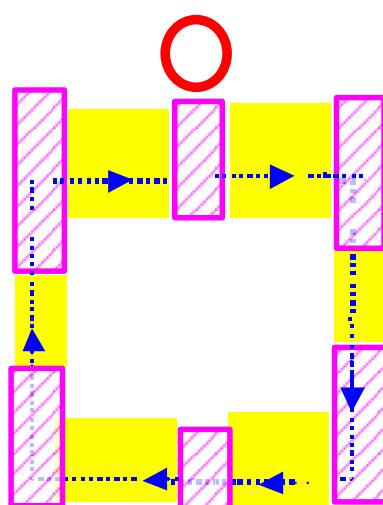
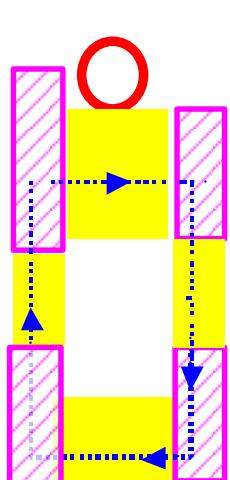
STI_PO_Bias
 $\{\{ALL_PO [width \leq 0.011 \mu m]\} NOT$
 $ALL_CPO\} [NOT INTERACT$
 $ALL_OD]\} interact MP$



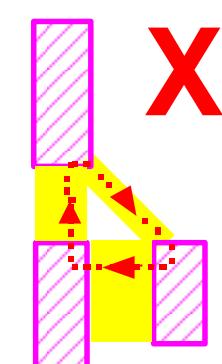




MD.G0.1



Count = 4, even



Count = 3, odd

MD.G0.2

4.5.34 Cut-MD (CMD) Layout Rules

CMD (CAD layer: 84;20) is used to cut MD.

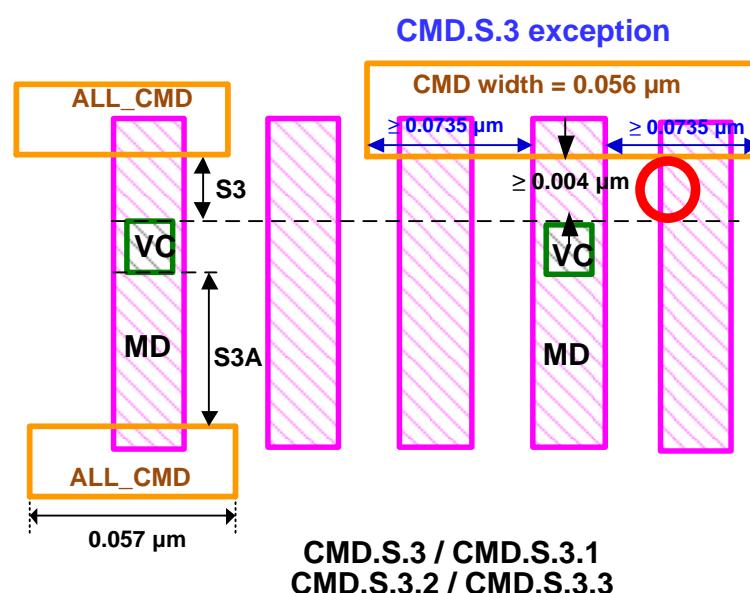
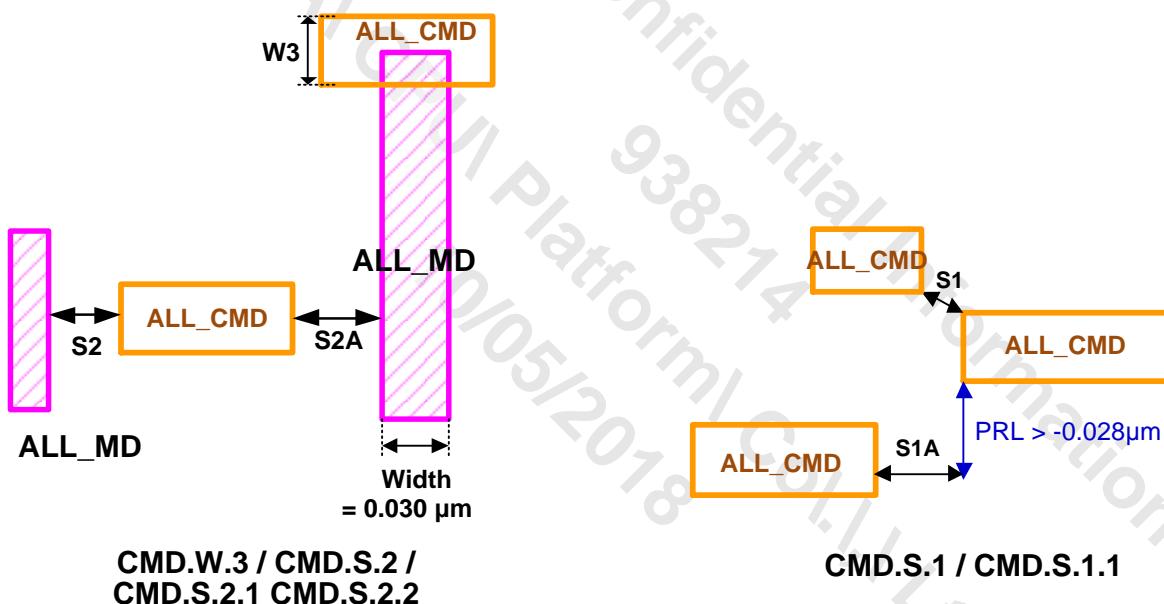
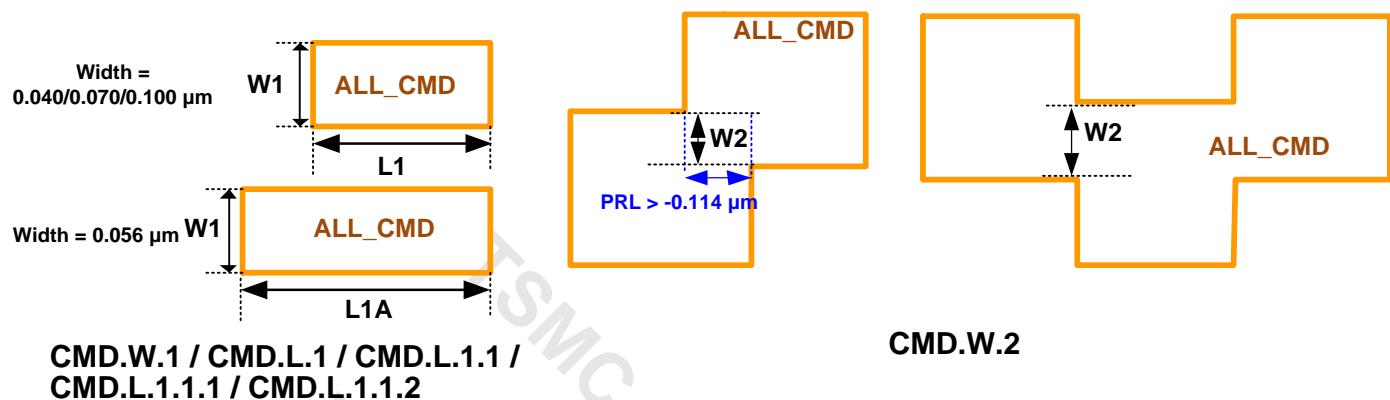
ALL_CMD = {CMD OR SR_DCMD}

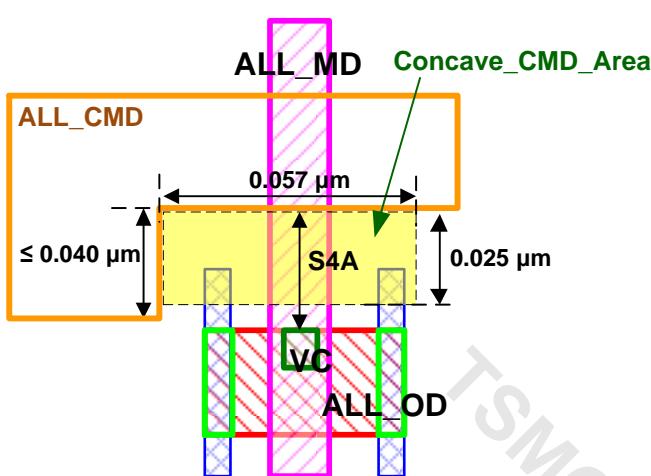
Rule No.	Description	Label	Op.	Rule
CMD.W.1	Width of ALL_CMD in vertical direction (Except FB_9, FB_8)	W1	=	0.0400, 0.0560, 0.0700, 0.1000
CMD.W.2	Concave corner to concave corner width of ALL_CMD in vertical direction [PRL > -0.114 μm] (Except FB_9, FB_8) DRC flags space between 2 horizontal ALL_CMD edge in vertical direction < 0.040 μm [PRL > -0.114 μm]	W2	≥	0.0400
CMD.W.3	Width of ALL_CMD [INTERACT ALL_MD [width = 0.030 μm]] in vertical direction	W3	≥	0.0560
CMD.S.1	Space of ALL_CMD (Except FB_8)	S1	≥	0.0280
CMD.S.1.1	Space of ALL_CMD in horizontal direction [PRL > -0.028 μm]	S1A	≥	0.0570
CMD.S.2	Space of ALL_CMD to ALL_MD	S2	≥	0.0165
CMD.S.2.1	Space of ALL_CMD to ALL_MD [width = 0.030 μm] in horizontal direction (Except PO_P76)	S2A	≥	0.0350
CMD.S.2.2	Space of ALL_CMD to ALL_MD [width = 0.030 μm] in horizontal direction [INSIDE PO_P76]	S2A	≥	0.0230
CMD.S.3	Space of ALL_CMD edge [INSIDE MD] to VC [INTERACT MD] [PRL > 0 μm] (VC [INTERACT MD] overlap ALL_CMD is not allowed) (Except FB_9, FB_8, or following conditions: 1. VC [INTETACT MD] space to edge of rectangular CMD [width = 0.056 μm, extension on the same MD ≥ 0.0735 μm in horizontal direction at both sides] ≥ 0.004 μm, [PRL > 0])	S3	≥	0.0050
CMD.S.3.1	Space of rectangular ALL_CMD edge [ALL_CMD length = 0.057 μm, INSIDE MD] to VC [INTERACT MD] [PRL > 0 μm] (VC [INTERACT MD] overlap ALL_CMD is not allowed) (Except FB_9, FB_8)	S3A	≥	0.0060
CMD.S.3.2	Space of rectangular ALL_CMD edge [ALL_CMD length ≤ 0.063 μm, INSIDE MD] to VC [INTERACT MD] [PRL > 0 μm, INSIDE PO_P63] (VC [INTERACT MD] overlap ALL_CMD is not allowed) (Except FB_9, FB_8)	S3	≥	0.0060
CMD.S.3.3	Space of rectangular ALL_CMD edge [ALL_CMD length ≤ 0.076 μm, INSIDE MD] to VC [INTERACT MD] [PRL > 0 μm, INSIDE PO_P76] (VC [INTERACT MD] overlap ALL_CMD is not allowed)	S3	≥	0.0060
CMD.S.4.1	Space of concave corner ALL_CMD edge [INSIDE ALL_MD] to {VC [INTERACT ALL_MD] OR ALL_OD} in vertical direction (Except FB_9, FB_8) DRC flags {VC OR ALL_OD} overlap Concave_CMD_Area [INTERACT {ALL_MD NOT ALL_CMD}] Definition of Concave_CMD_Area: A rectangle [0.057 μm x 0.025 μm] abut both edge of ALL_CMD concave corner [vertical edge length between two consecutive 270-90 degree corners ≤ 0.040 μm]	S4A	≥	0.0250

Rule No.	Description	Label	Op.	Rule
CMD.S.4.2	<p>Space of concave corner ALL_CMD edge [INSIDE ALL_MD] to {VC [INTERACT ALL_MD] OR ALL_OD} in vertical direction (Except FB_9, FB_8)</p> <p>DRC flags {VC OR ALL_OD} overlap Concave_CMD_Area2 [INTERACT {ALL_MD NOT ALL_CMD}]</p> <p>Definition of Concave_CMD_Area2: A rectangle [0.057 μm x 0.040 μm] abut both edge of ALL_CMD concave corner [vertical edge length between two consecutive 270-90 degree corners > 0.040 μm]</p>	S4B	≥	0.0400
CMD.S.4.3	<p>Space of concave corner ALL_CMD edge [INSIDE ALL_MD] to {VC [INTERACT ALL_MD] OR ALL_OD} in vertical direction [INSIDE PO_P63] (Except FB_9, FB_8)</p> <p>DRC flags {VC OR ALL_OD} overlap Concave_CMD_Area [INTERACT {ALL_MD NOT ALL_CMD}]</p> <p>Definition of Concave_CMD_Area: A rectangle [0.063 μm x 0.025 μm] abut both edge of ALL_CMD concave corner [vertical edge length between two consecutive 270-90 degree corners ≤ 0.040 μm]</p>	S4A	≥	0.0250
CMD.S.4.4	<p>Space of concave corner ALL_CMD edge [INSIDE ALL_MD] to {VC [INTERACT ALL_MD] OR ALL_OD} in vertical direction [INSIDE PO_P63] (Except FB_9, FB_8)</p> <p>DRC flags {VC OR ALL_OD} overlap Concave_CMD_Area [INTERACT {ALL_MD NOT ALL_CMD}]</p> <p>Definition of Concave_CMD_Area: A rectangle [0.063 μm x 0.040 μm] abut both edge of ALL_CMD concave corner [vertical edge length between two consecutive 270-90 degree corners > 0.040 μm]</p>	S4B	≥	0.0400
CMD.S.4.5	<p>Space of concave corner ALL_CMD edge [INSIDE ALL_MD] to {VC [INTERACT ALL_MD] OR ALL_OD} in vertical direction [INSIDE PO_P76]</p> <p>DRC flags {VC OR ALL_OD} overlap Concave_CMD_Area [INTERACT {ALL_MD NOT ALL_CMD}]</p> <p>Definition of Concave_CMD_Area: A rectangle [0.076 μm x 0.025 μm] abut both edge of ALL_CMD concave corner [vertical edge length between two consecutive 270-90 degree corners ≤ 0.040 μm]</p>	S4A	≥	0.0250
CMD.S.4.6	<p>Space of concave corner ALL_CMD edge [INSIDE ALL_MD] to {VC [INTERACT ALL_MD] OR ALL_OD} in vertical direction [INSIDE PO_P76]</p> <p>DRC flags {VC OR ALL_OD} overlap Concave_CMD_Area [INTERACT {ALL_MD NOT ALL_CMD}]</p> <p>Definition of Concave_CMD_Area: A rectangle [0.076 μm x 0.040 μm] abut both edge of ALL_CMD concave corner [vertical edge length between two consecutive 270-90 degree corners > 0.040 μm]</p>	S4B	≥	0.0400
CMD.S.5	Space of ALL_CMD to {SRM (50;0) OR {FB_9 OR FB_8}} (ALL_CMD CUT {SRM (50;0) OR {FB_9 OR FB_8}} is not allowed)	S5	≥	0.1080

Rule No.	Description	Label	Op.	Rule
CMD.S.6	Space of CMD_Concave_Corner in horizontal direction [PRL > -0.100 μm] (Except FB_9, FB_8) Definitions: 1. CMD_Concave_Corner: A rectangle [0.001 μm x 0.001 μm] abut both edge of ALL_CMD concave corner	S6	>	0.0570
CMD.EX.1	ALL_CMD extension on ALL_MD [width = 0.024 μm] in horizontal direction	EX1	\geq	0.0150
CMD.EX.1.1	ALL_CMD extension on ALL_MD [width = 0.030 μm] in horizontal direction (Except PO_P76)	EX1A	\geq	0.0350
CMD.EX.1.2	ALL_CMD extension on ALL_MD [width = 0.030 μm] in horizontal direction [INSIDE PO_P76]	EX1A	\geq	0.0230
CMD.EX.2	ALL_CMD extension on ALL_MD [width = 0.024 μm] in vertical direction (Except FB_9, FB_8)	EX2	\geq	0.0250
CMD.EX.2.1	ALL_CMD extension on ALL_MD [width = 0.030 μm] in vertical direction	EX2A	\geq	0.0280
CMD.O.1	ALL_CMD overlap of ALL_MD [width = 0.024 μm] in vertical direction (Except following conditions: 1. ALL_CMD overlap of ALL_MD [width = 0.024 μm] = 0.005 μm inside CCP_9)	O1	\geq	0.0150
CMD.O.2	ALL_CMD overlap of ALL_MD [width = 0.030 μm] in vertical direction	O2	\geq	0.0280
CMD.L.1	Length of ALL_CMD [width = 0.040/0.070/0.100 μm] in horizontal direction (Except FB_9, FB_8)	L1	\geq	0.1140
CMD.L.1.1	Length of ALL_CMD [width = 0.056 μm] in horizontal direction (Except FB_9, FB_8, PO_P63, PO_P76)	L1	=	0.0570, \geq 0.1140
CMD.L.1.1.1	Length of ALL_CMD [width = 0.056 μm] in horizontal direction [INSIDE PO_P63] (Except FB_9, FB_8)	L1	=	0.0630, \geq 0.1260
CMD.L.1.1.2	Length of ALL_CMD [width = 0.056 μm] in horizontal direction [INSIDE PO_P76]	L1	=	0.0760, \geq 0.1520
CMD.L.2	Horizontal edge length of ALL_CMD between two consecutive 270-270 degree corners (U-shape), or two consecutive 90-90 degree corners (T-shape), or two consecutive 90-270 degree corners (L-shape) (Except FB_9, FB_8)	L2	\geq	0.1140
CMD.L.3	Z-shape ALL_CMD length in horizontal direction (Except FB_9, FB_8) DRC flags space between 2 vertical CMD edge between 90-270 degree corners in horizontal direction < 0.1140 μm [PRL > -0.100 μm]	L3	\geq	0.1140
CMD.L.4	Vertical edge length of ALL_CMD between two consecutive 270-90 degree corners	L4	\leq	0.0560
CMD.DN.1	Maximum {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}} density in window 10 μm x 10 μm , stepping 5 μm (Except TCDDMY, ICOVL_SINGLE, FB_9, FB_8)		\leq	50%
CMD.DN.1.1	Minimum {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}} density in window 10 μm x 10 μm , stepping 5 μm (Except TCDDMY, ICOVL_SINGLE, SEALRING_ALL, RH_TNB, VAR, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	5%
CMD.R.1	Vertical edge of ALL_CMD must abut centerline of ALL_PO in horizontal direction (Except Dummy_Cell)			

Rule No.	Description	Label	Op.	Rule
CMD.R.2	{ALL_CMD OR BCMD} must be a rectangle orthogonal to grid or L-, T-, U-, Z- or combined L/T/U/Z shape. Horizontal_T_Shape is not allowed (Except FB_8) Definition of Horizontal_T_Shape: 2 vertical edge at the same vertical line			
CMD.R.2.1	SR_DCMD must be a rectangle orthogonal to grid			
CMD.R.2.2	H-shape, horizontal T-shape is not allowed (Except FB_8) DRC flags 2 vertical edge at the same vertical line			
CMD.R.4	ALL_CMD point touch of corners is not allowed (Except FB_8)			
CMD.R.5	Any vertex of ALL_CMD inside ALL_MD is not allowed			
CMD.R.6.3	SR_DCMD interact MD, or CMD is not allowed			
CMD.R.7	{ALL_MD AND ALL_OD} overlap ALL_CMD is not allowed			
CMD.R.8	{ALL_CMD OR BCMD} cut CCP_9, CCP_8 is not allowed			
CMD.R.9	Rectangular ALL_CMD [length = 0.057 μm] interact ALL_MP is not allowed			
CMD.R.9.1	Rectangular ALL_CMD [length ≤ 0.063 μm] interact ALL_MP is not allowed [INSIDE PO_P63]			
CMD.R.9.2	Rectangular ALL_CMD [length ≤ 0.076 μm] interact ALL_MP is not allowed [INSIDE PO_P76]			
CMD.R.10	ALL_CMD interact SRM (50;0) is not allowed			
CMD.G0.0	G0-SPACE definition: 1. G0 X space (G0XS) of ALL_CMD < 0.114 μm [PRL > -0.046 μm] 2. G0 Y space (G0YS) of ALL_CMD [width = 0.040/0.070/0.100 μm] < 0.074 μm [PRL > -0.057 μm] 3. G0 Y space (G0YS) of ALL_CMD to ALL_CMD [width = 0.056 μm] < 0.072 μm [PRL > -0.057 μm] 4. G0 Y space (G0YS) of ALL_CMD [width = 0.100 μm] < 0.084 μm [PRL > -0.057 μm] (Except FB_9, FB_8) G0-AREA definition: 1. G0 run-run area (G0RA): The projection area between 2 edges with G0XS/G0YS 2. G0-AREA is independent to all other ones, even if they are overlapped or crossed Loop: 1. A loop is formed when ALL_CMD polygons are connected in a cyclic sequence with G0-AREA in between 2. A loop cannot contain any sub-loops which share one or more polygons with it			
CMD.G0.1	G0-AREA cannot be formed by single polygon (Except FB_9, FB_8)			
CMD.G0.2	G0-AREA count of the close loop formed by original polygons and G0-AREAs cannot be odd number (Except FB_9, FB_8)			

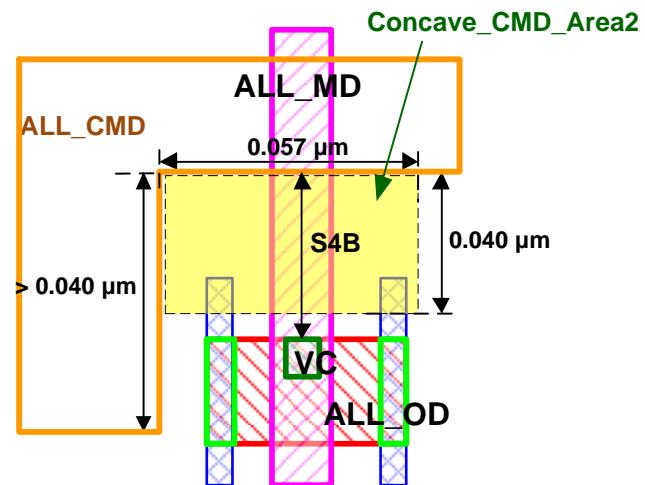
CMD



Definition of Concave_CMD_Area:

A rectangle [0.057 μm x 0.025 μm / 0.063 μm x 0.025 μm / 0.076 μm x 0.025 μm] abut both edge of ALL_CMD concave corner [vertical edge length between two consecutive 270-90 degree corners ≤ 0.040 μm]

CMD.S.4.1 / CMD.S.4.3 / CMD.S.4.5

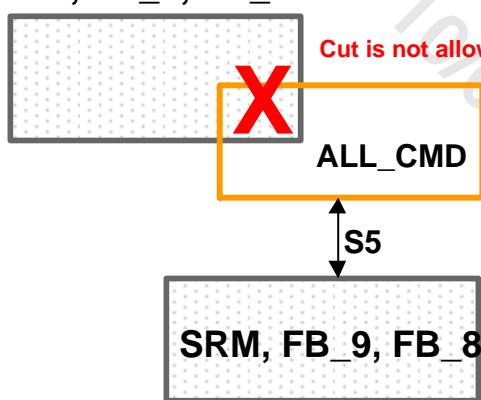


Definition of Concave_CMD_Area2:

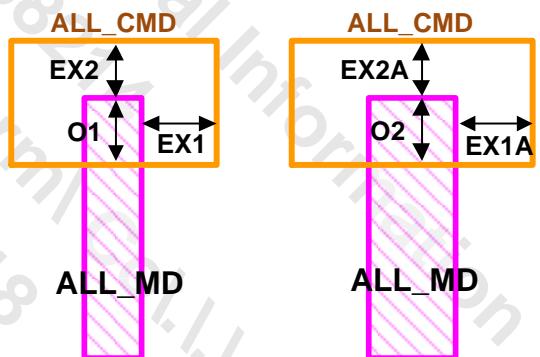
A rectangle [0.057 μm x 0.040 μm / 0.063 μm x 0.040 μm / 0.076 μm x 0.040 μm] abut both edge of ALL_CMD concave corner [vertical edge length between two consecutive 270-90 degree corners > 0.040 μm]

CMD.S.4.2 / CMD.S.4.4 / CMD.S.4.6

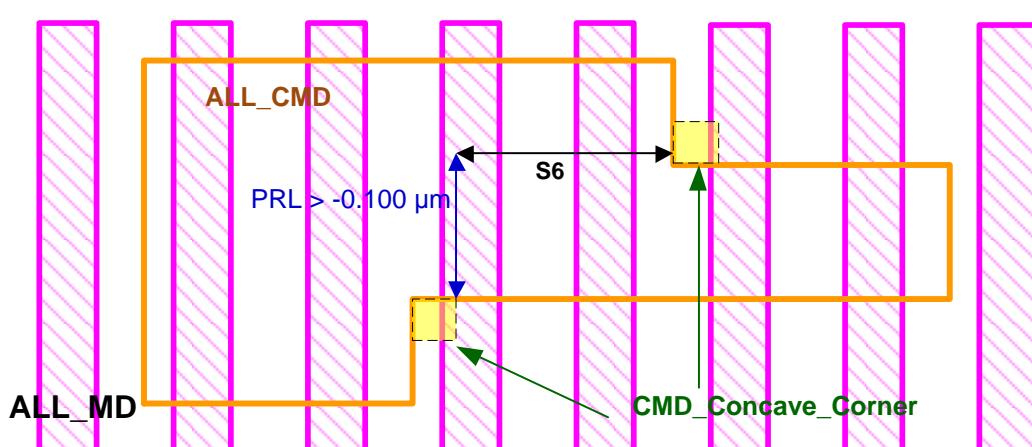
SRM, FB_9, FB_8



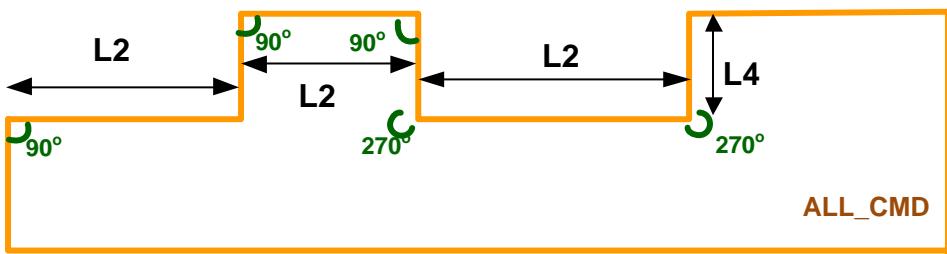
CMD.S.5



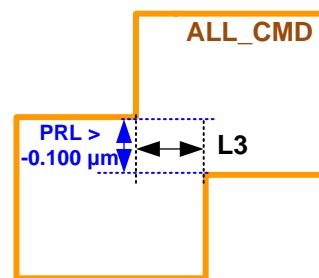
CMD.EX.1 / CMD.EX.1.1 / CMD.EX.1.2 / CMD.EX.2 / CMD.EX.2.1 / CMD.O.1 / CMD.O.2



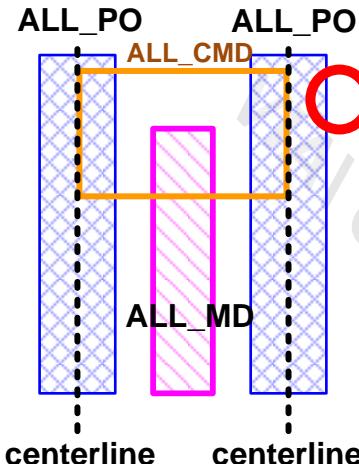
CMD.S.6



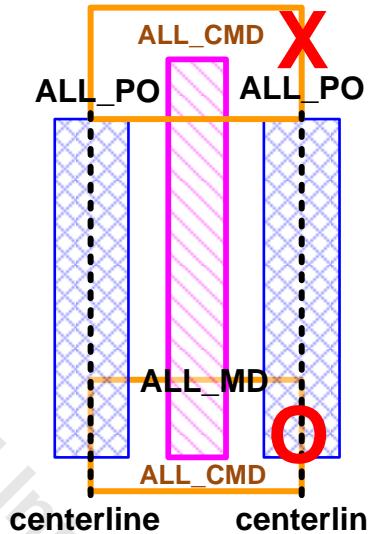
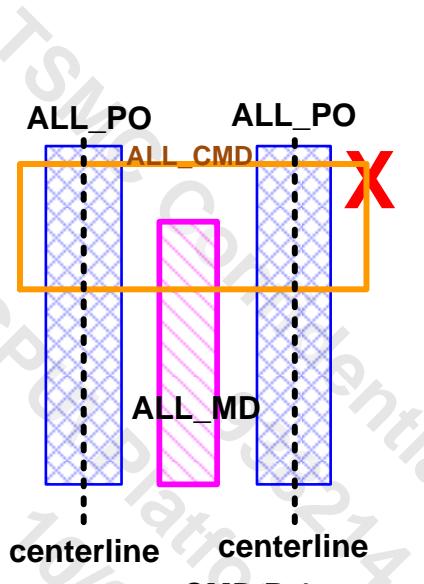
CMD.L.2 / CMD.L.4



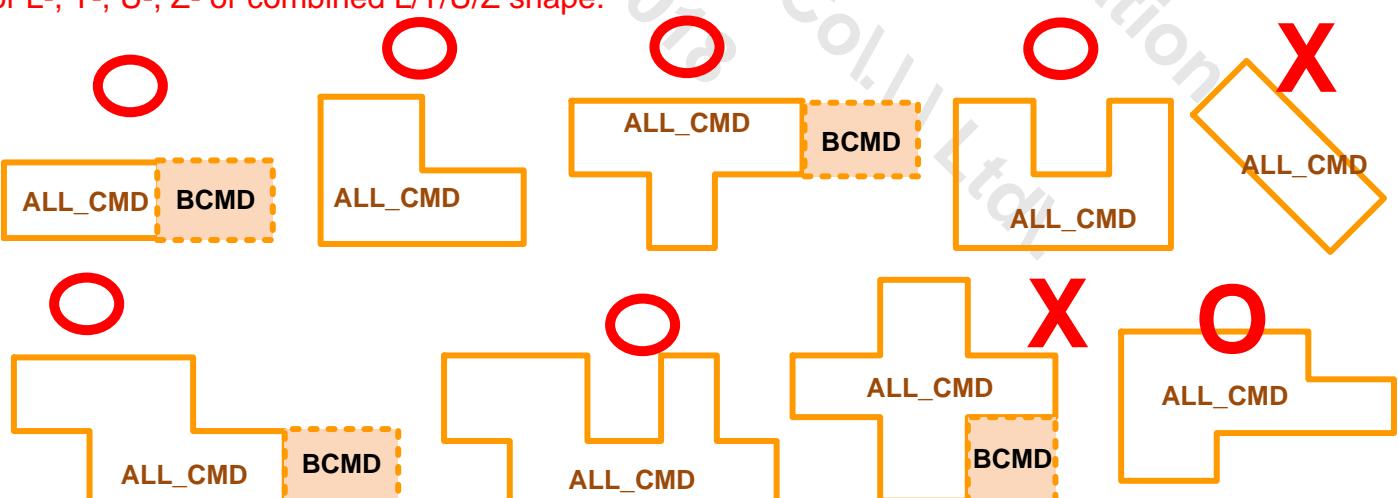
CMD.L.3



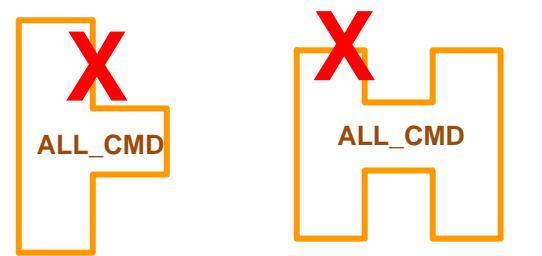
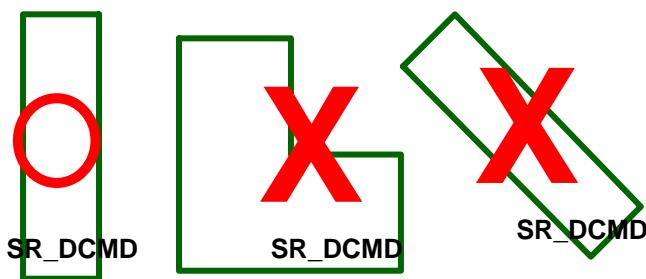
CMD.R.1



{ALL_CMD OR BCMD} must be a rectangle orthogonal to grid or L-, T-, U-, Z- or combined L/T/U/Z shape.



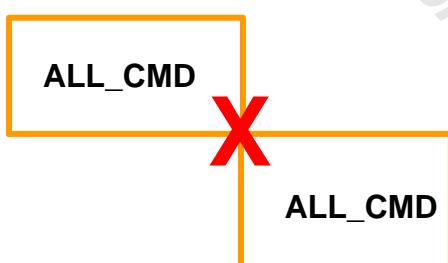
CMD.R.2



CMD.R.2.1

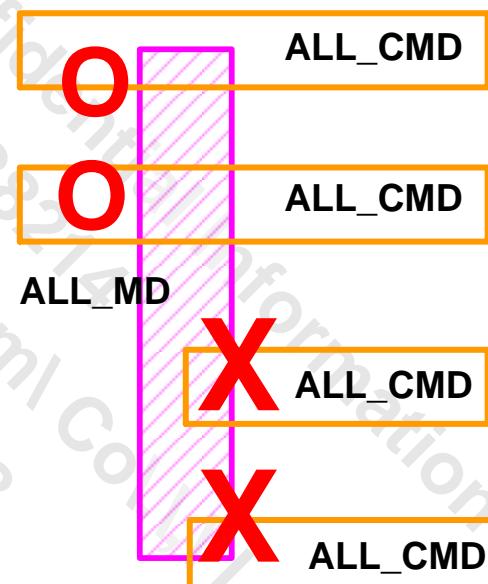
H-shape, horizontal T-shape is not allowed

CMD.R.2.2



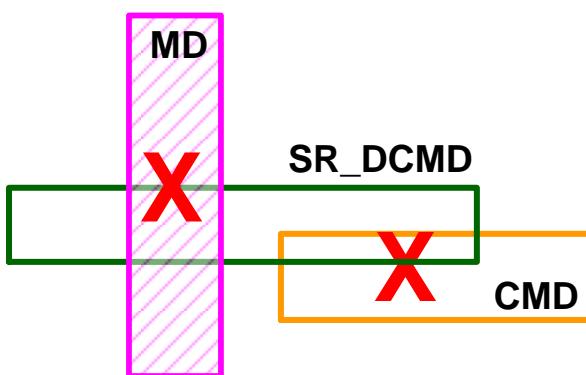
ALL_CMD point touch is not allowed

CMD.R.4

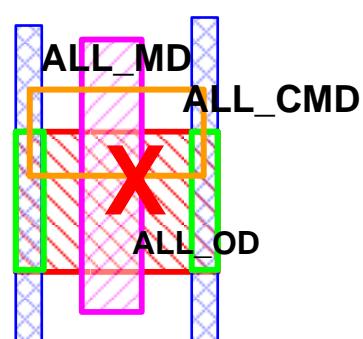


Any vertex of ALL_CMD inside ALL_MD is not allowed

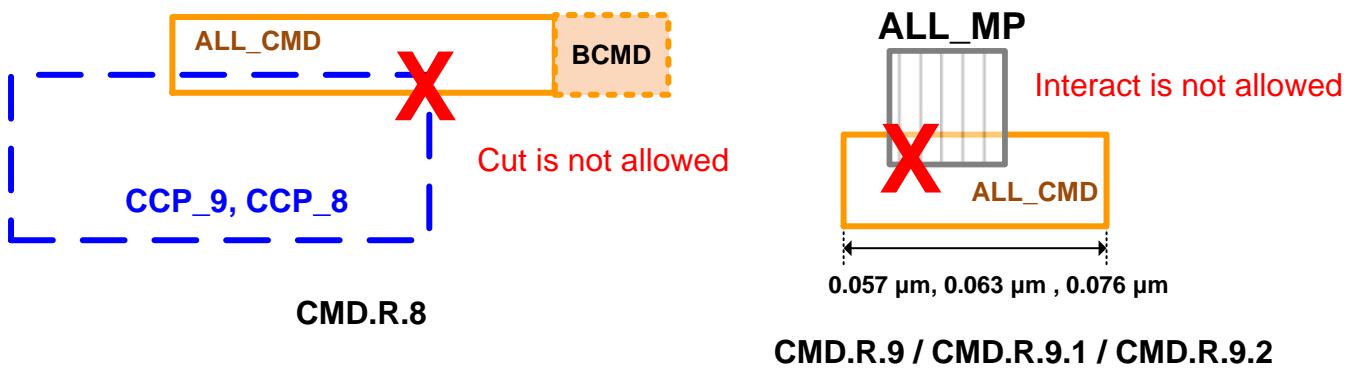
CMD.R.5



CMD.R.6.3

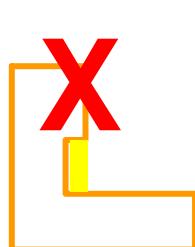
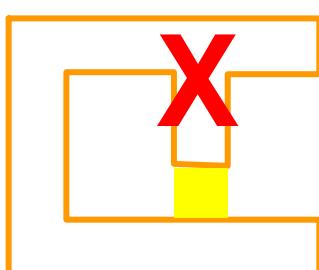
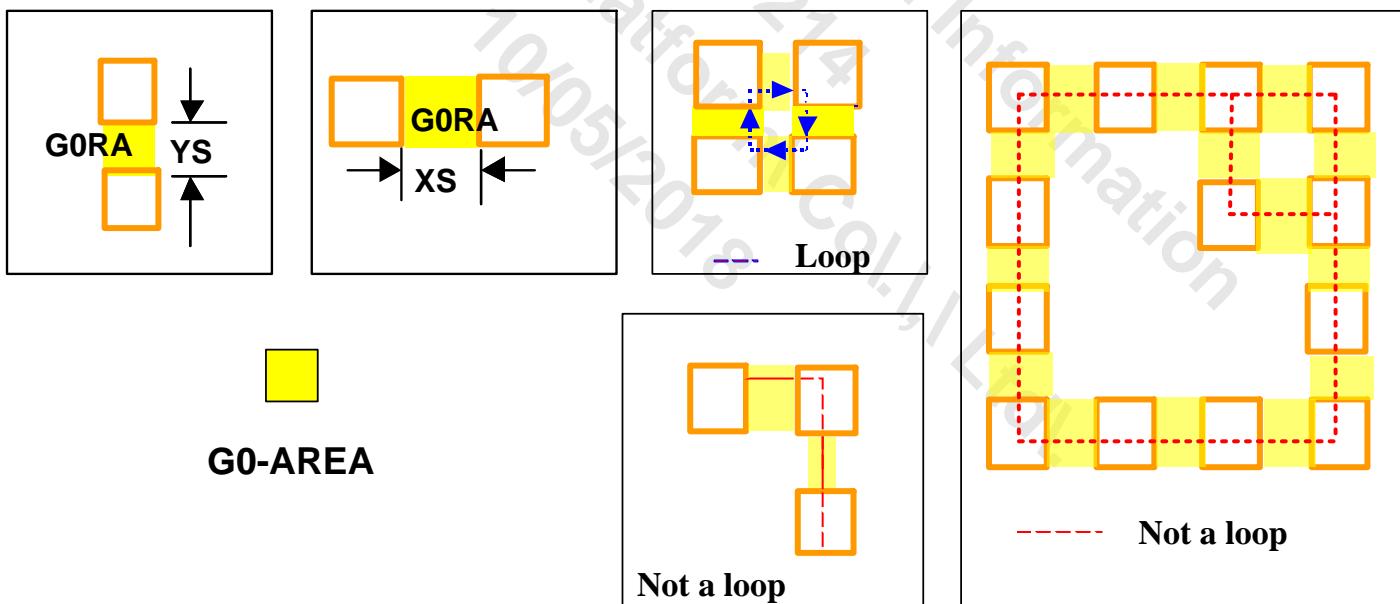


CMD.R.7

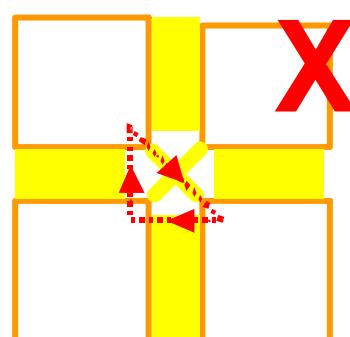


ALL CMD INTERACT SRM is not allowed

CMD.R.10



CMD.G0.0



CMD.G0.1

CMD.G0.2

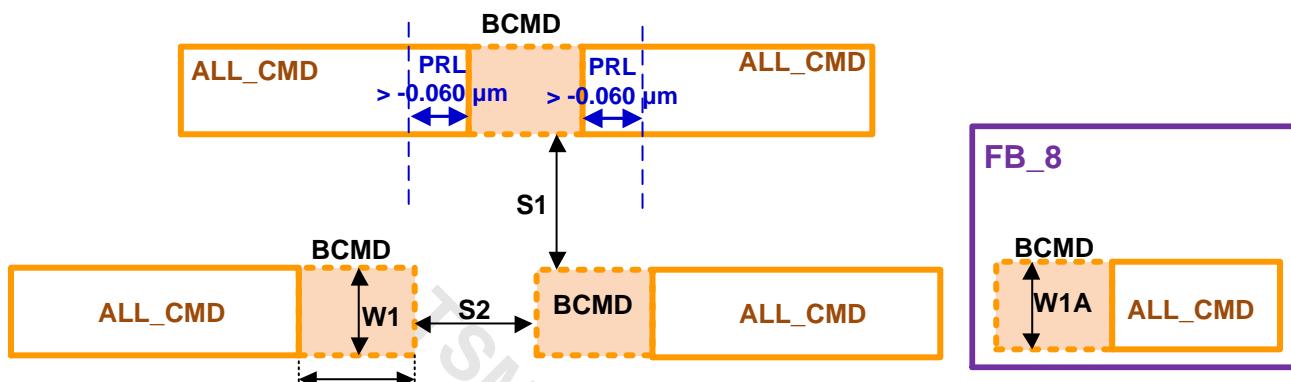
4.5.35 Butted CMD (BCMD) Layout Rules

BCMD (CAD layer: 84;160) is a tape-out layer, and it can be used as an interconnection layer between CMD at STD cell boundary.

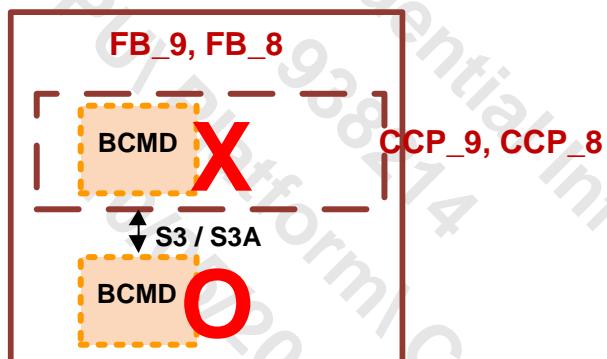
Two CMD edges interact the same BCMD after cell placement will be merged to one CMD during mask making process in TSMC.

Rule No.	Description	Label	Op.	Rule
BCMD.W.1	Width of BCMD in vertical direction (Except FB_8)	W1	=	0.0960
BCMD.W.1.1	Width of BCMD in vertical direction [INSIDE FB_8]	W1A	=	0.1360
BCMD.S.1	Space of BCMD in vertical direction [PRL > -0.060 μm]	S1	≥	0.0670
BCMD.S.2	Space of BCMD	S2	≥	0.0570
BCMD.S.3	Space of BCMD to CCP_9, CCP_8 in vertical direction	S3	=	0.0420
BCMD.L.1	Length of BCMD in horizontal direction (Except PO_P63)	L1	=	0.0570, 0.1000, 0.1140, 0.1710
BCMD.L.1.1	Length of BCMD in horizontal direction [INSIDE PO_P63]	L1	=	0.0630, 0.1260, 0.1890
BCMD.R.1	BCMD must be inside {FB_9 NOT CCP_9}, {FB_8 NOT CCP_8}			
BCMD.R.2	BCMD horizontal edge interact CMD is not allowed			
BCMD.R.4	BCMD must be a rectangle orthogonal to grid			
BCMD.R.5	BCMD overlap ALL_CMD is not allowed			
BCMD.R.6	Both {{MD NOT CMD} [intersect by BCMD] NOT BCMD} interact MP, or VC at the same time is not allowed.			

BCMD

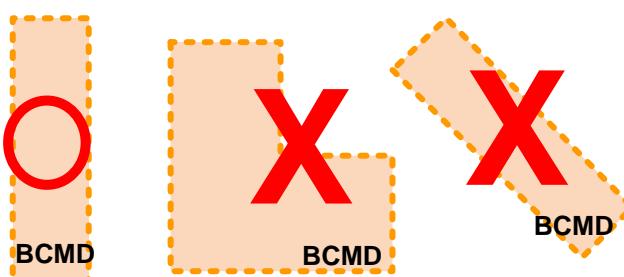


BCMD.W.1 / BCMD.W.1.1 / BCMD.S.1 / BCMD.S.2 / BCMD.L.1 / BCMD.L.1.1



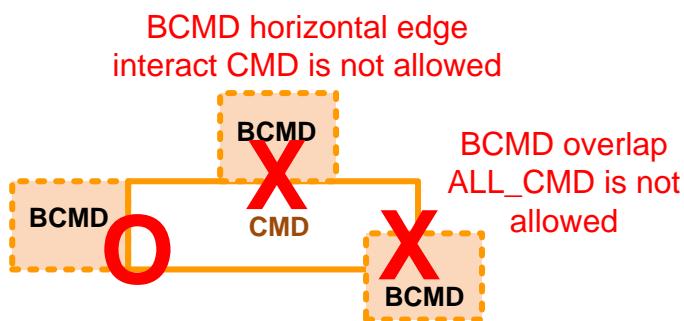
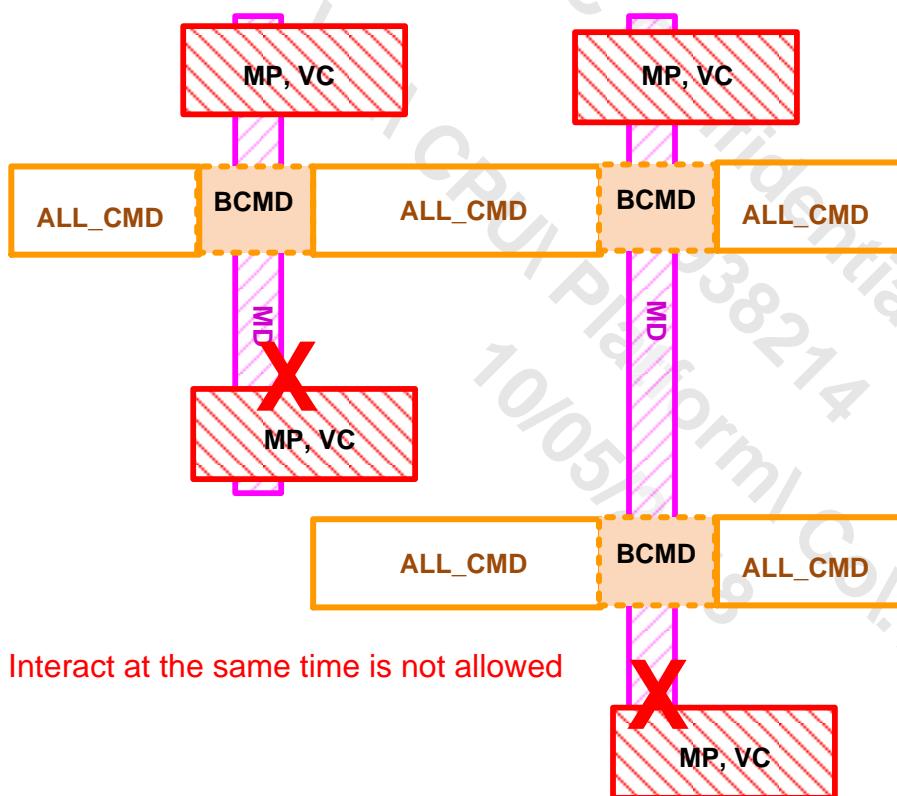
BCMD must be inside {FB_9 NOT CCP_9}, {FB_8 NOT CCP_8}

BCMD.S.3 / BCMD.R.1



BCMD must be a rectangle orthogonal to grid.

BCMD.R.4

**BCMD.R.2 / BCMD.R.5****BCMD.R.6**

4.5.36 MP Layout Rules

MP (CAD layer: 84;2) can be used as an interconnection layer between PO, MD, and VC.
 $\text{ALL_MP} = \{\text{MP OR SR_DMP}\}$

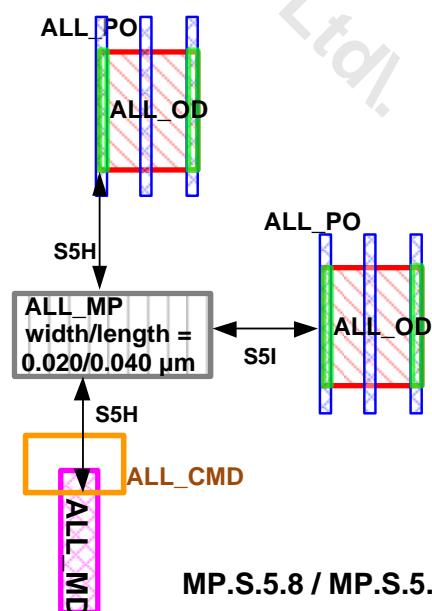
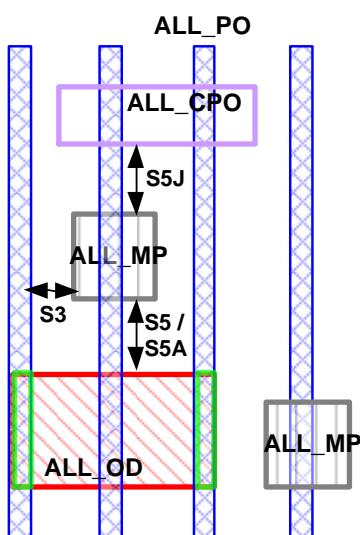
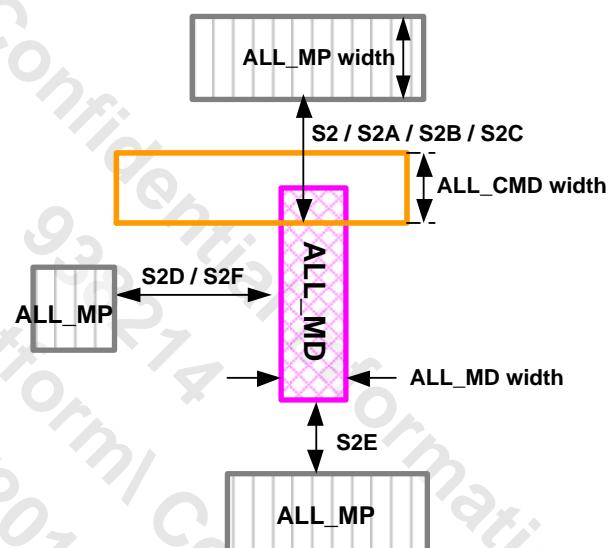
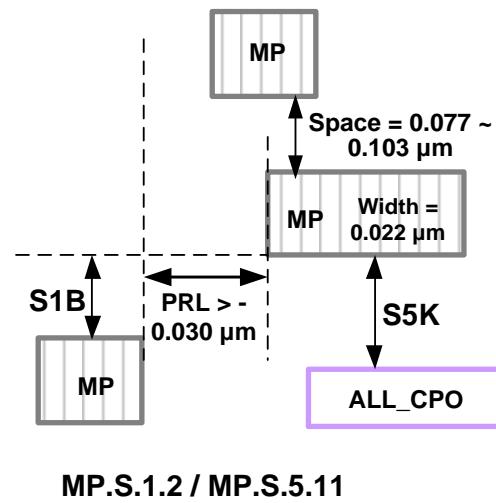
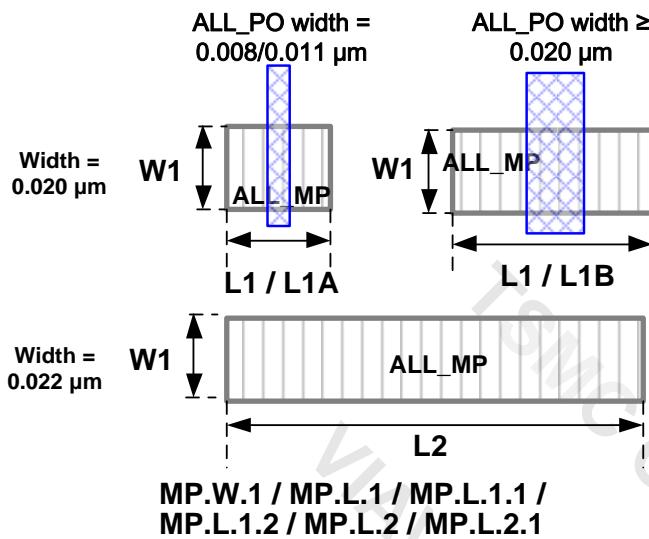
Rule No.	Description	Label	Op.	Rule
MP.W.1	Width of ALL_MP in vertical direction	W1	=	0.0200, 0.0220
MP.S.1	Space of ALL_MP (Except BLK_WF)	S1	\geq	0.0370
MP.S.1.1	Space of ALL_MP to rectangular ALL_MP (Except BLK_WF, FB_9, FB_8)	S1A	\geq	0.0430
MP.S.1.2	Space of long side of rectangular ALL_MP [width = 0.022 μm , the other side space to square ALL_MP = 0.077 ~ 0.103 μm , PRL > -0.030 μm] to square ALL_MP [PRL > -0.030 μm]	S1B	\geq	0.1200
MP.S.2	Space of ALL_MP to {ALL_MD NOT ALL_CMD} (Except BLK_WF)	S2	\geq	0.0180
MP.S.2.1	Space of ALL_MP to {{ALL_MD NOT ALL_CMD} line-end [INTERACT ALL_CMD width = 0.040 μm } (Except BLK_WF, FB_8)}	S2A	\geq	0.0250
MP.S.2.2	Space of ALL_MP to {ALL_MD [width = 0.030 μm] NOT ALL_CMD} (Except BLK_WF)	S2B	\geq	0.0250
MP.S.2.3	Space of ALL_MP [width = 0.022 μm] to {ALL_MD NOT ALL_CMD} (Except BLK_WF)	S2C	\geq	0.0250
MP.S.2.4	Space of ALL_MP [width = 0.022 μm] to {ALL_MD NOT ALL_CMD} in horizontal direction [PRL > -0.025 μm] (Except BLK_WF)	S2D	\geq	0.0450
MP.S.2.5	Space of ALL_MP to ALL_MD [short side NOT INTERACT ALL_CMD] (Except BLK_WF)	S2E	\geq	0.0300
MP.S.2.6	Space of ALL_MP to {ALL_MD NOT ALL_CMD} in horizontal direction [PRL > -0.018 μm] (Except BLK_WF)	S2F	\geq	0.0420
MP.S.2.7	Space of ALL_MP to {ALL_MD NOT ALL_CMD} in vertical direction (Except FB_9, FB_8) DRC flags MP overlap Convex_CMD_Area [INTERACT {ALL_MD NOT ALL_CMD}] Definition of Convex_CMD_Area: A rectangle [0.057 μm x 0.038 μm] abut both edge of ALL_CMD convex corner [vertical edge length between two consecutive 270-90 degree corners \leq 0.040 μm]	S2G	\geq	0.0380
MP.S.2.8	Space of ALL_MP to {ALL_MD NOT ALL_CMD} in vertical direction (Except FB_9, FB_8) DRC flags MP overlap Convex_CMD_Area2 [INTERACT {ALL_MD NOT ALL_CMD}] Definition of Convex_CMD_Area2: A rectangle [0.057 μm x 0.053 μm] abut both edge of ALL_CMD convex corner [vertical edge length between two consecutive 270-90 degree corners $>$ 0.040 μm]	S2H	\geq	0.0530
MP.S.3	Space of ALL_MP to ALL_PO (Except BLK_WF, or following conditions: 1. small ALL_PO jog \leq 0.002 μm)	S3	\geq	0.0230
MP.S.3.1	Space of SR_DMP [width = 0.022 μm] to PO [width \geq 0.020 μm]	S3A	\geq	0.0300
MP.S.5	Space of ALL_MP to ALL_OD (Except BLK_WF, Dummy_Cell)	S5	\geq	0.0200
MP.S.5.1	Space of ALL_MP to ALL_OD (Except FB_9, FB_8, BLK_WF, Dummy_Cell)	S5A	\geq	0.0230

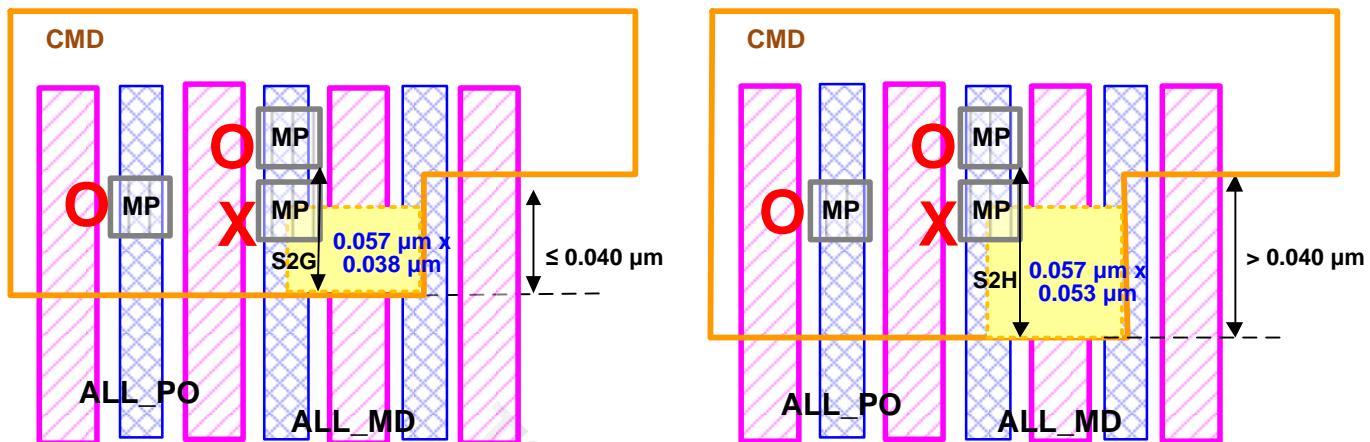
Rule No.	Description	Label	Op.	Rule
MP.S.5.8	Space of rectangular ALL_MP [width/length = 0.020/0.040 μm] to {{ALL_MD NOT ALL_CMD} OR ALL_OD} in vertical direction [PRL > - 0.018 μm] (Overlap is not allowed) (Except BLK_WF, Dummy_Cell)	S5H	≥	0.0500
MP.S.5.9	Space of rectangular ALL_MP [width/length = 0.020/0.040 μm] to ALL_OD in horizontal direction [PRL > - 0.018 μm] (Overlap is not allowed) (Except BLK_WF)	S5I	≥	0.0700
MP.S.5.10	Space of ALL_MP to ALL_CPO [INTERACT the same PO] in vertical direction (Except FB_9, FB_8)	S5J	≥	0.0200
MP.S.5.11	Space of rectangular ALL_MP [width = 0.022 μm] to ALL_CPO [INTERACT the same PO] in vertical direction [PRL > 0 μm]	S5K	≥	0.0230
MP.S.8	Space of ALL_MP to SRM (50;0) ({{ALL_MP CUT SRM (50;0)}} is not allowed)	S8	≥	0.1080
MP.S.8.1	Space of ALL_MP [NOT INSIDE FB_8] to ALL_MP [INSIDE FB_8] ({{ALL_MP CUT FB_8}} is not allowed)	S8A	≥	0.1080
MP.EN.0	1. Square MP landing on PO [width = 0.008/0.011 μm] is defined by MP.R.1 2. Rectangular MP [width/length = 0.020/0.040 μm] landing on PO [width = 0.020/0.036 μm] is defined by MP.R.1 and MP.EX.1.1 3. Rectangular MP [width/length = 0.020/0.040 μm] enclosure by PO [width ≥ 0.072 μm] is defined by MP.EN.1			
MP.EN.1	Long side of rectangular MP [width/length = 0.020/0.040 μm] enclosure by PO [width ≥ 0.072 μm, at least two opposite sides] with the other two sides ≥ 0.016 μm (Cut is not allowed)	EN1	≥	0.0240
MP.EX.1.1	Short side of PO [width = 0.036 μm] extension on rectangular MP [width/length = 0.020/0.040 μm] (Without CPO define, extension ≤ 0 μm is not allowed)	EX1A	≥	0.0570
MP.EX.2	Rectangular ALL_MP [width = 0.022 μm] extension on ALL_OD in vertical direction (Except BLK_WF)	EX2	≤	0.0010
MP.O.1	ALL_MP [width = 0.022 μm] overlap of {{ALL_MD [width = 0.024 μm] NOT ALL_CMD} AND ALL_OD} in horizontal direction (Except BLK_WF, Dummy_Cell, or following conditions: 1. {STRAP NOT VAR})	O1	=	0.0120
MP.L.1	Length of ALL_MP [width = 0.020 μm] in horizontal direction (Except BLK_WF)	L1	=	0.0200, 0.0400
MP.L.1.1	Length of ALL_MP [width = 0.020 μm, INTERACT ALL_PO [width = 0.008/0.011 μm]] in horizontal direction (Except BLK_WF)	L1A	=	0.0200
MP.L.1.2	Length of ALL_MP [width = 0.020 μm, INTERACT ALL_PO [width ≥ 0.020 μm]] in horizontal direction (Except Dummy_Cell)	L1B	=	0.0400
MP.L.2	Length of ALL_MP [width = 0.022 μm] in horizontal direction (Except BLK_WF, PO_P63)	L2	=	0.0570, 0.1140, 0.1710
MP.L.2.1	Length of ALL_MP [width = 0.022 μm] in horizontal direction [INSIDE PO_P63]	L2A	=	0.0630, 0.1260, 0.1890
MP.DN.1	Minimum ALL_MP density in window 125 μm x 125 μm, stepping 62.5 μm (Except NWDMY, LOGO, TCDDMY, ICOVL_SINGLE, RH_TNB, FB_9, FB_8, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	0.3%
MP.DN.1.1	Minimum {{ALL_MD NOT {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}} OR ALL_MP} density in window 125 μm x 125 μm, stepping 62.5 μm (Except TCDDMY, RH_TNB, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	5.3%
MP.DN.1.2	Minimum {{ALL_MD NOT {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}} OR ALL_MP} density in		≥	5%

Rule No.	Description	Label	Op.	Rule
	window 125 μm x 125 μm , stepping 62.5 μm (Except TCDDMY, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)			
MP.DN.2	Maximum ALL_MP density in window 20 μm x 20 μm , stepping 10 μm (Except TCDDMY, ICOVL_SINGLE)		\leq	18%
MP.DN.2.1	Maximum {{ALL_MD NOT {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}} OR ALL_MP} density in window 20 μm x 20 μm , stepping 10 μm (Except TCDDMY, ICOVL_SINGLE)		\leq	50%
MP.DN.2.2	Maximum {{ALL_MD NOT {ALL_CMD OR {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}} OR ALL_MP} density in window 25 μm x 25 μm , stepping 12.5 μm (Except TCDDMY, ICOVL_SINGLE)		\leq	36%
MP.R.1	MP [width = 0.020 μm] must be centered at centerline of PO [width \leq 0.036 μm] in horizontal direction (Except BLK_WF)			
MP.R.3	ALL_MP [width = 0.022 μm] interact VC [NOT INTERACT MD] is not allowed			
MP.R.5	ALL_MP must be a rectangle orthogonal to grid			
MP.R.7	MP [width = 0.022 μm] vertical edge must be at the centerline of MD [width = 0.024 μm] in horizontal direction (Except FB_9, BLK_WF)			
MP.R.8	ALL_MP must interact {ALL_PO NOT ALL_CPO} (Except DC9_1)			
MP.R.8.1	ALL_MP [width = 0.022 μm] must interact ALL_OD, ALL_PO, and ALL_MD (Except BLK_WF, DC9_1)			
MP.R.8.2	SR_DMP cut PO is not allowed			
MP.R.10	{}{{Semi-ISO-PO OR Next-Semi-ISO-PO} NOT CPO} interact MP is not allowed (Except BLK_WF) {}{{Semi-ISO-PO OR Next-Semi-ISO-PO} NOT CPO} is defined by segment Semi-ISO-PO : ALL_PO [width \leq 0.036 μm , one side poly space $>$ 0.080 μm] Next-Semi-ISO-PO : ALL_PO space to Semi-ISO-PO \leq 0.080 μm			
MP.R.11	{MP INTERACT {{{{SR_DPO NOT SR_DCPO} OR SR_DMD} OR ALL_CPO} OR SR_DMP}} is not allowed			
MP.R.11.1	ALL_MP [width = 0.020 μm] overlap ALL_OD, or ALL_MD is not allowed (Except BLK_WF)			
MP.G0.0	G0-SPACE definition: 1. G0 space (G0S) of ALL_MP [width/length = 0.020/0.020 μm] $<$ 0.088 μm [PRL $>$ -0.024 μm] 2. G0 corner-corner space (G0CS) of ALL_MP [width/length = 0.020/0.020 μm] $<$ 0.083 μm [PRL \leq -0.024 μm] 3. G0 space (G0S) of ALL_MP [width/length = 0.020/0.040 μm] to ALL_MP $<$ 0.104 μm [PRL $>$ -0.030 μm] 4. G0 corner-corner space (G0CS) of ALL_MP [width/length = 0.020/0.040 μm] to ALL_MP $<$ 0.104 μm [PRL \leq -0.030 μm] 5. G0 space (G0S) of short side of ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm and 0.022/0.171 μm] to ALL_MP [width/length = 0.020/0.020 μm] $<$ 0.108 μm [PRL $>$ -0.030 μm] 6. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm] to ALL_MP [width/length = 0.020/0.020 μm] $<$ 0.077 μm [PRL $>$ -0.030 μm] 7. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.171 μm] to ALL_MP [width/length = 0.020/0.020 μm] $<$ 0.117 μm [PRL $>$ -0.030 μm] 8. G0 corner-corner space (G0CS) of ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm and 0.022/0.171 μm] to ALL_MP [width/length = 0.020/0.020 μm] $<$ 0.078 μm [PRL \leq -0.030 μm] 9. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm] to ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm] $<$ 0.104 μm [PRL $>$ -0.030 μm] (Except FB_8) 10. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm] to ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm]			

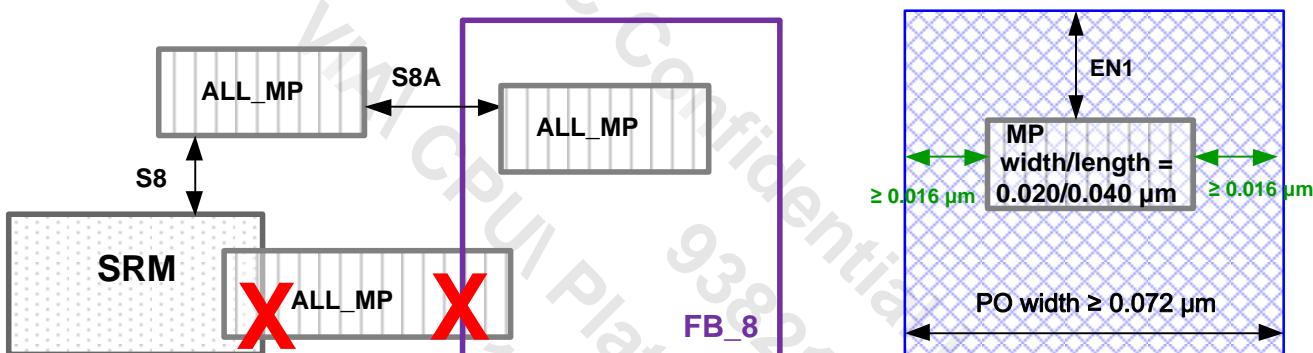
Rule No.	Description	Label	Op.	Rule	
	<p>$\mu\text{m}] < 0.082 \mu\text{m}$ [PRL > -0.030 μm] [INSIDE FB_8]</p> <p>11. G0 space (G0S) of short side of ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm and 0.022/0.171 μm] to ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm and 0.022/0.171 μm] < 0.108 μm [PRL > -0.030 μm]</p> <p>12. G0 corner-corner space (G0CS) of ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm and 0.022/0.171 μm] to ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm and 0.022/0.171 μm] < 0.082 μm [PRL ≤ -0.030 μm]</p> <p>13. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.171 μm] to ALL_MP [width/length = 0.022/0.057 μm and 0.022/0.114 μm and 0.022/0.171 μm] < 0.134 μm [PRL > -0.030 μm]</p> <p>14. G0 space (G0S) of short side of ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm and 0.022/0.189] to ALL_MP [width/length = 0.020/0.020 μm] < 0.150 μm [PRL > -0.030 μm]</p> <p>15. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm] to ALL_MP [width/length = 0.020/0.020 μm] < 0.077 μm [PRL > -0.030 μm]</p> <p>16. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.189 μm] to ALL_MP [width/length = 0.020/0.020 μm] < 0.117 μm [PRL > -0.030 μm]</p> <p>17. G0 corner-corner space (G0CS) of ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm and 0.022/0.189 μm] to ALL_MP [width/length = 0.020/0.020 μm] < 0.092 μm [PRL ≤ -0.030 μm]</p> <p>18. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm] to ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm] < 0.104 μm [PRL > -0.030 μm] (Except FB_8)</p> <p>19. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm] to ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm] < 0.082 μm [PRL > -0.030 μm] [INSIDE FB_8]</p> <p>20. G0 space (G0S) of short side of ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm and 0.022/0.189 μm] to ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm and 0.022/0.189 μm] < 0.126 μm [PRL > -0.030 μm]</p> <p>21. G0 corner-corner space (G0CS) of ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm and 0.022/0.189 μm] to ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm and 0.022/0.189 μm] < 0.088 μm [PRL ≤ -0.030 μm]</p> <p>22. G0 space (G0S) of long side of ALL_MP [width/length = 0.022/0.189 μm] to ALL_MP [width/length = 0.022/0.063 μm and 0.022/0.126 μm and 0.022/0.189 μm] < 0.134 μm [PRL > -0.030 μm]</p> <p>G0-AREA definition:</p> <ol style="list-style-type: none"> 1. G0 run-run area (G0RA): The projection area between 2 space with G0S 2. G0 corner-corner area (G0CA): The area between two corners with G0CS 3. G0-AREA is independent to all other ones, even if they are overlapped or crossed <p>Loop:</p> <ol style="list-style-type: none"> 1. A loop is formed when ALL_MP polygons are connected in a cyclic sequence with G0-AREA in between 2. A loop cannot contain any sub-loops which share one or more polygons with it 				
MP.G0.1	G0-AREA cannot be formed by single polygon				
MP.G0.2	G0CA cannot cross another G0CA or touch another G0RAs				
MP.G0.3	G0-AREA count of the close loop formed by original polygons and G0-AREAs cannot be odd number				

MP



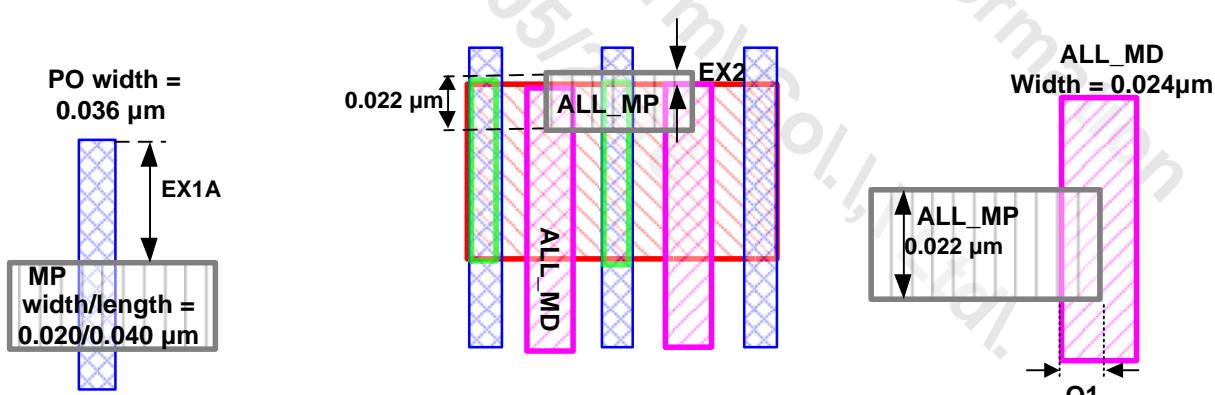


MP.S.2.7 / MP.S.2.8



MP.S.8 / MP.S.8.1

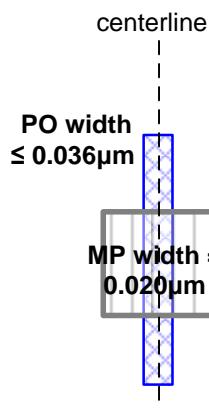
MP.EN.1



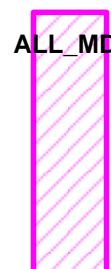
MP.EX.1.1

MP.EX.2

MP.O.1

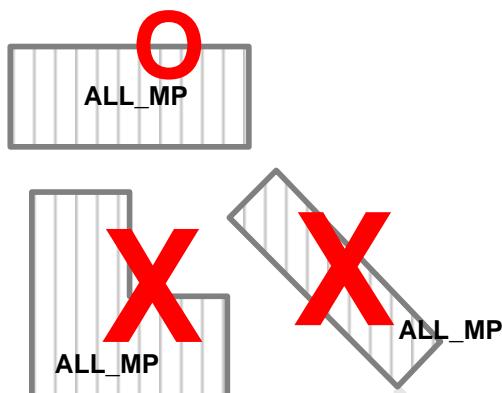


MP.R.1

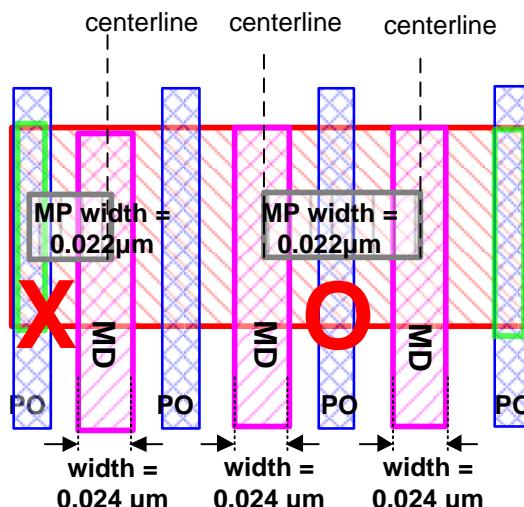


MP [width = 0.022 μm] interact with VC [NOT INTERACT MD] is not allowed.

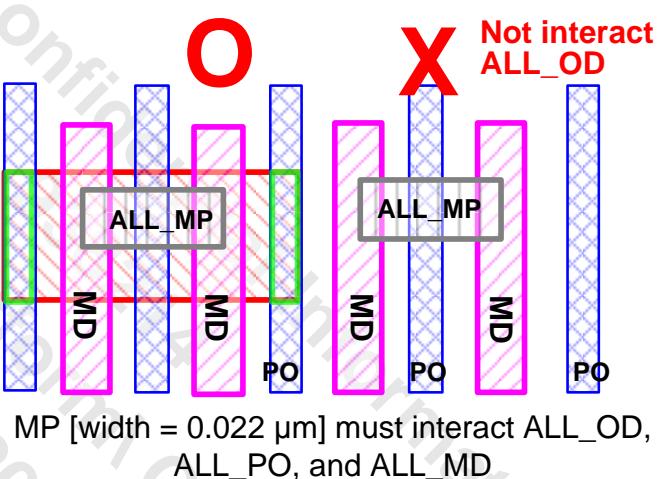
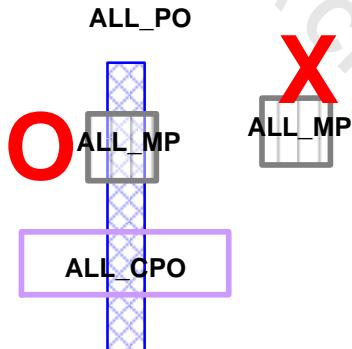
MP.R.3



ALL_MP must be a rectangle orthogonal to grid

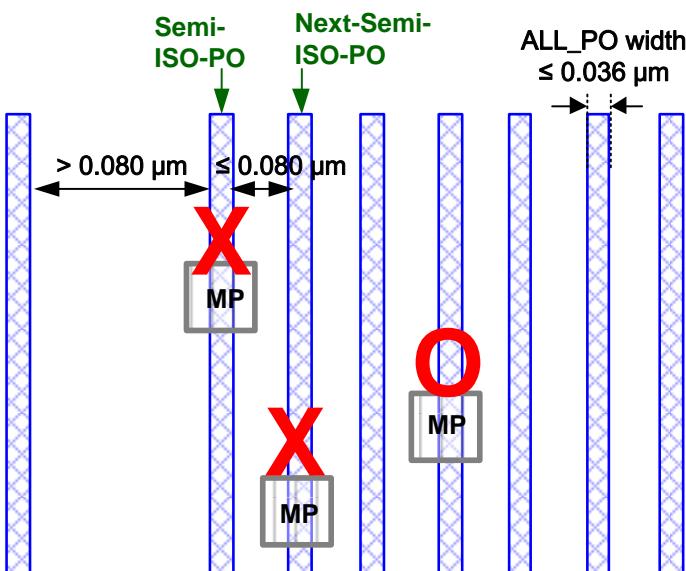


MP.R.5

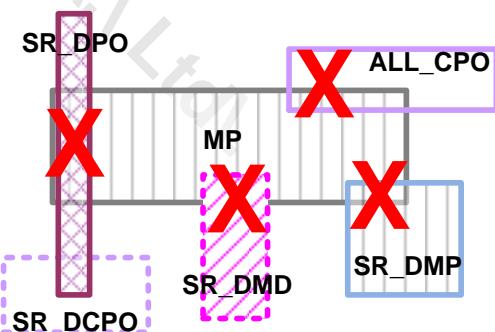


MP [width = 0.022 μm] must interact ALL_OD, ALL_PO, and ALL_MD

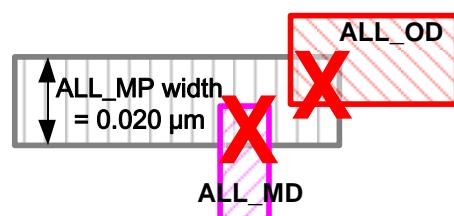
MP.R.8



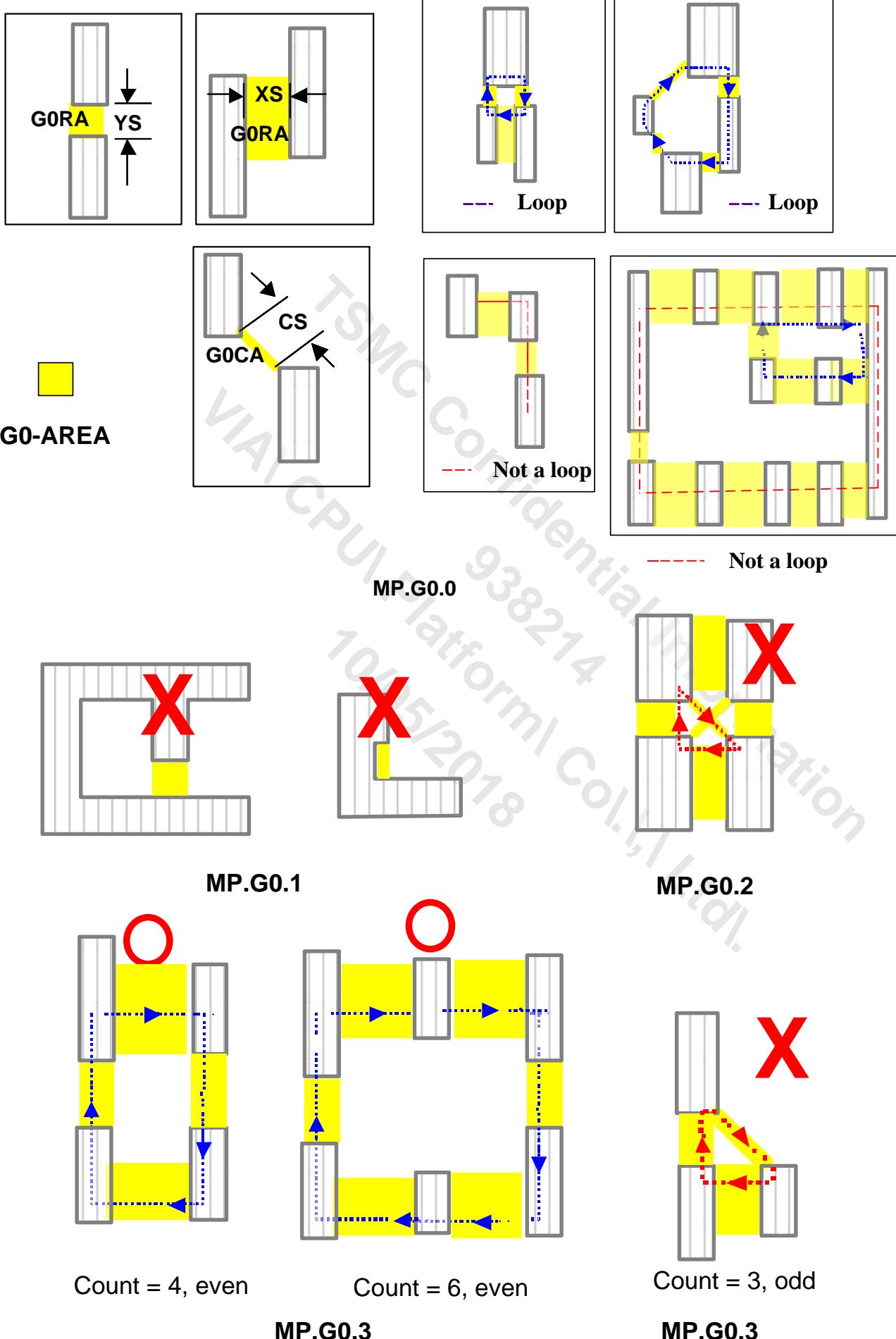
MP.R.10



MP.R.11



MP.R.11.1



4.5.37 VC Layout Rules

VC (CAD layer: 179;400) is used as Via Contact hole between MP and M0, or MD and M0.

Rule No.	Description	Label	Op.	Rule
VC.DEF.1	The following definitions are used for VC rules 1. VC_BVG = VC [derived from BVG]			
VC.W.1	Width of VC (Except SEALRING_ALL, or following conditions: 1. {RH_TN SIZING 0.014 μm})	W1	=	0.0160, 0.0200, 0.0280
VC.W.1.1	Width of VC [INTERACT MP [width/length = 0.020/0.020 μm]]	W1A	=	0.0160
VC.W.1.2	Width of VC [INTERACT MP [width/length = 0.020/0.040 μm]] (Except BLK_WF)	W1B	=	0.0200
VC.W.1.3	Width of VC [INTERACT MD [width = 0.024 μm]] (Except BLK_WF)	W1C	=	0.0160, 0.0200
VC.W.1.4	Width of VC [INTERACT MD [width = 0.030 μm]] (Except PO_P76)	W1D	=	0.0200
VC.W.1.5	Width of VC [INTERACT MD [width = 0.030 μm]] [INSIDE PO_P76]	W1E	=	0.0200, 0.0280
VC.W.3	Width of VC [INTERACT RH_TN]	W3	=	0.0800
VC.S.1	Space of VC (Except following conditions: 1. VC space inside BVG)	S1	≥	0.0260
VC.S.5.4	Space of VC [INTERACT RH_TN] to {{ALL_MD OR ALL_OD} OR ALL_PO} (Overlap is not allowed)	S5D	≥	0.0560
VC.S.7	Space of VC to MP or {MD NOT CMD} [maximum delta V > 0.96V]	S7	≥	0.0300
VC.S.7.1	Space of VC to MP or {MD NOT CMD} [maximum delta V > 1.32V] (1.2V + 10%)	S7	≥	0.0350
VC.S.7.2	Space of VC to MP or {MD NOT CMD} [maximum delta V > 1.65V] (1.5V + 10%)	S7	≥	0.0370
VC.S.7.3	Space of VC to MP or {MD NOT CMD} [maximum delta V > 1.98V] (1.8V + 10%)	S7	≥	0.0420
VC.S.7.4	Space of VC to MP or {MD NOT CMD} [maximum delta V > 2.75V] (2.5V + 10%)	S7	≥	0.0500
VC.S.8	Space of VC [maximum delta V > 0.96V]	S8	≥	0.0450
VC.S.8.1	Space of VC [maximum delta V > 1.32V] (1.2V + 10%)	S8	≥	0.0470
VC.S.8.2	Space of VC [maximum delta V > 1.65V] (1.5V + 10%)	S8	≥	0.0650
VC.S.8.3	Space of VC [maximum delta V > 1.98V] (1.8V + 10%)	S8	≥	0.0650
VC.S.8.4	Space of VC [maximum delta V > 2.75V] (2.5V + 10%)	S8	≥	0.0970
VC.S.9	Space of VC to SRAMDMY (186;0) ({VC CUT SRAMDMY (186;0)} is not allowed)	S9	≥	0.1040
VC.S.10	Space of VC to ALL_OD [maximum delta V > 0.96V]	S10	≥	0.0310
VC.S.10.1	Space of VC to ALL_OD [maximum delta V > 1.32V] (1.2V + 10%)	S10	≥	0.0470
VC.S.10.2	Space of VC to ALL_OD [maximum delta V > 1.65V] (1.5V + 10%)	S10	≥	0.0490
VC.S.10.3	Space of VC to ALL_OD [maximum delta V > 1.98V] (1.8V + 10%)	S10	≥	0.0520
VC.S.10.4	Space of VC to ALL_OD [maximum delta V > 2.75V] (2.5V + 10%)	S10	≥	0.0620
VC.S.31.1.T	Space of VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 μm] (Except BLK_WF)	S31AT	≥	0.0370
VC.S.31.2.T	Space of VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 μm]	S31BT	≥	0.0370
VC.S.31.3.T	Space of VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 μm in horizontal/vertical direction]	S31CT	≥	0.0260

Rule No.	Description	Label	Op.	Rule
VC.S.31.4.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 µm] (Except BLK_WF)	S31DT	≥	0.0370
VC.S.31.5.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 µm]	S31ET	≥	0.0370
VC.S.31.6.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S31FT	≥	0.0260
VC.S.31.9.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC [edge length = 0.040/0.020 µm in horizontal/vertical direction]	S31IT	≥	0.0450
VC.S.31.12.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction]	S31LT	≥	0.0370
VC.S.31.15.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction]	S31OT	≥	0.0370
VC.S.31.16.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 µm] (Except BLK_WF)	S31PT	≥	0.0370
VC.S.31.17.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 µm]	S31QT	≥	0.0370
VC.S.31.18.T	Space of VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction]	S31RT	≥	0.0260
VC.S.32.1.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 µm] (Except BLK_WF)	S32AT	≥	0.0370
VC.S.32.2.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 µm]	S32BT	≥	0.0370
VC.S.32.3.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction]	S32CT	≥	0.0260
VC.S.32.4.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 µm] (Except BLK_WF)	S32DT	≥	0.0370
VC.S.32.5.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 µm] (Except BVG)	S32E	≥	0.0370
VC.S.32.6.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except BVG)	S32F	≥	0.0260
VC.S.32.9.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.040/0.020 µm in horizontal/vertical direction]	S32IT	≥	0.0450
VC.S.32.12.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction]	S32LT	≥	0.0370
VC.S.32.15.T	Space of VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction]	S32OT	≥	0.0370
VC.S.32.16.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 µm] (Except BLK_WF)	S32PT	≥	0.0370
VC.S.32.17.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 µm]	S32QT	≥	0.0370
VC.S.32.18.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction]	S32RT	≥	0.0260
VC.S.33.3.T	Space of VC [edge length = 0.040/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction]	S33CT	≥	0.0450

Rule No.	Description	Label	Op.	Rule
VC.S.33.6.T	Space of VC [edge length = 0.040/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S33FT	≥	0.0450
VC.S.33.7.T	Space of VC [edge length = 0.040/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction]	S33GT	≥	0.0450
VC.S.33.9.T	Space of VC [edge length = 0.040/0.020 µm in horizontal/vertical direction] to VC [edge length = 0.040/0.020 µm in horizontal/vertical direction]	S33IT	≥	0.0450
VC.S.33.12.T	Space of VC [edge length = 0.040/0.020 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction]	S33LT	≥	0.0450
VC.S.33.15.T	Space of VC [edge length = 0.040/0.020 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction]	S33OT	≥	0.0450
VC.S.34.3.T	Space of VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction]	S34CT	≥	0.0370
VC.S.34.6.T	Space of VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S34FT	≥	0.0370
VC.S.34.7.T	Space of VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction]	S34GT	≥	0.0370
VC.S.34.9.T	Space of VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction] to VC [edge length = 0.040/0.020 µm in horizontal/vertical direction]	S34IT	≥	0.0450
VC.S.34.12.T	Space of VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction]	S34LT	≥	0.0370
VC.S.34.15.T	Space of VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction]	S34OT	≥	0.0370
VC.S.35.3.T	Space of VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction]	S35CT	≥	0.0370
VC.S.35.6.T	Space of VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction]	S35FT	≥	0.0370
VC.S.35.7.T	Space of VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction]	S35GT	≥	0.0370
VC.S.35.9.T	Space of VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction] to VC [edge length = 0.040/0.020 µm in horizontal/vertical direction]	S35IT	≥	0.0450
VC.S.35.12.T	Space of VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction]	S35LT	≥	0.0370
VC.S.35.15.T	Space of VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction]	S35OT	≥	0.0370
VC.S.38.15.T	Space of VC [edge length = 0.388~1.828/0.080 µm in horizontal/vertical direction] to VC [edge length = 0.388~1.828/0.080 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.132 µm]	S38OT	≥	0.1320
VC.S.38.16.T	Space of VC [edge length = 0.388~1.828/0.080 µm in horizontal/vertical direction] to VC [edge length = 0.388~1.828/0.080 µm in horizontal/vertical direction] in vertical direction [PRL > -0.132 µm]	S38PT	≥	0.1500
VC.S.39.1.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 µm] (Except BLK_WF)	S39AT	≥	0.0370
VC.S.39.2.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 µm]	S39BT	≥	0.0370
VC.S.39.3.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 µm in horizontal/vertical direction]	S39CT	≥	0.0260

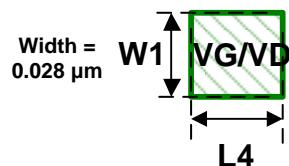
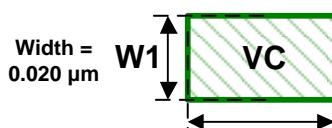
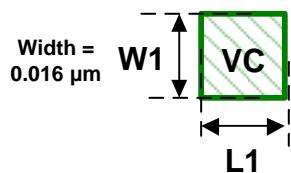
Rule No.	Description	Label	Op.	Rule
VC.S.39.4.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 µm] (Except BLK_WF)	S39DT	≥	0.0370
VC.S.39.5.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 µm] (Except BVG)	S39E	≥	0.0370
VC.S.39.6.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except BVG)	S39F	≥	0.0260
VC.S.39.9.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.040/0.020 µm in horizontal/vertical direction]	S39IT	≥	0.0450
VC.S.39.12.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.054 µm in horizontal/vertical direction]	S39LT	≥	0.0370
VC.S.39.15.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC_BVG [edge length = 0.020/0.074 µm in horizontal/vertical direction]	S39OT	≥	0.0370
VC.S.39.16.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.0200 µm] (Except BLK_WF)	S39PT	≥	0.0370
VC.S.39.17.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] in vertical direction [PRL > -0.0105 µm] (Except BVG)	S39QT	≥	0.0370
VC.S.39.18.T	Space of VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] to VC [edge length = 0.028/0.028 µm in horizontal/vertical direction] (Except BVG)	S39RT	≥	0.0260
VC.EN.0	1. Square VC enclosure by MD [width = 0.024 µm] is defined by VC.EN.1, VC.EN.1.1, VC.EN.2, H240.VC.EN.1, H240.VC.EN.1.1, H240.VC.EN.1.3, H300.VC.EN.1, H300.VC.EN.1.1, H300.VC.EN.1.3 2. Square VC enclosure by square MP is defined by VC.EN.3 3. Rectangular VC enclosure by MD [width = 0.030 µm] is defined by VC.R.1.2, VC.EX.2 4. Rectangular VC enclosure by rectangular MP [width/length = 0.020/0.040 µm] is defined by VC.EN.4 5. For enclosure of VC by {ALL_MD NOT ALL_CMD}, refer to the "Cut-MD (CMD) Layout Rules" section 6. Square VC [width = 0.028 µm] enclosure by MD [width = 0.030 µm] is defined by VC.EN.2.1			
VC.EN.1	Square VC [width = 0.016 µm, INTERACT MD [width = 0.024 µm]] enclosure by MD [width = 0.024 µm] for two opposite sides with the other two sides = 0.004 µm (Except FB_9, FB_8, BLK_WF)	EN1	≥	0.0200
VC.EN.1.1	Square VC [width = 0.020 µm, INTERACT MD [width = 0.024 µm]] enclosure by MD [width = 0.024 µm] for two opposite sides with the other two sides = 0.002 µm (Except FB_9, FB_8, BLK_WF)	EN1A	≥	0.0200
VC.EN.2	Square VC [width = 0.020 µm, INTERACT MD [width = 0.024 µm]] enclosure by MD [width = 0.030 µm] for two opposite sides with the other two sides = 0.005 µm (Except BLK_WF)	EN2	≥	0.0200
VC.EN.2.1	Square VC [width = 0.028 µm, INTERACT MD] enclosure by MD [width = 0.030 µm] for two opposite sides with the other two sides = 0.001 µm (Except BLK_WF)	EN2A	≥	0.0200
VC.EN.3	Square VC enclosure by square MP for all sides	EN3	≥	0.0020
VC.EN.4	Rectangular VC [width/length = 0.020/0.040 µm] enclosure by rectangular MP [width/length = 0.020/0.040 µm] for all sides	EN4	=	0
VC.EX.2	Short side of MD [width = 0.030 µm] extension on VC for two opposite sides in vertical direction (Extension ≤ 0 µm is not allowed)	EX2	≥	0.0150

Rule No.	Description	Label	Op.	Rule
VC.DN.1	Maximum VC density across full chip		\leq	7%
VC.DN.2	Maximum VC density in window $20 \mu\text{m} \times 20 \mu\text{m}$, stepping $10 \mu\text{m}$ (Except TCDDMY, ICOVL_SINGLE)		\leq	10%
VC.L.1	Length of VC [width = $0.016 \mu\text{m}$]	L1	=	0.0160
VC.L.2	Length of VC [width = $0.020 \mu\text{m}$]	L2	=	0.0200, 0.0400
VC.L.3	Length of VC [width = $0.080 \mu\text{m}$] (Except SEALRING_ALL)	L3	=	0.3880 ~ 1.828
VC.L.4	Length of VC [width = $0.028 \mu\text{m}$]	L4	=	0.0280
VC.R.1	VC must be a rectangle orthogonal to grid (Except SEALRING_ALL)			
VC.R.1.2	Rectangular VC [width/length = $0.020/0.040 \mu\text{m}$, INTERACT MD [width = $0.030 \mu\text{m}$]] must be centered at centerline of MD [width = $0.030 \mu\text{m}$] in horizontal direction			
VC.R.9.1	Square VC should be fully covered by {Square MP AND M0_NOT_CM0} or {{MD NOT ALL_CMD} AND M0_NOT_CM0} (Except BLK_WF)			
VC.R.9.2	Square VC [INSIDE {CCP_9 OR CCP_8}] should be fully covered by {{MD NOT CMD} AND M0}			
VC.R.9.3	Rectangular VC [width/length = $0.020/0.040 \mu\text{m}$] must interact MD [width = $0.030 \mu\text{m}$] or fully covered by rectangular MP [width/length = $0.020/0.040 \mu\text{m}$] (Except BLK_WF)			
VC.R.9.3.1	Rectangular VC [width/length = $0.020/0.040 \mu\text{m}$, INTERACT MD [width = $0.030 \mu\text{m}$]] interact PO_P76 is not allowed.			
VC.R.9.5	VC should be fully covered by M0_NOT_CM0			
VC.R.9.6	VC [width/length = $0.020/0.020 \mu\text{m}$] must be inside {MD NOT CMD} (Except BLK_WF)			
VC.R.9.7	VC [width/length = $0.028/0.028 \mu\text{m}$] must interact MD [width = $0.030 \mu\text{m}$, INSIDE PO_P76]			
VC.R.11	VC overlap {{SR_DOD OR SR_DPO} OR SR_DMD} is not allowed (Except SEALRING_ALL)			
VC.R.14	Maximum delta V > $3.63V$ is not allowed. DRC searching range of VC space to VC is < $0.405 \mu\text{m}$			
VC.R.14.3	{VC [NOT INTERACT {MD OR RH_TN}] INTERACT OD} is not allowed			
VC.R.18	VC [width = $0.016/0.020/0.028 \mu\text{m}$] interact {SEALRING_ALL OR RH_TNB} is not allowed			
VC.R.19.9	Space of VC $\leq 0.021 \mu\text{m}$ inside {RH_TNB [area $\geq 900 \mu\text{m}^2$] SIZING 2 μm } is not allowed			
VC.R.21	VC [INTERACT MD] interact BCMD [both 2 vertical edge abut CMD] is not allowed			
VC.R.22	VC [width/length = $0.020/0.040 \mu\text{m}$] must be horizontal direction (Except BLK_WF)			
VC.R.22.1	VC [width = $0.080 \mu\text{m}$] must be horizontal direction (Except SEALRING_ALL)			

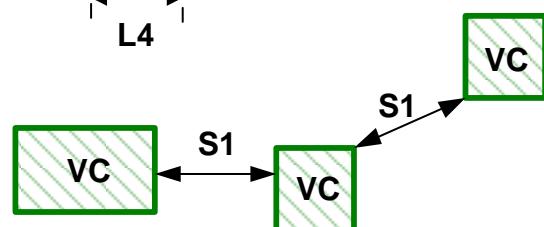
Table Notes:

- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

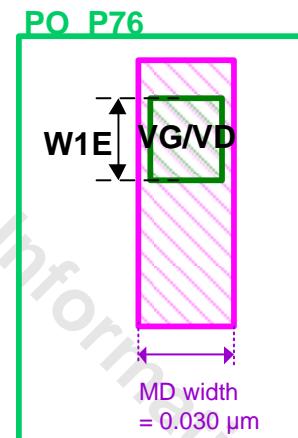
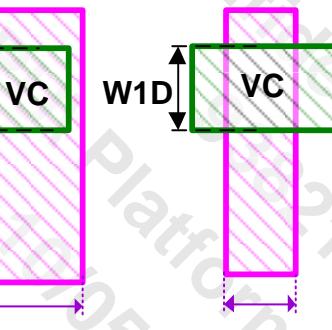
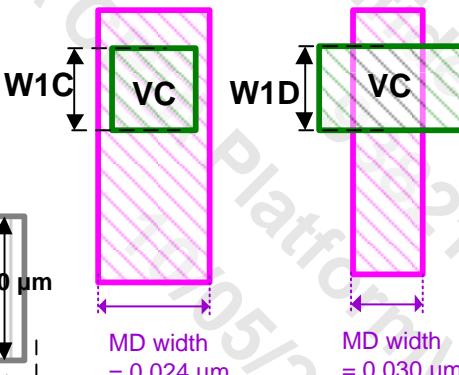
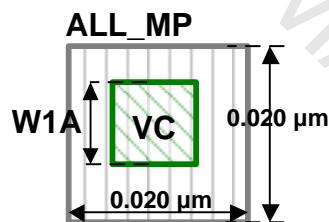
VC



VC.W.1 / VC.L.1 / VC.L.2 / VC.L.4

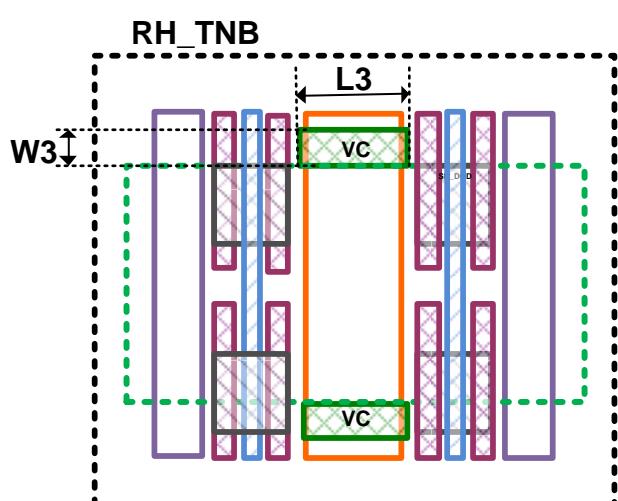


VC.S.1

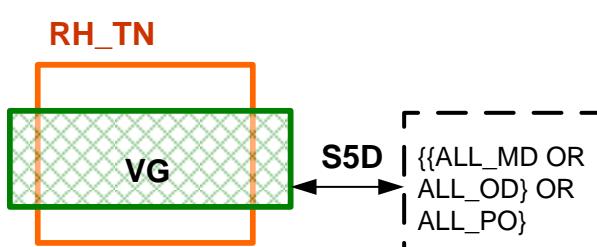


VC.W.1.1 / VC.W.1.2 / VC.W.1.3 / VC.W.1.4

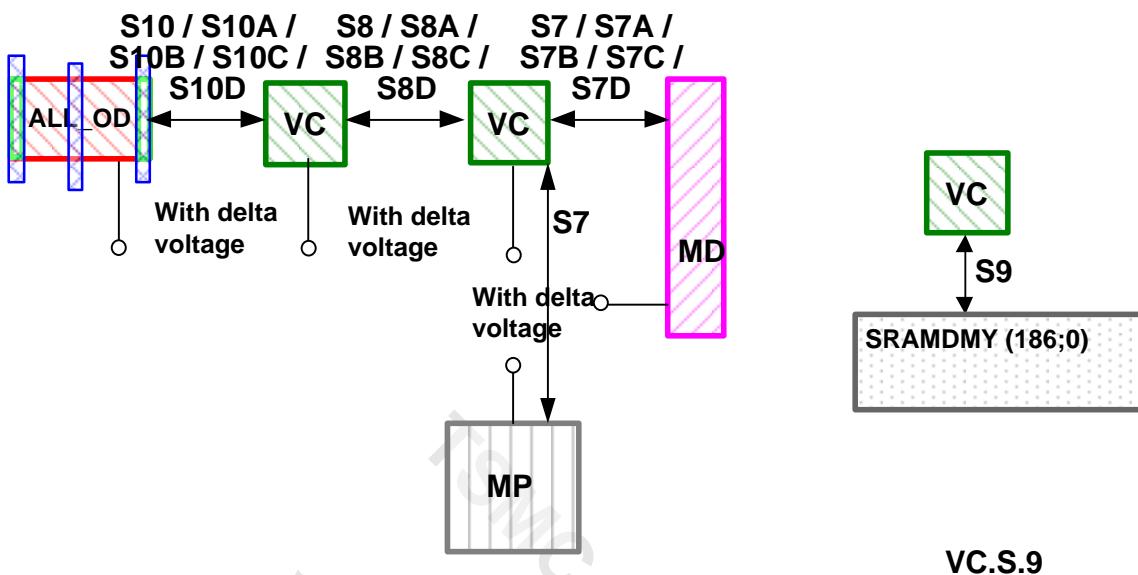
VC.W.1.5



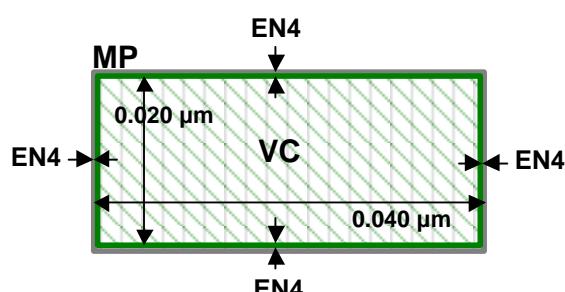
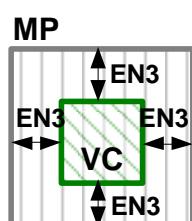
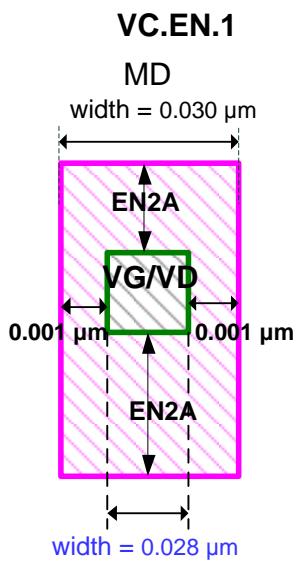
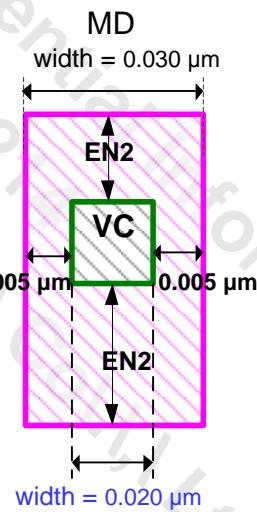
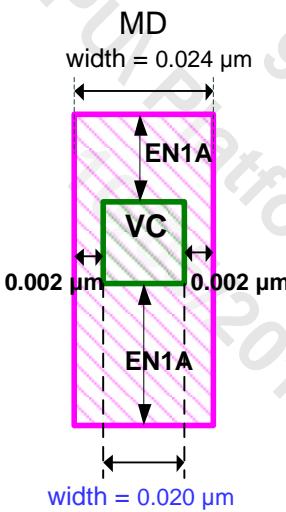
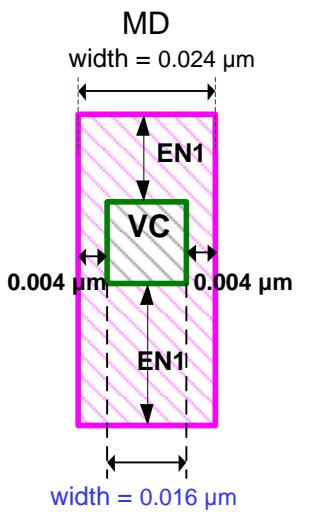
VC.W.3 / VC.L.3

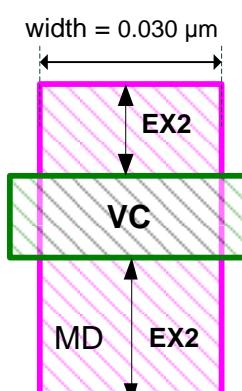


VC.S.5.4



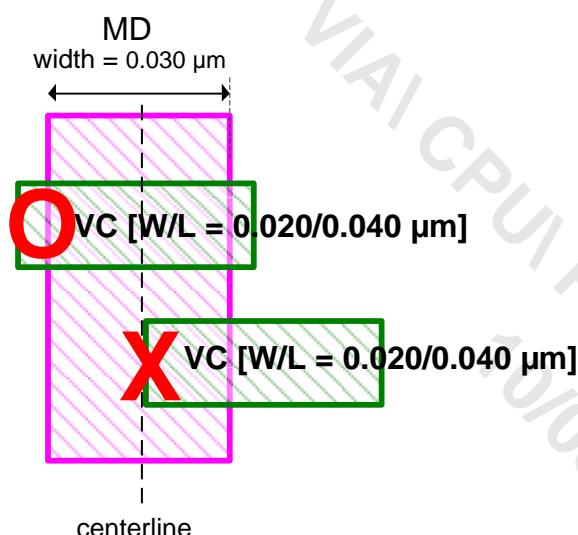
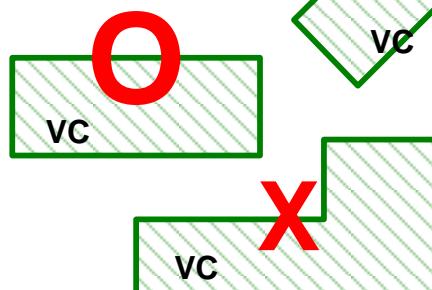
VC.S.7 / VC.S.7.1 / VC.S.7.2 / VC.S.7.3 / VC.S.7.4
VC.S.8 / VC.S.8.1 / VC.S.8.2 / VC.S.8.3 / VC.S.8.4
VC.S.10 / VC.S.10.1 / VC.S.10.2 / VC.S.10.3 / VC.S.10.4



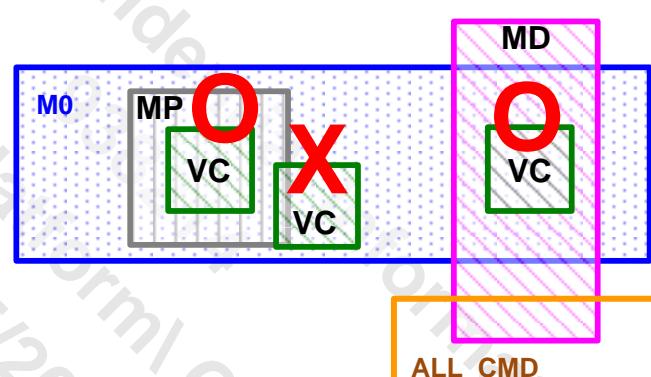


VC.EX.2

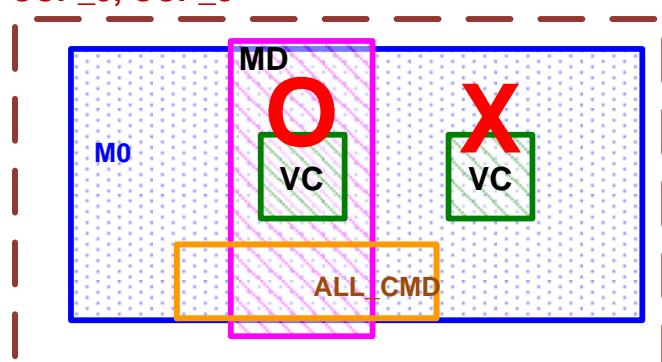
must be a rectangle
orthogonal to grid



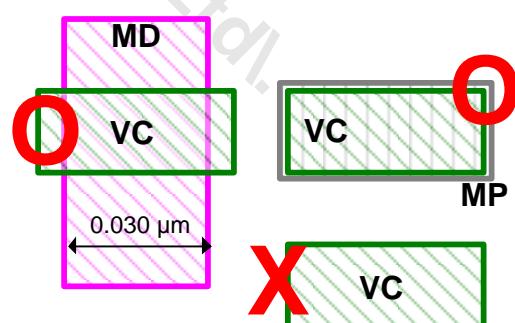
VC.R.1.2



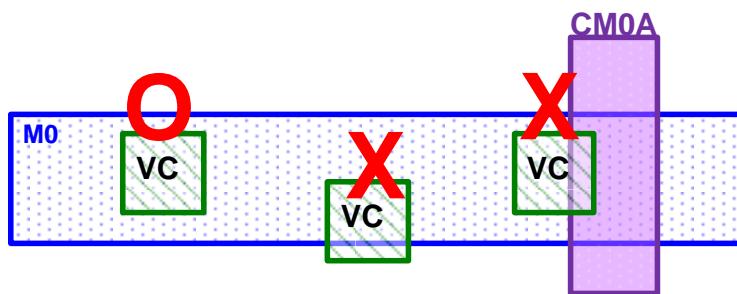
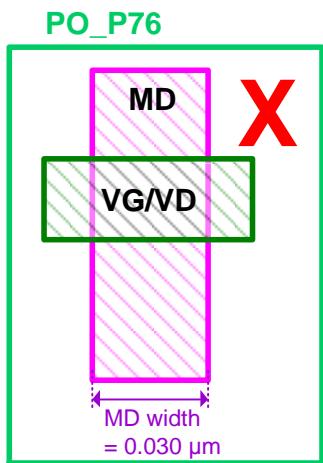
VC.R.9.1

CCP_9, CCP_8

VC.R.9.2

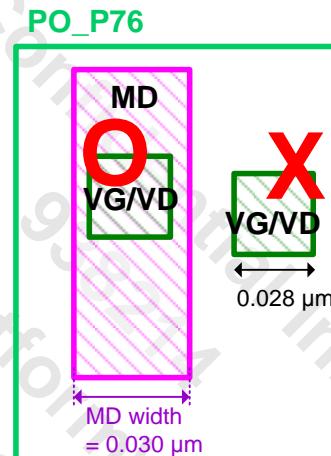
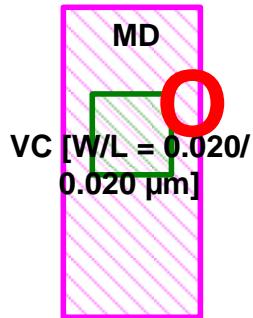


VC.R.9.3



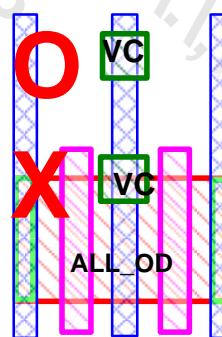
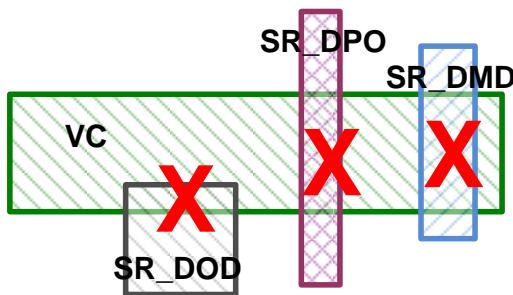
VC.R.9.3.1

VC.R.9.5



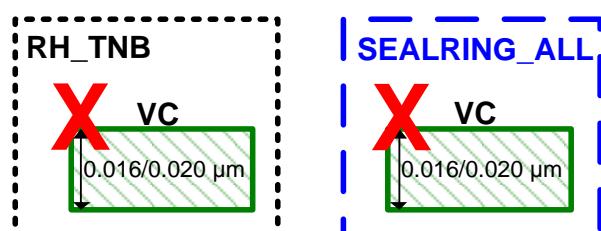
VC.R.9.6

VC.R.9.7

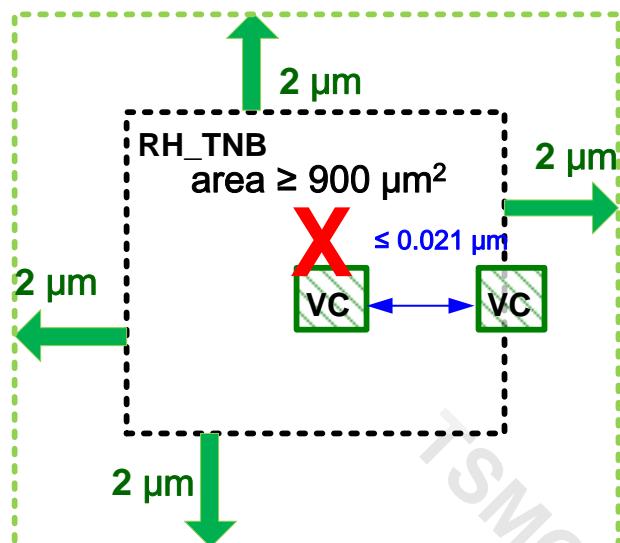


VC.R.11

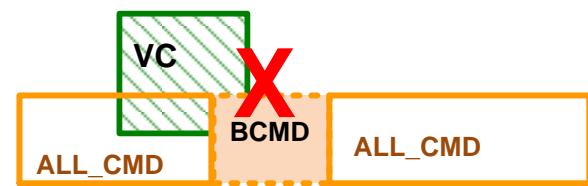
VC.R.14.3



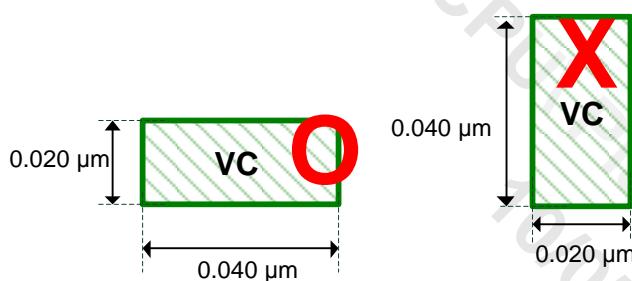
VC.R.18



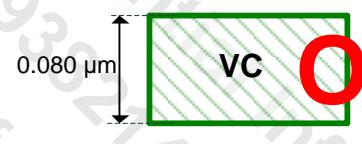
VC.R.19.9



VC.R.21



VC.R.22



VC.R.22.1



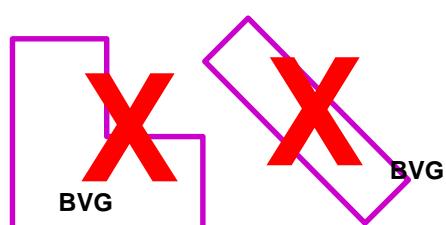
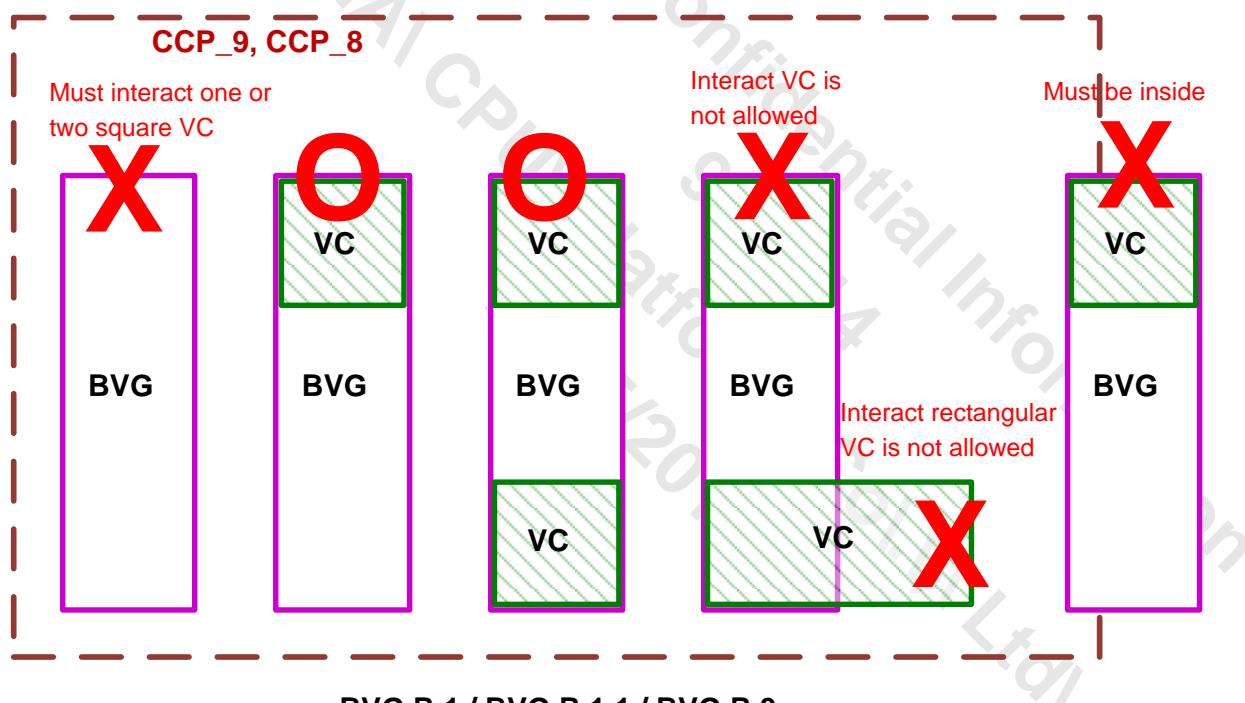
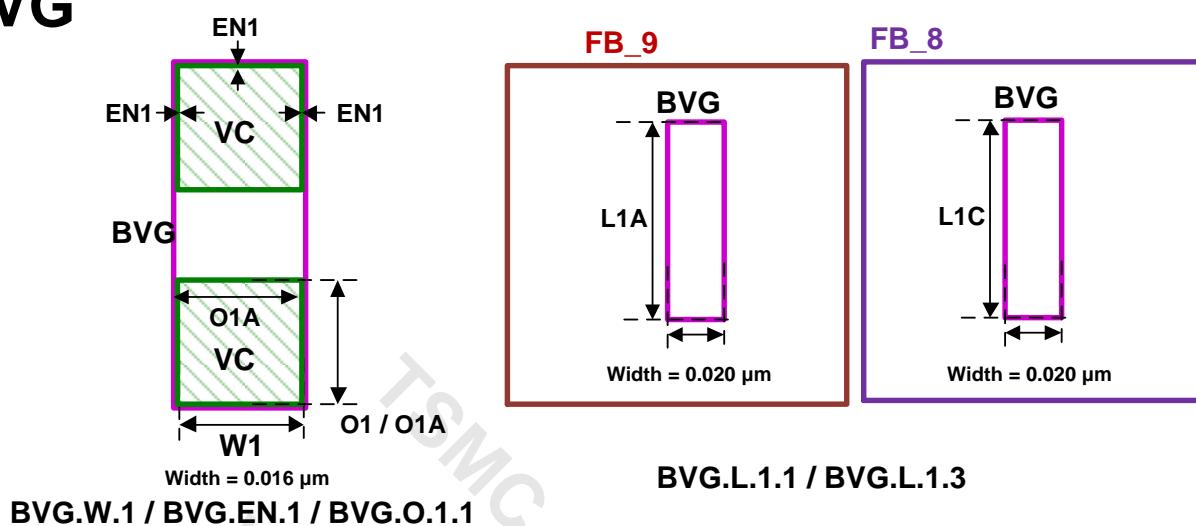
4.5.38 Butted VG (BVG) Layout Rules

BVG (CAD layer: 179;274) is a tape-out layer, and it can be used as an interconnection layer between VC at STDCELL cell boundary.

Two square VC interact BVG after cell placement will be merged to one rectangular VC during mask making process in TSMC.

VC (CAD layer: 179;400) is used as Via Contact hole between MD and M0, MP and M0, or RH_TN and M0.

Rule No.	Description	Label	Op.	Rule
BVG.W.1	Width	W1	=	0.0200
BVG.EN.1	Square VC enclosure by BVG for three sides	EN1	=	0
BVG.L.1.1	Length of BVG [width = 0.020 μm, INSIDE FB_9]	L1A	=	0.0540
BVG.L.1.3	Length of BVG [width = 0.020 μm, INSIDE FB_8]	L1C	=	0.0740
BVG.O.1.1	Overlap of square VC [width = 0.020 μm] in vertical/horizontal direction	O1A	=	0.0200
BVG.R.1	BVG must interact one or two square VC			
BVG.R.1.1	BVG interact rectangular VC is not allowed			
BVG.R.3	BVG must be inside {CCP_9 OR CCP_8}			
BVG.R.4	BVG must be a rectangle orthogonal to grid			
BVG.R.5	BVG must be vertical direction			

BVG

Must be a rectangle
orthogonal to grid

BVG.R.4 / BVG.R.5

4.5.39 M0 Layout Rules

- Minimum Pitch (MINP) 0.040 μm can only be drawn in parallel to PO direction.
- Data type 255, 256 is used for metal pitch 0.040 μm in parallel to core PO direction

- NonMinimum Pitch (NMNP) direction is perpendicular to Minimum pitch (MINP) direction.

For the specification of metals/VIAS stacking sequence and associated mask ID, please refer to section 2.5.

M0 = {M0CA (180;255) OR M0CB (180;256)}

M0_NOT_CM0 = {{M0CA NOT CM0A} OR {M0CB NOT CM0B}}

M0 line-end (end) definition: M0 width ≤ 0.060 μm.

DRC checks DM0_O as well as M0 in this section.

Rule No.	Description	Label	Op.	Rule
M0.W.1	Width	W1	≥	0.0200
M0.W.1.1	Width [MINP direction] (Except BLK_WB)	W1A	=	0.0200, 0.0220, 0.0240, 0.0260, 0.0280, 0.0400, 0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1800
M0.W.1.1.2	Width of DM0_O [MINP direction]	W1A2	=	0.0240, 0.0400, 0.1400
M0.W.1.1.3	Width of M0 [MINP direction, INTERACT VC [width = 0.028 μm]]	W1A3	≥	0.0400
M0.W.1.2	Width [NMNP direction]	W1B	=	0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1800
M0.W.2	Width of 45-degree bent M0 (Except SEALRING_ALL)	W2	≥	0.4000
M0.W.3	Maximum width (Except SEALRING_ALL, LOGO)	W3	≤	0.5000
M0.S.1	Space	S1	≥	0.0200
M0.S.2	Space to M0 [0.020 μm ≤ width ≤ 0.028 μm] in MINP direction [PRL > -0.080 μm] (Except BLK_WB)	SM	=	0.0200 ~ 0.0250, ≥ 0.0350
M0.S.2.1	Space to M0 [width = 0.040 μm] in MINP direction [PRL > -0.040 μm] (Except BLK_WB)	SM	≥	0.0350
M0.S.2.3	Space of M0 [width = 0.060 μm] to M0 [width = 0.020 μm] in MINP direction [PRL > -0.040 μm] (Except following conditions: 1. {{FB_9 OR BV_FBF [width = 0.120/0.240 μm]} SIZING 0.040 μm in horizontal direction})	SM	≥	0.0400
M0.S.2.3.1	Space of M0 [width = 0.080 μm] to M0 [width = 0.020 μm] in MINP direction [PRL > -0.040 μm] (Except following conditions: 1. {{FB_8 OR BV_FBF [width = 0.150/0.300 μm]} SIZING 0.040 μm in horizontal direction})	SM	≥	0.0400
M0.S.2.4	Space of M0 [width = 0.060/0.080 μm] to M0 [width > 0.020 μm] in MINP direction [PRL > -0.040 μm] (Except BLK_WB)	SM	≥	0.0400
M0.S.2.5	Space to M0 [width ≥ 0.100 μm] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0600
M0.S.2.6	Space to M0 [width ≥ 0.260 μm] in MINP direction [PRL > 0.080 μm]	SM	≥	0.1600
M0.S.3.1	Space to M0 [width = 0.060 μm] in NMNP direction [PRL > -0.060 μm]	SN	≥	0.0660
M0.S.3.2	Space to M0 [width = 0.080 μm] in NMNP direction [PRL > -0.060 μm]	SN	≥	0.0760
M0.S.3.3	Space to M0 [width = 0.100 μm] in NMNP direction [PRL > -0.060 μm]	SN	≥	0.0760
M0.S.3.4	Space to M0 [width = 0.120 μm] in NMNP direction [PRL > -0.060 μm]	SN	≥	0.0760
M0.S.3.5	Space of M0 [width = 0.140 μm with edge length > 0.060 μm in MINP direction] to M0 [with edge length > 0.060 μm in MINP direction] in NMNP direction [0 μm < PRL ≤ 0.080 μm]	SN	≥	0.1200
M0.S.3.6	Space to M0 [width = 0.140 μm] in NMNP direction [PRL > 0.080 μm]	SN	≥	0.1600

Rule No.	Description	Label	Op.	Rule
M0.S.3.7	Space of M0 [width \geq 0.180 μm with edge length $> 0.060 \mu\text{m}$ in MINP direction] to M0 [with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [0 $\mu\text{m} < \text{PRL} \leq 0.080 \mu\text{m}$]	SN	\geq	0.1400
M0.S.3.8	Space to M0 [width \geq 0.180 μm] in NMINP direction [$\text{PRL} > 0.080 \mu\text{m}$]	SN	\geq	0.1800
M0.S.3.9	Space of M0 [width \geq 0.260 μm with edge length $> 0.060 \mu\text{m}$ in MINP direction] to M0 [with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [0 $\mu\text{m} < \text{PRL} \leq 0.080 \mu\text{m}$]	SN	\geq	0.1800
M0.S.3.10	Space to M0 [width \geq 0.260 μm] in NMINP direction [$\text{PRL} > 0.080 \mu\text{m}$]	SN	\geq	0.2600
M0.S.4.1	Space to M0 line-end in NMINP direction [$\text{PRL} > -0.020 \mu\text{m}$]	S4A	\geq	0.1080
M0.S.4.2	Space to M0 line-end in MINP direction [$\text{PRL} > -0.020 \mu\text{m}$]	S4B	\geq	0.1080
M0.S.5	Corner projected space of M0 [-0.060 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$] (Except following conditions: 1. Corner with edge length $\leq 0.028 \mu\text{m}$ on both sides)	S5	\geq	0.0600
M0.S.12	Space to 45-degree bent M0 [$\text{PRL} > 0 \mu\text{m}$] (Except SEALRING_ALL)	S12	\geq	0.4000
M0.S.12.1	Space to 45-degree bent M0 (Except SEALRING_ALL)	S12A	\geq	0.1400
M0.S.13.1	Space to VC or VIA0 [maximum delta V $> 0.96\text{V}$]	S13	\geq	0.0550
M0.S.13.2	Space to VC or VIA0 [maximum delta V $> 1.32\text{V}$] (1.2V + 10%)	S13	\geq	0.0640
M0.S.13.3	Space to VC or VIA0 [maximum delta V $> 1.65\text{V}$] (1.5V + 10%)	S13	\geq	0.0700
M0.S.13.4	Space to VC or VIA0 [maximum delta V $> 1.98\text{V}$] (1.8V + 10%)	S13	\geq	0.0820
M0.S.13.5	Space to VC or VIA0 [maximum delta V $> 2.75\text{V}$] (2.5V + 10%)	S13	\geq	0.0870
M0.S.16	Space to {SRM (50;0) OR SRAMDMY (186;0)}	S16	\geq	0.1080
M0.S.18	Space to M0_NOT_CM0 [maximum delta V $> 0.96\text{V}$]	S18	\geq	0.0520
M0.S.18.1	Space to M0_NOT_CM0 [maximum delta V $> 1.32\text{V}$] (1.2V + 10%)	S18	\geq	0.0550
M0.S.18.2	Space to M0_NOT_CM0 [maximum delta V $> 1.65\text{V}$] (1.5V + 10%)	S18	\geq	0.0610
M0.S.18.3	Space to M0_NOT_CM0 [maximum delta V $> 1.98\text{V}$] (1.8V + 10%)	S18	\geq	0.0690
M0.S.18.4	Space to M0_NOT_CM0 [maximum delta V $> 2.75\text{V}$] (2.5V + 10%)	S18	\geq	0.0790
M0.S.18.6	Corner projected space of M0_NOT_CM0 [maximum delta V $> 0.96\text{V}$, -0.060 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$]	S18F	\geq	0.1000
M0.S.18.7	Corner projected space of M0_NOT_CM0 [maximum delta V $> 1.98\text{V}$, -0.100 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$]	S18G	\geq	0.1000
M0.EN.0	1. Enclosure of square VC is defined by either M0.EN.1 or M0.EN.1.1 or M0.EN.1.2 or M0.EN.1.3 or M0.EN.1.4 or M0.EN.1.5, M0.EN.1.7, M0.EN.1.8, M0.EN.2, M0.EN.2.1, M0.EN.2.2, M0.EN.2.3, M0.EN.2.4, M0.EN.2.5, M0.EN.2.7, M0.EN.2.8, M0.EN.3.1, M0.EN.3.2, or M0.EN.5.1, M0.EN.5.2, M0.EN.5.3, or H240.M0.EN.2.7, H300.M0.EN.2.8 2. Enclosure of rectangular VC is defined by either M0.EN.4, M0.EN.4.1, M0.EN.4.2, M0.EN.4.3, M0.EN.4.4, M0.EN.4.5, M0.EN.4.7, M0.EN.4.7.1, M0.EN.4.8 3. For enclosure of VC by M0_NOT_CM0, refer to the "Cut-M0 (CM0) Layout Rules" section			
M0.EN.1	Enclosure of square VC [width = 0.016 μm] by M0 [width = 0.020 μm] for two opposite sides with the other two sides = 0.002 μm (Except BLK_WB)	EN1	\geq	0.0200
M0.EN.1.1	Enclosure of square VC [width = 0.016 μm] by M0 [width = 0.022 μm] for two opposite sides with the other two sides = 0.003 μm (Except BLK_WB)	EN1	\geq	0.0200
M0.EN.1.2	Enclosure of square VC [width = 0.016 μm] by M0 [width = 0.024 μm] for two opposite sides with the other two sides = 0.004 μm	EN1	\geq	0.0200
M0.EN.1.3	Enclosure of square VC [width = 0.016 μm] by M0 [width = 0.026 μm] for two opposite sides with the other two sides = 0.005 μm	EN1	\geq	0.0200
M0.EN.1.4	Enclosure of square VC [width = 0.016 μm] by M0 [width = 0.028 μm] for two opposite sides with the other two sides $\geq 0.005 \mu\text{m}$	EN1	\geq	0.0200
M0.EN.1.5	Enclosure of square VC [width = 0.016 μm] by M0 [width = 0.040 μm] for two opposite sides with the other two sides = 0.012 μm	EN1	\geq	0.0300
M0.EN.1.7	Enclosure of square VC [width = 0.016 μm] by M0 [width = 0.060 μm] for two opposite sides with the other two sides = 0.022 μm (Except BLK_WB)	EN1	\geq	0.0250

Rule No.	Description	Label	Op.	Rule
M0.EN.1.8	Enclosure of square VC [width = 0.016 μm] by M0 [width = 0.080 μm] for two opposite sides with the other two sides = 0.032 μm	EN1	≥	0.0200
M0.EN.2	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.020 μm] for two opposite sides with the other two sides = 0 μm	EN2	≥	0.0200
M0.EN.2.1	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.022 μm] for two opposite sides with the other two sides = 0.001 μm	EN2	≥	0.0200
M0.EN.2.2	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.024 μm] for two opposite sides with the other two sides = 0.002 μm (Except BLK_WB)	EN2	≥	0.0200
M0.EN.2.3	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.026 μm] for two opposite sides with the other two sides = 0.003 μm (Except BLK_WB)	EN2	≥	0.0200
M0.EN.2.4	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.028 μm] for two opposite sides with the other two sides = 0.004 μm (Except BLK_WB)	EN2	≥	0.0200
M0.EN.2.5	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.040 μm] for two opposite sides with the other two sides = 0.010 μm (Except BLK_WB)	EN2	≥	0.0300
M0.EN.2.7	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.060 μm] for two opposite sides with the other two sides = 0.020 μm (Except CCP_9, BLK_WB)	EN2	≥	0.0250
M0.EN.2.8	Enclosure of square VC [width = 0.020 μm] by M0 [width = 0.080 μm] for two opposite sides with the other two sides = 0.030 μm (Except CCP_8)	EN2	≥	0.0200
M0.EN.3.1	Enclosure of square VC by M0 [0.100 μm ≤ width < 0.260 μm] for two opposite sides with the other two sides ≥ 0.030 μm	EN3A	≥	0.0200
M0.EN.3.2	Enclosure of square VC by M0 [width ≥ 0.260 μm] for two opposite sides with the other two sides ≥ 0.025 μm	EN3B	≥	0.0600
M0.EN.4	Enclosure of short side of rectangular VC by M0 [width = 0.020 μm] with the other two sides = 0 μm	EN4	≥	0.0250
M0.EN.4.1	Enclosure of short side of rectangular VC by M0 [width = 0.022 μm] with the other two sides = 0.001 μm	EN4	≥	0.0250
M0.EN.4.2	Enclosure of short side of rectangular VC by M0 [width = 0.024 μm] with the other two sides = 0.002 μm	EN4	≥	0.0250
M0.EN.4.3	Enclosure of short side of rectangular VC by M0 [width = 0.026 μm] with the other two sides = 0.003 μm	EN4	≥	0.0250
M0.EN.4.4	Enclosure of short side of rectangular VC by M0 [width = 0.028 μm] with the other two sides = 0.004 μm	EN4	≥	0.0250
M0.EN.4.5	Enclosure of short side of rectangular VC by M0 [width = 0.040 μm] with the other two sides = 0.010 μm	EN4	≥	0.0200
M0.EN.4.7	Enclosure of short side of rectangular VC by M0 [width = 0.060 μm] with the other two sides = 0.020 μm	EN4	≥	0.0200
M0.EN.4.7.1	Enclosure of short side of rectangular VC by M0 [width = 0.060 μm] with the other two sides ≥ 0.030 μm	EN4	≥	0.0100
M0.EN.4.8	Enclosure of short side of rectangular VC by M0 [width ≥ 0.080 μm] with the other two sides ≥ 0.030 μm	EN4	≥	0.0200
M0.EN.5.1	Enclosure of square VC [width = 0.028 μm] by M0 [width = 0.040 μm] for two opposite sides with the other two sides = 0.006 μm	EN5	≥	0.0300
M0.EN.5.2	Enclosure of square VC [width = 0.028 μm] by M0 [width = 0.060 μm] for two opposite sides with the other two sides = 0.016 μm	EN5	≥	0.0250
M0.EN.5.3	Enclosure of square VC [width = 0.028 μm] by M0 [width = 0.080 μm] for two opposite sides with the other two sides = 0.026 μm	EN5	≥	0.0200
M0.L.1	At least one edge length of 45-degree bent M0 (minimum edge length)	L1	≥	0.9100
M0.L.2	Edge length with adjacent edge [length < 0.090 μm]	L2	≥	0.0800
M0.A.1	Area of M0	A1	≥	0.00368
M0.A.2	Area of M0_NOT_CM0 (Except FB_9, FB_8, BLK_WB)	A2	≥	0.00255
M0.DN.1.1	Minimum All_metal density in window 40 μm x 40 μm, stepping 20 μm (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	12.5%

Rule No.	Description	Label	Op.	Rule
M0.DN.1.2	Minimum All_metal density in window 40 μm x 40 μm, stepping 20 μm [3 μm x 3 μm empty area exists in the window] (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	25%
M0.DN.2	Maximum All_metal density in window 40 μm x 40 μm, stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. {{M0;252 OR M0;253} OR {M0;258 OR M0;259}})		≤	65%
M0.DN.2.3	Maximum All_metal density in window 40 μm x 40 μm, stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	75%
M0.DN.3	The All_metal density difference between any two neighboring checking windows including DMnEXCL [window 40 μm x 40 μm, stepping 40 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≤	50%
M0.DN.3.3	Maximum density difference between {{M0CA OR M0;252} OR M0;258} NOT {M0CA AND {CCP_9 OR CCP_8}} and {{M0CB OR M0;253} OR M0;259} across full chip (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	12.5 %
M0.DN.3.6	Maximum local density difference between {{M0CA OR M0;252} OR M0;258} and {{M0CB OR M0;253} OR M0;259} in window 40 μm x 40 μm, stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	40%
M0.DN.3.7	Minimum local density of {{M0CA OR M0;252} OR M0;258} in window 40 μm x 40 μm, stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		>	4.5%
M0.DN.3.8	Minimum local density of {{M0CB OR M0;253} OR M0;259} in window 40 μm x 40 μm, stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		>	4.5%
M0.DN.6.1	All_metal density [window 9 μm x 9 μm, stepping 4.5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
M0.DN.7	It is not allowed to have local density < 5% of all 3 consecutive metal (M0, M1, and M2) over any 27 μm x 27 μm (stepping 13.5 μm), i.e. it is allowed for either one of M0, M1, or M2 to have a local density ≥ 5% (The metal layers include M0/M1/M2 and dummy metals for ELK film) (Except ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc, 2. TCDDMY_Mn (assume 30% pattern density INSIDE TCDDMY_Mn))			
M0.DN.9	Minimum Line edge Density (LeD) in window 20 μm x 20 μm, stepping 10 μm Definition of "Line edge Density": (((All_metal area) - (All_metal SIZING -0.001 μm area)) x 1000) / Checking window (Except TCDDMY_M0, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags only if the checking window has any one metal {M0CA OR M0CB} width < 0.060 μm		≥	8.5

Rule No.	Description	Label	Op.	Rule
M0.DN.9.1	<p>Minimum Line edge Density (LeD) in window 20 μm x 20 μm, stepping 10 μm</p> <p>Definition of "Line edge Density": $((\text{All_metal area}) - (\text{All_metal SIZING } -0.001 \mu\text{m area})) \times 1000 / \text{Checking window}$</p> <p>(Except TCDDMY_M0, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window has any one metal {M0CA OR M0CB} width < 0.120 μm</p>		≥	3
M0.DN.10	<p>M0_DN density in window 20 μm x 20 μm, stepping 5 μm</p> <p>(Except TCDDMY_M0, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>Definition of M0_DN: $\{\text{DN_M0CA} * 0.7 + \text{DN_CM0A} * 1.4\}$ in the same window 20 μm x 20 μm of DN_M0CA and DN_CM0A</p> <p>Definition of DN_M0CA: Density of {{M0CA OR M0;252} OR M0;258} NOT {CCP_9 OR CCP_8} in window 20 μm x 20 μm</p> <p>Definition of DN_CM0A: Density of CM0A in window 20 μm x 20 μm</p>		=	5.5%~40%
M0.DN.10.1	Maximum local density of {{M0CA OR M0;252} OR M0;258} in window 20 μm x 20 μm, stepping 10 μm (Except SEALRING_ALL)		<	47%
M0.R.1	M0 must be a rectangle (Except SEALRING_ALL, LOGO)			
M0.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
M0.R.10	Overlap MetalFuse_B1 (156;8) is not allowed			
M0.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of {M0 NOT CM0} space to {M0 NOT CM0} or VC or VIA0 or {MD NOT CMD} or MP is < 0.360 μm			
M0.R.11.1	Overlap {PO NOT CPO}, {MD NOT CMD} or MP is not allowed [delta V > 2.75V] (Except DM0_O)			
M0.R.14	{{M0_Empty_Area SIZING 0.330 μm} INTERACT M0 island} is not allowed Definitions: 1. M0_Empty_Area: Area of {{CHIP NOT {{TCDDMY_Mn OR ICOVL_SINGLE} OR {{M0 OR {M0;252 OR M0;253}} OR {M0;258 OR M0;259}}}}} SIZING down/up 0.380 μm} ≥ 1.96 μm ² 2. M0 island: Area of (M0_NOT_CM0 with only one square VC [width x length = 0.016 μm x 0.016 μm, 0.020 μm x 0.020 μm]) ≤ 0.010 μm ²			
M0.R.17	DM0 is a must in chip level.			
M0.R.19	M0 line-end interact {{SRM (50;0) OR SRAMDMY (186;0)} SIZING 0.108 μm} NOT {SRM (50;0) OR SRAMDMY (186;0)}} is not allowed (Abut is allowed)			

Rule No.	Description	Label	Op.	Rule
M0.R.21	<p>Both side space of Small_M0CA_Group to M0CA [width \geq 0.060 μm] in MINP direction \leq 0.220 μm is not allowed</p> <p>Definition of Small_M0CA_Group: $\{\{\{\text{Small_M0CA SIZING up/down }0.033 \mu\text{m in MINP direction}\} \text{ SIZING down/up }0.0895 \mu\text{m in MINP direction}\} [\text{length} < 0.140 \mu\text{m in NMNP direction}]\} [\text{length} = 0.180\sim0.490 \mu\text{m in MINP direction}]$</p> <p>Definition of Small_M0CA: M0CA [width \leq 0.024 μm in MINP direction, length \leq 0.300 μm in NMNP direction]</p>			
M0.CS.0	DRC checks same color space of {M0CA OR DM0_DO1} and {M0CB OR DM0_DO2}, respectively in M0.CS.x rules			
M0.CS.0.1	Space to M0 [width \geq 0.020 μm] in MINP direction [same color, PRL > -0.100 μm]	SM	\geq	0.0600
M0.CS.0.2	Space to M0 [width \geq 0.060 μm] in NMNP direction [same color, PRL > -0.060 μm]	SN	\geq	0.1080
M0.CS.1.1	<p>Space to M0 [width = 0.020 μm] in MINP direction [same color, PRL > -0.124 μm] (Except BLK_WB, or following conditions:</p> <ol style="list-style-type: none"> {DM0_DO1 OR DM0_DO2} space to M0 [width = 0.020 μm] \geq 0.120 μm, PRL > -0.124 μm, $\{\{\text{FB_9 OR BV_FB [width = }0.120/0.240 \mu\text{m]}\} \text{ SIZING }0.124 \mu\text{m in horizontal direction}\},$ $\{\{\text{FB_8 OR BV_FB [width = }0.150/0.300 \mu\text{m]}\} \text{ SIZING }0.124 \mu\text{m in horizontal direction}\})$ 	SM	=	0.0600, 0.0620, 0.0640, 0.0660, \geq 0.1400
M0.CS.1.1.1	<p>Space to M0 [0.022 $\mu\text{m} \leq$ width \leq 0.024 μm] in MINP direction [same color, PRL > -0.124 μm] (Except BLK_WB, or following conditions:</p> <ol style="list-style-type: none"> {DM0_DO1 OR DM0_DO2} space to M0 [0.022 $\mu\text{m} \leq$ width \leq 0.024 $\mu\text{m}] \geq$ 0.120 μm, PRL > -0.124 μm, Space of DM0_DO1 [width = 0.024 μm], DM0_DO2 [width = 0.024 $\mu\text{m}] \geq$ 0.068 μm, PRL > -0.124 $\mu\text{m})$ 	SM	=	0.0600, 0.0620, 0.0640, 0.0660, \geq 0.1400
M0.CS.1.1.2	<p>Space to M0 [width = 0.026 μm] in MINP direction [same color, PRL > -0.124 μm] (Except BLK_WB, or following conditions:</p> <ol style="list-style-type: none"> {DM0_DO1 OR DM0_DO2} space to M0 [width = 0.026 $\mu\text{m}] \geq$ 0.120 μm, PRL > -0.124 $\mu\text{m})$ 	SM	=	0.0600, 0.0620, 0.0640, 0.0680, \geq 0.1400
M0.CS.1.1.3	<p>Space to M0 [width = 0.028 μm] in MINP direction [same color, PRL > -0.124 μm] (Except BLK_WB, or following conditions:</p> <ol style="list-style-type: none"> {DM0_DO1 OR DM0_DO2} space to M0 [width = 0.028 $\mu\text{m}] \geq$ 0.120 μm, PRL > -0.124 $\mu\text{m})$ 	SM	=	0.0660, \geq 0.1400
M0.CS.1.1.4	<p>Space to M0 [width = 0.040 μm] in MINP direction [same color, PRL > -0.060 μm] (Except BLK_WB)</p>	SM	\geq	0.1200
M0.CS.1.1.6	<p>Forbidden space of M0 [0.020 $\mu\text{m} \leq$ width \leq 0.024 μm] in MINP direction [same color, PRL > 0 μm] (Except BLK_WB, or following conditions:</p> <ol style="list-style-type: none"> M0_Projection_Region fully projected by another M0 [width > 0.024 μm] or {CCP_9 OR CCP_8}) <p>Definition of M0_Projection_Region: Enclosed region formed by M0 [0.020 $\mu\text{m} \leq$ width \leq 0.024 <math>\mu\text{m}]], PRL > 0 μm</math></p>	SM	=	0.1870 ~ 0.2190, 0.2570 ~ 0.2990, 0.3370 ~ 0.3790
M0.CS.1.1.7	Space of DM0_O [width = 0.024 μm] to M0 in MINP direction [same color, PRL > -0.124 μm]	SM	=	0.0600, 0.0620, 0.0640, 0.0660, 0.0680, 0.0700, \geq 0.1000

Rule No.	Description	Label	Op.	Rule
M0.CS.1.2.1	Space of M0 [width = 0.060 μm] to M0 [width = 0.020 μm] in MINP direction [same color, PRL > -0.060 μm] (Except BLK_WB, or following conditions: 1. {{FB_9 OR BV_FB [width = 0.120/0.240 μm]}} SIZING 0.060 μm in horizontal direction))	SM	\geq	0.1000
M0.CS.1.2.2	Space of M0 [width = 0.060 μm] to M0 [width \geq 0.022 μm] in MINP direction [same color, PRL > -0.060 μm] (Except BLK_WB)	SM	\geq	0.1000
M0.CS.1.3	Space of M0 [width = 0.080 μm with edge length > 0.060 μm in NMINP direction] to M0 [width = 0.020 μm] in MINP direction [same color, PRL > -0.060 μm] (Except following conditions: 1. {{FB_8 OR BV_FB [width = 0.150/0.300 μm]}} SIZING 0.060 μm in horizontal direction))	SM	\geq	0.1200
M0.CS.1.3.1	Space of M0 [width = 0.080 μm with edge length > 0.060 μm in NMINP direction] to M0 [width \geq 0.022 μm] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1200
M0.CS.1.4	Space of M0 [0.100 μm \leq width \leq 0.120 μm with edge length > 0.060 μm in NMINP direction] to M0 [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1200
M0.CS.1.6	Space of M0 [width = 0.140 μm with edge length > 0.060 μm in NMINP direction] to M0 [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1300
M0.CS.1.7	Space to M0 [width = 0.140 μm] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.1600
M0.CS.1.8	Space of M0 [width \geq 0.180 μm with edge length > 0.060 μm in NMINP direction] to M0 [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1400
M0.CS.1.9	Space to M0 [width \geq 0.180 μm] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.1800
M0.CS.1.10	Space of M0 [width \geq 0.260 μm with edge length > 0.060 μm in NMINP direction] to M0 [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, 0 μm < PRL \leq 0.080 μm]	SM	\geq	0.1800
M0.CS.1.11	Space to M0 [width \geq 0.260 μm] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.2600
M0.CS.3.2	Space to M0 [width = 0.060 μm] in NMINP direction [same color, PRL > -0.060 μm]	SN	\geq	0.1250
M0.CS.3.3	Space to M0 [width = 0.080 μm] in NMINP direction [same color, -0.060 μm < PRL \leq 0.060 μm]	SN	\geq	0.1240
M0.CS.3.4	Space to M0 [width = 0.080 μm] in NMINP direction [same color, PRL > 0.060 μm]	SN	\geq	0.1300
M0.CS.3.5	Space to M0 [width = 0.100 μm] in NMINP direction [same color, -0.060 μm < PRL \leq 0.060 μm]	SN	\geq	0.1240
M0.CS.3.6	Space to M0 [width = 0.100 μm] in NMINP direction [same color, PRL > 0.060 μm]	SN	\geq	0.1400
M0.CS.3.7	Space to M0 [width = 0.120 μm] in NMINP direction [same color, -0.060 μm < PRL \leq 0.060 μm]	SN	\geq	0.1240
M0.CS.3.8	Space to M0 [width = 0.120 μm] in NMINP direction [same color, PRL > 0.060 μm]	SN	\geq	0.1400
M0.CS.3.9	Space of M0 [width = 0.140 μm with edge length > 0.060 μm in MINP direction] to M0 [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, 0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1300
M0.CS.3.10	Space to M0 [width = 0.140 μm] in NMINP direction [same color, PRL > 0.080 μm]	SN	\geq	0.1600
M0.CS.3.11	Space of M0 [width \geq 0.180 μm with edge length > 0.060 μm in MINP direction] to M0 [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, 0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1400
M0.CS.3.12	Space to M0 [width \geq 0.180 μm] in NMINP direction [same color, PRL > 0.080 μm]	SN	\geq	0.1800

Rule No.	Description	Label	Op.	Rule
M0.CS.3.13	Space of M0 [width \geq 0.260 μm with edge length $> 0.060 \mu\text{m}$ in MINP direction] to M0 [with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [same color, 0 $\mu\text{m} < \text{PRL} \leq 0.080 \mu\text{m}$]	SN	\geq	0.1800
M0.CS.3.14	Space to M0 [width \geq 0.260 μm] in NMINP direction [same color, PRL $> 0.080 \mu\text{m}$]	SN	\geq	0.2600
M0.CS.5.1	M0 end-end/end-run space [$\text{PRL} > -0.060 \mu\text{m}$] in NMINP direction	CS5A	\geq	0.1080
M0.CS.5.3	M0 end-end/end-run space [$\text{PRL} > -0.060 \mu\text{m}$] in MINP direction	CS5C	\geq	0.1080
M0.CS.6.1	Corner projected space of M0 [same color, $-0.100 \mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$] (Except following conditions: 1. Corner with edge length $\leq 0.028 \mu\text{m}$ on both sides)	CS6A	\geq	0.1000
M0.CS.8	More than one {M0CA OR DM0_DO1} interact M0CB_Corner_Projected_Region from the same short side is not allowed M0CB_Corner_Projected_Region definition: The corner projected space of {M0CB OR DM0_DO2} edge [width $\leq 0.060 \mu\text{m}$] $< 0.054 \mu\text{m}$ in NMINP direction [$-0.026 \mu\text{m} < \text{PRL} < 0 \mu\text{m}$]			
M0.CS.10	{M0CA OR DM0_DO1} interact {M0CB OR DM0_DO2} is not allowed			
M0.CS.14	Forbidden space of M0_Critical_Group to M0 [width $\leq 0.028 \mu\text{m}$] in MINP direction [$\text{PRL} > 0 \mu\text{m}$] (Except BLK_WB, or following conditions: 1. M0_Groups_Projection_Region fully projected by another M0 [width $> 0.028 \mu\text{m}$] or {CCP_9 OR CCP_8}) Definition of M0_Critical_Group: { {M0 [width $\leq 0.028 \mu\text{m}$] SIZING up/down 0.034 μm in MINP direction} SIZING down/up 0.0495 μm in NMINP direction} [$0.100 \mu\text{m} \leq \text{width in MINP direction} \leq 0.630 \mu\text{m}$, width in NMINP direction $\geq 0.100 \mu\text{m}$] Definition of M0_Critical_Groups_Projection_Region: Enclosed region formed by M0_Critical_Groups, PRL $> 0 \mu\text{m}$	CS14	=	0.0690~0.1390, 0.1530~0.2190, 0.2410~0.2990
M0.CS.15	Forbidden space of M0 in MINP direction [$\text{PRL} > 0 \mu\text{m}$] [one side is M0 [width = 0.040 μm] the other side is M0 [width = 0.020 μm]]	CS15	=	0.2510~0.2940, 0.3410~0.3590
M0.CS.15.1	Forbidden space of M0 in MINP direction [$\text{PRL} > 0 \mu\text{m}$] [one side is M0 [width = 0.040 μm] the other side is M0 [width = 0.022/0.024 μm]]	CS15A	=	0.2510~0.2620, 0.2640~0.2750, 0.2780~0.2940
M0.CS.16	Forbidden space of M0 in MINP direction [$\text{PRL} > 0 \mu\text{m}$] [one side is M0 [width = 0.060 μm] the other side is M0 [width = 0.020 μm]]	CS16	=	0.2510~0.2940, 0.3410~0.3590
M0.CS.16.1	Forbidden space of M0 in MINP direction [$\text{PRL} > 0 \mu\text{m}$] [one side is M0 [width = 0.060 μm] the other side is M0 [width = 0.022/0.024 μm]]	CS16A	=	0.2450~0.2520, 0.2540~0.2650, 0.2680~0.2940
M0.CS.17	Forbidden space of M0 in MINP direction [$\text{PRL} > 0 \mu\text{m}$] [one side is M0 [width = 0.080 μm] the other side is M0 [width $\leq 0.024 \mu\text{m}$]]	CS17	=	0.2510~0.2550, 0.2570~0.2940
M0.CS.18	Forbidden space of M0 in MINP direction [$\text{PRL} > 0 \mu\text{m}$] [one side is M0 [$0.100 \mu\text{m} \leq \text{width} < 0.140 \mu\text{m}$] the other side is M0 [width $\leq 0.024 \mu\text{m}$]]	CS18	=	0.2510~0.2940
M0.CS.19	Forbidden space of M0 in MINP direction [$\text{PRL} > 0.060 \mu\text{m}$] [one side is M0 [width $\geq 0.140 \mu\text{m}$] the other side is M0 [width $\leq 0.024 \mu\text{m}$]]	CS19	=	0.2510~0.2940

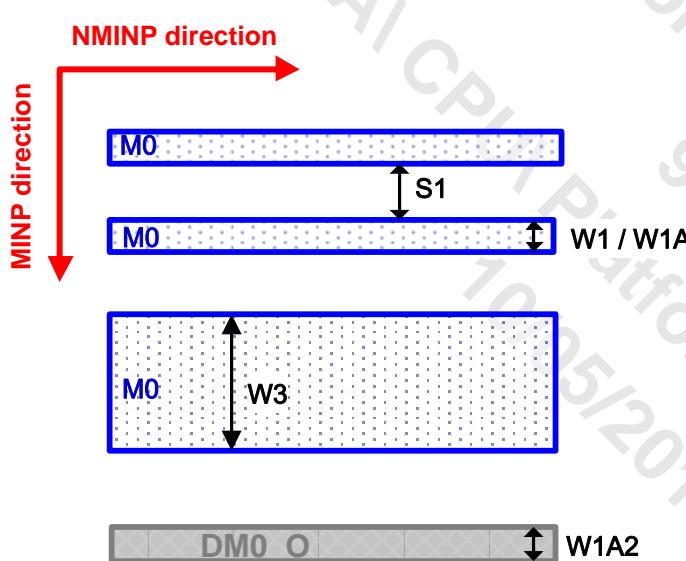
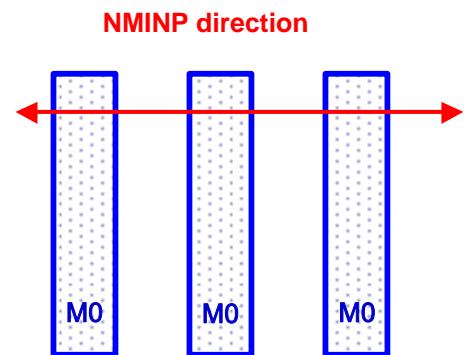
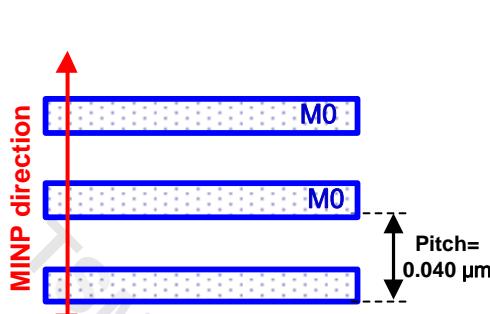
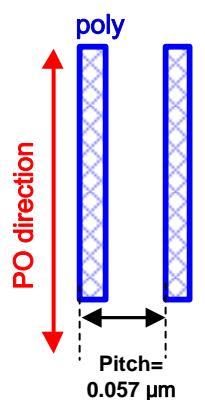
Table Notes:

- To meet the metal process window, filling the dummy metal globally and uniformly by tsmc utility is needed even if the originally drawn M0 has already met the density rules. For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, filling manually and evenly is still needed.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations during placement. Unexpected violations may occur during the IP/macro placement due to the environment, even if the IP/macro already passed the high density rule check. Therefore, customers need to carefully design the dimension of the width/space for wide metal (e.g., power/ground bus), under the proper high density limit.
- Please refer to section 3.9 DRC methodology of net voltage recognition and delta voltage calculation in high voltage spacing rules.

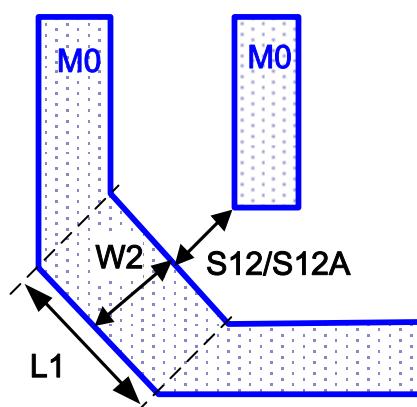
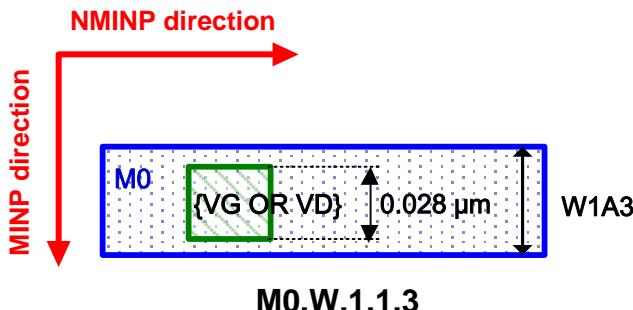
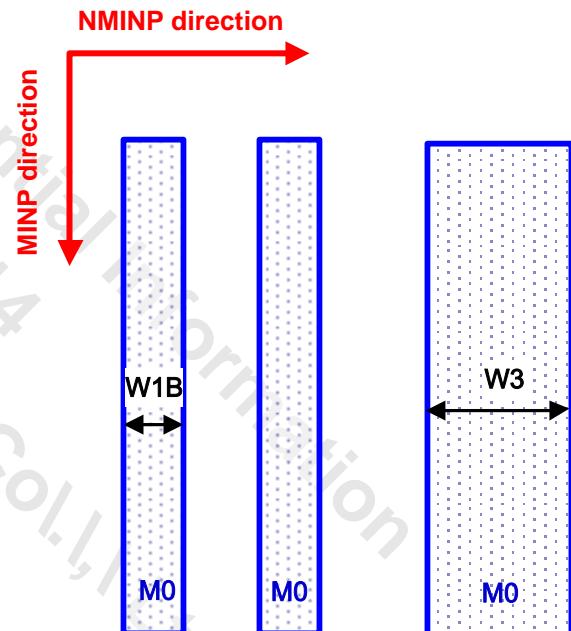
TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

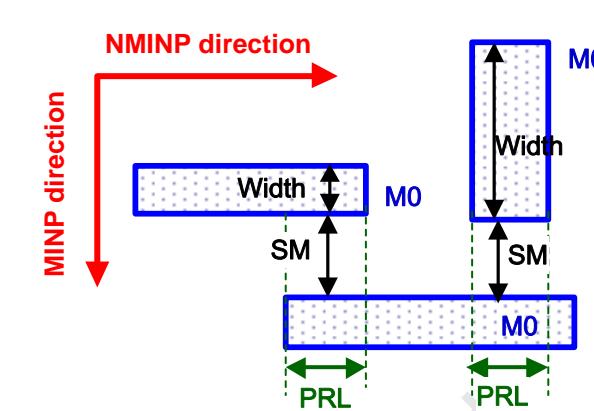
M0

- M0 MINP direction is parallel with PO direction
- M0 NMINP direction is perpendicular to PO direction.

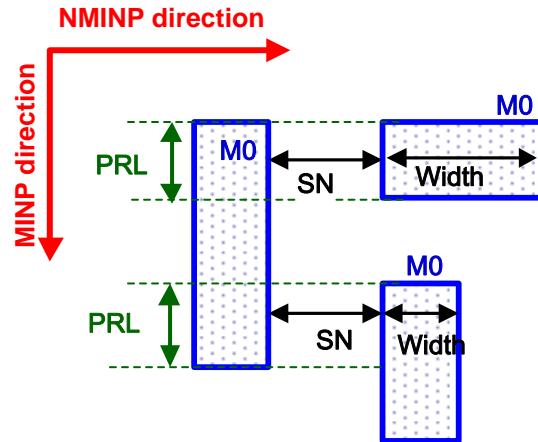


**M0.W.1 / M0.W.1.1 / M0.W.1.1.2 /
M0.W.3 / M0.S.1**

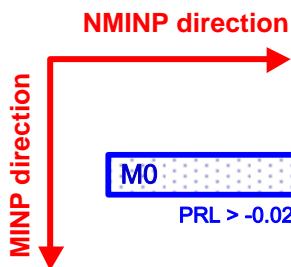




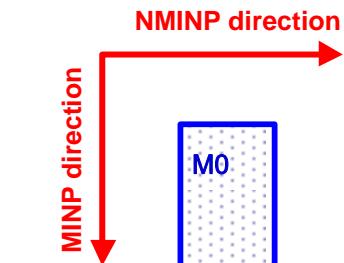
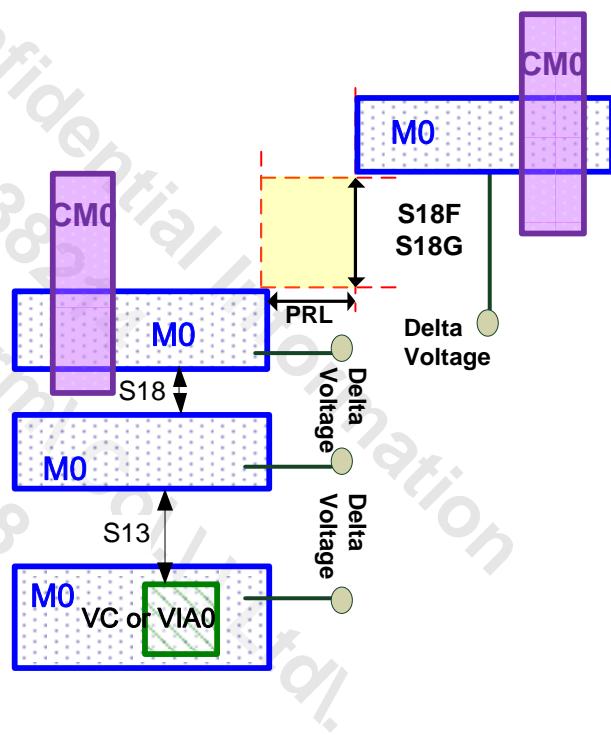
M0.S.2 / M0.S.2.1 / M0.S.2.3 /
M0.S.2.3.1 / M0.S.2.4 / M0.S.2.5 /
M0.S.2.6



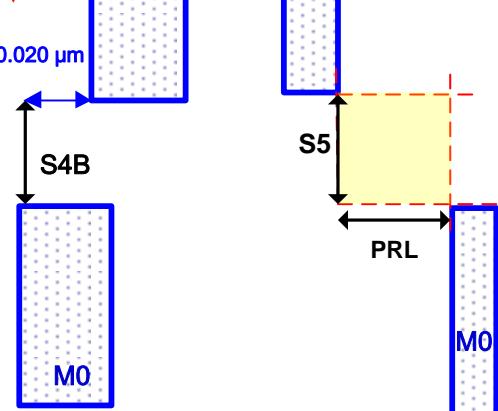
M0.S.3.1 / M0.S.3.2 / M0.S.3.3 / M0.S.3.4 /
M0.S.3.5 / M0.S.3.6 / M0.S.3.7 / M0.S.3.8 /
M0.S.3.9 / M0.S.3.10



M0.S.4.1

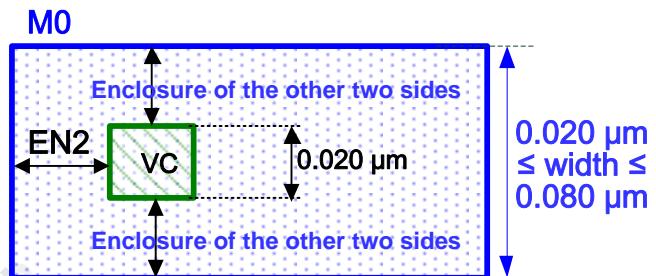
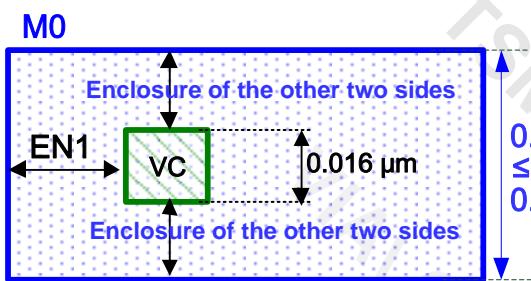
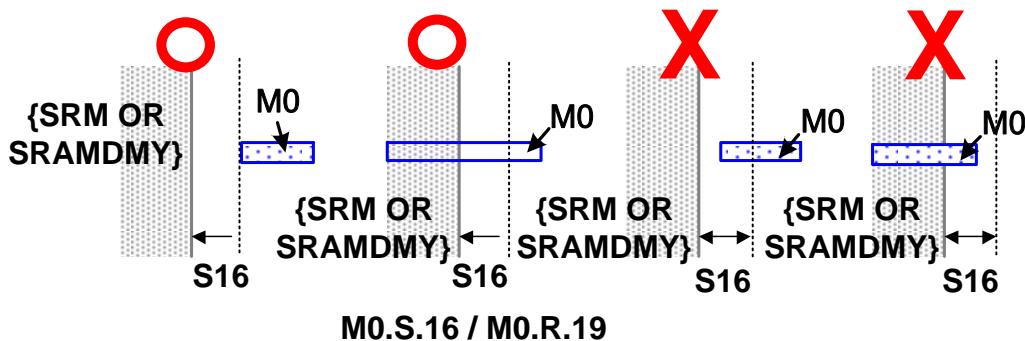


M0.S.13.1 / M0.S.13.2 / M0.S.13.3 / M0.S.13.4 / M0.S.13.5
M0.S.18 / M0.S.18.1 / M0.S.18.2 / M0.S.18.3 / M0.S.18.4
M0.S.18.6 / M0.S.18.7



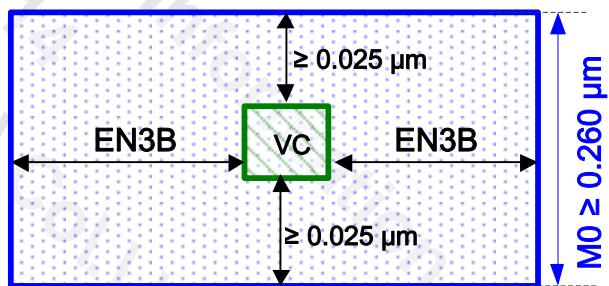
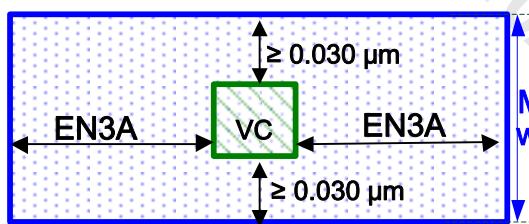
M0.S.4.2

M0.S.5



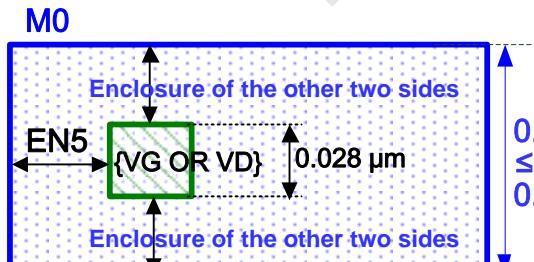
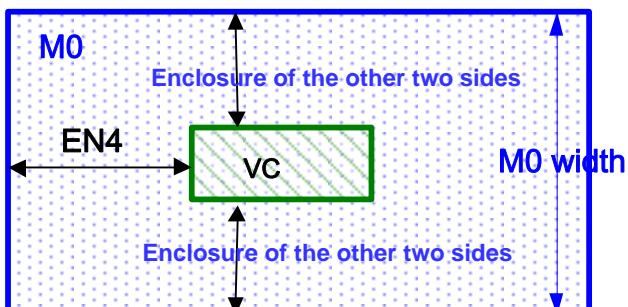
**M0.EN.1 / M0.EN.1.1 / M0.EN.1.2 /
M0.EN.1.3 / M0.EN.1.4 / M0.EN.1.5 /
M0.EN.1.7 / M0.EN.1.8**

**M0.EN.2 / M0.EN.2.1 / M0.EN.2.2 /
M0.EN.2.3 / M0.EN.2.4 / M0.EN.2.5 /
M0.EN.2.7 / M0.EN.2.8**



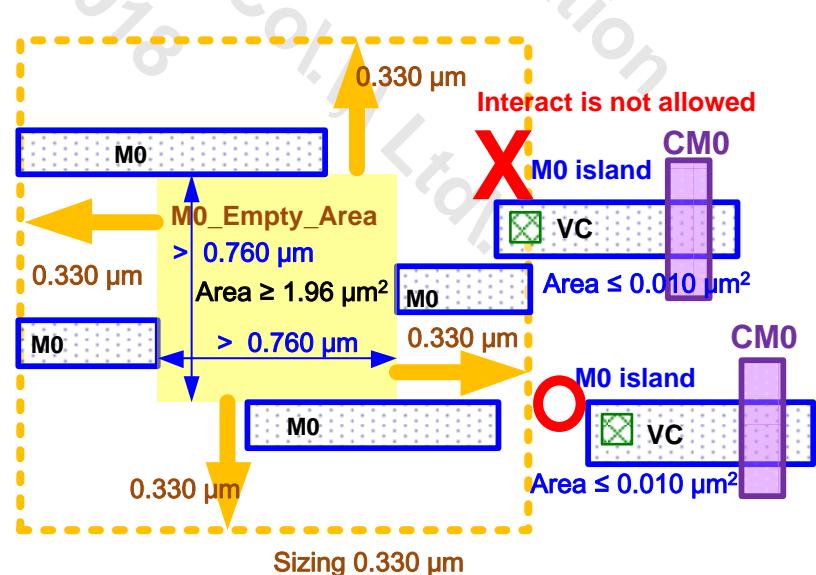
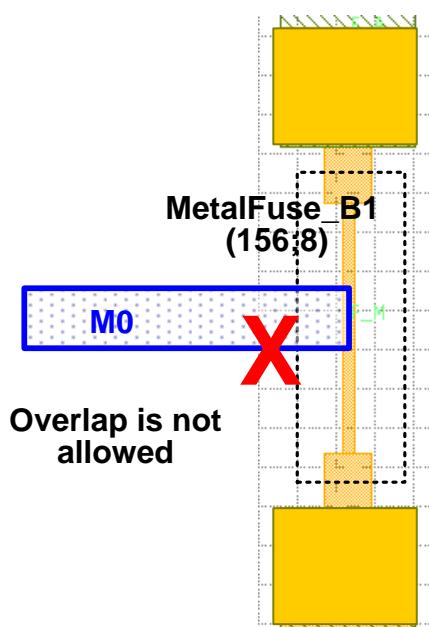
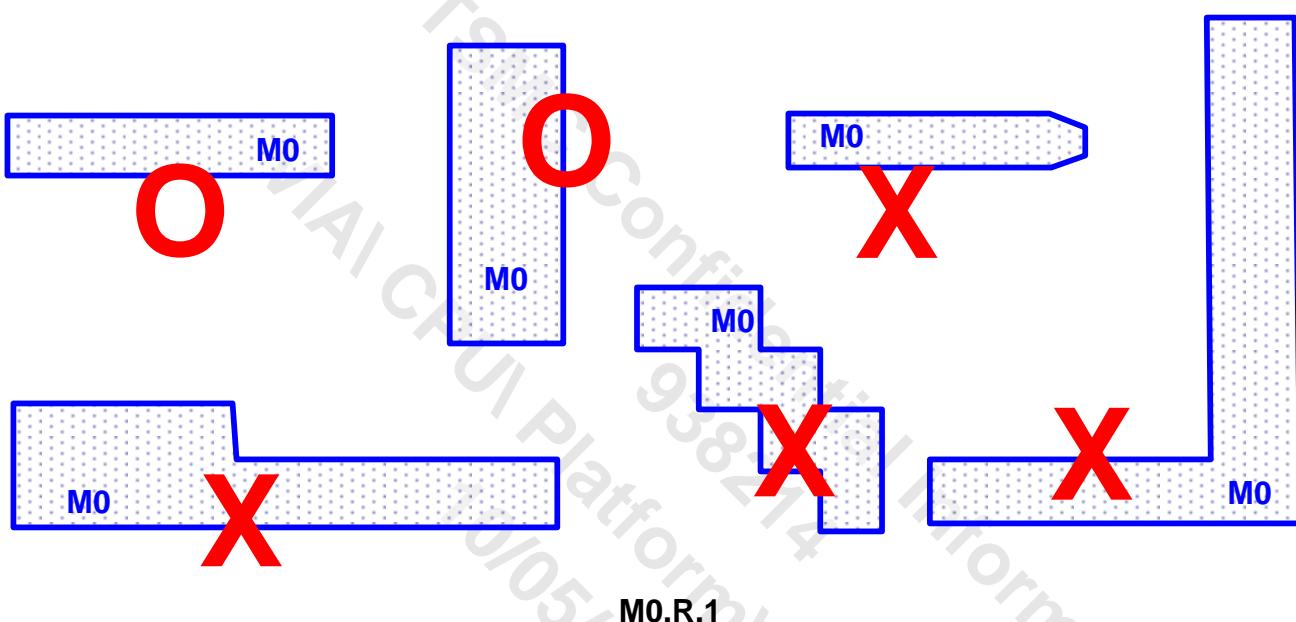
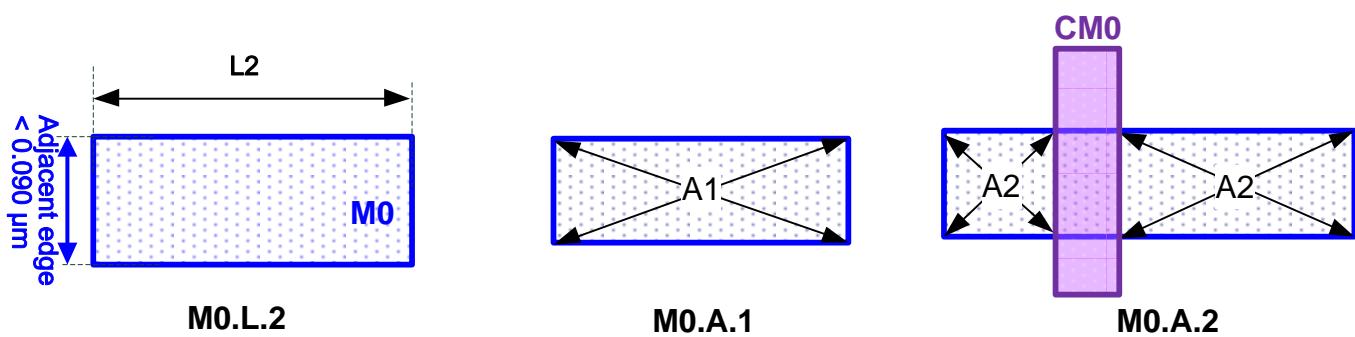
M0.EN.3.1

M0.EN.3.2



**M0.EN.4 / M0.EN.4.1 / M0.EN.4.2 / M0.EN.4.3 /
M0.EN.4.4 / M0.EN.4.5 / M0.EN.4.7 /
M0.EN.4.7.1 / M0.EN.4.8**

M0.EN.5.1 / M0.EN.5.2 / M0.EN.5.3

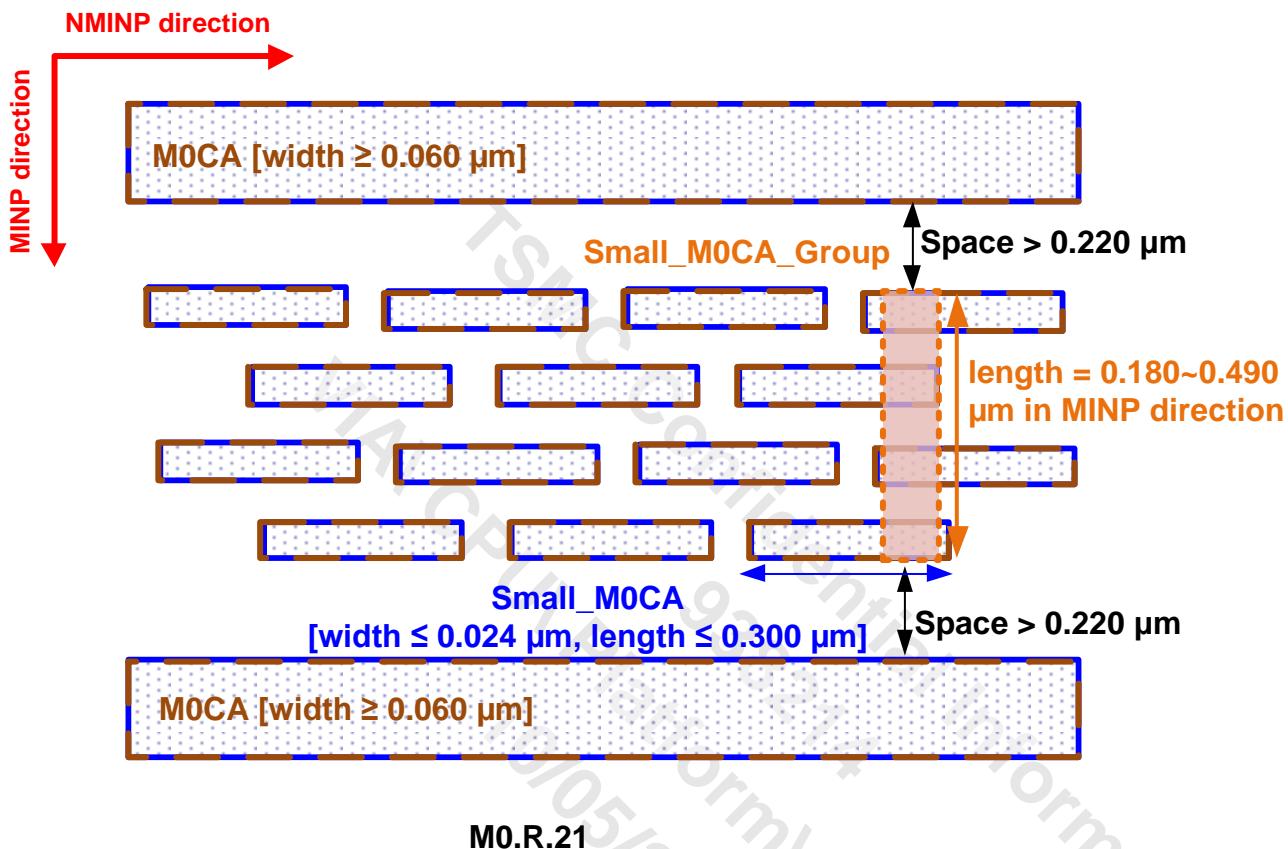


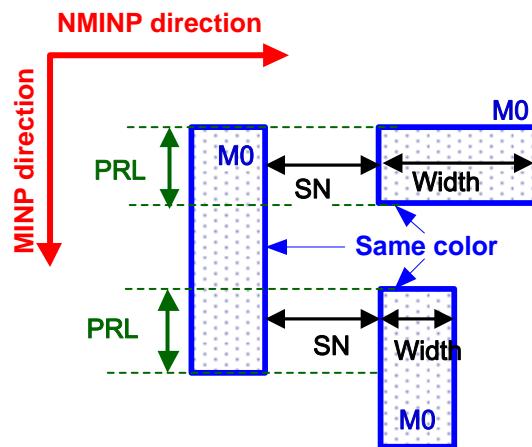
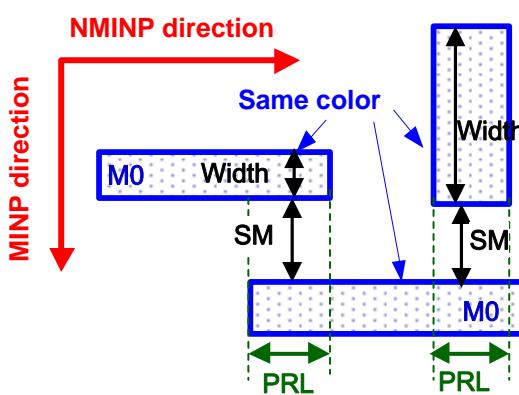
Small_M0CA_Group:

{{{Small_M0CA SIZING up/down 0.033 μm in MINP direction} SIZING down/up 0.0895 μm in MINP direction} [length < 0.140 μm in NMINP direction]} [length = 0.180~0.490 μm in MINP direction]}

Small_M0CA:

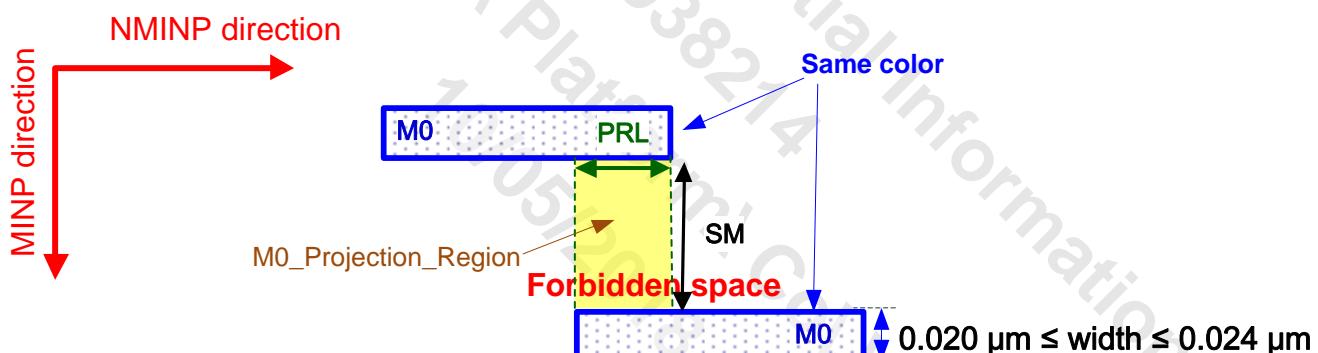
M0CA [width $\leq 0.024 \mu\text{m}$ in MINP direction, length $\leq 0.300 \mu\text{m}$ in NMINP direction]



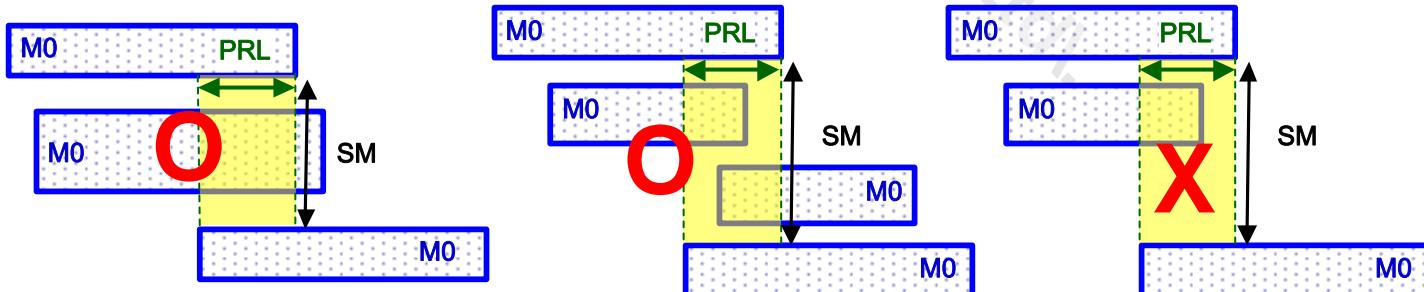


M0.CS.0.1 / M0.CS.1.1 / M0.CS.1.1.1 /
M0.CS.1.1.2 / M0.CS.1.1.3 / M0.CS.1.1.4 /
M0.CS.1.1.7 / M0.CS.1.2.1 / M0.CS.1.2.2 /
M0.CS.1.3 / M0.CS.1.3.1 / M0.CS.1.4 /
M0.CS.1.6 / M0.CS.1.7 / M0.CS.1.8 /
M0.CS.1.9 / M0.CS.1.10 / M0.CS.1.11

M0.CS.0.2 / M0.CS.3.2 / M0.CS.3.3 / M0.CS.3.4 /
M0.CS.3.5 / M0.CS.3.6 / M0.CS.3.7 / M0.CS.3.8 /
M0.CS.3.9 / M0.CS.3.10 / M0.CS.3.11 /
M0.CS.3.12 / M0.CS.3.13 / M0.CS.3.14



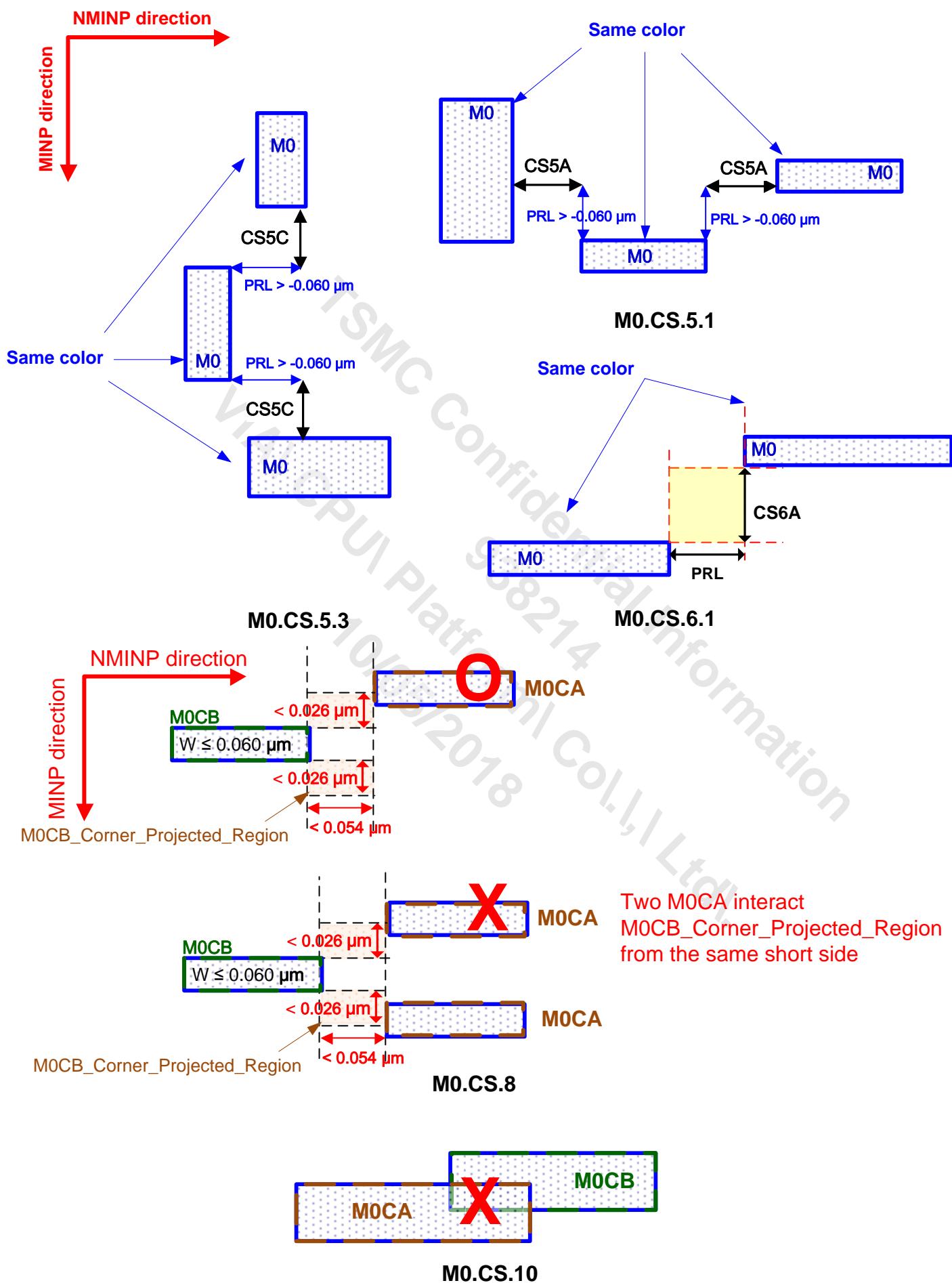
Exception

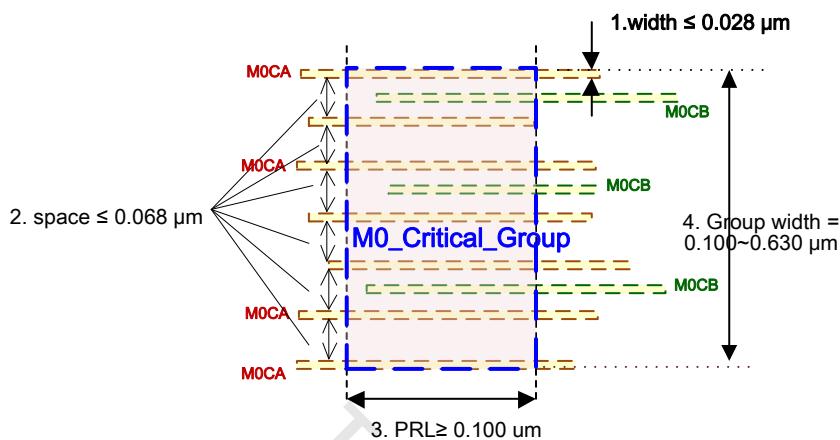


M0_Projection_Region fully projected by another M0
[width > 0.024 μm] or {CCP_9 OR CCP_8}

Not fully projected

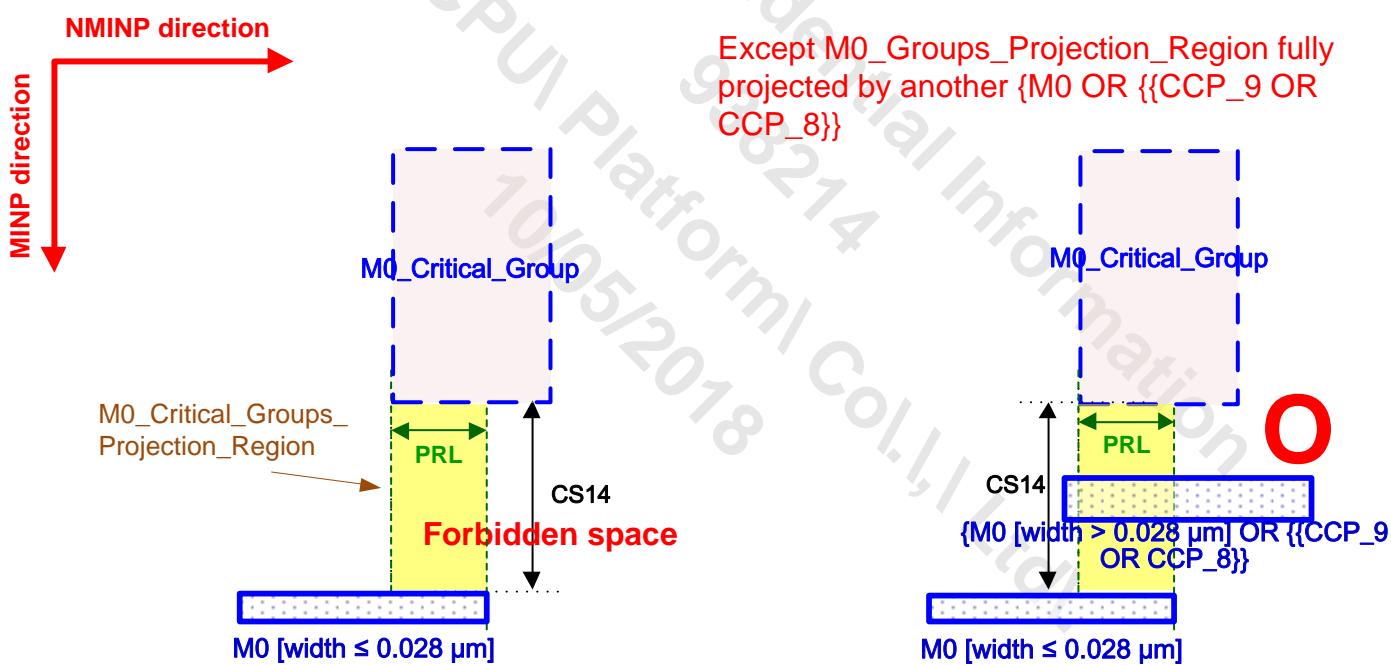
M0.CS.1.1.6



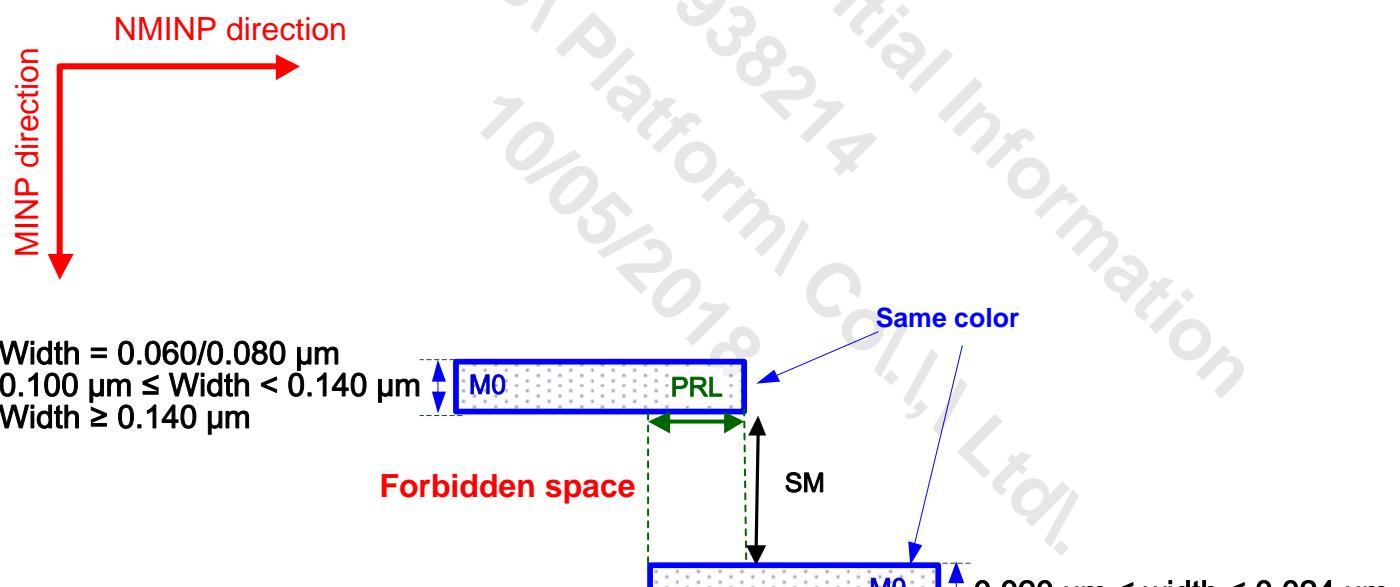
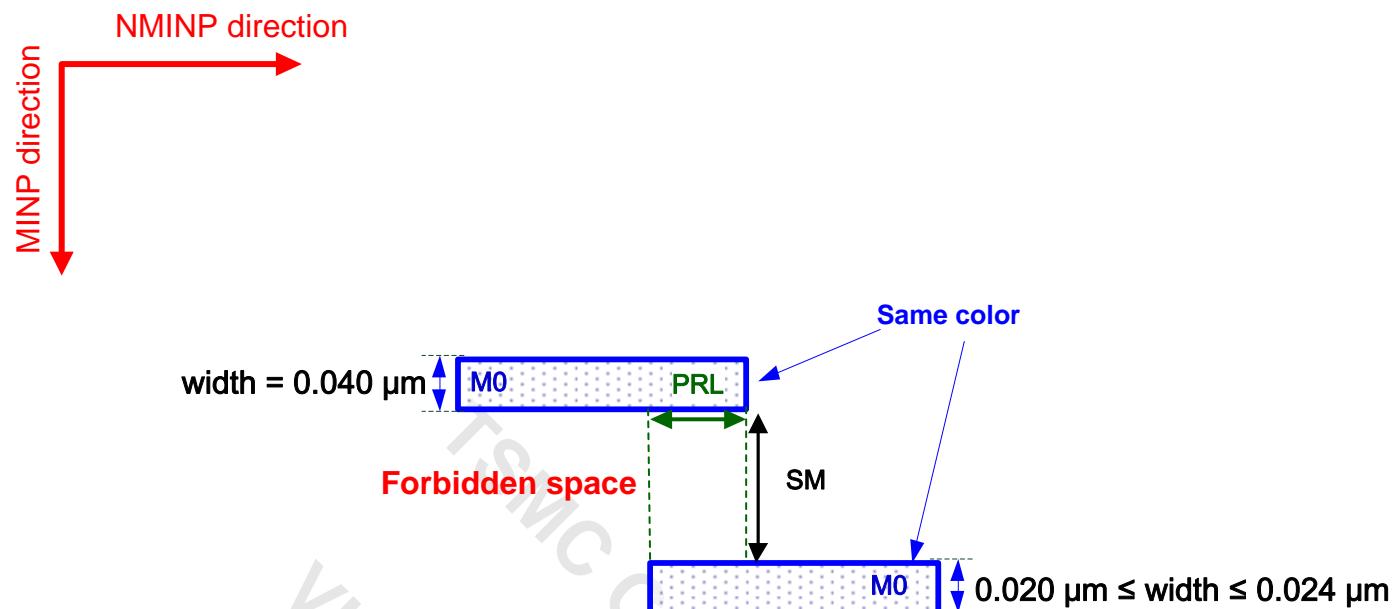


Definition of M0_Critical_Group:

$\{\{M0 [\text{width} \leq 0.028 \mu\text{m}] \text{ SIZING up/down } 0.034 \mu\text{m}\}$
 $\text{SIZING down/up } 0.0495 \mu\text{m in NMNP direction}\} [0.100 \mu\text{m}$
 $\leq \text{width in MINP direction} \leq 0.630 \mu\text{m}\}$



M0.CS.14



4.5.40 Cut-M0 (CM0) Layout Rules

CM0A (CAD layer: 180;109) is used to cut M0CA.

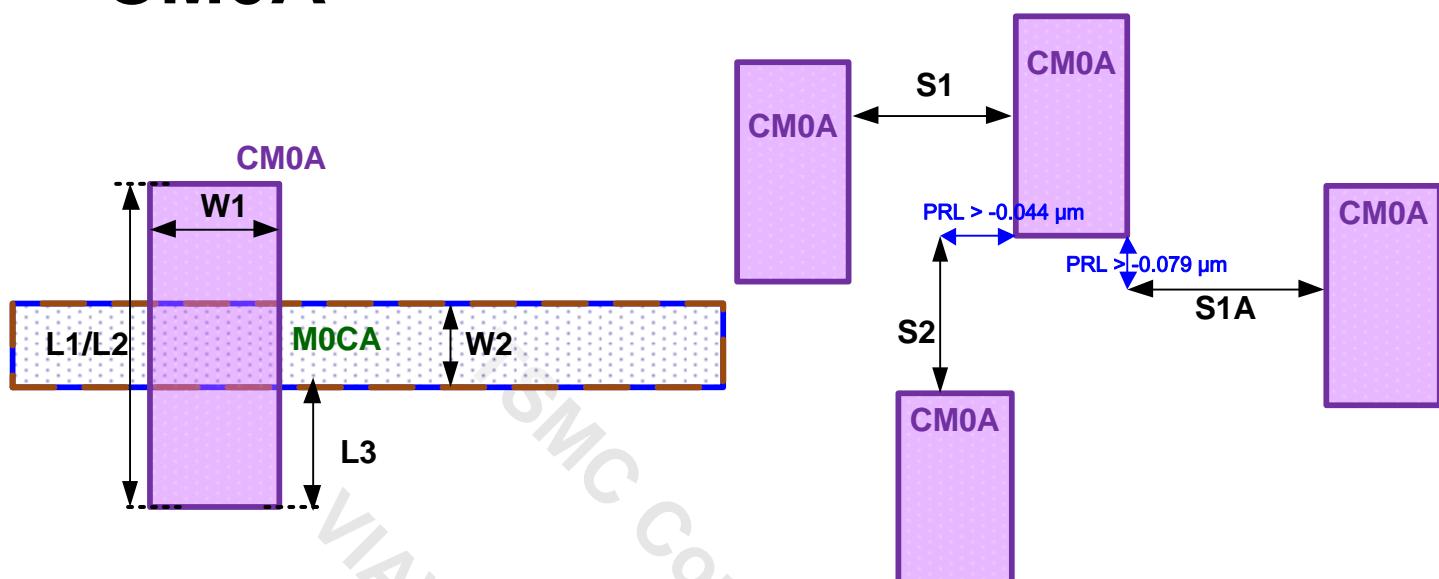
CM0B (CAD layer: 180;110) is used to cut M0CB.

Rule No.	Description	Label	Op.	Rule
CM0A.W.1	Width in horizontal direction (Except BLK_WB)	W1	=	0.0240
CM0A.W.2	Maximum width of M0CA [CUT by CM0A] (in perpendicular direction to CM0A) (Except BLK_WB)	W2	\leq	0.0600
CM0A.S.1	Space (Except following conditions: 1. both CM0A interact BCM0VA or BCM0H)	S1	\geq	0.0840
CM0A.S.1.1	Space of long side of CM0A [PRL > -0.079 μm] (Except following conditions: 1. both CM0A interact BCM0VA or BCM0H)	S1A	\geq	0.0840
CM0A.S.2	Space of short side of CM0A [PRL > -0.044 μm] (Except CCP_9, CCP_8, BLK_WB)	S2	\geq	0.1200
CM0A.S.3	Space to M0CA	S3	\geq	0.0140
CM0A.S.3.1	Space of short side of CM0A to M0CA	S3A	\geq	0.0300
CM0A.S.4	Space of CM0A edge [INSIDE M0CA] to VC [PRL > 0 μm] (VC [INTERACT M0CA] overlap CM0A is not allowed) (Except FB_9, FB_8, BLK_WB)	S4	\geq	0.0085
CM0A.S.4.1	Space of CM0A edge [INSIDE M0CA] to Checked_VC [PRL > 0 μm] (Except FB_9, FB_8, BLK_WB) Definition of Checked_VC: VC follow one of following conditions: 1. VC [INTERACT ALL_MD] or, 2. VC [INTERACT M0CA width < 0.024 μm , space to M0CB < 0.029 μm , NOT INSIDE Checked_M0] Definition of Checked_M0: { {{M0 SIZING up/down 0.0125 μm } SIZING -0.080 μm in vertical direction} SIZING -0.100 μm in horizontal direction}	S4A	\geq	0.0200
CM0A.S.5	Space of CM0A edge [INSIDE M0CA] to VIA0 [PRL > 0 μm] (Except FB_9, FB_8, BLK_WB)	S5	\geq	0.0170
CM0A.S.6	Space to {SRM (50;0) OR SRAMDMY (186;0)} ({CM0A CUT {SRM (50;0) OR SRAMDMY (186;0)}} is not allowed)	S6	\geq	0.1180
CM0A.O.1	Overlap of M0CA in CM0A width direction (Except BLK_WB)	O1	=	0.0240
CM0A.EX.1	Extension on M0CA in CM0A length direction	EX1	\geq	0.0300
CM0A.EX.1.1	Extension on M0CA [width > 0.028 μm or MINP space to M0 [PRL to CM0A short side > -0.022 μm] \geq 0.075 μm in CM0A length direction] (Except BLK_WB)	EX1A	\geq	0.0450
CM0A.L.1	Length in vertical direction	L1	\geq	0.0800
CM0A.L.2	Maximum length (Except BLK_WB)	L2	\leq	0.5000
CM0A.L.3	Maximum length of {CM0A NOT MOCA}	L3	\leq	0.1860
CM0A.L.4	Length of CM0A [INTERACT BCM0H]	L4	\geq	0.1600
CM0A.DN.1	Maximum CM0A density across full chip (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	10%
CM0A.R.1	CM0A must be a rectangle orthogonal to grid			
CM0A.R.2	Any vertex of CM0A inside M0CA is not allowed			
CM0A.R.3	Forbidden the parallel direction to NMINP M0CA			
CM0A.R.4	CM0A must interact M0CA			
CM0A.R.6	Short side of M0CA interact CM0A is not allowed			

Rule No.	Description	Label	Op.	Rule
CM0B.W.1	Width in horizontal direction	W1	=	0.0240
CM0B.W.2	Maximum width of M0CB [CUT by CM0B] (in perpendicular direction to CM0B) (Except BLK_WB)	W2	\leq	0.0600
CM0B.S.1	Space (Except FB_9, FB_8, BLK_WB)	S1	\geq	0.0840
CM0B.S.1.1	Space of long side of CM0B [PRL > -0.079 μm] (Except FB_9, FB_8, BLK_WB, PO_P63)	S1A	=	0.0840, 0.0900, 0.0960, 0.1110, \geq 0.1160
CM0B.S.1.2	Space of long side of CM0B [PRL > -0.079 μm] [INSIDE PO_P63] (Except FB_9, FB_8, BLK_WB)	S1B	=	0.0840, 0.0900, 0.0960, 0.1020, 0.1110, \geq 0.1160
CM0B.S.2	Space of short side of CM0B [PRL > -0.056 μm] (Except CCP_9, CCP_8, BLK_WB)	S2	\geq	0.1200
CM0B.S.3	Space to M0CB	S3	\geq	0.0140
CM0B.S.3.1	Space of short side of CM0B to M0CB	S3A	\geq	0.0300
CM0B.S.3.2	Space to MOCA (Except BLK_WB)	S3B	\geq	0.0080
CM0B.S.3.3	Space of short side of CM0B to MOCA (Except DM0_DO1, BLK_WB)	S3C	\geq	0.0300
CM0B.S.4	Space of CM0B edge [INSIDE M0CB] to VC [PRL > 0 μm] (VC [INTERACT M0CB] overlap CM0B is not allowed) (Except FB_9, FB_8, BLK_WB, or following conditions: 1. space of CM0B edge to VC \geq 0.0065 μm [INSIDE M0CB, and M0CB either one side space to M0 \geq 0.060 μm in MINP direction])	S4	\geq	0.0085
CM0B.S.4.1	Space of CM0B edge [INSIDE M0CB] to Checked_VC [PRL > 0 μm] (Except FB_9, FB_8, BLK_WB) Definition of Checked_VC: VC follow one of following conditions: 1. VC [INTERACT ALL_MD] or, 2. VC [INTERACT M0CB width < 0.024 μm , space to M0CA < 0.029 μm , NOT INSIDE Checked_M0] Definition of Checked_M0: { {{M0 SIZING up/down 0.0125 μm } SIZING -0.080 μm in vertical direction} SIZING -0.100 μm in horizontal direction}	S4A	\geq	0.0200
CM0B.S.5	Space of CM0B edge [INSIDE M0CB] to VIA0 [PRL > 0 μm] (Except FB_9, FB_8, BLK_WB)	S5	\geq	0.0170
CM0B.S.6	Space to {SRM (50;0) OR SRAMDMY (186;0)} ({CM0B CUT {SRM (50;0) OR SRAMDMY (186;0)}} is not allowed)	S6	\geq	0.1180
CM0B.S.7	Forbidden space of P855_Group in horizontal direction Definition of P855_Space: Space region = 0.0615 μm in horizontal direction formed by CM0B [length \geq 0.160 μm , PRL \geq 0.160 μm] Definition of P855_Group: {P855_Space SIZING 0.024 μm in horizontal direction}	S7	=	0.0960~0.1260
CM0B.O.1	Overlap of M0CA in CM0B width direction	O1	\geq	0.0120
CM0B.O.2	Overlap of M0CB in CM0B width direction	O2	=	0.0240
CM0B.EX.1	Extension on M0CB in CM0B length direction	EX1	\geq	0.0300
CM0B.EX.1.1	Extension on M0CB [width > 0.028 μm or MINP space to M0 [PRL to CM0B short side > -0.022 μm] \geq 0.075 μm in CM0B length direction] (Except BLK_WB)	EX1A	\geq	0.0450

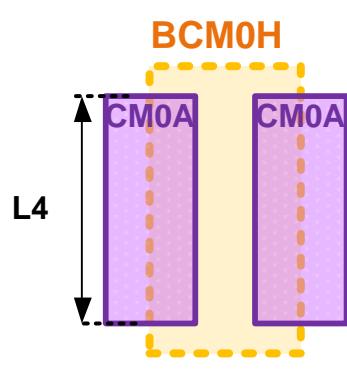
Rule No.	Description	Label	Op.	Rule
CM0B.L.1	Length in vertical direction	L1	\geq	0.0800
CM0B.L.4	Length of CM0B [INTERACT BCM0H]	L4	\geq	0.1600
CM0B.DN.1	Maximum CM0B density across full chip (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	10%
CM0B.R.1	CM0B must be a rectangle orthogonal to grid			
CM0B.R.2	Any vertex of CM0B inside M0CB is not allowed			
CM0B.R.3	Forbidden the parallel direction to NMINP M0CB			
CM0B.R.4	CM0B must interact M0CB			
CM0B.R.5	{CM0B INTERACT MOCA [width \geq 0.060 μm] is not allowed (Except following conditions: 1. CM0B interact CCP_9, CCP_8)}			
CM0B.R.6	Short side of M0CB interact CM0B is not allowed			
CM0B.R.7.1	P855_Group width in horizontal direction $>$ 1.221 μm is not allowed Definition of P855_Space: Space region = 0.0615 μm in horizontal direction formed by CM0B [length \geq 0.160 μm , PRL \geq 0.160 μm] Definition of P855_Group: {P855_Space SIZING 0.024 μm in horizontal direction}			
CM0B.R.7.1.1	P945_Group width in horizontal direction $>$ 0.969 μm is not allowed Definition of P945_Space: Space region = 0.0705 μm in horizontal direction formed by CM0B [length \geq 0.160 μm , PRL \geq 0.160 μm] Definition of P945_Group: {P945_Space SIZING 0.024 μm in horizontal direction}			
CM0B.R.7.2	P108_Group width in horizontal direction $>$ 0.348 μm is not allowed Definition of P108_Space: Space region = 0.084 μm in horizontal direction formed by CM0B [length \geq 0.160 μm , PRL \geq 0.160 μm] Definition of P108_Group: {P108_Space SIZING 0.024 μm in horizontal direction}			
CM0B.R.7.3	P114_Group width in horizontal direction $>$ 0.366 μm is not allowed (Except FB_9, FB_8) Definition of P114_Space: Space region = 0.090 μm in horizontal direction formed by CM0B [length \geq 0.160 μm , PRL \geq 0.160 μm] Definition of P114_Group: {P114_Space SIZING 0.024 μm in horizontal direction}			
CM0B.R.7.4	P120_Group width in horizontal direction $>$ 0.384 μm is not allowed Definition of P120_Space: Space region = 0.096 μm in horizontal direction formed by CM0B [length \geq 0.160 μm , PRL \geq 0.160 μm] Definition of P120_Group: {P120_Space SIZING 0.024 μm in horizontal direction}			
CM0B.R.7.5	P135_Group width in horizontal direction $>$ 0.429 μm is not allowed Definition of P135_Space: Space region = 0.111 μm in horizontal direction formed by CM0B [length \geq 0.160 μm , PRL \geq 0.160 μm] Definition of P135_Group: {P135_Space SIZING 0.024 μm in horizontal direction}			

CM0A

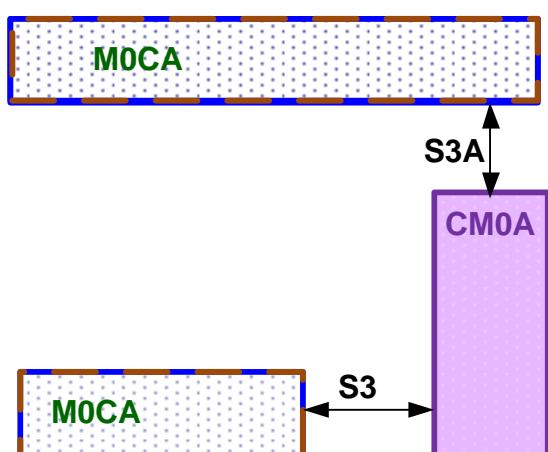


CM0A.W.1 / CM0A.W.2 / CM0A.L.1 /
CM0A.L.2 / CM0A.L.3

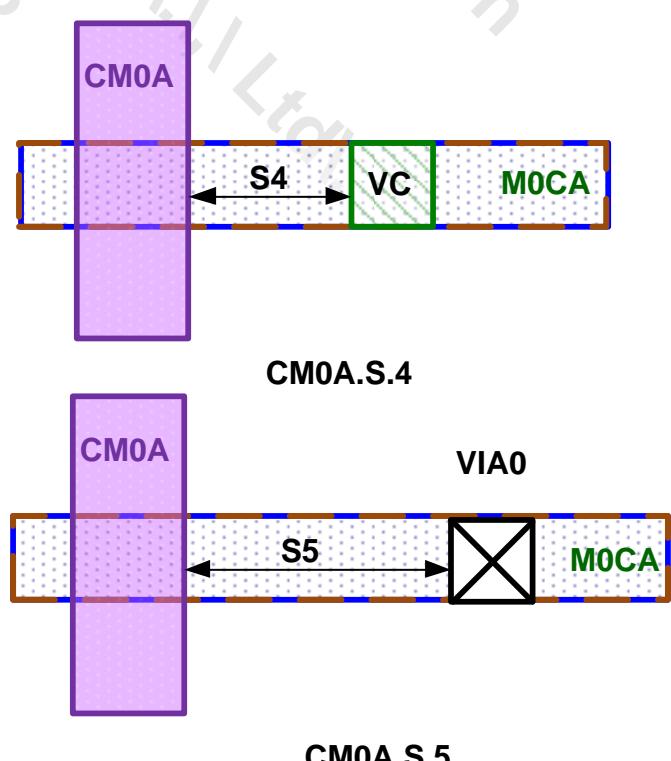
CM0A.S.1 / CM0A.S.1.1 / CM0A.S.2



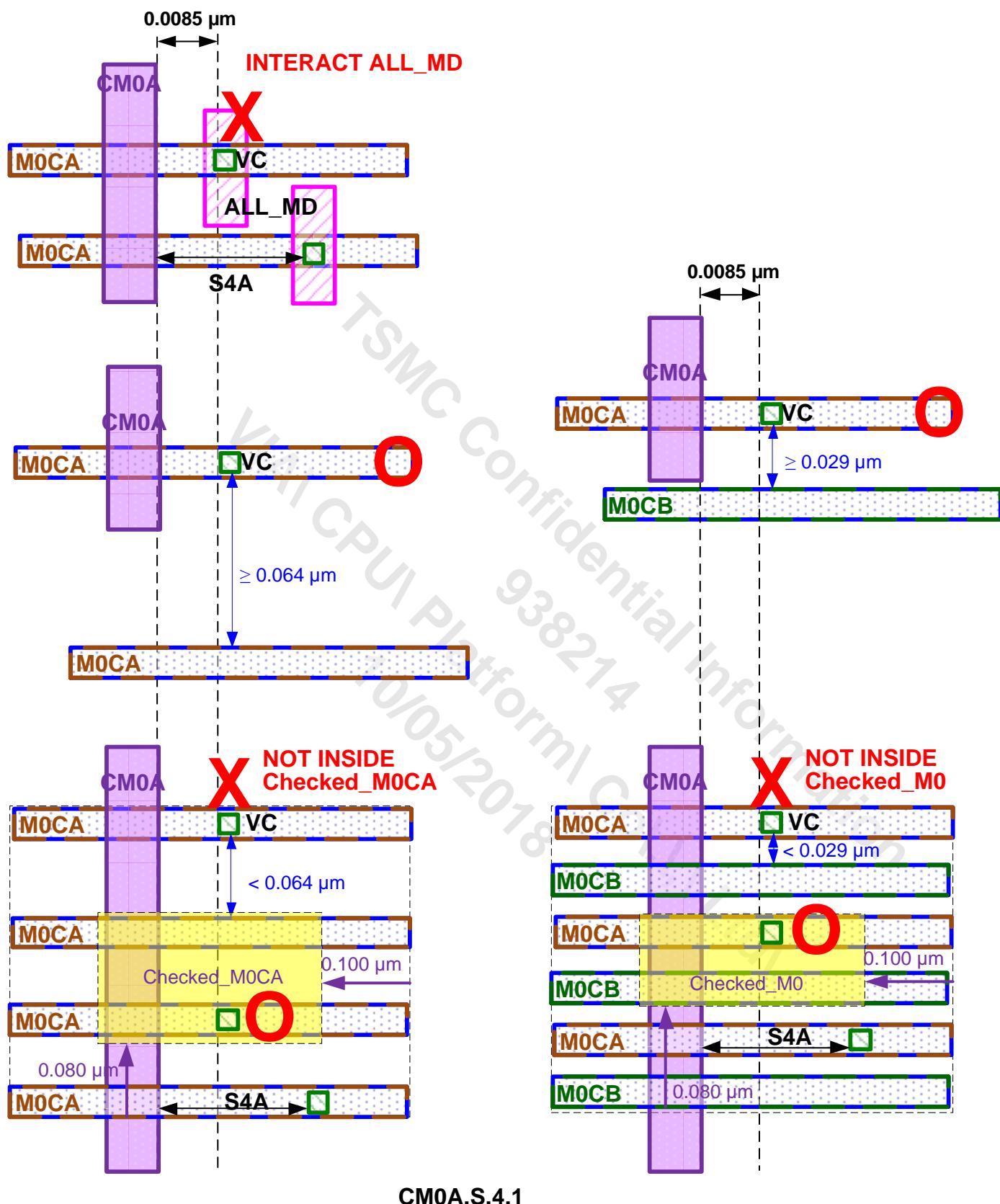
CM0A.L.4

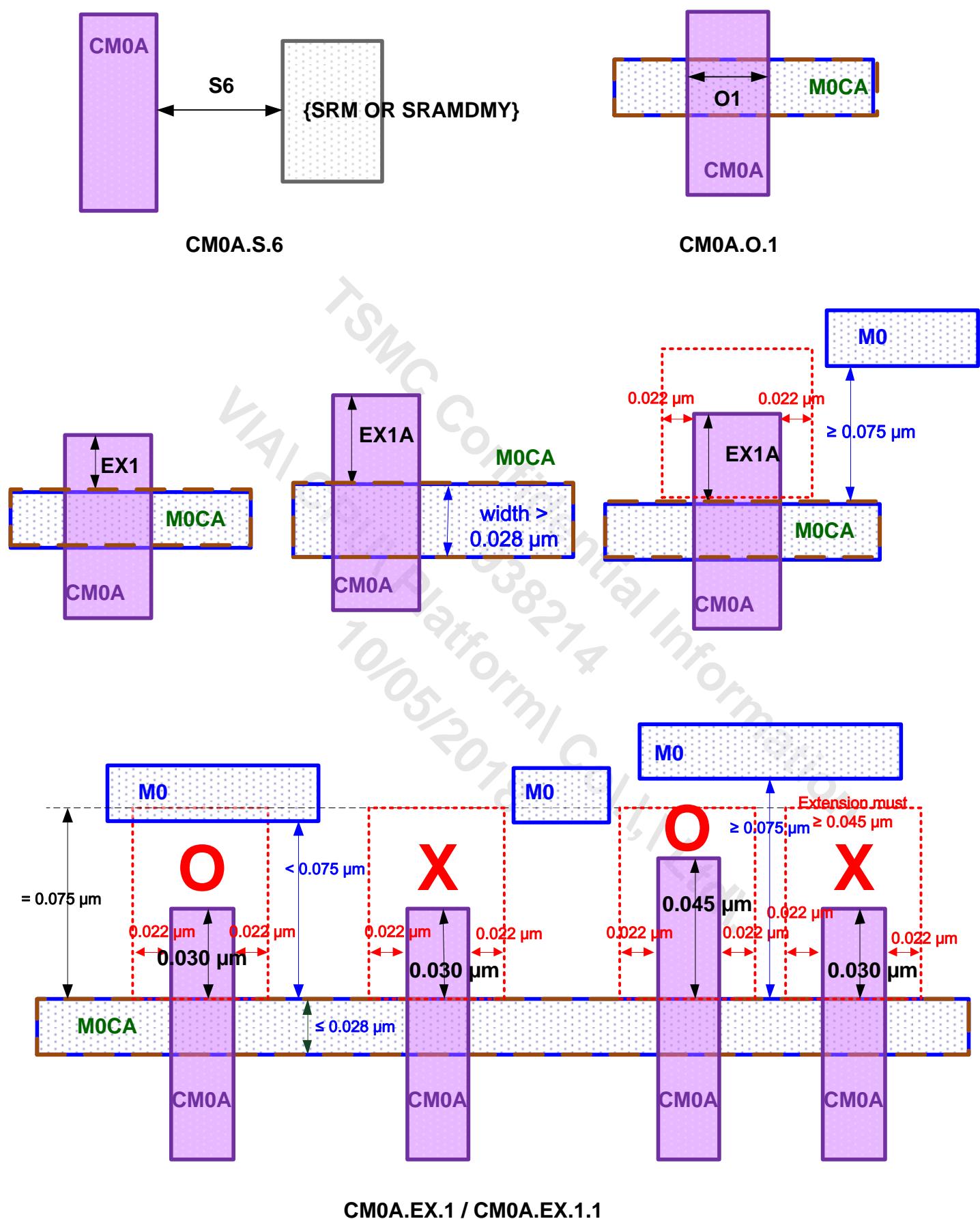


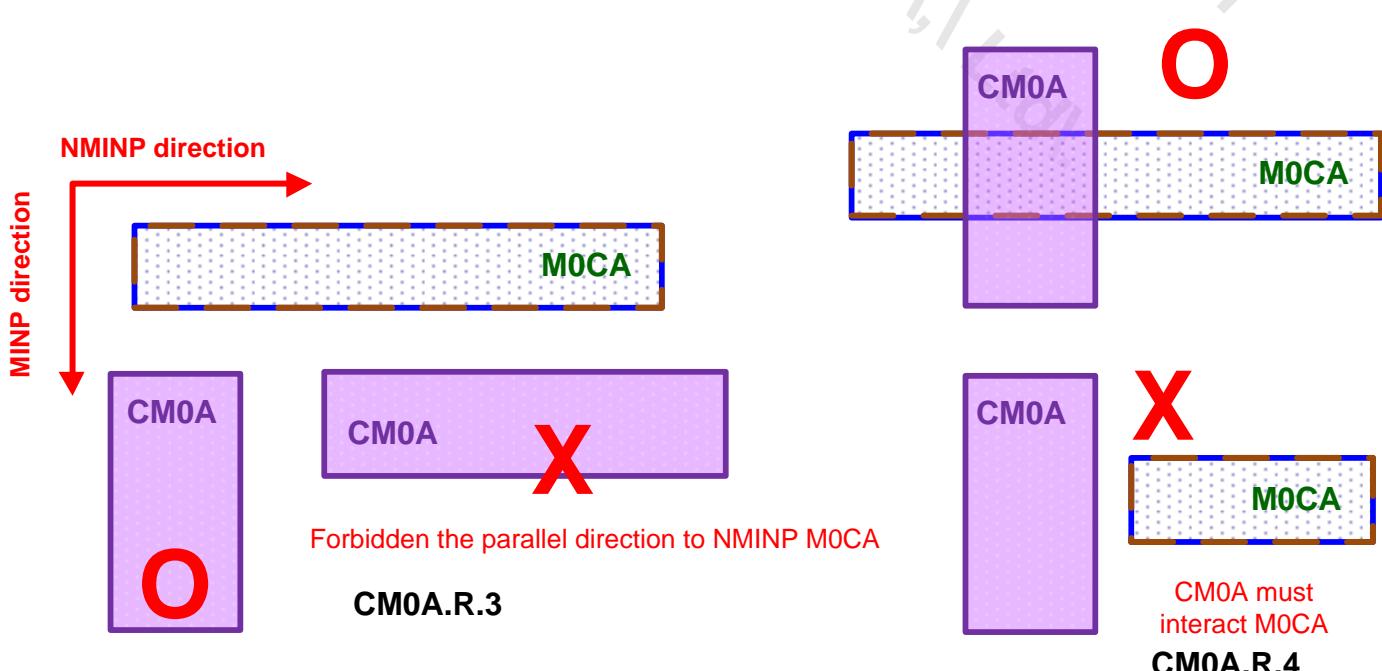
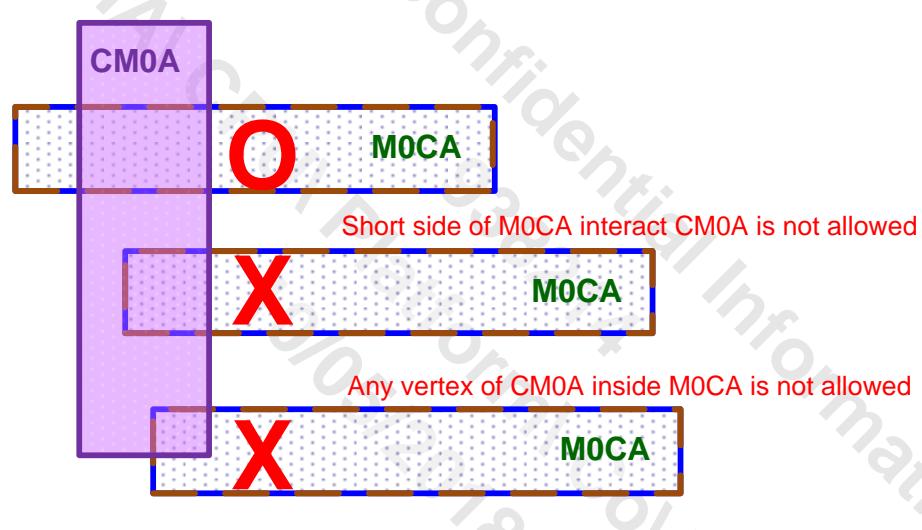
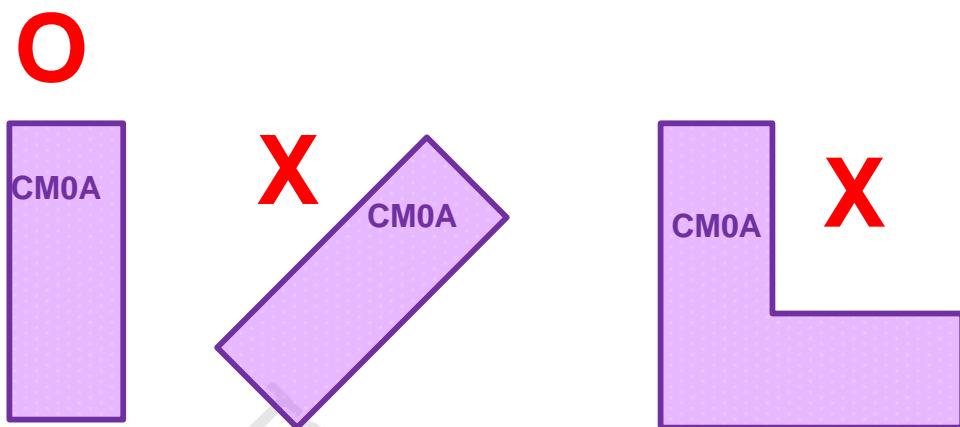
CM0A.S.3/ CM0A.S.3.1

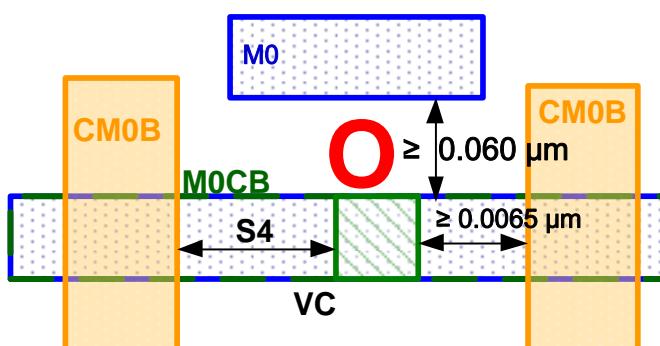
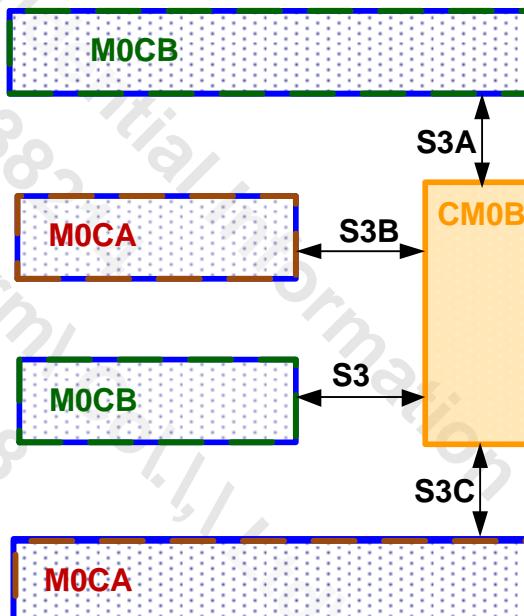
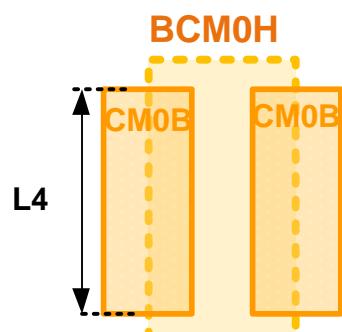
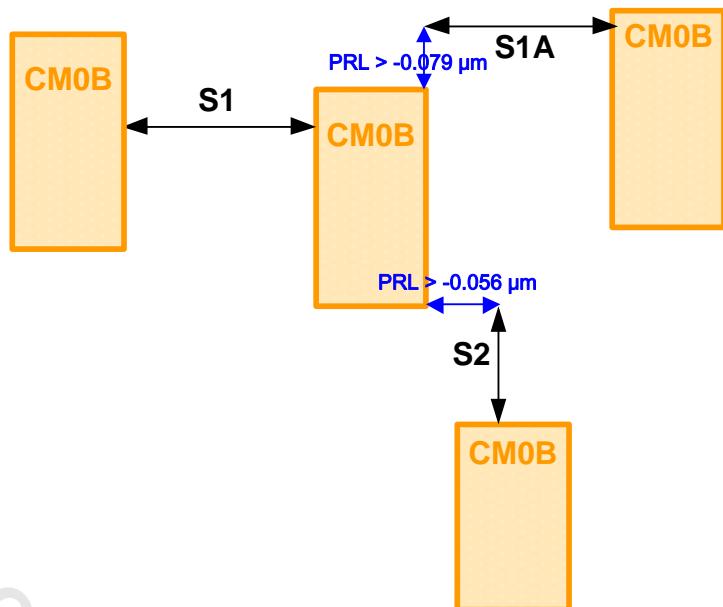
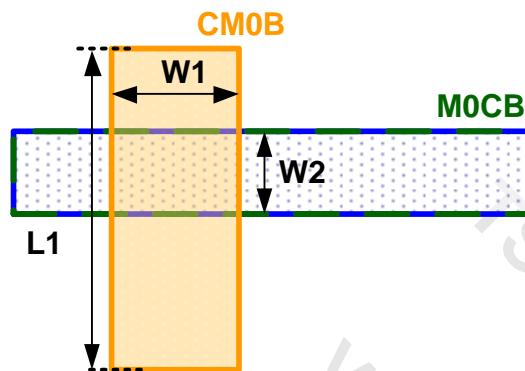


CM0A.S.5

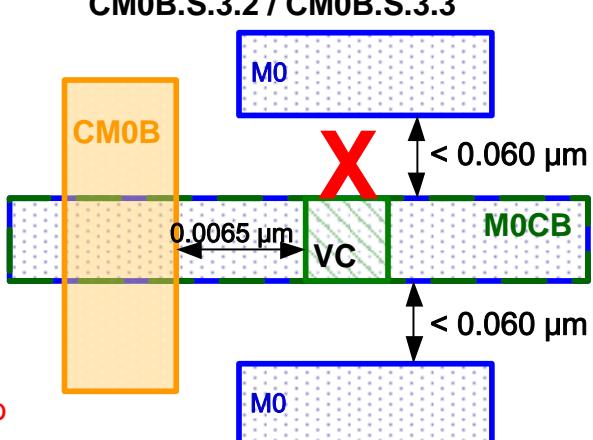




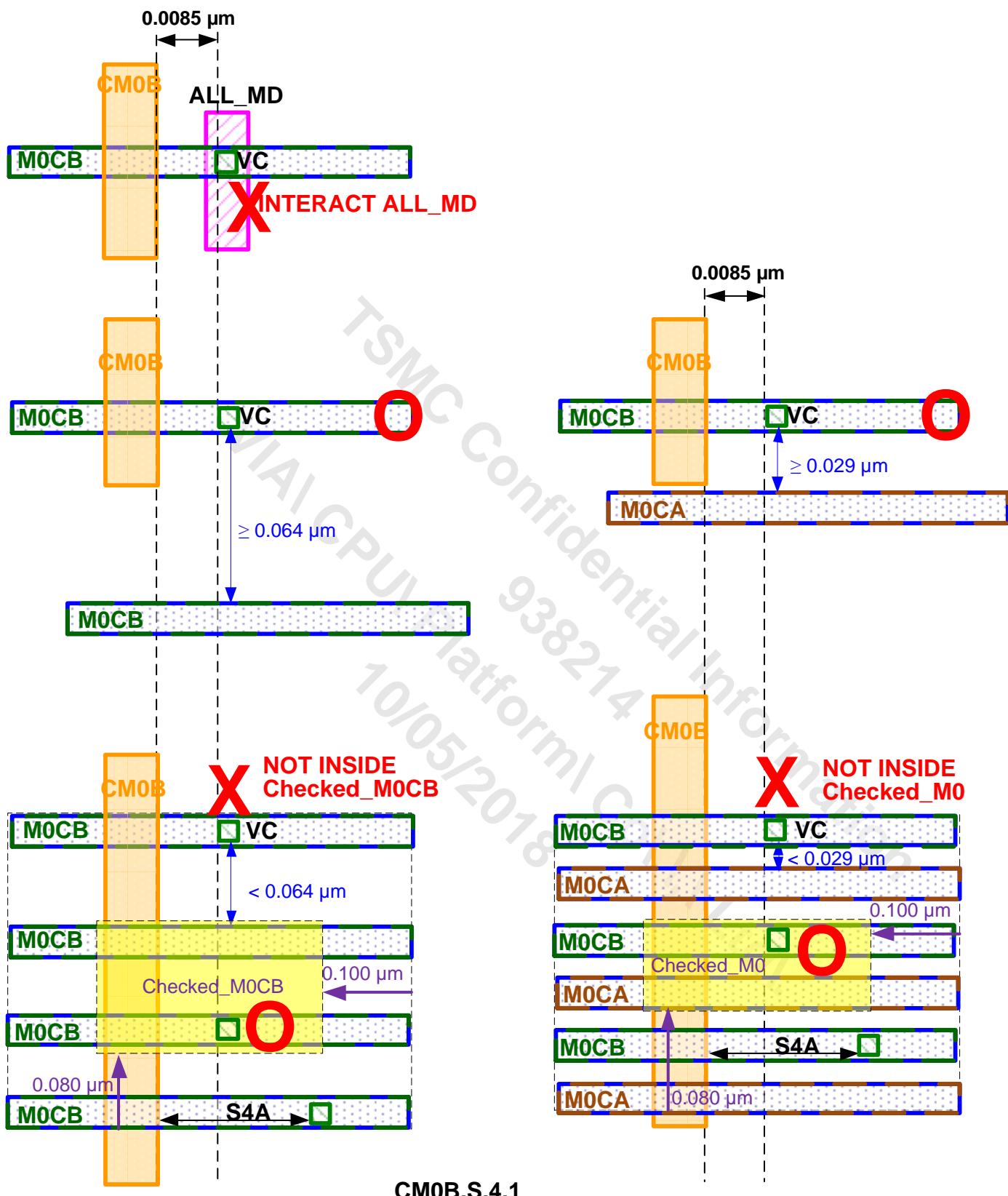


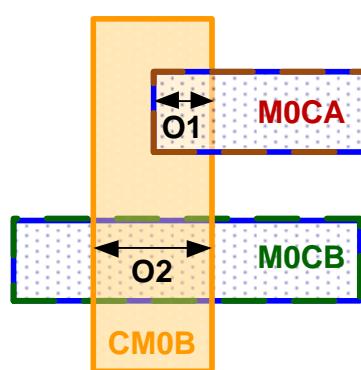
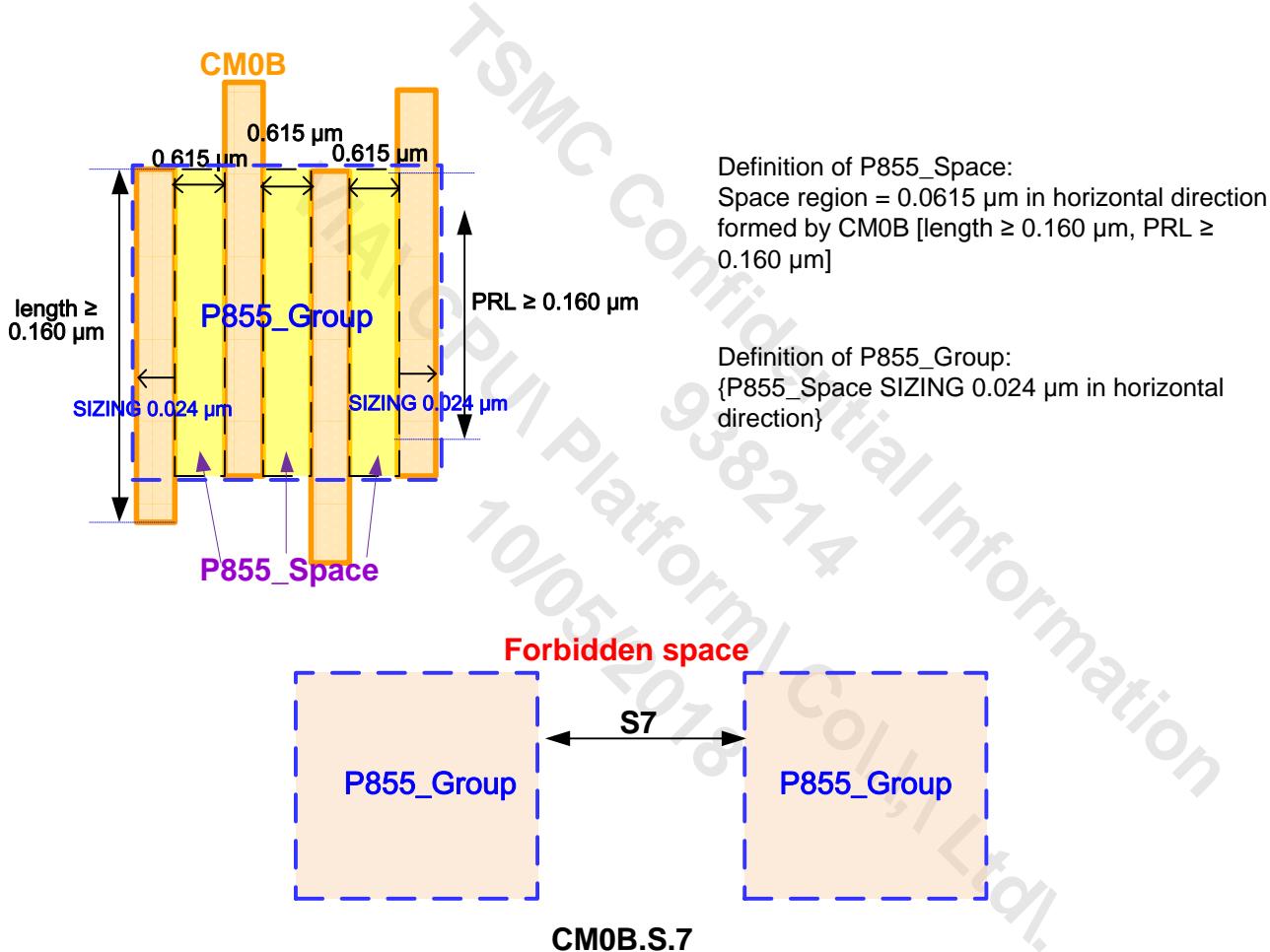
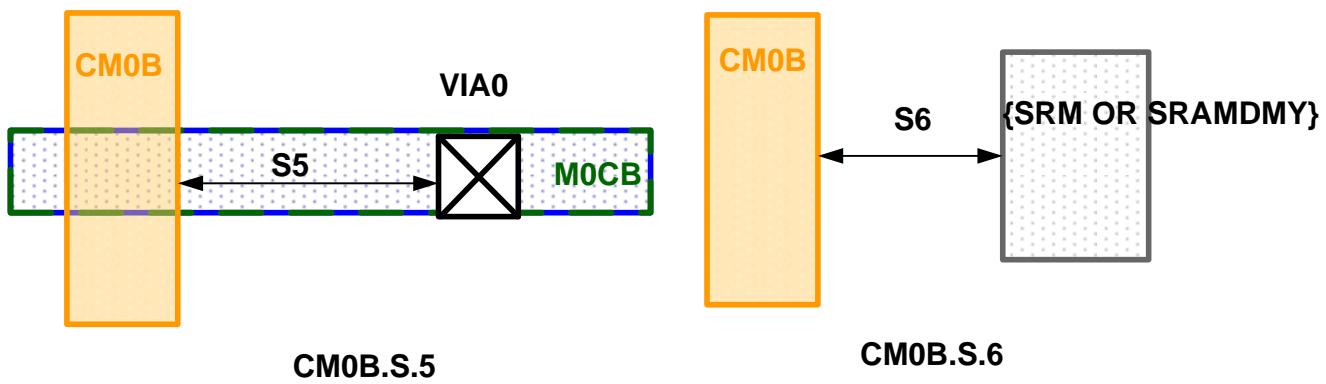
CM0B

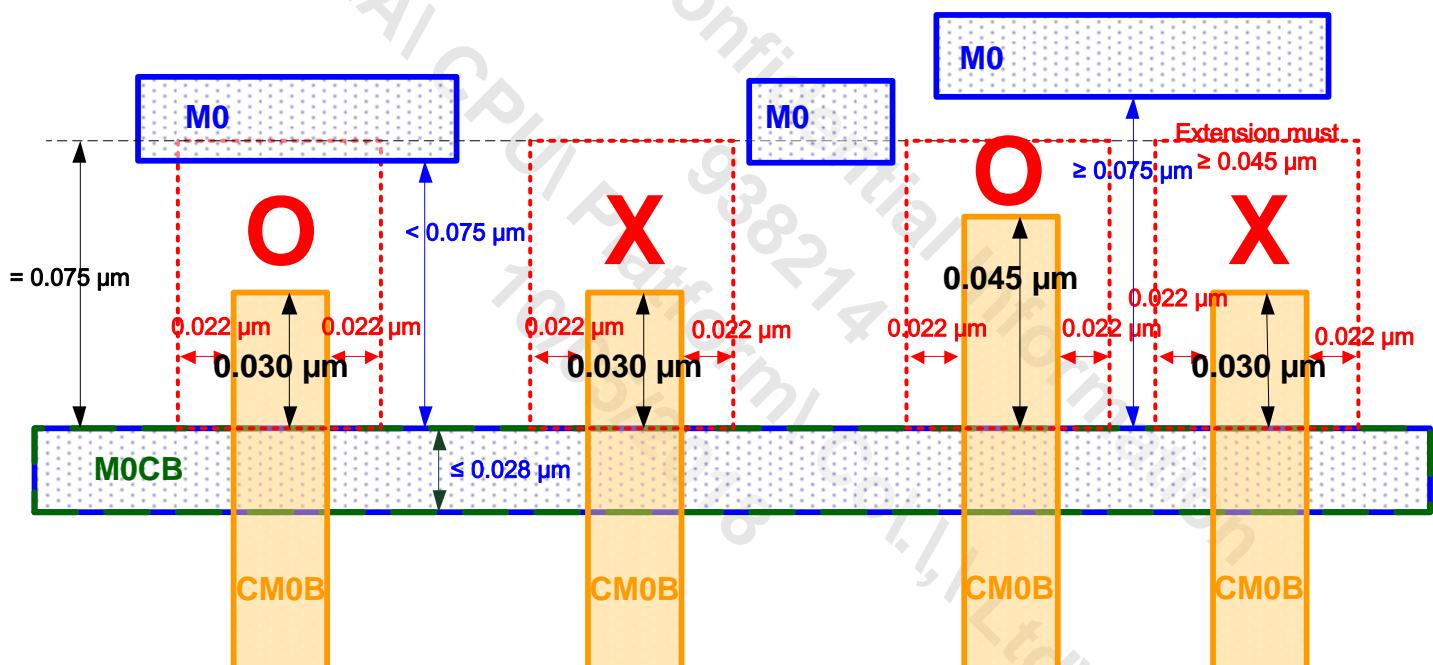
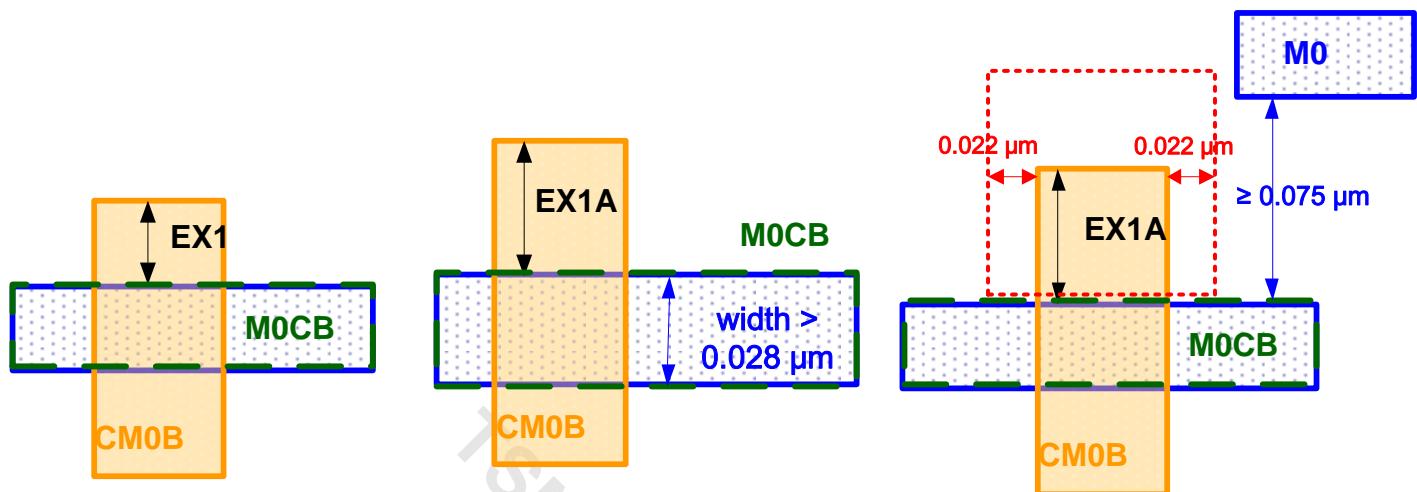
Except space of CM0B edge to VC $\geq 0.0065 \mu\text{m}$
[INSIDE M0CB, and M0CB either one side space to M0 $\geq 0.060 \mu\text{m}$ in MINP direction]



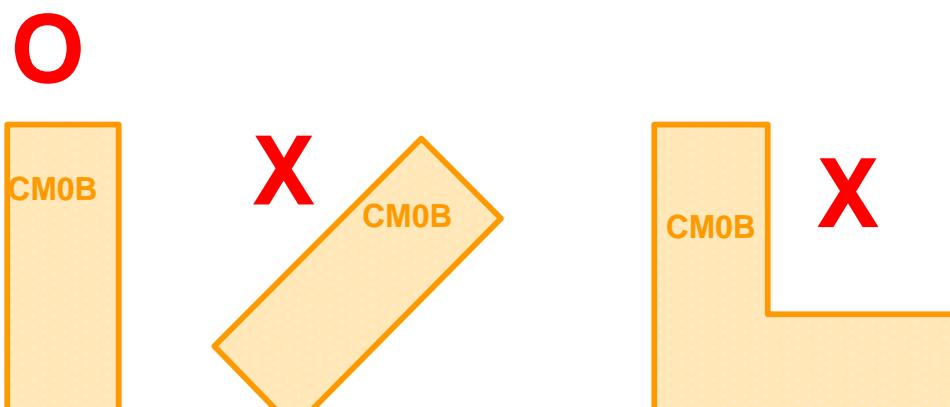
CM0B.S.4



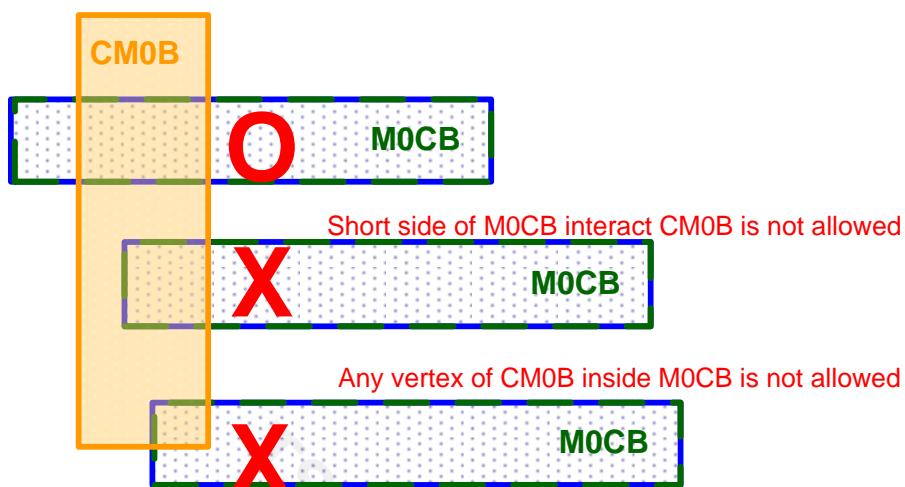




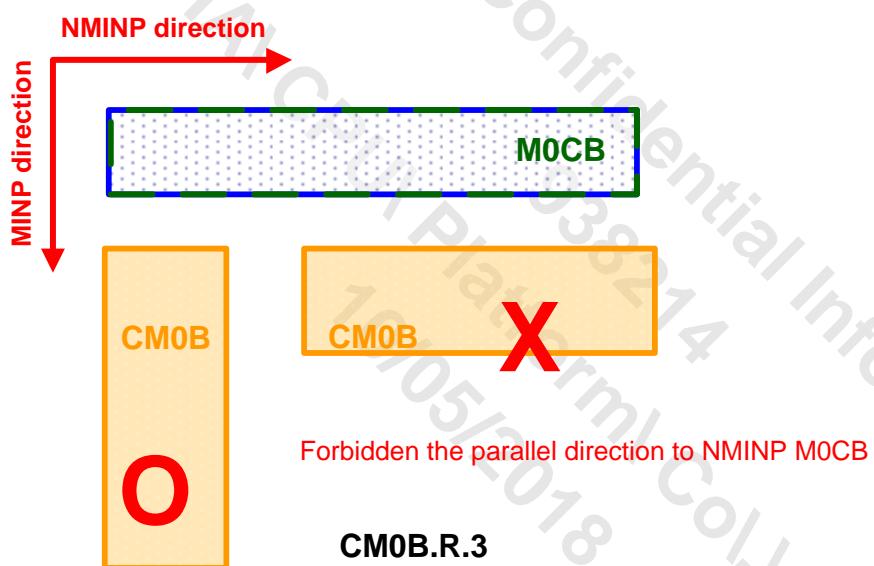
CM0B.EX.1 / CM0B.EX.1.1



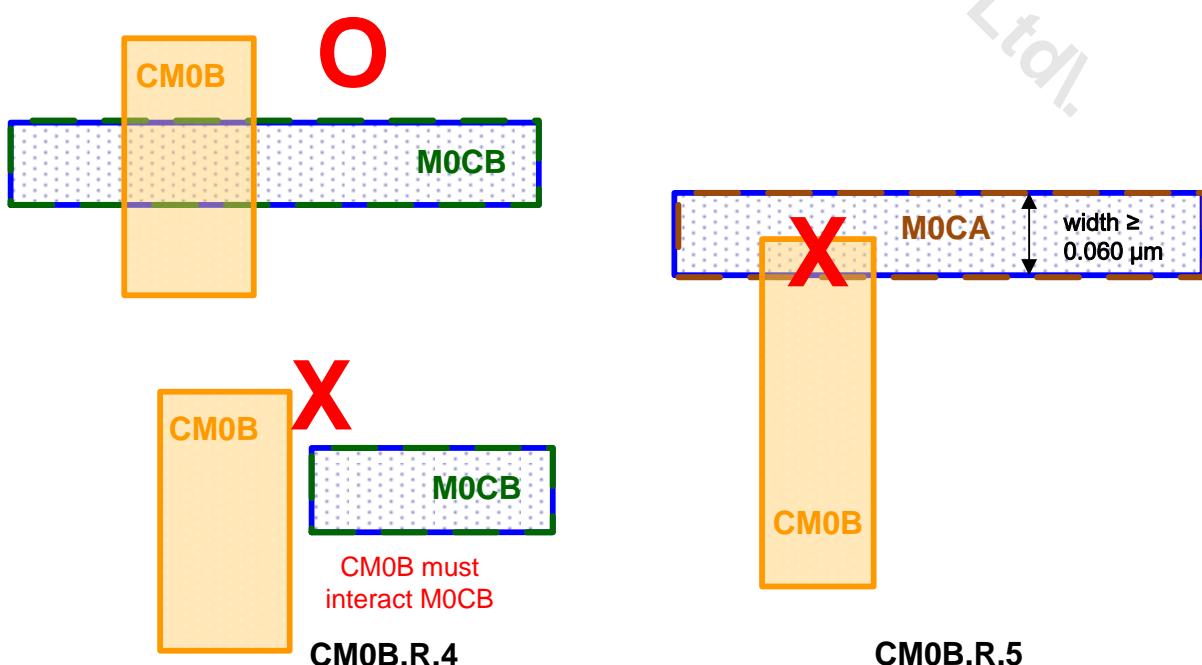
CM0B.R.1

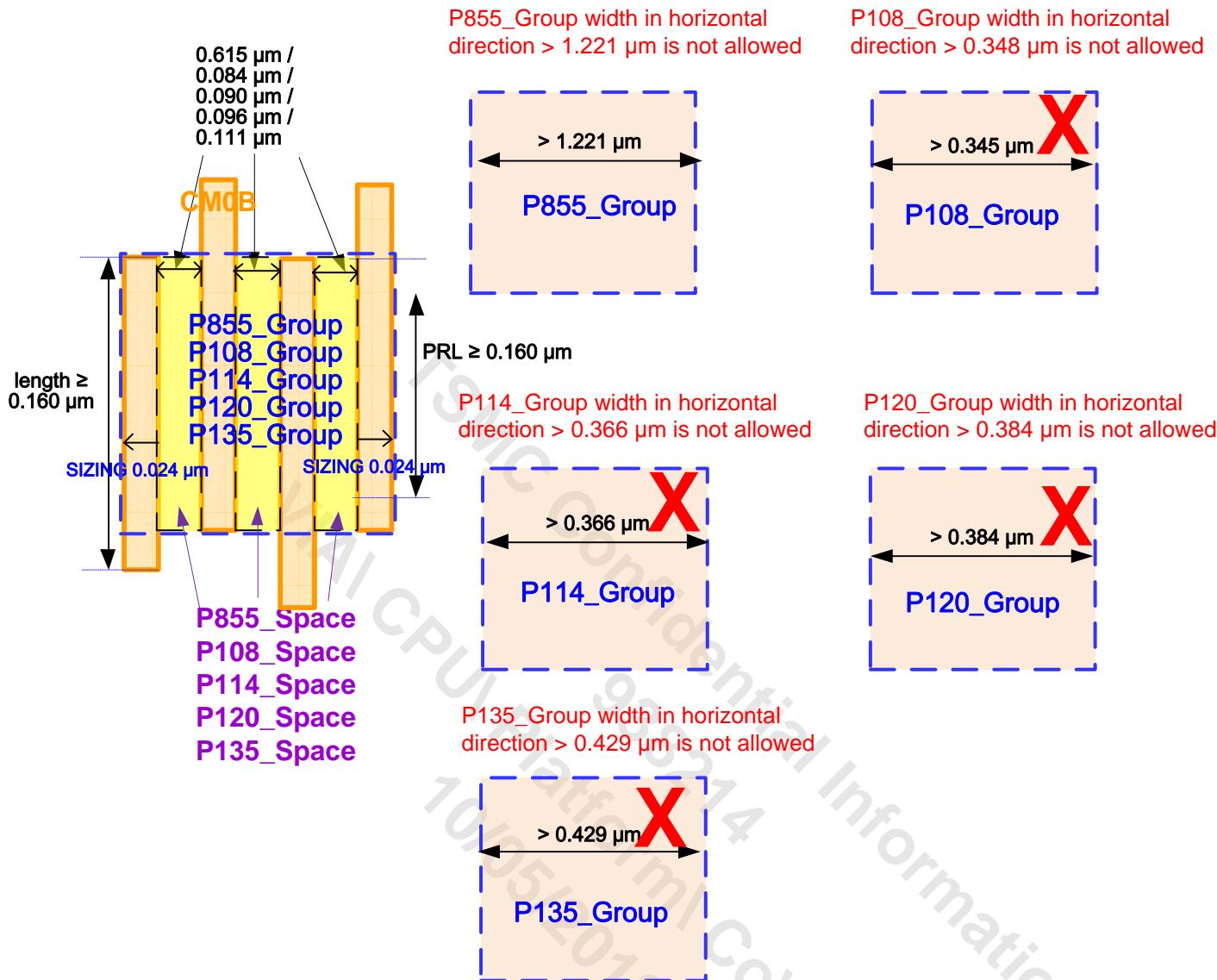


CM0B.R.2 / CM0B.R.6

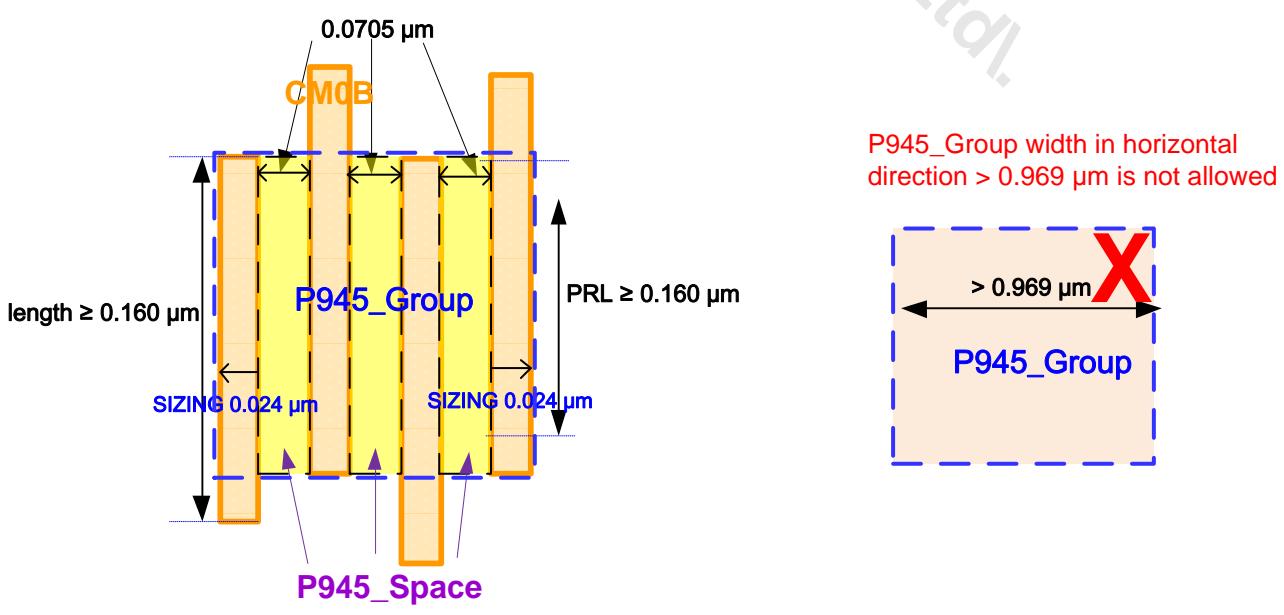


CM0B.R.3





CM0B.R.7.1 / CM0B.R.7.2 / CM0B.R.7.3 / CM0B.R.7.4 / CM0B.R.7.5



CM0B.R.7.1.1

4.5.41 Butted CM0 (BCM0) Layout Rules

BCM0VA (CAD Layer: 180;165) and BCM0VB (CAD Layer: 180;166) are tape-out layers, and they can be used to merge two CM0A or CM0B with space = 0.040/0.060/0.100 μm and PRL $\geq 0.019 \mu\text{m}$ at cell boundary, respectively.

BCM0H (CAD Layer: 180;161) is a tape-out layer, and it can be used as a block layer between CM0A or CM0B at cell boundary.

Two CM0A or CM0B interact the same BCM0H after cell placement will be transformed during mask making process in TSMC.

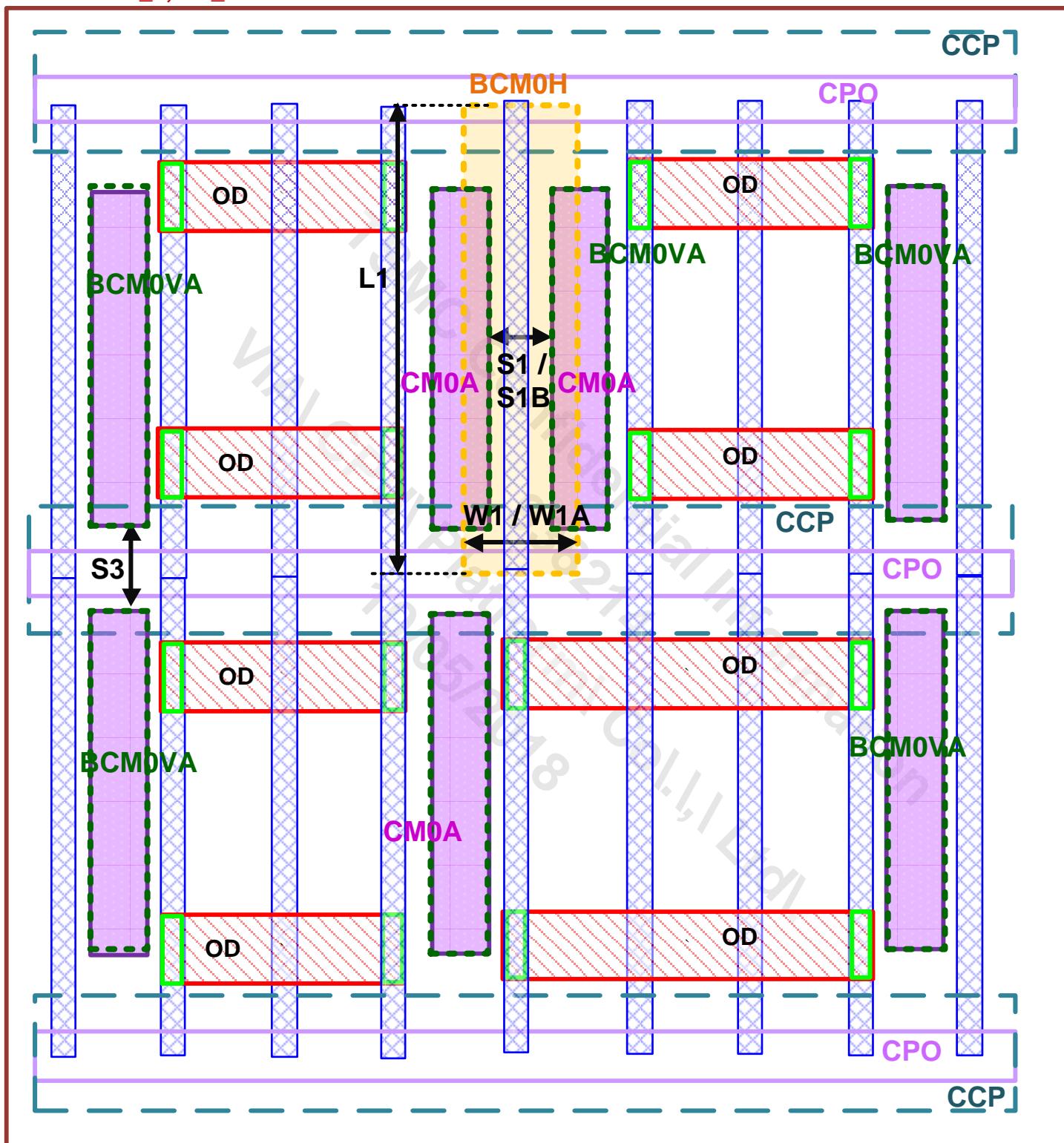
BCM0V = {BCM0VA OR BCM0VB}

CM0 = {CM0A OR CM0B}

Rule No.	Description	Label	Op.	Rule
BCM0.W.1	Width of BCM0H in horizontal direction (Except PO_P63)	W1	=	0.0570
BCM0.W.1.2	Width of BCM0H in horizontal direction [INSIDE PO_P63]	W1	=	0.0630
BCM0.S.1	Space of CM0A vertical edge [INSIDE BCM0H, PRL $\geq 0 \mu\text{m}$] (Except PO_P63)	S1	=	0.0330
BCM0.S.1.1	Space of CM0B vertical edge [INSIDE BCM0H, PRL $\geq 0 \mu\text{m}$] (Except PO_P63)	S1A	=	0.0330
BCM0.S.1.4	Space of CM0A vertical edge [INSIDE {BCM0H AND PO_P63}, PRL $\geq 0 \mu\text{m}$]	S1B	=	0.0390
BCM0.S.1.5	Space of CM0B vertical edge [INSIDE {BCM0H AND PO_P63}, PRL $\geq 0 \mu\text{m}$]	S1C	=	0.0390
BCM0.S.3	Space of CM0A [INTERACT BCM0VA] (Except BCM0H)	S3	\geq	0.0400
BCM0.S.3.1	Space of CM0B [INTERACT BCM0VB] (Except BCM0H)	S3A	\geq	0.0400
BCM0.L.1	Length of BCM0H	L1	\geq	0.2400
BCM0.R.1	BCM0H and BCM0V outside {FB_9 OR FB_8} is not allowed			
BCM0.R.2	BCM0H both vertical edges must abut centerline of CM0			
BCM0.R.3	BCM0H both horizontal edges must abut centerline of CCP_9, CCP_8			
BCM0.R.4	CM0A edge [INSIDE BCM0H] projection length difference (in vertical direction) must be 0 μm			
BCM0.R.4.1	CM0B edge [INSIDE BCM0H] projection length difference (in vertical direction) must be 0 μm			
BCM0.R.6	{CM0A [INTERACT BCM0H] SIZING up/down 0.0165 μm } overlap {VC OR VIA0} [INTERACT M0CA] is not allowed			
BCM0.R.6.1	{CM0B [INTERACT BCM0H] SIZING up/down 0.0165 μm } overlap {VC OR VIA0} [INTERACT M0CB] is not allowed			
BCM0.R.7	BCM0VA and CM0A [INTERACT {CCP_9 OR CCP_8}] must be drawn identically; BCM0VB and CM0B [INTERACT {CCP_9 OR CCP_8}] must be drawn identically (BCM0V overlap with CM0 [NOT INTERACT {CCP_9 OR CCP_8}] is not allowed)			
BCM0.R.8	BCM0H must be a rectangle orthogonal to grid			
BCM0.R.9	BCM0VA_Line-end_Region overlap M0CA is not allowed Definition of BCM0VA_Line-end_Region: { {BCM0VA SIZING up/down 0.034 μm in vertical direction} NOT BCM0VA }			
BCM0.R.9.1	BCM0VB_Line-end_Region overlap M0CB is not allowed Definition of BCM0VB_Line-end_Region: { {BCM0VB SIZING up/down 0.034 μm in vertical direction} NOT BCM0VB }			

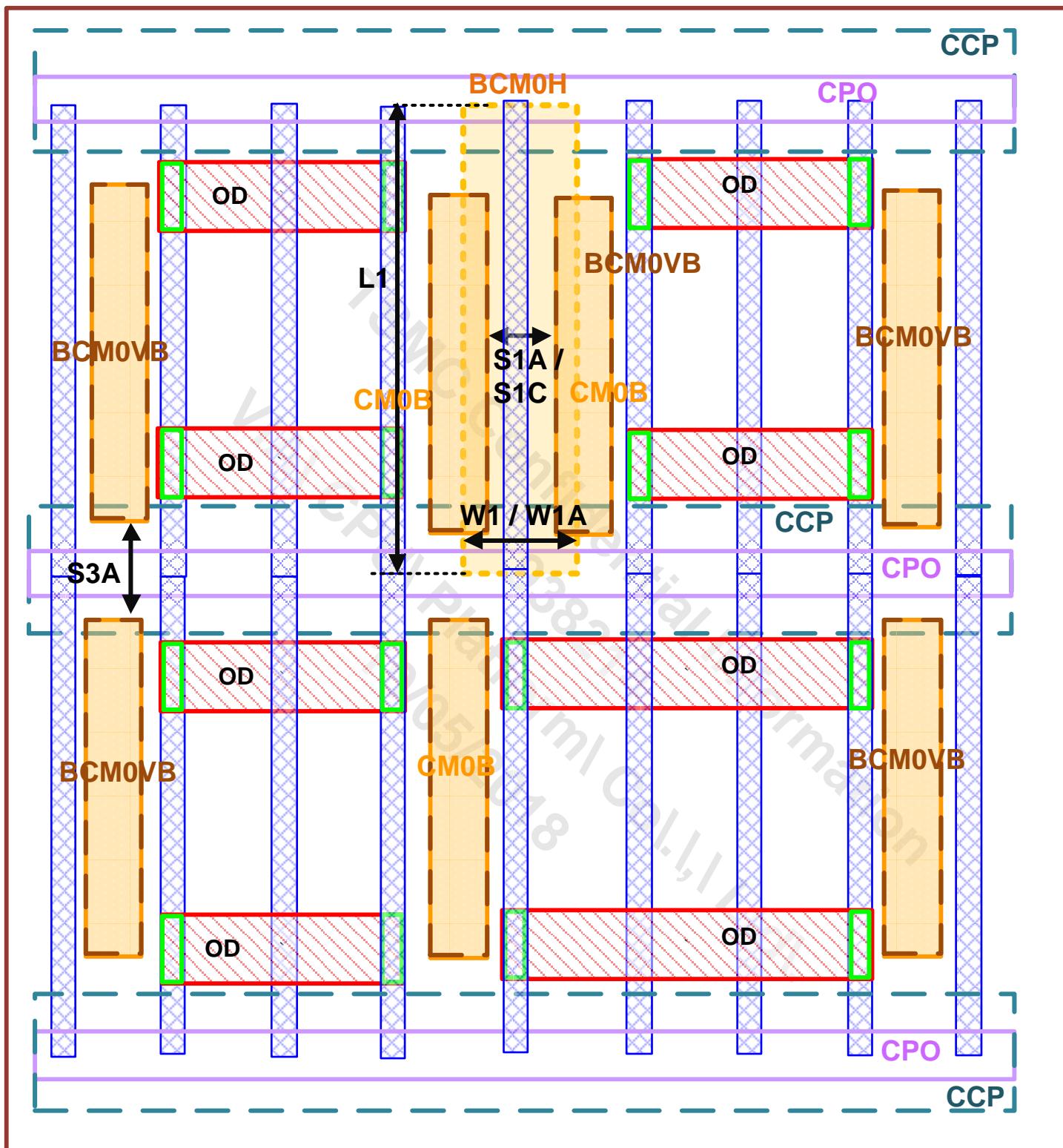
BCM0

FB_9, FB_8



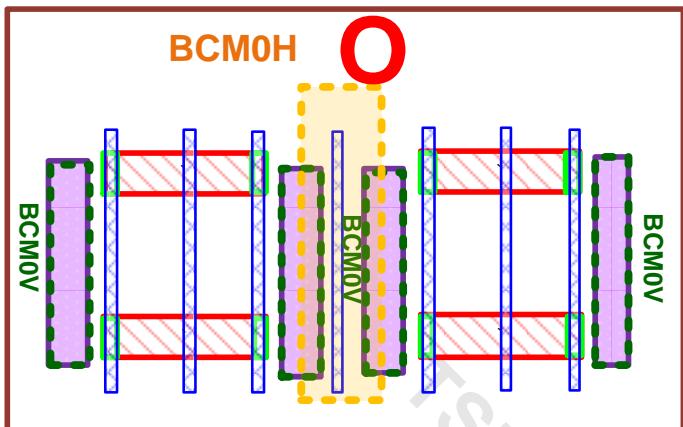
BCM0.W.1 / BCM0.W.1.1 / BCM0.W.1.2 /
BCM0.S.1 / BCM0.S.1.2 / BCM0.S.1.4 /
BCM0.S.3 / BCM0.L.1

FB_9, FB_8



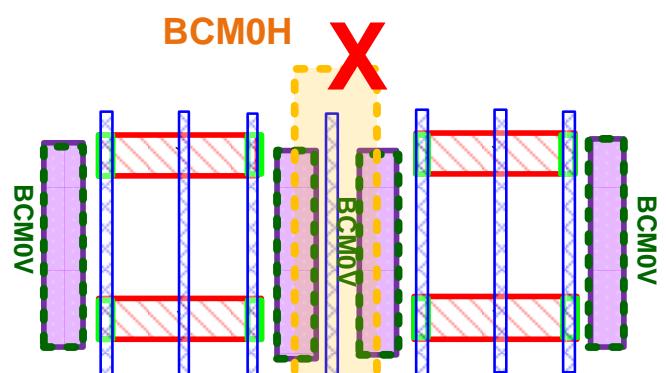
**BCM0.W.1 / BCM0.W.1.1 / BCM0.W.1.2 /
BCM0.S.1.1 / BCM0.S.1.3 / BCM0.S.1.5 /
BCM0.S.3.1 / BCM0.L.1**

FB_9, FB_8

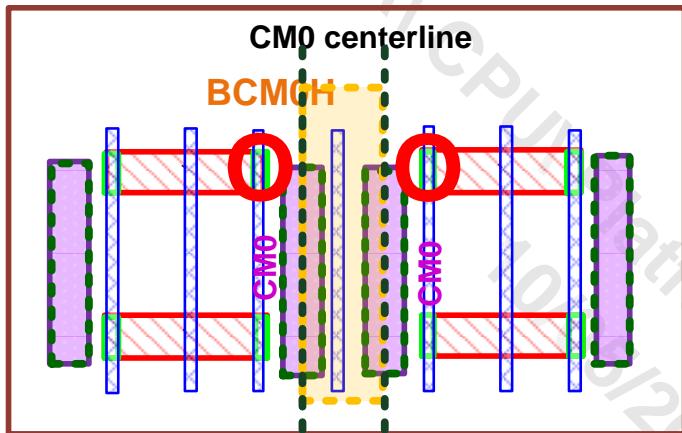


BCM0.R.1

Outside is not allowed

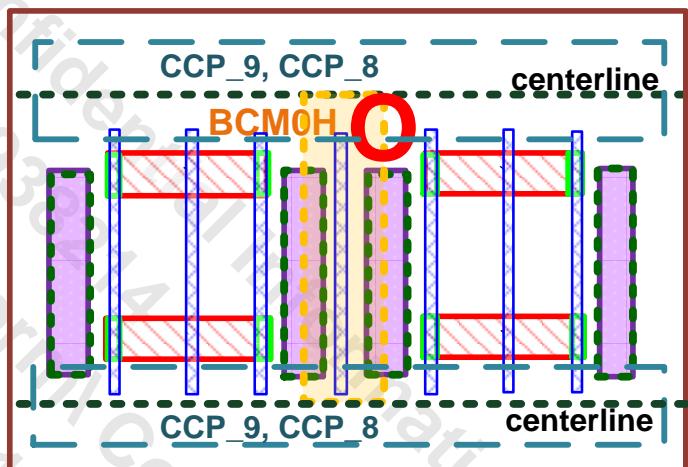


CM0 centerline



BCM0.R.2

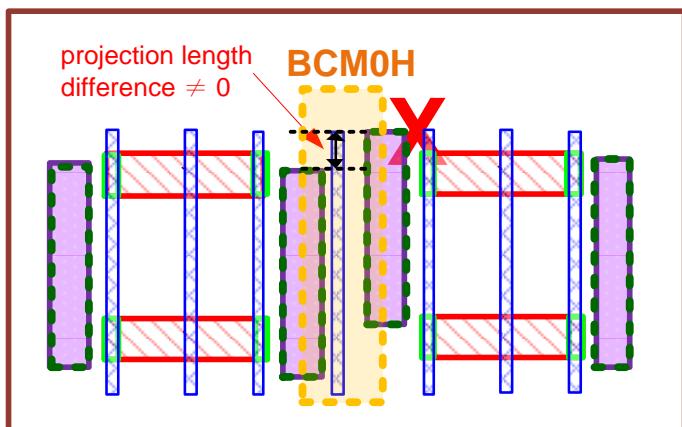
FB_9, FB_8



BCM0.R.3

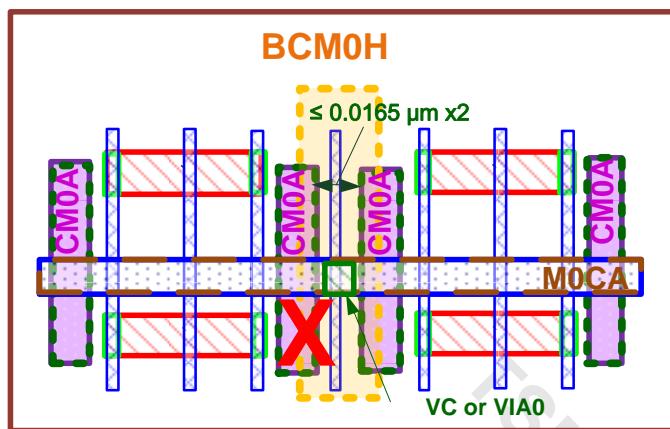
projection length difference $\neq 0$

BCM0H

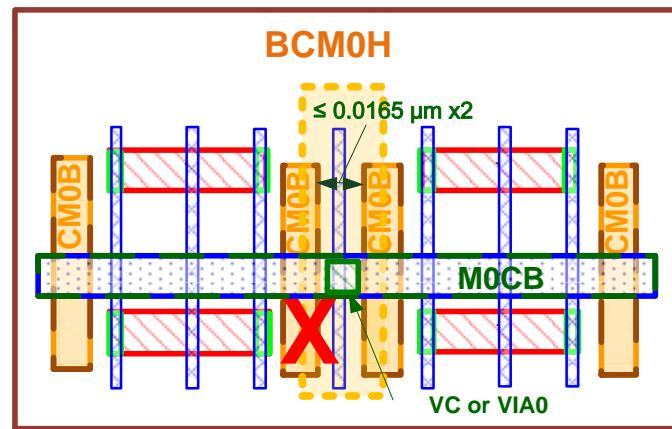


BCM0.R.4 / BCM0.R.4.1

FB_9, FB_8

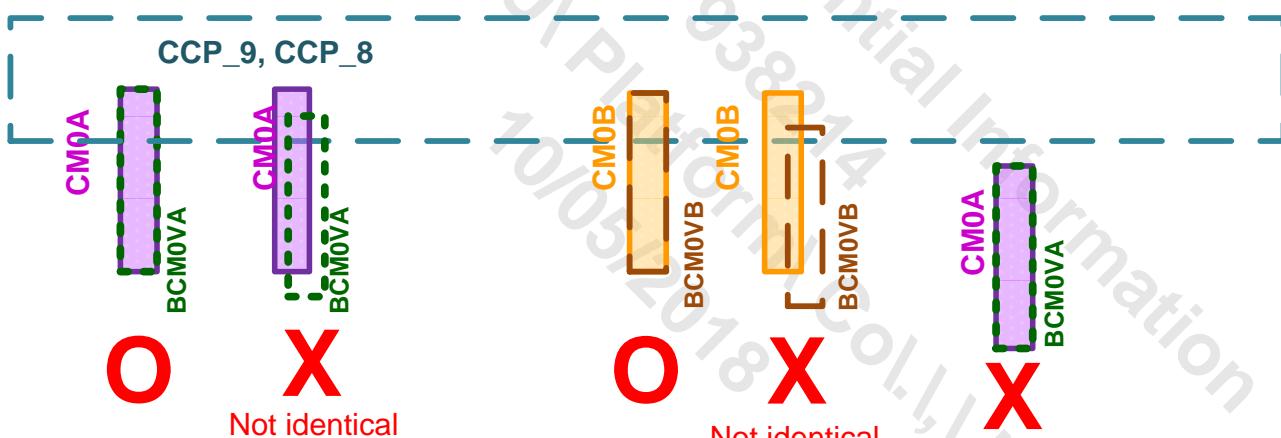


Overlap {VC OR VIA0} [INTERACT M0CA] is not allowed



Overlap {VC OR VIA0} [INTERACT M0CB] is not allowed

BCM0.R.6

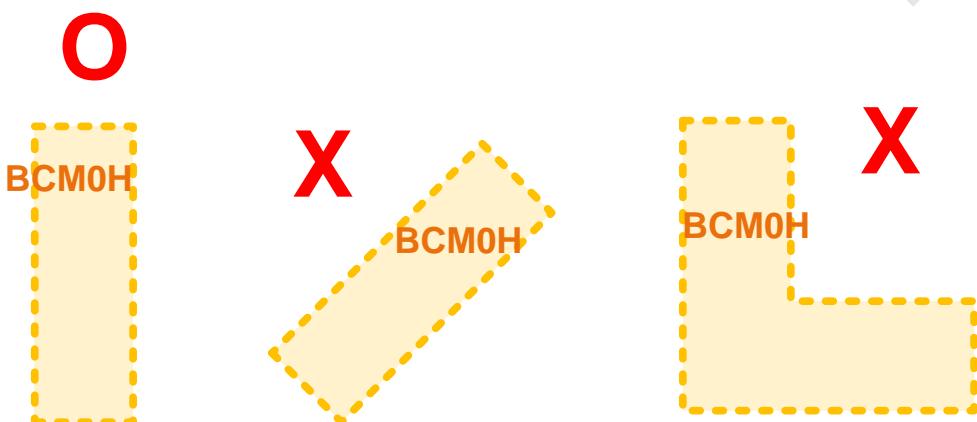


O X
Not identical

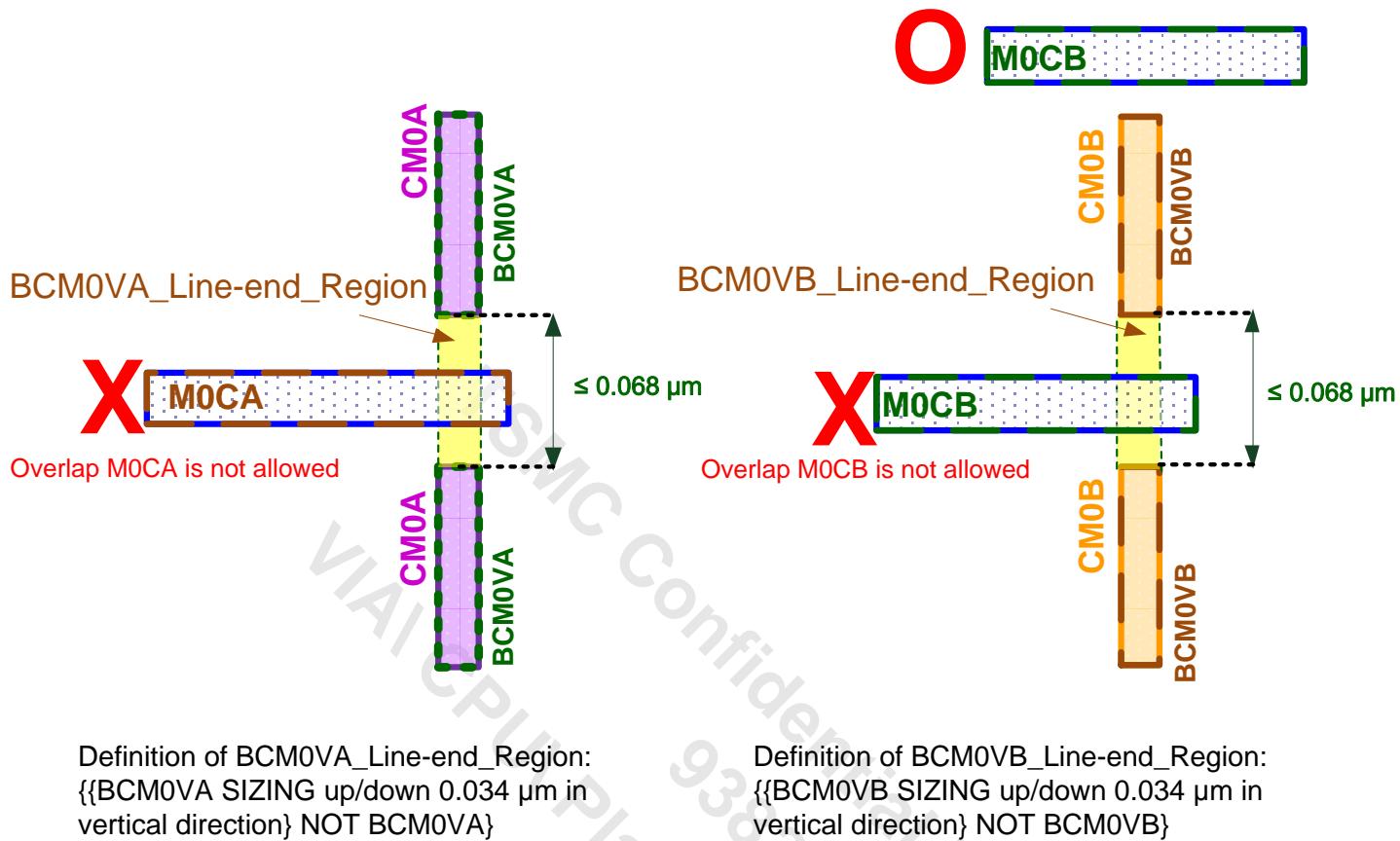
BCM0V overlap with CM0 [NOT INTERACT {CCP_9 OR CCP_8}] is not allowed

BCM0.R.6.1

O X
Not identical



BCM0.R.8



BCM0.R.9 / BCM0.R.9.1

4.5.42 VIA0 Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

VIA0xs (CAD layer: 159;420) is used for VIA0.

M0_NOT_CM0 = {{M0CA NOT CM0A} OR {M0CB NOT CM0B}}

Rule No.	Description	Label	Op.	Rule
VIA0.W.1	Width (Except SEALRING_ALL)	W1	=	0.0200
VIA0.W.2	Width of VIA0 bar in SEALRING_ALL	W2	=	0.1400
VIA0.S.1	Space (Except SEALRING_ALL)	S1	\geq	0.0265
VIA0.S.8	Space to VIA0 [maximum delta V > 0.96V]	S8	\geq	0.0620
VIA0.S.8.1	Space to VIA0 [maximum delta V > 1.32V] (1.2V + 10%)	S8	\geq	0.0640
VIA0.S.8.2	Space to VIA0 [maximum delta V > 1.65V] (1.5V + 10%)	S8	\geq	0.0700
VIA0.S.8.3	Space to VIA0 [maximum delta V > 1.98V] (1.8V + 10%)	S8	\geq	0.0820
VIA0.S.8.4	Space to VIA0 [maximum delta V > 2.75V] (2.5V + 10%)	S8	\geq	0.0870
VIA0.S.9	Space to {SRM (50;0) OR SRAMDMY (186;0)} ({VIA0 CUT {SRM (50;0) OR SRAMDMY (186;0)}} is not allowed)	S9	\geq	0.0840
VIA0.S.9.1	Space of short side of rectangular VIA0 to {SRM (50;0) OR SRAMDMY (186;0)} [PRL > -0.044 μ m]	S9A	\geq	0.1340
VIA0.S.11	Space of long side of rectangular VIA0 [PRL > 0 μ m (L1), with M1 width < 0.024 μ m in between] (Except BLK_WB)	S11	\geq	0.0680
VIA0.S.12	Space of Checked_VIA0 vertical edge [PRL > -0.020 μ m] Definition of Checked_VIA0: VIA0 space to {M1 OR M1_VIRT} \leq 0.022 μ m in M1 MINP direction [PRL > -0.080 μ m]	S12	\geq	0.0450
VIA0.S.31.1	Space of VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] in horizontal direction [different net, PRL > -0.020 μ m] (Except FB_9, FB_8, BLK_WB)	S31A	\geq	0.0440
VIA0.S.31.2	Space of VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] in vertical direction [different net, PRL > -0.018 μ m]	S31B	\geq	0.0440
VIA0.S.31.3.T	Space of VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 μ m in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μ m] (Except FB_9, FB_8)	S31CT	\geq	0.0740
VIA0.S.31.4.T	Space of VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 μ m in horizontal/vertical direction] in vertical direction [PRL > -0.020 μ m] (Except FB_9, FB_8)	S31DT	\geq	0.0490
VIA0.S.31.5.T	Space of VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 μ m in horizontal/vertical direction] (Except FB_9, FB_8)	S31ET	\geq	0.0490
VIA0.S.31.6.T	Space of VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 μ m in horizontal/vertical direction] in horizontal direction [PRL > -0.026 μ m]	S31FT	\geq	0.0370
VIA0.S.31.6.1.T	Space of VIA0 [edge length = 0.020/0.020 μ m in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 μ m in horizontal/vertical direction] in horizontal direction [PRL > -0.026 μ m] (Except FB_9, FB_8, BLK_WB)	S31FT	\geq	0.0490

Rule No.	Description	Label	Op.	Rule
VIA0.S.31.7.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S31GT	≥	0.0740
VIA0.S.31.8.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8, BLK_WB)	S31HT	≥	0.0490
VIA0.S.31.9.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S31IT	≥	0.0740
VIA0.S.31.10.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S31JT	≥	0.0490
VIA0.S.31.11.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S31KT	≥	0.0490
VIA0.S.31.12.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S31LT	≥	0.0490
VIA0.S.31.13.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S31MT	≥	0.0740
VIA0.S.31.14.T	Space of VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S31NT	≥	0.0490
VIA0.S.32.1.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32AT	≥	0.0740
VIA0.S.32.2.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32BT	≥	0.0490
VIA0.S.32.3.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32CT	≥	0.0490
VIA0.S.32.4.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32DT	≥	0.0740
VIA0.S.32.5.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32ET	≥	0.0490
VIA0.S.32.6.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32FT	≥	0.0490

Rule No.	Description	Label	Op.	Rule
VIA0.S.32.7.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32GT	≥	0.0740
VIA0.S.32.8.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32HT	≥	0.0740
VIA0.S.32.9.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32IT	≥	0.0490
VIA0.S.32.10.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32JT	≥	0.0740
VIA0.S.32.11.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32KT	≥	0.0490
VIA0.S.32.12.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32LT	≥	0.0490
VIA0.S.32.13.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32MT	≥	0.0740
VIA0.S.32.14.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32NT	≥	0.0740
VIA0.S.32.15.T	Space of VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32OT	≥	0.0490
VIA0.S.33.1.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm]	S33AT	≥	0.0370
VIA0.S.33.1.1.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8, BLK_WB)	S33AT	≥	0.0490
VIA0.S.33.2.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S33BT	≥	0.0740
VIA0.S.33.3.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8, BLK_WB)	S33CT	≥	0.0490
VIA0.S.33.4.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S33DT	≥	0.0740

Rule No.	Description	Label	Op.	Rule
VIA0.S.33.5.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S33ET	≥	0.0740
VIA0.S.33.6.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S33FT	≥	0.0490
VIA0.S.33.7.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except CCP_9, CCP_8, BLK_WB)	S33GT	≥	0.0490
VIA0.S.33.7.1	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [different net, PRL > -0.026 µm]	S33G1	≥	0.0440
VIA0.S.33.8.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S33HT	≥	0.0740
VIA0.S.33.9.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8, BLK_WB)	S33IT	≥	0.0490
VIA0.S.33.10.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S33JT	≥	0.0740
VIA0.S.33.11.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S33KT	≥	0.0740
VIA0.S.33.12.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S33LT	≥	0.0490
VIA0.S.33.13.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S33MT	≥	0.0490
VIA0.S.33.14.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S33NT	≥	0.0740
VIA0.S.33.15.T	Space of VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S33OT	≥	0.0490
VIA0.S.34.1.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34AT	≥	0.0740
VIA0.S.34.2.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34BT	≥	0.0490

Rule No.	Description	Label	Op.	Rule
VIA0.S.34.3.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34CT	≥	0.0490
VIA0.S.34.4.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34DT	≥	0.0740
VIA0.S.34.5.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34ET	≥	0.0490
VIA0.S.34.6.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34FT	≥	0.0490
VIA0.S.34.7.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34GT	≥	0.0740
VIA0.S.34.8.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34HT	≥	0.0740
VIA0.S.34.9.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34IT	≥	0.0490
VIA0.S.34.10.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34JT	≥	0.0740
VIA0.S.34.11.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34KT	≥	0.0490
VIA0.S.34.12.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34LT	≥	0.0490
VIA0.S.34.13.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34MT	≥	0.0740
VIA0.S.34.14.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34NT	≥	0.0740
VIA0.S.34.15.T	Space of VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34OT	≥	0.0490
VIA0.S.35.1.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S35AT	≥	0.0490

Rule No.	Description	Label	Op.	Rule
VIA0.S.35.2.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S35BT	≥	0.0740
VIA0.S.35.3.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S35CT	≥	0.0490
VIA0.S.35.4.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S35DT	≥	0.0740
VIA0.S.35.5.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S35ET	≥	0.0740
VIA0.S.35.6.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S35FT	≥	0.0490
VIA0.S.35.7.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S35GT	≥	0.0490
VIA0.S.35.8.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S35HT	≥	0.0740
VIA0.S.35.9.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S35IT	≥	0.0490
VIA0.S.35.10.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S35JT	≥	0.0740
VIA0.S.35.11.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S35KT	≥	0.0740
VIA0.S.35.12.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S35LT	≥	0.0490
VIA0.S.35.13.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except CCP_9, CCP_8, BLK_WB)	S35MT	≥	0.0490
VIA0.S.35.13.1	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [different net, PRL > -0.026 µm]	S35M1	≥	0.0440
VIA0.S.35.14.T	Space of VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S35NT	≥	0.0740

Rule No.	Description	Label	Op.	Rule
VIA0.S.35.15.T	Space of VIA0 [edge length = 0.020/0.050 μm in horizontal/vertical direction] to VIA0 [edge length = 0.020/0.050 μm in horizontal/vertical direction] (Except FB_9, FB_8, BLK_WB)	S35OT	≥	0.0490
VIA0.EN.0	1. Enclosure of square VIA0 [width = 0.020 μm] is defined by RuleTable.VIA0.EN.31 in the subsection 2. Enclosure of rectangular VIA0 [length = 0.050 μm] is defined by RuleTable.VIA0.EN.32 in the subsection 3. Enclosure of rectangular VIA0 [length = 0.034 μm] is defined by RuleTable.VIA0.EN.33 in the subsection 4. For enclosure of VIA0 by M0_NOT_CM0, refer to the "Cut-M0 (CM0) Layout Rules" section			
VIA0.EN.16.10	Checked_VIA0_Edge1 enclosure by M0 in M0 MINP direction (Except following conditions: 1. VIA0 inside BLK_M1) Definition of Checked_VIA0: VIA0 INTERACT M1 width > 0.040 μm Definition of Checked_VIA0_Edge1: 1. Checked_VIA0 edge space to {M0CA OR M0CB} < 0.040 μm with PRL > -0.100 μm in M0 MINP direction	EN16J	≥	0.0010
VIA0.EN.16.10.1	Checked_VIA0_Edge2 enclosure by M0 in M0 MINP direction (Except following conditions: 1. VIA0 inside BLK_M1) Definition of Checked_VIA0: VIA0 INTERACT M1 width > 0.040 μm Definition of Checked_VIA0_Edge2: 1. Checked_VIA0 edge space to {M0CA OR M0CB} < 0.040 μm with PRL > -0.100 μm in M0 MINP direction, and 2. Checked_VIA0 edge space to VC < 0.026 μm [PRL > 0, different net]	EN16J 1	≥	0.0020
VIA0.EN.18	Checked_VIA0_Edge1 enclosure by M0_NOT_CM0 in M0 NMINP direction Definition of Checked_VIA0: {VIA0 AND M0} INTERACT M1 width = 0.020 μm Definition of Checked_VIA0_Edge1: 1. Checked_VIA0 edge space to {M1 OR M1_VIRT} > 0.021 μm with PRL > -0.020 μm in M1 MINP direction	EN18	≥	0.0120
VIA0.EN.21.12	Short side enclosure of rectangular VIA0 by M0_NOT_CM0 edge [length = 0.080 μm, M0 width = 0.080 μm] (Except BLK_WB)	EN21	≥	0.0250
VIA0.EX.1	M0 extension on short side of VIA0 [width/length = 0.020/0.060 μm]	EX1	=	0.0000
VIA0.EX.1.1	M0 extension on long side of VIA0 [width/length = 0.020/0.060 μm]	EX1A	≥	0.0300
VIA0.O.1	VIA0 [width/length = 0.020/0.060 μm] overlap of M0 in VIA0 length direction	O1	=	0.0200
VIA0.O.1.1	VIA0 [width/length = 0.020/0.060 μm] overlap of M0 in VIA0 width direction	O1A	=	0.0200
VIA0.L.1	Length of VIA0 [width = 0.020 μm] (Except FB_9, FB_8)	L1	=	0.0200, 0.0340, 0.0500
VIA0.R.0	45-degree VIA0 is not allowed			

Rule No.	Description	Label	Op.	Rule
VIA0.R.2	Redundant via requirement must follow RuleTable.VIA0.R.2 of VIA0 numbers and space (S1) for M0 and M1 connection. [One of M0 or M1 has width and length (W1) > 0.160 μm]. (Except BLK_WB, or following conditions: 1. VIA bar)			
VIA0.R.2.1	Redundant via requirement must follow RuleTable.VIA0.R.2.1 of VIA0 numbers and space (S1) for M0 and M1 connection. [One of M0 or M1 has width and length (W1) > 0.300 μm] (Except BLK_WB, or following conditions: 1. VIA bar)			
VIA0.R.3	Redundant via requirement must follow RuleTable.VIA0.R.3 of VIA0 numbers and space (S1) for M0 and M1 connection. [One of M0 or M1 has width and length (W1) > 0.412 μm]. (Except BLK_WB, or following conditions: 1. VIA bar)			
VIA0.R.4	VIA0 [width/length = 0.020/0.060 μm] must be vertical direction			
VIA0.R.4.1	Space of vertical edge of Checked_VIA0 to {M1 OR M1_VIRT} in M1 MINP direction [PRL > 0 μm] > 0.022 μm is not allowed Definition of Checked_VIA0: Bridge_VIA0 with edge space to {M1 OR M1_VIRT} < 0.056 μm with PRL > -0.120 μm in M1 MINP direction Definition of Bridge_VIA0: VIA0 [edge length = 0.020/0.060 μm in horizontal/vertical direction] INTERACT M1 width < 0.034 μm			
VIA0.R.6	VIA0 overlap {CM0A AND M0CA}, {CM0B AND M0CB} is not allowed			
VIA0.R.7	VIA0 must be fully covered by {M0_NOT_CM0 AND M1} (Except following conditions: 1. VIA0 [width/length = 0.020/0.060 μm])			
VIA0.R.7.1	VIA0 [width/length = 0.020/0.060 μm] must be inside M1 [width \leq 0.037 μm]			
VIA0.R.7.2	VIA0 [width/length = 0.020/0.060 μm] both short side must abut M0 [width = 0.020 μm] from inside			
VIA0.R.10	Overlap MetalFuse_B1 (156;8) is not allowed			
VIA0.R.13	Maximum area ratio of M0 to upper VIA0 in the same net [connects to gate with area > 10700 μm^2 , and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	350000
VIA0.R.13.2	Maximum area ratio of I/O gate to single layer VIA0 in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area \geq 0.25 μm^2) Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	300000
VIA0.R.19	Isolated VIA0 is not allowed. (Except SEALRING_ALL) DRC flags VIA0 without neighboring {VIA0 OR DVIA0} distance \leq 4 μm			

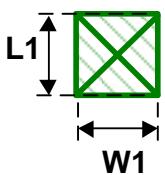
Rule No.	Description	Label	Op.	Rule
VIA0.R.21	VIA0 interact VIA0_Empty_Space_100 is not allowed in chip level (Except following conditions: 1. INDDMY, SEALRING_ALL for VIA0_Empty_Space_100) Definition of VIA0_Empty_Space_100: {{CHIP NOT {VIA0 OR DVIA0}} SIZING down/up 50 μm}			
VIA0.R.21.1	VIA0 interact VIA0_Empty_Space_50 is not allowed in cell level (Except following conditions: 1. INDDMY for VIA0_Empty_Space_50) Definition of VIA0_Empty_Space_50: {{CHIP NOT {VIA0 OR DVIA0}} SIZING down/up 25 μm}			
VIA0.R.22	VIA0 space to 4 or more VIA0 < 0.030 μm is not allowed			

Table Notes:

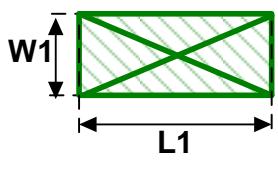
- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

VIA0

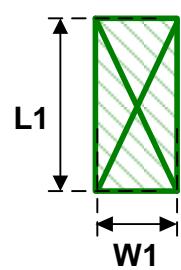
square VIA0



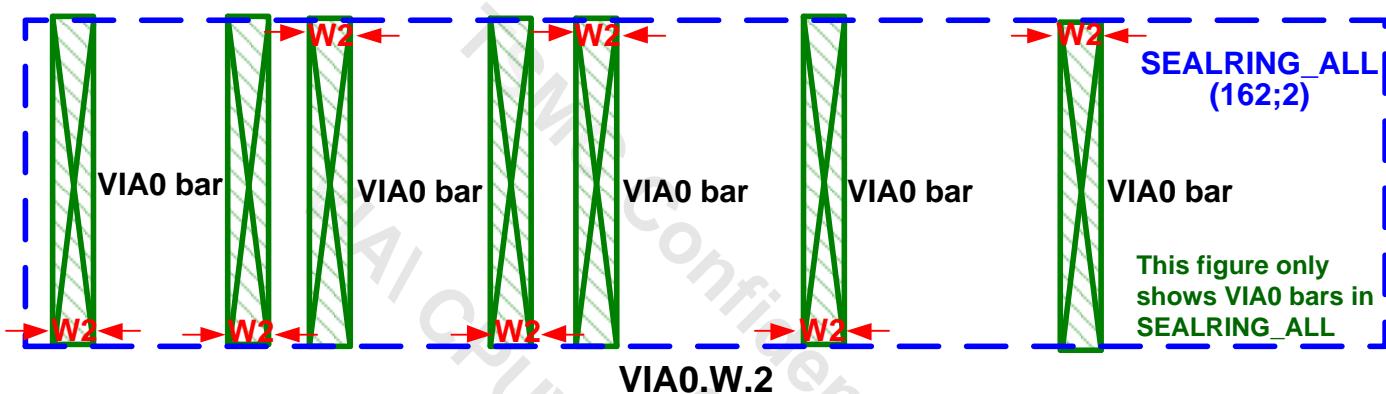
rectangular VIA0



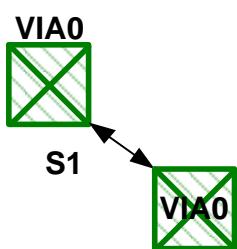
rectangular VIA0



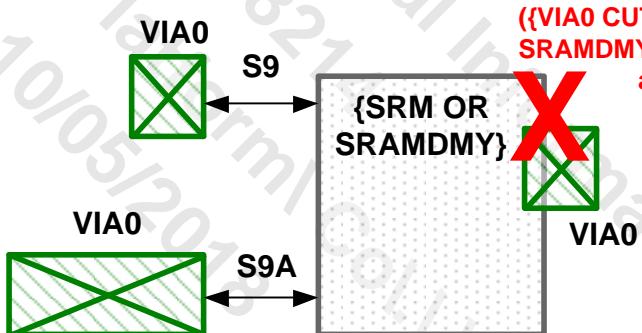
VIA0.W.1 / VIA0.L.1



VIA0.W.2

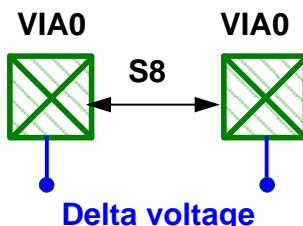


VIA0.S.1

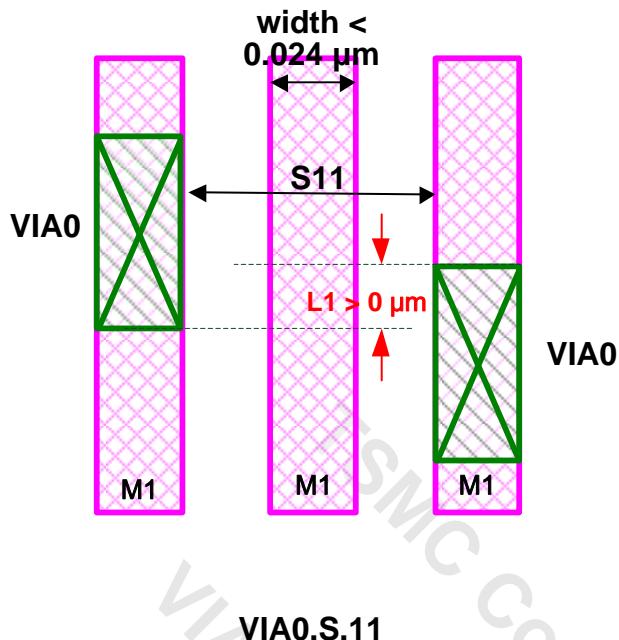


((VIA0 CUT {SRM (50;0) OR SRAMDMY;0 (186;0)} is not allowed)

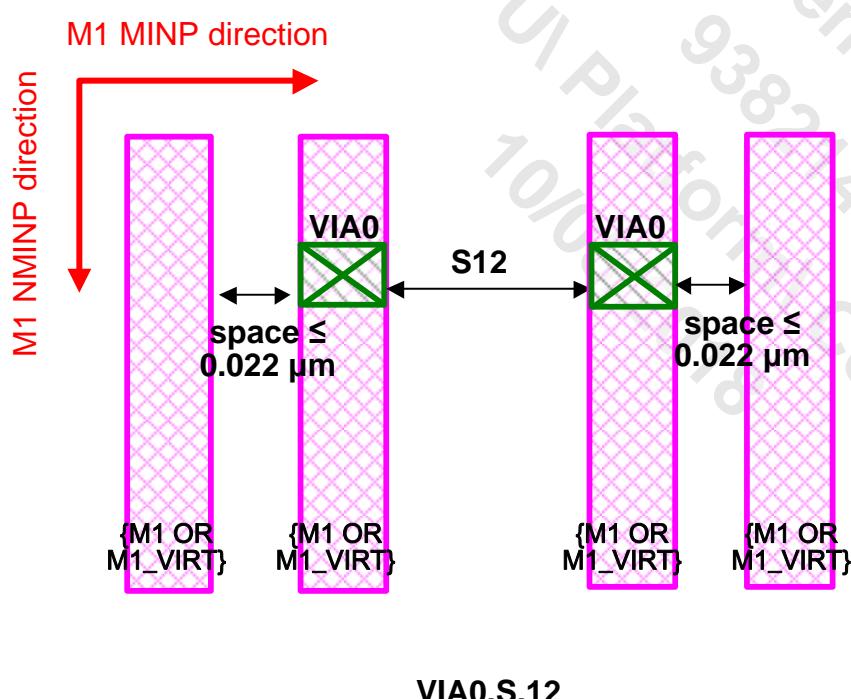
VIA0.S.9 / VIA0.S.9.1



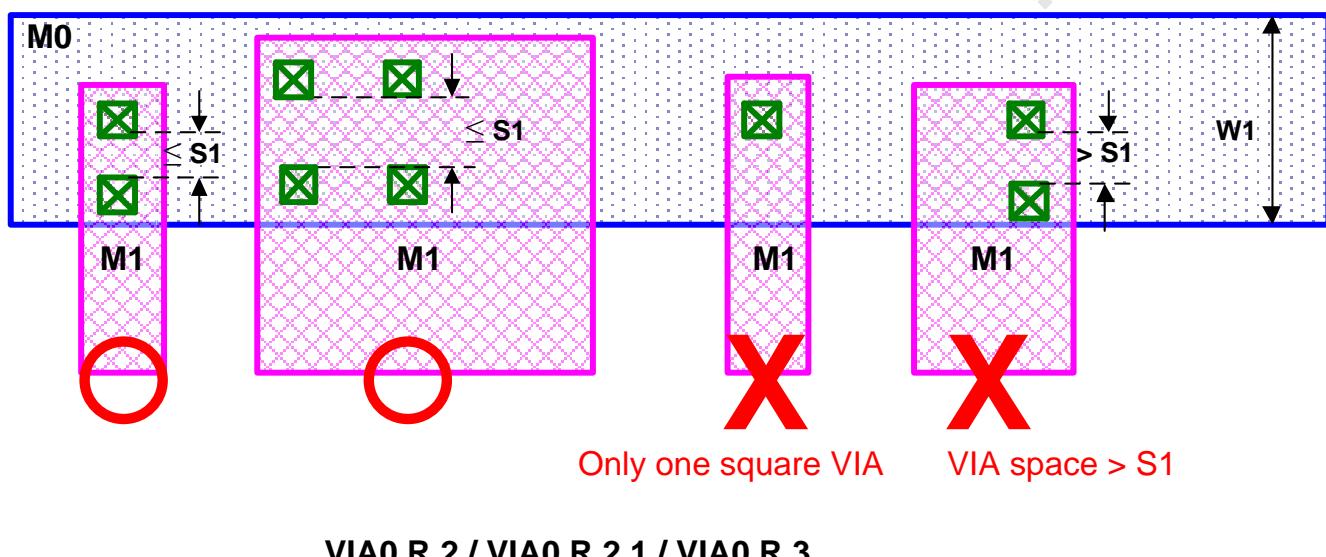
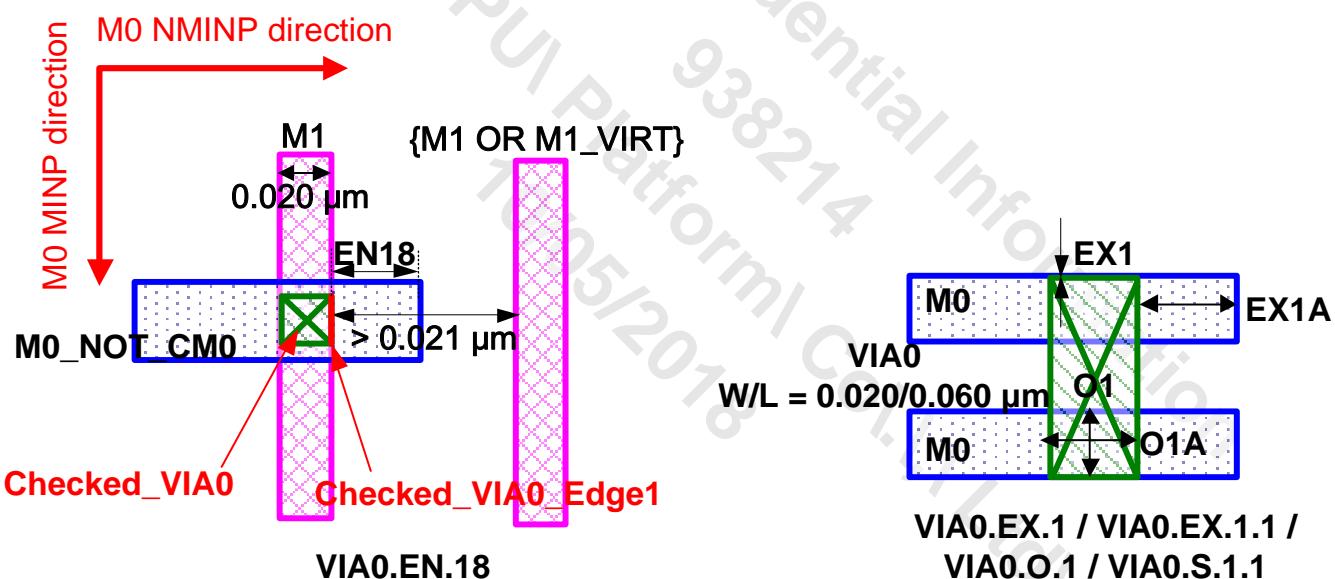
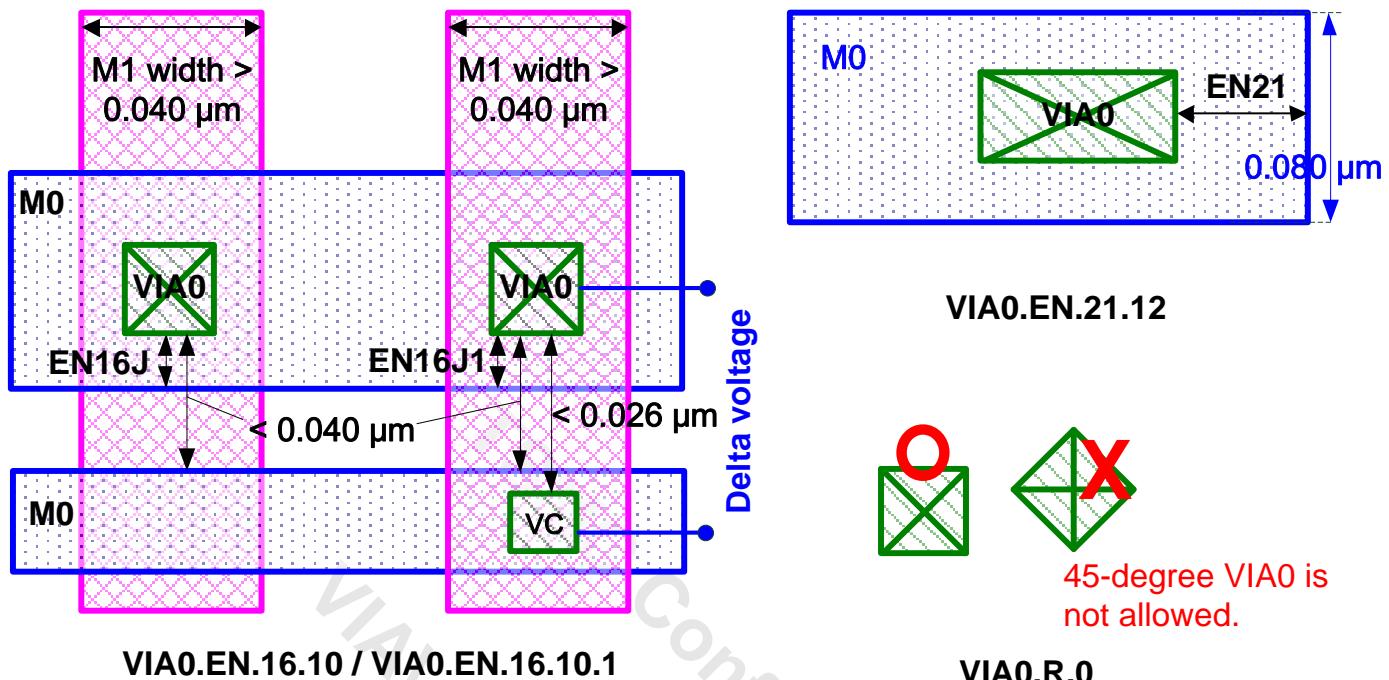
VIA0.S.8 / VIA0.S.8.1 /
VIA0.S.8.2 / VIA0.S.8.3 /
VIA0.S.8.4



VIA0.S.11



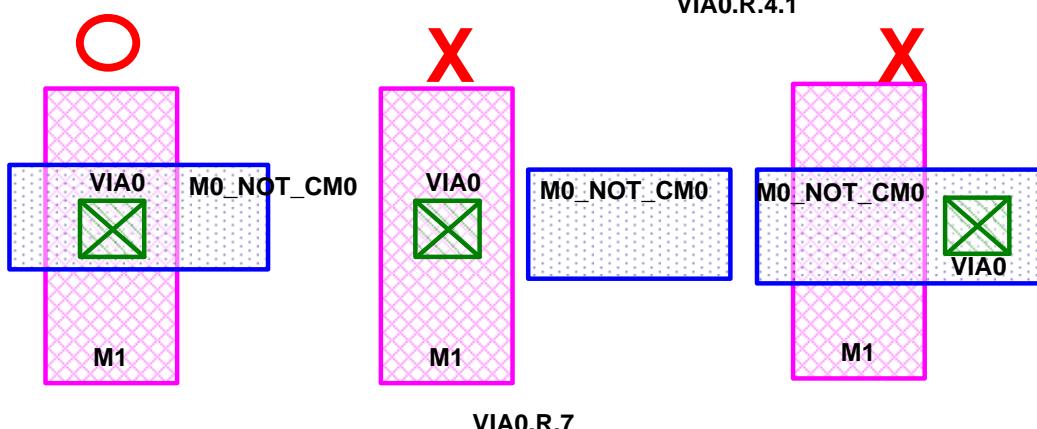
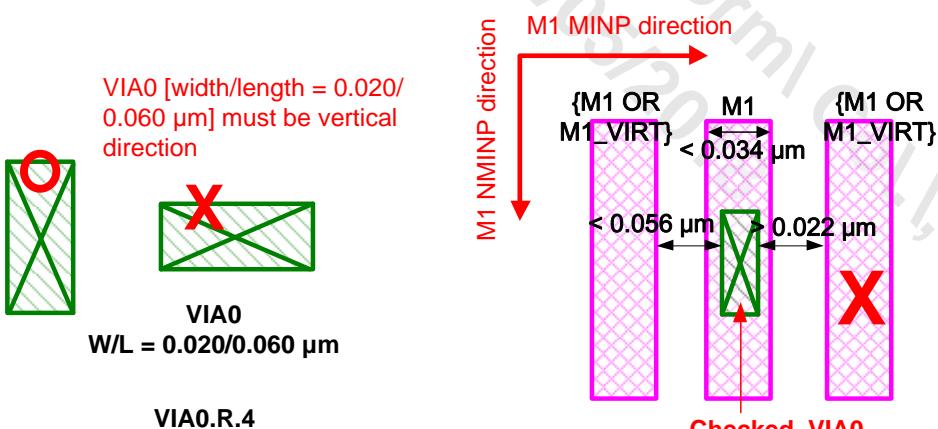
VIA0.S.12

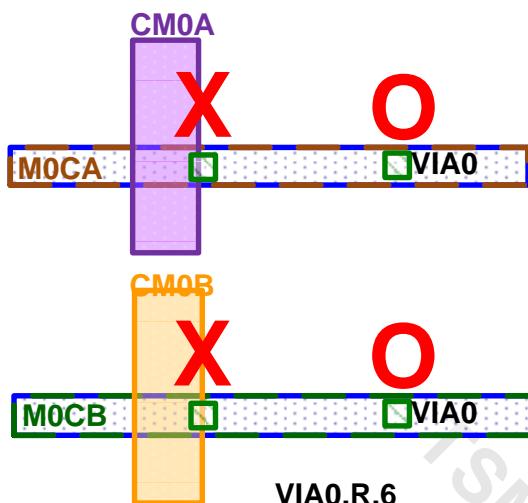


RuleTable.VIA0.R.2	$0.160 \mu\text{m} < W1 \leq 0.300 \mu\text{m}$							
VIA0 space (S1) (μm)	$0.070 \leq S1 \leq 0.160$				$0.160 < S1 \leq 0.400$			
Rectangular VIA0 [width/length = 0.020/0.050 μm] (#)	0	1			0	1	2	
{Square VIA0 [width = 0.020 μm] OR rectangular VIA0 [width/length = 0.020/0.034 μm] (#)}	≥ 2	≥ 0			≥ 4	≥ 2	≥ 0	

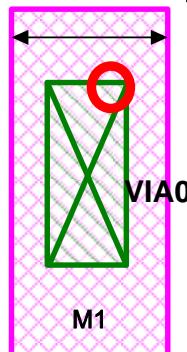
RuleTable.VIA0.R.2.1	$0.300 \mu\text{m} < W1 \leq 0.412 \mu\text{m}$							
VIA0 space (S1) (μm)	$0.070 \leq S1 \leq 0.160$				$0.160 < S1 \leq 0.400$			
Rectangular VIA0 [width/length = 0.020/0.050 μm] (#)	0	1	2		0	1	2	3
{Square VIA0 [width = 0.020 μm] OR rectangular VIA0 [width/length = 0.020/0.034 μm] (#)}	≥ 3	≥ 1	≥ 0		≥ 6	≥ 4	≥ 2	≥ 0

RuleTable.VIA0.R.3	W1 > 0.412 μm									
VIA0 space (S1) (μm)	$0.070 \leq S1 \leq 0.160$				$0.160 < S1 \leq 0.400$					
Rectangular VIA0 [width/length = 0.020/0.050 μm] (#)	0	1	2		0	1	2	3	4	5
{Square VIA0 [width = 0.020 μm] OR rectangular VIA0 [width/length = 0.020/0.034 μm] (#)}	≥ 4	≥ 2	≥ 0		≥ 9	≥ 7	≥ 5	≥ 3	≥ 1	≥ 0

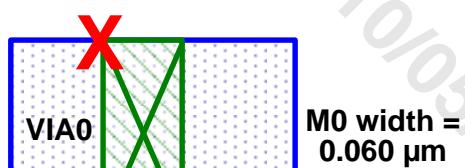
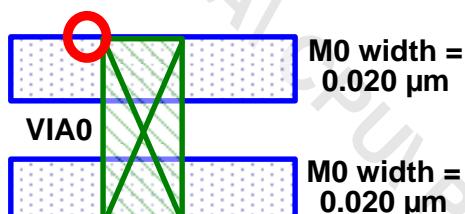




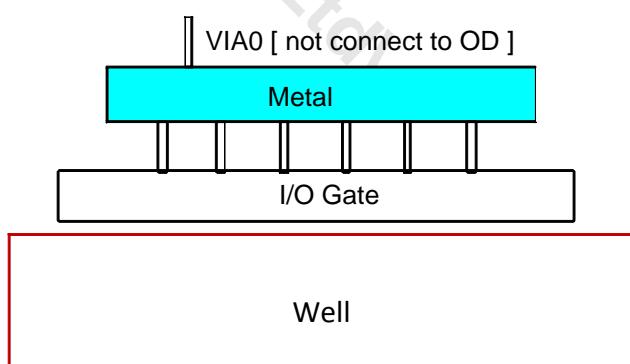
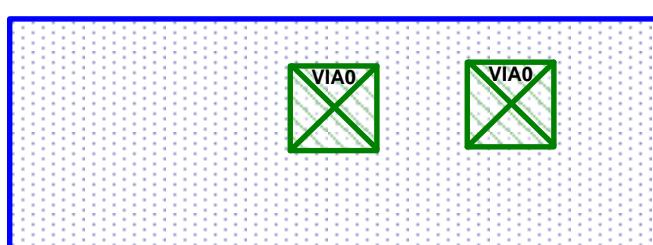
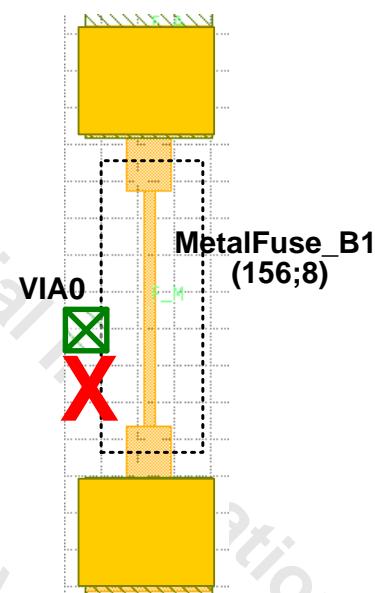
M1 width $\leq 0.037 \mu\text{m}$ M1 width $> 0.037 \mu\text{m}$



VIA0.R.7.1



VIA0.R.7.2

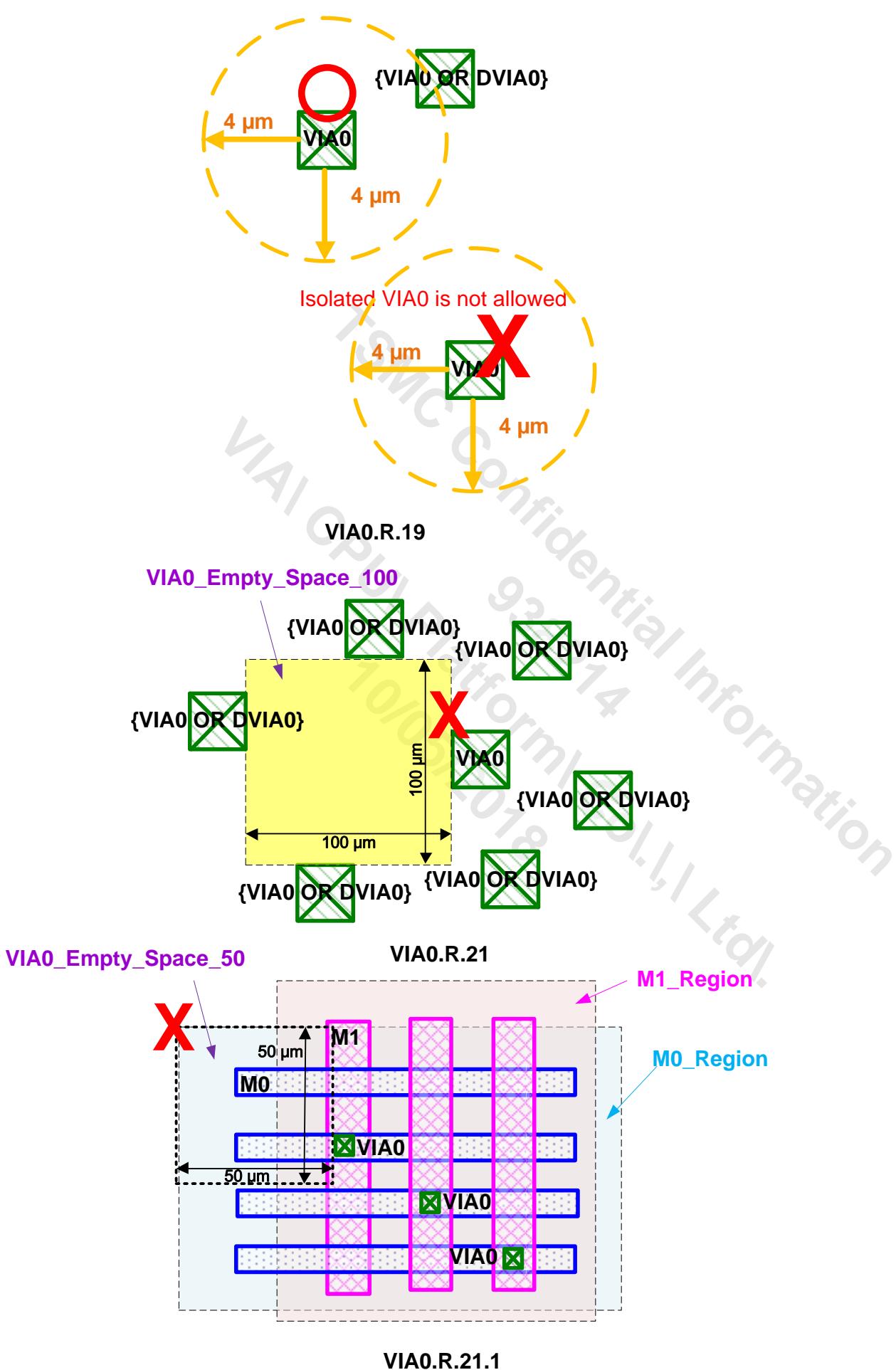


$$\frac{\text{I/O Gate Area}}{\text{VIA0 Area}} \leq 300000$$

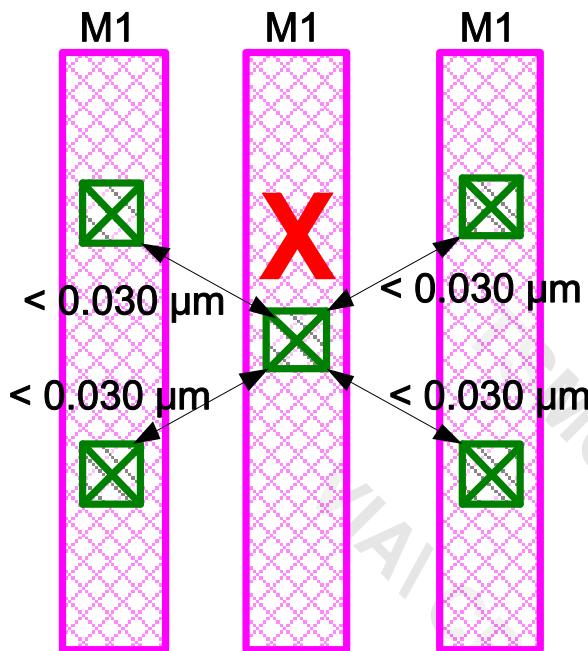
$$\frac{\text{M0/M1 Area}}{\text{VIA0 Area}} \leq 350000$$

VIA0.R.13

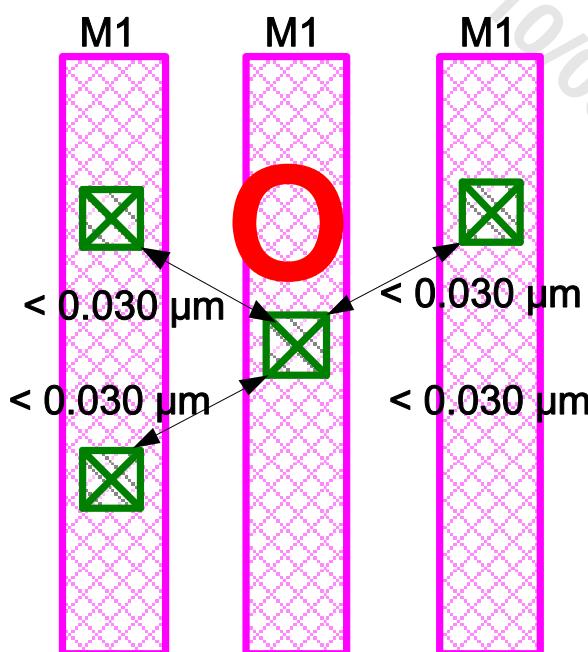
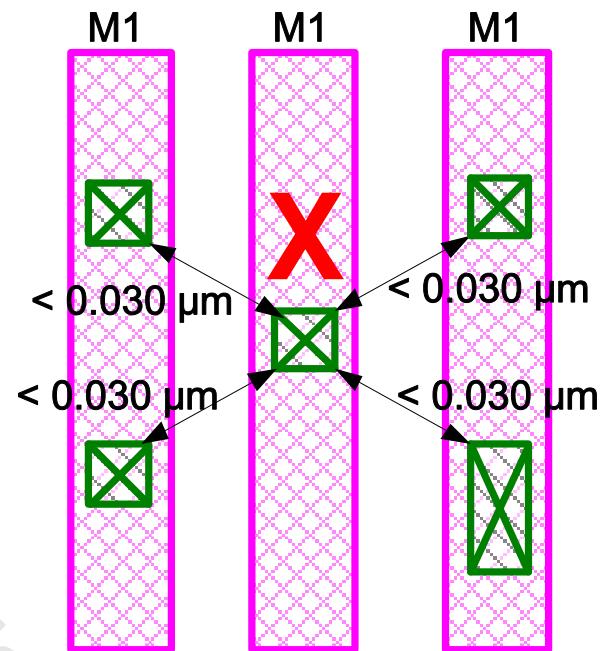
VIA0.R.13.2



VIA0 space to 4 or more VIA0
< 0.030 µm is not allowed



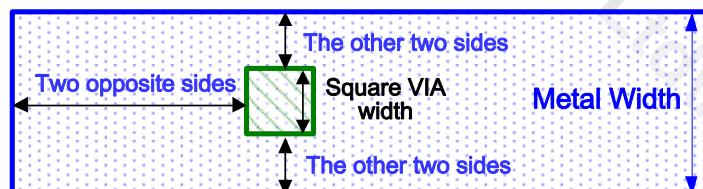
VIA0 space to 4 or more VIA0
< 0.030 µm is not allowed



VIA0.R.22

4.5.42.1 VIA0 Enclosure Rule Tabulation

RuleTable.VIA0.EN.31 (Enclosure of square VIA [width = 0.020 μm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIA0.EN.31.1.T	width < 0.022 μm	0.0300 μm	0 μm	BLK_WB
VIA0.EN.31.1.1.T	width < 0.022 μm	0.0240 μm	0 μm	
VIA0.EN.31.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	BLK_WB
VIA0.EN.31.2.1.T	0.022 μm ≤ width < 0.024 μm	0.0240 μm	0.0010 μm	
VIA0.EN.31.3.T	0.024 μm ≤ width < 0.026 μm	0.0300 μm	0.0020 μm	BLK_WB
VIA0.EN.31.3.1.T	0.024 μm ≤ width < 0.026 μm	0.0240 μm	0.0020 μm	
VIA0.EN.31.4.T	0.026 μm ≤ width < 0.028 μm	0.0300 μm	0.0030 μm	
VIA0.EN.31.5.T	0.028 μm ≤ width < 0.034 μm	0.0300 μm	0.0040 μm	BLK_WB
VIA0.EN.31.5.1.T	0.028 μm ≤ width < 0.034 μm	0.0240 μm	0.0040 μm	
VIA0.EN.31.6.T	0.034 μm ≤ width < 0.040 μm	0.0300 μm	0.0040 μm	BLK_WB
VIA0.EN.31.6.1.T	0.034 μm ≤ width < 0.040 μm	0.0300 μm	0.0010 μm	
VIA0.EN.31.7.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIA0.EN.31.8.T	0.060 μm ≤ width < 0.080 μm	0.0250 μm	0.0200 μm	
VIA0.EN.31.9.T	width = 0.080 μm	0.0200 μm	0.0300 μm	
VIA0.EN.31.10.T	0.080 μm < width < 0.260 μm	0.0200 μm	0.0300 μm	
VIA0.EN.31.11.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	

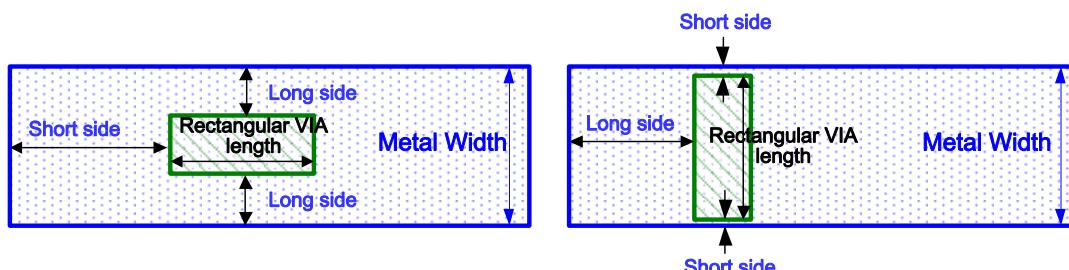


RuleTable.VIA0.EN.32 (Enclosure of rectangular VIA [length = 0.050 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIA0.EN.32.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIA0.EN.32.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIA0.EN.32.3.T	0.024 μm ≤ width < 0.026 μm	0.0300 μm	0.0020 μm	
VIA0.EN.32.4.T	0.026 μm ≤ width < 0.028 μm	0.0300 μm	0.0030 μm	
VIA0.EN.32.5.T	0.028 μm ≤ width < 0.034 μm	0.0300 μm	0.0040 μm	
VIA0.EN.32.6.T	0.034 μm ≤ width < 0.040 μm	0.0300 μm	0.0040 μm	
VIA0.EN.32.7.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIA0.EN.32.8.T	0.060 μm ≤ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0300 μm	
VIA0.EN.32.9.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIA0.EN.32.10.T	0.080 μm < width < 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	SEALRING_ALL
VIA0.EN.32.11.T	width ≥ 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	SEALRING_ALL

RuleTable.VIA0.EN.33 (Enclosure of rectangular VIA [length = 0.034 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIA0.EN.33.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIA0.EN.33.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIA0.EN.33.3.T	0.024 μm ≤ width < 0.026 μm	0.0300 μm	0.0020 μm	
VIA0.EN.33.4.T	0.026 μm ≤ width < 0.028 μm	0.0300 μm	0.0030 μm	
VIA0.EN.33.5.T	0.028 μm ≤ width < 0.034 μm	0.0300 μm	0.0040 μm	
VIA0.EN.33.6.T	0.034 μm ≤ width < 0.040 μm	0.0300 μm	0.0040 μm	
VIA0.EN.33.7.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	BLK_WB
VIA0.EN.33.7.1.T	0.040 μm ≤ width < 0.060 μm	0.0300/0.0050 μm	0.0100/0.0400 μm	
VIA0.EN.33.8.T	0.060 μm ≤ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0300 μm	
VIA0.EN.33.9.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIA0.EN.33.10.T	0.080 μm < width < 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	SEALRING_ALL
VIA0.EN.33.11.T	width ≥ 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	SEALRING_ALL



Rule No.	Description	Label	Op.	Rule
VIA0.EN.31.1.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
VIA0.EN.31.1.1.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$		\geq	0.0240
VIA0.EN.31.2.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.022 $\mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
VIA0.EN.31.2.1.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.022 $\mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0240
VIA0.EN.31.3.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.024 $\mu\text{m} \leq \text{width} < 0.026 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
VIA0.EN.31.3.1.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.024 $\mu\text{m} \leq \text{width} < 0.026 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0240
VIA0.EN.31.4.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.026 $\mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0030 \mu\text{m}$		\geq	0.0300
VIA0.EN.31.5.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.028 $\mu\text{m} \leq \text{width} < 0.034 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0040 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
VIA0.EN.31.5.1.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.028 $\mu\text{m} \leq \text{width} < 0.034 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0040 \mu\text{m}$		\geq	0.0240
VIA0.EN.31.6.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.034 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0040 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
VIA0.EN.31.6.1.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.034 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIA0.EN.31.7.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.040 $\mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
VIA0.EN.31.8.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.060 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$		\geq	0.0250
VIA0.EN.31.9.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [width = 0.080 μm] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$		\geq	0.0200
VIA0.EN.31.10.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [0.080 $\mu\text{m} < \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$		\geq	0.0200
VIA0.EN.31.11.T	Enclosure of square VIA0 [width = 0.020 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
VIA0.EN.32.1.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0300
VIA0.EN.32.2.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [0.022 $\mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIA0.EN.32.3.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [0.024 $\mu\text{m} \leq \text{width} < 0.026 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIA0.EN.32.4.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [0.026 $\mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] with the other two long sides $\geq 0.0030 \mu\text{m}$		\geq	0.0300

Rule No.	Description	Label	Op.	Rule
VIA0.EN.32.5.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [0.028 μm ≤ width < 0.034 μm] with the other two long sides ≥ 0.0040 μm		≥	0.0300
VIA0.EN.32.6.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [0.034 μm ≤ width < 0.040 μm] with the other two long sides ≥ 0.0040 μm		≥	0.0300
VIA0.EN.32.7.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [0.040 μm ≤ width < 0.060 μm] with the other two long sides ≥ 0.0100 μm		≥	0.0300
VIA0.EN.32.8.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [0.060 μm ≤ width < 0.080 μm] with the other two long sides ≥ 0.0200/0.0300 μm		≥	0.0250/0.0050
VIA0.EN.32.9.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides ≥ 0.0200/0.0300 μm		≥	0.0250/0.0150
VIA0.EN.32.10.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [0.080 μm < width < 0.260 μm] with the other two long sides ≥ 0.0300/0.0250 μm (Except SEALRING_ALL)		≥	0.0250/0.0300
VIA0.EN.32.11.T	Short side enclosure of rectangular VIA0 [length = 0.050 μm] by Lower_Metal [width ≥ 0.260 μm] with the other two long sides ≥ 0.0300/0.0250 μm (Except SEALRING_ALL)		≥	0.0250/0.0300
VIA0.EN.33.1.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides ≥ 0 μm		≥	0.0300
VIA0.EN.33.2.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.022 μm ≤ width < 0.024 μm] with the other two long sides ≥ 0.0010 μm		≥	0.0300
VIA0.EN.33.3.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.024 μm ≤ width < 0.026 μm] with the other two long sides ≥ 0.0020 μm		≥	0.0300
VIA0.EN.33.4.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.026 μm ≤ width < 0.028 μm] with the other two long sides ≥ 0.0030 μm		≥	0.0300
VIA0.EN.33.5.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.028 μm ≤ width < 0.034 μm] with the other two long sides ≥ 0.0040 μm		≥	0.0300
VIA0.EN.33.6.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.034 μm ≤ width < 0.040 μm] with the other two long sides ≥ 0.0040 μm		≥	0.0300
VIA0.EN.33.7.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.040 μm ≤ width < 0.060 μm] with the other two long sides ≥ 0.0100 μm (Except BLK_WB)		≥	0.0300
VIA0.EN.33.7.1.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.040 μm ≤ width < 0.060 μm] with the other two long sides ≥ 0.0100/0.0400 μm		≥	0.0300/0.0050
VIA0.EN.33.8.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.060 μm ≤ width < 0.080 μm] with the other two long sides ≥ 0.0200/0.0300 μm		≥	0.0250/0.0050
VIA0.EN.33.9.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides ≥ 0.0200/0.0300 μm		≥	0.0250/0.0150
VIA0.EN.33.10.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [0.080 μm < width < 0.260 μm] with the other two long sides ≥ 0.0300/0.0250 μm (Except SEALRING_ALL)		≥	0.0250/0.0300
VIA0.EN.33.11.T	Short side enclosure of rectangular VIA0 [length = 0.034 μm] by Lower_Metal [width ≥ 0.260 μm] with the other two long sides ≥ 0.0300/0.0250 μm (Except SEALRING_ALL)		≥	0.0250/0.0300

4.5.43 M1 Layout Rules

- Minimum Pitch (MINP) can only be drawn in perpendicular to PO direction.
- NonMinimum Pitch (NMINP) direction is perpendicular to Minimum pitch (MINP) direction.

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

M1 (CAD layer: 31;420) is used for main pattern M1

DM1_O (CAD layer: 31;427, or DM1_Oxs) is used for OPC dummy M1

DM1 (CAD layer: 31;421) is used for Non-OPC dummy M1

M1 line-end (end) definition: M1 width $\leq 0.060 \mu\text{m}$.

DRC checks DM1_O as well as M1 in this section.

Rule No.	Description	Label	Op.	Rule
M1.W.1	Width	W1	\geq	0.0200
M1.W.1.1	Width [MINP direction]	W1A	=	0.0200, 0.0220, 0.0240, 0.0310, ≥ 0.0340
M1.W.1.1.1	Width of M1 (31;420) [MINP direction] (Except BLK_M1)	W1A	=	0.0200, 0.0220, 0.0240, ≥ 0.0340
M1.W.1.1.2	Width of DM1_O [MINP direction]	W1A2	=	0.0240, 0.0400, 0.1400
M1.W.1.2	Width [NMINP direction]	W1B	=	0.0600, ≥ 0.0800
M1.W.1.2.1	Width [NMINP direction] (Except following conditions: 1. M1 [INTERACT BLK_M1, INSIDE BLK_WB])	W1B1	=	0.0600, 0.0800, ≥ 0.1000
M1.W.2	Width of 45-degree bent M1 (Except SEALRING_ALL)	W2	\geq	0.4000
M1.W.3	Maximum width (Except SEALRING_ALL, LOGO)	W3	\leq	0.5000
M1.W.4	Width of M1_VIRT in MINP direction	W4	=	0.0200, 0.0220
M1.W.4.1	Width of {M1_VIRT [width = 0.020 μm] OR M1 [INTERACT M1_VIRT [width = 0.020 μm]]} in MINP direction	W4A	=	0.0200
M1.W.4.1.1	Width of {M1_VIRT [width = 0.022 μm] OR M1 [INTERACT M1_VIRT [width = 0.022 μm]]} in MINP direction	W4A	=	0.0220
M1.W.4.2	Width of M1_VIRT in NMINP direction	W4B	\geq	0.1500
M1.S.1	Space	S1	\geq	0.0180
M1.S.2	Space of M1_VIRT [width = 0.020 μm in MINP direction] to M1 [with edge length $> 0.020 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > -0.018 μm]	S2	\geq	0.0400
M1.S.2.0.1	Space of M1_VIRT [width = 0.022 μm in MINP direction] to M1 [with edge length $< 0.022 \mu\text{m}$, or edge length $> 0.022 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > -0.020 μm]	S2	\geq	0.0400
M1.S.2.1	Space of M1_VIRT to DM1_O in NMINP direction [PRL > -0.020 μm]	S2A	\geq	0.0400
M1.S.12	Space to 45-degree bent M1 [PRL > 0 μm] (Except SEALRING_ALL)	S12	\geq	0.4000
M1.S.12.1	Space to 45-degree bent M1 (Except SEALRING_ALL)	S12A	\geq	0.1400
M1.S.13.1	Space to VIA0 or VIA1 [maximum delta V > 0.96V]	S13	\geq	0.0550
M1.S.13.2	Space to VIA0 or VIA1 [maximum delta V > 1.32V] (1.2V + 10%)	S13	\geq	0.0640
M1.S.13.3	Space to VIA0 or VIA1 [maximum delta V > 1.65V] (1.5V + 10%)	S13	\geq	0.0700
M1.S.13.4	Space to VIA0 or VIA1 [maximum delta V > 1.98V] (1.8V + 10%)	S13	\geq	0.0820
M1.S.13.5	Space to VIA0 or VIA1 [maximum delta V > 2.75V] (2.5V + 10%)	S13	\geq	0.0870
M1.S.16	Space to {SRM (50;0) OR SRAMDMY (186;0)}	S16	\geq	0.1080
M1.S.18	Space to M1 [maximum delta V > 0.96V] (Except following conditions: 1. M1 in MetalFuse)	S18	\geq	0.0520

Rule No.	Description	Label	Op.	Rule
M1.S.18.1	Space to M1 [maximum delta V > 1.32V] (1.2V + 10%) (Except following conditions: 1. M1 in MetalFuse)	S18	≥	0.0550
M1.S.18.2	Space to M1 [maximum delta V > 1.65V] (1.5V + 10%) (Except following conditions: 1. M1 in MetalFuse)	S18	≥	0.0610
M1.S.18.3	Space to M1 [maximum delta V > 1.98V] (1.8V + 10%) (Except following conditions: 1. M1 in MetalFuse)	S18	≥	0.0690
M1.S.18.4	Space to M1 [maximum delta V > 2.75V] (2.5V + 10%) (Except following conditions: 1. M1 in MetalFuse)	S18	≥	0.0790
M1.S.18.6	Corner projected space of M1 [maximum delta V > 0.96V, -0.060 μm < PRL ≤ 0 μm]	S18F	≥	0.1000
M1.S.18.7	Corner projected space of M1 [maximum delta V > 1.98V, -0.100 μm < PRL ≤ 0 μm]	S18G	≥	0.1000
M1.S.31.1	Space of M1 to M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.035 μm]	S31A	=	0.0180, 0.0200, ≥ 0.0340
M1.S.31.1.1	Space of M1 [NOT INTERACT BLK_M1] to M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	=	0.0180, 0.0200, ≥ 0.0340
M1.S.31.1.2	Space of M1 to M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	=	0.0180, 0.0200, ≥ 0.0340
M1.S.31.1.3	Space of {M1 OR M1_VIRT} to {M1 OR M1_VIRT} [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	=	0.0180, 0.0200, ≥ 0.0340
M1.S.31.2	Space of M1 to M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.035 μm]	SM	=	0.0200, ≥ 0.0340
M1.S.31.2.1	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	=	0.0200, ≥ 0.0340
M1.S.31.2.2	Space of M1 to M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	=	0.0200, ≥ 0.0340
M1.S.31.2.3	Space of {M1 OR M1_VIRT} to {M1 OR M1_VIRT} [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	=	0.0200, ≥ 0.0340
M1.S.31.3	Space of M1 to M1 [0.0225 μm ≤ width < 0.0245 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.035 μm]	SM	=	0.0200, ≥ 0.0260
M1.S.31.3.1	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.0225 μm ≤ width < 0.0245 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	=	0.0200, ≥ 0.0260
M1.S.31.3.2	Space of M1 to M1 [0.0225 μm ≤ width < 0.0245 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	=	0.0200, ≥ 0.0260
M1.S.31.3.3	Space of M1_VIRT to M1 [0.0225 μm ≤ width < 0.0245 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	=	0.0200, ≥ 0.0260
M1.S.32.1.T	Space of M1 to M1 [0.0245 μm ≤ width < 0.034 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0200
M1.S.32.1.1.T	Space of M1_VIRT to M1 [0.0245 μm ≤ width < 0.034 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.32.2.T	Space of M1 to M1 [0.034 μm ≤ width < 0.0605 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.038 μm]	SM	≥	0.0200
M1.S.32.2.1.T	Space of M1_VIRT to M1 [0.034 μm ≤ width < 0.0605 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.33.1.T	Space of M1 to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.035 μm]	SM	≥	0.0200

Rule No.	Description	Label	Op.	Rule
M1.S.33.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0200
M1.S.33.1.2.T	Space of M1 to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0200
M1.S.33.1.3.T	Space of M1_VIRT to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.34.1.T	Space of M1 to M1 [0.0845 μm ≤ width < 0.100 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.035 μm]	SM	≥	0.0260
M1.S.34.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.0845 μm ≤ width < 0.100 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.34.1.2.T	Space of M1 to M1 [0.0845 μm ≤ width < 0.100 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.34.1.3.T	Space of M1_VIRT to M1 [0.0845 μm ≤ width < 0.100 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.35.1.T	Space of M1 to M1 [0.100 μm ≤ width < 0.260 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0370
M1.S.35.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.100 μm ≤ width < 0.260 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.35.1.2.T	Space of M1 to M1 [0.100 μm ≤ width < 0.260 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.35.1.3.T	Space of M1_VIRT to M1 [0.100 μm ≤ width < 0.260 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.35.2.T	Space of M1 to M1 [width ≥ 0.260 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.35.2.1.T	Space of M1_VIRT to M1 [width ≥ 0.260 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.37.1.T	Space of M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.0245 μm ≤ width < 0.034 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.1.1.T	Space of M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.034 μm ≤ width < 0.0605 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.2.T	Space of M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.3.T	Space of M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.0245 μm ≤ width < 0.034 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.3.1.T	Space of M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.034 μm ≤ width < 0.0605 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.4.T	Space of M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.41.1.T	Space of M1 to M1 [width < 0.080 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0600

Rule No.	Description	Label	Op.	Rule
M1.S.41.1.1.T	Space of M1_VIRT to M1 [width < 0.080 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0600
M1.S.42.1.T	Space of M1 to M1 [0.080 μm ≤ width < 0.100 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0300
M1.S.42.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.080 μm ≤ width < 0.100 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760
M1.S.42.1.2.T	Space of M1 to M1 [0.080 μm ≤ width < 0.100 μm with edge length > 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760
M1.S.42.1.3.T	Space of M1_VIRT to M1 [0.080 μm ≤ width < 0.100 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760
M1.S.43.1.T	Space of M1 to M1 [0.100 μm ≤ width < 0.120 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0300
M1.S.43.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.100 μm ≤ width < 0.120 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760
M1.S.43.1.2.T	Space of M1 to M1 [0.100 μm ≤ width < 0.120 μm with edge length > 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760
M1.S.43.1.3.T	Space of M1_VIRT to M1 [0.100 μm ≤ width < 0.120 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760
M1.S.44.1.T	Space of M1 to M1 [0.120 μm ≤ width < 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0300
M1.S.44.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.120 μm ≤ width < 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0600
M1.S.44.1.2.T	Space of M1 to M1 [0.120 μm ≤ width < 0.140 μm with edge length > 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0600
M1.S.44.3.1.T	Space of M1_VIRT to M1 [0.120 μm ≤ width < 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0600
M1.S.44.2.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.120 μm ≤ width < 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.020 μm]	SN	≥	0.0760
M1.S.44.2.2.T	Space of M1 to M1 [0.120 μm ≤ width < 0.140 μm with edge length > 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL > -0.020 μm]	SN	≥	0.0760
M1.S.44.4.1.T	Space of M1_VIRT to M1 [0.120 μm ≤ width < 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.020 μm]	SN	≥	0.0760
M1.S.45.1.T	Space of M1 to M1 [width ≥ 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > 0 μm]	SN	≥	0.0300
M1.S.45.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [width ≥ 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > 0 μm]	SN	≥	0.1200
M1.S.45.1.2.T	Space of M1 to M1 [width ≥ 0.140 μm with edge length > 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL > 0 μm]	SN	≥	0.1200
M1.S.45.2.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [width ≥ 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > 0.080 μm]	SN	≥	0.1600
M1.S.45.2.2.T	Space of M1 to M1 [width ≥ 0.140 μm with edge length > 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL > 0.080 μm]	SN	≥	0.1600
M1.S.45.3.1.T	Space of M1_VIRT to M1 [width ≥ 0.140 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > 0 μm]	SN	≥	0.1200

Rule No.	Description	Label	Op.	Rule
M1.S.46.1.T	Space of M1 to M1 [width \geq 0.160 μm with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.0300
M1.S.46.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [width \geq 0.160 μm with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1200
M1.S.46.1.2.T	Space of M1 to M1 [width \geq 0.160 μm with edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1200
M1.S.46.1.3.T	Space of M1_VIRT to M1 [width \geq 0.160 μm with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1200
M1.S.46.2.T	Space of M1 [edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] to M1 [width \geq 0.160 μm with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1400
M1.S.46.2.1.T	Space of M1 [edge length $> 0.060 \mu\text{m}$ in MINP direction] to M1 [width $\geq 0.160 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1400
M1.S.46.3.T	Space of M1 [edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] to M1 [width $\geq 0.160 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0.080 \mu\text{m}$]	SN	\geq	0.1800
M1.S.46.3.1.T	Space of M1 [edge length $> 0.060 \mu\text{m}$ in MINP direction] to M1 [width $\geq 0.160 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $> 0.080 \mu\text{m}$]	SN	\geq	0.1800
M1.S.47.1.T	Space of M1 to M1 [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.0300
M1.S.47.1.1.T	Space of M1 [NOT INTERACT BLK_M1] to M1 [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1200
M1.S.47.1.2.T	Space of M1 to M1 [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1200
M1.S.47.1.3.T	Space of M1_VIRT to M1 [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1200
M1.S.47.2.T	Space of M1 [edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] to M1 [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1800
M1.S.47.2.1.T	Space of M1 [edge length $> 0.060 \mu\text{m}$ in MINP direction] to M1 [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $> 0 \mu\text{m}$]	SN	\geq	0.1800
M1.S.47.3.T	Space of M1 [edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] to M1 [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL $> 0.080 \mu\text{m}$]	SN	\geq	0.2600
M1.S.47.3.1.T	Space of M1 [edge length $> 0.060 \mu\text{m}$ in MINP direction] to M1 [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $> 0.080 \mu\text{m}$]	SN	\geq	0.2600
M1.S.51.1	Space of M1 to M1 line-end in NMINP direction [PRL $> -0.018 \mu\text{m}$]	S51	\geq	0.0300
M1.S.51.2	Space of M1 to M1 line-end [edge length = 0.020 μm] in NMINP direction [PRL $> -0.018 \mu\text{m}$]	S51	\geq	0.0350
M1.S.51.2.1	Space of M1 [NOT INTERACT BLK_M1] to M1 line-end [edge length = 0.020 μm] in NMINP direction [PRL $> -0.018 \mu\text{m}$]	S51	\geq	0.0400
M1.S.51.2.2	Space of M1 to M1 line-end [edge length = 0.020 μm , NOT INTERACT BLK_M1] in NMINP direction [PRL $> -0.018 \mu\text{m}$]	S51	\geq	0.0400
M1.S.51.3	Space of M1 to M1 line-end [0.020 μm $<$ edge length $<$ 0.034 μm] in NMINP direction [PRL $> -0.020 \mu\text{m}$]	S51	\geq	0.0350
M1.S.51.3.1	Space of M1 [NOT INTERACT BLK_M1] to M1 line-end [0.020 μm $<$ edge length $<$ 0.034 μm] in NMINP direction [PRL $> -0.020 \mu\text{m}$]	S51	\geq	0.0400
M1.S.51.3.2	Space of M1 to M1 line-end [0.020 μm $<$ edge length $<$ 0.034 μm , NOT INTERACT BLK_M1] in NMINP direction [PRL $> -0.020 \mu\text{m}$]	S51	\geq	0.0400
M1.S.51.4	Space of M1 to M1 line-end [0.034 μm \leq edge length $<$ 0.060 μm] in NMINP direction [PRL $> -0.020 \mu\text{m}$]	S51	\geq	0.0350
M1.S.51.4.1	Space of M1 [NOT INTERACT BLK_M1] to M1 line-end [0.034 μm \leq edge length $<$ 0.060 μm] in NMINP direction [PRL $> -0.020 \mu\text{m}$]	S51	\geq	0.0380

Rule No.	Description	Label	Op.	Rule
M1.S.51.4.2	Space of M1 to M1 line-end [$0.034 \mu\text{m} \leq \text{edge length} < 0.060 \mu\text{m}$, NOT INTERACT BLK_M1] in NMINP direction [PRL > -0.020 μm]	S51	\geq	0.0380
M1.S.51.5	Space of M1 to M1 line-end [edge length = 0.060 μm] in NMINP direction [PRL > -0.020 μm]	S51	\geq	0.0300
M1.S.51.5.1	Space of M1 [NOT INTERACT BLK_M1] to M1 line-end [edge length = 0.060 μm] in NMINP direction [PRL > -0.020 μm]	S51	\geq	0.0380
M1.S.51.5.2	Space of M1 to M1 line-end [edge length = 0.060 μm , NOT INTERACT BLK_M1] in NMINP direction [PRL > -0.020 μm]	S51	\geq	0.0380
M1.S.52.1	Space of M1 to M1 line-end in MINP direction [PRL > -0.060 μm]	S52	\geq	0.0600
M1.S.61	Corner projected space of M1 [-0.035 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$] (Except following conditions: 1. Corner with edge [length $\leq 0.040 \mu\text{m}$, between 2 consecutive 90-90 degree corners] on both sides)	S61	\geq	0.0350
M1.S.61.1	Corner projected space of M1 [-0.060 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$] (Except BLK_WB, or following conditions: 1. Corner with edge [length $\leq 0.040 \mu\text{m}$, between 2 consecutive 90-90 degree corners] on both sides)	S61	\geq	0.0600
M1.S.61.2	Corner projected space of {M1_VIRT OR M1} [-0.060 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$] (Except BLK_WB, or following conditions: 1. Corner with edge [length $\leq 0.040 \mu\text{m}$, between 2 consecutive 90-90 degree corners] on both sides)	S61	\geq	0.0600
M1.EN.0	1. Enclosure of square Lower_VIA [width = 0.020 μm] is defined by RuleTable.M1.EN.31 in the subsection 2. Enclosure of rectangular Lower_VIA [length = 0.050 μm] is defined by RuleTable.M1.EN.32 in the subsection 3. Enclosure of rectangular Lower_VIA [length = 0.034 μm] is defined by RuleTable.M1.EN.33 in the subsection 4. Enclosure of rectangular Lower_VIA [length = 0.060 μm] is defined by RuleTable.M1.EN.34 in the subsection			
M1.EN.5.1	Short side enclosure of rectangular VIA0 by M1 edge [length = 0.080 μm , M1 width = 0.080 μm]	EN5	\geq	0.0250
M1.L.1	At least one edge length of 45-degree bent M1 (minimum edge length)	L1	\geq	0.9100
M1.L.2	Edge length with adjacent edge [length < 0.080 μm]	L2	\geq	0.0800
M1.L.2.1	Edge length with adjacent edge [length < 0.090 μm] (Except BLK_M1)	L2A	\geq	0.0800
M1.A.1	Area of M1	A1	\geq	0.00192
M1.A.2	Area of M1 (Except BLK_M1)	A2	\geq	0.00280
M1.A.2.1	Area of M1 (Except FB_9, FB_8, BLK_M1)	A2A	\geq	0.00306
M1.DN.1.1	Minimum All_metal density in window 40 $\mu\text{m} \times 40 \mu\text{m}$, stepping 20 μm (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	12.5%
M1.DN.1.2	Minimum All_metal density in window 40 $\mu\text{m} \times 40 \mu\text{m}$, stepping 20 μm [3 $\mu\text{m} \times 3 \mu\text{m}$ empty area exists in the window] (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	25%
M1.DN.2	Maximum All_metal density in window 40 $\mu\text{m} \times 40 \mu\text{m}$, stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. {DM1_O OR DM1}, 2. {M1 AND BLK_WB})		\leq	65%
M1.DN.2.3	Maximum All_metal density in window 40 $\mu\text{m} \times 40 \mu\text{m}$, stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	75%

Rule No.	Description	Label	Op.	Rule
M1.DN.3	The All_metal density difference between any two neighboring checking windows including DMnEXCL [window 40 µm x 40 µm, stepping 40 µm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≤	50%
M1.DN.6.1	All_metal density [window 9 µm x 9 µm, stepping 4.5 µm] (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
M1.DN.7	It is not allowed to have local density < 5% of all 3 consecutive metal (M1, Mx, and Mx+1) over any 27 µm x 27 µm (stepping 13.5 µm), i.e. it is allowed for either one of M1, Mx, or Mx+1 to have a local density ≥ 5% (The metal layers include M1/Mx/Mx+1 and dummy metals for ELK film) (Except ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc, 2. TCDDMY_Mn (assume 30% pattern density INSIDE TCDDMY_Mn))			
M1.DN.9	Minimum Line edge Density (LeD) in window 20 µm x 20 µm, stepping 10 µm Definition of "Line edge Density": (((All_metal area) - (All_metal SIZING -0.001 µm area)) x 1000) / Checking window (Except TCDDMY_M1, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags only if the checking window has any one metal M1 width < 0.060 µm		≥	8.5
M1.DN.9.1	Minimum Line edge Density (LeD) in window 20 µm x 20 µm, stepping 10 µm Definition of "Line edge Density": (((All_metal area) - (All_metal SIZING -0.001 µm area)) x 1000) / Checking window (Except TCDDMY_M1, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags only if the checking window has any one metal M1 width < 0.120 µm		≥	3
M1.R.1	{M1 NOT BLK_M1} must be a rectangle (Except SEALRING_ALL, LOGO)			
M1.R.1.1	{M1 INTERACT M1 [width < 0.024 µm]} must be a rectangle			
M1.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
M1.R.10	Overlap MetalFuse_B1 (156;8) is not allowed			
M1.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of M1 space to M1 or VIA0 or VIA1 or {M0 NOT CM0} is < 0.360 µm			
M1.R.14	{}{M1_Empty_Area SIZING 0.330 µm} INTERACT M1 island} is not allowed Definitions: 1. M1_Empty_Area: Area of {{CHIP NOT {{TCDDMY_Mn OR ICOVL_SINGLE} OR {{M1 OR DM1} OR DM1_O}}} SIZING down/up 0.380 µm} ≥ 1.96 µm ² 2. M1 island: Area of (M1 with only one VIA0 [width x length = 0.020 µm x 0.020 µm]) ≤ 0.010 µm ²			

Rule No.	Description	Label	Op.	Rule
M1.R.17	DM1 is a must in chip level.			
M1.R.18	<p>M1 [width ≤ 0.022 μm] interact VIA0_array_region is not allowed</p> <p>VIA0_array_region definition:</p> <ul style="list-style-type: none"> (1) VIA0 array is ≥ 2x2 VIA0 array, and (2) Two VIA0 space < 0.140 μm in NMINP direction [PRL > 0 μm], and both of the VIA0 space = 0.0485~0.0760 μm in MINP direction [PRL > -0.020 μm], and (3) Form one region from one of each VIA0 corner (C1/C2/C3/C4), and the space of the corners is the minimum in MINP and NMINP direction. 			
M1.R.18.1	<p>M1 [width ≤ 0.022 μm] interact VIA0_array_region is not allowed</p> <p>VIA0_array_region definition:</p> <ul style="list-style-type: none"> (1) VIA0 array is ≥ 2x2 VIA0 array, and (2) Two VIA0 space < 0.100 μm in NMINP direction [PRL > 0 μm], and both of the VIA0 space = 0.0485~0.0760 μm in MINP direction [PRL > -0.0205 μm], and (3) Form one region from one of each VIA0 corner (C1/C2/C3/C4), and the space of the corners is the minimum in MINP and NMINP direction. 			
M1.R.18.2	<p>Space of M1 [width ≤ 0.022 μm] to Checked_VIA0_Edge in MINP direction [PRL > -0.0205 μm] < 0.056 μm is not allowed</p> <p>Definition of Checked_VIA0_Group: {VIA0 [space to VIA0 < 0.060 μm in NMINP direction, PRL > 0 μm]}</p> <p>Definition of Checked_VIA0_Edge: Checked_VIA0_Group NMINP edge[space to VIA0 = 0.056~0.0935 μm in MINP direction, PRL > -0.020 μm]</p>			
M1.R.18.3	<p>Checked_VIA space to 2 or more Lower_VIA [INTERACT another M1] < 0.029 μm is not allowed</p> <p>Definition of Checked_VIA: Lower_VIA [INTERACT M1 width ≤ 0.022 μm] enclosure by M1 < 0.046 μm in NMINP direction</p> <p>DRC flags Checked_VIA space to 2 or more Lower_VIA < 0.029 μm in MINP with corner direction</p>			
M1.R.19	M1 line-end interact {{SRM (50;0) OR SRAMDMY (186;0)} SIZING 0.108 μm} NOT {SRM (50;0) OR SRAMDMY (186;0)} is not allowed (Abut is allowed)			
M1.R.21	<p>Space of Checked_Metal ≤ 0.018 μm in MINP [PRL > 0 μm] is not allowed</p> <p>Definition of Checked_Metal: {{M1 OR M1_VIRT} [width ≤ 0.020 μm] AND Wide_Metal_Check_Region}</p> <p>Definition of Wide_Metal_Check_Region: {M1 [width ≥ 0.100 μm in MINP direction] expanding edge 0.160 μm in MINP direction}</p>			
M1.R.21.1	<p>Space of Checked_Metal ≤ 0.020 μm in MINP [PRL > 0 μm] is not allowed</p> <p>Definition of Checked_Metal: {{M1 OR M1_VIRT} [width ≤ 0.024 μm] AND Wide_Metal_Check_Region}</p> <p>Definition of Wide_Metal_Check_Region: {M1 [width ≥ 0.260 μm in MINP direction] expanding edge 0.200 μm in MINP direction}</p>			

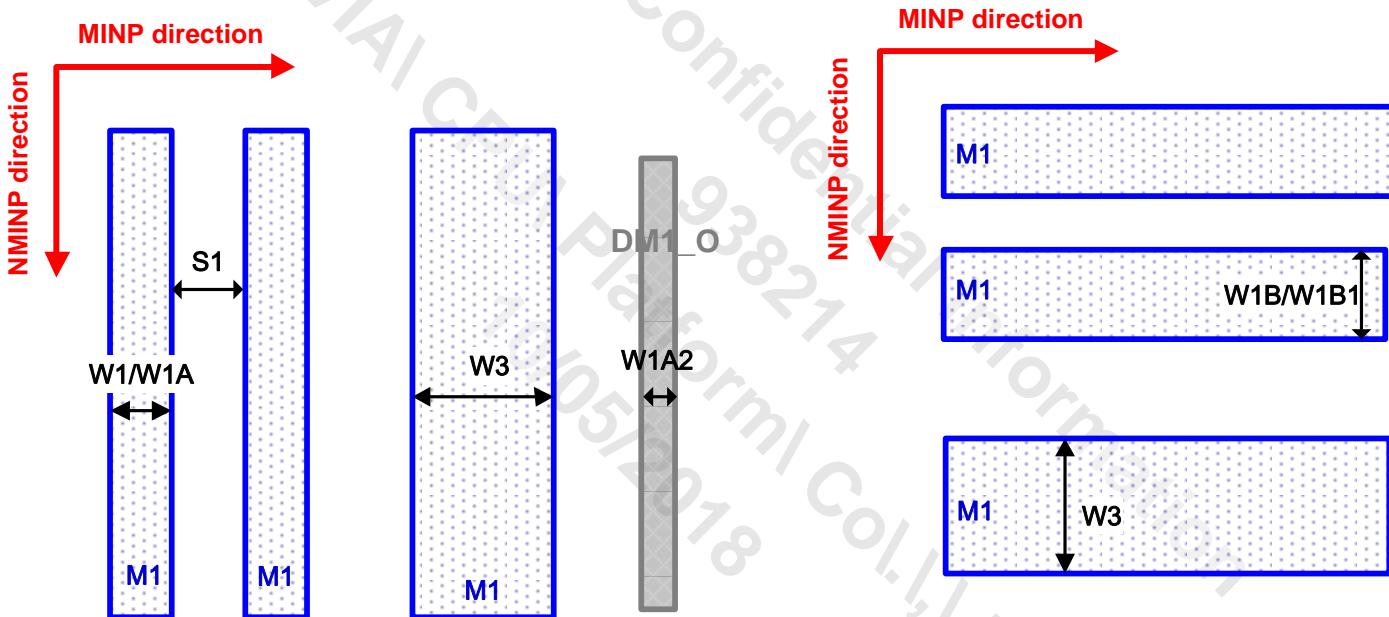
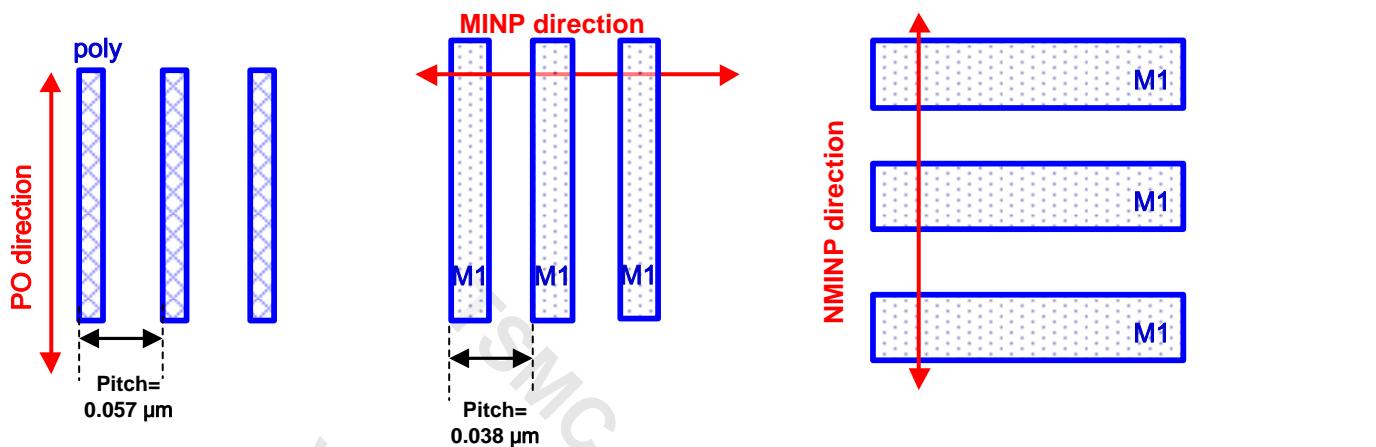
Rule No.	Description	Label	Op.	Rule
M1.R.31.1	M1_VIRT must be a rectangle orthogonal to grid			
M1.R.31.2	<p>$\{\{\{M1 \text{ NOT } \{BLK_M1 \text{ OR INDDMY}\} \text{ OR M1_VIRT}\} \text{ OR }$ Space_Region_1} OR Space_Region_2} must be a rectangle orthogonal to grid (Except SEALRING_ALL, LOGO)</p> <p>Definition of Space_Region_1: Space region < 0.040 μm in vertical direction formed by M1 and M1_VIRT [PRL > -0.018 μm]</p> <p>Definition of Space_Region_2: Space region < 0.040 μm in vertical direction formed by M1_VIRT [PRL > -0.018 μm]</p>			
M1.R.31.3	M1_VIRT interact DM1_O, DM1 is not allowed			
M1.R.31.4	M1_VIRT must be inside {FB_9 OR FB_8}			
M1.R.31.4.1	{FB_9 OR FB_8} [INTERACT M1 (31;420) width = 0.020 μm] interact {M1 (31;420) OR M1_VIRT} [width = 0.022/0.037 μm] is not allowed			
M1.R.31.4.2	{FB_9 OR FB_8} [INTERACT M1 (31;420) width = 0.022 μm] interact {M1 (31;420) OR M1_VIRT} [width = 0.020/0.037 μm] is not allowed			
M1.R.31.4.3	{FB_9 OR FB_8} [INTERACT M1 (31;420) width = 0.037 μm] interact {M1 (31;420) OR M1_VIRT} [width = 0.020/0.022 μm] is not allowed			
M1.R.31.5	{M1_VIRT OR M1} point touch of corners is not allowed			

Table Notes:

- To meet the metal process window, filling the dummy metal globally and uniformly by tsmc utility is needed even if the originally drawn M1 has already met the density rules. For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, filling manually and evenly is needed.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations during placement. Unexpected violations may occur during the IP/macro placement due to the environment, even if the IP/macro already passed the high density rule check. Therefore, customers need to carefully design the dimension of the width/space for wide metal (e.g., power/ground bus), under the proper high density limit.
- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

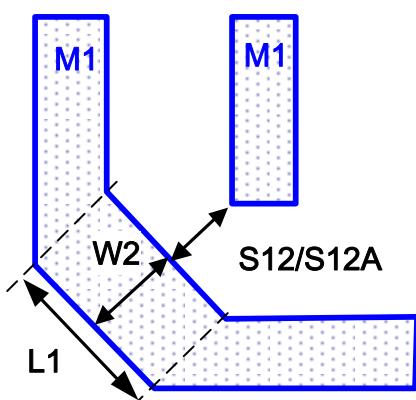
M1

- M1 MINP direction is perpendicular with PO direction
- M1 NMINP direction is parallel to PO direction.

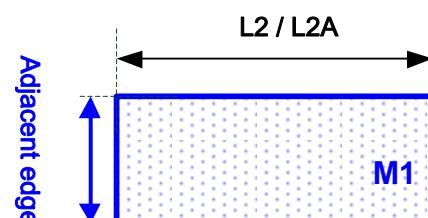


M1.W.1 / M1.W.1.1 / M1.W.1.1.1 /
M1.W.1.1.2 / M1.W.3 / M1.S.1

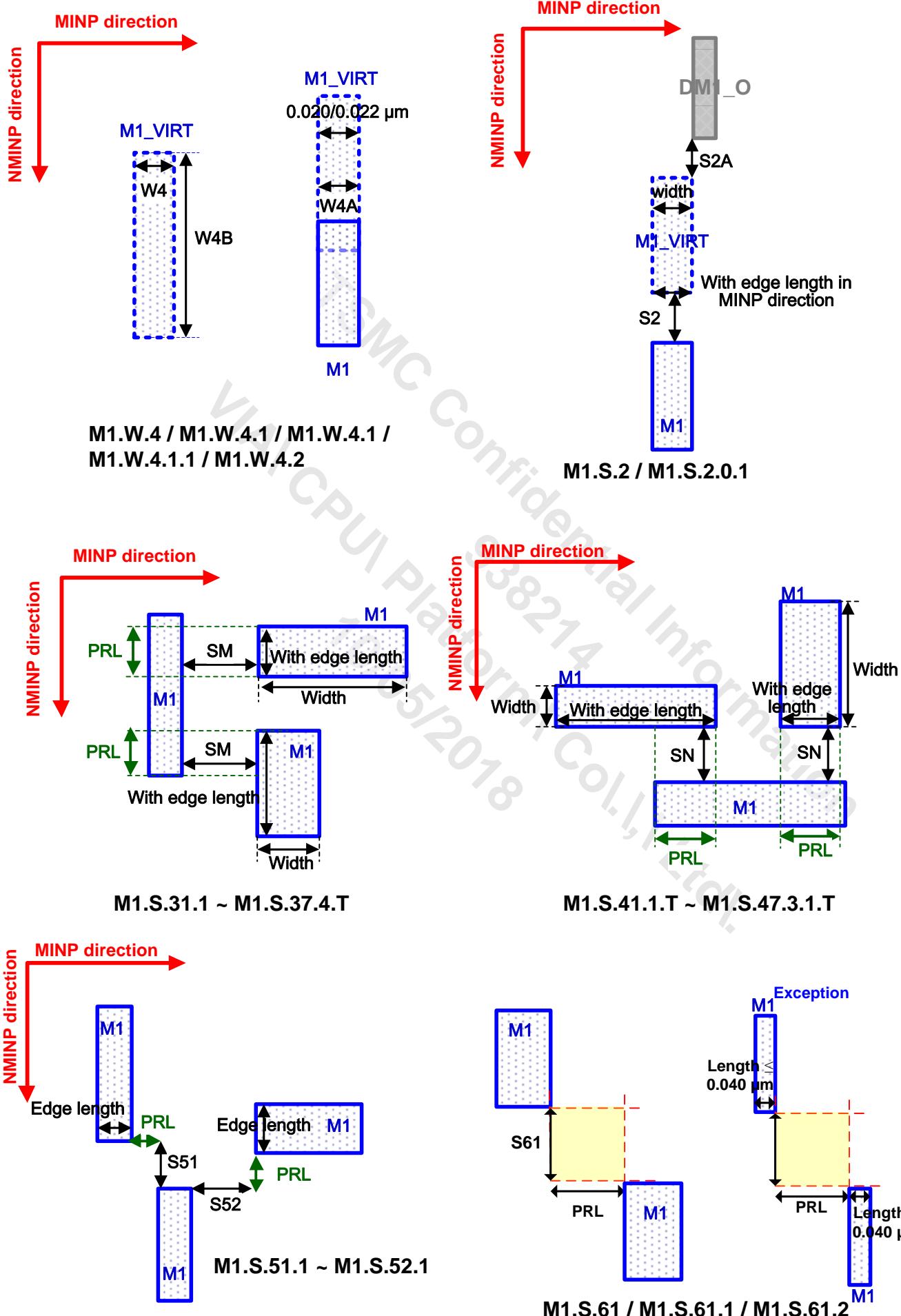
M1.W.1.2 / M1.W.1.2.1 /
M1.W.3

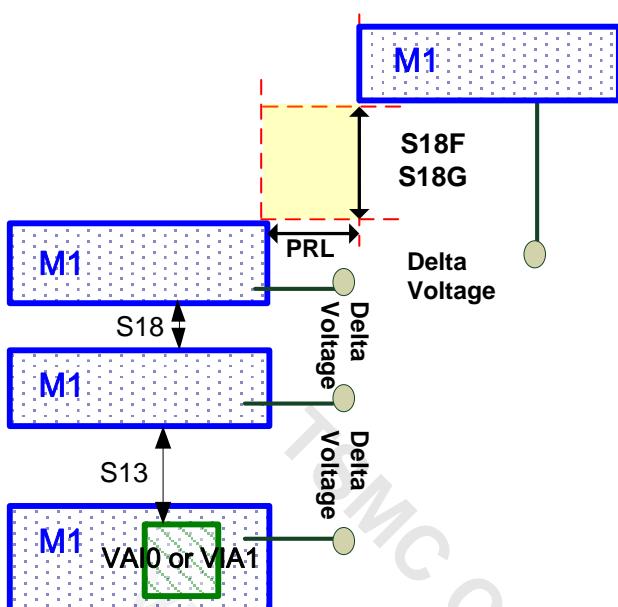


M1.W.2 / M1.S.12 / M1.S.12.1 / M1.L.1



M1.L.2 / M1.L.2.1

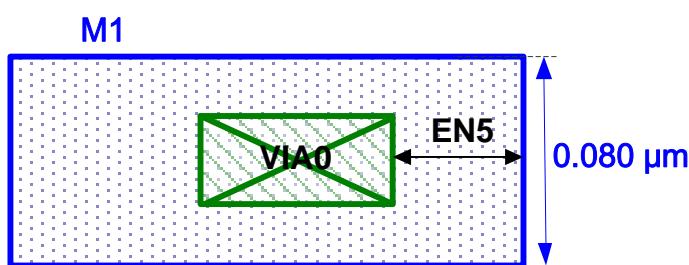
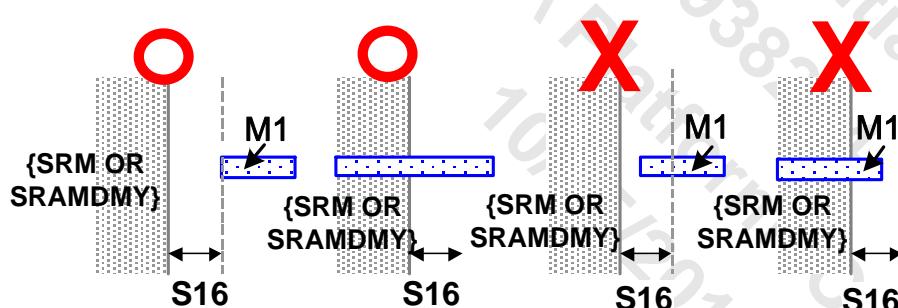




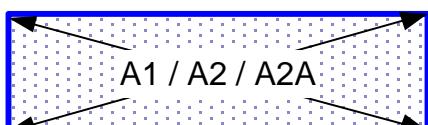
M1.S.13.1 / M1.S.13.2 / M1.S.13.3 / M1.S.13.4 / M1.S.13.5

M1.S.18 / M1.S.18.1 / M1.S.18.2 / M1.S.18.3 / M1.S.18.4

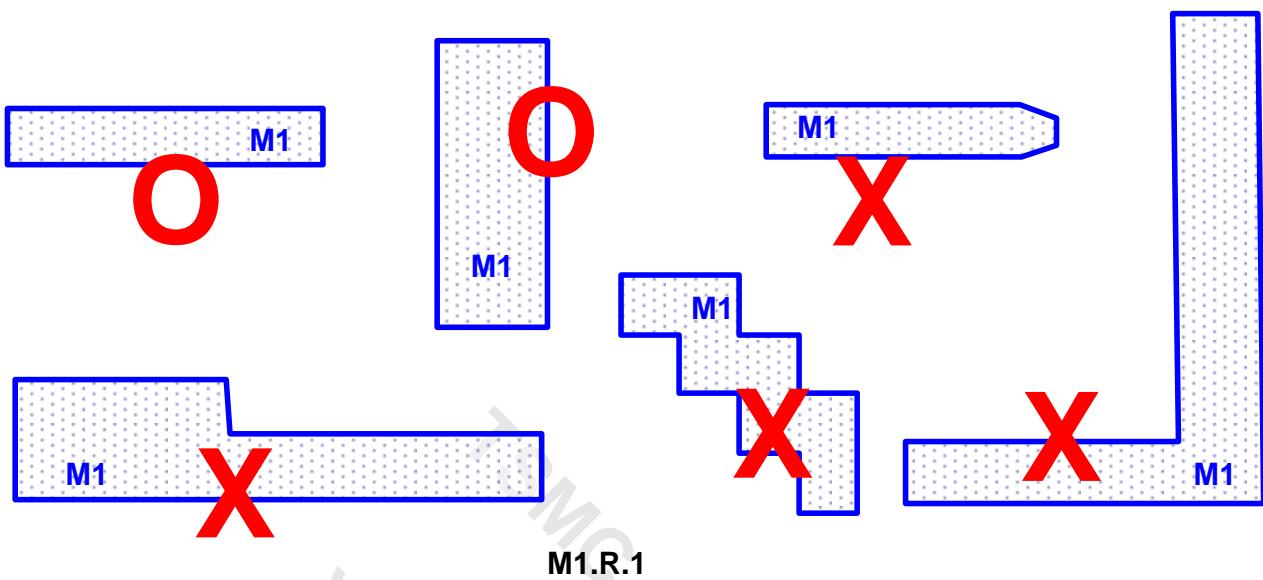
M1.S.18.6 / M1.S.18.7



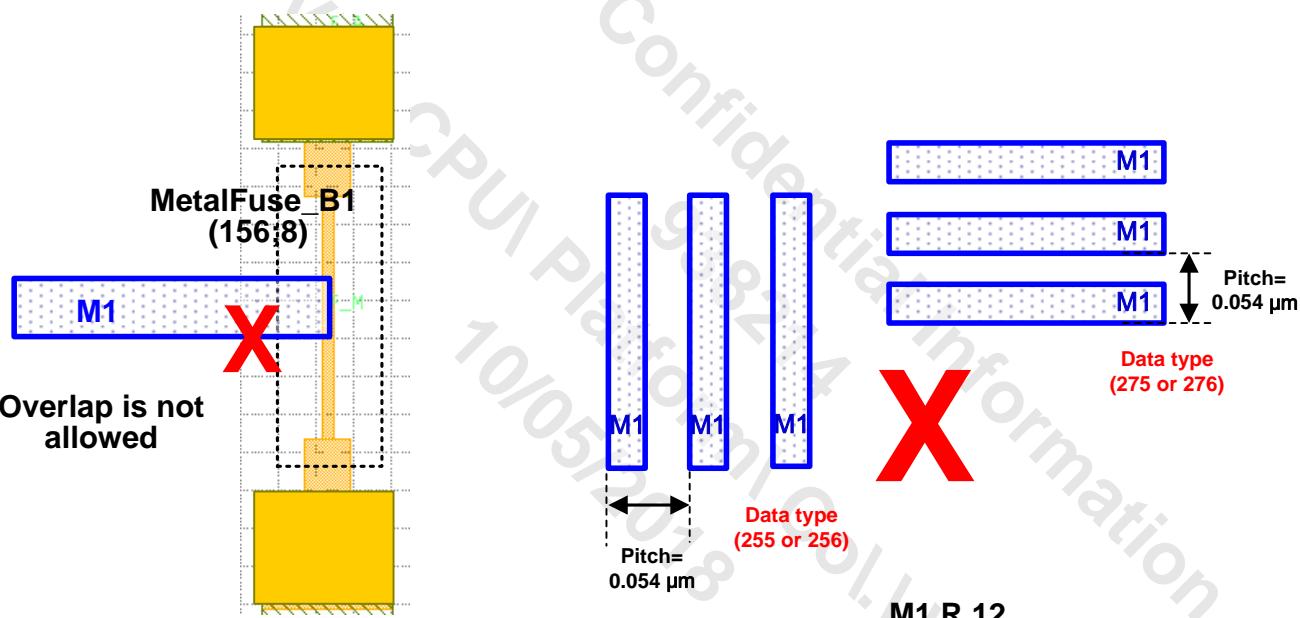
M1.EN.5.1



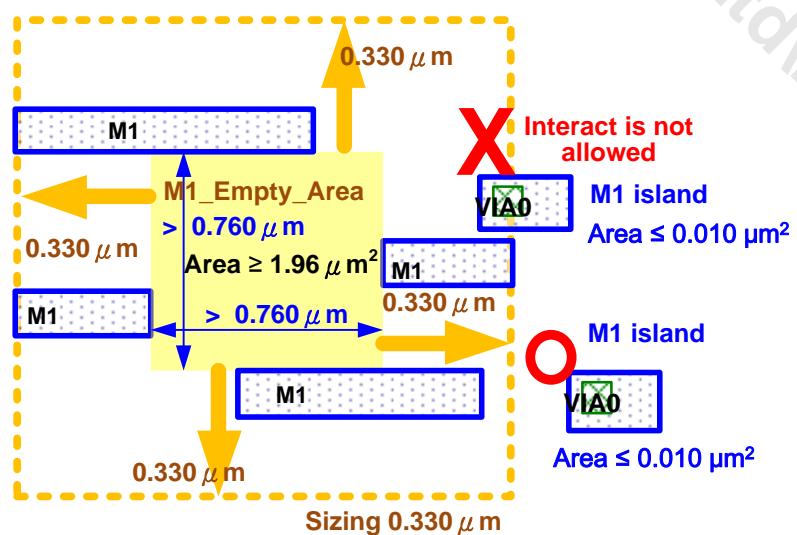
M1.A.1 / M1.A.2 / M1.A.2.1



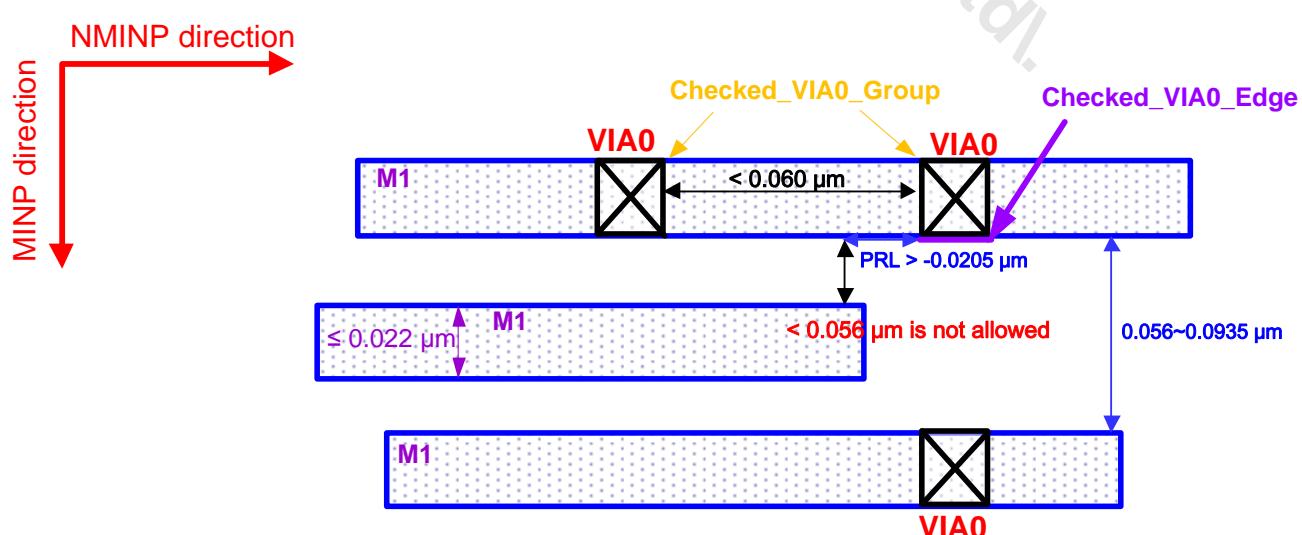
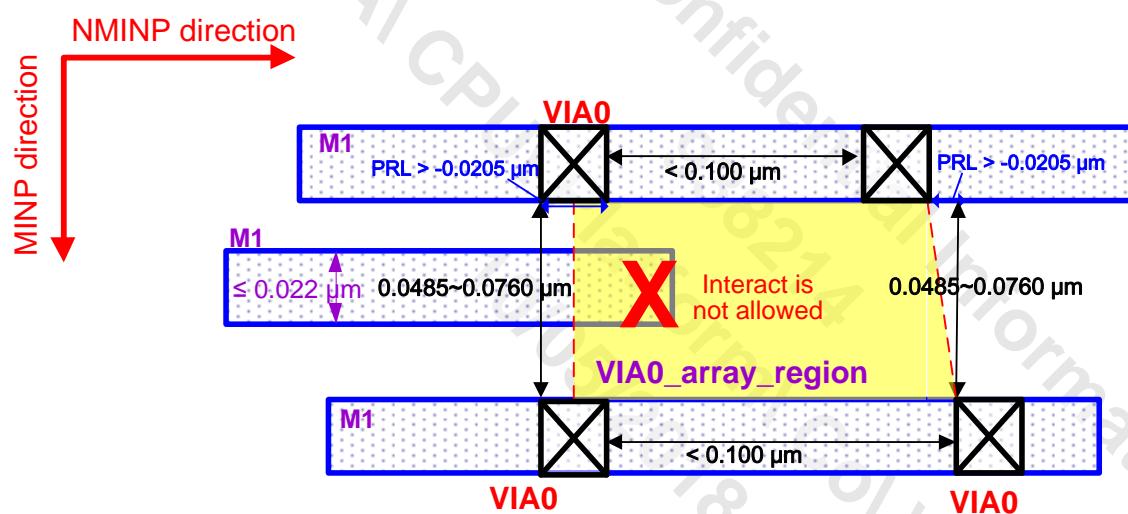
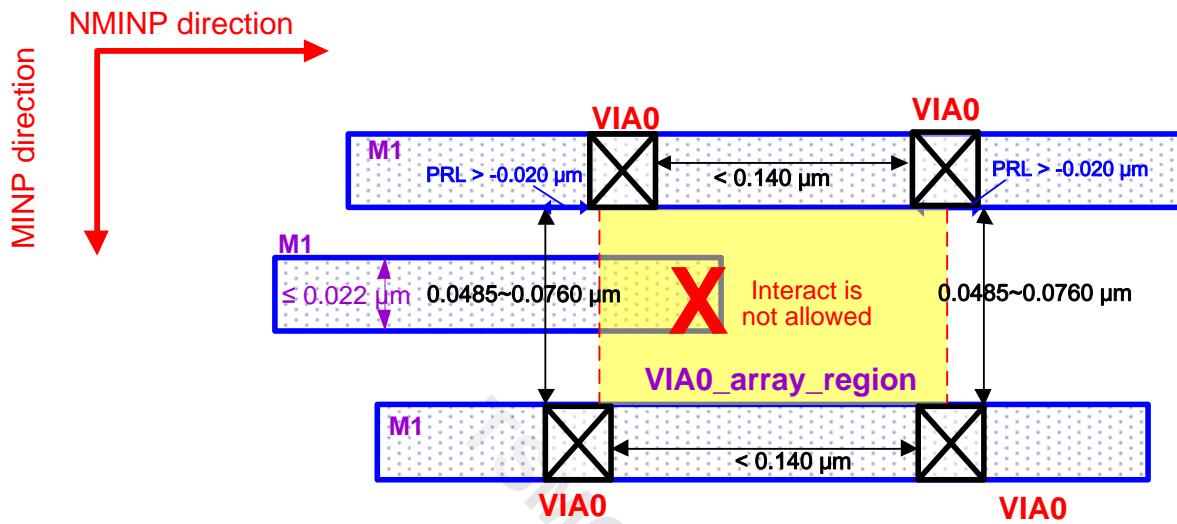
Overlap is not allowed

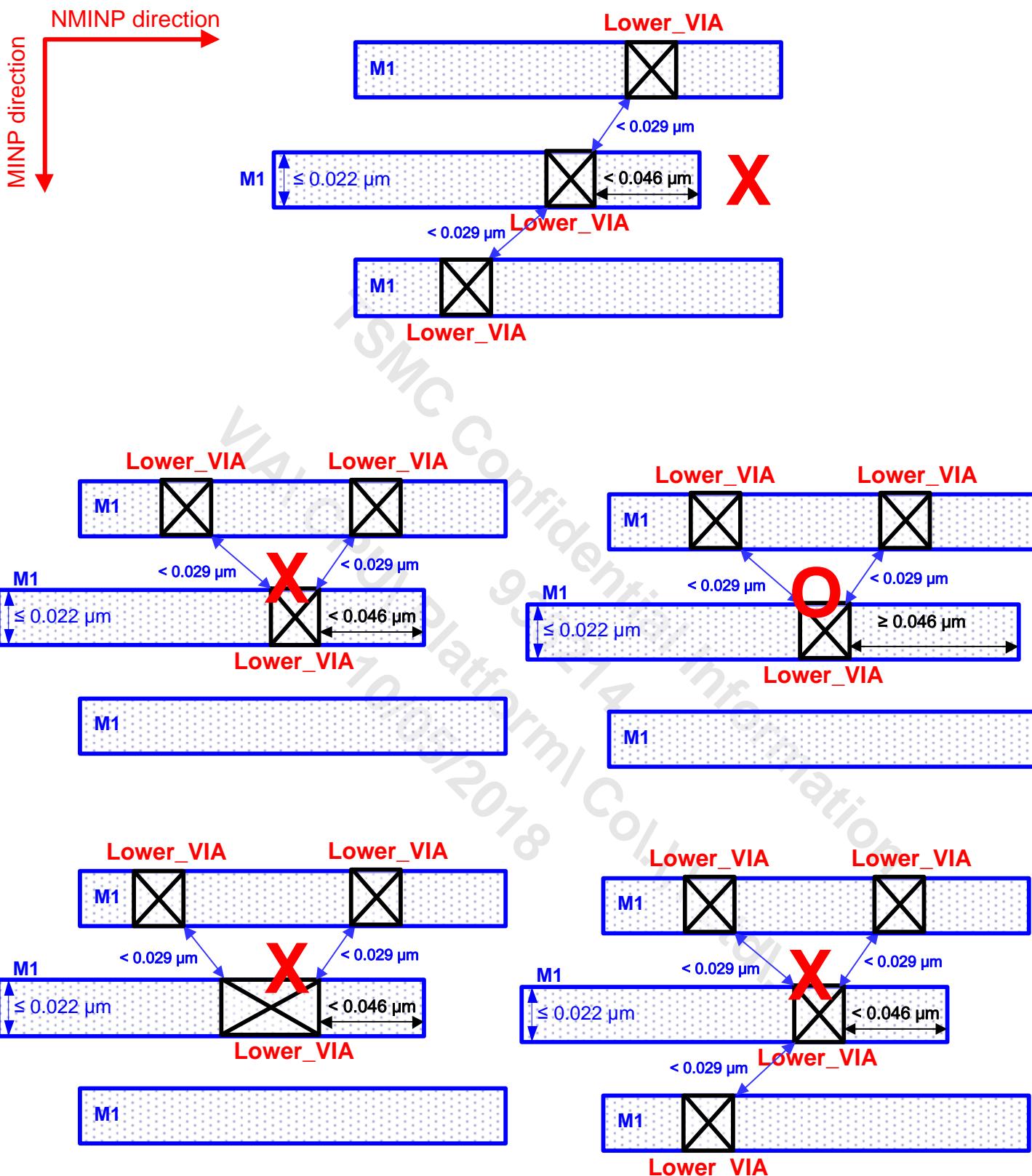


M1.R.10

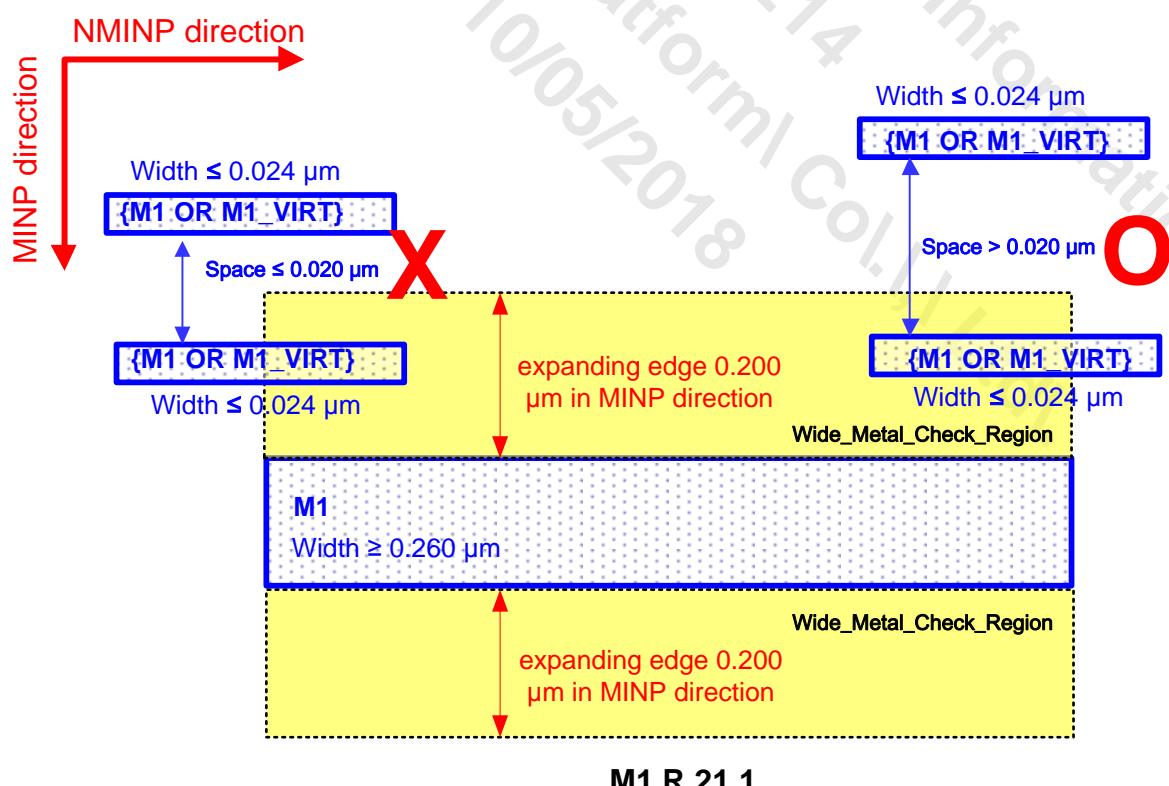
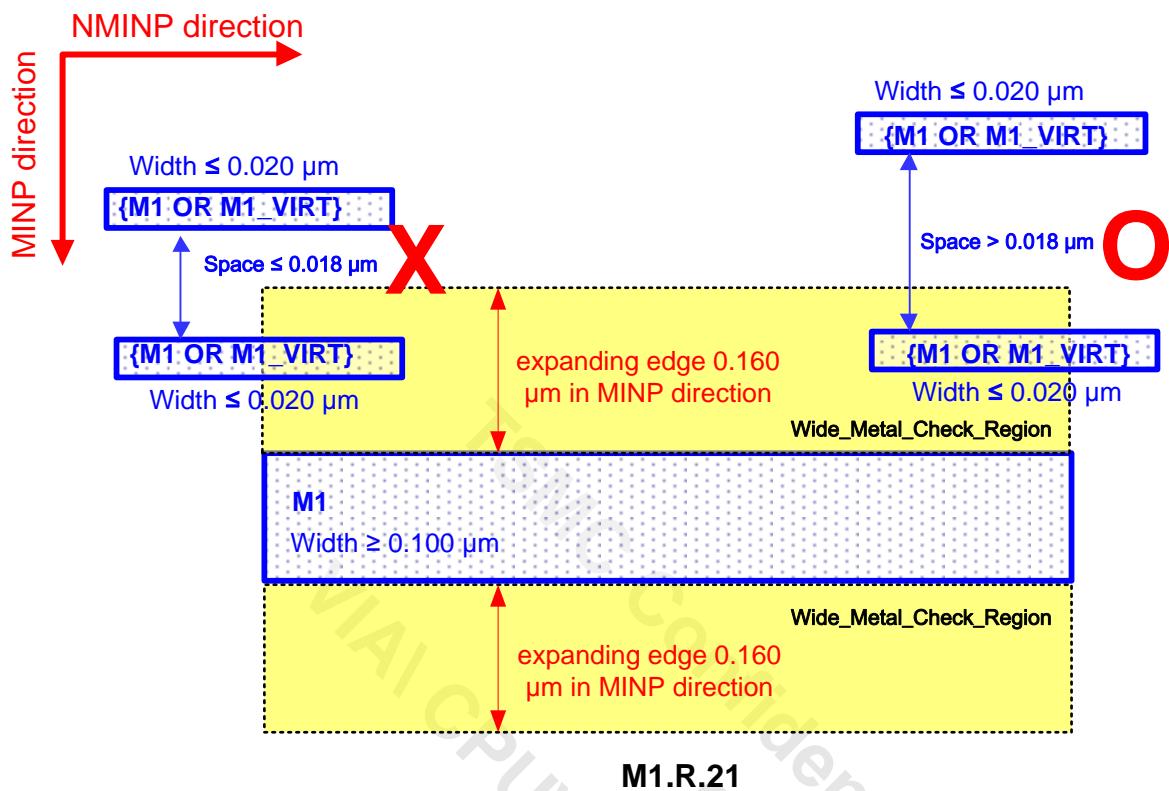


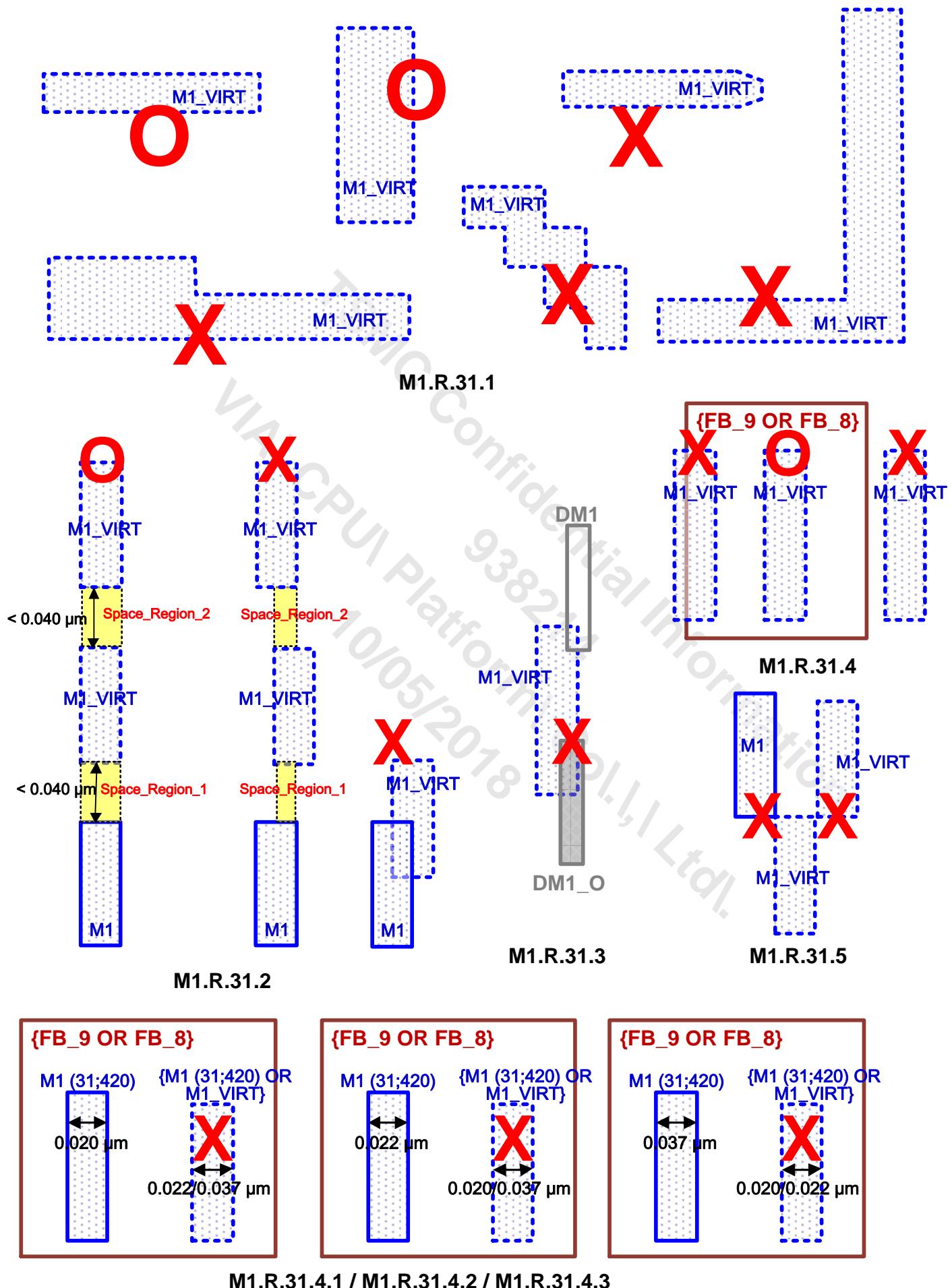
M1.R.14





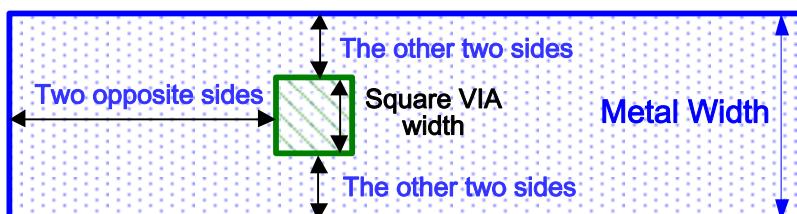
M1.R.18.3





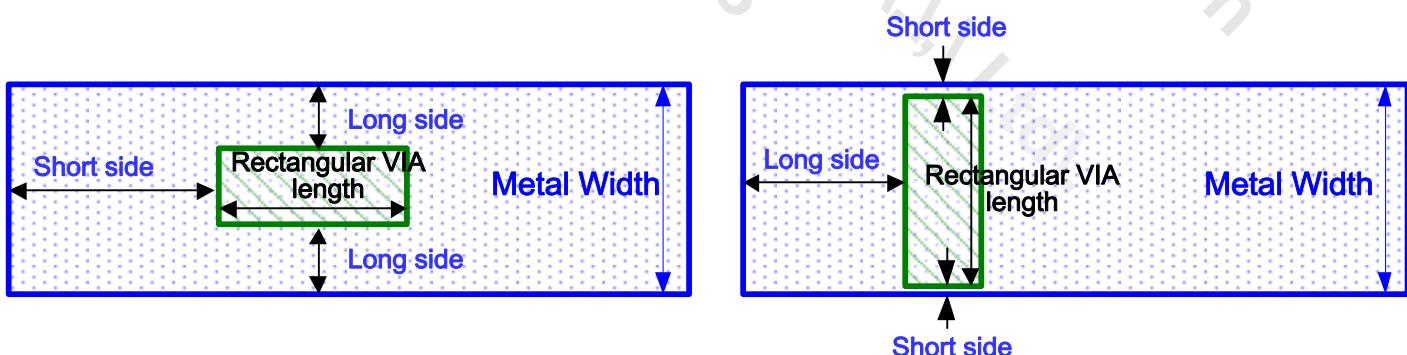
4.5.43.1 M1 Enclosure Rule Tabulation

RuleTable.M1.EN.31 (Enclosure of square VIA [width = 0.020 μm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
M1.EN.31.1.T	width ≤ 0.020 μm	0.0300 μm	0.0000 μm	
M1.EN.31.2.T	0.020 μm < width ≤ 0.022 μm	0.0300 μm	0.0010 μm	
M1.EN.31.3.T	0.022 μm < width ≤ 0.024 μm	0.0300 μm	0.0020 μm	BLK_M1
M1.EN.31.3.1.T	0.022 μm < width ≤ 0.024 μm	0.0130 μm	0.0020 μm	
M1.EN.31.4.T	0.024 μm < width < 0.036 μm	0.0260 μm	0.0070 μm	BLK_M1
M1.EN.31.4.1.T	0.024 μm < width < 0.036 μm	0.0150 μm	0.0030 μm	
M1.EN.31.5.T	0.036 μm ≤ width < 0.038 μm	0.0260 μm	0.0080 μm	
M1.EN.31.6.T	0.038 μm ≤ width < 0.040 μm	0.0260 μm	0.0090 μm	BLK_M1
M1.EN.31.6.1.T	0.038 μm ≤ width < 0.040 μm	0.0240 μm	0.0090 μm	
M1.EN.31.7.T	width = 0.040 μm	0.0260 μm	0.0100 μm	BLK_M1
M1.EN.31.7.1.T	width = 0.040 μm	0.0260 μm	0.0080 μm	
M1.EN.31.8.T	0.040 μm < width ≤ 0.045 μm	0.0250 μm	0.0105 μm	
M1.EN.31.9.T	0.045 μm < width ≤ 0.050 μm	0.0250 μm	0.0130 μm	
M1.EN.31.10.T	0.050 μm < width ≤ 0.055 μm	0.0250 μm	0.0155 μm	
M1.EN.31.11.T	0.055 μm < width < 0.060 μm	0.0250 μm	0.0180 μm	
M1.EN.31.12.T	width = 0.060 μm	0.0250 μm	0.0200 μm	BLK_M1
M1.EN.31.12.1.T	width = 0.060 μm	0.0100 μm	0.0200 μm	
M1.EN.31.13.T	0.060 μm < width < 0.070 μm	0.0250 μm	0.0205 μm	BLK_M1
M1.EN.31.13.1.T	0.060 μm < width < 0.070 μm	0.0250 μm	0.0140 μm	
M1.EN.31.14.T	0.070 μm ≤ width < 0.080 μm	0.0250 μm	0.0250 μm	
M1.EN.31.15.T	width = 0.080 μm	0.0250 μm	0.0300 μm	BLK_M1
M1.EN.31.15.1.T	width = 0.080 μm	0.0240 μm	0.0280 μm	
M1.EN.31.16.T	0.080 μm < width < 0.260 μm	0.0250 μm	0.0300 μm	BLK_M1
M1.EN.31.16.1.T	0.080 μm < width < 0.260 μm	0.0200 μm	0.0100 μm	
M1.EN.31.17.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	



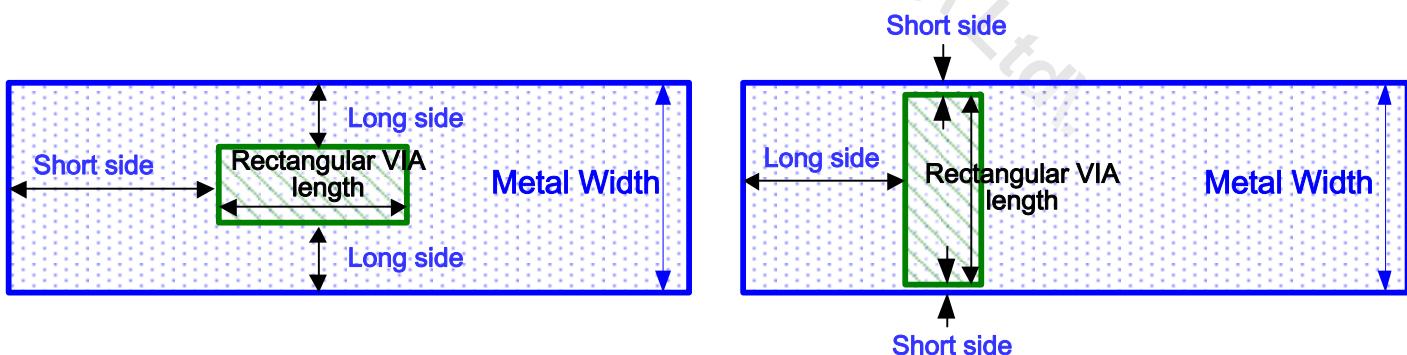
RuleTable.M1.EN.32 (Enclosure of rectangular VIA [length = 0.050 μm])

Rule Number	Metal Width	Short side	Long side	Exception
M1.EN.32.1.T	width ≤ 0.020 μm	0.0300 μm	0.0000 μm	
M1.EN.32.2.T	0.020 μm < width ≤ 0.022 μm	0.0300 μm	0.0010 μm	
M1.EN.32.3.T	0.022 μm < width ≤ 0.024 μm	0.0300 μm	0.0020 μm	
M1.EN.32.4.T	0.024 μm < width < 0.036 μm	0.0260 μm	0.0070 μm	BLK_M1
M1.EN.32.4.1.T	0.024 μm < width < 0.036 μm	0.0260 μm	0.0050 μm	
M1.EN.32.5.T	0.036 μm ≤ width < 0.038 μm	0.0260 μm	0.0080 μm	
M1.EN.32.6.T	0.038 μm ≤ width < 0.040 μm	0.0260 μm	0.0090 μm	
M1.EN.32.7.T	width = 0.040 μm	0.0260 μm	0.0100 μm	
M1.EN.32.8.T	0.040 μm < width ≤ 0.045 μm	0.0260 μm	0.0105 μm	
M1.EN.32.9.T	0.045 μm < width ≤ 0.050 μm	0.0260 μm	0.0130 μm	
M1.EN.32.10.T	0.050 μm < width ≤ 0.055 μm	0.0260 μm	0.0155 μm	
M1.EN.32.11.T	0.055 μm < width < 0.060 μm	0.0260 μm	0.0180 μm	
M1.EN.32.12.T	width = 0.060 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
M1.EN.32.13.T	0.060 μm < width < 0.070 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
M1.EN.32.14.T	0.070 μm ≤ width < 0.080 μm	0.0250/0.0100 μm	0.0250/0.0300 μm	
M1.EN.32.15.T	width = 0.080 μm	0.0150 μm	0.0300 μm	
M1.EN.32.16.T	0.080 μm < width < 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	
M1.EN.32.17.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	



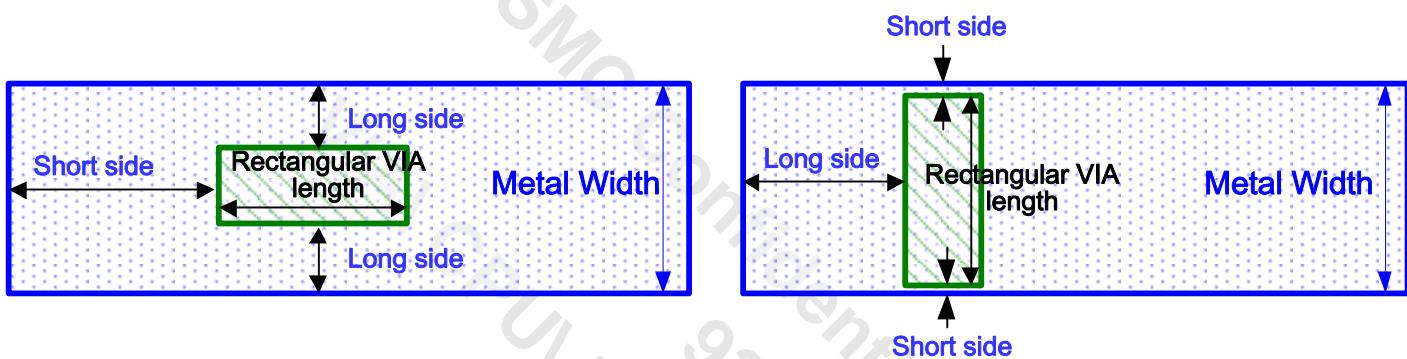
RuleTable.M1.EN.33 (Enclosure of rectangular VIA [length = 0.034 μm])

Rule Number	Metal Width	Short side	Long side	Exception
M1.EN.33.1.T	width ≤ 0.020 μm	0.0300 μm	0.0000 μm	
M1.EN.33.2.T	0.020 μm < width ≤ 0.022 μm	0.0300 μm	0.0010 μm	
M1.EN.33.3.T	0.022 μm < width ≤ 0.024 μm	0.0300 μm	0.0020 μm	BLK_M1
M1.EN.33.3.1.T	0.022 μm < width ≤ 0.024 μm	0.0230 μm	0.0020 μm	
M1.EN.33.4.T	0.024 μm < width < 0.036 μm	0.0260/0.0000 μm	0.0070/0.0400 μm	
M1.EN.33.5.T	0.036 μm ≤ width < 0.038 μm	0.0260/0.0010 μm	0.0080/0.0400 μm	
M1.EN.33.6.T	0.038 μm ≤ width < 0.040 μm	0.0260/0.0020 μm	0.0090/0.0400 μm	
M1.EN.33.7.T	width = 0.040 μm	0.0260/0.0030 μm	0.0100/0.0400 μm	
M1.EN.33.8.T	0.040 μm < width ≤ 0.045 μm	0.0260/0.0035 μm	0.0105/0.0400 μm	
M1.EN.33.9.T	0.045 μm < width ≤ 0.050 μm	0.0260/0.0060 μm	0.0130/0.0400 μm	
M1.EN.33.10.T	0.050 μm < width ≤ 0.055 μm	0.0260/0.0085 μm	0.0155/0.0400 μm	
M1.EN.33.11.T	0.055 μm < width < 0.060 μm	0.0260/0.0110 μm	0.0180/0.0400 μm	
M1.EN.33.12.T	width = 0.060 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
M1.EN.33.13.T	0.060 μm < width < 0.070 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	BLK_M1
M1.EN.33.13.1.T	0.060 μm < width < 0.070 μm	0.0250/0.0050 μm	0.0140/0.0250 μm	
M1.EN.33.14.T	0.070 μm ≤ width < 0.080 μm	0.0250/0.0100 μm	0.0250/0.0300 μm	
M1.EN.33.15.T	width = 0.080 μm	0.0150 μm	0.0300 μm	
M1.EN.33.16.T	0.080 μm < width < 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	
M1.EN.33.17.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	



RuleTable.M1.EN.34 (Enclosure of rectangular VIA [length = 0.060 μm])

Rule Number	Metal Width	Short side	Long side	Exception
M1.EN.34.1.T	width ≤ 0.020 μm	0.0300 μm	0.0000 μm	
M1.EN.34.2.T	0.020 μm < width ≤ 0.022 μm	0.0300 μm	0.0010 μm	
M1.EN.34.3.T	0.022 μm < width ≤ 0.024 μm	0.0300 μm	0.0020 μm	
M1.EN.34.4.T	0.024 μm < width < 0.036 μm	0.0260 μm	0.0070 μm	
M1.EN.34.5.T	0.036 μm ≤ width < 0.038 μm	0.0260 μm	0.0080 μm	



Rule No.	Description	Label	Op.	Rule
M1.EN.31.1.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [width ≤ 0.020 µm] for two opposite sides with the other two sides ≥ 0.0000 µm		≥	0.0300
M1.EN.31.2.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.020 µm < width ≤ 0.022 µm] for two opposite sides with the other two sides ≥ 0.0010 µm		≥	0.0300
M1.EN.31.3.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.022 µm < width ≤ 0.024 µm] for two opposite sides with the other two sides ≥ 0.0020 µm (Except BLK_M1)		≥	0.03
M1.EN.31.3.1.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.022 µm < width ≤ 0.024 µm] for two opposite sides with the other two sides ≥ 0.0020 µm		≥	0.0130
M1.EN.31.4.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.024 µm < width < 0.036 µm] for two opposite sides with the other two sides ≥ 0.0070 µm (Except BLK_M1)		≥	0.0260
M1.EN.31.4.1.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.024 µm < width < 0.036 µm] for two opposite sides with the other two sides ≥ 0.0030 µm		≥	0.0150
M1.EN.31.5.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.036 µm ≤ width < 0.038 µm] for two opposite sides with the other two sides ≥ 0.0080 µm		≥	0.0260
M1.EN.31.6.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.038 µm ≤ width < 0.040 µm] for two opposite sides with the other two sides ≥ 0.0090 µm (Except BLK_M1)		≥	0.0260
M1.EN.31.6.1.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.038 µm ≤ width < 0.040 µm] for two opposite sides with the other two sides ≥ 0.0090 µm		≥	0.0240
M1.EN.31.7.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [width = 0.040 µm] for two opposite sides with the other two sides ≥ 0.0100 µm (Except BLK_M1)		≥	0.0260
M1.EN.31.7.1.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [width = 0.040 µm] for two opposite sides with the other two sides ≥ 0.0080 µm		≥	0.0260
M1.EN.31.8.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.040 µm < width ≤ 0.045 µm] for two opposite sides with the other two sides ≥ 0.0105 µm		≥	0.0250
M1.EN.31.9.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.045 µm < width ≤ 0.050 µm] for two opposite sides with the other two sides ≥ 0.0130 µm		≥	0.0250
M1.EN.31.10.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.050 µm < width ≤ 0.055 µm] for two opposite sides with the other two sides ≥ 0.0155 µm		≥	0.0250
M1.EN.31.11.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.055 µm < width < 0.060 µm] for two opposite sides with the other two sides ≥ 0.0180 µm		≥	0.0250
M1.EN.31.12.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [width = 0.060 µm] for two opposite sides with the other two sides ≥ 0.0200 µm (Except BLK_M1)		≥	0.0250
M1.EN.31.12.1.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [width = 0.060 µm] for two opposite sides with the other two sides ≥ 0.0200 µm		≥	0.0100
M1.EN.31.13.T	Enclosure of square Lower_VIA [width = 0.020 µm] by M1 [0.060 µm < width < 0.070 µm] for two opposite sides with the other two sides ≥ 0.0205 µm (Except BLK_M1)		≥	0.0250

Rule No.	Description	Label	Op.	Rule
M1.EN.31.13.1.T	Enclosure of square Lower_VIA [width = 0.020 μm] by M1 [0.060 $\mu\text{m} < \text{width} < 0.070 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0140 \mu\text{m}$		\geq	0.0250
M1.EN.31.14.T	Enclosure of square Lower_VIA [width = 0.020 μm] by M1 [0.070 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0250
M1.EN.31.15.T	Enclosure of square Lower_VIA [width = 0.020 μm] by M1 [width = 0.080 μm] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$ (Except BLK_M1)		\geq	0.0250
M1.EN.31.15.1.T	Enclosure of square Lower_VIA [width = 0.020 μm] by M1 [width = 0.080 μm] for two opposite sides with the other two sides $\geq 0.0280 \mu\text{m}$		\geq	0.0240
M1.EN.31.16.T	Enclosure of square Lower_VIA [width = 0.020 μm] by M1 [0.080 $\mu\text{m} < \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$ (Except BLK_M1)		\geq	0.0250
M1.EN.31.16.1.T	Enclosure of square Lower_VIA [width = 0.020 μm] by M1 [0.080 $\mu\text{m} < \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$		\geq	0.0200
M1.EN.31.17.T	Enclosure of square Lower_VIA [width = 0.020 μm] by M1 [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
M1.EN.32.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [width $\leq 0.020 \mu\text{m}$] with the other two long sides $\geq 0.0000 \mu\text{m}$		\geq	0.0300
M1.EN.32.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.020 $\mu\text{m} < \text{width} \leq 0.022 \mu\text{m}$] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
M1.EN.32.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.022 $\mu\text{m} < \text{width} \leq 0.024 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
M1.EN.32.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.024 $\mu\text{m} < \text{width} < 0.036 \mu\text{m}$] with the other two long sides $\geq 0.0070 \mu\text{m}$ (Except BLK_M1)		\geq	0.0260
M1.EN.32.4.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.024 $\mu\text{m} < \text{width} < 0.036 \mu\text{m}$] with the other two long sides $\geq 0.0050 \mu\text{m}$		\geq	0.0260
M1.EN.32.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.036 $\mu\text{m} \leq \text{width} < 0.038 \mu\text{m}$] with the other two long sides $\geq 0.0080 \mu\text{m}$		\geq	0.0260
M1.EN.32.6.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.038 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0090 \mu\text{m}$		\geq	0.0260
M1.EN.32.7.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [width = 0.040 μm] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0260
M1.EN.32.8.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.040 $\mu\text{m} < \text{width} \leq 0.045 \mu\text{m}$] with the other two long sides $\geq 0.0105 \mu\text{m}$		\geq	0.0260
M1.EN.32.9.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.045 $\mu\text{m} < \text{width} \leq 0.050 \mu\text{m}$] with the other two long sides $\geq 0.0130 \mu\text{m}$		\geq	0.0260
M1.EN.32.10.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.050 $\mu\text{m} < \text{width} \leq 0.055 \mu\text{m}$] with the other two long sides $\geq 0.0155 \mu\text{m}$		\geq	0.0260
M1.EN.32.11.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.055 $\mu\text{m} < \text{width} < 0.060 \mu\text{m}$] with the other two long sides $\geq 0.0180 \mu\text{m}$		\geq	0.0260

Rule No.	Description	Label	Op.	Rule
M1.EN.32.12.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [width = 0.060 μm] with the other two long sides ≥ 0.0200/0.0250 μm		≥	0.0250/0.0050
M1.EN.32.13.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.060 μm < width < 0.070 μm] with the other two long sides ≥ 0.0200/0.0250 μm		≥	0.0250/0.0050
M1.EN.32.14.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.070 μm ≤ width < 0.080 μm] with the other two long sides ≥ 0.0250/0.0300 μm		≥	0.0250/0.0100
M1.EN.32.15.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [width = 0.080 μm] with the other two long sides ≥ 0.0300 μm		≥	0.0150
M1.EN.32.16.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [0.080 μm < width < 0.260 μm] with the other two long sides ≥ 0.0300/0.0250 μm		≥	0.0250/0.0300
M1.EN.32.17.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by M1 [width ≥ 0.260 μm] with the other two long sides ≥ 0.0250 μm		≥	0.0600
M1.EN.33.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [width ≤ 0.020 μm] with the other two long sides ≥ 0.0000 μm		≥	0.0300
M1.EN.33.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.020 μm < width ≤ 0.022 μm] with the other two long sides ≥ 0.0010 μm		≥	0.0300
M1.EN.33.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.022 μm < width ≤ 0.024 μm] with the other two long sides ≥ 0.0020 μm (Except BLK_M1)		≥	0.0300
M1.EN.33.3.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.022 μm < width ≤ 0.024 μm] with the other two long sides ≥ 0.0020 μm		≥	0.0230
M1.EN.33.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.024 μm < width < 0.036 μm] with the other two long sides ≥ 0.0070/0.0400 μm		≥	0.0260/0.0000
M1.EN.33.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.036 μm ≤ width < 0.038 μm] with the other two long sides ≥ 0.0080/0.0400 μm		≥	0.0260/0.0010
M1.EN.33.6.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.038 μm ≤ width < 0.040 μm] with the other two long sides ≥ 0.0090/0.0400 μm		≥	0.0260/0.0020
M1.EN.33.7.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [width = 0.040 μm] with the other two long sides ≥ 0.0100/0.0400 μm		≥	0.0260/0.0030
M1.EN.33.8.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.040 μm < width ≤ 0.045 μm] with the other two long sides ≥ 0.0105/0.0400 μm		≥	0.0260/0.0035
M1.EN.33.9.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.045 μm < width ≤ 0.050 μm] with the other two long sides ≥ 0.0130/0.0400 μm		≥	0.0260/0.0060
M1.EN.33.10.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.050 μm < width ≤ 0.055 μm] with the other two long sides ≥ 0.0155/0.0400 μm		≥	0.0260/0.0085
M1.EN.33.11.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.055 μm < width < 0.060 μm] with the other two long sides ≥ 0.0180/0.0400 μm		≥	0.0260/0.0110
M1.EN.33.12.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [width = 0.060 μm] with the other two long sides ≥ 0.0200/0.0250 μm		≥	0.0250/0.0050
M1.EN.33.13.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.060 μm < width < 0.070 μm] with the other two long sides ≥ 0.0200/0.0250 μm (Except BLK_M1)		≥	0.0250/0.0050

Rule No.	Description	Label	Op.	Rule
M1.EN.33.13.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.060 μm < width < 0.070 μm] with the other two long sides \geq 0.0140/0.0250 μm		\geq	0.0250/0.0050
M1.EN.33.14.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.070 μm \leq width < 0.080 μm] with the other two long sides \geq 0.0250/0.0300 μm		\geq	0.0250/0.0100
M1.EN.33.15.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [width = 0.080 μm] with the other two long sides \geq 0.0300 μm		\geq	0.0150
M1.EN.33.16.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [0.080 μm < width < 0.260 μm] with the other two long sides \geq 0.0300/0.0250 μm		\geq	0.0250/0.0300
M1.EN.33.17.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by M1 [width \geq 0.260 μm] with the other two long sides \geq 0.0250 μm		\geq	0.0600
M1.EN.34.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.060 μm] by M1 [width \leq 0.020 μm] with the other two long sides \geq 0.0000 μm		\geq	0.0300
M1.EN.34.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.060 μm] by M1 [0.020 μm < width \leq 0.022 μm] with the other two long sides \geq 0.0010 μm		\geq	0.0300
M1.EN.34.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.060 μm] by M1 [0.022 μm < width \leq 0.024 μm] with the other two long sides \geq 0.0020 μm		\geq	0.0300
M1.EN.34.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.060 μm] by M1 [0.024 μm < width < 0.036 μm] with the other two long sides \geq 0.0070 μm		\geq	0.0260
M1.EN.34.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.060 μm] by M1 [0.036 μm \leq width < 0.038 μm] with the other two long sides \geq 0.0080 μm		\geq	0.0260

4.5.44 VIAxs Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.
VIA1xs (CAD layer: 51;400, or VIA1) is used for VIA1.

Rule No.	Description	Label	Op.	Rule
VIAxs.W.1	Width (Except SEALRING_ALL)	W1	=	0.0200
VIAxs.W.2	Width of VIAxs bar in SEALRING_ALL	W2	=	0.1400
VIAxs.S.1	Space (Except SEALRING_ALL)	S1	\geq	0.0265
VIAxs.S.3	Space of the short side of rectangular VIA1 to M1 [PRL > -0.020 μm , different net] (Except following conditions: 1. VIA1 space inside {VIA1 [INSIDE BLK_M2] SIZING 0.045 μm })	S3	\geq	0.0450
VIAxs.S.8	Space to VIAxs or VIAxs-1 or VIA0 [maximum delta V > 0.96V]	S8	\geq	0.0620
VIAxs.S.8.1	Space to VIAxs or VIAxs-1 or VIA0 [maximum delta V > 1.32V] (1.2V + 10%)	S8	\geq	0.0640
VIAxs.S.8.2	Space to VIAxs or VIAxs-1 or VIA0 [maximum delta V > 1.65V] (1.5V + 10%)	S8	\geq	0.0700
VIAxs.S.8.3	Space to VIAxs or VIAxs-1 or VIA0 [maximum delta V > 1.98V] (1.8V + 10%)	S8	\geq	0.0820
VIAxs.S.8.4	Space to VIAxs or VIAxs-1 or VIA0 [maximum delta V > 2.75V] (2.5V + 10%)	S8	\geq	0.0870
VIAxs.S.9	Space to {SRM (50;0) OR SRAMDMY (186;0)} ({VIAxs CUT {SRM (50;0) OR SRAMDMY (186;0)}} is not allowed)	S9	\geq	0.0840
VIAxs.S.9.1	Space of short side of rectangular VIAxs to {SRM (50;0) OR SRAMDMY (186;0)} [PRL > -0.044 μm]	S9A	\geq	0.1340
VIAxs.S.11	Space of the long side of rectangular VIAxs [PRL > 0 μm (L1), with Mxs+1 in between, and Mxs+1 width < 0.024 μm]	S11	\geq	0.0680
VIAxs.S.12	Space of Checked_VIAxs horizontal edge [PRL > -0.018 μm] Definition of Checked_VIAxs: VIAxs space to Mxs+1 \leq 0.022 μm in Mxs+1 MINP direction [PRL > -0.080 μm]	S12	\geq	0.0450
VIAxs.S.12.1	Space of Checked_VIAxs vertical edge [PRL > -0.020 μm] Definition of Checked_VIAxs: VIAxs space to {M1 OR M1_VIRT} \leq 0.022 μm in M1 MINP direction [PRL > -0.080 μm]	S12	\geq	0.0450
VIAxs.S.31.1.T	Space of VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μm]	S31A	\geq	0.0370
VIAxs.S.31.1.1	Space of VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] in horizontal direction [different net, PRL > -0.020 μm]	S31A1	\geq	0.0440
VIAxs.S.31.2.T	Space of VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] in vertical direction [PRL > -0.018 μm]	S31BT	\geq	0.0370
VIAxs.S.31.2.1	Space of VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] in vertical direction [different net, PRL > -0.018 μm]	S31B1	\geq	0.0440
VIAxs.S.31.3.T	Space of VIAxs [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 μm] (Except FB_9, FB_8)	S31CT	\geq	0.0740

Rule No.	Description	Label	Op.	Rule
VIAxs.S.31.4.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S31DT	≥	0.0490
VIAxs.S.31.5.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S31ET	≥	0.0490
VIAxs.S.31.6.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S31FT	≥	0.0490
VIAxs.S.31.7.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S31GT	≥	0.0740
VIAxs.S.31.8.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S31HT	≥	0.0490
VIAxs.S.31.9.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S31IT	≥	0.0740
VIAxs.S.31.10.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S31JT	≥	0.0490
VIAxs.S.31.11.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S31KT	≥	0.0490
VIAxs.S.31.12.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S31LT	≥	0.0490
VIAxs.S.31.13.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S31MT	≥	0.0740
VIAxs.S.31.14.T	Space of VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S31NT	≥	0.0490
VIAxs.S.32.1.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32AT	≥	0.0740
VIAxs.S.32.2.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32BT	≥	0.0490
VIAxs.S.32.3.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32CT	≥	0.0490

Rule No.	Description	Label	Op.	Rule
VIAxs.S.32.4.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32DT	≥	0.0740
VIAxs.S.32.5.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32ET	≥	0.0490
VIAxs.S.32.6.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32FT	≥	0.0490
VIAxs.S.32.7.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32GT	≥	0.0740
VIAxs.S.32.8.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32HT	≥	0.0740
VIAxs.S.32.9.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32IT	≥	0.0490
VIAxs.S.32.10.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32JT	≥	0.0740
VIAxs.S.32.11.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32KT	≥	0.0490
VIAxs.S.32.12.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32LT	≥	0.0490
VIAxs.S.32.13.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32MT	≥	0.0740
VIAxs.S.32.14.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S32NT	≥	0.0740
VIAxs.S.32.15.T	Space of VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S32OT	≥	0.0490
VIAxs.S.33.1.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S33AT	≥	0.0490
VIAxs.S.33.2.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S33BT	≥	0.0740

Rule No.	Description	Label	Op.	Rule
VIAxs.S.33.3.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S33CT	≥	0.0490
VIAxs.S.33.4.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S33DT	≥	0.0740
VIAxs.S.33.5.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S33ET	≥	0.0740
VIAxs.S.33.6.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S33FT	≥	0.0490
VIAxs.S.33.7.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S33GT	≥	0.0490
VIAxs.S.33.8.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S33HT	≥	0.0740
VIAxs.S.33.9.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S33IT	≥	0.0490
VIAxs.S.33.10.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S33JT	≥	0.0740
VIAxs.S.33.11.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S33KT	≥	0.0740
VIAxs.S.33.12.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S33LT	≥	0.0490
VIAxs.S.33.13.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S33MT	≥	0.0490
VIAxs.S.33.14.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S33NT	≥	0.0740
VIAxs.S.33.15.T	Space of VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S33OT	≥	0.0490
VIAxs.S.34.1.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34AT	≥	0.0740

Rule No.	Description	Label	Op.	Rule
VIAxs.S.34.2.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34BT	≥	0.0490
VIAxs.S.34.3.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34CT	≥	0.0490
VIAxs.S.34.4.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34DT	≥	0.0740
VIAxs.S.34.5.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34ET	≥	0.0490
VIAxs.S.34.6.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34FT	≥	0.0490
VIAxs.S.34.7.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34GT	≥	0.0740
VIAxs.S.34.8.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34HT	≥	0.0740
VIAxs.S.34.9.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34IT	≥	0.0490
VIAxs.S.34.10.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34JT	≥	0.0740
VIAxs.S.34.11.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34KT	≥	0.0490
VIAxs.S.34.12.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34LT	≥	0.0490
VIAxs.S.34.13.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34MT	≥	0.0740
VIAxs.S.34.14.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S34NT	≥	0.0740
VIAxs.S.34.15.T	Space of VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S34OT	≥	0.0490

Rule No.	Description	Label	Op.	Rule
VIAxs.S.35.1.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S35AT	≥	0.0490
VIAxs.S.35.2.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S35BT	≥	0.0740
VIAxs.S.35.3.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S35CT	≥	0.0490
VIAxs.S.35.4.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S35DT	≥	0.0740
VIAxs.S.35.5.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S35ET	≥	0.0740
VIAxs.S.35.6.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.034/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S35FT	≥	0.0490
VIAxs.S.35.7.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S35GT	≥	0.0490
VIAxs.S.35.8.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S35HT	≥	0.0740
VIAxs.S.35.9.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.034 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S35IT	≥	0.0490
VIAxs.S.35.10.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S35JT	≥	0.0740
VIAxs.S.35.11.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] in vertical direction [PRL > -0.020 µm] (Except FB_9, FB_8)	S35KT	≥	0.0740
VIAxs.S.35.12.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.050/0.020 µm in horizontal/vertical direction] (Except FB_9, FB_8)	S35LT	≥	0.0490
VIAxs.S.35.13.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in horizontal direction [PRL > -0.026 µm] (Except FB_9, FB_8)	S35MT	≥	0.0490
VIAxs.S.35.14.T	Space of VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 µm in horizontal/vertical direction] in vertical direction [PRL > -0.018 µm] (Except FB_9, FB_8)	S35NT	≥	0.0740

Rule No.	Description	Label	Op.	Rule
VIAxs.S.35.15.T	Space of VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] to VIAxs [edge length = 0.020/0.050 μm in horizontal/vertical direction] (Except FB_9, FB_8)	S35OT	≥	0.0490
VIAxs.EN.0	1. Enclosure of square VIAxs [width = 0.020 μm] is defined by RuleTable.VIAxs.EN.31 in the subsection 2. Enclosure of rectangular VIAxs [length = 0.034 μm] is defined by RuleTable.VIAxs.EN.32 in the subsection 3. Enclosure of rectangular VIAxs [length = 0.050 μm] is defined by RuleTable.VIAxs.EN.33 in the subsection			
VIAxs.EN.1.8	Enclosure of square VIAxs by M1 [0.080 μm ≤ width < 0.260 μm] with the other two sides ≥ 0.030 μm (Except following conditions: 1. M1 [width = 0.120 μm] enclosure of square VIAxs array) Definition of square VIAxs array follows VIAxs.EN.19	EN1H	≥	0.0200
VIAxs.EN.16.10	Checked_VIAxs_Edge1 enclosure by M1 (31;420) in M1 MINP direction (Except following conditions: 1. VIA1 inside BLK_M2) Definition of Checked_VIAxs: VIAxs INTERACT Mxs width > 0.040 μm Definition of Checked_VIAxs_Edge1: 1. Checked_VIAxs edge space to M1 (31;420) < 0.040 μm with PRL > - 0.100 μm in M1 MINP direction	EN16J	≥	0.0010
VIAxs.EN.16.10.1	Checked_VIAxs_Edge2 enclosure by M1 (31;420) in M1 MINP direction (Except following conditions: 1. VIA1 inside BLK_M2) Definition of Checked_VIAxs: VIAxs INTERACT Mxs width > 0.040 μm Definition of Checked_VIAxs_Edge2: 1. Checked_VIAxs edge space to M1 (31;420) < 0.040 μm with PRL > - 0.100 μm in M1 MINP direction, and 2. Checked_VIAxs edge space to VIA0 < 0.026 μm [PRL > 0, different net]	EN16J	≥	0.0020
VIAxs.EN.19	Square VIAxs array enclosure by M1 [width = 0.120 μm] for two opposite sides with the other two sides [Square VIAxs array edge length = 0.020 μm] ≥ 0.018 μm Definition of square VIAxs array: VIAxs space = 0.044 μm [PRL = 0.020 μm] in M1 MINP direction	EN19	≥	0.0300
VIAxs.EN.21.10	Short side enclosure of rectangular VIAxs by M1 edge [length = 0.080 μm, M1 width = 0.080 μm]	EN21D	≥	0.0250
VIAxs.L.1.1	Length of VIAxs [width = 0.020 μm]	L1A	=	0.0200, 0.0340, 0.0500
VIAxs.R.0	45-degree VIAxs is not allowed			
VIAxs.R.2	Redundant via requirement must follow RuleTable.VIAxs.R.2 of VIAxs numbers and space (S1) for M1 and Mxs connection. [One of M1/Mxs has width and length (W1) > 0.160 μm]. (Except following conditions: 1. VIA bar)			
VIAxs.R.2.1	Redundant via requirement must follow RuleTable.VIAxs.R.2.1 of VIAxs numbers and space (S1) for M1 and Mxs connection. [One of M1/Mxs has width and length (W1) > 0.300 μm]. (Except following conditions: 1. VIA bar)			

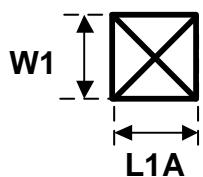
Rule No.	Description	Label	Op.	Rule
VIAxs.R.3	Redundant via requirement must follow RuleTable.VIAxs.R.3 of VIAxs numbers and space (S1) for M1 and Mxs connection. [One of M1/Mxs has width and length (W1) > 0.412 μm]. (Except following conditions: 1. VIA bar)			
VIAxs.R.7	VIAxs must be fully covered by {M1 AND Mxs}			
VIAxs.R.9®	Recommended maximum consecutive stacked VIAxs layer, which has only one via for each VIAxs layer to avoid high R_c		\leq	4
VIAxs.R.10	Overlap MetalFuse_B1 (156;8) is not allowed			
VIAxs.R.13	Maximum area ratio of M1 to upper VIAxs in the same net [connects to gate with area > 10700 μm^2 , and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = $(2.5 \times W_{dxLd})$ for \geq 2-fin device		\leq	350000
VIAxs.R.13.2	Maximum area ratio of I/O gate to single layer VIAxs in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area $\geq 0.25 \mu\text{m}^2$) Definition: Gate area = $(2.5 \times W_{dxLd})$ for \geq 2-fin device		\leq	300000
VIAxs.R.14	Maximum delta V > 3.63V is not allowed. DRC searching range of VIAxs space to VIAxs is < 0.405 μm			
VIAxs.R.15	VIAxs [width/length = 0.020/0.034 μm] must be horizontal direction			
VIAxs.R.19	Isolated VIAxs is not allowed. (Except SEALRING_ALL) DRC flags VIAxs without neighboring {VIAxs OR DVIAxs} distance $\leq 4 \mu\text{m}$			
VIAxs.R.21	VIAxs interact VIAxs_Empty_Space_100 is not allowed in chip level (Except following conditions: 1. INDDMY, SEALRING_ALL for VIAxs_Empty_Space_100) Definition of VIAxs_Empty_Space_100: {CHIP NOT {VIAxs OR DVIAxs}} SIZING down/up 50 μm			
VIAxs.R.21.1	VIAxs interact VIAxs_Empty_Space_50 is not allowed in cell level (Except following conditions: 1. INDDMY for VIAxs_Empty_Space_50) Definition of VIAxs_Empty_Space_50: {CHIP NOT {VIAxs OR DVIAxs}} SIZING down/up 25 μm			
VIAxs.R.22	VIAxs space to 4 or more VIAxs < 0.030 μm is not allowed			

Table Notes:

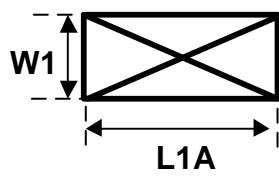
- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

VIAxes

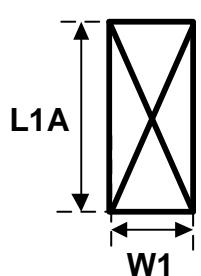
Square VIAxes



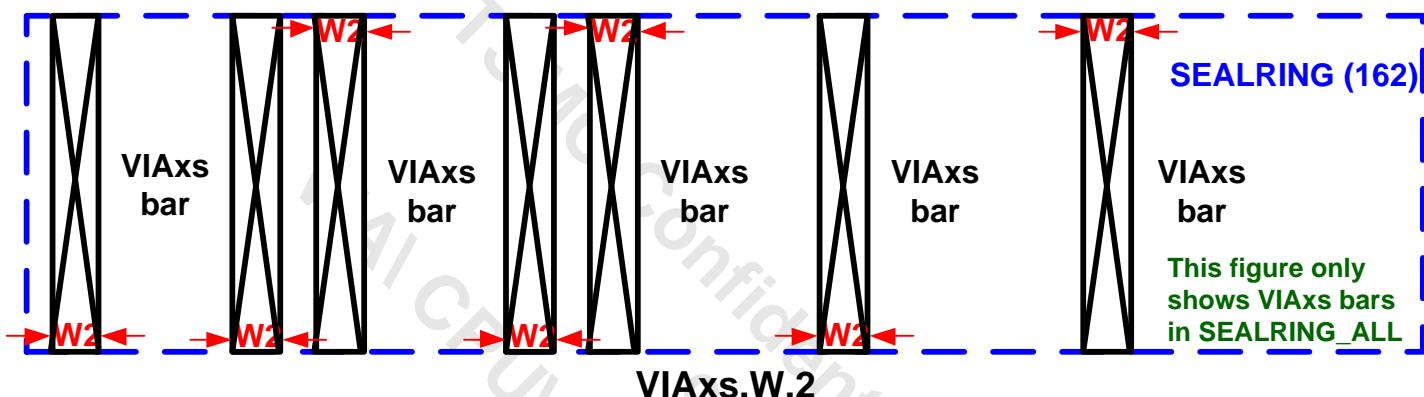
rectangular VIAxes



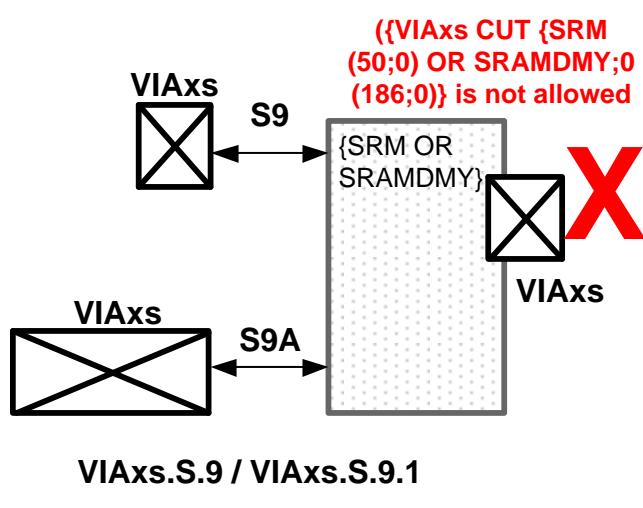
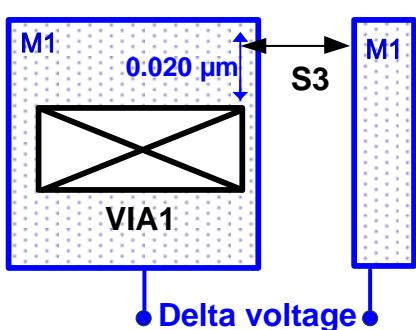
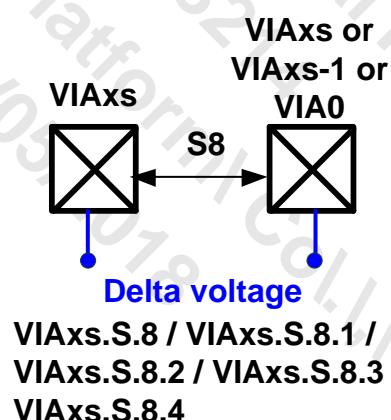
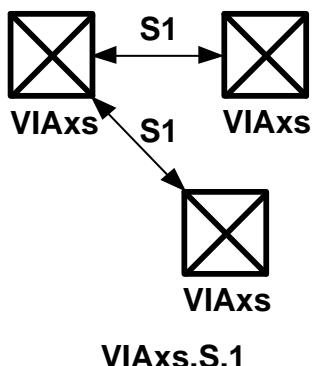
rectangular VIAxes

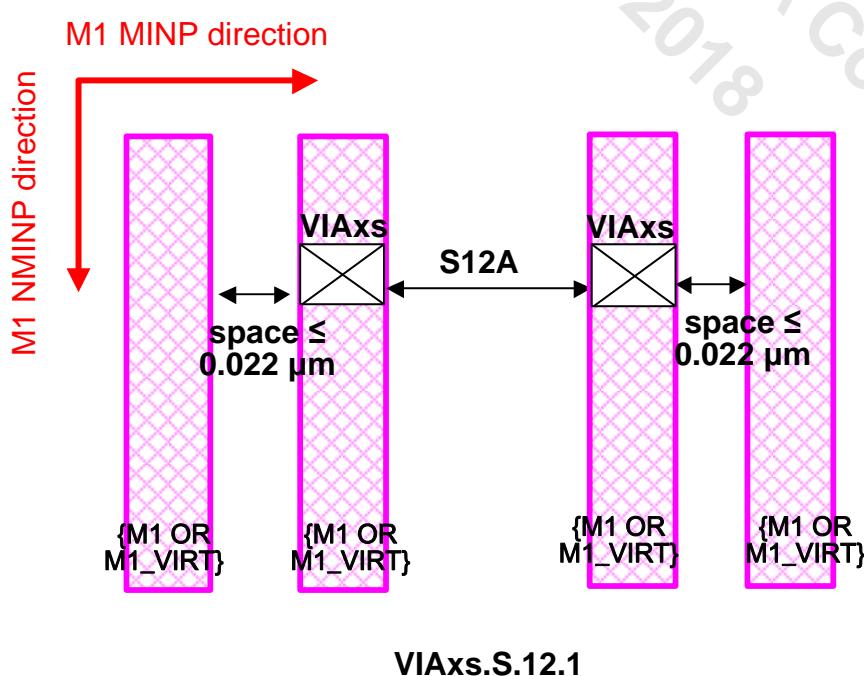
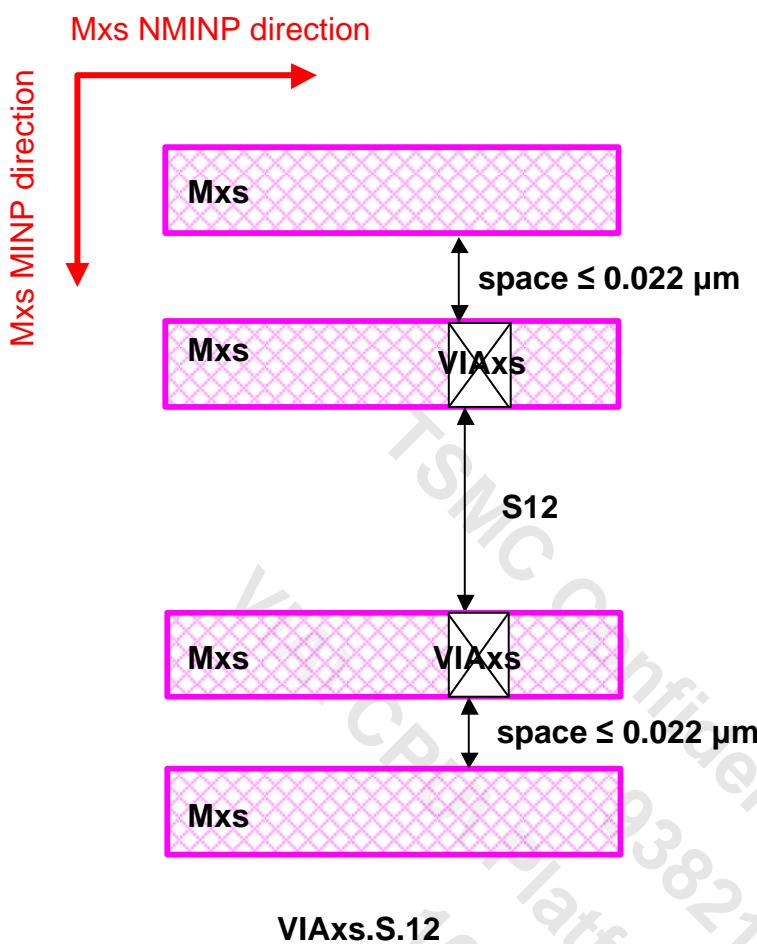


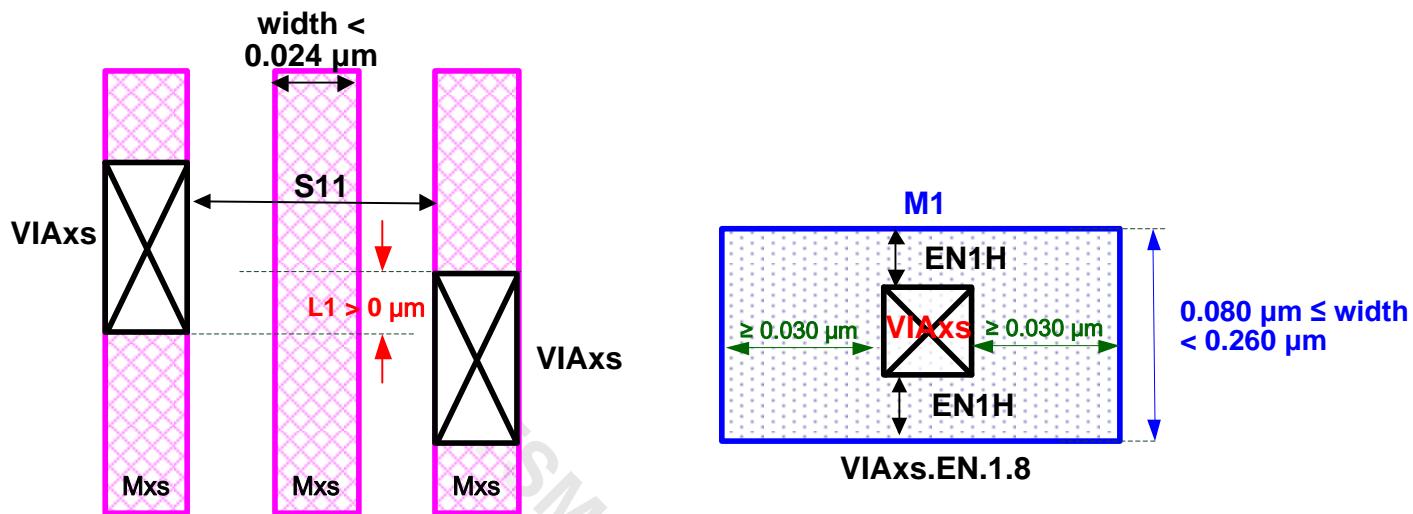
VIAxes.W.1 / VIAxes.L.1.1



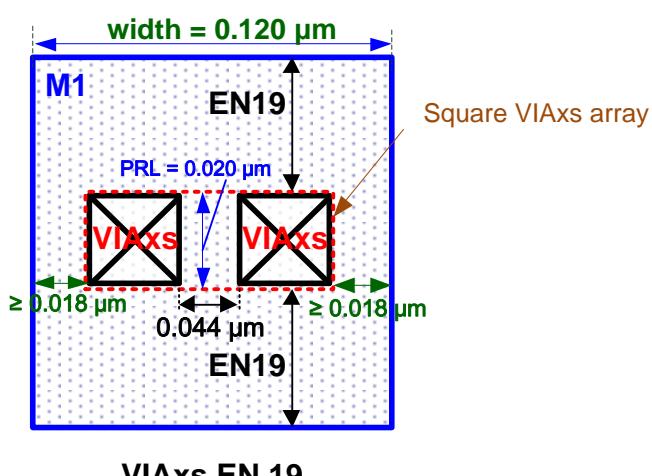
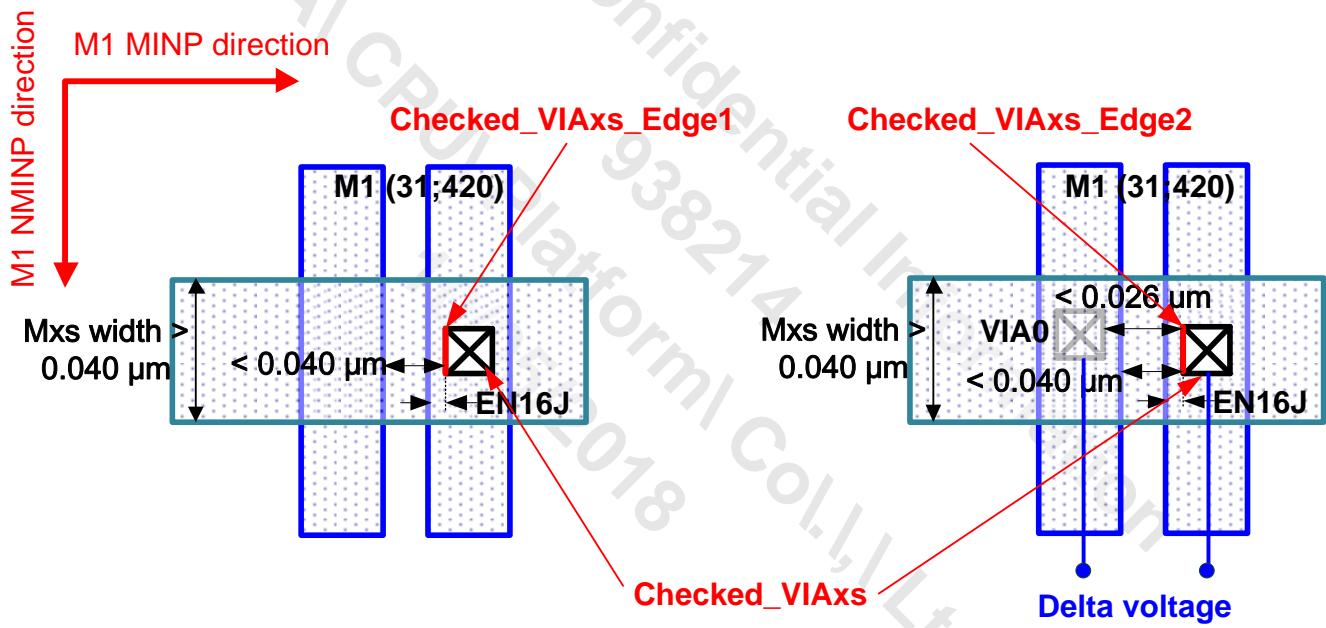
VIAxes.W.2

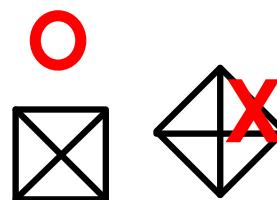
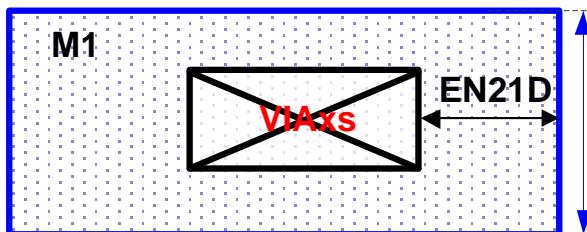






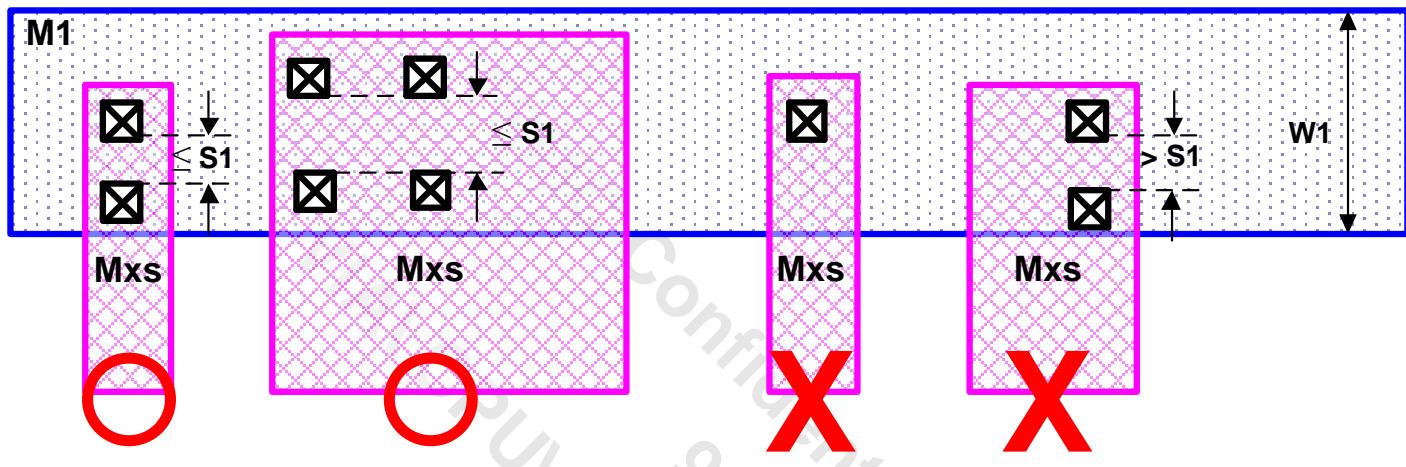
VIAxS.S.11





45-degree VIAXs is not allowed.

VIAXs.EN.21.10

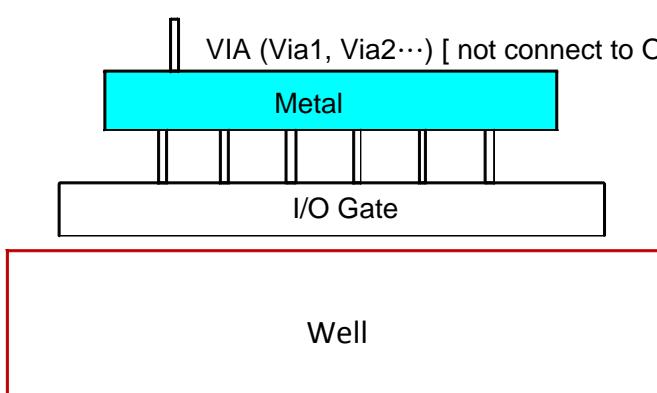
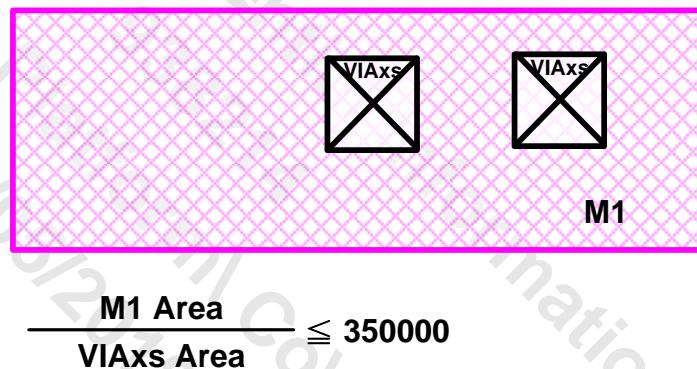
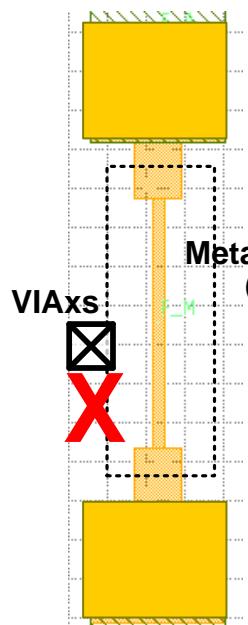
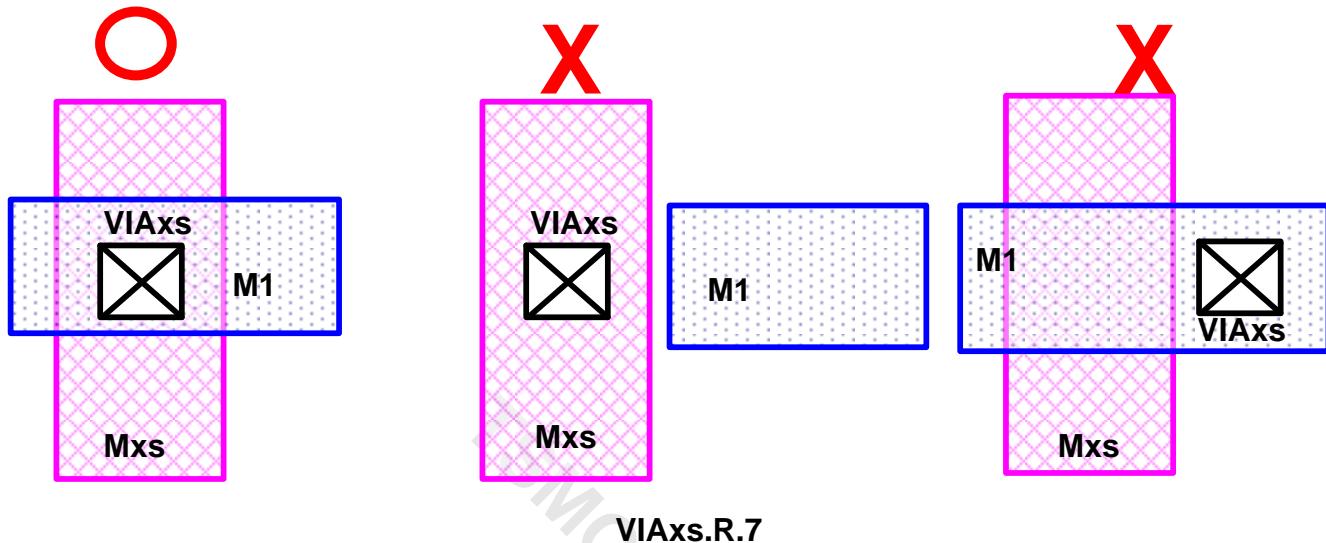


VIAXs.R.2 / VIAXs.R.2.1 / VIAXs.R.3

RuleTable.VIAXs.R.2	0.160 μm < W1 ≤ 0.300 μm							
VIAXs space (S1) (μm)	0.070 ≤ S1 ≤ 0.160				0.160 < S1 ≤ 0.400			
Rectangular VIAXs [width/length = 0.020/0.050 μm] (#)	0	1			0	1	2	
{Square VIAXs [width = 0.020 μm] OR rectangular VIAXs [width/length = 0.020/0.034 μm]} (#)	≥ 2	≥ 0			≥ 4	≥ 2	≥ 0	

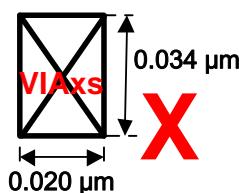
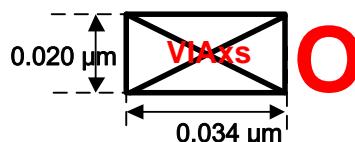
RuleTable.VIAXs.R.2.1	0.300 μm < W1 ≤ 0.412 μm							
VIAXs space (S1) (μm)	0.070 ≤ S1 ≤ 0.160				0.160 < S1 ≤ 0.400			
Rectangular VIAXs [width/length = 0.020/0.050 μm] (#)	0	1	2		0	1	2	3
{Square VIAXs [width = 0.020 μm] OR rectangular VIAXs [width/length = 0.020/0.034 μm]} (#)	≥ 3	≥ 1	≥ 0		≥ 6	≥ 4	≥ 2	≥ 0

RuleTable.VIAXs.R.3	W1 > 0.412 μm								
VIAXs space (S1) (μm)	0.070 ≤ S1 ≤ 0.160				0.160 < S1 ≤ 0.400				
Rectangular VIAXs [width/length = 0.020/0.050 μm] (#)	0	1	2		0	1	2	3	4
{Square VIAXs [width = 0.020 μm] OR rectangular VIAXs [width/length = 0.020/0.034 μm]} (#)	≥ 4	≥ 2	≥ 0		≥ 9	≥ 7	≥ 5	≥ 3	≥ 1

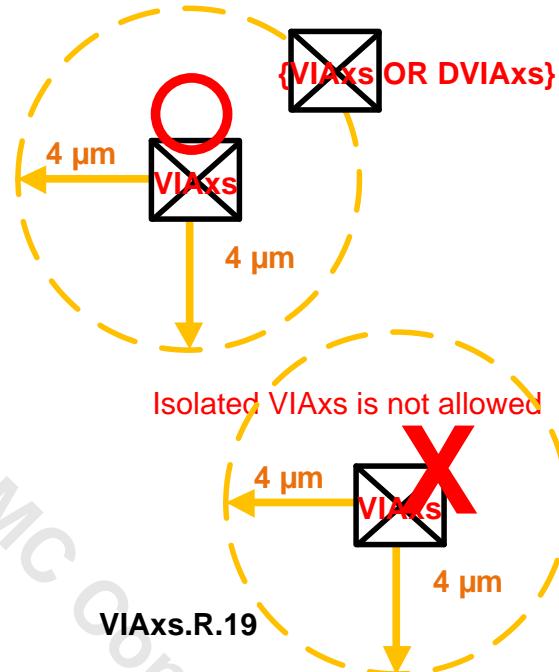


$$\frac{\text{IO Gate Area}}{\text{VIAxs Area}} \leq 300000$$

VIAxs.R.13.2

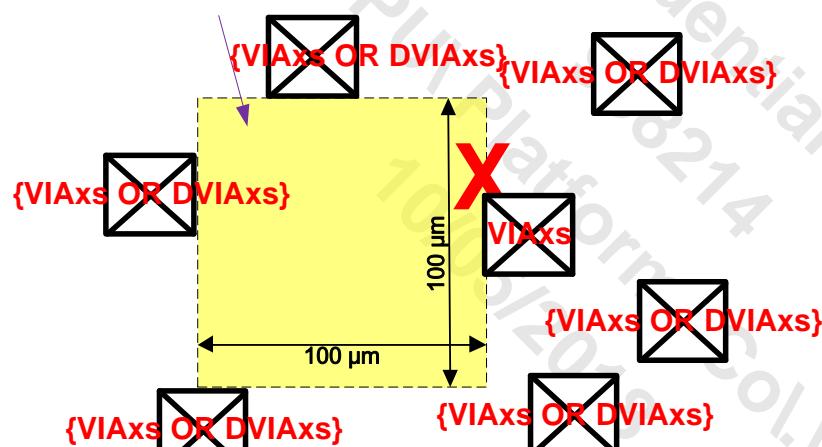


VIAxS.R.15



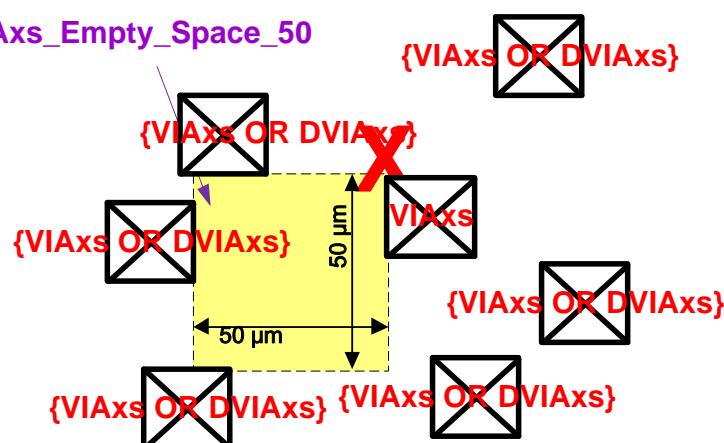
VIAxS.R.19

VIAxS_Empty_Space_100



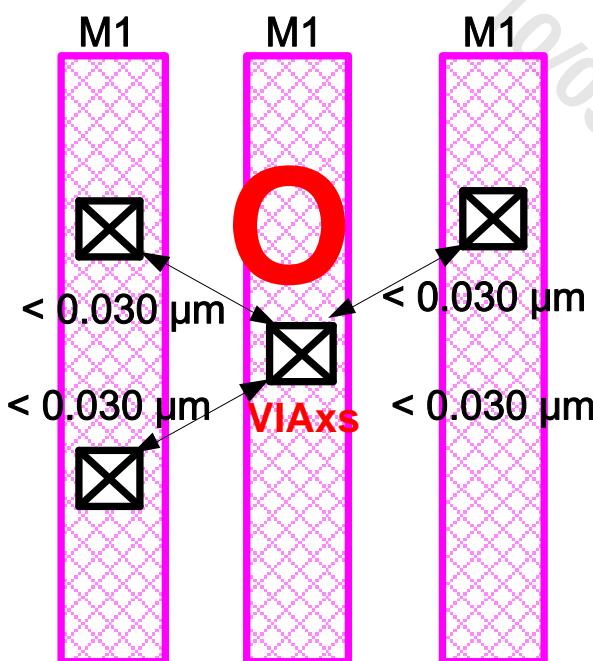
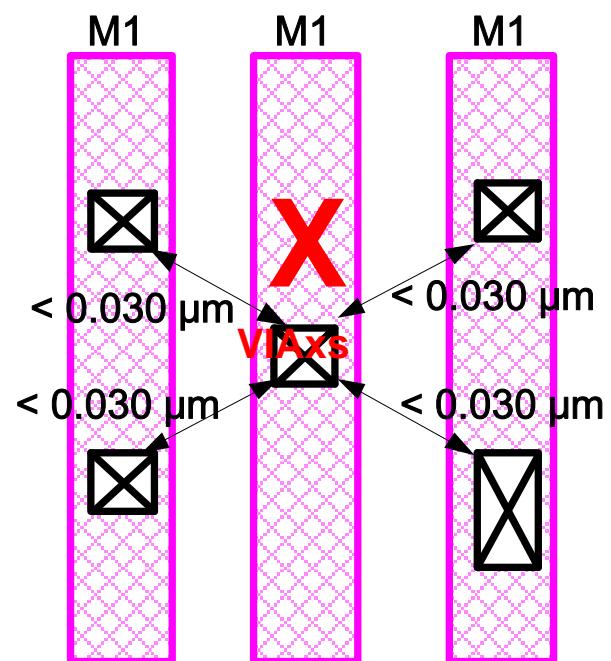
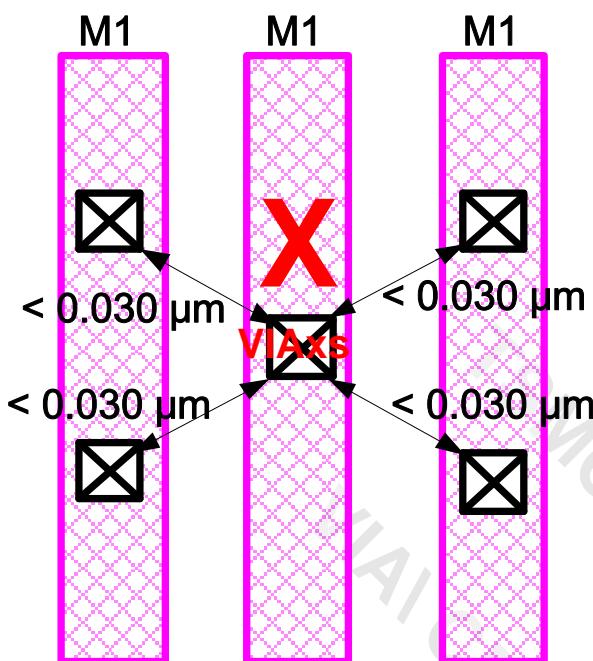
VIAxS.R.21

VIAxS_Empty_Space_50



VIAxS.R.21.1

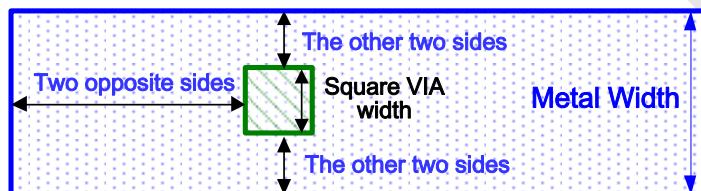
VIAxs space to 4 or more VIAxs < 0.030 μm is not allowed



VIAxs.R.22

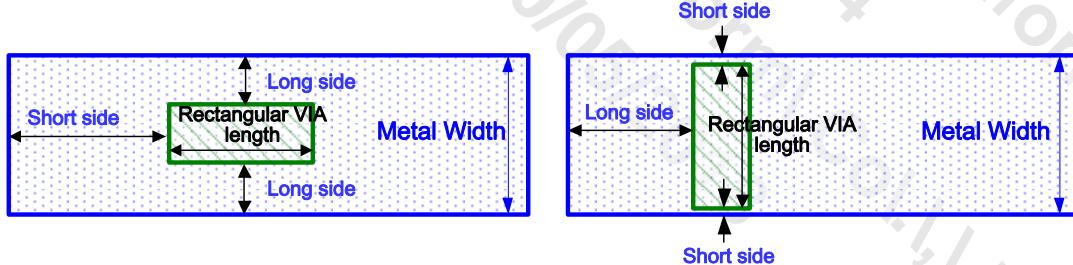
4.5.44.1 VIAxs Enclosure Rule Tabulation

RuleTable.VIAxs.EN.31 (Enclosure of square VIA [width = 0.020 μm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAxs.EN.31.1.T	width ≤ 0.020 μm	0.0300 μm	0.0000 μm	
VIAxs.EN.31.2.T	0.020 μm < width ≤ 0.022 μm	0.0300 μm	0.0010 μm	
VIAxs.EN.31.3.T	0.022 μm < width ≤ 0.024 μm	0.0300 μm	0.0020 μm	BLK_WB
VIAxs.EN.31.3.1.T	0.022 μm < width ≤ 0.024 μm	0.0120 μm	0.0020 μm	
VIAxs.EN.31.4.T	0.024 μm < width < 0.036 μm	0.0260 μm	0.0070 μm	BLK_WB
VIAxs.EN.31.4.1.T	0.024 μm < width < 0.036 μm	0.0150 μm	0.0040 μm	
VIAxs.EN.31.5.T	0.036 μm ≤ width < 0.038 μm	0.0260 μm	0.0080 μm	
VIAxs.EN.31.6.T	0.038 μm ≤ width < 0.040 μm	0.0260 μm	0.0090 μm	
VIAxs.EN.31.7.T	0.040 μm ≤ width < 0.045 μm	0.0250 μm	0.0100 μm	
VIAxs.EN.31.8.T	0.045 μm ≤ width < 0.050 μm	0.0250 μm	0.0125 μm	
VIAxs.EN.31.9.T	0.050 μm ≤ width < 0.055 μm	0.0250 μm	0.0150 μm	
VIAxs.EN.31.10.T	0.055 μm ≤ width < 0.060 μm	0.0250 μm	0.0175 μm	
VIAxs.EN.31.11.T	0.060 μm ≤ width < 0.070 μm	0.0250 μm	0.0200 μm	BLK_WB
VIAxs.EN.31.11.1.T	0.060 μm ≤ width < 0.070 μm	0.0200 μm	0.0150 μm	
VIAxs.EN.31.12.T	0.070 μm ≤ width < 0.080 μm	0.0250 μm	0.0250 μm	
VIAxs.EN.31.13.T	0.080 μm ≤ width < 0.260 μm	0.0250 μm	0.0300 μm	
VIAxs.EN.31.14.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	



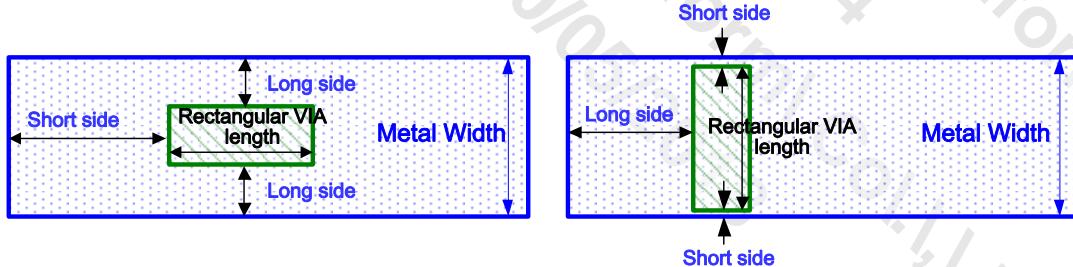
RuleTable.VIAxs.EN.32 (Enclosure of rectangular VIA [length = 0.034 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAxs.EN.32.1.T	width ≤ 0.020 μm	0.0300 μm	0.0000 μm	
VIAxs.EN.32.2.T	0.020 μm < width ≤ 0.022 μm	0.0300 μm	0.0010 μm	
VIAxs.EN.32.3.T	0.022 μm < width ≤ 0.024 μm	0.0300 μm	0.0020 μm	
VIAxs.EN.32.4.T	0.024 μm < width < 0.036 μm	0.0260/0 μm	0.0070/0.0400 μm	
VIAxs.EN.32.5.T	0.036 μm ≤ width < 0.038 μm	0.0260/0.0010 μm	0.0080/0.0400 μm	
VIAxs.EN.32.6.T	0.038 μm ≤ width < 0.040 μm	0.0260/0.0020 μm	0.0090/0.0400 μm	
VIAxs.EN.32.7.T	0.040 μm ≤ width < 0.045 μm	0.0260/0.0030 μm	0.0100/0.0400 μm	
VIAxs.EN.32.8.T	0.045 μm ≤ width < 0.050 μm	0.0260/0.0055 μm	0.0125/0.0400 μm	
VIAxs.EN.32.9.T	0.050 μm ≤ width < 0.055 μm	0.0260/0.0080 μm	0.0150/0.0400 μm	
VIAxs.EN.32.10.T	0.055 μm ≤ width < 0.060 μm	0.0260/0.0105 μm	0.0175/0.0400 μm	
VIAxs.EN.32.11.T	0.060 μm ≤ width < 0.070 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAxs.EN.32.12.T	0.070 μm ≤ width < 0.080 μm	0.0250/0.0100 μm	0.0250/0.0300 μm	
VIAxs.EN.32.13.T	width = 0.080 μm	0.0150 μm	0.0300 μm	
VIAxs.EN.32.14.T	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	



RuleTable.VIAxs.EN.33 (Enclosure of rectangular VIA [length = 0.050 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAxs.EN.33.1.T	width ≤ 0.020 μm	0.0300 μm	0.0000 μm	
VIAxs.EN.33.2.T	0.020 μm < width ≤ 0.022 μm	0.0300 μm	0.0010 μm	
VIAxs.EN.33.3.T	0.022 μm < width ≤ 0.024 μm	0.0300 μm	0.0020 μm	
VIAxs.EN.33.4.T	0.024 μm < width < 0.036 μm	0.0260 μm	0.0070 μm	
VIAxs.EN.33.5.T	0.036 μm ≤ width < 0.038 μm	0.0260 μm	0.0080 μm	
VIAxs.EN.33.6.T	0.038 μm ≤ width < 0.040 μm	0.0260 μm	0.0090 μm	
VIAxs.EN.33.7.T	0.040 μm ≤ width < 0.045 μm	0.0260 μm	0.0100 μm	
VIAxs.EN.33.8.T	0.045 μm ≤ width < 0.050 μm	0.0260 μm	0.0125 μm	
VIAxs.EN.33.9.T	0.050 μm ≤ width < 0.055 μm	0.0260 μm	0.0150 μm	
VIAxs.EN.33.10.T	0.055 μm ≤ width < 0.060 μm	0.0260 μm	0.0175 μm	
VIAxs.EN.33.11.T	0.060 μm ≤ width < 0.070 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAxs.EN.33.12.T	0.070 μm ≤ width < 0.080 μm	0.0250/0.0100 μm	0.0250/0.0300 μm	
VIAxs.EN.33.13.T	width = 0.080 μm	0.0150 μm	0.0300 μm	
VIAxs.EN.33.14.T	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	



Rule No.	Description	Label	Op.	Rule
VIAxs.EN.31.1.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [width \leq 0.020 μm] for two opposite sides with the other two sides \geq 0.0000 μm		\geq	0.0300
VIAxs.EN.31.2.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.020 μm < width \leq 0.022 μm] for two opposite sides with the other two sides \geq 0.0010 μm		\geq	0.0300
VIAxs.EN.31.3.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.022 μm < width \leq 0.024 μm] for two opposite sides with the other two sides \geq 0.0020 μm (Except BLK_WB)		\geq	0.0300
VIAxs.EN.31.3.1.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.022 μm < width \leq 0.024 μm] for two opposite sides with the other two sides \geq 0.0020 μm		\geq	0.0120
VIAxs.EN.31.4.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.024 μm < width < 0.036 μm] for two opposite sides with the other two sides \geq 0.0070 μm (Except BLK_WB)		\geq	0.0260
VIAxs.EN.31.4.1.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.024 μm < width < 0.036 μm] for two opposite sides with the other two sides \geq 0.0040 μm		\geq	0.0150
VIAxs.EN.31.5.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.036 μm \leq width < 0.038 μm] for two opposite sides with the other two sides \geq 0.0080 μm		\geq	0.0260
VIAxs.EN.31.6.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.038 μm \leq width < 0.040 μm] for two opposite sides with the other two sides \geq 0.0090 μm		\geq	0.0260
VIAxs.EN.31.7.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.040 μm \leq width < 0.045 μm] for two opposite sides with the other two sides \geq 0.0100 μm		\geq	0.0250
VIAxs.EN.31.8.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.045 μm \leq width < 0.050 μm] for two opposite sides with the other two sides \geq 0.0125 μm		\geq	0.0250
VIAxs.EN.31.9.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.050 μm \leq width < 0.055 μm] for two opposite sides with the other two sides \geq 0.0150 μm		\geq	0.0250
VIAxs.EN.31.10.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.055 μm \leq width < 0.060 μm] for two opposite sides with the other two sides \geq 0.0175 μm		\geq	0.0250
VIAxs.EN.31.11.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.060 μm \leq width < 0.070 μm] for two opposite sides with the other two sides \geq 0.0200 μm (Except BLK_WB)		\geq	0.0250
VIAxs.EN.31.11.1.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.060 μm \leq width < 0.070 μm] for two opposite sides with the other two sides \geq 0.0150 μm		\geq	0.0200
VIAxs.EN.31.12.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.070 μm \leq width < 0.080 μm] for two opposite sides with the other two sides \geq 0.0250 μm		\geq	0.0250
VIAxs.EN.31.13.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [0.080 μm \leq width < 0.260 μm] for two opposite sides with the other two sides \geq 0.0300 μm		\geq	0.0250
VIAxs.EN.31.14.T	Enclosure of square VIAxs [width = 0.020 μm] by Lower_Metal [width \geq 0.260 μm] for two opposite sides with the other two sides \geq 0.0250 μm		\geq	0.0600
VIAxs.EN.32.1.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [width \leq 0.020 μm] with the other two long sides \geq 0.0000 μm		\geq	0.0300
VIAxs.EN.32.2.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.020 μm < width \leq 0.022 μm] with the other two long sides \geq 0.0010 μm		\geq	0.0300

Rule No.	Description	Label	Op.	Rule
VIAxs.EN.32.3.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.022 μm < width ≤ 0.024 μm] with the other two long sides ≥ 0.0020 μm		≥	0.0300
VIAxs.EN.32.4.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.024 μm < width < 0.036 μm] with the other two long sides ≥ 0.0070/0.0400 μm		≥	0.0260/0
VIAxs.EN.32.5.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.036 μm ≤ width < 0.038 μm] with the other two long sides ≥ 0.0080/0.0400 μm		≥	0.0260/0.0010
VIAxs.EN.32.6.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.038 μm ≤ width < 0.040 μm] with the other two long sides ≥ 0.0090/0.0400 μm		≥	0.0260/0.0020
VIAxs.EN.32.7.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.040 μm ≤ width < 0.045 μm] with the other two long sides ≥ 0.0100/0.0400 μm		≥	0.0260/0.0030
VIAxs.EN.32.8.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.045 μm ≤ width < 0.050 μm] with the other two long sides ≥ 0.0125/0.0400 μm		≥	0.0260/0.0055
VIAxs.EN.32.9.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.050 μm ≤ width < 0.055 μm] with the other two long sides ≥ 0.0150/0.0400 μm		≥	0.0260/0.0080
VIAxs.EN.32.10.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.055 μm ≤ width < 0.060 μm] with the other two long sides ≥ 0.0175/0.0400 μm		≥	0.0260/0.0105
VIAxs.EN.32.11.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.060 μm ≤ width < 0.070 μm] with the other two long sides ≥ 0.0200/0.0250 μm		≥	0.0250/0.0050
VIAxs.EN.32.12.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [0.070 μm ≤ width < 0.080 μm] with the other two long sides ≥ 0.0250/0.0300 μm		≥	0.0250/0.0100
VIAxs.EN.32.13.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides ≥ 0.0300 μm		≥	0.0150
VIAxs.EN.32.14.T	Short side enclosure of rectangular VIAxs [length = 0.034 μm] by Lower_Metal [width > 0.080 μm] with the other two long sides ≥ 0.0300/0.0250 μm		≥	0.0250/0.0300
VIAxs.EN.33.1.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [width ≤ 0.020 μm] with the other two long sides ≥ 0.0000 μm		≥	0.0300
VIAxs.EN.33.2.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.020 μm < width ≤ 0.022 μm] with the other two long sides ≥ 0.0010 μm		≥	0.0300
VIAxs.EN.33.3.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.022 μm < width ≤ 0.024 μm] with the other two long sides ≥ 0.0020 μm		≥	0.0300
VIAxs.EN.33.4.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.024 μm < width < 0.036 μm] with the other two long sides ≥ 0.0070 μm		≥	0.0260
VIAxs.EN.33.5.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.036 μm ≤ width < 0.038 μm] with the other two long sides ≥ 0.0080 μm		≥	0.0260
VIAxs.EN.33.6.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.038 μm ≤ width < 0.040 μm] with the other two long sides ≥ 0.0090 μm		≥	0.0260
VIAxs.EN.33.7.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.040 μm ≤ width < 0.045 μm] with the other two long sides ≥ 0.0100 μm		≥	0.0260
VIAxs.EN.33.8.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.045 μm ≤ width < 0.050 μm] with the other two long sides ≥ 0.0125 μm		≥	0.0260

Rule No.	Description	Label	Op.	Rule
VIAxs.EN.33.9.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.050 μm ≤ width < 0.055 μm] with the other two long sides ≥ 0.0150 μm		≥	0.0260
VIAxs.EN.33.10.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.055 μm ≤ width < 0.060 μm] with the other two long sides ≥ 0.0175 μm		≥	0.0260
VIAxs.EN.33.11.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.060 μm ≤ width < 0.070 μm] with the other two long sides ≥ 0.0200/0.0250 μm		≥	0.0250/0.0050
VIAxs.EN.33.12.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [0.070 μm ≤ width < 0.080 μm] with the other two long sides ≥ 0.0250/0.0300 μm		≥	0.0250/0.0100
VIAxs.EN.33.13.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides ≥ 0.0300 μm		≥	0.0150
VIAxs.EN.33.14.T	Short side enclosure of rectangular VIAxs [length = 0.050 μm] by Lower_Metal [width > 0.080 μm] with the other two long sides ≥ 0.0300/0.0250 μm		≥	0.0250/0.0300

4.5.45 Mxs Layout Rules

- Minimum Pitch (MINP) 0.040 μm can only be drawn in either parallel or perpendicular to PO direction.
- NonMinimum Pitch (NMINP) direction is perpendicular to Minimum pitch (MINP) direction.

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.
M2 (CAD layer: 32;400) is used for M2

DM2_Oxs (CAD layer: 32;407, or DM2_O) is used for DM2_O

DM2 (CAD layer: 32;401) is used for Non-OPC dummy M2

M2 line-end (end) definition: M2 width ≤ 0.060 μm.

DRC checks DM2_O as well as M2 in this section.

Rule No.	Description	Label	Op.	Rule
Mxs.W.1	Width	W1	≥	0.0200
Mxs.W.1.1	Width [MINP direction]	W1A	=	0.0200, 0.0220, 0.0240, 0.0280, 0.0400, 0.0500, 0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1800
Mxs.W.1.1.0.1	Width [MINP direction] (Except following conditions: 1. M2 [INTERACT BLK_M2, INSIDE {SRAMDMY OR BCWDMY}])	W1A	=	0.0200, 0.0220, 0.0240, 0.0400, 0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1800
Mxs.W.1.1.1	Width of Mxs [MINP direction, INTERACT BCWDMY]	W1A1	=	0.0280, 0.0400
Mxs.W.1.1.2	Width of DMxs_O [MINP direction]	W1A2	=	0.0240, 0.0400, 0.1400
Mxs.W.1.2	Width [NMINP direction]	W1B	=	0.0600, 0.0800, 0.0840, 0.1000, 0.1200, 0.1400, ≥ 0.1500
Mxs.W.1.2.1	Width [NMINP direction] (Except following conditions: 1. M2 [INTERACT BLK_M2, INSIDE SRAMDMY])	W1B	=	0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1500
Mxs.W.2	Width of 45-degree bent Mxs (Except SEALRING_ALL)	W2	≥	0.4000
Mxs.W.3	Maximum width (Except SEALRING_ALL, LOGO)	W3	≤	0.5000
Mxs.S.1	Space	S1	≥	0.0200
Mxs.S.12	Space to 45-degree bent Mxs [PRL > 0 μm] (Except SEALRING_ALL)	S12	≥	0.4000
Mxs.S.12.1	Space to 45-degree bent Mxs (Except SEALRING_ALL)	S12A	≥	0.1400
Mxs.S.13.1	Space to VIAxs-1 or VIAxs or VIAx or VIAxa [maximum delta V > 0.96V]	S13	≥	0.0550
Mxs.S.13.2	Space to VIAxs-1 or VIAxs or VIAx or VIAxa [maximum delta V > 1.32V] (1.2V + 10%)	S13	≥	0.0640
Mxs.S.13.3	Space to VIAxs-1 or VIAxs or VIAx or VIAxa [maximum delta V > 1.65V] (1.5V + 10%)	S13	≥	0.0700
Mxs.S.13.4	Space to VIAxs-1 or VIAxs or VIAx or VIAxa [maximum delta V > 1.98V] (1.8V + 10%)	S13	≥	0.0820
Mxs.S.13.5	Space to VIAxs-1 or VIAxs or VIAx or VIAxa [maximum delta V > 2.75V] (2.5V + 10%)	S13	≥	0.0870
Mxs.S.18	Space to Mxs [maximum delta V > 0.96V] (Except following conditions: 1. M2 in MetalFuse)	S18	≥	0.0520

Rule No.	Description	Label	Op.	Rule
Mxs.S.18.1	Space to Mxs [maximum delta V > 1.32V] (1.2V + 10%) (Except following conditions: 1. M2 in MetalFuse)	S18	≥	0.0550
Mxs.S.18.2	Space to Mxs [maximum delta V > 1.65V] (1.5V + 10%) (Except following conditions: 1. M2 in MetalFuse)	S18	≥	0.0610
Mxs.S.18.3	Space to Mxs [maximum delta V > 1.98V] (1.8V + 10%) (Except following conditions: 1. M2 in MetalFuse)	S18	≥	0.0690
Mxs.S.18.4	Space to Mxs [maximum delta V > 2.75V] (2.5V + 10%) (Except following conditions: 1. M2 in MetalFuse)	S18	≥	0.0790
Mxs.S.18.6	Corner projected space of Mxs [maximum delta V > 0.96V, -0.060 μm < PRL ≤ 0 μm]	S18F	≥	0.1000
Mxs.S.18.7	Corner projected space of Mxs [maximum delta V > 1.98V, -0.100 μm < PRL ≤ 0 μm]	S18G	≥	0.1000
Mxs.S.31.1.T	Space of Mxs to Mxs [width < 0.022 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.038 μm]	S31AT	≥	0.0200
Mxs.S.32.1.T	Space of Mxs to Mxs [0.022 μm ≤ width < 0.024 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.038 μm]	S32AT	≥	0.0200
Mxs.S.33.1.T	Space of Mxs to Mxs [0.024 μm ≤ width < 0.040 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.038 μm]	S33AT	≥	0.0200
Mxs.S.34.1.T	Space of Mxs to Mxs [0.040 μm ≤ width < 0.0405 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.038 μm]	S34AT	≥	0.0250
Mxs.S.34.2.T	Space of Mxs [NOT INTERACT BLK_M2] to Mxs [0.040 μm ≤ width < 0.0405 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.038 μm]	S34B	≥	0.0350
Mxs.S.34.3.T	Space of Mxs to Mxs [0.040 μm ≤ width < 0.0405 μm with edge length > 0.060 μm in NMNP direction, NOT INTERACT BLK_M2] in MINP direction [PRL > -0.038 μm]	S34C	≥	0.0350
Mxs.S.35.1.T	Space of Mxs to Mxs [0.0405 μm ≤ width < 0.0605 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.038 μm]	S35AT	≥	0.0350
Mxs.S.35.2.T	Space of Mxs to Mxs [0.0605 μm ≤ width < 0.080 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm]	S35BT	≥	0.0350
Mxs.S.36.1.T	Space of Mxs to Mxs [0.080 μm ≤ width < 0.100 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm]		≥	0.0350
Mxs.S.37.1.T	Space of Mxs to Mxs [0.100 μm ≤ width < 0.120 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm]		≥	0.0600
Mxs.S.38.1.T	Space of Mxs to Mxs [0.120 μm ≤ width < 0.140 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm]		≥	0.0600
Mxs.S.39.1.T	Space of Mxs to Mxs [0.140 μm ≤ width < 0.180 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm]		≥	0.0600
Mxs.S.40.1.T	Space of Mxs to Mxs [0.180 μm ≤ width < 0.260 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm]		≥	0.0600
Mxs.S.41.1.T	Space of Mxs to Mxs [width ≥ 0.260 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm]		≥	0.0600
Mxs.S.42.1.T	Space of Mxs to Mxs [0.060 μm ≤ width < 0.080 μm with edge length > 0.060 μm in MINP direction] in NMNP direction [PRL > -0.060 μm]		≥	0.0600

Rule No.	Description	Label	Op.	Rule
Mxs.S.43.1.T	Space of Mxs to Mxs [$0.080 \mu\text{m} \leq \text{width} < 0.100 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > -0.060 μm]		\geq	0.0760
Mxs.S.44.1.T	Space of Mxs to Mxs [$0.100 \mu\text{m} \leq \text{width} < 0.120 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > -0.060 μm]		\geq	0.0760
Mxs.S.45.1.T	Space of Mxs to Mxs [$0.120 \mu\text{m} \leq \text{width} < 0.140 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > -0.060 μm]		\geq	0.0760
Mxs.S.46.1.T	Space of Mxs to Mxs [width $\geq 0.140 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > 0 μm]	S46AT	\geq	0.1200
Mxs.S.46.2.T	Space of Mxs to Mxs [width $\geq 0.140 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > 0.080 μm]	S46BT	\geq	0.1600
Mxs.S.47.1.T	Space of Mxs to Mxs [width $\geq 0.150 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > 0 μm]	S47AT	\geq	0.1200
Mxs.S.47.2.T	Space of Mxs [edge length $> 0.060 \mu\text{m}$ in MINP direction] to Mxs [width $\geq 0.150 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > 0 μm]	S47BT	\geq	0.1400
Mxs.S.47.3.T	Space of Mxs [edge length $> 0.060 \mu\text{m}$ in MINP direction] to Mxs [width $\geq 0.150 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > 0.080 μm]	S47CT	\geq	0.1800
Mxs.S.48.1.T	Space of Mxs to Mxs [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > 0 μm]		\geq	0.1200
Mxs.S.48.2.T	Space of Mxs [edge length $> 0.060 \mu\text{m}$ in MINP direction] to Mxs [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > 0 μm]	S48B	\geq	0.1800
Mxs.S.48.3.T	Space of Mxs [edge length $> 0.060 \mu\text{m}$ in MINP direction] to Mxs [width $\geq 0.260 \mu\text{m}$ with edge length $> 0.060 \mu\text{m}$ in MINP direction] in NMINP direction [PRL > 0.080 μm]	S48C	\geq	0.2600
Mxs.S.51.1	Space of Mxs to Mxs line-end in NMINP direction [PRL > -0.020 μm]		\geq	0.0300
Mxs.S.51.1.1	Space of Mxs [NOT INTERACT BLK_M2] to Mxs line-end in NMINP direction [PRL > -0.020 μm]		\geq	0.0380
Mxs.S.51.1.2	Space of Mxs to Mxs line-end [NOT INTERACT BLK_M2] in NMINP direction [PRL > -0.020 μm]		\geq	0.0380
Mxs.S.51.2	Space of Mxs to Mxs line-end in MINP direction [PRL > -0.060 μm]		\geq	0.0600
Mxs.S.61	Corner projected space of Mxs [-0.025 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$] (Except following conditions: 1. Corner with edge length $\leq 0.028 \mu\text{m}$ on both sides)		\geq	0.0250
Mxs.S.61.1	Corner projected space of Mxs [NOT INTERACT BLK_M2] to Mxs [-0.060 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$] (Except following conditions: 1. Corner with edge length $\leq 0.028 \mu\text{m}$ on both sides)		\geq	0.0600
Mxs.EN.0	1. Enclosure of square Lower_VIA [width = 0.020 μm] is defined by RuleTable.Mxs.EN.31 in the subsection 2. Enclosure of rectangular Lower_VIA [length = 0.034 μm] is defined by RuleTable.Mxs.EN.32 in the subsection 3. Enclosure of rectangular Lower_VIA [length = 0.050 μm] is defined by RuleTable.Mxs.EN.33 in the subsection			
Mxs.EN.1.6	Enclosure of square VIAxS by Mxs [$0.080 \mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.030 \mu\text{m}$ (Except following conditions: 1. Mxs [width = 0.120 μm] enclosure of square VIAxS array) Definition of square VIAxS-1 array follows Mxs.EN.3.5	EN1F	\geq	0.0200
Mxs.EN.3.5	Enclosure of square VIAxS array by Mxs [width = 0.120 μm] for two opposite sides with the other two sides [Square VIAxS array edge length = 0.020 μm] $\geq 0.018 \mu\text{m}$ Definition of square VIAxS array: VIAxS space = 0.044 μm [PRL = 0.020 μm] in Mxs MINP direction	EN3E	\geq	0.0300
Mxs.EN.6.4	Short side enclosure of rectangular VIAxS by Mxs edge [length = 0.080 μm , Mxs width = 0.080 μm]	EN6D	\geq	0.0250

Rule No.	Description	Label	Op.	Rule
Mxs.L.1	At least one edge length of 45-degree bent Mxs (minimum edge length)	L1	\geq	0.9100
Mxs.L.2	Edge length with adjacent edge [length < 0.080 μm]	L2	\geq	0.0800
Mxs.L.2.1	Edge length with adjacent edge [length < 0.090 μm] (Except BLK_M2)	L2	\geq	0.0800
Mxs.A.1	Area of Mxs	A1	\geq	0.00300
Mxs.DN.1.1	Minimum All_metal density in window 40 μm x 40 μm , stepping 20 μm (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	12.5%
Mxs.DN.1.2	Minimum All_metal density in window 40 μm x 40 μm , stepping 20 μm [3 μm x 3 μm empty area exists in the window] (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	25%
Mxs.DN.2	Maximum All_metal density in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, DMxs_O)		\leq	65%
Mxs.DN.2.3	Maximum All_metal density in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	75%
Mxs.DN.3	The All_metal density difference between any two neighboring checking windows including DMnEXCL [window 40 μm x 40 μm , stepping 40 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\leq	50%
Mxs.DN.3.8	Minimum All_metal local density in window 40 μm x 40 μm , stepping 20 μm (Except SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by TSMC)		>	4.5%
Mxs.DN.6.1	All_metal density [window 9 μm x 9 μm , stepping 4.5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	1%
Mxs.DN.7	It is not allowed to have local density < 5% of all 3 consecutive metal (Mxs, Mxs+1, and Mxs+2) over any 27 μm x 27 μm (stepping 13.5 μm), i.e. it is allowed for either one of Mxs, Mxs+1, or Mxs+2 to have a local density \geq 5% (The metal layers include Mxs/Mxs+1/Mxs+2 and dummy metals for ELK film) (Except ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc, 2. TCDDMY_Mn (assume 30% pattern density INSIDE TCDDMY_Mn))			
Mxs.DN.9	Minimum Line edge Density (LeD) in window 20 μm x 20 μm , stepping 10 μm Definition of "Line edge Density": (((All_metal area) - (All_metal SIZING -0.001 μm area)) x 1000) / Checking window (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags only if the checking window has any one Mxs metal width < 0.060 μm		\geq	8.5

Rule No.	Description	Label	Op.	Rule
Mxs.DN.9.1	<p>Minimum Line edge Density (LeD) in window 20 μm x 20 μm, stepping 10 μm</p> <p>Definition of "Line edge Density": $((\text{All_metal area}) - (\text{All_metal SIZING } -0.001 \mu\text{m area})) \times 1000 / \text{Checking window}$</p> <p>(Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window has any one Mxs metal width < 0.120 μm</p>		≥	3
Mxs.R.1	Mxs must be a rectangle (Except SEALRING_ALL, LOGO)			
Mxs.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
Mxs.R.10	Overlap MetalFuse_B1 (156;8) is not allowed (Except following conditions: 1. {M2 AND MetalFuseLink (156;3)})			
Mxs.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of Mxs space to Mxs or VIAx-1 or VIAx is < 0.360 μm			
Mxs.R.14	<p>{Mxs_Empty_Area SIZING 0.330 μm} INTERACT Mxs island is not allowed</p> <p>Definitions:</p> <p>1. Mxs_Empty_Area: Area of {{CHIP NOT {{TCDDMY_Mn OR ICOVL_SINGLE} OR {{Mxs OR DMxs} OR DMxs_O}}} SIZING down/up 0.380 μm} ≥ 1.96 μm²</p> <p>2. Mxs island: Area of (Mxs with only one square VIAx [width x length = 0.020 μm x 0.020 μm]) ≤ 0.010 μm²</p>			
Mxs.R.15	<p>{Mxs_Empty_Area SIZING 0.100 μm in MINP direction} interact VIAx-1 [INTERACT Mxs [width < 0.060 μm]] is not allowed</p> <p>(Except following conditions: 1. VIA1 inside BLK_M2)</p> <p>Definition of Mxs_Empty_Area: {{{CHIP NOT {{Mxs OR DMxs} OR DMxs_O}}} SIZING down/up 0.380 μm in MINP direction} SIZING down/up 0.400 μm in NMNP direction} can enclose a 0.760 μm x 0.800 μm (MINP x NMNP) orthogonal rectangle</p>			
Mxs.R.17	DMxs is a must in chip level.			
Mxs.R.18	<p>Mxs [width ≤ 0.022 μm] interact VIAx-1_array_region is not allowed</p> <p>(Except following conditions: 1. M2 interact BLK_M2)</p> <p>VIAx-1_array_region definition:</p> <p>(1) VIAx-1 array is ≥ 2x2 VIAx-1 array, and</p> <p>(2) Two VIAx-1 space < 0.132 μm in NMNP direction [PRL > 0 μm], and both of the VIAx-1 space = 0.0505~0.0760 μm in MINP direction [PRL > -0.018 μm], and</p> <p>(3) Form one region from one of each VIAx-1 corner (C1/C2/C3/C4), and the space of the corners is the minimum in MINP and NMNP direction.</p>			

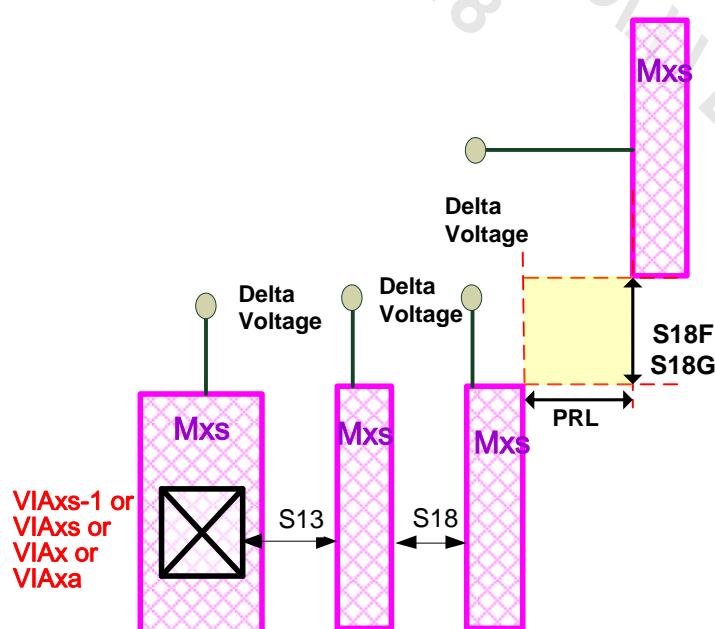
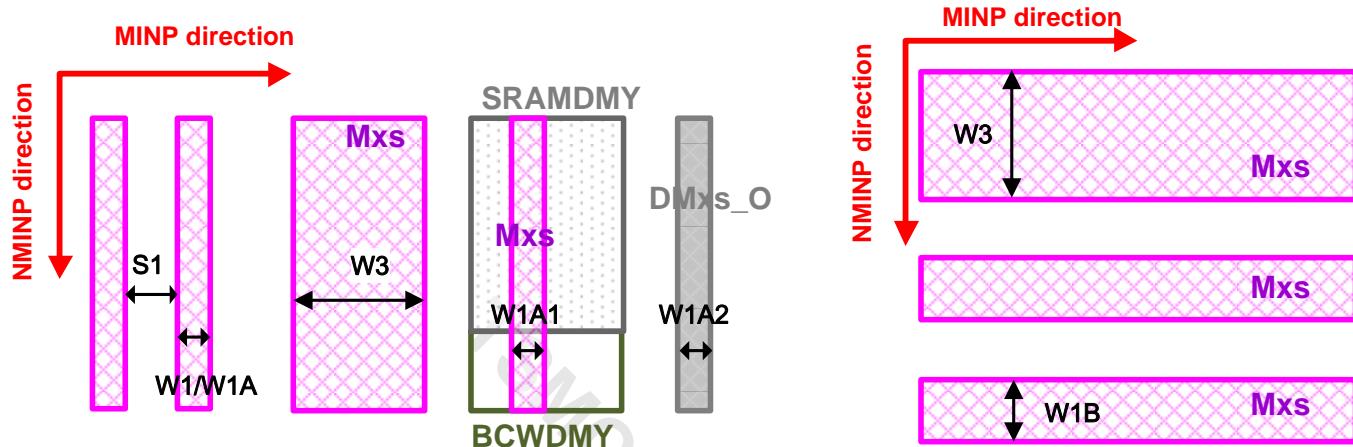
Rule No.	Description	Label	Op.	Rule
Mxs.R.18.1	<p>Mxs [width ≤ 0.022 μm] interact VIAx-1_array_region is not allowed (Except following conditions: 1. M2 interact BLK_M2)</p> <p>VIAx-1_array_region definition: (1) VIAx-1 array is ≥ 2x2 VIAx-1 array, and (2) Two VIAx-1 space < 0.094 μm in NMNP direction [PRL > 0 μm], and both of the VIAx-1 space = 0.0505~0.0760 μm in MNP direction [PRL > -0.0205 μm], and (3) Form one region from one of each VIAx-1 corner (C1/C2/C3/C4), and the space of the corners is the minimum in MNP and NMNP direction.</p>			
Mxs.R.18.2	<p>Space of Mxs [width ≤ 0.022 μm] to Checked_VIAx-1_Edge in MNP direction [PRL > -0.0205 μm] < 0.060 μm is not allowed (Except following conditions: 1. M2 interact BLK_M2)</p> <p>Definition of Checked_VIAx-1_Group: {VIAx-1 [space to VIAx-1 < 0.056 μm in NMNP direction, PRL > 0 μm]}</p> <p>Definition of Checked_VIAx-1_Edge: Checked_VIAx-1_Group NMNP edge[space to VIAx-1 = 0.060~0.0975 μm in MNP direction, PRL > -0.018 μm]</p>			
Mxs.R.18.3	<p>Checked_VIA space to 2 or more Lower_VIA [INTERACT another Mxs] < 0.029 μm is not allowed</p> <p>Definition of Checked_VIA: Lower_VIA [INTERACT Mxs width ≤ 0.022 μm] enclosure by Mxs < 0.046 μm in NMNP direction</p> <p>DRC flags Checked_VIA space to 2 or more Lower_VIA < 0.029 μm in MNP with corner direction</p>			
Mxs.R.21.1	<p>Space of Checked_Metal ≤ 0.020 μm in MNP [PRL > 0 μm] is not allowed</p> <p>Definition of Checked_Metal: {Mxs [width ≤ 0.024 μm] AND Wide_Metal_Check_Region}</p> <p>Definition of Wide_Metal_Check_Region: {Mxs [width ≥ 0.260 μm in MNP direction] SIZING 0.200 μm in MNP direction}</p>			

Table Notes:

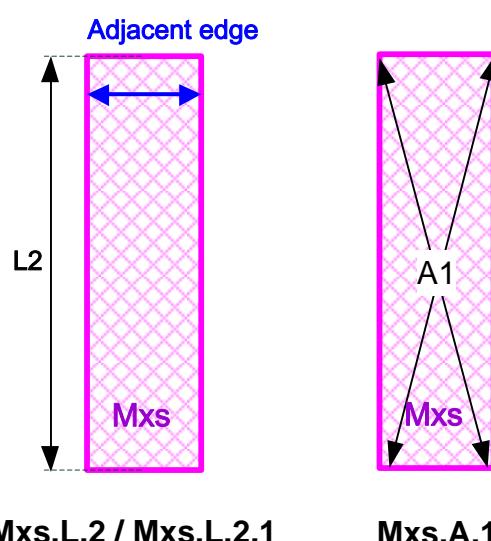
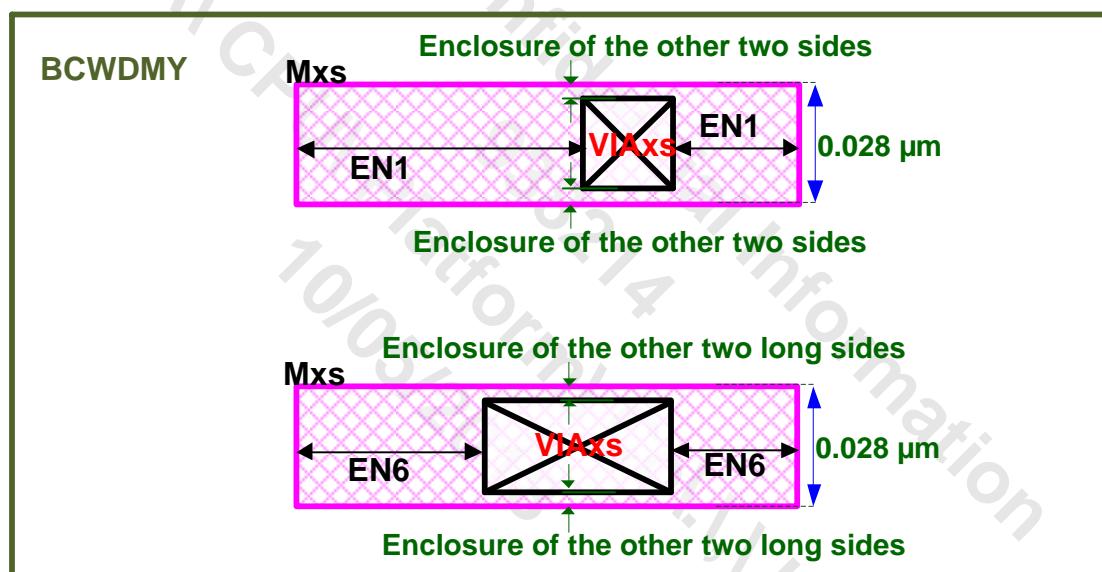
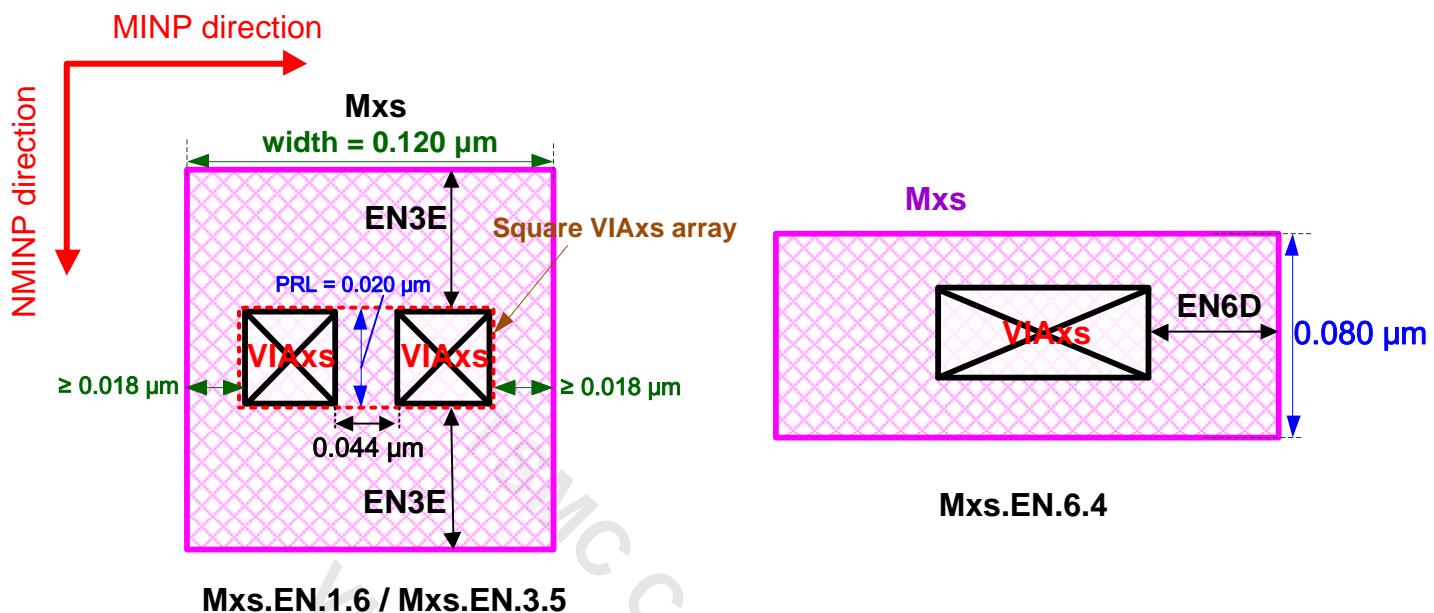
- To meet the metal process window, filling the dummy metal globally and uniformly by tsmc utility is needed even if the originally drawn Mxs has already met the density rules. For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, filling manually and evenly is still needed.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations during placement. Unexpected violations may occur during the IP/macro placement due to the environment, even if the IP/macro already passed the high density rule check. Therefore, customers need to carefully design the dimension of the width/space for wide metal (e.g., power/ground bus), under the proper high density limit.
- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

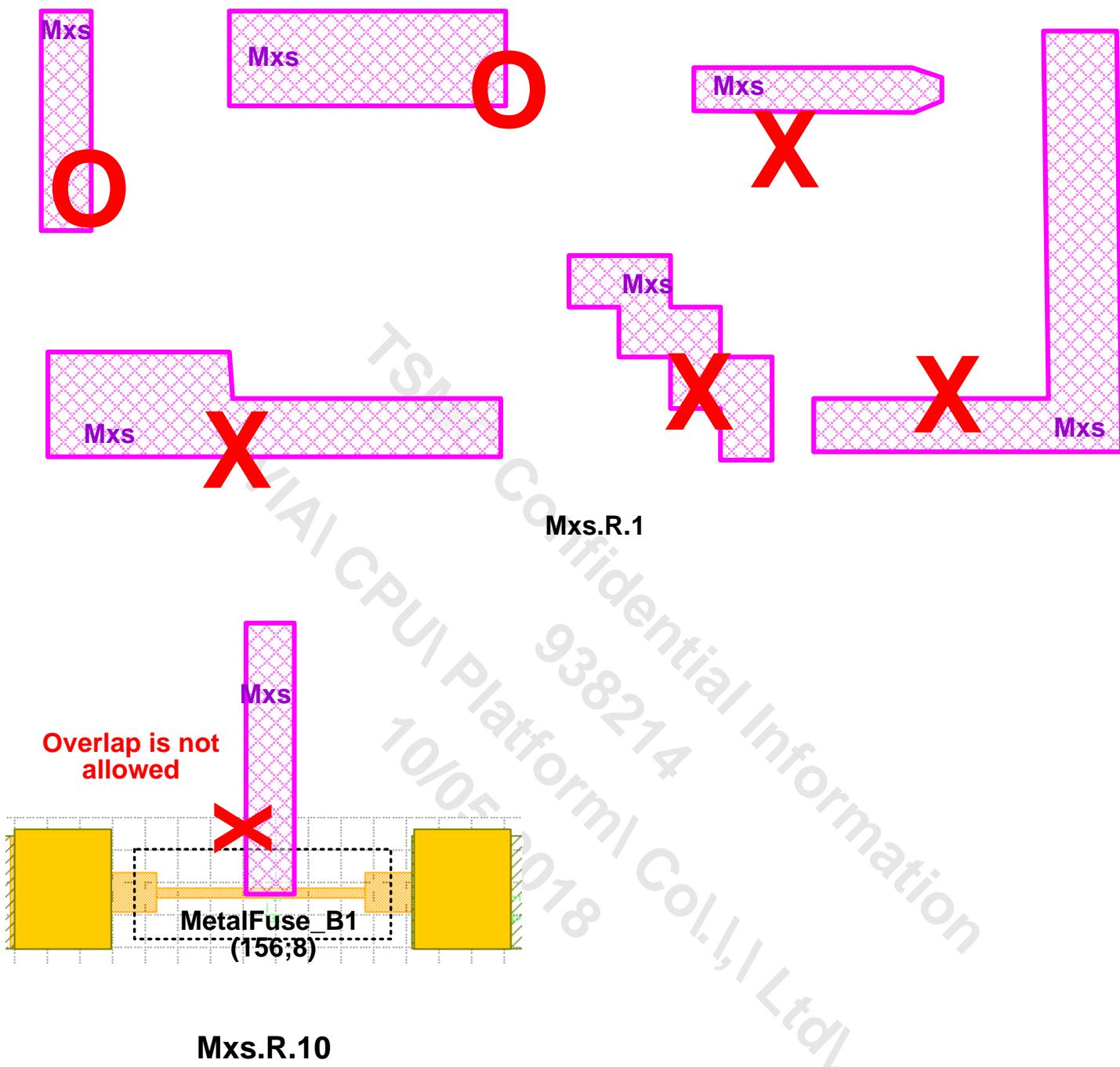
TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

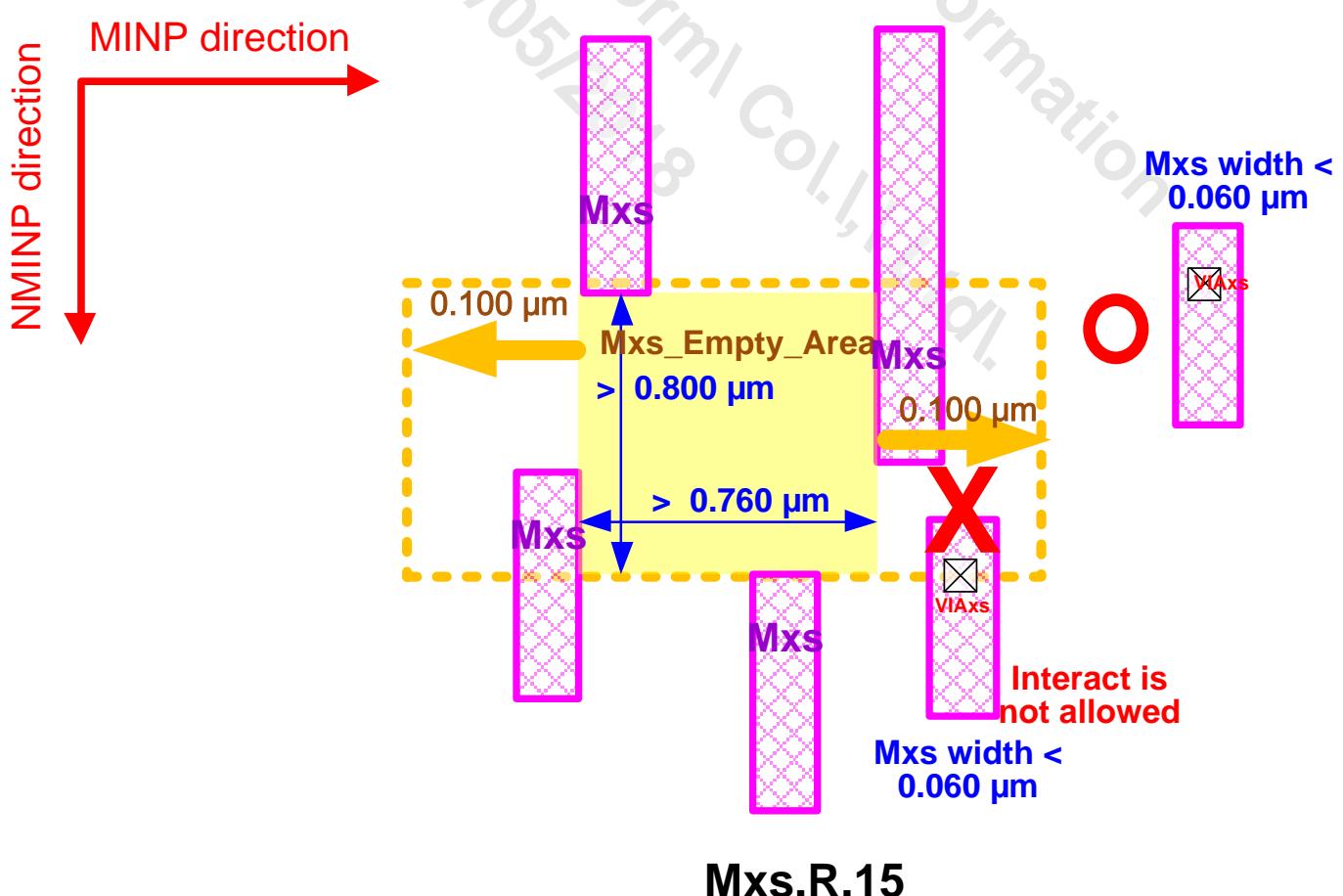
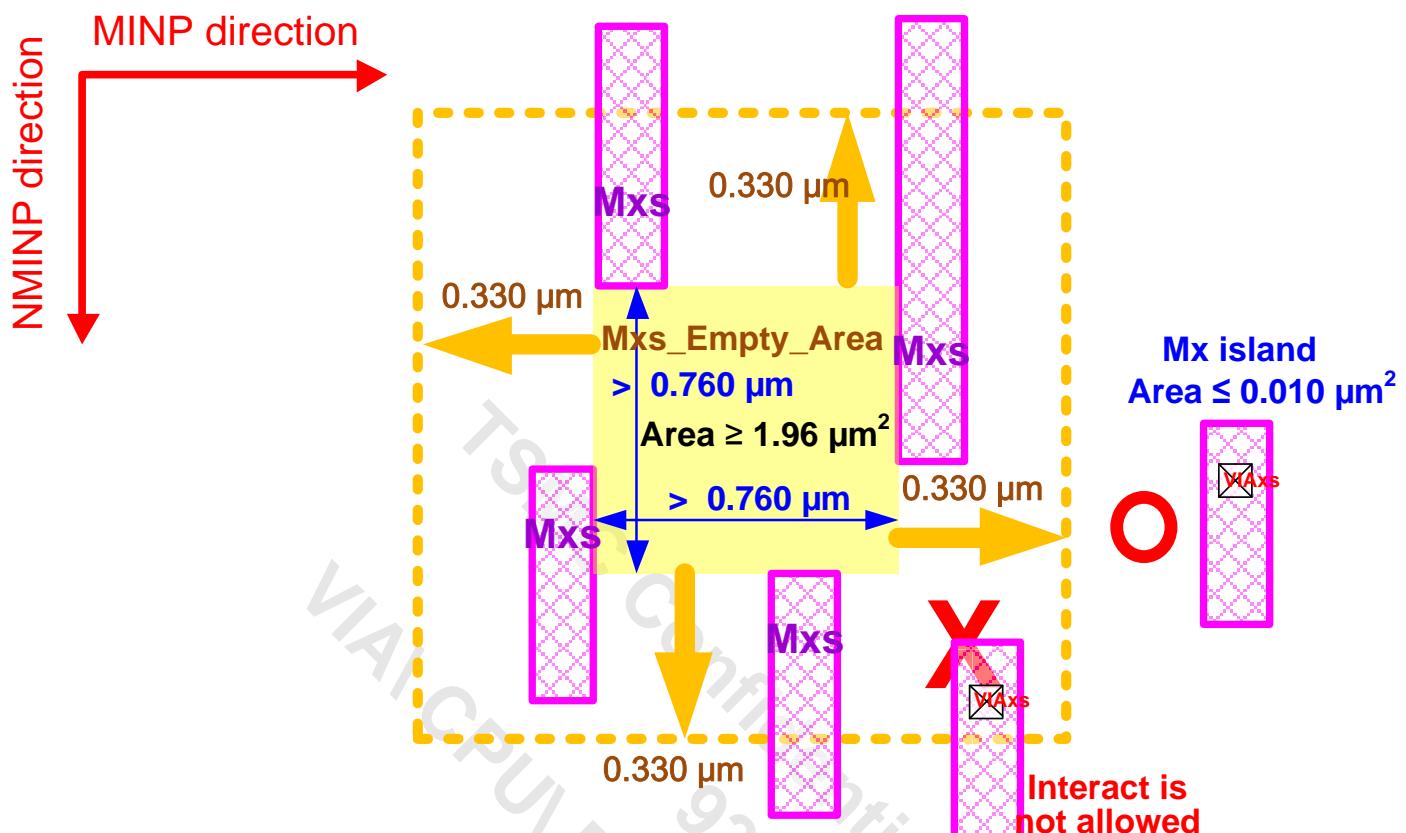
Mxs

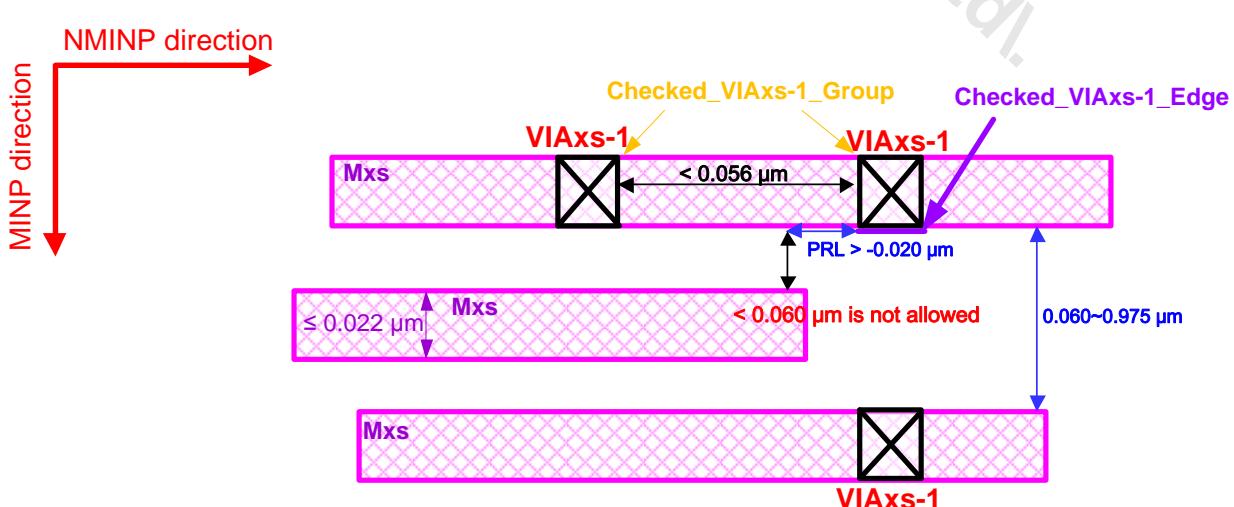
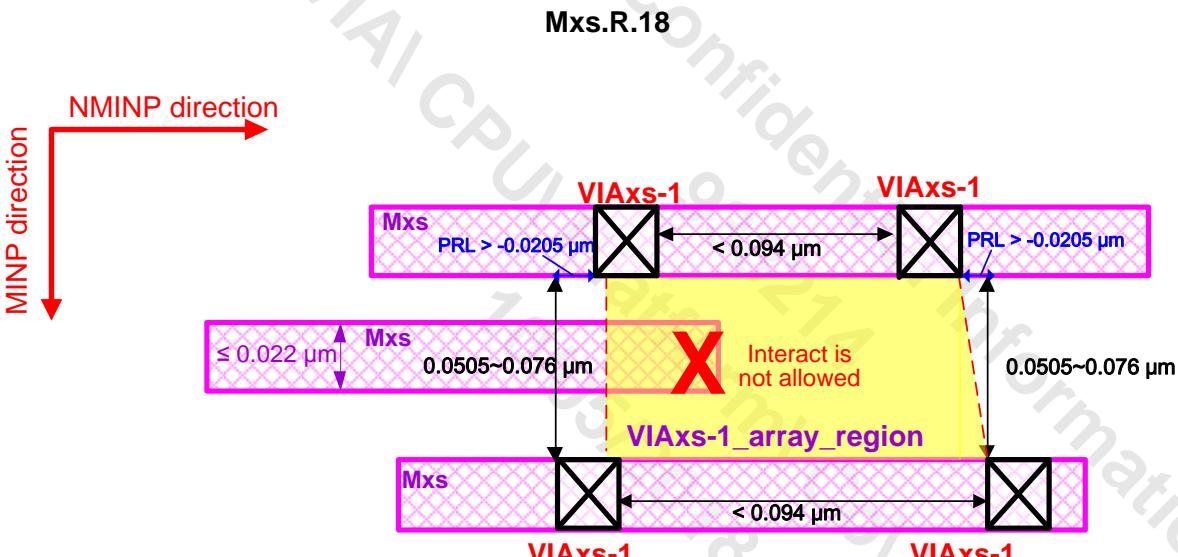
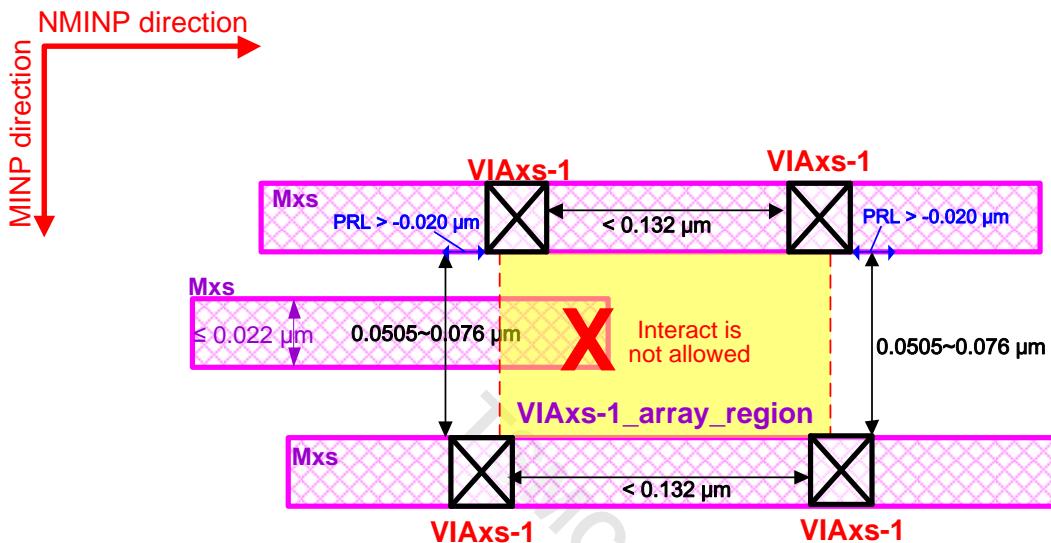


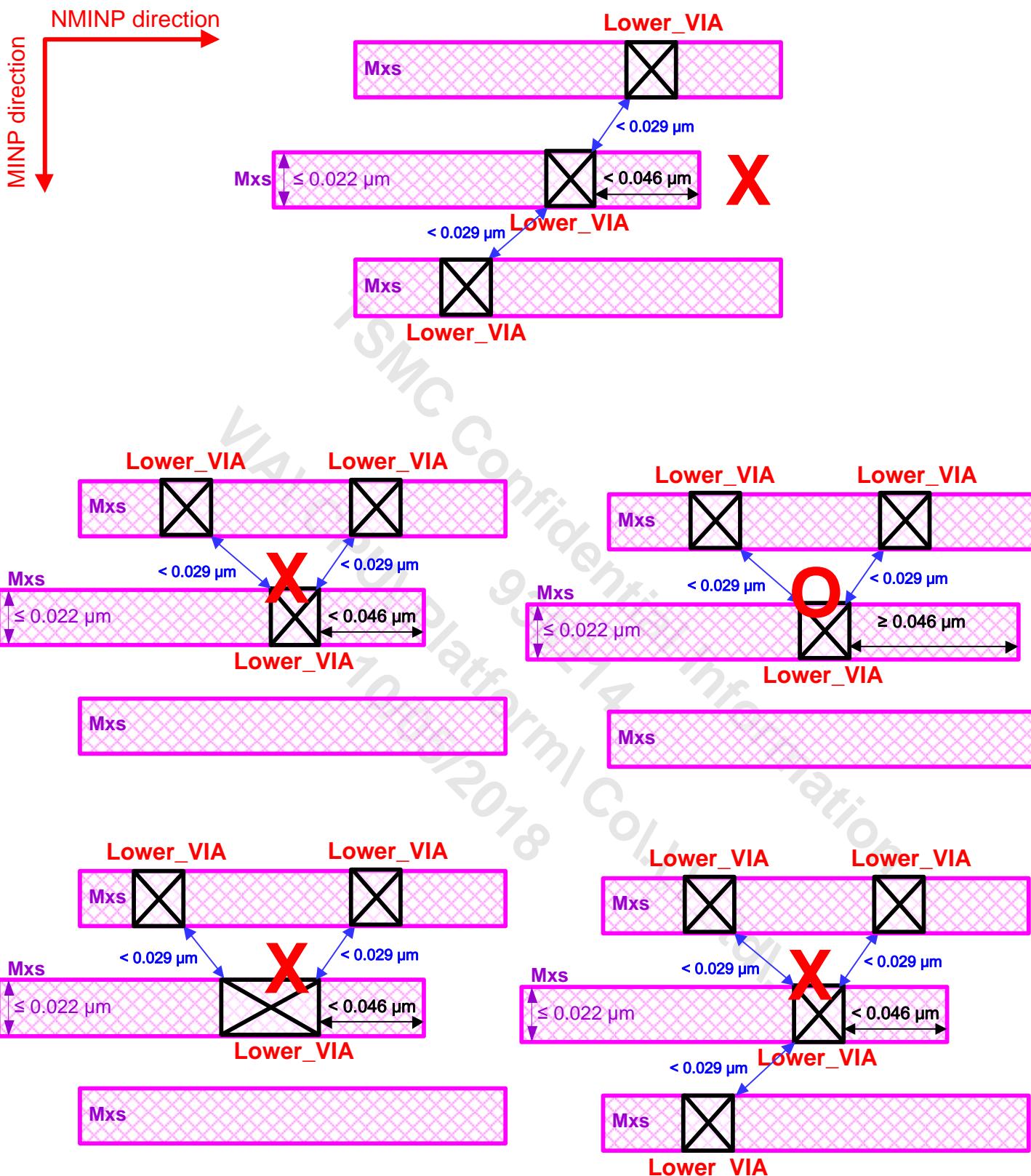
Mxs.S.13.1 / Mxs.S.13.2 / Mxs.S.13.3 / Mxs.S.13.4 / Mxs.S.13.5
Mxs.S.18 / Mxs.S.18.1 / Mxs.S.18.2 / Mxs.S.18.3 / Mxs.S.18.4
Mxs.S.18.6 / Mxs.S.18.7



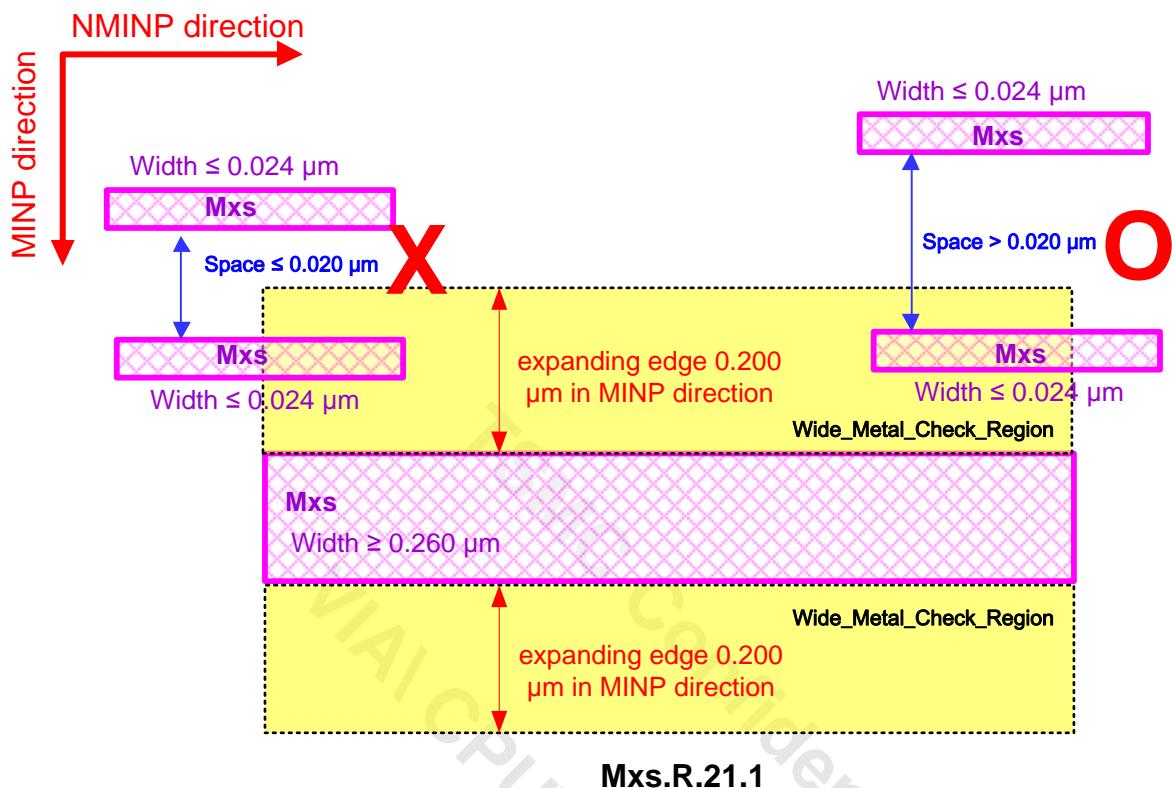






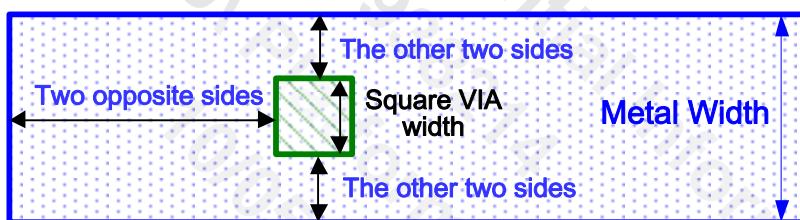


Mxs.R.18.3



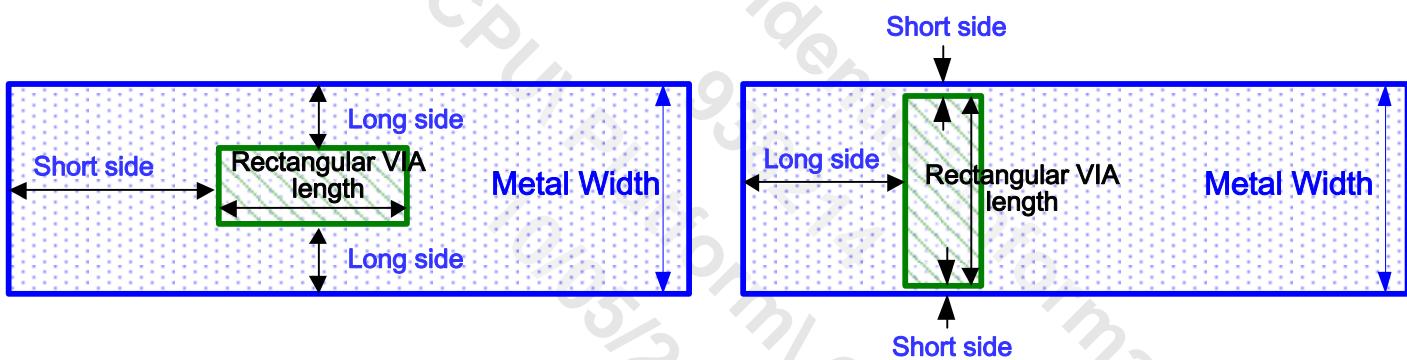
4.5.45.1 Mxs Enclosure Rule Tabulation

RuleTable.Mxs.EN.31 (Enclosure of square VIA [width = 0.020 μm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
Mxs.EN.31.1.T	width < 0.022 μm	0.0280 μm	0 μm	
Mxs.EN.31.2.T	0.022 μm ≤ width < 0.024 μm	0.0280 μm	0.0010 μm	
Mxs.EN.31.3.T	0.024 μm ≤ width < 0.026 μm	0.0280 μm	0.0020 μm	
Mxs.EN.31.4.T	0.026 μm ≤ width < 0.028 μm	0.0280 μm	0.0030 μm	
Mxs.EN.31.5.T	0.028 μm ≤ width < 0.040 μm	0.0280 μm	0.0040 μm	
Mxs.EN.31.6.T	0.040 μm ≤ width < 0.060 μm	0.0280 μm	0.0100 μm	BLK_M2
Mxs.EN.31.6.1.T	0.040 μm ≤ width < 0.060 μm	0.0120 μm	0.0050 μm	
Mxs.EN.31.7.T	0.060 μm ≤ width < 0.080 μm	0.0250 μm	0.0200 μm	
Mxs.EN.31.8.T	0.080 μm ≤ width < 0.260 μm	0.0180 μm	0.0300 μm	
Mxs.EN.31.9.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	



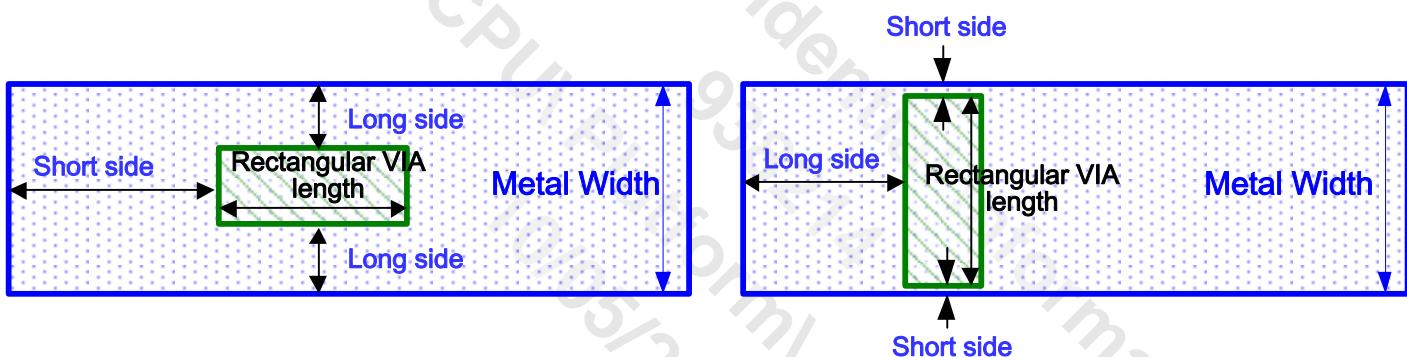
RuleTable.Mxs.EN.32 (Enclosure of rectangular VIA [length = 0.034 μm])

Rule Number	Metal Width	Short side	Long side	Exception
Mxs.EN.32.1.T	width < 0.022 μm	0.0280 μm	0 μm	
Mxs.EN.32.2.T	0.022 μm ≤ width < 0.024 μm	0.0280 μm	0.0010 μm	
Mxs.EN.32.3.T	0.024 μm ≤ width < 0.026 μm	0.0280 μm	0.0020 μm	
Mxs.EN.32.4.T	0.026 μm ≤ width < 0.028 μm	0.0280 μm	0.0030 μm	
Mxs.EN.32.5.T	0.028 μm ≤ width < 0.040 μm	0.0280 μm	0.0040 μm	
Mxs.EN.32.6.T	0.040 μm ≤ width < 0.060 μm	0.0280 μm	0.0100 μm	
Mxs.EN.32.7.T	0.060 μm ≤ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
Mxs.EN.32.8.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
Mxs.EN.32.9.T	0.080 μm < width < 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	
Mxs.EN.32.10.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	



RuleTable.Mxs.EN.33 (Enclosure of rectangular VIA [length = 0.050 μm])

Rule Number	Metal Width	Short side	Long side	Exception
Mxs.EN.33.1.T	width < 0.022 μm	0.0280 μm	0 μm	
Mxs.EN.33.2.T	0.022 μm ≤ width < 0.024 μm	0.0280 μm	0.0010 μm	
Mxs.EN.33.3.T	0.024 μm ≤ width < 0.026 μm	0.0280 μm	0.0020 μm	
Mxs.EN.33.4.T	0.026 μm ≤ width < 0.028 μm	0.0280 μm	0.0030 μm	
Mxs.EN.33.5.T	0.028 μm ≤ width < 0.040 μm	0.0280 μm	0.0040 μm	
Mxs.EN.33.6.T	0.040 μm ≤ width < 0.060 μm	0.0280 μm	0.0100 μm	
Mxs.EN.33.7.T	0.060 μm ≤ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
Mxs.EN.33.8.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
Mxs.EN.33.9.T	0.080 μm < width < 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	
Mxs.EN.33.10.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	



Rule No.	Description	Label	Op.	Rule
Mxs.EN.31.1.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [width < 0.022 μm] for two opposite sides with the other two sides \geq 0 μm		\geq	0.0280
Mxs.EN.31.2.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [0.022 μm \leq width < 0.024 μm] for two opposite sides with the other two sides \geq 0.0010 μm		\geq	0.0280
Mxs.EN.31.3.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [0.024 μm \leq width < 0.026 μm] for two opposite sides with the other two sides \geq 0.0020 μm		\geq	0.0280
Mxs.EN.31.4.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [0.026 μm \leq width < 0.028 μm] for two opposite sides with the other two sides \geq 0.0030 μm		\geq	0.0280
Mxs.EN.31.5.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [0.028 μm \leq width < 0.040 μm] for two opposite sides with the other two sides \geq 0.0040 μm		\geq	0.0280
Mxs.EN.31.6.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [0.040 μm \leq width < 0.060 μm] for two opposite sides with the other two sides \geq 0.0100 μm (Except BLK_M2)		\geq	0.0280
Mxs.EN.31.6.1.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [0.040 μm \leq width < 0.060 μm] for two opposite sides with the other two sides \geq 0.0050 μm		\geq	0.0120
Mxs.EN.31.7.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [0.060 μm \leq width < 0.080 μm] for two opposite sides with the other two sides \geq 0.0200 μm		\geq	0.0250
Mxs.EN.31.8.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [0.080 μm \leq width < 0.260 μm] for two opposite sides with the other two sides \geq 0.0300 μm		\geq	0.0180
Mxs.EN.31.9.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxs [width \geq 0.260 μm] for two opposite sides with the other two sides \geq 0.0250 μm		\geq	0.0600
Mxs.EN.32.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [width < 0.022 μm] with the other two long sides \geq 0 μm		\geq	0.0280
Mxs.EN.32.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [0.022 μm \leq width < 0.024 μm] with the other two long sides \geq 0.0010 μm		\geq	0.0280
Mxs.EN.32.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [0.024 μm \leq width < 0.026 μm] with the other two long sides \geq 0.0020 μm		\geq	0.0280
Mxs.EN.32.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [0.026 μm \leq width < 0.028 μm] with the other two long sides \geq 0.0030 μm		\geq	0.0280
Mxs.EN.32.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [0.028 μm \leq width < 0.040 μm] with the other two long sides \geq 0.0040 μm		\geq	0.0280
Mxs.EN.32.6.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [0.040 μm \leq width < 0.060 μm] with the other two long sides \geq 0.0100 μm		\geq	0.0280
Mxs.EN.32.7.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [0.060 μm \leq width < 0.080 μm] with the other two long sides \geq 0.0200/0.0250 μm		\geq	0.0250/0.0050
Mxs.EN.32.8.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [width = 0.080 μm] with the other two long sides \geq 0.0200/0.0300 μm		\geq	0.0250/0.0150
Mxs.EN.32.9.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [0.080 μm < width < 0.260 μm] with the other two long sides \geq 0.0300/0.0250 μm		\geq	0.0250/0.0300
Mxs.EN.32.10.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxs [width \geq 0.260 μm] with the other two long sides \geq 0.0250 μm		\geq	0.0600

Rule No.	Description	Label	Op.	Rule
Mxs.EN.33.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0280
Mxs.EN.33.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [0.022 $\mu\text{m} \leq$ width < 0.024 μm] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0280
Mxs.EN.33.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [0.024 $\mu\text{m} \leq$ width < 0.026 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
Mxs.EN.33.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [0.026 $\mu\text{m} \leq$ width < 0.028 μm] with the other two long sides $\geq 0.0030 \mu\text{m}$		\geq	0.0280
Mxs.EN.33.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [0.028 $\mu\text{m} \leq$ width < 0.040 μm] with the other two long sides $\geq 0.0040 \mu\text{m}$		\geq	0.0280
Mxs.EN.33.6.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [0.040 $\mu\text{m} \leq$ width < 0.060 μm] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0280
Mxs.EN.33.7.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [0.060 $\mu\text{m} \leq$ width < 0.080 μm] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
Mxs.EN.33.8.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
Mxs.EN.33.9.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [0.080 $\mu\text{m} <$ width < 0.260 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$		\geq	0.0250/0.0300
Mxs.EN.33.10.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxs [width $\geq 0.260 \mu\text{m}$] with the other two long sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600

4.5.46 VIAx Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.
VIAx in this section check VIA_n ($n \geq 2$)

Rule No.	Description	Label	Op.	Rule
VIAx.W.1	Width (Except SEALRING_ALL)	W1	=	0.0200, 0.0380
VIAx.W.2	Width of VIAx bar in SEALRING_ALL	W2	=	0.1400
VIAx.S.1	Space (Except SEALRING_ALL)	S1	\geq	0.0280
VIAx.S.2	Space of VIAx [PRL > -0.020 μm] (Except SEALRING_ALL)	S2	\geq	0.0440
VIAx.S.2.1	Space of the short side of rectangular VIAx to VIAx [PRL > -0.020 μm]	S2A	\geq	0.0740
VIAx.S.2.2	Space of rectangular VIAx to VIAx (Except SEALRING_ALL)	S2B	\geq	0.0490
VIAx.S.2.5	Space of square VIAx [width = 0.038 μm] to VIAx	S2E	\geq	0.0590
VIAx.S.2.5.1	Space of square VIAx [width = 0.038 μm] to VIAx [PRL > -0.038 μm]	S2E1	\geq	0.0740
VIAx.S.8	Space to VIAx or VIAx-1 [maximum delta V > 0.96V]	S8	\geq	0.0620
VIAx.S.8.1	Space to VIAx or VIAx-1 [maximum delta V > 1.32V] (1.2V + 10%)	S8	\geq	0.0640
VIAx.S.8.2	Space to VIAx or VIAx-1 [maximum delta V > 1.65V] (1.5V + 10%)	S8	\geq	0.0700
VIAx.S.8.3	Space to VIAx or VIAx-1 [maximum delta V > 1.98V] (1.8V + 10%)	S8	\geq	0.0820
VIAx.S.8.4	Space to VIAx or VIAx-1 [maximum delta V > 2.75V] (2.5V + 10%)	S8	\geq	0.0870
VIAx.S.9	Space to {SRM (50;0) OR SRAMDMY (186;0)} ({VIAx CUT {SRM (50;0) OR SRAMDMY (186;0)}} is not allowed)	S9	\geq	0.0840
VIAx.S.9.1	Space of short side of rectangular VIAx to {SRM (50;0) OR SRAMDMY (186;0)} [PRL > -0.044 μm]	S9A	\geq	0.1340
VIAx.S.10.1	Space of SVxCA	S10A	\geq	0.0700
VIAx.S.10.2	Space of SVxCB	S10B	\geq	0.0700
VIAx.S.10.3	Space of {square VIAx NOT {SVxCA OR SVxCB}} to {SVxCA OR SVxCB} [PRL > -0.050 μm]	S10C	\geq	0.0940
VIAx.S.10.4	Corner-to-corner space of {square VIAx NOT {SVxCA OR SVxCB}} to {SVxCA OR SVxCB} [PRL \leq -0.050 μm]	S10D	\geq	0.0870
VIAx.S.10.5	Space of SVxCA [NOT INTERACT VACPL] [PRL > -0.050 μm] Definition of SVxCA CRITICAL PITCH LINE (VACPL) : The line with corner to corner space PS [0.070 μm \leq PS < 0.087 μm] between two square SVxCA [-0.0605 μm < PRL \leq -0.037 μm along one direction (X or Y), and -0.0865 μm < PRL \leq -0.060 μm along another direction (Y or X)]	S10E	\geq	0.0940
VIAx.S.10.6	Corner-to-corner space of SVxCA [NOT INTERACT VACPL] [PRL \leq -0.050 μm] Definition of SVxCA CRITICAL PITCH LINE (VACPL) : The line with corner to corner space PS [0.070 μm \leq PS < 0.087 μm] between two square SVxCA [-0.0605 μm < PRL \leq -0.037 μm along one direction (X or Y), and -0.0865 μm < PRL \leq -0.060 μm along another direction (Y or X)]	S10F	\geq	0.0870
VIAx.S.10.7	Space of SVxCB [NOT INTERACT VBCPL] [PRL > -0.050 μm] Definition of SVxCB CRITICAL PITCH LINE (VBCPL) : The line with corner to corner space PS [0.070 μm \leq PS < 0.087 μm] between two square SVxCB [-0.0605 μm < PRL \leq -0.037 μm along one direction (X or Y), and -0.0865 μm < PRL \leq -0.060 μm along another direction (Y or X)]	S10G	\geq	0.0940

Rule No.	Description	Label	Op.	Rule
VIAx.S.10.8	Corner-to-corner space of SVxCB [NOT INTERACT VBCPL] [PRL ≤ -0.050 μm] Definition of SVxCB CRITICAL PITCH LINE (VBCPL) : The line with corner to corner space PS [0.070 μm ≤ PS < 0.087 μm] between two square SVxCB [-0.0605 μm < PRL ≤ -0.037 μm along one direction (X or Y), and -0.0865 μm < PRL ≤ -0.060 μm along another direction (Y or X)]	S10H	≥	0.0870
VIAx.S.10.11	Space of SVxCA to SVxCA [INTERACT another VACPL] [PRL > -0.050 μm]	S10K	≥	0.0940
VIAx.S.10.12	Corner-to-corner space of SVxCA to SVxCA [INTERACT another VACPL] [PRL ≤ -0.050 μm]	S10L	≥	0.0870
VIAx.S.10.13	Space of SVxCB to SVxCB [INTERACT another VBCPL] [PRL > -0.050 μm]	S10M	≥	0.0940
VIAx.S.10.14	Corner-to-corner space of SVxCB to SVxCB [INTERACT another VBCPL] [PRL ≤ -0.050 μm]	S10N	≥	0.0870
VIAx.S.11	Space of the long side of rectangular VIAx [PRL > 0 μm (L1), with Mx+1 in between, and Mx+1 width < 0.024 μm]	S11	≥	0.0680
VIAx.S.12	Space of long side of rectangular VIAx [length = 0.050 μm] to {SVxCA OR SVxCB} [PRL > -0.105 μm]	S12	≥	0.0910
VIAx.S.12.1	Space of long side of rectangular VIAx [length = 0.050 μm] to {SVxCA OR SVxCB} [PRL > -0.073 μm]	S12A	≥	0.0950
VIAx.S.12.2	Space of short side of rectangular VIAx [length = 0.050 μm] to {SVxCA OR SVxCB} [PRL > -0.034 μm]	S12B	≥	0.1340
VIAx.S.15.1	Space of long side of L50VxCA to {square VIAx NOT VxCB} [PRL > -0.105 μm]	S15A	≥	0.0910
VIAx.S.15.2	Space of long side of L50VxCA to {square VIAx NOT VxCB} [PRL > -0.073 μm]	S15B	≥	0.0950
VIAx.S.15.3	Space of short side of L50VxCA to {square VIAx NOT VxCB} [PRL > -0.034 μm]	S15C	≥	0.1340
VIAx.S.15.4	Space of long side of L50VxCB to {square VIAx NOT VxCA} [PRL > -0.105 μm]	S15D	≥	0.0910
VIAx.S.15.5	Space of long side of L50VxCB to {square VIAx NOT VxCA} [PRL > -0.073 μm]	S15E	≥	0.0950
VIAx.S.15.6	Space of short side of L50VxCB to {square VIAx NOT VxCA} [PRL > -0.034 μm]	S15F	≥	0.1340
VIAx.S.15.7	Space of long side of L50VxCA to {SLVIAx OR SLVxCA} [PRL > -0.089 μm]	S15G	≥	0.1000
VIAx.S.15.8	Space of short side of L50VxCA to {SLVIAx OR SLVxCA} [PRL > -0.044 μm]	S15H	≥	0.1340
VIAx.S.15.9	Corner-to-corner space L50VxCA to {SLVIAx OR SLVxCA} [long side PRL ≤ -0.089 μm, short side ≤ -0.044 μm from L50VxCA]	S15I	≥	0.1340
VIAx.S.15.10	Space of long side of L50VxCB to {SLVIAx OR SLVxCB} [PRL > -0.089 μm]	S15J	≥	0.1000
VIAx.S.15.11	Space of short side of L50VxCB to {SLVIAx OR SLVxCB} [PRL > -0.044 μm]	S15K	≥	0.1340
VIAx.S.15.12	Corner-to-corner space L50VxCB to {SLVIAx OR SLVxCB} [long side PRL ≤ -0.089 μm, short side ≤ -0.044 μm from L50VxCB]	S15L	≥	0.1340
VIAx.S.18.1	Space of long side of L34VxCA to {VIAx NOT VxCB} [PRL > -0.093 μm]	S18A	≥	0.1000
VIAx.S.18.1.1	Space of long side of L34VIAx to {VxCA OR VxCB} [PRL > -0.093 μm]	S18A	≥	0.1000
VIAx.S.18.2	Space of short side of L34VxCA to {VIAx NOT VxCB} [PRL > -0.060 μm]	S18B	≥	0.1280
VIAx.S.18.2.1	Space of short side of L34VIAx to {VxCA OR VxCB} [PRL > -0.060 μm]	S18B	≥	0.1280
VIAx.S.18.3	Space of long side of L34Vxcb to {VIAx NOT VxCA} [PRL > -0.093 μm]	S18C	≥	0.1000
VIAx.S.18.4	Space of short side of L34Vxcb to {VIAx NOT VxCA} [PRL > -0.060 μm]	S18D	≥	0.1280
VIAx.S.19	Corner-to-corner space of L34VxCA to {SLVIAx OR SLVxCA} [long side PRL ≤ -0.093 μm, short side ≤ -0.060 μm from L34VxCA]	S19	≥	0.1340

Rule No.	Description	Label	Op.	Rule
VIAx.S.19.1	Corner-to-corner space of L34VxCB to {SLVIAx OR SLVxCB} [long side PRL ≤ -0.093 μm, short side ≤ -0.060 μm from L34VxCB]	S19A	≥	0.1340
VIAx.S.19.2	Corner-to-corner space of L34VIAx to {SLVxCA OR SLVxCB} [long side PRL ≤ -0.093 μm, short side ≤ -0.060 μm from L34VIAx]	S19B	≥	0.1340
VIAx.S.21	Space of S38VxCA to {VIAx NOT VxCB}	S21	≥	0.0920
VIAx.S.21.0.1	Space of S38VIAx to {VxCA OR VxCB}	S21	≥	0.0920
VIAx.S.21.1	Space of S38VxCA to {VIAx NOT VxCB} [PRL > -0.050 μm]	S21A	≥	0.1120
VIAx.S.21.1.1	Space of S38VIAx to {VxCA OR VxCB} [PRL > -0.050 μm]	S21A	≥	0.1120
VIAx.S.21.2	Space of S38VxCA to {VIAx NOT {VxCB OR S38VxCA}}	S21B	≥	0.1040
VIAx.S.21.2.1	Space of S38VIAx to {{VxCA OR VxCB} NOT {S38VxCA OR S38VxCB}}	S21B	≥	0.1040
VIAx.S.21.3	Space of S38VxCA to {SLVIAx OR SLVxCA}	S21C	≥	0.5000
VIAx.S.21.3.1	Space of square VIAx [width = 0.038 μm] to rectangular VIAx	S21C	≥	0.5000
VIAx.S.22	Space of S38VxCB to {VIAx NOT VxCA}	S22	≥	0.0920
VIAx.S.22.1	Space of S38Vxcb to {VIAx NOT VxCA} [PRL > -0.050 μm]	S22A	≥	0.1120
VIAx.S.22.2	Space of S38Vxcb to {VIAx NOT {VxCA OR S38Vxcb}}	S22B	≥	0.1040
VIAx.S.22.3	Space of S38Vxcb to {SLVIAx OR SLVxcb}	S22C	≥	0.5000
VIAx.EN.0	1. Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] is defined by RuleTable.VIAx.EN.32 in the subsection 2. Enclosure of square VIAx ($x > 2$) [width = 0.038 μm] is defined by RuleTable.VIAx.EN.37 in the subsection 3. Enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] is defined by RuleTable.VIAx.EN.34 in the subsection 4. Enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] is defined by RuleTable.VIAx.EN.38 in the subsection 5. Enclosure of square VIA2 [width = 0.020 μm] is defined by RuleTable.VIAx.EN.31 in the subsection 6. Enclosure of square VIA2 [width = 0.038 μm] is defined by RuleTable.VIAx.EN.35 in the subsection 7. Enclosure of rectangular VIA2 [length = 0.050 μm] is defined by RuleTable.VIAx.EN.33 in the subsection 8. Enclosure of rectangular VIA2 [length = 0.034 μm] is defined by RuleTable.VIAx.EN.36 in the subsection			
VIAx.EN.1.2.1	Enclosure of square VIAx by Mxs or Mx [width = 0.028 μm, INTERACT BCWDMY] with the other two sides $\geq 0.004 \mu m$ ($x \geq 3$)	EN1	≥	0.0300
VIAx.EN.1.2.2	Enclosure of square VIA2 by M2 [width = 0.028 μm, INTERACT BCWDMY] with the other two sides $\geq 0.004 \mu m$	EN1	≥	0.0280
VIAx.EN.1.8	Enclosure of square VIAx by Mxs or Mx [$0.080 \mu m \leq width < 0.260 \mu m$] with the other two sides $\geq 0.030 \mu m$ (Except following conditions: 1. Mxs or Mx [width = 0.120 μm] enclosure of square VIAx array) Definition of square VIAx array follows VIAx.EN.19	EN1H	≥	0.0200
VIAx.EN.16.10	Checked_VIAx_Edge1 enclosure by Mxs (32;400) or Mx in Mxs or Mx MINP direction (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2}) Definition of Checked_VIAx: VIAx INTERACT Mx+1 width > 0.040 μm Definition of Checked_VIAx_Edge1: 1. Checked_VIAx edge space to Mxs (32;400) or {MxCA OR MxCB} < 0.040 μm with PRL > -0.100 μm in Mxs or Mx MINP direction	EN16J	≥	0.0010

Rule No.	Description	Label	Op.	Rule
VIAx.EN.16.10.1	<p>Checked_VIAx_Edge2 enclosure by Mxs (32;400) or Mx in Mxs or Mx MINP direction (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})</p> <p>Definition of Checked_VIAx: VIAx INTERACT Mx+1 width > 0.040 μm</p> <p>Definition of Checked_VIAx_Edge2: 1. Checked_VIAx edge space to Mxs (32;400) or {MxCA OR MxCB} < 0.040 μm with PRL > -0.100 μm in Mxs or Mx MINP direction, and 2. Checked_VIAx edge space to VIAxs or VIAx-1 < 0.026 μm [PRL > 0, different net]</p>	EN16J	≥	0.0020
VIAx.EN.19	<p>Square VIAx array enclosure by Mxs or Mx [width = 0.120 μm] for two opposite sides with the other two sides [Square VIAx array edge length = 0.020 μm] ≥ 0.018 μm</p> <p>Definition of square VIAx array: VIAx space = 0.044 μm [PRL = 0.020 μm] in Mxs or Mx MINP direction</p>	EN19	≥	0.0300
VIAx.EN.21.6.1	Short side enclosure of rectangular VIAx by Mxs or Mx [width = 0.028 μm, INTERACT BCWDMY] with the other two long side enclosure ≥ 0.004 μm (x ≥ 3)	EN21D	≥	0.0300
VIAx.EN.21.6.2	Short side enclosure of rectangular VIA2 by M2 [width = 0.028 μm, INTERACT BCWDMY] with the other two long side enclosure ≥ 0.004 μm	EN21D	≥	0.0280
VIAx.EN.21.10	Short side enclosure of rectangular VIAx by Mxs or Mx edge [length = 0.080 μm, Mxs/Mx width = 0.080 μm]	EN21D	≥	0.0250
VIAx.L.1	Length of VIAx [width = 0.020 μm]	L1	=	0.0200, 0.0340, 0.0500
VIAx.L.2	Length of VIAx [width = 0.038 μm]	L2	=	0.0380
VIAx.R.0	45-degree VIAx is not allowed			
VIAx.R.2	<p>Redundant via requirement must follow RuleTable.VIAx.R.2 of VIAx numbers and space (S1) for Mx and Mx+1 connection. [One of Mx or Mx+1 has width and length (W1) > 0.160 μm].</p> <p>(Except following conditions: 1. VIA bar)</p>			
VIAx.R.2.1	<p>Redundant via requirement must follow RuleTable.VIAx.R.2.1 of VIAx numbers and space (S1) for Mx and Mx+1 connection. [One of Mx or Mx+1 has width and length (W1) > 0.300 μm].</p> <p>(Except following conditions: 1. VIA bar)</p>			
VIAx.R.3	<p>Redundant via requirement must follow RuleTable.VIAx.R.3 of VIAx numbers and space (S1) for Mx and Mx+1 connection. [One of Mx or Mx+1 has width and length (W1) > 0.412 μm].</p> <p>(Except following conditions: 1. VIA bar)</p>			
VIAx.R.7	VIAx must be fully covered by {{Mxs OR Mx} AND Mx+1}			
VIAx.R.9®	Recommended maximum consecutive stacked VIAx layer, which has only one via for each VIAx layer to avoid high Rc		≤	4

Rule No.	Description	Label	Op.	Rule
VIAx.R.10	Overlap MetalFuse_B1 (156;8) is not allowed			
VIAx.R.13	Maximum area ratio of M1 to upper VIAx in the same net [connects to gate with area > 10700 μm^2 , and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = $(2.5 \times WdxLd)$ for ≥ 2 -fin device		\leq	350000
VIAx.R.13.2	Maximum area ratio of I/O gate to single layer VIAx in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area $\geq 0.25 \mu\text{m}^2$) Definition: Gate area = $(2.5 \times WdxLd)$ for ≥ 2 -fin device		\leq	300000
VIAx.R.19	Isolated VIAx is not allowed. (Except SEALRING_ALL) DRC flags VIAx without neighboring {VIAx OR DVIAx} distance $\leq 4 \mu\text{m}$			
VIAx.R.21	VIAx interact VIAx_Empty_Space_100 is not allowed in chip level (Except following conditions: 1. INDDMY, SEALRING_ALL for VIAx_Empty_Space_100) Definition of VIAx_Empty_Space_100: {CHIP NOT {VIAx OR DVIAx}} SIZING down/up 50 μm			
VIAx.R.21.1	VIAx interact VIAx_Empty_Space_50 is not allowed in cell level (Except following conditions: 1. INDDMY for VIAx_Empty_Space_50) Definition of VIAx_Empty_Space_50: {CHIP NOT {VIAx OR DVIAx}} SIZING down/up 25 μm			
VIAx.R.22	VIAx_GroupA space to two or more {VIAx NOT VxCB} $< 0.100 \mu\text{m}$ [PRL $> 0 \mu\text{m}$] is not allowed Definition of VIAx_GroupA: VIAx interact VACPL Definition of SVxCA CRITICAL PITCH LINE (VACPL) : The line with corner to corner space PS [$0.070 \mu\text{m} \leq PS < 0.087 \mu\text{m}$] between two square SVxCA [-0.0605 $\mu\text{m} < PRL \leq -0.037 \mu\text{m}$ along one direction (X or Y), and $-0.0865 \mu\text{m} < PRL \leq -0.060 \mu\text{m}$ along another direction (Y or X)]			
VIAx.R.22.1	VIAx_GroupB space to two or more {VIAx NOT VxCA} $< 0.100 \mu\text{m}$ [PRL $> 0 \mu\text{m}$] is not allowed Definition of VIAx_GroupB: VIAx interact VBCPL Definition of SVxCB CRITICAL PITCH LINE (VBCPL) : The line with corner to corner space PS [$0.070 \mu\text{m} \leq PS < 0.087 \mu\text{m}$] between two square SVxCB [-0.0605 $\mu\text{m} < PRL \leq -0.037 \mu\text{m}$ along one direction (X or Y), and $-0.0865 \mu\text{m} < PRL \leq -0.060 \mu\text{m}$ along another direction (Y or X)]			

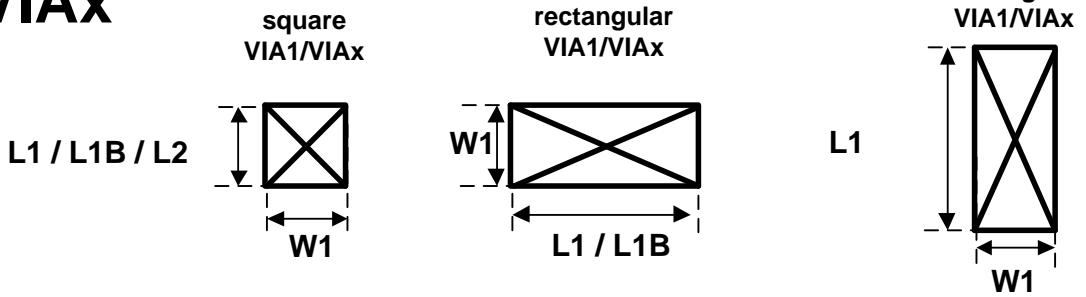
Rule No.	Description	Label	Op.	Rule
VIAx.G0.0.0	<p>Define Pre-coloring marker of VIAx :</p> <p>Define SVxCA (VIAx;255) and SVxCB (VIAx;256) to be the pre-coloring marker of square VIAx [width/length = 0.020/0.020 μm]</p> <p>Define S38VxCA (VIAx;255) and S38VxCB (VIAx;256) to be the pre-coloring marker of square VIAx [width/length = 0.038/0.038 μm]</p> <p>Define L34VxCA (VIAx;255) and L34VxCB (VIAx;256) to be the pre-coloring marker of rectangular VIAx [width/length = 0.020/0.034 μm]</p> <p>Define L50VxCA (VIAx;255) and L50VxCB (VIAx;256) to be the pre-coloring marker of rectangular VIAx [width/length = 0.020/0.050 μm]</p> <p>Define SVIAx = {square VIAx [width/length = 0.020/0.020 μm] NOT {SVxCA OR SVxCB}}</p> <p>Define S38VIAx = {square VIAx [width/length = 0.038/0.038 μm] NOT {S38VxCA OR S38VxCB}}</p> <p>Define L34VIAx = {rectangular VIAx [width/length = 0.020/0.034 μm] NOT {L34VxCA OR L34VxCB}}</p> <p>Define L50VIAx = {rectangular VIAx [width/length = 0.020/0.050 μm] NOT {L50VxCA OR L50VxCB}}</p> <p>Define SLVIAx = {L34VIAx OR L50VIAx}</p> <p>Define VxCA = {{SVxCA OR S38VxCA} OR L34VxCA} OR L50VxCA}</p> <p>Define VxCB = {{SVxCB OR S38VxCB} OR L34VxCB} OR L50VxCB}</p> <p>Define NCVIAx = {VIAx NOT {VxCA OR Vxcb}}</p> <p>Define SLVxCA = {L34VxCA OR L50VxCA}</p> <p>Define SLVxCB = {L34VxCB OR L50VxCB}</p>			

Rule No.	Description	Label	Op.	Rule
VIAx.G0.0.1	<p>G0-SPACE definition of VIAx ($x \geq 2$):</p> <p>Pre-colored marker VxCA and VxCB is for assigning the color of VIAx, and definition follow VIAx.G0.0.0</p> <ol style="list-style-type: none"> 1. G0 space (G0S) of SVIAx $< 0.094 \mu\text{m}$ [PRL $> -0.050 \mu\text{m}$] 2. G0 corner-to-corner space (G0CS) of SVIAx $< 0.087 \mu\text{m}$ [PRL $\leq -0.050 \mu\text{m}$] 3. G0 space (G0S) of long side of L50VIAx to SVIAx $< 0.095 \mu\text{m}$ [PRL $> -0.073 \mu\text{m}$] 4. G0 space (G0S) of long side of L50VIAx to SVIAx $< 0.091 \mu\text{m}$ [PRL $> -0.105 \mu\text{m}$] 5. G0 space (G0S) of long side of L50VIAx to SLVIAx $< 0.100 \mu\text{m}$ [PRL $> -0.089 \mu\text{m}$] 6. G0 space (G0S) of short side of L50VIAx to SVIAx $< 0.134 \mu\text{m}$ [PRL $> -0.034 \mu\text{m}$] 7. G0 space (G0S) of short side of L50VIAx to SLVIAx $< 0.134 \mu\text{m}$ [PRL $> -0.044 \mu\text{m}$] 8. G0 corner-to-corner space (G0CS) of L50VIAx to SLVIAx $< 0.134 \mu\text{m}$ [long side PRL $\leq -0.089 \mu\text{m}$, short side $\leq -0.044 \mu\text{m}$ from L50VIAx] 9. G0 space (G0S) of S38VIAx to NCVIAx $< 0.092 \mu\text{m}$ 10. G0 space (G0S) of S38VIAx to NCVIAx $< 0.112 \mu\text{m}$ [PRL $> -0.050 \mu\text{m}$] 11. G0 space (G0S) of S38VIAx to SVIAx $< 0.104 \mu\text{m}$ 12. G0 space (G0S) of S38VIAx to SLVIAx $< 0.500 \mu\text{m}$ 13. G0 space of long side of L34VIAx to NCVIAx $< 0.100 \mu\text{m}$ [PRL $> -0.093 \mu\text{m}$] 14. G0 space of short side of L34VIAx to NCVIAx $< 0.128 \mu\text{m}$ [PRL $> -0.060 \mu\text{m}$] 15. G0 corner-to-corner space (G0CS) of L34VIAx to SLVIAx $< 0.134 \mu\text{m}$ [long side PRL $\leq -0.093 \mu\text{m}$, short side $\leq -0.060 \mu\text{m}$ from L34VIAx] <p>G0 SPACE LINE definition:</p> <ol style="list-style-type: none"> 1. G0 SPACE LINE (G0SL): The line between two VIAxs with G0S and G0CS 2. G0SLs are independent to all other ones, even if they are overlapped or crossed <p>Loop:</p> <ol style="list-style-type: none"> 1. A loop is formed when VIAx polygons are connected in a cyclic sequence with G0SLs in between 2. A loop cannot contain any sub-loops which share one or more polygons with it <p>Odd loop: G0SL count of the closed loop formed by original polygons and G0SLs is odd number</p>			
VIAx.G0.1	G0SL cannot cross another G0SL or touch another G0SL s			
VIAx.G0.2	G0SL count of the closed loop formed by original polygons and G0SL s cannot be odd number			
VIAx.G0.4	VxCA and VxCB must be drawn identically to VIAx			
VIAx.G0.9	VxCA interact VxCB is not allowed			
VIAx.G0.10	VACPL cannot cross another VACPL			
VIAx.G0.10.1	VBCPL cannot cross another VBCPL			
VIAx.G0.10.2	A VxCA INTERACT VACPL number > 1 is not allowed			
VIAx.G0.10.3	A Vxcb INTERACT VBCPL number > 1 is not allowed			

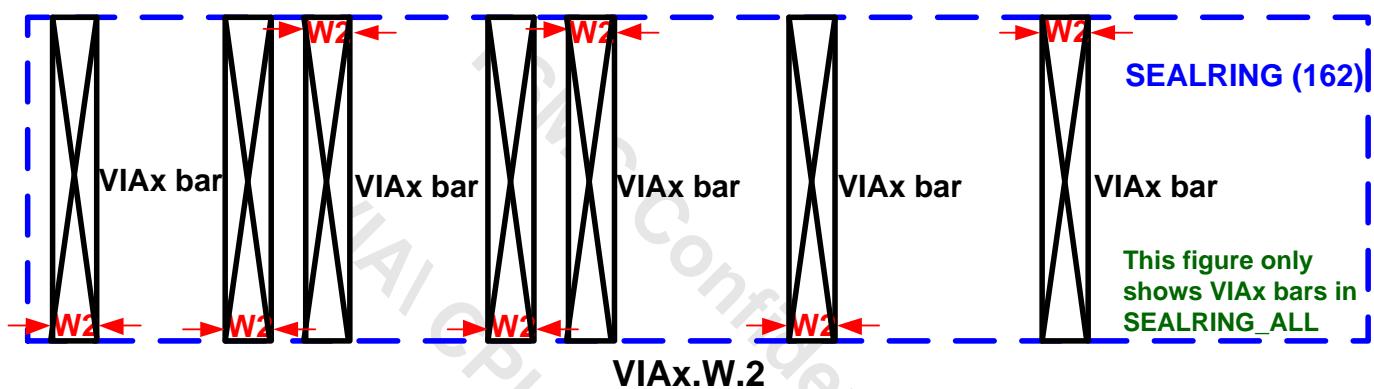
Table Notes:

- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

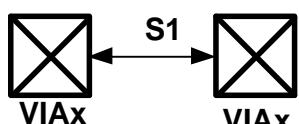
VIAx



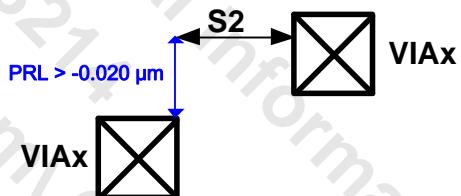
VIAx.W.1 / VIAx.L.1 / VIAx.L.2



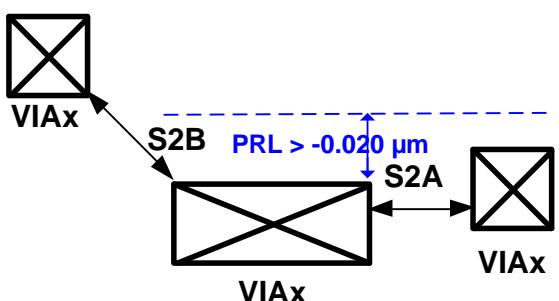
This figure only shows VIAx bars in SEAL RING ALL



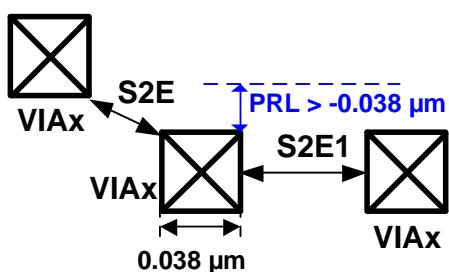
VIAx.S.1



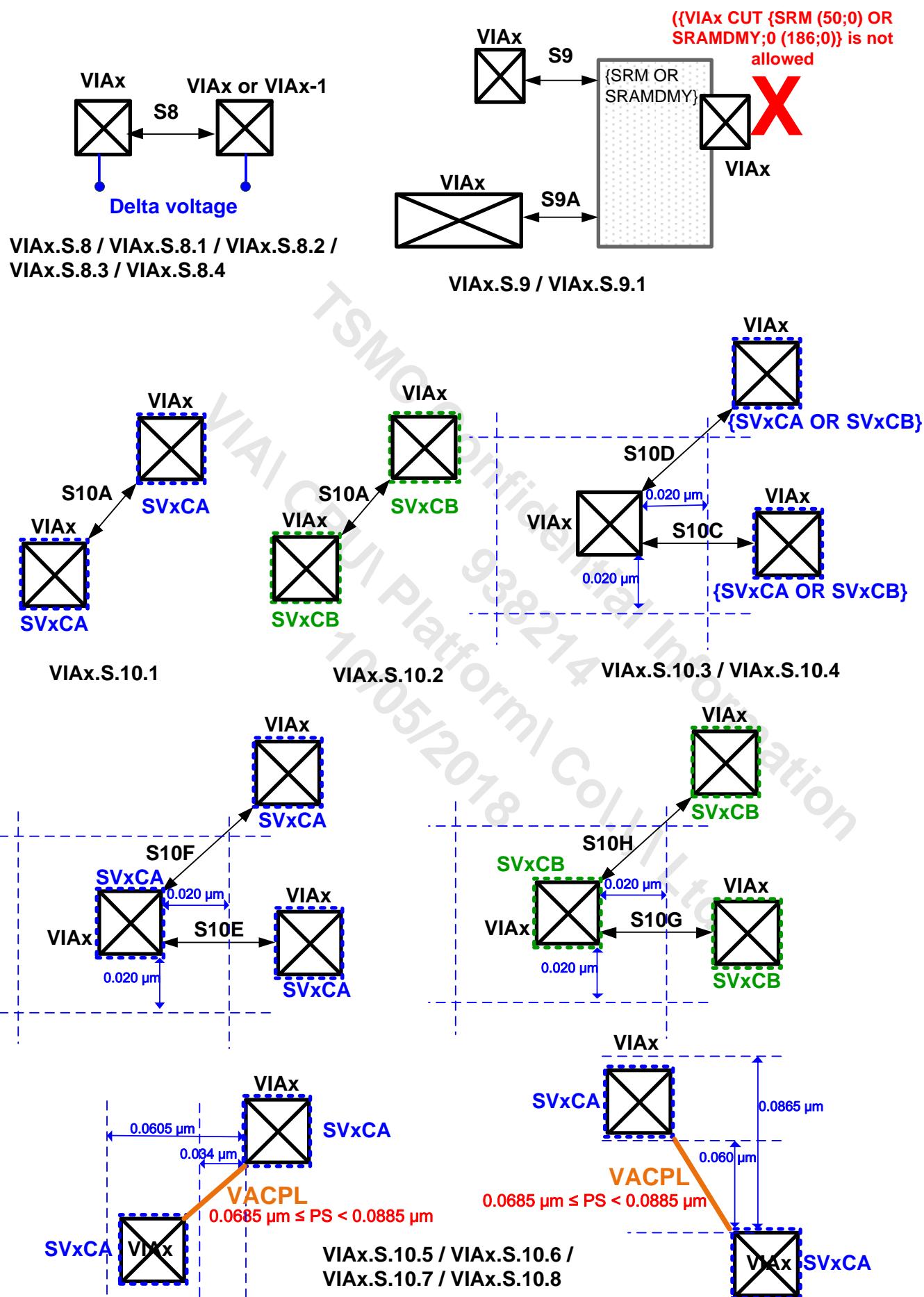
VIAx-S-2

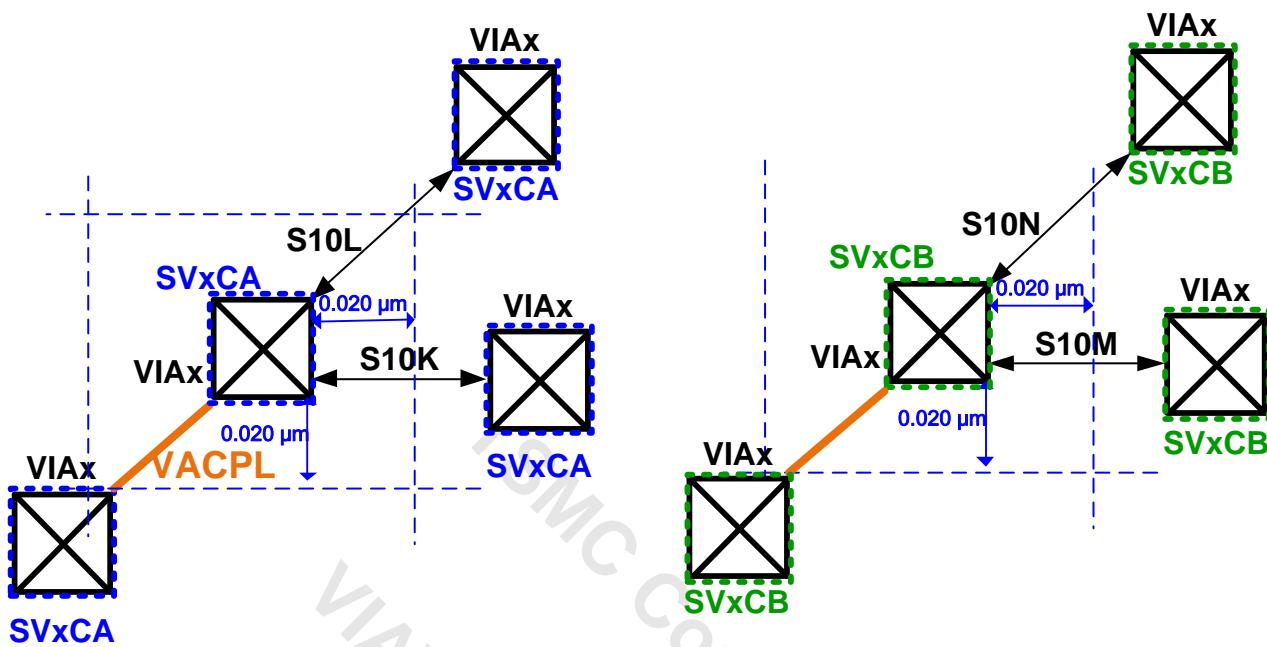


VIAx.S.2.1 / VIAx.S.2.2



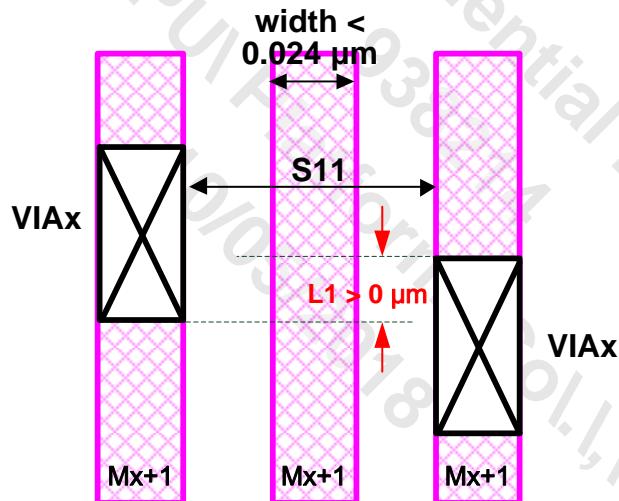
VIAx.S.2.5 / VIAx.S.2.5.1



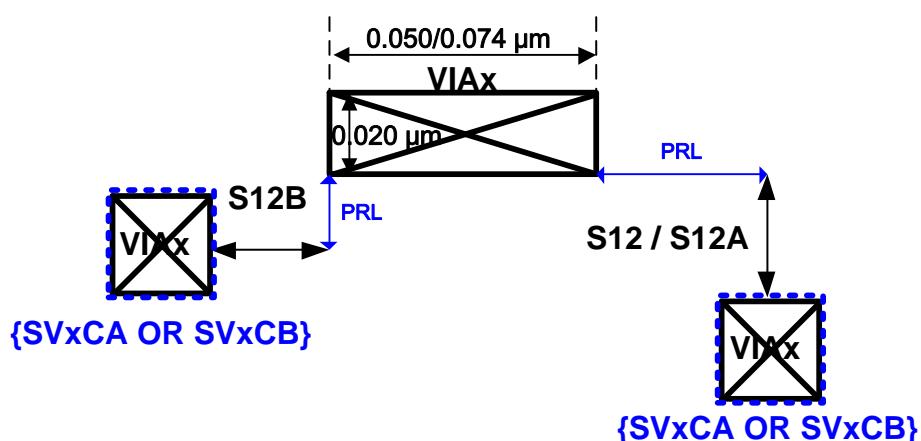


VIAx.S.10.11 / VIAx.S.10.12

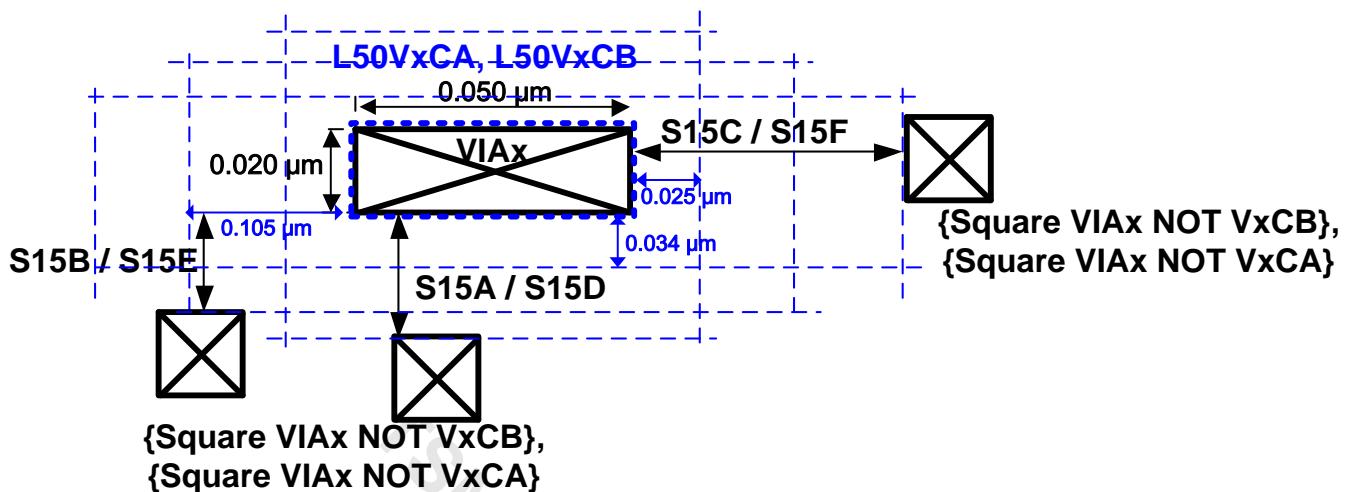
VIAx.S.10.13 / VIAx.S.10.14



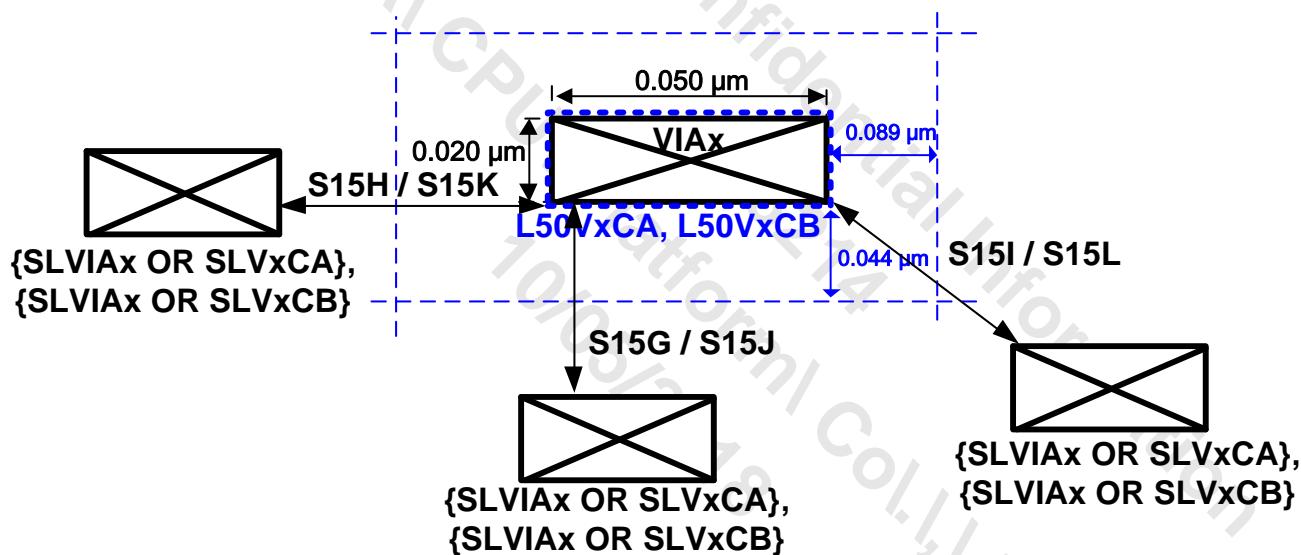
VIAx.S.11



VIAx.S.12 / VIAx.S.12.1 / VIAx.S.12.2

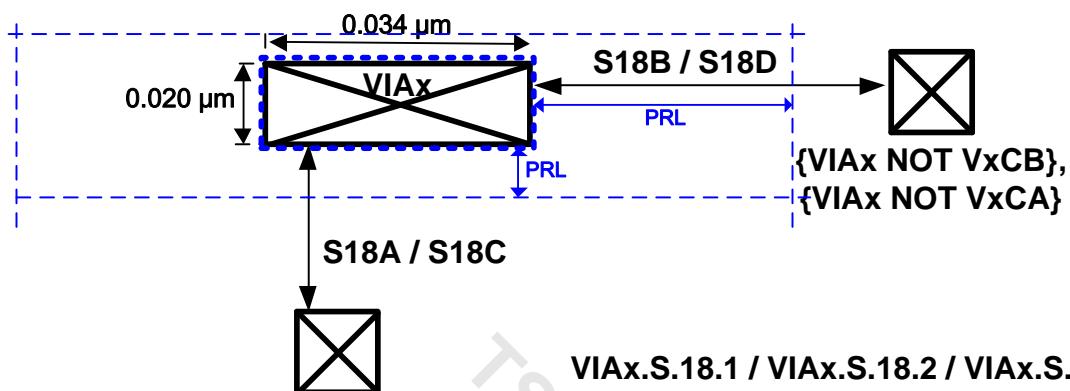


VIAx.S.15.1 / VIAx.S.15.2 / VIAx.S.15.3 /
VIAx.S.15.4 / VIAx.S.15.5 / VIAx.S.15.6

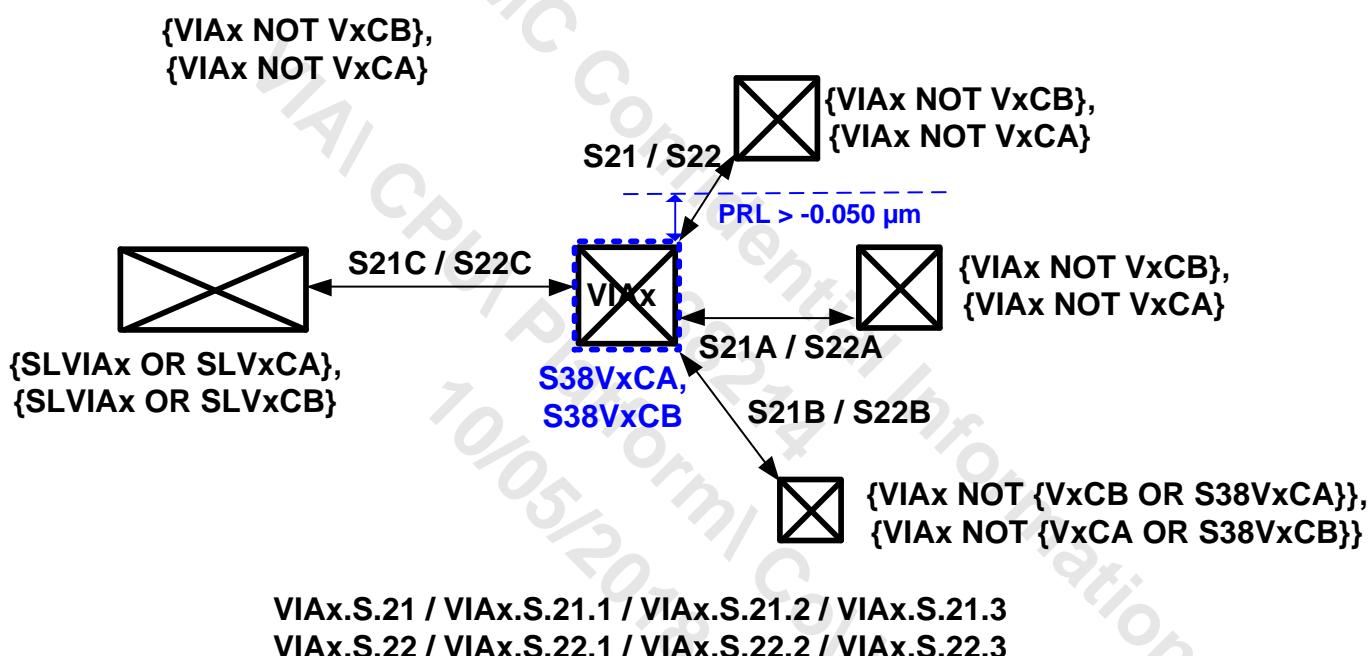
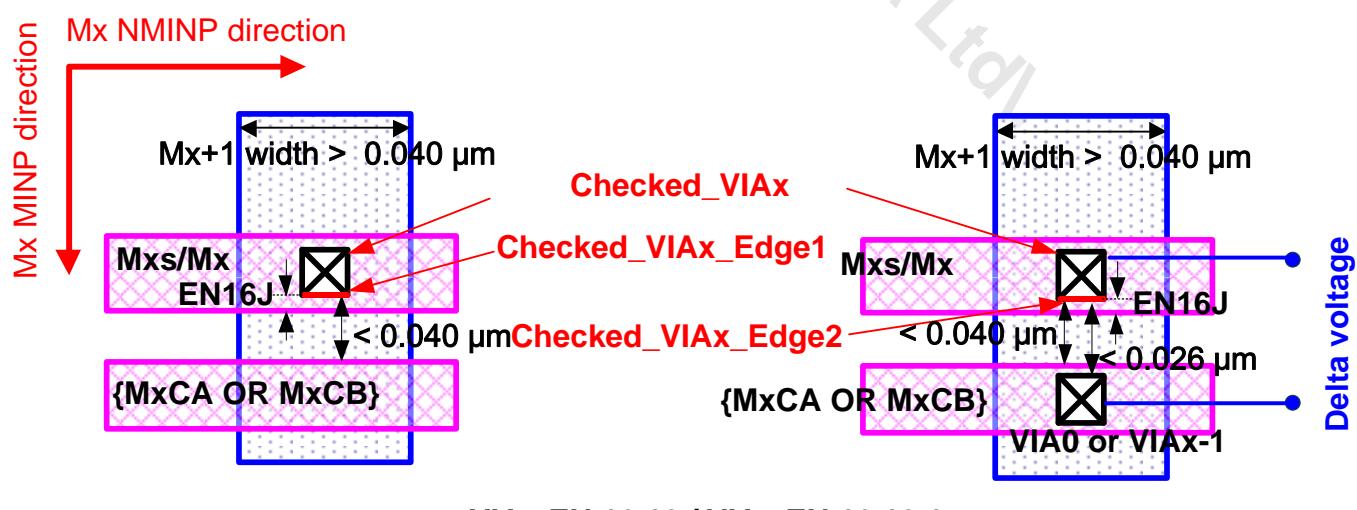


VIAx.S.15.7 / VIAx.S.15.8 / VIAx.S.15.9 /
VIAx.S.15.10 / VIAx.S.15.11 / VIAx.S.15.12

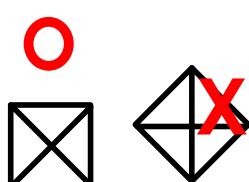
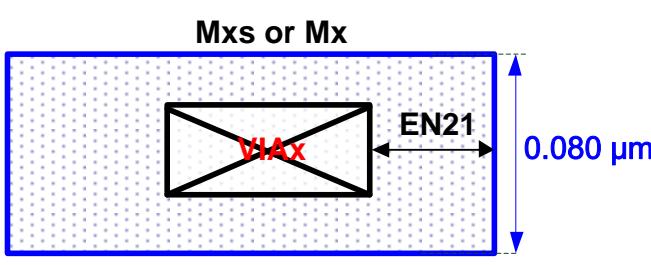
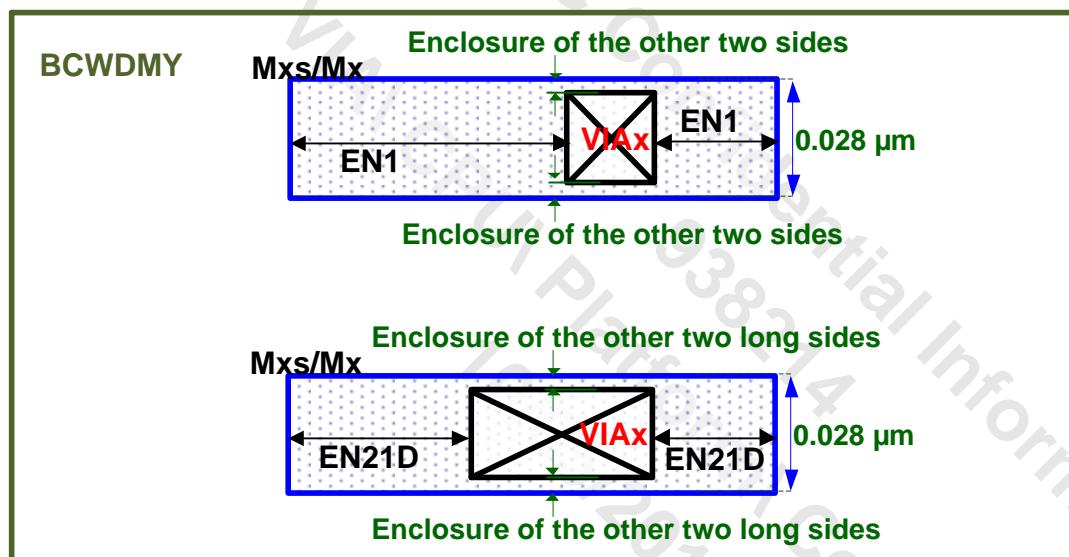
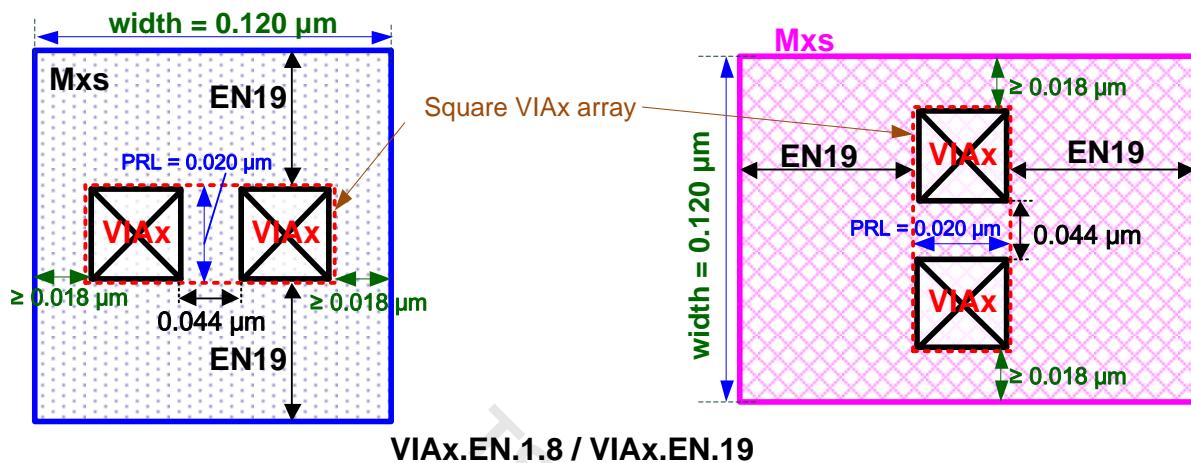
L34VxCA, L34VxCB



VIAx.S.18.1 / VIAx.S.18.2 / VIAx.S.18.3 / VIAx.S.18.4

VIAx.S.21 / VIAx.S.21.1 / VIAx.S.21.2 / VIAx.S.21.3
VIAx.S.22 / VIAx.S.22.1 / VIAx.S.22.2 / VIAx.S.22.3

VIAx.EN.16.10 / VIAx.EN.16.10.1



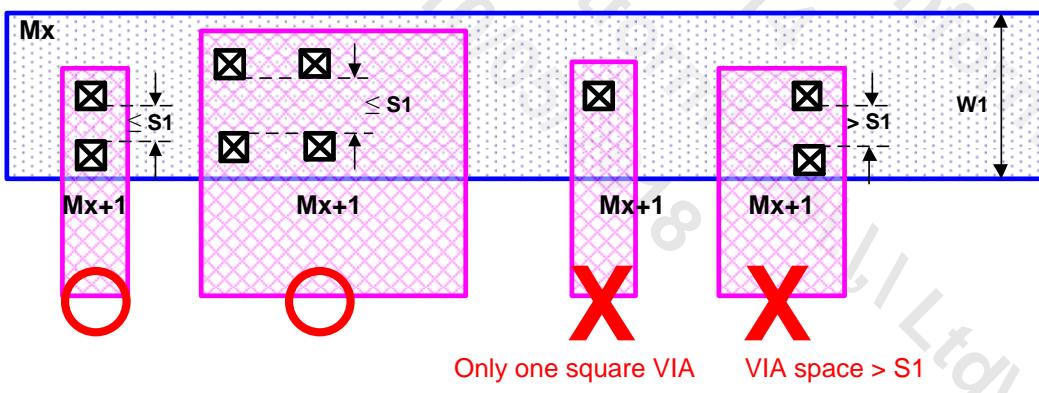
45-degree VIAx is
not allowed.

VIAx.R.0

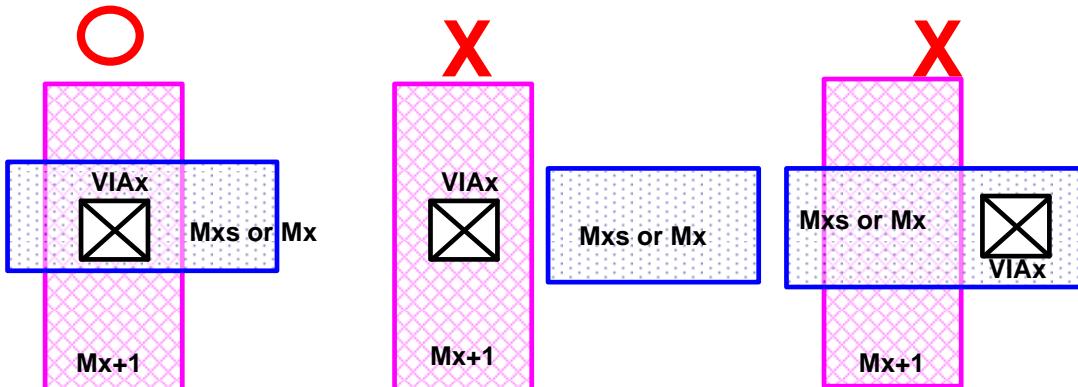
RuleTable.VIAx.R.2			$0.160 \mu\text{m} < W1 \leq 0.300 \mu\text{m}$							
VIAx space (S1) (μm)			$0.070 \leq S1 \leq 0.160$			$0.160 < S1 \leq 0.400$				
{Rectangular VIAx [width/length = 0.020/0.050 μm] OR square VIAx [width = 0.038 μm] (#)}	0	1				0	1	2		
{Square VIAx [width = 0.020 μm] OR rectangular VIAx [width/length = 0.020/0.034 μm] (#)}	≥ 2	≥ 0				≥ 4	≥ 2	≥ 0		

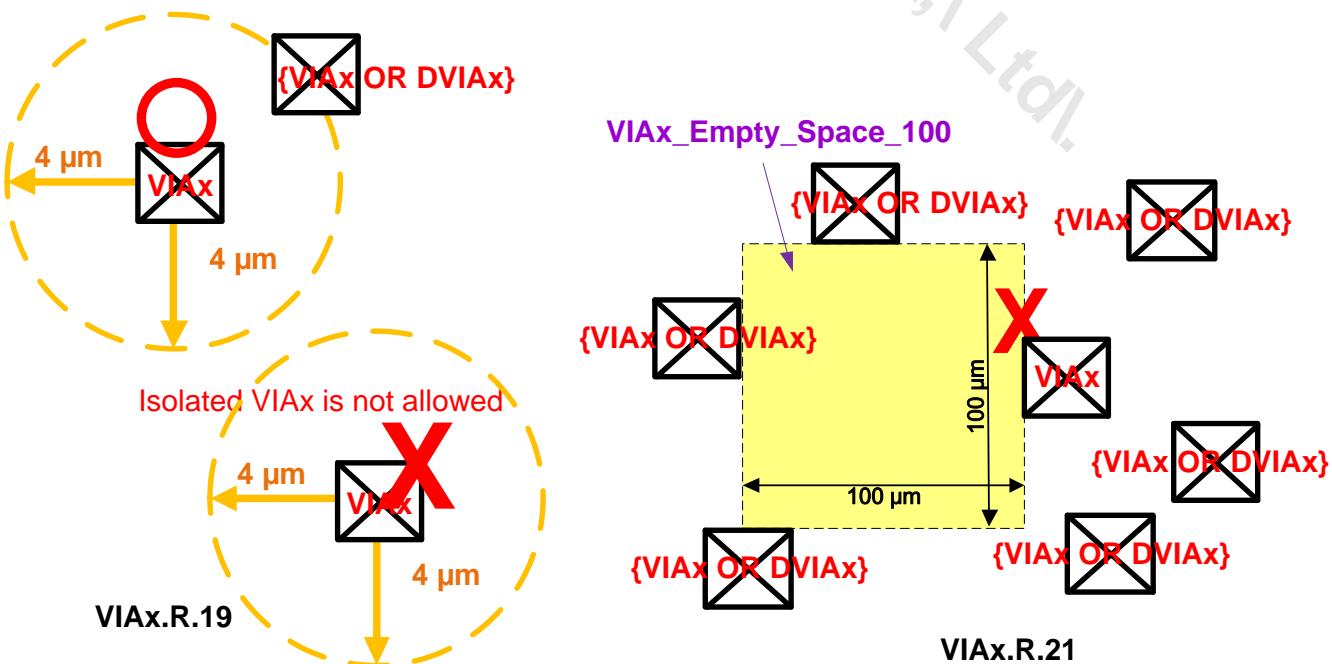
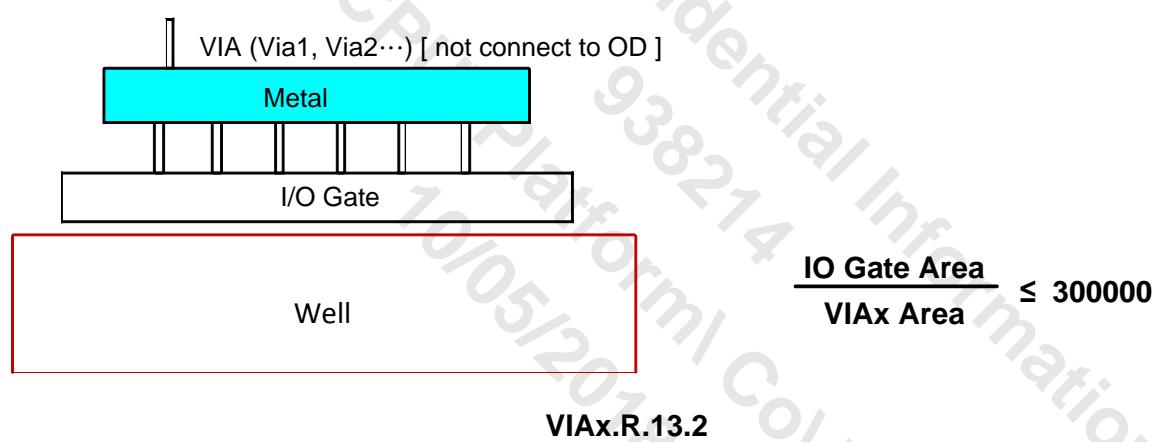
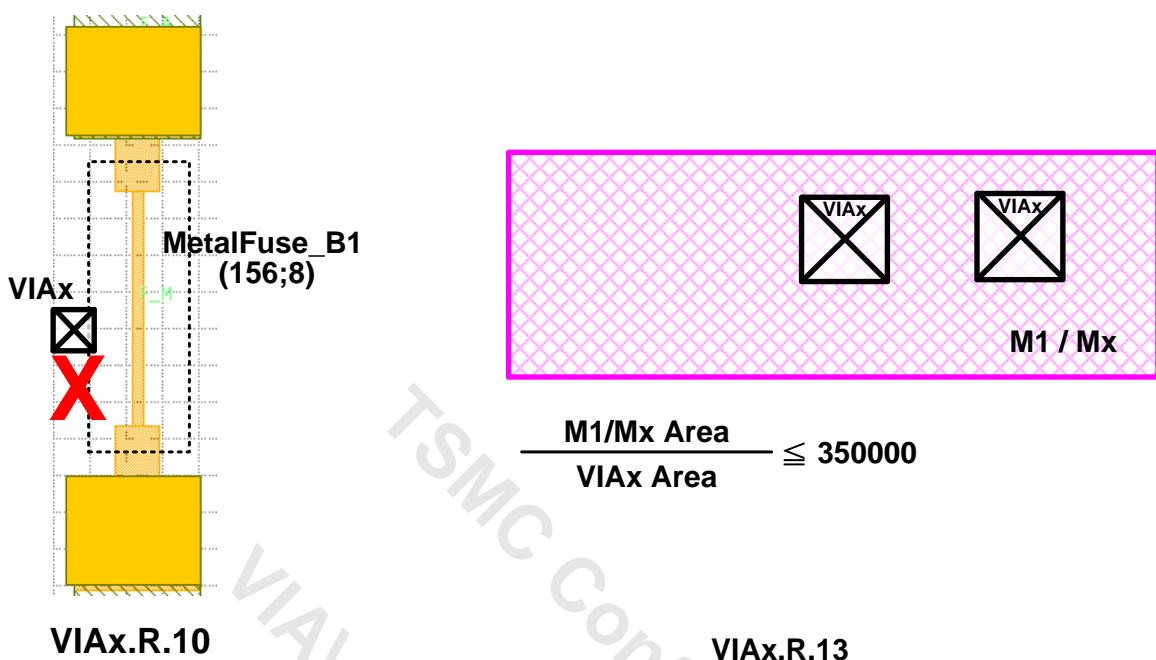
RuleTable.VIAx.R.2.1			$0.300 \mu\text{m} < W1 \leq 0.412 \mu\text{m}$							
VIAx space (S1) (μm)			$0.070 \leq S1 \leq 0.160$			$0.160 < S1 \leq 0.400$				
{Rectangular VIAx [width/length = 0.020/0.050 μm] OR square VIAx [width = 0.038 μm] (#)}	0	1	2			0	1	2	3	
{Square VIAx [width = 0.020 μm] OR rectangular VIAx [width/length = 0.020/0.034 μm] (#)}	≥ 3	≥ 1	≥ 0	≥ 6	≥ 4	≥ 2	≥ 0			

RuleTable.VIAx.R.3			$W1 > 0.412 \mu\text{m}$							
VIAx space (S1) (μm)			$0.070 \leq S1 \leq 0.160$			$0.160 < S1 \leq 0.400$				
{Rectangular VIAx [width/length = 0.020/0.050 μm] OR square VIAx [width = 0.038 μm] (#)}	0	1	2			0	1	2	3	4
{Square VIAx [width = 0.020 μm] OR rectangular VIAx [width/length = 0.020/0.034 μm] (#)}	≥ 4	≥ 2	≥ 0	≥ 9	≥ 7	≥ 5	≥ 3	≥ 1	≥ 0	

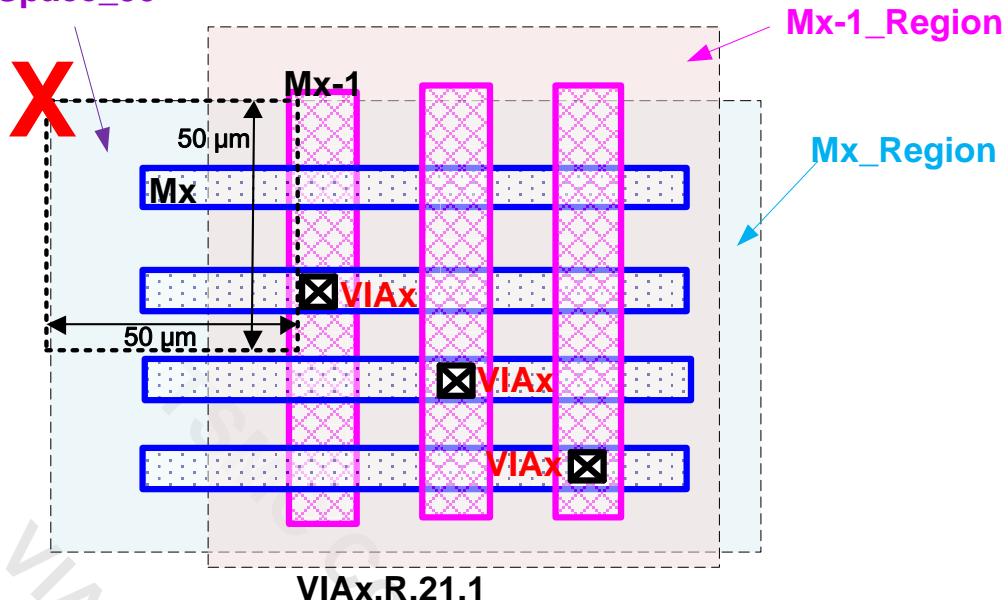


VIAx.R.2 / VIAx.R.2.1 / VIAx.R.3





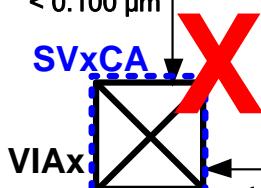
VIAx_Empty_Space_50



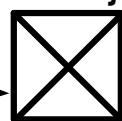
{VIAx NOT VxCB}

< 0.100 μm

SVxCA



{VIAx NOT VxCB}



VIAx

VACPL



SVxCA

VIAx.R.22

{VIAx NOT VxCA}

< 0.100 μm

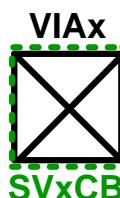
SVxCB



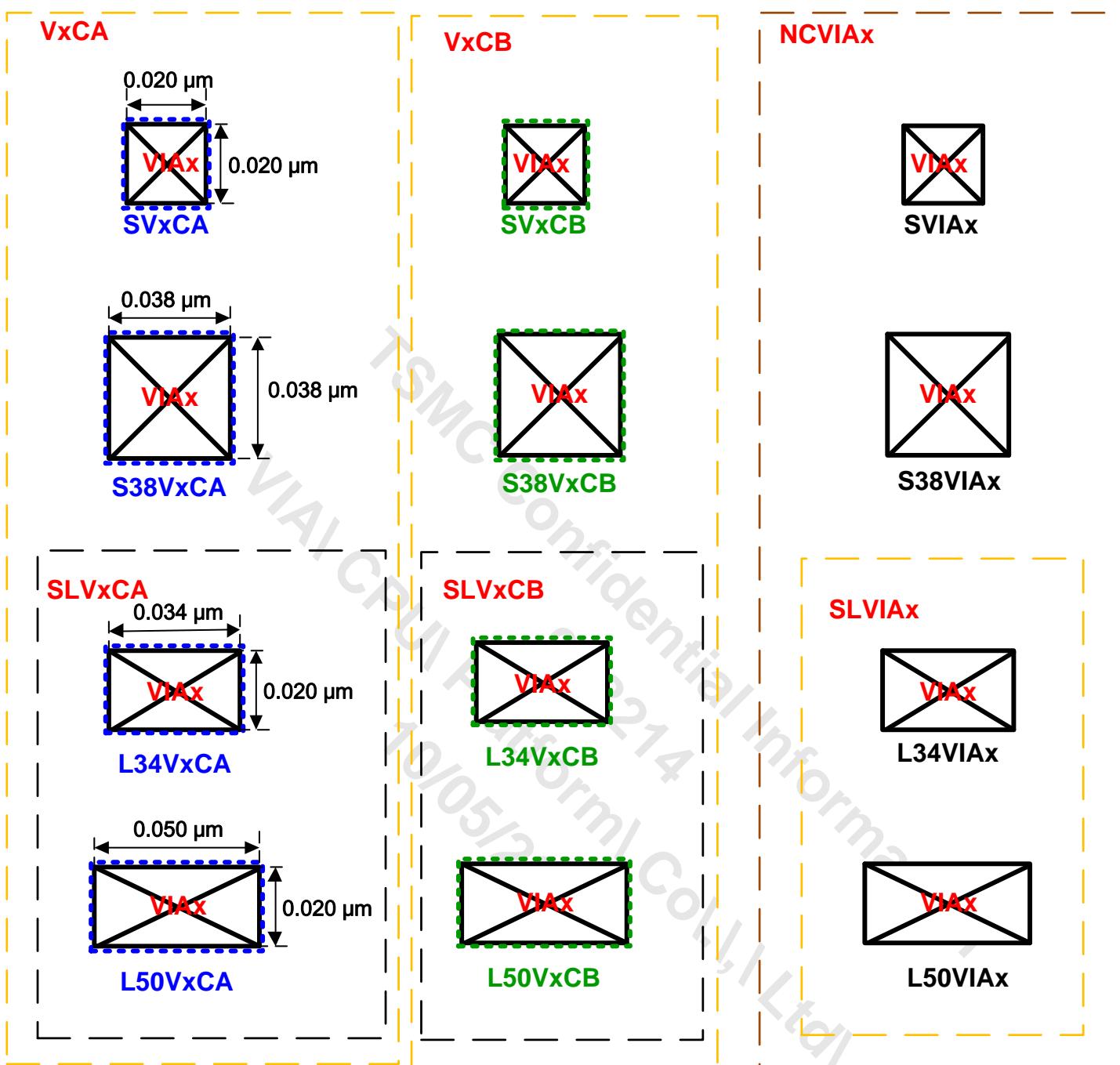
{VIAx NOT VxCA}



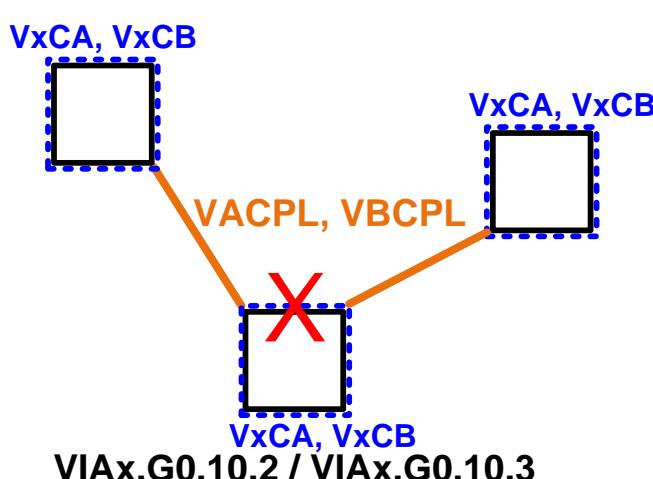
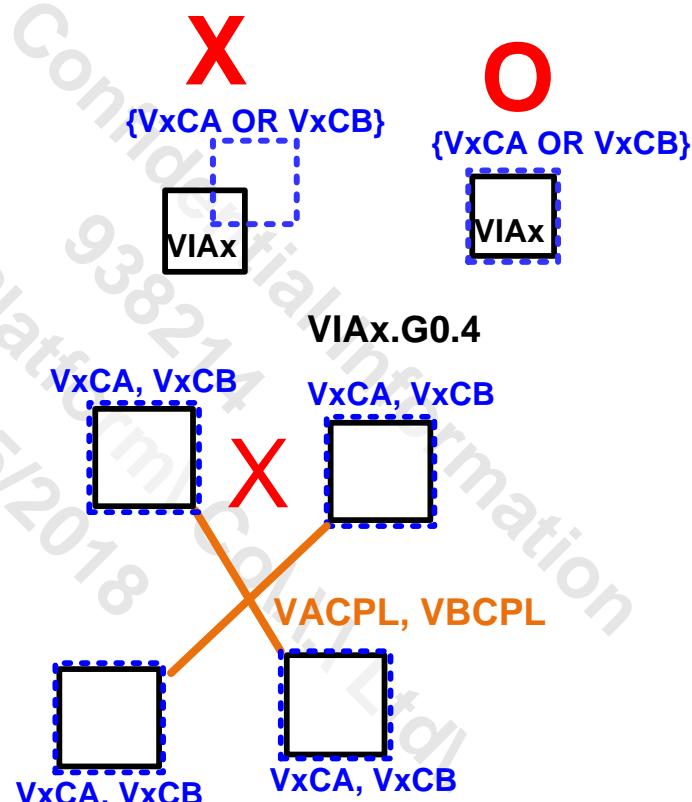
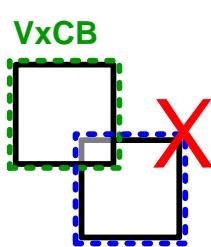
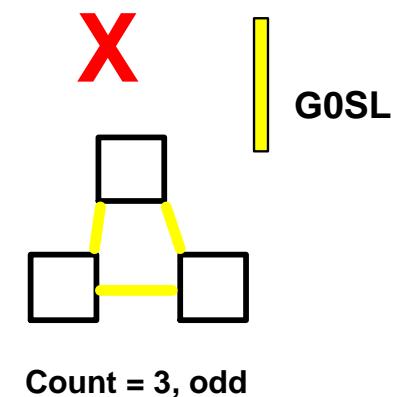
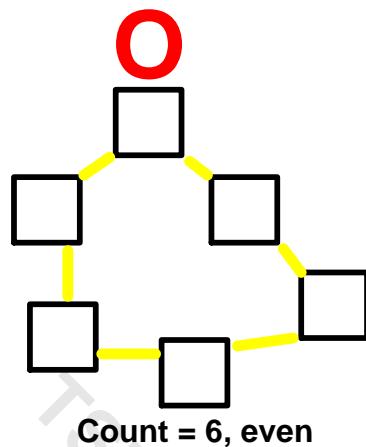
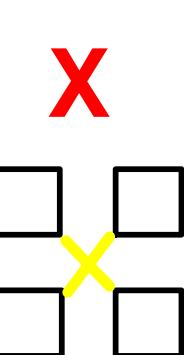
VIAx



VIAx.R.22.1



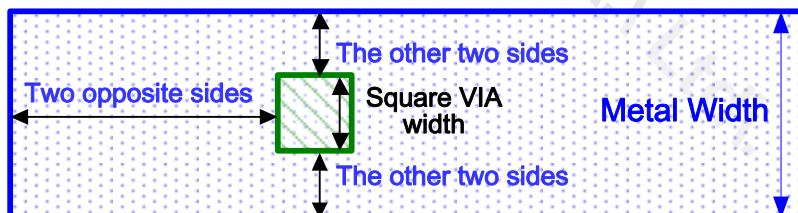
VIAx.G0.0.0 / VIAx.G0.0.1 / VIAx.G0.0.2



4.5.46.1 VIAx (x = 2) Enclosure Rule Tabulation

RuleTable.VIAx.EN.31 (Enclosure of square VIAx (x = 2) [width = 0.020 μm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAx.EN.31.1.T	width < 0.022 μm	0.0280 μm	0 μm	
VIAx.EN.31.2.T	0.022 μm ≤ width < 0.024 μm	0.0280 μm	0.0010 μm	
VIAx.EN.31.3.T	0.024 μm ≤ width < 0.028 μm	0.0280 μm	0.0020 μm	
VIAx.EN.31.4.T	0.028 μm ≤ width < 0.040 μm	0.0280 μm	0.0020 μm	
VIAx.EN.31.5	0.040 μm ≤ width < 0.060 μm	0.0280 μm	0.0100 μm	following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2}
VIAx.EN.31.5.1.T	0.040 μm ≤ width < 0.060 μm	0.0100 μm	0.0070 μm	
VIAx.EN.31.6.T	0.060 μm ≤ width < 0.080 μm	0.0250 μm	0.0200 μm	
VIAx.EN.31.7.T	0.080 μm ≤ width < 0.260 μm	0.0180 μm	0.0300 μm	
VIAx.EN.31.8.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	

RuleTable.VIAx.EN.35 (Enclosure of square VIAx (x = 2) [width = 0.038 μm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAx.EN.35.1.T	width < 0.060 μm	0.0590 μm	0.0010 μm	
VIAx.EN.35.2.T	0.060 μm ≤ width < 0.080 μm	0.0500 μm	0.0110 μm	
VIAx.EN.35.3.T	0.080 μm ≤ width < 0.100 μm	0.0430 μm	0.0210 μm	
VIAx.EN.35.4.T	0.100 μm ≤ width < 0.120 μm	0.0430 μm	0.0310 μm	
VIAx.EN.35.5.T	0.120 μm ≤ width < 0.260 μm	0.0400 μm	0.0400 μm	
VIAx.EN.35.6.T	width ≥ 0.260 μm	0.0600 μm	0.0500 μm	

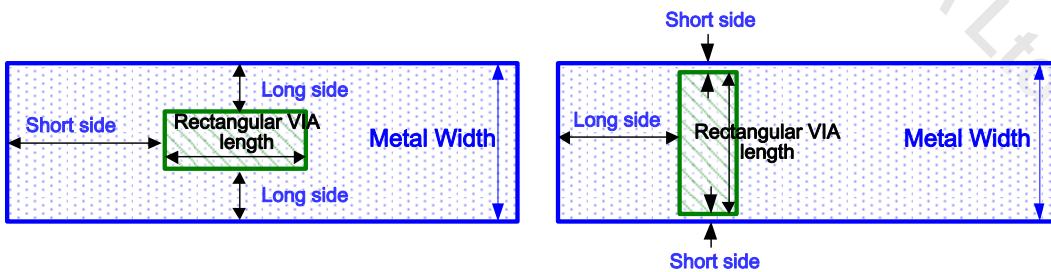


RuleTable.VIAx.EN.33 (Enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAx.EN.33.1.T	width < 0.022 μm	0.0280 μm	0 μm	
VIAx.EN.33.2.T	0.022 $\mu\text{m} \leq$ width < 0.024 μm	0.0280 μm	0.0010 μm	
VIAx.EN.33.3.T	0.024 $\mu\text{m} \leq$ width < 0.028 μm	0.0280 μm	0.0020 μm	
VIAx.EN.33.4.T	0.028 $\mu\text{m} \leq$ width < 0.040 μm	0.0280 μm	0.0020 μm	
VIAx.EN.33.5.T	0.040 $\mu\text{m} \leq$ width < 0.060 μm	0.0280 μm	0.0100 μm	
VIAx.EN.33.6.T	0.060 $\mu\text{m} \leq$ width < 0.070 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAx.EN.33.7.T	0.070 $\mu\text{m} \leq$ width < 0.080 μm	0.0250/0.0100 μm	0.0200/0.0300 μm	
VIAx.EN.33.8.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIAx.EN.33.9	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2}

RuleTable.VIAx.EN.36 (Enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAx.EN.36.1.T	width < 0.022 μm	0.0280 μm	0 μm	
VIAx.EN.36.2.T	0.022 $\mu\text{m} \leq$ width < 0.024 μm	0.0280 μm	0.0010 μm	
VIAx.EN.36.3.T	0.024 $\mu\text{m} \leq$ width < 0.028 μm	0.0280 μm	0.0020 μm	
VIAx.EN.36.4.T	0.028 $\mu\text{m} \leq$ width < 0.040 μm	0.0280 μm	0.0020 μm	
VIAx.EN.36.5.T	0.040 $\mu\text{m} \leq$ width < 0.060 μm	0.0280 μm	0.0100 μm	
VIAx.EN.36.6.T	0.060 $\mu\text{m} \leq$ width < 0.070 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAx.EN.36.7.T	0.070 $\mu\text{m} \leq$ width < 0.080 μm	0.0250/0.0100 μm	0.0200/0.0300 μm	
VIAx.EN.36.8.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIAx.EN.36.9.T	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	



Rule No.	Description	Label	Op.	Rule
VIAx.EN.31.1.T	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$		\geq	0.0280
VIAx.EN.31.2.T	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [0.022 $\mu\text{m} \leq$ width < 0.024 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0280
VIAx.EN.31.3.T	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [0.024 $\mu\text{m} \leq$ width < 0.028 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAx.EN.31.4.T	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [0.028 $\mu\text{m} \leq$ width < 0.040 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAx.EN.31.5	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0280
VIAx.EN.31.5.1.T	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0070 \mu\text{m}$		\geq	0.0100
VIAx.EN.31.6.T	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.080 μm] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$		\geq	0.0250
VIAx.EN.31.7.T	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [0.080 $\mu\text{m} \leq$ width < 0.260 μm] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$		\geq	0.0180
VIAx.EN.31.8.T	Enclosure of square VIAx ($x = 2$) [width = 0.020 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
VIAx.EN.33.1.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0280
VIAx.EN.33.2.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [0.022 $\mu\text{m} \leq$ width < 0.024 μm] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0280
VIAx.EN.33.3.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [0.024 $\mu\text{m} \leq$ width < 0.028 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAx.EN.33.4.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [0.028 $\mu\text{m} \leq$ width < 0.040 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAx.EN.33.5.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0280
VIAx.EN.33.6.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.070 μm] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
VIAx.EN.33.7.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [0.070 $\mu\text{m} \leq$ width < 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0100
VIAx.EN.33.8.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
VIAx.EN.33.9	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.050 μm] by Lower_Metal [width > 0.080 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0250/0.0300
VIAx.EN.35.1.T	Enclosure of square VIAx ($x = 2$) [width = 0.038 μm] by Lower_Metal [width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0590

Rule No.	Description	Label	Op.	Rule
VIAx.EN.35.2.T	Enclosure of square VIAx ($x = 2$) [width = 0.038 μm] by Lower_Metal [$0.060 \mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0110 \mu\text{m}$		\geq	0.0500
VIAx.EN.35.3.T	Enclosure of square VIAx ($x = 2$) [width = 0.038 μm] by Lower_Metal [$0.080 \mu\text{m} \leq \text{width} < 0.100 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0210 \mu\text{m}$		\geq	0.0430
VIAx.EN.35.4.T	Enclosure of square VIAx ($x = 2$) [width = 0.038 μm] by Lower_Metal [$0.100 \mu\text{m} \leq \text{width} < 0.120 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0310 \mu\text{m}$		\geq	0.0430
VIAx.EN.35.5.T	Enclosure of square VIAx ($x = 2$) [width = 0.038 μm] by Lower_Metal [$0.120 \mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0400 \mu\text{m}$		\geq	0.0400
VIAx.EN.35.6.T	Enclosure of square VIAx ($x = 2$) [width = 0.038 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0500 \mu\text{m}$		\geq	0.0600
VIAx.EN.36.1.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [width $< 0.022 \mu\text{m}$] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0280
VIAx.EN.36.2.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [$0.022 \mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0280
VIAx.EN.36.3.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [$0.024 \mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAx.EN.36.4.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [$0.028 \mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAx.EN.36.5.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [$0.040 \mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0280
VIAx.EN.36.6.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [$0.060 \mu\text{m} \leq \text{width} < 0.070 \mu\text{m}$] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
VIAx.EN.36.7.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [$0.070 \mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0100
VIAx.EN.36.8.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
VIAx.EN.36.9.T	Short side enclosure of rectangular VIAx ($x = 2$) [length = 0.034 μm] by Lower_Metal [width $> 0.080 \mu\text{m}$] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$		\geq	0.0250/0.0300

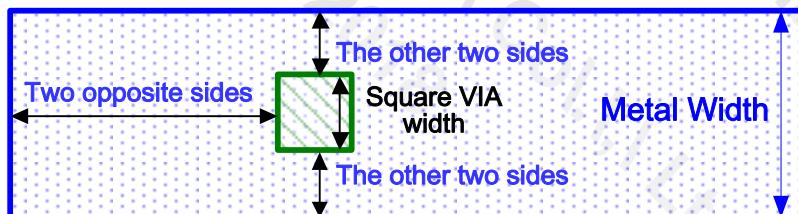
4.5.46.2 VIAx ($x > 2$) Enclosure Rule Tabulation

RuleTable.VIAx.EN.32 (Enclosure of square VIAx ($x > 2$) [width = 0.020 μm])

Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAx.EN.32.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIAx.EN.32.2.T	0.022 $\mu\text{m} \leq$ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIAx.EN.32.3.T	0.024 $\mu\text{m} \leq$ width < 0.028 μm	0.0300 μm	0.0020 μm	
VIAx.EN.32.4.T	0.028 $\mu\text{m} \leq$ width < 0.040 μm	0.0300 μm	0.0020 μm	
VIAx.EN.32.5.T	0.040 $\mu\text{m} \leq$ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIAx.EN.32.6.T	0.060 $\mu\text{m} \leq$ width < 0.080 μm	0.0250 μm	0.0200 μm	
VIAx.EN.32.7.T	0.080 $\mu\text{m} \leq$ width < 0.260 μm	0.0180 μm	0.0300 μm	
VIAx.EN.32.8.T	width \geq 0.260 μm	0.0600 μm	0.0250 μm	

RuleTable.VIAx.EN.37 (Enclosure of square VIAx ($x > 2$) [width = 0.038 μm])

Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAx.EN.37.1.T	width < 0.060 μm	0.0590 μm	0.0010 μm	
VIAx.EN.37.2.T	0.060 $\mu\text{m} \leq$ width < 0.080 μm	0.0500 μm	0.0110 μm	
VIAx.EN.37.3.T	0.080 $\mu\text{m} \leq$ width < 0.100 μm	0.0430 μm	0.0210 μm	
VIAx.EN.37.4.T	0.100 $\mu\text{m} \leq$ width < 0.120 μm	0.0430 μm	0.0310 μm	
VIAx.EN.37.5.T	0.120 $\mu\text{m} \leq$ width < 0.260 μm	0.0400 μm	0.0400 μm	
VIAx.EN.37.6.T	width \geq 0.260 μm	0.0600 μm	0.0500 μm	

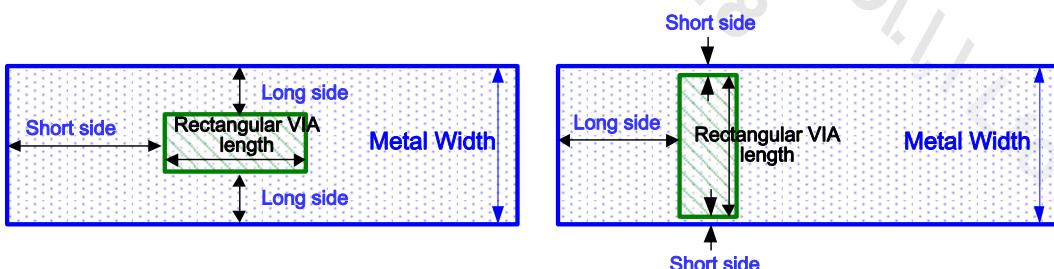


RuleTable.VIAx.EN.34 (Enclosure of rectangular VIAx ($x > 2$) [$\text{length} = 0.050 \mu\text{m}$])

Rule Number	Metal Width	Short side	Long side	Exception
VIAx.EN.34.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIAx.EN.34.2.T	0.022 $\mu\text{m} \leq$ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIAx.EN.34.3.T	0.024 $\mu\text{m} \leq$ width < 0.028 μm	0.0300 μm	0.0020 μm	
VIAx.EN.34.4.T	0.028 $\mu\text{m} \leq$ width < 0.040 μm	0.0300 μm	0.0020 μm	
VIAx.EN.34.5.T	0.040 $\mu\text{m} \leq$ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIAx.EN.34.6.T	0.060 $\mu\text{m} \leq$ width < 0.070 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAx.EN.34.7.T	0.070 $\mu\text{m} \leq$ width < 0.080 μm	0.0250/0.0100 μm	0.0200/0.0300 μm	
VIAx.EN.34.8.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIAx.EN.34.9.T	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	

RuleTable.VIAx.EN.38 (Enclosure of rectangular VIAx ($x > 2$) [$\text{length} = 0.034 \mu\text{m}$])

Rule Number	Metal Width	Short side	Long side	Exception
VIAx.EN.38.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIAx.EN.38.2.T	0.022 $\mu\text{m} \leq$ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIAx.EN.38.3.T	0.024 $\mu\text{m} \leq$ width < 0.028 μm	0.0300 μm	0.0020 μm	
VIAx.EN.38.4.T	0.028 $\mu\text{m} \leq$ width < 0.040 μm	0.0300 μm	0.0020 μm	
VIAx.EN.38.5.T	0.040 $\mu\text{m} \leq$ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIAx.EN.38.6.T	0.060 $\mu\text{m} \leq$ width < 0.070 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAx.EN.38.7.T	0.070 $\mu\text{m} \leq$ width < 0.080 μm	0.0250/0.0100 μm	0.0200/0.0300 μm	
VIAx.EN.38.8.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIAx.EN.38.9.T	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	



Rule No.	Description	Label	Op.	Rule
VIAx.EN.32.1.T	Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] by Lower_Metal [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$		\geq	0.0300
VIAx.EN.32.2.T	Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] by Lower_Metal [0.022 $\mu\text{m} \leq$ width < 0.024 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIAx.EN.32.3.T	Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] by Lower_Metal [0.024 $\mu\text{m} \leq$ width < 0.028 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAx.EN.32.4.T	Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] by Lower_Metal [0.028 $\mu\text{m} \leq$ width < 0.040 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAx.EN.32.5.T	Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
VIAx.EN.32.6.T	Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.080 μm] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$		\geq	0.0250
VIAx.EN.32.7.T	Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] by Lower_Metal [0.080 $\mu\text{m} \leq$ width < 0.260 μm] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$		\geq	0.0180
VIAx.EN.32.8.T	Enclosure of square VIAx ($x > 2$) [width = 0.020 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
VIAx.EN.34.1.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0300
VIAx.EN.34.2.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [0.022 $\mu\text{m} \leq$ width < 0.024 μm] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIAx.EN.34.3.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [0.024 $\mu\text{m} \leq$ width < 0.028 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAx.EN.34.4.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [0.028 $\mu\text{m} \leq$ width < 0.040 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAx.EN.34.5.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
VIAx.EN.34.6.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.070 μm] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
VIAx.EN.34.7.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [0.070 $\mu\text{m} \leq$ width < 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0100
VIAx.EN.34.8.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
VIAx.EN.34.9.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.050 μm] by Lower_Metal [width > 0.080 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$		\geq	0.0250/0.0300
VIAx.EN.37.1.T	Enclosure of square VIAx ($x > 2$) [width = 0.038 μm] by Lower_Metal [width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0590
VIAx.EN.37.2.T	Enclosure of square VIAx ($x > 2$) [width = 0.038 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.080 μm] for two opposite sides with the other two sides $\geq 0.0110 \mu\text{m}$		\geq	0.0500
VIAx.EN.37.3.T	Enclosure of square VIAx ($x > 2$) [width = 0.038 μm] by Lower_Metal [0.080 $\mu\text{m} \leq$ width < 0.100 μm] for two opposite sides with the other two sides $\geq 0.0210 \mu\text{m}$		\geq	0.0430

Rule No.	Description	Label	Op.	Rule
VIAx.EN.37.4.T	Enclosure of square VIAx ($x > 2$) [width = 0.038 μm] by Lower_Metal [$0.100 \mu\text{m} \leq \text{width} < 0.120 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0310 \mu\text{m}$		\geq	0.0430
VIAx.EN.37.5.T	Enclosure of square VIAx ($x > 2$) [width = 0.038 μm] by Lower_Metal [$0.120 \mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0400 \mu\text{m}$		\geq	0.0400
VIAx.EN.37.6.T	Enclosure of square VIAx ($x > 2$) [width = 0.038 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0500 \mu\text{m}$		\geq	0.0600
VIAx.EN.38.1.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [width $< 0.022 \mu\text{m}$] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0300
VIAx.EN.38.2.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [$0.022 \mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIAx.EN.38.3.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [$0.024 \mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAx.EN.38.4.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [$0.028 \mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAx.EN.38.5.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [$0.040 \mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
VIAx.EN.38.6.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [$0.060 \mu\text{m} \leq \text{width} < 0.070 \mu\text{m}$] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
VIAx.EN.38.7.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [$0.070 \mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0100
VIAx.EN.38.8.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
VIAx.EN.38.9.T	Short side enclosure of rectangular VIAx ($x > 2$) [length = 0.034 μm] by Lower_Metal [width $> 0.080 \mu\text{m}$] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$		\geq	0.0250/0.0300

4.5.47 Mx Layout Rules

- Minimum Pitch (MINP) 0.040 μm can only be drawn in either parallel or perpendicular to PO direction.
 - Data type 275, 276 is used for metal pitch 0.040 μm in perpendicular to core PO direction, or
 - Data type 255, 256 is used for metal pitch 0.040 μm in parallel to core PO direction
- NonMinimum Pitch (NMNP) direction is perpendicular to Minimum pitch (MINP) direction.

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Mx = {MxCA OR MxCB}

Mx line-end (end) definition: Mx width ≤ 0.060 μm.

DRC checks DMx_O as well as Mx in this section.

Mx in this section check Mn (n ≥ 3)

Rule No.	Description	Label	Op.	Rule
Mx.W.1	Width	W1	≥	0.0200
Mx.W.1.1	Width [MINP direction] (Except following conditions: 1. M3 [INTERACT BLK_M3, INSIDE {SRAMDMY OR BCWDMY}])	W1A	=	0.0200, 0.0220, 0.0240, 0.0400, 0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1800
Mx.W.1.1.1	Width of M3 [MINP direction, INTERACT BCWDMY]	W1A1	=	0.0280, 0.0400
Mx.W.1.1.2	Width of DMx_O [MINP direction]	W1A2	=	0.0240, 0.0400, 0.1400
Mx.W.1.2	Width [NMNP direction] (Except following conditions: 1. M3 interact BLK_M3)	W1B	=	0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1560
Mx.W.2	Width of 45-degree bent Mx (Except SEALRING_ALL)	W2	≥	0.4000
Mx.W.3	Maximum width (Except SEALRING_ALL, LOGO)	W3	≤	0.5000
Mx.W.4	Width of {{M3 [width = 0.028] SIZING up/down 0.010 μm in MINP direction} AND BCWDMY} in MINP direction	W4	=	0.1720
Mx.S.1	Space	S1	≥	0.0200
Mx.S.2	Space to Mx [0.020 μm ≤ width ≤ 0.024 μm] in MINP direction [PRL > -0.080 μm] (Except following conditions: 1. M3 space inside {{BLK_M3 SIZING 0.0175 μm in MINP direction} SIZING 0.080 μm in NMNP direction})	SM	=	0.0200 ~ 0.0250, ≥ 0.0350
Mx.S.2.1	Space to Mx [width = 0.040 μm] in MINP direction [PRL > -0.040 μm] (Except following conditions: 1. M3 space inside {{M3 [INTERACT BLK_M3] AND {SRAMDMY OR BCWDMY}} SIZING 0.0175 μm in MINP direction} SIZING 0.040 μm in NMNP direction})	SM	≥	0.0350
Mx.S.2.1.4	Space of M3 [width = 0.028 μm] in MINP direction [PRL > -0.040 μm, INTERACT BCWDMY]	SM	=	0.0200, 0.0680, 0.1160, ≥ 0.1400
Mx.S.2.1.5	Space of M3 [width = 0.040 μm] to M3 [width = 0.028 μm] in MINP direction [PRL > -0.040 μm, INTERACT BCWDMY]	SM	=	0.0460, 0.0940, 0.1220, ≥ 0.1400
Mx.S.2.1.6	Space of M3 [width = 0.040 μm] in MINP direction [PRL > -0.040 μm, INTERACT BCWDMY]	SM	=	0.0360, 0.1120, ≥ 0.1400
Mx.S.2.2	Space to Mx [0.040 μm < width ≤ 0.080 μm] in MINP direction [PRL > -0.040 μm] (Except following conditions: 1. M3 space inside {{BLK_M3 SIZING 0.020 μm in MINP direction} SIZING 0.040 μm in NMNP direction})	SM	≥	0.0400
Mx.S.2.5	Space to Mx [width ≥ 0.100 μm] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0600
Mx.S.2.6	Space to Mx [width ≥ 0.260 μm] in MINP direction [PRL > 0.080 μm]	SM	≥	0.1600

Rule No.	Description	Label	Op.	Rule
Mx.S.3.1	Space to Mx [width = 0.060 μm] in NMINP direction [PRL > -0.060 μm]	SN	\geq	0.0660
Mx.S.3.2	Space to Mx [width = 0.080 μm] in NMINP direction [PRL > -0.060 μm] (Except following conditions: 1. M3 space inside {{BLK_M3 SIZING 0.038 μm in NMINP direction} SIZING 0.060 μm in MINP direction})	SN	\geq	0.0760
Mx.S.3.3	Space to Mx [0.100 μm \leq width \leq 0.120 μm] in NMINP direction [PRL > -0.060 μm] (Except following conditions: 1. M3 space inside {{BLK_M3 SIZING 0.038 μm in NMINP direction} SIZING 0.060 μm in MINP direction})	SN	\geq	0.0760
Mx.S.3.5	Space of Mx [width = 0.140 μm with edge length > 0.060 μm in MINP direction] to Mx [with edge length > 0.060 μm in MINP direction] in NMINP direction [0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1200
Mx.S.3.6	Space to Mx [width = 0.140 μm] in NMINP direction [PRL > 0.080 μm]	SN	\geq	0.1600
Mx.S.3.7	Space of Mx [width \geq 0.156 μm with edge length > 0.060 μm in MINP direction] to Mx [with edge length > 0.060 μm in MINP direction] in NMINP direction [0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1400
Mx.S.3.8	Space to Mx [width \geq 0.156 μm] in NMINP direction [PRL > 0.080 μm]	SN	\geq	0.1800
Mx.S.3.9	Space of Mx [width \geq 0.260 μm with edge length > 0.060 μm in MINP direction] to Mx [with edge length > 0.060 μm in MINP direction] in NMINP direction [0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1800
Mx.S.3.10	Space to Mx [width \geq 0.260 μm] in NMINP direction [PRL > 0.080 μm]	SN	\geq	0.2600
Mx.S.4.1	Space to Mx line-end in NMINP direction [PRL > -0.020 μm] (Except FB_9, FB_8)	S4A	\geq	0.1240
Mx.S.4.2	Space to Mx line-end in MINP direction [PRL > -0.020 μm]	S4B	\geq	0.1240
Mx.S.5	Corner projected space of Mx [-0.060 μm < PRL \leq 0 μm] (Except following conditions: 1. Corner with edge length \leq 0.024 μm on both sides)	S5	\geq	0.0600
Mx.S.12	Space to 45-degree bent Mx [PRL > 0 μm] (Except SEALRING_ALL)	S12	\geq	0.4000
Mx.S.12.1	Space to 45-degree bent Mx (Except SEALRING_ALL)	S12A	\geq	0.1400
Mx.S.13.1	Space to VIAx-1 or VIAx or VIAxa [maximum delta V > 0.96V]	S13	\geq	0.0550
Mx.S.13.2	Space to VIAx-1 or VIAx or VIAxa [maximum delta V > 1.32V] (1.2V + 10%)	S13	\geq	0.0640
Mx.S.13.3	Space to VIAx-1 or VIAx or VIAxa [maximum delta V > 1.65V] (1.5V + 10%)	S13	\geq	0.0700
Mx.S.13.4	Space to VIAx-1 or VIAx or VIAxa [maximum delta V > 1.98V] (1.8V + 10%)	S13	\geq	0.0820
Mx.S.13.5	Space to VIAx-1 or VIAx or VIAxa [maximum delta V > 2.75V] (2.5V + 10%)	S13	\geq	0.0870
Mx.S.18	Space to Mx [maximum delta V > 0.96V] (Except following conditions: 1. Mx in MetalFuse)	S18	\geq	0.0520
Mx.S.18.1	Space to Mx [maximum delta V > 1.32V] (1.2V + 10%) (Except following conditions: 1. Mx in MetalFuse)	S18	\geq	0.0550
Mx.S.18.2	Space to Mx [maximum delta V > 1.65V] (1.5V + 10%) (Except following conditions: 1. Mx in MetalFuse)	S18	\geq	0.0610
Mx.S.18.3	Space to Mx [maximum delta V > 1.98V] (1.8V + 10%) (Except following conditions: 1. Mx in MetalFuse)	S18	\geq	0.0690
Mx.S.18.4	Space to Mx [maximum delta V > 2.75V] (2.5V + 10%) (Except following conditions: 1. Mx in MetalFuse)	S18	\geq	0.0790

Rule No.	Description	Label	Op.	Rule
Mx.S.18.6	Corner projected space of Mx [maximum delta V > 0.96V, -0.060 $\mu\text{m} \leq \text{PRL} \leq 0 \mu\text{m}$]	S18F	\geq	0.1000
Mx.S.18.7	Corner projected space of Mx [maximum delta V > 1.98V, -0.100 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$]	S18G	\geq	0.1000
Mx.EN.0	1. Enclosure of square Lower_VIA [width = 0.020 μm] is defined by RuleTable.Mx.EN.31 in the subsection 2. Enclosure of square Lower_VIA [width = 0.038 μm] is defined by RuleTable.Mx.EN.34 in the subsection 3. Enclosure of rectangular Lower_VIA [length = 0.050 μm] is defined by RuleTable.Mx.EN.32 in the subsection 4. Enclosure of rectangular Lower_VIA [length = 0.034 μm] is defined by RuleTable.Mx.EN.33 in the subsection			
Mx.EN.1.2.1	Enclosure of square VIAx-1 by Mx [width = 0.028 μm , INTERACT BCWDMY] for two opposite sides with the other two sides $\geq 0.004 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})	EN1	\geq	0.0300
Mx.EN.1.6	Enclosure of square VIAx-1 by Mx [0.080 $\mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.030 \mu\text{m}$ (Except following conditions: 1. Mx [width = 0.120 μm] enclosure of square VIAx-1 array, 2. VIA2 inside BLK_M3) Definition of square VIAx-1 array follows Mx.EN.3.5	EN1F	\geq	0.0200
Mx.EN.3.5	Enclosure of square VIAx-1 array by Mx [width = 0.120 μm] for two opposite sides with the other two sides [Square VIAx-1 array edge length = 0.020 μm] $\geq 0.018 \mu\text{m}$ Definition of square VIAx-1 array: VIAx-1 space = 0.044 μm [PRL = 0.020 μm] in Mx MINP direction	EN3E	\geq	0.0300
Mx.EN.6.2.1	Short side enclosure of rectangular VIAx-1 by Mx [width = 0.028 μm , INTERACT BCWDMY] with the other two long side enclosure $\geq 0.004 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})	EN6	\geq	0.0300
Mx.EN.6.4	Short side enclosure of rectangular VIAx-1 by Mx edge [length = 0.080 μm , Mx width = 0.080 μm] (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})	EN6D	\geq	0.0250
Mx.EN.31.3	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.024 $\mu\text{m} \leq \text{width} < 0.026 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0300
Mx.EN.31.5	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0300
Mx.EN.31.6	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.040 $\mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0300
Mx.EN.31.7	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.060 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$		\geq	0.0250
Mx.EN.32.5	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0300

Rule No.	Description	Label	Op.	Rule
Mx.EN.32.9	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.080 μm < width < 0.260 μm] with the other two long sides \geq 0.0300/0.0250 μm (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0250/0.0300
Mx.EN.33.5	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.028 μm \leq width < 0.040 μm] with the other two long sides \geq 0.0020 μm		\geq	0.0300
Mx.EN.33.9	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.080 μm < width < 0.260 μm] with the other two long sides \geq 0.0300/0.0250 μm		\geq	0.0250/0.0300
Mx.L.1	At least one edge length of 45-degree bent Mx (minimum edge length)	L1	\geq	0.9100
Mx.L.2	Edge length with adjacent edge [length < 0.090 μm]	L2	\geq	0.0800
Mx.A.1	Area of Mx (Except FB_9, FB_8)	A1	\geq	0.00416
Mx.DN.1.1	Minimum All_metal density in window 40 μm x 40 μm , stepping 20 μm (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	12.5%
Mx.DN.1.2	Minimum All_metal density in window 40 μm x 40 μm , stepping 20 μm [3 μm x 3 μm empty area exists in the window] (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	25%
Mx.DN.2	Maximum All_metal density in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. {{Mx;252 OR Mx;272} OR {Mx;253 OR Mx;273}} OR {{Mx;258 OR Mx;278} OR {Mx;259 OR Mx;279}}, 2. M3 inside BLK_WB)		\leq	65%
Mx.DN.2.3	Maximum All_metal density in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	75%
Mx.DN.3	The All_metal density difference between any two neighboring checking windows including DMnEXCL [window 40 μm x 40 μm , stepping 40 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\leq	50%
Mx.DN.3.3	Maximum density difference between {{MxCa OR {Mx;252 OR Mx;272}} OR {Mx;258 OR Mx;278}} and {{MxCB OR {Mx;253 OR Mx;273}} OR {Mx;259 OR Mx;279}} across full chip (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	10%
Mx.DN.3.6	Maximum local density difference between {{MxCa OR {Mx;252 OR Mx;272}} OR {Mx;258 OR Mx;278}} and {{MxCB OR {Mx;253 OR Mx;273}} OR {Mx;259 OR Mx;279}} in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	40%
Mx.DN.3.7	Minimum local density of {{MxCa OR {Mx;252 OR Mx;272}} OR {Mx;258 OR Mx;278}} in window 40 μm x 40 μm , stepping 20 μm (Except SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		$>$	4.5%
Mx.DN.3.8	Minimum local density of {{MxCB OR {Mx;253 OR Mx;273}} OR {Mx;259 OR Mx;279}} in window 40 μm x 40 μm , stepping 20 μm (Except SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		$>$	4.5%

Rule No.	Description	Label	Op.	Rule
Mx.DN.6.1	All_metal density [window 9 μm x 9 μm, stepping 4.5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
Mx.DN.7	It is not allowed to have local density < 5% of all 3 consecutive metal (Mx, Mx+1, and Mx+2) over any 27 μm x 27 μm (stepping 13.5 μm), i.e. it is allowed for either one of Mx, Mx+1, or Mx+2 to have a local density ≥ 5% (The metal layers include Mx/Mx+1/Mx+2 and dummy metals for ELK film) (Except ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc, 2. TCDDMY_Mn (assume 30% pattern density INSIDE TCDDMY_Mn))			
Mx.DN.9	Minimum Line edge Density (LeD) in window 20 μm x 20 μm, stepping 10 μm Definition of "Line edge Density": (((All_metal area) - (All_metal SIZING -0.001 μm area)) x 1000) / Checking window (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags only if the checking window has any one metal {MxCA OR MxCB} width < 0.060 μm		≥	8.5
Mx.DN.9.1	Minimum Line edge Density (LeD) in window 20 μm x 20 μm, stepping 10 μm Definition of "Line edge Density": (((All_metal area) - (All_metal SIZING -0.001 μm area)) x 1000) / Checking window (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags only if the checking window has any one metal {MxCA OR MxCB} width < 0.120 μm		≥	3
Mx.R.1	Mx must be a rectangle (Except SEALRING_ALL, LOGO)			
Mx.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
Mx.R.10	Overlap MetalFuse_B1 (156;8) is not allowed			
Mx.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of Mx space to Mx or VIAx-1 or VIAx is < 0.360 μm			

Rule No.	Description	Label	Op.	Rule
Mx.R.12	Datatype (255 or 256 or 252 or 253 or 258 or 259) and (275 or 276 or 272 or 273 or 278 or 279) exist on the same metal layer at the same time is not allowed			
Mx.R.12.2	Same datatype (255 or 256 or 252 or 253 or 258 or 259) or (275 or 276 or 272 or 273 or 278 or 279) in (Mx and Mx+1) at the same time is not allowed			
Mx.R.14	<p>$\{\{Mx_Empty_Area\ SIZING\ 0.330\ \mu m\}\ INTERACT\ Mx\ island\}$ is not allowed</p> <p>Definitions:</p> <ol style="list-style-type: none"> 1. Mx_Empty_Area: Area of $\{\{CHIP\ NOT\ \{\{TCDDMY_Mn\ OR\ ICOVL_SINGLE\}\ OR\ \{\{Mx\ OR\ DMx\}\ OR\ DMx_O\}\}\ SIZING\ down/up\ 0.380\ \mu m\}\ \geq\ 1.96\ \mu m^2$ 2. Mx island: Area of (Mx with only one square VIAx-1 [width x length = $0.020\ \mu m \times 0.020\ \mu m$]) $\leq\ 0.010\ \mu m^2$ 			
Mx.R.15	<p>$\{\{Mx_Empty_Area\ SIZING\ 0.100\ \mu m\ in\ MINP\ direction\}\ interact\ VIAx-1\ [INTERACT\ Mx\ [width\ <\ 0.060\ \mu m]\]$ is not allowed</p> <p>(Except following conditions:</p> <ol style="list-style-type: none"> 1. VIA1 inside BLK_M2) <p>Definition of Mx_Empty_Area:</p> <p>$\{\{\{CHIP\ NOT\ \{\{Mx\ OR\ DMx\}\ OR\ DMx_O\}\}\ SIZING\ down/up\ 0.380\ \mu m\ in\ MINP\ direction\}\ SIZING\ down/up\ 0.400\ \mu m\ in\ NMINP\ direction\}$ can enclose a $0.760\ \mu m \times 0.800\ \mu m$ (MINP x NMINP) orthogonal rectangle</p>			
Mx.R.17	DMx is a must in chip level.			
Mx.R.18	<p>Mx [width $\leq\ 0.022\ \mu m$] interact VIAx-1_array_region is not allowed</p> <p>(Except following conditions:</p> <ol style="list-style-type: none"> 1. M3 interact BLK_M3) <p>VIAx-1_array_region definition:</p> <ol style="list-style-type: none"> (1) VIAx-1 array is $\geq\ 2\times 2$ VIAx-1 array, and (2) Two VIAx-1 space $<\ 0.140\ \mu m$ in NMINP direction [PRL $>\ 0\ \mu m$], and both of the VIAx-1 space = $0.0505\sim 0.0760\ \mu m$ in MINP direction [PRL $>\ -0.020\ \mu m$], and (3) Form one region from one of each VIAx-1 corner (C1/C2/C3/C4), and the space of the corners is the minimum in MINP and NMINP direction. 			
Mx.R.18.1	<p>Mx [width $\leq\ 0.022\ \mu m$] interact VIAx-1_array_region is not allowed</p> <p>(Except following conditions:</p> <ol style="list-style-type: none"> 1. M3 interact BLK_M3) <p>VIAx-1_array_region definition:</p> <ol style="list-style-type: none"> (1) VIAx-1 array is $\geq\ 2\times 2$ VIAx-1 array, and (2) Two VIAx-1 space $<\ 0.100\ \mu m$ in NMINP direction [PRL $>\ 0\ \mu m$], and both of the VIAx-1 space = $0.0505\sim 0.0760\ \mu m$ in MINP direction [PRL $>\ -0.0205\ \mu m$], and (3) Form one region from one of each VIAx-1 corner (C1/C2/C3/C4), and the space of the corners is the minimum in MINP and NMINP direction. 			
Mx.R.18.2	<p>Space of Mx [width $\leq\ 0.022\ \mu m$] to Checked_VIAx-1_Edge in MINP direction [PRL $>\ -0.0205\ \mu m$] $<\ 0.060\ \mu m$ is not allowed</p> <p>(Except following conditions:</p> <ol style="list-style-type: none"> 1. M3 interact BLK_M3) <p>Definition of Checked_VIAx-1_Group:</p> <p>$\{\{VIAx-1\ [space\ to\ VIAx-1\ <\ 0.060\ \mu m\ in\ NMINP\ direction,\ PRL\ >\ 0\ \mu m]\}\}$</p> <p>Definition of Checked_VIAx-1_Edge:</p> <p>Checked_VIAx-1_Group NMINP edge[space to VIAx-1 = $0.060\sim 0.0975\ \mu m$ in MINP direction, PRL $>\ -0.020\ \mu m$]</p>			

Rule No.	Description	Label	Op.	Rule
Mx.R.21	<p>Both side space of Small_MxCA_Group to MxCA [width \geq 0.060 μm] in MINP direction \leq 0.220 μm is not allowed</p> <p>Definition of Small_MxCA_Group: $\{\{\{\text{Small_MxCA SIZING up/down }0.033 \mu\text{m in MINP direction}\}$ $\{\{\{\text{SIZING down/up }0.0895 \mu\text{m in MINP direction}\} [\text{length } < 0.140 \mu\text{m in NMINP direction}]\} [\text{length } = 0.180\text{--}0.490 \mu\text{m in MINP direction}]\}$</p> <p>Definition of Small_MxCA: $\{\{\{\text{MxCA [width } \leq 0.024 \mu\text{m in MINP direction, length } \leq 0.300 \mu\text{m in NMINP direction}\}\}$</p>			
Mx.CS.0	DRC checks same color space of {MxCA OR DMx_DO1} and {MxCB OR DMx_DO2}, respectively in Mx.CS.x rules			
Mx.CS.0.1	Space to Mx [width \geq 0.020 μm] in MINP direction [same color, PRL $> -0.100 \mu\text{m}$]	SM	\geq	0.0600
Mx.CS.0.2	Space to Mx [width \geq 0.060 μm] in NMINP direction [same color, PRL $> -0.060 \mu\text{m}$]	SN	\geq	0.1160
Mx.CS.1.1	<p>Space of Mx [width = 0.020 μm] to Mx [width $<$ 0.040 μm] in MINP direction [same color, PRL $> -0.124 \mu\text{m}$]</p> <p>DRC checks same color space of MxCA and MxCB</p>	SM	=	0.0600, 0.0620, 0.0640, \geq 0.1400
Mx.CS.1.1.1.1	<p>Space of Mx [width = 0.020 μm] to Mx [width = 0.040 μm] in MINP direction [same color, PRL $> -0.124 \mu\text{m}$]</p> <p>DRC checks same color space of MxCA and MxCB</p>	SM	=	0.0900, \geq 0.1400
Mx.CS.1.1.1.3	<p>Space of Mx [width = 0.020 μm] to Mx [width $>$ 0.060 μm] in MINP direction [same color, PRL $> -0.124 \mu\text{m}$]</p> <p>DRC checks same color space of MxCA and MxCB</p>	SM	=	0.0600, 0.0620, 0.0640, \geq 0.1400
Mx.CS.1.1.2	<p>Space of Mx [width = 0.022 μm] to Mx [width $<$ 0.040 μm, or width $>$ 0.060 μm] in MINP direction [same color, PRL $> -0.124 \mu\text{m}$]</p> <p>DRC checks same color space of MxCA and MxCB</p>	SM	=	0.0600, 0.0620, 0.0640, \geq 0.1400
Mx.CS.1.1.2.1	<p>Space of Mx [width = 0.022 μm] to Mx [width = 0.040 μm] in MINP direction [same color, PRL $> -0.124 \mu\text{m}$]</p> <p>DRC checks same color space of MxCA and MxCB</p>	SM	=	0.0950, \geq 0.1400
Mx.CS.1.1.3	<p>Space of Mx [width = 0.024 μm] to Mx [width $<$ 0.040 μm, or width $>$ 0.060 μm] in MINP direction [same color, PRL $> -0.124 \mu\text{m}$]</p> <p>(Except following conditions: 1. Both M3 interact BLK_M3)</p> <p>DRC checks same color space of MxCA and MxCB</p>	SM	=	0.0600, 0.0620, 0.0640, 0.1260, \geq 0.1400
Mx.CS.1.1.3.1	<p>Space of Mx [width = 0.024 μm] to Mx [width = 0.040 μm] in MINP direction [same color, PRL $> -0.124 \mu\text{m}$]</p> <p>DRC checks same color space of MxCA and MxCB</p>	SM	=	0.1000, \geq 0.1400
Mx.CS.1.1.3.3	Space of M3 [width = 0.028 μm] in MINP direction [same color, PRL $> -0.124 \mu\text{m}$, INTERACT BCWDMY]	SM	=	0.0680, \geq 0.1400
Mx.CS.1.1.4	<p>Space to Mx [width = 0.040 μm] in MINP direction [same color, PRL $> -0.060 \mu\text{m}$]</p> <p>(Except following conditions: 1. Both M3 interact BCWDMY, 2. Both M3 interact BLK_M3)</p>	SM	=	0.0900, 0.0950, 0.1000, 0.1100, 0.1120, \geq 0.1200
Mx.CS.1.1.4.11	Space of M3 [width = 0.040 μm] in MINP direction [same color, PRL $> -0.060 \mu\text{m}$, INTERACT BCWDMY]	SM	=	0.1120, \geq 0.1200
Mx.CS.1.1.4.12	Space of M3 [width = 0.040 μm] to M3 [width = 0.028 μm] in MINP direction [same color, PRL $> -0.060 \mu\text{m}$, INTERACT BCWDMY]	SM	=	0.0940, 0.1220, \geq 0.1400

Rule No.	Description	Label	Op.	Rule
Mx.CS.1.1.6	Forbidden space of Mx [$0.020 \mu\text{m} \leq \text{width} \leq 0.024 \mu\text{m}$] in MINP direction [same color, PRL > 0 μm] (Except following conditions: 1. Mx_Projection_Region fully projected by another Mx [width > 0.024 μm]) Definition of Mx_Projection_Region: Enclosed region formed by Mx [$0.020 \mu\text{m} \leq \text{width} \leq 0.024 \mu\text{m}$], PRL > 0 μm	SM	=	0.1870 ~ 0.2190, 0.2570 ~ 0.2990, 0.3370 ~ 0.3790
Mx.CS.1.1.7	Space of DMx_O [width = 0.024 μm] to Mx in MINP direction [same color, PRL > -0.124 μm]	SM	=	0.0600, 0.0620, 0.0640, 0.0660, 0.0680, 0.0700, ≥ 0.1000
Mx.CS.1.1.8	Space of DMx_O [width = 0.040 μm] to Mx in MINP direction [same color, PRL > -0.124 μm]	SM	\geq	0.1000
Mx.CS.1.2	Space of Mx [width = 0.060 μm] to Mx in MINP direction [same color, PRL > 0 μm]	SM	\geq	0.1000
Mx.CS.1.2.1	Space of Mx [width = 0.060 μm] to Mx [width = 0.020/0.022/0.024 μm] in MINP direction [same color, PRL > 0 μm] (Except FB_9)	SM	\geq	0.1400
Mx.CS.1.3	Space of Mx [$0.080 \mu\text{m} \leq \text{width} \leq 0.120 \mu\text{m}$ with edge length > 0.060 μm in NMINP direction] to Mx [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1200
Mx.CS.1.6	Space of Mx [width = 0.140 μm with edge length > 0.060 μm in NMINP direction] to Mx [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1300
Mx.CS.1.7	Space to Mx [width = 0.140 μm] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.1600
Mx.CS.1.8	Space of Mx [width $\geq 0.180 \mu\text{m}$ with edge length > 0.060 μm in NMINP direction] to Mx [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1400
Mx.CS.1.9	Space to Mx [width $\geq 0.180 \mu\text{m}$] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.1800
Mx.CS.1.10	Space of Mx [width $\geq 0.260 \mu\text{m}$ with edge length > 0.060 μm in NMINP direction] to Mx [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, 0 $\mu\text{m} < \text{PRL} \leq 0.080 \mu\text{m}$]	SM	\geq	0.1800
Mx.CS.1.11	Space to Mx [width $\geq 0.260 \mu\text{m}$] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.2600
Mx.CS.3.2	Space to Mx [width = 0.060 μm] in NMINP direction [same color, PRL > -0.060 μm]	SN	\geq	0.1250
Mx.CS.3.3	Space of Mx [width = 0.080 μm with edge length > 0.060 μm in MINP direction] to Mx [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, -0.060 $\mu\text{m} < \text{PRL} \leq 0.060 \mu\text{m}$]	SN	\geq	0.1240
Mx.CS.3.4	Space to Mx [width = 0.080 μm] in NMINP direction [same color, PRL > 0.060 μm]	SN	\geq	0.1300
Mx.CS.3.5	Space of Mx [$0.100 \mu\text{m} \leq \text{width} \leq 0.120 \mu\text{m}$ with edge length > 0.060 μm in MINP direction] to Mx [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, -0.060 $\mu\text{m} < \text{PRL} \leq 0.060 \mu\text{m}$]	SN	\geq	0.1240
Mx.CS.3.6	Space to Mx [$0.100 \mu\text{m} \leq \text{width} \leq 0.120 \mu\text{m}$] in NMINP direction [same color, PRL > 0.060 μm]	SN	\geq	0.1400
Mx.CS.3.9	Space of Mx [width = 0.140 μm with edge length > 0.060 μm in MINP direction] to Mx [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, 0 $\mu\text{m} < \text{PRL} \leq 0.080 \mu\text{m}$]	SN	\geq	0.1300
Mx.CS.3.10	Space to Mx [width = 0.140 μm] in NMINP direction [same color, PRL > 0.080 μm]	SN	\geq	0.1600
Mx.CS.3.11	Space of Mx [width $\geq 0.156 \mu\text{m}$ with edge length > 0.060 μm in MINP direction] to Mx [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, 0 $\mu\text{m} < \text{PRL} \leq 0.080 \mu\text{m}$]	SN	\geq	0.1400

Rule No.	Description	Label	Op.	Rule
Mx.CS.3.12	Space to Mx [width \geq 0.156 μm] in NMINP direction [same color, PRL > 0.080 μm]	SN	\geq	0.1800
Mx.CS.3.13	Space of Mx [width \geq 0.260 μm with edge length > 0.060 μm in MINP direction] to Mx [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, 0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1800
Mx.CS.3.14	Space to Mx [width \geq 0.260 μm] in NMINP direction [same color, PRL > 0.080 μm]	SN	\geq	0.2600
Mx.CS.5.1	Mx end-end/end-run space [PRL > -0.060 μm] in NMINP direction (Except FB_9, FB_8)	CS5A	\geq	0.1240
Mx.CS.5.3	Mx end-end/end-run space [PRL > -0.060 μm] in MINP direction	CS5C	\geq	0.1240
Mx.CS.6.1	Corner projected space of Mx [same color, -0.100 μm < PRL \leq 0 μm] (Except following conditions: 1. Corner with edge length \leq 0.024 μm on both sides)	CS6A	\geq	0.1000
Mx.CS.7	Long side of MxCA [width \leq 0.060 μm] space to MxCB [projection length difference on MxCA < 0.060 μm]	CS7	>	0.0360
Mx.CS.8	More than one {MxCA OR DMx_DO1} interact MxCB_Corner_Projected_Region from the same short side is not allowed MxCB_Corner_Projected_Region definition: The corner projected space of {MxCB OR DMx_DO2} short side edge [width \leq 0.060 μm] < 0.060 μm in NMINP direction [-0.026 μm < PRL < 0 μm]			
Mx.CS.10	{MxCA OR DMx_DO1} interact {MxCB OR DMx_DO2} is not allowed			
Mx.CS.14	Forbidden space of Mx_Critical_Group to Mx [width \leq 0.024 μm] in MINP direction [PRL > 0 μm] (Except following conditions: 1. Mx_Critical_Groups_Projection_Region fully projected by another Mx [width > 0.024 μm]) Definition of Mx_Critical_Group: { {Mx [width \leq 0.024 μm] SIZING up/down 0.032 μm in MINP direction} SIZING down/up 0.0495 μm in NMINP direction } [0.100 μm \leq width in MINP direction \leq 0.630 μm , width in NMINP direction \geq 0.100 μm] Definition of Mx_Critical_Groups_Projection_Region: Enclosed region formed by Mx_Critical_Groups, PRL > 0 μm	CS14	=	0.0650~0.1390, 0.1530~0.2190, 0.2410~0.2990
Mx.CS.15	Forbidden space of Mx in MINP direction [PRL > 0 μm] [one side is Mx [width = 0.040 μm] the other side is Mx [width = 0.020 μm]]	CS15	=	0.2510~0.2940, 0.3410~0.3590
Mx.CS.15.1	Forbidden space of Mx in MINP direction [PRL > 0 μm] [one side is Mx [width = 0.040 μm] the other side is Mx [width = 0.022/0.024 μm]]	CS15A	=	0.2510~0.2620, 0.2640~0.2750, 0.2780~0.2940
Mx.CS.16	Forbidden space of Mx in MINP direction [PRL > 0 μm] [one side is Mx [width = 0.060 μm] the other side is Mx [width = 0.020 μm]]	CS16	=	0.2510~0.2940, 0.3410~0.3590
Mx.CS.16.1	Forbidden space of Mx in MINP direction [PRL > 0 μm] [one side is Mx [width = 0.060 μm] the other side is Mx [width = 0.022/0.024 μm]]	CS16A	=	0.2450~0.2520, 0.2540~0.2650, 0.2680~0.2940
Mx.CS.17	Forbidden space of Mx in MINP direction [PRL > 0 μm] [one side is Mx [width = 0.080 μm] the other side is Mx [width \leq 0.024 μm]]	CS17	=	0.2510~0.2550, 0.2570~0.2940
Mx.CS.18	Forbidden space of Mx in MINP direction [PRL > 0 μm] [one side is Mx [0.100 μm \leq width < 0.140 μm] the other side is Mx [width \leq 0.024 μm]]	CS18	=	0.2510~0.2940
Mx.CS.19	Forbidden space of Mx in MINP direction [PRL > 0.060 μm] [one side is Mx [width \geq 0.140 μm] the other side is Mx [width \leq 0.024 μm]]	CS19	=	0.2510~0.2940

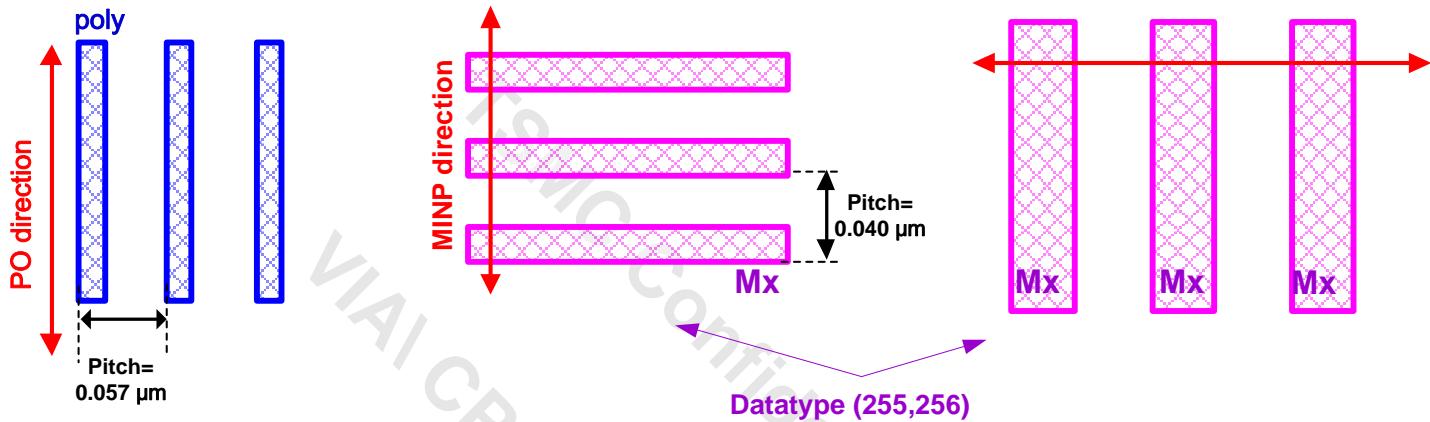
Table Notes:

- To meet the metal process window, filling the dummy metal globally and uniformly by tsmc utility is needed even if the originally drawn Mx has already met the density rules. For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, filling manually and evenly is still needed.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations during placement. Unexpected violations may occur during the IP/macro placement due to the environment, even if the IP/macro already passed the high density rule check. Therefore, customers need to carefully design the dimension of the width/space for wide metal (e.g., power/ground bus), under the proper high density limit.
- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

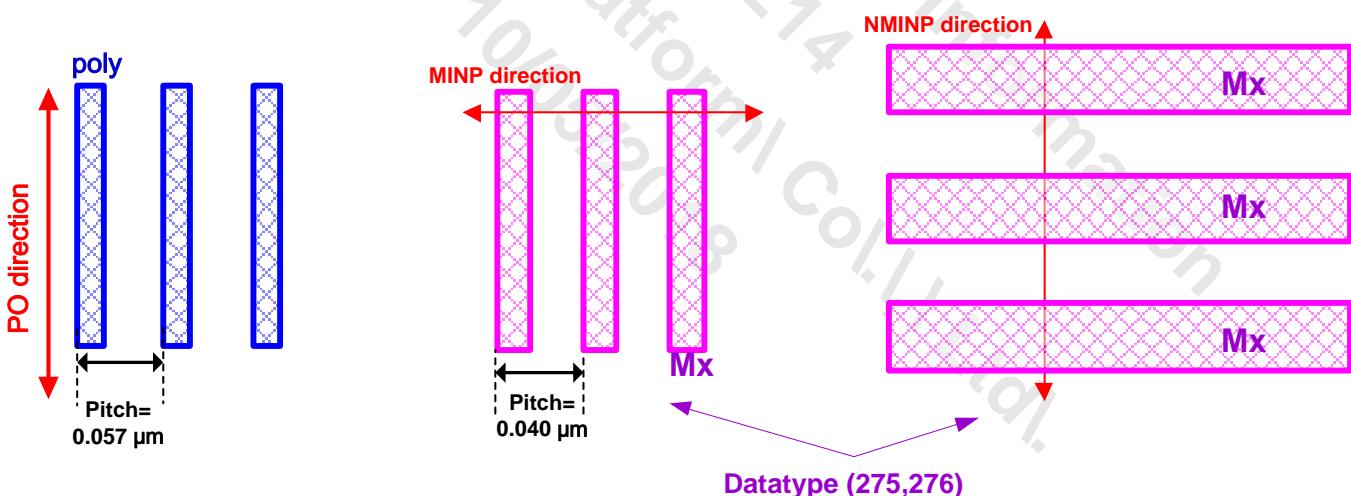
TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

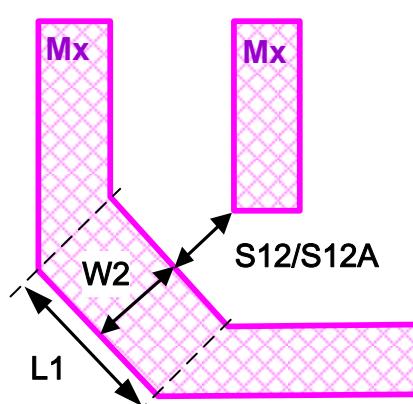
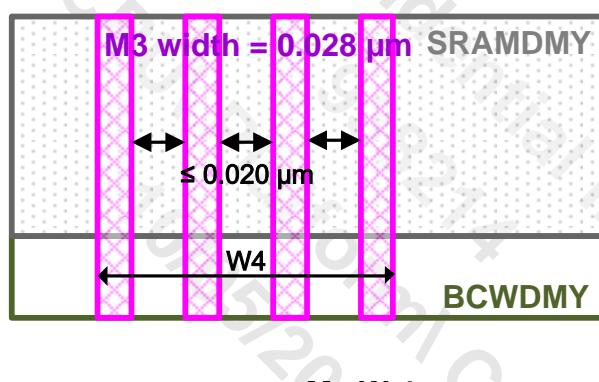
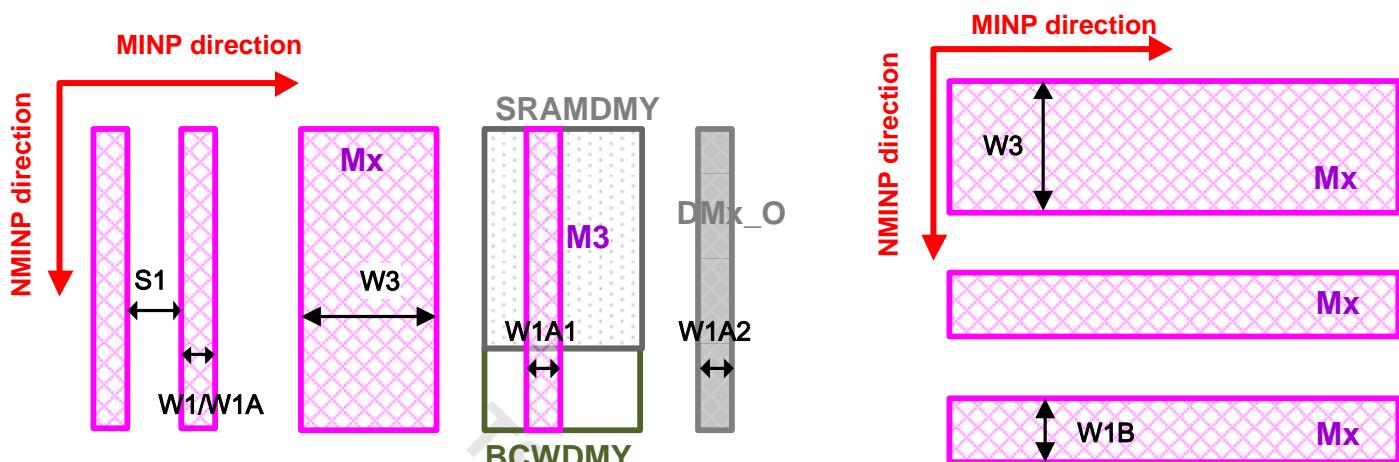
Mx

- Mx Datatype (255 or 256) MINP direction is parallel to PO direction
- Mx Datatype (255 or 256) NMNP direction is perpendicular to PO direction

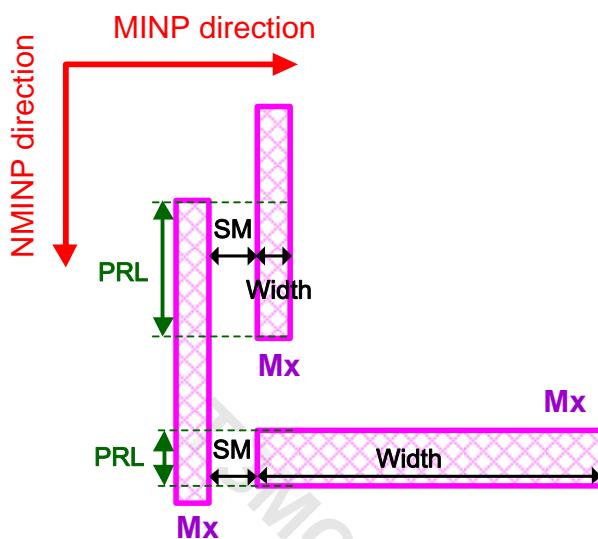


- Mx Datatype (275 or 276) MINP direction is perpendicular to PO direction
- Mx Datatype (275 or 276) NMNP direction is parallel to PO direction

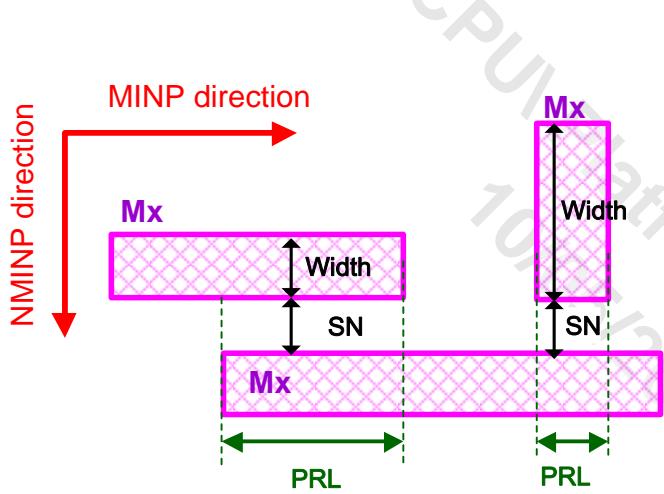




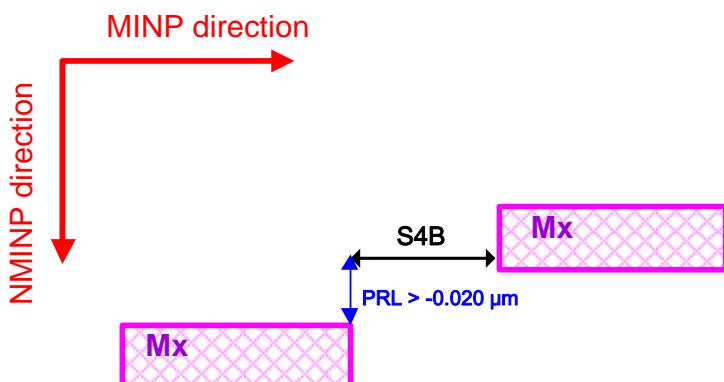
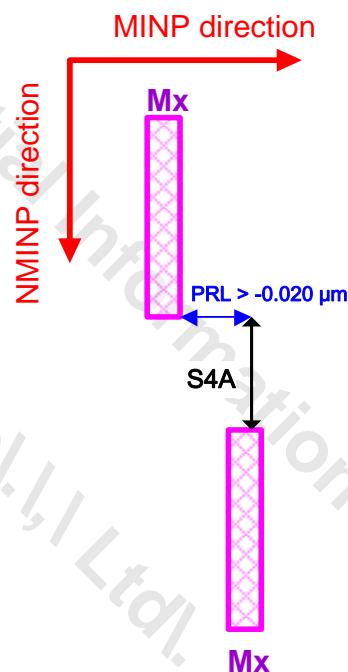
Mx.W.2 / Mx.S.12 / Mx.S.12.1 / Mx.L.1



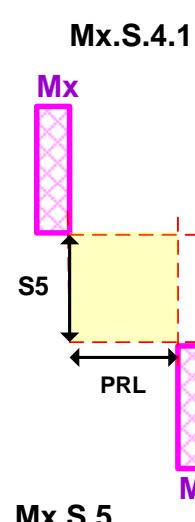
**Mx.S.2 / Mx.S.2.1 / Mx.S.2.1.4 / Mx.S.2.1.5 /
Mx.S.2.1.6 / Mx.S.2.2 / Mx.S.2.5 / Mx.S.2.6**

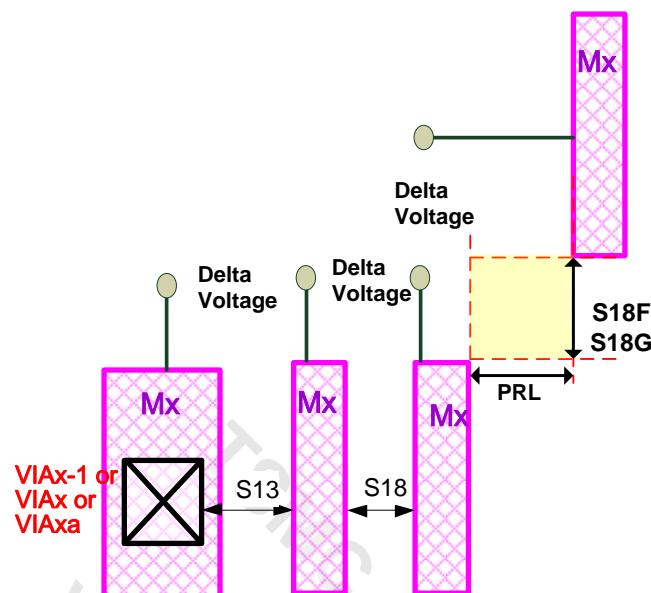


**Mx.S.3.1 / Mx.S.3.2 / Mx.S.3.3 / Mx.S.3.4 /
Mx.S.3.5 / Mx.S.3.6 / Mx.S.3.7 / Mx.S.3.8 /
Mx.S.3.9 / Mx.S.3.10**

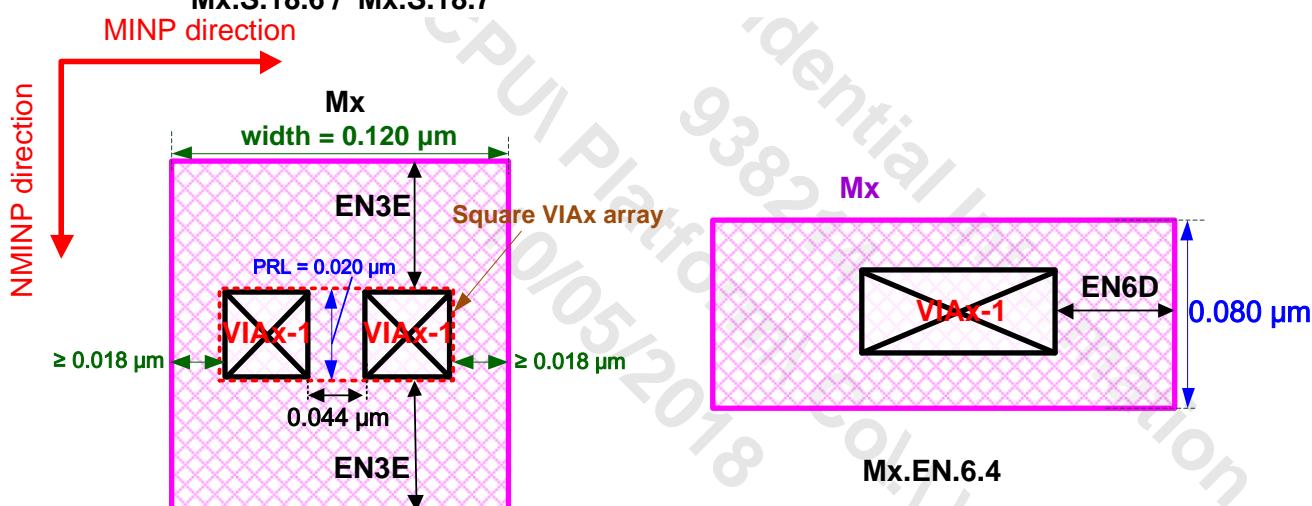


Mx.S.4.2

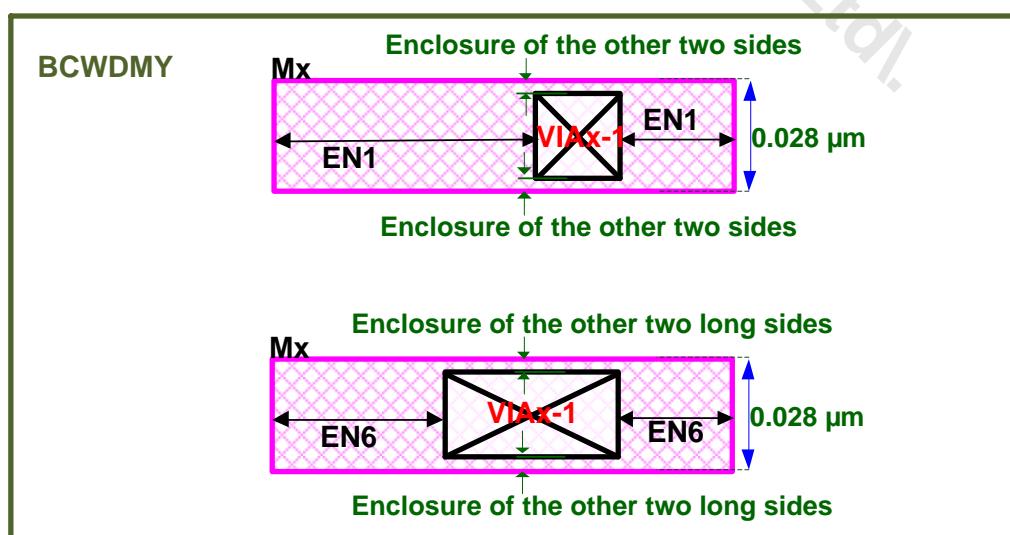




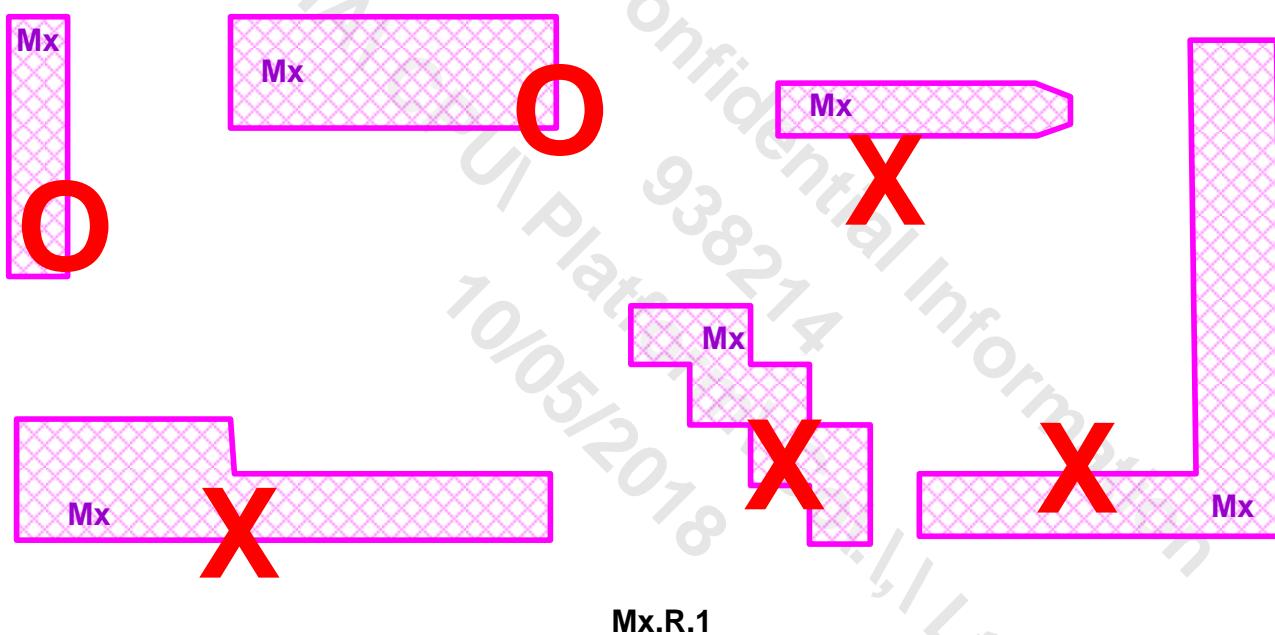
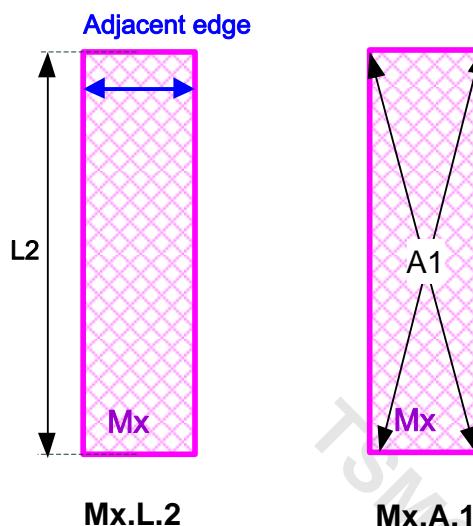
Mx.S.13.1 / Mx.S.13.2 / Mx.S.13.3 / Mx.S.13.4 / Mx.S.13.5
 Mx.S.18 / Mx.S.18.1 / Mx.S.18.2 / Mx.S.18.3 / Mx.S.18.4
 Mx.S.18.6 / Mx.S.18.7



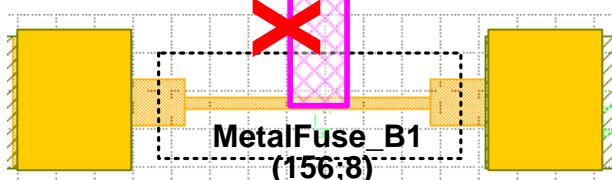
Mx.EN.1.6 / Mx.EN.3.5



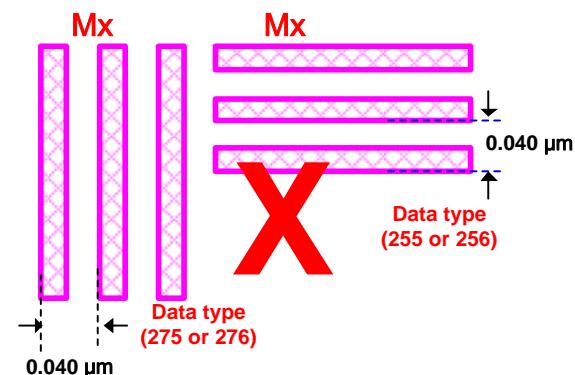
Mx.EN.1.2.1 / Mx.EN.6.2.1



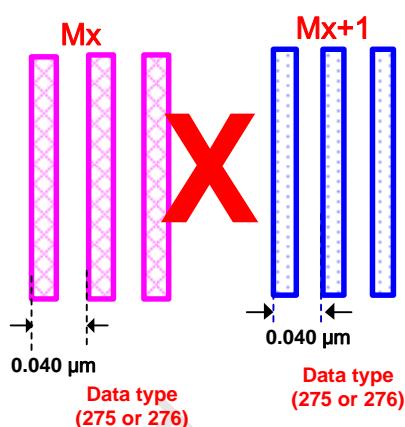
Overlap is not allowed



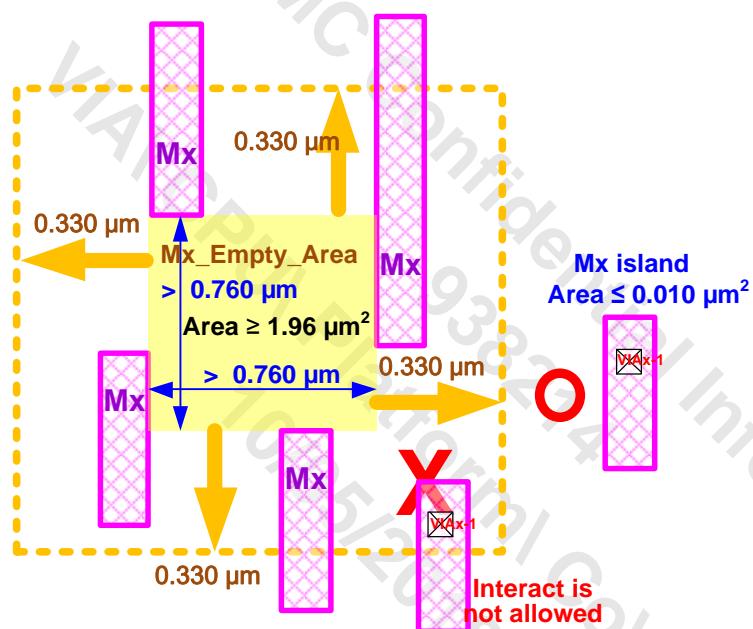
Mx.R.10



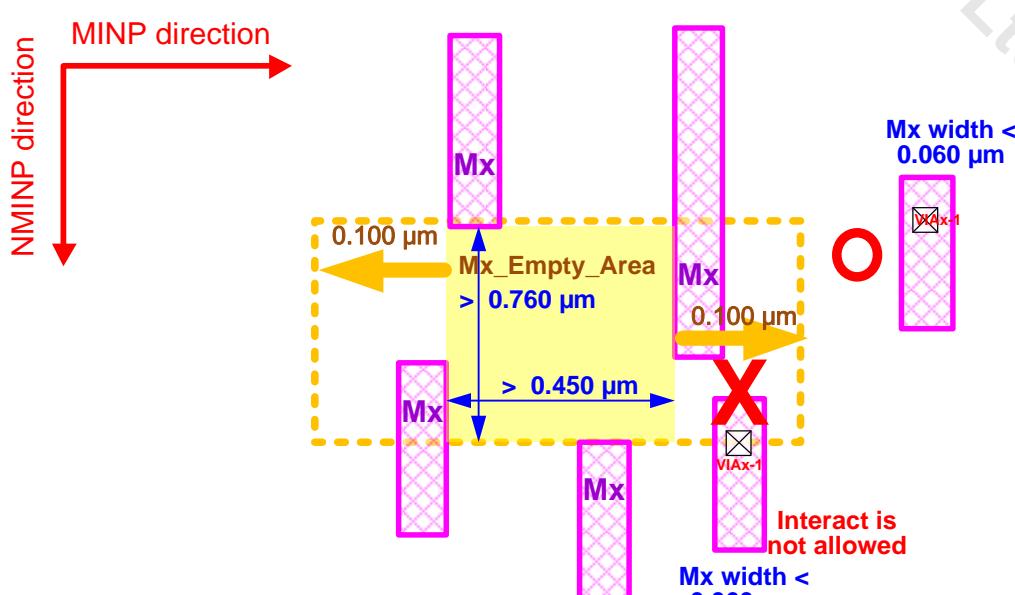
Mx.R.12



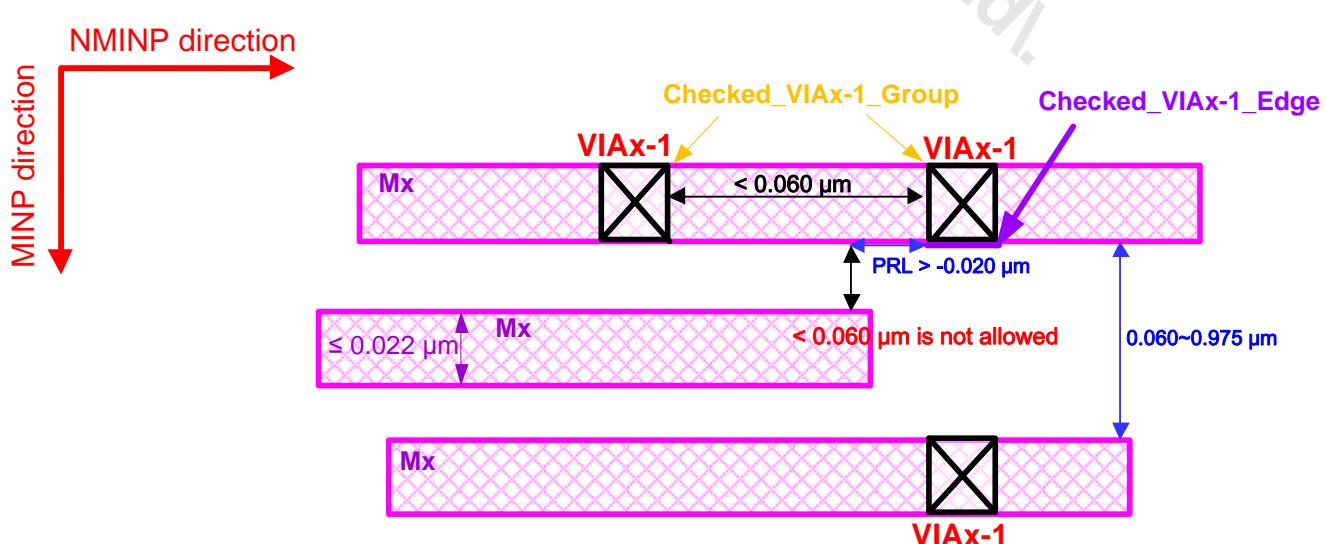
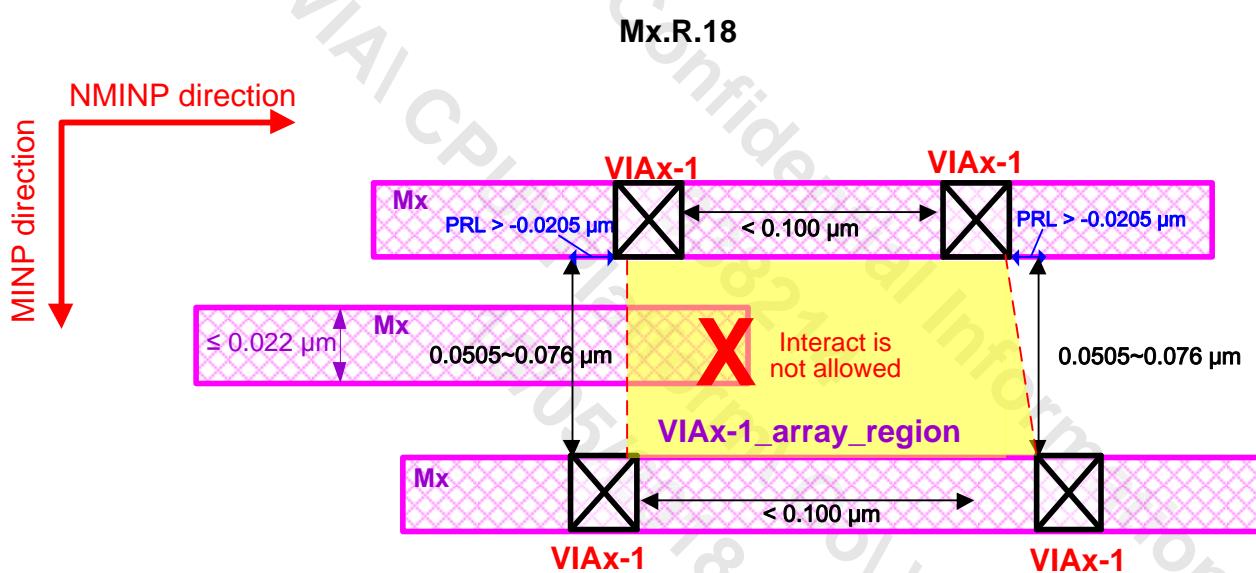
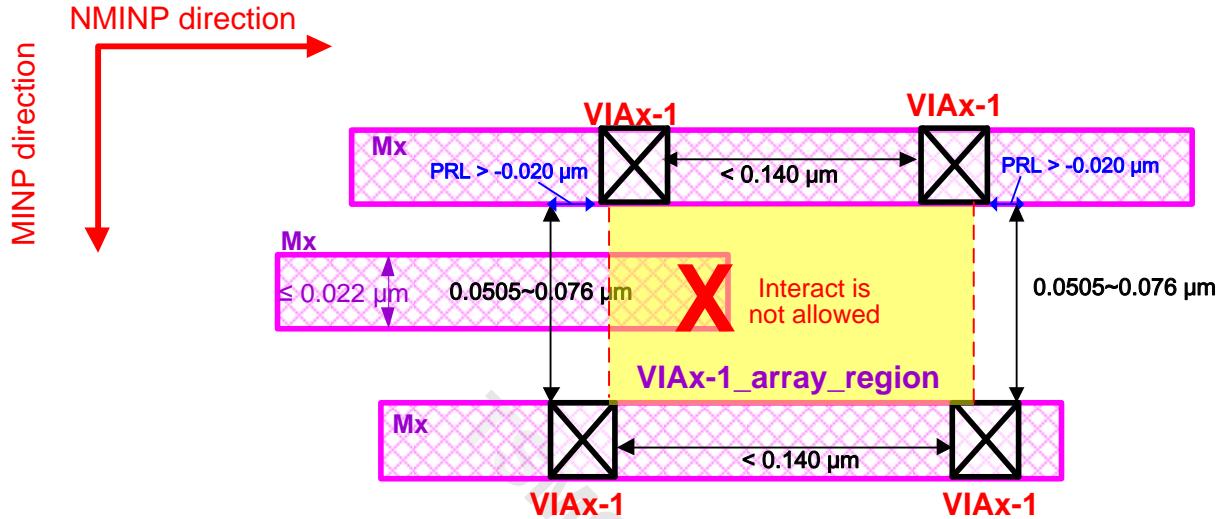
Mx.R.12.2



Mx.R.14

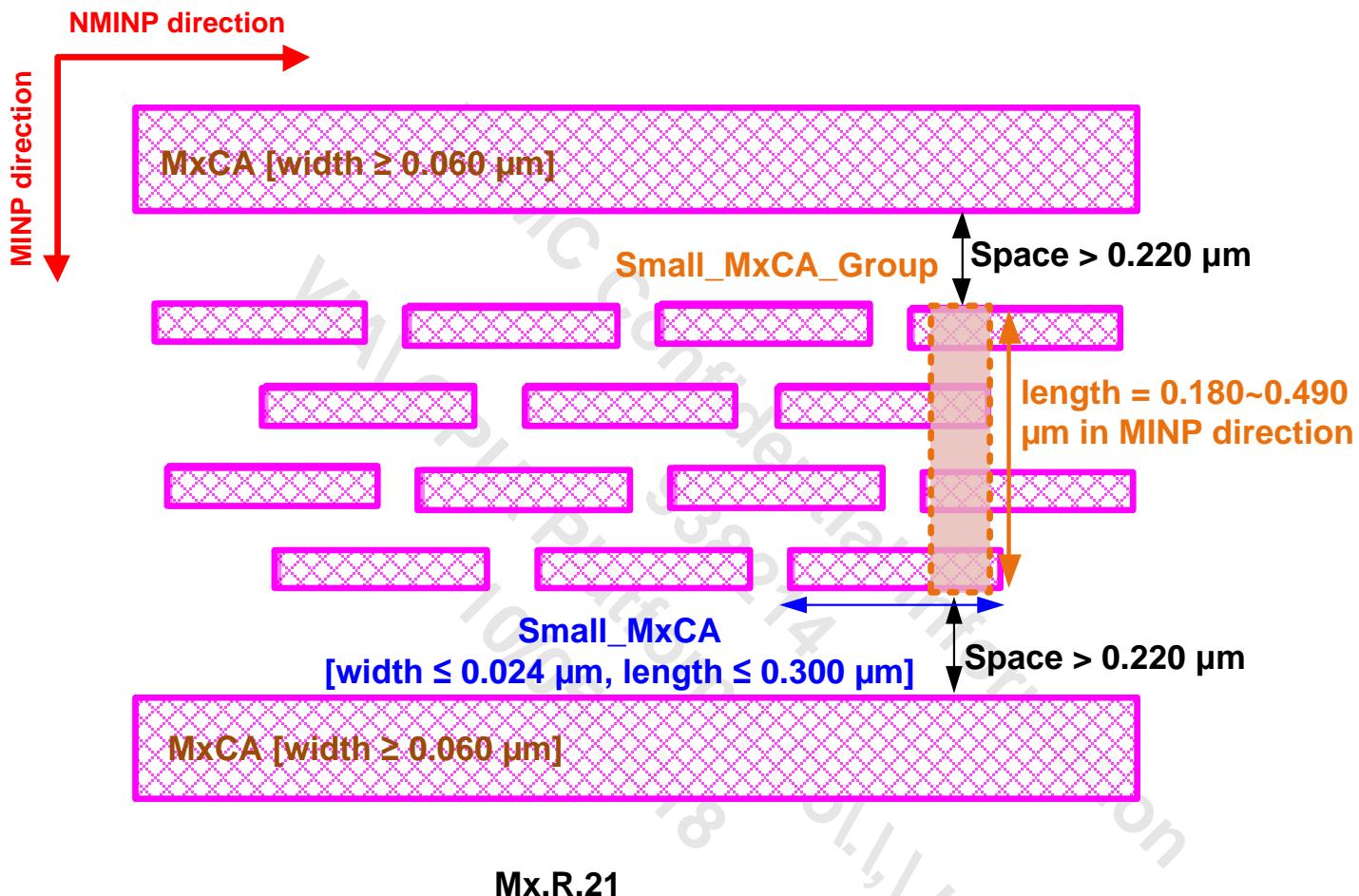


Mx R 15

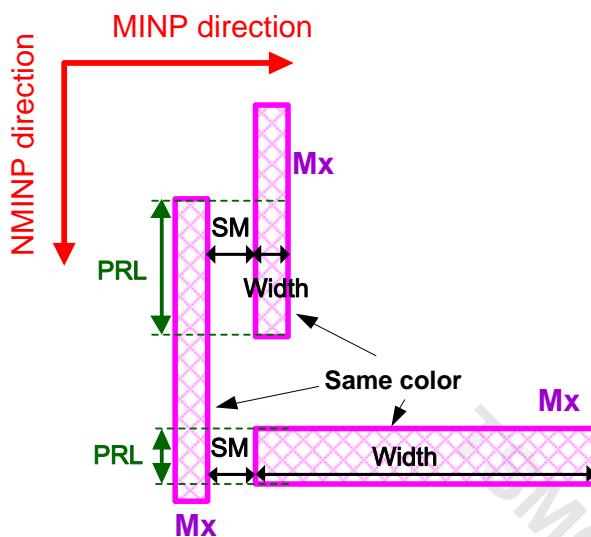


Small_MxCA_Group:
{{{Small_MxCA SIZING up/down 0.033 μm in MINP direction} SIZING down/up 0.0895 μm in MINP direction} [length < 0.140 μm in NMNP direction]} [length = 0.180~0.490 μm in MINP direction]}

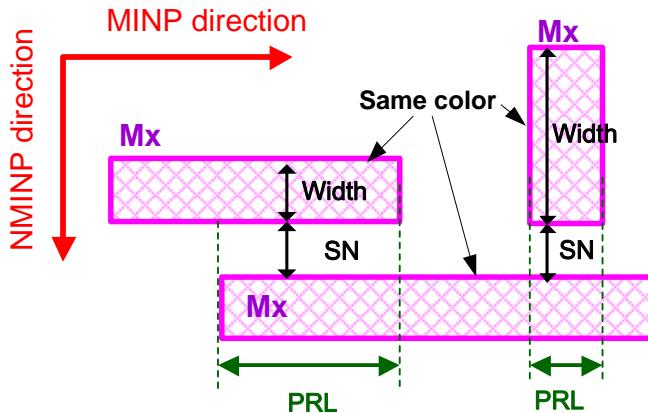
Small_MxCA:
MxCA [width ≤ 0.024 μm in MINP direction, length ≤ 0.300 μm in NMNP direction]



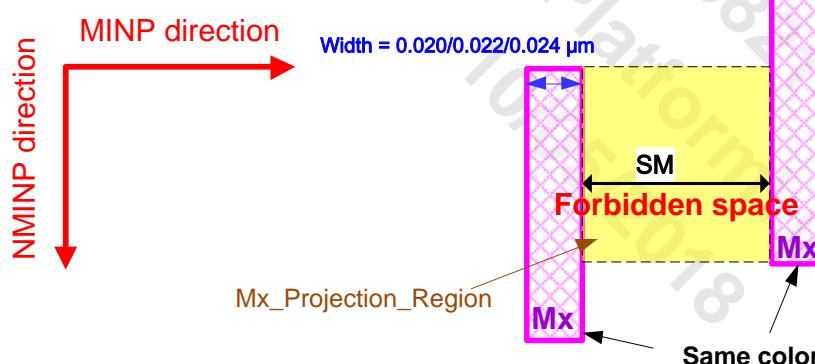
Mx.R.21



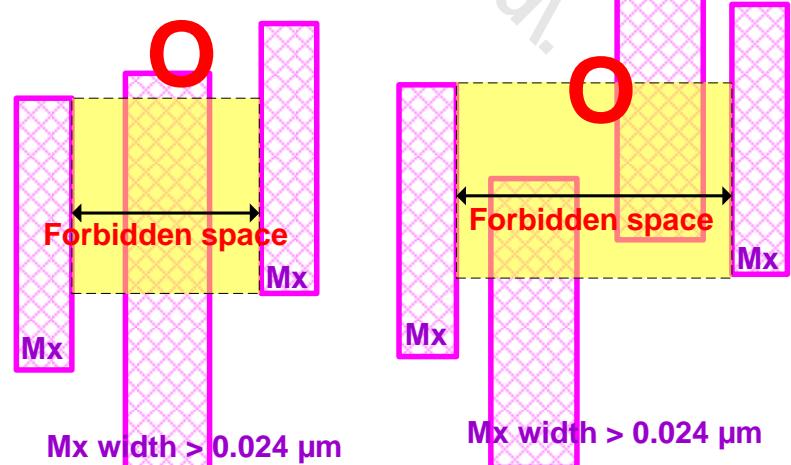
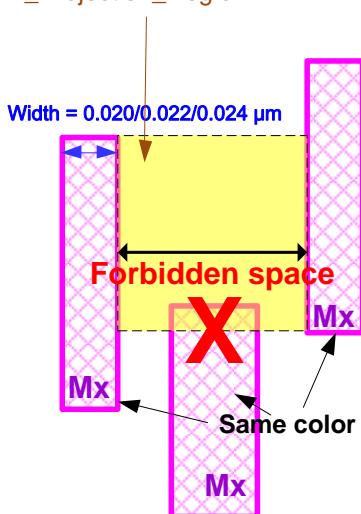
Mx.CS.0.1 / Mx.CS.1.1 / Mx.CS.1.1.1 /
Mx.CS.1.1.3 / Mx.CS.1.1.2 / Mx.CS.1.1.2.1 /
Mx.CS.1.1.3 / Mx.CS.1.1.3.1 / Mx.CS.1.1.3.3 /
Mx.CS.1.1.4 / Mx.CS.1.1.4.11 / Mx.CS.1.1.4.12 /
Mx.CS.1.1.7 / Mx.CS.1.1.8 / Mx.CS.1.2 /
Mx.CS.1.2.1 / Mx.CS.1.3 / Mx.CS.1.6 / Mx.CS.1.7 /
Mx.CS.1.8 / Mx.CS.1.9 / Mx.CS.1.10 / Mx.CS.1.11



Mx.CS.0.2 / Mx.CS.3.2 / Mx.CS.3.3 /
Mx.CS.3.4 / Mx.CS.3.5 / Mx.CS.3.6 /
Mx.CS.3.7 / Mx.CS.3.8 / Mx.CS.3.9 /
Mx.CS.3.10 / Mx.CS.3.11 / Mx.CS.3.12 /
Mx.CS.3.13 / Mx.CS.3.14

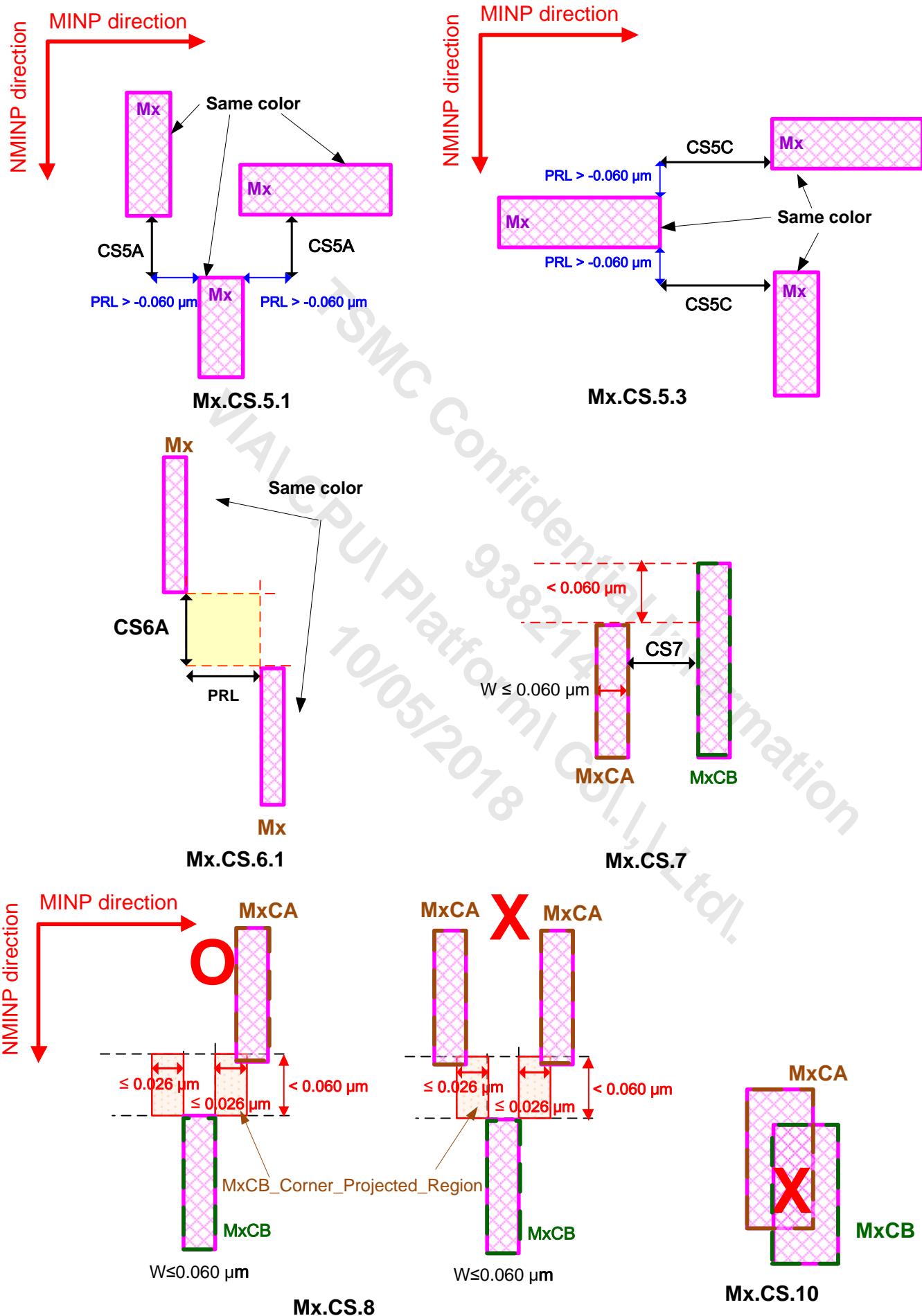


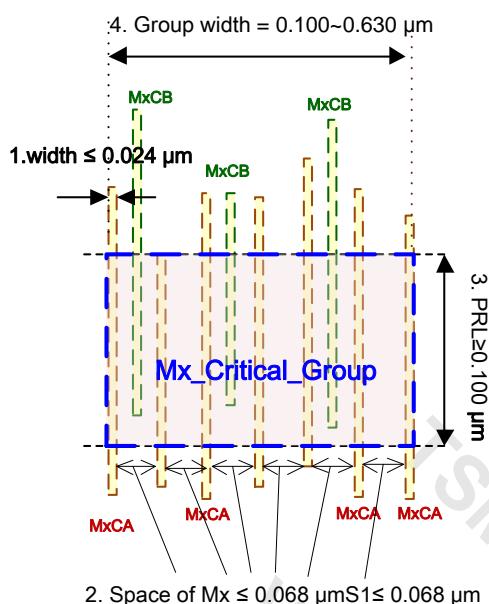
Mx_Projection_Region



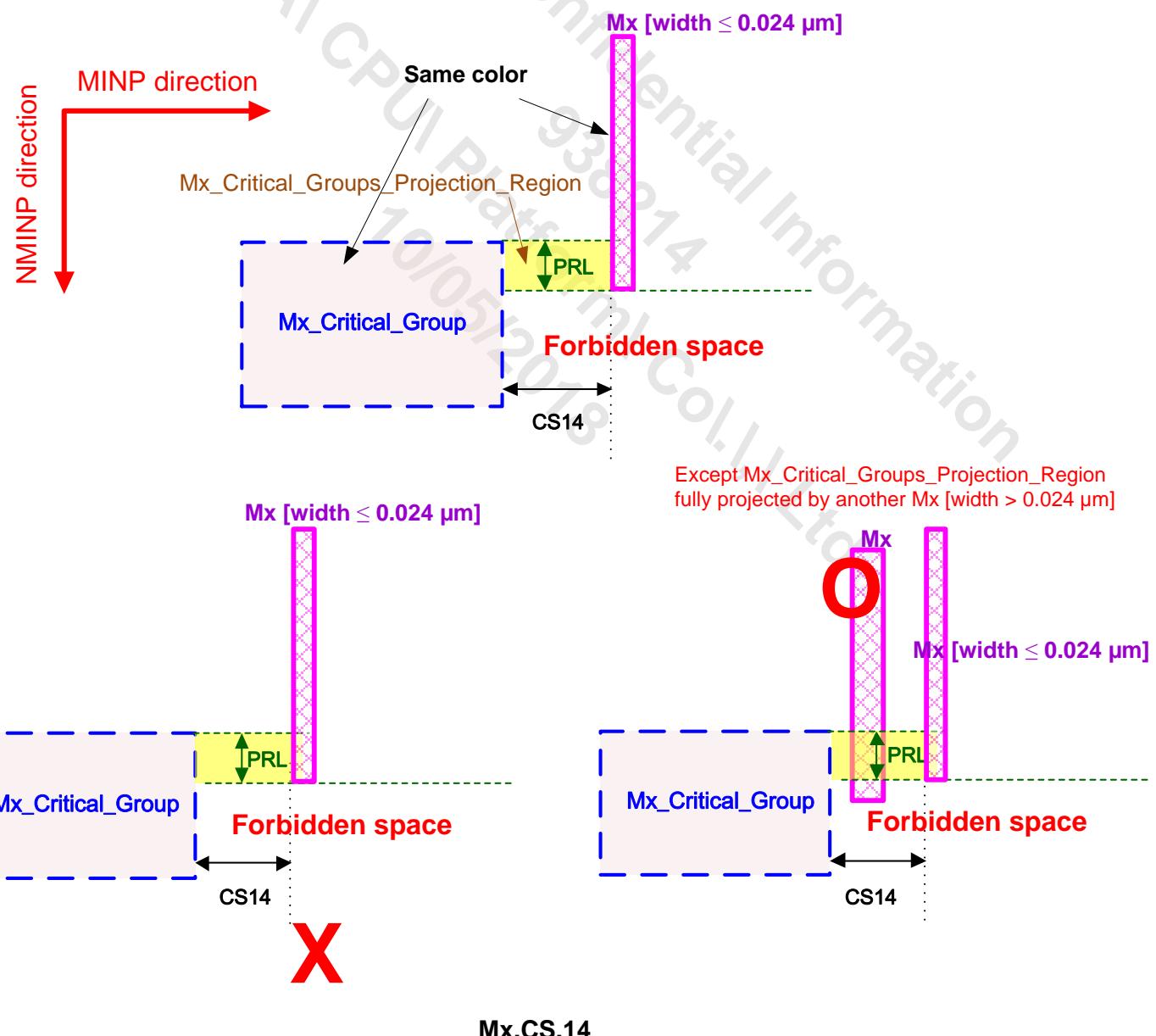
Except Mx_Projection_Region fully projected by another Mx [width > 0.024 μm]

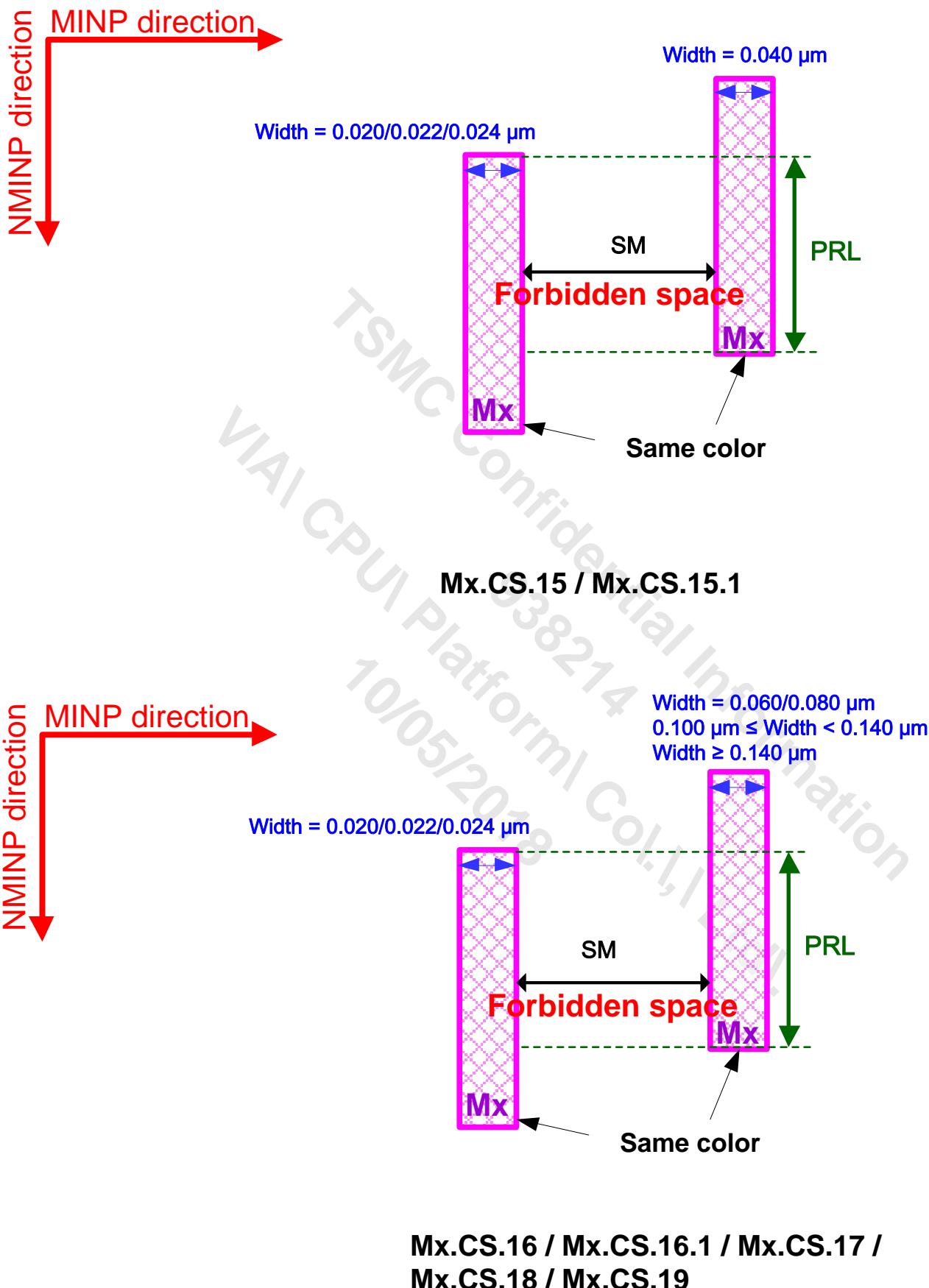
Mx.CS.1.1.6





Definition of Mx_Critical_Group:
 $\{\{Mx [width \leq 0.024 \mu\text{m}] \text{ SIZING up/down } 0.032 \mu\text{m}\} \text{ SIZING down/up } 0.0495 \mu\text{m} \text{ in NMINP direction}\} [0.100 \mu\text{m} \leq \text{width in MINP direction} \leq 0.630 \mu\text{m}]$





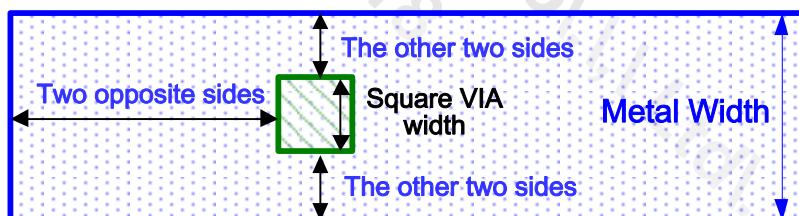
4.5.47.1 Mx Enclosure Rule Tabulation

RuleTable.Mx.EN.31 (Enclosure of square VIA [width = 0.020 µm])

Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
Mx.EN.31.1.T	width < 0.022 µm	0.0300 µm	0 µm	
Mx.EN.31.2.T	0.022 µm ≤ width < 0.024 µm	0.0300 µm	0.0010 µm	
Mx.EN.31.3.T	0.024 µm ≤ width < 0.026 µm	0.0300 µm	0.0020 µm	BLK_WB
Mx.EN.31.4.T	0.026 µm ≤ width < 0.028 µm	0.0300 µm	0.0030 µm	
Mx.EN.31.5.T	0.028 µm ≤ width < 0.040 µm	0.0300 µm	0.0020 µm	BLK_WB
Mx.EN.31.6.T	0.040 µm ≤ width < 0.060 µm	0.0300 µm	0.0100 µm	
Mx.EN.31.7.T	0.060 µm ≤ width < 0.080 µm	0.0250 µm	0.0200 µm	BLK_WB
Mx.EN.31.8.T	0.080 µm ≤ width < 0.260 µm	0.0180 µm	0.0300 µm	BLK_WB
Mx.EN.31.9.T	width ≥ 0.260 µm	0.0600 µm	0.0250 µm	

RuleTable.Mx.EN.34 (Enclosure of square VIA [width = 0.038 µm])

Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
Mx.EN.34.1.T	width < 0.060 µm	0.0590 µm	0.0010 µm	
Mx.EN.34.2.T	0.060 µm ≤ width < 0.080 µm	0.0500 µm	0.0110 µm	
Mx.EN.34.3.T	0.080 µm ≤ width < 0.100 µm	0.0430 µm	0.0210 µm	
Mx.EN.34.4.T	0.100 µm ≤ width < 0.120 µm	0.0430 µm	0.0310 µm	
Mx.EN.34.5.T	0.120 µm ≤ width < 0.260 µm	0.0400 µm	0.0400 µm	
Mx.EN.34.6.T	width ≥ 0.260 µm	0.0600 µm	0.0500 µm	



RuleTable.Mx.EN.32 (Enclosure of rectangular VIA [length = 0.050 μm])

Rule Number	Metal Width	Short side	Long side	Exception
Mx.EN.32.1.T	width < 0.022 μm	0.0300 μm	0 μm	
Mx.EN.32.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	
Mx.EN.32.3.T	0.024 μm ≤ width < 0.026 μm	0.0300 μm	0.0020 μm	
Mx.EN.32.4.T	0.026 μm ≤ width < 0.028 μm	0.0300 μm	0.0030 μm	
Mx.EN.32.5.T	0.028 μm ≤ width < 0.040 μm	0.0300 μm	0.0020 μm	BLK_WB
Mx.EN.32.6.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	
Mx.EN.32.7.T	0.060 μm ≤ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
Mx.EN.32.8.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
Mx.EN.32.9.T	0.080 μm < width < 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	BLK_WB
Mx.EN.32.10.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	

RuleTable.Mx.EN.33 (Enclosure of rectangular VIA [length = 0.034 μm])

Rule Number	Metal Width	Short side	Long side	Exception
Mx.EN.33.1.T	width < 0.022 μm	0.0300 μm	0 μm	
Mx.EN.33.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	
Mx.EN.33.3.T	0.024 μm ≤ width < 0.026 μm	0.0300 μm	0.0020 μm	
Mx.EN.33.4.T	0.026 μm ≤ width < 0.028 μm	0.0300 μm	0.0030 μm	
Mx.EN.33.5.T	0.028 μm ≤ width < 0.040 μm	0.0300 μm	0.0020 μm	BLK_WB
Mx.EN.33.6.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	
Mx.EN.33.7.T	0.060 μm ≤ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
Mx.EN.33.8.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
Mx.EN.33.9.T	0.080 μm < width < 0.260 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	BLK_WB
Mx.EN.33.10.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	

Rule No.	Description	Label	Op.	Rule
Mx.EN.31.1.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$		\geq	0.0300
Mx.EN.31.2.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.022 $\mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
Mx.EN.31.3.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.024 $\mu\text{m} \leq \text{width} < 0.026 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
Mx.EN.31.4.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.026 $\mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0030 \mu\text{m}$		\geq	0.0300
Mx.EN.31.5.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
Mx.EN.31.6.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.040 $\mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
Mx.EN.31.7.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.060 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$ (Except BLK_WB)		\geq	0.0250
Mx.EN.31.8.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [0.080 $\mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$ (Except BLK_WB)		\geq	0.0180
Mx.EN.31.9.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mx [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
Mx.EN.32.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0300
Mx.EN.32.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.022 $\mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
Mx.EN.32.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.024 $\mu\text{m} \leq \text{width} < 0.026 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
Mx.EN.32.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.026 $\mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] with the other two long sides $\geq 0.0030 \mu\text{m}$		\geq	0.0300
Mx.EN.32.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
Mx.EN.32.6.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.040 $\mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
Mx.EN.32.7.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.060 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
Mx.EN.32.8.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
Mx.EN.32.9.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [0.080 $\mu\text{m} < \text{width} < 0.260 \mu\text{m}$] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$ (Except BLK_WB)		\geq	0.0250/0.0300

Rule No.	Description	Label	Op.	Rule
Mx.EN.32.10.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mx [width \geq 0.260 μm] with the other two long sides \geq 0.0250 μm		\geq	0.0600
Mx.EN.33.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [width < 0.022 μm] with the other two long sides \geq 0 μm		\geq	0.0300
Mx.EN.33.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.022 μm \leq width < 0.024 μm] with the other two long sides \geq 0.0010 μm		\geq	0.0300
Mx.EN.33.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.024 μm \leq width < 0.026 μm] with the other two long sides \geq 0.0020 μm		\geq	0.0300
Mx.EN.33.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.026 μm \leq width < 0.028 μm] with the other two long sides \geq 0.0030 μm		\geq	0.0300
Mx.EN.33.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.028 μm \leq width < 0.040 μm] with the other two long sides \geq 0.0020 μm (Except BLK_WB)		\geq	0.0300
Mx.EN.33.6.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.040 μm \leq width < 0.060 μm] with the other two long sides \geq 0.0100 μm		\geq	0.0300
Mx.EN.33.7.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.060 μm \leq width < 0.080 μm] with the other two long sides \geq 0.0200/0.0250 μm		\geq	0.0250/0.0050
Mx.EN.33.8.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [width = 0.080 μm] with the other two long sides \geq 0.0200/0.0300 μm		\geq	0.0250/0.0150
Mx.EN.33.9.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [0.080 μm < width < 0.260 μm] with the other two long sides \geq 0.0300/0.0250 μm (Except BLK_WB)		\geq	0.0250/0.0300
Mx.EN.33.10.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mx [width \geq 0.260 μm] with the other two long sides \geq 0.0250 μm		\geq	0.0600
Mx.EN.34.1.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mx [width < 0.060 μm] for two opposite sides with the other two sides \geq 0.0010 μm		\geq	0.0590
Mx.EN.34.2.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mx [0.060 μm \leq width < 0.080 μm] for two opposite sides with the other two sides \geq 0.0110 μm		\geq	0.0500
Mx.EN.34.3.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mx [0.080 μm \leq width < 0.100 μm] for two opposite sides with the other two sides \geq 0.0210 μm		\geq	0.0430
Mx.EN.34.4.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mx [0.100 μm \leq width < 0.120 μm] for two opposite sides with the other two sides \geq 0.0310 μm		\geq	0.0430
Mx.EN.34.5.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mx [0.120 μm \leq width < 0.260 μm] for two opposite sides with the other two sides \geq 0.0400 μm		\geq	0.0400
Mx.EN.34.6.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mx [width \geq 0.260 μm] for two opposite sides with the other two sides \geq 0.0500 μm		\geq	0.0600

4.5.48 VIAxa Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
VIAxa.W.1	Width (Except SEALRING_ALL)	W1	=	0.0200, 0.0380
VIAxa.W.2	Width of VIAxa bar in SEALRING_ALL	W2	=	0.1400
VIAxa.S.1	Space (Except SEALRING_ALL)	S1	≥	0.0700
VIAxa.S.1.1	Space of VIAxa [PRL > -0.050 μm] (Except SEALRING_ALL, or following conditions: 1. Space of VIAxa [both VIAxa in same VIAxa_Group]) Definition of VIAxa_Group follows VIAxa.S.20	S1A	≥	0.0940
VIAxa.S.1.2	Space of VIAxa (Except SEALRING_ALL, or following conditions: 1. Space of VIAxa [both VIAxa in same VIAxa_Group]) Definition of VIAxa_Group follows VIAxa.S.20	S1B	≥	0.0870
VIAxa.S.2	Space of the long side of rectangular VIAxa [length = 0.050 μm] to rectangular VIAxa [PRL > -0.089 μm]	S2	≥	0.1000
VIAxa.S.2.1	Space of the short side of rectangular VIAxa [length = 0.050 μm] to VIAxa [PRL > -0.034 μm]	S2A	≥	0.1340
VIAxa.S.2.1.1	Space of the long side of rectangular VIAxa [length = 0.050 μm] to square VIAxa [PRL > -0.105 μm] (Except following conditions: 1. VIA2 space inside {VIA2 [INSIDE {BLK_M3 AND BLK_M2}] SIZING 0.0455 μm})	S2A1	≥	0.0910
VIAxa.S.2.1.2	Space of the long side of rectangular VIAxa [length = 0.050 μm] to square VIAxa [PRL > -0.073 μm]	S2A2	≥	0.0950
VIAxa.S.2.2	Space of the short side of rectangular VIAxa [length = 0.050 μm] to rectangular VIAxa [PRL > -0.044 μm]	S2B	≥	0.1340
VIAxa.S.2.3	Corner-to-corner space of rectangular VIAxa [length = 0.050 μm] to rectangular VIAxa [long side PRL ≤ -0.089 μm, short side ≤ -0.044 μm from rectangular VIAxa [length = 0.050 μm]]	S2C	≥	0.1340
VIAxa.S.3	Space of the long side of rectangular VIAxa [length = 0.034 μm] to VIAxa [PRL > -0.093 μm]	S3	≥	0.1000
VIAxa.S.3.1	Space of the short side of rectangular VIAxa [length = 0.034 μm] to VIAxa [PRL > -0.060 μm]	S3A	≥	0.1280
VIAxa.S.3.2	Corner-to-corner space of rectangular VIAxa [length = 0.034 μm] to rectangular VIAxa [long side PRL ≤ -0.093 μm, short side ≤ -0.060 μm from rectangular VIAxa [length = 0.034 μm]]	S3B	≥	0.1340
VIAxa.S.8	Space to VIAxa-1 or VIAx-1 [maximum delta V > 0.96V]	S8	≥	0.0620
VIAxa.S.8.1	Space to VIAxa-1 or VIAx-1 [maximum delta V > 1.32V] (1.2V + 10%)	S8	≥	0.0640
VIAxa.S.8.2	Space to VIAxa-1 or VIAx-1 [maximum delta V > 1.65V] (1.5V + 10%)	S8	≥	0.0700
VIAxa.S.8.3	Space to VIAxa or VIAxa-1 or VIAx-1 [maximum delta V > 1.98V] (1.8V + 10%)	S8	≥	0.0820
VIAxa.S.8.4	Space to VIAxa or VIAxa-1 or VIAx-1 [maximum delta V > 2.75V] (2.5V + 10%)	S8	≥	0.0870
VIAxa.S.11	Space of the long side of rectangular VIAxa [PRL > 0 μm (L1), with Mxa+1 in between, and Mxa+1 width < 0.024 μm]	S11	≥	0.0680
VIAxa.S.20	Space to VIAxa_Group Definition of VIAxa_Group: 2 square VIAxa space < 0.074 μm, or 0.078 μm < space < 0.081 μm, or 0.084 μm < space < 0.085 μm [PRL ≤ -0.020 μm] in diagonal direction in one group, and DRC flags the square VIAxa numbers > 2 in one group.	S20	≥	0.0900
VIAxa.S.21	Space of VIAxa [width = 0.038 μm] to VIAxa	S21	≥	0.0920
VIAxa.S.21.1	Space of VIAxa [width = 0.038 μm] to VIAxa [PRL > -0.050 μm]	S21A	≥	0.1120

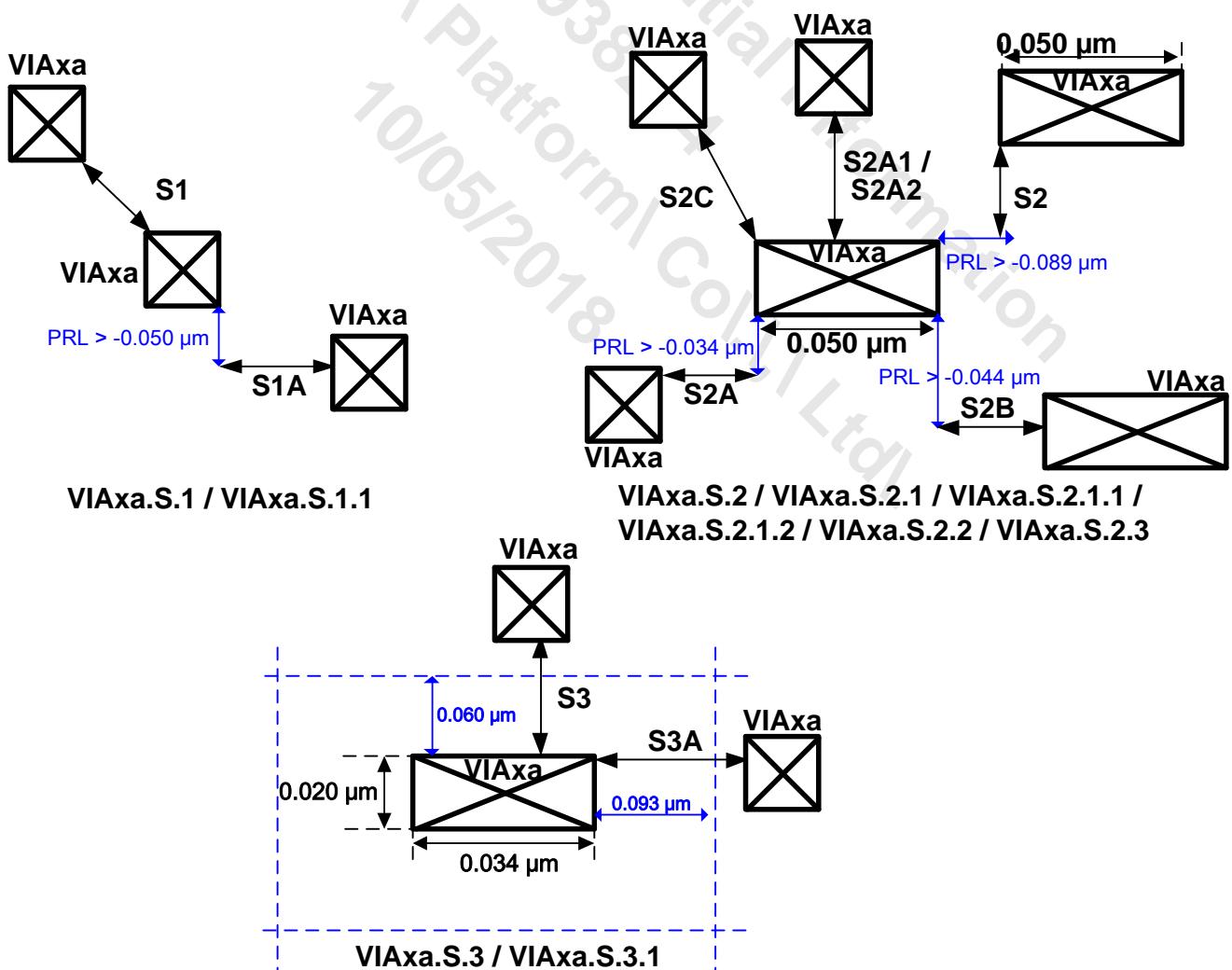
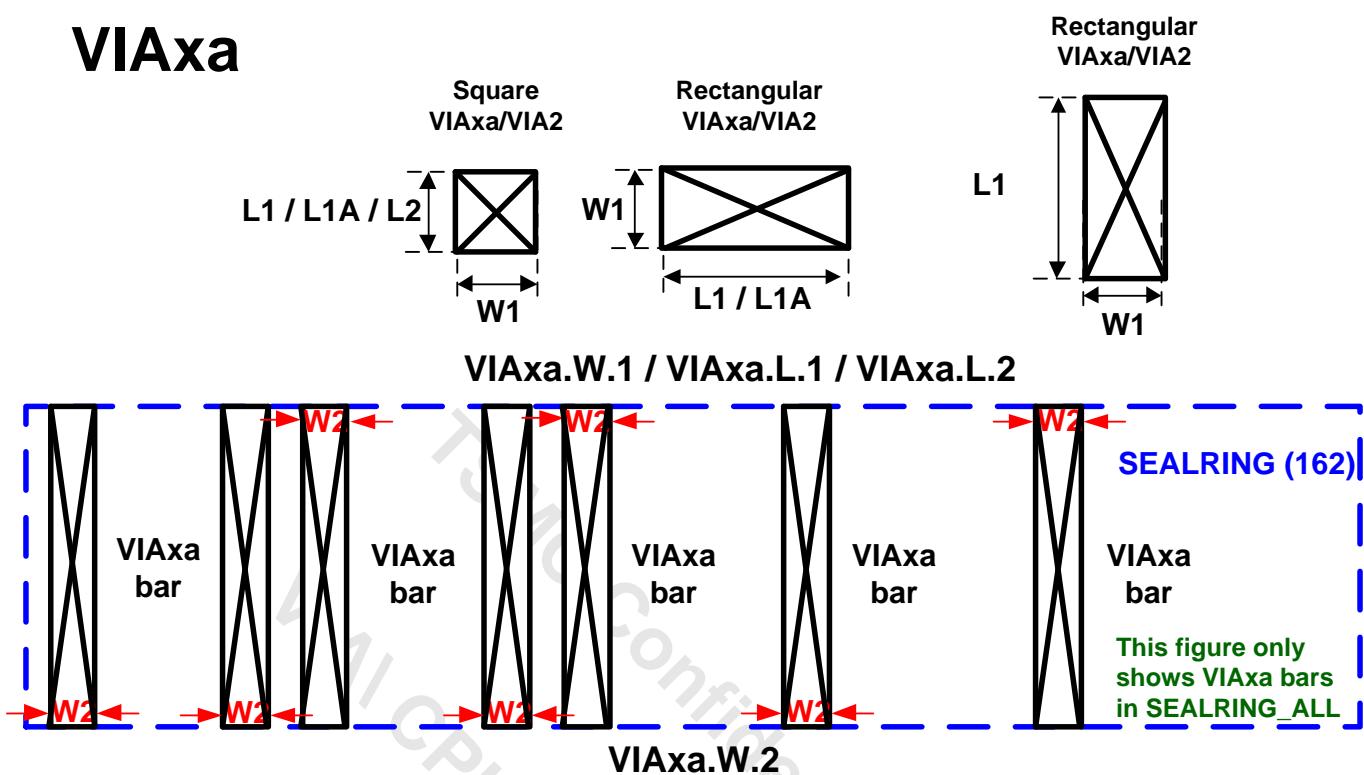
Rule No.	Description	Label	Op.	Rule
VIAxa.S.21.2	Space of VIAxa [width = 0.038 μm] to square VIAxa [width = 0.020 μm]	S21B	≥	0.1040
VIAxa.S.21.3	Space of VIAxa [width = 0.038 μm] to rectangular VIAxa	S21C	≥	0.5000
VIAxa.EN.0	1. Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] is defined by RuleTable.VIAxa.EN.31 in the subsection 2. Enclosure of square VIAxa ($xa > 2$) [width = 0.038 μm] is defined by RuleTable.VIAxa.EN.33 in the subsection 3. Enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] is defined by RuleTable.VIAxa.EN.32 in the subsection 4. Enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] is defined by RuleTable.VIAxa.EN.34 in the subsection 5. Enclosure of square VIA2 [width = 0.020 μm] is defined by RuleTable.VIAxa.EN.35 in the subsection 6. Enclosure of square VIA2 [width = 0.038 μm] is defined by RuleTable.VIAxa.EN.37 in the subsection 7. Enclosure of rectangular VIA2 [length = 0.050 μm] is defined by RuleTable.VIAxa.EN.36 in the subsection 8. Enclosure of rectangular VIA2 [length = 0.034 μm] is defined by RuleTable.VIAxa.EN.38 in the subsection			
VIAxa.EN.1.2.1	Enclosure of square VIAxa by Mxs, Mx or Mxa [width = 0.028 μm, INTERACT BCWDMY] with the other two sides $\geq 0.004 \mu m$ ($xa \geq 3$)	EN1	≥	0.0300
VIAxa.EN.1.2.2	Enclosure of square VIA2 by M2 [width = 0.028 μm, INTERACT BCWDMY] with the other two sides $\geq 0.004 \mu m$	EN1	≥	0.0280
VIAxa.EN.16.10	Checked_VIAxa_Edge1 enclosure by Mxs (32;400), Mx or Mxa in Mxs, Mx or Mxa MINP direction (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2}) Definition of Checked_VIAxa: VIAxa INTERACT Mxa+1 width > 0.040 μm Definition of Checked_VIAxa_Edge1: 1. Checked_VIAxa edge space to Mxs (32;400), {MxCA OR MxCB} or {MxaCA OR MxaCB} < 0.040 μm with PRL > -0.100 μm in Mxs, Mx or Mxa MINP direction	EN16J	≥	0.0010
VIAxa.EN.16.10.1	Checked_VIAxa_Edge2 enclosure by Mxs (32;400), Mx or Mxa in Mxs, Mx or Mxa MINP direction (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2}) Definition of Checked_VIAxa: VIAxa INTERACT Mxa+1 width > 0.040 μm Definition of Checked_VIAxa_Edge2: 1. Checked_VIAxa edge space to Mxs (32;400), {MxCA OR MxCB} or {MxaCA OR MxaCB} < 0.040 μm with PRL > -0.100 μm in Mxs, Mx or Mxa MINP direction, and 2. Checked_VIAxa edge space to VIAx or VIAxa-1 < 0.026 μm [PRL > 0, different net]	EN16J	≥	0.0020
VIAxa.EN.21.6.1	Short side enclosure of rectangular VIAxa by Mxs, Mx or Mxa [width = 0.028 μm, INTERACT BCWDMY] with the other two long side enclosure $\geq 0.004 \mu m$ ($xa \geq 3$)	EN21	≥	0.0300
VIAxa.EN.21.6.2	Short side enclosure of rectangular VIA2 by M2 [width = 0.028 μm, INTERACT BCWDMY] with the other two long side enclosure $\geq 0.004 \mu m$	EN21	≥	0.0280
VIAxa.EN.21.10	Short side enclosure of rectangular VIAxa by Mxs, Mx or Mxa edge [length = 0.080 μm, Mx/Mxa width = 0.080 μm]	EN21	≥	0.0250
VIAxa.L.1	Length of VIAxa [width = 0.020 μm]	L1	=	0.0200, 0.0340, 0.0500
VIAxa.L.2	Length of VIAxa [width = 0.038 μm]	L2	=	0.0380
VIAxa.R.0	45-degree VIAxa is not allowed			

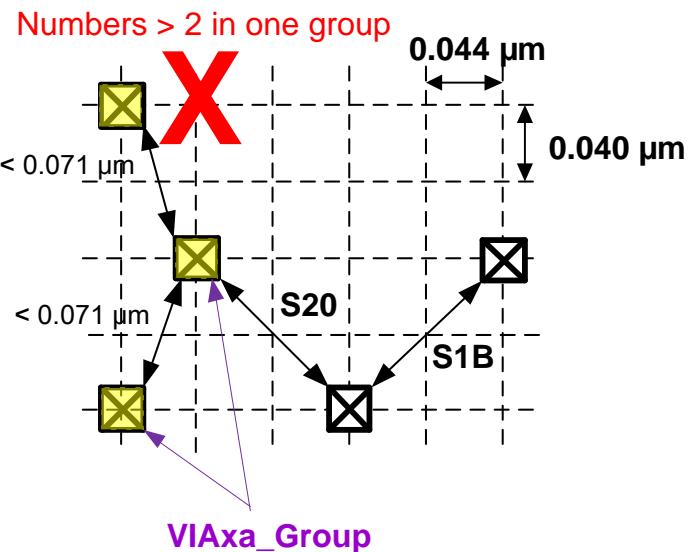
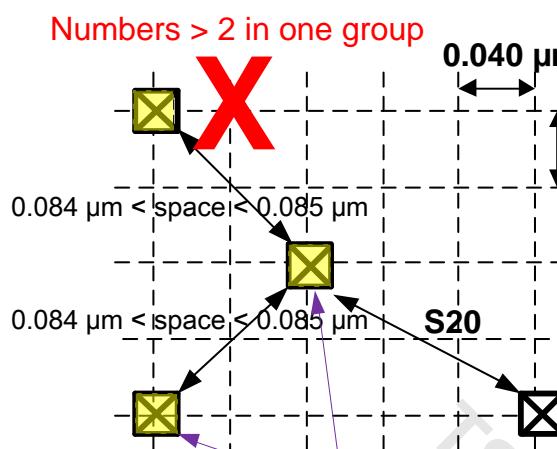
Rule No.	Description	Label	Op.	Rule
VIAxa.R.2	Redundant via requirement must follow RuleTable.VIAxa.R.2 of VIAxa numbers and space (S1) for Mxs/Mx/Mxa and Mxa+1 connection. [One of Mxs/Mx/Mxa or Mxa+1 has width and length (W1) > 0.160 μm]. (Except following conditions: 1. VIA bar)			
VIAxa.R.2.1	Redundant via requirement must follow RuleTable.VIAxa.R.2.1 of VIAxa numbers and space (S1) for Mxs/Mx/Mxa and Mxa+1 connection. [One of Mxs/Mx/Mxa or Mxa+1 has width and length (W1) > 0.300 μm]. (Except following conditions: 1. VIA bar)			
VIAxa.R.3	Redundant via requirement must follow RuleTable.VIAxa.R.3 of VIAxa numbers and space (S1) for Mx/Mxa and Mxa+1 connection. [One of Mxs/Mx/Mxa or Mxa+1 has width and length (W1) > 0.412 μm]. Refer to VIAxa.R.3 table behind. (Except following conditions: 1. VIA bar)			
VIAxa.R.7	VIAxa must be fully covered by {Mxs AND Mxa+1}, {Mx AND Mxa+1} or {Mxa AND Mxa+1}			
VIAxa.R.9®	Recommended maximum consecutive stacked VIAxa layer, which has only one via for each VIAxa layer to avoid high R_c		\leq	4
VIAxa.R.10	Overlap MetalFuse_B1 (156;8) is not allowed			
VIAxa.R.13	Maximum area ratio of Mxs/Mx/Mxa to upper VIAxa in the same net [connects to gate with area > 10700 μm^2 , and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	350000
VIAxa.R.13.2	Maximum area ratio of I/O gate to single layer VIAxa in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area \geq 0.25 μm^2) Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	300000
VIAxa.R.19	Isolated VIAxa is not allowed. (Except SEALRING_ALL) DRC flags VIAxa without neighboring {VIAxa OR DVIAxa} distance \leq 4 μm			
VIAxa.R.21	VIAxa interact VIAxa_Empty_Space_100 is not allowed in chip level (Except following conditions: 1. INDDMY, SEALRING_ALL for VIAxa_Empty_Space_100) Definition of VIAxa_Empty_Space_100: {CHIP NOT {VIAxa OR DVIAxa}} SIZING down/up 50 μm			
VIAxa.R.21.1	VIAxa interact VIAxa_Empty_Space_50 is not allowed in cell level (Except following conditions: 1. INDDMY for VIAxa_Empty_Space_50) Definition of VIAxa_Empty_Space_50: {CHIP NOT {VIAxa OR DVIAxa}} SIZING down/up 25 μm			

Rule No.	Description	Label	Op.	Rule
VIAxa.R.22	<p>Checked_VIAxa space to two or more VIAxa $< 0.100 \mu\text{m}$ [PRL $> 0 \mu\text{m}$] is not allowed</p> <p>Definition of Checked_VIAxa: VIAxa interact VIAxa_Group</p> <p>Definition of VIAxa_Group: 2 square VIAxa space $< 0.074 \mu\text{m}$, or $0.078 \mu\text{m} < \text{space} < 0.081 \mu\text{m}$, or $0.084 \mu\text{m} < \text{space} < 0.085 \mu\text{m}$ [PRL $\leq -0.020 \mu\text{m}$] in diagonal direction in one group, and DRC flags the square VIAxa numbers > 2 in one group.</p>			

Table Notes:

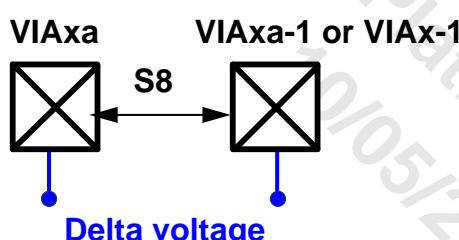
- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

VIAxa

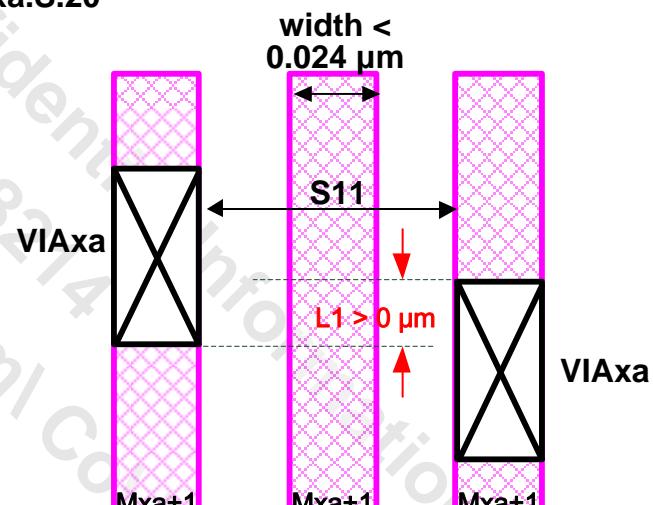


VIAxa_Group:
Space < 0.074 μm ,
0.078 μm < space < 0.081 μm ,
0.084 μm < space < 0.085 μm

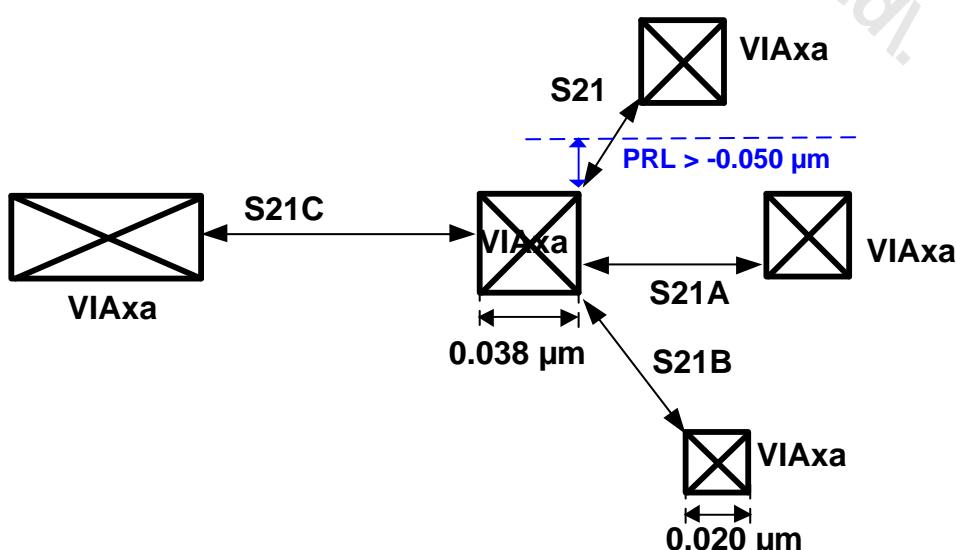
VIAxa.S.1.2 / VIAxa.S.20



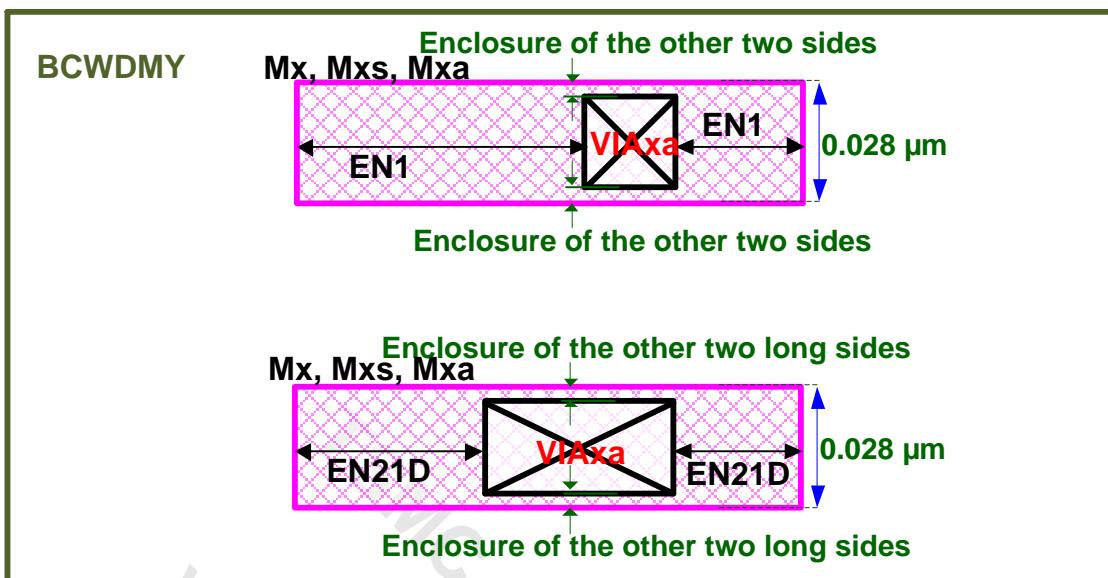
**VIAxa.S.8 / VIAxa.S.8.1 / VIAxa.S.8.2 /
VIAxa.S.8.3 / VIAxa.S.8.4**



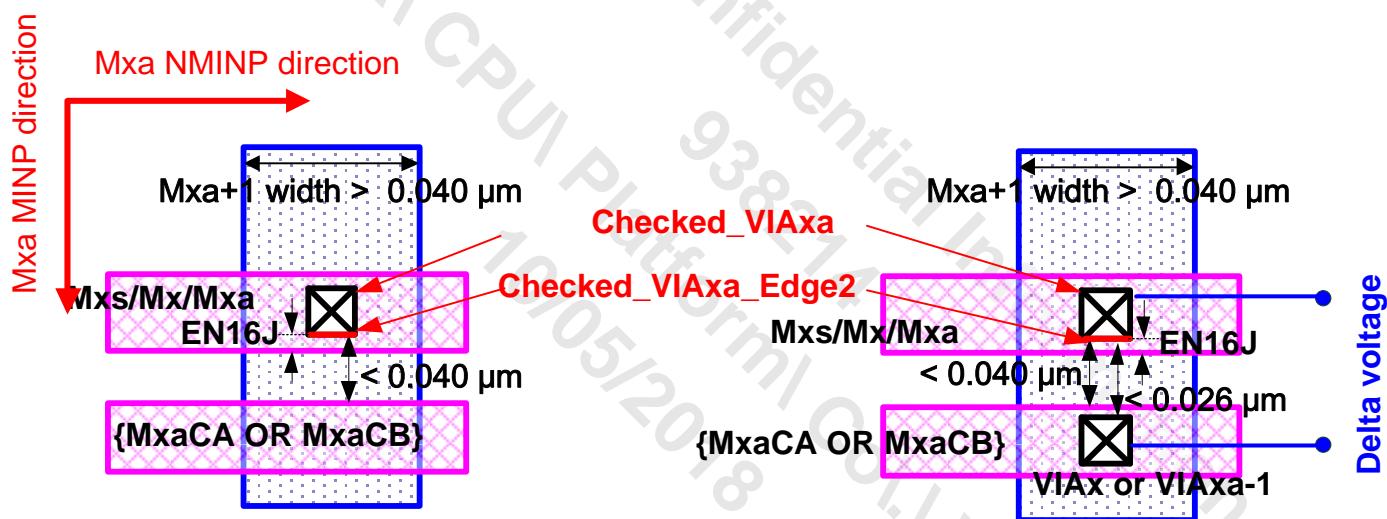
VIAxa.S.11



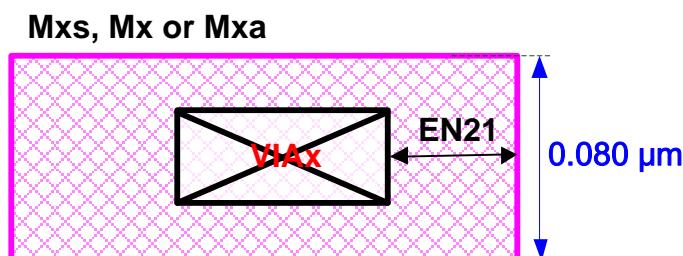
VIAxa.S.21 / VIAxa.S.21.1 / VIAxa.S.21.2 / VIAxa.S.21.3



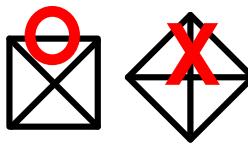
**VIAxa.EN.1.2.1 / VIAxa.EN.1.2.2 /
VIAxa.EN.21.6.1 / VIAxa.EN.21.6.2**



VIAxa.EN.16.10 / VIAxa.EN.16.10.1

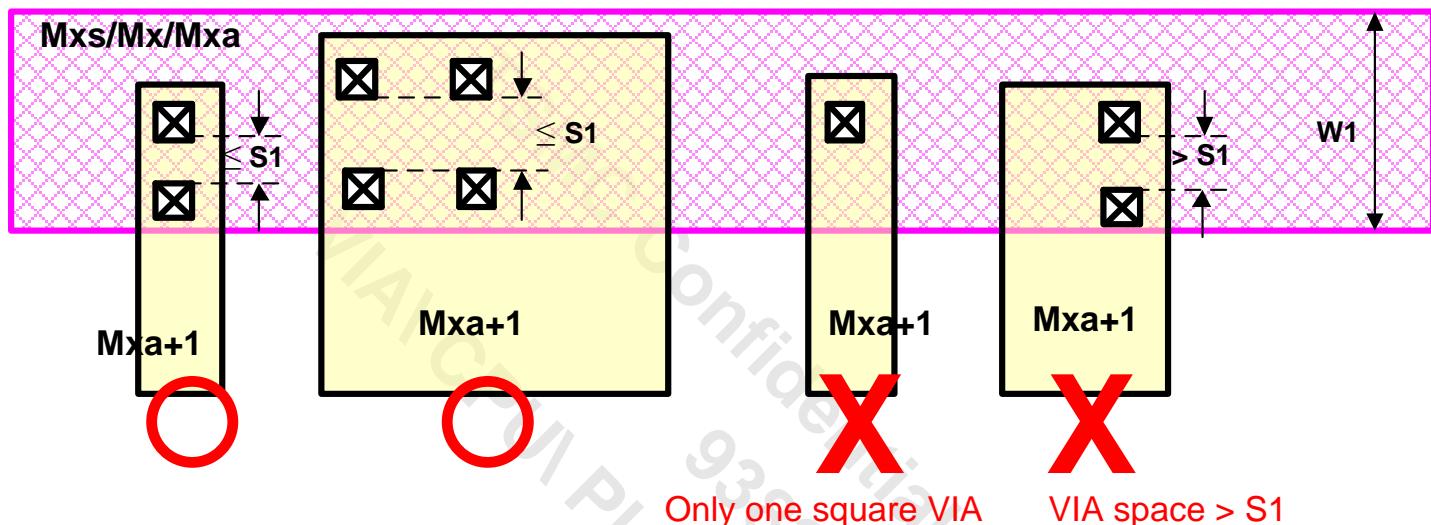


VIAxa.EN.21.10



45-degree VIAxa is not allowed.

VIAxa.R.0

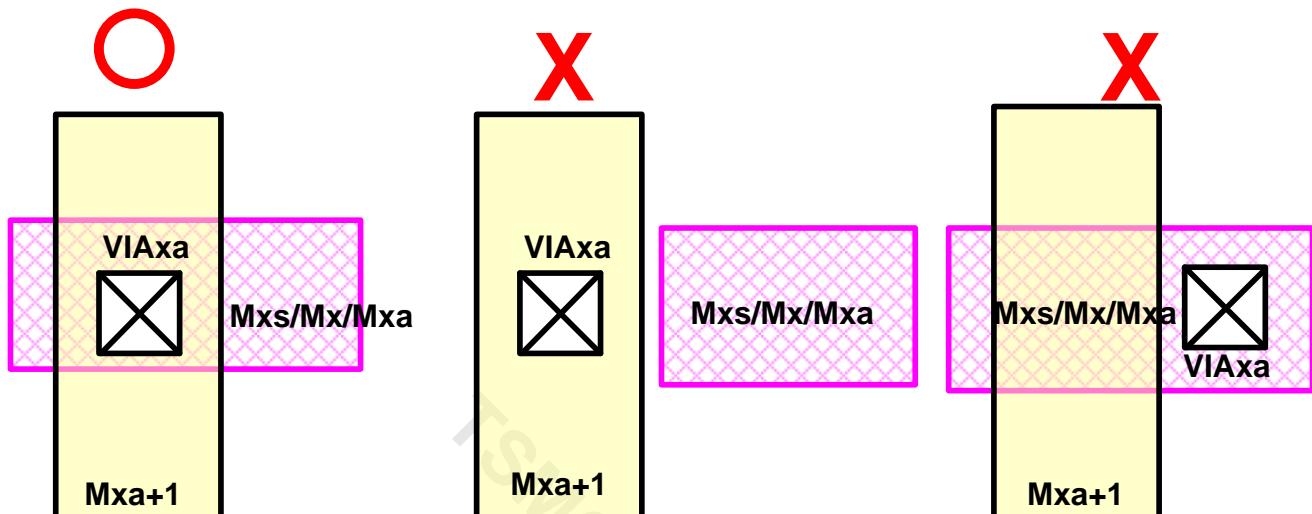


VIAxa.R.2 / VIAxa.R.2.1 / VIAxa.R.3

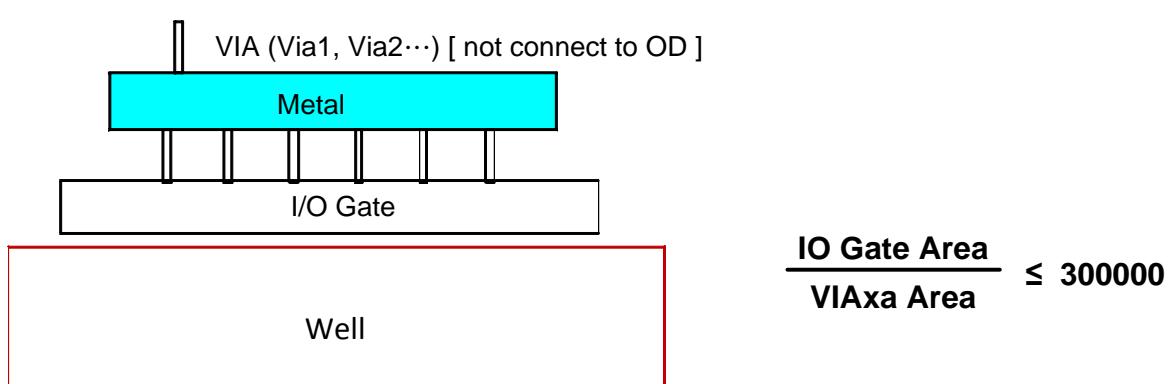
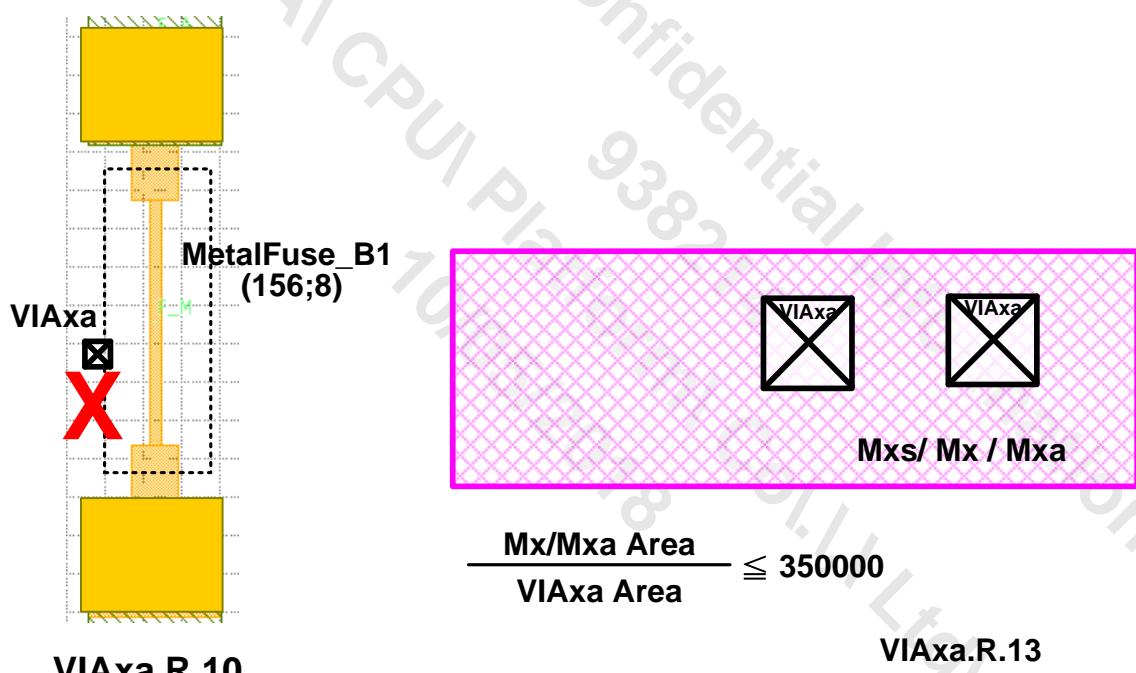
RuleTable.VIAxa.R.2	0.160 μm < W1 ≤ 0.300 μm							
VIAxa space (S1) (μm)	0.070 ≤ S1 ≤ 0.160				0.160 < S1 ≤ 0.400			
{Rectangular VIAxa [width/length = 0.020/0.050 μm] OR square VIAxa [width = 0.038 μm]} (#)	0	1	/	/	0	1	2	/
{Square VIAxa [width = 0.020 μm] OR rectangular VIAxa [width/length = 0.020/0.034 μm]} (#)	≥ 2	≥ 0	/	/	≥ 4	≥ 2	≥ 0	/

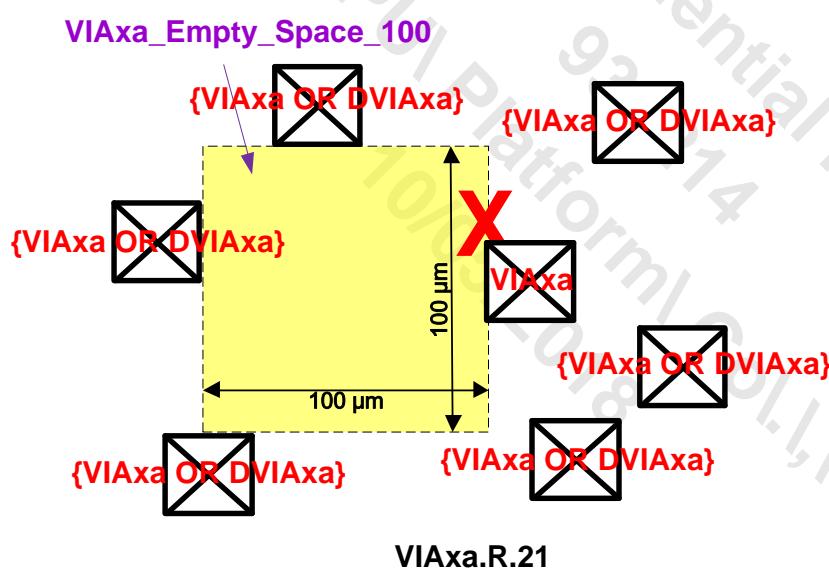
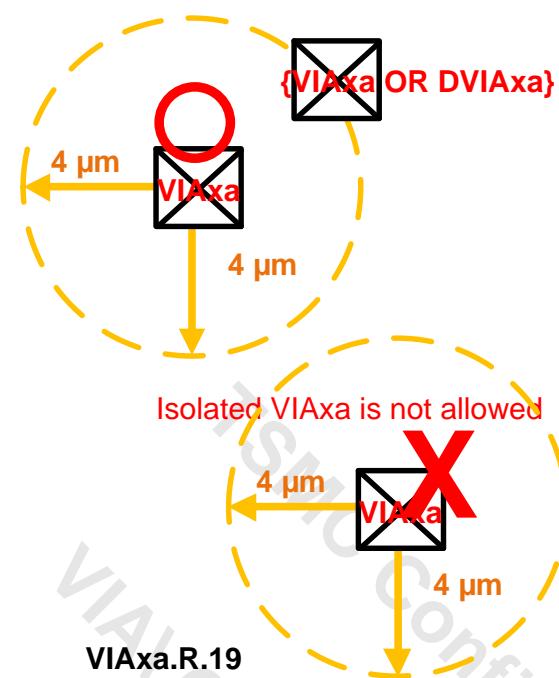
RuleTable.VIAxa.R.2.1	0.300 μm < W1 ≤ 0.412 μm							
VIAxa space (S1) (μm)	0.070 ≤ S1 ≤ 0.160				0.160 < S1 ≤ 0.400			
{Rectangular VIAxa [width/length = 0.020/0.050 μm] OR square VIAxa [width = 0.038 μm]} (#)	0	1	2	0	1	2	3	/
{Square VIAxa [width = 0.020 μm] OR rectangular VIAxa [width/length = 0.020/0.034 μm]} (#)	≥ 3	≥ 1	≥ 0	≥ 6	≥ 4	≥ 2	≥ 0	/

RuleTable.VIAxa.R.3	W1 > 0.412 μm							
VIAxa space (S1) (μm)	0.070 ≤ S1 ≤ 0.160				0.160 < S1 ≤ 0.400			
{Rectangular VIAxa [width/length = 0.020/0.050 μm] OR square VIAxa [width = 0.038 μm]} (#)	0	1	2	0	1	2	3	4
{Square VIAxa [width = 0.020 μm] OR rectangular VIAxa [width/length = 0.020/0.034 μm]} (#)	≥ 4	≥ 2	≥ 0	≥ 9	≥ 7	≥ 5	≥ 3	≥ 1

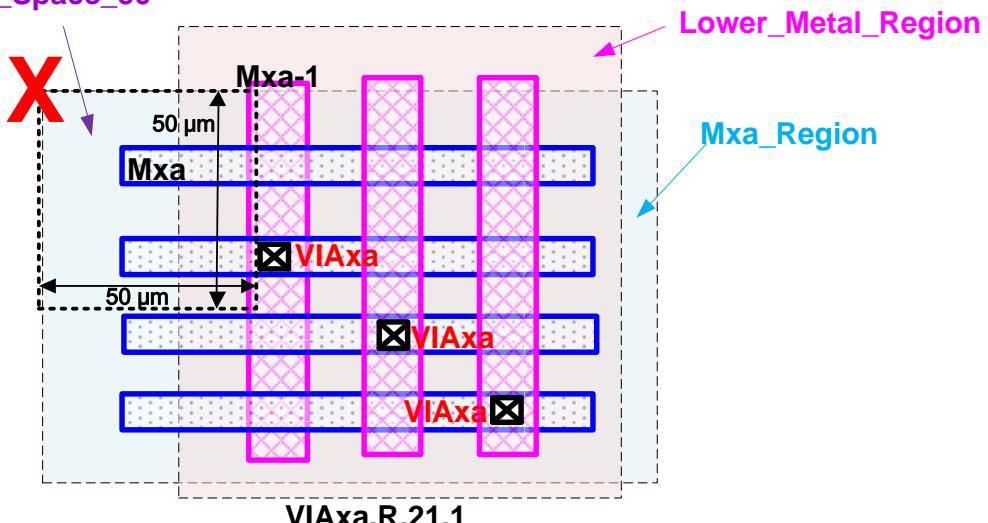


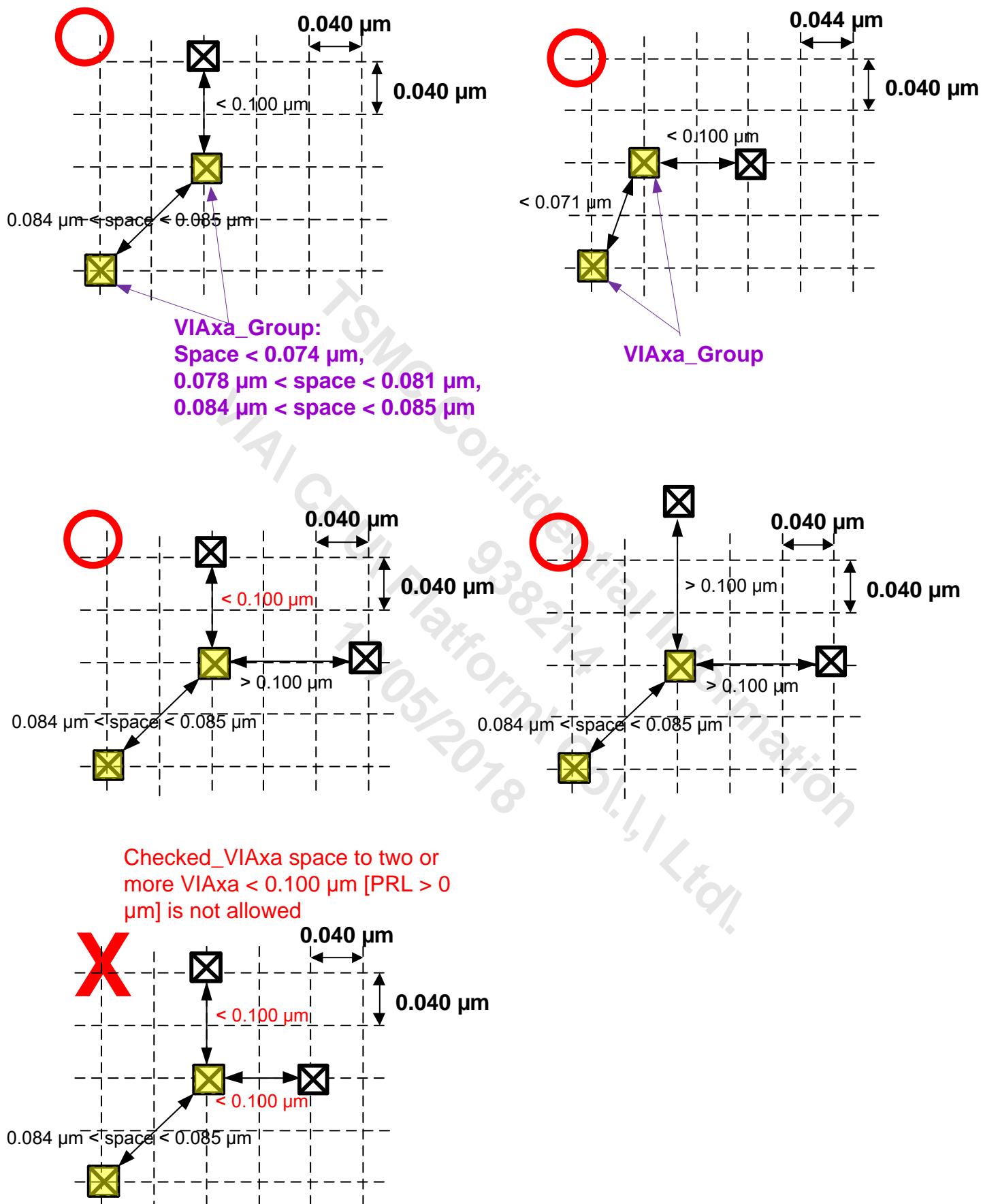
VIAxa.R.7





VIAxa_Empty_Space_50



**VIAxa.R.22**

4.5.48.1 VIAxa (xa = 2) Enclosure Rule Tabulation

RuleTable.VIAxa.EN.35 (Enclosure of square VIAxa (xa = 2) [width = 0.020 µm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAxa.EN.35.1.T	width < 0.022 µm	0.0280 µm	0 µm	
VIAxa.EN.35.2.T	0.022 µm ≤ width < 0.024 µm	0.0280 µm	0.0010 µm	
VIAxa.EN.35.3.T	0.024 µm ≤ width < 0.028 µm	0.0280 µm	0.0020 µm	
VIAxa.EN.35.4.T	0.028 µm ≤ width < 0.040 µm	0.0280 µm	0.0020 µm	
VIAxa.EN.35.5	0.040 µm ≤ width < 0.060 µm	0.0280 µm	0.0100 µm	following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2}
VIAxa.EN.35.5.1.T	0.040 µm ≤ width < 0.060 µm	0.0100 µm	0.0070 µm	
VIAxa.EN.35.6.T	0.060 µm ≤ width < 0.080 µm	0.0250 µm	0.0200 µm	
VIAxa.EN.35.7.T	0.080 µm ≤ width < 0.260 µm	0.0200 µm	0.0300 µm	
VIAxa.EN.35.8.T	width ≥ 0.260 µm	0.0600 µm	0.0250 µm	

RuleTable.VIAxa.EN.37 (Enclosure of square VIAxa (xa = 2) [width = 0.038 µm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAxa.EN.37.1.T	width < 0.060 µm	0.0590 µm	0.0010 µm	
VIAxa.EN.37.2.T	0.060 µm ≤ width < 0.080 µm	0.0500 µm	0.0110 µm	
VIAxa.EN.37.3.T	0.080 µm ≤ width < 0.100 µm	0.0430 µm	0.0210 µm	
VIAxa.EN.37.4.T	0.100 µm ≤ width < 0.120 µm	0.0430 µm	0.0310 µm	
VIAxa.EN.37.5.T	0.120 µm ≤ width < 0.260 µm	0.0400 µm	0.0400 µm	
VIAxa.EN.37.6.T	width ≥ 0.260 µm	0.0600 µm	0.0500 µm	

RuleTable.VIAxa.EN.36 (Enclosure of rectangular VIAxa (xa = 2) [length = 0.050 µm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAxa.EN.36.1.T	width < 0.022 µm	0.0280 µm	0 µm	
VIAxa.EN.36.2.T	0.022 µm ≤ width < 0.024 µm	0.0280 µm	0.0010 µm	
VIAxa.EN.36.3.T	0.024 µm ≤ width < 0.028 µm	0.0280 µm	0.0020 µm	
VIAxa.EN.36.4.T	0.028 µm ≤ width < 0.040 µm	0.0280 µm	0.0020 µm	
VIAxa.EN.36.5.T	0.040 µm ≤ width < 0.060 µm	0.0280 µm	0.0100 µm	
VIAxa.EN.36.6.T	0.060 µm ≤ width < 0.080 µm	0.0250/0.0050 µm	0.0200/0.0250 µm	
VIAxa.EN.36.7.T	width = 0.080 µm	0.0250/0.0150 µm	0.0200/0.0300 µm	
VIAxa.EN.36.8	width > 0.080 µm	0.0250/0.0300 µm	0.0300/0.0250 µm	following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2}

RuleTable.VIAxa.EN.38 (Enclosure of rectangular VIAxa (xa = 2) [length = 0.034 µm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAxa.EN.38.1.T	width < 0.022 µm	0.0280 µm	0.0000 µm	
VIAxa.EN.38.2.T	0.022 µm ≤ width < 0.024 µm	0.0280 µm	0.0010 µm	
VIAxa.EN.38.3.T	0.024 µm ≤ width < 0.028 µm	0.0280 µm	0.0020 µm	
VIAxa.EN.38.4.T	0.028 µm ≤ width < 0.040 µm	0.0280 µm	0.0040 µm	
VIAxa.EN.38.5.T	0.040 µm ≤ width < 0.060 µm	0.0280 µm	0.0100 µm	
VIAxa.EN.38.6.T	0.060 µm ≤ width < 0.080 µm	0.0250/0.0050 µm	0.0200/0.0250 µm	
VIAxa.EN.38.7.T	width = 0.080 µm	0.0250/0.0150 µm	0.0200/0.0300 µm	
VIAxa.EN.38.8.T	width > 0.080 µm	0.0250/0.0300 µm	0.0300/0.0250 µm	

Rule No.	Description	Label	Op.	Rule
VIAxa.EN.35.1.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$		\geq	0.0280
VIAxa.EN.35.2.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [0.022 $\mu\text{m} \leq$ width < 0.024 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0280
VIAxa.EN.35.3.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [0.024 $\mu\text{m} \leq$ width < 0.028 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAxa.EN.35.4.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [0.028 $\mu\text{m} \leq$ width < 0.040 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAxa.EN.35.5	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0280
VIAxa.EN.35.5.1.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0070 \mu\text{m}$		\geq	0.0100
VIAxa.EN.35.6.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.080 μm] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$		\geq	0.0250
VIAxa.EN.35.7.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [0.080 $\mu\text{m} \leq$ width < 0.260 μm] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$		\geq	0.0200
VIAxa.EN.35.8.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.020 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
VIAxa.EN.36.1.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.050 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0280
VIAxa.EN.36.2.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.050 μm] by Lower_Metal [0.022 $\mu\text{m} \leq$ width < 0.024 μm] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0280
VIAxa.EN.36.3.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.050 μm] by Lower_Metal [0.024 $\mu\text{m} \leq$ width < 0.028 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAxa.EN.36.4.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.050 μm] by Lower_Metal [0.028 $\mu\text{m} \leq$ width < 0.040 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAxa.EN.36.5.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.050 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0280
VIAxa.EN.36.6.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.050 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.080 μm] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
VIAxa.EN.36.7.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.050 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
VIAxa.EN.36.8	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.050 μm] by Lower_Metal [width > 0.080 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0250/0.0300
VIAxa.EN.37.1.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.038 μm] by Lower_Metal [width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0590

Rule No.	Description	Label	Op.	Rule
VIAxa.EN.37.2.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.038 μm] by Lower_Metal [$0.060 \mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0110 \mu\text{m}$		\geq	0.0500
VIAxa.EN.37.3.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.038 μm] by Lower_Metal [$0.080 \mu\text{m} \leq \text{width} < 0.100 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0210 \mu\text{m}$		\geq	0.0430
VIAxa.EN.37.4.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.038 μm] by Lower_Metal [$0.100 \mu\text{m} \leq \text{width} < 0.120 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0310 \mu\text{m}$		\geq	0.0430
VIAxa.EN.37.5.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.038 μm] by Lower_Metal [$0.120 \mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0400 \mu\text{m}$		\geq	0.0400
VIAxa.EN.37.6.T	Enclosure of square VIAxa ($xa = 2$) [width = 0.038 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0500 \mu\text{m}$		\geq	0.0600
VIAxa.EN.38.1.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.034 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides $\geq 0.0000 \mu\text{m}$		\geq	0.0280
VIAxa.EN.38.2.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.034 μm] by Lower_Metal [$0.022 \mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0280
VIAxa.EN.38.3.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.034 μm] by Lower_Metal [$0.024 \mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0280
VIAxa.EN.38.4.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.034 μm] by Lower_Metal [$0.028 \mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0040 \mu\text{m}$		\geq	0.0280
VIAxa.EN.38.5.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.034 μm] by Lower_Metal [$0.040 \mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0280
VIAxa.EN.38.6.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.034 μm] by Lower_Metal [$0.060 \mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
VIAxa.EN.38.7.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.034 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
VIAxa.EN.38.8.T	Short side enclosure of rectangular VIAxa ($xa = 2$) [length = 0.034 μm] by Lower_Metal [width > 0.080 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$		\geq	0.0250/0.0300

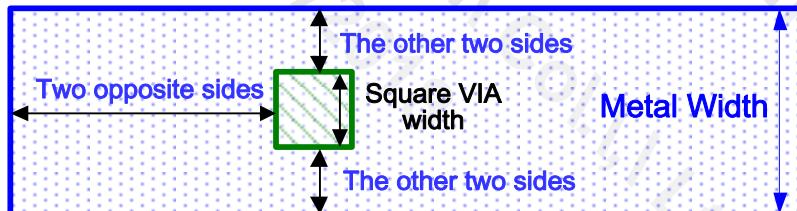
4.5.48.2 VIAxa (xa > 2) Enclosure Rule Tabulation

RuleTable.VIAxa.EN.31 (Enclosure of square VIAxa (xa > 2) [width = 0.020 μm])

Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAxa.EN.31.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIAxa.EN.31.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIAxa.EN.31.3.T	0.024 μm ≤ width < 0.028 μm	0.0300 μm	0.0020 μm	
VIAxa.EN.31.4.T	0.028 μm ≤ width < 0.040 μm	0.0300 μm	0.0020 μm	
VIAxa.EN.31.5.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIAxa.EN.31.6.T	0.060 μm ≤ width < 0.080 μm	0.0250 μm	0.0200 μm	
VIAxa.EN.31.7.T	0.080 μm ≤ width < 0.260 μm	0.0200 μm	0.0300 μm	
VIAxa.EN.31.8.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	

RuleTable.VIAxa.EN.33 (Enclosure of square VIAxa (xa > 2) [width = 0.038 μm])

Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAxa.EN.33.1.T	width < 0.060 μm	0.0590 μm	0.0010 μm	
VIAxa.EN.33.2.T	0.060 μm ≤ width < 0.080 μm	0.0500 μm	0.0110 μm	
VIAxa.EN.33.3.T	0.080 μm ≤ width < 0.100 μm	0.0430 μm	0.0210 μm	
VIAxa.EN.33.4.T	0.100 μm ≤ width < 0.120 μm	0.0430 μm	0.0310 μm	
VIAxa.EN.33.5.T	0.120 μm ≤ width < 0.260 μm	0.0400 μm	0.0400 μm	
VIAxa.EN.33.6.T	width ≥ 0.260 μm	0.0600 μm	0.0500 μm	

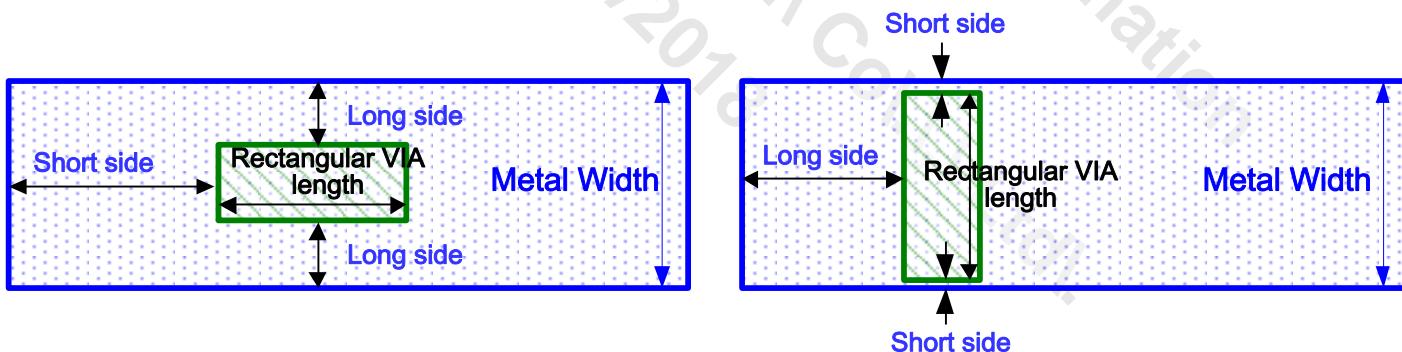


RuleTable.VIAxa.EN.32 (Enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAxa.EN.32.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIAxa.EN.32.2.T	0.022 $\mu\text{m} \leq$ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIAxa.EN.32.3.T	0.024 $\mu\text{m} \leq$ width < 0.028 μm	0.0300 μm	0.0020 μm	
VIAxa.EN.32.4.T	0.028 $\mu\text{m} \leq$ width < 0.040 μm	0.0300 μm	0.0020 μm	
VIAxa.EN.32.5.T	0.040 $\mu\text{m} \leq$ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIAxa.EN.32.6.T	0.060 $\mu\text{m} \leq$ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAxa.EN.32.7.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIAxa.EN.32.8.T	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	

RuleTable.VIAxa.EN.34 (Enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAxa.EN.34.1.T	width < 0.022 μm	0.0300 μm	0.0000 μm	
VIAxa.EN.34.2.T	0.022 $\mu\text{m} \leq$ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIAxa.EN.34.3.T	0.024 $\mu\text{m} \leq$ width < 0.028 μm	0.0300 μm	0.0020 μm	
VIAxa.EN.34.4.T	0.028 $\mu\text{m} \leq$ width < 0.040 μm	0.0300 μm	0.0040 μm	
VIAxa.EN.34.5.T	0.040 $\mu\text{m} \leq$ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIAxa.EN.34.6.T	0.060 $\mu\text{m} \leq$ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAxa.EN.34.7.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIAxa.EN.34.8.T	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	



Rule No.	Description	Label	Op.	Rule
VIAxa.EN.31.1.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] by Lower_Metal [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$		\geq	0.0300
VIAxa.EN.31.2.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] by Lower_Metal [0.022 $\mu\text{m} \leq$ width < 0.024 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIAxa.EN.31.3.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] by Lower_Metal [0.024 $\mu\text{m} \leq$ width < 0.028 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAxa.EN.31.4.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] by Lower_Metal [0.028 $\mu\text{m} \leq$ width < 0.040 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAxa.EN.31.5.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
VIAxa.EN.31.6.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.080 μm] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$		\geq	0.0250
VIAxa.EN.31.7.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] by Lower_Metal [0.080 $\mu\text{m} \leq$ width < 0.260 μm] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$		\geq	0.0200
VIAxa.EN.31.8.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.020 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
VIAxa.EN.32.1.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0300
VIAxa.EN.32.2.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] by Lower_Metal [0.022 $\mu\text{m} \leq$ width < 0.024 μm] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIAxa.EN.32.3.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] by Lower_Metal [0.024 $\mu\text{m} \leq$ width < 0.028 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAxa.EN.32.4.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] by Lower_Metal [0.028 $\mu\text{m} \leq$ width < 0.040 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAxa.EN.32.5.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] by Lower_Metal [0.040 $\mu\text{m} \leq$ width < 0.060 μm] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
VIAxa.EN.32.6.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.080 μm] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
VIAxa.EN.32.7.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
VIAxa.EN.32.8.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.050 μm] by Lower_Metal [width > 0.080 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$		\geq	0.0250/0.0300
VIAxa.EN.33.1.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.038 μm] by Lower_Metal [width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0590
VIAxa.EN.33.2.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.038 μm] by Lower_Metal [0.060 $\mu\text{m} \leq$ width < 0.080 μm] for two opposite sides with the other two sides $\geq 0.0110 \mu\text{m}$		\geq	0.0500
VIAxa.EN.33.3.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.038 μm] by Lower_Metal [0.080 $\mu\text{m} \leq$ width < 0.100 μm] for two opposite sides with the other two sides $\geq 0.0210 \mu\text{m}$		\geq	0.0430
VIAxa.EN.33.4.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.038 μm] by Lower_Metal [0.100 $\mu\text{m} \leq$ width < 0.120 μm] for two opposite sides with the other two sides $\geq 0.0310 \mu\text{m}$		\geq	0.0430

Rule No.	Description	Label	Op.	Rule
VIAxa.EN.33.5.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.038 μm] by Lower_Metal [$0.120 \mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0400 \mu\text{m}$		\geq	0.0400
VIAxa.EN.33.6.T	Enclosure of square VIAxa ($xa > 2$) [width = 0.038 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0500 \mu\text{m}$		\geq	0.0600
VIAxa.EN.34.1.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides $\geq 0.0000 \mu\text{m}$		\geq	0.0300
VIAxa.EN.34.2.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] by Lower_Metal [0.022 $\mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIAxa.EN.34.3.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] by Lower_Metal [0.024 $\mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAxa.EN.34.4.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] by Lower_Metal [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0040 \mu\text{m}$		\geq	0.0300
VIAxa.EN.34.5.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] by Lower_Metal [0.040 $\mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
VIAxa.EN.34.6.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] by Lower_Metal [0.060 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
VIAxa.EN.34.7.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] by Lower_Metal [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
VIAxa.EN.34.8.T	Short side enclosure of rectangular VIAxa ($xa > 2$) [length = 0.034 μm] by Lower_Metal [width > 0.080 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$		\geq	0.0250/0.0300

4.5.49 Mxa Layout Rules

- Minimum Pitch (MINP) 0.040 μm can only be drawn in either parallel or perpendicular to PO direction.
 - Data type 315, 316 is used for metal pitch 0.040 μm in perpendicular to core PO direction, or
 - Data type 295, 296 is used for metal pitch 0.040 μm in parallel to core PO direction
- NonMinimum Pitch (NMNP) direction is perpendicular to Minimum pitch (MINP) direction.

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Mxa = (MxaCA OR MxaCB)

DMxa = {(Mxa;298) OR (Mxa;299) OR (Mxa;318) OR (Mxa;319)}

DMxa_O = {(Mxa;292) OR (Mxa;293) OR (Mxa;312) OR (Mxa;313)}

Mxa line-end (end) definition: Mxa width ≤ 0.060 μm.

DRC checks DMxa_O as well as Mxa in this section

Rule No.	Description	Label	Op.	Rule
Mxa.W.1	Width	W1	≥	0.0200
Mxa.W.1.1	Width [MINP direction] (Except following conditions: 1. M3 [INTERACT BLK_M3, INSIDE {SRAMDMY OR BCWDMY}])	W1A	=	0.0200, 0.0220, 0.0240, 0.0400, 0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1800
Mxa.W.1.1.1	Width of M3 [MINP direction, INTERACT BCWDMY]	W1A1	=	0.0280, 0.0400
Mxa.W.1.1.2	Width of DMxa_O [MINP direction]	W1A2	=	0.0240, 0.0400, 0.1400
Mxa.W.1.2	Width [NMNP direction] (Except following conditions: 1. M3 interact BLK_M3)	W1B	=	0.0600, 0.0800, 0.1000, 0.1200, 0.1400, ≥ 0.1800
Mxa.W.2	Width of 45-degree bent Mxa (Except SEALRING_ALL)	W2	≥	0.4000
Mxa.W.3	Maximum width (Except SEALRING_ALL, LOGO)	W3	≤	0.5000
Mxa.W.4	Width of {{M3 [width = 0.028] SIZING up/down 0.010 μm in MINP direction} AND BCWDMY} in MINP direction	W4	=	0.1720
Mxa.S.1	Space	S1	≥	0.0200
Mxa.S.2	Space to Mxa [0.020 μm ≤ width ≤ 0.024 μm] in MINP direction [PRL > -0.080 μm] (Except following conditions: 1. M3 space inside {{BLK_M3 SIZING 0.0175 μm in MINP direction} SIZING 0.080 μm in NMNP direction})	SM	=	0.0200 ~ 0.0250, ≥ 0.0350
Mxa.S.2.1	Space to Mxa [width = 0.040 μm] in MINP direction [PRL > -0.040 μm] (Except following conditions: 1. Both M3 interact BCWDMY, 2. M3 space inside {{BLK_M3 SIZING 0.0175 μm in MINP direction} SIZING 0.040 μm in NMNP direction})	SM	≥	0.0350
Mxa.S.2.1.1	Space of M3 [width = 0.028 μm] in MINP direction [PRL > -0.040 μm, INTERACT BCWDMY]	SM	=	0.0200, 0.0680, 0.1160, ≥ 0.1400
Mxa.S.2.1.2	Space of M3 [width = 0.040 μm] to M3 [width = 0.028 μm] in MINP direction [PRL > -0.040 μm, INTERACT BCWDMY]	SM	=	0.0460, 0.0940, 0.1220, ≥ 0.1400
Mxa.S.2.1.3	Space of M3 [width = 0.040 μm] in MINP direction [PRL > -0.040 μm, INTERACT BCWDMY]	SM	=	0.0360, 0.1120, ≥ 0.1400
Mxa.S.2.3	Space to Mxa [width = 0.060 μm] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400

Rule No.	Description	Label	Op.	Rule
Mxa.S.2.4	Space to Mxa [width = 0.080 μm] in MINP direction [PRL > -0.040 μm] (Except following conditions: 1. M3 space inside {{BLK_M3 SIZING 0.020 μm in MINP direction} SIZING 0.040 μm in NMINP direction})	SM	\geq	0.0400
Mxa.S.2.5	Space to Mxa [width \geq 0.100 μm] in MINP direction [PRL > -0.040 μm]	SM	\geq	0.0600
Mxa.S.2.6	Space to Mxa [width \geq 0.260 μm] in MINP direction [PRL > 0.080 μm]	SM	\geq	0.1600
Mxa.S.3.1	Space to Mxa [width = 0.060 μm] in NMINP direction [PRL > -0.060 μm]	SN	\geq	0.0660
Mxa.S.3.2	Space to Mxa [width = 0.080 μm] in NMINP direction [PRL > -0.060 μm] (Except following conditions: 1. M3 space inside {{BLK_M3 SIZING 0.038 μm in MINP direction} SIZING 0.060 μm in NMINP direction})	SN	\geq	0.0760
Mxa.S.3.3	Space to Mxa [0.100 μm \leq width \leq 0.120 μm] in NMINP direction [PRL > -0.060 μm] (Except following conditions: 1. M3 space inside {{BLK_M3 SIZING 0.038 μm in MINP direction} SIZING 0.060 μm in NMINP direction})	SN	\geq	0.0760
Mxa.S.3.5	Space of Mxa [width = 0.140 μm with edge length > 0.060 μm in MINP direction] to Mxa [with edge length > 0.060 μm in MINP direction] in NMINP direction [0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1200
Mxa.S.3.6	Space to Mxa [width = 0.140 μm] in NMINP direction [PRL > 0.080 μm]	SN	\geq	0.1600
Mxa.S.3.7	Space of Mxa [width \geq 0.180 μm with edge length > 0.060 μm in MINP direction] to Mxa [with edge length > 0.060 μm in MINP direction] in NMINP direction [0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1400
Mxa.S.3.8	Space to Mxa [width \geq 0.180 μm] in NMINP direction [PRL > 0.080 μm]	SN	\geq	0.1800
Mxa.S.3.9	Space of Mxa [width \geq 0.260 μm with edge length > 0.060 μm in MINP direction] to Mxa [with edge length > 0.060 μm in MINP direction] in NMINP direction [0 μm < PRL \leq 0.080 μm]	SN	\geq	0.1800
Mxa.S.3.10	Space to Mxa [width \geq 0.260 μm] in NMINP direction [PRL > 0.080 μm]	SN	\geq	0.2600
Mxa.S.4.1	Space to Mxa line-end in NMINP direction [PRL > -0.020 μm]	S4A	\geq	0.1240
Mxa.S.4.2	Space to Mxa line-end in MINP direction [PRL > -0.020 μm]	S4B	\geq	0.1240
Mxa.S.5	Corner projected space of Mxa [-0.060 μm < PRL \leq 0 μm] (Except following conditions: 1. Corner with edge length \leq 0.024 μm on both sides)	S5	\geq	0.0600
Mxa.S.12	Space to 45-degree bent Mxa [PRL > 0 μm] (Except SEALRING_ALL)	S12	\geq	0.4000
Mxa.S.12.1	Space to 45-degree bent Mxa (Except SEALRING_ALL)	S12A	\geq	0.1400
Mxa.S.13.1	Space to VIAxa-1 or VIAxa or VIAYa [maximum delta V > 0.96V]	S13	\geq	0.0550
Mxa.S.13.2	Space to VIAxa-1 or VIAxa or VIAYa [maximum delta V > 1.32V] (1.2V + 10%)	S13	\geq	0.0640
Mxa.S.13.3	Space to VIAxa-1 or VIAxa or VIAYa [maximum delta V > 1.65V] (1.5V + 10%)	S13	\geq	0.0700
Mxa.S.13.4	Space to VIAxa-1 or VIAxa or VIAYa [maximum delta V > 1.98V] (1.8V + 10%)	S13	\geq	0.0820
Mxa.S.13.5	Space to VIAxa-1 or VIAxa or VIAYa [maximum delta V > 2.75V] (2.5V + 10%)	S13	\geq	0.0870
Mxa.S.18	Space to Mxa [maximum delta V > 0.96V]	S18	\geq	0.0520
Mxa.S.18.1	Space to Mxa [maximum delta V > 1.32V] (1.2V + 10%)	S18	\geq	0.0550
Mxa.S.18.2	Space to Mxa [maximum delta V > 1.65V] (1.5V + 10%)	S18	\geq	0.0610
Mxa.S.18.3	Space to Mxa [maximum delta V > 1.98V] (1.8V + 10%)	S18	\geq	0.0690
Mxa.S.18.4	Space to Mxa [maximum delta V > 2.75V] (2.5V + 10%)	S18	\geq	0.0790
Mxa.S.18.6	Corner projected space of Mxa [maximum delta V > 0.96V, -0.060 μm < PRL \leq 0 μm]	S18F	\geq	0.1000

Rule No.	Description	Label	Op.	Rule
Mxa.S.18.7	Corner projected space of Mxa [maximum delta V > 1.98V, -0.100 $\mu\text{m} < \text{PRL} \leq 0 \mu\text{m}$]	S18G	\geq	0.1000
Mxa.EN.0	1. Enclosure of square Lower_VIA [width = 0.020 μm] is defined by RuleTable.Mxa.EN.31 in the subsection 2. Enclosure of square Lower_VIA [width = 0.038 μm] is defined by RuleTable.Mxa.EN.33 in the subsection 3. Enclosure of rectangular Lower_VIA [length = 0.050 μm] is defined by RuleTable.Mxa.EN.32 in the subsection 4. Enclosure of rectangular Lower_VIA [length = 0.034 μm] is defined by RuleTable.Mxa.EN.34 in the subsection			
Mxa.EN.1.2.1	Enclosure of square VIAx-1 by Mxa [width = 0.028 μm , INTERACT BCWDMY] for two opposite sides with the other two sides $\geq 0.004 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})	EN1	\geq	0.0300
Mxa.EN.6.2.1	Short side enclosure of rectangular VIAx-1 by Mxa [width = 0.028 μm , INTERACT BCWDMY] with the other two long side enclosure $\geq 0.004 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})	EN6	\geq	0.0300
Mxa.EN.6.4	Short side enclosure of rectangular VIAx-1 by Mxa edge [length = 0.080 μm , Mxa width = 0.080 μm] (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})	EN6D	\geq	0.0250
Mxa.EN.31.4	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0300
Mxa.EN.31.5	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.040 $\mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0300
Mxa.EN.31.7	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.080 $\mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$ (Except following conditions: 1. VIA2 inside BLK_M3)		\geq	0.0200
Mxa.EN.32.4	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0300
Mxa.EN.32.8	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [0.080 $\mu\text{m} < \text{width} < 0.260 \mu\text{m}$] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$ (Except following conditions: 1. VIA2 inside {BLK_M3 AND BLK_M2})		\geq	0.0250/0.0300
Mxa.L.1	At least one edge length of 45-degree bent Mxa (minimum edge length)	L1	\geq	0.9100
Mxa.L.2	Edge length with adjacent edge [length < 0.090 μm]	L2	\geq	0.0800
Mxa.A.1	Area of Mxa	A1	\geq	0.00416
Mxa.DN.1.1	Minimum All_metal density in window 40 $\mu\text{m} \times 40 \mu\text{m}$, stepping 20 μm (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	12.5%

Rule No.	Description	Label	Op.	Rule
Mxa.DN.1.2	Minimum All_metal density in window 40 μm x 40 μm , stepping 20 μm [3 μm x 3 μm empty area exists in the window] (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	25%
Mxa.DN.2	Maximum All_metal density in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. {{Mxa;292 OR Mxa;312} OR {Mxa;293 OR Mxa;313}} OR {{Mxa;298 OR Mxa;318} OR {Mxa;299 OR Mxa;319}}, 2. M3 inside BLK_WB)		\leq	65%
Mxa.DN.2.3	Maximum All_metal density in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	75%
Mxa.DN.3	The All_metal density difference between any two neighboring checking windows including DMnEXCL [window 40 μm x 40 μm , stepping 40 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\leq	50%
Mxa.DN.3.3	Maximum density difference between {{MxaCA OR {Mxa;292 OR Mxa;312}} OR {{Mxa;298 OR Mxa;318}}} and {{MxaCB OR {Mxa;293 OR Mxa;313}} OR {{Mxa;299 OR Mxa;319}}} across full chip (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	10%
Mxa.DN.3.6	Maximum local density difference between {{MxaCA OR {Mxa;292 OR Mxa;312}} OR {{Mxa;298 OR Mxa;318}}} and {{MxaCB OR {Mxa;293 OR Mxa;313}} OR {{Mxa;299 OR Mxa;319}}} in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL)		\leq	40%
Mxa.DN.3.7	Minimum local density of {{MxaCA OR {Mxa;292 OR Mxa;312}} OR {{Mxa;298 OR Mxa;318}}} in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		$>$	4.5%
Mxa.DN.3.8	Minimum local density of {{MxaCB OR {Mxa;293 OR Mxa;313}} OR {{Mxa;299 OR Mxa;319}}} in window 40 μm x 40 μm , stepping 20 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		$>$	4.5%
Mxa.DN.6.1	All_metal density [window 9 μm x 9 μm , stepping 4.5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	1%
Mxa.DN.7	It is not allowed to have local density < 5% of all 3 consecutive metal (Mxa, Mxa+1, and Mxa+2) over any 27 μm x 27 μm (stepping 13.5 μm), i.e. it is allowed for either one of Mxa, Mxa+1, or Mxa+2 to have a local density \geq 5% (The metal layers include Mxa/Mxa+1/Mxa+2 and dummy metals for ELK film) (Except ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc, 2. TCDDMY_Mn (assume 30% pattern density INSIDE TCDDMY_Mn))			

Rule No.	Description	Label	Op.	Rule
Mxa.DN.9	<p>Minimum Line edge Density (LeD) in window 20 μm x 20 μm, stepping 10 μm</p> <p>Definition of "Line edge Density": $\left(\left(\text{All_metal area} - (\text{All_metal SIZING} - 0.001 \mu\text{m area}) \right) \times 1000 \right) / \text{Checking window}$</p> <p>(Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window has any one metal {MxaCA OR MxaCB} width < 0.060 μm</p>		≥	8.5
Mxa.DN.9.1	<p>Minimum Line edge Density (LeD) in window 20 μm x 20 μm, stepping 10 μm</p> <p>Definition of "Line edge Density": $\left(\left(\text{All_metal area} - (\text{All_metal SIZING} - 0.001 \mu\text{m area}) \right) \times 1000 \right) / \text{Checking window}$</p> <p>(Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window has any one metal {MxaCA OR MxaCB} width < 0.120 μm</p>		≥	3
Mxa.R.1	Mxa must be a rectangle (Except SEALRING_ALL, LOGO)			
Mxa.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
Mxa.R.10	Mxa (M3) overlap MetalFuse_B1 (156;8) is not allowed			
Mxa.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of Mxa space to Mxa or VIAx-1 or VIAx or VIAy is < 0.360 μm			

Rule No.	Description	Label	Op.	Rule
Mxa.R.12	Datatype (295 or 296 or 292 or 293 or 298 or 299) and (315 or 316 or 312 or 313 or 318 or 319) exist on the same metal layer at the same time is not allowed			
Mxa.R.12.1	Same datatype (295 or 296 or 292 or 293 or 298 or 299) or (315 or 316 or 312 or 313 or 318 or 319) in both Mxa and Mxa-1 at the same time is not allowed			
Mxa.R.12.2	Consecutive Mx datatype (255 or 256 or 252 or 253 or 258 or 259) and Mxa datatype (295 or 296 or 292 or 293 or 298 or 299) exist at the same time is not allowed; Consecutive Mx datatype (275 or 276 or 272 or 273 or 278 or 279) and Mxa datatype (315 or 316 or 312 or 313 or 318 or 319) exist at the same time is not allowed			
Mxa.R.14	{}{Mxa_Empty_Area SIZING 0.330 μm } INTERACT Mxa island} is not allowed Definitions: 1. Mxa_Empty_Area: Area of {{CHIP NOT {{TCDDMY_Mn OR ICOVL_SINGLE} OR {{Mxa OR DMxa} OR DMxa_O}}} SIZING down/up 0.380 μm } \geq 1.96 μm^2 2. Mxa island: Area of (Mxa with only one square VIAxa-1 [width x length = 0.020 μm x 0.020 μm]) \leq 0.010 μm^2			
Mxa.R.15	{Mxa_Empty_Area SIZING 0.100 μm in MINP direction} interact VIAxa-1 [INTERACT Mxa [width < 0.060 μm]] is not allowed Definitions of Mxa_Empty_Area: {{{CHIP NOT {{Mxa OR DMxa} OR DMxa_O}}} SIZING down/up 0.380 μm in MINP direction} SIZING down/up 0.400 μm in NMINP direction} can enclose a 0.760 μm x 0.800 μm (MINP x NMINP) orthogonal rectangle			
Mxa.R.17	DMxa is a must in chip level.			
Mxa.R.18	Mxa [width \leq 0.022 μm] interact VIAxa-1_array_region is not allowed (Except following conditions: 1. M3 interact BLK_M3) VIAxa-1_array_region definition: (1) VIAxa-1 array is \geq 2x2 VIAxa-1 array, and (2) Two VIAxa-1 space $<$ 0.140 μm in NMINP direction [PRL > 0 μm], and both of the VIAxa-1 space = 0.0505~0.0760 μm in MINP direction [PRL > -0.020 μm], and (3) Form one region from one of each VIAxa-1 corner (C1/C2/C3/C4), and the space of the corners is the minimum in MINP and NMINP direction.			
Mxa.R.18.1	Mxa [width \leq 0.022 μm] interact VIAxa-1_array_region is not allowed (Except following conditions: 1. M3 interact BLK_M3) VIAxa-1_array_region definition: (1) VIAxa-1 array is \geq 2x2 VIAxa-1 array, and (2) Two VIAxa-1 space $<$ 0.100 μm in NMINP direction [PRL > 0 μm], and both of the VIAxa-1 space = 0.0505~0.0760 μm in MINP direction [PRL > -0.0205 μm], and (3) Form one region from one of each VIAxa-1 corner (C1/C2/C3/C4), and the space of the corners is the minimum in MINP and NMINP direction.			

Rule No.	Description	Label	Op.	Rule
Mxa.R.18.2	<p>Space of Mxa [width \leq 0.022 μm] to Checked_VIAxa-1_Edge in MINP direction [PRL > -0.0205 μm] $<$ 0.060 μm is not allowed (Except following conditions: 1. M3 interact BLK_M3)</p> <p>Definition of Checked_VIAxa-1_Group: {VIAxa-1 [space to VIAxa-1 $<$ 0.060 μm in NMNP direction, PRL > 0 μm]} Definition of Checked_VIAxa-1_Edge: Checked_VIAxa-1_Group NMNP edge[space to VIAxa-1 = 0.060~0.0975 μm in MINP direction, PRL > -0.020 μm]</p>			
Mxa.R.21	<p>Both side space of Small_MxaCA_Group to MxaCA [width \geq 0.060 μm] in MINP direction \leq 0.220 μm is not allowed</p> <p>Definition of Small_MxaCA_Group: {{Small_MxaCA SIZING up/down 0.033 μm in MINP direction} SIZING down/up 0.0895 μm in MINP direction} [length $<$ 0.140 μm in NMNP direction] {length = 0.180~0.490 μm in MINP direction}]</p> <p>Definition of Small_MxaCA: MxaCA [width \leq 0.024 μm in MINP direction, length \leq 0.300 μm in NMNP direction]</p>			
Mxa.CS.0	DRC checks same color space of {MxaCA OR DMxa_DO1} and {MxaCB OR DMxa_DO2}, respectively in Mxa.CS.x rules			
Mxa.CS.0.1	Space to Mxa [width \geq 0.020 μm] in MINP direction [same color, PRL > -0.100 μm]	SM	\geq	0.0600
Mxa.CS.0.2	Space to Mxa [width \geq 0.060 μm] in NMNP direction [same color, PRL > -0.060 μm]	SN	\geq	0.1160
Mxa.CS.1.1	Space of Mxa [width = 0.020 μm] to Mxa [width $<$ 0.040 μm] in MINP direction [same color, PRL > -0.124 μm] DRC checks same color space of MxaCA and MxaCB	SM	=	0.0600, 0.0620, 0.0640, \geq 0.1400
Mxa.CS.1.1.1.1	Space of Mxa [width = 0.020 μm] to Mxa [width = 0.040 μm] in MINP direction [same color, PRL > -0.124 μm] DRC checks same color space of MxaCA and MxaCB	SM	=	0.0900, \geq 0.1400
Mxa.CS.1.1.1.3	Space of Mxa [width = 0.020 μm] to Mxa [width $>$ 0.060 μm] in MINP direction [same color, PRL > -0.124 μm] DRC checks same color space of MxaCA and MxaCB	SM	=	0.0600, 0.0620, 0.0640, \geq 0.1400
Mxa.CS.1.1.2	Space of Mxa [width = 0.022 μm] to Mxa [width $<$ 0.040 μm , or width $>$ 0.060 μm] in MINP direction [same color, PRL > -0.124 μm] DRC checks same color space of MxaCA and MxaCB	SM	=	0.0600, 0.0620, 0.0640, \geq 0.1400
Mxa.CS.1.1.2.1	Space of Mxa [width = 0.022 μm] to Mxa [width = 0.040 μm] in MINP direction [same color, PRL > -0.124 μm] DRC checks same color space of MxaCA and MxaCB	SM	=	0.0950, \geq 0.1400
Mxa.CS.1.1.3	Space of Mxa [width = 0.024 μm] to Mxa [width $<$ 0.040 μm , or width $>$ 0.060 μm] in MINP direction [same color, PRL > -0.124 μm] DRC checks same color space of MxaCA and MxaCB (Except following conditions: 1. Both M3 interact BLK_M3)	SM	=	0.0600, 0.0620, 0.0640, \geq 0.1400
Mxa.CS.1.1.3.1	Space of Mxa [width = 0.024 μm] to Mxa [width = 0.040 μm] in MINP direction [same color, PRL > -0.124 μm] DRC checks same color space of MxaCA and MxaCB	SM	=	0.1000, \geq 0.1400
Mxa.CS.1.1.3.2	Space of M3 [width = 0.028 μm] in MINP direction [same color, PRL > -0.124 μm , INTERACT BCWDMY]	SM	=	0.0680, \geq 0.1400
Mxa.CS.1.1.4	Space to Mxa [width = 0.040 μm] in MINP direction [same color, PRL > -0.060 μm] (Except following conditions: 1. Both M3 interact BCWDMY, 2. Both M3 interact BLK_M3)	SM	=	0.0900, 0.0950, 0.1000, 0.1100, 0.1120, \geq 0.1200
Mxa.CS.1.1.4.1	Space of M3 [width = 0.040 μm] in MINP direction [same color, PRL > -0.060 μm , INTERACT BCWDMY]	SM	=	0.1120, \geq 0.1200

Rule No.	Description	Label	Op.	Rule
Mxa.CS.1.1.4.2	Space of M3 [width = 0.040 μm] to M3 [width = 0.028 μm] in MINP direction [same color, PRL > -0.060 μm, INTERACT BCWDMY]	SM	=	0.0940, 0.1220, ≥ 0.1400
Mxa.CS.1.1.6	Forbidden space of Mxa [0.020 μm ≤ width ≤ 0.024 μm] in MINP direction [same color, PRL > 0 μm] (Except following conditions: 1. Mxa_Projection_Region fully projected by another Mxa [width > 0.024 μm]) Definition of Mxa_Projection_Region: Enclosed region formed by Mxa [0.020 μm ≤ width ≤ 0.024 μm], PRL > 0 μm	SM	=	0.1870 ~ 0.2190, 0.2570 ~ 0.2990, 0.3370 ~ 0.3790
Mxa.CS.1.1.7	Space of DMxa_O [width = 0.024 μm] to Mxa in MINP direction [same color, PRL > -0.124 μm]	SM	=	0.0600, 0.0620, 0.0640, 0.0660, 0.0680, 0.0700, ≥ 0.1000
Mxa.CS.1.1.8	Space of DMxa_O [width = 0.040 μm] to Mxa in MINP direction [same color, PRL > -0.124 μm]	SM	\geq	0.1000
Mxa.CS.1.2	Space to Mxa [width = 0.060 μm] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1000
Mxa.CS.1.2.1	Space of Mxa [width = 0.060 μm] to Mxa [width = 0.020/0.022/0.024 μm] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1400
Mxa.CS.1.3	Space of Mxa [0.080 μm ≤ width ≤ 0.120 μm with edge length > 0.060 μm in NMINP direction] to Mxa [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1200
Mxa.CS.1.6	Space of Mxa [width = 0.140 μm with edge length > 0.060 μm in NMINP direction] to Mxa [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1300
Mxa.CS.1.7	Space to Mxa [width = 0.140 μm] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.1600
Mxa.CS.1.8	Space of Mxa [width ≥ 0.180 μm with edge length > 0.060 μm in NMINP direction] to Mxa [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, PRL > -0.060 μm]	SM	\geq	0.1400
Mxa.CS.1.9	Space to Mxa [width ≥ 0.180 μm] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.1800
Mxa.CS.1.10	Space of Mxa [width ≥ 0.260 μm with edge length > 0.060 μm in NMINP direction] to Mxa [with edge length > 0.060 μm in NMINP direction] in MINP direction [same color, 0 μm < PRL ≤ 0.080 μm]	SM	\geq	0.1800
Mxa.CS.1.11	Space to Mxa [width ≥ 0.260 μm] in MINP direction [same color, PRL > 0.080 μm]	SM	\geq	0.2600
Mxa.CS.3.2	Space to Mxa [width = 0.060 μm] in NMINP direction [same color, PRL > -0.060 μm]	SN	\geq	0.1250
Mxa.CS.3.3	Space of Mxa [width = 0.080 μm with edge length > 0.060 μm in MINP direction] to Mxa [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, -0.060 μm < PRL ≤ 0.060 μm]	SN	\geq	0.1240
Mxa.CS.3.4	Space to Mxa [width = 0.080 μm] in NMINP direction [same color, PRL > 0.060 μm]	SN	\geq	0.1300
Mxa.CS.3.5	Space of Mxa [0.100 μm ≤ width ≤ 0.120 μm with edge length > 0.060 μm in MINP direction] to Mxa [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, -0.060 μm < PRL ≤ 0.060 μm]	SN	\geq	0.1240
Mxa.CS.3.6	Space to Mxa [0.100 μm ≤ width ≤ 0.120 μm] in NMINP direction [same color, PRL > 0.060 μm]	SN	\geq	0.1400
Mxa.CS.3.9	Space of Mxa [width = 0.140 μm with edge length > 0.060 μm in MINP direction] to Mxa [with edge length > 0.060 μm in MINP direction] in NMINP direction [same color, 0 μm < PRL ≤ 0.080 μm]	SN	\geq	0.1300
Mxa.CS.3.10	Space to Mxa [width = 0.140 μm] in NMINP direction [same color, PRL > 0.080 μm]	SN	\geq	0.1600

Rule No.	Description	Label	Op.	Rule
Mxa.CS.3.11	Space of Mxa [width \geq 0.180 μm with edge length $>$ 0.060 μm in MINP direction] to Mxa [with edge length $>$ 0.060 μm in MINP direction] in NMINP direction [same color, 0 μm $<$ PRL \leq 0.080 μm]	SN	\geq	0.1400
Mxa.CS.3.12	Space to Mxa [width \geq 0.180 μm] in NMINP direction [same color, PRL $>$ 0.080 μm]	SN	\geq	0.1800
Mxa.CS.3.13	Space of Mxa [width \geq 0.260 μm with edge length $>$ 0.060 μm in MINP direction] to Mxa [with edge length $>$ 0.060 μm in MINP direction] in NMINP direction [same color, 0 μm $<$ PRL \leq 0.080 μm]	SN	\geq	0.1800
Mxa.CS.3.14	Space to Mxa [width \geq 0.260 μm] in NMINP direction [same color, PRL $>$ 0.080 μm]	SN	\geq	0.2600
Mxa.CS.5.1	Mxa end-end/end-run space [PRL $>$ -0.060 μm] in NMINP direction	CS5A	\geq	0.1240
Mxa.CS.5.3	Mxa end-end/end-run space [PRL $>$ -0.060 μm] in MINP direction	CS5C	\geq	0.1240
Mxa.CS.6.1	Corner projected space of Mxa [same color, -0.100 μm $<$ PRL \leq 0 μm] (Except following conditions: 1. Corner with edge length \leq 0.024 μm on both sides)	CS6A	\geq	0.1000
Mxa.CS.7	Long side of MxaCA [width \leq 0.060 μm] space to MxaCB [projection length difference on MxaCA $<$ 0.060 μm]	CS7	$>$	0.0360
Mxa.CS.8	More than one {MxaCA OR DMxa_DO1} interact MxaCB_Corner_Projected_Region from the same short side is not allowed MxaCB_Corner_Projected_Region definition: The corner projected space of {MxaCB OR DMxa_DO2} short side edge [width \leq 0.060 μm] $<$ 0.060 μm in NMINP direction [-0.026 μm $<$ PRL $<$ 0 μm]			
Mxa.CS.10	{MxaCA OR DMxa_DO1} interact {MxaCB OR DMxa_DO2} is not allowed			
Mxa.CS.14	Forbidden space of Mxa_Critical_Group to Mxa [width \leq 0.024 μm] in MINP direction [PRL $>$ 0 μm] (Except following conditions: 1. Mxa_Critical_Groups_Projection_Region fully projected by another Mxa [width $>$ 0.024 μm]) Definition of Mxa_Critical_Group: {(Mxa [width \leq 0.024 μm] SIZING up/down 0.032 μm in MINP direction) SIZING down/up 0.0495 μm in NMINP direction} [0.100 μm \leq width in MINP direction \leq 0.630 μm , width in NMINP direction \geq 0.100 μm] Definition of Mxa_Critical_Groups_Projection_Region: Enclosed region formed by Mxa_Critical_Groups, PRL $>$ 0 μm	CS14	=	0.0650~0.1390, 0.1530~0.2190, 0.2410~0.2990
Mxa.CS.15	Forbidden space of Mxa in MINP direction [PRL $>$ 0 μm] [one side is Mxa [width = 0.040 μm] the other side is Mxa [width = 0.020 μm]]	CS15	=	0.2510~0.2940, 0.3410~0.3590
Mxa.CS.15.1	Forbidden space of Mxa in MINP direction [PRL $>$ 0 μm] [one side is Mxa [width = 0.040 μm] the other side is Mxa [width = 0.022/0.024 μm]]	CS15A	=	0.2510~0.2620, 0.2640~0.2750, 0.2780~0.2940
Mxa.CS.16	Forbidden space of Mxa in MINP direction [PRL $>$ 0 μm] [one side is Mxa [width = 0.060 μm] the other side is Mxa [width = 0.020 μm]]	CS16	=	0.2510~0.2940, 0.3410~0.3590
Mxa.CS.16.1	Forbidden space of Mxa in MINP direction [PRL $>$ 0 μm] [one side is Mxa [width = 0.060 μm] the other side is Mxa [width = 0.022/0.024 μm]]	CS16A	=	0.2450~0.2520, 0.2540~0.2650, 0.2680~0.2940
Mxa.CS.17	Forbidden space of Mxa in MINP direction [PRL $>$ 0 μm] [one side is Mxa [width = 0.080 μm] the other side is Mxa [width \leq 0.024 μm]]	CS17	=	0.2510~0.2550, 0.2570~0.2940
Mxa.CS.18	Forbidden space of Mxa in MINP direction [PRL $>$ 0 μm] [one side is Mxa [0.100 μm \leq width $<$ 0.140 μm] the other side is Mxa [width \leq 0.024 μm]]	CS18	=	0.2510~0.2940
Mxa.CS.19	Forbidden space of Mxa in MINP direction [PRL $>$ 0.060 μm] [one side is Mxa [width \geq 0.140 μm] the other side is Mxa [width \leq 0.024 μm]]	CS19	=	0.2510~0.2940

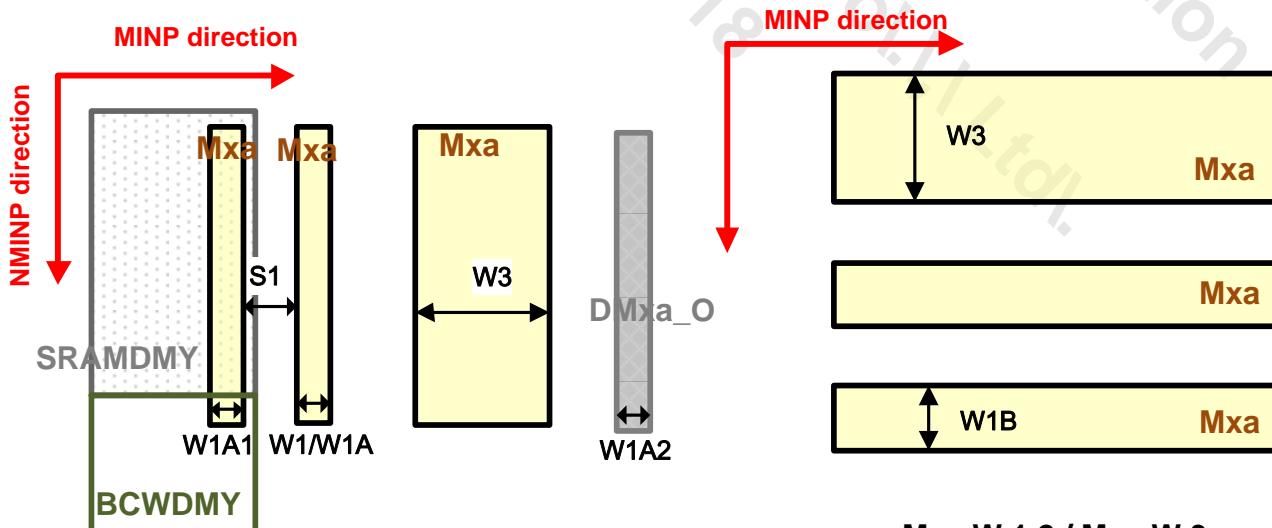
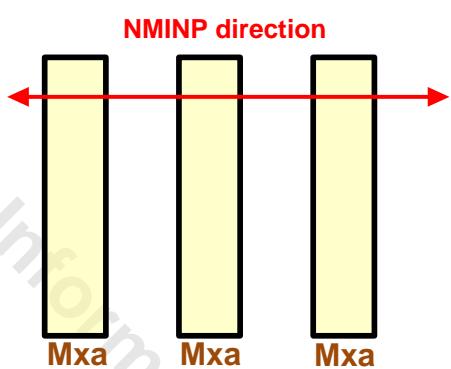
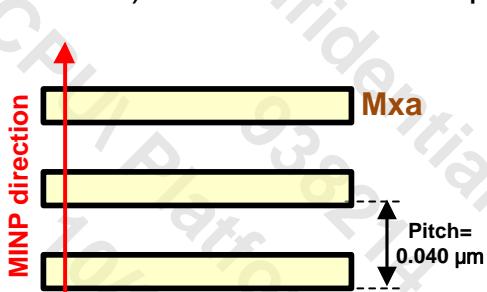
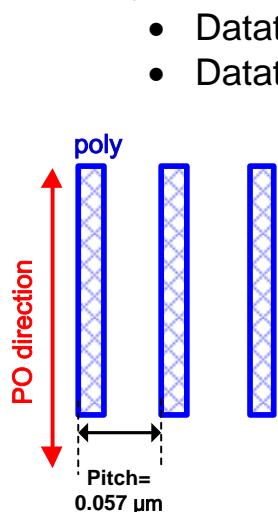
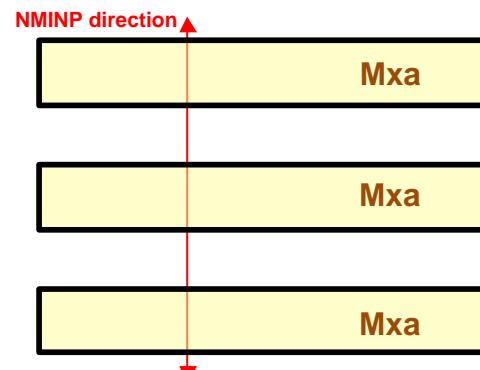
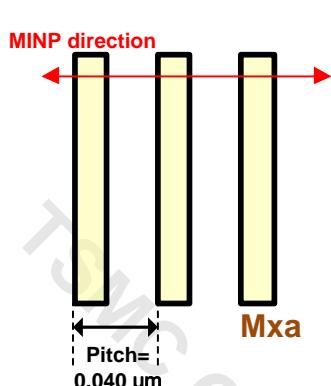
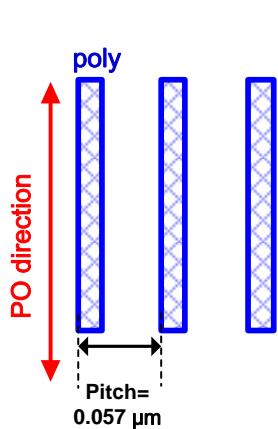
Table Notes:

- To meet the metal process window, filling the dummy metal globally and uniformly by tsmc utility is needed even if the originally drawn Mxa has already met the density rules. For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, filling manually and evenly is still needed.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations during placement. Unexpected violations may occur during the IP/macro placement due to the environment, even if the IP/macro already passed the high density rule check. Therefore, customers need to carefully design the dimension of the width/space for wide metal (e.g., power/ground bus), under the proper high density limit.
- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

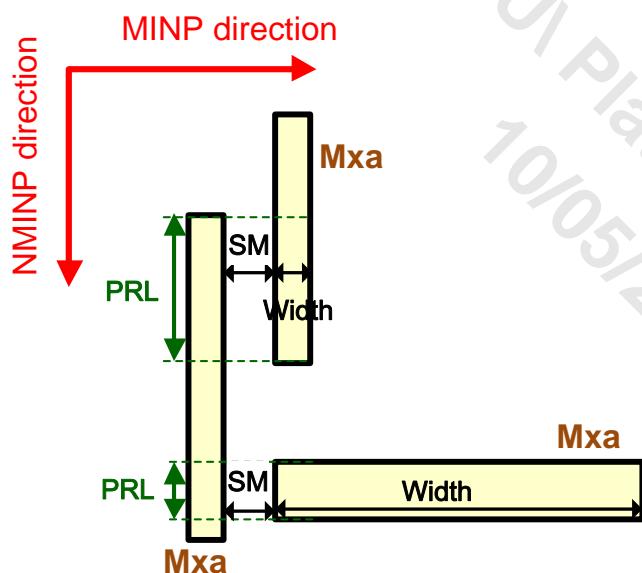
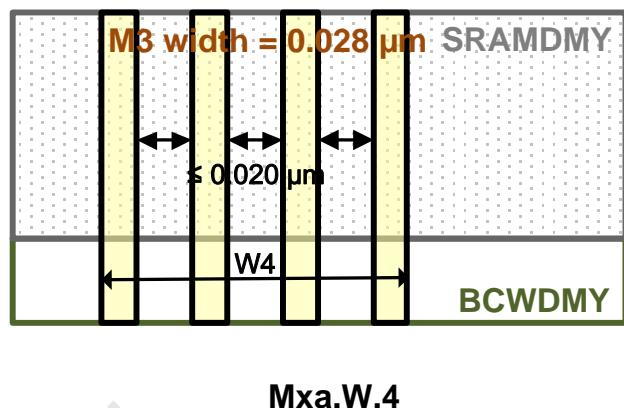
TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

Mxa

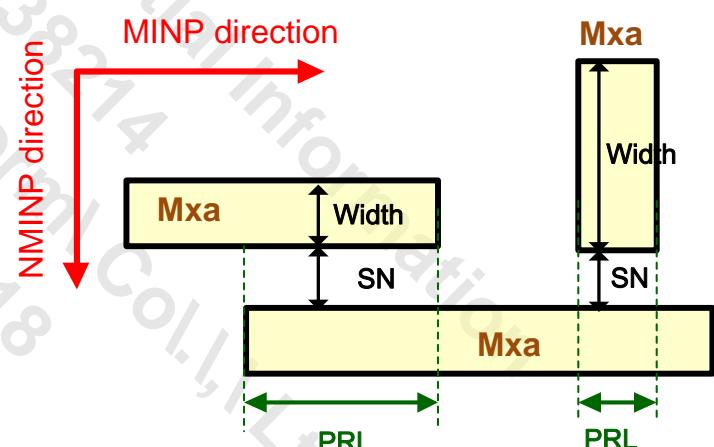
- Datatype (315 or 316) MINP direction is parallel to PO direction
- Datatype (315 or 316) NMINP direction is perpendicular to PO direction



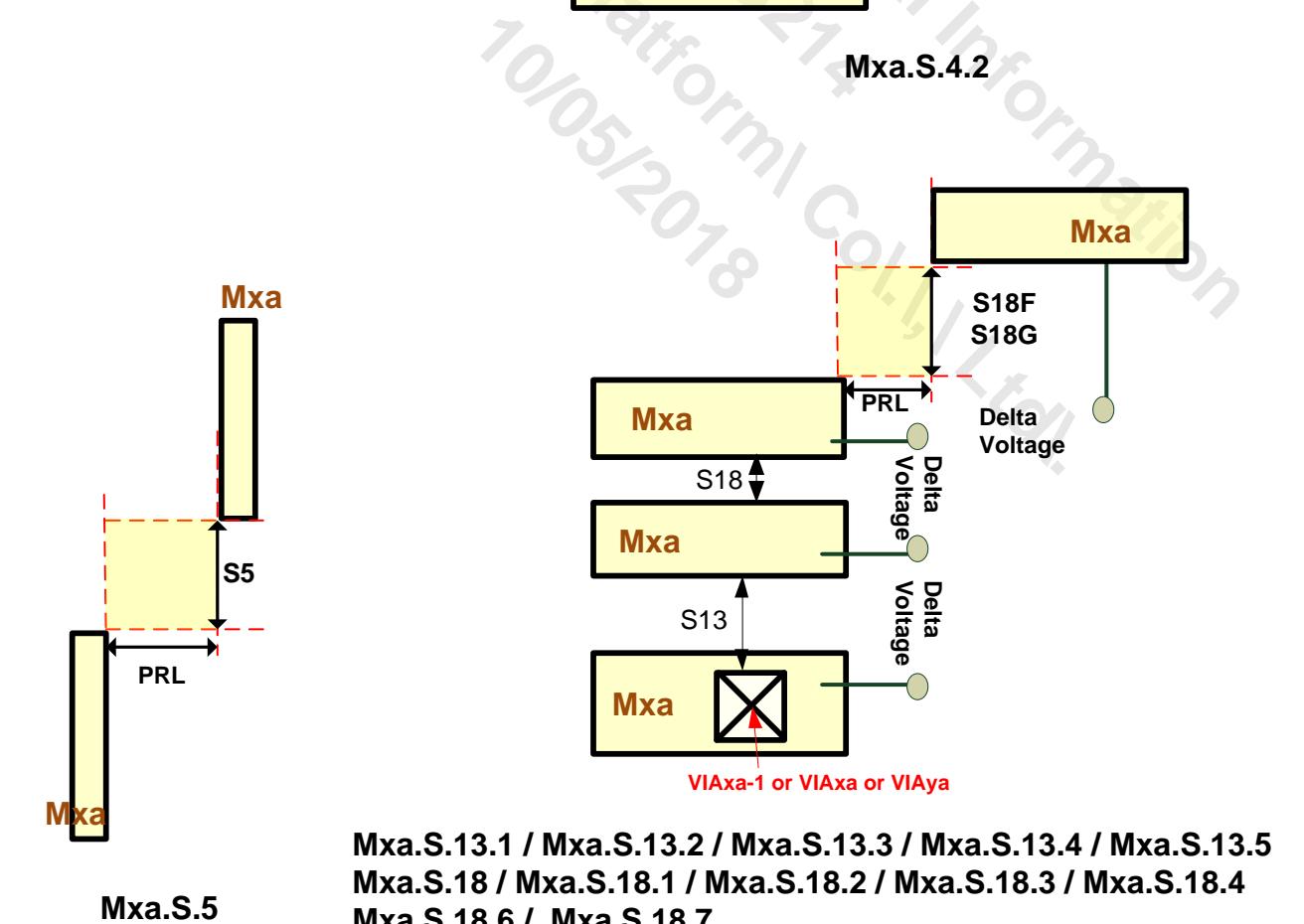
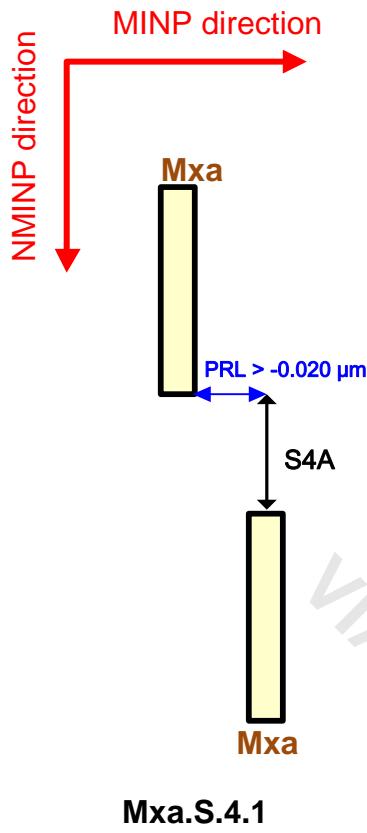
**Mxa.W.1 / Mxa.W.1.1 Mxa.W.1.1.1 /
Mxa.W.1.1.2 / Mxa.W.3 / Mxa.S.1**



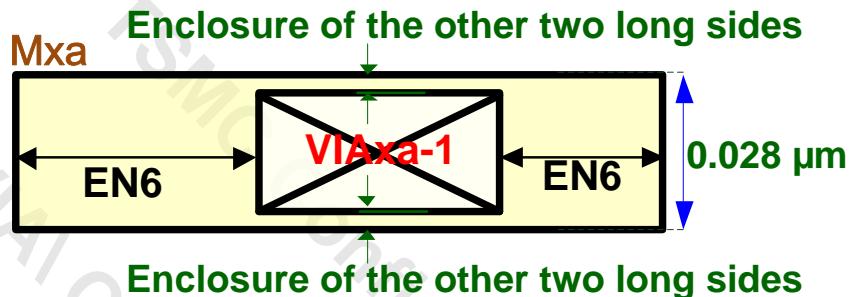
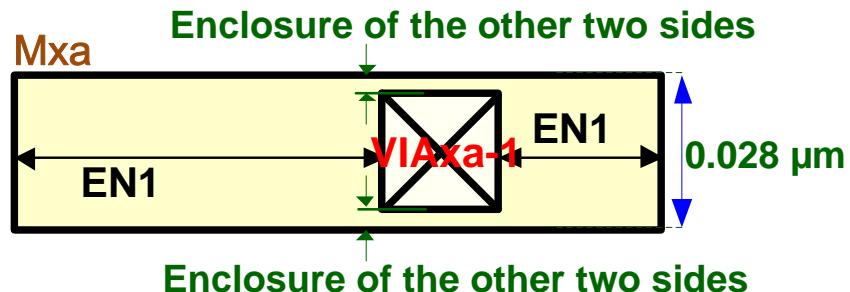
Mxa.S.2 / Mxa.S.2.1 / Mxa.S.2.1.1 /
Mxa.S.2.1.2 / Mxa.S.2.1.3 / Mxa.S.2.3 /
Mxa.S.2.4 / Mxa.S.2.5 / Mxa.S.2.6



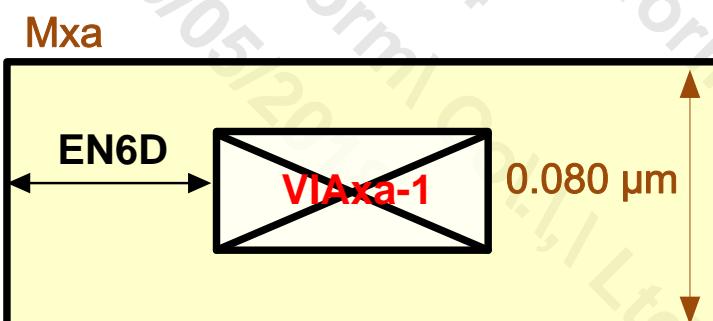
Mxa.S.3.1 / Mxa.S.3.2 / Mxa.S.3.3 /
Mxa.S.3.4 / Mxa.S.3.5 / Mxa.S.3.6 /
Mxa.S.3.7 / Mxa.S.3.8 / Mxa.S.3.9 /
Mxa.S.3.10



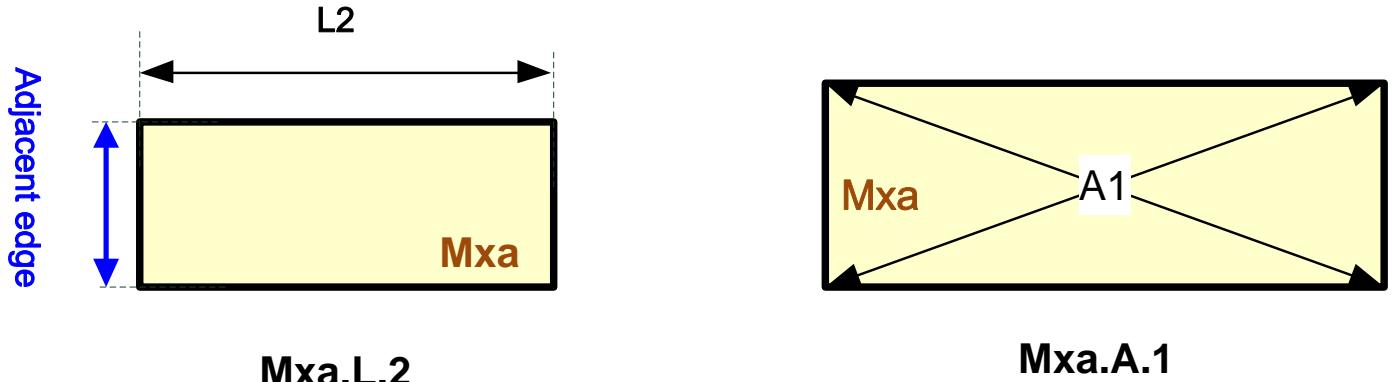
BCWDMY

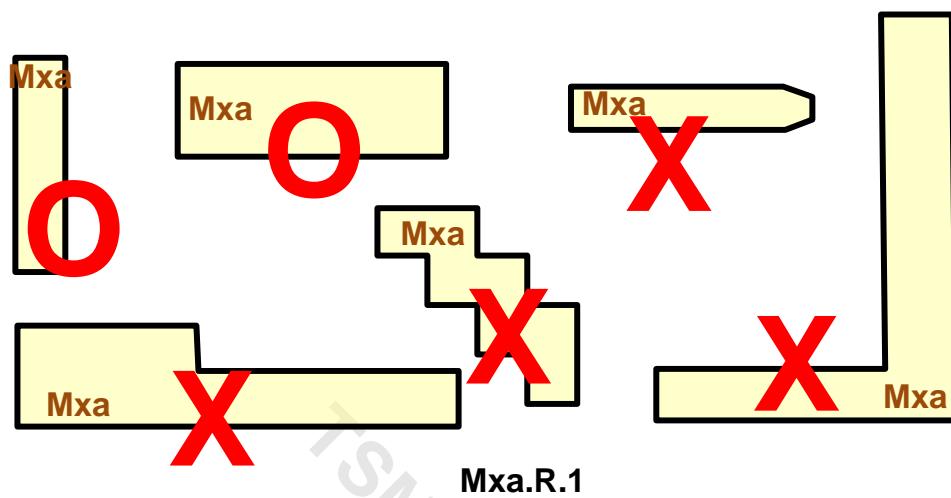


Mxa.EN.1.2.1 / Mxa.EN.6.2.1

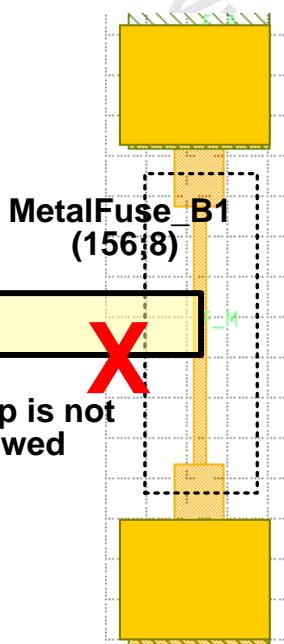


Mxa.EN.6.4



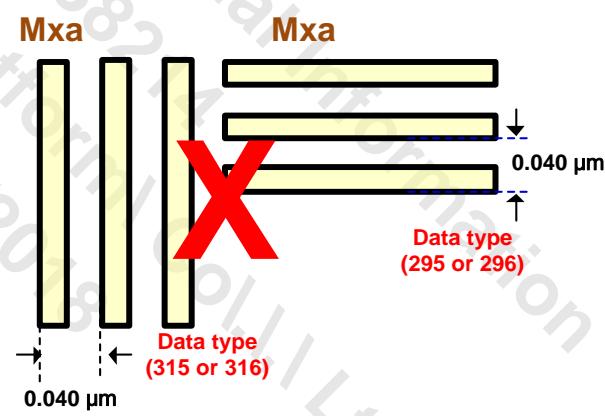


Mxa.R.1

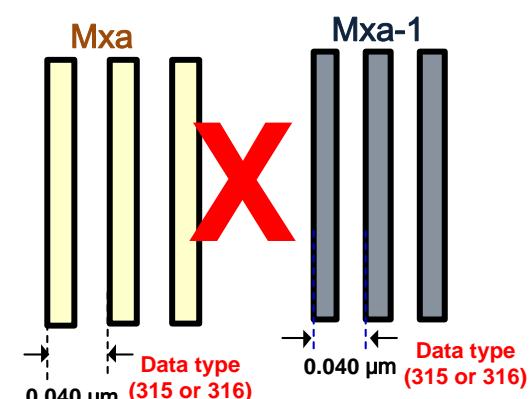
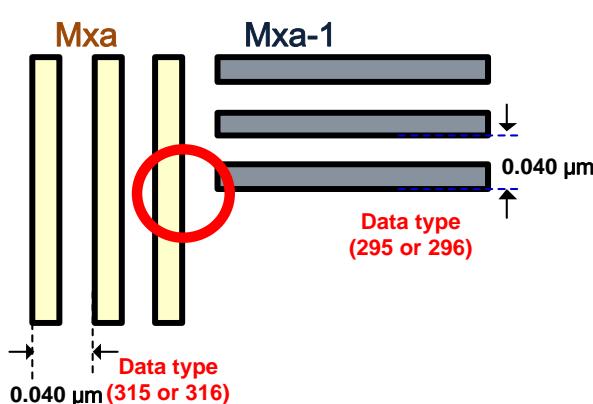


Overlap is not allowed

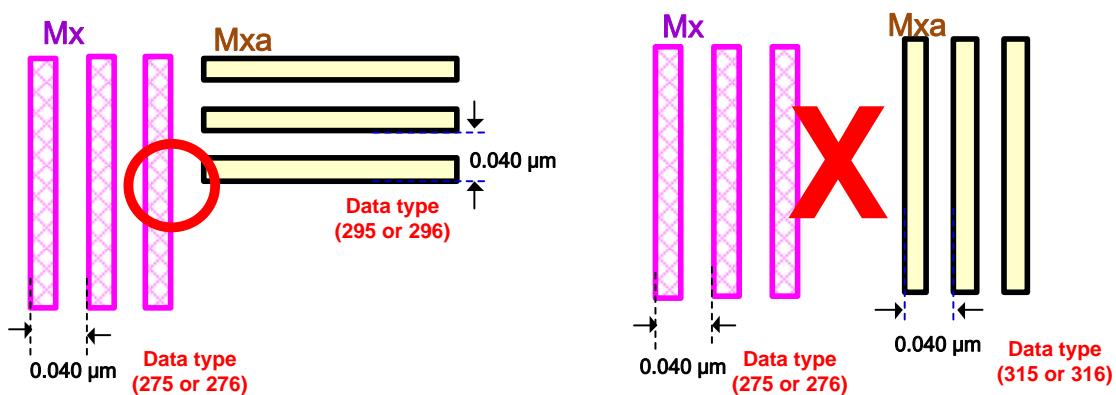
Mxa.R.10



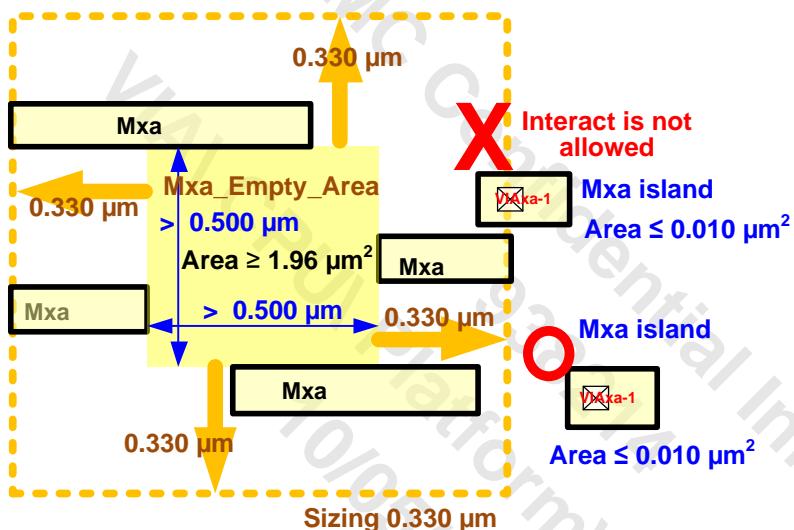
Mxa.R.12



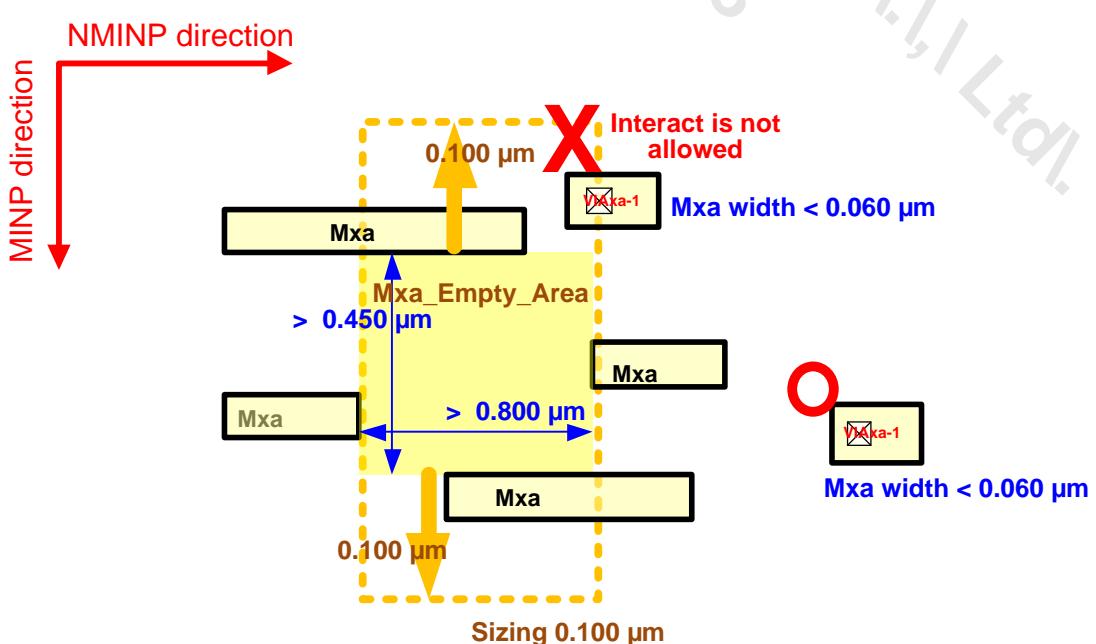
Mxa.R.12.1



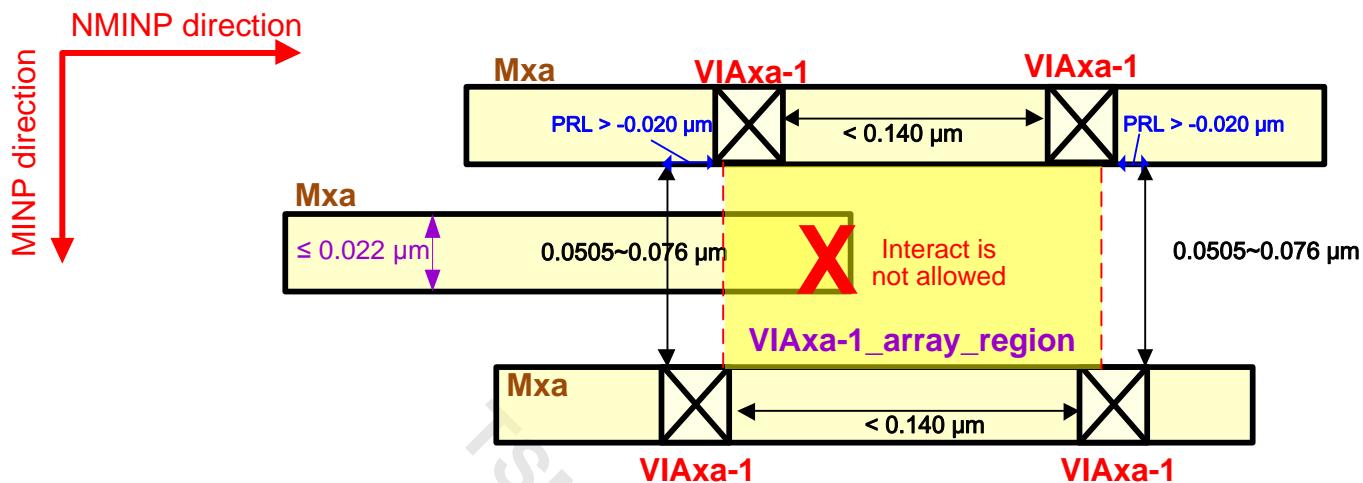
Mxa.R.12.2



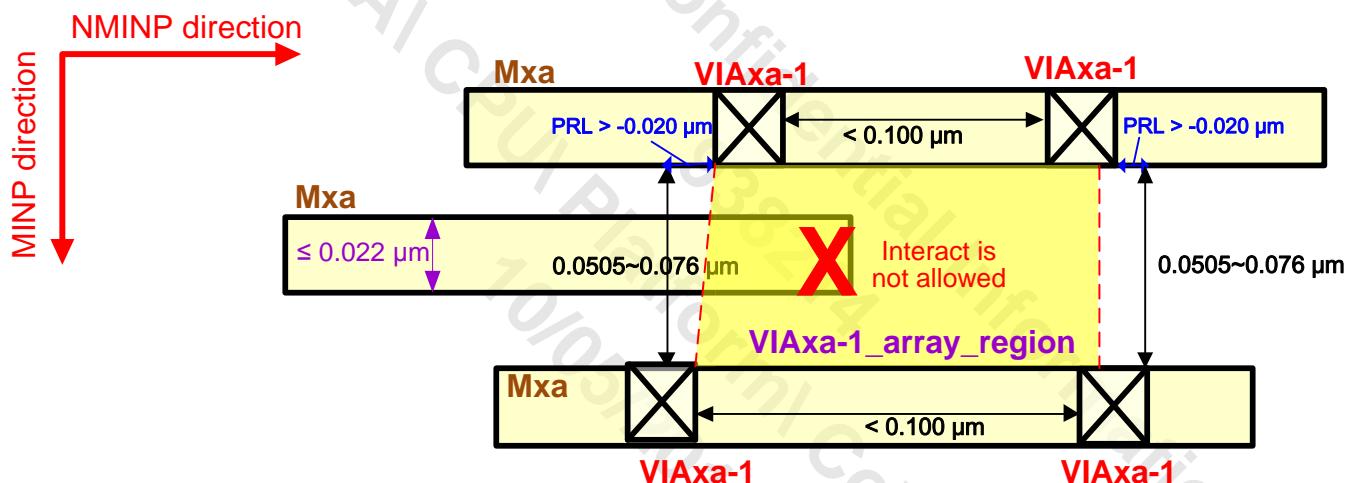
Mxa.R.14



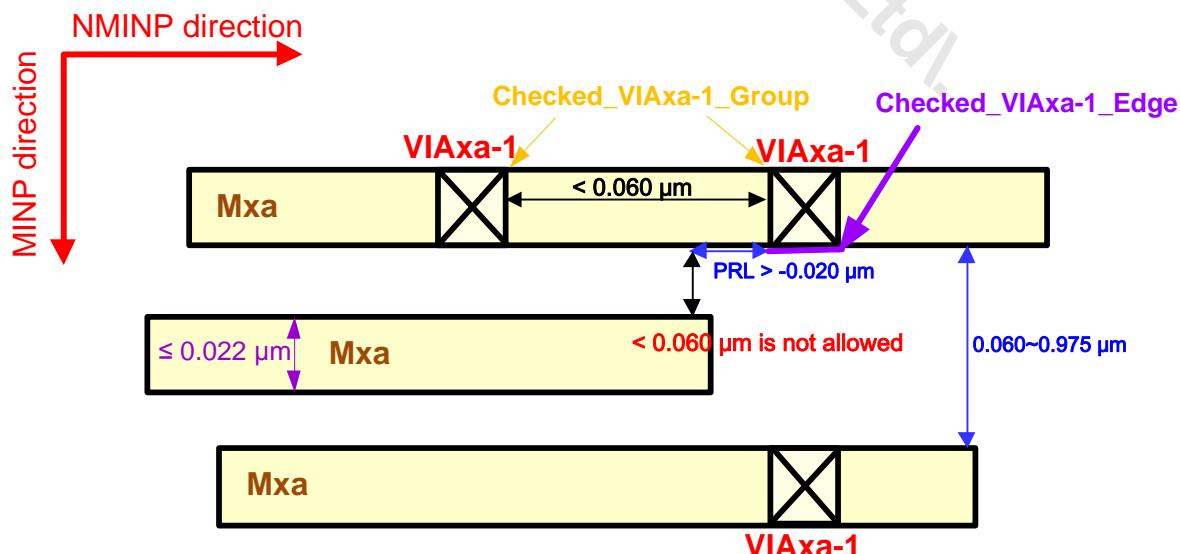
Mxa.R.15



Mxa.R.18



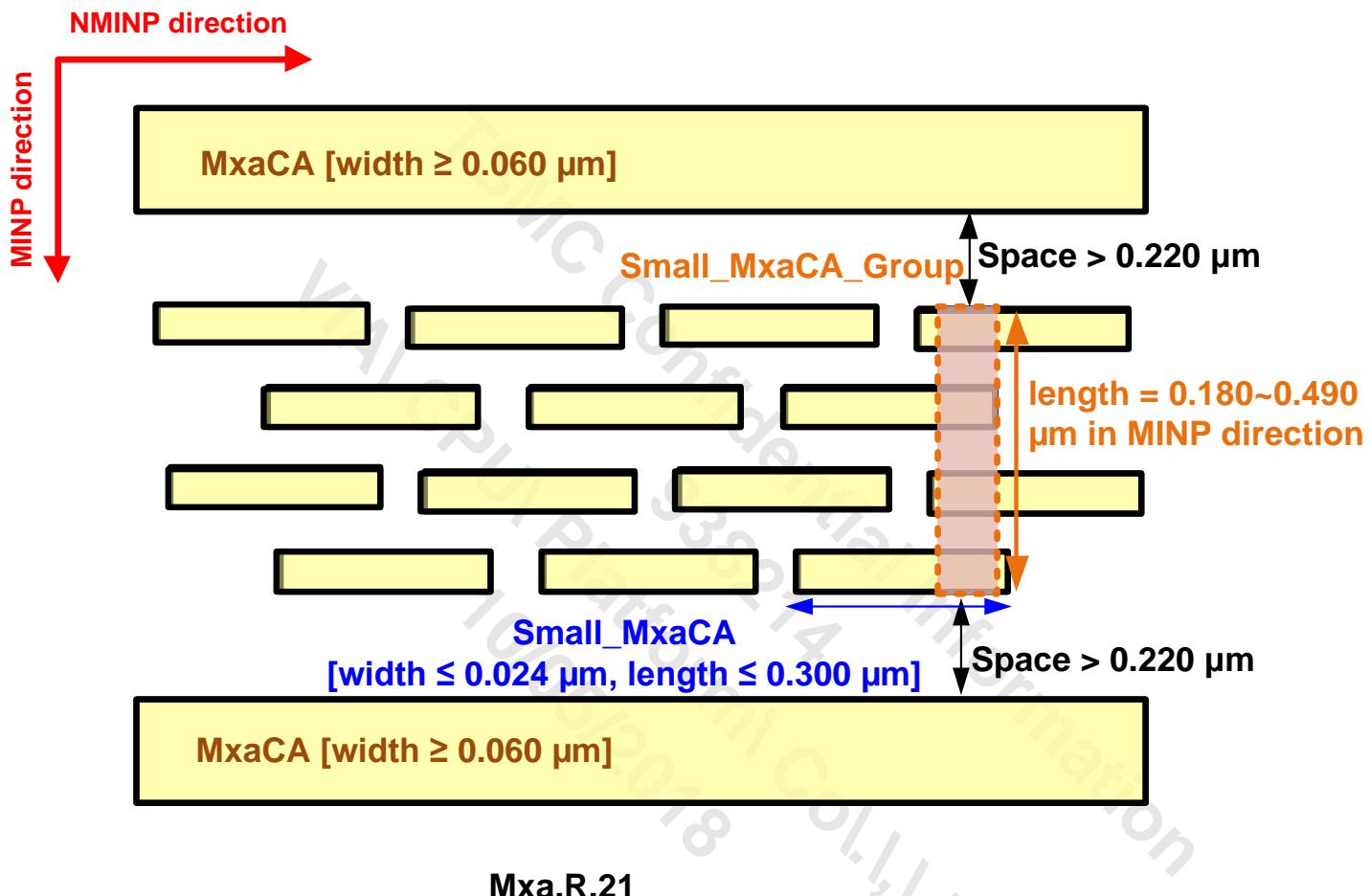
Mxa.R.18.1



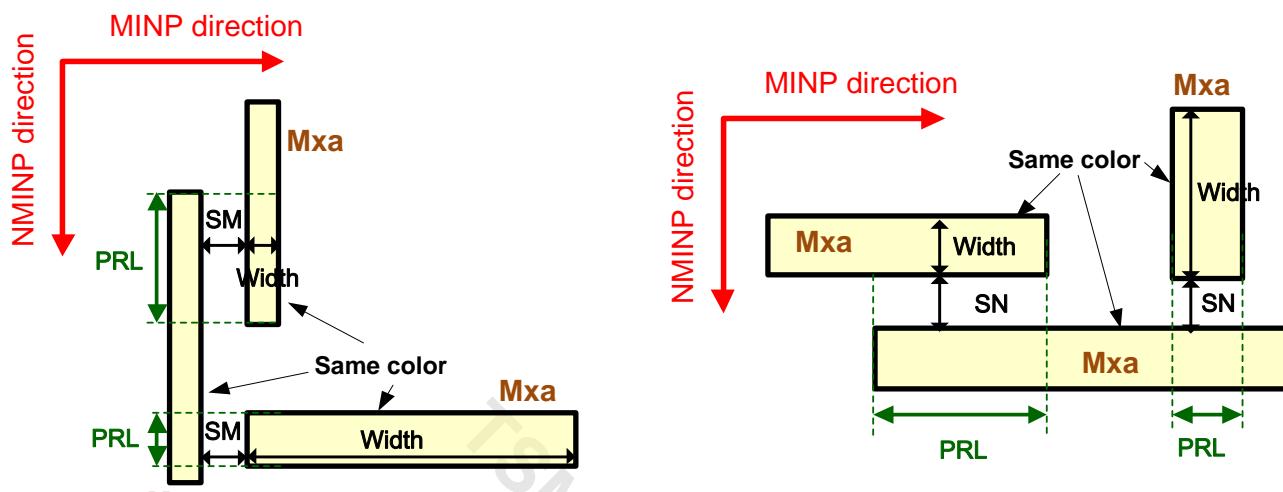
Mxa.R.18.2

Small_MxCA_Group:
{{{Small_MxaCA SIZING up/down 0.033 μm in MINP direction} SIZING down/up 0.0895 μm in MINP direction} [length < 0.140 μm in NMNP direction]} [length = 0.180~0.490 μm in MINP direction]}

Small_MxCA:
MxaCA [width $\leq 0.024 \mu\text{m}$ in MINP direction, length $\leq 0.300 \mu\text{m}$ in NMNP direction]

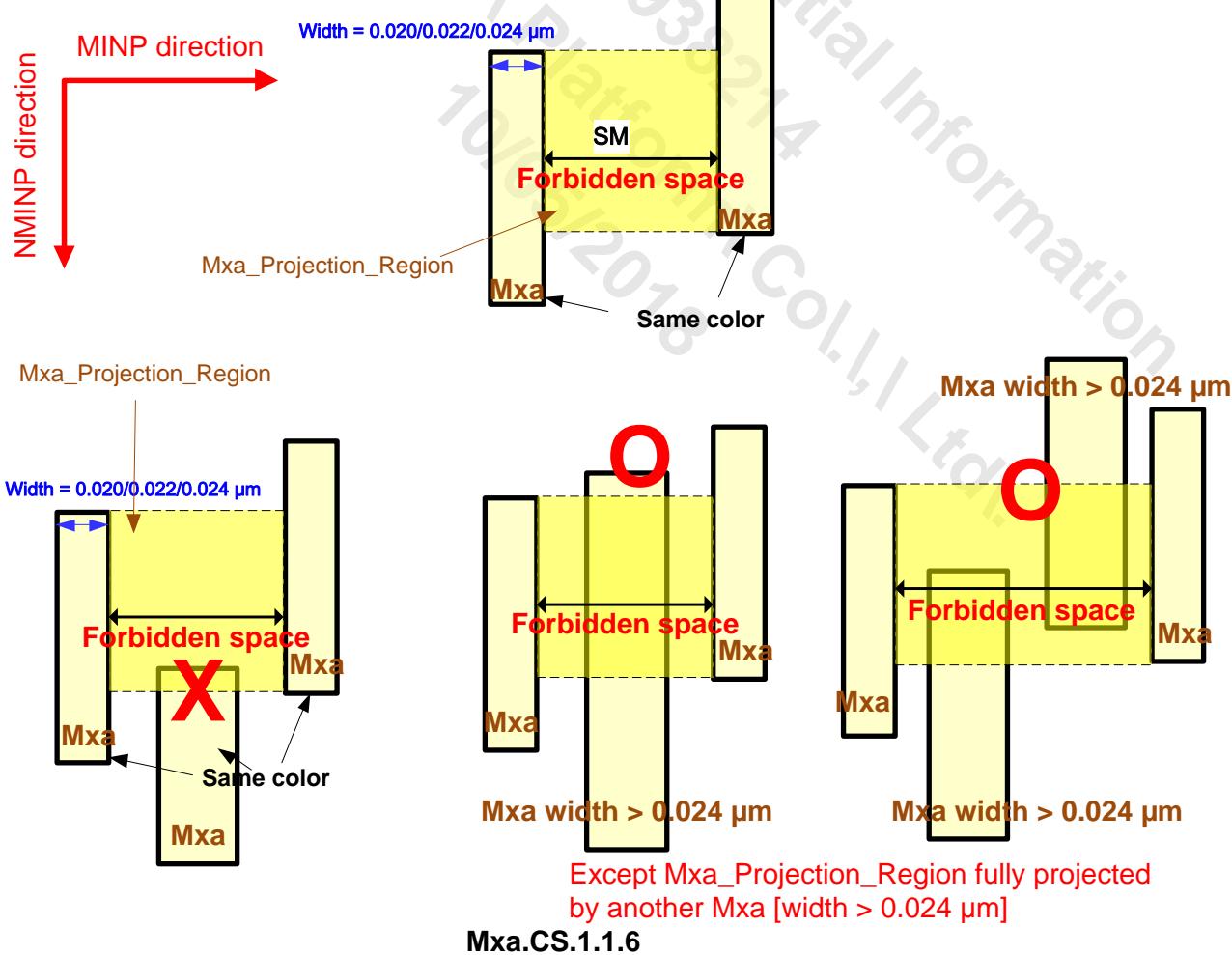


Mxa.R.21

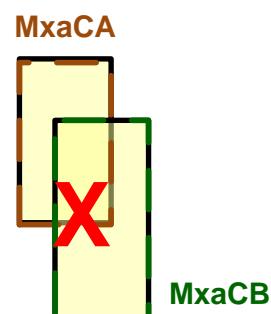
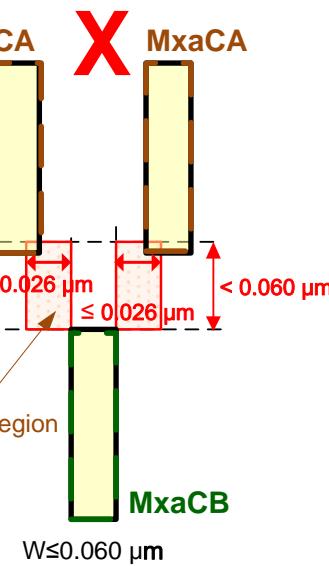
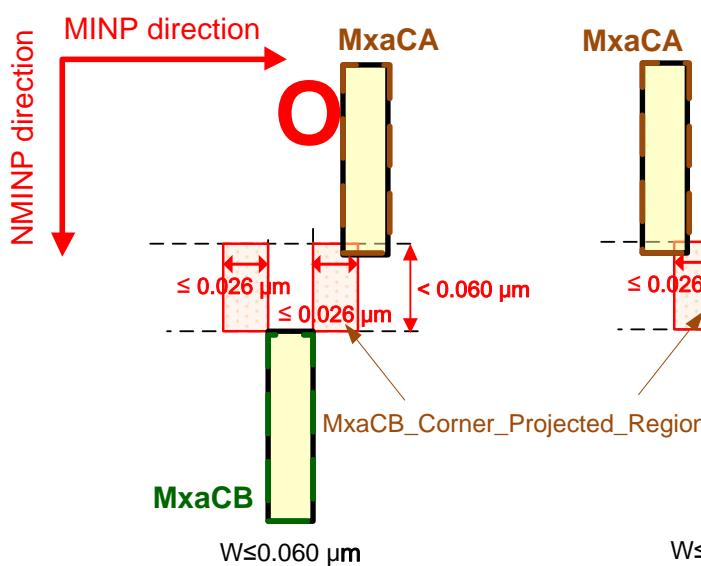
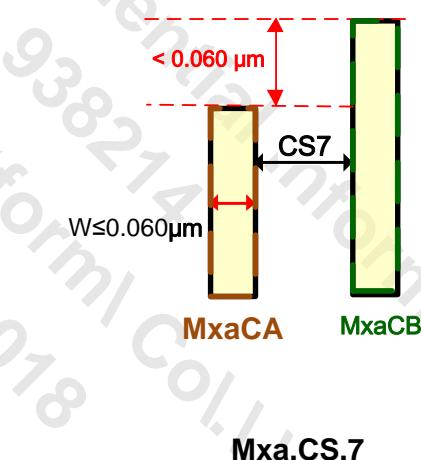
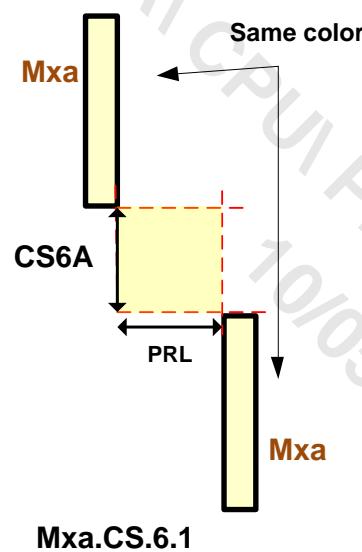
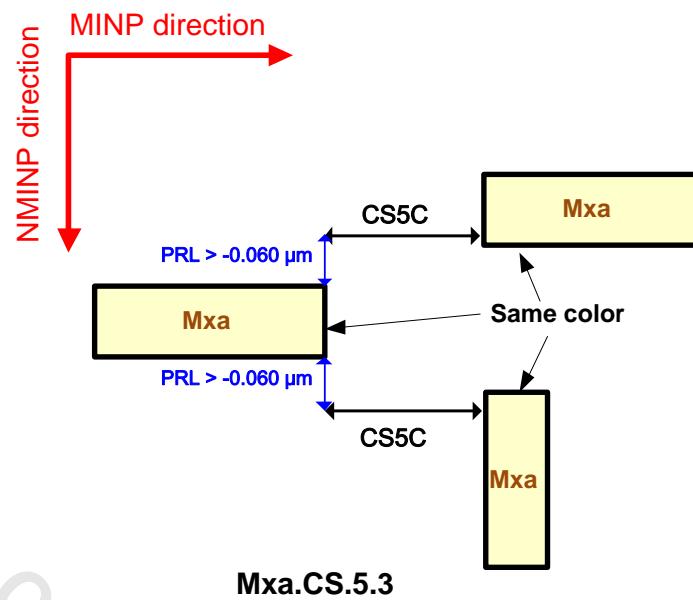
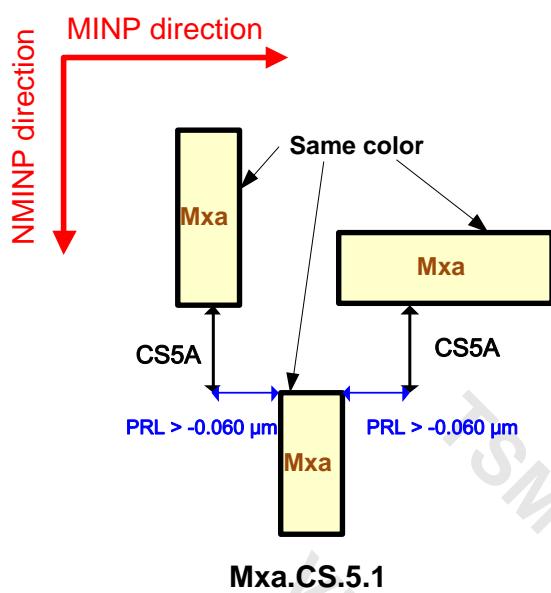


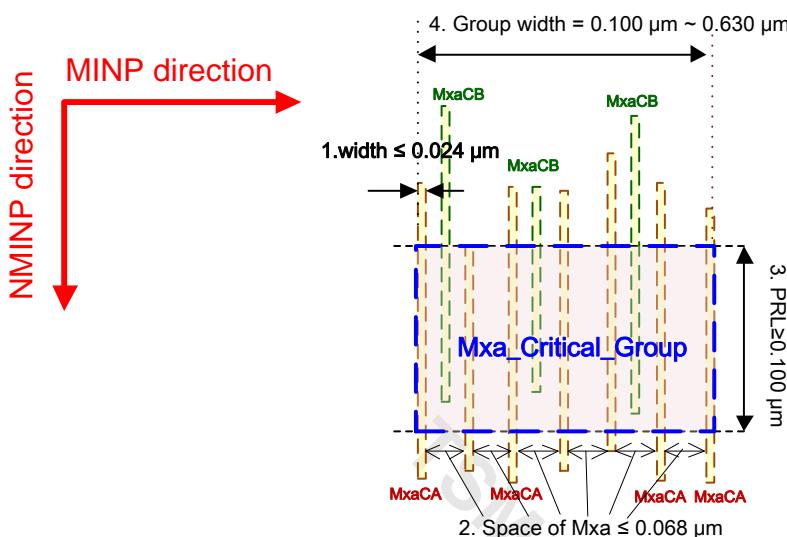
Mxa.CS.0.1 / Mxa.CS.0.2 / Mxa.CS.1.1 /
Mxa.CS.1.1.1 / Mxa.CS.1.1.3 / Mxa.CS.1.1.2 /
Mxa.CS.1.1.2.1 / Mxa.CS.1.1.3 / Mxa.CS.1.1.3.1 /
Mxa.CS.1.1.3.2 / Mxa.CS.1.1.4 / Mxa.CS.1.1.4.1 /
Mxa.CS.1.1.4.2 / Mxa.CS.1.1.7 / Mxa.CS.1.1.8 /
Mxa.CS.1.2 / Mxa.CS.1.2.1 / Mxa.CS.1.3 /
Mxa.CS.1.6 / Mxa.CS.1.7 / Mxa.CS.1.8 /
Mxa.CS.1.9 / Mxa.CS.1.10 / Mxa.CS.1.11

Mxa.CS.0.2 / Mxa.CS.3.2 / Mxa.CS.3.3 /
Mxa.CS.3.4 / Mxa.CS.3.5 / Mxa.CS.3.6 /
Mxa.CS.3.7 / Mxa.CS.3.8 / Mxa.CS.3.9 /
Mxa.CS.3.10 / Mxa.CS.3.11 / Mxa.CS.3.12 /
Mxa.CS.3.13 / Mxa.CS.3.14

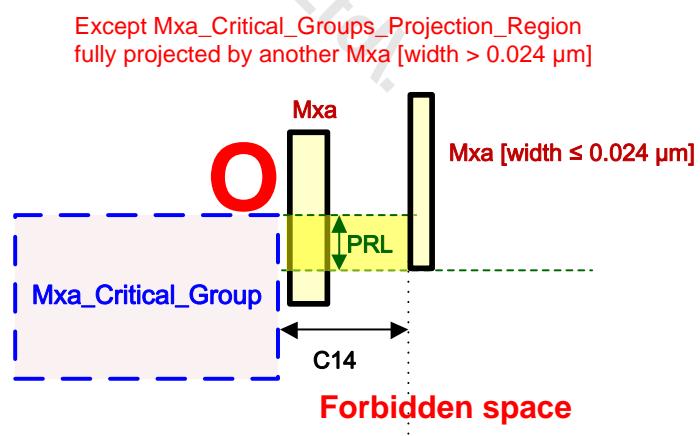
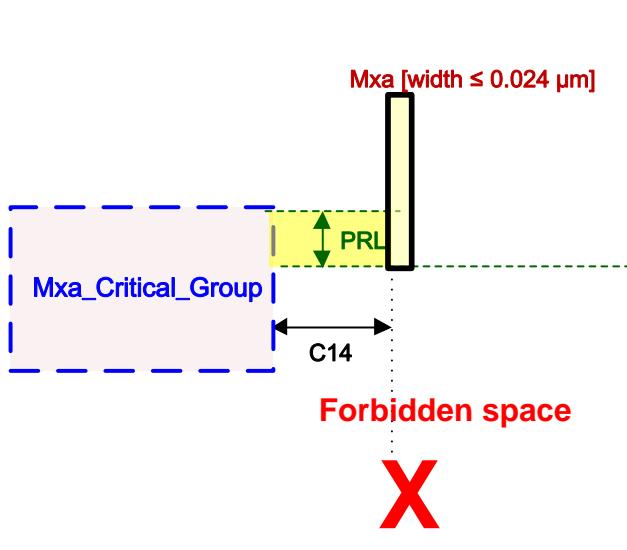
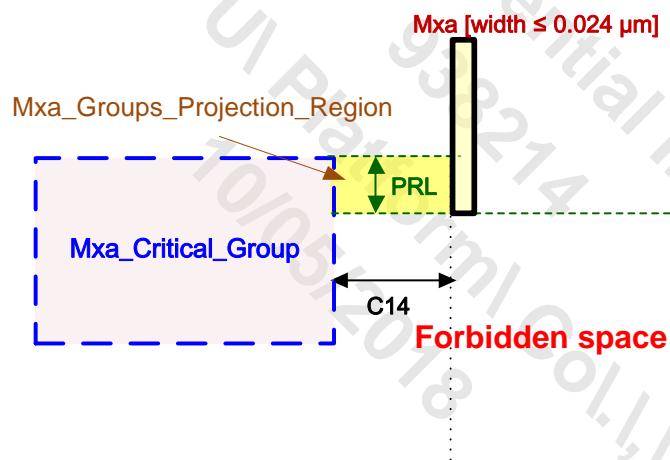


Mxa.CS.8

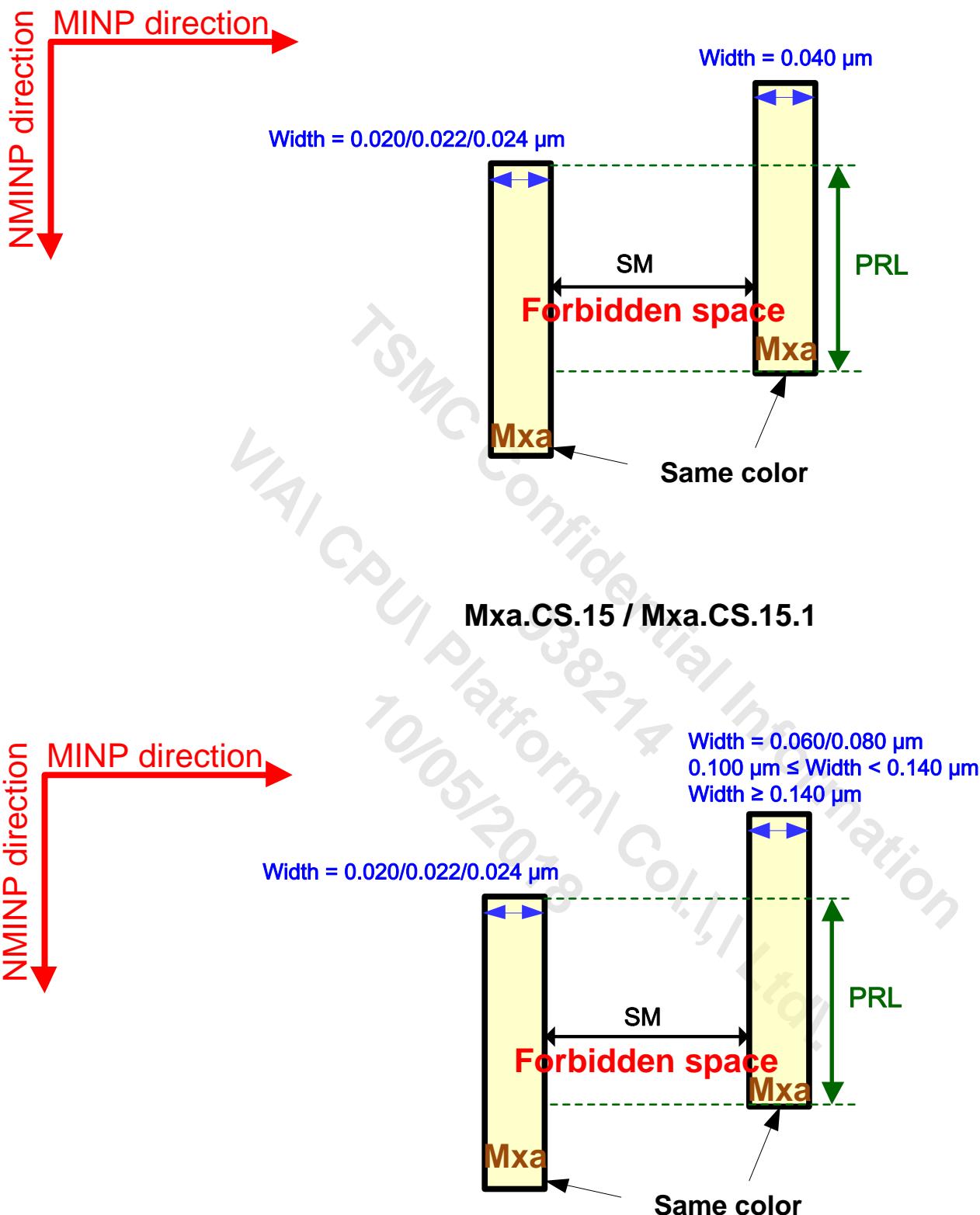




Definition of Mxa_Critical_Group:
 $\{(Mxa \text{ [width} \leq 0.024 \mu\text{m]} \text{ SIZING up/down } 0.032 \mu\text{m}\}$
 $\text{SIZING down/up } 0.0495 \mu\text{m in NMNP direction}\} [0.100 \mu\text{m}$
 $\leq \text{width in MINP direction} \leq 0.630 \mu\text{m}]$



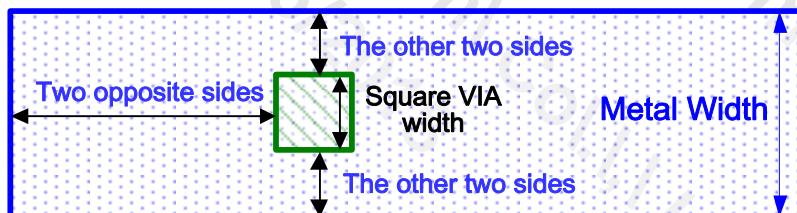
Mxa.CS.14



4.5.49.1 Mxa Enclosure Rule Tabulation

RuleTable.Mxa.EN.31 (Enclosure of square VIA [width = 0.020 μm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
Mxa.EN.31.1.T	width < 0.022 μm	0.0300 μm	0 μm	
Mxa.EN.31.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	
Mxa.EN.31.3.T	0.024 μm ≤ width < 0.028 μm	0.0300 μm	0.0020 μm	
Mxa.EN.31.4.T	0.028 μm ≤ width < 0.040 μm	0.0300 μm	0.0020 μm	BLK_WB
Mxa.EN.31.5.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	BLK_WB
Mxa.EN.31.6.T	0.060 μm ≤ width < 0.080 μm	0.0250 μm	0.0200 μm	
Mxa.EN.31.7.T	0.080 μm ≤ width < 0.260 μm	0.0200 μm	0.0300 μm	BLK_WB
Mxa.EN.31.8.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	

RuleTable.Mxa.EN.33 (Enclosure of square VIA [width = 0.038 μm])				
Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
Mxa.EN.33.1.T	width < 0.060 μm	0.0590 μm	0.0010 μm	
Mxa.EN.33.2.T	0.060 μm ≤ width < 0.080 μm	0.0500 μm	0.0110 μm	
Mxa.EN.33.3.T	0.080 μm ≤ width < 0.100 μm	0.0430 μm	0.0210 μm	
Mxa.EN.33.4.T	0.100 μm ≤ width < 0.120 μm	0.0430 μm	0.0310 μm	
Mxa.EN.33.5.T	0.120 μm ≤ width < 0.260 μm	0.0400 μm	0.0400 μm	
Mxa.EN.33.6.T	width ≥ 0.260 μm	0.0600 μm	0.0500 μm	

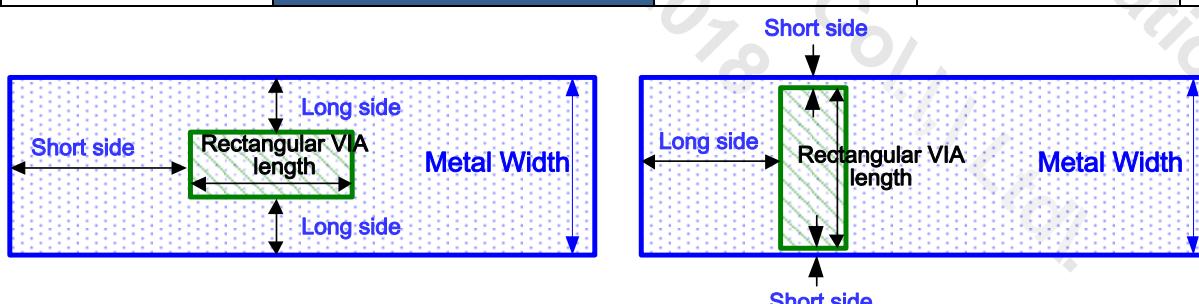


RuleTable.Mxa.EN.32 (Enclosure of rectangular VIA [length = 0.050 µm])

Rule Number	Metal Width	Short side	Long side	Exception
Mxa.EN.32.1.T	width < 0.022 µm	0.0300 µm	0 µm	
Mxa.EN.32.2.T	0.022 µm ≤ width < 0.024 µm	0.0300 µm	0.0010 µm	
Mxa.EN.32.3.T	0.024 µm ≤ width < 0.028 µm	0.0300 µm	0.0020 µm	
Mxa.EN.32.4.T	0.028 µm ≤ width < 0.040 µm	0.0300 µm	0.0020 µm	BLK_WB
Mxa.EN.32.5.T	0.040 µm ≤ width < 0.060 µm	0.0300 µm	0.0100 µm	
Mxa.EN.32.6.T	0.060 µm ≤ width < 0.080 µm	0.0250/0.0050 µm	0.0200/0.0250 µm	
Mxa.EN.32.7.T	width = 0.080 µm	0.0250/0.0150 µm	0.0200/0.0300 µm	
Mxa.EN.32.8.T	0.080 µm < width < 0.260 µm	0.0250/0.0300 µm	0.0300/0.0250 µm	BLK_WB
Mxa.EN.32.9.T	width ≥ 0.260 µm	0.0600 µm	0.0250 µm	

RuleTable.Mxa.EN.34 (Enclosure of rectangular VIA [length = 0.034 μm])

Rule Number	Metal Width	Short side	Long side	Exception
Mxa.EN.34.1.T	width < 0.022 µm	0.0300 µm	0.0000 µm	
Mxa.EN.34.2.T	0.022 µm ≤ width < 0.024 µm	0.0300 µm	0.0010 µm	
Mxa.EN.34.3.T	0.024 µm ≤ width < 0.028 µm	0.0300 µm	0.0020 µm	
Mxa.EN.34.4.T	0.028 µm ≤ width < 0.040 µm	0.0300 µm	0.0040 µm	
Mxa.EN.34.5.T	0.040 µm ≤ width < 0.060 µm	0.0300 µm	0.0100 µm	
Mxa.EN.34.6.T	0.060 µm ≤ width < 0.080 µm	0.0250/0.0050 µm	0.0200/0.0250 µm	
Mxa.EN.34.7.T	width = 0.080 µm	0.0250/0.0150 µm	0.0200/0.0300 µm	
Mxa.EN.34.8.T	0.080 µm < width < 0.260 µm	0.0250/0.0300 µm	0.0300/0.0250 µm	
Mxa.EN.34.9.T	width ≥ 0.260 µm	0.0600 µm	0.0250 µm	



Rule No.	Description	Label	Op.	Rule
Mxa.EN.31.1.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$		\geq	0.0300
Mxa.EN.31.2.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.022 $\mu\text{m} \leq$ width < 0.024 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
Mxa.EN.31.3.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.024 $\mu\text{m} \leq$ width < 0.028 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
Mxa.EN.31.4.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.028 $\mu\text{m} \leq$ width < 0.040 μm] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
Mxa.EN.31.5.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.040 $\mu\text{m} \leq$ width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
Mxa.EN.31.6.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.060 $\mu\text{m} \leq$ width < 0.080 μm] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$		\geq	0.0250
Mxa.EN.31.7.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [0.080 $\mu\text{m} \leq$ width < 0.260 μm] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$ (Except BLK_WB)		\geq	0.0200
Mxa.EN.31.8.T	Enclosure of square Lower_VIA [width = 0.020 μm] by Mxa [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
Mxa.EN.32.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0300
Mxa.EN.32.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [0.022 $\mu\text{m} \leq$ width < 0.024 μm] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
Mxa.EN.32.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [0.024 $\mu\text{m} \leq$ width < 0.028 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
Mxa.EN.32.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [0.028 $\mu\text{m} \leq$ width < 0.040 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$ (Except BLK_WB)		\geq	0.0300
Mxa.EN.32.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [0.040 $\mu\text{m} \leq$ width < 0.060 μm] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
Mxa.EN.32.6.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [0.060 $\mu\text{m} \leq$ width < 0.080 μm] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
Mxa.EN.32.7.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
Mxa.EN.32.8.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [0.080 $\mu\text{m} <$ width < 0.260 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$ (Except BLK_WB)		\geq	0.0250/0.0300
Mxa.EN.32.9.T	Short side enclosure of rectangular Lower_VIA [length = 0.050 μm] by Mxa [width $\geq 0.260 \mu\text{m}$] with the other two long sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
Mxa.EN.33.1.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mxa [width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0590

Rule No.	Description	Label	Op.	Rule
Mxa.EN.33.2.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mxa [0.060 $\mu\text{m} \leq$ width < 0.080 μm] for two opposite sides with the other two sides $\geq 0.0110 \mu\text{m}$		\geq	0.0500
Mxa.EN.33.3.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mxa [0.080 $\mu\text{m} \leq$ width < 0.100 μm] for two opposite sides with the other two sides $\geq 0.0210 \mu\text{m}$		\geq	0.0430
Mxa.EN.33.4.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mxa [0.100 $\mu\text{m} \leq$ width < 0.120 μm] for two opposite sides with the other two sides $\geq 0.0310 \mu\text{m}$		\geq	0.0430
Mxa.EN.33.5.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mxa [0.120 $\mu\text{m} \leq$ width < 0.260 μm] for two opposite sides with the other two sides $\geq 0.0400 \mu\text{m}$		\geq	0.0400
Mxa.EN.33.6.T	Enclosure of square Lower_VIA [width = 0.038 μm] by Mxa [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0500 \mu\text{m}$		\geq	0.0600
Mxa.EN.34.1.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [width < 0.022 μm] with the other two long sides $\geq 0.0000 \mu\text{m}$		\geq	0.0300
Mxa.EN.34.2.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [0.022 $\mu\text{m} \leq$ width < 0.024 μm] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
Mxa.EN.34.3.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [0.024 $\mu\text{m} \leq$ width < 0.028 μm] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
Mxa.EN.34.4.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [0.028 $\mu\text{m} \leq$ width < 0.040 μm] with the other two long sides $\geq 0.0040 \mu\text{m}$		\geq	0.0300
Mxa.EN.34.5.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [0.040 $\mu\text{m} \leq$ width < 0.060 μm] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
Mxa.EN.34.6.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [0.060 $\mu\text{m} \leq$ width < 0.080 μm] with the other two long sides $\geq 0.0200/0.0250 \mu\text{m}$		\geq	0.0250/0.0050
Mxa.EN.34.7.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [width = 0.080 μm] with the other two long sides $\geq 0.0200/0.0300 \mu\text{m}$		\geq	0.0250/0.0150
Mxa.EN.34.8.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [0.080 $\mu\text{m} <$ width < 0.260 μm] with the other two long sides $\geq 0.0300/0.0250 \mu\text{m}$		\geq	0.0250/0.0300
Mxa.EN.34.9.T	Short side enclosure of rectangular Lower_VIA [length = 0.034 μm] by Mxa [width $\geq 0.260 \mu\text{m}$] with the other two long sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600

4.5.50 VIAya Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
VIAya.W.1	Width (Except SEALRING_ALL)	W1	=	0.0200, 0.0380
VIAya.W.2	Width of VIAya bar in SEALRING_ALL	W2	=	0.1400
VIAya.S.1	Space (Except SEALRING_ALL)	S1	\geq	0.0850
VIAya.S.1.1	Space of VIAya [PRL > -0.050 μm] (Except SEALRING_ALL)	S1A	\geq	0.0940
VIAya.S.1.2	Space (Except SEALRING_ALL, or following conditions: 1. VIAya_Group) Definition of VIAya_Group follows VIAya.S.14	S1B	\geq	0.0870
VIAya.S.2	Space of the long side of rectangular VIAya to rectangular VIAya [PRL > -0.089 μm]	S2	\geq	0.1000
VIAya.S.2.1	Space of the short side of rectangular VIAya to neighboring VIAya [PRL > -0.034 μm]	S2A	\geq	0.1340
VIAya.S.2.1.1	Space of the long side of rectangular VIAya to square VIAya [PRL > -0.105 μm]	S2A1	\geq	0.0910
VIAya.S.2.1.2	Space of the long side of rectangular VIAya to square VIAya [PRL > -0.073 μm]	S2A2	\geq	0.0950
VIAya.S.2.2	Space of the short side of rectangular VIAya to neighboring rectangular VIAya [PRL > -0.044 μm]	S2B	\geq	0.1340
VIAya.S.2.3	Corner-to-corner space of rectangular VIAya to rectangular VIAya [long side PRL \leq -0.089 μm , short side \leq -0.044 μm]	S2C	\geq	0.1340
VIAya.S.8	Space to VIAxa or VIAx [maximum delta V > 0.96V]	S8	\geq	0.0620
VIAya.S.8.1	Space to VIAxa or VIAx [maximum delta V > 1.32V] (1.2V + 10%)	S8	\geq	0.0640
VIAya.S.8.2	Space to VIAxa or VIAx [maximum delta V > 1.65V] (1.5V + 10%)	S8	\geq	0.0700
VIAya.S.8.3	Space to VIAya or VIAxa or VIAx [maximum delta V > 1.98V] (1.8V + 10%)	S8	\geq	0.0820
VIAya.S.8.4	Space to VIAya or VIAxa or VIAx [maximum delta V > 2.75V] (2.5V + 10%)	S8	\geq	0.0870
VIAya.S.12	Space to Isolating_Edge_Semi-iso_VIAya [Dense_Edge_Semi-iso_VIAya enclosure by Mya+1 < 0.016 μm] [PRL > -0.096 μm] Definition of Semi-iso_VIAya: VIAya [PRL > -0.0525 μm] one side space to Mya+1 \leq 0.058 μm , and the other side space > 0.058 μm in MINP direction Definition of Isolating_Edge_Semi-iso_VIAya: Semi-iso_VIAya edge [space to Mya+1 > 0.058 μm in MINP direction] Definition of Dense_Edge_Semi-iso_VIAya: Semi-iso_VIAya edge [space to Mya+1 \leq 0.058 μm in MINP direction]	S12	\geq	0.1000
VIAya.S.14	Space to VIAya_Group Definition of VIAya_Group: 2 or 3 square VIAya space < 0.086 μm in one group, and DRC flags the square VIAya numbers > 3 in one group.	S14	\geq	0.0910
VIAya.S.19	Space of VIAya [Mya+1 enclosure of VIAya > 0 μm] to VIAx or VIAxa [different net and PRL > 0 μm]	S19	\geq	0.0260
VIAya.S.21	Space of VIAya [width = 0.038 μm] to VIAya	S21	\geq	0.0955
VIAya.S.21.1	Space of VIAya [width = 0.038 μm] to VIAya [PRL > -0.038 μm]	S21A	\geq	0.1120
VIAya.S.21.2	Space of VIAya [width = 0.038 μm] to square VIAya [width = 0.020 μm]	S21B	\geq	0.1070

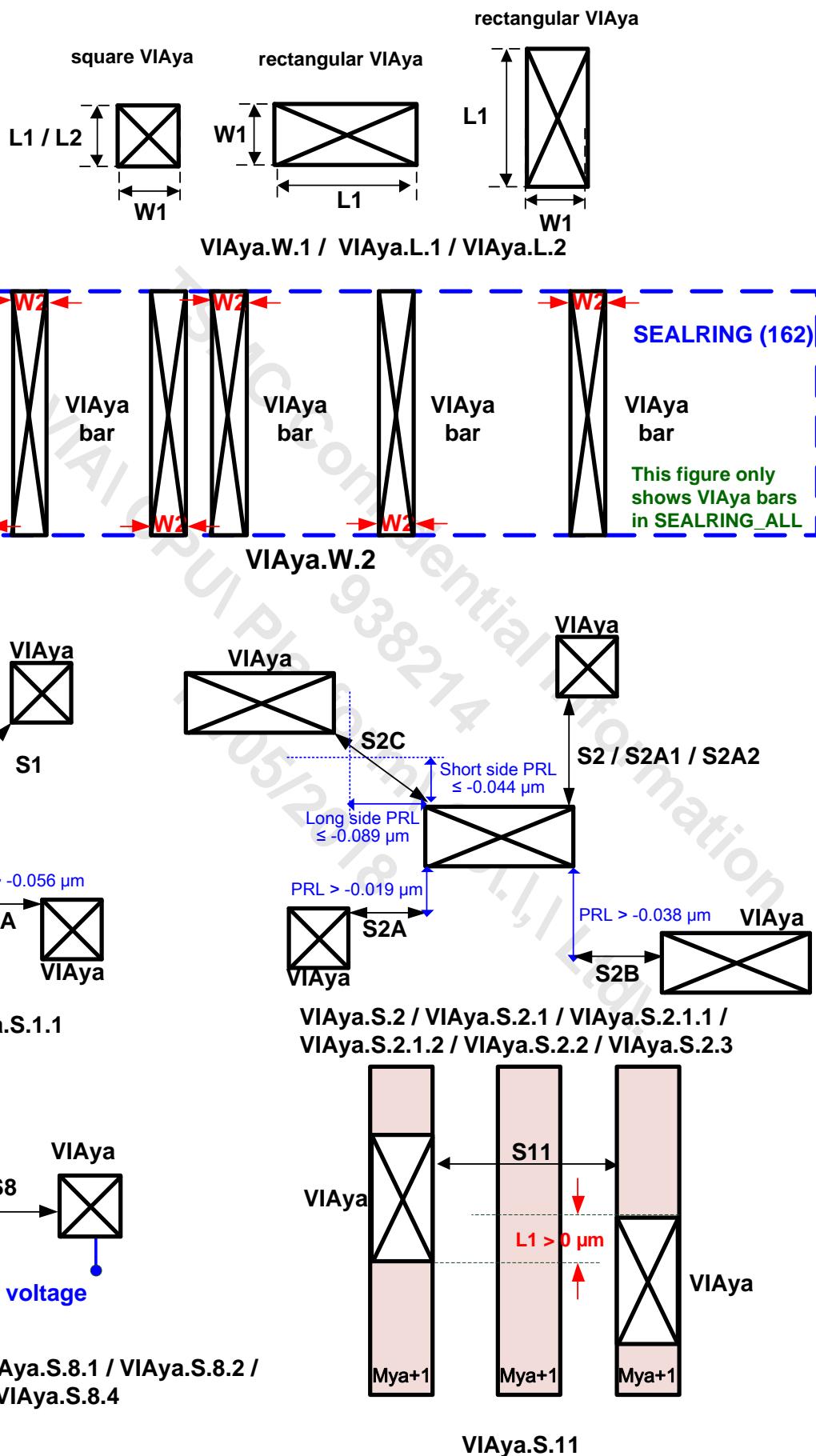
Rule No.	Description	Label	Op.	Rule
VIAya.S.21.3	Space of VIAya [width = 0.038 μm] to square VIAya [width = 0.020 μm] [PRL > -0.047 μm]	S21C	≥	0.1120
VIAya.S.21.4	Space of VIAya [width = 0.038 μm] to rectangular VIAya	S21D	≥	0.5000
VIAya.S.29	Space of square VIAya to Mya+1_Concave_Corner Definition of Mya+1_Concave_Corner: A rectangle [0.001 μm x 0.001 μm] abut both edge of Mya+1 concave corner	S29	≥	0.0100
VIAya.EN.0	1. Enclosure of square VIAya [width = 0.020 μm] is defined by RuleTable.VIAya.EN.31 in the subsection 2. Enclosure of square VIAya [width = 0.038 μm] is defined by RuleTable.VIAya.EN.33 in the subsection 3. Enclosure of rectangular VIAya [length = 0.050 μm] is defined by RuleTable.VIAya.EN.32 in the subsection			
VIAya.EN.2.1	Enclosure of square VIAya by Mx or Mxa [width = 0.028 μm, INTERACT BCWDMY] with the other two sides ≥ 0.004 μm	EN2A	≥	0.0300
VIAya.EN.6.2.1	Short side enclosure of rectangular VIAya by Mx or Mxa [width = 0.028 μm, INTERACT BCWDMY] with the other two sides ≥ 0.004 μm	EN6	≥	0.0300
VIAya.EN.7.3	Short side enclosure of rectangular VIAya by Mx or Mxa edge [length = 0.080 μm, Mx/Mxa width = 0.080 μm]	EN7	≥	0.0250
VIAya.EN.16.10	Checked_VIAya_Edge1 enclosure by Mx or Mxa in Mx or Mxa MINP direction Definition of Checked_VIAya: VIAya INTERACT Mya+1 width > 0.040 μm Definition of Checked_VIAya_Edge1: 1. Checked_VIAya edge space to {MxCA OR MxCB} or {MxaCA OR MxaCB} < 0.040 μm with PRL > -0.100 μm in Mx or Mxa MINP direction	EN16J	≥	0.0020
VIAya.EN.16.11	Checked_VIAya_Edge2 enclosure by Mx or Mxa in Mx or Mxa MINP direction Definition of Checked_VIAya: VIAya INTERACT Mya+1 width ≤ 0.040 μm Definition of Checked_VIAya_Edge2: 1. Checked_VIAya edge space to {MxCA OR MxCB} or {MxaCA OR MxaCB} < 0.040 μm with PRL > -0.100 μm in Mx or Mxa MINP direction	EN16K	≥	0.0010
VIAya.L.1	Length of VIAya [width = 0.020 μm]	L1	=	0.0200, 0.0500
VIAya.L.2	Length of VIAya [width = 0.038 μm]	L2	=	0.0380
VIAya.R.0	45-degree VIAya is not allowed			
VIAya.R.2	Redundant via requirement must follow RuleTable.VIAya.R.2 of VIAya numbers and space (S1) for Mx/Mxa and Mya+1 connection. [One of Mx/Mxa or Mya+1 has width and length (W1) > 0.160 μm]. (Except following conditions: 1. VIA bar)			
VIAya.R.2.1	Redundant via requirement must follow RuleTable.VIAya.R.2.1 of VIAya numbers and space (S1) for Mx/Mxa and Mya+1 connection. [One of Mx/Mxa or Mya+1 has width and length (W1) > 0.300 μm]. (Except following conditions: 1. VIA bar)			
VIAya.R.3	Redundant via requirement must follow RuleTable.VIAya.R.3 of VIAya numbers and space (S1) for Mx/Mxa and Mya+1 connection. [One of Mx/Mxa or Mya+1 has width and length (W1) > 0.412 μm]. Refer to VIAya.R.3 table behind. (Except following conditions: 1. VIA bar)			

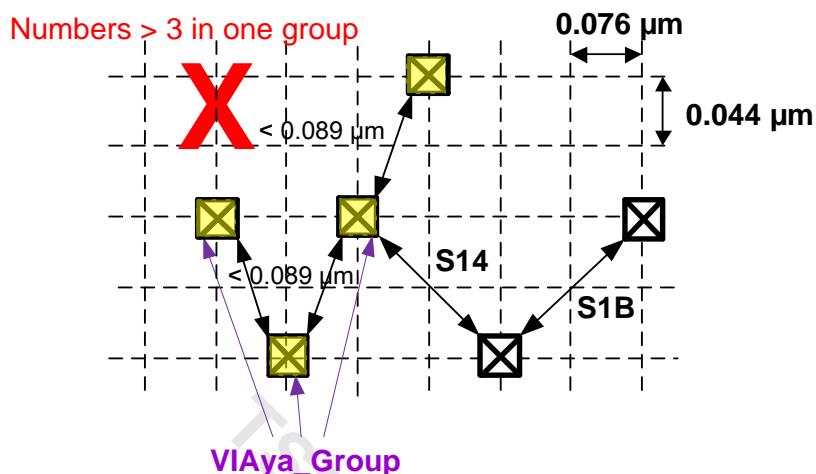
Rule No.	Description	Label	Op.	Rule
VIAya.R.4	At least two square VIAya [width = 0.020 μm] or one {rectangular VIAya OR square VIAya [width = 0.038 μm] must be used for a connection that distance $\leq 0.500 \mu\text{m}$ (D) away from a metal plate (either Mx/Mxa or Mya+1) with length $\geq 0.120 \mu\text{m}$ (L) and width $\geq 0.120 \mu\text{m}$ (W) (Except following conditions: 1. VIA bar)			
VIAya.R.5	At least two square VIAya [width = 0.020 μm] or one {rectangular VIAya OR square VIAya [width = 0.038 μm] must be used for a connection that distance $\leq 1 \mu\text{m}$ (D) away from a metal plate (either Mx/Mxa or Mya+1) with length $> 0.270 \mu\text{m}$ (L) and width $> 0.270 \mu\text{m}$ (W) (Except following conditions: 1. VIA bar)			
VIAya.R.6	At least two square VIAya [width = 0.020 μm] or one {rectangular VIAya OR square VIAya [width = 0.038 μm] must be used for a connection that distance $\leq 3 \mu\text{m}$ (D) away from a metal plate (either Mx/Mxa or Mya+1) with length $> 0.540 \mu\text{m}$ (L) and width $> 0.540 \mu\text{m}$ (W) (Except following conditions: 1. VIA bar)			
VIAya.R.6.1	At least two square VIAya [width = 0.020 μm] or one {rectangular VIAya OR square VIAya [width = 0.038 μm] must be used for a connection that distance $\leq 5 \mu\text{m}$ (D) away from a metal plate (either Mx/Mxa or Mya+1) with length $> 1 \mu\text{m}$ (L) and width $> 1 \mu\text{m}$ (W) (Except following conditions: 1. VIA bar)			
VIAya.R.7	VIAya must be fully covered by {Mx AND Mya+1} or {Mxa AND Mya+1}			
VIAya.R.8	Single VIAya is not allowed in "H-shape" Mya+1 when all of the following conditions come into existence: 1. The Mya+1 has "H-shape" interact two metal holes: both two metal hole length (L2) $\leq 4.5 \mu\text{m}$ and two metal hole area $\leq 4.05 \mu\text{m}^2$ 2. The VIAya overlaps on the center metal bar of this "H-shape" Mya+1 3. The center metal bar length $\leq 0.900 \mu\text{m}$ (L) and the metal bar width $\leq 0.120 \mu\text{m}$			
VIAya.R.9®	Recommended maximum consecutive stacked VIAya layer, which has only one via for each VIAya layer to avoid high Rc		\leq	4
VIAya.R.10.2	Overlap MetalFuse_B1 (156;8) is not allowed			
VIAya.R.13	Maximum area ratio of Mx/Mxa to upper VIAya in the same net [connects to gate with area $> 10700 \mu\text{m}^2$, and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = $(2.5 \times WdxLd)$ for ≥ 2 -fin device		\leq	350000
VIAya.R.13.2	Maximum area ratio of I/O gate to single layer VIAya in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area $\geq 0.25 \mu\text{m}^2$) Definition: Gate area = $(2.5 \times WdxLd)$ for ≥ 2 -fin device		\leq	300000

Table Notes

- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

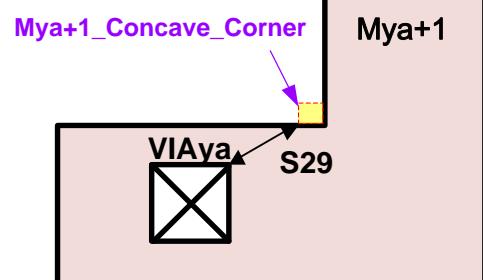
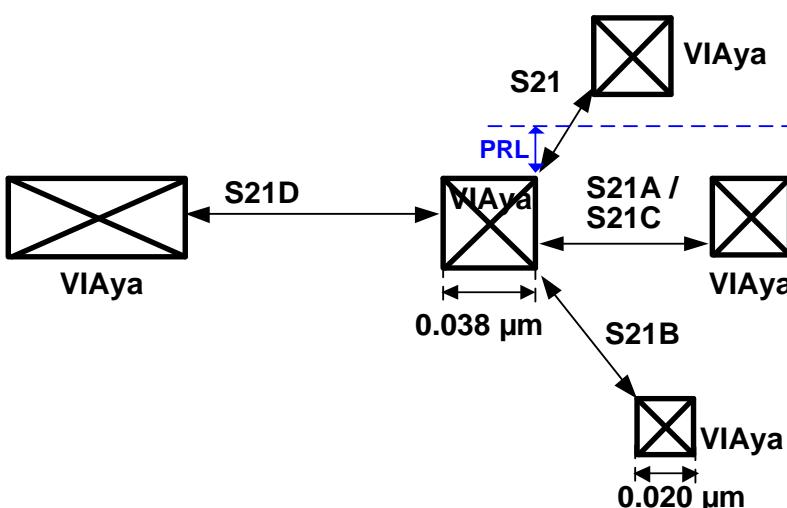
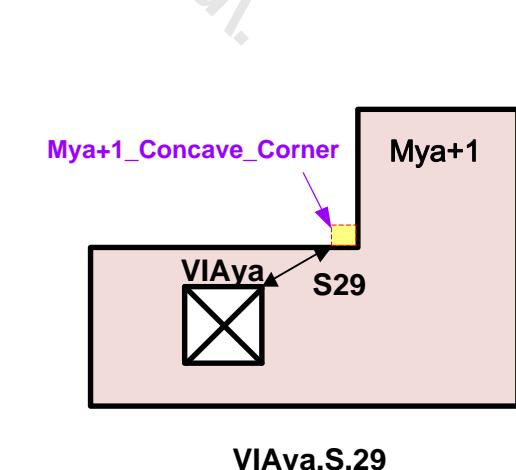
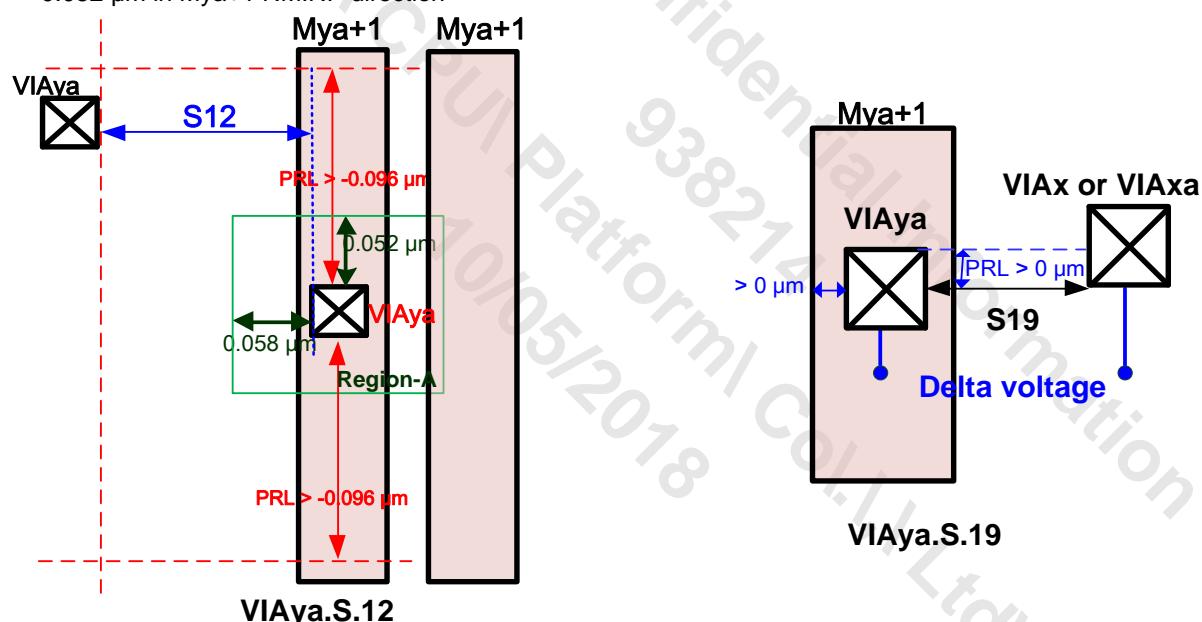
VIAya

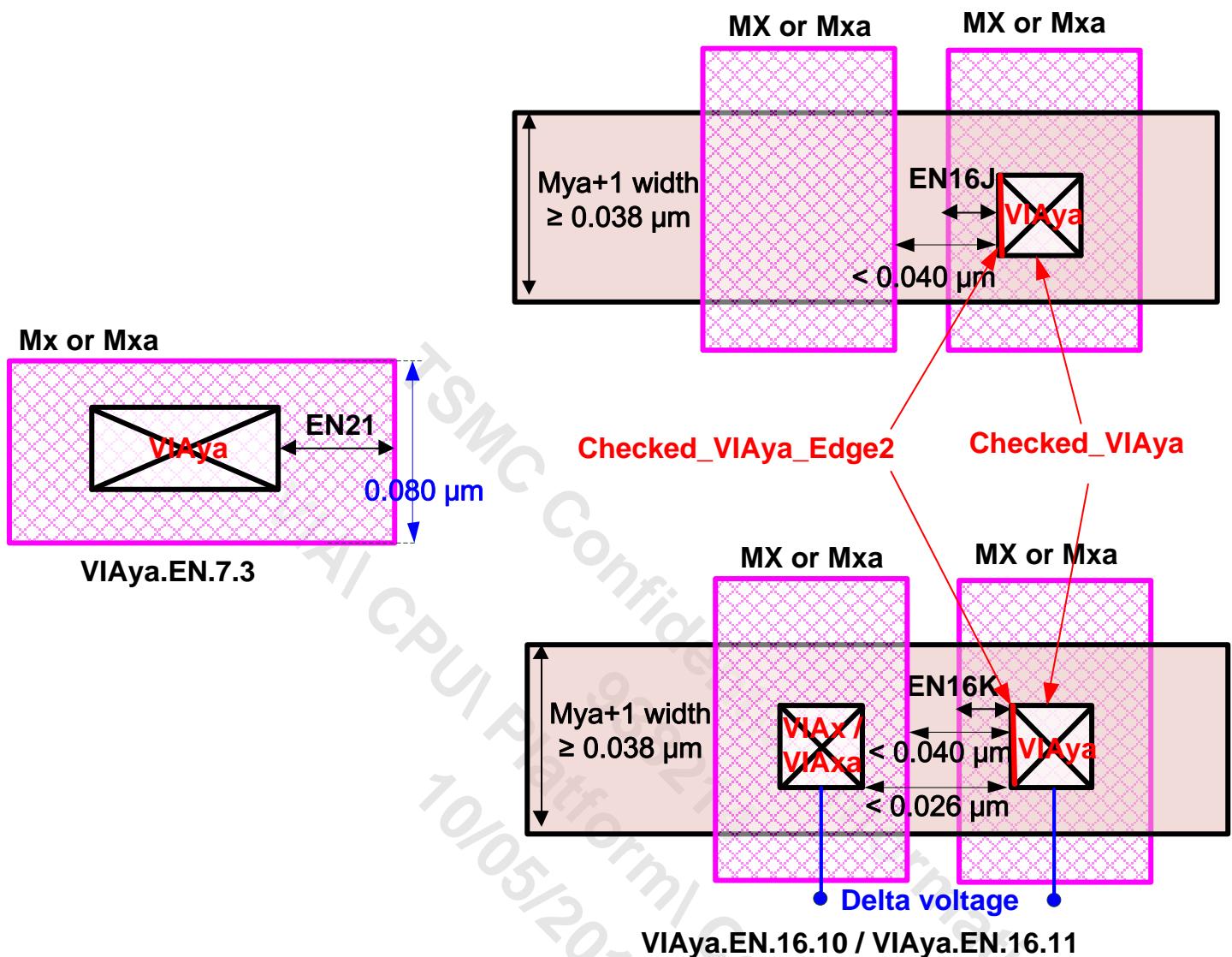


**VIAya.S.1.2 / VIAya.S.14**

Definition of VIAya_Search_Region:

A rectangle formed by VIAya edge expanding 0.058 μm in Mya+1 MINP direction and expanding 0.052 μm in Mya+1 NMINP direction



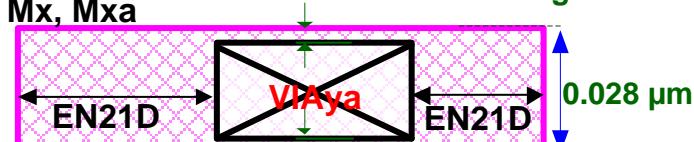


BCWDMY

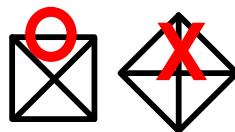
Enclosure of the other two sides



Enclosure of the other two long sides

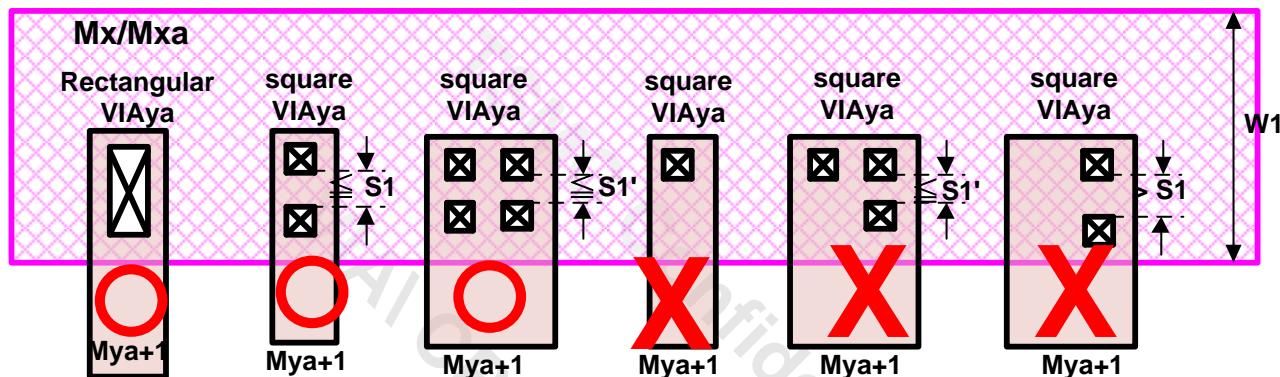


VIAya.EN.2.1 / VIAya.EN.6.2.1



45-degree VIAya is not allowed.

VIAya.R.0

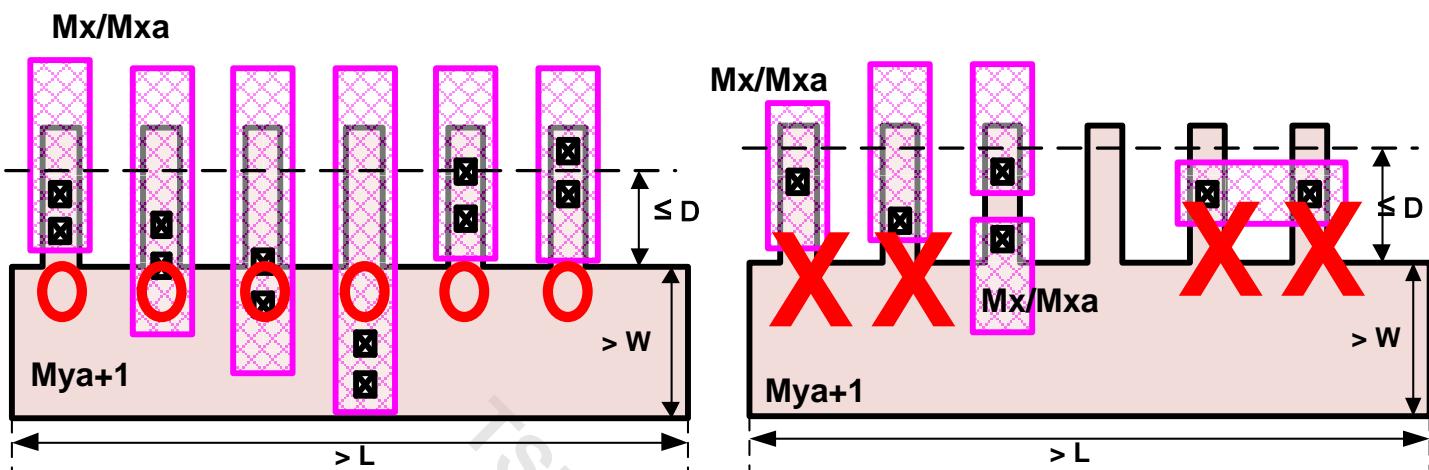


VIAya.R.2 / VIAya.R.2.1 / VIAya.R.3

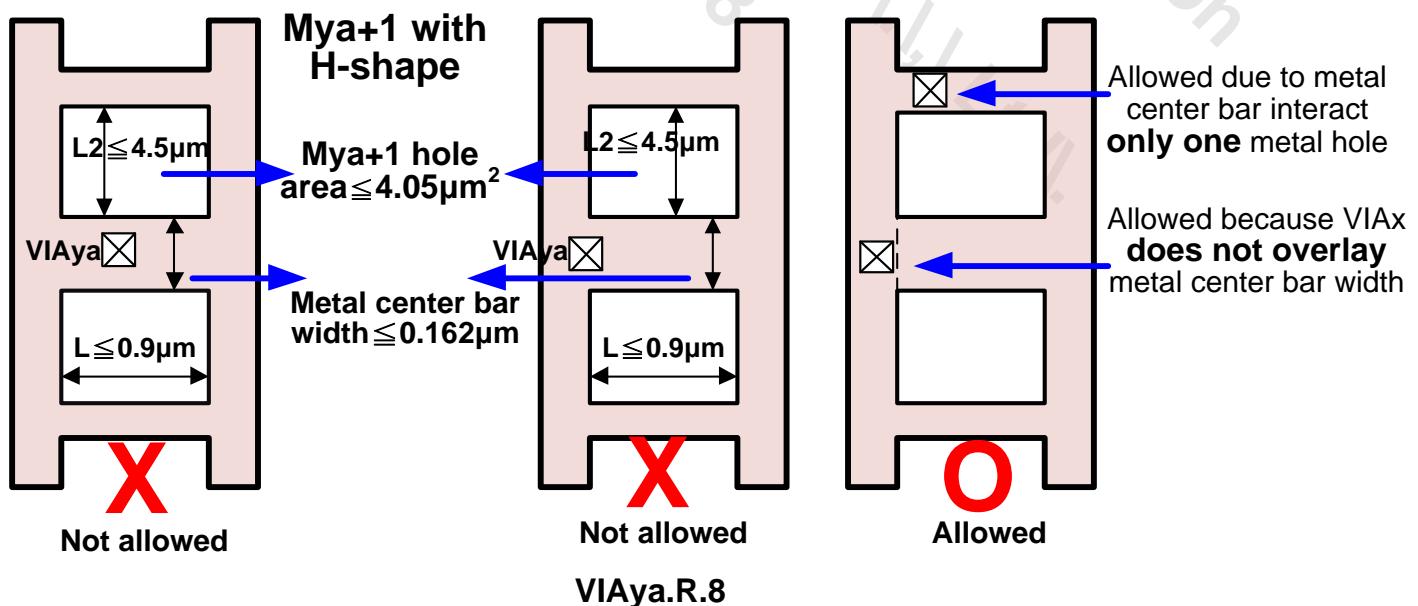
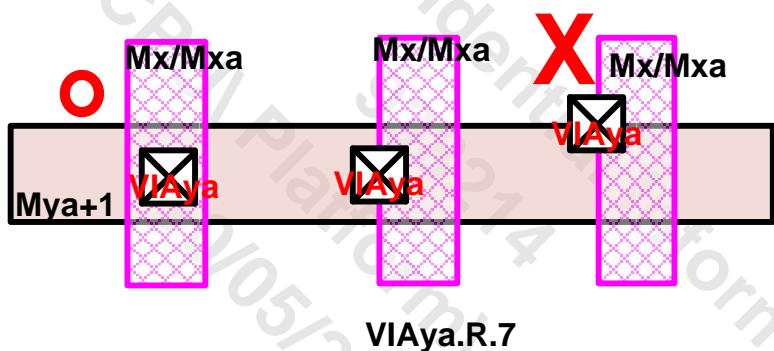
RuleTable.VIAya.R.2	$0.160 \mu\text{m} < W1 \leq 0.300 \mu\text{m}$							
VIAya space (S1) (μm)	$0.070 \leq S1 \leq 0.160$				$0.160 < S1 \leq 0.400$			
{Rectangular VIAya [width/length = 0.020/0.050 μm] OR square VIAya [width = 0.038 μm] (#)}	0	1	/	/	0	1	2	/
Square VIAya [width = 0.020 μm] (#)	≥ 2	≥ 0	/	/	≥ 4	≥ 2	≥ 0	/

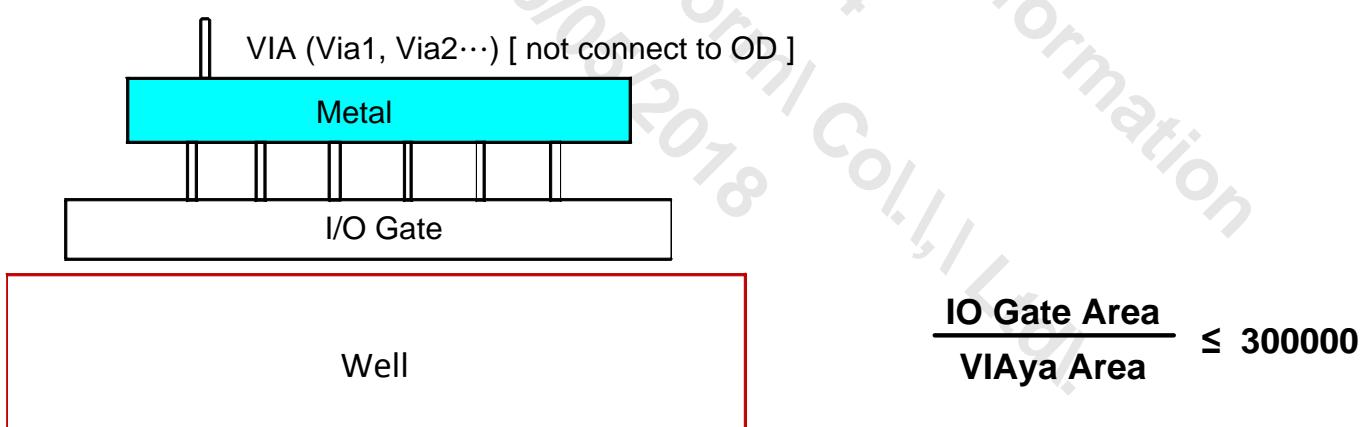
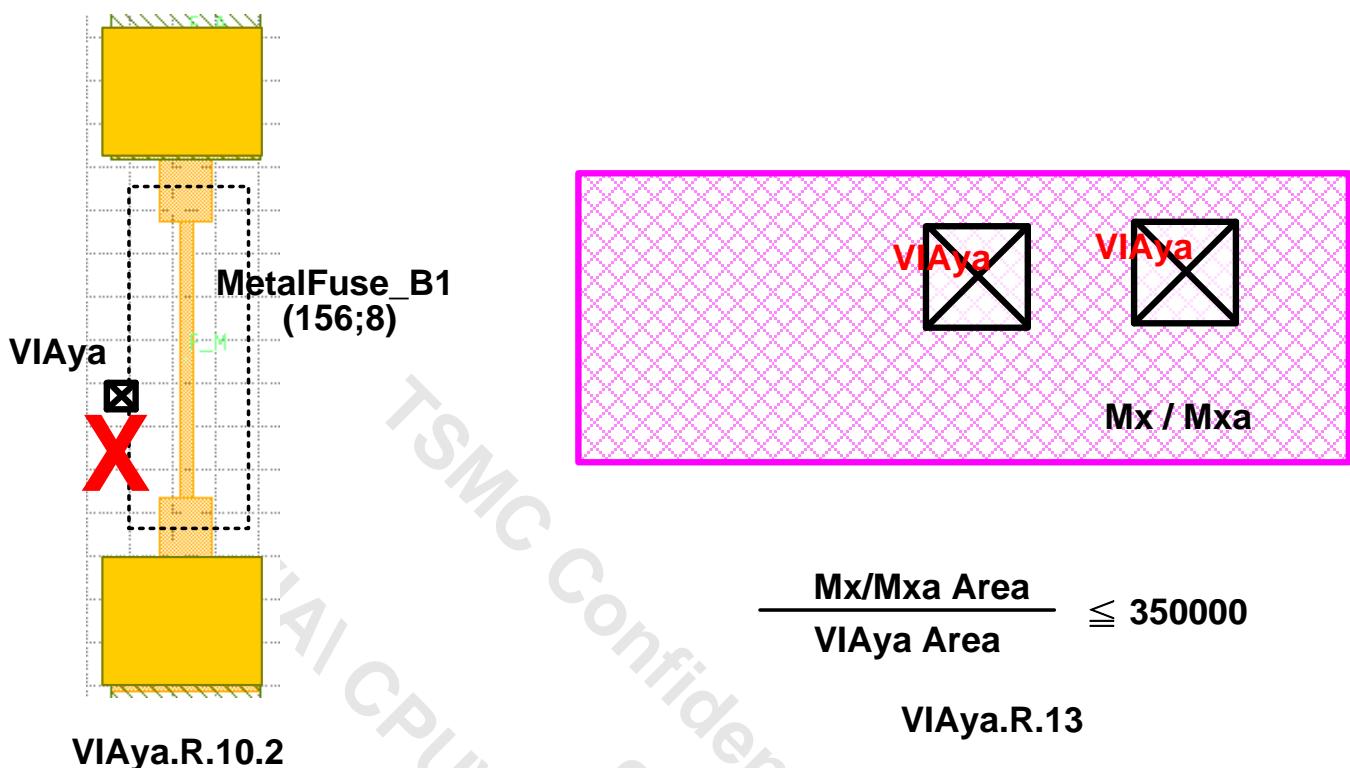
RuleTable.VIAya.R.2.1	$0.300 \mu\text{m} < W1 \leq 0.412 \mu\text{m}$							
VIAya space (S1) (μm)	$0.070 \leq S1 \leq 0.160$				$0.160 < S1 \leq 0.400$			
{Rectangular VIAya [width/length = 0.020/0.050 μm] OR square VIAya [width = 0.038 μm] (#)}	0	1	2	/	0	1	2	3
Square VIAya [width = 0.020 μm] (#)	≥ 3	≥ 1	≥ 0	≥ 6	≥ 4	≥ 2	≥ 0	/

RuleTable.VIAya.R.3	$W1 > 0.412 \mu\text{m}$							
VIAya space (S1) (μm)	$0.070 \leq S1 \leq 0.160$				$0.160 < S1 \leq 0.400$			
{Rectangular VIAya [width/length = 0.020/0.050 μm] OR square VIAya [width = 0.038 μm] (#)}	0	1	2	/	0	1	2	3
Square VIAya [width = 0.020 μm] (#)	≥ 4	≥ 2	≥ 0	≥ 9	≥ 7	≥ 5	≥ 3	≥ 1



VIAYa.R.4 / VIAYa.R.5 / VIAYa.R.6 / VIAYa.R.6.1





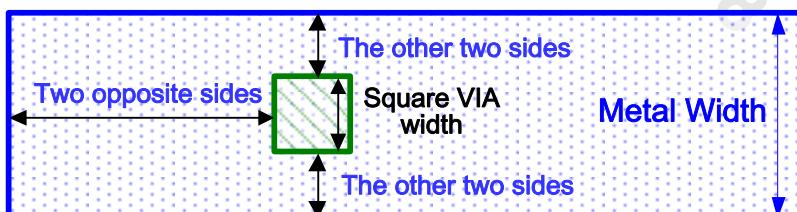
4.5.50.1 VIAYa Enclosure Rule Tabulation

RuleTable.VIAYa.EN.31 (Enclosure of square VIA [width = 0.020 μm])

Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAYa.EN.31.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIAYa.EN.31.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIAYa.EN.31.3.T	0.024 μm ≤ width < 0.028 μm	0.0300 μm	0.0020 μm	
VIAYa.EN.31.4.T	0.028 μm ≤ width < 0.040 μm	0.0300 μm	0.0020 μm	
VIAYa.EN.31.5.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIAYa.EN.31.6	0.060 μm ≤ width < 0.080 μm	0.0250 μm	0.0200 μm	following conditions: 1. VIA3 inside {BLK_M4 AND BLK_M3}
VIAYa.EN.31.6.1.T	0.060 μm ≤ width < 0.080 μm	0.0250 μm	0.0160 μm	
VIAYa.EN.31.7.T	0.080 μm ≤ width < 0.260 μm	0.0200 μm	0.0300 μm	
VIAYa.EN.31.8.T	width ≥ 0.260 μm	0.0600 μm	0.0250 μm	

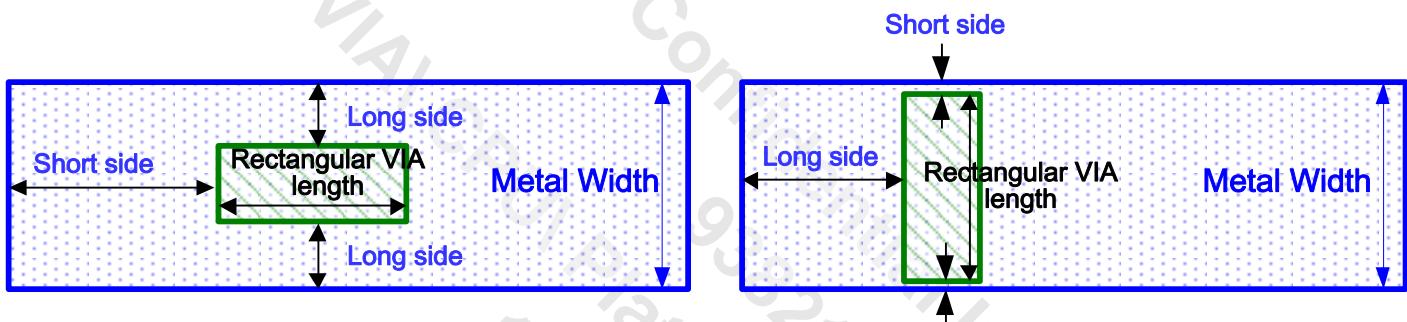
RuleTable.VIAYa.EN.33 (Enclosure of square VIA [width = 0.038 μm])

Rule Number	Metal Width	Two opposite sides	The other two sides	Exception
VIAYa.EN.33.1.T	width < 0.060 μm	0.0590 μm	0.0010 μm	
VIAYa.EN.33.2.T	0.060 μm ≤ width < 0.080 μm	0.0500 μm	0.0110 μm	
VIAYa.EN.33.3.T	0.080 μm ≤ width < 0.100 μm	0.0430 μm	0.0210 μm	
VIAYa.EN.33.4.T	0.100 μm ≤ width < 0.120 μm	0.0430 μm	0.0310 μm	
VIAYa.EN.33.5.T	0.120 μm ≤ width < 0.260 μm	0.0400 μm	0.0400 μm	
VIAYa.EN.33.6.T	width ≥ 0.260 μm	0.0600 μm	0.0500 μm	



RuleTable.VIAYA.EN.32 (Enclosure of rectangular VIA [length = 0.050 μm])

Rule Number	Metal Width	Short side	Long side	Exception
VIAYA.EN.32.1.T	width < 0.022 μm	0.0300 μm	0 μm	
VIAYA.EN.32.2.T	0.022 μm ≤ width < 0.024 μm	0.0300 μm	0.0010 μm	
VIAYA.EN.32.3.T	0.024 μm ≤ width < 0.028 μm	0.0300 μm	0.0020 μm	
VIAYA.EN.32.4.T	0.028 μm ≤ width < 0.040 μm	0.0300 μm	0.0020 μm	
VIAYA.EN.32.5.T	0.040 μm ≤ width < 0.060 μm	0.0300 μm	0.0100 μm	
VIAYA.EN.32.6.T	0.060 μm ≤ width < 0.080 μm	0.0250/0.0050 μm	0.0200/0.0250 μm	
VIAYA.EN.32.7.T	width = 0.080 μm	0.0250/0.0150 μm	0.0200/0.0300 μm	
VIAYA.EN.32.8.T	width > 0.080 μm	0.0250/0.0300 μm	0.0300/0.0250 μm	



Rule No.	Description	Label	Op.	Rule
VIAya.EN.31.1.T	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [width < 0.022 μm] for two opposite sides with the other two sides $\geq 0 \mu\text{m}$		\geq	0.0300
VIAya.EN.31.2.T	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [0.022 $\mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIAya.EN.31.3.T	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [0.024 $\mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAya.EN.31.4.T	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAya.EN.31.5.T	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [0.040 $\mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300
VIAya.EN.31.6	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [0.060 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0200 \mu\text{m}$ (Except following conditions: 1. VIA3 inside {BLK_M4 AND BLK_M3})		\geq	0.0250
VIAya.EN.31.6.1.T	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [0.060 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0160 \mu\text{m}$		\geq	0.0250
VIAya.EN.31.7.T	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [0.080 $\mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0300 \mu\text{m}$		\geq	0.0200
VIAya.EN.31.8.T	Enclosure of square VIAya [width = 0.020 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0250 \mu\text{m}$		\geq	0.0600
VIAya.EN.33.1.T	Enclosure of square VIAya [width = 0.038 μm] by Lower_Metal [width < 0.060 μm] for two opposite sides with the other two sides $\geq 0.0010 \mu\text{m}$		\geq	0.0590
VIAya.EN.33.2.T	Enclosure of square VIAya [width = 0.038 μm] by Lower_Metal [0.060 $\mu\text{m} \leq \text{width} < 0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0110 \mu\text{m}$		\geq	0.0500
VIAya.EN.33.3.T	Enclosure of square VIAya [width = 0.038 μm] by Lower_Metal [0.080 $\mu\text{m} \leq \text{width} < 0.100 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0210 \mu\text{m}$		\geq	0.0430
VIAya.EN.33.4.T	Enclosure of square VIAya [width = 0.038 μm] by Lower_Metal [0.100 $\mu\text{m} \leq \text{width} < 0.120 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0310 \mu\text{m}$		\geq	0.0430
VIAya.EN.33.5.T	Enclosure of square VIAya [width = 0.038 μm] by Lower_Metal [0.120 $\mu\text{m} \leq \text{width} < 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0400 \mu\text{m}$		\geq	0.0400
VIAya.EN.33.6.T	Enclosure of square VIAya [width = 0.038 μm] by Lower_Metal [width $\geq 0.260 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.0500 \mu\text{m}$		\geq	0.0600
VIAya.EN.32.1.T	Short side enclosure of rectangular VIAya [length = 0.050 μm] by Lower_Metal [width < 0.022 μm] with the other two long sides $\geq 0 \mu\text{m}$		\geq	0.0300
VIAya.EN.32.2.T	Short side enclosure of rectangular VIAya [length = 0.050 μm] by Lower_Metal [0.022 $\mu\text{m} \leq \text{width} < 0.024 \mu\text{m}$] with the other two long sides $\geq 0.0010 \mu\text{m}$		\geq	0.0300
VIAya.EN.32.3.T	Short side enclosure of rectangular VIAya [length = 0.050 μm] by Lower_Metal [0.024 $\mu\text{m} \leq \text{width} < 0.028 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAya.EN.32.4.T	Short side enclosure of rectangular VIAya [length = 0.050 μm] by Lower_Metal [0.028 $\mu\text{m} \leq \text{width} < 0.040 \mu\text{m}$] with the other two long sides $\geq 0.0020 \mu\text{m}$		\geq	0.0300
VIAya.EN.32.5.T	Short side enclosure of rectangular VIAya [length = 0.050 μm] by Lower_Metal [0.040 $\mu\text{m} \leq \text{width} < 0.060 \mu\text{m}$] with the other two long sides $\geq 0.0100 \mu\text{m}$		\geq	0.0300

Rule No.	Description	Label	Op.	Rule
VIAya.EN.32.6.T	Short side enclosure of rectangular VIAya [length = 0.050 µm] by Lower_Metal [0.060 µm ≤ width < 0.080 µm] with the other two long sides ≥ 0.0200/0.0250 µm		≥	0.0250/0.0050
VIAya.EN.32.7.T	Short side enclosure of rectangular VIAya [length = 0.050 µm] by Lower_Metal [width = 0.080 µm] with the other two long sides ≥ 0.0200/0.0300 µm		≥	0.0250/0.0150
VIAya.EN.32.8.T	Short side enclosure of rectangular VIAya [length = 0.050 µm] by Lower_Metal [width > 0.080 µm] with the other two long sides ≥ 0.0300/0.0250 µm		≥	0.0250/0.0300

TSMC Confidential Information
VIAI CPU Platform Col., Ltd.
938214
10/05/2018

4.5.51 Mya Layout Rules

- Minimum Pitch (MINP) 0.076 μm can only be drawn in either parallel or perpendicular to PO direction.
 - Data type 340 is used for metal pitch 0.076 μm in perpendicular to core PO direction, or
 - Data type 330 is used for metal pitch 0.076 μm in parallel to core PO direction
- NonMinimum Pitch (NMINP) direction is perpendicular to Minimum pitch (MINP) direction.

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5. DRC checks DMya_O as well as Mya in this section.

Rule No.	Description	Label	Op.	Rule
Mya.W.1	Width	W1	\geq	0.0380
Mya.W.1.1	Width [MINP direction]	W1A	=	0.0380, 0.0400, 0.0580, 0.0600, 0.0760, 0.0800, 0.1140, 0.1200, \geq 0.1520
Mya.W.1.3	Width [NMINP direction] (Except following conditions: 1. M4 interact BLK_M4)	W1C	=	0.0760, 0.0800, 0.1140, 0.1200, \geq 0.1520
Mya.W.1.4	Width of DMya_O [MINP direction]	W1D	=	0.0580, 0.1900
Mya.W.2	Width of 45-degree bent Mya (Except SEALRING_ALL)	W2	\geq	0.4000
Mya.W.3	Maximum width (Except SEALRING_ALL)	W3	\leq	2
Mya.W.5	Mya branch width connected to Mya plate with length > 0.400 μm (L) and width > 0.400 μm (W)	W5	\geq	0.0760
Mya.W.6	Concave corner to concave corner width	W6	\geq	0.0890
Mya.S.1	Space	S1	\geq	0.0380
Mya.S.1.1	Space of DMya_O [MINP direction]	S1A	\geq	0.0760
Mya.S.2.1.1	Space of Mya [width = 0.038 μm in MINP direction] to Mya [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.076 μm] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape [0.040 μm < edge length < 0.201 μm between 2 consecutive 90-270 degree corners, corresponding width = 0.076/0.080 μm in NMINP direction between 2 opposite 0.040 μm < edge length < 0.201 μm, not including T-shape]	SM	=	0.0380, 0.0570, 0.0660, 0.0760, 0.0950, \geq 0.1140
Mya.S.2.1.2	Space of Mya [width = 0.038 μm in MINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0380, \geq 0.1140
Mya.S.2.2.1	Space of Mya [width = 0.058 μm in MINP direction] in MINP direction [PRL > -0.076 μm] DRC checks space of Mya drawing pattern only	SM	=	0.0560, 0.0940, \geq 0.1140
Mya.S.2.2.2	Space of Mya [width = 0.058 μm in MINP direction] to Mya [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.076 μm] DRC checks space of Mya drawing pattern only	SM	=	0.0470, 0.0560, 0.0660, 0.0940, \geq 0.1140
Mya.S.2.2.3	Space of DMya_O [width = 0.058 μm in MINP direction] to Mya [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0760, \geq 0.1140
Mya.S.2.3.1	Space of Mya [width = 0.076 μm] to Mya [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.076 μm] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	=	0.0470, 0.0570, 0.0760, 0.0950, \geq 0.1140

Rule No.	Description	Label	Op.	Rule
Mya.S.2.3.2	Space of Mya [width = 0.076 μm in MINP direction] to Mya [width = 0.038 μm in MINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0570, 0.0950, ≥ 0.1140
Mya.S.2.3.2.1	Space of Mya [width = 0.076 μm in MINP direction] to Mya [width = 0.058 μm in MINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0470, ≥ 0.1140
Mya.S.2.3.3	Space of Mya [width = 0.076 μm in MINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0760, ≥ 0.1140
Mya.S.2.4.1	Space of Mya edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.038 μm] [at least one Mya width = 0.114 μm in MINP direction] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	=	0.0760, ≥ 0.1140
Mya.S.2.4.2	Space of Mya edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.038 μm] [both Mya width = 0.114 μm in MINP direction] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	≥	0.1140
Mya.S.2.4.3	Space of Mya edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.038 μm] [one Mya width = 0.114 μm, the other Mya width = 0.076 μm, in MINP direction] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	≥	0.1140
Mya.S.2.4.4	Space of Mya [width ≥ 0.080 μm in MINP direction] to Mya [width > 0.040 μm in MINP direction] in MINP direction [PRL > -0.038 μm] (Except following conditions: 1. Space between Z-/Z-shape) Definition of Z-shape follows Mya.S.2.1.1	SM	≥	0.0560
Mya.S.2.4.5	Space of Mya [width ≥ 0.080 μm in MINP direction] to Mya [width > 0.060 μm in MINP direction] in MINP direction [PRL > -0.038 μm] (Except following conditions: 1. Space between Z-/Z-shape) Definition of Z-shape follows Mya.S.2.1.1	SM	≥	0.0760
Mya.S.2.11.1	Space of Mya [width = 0.040 μm in MINP direction] to Mya [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.080 μm] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	=	0.0400, 0.0600, 0.0700, 0.0800, 0.1000, ≥ 0.1200
Mya.S.2.11.2	Space of Mya [width = 0.040 μm in MINP direction] in MINP direction [PRL > -0.080 μm]	SM	=	0.0400, ≥ 0.1200
Mya.S.2.12.1	Space of Mya [width = 0.060 μm in MINP direction] to Mya [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.080 μm] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	=	0.0600, 0.0700, 0.1000, ≥ 0.1200
Mya.S.2.12.2	Space of Mya [width = 0.060 μm in MINP direction] in MINP direction [PRL > -0.080 μm]	SM	=	0.0600, 0.1000, ≥ 0.1200
Mya.S.2.12.3	Space of Mya [width = 0.060 μm in MINP direction] to Mya [width = 0.080 μm in MINP direction] in MINP direction [PRL > -0.080 μm]	SM	≥	0.1200
Mya.S.2.12.4	Space of Mya [width = 0.060 μm in MINP direction] to Mya [width = 0.040 μm in MINP direction] in MINP direction [PRL > -0.080 μm]	SM	=	0.0700, ≥ 0.1200

Rule No.	Description	Label	Op.	Rule
Mya.S.2.13.1	Space of Mya [width = 0.080 µm in MINP direction] to Mya [with edge length > 0.080 µm in NMNIP direction] in MINP direction [PRL > -0.080 µm] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	=	0.0600, 0.0800, 0.1000, ≥ 0.1200
Mya.S.2.13.2	Space of Mya [width = 0.080 µm in MINP direction] in MINP direction [PRL > -0.080 µm]	SM	=	0.0800, ≥ 0.1200
Mya.S.2.13.3	Space of Mya [width = 0.080 µm in MINP direction] to Mya [width = 0.040 µm in MINP direction] in MINP direction [PRL > -0.080 µm]	SM	=	0.0600, 0.1000, ≥ 0.1200
Mya.S.2.14.1	Space of Mya edge [edge length > 0.080 µm in NMNIP direction] in MINP direction [PRL > -0.040 µm] [at least one Mya width = 0.120 µm in MINP direction] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	=	0.0800, ≥ 0.1200
Mya.S.2.14.2	Space of Mya edge [edge length > 0.080 µm in NMNIP direction] in MINP direction [PRL > -0.040 µm] [one Mya width = 0.120 µm, the other one Mya width = 0.038 µm or ≥ 0.058 µm in MINP direction] (Except following conditions: 1. adjacent edge of Z-shape corner) Definition of Z-shape follows Mya.S.2.1.1	SM	≥	0.1200
Mya.S.3.1	Space of Mya edge [edge length > 0.080 µm in MINP direction] in NMNIP direction [PRL > -0.038 µm] [at least one Mya width = 0.114 µm in NMNIP direction]	SN	≥	0.1140
Mya.S.3.11.1	Space of Mya [width = 0.080 µm in NMNIP direction] to Mya [with edge length > 0.080 µm in MINP direction] in NMNIP direction [PRL > -0.080 µm]	SN	=	0.0800, ≥ 0.1200
Mya.S.3.11.2	Space of Mya [width = 0.120 µm in NMNIP direction] to Mya [with edge length > 0.080 µm in MINP direction] in NMNIP direction [PRL > -0.040 µm]	SN	≥	0.1200
Mya.S.5.1	Space of Mya edge [edge length > 0.080 µm in MINP direction] in NMNIP direction [PRL > -0.076 µm] [at least one Mya width = 0.076 µm in NMNIP direction]	SN	=	0.0760, ≥ 0.1140
Mya.S.5.4	Space of Mya [width = 0.038 µm in MINP direction] to Mya [width = 0.040/0.060 µm in MINP direction] [PRL > -0.300 µm]	S5D	≥	0.3000
Mya.S.5.4.1	Space of Mya [width = 0.058 µm in MINP direction] to Mya [width = 0.040 µm in MINP direction] [PRL > -0.300 µm] DRC checks space of Mya drawing pattern only	S5D	≥	0.3000
Mya.S.5.4.1.1	Space of DMya_O [width = 0.058 µm in MINP direction] to Mya [width = 0.040 µm in MINP direction] [PRL > -0.120 µm]	S5D	≥	0.1200
Mya.S.5.4.2	Space of Mya [width = 0.076 µm in MINP direction] to Mya [width = 0.080 µm in MINP direction] in NMNIP direction [PRL > -0.300 µm]	S5D	≥	0.3000
Mya.S.6	Corner projected space of Mya [-0.076 µm < PRL ≤ 0 µm] (Except following conditions: 1. both two corners from Line-end or Z-shape) Definition of Line-end [both width ≤ 0.060 µm between 2 consecutive 90-90 degree corners] Definition of Z-shape follows Mya.S.2.1.1	S6	≥	0.0760
Mya.S.6.1	Corner projected space in NMNIP direction [-0.038 µm < PRL ≤ 0 µm in MINP direction]	S6	≥	0.0760
Mya.S.6.2	Corner projected space of Mya [width ≥ 0.240 µm, -0.160 µm < PRL ≤ 0 µm]	S6	≥	0.1600
Mya.S.8	Space of Mya edge [edge length > 0.080 µm in NMNIP direction] in MINP direction [PRL > 0.080 µm] [at least one Mya width ≥ 0.152 µm in MINP direction]	SM	≥	0.1140

Rule No.	Description	Label	Op.	Rule
Mya.S.8.0.1	Space of Mya edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.030 μm] [at least one Mya width \geq 0.152 μm in MINP direction] (Except following conditions: 1. Space between Z-/Z-shape, Z-shape/Mya [width < 0.152 μm in MINP direction]) Definition of Z-shape follows Mya.S.2.1.1	SM	\geq	0.0760
Mya.S.8.0.2	Space of Mya edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > 0 μm] [at least one Mya width \geq 0.152 μm in MINP direction and enclosure of Lower_VIA < 0.030 μm]	SM	\geq	0.1140
Mya.S.8.1	Space of Mya edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > 0.080 μm] [at least one Mya width \geq 0.152 μm in NMINP direction]	SN	\geq	0.1300
Mya.S.8.1.1	Space of Mya edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > -0.030 μm] [at least one Mya width \geq 0.152 μm in NMINP direction]	SN	\geq	0.0760
Mya.S.8.1.2	Space of Mya edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > 0 μm] [at least one Mya width \geq 0.152 μm in NMINP direction and enclosure of Lower_VIA < 0.030 μm]	SN	\geq	0.1140
Mya.S.11	Space of Mya edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > 0.120 μm] [at least one Mya width \geq 0.201 μm in MINP direction] (Except following conditions: 1. adjacent edge of Z-shape corner, 2. Space to DMya_O) Definition of Z-shape follows Mya.S.2.1.1	SM	\geq	0.1450
Mya.S.11.1	Space of Mya edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > 0.080 μm] [at least one Mya width \geq 0.190 μm in NMINP direction] (Except following conditions: 1. Space to DMya_O)	SN	\geq	0.1500
Mya.S.11.2	Space to Mya [width \geq 0.231 μm , PRL > 0.120 μm]	SM/SN	\geq	0.1600
Mya.S.11.3	Space to Mya [width \geq 0.280 μm , PRL > 0.160 μm]	SM/SN	\geq	0.2000
Mya.S.15	Space to Mya [width > 1.350 μm , PRL > 1.350 μm] (Except SEALRING_ALL)	SM/SN	\geq	0.4500
Mya.S.15®	Recommended space [at least one metal line width > 1.350 μm]	SN	\geq	0.4500
Mya.S.16	Space to Mya line-end [edge length = 0.038 μm between 2 consecutive 90-90 degree corners, PRL > -0.038 μm] in NMINP direction	S16	\geq	0.0900
Mya.S.16.0	Space to Mya line-end [edge length = 0.058 μm between 2 consecutive 90-90 degree corners, PRL > -0.058 μm] in NMINP direction	S16	\geq	0.0900
Mya.S.16.1	Space to Mya line-end [edge length = 0.076 μm between 2 consecutive 90-90 degree corners, PRL > -0.076 μm] in NMINP direction	S16A	\geq	0.0760
Mya.S.16.2	Space to Mya line-end [edge length = 0.076 μm between 2 consecutive 90-90 degree corners, PRL > -0.076 μm , both adjacent edge length > 0.090 μm] in MINP direction	S16B	\geq	0.1000

Rule No.	Description	Label	Op.	Rule
Mya.S.16.4	<p>Space of Mya to Checked_Mya_Line_End in NMINP direction [PRL > -0.038 μm]</p> <p>Definition of Mya_Group: $\{\{\text{Mya} [\text{width} \leq 0.040 \mu\text{m}] \text{ SIZING up/down } 0.020 \mu\text{m in MINP direction}\}$ $\{\{\text{SIZING } -0.140 \mu\text{m in MINP direction}\} \text{ SIZING down/up } 0.050 \mu\text{m in NMINP direction}\}$</p> <p>Definition of Checked_VIAya: $\{\text{VIAya-1 inside }\{\text{Mya_Group SIZING } 0.100 \mu\text{m in NMINP direction}\}\}$</p> <p>Definition of Checked_Mya_Line_End: $\{\text{Mya line_end enclosure of square Checked_VIAya } < 0.050 \mu\text{m}\}$</p> <p>(Except following conditions: 1. From Checked_Mya_Line_End edge corner to form two region-A (width in MINP/NMINP direction is 0.280 μm /0.085 μm), and neighboring Mya extension to region-A $\geq 0 \mu\text{m}$)</p>	S16D	\geq	0.1350
Mya.S.17	Space to Mya line-end [edge length = 0.040 μm between 2 consecutive 90-90 degree corners, PRL > -0.040 μm] in NMINP direction	S17	\geq	0.0900
Mya.S.17.1	Space to Mya line-end [edge length = 0.060 μm between 2 consecutive 90-90 degree corners, PRL > -0.040 μm] in NMINP direction	S17	\geq	0.0900
Mya.S.17.2	Space to Mya line-end [edge length = 0.080 μm between 2 consecutive 90-90 degree corners, PRL > -0.080 μm] in NMINP direction	S17B	\geq	0.0800
Mya.S.17.3	Space to Mya line-end [edge length = 0.080 μm between 2 consecutive 90-90 degree corners, PRL > -0.080 μm] in MINP direction	S17C	\geq	0.1000
Mya.S.18	Space to 45-degree bent Mya [PRL > 0 μm] (Except SEALRING_ALL)	S18	\geq	0.4000
Mya.S.18.1	Space to 45-degree bent Mya (Except SEALRING_ALL)	S18A	\geq	0.1400
Mya.S.19	Space to VIAya-1 or VIAy [maximum delta V > 0.96V]	S19	\geq	0.0460
Mya.S.19.1	Space to VIAya-1 or VIAy [maximum delta V > 1.32V] (1.2V + 10%)	S19	\geq	0.0600
Mya.S.19.1.1	Space to VIAya-1 or VIAy [maximum delta V > 1.98V] (1.8V + 10%)	S19	\geq	0.0800
Mya.S.20	Space to Mya [maximum delta V > 1.98V] (1.8V + 10%)	S20	\geq	0.0460
Mya.S.20.1	Space to Mya [maximum delta V > 2.75V] (2.5V + 10%)	S20	\geq	0.0800

Rule No.	Description	Label	Op.	Rule
Mya.S.22	<p>Space to the edge of concave corner in MINP direction (Except following conditions: 1. Edge length between 2 concave corner < 0.114 μm 2. Either one edge length of concave corner ≤ 0.040 μm 3. 45-degree Mya)</p> <p>DRC flags Mya overlap Concave_Mya_Area Definition of Concave_Mya_Area: A rectangle [0.114 μm x 0.200 μm] abut both edge of Mya concave corner</p>	S22	≥	0.1140
Mya.S.27	<p>Forbidden space of Mya in MINP direction [PRL > 0 μm] [one side is Mya [width = 0.038 μm and one side space = 0.038 μm (W1)] the other side is Mya [width < 0.076 μm (W2)]] (Except following conditions: 1. both side of Mya [width < 0.076 μm (W2)] to Mya space > 0.095 μm)</p> <p>DRC checks space of Mya drawing pattern only</p>	S27	=	0.1150~0.1890
Mya.S.27.1	<p>Forbidden space of Mya in MINP direction [PRL > 0 μm] [one side is My [width = 0.040 μm and one side space = 0.040 μm (W1)] the other side is My [width < 0.080 μm (W2)]] (Except following conditions: 1. both side of Mya [width < 0.080 μm (W2)] to Mya space > 0.099 μm)</p> <p>DRC checks space of Mya drawing pattern only</p>	S27A	=	0.1300~0.1790
Mya.EN.0	<p>1. Enclosure of square VIAya-1 is defined by one of Mya.EN.1 or Mya.EN.1.0 or Mya.EN.1.1 or Mya.EN.1.3, Mya.EN.1.11.1, Mya.EN.1.11.2, Mya.EN.1.11.3 2. Enclosure of rectangular VIAya-1 is defined by one of Mya.EN.4 or Mya.EN.5 or Mya.EN.5.1, Mya.EN.5.11.1, Mya.EN.5.11.2, Mya.EN.5.11.4</p> <p>Note: 1. DRC only checks the VIAya-1 which overlaps the metal width of corresponding rule 2. DRC checks Mya.EN.1.3, Mya.EN.1.11.3, Mya.EN.1.1, Mya.EN.1.11.1, Mya.EN.1 in sequence</p>			
Mya.EN.1	Enclosure of square VIAya-1 [width = 0.020 μm] by Mya [width = 0.038 μm] for two opposite sides with the other two sides ≥ 0.035 μm	EN1	≥	0.0090
Mya.EN.1.0	Enclosure of square VIAya-1 [width = 0.020 μm] by Mya [width = 0.058 μm] for two opposite sides with the other two sides ≥ 0.035 μm (Except following conditions: 1. VIA3 inside {BLK_M4 AND BLK_M3})	EN1	≥	0.0190
Mya.EN.1.0.1	Enclosure of square VIA3 [width = 0.020 μm] by M4 [width = 0.058 μm] for two opposite sides with the other two sides ≥ 0.035 μm	EN1	≥	0.0060
Mya.EN.1.1	Enclosure of square VIAya-1 [width = 0.020 μm] by Mya [width = 0.076 μm] for two opposite sides with the other two sides ≥ 0.020 μm	EN1A	≥	0.0280
Mya.EN.1.3	Enclosure of square VIAya-1 [width = 0.020 μm] by Mya [width ≥ 0.114 μm] for all sides	EN1C	≥	0.0280
Mya.EN.1.11.1	Enclosure of square VIAya-1 [width = 0.020 μm] by Mya [width = 0.040 μm] for two opposite sides with the other two sides ≥ 0.035 μm	EN1K1	≥	0.0100
Mya.EN.1.11.2	Enclosure of square VIAya-1 [width = 0.020 μm] by Mya [width = 0.060 μm] for two opposite sides with the other two sides ≥ 0.035 μm	EN1K2	≥	0.0200
Mya.EN.1.11.3	Enclosure of square VIAya-1 [width = 0.020 μm] by Mya [width = 0.080 μm] for two opposite sides with the other two sides ≥ 0.020 μm	EN1K3	≥	0.0300
Mya.EN.2	Enclosure of square VIAya-1 [width = 0.038 μm] by Mya [width = 0.038 μm] for two opposite sides with the other two sides ≥ 0.061 μm	EN2	≥	0
Mya.EN.2.0	Enclosure of square VIAya-1 [width = 0.038 μm] by Mya [width = 0.058 μm] for two opposite sides with the other two sides ≥ 0.061 μm	EN2	≥	0.0100

Rule No.	Description	Label	Op.	Rule
Mya.EN.2.1	Enclosure of square VIAYA-1 [width = 0.038 μm] by Mya [width = 0.076 μm] for two opposite sides with the other two sides ≥ 0.043 μm	EN2A	≥	0.0190
Mya.EN.2.3	Enclosure of square VIAYA-1 [width = 0.038 μm] by Mya [width ≥ 0.114 μm] for two opposite sides with the other two sides ≥ 0.040 μm	EN2C	≥	0.0380
Mya.EN.2.11.1	Enclosure of square VIAYA-1 [width = 0.038 μm] by Mya [width = 0.040 μm] for two opposite sides with the other two sides ≥ 0.061 μm	EN2K1	≥	0.0010
Mya.EN.2.11.2	Enclosure of square VIAYA-1 [width = 0.038 μm] by Mya [width = 0.060 μm] for two opposite sides with the other two sides ≥ 0.061 μm	EN2K2	≥	0.0110
Mya.EN.2.11.3	Enclosure of square VIAYA-1 [width = 0.038 μm] by Mya [width = 0.080 μm] for two opposite sides with the other two sides ≥ 0.043 μm	EN2K3	≥	0.0210
Mya.EN.4	Enclosure of short side of rectangular VIAYA-1 by Mya [width = 0.038 μm] with the other two long side enclosure ≥ 0.009 μm	EN4	≥	0.0400
Mya.EN.4.1	Enclosure of short side of rectangular VIAYA-1 by Mya [width = 0.058 μm] with the other two long side enclosure ≥ 0.019 μm	EN4A	≥	0.0400
Mya.EN.5	Enclosure of short side of rectangular VIAYA-1 by Mya [width ≥ 0.076 μm] with the other two long side enclosure ≥ 0.028 μm	EN5	≥	0.0200
Mya.EN.5.1	Enclosure of short side of rectangular VIAYA-1 by Mya [width = 0.076 μm] with the other two long side enclosure ≥ 0.040 μm	EN5A	≥	0.0130
Mya.EN.5.11.1	Enclosure of short side of rectangular VIAYA-1 by Mya [width = 0.040 μm] with the other two long side enclosure ≥ 0.010 μm	EN5K1	≥	0.0400
Mya.EN.5.11.2	Enclosure of short side of rectangular VIAYA-1 by Mya [width = 0.060 μm] with the other two long side enclosure ≥ 0.020 μm	EN5K2	≥	0.0400
Mya.EN.5.11.4	Enclosure of short side of rectangular VIAYA-1 by Mya [width = 0.080 μm] with the other two long side enclosure ≥ 0.040 μm	EN5K4	≥	0.0150
Mya.EN.10	Enclosure of square or rectangular VIAYA-1 by Mya edge [between 2 consecutive 90-270 degree corners, length < 0.152 μm]	EN10	≥	0.0300
Mya.EN.10.1	Enclosure of square or rectangular VIAYA-1 by Mya for two opposite sides with the other side enclosure < 0.038 μm [edge length < 0.152 μm between 2 consecutive 90-270 degree corners]	EN10A	≥	0.0380
Mya.L.1	Length of 45-degree bent Mya (minimum edge length) (Except SEALRING_ALL)	L1	≥	0.9100
Mya.L.3	Edge length with adjacent edge [length < 0.090 μm]	L3	≥	0.1000
Mya.L.3.1	Edge length with adjacent edge [length < 0.038 μm]	L3	≥	0.1140
Mya.L.3.2	Edge length with adjacent line-end edge [length < 0.060 μm (L), between 2 consecutive 90-90 degree corners]	L3B	≥	0.1600
Mya.L.3.3	Edge length with adjacent line-end edge [length < 0.085 μm (L), between 2 consecutive 90-90 degree corners]	L3B	≥	0.1100
Mya.L.4	U-shape edge length [between 2 consecutive 270-270 degree corners]	L4	≥	0.0760
Mya.L.5	Edge length [between 2 consecutive 90-270 degree corners]	L5	≥	0.0190
Mya.L.6	Length of Mya branch [width < 0.270 μm] with one square VIAYA-1/VIAY within the distance ≤ 1.063 μm (L6) from Mya plate [both width (W) and length (L) > 0.400 μm] (DRC flags branch that can't enclose a 0.076 μm X 1.063 μm orthogonal rectangle.)	L6	≥	1.063
Mya.L.6.1	Length of Mya branch [width < 0.270 μm] with one square VIAYA-1/VIAY within the distance ≤ 3.063 μm (L6) from Mya plate [both width (W) and length (L) > 0.540 μm] (DRC flags branch that can't enclose a 0.076 μm X 3.063 μm orthogonal rectangle.)	L6	≥	3.063
Mya.L.6.2	Length of Mya branch [width < 0.270 μm] with one square VIAYA-1/VIAY within the distance ≤ 5.063 μm (L6) from Mya plate [both width (W) and length (L) > 1 μm] (DRC flags branch that can't enclose a 0.076 μm X 5.063 μm orthogonal rectangle.)	L6	≥	5.063

Rule No.	Description	Label	Op.	Rule
Mya.L.7	Mya edge length (L7) between consecutive 90-270 degree corners with adjacent edge in line-end [width < 0.076 μm] and another adjacent edge > 0.070 μm (Except following conditions: 1. edge length (L7) \leq 0.070 μm)	L7	\geq	0.2400
Mya.A.1	Area	A1	\geq	0.01500
Mya.A.1®	Recommended area (Except DMya_O)	A1	\geq	0.02200
Mya.A.3	Area [with all of edge lengths < 0.117 μm] (Except following conditions: 1. a pattern filling 0.050 μm x 0.130 μm tile)	A3	\geq	0.04000
Mya.A.4	Enclosed area	A4	\geq	0.18200
Mya.DN.1.1	Minimum All_metal density in window 50 μm x 50 μm , stepping 25 μm (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	10%
Mya.DN.1.2	Minimum All_metal density in window 50 μm x 50 μm , stepping 25 μm [3 μm x 3 μm empty area exists in the window] (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	25%
Mya.DN.2	Maximum metal density in window 50 μm x 50 μm , stepping 25 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, DMya, DMya_O)		\leq	65%
Mya.DN.2.3	Maximum {{Mya OR DMya_O} OR DMya} density in window 50 μm x 50 μm , stepping 25 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	75%
Mya.DN.3.1	The metal density difference between any two neighboring checking windows including DMnEXCL [window 180 μm x 180 μm , stepping 180 μm] (Except TCDDMY_Mn, ICOVL_SINGLE)		\leq	50%
Mya.DN.6.1	Metal density [window 9 μm x 9 μm , stepping 4.5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. the maximum area of the merged low density windows [density < 1%] \leq 5184 μm^2 , while the merged low density windows width is > 27 μm , 2. the maximum area of the merged low density windows [density < 1%] \leq 14580 μm^2 , 3. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	1%
Mya.DN.7	It is not allowed to have local density < 5% of all 3 consecutive metal (Mya, My, and My+1) over any 27 μm x 27 μm (stepping 13.5 μm), i.e. it is allowed for either one of Mya, My, or My+1 to have a local density \geq 5% (The metal layers include Mya/My/My+1 and dummy metals for ELK film) (Except ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc, 2. TCDDMY_Mn (assume 45% pattern density INSIDE TCDDMY_Mn))			
Mya.DN.5.1®	Recommended minimum metal density in window 25 μm x 25 μm , stepping 12.5 μm (Except LOGO, INDDMY, TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	30%

Rule No.	Description	Label	Op.	Rule
Mya.DN.6.1®	Recommend metal density for IP level [window 10 μm x 10 μm, stepping 5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. the maximum area of the merged low density windows [density < 1%] ≤ 1600 μm ² , while the merged low density windows width is > 30 μm, 2. the maximum area of the merged low density windows [density < 1%] ≤ 4500 μm ² , 3. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
Mya.DN.8®	Recommended maximum metal density in window 25 μm x 25 μm, stepping 12.5 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	60%
Mya.R.1 ^U	Mya line-end must be rectangular. Other shapes are not allowed			
Mya.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
Mya.R.4®	Recommended maximum stacked M1, Mx, Mxa and Mya layers of high density area [density > 70% in window 800 μm x 800 μm, stepping 80 μm]		≤	4
Mya.R.6	Datatype 330 and 340 exist on the same metal layer at the same time is not allowed			
Mya.R.6.1	Same datatype (330 or 340) in both Mya and Mya-1 at the same time is not allowed Same datatype (331 or 341) in both Mya and Mya-1 at the same time is not allowed; Same datatype (337 or 347) in both Mya and Mya-1 at the same time is not allowed.			
Mya.R.6.2	Consecutive Mx datatype (255 or 256 or 252 or 253 or 258 or 259) and Mya datatype (330 or 331 or 337) exist at the same time is not allowed; Consecutive Mx datatype (275 or 276 or 272 or 273 or 278 or 279) and Mya datatype (340 or 341 or 347) exist at the same time is not allowed; Consecutive Mxa datatype (295 or 296 or 292 or 293 or 298 or 299) and Mya datatype (330 or 331 or 337) exist at the same time is not allowed; Consecutive Mxa datatype (315 or 316 or 312 or 313 or 318 or 319) and Mya datatype (340 or 341 or 347) exist at the same time is not allowed.			
Mya.R.7	Mya must follow either one of the conditions. 1. {Checked_Mya AND Dense_Region_Mya} must be projected [PRL ≥ 0 μm] to another two {Mya AND Dense_Region_Mya} at both sides in MINP direction, or 2. There is no other {Mya OVERLAP Iso_Region_Mya} and simultaneously {Checked_Mya AND Iso_Region_Mya} can't be projected [PRL ≥ 0 μm] to {Checked_Mya AND Iso_Region_Mya} at four sides. Definition of Checked_Lower_VIA: {Lower_VIA [enclosure by Mya < 0.010 μm and enclosure by Lower_Metal < 0.050 μm at the same time] NOT INSIDE {BLK_M4 AND BLK_M3}} Definition of Checked_Mya: {Mya OVERLAP Checked_Lower_VIA} Definition of Dense_Region_Mya: A rectangle formed by Checked_Lower_VIA edge expanding 0.048 μm in MINP direction Definition of Iso_Region_Mya: A rectangle formed by Checked_Lower_VIA edge expanding 0.085 μm in MINP direction and expanding 0.300 μm in NMINP direction DRC checks Mya drawing pattern only			

Rule No.	Description	Label	Op.	Rule
Mya.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of Mya space to Mya or VIAya-1 or VIAya is < 0.360 μm			
Mya.R.17	DMya is a must in chip level.			

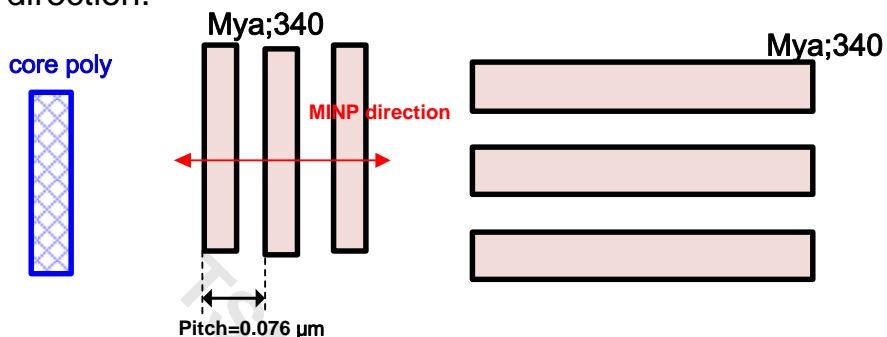
Table Notes:

- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

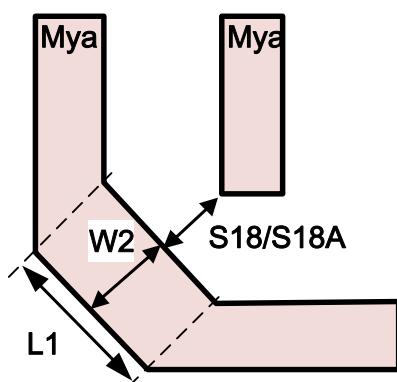
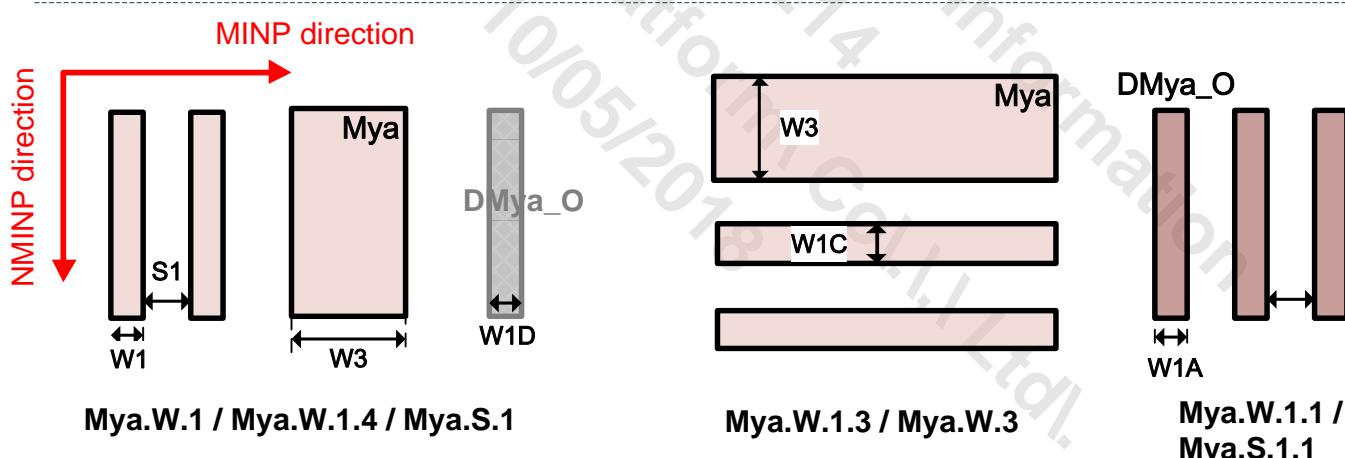
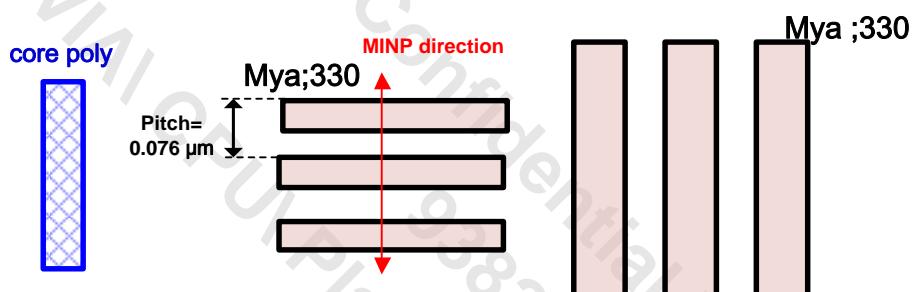
TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

Mya

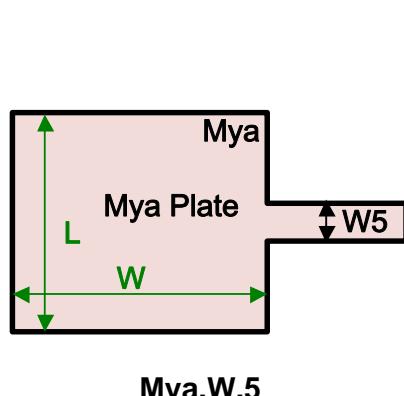
Data type 340 is used for metal pitch 0.076 μm in perpendicular to core PO direction.



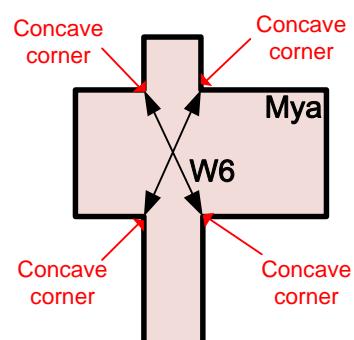
- Data type 330 is used for metal pitch 0.076 μm in parallel to core PO direction.



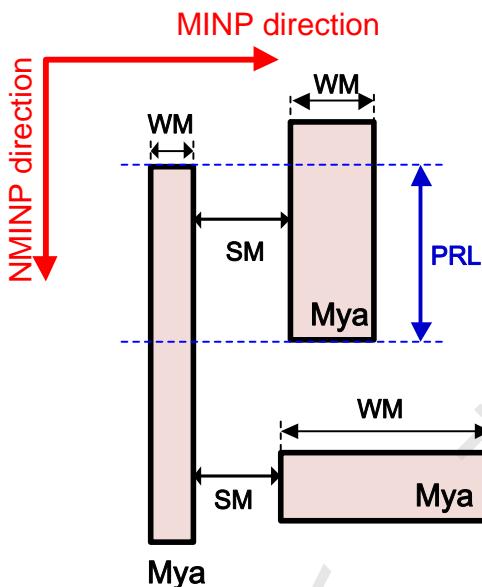
Mya.W.2 / Mya.S.18 /
Mya.S.18.1 / Mya.L.1



Mya.W.5



Mva.W.6



Mya.S.2.1.1 / Mya.S.2.1.2 / Mya.S.2.2.1 /
 Mya.S.2.2.2 / Mya.S.2.2.3 / Mya.S.2.3.1 /
 Mya.S.2.3.2 / Mya.S.2.3.2.1 / Mya.S.2.3.3 /
 Mya.S.2.4.1 / Mya.S.2.4.2 / Mya.S.2.4.3 /
 Mya.S.2.11.1 / Mya.S.2.11.2 / Mya.S.2.12.1 /
 Mya.S.2.12.2 / Mya.S.2.12.3 / Mya.S.2.12.4 /
 Mya.S.2.13.1 / Mya.S.2.13.2 / Mya.S.2.13.3 /
 Mya.S.2.14.1 / Mya.S.2.14.2 / Mya.S.8 / Mya.S.11 /
 Mya.S.11.2 / Mya.S.11.3 / Mya.S.15/ Mya.S.15®

	Width / Space Table (unit: μm)														
MINP Width (WM)	0.038	0.040	0.058	0.060	0.076	0.080	0.114	0.120	≥ 0.152	≥ 0.201	≥ 0.231	≥ 0.280	> 1.350	≥ 0.038	≥ 0.240
PRL	> -0.076	> -0.080	> -0.076	> -0.080	> -0.076	> -0.080	> -0.038	> -0.080	> 0.080	> 0.120	> 0.120	> 0.160	> 1.350	$-0.076 - 0$	$-0.160 - 0$
Space (SM)	0.038	0.040	0.047	0.061	0.047	0.060	0.076	0.080	≥ 0.114	≥ 0.145	≥ 0.160	≥ 0.200	≥ 0.450	Corner projected space ≥ 0.076	Corner projected space ≥ 0.160
	0.057	0.060	0.056	0.070	0.057	0.080	0.114	≥ 0.120							
	0.066	0.070	0.066	0.100	0.076	0.100									
	0.076	0.080	0.094	≥ 0.120	0.095	≥ 0.120									
	0.095	0.100	≥ 0.114		≥ 0.114										
	≥ 0.114	≥ 0.120													
Related Rule	Mya.S.2.1.1 ^{#1} Mya.S.2.1.2	Mya.S.2.11.1 ^{#1} Mya.S.2.11.2	Mya.S.2.2.1 Mya.S.2.2.2	Mya.S.2.12.1 ^{#1} Mya.S.2.12.2	Mya.S.2.3.1 ^{#1} Mya.S.2.3.2	Mya.S.2.13.1 ^{#1} Mya.S.2.13.2	Mya.S.2.4.1 ^{#1} Mya.S.2.4.2 ^{#1} Mya.S.2.4.3 ^{#1}	Mya.S.2.14.1 ^{#1} Mya.S.2.14.2	Mya.S.8 ^{#2}	Mya.S.11 ^{#2}	Mya.S.11.2	Mya.S.11.3	Mya.S.15	Mya.S.6	Mya.S.6.2

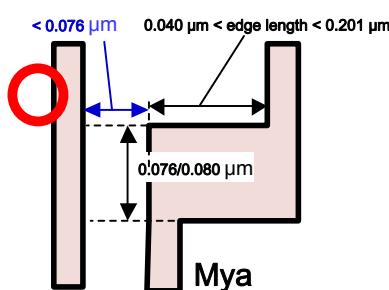
Note:

#1: Except adjacent edge of Z-shape corner

#2: Except line-end [edge length $\leq 0.080 \mu\text{m}$] space $\geq 0.100 \mu\text{m}$

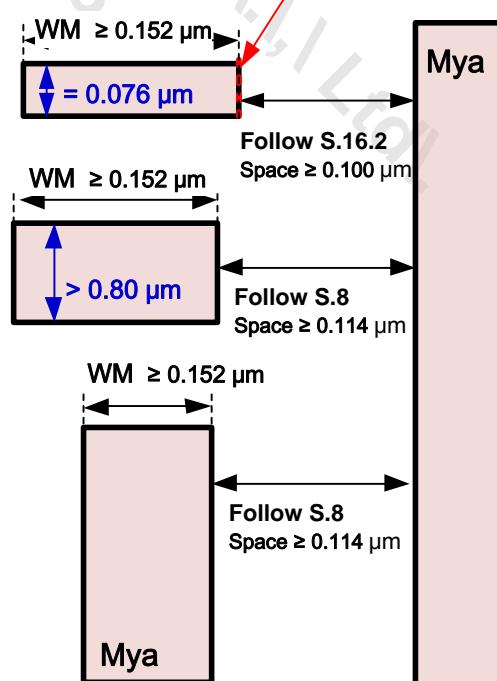
#3: Space of Mya [width = 0.038/0.076/0.114 μm] to Mya [width 0.040/0.080 μm] follows Mya.S.5.4

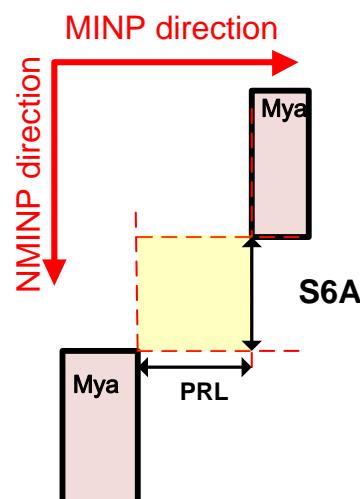
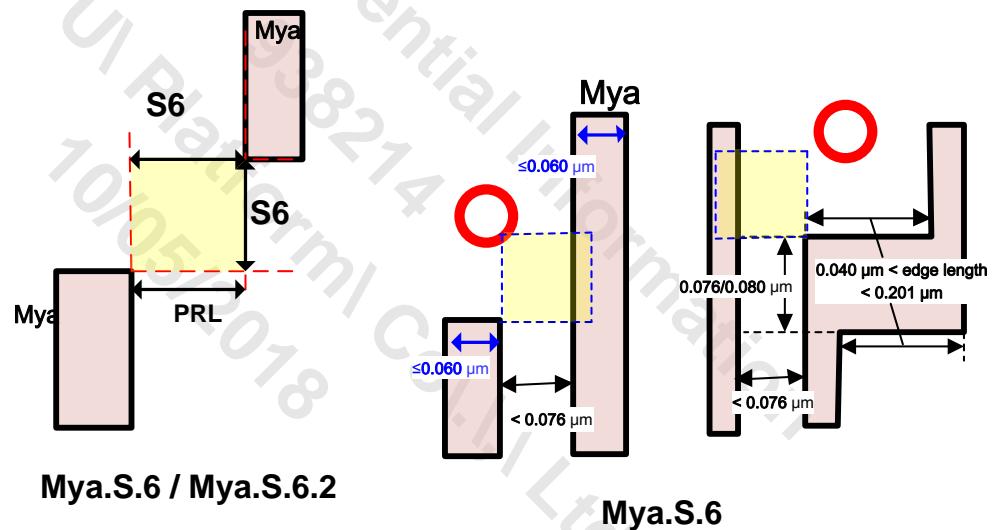
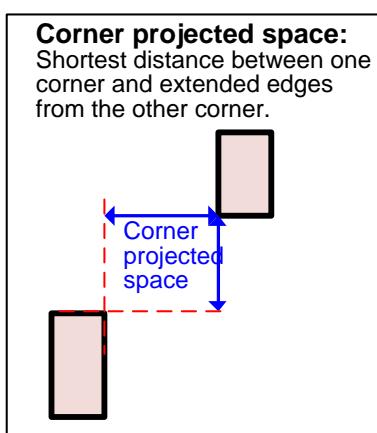
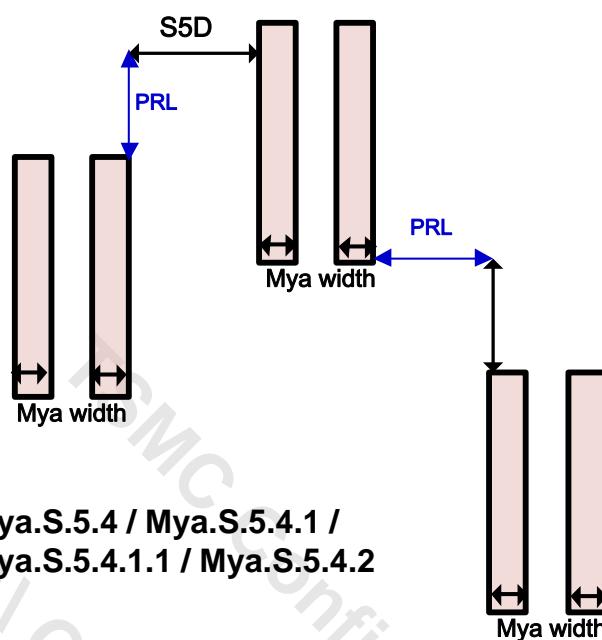
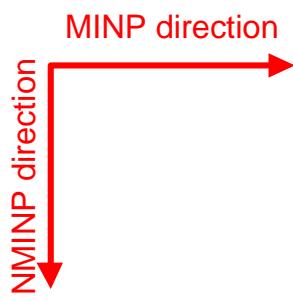
Note #1

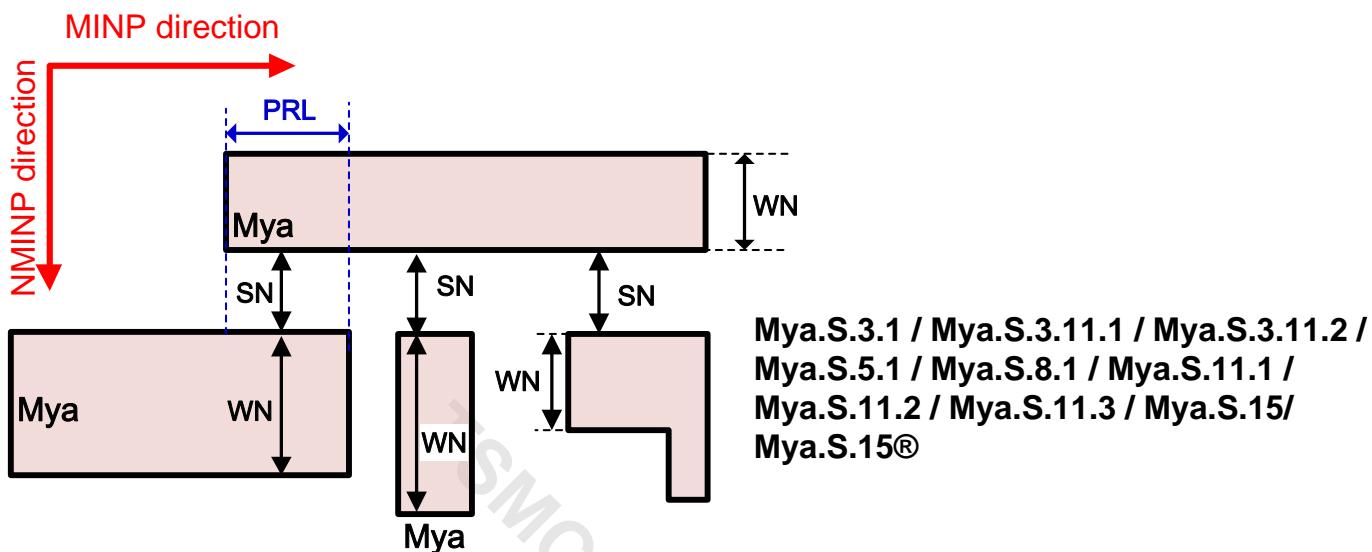


Note #2

Line end: edge length $\leq 0.080 \mu\text{m}$ between 2 consecutive 90-90 degree corners





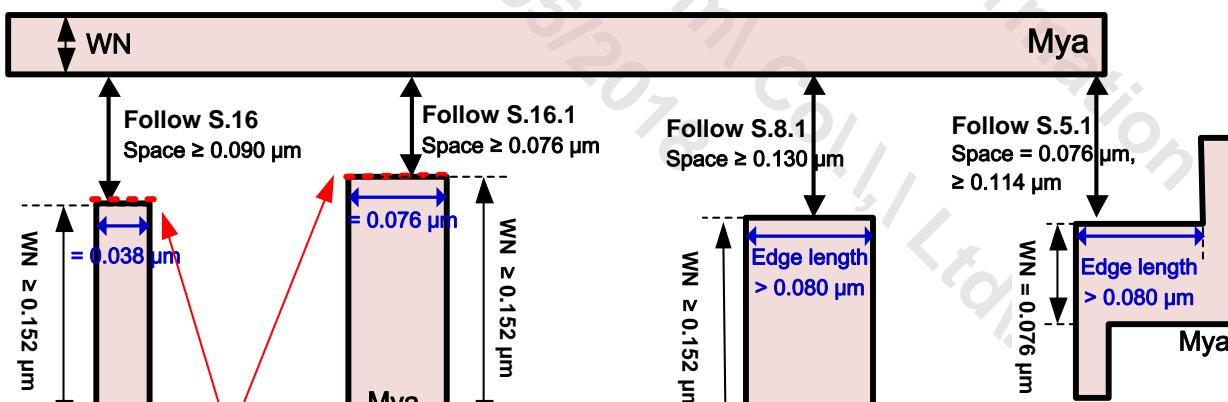


NMINP	Width / Space Table (unit: μm)											
Width (WN)	0.076	0.080	0.114	0.120	≥ 0.152	≥ 0.190	≥ 0.231	≥ 0.280	> 1.350	≥ 0.038	≥ 0.038	≥ 0.240
PRL	> -0.076	> -0.080	> -0.038	> -0.080	> 0.080	> 0.080	> 0.120	> 0.160	> 1.350	-0.076 ~ 0	-0.040 ~ 0	-0.160 ~ 0
Space (SN)	0.076	0.080	≥ 0.114	≥ 0.120	≥ 0.114	≥ 0.120	≥ 0.130	≥ 0.150	≥ 0.160	≥ 0.200	≥ 0.450	Corner projected space
												Corner projected space
Related Rule	Mva.S.5.1 ^{#1}	Mva.S.3.11.1 ^{#1}	Mva.S.3.1 ^{#1}	Mva.S.3.11.2 ^{#1}	Mva.S.8.1 ^{#1}	Mva.S.11.1 ^{#1}	Mya.S.11.2	Mya.S.11.3	Mya.S.15	Mya.S.6	Mya.S.6.1	Mya.S.6.2

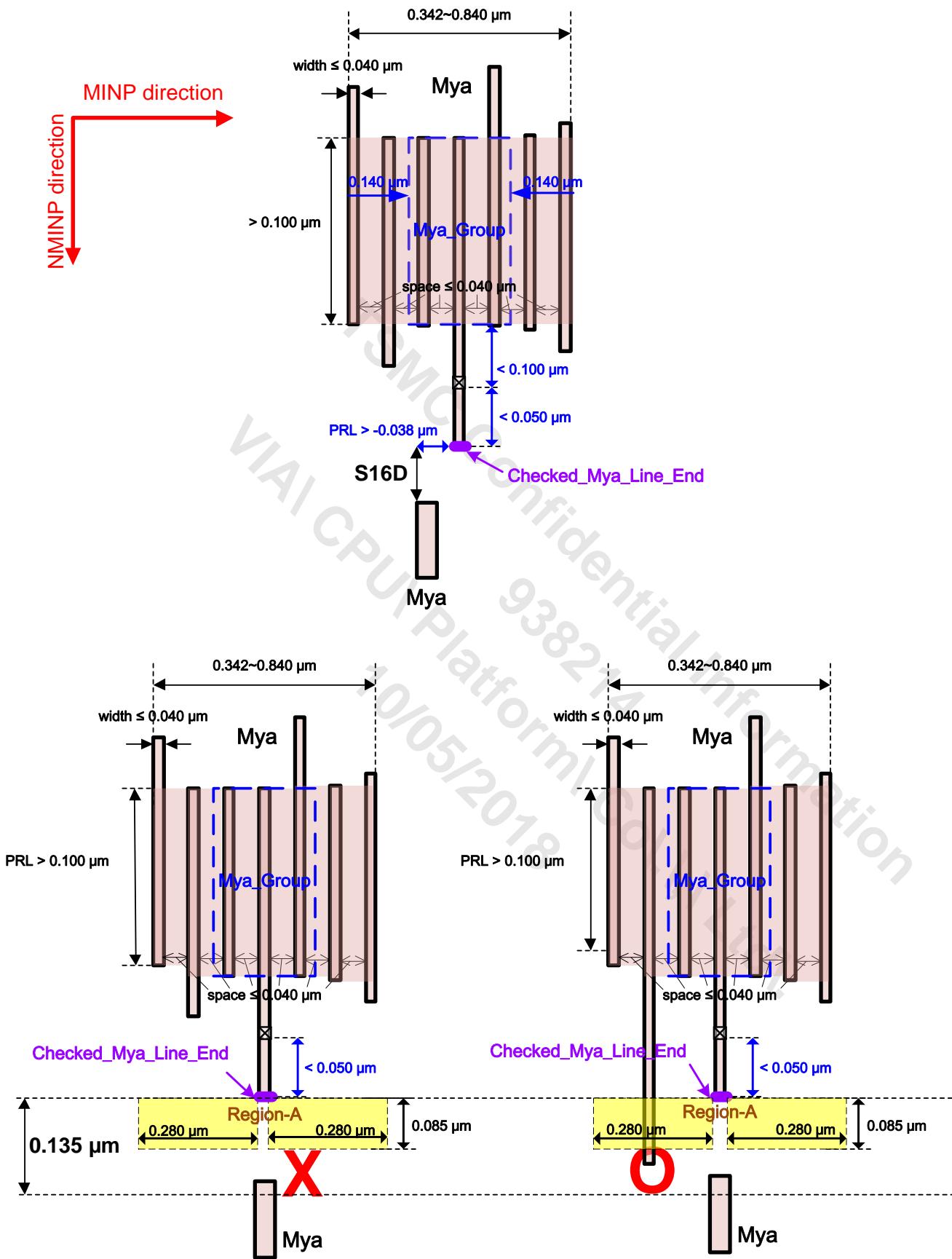
Note:

#1: Except line-end [edge length = 0.038/0.040 μm] space ≥ 0.090 μm, line-end [edge length = 0.076 μm] space ≥ 0.076 μm, line-end [edge length = 0.080 μm] space ≥ 0.080 μm

Note #1

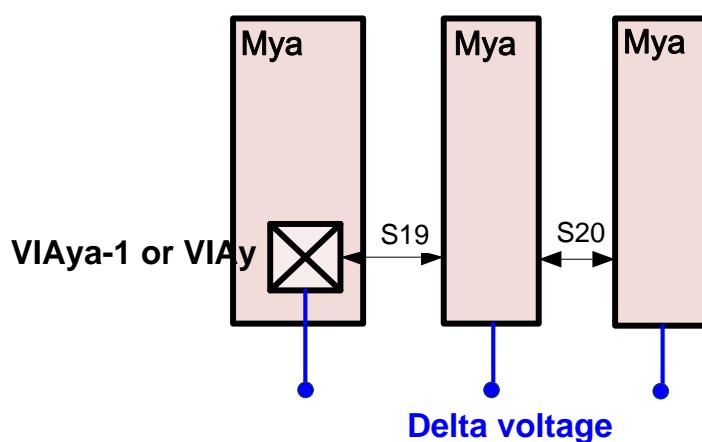
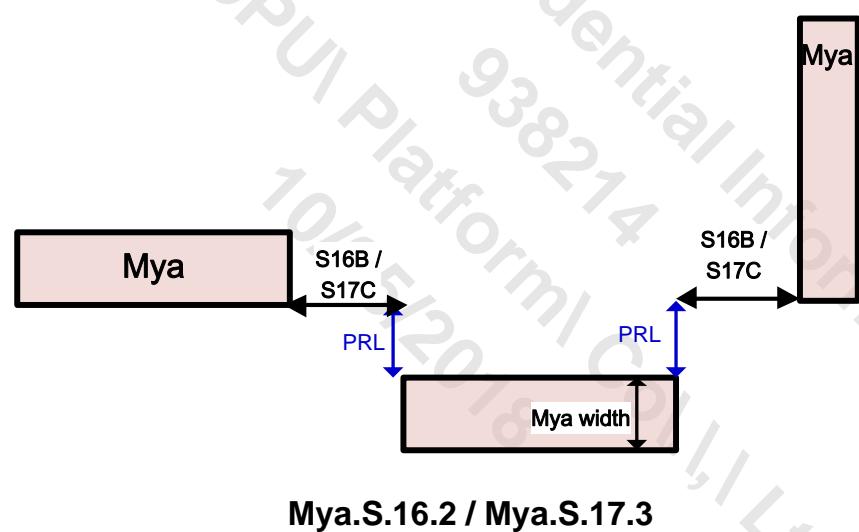
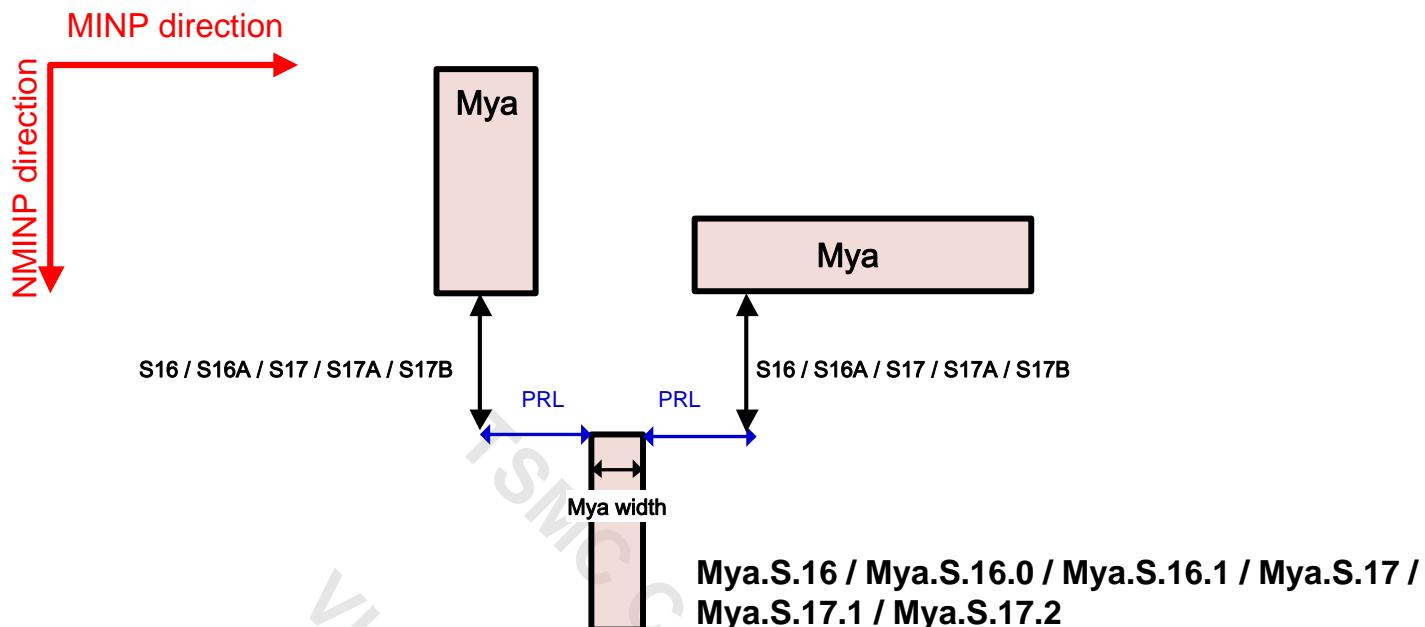


Line end: edge length $\leq 0.080 \mu\text{m}$ between
2 consecutive 90-90 degree corners

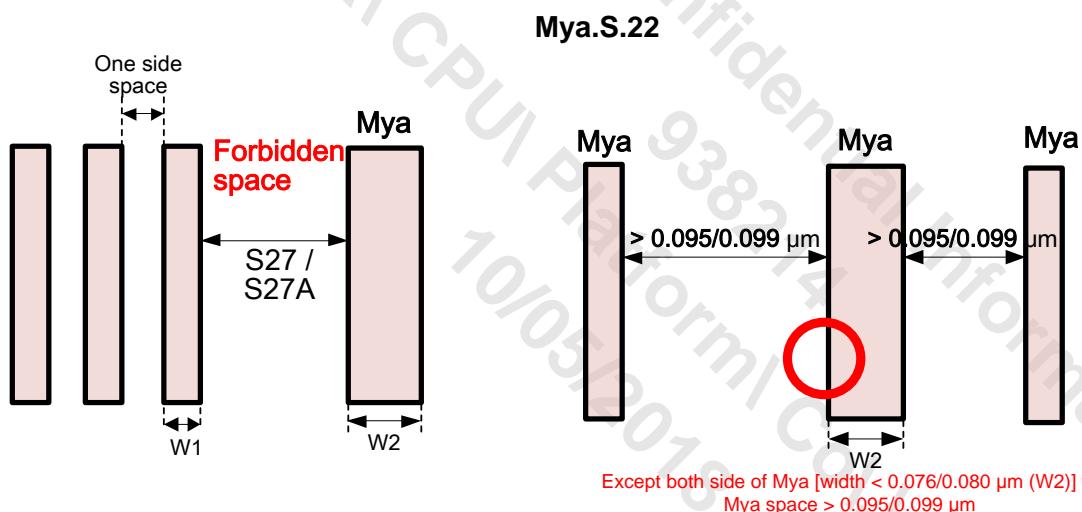
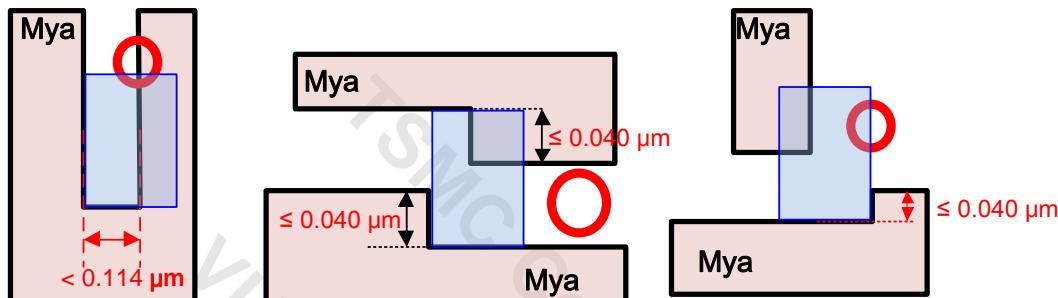
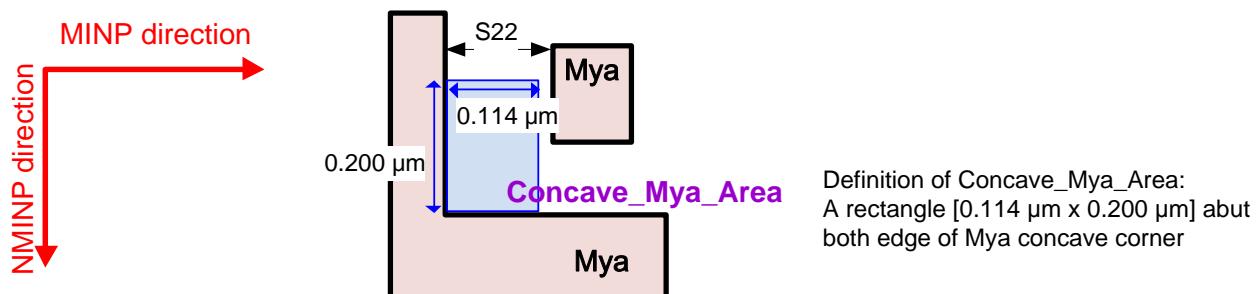


Except from **Checked_Mya_Line_End** corner to form two **Region-A** (Width in MINP/NMINP is 0.280 $\mu\text{m}/0.085 \mu\text{m}$), and neighboring Mya extension to region-A ≥ 0

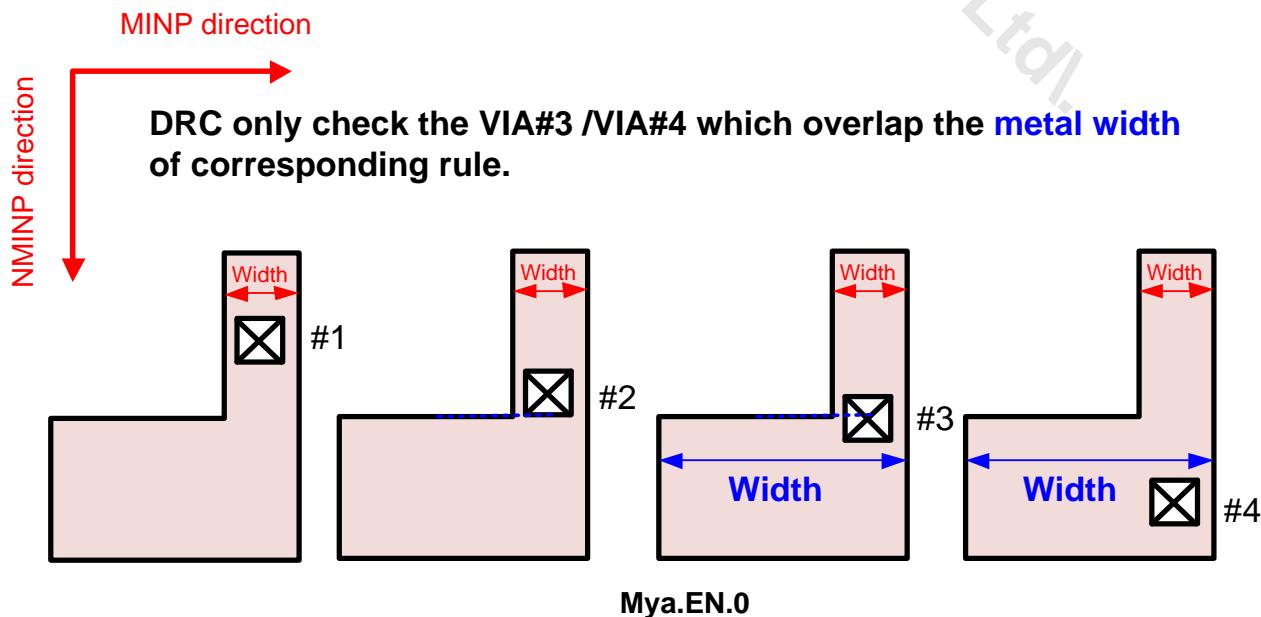
Mya.S.16.4

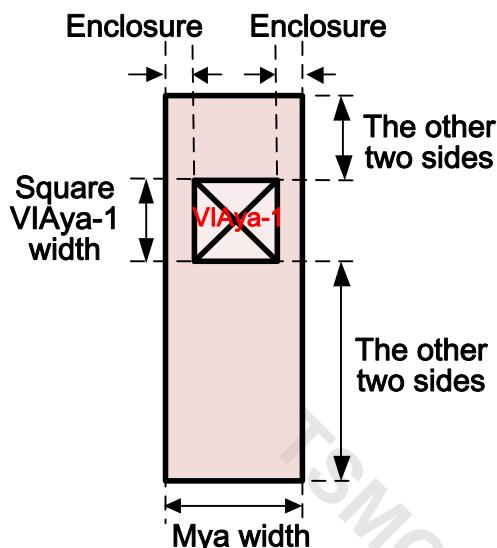


Mya.S.19 / Mya.S.19.1 / Mya.S.19.1.1
Mya.S.20 / Mya.S.20.1

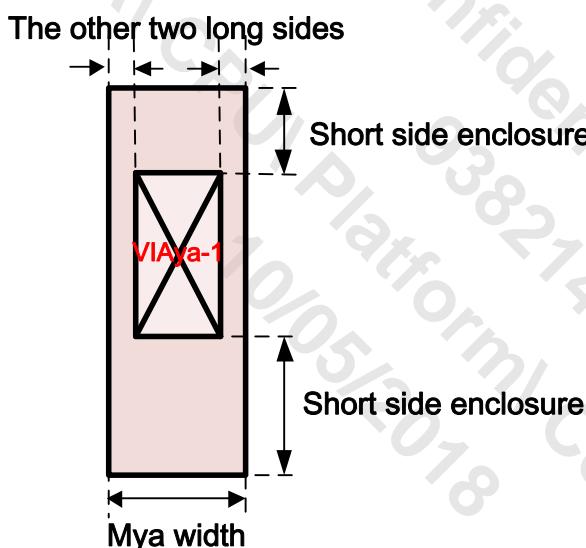


Mya.S.27 / Mya.S.27.1

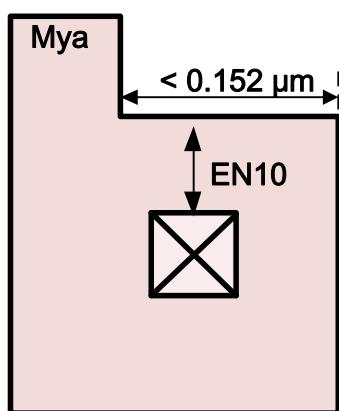




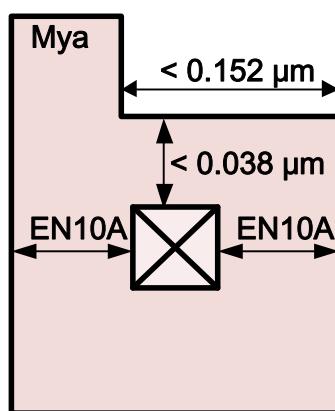
Mya.EN.1 / Mya.EN.1.0 / Mya.EN.1.1 / Mya.EN.1.3 / Mya.EN.1.11.1 /
Mya.EN.1.11.2 / Mya.EN.1.11.3 / Mya.EN.2 / Mya.EN.2.0 / Mya.EN.2.1 /
Mya.EN.2.3 / Mya.EN.2.11.1 / Mya.EN.2.11.2 / Mya.EN.2.11.3



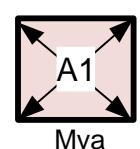
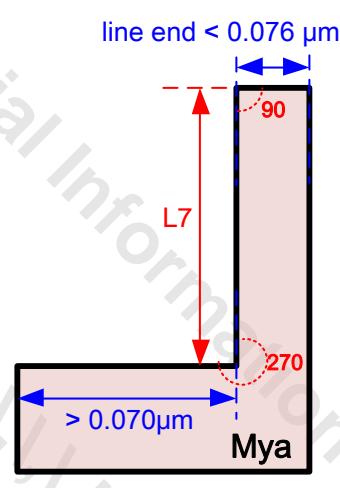
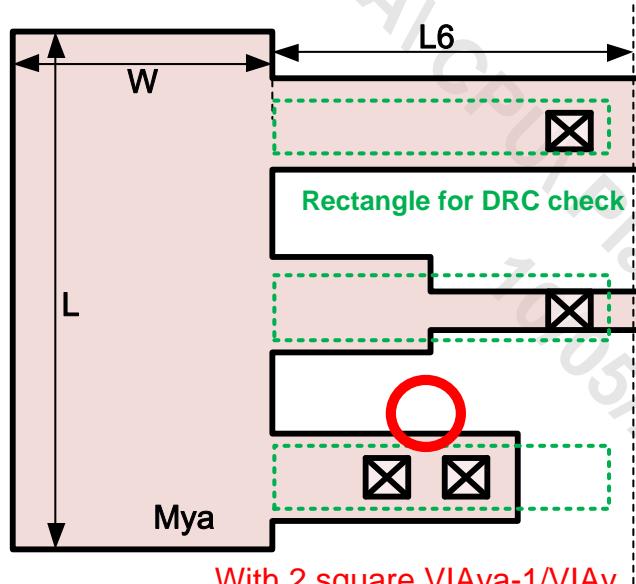
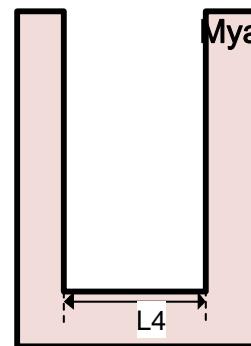
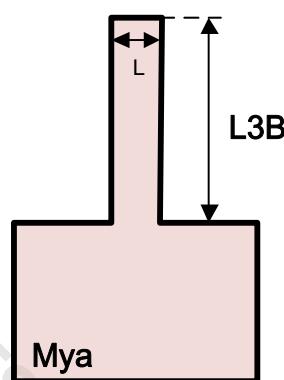
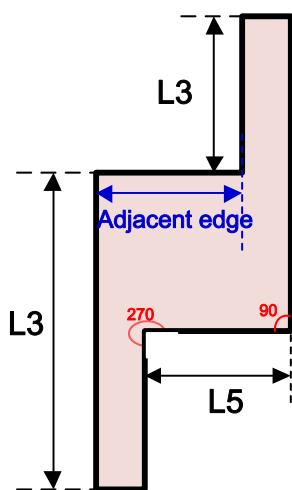
Mya.EN.4 / Mya.EN.4.1 / Mya.EN.5 / Mya.EN.5.1 /
Mya.EN.5.11.1 / Mya.EN.5.11.2 / Mya.EN.5.11.4 / Mya.EN.10



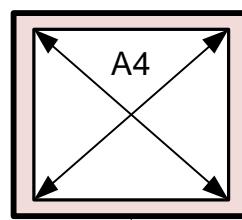
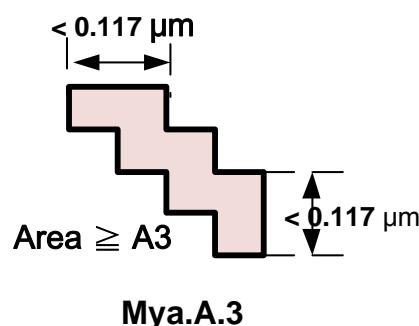
Mya.EN.10

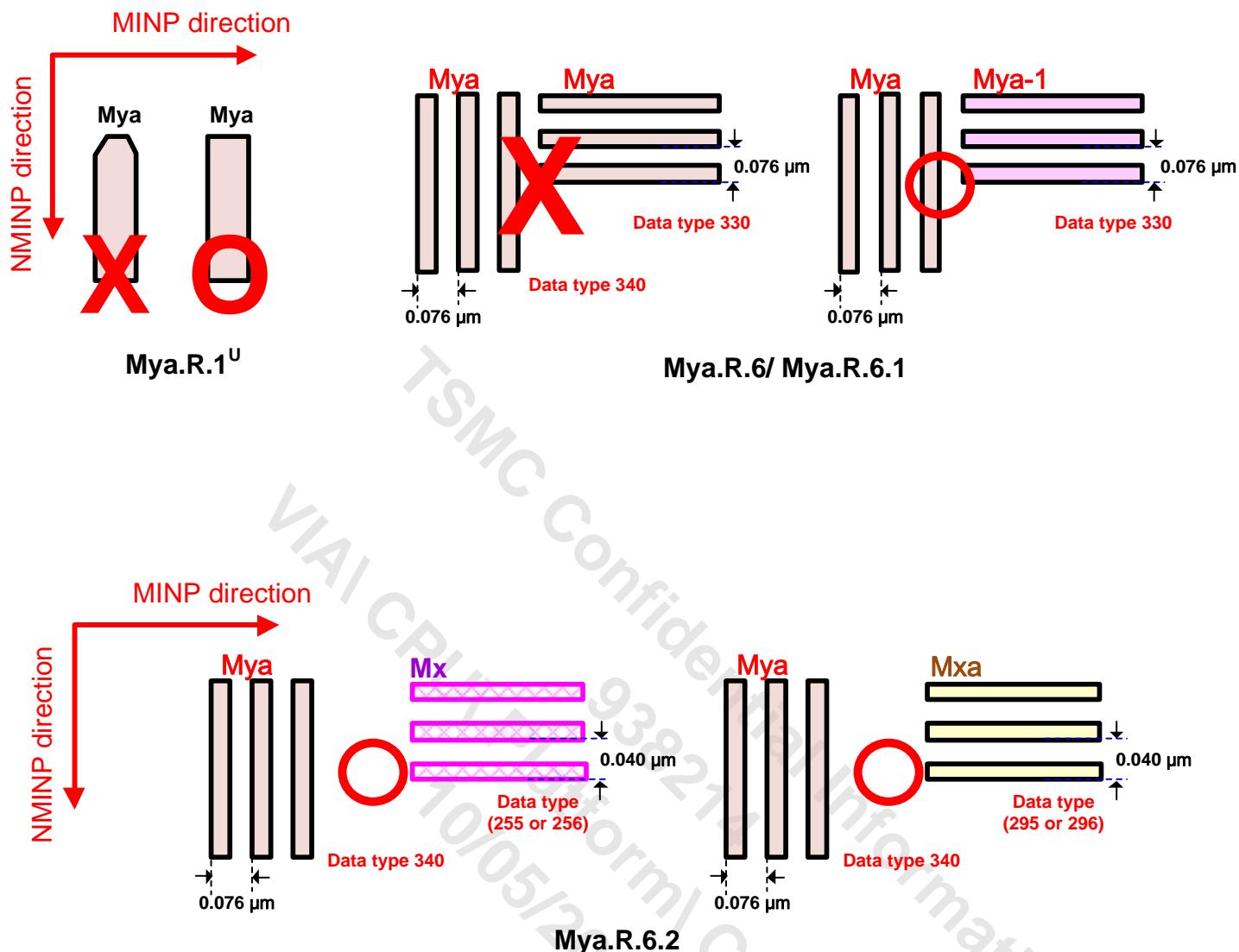


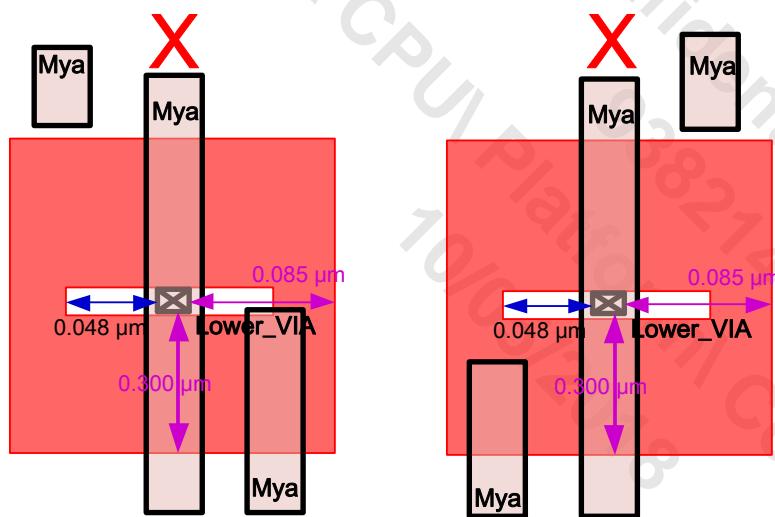
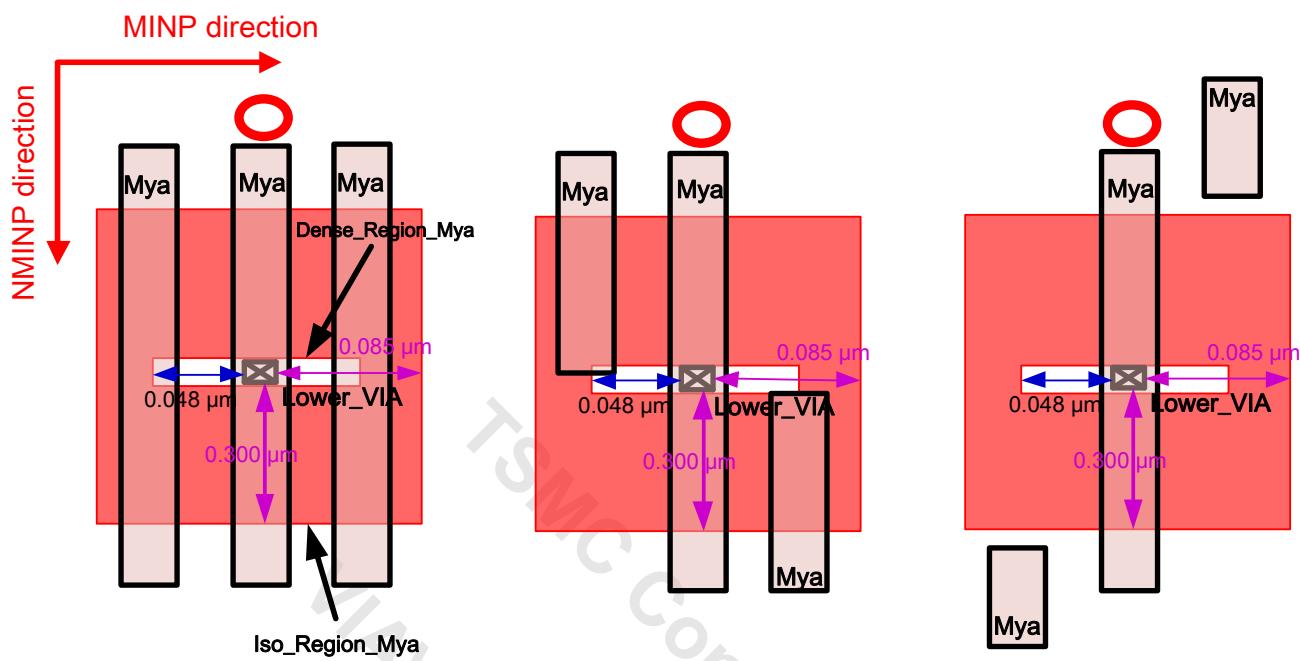
Mya.EN.10.1



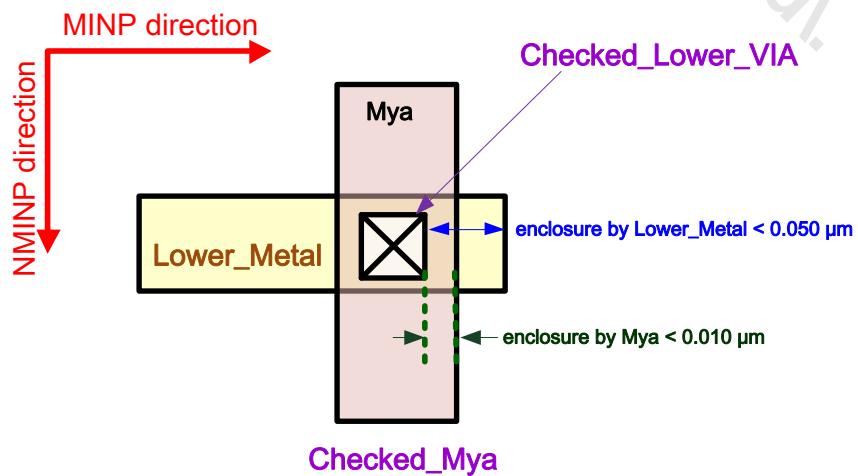
Mya.A.1®







Definition of Checked_Lower_VIA



Mya.R.7

4.5.52 VIAy Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
VIAy.W.1	Width (Except SEALRING_ALL)	W1	=	0.0380, 0.0580
VIAy.W.2	Width of VIAy bar in SEALRING_ALL	W2	=	0.4500
VIAy.S.1	Space (Except SEALRING_ALL)	S1	\geq	0.0530
VIAy.S.1.4	Space of VIAy [enclosure by My+1 > 0.001 μm for all sides] to VIAya [different net and PRL > 0 μm]	S1D	\geq	0.0540
VIAy.S.1.5	Space of VIAy [enclosure by My+1 > 0.001 μm for all sides] to VIAy-1 [different net and PRL > 0 μm]	S1E	\geq	0.0540
VIAy.S.4	Space of the long side of rectangular VIAy to VIAy [PRL > -0.076 μm]	S4	\geq	0.0820
VIAy.S.4.1	Space of the long side of rectangular VIAy to rectangular VIAy [PRL > -0.106 μm]	S4A	\geq	0.0820
VIAy.S.4.2	Corner-to-corner space of rectangular VIAy to rectangular VIAy [long side PRL \leq -0.106 μm , short side \leq -0.044 μm]	S4B	\geq	0.1340
VIAy.S.5	Space [different net and PRL > -0.038 μm] (Except SEALRING_ALL)	S5	\geq	0.0760
VIAy.S.5.1	Space (Except SEALRING_ALL, or following conditions: 1. VIAy_Group) Definition of VIAy_Group follows VIAy.S.14	S5A	\geq	0.0620
VIAy.S.5.2	Space [PRL > -0.038 μm] (Except SEALRING_ALL)	S5B	\geq	0.0740
VIAy.S.8	Space of the short side of rectangular VIAy to neighboring VIAy [PRL > - 0.038 μm]	S8	\geq	0.1340
VIAy.S.8.1	Space of the short side of rectangular VIAy to rectangular VIAy [PRL > - 0.044 μm]	S8A	\geq	0.1340
VIAy.S.12	Space to Isolating_Edge_Semi-iso_VIAy [Dense_Edge_Semi-iso_VIAy enclosure by Mya/My/My+1 < 0.010 μm] [PRL > -0.113 μm] Definition of Semi-iso_VIAy: VIAy [PRL > -0.0465 μm] one side space to Mya/My/My+1 \leq 0.050 μm , and the other side space > 0.050 μm in MINP direction Definition of Isolating_Edge_Semi-iso_VIAy: Semi-iso_VIAy edge [space to Mya/My/My+1 > 0.050 μm in MINP direction] Definition of Dense_Edge_Semi-iso_VIAy: Semi-iso_VIAy edge [space to Mya/My/My+1 \leq 0.050 μm in MINP direction]	S12	\geq	0.1130
VIAy.S.13	Space of square VIAy to Metal_Concave_Corner: Definition of Metal_Concave_Corner: A rectangle [0.001 μm x 0.001 μm] abut both edge of Mya/My/My+1 concave corner	S13	\geq	0.0100
VIAy.S.14	Space to VIAy_Group Definition of VIAy_Group: 2 square VIAy space < 0.054 μm , or 0.056 μm < space < 0.057 μm , or 0.059 μm < space < 0.060 μm in diagonal direction in one group, and DRC flags the square VIAy numbers > 2 in one group.	S14	\geq	0.0660
VIAy.S.21	Space of VIAy [width = 0.058 μm] to VIAy	S21	\geq	0.0930
VIAy.S.21.1	Space of VIAy [width = 0.058 μm] to VIAy [PRL > -0.050 μm]	S21A	\geq	0.1020
VIAy.S.21.2.1	Space of VIAy [width = 0.058 μm]	S21B1	\geq	0.0955
VIAy.S.21.2.2	Space of VIAy [width = 0.058 μm] [PRL > -0.050 μm]	S21B2	\geq	0.1220
VIAy.S.21.3	Space of VIAy [width = 0.058 μm] to rectangular VIAy	S21C	\geq	0.5000

Rule No.	Description	Label	Op.	Rule
VIAy.EN.0	Square VIAy enclosure by Mya, or My is defined by one of VIAy.EN.1 or VIAy.EN.1.4 or VIAy.EN.1.5, VIAy.EN.1.11.1, VIAy.EN.1.11.3			
VIAy.EN.1	Enclosure of square VIAy [width = 0.038 μm] by My or Mya [width = 0.038 μm] for two opposite sides with the other two sides ≥ 0.050 μm	EN1	≥	0
VIAy.EN.1.1	Enclosure of square VIAy [width = 0.038 μm] by My or Mya [width = 0.058 μm] for two opposite sides with the other two sides ≥ 0.050 μm	EN1	≥	0.0100
VIAy.EN.1.4	Enclosure of square VIAy [width = 0.038 μm] by My or Mya [width = 0.076 μm] for all sides	EN1D	≥	0.0190
VIAy.EN.1.5	Enclosure of square VIAy [width = 0.038 μm] by My or Mya [width ≥ 0.114 μm] for two opposite sides with the other two sides ≥ 0.030 μm	EN1E	≥	0.0200
VIAy.EN.1.11.1	Enclosure of square VIAy [width = 0.038 μm] by My or Mya [width = 0.040 μm] for two opposite sides with the other two sides ≥ 0.050 μm	EN1K1	≥	0.0010
VIAy.EN.1.11.2	Enclosure of square VIAy [width = 0.038 μm] by My or Mya [width = 0.060 μm] for two opposite sides with the other two sides ≥ 0.050 μm	EN1K1	≥	0.0110
VIAy.EN.1.11.3	Enclosure of square VIAy [width = 0.038 μm] by My or Mya [width = 0.080 μm] for all sides	EN1K3	≥	0.0210
VIAy.EN.2.1	Enclosure of square VIAy [width = 0.058 μm] by My or Mya [width = 0.058 μm] for two opposite sides with the other two sides ≥ 0.054 μm	EN2	≥	0
VIAy.EN.2.4	Enclosure of square VIAy [width = 0.058 μm] by My or Mya [width = 0.076 μm] for two opposite sides with the other two sides ≥ 0.047 μm	EN2D	≥	0.0090
VIAy.EN.2.5	Enclosure of square VIAy [width = 0.058 μm] by My or Mya [width ≥ 0.114 μm] for two opposite sides with the other two sides ≥ 0.040 μm	EN2E	≥	0.0280
VIAy.EN.2.11.2	Enclosure of square VIAy [width = 0.058 μm] by My or Mya [width = 0.060 μm] for two opposite sides with the other two sides ≥ 0.054 μm	EN2K1	≥	0.0010
VIAy.EN.2.11.3	Enclosure of square VIAy [width = 0.058 μm] by My or Mya [width = 0.080 μm] for two opposite sides with the other two sides ≥ 0.047 μm	EN2K3	≥	0.0110
VIAy.EN.4	Rectangular VIAy enclosure by Mya or My is defined by one of VIAy.EN.6 or VIAy.EN.6.1, VIAy.EN.6.1.1, VIAy.EN.6.1.2, or VIAy.EN.6.2 or VIAy.EN.7			
VIAy.EN.6	Enclosure of rectangular VIAy by My or Mya [width = 0.038 μm] for two opposite sides with the other two sides ≥ 0.050 μm	EN6	≥	0
VIAy.EN.6.0	Enclosure of rectangular VIAy by My or Mya [width = 0.058 μm] for two opposite sides with the other two sides ≥ 0.050 μm	EN6	≥	0.0100
VIAy.EN.6.1	Enclosure of rectangular VIAy by My or Mya [width = 0.076 μm] for two opposite sides with the other two sides ≥ 0.019 μm	EN6A	≥	0.0190
VIAy.EN.6.1.1	Enclosure of rectangular VIAy by My or Mya [width = 0.040 μm] for two opposite sides with the other two sides ≥ 0.050 μm	EN6A1	≥	0.0010
VIAy.EN.6.1.1.1	Enclosure of rectangular VIAy by My or Mya [width = 0.060 μm] for two opposite sides with the other two sides ≥ 0.050 μm	EN6A1	≥	0.0110
VIAy.EN.6.1.2	Enclosure of rectangular VIAy by My or Mya [width = 0.080 μm] for two opposite sides with the other two sides ≥ 0.021 μm	EN6A2	≥	0.0210
VIAy.EN.6.2	Short side enclosure of rectangular VIAy by My or Mya [width ≥ 0.114 μm] with the other two long side enclosure ≥ 0.038 μm (Except following conditions: 1. rectangular VIAy array)	EN6B	≥	0.0070
VIAy.EN.7	Enclosure of rectangular VIAy array by My/Mya for two opposite sides with the other two sides [rectangular VIAy array edge length = 0.100 μm] ≥ 0.016 μm Definition of rectangular VIAy array: VIAy long side space = 0.082 μm [PRL = 0.100 μm]	EN7	≥	0.0070
VIAy.L.1	Length of VIAy [width = 0.038 μm]	L1	=	0.0380, 0.1000
VIAy.L.2	Length of VIAy [width = 0.058 μm]	L2	=	0.0580
VIAy.R.0	45-degree VIAy is not allowed			
VIAy.R.2	Redundant via requirement must follow RuleTable.VIAy.R.2 of VIAy numbers and space (S1) for Mya/My and My+1 connection. [One of Mya/My or My+1 have width and length (W1) > 0.162 μm]. (Except following conditions: 1. VIA bar)			

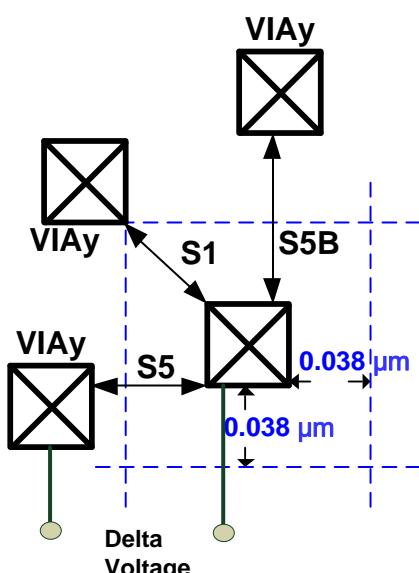
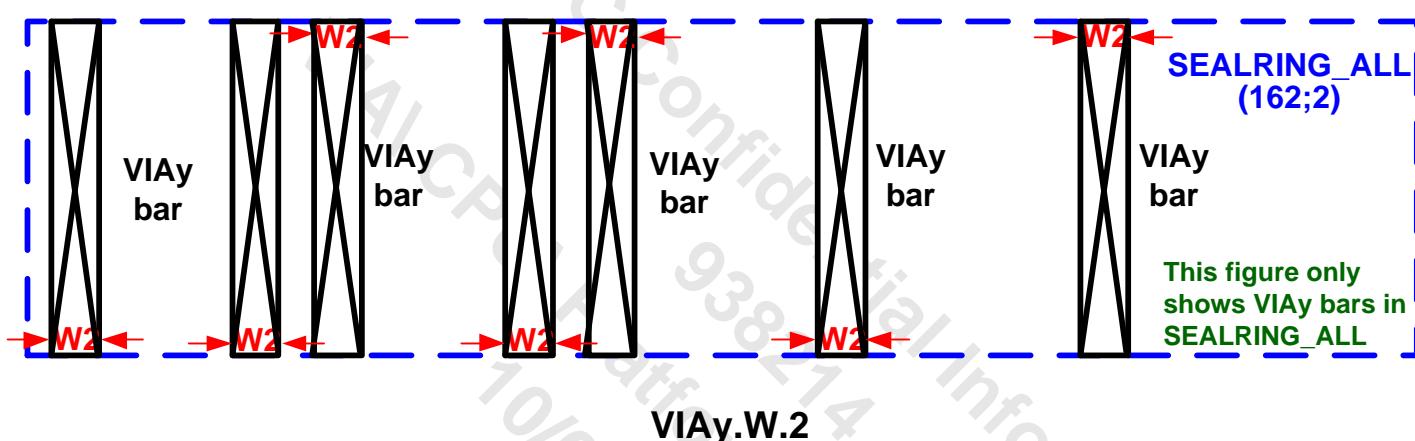
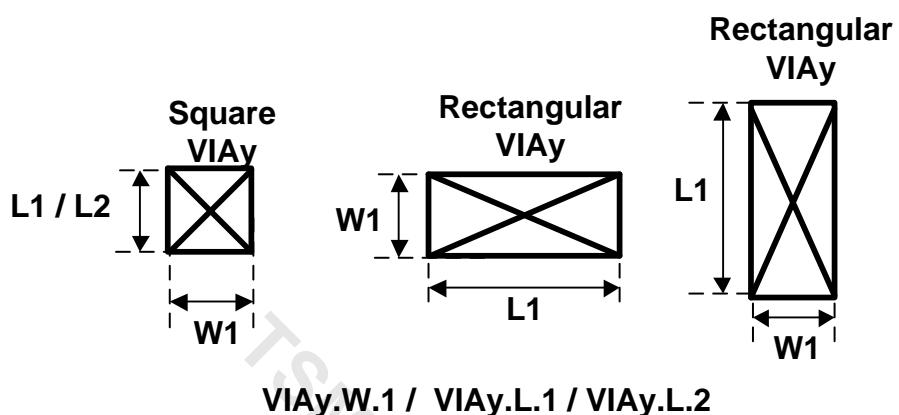
Rule No.	Description	Label	Op.	Rule
VIAy.R.2.1	Redundant via requirement must follow RuleTable.VIAy.R.2.1 of VIAy numbers and space (S1) for Mya/My and My+1 connection. [One of Mya/My or My+1 have width and length (W1) > 0.306 μm]. (Except following conditions: 1. VIA bar)			
VIAy.R.3	Redundant via requirement must follow RuleTable.VIAy.R.3 of VIAy numbers and space (S1) for Mya/My and My+1 connection. [One of Mya/My or My+1 have width and length (W1) > 0.420 μm]. (Except following conditions: 1. VIA bar)			
VIAy.R.4	At least two square VIAy [width = 0.038 μm] or one {rectangular VIAy OR square VIAya [width = 0.058 μm] must be used for a connection that distance \leq 1.485 μm (D) away from a metal plate (either Mya/My or My+1) with length > 0.162 μm (L) and width > 0.162 μm (W). (Except following conditions: 1. VIA bar)			
VIAy.R.5	At least two square VIAy [width = 0.038 μm] or one {rectangular VIAy OR square VIAya [width = 0.058 μm] must be used for a connection that distance \leq 3.6 μm (D) away from a metal plate (either Mya/My or My+1) with length > 0.900 μm (L) and width > 0.900 μm (W). (Except following conditions: 1. VIA bar)			
VIAy.R.6	At least two square VIAy [width = 0.038 μm] or one {rectangular VIAy OR square VIAya [width = 0.058 μm] must be used for a connection that distance \leq 9 μm (D) away from a metal plate (either Mya/My or My+1) with length > 1.35 μm (L) and width > 1.35 μm (W). (Except following conditions: 1. VIA bar)			
VIAy.R.7	VIAy must be fully covered by {Mya AND My+1} or {My AND My+1}			
VIAy.R.8	Single VIAy is not allowed in "H-shape" My+1 when all of the following conditions come into existence: 1. The My+1 has "H-shape" interact two metal holes: both two metal hole length (L2) \leq 4.5 μm and two metal hole area \leq 4.05 μm^2 2. The VIAy overlaps on the center metal bar of this "H-shape" My+1 3. The center metal bar length \leq 0.900 μm (L) and the metal bar width \leq 0.162 μm			
VIAy.R.13	Maximum area ratio of Mx/Mxa/Mya/My to upper VIAy in the same net [connects to gate with area > 10700 μm^2 , and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	350000
VIAy.R.13.2	Maximum area ratio of I/O gate to single layer VIAy in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area \geq 0.25 μm^2) Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	300000

Rule No.	Description	Label	Op.	Rule
VIAy.R.15	<p>VIAy must follow either one of the conditions.</p> <p>1. {Checked_Lower_Metal AND Dense_Region_Lower_Metal} must be projected [PRL \geq 0 μm] to another two {Lower_Metal AND Dense_Region_Lower_Metal} at both sides in MINP direction, or</p> <p>2. There is no other {Lower_Metal OVERLAP Iso_Region_Lower_Metal} and simultaneously {Checked_Lower_Metal AND Iso_Region_Lower_Metal} can't be projected [PRL \geq 0 μm] to {Checked_Lower_Metal AND Iso_Region_Lower_Metal} at four sides.</p> <p>Definition of Checked_VIAy: VIAy [enclosure by Lower_Metal < 0.001 μm and enclosure by Upper_Metal < 0.065 μm at the same time]</p> <p>Definition of Checked_Lower_Metal: {Lower_Metal OVERLAP Checked_VIAy}</p> <p>Definition of Dense_Region_Lower_Metal: A rectangle formed by Checked_VIAy edge expanding 0.039 μm in Lower_Metal MINP direction</p> <p>Definition of Iso_Region_Lower_Metal: A rectangle formed by Checked_VIAy edge expanding 0.076 μm in Lower_Metal MINP direction and expanding 0.300 μm in Lower_Metal NMNP direction</p> <p>DRC checks Mya/My drawing pattern only</p>			
VIAy.R.9®	Recommended maximum consecutive stacked VIAy layer, which has only one square via for each VIAy layer to avoid high Rc		\leq	4

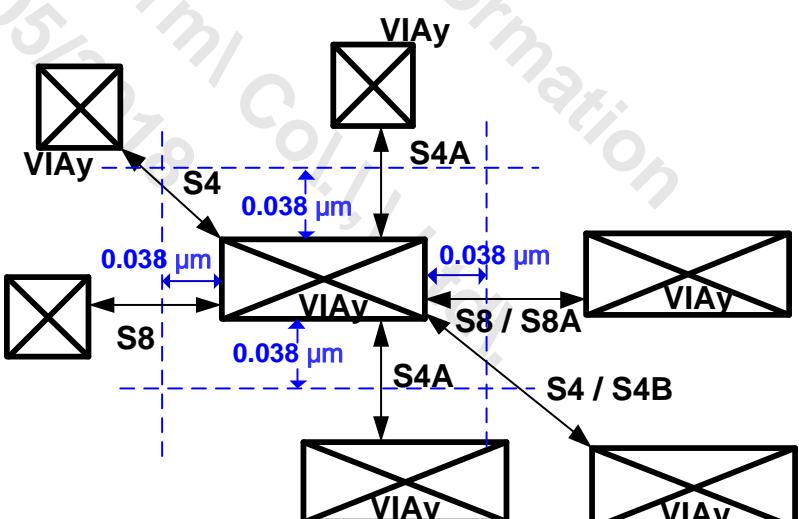
Table Notes:

- Delta Voltage Calculation in high voltage spacing rules please refer to section 3.9 DRC methodology of net voltage recognition.

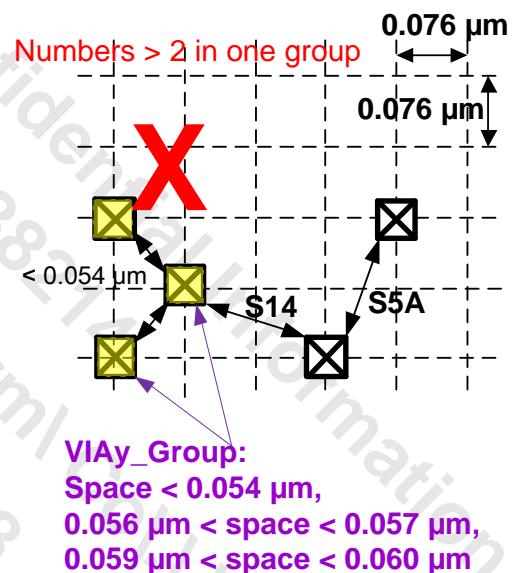
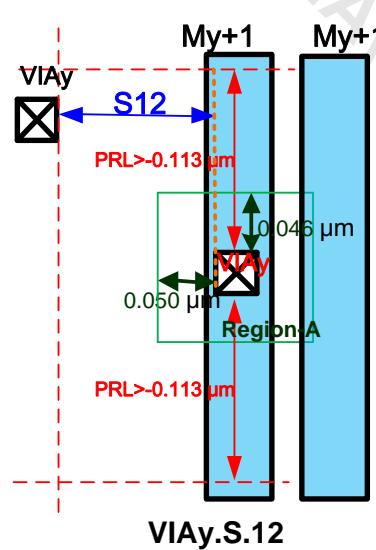
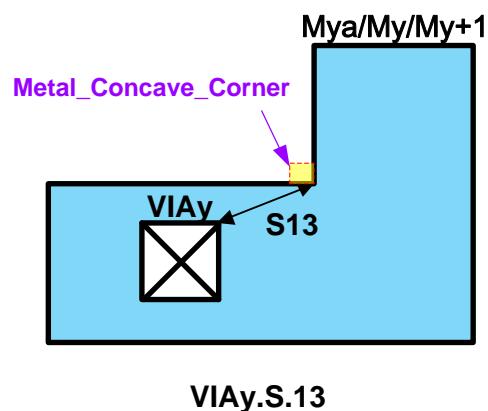
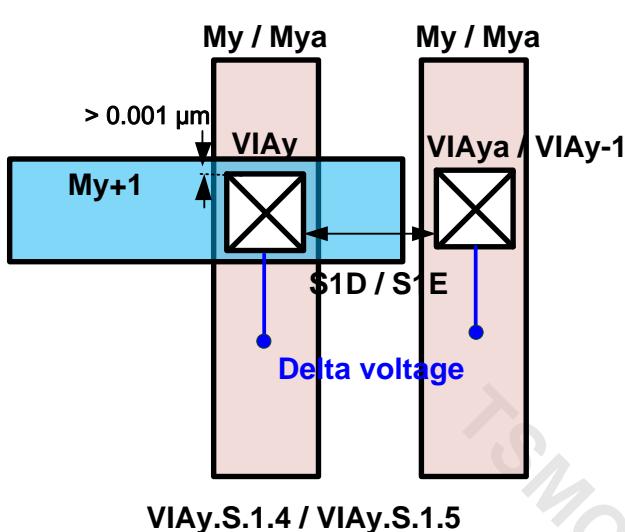
VIAy



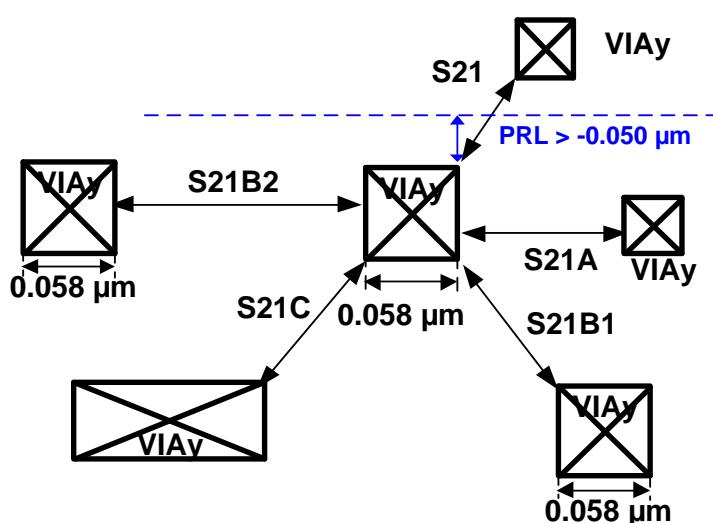
**VIAy.S.1 / VIAy.S.5 /
VIAy.S.5.2**

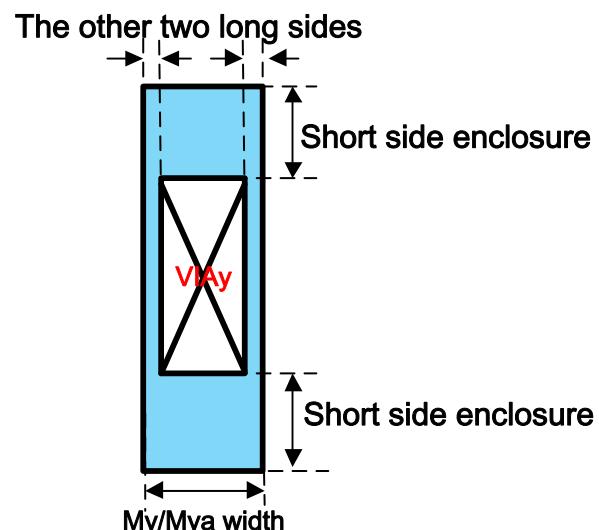
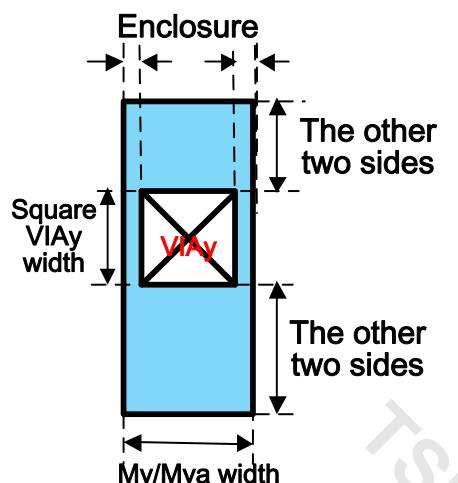


**VIAy.S.4 / VIAy.S.4.1 / VIAy.S.4.2 / VIAy.S.8 /
VIAy.S.8.1**



VIAy.S.5.1 / VIAy.S.14





VIAy.EN.1 / VIAy.EN.1.1 / VIAy.EN.1.4 /

VIAy.EN.1.5 / VIAy.EN.1.11.1 / VIAy.EN.1.11.2 /

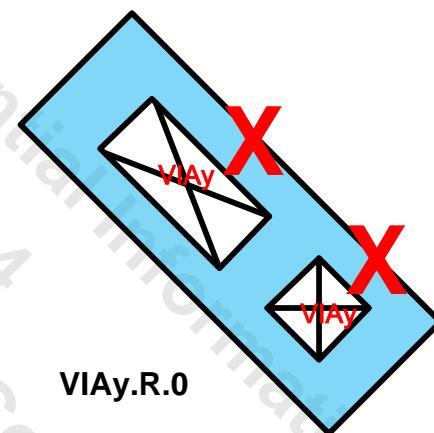
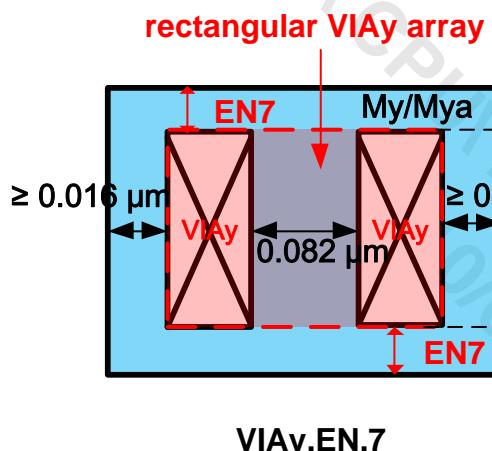
VIAy.EN.1.11.3 / VIAy.EN.2.1 / VIAy.EN.2.4 /

VIAy.EN.2.5 / VIAy.EN.2.11.2 / VIAy.EN.2.11.3

VIAy.EN.4 / VIAy.EN.6 / VIAy.EN.6.0 /

VIAy.EN.6.1 / VIAy.EN.6.1.1 / VIAy.EN.6.1.1.1 /

VIAy.EN.6.1.2 / VIAy.EN.6.2



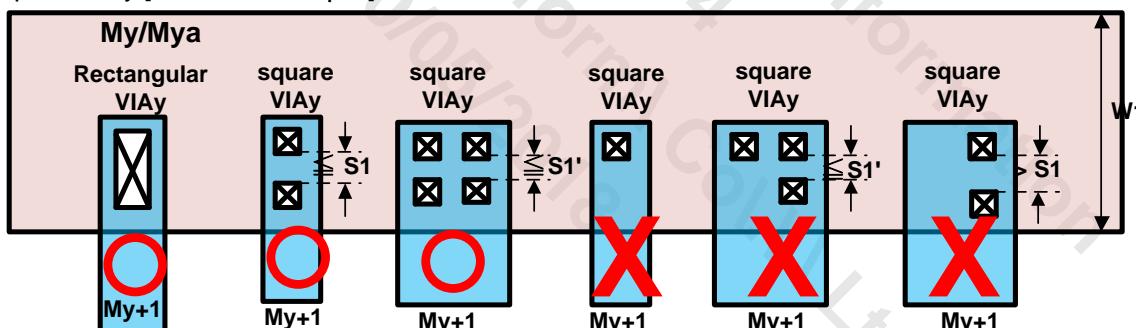
RuleTable.VIAy.R.2	0.162 μm < W1 ≤ 0.306 μm					
VIAy space (S1) (μm)	0.070 ≤ S1 ≤ 0.090			0.090 < S1 ≤ 0.765		
{Rectangular VIAy [width/length = 0.038/0.100 μm] OR square VIAy [width = 0.058 μm]} (#)	0	1	/	0	1	2
Square VIAy [width = 0.038 μm] (#)	≥ 2	≥ 0	/	≥ 4	≥ 2	≥ 0

RuleTable.VIAy.R.2.1	0.306 μm < W1 ≤ 0.420 μm							
VIAy space (S1) (μm)	0.070 ≤ S1 ≤ 0.090			0.090 < S1 ≤ 0.765				
{Rectangular VIAy [width/length = 0.038/0.100 μm] OR square VIAy [width = 0.058 μm]} (#)	0	1	2*	0	1	2	3	/
Square VIAy [width = 0.038 μm] (#)	≥ 3	≥ 1	≥ 0	≥ 6	≥ 4	≥ 2	≥ 0	/

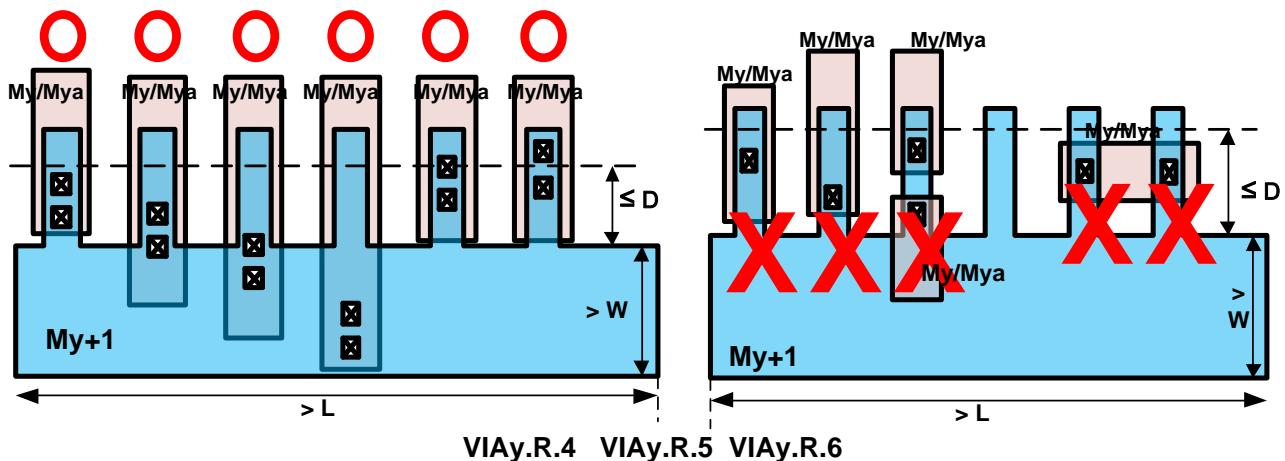
*Not for square VIAy [width = 0.058 μm]

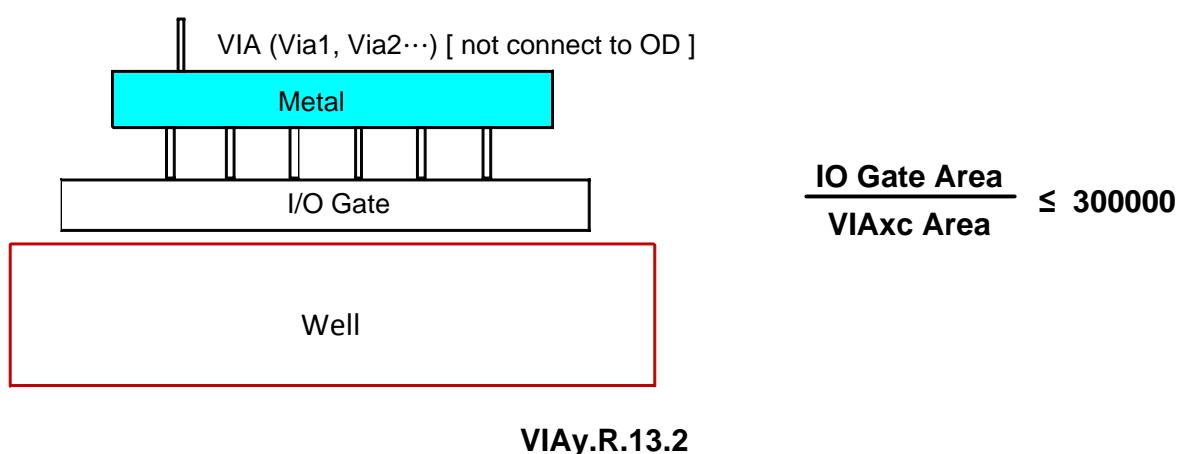
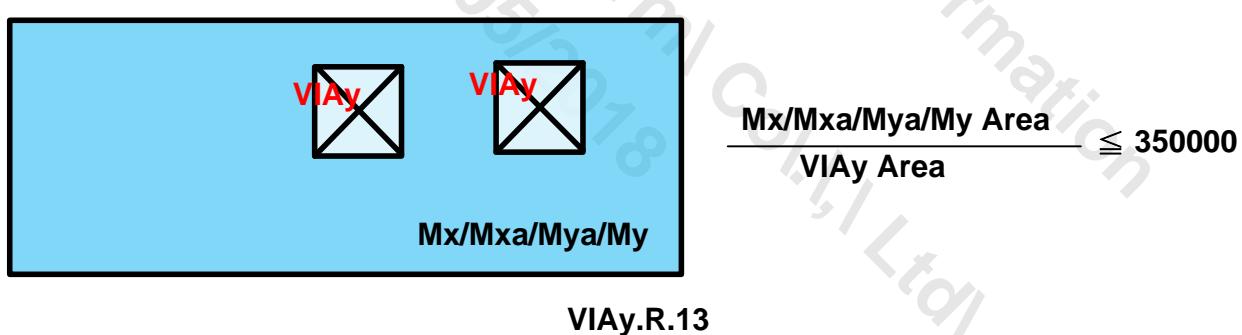
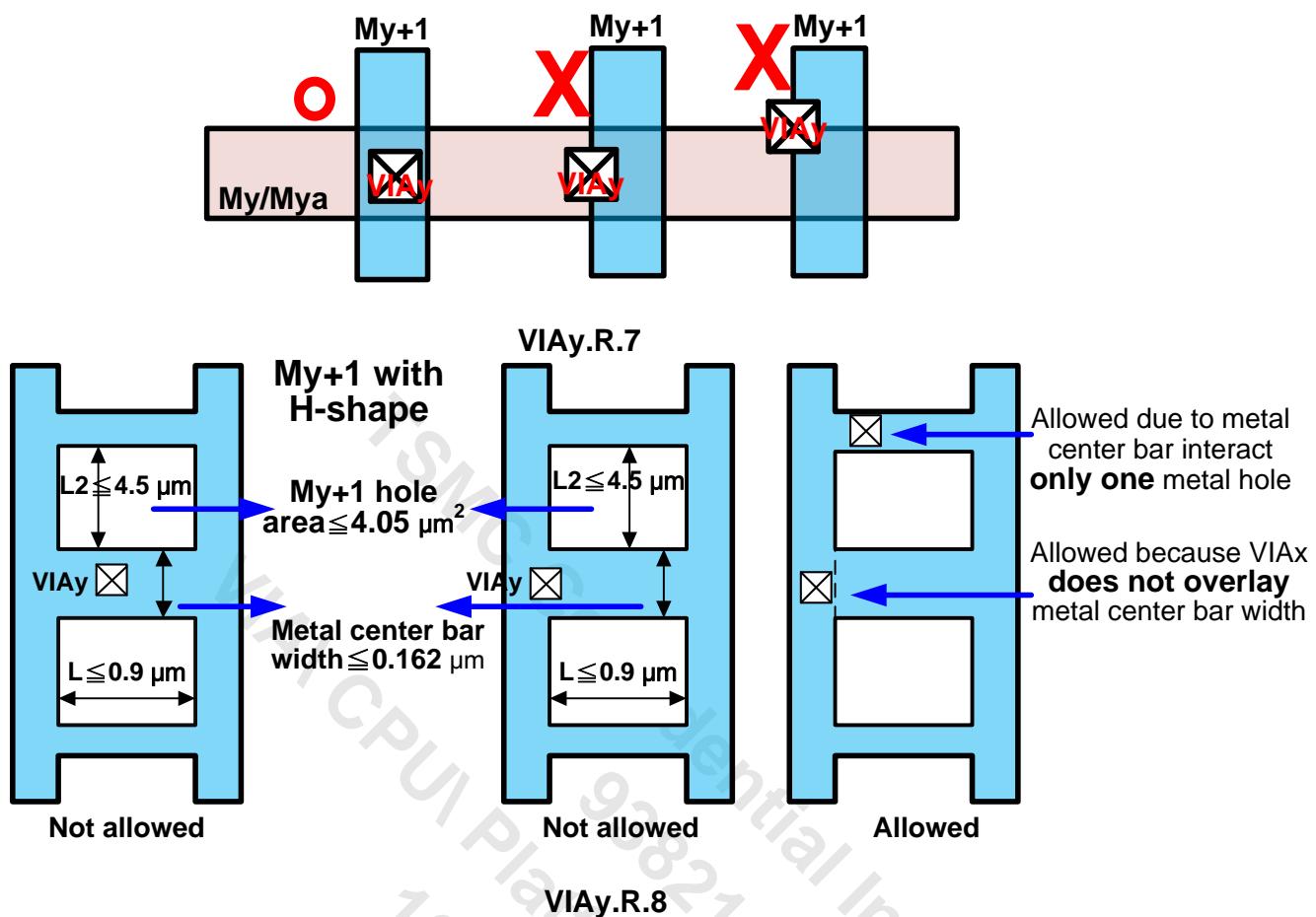
RuleTable.VIAy.R.3	W1 > 0.420 μm								
VIAy space (S1) (μm)	0.070 ≤ S1 ≤ 0.090			0.090 < S1 ≤ 0.765					
{Rectangular VIAy [width/length = 0.038/0.100 μm] OR square VIAy [width = 0.058 μm]} (#)	0	1	2*	0	1	2	3	4	5
Square VIAy [width = 0.038 μm] (#)	≥ 4	≥ 2	≥ 0	≥ 9	≥ 7	≥ 5	≥ 3	≥ 1	≥ 0

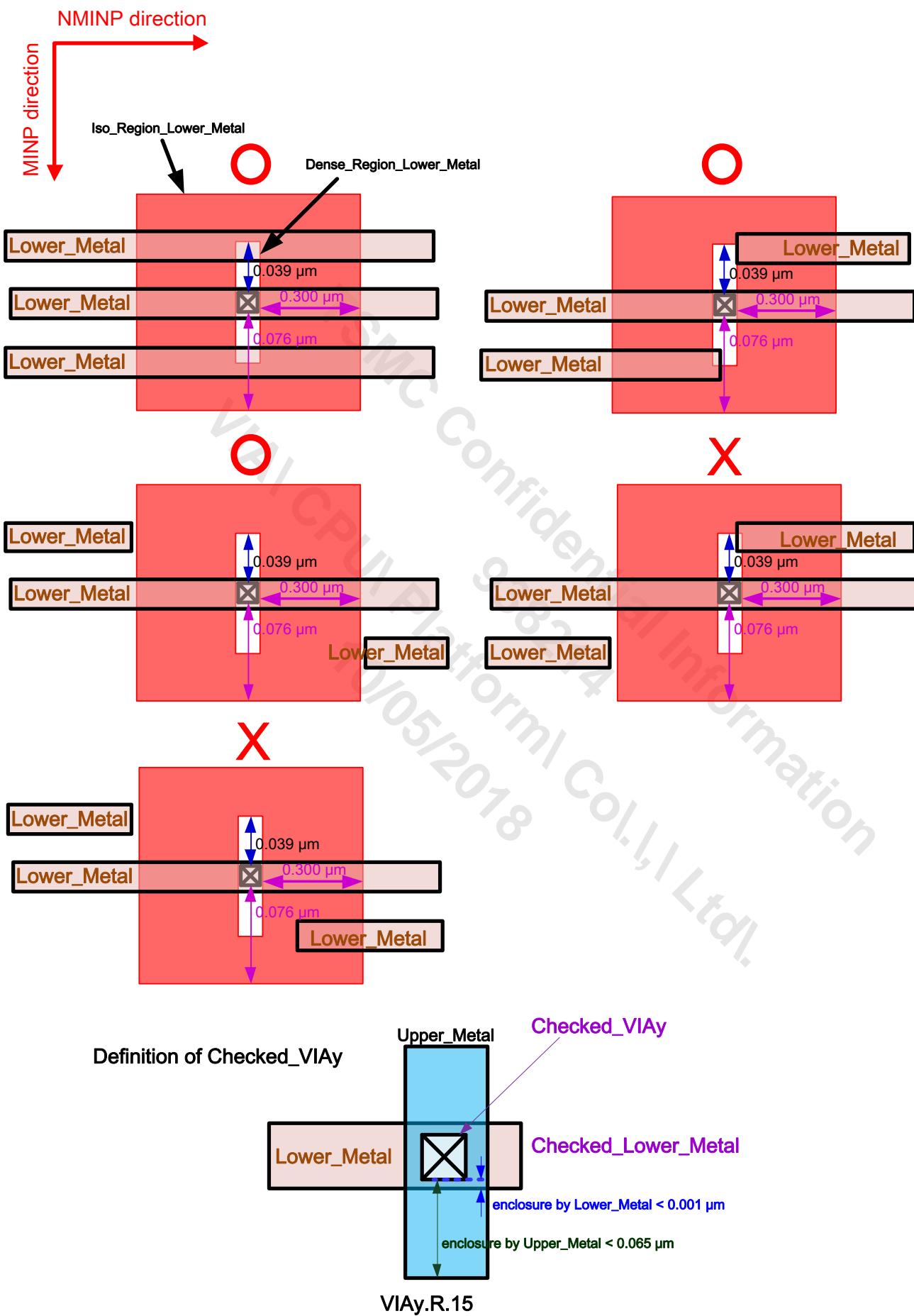
*Not for square VIAy [width = 0.058 μm]



VIAy.R.2 / VIAy.R.2.1 / VIAy.R.3







4.5.53 My Layout Rules

- MINimum Pitch (MINP) 0.076 μm can only be drawn in either parallel or perpendicular to PO direction
 - Data type 360 is used for metal pitch 0.076 μm in perpendicular to core PO direction, or
 - Data type 350 is used for metal pitch 0.076 μm in parallel to core PO direction
- NonMINimum Pitch (NMINP) direction is perpendicular to Minimum pitch (MINP) direction.

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5. DRC checks DMy_O as well as My in this section.

Rule No.	Description	Label	Op.	Rule
My.W.1	Width	W1	≥	0.0380
My.W.1.1	Width [MINP direction]	W1A	=	0.0380, 0.0400, 0.0580, 0.0600, 0.0760, 0.0800, 0.1140, 0.1200, ≥ 0.1520
My.W.1.3	Width [NMINP direction]	W1C	=	0.0760, 0.0800, 0.1140, 0.1200, ≥ 0.1520
My.W.1.4	Width of DMy_O [MINP direction]	W1D	=	0.0580, 0.1900
My.W.2	Width of 45-degree bent My	W2	≥	0.4000
My.W.3	Maximum width (Except SEALRING_ALL)	W3	≤	2
My.W.5	My branch width connected to My plate with length > 0.400 μm (L) and width > 0.400 μm (W)	W5	≥	0.0760
My.W.6	Concave corner to concave corner width	W6	≥	0.0890
My.S.1	Space	S1	≥	0.0380
My.S.1.1	Space of DMy_O [MINP direction]	S1A	≥	0.0760
My.S.2.1.1	Space of My [width = 0.038 μm in MINP direction] to My [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.076 μm] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition: (1) Z-shape [0.040 μm < edge length < 0.201 μm between 2 consecutive 90-270 degree corners, corresponding width = 0.076/0.080 μm in NMINP direction between 2 opposite 0.040 μm < edge length < 0.201 μm, not including T-shape] (2) flag-shape [0.040 μm < edge length < 0.201 μm between 2 consecutive 90-270 degree corners, the opposite 0.080 μm < edge length < 0.201 μm between 2 consecutive 90-90 degree corners, corresponding width = 0.076/0.080 μm in NMINP direction between these 2 opposite edge, and the other corresponding width > 0.040 μm in MINP direction]	SM	=	0.0380, 0.0570, 0.0660, 0.0760, 0.0950, ≥ 0.1140
My.S.2.1.2	Space of My [width = 0.038 μm in MINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0380, ≥ 0.1140
My.S.2.2.1	Space of My [width = 0.058 μm in MINP direction] in MINP direction [PRL > -0.076 μm] DRC checks space of My drawing pattern only	SM	=	0.0560, 0.0940, ≥ 0.1140
My.S.2.2.2	Space of My [width = 0.058 μm in MINP direction] to My [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.076 μm] DRC checks space of My drawing pattern only	SM	=	0.0470, 0.0560, 0.0660, 0.0940, ≥ 0.1140
My.S.2.2.3	Space of DMy_O [width = 0.058 μm in MINP direction] to My [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0760, ≥ 0.1140

Rule No.	Description	Label	Op.	Rule
My.S.2.3.1	Space of My [width = 0.076 μm in MINP direction] to My [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.076 μm] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	=	0.0470, 0.0570, 0.0760, 0.0950, ≥ 0.1140
My.S.2.3.2	Space of My [width = 0.076 μm in MINP direction] to My [width = 0.038 μm in MINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0570, 0.0950, ≥ 0.1140
My.S.2.3.2.1	Space of My [width = 0.076 μm in MINP direction] to My [width = 0.058 μm in MINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0470, ≥ 0.1140
My.S.2.3.3	Space of My [width = 0.076 μm in MINP direction] in MINP direction [PRL > -0.076 μm]	SM	=	0.0760, ≥ 0.1140
My.S.2.4.1	Space of My edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.038 μm] [at least one My width = 0.114 μm in MINP direction] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	=	0.0760, ≥ 0.1140
My.S.2.4.2	Space of My edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.038 μm] [both My width = 0.114 μm in MINP direction] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	≥	0.1140
My.S.2.4.3	Space of My edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.038 μm] [one My width = 0.114 μm, the other one My width = 0.076 μm, in MINP direction] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	≥	0.1140
My.S.2.4.4	Space of My [width ≥ 0.080 μm in MINP direction] to My [width > 0.040 μm in MINP direction] in MINP direction [PRL > -0.038 μm] (Except following conditions: 1. Space between Z-/Z-, Z-/flag, or flag-/flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	≥	0.0560
My.S.2.4.5	Space of My [width ≥ 0.080 μm in MINP direction] to My [width > 0.060 μm in MINP direction] in MINP direction [PRL > -0.038 μm] (Except following conditions: 1. Space between Z-/Z-, Z-/flag, or flag-/flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	≥	0.0760
My.S.2.11.1	Space of My [width = 0.040 μm in MINP direction] to My [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.080 μm] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	=	0.0400, 0.0600, 0.0700, 0.0800, 0.1000, ≥ 0.1200
My.S.2.11.2	Space of My [width = 0.040 μm in MINP direction] in MINP direction [PRL > -0.080 μm]	SM	=	0.0400, ≥ 0.1200
My.S.2.12.1	Space of My [width = 0.060 μm in MINP direction] to My [with edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.080 μm] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	=	0.0600, 0.0700, 0.1000, ≥ 0.1200
My.S.2.12.2	Space of My [width = 0.060 μm in MINP direction] in MINP direction [PRL > -0.080 μm]	SM	=	0.0600, 0.1000, ≥ 0.1200

Rule No.	Description	Label	Op.	Rule
My.S.2.12.3	Space of My [width = 0.060 µm in MINP direction] to My [width = 0.080 µm in MINP direction] in MINP direction [PRL > -0.080 µm]	SM	≥	0.1200
My.S.2.12.4	Space of My [width = 0.060 µm in MINP direction] to My [width = 0.040 µm in MINP direction] in MINP direction [PRL > -0.080 µm]	SM	=	0.0700, ≥ 0.1200
My.S.2.13.1	Space of My [width = 0.080 µm in MINP direction] to My [with edge length > 0.080 µm in NMINP direction] in MINP direction [PRL > -0.080 µm] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	=	0.0600, 0.0800, 0.1000, ≥ 0.1200
My.S.2.13.2	Space of My [width = 0.080 µm in MINP direction] in MINP direction [PRL > -0.080 µm]	SM	=	0.0800, ≥ 0.1200
My.S.2.13.3	Space of My [width = 0.080 µm in MINP direction] to My [width = 0.040 µm in MINP direction] in MINP direction [PRL > -0.080 µm]	SM	≥	0.0600, 0.1000, ≥ 0.1200
My.S.2.14.1	Space of My edge [edge length > 0.080 µm in NMINP direction] in MINP direction [PRL > -0.040 µm] [at least one My width = 0.120 µm in MINP direction] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	=	0.0800, ≥ 0.1200
My.S.2.14.2	Space of My edge [edge length > 0.080 µm in NMINP direction] in MINP direction [PRL > -0.040 µm] [one My width = 0.120 µm, the other one My width = 0.038 µm or ≥ 0.058 µm in MINP direction] (Except following conditions: 1. both two corners from Z-shape, or flag-shape) Definition of Z-shape/flag-shape follows My.S.2.1.1	SM	≥	0.1200
My.S.3.1	Space of My edge [edge length > 0.080 µm in MINP direction] in NMINP direction [PRL > -0.038 µm] [at least one My width = 0.114 µm in NMINP direction]	SN	≥	0.1140
My.S.3.11.1	Space of My [width = 0.080 µm in NMINP direction] to My [with edge length > 0.080 µm in MINP direction] in NMINP direction [PRL > -0.080 µm]	SN	=	0.0800, ≥ 0.1200
My.S.3.11.2	Space of My [width = 0.120 µm in NMINP direction] to My [with edge length > 0.080 µm in MINP direction] in NMINP direction [PRL > -0.040 µm]	SN	≥	0.1200
My.S.5.1	Space of My edge [edge length > 0.080 µm in MINP direction] in NMINP direction [PRL > -0.076 µm] [at least one My width = 0.076 µm in NMINP direction]	SN	=	0.0760, ≥ 0.1140
My.S.5.4	Space of My [width = 0.038 µm in MINP direction] to My [width = 0.040/0.060 µm in MINP direction] [PRL > -0.300 µm]	S5D	≥	0.3000
My.S.5.4.1	Space of My [width = 0.058 µm in MINP direction] to My [width = 0.040 µm in MINP direction] [PRL > -0.300 µm] DRC checks space of My drawing pattern only	S5D	≥	0.3000
My.S.5.4.1.1	Space of DMy_O [width = 0.058 µm in MINP direction] to My [width = 0.040 µm in MINP direction] [PRL > -0.120 µm]	S5D	≥	0.1200
My.S.5.4.2	Space of My [width = 0.076 µm in MINP direction] to My [width = 0.080 µm in MINP direction] in NMINP direction [PRL > -0.300 µm]	S5D	≥	0.3000
My.S.6	Corner projected space of My [-0.076 µm < PRL ≤ 0 µm] (Except following conditions: 1. both two corners from Line-end, Z-shape, or flag-shape) Definition of Line-end [both width ≤ 0.060 µm between 2 consecutive 90-90 degree corners] Definition of Z-shape/flag-shape follows My.S.2.1.1	S6	≥	0.0760
My.S.6.1	Corner projected space in NMINP direction [-0.038 µm < PRL ≤ 0 µm in MINP direction]	S6	≥	0.0760
My.S.6.2	Corner projected space of My [width ≥ 0.240 µm, -0.160 µm < PRL ≤ 0 µm]	S6	≥	0.1600

Rule No.	Description	Label	Op.	Rule
My.S.8	Space of My edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > 0.080 μm] [at least one My width \geq 0.152 μm in MINP direction]	SM	\geq	0.1140
My.S.8.0.1	Space of My edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > -0.030 μm] [at least one My width \geq 0.152 μm in MINP direction] (Except following conditions: 1. Space between Z-Z-shape, Z-flag-shape, flag-/flag-shape, Z-shape/My [width < 0.152 μm in MINP direction], flag-shape/My [width < 0.152 μm in MINP direction]) Definition of Z-shape(flag-shape follows My.S.2.1.1)	SM	\geq	0.0760
My.S.8.0.2	Space of My edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > 0 μm] [at least one My width \geq 0.152 μm in MINP direction and enclosure of Lower_VIA < 0.030 μm]	SM	\geq	0.1140
My.S.8.1	Space of My edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > 0.080 μm] [at least one My width \geq 0.152 μm in NMINP direction]	SN	\geq	0.1300
My.S.8.1.1	Space of My edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > -0.030 μm] [at least one My width \geq 0.152 μm in NMINP direction]	SN	\geq	0.0760
My.S.8.1.2	Space of My edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > 0 μm] [at least one My width \geq 0.152 μm in NMINP direction and enclosure of Lower_VIA < 0.030 μm]	SN	\geq	0.1140
My.S.11	Space of My edge [edge length > 0.080 μm in NMINP direction] in MINP direction [PRL > 0.120 μm] [at least one My width \geq 0.201 μm in MINP direction] (Except following conditions: 1. both two corners from Z-shape, or flag-shape, 2. Space to DMy_O) Definition of Z-shape follows My.S.2.1.1	SM	\geq	0.1450
My.S.11.1	Space of My edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > 0.080 μm] [at least one My width \geq 0.190 μm in NMINP direction] (Except following conditions: 1. Space to DMy_O)	SN	\geq	0.1500
My.S.11.2	Space to My [width \geq 0.231 μm , PRL > 0.120 μm]	SM/SN	\geq	0.1600
My.S.11.3	Space to My [width \geq 0.280 μm , PRL > 0.160 μm]	SM/SN	\geq	0.2000
My.S.15	Space to My [width > 1.350 μm , PRL > 1.350 μm]	SM/SN	\geq	0.4500
My.S.15®	Recommended space [at least one metal line width > 1.350 μm]	SN	\geq	0.4500
My.S.16	Space to My line-end [edge length = 0.038 μm between 2 consecutive 90-90 degree corners, PRL > -0.038 μm] in NMINP direction	S16	\geq	0.0900
My.S.16.0	Space to My line-end [edge length = 0.058 μm between 2 consecutive 90-90 degree corners, PRL > -0.058 μm] in NMINP direction	S16	\geq	0.0900
My.S.16.1	Space to My line-end [edge length = 0.076 μm between 2 consecutive 90-90 degree corners, PRL > -0.076 μm] in NMINP direction	S16A	\geq	0.0760
My.S.16.2	Space to My line-end [edge length = 0.076 μm between 2 consecutive 90-90 degree corners, PRL > -0.076 μm , both adjacent edge length > 0.090 μm] in MINP direction	S16B	\geq	0.1000
My.S.17	Space to My line-end [edge length = 0.040 μm between 2 consecutive 90-90 degree corners, PRL > -0.040 μm] in NMINP direction	S17	\geq	0.0900
My.S.17.1	Space to My line-end [edge length = 0.060 μm between 2 consecutive 90-90 degree corners, PRL > -0.040 μm] in NMINP direction	S17	\geq	0.0900
My.S.17.2	Space to My line-end [edge length = 0.080 μm between 2 consecutive 90-90 degree corners, PRL > -0.080 μm] in NMINP direction	S17B	\geq	0.0800
My.S.17.3	Space to My line-end [edge length = 0.080 μm between 2 consecutive 90-90 degree corners, PRL > -0.080 μm] in MINP direction	S17C	\geq	0.1000
My.S.18	Space to 45-degree bent My [PRL > 0 μm] (Except SEALRING_ALL)	S18	\geq	0.4000
My.S.18.1	Space to 45-degree bent My (Except SEALRING_ALL)	S18A	\geq	0.1400

Rule No.	Description	Label	Op.	Rule
My.S.19	Space to VIAy-1 or VIAy/VIAyz/VIAyy/VIAz [maximum delta V > 0.96V]	S19	\geq	0.0460
My.S.19.1	Space to VIAy-1 or VIAy/VIAyz/VIAyy/VIAz [maximum delta V > 1.32V] (1.2V + 10%)	S19	\geq	0.0600
My.S.19.1.1	Space to VIAy-1 or VIAy/VIAyz/VIAyy/VIAz [maximum delta V > 1.98V] (1.8V + 10%)	S19	\geq	0.0800
My.S.20	Space to My [maximum delta V > 1.98V] (1.8V + 10%)	S20	\geq	0.0460
My.S.20.1	Space to My [maximum delta V > 2.75V] (2.5V + 10%)	S20	\geq	0.0800
My.S.22	Space to the edge of concave corner in MINP direction (Except following conditions: 1. Edge length between 2 concave corner < 0.114 μm 2. Either one edge length of concave corner \leq 0.040 μm 3. 45-degree My) DRC flags My overlap Concave_My_Area Definition of Concave_My_Area: A rectangle [0.114 μm x 0.200 μm] abut both edge of My concave corner	S22	\geq	0.1140
My.S.27	Forbidden space of My in MINP direction [PRL > 0 μm] [one side is My [width = 0.038 μm and one side space = 0.038 μm (W1)] the other side is My [width < 0.076 μm (W2)]]. (Except following conditions: 1. both side of My [width < 0.076 μm (W2)] to My space > 0.095 μm) DRC checks space of My drawing pattern only	S27	=	0.1150~0.1890
My.S.27.1	Forbidden space of My in MINP direction [PRL > 0 μm] [one side is My [width = 0.040 μm and one side space = 0.040 μm (W1)] the other side is My [width < 0.080 μm (W2)]]. (Except following conditions: 1. both side of My [width < 0.080 μm (W2)] to My space > 0.099 μm) DRC checks space of My drawing pattern only	S27A	=	0.1300~0.1790
My.EN.0	Enclosure of square VIAy-1 is defined by one of My.EN.1, My.EN.1.0, My.EN.1.2, My.EN.1.2.1, or My.EN.1.3, My.EN.1.3.1, or My.EN.1.4 or Enclosure of rectangular VIAy-1 is defined by My.EN.4 or My.EN.4.1 or My.EN.5 or My.EN.5.1 or My.EN.5.2 or My.EN.5.3, My.EN.5.11.1, My.EN.5.11.2, My.EN.5.11.3 Note: 1. DRC only checks the VIAy-1 which overlaps the metal width of corresponding rule 2. DRC checks My.EN.1.4, My.EN.1.3, My.EN.1.3.1, My.EN.1, My.EN.1.2, in sequence 3. DRC checks My.EN.5.3, My.EN.5.2, My.EN.5.1, My.EN.5.11.3, My.EN.5, My.EN.5.11.1, My.EN.4 in sequence			
My.EN.1	Enclosure of square VIAy-1 [width = 0.038 μm] by My [width = 0.038 μm] for two opposite sides with the other two sides \geq 0.050 μm	EN1	\geq	0
My.EN.1.0	Enclosure of square VIAy-1 [width = 0.038 μm] by My [width = 0.058 μm] for two opposite sides with the other two sides \geq 0.050 μm	EN1	\geq	0.0100
My.EN.1.2	Enclosure of square VIAy-1 [width = 0.038 μm] by My [width = 0.040 μm] for two opposite sides with the other two sides \geq 0.050 μm	EN1B	\geq	0.0010
My.EN.1.2.1	Enclosure of square VIAy-1 [width = 0.038 μm] by My [width = 0.060 μm] for two opposite sides with the other two sides \geq 0.050 μm	EN1K1	\geq	0.0110
My.EN.1.3	Enclosure of square VIAy-1 [width = 0.038 μm] by My [width = 0.076 μm] for all sides	EN1C	\geq	0.0190
My.EN.1.3.1	Enclosure of square VIAy-1 [width = 0.038 μm] by My [width = 0.080 μm] for all sides	EN1C	\geq	0.0210
My.EN.1.4	Enclosure of square VIAy-1 [width = 0.038 μm] by My [width > 0.080 μm] for two opposite sides with the other two sides \geq 0.030 μm	EN1D	\geq	0.0200
My.EN.2.0	Enclosure of square VIAy-1 [width = 0.058 μm] by My [width = 0.058 μm] for two opposite sides with the other two sides \geq 0.054 μm	EN2	\geq	0
My.EN.2.2.1	Enclosure of square VIAy-1 [width = 0.058 μm] by My [width = 0.060 μm] for two opposite sides with the other two sides \geq 0.054 μm	EN2K1	\geq	0.0010

Rule No.	Description	Label	Op.	Rule
My.EN.2.3	Enclosure of square VIAy-1 [width = 0.058 μm] by My [width = 0.076 μm] for two opposite sides with the other two sides ≥ 0.047 μm	EN2C	≥	0.0090
My.EN.2.3.1	Enclosure of square VIAy-1 [width = 0.058 μm] by My [width = 0.080 μm] for two opposite sides with the other two sides ≥ 0.047 μm	EN2C	≥	0.0110
My.EN.2.4	Enclosure of square VIAy-1 [width = 0.058 μm] by My [width > 0.080 μm] for two opposite sides with the other two sides ≥ 0.040 μm	EN2D	≥	0.0280
My.EN.4	Short side enclosure of rectangular VIAy-1 by My [width = 0.038 μm] with the other two long side enclosure ≥ 0 μm	EN4	≥	0.0500
My.EN.4.1	Enclosure of short side of rectangular VIAy-1 by My [width = 0.058 μm] with the other two long side enclosure ≥ 0.010 μm	EN4	≥	0.0500
My.EN.5	Enclosure of rectangular VIAy-1 by My [width = 0.076 μm] for all sides	EN5	≥	0.0190
My.EN.5.1	Enclosure of rectangular VIAy-1 by My [width ≥ 0.114 μm] for two opposite sides with the other two sides ≥ 0.030 μm (Except following conditions: 1. rectangular VIAy-1 array)	EN5A	≥	0.0200
My.EN.5.2	Short side enclosure of rectangular VIAy-1 by My [width ≥ 0.114 μm] with the other two long side enclosure ≥ 0.038 μm (Except following conditions: 1. rectangular VIAy-1 array)	EN5B	≥	0.0070
My.EN.5.3	Enclosure of rectangular VIAy-1 array for two opposite sides with the other two sides [rectangular VIAy-1 array edge length = 0.100 μm] ≥ 0.016 μm Definition of rectangular VIAy-1 array: VIAy-1 long side space = 0.082 μm [PRL = 0.100 μm]	EN5C	≥	0.0070
My.EN.5.11.1	Enclosure of short side of rectangular VIAy-1 by My [width = 0.040 μm] with the other two long side enclosure ≥ 0.001 μm	EN5K1	≥	0.0500
My.EN.5.11.2	Enclosure of short side of rectangular VIAy-1 by My [width = 0.060 μm] with the other two long side enclosure ≥ 0.011 μm	EN5K1	≥	0.0500
My.EN.5.11.3	Enclosure of rectangular VIAy-1 by My [width = 0.080 μm] for all sides	EN5K3	≥	0.0210
My.EN.10	Enclosure of square or rectangular VIAy-1 by My edge [between 2 consecutive 90-270 degree corners, length < 0.152 μm]	EN10	≥	0.0300
My.EN.10.1	Enclosure of square or rectangular VIAy-1 for two opposite sides with the other side enclosure < 0.038 μm [edge length < 0.152 μm between 2 consecutive 90-270 degree corners]	EN10A	≥	0.0380
My.L.1	Length of 45-degree bent My (minimum edge length)	L1	≥	0.9100
My.L.3	Edge length with adjacent edge [length < 0.090 μm]	L3	≥	0.0760
My.L.3.1	Edge length with adjacent edge [length < 0.038 μm]	L3	≥	0.1140
My.L.3.2	Edge length with adjacent line-end edge [length < 0.060 μm (L), between 2 consecutive 90-90 degree corners]	L3B	≥	0.1600
My.L.3.3	Edge length with adjacent line-end edge [length < 0.076 μm (L), between 2 consecutive 90-90 degree corners]	L3B	≥	0.1100
My.L.3.4	At least one adjacent edge of My edge [length < 0.090 μm]	L3D	≥	0.1100
My.L.4	U-shape edge length [between 2 consecutive 270-270 degree corners]	L4	≥	0.0760
My.L.5	Edge length [between 2 consecutive 90-270 degree corners]	L5	≥	0.0190
My.L.6	Length of My branch [width < 0.270 μm] with one square VIAy-1/VIAy/VIAyz/VIAYy/VIAz within the distance ≤ 1.556 μm (L6) from My plate [both width (W) and length (L) > 0.400 μm] DRC flags branch that can't enclose a 0.076 μm X 1.556 μm orthogonal rectangle	L6	≥	1.556
My.L.6.1	Length of My branch [width < 0.270 μm] with one square VIAy-1/VIAy/VIAyz/VIAYy/VIAz within the distance ≤ 3.671 μm (L6) from My plate [both width (W) and length (L) > 0.900 μm] DRC flags branch that can't enclose a 0.076 μm X 3.671 μm orthogonal rectangle	L6	≥	3.671
My.L.6.2	Length of My branch [width < 0.270 μm] with one square VIAy-1/VIAy/VIAyz/VIAYy/VIAz within the distance ≤ 9.071 μm (L6) from My plate [both width (W) and length (L) > 1.35 μm] DRC flags branch that can't enclose a 0.076 μm X 9.071 μm orthogonal rectangle	L6	≥	9.071

Rule No.	Description	Label	Op.	Rule
My.L.7	My edge length (L7) between consecutive 90-270 degree corners with adjacent edge in line-end [width < 0.076 μm] and another adjacent edge > 0.070 μm (Except following conditions: 1. edge length (L7) ≤ 0.070 μm)	L7	≥	0.2400
My.A.1	Area	A1	≥	0.01500
My.A.1®	Recommended area (Except DMy_O)	A1	≥	0.02200
My.A.3	Area [with all of edge lengths < 0.117 μm] (Except following conditions: 1. a pattern filling 0.050 μm x 0.130 μm tile)	A3	≥	0.04000
My.A.4	Enclosed area	A4	≥	0.18200
My.DN.1.1	Minimum All_metal density in window 50 μm x 50 μm, stepping 25 μm (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	10%
My.DN.1.2	Minimum All_metal density in window 50 μm x 50 μm, stepping 25 μm [3 μm x 3 μm empty area exists in the window] (Except LOGO, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	25%
My.DN.2	Maximum metal density in window 50 μm x 50 μm, stepping 25 μm (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, DMy, DMy_O)		≤	65%
My.DN.2.3	Maximum {{My OR DMy_O} OR DMy} density in window 50 μm x 50 μm, stepping 25 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	75%
My.DN.3.1	The metal density difference between any two neighboring checking windows including DMnEXCL [window 180 μm x 180 μm, stepping 180 μm] (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	50%
My.DN.6.1	Metal density [window 9 μm x 9 μm, stepping 4.5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. the maximum area of the merged low density windows [density < 1%] ≤ 5184 μm², while the merged low density windows width is > 27 μm, 2. the maximum area of the merged low density windows [density < 1%] ≤ 14580 μm², 3. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
My.DN.7	It is not allowed to have local density < 5% of all 3 consecutive metal (My, My+1, and My+2) over any 27 μm x 27 μm (stepping 13.5 μm), i.e. it is allowed for either one of My, My+1, or My+2 to have a local density ≥ 5% (The metal layers include My/My+1/My+2 and dummy metals for ELK film) (Except ICOVL_SINGLE, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc, 2. TCDDMY_Mn (assume 45% pattern density INSIDE TCDDMY_Mn))			
My.DN.5.1®	Recommended minimum metal density in window 25 μm x 25 μm, stepping 12.5 μm (Except LOGO, INDDMY, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE)		≥	30%
My.DN.6.1®	Recommend metal density for IP level [window 10 μm x 10 μm, stepping 5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. the maximum area of the merged low density windows [density < 1%] ≤ 1600 μm², while the merged low density windows width is > 30 μm, 2. the maximum area of the merged low density windows [density < 1%] ≤ 4500 μm², 3. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%

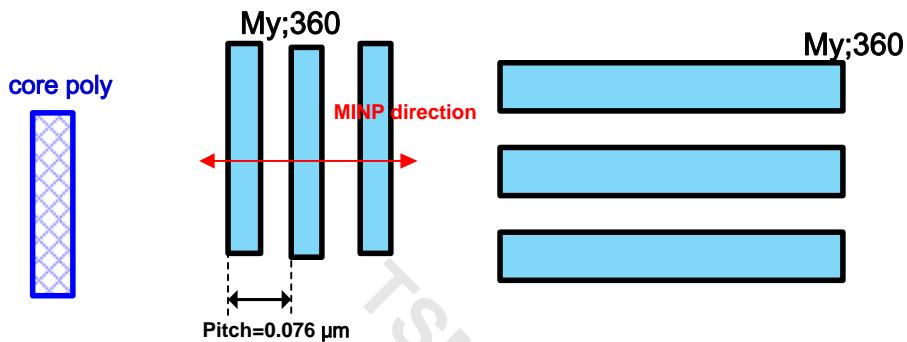
Rule No.	Description	Label	Op.	Rule
My.DN.8®	Recommended maximum metal density in window 25 µm x 25 µm, stepping 12.5 µm (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	60%
My.R.1 ^U	My line-end must be rectangular. Other shapes are not allowed			
My.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
My.R.4®	Recommended maximum stacked M1, Mx, Mxa, Mya and My layers of high density area [density > 70% in window 800 µm x 800 µm, stepping 80 µm]		≤	4
My.R.6	Datatype 350 and 360 exist on the same metal layer at the same time is not allowed			
My.R.6.1	Same datatype (350 or 360) in both My and My-1 at the same time is not allowed Same datatype (351 or 361) in both My and My-1 at the same time is not allowed; Same datatype (357 or 367) in both My and My-1 at the same time is not allowed.			
My.R.6.2	Consecutive My datatype (350 or 351 or 357) and Mya datatype (330 or 331 or 337) exist at the same time is not allowed; Consecutive My datatype (360 or 361 or 367) and Mya datatype (340 or 341 or 347) exist at the same time is not allowed.			
My.R.7	My must follow either one of the conditions. 1. {Checked_My AND Dense_Region_My} must be projected [PRL ≥ 0 µm] to another two {My AND Dense_Region_My} at both sides in MINP direction, or 2. There is no other {My OVERLAP Iso_Region_My} and simultaneously {Checked_My AND Iso_Region_My} can't be projected [PRL ≥ 0 µm] to {Checked_My AND Iso_Region_My} at four sides. Definition of Checked_Lower_VIA: Lower_VIA [enclosure by My < 0.001 µm and enclosure by Lower_Metal < 0.065 µm at the same time] Definition of Checked_My: {My OVERLAP Checked_Lower_VIA} Definition of Dense_Region_My: A rectangle formed by Checked_Lower_VIA edge expanding 0.039 µm in MINP direction Definition of Iso_Region_My: A rectangle formed by Checked_Lower_VIA edge expanding 0.076 µm in MINP direction and expanding 0.300 µm in NMINP direction DRC checks My drawing pattern only			
My.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of My space to My or VIAy-1 or VIAy is < 0.360 µm			
My.R.17	DMy is a must in chip level.			

Table Notes:

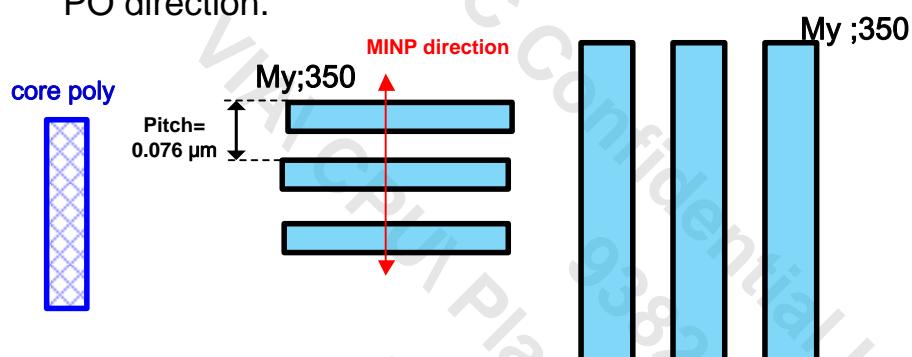
- Please refer to section 3.9 “DRC methodology of net voltage recognition” for delta voltage calculation of high voltage spacing rules.

My

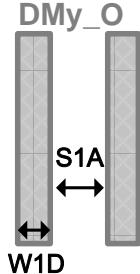
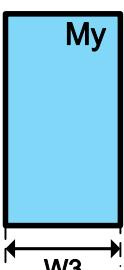
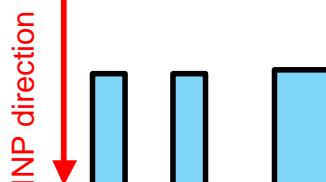
- Data type 360 is used for metal pitch 0.076 μm in perpendicular to core PO direction.



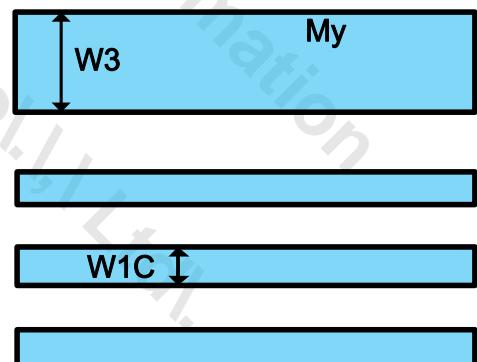
- Data type 350 is used for metal pitch 0.076 μm in parallel to core PO direction.



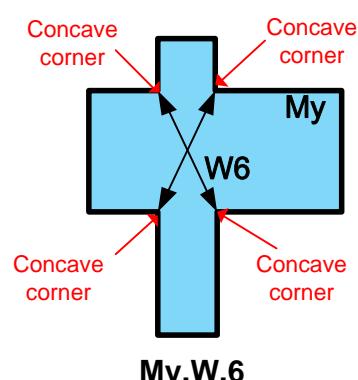
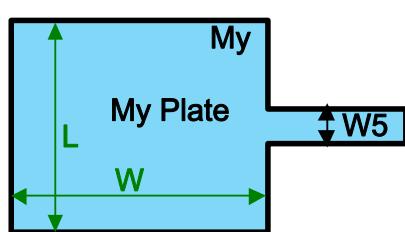
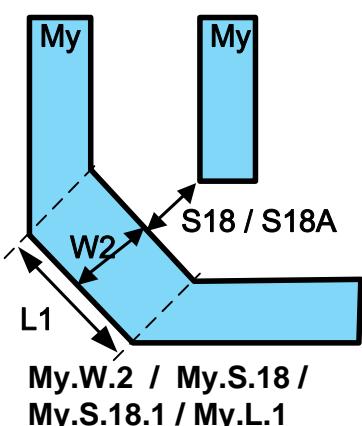
MINP direction

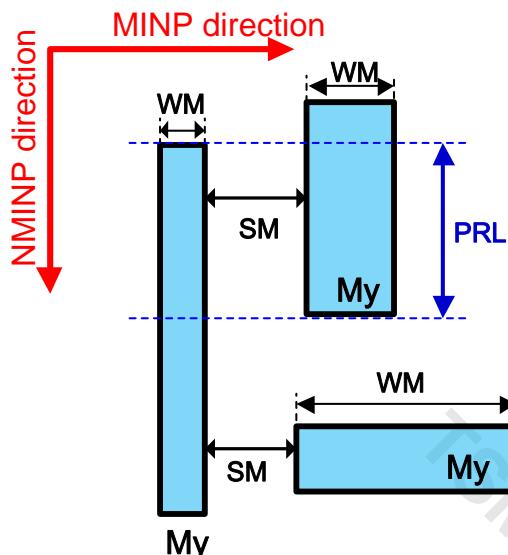


My.W.1 / My.W.1.1 / My.W.1.4 /
My.W.3 / My.S.1 / My.S.1.1



My.W.1.3 / My.W.3





My.S.2.1.1 / My.S.2.1.2 / My.S.2.2.1 / My.S.2.2.2 /
 My.S.2.2.3 / My.S.2.3.1 / My.S.2.3.2 / My.S.2.3.2.1 /
 My.S.2.3.3 / My.S.2.4.1 / My.S.2.4.2 / My.S.2.4.3 /
 My.S.2.11.1 / My.S.2.11.2 / My.S.2.12.1 /
 My.S.2.12.2 / My.S.2.12.3 / My.S.2.12.4 /
 My.S.2.13.1 / My.S.2.13.2 / My.S.2.13.3 /
 My.S.2.14.1 / My.S.2.14.2 / My.S.8 / My.S.11 /
 My.S.11.2 / My.S.11.3 / My.S.15/ My.S.15®

MINP	Width / Space Table (unit: μm)														
Width (WM)	0.038	0.040	0.058	0.060	0.076	0.080	0.114	0.120	≥ 0.152	≥ 0.201	≥ 0.231	≥ 0.280	> 1.350	≥ 0.038	≥ 0.240
PRL	> -0.076	> -0.080	> -0.076	> -0.080	> -0.076	> -0.080	> -0.038	> -0.080	> 0.080	> 0.120	> 0.120	> 0.160	> 1.350	-0.076 ~ 0	-0.160 ~ 0
Space (SM)	0.038	0.040	0.047	0.060	0.047	0.060	0.076	0.080	≥ 0.114	≥ 0.145	≥ 0.160	≥ 0.200	≥ 0.450	Corner	Corner
	0.057	0.060	0.056	0.070	0.057	0.080	≥ 0.114	≥ 0.120						projected space ≥ 0.076	projected space ≥ 0.160
	0.066	0.070	0.066	0.100	0.076	0.100									
	0.076	0.080	0.094	≥ 0.120	0.095	≥ 0.120									
	0.095	0.100	≥ 0.114		≥ 0.114										
	≥ 0.114	≥ 0.120													
Related Rule	My.S.2.1.1 ^{#1} My.S.2.1.2 My.S.2.3.2 ^{#1}	My.S.2.11.1 ^{#1} My.S.2.11.2	My.S.2.2.1 My.S.2.2.2	My.S.2.12.1 My.S.2.12.2 My.S.2.12.3 My.S.2.12.4	My.S.2.13.1 ^{#1} My.S.2.13.2 My.S.2.13.3 My.S.2.3.2.1 My.S.2.3.3	My.S.2.4.1 ^{#1} My.S.2.4.2 ^{#1} My.S.2.4.3 ^{#1}	My.S.2.14.1 ^{#1} My.S.2.14.2	My.S.8 ^{#2} My.S.11 ^{#2}	My.S.11.2	My.S.11.3	My.S.15	My.S.6	My.S.6.2		

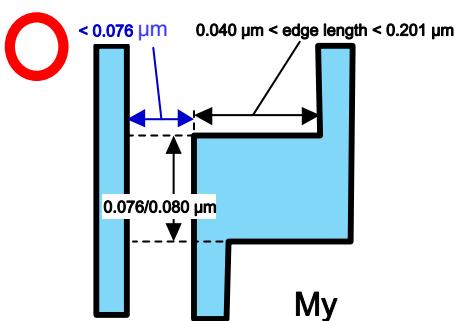
Note:

#1: Except adjacent edge of Z-shape corner, or flag-shape

#2: Except line-end [edge length $\leq 0.080 \mu\text{m}$] space $\geq 0.100 \mu\text{m}$

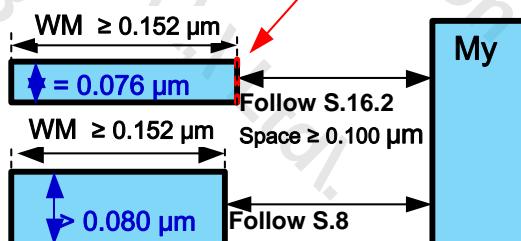
#3: Space of My [width = 0.038/0.076/0.114 μm] to My [width 0.040/0.080 μm] follows My.S.5.4

Note #1 (Z-shape):

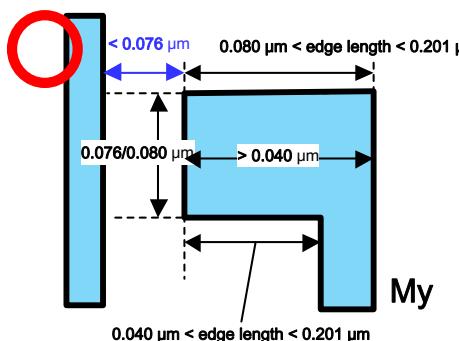


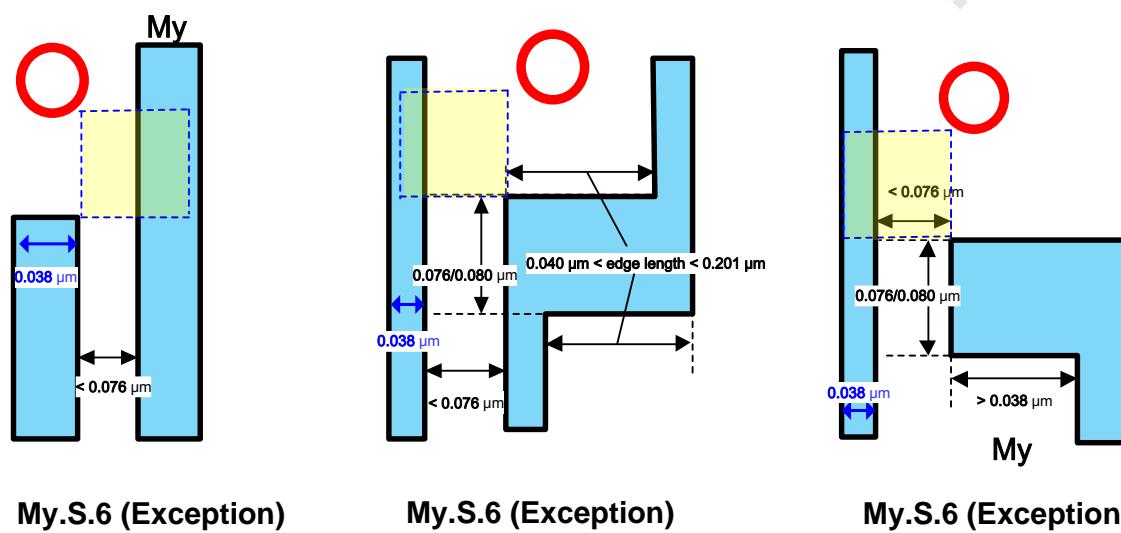
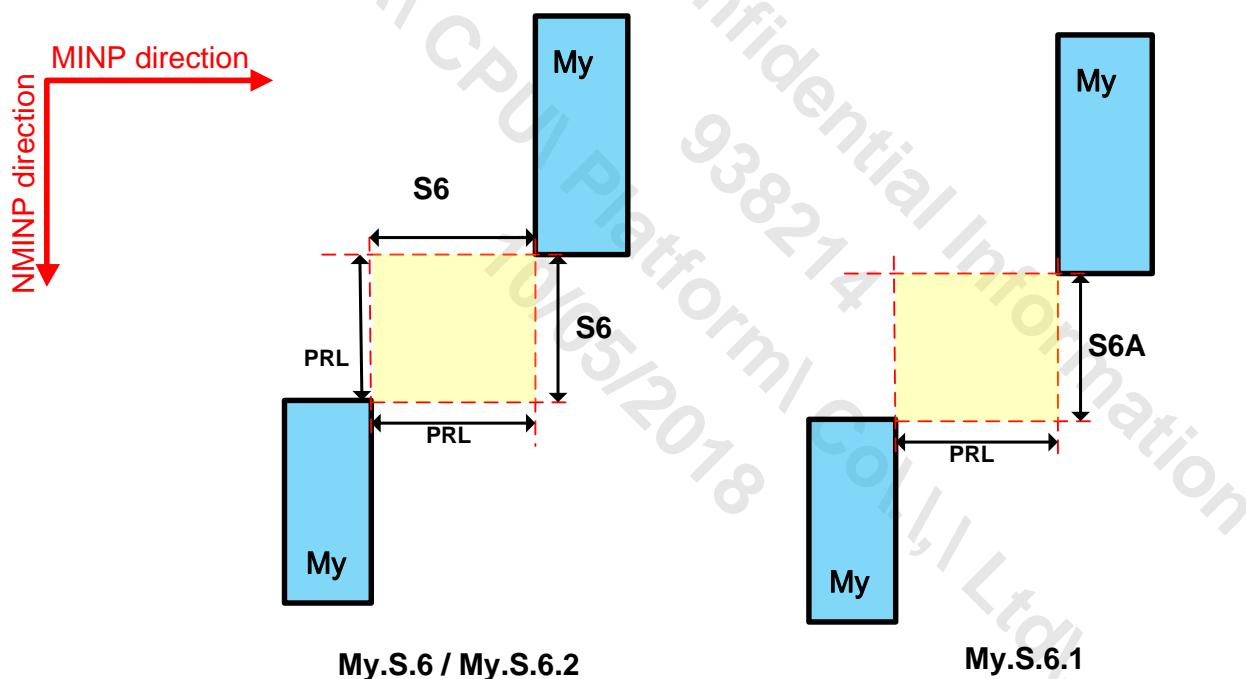
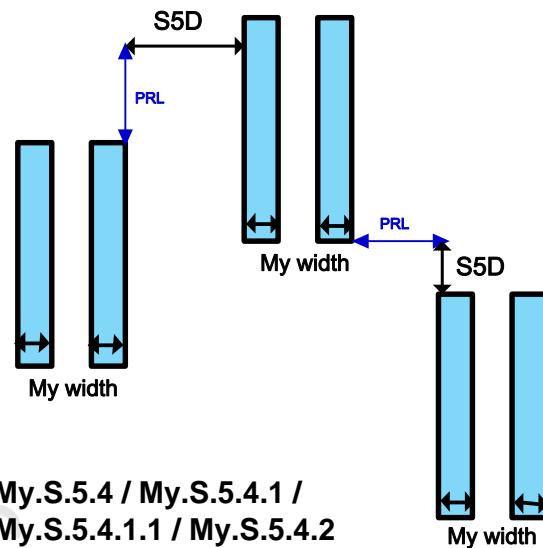
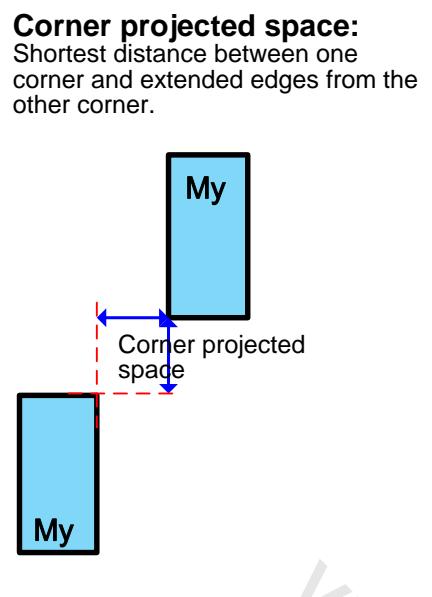
Note #2:

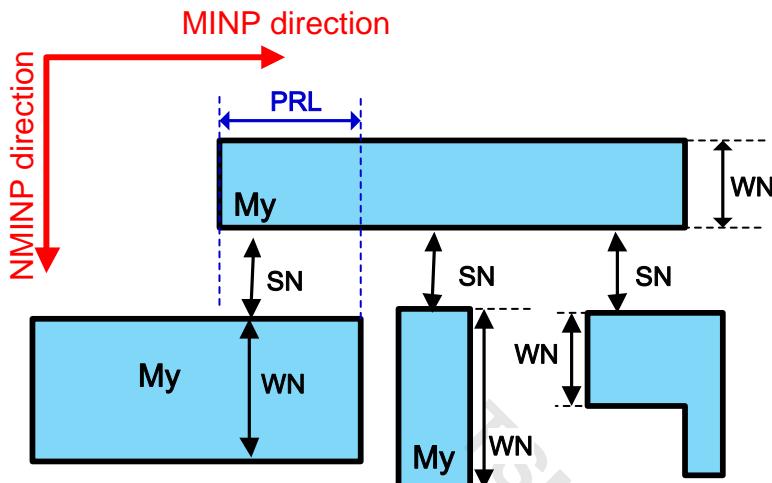
Line end: edge length $\leq 0.080 \mu\text{m}$ between 2 consecutive 90-90 degree corners



Note #1 (flag-shape):







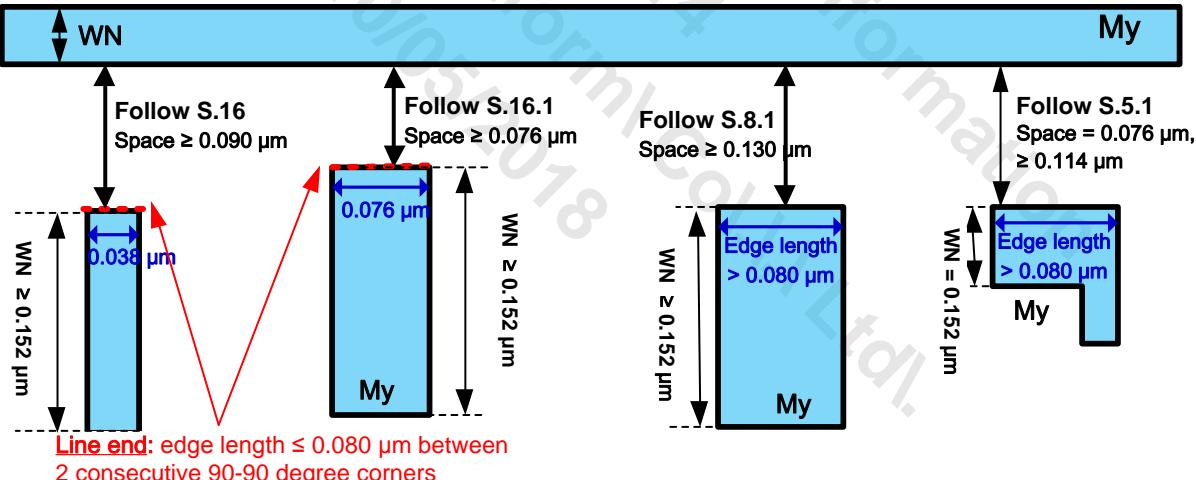
My.S.3.1 / My.S.3.11.1 / My.S.3.11.2 /
My.S.5.1 / My.S.8.1 / My.S.11.1 /
My.S.11.2 / My.S.11.3 / My.S.15/
My.S.15®

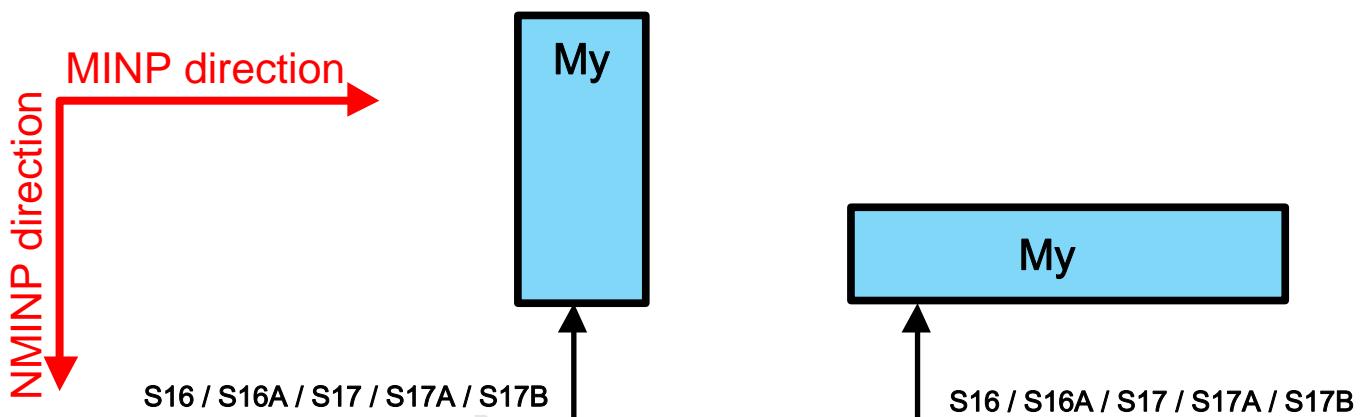
NMINP	Width / Space Table (unit: μm)											
Width (WN)	0.076	0.080	0.114	0.120	≥ 0.152	≥ 0.190	≥ 0.231	≥ 0.280	> 1.350	≥ 0.038	≥ 0.038	≥ 0.240
PRL	> -0.076	> -0.080	> -0.038	> -0.080	> 0.080	> 0.080	> 0.120	> 0.160	> 1.350	$-0.076 \sim 0$	$-0.040 \sim 0$	$-0.160 \sim 0$
Space (SN)	0.076	0.080	≥ 0.114	≥ 0.120	≥ 0.114	≥ 0.120	≥ 0.130	≥ 0.150	≥ 0.200	≥ 0.450	Corner projected space ≥ 0.076	Corner projected space ≥ 0.080
Related Rule	My.S.5.1 ^{#1}	My.S.3.11.1 ^{#1}	My.S.3.1 ^{#1}	My.S.3.11.2 ^{#1}	My.S.8.1 ^{#1}	My.S.11.1 ^{#1}	My.S.11.2	My.S.11.3	My.S.15	My.S.6	My.S.6.1	My.S.6.2

Note:

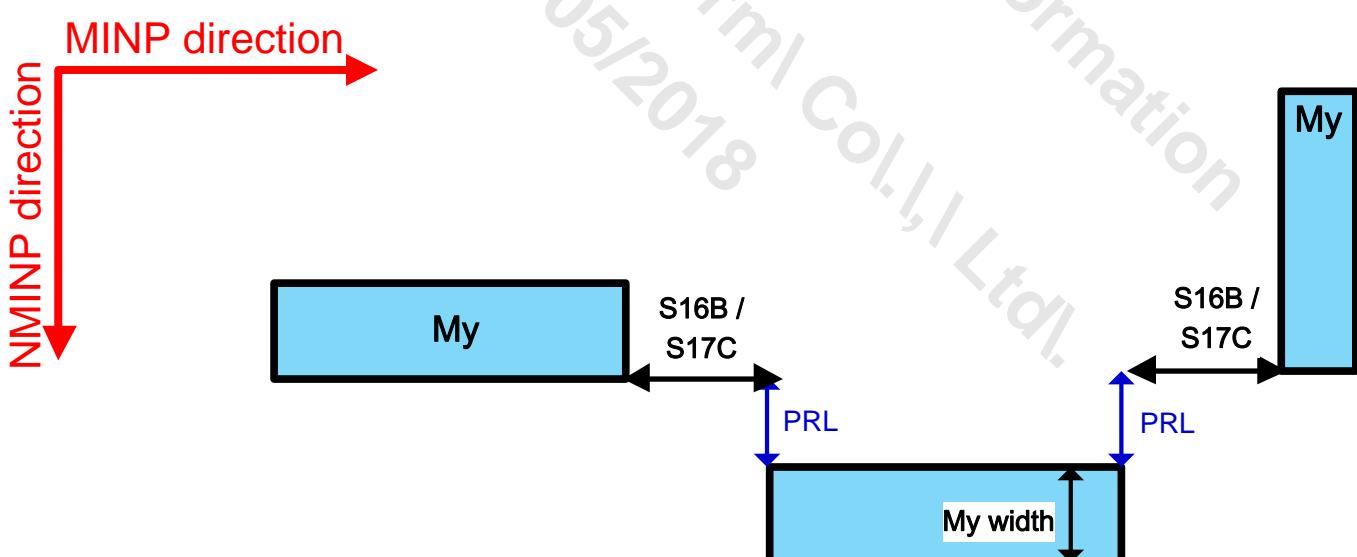
#1: Except line-end [edge length = 0.038 μm] space $\geq 0.090 \mu\text{m}$, line-end [edge length = 0.076 μm] space $\geq 0.076 \mu\text{m}$, line-end [edge length = 0.080 μm] space $\geq 0.080 \mu\text{m}$

Note #1:

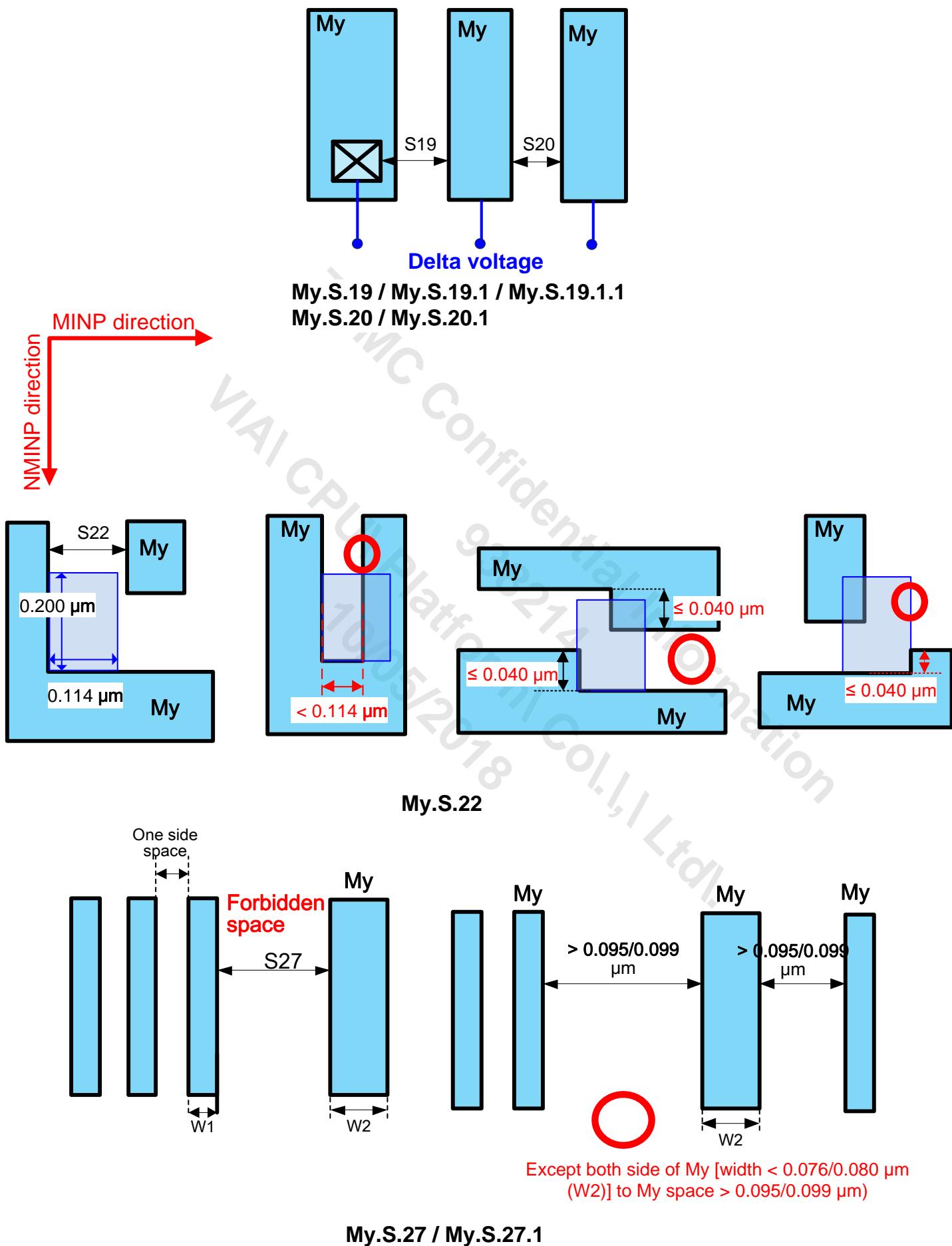




**My.S.16 / My.S.16.0 / My.S.16.1 /
My.S.17 / My.S.17.1 / My.S.17.2**



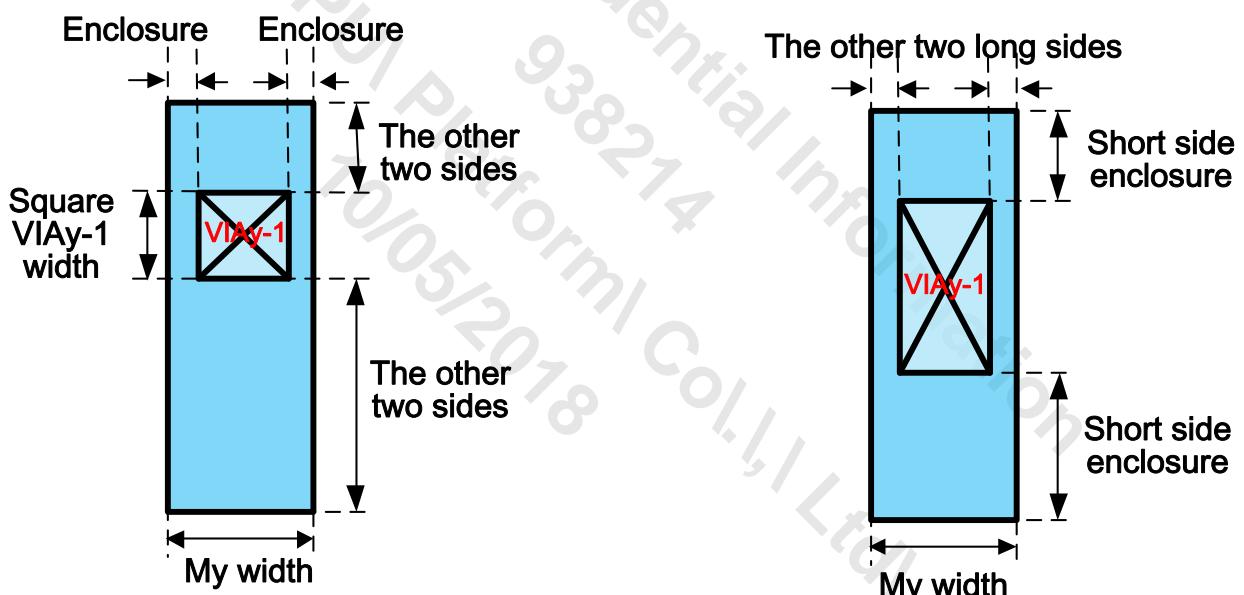
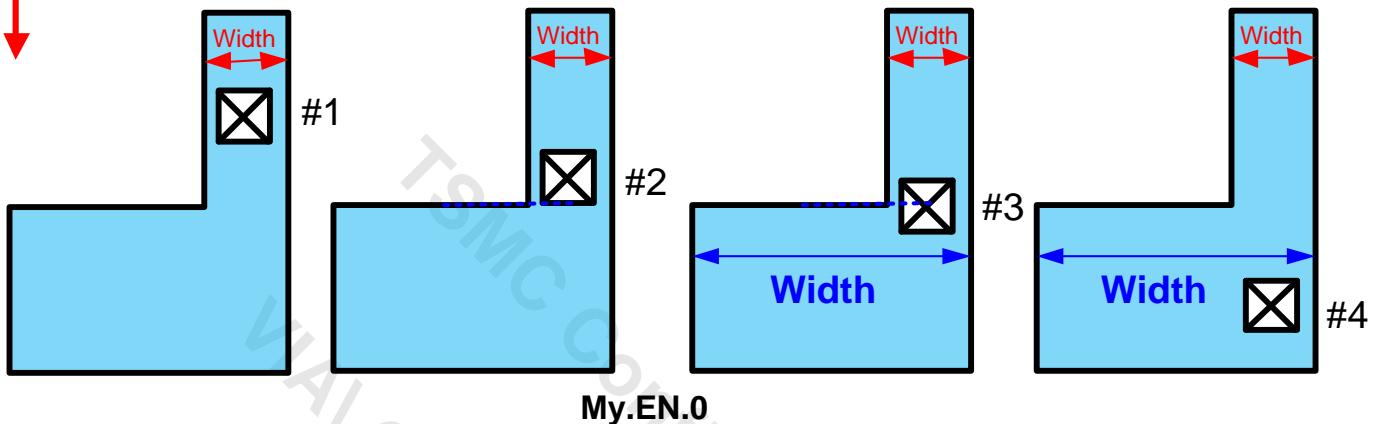
My.S.16.2 / My.S.17.3



MINP direction

NMINP direction

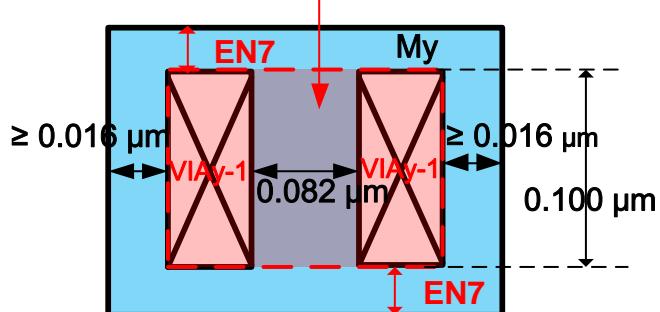
DRC only check the VIA#3 /VIA#4 which overlap the metal width of corresponding rule.



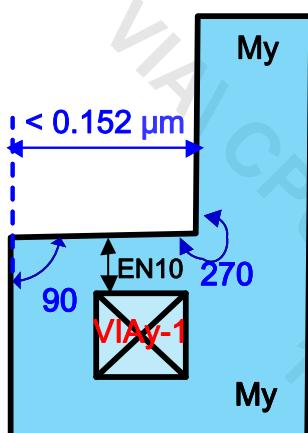
My.EN.1 / My.EN.1.0 / My.EN.1.2 /
 My.EN.1.2.1 / My.EN.1.3 / My.EN.1.3.1 /
 My.EN.1.4 / My.EN.2.0 / My.EN.2.2.1 /
 My.EN.2.3 / My.EN.2.3.1 / My.EN.2.4

My.EN.4 / My.EN.4.1 / My.EN.5 /
 My.EN.5.1 / My.EN.5.2 / My.EN.5.3 /
 My.EN.5.11.1 / My.EN.5.11.2 /
 My.EN.5.11.3

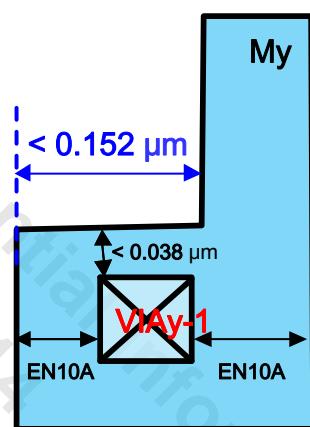
rectangular VIAy-1 array



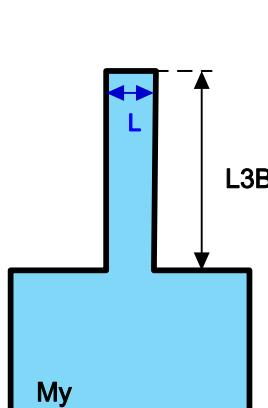
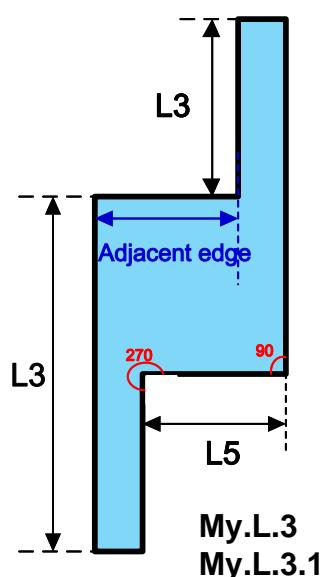
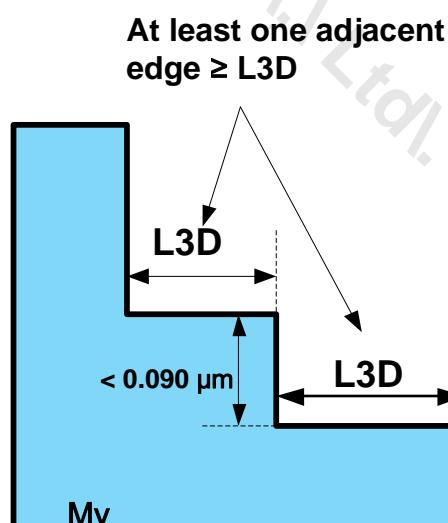
My.EN.5.3



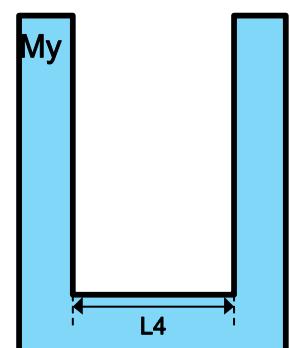
My.EN.10



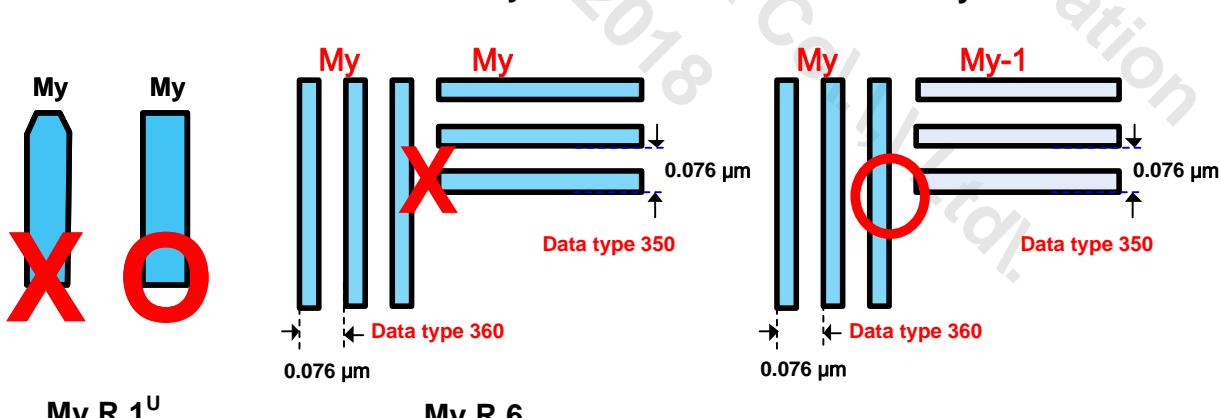
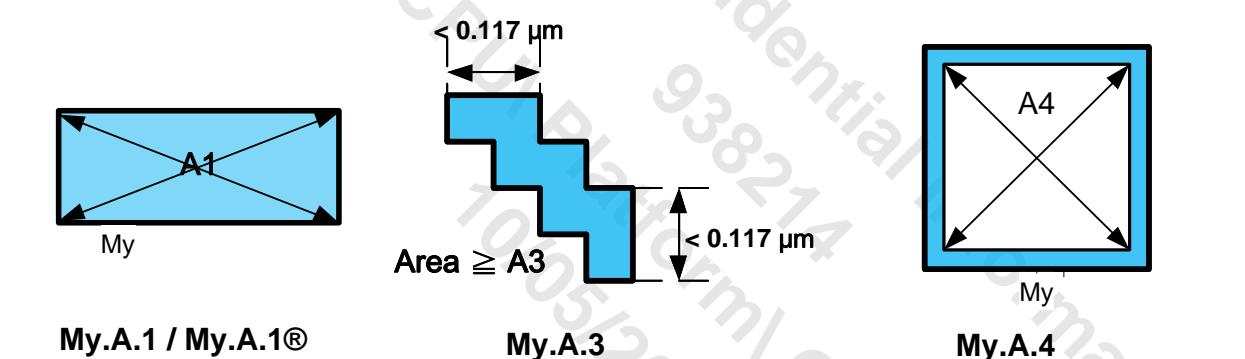
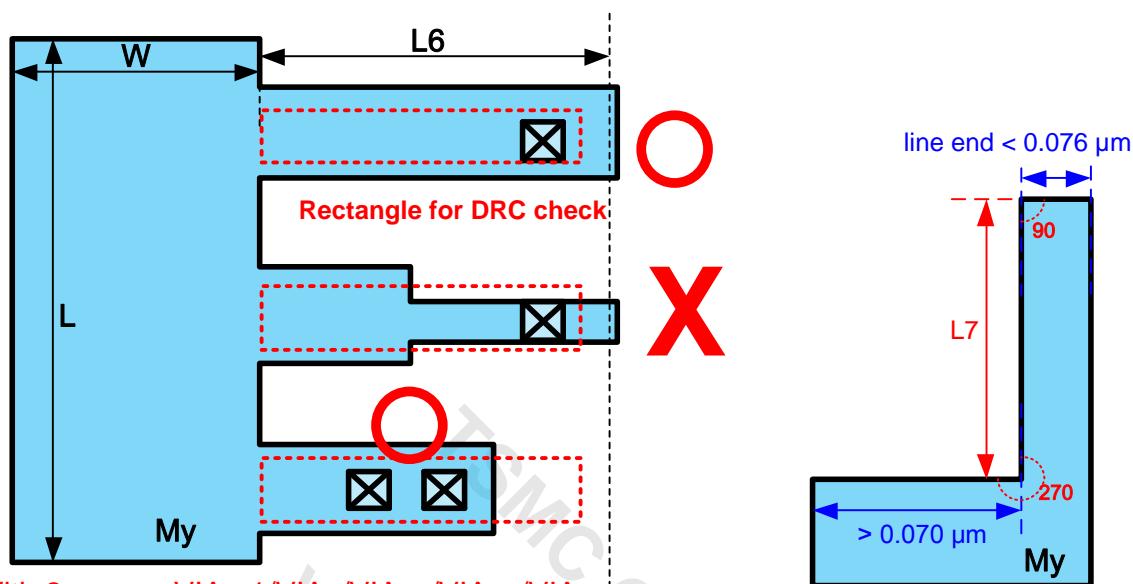
My.EN.10.1

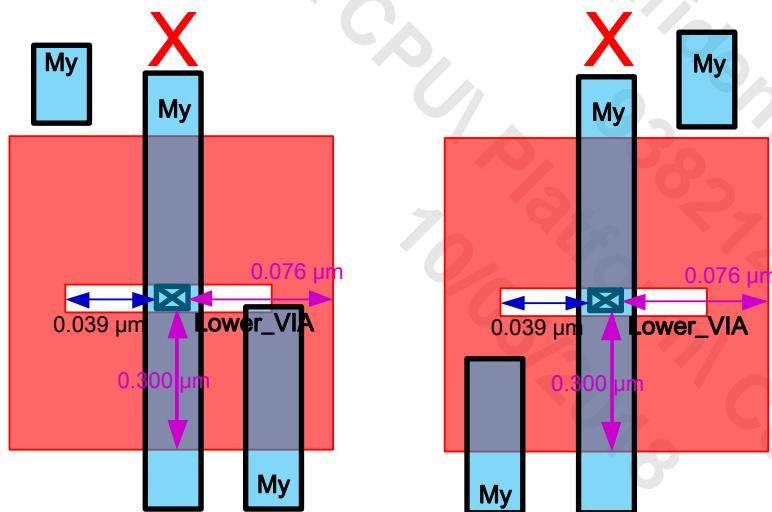
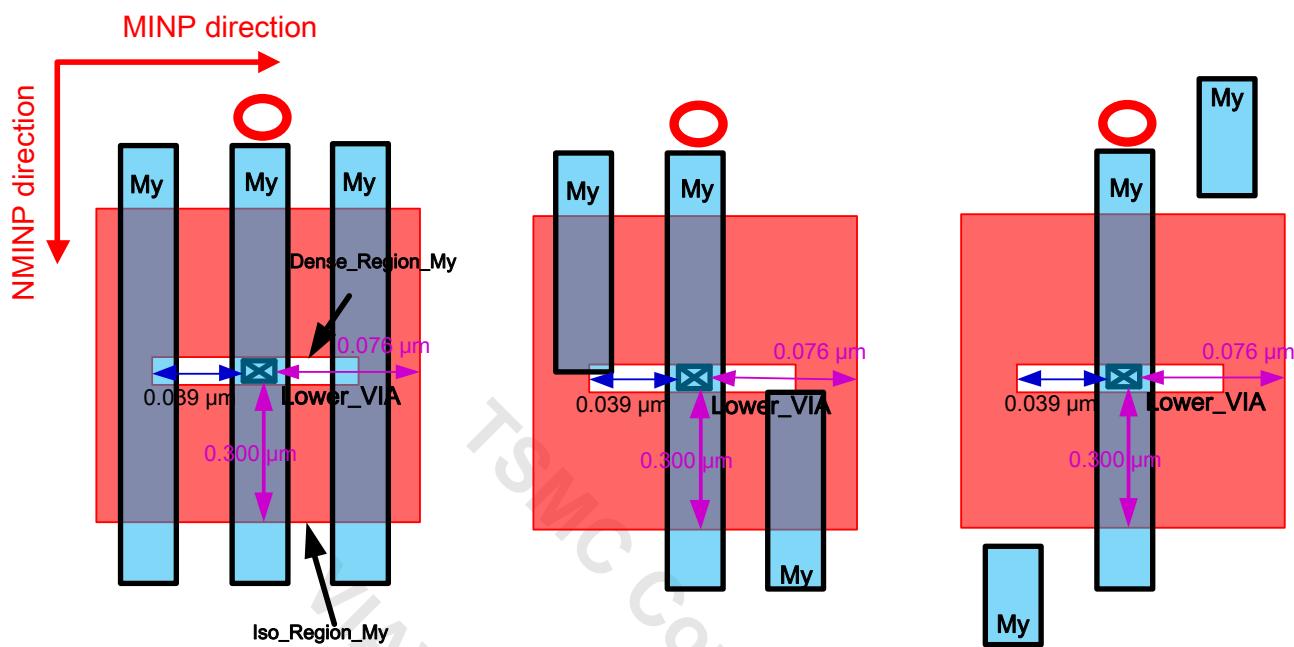
My.L.3.2
My.L.3.3My.L.3.1
My.L.5

My.L.3.4

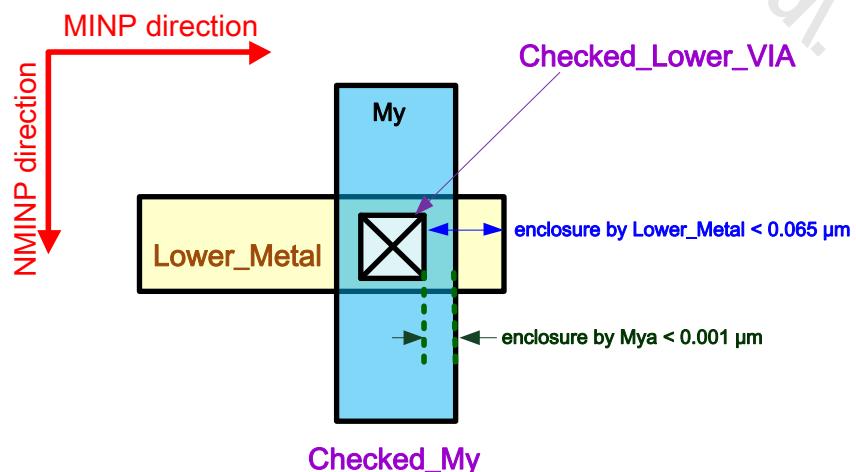


My.L.4





Definition of Checked_Lower_VIA



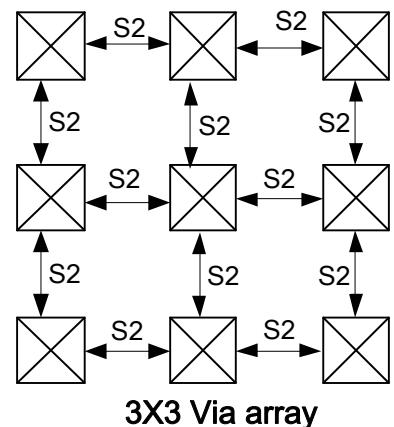
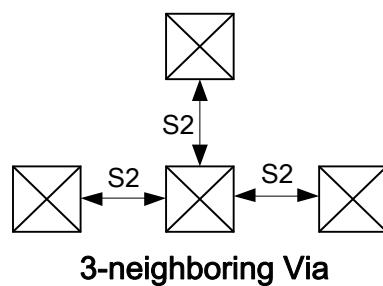
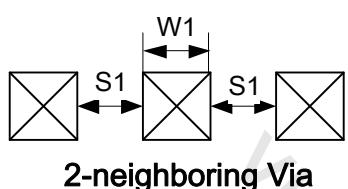
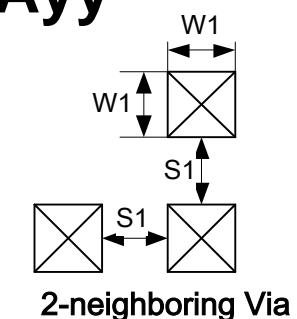
My.R.7

4.5.54 VIAyy Layout Rules

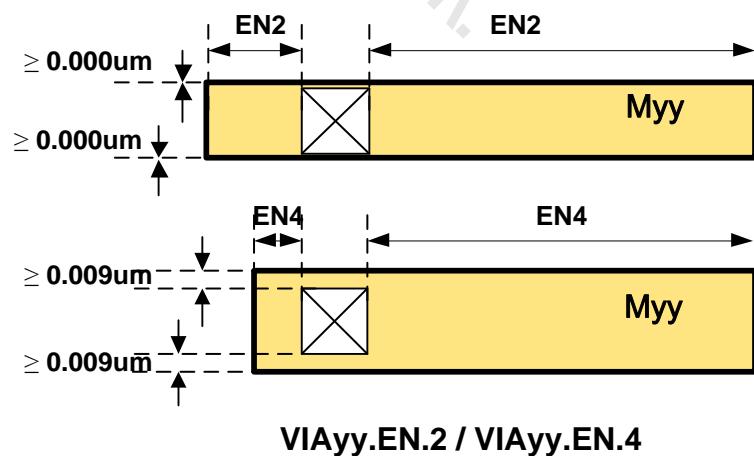
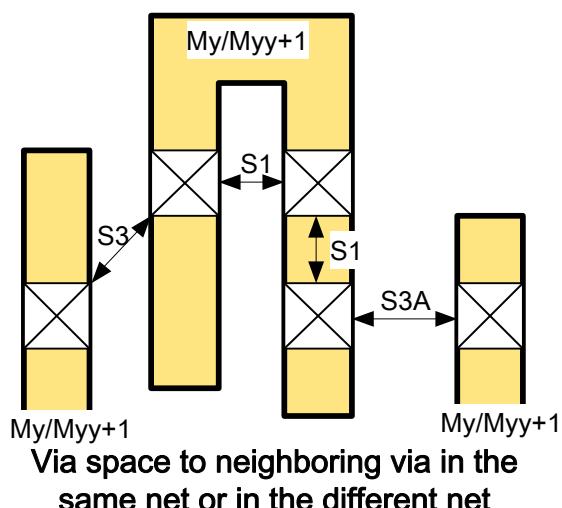
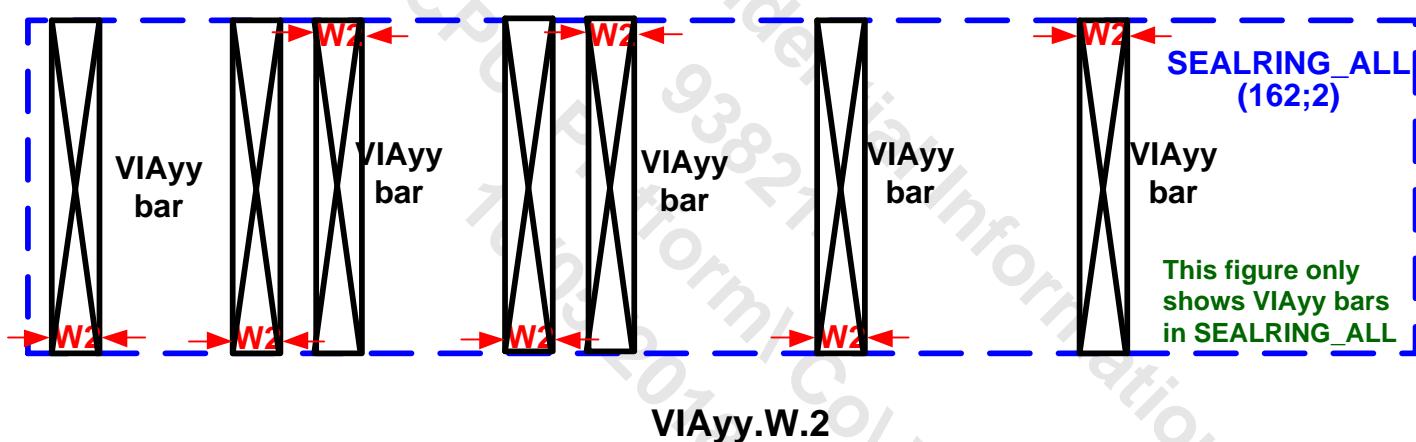
For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

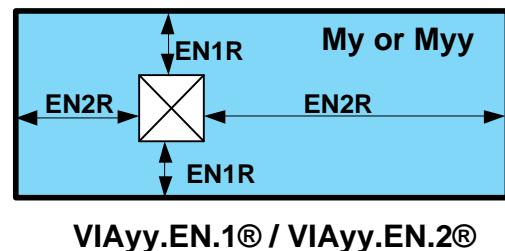
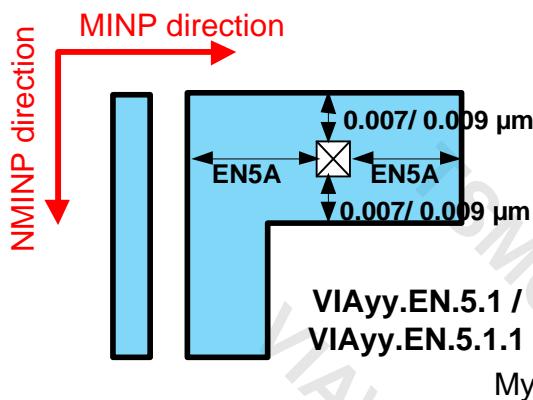
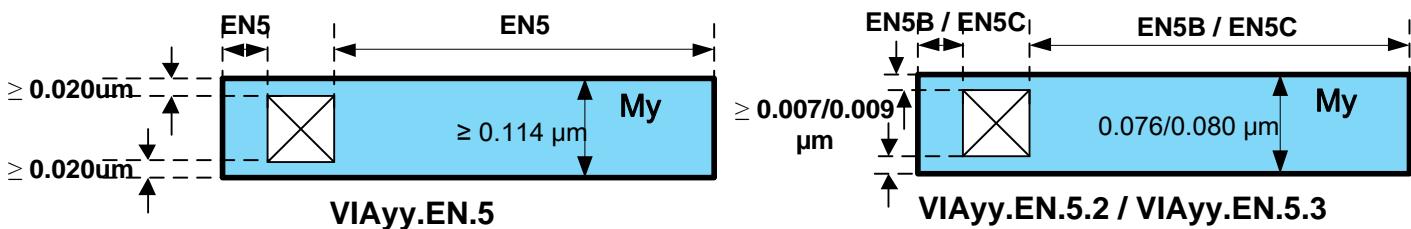
Rule No.	Description	Label	Op.	Rule
VIAyy.W.1	Width (maximum = minimum) (Except SEALRING_ALL)	W1	=	0.0620
VIAyy.W.2	Width of VIAyy bar in SEALRING_ALL	W2	=	0.4500
VIAyy.S.1	Space (Except SEALRING_ALL)	S1	\geq	0.0640
VIAyy.S.2	Space to 3-neighboring VIAyy (distance < 0.089 μm)	S2	\geq	0.0810
VIAyy.S.3	Space to VIAyy [different net]	S3	\geq	0.0860
VIAyy.S.3.1	Space to VIAyy [different net and common PRL > 0 μm]	S3A	\geq	0.0990
VIAyy.EN.0	Enclosure by Myy is defined by VIAyy.EN.2 or VIAyy.EN.4 Enclosure by My is defined by VIAyy.EN.5 or VIAyy.EN.5.1, VIAyy.EN.5.1.1, or VIAyy.EN.5.2, VIAyy.EN.5.3			
VIAyy.EN.2	Enclosure by Myy for two opposite sides with the other two sides $\geq 0 \mu\text{m}$	EN2	\geq	0.0270
VIAyy.EN.4	Enclosure by Myy for two opposite sides with the other two sides $\geq 0.009 \mu\text{m}$	EN4	\geq	0.0180
VIAyy.EN.5	Enclosure by My [width $\geq 0.114 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.020 \mu\text{m}$ (Except SEALRING_ALL, or following conditions: 1. Z-shape, flag-shape) Definition of Z-shape(flag-shape) follows VIAyy.EN.5.1	EN5	\geq	0.0260
VIAyy.EN.5.1	Enclosure by My [Z-shape or flag-shape] for two opposite sides in MINP direction with the other two sides $\geq 0.007 \mu\text{m}$ in NMINP direction Definition: (1) Z-shape [$0.038 \mu\text{m} < \text{edge length} < 0.191 \mu\text{m}$ between 2 consecutive 90-270 degree corners, corresponding width = $0.076 \mu\text{m}$ in NMINP direction between 2 opposite $0.038 \mu\text{m} < \text{edge length} < 0.191 \mu\text{m}$, not including T-shape] (2) flag-shape [$0.038 \mu\text{m} < \text{edge length} < 0.191 \mu\text{m}$ between 2 consecutive 90-270 degree corners, the opposite $0.076 \mu\text{m} < \text{edge length} < 0.191 \mu\text{m}$ between 2 consecutive 90-90 degree corners, corresponding width = $0.076 \mu\text{m}$ in NMINP direction between these 2 opposite edge, and the other corresponding width $> 0.038 \mu\text{m}$ in MINP direction]	EN5A	\geq	0.0260
VIAyy.EN.5.1.1	Enclosure by My [P80_Z-shape or P80_flag-shape] for two opposite sides in MINP direction with the other two sides $\geq 0.009 \mu\text{m}$ in NMINP direction Definition: (1) P80_Z-shape [$0.040 \mu\text{m} < \text{edge length} < 0.201 \mu\text{m}$ between 2 consecutive 90-270 degree corners, corresponding width = $0.080 \mu\text{m}$ in NMINP direction between 2 opposite $0.040 \mu\text{m} < \text{edge length} < 0.201 \mu\text{m}$, not including T-shape] (2) P80_flag-shape [$0.040 \mu\text{m} < \text{edge length} < 0.201 \mu\text{m}$ between 2 consecutive 90-270 degree corners, the opposite $0.080 \mu\text{m} < \text{edge length} < 0.201 \mu\text{m}$ between 2 consecutive 90-90 degree corners, corresponding width = $0.080 \mu\text{m}$ in NMINP direction between these 2 opposite edge, and the other corresponding width $> 0.040 \mu\text{m}$ in MINP direction]	EN5A	\geq	0.0260
VIAyy.EN.5.2	Enclosure by My [width = $0.076 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.007 \mu\text{m}$ (Except following conditions: 1. Z-shape, flag-shape) Definition of Z-shape(flag-shape) follows VIAyy.EN.5.1	EN5B	\geq	0.0500
VIAyy.EN.5.3	Enclosure by My [width = $0.080 \mu\text{m}$] for two opposite sides with the other two sides $\geq 0.009 \mu\text{m}$ (Except following conditions: 1. P80_Z-shape, P80_flag-shape) Definition of P80_Z-shape/ P80_flag-shape follows VIAyy.EN.5.1.1	EN5C	\geq	0.0500
VIAyy.EN.0®	Recommended enclosure by My or Myy is defined by either VIAyy.EN.1® or VIAyy.EN.2® or VIAyy.EN.2.1®			
VIAyy.EN.1®	Recommended enclosure by My or Myy to avoid high Rc	EN1R	\geq	0.0260

Rule No.	Description	Label	Op.	Rule
VIAyy.EN.2®	Recommended enclosure by My [at least two opposite sides] to avoid high Rc	EN2R	≥	0.0450
VIAyy.EN.2.1®	Recommended enclosure by Myy [at least two opposite sides] to avoid high Rc	EN2R	≥	0.0450
VIAyy.R.1	45-degree rotated VIAyy is not allowed			
VIAyy.R.2	At least two VIAyy with space $\leq 0.126 \mu\text{m}$ (S1), or at least four VIAyy with space $\leq 0.567 \mu\text{m}$ (S1') are required to connect My/Myy and Myy+1 when one of these two metals has width and length $> 0.189 \mu\text{m}$ (W1). (Except following conditions: 1. VIA bar)			
VIAyy.R.3	At least four VIAyy with space $\leq 0.126 \mu\text{m}$ (S2), or at least nine VIAyy with space $\leq 0.747 \mu\text{m}$ (S2') are required to connect My/Myy and Myy+1 when one of these two metals has width and length $> 0.495 \mu\text{m}$ (W2). (Except following conditions: 1. VIA bar)			
VIAyy.R.4	At least two VIAyy must be used for a connection that distance $\leq 1.026 \mu\text{m}$ (D) away from a metal plate (either My/Myy or Myy+1) with length $> 0.189 \mu\text{m}$ (L) and width $> 0.189 \mu\text{m}$ (W). (Except following conditions: 1. VIA bar)			
VIAyy.R.5	At least two VIAyy must be used for a connection that distance $\leq 2.52 \mu\text{m}$ (D) away from a metal plate (either My/Myy or Myy+1) with length $> 1.26 \mu\text{m}$ (L) and width $> 1.26 \mu\text{m}$ (W). (Except following conditions: 1. VIA bar)			
VIAyy.R.6	At least two VIAyy must be used for a connection that distance $\leq 6.39 \mu\text{m}$ (D) away from a metal plate (either My/Myy or Myy+1) with length $> 6.3 \mu\text{m}$ (L) and width $> 1.89 \mu\text{m}$ (W). (Except following conditions: 1. VIA bar)			
VIAyy.R.7	VIAyy must be fully covered by {My AND Myy+1} or {Myy AND Myy+1}			
VIAyy.R.8®	Recommended maximum consecutive stacked VIAyy layer, which has only one via for each VIAyy layer to avoid high Rc (It is allowed to stack more than four VIAyy layers if two or more VIAs in each VIAyy layer are on the same metal)		≤	4
VIAyy.R.11	Single VIAyy is not allowed in "H-shape" Myy+1 when all of the following conditions come into existence: (1) The Myy+1 has "H-shape" interact two metal holes: both two metal hole length $\leq 4.5 \mu\text{m}$ (L2) and two metal hole area $\leq 4.05 \mu\text{m}^2$ (2) The VIAyy overlaps on the center metal bar of this "H-shape" Myy+1 (3) The center metal bar length $\leq 0.900 \mu\text{m}$ (L) and the metal bar width $\leq 0.189 \mu\text{m}$			
VIAyy.R.12	VIAyy connected to DMy, DMy_O, DMyy, DMyy_O, DMyy+1, DMyy+1_O is not allowed			
VIAyy.R.13	Maximum area ratio of My/Myy to upper VIAyy in the same net [connects to gate with area $> 10700 \mu\text{m}^2$, and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = $(2.5 \times W \times L_d)$ for ≥ 2 -fin device		≤	350000
VIAyy.R.13.2	Maximum area ratio of I/O gate to single layer VIAyy in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area $\geq 0.25 \mu\text{m}^2$) Definition: Gate area = $(2.5 \times W \times L_d)$ for ≥ 2 -fin device		≤	300000
VIAyy.R.9g ^U	Recommend using redundant VIAs to avoid high Rc wherever layout allows.			

VIAyy

VIAyy.W.1 / VIAyy.S.1 / VIAyy.S.2

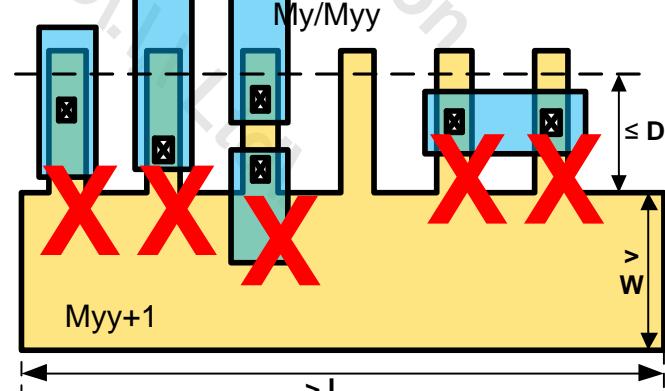
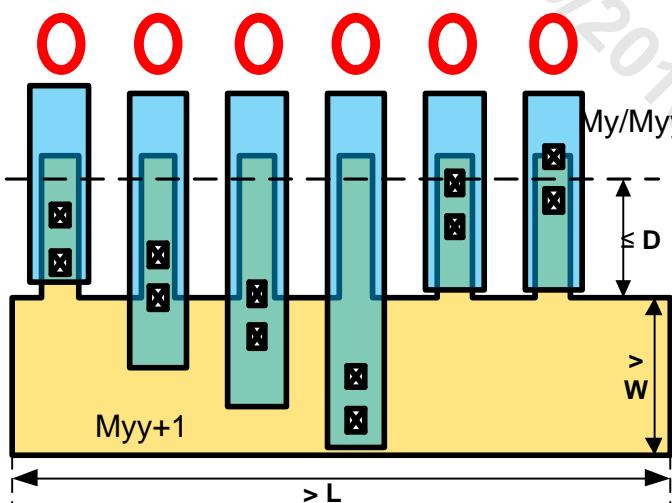
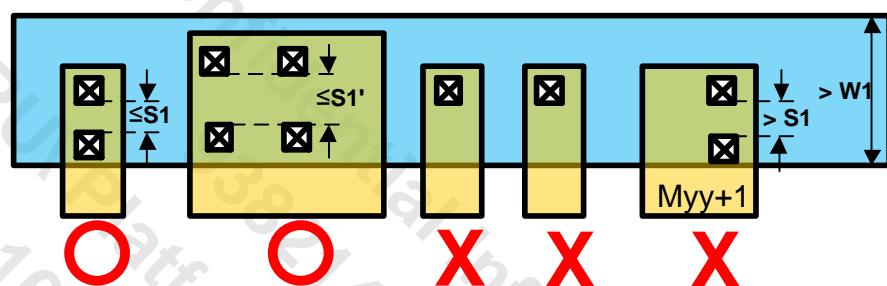




45-degree rotated VIAyy is not allowed.



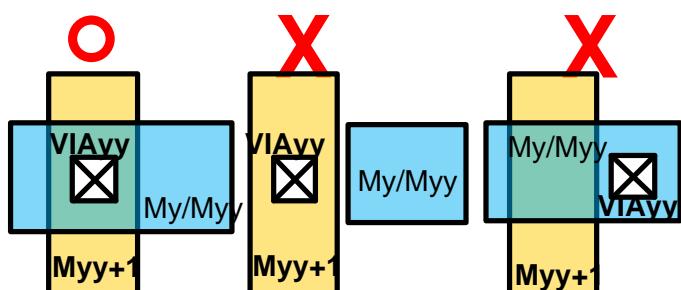
VIAyy.R.1



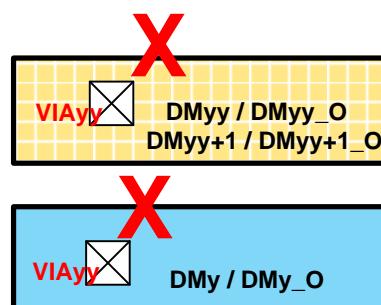
Rule No	VIAyy.R.4	VIAyy.R.5	VIAyy.R.6
W	$> 0.189\mu\text{m}$	$> 1.26\mu\text{m}$	$> 1.89\mu\text{m}$
L	$> 0.189\mu\text{m}$	$> 1.26\mu\text{m}$	$> 6.3\mu\text{m}$
D	$\leq 1.026\mu\text{m}$	$\leq 2.52\mu\text{m}$	$\leq 6.39\mu\text{m}$

VIAyy.R.4 / VIAyy.R.5 / VIAyy.R.6

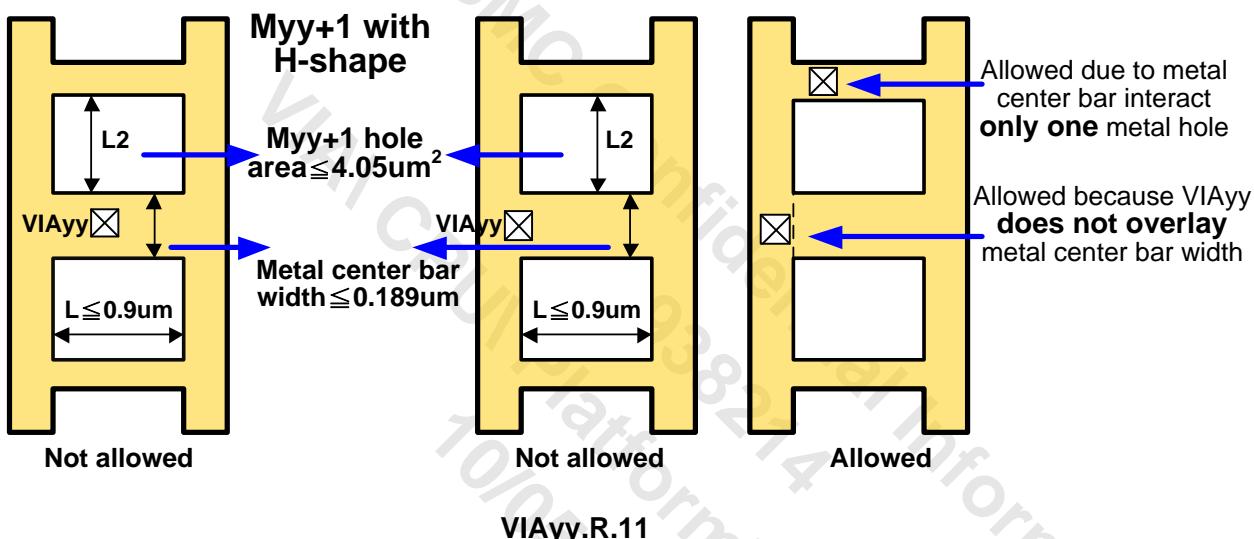
VIAyy connected to DM_y, DM_{y_O},
DM_{y+1}, DM_{y+1_O} is not allowed.



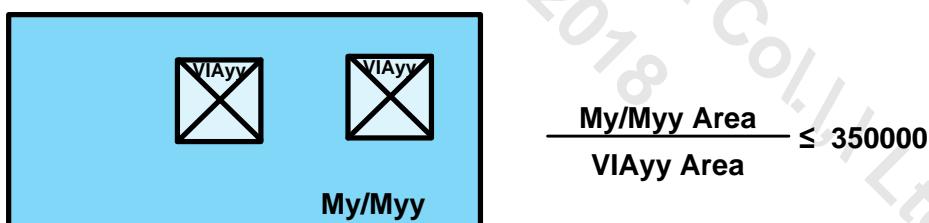
VIAyy.R.7



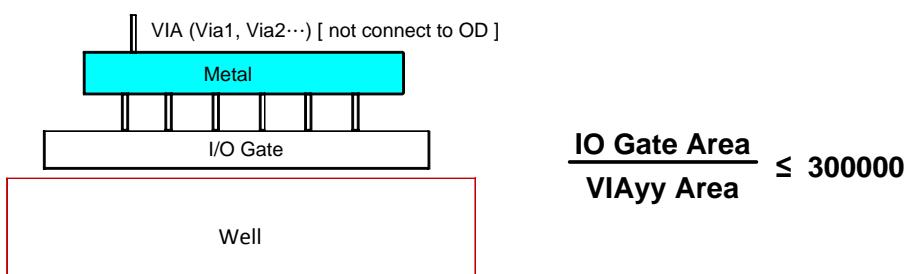
VIAyy.R.12



VIAyy.R.11



VIAyy.R.13



VIAyy.R.13.2

4.5.55 Myy Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5. DRC checks DMyy_O as well as Myy in this section.

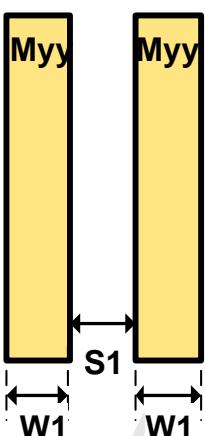
Rule No.	Description	Label	Op.	Rule
Myy.W.1	Width	W1	\geq	0.0620
Myy.W.2	Width of 45-degree bent Myy	W2	\geq	0.1530
Myy.W.3	Maximum width (Except SEALRING_ALL)	W3	\leq	4.05
Myy.S.1	Space	S1	\geq	0.0640
Myy.S.1®	Recommended space (to reduce the short possibility)	S1	\geq	0.0810
Myy.S.2	Space to Myy [width > 0.153 μm (W1) and the PRL > 0.243 μm (L1)]	S2	\geq	0.0900
Myy.S.2.1	Space to Myy [width > 0.216 μm (W2) and the PRL > 0.243 μm (L2)]	S2	\geq	0.1080
Myy.S.2.2	Space to Myy [width > 0.279 μm (W3) and the PRL > 0.360 μm (L3)]	S2	\geq	0.1350
Myy.S.2.3	Space to Myy [width > 0.558 μm (W4) and the PRL > 0.558 μm (L4)]	S2	\geq	0.1890
Myy.S.3	Space to Myy [width > 1.35 μm (W5) and the PRL > 1.35 μm (L5)]	S3	\geq	0.4500
Myy.S.5	Dense metal line-end rule: Space at Myy line-end ($W < 0.090 \mu\text{m}$ (Q)) in a dense-line-end configuration: Myy has PRL with Myy (measured with $T = 0.035 \mu\text{m}$ extension) along 2 adjacent edges of Myy [any one edge < Q distance from the corner of the two edges] (Except following conditions: 1. small jog with edge length < 0.062 μm (R))	S1/S2	\geq	0.0900
Myy.S.5.1	Dense metal line-end rule: Space at Myy line-end ($W < 0.090 \mu\text{m}$ (Q)) in a dense-line-end configuration: Myy has PRL with Myy (measured with $T = 0.035 \mu\text{m}$ extension) along 2 adjacent edges of Myy [any one edge < Q distance from the corner of the two edges], and Myy enclose VIAyy-1 < 0.045 μm at line-end (Except following conditions: 1. small jog with edge length < 0.062 μm (R), 2. two or more VIAyy-1 (at least one via does not violate this rule) present in the metal intersection, 3. The following conditions can pass the check flow (i) S1/S2 $\geq 0.108 \mu\text{m}$ and Myy enclosure VIAyy-1 $\geq 0.027 \mu\text{m}$ (ii) S1/S2 < 0.108 μm and Myy enclosure VIAyy-1 $\geq 0.045 \mu\text{m}$ (iii) Sum of S1 and Myy enclosure of VIAyy-1 $\geq 0.135 \mu\text{m}$ with 5 examples (S1/Myy enclosure VIAyy-1): (a) space $\geq 0.108 \mu\text{m}$ / enclosure $\geq 0.027 \mu\text{m}$ (b) space $\geq 0.104 \mu\text{m}$ / enclosure $\geq 0.031 \mu\text{m}$ (c) space $\geq 0.099 \mu\text{m}$ / enclosure $\geq 0.036 \mu\text{m}$ (d) space $\geq 0.095 \mu\text{m}$ / enclosure $\geq 0.040 \mu\text{m}$ (e) space $\geq 0.090 \mu\text{m}$ / enclosure $\geq 0.045 \mu\text{m}$)	S1/S2	\geq	0.1080
Myy.S.6	Space to 45-degree bent Myy	S6	\geq	0.1530
Myy.S.8	Space to VIAyy-1 or VIAyy/VIAz/VIAr [maximum delta V > 1.65V] (1.5V + 10%)	S8	\geq	0.0720
Myy.S.8.1	Space to VIAyy-1 or VIAyy/VIAz/VIAr [maximum delta V > 1.98V] (1.8V + 10%)	S8	\geq	0.0900
Myy.EN.0	Enclosure of VIAyy-1 is defined by either Myy.EN.1 or Myy.EN.3			
Myy.EN.1	Enclosure of square VIAyy-1 for two opposite sides with the other two sides $\geq 0 \mu\text{m}$ (Except SEALRING_ALL)	EN1	\geq	0.0270
Myy.EN.3	Enclosure of square VIAyy-1 for two opposite sides with the other two sides $\geq 0.009 \mu\text{m}$ (Except SEALRING_ALL)	EN3	\geq	0.0180
Myy.EN.0®	Recommended enclosure of VIAyy-1 is defined by either Myy.EN.1® or Myy.EN.2®			
Myy.EN.1®	Recommended enclosure of VIAyy-1 to avoid high Rc	EN1R	\geq	0.0270
Myy.EN.2®	Recommended enclosure of VIAyy-1 [at least two opposite sides] to avoid high Rc	EN2R	\geq	0.0450
Myy.A.1	Area	A1	\geq	0.02190

Rule No.	Description	Label	Op.	Rule
Myy.A.1®	Recommended area (Except DMyy_O)	A1	≥	0.02850
Myy.A.2	Area [with all of edge length < 0.153 μm] (Except following conditions: 1. a pattern filling 0.062 μm x 0.153 μm tile)	A2	≥	0.04860
Myy.A.3	Enclosed area	A3	≥	0.16200
Myy.DN.1.3	Minimum metal density in window 112 μm x 112 μm, stepping 56 μm		≥	10%
Myy.DN.2.4	Maximum metal density in window 112 μm x 112 μm, stepping 56 μm		≤	85%
Myy.DN.3.1	The metal density difference between any two neighboring checking windows including DMnEXCL [window 180 μm x 180 μm, stepping 180 μm]		≤	50%
Myy.DN.5®	Recommended minimum metal density in window 50 μm x 50 μm, stepping 25 μm (Except LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	30%
Myy.DN.6	Metal density [window 72 μm x 72 μm, stepping 36 μm] (Except SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
Myy.DN.6®	Recommend metal density ≥ 1% for IP level. All of condition-A, condition-B, and condition-C are recommended (1) Condition-A: For IP level, recommend metal density [window 36 μm x 36 μm, stepping 36 μm] ≥ 1% (2) Condition-B: For IP level, recommend maximum area of merged low density windows [checking window 9 μm x 9 μm, stepping 4.5 μm, density < 1%] ≤ 1296 μm ² , except merged low density windows width ≤ 27 μm (3) Condition-C: For IP level, recommend maximum area of merged low density windows [checking window 9 μm x 9 μm, stepping 4.5 μm, density < 1%] ≤ 3645 μm ² (Except following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)			
Myy.DN.6.1	Metal density [window 9 μm x 9 μm, stepping 4.5 μm] (Except SEALRING_ALL, or following conditions: 1. the maximum area of the merged low density windows [density < 1%] ≤ 5184 μm ² , while the merged low density windows width is > 27 μm, 2. the maximum area of the merged low density windows [density < 1%] ≤ 14580 μm ² , 3. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
Myy.DN.7	It is not allowed to have local density < 5% of all 3 consecutive metal (Myy, Myy+1 and Myy+2) over any 27 μm x 27 μm (stepping 13.5 μm), i.e. it is allowed for either one of Myy, Myy+1, or Myy+2 to have a local density ≥ 5% (The metal layers include Myy and dummy metals) (Except following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)			
Myy.DN.7®	It is not recommended to have local density < 5% of all 3 consecutive metal (Myy, Myy+1 and Myy+2) over any 13.5 μm x 13.5 μm (stepping 13.5 μm) for IP level, i.e. it is allowed for either one of Myy, Myy+1, or Myy+2 to have a local density ≥ 5% (The metal layers include Myy and dummy metals) (Except following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)			
Myy.DN.8®	Recommended total Myy island (for all Myy layers) density < 5.3E+4 ea/mm ² across full chip The definition of counts of small Myy island: 1. Myy width = 0.064 μm 2. Myy length ≤ 0.468 μm 3. Myy has two segments with space = 0.062 μm with the PRL (0.188 μm ≤ PRL < 0.468 μm)			

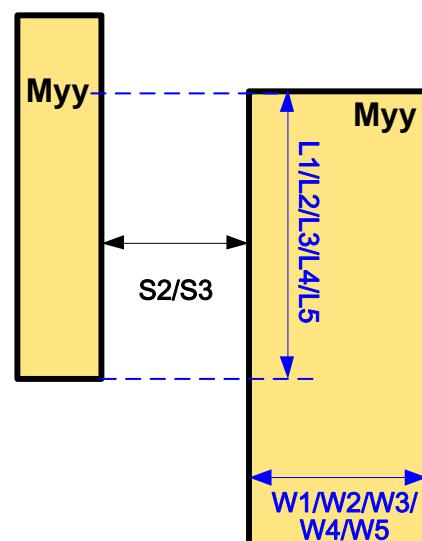
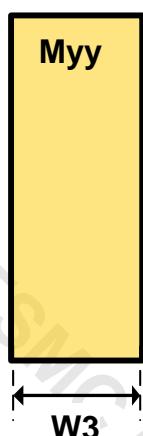
Rule No.	Description	Label	Op.	Rule
Myy.R.1 ^U	Myy line-end must be rectangular. Other shapes are not allowed			
Myy.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers.			
Myy.R.11	Maximum delta V > 3.63V is not allowed DRC searching range of Myy space to Myy or VIAyy-1 or VIAyy is < 0.360 μm			
Myy.R.17	DMyy is a must in chip level.			

TSMC Confidential Information
938214
VIAI CPU Platform\ Col., I Ltd.
10/05/2018

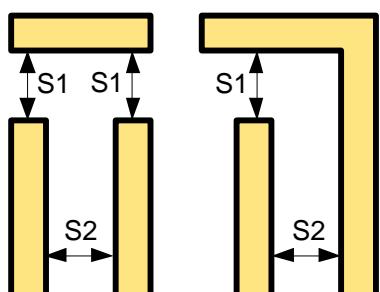
Myy



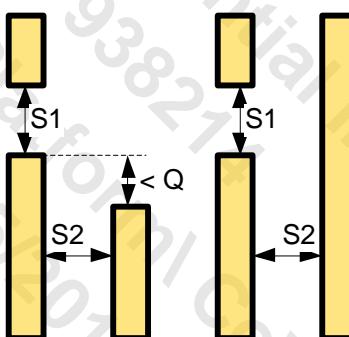
**Myy.W.1/ Myy.W.3
Myy.S.1/ Myy.S.1®**



**Myy.S.2 / Myy.S.2.1/ Myy.S.2.2 /
Myy.S.2.3 / Myy.S.3**

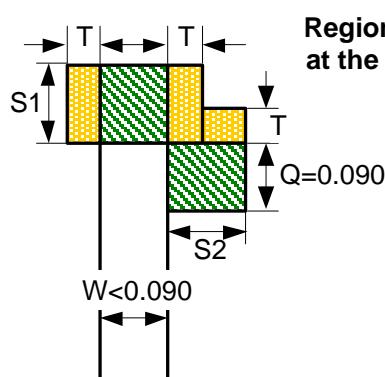


Myy.S.5.1

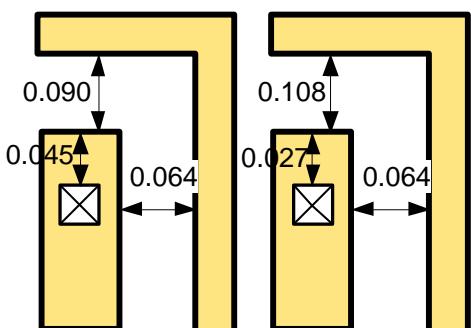
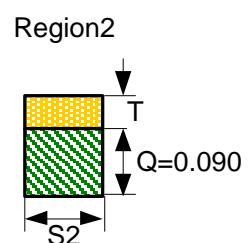
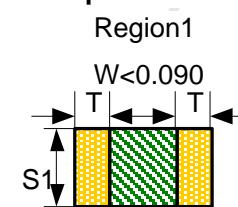


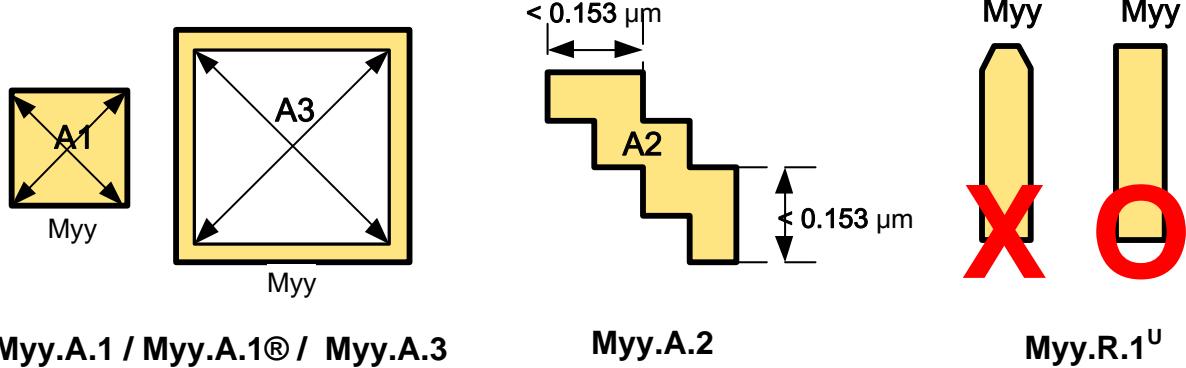
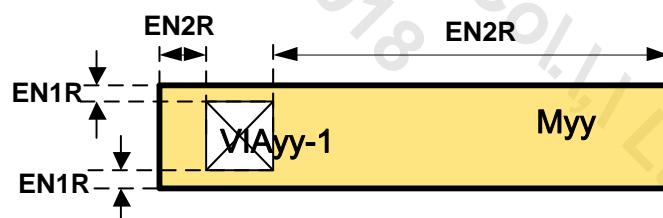
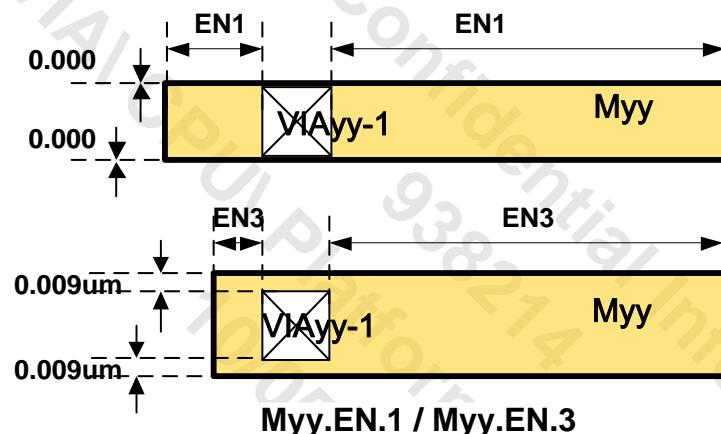
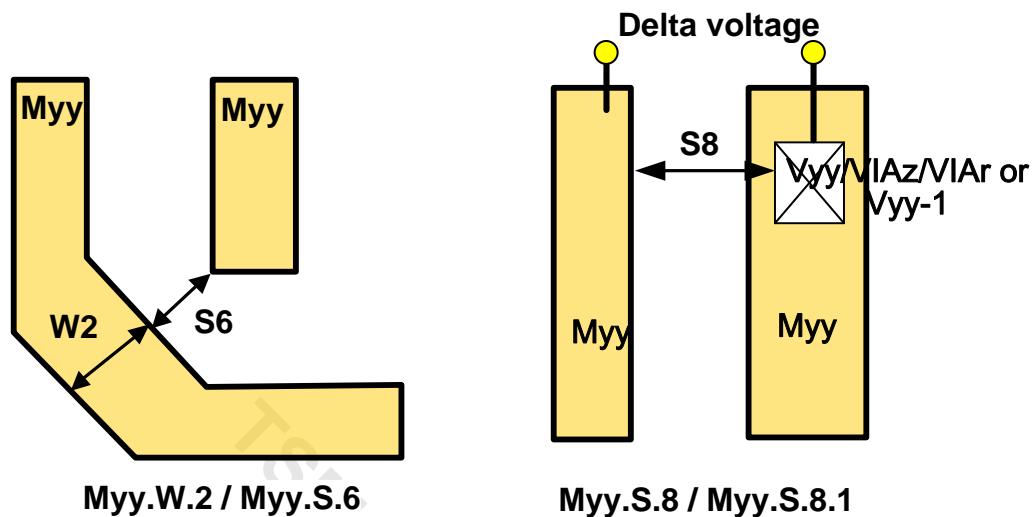
Myy.S.5

S1	S2	Myy enclosure of Vyy-1
0.108	0.064	0.027
0.104	0.064	0.031
0.099	0.064	0.036
0.095	0.064	0.040
0.090	0.064	0.045



Region1 or 2 can not have other Myy patterns at the same time. One of them with other Myy patterns is allowed.



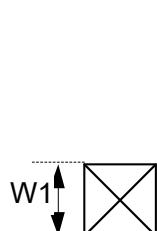


4.5.56 VIAxy Layout Rules

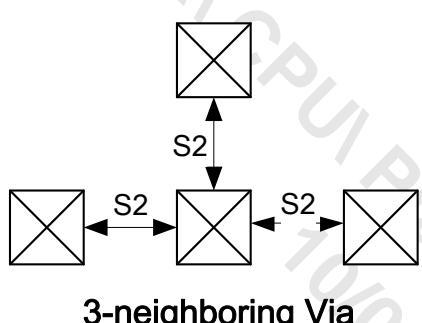
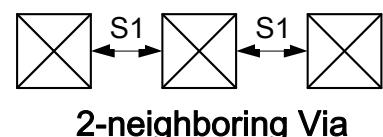
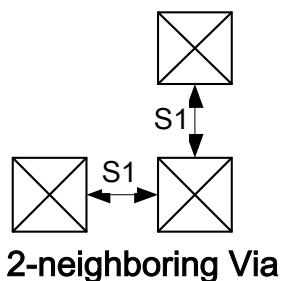
For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
VIAxy.W.1	Width (maximum = minimum) (Except SEALRING_ALL)	W1	=	0.1260
VIAxy.S.1	Space	S1	\geq	0.1260
VIAxy.S.2	Space to 3-neighboring VIAxy (distance $< 0.158 \mu\text{m}$)	S2	\geq	0.1440
VIAxy.EN.1	Enclosure by Myx for two opposite sides with the other two sides $\geq 0 \mu\text{m}$ (Except SEALRING_ALL)	EN1	\geq	0.0410
VIAxy.EN.2	Enclosure by Myy for two opposite sides with the other two sides $\geq 0.015 \mu\text{m}$	EN2	\geq	0.0410
VIAxy.R.1	45-degree rotated VIAxy is not allowed.			
VIAxy.R.2	At least two VIAxy with space $\leq 0.261 \mu\text{m}$ (S1), or at least four VIAxy with space $\leq 0.513 \mu\text{m}$ (S1') are required to connect Myy/Myx and Myx+1 when one of these two metals has width and length $> 0.378 \mu\text{m}$ (W1). (Except SEALRING_ALL)			
VIAxy.R.3	At least four VIAxy with space $\leq 0.261 \mu\text{m}$ (S2), or at least nine VIAxy with space $\leq 0.693 \mu\text{m}$ (S2') are required to connect Myy/Myx and Myx+1 when one of these two metals has width and length $> 1.026 \mu\text{m}$ (W2). (Except SEALRING_ALL)			
VIAxy.R.4	At least two VIAxy must be used for a connection that distance $\leq 1.26 \mu\text{m}$ (D) away from a metal plate (either Myy/Myx or Myx+1) with length $> 0.630 \mu\text{m}$ (L) and width $> 0.630 \mu\text{m}$ (W). (Except SEALRING_ALL)			
VIAxy.R.5	At least two VIAxy must be used for a connection that distance $\leq 2.52 \mu\text{m}$ (D) away from a metal plate (either Myy/Myx or Myx+1) with length $> 1.8 \mu\text{m}$ (L) and width $> 1.8 \mu\text{m}$ (W). (Except SEALRING_ALL)			
VIAxy.R.6	At least two VIAxy must be used for a connection that distance $\leq 6.39 \mu\text{m}$ (D) away from a metal plate (either Myy/Myx or Myx+1) with length $> 9 \mu\text{m}$ (L) and width $> 2.7 \mu\text{m}$ (W). (Except SEALRING_ALL)			
VIAxy.R.7	VIAxy must be fully covered by {Myy AND Myx+1} or {Myx AND Myx+1}			
VIAxy.R.11	Single VIAxy is not allowed in "H-shape" Myx+1 when all of the following conditions come into existence: (1) The Myx+1 has "H-shape" interact two metal holes: both two metal hole length $\leq 4.5 \mu\text{m}$ (L2) and two metal hole area $\leq 4.05 \mu\text{m}^2$ (2) The VIAxy overlaps on the center metal bar of this "H-shape" Myx+1 (3) The center metal bar length $\leq 0.900 \mu\text{m}$ (L) and the metal bar width $\leq 0.378 \mu\text{m}$.			
VIAxy.R.9g ^U	Recommend using redundant VIAs to avoid high Rc wherever layout allows.			
VIAxy.R.10	VIAxy connected to DM _y , DM _{yy} , DM _{yx} is not allowed.			
VIAxy.R.13	Maximum area ratio of Myy/Myx to upper VIAxy in the same net [connects to gate with area $> 10700 \mu\text{m}^2$, and does not connect to OD]. This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = $(2.5 \times WdxLd)$ for ≥ 2 -fin device		\leq	350000
VIAxy.R.13.2	Maximum area ratio of I/O gate to single layer VIAxy in the same net. (Except following conditions: 1. the protection OD area $\geq 0.25 \mu\text{m}^2$). This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = $(2.5 \times WdxLd)$ for ≥ 2 -fin device		\leq	300000
VIAxy.EN.0®	Recommended enclosure by Myy or Myx is defined by either VIAxy.EN.1® or VIAxy.EN.2®.			
VIAxy.EN.1®	Recommended enclosure by Myy or Myx to avoid high Rc. [all sides]	EN1R	\geq	0.0410
VIAxy.EN.2®	Recommended enclosure by Myy or Myx [at least two opposite sides] to avoid high Rc.	EN2R	\geq	0.0680

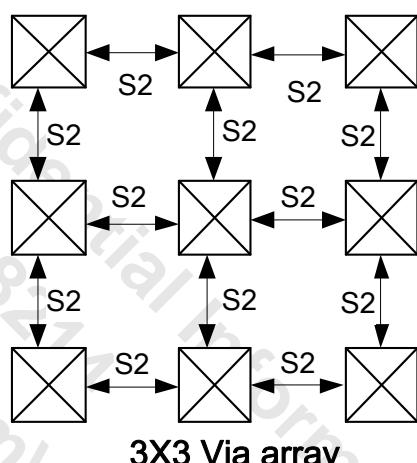
VIAyx



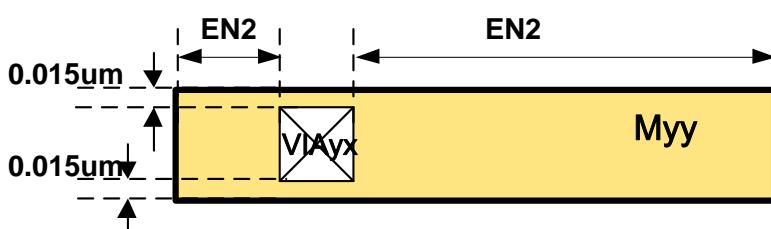
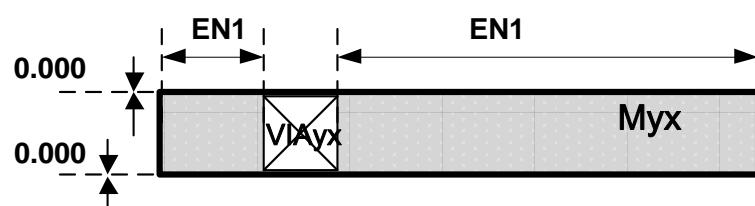
VIAyx.W.1



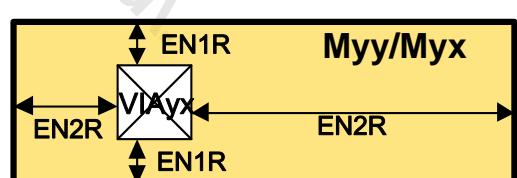
VIAyx.S.1



VIAyx.S.2



VIAyx.EN.1 / VIAyx.EN.2

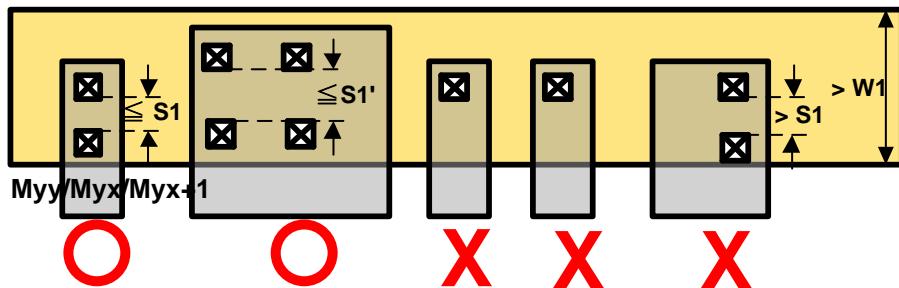


VIAyx.EN.1® / VIAyx.EN.2®

45-degree rotated VIAyx is not allowed.

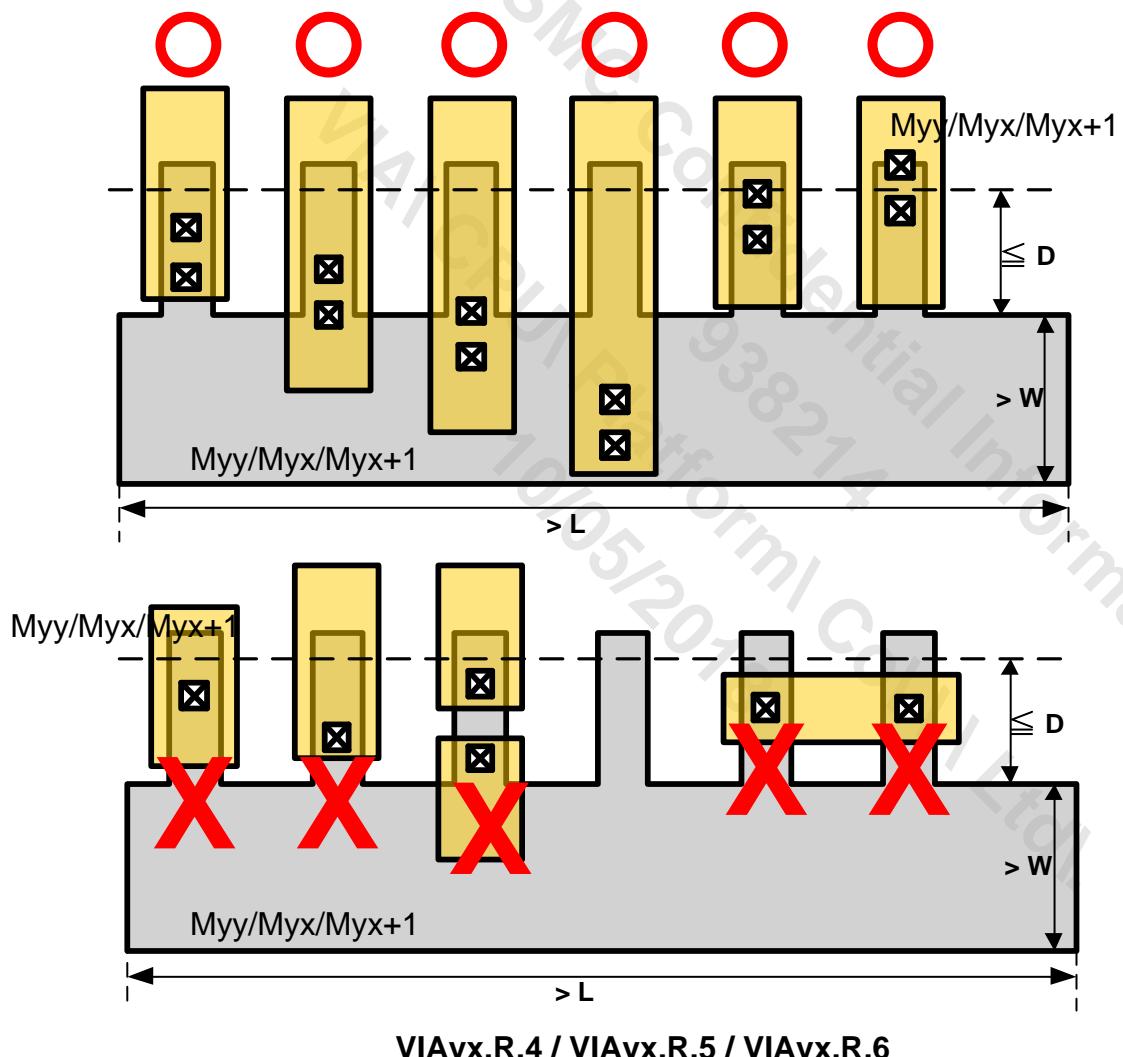


Myy/Myx/Myx+1



VIAyx.R.1

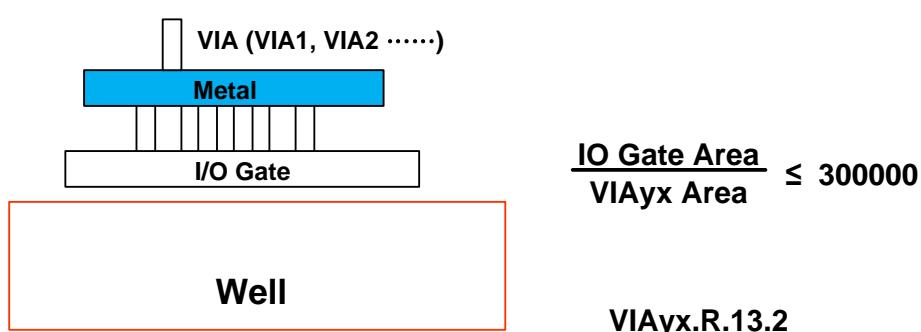
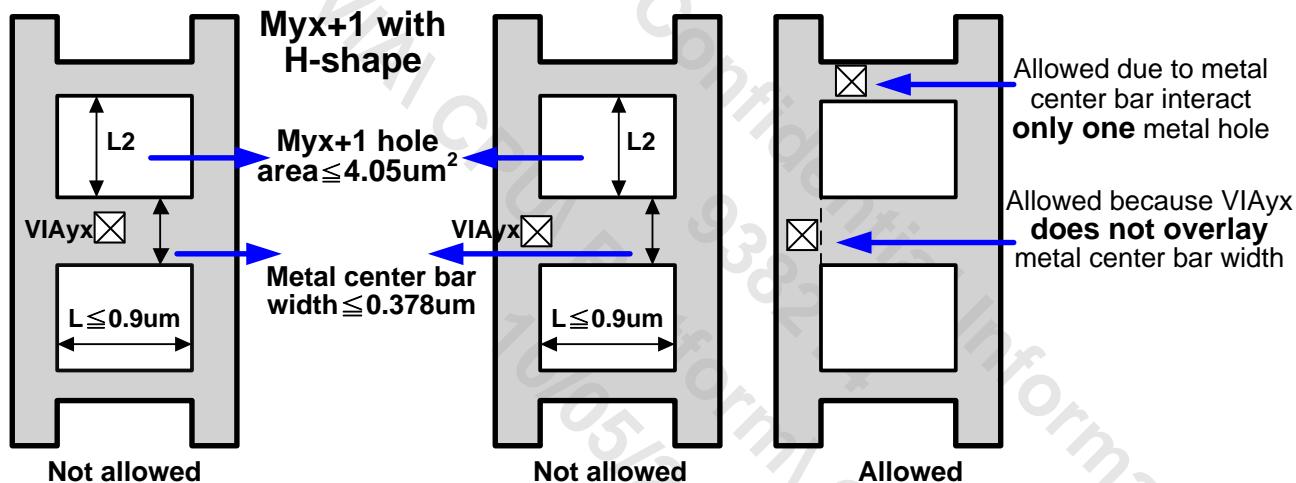
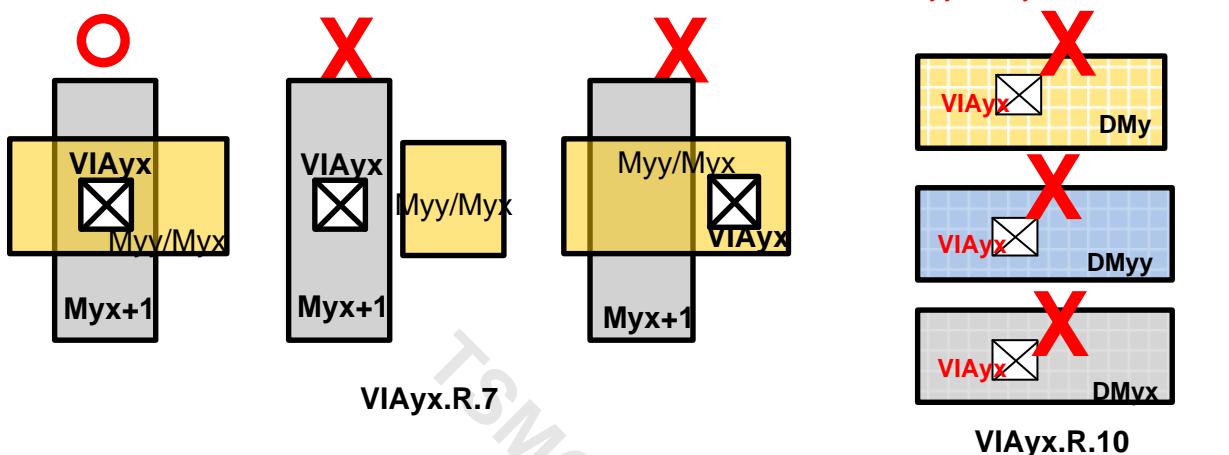
VIAyx.R.2 / VIAyx.R.3



VIAyx.R.4 / VIAyx.R.5 / VIAyx.R.6

Rule No	VIAyx.R.4	VIAyx.R.5	VIAyx.R.6
W	> 0.630 μm	> 1.8 μm	> 2.7 μm
L	> 0.630 μm	> 1.8 μm	> 9 μm
D	\leq 1.26 μm	\leq 2.52 μm	\leq 6.39 μm

VIAyx connected to DMy,
DMyy, DMyx is not allowed.

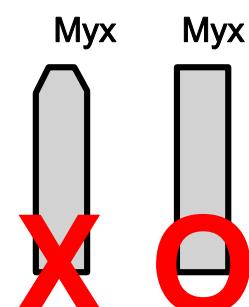
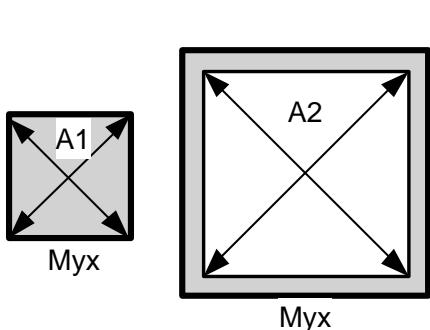
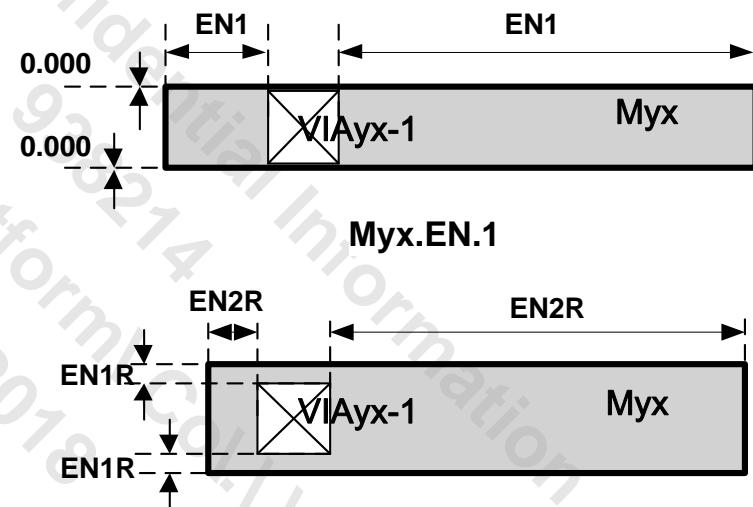
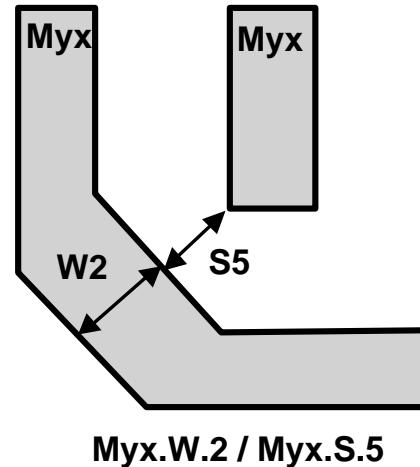
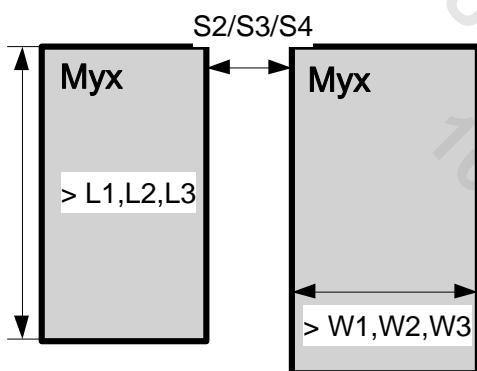
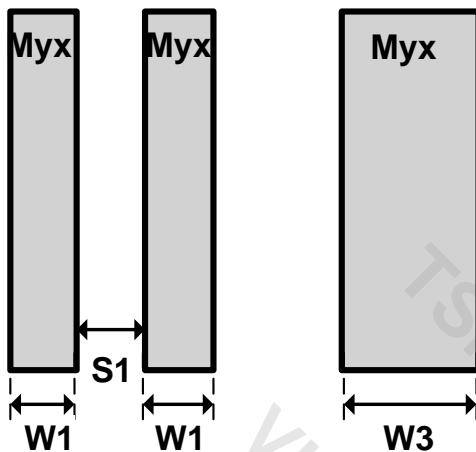


4.5.57 Myx Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
Myx.W.1	Width	W1	\geq	0.1260
Myx.W.2	Width of 45-degree bent Myx.	W2	\geq	0.3600
Myx.W.3	Maximum width (Except following conditions: 1. {INDDMY SIZING 19.8 μm })	W3	\leq	10.8
Myx.S.1	Space	S1	\geq	0.1260
Myx.S.2	Space to Myx [width > 0.189 μm (W1) and the PRL > 0.468 μm (L1)]	S2	\geq	0.1710
Myx.S.3	Space to Myx [width > 1.35 μm (W2) and the PRL > 1.35 μm (L2)]	S3	\geq	0.4500
Myx.S.4	Space to Myx [width > 4.05 μm (W3) and the PRL > 4.05 μm (L3)]	S4	\geq	1.35
Myx.S.5	Space to 45-degree bent Myx	S5	\geq	0.3600
Myx.EN.1	Enclosure of VIAyx-1 for two opposite sides with the other two sides \geq 0 μm (Except SEALRING_ALL)	EN1	\geq	0.0410
Myx.A.1	Area	A1	\geq	0.05700
Myx.A.2	Enclosed area	A2	\geq	0.18000
Myx.DN.1.3	Minimum metal density in window 112 μm x 112 μm , stepping 56 μm (Except INDDMY, LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	10%
Myx.DN.2.4	Maximum metal density in window 112 μm x 112 μm , stepping 56 μm (Except LOGO, SEALRING_ALL, or following conditions: 1. bond pad, 2. Chip corner triangle empty areas if seal-ring is added by tsmc)		\leq	85%
Myx.DN.3.1	The metal density difference between any two neighboring checking windows including DMnEXCL [window 180 μm x 180 μm , stepping 180 μm].		\leq	50%
Myx.DN.5®	Recommended minimum metal density in window 50 μm x 50 μm , stepping 25 μm (Except LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	30%
Myx.R.1 ^U	Myx line-end must be rectangular. Other shapes are not allowed.			
Myx.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers.			
Myx.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of Myx space to Myx or VIAyx-1 or VIAyx is < 0.360 μm			
Myx.R.17	DMyx is a must in chip level.			
Myx.EN.0®	Recommended enclosure of VIAyx-1 is defined by either Myx.EN.1® or Myx.EN.2®.			
Myx.EN.1®	Recommended enclosure of VIAyx-1 to avoid high Rc. [all sides]	EN1R	\geq	0.0410
Myx.EN.2®	Recommended enclosure of VIAyx-1 [at least two opposite sides] to avoid high Rc.	EN2R	\geq	0.0680

Myx

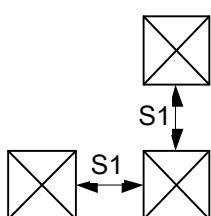
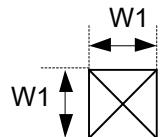


4.5.58 VIAyz Layout Rules

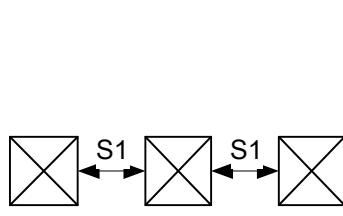
For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
VIAyz.W.1	Width (maximum = minimum) (Except SEALRING_ALL)	W1	=	0.1800
VIAyz.S.1	Space	S1	\geq	0.1800
VIAyz.S.2	Space to 3-neighboring VIAyz (distance < 0.252 μm)	S2	\geq	0.2250
VIAyz.EN.1	Enclosure by Myz	EN1	\geq	0
VIAyz.EN.2	Enclosure by Myy, or Myx (Except SEALRING_ALL)	EN2	\geq	0.0250
VIAyz.EN.3	Enclosure by Myy, Myx, or Myz [at least two opposite sides] (Except SEALRING_ALL)	EN3	\geq	0.0450
VIAyz.R.1	45-degree rotated VIAyz is not allowed			
VIAyz.R.2	At least two VIAyz with space $\leq 0.36 \mu\text{m}$ (S1), or at least four VIAyz with space $\leq 0.45 \mu\text{m}$ (S1') are required to connect Myy/Myx/Myz and Myz+1 when one of these two metals has width and length $> 0.54 \mu\text{m}$ (W1)			
VIAyz.R.3	At least four VIAyz with space $\leq 0.36 \mu\text{m}$ (S1') are required to connect Myy/Myx/Myz and Myz+1 when one of these two metals has width and length $> 1.26 \mu\text{m}$ (W1)			
VIAyz.R.4	At least two VIAyz must be used for a connection that distance $\leq 1.44 \mu\text{m}$ (D) away from a metal plate (either Myy/Myx/Myz or Myz+1) with length $> 0.54 \mu\text{m}$ (L) and width $> 0.54 \mu\text{m}$ (W)			
VIAyz.R.5	At least two VIAyz must be used for a connection that distance $\leq 1.8 \mu\text{m}$ (D) away from a metal plate (either Myy/Myx/Myz or Myz+1) with length $> 1.8 \mu\text{m}$ (L) and width $> 1.8 \mu\text{m}$ (W)			
VIAyz.R.6	At least two VIAyz must be used for a connection that distance $\leq 4.5 \mu\text{m}$ (D) away from a metal plate (either Myy/Myx/Myz or Myz+1) with length $> 9 \mu\text{m}$ (L) and width $> 2.7 \mu\text{m}$ (W)			
VIAyz.R.7	VIAyz must be fully covered by {Myz AND Myz+1} or {Myy AND Myz+1} or {Myx AND Myz+1}			
VIAyz.R.13	Maximum area ratio of Myy/Myx/Myz to upper VIAyz in the same net [connects to gate with area $> 10700 \mu\text{m}^2$, and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = $(2.5 \times W \times D)$ for ≥ 2 -fin device		\leq	350000
VIAyz.R.13.2	Maximum area ratio of I/O gate to single layer VIAyz in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area $\geq 0.25 \mu\text{m}^2$) Definition: Gate area = $(2.5 \times W \times D)$ for ≥ 2 -fin device		\leq	300000

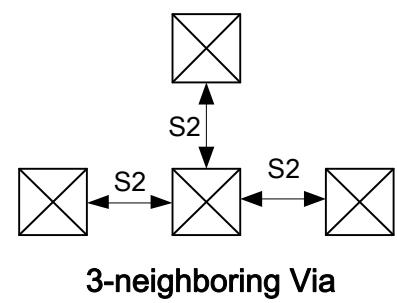
VIAyz



2-neighboring Via



2-neighboring Via

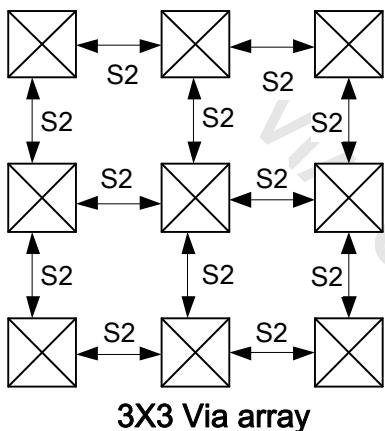


3-neighboring Via

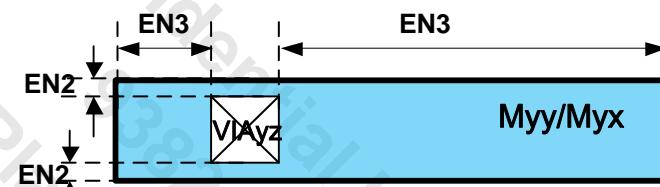
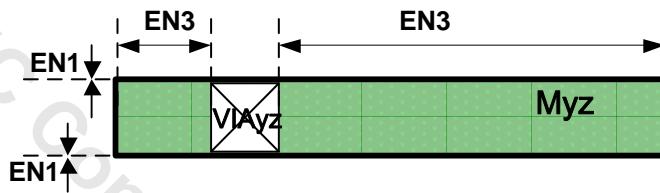
VIAyz.W.1

VIAyz.S.1

VIAyz.S.2

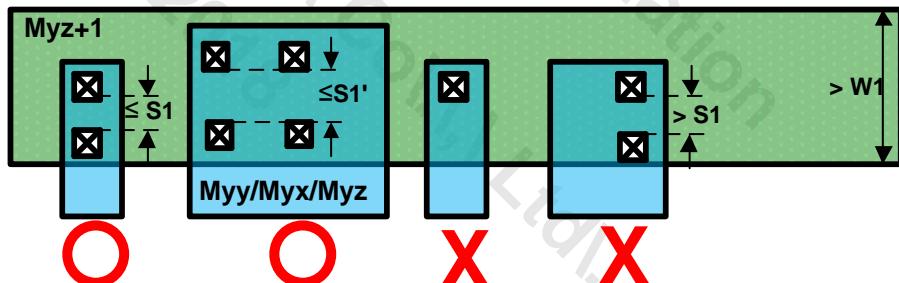


3X3 Via array



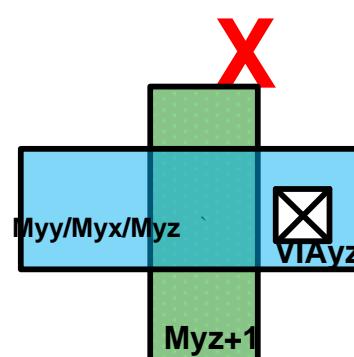
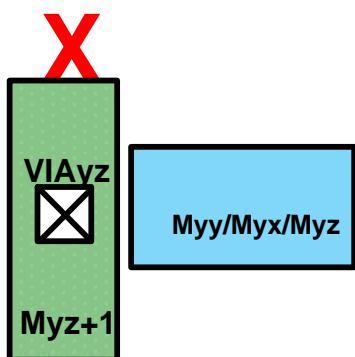
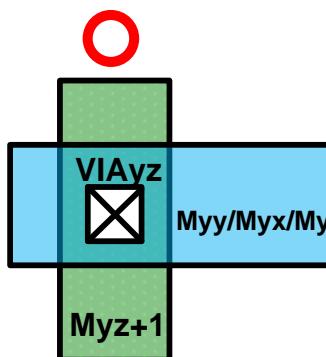
VIAyz.EN.1 / VIAyz.EN.2 / VIAyz.EN.3

45-degree rotated VIAyz is not allowed.

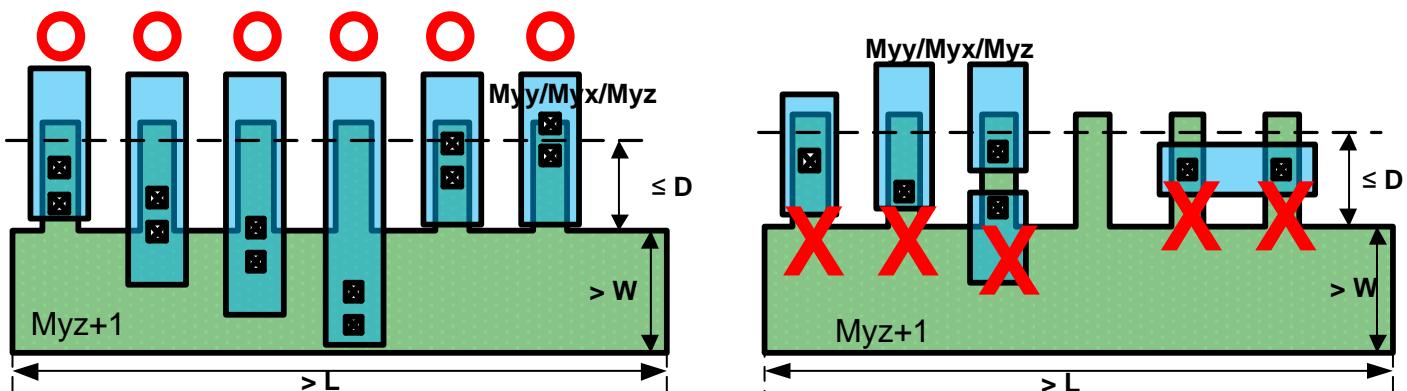


VIAyz.R.1

VIAyz.R.2 / VIAyz.R.3

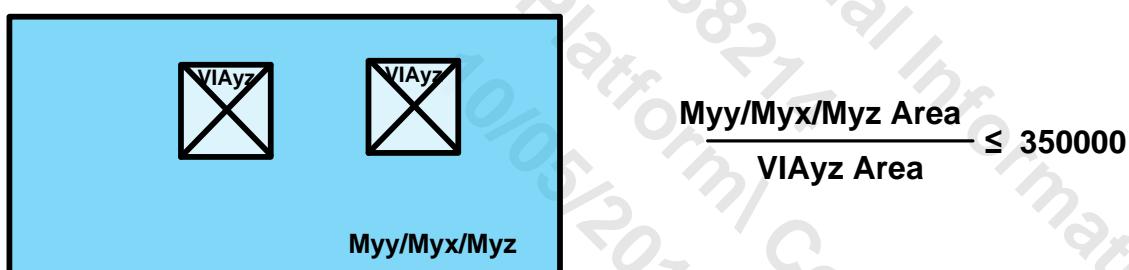


VIAyz.R.7

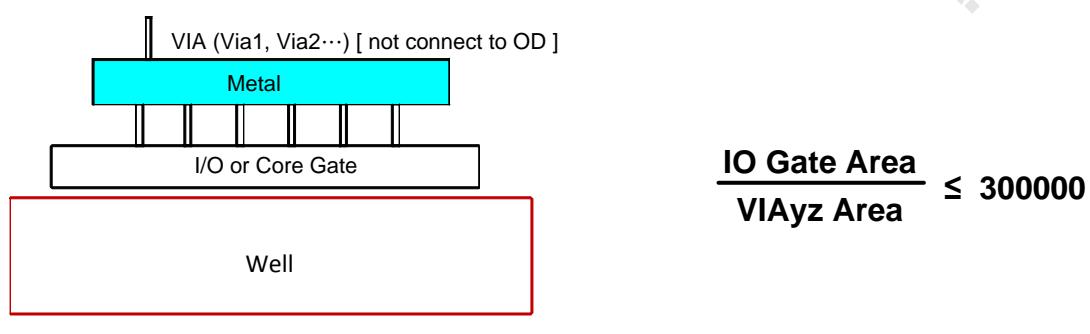


Rule No	VIAyz.R.4	VIAyz.R.5	VIAyz.R.6
W	> 0.540 μm	> 1.8 μm	> 2.7 μm
L	> 0.540 μm	> 1.8 μm	> 9 μm
D	≤ 1.44 μm	≤ 1.8 μm	≤ 4.5 μm

VIAyz.R.4 / VIAyz.R.5 / VIAyz.R.6



VIAyz.R.13

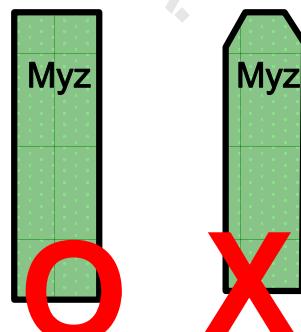
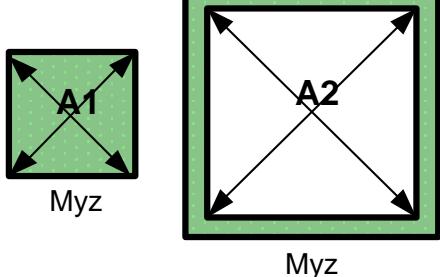
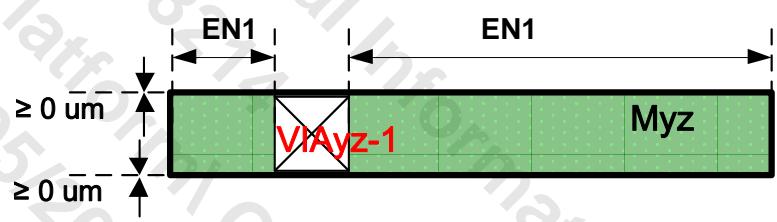
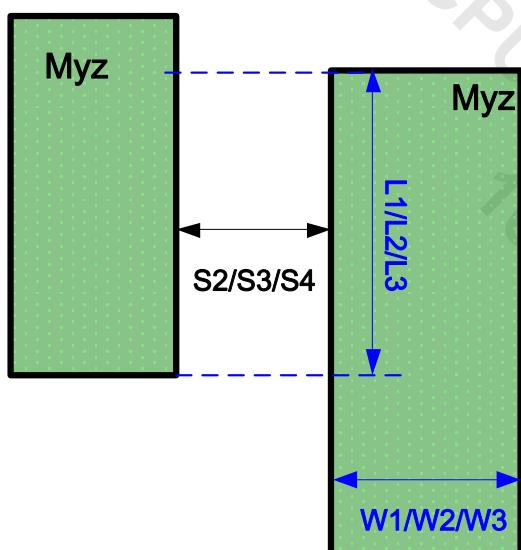
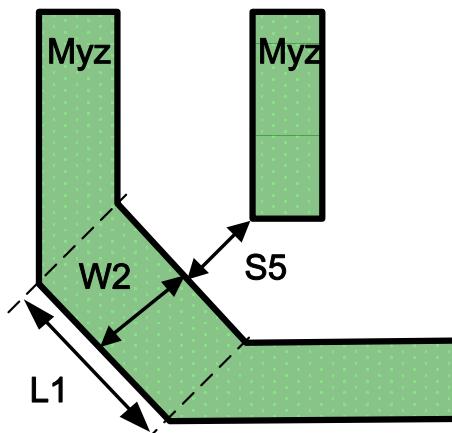
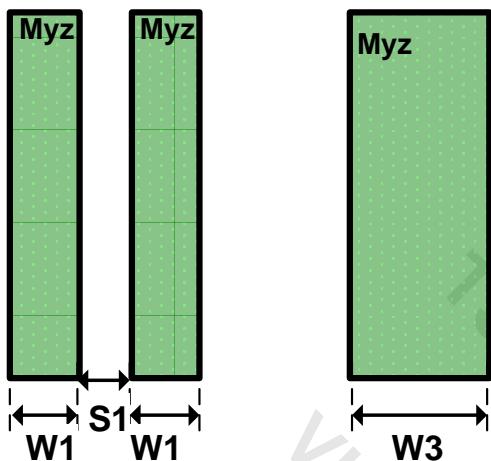


VIAyz.R.13.2

4.5.59 Myz Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
Myz.W.1	Width	W1	\geq	0.1800
Myz.W.2	Width of 45-degree bent Myz	W2	\geq	0.3510
Myz.W.3	Maximum width	W3	\leq	10.8
Myz.S.1	Space	S1	\geq	0.1800
Myz.S.2	Space to Myz [width > 0.351 μm (W1) and the PRL > 0.900 μm (L1)]	S2	\geq	0.2160
Myz.S.3	Space to Myz [width > 1.35 μm (W2) and the PRL > 1.35 μm (L2)]	S3	\geq	0.4500
Myz.S.4	Space to Myz [width > 4.05 μm (W3) and the PRL > 4.050 μm (L3)]	S4	\geq	1.35
Myz.S.5	Space to 45-degree bent Myz	S5	\geq	0.3510
Myz.EN.1	Enclosure of VIAyz-1 for two opposite sides with the other two sides \geq 0.000 μm (Except SEALRING_ALL)	EN1	\geq	0.0450
Myz.L.1	Length of 45-degree bent Myz (minimum edge length)	L1	\geq	0.9000
Myz.A.1	Area	A1	\geq	0.11660
Myz.A.2	Enclosed area	A2	\geq	0.21460
Myz.DN.1.3	Minimum Metal density in window 112 $\mu\text{m} \times$ 112 μm , stepping 56 μm (Except INDDMY)		\geq	10%
Myz.DN.2.4	Maximum Metal density in window 112 $\mu\text{m} \times$ 112 μm , stepping 56 μm		\leq	85%
Myz.DN.3.1	The metal density difference between any two neighboring checking windows including DMnEXCL [window 180 $\mu\text{m} \times$ 180 μm , stepping 180 μm]		\leq	50%
Myz.R.1 ^U	Myz line-end must be rectangular. Other shapes are not allowed			
Myz.R.2	Metal (pin) layers must be drawn only interact with one relative Metal (drawing) layers			
Myz.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of Myz space to Myz or VIAyz-1 or VIAyz is < 0.360 μm			
Myz.R.17	DMyz is a must in chip level.			

Myz

Myz line-end must be rectangular.

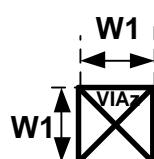
Myz.R.1^U

4.5.60 VIAz Layout Rules

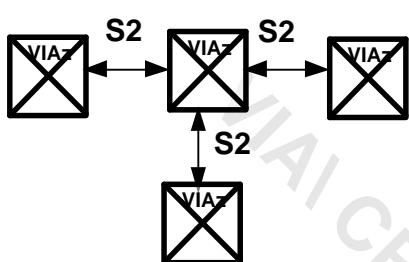
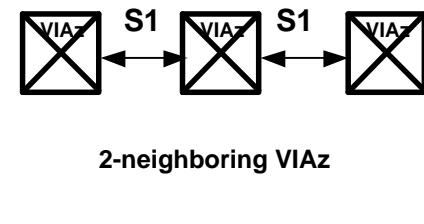
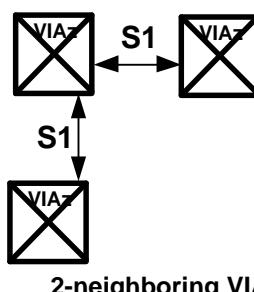
For the specification of metals/VIAz stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
VIAz.W.1	Width (maximum = minimum) (Except SEALRING_ALL)	W1	=	0.3240
VIAz.S.1	Space	S1	\geq	0.3060
VIAz.S.2	Space to 3-neighboring VIAz (distance < 0.504 μm)	S2	\geq	0.4860
VIAz.EN.1	Enclosure by My, Myy, Myx, Myz, or Mz for two opposite sides with the other two sides $\geq 0.018 \mu\text{m}$ (Except SEALRING_ALL, or following conditions: 1. top VIA inside CBMFFINAL)	EN1	\geq	0.0720
VIAz.R.1	45-degree rotated VIAz is not allowed			
VIAz.R.2	At least two VIAz with spacing $\leq 1.53 \mu\text{m}$ are required to connect My/Myy/Myx/Myz/Mz and Mz+1 when one of these metals has a width and length $> 1.62 \mu\text{m}$			
VIAz.R.3	At least two VIAz must be used for a connection that distance $\leq 4.5 \mu\text{m}$ (D) away from a metal plate (either My/Myy/Myx/Myz/Mz or Mz+1) with length $> 9 \mu\text{m}$ (L) and width $> 2.7 \mu\text{m}$ (W)			
VIAz.R.4	VIAz must be fully covered by {My AND Mz+1} or {Myy AND Mz+1} or {Myx AND Mz+1} or {Myz AND Mz+1} or {Mz AND Mz+1} (Except following conditions: 1. top VIA inside CBMFFINAL)			
VIAz.R.13	Maximum area ratio of My/Myy/Myx/Myz/Mz to upper VIAz in the same net [connects to gate with area $> 10700 \mu\text{m}^2$, and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = $(2.5 \times W \times D \times L_d)$ for ≥ 2 -fin device		\leq	350000
VIAz.R.13.2	Maximum area ratio of I/O gate to single layer VIAz in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area $\geq 0.25 \mu\text{m}^2$) Definition: Gate area = $(2.5 \times W \times D \times L_d)$ for ≥ 2 -fin device		\leq	300000

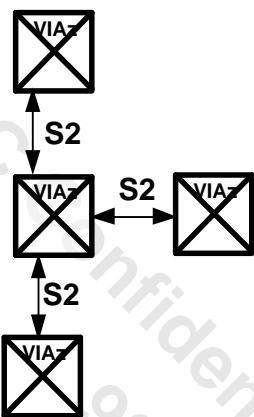
VIAz



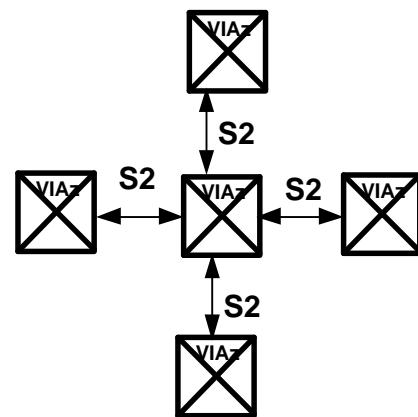
VIAz.W.1



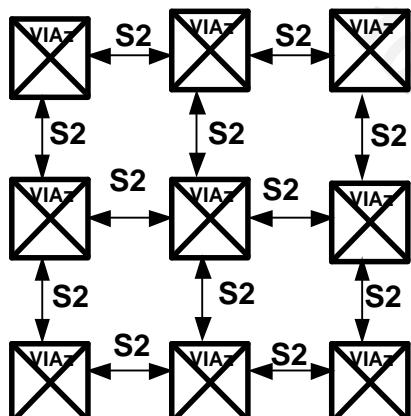
3-neighboring VIAz



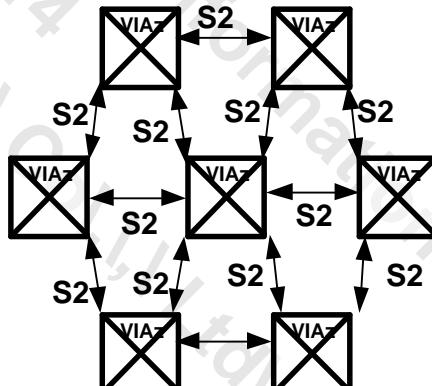
3-neighboring VIAz



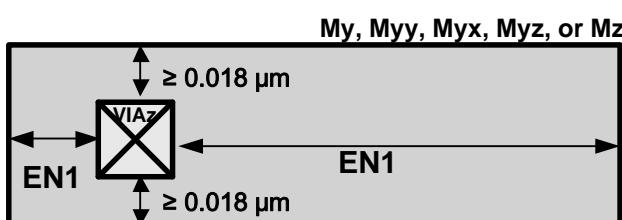
4-neighboring VIAz



3 X 3 array of VIAz



VIAz.S.1 / VIAz.S.2

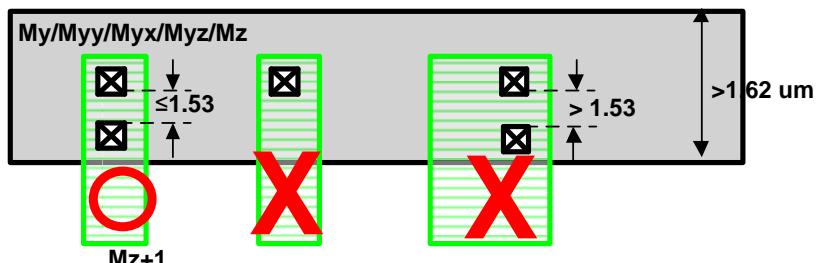


VIAz.EN.1

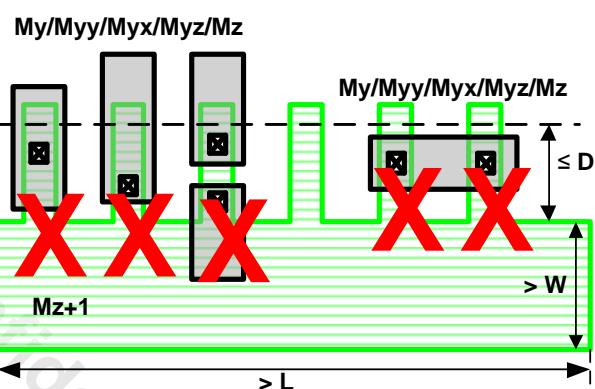
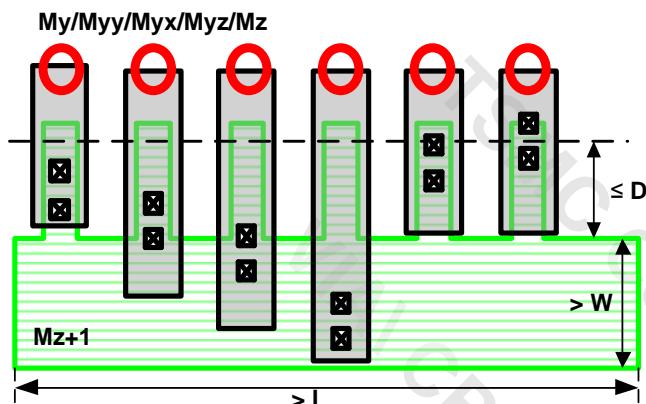
45-degree rotated VIAz is not allowed.



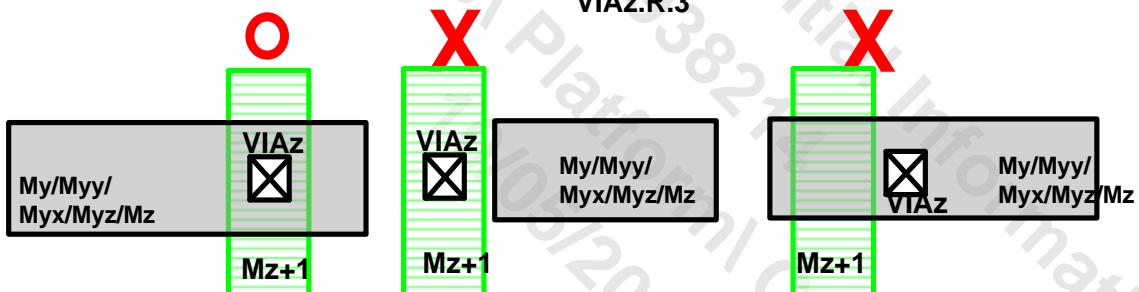
VIAz.R.1



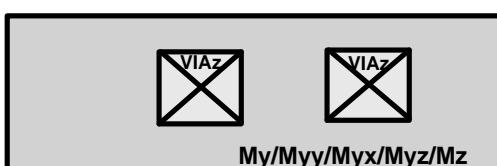
VIAz.R.2



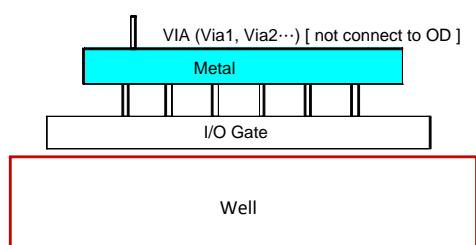
VIAz.R.3



VIAz.R.4



VIAz.R.13



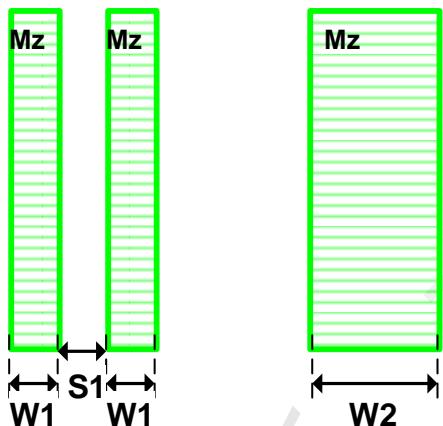
$$\frac{\text{IO Gate Area}}{\text{VIAz Area}} \leq 300000$$

VIAz.R.13.2

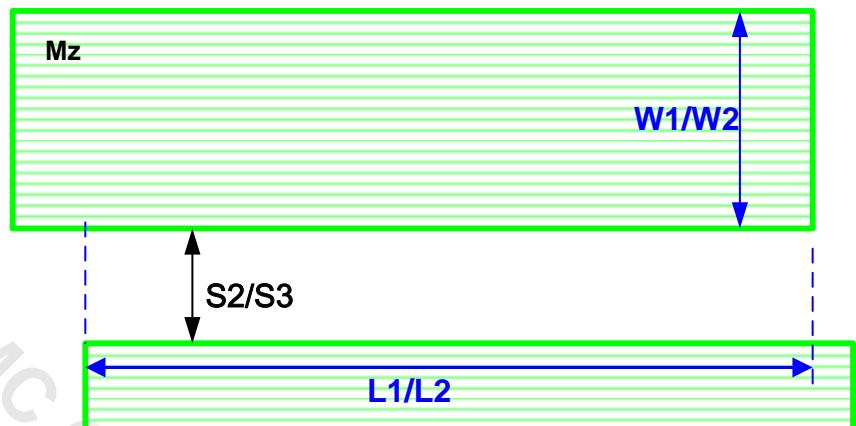
4.5.61 Mz Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

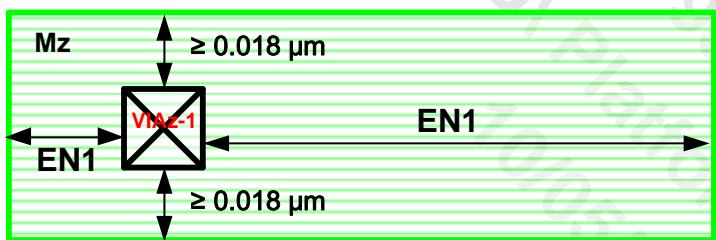
Rule No.	Description	Label	Op.	Rule
Mz.W.1	Width	W1	\geq	0.3600
Mz.W.2	Maximum width (Except following conditions: 1. bond pad, 2. {INDDMY SIZING 19.8 μm })	W2	\leq	10.8
Mz.S.1	Space	S1	\geq	0.3600
Mz.S.2	Space to Mz [width > 1.35 μm (W1) and the PRL > 1.35 μm (L1)]	S2	\geq	0.4500
Mz.S.3	Space to Mz [width > 4.05 μm (W2) and the PRL > 4.05 μm (L2)]	S3	\geq	1.35
Mz.EN.1	Enclosure of VIAz-1 for two opposite sides with the other two sides \geq 0.018 μm (Except SEALRING_ALL)	EN1	\geq	0.0720
Mz.A.1	Area	A1	\geq	0.50900
Mz.A.2	Enclosed area	A2	\geq	0.50900
Mz.DN.1.3	Minimum metal density in window 112 μm x 112 μm , stepping 56 μm (Except INDDMY)		\geq	10%
Mz.DN.2.1	Maximum metal density in window 112 μm x 112 μm , stepping 56 μm (Except LOGO, INDDMY, SEALRING_ALL, or following conditions: 1. bond pad, 2. Chip corner triangle empty areas if seal-ring is added by tsmc)		\leq	85%
Mz.DN.3.1	The metal density difference between any two neighboring checking windows including DMnEXCL [window 180 μm x 180 μm , stepping 180 μm]		\leq	50%
Mz.DN.5®	Recommended minimum metal density in window 50 μm x 50 μm , stepping 25 μm (Except LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	30%
Mz.R.1 ^U	Mz line-end must be rectangular. Other shapes are not allowed			
Mz.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
Mz.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of Mz space to Mz or VIAz-1 or VIAz is < 3.6 μm			
Mz.R.17	DMz is a must in chip level.			

Mz

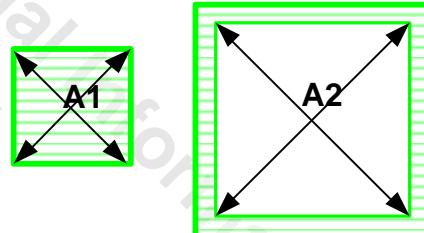
Mz.W.1 / Mz.W.2 / Mz.S.1



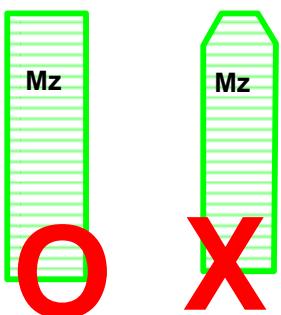
Mz.S.2 / Mz.S.3



Mz.EN.1



Mz.A.1 / Mz.A.2



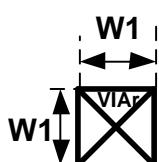
Mz line-end must be rectangular.

Mz.R.1^U

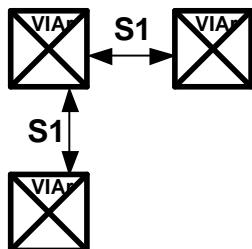
4.5.62 VIAr Layout Rules

For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
VIAr.W.1	Width (square)(maximum = minimum) (Except SEALRING_ALL)	W1	=	0.4140
VIAr.S.1	Space	S1	\geq	0.3960
VIAr.S.2	Space to 3-neighboring VIAr (distance \leq 0.594 μm distance) (Except following conditions: 1. 2*2 array on the same net)	S2	\geq	0.5940
VIAr.S.2.1	Space of 2*2 array on the same net	S2A	\geq	0.4860
VIAr.EN.1	Enclosure by My, Myy, Myx, Myz, Mz, or Mr for two opposite sides with the other two sides \geq 0.018 μm (Except SEALRING_ALL, or following conditions: 1. top VIA inside CBMFINAL)	EN1	\geq	0.0720
VIAr.R.1	45-degree rotated VIAr is not allowed			
VIAr.R.2	At least two VIAr with spacing \leq 1.53 μm are required to connect My/ Myy/ Myx/Myz/Mz/Mr and Mr+1 when one of these metals has a width and length $>$ 1.62 μm .			
VIAr.R.3	At least two VIAr must be used for a connection that distance \leq 4.5 μm (D) away from a metal plate (either My/Myy/Myx/Myz/Mz/Mr or Mr+1) with length $>$ 9 μm (L) and width $>$ 2.7 μm (W)			
VIAr.R.4	VIAr must be fully covered by {Mr AND Mr+1} or {Mz AND Mr+1} or {My AND Mr+1} or {Myy AND Mr+1} or {Myx AND Mr+1} or {Myz AND Mr+1} (Except following conditions: 1. top VIA inside CBMFINAL)			
VIAr.R.13	Maximum area ratio of My/Myy/Myx/Myz/Mz/Mr to upper VIAr in the same net [connects to gate with area $>$ 10700 μm^2 , and does not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	350000
VIAr.R.13.2	Maximum area ratio of I/O gate to single layer VIAr in the same net [not connect to OD] This rule is checked by the DRC command files in ANTENNA_DRC directory (Except following conditions: 1. Protection OD area \geq 0.25 μm^2) Definition: Gate area = (2.5xWdxLd) for \geq 2-fin device		\leq	300000

VIAr

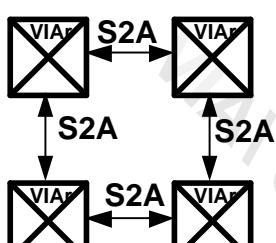
VIAr.W.1



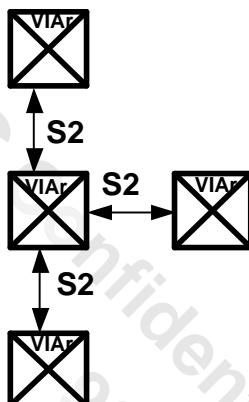
2-neighboring VIAr



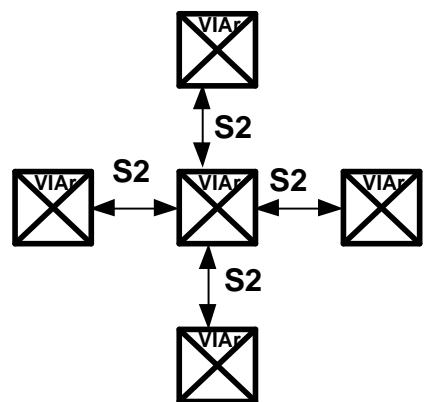
2-neighboring VIAr



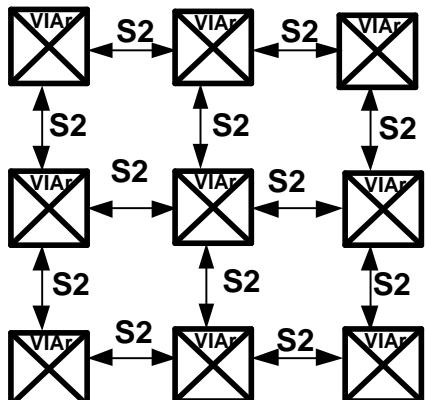
2 X 2 array of VIAr



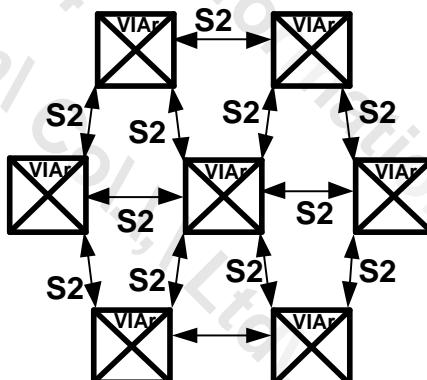
3-neighboring VIAr



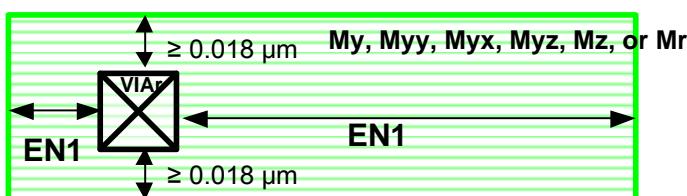
4-neighboring VIAr



3 X 3 array of VIAr



VIAr.S.1 / VIAr.S.2 / VIAr.S.2.1

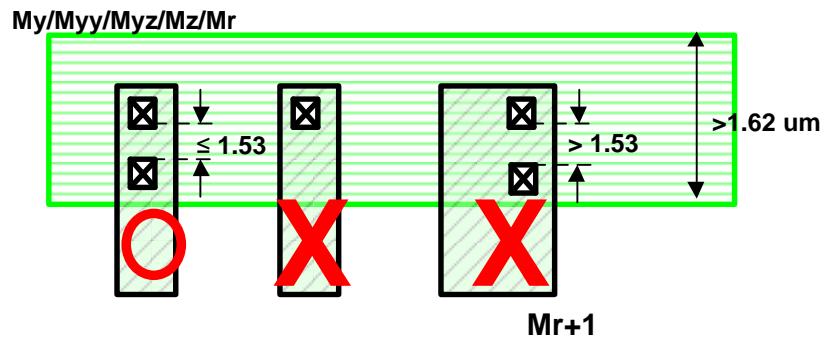


VIAr.EN.1

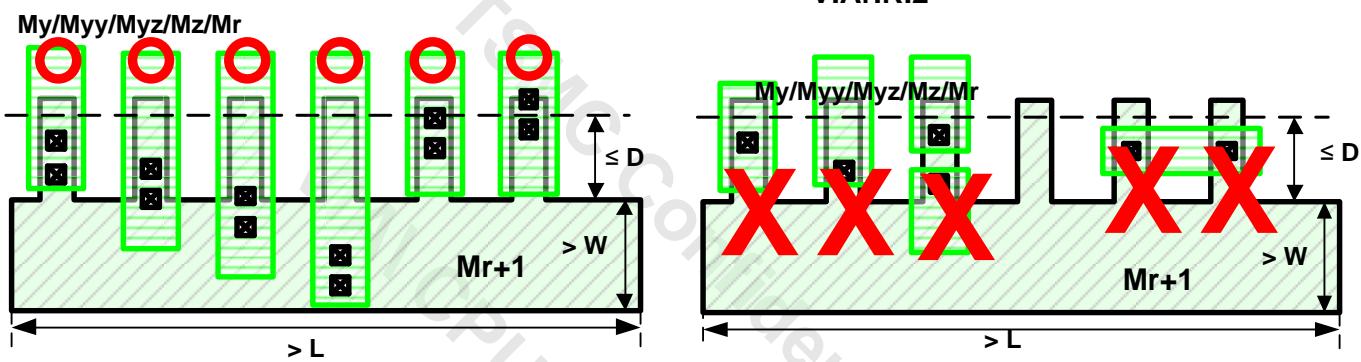
45-degree rotated VIAr is not allowed.



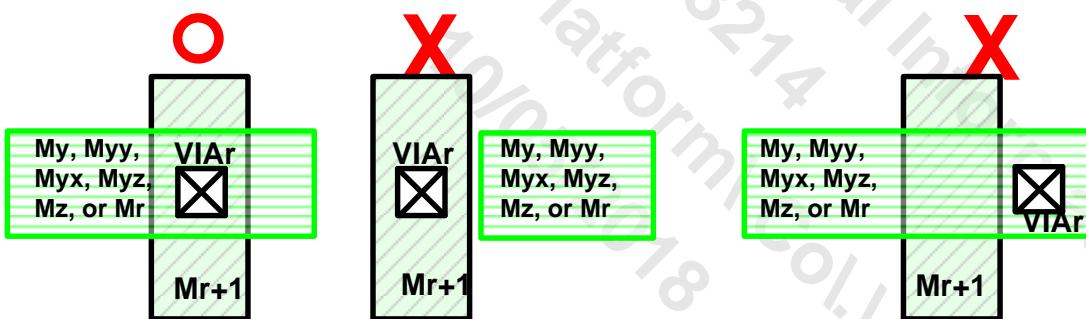
VIAr.R.1



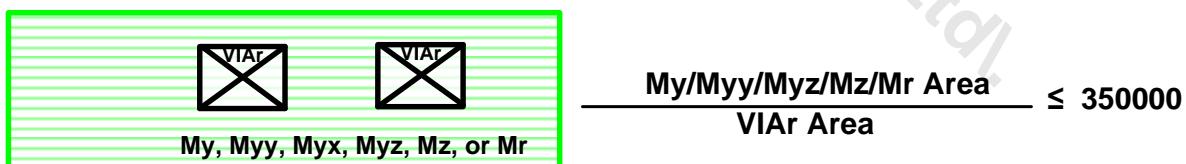
VIAr.R.2



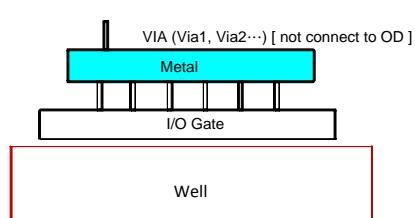
VIAr.R.3



VIAr.R.4



VIAr.R.13



$$\frac{\text{IO Gate Area}}{\text{VIAr Area}} \leq 300000$$

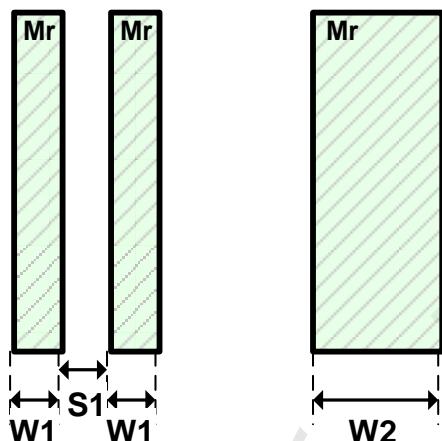
VIAr.R.13.2

4.5.63 Mr Layout Rules

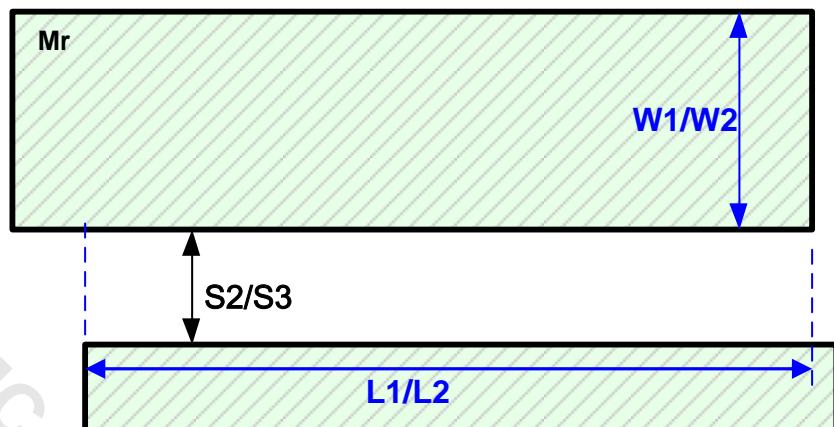
For the specification of metals/VIAs stacking sequence and associated mask ID, please refer to section 2.5.

Rule No.	Description	Label	Op.	Rule
Mr.W.1	Width	W1	\geq	0.4500
Mr.W.2	Maximum width (Except following conditions: 1. bond pad, 2. {INDDMY SIZING 19.8 μm })	W2	\leq	10.8
Mr.S.1	Space	S1	\geq	0.4500
Mr.S.2	Space to Mr [width > 1.35 μm (W1) and the PRL > 1.35 μm (L1)]	S2	\geq	0.5850
Mr.S.3	Space to Mr [width > 4.05 μm (W2) and the PRL > 4.05 μm (L2)] Note: When Mr width > 8.1 μm is used, take care of the Mr.DN.2.1 rule by using larger space	S3	\geq	1.35
Mr.EN.1	Enclosure of VIAr-1 for two opposite sides with the other two sides \geq 0.018 μm (Except SEALRING_ALL)	EN1	\geq	0.0720
Mr.A.1	Area	A1	\geq	0.81000
Mr.A.2	Enclosed area	A2	\geq	0.81000
Mr.DN.1.3	Minimum metal density in window 112 μm x 112 μm , stepping 56 μm (Except INDDMY)		\geq	10%
Mr.DN.2.1	Maximum metal density in window 112 μm x 112 μm , stepping 56 μm (Except LOGO, SEALRING_ALL, INDDMY, or following conditions: 1. bond pad, 2. Chip corner triangle empty areas if seal-ring is added by tsmc)		\leq	85%
Mr.DN.3.1	The metal density difference between any two neighboring checking windows including DMnEXCL [window 180 μm x 180 μm , stepping 180 μm]		\leq	50%
Mr.DN.5®	Recommended minimum metal density in window 50 μm x 50 μm , stepping 25 μm (Except LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		\geq	30%
Mr.R.1 ^U	Mr line-end must be rectangular. Other shapes are not allowed			
Mr.R.3	Metal (pin) layers must be drawn only interact one relative Metal (drawing) layers			
Mr.R.11	Maximum delta V > 3.63V is not allowed. DRC searching range of Mr space to Mr or VIAr-1 or VIAr is < 4.5 μm			
Mr.R.17	DMr is a must in chip level.			

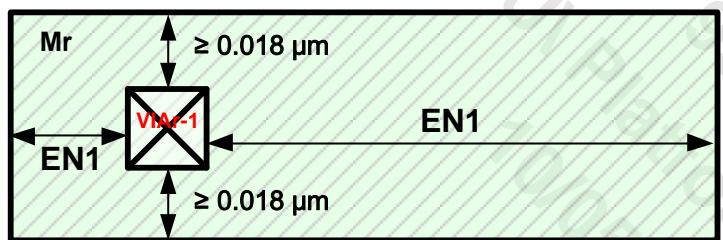
Mr



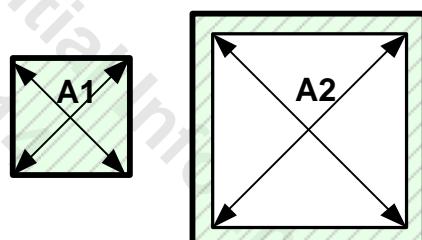
Mr.W.1 / Mr.W.2 / Mr.S.1



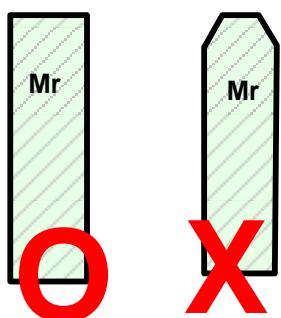
Mr.S.2 / Mr.S.3



Mr.EN.1



Mr.A.1 / Mr.A.2



Mr line-end must be rectangular.

Mr.B.1^U

4.5.64 MOM Layout Rules

- MOM is a fringe Metal-Oxide-Metal capacitor, which is mainly based on the capacitance between parallel metal lines separated by inter-level dielectric. The device does not require any additional mask.
- Although various kinds of metal combination are allowed to build a MOM element in terms of process, TSMC only provides MOM SPICE model and PDK with limited metal combinations. Please refer to below table.

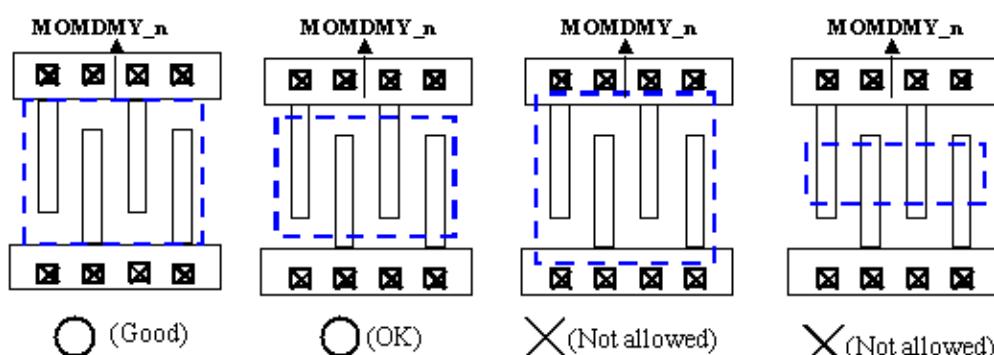
	Non-TSMC MOM structure			TSMC MOM structure		
	SPICE	PDK	Process	SPICE	PDK	Process
M0/M1/Mx/Mxa/Mya/My	X	X	O	O	O	O
Other Metals	X	X	O	X	X	O

O: available X: not available

- Special dummy layers for MOM.

Layer name	CAD layer	Description	Non-TSMC MOM structure	TSMC MOM structure
MOMDMY_0	155;180	DRC/LVS dummy layer for M0 MOM	O	O
MOMDMY_1	155;1	DRC/LVS dummy layer for M1 MOM	O	O
MOMDMY_2	155;2	DRC/LVS dummy layer for M2 MOM	O	O
MOMDMY_3	155;3	DRC/LVS dummy layer for M3 MOM	O	O
MOMDMY_4	155;4	DRC/LVS dummy layer for M4 MOM	O	O
MOMDMY_5	155;5	DRC/LVS dummy layer for M5 MOM	O	O
MOMDMY_6	155;6	DRC/LVS dummy layer for M6 MOM	O	O
MOMDMY_7	155;7	DRC/LVS dummy layer for M7 MOM	O	O
MOMDMY_8	155;8	DRC/LVS dummy layer for M8 MOM	O	O
MOMDMY_9	155;9	DRC/LVS dummy layer for M9 MOM	O	O
MOMDMY_10	155;10	DRC/LVS dummy layer for M10 MOM	O	O
MOMDMY_AP	155;20	DRC/LVS dummy layer for AP MOM	O	X
MOMDMY	155;21	DRC dummy layer to recognize MOM for DRC check	X	O
MOMDMY_22	155;22	LVS dummy layer for multi-cross coupled MOM	X	O
MOMDMY_23	155;23	LVS dummy layer for multi-cross couple MOM plus1 & minus1	X	O
MOMDMY_24	155;24	LVS dummy layer for multi-cross couple MOM plus2 & minus2	X	O
MOMDMY_25	155;25	LVS dummy layer for multi-cross couple MOM plus1 & plus2	X	O
MOMDMY_27	155;27	For LVS/PDK to verify 2T MOM	X	O
MOMDMY_31	155;31	For LVS/PDK to verify N-Well under MOM without poly shield	X	O
MOMDMY_32	155;32	For LVS/PDK to verify P-Well under MOM without poly shield	X	O
MOMDMY_33	155;33	For LVS/PDK to verify NTN-Well under MOM without poly shield	X	O

- In order to have a good DRC check, you need to draw the MOMDMY_n carefully. The following examples are for your reference.



- Please pay attention to meet metal local density rules above/under MOM element. If you want to design a MOM circuit with a large area, it is recommended to either use tsmc PDK MOM build-in dummy metal insertion option or insert dummy metal to the customized MOM by customer to meet design rules.
- For better matching performance,
 - the Multi-X Couple layout is recommended for large capacitor pair. (Please refer to “MOM (Metal Oxide Metal) Capacitor Guidelines” section).
 - Using symmetrical dummy metals around matching pairs, instead of using automatically generated dummy metals.
 - Carefully design wire access to capacitor terminals to ensure an optimal symmetry of the device environment.

Rule No.	Description	Label	Op.	Rule
MOM.L.1	PRL of MOM fingers [finger space < 0.038 μm (S1)] (This check is only applied to M0/M1/Mxs/Mx/Mxa)	D	≤	32
MOM.A.0	Maximum sidewall area of total metals in MOM are defined by: M0/M1/Mxs/Mx/Mxa: MOM.A.1.1~MOM.A.1.6 Mya/My: MOM.A.2.1~MOM.A.2.5 Myy: MOM.A.4.1~MOM.A.4.3 For the definition of the sidewall area of total metals, refer to the following table			
MOM.A.1.1	Maximum sidewall area of total M0/M1/Mxs/Mx/Mxa metals in MOM without Via [0V ≤ delta Vmax ≤ 0.96V]	C	≤	1.00E+07
MOM.A.1.2	Maximum sidewall area of total M0/M1/Mxs/Mx/Mxa metals in MOM without Via [0.96V < delta Vmax ≤ 1.32V]	C	≤	1.00E+07
MOM.A.1.3	Maximum sidewall area of total M0/M1/Mxs/Mx/Mxa metals in MOM without Via [1.32V < delta Vmax ≤ 1.65V]	C	≤	1.00E+07
MOM.A.1.4	Maximum sidewall area of total M0/M1/Mxs/Mx/Mxa metals in MOM without Via [1.65V < delta Vmax ≤ 1.98V]	C	≤	1.00E+07
MOM.A.1.5	Maximum sidewall area of total M0/M1/Mxs/Mx/Mxa metals in MOM without Via [1.98V < delta Vmax ≤ 2.75V]	C	≤	1.00E+07
MOM.A.1.6	Maximum sidewall area of total M0/M1/Mxs/Mx/Mxa metals in MOM without Via [2.75V < delta Vmax ≤ 3.63V]	C	≤	1.00E+07
MOM.A.2.1	Maximum sidewall area of total Mya/My metals in MOM without Via [0V ≤ delta Vmax ≤ 1.32V]	C	≤	1.83E+09
MOM.A.2.2	Maximum sidewall area of total Mya/My metals in MOM without Via [1.32V < delta Vmax ≤ 1.65V]	C	≤	1.34E+08
MOM.A.2.3	Maximum sidewall area of total Mya/My metals in MOM without Via [1.65V < delta Vmax ≤ 1.98V]	C	≤	1.00E+07
MOM.A.2.4	Maximum sidewall area of total Mya/My metals in MOM without Via [1.98V < delta Vmax ≤ 2.75V]	C	≤	1.00E+07
MOM.A.2.5	Maximum sidewall area of total Mya/My metals in MOM without Via [2.75V < delta Vmax ≤ 3.63V]	C	≤	1.00E+07
MOM.A.4.1	Maximum sidewall area of total Myy metals in MOM without Via [0V ≤ delta Vmax ≤ 1.98V]	C	≤	3.74E+08
MOM.A.4.2	Maximum sidewall area of total Myy metals in MOM without Via [1.98V < delta Vmax ≤ 2.75V]	C	≤	2.04E+07
MOM.A.4.3	Maximum sidewall area of total Myy metals in MOM without Via [2.75V < delta Vmax ≤ 3.63V]	C	≤	1.18E+06
MOM.R.1	VIA in MOMDMY is not allowed.			
MOM.R.2	Each MOM cell must be covered by MOMDMY_n (n = 0~10/20/21) in chip level. DRC flags no MOMDMY_n (n = 0~10/20/21) in Chip_Boundary. But if there is no MOM cell in Chip_Boundary, the violation can be waived.			

**The rule values of MOM.A.1.1~ MOM.A.1.6 & MOM.A.2.1~ MOM.A.2.5 are based on the corresponding maximum sidewall table with minimal allowed space for the given delta V_{max}. If your layout violates those rules but the metal space is not the same as this condition, please refer to the following table to check the rules again.

M0/M1/Mxs/Mx/Mxa Maximum Sidewall Table

Voltage\ Space	$0V \leq \delta V_{max} \leq 0.96V$	$0.96V < \delta V_{max} \leq 1.32V$	$1.32V < \delta V_{max} \leq 1.65V$	$1.65V < \delta V_{max} \leq 1.98V$	$1.98V < \delta V_{max} \leq 2.75V$	$2.75V < \delta V_{max} \leq 3.63V$
$\geq 0.020 \mu m$	1.00E+07					
$\geq 0.052 \mu m$	4.24E+08	1.00E+07				
$\geq 0.055 \mu m$	8.41E+08	1.48E+07	1.00E+07			
$\geq 0.061 \mu m$	1.39E+09	2.68E+07	1.28E+07	1.00E+07		
$\geq 0.069 \mu m$	1.92E+09	5.61E+07	2.93E+07	1.64E+07	1.00E+07	
$\geq 0.079 \mu m$	1.92E+09	1.17E+08	6.68E+07	4.04E+07	1.92E+07	1.00E+07

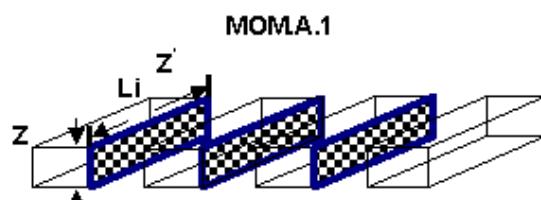
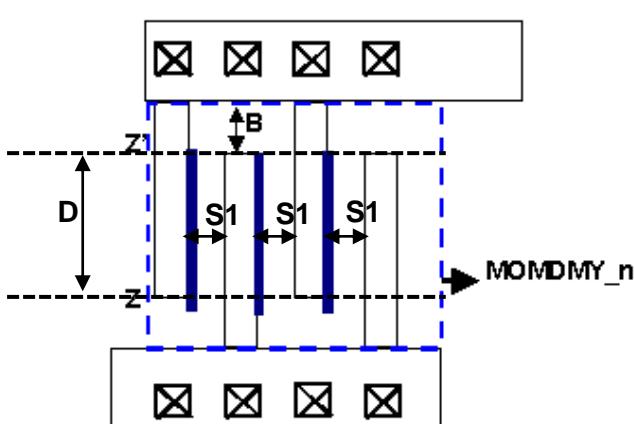
Mya/My Maximum Sidewall Table

Voltage/ Space	$0V < \delta V_{max} \leq 1.32V$	$1.32V < \delta V_{max} \leq 1.65V$	$1.65V < \delta V_{max} \leq 1.98V$	$1.98V < \delta V_{max} \leq 2.75V$	$2.75V < \delta V_{max} \leq 3.63V$
$\geq 0.038 \mu m$	1.83E+09	1.34E+08	1.00E+07	-----	-----
$\geq 0.046 \mu m$	1.83E+09	1.83E+09	1.75E+09	1.00E+07	-----
$\geq 0.080 \mu m$	1.83E+09	1.83E+09	1.83E+09	4.44E+08	1.00E+07

Myy Maximum Sidewall Table

Voltage	$0V \leq \delta V_{max} \leq 1.98V$	$1.98V < \delta V_{max} \leq 2.75V$	$2.75V < \delta V_{max} \leq 3.63V$
Max Sidewall Area (μm^2) (Space(μm))	3.74E+08 (S=0.064)	2.04E+07 (S=0.064)	1.18E+06 (S=0.064)

MOM without Via



$$C = \text{Total metal sidewall area}$$

$$= \sum_{i=1}^n H_i \times L_i$$

L_i = finger length

H_i = metal thickness

n =total metal finger number-1

4.5.64.1 MOM (Metal Oxide Metal) Capacitor Guidelines

This section lists the guidelines for MOM PDK cell application.

1. The offered MOM cell in PDK is implemented by M0/M1/Mx/Mxa/Mya/My.
2. MOM PDK cell has pre-inserted uniform dummy OD, dummy PO, dummy MD, dummy MP, and dummy metal patterns underneath MOM to meet design rule requirement.
3. Please note that the MOM SPICE model is built based on the layout provided in PDK, any modification to the MOM layout provided in PDK would have the risk for model inaccuracy and design flow issue (e.g. LVS recognition fail).
4. The Multi-X Couple layout is recommended for large capacitor pair design, which can improve the matching performance. The Parallel and Multi-X Couple layout for match pairs is illustrated in Figure MOM Parallel and Figure MOM Multi-X.
 - The unit cell C1 and the unit cell C2 of the Multi-X Couple MOM are placed in an array with alternate pattern placement in each row and each column.
 - For example, if the total capacitance $C > 200fF$ is required, it is recommended to use Multi-X Couple layout type with unit cell $<<100fF$, to improve the matching performance. It is not recommended to use $2 \times 100fF$ Parallel MOM design.

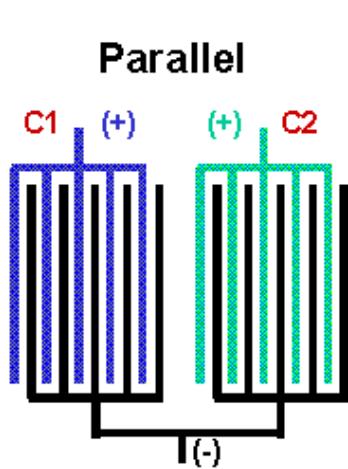


Figure Parallel

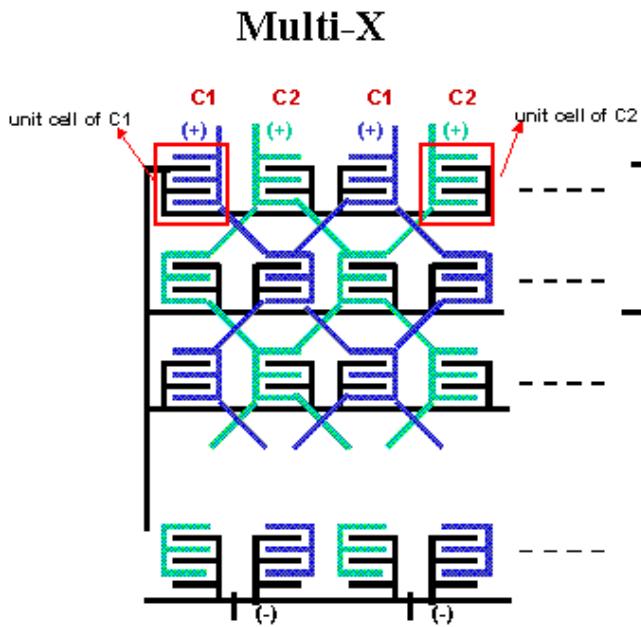


Figure Multi-X

5. In order to make sure the SPICE simulation accuracy, and avoid the density rule violation, the following guidelines are recommended.
 - The dummy metal exclusive layers (DMnEXCL) are adopted under MOM to avoid dummy pattern insertion. To meet strict local metal density rules, it is highly recommended to use MOM layout in PDK with pre-inserted dummy metal. If dummy metal (not generated by PDK itself) are added into the region below/above the MOM generated by PDK, the resulting extra parasitic and model inaccuracy must be taken into consideration by designers.
 - If the metal density rule is violated due to the large area of MOM, parallel connected small MOMs array with dummy metals between individual MOM is recommended, as shown in Figure MOM array with dummy metals.

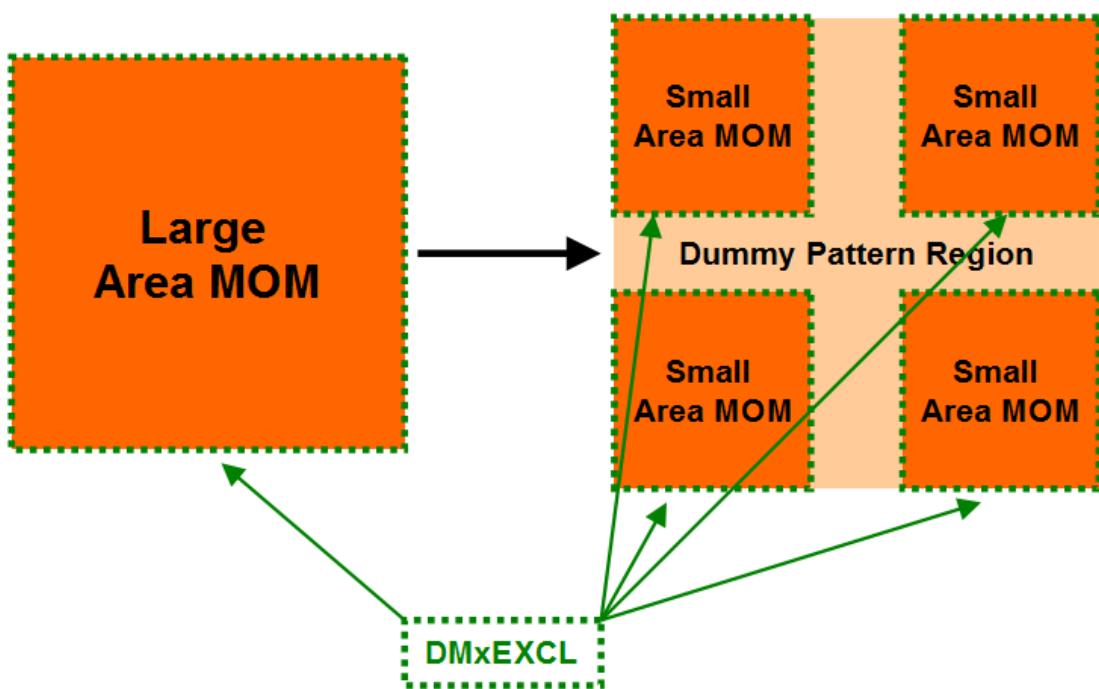


Figure MOM array with dummy metals

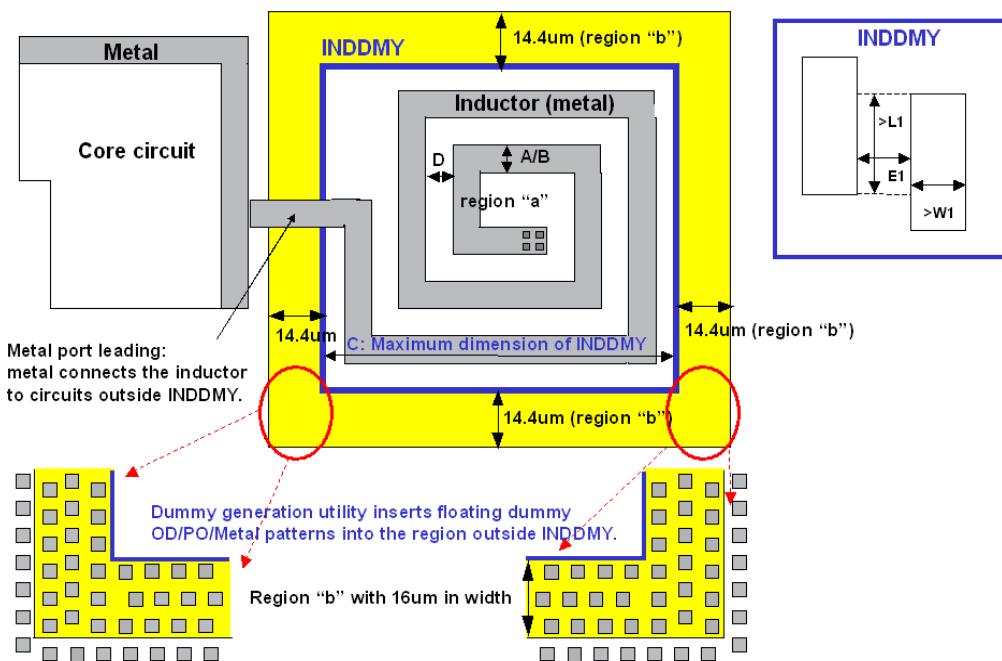
4.5.65 INDDMY Layer Identified Inductor Layout Rules

For eddy current reduction to achieve better inductor performance, a special OD/PO/MD/Metal dummy block layer called “INDDMY” (144;0) is offered to allow customized metal patterns within an inductor, provided a proper surrounding (dummy) metal scheme requirement is satisfied. When “INDDMY” layer is used to construct inductors, one must follow the additional process-related design rules listed below. Please be noted that “INDDMY” can only be used for inductor devices, TSMC does not support the non-inductor devices constructed with “INDDMY”. Inductor devices offered in TSMC PDK can fit the design rule listed below. For customized inductors using this “INDDMY” layer that meets the following design rules, it is still suggested to perform the necessary sanity check to avoid undesired layout mistake due to possible design rule deficiency. For better process robustness, the thin inter-metals with ELK dielectric (including M0, M1, Mxs, Mx, Mxa, Mya, My, Myy) are no longer allowed to waive the low density related rules in inductor region. Those thin inter-metals with ELK dielectric must follow the associated logic design rules. Please be aware of the compulsory metal insertion in inductor region would impact inductor performances. Besides, since the thin inter-metals with ELK dielectric inside inductor region are logic rule compliant, the associated VIAs are also allowed in the inductor region.

Rule No.	Description	Label	Op.	Rule
IND.W.2	Mz and DMz width in {INDDMY SIZING 14.4 μm }	A2	\geq	0.7200
IND.W.3	Mr and DMr width in {INDDMY SIZING 14.4 μm }	A3	\geq	0.9000
IND.W.4	Mz and DMz /Mr and DMr maximum width inside {INDDMY SIZING 19.8 μm } (for inductor application only)	B	\leq	27
IND.W.5	Maximum dimension (either width or length) of an INDDMY	C	\leq	600
IND.W.6	Myz and DMyz width in {INDDMY SIZING 14.4 μm }		\geq	0.3600
IND.S.2	Mz and DMz space in {INDDMY SIZING 14.4 μm }	D2	\geq	0.7200
IND.S.3	Mr and DMr space in {INDDMY SIZING 14.4 μm }	D3	\geq	0.9000
IND.S.4	Mz, and DMz /Mr, and DMr space in {INDDMY SIZING 14.4 μm } to [width > 10.8 μm (W1) and the PRL > 10.8 μm (L1)]	E1	\geq	1.8
IND.S.6	Myz and DMyz space in {INDDMY SIZING 14.4 μm }		\geq	0.3600
IND.DN.1	Maximum density of INDDMY across full chip		\leq	5%
IND.DN.2	Myz/Mz/Mr metal density across full chip (include INDDMY)		\leq	20%
IND.DN.3	Maximum density of INDDMY in window 1440 μm x 1440 μm , stepping 720 μm		\leq	14%
IND.R.2	At least four VIAz with space \leq 1.53 μm are required to connect Myx/Myz/Mz to Mz+1 in {INDDMY SIZING 14.4 μm } (DRC checks VIAz counts including VIAz beside {INDDMY SIZING 14.4 μm })		\leq	1.53
IND.R.4	At least four VIAr with space \leq 1.53 μm are required to connect Myx/Myz/Mz/Mr to Mr+1 in {INDDMY SIZING 14.4 μm } (DRC checks VIAr counts including VIAr beside {INDDMY SIZING 14.4 μm })		\leq	1.53
IND.R.7	A 45-degree rotated RV is allowed inside {INDDMY SIZING 19.8 μm }			
IND.R.8 ^U	Guard-ring enclosure of inductor metal spirals. 1. The larger distance (such as 50 μm) from inductor metal spirals to guard-ring would make better inductor electrical performance and reduce the coupling on/between components nearby. Take the impact of the guard-ring enclosure of inductor metal spirals into consideration. 2. Keep the INDDMY regions of separate inductors located as uniform as possible in Chip_Boundary to maintain CMP uniformity.			
IND.R.9	A 0.005 μm checking tolerance is allowed for the rules: IND.W.2, IND.W.3, IND.W.4, IND.S.2, IND.S.3, IND.S.4			
IND.R.10	A 0.009 μm checking tolerance in {INDDMY SIZING 14.4 μm } is allowed for the listed regular logic rules: Mz.S.3, RV.W.1, RV.S.1, RV.EN.1, AP.W.1, AP.W.2, and AP.EN.1. Note: DRC implement 0.009 μm tolerance on Vertical, Horizontal, and 45-degree bent.			
IND.R.11g ^U	Recommend putting NT_N to fully cover the inductor (metal) to achieve the high quality factor.			

Table Notes:

1. The INDDMY layer (144;0) blocks the automated dummy patterns generation.
2. It is required to put SR_DOD and, SR_DPO, and thin inter-metals with ELK dielectric (including M0, M1, Mx, Mxa, Mya, My, and Myy) dummy patterns inside INDDMY region for process robustness consideration. And, the density of dummy patterns should be larger than design rule requirements and recommended to be as low as possible to minimize the electrical performance impact due to dummy insertion.
3. For TSMC PDK offered inductor, a native substrate region is created under inductor coil to minimize eddy currents. This region is specified/implemented by the implant blocking NT_N layer (CAD layer: 11;0). The NT_N drawn layer adds no process cost and no extra mask.
4. TSMC offered PDK inductor is octagonal type, the square type inductor in Figure IND is only for rule illustrations.
5. For an inductor to be with dummy patterns inserted by TSMC dummy utility, the INDDMY layer (144;0) should be removed. If the inductor layout is already compliant with all logic design rules, there is no need to draw the INDDMY layer for the inductor.
6. Please put as many VIAs as possible for reliability and RF applications for IND.R.2, and IND.R.4.
7. The above inductor rule descriptions are based on the concept of different regions ("a" and "b") from center to edge to achieve the flexibility of design easiness and maintaining density for uniformity. Please refer to Figure IND.
8. It is not recommended to put devices or sensitive metal routings inside inductor region, unless the coupling and electrical performance impacts are properly assessed.

**Figure IND**

4.5.66 Product Labels and Logo Layout Rules

1. Use any of the following product labels:

- Copyright and year
- Company logo
- Part number
- Mask level names
- Other similar labels

2. For OD layer, Manual Mandrel is not allowed, OD have to follow the rule (on-grid), recommend to refer to “tsmc label” which apply “MOSAIC” approach with “unit cell” to make label.

3. Make sure there is a dummy layer LOGO (CAD layer no. 158) to do DRC for product labels.

- Product labels must be fully covered by LOGO dummy layer.

4. Form the product labels for the V0/Via layer by using squares with minimum width.

- A big V0/Via polygon for a character (or a numeral) is not allowed.

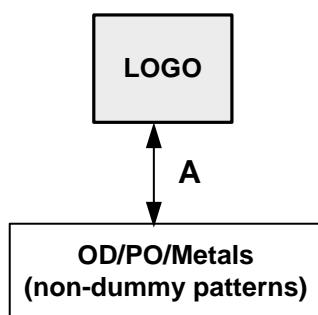
5. Don't use minimum rules for the product labels, except for V0/Vias.

It is best to have greater than, or equal to, 1 μm of width and space. If the minimum width and space is greater than 1 μm in the rule (for example, 30K thick metal) please use at least the minimum width and space.

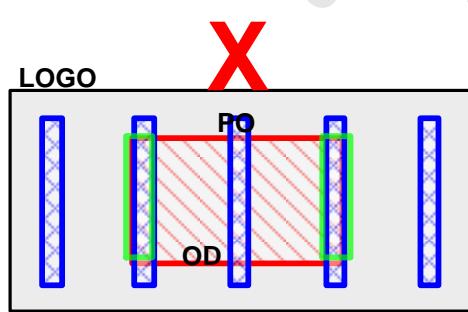
6. TSMC's dummy fill generation utilities insert dummy patterns into LOGO (158;0) by default.

If you don't want to fill dummy patterns into LOGO (158;0), properly use the dummy pattern exclusion layers, e.g. DMnEXCL (150;n), and take care of associated rules, e.g. density rules.

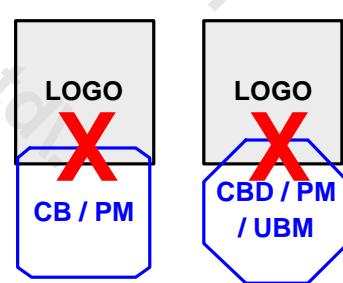
Rule No.	Description	Label	Op.	Rule
LOGO.S.1	Space to OD, PO, MD, or Metals (non-dummy patterns)	A	\geq	10
LOGO.R.1 ^U	A circuit in the LOGO is not allowed.			
LOGO.R.3	Overlap of CB, CBD, PM, or UBM is not allowed.			



LOGO.S.1



LOGO.R.1



LOGO.R.3

4.5.67 SRAM Layout Rules

Rule No.	Description	Label	Op.	Rule
SRAM.W.1	At least 8 bitcell + 2 edge cell are required in horizontal direction in a single SRAM array. DRC checks : SRAMDMY width in horizontal direction \geq 1.824 μm .			
SRAM.W.1.1	At least 8 bitcell + 2 edge cell are required in vertical direction in a single SRM_11 (50;11) & SRM_12 (50;12) SRAM array. At least 6 bitcell + 2 edge cell for other cells. DRC checks : SRM_11 (50;11) array width in vertical direction \geq 2.4 μm . SRM_12 (50;12) array width in vertical direction \geq 3.0 μm . SRM_14 (50;14) array width in vertical direction \geq 4.08 μm . SRM_15 (50;15) array width in vertical direction \geq 4.32 μm . SRM_17 (50;17) array width in vertical direction \geq 5.88 μm . SRM_21 (50;21) array width in vertical direction \geq 5.64 μm . SRM_23 (50;23) array width in vertical direction \geq 4.80 μm .			
SRAM.W.2	Width of OD_DA (6;15) [INSIDE {SRM (50;0) OR SRAMDMY (186;0)}]	W2	\geq	0.0380
SRAM.W.3	Width of COD_H (6;17) [INSIDE {SRM (50;0) OR SRAMDMY (186;0)}]	W3	\geq	0.0480
SRAM.W.4	Width of COD_V (6;18) [INSIDE {SRM (50;0) OR SRAMDMY (186;0)}]	W4	\geq	0.0560
SRAM.W.5	Width/length of DUMMYMO_18 (83;18) [INTERACT CO_SRAM18 (30;18)]	W5	$=$	0.0120/0.0120
SRAM.W.5.1	Width/length of DUMMYMO_18 (83;18) [NOT INTERACT CO_SRAM18 (30;18)]	W5A	$=$	0.0120/0.0150
SRAM.S.1	Space of SRAMDMY (186;0)	S1	\geq	0.1140
SRAM.S.3	Forbidden space of OD_DA (6;15) [INSIDE {SRM (50;0) OR SRAMDMY (186;0)}]	S3	$=$	0.0620~0.0790
SRAM.S.4	Space of COD_H (6;17) [INSIDE {SRM (50;0) OR SRAMDMY (186;0)}]	S4	\geq	0.0600
SRAM.S.5	Space of COD_V (6;18) [INSIDE {SRM (50;0) OR SRAMDMY (186;0)}]	S5	\geq	0.0560
SRAM.S.9	Space of SRM_11, SRM_12, SRM_14, SRM_15, SRM_17, SRM_21 [INSIDE {SRM (50;0) OR SRAMDMY (186;0)}] (Overlap is not allowed.)	S9	\geq	0.1440
SRAM.R.1 ^U	Customer-designed SRAM bit cell: Review by TSMC's R&D and PE before use a customer-designed SRAM bit cell. It is recommended to use the standard TSMC SRAM cells including core, edge, and strap cells. Non-tsmc-standard cell is not allowed, unless all logic rules are followed. (SRAMDMY (186;0), BLK_WB (255,11), SRM (50;0) and BLK_WF (255,10) can not be used) [Customer's product: need silicon to verify its function, performance, speed, and Vccmin before product tape-out.]			
SRAM.R.1.1 ^U	Logic SPICE model: Don't use a logic SPICE model to design SRAM unless the layout strictly follows the logic design rule for designing SRAM. The logic rule SRAM must be reviewed by TSMC R&D and PE.			
SRAM.R.2	BCWDMY must abut SRAMDMY from outside			
SRAM.R.2.2	BCWDMY must be a rectangle orthogonal to grid			
SRAM.R.2.3	BCWDMY edge [INTERACT SRAMDMY] must fully abut SRAMDMY			
SRAM.R.2.4	M2, M3 inside BCWDMY is not allowed			
SRAM.R.2.5	M2 interact horizontal edge of BCWDMY is not allowed			
SRAM.R.2.6	M3 interact vertical edge of BCWDMY is not allowed			
SRAM.R.2.7	M2 vertical edge [INTERACT BCWDMY, with M2 cut SRAMDMY] must abut BCWDMY			

Rule No.	Description	Label	Op.	Rule
SRAM.R.2.8	M3 horizontal edge [INTERACT BCWDMY, with M3 cut SRAMDMY] must abut BCWDMY			
SRAM.R.3	SRM_22 (50;22) must be drawn identically to SRAMDMY			
SRAM.R.6 ^U	Array delay-tracking bit cells: This kind of bit cell should be embedded inside an array. If a delay-tracking cell is to be placed OUTSIDE an array, it should be fully surrounded by TSMC SRAM standard dummy cells in TSMC IP.			
SRAM.R.9g ^U	Sense-amp and decoder redundancy: In addition to bit-row and/or bit-column redundancy design, redundancy in peripheral array elements, such as sense amplifiers and decoders, is recommended. Architectural efficiency can minimize the added overhead area entailed by this additional redundancy. Peripheral element redundancy is especially important for high-density memory blocks.			
SRAM.R.11g ^U	Guardring: It is recommended to have an additional VSS (PW) guardring around the memory circuit block.			
SRAM.R.14 ^U	Dummy layouts for embedded SRAM: To minimize proximity and loading effects during processing, you must add dummy layouts to provide a similar surrounding for every cell. To add dummy layouts, please refer to SRAM cell layout documents for guidelines and GDS examples. These documents provide instructions for adding dummy layouts in both columns and rows, at array edges, and at the connection/tap in-between arrays.			
SRAM.R.16 ^U	SRAM array layout, name, and hierarchy should follow TSMC layout such as strap cell, strap edge cell, column edge cell and row edge cell. The detail is described in SRAM cell layout and model document (Document number: T-N07-CL-CL-007).			
SRAM.R.17	SRAMDMY (186;0) must fully cover OD, MD, MP, VIA0, VIA1.			
SRAM.R.18	SRAMDMY (186;0) can not have any holes			
SRAM.R.20	BLK_M1 and {M1 (31;420) AND SRAMDMY} must be drawn identically			
SRAM.R.21	BLK_M2 must be drawn identically to {M2 AND SRAMDMY}			
SRAM.R.22	BLK_M3 must be drawn identically to {M3 AND SRAMDMY}			
SRAM.R.22.1	BLK_M4 must be drawn identically to {M4 AND SRAMDMY}			
SRAM.R.36	SRM (50;0), SRAMDMY(186;0) must be a rectangle orthogonal to grid			
SRAM.R.36.1	CPO_SRAM (17;12) [INSIDE {SRM (50;0) OR SRAMDMY(186;0)}] must be a rectangle orthogonal to grid			
SRAM.R.37	DUMMYM0_18 (83;18) must be fully inside SRAMDMY (186;0)			
SRAM.R.37.1	SRAMDMY (186;0) must interact DUMMYM0_18 (83;18)			
SRAM.R.38	{M1 CUT SRAMDMY} NOT INTERACT {{VIA0 AND SRAMDMY} OR {VIA1 AND SRAMDMY}} is not allowed			
SRAM.R.38.1	{M0 CUT SRAMDMY} NOT INTERACT {{VC AND SRAMDMY} OR {VIA0 AND SRAMDMY}} is not allowed			
SRAM.OD.R.1	OD_DA must be a rectangle orthogonal to grid [INSIDE SRM]			
SRAM.OD.R.2	SRM (50;0) must interact OD_DA			
SRAM.OD.R.3	Either one horizontal edge of {ALL_OD [INSIDE SRM, NOT INTERACT OD_DA] SIZING 0.022 μm in vertical direction} must abut OD_DA			
SRAM.COD_H.EX.1	ALL_COD_H [INSIDE SRM] extension on OD_DA in horizontal direction	EX1	=	0.0190
SRAM.COD_V.EN.1	SRM enclosure of ALL_COD_V in vertical direction	EN1	=	0, ≥ 0.0800
SRAM.COD_V.EX.1	ALL_COD_V [INSIDE SRM] extension on {ALL_OD SIZING 0.001 μm in horizontal direction} in vertical direction	EX1	≥	0.0200
SRAM.COD_V.EX.1.1	ALL_COD_V [INSIDE SRM] extension on horizontal edge of {ALL_OD SIZING 0.001 μm in horizontal direction} [edge space to ALL_OD ≥ 0.121 μm] in vertical direction	EX1A	≥	0.0410

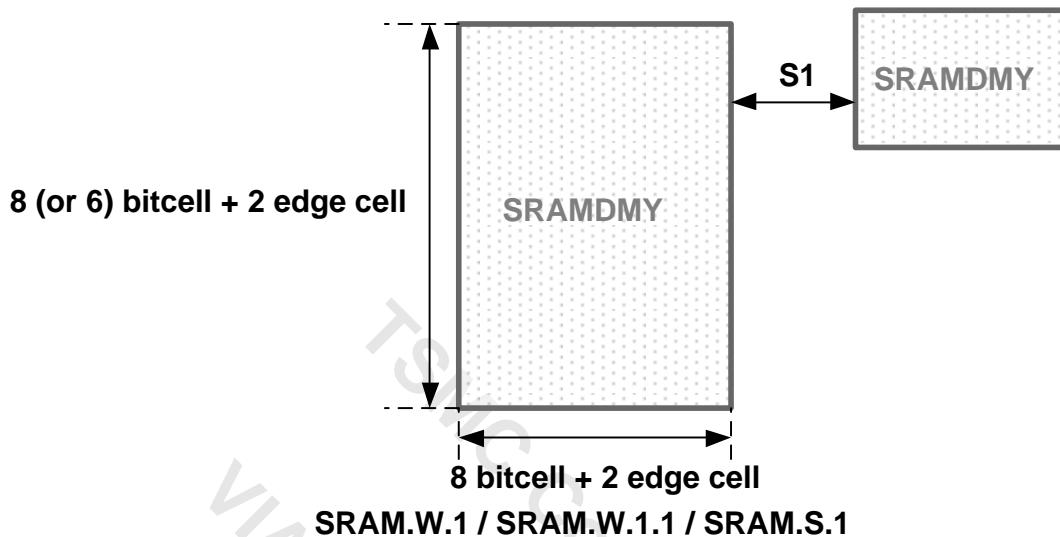
Rule No.	Description	Label	Op.	Rule
SRAM.COD_V.R.1	ALL_COD_V [INSIDE SRM] vertical edge [NOT INTERACT ALL_OD] must fully abut SRM			
SRAM.NW.W.1	Width (Not outside BLK_WF)	W1	\geq	0.1080
SRAM.VT.W.1	Width (Not outside BLK_WF)	W1	\geq	0.1000
SRAM.PP.W.1	Width (Not outside BLK_WF)	W1	\geq	0.1000
SRAM.NP.W.1	Width (Not outside BLK_WF)	W1	\geq	0.1000
SRAM.BPO.W.1	Width of BPO_SRAM in horizontal direction Definition of BPO_SRAM: {BPO SIZING up/down 0.137 μm in horizontal direction} INTERACT {SRM SIZING -0.057 μm in horizontal direction}	W1	=	0.2960
SRAM.BPO.R.5.1	{BPO SIZING up/down 0.023 μm } [width > 0.011 μm] INTERACT {SRM SIZING -0.057 μm horizontal direction} is not allowed			
SRAM.BPO.R.5.2	Number of BPO INTERACT BPO_SRAM > 2 is not allowed Definition of BPO_SRAM follows SRAM.BPO.W.1			
SRAM.BPO.R.5.3	Number of BPO_SRAM INTERACT SRAM > 1 is not allowed Definition of BPO_SRAM follows SRAM.BPO.W.1			
SRAM.CPO.S.1	Space of PO_SRAM2 (17;13) in vertical direction	S1	\geq	0.0960
SRAM.CPO.S.1.1	Space of PO_SRAM3 (17;14) in vertical direction	S1A	\geq	0.0960
SRAM.CPO.R.1	{PO_SRAM2 (17;13) OR PO_SRAM3 (17;14)} and CPO_SRAM (17;12) must be drawn identically			
SRAM.CPO.R.2	PO_SRAM2 (17;13) interact PO_SRAM3 (17;14) is not allowed			
SRAM.MD.S.1	Space of MD (84;0) [INTERACT {CO_SRAM16 (30;16) OR CO_SRAM17 (30;17)}] in horizontal direction	S1	\geq	0.0840
SRAM.MD.S.1.1	Space of MD (84;0) [INTERACT {CO_SRAM16 (30;16) OR CO_SRAM17 (30;17)}] in vertical direction	S1A	\geq	0.0960
SRAM.CMD.W.1	Width of CO_SRAM12 (30;12), CO_SRAM13 (30;13), CO_SRAM15 (30;15) in vertical direction	W1	\geq	0.0360
SRAM.CMD.W.2	Concave corner to concave corner width of CO_SRAM12 (30;12) in vertical direction	W2	\geq	0.0230
SRAM.CMD.W.2.1	Concave corner to concave corner width of CO_SRAM13 (30;13) in vertical direction	W2A	\geq	0.0230
SRAM.CMD.S.1	Space of CO_SRAM12 (30;12) in vertical direction	S1	\geq	0.0540
SRAM.CMD.S.1.1	Space of CO_SRAM13 (30;13) in vertical direction	S1A	\geq	0.0540
SRAM.CMD.S.1.2	Space of CO_SRAM15 (30;15) in vertical direction	S1B	\geq	0.0540
SRAM.CMD.S.3	Space of {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)} to {ALL_MD [width = 0.024 μm] NOT {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}} in horizontal direction	S3	\geq	0.0150
SRAM.CMD.S.4	Space of CO_SRAM12 (30;12)/CO_SRAM13 (30;13)/CO_SRAM15 (30;15) edge [INSIDE ALL_MD] to VC [INSIDE ALL_MD] [PRL > 0 μm] (VC [INSIDE ALL_MD] overlap CO_SRAM12 (30;12)/CO_SRAM13 (30;13)/CO_SRAM15 (30;15) is not allowed)	S4	\geq	0.0020
SRAM.CMD.S.11	Space of {CO_SRAM12 (30;12) to CO_SRAM12 (30;12)} or {CO_SRAM13 (30;13) to CO_SRAM13 (30;13)} or {CO_SRAM15 (30;15) to CO_SRAM15 (30;15)} in horizontal direction	S11	\geq	0.0200
SRAM.CMD.L.1	Length of CO_SRAM12 (30;12), CO_SRAM13 (30;13), CO_SRAM15 (30;15) in horizontal direction	L1	\geq	0.0560
SRAM.CMD.L.11	Horizontal edge length of CO_SRAM12 (30;12) / CO_SRAM13 (30;13) / CO_SRAM15 (30;15) between two consecutive 270-270 degree corners (U-shape)	L11	\geq	0.1710

Rule No.	Description	Label	Op.	Rule
SRAM.CMD.L.12	Vertical edge length of CO_SRAM12 (30;12) / CO_SRAM13 (30;13) / CO_SRAM15 (30;15) between two consecutive 90-270 degree corners	L12	\leq	0.0200
SRAM.CMD.EX.1	$\{\{CO_SRAM12\,(30;12)\,\text{OR}\,CO_SRAM13\,(30;13)\}\,\text{OR}\,CO_SRAM15\,(30;15)\}$ extension on ALL_MD [width = 0.024 μm] in horizontal direction	EX1	\geq	0.0150
SRAM.CMD.EN.11	CO_SRAM41 (30;41) enclosure of CO_SRAM12 (30;12), CO_SRAM15 (30;15) for three side with the other one side = 0/0.005 μm in vertical direction	EN11	=	0
SRAM.CMD.EN.12	CO_SRAM42 (30;42) enclosure of CO_SRAM12 (30;12) for three side with the other one side = 0/0.005 μm in vertical direction	EN12	=	0
SRAM.CMD.O.3	CO_SRAM12 (30;12) / CO_SRAM13 (30;13) / CO_SRAM15 (30;15) overlap of each other in vertical direction [PRL > 0.049 μm]	O3	\geq	0.0080
SRAM.CMD.R.1	$\{\{CO_SRAM12\,(30;12)\,\text{OR}\,CO_SRAM13\,(30;13)\}\,\text{OR}\,CO_SRAM15\,(30;15)\}$ outside {SRM (50;0) AND $\{\{\{\{\{SRM_11\,\text{OR}\,SRM_12\}\,\text{OR}\,SRM_14\}\,\text{OR}\,SRM_15\}\,\text{OR}\,SRM_17\}\,\text{OR}\,SRM_20\}\,\text{OR}\,SRM_21\}\,\text{OR}\,SRM_23\}$ } is not allowed			
SRAM.CMD.R.6	SRM (50;0) must interact CO_SRAM15 (30;15)			
SRAM.CMD.R.7	Horizontal edge of CO_SRAM11 (30;11) [INSIDE CO_SRAM18 (30;18)] must fully abut either CO_SRAM12 (30;12), CO_SRAM13 (30;13), CO_SRAM15 (30;15)			
SRAM.CMD.R.8	CO_SRAM12 (30;12), CO_SRAM13 (30;13), CO_SRAM15 (30;15) must be a rectangle orthogonal to grid			
SRAM.CMD.R.11	CO_SRAM29 (30;29) must be drawn identically to CO_SRAM13 (30;13)			
SRAM.CMD.R.12	CO_SRAM41 (30;41) must interact CO_SRAM12 (30;12) or CO_SRAM15 (30;15)			
SRAM.CMD.R.13	CO_SRAM42 (30;42) must interact CO_SRAM12 (30;12)			
SRAM.CMD.R.14	CO_SRAM33 (30;33) must be drawn identically to CO_SRAM12 (30;12) or CO_SRAM13 (30;13) or CO_SRAM15 (30;15) or $\{\{CO_SRAM12\,(30;12)\,\text{OR}\,CO_SRAM13\,(30;13)\}\,\text{OR}\,CO_SRAM15\,(30;15)\}$			
SRAM.CMD.R.17	CO_SRAM29 (30;29), CO_SRAM33 (30;33), CO_SRAM41 (30;41), CO_SRAM42 (30;42) overlap each other is not allowed			
SRAM.MP.S.1	Space of MP [INSIDE SRM] to {MD NOT $\{\{CO_SRAM12\,(30;12)\}\,\text{OR}\,CO_SRAM13\,(30;13)\}\,\text{OR}\,CO_SRAM15\,(30;15)\}$ } [INTERACT OD] (Except following conditions: 1. MP and MD interact same M0)	S1	\geq	0.0160
SRAM.MP.S.2	Space of MP_A (84;285)	S2	\geq	0.0760
SRAM.MP.S.3	Space of MP_B (84;286)	S3	\geq	0.0760
SRAM.MP.R.1	{MP_A (84;285) OR MP_B (84;286)} and MP [INSIDE SRM] must be drawn identically			
SRAM.MP.R.2	MP_A (84;285) interact MP_B (84;286) is not allowed			
SRAM.VC.S.31.1	Space of VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.0105 μm , INSIDE SRM]	S31A T	\geq	0.0370
SRAM.VC.S.31.4	Space of VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.0105 μm , INSIDE SRM]	S31D T	\geq	0.0370
SRAM.VC.S.32.1	Space of VC [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VC [edge length = 0.016/0.016 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.0105 μm , INSIDE SRM]	S32A T	\geq	0.0370

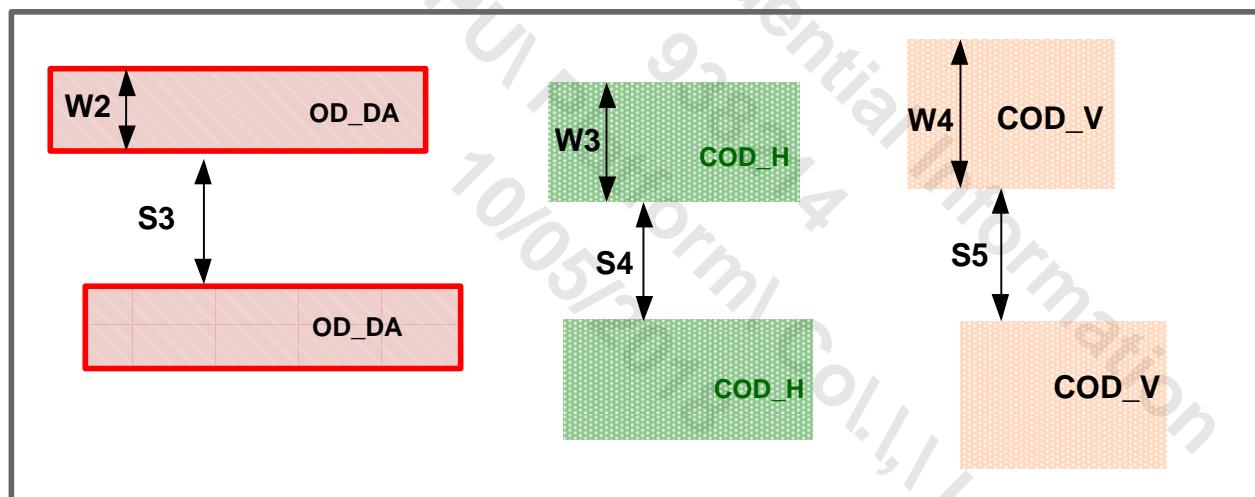
Rule No.	Description	Label	Op.	Rule
SRAM.VC.S.32.4	Space of VC [edge length = 0.020/0.020 μm in horizontal/vertical direction] to VC [edge length = 0.020/0.020 μm in horizontal/vertical direction] in horizontal direction [PRL > -0.0105 μm , INSIDE SRM]	S32D T	\geq	0.0370
SRAM.VC.R.3	Rectangular VC [width/length = 0.020/0.040 μm , INSIDE SRM] must be inside {{MD [width = 0.024 μm] NOT {{CO_SRAM12 (30;12) OR CO_SRAM13 (30;13)} OR CO_SRAM15 (30;15)}}}			
SRAM.VC.R.4	Rectangular VC [width/length = 0.020/0.040 μm] must be vertical direction [INSIDE SRM]			
SRAM.VC.R.9.1	Square VC should be fully covered by {{MP AND M0_NOT_CM0} OR {{MD NOT ALL_CMD} AND M0_NOT_CM0}} [INSIDE SRAMDMY]			
SRAM.CM0B.R.1	{CM0B [INTERACT SRM_22] SIZING up/down 0.045 μm in vertical direction} interact CM0B_2 (180;112) number > 1 is not allowed			
SRAM.CM0B.R.2	CM0B_2 (180;112) must be drawn identically to CM0B (180;110) [INSIDE SRAMDMY]			
SRAM.VIA0.S.31.1	Space of VIA0 in horizontal direction [different net, PRL > -0.020 μm] [INSIDE SRAMDMY]	S31	\geq	0.0370
SRAM.VIA0.R.1	VIA0 [INTERACT BLK_WB] must be inside BLK_M1			
SRAM.M1.W.1	Concave corner to concave corner width of M1 in MINP direction [-0.060 μm < PRL \leq 0 μm]	W1	\geq	0.0240
SRAM.M1.W.1.1	Concave corner to concave corner width of M1 in NMINP direction [-0.024 μm < PRL \leq 0 μm]	W1A	\geq	0.0600
SRAM.M1.S.2	Space of M1 to M1 edge [length \leq 0.060 μm , between two consecutive 90-270 degree corners] [PRL > 0 μm]	S2	\geq	0.0400
SRAM.M1.S.32.1	Space of BLK_M1 to BLK_M1 [0.0245 μm \leq width < 0.028 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	S32A	\geq	0.0240
SRAM.M1.S.32.2	Space of BLK_M1 to BLK_M1 [width \geq 0.028 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.035 μm]	S32B	\geq	0.0260
SRAM.M1.S.33.1	Space of BLK_M1 [width \geq 0.040 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.035 μm]	S33A	\geq	0.0280
SRAM.M1.L.2.2	Edge length with adjacent edge [length \leq 0.060 μm , between two consecutive 90-270 degree corners]	L2B	\geq	0.0900
SRAM.M1.L.3	Edge length [between two consecutive 90-270 degree corners, ABUT SRAMDMY]	L3	\leq	0.0050
SRAM.M1.L.3.1	Edge length [between two consecutive 90-270 degree corners, NOT ABUT SRAMDMY]	L3A	=	0.0240, 0.0480, \geq 0.0900
SRAM.M1.L.4	Edge length [between two consecutive 270-270 degree corners]	L3	\geq	0.1500
SRAM.M1.R.2	M1 edge [length \leq 0.060 μm , between two consecutive 90-270 degree corners] must be MINP direction			
SRAM.M1.R.2.1	M1 edge [between two consecutive 270-270 degree corners] must be NMINP direction (Except SEALRING_ALL)			
SRAM.M1.R.2.2	M1 edge [between two consecutive 90-270 degree corners] abut SRAMDMY from outside is not allowed			
SRAM.M1.R.2.3	M1 horizontal edge inside Checked_Region is not allowed Definition of Checked_Region: {{{{SRAMDMY SIZING 0.090 μm in M1 NMINP direction}} NOT {{{SRAMDMY SIZING 0.0005 μm in M1 NMINP direction}}} OR {{{SRAMDMY SIZING -0.0005 μm in M1 NMINP direction}} NOT {{{SRAMDMY SIZING -0.090 μm in M1 NMINP direction}}}}			
SRAM.M1.R.2.4	M1 overlap Checked_Region_H is not allowed Definition of Checked_Region_H: {{{SRAMDMY SIZING 0.108 μm in M1 MINP direction}} NOT SRAMDMY} SIZING 0.001 μm in M1 NMINP direction}			

Rule No.	Description	Label	Op.	Rule
SRAM.M1.R.3	M1 overlap Concave_Area is not allowed (Except SEALRING_ALL) Definition of Concave_Area: A rectangle [0.060 μm x 0.060 μm] abut both edge of M1 concave corner [NOT INTERACT M1 edge length ≤ 0.060 μm]			
SRAM.VIA1.R.1	VIA1 [INTERACT BLK_WB] must be inside BLK_M1			
SRAM.M2.W.1.1	Width of M2 [INTERACT BLK_M2, MINP direction]	W1A	=	0.0240, 0.0280, 0.0400, 0.0500, 0.0800, ≥ 0.1800
SRAM.VIA2.S.2.1.1	Space of the long side of rectangular VIA2 to square VIA2 [PRL > -0.105 μm, INTERACT SRAMDMY]	S2A1	≥	0.0600
SRAM.VIA2.EN.1.1	Short side enclosure of rectangular VIA2 [INTERACT SRAMDMY] by M2 with the other two long sides ≥ 0 μm	EN1A	≥	0.0250
SRAM.M3.W.1.1	Width of M3 [INTERACT BLK_M3, MINP direction]	W1A	=	0.0240, 0.0400, 0.0600, 0.0800, ≥ 0.1800
SRAM.M3.W.1.2	Width of M3 [INTERACT BLK_M3, NMINP direction]	W1B	=	0.0800, 0.1100, ≥ 0.1800
SRAM.M3.S.2	Space to M3 [0.020 μm ≤ width ≤ 0.024 μm] in MINP direction [PRL > -0.080 μm, INTERACT SRAMDMY]	SM	=	0.0200 ~ 0.0250, ≥ 0.0280
SRAM.M3.S.2.1	Space to M3 [0.040 μm ≤ width ≤ 0.080 μm] in MINP direction [PRL > -0.040 μm, INTERACT SRAMDMY]	SM	=	0.0250, ≥ 0.0340
SRAM.M3.S.3.2	Space to M3 [width = 0.080 μm] in NMINP direction [PRL > -0.060 μm, INTERACT SRAMDMY]	SN	≥	0.0400
SRAM.M3.S.3.3	Space to M3 [0.100 μm ≤ width ≤ 0.120 μm] in NMINP direction [PRL > -0.060 μm, INTERACT SRAMDMY]	SN	≥	0.0400
SRAM.M3.EN.1	Enclosure of square VIA2 [INTERACT SRAMDMY] by M3 for two opposite sides with the other two sides ≥ 0 μm	EN1	≥	0.0250
SRAM.M3.EN.1.1	Long side enclosure of rectangular VIA2 [INTERACT SRAMDMY] by M3 with other two short sides ≥ 0 μm	EN1A	≥	0.0250
SRAM.M3.EN.31.7	Enclosure of square Lower_VIA [width = 0.020 μm, INTERACT SRAMDMY] by M3 [0.080 μm ≤ width < 0.260 μm] for two opposite sides with the other two sides ≥ 0.030 μm	EN31 G	≥	0.0100
SRAM.M3.CS.1.1.3	Space of M3 [width = 0.024 μm] to M3 [width < 0.040 μm, or width > 0.060 μm] in MINP direction [same color, PRL > -0.124 μm, INTERACT SRAMDMY] DRC checks same color space of M3CA and M3CB	SM	=	0.0600, 0.0620, 0.0640, 0.0900, 0.1100, 0.1260, ≥ 0.1400
SRAM.M3.CS.1.1.4	Space to M3 [width = 0.040 μm] in MINP direction [same color, PRL > -0.060 μm, INTERACT SRAMDMY]	SM	=	0.0740, 0.0900, 0.0940, 0.1000, 0.1100, 0.1120, 0.1190, ≥ 0.1200
SRAM.M4.W.1.3	Width [NMINP direction, INTERACT BLK_M4]	W1C	=	0.0580
SRAM.M4.S.5.5	Space of M4 edge [edge length > 0.080 μm in MINP direction] in NMINP direction [PRL > -0.076 μm] [at least one Mya width = 0.058 μm [INTERACT BLK_M4] in NMINP direction]	SN	=	0.0560, 0.0700, ≥ 0.1140
SRAM.M4.S.16.3	Space to M4 [INTERACT BLK_M4] line-end [edge length = 0.058 μm between 2 consecutive 90-90 degree corners, PRL > -0.076 μm] in MINP direction	S16C	≥	0.1000

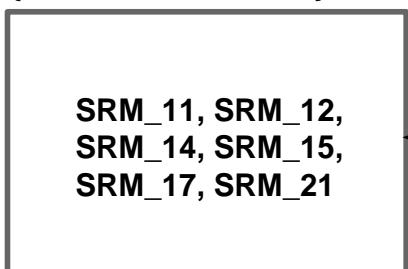
SRAM



{SRM OR SRAM.DMY}



{SRM OR SRAM.DMY}



{SRM OR SRAM.DMY}

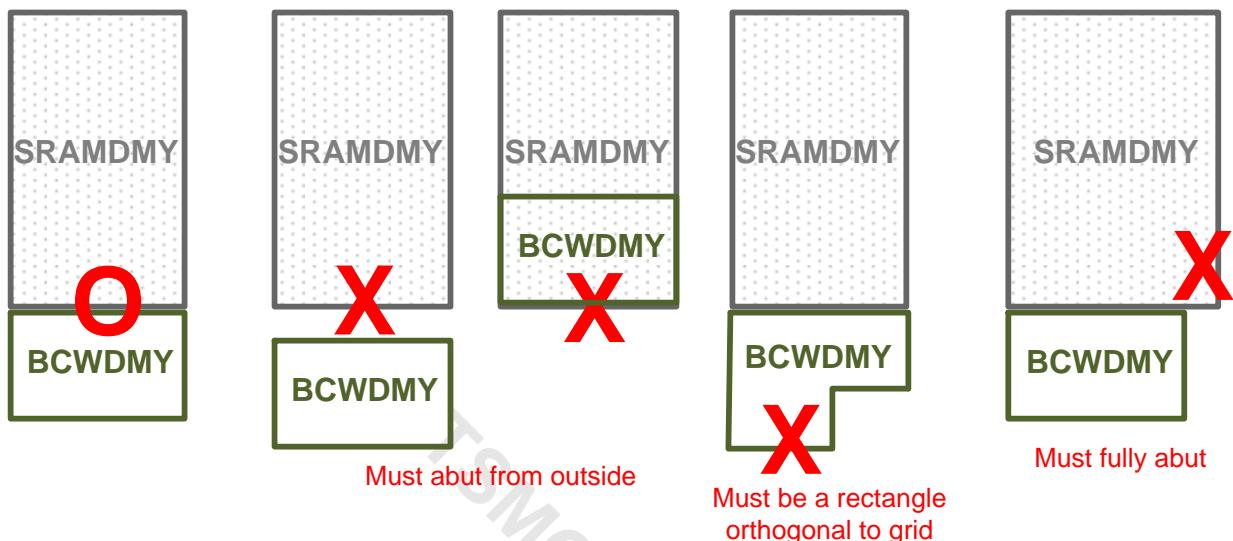
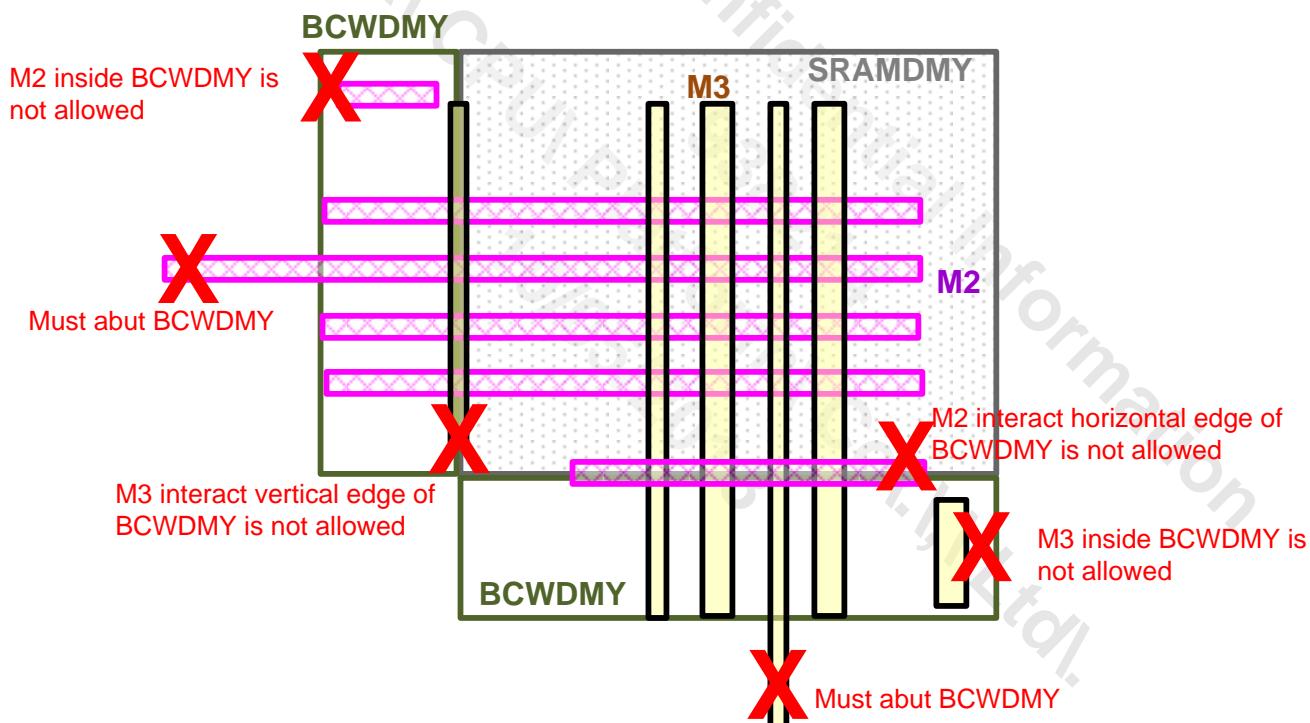
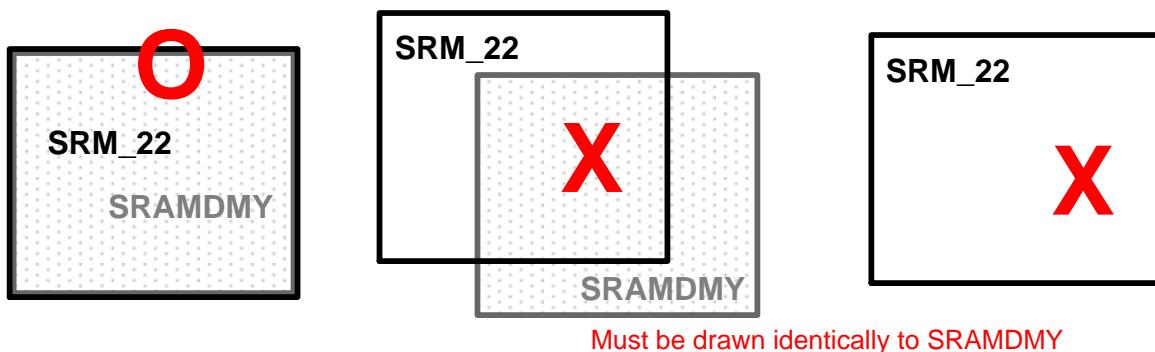
SRM_11, SRM_12,
SRM_14, SRM_15,
SRM_17, SRM_21

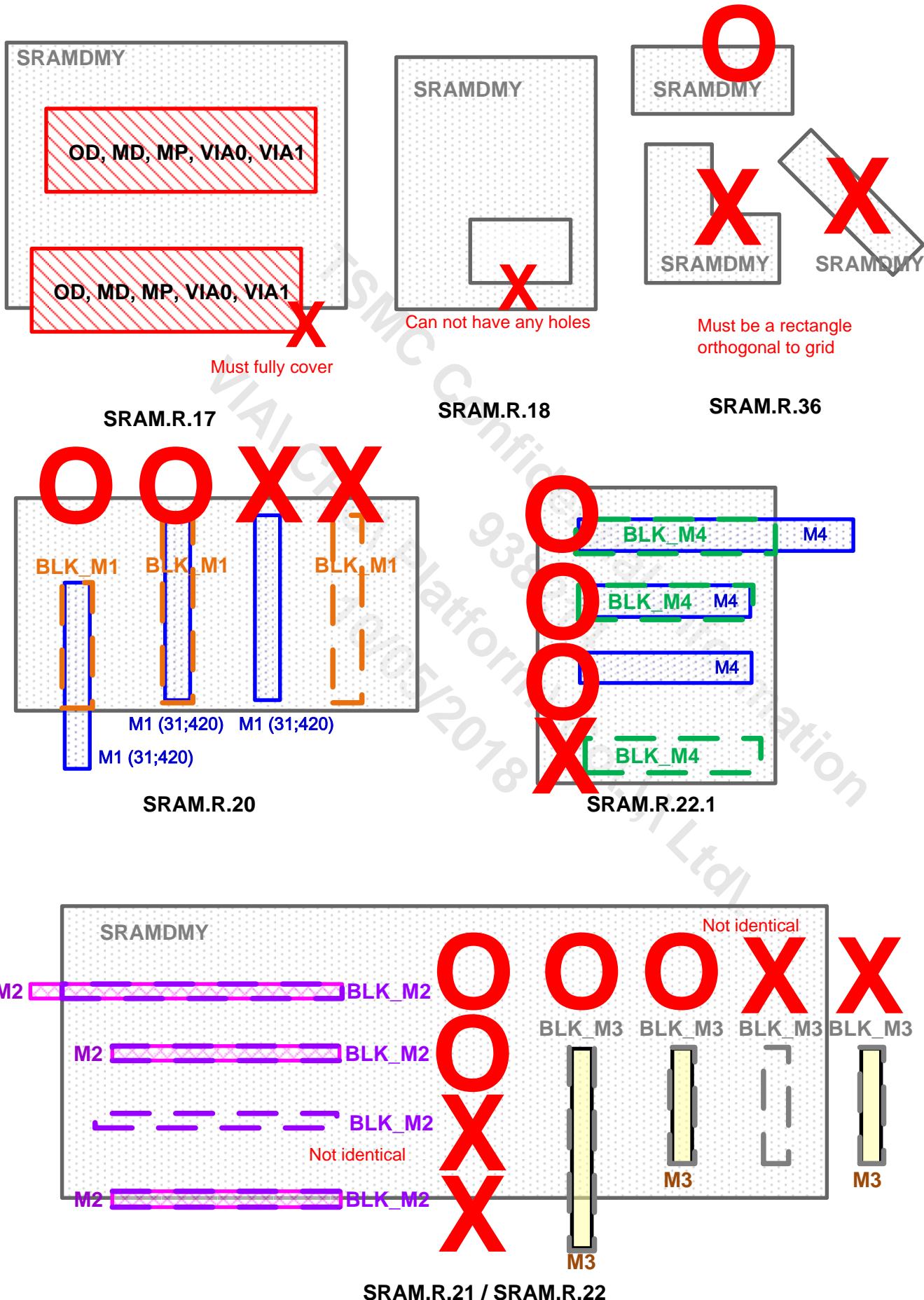
Overlap is not allowed

{SRM OR SRAM.DMY}

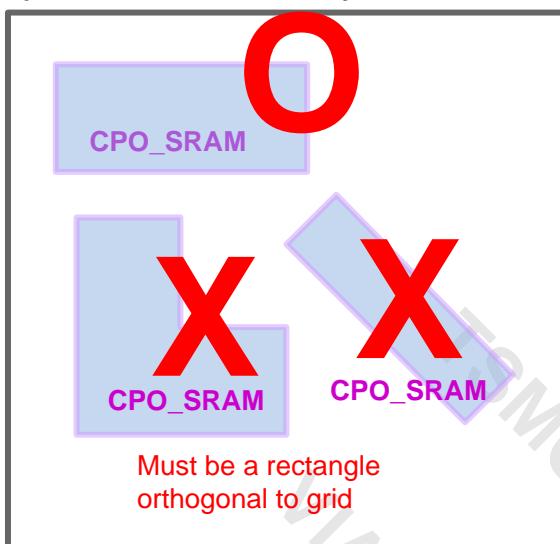
SRM_11, SRM_12,
SRM_14, SRM_15,
SRM_17, SRM_21

SRAM.S.9

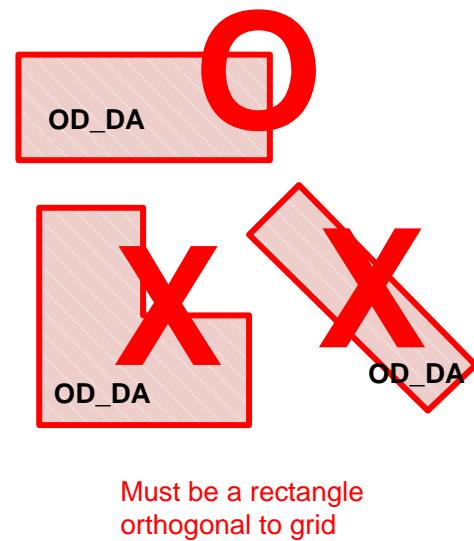
**SRAM.R.2 / SRAM.R.2.2 / SRAM.R.2.3****SRAM.R.2.4 / SRAM.R.2.5 / SRAM.R.2.6 / SRAM.R.2.7 / SRAM.R.2.8****SRAM.R.3**



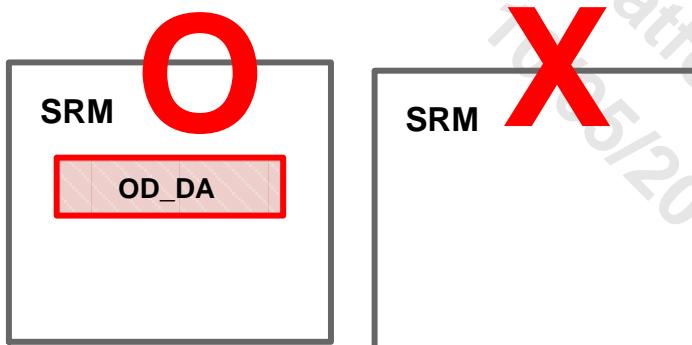
{SRM OR SRAMDMY}



SRAM.R.36.1

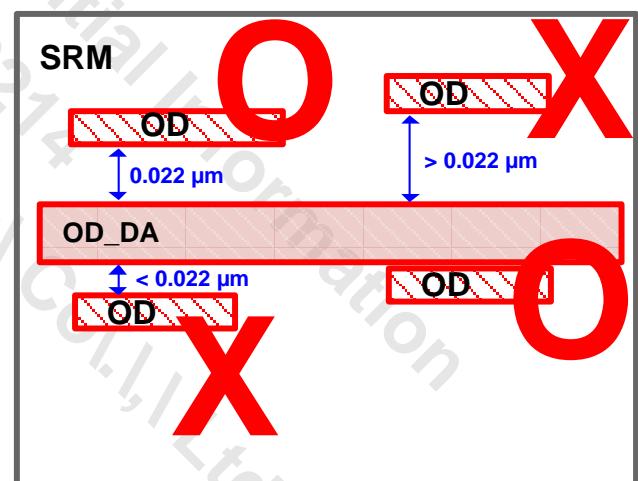


SRAM.OD.R.1

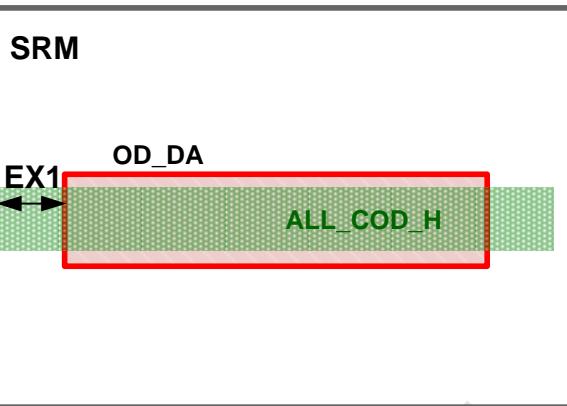


Must interact OD_DA

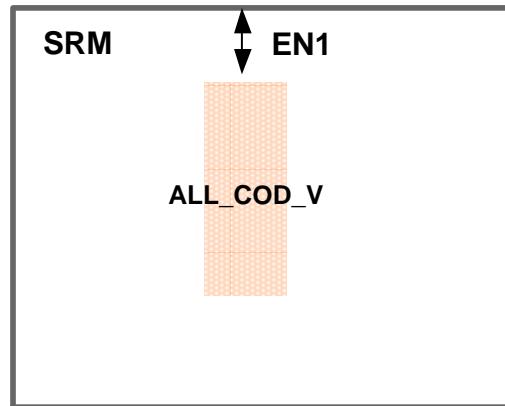
SRAM.OD.R.2



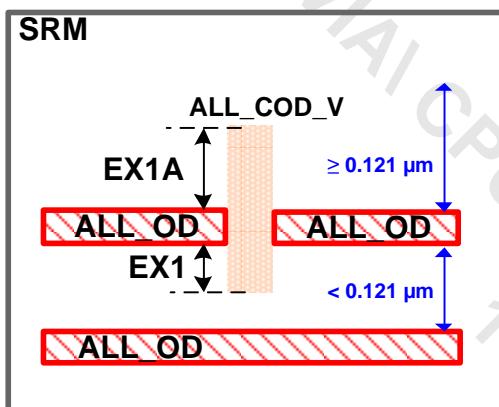
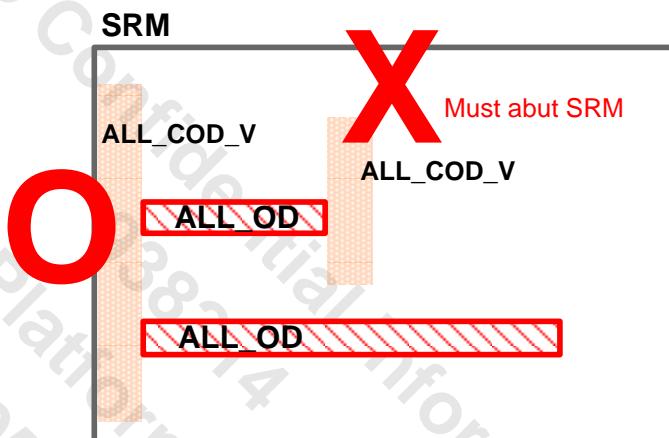
SRAM.OD.R.3



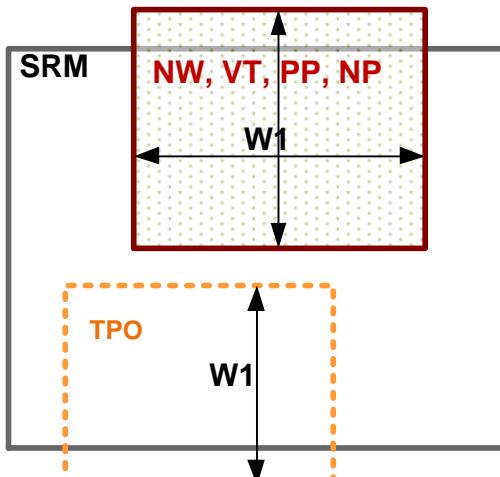
SRAM.COD_H.EX.1

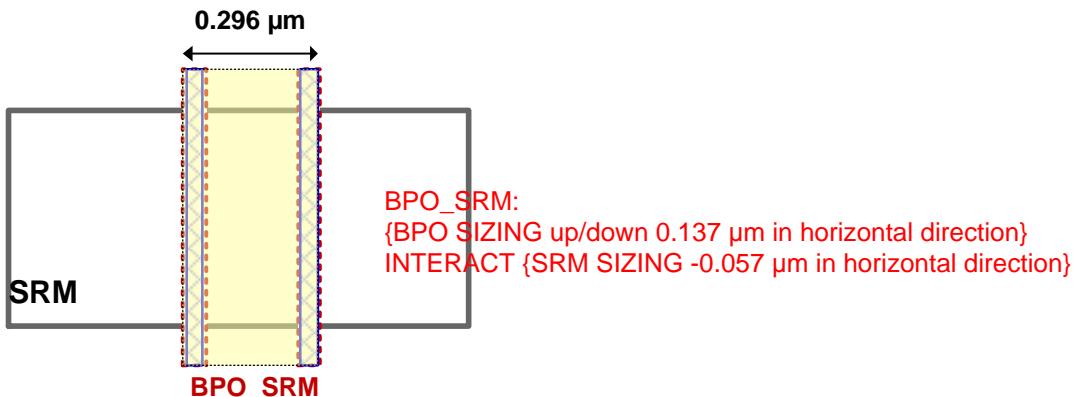
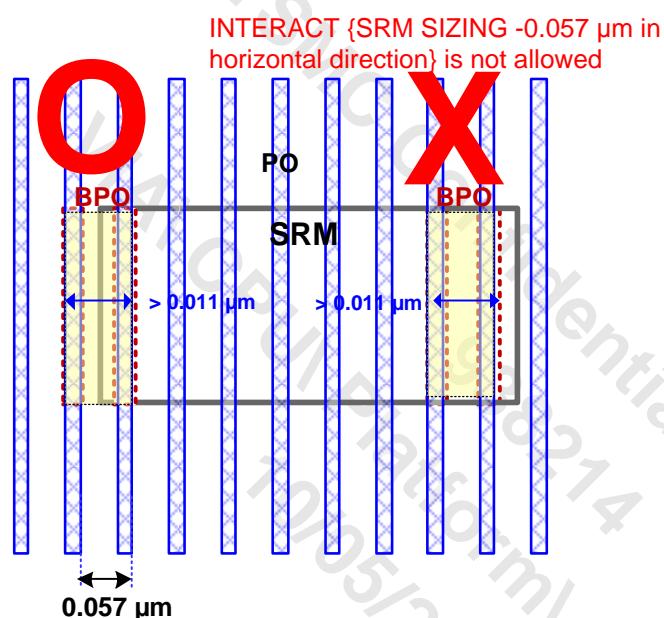
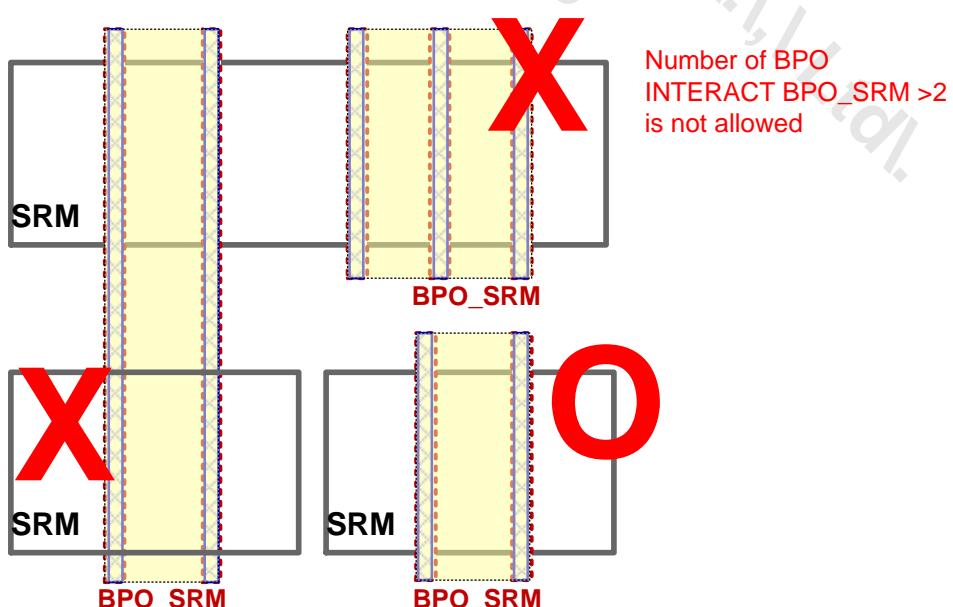


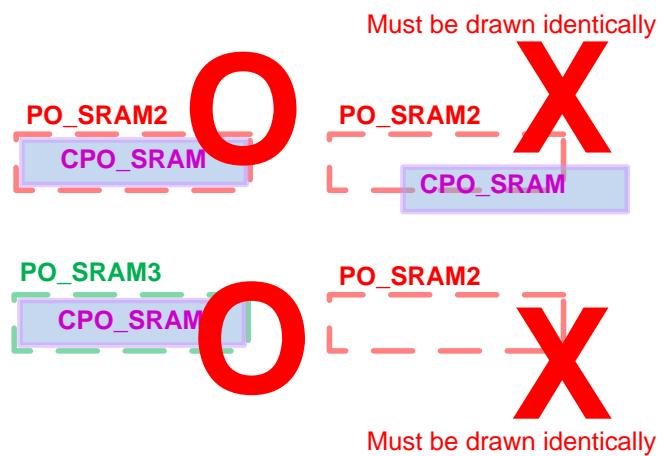
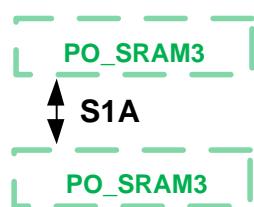
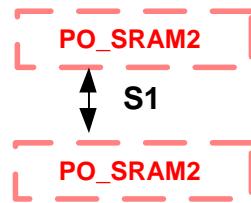
SRAM.COD_V.EN.1

SRAM.COD_V.EX.1 /
SRAM.COD_V.EX.1.1

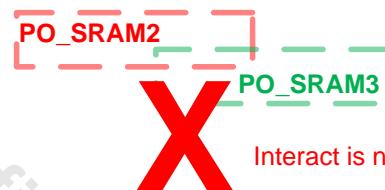
SRAM.COD_V.R.1

SRAM.NW.W.1 /
SRAM.VT.W.1 /
SRAM.PP.W.1 /
SRAM.NP.W.1 /
SRAM.TPO.W.1

**SRAM.BPO.W.1****SRAM.BPO.R.5.1****SRAM.BPO.R.5.2 / SRAM.BPO.R.5.3**

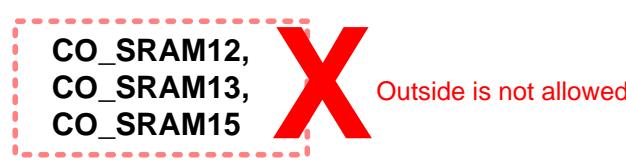
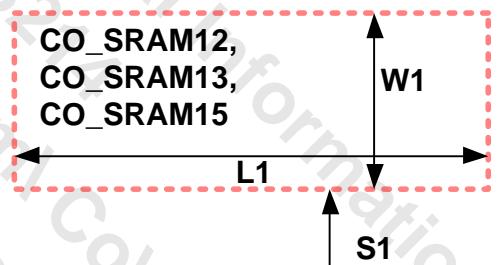
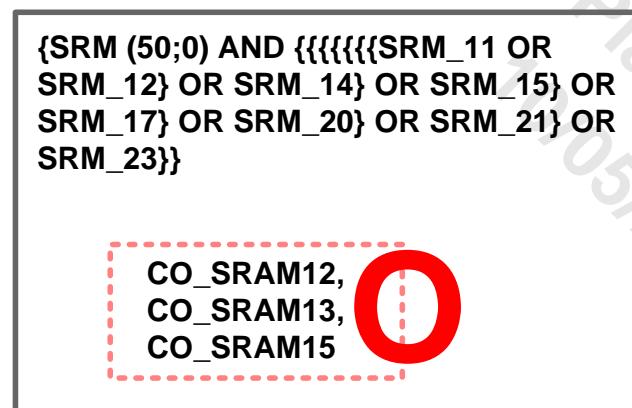


SRAM.CPO.S.1 / SRAM.CPO.S.1.1

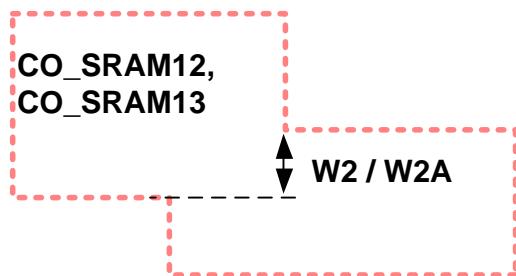


Interact is not allowed

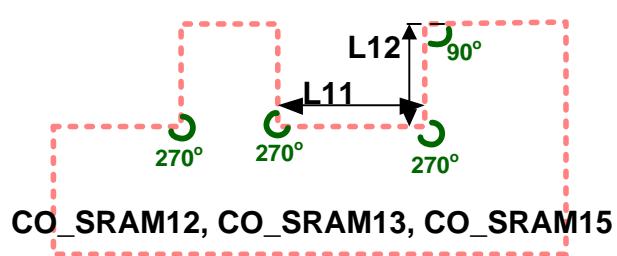
SRAM.CPO.R.1 / SRAM.CPO.R.2



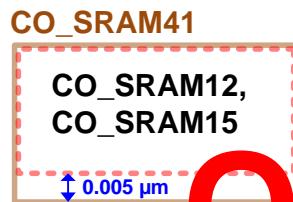
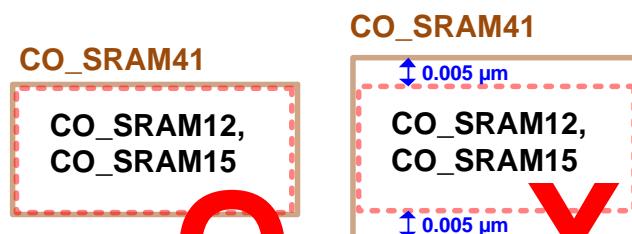
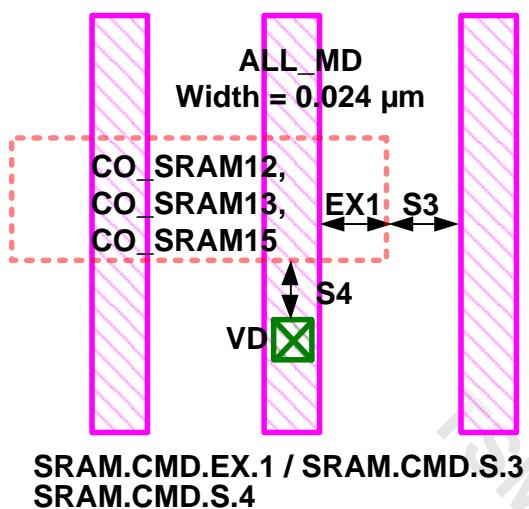
SRAM.CMD.R.1



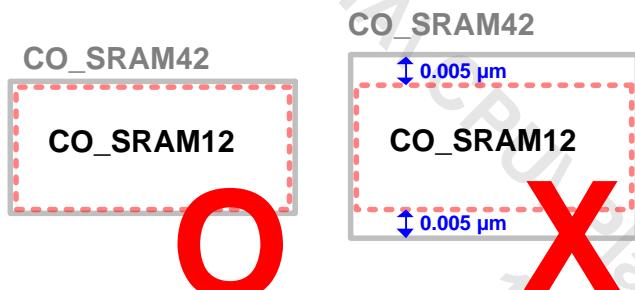
SRAM.CMD.W.2 / SRAM.CMD.W.2.1



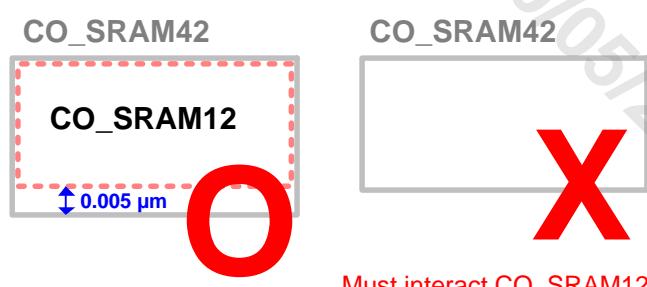
SRAM.CMD.L.11 / SRAM.CMD.L.12



Must interact CO_SRAM12,
CO_SRAM15

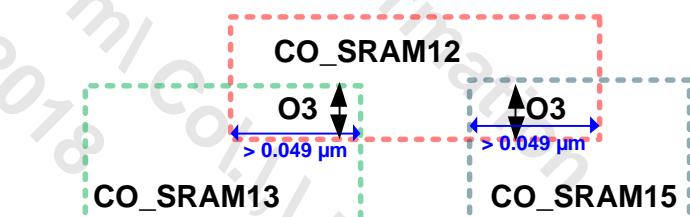


SRAM.CMD.EN.11 / SRAM.CMD.R.12

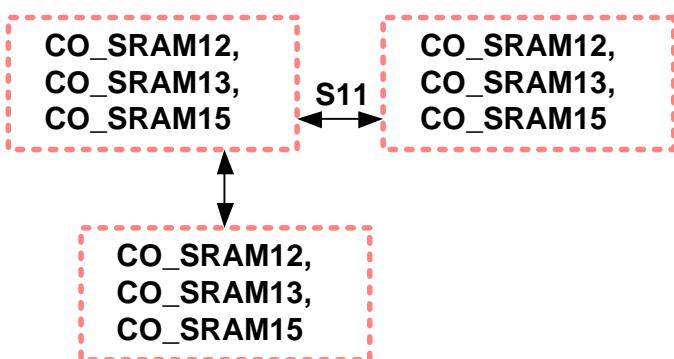


Must interact CO_SRAM12

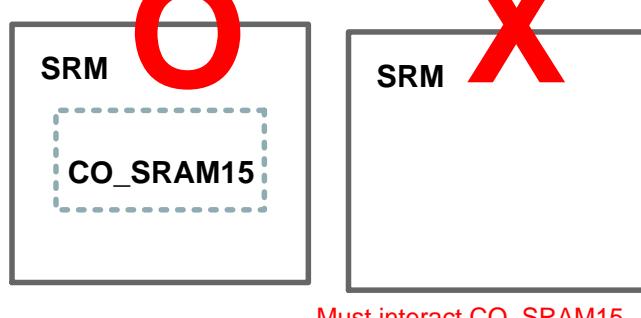
SRAM.CMD.EN.12 / SRAM.CMD.R.13



SRAM.CMD.O.3

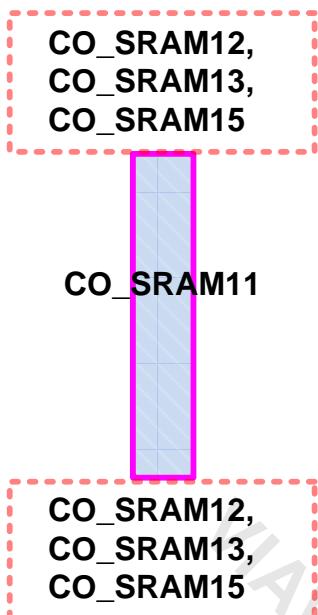


SRAM.CMD.EN.12 / SRAM.CMD.S.11

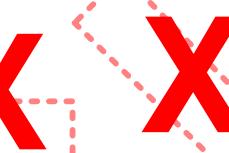


Must interact CO_SRAM15

SRAM.CMD.R.6

CO_SRAM18**SRAM.CMD.R.7**

CO_SRAM12,
CO_SRAM13,
CO_SRAM15



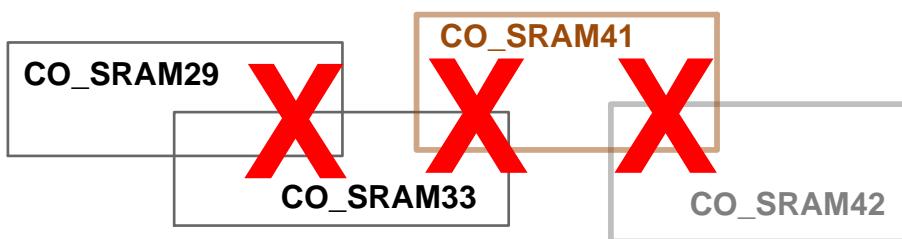
CO_SRAM12,
CO_SRAM13,
CO_SRAM15

Must be a rectangle
orthogonal to grid

SRAM.CMD.R.8**CO_SRAM29**

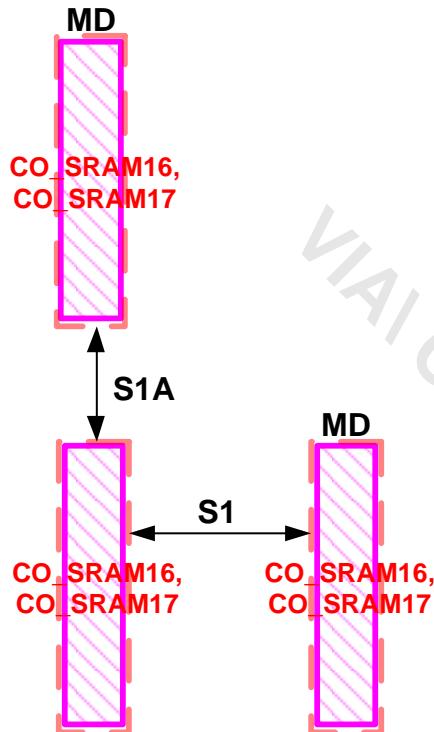
Must be drawn identically

**SRAM.CMD.R.11****CO_SRAM33****CO_SRAM33****CO_SRAM33****CO_SRAM33****SRAM.CMD.R.14**

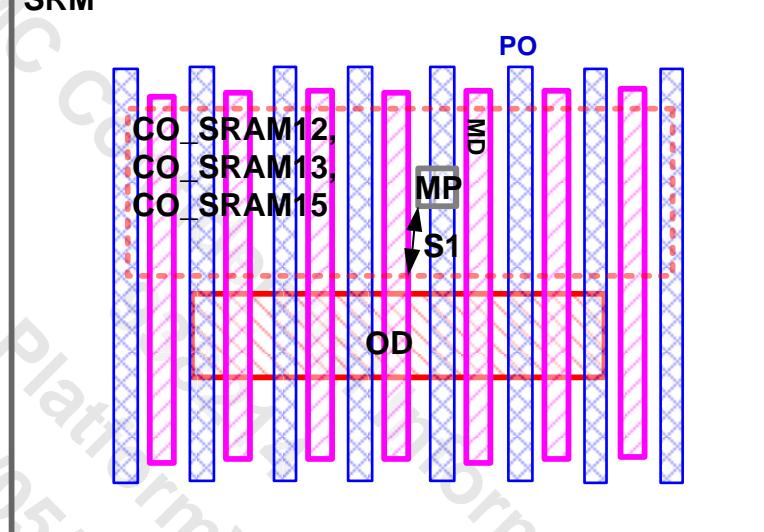


Overlap each other is not allowed

SRAM.CMD.R.17

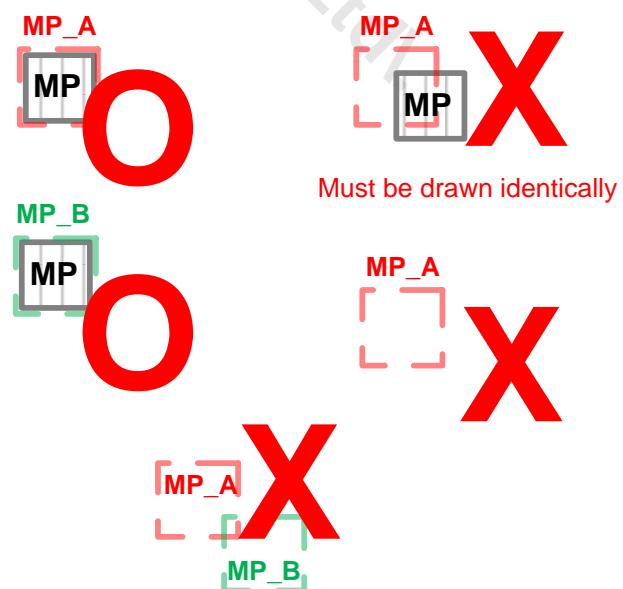
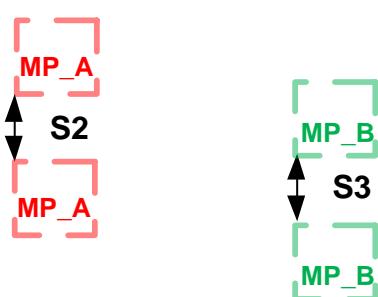


SRM



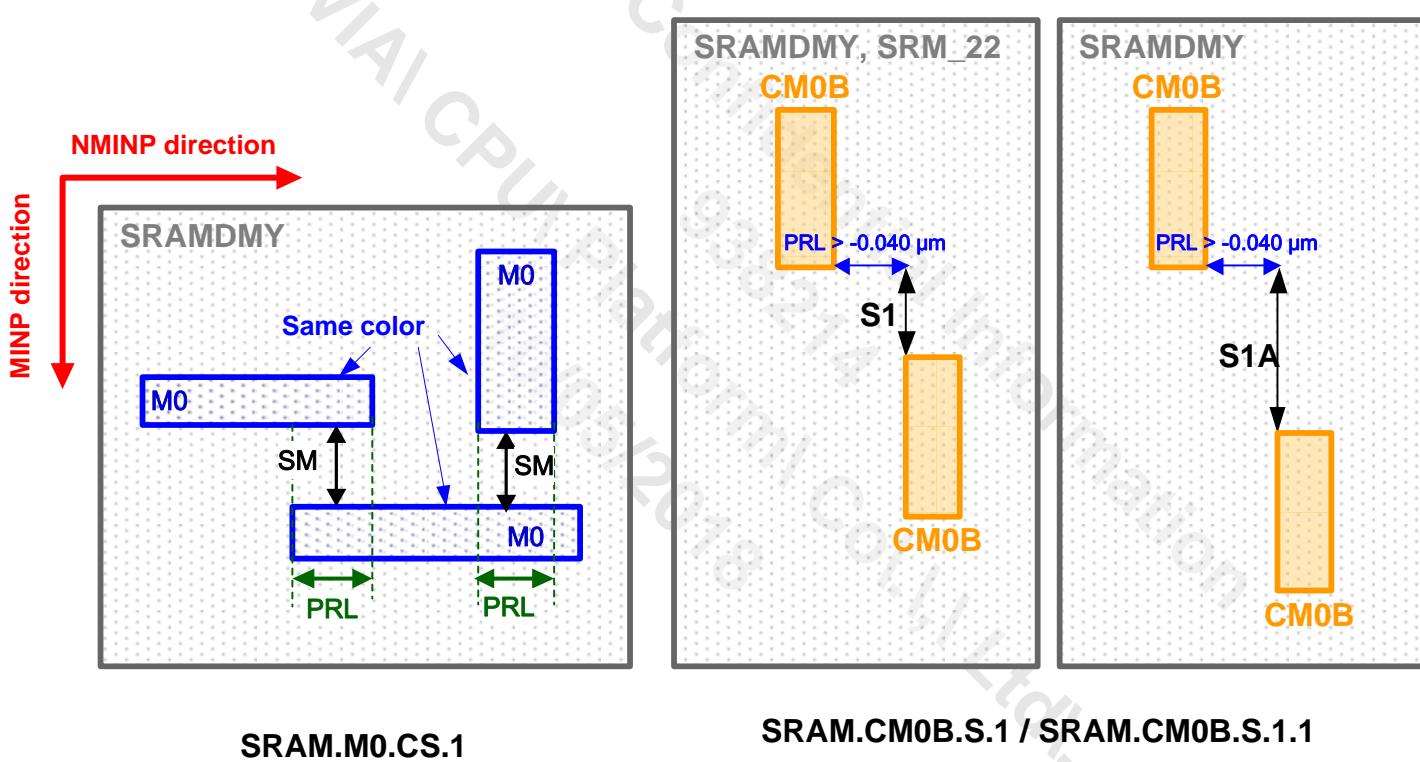
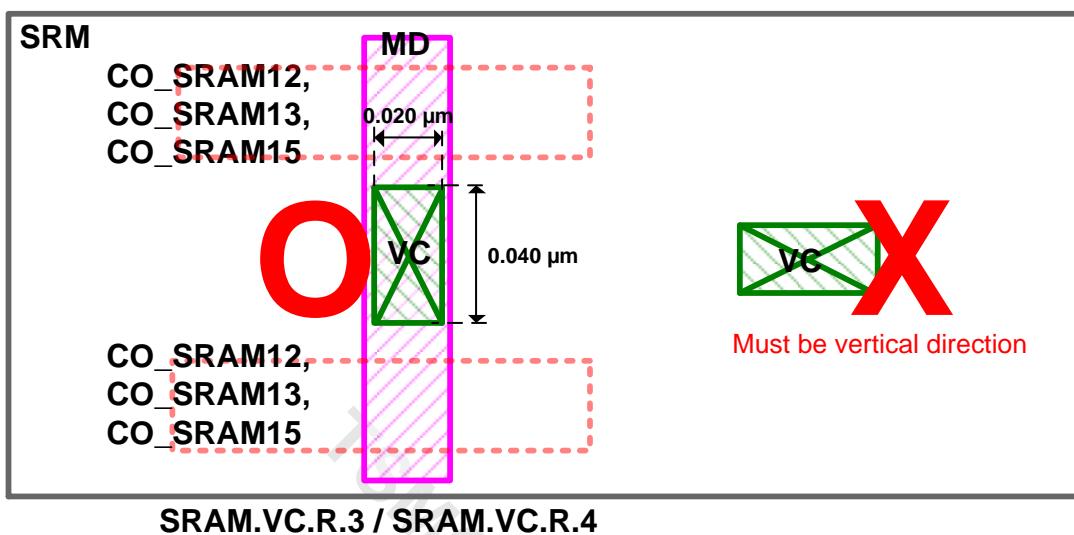
SRAM.MP.S.1

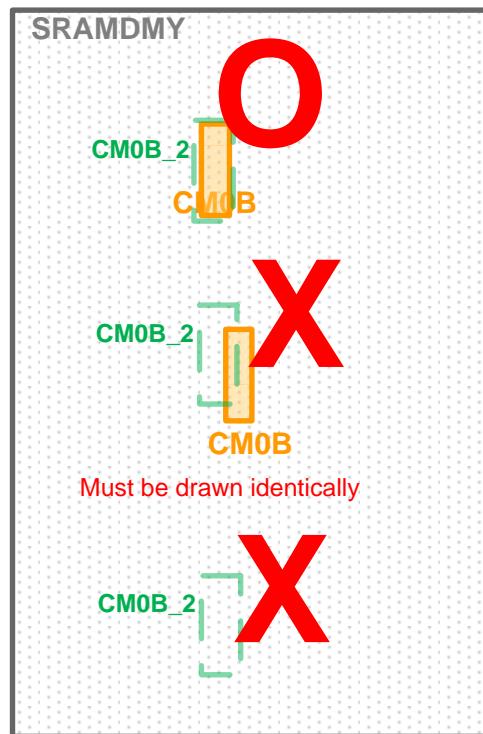
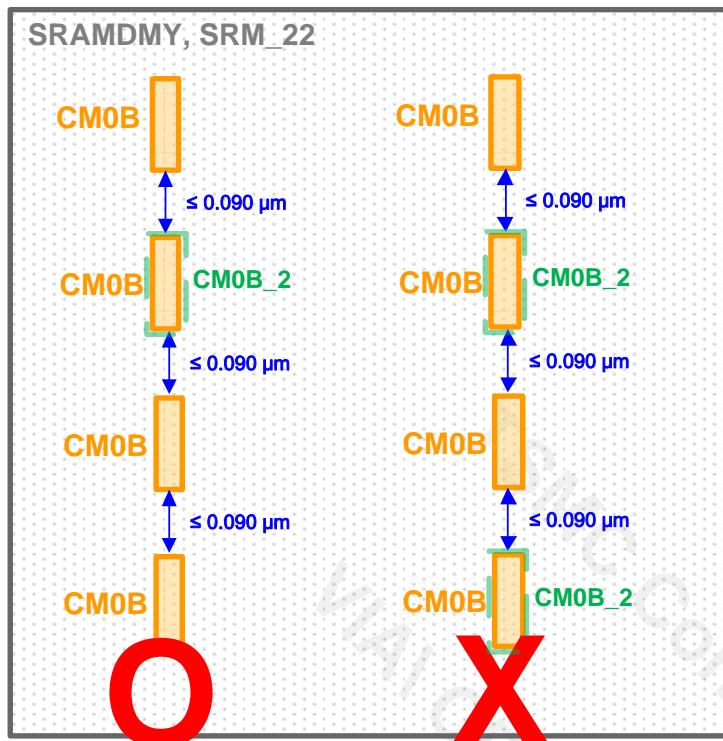
SRAM.MD.S.1 / SRAM.MD.S.1.1



SRAM.MP.S.2 / SRAM.MP.S.3

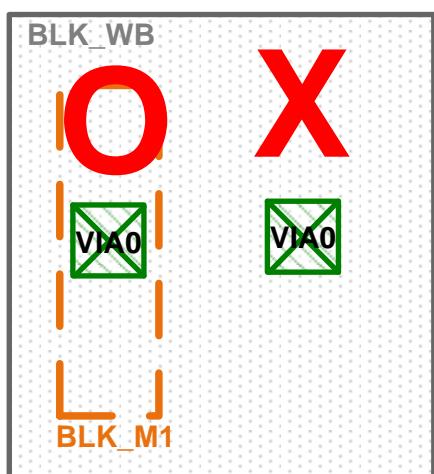
SRAM.MP.R.1 / SRAM.MP.R.2



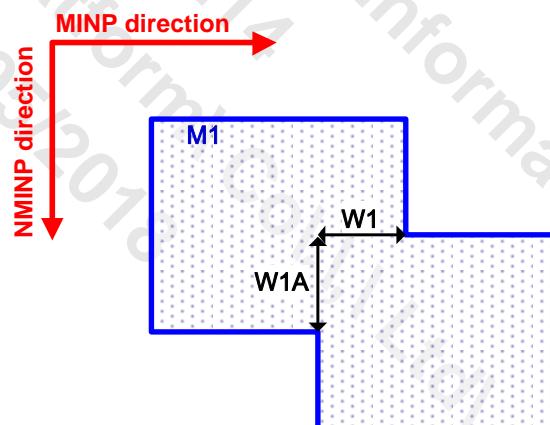


Interact CM0B_2 number > 1
is not allowed

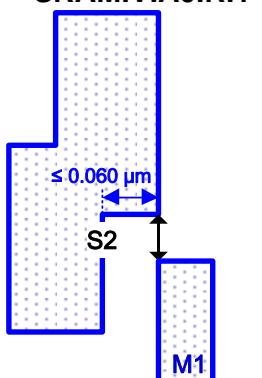
SRAM.CM0B.R.1



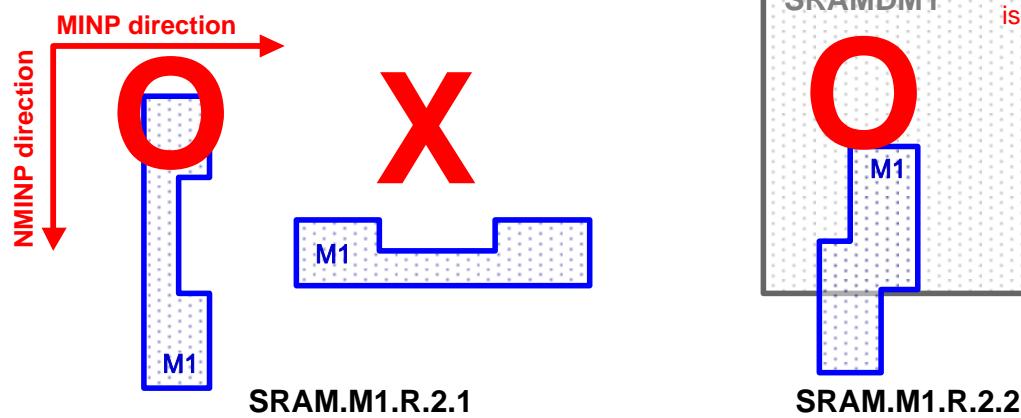
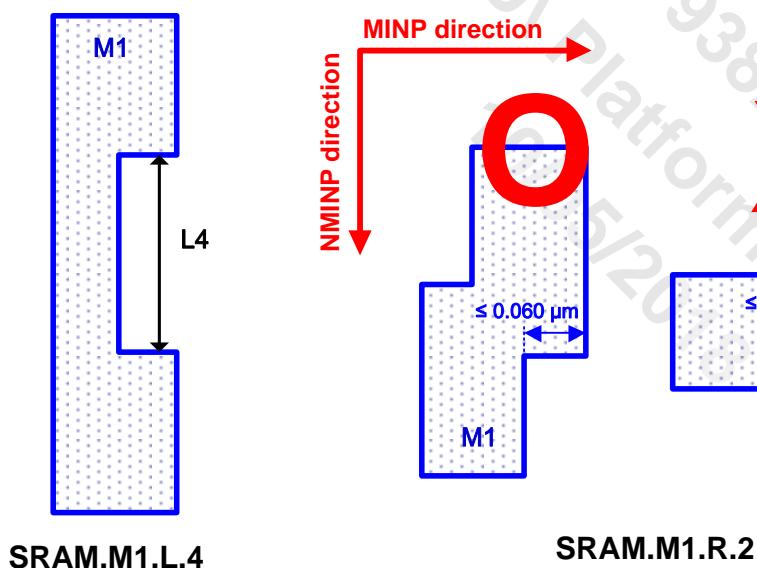
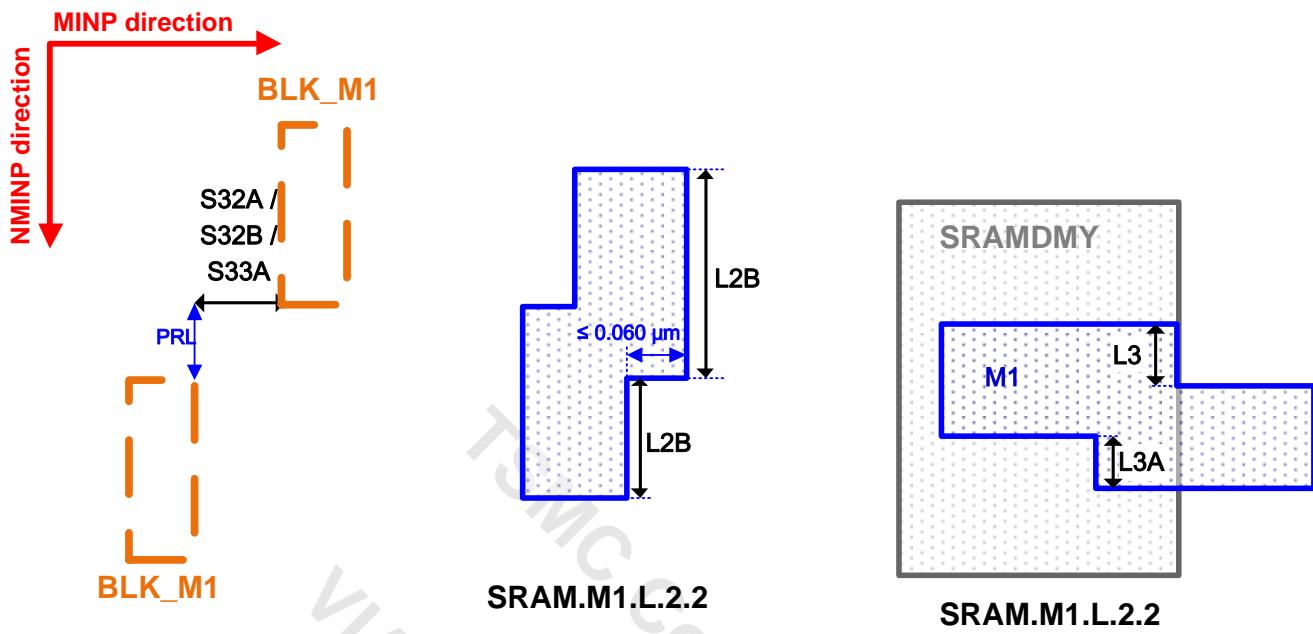
SRAM.CM0B.R.2

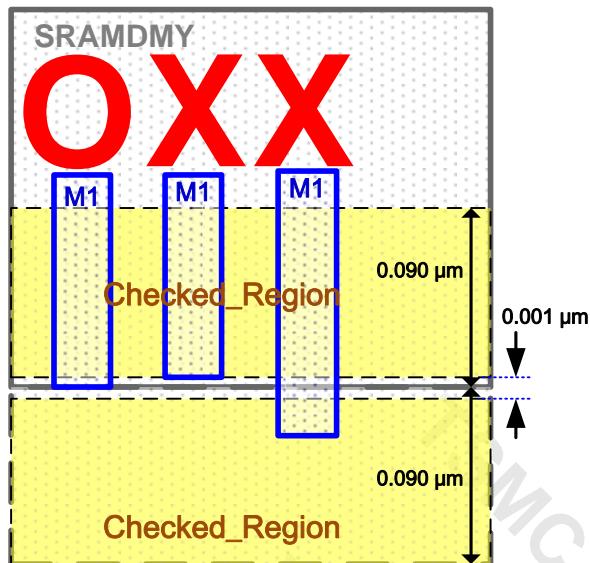


SRAM.VIA0.R.1

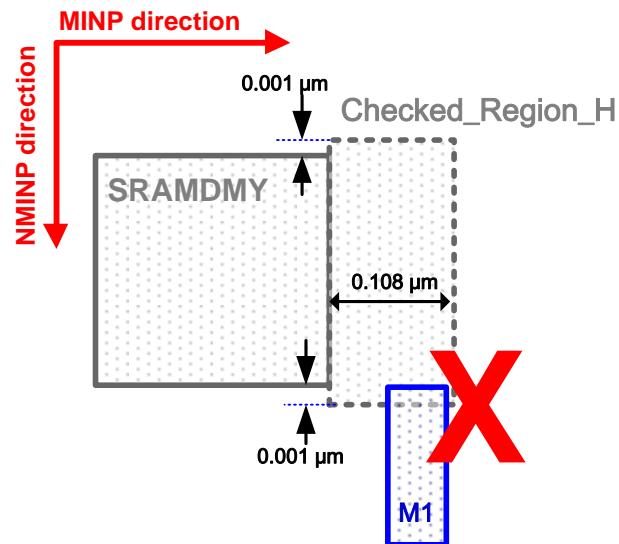


SRAM.M1.W.1 / SRAM.M1.W.1.1

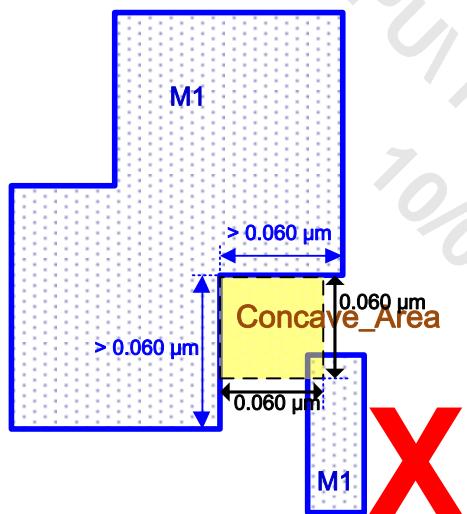




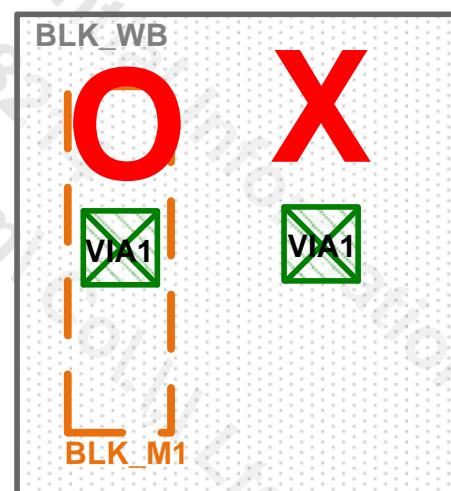
SRAM.M1.R.2.3



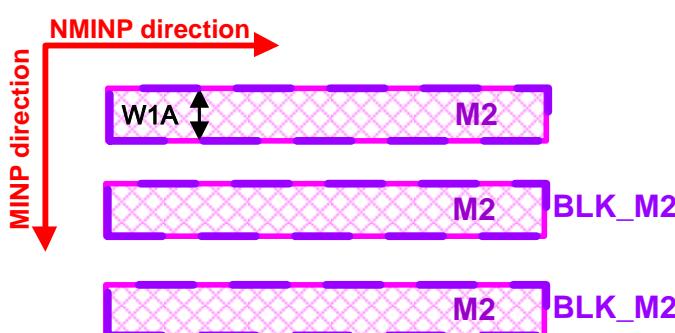
SRAM.M1.R.2.4



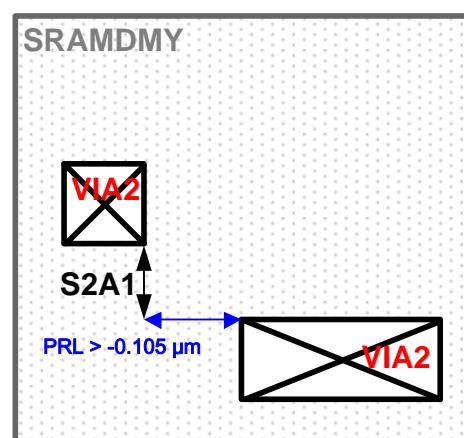
SRAM.M1.R.3



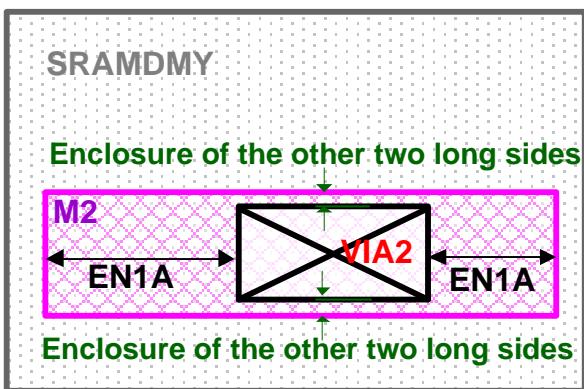
SRAM.VIA1.R.1



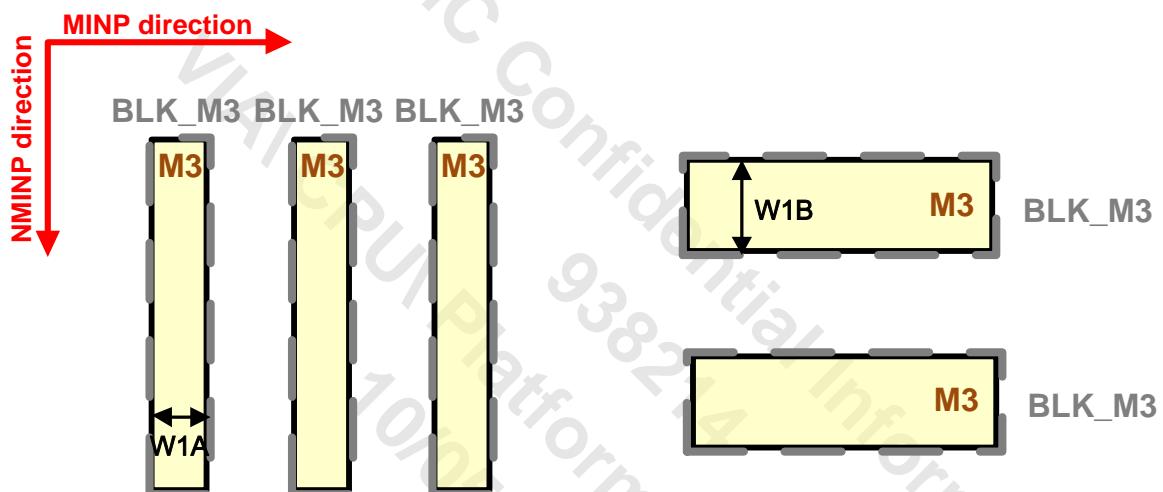
SRAM.M2.W.1.1



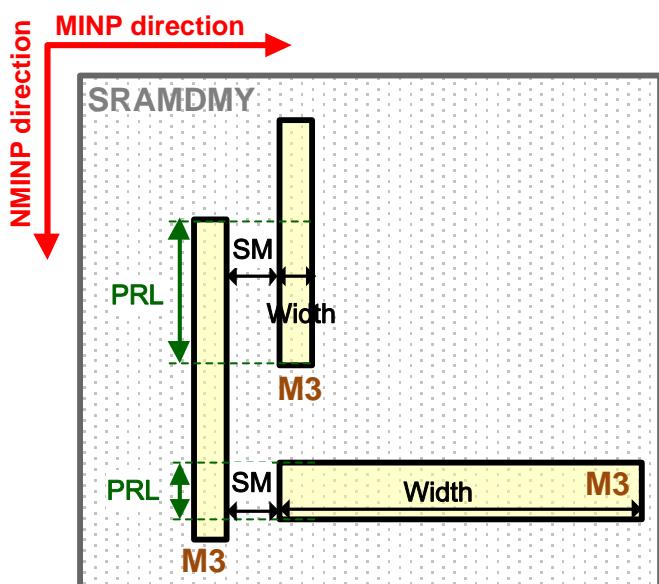
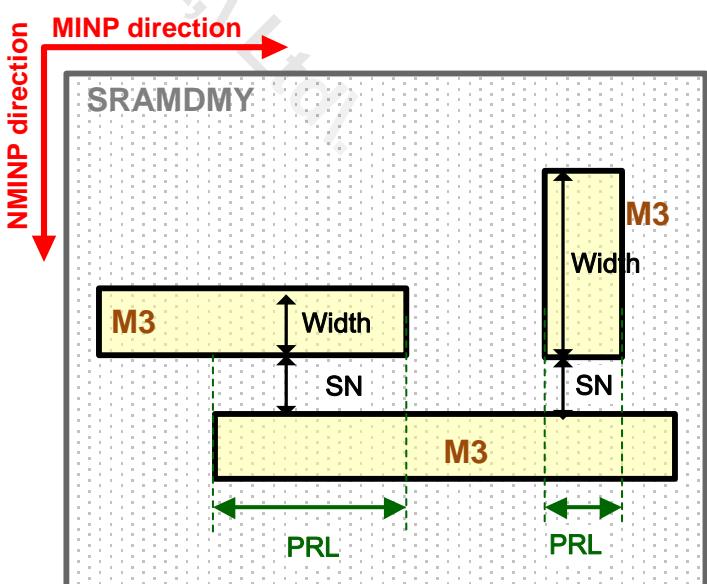
SRAM.VIA2.S.2.1.1

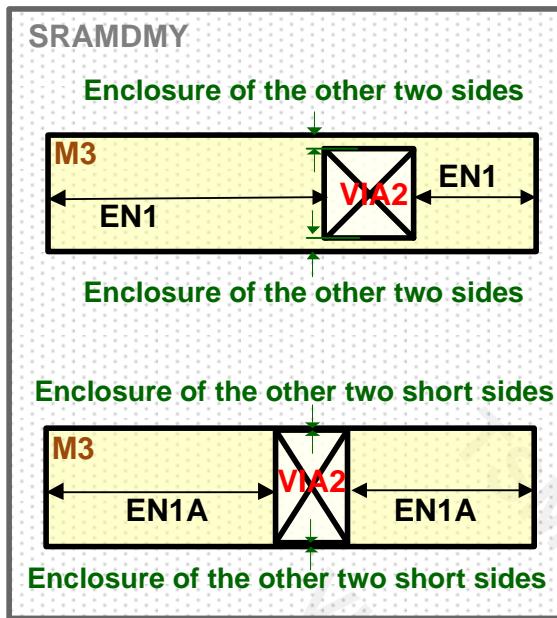


SRAM.VIA2.EN.1.1

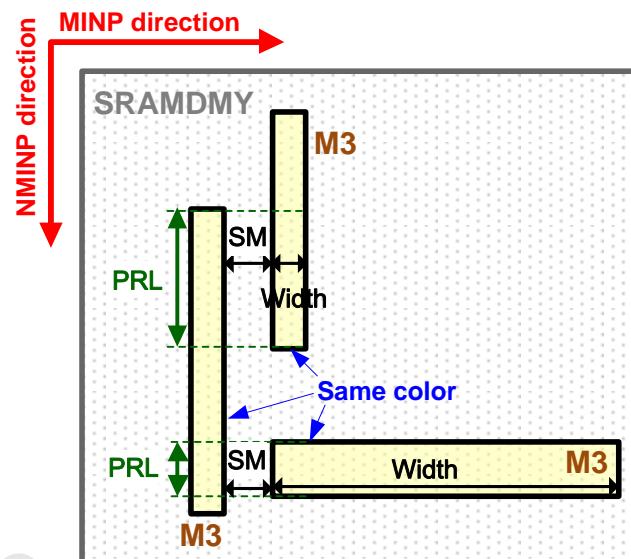


SRAM.M3.W.1.1 / SRAM.M3.W.1.2

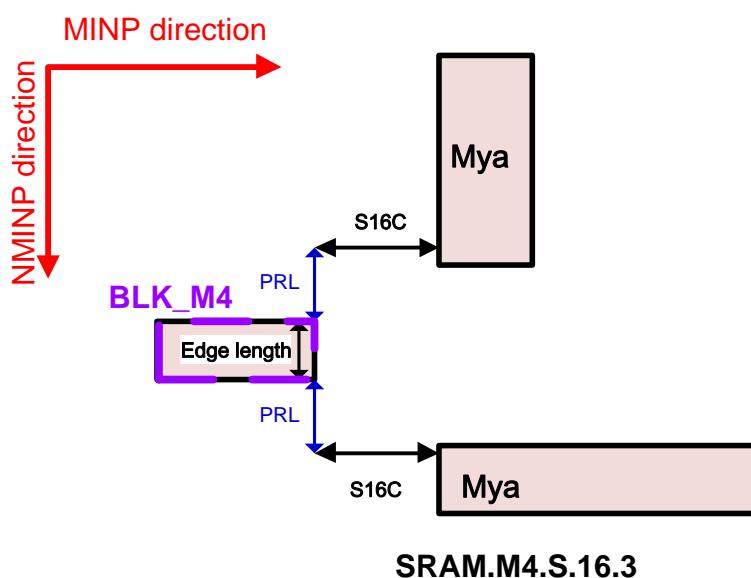
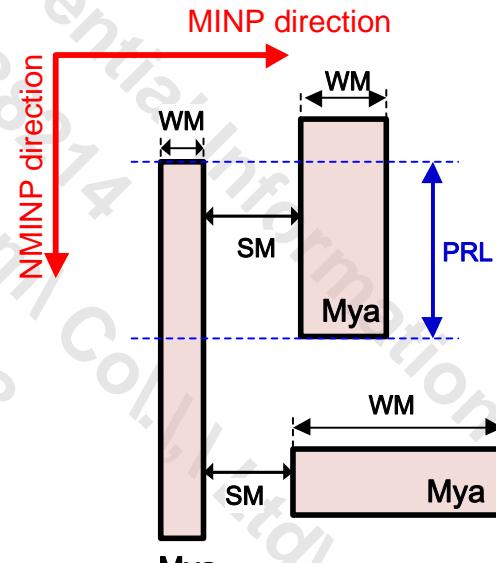
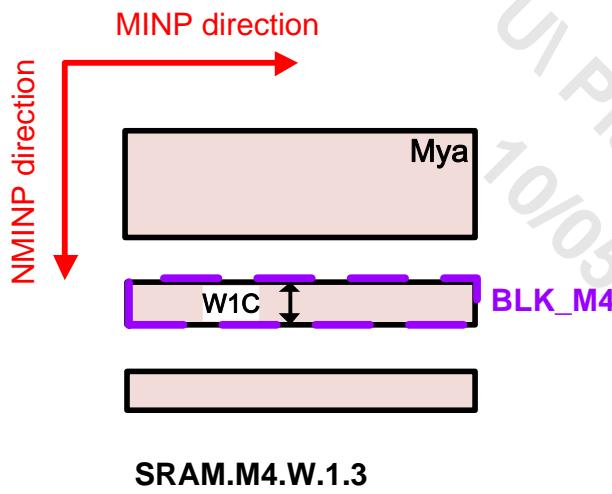
SRAM.M3.S.2 /
SRAM.M3.S.2.1SRAM.M3.S.3.2 /
SRAM.M3.S.3.3



**SRAM.M3.EN.1 / SRAM.M3.EN.1.1 /
SRAM.M3.EN.31.7**



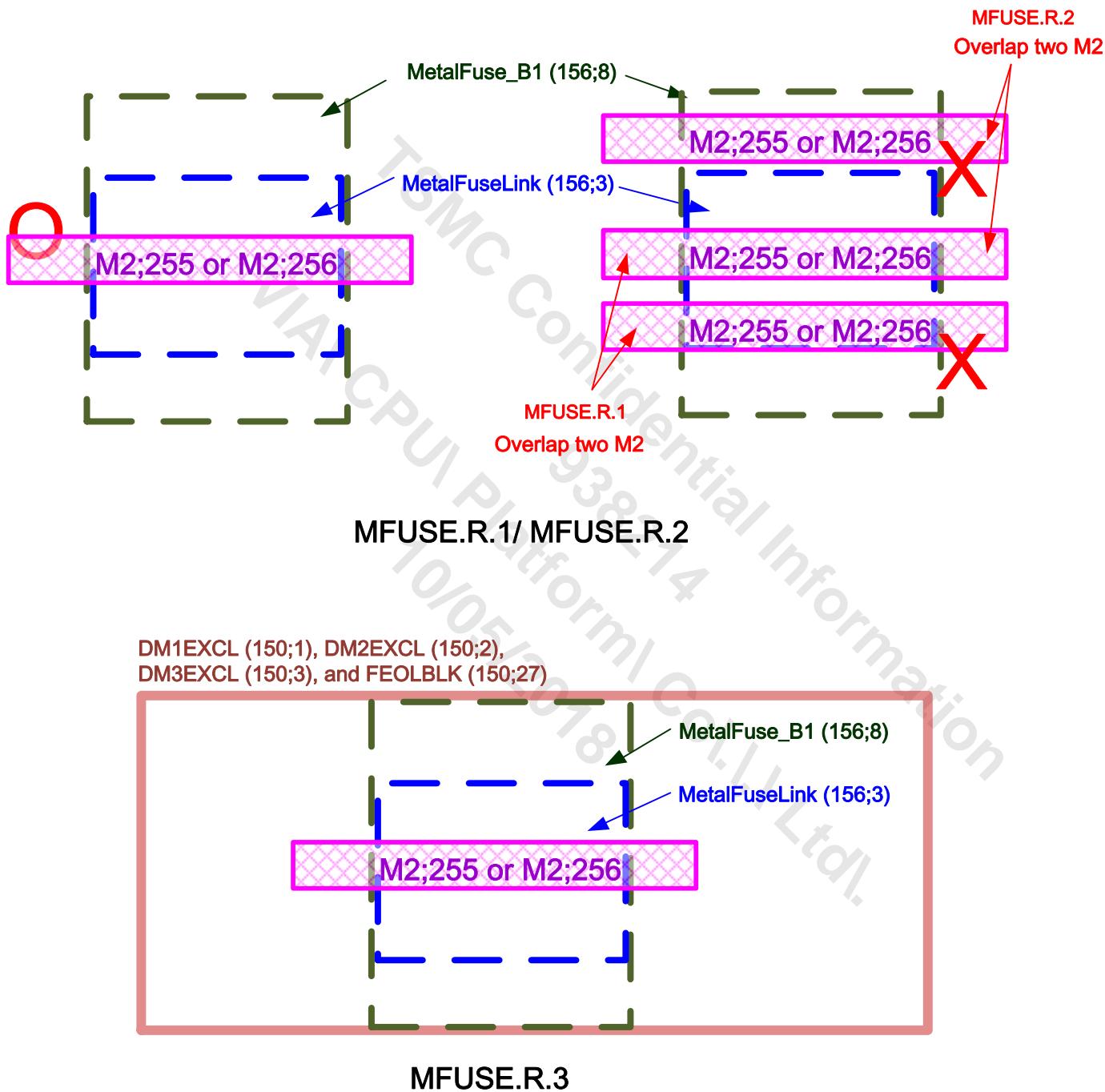
**SRAM.M3.CS.1.1.3 /
SRAM.M3.CS.1.1.4**

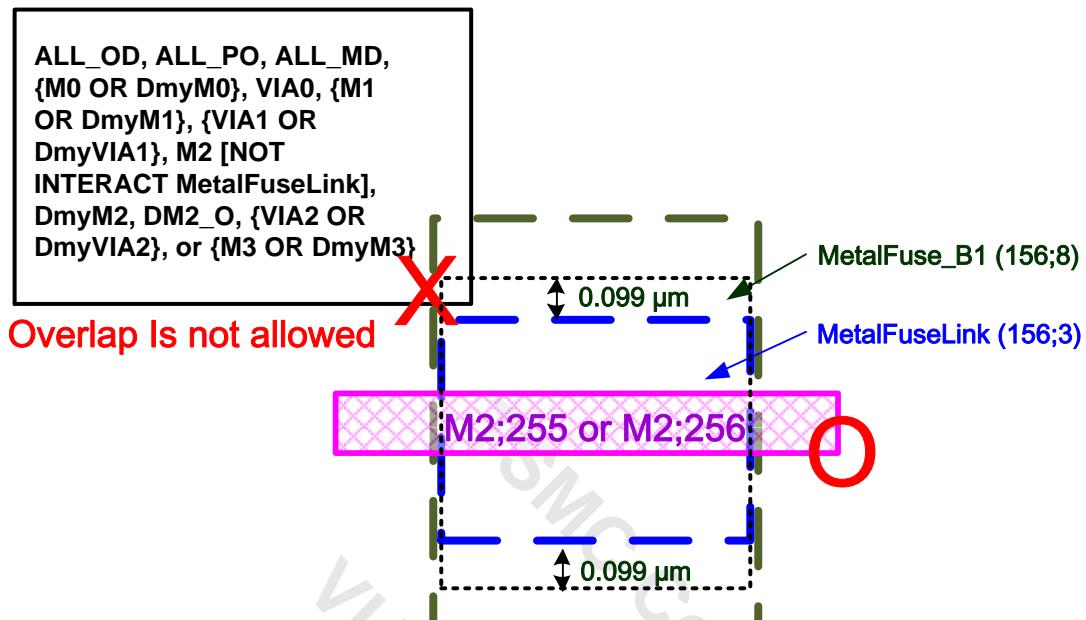


4.5.68 MetalFuse Layout Rules

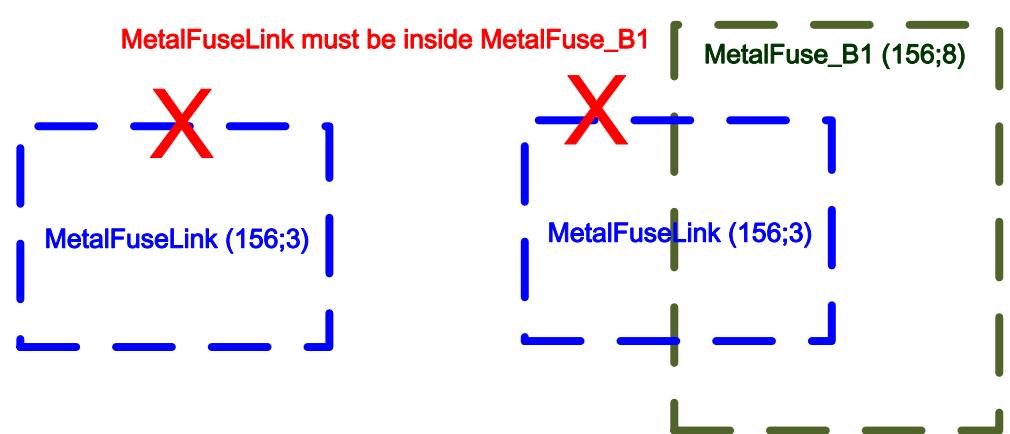
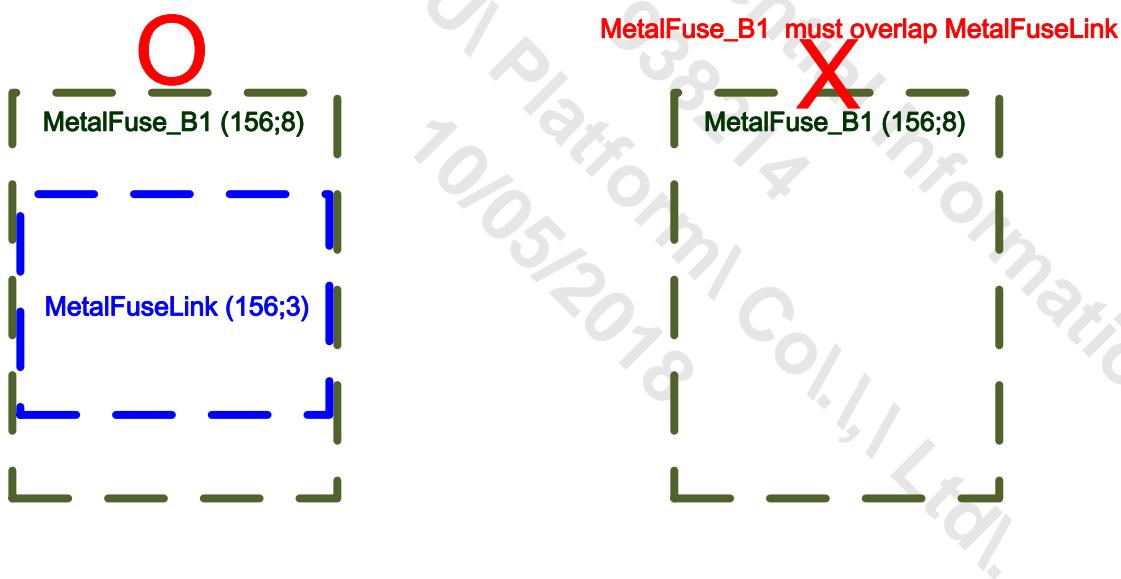
Rule No.	Description	Label	Op.	Rule
MFUSE.R.1	MetalFuseLink (156;3) must overlap M2;400.			
MFUSE.R.2	MetalFuse_B1 (156;8) must overlap M2;400.			
MFUSE.R.3	MetalFuse_B1 (156;8) must be inside DM1EXCL (150;1), DM2EXCL (150;2), DM3EXCL (150;3), and FEOLBLK (150;27). MetalFuse_B1 (156;8) must overlap DM1EXCL (150;1), DM2EXCL (150;2), DM3EXCL (150;3), and FEOLBLK (150;27) at the same time.			
MFUSE.R.4	{MetalFuseLink (156;3) SIZING 0.099 μ m in vertical direction} overlap ALL_OD, ALL_PO, ALL_MD, {M0 OR DmyM0}, VIA0, {M1 OR DmyM1}, {VIA1 OR DmyVIA1}, M2 [NOT INTERACT MetalFuseLink], DmyM2, DM2_O, {VIA2 OR DmyVIA2}, or {M3 OR DmyM3} is not allowed.			
MFUSE.R.5	MetalFuse_B1 (156;8) must overlap MetalFuseLink (156;3). MetalFuseLink (156;3) must be inside MetalFuse_B1 (156;8).			

MetalFuse





MFUSE.R.4



MFUSE.R.5

4.5.69 Antenna Effect Prevention (A) Layout Rules

Rule No.	Description	Label	Op.	Rule
A.R.0	Antenna prevention without OD rules: A.R.1, A.R.2, A.R.3, A.R.4, A.R.6, A.R.6.1, A.R.6.4, A.R.9, A.R.10, A.R.11 Antenna prevention with OD rules: A.R.7, A.R.8, A.R.8.1, A.R.12, A.R.13 (DRC won't check PODE_GATE [on STRAP] not connect to GATE [on ACTIVE])			
A.R.1	Drawn ratio of the cumulative poly (PO NOT CPO) top area to the cumulatively connected GATE area		≤	50
A.R.2	Drawn ratio of the cumulative poly (PO NOT CPO) sidewall area to the cumulatively connected GATE area (Except BLK_WF)		≤	125
A.R.3	Drawn ratio of the cumulative {MP OR MD} [INTERACT PO] area to the cumulatively connected GATE area		≤	100
A.R.4	Single-layer drawn ratio of the cumulative via area to the cumulatively connected GATE area that is connected directly to it		≤	20
A.R.6	Ratio of the cumulative metal top area (from M0 to top metal) to the cumulatively connected GATE area [I/O in OD2/ NOT in OD2]		≤	500/5000
A.R.6.1	Ratio of the cumulative metal top area (from M0 to top metal) to the cumulatively connected GATE area [I/O in OD2, GATE area $\geq 220 \mu\text{m}^2$]		≤	$54900 \times (\text{GATE area})^{(-0.87)}$
A.R.6.2	Top metal [connect to {GATE in OD2}] must connect to protection OD			
A.R.6.4	Maximum 1.8V/1.5V IO gate area in same connection This rule checked by the cumulative connection (from M0 to top metal respectively)		≤	1000000
A.R.7	Drawn ratio of the cumulative via area (from VIA0 to top VIA) to the cumulatively connected GATE area with protection OD (1) for gate area $\leq 0.0300 \mu\text{m}^2$, the formula is VIA_area / (gate area + 5 x OD_area) (2) for gate area $> 0.0300 \mu\text{m}^2$, the formula is VIA_area / (gate area + 5 x OD_area + 17)		≤	50
A.R.8	Drawn ratio of the cumulative metal top area (from M0 to Last Metal-1) to the cumulatively connected GATE area with protection OD (1) for gate area $\leq 0.0300 \mu\text{m}^2$, the formula is Metal_area / (gate area + 0.5 x OD_area) (2) for gate area $> 0.0300 \mu\text{m}^2$, the formula is Metal_area / (gate area + 0.5 x OD_area + 7.6)		≤	5000
A.R.8.1	Drawn ratio of the cumulative top metal top area to the cumulatively connected GATE area with protection OD		≤	$\text{OD area} \times 8000 + 50000$
A.R.8.3	Risk_Floating_net space to Mn ($n = 0 \sim 5$) [connects to OD] $< 0.0365 \mu\text{m}$, and $\geq 0.0315 \mu\text{m}$ is not allowed Definition: 1. Risk_Floating_net: cumulative floating metal and VIA top area [cumulative area $> 36000 \mu\text{m}^2$, from M0 to top metal and VIA0 to top VIA, and does not connect to OD] 2. floating metal and VIA: metal and VIA does not connect to OD This rule is checked by the cumulative connections (from M0 to top metal and VIA0 to top VIA respectively)			
A.R.8.4	Risk_Floating_net space to Mn ($n = 0 \sim 5$) [connects to OD] $< 0.0315 \mu\text{m}$ is not allowed Definition: 1. Risk_Floating_net: cumulative floating metal and VIA top area [cumulative area $> 10000 \mu\text{m}^2$, from M0 to top metal and VIA0 to top VIA, and does not connect to OD] 2. floating metal and VIA: metal and VIA does not connect to OD			

Rule No.	Description	Label	Op.	Rule
	This rule is checked by the cumulative connections (from M0 to top metal and VIA0 to top VIA respectively)			
A.R.8.5	<p>Mn_pad_floating space to Mn [connects to OD ,from M0 to AP] $\leq 0.100 \mu\text{m}$ is not allowed</p> <p>Definition of Mn_pad_floating : The metal (from M0 to AP) follows the following conditions (1) does not connect to OD, and (2) connect to AP_PAD [width of AP interact {CB2_WB OR CB2_FC} > 31.5 μm]</p> <p>This rule is checked from M0 to AP respectively</p>			
A.R.9	Ratio of the cumulative via area (from VIA0 to top VIA) to the cumulatively connected GATE area [in OD2/ NOT in OD2]		\leq	50/NA
A.R.10	Drawn ratio of the cumulative RV area to the cumulatively connected GATE area [in OD2/ NOT in OD2]		\leq	20/200
A.R.11	Drawn ratio of the cumulative AP sidewall area to the cumulatively connected GATE area [in OD2/ NOT in OD2]		\leq	1000/2000
A.R.12	Drawn ratio of the cumulative RV area to the cumulatively connected GATE area with protection OD		\leq	OD area x 83 + 400
A.R.13	Drawn ratio of the cumulative AP sidewall area to the cumulatively connected GATE area with protection OD		\leq	OD area x 8000 + 30000
A.R.14	<p>Drawn ratio of the cumulative top metal top area (top_metal + top_metal-1) to the cumulatively connected M0_AR area [area > 0.5 μm^2]</p> <p>Definition of M0_AR: $\{\text{Checked_M0 AR AND Checked_MEAR}\}$ [Different net]</p> <p>Definition of Checked_M0 AR: $\{\text{M0 NOT CM0}\}$ does not connect to OD</p> <p>Definition of Checked_MEAR: $\{\text{MP [width = 0.022 } \mu\text{m}] \text{ OR } \{\text{ALL_MD NOT ALL_CMD}\} [\text{INTERACT }\{\text{ALL_OD OR MP [width = 0.022 } \mu\text{m}]\}]\}$</p>		\leq	100
A.R.15	<p>Risk_net_area_product [connects to Risk_metal] is not allowed</p> <p>Definition of Risk_net_area_product for respective VIAn layer: (1) Floating_VIAn: VIAn connects none of OD or GATE (2) Floating_VIAnA: Cumulative area of each/single Floating_VIAn layer (3) Floating_MnA: Cumulative areas of all metal layers under Floating_VIAn (4) Risk_net_area_product = (Floating_VIAnA) x (Floating_MnA) ≥ 260000</p> <p>Definition of Risk_metal for respective Mn layer: (1) Floating_Mn+1: Mn+1 [connects to Risk_net_area_product] (2) Risk_metal : Cumulative area of Floating_Mn+1 [width $\leq 0.048 \mu\text{m}$] > 100 μm^2</p> <p>(This check is only applied to VIA0/VIAx/VIAxa/VIAya/VIAy/VIAyy/VIAYx/VIAYz/VIAz/VIAr)</p>			

Table Notes:

- It is recommended to have OD connection to the poly gate through metal lines for all devices.
- All N+ OD and P+ OD areas connected to metal or via do contribute to the OD area. (Including source or drain diffusion of MOSFET and Strap areas)
- The Antenna rules apply separately to both thin (core) and thick (I/O) gate oxides.
- RDL designs should take antenna rules into account.
- All of the ODs in the same net can be treated as effective protection OD (s) against plasma charging.

6. In order to avoid the antenna ratio mismatch between the paired devices, metal lines need to be as symmetry as possible.
7. The transistors in mismatch sensitive configurations shall be tied to an active region by M0 to prevent process-induced damage.
8. When an error is detected at DRC, antenna ratio can be reduced by the following suggestion; connect the node to a OD, connect the gate to the highest metal level as close to the gate as possible, or connect the node to the output of the driver with a lower metal level.
9. DRC implementation for calculations of metal to gate area ratio in cumulative antenna rules,

“Cumulated Ratio” of A.R.6 rule is defined as:

$$\text{Area}(Mx(n))/\text{Area}(\text{GATE}(n)) + \text{Area}(Mx-1(n-1))/\text{Area}(\text{GATE}(n-1)) + \dots + \text{Area}(M0(0))/\text{Area}(\text{GATE}(0))$$

Where GATE(n) is the total GATE area in a particular net constructed by the incremental connections up to current nth stage.

Mx(n) is the whole area of metal x (x = 0 ~ top) in the same net.

Definition of the protection OD for antenna rules:

Total area of (OD NOT POLY) INTERACT MD on the same net

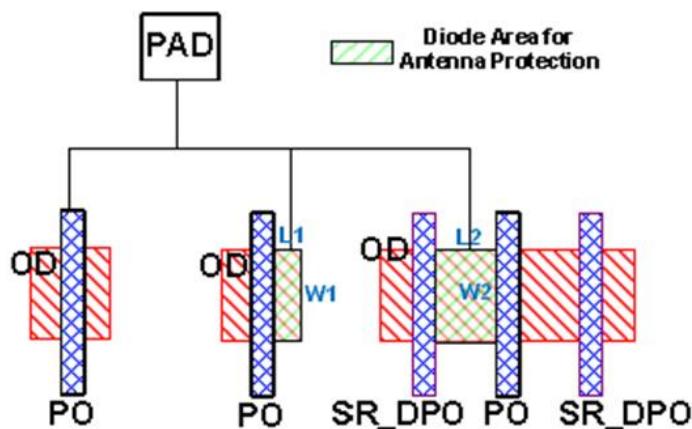
10. Failure Criterion

- Tailing percentage of 20% changes in gate current in Log-normal distribution (which is expressed with the following equation) is less than 5%.

$$\Delta Ig (\%) \equiv \left| \frac{Ig(n) - Ig(n - 1)}{Ig(n - 1)} \right| \times 100\%$$

11. OD area illustration

$$\text{OD area} = (W1 \times L1 + W2 \times L2)$$

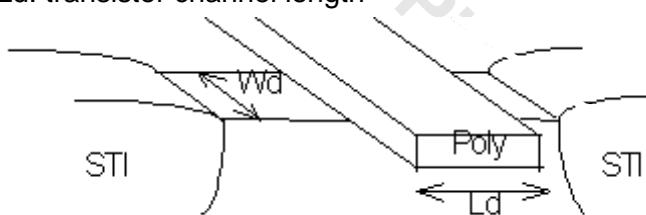


12.

$$\text{Gate area} = (2.5 \times Wd \times Ld) \text{ for } \geq 2\text{-fin device}$$

Wd: transistor channel width

Ld: transistor channel length



4.5.69.1 Poly Antenna Ratio

The definition of the **poly top area antenna ratio** for each layer is:

$$\text{ratio} = (L_p \times L_d + L_{pe} \times W_{pe}) / \text{Gate area}$$

The definition of the **poly sidewall area antenna ratio** for each layer is:

$$\text{ratio} = 2 \times [(L_{pe} + W_{pe} + L_p) \times t] / \text{Gate area}$$

- L_p: length of field poly connected to gate
- W_p: width of field poly connected to gate
- L_{pe}: length of field poly extension connected to gate
- W_{pe}: width of field poly extension connected to gate
- t: poly thickness
- L_d: transistor channel length

4.5.69.2 M0-top metal Antenna Ratio

The definition of the M0-top metal antenna ratio for each layer is:

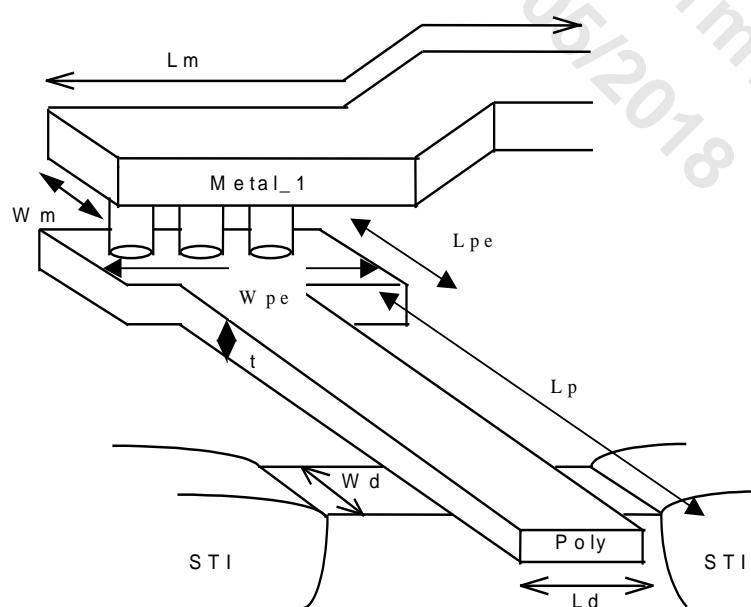
$$\text{ratio} = (W_m \times L_m) / \text{Gate area}$$

- L_m: length of metal line connected to gate
- W_m: width of metal line connected to gate

4.5.69.3 Via0 – top Via Antenna Ratio

The definition of VIA0-top Via antenna ratio is:

$$\text{ratio} = \{\text{total via area}\} / \text{Gate area}$$



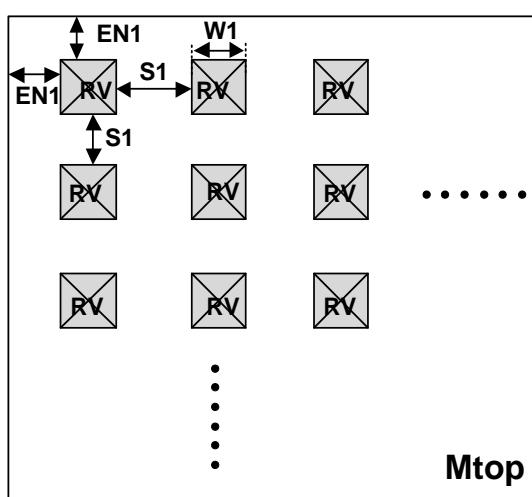
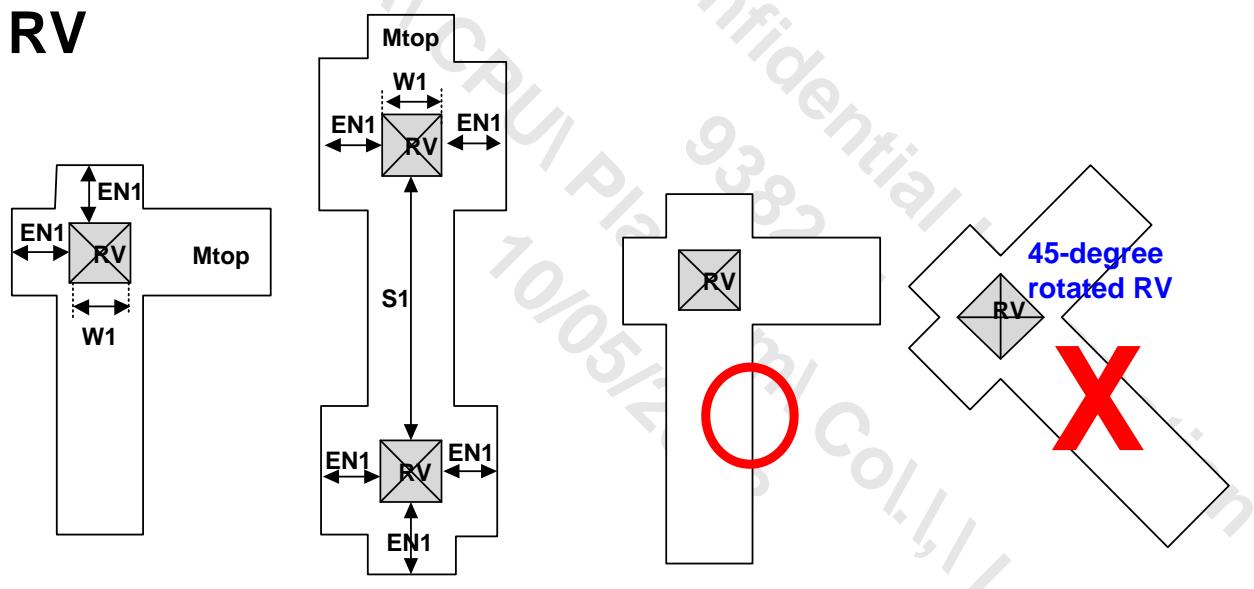
4.5.70 RV Layout Rules [optional]

CB-VD mask (306) is generated by the logical operation of CB (CAD layer: 76) and RV (CAD layer: 85).

Please allow sufficient RV counts to provide enough current for EM and ESD protection. Therefore, it is recommended to put as many RV holes as possible.

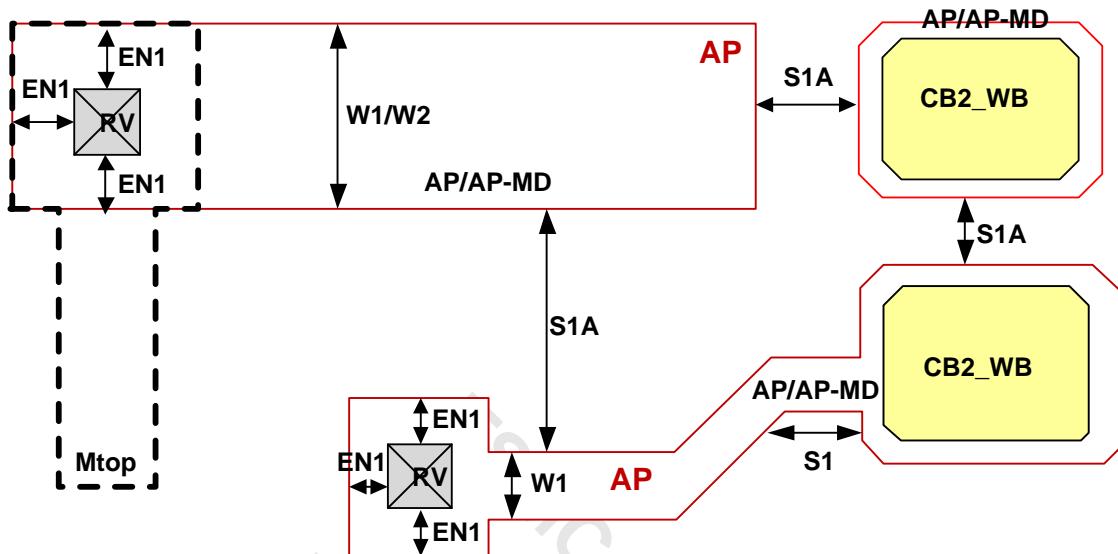
Rule No.	Description	Label	Op.	Rule
RV.W.1	Width (maximum = minimum) (Except SEALRING_ALL)	W1	=	2.7
RV.S.1	Space	S1	\geq	1.8
RV.EN.1	Enclosure by Mtop (Except SEALRING_ALL)	EN1	\geq	0.4500
RV.R.1	45-degree RV is not allowed (Except SEALRING_ALL, INDDMY)			
RV.R.2	RV.W.1, RV.S.1, and RV.EN.1 allow 0.009 μm tolerance on 45-degree rotated RV in INDDMY			

RV



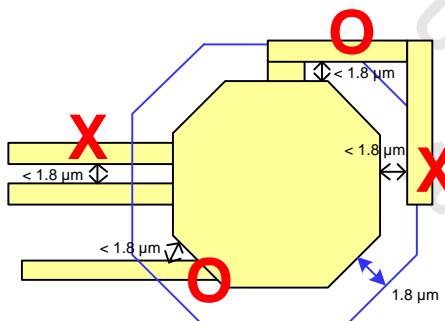
4.5.71 AI Redistribution Layer (AP RDL) Layout Rules [optional]

Rule No.	Description	Label	Op.	Rule
AP.W.1	Width (interconnection only)	W1	\geq	1.8
AP.W.2	Maximum width by {AP/AP-MD SIZING up/down 0.899 μm } (Interconnection only) (Except UBM, CBD, CB2_FC, CB, CB2_WB)	W2	\leq	31.5
AP.W.3	AP hole width for 28K \AA AP (Except following conditions: 1. < 100 inner 90-degree corner of AP holes [width < 2.7 μm] within window 100 $\mu\text{m} \times 100 \mu\text{m}$, stepping 50 μm)	W3	\geq	2.7
AP.S.1	Space (Except following conditions in the same polygon: 1. {{AP AND {AP_PAD SIZING 1.8 μm }} NOT AP_PAD} [INTERACT AP_PAD], 2. jog length \leq 0.9 μm , 3. AP hole [Width < 1.8 μm]) Definition of AP_PAD: Width of AP [INTERACT {CB2_WB OR CB2_FC}] > 31.5 μm	S1	\geq	1.8
AP.S.1.1	Space of metal pad, or space of metal pad to metal line [different nets] The definition of metal pad: The width of {AP INTERACT CB2_WB} > 31.5 μm	S1A	\geq	2.25
AP.S.1.2	Space [INSIDE INDDMY]	S1B	\geq	1.8
AP.EN.1	Enclosure of RV	EN1	\geq	0.4500
AP.DN.1	Minimum AP density across full chip		\geq	10%
AP.DN.2	Maximum AP density across full chip		\leq	80%
AP.R.1	AP.S.1 allow 0.009 μm tolerance on 45-degree bent AP in INDDMY.			

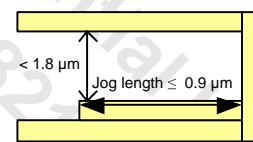


AP.W.1 / AP.W.2 / AP.S.1 / AP.S.1.1 / AP.EN.1

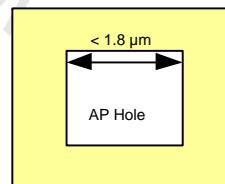
Exception 1: Surround PAD



Exception 2: Jog length ≤ 0.9 μm

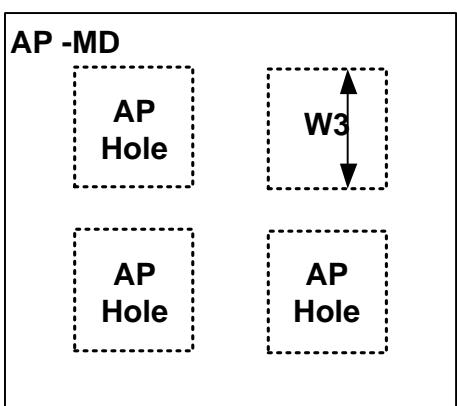


Exception 3: AP hole < 1.8 μm

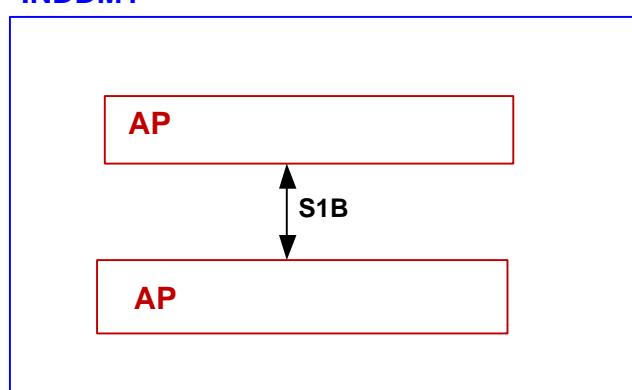


AP.S.1

INDDMY



AP.W.3



AP.S.1.2

4.5.72 Seal Ring Rules

This chapter has been divided into the following topics:

- 4.5.71.1 Seal ring overview
- 4.5.71.2 Guidelines for placing seal ring
- 4.5.71.3 Seal ring dummy OD/PO rules
- 4.5.71.4 Chip corner stress relief (CSR) pattern
- 4.5.71.5 Seal ring layout rules
- 4.5.71.6 Scribe line dummy bar (SLDB) layout rules

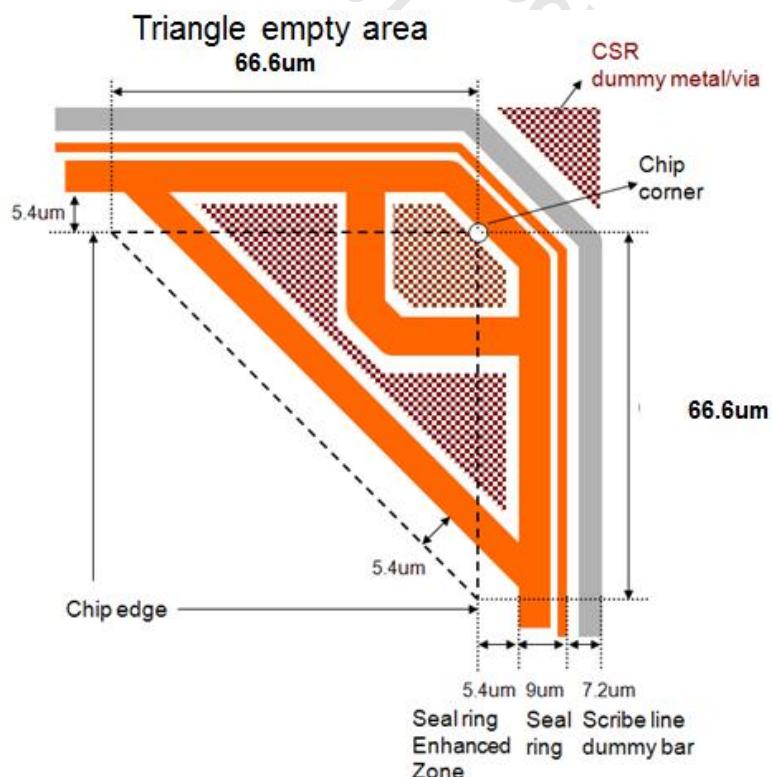
4.5.72.1 Seal Ring Overview

- The general N7+ seal ring structure consists of three major parts: (i) seal ring enhanced zone (SREZ); (ii) corner stress relief (CSR) pattern; and (iii) seal ring wall. In addition, the seal ring is surrounded by 7.2- μm -wide scribe line dummy bar (SLDB). Fig. 2.1.1. Shows the details.
- The seal ring structure can protect the chip from the die saw damage in order to manage the saw quality. It can reduce the impact of damage induced by thermal stress during packaging and field applications.
- To add seal ring, triangle empty areas ($66.6 \mu\text{m}$) at 4 chip corners must be reserved and no layout is allowed inside. Please must follow the triangle empty rule CSR.R.1.



Warning: Violation of this rule, CSR.R.1, may result in serious layout mistake thus the corrections of many masks may be required! Please do jobview the mask data after adding the seal ring.

Fig. 2.1.1. Three major parts of the seal ring and the scribe line dummy bar: (i) seal ring enhanced zone (SREZ); (ii) seal ring wall; (iii) corner stress relief (CSR) pattern; (iv) scribe line dummy bar (SLDB).



4.5.72.2 Guidelines for Placing Seal Ring

There are two ways to mount the seal ring structure into your design:

1. Added by TSMC: Customers can request TSMC to add the seal ring during post tape out data preparation. Please must follow CSR.R.1 if this option is selected.

2. Added by Customer: Customers can choose to add the seal ring before tape out. Six unit cells GDS files (archived along with this document) are prepared for this purpose. Please select the proper gds layers matching with the metal scheme of your design by following the seal ring rules and SLDB rules in the following. Customers also need to follow the N7+ seal ring placement guide document to combine the seal ring unit cell as completed seal ring.



Warning: It is strongly recommended to use the TSMC standard seal ring. Seal ring different from the TSMC standard one requires a special approval from TSMC to mitigate risk during die saw and package. Please contact TSMC to get assistance if an approval process is needed.

The following CAD layers are required for seal ring structure and SLDB in addition to Via and Metal layers, please keep these layers in the sample gds file:

Layer Name	CAD Layer #/Data type	Flip Chip required	Wire Bond required
SR_DOD	6;7	V	V
OD_DA	6;15	V	V
COD_H	6;17	V	V
COD_V	6;18	V	V
COD_BLOCK	6;22	V	V
SR_DPO	17;7	V	V
POMM	17;15	V	V
WPOM	17;19	V	V
POMMB	17;20	V	V
PP	25;0	V	V
NP	26;0	V	V
SR_DMD	84;7	V	V
VC	179;400	V	V
VIA0	159;250	V	V
CBD	169;0	V	X
CB	76;0	X	V
CB2_FC	86;0	X	X
CB2_WB	86;20	X	X
PM	5;0	V	Optional
LMARK	109;0	V	V
SEALRING	162;0	V	V
SEALRING_DB	162;1	V	V
SEALRING_ALL	162;2	V	V
SEALRING_EN	162;3	V	V
CSRDMY	166;0	V	V

- a.CBD is a required layer in seal ring region for CB-VD mask (passivation-1) generated from (RV or CBD).
 b.Layer SEALRING_ALL (162;2) is used to waive logic rule violations in the seal ring, SLDB, CSR, and seal ring enhanced zone (SREZ) regions.

4.5.72.2.1 Metallization Options

For any metal combination, a marker “(1+X+Z+R)M_XxZzRr” can be used to represent the metal combination of M_x, M_z, and M_r.

The marker is interpreted as one layer of M₁, X layers of M_x, Z layers of M_z, and R layers of M_r. The total metal layer number is (1+X+Z+R)

Naming for different metal types

Metal type	Code	Data Type	Code on MT	Material
M ₀	M ₀	255, 256	M ₀	ELK
M ₁	M ₁	420	M ₁	ELK
M _{xs}	M _{xs}	400	M _{xs}	ELK
M _x	M _x	255, 256, 275, 276	M _x	ELK
M _{xa}	M _{xa}	295, 296, 315, 316	M _{xa}	ELK
M _{ya}	M _{ya}	330, 340	M _{ya}	ELK
M _y	M _y	350, 360	M _y	ELK
M _{yy}	M _{yy}	90	M _{yy}	ELK
M _{yx}	M _{yx}	370	M _{yx}	LK
M _{yz}	M _{yz}	30	M _{yz}	LK
M _z	M _z	40	M _z	USG
M _r	M _r	80	M _r	USG

Naming for different Via types

Via type	Code	Data Type	Code on MT
VIA0	VIA0	420	V0
VIAxs	VIAxs	400	Vxs
V _x	V _x	250	V _x
V _{xa}	V _{xa}	290	V _{xa}
V _{ya}	V _{ya}	330	V _{ya}
V _y	V _y	350	V _y
V _{yy}	V _{yy}	90	V _{yy}
V _{yx}	V _{yx}	370	V _{yx}
V _{yz}	V _{yz}	30	V _{yz}
V _z	V _z	40	V _z
V _r	V _r	80	V _r

Metallization CAD layers

Layer	CAD Layer ID
MD	84
VC	179
Metal-0	180
Via-0	159
Metal-1	31
Via-1	51
Metal-2	32
Via-2	52
Metal-3	33
Via-3	53
Metal-4	34
Via-4	54
Metal-5	35
Via-5	55
Metal-6	36
Via-6	56
Metal-7	37
Via-7	57
Metal-8	38
Via-8	58
Metal-9	39
Via-9	59
Metal-10	40
Via-10	60
Metal-11	41
Via-11	61
Metal-12	42
Via-12	62
Metal-13	43
Via-13	63
Metal-14	44
Via-14	64
Metal-15	45

TSMC Confidential Information
938214
10/05/2018

For example, in a 9M_1xs1xa1ya3y2z scheme, the Metal-0,Via-0,Metal-1, should be use layer (180;255), (180;256), (159;420) and (31;420) respectively, for M0,Via-0, and M1 layers. The Via-1 and Metal-2 should be use layer (51;400),(32;400), respectively, for Vxs and Mxs layers. The Via-2 and Metal-3 should be use layer (52;290),(33;295),(33;296), respectively, for Vxa and Mxa layers. The Via-3 and Metal-4 should be use layer (53;330), (34;340), respectively, for Vya and Mya layers. The Via-4 and Metal-5, Via-5 and Metal-6, Via-6 and Metal-7 should be use layer (54;350), (35;350), (55;350), (36;360), (56;350), (37;360) respectively, for Vy and My layers. The Via-7, Metal-8, Via-8 and Metal-9 should be use layer (57;40), (38;40), (58;40) and (39;40) respectively, for Vz and Mz layers.

If customers want to add the seal ring and SLDB before tape out (option 2), please use TSMC sample GDS file for seal ring and SLDB as a starting file, and follow the descriptions below to select the related metal and via layers for your design.

4.5.72.3 Seal Ring Dummy OD/PO Rules

1. In order to meet the extremely tight requirement in terms of process control for good Poly uniformity to meet the PO CD as well as circuit performance requirement. The PO is needed to design under the seal ring structure. Please refer to Fig. 2.3.1. for example.
2. PO is uniformly designed under the seal ring and scribe line dummy bar (SLDB). The general N16 seal ring structure consists of three major parts: (i) seal ring enhanced zone (SREZ); (ii) corner stress relief (CSR) pattern; and (iii) seal ring wall. In addition, the seal ring is surrounded by 7.2- μm -wide scribe line dummy bar (SLDB). Fig. 2.1.1. shows the details.
3. SEALRING_ALL (CAD layer 162;2) must cover seal ring enhanced zone (SREZ), seal ring wall, CSR and SLDB according to section 1.3. Following rules are to be checked inside SEALRING_ALL.

Rule No.	Description	Label	Op.	Rule
SLR.W.1	OD_DA width in SEALRING_EN (in vertical direction)	A	=	0.0380
SLR.W.1.1	OD_DA width in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	A1	=	0.1100
SLR.W.2	SR_DPO width in SEALRING_EN	B	=	0.0110
SLR.W.2.1	SR_DPO width in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	B1	=	0.1900, 0.2400
SLR.W.3	SR_DOD width in SEALRING_EN (in vertical direction)	A3	\geq	0.1580
SLR.W.4	SR_DMD width in SEALRING_EN	B2	\geq	0.0240
SLR.S.1	Space of OD_DA in SEALRING_EN	C	=	0.0820
SLR.S.1.1	Space of OD_DA in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	C1	\geq	0.1100
SLR.S.2	Space of SR_DPO in SEALRING_EZ	D	\geq	0.0460
SLR.S.2.1	Space of SR_DPO in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D1	\geq	0.2500
SLR.S.3	Space of SR_DOD in SEALRING_EN	C2	\geq	0.1600
SLR.S.3.1	Space of SR_DOD in SEALRING_EN (in vertical direction)	C3	\geq	0.2920
SLR.S.4	SR_DPO space to SR_DMD, in {SEALRING_ALL NOT SEALRING_EN} (SR_DPO overlap SR_DMD is not allowed) (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E1	\geq	0.2510
SLR.S.4.1	SR_DPO space to SR_DMD, in SEALRING_EN (SR_DPO overlap SR_DMD is not allowed)	E2	\geq	0.0110
SLR.S.6	Space of SR_DMD, in SEALRING_EN	E3	\geq	0.0330
SLR.EN.1	OD_DA enclosure by SEALRING_EN outer edge in horizontal Direction.	F	\geq	0.0740
SLR.EN.2	OD_DA in SEALRING_EN enclosure by chip edge in vertical direction	F1	=	0.0410
SLR.EN.3	CPO enclosure by SEALRING_ALL	F2	\geq	0.1080
SLR.EN.4	SR_DPO enclosure PP in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.001 \mu\text{m}$)	F3	=	0.0050
SLR.EN.5	OD_DA enclosure by SEALRING_EN inner edge in Horizontal Direction	F4	=	0
SLR.EN.6	NP enclosure by SEALRING_EN inner edge (DRC tolerance at 45-degree turning: $\pm 0.010 \mu\text{m}$)	F5	\geq	0.2400
SLR.O.1	SR_DPO overlap on OD_DA in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	G1	=	0.0400
SLR.O.2	SR_DMD overlap on OD_DA in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	G2	=	0.0390

Rule No.	Description	Label	Op.	Rule
SLR.O.3	PP outside SR_DPO overlap on OD_DA in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	G3	=	0.0550
SLR.PO.DN.7	Minimum {{PO OR SR_DPO} NOT CPO} local density in SEALRING_ALL 1. SLR.PO.DN.7 rule is checked over any $10 \mu\text{m} \times 10 \mu\text{m}$ area. (Stepping in $5 \mu\text{m}$ increments).		\geq	4.5%
SLR.PO.DN.8	Maximum {{PO OR SR_DPO} NOT CPO} local density in SEALRING_ALL 1. SLR.PO.DN.8 rule is checked over any $10 \mu\text{m} \times 10 \mu\text{m}$ area. (Stepping in $5 \mu\text{m}$ increments)		\leq	60%
SLR.R.1	OD_DA in SEALRING_EN must be rectangular			
SLR.R.2	CB2_WB/CB2_FC interact SEALRING_ALL is not allowed.			
SLR.R.4	COD_H / COD_V must be covered with COD_BLOCK in SEALRING_ALL			
SLR.R.5	SR_DPO must be vertical direction in SEALRING_EN			
SLR.R.6	SR_DMD must be vertical direction in SEALRING_EN			

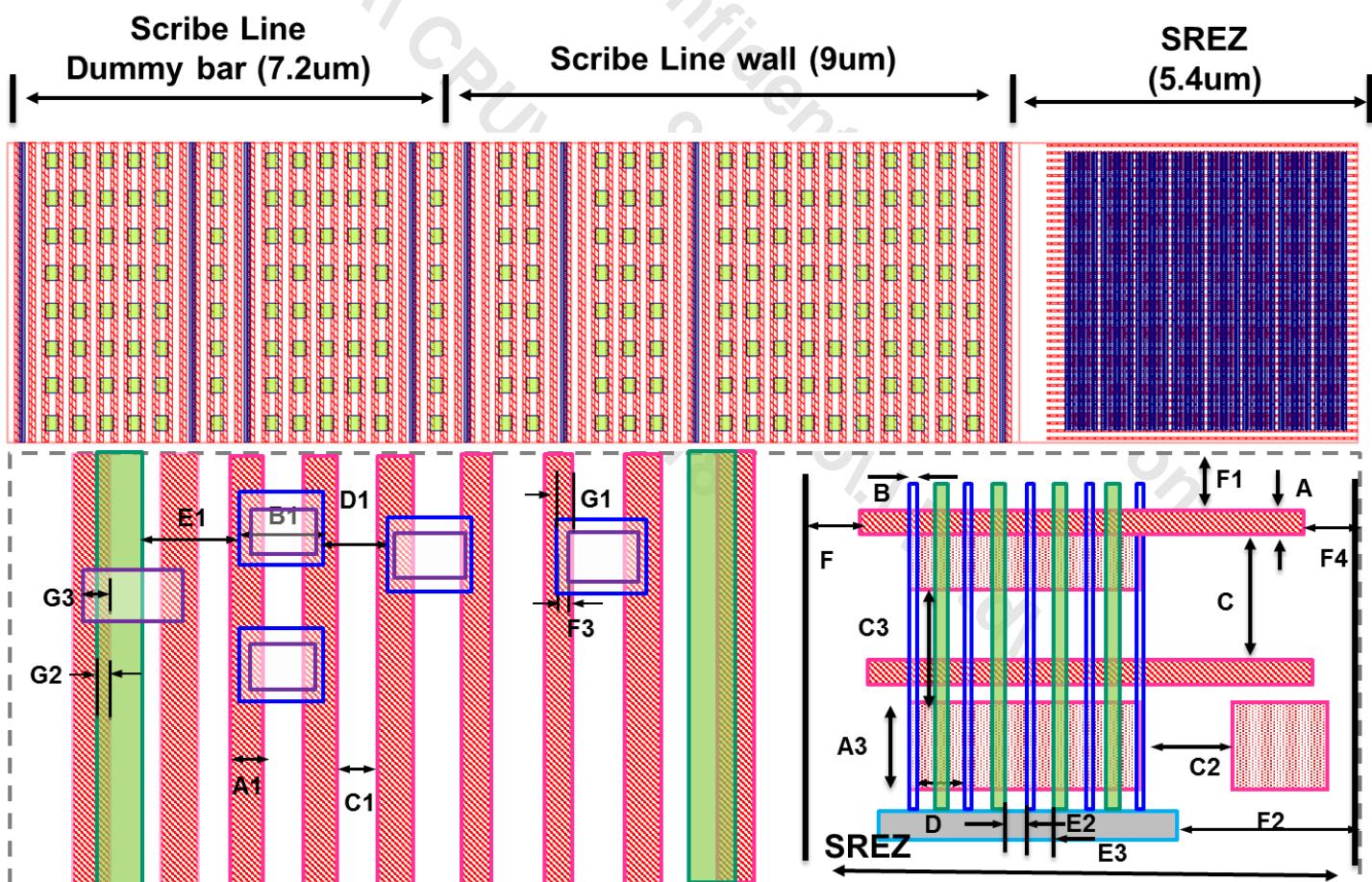
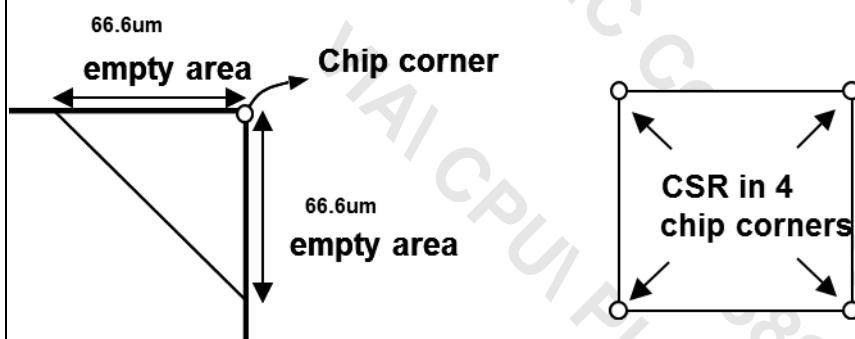


Fig. 2.3.1

4.5.72.4 Chip Corner Stress Relief (CSR) Pattern

Rule No.	Description	Label	Op.	Rule
CSR.R.1	Triangle empty areas (66.6 μm) at 4 chip corners must be reserved and no layout is allowed inside, as shown in Fig. CSR.R.1 Warning: Violation of this rule may result in serious layout mistake thus the corrections of many masks may be required! Please jobview the mask data after adding CSR and seal ring by tsmc.		=	66.6
CSR.R.1.1	Square empty areas (66.6 μm) at 4 chip corners interact AP is not allowed			



CSR.R.1 Triangle empty areas at 4 chip corners.

CSR.R.2	The CSR structure must include PM, AP, {{CB OR CBD} OR RV}, Mtop/Mtop-1 (top metal), VIAtop/VIAtop-1, M12, VIA11...VIA1, M1, VIA0, M0, VC, SR_DMD, PP, OD_DA, SR_DPO layers. The CSR pattern includes additional 1.8/5.4 μm width seal ring and reinforced metal structure, as shown in Fig. 4.5.71.4.2.			
CSR.R.4	CSRDMDY layer (CAD layer: 166;0), is must if customers add seal ring by themselves. DRC does not check CSR related rules w/o those dummy layers.			
CSR.R.6	CSRDMDY_A interact AP is not allowed (Except following conditions: 1. AP [INSIDE {{SEALRING (162;0) SIZING 3.6 μm } OR SEALRING_DB (162;1)}]) Definition of CSDMDY_A: The bounding box enclosed CSDMDY DRC flags CSDMDY_A INTERACT {AP NOT {{SEALRING (162;0) SIZING 3.6 μm } OR SEALRING_DB (162;1)}}}			
CSR.W.1	Width of reinforced metal structure only for My, Myy and Mz	a	=	8.1~9.1
CSR.L.1	Length of reinforced metal structure	b	=	21.6~22.5
CSR.R.3	Distance between 45-degree outer seal ring and seal ring corner	d	=	16.2~18
CSR.R.5	DMV pattern in CSR must include Mtop/VIAtop/Mtop-1/VIAtop-1/Mtop-2/VIAtop-2.../VIA1/M1 (DMV pattern: metal/via dummy pattern)			
CSR.DM.W.1	Metal width of DMV in CSR region	S	=	Table. 4.5.71.4.1.
CSR.DM.S.1	Metal space of DMV in CSR region	T	\geq	Table. 4.5.71.4.1.

Rule No.	Description	Label	Op.	Rule
CSR.DM.S.2	Metal space of DMV to CSR metal bar	R	\geq	Table. 4.5.71.4.1.
CSR.DM.O.1	Overlay of two adjacent DMV metal layers. Except Mr.	U	=	Table. 4.5.71.4.1.
CSR.DV.W.1	Via width of DMV in CSR region	P	=	Table. 4.5.71.4.1.
CSR.DV.S.1	Via space of DMV in CSR region	Q	\geq	Table. 4.5.71.4.1.
CSR.DV.EN.1	DMV via enclosure by DMV metal in CSR region. DMV via must be inside DMV metal.	V	\geq	Table. 4.5.71.4.1.

Remark:

Chip corner stress relief pattern and seal ring structures are based on 1P12M process:

*CSRDMDY is a dummy layer aligned to the boundary of stress relief pattern in region for DRC. Please refer to Fig. 4.5.71.4.2. in the following.

*Please be careful with the non-generic logical operation, CAD bias, and shrinkage effects on the drawn dimensions of stress relief pattern and seal ring.

* Dummy metal/via is implemented in no pattern area to strengthen CSR structure. Please follow the sample gds file and use correct CAD layers with correct data types for DMV at CSR area.

* Seal ring is surrounded by 7.2 μm scribe line dummy bar to enhance die saw quality against laser and mechanical die saw alike for wider package reliability margin. Please refer to scribe line dummy bar layout rule in Section 2.5.

* The seal ring wall structure includes the outer and inner seal ring walls with 1.8um and 5.4um region, respectively. The outer seal ring is designed for railing-like and adjacent to scribe line; the inner seal ring is also designed for railing-like and far away from scribe line. Please refer to Fig. 2.5.1.1. for an example.

For wire bond product,

* PM (mask code 009, CAD layer: 5;0).

* Polyimide only covers inner seal ring. Please refer to Fig. 2.5.1.1. for the details.

For flip-chip product,

* Polyimide only covers inner seal ring. Please refer to Fig. 2.5.1.1. for the details.

* CBD (mask code 306) layout is same as CB.

*** Do not draw UBM (mask code 020) layout on the seal ring (chip corner stress relief pattern, seal ring wall, and seal ring enhanced zone (SREZ)) and SLDB. No UBM metal is left on these regions.**

* AP (mask 309) must be drawn on seal ring according to the rules.

Chip Corner Stress Relief Pattern (Fig. 4.5.71.4.2)

Scribe line dummy bar is not drawn in this figure.

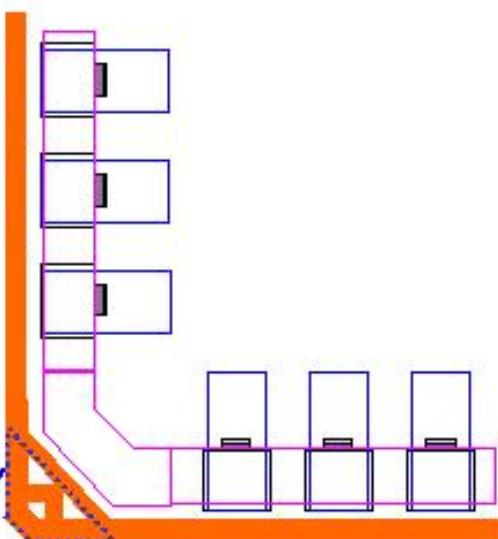
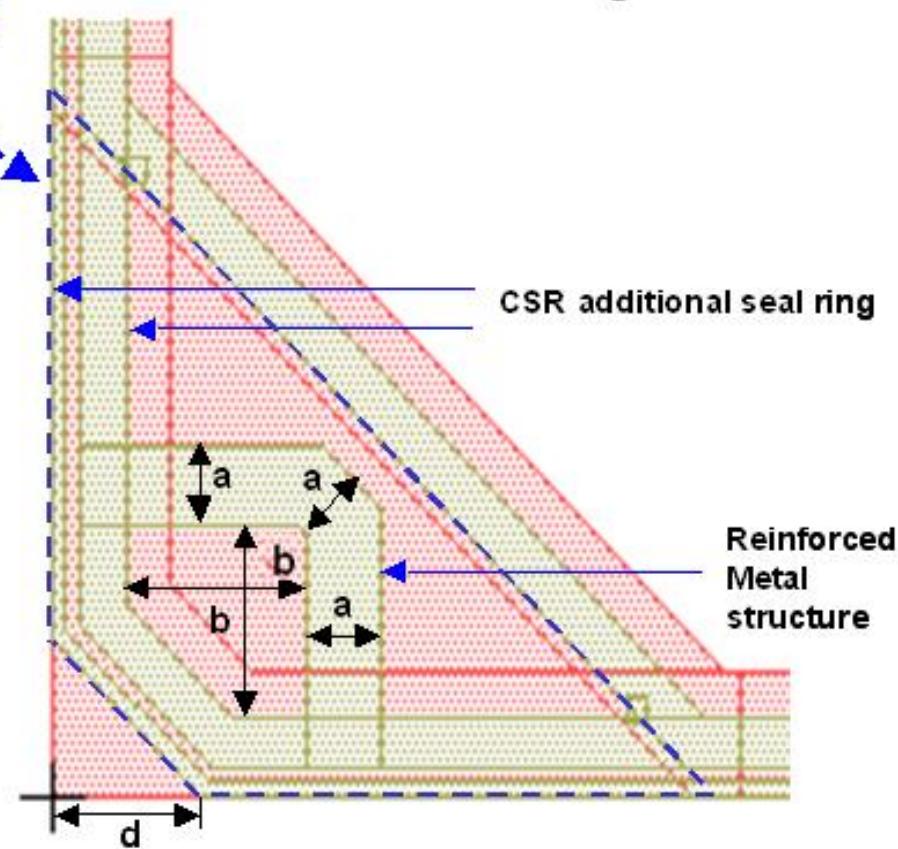
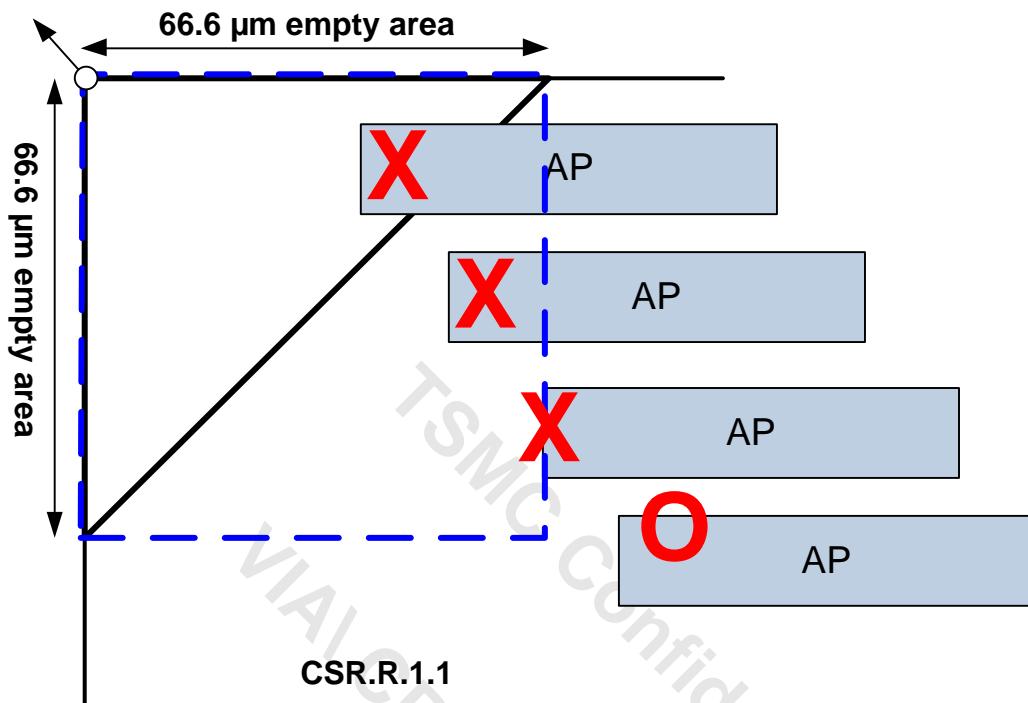


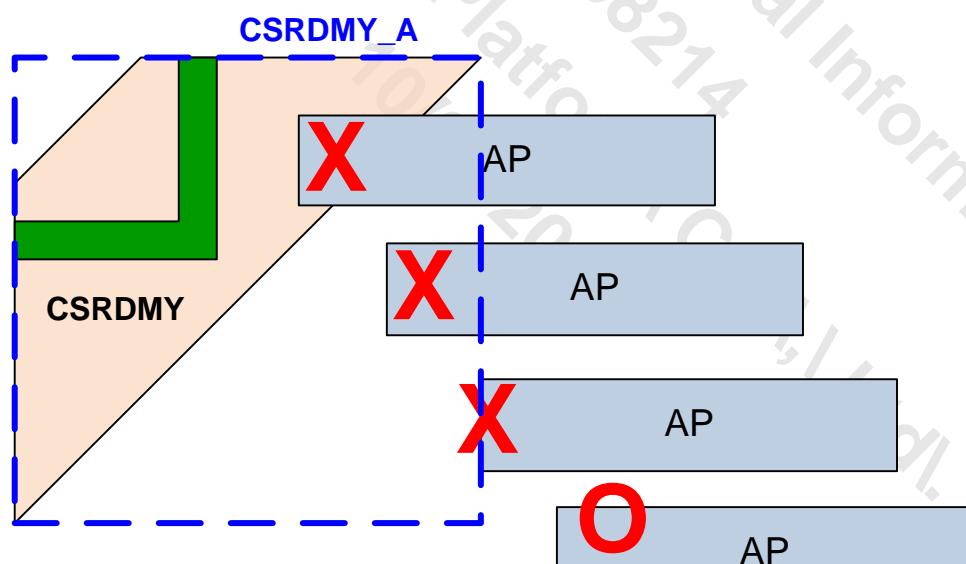
Fig. 2.4.2



Chip corner



CSR.R.1.1



CSR.R.6

Chip Corner Stress Relief pattern (Fig. 4.5.71.4.3)

Chip corner stress relief pattern can reduce the impact of damage induced by thermal stress during packaging and field application. Please refer to region I as an example.

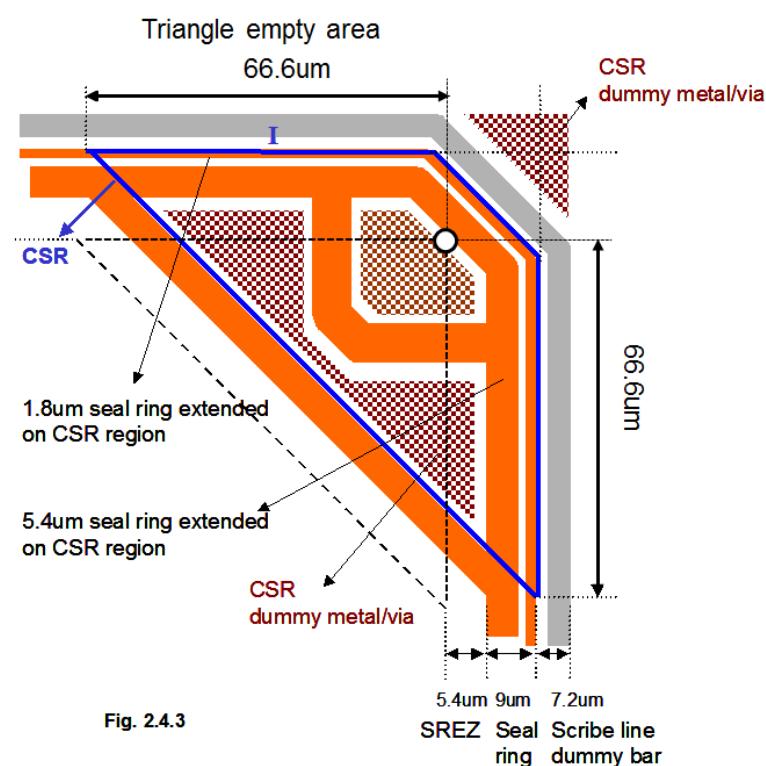
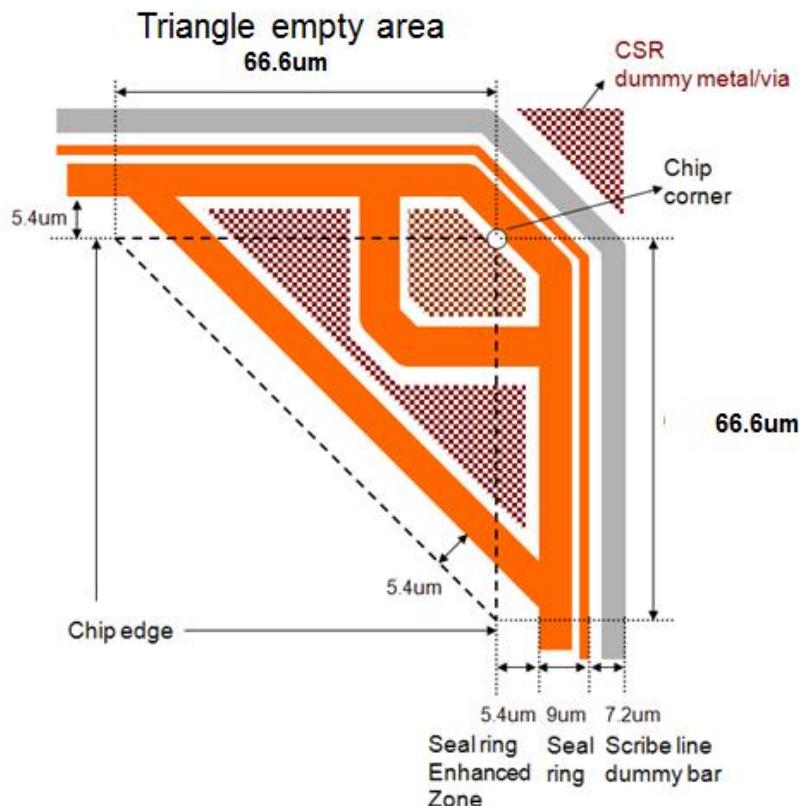


Fig. 2.4.3

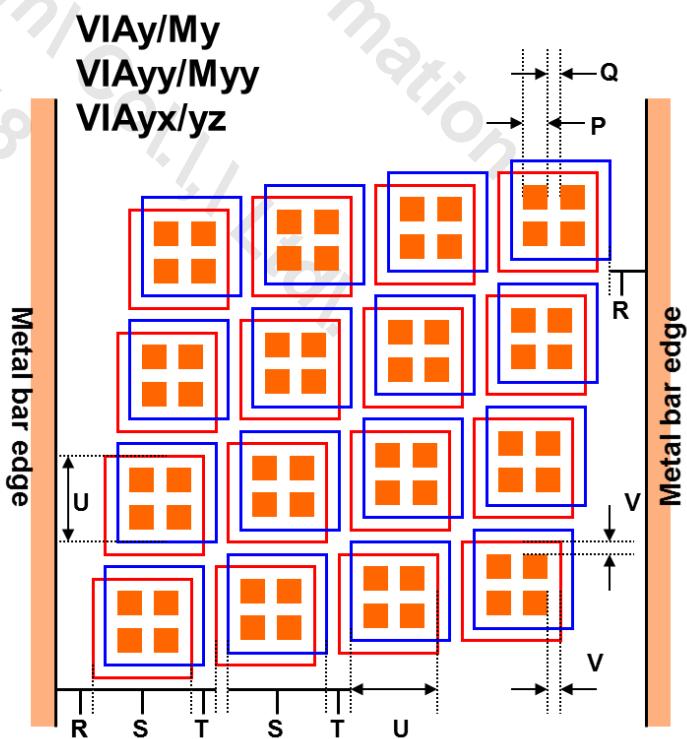
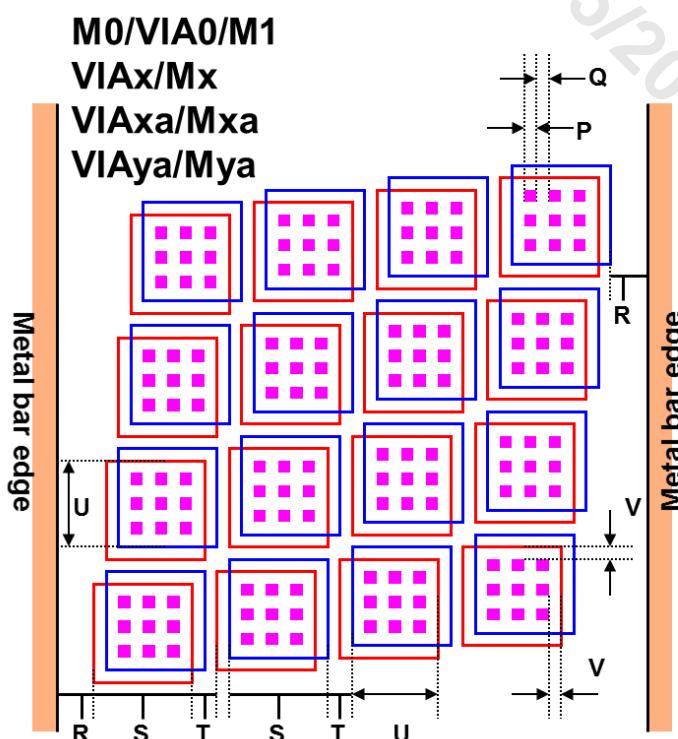
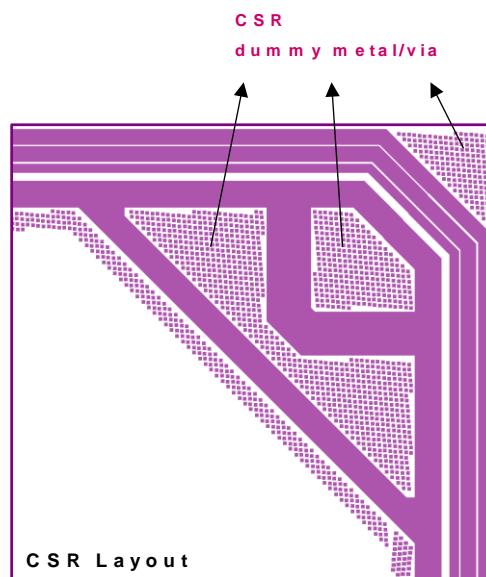
Dummy metal/via (DMV) in CSR region (Fig. 4.5.71.4.4)

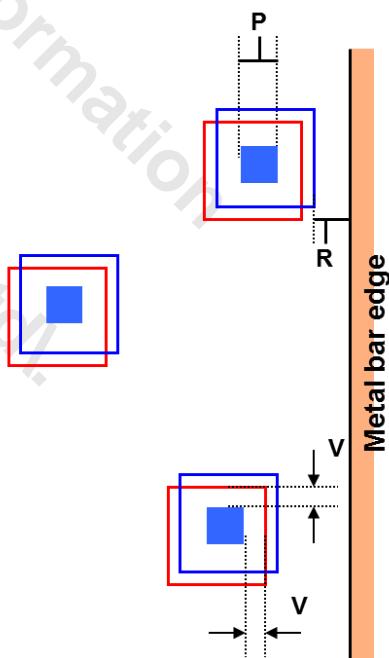
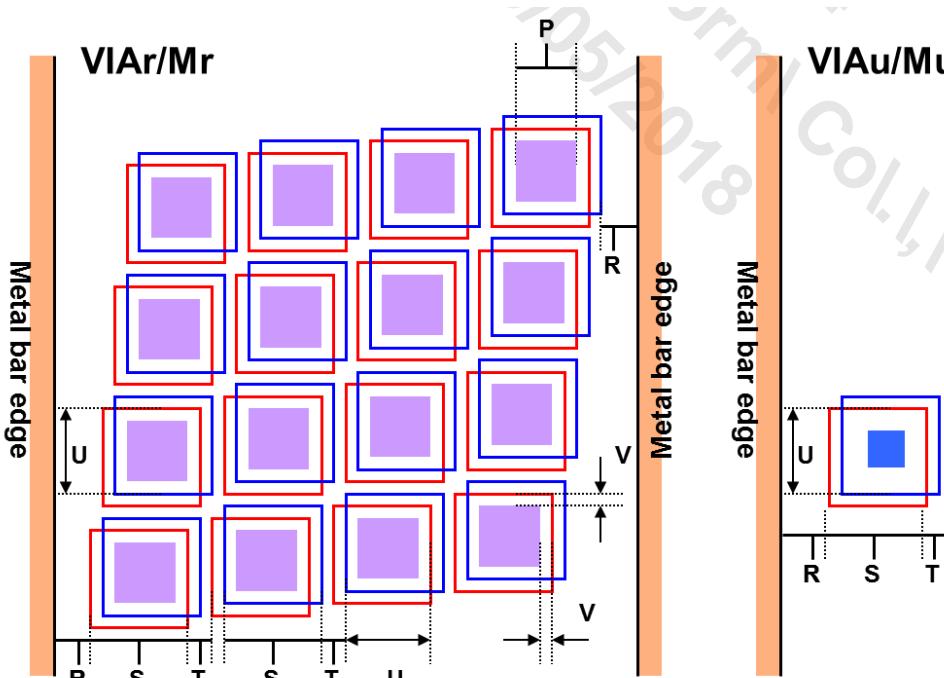
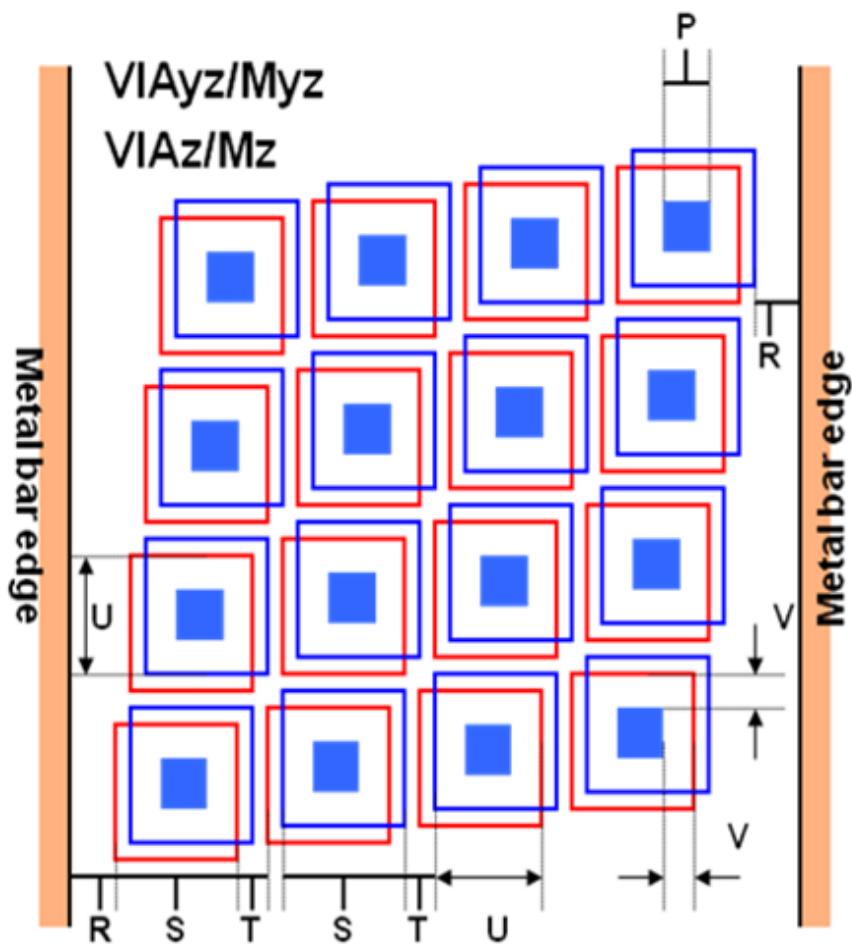
Table. 4.5.71.4.1 Rule summary of DMV in CSR for items P~V.

Label	P	Q	R	S	T	U	V
M0	-	-	0.45	0.72	0.36	0.63	-
VIA0	0.020	0.044	0.45	0.72	0.36	0.63	0.020
M1	-	-	0.45	0.72	0.36	0.63	-
VIAxs/Mxs	0.020	0.044	0.45	0.72	0.36	0.63	0.020
VIAx/Mx	0.020	0.044	0.45	0.72	0.36	0.63	0.020
VIAxa/Mxa	0.020	0.094	0.45	0.72	0.36	0.63	0.02
VIAya/Mya	0.020	0.094	0.45	0.72	0.36	0.63	0.020
VIAy/My	0.038	0.077	0.45	0.72	0.36	0.63	0.020
VIAyy/Myy	0.062	0.099	0.45	0.72	0.36	0.63	0.027
VIAyx/Myx	0.126	0.144	0.45	0.72	0.36	0.63	0.041
VIAyz/Myz	0.18	0.486	0.45	0.72	0.36	0.63	0.072
VIAz/Mz	0.324	0.486	0.45	0.72	0.36	0.63	0.072
VIAr/Mr	0.414	0.594	1.35	0.9	0.45	0.81	0.072

* Recommended value, DRC doesn't check.

(DRC tolerance at 45-degree turning: ± 0.010)





4.5.72.5 Seal Ring Layout Rules

The seal ring wall rules, and DMV (dummy metal/via) in seal ring enhanced zone (SREZ) rules are described in this section.

Please follow exactly the schematic diagram below (as in the GDS example) for seal ring layout. Now, DRC clean does not mean the new design structure is accepted. If you do not use these dimensions as below, please consult with TSMC. Any seal ring design different from TSMC standard offer cannot be accepted in product tape out due to unknown risk for die saw and packaging. Please contact TSMC for a special approval of non-TSMC standard seal ring.

In the following figures, the 5.4 μm measure for seal ring enhanced zone (SREZ) is for reference only. Seal ring enhanced zone (SREZ) depends on the capability of assembly house. If the seal ring is added by TSMC, TSMC will add seal ring enhanced zone (SREZ) and seal ring structure at the same time.

Only DMV is allowed in seal ring enhanced zone (SREZ) region. Please use the sample gds file for DMV and follow the DMV rules in this region.

AICu pad (AP) can be generated by logic operation for wire-bond non-RDL products.

4.5.72.5.1 Seal Ring Wall Layout Rules

The seal ring wall structure includes the outer and inner seal ring walls with 1.8um and 5.4um region, respectively. The outer seal ring is designed for railing-like and adjacent to scribe line; the inner seal ring is also designed for railing-like and far away from scribe line. Please refer to Fig. 2.5.1.1. for example.

Rule No.	Description	Label	Op.	Rule
SR.R.1	SEALRING layer (CAD layer: 162;0) SEALRING_DB layer (CAD layer: 162;1) and SEALRING_ALL layer (162;2) are Must if customers add seal ring by themselves. 162;0 is used to cover the outer seal ring (1.8 μm) and inner seal ring (5.4 μm);162;1 is used to cover SLDB (3.15 μm duplicate); 162;2 is used to cover SEALRING region, SLDB, CSR, and seal ring enhanced zone (SREZ). SEALRING layer (162;0), SEALRING_DB layer (162;1), and SEALRING_ALL layer (162;2) must exist. All the drawing of seal ring wall and SLDB structures must be inside of SEALRING (162;0) and SEALRING_DB (162;1). (Except AP) DMV structure and reinforced metal structure in CSR must be inside of SEALRING_ALL (162;2) Please follow the CAD layers usage of 162;0, 162;1 and 162;2. DRC does not check seal ring related rules w/o those layers.			
SR.R.7	SR_DMD bar, VC bar, all VIA bar and CB/CBD/RV must be continuous as a ring.(except inner sealring NOT INTERACT csdmy)			
SR.R.8 ^U	Only tsmc standard seal-ring is allowed.			
SR.R.9	SEALRING_ALL must interact OD_DA, COD_H, COD_V, COD_BLOCK, PO_MM, WPOM, POMMB, SR_DMD, VC			
SR.R.10	Width of seal-ring enhanced zone (SREZ) = 5.4 μm (layout forbidden area.) Only M1~AP and DMV pattern are allowed in seal-ring enhanced zone region. (DMV pattern: metal/via dummy pattern, SR_DOD,OD_DA, COD_H, COD_V, SR_DPO, SR_DMD,) Each M1~AP patterns in seal-ring enhanced zone region must follow the following conditions:			

Rule No.	Description	Label	Op.	Rule
	1. Each M1~Mtop must be connected to seal ring wall, and 2. Each AP can only connect to the inner seal ring wall, and 3. Each M1~AP overlap SLDB is not allowed			
SR.SR_DMD.W.3	Width of SR_DMD bar in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	A	=	0.1000
SR.SR_DMD.O.1	SR_DMD bar overlap OD_DA in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	B	=	0.0390
SR.SR_DMD.R.1	SR_DMD must overlap with OD_DA in {SEALRING_ALL NOT SEALRING_EN}			
SR.VC.W.3	Width of VC bar in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	A1	=	0.0800
SR.VC.EN.1	VC bar enclosure by SR_DMD bar in {SEALRING_ALL NOT SEALRING_EN} (DRC tolerance at 45-degree turning: $\pm 0.005 \mu\text{m}$)	B1	=	0.0100
SR.VC.R.1	VC bar must fully inside SR_DMD in {SEALRING_ALL NOT SEALRING_EN}			
SR.M0.W.6	Width of 45-degree bent M0 in seal ring (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q1	\geq	0.4000
SR.M0.W.7	Width of M0 metal line in seal ring. (Except CSRDMY region) (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q	\leq	1.0
SR.M0.S.1	Minimum space of M0 between M0 metal bars in the direction parallel/ vertical to chip edge in seal ring.	C	\geq	0.4000
SR.M0.S.2	Space of M0 between M0 metal bars in the direction parallel to chip edge between the same metal bars in seal ring.	L	\geq	2.5
SR.VIA0.W.2	Width of VIA0 bar in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)		=	0.1400
SR.VIA0.W.3	Width of VIA0 hole in seal ring.		=	0.0200
SR.VIA0.S.1	Space of VIA0 in seal ring.		\geq	0.0200
SR.VIA0.EN.25	Enclosure of VIA0 bar by M0 in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)		\leq	0.1500
SR.VIA0.EN.26	Enclosure of VIA0 hole by M0 in seal ring.		\geq	0.0200
SR.M1.W.6	Width of 45-degree bent M1 in seal ring (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q1	\geq	0.4000
SR.M1.W.7	Width of M1 metal line in seal ring. (Except CSRDMY region) (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q	\leq	1.0
SR.M1.S.1	Minimum space of M1 between M1 metal bars in the direction parallel/ vertical to chip edge in seal ring.	C	\geq	0.4000
SR.M1.S.2	Space of M1 between M1 metal bars in the direction parallel to chip edge between the same metal bars in seal ring.	L	\geq	2.5
SR.VIAxs.W.2	Width of VIAxs bar in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D	=	0.1400
SR.VIAxs.W.3	Width of VIAxs hole in seal ring.	D1	=	0.0200
SR.VIAxs.EN.25	Enclosure of VIAxs bar by Mxs in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	I	\geq	0.1500
SR.VIAxs.EN.26	Enclosure of VIAxs hole by Mxs in seal ring.	I1	\geq	0.0200
SR.VIAxs.S.1	Maximum space of VIAxs hole [INSIDE SEALRING] DRC flags: {SEALRING AND Mxs} must be fully covered by {{SEALRING AND VIAxs holes} SIZING 3.5 μm }	G	\leq	7
SR.VIAxs.S.24	Space of Vlxsx hole in seal ring	G	\geq	0.0440
SR.VIAxs.S.25	Space of VIAxs hole to VIAxs bar in seal ring.	H	\geq	0.3500
SR.Mxs.W.6	Width of 45-degree bent Mxs in seal ring (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q1	\geq	0.4000
SR.Mxs.W.7	Width of Mxs metal line in seal ring. (Except CSRDMY region) (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q	\leq	1.0
SR.Mxs.S.1	Minimum space of Mxs between Mxs metal bars in the direction parallel/ vertical to chip edge in seal ring	C	\geq	0.4000

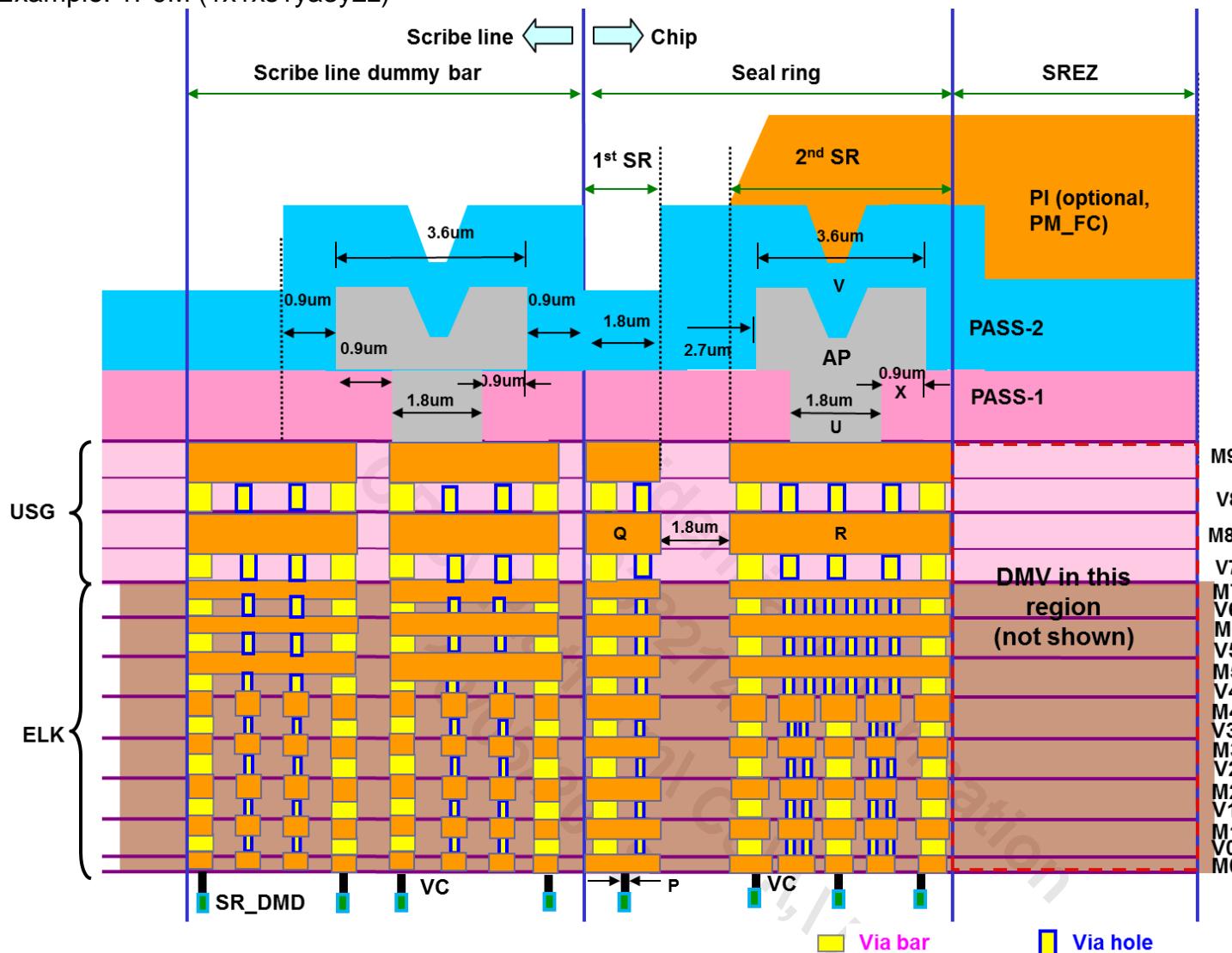
Rule No.	Description	Label	Op.	Rule
SR.Mxs.S.2	Space of Mxs between Mxs metal bars in the direction parallel to chip edge between the same metal bars in seal ring	L	\geq	2.5
SR.VIAx.W.2	Width of VIAx bar in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	D	=	0.1400
SR.VIAx.W.3	Width of VIAx hole in seal ring.	D1	=	0.0200
SR.VIAx.EN.25	Enclosure of VIAx bar by Mx in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	I	\geq	0.1500
SR.VIAx.EN.26	Enclosure of VIAx hole by Mx in seal ring.	I1	\geq	0.0200
SR.VIAx.S.1	Maximum space of VIAx hole [INSIDE SEALRING] DRC flags: {SEALRING AND Mx} must be fully covered by {{SEALRING AND VIAx holes} SIZING 3.5 μm }	G	\leq	7
SR.VIAx.S.24	Space of VIAx hole in seal ring	G	\geq	0.0440
SR.VIAx.S.25	Space of VIAx hole to VIAx bar in seal ring.	H	\geq	0.3500
SR.Mx.W.6	Width of 45-degree bent Mx in seal ring (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	Q1	\geq	0.4000
SR.Mx.W.7	Width of Mx metal line in seal ring. (Except CSRDMDY region) (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	Q	\leq	1.0
SR.Mx.S.1	Minimum space of Mx between Mx metal bars in the direction parallel/ vertical to chip edge in seal ring	C	\geq	0.4000
SR.Mx.S.2	Space of Mx between Mx metal bars in the direction parallel to chip edge between the same metal bars in seal ring	L	\geq	2.5
SR.VIAXa.W.2	Width of VIAXa bar in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	D	=	0.1400
SR.VIAXa.W.3	Width of VIAXa hole in seal ring.	D1	=	0.0200
SR.VIAXa.EN.25	Enclosure of VIAXa bar by Mxa in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	I	\geq	0.1500
SR.VIAXa.EN.26	Enclosure of VIAXa hole by Mxa in seal ring.	I1	\geq	0.0200
SR.VIAXa.S.1	Maximum space of VIAXa hole [INSIDE SEALRING] DRC flags: {SEALRING AND Mxa} must be fully covered by {{SEALRING AND VIAXa holes} SIZING 3.5 μm }	G	\leq	7
SR.VIAXa.S.24	Space of VIAXa hole in seal ring.	G	\geq	0.0940
SR.VIAXa.S.25	Space of VIAXa hole to VIAXa bar in seal ring.	H	\geq	0.3500
SR.Mxa.W.6	Width of 45-degree bent Mxa in seal ring (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	Q1	\geq	0.4000
SR.Mxa.W.4	Width of Mxa metal line in seal ring. (Except CSRDMDY region) (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	Q	\leq	1.0
SR.Mxa.S.1	Minimum space of Mxa between Mxa metal bars in the direction parallel/ vertical to chip edge in seal ring	C	\geq	0.4000
SR.Mxa.S.2	Space of Mxa between Mxa metal bars in the direction parallel to chip edge between the same metal bars in seal ring	L	\geq	2.5
SR.VIAYa.W.2	Width of VIAYa bar in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	D	=	0.1400
SR.VIAYa.W.3	Width of VIAYa hole in seal ring.	D1	=	0.0200
SR.VIAYa.EN.25	Enclosure of VIAYa bar by Mya in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	I	\geq	0.1500
SR.VIAYa.EN.26	Enclosure of VIAYa hole by Mya in seal ring.	I1	\geq	0.0200
SR.VIAYa.S.1	Maximum space of VIAYa hole [INSIDE SEALRING] DRC flags: {SEALRING AND Mya} must be fully covered by {{SEALRING AND VIAYa holes} SIZING 3.5 μm }	G	\leq	7
SR.VIAYa.S.24	Space of VIAYa hole in seal ring.	G	\geq	0.0940
SR.VIAYa.S.25	Space of VIAYa hole to VIAYa bar in seal ring.	H	\geq	0.3500
SR.My.W.6	Width of 45-degree bent Mya in seal ring (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	Q1	\geq	0.4000
SR.My.W.7	Width of Mya metal line in seal ring. (Except CSRDMDY region) (DRC tolerance at 45-degree turning: $\pm 0.020 \mu m$)	Q	\leq	1.0

Rule No.	Description	Label	Op.	Rule
SR.MyA.S.1	Minimum space of Mya between Mya metal bars in the direction parallel/vertical to chip edge in seal ring	C	≥	0.4000
SR.MyA.S.2	Space of Mya between Mya metal bars in the direction parallel to chip edge between the same metal bars in seal ring	L	≥	2.5
SR.VIAy.W.2	Width of VIAy bar in seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	D2	=	0.4500
SR.VIAy.W.3	Width of VIAy hole in seal ring.	D4	=	0.0380
SR.VIAy.EN.5	Enclosure of VIAy bar by My in seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	I4	≥	0.1900
SR.VIAy.EN.6	Enclosure of VIAy hole by My in seal ring.	I5	≥	0.0200
SR.VIAy.S.1	Maximum space of VIAy hole [INSIDE SEALRING] DRC flags: {SEALRING AND My} must be fully covered by {{SEALRING AND VIAy holes} SIZING 3.5 μm}	G2	≤	7
SR.VIAy.S.4	Space of VIAy hole in seal ring.	G2	≥	0.0760
SR.VIAy.S.5	Space of VIAy hole to VIAy bar in seal ring.	H2	≥	0.3500
SR.My.W.4	Width of My metal line in outer seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	Q2	=	1.8
SR.My.W.5	Width of My metal line in inner seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	Q3	=	5.4
SR.VIAyy.W.2	Width of VIAyy bar in seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	D2	=	0.4500
SR.VIAyy.W.3	Width of VIAyy hole in seal ring.	D4	=	0.0620
SR.VIAyy.EN.5	Enclosure of VIAyy bar by Myy in seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	I4	≥	0.1900
SR.VIAyy.EN.6	Enclosure of VIAyy hole by Myy in seal ring.	I5	≥	0.0360
SR.VIAyy.S.1	Maximum space of VIAyy hole [INSIDE SEALRING] DRC flags: {SEALRING AND Myy} must be fully covered by {{SEALRING AND VIAyy holes} SIZING 3.5 μm}	G2	≤	7
SR.VIAyy.S.4	Space of VIAyy hole in seal ring.	G2	≥	0.0640
SR.VIAyy.S.5	Space of VIAyy hole to VIAyy bar in seal ring.	H2	≥	0.3500
SR.My.W.4	Width of Myy metal line in outer seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	Q2	=	1.8
SR.My.W.5	Width of Myy metal line in inner seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	Q3	=	5.4
SR.VIAyx.W.2	Width of VIAyx bar in seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	D2	=	0.4500
SR.VIAyx.W.3	Width of VIAyx hole in seal ring.	D4	=	0.1260
SR.VIAyx.EN.5	Enclosure of VIAyx bar by Myx in seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	I4	≥	0.1900
SR.VIAyx.EN.6	Enclosure of VIAyx hole by Myx in seal ring.	I5	≥	0.0410
SR.VIAyx.S.1	Maximum space of VIAyx hole [INSIDE SEALRING] DRC flags: {SEALRING AND Myx} must be fully covered by {{SEALRING AND VIAyx holes} SIZING 3.5 μm}	G2	≤	7
SR.VIAyx.S.4	Space of VIAyx hole in seal ring.	G2	≥	0.1440
SR.VIAyx.S.5	Space of VIAyx hole to VIAyy bar in seal ring.	H2	≥	0.3500
SR.My.W.4	Width of Myx metal line in outer seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	Q2	=	1.8
SR.My.W.5	Width of Myx metal line in inner seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	Q3	=	5.4
SR.VIAyz.W.2	Width of VIAyz bar in seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	D2	=	0.4500
SR.VIAyz.W.3	Width of VIAyz hole in seal ring.	D4	=	0.1800
SR.VIAyz.EN.5	Enclosure of VIAyz bar by Myz in seal ring. (DRC tolerance at 45-degree turning: ± 0.020 μm)	I4	≥	0.1900
SR.VIAyz.EN.6	Enclosure of VIAyz hole by Myz in seal ring.	I5	≥	0.0720

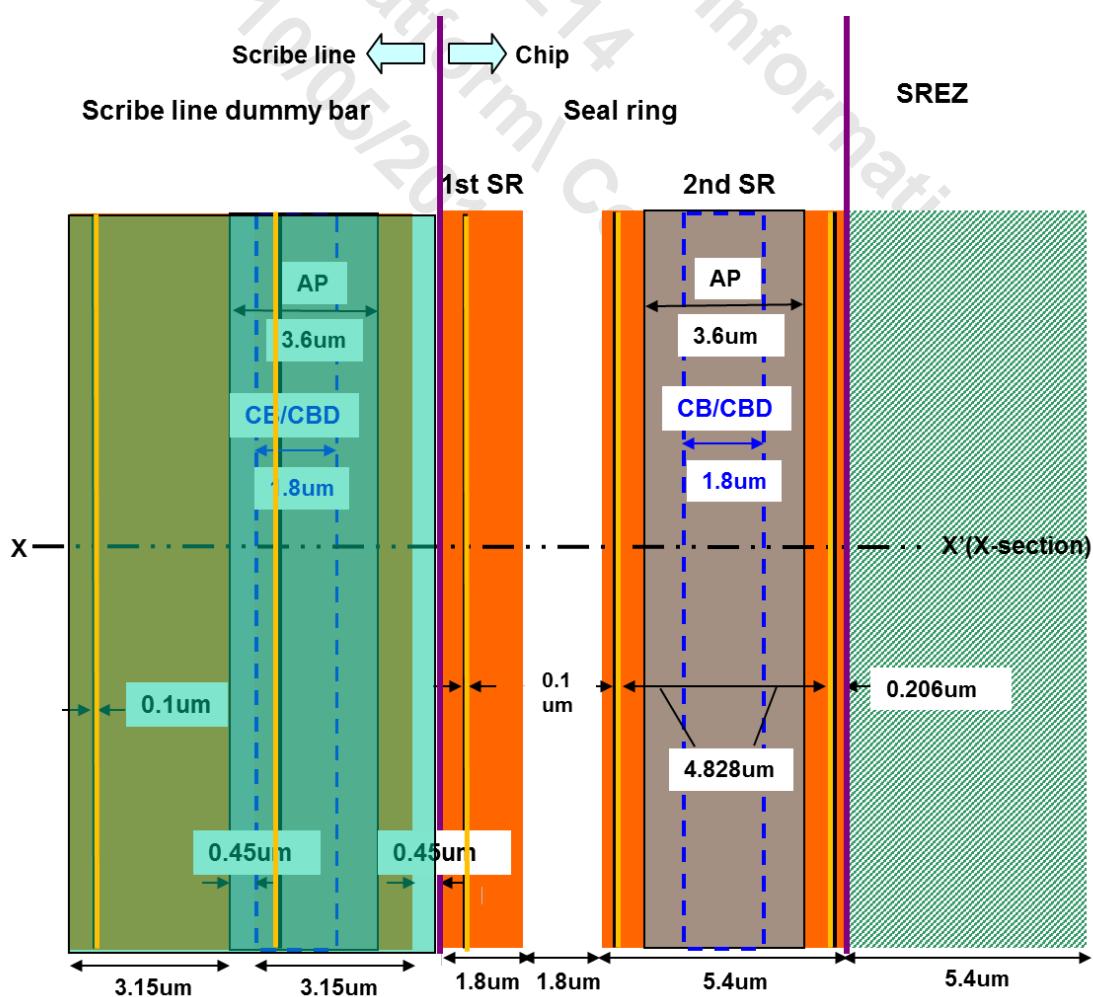
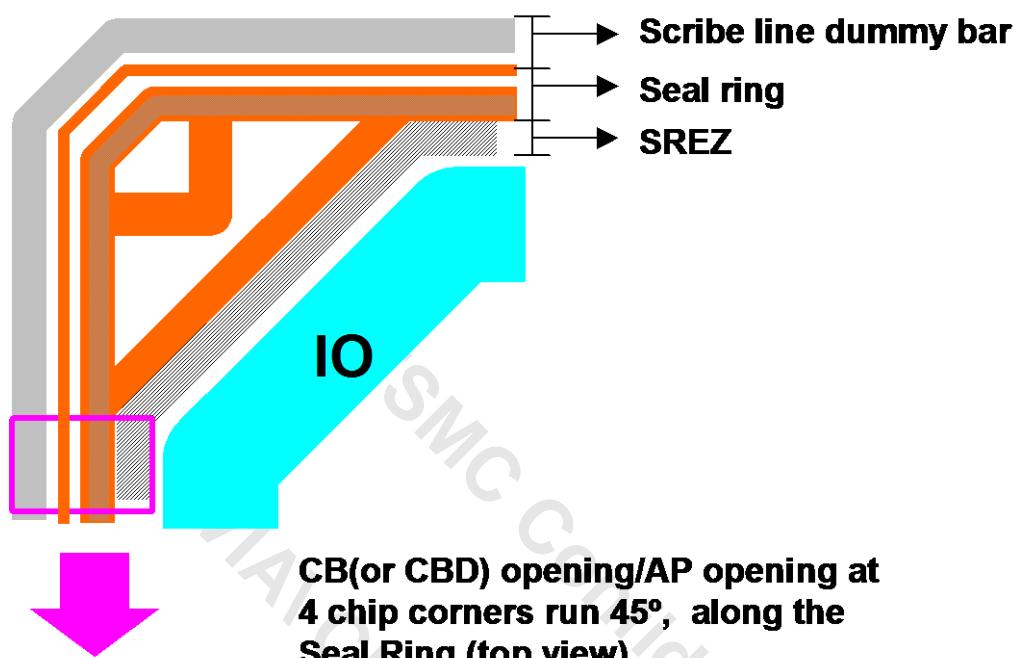
Rule No.	Description	Label	Op.	Rule
SR.VIAyz.S.1	Maximum space of VIAyz hole [INSIDE SEALRING] DRC flags: {SEALRING AND Myz} must be fully covered by {{SEALRING AND VIAyz holes} SIZING 3.5 μm }	G2	\leq	7
SR.VIAyz.S.4	Space of VIAyz hole in seal ring.	G2	\geq	0.2250
SR.VIAyz.S.5	Space of VIAyz hole to VIAyz bar in seal ring.	H2	\geq	0.3500
SR.Myz.W.4	Width of Myz metal line in outer seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q2	$=$	1.8
SR.Myz.W.5	Width of Myz metal line in inner seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q3	$=$	5.4
SR.VIAz.W.2	Width of VIAz bar in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D2	$=$	0.4500
SR.VIAz.W.3	Width of VIAz hole in seal ring.	D4	$=$	0.3240
SR.VIAz.EN.5	Enclosure of VIAz bar by Mz in seal ring (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	I4	\geq	0.1900
SR.VIAz.EN.6	Enclosure of VIAz hole by Mz in seal ring.	I5	\geq	0.0720
SR.VIAz.S.1	Maximum space of VIAz hole [INSIDE SEALRING] DRC flags: {SEALRING AND Mz} must be fully covered by {{SEALRING AND VIAz holes} SIZING 3.5 μm }	G2	\leq	7
SR.VIAz.S.4	Space of VIAz hole in seal ring.	G2	\geq	0.4860
SR.VIAz.S.5	Space of VIAz hole to VIAz bar in seal ring.	H2	\geq	0.3500
SR.Mz.W.4	Width of Mz metal line in outer seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q2	$=$	1.8
SR.Mz.W.5	Width of Mz metal line in inner seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q3	$=$	5.4
SR.VIAr.W.2	Width of VIAr bar in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D2	$=$	0.4500
SR.VIAr.W.3	Width of VIAr hole in seal ring.	D4	$=$	0.4140
SR.VIAr.EN.5	Enclosure of VIAr bar by Mr in seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	I4	\geq	0.0720
SR.VIAr.EN.6	Enclosure of VIAr hole by Mr in seal ring.	I5	\geq	0.0720
SR.VIAr.S.1	Maximum space of VIAr hole [INSIDE SEALRING] DRC flags: {SEALRING AND Mr} must be fully covered by {{SEALRING AND VIAr holes} SIZING 3.5 μm }	G2	\leq	7
SR.VIAr.S.4	Space of VIAr hole in seal ring.	G2	\geq	0.3960
SR.VIAr.S.5	Space of VIAr hole to VIAr bar in seal ring.	H2	\geq	0.3500
SR.Mr.W.4	Width of Mr metal line in outer seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q2	$=$	1.8
SR.Mr.W.5	Width of Mr metal line in inner seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	Q3	$=$	5.4
SR.CB.W.3	Width of CB/CBD/RV line opening in inner seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	U	$=$	1.8
SR.CB.EN.2	Enclosure of CB/CBD/RV by AP in seal ring	X	\geq	0.8900
SR.AP.W.3	Width of AP bar in inner seal ring. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	V	$=$	7.2
SR.PM.R.3	Polyimide is prohibited over outer seal ring and SLDB regions. It only covers inner seal ring area (5.4 μm). Please see Fig. 4.5.71.5.1.1. (PM drawn pattern must cover outer seal ring and SLDB regions.)			
SR.R.4	Please add VIA holes in metal lines of inner and outer seal ring as many as possible.			

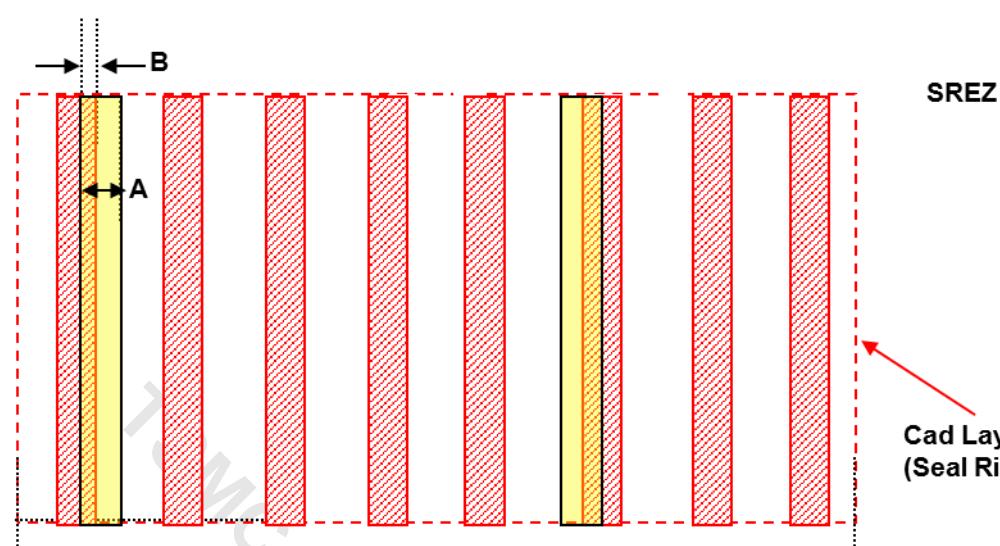
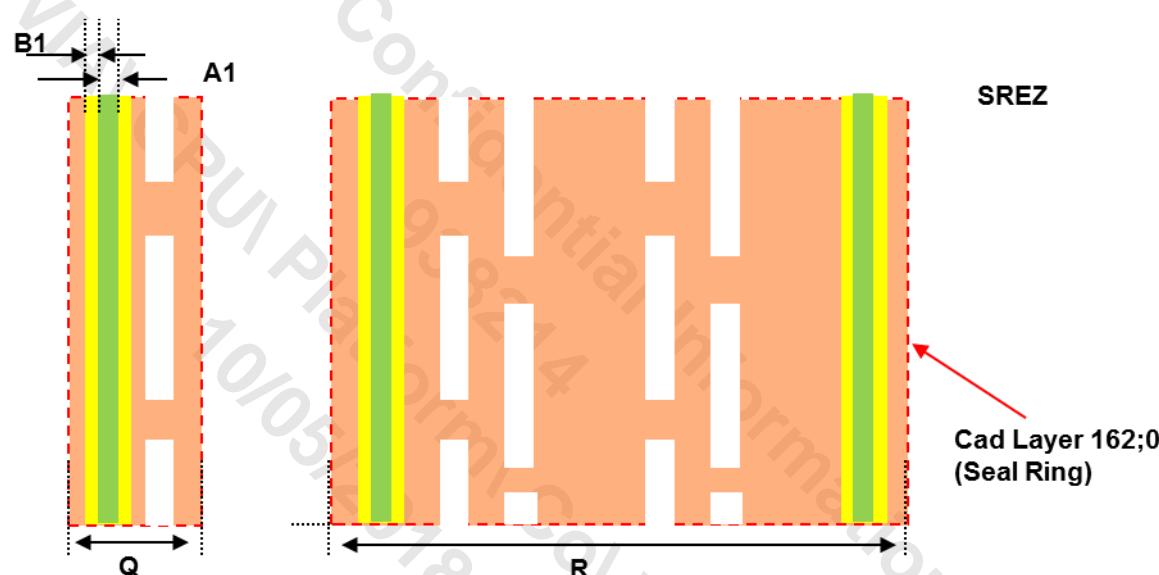
Fig. 4.5.71.5.1.1. Cross-sectional view of seal ring wall

Example: 1P9M (1x1xs1ya3y2z)

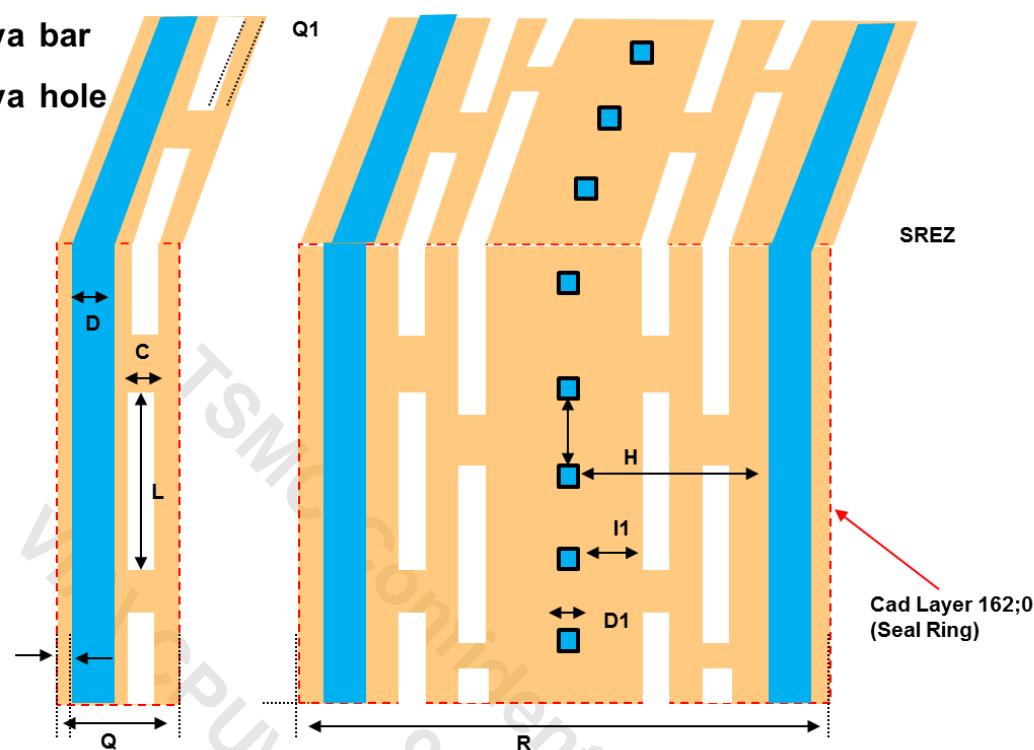


Top view of seal ring

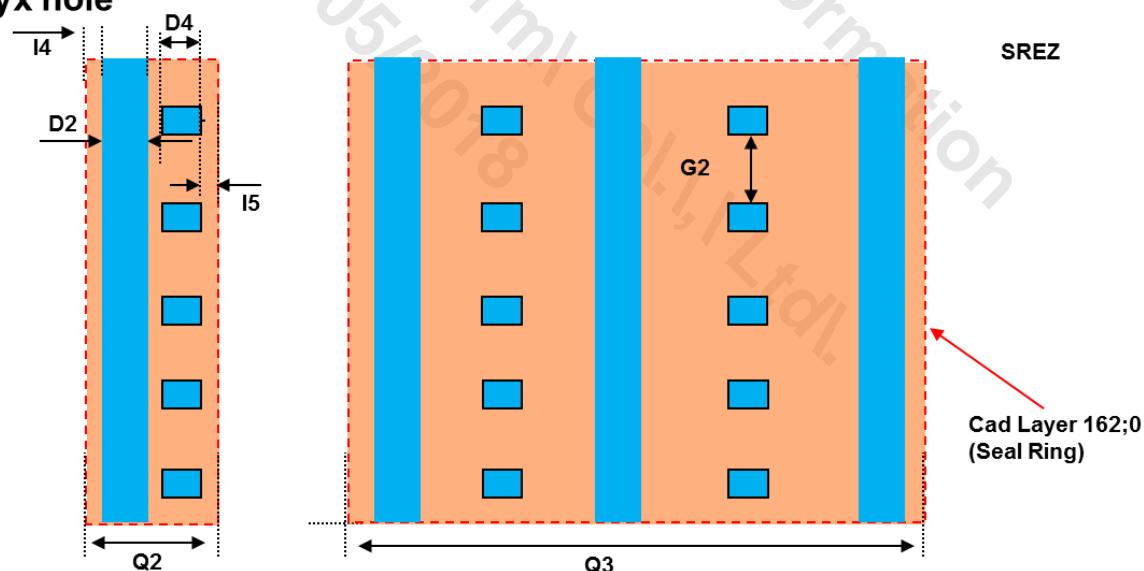


OD_DA **SR_DMD** **SR_DMD** **VC** **Metal** 

- M0/M1/Mx/Mxa/Mya
- Via0/Vx/Vxa/Vya bar
- Via0/Vx/Vxa/Vya hole



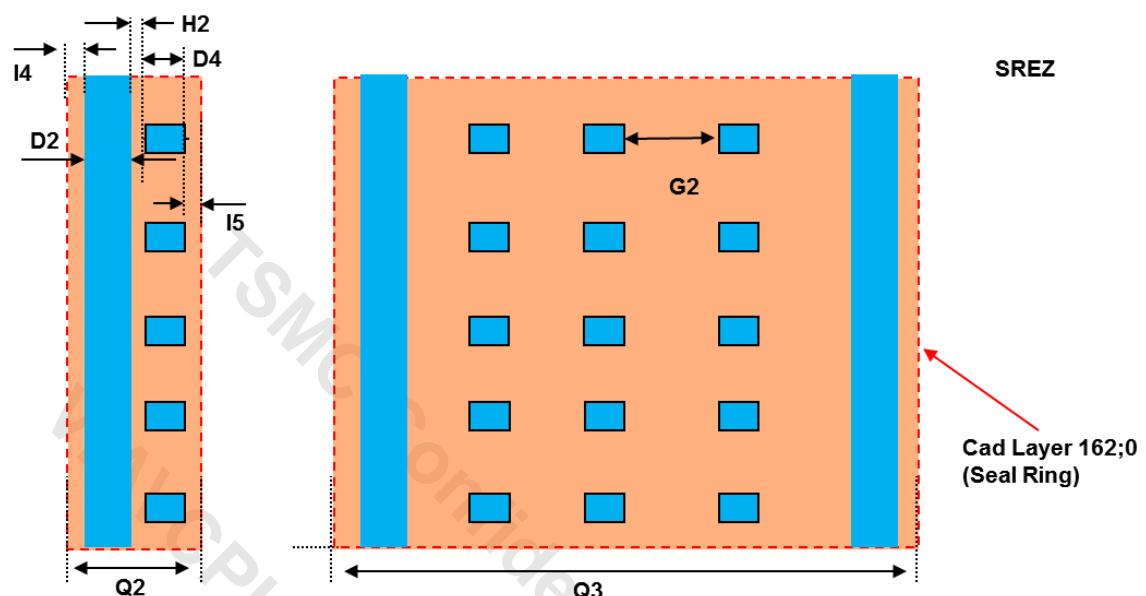
- My/Myy/Myx
- Vy/Vyy/Vyx bar
- Vy/Vyy/Vyx hole



■ Myz/Mz/Mr/Mu

■ Vyz/Vz/Vr/Vu bar

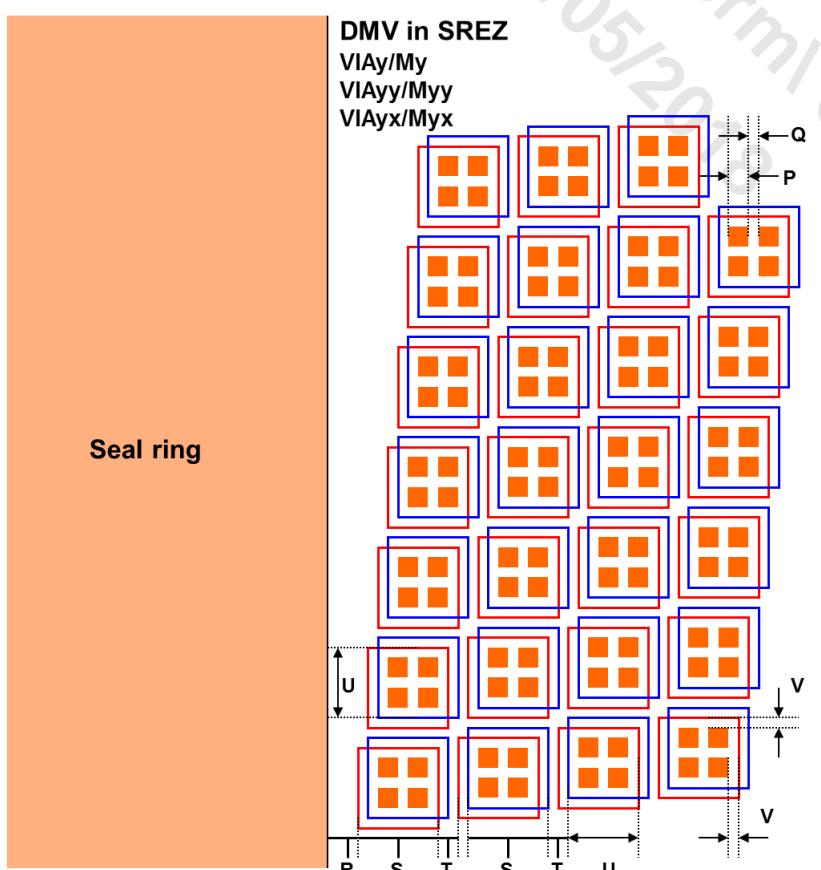
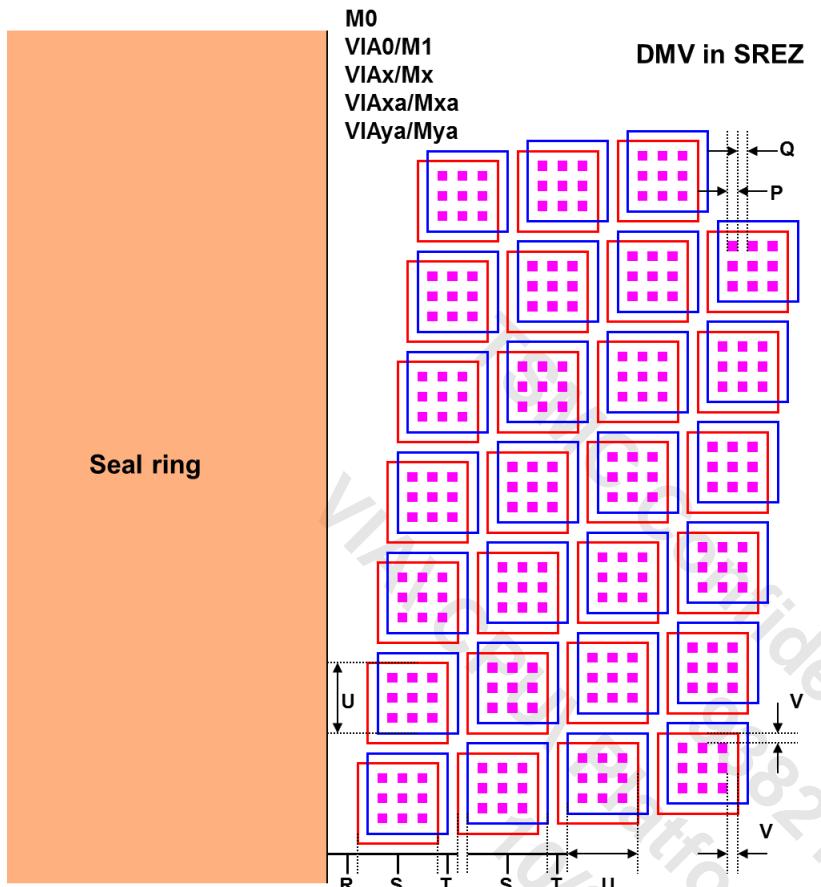
■ Vyz/Vz/Vr/Vu hole



4.5.72.5.2 Dummy metal/via (DMV) in Seal ring enhanced zone (SREZ) Layout Rules

Rule No.	Description	Label	Op.	Rule
SR.DM.W.1	Metal width of DMV in seal ring enhanced zone (SREZ)	S	=	Table. 4.5.71.5.2.1
SR.DM.S.1	Metal space of DMV in seal ring enhanced zone (SREZ)	T	\geq	Table. 4.5.71.5.2.1
SR.DM.S.2	Metal space of DMV to seal ring metal bar	R	\geq	Table. 4.5.71.5.2.1
SR.DM.O.1	Overlay of two adjacent DMV metal layers, except Mr	U	=	Table. 4.5.71.5.2.1
SR.DV.W.1	Via width of DMV in seal ring enhanced zone (SREZ)	P	=	Table. 4.5.71.5.2.1
SR.DV.S.1	Via space of DMV in seal ring enhanced zone (SREZ)	Q	\geq	Table. 4.5.71.5.2.1
SR.DV.EN.1	Enclosure of DMV via by DMV metal in seal ring enhanced zone (SREZ) DMV via must be inside DMV metal.	V	\geq	Table. 4.5.71.5.2.1
SR.R.2	DMV pattern in seal ring enhanced zone (SREZ) region must include Mtop/VIAtop/ Mtop-1/VIAtop-1/Mtop-2/VIAtop-2/.../V1/M1. (DMV pattern: metal/via dummy pattern)			

Top view of DMV in seal ring enhanced zone (SREZ)



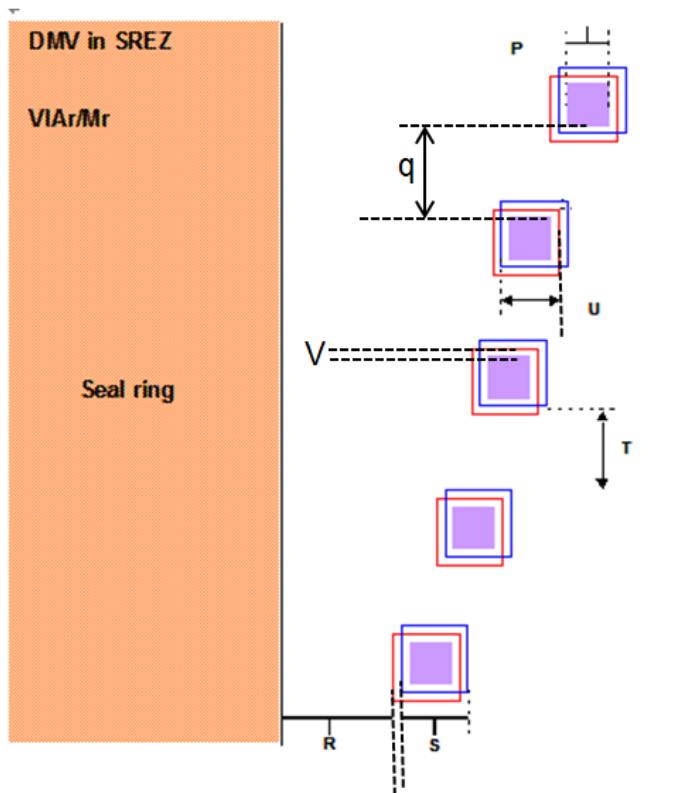
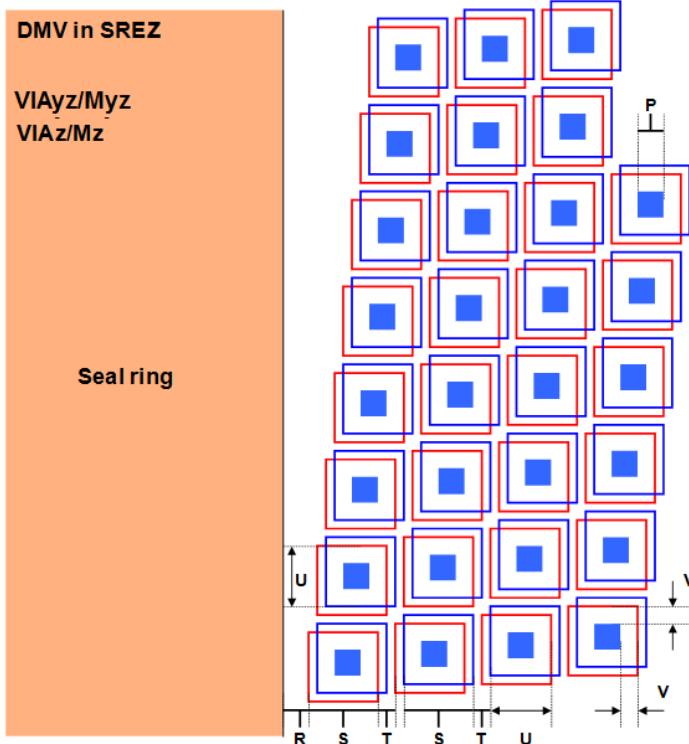


Table. 4.5.71.5.2.1 Rule summary of DMV in seal ring enhanced zone (SREZ) for items P~V.

Label	P	Q	R	S	T	U	V
M0	-	-	0.36	0.72	0.36	0.63	-
VIA0	0.020	0.044	0.36	0.72	0.36	0.63	0.020
M1	-	-	0.36	0.72	0.36	0.63	-
VIAxs/Mxs	0.020	0.044	0.36	0.72	0.36	0.63	0.020
VIAx/Mx	0.020	0.044	0.36	0.72	0.36	0.63	0.020
VIAxa/Mxa	0.020	0.094	0.36	0.72	0.36	0.63	0.020
VIAya/Mya	0.020	0.094	0.36	0.72	0.36	0.63	0.020
VIAy/My	0.038	0.076	0.36	0.72	0.36	0.63	0.020
VIAyy/Myy	0.062	0.099	0.45	0.72	0.36	0.63	0.027
VIAyx/Myx	0.126	0.144	0.45	0.72	0.36	0.63	0.041
VIAyz/Myz	0.180	0.225	0.45	0.72	0.36	0.63	0.045
VIAz/Mz	0.324	0.486	0.45	0.72	0.36	0.63	0.072
VIAr/Mr	0.414	0.594	0.585	0.9	0.45	-	0.072

(DRC tolerance at 45-degree turning: ±0.010)

Seal Ring Mask Pattern Definition

C: Digitized area is clear on mask D: Digitized area is dark on mask.

Seal-ring enhanced zone (SREZ) (5.4μm)	Seal-ring (9μm)	SLDB (7.2μm)	Layer
C	C	C	120 (OD1-ETCH)
C	D	D	12M (OD-FINFET-FCUT-ETCH)
D	D	D	12L (OD-ISO-SRAM-FINFET-ETCH)
D	D	D	12N (OD-CUT-FINFET-ETCH)
C	D	D	12P (OD-FINFE-CCUT-ETCH)
D	D	D	119 (WELL-N-DEEP-IMP)
C	C	C	191 (WELL-P-CORE-IMP)
D	D	D	193 (WELL-P-I/O-IMP)
D	D	D	192 (WELL-N-CORE-IMP)
D	D	D	194 (WELL-N-I/O-IMP)
C	D	D	130 (POLY-GATE-ETCH)
D	C	C	13G (POLY-WIDE-POLY-ETCH)
D	D	D	13B (POLY-TRIM-ETCH)
C	D	D	739 (POLY-CUT-DPL1-ETCH)
C	D	D	839 (POLY-CUT-DPL2-ETCH)
D	D	D	116 (LDD-N-I/O-IMP)
D	D	D	115 (LDD-P-I/O-IMP)
C	D	D	126 (N-SSD-ETCH)
D	C	C	123 (SSD-ETCH)
C	D	D	197 (S/D-P-IMP)
D	C	C	198 (S/D-N-IMP)
D	D	D	152 (OD2-ETCH)
D	D	D	13C (MG-HM-HK-ETCH)
D	D	D	13D (VT1-TUNING-PHO)
D	D	D	13E (VT2-TUNING-PHO)
D	D	D	137 (VT3-TUNNING-PHO)
D	D	D	138 (VT4-TUNNING-PHO)
D	D	D	134 (HR-RESISTOR-ETCH)
D	D	D	A58 (CMD-3P1-ETCH)
D	D	D	B58 (CMD-3P2-ETCH)
D	D	D	C58 (CMD-3P3-ETCH)
C	C	C	756 (CONTACT-METAL-DPL1-ETCH)
C	C	C	856 (CONTACT-METAL-DPL2-ETCH)
D	D	D	759 (CONTACT-M0PO-DPL1-ETCH)
D	D	D	859 (CONTACT-M0PO-DPL2-ETCH)
D	D	D	19N(SPD-BSG-ETCH)
C	C	C	97A (VIA0-MG-DPL1-ETCH)
D	D	D	3AA (METAL0-Cut-ETCH)
D	D	D	7A0 (METAL0-CutB-DPL1-ETCH)
D	D	D	8A0 (METAL0-CutB-DPL2-ETCH)
D	D	D	750 (METAL0-CU-DPL1-ETCH)
D	D	D	850 (METAL0-CU-DPL2-ETCH)
C	C	C	970 (VIA0-CU-3P1-ETCH)
C	C	C	960 (METAL1-CU-ETCH-1)
C	C	C	978 (VIA1-CU-ETCH)
C	C	C	980 (METAL2-CU-ETCH-1)
C	C	C	779 (VIA2-CU-ETCH)
C	C	C	879 (VIA2-CU-ETCH)
C	C	C	379 (VIA2-CU-ETCH)
C	C	C	781 (METAL3-CU-ETCH-1)
C	C	C	881 (METAL3-CU-ETCH-2)
C	C	C	773 (VIA3-CU-ETCH)

Seal-ring enhanced zone (SREZ) (5.4μm)	Seal-ring (9μm)	SLDB (7.2μm)	Layer
C	C	C	873 (VIA3-CU-ETCH)
C	C	C	373 (VIA3-CU-ETCH)
C	C	C	784 (METAL4-CU-ETCH-1)
C	C	C	884 (METAL4-CU-ETCH-2)
C	C	C	384 (METAL4-CU-ETCH)
C	C	C	774 (VIA4-CU-ETCH)
C	C	C	874 (VIA4-CU-ETCH)
C	C	C	374 (VIA4-CU-ETCH)
C	C	C	785 (METAL5-CU-ETCH-1)
C	C	C	885 (METAL5-CU-ETCH-2)
C	C	C	385 (METAL5-CU-ETCH)
C	C	C	775 (VIA5-CU-ETCH)
C	C	C	875 (VIA5-CU-ETCH)
C	C	C	375 (VIA5-CU-ETCH)
C	C	C	786 (METAL6-CU-ETCH-1)
C	C	C	886 (METAL6-CU-ETCH-2)
C	C	C	386 (METAL6-CU-ETCH)
C	C	C	776 (VIA6-CU-ETCH)
C	C	C	876 (VIA6-CU-ETCH)
C	C	C	376 (VIA6-CU-ETCH)
C	C	C	787 (METAL7-CU-ETCH-1)
C	C	C	887 (METAL7-CU-ETCH-2)
C	C	C	387 (METAL7-CU-ETCH)
C	C	C	377 (VIA7-CU-ETCH)
C	C	C	388 (METAL8-CU-ETCH)
C	C	C	372 (VIA8-CU-ETCH)
C	C	C	389 (METAL9-CU-ETCH)
C	C	C	37A (VIA9-CU-ETCH)
C	C	C	38A (METAL10-CU-ETCH)
C	C	C	37B (VIA10-CU-ETCH)
C	C	C	38B (METAL11-CU-ETCH)
C	C	C	37C (VIA11-CU-ETCH)
C	C	C	38C (METAL12-CU-ETCH)
C	C	C	37D (VIA12-CU-ETCH)
C	C	C	38D (METAL13-CU-ETCH)
C	C	C	37E (VIA13-CU-ETCH)
C	C	C	38E (METAL14-CU-ETCH)
D	C	C	306 (VIAR-AL-ETCH)
D	C	C	309 (METALR-AL-ETCH)
D	D	D	308 (PASSIVATION-FUSE-FUSE-CU-ETCH)
D	C	C	009 (PI)

4.5.72.6 Scribe Line Dummy Bar Layout Rules

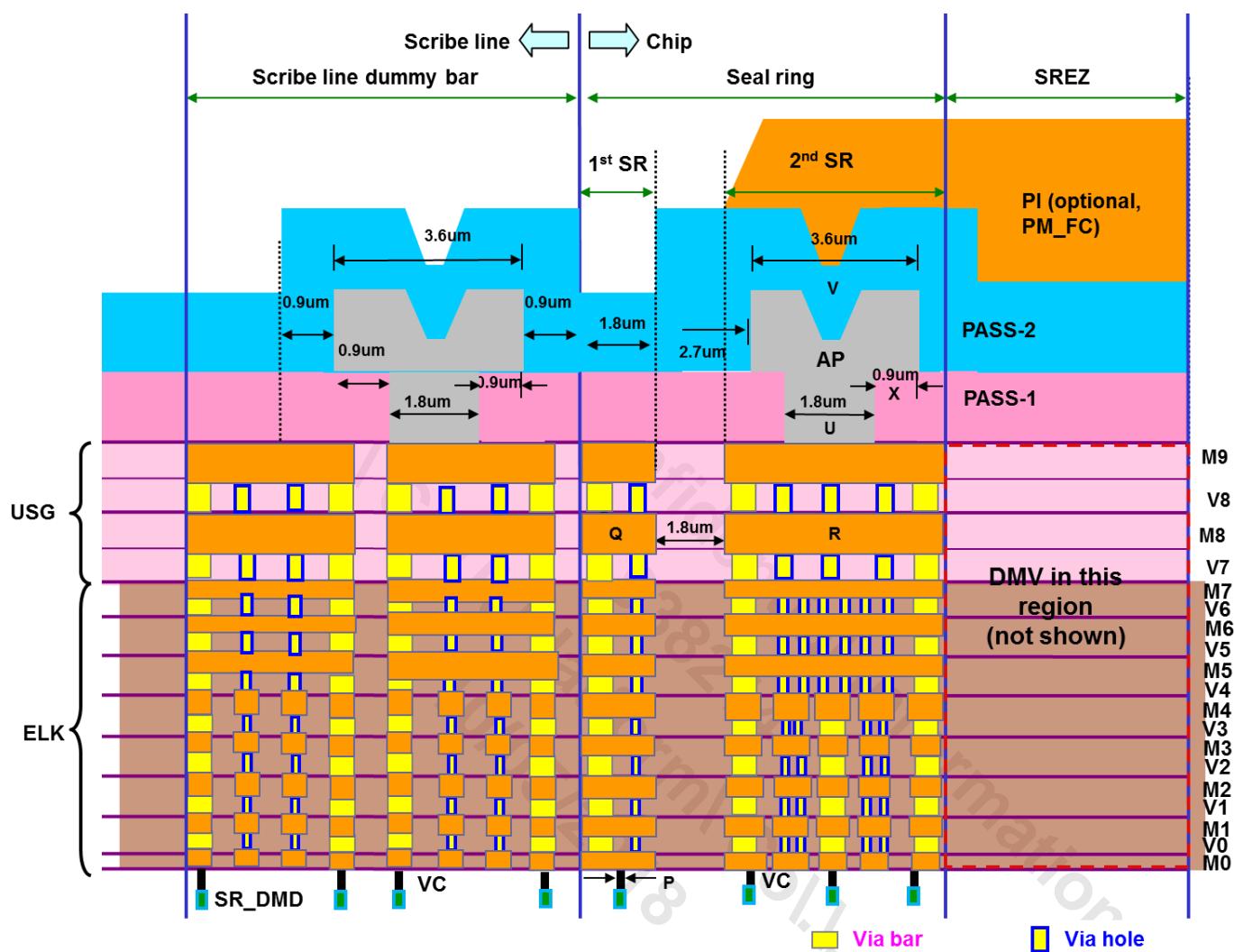
Scribe line dummy bar (SLDB) is an auxiliary structure at scribe line, which is to enhance die saw quality against laser and mechanical die saw alike for wider package reliability margin. 7.2 μm extra space outside the original seal ring structure is needed for SLDB. Please follow exactly the schematic diagram below (as in GDS example) for SLDB. Now, DRC clean does not mean the new design structure is accepted. If you do not use these dimensions as below, please consult with TSMC. Scribe line dummy bar includes two duplicate of 3.15 μm wide structure. Please refer to Fig. 2.6.1 for details.

Rule No.	Description	Label	Op.	Rule
SR.SR_DMD.W.5	Width of SR_DMD bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	A	=	0.1000
SR.SR_DMD.O.2	SR_DMD bar overlap OD_DA in SLDB (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	C	=	0.0390
SR.VC.W.5	Width of VC bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	A1	=	0.0800
SR.VC.EN.2	VC bar enclosure by SR_DMD bar in SLDB (DRC tolerance at 45-degree turning: $\pm 0.005 \mu\text{m}$)	C1	=	0.0100
SR.M0.W.8	Width of M0 metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D	=	0.4500
SR.VIA0.W.4	Width of VIA0 bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E	=	0.1400
SR.VIA0.W.5	Width of VIA0 hole in SLDB.	E1	=	0.0200
SR.VIA0.EN.27	Enclosure of VIA0 hole by M0 in SLDB.	F1	\geq	0.0200
SR.VIA0.EN.28	Enclosure of VIA0 bar by M0 in SLDB.	F	\geq	0.1500
SR.VIA0.S.26	Space of VIA0 hole in SLDB	G	\geq	0.0440
SR.VIA0.S.27	Space of VIA0 hole to VIA0 bar in SLDB.	H	\geq	0.3500
SR.M1.W.8	Width of M1 metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D	=	0.4500
SR.VIAs.W.4	Width of VIAs bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E	=	0.1400
SR.VIAs.W.5	Width of VIAs hole in SLDB.	E1	=	0.0200
SR.VIAs.EN.27	Enclosure of VIAs hole by Mxs in SLDB.	F1	\geq	0.0200
SR.VIAs.EN.28	Enclosure of VIAs bar by Mxs in SLDB.	F	\geq	0.1500
SR.VIAs.S.26	Space of VIAs hole in SLDB	G	\geq	0.0440
SR.VIAs.S.27	Space of VIAs hole to VIAs bar in SLDB.	H	\geq	0.3500
SR.Mxs.W.8	Width of Mxs metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D	=	0.4500
SR.VIAx.W.4	Width of VIAx bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E	=	0.1400
SR.VIAx.W.5	Width of VIAx hole in SLDB.	E1	=	0.0200
SR.VIAx.EN.27	Enclosure of VIAx hole by Mx in SLDB.	F1	\geq	0.0200
SR.VIAx.EN.28	Enclosure of VIAx bar by Mx in SLDB.	F	\geq	0.1500
SR.VIAx.S.26	Space of VIAx hole in SLDB	G	\geq	0.0440
SR.VIAx.S.27	Space of VIAx hole to VIAx bar in SLDB.	H	\geq	0.3500
SR.Mx.W.8	Width of Mx metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D	=	0.4500
SR.VIAXa.W.4	Width of VIAXa bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E	=	0.1400

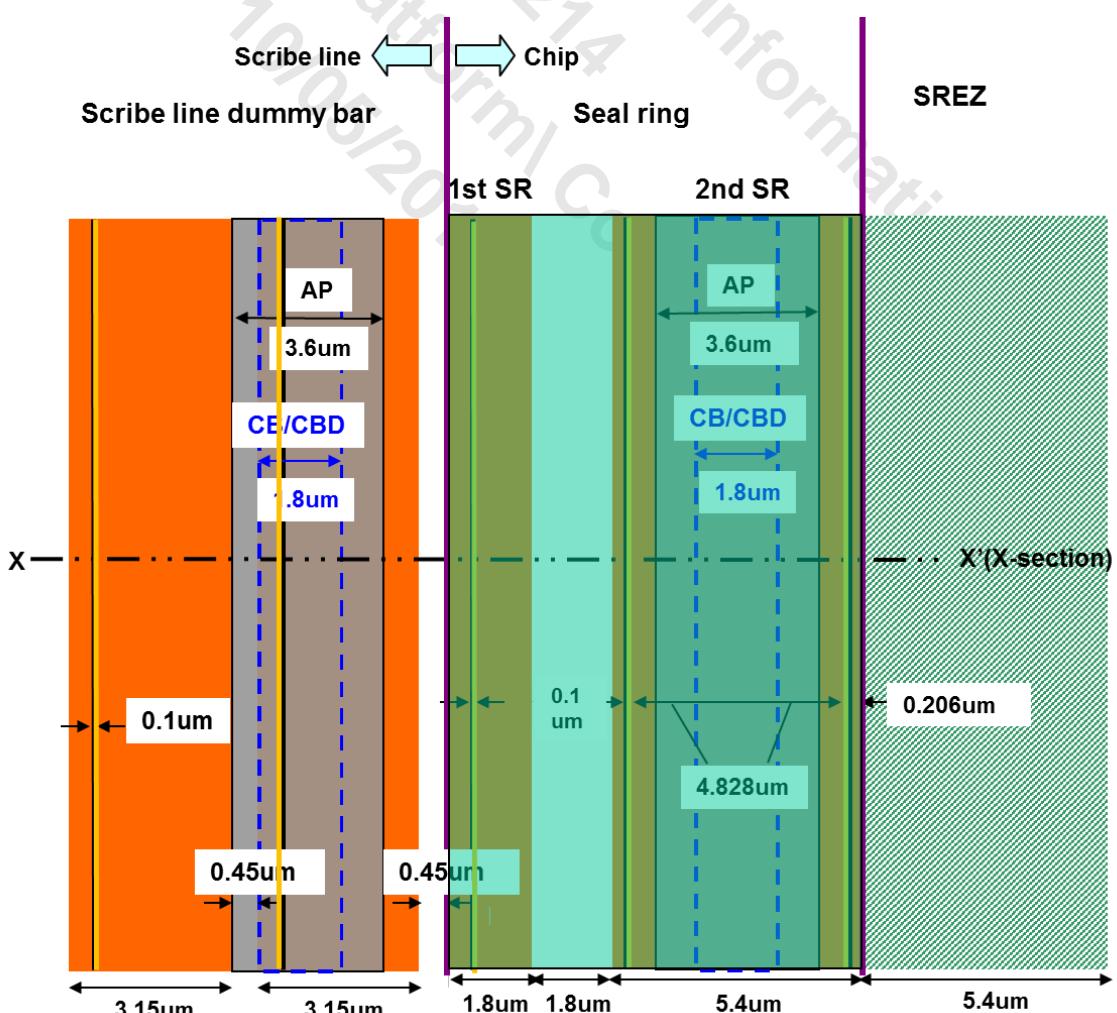
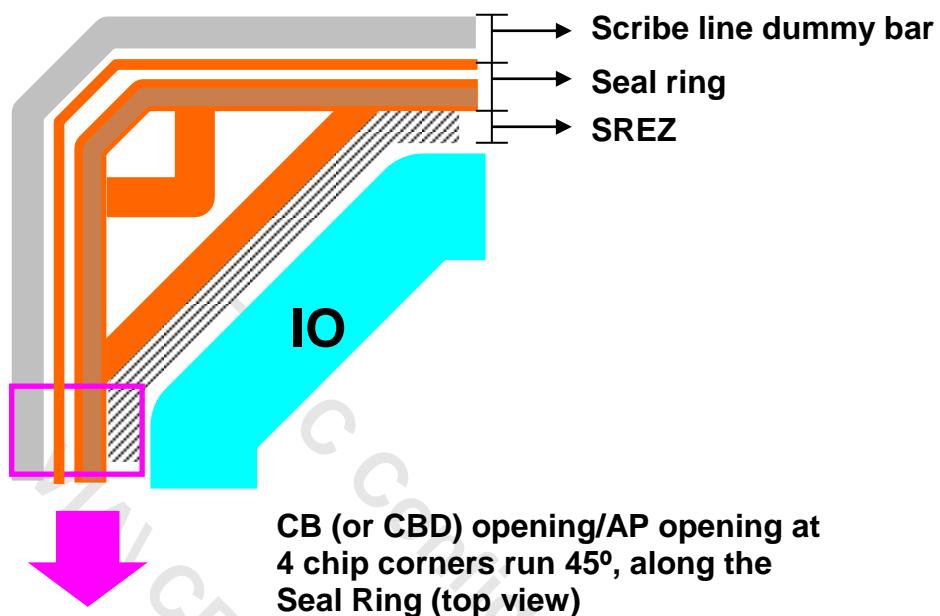
Rule No.	Description	Label	Op.	Rule
SR.VIAxa.W.5	Width of VIAxa hole in SLDB.	E1	=	0.0200
SR.VIAxa.EN.27	Enclosure of VIAxa hole by Mxa in SLDB.	F1	\geq	0.0200
SR.VIAxa.EN.28	Enclosure of VIAxa bar by Mxa in SLDB.	F	\geq	0.1500
SR.VIAxa.S.26	Space of VIAxa hole in SLDB	G	\geq	0.0940
SR.VIAxa.S.27	Space of VIAxa hole to VIAxa bar in SLDB.	H	\geq	0.3500
SR.Mxa.W.8	Width of Mxa metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D	=	0.4500
SR.VIAYa.W.4	Width of VIAYa bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E	=	0.1400
SR.VIAYa.W.5	Width of VIAYa hole in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E1	=	0.0200
SR.VIAYa.EN.27	Enclosure of VIAYa hole by Mya in SLDB.	F1	\geq	0.0200
SR.VIAYa.EN.28	Enclosure of VIAYa bar by Mya in SLDB.	F	\geq	0.1500
SR.VIAYa.S.6	Space of VIAYa hole in SLDB	G	\geq	0.0940
SR.VIAYa.S.7	Space of VIAYa hole to VIAYa bar in SLDB	H	\geq	0.3500
SR.MyA.W.8	Width of Mya metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D	=	0.4500
SR.VIAY.W.4	Width of VIAY bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E2	=	0.4500
SR.VIAY.W.5	Width of VIAY hole in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E4	=	0.0380
SR.VIAY.S.6	Space of VIAY hole in SLDB.	G2		0.0760
SR.VIAY.S.7	Space of VIAY hole to VIAY bar in SLDB.	H2		0.3500
SR.My.W.6	Width of My metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D1	=	3.15
SR.VIAYy.W.4	Width of VIAYy bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E2	=	0.4500
SR.VIAYy.W.5	Width of VIAYy hole in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E4	=	0.0620
SR.VIAYy.S.6	Space of VIAYy hole in SLDB.	G2	\geq	0.0990
SR.VIAYy.S.7	Space of VIAYy hole to VIAYy bar in SLDB.	H2	\geq	0.3500
SR.Myy.W.6	Width of Myy metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D1	=	3.15
SR.VIAYx.W.4	Width of VIAYx bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E2	=	0.4500
SR.VIAYx.W.5	Width of VIAYx hole in SLDB.	E4	=	0.1260
SR.VIAYx.S.6	Space of VIAYx hole in SLDB.	G2	\geq	0.1440

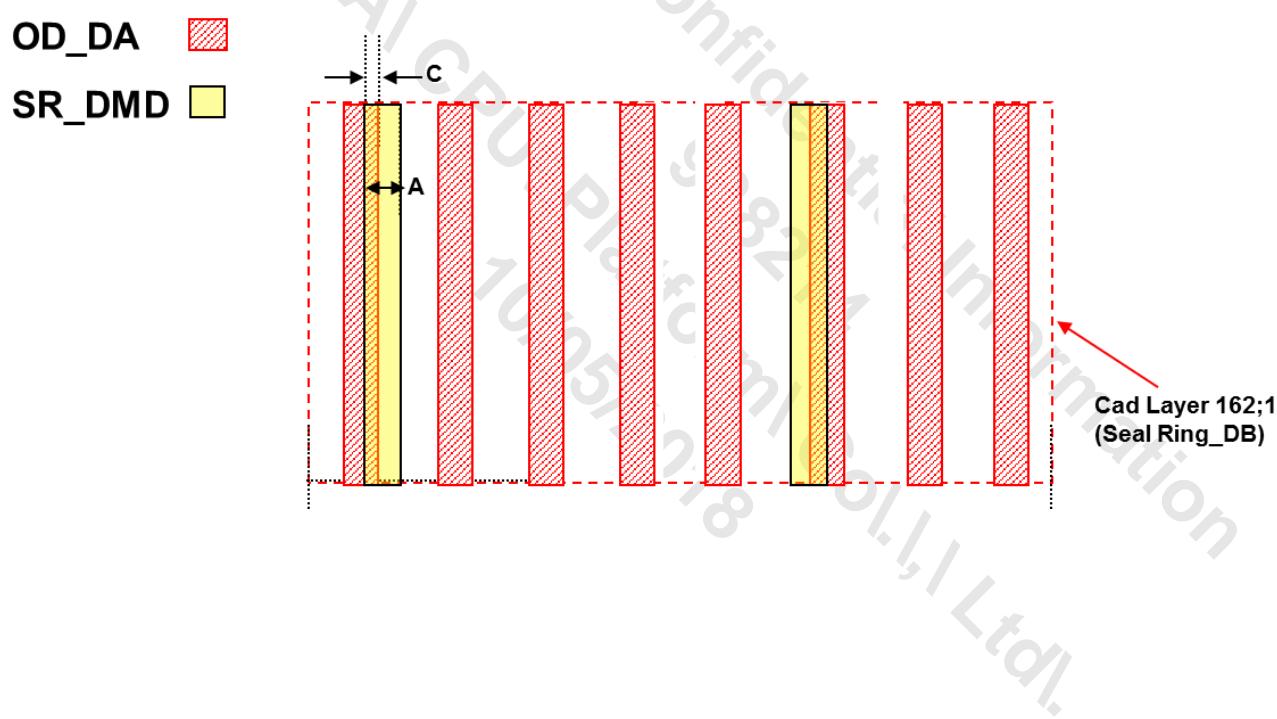
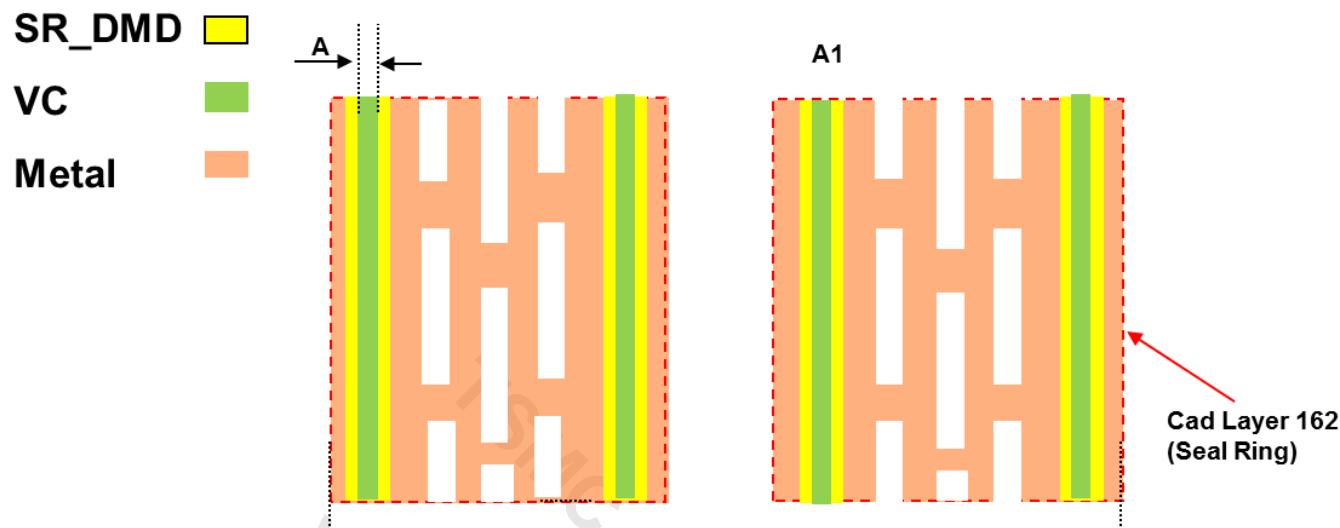
Rule No.	Description	Label	Op.	Rule
SR.VIAyx.S.7	Space of VIAyx hole to VIAyx bar in SLDB.	H2	\geq	0.3500
SR.Myx.W.6	Width of Myx metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D1	=	3.15
SR.VIAYz.W.4	Width of VIAYz bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E2	=	0.4500
SR.VIAYz.W.5	Width of VIAYz hole in SLDB.	E3	=	0.1800
SR.VIAYz.S.6	Space of VIAYz hole in SLDB.	G1	\geq	0.2250
SR.VIAYz.S.7	Space of VIAYz hole to VIAYz bar in SLDB.	H1	\geq	0.3500
SR.Myz.W.6	Width of Myz metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D1	=	3.15
SR.VIAz.W.4	Width of VIAz bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E2	=	0.4500
SR.VIAz.W.5	Width of VIAz hole in SLDB.	E3	=	0.3240
SR.VIAz.S.6	Space of VIAz hole in SLDB.	G1	\geq	0.4860
SR.VIAz.S.7	Space of VIAz hole to VIAz bar in SLDB.	H1	\geq	0.3500
SR.Mz.W.6	Width of Mz metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D1	=	3.15
SR.VIAr.W.4	Width of VIAr bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	E2	=	0.4500
SR.VIAr.W.5	Width of VIAr hole in SLDB.	E3	=	0.4140
SR.VIAr.S.6	Space of VIAr hole in SLDB.	G1	\geq	0.3960
SR.VIAr.S.7	Space of VIAr hole to VIAr bar in SLDB	H1	\geq	0.3500
SR.Mr.W.6	Width of Mr metal line in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	D1	=	2.7
SR.CB.W.4	Width of CB/CBD/RV line opening in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	U	=	1.8
SR.CB.EN.3	Enclosure of CB/CBD/RV by AP in SLDB.	X	\geq	0.8900
SR.AP.W.4	Width of AP bar in SLDB. (DRC tolerance at 45-degree turning: $\pm 0.020 \mu\text{m}$)	V	=	3.6
SR.R.5 ^U	Please add VIA holes in metal lines of SLDB as many as possible.			

**Fig. 4.5.71.6.1. Cross-sectional view of scribe line dummy bar
(Example: 1P9M (1xs1x1ya3y2z))**

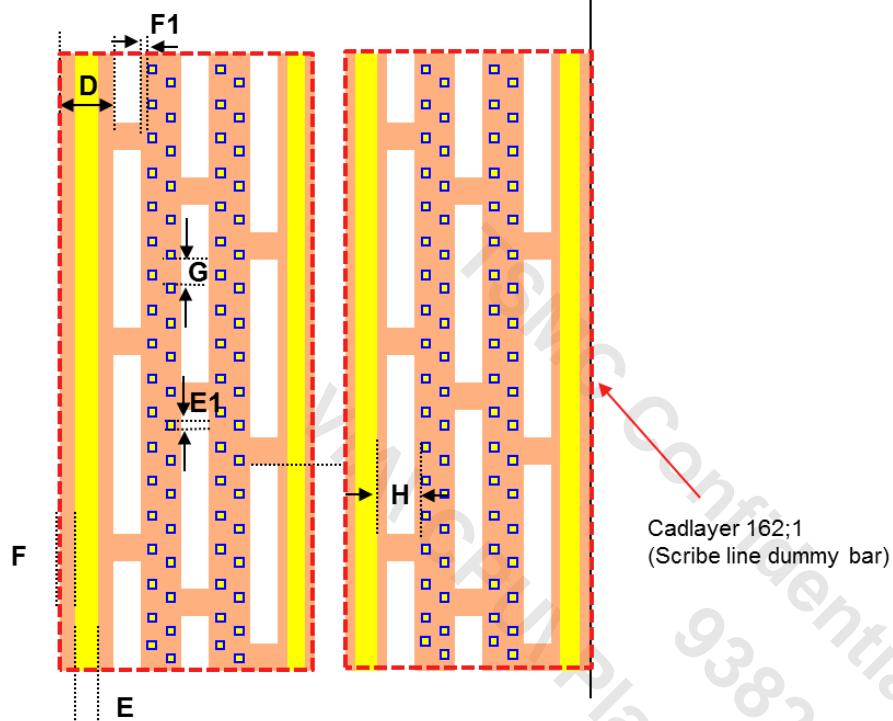


Top view of scribe line dummy bar

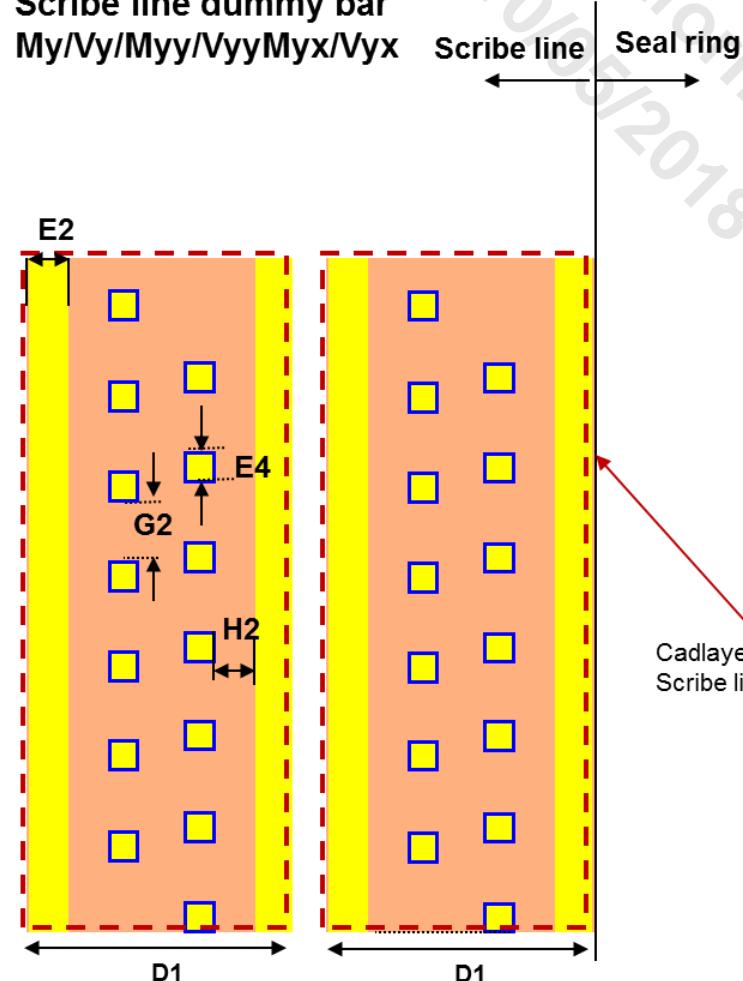




Scribe line dummy bar
M0/V0/M1/Mx/Vx
Mxa/Vxa/Mya/Vya



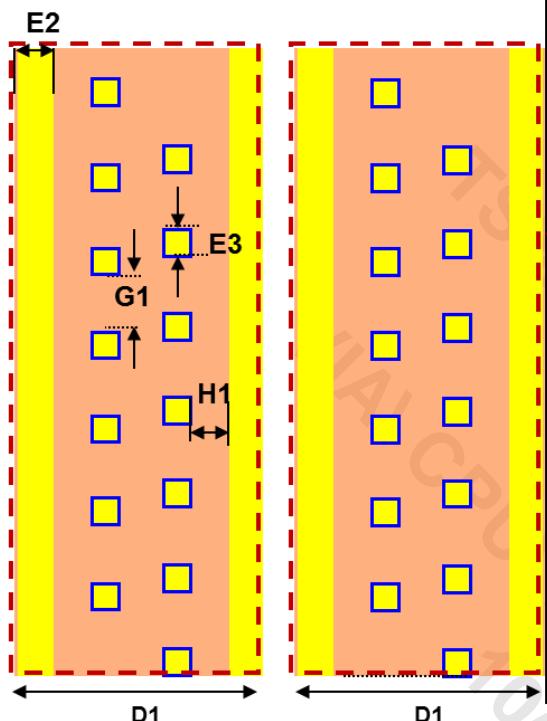
Scribe line dummy bar
My/Vy/Myy/VyyMyx/Vyx



Scribe line dummy bar

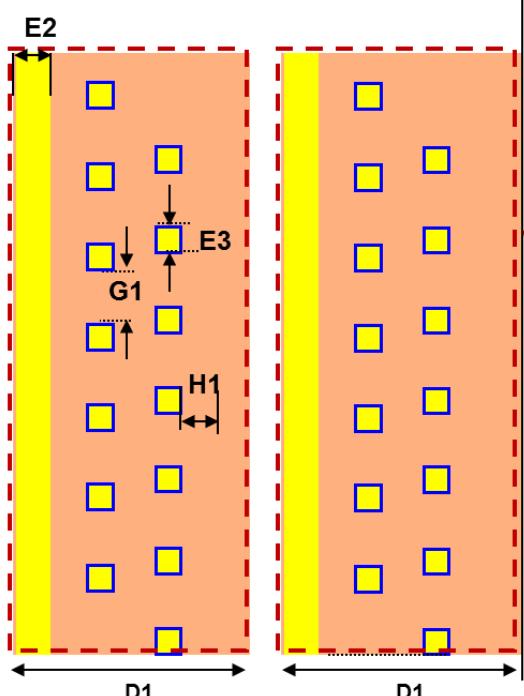
Mz/Vz/Myz/Vyz

Scribe line Seal ring

Cadlayer 162;1
Scribe line dummy bar**Scribe line dummy bar**

Mr/Vr

Scribe line Seal ring

Cadlayer 162;1
Scribe line dummy bar

4.5.73 Pattern Treatment (PT) Rules

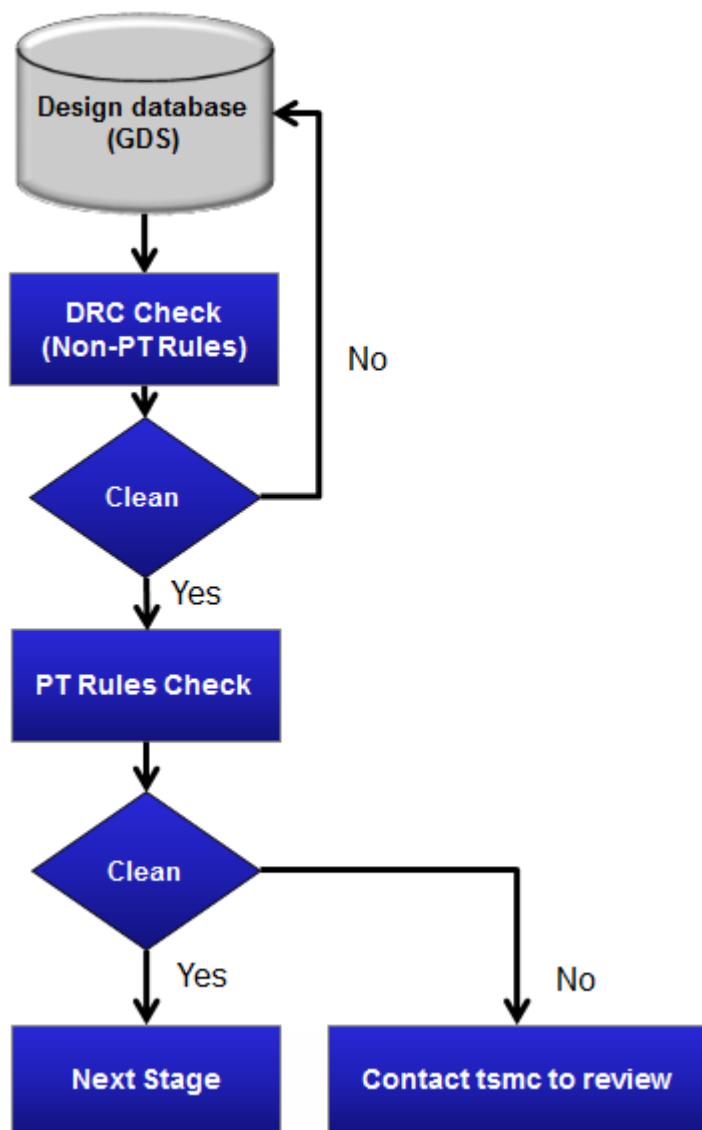
This chapter has been divided into the following topics:

Pattern treatment (PT) rule check is to guarantee CMD/CM0 patterning in post-operations after tape out. In general, layout complying non-PT rules should pass PT rule check. However, if PT rules flag only, please contact TSMC to review any patterning issue

This chapter has been divided into the following topics:

- 4.5.72.1 DRC Flow with PT Rules
- 4.5.72.2 CMD Pattern Treatment Rules
- 4.5.72.3 CM0 Pattern Treatment Rules
- 4.5.72.4 M1_VIRT Pattern Treatment Rules

4.5.73.1 DRC Flow with PT Rules



4.5.73.2 CMD Pattern Treatment Rules

Rule No. ¹⁾	Description ¹⁾	Label ¹⁾	Op. ¹⁾	Rule ¹⁾
CELL.CMD.R.1.PT. ¹⁾	{}{(CMDA NOT BCMD) OR (CMDB NOT BCMD)} and ALL_CMD must be drawn identically... DRC checks in FB_9, FB_8. ¹⁾	¹⁾	¹⁾	¹⁾
H240.CMD.S.56.PT. ¹⁾	Space of CMDA in vertical direction [PRL > -0.060 μm, INSIDE FB_9]. ¹⁾	S6. ¹⁾	\geq ¹⁾	0.0670. ¹⁾
H240.CMD.S.56.1.PT. ¹⁾	Space of CMDB in vertical direction [PRL > -0.060 μm, INSIDE FB_9]. ¹⁾	S6A. ¹⁾	\geq ¹⁾	0.0670. ¹⁾
H240.CMD.S.57.PT. ¹⁾	Space of CMDA in horizontal direction [PRL > -0.060 μm, INSIDE {FB_9 NOT CCP_9}]. ¹⁾	S7. ¹⁾	\geq ¹⁾	0.1140. ¹⁾
H240.CMD.S.57.1.PT. ¹⁾	Space of CMDB in horizontal direction [PRL > -0.060 μm, INSIDE {FB_9 NOT CCP_9}]. ¹⁾	S7A. ¹⁾	\geq ¹⁾	0.1140. ¹⁾
H240.CMD.S.58.PT. ¹⁾	Space of CMDA in horizontal direction [PRL > -0.060 μm, INSIDE CCP_9]. ¹⁾	S8. ¹⁾	$=$ ¹⁾	0.0570, \geq 0.1140. ¹⁾
H240.CMD.S.58.1.PT. ¹⁾	Space of CMDB in horizontal direction [PRL > -0.060 μm, INSIDE CCP_9]. ¹⁾	S8A. ¹⁾	$=$ ¹⁾	0.0570, \geq 0.1140. ¹⁾
H240.CMD.L.55.PT. ¹⁾	Length of CMDA/CMDB [INSIDE {FB_9 NOT CCP_9}] in horizontal direction. ¹⁾	L5. ¹⁾	\geq ¹⁾	0.1140. ¹⁾
H240.CMD.L.55.1.PT. ¹⁾	Length of CMDA/CMDB [INSIDE CCP_9] in horizontal direction. ¹⁾	L5A. ¹⁾	$=$ ¹⁾	0.0570, \geq 0.1140. ¹⁾
H240.CMD.R.56.1.PT. ¹⁾	CMDA/CMDB must be a rectangle orthogonal to grid. ¹⁾	¹⁾	¹⁾	¹⁾
H240.CMD.R.56.4.PT. ¹⁾	CMDA/CMDB [width = 0.056 μm] must abut{CCP_9 SIZING 0.042 μm in vertical direction}. ¹⁾	¹⁾	¹⁾	¹⁾
H300.CMD.S.56.PT. ¹⁾	Space of CMDA/CMDB [width = 0.040 μm] to CMDA/CMDB in vertical direction [PRL > -0.054 μm, INSIDE FB_8]. ¹⁾	S6. ¹⁾	$=$ ¹⁾	0.0560, \geq 0.0670. ¹⁾
H300.CMD.S.56.1.PT. ¹⁾	Space of CMDA/CMDB [width = 0.054 μm] to CMDA/CMDB in vertical direction [PRL > -0.060 μm, INSIDE FB_8]. ¹⁾	S6. ¹⁾	$=$ ¹⁾	0.0670, \geq 0.0830. ¹⁾
H300.CMD.S.56.2.PT. ¹⁾	Space of CMDA/CMDB [width = 0.056 μm] to CMDA/CMDB in vertical direction [PRL > -0.060 μm, INSIDE FB_8]. ¹⁾	S6. ¹⁾	\geq ¹⁾	0.0830. ¹⁾
H300.CMD.S.58.PT. ¹⁾	Space of CMDA/CMDB in horizontal direction [PRL > 0 μm, INSIDE CCP_8]. ¹⁾	S8. ¹⁾	$=$ ¹⁾	0.0570, 0.0630, \geq 0.1140. ¹⁾
H300.CMD.S.58.2.PT. ¹⁾	Space of CMDA/CMDB in horizontal direction [PRL > 0 μm, INSIDE {FB_8 NOT CCP_8}]. ¹⁾	S8. ¹⁾	\geq ¹⁾	0.1140. ¹⁾
H300.CMD.L.55.PT. ¹⁾	Length of CMDA/CMDB [INSIDE {FB_8 NOT CCP_8}] in horizontal direction. ¹⁾	L5. ¹⁾	\geq ¹⁾	0.1140. ¹⁾
H300.CMD.L.55.1.PT. ¹⁾	Length of CMDA/CMDB [INSIDE CCP_8] in horizontal direction. ¹⁾	L5A. ¹⁾	$=$ ¹⁾	0.0570, 0.0630, \geq 0.1140. ¹⁾
H300.CMD.R.56.1.PT. ¹⁾	CMDA/CMDB must be a rectangle orthogonal to grid. ¹⁾	¹⁾	¹⁾	¹⁾
H300.CMD.R.56.4.PT. ¹⁾	CMDA/CMDB [width = 0.040 μm] must abut{CCP_8 SIZING 0.042 μm in vertical direction}. ¹⁾	¹⁾	¹⁾	¹⁾
H300.CMD.R.56.5.PT. ¹⁾	CMDA/CMDB [width = 0.056 μm] must abut{CCP_8 SIZING 0.082 μm in vertical direction}. ¹⁾	¹⁾	¹⁾	¹⁾

4.5.73.3 CM0 Pattern Treatment Rules

Rule No..	Description..	Label..	Op..	Rule..
CM0.R.0.PT..	Use CM0_CA_LOP, CM0_CB_LOP, BCM0V_CAf, BCM0V_CBF, as inputs for all XXX.PT rule..	.1	=P	.1
CELL.M0.A.2.PT..	Area of M0_NOT_CM0..	A2..	$\geq P$	0.00123..
CELL.CM0A.S.4.PT..	Space of CM0A edge [INSIDE M0CA] to VC [PRL > 0 μm] (VC [INSIDE M0CA] overlap CM0Ais not allowed)..	S4..	$\geq .1$	0.0065..
CELL.CM0A.S.4.1.PT..	Space of CM0A edge [INSIDE M0CA] to VC [width/length = 0.016/0.056 μm , 0.020/0.064 μm] [PRL > 0 μm]..	S4..	$\geq .1$	0.0200..
CELL.CM0A.S.5.PT..	Space of CM0A edge [INSIDE M0CA] to VIA0 [PRL > 0 μm] (VIA0 [INSIDE M0CA] overlap CM0Ais not allowed).. (Except BLK_WB)..	S5..	$\geq .1$	0.0065..
CELL.CM0B.S.1.PT..	Space.. (Except BLK_WB, or following conditions: .. 1. Both CM0B interact BCM0VB, .. 2. Two CM0B space = 0.0615 μm [both CM0B length \geq 0.160 μm , PRL > -0.079 μm])..	S1..	$\geq .1$	0.0840..
CELL.CM0B.S.1.2.PT..	Space to long side of CM0B [length < 0.160 μm , PRL > -0.079 μm , INSIDE {{FB_9 OR FB_8} NOT {{CCP_9 OR CCP_8} SIZING -0.010 μm }]}..	S1B..	$\geq .1$	0.0840..
CELL.CM0B.S.4.PT..	Space of CM0B edge [INSIDE M0CB] to VC [PRL > 0 μm] (VC [INSIDE M0CB] overlap CM0B is not allowed).. (Except BLK_WB)..	S4..	$\geq .1$	0.0065..
CELL.CM0B.S.4.1.PT..	Space of CM0B edge [INSIDE M0CB] to VC [width/length = 0.016/0.056 μm , 0.020/0.064 μm] [PRL > 0 μm]..	S4..	$\geq .1$	0.0200..
CELL.CM0B.S.5.PT..	Space of CM0B edge [INSIDE M0CB] to VIA0 [PRL > 0 μm] (VIA0 [INSIDE M0CB] overlap CM0B is not allowed).. (Except BLK_WB)..	S5..	$\geq .1$	0.0065..
CELL.CM0B.R.7.3.PT..	P114_Group width in horizontal direction > 0.936 μm is not allowed.. Definition of P114_Space:.. Space region = 0.090 μm in horizontal direction formed by CM0B [length > 0.240 μm , PRL > 0.240 μm].. Definition of P114_Group:.. {{P114_Space SIZING 0.024 μm in horizontal direction} SIZING down/up 0.280 μm in vertical direction}..	.1	.1	.1
H240.CM0A.W.3.PT..	Width of CM0A_Group in horizontal direction.. Definition of CM0A_Group:.. {{CM0A[INTERACT CCP_9, length < 0.160 μm , space = 0.090 μm in horizontal direction, PRL > 0 μm] SIZING 0.070 μm in vertical direction} SIZING up/down 0.017 μm in horizontal direction} AND CCP_9)..	W3..	$\leq .1$	0.3090..
H240.CM0A.S.2.PT..	Space of short side of CM0A[PRL > -0.044 μm , INSIDE FB_9] (Except following conditions: .. 1. short side space of CM0A[INTERACT BCM0VA] = 0.040 μm [PRL > -0.044 μm] inside CCP_9)..	S2..	$\geq .1$	0.1200..
H240.CM0B.W.3.PT..	Width of CM0B_Group in horizontal direction.. Definition of CM0B_Group:.. {{CM0B[INTERACT CCP_9, length < 0.160 μm , space = 0.090 μm in horizontal direction, PRL > 0 μm] SIZING 0.070 μm in vertical direction} SIZING up/down 0.017 μm in horizontal direction} AND CCP_9)..	W3..	$\leq .1$	0.3090..
H240.CM0B.S.1.1.PT..	Space of long side of CM0B[PRL > -0.079 μm , INSIDE {FB_9 NOT {CCP_9 SIZING -0.010 μm }]}..	S1A..	$= .1$	0.0615, 0.0705, 0.0840, 0.0900, 0.0960, 0.1020, 0.1110, ≥ 0.1160 .

Rule No..	Description..	Label..	Op..	Rule..
H240.CM0B.S.2.PT..	Space of short side of CM0B [PRL > -0.056 μm, INSIDE FB_9] (Except following conditions: .. 1. short side space of CM0B [INTERACT BCM0VB] = 0.040 μm [PRL > -0.056 μm] inside CCP_9).)	S2..	≥..	0.1200..
H300.CM0A.S.2.PT..	Space of short side of CM0A [PRL > -0.044 μm, INSIDE FB_8] (Except following conditions: .. 1. short side space of CM0A [INTERACT BCM0VA] = 0.060 μm [PRL > -0.044 μm] inside CCP_8).)	S2..	≥..	0.1200..
H300.CM0B.W.3.PT..	Width of CM0B_Group in horizontal direction.. .. Definition of CM0B_Group:.. {{{CM0B [INTERACT CCP_8, length < 0.160 μm, space = 0.090 μm in horizontal direction, PRL > 0 μm] SIZING 0.070 μm in vertical direction} SIZING up/down 0.017 μm in horizontal direction} AND CCP_8}.)	W3..	≤..	0.3090..
H300.CM0B.W.3.1.PT..	Width of CM0B_Group_P63 in horizontal direction.. .. Definition of CM0B_Group_P63:.. {{{CM0B [INTERACT CCP_8, length < 0.160 μm, space = 0.102 μm in horizontal direction, PRL > 0 μm] SIZING 0.070 μm in vertical direction} SIZING up/down 0.0195 μm in horizontal direction} AND CCP_8}.)	W3..	≤..	0.3390..
H300.CM0B.S.1.1.PT..	Space of long side of CM0B [PRL > -0.079 μm, INSIDE {FB_8 NOT {CCP_8 SIZING -0.010 μm}}].)	S1A..	=..	0.0615, 0.0705, 0.0840, 0.0900, 0.0960, 0.1020, 0.1110, ≥ 0.1160.
H300.CM0B.S.2.PT..	Space of short side of CM0B [PRL > -0.056 μm, INSIDE FB_8] (Except following conditions: .. 1. short side space of CM0B [INTERACT BCM0VB] = 0.060 μm [PRL > -0.056 μm] inside CCP_8).)	S2..	≥..	0.1200..
CM0A.S.1.PT..	Space.. (Except following conditions: .. 1. both CM0A interact BCM0VA).)	S1..	≥..	0.0840..
CM0A.S.1.1.PT..	Space of long side of CM0A[PRL > -0.079 μm]. (Except following conditions: .. 1. both CM0A interact BCM0VA).)	S1A..	≥..	0.0840..
CM0A.S.3.PT..	Space to M0CA..	S3..	≥..	0.0140..
CM0A.S.3.1.PT..	Space of short side of CM0Ato M0CA..	S3A..	≥..	0.0300..
CM0A.O.1.PT..	Overlap of M0CAin CM0A width direction.. (Except BLK_WB).)	O1..	=..	0.0240..
CM0A.EX.1.PT..	Extension on M0CAin CM0A length direction..	EX1..	≥..	0.0300..
CM0A.EX.1.1.PT..	Extension on M0CA[width > 0.028 μm or MINP space to M0 [PRL to CM0A short side > -0.022 μm] ≥ 0.075 μm in CM0A length direction]. (Except BLK_WB).)	EX1A..	≥..	0.0450..
CM0B.S.3.PT..	Space to M0CB..	S3..	≥..	0.0140..
CM0B.S.3.1.PT..	Space of short side of CM0B to M0CB..	S3A..	≥..	0.0300..
CM0B.S.3.2.PT..	Space to M0CA.. (Except BLK_WB).)	S3B..	≥..	0.0080..
CM0B.S.3.3.PT..	Space of short side of CM0B to M0CA.. (Except DM0_DO1, BLK_WB).)	S3C..	≥..	0.0300..
CM0B.S.7.PT..	Forbidden space of P855_Group in horizontal direction.. .. Definition of P855_Space:.. Space region = 0.0615 μm in horizontal direction formed by CM0B [length ≥ 0.160 μm, PRL ≥ 0.160 μm]. .. Definition of P855_Group:.. {P855_Space SIZING 0.024 μm in horizontal direction}.)	S7..	=..	0.0960~0.1260..

Rule No..	Description..	Label..	Op..	Rule..
CM0B.S.8.PT..	<p>Space of CM0B [length $\geq 0.560 \mu\text{m}$] to P108_Group_L, P114_Group_L in horizontal direction [PRL $> 0.560 \mu\text{m}$].</p> <p>Definition of P108_Space:.. Space region = $0.084 \mu\text{m}$ in horizontal direction formed by CM0B..</p> <p>Definition of P108_Group_L:.. { {P108_Space SIZING $0.024 \mu\text{m}$ in horizontal direction} SIZING down/up $0.280 \mu\text{m}$ in vertical direction } [width in horizontal direction $\geq 0.348 \mu\text{m}$].</p> <p>Definition of P114_Space:.. Space region = $0.090 \mu\text{m}$ in horizontal direction formed by CM0B..</p> <p>Definition of P114_Group_L:.. { {P114_Space SIZING $0.024 \mu\text{m}$ in horizontal direction} SIZING down/up $0.280 \mu\text{m}$ in vertical direction } [width in horizontal direction $\geq 0.366 \mu\text{m}$].</p>	S8..	\geq ..	0.5000..
CM0B.O.1.PT..	Overlap of M0CA in CM0B width direction..	O1..	\geq ..	0.0120..
CM0B.O.2.PT..	Overlap of M0CB in CM0B width direction..	O2..	=..	0.0240..
CM0B.EX.1.PT..	Extension on M0CB in CM0B length direction..	EX1..	\geq ..	0.0300..
CM0B.EX.1.1.PT..	Extension on M0CB [width $> 0.028 \mu\text{m}$ or MINP space to M0 [PRL to CM0B short side $> -0.022 \mu\text{m}$] $\geq 0.075 \mu\text{m}$ in CM0B length direction]. (Except BLK_WB)..	EX1A..	\geq ..	0.0450..
CM0B.R.5.PT..	{CM0B INTERACT M0CA [width $\geq 0.060 \mu\text{m}$]} is not allowed. (Except following conditions: .. 1. CM0B interact CCP_9, CCP_8).
CM0B.R.7.1.PT..	P855_Group width in horizontal direction $> 1.221 \mu\text{m}$ is not allowed.. Definition of P855_Space:.. Space region = $0.0615 \mu\text{m}$ in horizontal direction formed by CM0B [length $\geq 0.160 \mu\text{m}$, PRL $\geq 0.160 \mu\text{m}$]. Definition of P855_Group:.. {P855_Space SIZING $0.024 \mu\text{m}$ in horizontal direction}.
CM0B.R.7.1.1.PT..	P945_Group width in horizontal direction $> 0.969 \mu\text{m}$ is not allowed.. Definition of P945_Space:.. Space region = $0.0705 \mu\text{m}$ in horizontal direction formed by CM0B [length $\geq 0.160 \mu\text{m}$, PRL $\geq 0.160 \mu\text{m}$]. Definition of P945_Group:.. {P945_Space SIZING $0.024 \mu\text{m}$ in horizontal direction}.
CM0B.R.7.2.PT..	P108_Group width in horizontal direction $> 0.348 \mu\text{m}$ is not allowed.. Definition of P108_Space:.. Space region = $0.084 \mu\text{m}$ in horizontal direction formed by CM0B [length $\geq 0.160 \mu\text{m}$, PRL $\geq 0.160 \mu\text{m}$]. Definition of P108_Group:.. {P108_Space SIZING $0.024 \mu\text{m}$ in horizontal direction}.

Rule No..	Description..	Label..	Op..	Rule..
CM0B.R.7.3.PT..	<p>P114_Group width in horizontal direction > 0.366 μm is not allowed. (Except FB_9, FB_8)..</p> <p>Definition of P114_Space:.. Space region = 0.090 μm in horizontal direction formed by CM0B [length > 0.160 μm, PRL > 0.160 μm]..</p> <p>Definition of P114_Group:.. {P114_Space SIZING 0.024 μm in horizontal direction}..</p>	.1	.1	.1
CM0B.R.7.4.PT..	<p>P120_Group width in horizontal direction > 0.384 μm is not allowed..</p> <p>Definition of P120_Space:.. Space region = 0.096 μm in horizontal direction formed by CM0B [length \geq 0.160 μm, PRL \geq 0.160 μm]..</p> <p>Definition of P120_Group:.. {P120_Space SIZING 0.024 μm in horizontal direction}..</p>	.1	.1	.1
CM0B.R.7.5.PT..	<p>P135_Group width in horizontal direction > 0.429 μm is not allowed..</p> <p>Definition of P135_Space:.. Space region = 0.111 μm in horizontal direction formed by CM0B [length \geq 0.160 μm, PRL \geq 0.160 μm]..</p> <p>Definition of P135_Group:.. {P135_Space SIZING 0.024 μm in horizontal direction}..</p>	.1	.1	.1

Platform Col., Ltd.
10/05/2018

4.5.73.4 M1_VIRT Pattern Treatment Rules

Rule No.,	Description.,	Label.,	Op.,	Rule.,
VIA0.R.0.PT ^U ,	Use M1i_Output as M1 (31;420) for all VIA0.XXX.PT rule.,	,,	,,	,,
VIA0.EN.18.PT.,	Checked_VIA0_Edge1 enclosure by M0_NOT_CM0 in M0 NMNP direction., Definition of Checked_VIA0.:. {VIA0 AND M0} INTERACT M1 width = 0.020 μm., Definition of Checked_VIA0_Edge1.:. 1. Checked_VIA0 edge space to M1 > 0.021 μm with PRL > -0.020 μm in M1 MINP direction.,	EN18.,	≥.,	0.0120.,
VIA0.R.4.1.PT.,	Space of vertical edge of Checked_VIA0 to M1 in M1 MINP direction [PRL > 0 μm] > 0.022 μm is not allowed., Definition of Checked_VIA0.:. Bridge_VIA0 with edge space to M1 < 0.056 μm with PRL > -0.120 μm in M1 MINP direction., Definition of Bridge_VIA0.:. VIA0 [edge length = 0.020/0.060 μm in horizontal/vertical direction] INTERACT M1 width < 0.034 μm.,	,,	,,	,,
M1.R.0.PT ^U ,	Use M1i_Output as M1 (31;420) for all M1.XXX.PT rule.,	,,	,,	,,
M1.W.1.PT.,	Width.,	W1.,	≥.,	0.0200.,
M1.W.1.1.1.PT.,	Width of M1 (31;420) [MINP direction]., (Except BLK_M1).,	W1A.,	=.,	0.0200, 0.0220, 0.0240, ≥ 0.0340.,
M1.S.1.PT.,	Space.,	S1.,	≥.,	0.0180.,
M1.S.31.1.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 [width < 0.0205 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm].,	SM.,	=.,	0.0180, 0.0200, ≥ 0.0340.,
M1.S.31.1.2.PT.,	Space of M1 to M1 [width < 0.0205 μm with edge length > 0.060 μm in NMNP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm].,	SM.,	=.,	0.0180, 0.0200, ≥ 0.0340.,
M1.S.31.2.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm].,	SM.,	=.,	0.0200, ≥ 0.0340.,
M1.S.31.2.2.PT.,	Space of M1 to M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMNP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm].,	SM.,	=.,	0.0200, ≥ 0.0340.,
M1.S.31.3.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.0225 μm ≤ width < 0.0245 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm].,	SM.,	=.,	0.0200, ≥ 0.0260.,
M1.S.31.3.2.PT.,	Space of M1 to M1 [0.0225 μm ≤ width < 0.0245 μm with edge length > 0.060 μm in NMNP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm].,	SM.,	=.,	0.0200, ≥ 0.0260.,
M1.S.32.1.PT.,	Space of M1 to M1 [0.0245 μm ≤ width < 0.034 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm].,	SM.,	≥.,	0.0200.,
M1.S.32.2.PT.,	Space of M1 to M1 [0.034 μm ≤ width < 0.0605 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.038 μm].,	SM.,	≥.,	0.0200.,
M1.S.33.1.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMNP direction] in MINP direction [PRL > -0.040 μm].,	SM.,	≥.,	0.0200.,

Rule No.	Description	Label	Op.	Rule
M1.S.33.1.2.PT	Space of M1 to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0200
M1.S.34.1.1.PT	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.0845 μm ≤ width < 0.100 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.34.1.2.PT	Space of M1 to M1 [0.0845 μm ≤ width < 0.100 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.35.1.1.PT	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.100 μm ≤ width < 0.260 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.35.1.2.PT	Space of M1 to M1 [0.100 μm ≤ width < 0.260 μm with edge length > 0.060 μm in NMINP direction, NOT INTERACT BLK_M1] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.35.2.PT	Space of M1 to M1 [width ≥ 0.260 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0400
M1.S.37.1.PT	Space of M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.0245 μm ≤ width < 0.034 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.1.1.PT	Space of M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.034 μm ≤ width < 0.0605 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.2.PT	Space of M1 [width < 0.0205 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.3.PT	Space of M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.0245 μm ≤ width < 0.034 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.3.1.PT	Space of M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.034 μm ≤ width < 0.0605 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.37.4.PT	Space of M1 [0.0205 μm ≤ width < 0.0225 μm with edge length > 0.060 μm in NMINP direction] to M1 [0.0605 μm ≤ width < 0.0845 μm with edge length > 0.060 μm in NMINP direction] in MINP direction [PRL > -0.040 μm]	SM	≥	0.0340
M1.S.41.1.PT	Space of M1 to M1 [width < 0.080 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0600
M1.S.42.1.1.PT	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.080 μm ≤ width < 0.100 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760
M1.S.42.1.2.PT	Space of M1 to M1 [0.080 μm ≤ width < 0.100 μm with edge length > 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760
M1.S.43.1.1.PT	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.100 μm ≤ width < 0.120 μm with edge length > 0.060 μm in MINP direction] in NMINP direction [PRL > -0.060 μm]	SN	≥	0.0760

Rule No.,	Description.,	Label,	Op.,	Rule.,
M1.S.43.1.2.PT.,	Space of M1 to M1 [0.100 μm \leq width $<$ 0.120 μm with edge length $>$ 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $>$ -0.060 μm .]	SN.,	\geq ,	0.0760.,
M1.S.44.1.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.120 μm \leq width $<$ 0.140 μm with edge length $>$ 0.060 μm in MINP direction] in NMINP direction [PRL $>$ -0.060 μm .]	SN.,	\geq ,	0.0600.,
M1.S.44.1.2.PT.,	Space of M1 to M1 [0.120 μm \leq width $<$ 0.140 μm with edge length $>$ 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $>$ -0.060 μm .]	SN.,	\geq ,	0.0600.,
M1.S.44.2.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 [0.120 μm \leq width $<$ 0.140 μm with edge length $>$ 0.060 μm in MINP direction] in NMINP direction [PRL $>$ -0.020 μm .]	SN.,	\geq ,	0.0760.,
M1.S.44.2.2.PT.,	Space of M1 to M1 [0.120 μm \leq width $<$ 0.140 μm with edge length $>$ 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $>$ -0.020 μm .]	SN.,	\geq ,	0.0760.,
M1.S.45.1.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 [width \geq 0.140 μm with edge length $>$ 0.060 μm in MINP direction] in NMINP direction [PRL $>$ 0 μm .]	SN.,	\geq ,	0.1200.,
M1.S.45.1.2.PT.,	Space of M1 to M1 [width \geq 0.140 μm with edge length $>$ 0.060 μm in MINP direction, NOT INTERACT BLK_M1] in NMINP direction [PRL $>$ 0 μm .]	SN.,	\geq ,	0.1200.,
M1.S.51.1.PT.,	Space of M1 to M1 line-end in NMINP direction [PRL $>$ -0.018 μm .]	S51.,	\geq ,	0.0300.,
M1.S.51.2.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 line-end [edge length = 0.020 μm] in NMINP direction [PRL $>$ -0.018 μm .]	S51.,	\geq ,	0.0400.,
M1.S.51.2.2.PT.,	Space of M1 to M1 line-end [edge length = 0.020 μm , NOT INTERACT BLK_M1] in NMINP direction [PRL $>$ -0.018 μm .]	S51.,	\geq ,	0.0400.,
M1.S.51.3.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 line-end [0.020 μm $<$ edge length $<$ 0.034 μm] in NMINP direction [PRL $>$ -0.020 μm .]	S51.,	\geq ,	0.0400.,
M1.S.51.3.2.PT.,	Space of M1 to M1 line-end [0.020 μm $<$ edge length $<$ 0.034 μm , NOT INTERACT BLK_M1] in NMINP direction [PRL $>$ -0.020 μm .]	S51.,	\geq ,	0.0400.,
M1.S.51.4.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 line-end [0.034 μm \leq edge length $<$ 0.060 μm] in NMINP direction [PRL $>$ -0.020 μm .]	S51.,	\geq ,	0.0380.,
M1.S.51.4.2.PT.,	Space of M1 to M1 line-end [0.034 μm \leq edge length $<$ 0.060 μm , NOT INTERACT BLK_M1] in NMINP direction [PRL $>$ -0.020 μm .]	S51.,	\geq ,	0.0380.,
M1.S.51.5.1.PT.,	Space of M1 [NOT INTERACT BLK_M1] to M1 line-end [edge length = 0.060 μm] in NMINP direction [PRL $>$ -0.020 μm .]	S51.,	\geq ,	0.0380.,
M1.S.51.5.2.PT.,	Space of M1 to M1 line-end [edge length = 0.060 μm , NOT INTERACT BLK_M1] in NMINP direction [PRL $>$ -0.020 μm .]	S51.,	\geq ,	0.0380.,
M1.S.52.1.PT.,	Space of M1 to M1 line-end in MINP direction [PRL $>$ -0.060 μm .]	S52.,	\geq ,	0.0600.,
M1.S.61.1.PT.,	Corner projected space of M1 [-0.060 μm $<$ PRL \leq 0 μm .] (Except BLK_WB, or following conditions: .. 1. Corner with edge [length \leq 0.040 μm , between 2 consecutive 90-90 degree corners] on both sides).,	S61.,	\geq ,	0.0600.,
M1.L.2.1.PT.,	Edge length with adjacent edge [length $<$ 0.090 μm .] (Except BLK_M1).,	L2A.,	\geq ,	0.0800.,

Rule No..	Description..	Label..	Op..	Rule..
M1.A.2.PT..	Area of M1.. (Except BLK_M1)..	A2..	\geq ..	0.00280..
M1.R.1.PT..	{M1 NOT BLK_M1} must be a rectangle.. (Except SEALRING_ALL)..
M1.R.10.PT..	Overlap MetalFuse_B1(156,8) is not allowed..
M1.EN.31.1.PT..	Enclosure of square <u>Lower_VIA</u> [width = 0.020 μm] by M1 [width \leq 0.020 μm] for two opposite sides with the other two sides \geq 0.0000 μm	\geq ..	0.0300..
M1.EN.31.2.PT..	Enclosure of square <u>Lower_VIA</u> [width = 0.020 μm] by M1 [0.020 μm < width \leq 0.022 μm] for two opposite sides with the other two sides \geq 0.0010 μm	\geq ..	0.0300..
M1.EN.31.3.PT..	Enclosure of square <u>Lower_VIA</u> [width = 0.020 μm] by M1 [0.022 μm < width \leq 0.024 μm] for two opposite sides with the other two sides \geq 0.0020 μm .. (Except BLK_M1)..	..	\geq ..	0.03..
M1.EN.32.1.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.050 μm] by M1 [width \leq 0.020 μm] with the other two long sides \geq 0.0000 μm	\geq ..	0.0300..
M1.EN.32.2.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.050 μm] by M1 [0.020 μm < width \leq 0.022 μm] with the other two long sides \geq 0.0010 μm	\geq ..	0.0300..
M1.EN.32.3.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.050 μm] by M1 [0.022 μm < width \leq 0.024 μm] with the other two long sides \geq 0.0020 μm	\geq ..	0.0300..
M1.EN.33.1.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.034 μm] by M1 [width \leq 0.020 μm] with the other two long sides \geq 0.0000 μm	\geq ..	0.0300..
M1.EN.33.2.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.034 μm] by M1 [0.020 μm < width \leq 0.022 μm] with the other two long sides \geq 0.0010 μm	\geq ..	0.0300..
M1.EN.33.3.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.034 μm] by M1 [0.022 μm < width \leq 0.024 μm] with the other two long sides \geq 0.0020 μm .. (Except BLK_M1)..	..	\geq ..	0.0300..
M1.EN.34.1.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.060 μm] by M1 [width \leq 0.020 μm] with the other two long sides \geq 0.0000 μm	\geq ..	0.0300..
M1.EN.34.2.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.060 μm] by M1 [0.020 μm < width \leq 0.022 μm] with the other two long sides \geq 0.0010 μm	\geq ..	0.0300..
M1.EN.34.3.PT..	Short side enclosure of rectangular <u>Lower_VIA</u> [length = 0.060 μm] by M1 [0.022 μm < width \leq 0.024 μm] with the other two long sides \geq 0.0020 μm	\geq ..	0.0300..

4.5.74 HD MIM Layout Rules

- HD MIM is used for de-coupling capacitor.

4.5.74.1 Capacitor Top Metal Dummy Layer (CTMDMY) Layout Rules

- CTMDMY_n ($n = 7 \sim 14$) is a dummy layer (GDS layer: 148;n) for DRC/LVS to recognize the M(n) HD MIM region. “n” is the number of the 1st metal layer above HD MIM region. In other words, CTMDMY_n is defined the HD MIM dummy layer inserted between M(n) and M($n-1$).

For example: CTMDMY₉ is for the HD MIM region between M8 and M9 (refer to Fig. 4.3.1).

M(n) HD MIM must be fully covered by CTMDMY_n.

The corresponding M(n) should only be the M_{TOP} layer, since HD MIM can only be inserted between “M_{TOP} and M_{TOP-1}” .

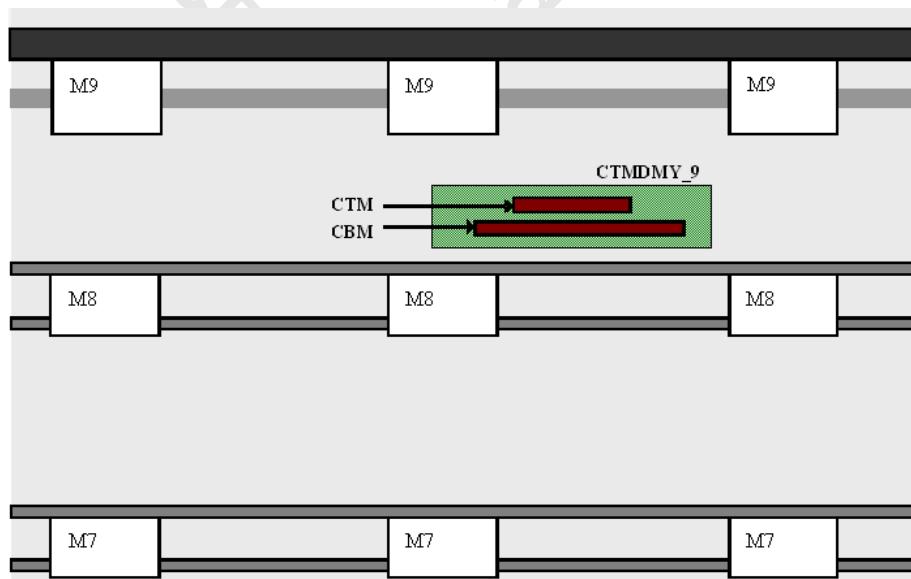


Fig. 4.3.1

Rule No.	Description	Label	Op.	Rule
CTMDMY.R.2	The corresponding M(n) of CTMDMY _n must be the M _{TOP-1} / M _{TOP} (Myz/Mz, Mz/Mz, Mr/Mr, Mz/Mr) layer.			

4.5.74.2 Capacitor Top Metal (CTM) Layout Rules (Mask ID: 182)

The HD MIM capacitance is defined by the CTM and CBM area. Individual CTM or CBM (i.e, dummy CTM or CBM) is not allowed. CTM_O (CAD layer: 77;1) is defined for CTM opening, and CTMFINAL = {CTM NOT CTM_O}, which is defined in the section 4.2.1.

Customer must provide the CAD layer (as below table) to perform the CTM logical operation for non-rectangular HD MIM patterns during CTM mask making process.

Layer Name	CAD Layer #	Description
CTM	77;0	CTM drawing layer
CTM_O	77;1	CTM Open Area (drawing layer)

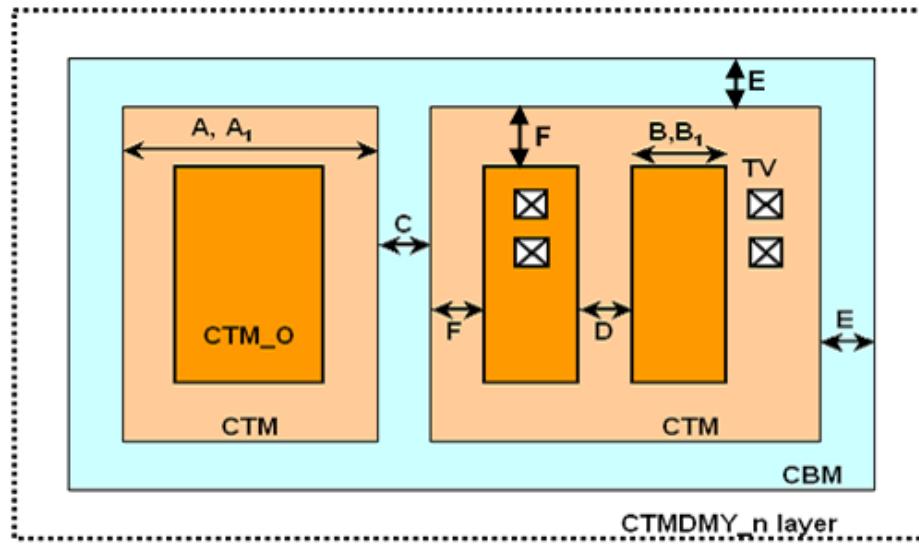
In this section, CTM layout rules are defined for both drawing layers (CTM, CTM_O) and mask logical operation (CTMFINAL).

Rule No.	Description	Label	Op.	Rule
CTM.W.1	Width	A	\geq	0.6000
CTM.W.2	Maximum width or length For example, 10 μm x 201 μm CTM is not allowed.	A1	\leq	200
CTM.W.3	Width of CTM_O	B	\geq	1.014
CTM.W.4	Maximum width or length of CTM_O	B1	\leq	10
CTM.S.1	Space	C	\geq	0.8000
CTM.S.2	Space of CTM_O	D	\geq	0.6000
CTM.A.1	Maximum total area of CTMFINAL in the whole chip		\leq	1.0E+08
CTM.EN.1.1	CTM [0.600 μm \leq width < 2 μm] enclosure by CBM	E	\geq	0.2000
CTM.EN.1.2	CTM [2 μm \leq width < 5 μm] enclosure by CBM	E	\geq	0.3000
CTM.EN.1.3	CTM [width \geq 5 μm] enclosure by CBM	E	\geq	0.4000
CTM.EN.2	Enclosure of CTM_O	F	\geq	0.6000
CTM.DN.1.2	Maximum CTMFINAL density across full chip		\leq	60%
CTM.R.1	CTM must be orthogonal to grid.			
CTM.R.1.1	CTM is not allowed to have any hole in CTM			
CTM.R.2	CTM must be inside CBM.			
CTM.R.3	CTM_O must be rectangular and orthogonal to grid. Other shapes are not allowed.			
CTM.R.4	CTM_O must be inside CTM.			
CTM.R.5	It is not allowed to have maximum delta V > 1.8V [between CTM and CBM] for one HD MIM capacitor.			

Table Notes:

Delta Voltage Calculation in high voltage spacing rules please refer to *T-N07-CL-DR-022* section 3.9.1 DRC methodology of net voltage recognition.

CTM and CTM_O



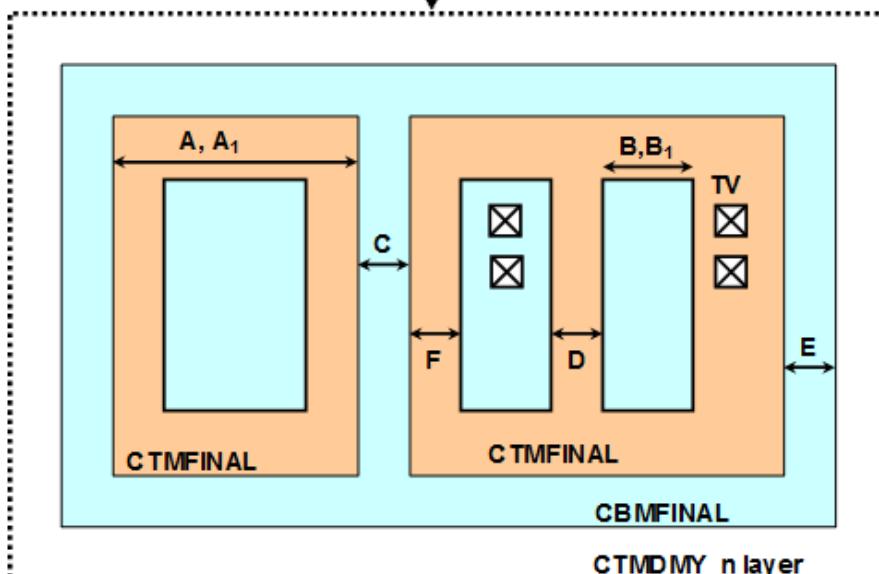
Top Plate Metal
CTM

Bottom Plate Metal
CBM

Top Plate Metal open area
CTM_O

Top VIA (VIAz/VIAr/VIAu)
TV

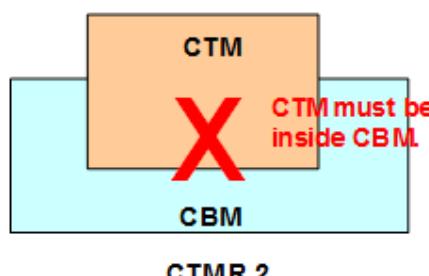
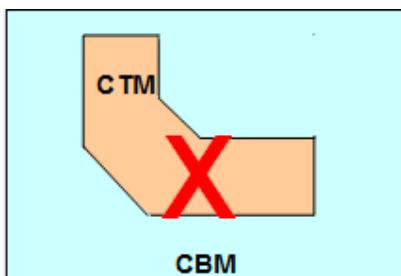
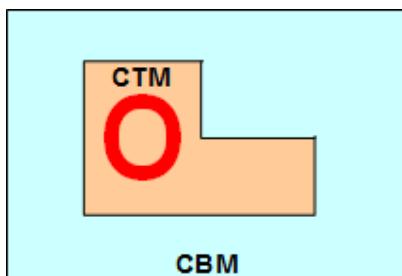
Logical Operation: **CTMFFINAL**



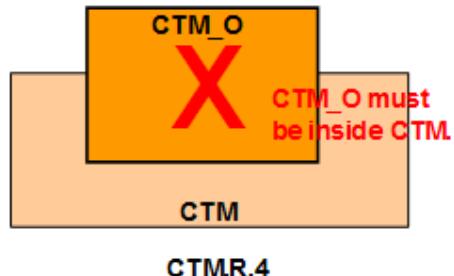
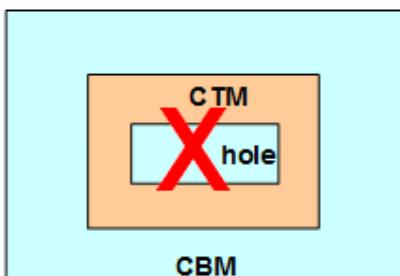
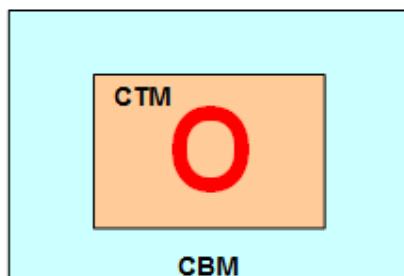
Top Plate Metal
CTMFFINAL

Bottom Plate Metal
CBMFINAL

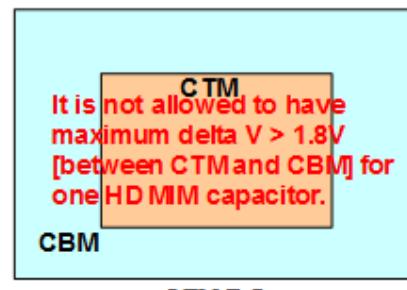
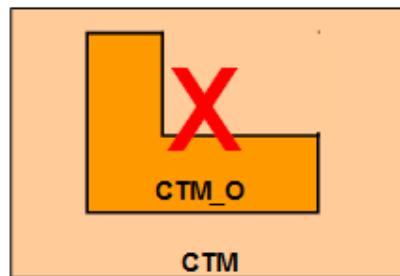
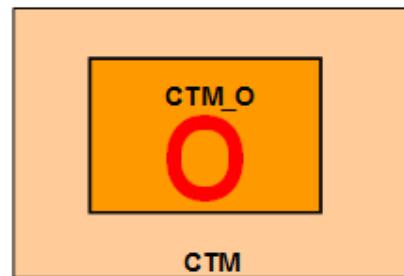
Top VIA (VIAz/VIAr/VIAu)
TV



CTMR.1



CTMR.1.1



CTMR.3

CTMR.5

4.5.74.3 Capacitor Bottom Metal (CBM) Layout Rules (Mask ID: 183)

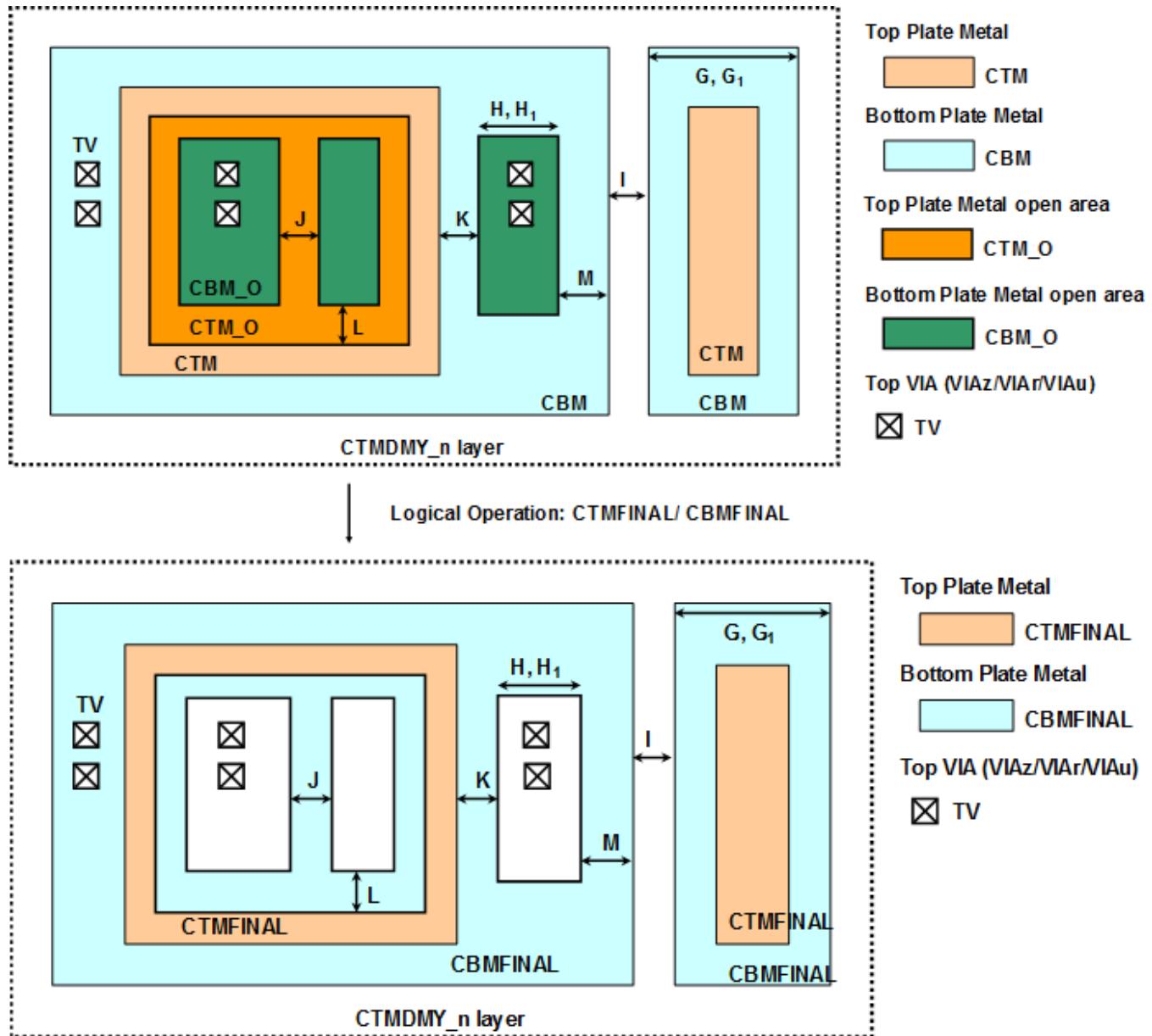
The HD MIM capacitance is defined by the CTM and CBM area. Individual CTM or CBM (i.e. dummy CTM or CBM) is not allowed. CBM_O (CAD layer: 88;1) is defined for CBM opening, and CBMFINAL = {CBM NOT CBM_O}, which is defined in 4.2.1.

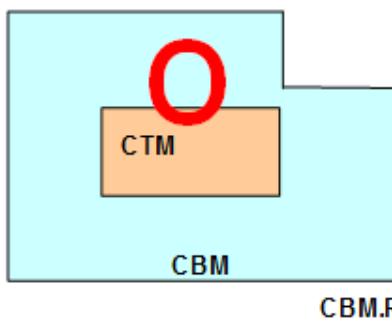
Customer must provide the CAD layer (as below table) to perform the CBM logical operation for non-rectangular HD MIM patterns during CBM mask making process.

Layer Name	CAD Layer #	Description
CBM	88;0	CBM drawing layer
CBM_O	88;1	CBM Open Area (drawing layer)

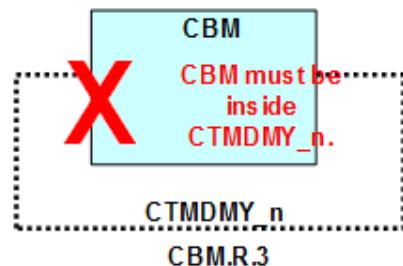
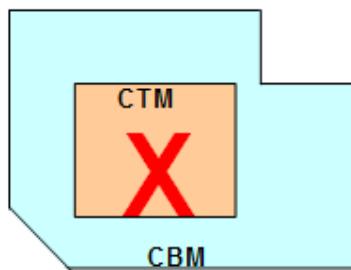
In this section, CBM layout rules are defined for both drawing layers (CBM, CBM_O) and mask logical operation (CBMFINAL).

Rule No.	Description	Label	Op.	Rule
CBM.W.1	Width	G	\geq	1
CBM.W.2	Maximum width or length For example, 10 μm x 211 μm CBM is not allowed.	G1	\leq	210
CBM.W.3	Width of CBM_O	H	\geq	1.5
CBM.W.4	Maximum width or length of CBM_O	H1	\leq	9
CBM.S.1	Space	I	\geq	1.5
CBM.S.2	Space of CBM_O	J	\geq	1
CBM.S.3	Space of CBM_O to CTM	K	\geq	0.4000
CBM.EN.1	CTM_O enclosure of CBM_O	L	\geq	0.4000
CBM.EN.2	Enclosure of CBM_O	M	\geq	1
CBM.DN.1.2	Maximum CBMFINAL density across full chip		\leq	60%
CBM.R.1 ^U	Circuits under HD MIM are allowed from process point of view. But the parasitic and signal coupling effects should be considered by designers.			
CBM.R.3	CBM must be inside CTMDMY_n.			
CBM.R.4	CBM must be orthogonal to grid.			
CBM.R.4.1	CBM is not allowed to have any hole in CBM			
CBM.R.5	CBM_O must be rectangular and orthogonal to grid. Other shapes are not allowed.			
CBM.R.6	CBM_O must be inside CBM.			
CBM.R.7	{CBM_O INTERACT CTM} must be inside CTM_O.			

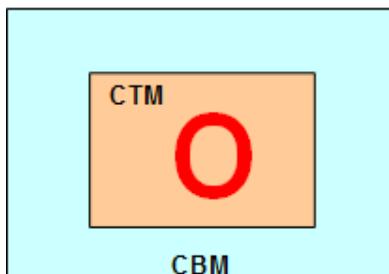
CBM and CBM_O



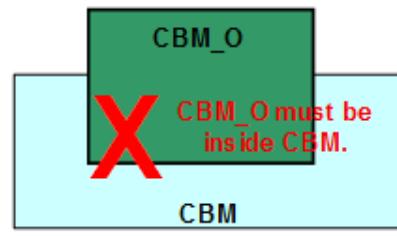
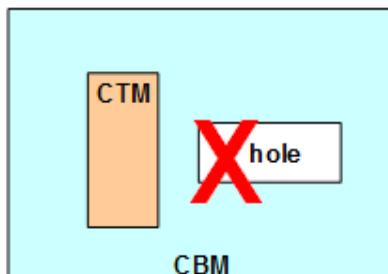
CBM.R.4



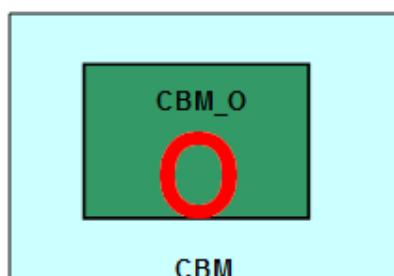
CBM.R.3



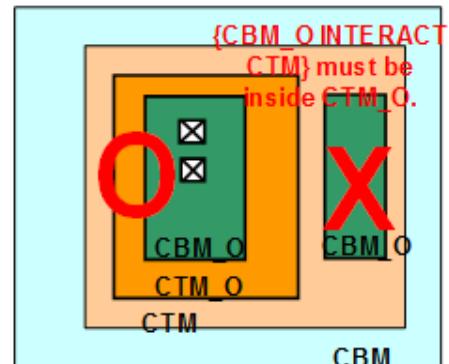
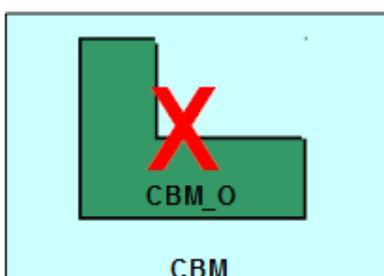
CBM.R.4.1



CBM.R.6



CBM.R.5



CBM.R.7

4.5.74.4 TV Layout Rules for HD MIM

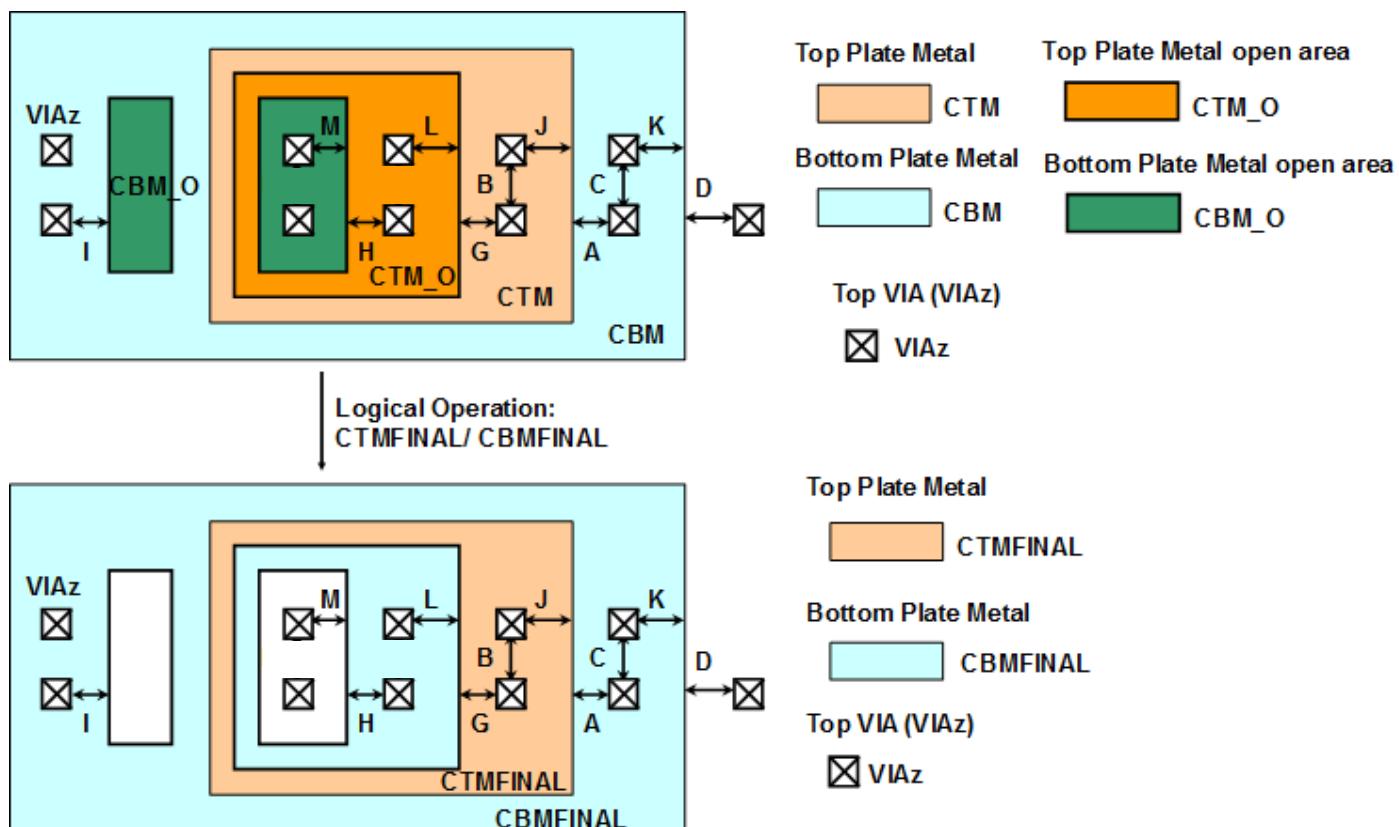
In this section, VIAz/ VIAr layers are the top VIA above CTM or CBM. Except following the VIAz/ VIAr rules in T-N07-CL-DR-022 section 4.5, you also need to meet the following specific rules which are related to HD MIM.

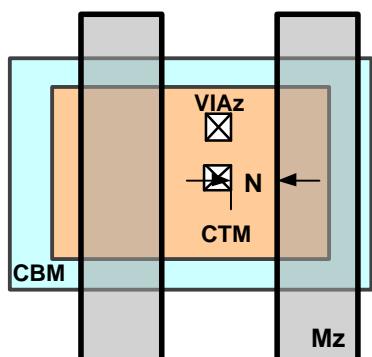
4.5.74.4.1 VIAz Layout Rules for HD MIM

Rule No.	Description	Label	Op.	Rule
MIM.VIAz.S.1.1	Space of VIAz [INSIDE CBM but OUTSIDE CTM] to CTM [corresponding width < 2 μm].	A	\geq	0.2400
MIM.VIAz.S.1.2	Space of VIAz [INSIDE CBM but OUTSIDE CTM] to CTM [2 μm \leq corresponding width < 5 μm].	A	\geq	0.2700
MIM.VIAz.S.1.3	Space of VIAz [INSIDE CBM but OUTSIDE CTM] to CTM [corresponding width \geq 5 μm].	A	\geq	0.3000
MIM.VIAz.S.2	Space of VIAz inside {CTM NOT CTM_O}.	B	\geq	0.4860
MIM.VIAz.S.3	Space of VIAz inside {CBM NOT CBM_O}.	C	\geq	0.4860
MIM.VIAz.S.4.1	Space of VIAz [OUTSIDE CBM] to CBM [corresponding width < 2 μm].	D	\geq	0.2650
MIM.VIAz.S.4.2	Space of VIAz [OUTSIDE CBM] to CBM [corresponding width < 2 μm] [maximum delta V > 1.32V] (1.2V + 10%).	D	\geq	0.3000
MIM.VIAz.S.4.3	Space of VIAz [OUTSIDE CBM] to CBM [2 μm \leq corresponding width < 5 μm].	D	\geq	0.4000
MIM.VIAz.S.4.4	Space of VIAz [OUTSIDE CBM] to CBM [corresponding width \geq 5 μm].	D	\geq	0.5000
MIM.VIAz.S.7	Space of VIAz [INSIDE CTM but OUTSIDE CTM_O] to CTM_O.	G	\geq	0.2400
MIM.VIAz.S.8	Space of VIAz [INSIDE CTM_O but OUTSIDE CBM_O] to CBM_O.	H	\geq	0.2000
MIM.VIAz.S.9	Space of VIAz [INSIDE CBM [NOT INSIDE CTM_O] but OUTSIDE CBM_O] to CBM_O.	I	\geq	0.2000
MIM.VIAz.S.10®	Space of VIAz [INSIDE CTMFINAL] to under metal (Mz/Myz) [the first metal layer below HD MIM]. (Overlap is not allowed)	N	\geq	0.0720
MIM.VIAz.S.10.1	Space of VIAz [INSIDE CTMFINAL] to under dummy metal (Mz/Myz) [the first metal layer below HD MIM]. (Overlap is not allowed)	N2	\geq	0.1000
MIM.VIAz.S.10.2®	VIAz [INSIDE {CBMFFINAL NOT CTMFFINAL}] space to under metal (Mz/Myz) [the first metal layer below HD MIM, with different net]. (Overlap is not allowed)	O1	\geq	0.0720
MIM.VIAz.S.12	Space of VIAz [INSIDE CTMFINAL] to under metal (Mz/Myz) [the first metal layer below HD MIM]. (Overlap is not allowed)	N1	\geq	0.0500
MIM.VIAz.S.13	Space of VIAz [INSIDE {CBMFFINAL NOT CTMFFINAL}] to under metal (Mz/Myz) [the first metal layer below HD MIM, with different net]. (Overlap is not allowed)	N1	\geq	0.0500
MIM.VIAz.EN.1.1	Enclosure by CTM [corresponding width < 2 μm]	J	\geq	0.2000
MIM.VIAz.EN.1.2	Enclosure by CTM [corresponding width \geq 2 μm]	J	\geq	0.2400
MIM.VIAz.EN.2	Enclosure by CBM (Cut is not allowed)	K	\geq	0.2000
MIM.VIAz.EN.3	Enclosure by CTM_O	L	\geq	0.3000
MIM.VIAz.EN.4	Enclosure by CBM_O	M	\geq	0.5000
MIM.VIAz.R.1	Single VIAz inside CTMFINAL or {CBMFFINAL NOT CTMFFINAL} is not allowed.			
MIM.VIAz.R.2®	Space of VIAz [INSIDE CTMFINAL] to under metal (Mz/Myz) [the first metal layer below HD MIM, space < 0.468 μm] must be equal at both side of VIAz.			
MIM.VIAz.R.2.1®	VIAz [INSIDE {CBMFFINAL NOT CTMFFINAL}] space to under metal (Mz/Myz) [the first metal layer below HD MIM, space < 0.468 μm] must be equal at both side of VIAz.			
MIM.VIAz.R.3	VIAz [INSIDE CBMFFINAL] must be fully covered by {CBMFFINAL AND Mz+1}			

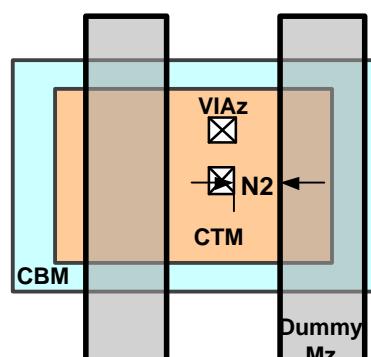
MIM.VIAz.R.4

VIAz cut CTM is not allowed

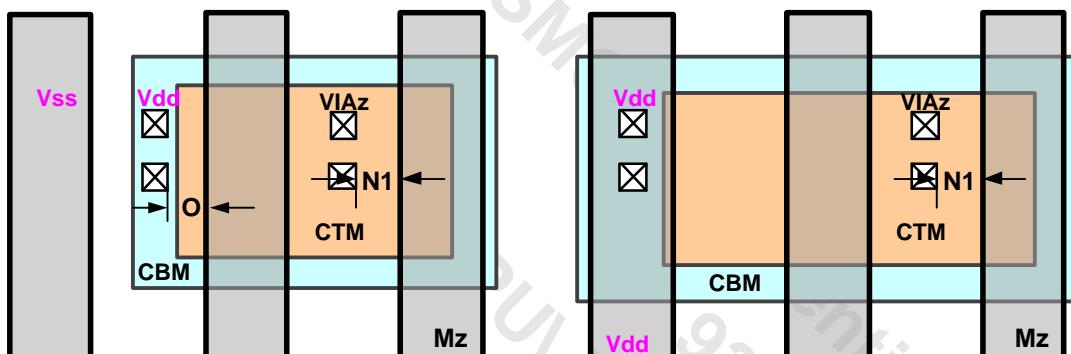




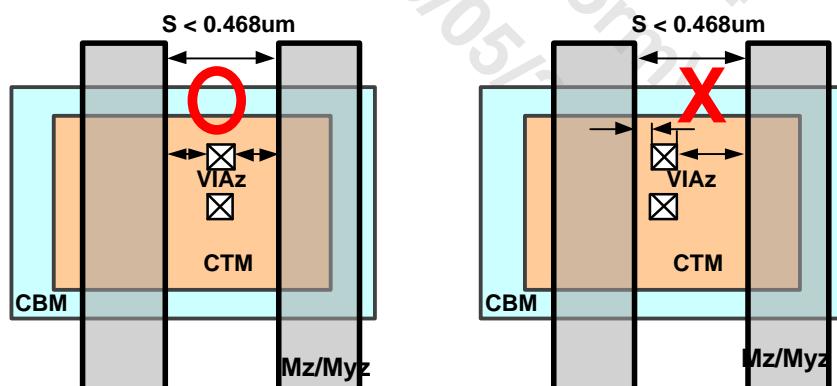
MIM.VIAz.S.10®



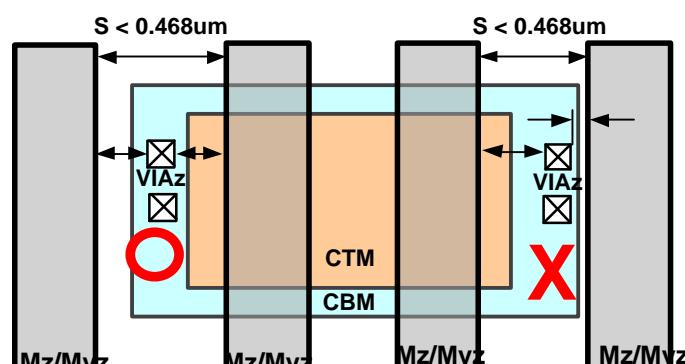
MIM.VIAz.S.10.1



MIM.VIAz.S.12/MIM.VIAz.S.13



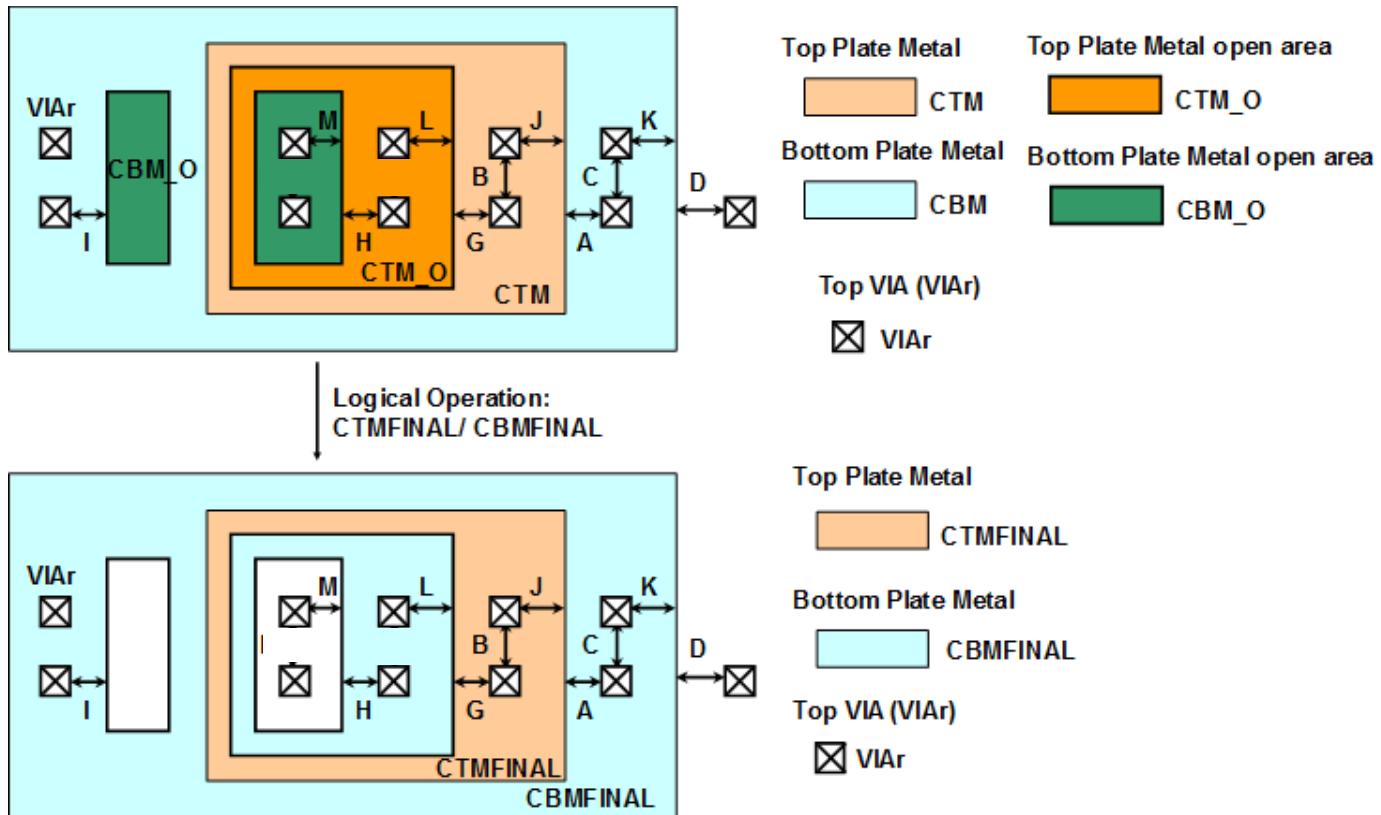
MIM.VIAz.R.2®

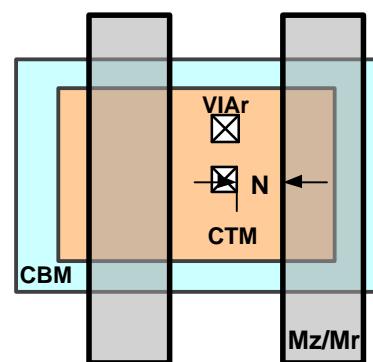


MIM.VIAz.R.2.1®

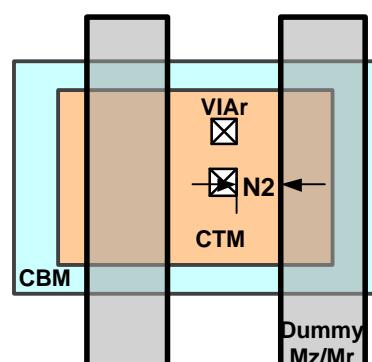
4.5.74.4.2 VIAr Layout Rules for HD MIM

Rule No.	Description	Label	Op.	Rule
MIM.VIAr.S.1.1	Space of VIAr [INSIDE CBM but OUTSIDE CTM] to CTM [corresponding width < 2 μm].	A	\geq	0.2400
MIM.VIAr.S.1.2	Space of VIAr [INSIDE CBM but OUTSIDE CTM] to CTM [2 μm \leq corresponding width < 5 μm].	A	\geq	0.2700
MIM.VIAr.S.1.3	Space of VIAr [INSIDE CBM but OUTSIDE CTM] to CTM [corresponding width \geq 5 μm].	A	\geq	0.3000
MIM.VIAr.S.2	Space of VIAr inside {CTM NOT CTM_O}.	B	\geq	0.5940
MIM.VIAr.S.3	Space of VIAr inside {CBM NOT CBM_O}.	C	\geq	0.5940
MIM.VIAr.S.4.1	Space of VIAr [OUTSIDE CBM] to CBM [corresponding width < 2 μm].	D	\geq	0.2650
MIM.VIAr.S.4.2	Space of VIAr [OUTSIDE CBM] to CBM [corresponding width < 2 μm] [maximum delta V > 1.32V] (1.2V + 10%).	D	\geq	0.3000
MIM.VIAr.S.4.3	Space of VIAr [OUTSIDE CBM] to CBM [2 μm \leq corresponding width < 5 μm].	D	\geq	0.4000
MIM.VIAr.S.4.4	Space of VIAr [OUTSIDE CBM] to CBM [corresponding width \geq 5 μm].	D	\geq	0.5000
MIM.VIAr.S.7	Space of VIAr [INSIDE CTM but OUTSIDE CTM_O] to CTM_O.	G	\geq	0.2400
MIM.VIAr.S.8	Space of VIAr [INSIDE CTM_O but OUTSIDE CBM_O] to CBM_O.	H	\geq	0.2000
MIM.VIAr.S.9	Space of VIAr [INSIDE CBM but OUTSIDE CBM_O] to CBM_O.	I	\geq	0.2000
MIM.VIAr.S.10®	Space of VIAr [INSIDE CTMFINAL] to under metal (Mz/Mr) [the first metal layer below HD MIM]. (Overlap is not allowed)	N	\geq	0.0720
MIM.VIAr.S.10.1	Space of VIAr [INSIDE CTMFINAL] to under dummy metal (Mz/Mr) [the first metal layer below HD MIM]. (Overlap is not allowed)	N2	\geq	0.1000
MIM.VIAr.S.10.2®	VIAr [INSIDE {CBMFFINAL NOT CTMFFINAL}] space to under metal (Mz/Mr) [the first metal layer below HD MIM, with different net]. (Overlap is not allowed)	O1	\geq	0.0720
MIM.VIAr.S.12	Space of VIAr [INSIDE CTMFINAL] to under metal (Mz/Mr) [the first metal layer below HD MIM]. (Overlap is not allowed)	N1	\geq	0.0500
MIM.VIAr.S.13	Space of VIAr [INSIDE {CBMFFINAL NOT CTMFFINAL}] to under metal (Mz/Mr) [the first metal layer below HD MIM, with different net]. (Overlap is not allowed)	N1	\geq	0.0500
MIM.VIAr.EN.1.1	Enclosure by CTM [corresponding width < 2 μm]	J	\geq	0.2000
MIM.VIAr.EN.1.2	Enclosure by CTM [corresponding width \geq 2 μm]	J	\geq	0.2400
MIM.VIAr.EN.2	Enclosure by CBM (Cut is not allowed)	K	\geq	0.2000
MIM.VIAr.EN.3	Enclosure by CTM_O	L	\geq	0.3000
MIM.VIAr.EN.4	Enclosure by CBM_O	M	\geq	0.5000
MIM.VIAr.R.1	Single VIAr inside CTMFINAL or {CBMFFINAL NOT CTMFFINAL} is not allowed.			
MIM.VIAr.R.2®	Space of VIAr [INSIDE CTMFINAL] to under metal (Mz/Mr) [the first metal layer below HD MIM, space < 0.558 μm] must be equal at both side of VIAr.			
MIM.VIAr.R.2.1®	VIAr [INSIDE {CBMFFINAL NOT CTMFFINAL}] space to under metal (Mz/Mr) [the first metal layer below HD MIM, space < 0.558 μm] must be equal at both side of VIAr.			
MIM.VIAr.R.3	VIAr [INSIDE CBMFFINAL] must be fully covered by {CBMFFINAL AND Mr+1}			
MIM.VIAr.R.4	VIAr cut CTM is not allowed			

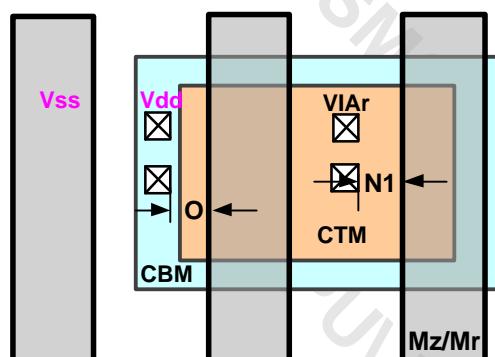




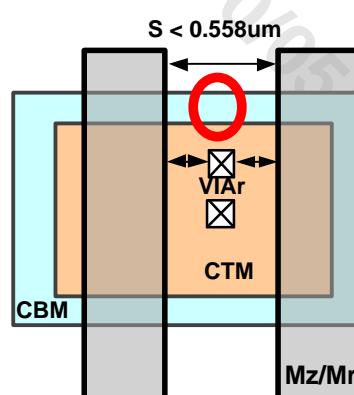
MIM.VIAr.S.10®



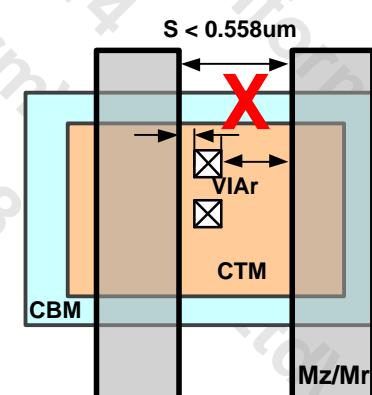
MIM.VIAr.S.10.1



MIM.VIAr.S.12/MIM.VIAr.S.13



MIM.VIAr.R.2®



MIM.VIAr.R.2.1®

4.5.74.5 TM Layout Rules for HD MIM

Mz/Mr layers are the top metal which might be the first metal layer above the HD MIM capacitor and connect to CTM or CBM.

TSMC Confidential Information
938214
VIAI CPU Platform\ Col. I Ltd.
10/05/2018

4.5.74.6 Antenna Effect Prevention Design Rules for HD MIM

4.5.74.6.1 HD MIM Structures With The Antenna Effect

The antenna effect should be taken into consideration for the HD MIM capacitor design. The layout style of the HD MIM capacitor routing will impact its immunity to the antenna effect during FAB process. Antenna rules are defined separately for the various metallization options.

4.5.74.6.1.1 Terminology

- “**Floating**” defines as below:

CTM or CBM node is not connected to any OD or poly gate region.

- “**Grounded**” defines as below:

CTM or CBM node is connected to OD region.

- “**Balanced structures**” defines as below:

Both CTM and CBM nodes are floating or connected to ground (including protection diode) through the same metal path (i.e. Mz, Mr, or AP-MD) after HD MIM structure is formed. Please refer to Fig.

4.5.74.6.1.

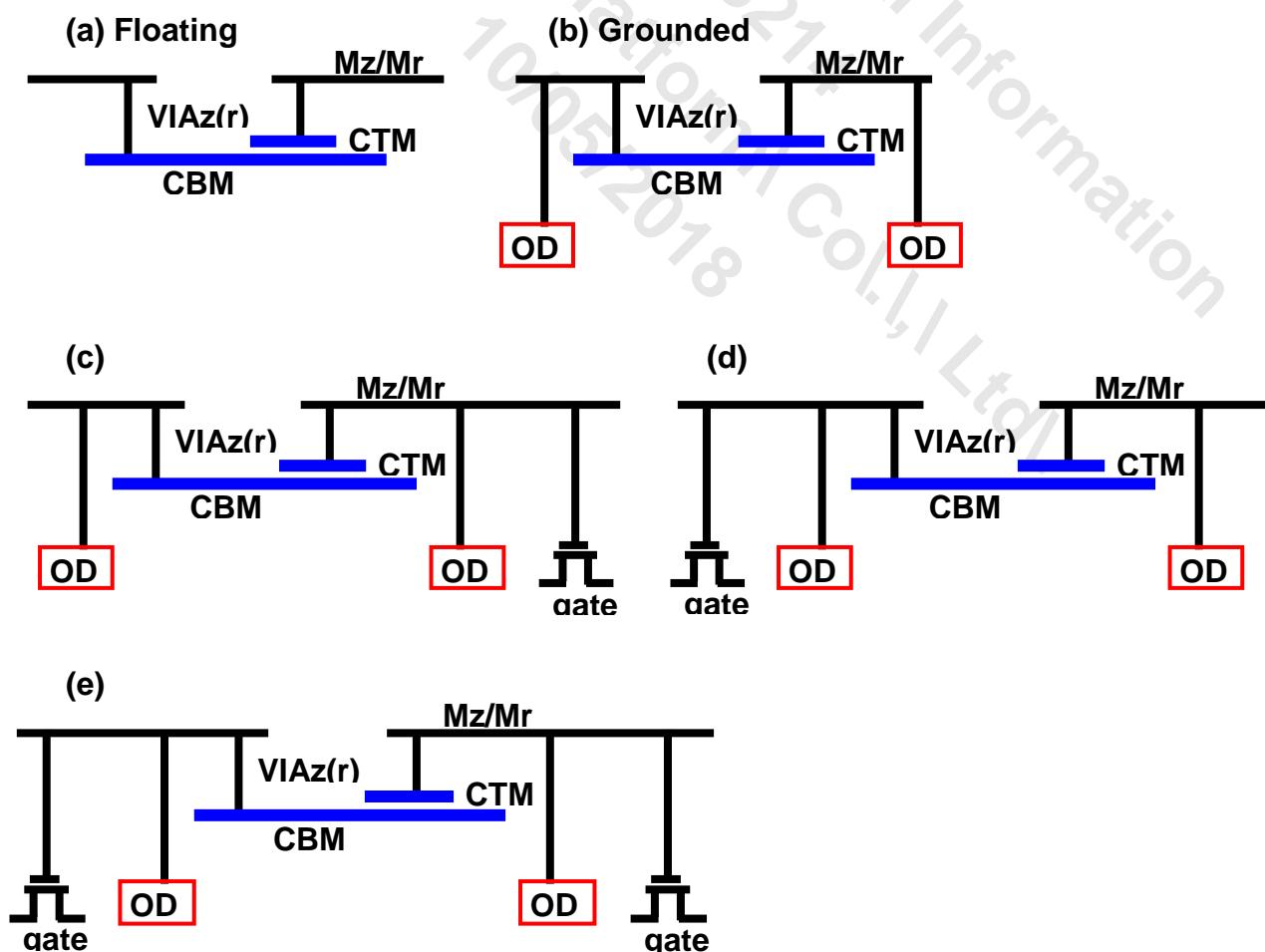


Fig. 4.5.74.6.1 Examples of balanced structures

- “Unbalanced structures” defines as below:
- If one node of the HD MIM capacitor is connected to OD, but the other node is not connected to OD at the same metal layer. Please refer to Fig. 4.5.74.6.2.
- If any node of the HD MIM capacitor is connected to gate but without protection OD.
- Unbalanced structures are not allowed.

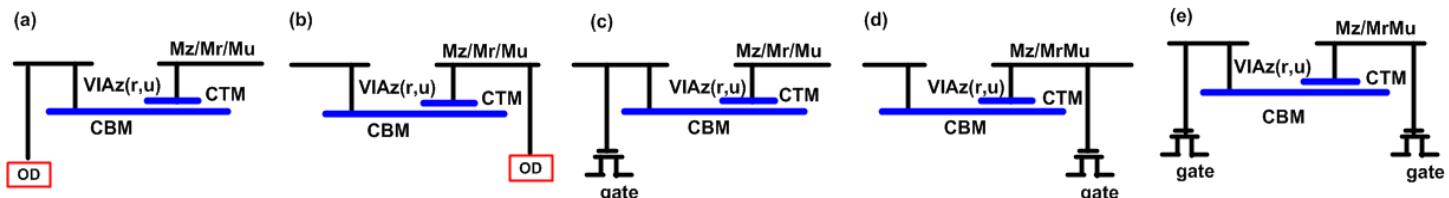


Fig. 4.5.74.6.2 Examples of unbalanced structures

4.5.74.6.1.2 HD MIM Structure Recognition Methodology

Below tables are for clear definition of balanced and unbalanced HD MIM structure.

A, B: Two terminals of HD MIM

All structures = Balanced (float) + Balanced (OD) + Unbalanced

Table 4.5.74.6.1.1.2.1 One metal layer above HD MIM

1st A, B	Metal Structure Unity	In TSMC
Both A, B floating	Balanced (float)	Allowed
Both A, B connect to OD	Balanced (OD)	Allowed
Other combinations	Unbalanced	Not allowed

Check Methods

- For only one metal (Mz, Mr) above the HD MIM capacitor:

Refer to Fig. 4.5.74.6.1 and Fig. 4.5.74.6.2 to check HD MIM structure is balanced or unbalanced.

4.5.74.6.2 Antenna Effect Prevention Layout Rules

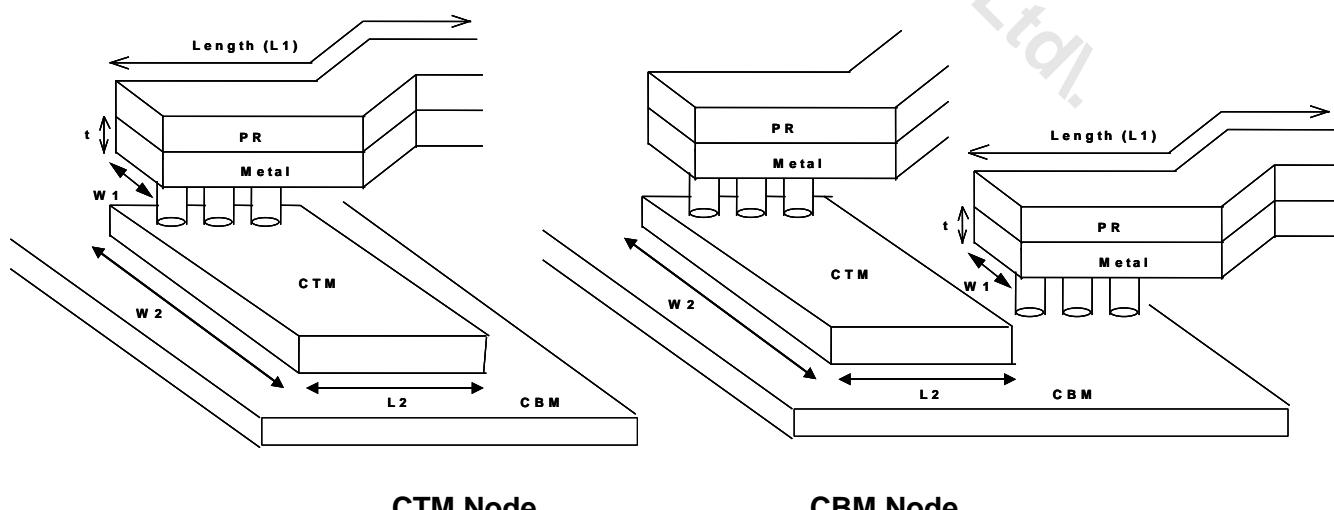
The rules are for the metal layer and VIA layer above the CTM and CBM. By taking “1P9M where M8 and M9 are Mz, and HD MIM is inserted between M8 and M9” as an example, the antenna effect of VIA8/ M9 to the HD MIM capacitors needs to be considered.

Rule No.	Description	Label	Op.	Rule
MIM.A.R.1	Unbalanced structure is not allowed.			
MIM.A.R.2	Maximum ratio of the cumulative metal area and AP-MD sidewall area to the HD MIM capacitor for balanced structure when both CTM and CBM are floating.		≤	1000
MIM.A.R.3	Maximum ratio of the cumulative metal area and AP-MD sidewall area to the HD MIM capacitor for balanced structure when both CTM and CBM are connected to OD.		≤	OD area x 8000 + 1000
MIM.A.R.4	Maximum ratio of the cumulative VIA and RV area to the HD MIM capacitor for balanced structure when both CTM and CBM are floating.		≤	20
MIM.A.R.5	Maximum ratio of the cumulative VIA and RV area to the HD MIM capacitor for balanced structure when both CTM and CBM are connected to OD.		≤	OD area x 210 + 20

Definition of Antenna Ratio

Different antenna ratio formulas are defined for Cu and AP-MD due to the process differences.

Metal Layer	HD MIM node	Drawn Ratio Formula	Definition
Cu Antenna (Mz, Mr, MD)	CTM node	{ total (L1 x W1) } / (W2 x L2)	L1: metal length connected to CTM W1: metal width connected to CTM W2: connected CTM width L2: connected CTM length
	CBM node	{ total (L1 x W1) } / (W2 x L2)	L1: metal length connected to CBM W1: metal width connected to CBM W2: connected CTM width L2: connected CTM length
VIA Antenna	CTM node	{ total VIA area } / (W2 x L2)	total VIA area connected to CTM W2: connected CTM width L2: connected CTM length
	CBM node	{ total VIA area } / (W2 x L2)	total VIA area connected to CBM W2: connected CTM width L2: connected CTM length
AP-MD Antenna	CTM node	2 [total (L1 +W1) x t] / (W2 x L2)	L1: metal length connected to CTM W1: metal width connected to CTM t : metal thickness of AP-MD W2: connected CTM width L2: connected CTM length
	CBM node	2 [total (L1 +W1) x t] / (W2 x L2)	L1: metal length connected to CBM W1: metal width connected to CBM t : metal thickness of AP-MD W2: connected CTM width L2: connected CTM length
RV Antenna	CTM node	{ total RV area } / (W2 x L2)	total RV area connected to CTM W2: connected CTM width L2: connected CTM length
	CBM node	{ total RV area } / (W2 x L2)	total RV area connected to CBM W2: connected CTM width L2: connected CTM length



CTM Node

CBM Node

4.5.74.7 Keep-out Zone Layout Rules for HD MIM Capacitor

For thermal-mechanical reliability concern, HD MIM capacitors are needed to be away from die corner/edge. The keep-out zone (KOZ) rules are defined in this section related to HD MIM.

- The rules listed in this section are the dimensions for N7+ ELK Cu process.

Rule No.	Description	Label	Op.	Rule
KOZ.R.1	<p>It is not allowed to have any CTM/CBM in the MIM KOZ (keep-out zone) at chip corner region for eutectic bump. (Figure 4.5.2)</p> <p>Definition of KOZ at chip corner region: A KOZ is determined by Chip_Boundary size, minimum enclosure of UBM by Chip_Boundary edge (Q in Figure 4.5.1) and minimum bump pitch (P in Table 4.5.1). The width (A) of KOZ at chip corner region follows the formula in Table 4.5.2.</p> <ul style="list-style-type: none"> Minimum enclosure of UBM by Chip_Boundary edge (Q) for eutectic bump = 50 μm. (Please refer to pad rule) 	A	=	Figure 4.5.1 Table 4.5.1 Table 4.5.2
KOZ.R.2	<p>It is not allowed to have any CTM/CBM in the MIM KOZ (keep-out zone) at chip edge region for eutectic bump. (Figure 4.5.2)</p> <p>Definition of KOZ at chip edge region: A KOZ is determined by Chip_Boundary size, minimum enclosure of UBM by Chip_Boundary edge (Q in Figure 4.5.1), and minimum bump pitch (P in Table 4.5.1). The width (B) of KOZ at chip edge region follows the formula in Table 4.5.2.</p> <ul style="list-style-type: none"> Minimum enclosure of UBM by Chip_Boundary edge (Q) for eutectic bump = 50 μm. (Please refer to pad rule) 	B	=	Figure 4.5.1 Table 4.5.1 Table 4.5.2
KOZ.R.3	<p>It is not allowed to have any CTM/CBM in the MIM KOZ (keep-out zone) at chip corner region for lead-free bump. (Figure 4.5.2)</p> <p>Definition of KOZ at chip corner region: A KOZ is determined by Chip_Boundary size, minimum enclosure of UBM by Chip_Boundary edge (Q in Figure 4.5.2), and minimum bump pitch (P in Table 4.5.3). The width (A) of KOZ at chip corner region follows the formula in Table 4.5.4.</p> <ul style="list-style-type: none"> Minimum enclosure of UBM by Chip_Boundary edge (Q) for lead-free bump = 50 μm. (Please refer to pad rule) 	A	=	Figure 4.5.2 Table 4.5.3 Table 4.5.4
KOZ.R.4	<p>It is not allowed to have any CTM/CBM in the MIM KOZ (keep-out zone) at chip edge region for lead-free bump. (Figure 4.5.2)</p> <p>Definition of KOZ at chip edge region: A KOZ is determined by Chip_Boundary size, minimum enclosure of UBM by Chip_Boundary edge (Q in Figure 4.5.2), and minimum bump pitch (P in Table 4.5.3). The width (B) of KOZ at chip edge region follows the formula in Table 4.5.4.</p> <ul style="list-style-type: none"> Minimum enclosure of UBM by Chip_Boundary edge (Q) for lead-free bump = 50 μm. (Please refer to pad rule) 	B	=	Figure 4.5.2 Table 4.5.3 Table 4.5.4

Rule No.	Description	Label	Op.	Rule
KOZ.R.5	<p>It is not allowed to have any CTM/CBM in the MIM KOZ (keep-out zone) at chip corner region for Cu bump on pad. (Figure 4.5.3)</p> <p>Definition of KOZ at chip corner region: A KOZ is determined by Chip_Boundary size, minimum enclosure of UBM by Chip_Boundary edge (Q2/Q3 in Figure 4.5.3), and minimum bump pitch (P in Table 4.5.5). The width (A2/A3) of KOZ at chip corner region follows the formula in Table 4.5.6</p> <p>Minimum enclosure of UBM by Chip_Boundary edge in the horizontal direction (Q2) for Cu bump on pad = 39 μm.</p> <ul style="list-style-type: none"> • Minimum enclosure of UBM by Chip_Boundary edge in the vertical direction (Q3) for Cu bump on pad = 50 μm. (Please refer to pad rule) 	A	=	Figure 4.5.3 Table 4.5.5 Table 4.5.6
KOZ.R.6	<p>It is not allowed to have any CTM/CBM in the MIM KOZ (keep-out zone) at chip edge region for Cu bump on pad. (Figure 4.5.3)</p> <p>Definition of KOZ at chip edge region: A KOZ is determined by Chip_Boundary size, minimum enclosure of UBM by Chip_Boundary edge (Q2/Q3 in Figure 4.5.3), and minimum bump pitch (P in Table 4.5.5). The width (B2/B3) of KOZ at chip edge region follows the formula in Table 4.5.6.</p> <p>Minimum enclosure of UBM by Chip_Boundary edge in the horizontal direction (Q2) for Cu bump on pad = 39 μm.</p> <ul style="list-style-type: none"> • Minimum enclosure of UBM by Chip_Boundary edge in the vertical direction (Q3) for Cu bump on pad = 50 μm. (Please refer to pad rule) 	B	=	Figure 4.5.3 Table 4.5.5 Table 4.5.6
KOZ.R.7	<p>It is not allowed to have any CTM/CBM in the MIM KOZ (keep-out zone) at chip corner region for ubump. (Figure 4.5.6)</p> <p>Definition of KOZ at chip corner region: A KOZ is determined by Chip_Boundary size, minimum enclosure of UBM by Chip_Boundary edge (Q in Figure 4.5.1) and minimum bump pitch (P in Table 4.5.7). The width (A) of KOZ at chip corner region follows the formula in Table 4.5.8.</p> <p>Minimum enclosure of UBM by Chip_Boundary edge (Q) for ubump = 70 μm. (Please refer to pad rule)</p>	A	=	Figure 4.5.1 Figure 4.5.6 Table 4.5.7 Table 4.5.8
KOZ.R.8	<p>It is not allowed to have any CTM/CBM in the MIM KOZ (keep-out zone) at chip edge region for ubump. (Figure 4.5.6)</p> <p>Definition of KOZ at chip edge region: A KOZ is determined by Chip_Boundary size, minimum enclosure of UBM by Chip_Boundary edge (Q in Figure 4.5.1), and minimum bump pitch (P in Table 4.5.7). The width (B) of KOZ at chip edge region follows the formula in Table 4.5.8.</p> <p>Minimum enclosure of UBM by Chip_Boundary edge (Q) for ubump = 70 μm. (Please refer to pad rule)</p>	B	=	Figure 4.5.1 Figure 4.5.6 Table 4.5.7 Table 4.5.8

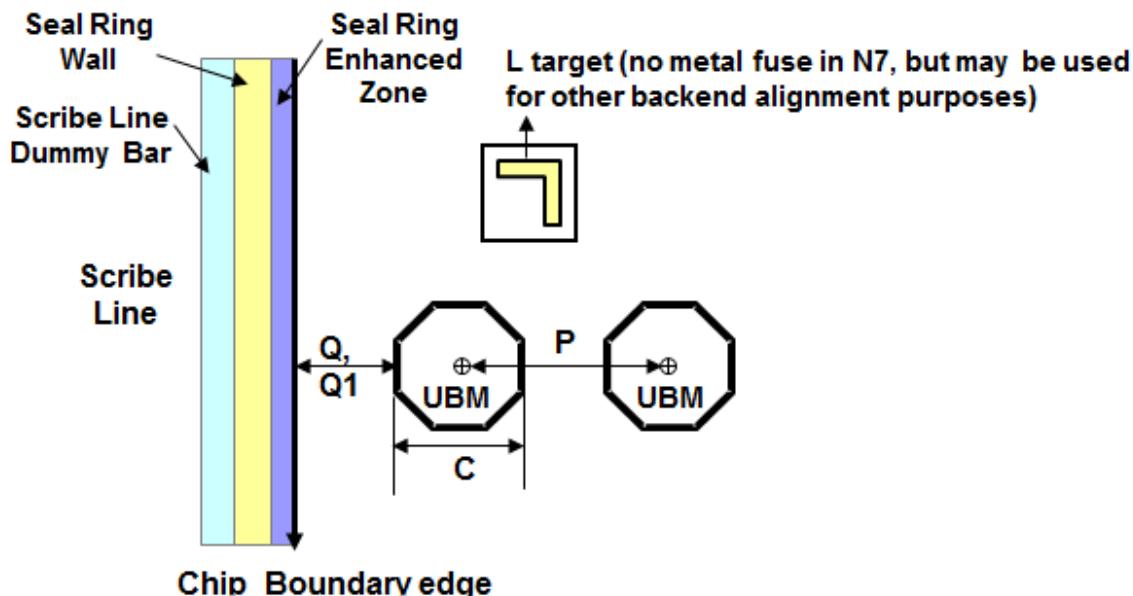


Figure 4.5.1 Schematic diagram for eutectic bump and lead-free bump

Table 4.5.1 Chip_Boundary size to bump pitch rule for eutectic bump.

The design rule dimensions (Layout) for N7+ are the same as on-silicon (On-Si) dimensions. (All numbers are **on-silicon dimensions** within $\pm 1 \mu\text{m}$ tolerance for bump pitch)

On design / silicon dimension (μm)	Chip_Boundary size (mm^2)	Area ≤ 100	$100 < \text{Area} \leq 225$	$225 < \text{Area} \leq 400$	$400 < \text{Area} \leq 625$	Area > 625
	Bump pitch ^a (P) (μm)	≥ 150	≥ 160	≥ 170	≥ 180	Contact TSMC ^b

Note:

- a. Bump pitch = UBM pitch.
- b. When the Chip_Boundary size falls into "Contact TSMC" area, please contact TSMC for a joint assessment.

Table 4.5.2 Chip_Boundary size to dimension of KOZ at chip corner and chip edge regions for eutectic bump.

The design rule dimensions (Layout) for N7+ are the same as on-silicon (On-Si) dimensions. (All numbers are **on-silicon dimensions** within $\pm 1 \mu\text{m}$ tolerance for bump pitch)

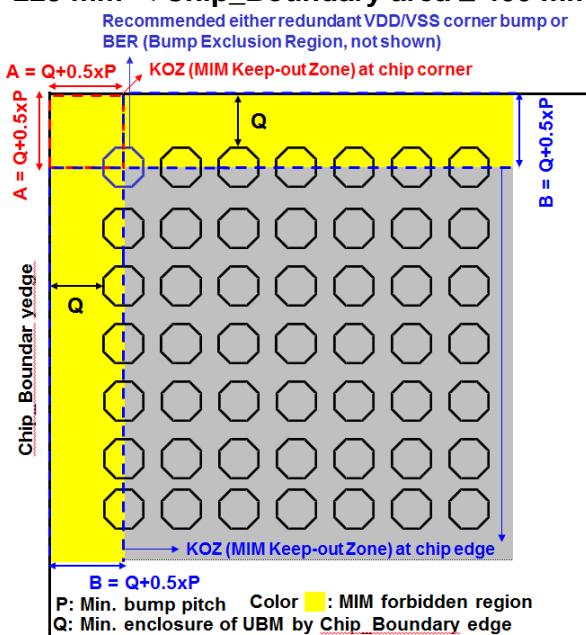
Chip_Boundary size on design / silicon dimension (mm^2)	Area ≤ 100	$100 < \text{Area} \leq 225$	$225 < \text{Area} \leq 400$	$400 < \text{Area} \leq 625$	Area > 625
Dimension of KOZ ^a at chip corner region (A) (μm)	$A = Q + 0.5 \times P^b$	$A = Q + 0.5 \times P^b$	$A = Q + 0.5 \times P^b$	$A = Q + 1 \times P^b$	Contact TSMC ^c
Dimension of KOZ ^a at chip edge region (B) (μm)	$B = Q + 0.5 \times P^b$	$B = Q + 0.5 \times P^b$	$B = Q + 0.5 \times P^b$	$B = Q + 1 \times P^b$	Contact TSMC ^c

Note:

- a. KOZ is MIM keep-out zone.
- b. (1) P: Minimum bump pitch. (2) Q: Minimum enclosure of UBM by Chip_Boundary edge.
- c. When the Chip_Boundary size falls into "Contact TSMC" area, please contact TSMC for a joint assessment.
 - The figure shows the DRC check zones for MIM KOZ (Keep-out Zone).
 - The following Chip_Boundary sizes are "Design / Silicon Dimension".

Chip_Boundary area $\leq 100 \text{ mm}^2$

$100 \text{ mm}^2 < \text{Chip_Boundary area} \leq 225 \text{ mm}^2$
 $225 \text{ mm}^2 < \text{Chip_Boundary area} \leq 400 \text{ mm}^2$



$400 \text{ mm}^2 < \text{Chip_Boundary area} \leq 625 \text{ mm}^2$

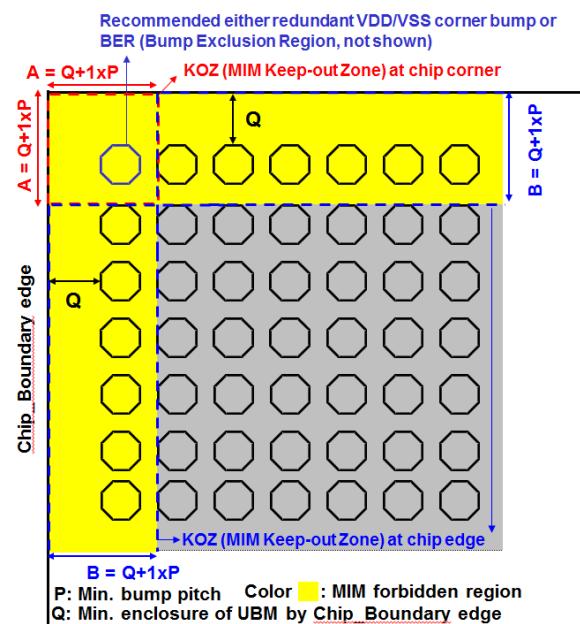


Figure 4.5.2 Schematic diagram for KOZ.R.1 and KOZ.R.2 (eutectic bump).

Table 4.5.3 Chip_Boundary size to bump pitch rule for lead-free bump.

The design rule dimensions (Layout) for N7+ are the same as on-silicon (On-Si) dimensions. (All numbers are **on-silicon dimensions** within $\pm 1 \mu\text{m}$ tolerance for bump pitch)

On design / silicon dimension (μm)	Chip_Boundary size (mm^2)	Area ≤ 100	100 < Area ≤ 225	225 < Area ≤ 400	400 < Area ≤ 755	Area > 755
	Bump pitch ^a (P) (μm)	≥ 150	≥ 150	≥ 150	≥ 150	Contact TSMC ^c

Note:

- Bump pitch = UBM pitch.
- When the Chip_Boundary size falls into “Contact TSMC” area, please contact TSMC for a joint assessment.

Table 4.5.74. Chip_Boundary size to dimension of KOZ at chip corner and chip edge regions for lead-free bump.

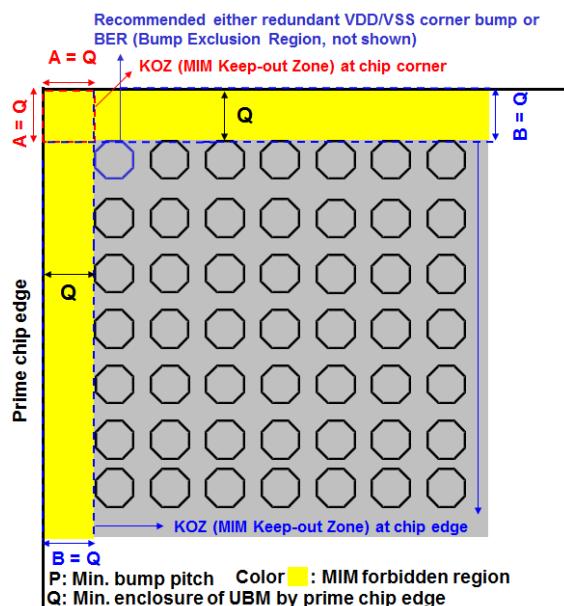
The design rule dimensions (Layout) for N7+ are the same as on-silicon (On-Si) dimensions. (All numbers are **on-silicon dimensions** within $\pm 1 \mu\text{m}$ tolerance for bump pitch)

Chip_Boundary size on design / silicon dimension (mm^2)	Area ≤ 100	100 < Area ≤ 225	225 < Area ≤ 400	400 < Area ≤ 755	Area > 755
Dimension of KOZ ^a at chip corner region (A) (μm)	$A = Q$	$A = Q$	$A = Q + 0.5xP^b$	$A = Q + 0.5xP^b$	Contact TSMC ^c
Dimension of KOZ ^a at chip edge region (B) (μm)	$B = Q$	$B = Q$	$B = Q$	$B = Q$	Contact TSMC ^c

Note:

- KOZ is MIM keep-out zone.
- (1) P: Minimum bump pitch. (2) Q: Minimum enclosure of UBM by Chip_Boundary edge.
- When the Chip_Boundary size falls into “Contact TSMC” area, please contact TSMC for a joint assessment.
 - The figure shows the DRC check zones for MIM KOZ (Keep-out Zone).
 - The following Chip_Boundary sizes are “Design / Silicon Dimension”.

Chip_Boundary area $\leq 100 \text{ mm}^2$
 $100 \text{ mm}^2 < \text{Chip_Boundary area} \leq 225 \text{ mm}^2$



$225 \text{ mm}^2 < \text{Chip_Boundary area} \leq 400 \text{ mm}^2$
 $400 \text{ mm}^2 < \text{Chip_Boundary area} \leq 755 \text{ mm}^2$

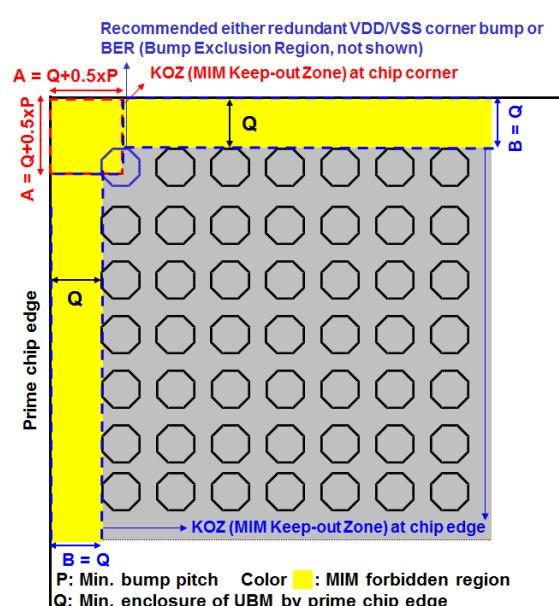


Figure 4.5.3 Schematic diagram for KOZ.R.3 and KOZ.R.4 (lead-free bump).

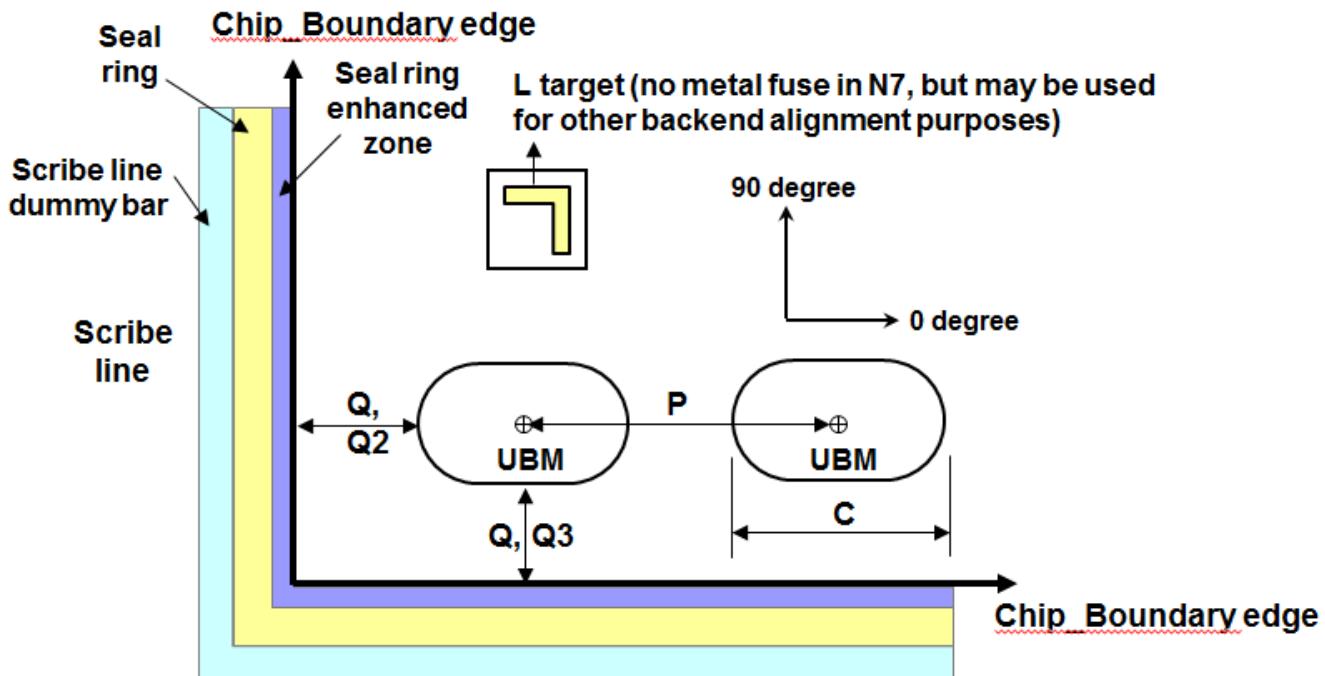


Figure 4.5.4 Schematic diagram for Cu bump on pad.

Table 4.5.5 Chip_Boundary size to bump pitch rule for Cu bump on pad.

The design rule dimensions (Layout) for N7+ are the same as on-silicon (On-Si) dimensions. (All numbers are **on-silicon dimensions** within $\pm 1 \mu\text{m}$ tolerance for bump pitch)

On design / silicon dimension (μm)	Chip_Boundary size (mm^2)	Area ≤ 100	100 < Area ≤ 225	225 < Area ≤ 400	400 < Area ≤ 625	Area > 625
	Bump pitch ^a (P) (μm)	≥ 130	≥ 130	≥ 130	≥ 130	Contact TSMC ^b

Note:

a. Bump pitch = UBM pitch.

b. When the Chip_Boundary size falls into “Contact TSMC” area, please contact TSMC for a joint assessment.

Table 4.5.6 Chip_Boundary size to dimension of KOZ at chip corner and chip edge regions for Cu bump on pad.

The design rule dimensions (Layout) for N7+ are the same as on-silicon (On-Si) dimensions. (All numbers are **on-silicon dimensions** within $\pm 1 \mu\text{m}$ tolerance for bump pitch)

Chip_Boundary size on design / silicon dimension (mm^2)	Area ≤ 100	$100 < \text{Area} \leq 225$	$225 < \text{Area} \leq 400$	$400 < \text{Area} \leq 625$	$\text{Area} > 625$
Dimension of KOZ ^a at chip corner region (A) (μm)	$A2 = Q2 + 0.5xP^b$ $A3 = Q3 + 0.5xP^b$	$A2 = Q2 + 0.5xP^b$ $A3 = Q3 + 0.5xP^b$	$A2 = Q2 + 0.5xP^b$ $A3 = Q3 + 0.5xP^b$	$A2 = Q2 + 1xP^b$ $A3 = Q3 + 1xP^b$	Contact TSMC ^c
Dimension of KOZ ^a at chip edge region (B) (μm)	$B2 = Q2 + 0.5xP^b$ $B3 = Q3 + 0.5xP^b$	$B2 = Q2 + 0.5xP^b$ $B3 = Q3 + 0.5xP^b$	$B2 = Q2 + 0.5xP^b$ $B3 = Q3 + 0.5xP^b$	$B2 = Q2 + 1xP^b$ $B3 = Q3 + 1xP^b$	Contact TSMC ^c

Note:

- a. KOZ is MIM keep-out zone.
- b. (1) P: Minimum bump pitch. (2) Q2: Minimum enclosure of UBM by Chip_Boundary edge in horizontal direction. (3) Q3: Minimum enclosure of UBM by Chip_Boundary edge in vertical direction.
- c. When the Chip_Boundary size falls into “Contact TSMC” area, please contact TSMC for a joint assessment.
 - The figure shows the DRC check zones for MIM KOZ (Keep-out Zone).
 - The following Chip_Boundary sizes are “Design / Silicon Dimension”.

Chip_Boundary area $\leq 100 \text{ mm}^2$

$100 \text{ mm}^2 < \text{Chip_Boundary area} \leq 225 \text{ mm}^2$
 $225 \text{ mm}^2 < \text{Chip_Boundary area} \leq 400 \text{ mm}^2$

$400 \text{ mm}^2 < \text{Chip_Boundary area} \leq 625 \text{ mm}^2$

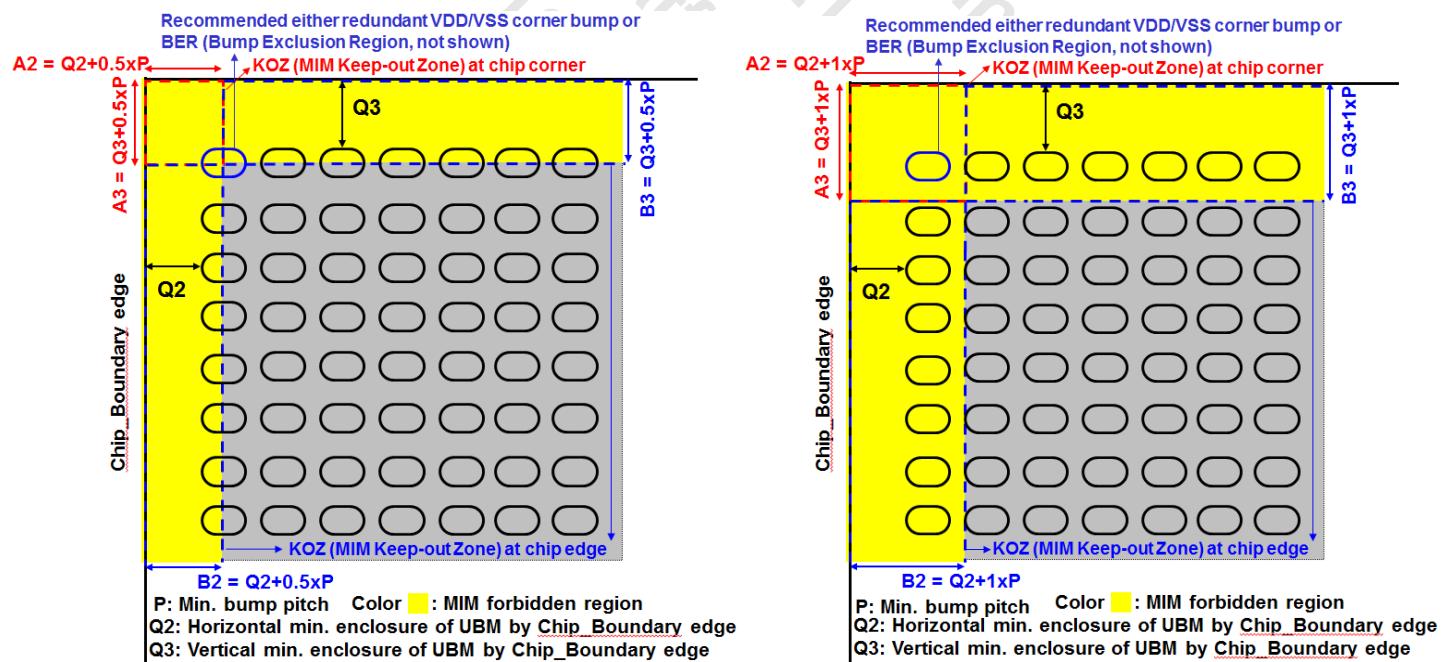


Figure 4.5.5 Schematic diagram for KOZ.R.5 and KOZ.R.6 (Cu bump on pad).

Table 4.5.7 Chip_Boundary size to bump pitch rule for ubump.

- The design rule dimensions (Layout) for N7 are the same as on-silicon (On-Si) dimensions. (All numbers are **on-silicon dimensions** within $\pm 1 \mu\text{m}$ tolerance for bump pitch)

On design / silicon dimension (μm)	Chip_Boundary size (mm^2)	Area ≤ 400	400 $<$ Area
	Bump pitch ^a (P) (μm)	≥ 39.96	≥ 39.96

Note:

- c. Bump pitch = UBM pitch.

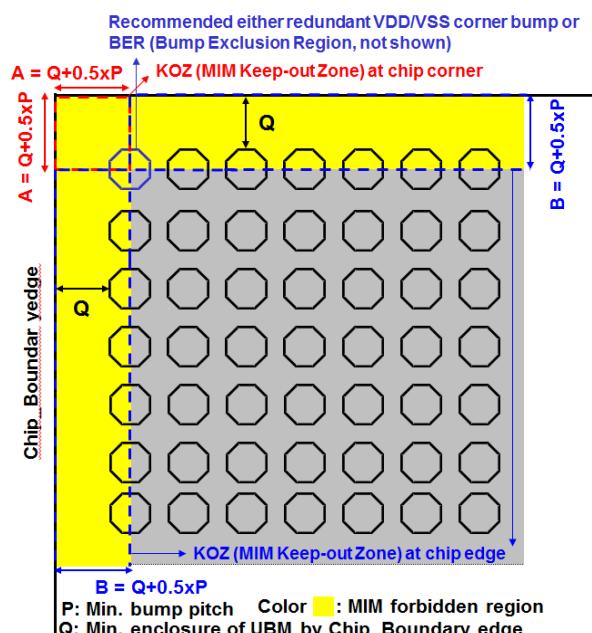
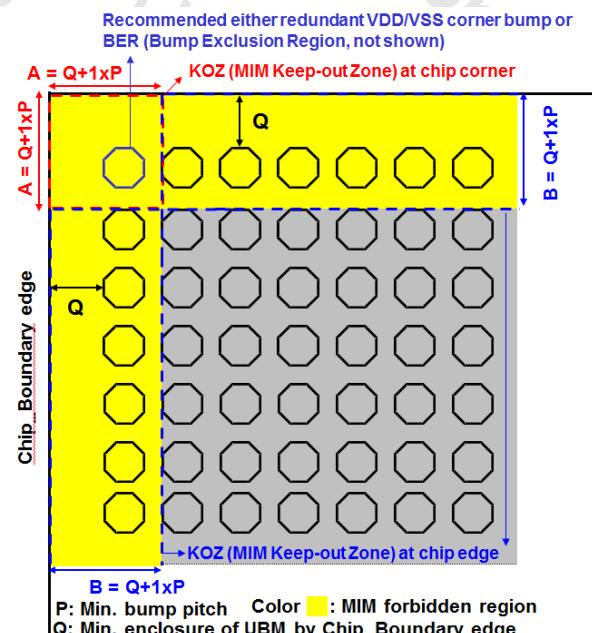
Table 4.5.748. Chip_Boundary size to dimension of KOZ at chip corner and chip edge regions for ubump.

- The design rule dimensions (Layout) for N7 are the same as on-silicon (On-Si) dimensions. (All numbers are **on-silicon dimensions** within $\pm 1 \mu\text{m}$ tolerance for bump pitch)

Chip_Boundary size on design / silicon dimension (mm^2)	Area ≤ 400	400 $<$ Area
Dimension of KOZ ^a at chip corner region (A) (μm)	$A = Q + 0.5xP^b$	$A = Q + 1xP^b$
Dimension of KOZ ^a at chip edge region (B) (μm)	$B = Q + 0.5xP^b$	$B = Q + 1xP^b$

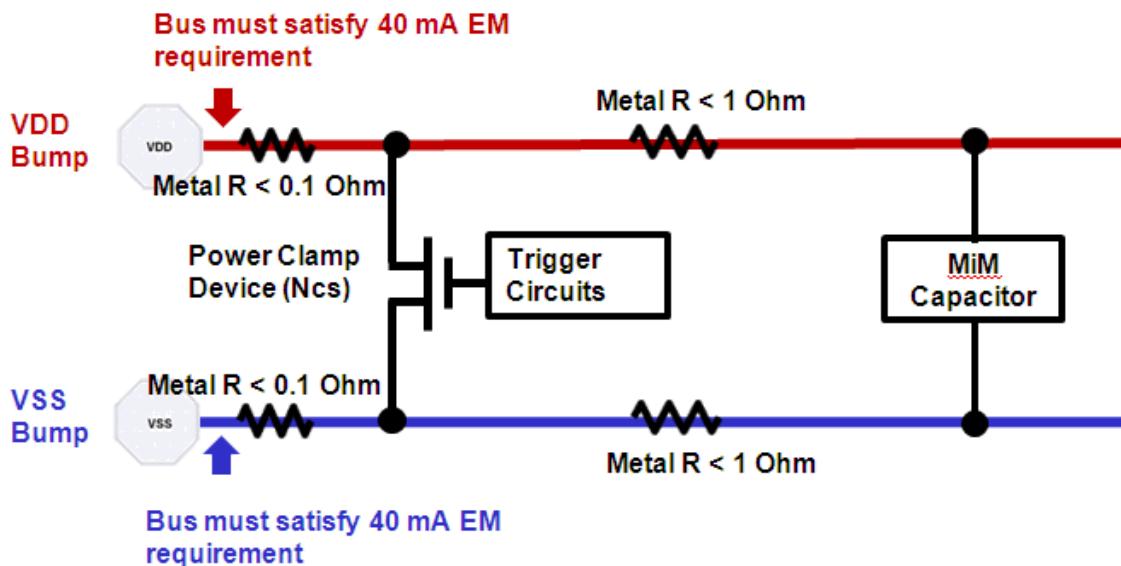
Note:

- d. KOZ is MIM keep-out zone.
e. (1) P: Minimum bump pitch. (2) Q: Minimum enclosure of UBM by Chip_Boundary edge.
• The figure shows the DRC check zones for MIM KOZ (Keep-out Zone).
• The following Chip_Boundary sizes are “Design / Silicon Dimension”.

Chip_Boundary area $\leq 400 \text{ mm}^2$ **400 $\text{mm}^2 <$ Chip_Boundary area****Figure 4.5.6 Schematic diagram for KOZ.R.7 and KOZ.R.8 (ubump).**

4.5.74.8 HD MIM ESD Protection Design Guidelines

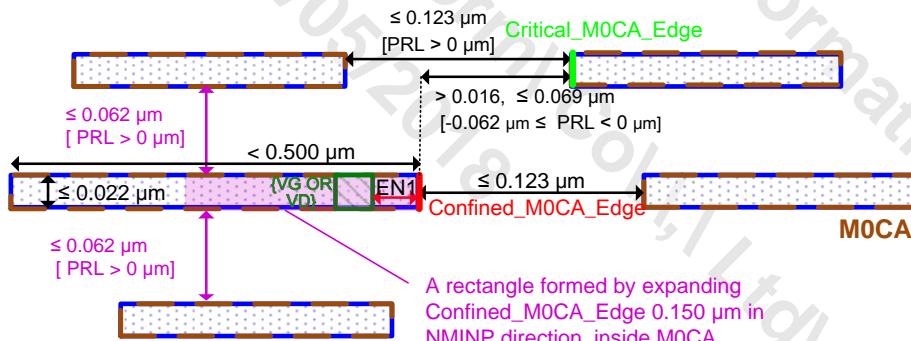
- Please refer to the T-N07-CL-DR-022 Chapter 9.2.6.4 of for the clamp cell design.
- Resistance of the bus line from the clamp cell to the HD MIM circuitry needs to be < 1 ohm.
- If the HD MIM is between VDD and VSS, the max resistance from the power bump (VDD)/ground bump (VSS) to the clamp cell is 0.1 ohm for core voltage power clamp, and 0.4 ohm for IO voltage power clamp.
- The metal rails connecting from VDD and VSS bumps to the power clamp must be wide enough and satisfy 40mA (minimum) EM requirement at 110 °C.



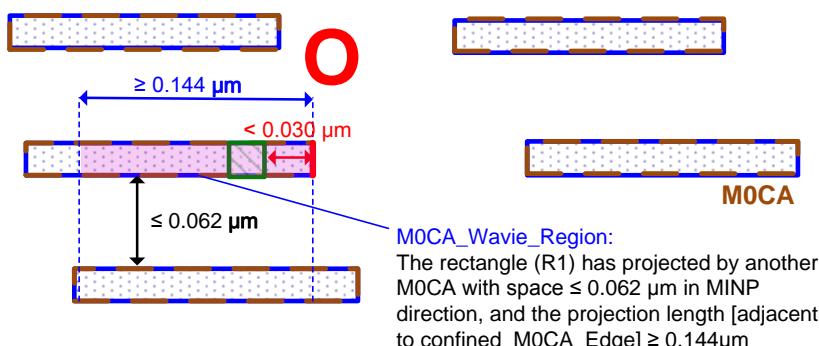
4.5.75 Extensive Forbidden Pattern (EFP) Rules

This section is to accommodate the very confined patterns that located in a very specific and complex environment where design rule is hard to describe with traditional way. These confined patterns may harm process robustness. Hence, these rules and recommendations are set to secure successful production.

Rule No.	Description	Label	Op.	Rule
EFP.M0.EN.1	<p>Enclosure of VC by Confined_M0CA_Edge (Except Confined_M0CA_Edge coincident edge with M0CA_Waive_Region)</p> <p>Definition of Confined_M0CA_Edge: A Critical_M0CA_Edge of M0CA [width $\leq 0.022 \mu\text{m}$ in MINP direction, length $< 0.500 \mu\text{m}$ in NMINP direction] follows the following conditions:</p> <ul style="list-style-type: none"> (1) Space to Critical_M0CA_Edge $> 0.016 \mu\text{m}$, and $\leq 0.069 \mu\text{m}$ in NMINP direction [PRL > -0.0625 μm], and (2) Expands 0.150 μm in NMINP direction, inside M0CA to form a rectangle (R1). Both side of the rectangle (R1) space to M0CA $\leq 0.062 \mu\text{m}$ in MINP direction [PRL > 0 μm] <p>Definition of Critical_M0CA_Edge: M0CA line-end edge space to M0CA $\leq 0.123 \mu\text{m}$ in NMINP direction [PRL > 0 μm]</p> <p>Definition of M0CA_Wavie_Region: The rectangle (R1) has projected by another M0CA with space $\leq 0.062 \mu\text{m}$ in MINP direction, and the projection length [adjacent to confined_M0CA_Edge] $\geq 0.144 \mu\text{m}$.</p>	EN1	\geq	0.0300



Except: Confined_M0CA_Edge coincident edge with M0CA_Waive_Region



5 Layout Rules For the Device Geometry Effect

This chapter contains the following topics:

- 5.1 Layout Guidelines for the WPE (Well Proximity Effect)
- 5.2 Layout Guidelines for the CPO Effect
- 5.3 Layout Guidelines for LOD (Length of the OD region) Effect
- 5.4 Layout Guidelines for OSE (OD Space Effect)
- 5.5 Layout Guidelines for MBE (Metal Boundary Effect)

5.1 Layout Guidelines for the WPE (Well Proximity Effect)

NMOSFET or PMOSFET very close to well edge will exhibit a difference in threshold voltage (V_t) and drive current (I_d) from that of the device located remotely from well edge. As well edge and gate spacing gets smaller, the V_t of MOS device is raised and the I_d is degraded.

In N16, SPICE model only considers the core NMOS WPE phenomenon in horizontal direction. As the space between Well edge and core NMOS Gate gets smaller, the V_t will be raised and the I_d will be degraded.

WPE of core PMOS, IO N/PMOS, and core NMOS vertical direction can be neglected.

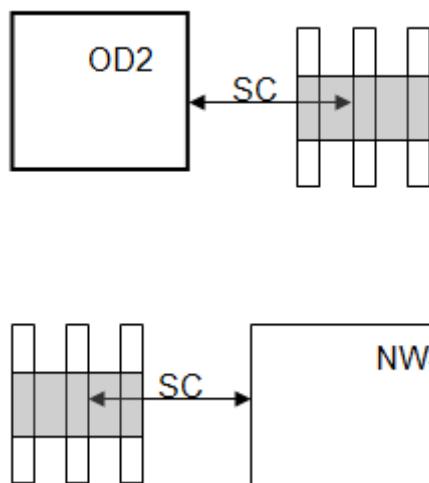
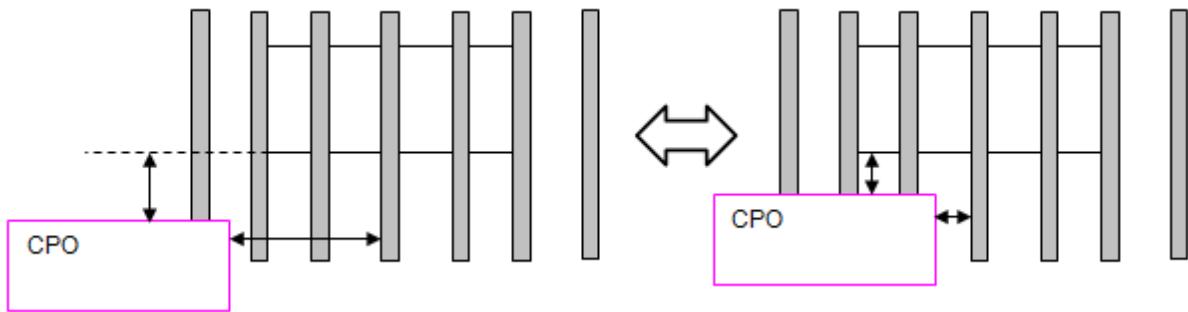


Figure 5.1.1 Both NW layout and OD2 layout are related to WPE

5.2 Layout Guidelines for the CPO Effect

When NMOSFET or PMOSFET is very close to CPO and result in different poly extension length between active poly gate and nearby poly, the MOSFET will exhibit a difference in drive current (I_d) from that of the device located remotely from CPO.



5.3 Layout Guidelines for LOD (Length of the OD region) Effect

5.3.1 What is LOD?

1. The device performance (V_t or I_d) will be impacted by LOD effect. It is due to the different mechanical stress induced by the different OD length.
2. SPICE model has included the LOD effect. Users need to input SA and SB in the netlist to activate these new features. (SA and SB are the distance between TrGATE to OD edge). (Figure 5.3.1.1)

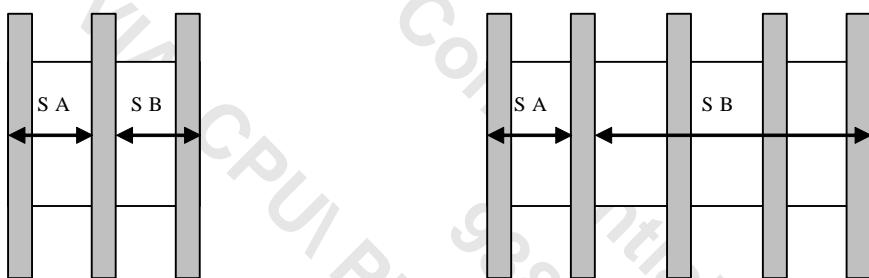


Figure 5.3.1.1 Example of SA and SB

5.4 Layout Guidelines for OSE (OD Space Effect)

5.4.1 What is OSE?

1. The MOSFET characteristics will be impacted by OSE. This is due to the varying levels of STI mechanical stress induced by differences in OD space.
2. The MOSFET characteristics depend on the surrounding OD space in both the “L-direction” ($OD-S_L$) and the “W-direction” ($OD-S_W$). (Figure 5.4.1.1)

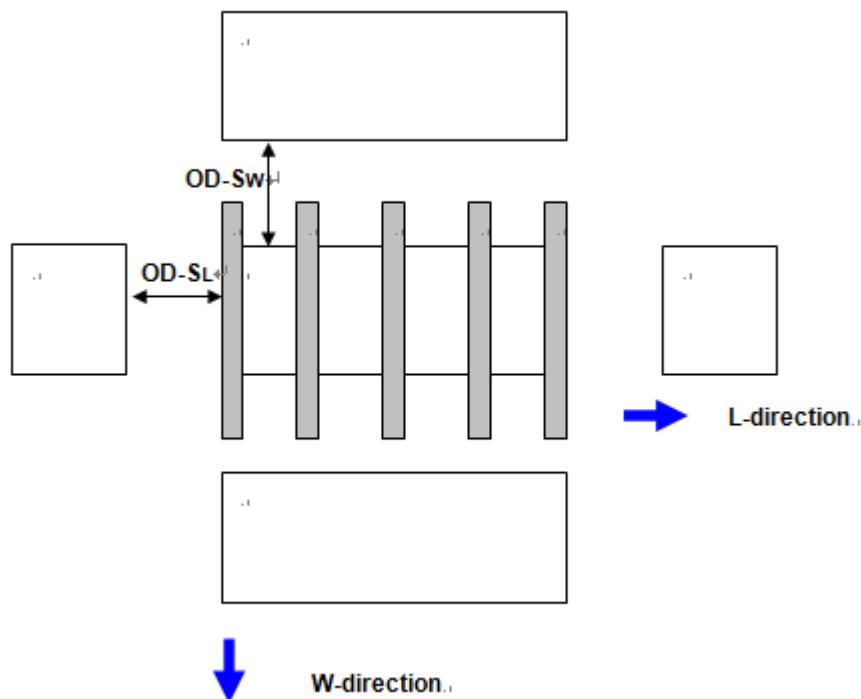


Figure 5.4.1.1 Example of $OD-S_L$ and $OD-S_W$

5.5 Layout Guidelines for MBE (Metal Boundary Effect)

5.5.1 What is MBE?

NMOSFET or PMOSFET threshold voltage (V_t) or drain current (I_d) will be modulated by N/P gate boundary shift. This N/P gate boundary shift induced MOSFET characteristic changes are included in SPICE MBE model.

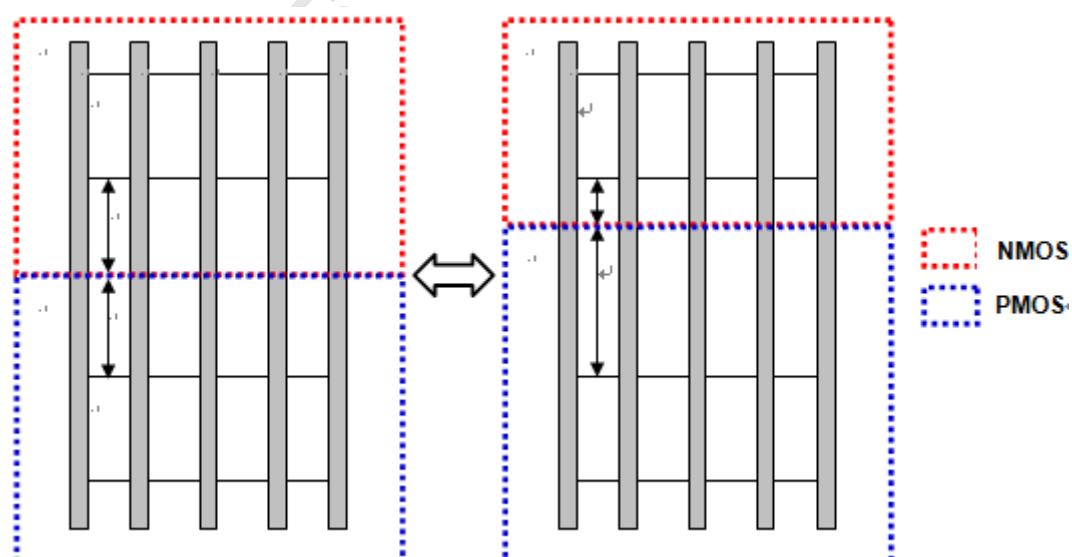


Figure 5.5.1.1 Example of MBE

6 Dummy Pattern rule and Filling Guideline

This chapter contains the following topics:

- 6.1 Dummy Cell Rules
- 6.2 Dummy Metal (DM) Rules
- 6.3 Dummy VIA (DVIA) Rules
- 6.4 Dummy TCD (DTCD) rules and Filling Guideline
- 6.5 In Chip Overlay (ICOVL) Rules and Filling Guideline
- 6.6 IP Density Guidelines

- It is a must to use TSMC utility to insert dummy patterns. Do not change any dimension and variable related to dummy patterns dimensions in utility

6.1 Dummy Cell Rules

- Dummy cell can be used in tsmc dummy utility only.

Dummy_Cell = {{{{DC_Core OR DC_IO} OR DC_WPO} OR DC7} OR DC8_1} OR DC8_2}

DC_Mandrel = {DC3 OR DC2_MANDREL}

DC_PO36 = {DC2_CORE OR DC4_CORE} OR DC6_1}

DC_Core = {DC_Mandrel OR DC_PO36}

DC_IO = {DC2_IO OR DC4_IO}

DC_WPO = {{DC6_2 OR DC5_1} OR DC5_2}

DC_WO_IMP = {Dummy_Cell NOT DC3}

DC_OD_WONP = {{{DC_Core NOT DC3} OR DC_IO} OR DC6_2}

DC_PO = {{{Dummy_Cell NOT DC_7} NOT DC8_1} OR DC8_2}

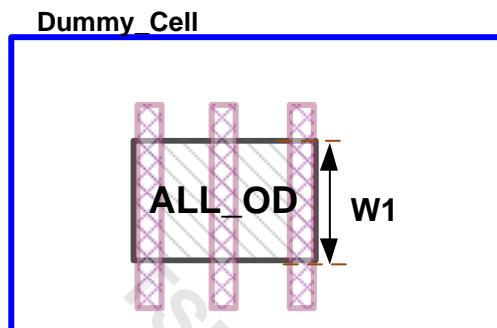
Rule No.	Description	Label	Op.	Rule
DC.W.2	Width of DC8_1 in vertical /horizontal direction	W2	=	0.0900/0.2700
DC.W.2.1	Width of DC8_2 in vertical /horizontal direction	W2A	=	0.1800/0.2000
DC.S.1	Space of ALL_PO [INSIDE DC_PO36] to ALL_PO [width ≤ 0.011 μm]	S1	≥	0.1500
DC.S.1.1	Space of ALL_PO [INSIDE DC_WPO] to ALL_PO	S1A	≥	0.1300
DC.S.1.2	Space of ALL_PO [INSIDE DC_Mandrel] to ALL_PO [width ≤ 0.011 μm] in horizontal direction	S1B	=	0.0460, 0.1600, 0.1800
DC.S.2	Space of DC6_1 to {{FB_9 OR FB_8} OR SRM (50;0)} in horizontal direction	S2	≥	0.2000
DC.S.3	Space of DC4_CORE to {{FB_9 OR FB_8} OR SRM (50;0)} in horizontal direction	S3	≥	0.1600
DC.S.4	Space of DC2_MANDREL to SRM in horizontal direction [PRL > -0.209 μm]	S4	≥	0.1560
DC.S.4.1	Space of DC2_MANDREL to {FB_9 OR FB_8} in horizontal direction [PRL > -0.110 μm]	S4A	≥	0.1720
DC.S.4.2	Space of {DC8_1 OR DC8_2} to {SRM OR {FB_9 OR FB_8}} in vertical direction [PRL > -0.187 μm]	S4B	≥	0.1800
DC.S.5	Space of DC_PO	S5	≥	0.0200
DC.S.6.T	Space of TCDDMY1 to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC2_IO OR DC4_CORE OR DC4_IO OR DC6_1 OR DC6_2 OR DC5_1 OR DC5_2 OR DC7 OR DC8_1 OR DC8_2 OR DC9_1}	S6	≥	0.0200
DC.S.6.1.T	Space of ICOVL_single to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC2_IO OR DC4_CORE OR DC4_IO OR DC6_1 OR DC6_2 OR DC5_1 OR DC5_2 OR DC7 OR DC9_1}	S6A	≥	0.0200
DC.S.6.2.T	Space of IBJTDY to {DC3 OR DC2_MANDREL OR DC2_CORE OR	S6B	≥	1.8000

	DC4_CORE OR DC6_1}			
DC.S.6.3.T	Space of NWDMY to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC2_IO OR DC4_CORE OR DC4_IO OR DC6_1 OR DC6_2 OR DC7}	S6C	≥	0.5400
DC.S.6.4.T	Space of DC9_1 to {SR_ESD OR DIODMY OR NWDMY OR INDDMY OR IBJTDMDY}	S6D	≥	0.1500
DC.S.6.5.T	Space of DC5_1 to {VAR OR MOMDMY OR MetalFuse}	S6E	≥	0.0350
DC.S.6.6.T	Space of DC5_2 to {VAR OR MOMDMY OR MetalFuse}	S6F	≥	0.0350
DC.S.7.T	Space of OD2 to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC2_IO OR DC4_CORE OR DC4_IO OR DC6_2}	S7	≥	0.0220
DC.S.7.1.T	Space of FB_9 to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC2_IO OR DC4_CORE OR DC4_IO OR DC6_1 OR DC6_2 OR DC8_1 OR DC8_2}	S7A	≥	0.1720
DC.S.7.2.T	Space of FB_8 to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC2_IO OR DC4_CORE OR DC4_IO OR DC6_1 OR DC6_2 OR DC8_1 OR DC8_2}	S7B	≥	0.1720
DC.S.7.3.T	Space of FB_9 to {DC7 OR DC9_1}	S7C	≥	0.1080
DC.S.7.4.T	Space of FB_8 to {DC7 OR DC9_1}	S7D	≥	0.1080
DC.S.8.T	Space of SRM to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC2_IO OR DC4_CORE OR DC4_IO OR DC6_1 OR DC6_2 OR DC7 OR DC8_1 OR DC8_2 OR DC9_1}	S8	≥	0.1080
DC.S.8.1.T	Space of SRM to {DC5_1 OR DC5_2}	S8A	≥	0.0780
DC.S.9.T	Space of NW to {DC3}	S9	≥	0.2000
DC.S.9.1.T	Space of RH_TN to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC4_CORE OR DC6_1}	S9A	≥	0.6000
DC.S.9.2.T	Space of RH_TN to {DC2_IO OR DC4_IO OR DC6_2 OR DC5_1 OR DC5_2 OR DC9_1}	S9B	≥	0.1000
DC.S.9.3.T	Space of TPO_2 to {DC3 OR DC2_MANDREL OR DC2_CORE OR DC2_IO OR DC4_CORE OR DC4_IO OR DC6_1 OR DC6_2}	S9C	≥	0.0230
DC.R.1	{DC8_1 OR DC8_2} overlap {{ALL_OD SIZING 0.140 μm in horizontal direction} SIZING 0.191 μm in vertical direction} is not allowed			
DC.R.2.1.T	DC3 interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMDY, NWDMY, OD2, NW, RH_TN, TPO_2, DC2_MANDREL, DC2_CORE, DC2_IO, DC4_CORE, DC4_IO, DC6_1, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2, DC9_1} is not allowed			
DC.R.2.2.T	DC2_MANDREL interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMDY, NWDMY, OD2, RH_TN, TPO_2, DC2_CORE, DC2_IO, DC4_CORE, DC4_IO, DC6_1, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2, DC9_1} is not allowed			
DC.R.2.3.T	DC2_CORE interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMDY, NWDMY, OD2, RH_TN, TPO_2, DCPODE, DC2_IO, DC4_CORE, DC4_IO, DC6_1, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2, DC9_1} is not allowed			
DC.R.2.4.T	DC2_IO interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMDY, NWDMY, RH_TN, TPO_2, SR_DMP, DCPODE, DC4_CORE, DC4_IO, DC6_1, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2, DC9_1} is not allowed			
DC.R.2.5.T	DC4_CORE interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMDY, NWDMY, RH_TN, TPO_2, SR_DCPO, SR_DCMD, SR_DMP, DCPODE, DC4_IO, DC6_1, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2, DC9_1} is not allowed			
DC.R.2.6.T	DC4_IO interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMDY, NWDMY, RH_TN, TPO_2, SR_DCPO, SR_DCMD, SR_DMP, DCPODE, DC6_1, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2, DC9_1} is not allowed			
DC.R.2.7.T	DC6_1 interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMDY, NWDMY, OD2, RH_TN, TPO_2, SR_DCPO, SR_DCMD, SR_DMP, DCPODE, DC6_2, DC5_1, DC5_2, DC7, DC8_1, DC8_2, DC9_1} is not allowed			
DC.R.2.8.T	DC6_2 interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMDY, NWDMY, RH_TN, TPO_2, SR_DCPO, SR_DCMD, SR_DMD, DCPODE, DC5_1, DC5_2, DC7, DC8_1, DC8_2, DC9_1} is not allowed			

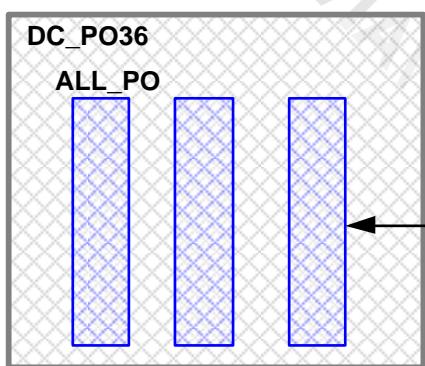
DC.R.3.1.T	DC5_1 interact {OD, PO, MD, MP, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMY, MOMDMY, RH_TN, DC5_2, DC9_1} is not allowed			
DC.R.3.2.T	DC5_2 interact {OD, PO, MD, MP, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, IBJTDMY, MOMDMY, RH_TN, DC9_1} is not allowed			
DC.R.4.T	DC7 interact {OD, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, SR_DMD, DCPODE, NWDMY, RH_TN} is not allowed			
DC.R.5.1.T	DC8_1 interact {OD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, DCPODE, DC8_2} is not allowed			
DC.R.5.2.T	DC8_2 interact {OD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, DCPODE} is not allowed			
DC.R.6.T	DC9_1 interact {OD, PO, MD, MP, CMD, FB_7, FB_8, FB_9, TCDDMY, ICOVL_SINGLE, SEALRING_ALL, SRM, SR_DCPO, SR_DMD, DCPODE, SR_ESD, DIODMY, NWDMY, INDDMY, IBJTDMY, RH_TN} is not allowed			

VIAI CPU Confidential Information
938214
10/05/2018

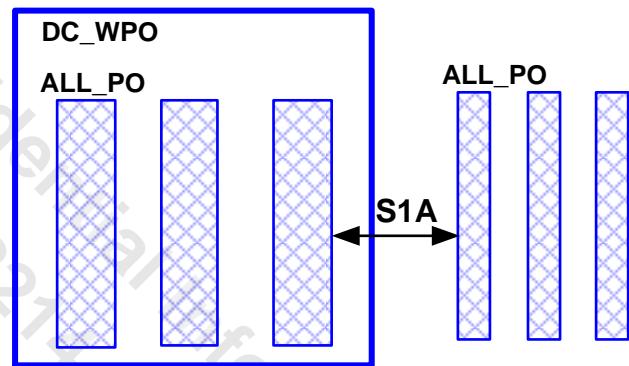
DC



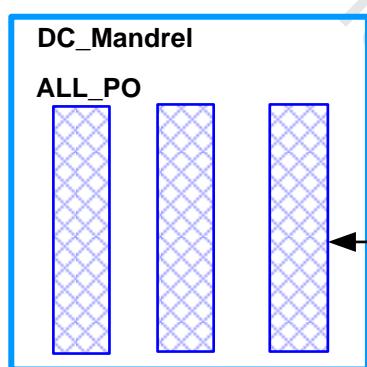
DC.W.1



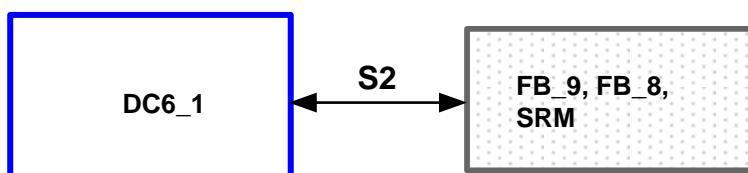
DC.S.1



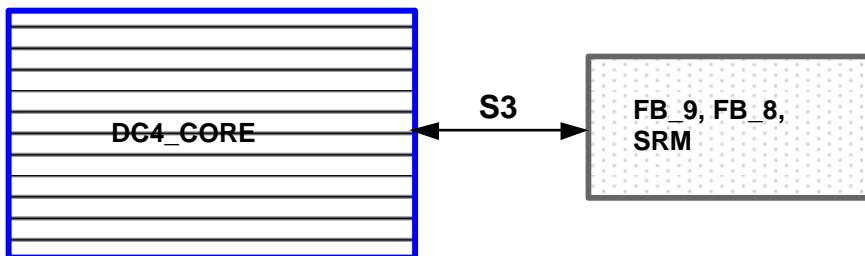
DC.S.1.1



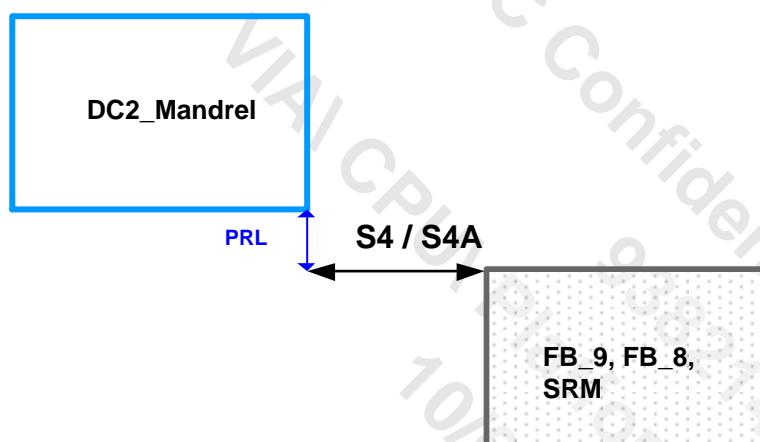
DC.S.1.2



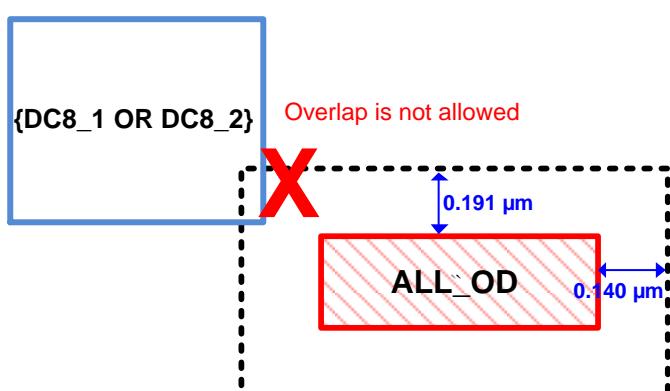
DC.S.2



DC.S.3



DC.S.4 / DC.S.4.1



DC.R.1

6.2 Dummy Metal (DM) Rules

(DMn, n = 0,1, xs, x, xa, ya, y, yy, yx, yz, z, r)

1. To improve the metal CMP process window, **you must fill the DMn globally and uniformly** even if the originally drawn Mn has already met the density rule (Mn.DN.1.1/ Mn.DN.1.2/Mn.DN.2).
2. **Use the utility dummy fill as a method for automated dummy metal insertion.**
 - The utility dummy fill is better for IP blocks, library cells, and full custom cells.
 - The TSMC utility can insert dummy metal uniformly within the original layout. (document no: *T-N07-CL-DR-022-X3, X is the code of EDA tool*)
 - If you use TSMC's auto-fill utility to fill the DMn on the whole chip GDS, TSMC will waive the local density violation. If you do not use TSMC's utility to perform the DMn generation, you must meet the local density rule.
3. In the TSMC utility, 2 kinds of dummy metal are generated, DMn and DMn_O.
 - DMn: dummy metal
 - No OPC on DMn
 - DMn for M0, M1, Mxs, Mx, Mxa, Mya, My, Myy, Myx, Myz, Mz, and Mr.
 - DMn_O: OPC dummy of inter-metal.
 - The rule of DMn_O is the same as real metal, Mn. So, there is no related rule in this section.
 - There is no DMn_O for Myx, Myz, Mz, and Mr.
 - DMn_O receives OPC.
 - The distinction between Mn, DMn and DMn_O.

	Mn	DMn	DMn_O
GDS datatype	255/256 (0), 420 (1), 400 (xs), 255/256/275/276 (x), 295/296/315/316 (xa), 330/340 (ya), 350/360 (y), 90 (yy), 30 (yz), 40 (z), 80 (r)	258/259 (0) 421 (1), 401 (xs), 258/259/278/279 (x), 298/299/318/319 (xa), 331/341 (ya), 351/361 (y), 91 (yy), 371 (yx), 31 (yz), 41 (z), 81 (r)	252/253 (0) 427 (1), 407 (xs), 252/253/272/273 (x), 292/293/312/313 (xa), 337/347 (ya), 357/367 (y), 97 (yy)
Do OPC modification on it	Yes	No	Yes
Refer to it during OPC	Yes	Yes	Yes
Follow Mn rule	Yes	No	Yes

4. Use the dummy layer DMxEXCL properly. This layer directs TSMC's utility that the area covered should be blocked from DM fill operations. **All metal (geometry) beneath a customer-drawn blockage layer (DMxEXCL) must meet the local density rules.**
5. **It is suggested to make sure that DMxEXCL is drawn over the following:**
 - Sensitive circuits (such as SRAM sensitive function blocks and bit cell array) and analog circuits (such as DAV/ADC, and PLL)
 - RF application circuits
 - Pad areas for high frequency signals

For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, careful manual uniform fill addition is still recommended so as to gain a better process window and electrical performance.

6. **For DMxEXCL, use the GDS layer numbers 150;n (n = 180,1,2,3,4,5,6,7,8,9,10,11,12,13,14).**
7. Revision of the following layers may necessitate re-filling of DMn. Because of this, **evaluate the impact on the metal layer mask carefully** when any one of the following layouts is revised:
 - Mn and DMxEXCL layers. This layout revision impacts the Mn mask only.
 - LOGO/INDDMY. This revision impacts all the metal layer masks.

8. In order to have an accurate interconnect RC for timing and power analysis, it is important to extract RC after dummy metal insertion, and extract RC with density based metal thickness variation feature enabled.

9. Don't put DMn in areas covered by the following marker layers:

- Inductor region (INDDMY)
- Regions of chip corner stress relief pattern, seal-ring, and CDU pattern

TSMC's fill generation utility will not add DMn into these regions because these layers are well defined.

The DMxEXCL covered areas should not cover or overlap the above areas for DRC reasons.

10. Please refer to the “Dummy Pattern Fill Usage Summary” section in this chapter for additional information.

11. Please consult with TSMC first before you use your own DMn rules.

Rule No.	Description	Label	Op.	Rule
DMn.W.1	Width (minimum)	A	\geq	
DMn.W.1.1	Width of DMn_O (minimum)	A	\geq	
DMn.W.2	Width of {DMn OR DMn_O} (maximum)	B	\leq	
DMn.S.1	Space	C	\geq	
DMn.S.1.1	Space of DMn_O (minimum)	C	\geq	
DMn.S.2	Space to Mn (Overlap is not allowed) (Except SEALRING_ALL)	D	\geq	
DMn.S.2.1	Space of DMn_O to Mn (Overlap is not allowed)	D	\geq	
DMn.S.2.1.1	Space of DMn to DMn_O (Overlap is not allowed) (This check is only applied to M0/Mx/Mxa)	S	\geq	0.1600
DMn.S.2.1.2	Space of DMn to DMn_O (Overlap is not allowed) (This check is only applied to M1/Mxs)	S	\geq	0.1000
DMn.S.2.2	Space of DMn to DMn_O (Overlap is not allowed) (This check is only applied to Mya/My)	S	\geq	0.1800
DMn.S.2.3	Space of DMyy to DMyy_O (Overlap is not allowed)	S	\geq	0.5400
DMn.S.2.4	Space of DMn_O to Mn line-end [edge length \leq 0.060 μm between 2 consecutive 90-90 degree corners, PRL > -0.040 μm]. (Overlap is not allowed) (Only check M0, M1, Mxs, Mx, Mxa, Mya and My)	D1	\geq	
DMn.S.2.5	Space of {DMn OR DMn_O} to {Mn OR DMn} (Overlap is not allowed) [Mn or DMn width > 0.040 μm] (This check is only applied to M0/M1/Mxs/Mx/Mxa)	E	\geq	0.0350
DMn.S.2.6	Space of {DMn OR DMn_O} to {Mn OR DMn} (Overlap is not allowed) [Mn or DMn width > 0.140 μm and the PRL > 0.080 μm] (This check is only applied to M0/Mx/Mxa)	E	\geq	0.1600
DMn.S.2.6.1	Space of DMn to {{Mn OR DMn} OR DMn_O} [width \geq 0.140 μm] in MINP direction [PRL > 0.080 μm] (Overlap is not allowed) (This check is only applied to M1/Mxs)	E	\geq	0.0600
DMn.S.2.6.2	Space of DMn to {{Mn OR DMn} OR DMn_O} [width \geq 0.140 μm] in NMNP direction [PRL > 0.080 μm] (Overlap is not allowed) (This check is only applied to M1/Mxs)	E	\geq	0.1200
DMn.S.2.7	Space of {DMn OR DMn_O} to {Mn OR DMn} (Overlap is not allowed) [Mn or DMn width > 0.260 μm and the PRL > 0.080 μm] (This check is only applied to M0/Mx/Mxa)	E	\geq	0.2600
DMn.S.3	Space of {DMn OR DMn_O} to {Mn OR DMn} (Overlap is not allowed) [Mn or DMn width > 0.20 μm and the PRL > 0.120 μm] (This check is only applied to Mya/My)	E	\geq	0.1600
DMn.S.3.1	Space of {DMn OR DMn_O} to {Mn OR DMn} (Overlap is not allowed) [Mn or DMn width > 1.35 μm and the PRL > 1.35 μm] (This check is only applied to Mya/My/Myy/Myx/Myz/Mz/Mr)	E	\geq	0.4500

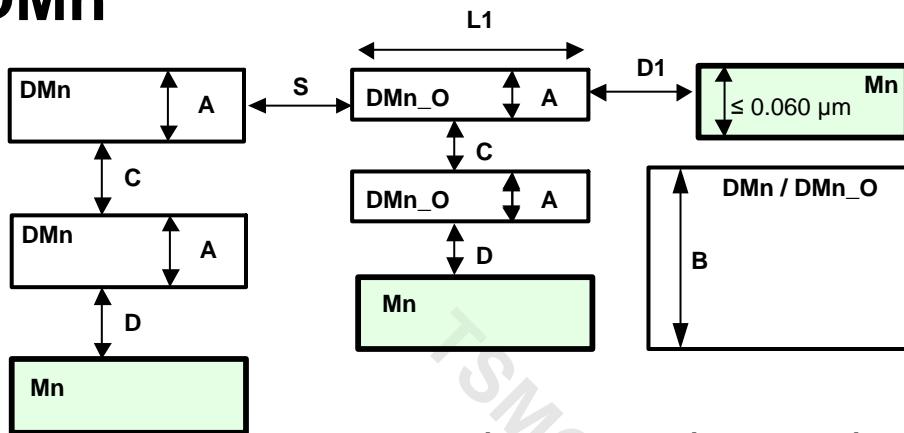
Rule No.	Description	Label	Op.	Rule
DMn.S.3.3	Space to {Mn OR DMn} (Overlap is not allowed) [Mn or DMn width > 4.05 μm and the PRL > 4.05 μm] (This check is only applied to Myy/Myx/Myz/Mz/Mr)	E	≥	1.35
DMn.S.3.5	Space of {DMn OR DMn_O} to {Mn OR DMn} (Overlap is not allowed) [Mn or DMn width ≥ 0.280 μm and the PRL > 0.160 μm] (This check is only applied to Mya/My)	E	≥	0.2000
DMn.S.7	Empty space of {{Mn OR DMn} OR DMn_O} DRC flags {{CHIP NOT {{Mn OR DMn} OR DMn_O}} SIZING down/up 0.500 μm} (Except LOGO, INDDMY, or following conditions: 1. {SEALRING_ALL SIZING 0.500 μm}, 2. {TCDDMY_Mn SIZING 0.2 μm}, 3. ICOVL_SINGLE, 4. Chip corner triangle empty areas if seal-ring is added by tsmc) (This check is only applied to M0/M1/Mxs/Mx/Mxa/Mya/My)	S7	≤	1
DMn.S.7®	Empty space of {{Mn OR DMn} OR DMn_O} DRC flags {{CHIP NOT {{Mn OR DMn} OR DMn_O}} SIZING down/up 0.400 μm} (Except LOGO, INDDMY, or following conditions: 1. {SEALRING_ALL SIZING 0.500 μm}, 2. {TCDDMY_Mn SIZING 0.2 μm}, 3. ICOVL_SINGLE, 4. Chip corner triangle empty areas if seal-ring is added by tsmc) (This check is only applied to M0/M1/Mxs/Mx/Mxa/Mya/My)	S7R	≤	0.8000
DMn.EN.1	Enclosure of DVIA n-1 by {DMn_O OR DMn} (n= 1, xs, x, xa)	EN1	≥	0
DMn.EN.1.1	Enclosure of DVIA n-1 by {DMn_O OR DMn} (at least two opposite sides) (n= 1, xs, x, xa)	EN1A	≥	0.0300
DMn.EN.2	Enclosure of DVIA n-1 by DMn (n= ya or y)	EN2	≥	0.0080
DMn.EN.2.1	Enclosure of DVIA n-1 by DMn (at least two opposite sides) (n= ya or y)	EN2A	≥	0.0900
DMn.EN.3	Enclosure of DVIA n-1 by DMn (n= yy)	EN3	≥	0.0090
DMn.EN.3.1	Enclosure of DVIA n-1 by DMn (at least two opposite sides) (n= yy)	EN3A	≥	0.0900
DMn.L.1	Edge length of DMn_O with adjacent edge [length < 0.090 μm] (This check is only applied to M0/M1/Mxs/Mx/Mxa)	L1	≥	0.1100
DMn.A.1	Area (minimum)	M	≥	
DMn.A.1.1	Area of DMn_O (minimum)	M	≥	
DMn.A.2	Area of {DMn OR DMn_O} (maximum)	N	≤	

RuleTable.DMn.R.0			Dimension						
Layer			A	B*	C	D	D1	M	N
M0	OPC dummy, in MINP direction	different color	0.024	0.5	0.020	0.020	0.108	0.0048	1
M0	OPC dummy, in MINP direction	same color	0.024	0.5	0.060	0.060	0.108	0.0048	1
M0	OPC dummy, in NMINP direction	different color	0.060	0.5	0.066	0.066	0.108	0.0048	1
M0	OPC dummy, in NMINP direction	same color	0.060	0.5	0.108	0.108	0.108	0.0048	1
M1	OPC dummy, in MINP direction		0.024	0.5	0.034	0.034	0.060	0.0048	1
M1	OPC dummy, in NMINP direction		0.060	0.5	0.060	0.060	0.060	0.0048	1
Mxs	OPC dummy, in MINP direction		0.024	0.5	0.034	0.034	0.060	0.0048	1
Mxs	OPC dummy, in NMINP direction		0.060	0.5	0.060	0.060	0.060	0.0048	1
Mx, Mxa	OPC dummy, in MINP direction	different color	0.024	0.5	0.020	0.020	0.124	0.0048	1
Mx, Mxa	OPC dummy, in MINP direction	same color	0.024	0.5	0.060	0.060	0.124	0.0048	1
Mx, Mxa	OPC dummy, in NMINP direction	different color	0.060	0.5	0.066	0.066	0.124	0.0048	1
Mx, Mxa	OPC dummy, in NMINP direction	same color	0.060	0.5	0.120	0.120	0.124	0.0048	1
M0, Mx, Mxa	Non OPC dummy	different color	0.106	0.5	0.076	2	N/A	0.0477	5
M0, Mx, Mxa	Non OPC dummy	same color	0.106	0.5	0.106	2	N/A	0.0477	5
M1	Non OPC dummy		0.106	0.5	0.076	2	N/A	0.0477	5
Mxs	Non OPC dummy		0.106	0.5	0.076	2	N/A	0.0477	5
Mya, My	OPC dummy, in MINP direction		0.058	2	0.076	0.114	0.114	0.0162	80
Mya, My	OPC dummy, in NMINP direction		0.114	2	0.114	0.114	0.114	0.0162	80
Mya, My	Non OPC dummy		0.106	2	0.106	1	N/A	0.0486	80
Myy	OPC dummy		0.090	2	0.090	0.270	N/A	0.0219	80
Myy	Non OPC dummy		0.180	2	0.270	1	N/A	0.1620	80
Myx, Myz, Mz	Non OPC dummy		0.360	3	0.360	0.540	N/A	0.4608	160
Mr	Non OPC dummy		0.800	3	0.800	0.800	N/A	1.44	160

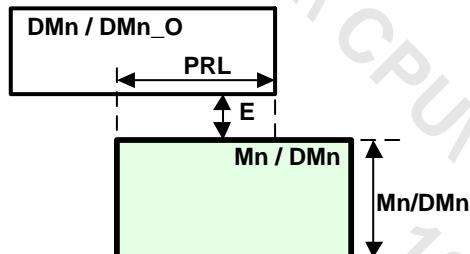
Table Notes:

* The maximum DMn. width need follow Mn.S.x

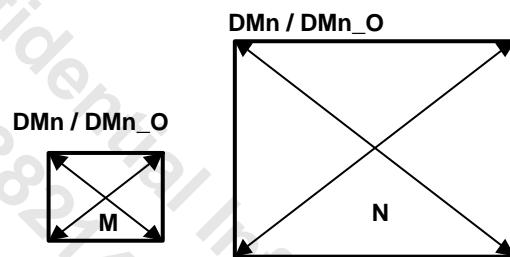
Rule No.	Description	Label	Op.	Rule												
DMn.R.0	DMn.W.1, DMn.W.1.1, DMn.W.2, DMn.S.1, DMn.S.1.1, DMn.S.2, DMn.S.2.1, DMn.A.1, DMn.A.1.1, DMn.A.2 follow RuleTable.DMn.R.0															
DMn.R.1	DMn is a must in chip level. The DMn CAD layer (TSMC default, 31;421 for DM1) must be different from the Mn CAD layer.															
DMn.R.2	DMn inside chip corner stress relief area is not allowed (Except seal-ring, or following conditions: 1. stress relief patterns drawn by customers)															
DMn.R.3	DMn and DMn_O must be a rectangle orthogonal to grid.															
DMn.R.4	Mn;258, and Mn;259 cannot interact with each other. (for M0) Mn;258, Mn;259, Mn;278, and Mn;279 cannot interact with each other. (for Mx) Mn;298, Mn;299, Mn;318, and Mn;319 cannot interact with each other. (for Mxa)															
DMn.R.5	Mn;252, and Mn;253 cannot interact with each other. (for M0) Mn;252, Mn;253, Mn;272, and Mn;273 cannot interact with each other. (for Mx) Mn;292, Mn;293, Mn;312, and Mn;313 cannot interact with each other. (for Mxa)															
DMn.R.6	DMn interact {prBoundary NOT {prBoundary SIZING -2 μm}} is not allowed in cell level (This check is only applied to M0/M1/Mxs/Mx/Mxa)															
DMn.R.6.1	DMn interact {prBoundary NOT {prBoundary SIZING -1 μm}} is not allowed in cell level (This check is only applied to Mya/My/Myy)															
DMn.R.7	{DMn OR DMn_O} INTERACT {Lower_VIA OR Upper_VIA} is not allowed (Except following conditions: 1. DMtop-1 only interact one CBMFINAL)															
DMn.R.7.1	{DM0 OR DM0_O} INTERACT {VC OR Upper_VIA} is not allowed.															
DMn.W.1g ^U	Recommended DMn size (width x length) <table border="1"> <tr> <td></td> <td>Square (Utility Fill)</td> </tr> <tr> <td></td> <td>Width x Length</td> </tr> <tr> <td>M0, M1, Mxs, Mx and Mxa</td> <td>0.12x1.4~0.24x0.7</td> </tr> <tr> <td>Mya and My</td> <td>0.108x0.450~2x2</td> </tr> <tr> <td>Myy</td> <td>0.180x0.900 ~ 0.270x1.800</td> </tr> <tr> <td>Myx, Myz and Mz</td> <td>0.36x1.28~1.8x1.8</td> </tr> </table>		Square (Utility Fill)		Width x Length	M0, M1, Mxs, Mx and Mxa	0.12x1.4~0.24x0.7	Mya and My	0.108x0.450~2x2	Myy	0.180x0.900 ~ 0.270x1.800	Myx, Myz and Mz	0.36x1.28~1.8x1.8			
	Square (Utility Fill)															
	Width x Length															
M0, M1, Mxs, Mx and Mxa	0.12x1.4~0.24x0.7															
Mya and My	0.108x0.450~2x2															
Myy	0.180x0.900 ~ 0.270x1.800															
Myx, Myz and Mz	0.36x1.28~1.8x1.8															

DMn

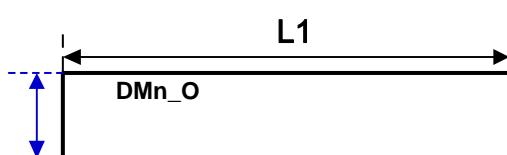
DMn.W.1 / DMn.W.1.1 / DMn.W.2 / DMn.S.1 / DMn.S.1.1 /
DMn.S.2 / DMn.S.2.1 / DMn.S.2.1.1 / DMn.S.2.1.2 /
DMn.S.2.2 / DMn.S.2.3 / DMn.S.2.4 / DMn.L.1



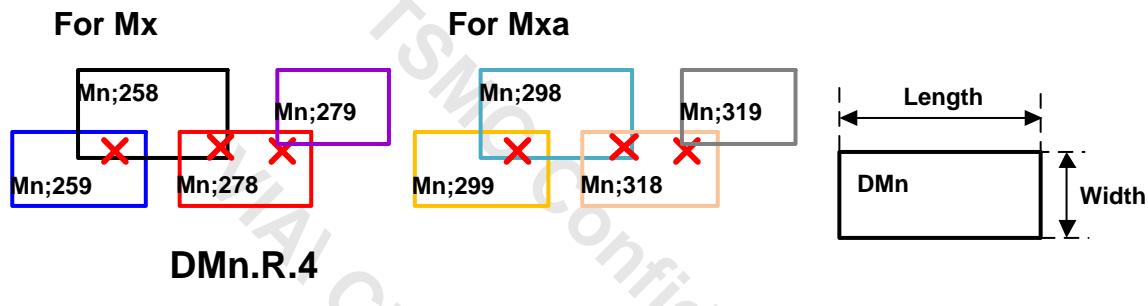
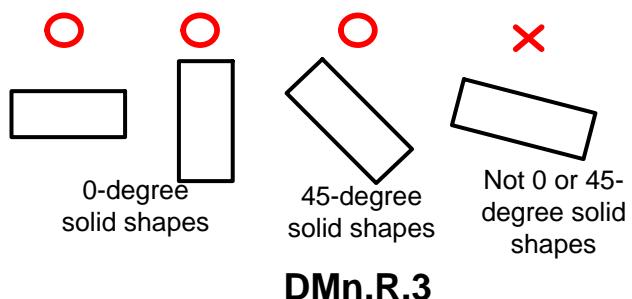
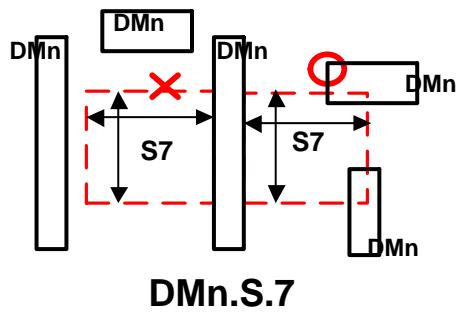
DMn.S.2.5 / DMn.S.2.6 / DMn.S.2.6.1 /
DMn.S.2.6.2 / DMn.S.2.7 / DMn.S.3 /
DMn.S.3.1 / DMn.S.3.3 / DMn.S.3.5



DMn.A.1 / DMn.A.1.1 / DMn.A.2

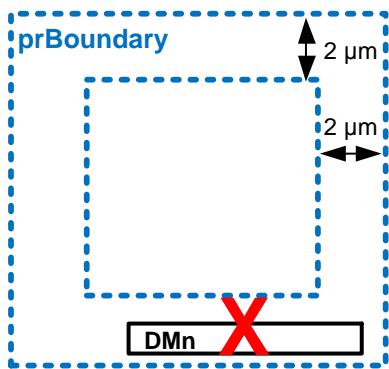


DMn.L.1



	Square (Utility Fill),
-1	Width x Length.,
-1	M0, M1, Mxs, Mx and Mxa., 0.12x1.4~0.24x0.7.,
Mya and My.,	0.108x0.450~2x2.,
Myz.,	0.180x0.900 ~ 0.270x1.800.,
Myx, Myz and Mz.,	0.36x1.28~1.8x1.8.,

DMn.W.1gU



6.3 Dummy VIA (DVIAn) Rules

(DVIAn, n = 0, x, xs, xa, ya, y, yy)

- To meet process window needs, it is a must to fill the dummy VIA by tsmc utility globally and uniformly.
- Use the utility dummy fill as a method for automated dummy VIA insertion
 - The TSMC DMn utility can insert DVIAn with good efficiency. It can support IP blocks, library cells, and full custom cells.
- In the TSMC utility, 1 kind of dummy VIA is generated, DVIAn.
 - DVIAn: dummy VIA
 - ◆ OPC on DVIA0, DVIAx, DVIAxs and DVIAxa
 - ◆ No OPC on DVIAya, DVIAy and DVIAyy
 - ◆ DVIAn for DVIA0, DVIA1, DVIAx, DVIAxa, VIAya, VIAy, and VIAyy only.
 - The distinction between VIA, DVIAn

	VIA	DVIAn	DVIAn
GDS datatype	420(0), 400(xs), 250(x), 290(xa), 330(ya), 350(y), 90(yy), 370(yx), 30(yz), 40(z), 80(r)	427(0), 407(xs) 252/253(x), 297(xa)	331(ya), 351(y), 91(yy)
Do OPC modification on it	Yes	Yes	No
Refer to it during OPC	Yes	Yes	Yes
Follow VIA rule	Yes	No	No

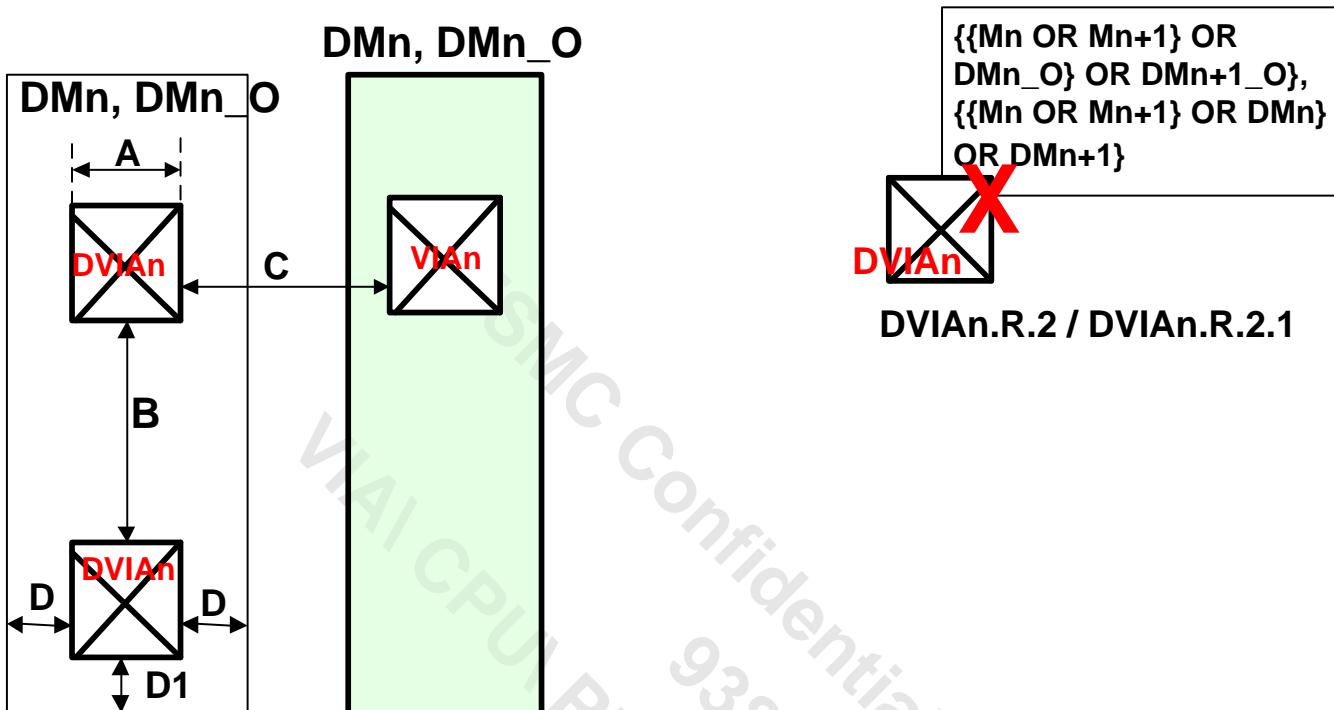
- Use the dummy layer DVIAnEXCL properly. This layer directs TSMC's utility that the area covered should be blocked from DVIAn fill operations.
- It is suggested to make sure that DVIAnEXCL is drawn over the following:
 - Sensitive circuits (such as SRAM sensitive function blocks and bit cell array) and analog circuits (such as DAV/ADC, and PLL)
 - RF application circuits
 - Pad areas for high frequency signals

For sensitive areas with auto-fill operations blocked by the DVIAnEXCL layer, careful manual uniform fill addition is still recommended so as to gain a better process window and electrical performance.

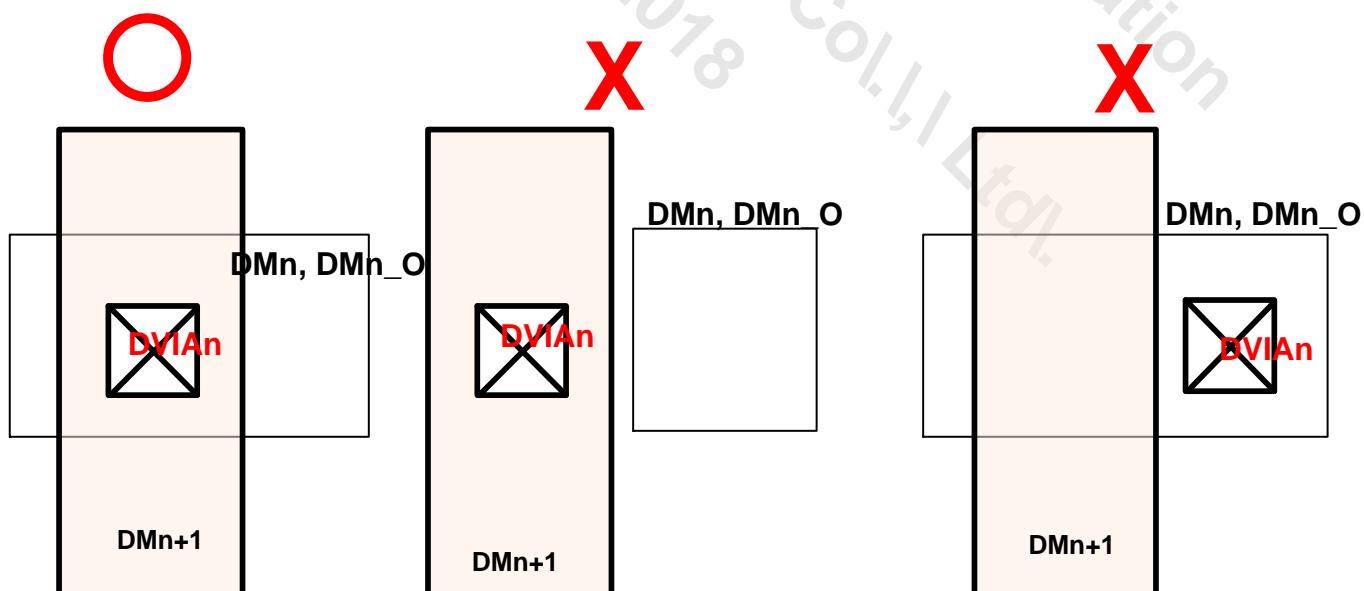
- For DVIAnEXCL, use the GDS layer numbers 150;n (n = 159,51,52,53,54,55,56,57,58,59,60,61,62,63).
- Revision of the following layers may necessitate re-filling of dummy VIA. Because of this, evaluate the impact on the metal/VIA layer mask carefully when any one of the following layouts is revised:
 - Mn/DMn/VIA/DVIAn/DMxEXCL and DVIAnEXCL layers. This layout revision impacts the Mn/VIA/Mn+1 masks.
 - LOGO/INDDMY. This revision impacts all the metal/VIA layer masks.
- Please refer to the "Dummy Pattern Fill Usage Summary" section in this chapter for additional information.

Rule No.	Description	Label	Op.	Rule
DVIAn.W.1	Width (maximum = minimum) (n = 0, xs, x, xa)	A	=	0.0200
DVIAn.W.2	Width (maximum = minimum) (n = ya or y)	A	=	0.0900
DVIAn.S.1	Space (n = x)	B	\geq	0.0440
DVIAn.S.1.1	Space (n = x) (DRC checks same color VIA space)	B	\geq	0.0950
DVIAn.S.1.2	Space (n = xa)	B	\geq	0.0950
DVIAn.S.1.3	Space (n = 0, xs)	B	\geq	0.0880
DVIAn.S.2	Space (n = ya or y)	B	\geq	0.3340
DVIAn.S.3	Space to VIAn (n = 0, xs , x, xa)	C	\geq	0.1000
DVIAn.S.3.1	Space to rectangular VIAn (n = 0, xs, x, xa)	C	\geq	0.1340
DVIAn.S.4	Space to VIAn (n = ya or y)	C	\geq	0.5000
DVIAn.EN.1	Enclosure by {DMn_O OR DMn} (n = x, xa)	D1	\geq	0
DVIAn.EN.1.0.1	Enclosure by {DMn_O OR DMn} (n = 0, xs)	D1	\geq	0.0020
DVIAn.EN.1.1	Enclosure by {DMn_O OR DMn} (at least two opposite sides) (n = 0, xs, x, xa)	D	\geq	0.0300
DVIAn.EN.2	Enclosure by DMn (n = ya or y)	D1	\geq	0.0080
DVIAn.EN.2.1	Enclosure by DMn (at least two opposite sides) (n = ya or y)	D	\geq	0.0900
DVIAn.R.1	DVIAn must be inside {DMn_O AND DMn+1_O}, {DMn_O AND DMn+1}, {DMn AND DMn+1_O}, {DMn AND DMn+1}. (n = 0, xs, x, xa)			
DVIAn.R.1.1	DVIAn must be inside {DMn AND DMn+1}. (n = ya or y)			
DVIAn.R.2	DVIAn INTERACT {{{Mn OR Mn+1} OR DMn_O} OR DMn+1_O} is not allowed. (n = ya or y)			
DVIAn.R.2.1	DVIAn INTERACT {Mn OR Mn+1} is not allowed. (n = 0, xs, x, xa)			
DVIAn.R.3	DVIAn is a must for Flip Chip in chip level. To comply tsmc dummy utility, DRC flags as violation when the area ratio of (DVIAn to DMn) & (DVIAn to DMn+1) are < 1% at the same time. (n = ya or y)			
DVIAyy.W.1	Width (maximum = minimum)	A	=	0.1060
DVIAyy.S.1	Space	B	\geq	0.1800
DVIAyy.S.2	Space to VIAyy	C	\geq	0.1800
DVIAyy.EN.1	Enclosure by DMyy	D1	\geq	0.0090
DVIAyy.EN.2	Enclosure by DMyy (at least two opposite sides)	D	\geq	0.0900
DVIAyy.EN.3	Enclosure by DMy	EN3	\geq	0.0090
DVIAyy.EN.4	Enclosure by DMy (at least two opposite sides)	EN4	\geq	0
DVIAyy.R.1	DVIAyy must be inside {DMyy AND DMyy+1} or {DMy AND DMyy+1}.			
DVIAyy.R.2	DVIAyy INTERACT {{{{My OR My+1} OR DMyy_O} OR DMyy+1_O} OR {{My OR DMy_O}}} is not allowed.			
DVIAyy.R.3	DVIAyy is a must for Flip Chip. To comply tsmc dummy utility, DRC flags as violation when the area ratio of ((DVIAyy to DMyy) & (DVIAyy to DMyy+1)) or (DVIAyy to DMyy+1) are < 1% at the same time.			

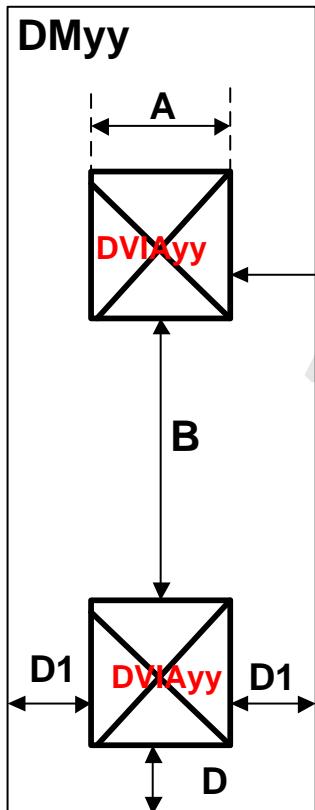
DVIAn



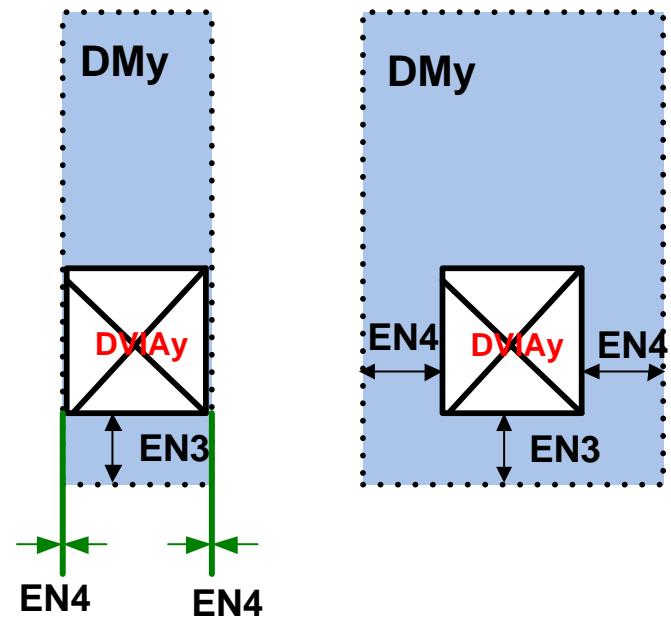
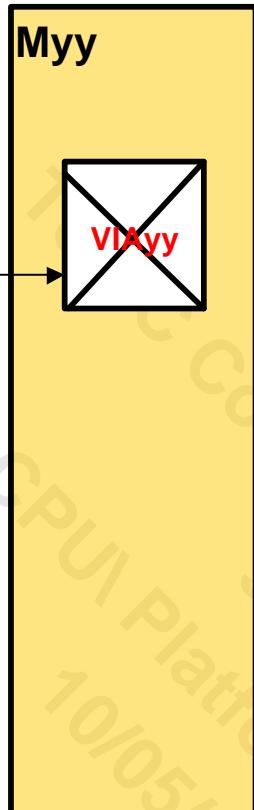
DVIAn.W.1 / DVIAn.W.2 / DVIAn.S.1 / DVIAn.S.1.1 /
 DVIAn.S.1.2 / DVIAn.S.2 / DVIAn.S.3 / DVIAn.S.3.1 /
 DVIAn.S.4 / DVIAn.EN.1 / DVIAn.EN.1.1 / DVIAn.EN.2
 / DVIAn.EN.2.1



DVIAn.R.1 / DVIAn.R.1.1

DVIAYy

**DVIAYy.W.1 / DVIAYy.S.1 /
DVIAYy.S.2 / DVIAYy.EN.1 /
DVIAYy.EN.2**

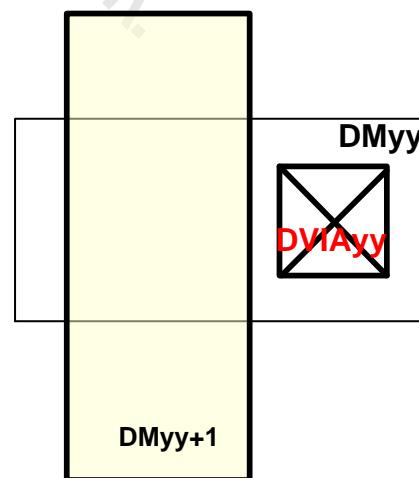
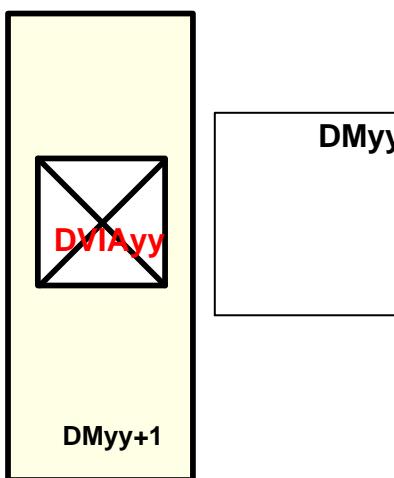
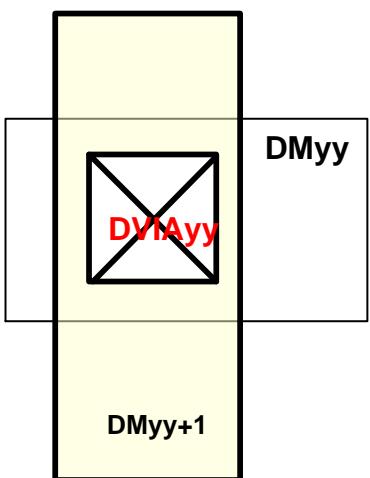


DVIAYy.EN.3 / DVIAYy.EN.4

$\{\{\{(Myy \text{ OR } Myy+1) \text{ OR } DMyy_O\} \text{ OR } DMyy+1_O\} \text{ OR } \{My \text{ OR } DMy_O\}\}$



DVIAYy.R.2



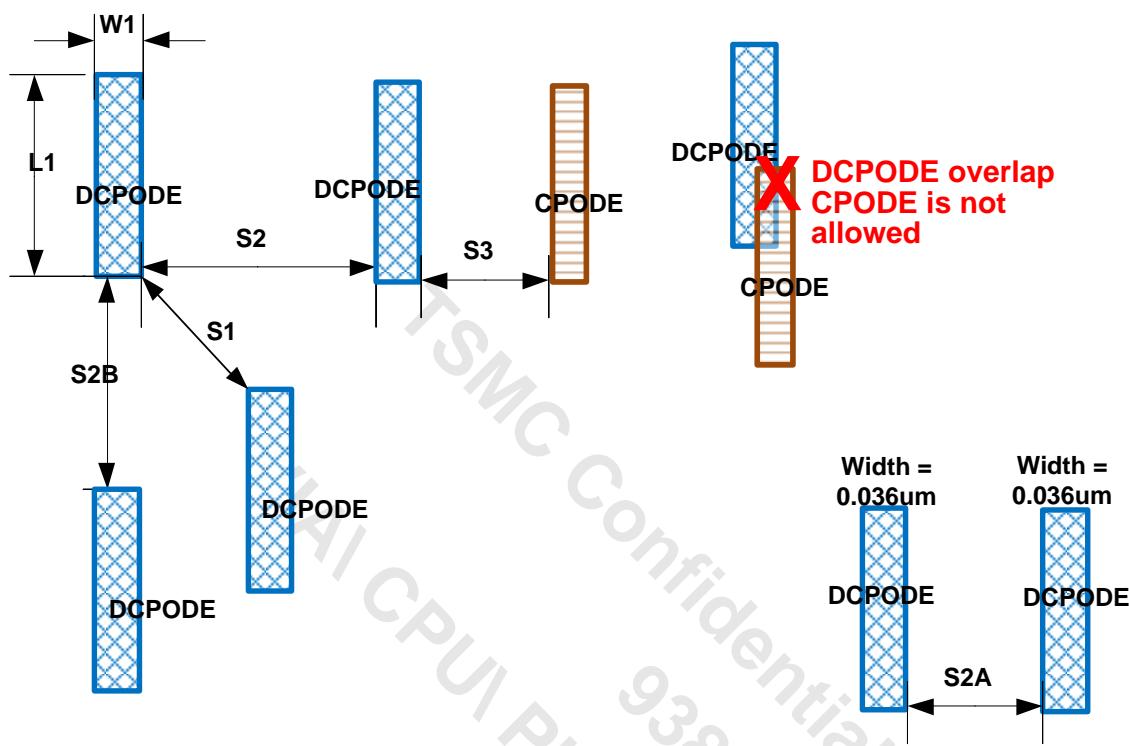
DVIAYy.R.1

6.4 Dummy CPODE (DCPODE) Rules

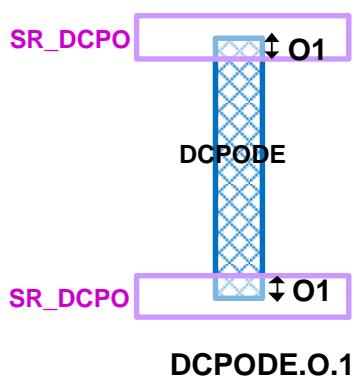
DCPODE (CAD layer: 206;33) is only used for the dummy cell.

Rule No.	Description	Label	Op.	Rule
DCPODE.W.1	Width in horizontal direction	W1	=	0.0110, 0.0360
DCPODE.S.1	Space	S1	\geq	0.0460
DCPODE.S.2	Space of DCPODE in horizontal direction	S2	\geq	0.1030
DCPODE.S.2.1	Space of DCPODE [width = 0.036 μm] in horizontal direction	S2A	\geq	0.1960
DCPODE.S.2.2	Space of DCPODE in vertical direction	S2B	\geq	0.1200
DCPODE.S.3	Space to CPODE (Overlap is not allowed)	S3	\geq	0.1030
DCPODE.O.1	Short side of DCPODE overlap of SR_DCPO in vertical direction	O1	=	0.0080
DCPODE.L.1	Length of DCPODE in vertical direction	L1	\geq	0.2400
DCPODE.R.1	DCPODE must be inside {Dummy_Cell NOT DC_WPO}			
DCPODE.R.2	DCPODE must be rectangular orthogonal to grid			
DCPODE.R.3	DCPODE inside chip corner stress relief area is not allowed (Except following conditions: 1. seal-ring, stress relief patterns drawn by customers).			
DCPODE.R.4	DCPODE short side must inside SR_DCPO (Except DC2_CORE)			

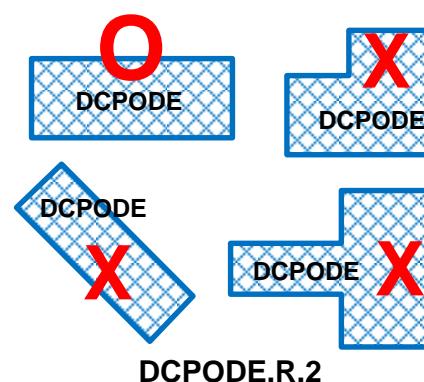
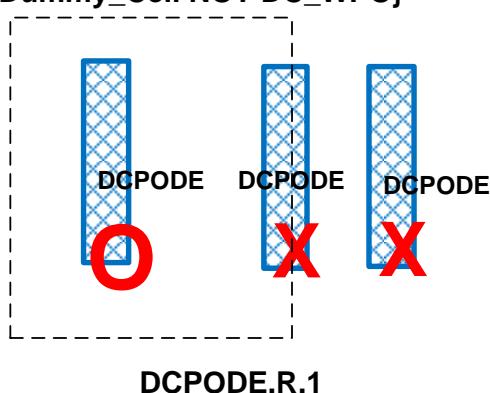
DCPODE

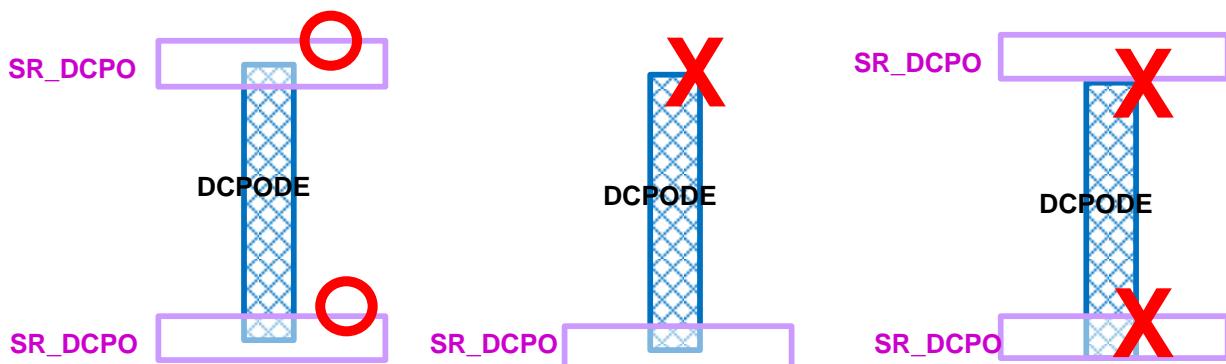


DCPODE.W.1/DCPODE.S.1
DCPODE.S.2/DCPODE.S.2.2
DCPODE.S.3/DCPODE.L.1



{Dummy_Cell NOT DC_WPO}





DCPODE short side must interact SR_DCPO (abut is not allowed)

DCPODE.R.4

VIAI CPU Platform Col., I Ltd.
938214
10/05/2018

6.5 Dummy TCD Rules and Filling Guideline

This chapter contains the following topics:

- 6.4.1 Dummy TCD rules
- 6.4.2 Dummy TCD Insertion Guideline

6.5.1 Dummy TCD Rules

1. In order to meet the extremely tight process control, Dummy TCD is required. According to design rules, there should be at least one full stack dummy TCD (165;20) in each 2mmx2mm window.
2. Dummy TCD insertion
 - Use EDA tools to insert full stacked dummy TCD (165;20) in floor plan stage, and to comply with dummy TCD density rules and count rule.
 - ◆ TSMC full stacked DTCD take cares the metal till Mytop layer. You have to identify the correct Mytop layer to select the corresponding full stacked dummy TCD cell gds. For example, if the Mytop layer of your chip is M12, you have to choose N7+_DTCD_ALL_M12_160415 cell to do placement in floor plan stage.
 - If your IP size is close to, or \geq 2mmx2mm, you have to manually insert full stacked dummy TCD in your IP
 - Use TSMC's auto-fill dummy utilities (documents: *T-N07-CL-DR-022-X2/X3, X is the code of EDA tool*) to insert dummy TCD at final GDS, to increase dummy TCD counts and improve dummy TCD uniformity.
 - ◆ TSMC's auto-fill dummy utilities are only supplement. It cannot meet dummy TCD density and count rules.
 - ◆ Dummy utility only support FEOL/BEOL dummy TCD. It does not support dummy TCD for VC
3. Three folders are included in the tarball (file name: N07+_DTCD_library_kit.v0d5.tar.gz): (1) gds, (2) LEF: P&R physical library for dummy TCD, (3) NDM: P&R physical library for dummy TCD.

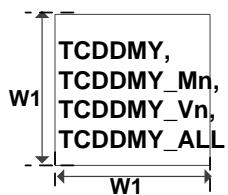
Process	TCD Name	TCD CAD no.	Cell name in gds	Cell size
Stacked DTCD gds from FEOL/MEOL till M4	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M4_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M5	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M5_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M6	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M6_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M7	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M7_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M8	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M8_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M9	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M9_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M10	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M10_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M11	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M11_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M12	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M12_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M13	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M13_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M14	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M14_160415	5.04 x 5.04
Stacked DTCD gds from FEOL/MEOL till M15	TCDDMY_ALL	165;20	N7+_DTCD_ALL_M15_160415	5.04 x 5.04

6.5.1.1 Dummy TCD Rules

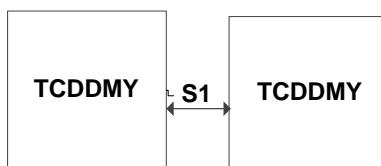
Rule No.	Description	Label	Op.	Rule
DTCD.0	1. FEOL/MEOL dummy TCD recognized layer is TCDDMY. BEOL dummy TCD recognized layer is TCDDMY_Mn & TCDDMY_Vn. Full stack dummy TCD recognized layer is TCDDMY_ALL. 2. TCDDMY_Mn is offered for M0/M1/Mx/Mxa/Mya/My. Mn = 0~12 for metal layers. n starts from 3 for Mxa, 4 for Mya, and 5 for My. 3. TCDDMY_Vn is offered for VIA0/VIAx/VIAxa/VIAya/Vy. Vn = 0~11 for Via layers. n starts from 2 for VIAxa, 3 for VIAya, and 4 for VIAy. 4. Full stack dummy TCD includes TCDDMY, TCDDMY_Mn in gds. It also include TCDDMY_Vn & dummy TCD for VC after tsmc swap while mask making. 5. You have to implement TCDDMY_ALL manually or by P&R EDA tool. You can implement FEOL/MEOL and BEOL dummy TCD manually or by tsmc dummy utility.			
DTCD.W.1	Width of {{TCDDMY OR {TCDDMY_Mn OR TCDDMY_Vn}} OR TCDDMY_ALL}	W1	=	5.04
DTCD.S.1	Space of TCDDMY	S1	\geq	5
DTCD.S.1.1	Space of TCDDMY_Mn	S1A	\geq	5
DTCD.S.3	Space of TCDDMY to OD, DNW, NW, PO, OD2, CPO, MD, CMD, MP, VT, RH_TNB, VAR, IBJTDY, INDDMY, MOMDMY, DIODMY, NWDMY, NT_N, MetalFuse (Except Dummy_Cell)	S3	\geq	1
DTCD.S.3.1	Space of TCDDMY to Dummy_Cell, ALL_CPO, ALL_MD, ALL_CMD, ALL_MP	S3A	\geq	0.2000
DTCD.S.4	Space of TCDDMY to SR_DOD, NP, PP (Except Dummy_Cell)	S4	\geq	0.2000
DTCD.S.5	Space of TCDDMY to SR_DPO [Width \leq 0.011 μm]	S5	\geq	0.0500
DTCD.S.5.1	Space of TCDDMY to SR_DPO [0.011 μm $<$ Width $<$ 0.072 μm]	S5A	\geq	0.0800
DTCD.S.5.2	Space of TCDDMY to SR_DPO [Width \geq 0.072 μm]	S5B	\geq	0.1000
DTCD.S.7	Space of TCDDMY_Mn to Mn	S7	\geq	1
DTCD.S.8	Space of TCDDMY_Mn to {DMn OR DMn_O}	S8	\geq	0.2000
DTCD.S.8.1	Space of TCDDMY_M0 to {CM0A OR CM0B}	S8A	\geq	0.0500
DTCD.S.9	Space of {TCDDMY OR TCDDMY_Mn} to ICOVL_SINGLE	S9	\geq	15
DTCD.S.10	Space of {TCDDMY OR TCDDMY_Mn} to {SRM OR SRAMDMY}	S10	\geq	2
DTCD.S.10.1	Space of {TCDDMY OR TCDDMY_Mn} to {LOGO OR CSRDMY (166;0)}	S10A	\geq	5
DTCD.S.11	Space of TCDDMY_Mn to INDDMY.	S11	\geq	14.4
DTCD.S.12	Space of TCDDMY_Mn to MOMDMY.	S12	\geq	0.2500
DTCD.DN.1	Minimum density of TCDDMY_ALL in window 2000 μm x 2000 μm , stepping 2000 μm DRC checks CHIP or IP area > 2000 μm x 2000 μm		$>$	0%
DTCD.R.5	TCDDMY overlap ALL_OD, OD2, ALL_COD_H, ALL_COD_V, NW, DNW, ALL_PO, ALL_CPO, TPO, NP, PP, VT, ALL_MD, ALL_CMD, ALL_MP, Dummy_Cell, RH_TNB, VAR, IBJTDY, DIODMY, NWDMY, NT_N, MetalFuse is not allowed			
DTCD.R.5.1	TCDDMY_Mn overlap Mn, DMn, DMn_O, CM0A, CM0B, is not allowed			
DTCD.R.5.2	{TCDDMY OR TCDDMY_Mn} overlap ICOVL_SINGLE, SRM, SRAMDMY, LOGO, INDDMY, MOMDMY, CSRDMY is not allowed			
DTCD.R.7	TCDDMY_Vn must be drawn identically with TCDDMY_Mn & TCDDMY_Mn+1.			

Rule No.	Description	Label	Op.	Rule
DTCD.R.9.0	<p>Place TCDDMY_ALL as uniform as possible. The related rule is defined by DTCD.R.9.1. Insert TCDDMY, TCDDMY_Mn & TCDDMY_Vn by dummy utility is supplementary DRC methodology:</p> <ol style="list-style-type: none"> 1. Calculate die number in a reticle (Column x Row), same as the method in sec.6.5.1. 2. Calculate total dummy TCD counts in Chip_Boundary (C) 3. TCDDMY counts in a reticle = C*(Column x Row) 			
DTCD.R.9.1	<p>Minimum TCDDMY_ALL unit counts in a reticle. For example, in chip level, at least 144 unit counts for 1X1 die, 72 unit counts for 1X2 or 2x1 die. (Except following conditions:</p> <ol style="list-style-type: none"> 1. For 1x1 die, if the Chip_Boundary with SEALRING area (A) $< 237 \text{ mm}^2$, the min TCDDMY_ALL unit counts ≥ 100, 2. For 1x1 die, if the Chip_Boundary with SEALRING area (A) $237 \text{ mm}^2 \leq A < 262 \text{ mm}^2$, the min TCDDMY_ALL unit counts ≥ 110, 3. For 1x1 die, if the Chip_Boundary with SEALRING area (A) $262 \text{ mm}^2 \leq A < 288 \text{ mm}^2$, the min TCDDMY_ALL unit counts ≥ 120, 4. For 1x1 die, if the Chip_Boundary with SEALRING area (A) $288 \text{ mm}^2 \leq A < 314 \text{ mm}^2$, the min TCDDMY_ALL unit counts ≥ 130, 5. For 1x1 die, if the Chip_Boundary with SEALRING area (A) $314 \text{ mm}^2 \leq A < 324 \text{ mm}^2$, the min TCDDMY_ALL unit counts ≥ 140.) 		\geq	144
DTCD.R.9.4	TCDDMY_ALL (165;20) must be drawn identical to TCDDMY, TCDDMY_Mn and TCDDMY_Vn			
DTCD.R.10	TCDDMY_Mn is not allowed in Myy, Myx, Myz, Mz, Mr metal layers			
DTCD.R.11	<p>TCDDMY_ALL must interact corresponding TCDDMY, TCDDMY_Mn for M0, M1, Mx, Mxa, Mya, My & TCDDMY_Vn for V0, Vx, Vxa, Vya, Vy</p> <p>Identify My top layer of your chip to select the corresponding DTCD cell. e.g. for 12M_1x1xa1ya4y2yy2z metal scheme, TCDDMY_ALL must interact TCDDMY_Mn (n = 0~8) & TCDDMY_Vn (n = 0~7)</p>			

DTCD



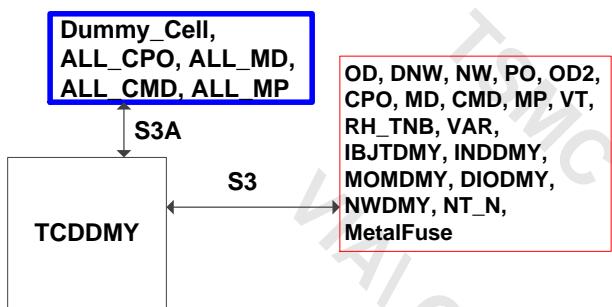
DTCD.W.1



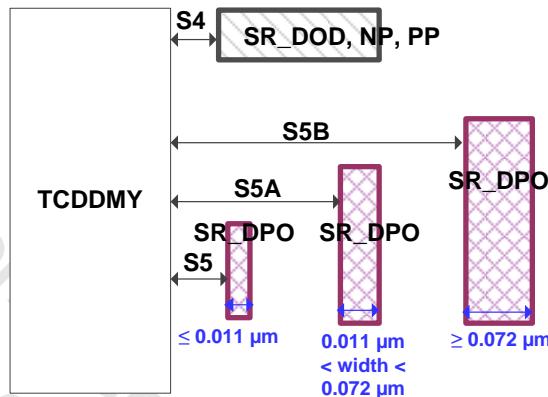
DTCD.S.1



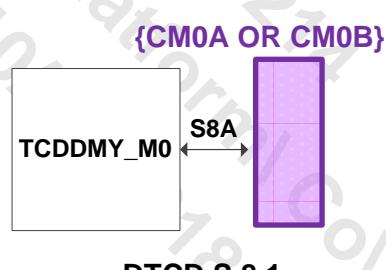
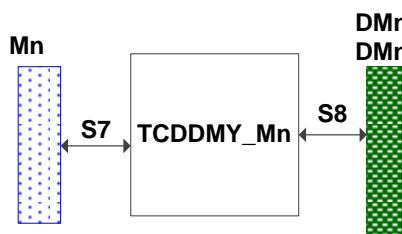
DTCD.S.1.1



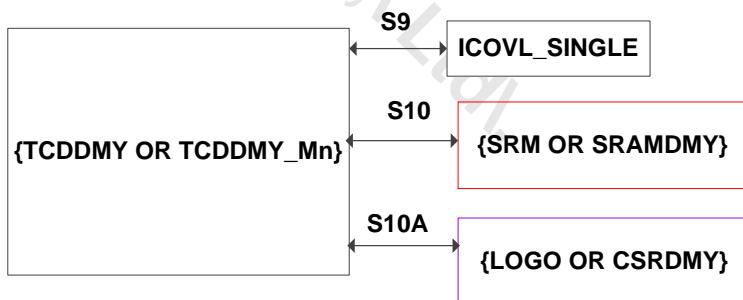
DTCD.S.3 / DTCD.S.3.1



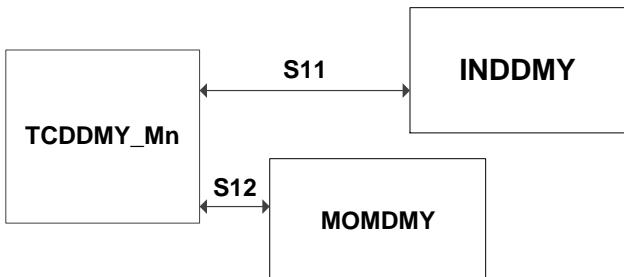
DTCD.S.4 / DTCD.S.5 / DTCD.S.5.1 / DTCD.S.5.2



DTCD.S.7 / DTCD.S.8

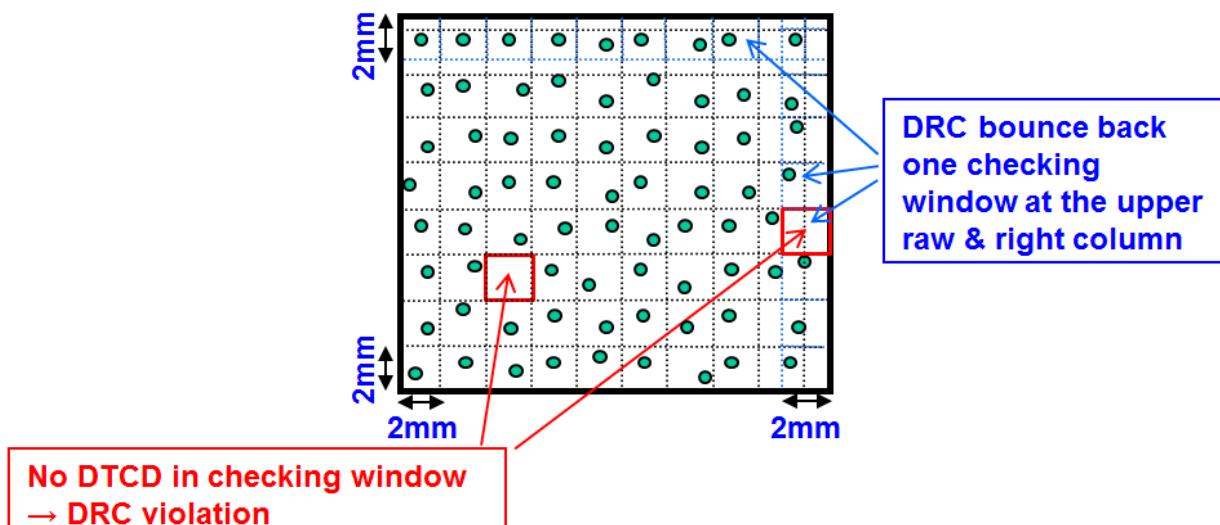


DTCD.S.9 / DTCD.S.10 / DTCD.S.10.1

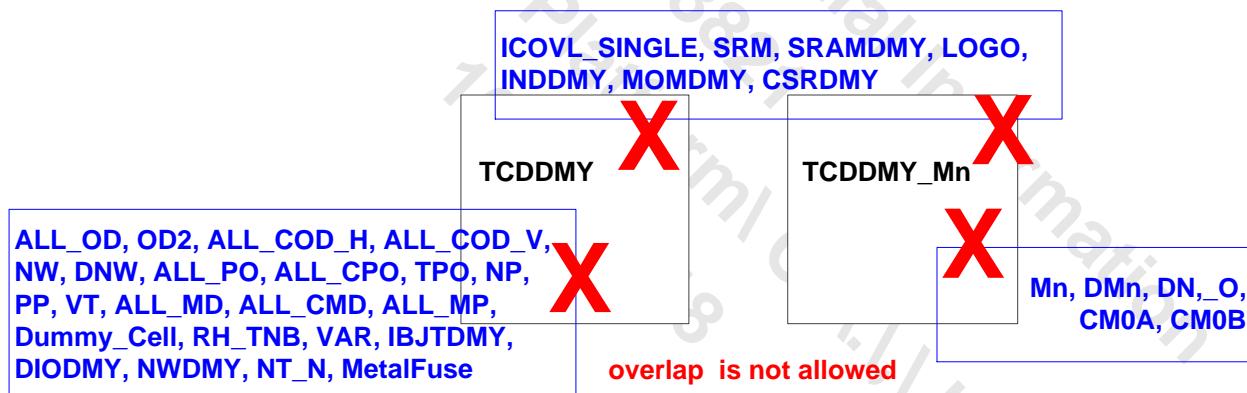


DTCD.S.11/ DTCD.S.12

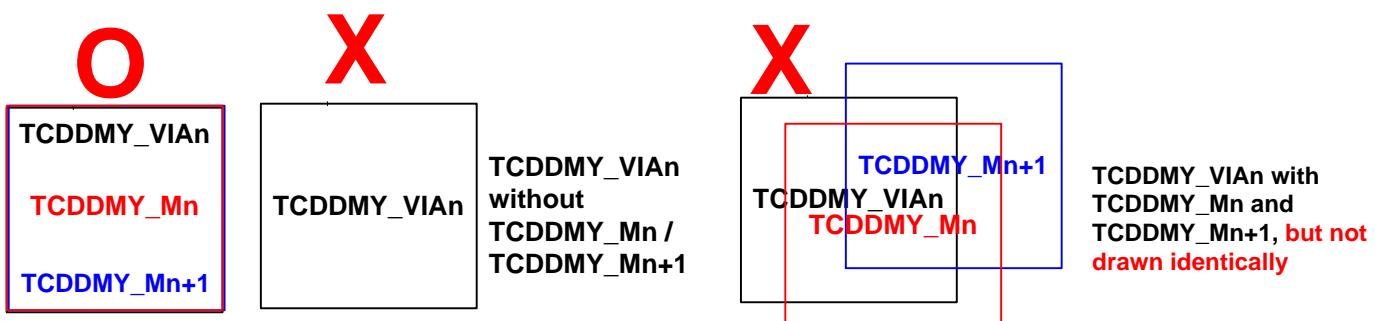
Example for Dummy TCD density calculation:
Chip size = 19 mm x 16.5 mm (9 units x 8 units)



DTCD.DN.1

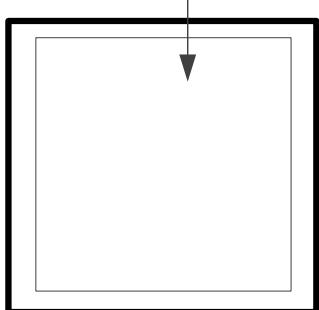


DTCD.R.5 / DTCD.R.5.1 / DTCD.R.5.2

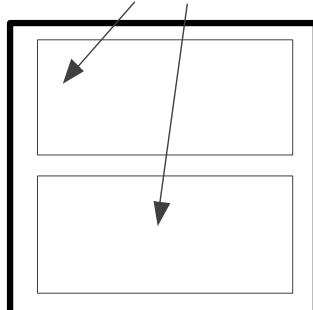
**TCDDMY_Vn must be drawn identically with TCDDMY_Mn & TCDDMY_Mn+1.**

DTCD.R.7

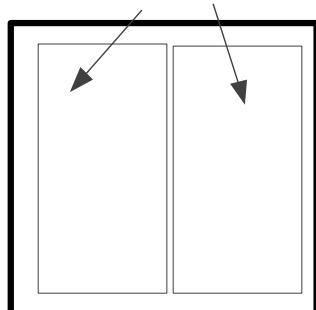
1X1 die: 144 unit counts



1X2 die: 72 unit counts

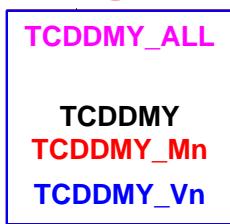


2X1 die: 72 unit counts



DTCD.R.9.1

O

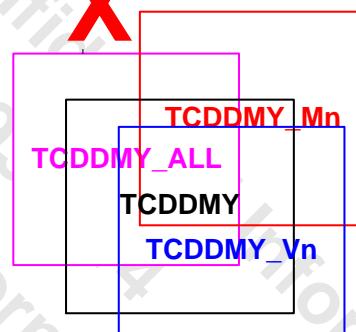


X



TCDDMY_ALL
without
TCDDMY /
TCDDMY_MN /
TCDDMY_Vn

X



TCDDMY_ALL with
TCDDMY, TCDDMY_Mn,
and TCDDMY_Vn, but
not drawn identically

TCDDMY_ALL must be drawn identically to TCDDMY & TCDDMY_Mn & TCDDMY_Vn

DTCD.R.9.4

Myy, Myx, Myz, Mz, Mr



TCDDMY_Mn is not allowed in Myy, Myx, Myz, Mz, Mr metal layers

DTCD.R.10

6.5.2 Dummy TCD Insertion Guideline

6.5.2.1 Overview

- Inserting full stacked dummy TCD (165;20) in chip design planning stage is required to meet even distribution requirement.
- You have to manually insert full stacked DTCD in your IP as your IP is close to, or $\geq 2\text{mm} \times 2\text{mm}$
- Post-route dummy TCD (separate FEOL/MEOL & BEOL DTCD) insertion by utility is also important. Don't turn off DTCD insertion function while executing dummy utility.

6.5.2.2 Dummy TCD Insertion in Chip Level Planning Stage

- Use P&R tool to insert full stacked DTCD (165;20).
- Full stacked DTCD needs to be distributed uniformly. Max 3mm space is recommended.
- Make sure DRC clean for full stacked DTCD density & count rule in this stage.

6.5.2.3 Dummy TCD Insertion in Macro Design

- If your IP size is close to, or $\geq 2\text{mm} \times 2\text{mm}$, you have to manually insert full stacked DTCD (165;20) in your IP center
- Minimize dummy macro electrical impact to main pattern circuits like std cell, SRAM, analog IP by either one of the approaches as below.
 - For custom IP design, reserve at least 2 μm space around dummy TCD macro by placement blockage as Fig.6.4.2.3.1, to let utility insert dummy OD/dummy PO.
 - For STD cell array design, reserve at least X/Y space around dummy TCD macro. And use boundary cells to surround dummy TCD macro as Fig. 6.4.2.3.2.

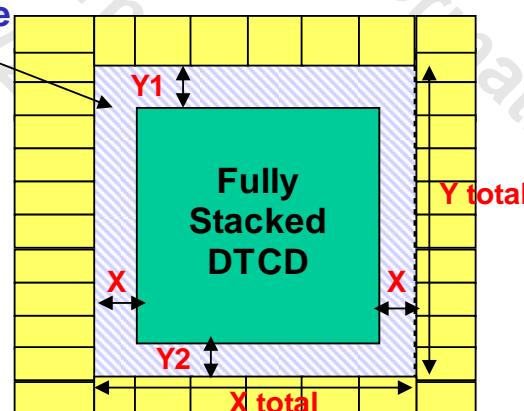
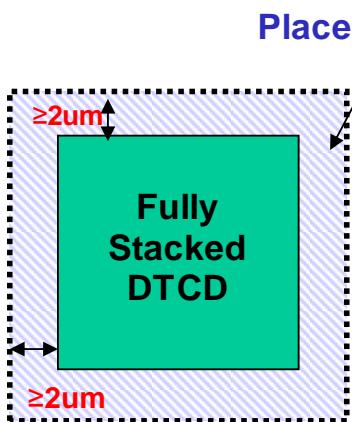


Fig.6.4.2.3.1

Fig. 6.4.2.3.2

	X	X total
P57	2.04	9.12
P63	2.016	9.072

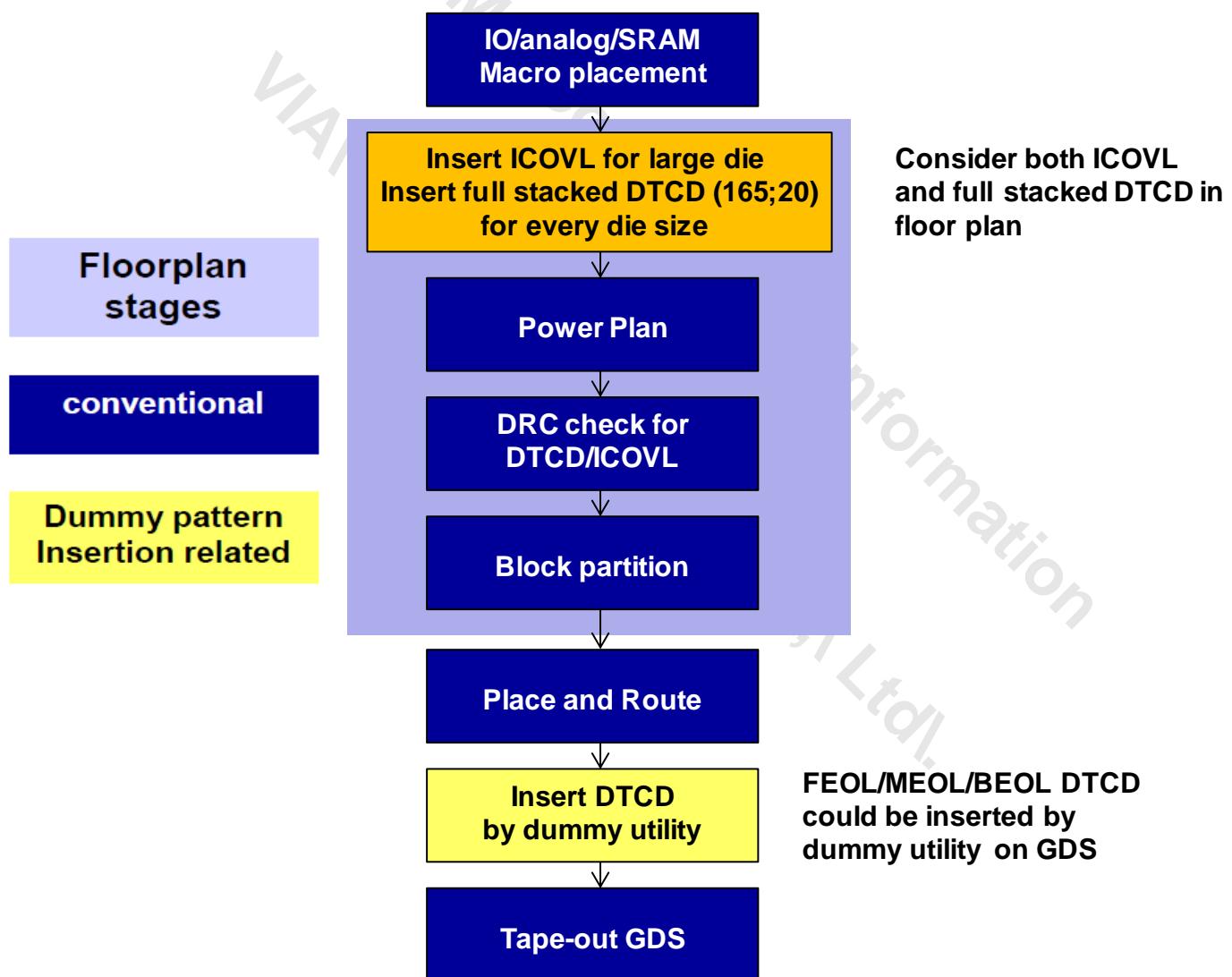
	Y1	Y2	Y total
H240	2.34	2.22	9.6
H300	2.34	2.22	9.6

- Dummy TCD enclosure of IP needs to follow FB.EN.7.1 and DTCD.DN.1

6.5.2.4 Dummy TCD Placement in Chip Final Stage

- In order to increase DTCD counts & improve DTCD uniformity, it is important to use dummy utilities to insert individual FEOL/MEOL & BEOL DTCD at final gds stage. Do not turn off DTCD insertion function while executing dummy utility.

6.5.2.4.1 Dummy TCD Macro Insertion Flow



6.6 In Chip Overlay (ICOVL) Rule and Filling Guideline

- 6.5.1 In Chip Overlay (ICOVL) Rules
- 6.5.2 N7+ In-Chip OVL Insertion Methodology

6.6.1 In Chip Overlay (ICOVL) Introduction

- ICOVL is must for large chip.
 - Large chip definition: the die count in a reticle is 1x1, 1x2, 2x1, 1x3, 3x1, 2x2 (Column x Row).
 - Die count in a reticle (Column x Row) in DRC:
 - ◆ Column = an integer by rounding down $[(26000 - Sx) / (Cx + Sx)]$
 - ◆ Row = an integer by rounding down $[(33000 - Sy) / (Cy + Sy)]$
 - Sx and Sy: Scribeline width in X- and Y-direction. Single scribeline width = 65.6 μm . Multiple scribeline width = $n * 60 \mu\text{m}$ ($n = 2,3,4\dots$)
 - Cx and Cy: The dimension of (Chip_Boundary with SEALRING_ALL) = (Chip_Boundary + 2*21.6 μm) in X- and Y-direction respectively.
 - For example, if the Chip_Boundary size is 13800 $\mu\text{m} * 10800 \mu\text{m}$, the scribeline width in X- and Y-direction is 360 μm and 600 μm , the die count in a reticle is 1x2 as the following calculation:
 - ◆ Column = round down of $[(26000 - 360) / ((13800 + 2*21.6) + 360)] = 1$
 - ◆ Row = round down of $[(33000 - 600) / ((10800 + 2*21.6) + 600)] = 2$
 - Customer must input correct scribeline width during DRC check, otherwise DRC will calculate by default setting - 180 μm (triple scribelines). The variable settings in DRC deck can be modified based on your real tape-out situation.

```
// The following variables are for Mask Field Utilization Check. Please change it if using different value.
VARIABLE ScribeLineX 180.0 // Width of scribe_line X (um) for Mask Field Utilization (MFU)
VARIABLE ScribeLineY 180.0 // Width of scribe_line Y (um) for Mask Field Utilization (MFU)
```

You can modify the variables in DRC deck based on real tape-out situation

Figure 6.5.1.1 Variable sets of scribeline width in DRC deck

- Three folders are including in tarball file (name: N07+_ICOVL_library_kit.v0d5.tar.gz.tar.gz): (1) gds, (2) LEF: P&R physical library for ICOVL, (3) NDM: P&R physical library for ICOVL.
- ICOVL cells includes ICOVL_A, ICOVL_B, ICOVL_B1, ICOVL_C, ICOVL_D, ICOVL_D1, ICOVL_E
 - ICOVL_A is square. You can place individual ICOVL_A.
 - ICOVL_B, ICOVL_B1, ICOVL_C, ICOVL_D, ICOVL_D1 and ICOVL_E are rectangles.
 - You have to group (ICOVL_B or ICOVL_B1) with (ICOVL_C or ICOVL_E) together. Group (ICOVL_D or ICOVL_D1) with (ICOVL_C or ICOVL_E) together.
- Each ICOVL_SINGLE cell includes (165;6xx) block layer. For example, (165;612) block layer means Mytop layer is M12. Therefore, M13 is allowed to route above ICOVL_SINGLE.

Table 6.5.1 ICOVL_XX CAD layer

ICOVL_XX Name	ICOVL CAD no.
ICOVL_SINGLE	165;320
ICOVL_A	165;70
ICOVL_B	165;71
ICOVL_C	165;72
ICOVL_D	165;73
ICOVL_E	165;74
ICOVL_B1	165;521
ICOVL_D1	165;523

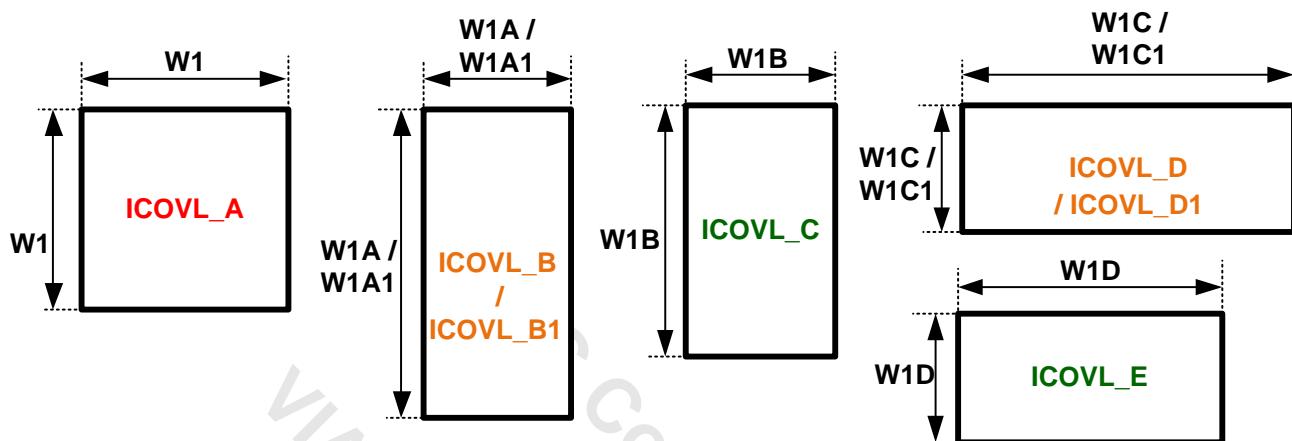
Rule No.	Description	Label	Op.	Rule
ICOVL.0	<p>1. ICOVL includes FEOL/MEOL & BEOL. BEOL part is offered for M0/M1/Mx/Mxa/Mya/My layers.</p> <p>2. ICOVL, or ICOVL_SINGLE (165;320) includes ICOVL_A (165;70), ICOVL_B (165;71), ICOVL_C (165;72), ICOVL_D (165;73), ICOVL_E (165;74), ICOVL_B1 (165;521), ICOVL_D1 (165;523), where</p> <ul style="list-style-type: none"> 2-1. ICOVL_A is square. You can place individual ICOVL_A. 2-2. ICOVL_B, ICOVL_B1, ICOVL_C, ICOVL_D, ICOVL_D1 and ICOVL_E are rectangles. 2-3. You have to group {ICOVL_B OR ICOVL_B1} with {ICOVL_C OR ICOVL_E} together. Group {ICOVL_D OR ICOVL_D1} with {ICOVL_C OR ICOVL_E} together. (ICOVL.R.3.4, ICOVL.R.3.5) <p>3. ICOVL_Single_Center: Center Grid (10 μm x 10 μm) of ICOVL_SINGLE</p> <p>4. ICOVL_set includes ICOVL_A, ICOVL_BC, ICOVL_BE, ICOVL_DE, ICOVL_DC, where</p> <ul style="list-style-type: none"> ICOVL_BC = {{{ICOVL_B OR ICOVL_B1} OR ICOVL_C} SIZING up/down 500 μm} ICOVL_BE = {{{ICOVL_B OR ICOVL_B1} OR ICOVL_E} SIZING up/down 500 μm} ICOVL_DE = {{{ICOVL_D OR ICOVL_D1} OR ICOVL_E} SIZING up/down 500 μm} ICOVL_DC = {{{ICOVL_D OR ICOVL_D1} OR ICOVL_C} SIZING up/down 500 μm} <p>5. Cx and Cy are dimension of (Chip Boundary with SEALRING_ALL) = (Chip Boundary + 2*21.6 μm) in H and V respectively</p>			
ICOVL.W.1	Width of ICOVL_A in horizontal/vertical direction	W1	=	150/150
ICOVL.W.1.1	Width of ICOVL_B in horizontal/vertical direction	W1A	=	60/210
ICOVL.W.1.1.1	Width of ICOVL_B1 in horizontal/vertical direction	W1A1	=	30/420
ICOVL.W.1.2	Width of ICOVL_C in horizontal/vertical direction	W1B	=	60/165
ICOVL.W.1.3	Width of ICOVL_D in horizontal/vertical direction	W1C	=	210/60
ICOVL.W.1.3.1	Width of ICOVL_D1 in horizontal/vertical direction	W1C1	=	420/30
ICOVL.W.1.4	Width of ICOVL_E in horizontal/vertical direction	W1D	=	165/60
ICOVL.W.2	Width of {My AND {ICOVL_SINGLE SIZING 8 μm}}. [My is Mn+1, Mn+2. n is the last inter metal (Mx, Mxa, Mya, My) layer number]. (Except DMyy_O) DRC flags: {My [width < 0.124 μm] AND {ICOVL_SINGLE SIZING 8 μm}}	W2	≥	0.1240
ICOVL.S.1	Space of ICOVL_A, ICOVL_B, ICOVL_C, ICOVL_D, ICOVL_E, ICOVL_B1, ICOVL_D1. (Overlap is not allowed) (Except following conditions: 1. {ICOVL_C OR ICOVL_E} space to {ICOVL_B OR ICOVL_B1} ≤ 500 μm, 2. {ICOVL_C OR ICOVL_E} space to {ICOVL_D OR ICOVL_D1} ≤ 500 μm)	S1	≥	1500
ICOVL.S.2.1	Space of {ICOVL_B OR ICOVL_B1} to ICOVL_C, ICOVL_E. (Overlap is not allowed)	S2A	=	0, 1~500, ≥ 1500
ICOVL.S.2.2	Space of {ICOVL_D OR ICOVL_D1} to ICOVL_C, ICOVL_E. (Overlap is not allowed)	S2B	=	0, 1~500, ≥ 1500
ICOVL.S.2.3	Space of ICOVL_SINGLE to ALL_OD, ALL_PO, ALL_CPO, ALL_MD, ALL_CMD, ALL_MP, DMn, DMn_O, {NP OR PP} [INSIDE Dummy_Cell]. (Overlap is not allowed). (n is 0, 1, xs, x, xa, ya, y)	S2C	≥	0.2000
ICOVL.S.3	Space of ICOVL_SINGLE to NW, DNW, OD, OD2, ALL_COD_H, ALL_COD_V, PO, CPO, TPO, NT_N, NP, PP, VT, MD, CMD, MP, RH_TNB, SRM, SRAMDMY, IBJTDMDY (Overlap is not allowed). (Except Dummy_Cell)	S3	≥	15
ICOVL.S.4	Space of ICOVL_SINGLE to M0, M1~Mn, CM0, VIA0, VIA1~VIA_n-1, INDDMY, MOMDMY, LOGO (Overlap is not allowed). (n is xs, x, xa, ya, y) (Except DMn, DMn_O)	S4	≥	8

Rule No.	Description	Label	Op.	Rule
ICOVL.S.4.1	Space of {Myy AND {ICOVL_SINGLE SIZING 8 μm }}. [Myy is Mn+1, Mn+2. n is the last inter metal (Mx, Mxa, Mya, My) layer number]. (Except DMyy_O)	S4A	\geq	0.2560
ICOVL.R.3.4	{ICOVL_B OR ICOVL_B1} environment need to pass either one of below conditions: 1. {{ICOVL_B OR ICOVL_B1} SIZING 500 μm } interact one ICOVL_C or ICOVL_E			
ICOVL.R.3.5	{ICOVL_D OR ICOVL_D1} environment need to pass either one of below conditions: 1. {{ICOVL_D OR ICOVL_D1} SIZING 500 μm } interact one ICOVL_C or ICOVL_E			
ICOVL.R.7.1 ^U	Do NOT put ICOVL_SINGLE on top row by (1) Dividing Chip_Boundary Y direction into 8 segments for 1X1 die or 2X1 die or 3X1 die (2) Dividing Chip_Boundary Y direction into 4 segments for 1X2 die or 2X2 die (3) Dividing Chip_Boundary Y direction into 3 segments for 1X3 die			
ICOVL.R.10	At least 6 respective ICOVL_set must be fully inside Central_Zone for 1X1 die Definition of Central_Zone: {((Chip_Boundary with SEALRING_ALL) SIZING -Cx/8 in horizontal direction} SIZING -Cy/8 in vertical direction)			
ICOVL.R.11	At least 3 respective ICOVL_set for 2X1 die			
ICOVL.R.12	At least 2 respective ICOVL_set for 1X2 die or 3X1 die			
ICOVL.R.13	At least 1 respective ICOVL_set for 1X3 die or 2X2 die			
ICOVL.R.14.0	Put ICOVL_set as uniform as possible. The related rules are defined by: 1X1 die: ICOVL.R.14.1, and ICOVL.R.14.3, ICOVL.R.14.7 and ICOVL.R.49 1X2 die: ICOVL.R.14.1, and ICOVL.R.14.4 and ICOVL.R.14.8 1X3 die: ICOVL.R.14.1, and ICOVL.R.14.5 and ICOVL.R.14.8 2X1 die: ICOVL.R.14.2, and ICOVL.R.14.4 and ICOVL.R.14.8 2X2 die: ICOVL.R.14.1, and ICOVL.R.14.4 and ICOVL.R.14.8 3X1 die: ICOVL.R.14.2, and ICOVL.R.14.6 and ICOVL.R.14.7 DRC generates two ICOVL_virtuels (150 μm x 150 μm) for ICOVL.R.14.1~ICOVL.R.14.8: 1X1 or 1X2 or 1X3 die: at 5500 μm (X1) from two corners of Chip_Boundary along Chip_Boundary top edge 2X1 or 2X2 die: at 2500 μm (X1) from two corners of Chip_Boundary along Chip_Boundary top edge 3X1 die: at 1800 μm (X1) from two corners of Chip_Boundary along Chip_Boundary top edge			
ICOVL.R.14.1	Only one polygon is allowed in Chip_Boundary by {{ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} SIZING 6500 μm (X2)} for 1X1 or 1X2 or 1X3 or 2X2 die Only one polygon is allowed in Chip_Boundary by {{ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} SIZING 6500 μm (X2)} for 1X1 or 1X2 or 1X3 or 2X2 die			
ICOVL.R.14.2	Only one polygon is allowed in Chip_Boundary by {{ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} SIZING 8000 μm (X2)} for 2X1 die or 3X1 die Only one polygon is allowed in Chip_Boundary by {{ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} SIZING 8000 μm (X2)} for 2X1 die or 3X1 die			

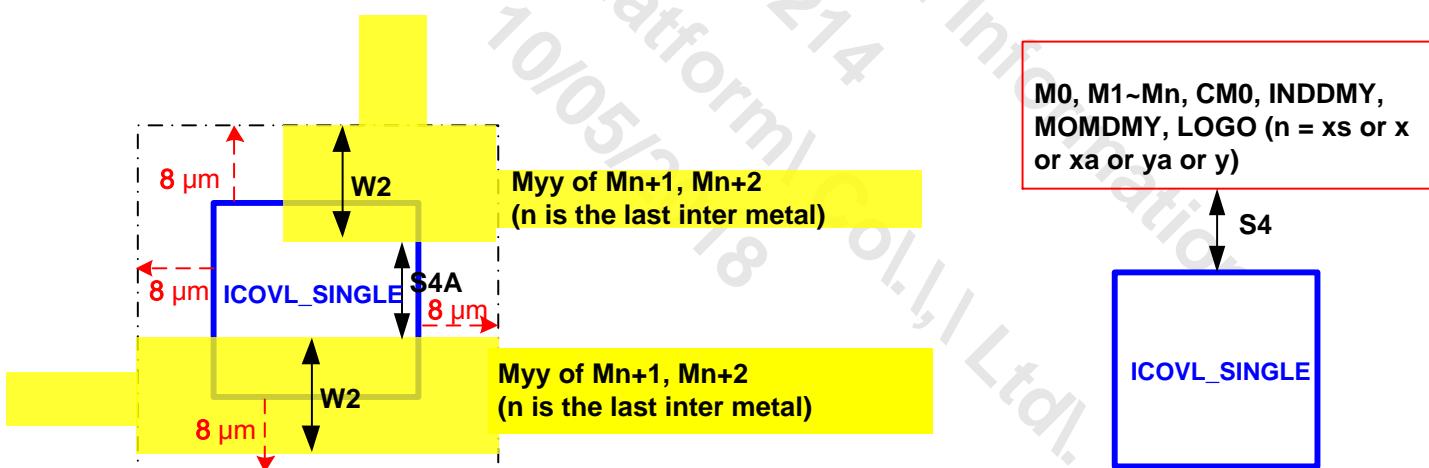
Rule No.	Description	Label	Op.	Rule
ICOVL.R.14.3	Maximum {ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} space of 1X1 die Maximum {ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} space of 1X1 die DRC check: {{Chip_Boundary NOT {ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual}} SIZING down/up 8000 µm (X4)} {{Chip_Boundary NOT {ICOVL_A_Center ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual}} SIZING down/up 8000 µm (X4)}	S1	≤	16000
ICOVL.R.14.4	Maximum {ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} space of 1X2 die or 2X1 die or 2X2 die Maximum {ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} space of 1X2 die or 2X1 die or 2X2 die DRC check: {{Chip_Boundary NOT {ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual}} SIZING down/up 6000 µm (X4)} {{Chip_Boundary NOT {ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual}} SIZING down/up 6000 µm (X4)}	S1	≤	12000
ICOVL.R.14.5	Maximum {ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} space of 1X3 die Maximum {ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} space of 1X3 die DRC check: {{Chip_Boundary NOT {{ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} SIZING 11000 µm in V direction (X7)}} SIZING down/up 5000 µm in H direction (X5)} {{Chip_Boundary NOT {{ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} SIZING 11000 µm in V direction (X7)}} SIZING down/up 5000 µm in H direction (X5)}	S1	≤	10000
ICOVL.R.14.6	Maximum {ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} space of 3X1 die Maximum {ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} space of 3X1 die DRC check: {{Chip_Boundary NOT {{ICOVL_set A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} SIZING 8600 µm in H direction (X8)}} SIZING down/up 6000 µm in V direction (X6)} {{Chip_Boundary NOT {{ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} SIZING 8600 µm in H direction (X8)}} SIZING down/up 6000 µm in V direction (X6)}	S1	≤	12000
ICOVL.R.14.7	Density of {{{ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} SIZING 16500 µm (X2)} SIZING -15500 µm (X3)} for 1X1 die or 3X1 die Density of {{{ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} SIZING 16500 µm (X2)} SIZING -15500 µm (X3)} for 1X1 die or 3X1 die		≥	25%
ICOVL.R.14.8	Density of {{{ICOVL_A_Center OR ICOVL_B_Center OR ICOVL_B1_Center OR ICOVL_D_Center OR ICOVL_D1_Center OR ICOVL_virtual} SIZING 13000 µm (X2)} SIZING -10000 µm (X3)} for 1X2 die or 2X1 die or 2X2 die or 1X3 die Density of {{{ICOVL_A_Center OR ICOVL_C_Center OR ICOVL_E_Center OR ICOVL_virtual} SIZING 13000 µm (X2)} SIZING -10000 µm (X3)} for 1X2 die or 2X1 die or 2X2 die or 1X3 die		≥	25%

Rule No.	Description	Label	Op.	Rule
ICOVL.R.14.9	Density of ICOVL_set inside each Effective_Quadrant_of_Chip for 1x1 die Definition of Effective_Quadrant_of_Chip: Every quadrant of {{(Chip_Boundary with SEALRING_ALL) SIZING -Cx/8 in horizontal direction} SIZING -Cy/8 in vertical direction}		=	100%
ICOVL.R.14.10	tsmc uses 165;80 ~ 165;158, 165;160~165;179, 165;181~165;309, 165;321, 165;500~165;514, 165;870~165;879 layers to do pattern replacement.Your chip is not allowed to have these layers.			
ICOVL.R.49	At least one ICOVL_set must be placed inside Central_Region for 1X1 die in chip level The definition of Central_Region: 1. Find Chip_Center by (Cx/2, Cy/2) 2. Central_Region = {{{Chip_Center SIZING Cx/3 in horizontal direction} SIZING up Cy/6 in vertical direction} OR {{Chip_Center SIZING Cx/6 in horizontal direction} SIZING Cy/3 in vertical direction}}			
ICOVL.R.50	{ICOVL_A OR ICOVL_B OR ICOVL_C OR ICOVL_D OR ICOVL_E OR ICOVL_B1 OR ICOVL_D1} and ICOVL_SINGLE must be drawn identically.			

ICOVL

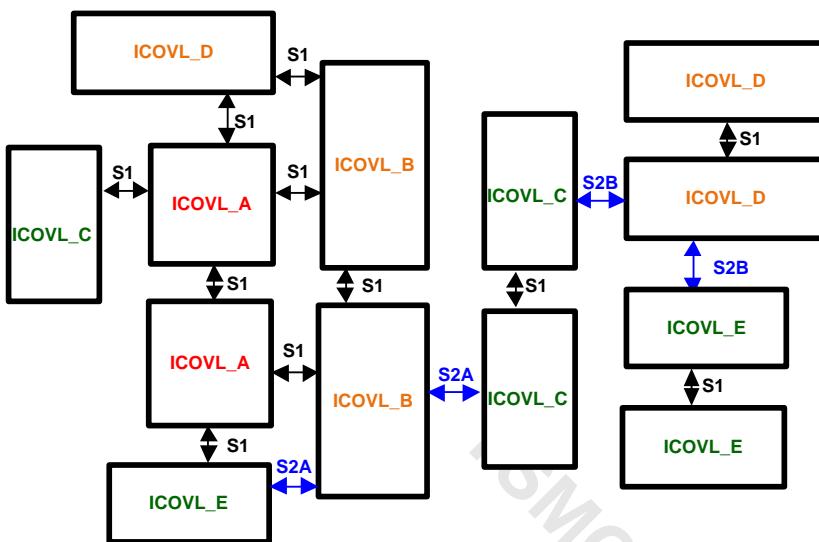


**ICOVL.W.1 / ICOVL.W.1.1 / ICOVL.W.1.1.1 / ICOVL.W.1.2 / ICOVL.W.1.3 /
ICOVL.W.1.3.1 / ICOVL.W.1.4**



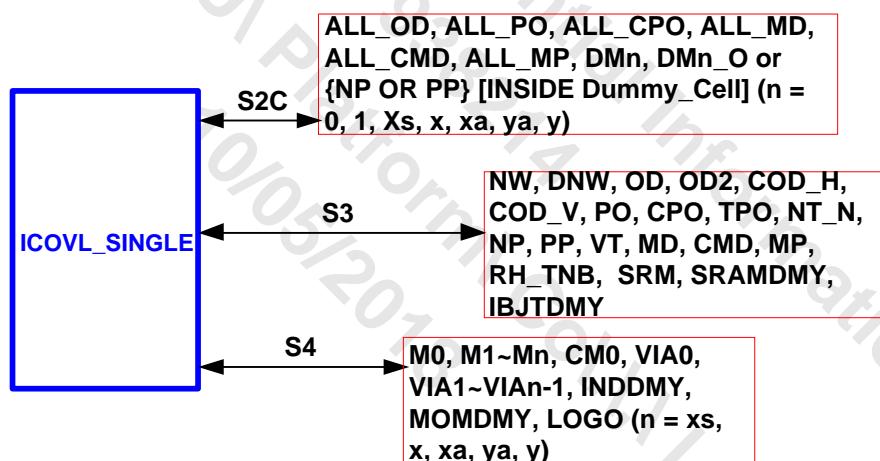
ICOVL.W.2 / ICOVL.S.4.1

ICOVL.S.4



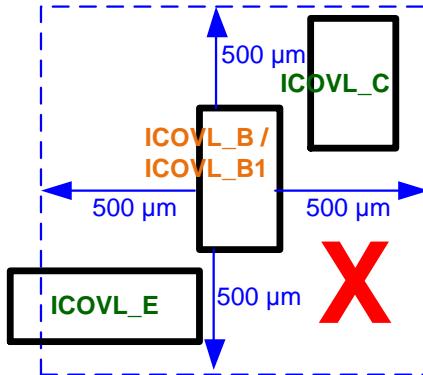
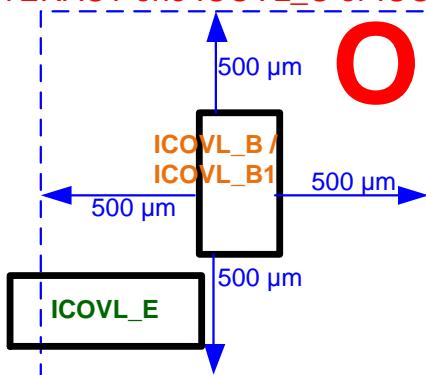
Space	ICOVL_A	{ICOVL_B OR ICOVL_B1}	ICOVL_C	{ICOVL_D OR ICOVL_D1}	ICOVL_E
ICOVL_A	S1	S1	S1	S1	S1
{ICOVL_B OR ICOVL_B1}			S1	S2A	S1
ICOVL_C				S1	S2B
{ICOVL_D OR ICOVL_D1}				S1	S2B
ICOVL_E					S1

ICOVL.S.1 / ICOVL.S.2.1 / ICOVL.S.2.2



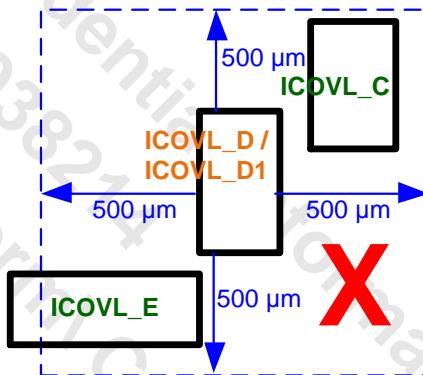
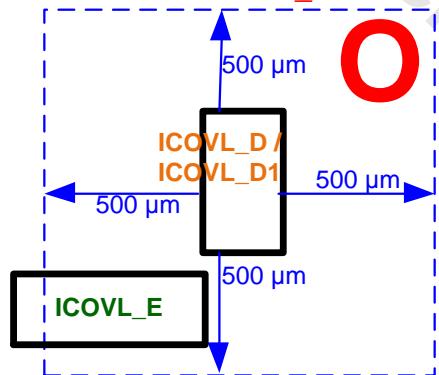
ICOVL.S.2.3 / ICOVL.S.3 / ICOVL.S.4

INTERACT one ICOVL_C or ICOVL_E



ICOVL.R.3.4

INTERACT one ICOVL_C or ICOVL_E



ICOVL.R.3.5

ICOVL_SINGLE

VIAyy



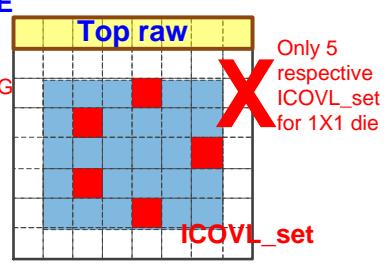
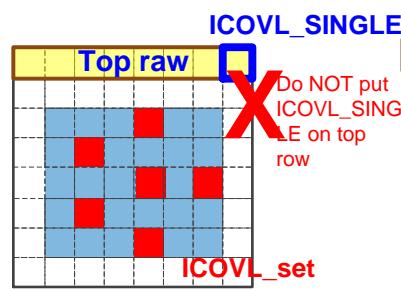
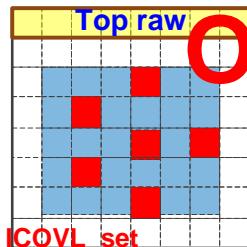
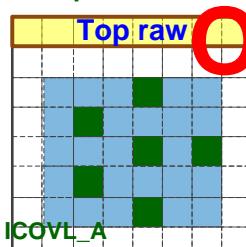
Overlap is not allowed

ICOVL.R.5.1

1X1 Die in a reticle: At least 6 ICOVL_set in 1 Die

- (1) Do NOT put ICOVL_SINGLE on top row
- (2) Put 6 ICOVL_set as uniform as possible

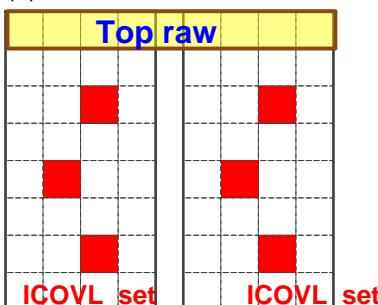
Example



ICOVL.R.7.1^U & ICOVL.R.10

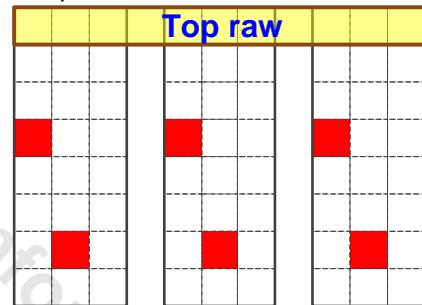
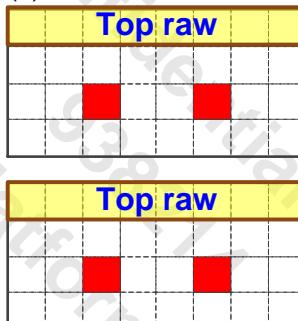
2X1 Die in a reticle: At least 3 ICOVL_set in 1 Die

- (1) Do NOT put ICOVL_SINGLE on top row
- (2) Put 3 ICOVL_set as uniform as possible



1X2 Die & 3X1 Die in a reticle: At least 2 ICOVL_set in 1 Die

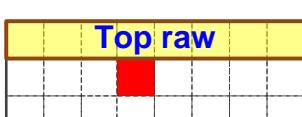
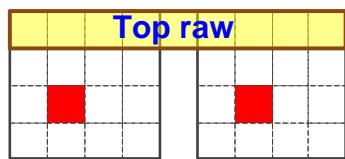
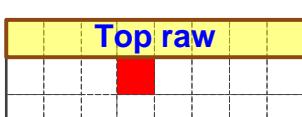
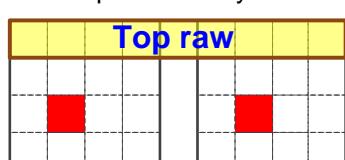
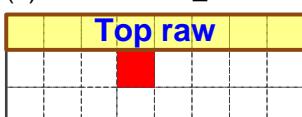
- (1) Don't put ICOVL_SINGLE on top row
- (2) Put 2 ICOVL_set as uniform as possible



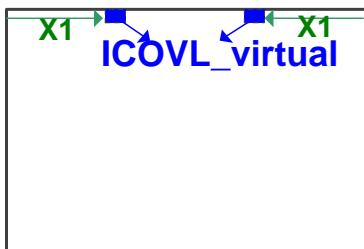
ICOVL.R.7.1^U & ICOVL.R.11

1X3 Die & 2X2 Die in a reticle: At least 1 ICOVL_set in 1 Die

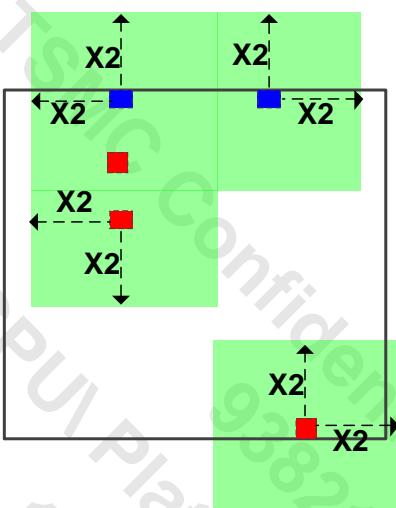
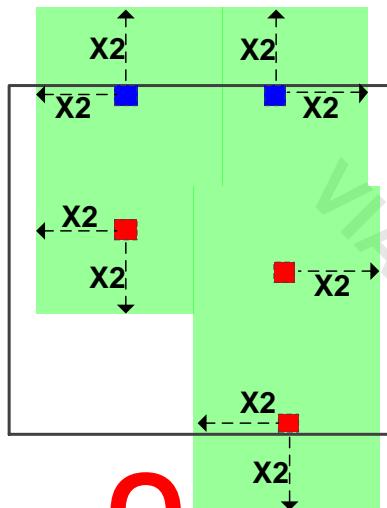
- (1) Don't put ICOVL_SINGLE on top row
- (2) Put 1 ICOVL_set at chip center as you can



ICOVL.R.7.1^U & ICOVL.R.12

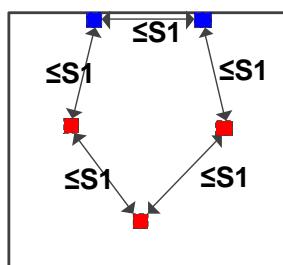


ICOVL.R.14.0

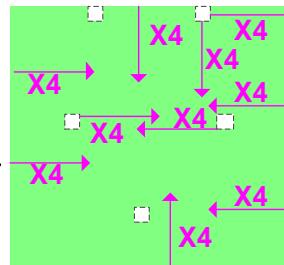


- {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center}
- {{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center}
- ICOVL_virtual
- {{{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual} SIZING (X2)}
- {{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual} SIZING (X2)}

ICOVL.R.14.1/ ICOVL.R.14.2



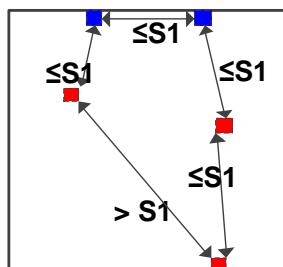
`{(Chip NOT {ICOVL_set OR ICOVL_virtual}) SIZING -(X4)}`



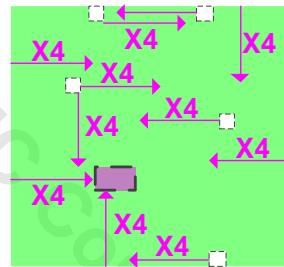
SIZING (X4)

No remaining pattern O

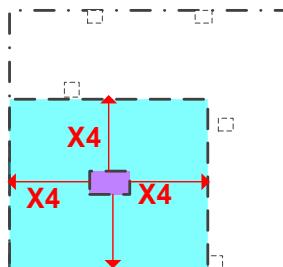
(No remaining pattern)



`{(Chip NOT {ICOVL_set OR ICOVL_virtual}) SIZING -(X4)}`



SIZING (X4)

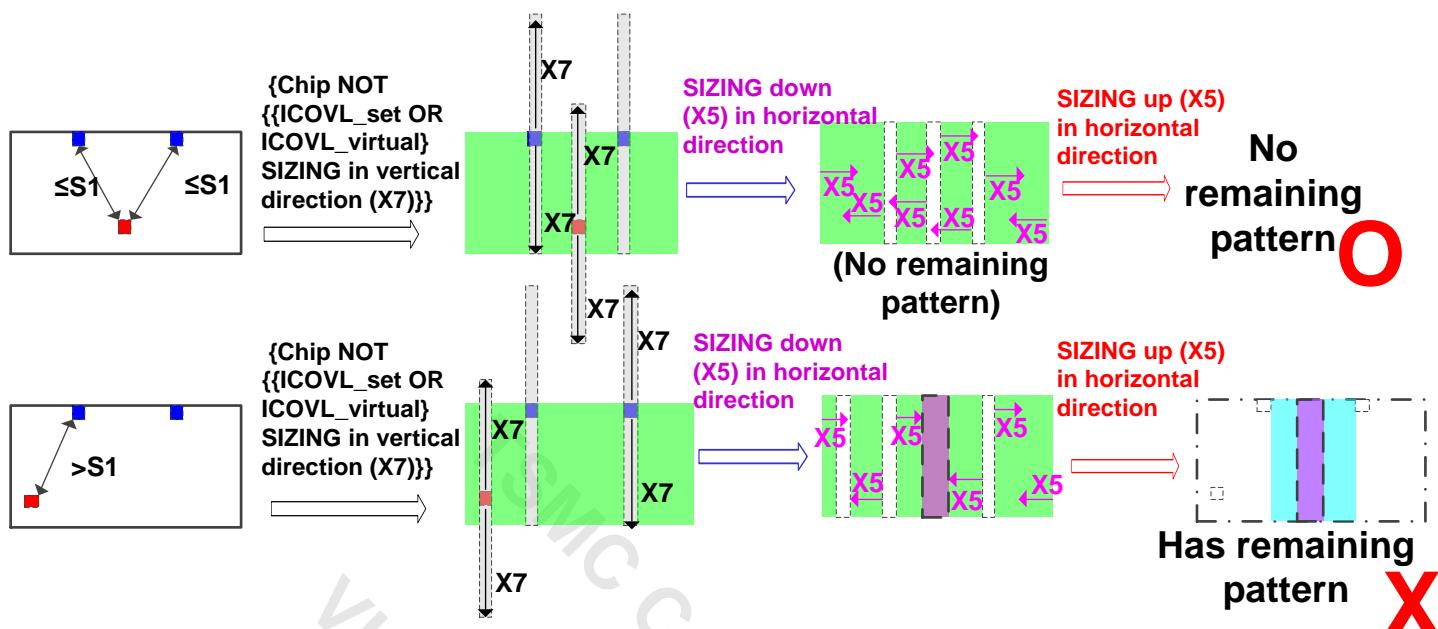


Has remaining pattern

(Has remaining pattern)

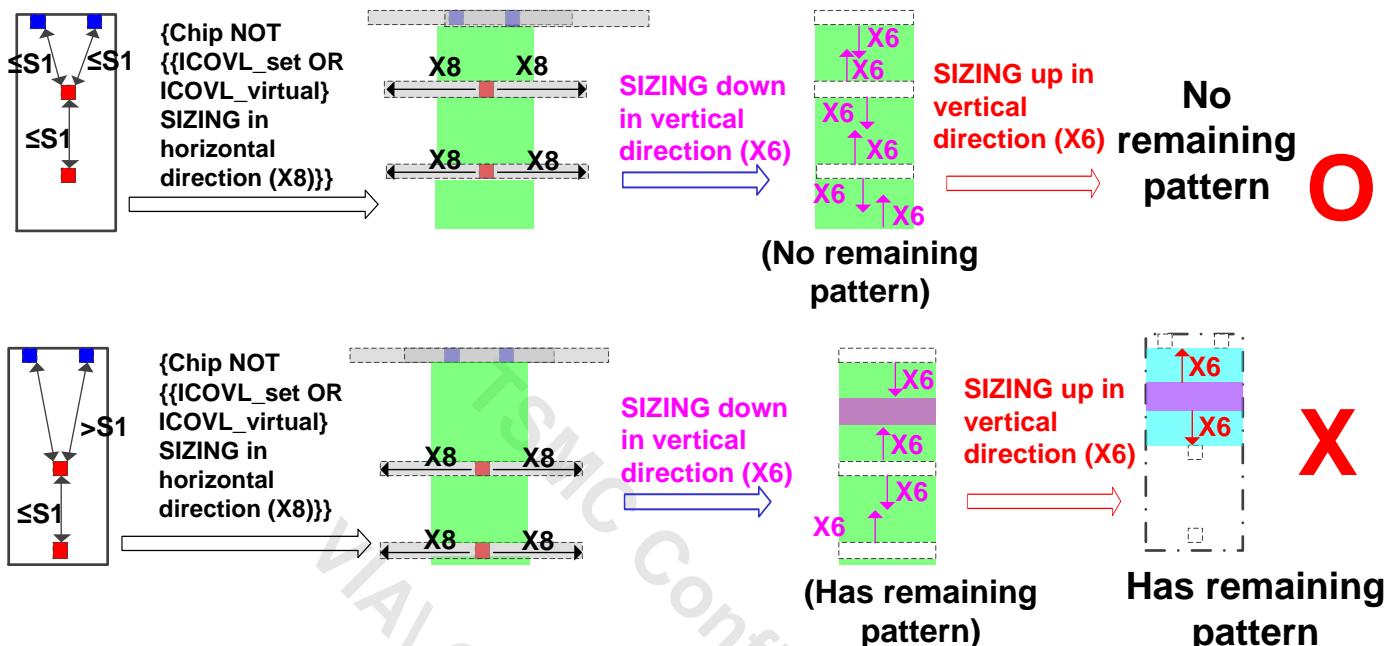
- `{({{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center}`
- `{(ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center}`
- ICOVL_virtual
- `{(Chip NOT {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual})`
- `{(Chip NOT {{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual}) SIZING -(X4)}`
- `{(Chip NOT {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual}) SIZING -(X4) SIZING (X4)`
- `{{{{Chip NOT {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual}} SIZING -(X4)} SIZING (X4)}`

ICOVL.R.14.3 / ICOVL.R.14.4



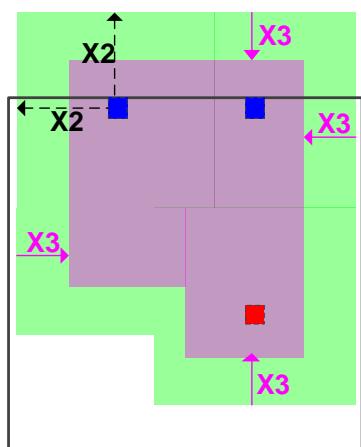
- {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center}
- {{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center}
- ICOVL_virtual
- {Chip NOT {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual} SIZING in vertical direction (X7)}
- {Chip NOT {{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual} SIZING in vertical direction (X7)}}
- {{Chip NOT {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual} SIZING in vertical direction (X7)}} SIZING down (X5) in horizontal direction
- {{Chip NOT {{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual} SIZING in vertical direction (X7)}} SIZING down (X5) in horizontal direction}
- {{{{Chip NOT {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual} SIZING in vertical direction (X7)}} SIZING down (X5) in horizontal direction} SIZING up (X5) in horizontal direction}
- {{{{Chip NOT {{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual} SIZING in vertical direction (X7)}} SIZING down (X5) in horizontal direction} SIZING up (X5) in horizontal direction}}

ICOVL.R.14.5

SIZING down/up 6000 μm in vertical

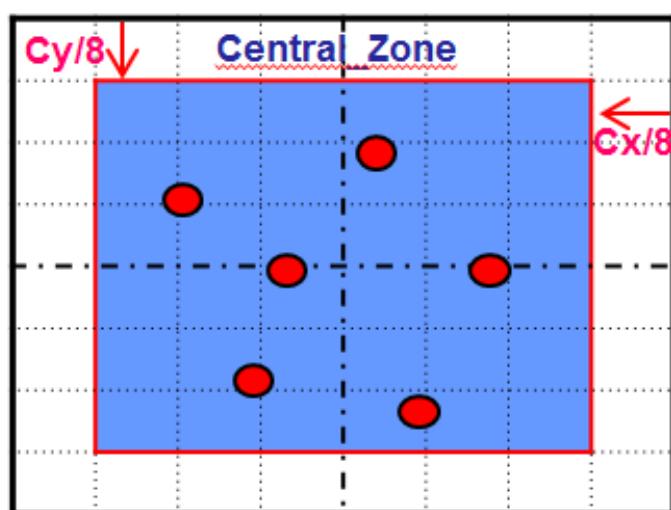
- {{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center}
- {{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center}
- ICOVL_virtual
- {Chip NOT {{{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual}} SIZING in horizontal direction (X8)}
- {Chip NOT {{{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual}} SIZING in horizontal direction (X8)}}
- {Chip NOT {{{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual}} SIZING in horizontal direction (X8)}
- SIZING down in vertical direction (X6)
- {{Chip NOT {{{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual}} SIZING in horizontal direction (X8)}} SIZING down in vertical direction (X6)}
- {{{{Chip NOT {{{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual}} SIZING in horizontal direction (X8)}} SIZING down in vertical direction (X6)} SIZING up in vertical direction (X6)}
- {{{{{{Chip NOT {{{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual}} SIZING in horizontal direction (X8)}} SIZING down in vertical direction (X6)}} SIZING up in vertical direction (X6)}}

ICOVL.R.14.6

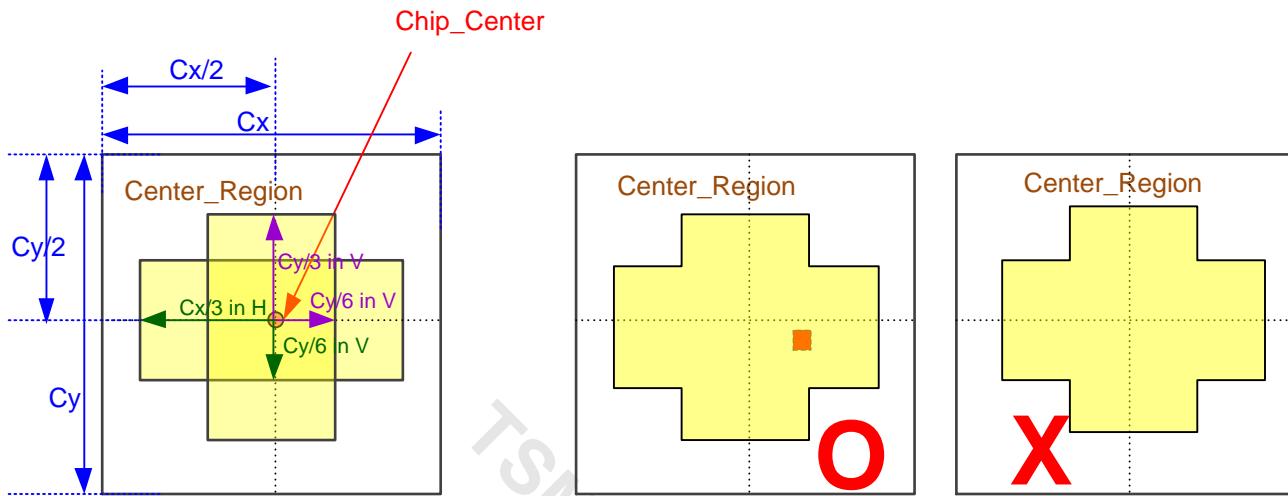


- {{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center}
- {{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center}
- ICOVL_virtual
- {{{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual} SIZING (X2)}
- {{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual} SIZING (X2)}
- {{{{{ICOVL_A_Center OR ICOVL_B_Center} OR ICOVL_B1_Center} OR ICOVL_D_Center} OR ICOVL_D1_Center} OR ICOVL_virtual} SIZING (X2)} SIZING -(X3)}
- {{{{ICOVL_A_Center OR ICOVL_C_Center} OR ICOVL_E_Center} OR ICOVL_virtual} SIZING (X2)} SIZING -(X3)}

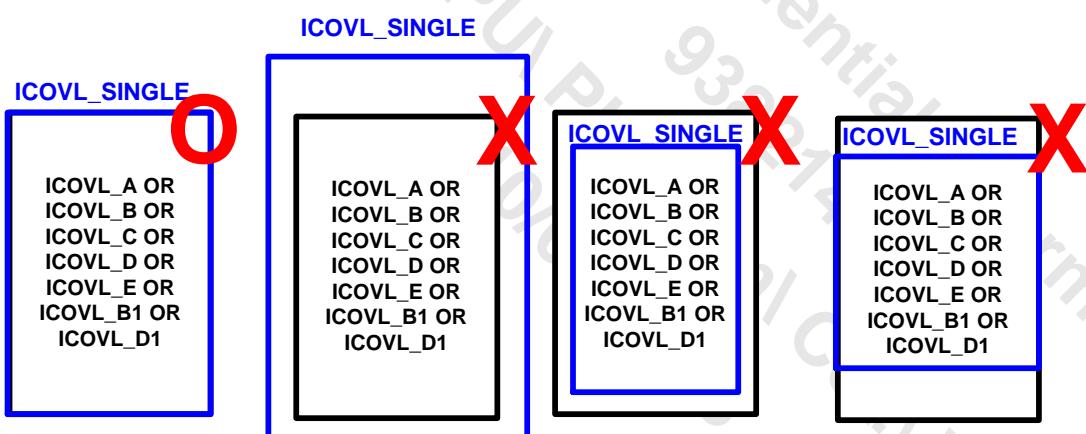
ICOVL.R.14.7/ ICOVL.R.14.8



ICOVL.R.14.9



ICOVL.R.49



{ICOVL_A OR ICOVL_B OR ICOVL_C OR ICOVL_D OR ICOVL_E OR ICOVL_B1 OR ICOVL_D1} and ICOVL_SINGLE must be drawn identically.

ICOVL.R.50

6.6.2 N7+ In-Chip OVL Insertion Methodology

6.6.2.1 Dummy Patterns Priority

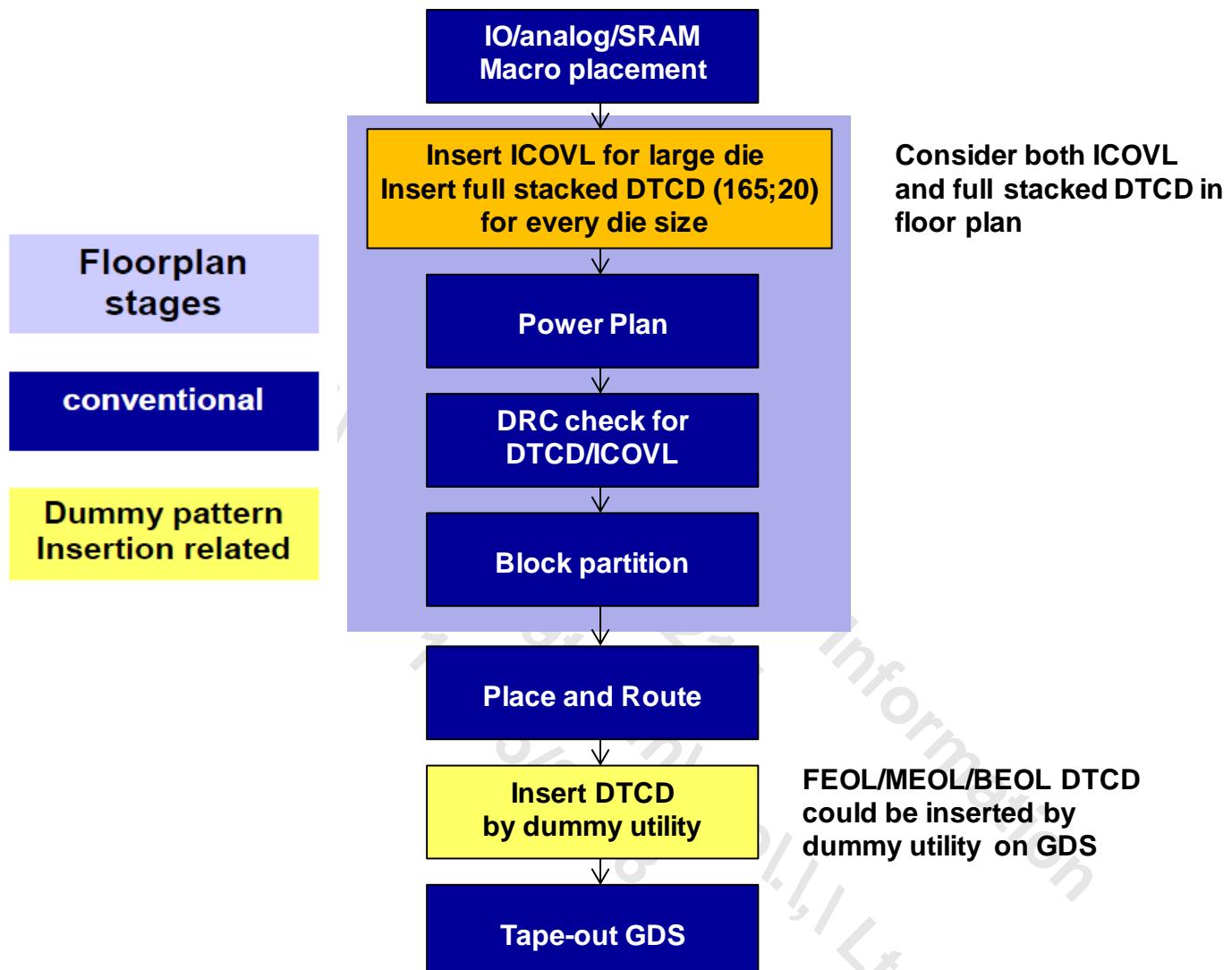
- ICOVL placement priority is higher than TCD dummy
- Need to consider ICOVL insertion in floor plan design level. Insertion in block or IP might not be able to meet uniformity requirement.

6.6.2.2 ICOVL Insertion Guidelines

Die count in a reticle	1X1 reticle	2X1 reticle	1X2 reticle	3X1 reticle	1X3 reticle	2X2 reticle
Window partition	8X8	4X8	8X4	3X8	8X3	4X4
Number of ICOVL required	6	3	2	2	1	1

- Select windows for ICOVL to achieve maximum ICOVL placement evenness. Please refer to sec.6.5.1 about the definition of 1X1, 1X2, 2X1, 1X3, 3X1 and 2X2 die count in a reticle.
- In each window partition, choose either a set of single ICOVL.
 - ◆ For 1X1 Die, please refer to ICOVL.R.7.1^U, ICOVL.R.10, ICOVL.R.14.1, ICOVL.R.14.3, ICOVL.R.14.7 and ICOVL.R.49 for details.
 - ◆ For 1X2 Die, please refer to ICOVL.R.7.1^U, ICOVL.R.12, ICOVL.R.14.1, ICOVL.R.14.4 and ICOVL.R.14.8 for details.
 - ◆ For 1X3 Die, please refer to ICOVL.R.7.1^U, ICOVL.R.13, ICOVL.R.14.1, ICOVL.R.14.5 and ICOVL.R.14.8 for details.
 - ◆ For 2X1 Die, please refer to ICOVL.R.7.1^U, ICOVL.R.11, ICOVL.R.14.2, ICOVL.R.14.4 and ICOVL.R.14.8 for details
 - ◆ For 3X1 Die, please refer to ICOVL.R.7.1^U, ICOVL.R.12, ICOVL.R.14.2, ICOVL.R.14.6 and ICOVL.R.14.7 for details
 - ◆ For 2X2 Die, please refer to ICOVL.R.7.1^U, ICOVL.R.13, ICOVL.R.14.1 and ICOVL.R.14.8 for details
- ICOVL mirror image placement in X,Y is legal.

6.6.2.3 Dummy Pattern Insertion in Design Phase



6.7 IP Density Guidelines

6.6.1 IP_TIGHTEN_DENSITY Switch

6.6.2 IP_TIGHTEN_BOUNDARY Switch

An IP which passes local density rules may become failure after chip integration because:

1. Initial point is changed and then checking window shift.
2. The density environment around this IP may change the final density of the windows across IP boundary.

There are two options to improve design layout with more density margin to reduce high/low density violation possibility while IP repeats (up/down, left/right) or IP abutting with others:

- Option-1: It is recommended to follow the density DFM Recommendations at IP level.
- Option-2: turns on the "IP_TIGHTEN_DENSITY" switch in the DRC deck for tighter density and empty space requirement at IP level. (refer sec.6.6.1 IP_TIGHTEN_DENSITY)

OD/Metal Gate/ High R resistors, Diodes, BJT, varactor are the most critical. If you use dummy block to avoid dummy insertion after IP design, please make sure to insert dummy patterns in the IP completely, either by utility or manual. Do not leave empty space arbitrarily.

For chip level, please insert dummy comprehensively by utility.

6.7.1 IP_TIGHTEN_DENSITY Switch

There are two options to evaluate the possible local density violation early in IP/macro/block level validation stage by turning on "IP_TIGHTEN_DENSITY" switch, please select the either one and follow the procedures:

- **Option1:** check the possible local density violation by IP_TIGHTEN_DENSITY default settings.
1. Turn off "FULL_CHIP" option and turn on "IP_TIGHTEN_DENSITY" option in the DRC deck.
 - If you turn on "FULL_CHIP" option, "IP_TIGHTEN_DENSITY" option will be turned off automatically even you turn on this option.
 2. Follow IP_TIGHTEN_DENSITY default settings:
 1. Using fine window step: there are three checking window sets (window size/50, window size/50, and window size/50 by default), named DENSITY_STEP_RATIOa, DENSITY_STEP_RATIOb, and DENSITY_STEP_RATIOc.
 2. Increase / Decrease density value of low / high density check by (1%, 1% x density spec^0.5, and 1%) set, named DENSITY_DELTAa, DENSITY_DELTab and DENSITY_DELTAc.
 - DENSITY_DELTAa & DENSITY_STEP_RATIOa affect rules and recommendations:
OD.DN.3.1, OD.DN.4, OD.DN.10, PO.DN.3.1, PO.DN.3.2, PO.DN.3.4, PO.DN.3.6, PO.DN.6, PO.DN.7, CPO.DN.1.1, SSD.DN.5, SSD.DN.6, MD.DN.2, MP.DN.2, MP.DN.2.1, MP.DN.2.2, M0.DN.2.3, CMD.DN.1, CELL.CMD.DN.1, CMD.DN.1.1, RH_TN.DN.4, M0.DN.2, M0.DN.9, M0.DN.9.1, M1.DN.2, M1.DN.2.3, M1.DN.9, M1.DN.9.1, M1.DN.10.1, Mx.DN.2, Mx.DN.2.3, Mx.DN.9, Mx.DN.9.1, Mxa.DN.2, Mxa.DN.2.3, Mxa.DN.9, Mxa.DN.9.1, Mya.DN.2, Mya.DN.2.3, My.DN.2, My.DN.2.3, Myy.DN.2.4, Myy.DN.5®, Myx.DN.2.4, Myx.DN.5®, Myz.DN.2.4, Mz.DN.2.1, and Mr.DN.2.1
 - DENSITY_DELTab & DENSITY_STEP_RATIOb affect rules and recommendations:
PO.DN.2, PO.DN.2.1, MD.DN.1, MD.DN.1.1, MP.DN.1, MP.DN.1.1, MP.DN.1.2, VC.DN.2, M0.DN.1.1, M0.DN.1.2, M0.DN.3.7, M0.DN.3.8, M1.DN.1.1, M1.DN.1.2, Mx.DN.1.1, Mx.DN.1.2, Mx.DN.3.7, Mx.DN.3.8, Mxa.DN.1.1, Mxa.DN.1.2, Mxa.DN.3.7, Mxa.DN.3.8, Mya.DN.1.1, Mya.DN.1.2, My.DN.1.1, My.DN.1.2, My.DN.7, My.DN.1.3, Myy.DN.6, Myy.DN.7, Myx.DN.1.3, Myz.DN.1.3, Mz.DN.1.3, and Mr.DN.1.3.

```
#IFDEF IP_TIGHTEN_DENSITY
VARIABLE DENSITY_STEP_RATIOa    1/50   : Turn on IP_TIGHTEN_DENSITY switch
VARIABLE DENSITY_DELTAa        1/100  : Turn on IP_TIGHTEN_DENSITY switch
VARIABLE DENSITY_STEP_RATIOb    1/50   : Turn on IP_TIGHTEN_DENSITY switch
VARIABLE DENSITY_DELTab       1/100  : Turn on IP_TIGHTEN_DENSITY switch
#ELSE
VARIABLE DENSITY_STEP_RATIOa    1/2    : Turn off IP_TIGHTEN_DENSITY switch
VARIABLE DENSITY_DELTAa        0      : Turn off IP_TIGHTEN_DENSITY switch
VARIABLE DENSITY_STEP_RATIOb    1/2    : Turn off IP_TIGHTEN_DENSITY switch
VARIABLE DENSITY_DELTab       0      : Turn off IP_TIGHTEN_DENSITY switch
#endif
```

Figure 6.6.1.1 "IP_TIGHTEN_DENSITY" variable sets of DRC deck

Here are some examples for density check:

- Example-1: OD.DN.3.1 (OD density $\geq 14\%$ [window 18 μm x 18 μm , stepping 9 μm]), DRC flags 18 μm x18 μm checking window OD density < 15% by stepping 0.36 μm if you TURN ON “IP_TIGHTEN_DENSITY” option. (refer following calculations)

Example-1: OD.DN.3.1

Rule No. ^a	Description ^a	Label ^a	Op. ^a	Rule ^a
OD.DN.3.1 ^a	Minimum ALL_OD density in window 18 μm x 18 μm , stepping 9 μm . (Except TCDDMY, ICOVL_SINGLE, BLK_WF, NWDMY, SEALRING_ALL) ^a	^a	\geq ^a	14% ^a

Turn off IP_TIGHTEN_DENSITY

checking window: 18x18

Stepping: 9

Rule spec: 14%

Turn ON IP_TIGHTEN_DENSITY

checking window: 18x18

Stepping: $0.36 = 18 \times \text{DENSITY_STEP_RATIOa} = 18 \times 1/50$

Rule spec: $15\% = 0.14 + \text{DENSITY_DELTAA} = 0.14 + 1/100$

Figure 6.6.1.2 OD.DN.3.1 example for "IP_TIGHTEN_DENSITY" check

- Example-2: PO.DN.2 (PO density $\geq 10\%$ [window 10 μm x 10 μm , stepping 5 μm]), DRC flags 10 μm x10 μm checking window PO density < 10.316 % by stepping 0.2 μm if you TURN ON “IP_TIGHTEN_DENSITY” option. (refer following calculations)

Example-2: PO.DN.2

Rule NO.	Description	Label	Rule
PO.DN.2	Minimum {ALL_PO NOT CPO} density in window 10 μm x 10 μm , stepping 5 μm Except the following regions: (1) {{CSR AND SEALRING_ALL} SIZING 1 μm } (2) TCDDMY (3) ICOVL_single (4) SEALRING_ALL (5) RH_TNB (This rule only apply while the area of {checking window NOT exclusive region} $\geq 1/2$ window area)	\geq	10%

Turn off IP_TIGHTEN_DENSITY

Checking window: 10 x 10

Stepping: 5

Rule spec: 10 %

Turn on IP_TIGHTEN_DENSITY

Checking window: 10 x 10

Stepping: $0.2 = 10 \times \text{DENSITY_STEP_RATIOb} = 10 \times 1/50$

Rule spec: $10.316\% = 0.1 + \text{DENSITY_DELTAb} \times (0.1^{0.5}) = 0.1 + 1/100 \times 0.31622..$

Figure 6.6.1.3 PO.DN.2 example for "IP_TIGHTEN_DENSITY" check

- **Option2:** check the possible local density violation by modifying the density rule variables in DRC deck if you think the default settings are too tight. (refers Figure 6.6.1.4)

1. Turn off "FULL_CHIP" option and turn on "IP_TIGHTEN_DENSITY" option in the DRC deck.
 - If you turn on "FULL_CHIP" option, "IP_TIGHTEN_DENSITY" option will be turned off automatically even you turn on this option.
2. According to your demand to change the variable sets in the deck.

```
#IFDEF IP_TIGHTEN_DENSITY
VARIABLE DENSITY_STEP_RATIOa
VARIABLE DENSITY_DELTAa
VARIABLE DENSITY_STEP_RATIOb
VARIABLE DENSITY_DELTab
#else
VARIABLE DENSITY_STEP_RATIOa      1/2
VARIABLE DENSITY_DELTAa          0
VARIABLE DENSITY_STEP_RATIOb    1/2
VARIABLE DENSITY_DELTab         0
#endif
```

Default set

1/50
1/100
1/50
1/100

You can modify the variables in DRC deck

Figure 6.6.1.4 Modify example of "IP_TIGHTEN_DENSITY" variable sets

6.7.1.1 DRC methodology for boundary of IP

To avoid minimum Line edge Density (LeD) violations after IP abutment, the below items (named with **IP_TIGHTEN_LED) will be executed simultaneously on the boundary region of IP when turning on the switch of "IP_TIGHTEN_DENSITY". Similar DRC setting method as section 6.6.1.1, please select the either one and follow the procedures:

- **Option1:** check the possible local density violation by default settings.
1. Turn off "FULL_CHIP" option and turn on "IP_TIGHTEN_DENSITY" option in the DRC deck.
 - If you turn on "FULL_CHIP" option, "IP_TIGHTEN_DENSITY" option will be turned off automatically even you turn on this option.
 2. Follow IP_TIGHTEN_DENSITY default settings:
 1. Only {prBoundary NOT {prBoundary size -20µm}} region will be checked.
 2. Density checking window is 10 µm x 10 µm, stepping 5 µm.
 3. Increase density value of spec by LeD_DELTA (default is 0).
 - The related rules are listed as below,

Rule No.	Description	Label	Op.	Rule
M0.DN.9.IP_TIGHTEN_LED	<p>Minimum Line edge Density (LeD) $\geq 8.5 + \text{LeD_DELTA}$ [inside region of {prBoundary NOT {prBoundary SIZING -10 µm}}, by window 10 µm x 10 µm, stepping 5 µm]</p> <p>Definition of "Line edge Density": $((\text{All_metal area}) - (\text{All_metal SIZING } -0.001 \mu\text{m area})) \times 1000 / \text{Checking window}$</p> <p>(Except TCDDMY_M0, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window inside region of {prBoundary NOT {prBoundary SIZING -10 µm}}, and LeD $< 8.5 + \text{LeD_DELTA}$</p>			
M1.DN.9.IP_TIGHTEN_LED	<p>Minimum Line edge Density (LeD) $\geq 8.5 + \text{LeD_DELTA}$ [inside region of {prBoundary NOT {prBoundary SIZING -10 µm}}, by window 10 µm x 10 µm, stepping 5 µm]</p> <p>Definition of "Line edge Density": $((\text{All_metal area}) - (\text{All_metal SIZING } -0.001 \mu\text{m area})) \times 1000 / \text{Checking window}$</p> <p>(Except TCDDMY_M1, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window inside region of {prBoundary NOT {prBoundary SIZING -10 µm}}, and LeD $< 8.5 + \text{LeD_DELTA}$</p>			
Mxs.DN.9.IP_TIGHTEN_LED	<p>Minimum Line edge Density (LeD) $\geq 8.5 + \text{LeD_DELTA}$ [inside region of {prBoundary NOT {prBoundary SIZING -10 µm}}, by window 10 µm x 10 µm, stepping 5 µm]</p> <p>Definition of "Line edge Density": $((\text{All_metal area}) - (\text{All_metal SIZING } -0.001 \mu\text{m area})) \times 1000 / \text{Checking window}$</p> <p>(Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window inside region of {prBoundary NOT {prBoundary SIZING -10 µm}}, and LeD $< 8.5 + \text{LeD_DELTA}$</p>			

Mx.DN.9.IP_TIG HTEN_LED	<p>Minimum Line edge Density (LeD) $\geq 8.5 + \text{LeD_DELTA}$ [inside region of {prBoundary NOT {prBoundary SIZING -10 μm}}, by window 10 $\mu\text{m} \times 10 \mu\text{m}$, stepping 5 μm]</p> <p>Definition of "Line edge Density": $((\text{All_metal area}) - (\text{All_metal SIZING } -0.001 \mu\text{m area})) \times 1000) / \text{Checking window}$</p> <p>(Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window inside region of {prBoundary NOT {prBoundary SIZING -10 μm}}, and LeD $< 8.5 + \text{LeD_DELTA}$</p>		
Mxa.DN.9.IP_TI GHTEN_LED	<p>Minimum Line edge Density (LeD) $\geq 8.5 + \text{LeD_DELTA}$ [inside region of {prBoundary NOT {prBoundary SIZING -10 μm}}, by window 10 $\mu\text{m} \times 10 \mu\text{m}$, stepping 5 μm]</p> <p>Definition of "Line edge Density": $((\text{All_metal area}) - (\text{All_metal SIZING } -0.001 \mu\text{m area})) \times 1000) / \text{Checking window}$</p> <p>(Except TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)</p> <p>DRC flags only if the checking window inside region of {prBoundary NOT {prBoundary SIZING -10 μm}}, and LeD $< 8.5 + \text{LeD_DELTA}$</p>		

- **Option2:** check the possible local density violation by modifying the density rule variables in DRC deck if you think the default settings are too tight. (refers Figure 6.7.1.2.1)
 1. Turn off “FULL_CHIP” option and turn on “IP_TIGHTEN_DENSITY” option in the DRC deck.
 - If you turn on “FULL_CHIP” option, “IP_TIGHTEN_DENSITY” option will be turned off automatically even you turn on this option.
 2. According to your demand to change the variable sets in the deck.

```
#DEFINE IP_TIGHTEN_DENSITY
VARIABLE LeD_DELTA 0
Default set
```

You can modify the
variables in DRC deck

Figure 6.7.1.2.1 Modify example of “LeD_DELTA” setting

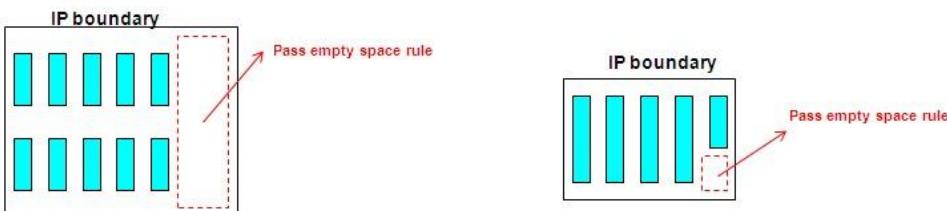
6.7.2 IP_TIGHTEN_BOUNDARY Switch

To evaluate the possible empty space violation early in IP/macro/block level validation stage, you can turn on “IP_TIGHTEN_BOUNDARY” switch to trigger following sanity check.

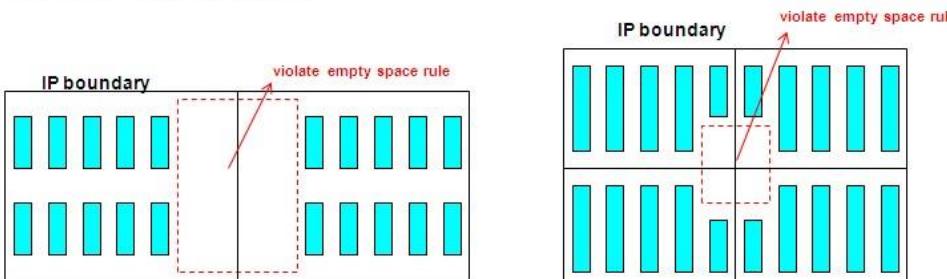
Rule No.	Description	Label	Op.	Rule
OD.S.11.IP_TIGHTEN_BOUNDARY	To avoid $> 5 \mu\text{m} \times 5 \mu\text{m}$ OD empty space after IP abutment OD empty space must $\leq 2.5 \mu\text{m} \times 5 \mu\text{m}$ on IP boundary edge OD empty space must $\leq 2.5 \mu\text{m} \times 2.5 \mu\text{m}$ on IP boundary corner			
OD.S.11.1.IP_TIGHTEN_BOUNDARY	To avoid $> 1.2 \mu\text{m} \times 1.2 \mu\text{m}$ OD empty space after IP abutment OD empty space must $\leq 0.6 \mu\text{m} \times 1.2 \mu\text{m}$ on IP boundary edge OD empty space must $\leq 0.6 \mu\text{m} \times 0.6 \mu\text{m}$ on IP boundary corner			
OD.A.7.IP_TIGHTEN_BOUNDARY	To avoid $> 0.9 \mu\text{m} \times 5 \mu\text{m}$ OD empty area after IP abutment OD empty area must $\leq 0.45 \mu\text{m} \times 5 \mu\text{m}$ on IP boundary edge OD empty area must $\leq 0.45 \mu\text{m} \times 2.5 \mu\text{m}$ on IP boundary corner			
PO.S.25.IP_TIGHTEN_BOUNDARY	To avoid $> 1 \mu\text{m} \times 1 \mu\text{m}$ PO empty space after IP abutment PO empty space must $\leq 0.5 \mu\text{m} \times 1 \mu\text{m}$ on IP boundary edge PO empty space must $\leq 0.5 \mu\text{m} \times 0.5 \mu\text{m}$ on IP boundary corner			
PO.A.4.IP_TIGHTEN_BOUNDARY	To avoid $> 1.2 \mu\text{m} \times 16 \mu\text{m}$ PO empty space after IP abutment PO empty space must $\leq 0.6 \mu\text{m} \times 16 \mu\text{m}$ on IP boundary edge PO empty space must $\leq 0.6 \mu\text{m} \times 8 \mu\text{m}$ on IP boundary corner			
PO.A.4.1.IP_TIGHTEN_BOUNDARY	To avoid $> 0.8 \mu\text{m} \times 5 \mu\text{m}$ PO empty area after IP abutment PO empty area must $\leq 0.4 \mu\text{m} \times 5 \mu\text{m}$ on IP boundary edge PO empty area must $\leq 0.4 \mu\text{m} \times 2.5 \mu\text{m}$ on IP boundary corner			
PO.A.4.2.IP_TIGHTEN_BOUNDARY	To avoid $> 0.570 \mu\text{m} \times 7 \mu\text{m}$ PO empty area after IP abutment PO empty area must $\leq 0.285 \mu\text{m} \times 7 \mu\text{m}$ on IP boundary edge PO empty area must $\leq 0.285 \mu\text{m} \times 3.5 \mu\text{m}$ on IP boundary corner			
M0.R.14.IP_TIGHTEN_BOUNDARY	To avoid $> 0.760 \mu\text{m} \times 0.760 \mu\text{m}$ metal empty space after IP abutment Metal empty space must $\leq 0.380 \mu\text{m} \times 0.760 \mu\text{m}$ on IP boundary edge Metal empty space must $\leq 0.380 \mu\text{m} \times 0.380 \mu\text{m}$ on IP boundary corner			
M1.R.14.IP_TIGHTEN_BOUNDARY	To avoid $> 0.760 \mu\text{m} \times 0.760 \mu\text{m}$ metal empty space after IP abutment Metal empty space must $\leq 0.380 \mu\text{m} \times 0.760 \mu\text{m}$ on IP boundary edge Metal empty space must $\leq 0.380 \mu\text{m} \times 0.380 \mu\text{m}$ on IP boundary corner			

Rule No.	Description	Label	Op.	Rule
Mxs.R.14.IP_TIGHTEN_BOUNDARY	To avoid $> 0.760 \mu\text{m} \times 0.760 \mu\text{m}$ metal empty space after IP abutment Metal empty space must $\leq 0.380 \mu\text{m} \times 0.760 \mu\text{m}$ on IP boundary edge Metal empty space must $\leq 0.380 \mu\text{m} \times 0.380 \mu\text{m}$ on IP boundary corner			
Mx.R.14.IP_TIGHTEN_BOUNDARY	To avoid $> 0.760 \mu\text{m} \times 0.760 \mu\text{m}$ metal empty space after IP abutment Metal empty space must $\leq 0.380 \mu\text{m} \times 0.760 \mu\text{m}$ on IP boundary edge Metal empty space must $\leq 0.380 \mu\text{m} \times 0.380 \mu\text{m}$ on IP boundary corner			
Mxa.R.14.IP_TIGHTEN_BOUNDARY	To avoid $> 0.760 \mu\text{m} \times 0.760 \mu\text{m}$ metal empty space after IP abutment Metal empty space must $\leq 0.380 \mu\text{m} \times 0.760 \mu\text{m}$ on IP boundary edge Metal empty space must $\leq 0.380 \mu\text{m} \times 0.380 \mu\text{m}$ on IP boundary corner			
DMn.S.7.IP_TIGHTEN_BOUNDARY	To avoid $> 1.0 \mu\text{m} \times 1.0 \mu\text{m}$ Metal empty space after IP abutment Metal empty space must $\leq 0.5 \mu\text{m} \times 1.0 \mu\text{m}$ on IP boundary edge Metal empty space must $\leq 0.5 \mu\text{m} \times 0.5 \mu\text{m}$ on IP boundary corner (This check is only applied to M0/M1/Mxs/Mx/Mxa/My)			

Single IP



After IP abutment



If the IP meets all following conditions, suggest to turn on this switch

1. The IP is already filled by dummy utility
2. The IP will use FEOLBLK/ BEOLBLK/DMnExCL layer to cover entire area to avoid dummy insertion in Top level.
3. The IP will abut by itself or other IP in Top level

7 Design For Manufacturing (DFM)

This chapter provides information about the following topics:

- 7.1 Layout Guidelines for Yield Enhancement
 - 7.2 DFM Recommendations and Guidelines Summary
 - 7.3 Guidelines for Mask Making Efficiency
 - 7.4 Die Size Optimization Kit (GDA and MFU)

7.1 Layout Guidelines for Yield Enhancement

This section provides guidelines for layout optimization to minimize certain potential and unnecessary yield or timing loss under the condition without area penalty. For a given chip design, first and foremost, efforts should be made to achieve as small a die size as possible. The guidelines should not be used indiscriminately, which could result in unnecessarily large chip sizes.

This section is divided into the following topics:

- Guidelines for optimal electrical model and silicon correlation
 - Layout tips for minimizing critical areas

7.1.1 Guidelines for Optimal Electrical Model and Silicon Correlation

The following sections offer recommended practices to minimize the deviation of processed hardware from electrical models.

7.1.1.1 Transistors

- Avoid layout styles that may contribute to silicon-to-model deviation.
 - Use uniform OD, PO/CPO, and MEOL density across a design.
 - The OD and PO density in the neighboring area could affect the gate critical dimension and also the device performance. Please avoid putting sensitive circuit near the region with high OD/PO density gradient.
 - Avoid placing the devices in a big empty space of OD and PO environment, specially the small OD devices. It's better to surround the devices with OD and PO both.
 - Avoid abutting your sensitive IP to the regions of high or low OD/PO density circuits, like the array of PO resistor, varactor, capacitor, large BJT, large diode, SRAM, MOM and wide OD.
 - It is important not to have large DECAP surrounding the sensitive IP and not to insert too many DECAP in the std cell array
 - Remove some DECAP as the IP violates the PO density
 - Only insert DECAP on the IP sensitive area. Use other filler cells if possible.
 - Avoid to place the IP close to I/O and chip corner if possible
 - Pay attention to the leakage current for narrow-width devices with a low-Vt option. Please consult the SPICE model for detailed information.
 - Device behavior is influenced by layout style possibly due to stress distribution induced by STI/OD edge. Designer should take the length of OD (LOD) effect into consideration during device or cell level design.
 - For PMOS device, if the NWELL is tied to the source used as an internal AC node, the NWELL total area junction capacitance should be included in the circuit simulation by adding the Well capacitance at the bulk node.

- Take NWELL sheet resistance into consideration during simulation, to reflect the transient bias variation by adding the Well resistance between source node and substrate node.
- For stacked device, multiple transistors are adjusted to fit into the same OD with performance trade-off. Refer to Figure 7.1.1.

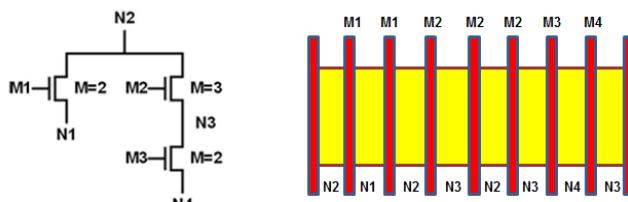


Figure 7.1.1 Stacked device

7.1.1.1 Improvement CD uniformity

- Further recommendation for improvement of CD uniformity (3-sigma):
 - Besides follow the rules, it's better to have extra dummy PO with the same width and space around the device gate, even this gate does not need to follow the 1st/2nd PO rules.
 - It is requested to have OD and PO patterns uniformly across the whole filler cell, as Figure 7.1.2. Maximize the length of the OD and PO as much as you can (to match the cell height).
 - Dummy fillers of floating and fixed voltage are both acceptable from process point of view. However, the associated implant layers are must if the filler cell is connected to a fixed voltage.

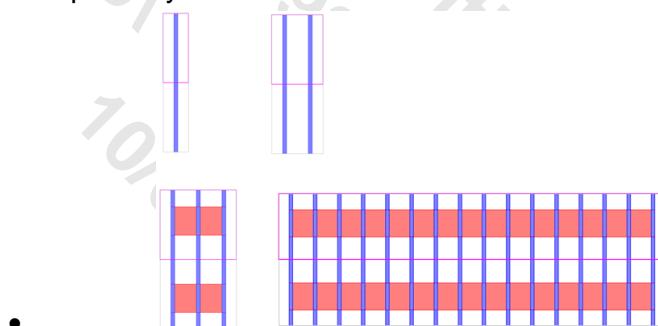


Figure 7.1.2 Example of filler cell

- Add dummy OD and PO either by utility or manual drawn inside the whole IP to fill the remaining sparse area. Treat this dummy insertion as default step of IP design and being verified together with library characterization process.
 - It is also recommended to put filler cell at the edges of standard cell arrays during P&R.
- Guidelines for P&R during filler cell insertion: Use different types of filler cells at P&R to optimize the FEOL and MEOL environment, see Figure 7.1.3 and Figure 7.1.4.
 - (1) Boundary filler cells: Before standard cell placement, inserting these fillers on block boundary and macro boundary for occupying the placement locations.
 - (2) Internal filler cells: After standard cell placement, using original filler insertion command.
- During chip integration, please insert the dummy PO/OD by utility again to eliminate the white empty space due to the placement blockage layer which added for avoiding std_cells abutment with this IP.

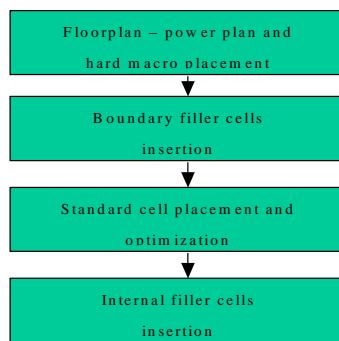


Figure 7.1.3 Example of filler cell

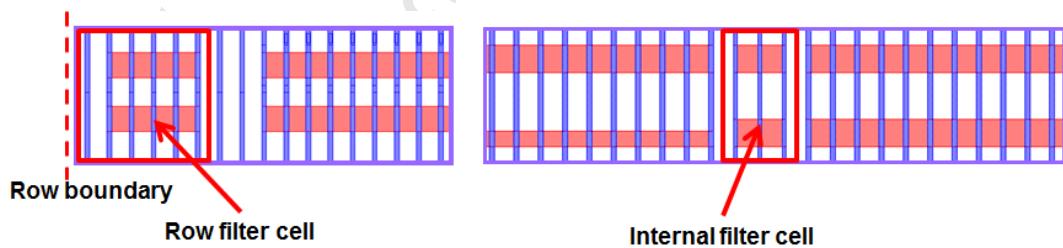


Figure 7.1.4 Layout with filler cells

7.1.1.1.2 Guidelines for device VC placement

- Special VC placement design might introduce device drive-current effect on large-width devices. For high speed purpose, it is recommended to have symmetric and more than one VC at device. In contrast, a single or asymmetric VC placement is estimated to have drive-current penalty than standard layout. If asymmetric VC placement is necessary, shorten VC space is strongly suggested.

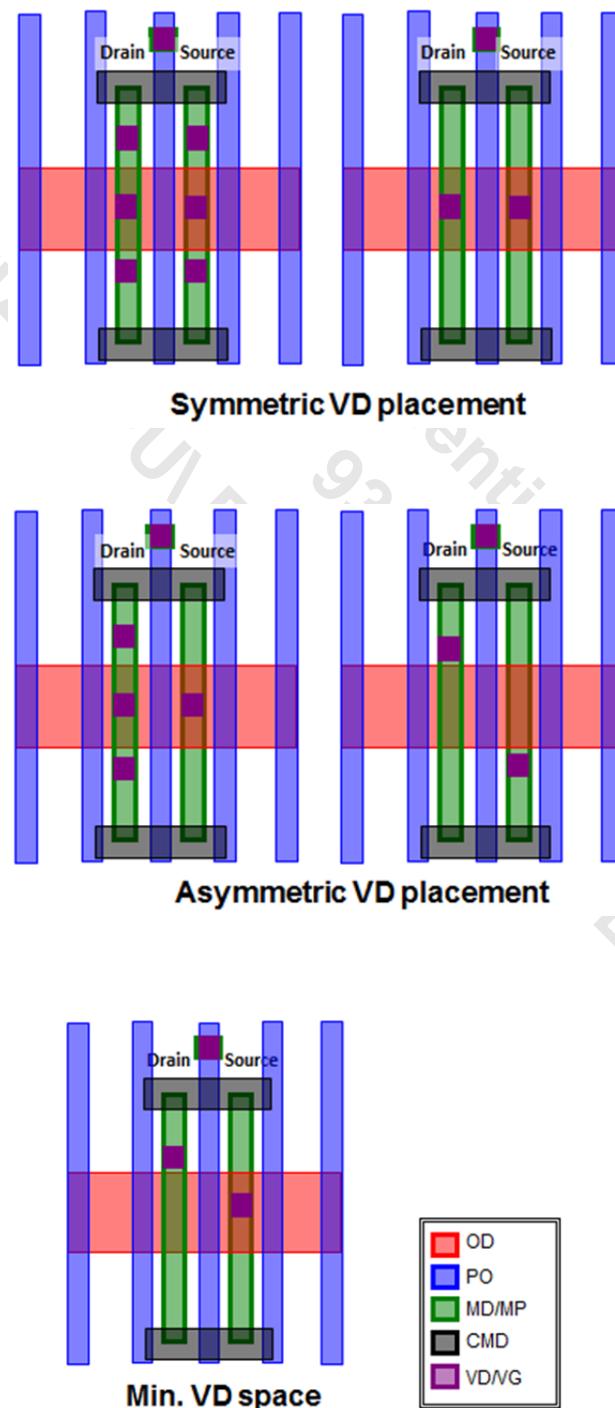


Figure 7.1.5 Illustration for VD placement on device

7.1.1.2 Electrical Wiring

- It is not recommended to use PO or MEOL as the interconnection between two circuits with long distance.
- Maintain uniform metal density to minimize wire sheet resistance variation, especially for min. long metal wire.
- Wherever possible, use two or more narrower metal buses to replace a single bus that uses the maximum width.
- Maintain metal density in the mid-range of the specification, avoiding the two extreme ends.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations during placement. It may have unexpected violation during the IP/macro placement due to the environment, even if the IP/macro already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (e.g., power/ground bus), under the proper high density limit.
- Need dummy insertion in the library/IP/Macro blockage area:
 - Either extend hard macro boundary to align with blockage area or minimize the distance from the blockage edge to the macro cell boundary. Also embed this blockage region in macro cell.
 - Have dummy patterns in the blockage area as default and being verified with library characterization process.
 - Need to re-define I/O pin for P&R at new macro cell boundary if you push out hard macro boundary to align with blockage area.
 - Avoid any large open area without any metal patterns inside in the macro cell area.

7.1.2 Layout Tips for Minimizing Critical Areas

Defects are variable in size and therefore follow a size distribution. A *critical area* of a given layout is an accumulative area that is susceptible to certain failures (shorts or opens) caused by defects of a certain size. For example, although the total occupied areas are the same in panels A and B of Figure 7.1.2, the wires in layout A are more vulnerable to defect-induced shorts because they have a larger critical area.

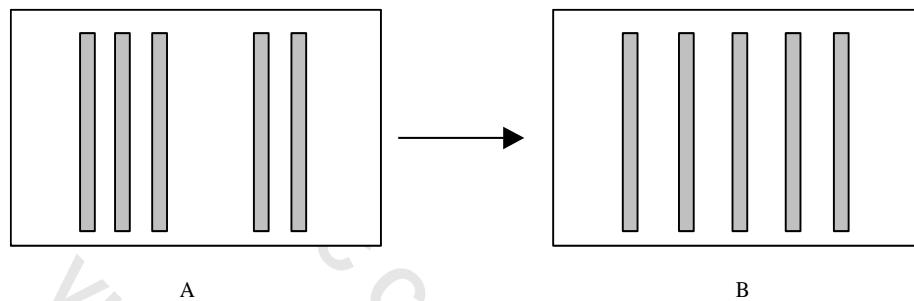


Figure 7.1.2 Layout Examples of Critical Areas

- Reduce the critical area of wire open/short

Spacing out the wiring with the same or similar pitch, with manually layout modification since cell level, to take advantage of a little larger space with similar wire pitch can reduce the critical area of wire short but also wire uniformity. This practice has additional benefits:

- It can reduce wire cross coupling.
- It can reduce the possibility of pattern short.
- It can evenly distribute the local pattern density, thereby creating less variation in wire Rs.

- Reduce the probability of via (including VIA0) open circuit.

Open and soft open (excessively high R_c) of a single via (including VIA0) is usually a yield bottleneck, given their sheer number in a chip. While the manufacturer strives to bring down the failure rate as low as possible, a designer can contribute to further reduction of this failure probability:

Whenever possible, include redundant VIA0 and VIA for the following benefits:

- Reduces the probability of an open circuit
- Reduces the resistance and potential variation.
- Potentially increases the stress migration immunity.

- Reduce the probability of open via in a metal island with single-via stack.

- Whenever possible, use a larger than minimum size metal island with stacking single via. This can reduce the risk of via resistance variation or open via.

7.2 DFM Recommendations and Guidelines Summary

- Please use the following advisory/recommended dimensions and guidelines whenever possible, unless doing so impacts chip size or performance.
- DFM does not have to comply to the advisory/recommendation value completely. Any change even by one grid helps.
- By using DFM recommendations and guidelines, higher precision of models, better reliability, lower variation on process, timing or yield may be expected.
- If your circuits want to adopt the Recommendations of section 7.2.1, TSMC DRC deck can help you to detect the designs not following with the recommendations. This DFM Recommendation DRC deck is bundled in the TSMC logic DRC deck. The following 2 methods can specify the region for examining DFM recommendation compliance by DFM DRC deck. Please also refer to the “User Guide” in the DFM deck
 - (1) Cover the design by special CAD layer “RruleRecommend” (CAD_ID: 182;2).
 - (2) Cell selection based on the following variables: CellsForRRuleRecommended

7.2.1 Recommendations

- Using minimum dimension of the following rules is okay. If a non-minimum recommendation is used, however, the variation of the related electrical parameter (e.g. via R_c) can be minimized and better yield stability may be expected. It is recommended that the Recommendations be used wherever possible.

Rule No.	Description	Label	Op.	Rule
H240.FB.W.1.6®	Recommended width of FB_9 in vertical direction	W1F	=	1.2000+0.24 00*n
H300.FB.W.1.6®	Recommended width of {FB_8 OR BV_FB [width = 0.300 μm] } in vertical direction	W1F	=	1.5000+0.60 00*n
PO.S.25®	Empty space of {ALL_PO NOT CPO} (Except RH_TNB, NWDMY, TCDDMY, ICOVL_SINGLE, or following conditions: 1. {SEALRING_ALL SIZING 0.450 μm }, 2. Chip corner triangle empty areas if seal-ring is added by tsmc) DRC flags {{CHIP NOT {ALL_PO NOT CPO}} SIZING down/up 0.450 μm }	S25	\leq	0.9000
MD.S.23.1®	MD [INTERACT OD] to 2nd MD space rule: Space of Checked_MD to the second {ALL_MD NOT ALL_CMD} in horizontal direction (Except FB_9, FB_8, BLK_WF, PO_P63) Definition of Checked_MD: { {{MD [width = 0.024 μm] NOT CMD} AND OD [width < 0.188 μm] } SIZING 0.005 μm in vertical direction } (The second MD is required to be placed beside the MD [INTERACT OD])	S23A	=	0.0900

Rule No.	Description	Label	Op.	Rule
MD.S.24.1®	MD [INTERACT OD] to 2nd MD space rule: Space of Checked_MD to the second {ALL_MD NOT ALL_CMD} in horizontal direction [INSIDE PO_P63] (Except FB_9, FB_8, BLK_WF) Definition of Checked_MD follows MD.S.23 (The second MD is required to be placed beside the MD [INTERACT OD])	S23A	=	0.1020
MD.S.25.1®	MD [INTERACT OD] to 2nd MD space rule: Space of Checked_MD to the second {ALL_MD NOT ALL_CMD} in horizontal direction [INSIDE PO_P76] Definition of Checked_MD follows MD.S.25(The second MD is required to be placed beside the MD [INTERACT OD])	S25A	=	0.1220
VIAx.R.9®	Recommended maximum consecutive stacked VIAx layer, which has only one via for each VIAx layer to avoid high Rc		≤	4
VIAxs.R.9®	Recommended maximum consecutive stacked VIAxs layer, which has only one via for each VIAxs layer to avoid high Rc		≤	4
VIAxa.R.9®	Recommended maximum consecutive stacked VIAxa layer, which has only one via for each VIAxa layer to avoid high Rc		≤	4
VIAya.R.9®	Recommended maximum consecutive stacked VIAya layer, which has only one via for each VIAya layer to avoid high Rc		≤	4
Mya.S.15®	Recommended space [at least one metal line width > 1.350 μm]	SN	≥	0.4500
Mya.DN.5.1®	Recommended minimum metal density in window 25 μm x 25 μm, stepping 12.5 μm (Except LOGO, INDDMY, TCDDMY_Mn, ICOVL_SINGLE, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	30%
Mya.DN.6.1®	Recommend metal density for IP level [window 10 μm x 10 μm, stepping 5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. the maximum area of the merged low density windows [density < 1%] ≤ 1600 μm², while the merged low density windows width is > 30 μm, 2. the maximum area of the merged low density windows [density < 1%] ≤ 4500 μm², 3. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%
Mya.DN.8®	Recommended maximum metal density in window 25 μm x 25 μm, stepping 12.5 μm (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	60%
Mya.R.4®	Recommended maximum stacked M1, Mx, Mxa and Mya layers of high density area [density > 70% in window 800 μm x 800 μm, stepping 80 μm]		≤	4
Mya.A.1®	Recommended area (Except DMya_O)	A1	≥	0.02200
VIAy.R.9®	Recommended maximum consecutive stacked VIAy layer, which has only one square via for each VIAy layer to avoid high Rc		≤	4
My.S.15®	Recommended space [at least one metal line width > 1.350 μm]	SN	≥	0.4500
My.DN.5.1®	Recommended minimum metal density in window 25 μm x 25 μm, stepping 12.5 μm (Except LOGO, INDDMY, SEALRING_ALL, TCDDMY_Mn, ICOVL_SINGLE)		≥	30%
My.DN.6.1®	Recommend metal density for IP level [window 10 μm x 10 μm, stepping 5 μm] (Except TCDDMY_Mn, ICOVL_SINGLE, or following conditions: 1. the maximum area of the merged low density windows [density < 1%] ≤ 1600 μm², while the merged low density windows width is > 30 μm, 2. the maximum area of the merged low density windows [density < 1%] ≤ 4500 μm², 3. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	1%

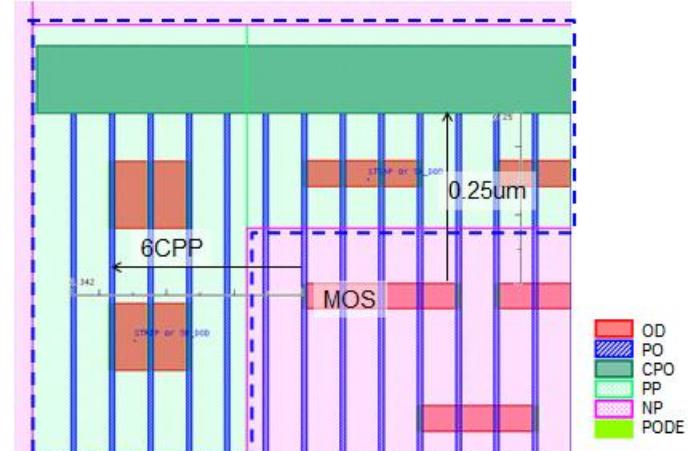
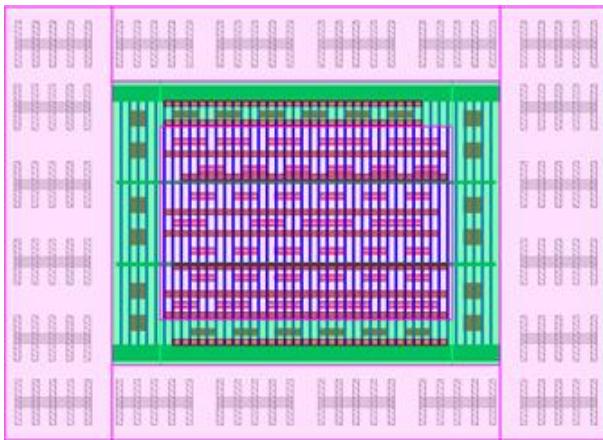
Rule No.	Description	Label	Op.	Rule
My.DN.8®	Recommended maximum metal density in window 25 µm x 25 µm, stepping 12.5 µm (Except TCDDMY_Mn, ICOVL_SINGLE)		≤	60%
My.R.4®	Recommended maximum stacked M1, Mx, Mxa, Mya and My layers of high density area [density > 70% in window 800 µm x 800 µm, stepping 80 µm]		≤	4
My.A.1®	Recommended area (Except DMy_O)	A1	≥	0.02200
VIAyy.EN.0®	Recommended enclosure by My or Myy is defined by either VIAyy.EN.1® or VIAyy.EN.2® or VIAyy.EN.2.1®			
VIAyy.EN.1®	Recommended enclosure by My or Myy to avoid high Rc	EN1R	≥	0.0260
VIAyy.EN.2®	Recommended enclosure by My [at least two opposite sides] to avoid high Rc	EN2R	≥	0.0450
VIAyy.EN.2.1®	Recommended enclosure by Myy [at least two opposite sides] to avoid high Rc	EN2R	≥	0.0450
VIAyy.R.8®	Recommended maximum consecutive stacked VIAyy layer, which has only one via for each VIAyy layer to avoid high Rc (It is allowed to stack more than four VIAyy layers if two or more VIAs in each VIAyy layer are on the same metal)		≤	4
Myy.S.1®	Recommended space (to reduce the short possibility)	S1	≥	0.0810
Myy.EN.0®	Recommended enclosure of VIAyy-1 is defined by either Myy.EN.1® or Myy.EN.2®			
Myy.EN.1®	Recommended enclosure of VIAyy-1 to avoid high Rc	EN1R	≥	0.0270
Myy.EN.2®	Recommended enclosure of VIAyy-1 [at least two opposite sides] to avoid high Rc	EN2R	≥	0.0450
Myy.A.1®	Recommended area (Except DMyy_O)	A1	≥	0.02850
Myy.DN.5®	Recommended minimum metal density in window 50 µm x 50 µm, stepping 25 µm (Except LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	30%
Myy.DN.6®	Recommend metal density ≥ 1% for IP level. All of condition-A, condition-B, and condition-C are recommended (1) Condition-A: For IP level, recommend metal density [window 36 µm x 36 µm, stepping 36 µm] ≥ 1% (2) Condition-B: For IP level, recommend maximum area of merged low density windows [checking window 9 µm x 9 µm, stepping 4.5 µm, density < 1%] ≤ 1296 µm², except merged low density windows width ≤ 27 µm (3) Condition-C: For IP level, recommend maximum area of merged low density windows [checking window 9 µm x 9 µm, stepping 4.5 µm, density < 1%] ≤ 3645 µm² (Except following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)			
Myy.DN.7®	It is not recommended to have local density < 5% of all 3 consecutive metal (Myy, Myy+1 and Myy+2) over any 13.5 µm x 13.5 µm (stepping 13.5 µm) for IP level, i.e. it is allowed for either one of Myy, Myy+1, or Myy+2 to have a local density ≥ 5% (The metal layers include Myy and dummy metals) (Except following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)			

Rule No.	Description	Label	Op.	Rule
Myy.DN.8®	Recommended total Myy island (for all Myy layers) density < 5.3E+4 ea/mm ² across full chip The definition of counts of small Myy island: 1. Myy width = 0.064 μm 2. Myy length ≤ 0.468 μm 3. Myy has two segments with space = 0.062 μm with the PRL (0.188 μm ≤ PRL < 0.468 μm)			
VIAyx.EN.0®	Recommended enclosure by Myy or Myx is defined by either VIAyx.EN.1® or VIAyx.EN.2®.			
VIAyx.EN.1®	Recommended enclosure by Myy or Myx to avoid high Rc. [all sides]	EN1R	≥	0.0410
VIAyx.EN.2®	Recommended enclosure by Myy or Myx [at least two opposite sides] to avoid high Rc.	EN2R	≥	0.0680
Myx.DN.5®	Recommended minimum metal density in window 50 μm x 50 μm, stepping 25 μm (Except LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	30%
Myx.EN.0®	Recommended enclosure of VIAyx-1 is defined by either Myx.EN.1® or Myx.EN.2®.			
Myx.EN.1®	Recommended enclosure of VIAyx-1 to avoid high Rc. [all sides]	EN1R	≥	0.0410
Myx.EN.2®	Recommended enclosure of VIAyx-1 [at least two opposite sides] to avoid high Rc.	EN2R	≥	0.0680
Mz.DN.5®	Recommended minimum metal density in window 50 μm x 50 μm, stepping 25 μm (Except LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	30%
Mr.DN.5®	Recommended minimum metal density in window 50 μm x 50 μm, stepping 25 μm (Except LOGO, SEALRING_ALL, or following conditions: 1. Chip corner triangle empty areas if seal-ring is added by tsmc)		≥	30%
OD2.DH.1®	OD2 extension on OD/PO ≤ 0.5 μm (Except the empty extension region smaller than 0.5 μm x 2 μm) DRC flags {{OD2 NOT ALL_OD} NOT ALL_PO} can enclose a 0.5 μm x 2 μm rectangle. Action: Please reduce OD2 extension on OD/PO to increase the insertion region for dummy fill.			
FEOLBLK.DH.1®	FEOLBLK extension on OD/PO ≤ 0.2 μm (Except the empty extension region smaller than 0.2 μm x 20 μm) DRC flags {{FEOLBLK NOT ALL_OD} NOT ALL_PO} can enclose a 0.2 μm x 20 μm rectangle. Action: Please reduce FEOLBLK extension on OD/PO to increase the insertion region for dummy fill.			
INDDMY.DH.1®	INDDMY extension on OD/PO ≤ 0.14 μm (Except the empty extension region smaller than 0.14 μm x 2 μm) DRC flags {{INDDMY NOT ALL_OD} NOT ALL_PO} can enclose a 0.14 μm x 2 μm rectangle. Action: Please reduce INDDMY extension on OD/PO to increase the insertion region for dummy fill.			
DIODMY.DH.1®	DIODMY extension on OD/PO ≤ 0.14 μm (Except the empty extension region smaller than 0.14 μm x 2 μm) DRC flags {{DIODMY NOT ALL_OD} NOT ALL_PO} can enclose a 0.14 μm x 2 μm rectangle. Action: Please reduce DIODMY extension on OD/PO to increase the insertion region for dummy fill.			
SR_ESD.DH.1®	SR_ESD extension on OD/PO ≤ 0.14 μm (Except the empty extension region smaller than 0.14 μm x 2 μm) DRC flags {{SR_ESD NOT ALL_OD} NOT ALL_PO} can enclose a 0.14 μm x 2 μm rectangle. Action: Please reduce SR_ESD extension on OD/PO to increase the insertion region for dummy fill.			

Rule No.	Description	Label	Op.	Rule
NWDMY.DH.1®	NWDMY extension on NW $\leq 0.14 \mu\text{m}$ (Except the empty extension region smaller than $0.14 \mu\text{m} \times 2 \mu\text{m}$) DRC flags {{NWDMY NOT NW} can enclose a $0.14 \mu\text{m} \times 2 \mu\text{m}$ rectangle. Action: Please reduce NWDMY extension on NW to increase the insertion region for dummy fill.			
VT.DH.1®	ALL_VT extension on OD/PO $\leq 0.14 \mu\text{m}$ (Except the empty extension region smaller than $0.14 \mu\text{m} \times 2 \mu\text{m}$) DRC flags {{ALL_VT NOT ALL_OD} NOT ALL_PO} can enclose a $0.14 \mu\text{m} \times 2 \mu\text{m}$ rectangle. Action: Please reduce ALL_VT extension on OD/PO to increase the insertion region for dummy fill.			
AN.R.93m®	Recommended ANARRAY_M enclosure by Chip_Boundary in chip level		\geq	5
DMn.S.7®	Empty space of {{Mn OR DMn} OR DMn_O} DRC flags {{CHIP NOT {{Mn OR DMn} OR DMn_O}} SIZING down/up 0.400 μm } (Except LOGO, INDDMY, or following conditions: 1. {SEALRING_ALL SIZING 0.500 μm }, 2. {TCDDMY_Mn SIZING 0.2 μm }, 3. ICOVL_SINGLE, 4. Chip corner triangle empty areas if seal-ring is added by tsmc) (This check is only applied to M0/M1/Mxs/Mx/Mxa/Mya/My)	S7R	\leq	0.8000
MIM.VIAz.S.10®	Space of VIAz [INSIDE CTMFFINAL] to under metal (Mz/Myz) [the first metal layer below HD MIM]. (Overlap is not allowed)	N	\geq	0.0720
MIM.VIAz.S.10.2®	VIAz [INSIDE {CBMFFINAL NOT CTMFFINAL}] space to under metal (Mz/Myz) [the first metal layer below HD MIM, with different net]. (Overlap is not allowed)	O1	\geq	0.0720
MIM.VIAz.R.2®	Space of VIAz [INSIDE CTMFFINAL] to under metal (Mz/Myz) [the first metal layer below HD MIM, space < 0.468 μm] must be equal at both side of VIAz.			
MIM.VIAz.R.2.1®	VIAz [INSIDE {CBMFFINAL NOT CTMFFINAL}] space to under metal (Mz/Myz) [the first metal layer below HD MIM, space < 0.468 μm] must be equal at both side of VIAz.			
MIM.VIAr.S.10®	Space of VIAr [INSIDE CTMFFINAL] to under metal (Mz/Mr) [the first metal layer below HD MIM]. (Overlap is not allowed)	N	\geq	0.0720
MIM.VIAr.S.10.2®	VIAr [INSIDE {CBMFFINAL NOT CTMFFINAL}] space to under metal (Mz/Mr) [the first metal layer below HD MIM, with different net]. (Overlap is not allowed)	O1	\geq	0.0720
MIM.VIAr.R.2®	Space of VIAr [INSIDE CTMFFINAL] to under metal (Mz/Mr) [the first metal layer below HD MIM, space < 0.558 μm] must be equal at both side of VIAr.			
MIM.VIAr.R.2.1®	VIAr [INSIDE {CBMFFINAL NOT CTMFFINAL}] space to under metal (Mz/Mr) [the first metal layer below HD MIM, space < 0.558 μm] must be equal at both side of VIAr.			

7.2.2 Guidelines

Rule No.	Description	Label	Op.	Rule												
G.6g ^U	For DNW, NW, NP, PP, Mn ($n = 0, 1, x, xa, ya, y, yy, yx, yz, z, r$) all vertices and intersections of 45-degree polygon must be on an integer multiple of 0.0005 μm .															
OPC.R.2g ^U	Avoid small jogs (Figure 3.6.4) It is recommended to use greater than, or equal to, half of the minimum width of each layer for each segment of a jog.															
OD.L.2g ^U	It is strongly suggested to limit the max interconnect length to be as short as possible to avoid high R_s variation															
OD.R.1g ^U	It is strongly suggested to surround MOS with SR_DOD or STRAP in PO_P57_Group.															
DNW.R.5g ^U	Recommended not using floating RW unless necessary to avoid unstable device performance															
NW.R.1g ^U	Recommend not using unintentional floating well to avoid unstable device performance															
NWRSTI.R.3g	Recommended to use rectangle shape resistor DRC flags {NWDMDY AND NWRSTI} is not a rectangle															
VIAyy.R.9g ^U	Recommend using redundant VIAs to avoid high R_c wherever layout allows.															
VIAyx.R.9g ^U	Recommend using redundant VIAs to avoid high R_c wherever layout allows.															
VIAr.R.5g ^U	Recommend using redundant VIAs wherever layout allows															
IND.R.11g ^U	Recommend putting NT_N to fully cover the inductor (metal) to achieve the high quality factor.															
SRAM.R.9g ^U	Sense-amp and decoder redundancy: In addition to bit-row and/or bit-column redundancy design, redundancy in peripheral array elements, such as sense amplifiers and decoders, is recommended. Architectural efficiency can minimize the added overhead area entailed by this additional redundancy. Peripheral element redundancy is especially important for high-density memory blocks.															
SRAM.R.11g ^U	Guardring: It is recommended to have an additional VSS (PW) guardring around the memory circuit block.															
DMn.W.1g ^U	Recommended DMn size (width x length) <table border="1" style="margin-left: 20px;"> <tr><td></td><td>Square (Utility Fill)</td></tr> <tr><td></td><td>Width x Length</td></tr> <tr><td>M0, M1, Mxs, Mx and Mxa</td><td>0.12x1.4~0.24x0.7</td></tr> <tr><td>Mya and My</td><td>0.108x0.450~2x2</td></tr> <tr><td>Myy</td><td>0.180x0.900 ~ 0.270x1.800</td></tr> <tr><td>Myx, Myz and Mz</td><td>0.36x1.28~1.8x1.8</td></tr> </table>		Square (Utility Fill)		Width x Length	M0, M1, Mxs, Mx and Mxa	0.12x1.4~0.24x0.7	Mya and My	0.108x0.450~2x2	Myy	0.180x0.900 ~ 0.270x1.800	Myx, Myz and Mz	0.36x1.28~1.8x1.8			
	Square (Utility Fill)															
	Width x Length															
M0, M1, Mxs, Mx and Mxa	0.12x1.4~0.24x0.7															
Mya and My	0.108x0.450~2x2															
Myy	0.180x0.900 ~ 0.270x1.800															
Myx, Myz and Mz	0.36x1.28~1.8x1.8															



7.2.3 Grouping Table of Recommendations

Rule No.	Priority	Manufacturing Concern				Device performance	Executable Design Implementation	Dummy Health
		CMP	Litho/OPC	Defect	Others			
H240.FB.W.1.6®	2		v					
H300.FB.W.1.6®	2		v					
PO.S.25®	2	v						
MD.S.23.1®	2		v					
MD.S.24.1®	2		v					
MD.S.25.1®	2		v					
VIAx.R.9®	2	v						
VIAxs.R.9®	2	v						
VIAxa.R.9®	2	v						
VIAya.R.9®	2	v						
VIAyy.R.8®	2	v						
Mya.S.15®	2			v				
Mya.A.1®	2		v					
Mya.DN.5.1®	2	v						
Mya.DN.6.1®	2				v		Apply tsmc dummy metal utility	
Mya.DN.8®	2	v						
Mya.R.4®	2	v						
VIAy.R.9®	2	v					Apply tsmc P&R techfile	
My.S.15®	2			v				
My.DN.5.1®	2	v						
My.DN.6.1®	2				v		Apply tsmc dummy metal utility	
My.DN.8®	2	v						
My.R.4®	2	v						
My.A.1®	2		v					
VIAyy.EN.0®	1				v		Apply tsmc P&R techfile for DFM-VIA	
VIAyy.EN.1®	1				v		Apply tsmc P&R techfile for DFM-VIA	
VIAyy.EN.2®	2				v			
VIAyy.EN.2.1®	1				v		Apply tsmc P&R techfile for DFM-VIA	
Myy.S.1®	2			v				
Myy.EN.0®	1				v		Apply tsmc P&R techfile for DFM-VIA	
Myy.EN.1®	1				v		Apply tsmc P&R techfile for DFM-VIA	
Myy.EN.2®	1				v		Apply tsmc P&R techfile for DFM-VIA	
Myy.A.1®	2		v					
Myy.DN.5®	2	v						
Myy.DN.6®	2				v		Apply tsmc dummy metal utility	
Myy.DN.7®	2	v					Apply tsmc dummy metal utility	
Myy.DN.8®	2				v		Apply tsmc P&R techfile for DFM-VIA	
VIAyx.EN.0®	1				v		Apply tsmc P&R techfile for DFM-VIA	
VIAyx.EN.1®	1				v		Apply tsmc P&R techfile for DFM-VIA	
VIAyx.EN.2®	1				v		Apply tsmc P&R techfile for DFM-VIA	
Myx.DN.5®	2	v						

Rule No.	Priority	Manufacturing Concern				Device performance	Executable Design Implementation	Dummy Health
		CMP	Litho/OPC	Defect	Others			
Myx.EN.0®	1				v		Apply tsmc P&R techfile for DFM-VIA	
Myx.EN.1®	1				v		Apply tsmc P&R techfile for DFM-VIA	
Myx.EN.2®	1				v		Apply tsmc P&R techfile for DFM-VIA	
Mz.DN.5®	2	v						
Mr.DN.5®	2	v						
OD2.DH.1®	2							v
FEOLBLK.DH.1®	2							v
INDDMY.DH.1®	2							v
DIODMY.DH.1®	2							v
SR_ESD.DH.1®	2							v
NWDMY.DH.1®	2							v
VT.DH.1®	2							v
AN.R.93m®	2				v			
DMn.S.7®	2	v						
G.6g ^U	3		v					
OPC.R.2g ^U	3		v					
OD.R.1g ^U	2	v					Manual draw STRAP or SR_DOD	
OD.L.2g ^U	3					v		
DNW.R.5g ^U	3					v		
NW.R.1g ^U	3					v		
NWRSTI.R.3g	3					v		
VIAyy.R.9g ^U	2			v			Apply tsmc P&R techfile for DFM-VIA	
VIAyx.R.9g ^U	2			v			Apply tsmc P&R techfile for DFM-VIA	
VIAr.R.5g ^U	2			v			Apply tsmc P&R techfile for DFM-VIA	
IND.R.11g ^U	3				v			
SRAM.R.9g ^U	2				v			
SRAM.R.11g ^U	2				v			
DMn.W.1g ^U	2				v			
MIM.VIAz.S.10®	2				v			
MIM.VIAz.S.10.2®	2				v			
MIM.VIAz.R.2®	2				v			
MIM.VIAz.R.2.1®	2				v			
MIM.VIAr.S.10®	2				v			
MIM.VIAr.S.10.2®	2				v			
MIM.VIAr.R.2®	2				v			
MIM.VIAr.R.2.1®	2				v			

7.3 Guidelines for mask making efficiency

- Draw wires (polygons) in an orthogonal fashion.
- Avoid the metal routing with minimum metal space of U-shape metal, especially this U-shape metal with a short length line-end. Such U-shape routing is non-necessary and can be replaced by simple L-shape metal.
- Avoid leaving small jogs, especially in the corner areas where metal space is at a minimum.
- Avoid using 45-degree turns, except for very wide metal buses, where the length of the 45-degree portion should be sufficiently large.

TSMC Confidential Information
938214
VIAI CPU Platform\ Col. I Ltd.
10/05/2018

7.4 Die Size Optimization Kit (GDA and MFU)

- Gross Die Advisor (GDA) is to optimize die size x-y for higher mask field utilization (MFU) and gross die (GD) while keep die area as constant. This is only available at TSMC online in below path:
Home/Design Portal 2.0/Technology Selection (GDA) /Gross Die Advisor (MFU calculator)
- The function of GDA is based on user's input about die size, scribe_line width and TSMC generic fabrication conditions to recommend a list of other die size with higher gross die and MFU. Based on the result, customer can have further survey on adjusting the die size in the early design phase.

7.4.1 What is MFU?

- Mask Field Utilization (MFU) is a ratio of mask utilized region and is conceptually defined as (multiple die area+ scribe_line area) / (scanner maximum field area), as Fig.7.4.1.1 shown.
- Low MFU implies low productivity of photo scanner at all lithography layers. It is important to maximize MFU as large as possible.

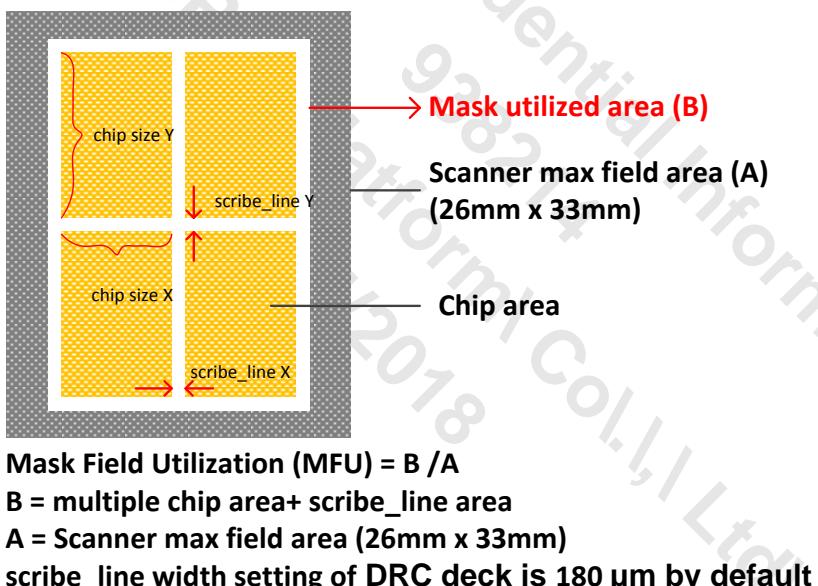


Figure 7.4.1.1 Example of MFU

7.4.2 How to simulate MFU?

- Estimate the mask field utilization (MFU) of your chip in following stages and adjust your die dimension base on the advised results for high MFU and even gross dies gain:
 - **During chip specification:** use MFU Advisor of T-000-CL-RP-013 (TSMC MFU ADVISOR) or TSMC On-line MFU/GDA.
 - **During chip floor-plan:** use MFU Advisor or MFU floor-plan tcl script of T-000-CL-RP-013 (TSMC MFU ADVISOR) or TSMC On-line MFU/GDA.
 - **Before tapeout:** check MFU.R.1 by DRC and confirm the final MFU by TSMC On-line MFU/GDA.
- MFU estimation is related to the width of scribe_line, you can consult tsmc for the required scribe_line width if accurate MFU is required.

Notes: TSMC online path for MFU/GDA :

Home/Design Portal 2.0/Technology Selection (GDA) /Gross Die Advisor (MFU calculator)

7.4.3 Design Guidelines for Higher MFU

- **Before design:**
 - Square shape digital block and IP is preferred.
 - For rectangular shape IP, provide 2 orientation types of the same IP with keeping core PO gate in vertical direction. For example, left/right type IO and top/bottom type IO or horizontal and vertical type IP shapes.
 - Use “MFU Advisor” or “MFU Floor plan tcl script” for die size with better MFU in floor plan design phase.
 - Avoid die size at the borderline with low MFU
- **At floor-plan stage or after floor-plan stage:**
 - Core limited design: IP and blocks size and floor-plan adjustment may be needed.
 - I/O limited design: I/O and interface IP adjustment may be needed.

7.4.4 MFU DRC examination

Rule No.	Description	Label	Op.	Rule
MFU.R.1	Mask Field Utilization (MFU) is a ratio of mask utilized region which is calculated by (multiple die area + scribe_line area) / (scanner maximum field area) in chip level.		\geq	80%

- MFU calculation in DRC is defined as : $MFU = (Fx \cdot Fy) / (Rx \cdot Ry)$
 - Rx and Ry: maximum mask field size in X- and Y-direction, Rx = 26000 μm and Ry = 33000 μm .
 - Fx = (gross die Column)*(Cx+Sx) + Sx
 - Fy = (gross die Row)*(Cy+Sy) + Sy
 - Cx and Cy: the dimension of (Chip_Boundary with SEALRING_ALL) = (Chip_Boundary + 2*21.6 μm) in X- and Y-direction respectively.
 - Sx and Sy: the scribe_line width in X- and Y-direction. Single scribe_line width = 65.6 μm . Multiple scribe_line width = n * 60 μm (n = 2,3,4...)
 - The scribe_line width will affect the accuracy of large chip recognition. Customers must confirm the scribe_line width information during DRC process otherwise it will follow the default setting – 180 μm (triple scribelines).
 - The variable settings in DRC deck (as the example of Figure 7.4.1.2) can be modified based on the final scribe_line width of real tape-out. In general, tsmc's single scribe_line width is 65.6 μm and multiple scribe_line width is n * 60 μm (n = 2,3,4...). e.g. 5x scribeline width = 5 * 60 μm = 300 μm .

```
// The following variables are for Mask Field Utilization Check. Please change it if using different value.
VARIABLE ScribeLineX 180.0 // Width of scribe_line X (um) for Mask Field Utilization (MFU)
VARIABLE ScribeLineY 180.0 // Width of scribe_line Y (um) for Mask Field Utilization (MFU)
```

You can modify the variables in DRC deck based on real tape-out situation

Figure 7.4.1.2 Variable settings of scribe_line width in DRC deck

8 Layout Rules and Recommendations for Analog Circuits

This chapter provides information about the following topics:

- 8.1 User guides
- 8.2 Layout rules, recommendations and guidelines for the analog design
- 8.3 Noise
- 8.4 Burn-in Guidelines for Analog Circuits

8.1 User Guides

1. Use these rules, recommendations, and guidelines to achieve better analog device performance and matching. In analog circuits, good device matching provides good performance margin and production yield.
2. Examples of analog circuits:
 - Operational Amplifier: this includes differential input pair, bias circuit, and current mirror.
 - DAC: this includes constant current source, amplifier using external Rset to adjust full range current, and bias circuit.
 - ADC: this includes comparator, amplifier, sample/hold switches, switching capacitor, and reference voltage resistor ladder.
 - PLL: this includes VCO (delay stage) and charge pump (current mirror and buffer/opamp)
 - Bandgap: BJT, current mirror, bias circuit, differential amplifier, and ratioed resistor.
 - LNA and mixer
 - Sense amplifiers in memories.
 - Matching pair includes active and passive devices.
3. If you have concern about the rules, recommendations, and guidelines with respect to your circuit, TSMC DRC deck can help you to flag the violations. Analog DRC deck is bundled in the TSMC logic DRC deck. The following two methods can specify the region to the run analog part. Please also refer to the user guide in the DRC deck.
 - Dummy layer
 - RRuleAnalog (CAD layer: 182;3): for the layout rules, recommendations, and guidelines of the analog designs.
 - Cell selection based on the following variable:
 - CellsForRRuleAnalog: only check the cells listed in the variable
 - ExclCellsForRRuleAnalog: don't check the cells listed in the variable
4. A registered symbol “U” is marked after the rule number to indicate that the rule is not checked by DRC.

8.2 Layout Rules, Recommendations and Guidelines for the Analog Designs

8.2.1 General Guidelines

Rule No.	Description	Label	Op.	Rule
AN.R.1mg ^U	Do not use minimum widths and lengths for matching devices. Using current source device as an example, the designer should refer to the device I-V curve to check at which W/L range does the drain saturation current reach constant.			
AN.R.3m ^U	<p>Recommend to insert dummy patterns in the empty area, even if the OD, PO, and metal densities have already met the density rules. Insert the dummy patterns properly.</p> <p>The recommended steps for this is given as AN.R.3m:</p> <ol style="list-style-type: none"> 1. Insert the same geometric dummy cells manually to minimize the proximity effect in all directions (Figure 8.2.1.1) 2. Use ODBLK, POBLK, or DM1EXCL/DMxEXCL layer to cover your analog circuit, which will exclude SR_DOD, SR_DPO, or DMn_O insertion during chip level dummification. 3. Do electrical or silicon characterization. 			

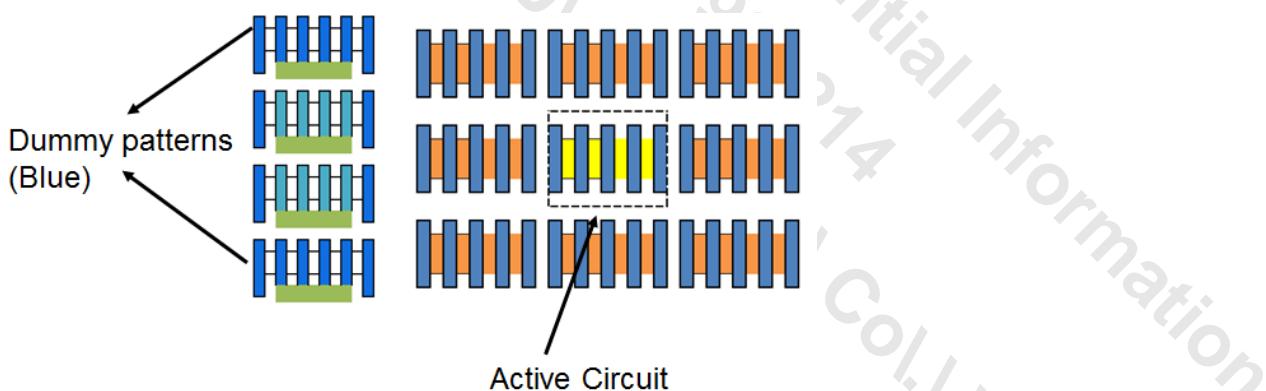


Figure 8.2.1.1 Example of manual DOD, SR_DOD, DPO, SR_DPO, or unit cell

8.2.2 MOS Recommendations

8.2.2.1 MOS

8.2.2.1.1 Rule of Thumb for MOS devices in analog circuits

No.	Description
1	It is recommended to keep the total I_{g_off} [I_{g_off} of "Mref + M1 + ... + Mn + Mc" at all PVT (Process Voltage Temperature) corners] lower than 0.1% of I_{ref} for better matching performance of the current mirror. (Figure 8.2.2.1.1)
2	It is recommended to do the following actions for EM concerns. Put full VC on source and drain, and stack VIA0 on top of VC. Analog designs may have EM concerns: Analog design with $L_g \leq 0.020 \mu m$ and operating frequency \geq core 5GHz & IO 3GHz. Example: I/O devices for Graphics GDDR5/6 (F=5~12GHz), core device > 12GHz serdes VCO/DFF/output stage
3	In order to avoid the drift of electrical parameter matching, it is important to maintain identical DC bias on each matching-transistor (NMOS or PMOS) at all operation conditions (e.g., standby conditions). If the DC bias is not identical, please evaluate the impact of matching performance.
4	It is recommended to floor-plan the building blocks as individual groups, and then keep the poly density difference within 3% among each group for better operation of the devices with $V_{gs}-V_{th_gm} < 350mV$.

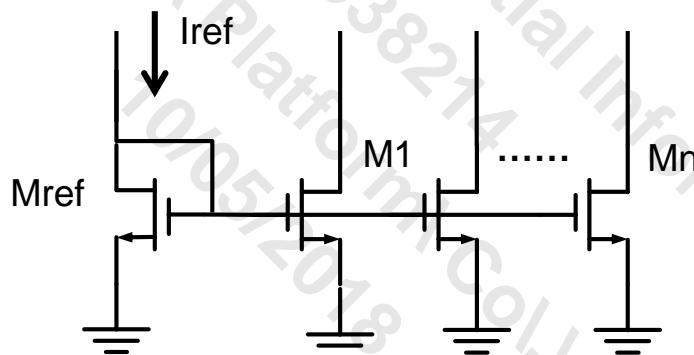


Figure 8.2.2.1.1 Current mirror

8.2.2.1.2 High MOS Rout application

Rule No.	Description	Label	Op.	Rule
AN.R.103mg ^U	For core devices, to achieve low gds of longer channel, stack gate solution is recommended.			
AN.R.104mg ^U	For core devices, stack gate with shorter Lg shows better or competitive performance in Id variation and low gds.			

8.2.2.1.3 High Power application

Rule No.	Description	Label	Op.	Rule
AN.R.112mg ^U	For reducing self-heating temperature in high power dissipating MOS: a. Recommend to use source connected guard ring with minimum distance to the device b. Recommend to put stacked metals at source and drain			

8.2.2.1.4 Matching guidelines

Rule No.	Description	Label	Op.	Rule
PO.EX.2mg ^U	For current mirror devices using common OD, pay attention to LOD effect, e.g. when using common OD, follow the following items (Figure 8.2.2.1.4.1): 1. Keep the same SA/SB 2. Enlarge OD to put two dummy gates at both side of OD with the same channel width, length, and pitch.			
AN.R.61mg ^U	For an analog matching pair, recommend to use the same ENDCAP size, even for the dummy poly (Figure 8.2.2.1.4.3)			
AN.R.65mg ^U	Recommend to use equivalent drain and source orientation. The total number of D/S and S/D orientations need to be matched. (Figure 8.2.2.1.4.4)			
AN.R.66mg ^U	Recommend to equalize interconnect and gate loading for matched transistors and to tap the gate connection from both ends. (Figure 8.2.2.1.4.5)			
AN.R.75mg ^U	If you use PO or dummy PO on STI to meet the spacing rule of the neighboring to LAST GATE on the matching pair, recommend that the width is equal to the MOS channel length			

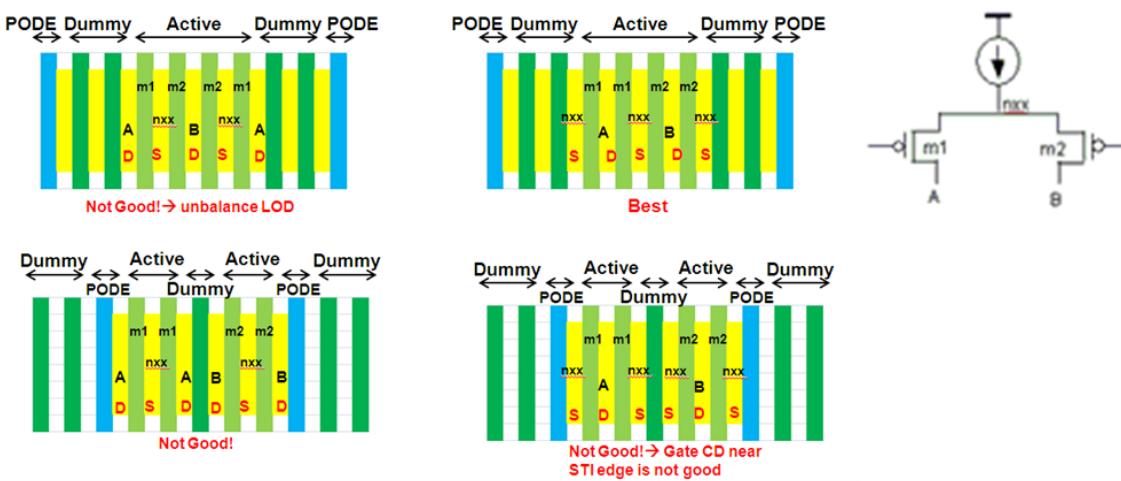


Figure 8.2.2.1.4.1 Example of dummy poly besides matching pairs

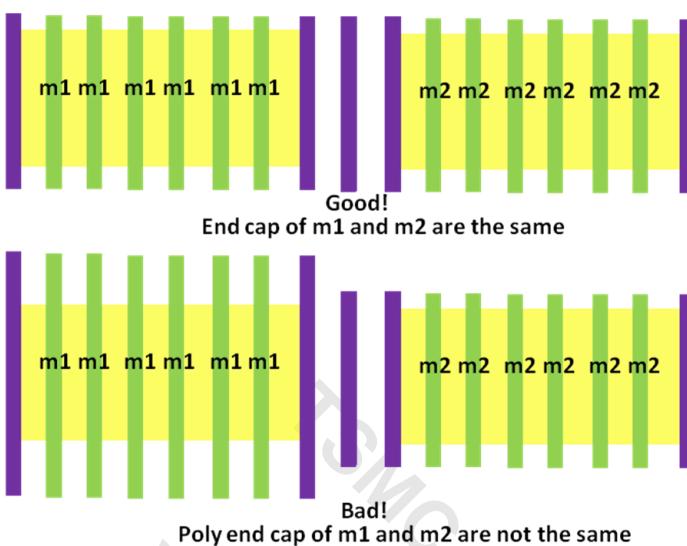


Figure 8.2.2.1.4.3 Example of same poly endcap size in the same OD

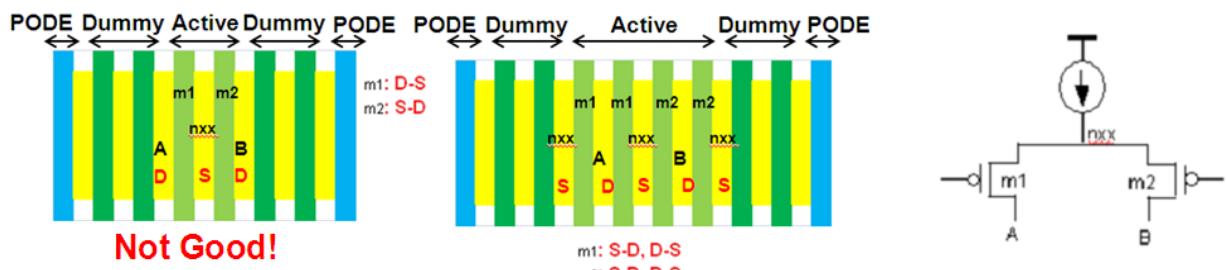


Figure 8.2.2.1.4.4 Example of equivalent drain and source orientation

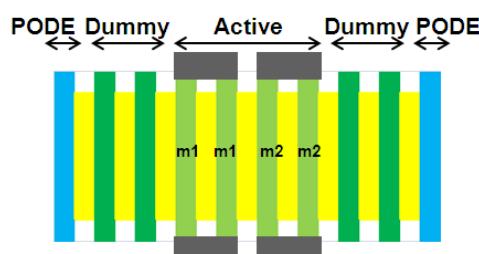


Figure 8.2.2.1.4.5 Example to tap the gate connection from both ends of the gate

Rule No.	Description	Label	Op.	Rule
AN.R.46mg ^U	<ol style="list-style-type: none"> 1. Make certain that the local pattern density of, and nearby, the matching pair are identical. Use enough dummy cells surrounding the matching pair is highly recommended. 2. Draw the dummy pattern manually and uniformly, surrounding the matching pair for both the source/drain direction and the ENDCAP direction. (Figure 8.2.2.1.4.6) <ul style="list-style-type: none"> • The dummy patterns should be identical in shape, dimension, space to the main circuit, and from the source/drain direction and the ENDCAP direction, respectively. • The dummy OD and dummy PO should be 100% cover the projection edge of the matching devices. 			
AN.R.8mg ^U	Place the matching pairs close together and, if possible, use "Symmetrical" or "inter-digitated" placement for better matching. For matching pair larger than 5 $\mu\text{m} \times 5 \mu\text{m}$, interdigitated placement is recommended to minimize the impact from unmatched surroundings			

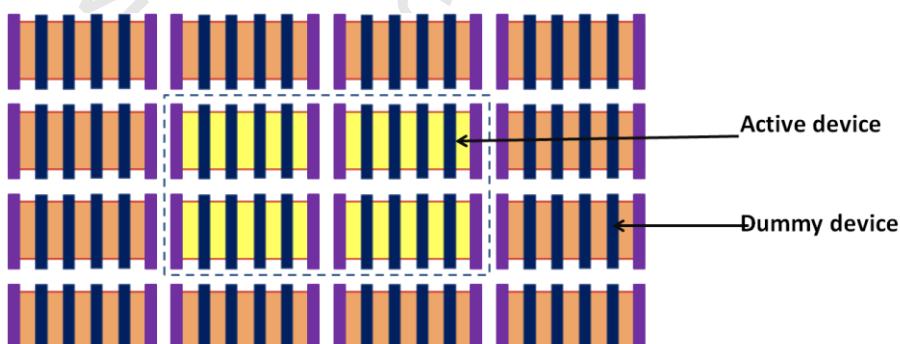
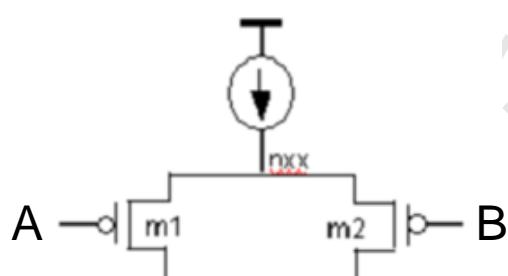


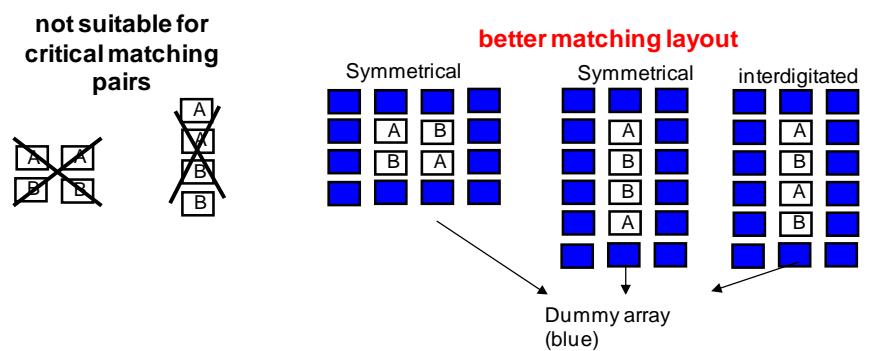
Figure 8.2.2.1.4.6

Dummy pattern for matching pairs

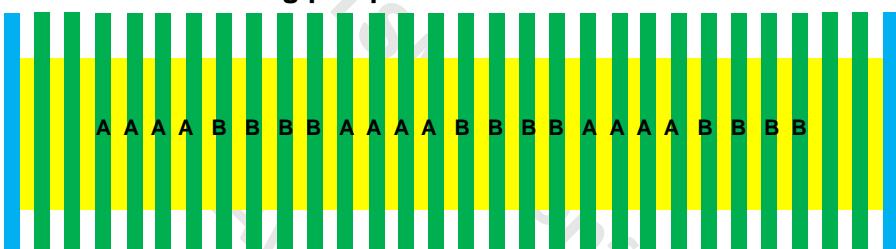
Matching Pair m1 and m2



Matching pair placement for separate OD

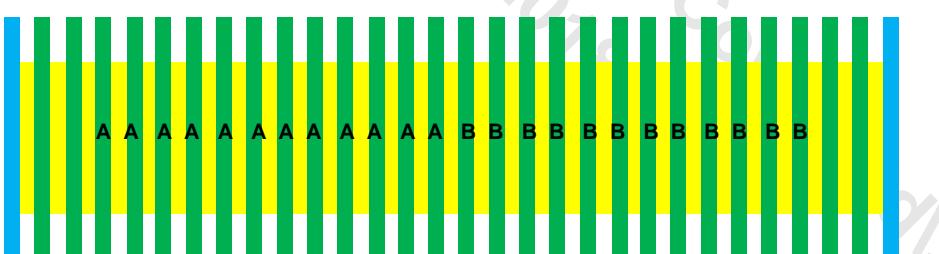


Matching pair placement for common OD



Interdigitated placement

Interdigitated placement
(Recommended for matching pair larger than 5 μmx5 μm)



Symmetric placement

Symmetric placement
(Not recommended for matching pair larger than 5 $\mu\text{m} \times 5 \mu\text{m}$, due to hard to control the symmetric surrounding)

Figure 8.2.2.1.4.7 Example of Symmetrical or inter-digitated layout for matching pairs

Rule No.	Description	Label	Op.	Rule
AN.R.9mg ^U	Regardless of any device dimensions of matching pairs with consistent resistance concerns, use the symmetrical number of VC, same MD overlapping on OD, and the same MG shape, VC to GATE space. The layout of interconnection routing should be symmetrical with respect to each branch.			
AN.R.12mg ^U	PO gate must connect to a protection diode by M1 to reduce the antenna effects on matching pairs.			
AN.R.67mg ^U	Recommend to match antenna diode and their metal routing. (Figure 8.2.2.1.4.8)			

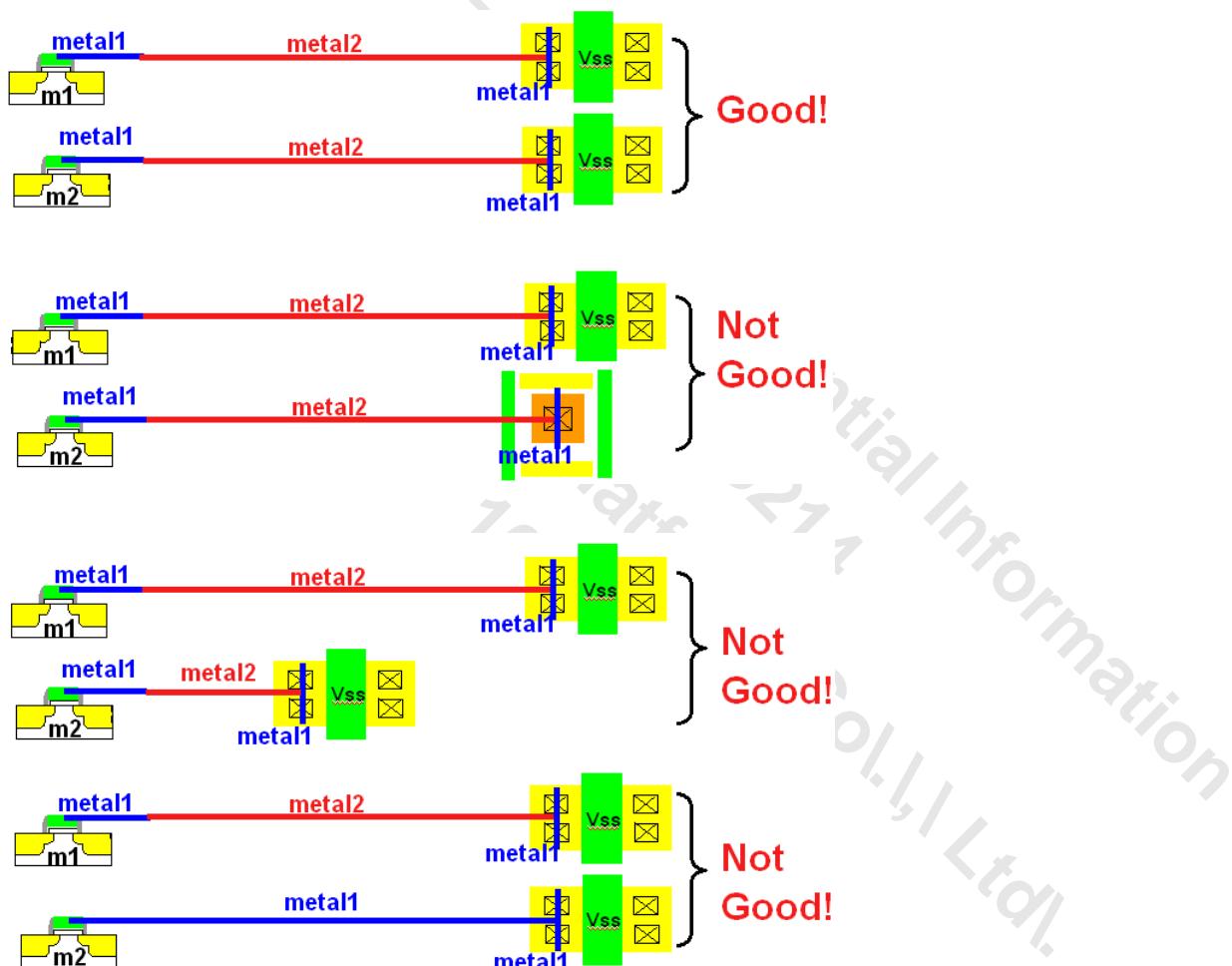
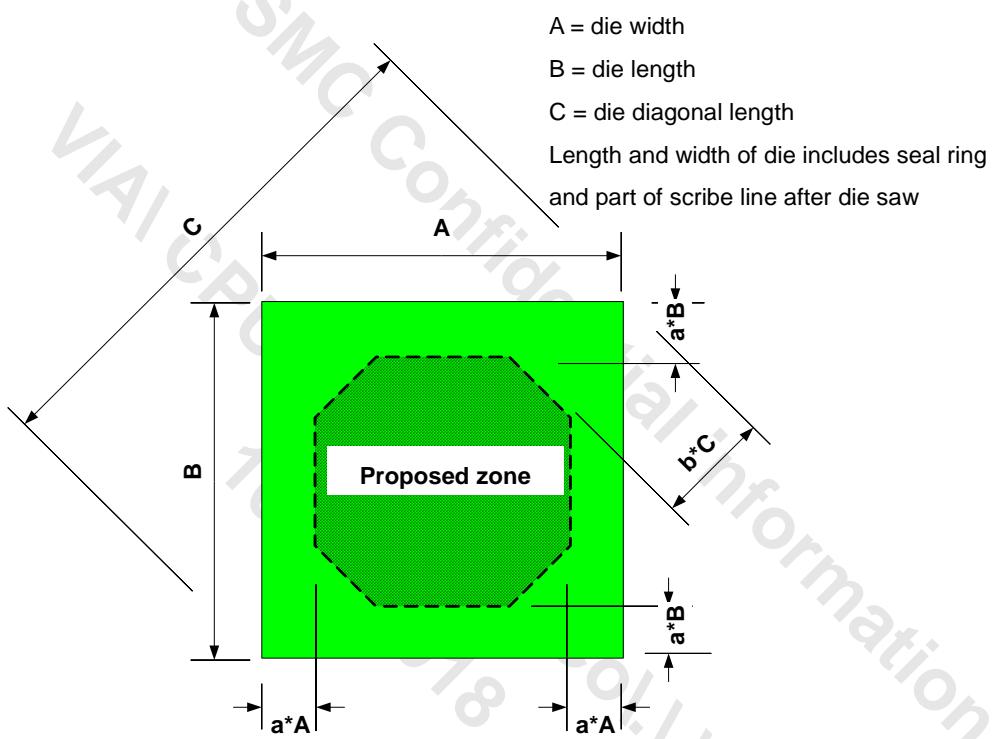


Figure 8.2.2.1.4.8 Example to match antenna diode and their metal routing

Rule No.	Description	Label	Op.	Rule
AN.R.13m ^U	Avoid placing the matching pairs or performance-critical devices at the Chip_Boundary corner and Chip_Boundary edge. (Figure 8.2.2.1.4.9)			
AN.R.21mg ^U	CB and CBD are not recommended to put on the top of matching pairs or performance-critical devices.			
AN.R.15mg ^U	Use the optimized VC number and the same VC to GATE space at both source and drain sides of performance-critical devices.			
AN.R.72mg ^U	For less device offset and variation in Id_analog (Ids at Vds = Vgs = 0.5*Vdd) of core device, recommend to use merged-OD than separate-ODs or use symmetrical layout style. (Figure 8.2.2.1.4.11)			



For the bottom die in a stacked-die wirebond PBGA package

- 1) a: away from die edge $\geq 10\%$ of the chip edge length
- 2) b: away from die corner $\geq 15\%$ of the chip diagonal dimension

For a single-die wirebond PBGA package

- 1) a: away from die edge $\geq 3\%$ of the chip edge length
- 2) b: away from die corner $\geq 5\%$ of the chip diagonal dimension

For a single-die flip chip PBGA package

- 1) a: away from die edge $\geq 1\%$ of the chip edge length
- 2) b: away from die corner $\geq 3\%$ of the chip diagonal dimension

The above numbers may be changed by several factors, e.g. die size, die thickness, package type, package material, package size, and circuit design margin, please contact TSMC for more details.

Figure 8.2.2.1.4.9 The proposed zone for matching pairs or performance-critical devices

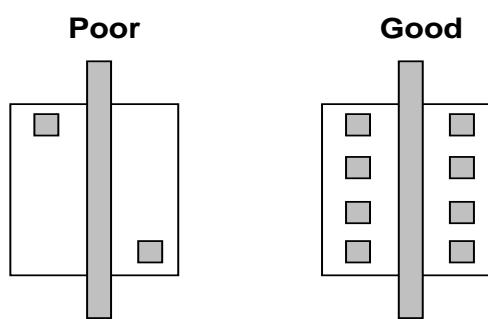


Figure 8.2.2.1.4.10
Adequate VC numbers at both source and drain sides of performance-critical devices.

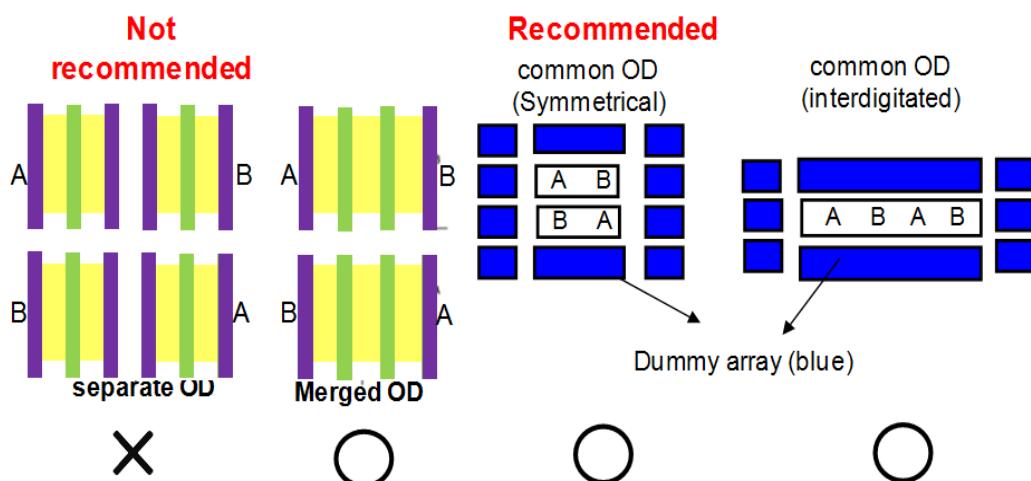


Figure 8.2.2.1.4.11 Example for common centroid, merged OD and separate OD.

8.2.2.1.5 DRC methodology for MOS Array

8.2.2.1.5.1 MOS array Dummy Layer

ANARRAY_H (CAD layer: 255;20), ANARRAY_M (CAD layer: 255;21), and ANARRAY_S (255;24) are DRC layers for checking surrounding environment with large, medium, and small matching MOS array, while ANARRAY_HS (CAD layer: 255;23) is used to identify edge cells and inner cells within a large MOS array when doing extraction. The MOS array will have higher variations in the edge cells comparing to the inner cells.

ANARRAY_HS (CAD layer: 255;23) is also used for high matching MOS array with only 5 μm identical dummy, because the surrounding environment effect will be covered in LPE simulation. The simulation result will have higher variation at the cells of the MOS array edges.

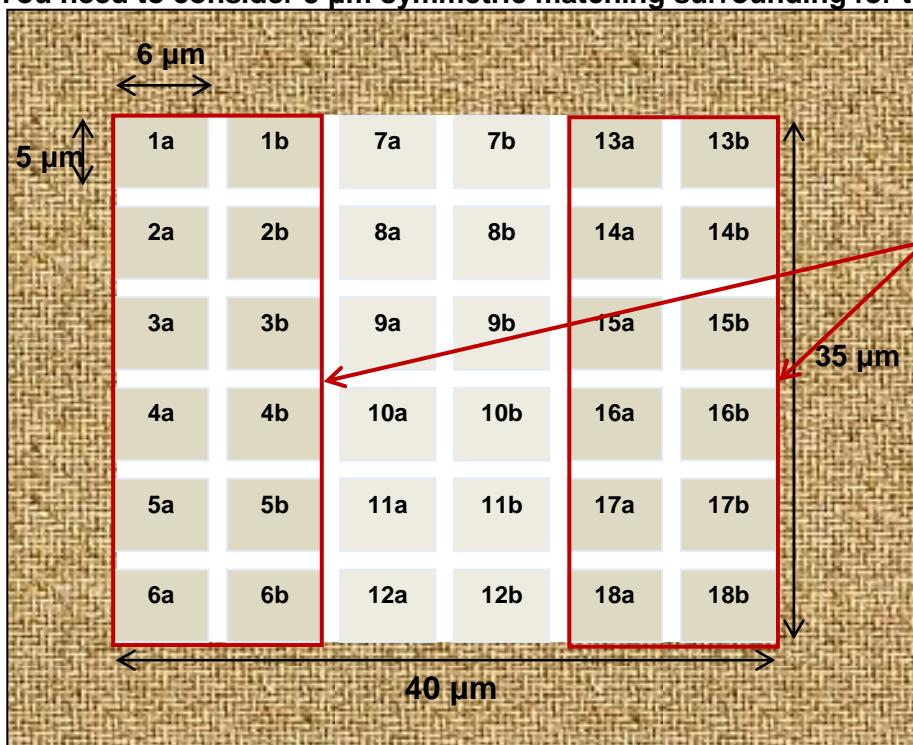


Drawing Guidance:

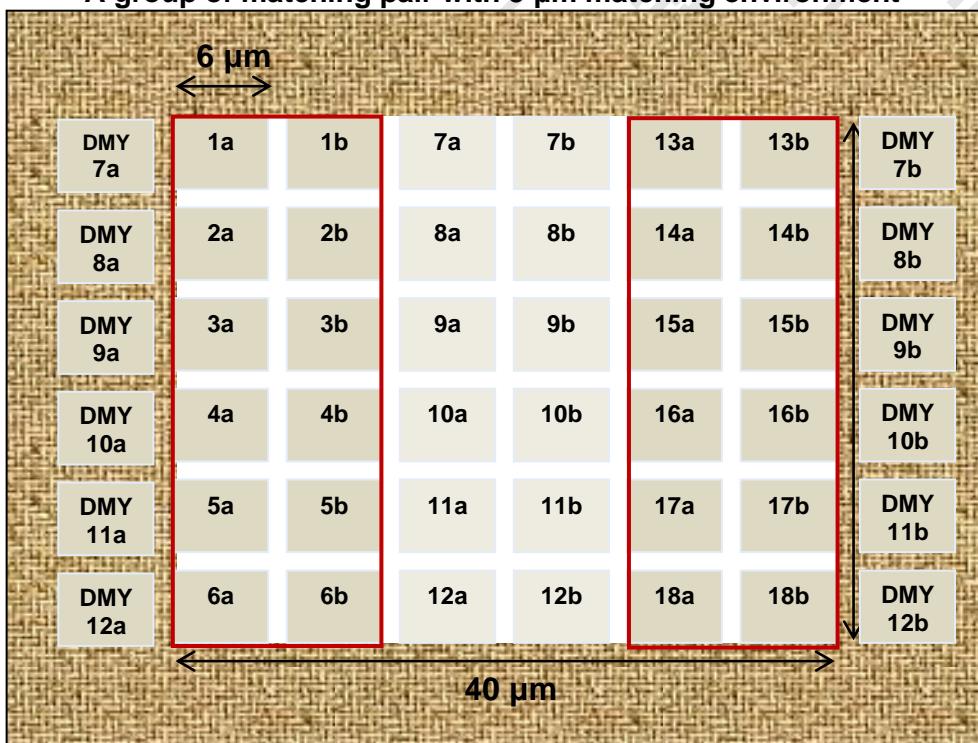
1. Analog MOS array must be covered by DRC CAD layer: ANARRAY_H (CAD layer: 255;20), ANARRAY_HS (CAD layer: 255;23), ANARRAY_M (CAD layer: 255;21) or ANARRAY_S (255;24) (CAD layer: 205;8) for large/ medium/ small matching requirement. The surrounding or identical dummy cells next to the MOS array cannot be covered by the DRC CAD layers mentioned above.
2. The DRC CAD layer boundary must be drawn exactly at the centerline between analog MOS array and dummy cells or at the centerline of well strap if well strap is placed between analog MOS array and dummy cells.
3. ANARRAY_HS are used for devices with $L_g \geq 0.072 \mu\text{m}$.
4. ANARRAY_M, ANARRAY_H, and ANARRAY_HS are in general used for the matching MOS array consisting of more than **three matching MOS devices**. However, if a group of matching pairs' size is greater than $5 \mu\text{m} \times 5 \mu\text{m}$ (smaller than $40 \mu\text{m} \times 40 \mu\text{m}$), the 5 μm surrounding should be carefully implemented as matching as possible.
5. For differential pair layout style, suggest to follow DRM 8.2.2.1

Example of an array with 18 matching pairs

You need to consider 5 μm symmetric matching surrounding for this array.



A group of matching pair with 5 μm matching environment



8.2.2.1.5.2 DRC methodology for AN.R.84m of High Matching MOS array

To define sensitive analog MOS array with High matching requirement (e.g. current DAC, ADC), please use ANARRAY_H (CAD layer:255;20) to mark the analog MOS array. It doesn't include the identical dummy devices.

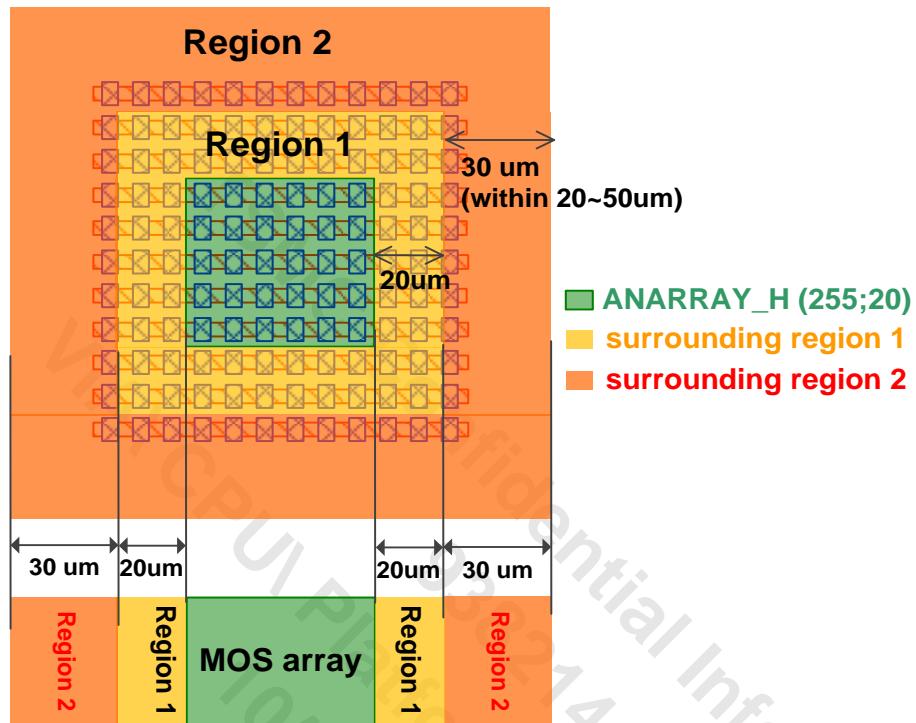


Figure 8.2.2.1.5.1

DRC methodology for AN.R.88.1mg of Medium Matching MOS array

To define sensitive analog MOS array with Medium matching requirement (e.g. Bandgap, OPAMP, and current mirror), please use ANARRAY_M (CAD layer:255;21) to mark the analog MOS array. It doesn't include the identical dummy devices. Please refer to Figure 8.2.2.1.5.2, shown as below,

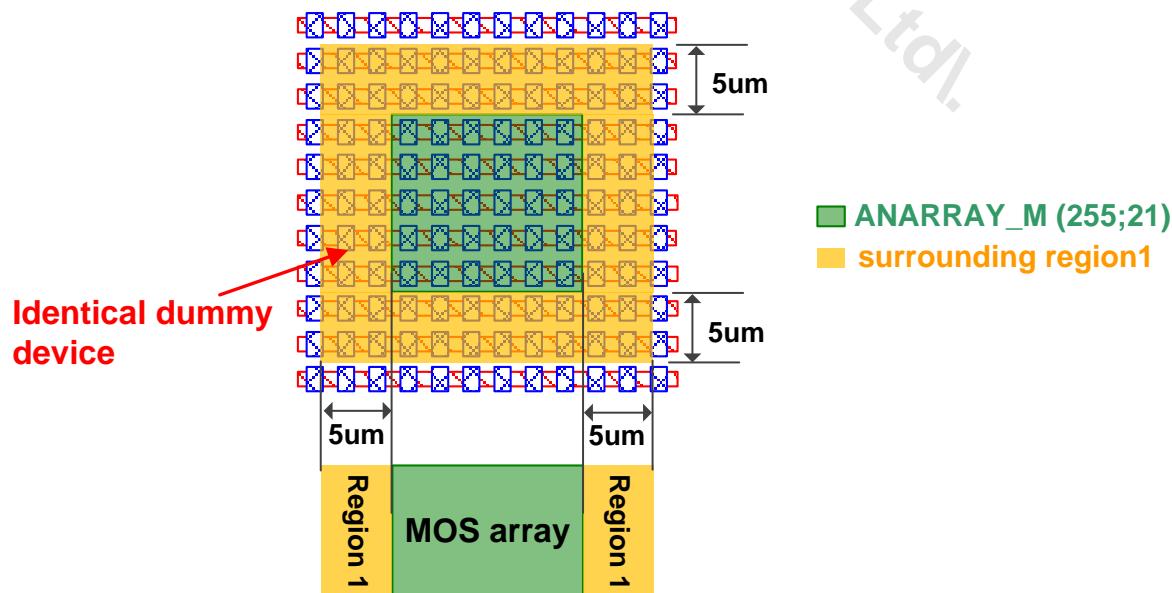
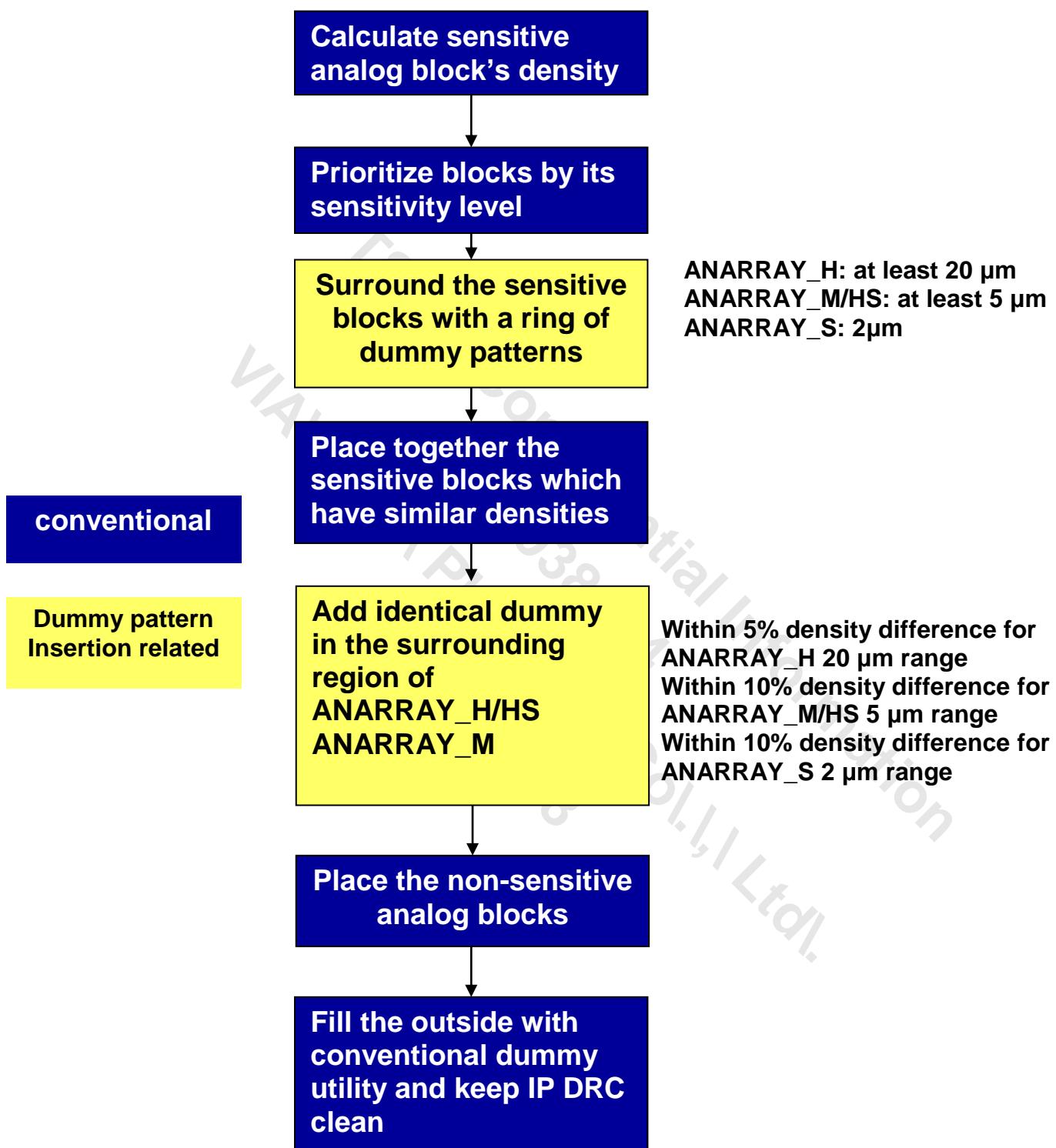


Figure 8.2.2.1.5.2

Dummy Pattern Insertion in Design Phase

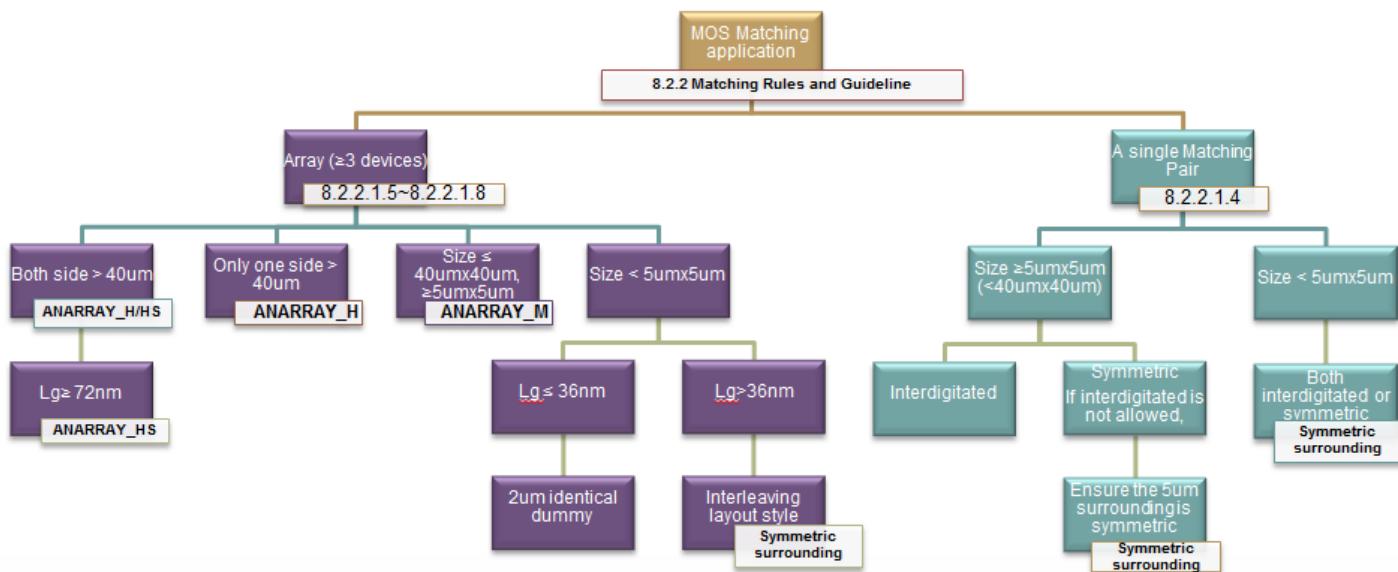


8.2.2.1.5.3 MOS array Matching Summary

Table 8.2.2.1.3

Array size	Dummy Layer	DRC check region	Layout Guidelines	Corresponding Rule
Matching pair (Array size refer to next page)	MATCHING (205;8)	Within MOS array	1. Recommend the width of STRAP \leq 1 μm 2. Recommend to put matching devices in the same OD, and fingers distributed uniformly in each OD inside DUT	AN.R.86.1mg AN.R.86.2mg ^U
$\leq 5 \mu\text{m} \times 5 \mu\text{m}$	ANARRAY_S (255;24)	Within MOS array	1. Recommend the width of STRAP \leq 1 μm 2. Recommend to put matching devices in the same OD, and fingers distributed uniformly in each OD inside DUT	AN.R.86.1mg AN.R.86.2mg ^U
		Region 1 ($\leq 2 \mu\text{m}$)	1. Recommend to fill identical MOS array dummy patterns with $\geq 2 \mu\text{m}$ surrounding width	AN.R.94.1mg
$\leq 40 \mu\text{m} \times 40 \mu\text{m}$	ANARRAY_M (255;21)	Within MOS array	1. Recommend the width of STRAP \leq 1 μm 2. Recommend to put matching devices in the same OD, and fingers distributed uniformly in each OD inside DUT	AN.R.86.1mg AN.R.86.2mg ^U
		Region 1 ($\leq 5 \mu\text{m}$)	1. Recommend to fill identical MOS array dummy patterns with $\geq 5 \mu\text{m}$ surrounding width	AN.R.88.1mg
		Within MOS array	1. Recommend the width of STRAP \leq 1 μm 2. Recommend to put matching devices in the same OD, and fingers distributed uniformly in each OD inside DUT	AN.R.86.1mg AN.R.86.2mg ^U
One side $> 40 \mu\text{m}$	ANARRAY_H (255;20)	Region 1 ($\leq 20 \mu\text{m}$)	1. Fill identical dummy with $\geq 20 \mu\text{m}$ surrounding width	AN.R.84m
		Region 2 (within 20~50 μm)	1. Recommend to fill surrounding patterns with uniform and symmetric OD/PO density in the outer ring for high-matching circuits	AN.R.87.3mg ^U
$>40 \mu\text{m} \times 40 \mu\text{m}$	ANARRAY_HS (255;23)	Within MOS array	1. Recommend the width of STRAP \leq 1 μm 2. Recommend to put matching devices in the same OD, and fingers distributed uniformly in each OD inside DUT	AN.R.86.1mg AN.R.86.2mg ^U

Array size	Dummy Layer	DRC check region	Layout Guidelines	Corresponding Rule
			Dimension of ANARRAY_HS must be $\geq 40 \mu\text{m} \times 40.001 \mu\text{m}$ or $\geq 40.001 \mu\text{m} \times 40 \mu\text{m}$ with MOS Gate Length $\geq 0.072 \mu\text{m}$. ANARRAY_HS must be rectangular	AN.R.84.1m
		Region 1 ($\leq 5 \mu\text{m}$)	Recommend to fill identical MOS array dummy patterns with $\geq 5 \mu\text{m}$ surrounding width	AN.R.84.2m



8.2.2.1.6 Normal matching

Rule No.	Description	Label	Op.	Rule
AN.R.86.0mg	In order to reduce the current mismatch for sensitive MOS arrays (inside ANARRAY_H or ANARRAY_HS or ANARRAY_M or ANARRAY_S or MATCHING), recommend to follow AN.R.86.1mg, AN.R.86.2mg ^U (Fig. 8.2.2.1.6.1) and AN.R.86.3mg ^U (Fig. 8.2.2.1.6.2) in MOS array			
AN.R.86.1mg	Recommended width of STRAP		\leq	1
AN.R.86.2mg ^U	Recommend to put matching devices in the same OD, and distribute fingers uniformly in each OD inside DUT			
AN.R.86.3mg ^U	Recommend to place multi-finger matching pairs by interleaving arrangement to minimize AP coverage effect			
AN.R.91m	MATCHING, ANARRAY_H, ANARRAY_HS, ANARRAY_S, and ANARRAY_M cannot overlap each other			
AN.R.92m	ANARRAY_H enclosure by Chip_Boundary in chip level		\geq	20
AN.R.93m®	Recommended ANARRAY_M enclosure by Chip_Boundary in chip level		\geq	5
MATCH.WARN.1	<p>Warning: It is important to cover MATCHING (205;8), ANARRAY_H (255;20), ANARRAY_M (255;21), ANARRAY_S (255;24), or ANARRAY_HS (255;23) for each MOS array of the matching circuit. Otherwise, the related rules (PO.DN.6 and PO.R.18) or MOS array matching rules will not be checked.</p> <p>Mismatch degradation will occur if PO.DN.6, PO.R.18 and MOS array matching rules are violated.</p> <p>If there is no matching circuit in the chip, this warning can be bypassed.</p> <p>DRC only flags this error message in chip level.</p>			

- Usage of MATCHING(205;8)

1. MATCHING cad layer didn't consider different surrounding environment effect. MATCHING is not recommended to use for array size > 5 μm x 5 μm.

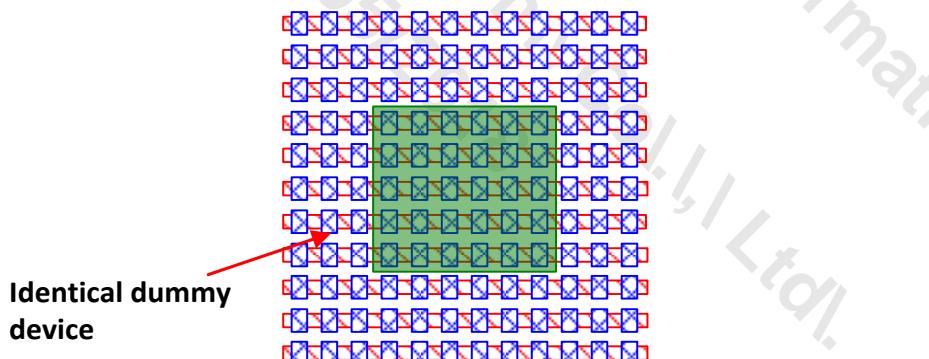
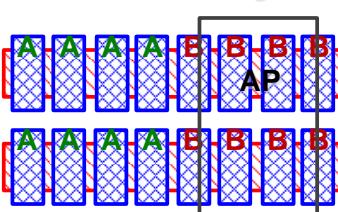


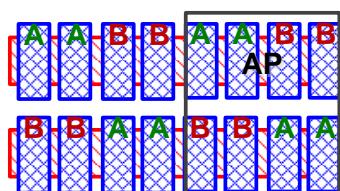
Figure 8.2.2.1.6.1

Bad Layout:
Multiple finger matching pair without interleaving arrangement



Note: A v.s B is matching pair

Good Layout:
Multiple finger matching pair with interleaving arrangement in vertical and horizontal direction



Same finger number of A and B devices under the AP layer

Figure 8.2.2.1.6.2

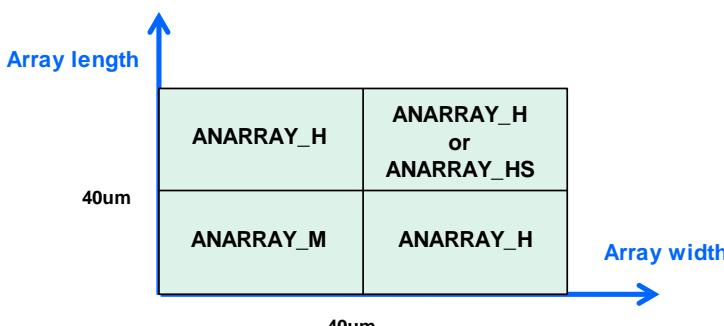
8.2.2.1.7 High matching

8.2.2.1.7.1 High matching with 20 μm identical surrounding patterns

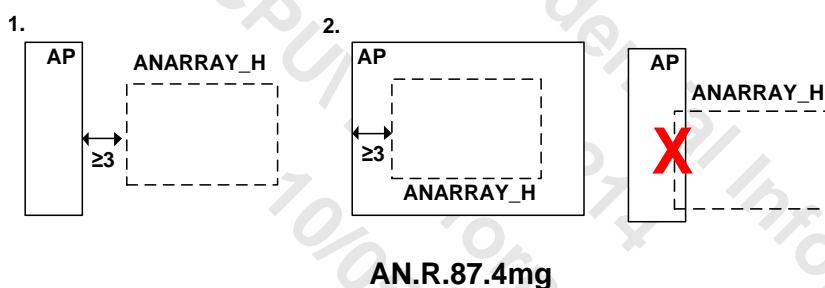
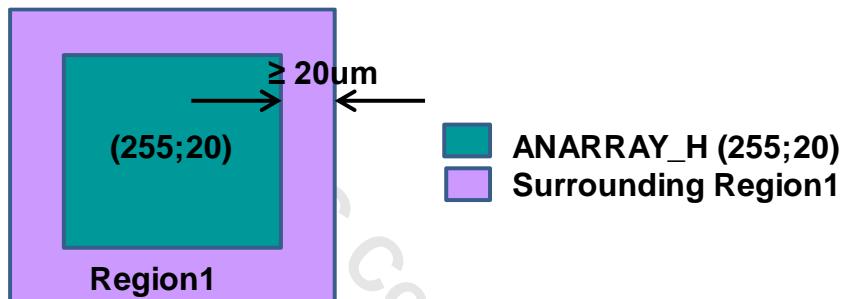
Rule No.	Description	Label	Op.	Rule
AN.R.87.0mg	In order to reduce the current mismatch for high matching MOS arrays, MOS array must either be inside ANARRAY_H to follow AN.R.84m, and recommend to follow AN.R.87.3mg ^U or be inside ANARRAY_HS to follow AN.R.84.1m and AN.R.84.2m.			
AN.R.84m	<p>Surrounding width of identical dummy MOS neighboring to the highly mismatch sensitive MOS array (e.g. current mirror, DAC) in order to reduce the gap between Si and simulation.</p> <p>Mismatch sensitive MOS array: e.g. $V_{gs} - V_{th_gm} < 350 \text{ mV}$. Covered by ANARRAY_H* (255;20).</p> <p>Identical dummy MOS: Dimension difference between dummy MOS and highly mismatch sensitive MOS array within +/-3%. The same is better.</p> <p>Auxiliary definitions: DRC flags density difference > 5% between inner ring-1 & outer ring-1 and between inner ring-2 & outer ring-2 for the following layers: OD, PO, NW, DNW, PP, NP, OD_18, VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P, MD, MP, VC, M0</p> <p>Inner ring-1: {ANARRAY_H NOT {ANARRAY_H SIZING -10 μm}} Outer ring-1: {{ANARRAY_H SIZING 10 μm} NOT ANARRAY_H} Inner ring-2: {ANARRAY_H NOT {ANARRAY_H SIZING -20 μm}} Outer ring-2: {{ANARRAY_H SIZING 20 μm} NOT ANARRAY_H} (Figure 8.2.2.1.7.1)</p>		\geq	20
AN.R.87.3mg ^U	For within 20~50 μm surrounding range around ANARRAY_H, fill surrounding patterns with uniform and symmetric OD/PO density in the outer ring for high-matching circuits (Figure 8.2.2.1.7.2)			
AN.R.87.4mg	<p>In order to reduce the current mismatch of MOS array, recommend to follow one of the following conditions:</p> <ol style="list-style-type: none"> 1. ANARRAY_H space to AP (CUT is not allowed) $\geq 3 \mu\text{m}$, or 2. ANARRAY_H enclosure by AP $\geq 3 \mu\text{m}$ <p>Warning: If violated AN.R.87.4mg, > 2X current mean shift will occur by comparing with 1-sigma of device mismatch within a MOS array.</p>			

- Usage of ANARRAY_H (255;20)

2. ANARRAY_H must be rectangular and the array size must follow the table/figure below.

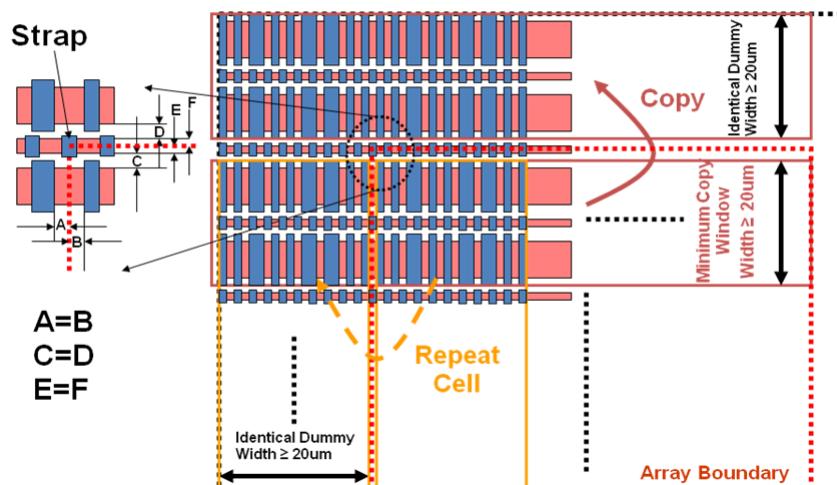


3. OD, PO density gradient $\leq 5\%$ for checking window $10 \mu\text{m} \times 10 \mu\text{m}$ stepping $5 \mu\text{m}$
4. Only allow to place one type device as shown in section 3.5 "Device truth table". For example, all devices within one ANARRAY_H must be nch_svt_mac or pch_svt_mac. It is not allowed to place both nch_svt_mac and pch_svt_mac in the same ANARRAY_H. Different Vt or Tox is also not allowed to be put in the same ANARRAY_H.
5. Creating surrounding dummy patterns by repeating unit cell of analog MOS array (refer to Figure 8.2.2.1.7.1)
6. Following the layout guideline of ANARRAY_H (CAD layer:255;20) in section 8.2.2.3.3.



Layout example for identical dummy

Identical Dummy Definition (Pattern 1)



Identical Dummy Definition (Pattern 2)

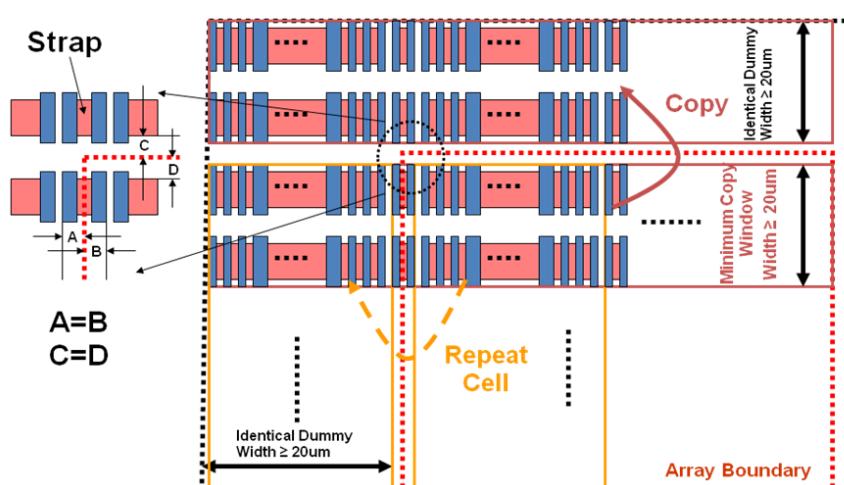


Figure 8.2.2.1.7.1

Uniform and symmetric OD/PO

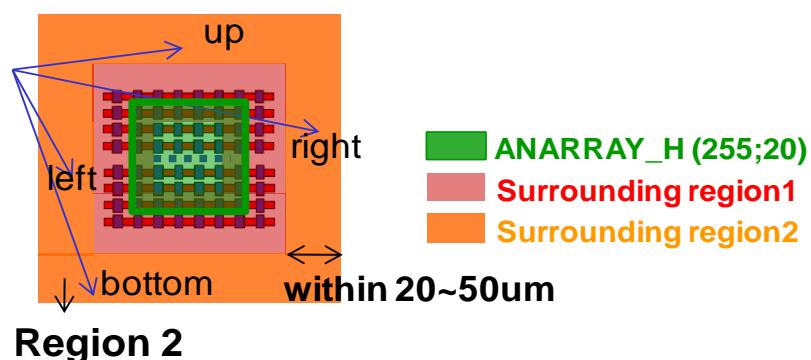


Figure 8.2.2.1.7.2

8.2.2.1.7.2 High matching with 5 μm identical surrounding patterns

Rule No.	Description	Label	Op.	Rule
AN.R.84.1m	Dimension of ANARRAY_HS must be $\geq 40 \mu\text{m} \times 40.001 \mu\text{m}$ or $\geq 40.001 \mu\text{m} \times 40 \mu\text{m}$ with MOS Gate Length $\geq 0.072 \mu\text{m}$. ANARRAY_HS must be rectangular.			
AN.R.84.2m	<p>Surrounding width of identical dummy MOS neighboring to highly mismatch sensitive MOS array (e.g. current mirror, DAC) with ANARRAY_HS to reduce the gap between Si and simulation.</p> <p>Identical dummy MOS: Dimension difference between dummy MOS and mismatch sensitive MOS array within $+/-3\%$. The same is better.</p> <p>Auxiliary definitions: DRC flags density difference $> 10\%$ between inner ring-1 and outer ring-1 for the following layers. OD, PO, NW, DNW, PP, NP, OD_18, VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P, MD, MP, VC, M0</p> <p>Inner ring-1: {ANARRAY_HS NOT {ANARRAY_HS SIZING -5 μm}} Outer ring-1: {{ANARRAY_HS SIZING 5 μm} NOT ANARRAY_HS}</p>		\geq	5
AN.R.84.3mg	<p>In order to reduce the current mismatch of MOS array, recommend to follow one of the following conditions:</p> <ol style="list-style-type: none"> 1. ANARRAY_HS space to AP (CUT is not allowed) $\geq 3 \mu\text{m}$, or 2. ANARRAY_HS enclosure by AP $\geq 3 \mu\text{m}$ <p>Warning: If violate AN.R.84.3mg, $> 2X$ current mean shift will occur by comparing with 1-sigma of device mismatch within a MOS array.</p>			

● Usage of ANARRAY_HS (255;23)

1. Dimension of ANARRAY_HS must be $\geq 40 \mu\text{m} \times 40.001 \mu\text{m}$ or $\geq 40.001 \mu\text{m} \times 40 \mu\text{m}$ and ANARRAY_HS must be rectangular with MOS gate length $\geq 0.072 \mu\text{m}$
2. ANARRAY_HS is used for highly mismatch sensitive array. Eg. $V_{gs}-V_{th_gm} < 350\text{mV}$.
3. Only allow to place one type of device as shown in section 3.5 "Device truth table". For example, all devices within one ANARRAY_HS must be nch_svt_mac or pch_svt_mac. It is not allowed to place both nch_svt_mac and pch_svt_mac in the same ANARRAY_HS. Different V_t or Tox is also not allowed to be put in the same ANARRAY_HS.

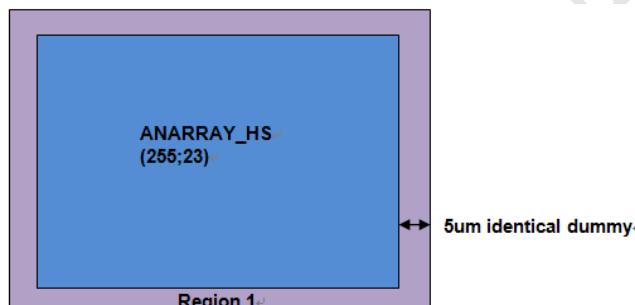
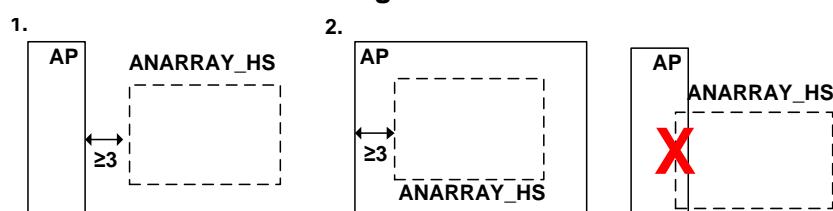


Figure 8.2.2.1.7.3



AN.R.84.3mg

8.2.2.1.8 Medium matching

Rule No.	Description	Label	Op.	Rule
AN.R.88.0mg	In order to reduce the current mismatch for medium matching MOS arrays (inside ANARRAY_M, eg. Bandgap), recommend to follow AN.R.88.1mg			
AN.R.88.1mg	<p>Recommended surrounding width of identical dummy MOS neighboring to median mismatch sensitive MOS array (Figure 8.2.2.1.8.1)</p> <p>Mismatch sensitive MOS array: e.g. $V_{gs} - V_{th_gm} < 350$ mV. Covered by ANARRAY_M (255;21).</p> <p>Identical dummy MOS: Dimension difference between dummy MOS and median mismatch sensitive MOS array within $+/-3\%$. The same is better.</p> <p>Auxiliary definitions: DRC flags density difference $> 10\%$ between inner ring-1 and outer ring-1 for the following layers. OD, PO, NW, DNW, PP, NP, OD_18, VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P, MD, MP, VC, M0</p> <p>Inner ring-1: {ANARRAY_M NOT {ANARRAY_M SIZING -5 μm}}</p> <p>Outer ring-1: {{ANARRAY_M SIZING 5 μm} NOT ANARRAY_M}</p>		\geq	5
AN.R.88.2mg	<p>In order to reduce the current mismatch of MOS array, recommend to follow one of the following conditions:</p> <ol style="list-style-type: none"> 1. ANARRAY_M space to AP (CUT is not allowed) $\geq 3 \mu$m, or 2. ANARRAY_M enclosure by AP $\geq 3 \mu$m <p>Warning: If violate AN.R.88.2mg, $> 2X$ current mean shift will occur by comparing with 1-sigma of device mismatch within a MOS array.</p>			

- Usage of ANARRAY_M (255;21)

1. ANARRAY_M must be rectangular and the dimension of ANARRAY_M must be $\leq 40 \mu$ m \times 40μ m.
2. OD, PO density gradient $\leq 5\%$ for checking window 10μ m \times 10μ m stepping 5μ m.
3. Only allow to place one type of device as shown in section 3.5 “Device truth table”. For example, all devices within one ANARRAY_M must be nch_svt_mac or pch_svt_mac. It is not allowed to place both nch_svt_mac and pch_svt_mac in the same ANARRAY_M. Different Vt or Tox is also not allowed to be put in the same ANARRAY_M.
4. Creating surrounding dummy patterns by repeating unit cell of analog MOS array (refer to Figure 8.2.2.1.7.1)
5. Follow the layout guideline of ANARRAY_M (CAD layer:255;21) in section 8.2.2.1.8.

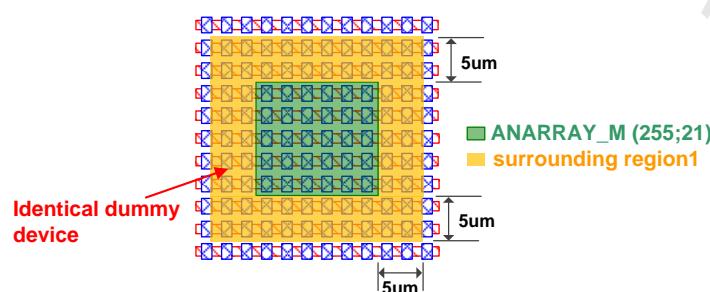
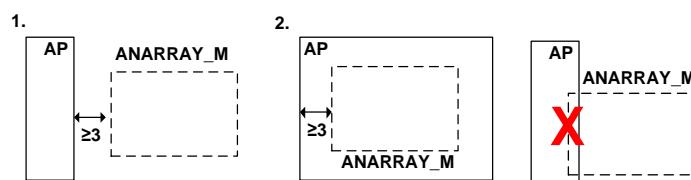


Figure 8.2.2.1.8.1



AN.R.88.2mg

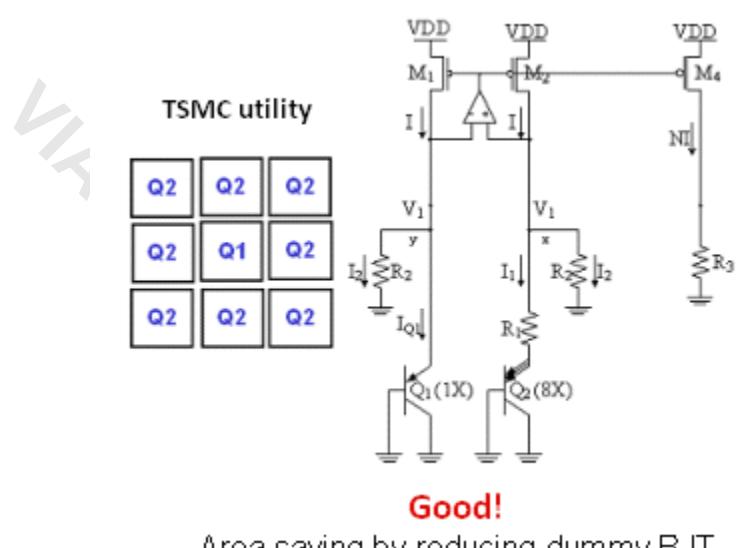
8.2.2.1.9 Small matching

Rule No.	Description	Label	Op.	Rule
AN.R.94.0mg	In order to reduce the current mismatch for small matching MOS arrays (inside ANARRAY_S), recommend to follow AN.R.94.1mg			
AN.R.94.1mg	<p>Recommended surrounding width of identical dummy MOS neighboring to small sensitive MOS array with $L_g \leq 0.036 \mu m$ (Figure 8.2.2.1.8.1)</p> <p>Mismatch sensitive MOS array: e.g. $V_{gs} - V_{th_gm} < 350 \text{ mV}$. Covered by ANARRAY_S (255;24).</p> <p>Identical dummy MOS: Dimension difference between dummy MOS and small sensitive MOS array within +/- 3%. The same is better.</p> <p>Auxiliary definitions: DRC flags density difference > 10% between inner ring-1 and outer ring-1 for the following layers. OD, PO, NW, DNW, PP, NP, OD_18, VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P, MD, MP, VC, M0</p> <p>Inner ring-1: {ANARRAY_S NOT {ANARRAY_S SIZING -2 μm}} Outer ring-1: {{ANARRAY_S SIZING 2 μm} NOT ANARRAY_S}</p>		\geq	2
AN.R.94.2mg	<p>In order to reduce the current mismatch of MOS array, recommend to follow one of the following conditions:</p> <p>ANARRAY_S space to AP (CUT is not allowed) $\geq 3 \mu m$, or ANARRAY_S enclosure by AP $\geq 3 \mu m$</p> <p>Warning: If violate AN.R.94.2mg, > 2X current mean shift will occur by comparing with 1-sigma of device mismatch within a MOS array.</p>			

- Usage of ANARRAY_S (255;24)
 1. ANARRAY_S must be rectangular and the dimension of ANARRAY_S must be $\leq 5 \mu m \times 5 \mu m$.
 2. Only allow to place one type of device as shown in section 3.5 “Device truth table”. For example, all devices within one ANARRAY_S must be nch_svt_mac or pch_svt_mac. It is not allowed to place both nch_svt_mac and pch_svt_mac in the same ANARRAY_S. Different Vt or Tox is also not allowed to be put in the same ANARRAY_S.
 3. Creating surrounding dummy patterns by repeating unit cell of analog MOS array (refer to Figure 8.2.2.1.7.1)

8.2.3 Bipolar Transistor (BJT) Rules and Recommendations

Rule No.	Description	Label	Op.	Rule
AN.R.69mg ^U	Recommend to use common central layout for BJT diodes and surrounding dummy pattern by tsmc utility (Figure 8.2.3.1)			
AN.R.70mg ^U	Recommend current density range of Low mismatch BJT from 100nA/ μm^2 to 10uA/ μm^2			



Area saving by reducing dummy BJT

Figure 8.2.3.1 Example of common central layout for BJT diodes

8.2.4 Bipolar Transistor (IBJT) Rules and Recommendations

1. Two kinds of vertical bipolar are provided, PNP bipolar (P+/NW/PSUB) and NPN bipolar (N+/PW/DNW).
2. SPICE and PDK offer 2 kinds of emitter size and base size:

	PNP_i1 and NPN_i1	PNP_i2 and NPN_i2
Emitter size	0.428 x 3.686	0.856 x 3.686

3. In order to have precise SPICE model prediction, it is strongly recommended that users should apply the standard TSMC bipolar layouts in their designs.
4. The entire device needs to be covered with IBJTD MY (CAD layer: 110;3) which is used for DRC and LVS check.
5. The entire Emitter needs to be covered with BJTED MY (CAD layer: 110;2) which is used for DRC and LVS check.

Rule No.	Description	Label	Op.	Rule
IBJT.W.1	Width of Base OD in vertical direction	W1	=	0.0680
IBJT.W.1.1	Width of Collector OD in vertical direction	W1A	=	0.0680
IBJT.W.3	Width of ALL_PO in IBJTD MY	W3	=	0.0860
IBJT.S.1	Space of Collector OD to Base OD in vertical direction	S1	=	0.3520, 0.9820
IBJT.S.1.1	Space of either one horizontal edge of Emitter OD to Base OD in vertical direction	S1A	=	0.2020
IBJT.S.3	Space of Collector OD [PRL > 0 μm] between different unit in same IBJTD MY	S3	=	0.8000 ~ 1
IBJT.EN.1	IBJTD MY enclosure of Collector OD	EN1	=	0.5000 ~ 1
IBJT.EN.2	Enclosure of ALL_PO	EN2	≥	0.0350
IBJT.R.2	Overlap VTUL_N, VTUL_P, VTL_N, VTL_P, VTS_N, VTS_P, VAR, or SRM (50;0) is not allowed			
IBJT.R.3	BJTED MY (110;2) must be inside IBJTD MY (110;3)			
IBJT.R.4	IBJTD MY(110;3) must be inside OD2			
IBJT.R.6	PO on Emitter OD must connect to Base OD			

8.2.5 MOS Capacitor and Varactor

Rule No.	Description	Label	Op.	Rule
AN.R.36mg ^U	It is recommended not to use a very long channel device in the design. In order to ensure the channel relaxation time of the MOS capacitor (excluding varactor) is enough to build up charge to steady state, it is recommended to use proper channel length at the high operation frequency range. The operating frequency shall be below $0.2 * gm / Cgate$, where gm is the transconductance of the transistor and Cgate is the gate-oxide capacitance.			
AN.R.37mg ^U	Varactor (NMOS capacitor in NW) is the best choice as MOS capacitor. The NW should have a P-type guard ring tied to ground.			
AN.R.20mg	Use thick oxide (OD_18) MOS varactor and capacitor to reduce gate oxide leakage. DRC cannot check capacitor.			
AN.R.52mg ^U	Recommend the following items for MOS capacitor matching (Figure 8.2.5.1) <ul style="list-style-type: none"> - Small identical geometry - Dummy capacitor - No on-top metal routing - Away from power source 			
AN.R.74mg ^U	Recommend the following items for varactor matching (Figure 8.2.5.2) <ul style="list-style-type: none"> - Use I/O varactor - Interdigital unit cell layout - Dummy varactor cell - Away from different power domain 			

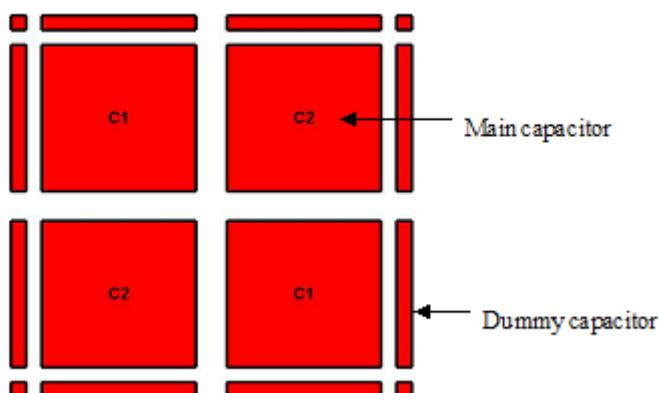


Figure 8.2.5.1 Example of capacitor matching

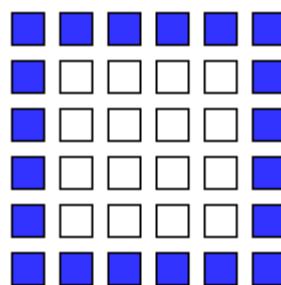


Figure 8.2.5.2 Example of Varactor matching

8.2.6 RF Varactor Guidelines

Rule No.	Description	Label	Op.	Rule
AN.R.106mg ^U	<p>It is recommended to use two varactors in parallel for adjusting C-V curve of MOS varactor. The additional port (G₁ or G₂, and S/D_{_1} or S/D_{_2}) makes the design more flexible, and the C-V curve can be adjusted by additional port (Figure 8.2.6.1). The two varactors in parallel achieve lower sensitivity and KVCO. (Figure 8.2.6.2) The total capacitance ($C_{\text{total}}(V)$) is $C_1(V) + (C_2(V)/C_p)$, where $C_1(V)$ and $C_2(V)$ are the capacitance of two varactors, and C_p is the dc block capacitor between G₁ and G₂ or S/D_{_1} or S/D_{_2}.</p>			
AN.R.107mg ^U	<p>It is recommended to use multi-gate varactor as switched capacitors array for saving chip area. $C_1(V)$ and $C_2(V)$ are the fine tuning capacitors, and $C_3(V)$, $C_4(V)$, $C_5(V)$, and $C_6(V)$ are the coarse tuning capacitors as the switched capacitor bank. The bit number and capacitance ratio between $C_3(V)$, $C_4(V)$ and $C_5(V)$, $C_6(V)$ are customized by the demand. (Figure 8.6.5.3) Figure 8.2.5.3 and 8.2.5.4 are an 2-bits example and $C_5(V)$ and $C_6(V)$ are twice of $C_3(V)$ and $C_4(V)$.</p>			

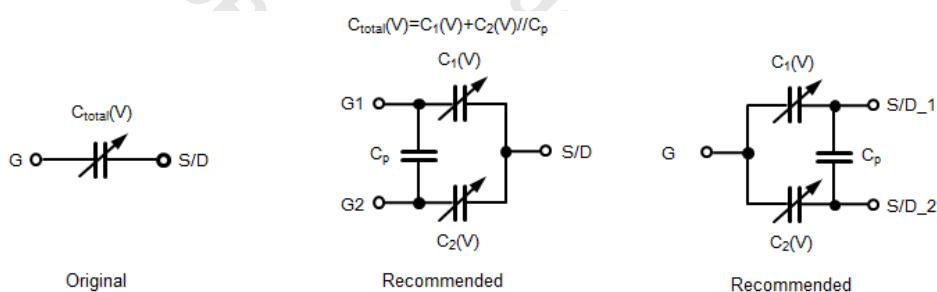


Figure 8.2.6.1

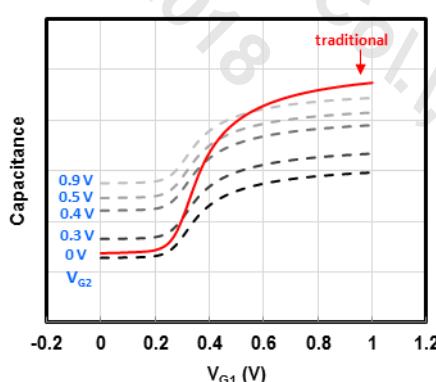


Figure 8.2.6.2

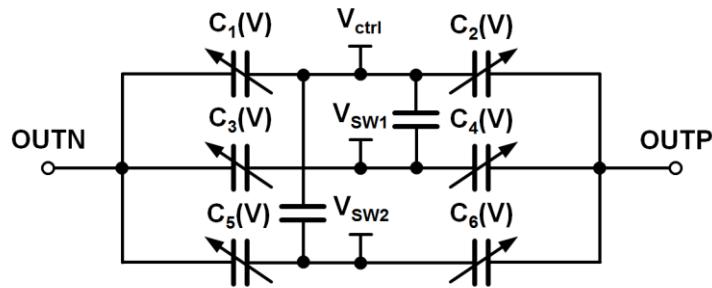


Figure 8.2.6.3

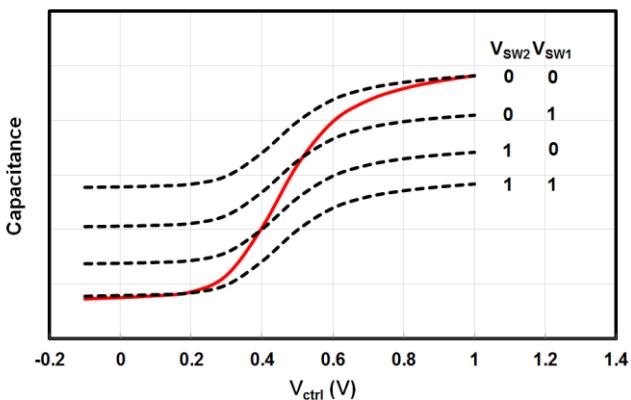


Figure 8.2.6.4

8.2.7 MoM Guidelines

Rule No.	Description	Label	Op.	Rule
AN.R.54mg ^U	Recommend the following items for MOM matching (Figure 8. 2.7.1) <ul style="list-style-type: none"> - Uniform metal density - Dummy MOM - Away from different power domain - Need to take care of RC extraction carefully during IP placement - Use MOM mismatch pair as close as possible - Neighboring metal density 30~50% in 200 μm x 200 μm area 			
AN.R.89mg ^U	Common-centroid pattern is not recommended for the large MOM array. It is recommended to draw a large MOM array with hybrid layout (the combination of parallel and MX (Multi-cross) types) by splitting capacitor elements equally into a number of sub-arrays. Each sub-array is recommended containing ≤ 32 and ≤ 8 unit cells for 8-bit and 10-bit resolution, respectively. (Fig. 8.2.7.2)			
AN.R.90mg ^U	It is recommended to add identical dummy MOM unit surrounding the MOM array for better matching.			
AN.R.108mg ^U	Recommend to shorten the center distance of the MoM matching pairs. (Fig 8.2.7.4)			

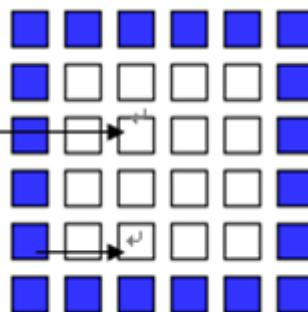


Figure 8.2.7.1 Example of MOM matching

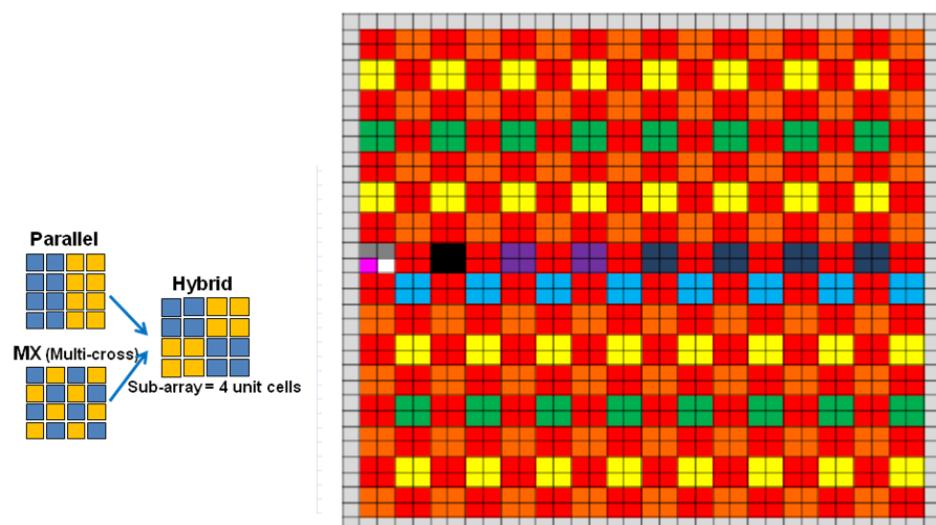


Figure 8.2.7.2

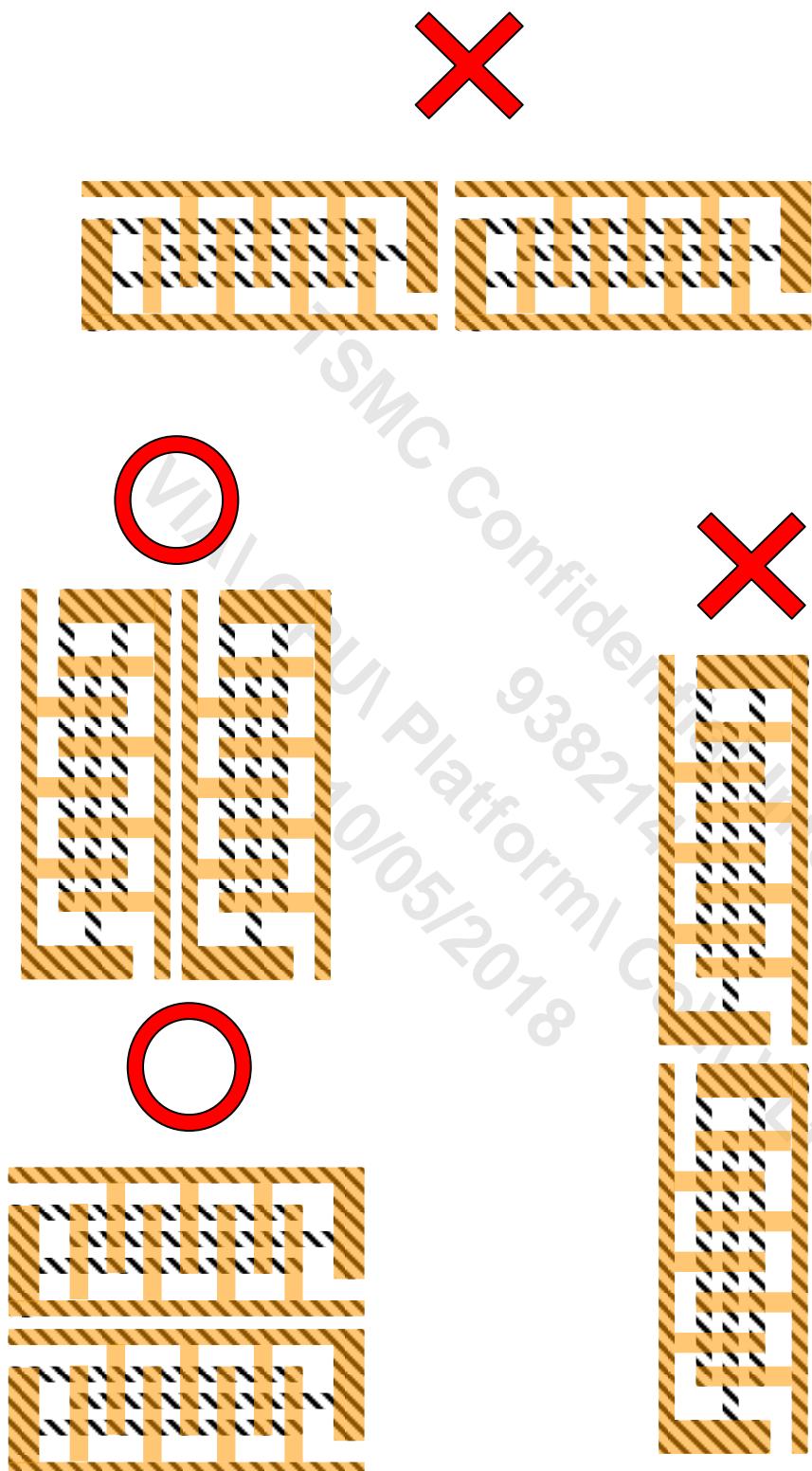


Figure 8.2.7.4

8.2.8 Hi-R Guidelines

Rule No.	Description	Label	Op.	Rule
AN.R.53mg ^U	<p>1. Pay attention on the matching topology of the resistor layout (Figure 8.2.2.4.1)</p> <ul style="list-style-type: none"> - Recommend the following items for resistor matching\Interdigital configuration - Equal structure - Suitable dimension - Dummy pattern - Away from different power source 			
AN.R.99mg ^U	For high-matching resistor array applications (e.g. bandgap, 8-bit R-DAC), recommend to place SR_DTN with identical width and square number ($\text{length}/\text{width} \geq 1$) to surround high R resistor array in length direction.			
AN.R.101mg ^U	<p>For high-speed circuit applications, resistor width $1.8 \mu\text{m}$ with square number ($\text{length}/\text{width} \geq 0.2$) can be adopted to have better EM capability and smaller parasitic capacitance.</p> <p>The warning from RH_TN.R.1 (square number ≥ 1) can be removed by adding RHDMY(117;4).</p>			
AN.R.101.1mg ^U	For resistance matching between two Hi-R arrays, recommend to keep arrays with the same pattern (density) for better matching			
AN.R.102mg ^U	<p>For matching high R resistor arrays, recommend to keep array-to-array distance $\leq 1000 \mu\text{m}$</p> <p>DRC checks resistor to resistor distance in the enclosed area of RH_MATCHING (117;20).</p>			
AN.R.102.1mg	RH_MATCHING (117;20) must be a rectangle orthogonal to grid			
AN.R.102m	Width and length of RH_MATCHING (117;20)		\leq	700
AN.R.17mg ^U	Place high R resistor on an N-well for better noise immunity.			

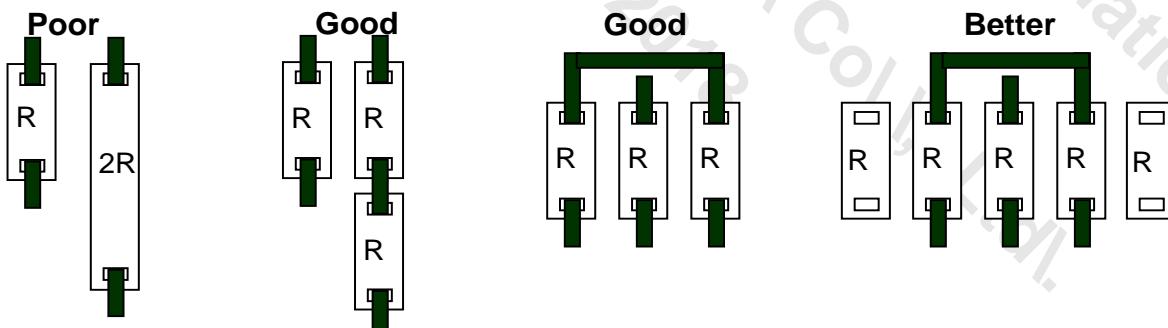


Figure 8.2.2.4.1 Example of matching topology of resistor layout for matching pairs

SR_DPO width = 86nm

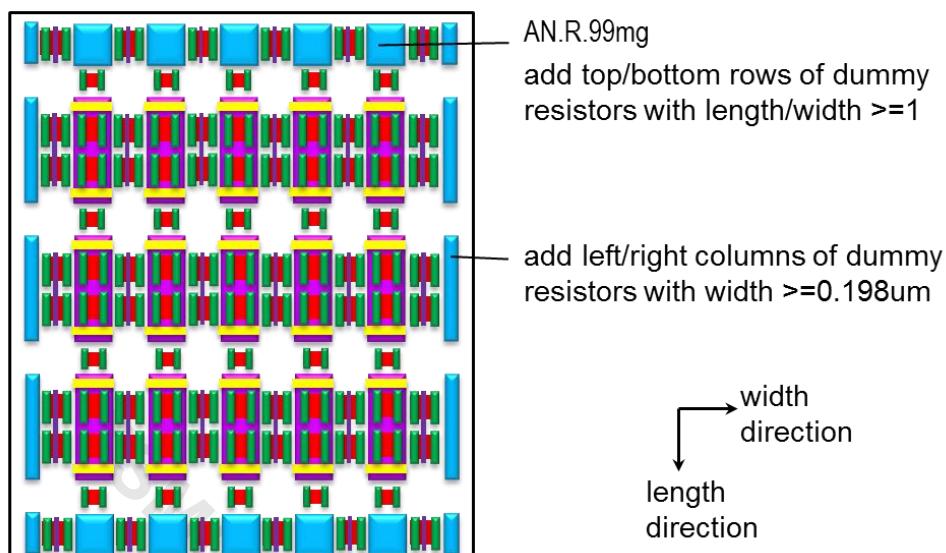


Figure 8.2.2.4.2 Example of matching resistor array layout

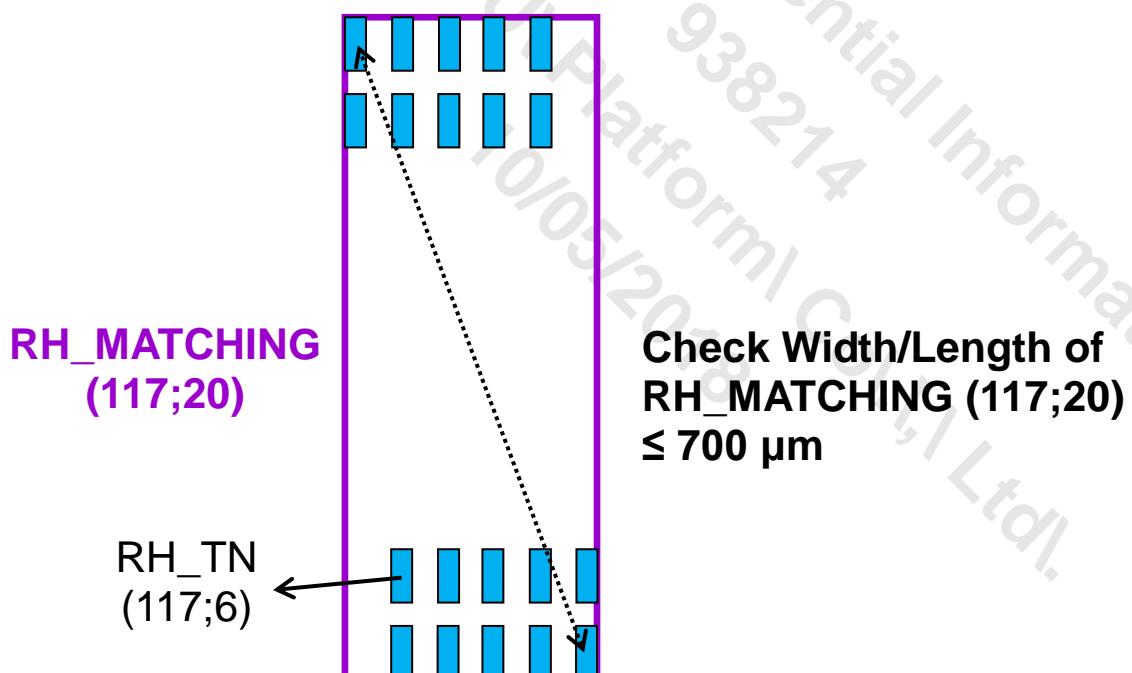


Figure 8.2.2.4.3 Drawing Example of RH_MATCHING for Hi-R distance DRC check

8.2.9 Metal Routing Guidelines

Rule No.	Description	Label	Op.	Rule
AN.R.10mg ^U	Pay attention on the associated routing layout, as well as the associated pattern density, of the matching pair, to minimize the Rs difference. (Figure 8.2.2.7.2). All the routing should be symmetrical to avoid mismatch.			

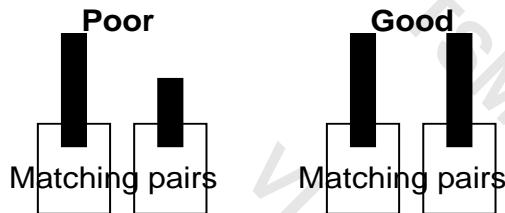


Figure 8.2.2.7.2 Example of the associated routing layout of the matching pair

8.3 Noise

8.3.1 Power and Ground

Rule No.	Description	Label	Op.	Rule
AN.R.22mg ^U	For the low noise circuit, a P-Well ring, which is tied to VSS, is recommended to surround all PMOS devices in each analog circuit block.			
AN.R.23mg ^U	For the low noise circuit, a N-Well ring, which is tied to VDD, is recommended to surround all NMOS devices in each analog circuit block.			
AN.R.24mg ^U	Put NMOS in RW (NW hole in DNW) is a good practice of isolating critical circuit from substrate noise (Figure 8.3.1.1.1). Make sure every NW connected to DNW must be the same potential (refer to DNW.R.4).			
AN.R.26mg ^U	Use separate power supplies and ground buses for the noisy and sensitive circuit and also for the analog and digital circuits. (Figure 8.3.1.1.4).			
AN.R.27mg ^U	Keep enough distance between the noisy and sensitive area.			
AN.R.28mg ^U	Use guard ring to stabilize substrate and well potential.			
AN.R.113mg ^U	For low noise OTA circuit, recommend input pair to be surrounded by identical dummy device tied to ground or power.			

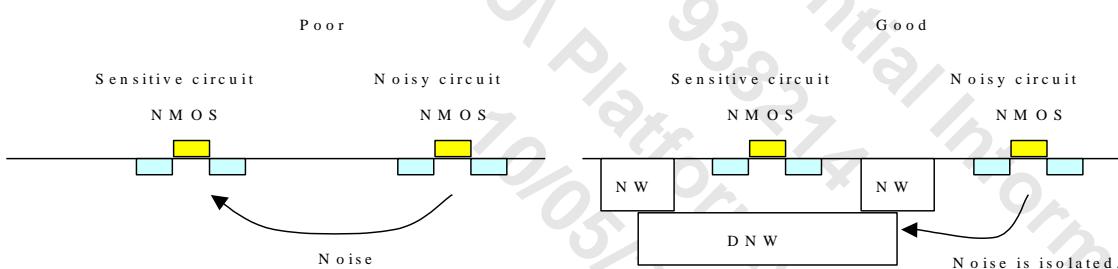


Figure 8.3.1.1.1 Example of NMOS in RW

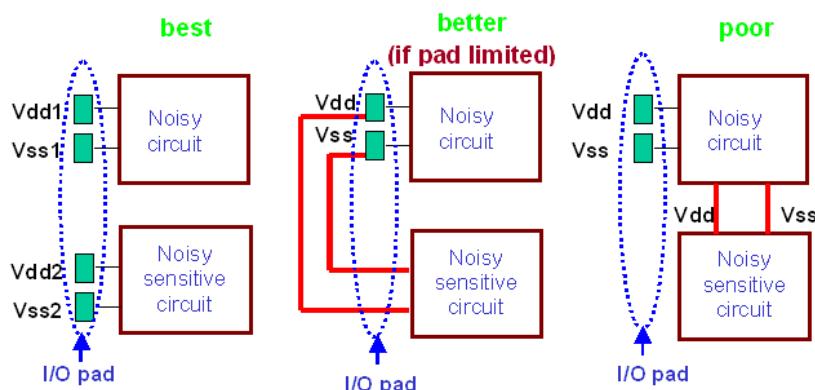
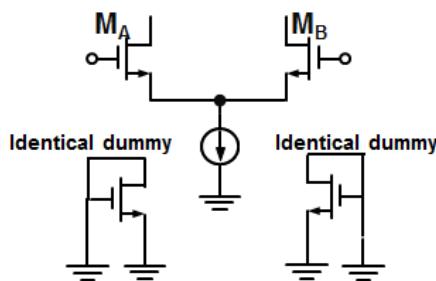
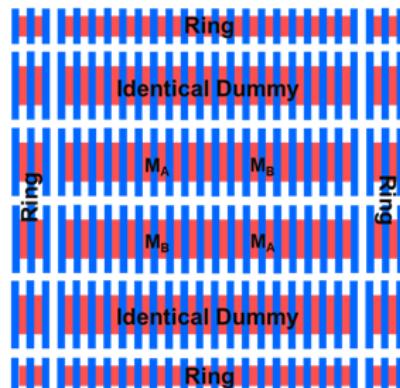


Figure 8.3.1.1.4 Example of separated power supplies and ground buses for the noisy and sensitive circuit



Input pair schematic



Dummy pattern for Input Pair

Figure 8.3.1.1.5 Example of low noise OTA circuit

8.3.2 Signal

Rule of thumb

No.	Description	Label	Op.	Rule
1	Keep high frequency signal in high level metal layer.			
2	Use metal shield for victim line that is noise sensitive.			
3	Use metal and poly shield for attacker line that travels through long distance.			
4	Prevent feedback path through chip seal-ring between critical input and output. Use additional guard ring to isolate the coupling. (Figure 8.3.2.1)			

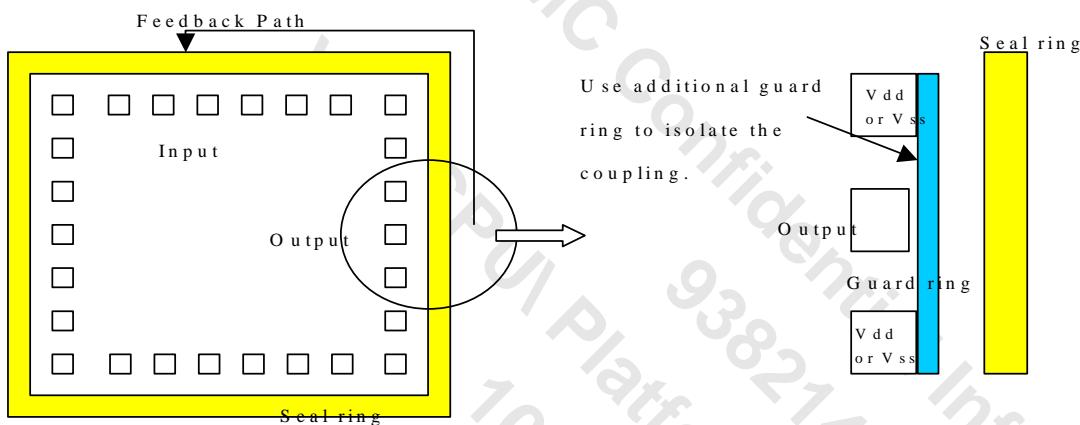


Figure 8.3.2.1 Example of prevention from feedback path through chip seal-ring

8.4 Burn-in Guidelines for Analog Circuits

Rule No.	Description	Label	Op.	Rule
AN.R.41mg ^U	The sensitive circuit, e.g. differential input pair, needs precise device mismatching parameter control such as ΔV_t and ΔI_{sat} . Therefore, it must avoid unbalanced DC bias stress during burn-in period. For example, $V_A = Vdd$ or GND & $V_B = 1/2Vdd$, which causes current supplied from current source flowing differently on the differential input pair ($I_A \neq I_B$). This will make differential pair matching become worse after burn-in stress. (Figure 8.4.1)			
AN.R.42mg ^U	Be sure that the analog circuit operates at normal operational condition during burn-in. For example, avoid P1 floating (when R is external) and make it be biased at the normal condition during burn-in. (Figure 8.4.2)			
AN.R.43mg ^U	Add a protection diode connection in the sensitive circuit to reduce plasma induced damage during wafer processing.			

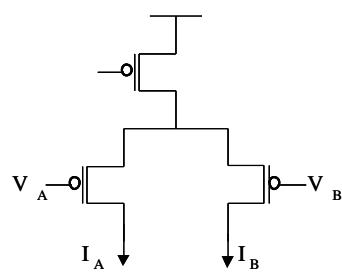


Figure 8.4.1 Example of differential input pair

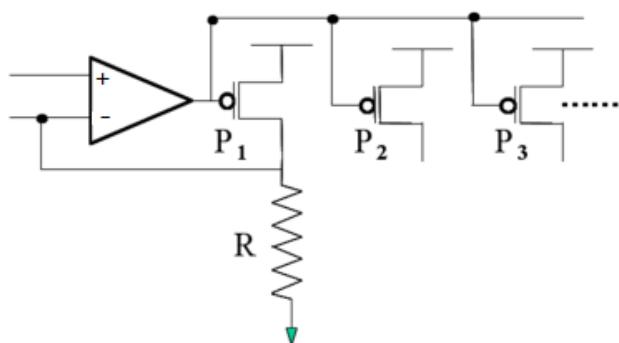


Figure 8.4.2 Example of analog circuit

9 Layout Guidelines for Latch-Up and I/O ESD

This chapter consists of the following 5 sections:

- 9.1 Layout rules and guidelines for latch-up prevention
- 9.2 I/O ESD protection circuit design and layout guideline
- 9.3 ESD Back-End Reliability Rule
- 9.4 Tips for the ESD/LU Design
- 9.5 ESD test methodology

Uses and limitation of ESD guidelines and Latch-up rule

Uses and Limitations of latch-up rules:

The Latch-up rules/guidelines are for design reference to achieve the target proposed by TSMC (JESD 78D). There are no specification or guaranteed levels for final chip/product qualifications, since Latch-up immunity is absolutely layout and circuit design dependent, including over-driven and substrate bias conditions, floating body circuits, SCR ESD IPs, and so on. Therefore, product latch-up validation is must before mass production. Also, note that these rules/guidelines do not cover the conditions such as power surge test, electrical fast transient test, high-level current injection by inductance load, cable discharge event, transient Latch-up by special function request or by system-level ESD test, etc.

Uses and Limitations of ESD guideline:

ESD design guidelines are for reference only, and do not provide specification or guaranteed levels of product performance and system level ESD. Devices passing device-level ESD testing do not guarantee ESD qualifications of a particular circuit using such devices.

In addition to the dedicated ESD protection device, the final chip/product ESD level may vary by but not limited to the following:

1. The normal functional devices in parallel (whose immunity and gate bias during ESD rely on the specific circuit design),
2. The power clamp protection cell/network, interface, the separation of high (Vdd, Vcc) and low (Vss, GND) power supply pads/groups,
3. The floor plan/metal bus routing and current density (endurance) of the backend interconnection's design.
4. Package type/size, connection/routing within package, physical die size, and others

The customer is ultimately responsible for the performance of design in question, thus TSMC can not guarantee or be hold responsible in any way on the customer's design success.

All rules and illustrations in this document are for reference only, and is subject to change as a result of further development by TSMC. All rules and illustrations shown are based on and representative of only TSMC in-house test structures. Performance difference & deviation may be expected in customer's own design.

9.1 Layout Rules and Guidelines for Latch-up Prevention

9.1.1 Latch-up Introduction

Latchup is a high-current state of a semiconductor device due to interactions between a PNP and NPN bipolar transistor where they are typically parasitic devices. In explaining latchup, the parasitic components of an inverter can be modeled as the equivalent circuit in Figure 9.1.1. When the output signal is higher than $V_{dd}+0.7V$ (overshoot trigger event), the bipolar VBJT2 turns on first. Similarly, as the output signal is lower than $-0.7V$ (undershoot trigger event), the bipolar LBJT2 turns on first. The collector of each BJT is connected to the base of another bipolar transistor and can inject the minority carriers to the well to induce a potential difference between PW and Vss, or NW and Vdd. This potential difference could forward the base to emitter junction of other bipolar transistors (LBJT1 or VBJT1), resulting in them turning on. When both BJTs connecting to V_{dd} (VBJT1) and V_{ss} (LBJT1) turn on, the injected minority carrier concentrations increase to be higher than the doping concentrations of NW and PW (Figure 9.1.2). Subsequently, NW and PW disappear and a heavy conductivity region creates a low resistance path between V_{dd} and V_{ss} . This latchup event between V_{dd} and V_{ss} may result in circuit malfunctions and device destructions in the worst case.

Note: LBJT1/LBJT2/VBJT2/VBJT1 mean parasitic BJT

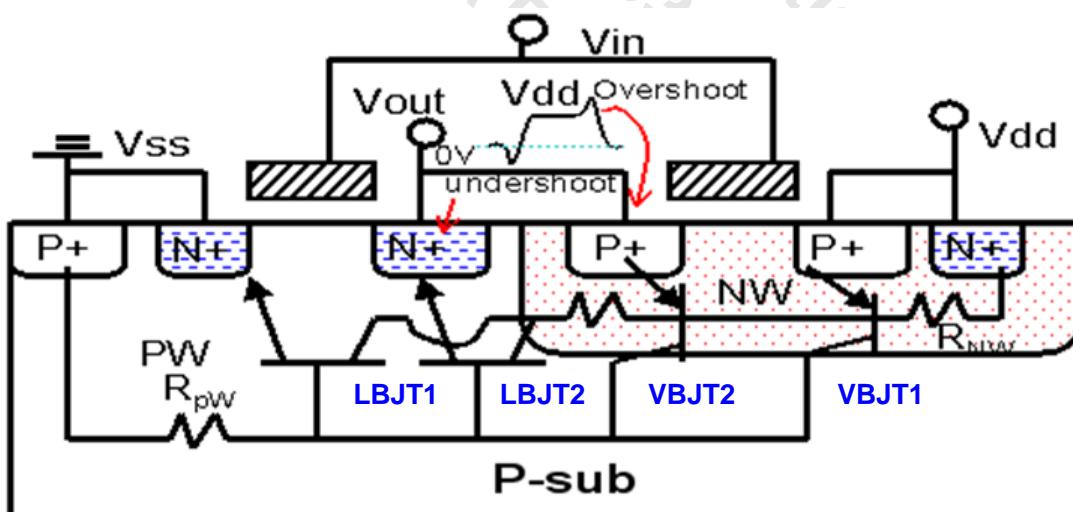


Figure 9.1.1 Lump element model for an inverter before latch-up

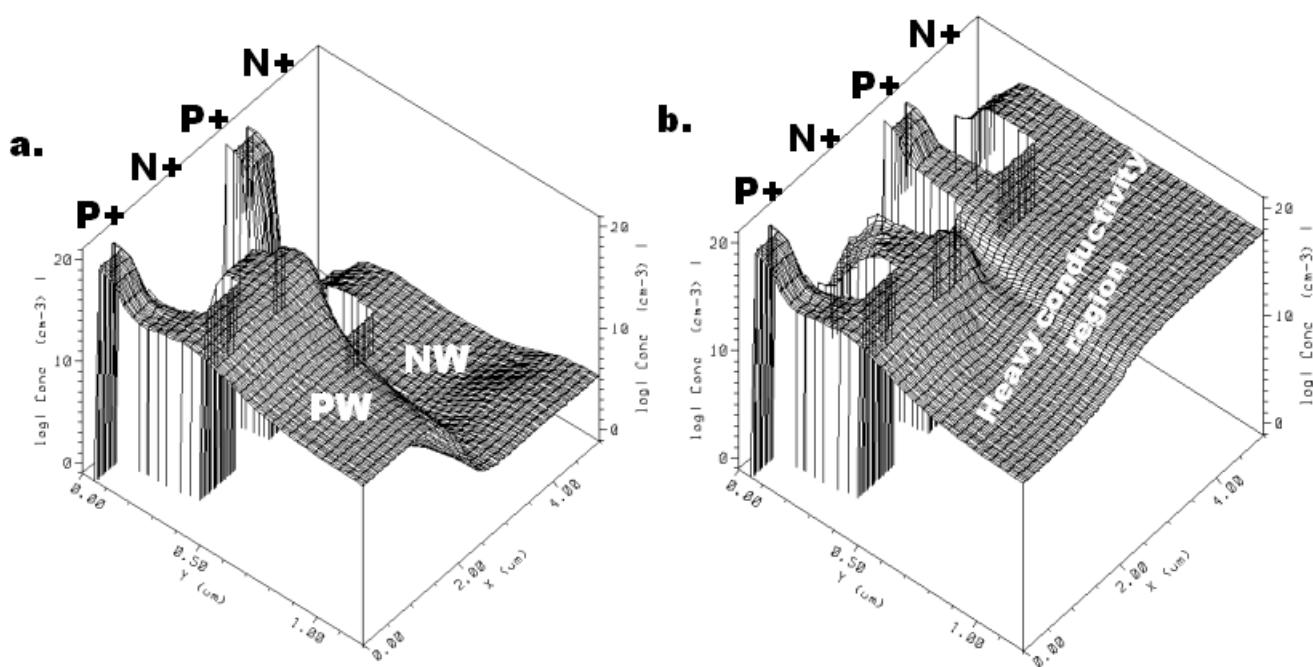


Figure 9.1.2 Hole concentrations (a) before latch-up, (b) after latch-up

The latch-up trigger sources often come from the I/O Pads, but both I/O circuits and internal circuits might cause latch-up if the layout does not follow the latch-up design rules. The following show some latch-up failure cases resulting from layout rule violations.

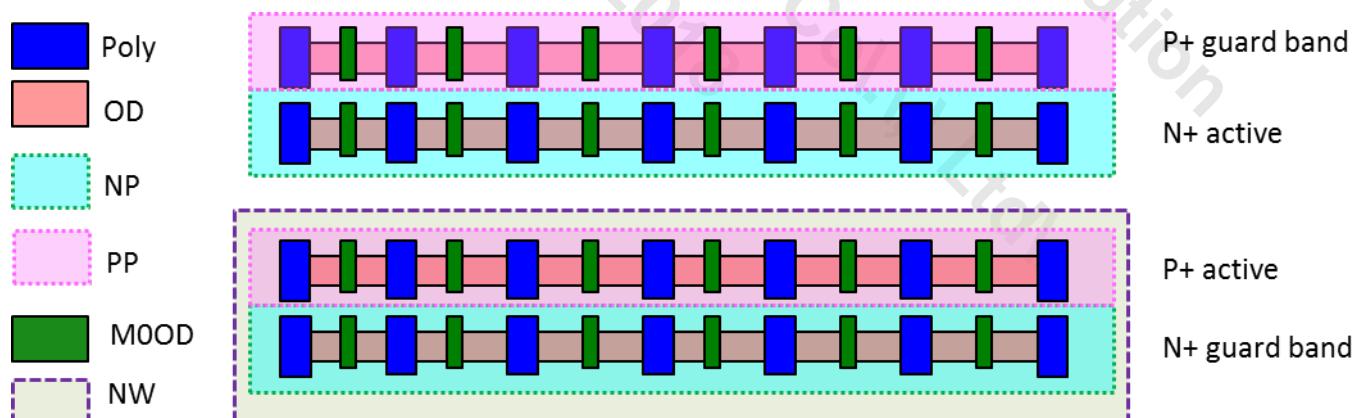


Figure 9.1.3 LUP.1 rule violation: (I/O without Guard-ring)

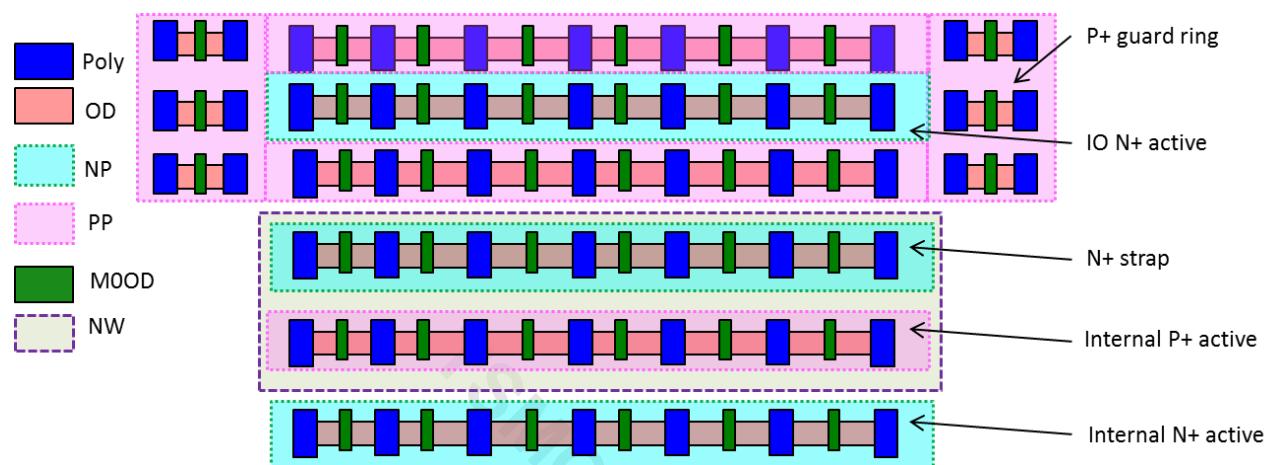


Figure 9.1.4 LUP.2 rule violation:
(Within 15 μm from I/O, N/PMOS in the internal circuit without the Guard-ring)

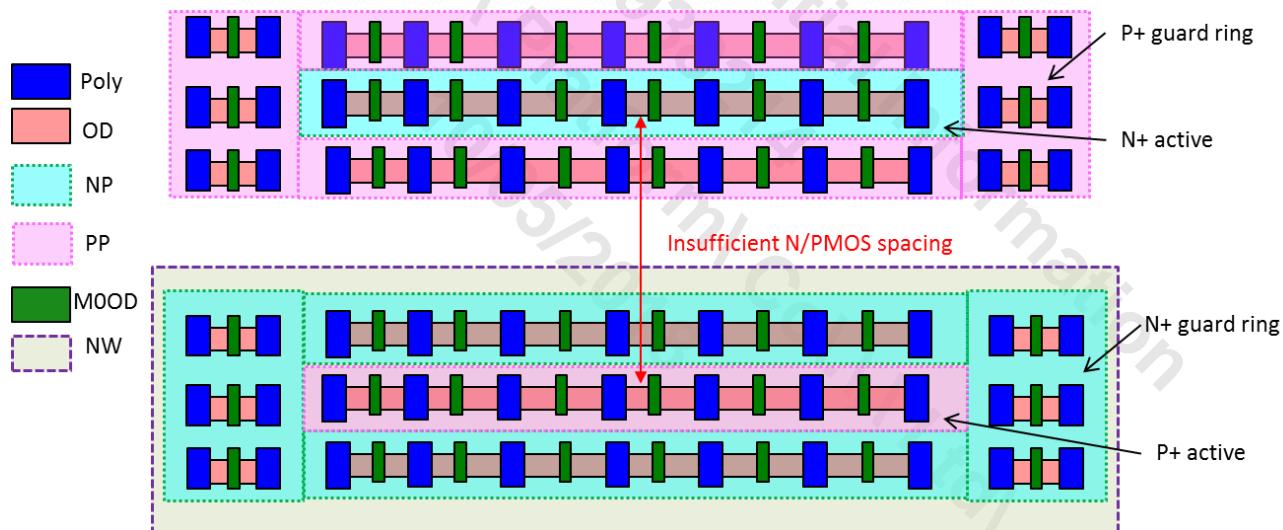


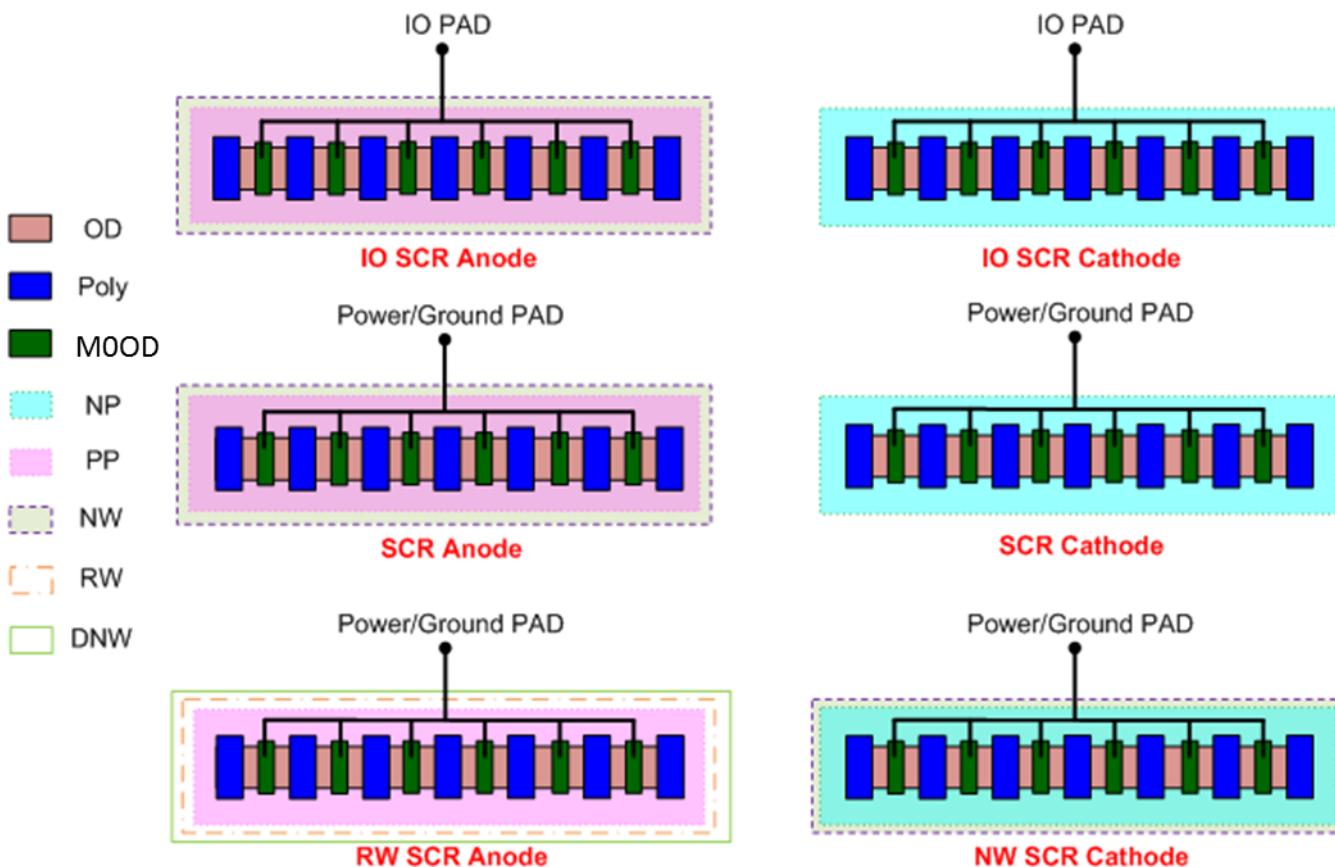
Figure 9.1.5 LUP.3 rule violation: (Insufficient I/O N/PMOS spacing)

9.1.2 Layout Rules and Guidelines for Latch-up Prevention

9.1.2.1 Special Definition in Latch-up Prevention

Term	Definition
I/O pads	Do not include Vdd pad and Vss pad.
Internal circuit	Include NMOS, PMOS, de-coupling capacitors and varactors that do not connect to an I/O pad.
LUP STRAP	<p>LUP STRAP includes LUP NWSTRAP and LUP PWSTRAP</p> <p>DRC defines effective LUP STRAP by followings:</p> <ol style="list-style-type: none"> 1. LUP STRAP = {effective STRAP_SEGMENT OR LUP_GATE} 2. STRAP_SEGMENT = {NWSTRAP OR PWSTRAP} NOT PO; DRC take effective STRAP_SEGMENT only. Effective STRAP_SEGMENT should be connected to VC or MP through (MD NOT CMD). 3. LUP_GATE = GATE INTERACT effective STRAP_SEGMENT <p>This definition applied to LUP.2.2/.2.3/.2.5/.2.6, LUP.6/.6.1/.6.2, LUP.13 group, LUP.13.1 group and LUP.13.2 group.</p>
LUP NWSTRAP	LUP NW STRAP means the NW STRAP of LUP STRAP connected to “solid power nets” or “design-intended virtual power nets”.
LUP PWSTRAP	LUP PW STRAP means the PW STRAP of LUP STRAP connected to “solid ground nets.”
Guard-ring	Complete, ring-type OD and M1 with as many MD and VIA0 as possible, connected to Vdd or Vss.(Please refer to the Figure 9.1.7 for the guard ring layout style)
N+ guard-ring	Complete, ring-type ((NP AND OD) AND NW) and M1 with as many MD and VIA0 as possible, connected to Vdd. (Please refer to the Figure 9.1.7 for the guard ring layout style)
P+ guard-ring	Complete, ring-type (PP AND OD) and M1 with as many MD and VIA0 as possible, connected to Vss. (Please refer to the Figure 9.1.7 for the guard ring layout style)
N+ pick-up ring	Complete, ring-type ((NP AND OD) AND NW) and M1 with as many MD and VIA0 as possible, connected to Vdd and surrounded around P+ active region. (Please refer to the Figure 9.1.7 for the guard ring layout style)
P+ pick-up ring	Complete, ring-type (PP AND OD) and M1 with as many MD and VIA0 as possible, connected to Vss and surrounded around N+ active region. (Please refer to the Figure 9.1.7 for the guard ring layout style)
NMOS cluster	A group of NMOSs.
PMOS cluster	A group of PMOSs.
OD injector	<p>Any Active OD (Ex. MOS, STI diode, diode string (DRC unchecked), and well resistor) or NWSTRAP/RWSTRAP covered by {DIODMY OR VAR} (Ex. Well diode and so on) directly connected to I/O PAD.</p> <p>N+ OD or NWSTRAP covered by {DIODMY OR VAR} directly connected to I/O pad is N+ OD injector.</p> <p>P+ OD or RWSTRAP covered by {DIODMY OR VAR} directly connected to I/O pad is P+ OD injector.</p> <p>When “DEFINE_PAD_BY_TEXT” is switched ON, all NWSTRAP/RWSTRAP connected to I/O pad would be taken as OD injector.</p>
IO SCR Anode	<p>Any P+ Active OD or RWSTRAP covered by {DIODMY OR VAR} directly connected to I/O pad.</p> <p>When “DEFINE_PAD_BY_TEXT” is switched ON, all RWSTRAP connected to I/O pad would be taken as IO SCR Anode. (Figure 9.1.6)</p>
IO SCR Cathode	<p>Any N+ Active OD or NWSTRAP covered by {DIODMY OR VAR} directly connected to I/O pad.</p> <p>When “DEFINE_PAD_BY_TEXT” is switched ON, all NWSTRAP connected to I/O pad would be taken as IO SCR Cathode. (Figure 9.1.6)</p>
SCR Anode	Any P+ Active OD directly connected to Power/Ground pad. (Figure 9.1.6)
SCR Cathode	Any N+ Active OD directly connected to Power/Ground pad.
NW SCR Cathode	Any NW directly connected to Power/Ground pad

Term	Definition
RW SCR Anode	Any RW in DNW directly connected to Power/Ground pad
SCR	SCR means parasitic silicon-controlled rectifier (SCR) which is usually formed by PMOS and NMOS, (Fig.9.1.1)



For MOS structure, drain and source may refer to different definition.

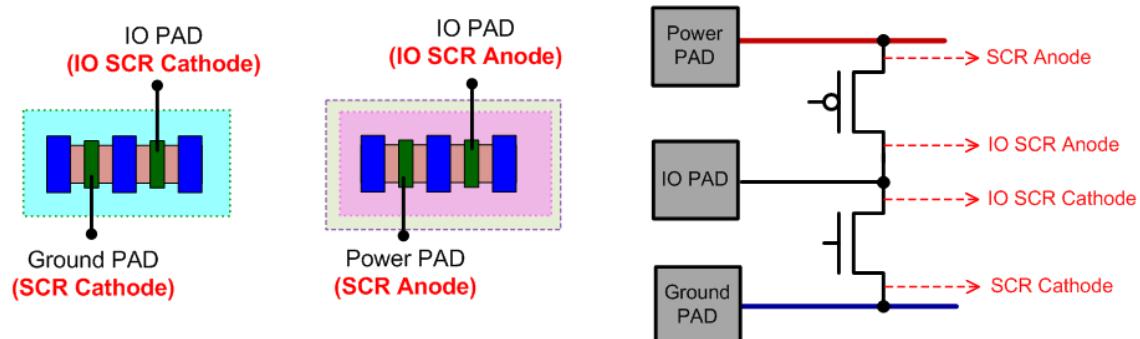


Figure 9.1.6 Example of “SCR Anode / Cathode”

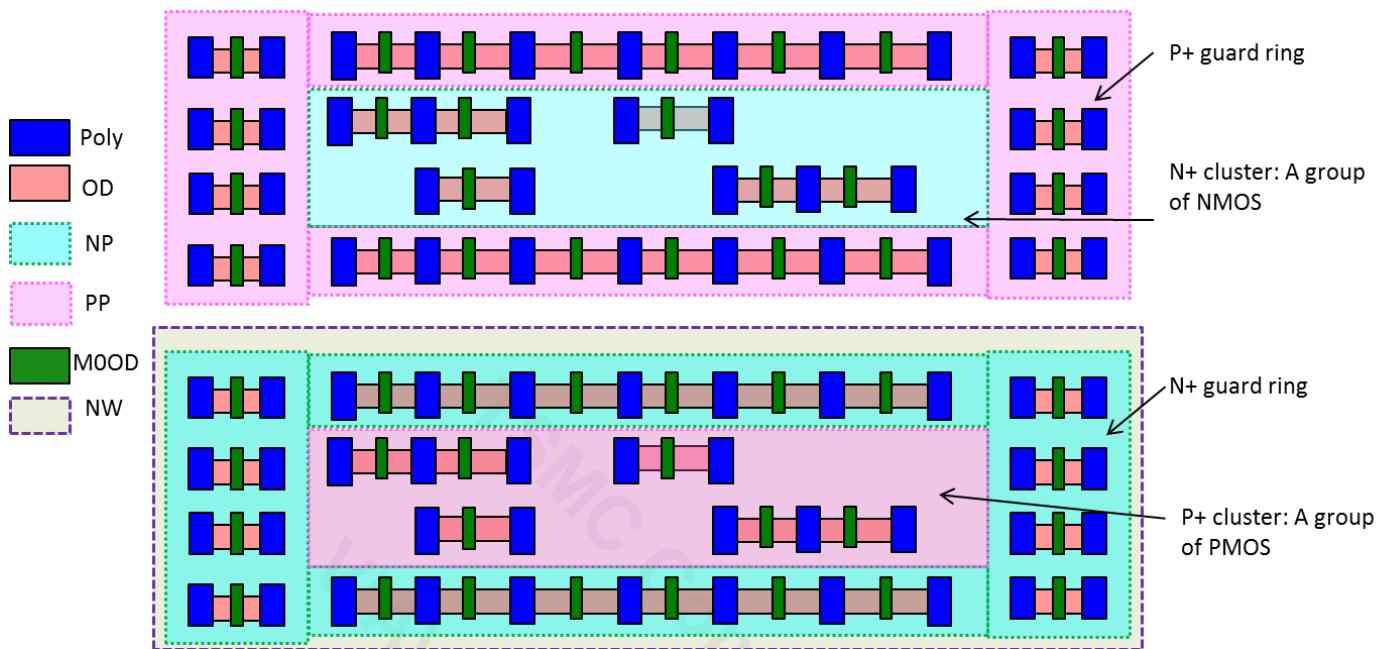


Figure 9.1.7 Example of an NMOS cluster and a PMOS cluster

9.1.2.2 Latch-up Dummy Layers Summary

The CAD layer and description for Latch-up Special Layers:

Special Layer Name	TSMC Default CAD Layer	Description	Associated With
LUPWDMY	255;1	To exclude OD injector from all latch-up rules.	LUP guidelines
LUPWDMY_2	255;18	DRC dummy layer to trigger the Area I/O latch-up rules check	LUP guidelines
LUPWDMY_IP	255;235	To waive specific latch-up rules	LUP guidelines
LUPIEDMY	255;56	To waive defined latch-up rules	LUP guidelines
LUP18VIEDMY	255;66	To relax defined latch-up rule for OD injector connected to medium noise signal PIN	LUP guidelines
LUP18VIEDMY_BUMP	255;63	To relax defined latch-up rule for OD injector connected to medium noise signal PIN	LUP guidelines
LUP15VIEDMY	255;65	To relax defined latch-up rule for OD injector connected to medium-low noise signal PIN	LUP guidelines
LUP15VIEDMY_BUMP	255;62	To relax defined latch-up rule for OD injector connected to medium-low noise signal PIN	LUP guidelines
LUPVIEDMY	255;58	To waive defined latch-up rule for OD injector connected to low noise signal PIN	LUP guidelines
LUPVIEDMY_BUMP	255;60	To waive defined latch-up rule for OD injector connected to low noise signal PIN	LUP guidelines
LUPULVIEDMY	255;67	To waive defined latch-up rule for OD injector connected to ultra-low noise signal PIN	LUP guidelines
LUPULVIEDMY_BUMP	255;68	To waive defined latch-up rule for OD injector connected to ultra-low noise signal PIN	LUP guidelines
LUPDWDMY	255;59	To waived defined STRAP density rules on specified region	LUP guidelines
LUP_015U	255;70	To recognize OD injector 15 µm checking window for IP level LUP rule check	LUP guidelines
LUP_045U	255;71	To recognize high-noise OD injector 45 µm checking window for IP level LUP rule check	LUP guidelines
LUP_075U	255;72	To recognize high-noise OD injector 75 µm checking window for IP level LUP rule check	LUP guidelines
LUP_045U_18V	255;91	To recognize med-noise OD injector 45 µm checking window for IP level LUP rule check	LUP guidelines
LUP_075U_18V	255;92	To recognize med-noise OD injector 75 µm checking window for IP level LUP rule check	LUP guidelines
LUP_045U_15V	255;101	To recognize med-low-noise OD injector 45 µm checking window for IP level LUP rule check	LUP guidelines
LUP_075U_15V	255;102	To recognize med-low-noise OD injector 75 µm checking window for IP level LUP rule check	LUP guidelines
RES200	255;9	Recognize resistor over 200ohm	LUP guidelines
VDDDMY	255;4	Dummy Layer for Power(Vdd) PAD	ESD/LUP guidelines
VSSDMY	255;5	Dummy Layer for Ground(Vss) PAD	ESD/LUP guidelines
IODMY	255;31	Dummy Layer for IO PAD	ESD/LUP guidelines

9.1.2.2.1 LUPWDMY Dummy Layer (CAD layer: 255;1)

LUPWDMY is a dummy layer to exclude OD injector from all latch-up rules.

Condition:

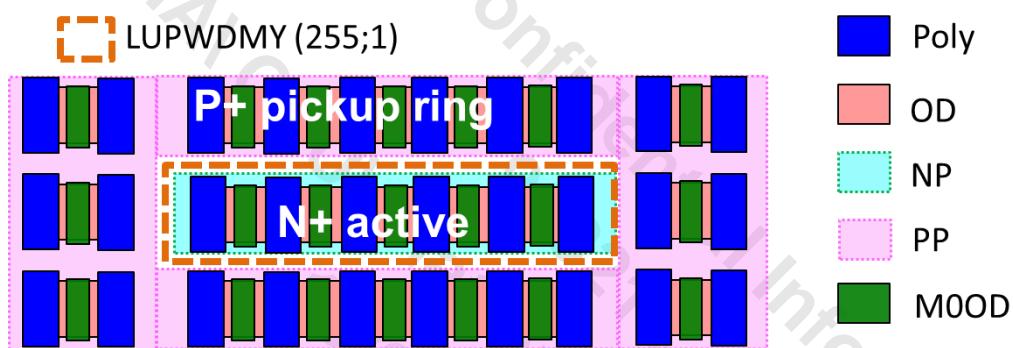
It is not recommended to use this layer before silicon proven.

Please consult TSMC if you would like to follow it as rules and have DRC violations before tape out.

Usage:

Draw LUPWDMY (255;1) to fully cover MOS/ACTIVE OD/ Diode regions that are connected to I/O pads, including the source, gate, drain, and diode, but not necessarily to cover Well STRAP, guard-ring.

It is for DRC usage but not a tapeout required CAD layer.



9.1.2.2.2 LUPWDMY_2 Dummy Layer (CAD layer: 255;18)

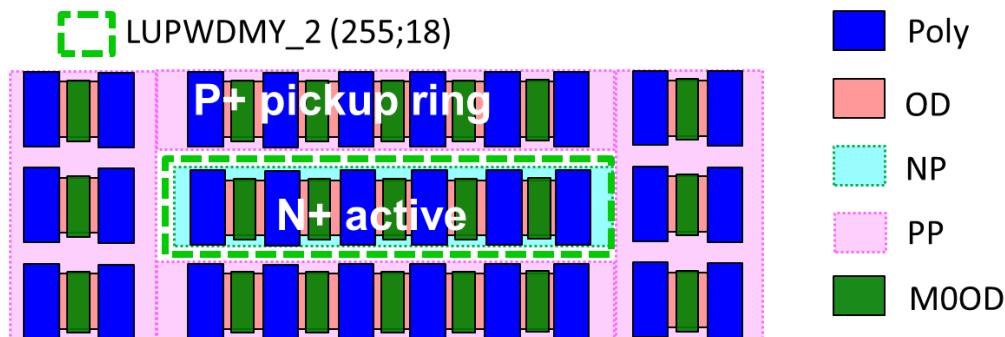
LUPWDMY_2 (255;18) is a DRC dummy layer to trigger the Area I/O latch-up rules check.

Condition:

Please refer to 9.1.2.5 for detailed AAIO I/O latch-up rule introduction.

Usage:

Draw a LUPWDMY_2 pattern to fully cover the OD injector. However it is not necessary to cover the Well STRAP or guard-ring.

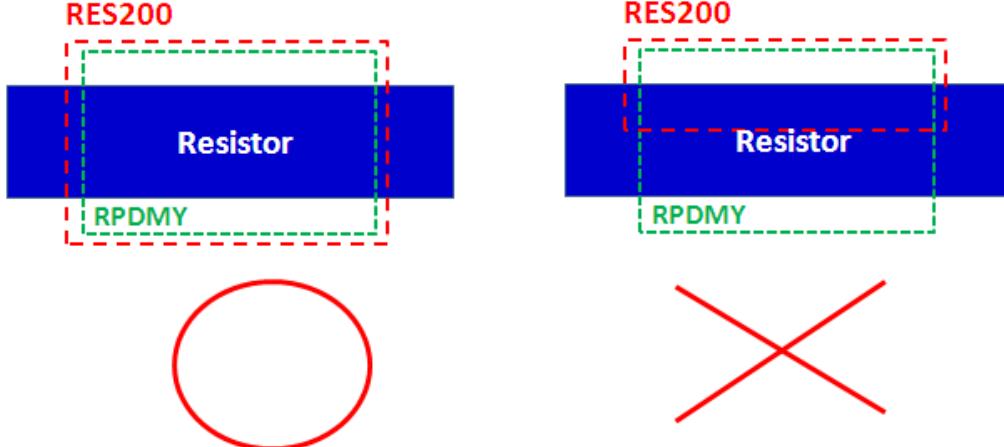


9.1.2.2.3 RES200 Dummy Layer (CAD layer: 255;9)

RES200 is a DRC layer for High R resistor (rhim) and it is used to recognize resistors with resistance larger than 200 ohm.

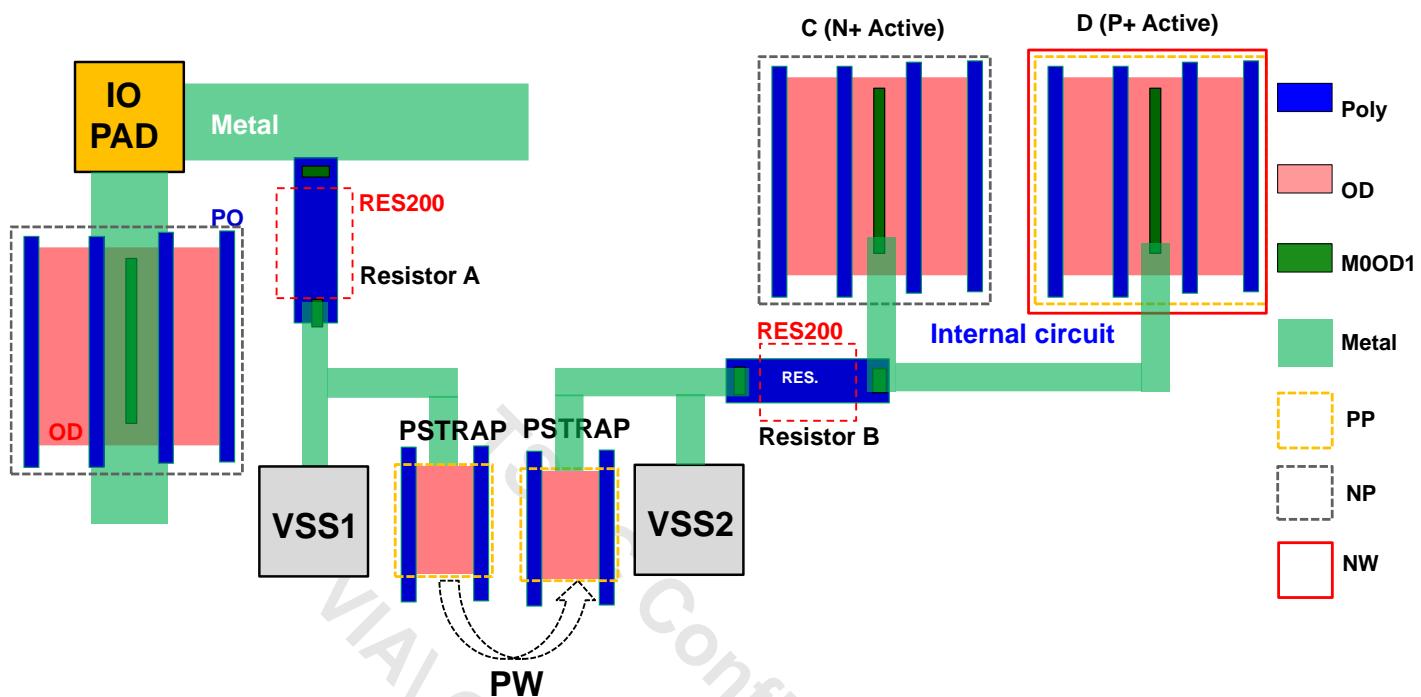
If the resistance of resistors between PAD and the Active/MOS OD is larger than 200 ohm, the dummy layer RES200 (255;9) should be covered on the resistor.

Latchup rules check connection will be broken by resistors with RES200 layer.



If resistors are added between PAD/Ground or Ground/devices, RES200 is suggested to cover on the resistor.

1. For below case, even C (N+ Active) or D (P+ Active) do not connect to IO PAD directly. C (N+ Active) or D (P+ Active) will be viewed as the OD injector owing to that they are connected to IO PAD through resistor A/PW/resistor B.
2. To exempt C(N+ Active) and D(P+ Active) as the OD injectors for latch-up checking, it can add RES200 to A or B resistor to break the connection from IO PAD.



9.1.2.2.4 LUPIEDMY Dummy Layer (CAD layer: 255;56)

LUPIEDMY is a dummy layer to waive the indicated latch-up rules of specific OD injectors.

Condition:

It is not recommended to use this layer before silicon proven.

Please consult TSMC if you would like to follow it as rules and have DRC violations before tape out.

Usage:

Draw LUPIEDMY (255;56) to fully cover OD injector regions that are connected to I/O pads, including the source, gate, drain, and diode, but not necessarily to cover Well STRAP, guard-ring.

It is for DRC usage but not a tapeout required CAD layer.

Usage scope of LUPIEDMY in LUP.7.6:

1. The body (NW) of OD injector PMOS isn't connected to VDD pin
2. The body (NW) of OD injector PMOS isn't connected to its self active OD

This table shows the latch-up rule exemption coverage by LUPIEDMY.

CAD Layer	Rule waive list by LUPIEDMY	
Rule List	LUP.1	LUP.5.0
	LUP.1.0.1 ^U	LUP.5.6
	LUP.2	LUP.7.6
	LUP.2.0.1 ^U	LUP.10
	LUP.2.2	LUP.13 group
	LUP.2.3	LUP.13.1 group
	LUP.2.4	LUP.13.2 group
	LUP.2.5	LUP.14
	LUP.2.6	--

9.1.2.2.5 Dummy Layers for Medium, Med-low, Low and Ultra-low Noise OD Injector Recognition

DRC dummy layers listed below are used to recognize OD injectors with different noise level by nets. They are not tape-out layers.

CAD layer usage for OD injector recognition	Medium noise OD injector	Medium-Low noise OD injector	Low noise OD injector	Ultra-Low noise OD injector
Cover CAD layer on M1 of specific signal net	LUP18VIEDMY (255;66)	LUP15VIEDMY (255;65)	LUPVIEDMY (255;58)	LUPULVIEDMY (255;67)
Cover CAD layer on CB, CB2 or UBM of specific signal net	LUP18VIEDMY_BUMP (255;63)	LUP15VIEDMY_BUMP (255;62)	LUPVIEDMY_BUMP (255;60)	LUPULVIEDMY_BUMP (255;68)

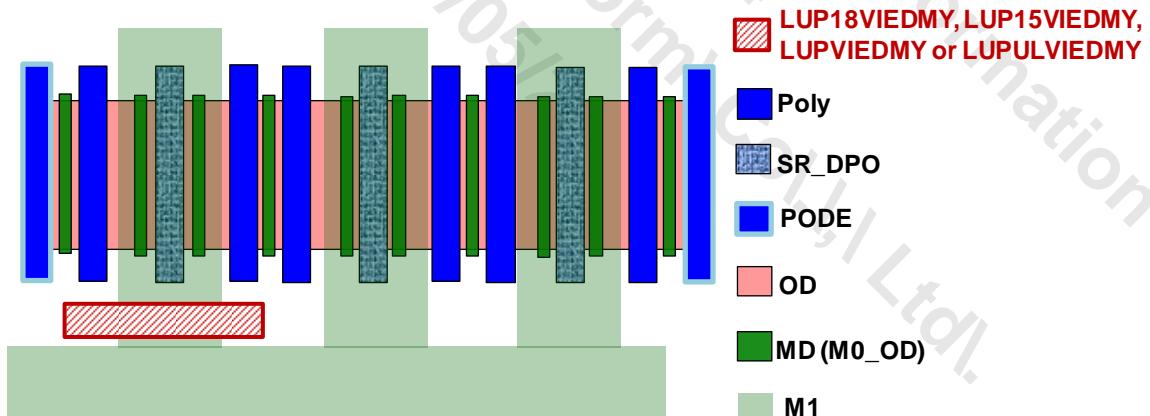
Condition:

It is not recommended to use this layer before confirming operation condition of signal pins.

Please consult TSMC if you would like to follow it as rules and have DRC violations before tape out.

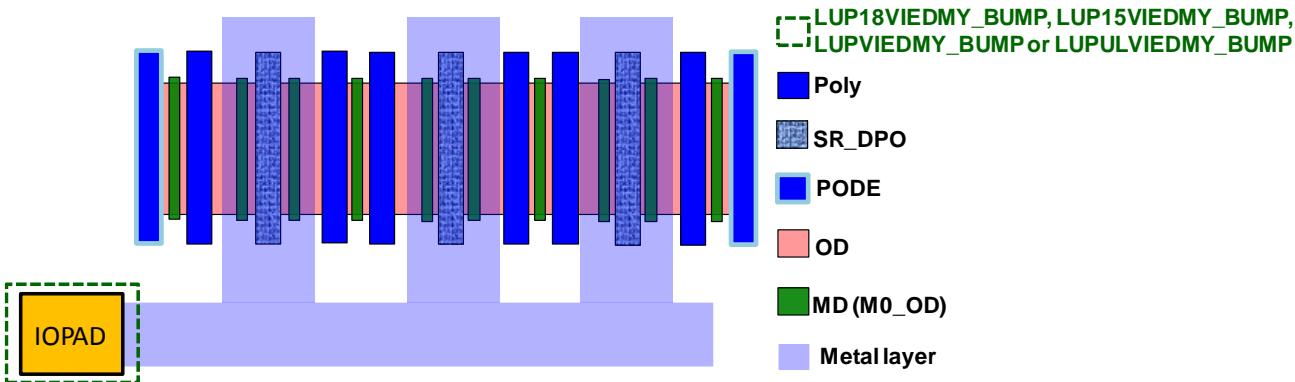
Usage for LUP18VIEDMY, LUP15VIEDMY, LUPVIEDMY and LUPULVIEDMY:

- As the “M1” layer overlaps with “LUP18VIEDMY”, “LUP15VIEDMY”, “LUPVIEDMY” or “LUPULVIEDMY” layer, all devices connecting to this “Net” will be treated as medium, medium-low, low or ultra-low noise OD injectors.
- It is for DRC usage but not a tapeout required CAD layer.



Usage for LUP18VIEDMY_BUMP, LUP15VIEDMY_BUMP, LUPVIEDMY_BUMP and LUPULVIEDMY_BUMP:

- As the “CB, CB2 or UBM” layer overlaps with “LUP18VIEDMY_BUMP”, “LUP15VIEDMY_BUMP”, “LUPVIEDMY_BUMP” or “LUPULVIEDMY_BUMP” layer, all devices connecting to this “Net” will be treated as medium, medium-low, low or ultra-low noise OD injectors.
- It is for DRC usage but not a tapeout required CAD layer.



For ultra-low noise OD injectors, they would be waived from following Latch-up rule checking

CAD Layer	LUP rule waive list for ultra-low noise signal pin (By LUPULVIEDMY or LUPULVIEDMY_BUMP)	
Rule List	LUP.2	LUP.4.1
	LUP.2.1 ^U	LUP.4.2 ^U
	LUP.2.2	LUP.7.6
	LUP.2.3	LUP.10
	LUP.2.4	LUP.13 group
	LUP.2.5	LUP.13.1 group
	LUP.2.6	LUP.13.2 group

For low noise OD injectors, they would be waived from following Latch-up rule checking.

CAD Layer	LUP rule waive list for low noise signal pin (By LUPVIEDMY or LUPVIEDMY_BUMP)	
Rule List	LUP.2.2	LUP.10
	LUP.2.3	LUP.13 group
	LUP.2.5	LUP.13.1 group
	LUP.2.6	LUP.13.2 group

For medium and medium-low noise OD injectors, some rules would be relaxed with different rule value between them. The relaxed rule list is shown below.

CAD Layer	LUP rule relax list for medium and med-low noise signal pin (By LUP18VIEDMY/LUP18VIEDMY_BUMP or LUP15VIEDMY/LUP15VIEDMY_BUMP)	
Rule List	LUP.10	LUP.13.1 group
	LUP.13 group	LUP.13.2 group

Note that, for HIANMOS (N+ ACTIVE INTERACT SDI_2) and well diodes (NW/RWSTRAP) OD injectors, its noise level does not purely judge by voltage swing.

- If their swing is controlled under certain level (i.e. $\leq +/-0.99V$, connected to medium/med-low/low or ultra-low noise pin), single stage HIANMOS is defined as **medium noise** OD injector; cascaded HIANMOS and NW/RW diodes (NWSTRAP/RWSTRAP) are defined as **high noise** OD injector.
- If their swing is very high (i.e. $> +/-0.99V$, connected to high noise pin), single stage HIANMOS, cascaded HIANMOS and NW/RW diodes (NWSTRAP/RWSTRAP) are defined as **high noise** OD injector.

When there are multiple CAD layers applied on the same signal nets, the most conservative rules value should be followed. For example, there is “LUP18VIEDMY” on M1 of net A. Meanwhile, there is a “LUPVIEDMY_BUMP” CAD layer on the bump of same net, net A. Then, the OD injectors connected to this net would be regarded as medium noise OD injectors instead of low noise OD injectors.

TSMC Confidential Information
938214
VIAI CPU Platform\ Col. I Ltd.
10/05/2018

9.1.2.2.6 LUPDWDMDY Dummy Layer (CAD layer: 255;59)

LUPDWDMDY is a DRC dummy layer to waive the indicated latch-up STRAP density rules. It is not a tape-out layer.

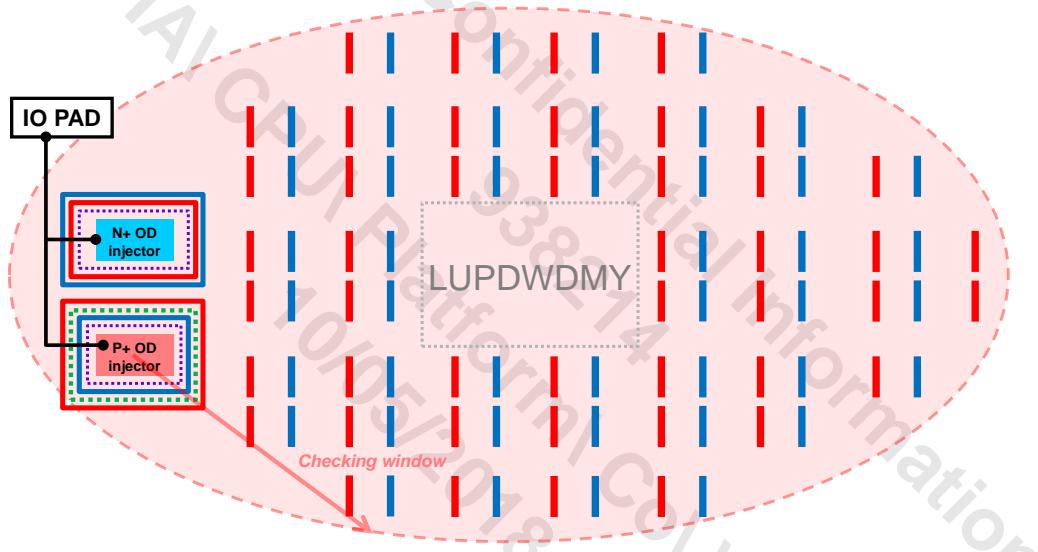
Condition:

It is not recommended to use this layer before silicon proven.

Please consult TSMC if you would like to follow it as rules and have DRC violations before tape out.

Usage:

Draw LUPDWDMDY (255;59) on regions without sufficiently STRAPS within specific checking window of latch-up STRAP density rules. The regions covered by this CAD layer would be excluded from rule checking.



LUPDWDMDY would waive following rules from Latch-up rule checking.

Rule lists
LUP.2.2
LUP.2.3
LUP.2.5
LUP.2.6

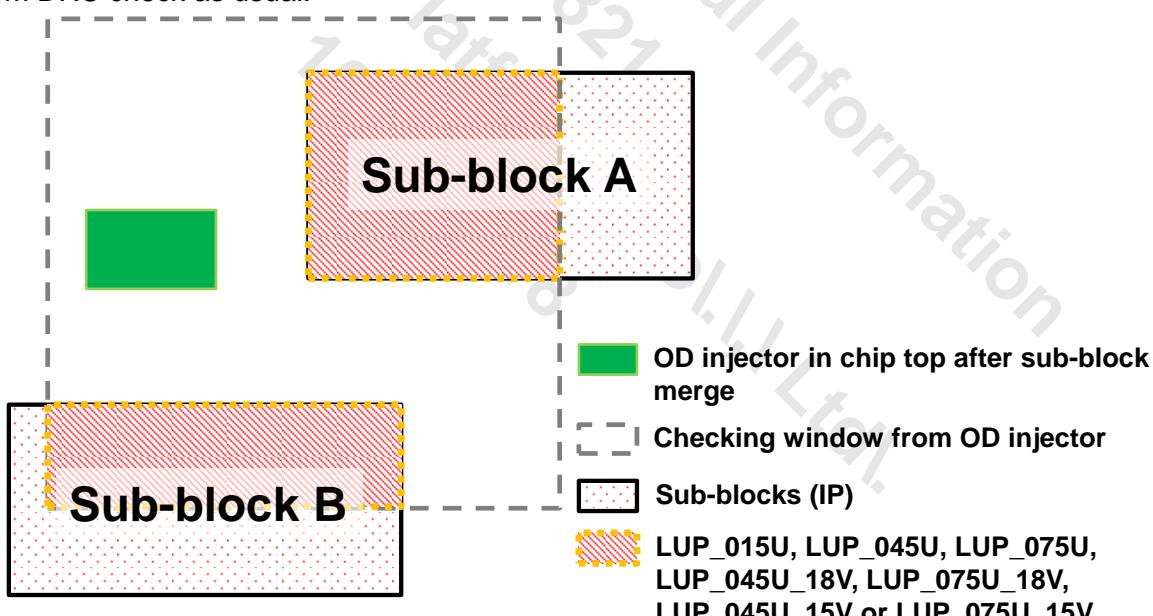
9.1.2.2.7 LUP Dummy Layers for checking window recognition

DRC dummy layers listed below are used to recognize checking window of OD injectors with different noise level in IP level LUP rule check. They are not tape-out layers.

LUP Dummy Layers	High noise OD injector	Medium noise OD injector	Medium-Low noise OD injector	Low noise OD injector	Ultra-Low noise OD injector
For checking window recognition	LUP_015U (255;70)				N/A
	LUP_045U (255;71)	LUP_045U_18V (255;91)	LUP_045U_15V (255;101)	N/A	N/A
	LUP_075U (255;72)	LUP_075U_18V (255;92)	LUP_075U_15V (255;102)	N/A	N/A

Usage:

1. Draw LUP_015U, LUP_045U/ LUP_045U_18V/ LUP_045U_15V or LUP_075U/ LUP_075U_18V/ LUP_075U_15V on regions which will be within 15um, 45um or 75um from OD injector after sub-blocks integration.
2. Turn-on DRC option “IP_LEVEL_LUP_CHECK.”
3. Perform DRC check as usual.



Note:

- a. “IP_LEVEL_LUP_CHECK” should not be turned on when the “FULL_CHIP” DRC option is switched on.
- b. The function of these CAD layers is enabled only when “IP_LEVEL_LUP_CHECK” is turned on.
- c. When considering the checking window of OD injector after sub-block integration, please be aware of that the shape of checking window is different for LUP_015U and others. The checking window for LUP_015U is a circle with radius of 15 µm. As for others, the checking window is recognized by sizing up OD injectors 45um or 75um, respectively.
- d. If there is OD injector drawn inside IP layout database, the DRC takes both of “the checking window detected by OD injector” and “the regions recognized by these CAD layers” into consideration.

- e. These CAD layers can be overlapped on same regions. And it would be taken to check specific LUP rules, separately. The specific LUP rule coverage for these CAD layers is listed below.

CAD Layer	LUP_015U	LUP_045U/LUP_075U/ LUP_045U_15V/LUP_075U_15V/ LUP_045U_18V/LUP_075U_18V
Rule List	LUP.2	LUP.2.5
	LUP.2.2	LUP.2.6
	LUP.2.3	LUP.10
	LUP.2.5	LUP.13 group
	LUP.2.6	LUP.13.1 group
	LUP.4.1	LUP.13.2 group

- f. The shape of latch-up rule checking window is highly correlated with OD injectors itself. In DRC, OD injectors checking window can be generated in RDB format, LUP*_WIN.rdb, after each of DRC runs. To enable this function, a DRC option “LUP_MASK_HINT” should be switched on. Those generated checking window RDB are rule based, user can refer to information inside RDB and transform them into layout database with corresponding CAD layer number/datatype individually.

9.1.2.3 DRC methodology for Latch-up Rules

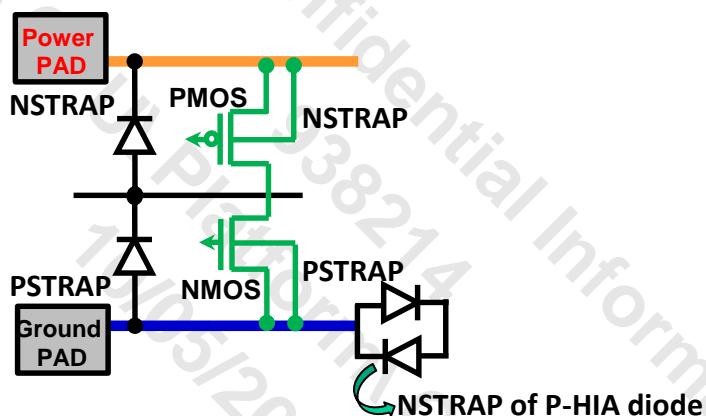
9.1.2.3.1 General DRC methodology for PAD type

DRC use the following features to distinguish Power and I/O PAD:

1. By default, DRC will recognize power PAD according to the connectivity of CB, CB2, and UBM to STRAP.

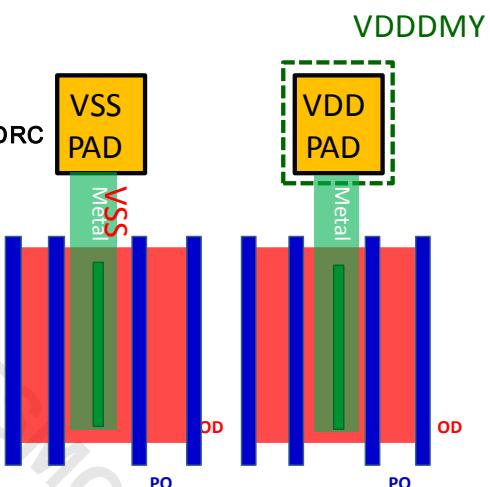
- I. DRC will recognize ground PAD according to the connectivity of CB, CB2, and UBM to PSTRAP [except VAR, DIODMY].
- II. DRC will recognize power PAD according to the connectivity of CB, CB2, and UBM to NSTRAP [except VAR, NW resistor, HIA_DUMMY (168;0), DIODMY] without the connectivity of CB, CB2, and UBM to PSTRAP.

Ex. The connectivity of CB, CB2, and UBM to PSTRAP only: ground PAD. The connectivity of CB, CB2, and UBM to PSTRAP and NSTRAP both: ground PAD. The connectivity of CB, CB2, and UBM to NSTRAP only: power PAD.

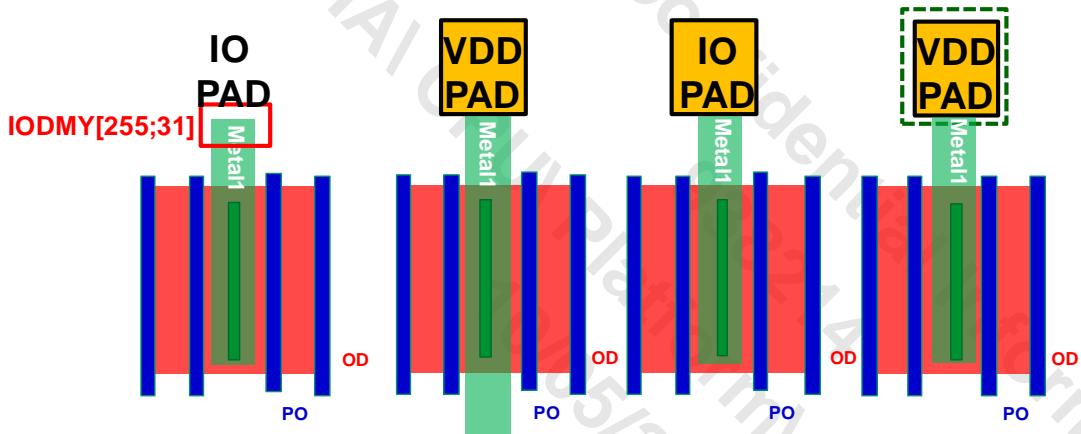


2. DRC will also recognize PAD with “power dummy layer” as power PAD, and “IO dummy layer” as IO PAD.
 - I. VDDDMY(255;4): Dummy Layer for Power(Vdd) PAD
 - II. VSSDMY(255;5): Dummy Layer for Ground(Vss) PAD
 - III. IODMY(255;31): Dummy Layer for IO PAD
3. Alternatively, with corresponding DRC switch turned-on manually, DRC will recognize PAD with “power text” as power PAD.
 - I. Control by the switch of #DEFINE_PAD_BY_TEXT. The switch is off by default.
 - II. Default power text name is “VDD?” “VSS?”
4. IODMY methodology is default turn-on and it can be used for IP level latch-up checking especially for without PAD existing condition. For more usage information, please refer to chapter 9.1.2.3.3.
5. As ESD or IO related devices has embedded IODMY marker layer, the latch-up rule checker will be triggered even if DRC option "DEFINE_PAD_BY_TEXT" is off in IP level DRC verification.
6. For I/O net that does not connect to TSMC ESD library device, two options can be implemented to trigger latch-up rule checker in DRC.
 - I. Turn on DRC option of "DEFINE_PAD_BY_TEXT" and assign correct pin name of I/O pad in DRC variable "PAD_TEXT" to trigger latch-up checker
 - II. Manually add IODMY layer on the IO net. For dummy layer usage, please refer to chapter 9.1.2.3.3.
7. All other unrecognized PADs through step 1~3 are also I/O PAD

"VSS" is a top level text attached on metal, and
DEFINE_PAD_BY_TEXT option is turned on in DRC



VDDDMY (255;4)



Check LUP.1, LUP.2, LUP.2.1 LUP.3.0, LUP.3.1.1, LUP.3.2.1, LUP.4, LUP.5.1.1, LUP.5.2.1, LUP.5.6.1~4, LUP.7.6.1~4, LUP.9. in Cell level without PAD

1. Attach top-level text on metal. E.g. "PAD"
2. Turn on DEFINE_PAD_BY_TEXT option.

9.1.2.3.2 General DRC methodology for I/O PAD type connectivity

DRC use the following features to check the device connectivity to I/O pad:

1. Build-up the connection by Metal, Via, RV, AP, CB, CB2, and UBM
2. Latch-up risk of the junction/OD connects to pad through a resistor:
 - a. If $R \geq 200$ ohm. → low latch-up risk
 - b. If $R \leq 50$ ohm. → High latch-up risk
 - c. If $50\text{ohm} < R < 200\text{ohm}$ → it depends.

RES200 CAD layer is a DRC layer used to recognize resistors between PAD and active/MOS OD regions whose value is larger than 200 ohm. In this case, dummy layer RES200 (255;9) should cover the resistor to disable Latch-up check.

3. There are two DRC switches and one required CAD layer (RES200 layer) related to the resistor in series: "**DISCONNECT_ALL_RESISTOR**" (1st DRC switch; default OFF), "**CONNECT_ALL_RESISTOR**" (2nd DRC switch; default OFF), and **RES200 CAD layer (manually placed)**.

Below are possible scenarios for their interactions in between:

1. Consider resistance (default) to check circuits behind resistor:

- ($R < 200\text{ohm}$) => Set both switches to OFF and W/O RES200, circuits after resistor will be checked.
- ($R \geq 200\text{ohm}$) => Set both switches to OFF and the $R \geq 200\text{ohm}$ resistor is covered by RES200 layer, circuits after resistor will NOT be checked

2. Neglect circuits behind resistor

- Set "DISCONNECT_ALL_RESISTOR" to ON, all circuits after resistor will NOT be checked (RES200 layer is irrelevant this scenario.)

3. Check circuits behind resistor

- Set "CONNECT_ALL_RESISTOR" to ON, all circuits after resistor will be checked (RES200 layer is irrelevant this scenario.)

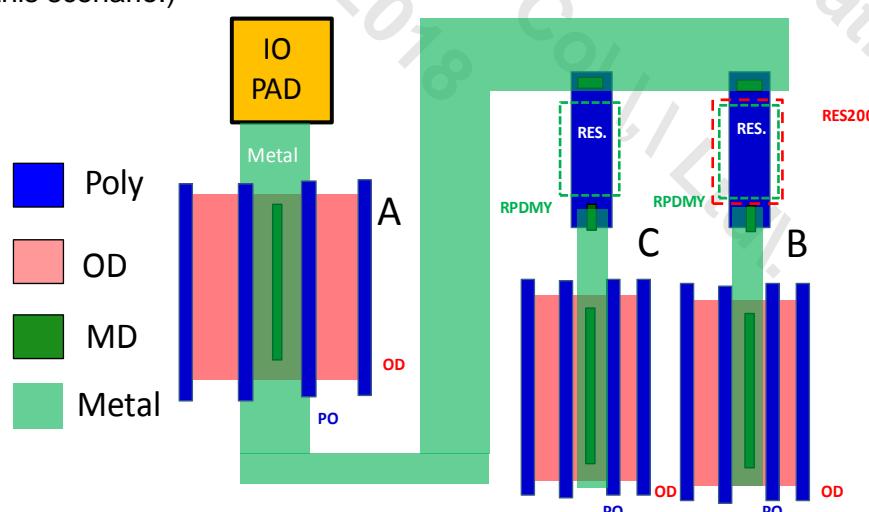


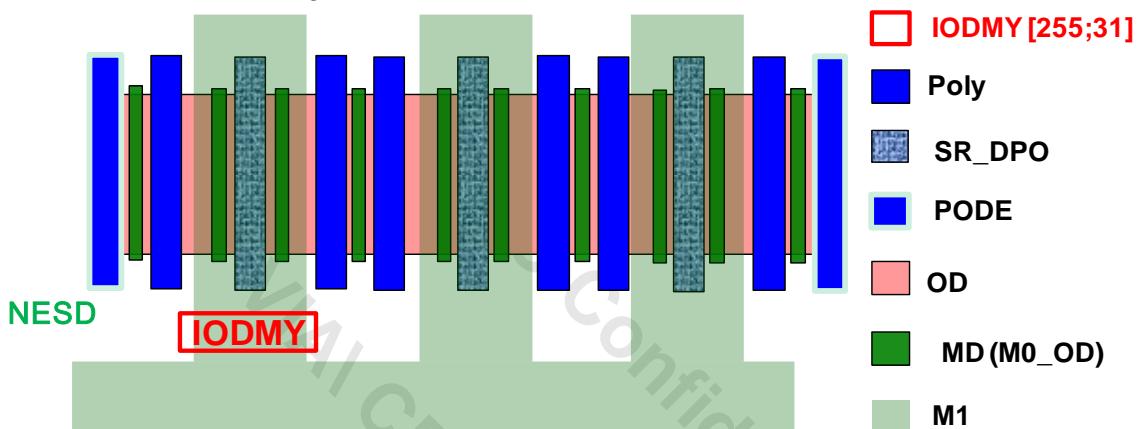
Figure 9.1.2.3.3

A/B/C in Fig. 9.1.2.3.3	DRC deck setup		
	Default (DISCONNECT_ALL_RESISTOR: OFF) (CONNECT_ALL_RESISTOR: OFF)	Turn ON DISCONNECT_ALL_RESISTOR	Turn ON CONNECT_ALL_RESISTOR
A	OD injector	OD injector	OD injector
B	Internal circuit	Internal circuit	OD injector
C	OD injector	Internal circuit	OD injector

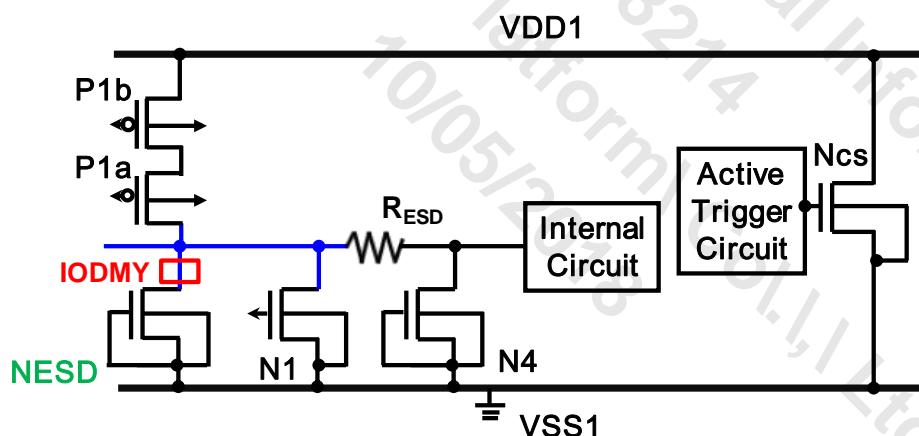
9.1.2.3.3 General DRC methodology for I/O Net type connectivity

DRC use the following features to check the device connectivity to I/O net:

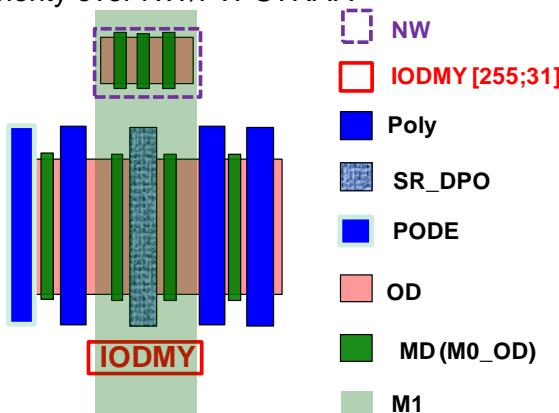
1. As the “M1” layer overlaps “IODMY” (255;31) layer, the “Net” connecting to M1 will be taken as connecting to IO PAD directly. All devices connecting to this “Net” will be taken as OD injector and DRC latch-up checking will be applied for them.
2. This methodology is default turn-on and it can be used for IP level latch-up checking especially for without PAD existing condition.



3. NESD's M1 overlaps IODMY (255;31), thus this “Net” will be taken as connecting to IO PAD directly even if there is no PAD existing. P1a, N1 will also be taken as OD injector and latch-up checker will be applied for them.

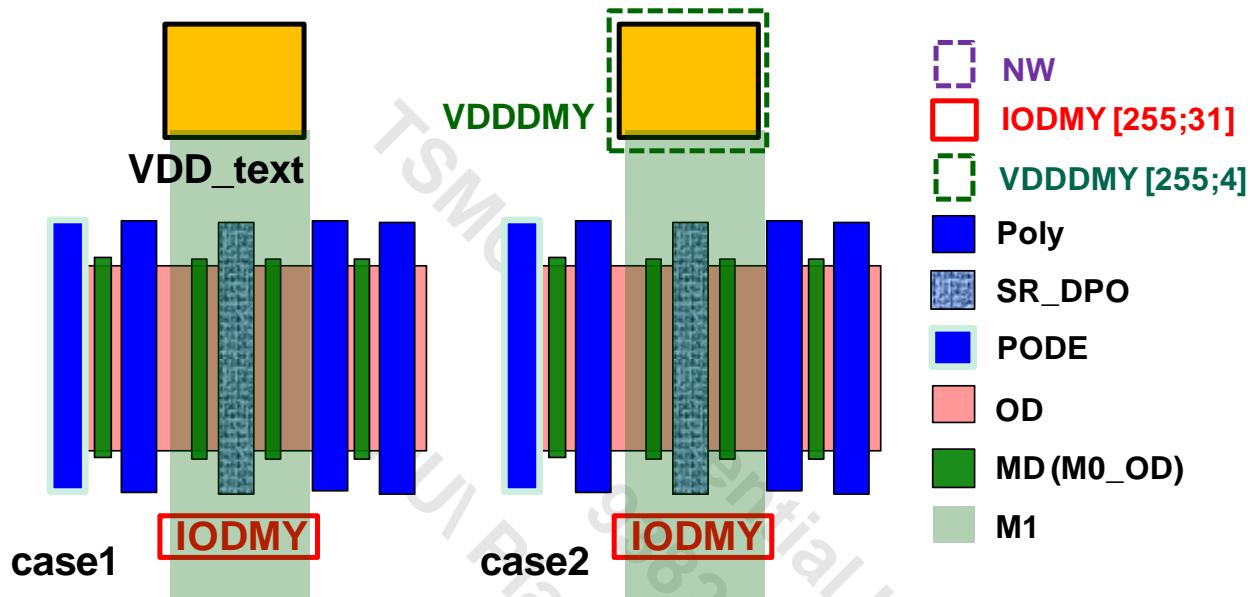


4. Priority of Latch up checking if “DEFINE_PAD_BY_TEXT is turn-off.
 - a. Priority : IODMY (255;31) > NW/PW STRAP (guard ring)
 - b. For below figure, this “Net” will be taken as connecting to IO PAD directly because the IODMY has priority over NW/PW STRAP.



5. Priority of Latch up checking if “DEFINE_PAD_BY_TEXT is turn-on

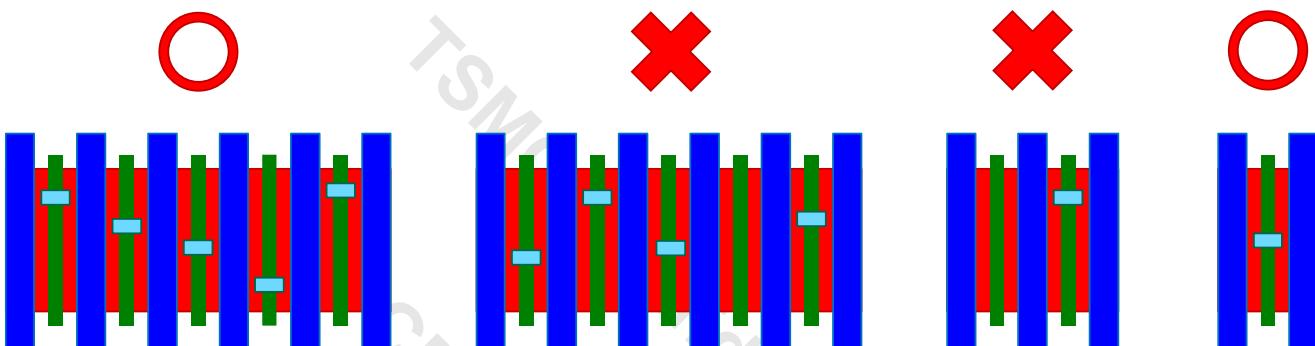
- I. Priority of PAD dummy and text if all of them existed: VDD/VSS text > IODMY > VDDDMY/VSSDMY
- II. For case 1 shown in below, this Net will be taken as connecting to VDD PAD because “VDD text” has priority over “IODMY”.
- III. For case 2 shown in below, this Net will be taken as connecting to IO PAD because “IODMY” has priority over “VDDDMY”.



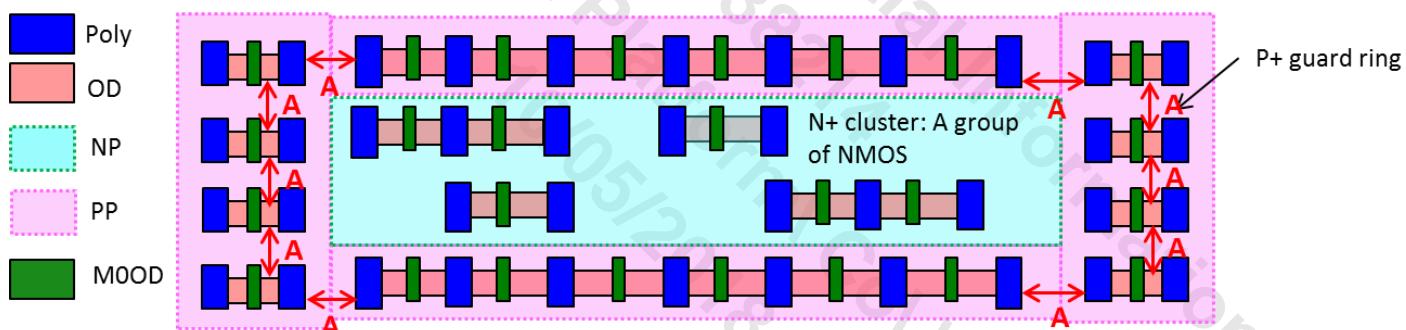
9.1.2.3.4 General DRC methodology for Guard Ring

DRC take the effective STRAP as guard ring element to recognize a complete guard ring when OD space (A) $\leq 0.562 \mu\text{m}$ and parallel run length (B) $\geq 0.2 \mu\text{m}$.

For the effective STRAP, all of STRAP_SEGMENT (STRAP NOT PO) on single STRAP should be connected to VC or MP through (MD NOT CMD). If there is one or more STRAP_SEGMENT without connection to VC nor MP, it would not be taken as valid STRAP for guard ring formation.

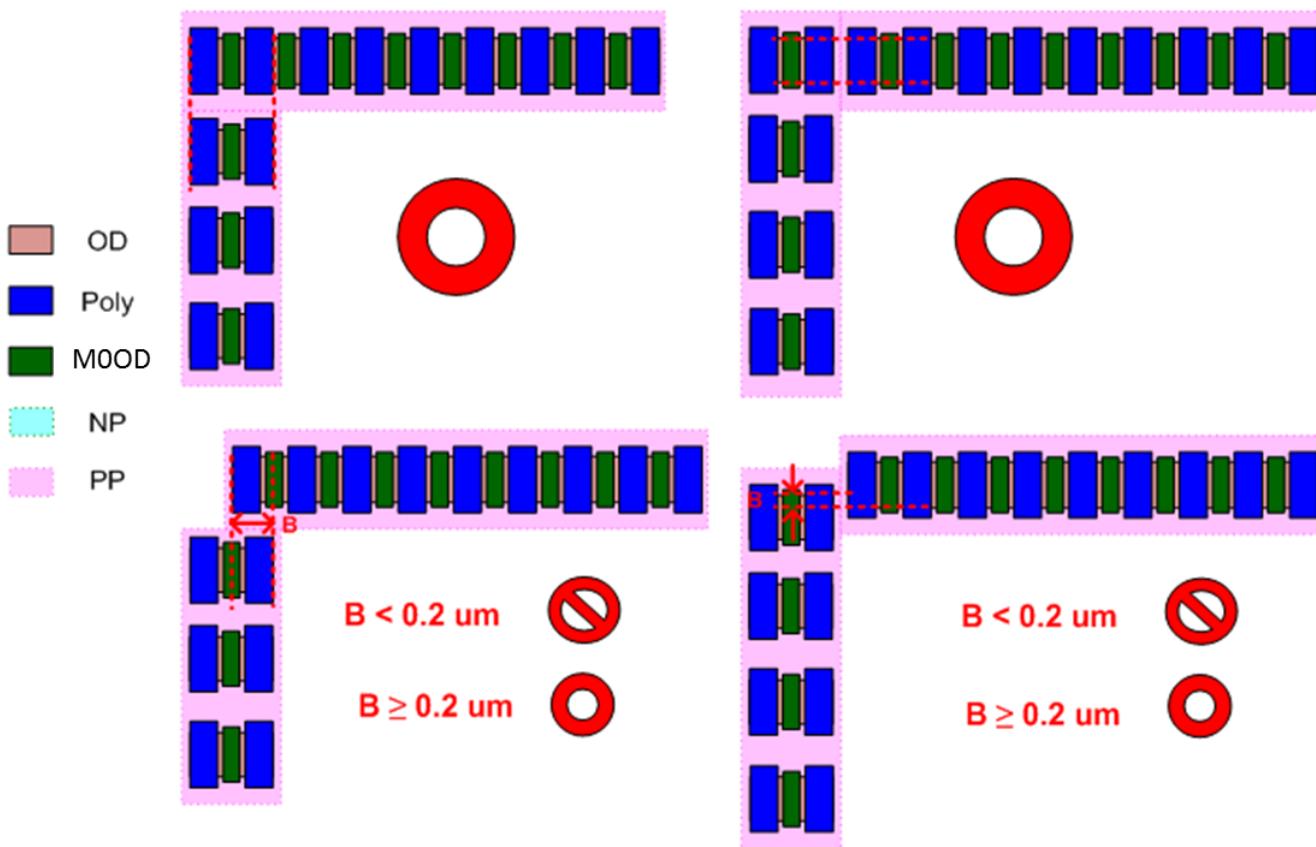


This definition applies to LUP.1, LUP.1.1, LUP.1.2, LUP.1.3, LUP.2, LUP.4, LUP.4.1 and LUP.14.



If OD to OD space (A) $\leq 0.562 \mu\text{m}$, it will be regarded as a ring.

If OD to OD space (A) $> 0.562 \mu\text{m}$, it won't be regarded as a ring.



If OD parallel run length ($B \geq 0.2 \mu m$) it will be regarded as a ring.

If OD parallel run length ($B < 0.2 \mu m$) it won't be regarded as a ring.

9.1.2.3.5 General DRC methodology for Delta Voltage LUP Rule

Below section describes the checking methodology of delta voltage LUP rule.

Delta voltage LUP rule includes LUP.3.0, LUP.5.0, LUP.5.6, LUP.7.6. DRC check would not be correct if no proper voltage information.

Each signal, power and ground PAD needs to have its own voltage text to recognize its operation voltage to perform latchup checking. The voltage text in each net needs to have “Voltage High” and “Voltage Low” information. The “Voltage High” means the max. operation voltage and “Voltage Low” is the min. operation voltage.

1. Three options can be used for voltage recognition in DRC.

For detailed description, please refer to chapter “DRC methodology of net voltage recognition”.

(a) Voltage text layer

- (i) “Voltage High” (84;230 for MP, 84;236 for MD, 31~44;230 for M1~M14, and 74;230 for AP)
- (ii) “Voltage Low” (84;231 for MP, 84;237 for MD, 31~44;231 for M1~M14, and 74;231 for AP)

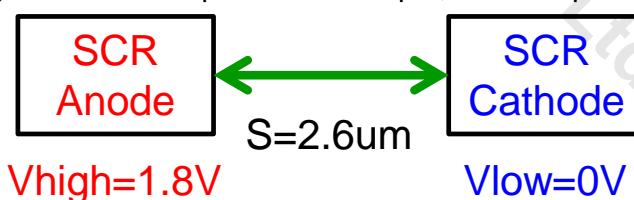
(b) Voltage marker layer

- (i) “Voltage High” (31~44;200~222 for M1~M14):

- o Voltage definition table of marker layers

Data Type	200	201	202	203	204	205	206	207	208	209	210	211
Voltage	0.0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1
Data Type	212	213	214	215	216	217	218	219	220	221	222	
Voltage	1.2	1.3	1.4	1.5	1.6	1.7	1.8	2.5	3.3	5.0	7.0	

- (ii) "Voltage Low": no support
 - (c) Default voltage recognized by layout drawing layer / strap.
2. For Power net, both "Voltage High" and "Voltage Low" information by voltage text layer are must. If the user doesn't provide "Voltage Low" information, the "Voltage Low" would be considered as "0V". Therefore, if no power-down mode (Power=0V) application in your chip, please remember to provide the "Voltage Low" information. For example, if your power net is always "1.8V", both "Voltage High" and "Voltage Low" need to be defined as "1.8V."
3. All voltage information need to be correct. Users need to take their own risk if applying wrong voltage information into latch-up checking.
4. DRC checking flow of the delta voltage LUP rule
- (a) Need to find the voltage rating for all devices connected to "PAD" directly.
 - (b) Calculate the voltage drop among P-diode, N-diode, NW/NSTRAP, PMOS and NMOS.
 - i. Classify:
 - 1) SCR Anode: PMOS/P-diode(P-Active OD) connect to VDD/VSS PAD
 - 2) SCR Cathode: NMOS/N-diode (N-Active OD) connect to VDD/VSS PAD
 - 3) IO SCR Anode: PMOS/P-diode(P-Active OD) connect to IO PAD
 - 4) IO SCR Cathode: NMOS/N-diode (N-Active OD) connect to IO PAD
 - 5) NW SCR Cathode: Any NW directly connected to VDD/VSS PAD
 - 6) RW SCR Anode : Any RW in DNW directly connected to VDD/VSS PAD
 - ii. Latch_up checking
 - 1) $\{(\text{IO , RW}) \text{ SCR Anode}' \text{ voltage} - (\text{IO , NW}) \text{ SCR Cathode's voltage}\} > 0 \rightarrow \text{Perform checking}$
 - 2) $\{(\text{IO , RW}) \text{ SCR Anode}' \text{ voltage} - (\text{IO , NW}) \text{ SCR Cathode's voltage}\} \leq 0 \rightarrow \text{Don't perform checking}$
 - 3) "(IO , RW) SCR Anode" will take "voltage high" and "(IO , NW) SCR Cathode" will take "voltage low" for latch-up checking.
 - iii. The voltage drop between "(IO , RW) SCR Anode" and "(IO , NW) SCR Cathode" will decide the latch-up spacing rule. For example: 1.8V \rightarrow 2.6 μm , 2.5V \rightarrow 4 μm .



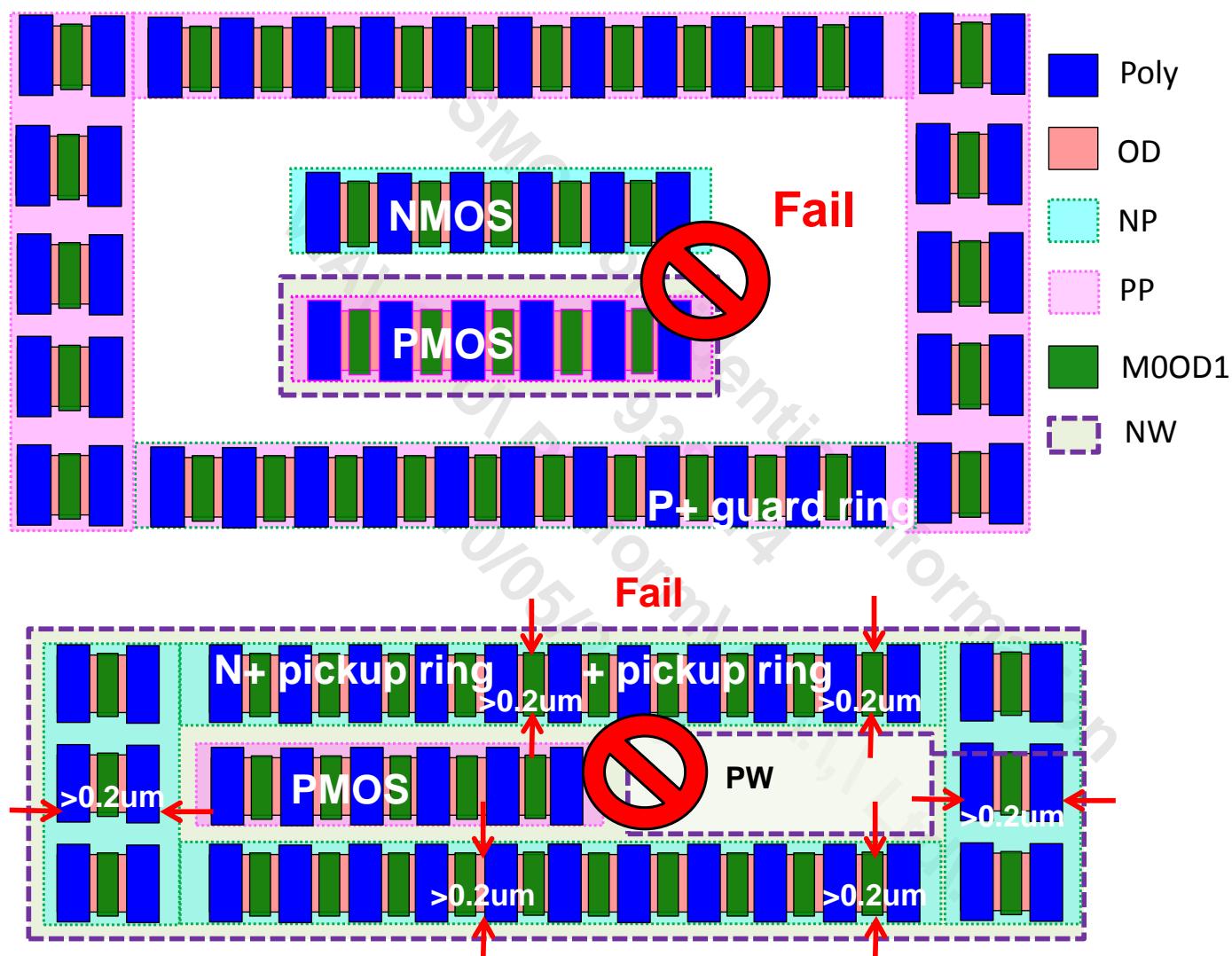
9.1.2.3.6 DRC methodology for LUP.1

OD injector is defined by any OD directly connected to I/O pad.

Ex. MOS, and STI diode (STI bonded) directly connected I/O PAD.

1. When an OD injector is covered by LUPWDMY (255;1), it is excluded by DRC from LUP.1 check.

2. The guard ring can not be shared by different type devices.



9.1.2.3.7 DRC methodology for LUP.2

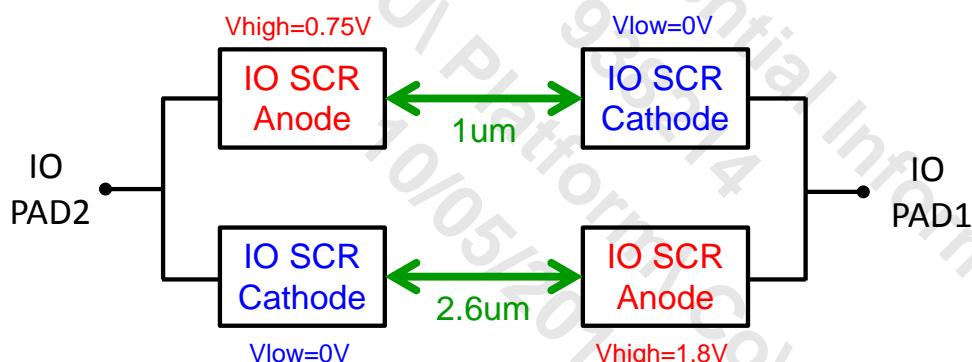
DRC use the following features to detect the devices for LUP.2:

1. The MOS OD within 15 μm space from the OD injector for LUP.1 check
2. The following cases are excluded:
 - I. The MOS OD is floating and does not connect to any VC, MP.
 - II. The MOS OD is covered by LUPWDMY (255;1).

9.1.2.3.8 DRC methodology for LUP.3 group

DRC use the following features to detect the devices for LUP.3 group:

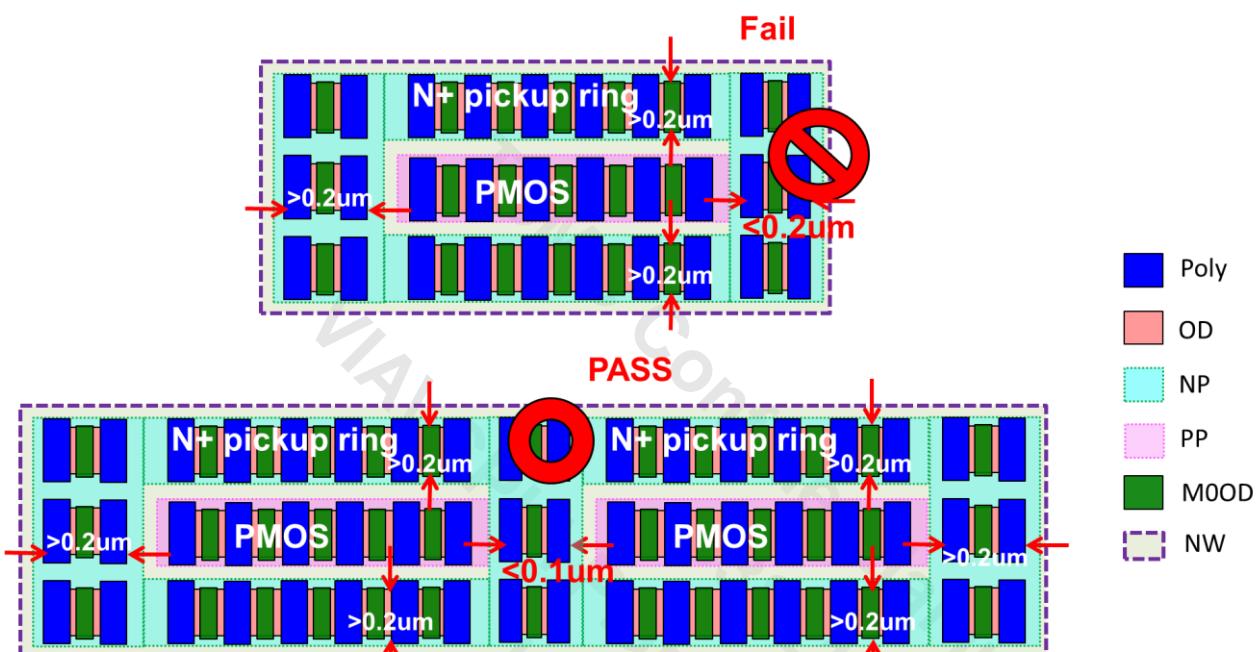
1. Voltage text usage is the same as described in section 9.1.2.3.5
2. DRC recognize the "IO SCR Anode" and "IO SCR Cathode" and their voltage information.
3. Check the spacing between "IO SCR Anode" and "IO SCR Cathode" per their voltage difference.
4. "IO SCR Anode" and "IO SCR Cathode" connected to the same IO PAD would not be checked in DRC.
5. The excluded cases are "I" and "II" in LUP.2.



9.1.2.3.9 DRC methodology for LUP.4

DRC use the following features to check the guard-ring width.

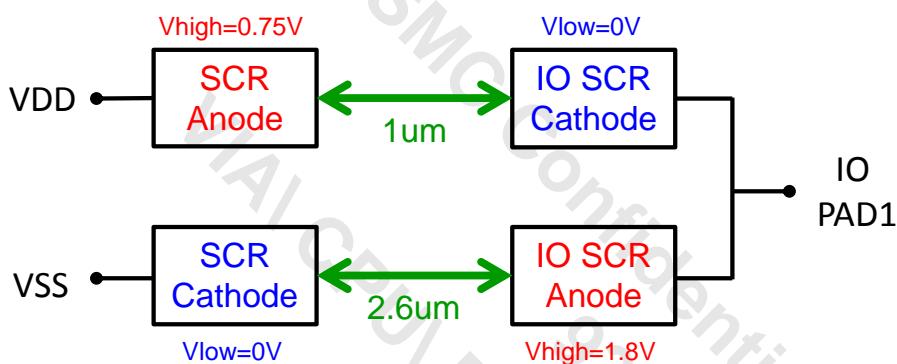
1. Find out the OD injector for LUP.1 & LUP.2 check.
2. The devices should be placed inside a complete guard-ring with width $\geq 0.218 \mu\text{m}$.



9.1.2.3.10 DRC methodology for LUP.5 group

DRC use the following features to detect the devices for LUP.5 group:

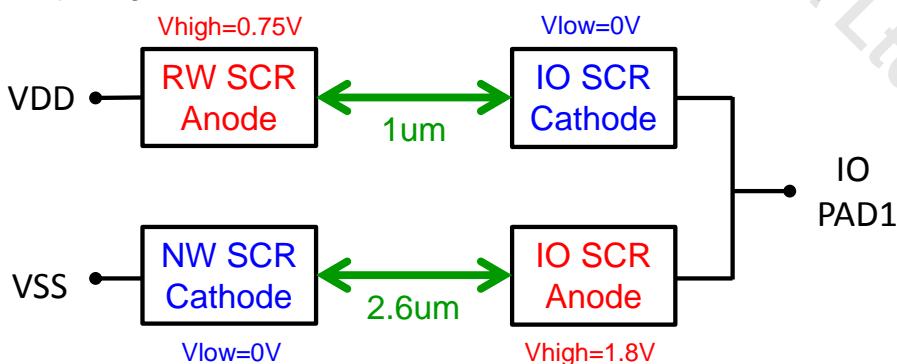
1. Voltage text usage is the same as described in section 9.1.2.3.5.
2. DRC recognize the "IO SCR Anode", "IO SCR Cathode", "SCR Anode", and "SCR Cathode" and their voltage information.
3. Check the spacing between "IO SCR Anode" and "SCR Cathode" per their voltage difference.
Measure the spacing between "SCR Anode" and "IO SCR Cathode" referring to their voltage difference.
4. The excluded cases are "I" and "II" in LUP.2.



9.1.2.3.11 DRC methodology for LUP.5.6 group

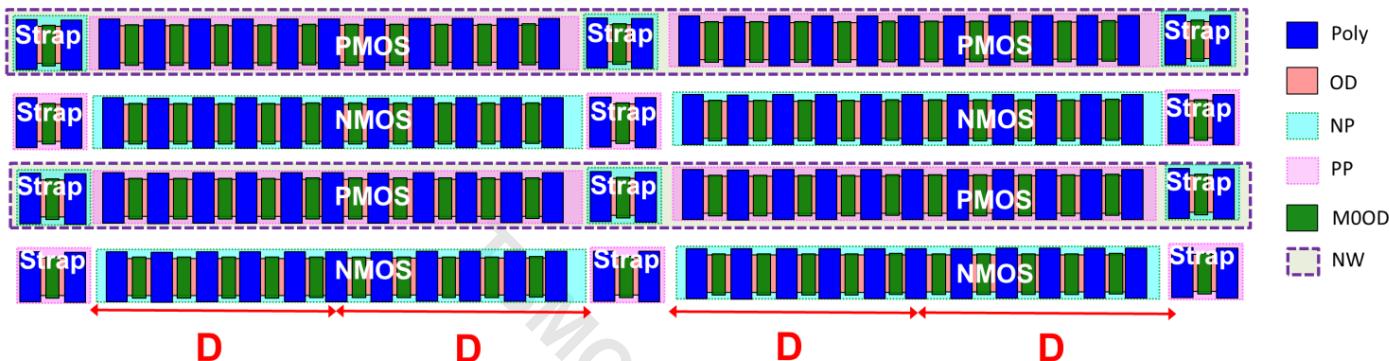
DRC use the following features to detect the devices for LUP.5.6 group:

1. Voltage text usage is the same as described in section 9.1.2.3.5
2. DRC recognize the "IO SCR Anode", "IO SCR Cathode", "RW SCR Anode", and "NW SCR Cathode" and their voltage information.
3. Check the spacing between "IO SCR Anode" and "NW SCR Cathode" per their voltage difference.
Check the spacing between "RW SCR Anode" and "IO SCR Cathode" per their voltage difference.



9.1.2.3.12 DRC methodology for LUP.6 group

For all NMOS and PMOS, the pick-up STRAP spacing rule need to be smaller than $2*D$.



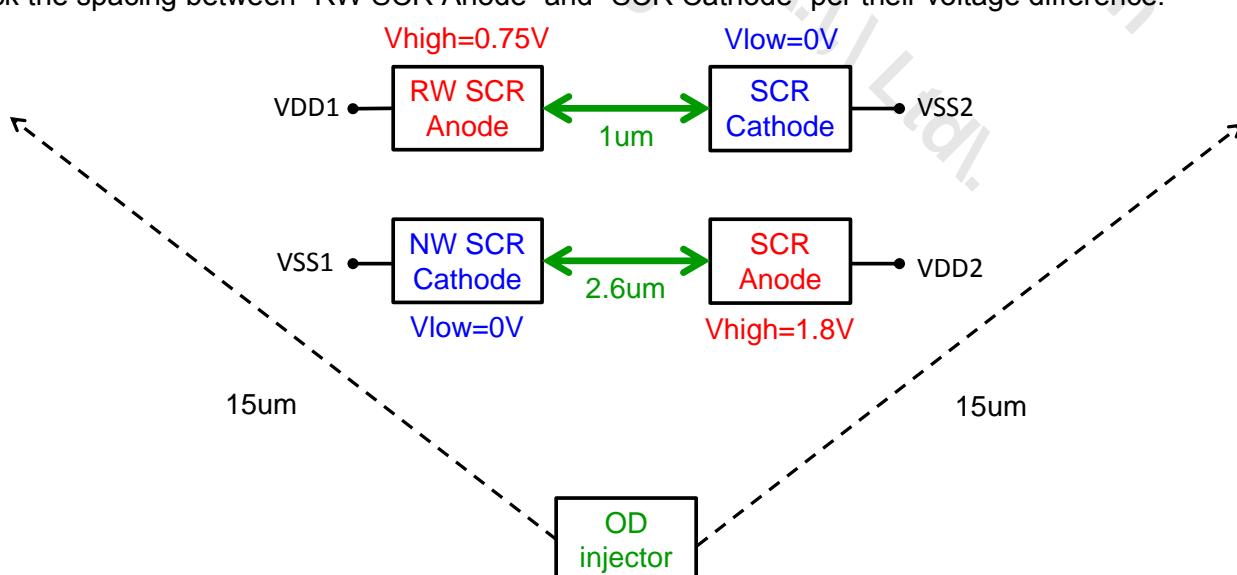
D is defined in LUP.6:

- “1. Any point inside NMOS source/drain {(N+ ACTIVE INTERACT TrGATE) NOT PO} SPACE to the nearest PW STRAP in the same PW.”
- 2. Any point inside PMOS source/drain {(P+ ACTIVE INTERACT TrGATE) NOT PO} SPACE to the nearest NW STRAP in the same NW.”

9.1.2.3.13 DRC methodology for LUP.7.6 group

DRC use the following features to detect the devices for LUP.7.6 group:

1. Voltage text usage is the same as described in section 9.1.2.3.5
 2. Checking window is 15 μm away from OD injector.
 3. DRC recognizes the “SCR Anode”, “SCR Cathode”, “RW SCR Anode”, and “NW SCR Cathode” and their voltage information.
 4. Check the spacing between “SCR Anode” and “NW SCR Cathode” per their voltage difference.
- Check the spacing between “RW SCR Anode” and “SCR Cathode” per their voltage difference.



9.1.2.3.14 DRC methodology for high/medium/medium-low/low and ultra-low noise OD injector

Definition of OD injectors with different noise level

1. For signal pins which overshoot/undershoot swing is controlled under a certain level (JESD78D), they will not inject significant current easily into substrate. The detail judgement criteria and example application for OD injectors with different noise level are listed below.

OD injector	Judgment criteria	Typical pin voltage	Example application
High noise pin	Overshoot/undershoot swing: $> +/-0.99V$	$>1.98V$	eg. 3.3V I/O
Med noise pin	Overshoot/undershoot swing: $\leq +/-0.99V$	$1.98V \rightarrow 1.65V$	eg. 1.8V I/O
Med-Low noise pin	Overshoot/undershoot swing: $\leq +/-0.825V$	$1.65V \rightarrow 1.32V$	eg. 1.5V & 1.35V I/O
Low noise pin	Overshoot/undershoot swing: $\leq +/-0.66V$	$1.32V \rightarrow 0.66V$	eg. 1.2V I/O
Ultra-Low noise pin	Overshoot/undershoot swing: $\leq +/-0.33V$	$\leq 0.66V$	eg. 0.6V I/O

DRC methodology

1. By default, all of OD injectors would be considered as “high-noise OD injector” and required to follow all of latch-up rules.
2. If the signal pins are with low injection current in system operation and low risk during latch-up testing (JESD78D), they can be defined as “low noise pins” or “ultra-low noise pins” and the OD injector connected to these pins would be defined as low or ultra-low noise OD injectors. Similar concept applies to medium and medium-low pins.

For low or ultra-low noise OD injectors, the specific latch-up rules can be waived. As for medium and medium-low OD injectors, some of latch-up rules can be relaxed.

For details, please refer to section 9.1.2.2.5.

Note that, for HIANMOS (N+ ACTIVE INTERACT SDI_2) and well diodes (NW/RWSTRAP) OD injectors, its noise level does not purely judge by voltage swing.

- If their swing is controlled under certain level (i.e. $\leq +/-0.99V$, connected to medium/med-low/low or ultra-low noise pin), single stage HIANMOS is defined as **medium noise** OD injector; cascaded HIANMOS and NW/RW diodes (NWSTRAP/RWSTRAP) are defined as **high noise** OD injector.
- If their swing very high (i.e. $> +/-0.99V$, connected to high noise pin), single stage HIANMOS, cascaded HIANMOS and NW/RW diodes (NWSTRAP/RWSTRAP) are defined as **high noise** OD injector.

3. In DRC, there are three methods to recognize OD injector with different noise level. In both IP level and chip level check, the noise level tagged by pin text (Method III) is with highest priority, which can overwrite the one tagged by CAD layers (Method I and II). As for priority between Method I and Method II, they are set as equal.

Method I: Cover CAD layer on M1 of specific OD injector. (For details, refer to Section 9.1.2.2 Latch-up Dummy Layers Summary)

Method II: Cover CAD layer on CB, CB2 or UBM of specific signal bumps. (For details, refer to Section 9.1.2.2 Latch-up Dummy Layers Summary)

Method III: Input pin name into DRC command file. This function is disabled by default. To enable it, users need to turn on “DEFINE_PAD_BY_TEXT” switch, enable specific variables and input the pin name.

OD injector recognition	Method I	Method II	Method III
High noise OD injector	--	--	HIGH_NOISE_PAD_TEXT
Medium noise OD injector	LUP18VIEDMY (255;66)	LUP18VIEDMY_BUMP (255;63)	MED_NOISE_PAD_TEXT
Medium-Low noise OD injector	LUP15VIEDMY (255;65)	LUP15VIEDMY_BUMP (255;62)	MED_LOW_NOISE_PAD_TEXT
Low noise OD injector	LUPVIEDMY (255;58)	LUPVIEDMY_BUMP (255;60)	LOW_NOISE_PAD_TEXT
Ultra-Low noise OD injector	LUPULVIEDMY (255;67)	LUPULVIEDMY_BUMP (255;68)	ULTRA_LOW_NOISE_PAD_TEXT

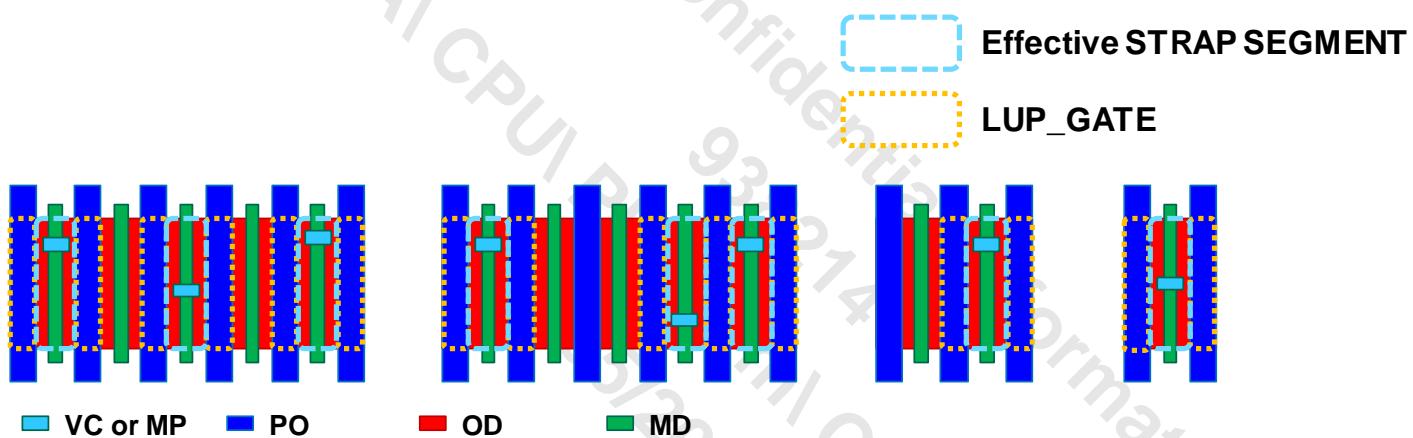
4. For signal pins without any noise level information, it is treated as high noise signal pin. When multiple noise level information is tagged on single signal pin, the most conservative one is taken. It is highly recommended to define noise level for all signal pins by pin text in DRC command file to avoid unexpected checking results.

	Information tagging scenario	OD injector noise level recognized in DRC
OD injector (signal pin) Noise level recognition	Without any noise level information	High noise
	With only one noise level information	High, Medium, Medium-low, Low, or Ultra-low (depends on the information tagged)
	With multiple noise level information	<p><u>Purely by Pin text or CAD layer:</u></p> <p>High + Medium + Medium-low + Low + Ultra-low → High Medium + Medium-low + Low + Ultra-low → Medium Medium-low + Low + Ultra-low → Medium-low Low + Ultra-low → Low</p> <p><u>By both pin text and CAD layer:</u></p> <p>High (pin text) + Medium (CAD layer on M1) → High High (pin text) + Medium (CAD layer on bump) → High High (CAD layer on M1) + Medium (CAD layer on bump) → High High (CAD layer on bump) + Medium (CAD layer on M1) → High High (CAD layer on M1) + Medium (pin layer) → Medium High (CAD layer on bump) + Medium (pin layer) → Medium</p>

9.1.2.3.15 DRC methodology for LUP STRAP

Definition of LUP STRAP

- DRC take effective STRAP_SEGMENT only.
- Effective STRAP_SEGMENT should be connected to VC or MP through (MD NOT CMD).
- STRAP_SEGMENT = {NWSTRAP OR PWSTRAP} NOT PO
- LUP STRAP = {effective STRAP_SEGMENT OR LUP_GATE}
- LUP_GATE = GATE INTERACT effective STRAP_SEGMENT
- If some of the STRAP SEGMENTS are lack of connection to VC or MP, they would be treated as invalid STRAP_SEGMENT and being dropped in LUP STRAP density calculation and related ACTIVE to LUP STRAP space check.
- This methodology applies to LUP.2.2, LUP.2.3, LUP.2.5, LUP.2.6, LUP.6, LUP.6.1, LUP.6.2, LUP.13 group, LUP.13.1 group and LUP.13.2 group.



9.1.2.4 Layout Rules and Guidelines for Latch-up Prevention

The LUP rules are for design reference to achieve the specifications proposed by TSMC. They are extracted by the standard digital I/O and Area I/O test structures. Note that Latch-up free can not be guaranteed for all applications such as substrate bias condition, floating body circuits, SCR ESD IPs, etc. The P+ pick-up strap density between OD injectors /NW/RW should be as much as possible.

Table 9.1.1 Layout Rules and Guidelines for Latch-up Prevention

Rule No.	Description	Label	Op.	Rule
LUP.WARN.1	Voltage high text or voltage marker layer must exist in bond pad in chip level. (Except SEALRING_ALL) When turn on option "define_pad_by_text," DRC checks voltage text on power/ground/signal virtual pad for IP level and all of bond pad for chip level. When turn off option "define_pad_by_text," DRC checks this rule only when it is chip level.			
LUP.WARN.2	Delta V > 5.5V between any SCR Anode and SCR Cathode is not allowed.			
LUP.WARN.3 ^U	For LUP OD injector blocking purpose, RES200 should be covered on resistors between IOPAD and Ground nets.			
LUP.WARN.3.1 ^U	For LUP OD injector blocking purpose, RES200 should be covered on resistors between IOPAD and Power nets.			
LUP.WARN.4 ^U	For LUP OD injector blocking purpose, the resistor between internal device and IOPAD should be high resistance ($R \geq 200\text{ohm}$) with RES200. The internal device includes all devices except gate of MOS and high-R resistor (rhim).			
LUP.WARN.5	All {STRAP NOT PO} should be connected to VC or MP through (MD NOT CMD). (Except SRM) (This rule is enabled when the option "LUP_SANITY_CHECK" is switched on.)			
LUP.1	Any N+ OD injector or a N+ OD injector cluster must be surrounded by a P+ guard-ring (P+ pick-up ring) (Except IBJTDMY (110;3), and LUPIEDMY (255;56)).(Figure 9.1.9) Any P+ OD injector or a P+ OD injector cluster must be surrounded by a N+ guard-ring (N+ pick-up ring) (Except IBJTDMY (110;3), and LUPIEDMY (255;56)).(Figure 9.1.9) Please also refer to LUP.14 ^U for further information. It is not recommended to use LUPIEDMY before silicon proven.			
LUP.1.0.1 ^U	The N+ / P+ guard-ring for LUP.1 should be tied to power / ground accordingly. Except for the devices covered by IBJTDMY (110;3), or LUPIEDMY (255;56) Except for the devices/guard-rings covered by LUPWDMDY_IP (255;235). It is not recommended to use LUPIEDMY before silicon proven.			

Rule No.	Description	Label	Op.	Rule
LUP.1.1	<p>OD injector (INSIDE IBJTD MY (110;3)) must be surrounded by two guard-rings (NOT INSIDE IBJTD MY). And both of the guard-ring (NOT INSIDE IBJTD MY) widths must be $\geq 0.2180 \mu\text{m}$. (Figure 9.1.9.1)</p> <p>IBJT (INSIDE IBJTD MY) OD injector must be surrounded by P+ guard-ring or N+ guard ring (NOT INSIDE IBJTD MY) and that cannot contain internal IBJT or other devices (NOT INSIDE IBJTD MY).</p> <p>The first P+guard-ring (NOT INSIDE IBJTD MY) of IBJT (INSIDE IBJTD MY) OD injector must be surrounded by N+ guard ring.</p> <p>The first N+guard-ring (NOT INSIDE IBJTD MY) of IBJT (INSIDE IBJTD MY) OD injector must be surrounded by P+ guard ring.</p> <p>Different type of IBJT cannot share guard rings.</p>	E	\geq	0.2180
LUP.1.2	DNW {INTERACT P+ OD injector} must be surrounded by P+ guard ring. [OD width $\geq 0.2180 \mu\text{m}$] (Figure 9.1.9.2)			
LUP.1.3	Internal circuit exists between {DNW INTERACT P+ OD injector} and 1st P+ guard ring of DNW [surrounding {DNW INTERACT P+ OD injector}] is not allowed. (Figure 9.1.9.2)			
LUP.2	<p>Within 15 μm ($\leq 15 \mu\text{m}$) space from the OD injector, a P+ guard-ring (P+ pick-up ring) is required to surround an N+ ACTIVE OD or an N+ ACTIVE OD cluster. And an N+ guard-ring (N+ pick-up ring) is required to surround a P+ ACTIVE OD or a P+ ACTIVE OD cluster (Figure 9.1.13)</p> <p>(Checking window is also recognized by cad layer LUP_015U when the option "IP_LEVEL_LUP_CHECK" is switched on.)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. ACTIVE OD not connect to VC or MP b. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to ultra-low noise signal pin. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14.c. OD injectors covered by LUPIED MY (255;56). It is not recommended to use LUPIED MY before silicon proven. 			
LUP.2.0.1 ^U	<p>The N+ / P+ guard-ring for LUP.2 should be tied to power / ground accordingly.</p> <p>Exception:</p> <ul style="list-style-type: none"> a. ACTIVE OD not connect to VC or MP b. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to ultra-low noise signal pin. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. c. OD injectors covered by LUPIED MY (255;56). It is not recommended to use LUPIED MY before silicon proven. d. Devices/Guard-rings covered by LUPWD MY_IP (255;235). 			
LUP.2.1 ^U	<p>Within 15 μm ($\leq 15 \mu\text{m}$) space from the OD injector, an P+ACTIVE in proximity to another NW and with the relative higher potential to another NW, a PWSTRAP is required to be inserted between P+ ACTIVE to another NW. (Figure 9.1.13)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. ACTIVE OD not connect to VC or MP b. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to ultra-low noise signal pin. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. c. Devices/Straps covered by LUPWD MY_IP (255;235). 			

Rule No.	Description	Label	Op.	Rule
LUP.2.2	<p>Minimum LUP PWSTRAP density within 15 μm of {(HIADMY INTERACT P+ OD injector) OR (RWSTRAP OD injector)}, using window 10 $\mu\text{m} \times 10 \mu\text{m}$ with stepping 5 μm. (This rule only apply while the area of {checking window} \geq 1/2 window area.) (LUP.2.2 would be tighten to 6% with adjusted checking stepping, 0.2 μm, if turning on “ESDLU_IP_TIGHTEN_DENSITY”) (Checking window is also recognized by cad layer LUP_015U when the option “IP_LEVEL_LUP_CHECK” is switched on.)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. If the summation of Active OD density and LUP PWSTRAP density is \geq 25%, LUP.2.2 can be excluded. b. If the LUP NWSTRAP OD density is \geq 25%, LUP.2.2 can be excluded. c. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to low/ultra-low noise signal pin. For the detail of low/ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. d. If OD injector is covered by LUPIEDMY, LUP.2.2 can be excluded. (It is not recommended to use this layer before silicon proven). e. Regions covered by LUPDWDMDY are excluded from checking window. f. Triangle empty areas at 4 chip corners / SEALRING_ALL are excluded from checking window. 		\geq	5%
LUP.2.3	<p>Minimum LUP NWSTRAP density within 15 μm of {(HIADMY INTERACT N+ OD injector) OR ((N+ OD injector INTERACT SR_ESD) sizing up/down 0.851 μm) OR (NWSTRAP OD injector)}, using window 10 $\mu\text{m} \times 10 \mu\text{m}$ with stepping 5 μm. (This rule only apply while the area of {checking window} \geq 1/2 window area.) (LUP.2.3 would be tighten to 3.5% with adjusted checking stepping, 0.2 μm, if turning on “ESDLU_IP_TIGHTEN_DENSITY”) (Checking window is also recognized by cad layer LUP_015U when the option “IP_LEVEL_LUP_CHECK” is switched on.)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. If the summation of Active OD density and LUP NWSTRAP density is \geq 25%, LUP.2.3 can be excluded. b. If the LUP PWSTRAP OD density is \geq 25%, LUP.2.3 can be excluded. c. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to low/ultra-low noise signal pin. For the detail of low/ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. d. If OD injector is covered by LUPIEDMY, LUP.2.3 can be excluded. (It is not recommended to use this layer before silicon proven). e. Regions covered by LUPDWDMDY are excluded from checking window. f. Triangle empty areas at 4 chip corners / SEALRING_ALL are excluded from checking window. 		\geq	2.5%
LUP.2.4	<p>OD injector {INTERACT {HIADMY OR SR_ESD}} to the IP boundary distance is required to be larger than or equal to 15 μm (LUP.2.4 would be checked by turning on “IP_LEVEL_LUP_CHECK”)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. If OD injector is covered by LUPIEDMY, LUP.2.4 can be excluded. (It is not recommended to use this layer before silicon proven). b. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to ultra-low noise signal pin. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. 	S	\geq	15

Rule No.	Description	Label	Op.	Rule
LUP.2.5	<p>Minimum LUP PWSTRAP density within 75 μm of {(HIADMY INTERACT P+ OD injector) OR (RWSTRAP OD injector)}, using window 10 $\mu\text{m} \times 10 \mu\text{m}$ with stepping 5 μm.</p> <p>(This rule only apply while the area of {checking window} \geq 1/2 window area.)</p> <p>(LUP.2.5 checking stepping would be adjusted, 0.2 μm, if turning on "ESDLU_IP_TIGHTEN_DENSITY")</p> <p>(Checking window is also recognized by cad layer LUP_015U, LUP_045U, LUP_075U, LUP_045U_18V, LUP_075U_18V, LUP_045U_15V and LUP_075U_15V when the option "IP_LEVEL_LUP_CHECK" is switched on.)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. If the summation of Active OD density and LUP PWSTRAP density is \geq 10%, LUP.2.5 can be excluded. b. If the LUP NWSTRAP OD density is \geq 10%, LUP.2.5 can be excluded. c. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to low/ultra-low noise signal pin. For the detail of low/ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. d. If OD injector is covered by LUPIEDMY, LUP.2.5 can be excluded. (It is not recommended to use this layer before silicon proven). e. Regions covered by {LUPDWDMDY OR RH_TNB} are excluded from checking window. f. Triangle empty areas at 4 chip corners / SEALRING_ALL are excluded from checking window. 		\geq	0.1%
LUP.2.6	<p>Minimum LUP NWSTRAP density within 75 μm of {(HIADMY INTERACT N+ OD injector) OR ((N+ OD injector INTERACT SR_ESD) sizing up/down 0.851 μm) OR (NWSTRAP OD injector)}, using window 10 $\mu\text{m} \times 10 \mu\text{m}$ with stepping 5 μm.</p> <p>(This rule only apply while the area of {checking window} \geq 1/2 window area.)</p> <p>(LUP.2.6 checking stepping would be adjusted, 0.2 μm, if turning on "ESDLU_IP_TIGHTEN_DENSITY")</p> <p>(Checking window is also recognized by cad layer LUP_015U, LUP_045U, LUP_075U, LUP_045U_18V, LUP_075U_18V, LUP_045U_15V and LUP_075U_15V when the option "IP_LEVEL_LUP_CHECK" is switched on.)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. If the summation of Active OD density and LUP NWSTRAP density is \geq 10%, LUP.2.6 can be excluded. b. If the LUP PWSTRAP OD density is \geq 10%, LUP.2.6 can be excluded. c. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to low/ultra-low noise signal pin. For the detail of low/ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. d. If OD injector is covered by LUPIEDMY, LUP.2.6 can be excluded. (It is not recommended to use this layer before silicon proven). e. Regions covered by {LUPDWDMDY OR RH_TNB} are excluded from checking window. f. Triangle empty areas at 4 chip corners / SEALRING_ALL are excluded from checking window. 		\geq	0.1%
LUP.3.0	Space between "IO SCR Anode" and "IO SCR Cathode" needs to follow Table.9.1.1.1 if "IO SCR Anode" voltage potential > "IO SCR Cathode" voltage potential ($\Delta V > 0$).	A	\geq	Table 9.1.1.1
LUP.4	OD width of the N+ guard-ring (N+ pick-up ring) and P+ guard-ring (P+ pick-up ring) for the OD injector. (e. g. OD width of guard-ring (pick-up ring) of LUP.1) (Except IBJTDMY (110;3)) (Figure 9.1.9 and 9.1.11)	B	\geq	0.2180

Rule No.	Description	Label	Op.	Rule
LUP.4.1	<p>OD width of the N+ guard-ring (N+ pick-up ring) for P+ ACTIVE OD and P+ guard-ring (P+ pick-up ring) for N+ ACTIVE OD within 15 μm space from the OD injector. (e. g. OD width of guard-ring (pick-up ring) of LUP.2) (Figure 9.1.11)</p> <p>(Checking window is also recognized by cad layer LUP_015U when the option “IP_LEVEL_LUP_CHECK” is switched on.)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. ACTIVE OD not connect to VC or MP b. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to ultra-low noise signal pin. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. c. OD injectors covered by LUPIEDMY (255;56). It is not recommended to use LUPIEDMY before silicon proven. 	B1	\geq	0.0980
LUP.4.2 ^U	<p>OD width of the PWSTRAP for LUP.2.1^U. (Figure 9.1.11)</p> <p>Exception:</p> <ul style="list-style-type: none"> a. ACTIVE OD not connect to VC or MP b. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to ultra-low noise signal pin. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. c. Devices/Straps covered by LUPWDMY_IP (255;235). 	B2	\geq	0.0980
LUP.5.0	<p>Space between “IO SCR Anode” and “SCR Cathode” needs to follow Table.9.1.1.1 if “IO SCR Anode” voltage potential > “SCR Cathode” voltage potential ($\Delta V > 0$). (Figure.9.1.11)</p> <p>Space between “SCR Anode” and “IO SCR Cathode” needs to follow Table.9.1.1.1 if the “SCR Anode” voltage potential > “IO SCR Cathode” voltage potential ($\Delta V > 0$). (Figure.9.1.11)</p> <p>If the “IO SCR Anode” or “IO SCR Cathode” is covered by LUPIEDMY, LUP.5.0 can be exempted.</p> <p>It is not recommended to use LUPIEDMY before silicon proven.</p>	C	\geq	Table 9.1.1.1
LUP.5.6	<p>Space between “IO SCR Anode” and “NW SCR Cathode” needs to follow Table.9.1.1.1 if “IO SCR Anode” voltage potential > “NW SCR Cathode” voltage potential ($\Delta V > 0$). (Figure 9.1.11)</p> <p>Space between “RW SCR Anode” and “IO SCR Cathode” needs to follow Table.9.1.1.1 if the “RW SCR Anode” voltage potential > “IO SCR Cathode” voltage potential ($\Delta V > 0$).</p> <p>For below conditions, we will exempt them from LUP.5.6 checking.</p> <ol style="list-style-type: none"> 1. NW SCR cathode(N2) connects to the NW of (IO) SCR anode (N1) 2. RW SCR Anode (P1) connects to the PW of (IO) SCR cathode (P2) <p>If the “IO SCR Anode” or “IO SCR Cathode” is covered by LUPIEDMY, LUP.5.6 can be exempted.</p> <p>It is not recommended to use LUPIEDMY before silicon proven.</p>	C1	\geq	Table 9.1.1.1
LUP.6	<ol style="list-style-type: none"> 1. Any point inside NMOS source/drain {(N+ ACTIVE INTERACT TrGATE) NOT PO} SPACE to the nearest LUP PWSTRAP in the same PW. (Figure 9.1.12) 2. Any point inside PMOS source/drain {(P+ ACTIVE INTERACT TrGATE) NOT PO} SPACE to the nearest LUP NWSTRAP in the same NW. (Figure 9.1.12) <p>LUP PW(NW)STRAP should meet minimum fin number criteria for each of group, i.e. ≥ 4 fins. The LUP NW(PW) STRAP group means the LUP STRAPS with space $\leq 0.6 \mu\text{m}$ along same NW(PW) strait. DRC counts the total fin number in the same LUP STRAP group.</p> <p>Exception: ACTIVE OD not connect to VC or MP</p>	D	\leq	51

Rule No.	Description	Label	Op.	Rule
LUP.6.1	<p>1. Any point inside IO NMOS source/drain {{{(N+ ACTIVE INTERACT TrGATE) NOT PO) AND OD2} SPACE to the nearest LUP PWSTRAP in the same PW. (Figure 9.1.12)}</p> <p>2. Any point inside IO PMOS source/drain {{{(P+ ACTIVE INTERACT TrGATE) NOT PO) AND OD2} SPACE to the nearest LUP NWSTRAP in the same NW. (Figure 9.1.12)}</p> <p>LUP PW(NW)STRAP should meet minimum fin number criteria for each of group, i.e. ≥ 4 fins. The LUP NW(PW) STRAP group means the LUP STRAPS with space $\leq 0.6 \mu m$ along same NW(PW) strait. DRC counts the total fin number in the same LUP STRAP group. Exception: ACTIVE OD not connect to VC or MP</p>	D	\leq	25
LUP.6.2	<p>For SRAM:</p> <p>1. Any point inside NMOS source/drain {{{(N+ ACTIVE INTERACT TrGATE) NOT PO) AND {SRAMDMDY OR SRM}} SPACE to the nearest LUP PW STRAP in the same PW. (Figure 9.1.12)}</p> <p>2. Any point inside PMOS source/drain {{{(P+ ACTIVE INTERACT TrGATE) NOT PO) AND {SRAMDMDY OR SRM}} SPACE to the nearest LUP NW STRAP in the same NW. (Figure 9.1.12)}</p> <p>LUP PW(NW)STRAP should meet minimum fin number criteria for each of group, i.e. ≥ 4 fins. The LUP NW(PW) STRAP group means the LUP STRAPS with space $\leq 0.6 \mu m$ along same NW(PW) strait. DRC counts the total fin number in the same LUP STRAP group. Exception: ACTIVE OD not connect to VC or MP</p>	D	\leq	16
LUP.6.3	<p>1. Any point inside NMOS source/drain {{{(N+ ACTIVE INTERACT CPODE(206;32)) INTERACT TrGATE) NOT PO} SPACE to the nearest LUP PWSTRAP in the same PW. (Figure 9.1.12)}</p> <p>2. Any point inside PMOS source/drain {{{(P+ ACTIVE INTERACT CPODE(206;32)) INTERACT TrGATE) NOT PO} SPACE to the nearest LUP NWSTRAP in the same NW. (Figure 9.1.12)}</p> <p>The LUP PW(NW) STRAP to N+(P+) ACTIVE space requirement is dependent on “LUP STRAP group size”, “NW strait width” and application spec.</p> <p>a. The LUP NW(PW) STRAP group means the LUP STRAPS with space $\leq 0.6 \mu m$ along same NW(PW) strait. DRC counts the total fin number in the same LUP STRAP group. Total fin number for each of LUP STRAP = {{{(LUP STRAP vertical width - 0.008)/ 0.030 + 1} * (POLY count -1)}}.</p> <p>b. For the NW strait width judgment, it takes minimum width of NW. DRC considers NW strait width from where STRAP located to where N/PMOS placed.</p> <p>c. There are two DRC options, i.e. LUP_VTRIG_25C_1d60V and LUP_VTRIG_25C_1d55V, to control rule spec by application. By default, both options are turned on. For details ,please refer to Table.</p> <p>Exception: ACTIVE OD not connect to VC or MP</p>	D	\leq	Table 9.1.1.2

Rule No.	Description	Label	Op.	Rule
LUP.7.6	<p>For anode and cathode within 15 μm from OD injector, Space between “SCR Anode” and “NW SCR Cathode” needs to follow Table.9.1.1.1 if the “SCR Anode” voltage potential > “NW SCR Cathode” voltage potential ($\Delta V > 0$). (Figure 9.1.13)</p> <p>Space between “RW SCR Anode” and “SCR Cathode” needs to follow Table.9.1.1.1 if the “RW SCR Anode” voltage potential > “SCR Cathode” voltage potential ($\Delta V > 0$). (Figure 9.1.13)</p> <p>Space between “RW SCR Anode” and “NW SCR Cathode” needs to follow Table.9.1.1.1 if the “RW SCR Anode” voltage potential > “SCR Cathode” voltage potential ($\Delta V > 0$). (Figure 9.1.13)</p> <p>If the P+ OD injector covered by LUPIEDMY, LUP.7.6 can be excepted. For below conditions, we will exempt them from LUP.7.6 checking.</p> <ol style="list-style-type: none"> 1. NW SCR cathode(N2) connects to the NW of (IO) SCR anode (N1) 2. RW SCR Anode (P1) connects to the PW of (IO) SCR cathode (P2) 3. NW SCR Cathode (N2) connects to the NW of RW SCR Anode (N1) <p>Exception:</p> <p>a. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to ultra-low noise signal pin. For the detail of ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14.</p>	E1	\geq	Table 9.1.1.1

For delta voltage LUP rule checking, the voltage text is set as the rating operation voltage.

For LUP.3, LUP.5.0, LUP.5.6 and LUP.7.6 series rules, we use holding voltage (V_h) > supply power voltage criterion to define latchup spacing rules.

The supply power voltage criterion for V_h (use burn-in/HTOL condition as the criterion):

Core devices: $1.4 \times V_{DD}$

1.8V IO devices: $1.3 \times V_{DD}$

2.5/3.3V devices: $1.1 \times V_{DD}$

Table 9.1.1.1 Layout Space Rule for LUP.3.0, LUP.5.0, LUP.5.6, and LUP.7.6 groups

SPACE (Anode to Cathode) (um)	LUP.3.0 (A)	LUP.5.0 (C)	LUP.5.6 (C1)	LUP.7.6 (E1)
$0 < \Delta V \leq 1.115V (1.014V+10\%)$	1	1	1	1
$1.115V (1.014V+10\%) < \Delta V \leq 1.32V (1.2V +10\%)$	1.8	1.8	2	2
$1.32V (1.2V+10\%) < \Delta V \leq 1.65V (1.5V +10\%)$	2	2	3	3
$1.65V (1.5V+10\%) < \Delta V \leq 1.98V (1.8V +10\%)$	2.6	2.6	6	6
$1.98V (1.8V+10\%) < \Delta V \leq 2.75V (2.5V +10\%)$	4	4	9	9
$2.75V (2.5V+10\%) < \Delta V$	10	10	18	18

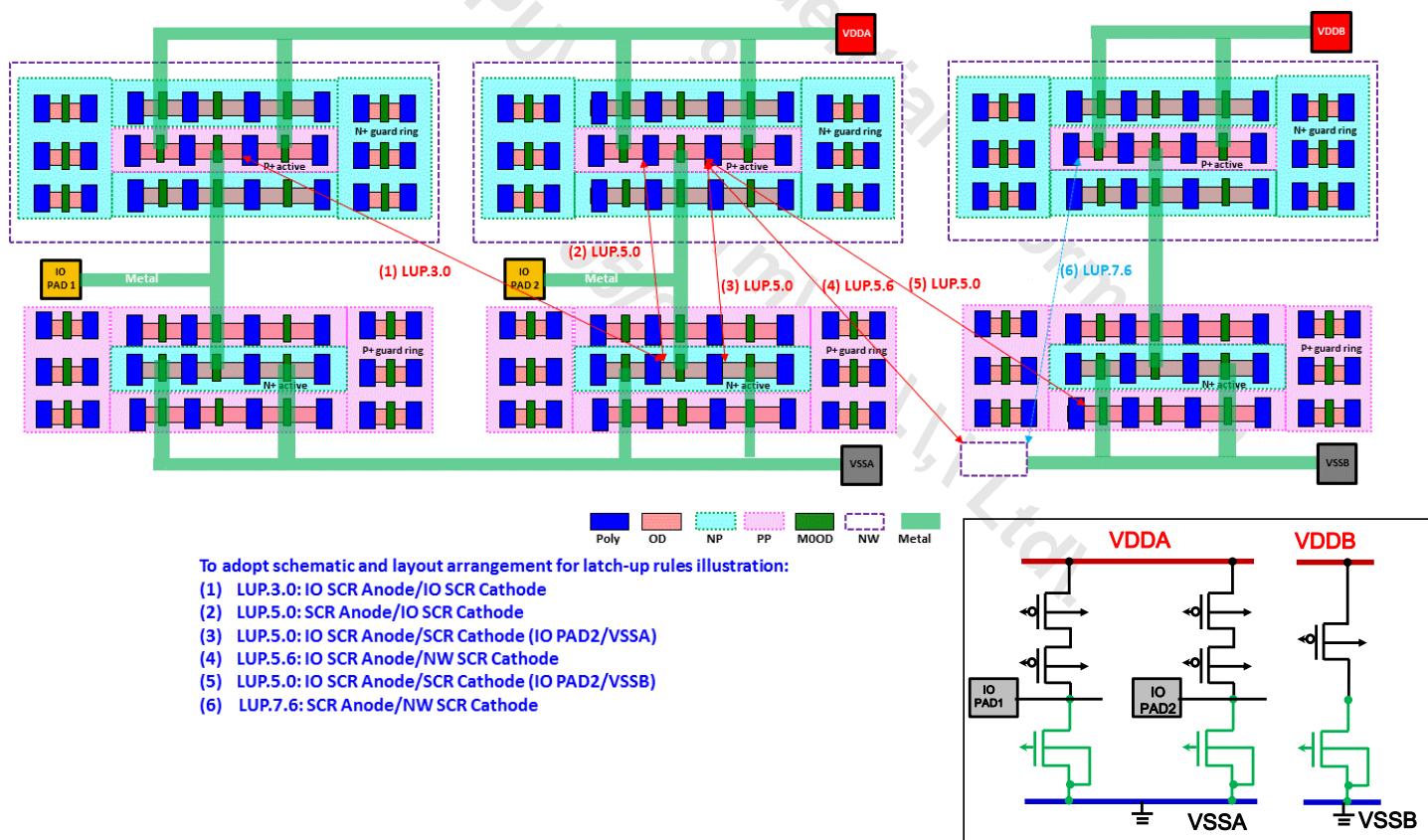


Figure 9.1.8 Layout arrangement vs. schematic for the latch-up rules illustration.

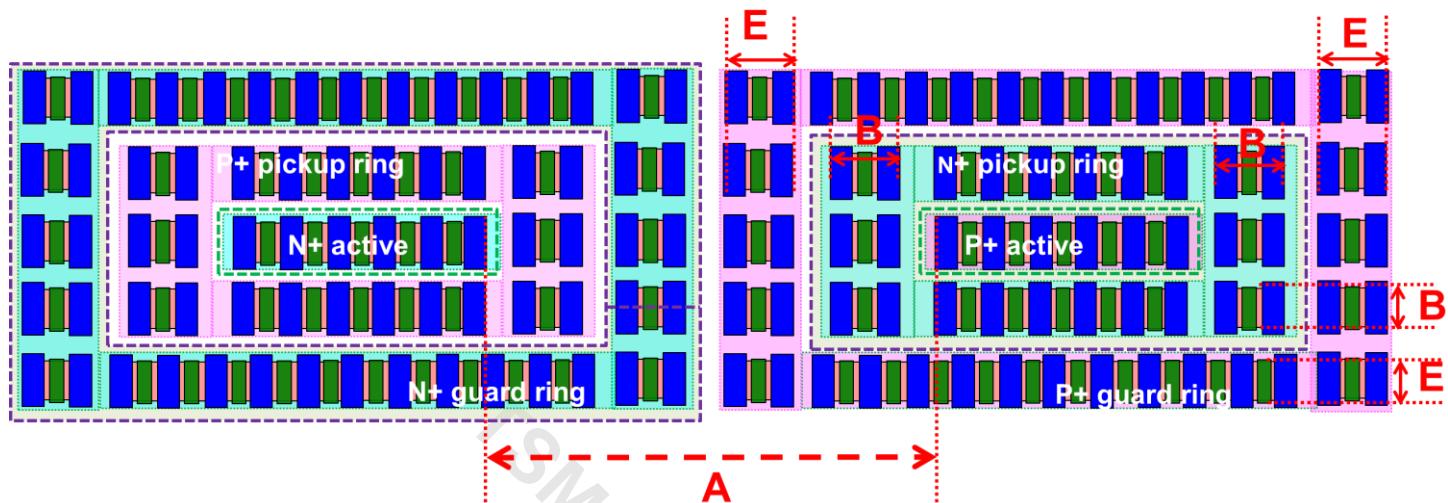


Figure 9.1.9 Latch-up prevention design for LUP.1, LUP.3.0, LUP.4 and LUP.14.

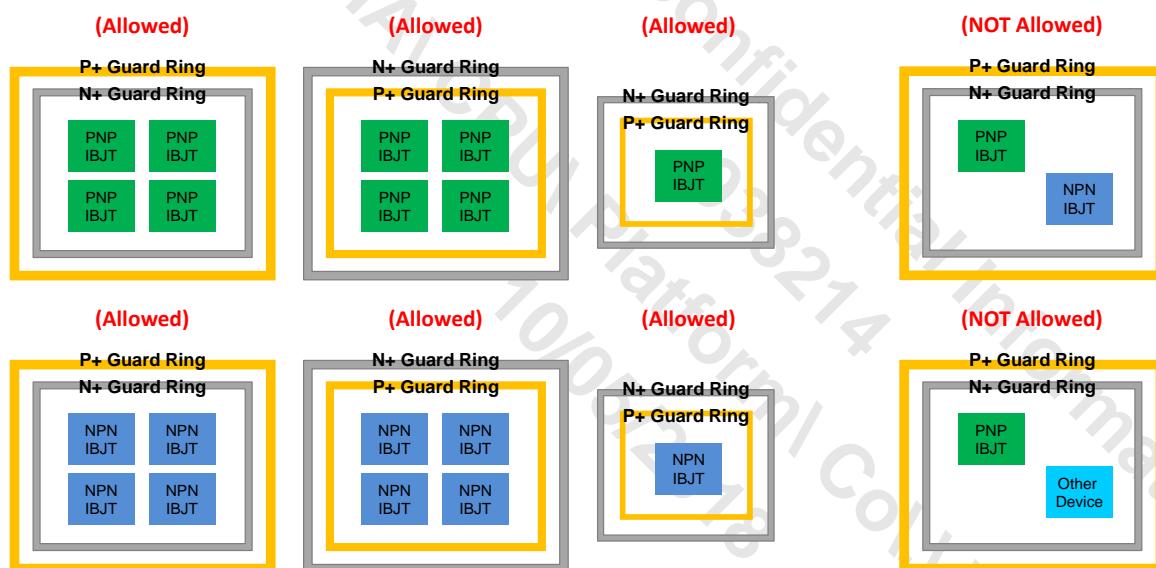


Figure 9.1.9.1 Surrounded rings example of LUP.1.1 for BJT

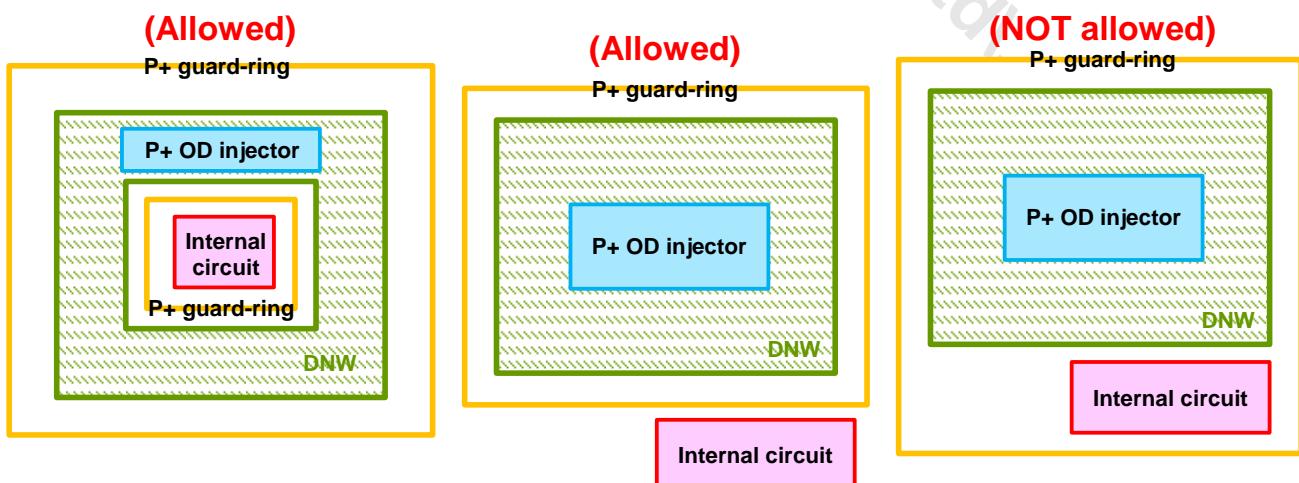


Figure 9.1.9.2 Surrounded P+ guard rings example of LUP.1.2 and LUP.1.3 for DNW.

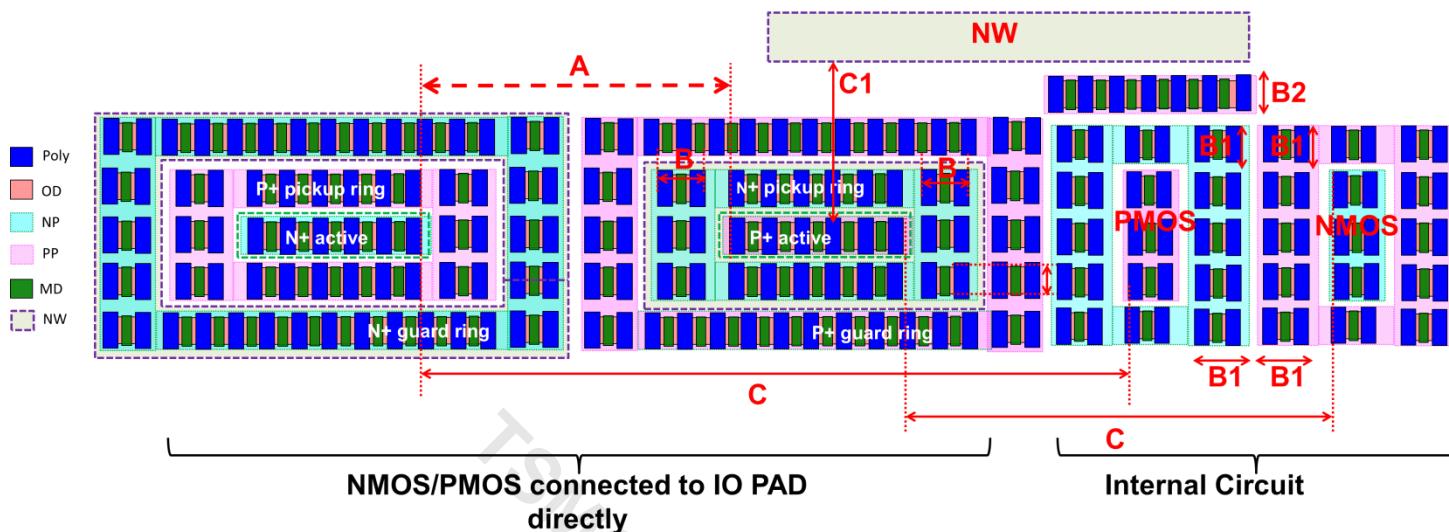


Figure 9.1.11 Latch-up prevention design for LUP.3.0, LUP.5.0 and LUP.5.6

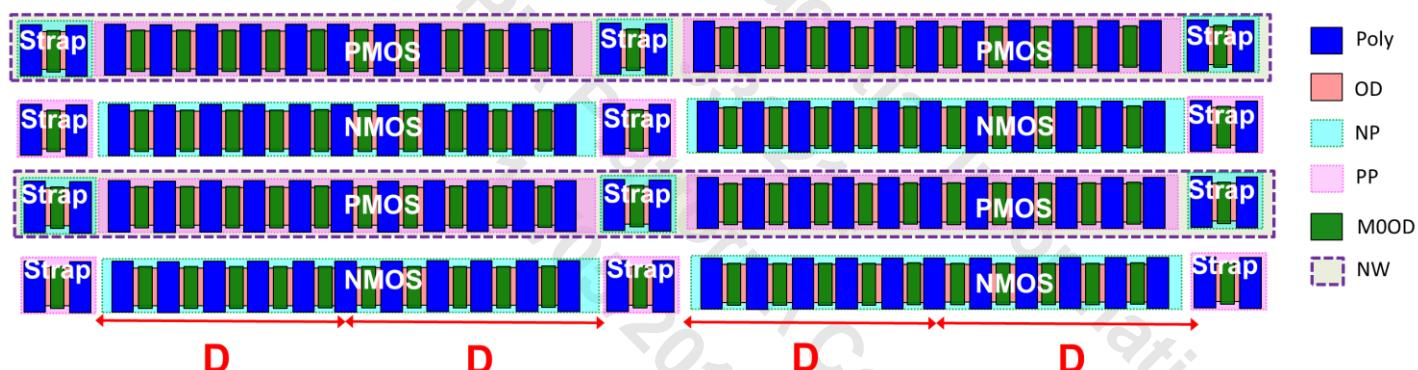


Figure 9.1.12 Latch-up prevention design for LUP 6, LUP.6.1 and LUP.6.2.

Table 9.1.1.2 Layout Space Rule for LUP.6.3 groups

Rule table for LUP.6 and LUP.CPODE.6	V-trigger @25C Temperature coefficient is 2.5mV/C						
	1.6V		1.55V		1.50V		
DRC option	LUP_VTRIG_25C_1d55V: on or off LUP_VTRIG_25C_1d60V: on	LUP_VTRIG_25C_1d55V: on LUP_VTRIG_25C_1d60V: off	LUP_VTRIG_25C_1d55V: off LUP_VTRIG_25C_1d60V: off	CPODE	PODE	CPODE	PODE
NW width: any	Tap OD: ≥4fins D≤26um		Tap OD: ≥4fins D≤37.5um	Tap OD: ≥4fins D≤51um		Tap OD: ≥4fins D≤51um	
	Tap OD: ≥8fins D≤51um			Tap OD: ≥8fins D≤51um			

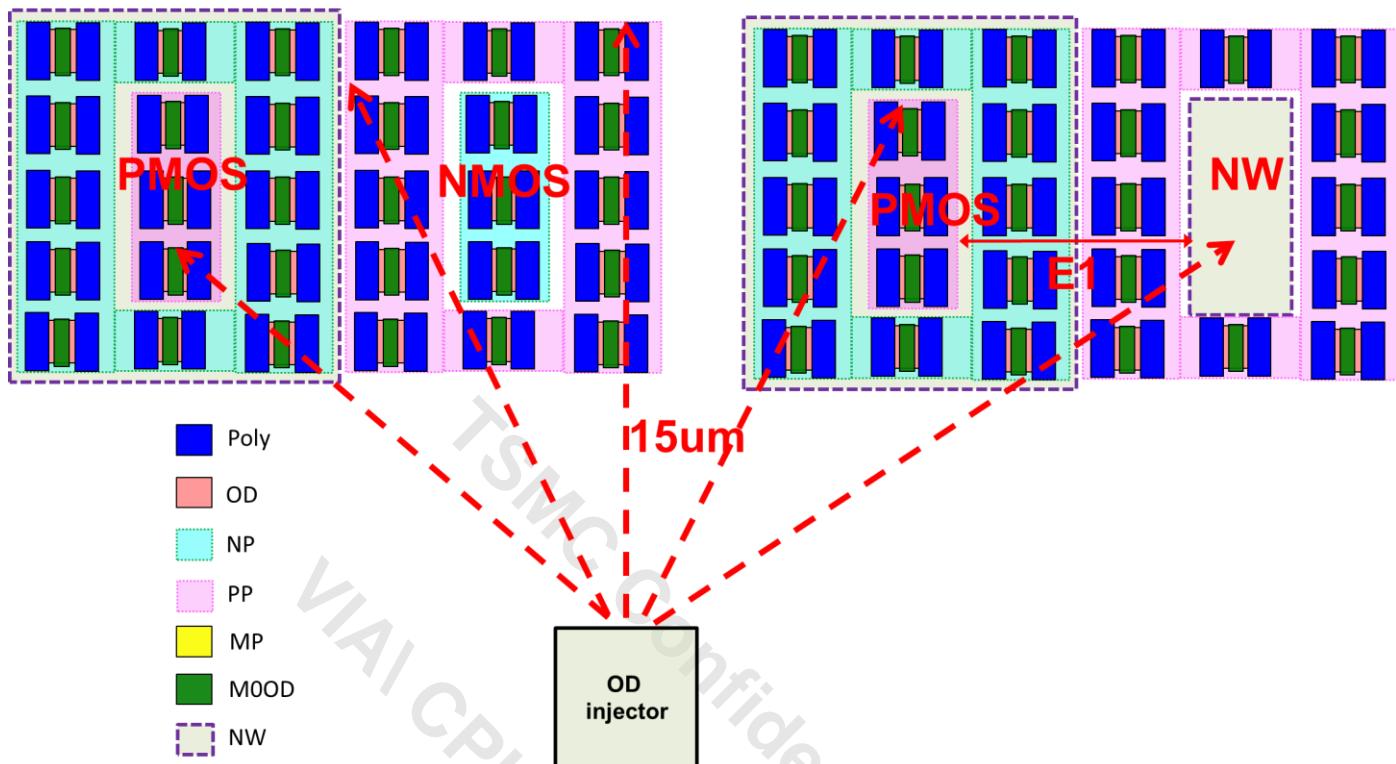


Figure 9.1.13 Latch-up prevention design for LUP 2, LUP.2.1 and LUP.7.6.

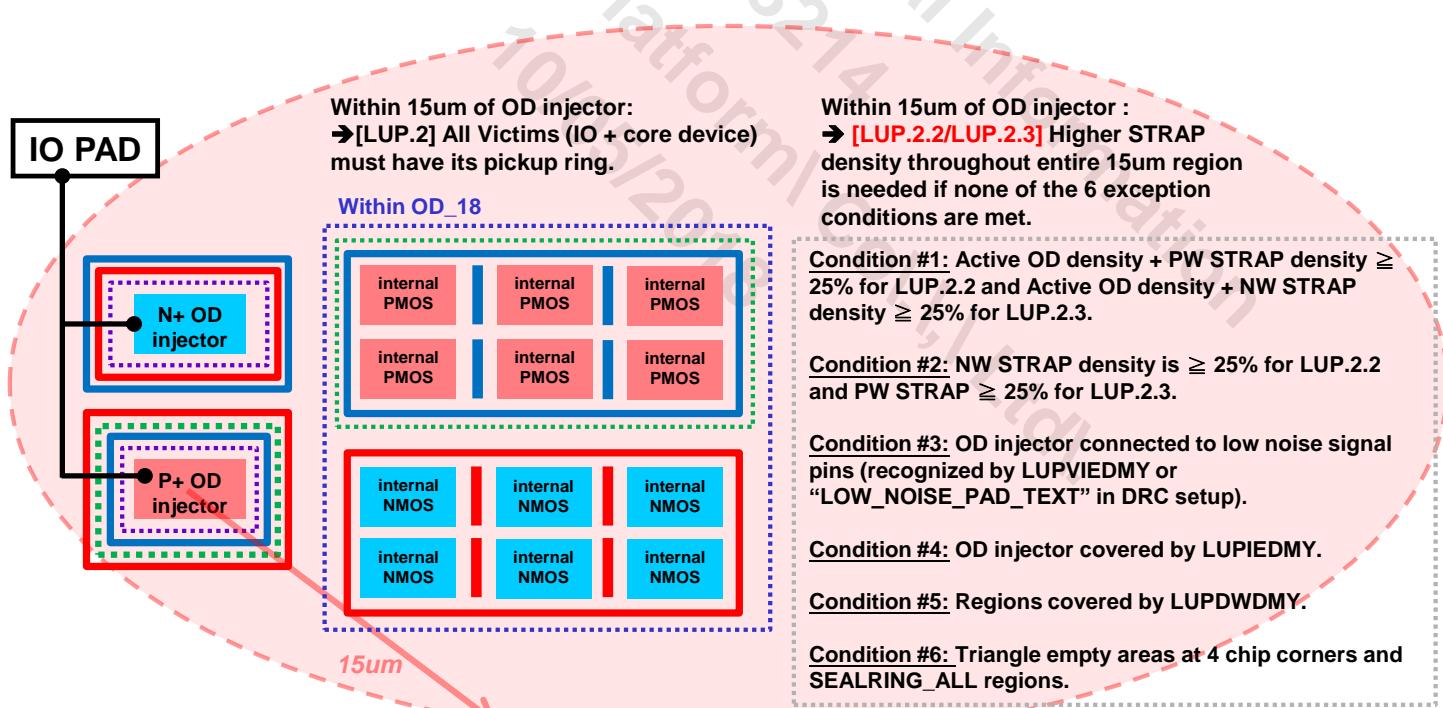


Figure 9.1.14 Latch-up prevention design for LUP.2.2 and LUP.2.3.

9.1.2.5 Layout Rules and Guidelines for Area I/O Latch-up Prevention

To increase the number or density of I/Os in VLSI designs, the Area-I/O is adopted to achieve smaller package size (such as flip-chip), shorter wire length, and better signal & power integrity. However, an external injection of minority carriers from an Area IO cell can trigger a latchup event easily in the parasitic pnpn path of the surrounding CMOS circuits in the chip's core area. The Area I/O cell is different from the peripheral type I/O ring, it does not have pre-driver structure between the post driver (carrier injector) and the core CMOS circuits, which can help absorb the substrate currents or carriers from an external injection. The AAIO latch-up rules need to be applied to the IO cells put in chip center and next to internal circuit. Fig 9.1.14 shows the schematic diagram of the Area I/O structure.

Two AAIO latchup DRC enablement options are available:

1) Switch-based (Regard whole chip IO as AAIO design):

“ALL_AREA_IO” DRC switch controls whether the entire chip will be checked for AAIO rules.

Usage:

“ALL_AREA_IO” is turned ON by default to enable whole chip AAIO check. After switching “ALL_AREA_IO” OFF, the AAIO DRC check would rely on LUPWDMY_2 (255;18) marker layer.

2) Marker CAD layer based (Regard specific IO which covered by LUPWDMY_2 as AAIO only):

“LUPWDMY_2 (255;18)” is a DRC dummy layer to trigger the AAIO latch-up rules check.

Usage:

Draw a LUPWDMY_2 pattern to fully cover the OD injector. However it is not necessary to cover the Well STRAP, or guard-ring. (Fig 9.1.15)

DRC switch of “ALL_AREA_IO”	OD injector covered by LUPWDMY_2 (255;18)	
	NO	YES
OFF	Follow standard LUP rules	Follow AAIO LUP rules
ON (Default DRC setting)	Follow AAIO LUP rules	Follow AAIO LUP rules

Table 9.2.1 Layout Rules and Guidelines for Area I/O Latch-up Prevention

Rule No.	Description	Label	Op.	Rule
LUP.10	<p>For Area I/O, within “A” sizing of the OD injector (covered by LUPWDMDY_2), specific guard rings rules and N/P wells STRAP rules (LUP.13, LUP.13.1, LUP.13.2 and LUP.14) should be followed to enhance latch up immunity (Fig 9.1.14)</p> <p>A = 75 μm for LUP.13, A = 75 μm for LUP.13.1, and A = 75 μm for LUP.13.2.</p> <p>(Checking window is also recognized by cad layers LUP_045U, LUP_075U, LUP_045U_18V, LUP_075U_18V, LUP_045U_15V and LUP_075U_15V when the option “IP_LEVEL_LUP_CHECK” is switched on.)</p> <p>Rule exclusion: if one of the following conditions is true:</p> <ol style="list-style-type: none"> 1. Area of specific injector cluster < 3 μm^2. Area I/O injector cluster for this exception = {(Area I/O OD injector (NOT HIADMY, SDI, NWSTRAP/RWSTRAP) sizing up/down 0.851 μm)}. (except LUP.14). 2. Spacing between the N+ OD and P+ OD of the CMOS circuits \geq 3 μm. (except LUP.13.2) 3. NMOS (PMOS) of the CMOS circuits are surrounded by P+ guard-ring (N+ guard-ring). 4. OD injectors [NOT HIANMOS OD injector, NOT NW/RWSTRAP OD injector] connect to low/ultra-low noise signal pin. For the detail of low/ultra-low noise OD injector recognition methodology, please refer to Section 9.1.2.3.14. (except LUP.14) 5. OD injector covered by LUPIEDMY. (This is for failsafe IO; It is not recommended to use this layer before silicon proven) 6. ACTIVE OD does not connect to VC or MP 	A		
LUP.13	<p>For Area I/O, PMOS source/drain voltage \geq 0.75V (0.68V+10%) within “A” sizing of “B” OD injector (covered by LUPWDMDY_2) and NMOS within 3 μm space from “\geq 0.75V PMOS.”</p> <ol style="list-style-type: none"> 1. Any point inside NMOS source/drain {(N+ ACTIVE INTERACT TrGATE) NOT PO} space to the nearest LUP PW STRAP in the same PW needs to follow LUP.13.0.1 ~LUP.13.0.6. (Figure 9.1.14) 2. Any point inside PMOS source/drain {(P+ ACTIVE INTERACT TrGATE) NOT PO} space to the nearest LUP NW STRAP in the same NW needs to follow LUP.13.0.1 ~LUP.13.0.6. (Figure 9.1.14) 3. The height of pick-up OD is recommended to be equal to that of source/drain ODs. (Figure 9.1.14) <p>The LUP PW(NW) STRAP to N+(P+) ACTIVE space requirement is dependent on a. “LUP STRAP group size”, b. “NW strait width”, c. “N/PMOS distance to OD injector”, d. “circuit category (SRAM or non-SRAM circuit)”, and e. “OD injector noise level”. When multiple overlapping checking windows from OD injectors with different noise level coincide, the most conservative rule will be checked.</p> <ol style="list-style-type: none"> a. The LUP NW(PW) STRAP group means the LUP STRAPS with space \leq 0.6 μm along same NW(PW) strait. DRC counts the total fin number in the same LUP STRAP group. Total fin number for each of LUP STRAP = {((LUP STRAP vertical width - 0.008)/ 0.030 + 1) * (POLY count -1)}. b. For the NW strait width judgement, it takes minimum width of {NW NOT {LUP NWSTRAP SIZING 1 μm along the same NW}} or minimum width of NW. DRC considers NW strait width from where STRAP located to where N/PMOS placed. c. For PMOS with NW width < 0.240 μm outside SRAMDMDY (186;0)/SRM (50;0), this rule will always flag PMOS. d. The SRAM circuit is recognized by SRAMDMDY(186;0) or SRM (50;0). e. Med-Low noise/ Med noise OD injector are recognized by CAD layer LUP15VIEDMY/ LUP18VIEDMY on M1 or LUP15VIEDMY_BUMP/ LUP18VIEDMY_BUMP on CB/CB2/UBM or pin text defined in MED_LOW_NOISE_PAD_TEXT/ MED_NOISE_PAD_TEXT in DRC setup. f. LUP.13.0.1 /LUP.13.0.2 /LUP.13.0.3 cover requirement within 45um spacing to OD injector. LUP.13.0.4 /LUP.13.0.5 /LUP.13.0.6 cover requirement within 75um spacing to OD injector. 			
LUP.13.0.1	If the N/PMOS is within 45 μm sizing of the high noise OD injector or (cascoded HIANMOS OD injector) or NW/RWSTRAP OD injector	D	\leq	Table 9.2.1.1

Rule No.	Description	Label	Op.	Rule
	<p>OD injector meet one of following conditions is recognized as cascaded HIANMOS OD injector for this rule.</p> <ul style="list-style-type: none"> a. N+ ACTIVE OD injector [INTERACT SDI_2, INTERACT ((GATE NOT INTERACT PODE GATE) NOT INTERACT SDI_2)] b. N+ ACTIVE OD injector [INTERACT SDI_2, with one side connected to IOPAD, without direct connection to PWSTRAP] 			
LUP.13.0.2	If the N/PMOS is within 45 μm sizing of the medium noise OD injector or HIANMOS OD injector HIANMOS OD injector = N+ ACTIVE OD injector [INTERACT SDI_2]	D	\leq	Table 9.2.1.1
LUP.13.0.3	If the N/PMOS is within 45 μm sizing of the medium-low noise OD injector	D	\leq	Table 9.2.1.1
LUP.13.0.4	If the N/PMOS is within 75 μm sizing of the high noise OD injector or (cascaded HIANMOS OD injector) or NW/RWSTRAP OD injector OD injector meet one of following conditions is recognized as cascaded HIANMOS OD injector for this rule. <ul style="list-style-type: none"> a. N+ ACTIVE OD injector [INTERACT SDI_2, INTERACT ((GATE NOT INTERACT PODE GATE) NOT INTERACT SDI_2)] b. N+ ACTIVE OD injector [INTERACT SDI_2, with one side connected to IOPAD, without direct connection to PWSTRAP] 	D	\leq	Table 9.2.1.1
LUP.13.0.5	If the N/PMOS is within 75 μm sizing of the medium noise OD injector or HIANMOS OD injector HIANMOS OD injector = N+ ACTIVE OD injector [INTERACT SDI_2]	D	\leq	Table 9.2.1.1
LUP.13.0.6	If the N/PMOS is within 75 μm sizing of the medium-low noise OD injector	D	\leq	Table 9.2.1.1
LUP.13.1	<p>For Area I/O, PMOS source /drain voltage $> 0.825\text{V}$ ($0.75\text{V}+10\%$) and $\leq 1.2\text{V}$ within “A” sizing of “B” OD injector (covered by LUPWDMDY_2) and NMOS within 3 μm space from “$> 0.825\text{V}$ PMOS”</p> <ol style="list-style-type: none"> 1. Any point inside core NMOS source/drain {(N+ ACTIVE INTERACT TrGATE) NOT PO} space to the nearest LUP PW STRAP in the same PW needs to follow LUP.13.1.1 ~LUP.13.1.6. (Figure 9.1.14). 2. Any point inside core PMOS source/drain {(P+ ACTIVE INTERACT TrGATE) NOT PO} space to the nearest LUP NW STRAP in the same NW needs to follow LUP.13.1.1 ~LUP.13.1.6. (Figure 9.1.14). 3. The height of pick-up OD is recommended to be equal to that of source/drain ODs. (Figure 9.1.14) 4. If PMOS source/drain voltage $> 1.2\text{V}$, this rule will always flag PMOS. 5. The defined voltage range means max power supply voltage of core devices (+10% of nominal supply voltage). If operation voltage $> 0.825\text{V}$, please contact tsmc for reliability concern. For details, please refer to Section 2.3. <p>The LUP PW(NW) STRAP to N+(P+) ACTIVE space requirement is dependent on a. “LUP STRAP group size”, b. “NW strait width”, c. “N/PMOS distance to OD injector”, d. “circuit category (SRAM or non-SRAM circuit)”, and e. “OD injector noise level”. When multiple overlapping checking windows from OD injectors with different noise level coincide, the most conservative rule will be checked.</p> <ol style="list-style-type: none"> a. The LUP NW(PW) STRAP group means the LUP STRAPS with space $\leq 0.6 \mu\text{m}$ along same NW(PW) strait. DRC counts the total fin number in the same LUP STRAP group. Total fin number for each of LUP STRAP = {((LUP STRAP vertical width - 0.008)/ 0.030 + 1) * (POLY count -1)}. b. For the NW strait width judgement, it takes minimum width of {NW NOT {LUP NWSTRAP SIZING 1 μm along the same NW}} or minimum width of NW. DRC considers NW strait width from where STRAP located to where N/PMOS placed. c. For PMOS with NW width $< 0.240 \mu\text{m}$ outside SRAMDMDY (186;0)/SRM (50;0), this rule will always flag PMOS. d. The SRAM circuit is recognized by SRAMDMDY (186;0) or SRM (50;0). e. Med-Low noise/ Med noise OD injector are recognized by CAD layer LUP15VIEDMY/ LUP18VIEDMY on M1 or LUP15VIEDMY_BUMP/ 			

Rule No.	Description	Label	Op.	Rule
	LUP18VIEDMY_BUMP on CB/CB2/UBM or pin text defined in MED_LOW_NOISE_PAD_TEXT/ MED_NOISE_PAD_TEXT in DRC setup. f. LUP.13.1.1 /LUP.13.1.2 /LUP.13.1.3 cover requirement within 45 µm spacing to OD injector. LUP.13.1.4 /LUP.13.1.5 /LUP.13.1.6 cover requirement within 75 µm spacing to OD injector.			
LUP.13.1.1	If the N/PMOS is within 45 µm sizing of the high noise OD injector or (cascoded HIANMOS OD injector) or NW/RWSTRAP OD injector OD injector meet one of following conditions is recognized as cascoded HIANMOS OD injector for this rule. a. N+ ACTIVE OD injector [INTERACT SDI_2, INTERACT ((GATE NOT INTERACT PODE GATE) NOT INTERACT SDI_2)] b. N+ ACTIVE OD injector [INTERACT SDI_2, with one side connected to IOPAD, without direct connection to PWSTRAP]	D	\leq	Table 9.2.1.2
LUP.13.1.2	If the N/PMOS is within 45 µm sizing of the medium noise OD injector or HIANMOS OD injector HIANMOS OD injector = N+ ACTIVE OD injector [INTERACT SDI_2]	D	\leq	Table 9.2.1.2
LUP.13.1.3	If the N/PMOS is within 45 µm sizing of the medium-low noise OD injector	D	\leq	Table 9.2.1.2
LUP.13.1.4	If the N/PMOS is within 75 µm sizing of the high noise OD injector or (cascoded HIANMOS OD injector) or NW/RWSTRAP OD injector OD injector meet one of following conditions is recognized as cascoded HIANMOS OD injector for this rule. a. N+ ACTIVE OD injector [INTERACT SDI_2, INTERACT ((GATE NOT INTERACT PODE GATE) NOT INTERACT SDI_2)] b. N+ ACTIVE OD injector [INTERACT SDI_2, with one side connected to IOPAD, without direct connection to PWSTRAP]	D	\leq	Table 9.2.1.2
LUP.13.1.5	If the N/PMOS is within 75 µm sizing of the medium noise OD injector or HIANMOS OD injector HIANMOS OD injector = N+ ACTIVE OD injector [INTERACT SDI_2]	D	\leq	Table 9.2.1.2
LUP.13.1.6	If the N/PMOS is within 75 µm sizing of the medium-low noise OD injector	D	\leq	Table 9.2.1.2
LUP.13.2	For Area I/O, PMOS source/drain voltage \geq 0.75V (0.68V+10%) within “A” sizing of “B” OD injector (covered by LUPWDMDY_2) and NMOS within 3 µm space from “ \geq 0.75V PMOS,” 1. Any point inside IO NMOS source/drain {(N+ ACTIVE INTERACT TrGATE) NOT PO} space to the nearest LUP PW STRAP in the same PW needs to follow LUP.13.2.1 ~LUP.13.2.6. (Figure 9.1.14) 2. Any point inside IO PMOS source/drain {(P+ ACTIVE INTERACT TrGATE) NOT PO} space to the nearest LUP NW STRAP in the same NW needs to follow LUP.13.2.1 ~LUP.13.2.6. (Figure 9.1.14) 3. The height of pick-up OD is recommended to be equal to that of source/drain ODs. (Figure 9.1.14) The LUP PW(NW) STRAP to N+(P+) ACTIVE space requirement is dependent on a. “LUP STRAP group size”, b. “NW strait width”, c. “N/PMOS distance to OD injector”, and d. “OD injector noise level”. When multiple overlapping checking windows from OD injectors with different noise level coincide, the most conservative rule will be checked. a. The LUP NW(PW) STRAP group means the LUP STRAPs with space \leq 0.6 µm along same NW(PW) strait. DRC counts the total fin number in the same LUP STRAP group. Total fin number for each of LUP STRAP = {((LUP STRAP vertical width - 0.008)/ 0.030 + 1) * (POLY count -1)}. b. For the NW strait width judgement, it takes minimum width of {NW NOT {LUP NWSTRAP SIZING 1 µm along the same NW}} or minimum width of NW. DRC considers NW strait width from where STRAP located to where N/PMOS placed. c. For PMOS with NW width $<$ 0.360 µm, this rule will always flag PMOS. d. Med-Low noise/ Med noise OD injector are recognized by CAD layer LUP15VIEDMY/ LUP18VIEDMY on M1 or LUP15VIEDMY_BUMP/ LUP18VIEDMY_BUMP on CB/CB2/UBM or pin text defined in			

Rule No.	Description	Label	Op.	Rule
	MED_LOW_NOISE_PAD_TEXT/ MED_NOISE_PAD_TEXT in DRC setup. e. LUP.13.2.1 /LUP.13.2.2 /LUP.13.2.3 cover requirement within 45 µm spacing to OD injector. LUP.13.2.4 /LUP.13.2.5 /LUP.13.2.6 cover requirement within 75 µm spacing to OD injector.			
LUP.13.2.1	If the N/PMOS is within 45 µm sizing of the high noise OD injector or (cascoded HIANMOS OD injector) or NW/RWSTRAP OD injector OD injector meet one of following conditions is recognized as cascoded HIANMOS OD injector for this rule. a. N+ ACTIVE OD injector [INTERACT SDI_2, INTERACT ((GATE NOT INTERACT PODE GATE) NOT INTERACT SDI_2)] b. N+ ACTIVE OD injector [INTERACT SDI_2, with one side connected to IOPAD, without direct connection to PWSTRAP]	D	≤	Table 9.2.1.3
LUP.13.2.2	If the N/PMOS is within 45 µm sizing of the medium noise OD injector or HIANMOS OD injector HIANMOS OD injector = N+ ACTIVE OD injector [INTERACT SDI_2]	D	≤	Table 9.2.1.3
LUP.13.2.3	If the N/PMOS is within 45 µm sizing of the medium-low noise OD injector	D	≤	Table 9.2.1.3
LUP.13.2.4	If the N/PMOS is within 75 µm sizing of the high noise OD injector or (cascoded HIANMOS OD injector) or NW/RWSTRAP OD injector OD injector meet one of following conditions is recognized as cascoded HIANMOS OD injector for this rule. a. N+ ACTIVE OD injector [INTERACT SDI_2, INTERACT ((GATE NOT INTERACT PODE GATE) NOT INTERACT SDI_2)] b. N+ ACTIVE OD injector [INTERACT SDI_2, with one side connected to IOPAD, without direct connection to PWSTRAP]	D	≤	Table 9.2.1.3
LUP.13.2.5	If the N/PMOS is within 75 µm sizing of the medium noise OD injector or HIANMOS OD injector HIANMOS OD injector = N+ ACTIVE OD injector [INTERACT SDI_2]	D	≤	Table 9.2.1.3
LUP.13.2.6	If the N/PMOS is within 75 µm sizing of the medium-low noise OD injector	D	≤	Table 9.2.1.3
LUP.14	For Area I/O, OD injector (NOT INSIDE IBJTDY (110;3), LUPIEDMY (255;56)) must be surrounded by two guard-rings for the OD injector. And all of the guard-ring widths must be $\geq 0.218 \mu m$ N+OD injector must be surrounded by P+ guard-ring (P+ pick-up ring). P+OD injector must be surrounded by N+ guard-ring (N+ pick-up ring). The PW of N+OD injector must be surrounded by N+ guard-ring. The NW of P+OD injector must be surrounded by P+ guard-ring.	E	≥	0.2180
LUP.14.0.1 ^U	The N+ / P+ guard-ring for LUP.14 should be tied to power / ground accordingly. Except for the devices covered by IBJTDY (110;3), or LUPIEDMY (255;56) Except for the devices/ guard-rings covered by LUPWDMDY_IP (255;235). It is not recommended to use LUPIEDMY before silicon proven.			

For core (thin oxide) device, the max power supply refers to the “Power Supply and Operation Temperature Ranges” chapter.

Table 9.2.1.1 Layout Sapce Rule for LUP.13, LUP.6 and LUP.6.2

N7+ core AAIQ latch-up rule For near interface IP connecting to signal bump with risk of high injection current in system operation or latch-up testing (JESD78D)									
Checking window	within 15~45um				within 45~75um				outside 75um
Application	High noise ODinj (>1.98V)	Medium noise ODinj (>1.65V)	Med-Low noise ODinj (>1.32V)	Low & Ultra-Low noise ODinj ($\leq 1.32V$)	High noise ODinj (>1.98V)	Medium noise ODinj (>1.65V)	Med-Low noise ODinj (>1.32V)	Low & Ultra-Low noise ODinj ($\leq 1.32V$)	All OD injector
	3.3V I/O	1.8V I/O	1.5V&1.35V I/O	1.2V/core I/O	3.3V I/O	1.8V I/O	1.5V&1.35V I/O	1.2V/core I/O	All
Binning	LUP.13 group STD cell $\geq 0.75V$			Waive LUP.13	LUP.13 group STD cell $\geq 0.75V$			Waive LUP.13	LUP.6/ LUP.6.2
	LUP.13.0.1	LUP.13.0.2	LUP.13.0.3		LUP.13.0.4	LUP.13.0.5	LUP.13.0.6		
SRAM bit cell	flag	flag	flag	Tap OD: 4Fins D=16um (LUP.6.2)	flag	flag	flag	Tap OD: 4Fins D=16um (LUP.6.2)	Tap OD: 4Fins D=16um (LUP.6.2)
NW width <240nm	flag	flag	flag	Tap OD: 4Fins D=51um (LUP.6)	flag	flag	flag	Tap OD: 4Fins D=51um (LUP.6)	Tap OD: 4Fins D=51um (LUP.6)
NW width $\geq 240nm$	Tap OD: 4Fins D=1um	Tap OD: 4Fins D=3um	Tap OD: 4Fins D=5um		Tap OD: 4Fins D=3um	Tap OD: 4Fins D=16um	Tap OD: 4Fins D=25um		
	Tap OD: 8Fins D=4um	Tap OD: 8Fins D=4um	Tap OD: 8Fins D=15um		Tap OD: 8Fins D=5um	Tap OD: 8Fins D=20um	Tap OD: 8Fins D=30um		
NW width $\geq 360nm$	Tap OD: 12Fins D=6um	Tap OD: 12Fins D=6um	Tap OD: 12Fins D=20um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		
	Tap OD: 12Fins D=7.5um	Tap OD: 12Fins D=8um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=7.5um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		
NW width $\geq 480nm$	Tap OD: 12Fins D=9um	Tap OD: 12Fins D=9um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=9um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		
	Tap OD: 12Fins D=10.5um	Tap OD: 12Fins D=10.5um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=10.5um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		
NW width $\geq 1000nm$	Tap OD: 12Fins D=12.5um	Tap OD: 12Fins D=12.5um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=12.5um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		

Table 9.2.1.2 Layout Sapce Rule for LUP.13.1, LUP.6 and LUP.6.2

N7+ core AAIQ latch-up rule

For near interface IP connecting to signal bump with risk of high injection current in system operation or latch-up testing
(JESD78D)

Checking window	within 15~45um				within 45~75um				outside 75um
Application	High noise ODinj (>1.98V)	Medium noise ODinj (>1.65V)	Med-Low noise ODinj (>1.32V)	Low & Ultra-Low noise ODinj ($\leq 1.32V$)	High noise ODinj (>1.98V)	Medium noise ODinj (>1.65V)	Med-Low noise ODinj (>1.32V)	Low & Ultra-Low noise ODinj ($\leq 1.32V$)	All OD injector
	3.3V I/O	1.8V I/O	1.5V&1.35V I/O	1.2V/core I/O	3.3V I/O	1.8V I/O	1.5V&1.35V I/O	1.2V/core I/O	All
Binning	LUP.13.1 group STD cell >0.825V			Waive LUP.13.1	LUP.13.1 group STD cell >0.825V			Waive LUP.13.1	LUP.6/ LUP.6.2
	LUP.13.1.1	LUP.13.1.2	LUP.13.1.3		LUP.13.1.4	LUP.13.1.5	LUP.13.1.6		
SRAM bit cell	flag	flag	flag	Tap OD: 4Fins D=16um (LUP.6.2)	flag	flag	flag	Tap OD: 4Fins D=16um (LUP.6.2)	Tap OD: 4Fins D=16um (LUP.6.2)
NW width <240nm	flag	flag	flag	Tap OD: 4Fins D=51um (LUP.6)	flag	flag	flag	Tap OD: 4Fins D=51um (LUP.6)	Tap OD: 4Fins D=51um (LUP.6)
NW width $\geq 240nm$	Tap OD: 4Fins D=1um	Tap OD: 4Fins D=3um	Tap OD: 4Fins D=5um		Tap OD: 4Fins D=3um	Tap OD: 4Fins D=16um	Tap OD: 4Fins D=25um		
	Tap OD: 8Fins D=1.5um	Tap OD: 8Fins D=4um	Tap OD: 8Fins D=15um		Tap OD: 8Fins D=5um	Tap OD: 8Fins D=20um	Tap OD: 8Fins D=30um		
NW width $\geq 360nm$	Tap OD: 12Fins D=2um	Tap OD: 12Fins D=5um	Tap OD: 12Fins D=20um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		
NW width $\geq 480nm$	Tap OD: 12Fins D=2.5um	Tap OD: 12Fins D=8um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		
NW width $\geq 650nm$	Tap OD: 12Fins D=3um	Tap OD: 12Fins D=8um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		
NW width $\geq 820nm$	Tap OD: 12Fins D=3.5um	Tap OD: 12Fins D=8um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		
NW width $\geq 1000nm$	Tap OD: 12Fins D=4um	Tap OD: 12Fins D=8um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=22.5um	Tap OD: 12Fins D=30um		

Table 9.2.1.3 Layout Sapce Rule for LUP.13.2 and LUP.6.1**N7+ IO (with OD18) AAI0 latch-up rule**

For near interface IP connecting to signal bump with risk of high injection current in system operation or latch-up testing
(JESD78D)

Checking window	within 15~45um				within 45~75um				outside 75um	
Application	High noise ODinj (>1.98V)	Medium noise ODinj (>1.65V)	Med-Low noise ODinj (>1.32V)	Low & Ultra-Low noise ODinj ($\leq 1.32V$)	High noise ODinj (>1.98V)	Medium noise ODinj (>1.65V)	Med-Low noise ODinj (>1.32V)	Low & Ultra-Low noise ODinj ($\leq 1.32V$)	All OD injector	
	3.3V I/O	1.8V I/O	1.5V&1.35V I/O	1.2V/core I/O	3.3V I/O	1.8V I/O	1.5V&1.35V I/O	1.2V/core I/O	All	
Binning	LUP.13.2 group IO STD cell (OD_18)			Waive LUP.13.2	LUP.13.2 group IO STD cell (OD_18)			Waive LUP.13.2	LUP.6.1	
	LUP.13.2.1	LUP.13.2.2	LUP.13.2.3		LUP.13.2.4	LUP.13.2.5	LUP.13.2.6			
NW width <360nm	flag	flag	flag	Tap OD: 4Fins D=1um Tap OD: 8Fins D=1.5um Tap OD: 12Fins D=2.5um Tap OD: 12Fins D=3um Tap OD: 12Fins D=3.5um Tap OD: 12Fins D=4um	flag	flag	flag	Tap OD: 4Fins D=3um Tap OD: 8Fins D=5um Tap OD: 12Fins D=6um Tap OD: 12Fins D=6um Tap OD: 12Fins D=6um Tap OD: 12Fins D=6um	Tap OD: 4Fins D=15um Tap OD: 8Fins D=20um Tap OD: 12Fins D=25um Tap OD: 12Fins D=25um Tap OD: 12Fins D=25um Tap OD: 12Fins D=25um	Tap OD: 4Fins D=25um Tap OD: 8Fins D=25um Tap OD: 12Fins D=25um Tap OD: 12Fins D=25um Tap OD: 12Fins D=25um Tap OD: 12Fins D=25um
NW width $\geq 360nm$	Tap OD: 4Fins D=1um	Tap OD: 4Fins D=3um	Tap OD: 4Fins D=5um		Tap OD: 4Fins D=3um	Tap OD: 4Fins D=15um	Tap OD: 4Fins D=25um			
NW width $\geq 480nm$	Tap OD: 8Fins D=1.5um	Tap OD: 8Fins D=4um	Tap OD: 8Fins D=15um		Tap OD: 8Fins D=5um	Tap OD: 8Fins D=20um	Tap OD: 8Fins D=25um			
NW width $\geq 650nm$	Tap OD: 12Fins D=2.5um	Tap OD: 12Fins D=8um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=25um	Tap OD: 8Fins D=25um			
NW width $\geq 820nm$	Tap OD: 12Fins D=3um	Tap OD: 12Fins D=8um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=25um	Tap OD: 8Fins D=25um			
NW width $\geq 1000nm$	Tap OD: 12Fins D=3.5um	Tap OD: 12Fins D=8um	Tap OD: 12Fins D=25um		Tap OD: 12Fins D=6um	Tap OD: 12Fins D=25um	Tap OD: 8Fins D=25um			

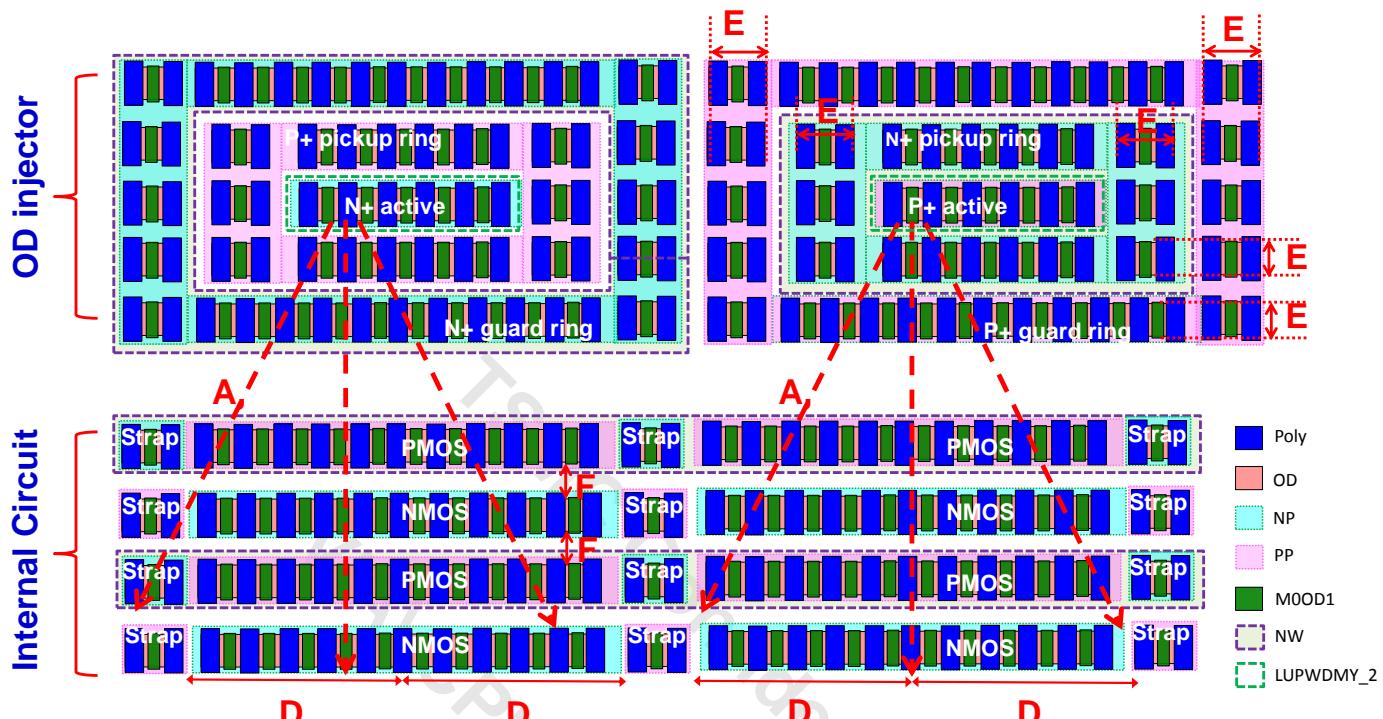


Figure 9.1.14 Area I/O latchup prevention

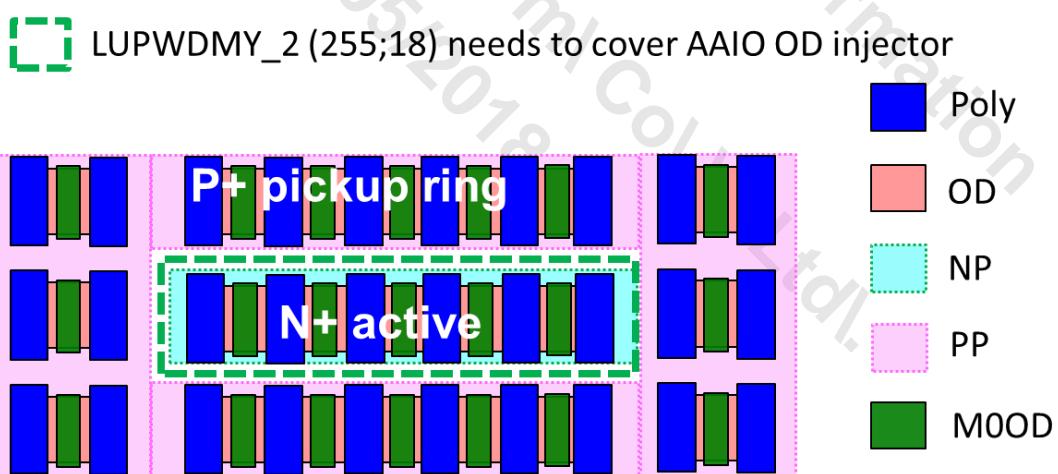


Figure 9.1.15 Example of LUPWDMDY_2 Usage

9.1.3 Test Specification and Requirements

TSMC Latch-Up testing is complied with the Latch-up test methodology defined by JESD 78D (JEDEC). For details, please refer to JESD78D.

TSMC Confidential Information
938214
VIAI CPU Platform\ Col. I Ltd.
10/05/2018

9.2 I/O ESD Protection Circuit Design, Layout Rules and Guidelines

9.2.1 ESD introduction

During manufacturing, it is inevitable the IC will suffer various kinds of Electrostatic-Discharge (ESD) damage. Different environments, wafer during CMOS process, package, testing and human handling, will generate different kinds of ESD's. Currently, the charge device model (CDM) and Human-Body mode (HBM) are the most common models used to simulate the ESD events generated from various environments. The main difference between CDM and HBM is that CDM charges initially store inside the chip and will discharge through the internal circuit to the pad, while the ESD for HBM comes from the external environment to the pad. The cases of HBM are less complex than the CDM events, thus most ESD protection devices are designed for HBM protection to provide a direct current shunting path between the I/O pad and VSS/VDD. In consideration of CDM protection, appropriate design of secondary protection and active clamp are essential and have become an important topic for the advance technology, in which the gate oxide is getting thinner and thinner.

VIAI CPU Platform Col., Ltd.
Confidential Information
938214
10/05/2018

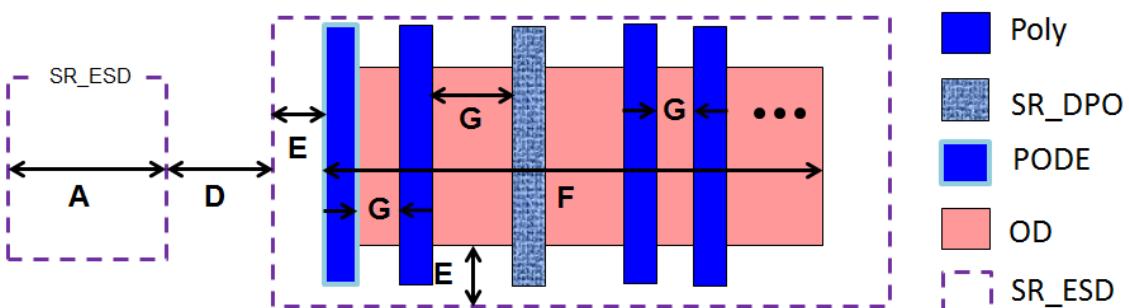
9.2.2 ESD Implant (ESDIMP) Layout Rules

The ESD implant process is not offered in the N7+ FinFET technology.

9.2.3 SR_ESD device Layout Rules

The SR_ESD layer (CAD layer: 121;0) is used for drain-ballasted NMOS and cascaded drain-ballasted NMOS only. SR_ESD is a DRC layer to check the ESD guidelines and a tape-out layer.

Rule No.	Description	Label	Op.	Rule
SR_ESD.W.1	Width	A	\geq	0.2100
SR_ESD.S.1	Space	D	\geq	0.2100
SR_ESD.S.3	SR_DPO space to PO [INSIDE SR_ESD]	G	=	0.2320
SR_ESD.S.3.1	Space of ALL_PO [INSIDE SR_ESD]	G	=	0.0940, 0.2320
SR_ESD.EX.1	Extension on ACTIVE	E	\geq	0.0650
SR_ESD.L.1	Maximum ACTIVE length of I/O device in SR_ESD regions	F	\leq	60
SR_ESD.R.1	SR_ESD must be fully covered by SDI; SR_ESD can not cover core N/PMos and IO PMOS.			
SR_ESD.R.2	SR_ESD interact DNW is not allowed			
SR_ESD.R.3	Drain-ballasted NMOS should be in common drain layout style. DRC checks: {{SDI_2 INTERACT SR_ESD} INTERACT PODE_GATE} is not allowed.			
SR_ESD.R.7 ^U	{OD NOT ALL_PO} inside same SDI_2 should be shorted together			



9.2.4 SDI Dummy Layer

SDI (CAD layer: 122;0) is a DRC layer to check the ESD guidelines but not a tape-out layer. It is required to cover all ESD MOS OD regions.

This includes the source, gate, and drain, but not necessarily the field PO and well strap OD regions. Please refer to Figure 9.2.4, shown below.

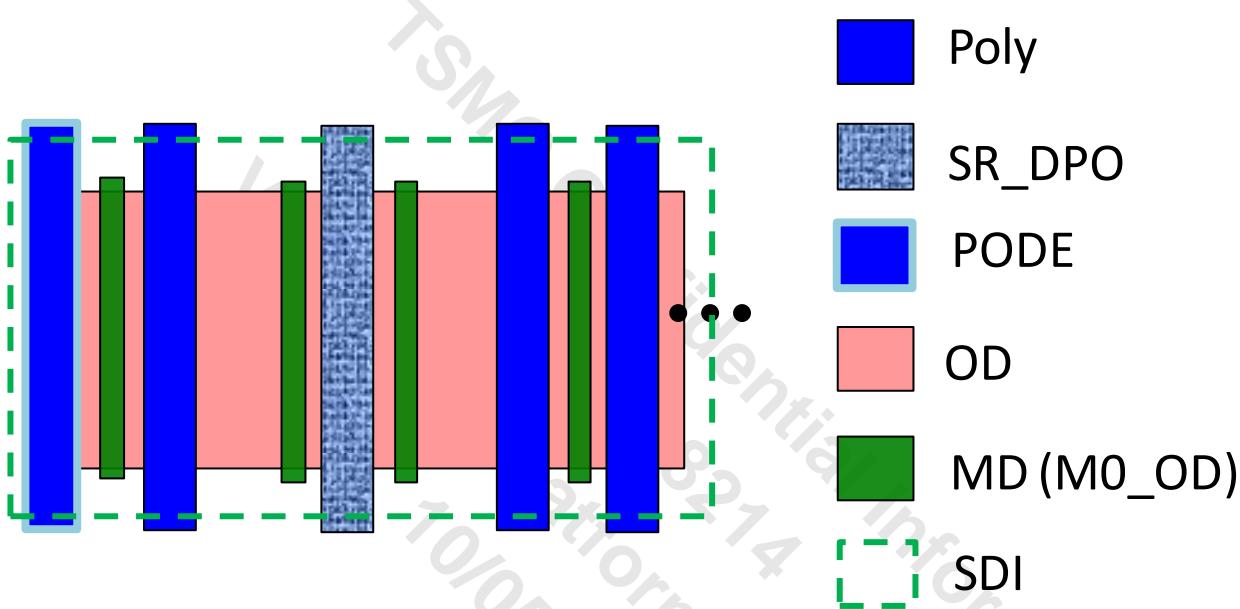


Figure 9.2.4 The SDI dummy layer layout

SDI_2 (CAD layer: 122;2) is a tapeout layer and DRC layer to recognize drain-ballasted NMOS, and identify drain side of it. SDI_2 layer can only be covered on drain-ballasted NMOS.

The SDI_2 layer should cover drain OD regions and partial POLY of drain-ballasted MOS, but not necessarily the field PO and well strap OD regions. For all PMOS, drain-ballasted type is forbidden. Please refer to Figure 9.2.5, shown below.

Rule No.	Description	Label	Op.	Rule
SDI_2.W.1	Width of {SDI_2 [INSIDE SR_ESD] SIZING up/down 0.221 μm } in vertical direction		\geq	0.6980
SDI_2.W.2	Width of {SDI_2 [INSIDE SR_ESD]} in horizontal direction		$=$	0.6700
SDI_2.W.3	Width of {(OD AND SDI_2) NOT PO [INSIDE SR_ESD]} in horizontal direction		$=$	0.5500
SDI_2.S.1	Space of {OD AND SDI_2 [INSIDE SR_ESD]} to NW with different potential (Overlap is not allowed)		\geq	1.0610
SDI_2.S.1.1	Space of {OD AND SDI_2 [INSIDE SR_ESD]} to NW [maximum delta V > 1.98V] (1.8V + 10%)		\geq	2.1610
SDI_2.S.2	Space of SDI_2 [INSIDE SR_ESD] to PWSTRAP in the vertical direction		\geq	0.2620
SDI_2.S.3	Space of {OD AND SDI_2 [INSIDE SR_ESD]} to {OD AND SDI_2 [INSIDE SR_ESD]} with different potential		\geq	1.2220
SDI_2.S.3.1	Space of {OD AND SDI_2 [INSIDE SR_ESD]} to {OD AND SDI_2 [INSIDE SR_ESD]} [maximum delta V > 1.98V] (1.8V + 10%)		\geq	2.3220
SDI_2.S.4	Space of {OD AND SDI_2 [INSIDE SR_ESD]} to DNW with different potential		\geq	1.6610
SDI_2.S.5	Space of {OD AND SDI_2 [INSIDE SR_ESD]} in horizontal direction		\geq	0.2440
SDI_2.EN.1	Enclosure of OD [INSIDE SR_ESD] in vertical direction.		$=$	0.0600
SDI_2.R.1	{OD AND SDI_2 [INSIDE SR_ESD]} must INTERACT with SR_DPO			
SDI_2.R.2	{SDI_2 [INSIDE SR_ESD] SIZING up/down 0.221 μm in vertical direction} must be a rectangle			
SDI_2.R.3	{ALL_OD NOT PO} [Horizontal width = 0.55 μm] must be fully covered by SDI_2			
SDI_2.R.4	{OD AND SDI_2 [INSIDE SR_ESD] SIZING 0.281 μm / SIZING -0.120 μm in vertical direction} INTERACT with {DNW OR SR_DOD} is not allowed.			

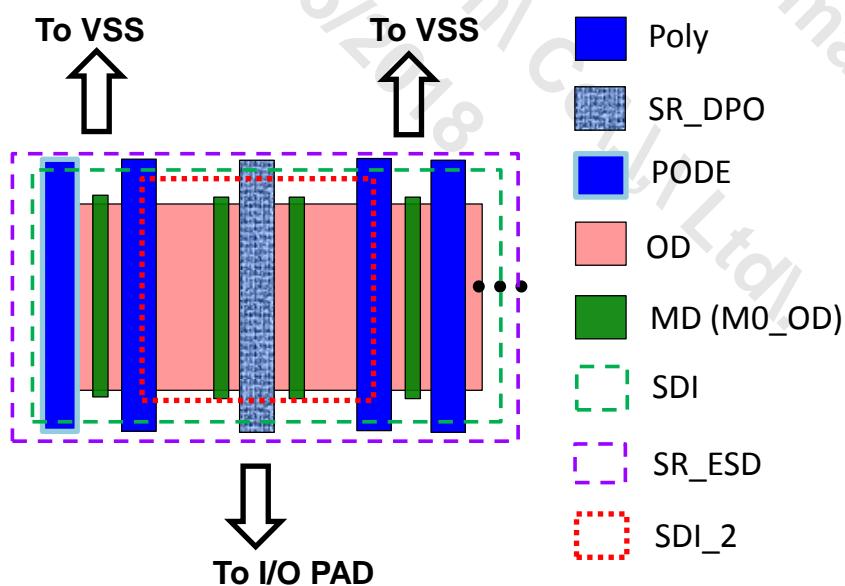


Figure 9.2.5 The SDI_2 dummy layer layout

9.2.5 DRC methodology for ESD guidelines

9.2.5.1 DRC methodology to identify ESD devices

1. The ESD device is defined by MOS covered by SDI (122;0).
2. The Drain-ballasted ESD NMOS is defined in the following:
 - (ESD NMOS INTERACT SR_ESD) with gate partially covered by SDI_2 & without gate not covered by SDI_2
3. The Power Clamp ESD NMOS is defined in the following:
 - ESD NMOS without SR_ESD overlap

Note: Others are not TSMC-standard ESD devices. So, there is no rule to check it.

Table 9.2.2 how to recognize ESD device

SDI	SDI_2 Partially Cover Gate	SDI_2 Not Cover Gate	SR_ESD	ESD Device Type
Y	Y	N	Y	Drain-ballasted ESD NMOS
Y	Y	Y	Y	Drain-ballasted Cascoded ESD NMOS
Y	N	N	N	Power Clamp ESD NMOS

9.2.5.2 DRC methodology to identify ESD devices

1. The S/D region is defined by {MOS_OD NOT POLY}
2. The S/D region which connected to well pick-up is Source.
 - The connectivity is not broken by resistor for this check.
3. The S/D region OUTSIDE SDI_2 is Source. (except for Power Clamp)
4. Except for recognized Source, all the others are Drain.

Note: If the ESD layout structure is not TSMC-standard, this approach will fail.

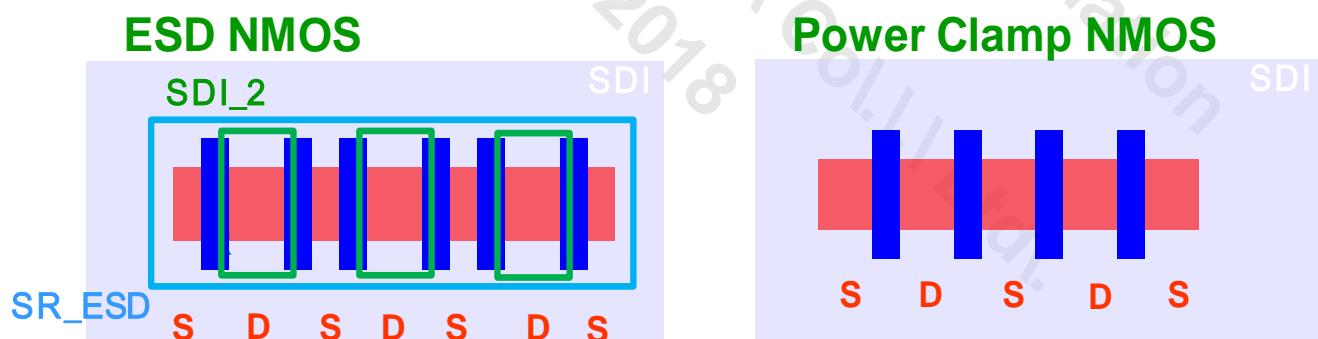


Figure 9.2.6 Example of S/D for ESD device

9.2.5.3 DRC methodology for ESD.1g

1. ESD S/D is covered by OD2, and connected to Core device S/D/G (without OD2).
2. If ESD S/D is connected to P-well pick-up, it is excluded from this rule check.

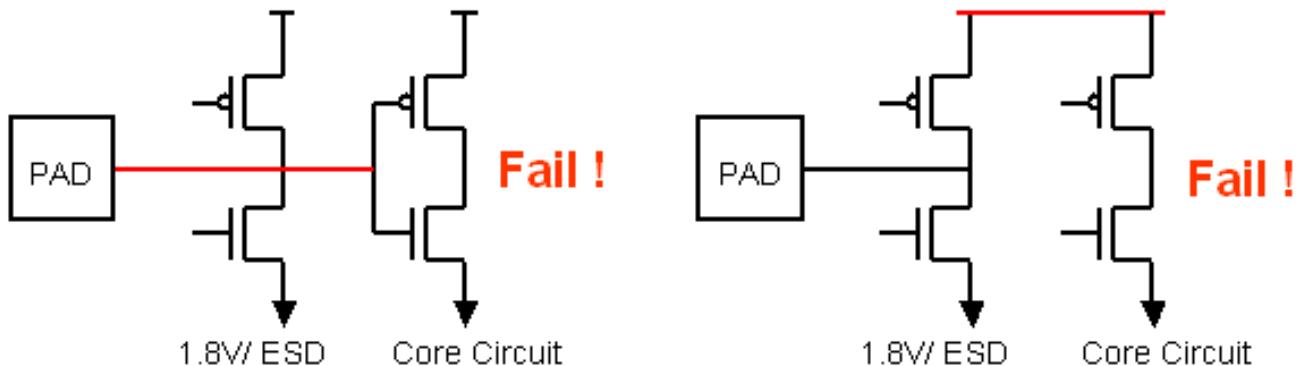
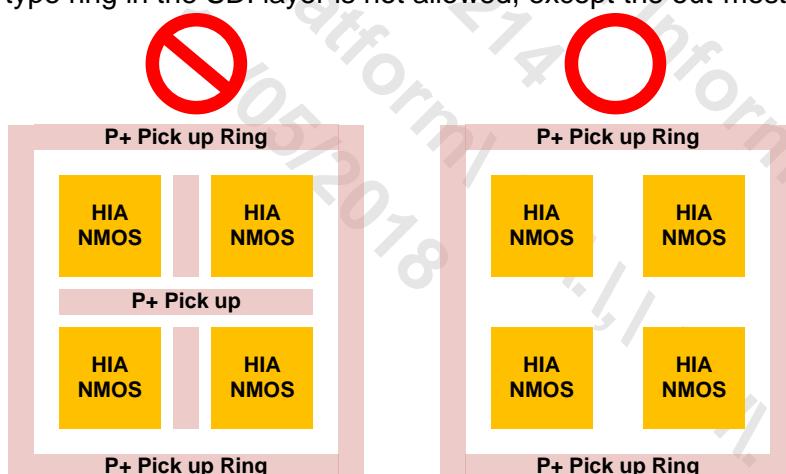


Figure 9.2.7 Example of ESD.1g

9.2.5.4 DRC methodology for ESD.6g

Drain-ballasted NMOS should be surrounded by one outer P+ pick-up ring only. DRC methodology of ESD.6g is as follows:

1. SDI layers with spacing < 1.2 μm will merge into one SDI layer.
2. Any P-type strap or P-type ring in the SDI layer is not allowed, except the out-most guard-ring.



9.2.5.5 DRC methodology for finger width

This check is for ESD.18g, ESD.27g, ESD.40g and ESD.40.1g.

The total finger width is calculated by the ESD MOS in the same Drain connection.

The connectivity is broken by resistor for this check.

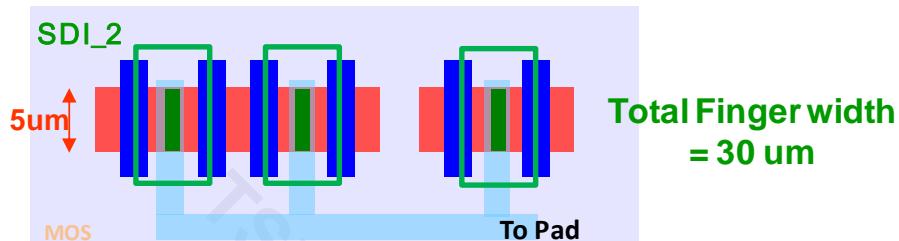


Figure 9.2.8 Example of finger width

9.2.5.6 DRC methodology for ESD.24g

1. For Drain-ballasted ESD NMOS :

- The overlap of SDI_2 and Gate should exactly equal to 0.060 μm .
- The overlap should occur in one-side only
- Without overlap is not allowed

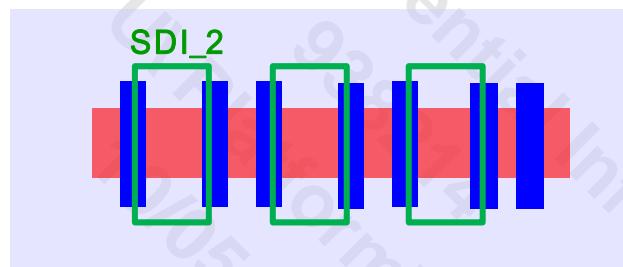


Figure 9.2.9 Example of ESD.24g

9.2.5.7 DRC methodology for ESD.31g

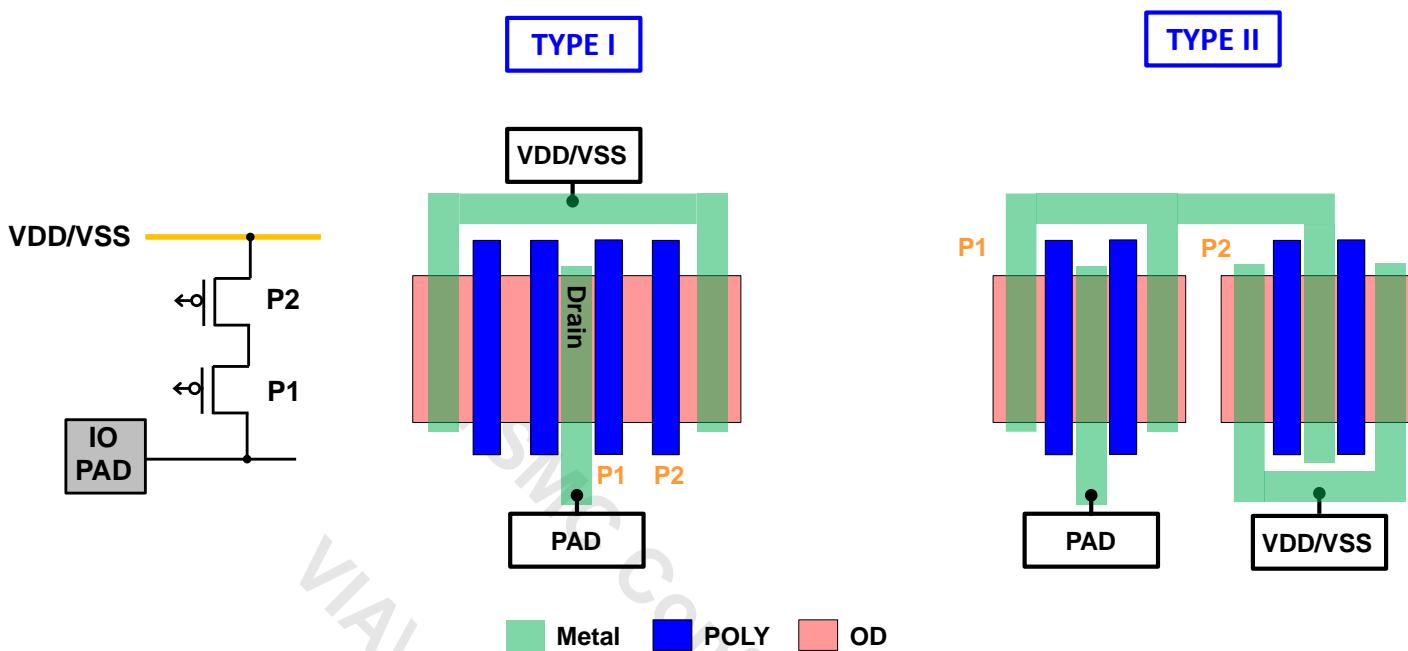
For 2-stage cascaded PMOS, there are two kinds of layout style, as shown in Figure 9.2.10 (a).

1. Type I: Two PMOSs are in the same OD with drain tie to IO pad
 2. Type II: Two PMOSs are in separate OD with source of P2 tied to VDD/VSS
- DRC would flag if source of P1 in type II ties to VDD/VSS

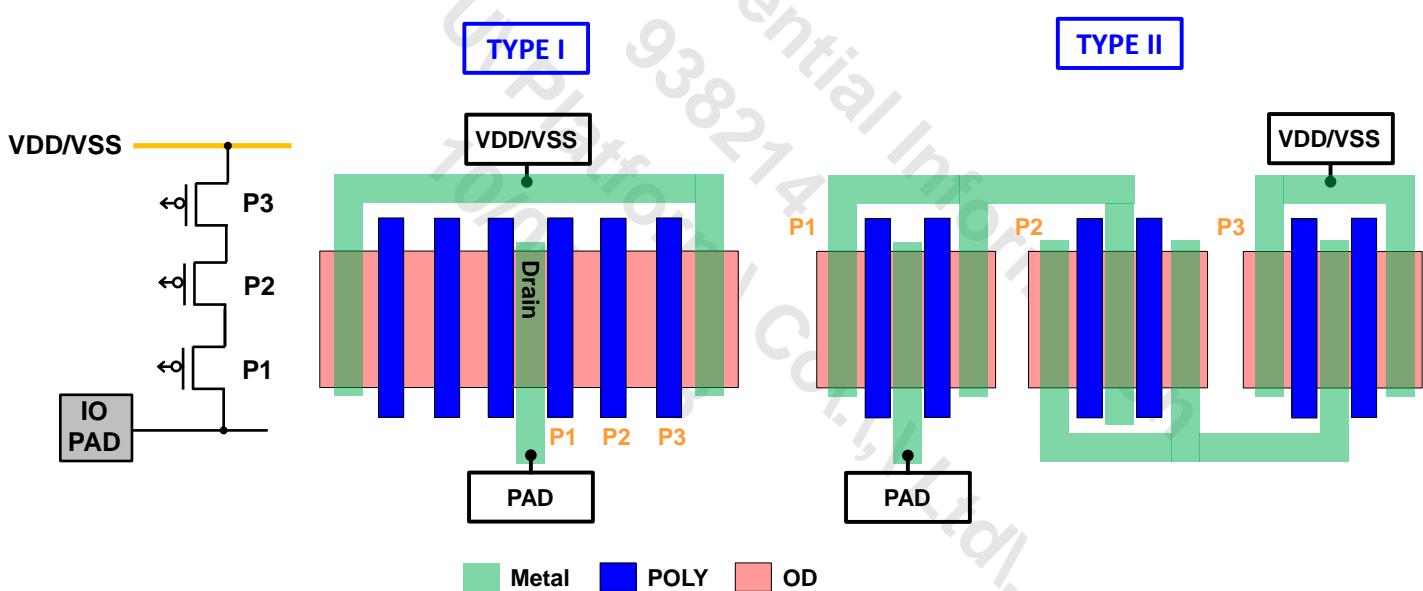
For 3-stage cascaded PMOS, there are two kinds of layout style, as shown in Figure 9.2.10(b).

1. Type I: Three PMOSs are in the same OD with drain tie to IO pad
 2. Type II: Three PMOSs are in separate OD with source of P3 tied to VDD/VSS
- DRC would flag if source of P1 in type II ties to VDD/VSS

If cascaded stages larger than three, DRC checking methodology follows the same method.



1. Two stages cascode PMOS layout style



2. Three stages cascode PMOS layout style

Note:

For products with CDM requirement, there is further layout/design constrain needs to be met.

- Snapback based primary protection scheme: Separated NW layout constrain is required (refer to ESD.CDM.1g and ESD.CDM.1.1g)
- Diode based primary protection scheme: Separated OD layout constrain is required. (refer to ESD.CDM.2g)

Figure 9.2.10 Cascoded PMOS Connection and Layout of ESD.31g

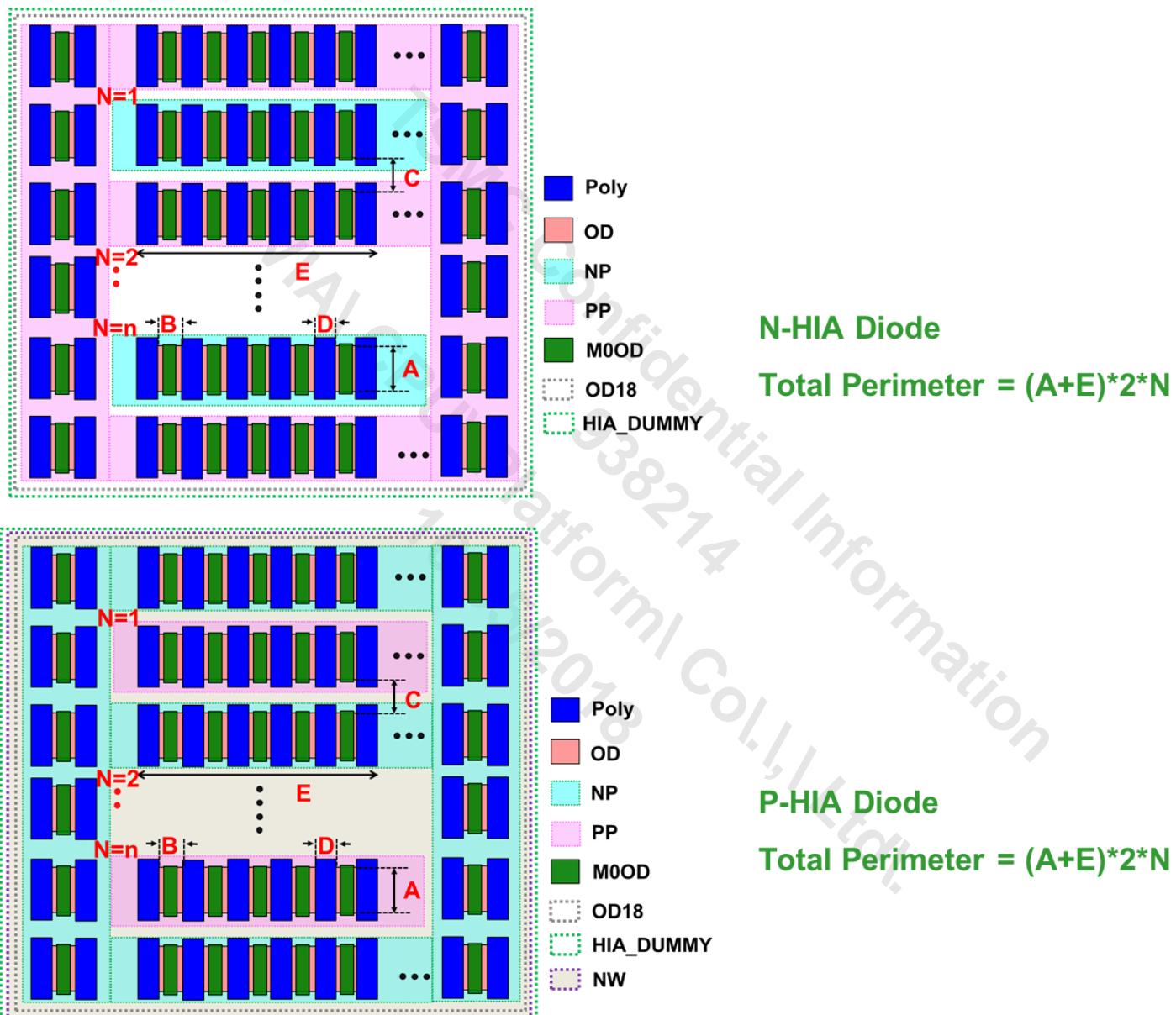
9.2.5.8 DRC methodology for HIA.3g

This check is for HIA.3q, total perimeter of HIA diode.

The total perimeter is calculated by the HIA diode in the same connection.

DRC check the diode perimeter only with diode connected to IO PAD.

The connectivity is broken by resistor for this check



9.2.5.9 DRC methodology for higher CDM requirement

By default, this DRM provides ESD guidelines for HBM2KV and CDM peak current 5A (FWHM <1ns). For products designed for higher CDM requirement, please turn on corresponding DRC switch and check related rules.

Table below shows the summary of DRC switch vs. ESD guidelines selective checked.

	GUIDELINE_ESD_CDM7A	GUIDELINE_ESD_CDM9A	GUIDELINE_ESD_CDM14A
ESD target	HBM2KV and CDM Ipeak 7A (FWHM <1ns)	HBM2KV and CDM Ipeak 9A (FWHM <1ns)	HBM2KV and CDM Ipeak 14A (FWHM <1ns)
Default settings	OFF	OFF	OFF
Selected rules when turning on switch	ESD.CDM7A.18g	ESD.CDM9A.18g	ESD.CDM14A.18g
	ESD.CDM7A.27g	ESD.CDM9A.27g	ESD.CDM14A.27g
	HIA.CDM7A.3g	HIA.CDM9A.3g	HIA.CDM14A.3g
	HIA.CDM7A.3.1g	HIA.CDM9A.3.1g	HIA.CDM14A.3.1g
	ESD.CDM7A.LC.3g	ESD.CDM9A.LC.3g	ESD.CDM14A.LC.3g
	ESD.CDM7A.LC.3.1g	ESD.CDM9A.LC.3.1g	ESD.CDM14A.LC.3.1g
	ESD.CDM7A.40g	ESD.CDM9A.40g	ESD.CDM14A.40g
	ESD.CDM7A.40.1g	ESD.CDM9A.40.1g	ESD.CDM14A.40.1g
	ESD.CDM7A.40.3g	ESD.CDM9A.40.3g	ESD.CDM14A.40.3g

Note:

1. To achieve higher CDM requirement, ESD device total size is enlarged (MOS channel width, diode Pj/ area). Please ensure good backend routing uniformity from end to end.
2. Similar to CDM Ipeak 5A, for CDM Ipeak 7A/9A/14A, both DRC checkable (listed above) and uncheckable ESD guidelines are necessary to follow.

9.2.6 ESD Guidelines

9.2.6.1 Whole chip ESD design scheme overview

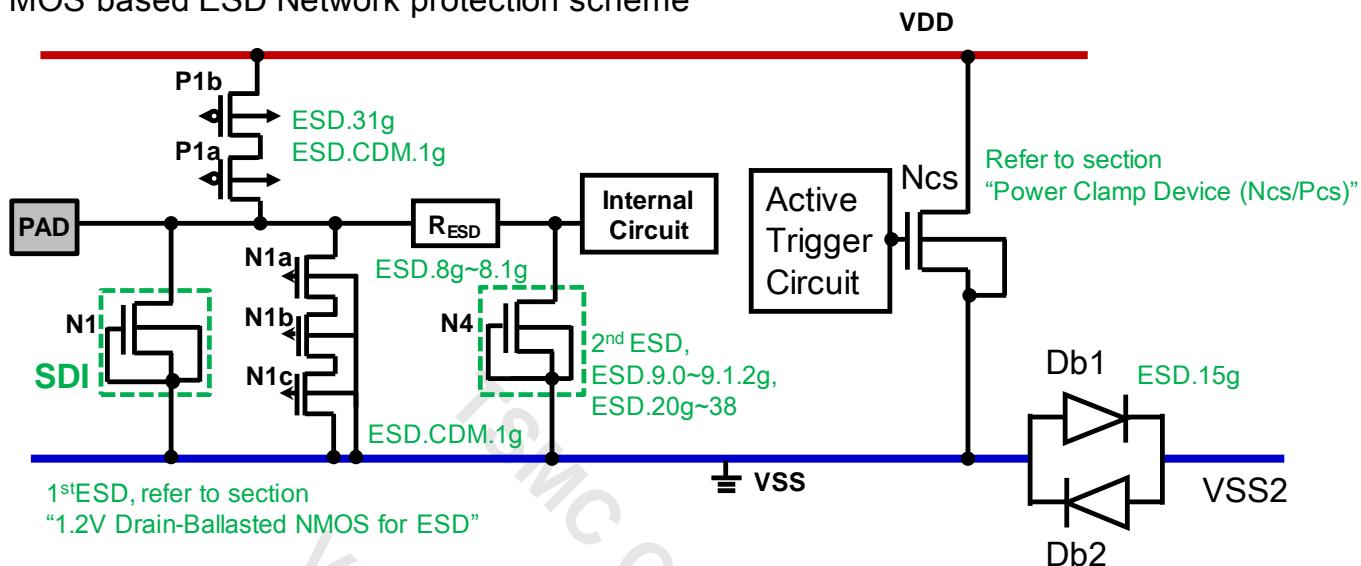
TSMC's N7+ ESD POR device target is 2KV for Human Body Model (HBM). CDM is with the peak current of 5A at FWHM< 1n sec.

The well designed ESD protection network is required for all I/O pads and Power/Ground pads.

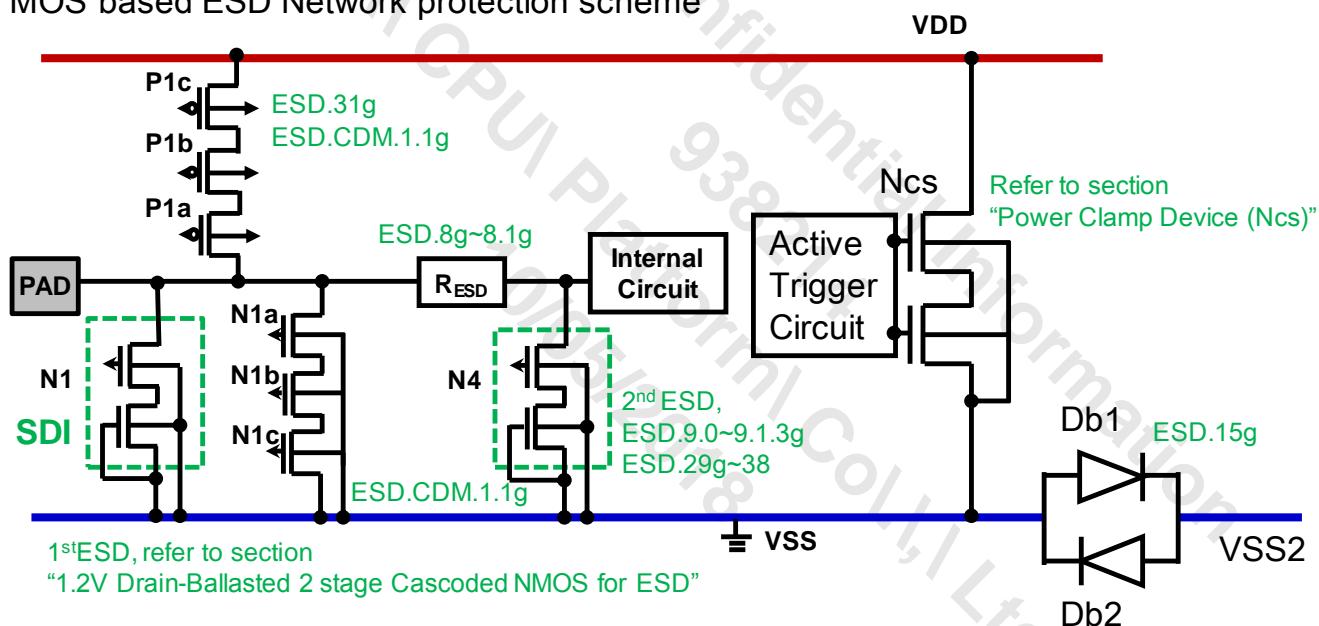
1. For I/O, input and output pin ESD protection scheme, the primary ESD (1st ESD) protection devices are required.
 - a. As the user plans to adopt tsmc ESD design scheme, the 1st ESD can be one of following listed devices.
 - i. Drain-ballasted NMOS (N1) (refer to the section of "1.8V Drain-Ballasted NMOS for ESD" and "1.8V Drain-Ballasted 2 stage Cascoded NMOS for ESD")
 - ii. HIA diode (D1/D2) (refer to the section of "Diode for ESD")
 - b. As PMOS is connected to IO PAD, the PMOS must be cascaded structure. (refer to ESD.31g)
 - c. ESD.NET.1g^U is for the existence checking of 1st ESD.
2. For input pin ESD protection scheme or high ESD risk victim, the secondary ESD protection (2nd ESD) (N4/D3/D4) devices and ESD resistor (R_{ESD}) are required.
 - a. Refer to ESD.8g^U and ESD.8.1g^U for R_{ESD} guideline.
 - b. Refer to ESD.9.0~3g^U for 2nd ESD related guidelines.
3. For Power and ground pin ESD protection scheme, power clamp (Ncs) and back to back diode (Db1 and Db2) are must for each power pin and ground pin.
 - a. Refer to the section of "Power Clamp Device"
 - b. Refer to ESD.15g for back to back diode guideline.
4. If the ESD circuit design is based on TSMC ESD protection scheme, either dual-diode based or MOS/snapback based ESD protection design guidelines is required to be followed. Dual-diode ESD guideline DRC violation can only be waived on the condition that MOS/snapback-based guideline is followed, vice versa for Dual-diode ESD centric design.
5. Furthermore, internal circuit and ESD circuit co-design is essential. For example, for N/PMOS post-driver under dual-diodes based or MOS/snapback based ESD protection, it is required to follow guidelines in 9.2.7.3. Circuits beyond the scope of these guidelines, extra case-by-case reviews are needed.

Following shows the suggested ESD protection network.

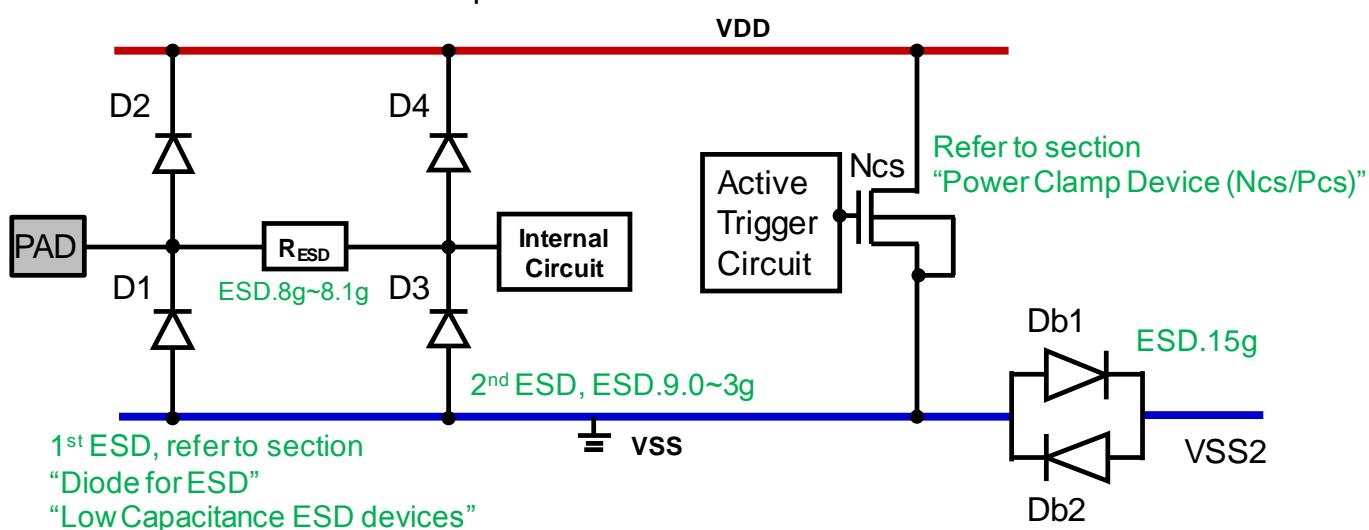
MOS based ESD Network protection scheme



MOS based ESD Network protection scheme



Diode based ESD Network protection scheme



9.2.6.2 General Guideline for ESD Protection

Rule No.	Description	Label	Op.	Rule
ESD.NET.1g ^U	<p>For I/O pin ESD protection scheme, the primary ESD protection (1st ESD) devices are required and it can be one of following listed devices.</p> <ol style="list-style-type: none"> 1. Single stage Drain-ballasted NMOS (refer to ESD.18g~38) 2. 2-stage cascoded Drain-ballasted NMOS (refer to ESD.18g~38) 3. HIA diode (single stage or 2-stacked) (refer to HIA.1~18g) (ESD device size requirement is changed with target CDM level. For details, please refer to 9.2.5.9) 			
ESD.NET.1.1g ^U	<p>For 3.3V I/O pin ESD protection scheme, the primary ESD protection (1st ESD) devices are required and it can be one of following listed devices. Single stage Drain-ballasted NMOS is not allowed.</p> <ol style="list-style-type: none"> 1. 2-stage cascoded Drain-ballasted NMOS 2. HIA diode (single stage or 2-stacked) <p>(ESD device size requirement is changed with target CDM level. For details, please refer to 9.2.5.9)</p>			
ESD.WARN.1	<p>[SDI (122;0) AND ACTIVE] needs to be found in each power pad of CB, CB2, and UBM. [One of ESD dummy layers AND ACTIVE] needs to be found in each IO pad and ground pad of CB, CB2, and UBM. The ESD dummy layers include SDI (122;0), and HIA_DUMMY (168;0).</p> <p>Exception: SEALRING_ALL</p> <p>When turn on option "define_pad_by_text", only check connectivity of CB, CB2, and UBM with text</p> <p>When turn off option "define_pad_by_text", only check connectivity of CB, CB2, and UBM to STRAP/VDDDMY/VSSDMY/IODMY</p>			
ESD.WARN.2	SDI enclosure of ACTIVE		≥	0
ESD.WARN.3g ^U	<p>If the circuits have core gate directly tie to VDD(VSS) and source/drain tie to VSS(VDD), rules below must be followed to get the ESD design scheme robust.</p> <ol style="list-style-type: none"> 1. ESD.14.4g, ESD.40.1g and ESD.43g for HBM 2. ESD.CDM.P.3g, ESD.CDM.P.7.1.1g, ESD.CDM.P.7.1.2g, ESD.40.1g, ESD.43g, ESD.CDM.C.2g and ESD.CDM.C.3.1g for CDM <p>As for Decap and footer/header design, they can be exempted. (ESD device size and Rbus resistance requirements are changed with target CDM level. For details, please refer to 9.2.5.9 and 9.2.7.3)</p>			
ESD.WARN.3.1g ^U	<p>As core gate connects to IOPAD directly or through resistor, the source/drain cannot connect to any power/ground directly or through resistor.</p> <p>As source/drain connects to IOPAD directly or through resistor, the core gate cannot connect to any power/ground directly or through resistor. (Figure 9.2.12)</p> <p>ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.</p>			
ESD.WARN.4.2g ^U	<p>For cascoded power clamp protected power domain, As IO gate connects to power directly, the source/drain cannot connect to ground directly.</p> <p>As source/drain connects to power directly or through resistor, the IO gate cannot connect to ground directly. (Figure 9.2.13).</p>			

Rule No.	Description	Label	Op.	Rule
ESD.1g	<p>It is not allowed that IO MOS with SDI connects to core MOS. (Figure 9.2.14).</p> <p>DRC will flag the following condition: ((MOS INTERACT OD2) INTERACT SDI) connected to (MOS NOT INTERACT OD2)</p> <p>DRC will exclude Drain/Source/Gate connected to {(PW NOT RW) STRAP} or VSS net.</p>			
ESD.1.1g ^U	<p>Use thick oxide transistor for thick oxide secondary ESD protection (2nd ESD, N4). (Figure 9.2.14)</p> <p>For diode based 2nd ESD protection, use thin oxide transistor (Mp/Mn) for thin oxide power clamp (Ncs); use thick oxide transistor (Mp/Mn) for thick oxide power clamp (Ncs) (Fig 9.2.14.1)</p> <p>Thick oxide ESD protection or power clamp connect to thin oxide transistor is not allowed.</p> <p>Both input pin and cross domain 2nd ESD are required to comply with this rule.</p>			
ESD.5g	<p>The same type OD of the Power Clamp should be surrounded by a guard-ring (pick-up ring). All other type ODs should be placed outside this guard-ring (pick-up ring). DRC will flag the following conditions:</p> <ol style="list-style-type: none"> 1. Different type ODs in the most inner guard-ring (pick-up ring). 2. OD not inside the most inner guard-ring (pick-up ring). 			
ESD.6g	<p>Drain-ballasted NMOS should be surrounded by one outer P+ pick-up ring only. All other P-type straps or guard-ring should be placed outside this pick-up ring.</p> <p>DRC will flag the following conditions:</p> <p>Any kind of p-type strap inside the out-most pick-ring.</p>			
ESD.8g ^U	<p>Value of resistor R_{ESD} (ohm) between the internal circuits with gate oxide ESD path and IO pad.</p> <p>If the design is verified by ESD network calculator, it can be exempted.</p> <p>For snapback based ESD protection scheme, secondary ESD protection device total channel width multiplies with RESD resistor value should be $\geq 1600\mu m \cdot \text{ohm}$. Also, primary ESD device and secondary ESD device should be “both single-stage” or “both 2-stage”, and primary ESD device and secondary ESD device should be on the common ground. These are checked by ESD.CDM.1g, ESD.CDM.1.1g and ESD.CDM.1.3g.</p>		\geq	200
ESD.8.1g ^U	Minimum width of $R_{ESD}(\text{rhim})$ resistor.		\geq	1.8500
ESD.CDM7A.8.1g ^U	Minimum width of $R_{ESD}(\text{rhim})$ resistor		\geq	1.8500
ESD.CDM9A.8.1g ^U	Minimum width of $R_{ESD}(\text{rhim})$ resistor		\geq	2.4000
ESD.CDM14A.8.1g ^U	Minimum width of $R_{ESD}(\text{rhim})$ resistor		\geq	3.7000

Rule No.	Description	Label	Op.	Rule
ESD.9.0g ^U	<p>Either MOS based or diode based secondary ESD protection (2nd ESD) with ESD resistor is required for internal circuits with gate oxide ESD path between IOPAD and power/ground PAD. This rule checks on internal circuits with single stage, 2-stage or > 2-stage gate oxide ESD path to VDD/VSS. (Figure 9.2.16.1/9.2.16.2/9.2.16.3) For N/PMOS mixed scenario, it's checked as well.</p> <p>For 2nd ESD, HIANMOS (single stage and 2-stage cascoded) and HIA diodes can be used and needs to be put between resistor and the internal circuit. (N4 in Figure 9.2.17.1 and D3/D4 in Figure 9.2.17.2)</p> <p>Exception:</p> <ol style="list-style-type: none"> 1. Dummy device (D/G/S shorted) is exempted from this rule check. 2. Single stage or cascoded (2-stage) snapback NMOS as primary or secondary ESD protection. 3. Single stage I/O gate oxide ESD path with source or drain tied to IOPAD through resistor (device width*Rout \geq 100um*ohm) and gate tied to VDD or VSS. 4. Cascoded gate oxide ESD path with source or drain tied to IOPAD through resistor (device width*Rout \geq 100um*ohm) and 2nd- stage tied to VDD or VSS. 5. Cascoded gate oxide ESD path [through one or more I/O GOX] with source or drain tied to IOPAD directly or through resistor and 2nd-stage tied to VDD or VSS. 6. Cascoded (> 2 stack) gate oxide ESD path with source or drain tied to IOPAD. <p>ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.</p>			
ESD.9.0.1g ^U	<p>For 3.3V application, the secondary ESD protection device with ESD resistor is required for input path and it can be one of following listed devices. Single stage Drain-ballasted NMOS is not allowed.</p> <ol style="list-style-type: none"> 1. 2-stage cascoded Drain-ballasted NMOS 2. HIA diode (single stage) 			
ESD.9.1g ^U	<p>Channel length for 1.8V single stage drain-ballasted NMOS (N4) and 2-stage cascoded drain-ballasted NMOS of MOS based ESD secondary protection (2nd ESD) in Figure 9.2.17.1.</p> <p>The drain-ballasted NMOS for 2nd ESD purpose needs to follow ESD.20g~ESD.26.1 and ESD.29g~ESD.38 in chap.9.2.6.3 and chap.9.2.6.4</p>		=	0.1350
ESD.9.1.1g ^U	<p>Channel width for 1.8V single stage drain-ballasted NMOS (N4) and 2-stage cascoded drain-ballasted NMOS of MOS based ESD secondary protection (2nd ESD) in Figure 9.2.17.1.</p> <p>The drain-ballasted NMOS for 2nd ESD purpose needs to follow ESD.20g~ESD.26.1 and ESD.29g~ESD.38 in chap.9.2.6.3 and chap.9.2.6.4</p> <p>For snapback based ESD protection scheme, secondary ESD protection device total channel width multiplies RESD resistor value should be \geq 1600um*ohm. Also, primary ESD device and secondary ESD device should be “both single-stage” or “both 2-stage”, and primary ESD device and secondary ESD device should be on the common ground. These are checked by ESD.CDM.1g, ESD.CDM.1.1g and ESD.CDM.1.3g.</p>		\geq	8

Rule No.	Description	Label	Op.	Rule
ESD.9.1.2g ^U	Unit OD width of 1.8V single stage drain-ballasted NMOS (N4) and 2-stage cascoded drain-ballasted NMOS of MOS based ESD secondary protection (2nd ESD) in Figure 9.2.17.1. The drain-ballasted NMOS for 2nd ESD purpose needs to follow ESD.20g~ESD.26.1 and ESD.29g~ESD.38 in chap.9.2.6.3 and chap.9.2.6.4		=	0.5780
ESD.9.1.3g ^U	2-stage cascoded drain-ballasted NMOS of MOS based ESD secondary protection (2nd ESD) needs to be common OD structure			
ESD.9.3g ^U	Total perimeter of HIA diode (D3/D4) of diode based ESD secondary protection (2nd ESD) in Figure 9.2.17.2, the perimeter calculation align with HIA diode.		\geq	4
ESD.9.5g ^U	Gate oxide connected to IOPAD directly or through resistor should be surrounded by a P+ guard ring. N/PMOS can share the same ring.			
ESD.14.3g ^U	1. Resistance of the Power bus line from IO pad to the closest Power clamp. (R1+R2+R4 in Figure 9.2.19.2) (Ω) 2. Resistance of the ground bus line from IO pad to the closest Power clamp. (R1+R5+R6 in Figure 9.2.19.2) (Ω) If the IO PAD connects to ESD cell first, the R1 can be ignored.		\leq	1
ESD.14.4g ^U	Resistance of the bus line from Power pad to the closest GND pad. (R3+R4+R6+R7 in Figure 9.2.19.1~3) (Ω) If the Power/Ground PAD connects to power clamp first, this rule can be waived.		\leq	1
ESD.14.5g ^U	Resistance of the bus line from 2 nd ESD Diode to the closest Power Clamp. 1. Resistance of the power bus line from 2 nd ESD diode to the closest Power clamp. (R2' in Figure 9.2.19.4) (Ω) 2. Resistance of the ground bus line from 2 nd ESD diode to the closest Power clamp. (R5' in Figure 9.2.19.4) (Ω)		\leq	10
ESD.14.6g ^U	Resistance of bus line from the pick-up ring of LUP.1.0.1 ^U to the closest Power / Ground Pad (Ω)		\leq	1
ESD.14.7g ^U	Resistance of bus line from the pick-up ring/ guard-ring/ strap of LUP.2.0.1 ^U and LUP.2.1 ^U to the closest Power / Ground Pad (Ω)		\leq	10
ESD.14.8g ^U	Resistance of bus line from the guard-ring of LUP.14.0.1 ^U to the closest Power / Ground Pad (Ω)		\leq	10
ESD.15g ^U	Bypass discharge cells should be inserted between each separate Vss to avoid ESD damage to internal circuits. The suggested bypass discharge cell is back to back diode (Figure.9.2.21) and it can be HIA diode. The perimeter of back to back diodes (Db1/Db2) needs to meet HIA.3g The connections are illustrated in Figure 9.2.20. (For more details, please see the “Tips for the Power Protection” section in this chapter.) (ESD device size requirement is changed with target CDM level. For details, please refer to 9.2.5.9)			

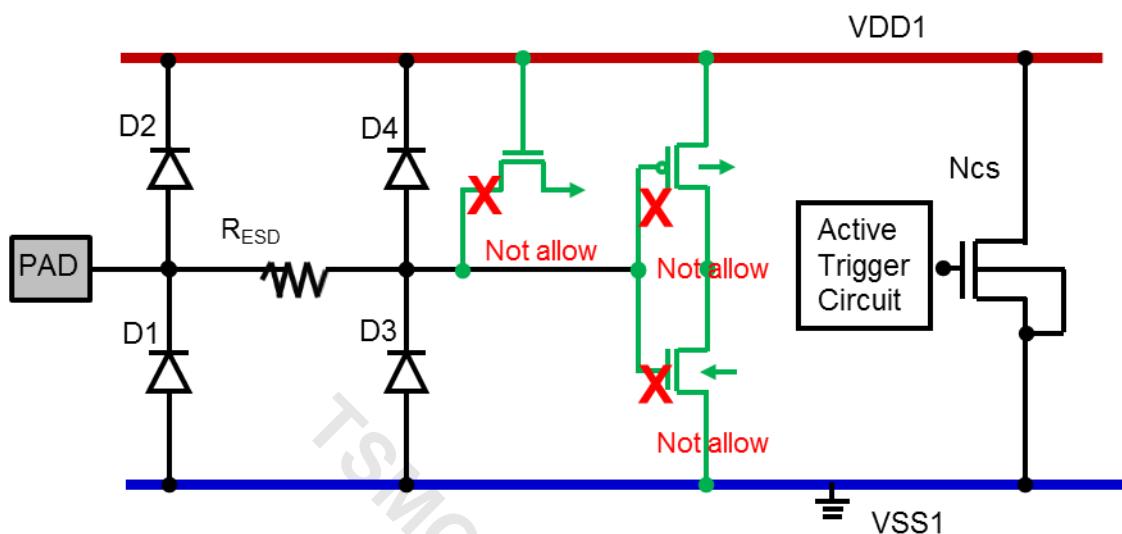
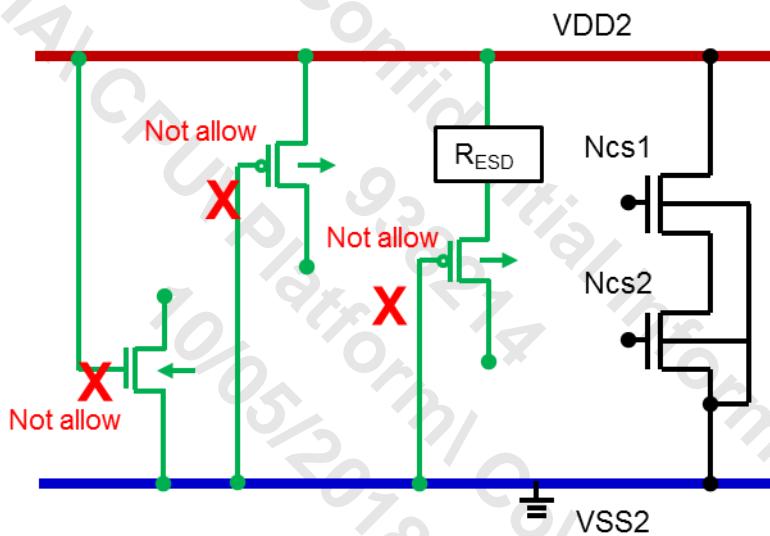
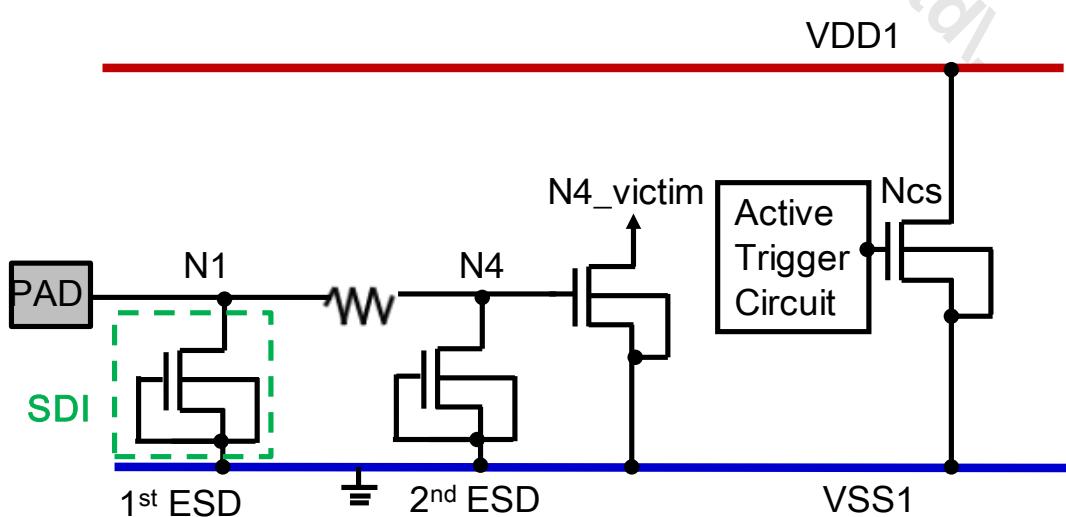
Figure 9.2.12 Diagram for ESD.WARN.3.1^UFigure 9.2.13 Diagram for ESD.WARN.4.2^U

Figure 9.2.14 Diagram for ESD.1.1gU with I/O HIANMOS as secondary ESD Device

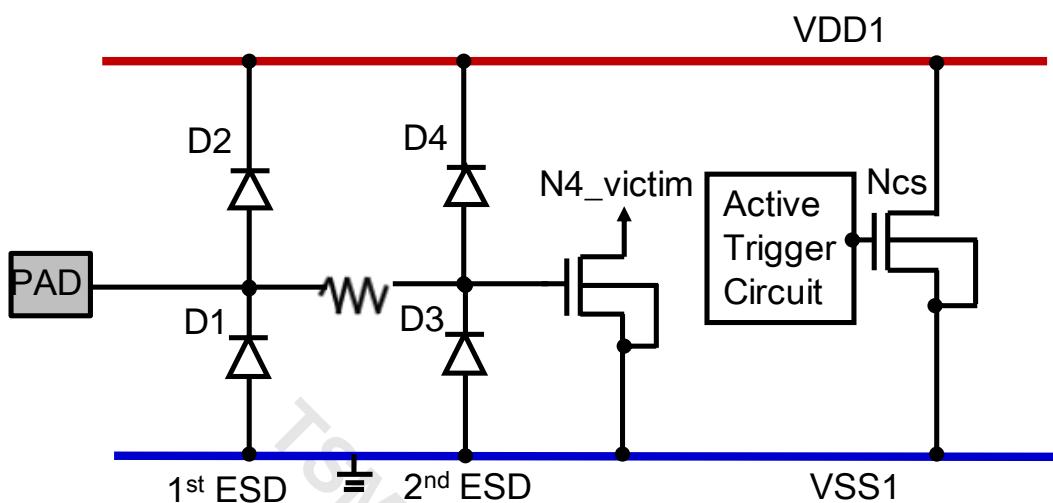


Figure 9.2.14.1 Diagram for ESD.1.1gU with dual diode as secondary ESD Device

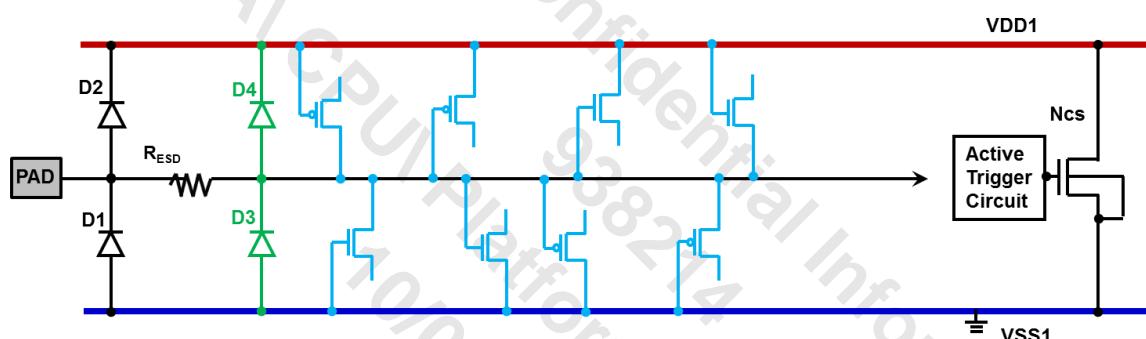


Figure 9.2.16.1 Single stage gate oxide ESD path to VDD/VSS

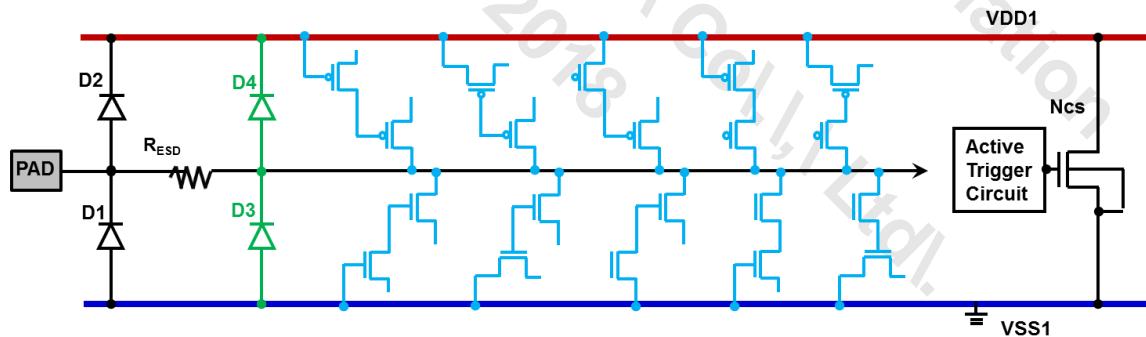


Figure 9.2.16.2 2-stack cascoded gate oxide ESD path to VDD/VSS with MOS source/drain connected to IOPAD.

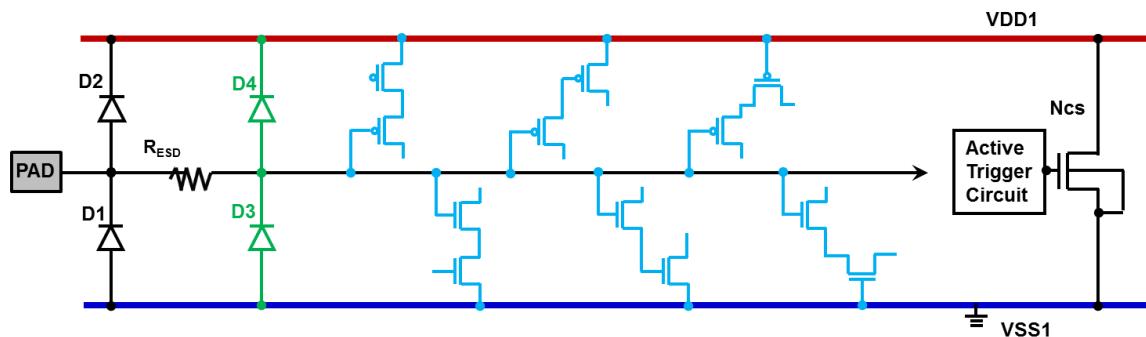


Figure 9.2.16.3 2-stack cascoded gate oxide ESD path to VDD/VSS with MOS gate connected to IOPAD

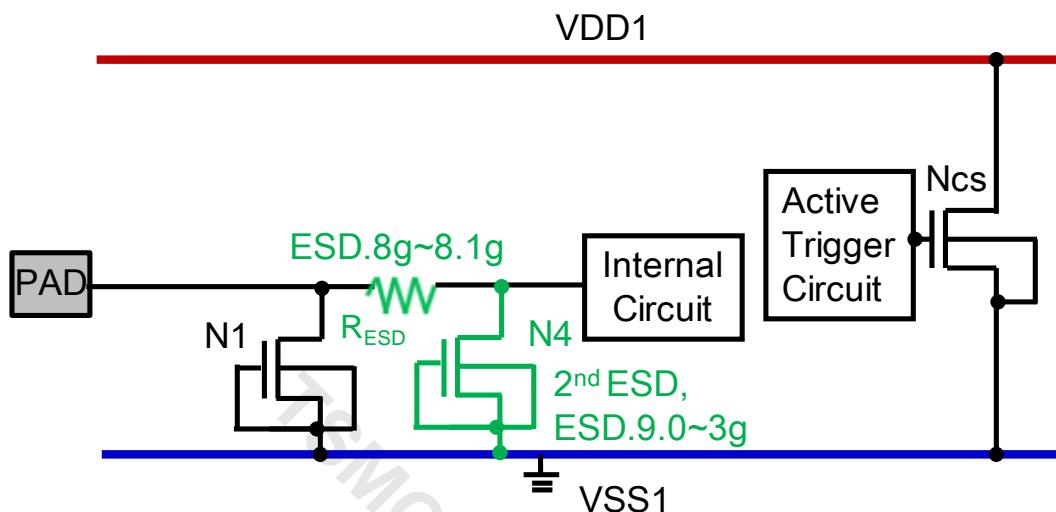


Figure 9.2.17.1 MOS-based 2nd ESD protection scheme

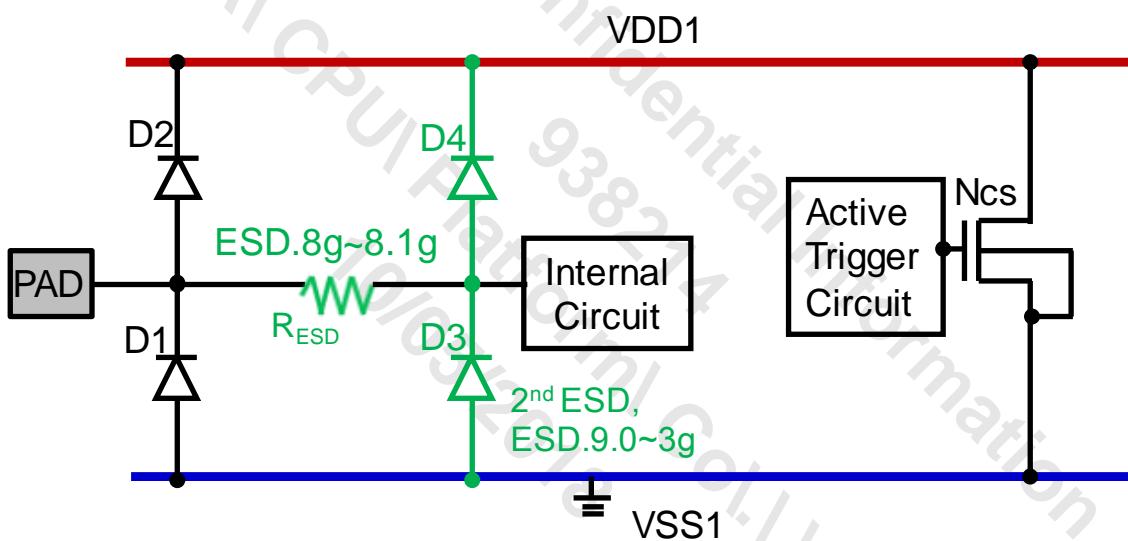
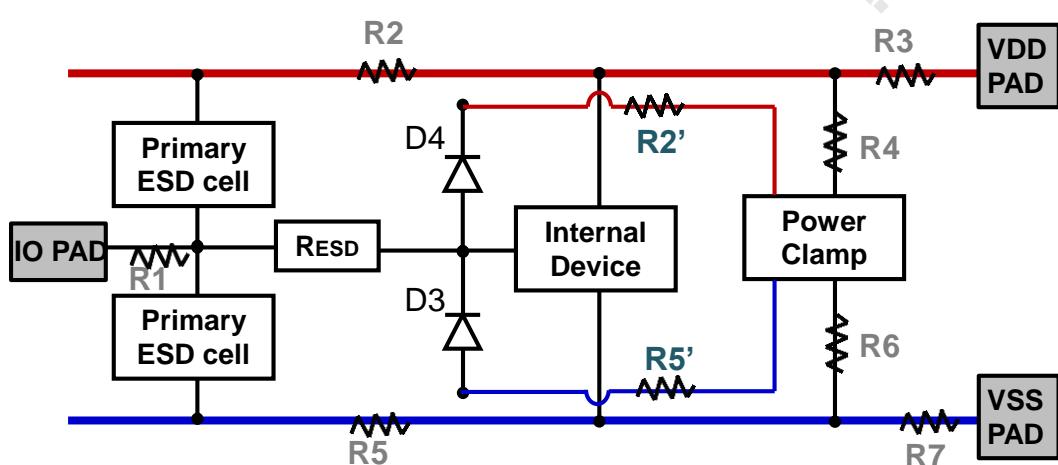
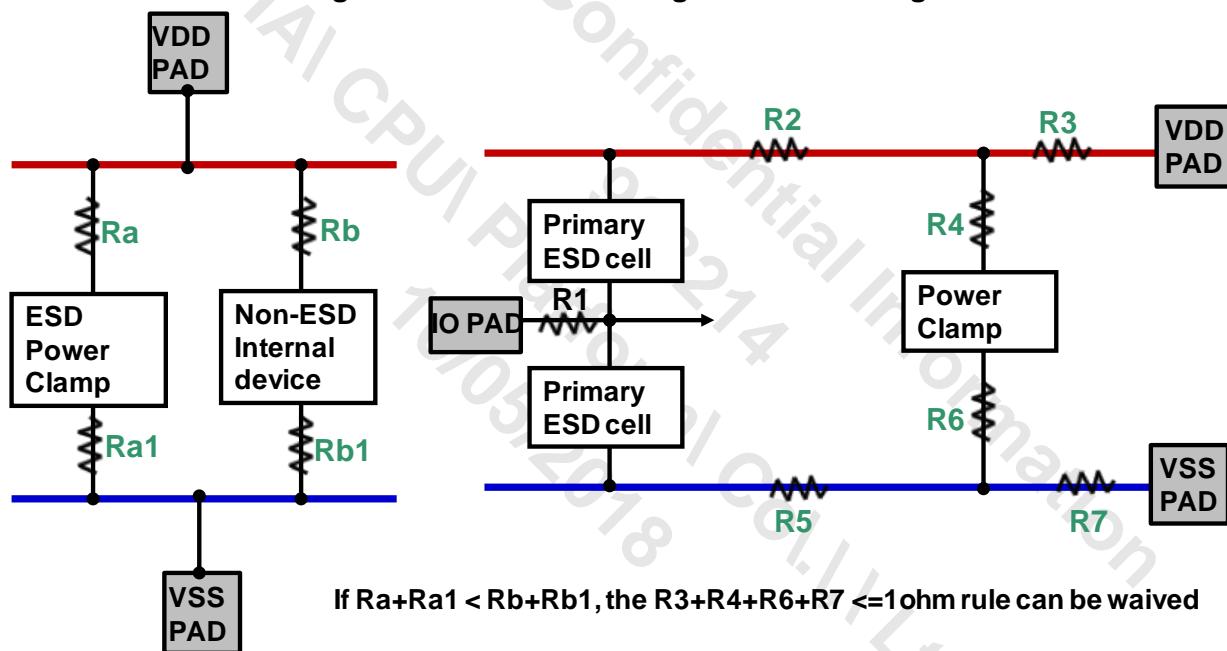
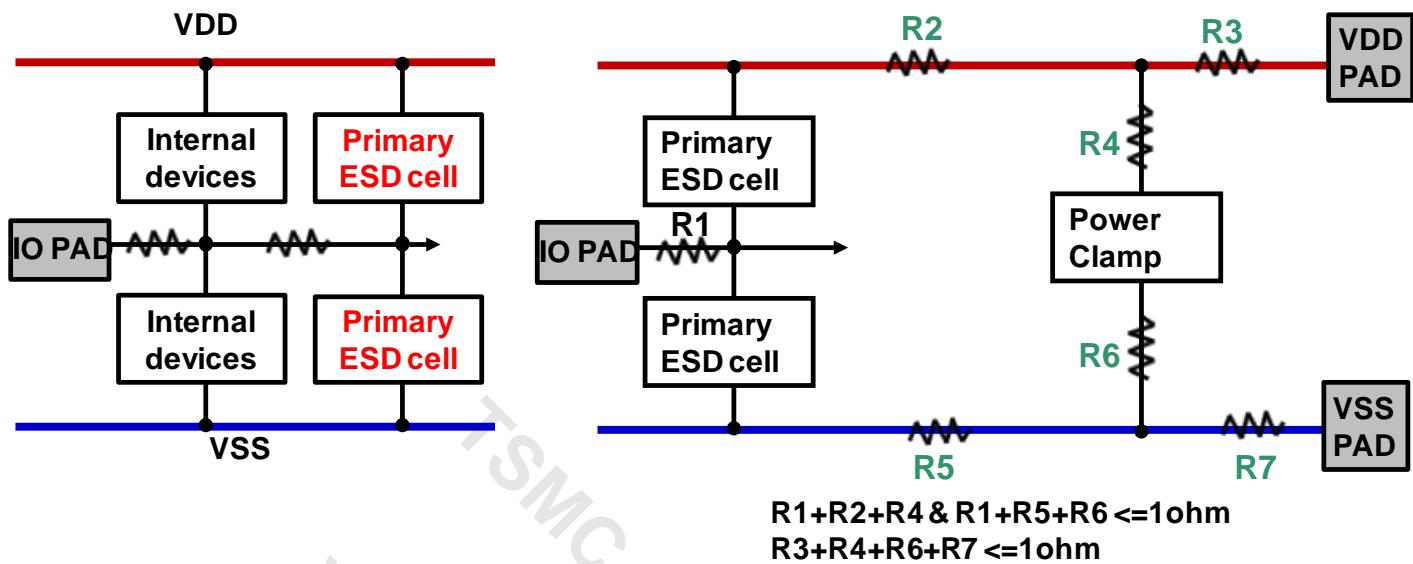


Figure 9.2.17.2 Diode-based secondary protection



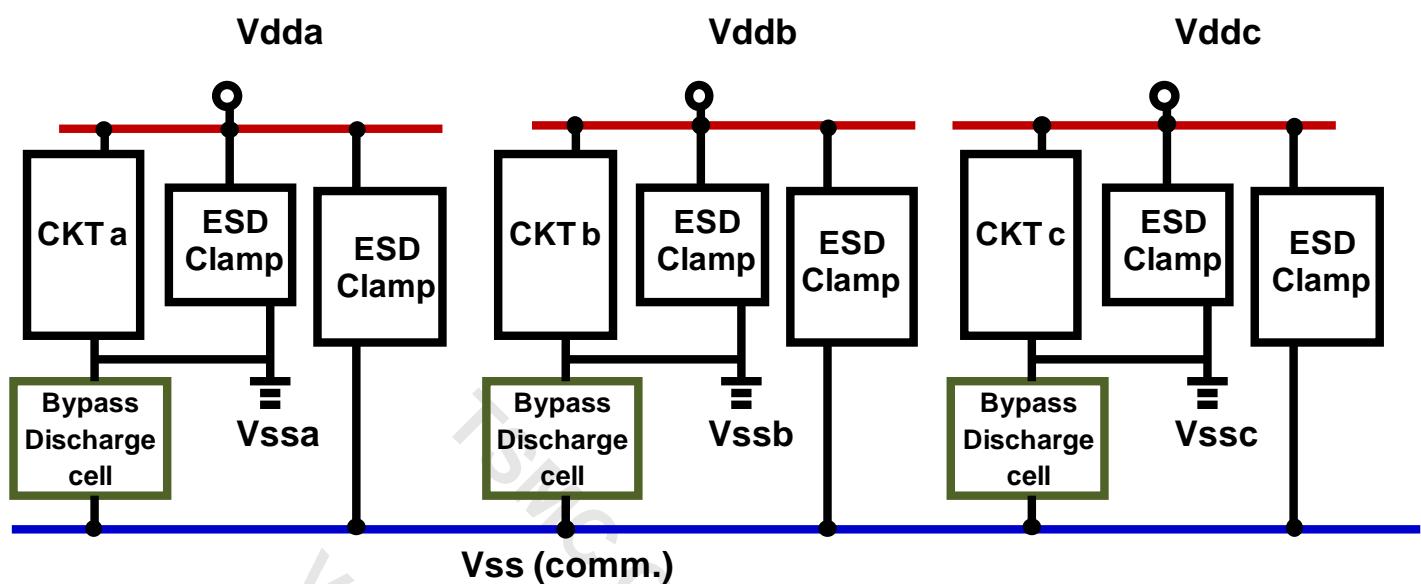


Figure 9.2.20 Schematic of a Multiple Power ESD Protection Design

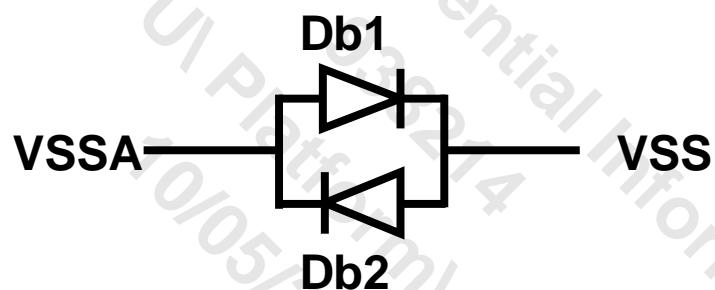


Figure 9.2.21 Schematic of a back to back (B2B) diode

9.2.6.3 1.8V Drain-Ballasted NMOS for ESD

- DRC deck uses (N+ ACTIVE AND SDI AND SR_ESD AND OD2) AND (some of the related Gate partially overlap SDI_2 but not fully INSIDE SDI_2) to recognize drain-ballasted NMOS.
- The 1.8V drain-ballasted NMOS can be used as primary ESD protection device (1st ESD) and secondary ESD protection device (ESD.9.1g, ESD.9.1.1g and ESD.9.1.2g^U)

Rule No.	Description	Label	Op.	Rule
ESD.18g	<p>Total finger width of NMOS in same connection of IO PAD.</p> <p>NMOS stated above [one side connected to IOPAD, the other side connected to PWSTRAP directly], inside same PWSTRAP enclosed area, should meet total finger width criteria as well.</p> <p>Inside each of PWSTRAP enclosed area, drain of NMOS stated above should be shorted together. This is checked in ESD.36.</p>		\geq	490
ESD.CDM7A.1 8g	<p>Total finger width of NMOS in same connection of IO PAD.</p> <p>NMOS stated above [one side connected to IOPAD, the other side connected to PWSTRAP directly], inside same PWSTRAP enclosed area, should meet total finger width criteria as well.</p> <p>Inside each of PWSTRAP enclosed area, drain of NMOS stated above should be shorted together. This is checked in ESD.36.</p> <p>(This rule is enabled when DRC option “GUIDELINE_ESD_CDM7A” is switched on)</p>		\geq	780
ESD.CDM9A.1 8g	<p>Total finger width of NMOS in same connection of IO PAD.</p> <p>NMOS stated above [one side connected to IOPAD, the other side connected to PWSTRAP directly], inside same PWSTRAP enclosed area, should meet total finger width criteria as well.</p> <p>Inside each of PWSTRAP enclosed area, drain of NMOS stated above should be shorted together. This is checked in ESD.36.</p> <p>(This rule is enabled when DRC option “GUIDELINE_ESD_CDM9A” is switched on)</p>		\geq	990
ESD.CDM14A.18g	<p>Total finger width of NMOS in same connection of IO PAD.</p> <p>NMOS stated above [one side connected to IOPAD, the other side connected to PWSTRAP directly], inside same PWSTRAP enclosed area, should meet total finger width criteria as well.</p> <p>Inside each of PWSTRAP enclosed area, drain of NMOS stated above should be shorted together. This is checked in ESD.36.</p> <p>(This rule is enabled when DRC option “GUIDELINE_ESD_CDM14A” is switched on)</p>		\geq	1470
ESD.20g	Channel length: 1.8V drain-ballasted NMOS (in OD_18) (Figure 9.2.22)	L	\geq	0.1350
ESD.23	NMOS drain side MD to poly spacing (Figure 9.2.22)	X	=	0.1600
ESD.24	Overlap of SDI_2 on the drain side to the poly gate (Figure 9.2.5)	Z	=	0.0600
ESD.26	SR_DPO [INTERACT SDI_2] space to PO in horizontal direction	M	=	0.2320

Rule No.	Description	Label	Op.	Rule
ESD.36	<p>Each HIANMOS group must be surrounded by (PWSTRAP inside OD2)</p> <p>1. PWSTRAP enclosed area cannot contain other ACTIVE OD or NW/PWSTRAP except 1.8V_HIANMOS and 3.3V_HIANMOS. 2. For each of HIANMOS group, the drain should be shorted together, respectively. 3. 1.8V_HIANMOS and 3.3V_HIANMOS cannot inside the same region. HIANMOS group = 1.8V_HIANMOS /3.3V_HIANMOS inside same SR_ESD 1.8V_HIANMOS = ((N+ACTIVE INTERACT SDI_2) NOT INTERACT ((GATE NOT INTERACT PODE_GATE) NOT INTERACT SDI_2)) 3.3V_HIANMOS = ((N+ACTIVE INTERACT SDI_2) INTERACT ((GATE NOT INTERACT PODE_GATE) NOT INTERACT SDI_2)) This rule checks on 1.8V_HIANMOS and 3.3V_HIANMOS.</p>			
ESD.36.1	For each of PWSTRAP enclosed area, only one SR_ESD can be found. This rule checks on single stage drain-ballasted NMOS and cascoded drain-ballasted NMOS.			
ESD.36.2g	<p>Aspect ratio of HIANMOS array connected to IOPAD (Figure 9.2.22.2)</p> <p>HIANMOS array connected to IOPAD = ((OD INTERACT SDI_2) connected to IOPAD) sizing up/down 0.281 μm in vertical direction Aspect ratio = Vertical width / Horizontal width</p> <p>DRC flags on non-rectangular HIANMOS array state above This rule checks on single stage drain-ballasted NMOS and cascoded drain-ballasted NMOS.</p>		=	0.74~1.34
ESD.37	Number of VC interacted each of {{(MD NOT CMD) INTERACT {N+ACTIVE INTERACT SR_ESD}} and connected to IO, power and ground PAD. This rule checks on OD with nfin > 12 inside SR_ESD. This rule checks on single stage drain-ballasted NMOS and cascoded drain-ballasted NMOS.		≥	2
ESD.38	<p>For ESD protection purpose, drain side of HIANMOS should be connected to IOPAD directly as primary protection or connected to resistor with RES200 as 2nd protection.</p> <p>DRC flags following conditions:</p> <ol style="list-style-type: none"> 1. Drain side of HIANMOS connected to PSTRAP directly is not allowed. 2. Source side of HIANMOS connected to IOPAD directly is not allowed. 3. Source side of cascoded HIANMOS connected to PSTRAP directly is not allowed. <p>(Figure 9.2.22.1)</p> <p>Drain side of HIANMOS = {{(N+ ACTIVE NOT PO) AND SDI_2} AND SR_ESD}</p> <p>Source side of HIANMOS = {{(N+ ACTIVE NOT PO) INTERACT {PO INTERACT SDI_2} AND SR_ESD} NOT SDI_2}</p> <p>Cascoded HIANMOS = {{{(N+ ACTIVE AND SDI) AND SR_ESD) AND OD2) AND (some of the related Gate partially overlap SDI_2 and some of the related Gate [NOT PODE_GATE] outside SDI_2)}}</p>			

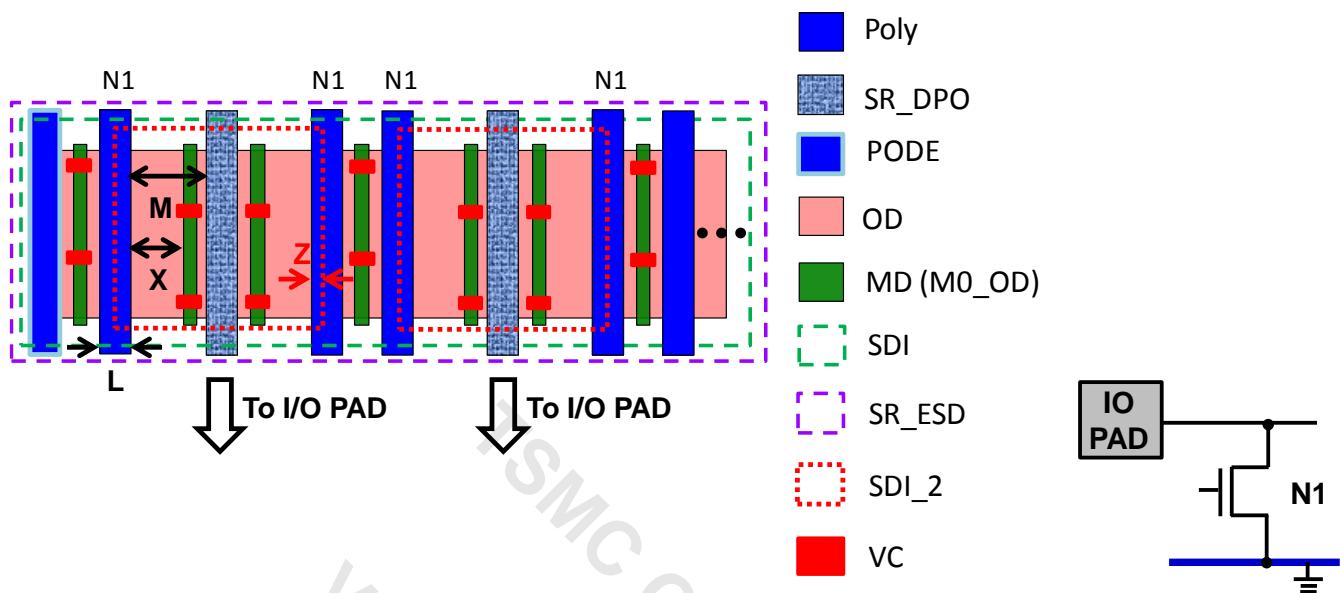


Figure 9.2.22 NMOS (N1 Figure 9.1.17) for I/O pin ESD protection

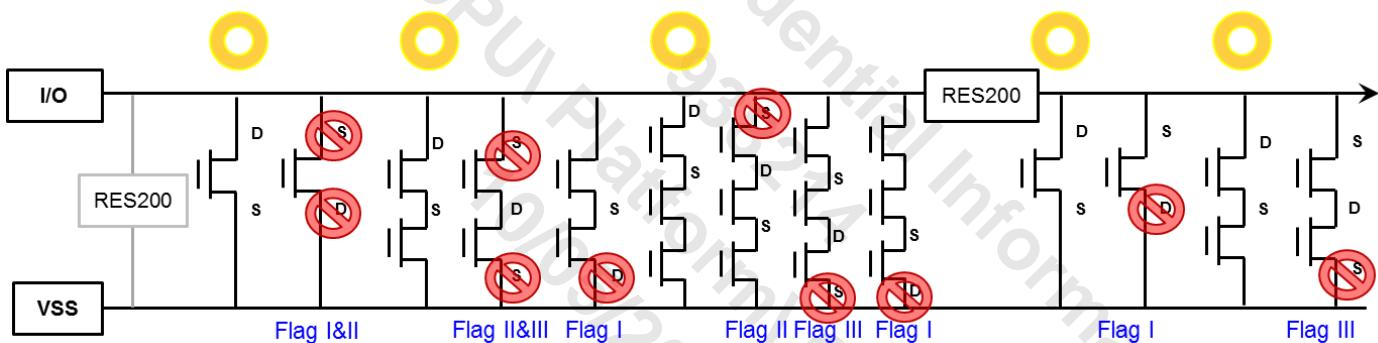


Figure 9.2.22.1 HIANMOS usage

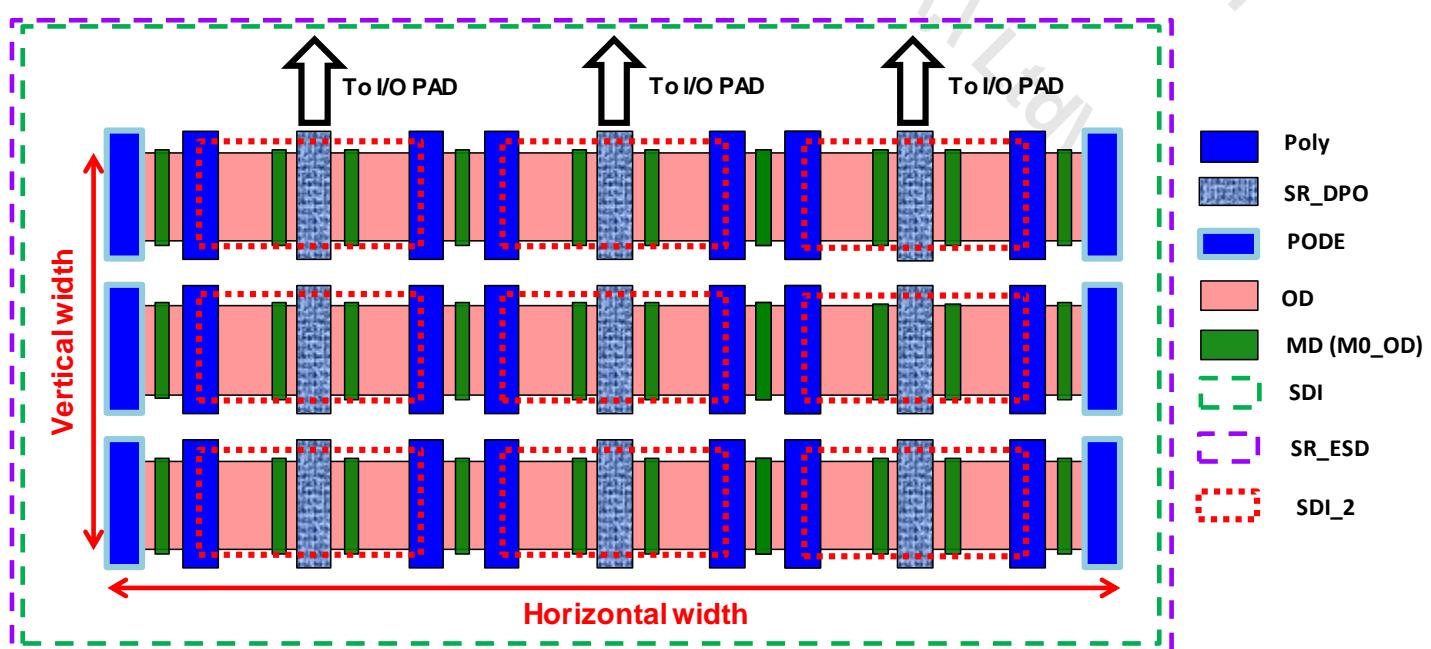
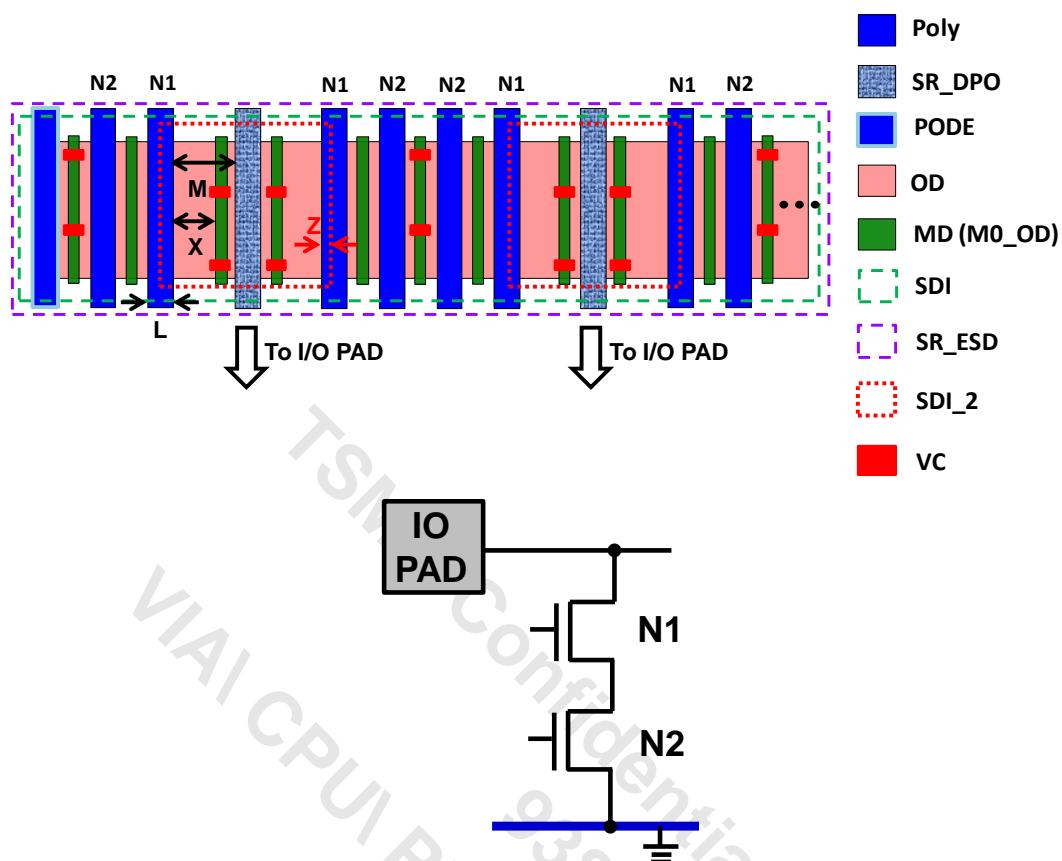


Figure 9.2.22.2 Aspect ratio of HIANMOS array

9.2.6.4 1.8V Drain-Ballasted 2 stage Cascoded NMOS for ESD

- DRC deck uses (N+ ACTIVE AND SDI AND SR_ESD AND OD2) AND (some of the related Gate partially overlap SDI_2 and some of the related Gate [NOT PODE_GATE] outside SDI_2) to recognize drain-ballasted cascaded NMOS.
 - For the Z definition in 1.8V drain-ballasted 2 stages Cascoded NMOS, please follow ESD.24g.
 - The 1.8V drain-ballasted 2 stages NMOS can only be used as primary ESD protection device (1st ESD) and secondary ESD protection device is not allowed.

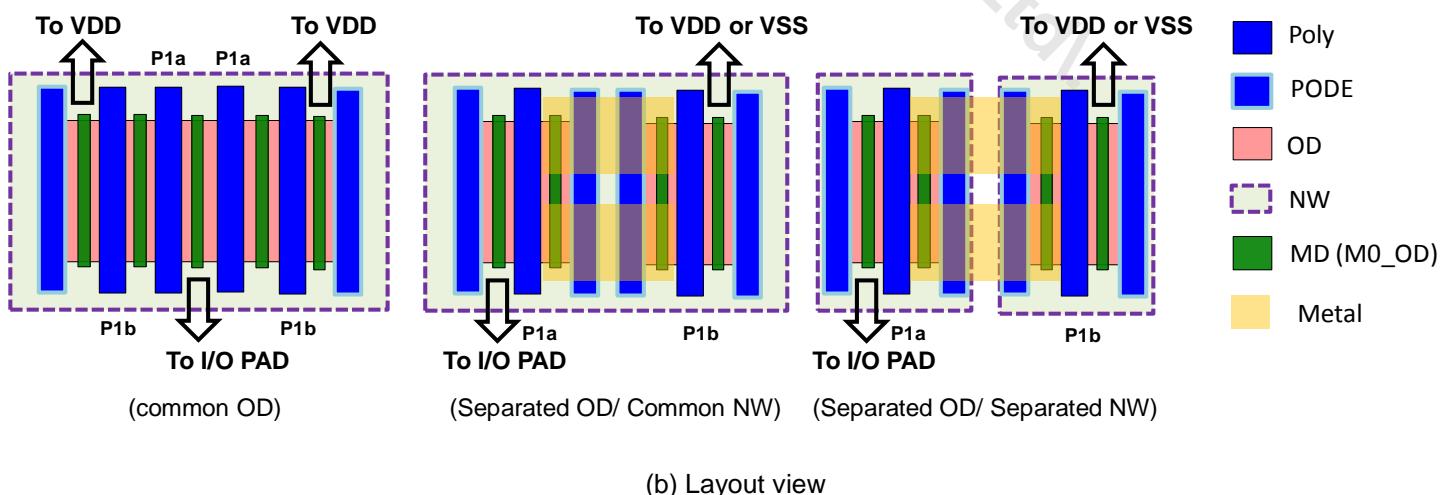
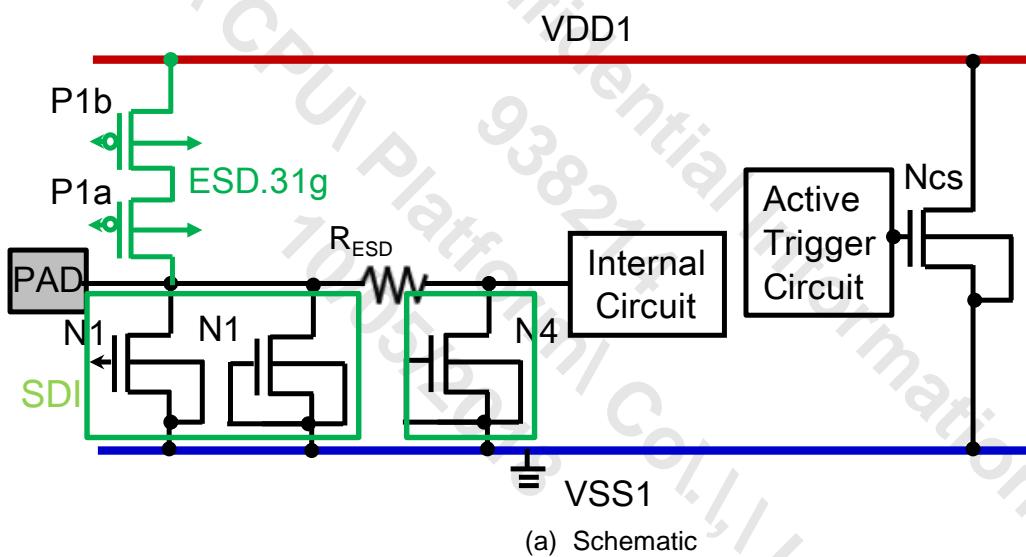
Rule No.	Description	Label	Op.	Rule
ESD.27g	Total finger width of 2-stage cascoded NMOS in same connection of drain connected to IOPAD. NMOS stated above [one side connected to IOPAD, the other side connected to PWSTRAP directly], inside same PWSTRAP enclosed area, should meet total finger width criteria as well. Inside each of PWSTRAP enclosed area, drain of NMOS stated above should be shorted together. This is checked in ESD.36.		\geq	540
ESD.CDM7A.27g	Total finger width of 2-stage cascoded NMOS in same connection of drain connected to IOPAD. NMOS stated above [one side connected to IOPAD, the other side connected to PWSTRAP directly], inside same PWSTRAP enclosed area, should meet total finger width criteria as well. Inside each of PWSTRAP enclosed area, drain of NMOS stated above should be shorted together. This is checked in ESD.36. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		\geq	860
ESD.CDM9A.27g	Total finger width of 2-stage cascoded NMOS in same connection of drain connected to IOPAD. NMOS stated above [one side connected to IOPAD, the other side connected to PWSTRAP directly], inside same PWSTRAP enclosed area, should meet total finger width criteria as well. Inside each of PWSTRAP enclosed area, drain of NMOS stated above should be shorted together. This is checked in ESD.36. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		\geq	1200
ESD.CDM14A.27g	Total finger width of 2-stage cascoded NMOS in same connection of drain connected to IOPAD. NMOS stated above [one side connected to IOPAD, the other side connected to PWSTRAP directly], inside same PWSTRAP enclosed area, should meet total finger width criteria as well. Inside each of PWSTRAP enclosed area, drain of NMOS stated above should be shorted together. This is checked in ESD.36. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		\geq	1820
ESD.29g	Channel length: 1.8V drain-ballasted 2-stage cascoded NMOS (2.5V tolerant I/O). N2 and N3 in Figure 9.2.23.1 and Figure 9.2.23.2.	L	\geq	0.1350
ESD.32	Overlap of SDI_2 on the drain side to the poly gate	Z	$=$	0.0600
ESD.33	NMOS drain side MD to poly spacing (Figure 9.2.23.1 and Figure 9.2.23.2)	X	$=$	0.1600
ESD.34	SR_DPO [INTERACT SDI_2] space to PO in horizontal direction	M	$=$	0.2320
ESD.35g ^U	2-stage cascoded NMOS need to be same OD structure			



9.2.6.5 1.8V Cascoded PMOS for ESD

- This guideline is for enlarging trigger voltage of PMOS and avoid ESD current going through PMOS leading to ESD damage.

Rule No.	Description	Label	Op.	Rule
ESD.31g	<p>As PMOS is connected between IO PAD and VDD/VSS PAD, the PMOS must be cascaded structure. (Figure 9.2.24)</p> <p>The PMOS after resistor will not be flagged by ESD.31g DRC checking.</p> <p>For CDM 5A application with snapback as primary ESD, separated NW is must. Please refer to ESD.CDM.1g</p> <p>This rule is based on limited test structure. For single stage MOS, it is based on gate-grounded design. For cascaded scheme, the test structure is with top-gate floating and bottom-gate grounded. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.</p>			



(For the detail layout constrain on separated OD and separated NW, please refer to ESD.CDM.1g, ESD.CDM.1.1g and ESD.CDM.2g)

Figure 9.2.24 Cascoded PMOS Connection and Layout of ESD.31g

9.2.6.6 Power Clamp Device (Ncs/Pcs)

- DRC deck uses (((N+ ACTIVE or P+ ACTIVE) AND SDI) NOT INTERACT SR_ESD) to recognize Power Clamp
- The Active Power Clamp is required to put between power and ground buses. The Active Power Clamp is consisted of one trigger circuit and one clamp device. The trigger circuit is designed to turn on the clamp device during ESD events and keep the clamp device in off state at normal operation.
- Care should be taken to avoid potential damage risk to the thin gate oxide. An active power clamp (Vtrigger1~0.5V) is needed if there are thin-oxide devices whose gates directly connect to power (for example the NMOS's and PMOS's gates connect to VDD and VSS, respectively). Ex. MOS capacitors.
- The total width is calculated by OD drawing width instead of the physical dimension of FinFET width.

Rule No.	Description	Label	Op.	Rule
ESD.40g	Total finger width of IO Power Clamp (in OD2) in same connection of Power PAD. (Ncs/Pcs in Figure 9.2.25) This rule checks on power PAD only.		≥	2000
ESD.CDM7A.40g	Total finger width of IO Power Clamp (in OD2) in same connection of Power PAD. (Ncs/Pcs in Figure 9.2.25) This rule checks on power PAD only. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		≥	3200
ESD.CDM9A.40g	Total finger width of IO Power Clamp (in OD2) in same connection of Power PAD. (Ncs/Pcs in Figure 9.2.25) This rule checks on power PAD only. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		≥	4500
ESD.CDM14A.40g	Total finger width of IO Power Clamp (in OD2) in same connection of Power PAD. (Ncs/Pcs in Figure 9.2.25) This rule checks on power PAD only. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		≥	7500
ESD.40.1g	Total finger width of core Power Clamp in same connection of Power PAD. (Ncs/Pcs in Figure 9.2.25) This rule checks on power PAD only.		≥	2200
ESD.CDM7A.40.1g	Total finger width of core Power Clamp in same connection of Power PAD. (Ncs/Pcs in Figure 9.2.25) This rule checks on power PAD only. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		≥	3400
ESD.CDM9A.40.1g	Total finger width of core Power Clamp in same connection of Power PAD. (Ncs/Pcs in Figure 9.2.25) This rule checks on power PAD only. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		≥	4900
ESD.CDM14A.40.1g	Total finger width of core Power Clamp in same connection of Power PAD. (Ncs/Pcs in Figure 9.2.25) This rule checks on power PAD only. (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		≥	8400
ESD.40.2g ^U	Total finger width of 2.5V/3.3V Power Clamp in same connection of Power PAD. The suggested 2.5V and 3.3V Power Clamps are formed by cascaded 1.8V NMOS. (Ncs in Figure 9.2.25)		≥	2200
ESD.CDM7A.40.2g ^U	Total finger width of 2.5V/3.3V Power Clamp in same connection of Power PAD. The suggested 2.5V and 3.3V Power Clamps are formed by cascaded 1.8V NMOS. (Ncs in Figure 9.2.25) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		≥	3400

ESD.CDM9A.40.2g ^U	Total finger width of 2.5V/3.3V Power Clamp in same connection of Power PAD. The suggested 2.5V and 3.3V Power Clamps are formed by cascaded 1.8V NMOS. (Ncs in Figure 9.2.25) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		\geq	4900
ESD.CDM14A.40.2g ^U	Total finger width of 2.5V/3.3V Power Clamp in same connection of Power PAD. The suggested 2.5V and 3.3V Power Clamps are formed by cascaded 1.8V NMOS. (Ncs in Figure 9.2.25) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		\geq	8400
ESD.40.3g	Total width of the unit cell power clamp (DRC will use gate connection to decide the unit cell power clamp) (Figure 9.2.26)		\geq	400
ESD.CDM7A.40.3g	Total width of the unit cell power clamp (DRC will use gate connection to decide the unit cell power clamp) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on) (Figure 9.2.26)		\geq	1200
ESD.CDM9A.40.3g	Total width of the unit cell power clamp (DRC will use gate connection to decide the unit cell power clamp) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on) (Figure 9.2.26)		\geq	1500
ESD.CDM14A.40.3g	Total width of the unit cell power clamp (DRC will use gate connection to decide the unit cell power clamp) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on) (Figure 9.2.26)		\geq	2000
ESD.40.3.1g ^U	Total width of the unit cell power clamp (unit cell: group of devices close to each other)		\geq	400
ESD.CDM7A.40.3.1g ^U	Total width of the unit cell power clamp (unit cell: group of devices close to each other) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		\geq	1200
ESD.CDM9A.40.3.1g ^U	Total width of the unit cell power clamp (unit cell: group of devices close to each other) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		\geq	1500
ESD.CDM14A.40.3.1g ^U	Total width of the unit cell power clamp (unit cell: group of devices close to each other) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		\geq	2000
ESD.42g	Channel length: IO Power Clamp (in OD2)	L	=	0.1350~0.2400
ESD.42.1g ^U	Channel length: 2.5V/3.3V Power Clamp (cascoded 1.8V NMOS in OD2)	L	=	0.1500~0.2400
ESD.42.2g	Channel length: core Power Clamp (not in OD2)	L	=	0.0720~0.1300
ESD.43g ^U	Each set of VDD and VSS must have its own power clamp cells and active Power Clamp is required (Figure 9.2.25)			
ESD.43.1g ^U	The single stage power clamp (between VDD and VSS) needs to be covered by SDI layer.			

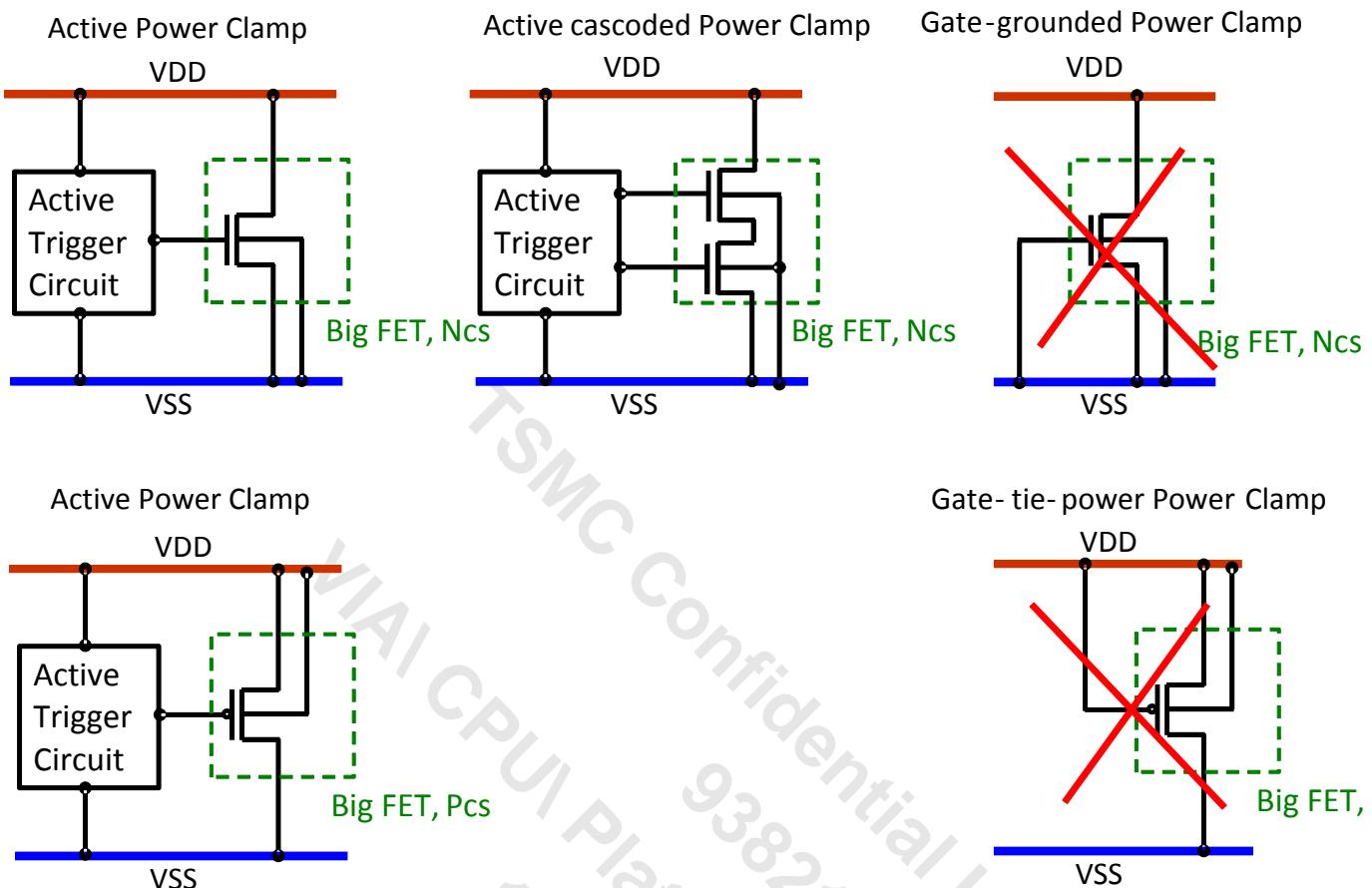


Figure 9.2.25 The schematic of the Active Power Clamp

The total unit finger width is calculated by the ESD MOS in the same gate connection.

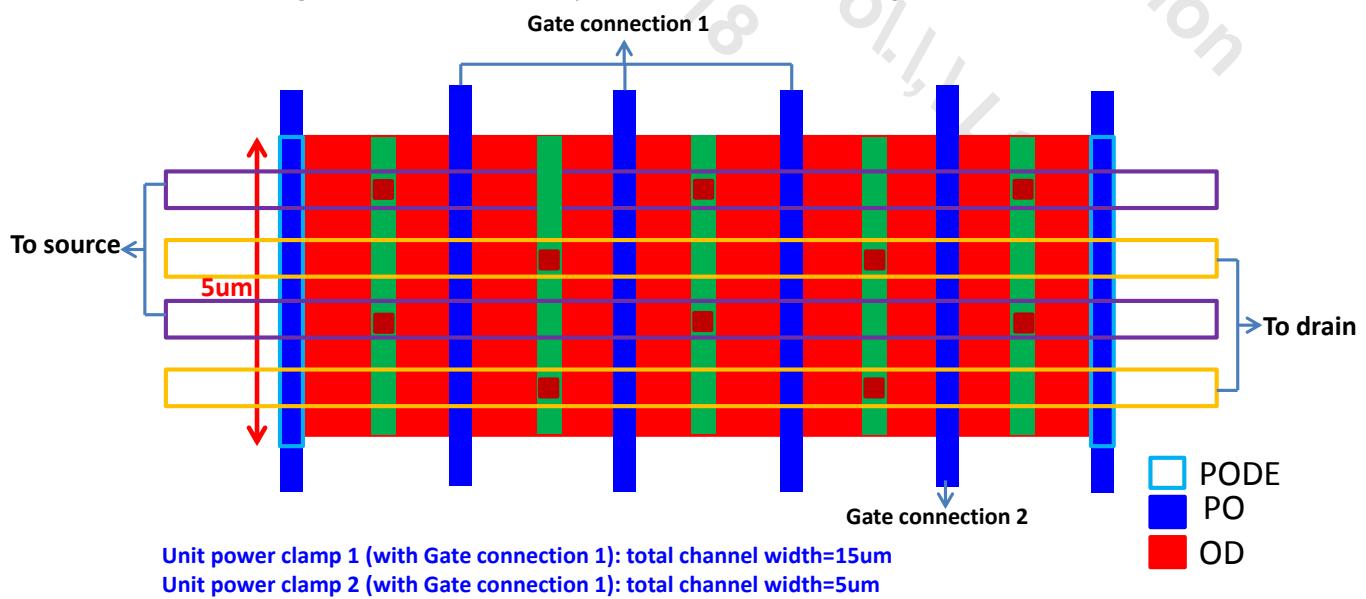


Figure 9.2.26 The schematic and illustration of the unit power in ESD.40.3g

9.2.6.7 Diode for ESD

- Provided that dual-diode based ESD protection is used and associated guidelines are met, the DRC violations of MOS/snapback base ESD protection approach can be waived based on previous silicon results and experiences.
- As the customer choose to adopt tsmc dual-diode based ESD protection scheme, it is suggested to use HIA diode (HIA_dummy, 168;0) as their ESD diodes. The HIA diode provide diode forward vfTLP behavior fitting model in the SPICE model and related ESD design rules.
- The poor metal routing will result in the current-crowding effect and impact on the vfTLP behavior. The vfTLP spice model of HIA diode extraction is from specific metal routing layout style, thus the current-crowding effect is not included in it. Besides, the test patterns of vfTLP model are also limited so it is hard to cover all layout style. Therefore, to keep more ESD margin, please follow tsmc all HIA diode related rules to obtain optimum ESD capability.

9.2.6.7.1 Dual-Diode I/O Protection

Diodes can be used for the logic, low capacitance or high speed/frequency ESD protection. For diode-base ESD protection scheme, it should work together with the low-trigger power clamps, such as RC-gate driven clamp.

Figure 9.2.26 shows the common dual-diode protection scheme. One diode is for pull-up path to the VDD and the other is for pull-down path to the VSS. There are four current discharge paths between the PAD, VDD and VSS. The brief descriptions are as follows:

1. For a positive pulse from PAD respect to VDD, the current flows through the pull-up diode to VDD.
2. For a negative pulse from PAD respect to VDD, the current first enters the VDD pin, goes through the power clamp, and then flows through the pull-down diode,
3. For a positive pulse from PAD respect to VSS, the current goes through the pull-up diode, along the supply metal bus, through the power clamp and out the VSS.
4. For a negative pulse from PAD respect to VSS, the current flows through the pull-down diode and out the PAD.

Please note that excellent ESD performance is achieved when the discharge paths are confined to the design paths as mentioned above. It depends on the low turn-on resistance of the diode, wiring and power clamp devices. The designer should minimize the I-R drop effect as much as possible. The resistance of metal bus between the PAD and power clamp should be less than 1 ohm. Also, both the ESD level and parasitic capacitance are directly proportional to the diode's perimeter. Hence, the designer should consider the parasitic capacitance of the diodes on the I/O PAD and have to balance the ESD and circuit's performance.

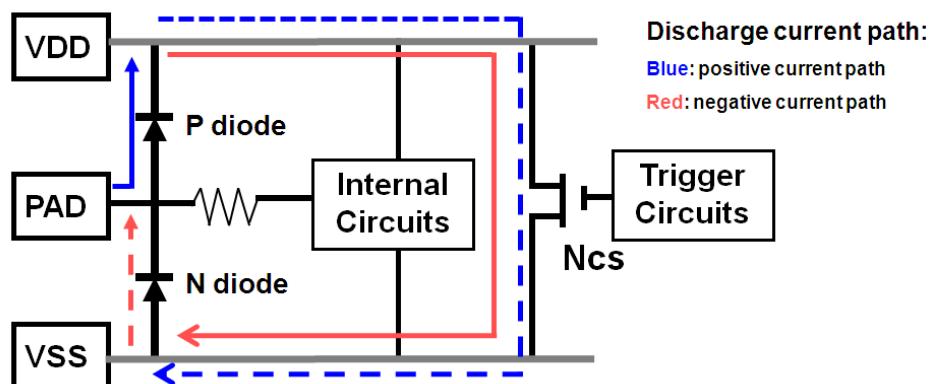


Figure 9.2.26 The schematic diagram for diode-base protection

9.2.6.7.2 Layout Guidelines for HIA_DIO

- HIA_DIO can be used for logic or high speed circuits ESD protection. A layout example is shown in Figure 9.2.28.
- The naming of HIA comes from high current application purposes (High Amp). HIA_DIO provides diode forward vTLP behavior fitting model in the SPICE model, and there is no process difference between HIA_DIO and regular diode.
- HIA_PWSTRAP: PWSTRAP INTERACT (SIZE (HIA_DUMMY AND N+ ACTIVE) BY 0.562 μm)
- HIA_NWSTRAP: NWSTRAP INTERACT (SIZE (HIA_DUMMY AND P+ ACTIVE) BY 0.562 μm)

9.2.6.7.2.1 HIA_DIO Layout Guidelines

9.2.6.7.2.1.1 HIA_DUMMY Layer (CAD layer: 168;0)

- DRC deck uses (N+ ACTIVE AND HIA_DUMMY NOT NW) to recognize N-HIA diode's cathode.
- DRC deck uses (P+ ACTIVE AND HIA_DUMMY AND NW) to recognize P-HIA diode's anode.
- Draw HIA_DUMMY (CAD layer: 168;0) to fully cover diode's anode OD regions that are connected to I/O pads, including the anode, instead of cathode. (Figure 9.2.27) N+ Active and P+ Active inside HIA_DUMMY must be a rectangle orthogonal to grid.
- HIA_DUMMY is a tape-out layer. All Poly & PODE (poly on OD edge) within HIA_dummy and their associated ODs are required to be connected by MP. (Figure 9.2.27) Floating poly/PODE within HIA_dummy is not allowed.

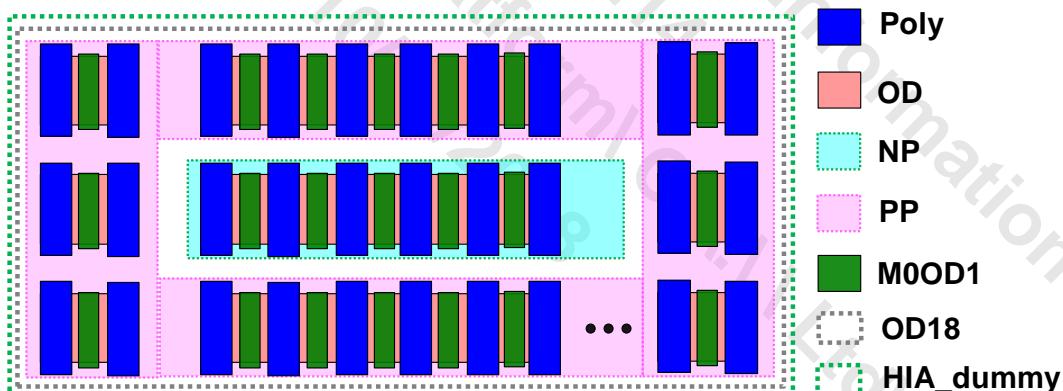


Figure 9.2.27 HIA_DUMMY layout example

9.2.6.7.2.1.2 High current diodes layout guidelines (STI-bounded junction diode)

Rule No.	Description	Label	Op.	Rule
HIA.1g	Width of N+ Active (N-HIA diode's cathode) and P+ Active (P-HIA diode's anode) inside HIA_DUMMY and connect to IO PAD. (Except LC_DMY). (Figure 9.2.28 and 9.2.28.1)	A	=	0.4580~0.5180
HIA.1.1g	Width of {PWSTRAP/NWSTRAP INTERACT ((HIA_DUMMY AND (N+/P+ ACTIVE connected to IO PAD)) SIZING up 0.562 μm in vertical direction)}	A1	=	0.3080~0.5180
HIA.2	Space of GATE [INSIDE HIA_DUMMY] (Figure 9.2.28 and 9.2.28.1)	B	=	0.0940
HIA.3g	Total perimeter of N+ or P+ Active inside HIA_DUMMY in same connection of IO PAD (Figure 9.2.28 and 9.2.28.1), the perimeter counts the drawn anode junction parameter region ex. The drawing OD perimeter dimension of active inside HIA_DUMMY= $(A+E)^*2^*N$ (Except LC_DMY)		\geq	180
HIA.CDM7A.3g	Total perimeter of N+ or P+ Active inside HIA_DUMMY in same connection of IO PAD (Figure 9.2.28 and 9.2.28.1), the perimeter counts the drawn anode junction parameter region ex. The drawing OD perimeter dimension of active inside HIA_DUMMY= $(A+E)^*2^*N$ (Except LC_DMY) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		\geq	300
HIA.CDM9A.3g	Total perimeter of N+ or P+ Active inside HIA_DUMMY in same connection of IO PAD (Figure 9.2.28 and 9.2.28.1), the perimeter counts the drawn anode junction parameter region ex. The drawing OD perimeter dimension of active inside HIA_DUMMY= $(A+E)^*2^*N$ (Except LC_DMY) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		\geq	400
HIA.CDM14A.3g	Total perimeter of N+ or P+ Active inside HIA_DUMMY in same connection of IO PAD (Figure 9.2.28 and 9.2.28.1), the perimeter counts the drawn anode junction parameter region ex. The drawing OD perimeter dimension of active inside HIA_DUMMY= $(A+E)^*2^*N$ (Except LC_DMY) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		\geq	600
HIA.3.1g	Total OD area of both N+ or P+ Active inside HIA_DUMMY in the same connection of IO PAD (Except LC_DMY) (Figure 9.2.28 and 9.2.28.1) (μm^2)		\geq	36
HIA.CDM7A.3.1g	Total OD area of both N+ or P+ Active inside HIA_DUMMY in the same connection of IO PAD (Except LC_DMY) (Figure 9.2.28 and 9.2.28.1) (μm^2) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		\geq	60
HIA.CDM9A.3.1g	Total OD area of both N+ or P+ Active inside HIA_DUMMY in the same connection of IO PAD (Except LC_DMY) (Figure 9.2.28 and 9.2.28.1) (μm^2) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		\geq	80
HIA.CDM14A.3.1g	Total OD area of both N+ or P+ Active inside HIA_DUMMY in the same connection of IO PAD (Except LC_DMY) (Figure 9.2.28 and 9.2.28.1) (μm^2) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		\geq	120
HIA.3.2g	Minimum length of {PWSTRAP/NWSTRAP INTERACT ((HIA_DUMMY AND N+/P+ ACTIVE) SIZING up 0.562 μm in vertical direction)} must be larger than or equal to the maximum length of nearby (N+/P+ Active INSIDE HIA_DUMMY)			

Rule No.	Description	Label	Op.	Rule
HIA.4	The OD spacing between N+/P+ Active (length \geq 1 μ m, INSIDE HIA_DUMMY, connect to IO PAD) and nearby {HIA_PWSTRAP/HIA_NWSTRAP}. (Except LC_DMY) (Figure 9.2.28 and 9.2.28.1)	C	\leq	0.5020
HIA.5	The length of poly gate	D	=	0.0860
HIA.6	HIA diode {{HIA_DUMMY AND OD} INTERACT Active} must be fully covered by OD2 (OD_18).			
HIA.7	{OD CUT HIA_DUMMY} is not allowed			
HIA.8	HIA diode cannot be used for > 3.63V (3.3V+10%) application.			
HIA.9	HIA_DUMMY enclosure of OD.	EN1	\geq	0.0430
HIA.9.1	HIA_DUMMY enclosure of ALL_PO. ALL_PO CUT HIA_DUMMY is not allowed.	EN2	\geq	0.0350
HIA.9.2	Maximum enclosure of (OD inside HIA_DUMMY) by HIA_DUMMY	EN1	\leq	0.2810
HIA.9.3	Maximum enclosure of (ALL_PO inside HIA_DUMMY) by HIA_DUMMY	EN2	\leq	0.2200
HIA.11g	Length of N+ Active (N-HIA diode's cathode) and P+ Active (P-HIA diode's anode) inside HIA_DUMMY and connect to IO PAD. (Figure 9.2.28 and 9.2.28.1)	E	\leq	30
HIA.12g	Width (A) and length (E) of each N+ Active (N-HIA diode's cathode) and each P+ Active (P-HIA diode's anode) inside HIA_DUMMY must be the same. (Figure 9.2.28 and 9.2.28.1)			
HIA.13g	{PO NOT CPO} [INTERACT ACTIVE] must connect to source/drain ACTIVE [INSIDE HIA_DUMMY]			
HIA.14	Space of HIA_DUMMY	S1	\geq	0.1920
HIA.15	HIA_DUMMY [INTERACT ACTIVE] space to ACTIVE ({ACTIVE CUT HIA_DUMMY} is not allowed)	S2	\geq	0.0430
HIA.16	HIA_DUMMY overlap VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N or VTUL_P is not allowed.			
HIA.17	All ACTIVE OD inside same HIA_DUMMY should be short together.			
HIA.18g	Number of {N+/P+ Active INTERACT HIA_DUMMY} inside each of {HIA_PWSTRAP SIZING up/down 0.281 μ m and HIA_NWSTRAP SIZING up/down 0.281 μ m} enclosed area (Except LC_DMY)		=	1

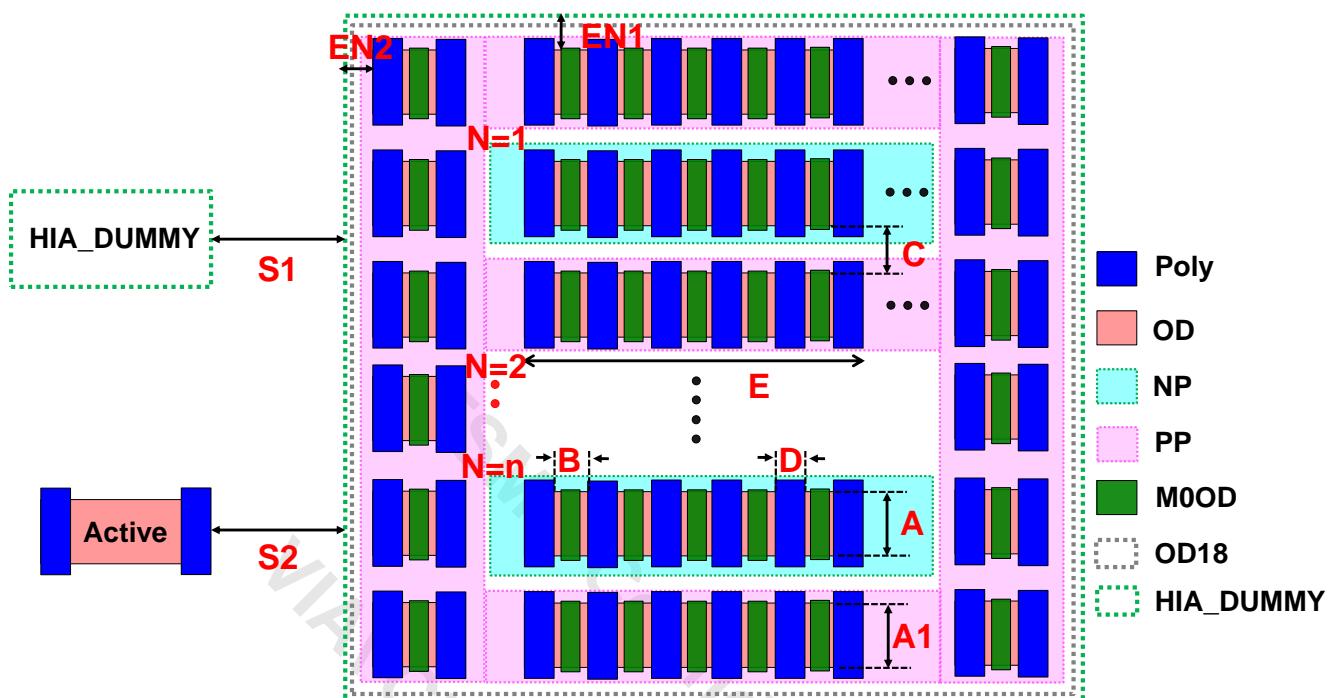


Figure 9.2.28 HIA_DIO layout (N-HIA diode)

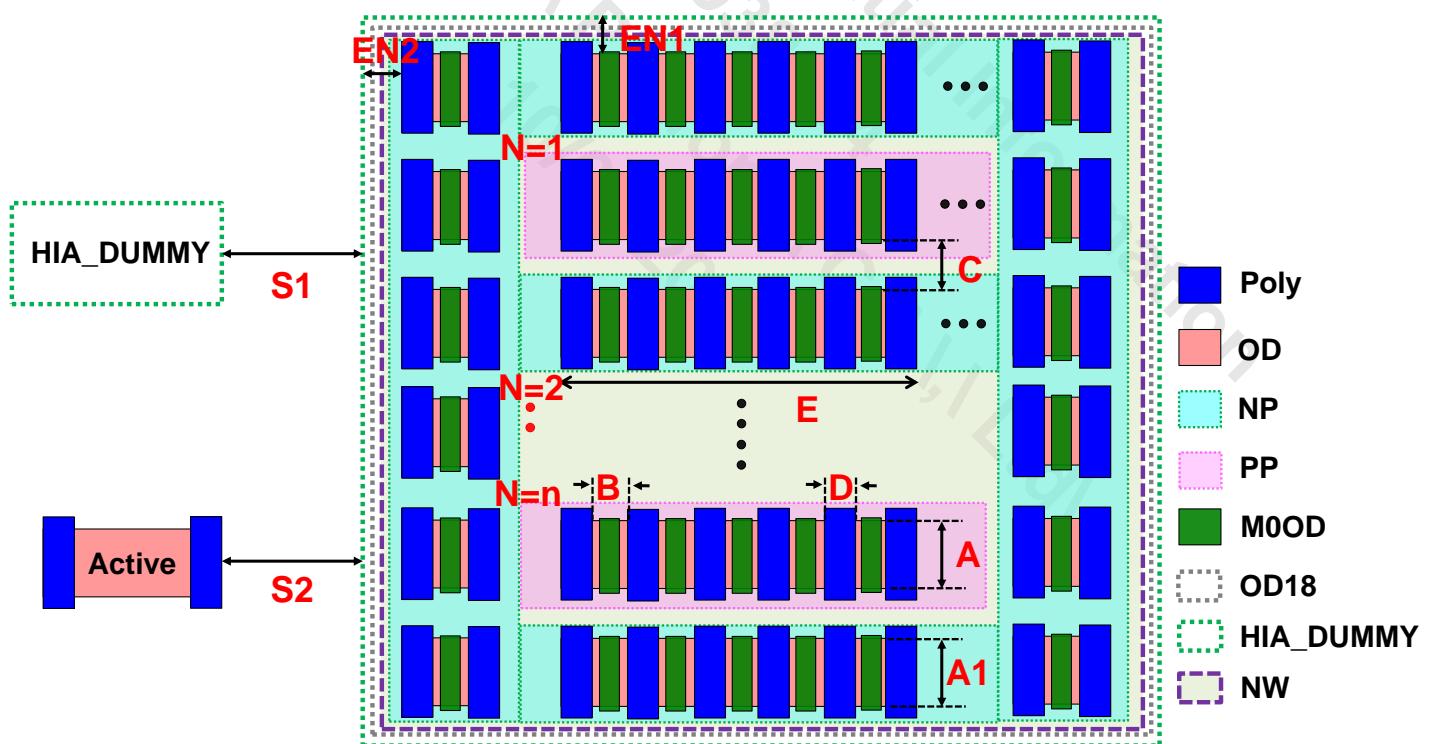


Figure 9.2.28.1 HIA_DIO layout (P-HIA diode)

9.2.6.8 Low Capacitance ESD Devices

9.2.6.8.1 Low Capacitance HIA_DIO

The low capacitance HIA_DIO (HIA diode) shares the same spice model with regular HIA diode, and, the major differences are that low-C diodes allow smaller total perimeter (ESD.LC.3g) and has rule tighten on bus resistance (ESD.LCP2P.2g^U).

9.2.6.8.1.1 Low_C Layer (CAD layer: 168;1)

- DRC deck uses (LC_DMY AND N+ ACTIVE AND HIA_DUMMY NOT NW) to recognize low capacitance N-HIA diode's cathode.
- DRC deck uses (LC_DMY AND P+ ACTIVE AND HIA_DUMMY AND NW) to recognize low capacitance P-HIA diode's anode.
- Draw LC_DMY (CAD layer:168;1) to fully cover diode's anode OD regions that are connected to I/O pads, including the anode, instead of cathode. (Figure 9.2.27) N+ Active and P+ Active inside HIA_DUMMY must be a rectangle orthogonal to grid.

9.2.6.8.1.2 Low Capacitance HIA_DIO Layout Guidelines

- HIA_DIO can be used for low capacitance oriented ESD protection with certain backend metal routing optimization. Besides the special metal routing implementation, please follow all the layout guidelines. The suggested backend metal routing approaches are explained as following. Several ESD rules have to be tighten due to the implementation of low capacitance HIA_DIO.
- Keep distances between metal lines with different potentials as far as possible.
- Minimize metal direction changes between different layers in order to avoid overlap of metal layers with different potentials.
- When metal direction switching between different layers is necessary, Skip at least one layer between horizontal and vertical metal layers.(Figure 9.2.31)

Rule No.	Description	Label	Op.	Rule
ESD.LC.1g	Width of N+ Active (N-HIA diode's cathode) and P+ Active (P-HIA diode's anode) inside LC_DMY and connect to IO PAD. (Figure 9.2.30.1 and 9.2.30.2)	A	=	0.2180
ESD.LC.2g	LC_DMY must be fully covered by HIA_DUMMY			
ESD.LC.3g	Total perimeter of N+ or P+ Active inside LC_DMY in same connection of IO PAD (Figure 9.2.30.1 and 9.2.30.2). The perimeter counts the effective anode junction region inside HIA_DUMMY. DRC check {total perimeter - (total length /2)}		\geq	100
ESD.CDM7A.LC.3g	Total perimeter of N+ or P+ Active inside LC_DMY in same connection of IO PAD (Figure 9.2.30.1 and 9.2.30.2). The perimeter counts the effective anode junction region inside HIA_DUMMY. DRC check {total perimeter - (total length /2)} (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		\geq	220
ESD.CDM9A.LC.3g	Total perimeter of N+ or P+ Active inside LC_DMY in same connection of IO PAD (Figure 9.2.30.1 and 9.2.30.2). The perimeter counts the effective anode junction region inside HIA_DUMMY. DRC check {total perimeter - (total length /2)} (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		\geq	330

Rule No.	Description	Label	Op.	Rule
ESD.CDM14A.LC.3g	Total perimeter of N+ or P+ Active inside LC_DMY in same connection of IO PAD (Figure 9.2.30.1 and 9.2.30.2). The perimeter counts the effective anode junction region inside HIA_DUMMY. DRC check {total perimeter - (total length /2)} (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		\geq	440
ESD.LC.3.1g	Total OD area of both N+ or P+ Active inside LC_DMY in the same connection of IO PAD. (Figure 9.2.30.1 and 9.2.30.2). (μm^2)		\geq	18
ESD.CDM7A.LC.3.1g	Total OD area of both N+ or P+ Active inside LC_DMY in the same connection of IO PAD. (Figure 9.2.30.1 and 9.2.30.2). (μm^2) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM7A" is switched on)		\geq	30
ESD.CDM9A.LC.3.1g	Total OD area of both N+ or P+ Active inside LC_DMY in the same connection of IO PAD. (Figure 9.2.30.1 and 9.2.30.2). (μm^2) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM9A" is switched on)		\geq	45
ESD.CDM14A.LC.3.1g	Total OD area of both N+ or P+ Active inside LC_DMY in the same connection of IO PAD. (Figure 9.2.30.1 and 9.2.30.2). (μm^2) (This rule is enabled when DRC option "GUIDELINE_ESD_CDM14A" is switched on)		\geq	60
ESD.LC.4g	The OD spacing between {N+/P+ Active [length \geq 1 μm , INSIDE LC_DMY, connected to IO PAD] SIZING up/down 0.071um} and nearby PWSTRAP/NWSTRAP. (Figure 9.2.30.1 and 9.2.30.2)	C	=	0.3820~0.5620
ESD.LC.4.1g	The OD spacing between {N+/P+ Active INTERACT LC_DMY} inside each of {HIA_PWSTRAP SIZING up/down 0.281um and HIA_NWSTRAP SIZING up/down 0.281um} enclosed area. (Figure 9.2.30.1 and 9.2.30.2)	F	=	0.1420
ESD.LCP2P.1g ^U	Metal Bus resistance of IOPAD to ESD dual diode inside LC_DMY R1 & R3 \leq 0.1 ohm. (Fig.9.2.32.2) No needed to take "R0" into account.		\leq	Table 9.2.6.8.1
ESD.LCP2P.2g ^U	Metal Bus resistance of ESD dual diode inside LC_DMY to power clamp R1'+R2'+R4 \leq 0.1 ohm, R3'+R5'+R6 \leq 0.1 ohm. (Fig.9.2.32.2)		\leq	Table 9.2.6.8.1
ESD.LC.5g ^U	Cascoded power clamp is not allowed as the primary protection is dual diode inside LC_DMY			
ESD.LC.10g	Number of {N+/P+ Active INTERACT LC_DMY} inside each of {HIA_PWSTRAP SIZING up/down 0.281 μm and HIA_NWSTRAP SIZING up/down 0.281 μm } enclosed area. (Figure 9.2.30.1 and 9.2.30.2)		=	2

Table 9.2.6.8.1 ESD Rbus requirement for LC signal pin

	CDM 5A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)	CDM 14A (FWHM < 1ns)
ESD.LCP2P.1g ^U (Ω)	0.1	0.07	0.05	0.03
ESD.LCP2P.2g ^U (Ω)	0.1	0.1	0.1	0.03

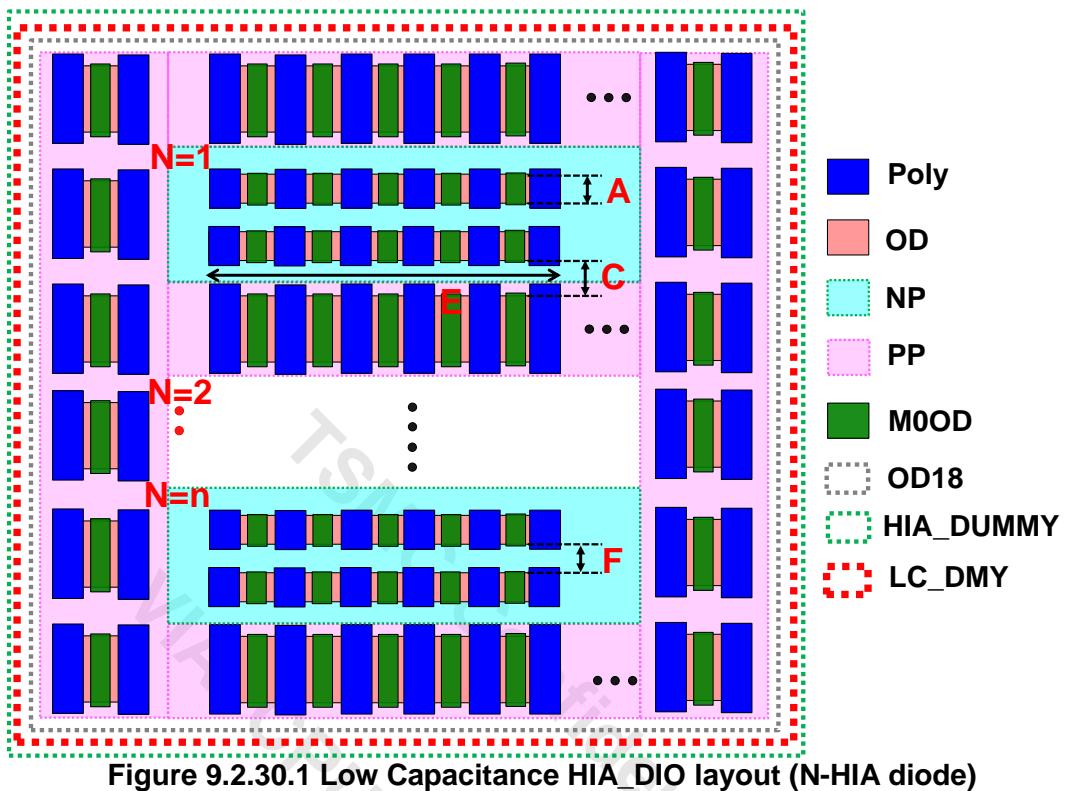


Figure 9.2.30.1 Low Capacitance HIA_DIO layout (N-HIA diode)

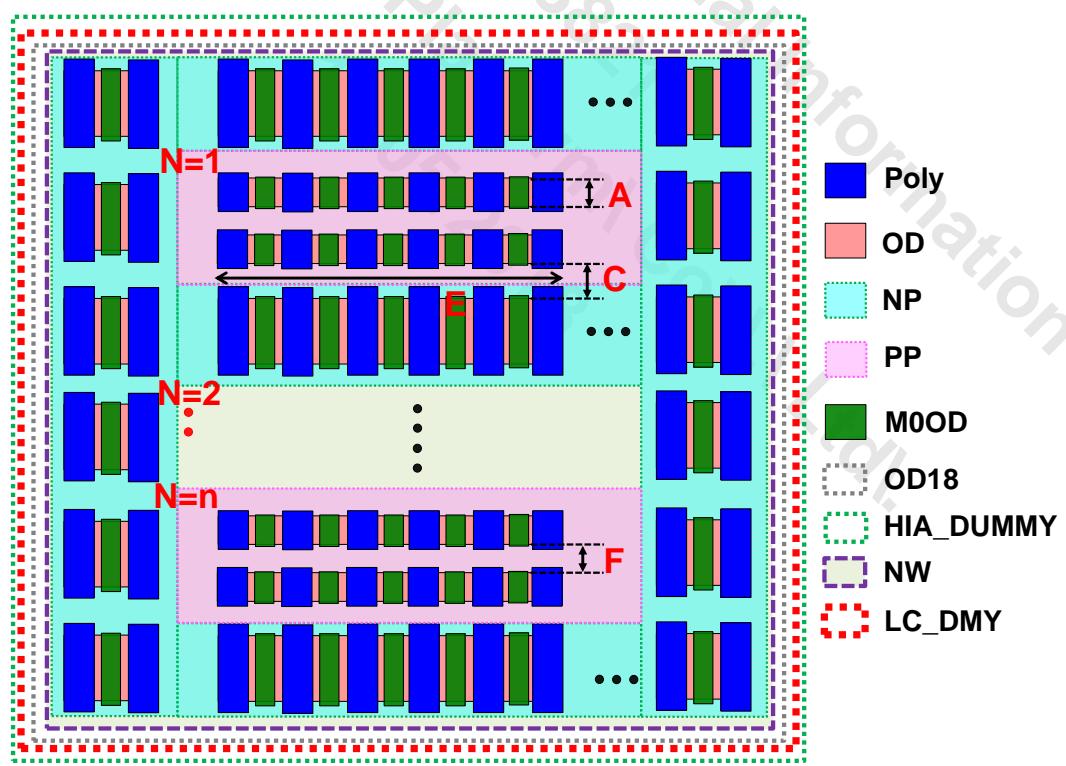


Figure 9.2.30.2 Low Capacitance HIA_DIO layout (P-HIA diode)

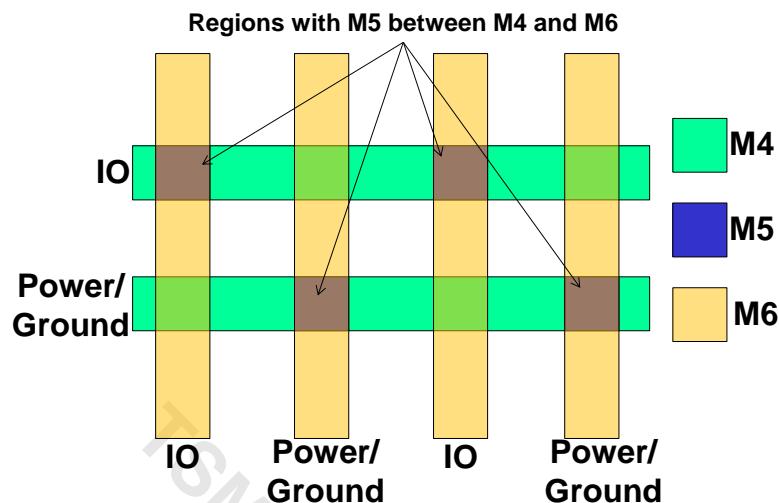


Figure 9.2.31 Example of skip one metal layer between horizontal and vertical metal layers.

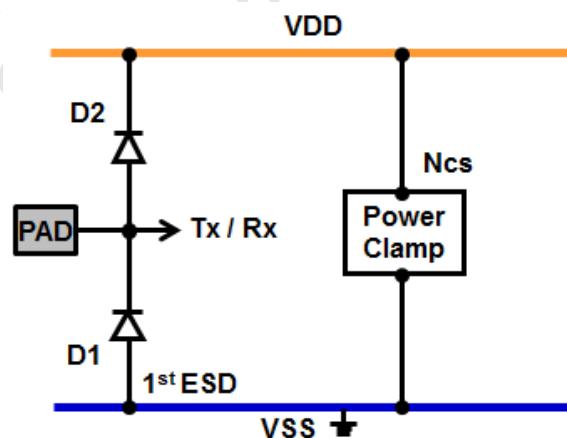


Figure 9.2.32.1 Primary ESD Network Scheme

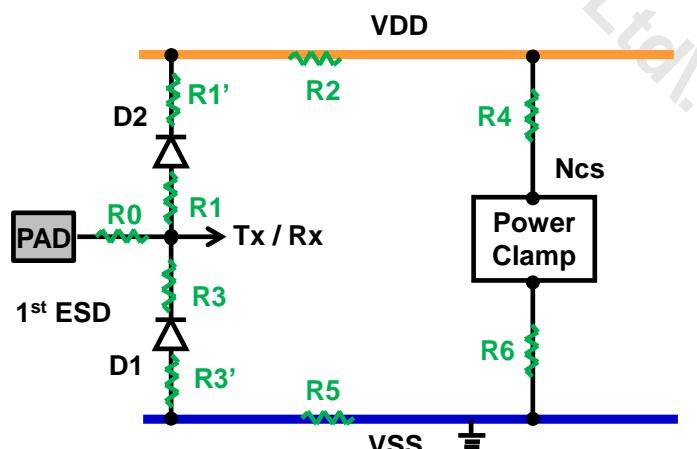


Figure 9.2.32.2 Primary ESD Rbus Network Scheme

9.2.6.9 ESD Device Special Layer Summary

Device	SPICE Name	Special Layer				
		HIA_DUMMY	SR_ESD	SDI	SDI_2	LC_DMY
Drain-ballasted NMOS (1.8V)	nch_hia18_mac	0	1	1	1	0
Drain-ballasted Cascoded NMOS (1.8V)	nch_hia18_mac+nch_18_mac	0	1	1	1	0
2.5V/3.3V ESD Power Clamp NMOS (cascoded 1.8V NMOS)	nch_18_mac	0	0	1	0	0
1.8V ESD Power Clamp NMOS	nch_18_mac	0	0	1	0	0
1.8V ESD Power Clamp PMOS	pch_18_mac	0	0	1	0	0
Core ESD Power Clamp NMOS	nch_svt_mac	0	0	1	0	0
Core ESD Power Clamp PMOS	pch_svt_mac	0	0	1	0	0
N-HIA Diode	ndio_hia18_mac	1	0	0	0	*
P-HIA Diode	pdio_hia18_mac	1	0	0	0	*
"1" Required, "0" Not allowed, "*" Don't Care						

The CAD layer and description for ESD Special Layers:

Special Layer Name	TSMC Default CAD Layer	Description	Associated With
ESDWDMY	255;110	To waive specific ESD rules	ESD guidelines
SDI	122;0	It is required to cover all ESD MOS OD regions that are connected to the pads	ESD guidelines
SDI_2	122;2	IO ESD area dummy layer. For drain-ballasted NMOS	ESD guidelines
SR_ESD	121;0	The layer is required for drain-ballasted NMOS	OD and PO layout rules
HIA_DUMMY	168;0	It is required to cover HIA_diode's anode and cathode regions	HIA diodes layout rules
LC_DMY	168;1	Dummy Layer for low capacitance rules	ESD guidelines
VDDDMY	255;4	Dummy Layer for Power(Vdd) PAD	ESD/LUP guidelines
VSSDMY	255;5	Dummy Layer for Ground(Vss) PAD	ESD/LUP guidelines
IODMY	255;31	Dummy Layer for IO PAD	ESD/LUP guidelines

9.2.7 CDM Protection for Cross Domain Interface

CDM is an increasingly important issue for modern technology integrated circuits as the gate oxide thickness keeps on shrinking and the number of power domains continues increasing. With respect to the CDM protection, the cross-domain interface is the most crucial situation as compared with the I/O input gate (defined as ESD.9g in DRM), the gate directly connected to power/ground, and the long signal path without parasitic junction diode. It is because that the fatal CDM charges are mostly accumulated at the power/ground metal buses and easily damage the gate oxide at the interface when the discharge current path crosses the different power domains.

To prevent this kind of CDM damage for the complex power domains, the protection scheme is proposed as figure 9.2.33.2 shown. The protection network consists of a resistor, a 2nd ESD NMOS and active power clamp cells. Basically, the CDM protection devices have to be placed as close to the receiver gates as possible, and share the same power/ground and well of the receiver cell. A global active clamp cell should be placed near the cross-domain interface to help conducting the CDM currents. Additionally, the resistance of power bus between the global active power clamp cells is recommended to be equal or smaller than 1Ω. The turn-on resistance of “current conducting element” should be as small as possible to minimize the voltage drop during CDM zapping.

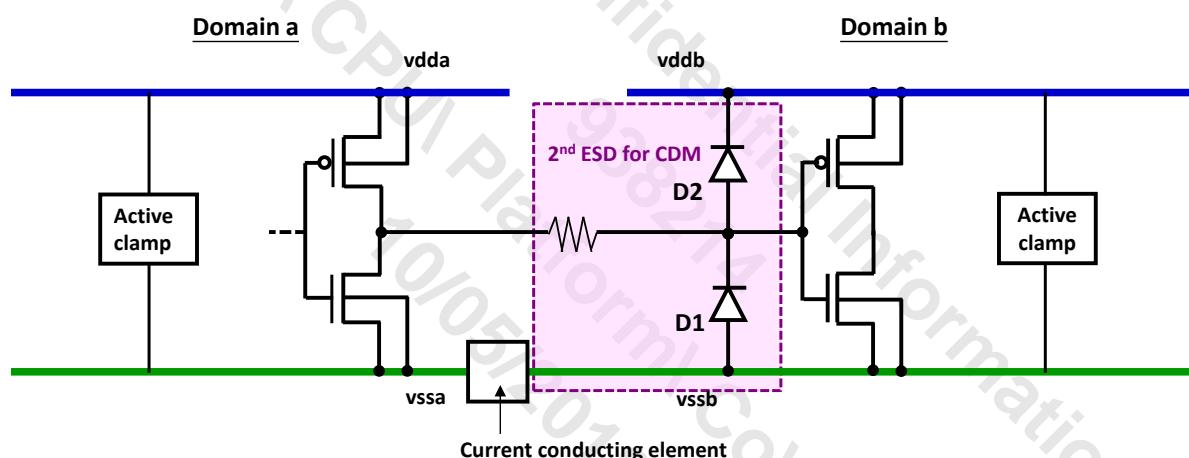


Figure 9.2.33.2 The diode-based cross-domain CDM ESD protection scheme

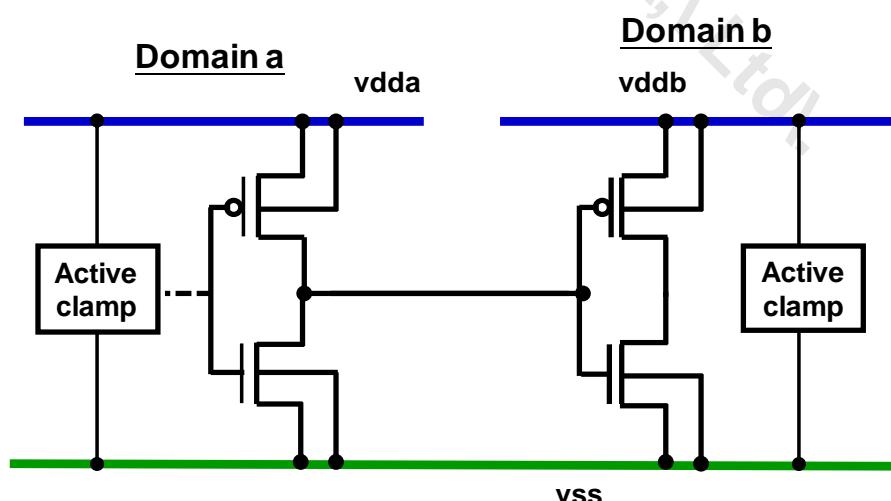


Figure 9.2.33.3 Common-grounded cross-domain CDM ESD protection scheme

9.2.7.1 Interface CDM MOS Layout Guidelines

Rule No.	Description	Label	Op.	Rule
ESD.45.0g ^U	1. For cross domain with separated grounds (Fig. 9.2.33.2), diode based secondary protection with interface resistor is required at interface. (D1/D2 in Figure 9.2.33.2). 2. If the receiver is I/O device, the secondary protection is not required. 3. As the cross domain with on-rule power clamp added between vdda and vssb, the secondary protection is not required.			
ESD.45.0.1g ^U	Single stage N/PMOS in series under cross domain scenario is not allowed. As cross domain with on-rule power clamp, this rule can be waived. (Fig. 9.2.33.4)			
ESD.45.0.2g ^U	Cascoded (2-stage) N/PMOS under cross domain scenario is not allowed. As cross domain with on-rule power clamp, this rule can be waived. (Fig. 9.2.33.5)			
ESD.45.1g ^U	Total perimeter of cross-domain diode based secondary protection. (D1/D2 in Figure 9.2.33.2)		\geq	4
ESD.47g ^U	Recommended interface voltage clamping resistor resistance for cross-domain with separated ground (resistor in Figure 9.2.33.1~2)		\geq	200

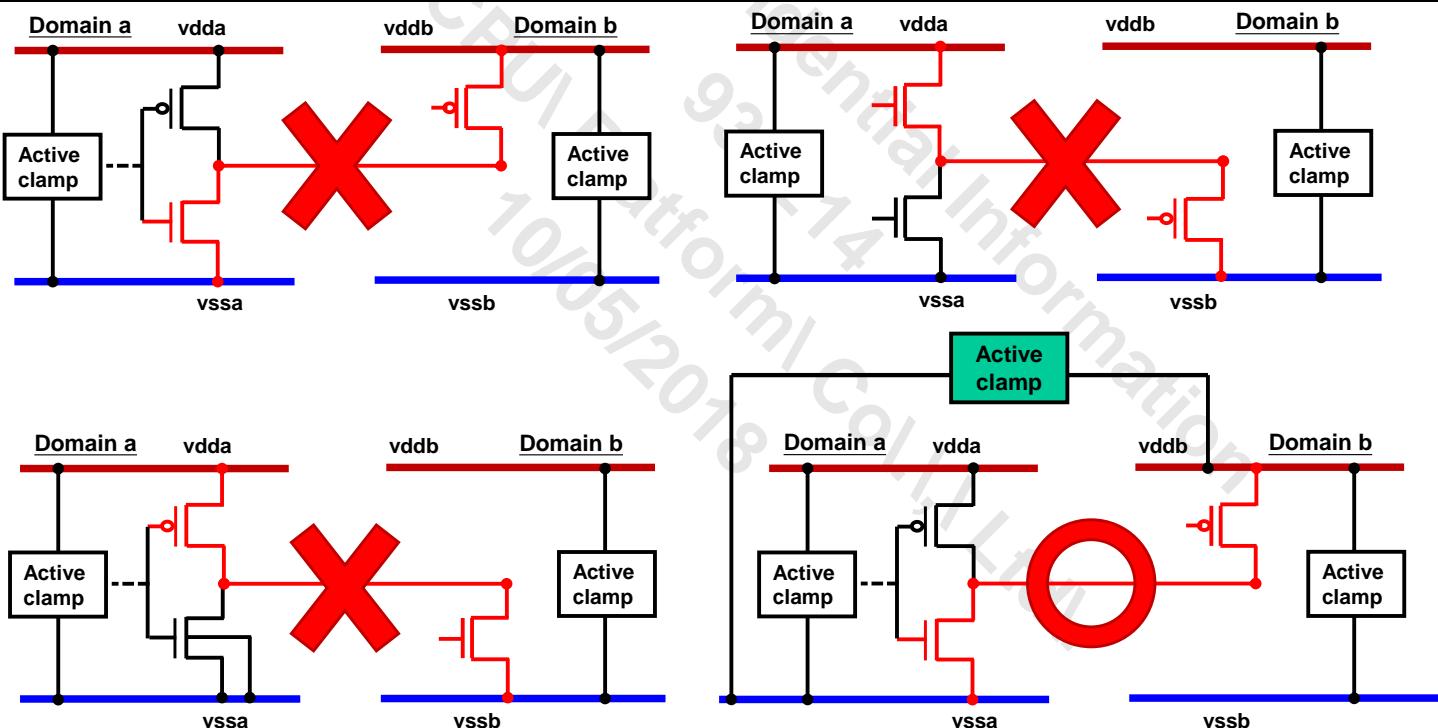


Figure 9.2.33.4 Single stage N/PMOS in series under cross domain scenario is not allowed.

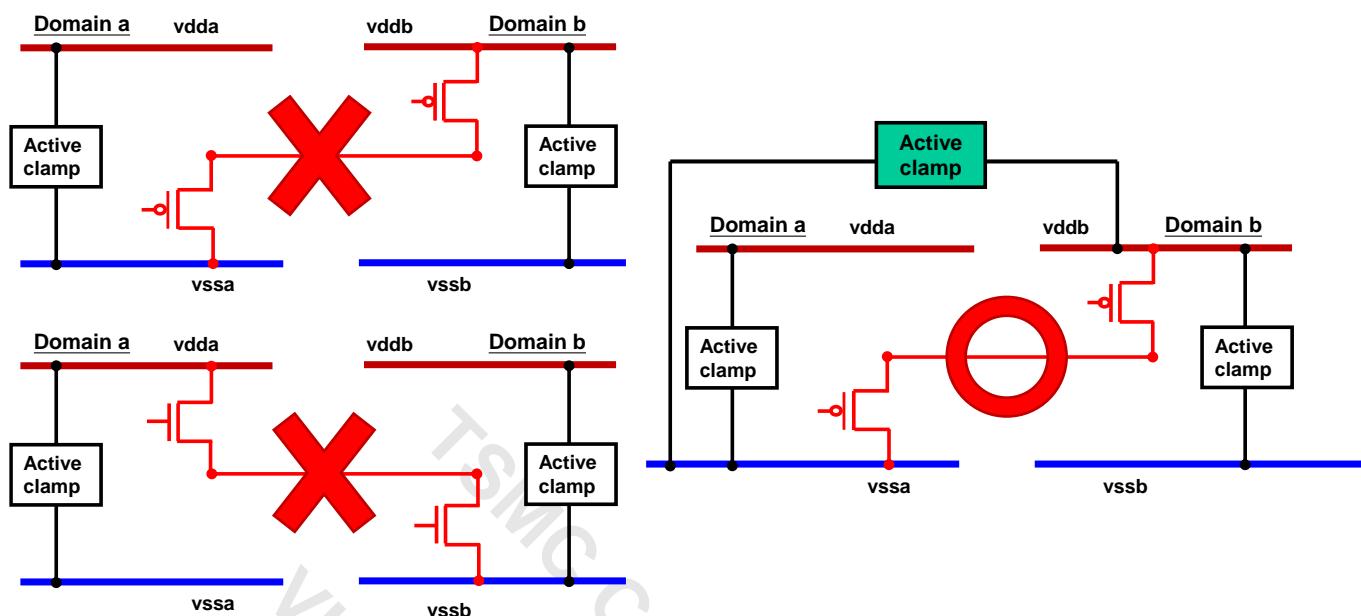


Figure 9.2.33.5 Cascoded (2-stage) N/PMOS under cross domain scenario is not allowed.

9.2.7.2 Metal Routing design Tip for HIA_DIO

- It is highly recommended to use Mz or metal layers above Mz for ESD devices local metal routing in order to maximize ESD devices performance.
- The width ($W \geq 2 \mu\text{m}$) of wide metal blocks at the boundaries of HIA_DIO. At least one metal layer is required to form the wide metal block pattern. All metal layers used to connect the HIA_DIO are required to have the wide metal blocks except for M1~M3. It is recommended to use as many metal layers as possible. (Figure 9.2.34)
- Metal widths and Via numbers have to follow the I_{ESD_DIO} in section 9.3.4 when enclosed by HIA_DUMMY. (Figure 9.2.34)

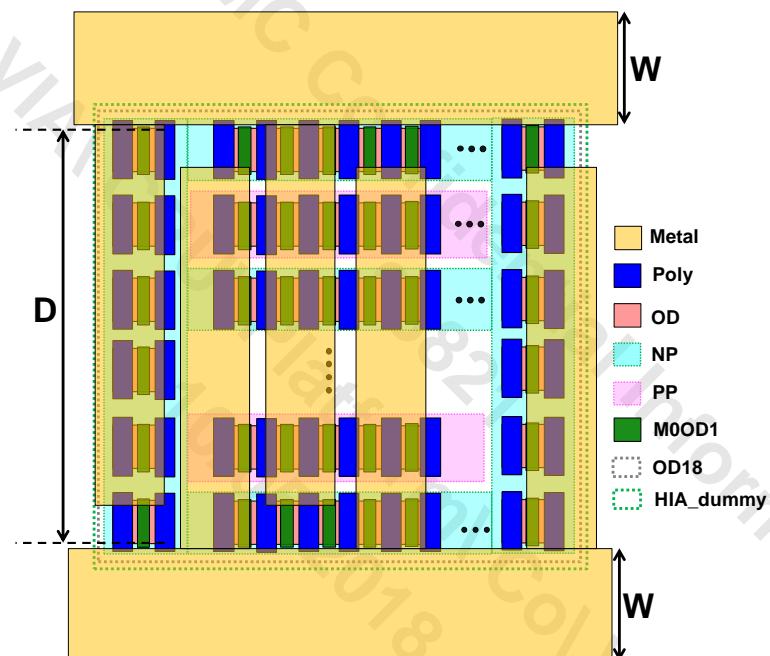


Figure 9.2.34 Metal routing for HIA_DIO

9.2.7.3 General Guideline for CDM Protection

- The guideline is for CDM 5/7/9/14A (FWHM< 1n sec) design reference.

General rules:

Rule No.	Description	Label	Op.	Rule
ESD.CDM.1g ^U	<p>For single stage snapback NMOS based primary protection, Output driving NMOS should be ≥ 3 stack I/O device ($L_g \geq 135\text{nm}$) with separated OD structure for all three stages. Output driving PMOS should be ≥ 2 stack I/O device ($L_g \geq 135\text{nm}$) with separated NW structure. (Figure 9.2.35~9.2.35.2) Core device or core-I/O device in cascaded scheme is not allowed. For I/O NMOS cascaded with I/O PMOS scheme, it is not allowed</p> <p>Exception:</p> <ol style="list-style-type: none"> Single stage snapback NMOS as secondary ESD protection with Rout (RESD) in series. Total channel width multiplies with Rout (RESD) value should be $\geq 1600\mu\text{m}^*\text{ohm}$. ≥ 2 stage I/O NMOS ($L_g \geq 135\text{nm}$) in separated OD structure with additional Rout in series. Rout value depends on the total width of NMOS, please refer to network calculator. ≥ 2 stage I/O NMOS ($L_g \geq 135\text{nm}$) with first stage being HIANMOS and in separated OD structure from others. Devices covered by ESDWDMY (255;110) are exempted from separated OD check. Devices without ESD path (S/D shorted) is exempted from this rule check. <p>Definition of separated OD:</p> <ol style="list-style-type: none"> 1st stage NMOS are surrounded by P+ guard ring. All devices inside the guard ring are the 1st stage ones only. 2nd stage NMOS are surrounded by P+ guard ring. All devices inside the guard ring are the 2nd stage ones only. 3rd stage NMOS are surrounded by P+ guard ring. The guard rings are tied to ground accordingly. For > 3 stack design scheme, the checker covers first three stages only. <p>Definition of separated NW:</p> <ol style="list-style-type: none"> The NW of each PMOS (P1a/P1b) of 2stack PMOS cannot tie to VDD. The NW of each PMOS (P1a/P1b) of 2stack PMOS cannot tie to its active OD. The NW of each PMOS (P1a/P1b) of 2 stack PMOS cannot tie to active OD of the other PMOS. The NW of PMOS(P1a) cannot tie to that of the other PMOS (P1b). 1st stage PMOS are surrounded by N+ guard ring. All devices inside the guard ring are the 1st stage ones only. 2nd stage PMOS are surrounded by N+ guard ring. The guard rings are tied to virtual power accordingly. For > 3 stack design scheme, the checker covers first three stages only. <p>This rule is based on limited test structure. For single stage MOS, it is based on gate-grounded design. For cascaded scheme, the test structure is with top-gate floating and bottom-gate grounded. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.</p>			
ESD.CDM.1.1g ^U	For 2-stage cascaded snapback NMOS based primary protection, Output driving NMOS should be ≥ 3 stack I/O device ($L_g \geq 135\text{nm}$) with first			

Rule No.	Description	Label	Op.	Rule
	<p>stage being HIANMOS and in separated OD structure (surrounded by double ring) for all three stages.</p> <p>Output driving PMOS should be ≥ 3 stack I/O device ($Lg \geq 135nm$) with separated NW structure (surrounded by double ring) for all three stages. (Figure 9.2.36~9.2.36.2)</p> <p>Core device or core-I/O device in cascaded scheme is not allowed. For I/O NMOS cascaded with I/O PMOS scheme, it is not allowed</p> <p>Exception:</p> <ol style="list-style-type: none"> 1. 2-stage cascaded snapback NMOS as secondary ESD protection (common OD) with Rout (RESD) in series. Total channel width multiplies with Rout (RESD) value should be $\geq 1600\mu m \cdot ohm$. 2. Devices covered by ESDWDMY (255;110) are exempted from separated OD check. 3. Devices without ESD path (S/D shorted) is exempted from this rule check. <p>Definition of separated OD (surrounded by double ring):</p> <ol style="list-style-type: none"> 1. 1st stage NMOS are surrounded by P+ guard ring and the P+ guard ring is surrounded by N+ guard ring. All device inside the guard ring are the 1st stage ones only. 2. 2nd stage NMOS are surrounded by P+ guard ring and the P+ guard ring is surrounded by N+ guard ring. All device inside the guard ring are the 2nd stage ones only. 3. 3rd stage NMOS are surrounded by P+ guard ring and the P+ guard ring is surrounded by N+ guard ring. 4. P+ guard rings are tied to ground accordingly and N+ guard ring are tied to power accordingly. 5. For > 3 stack design scheme, the checker only check first three stage only. <p>Definition of three separated NWs (surrounded by double ring):</p> <ol style="list-style-type: none"> 1. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to VDD. 2. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to its active OD. 3. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to active OD of the other PMOS. 4. The NW of each PMOS (P1a/P1b/P1c) of 3 stack PMOS cannot tie to each other. 5. 1st stage PMOS are surrounded by N+ guard ring and the N+ guard ring is surrounded by P+ guard ring. All device inside the guard ring are the 1st stage ones only. 6. 2nd stage PMOS are surrounded by N+ guard ring and the N+ guard ring is surrounded by P+ guard ring. All device inside the guard ring are the 2nd stage ones only. 7. 3rd stage PMOS are surrounded by N+ guard ring and the N+ guard ring is surrounded by P+ guard ring 8. P+ guard rings are tied to ground accordingly and N+ guard ring are tied to virtual power accordingly. 9. For > 3 stack design scheme, the checker only check first three stage PMOS only. <p>This rule is based on limited test structure. For single stage MOS, it is based on gate-grounded design. For cascaded scheme, the test structure is with top-gate floating and bottom-gate grounded. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.</p>			
ESD.CDM.1.3g ^U	For snapback NMOS protected IOPAD, its primary ESD protection and secondary ESD protection should be on the common ground.			

Rule No.	Description	Label	Op.	Rule
ESD.CDM.2g ^U	<p>For diode based primary protection, Output driving N/PMOS need ≥ 2 stack for pure I/O device scheme and ≥ 3 stack for pure core device scheme (Figure 9.2.37). All of them need to follow separated OD structure (Figure 9.2.37.2 and 9.2.37.3).</p> <p>For NMOS cascoded with PMOS scheme, additional Rout in series is required.</p> <p>For core device cascoded with I/O device, additional Rout in series is required.</p> <p>Definition of separated OD</p> <ol style="list-style-type: none"> 1. 1st stage NMOS (PMOS) are surrounded by P+ guard ring (N+ guard ring). All device inside the guard ring are the 1st stage ones only. 2. 2nd stage NMOS (PMOS) are surrounded by P+ guard ring (N+ guard ring). All device inside the guard ring are the 2nd stage ones only. For ≥ 2 stack pure I/O cascaded scheme, the 2nd stage NMOS (PMOS) can share guard ring with the other internal device except the 1st stage ones. 3. 3rd stage NMOS (PMOS) are surrounded by P+ guard ring (N+ guard ring) 4. The guard rings are tied to power/ground accordingly. 5. For > 2 stack design scheme, the checker only check first two stage only. <p>Exception:</p> <ol style="list-style-type: none"> 1. Single stage N/PMOS connected VDD/VSS with Rout in series (Fig.9.2.37.1). The Rout value depends on the total width of N/PMOS, please refer to network calculator. 2. Cascoded N/PMOS with common OD structure and Rout in series. The Rout value depends on the total width of cas-N/PMOS, please refer to network calculator. 3. Devices without ESD path (S/D shorted) is exempted from this rule check. 4. Devices covered by ESDWDMY (255;110) are exempted from separated OD check. 5. Devices without ESD path (S/D shorted) is exempted from this rule check <p>This rule is based on limited test structure. For single stage MOS, it is based on gate-grounded design. For cascaded scheme, the test structure is with top-gate floating and bottom-gate grounded. ESD immunity highly depends on circuit design and real layout implantation, please ensure the MOS channel are turned off during ESD event and design is Si-proven before mass production.</p>			
ESD.CDM.B.1g ^U	<p>On-chip global ESD bus (user defined) is required, each Ground bus need connecting the global bus with back-to-back (B2B) diode or metal in short scheme.</p> <p>The back to back (B2B) diode can be HIA diode (Rotated-STI). (Fig. 9.2.38)</p> <p>The perimeter of HIA diode as back to back diode need to meet HIA.3g.</p> <p>(ESD device size requirement is changed with target CDM level. For details, please refer to 9.2.5.9)</p>			
ESD.CDM.B.2g ^U	<p>Cross domain back to back (B2B) diode is needed. (Fig. 9.2.38.1)</p> <p>The back to back diode can be HIA diode (Rotated-STI).</p> <p>The perimeter of HIA diode as back to back diode need to meet HIA.3g</p> <p>(ESD device size requirement is changed with target CDM level. For details, please refer to 9.2.5.9)</p>			
ESD.CDM.4g ^U	<p>For cascaded (3.3V) power clamp protected power domain, additional reverse HIA diode (in parallel with cascaded power clamp) is need.</p> <p>The area of HIA diode needs to meet HIA.3.1g. (Fig. 9.2.39)</p> <p>(ESD device size requirement is changed with target CDM level. For details, please refer to 9.2.5.9)</p>			
ESD.CDM14A.4.1 ^g ^U	<p>For 2-stage cascaded snapback NMOS based primary protection, additional n-type HIA diode, between IOPAD and ground net, is needed. (Fig. 9.2.39)</p> <p>The perimeter of HIA diode needs to meet HIA.CDM14A.3g.</p>			

Rule No.	Description	Label	Op.	Rule
	(This rule is defined for CDM peak current 14A)			
ESD.CDM.6g	Core ESD power clamp (not in OD2) can not be used for > 1.115V application. (Fig. 9.2.40)			
ESD.CDM.6.1g	Single stage IO ESD power clamp can not be used for > 1.98V application. (Fig. 9.2.40) Single stage means all ACTIVE OD SEGMENT on single ACTIVE OD are connected to power or ground net.			
ESD.CDM.C.2g ^U	For any MOS connected to Power or Ground, there should be a power clamp with spacing $\leq A \mu\text{m}$ or $R_{bus} \leq B \text{ ohm}$ for core (0.75V) domain and $\leq C \text{ ohm}$ for IO (1.8V) domain. (Fig.9.2.41) Devices covered by ESDWDMY (255;110) are exempted. (ESD Rbus resistance requirements are changed with target CDM level.)			RuleTable .9.2.7.3.1
ESD.CDM.C.3.1g ^U	For any core MOS with gate and source/drain connected between power or ground, there should be a single stage core power clamp with spacing $\leq A \mu\text{m}$ or $R_{bus} \leq B \text{ ohm}$. (Fig.9.2.41.1) The power clamp and the protected core MOS must be at the same P/G pair. Lack of direct clamping ESD device is not allowed. Decap is excluded from this rule. Devices covered by ESDWDMY (255;110) are exempted. (ESD Rbus resistance requirements are changed with target CDM level.)			RuleTable .9.2.7.3.1
ESD.CDM.C.3.2g ^U	For any I/O MOS with gate and source/drain connected between power or ground, there should be a single stage I/O or core power clamp with spacing $\leq A \mu\text{m}$ or $R_{bus} \leq C \text{ ohm}$. (Fig.9.2.41.1) The power clamp and the protected I/O MOS must be at the same P/G pair. Lack of direct clamping ESD device is not allowed. Decap is excluded from this rule. Devices covered by ESDWDMY (255;110) are exempted. (ESD Rbus resistance requirements are changed with target CDM level.)			RuleTable .9.2.7.3.1
ESD.CDM.C.4g ^U	For IO/core cross domain interface, there should be a rule compliance cross domain power clamp with spacing $\leq A \mu\text{m}$ or $R_{bus} \leq B \text{ ohm}$ for core (0.75V) domain and $\leq C \text{ ohm}$ for IO (1.8V) domain. (Fig 9.2.42) Devices covered by ESDWDMY (255;110) are exempted. (ESD Rbus resistance requirements are changed with target CDM level.)			RuleTable .9.2.7.3.1
ESD.CDM.C.4.1g ^U	For IO/core cross domain interface, there should be a rule compliance cross domain back-to-back diode with spacing $\leq A \mu\text{m}$ or $R_{bus} \leq B \text{ ohm}$ for core (0.75V) domain and $\leq C \text{ ohm}$ for IO (1.8V) domain. (Fig 9.2.42.1) Devices covered by ESDWDMY (255;110) are exempted. (ESD Rbus resistance requirements are changed with target CDM level.)			RuleTable .9.2.7.3.1
ESD.CDM.C.5g ^U	For any MOS connected to Power or Ground in small power domain, there should be a power clamp with spacing $\leq A \mu\text{m}$ or $R_{bus} \leq B \text{ ohm}$ for core (0.75V) domain and $\leq C \text{ ohm}$ for IO (1.8V) domain. (Figure 9.2.41) For the power domain with power clamp total channel width less than two times of rule criteria, ESD.40g, ESD.40.1g and ESD.40.2g group, it is defined as a small power domain. For those non-small power domain, the spacing between power clamp and MOS can be relaxed and referred to ESD.CDM.C.2g. Devices covered by ESDWDMY (255;110) are exempted. (ESD device size and ESD Rbus resistance requirements are changed with target CDM level. For details, please refer to 9.2.5.9 and table 9.2.7.3.1)			RuleTable .9.2.7.3.1
ESD.CDM.X.1g ^U	For cross domain interface with core receiver (non-footer/header design),			RuleTable

Rule No.	Description	Label	Op.	Rule
	<p>secondary ESD with ESD resistor is required. The secondary ESD requirement follows ESD.1.1gU, ESD.8.1gU~ESD.9.3gU and ESD.45gU ~ ESD.47gU.</p> <p>For IO/core cross domain interface, cross domain power clamps between vdda-to-vssb and vdःdb-to-vssa are required. (Figure 9.2.43)</p> <p>This rule checks on both core/IO receiver without footer/header design. (ESD resistor width and ESD device size requirements are changed with target CDM level. For details, please refer to ESD.8.1gU group and section 9.2.5.9)</p>			.9.2.7.3.1
ESD.XDM.VIC.3g ^U	<p>N/PMOS with gate connected to power directly, and source/drain connected to different power through MOS source/drain is not allowed, vice versa.</p> <p>Both IO and core device are checked. N/PMOS mixed scheme is also checked. This rule checks for both common ground and separated ground scenario. (Figure 9.2.44)</p> <p>Exception: Power clamp between both vdda/vss and vdःdb/vss (on the same ground plane) is two times larger than ESD.40g, ESD.40.1g, ESD.40.2.1g defined. (ESD device size requirement is changed with target CDM level. For details, please refer to 9.2.5.9)</p>			
ESD.XDM.VIC.4g ^U	<p>N/PMOS with source connected to power directly, and drain connected to different power through MOS source/drain is not allowed.</p> <p>Both IO and core device are checked. N/PMOS mixed scheme is also checked. This rule checks for both common ground and separated ground scenario. (Figure 9.2.44)</p> <p>Exception: Power clamp between vdda/vss and vdःdb/vss (on the same ground plane) is two times larger than ESD.40g, ESD.40.1g, ESD.40.2.1g defined. (ESD device size requirement is changed with target CDM level. For details, please refer to 9.2.5.9)</p>			

Table 9.2.7.3.1 ESD power clamp, B2B diode placement and effective Rbus requirement

RuleTable.9.2.7.3.1		CDM 5A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)	CDM 14A (FWHM < 1ns)
ESD.CDM.C.2g ^U	Internal device to power clamp space (A) (μm)	1500	1500	1250	1000
	Rbus for core domain (B) (Ω)	0.5	0.5	0.35	0.2
	Rbus for IO domain (C) (Ω)	2	2	1.5	1
ESD.CDM.C.3.1g ^U	Internal device to power clamp space (A) (μm)	1500	1500	1250	1000
	Rbus for core domain (B) (Ω)	0.5	0.5	0.35	0.2
ESD.CDM.C.3.2g ^U	Internal device to power clamp space (A) (μm)	1500	1500	1250	1000
	Rbus for IO domain (C) (Ω)	2	2	1.5	1
ESD.CDM.C.4g ^U	Internal device to power clamp space (A) (μm)	--	500	500	500
	Rbus for core domain (B) (Ω)	--	0.1	0.1	0.1
	Rbus for IO domain (C) (Ω)	--	0.5	0.5	0.5
ESD.CDM.C.4.1g ^U	Internal device to B2B diode space (A) (μm)	--	500	500	500
	Rbus for core domain (B) (Ω)	--	0.1	0.1	0.1
	Rbus for IO domain (C) (Ω)	--	0.5	0.5	0.5
ESD.CDM.C.5g ^U	Internal device to power clamp space (A) (μm)	--	500	500	500
	Rbus for core domain (B) (Ω)	--	0.1	0.1	0.1
	Rbus for IO domain (C) (Ω)	--	0.5	0.5	0.5
ESD.XDM.X.1g ^U	Cross domain power clamp/2 nd ESD requirement	Nice to have	Needed	Needed	Needed

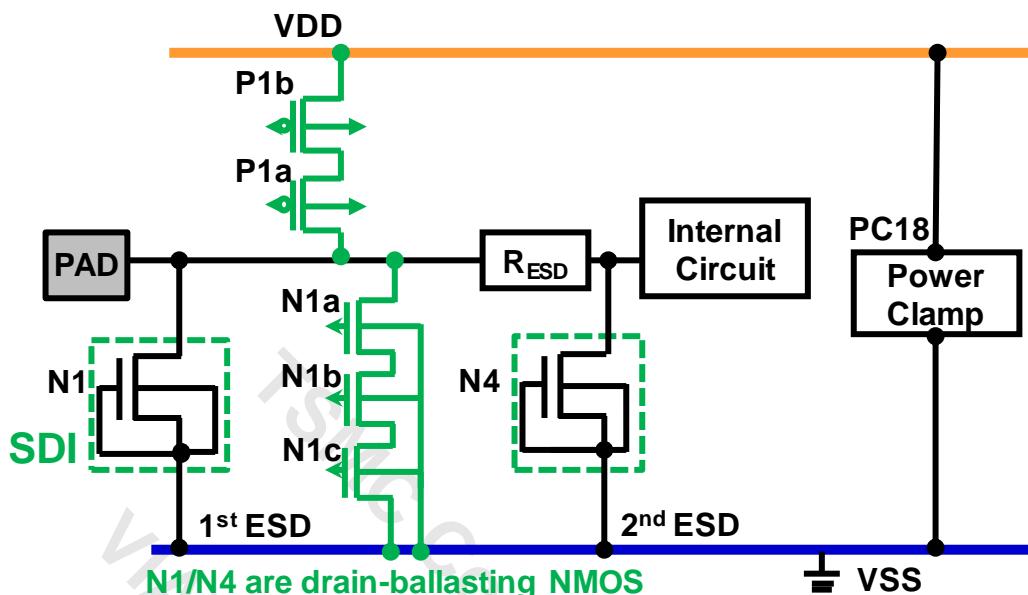


Figure 9.2.35 Snapback base primary protection scheme

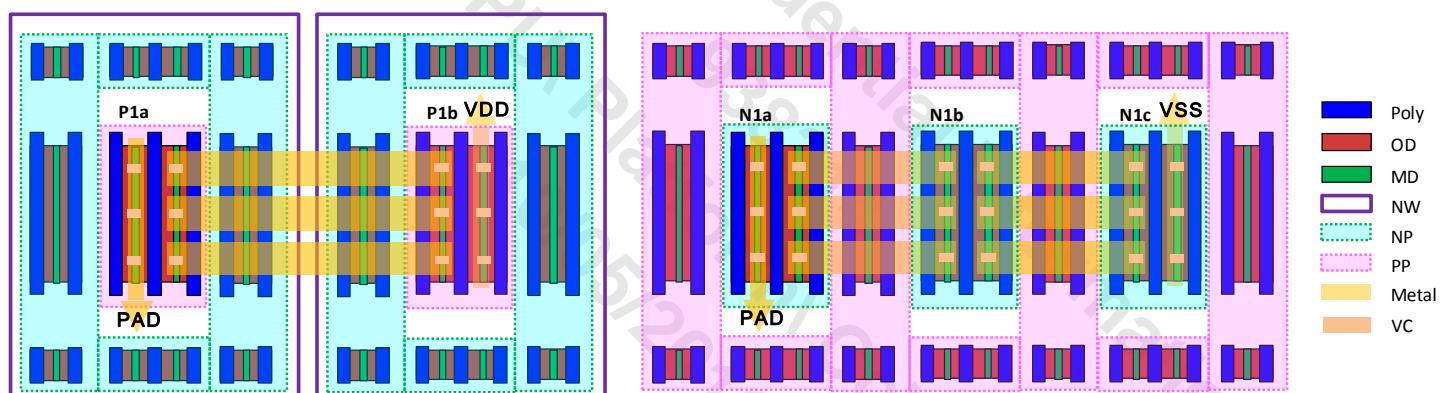


Figure 9.2.35.1 Layout view of 3-stack separated OD NMOS and 2-stack separated NW PMOS

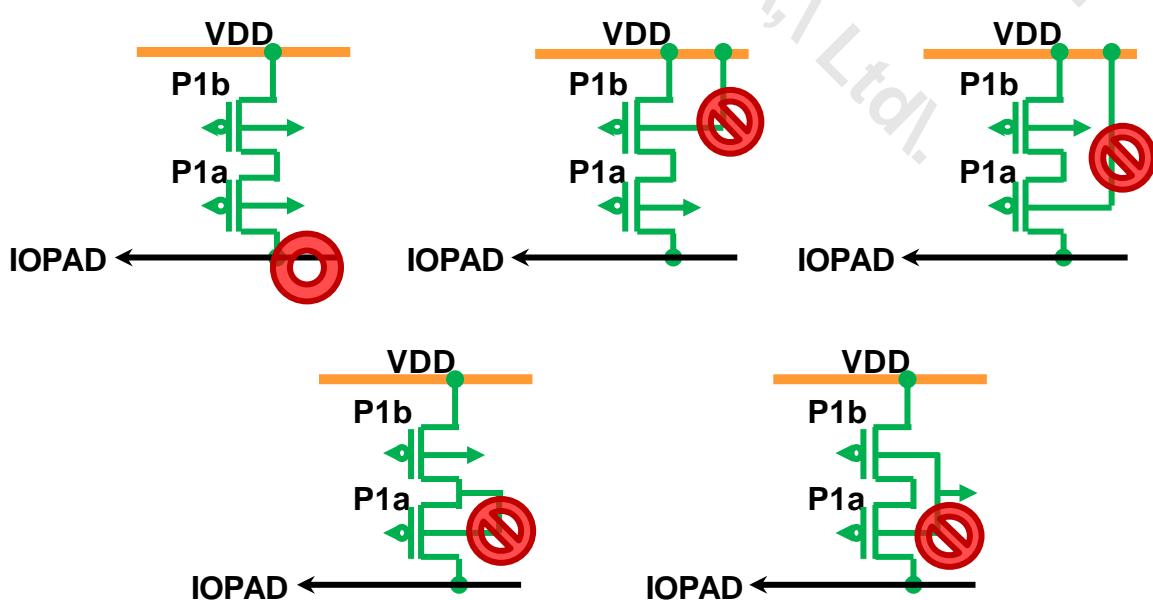


Figure 9.2.35.2 Schematic view of 2-stack PMOS with 2 separated NWs

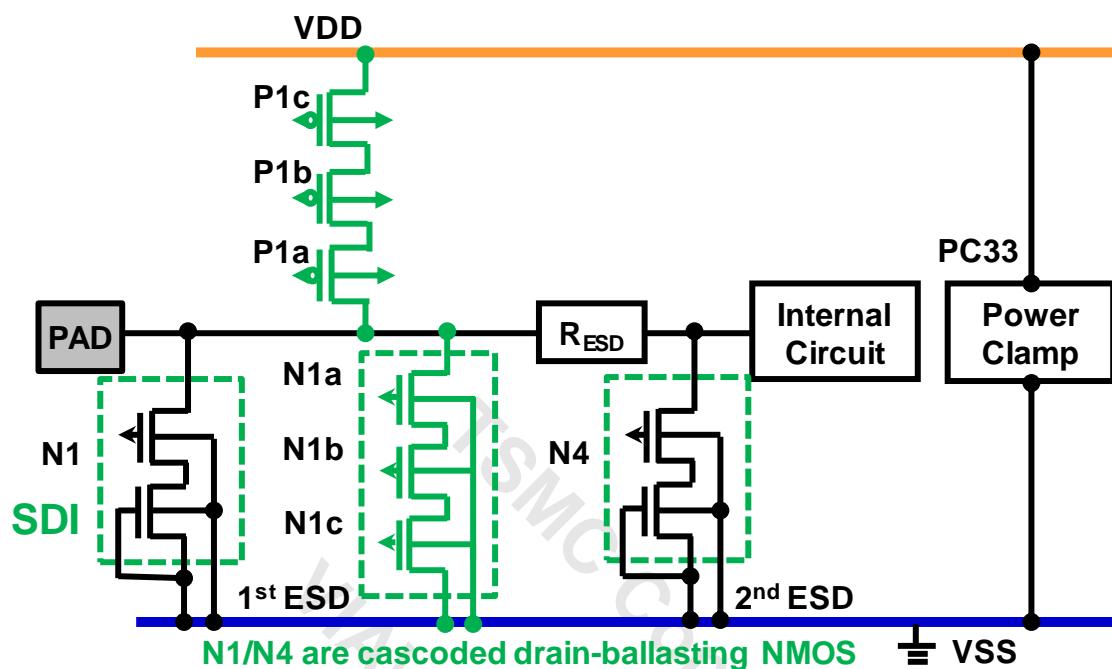


Figure 9.2.36 Cascoded snapback base primary protection scheme

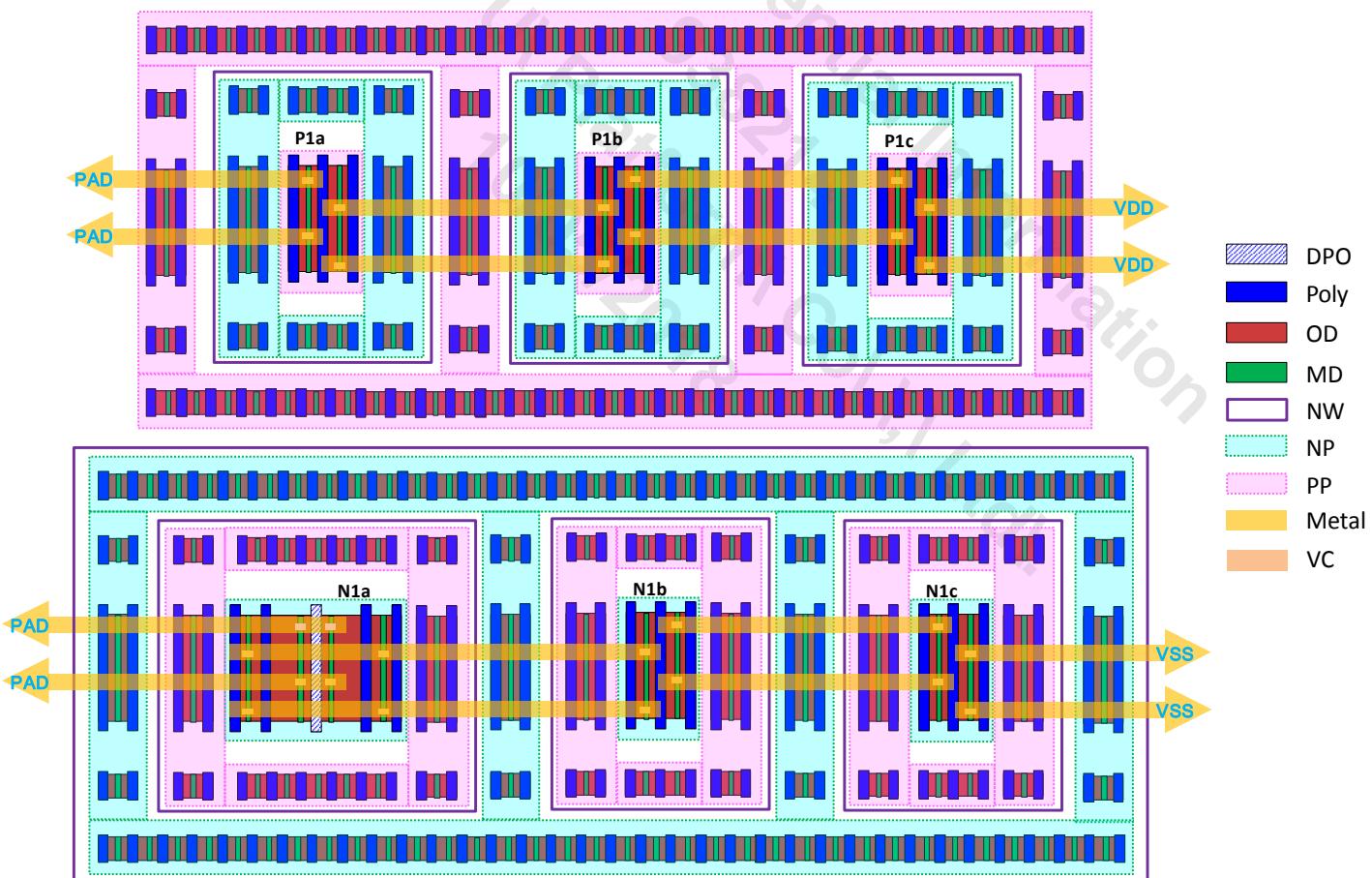


Figure 9.2.36.1 Layout view of 3-stack separated OD NMOS (first-stage is HIANMOS) and 3-stack separated NW PMOS

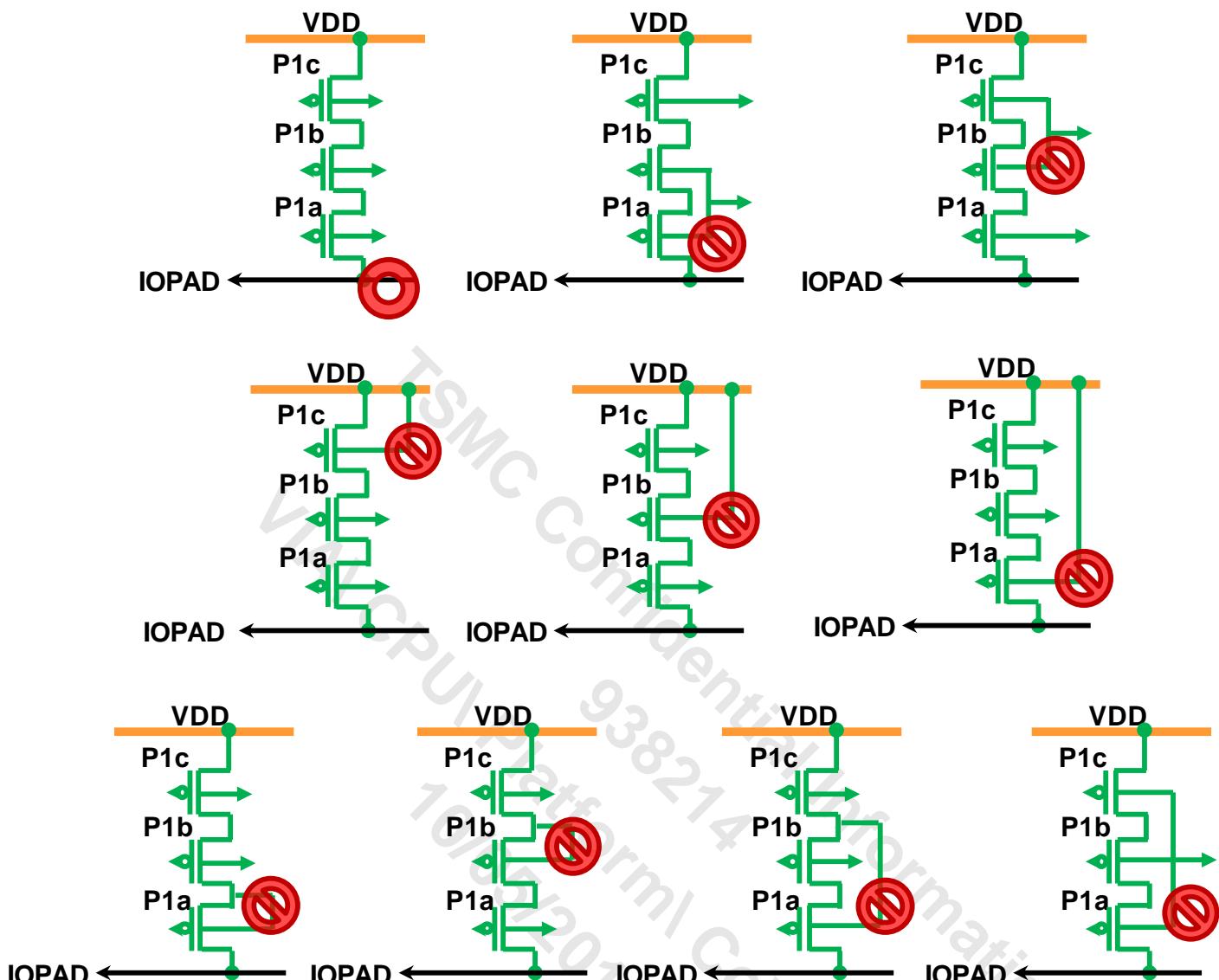


Figure 9.2.36.2 Schematic view of 3-stack PMOS with 3 separated NWs

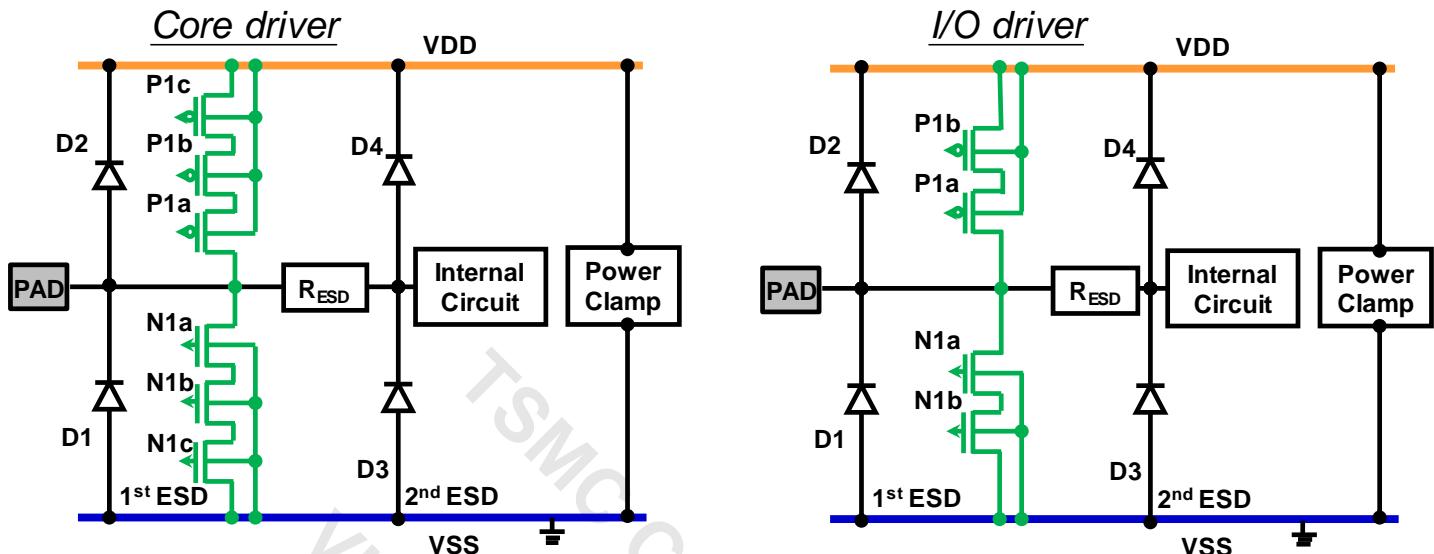
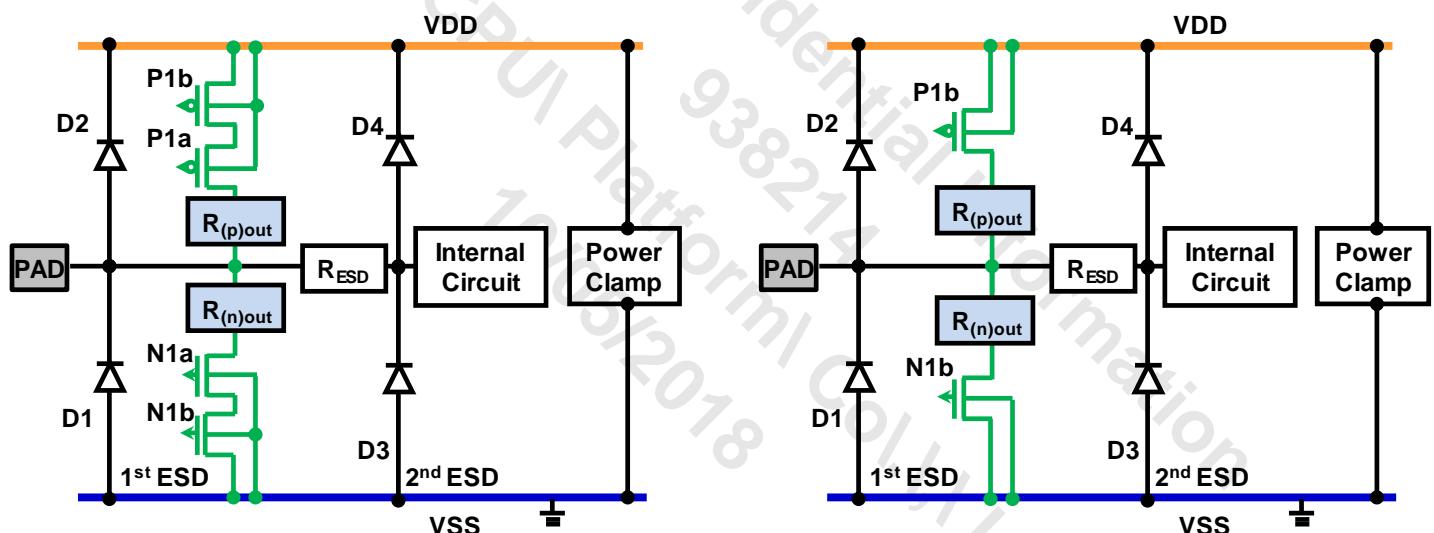
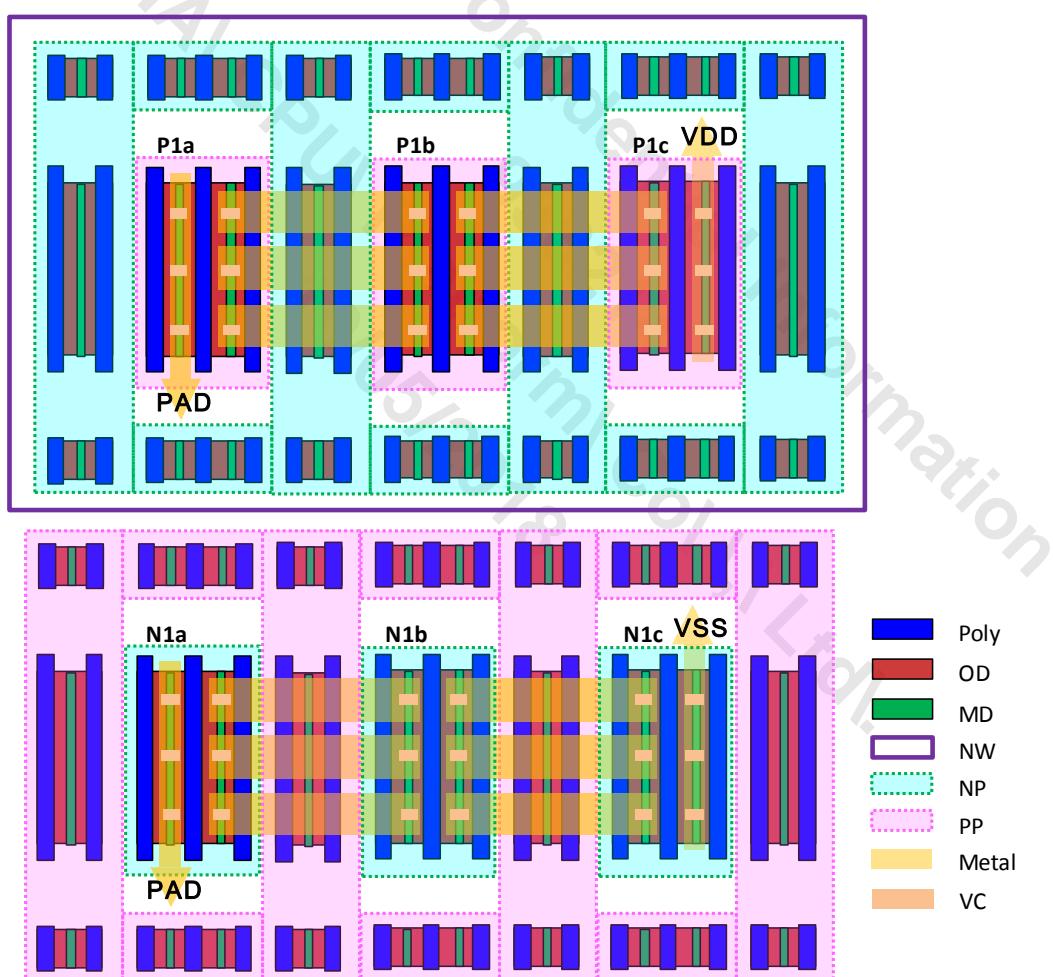
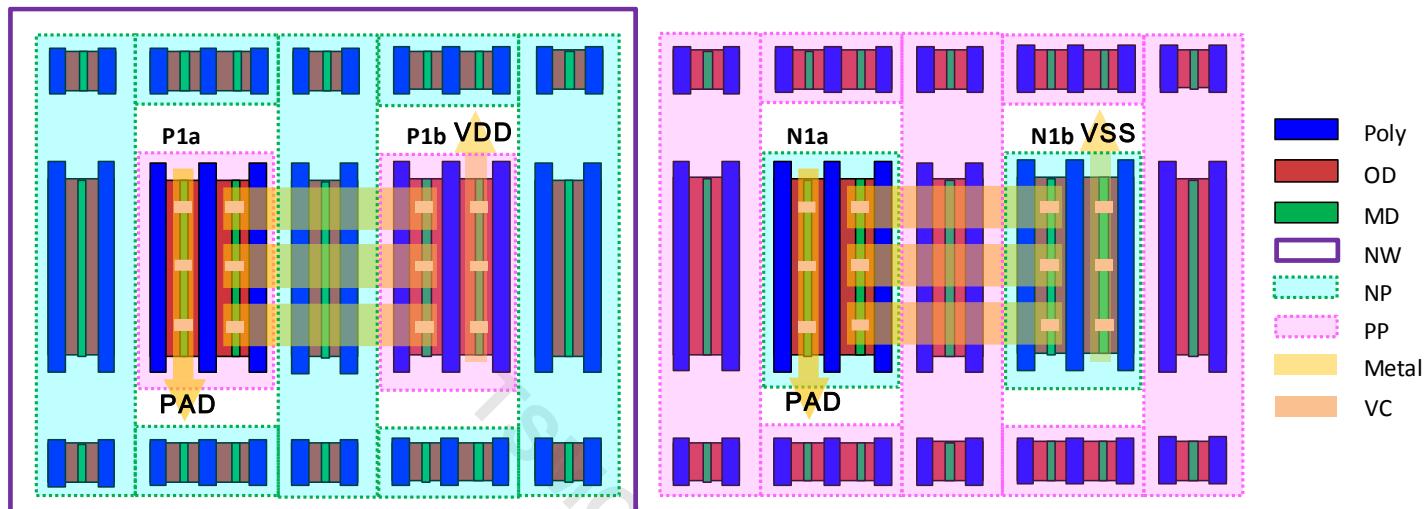


Figure 9.2.37 Diode Base Primary Protection scheme

Figure 9.2.37.1 Diode base primary protection scheme with serial resistor R_{out}



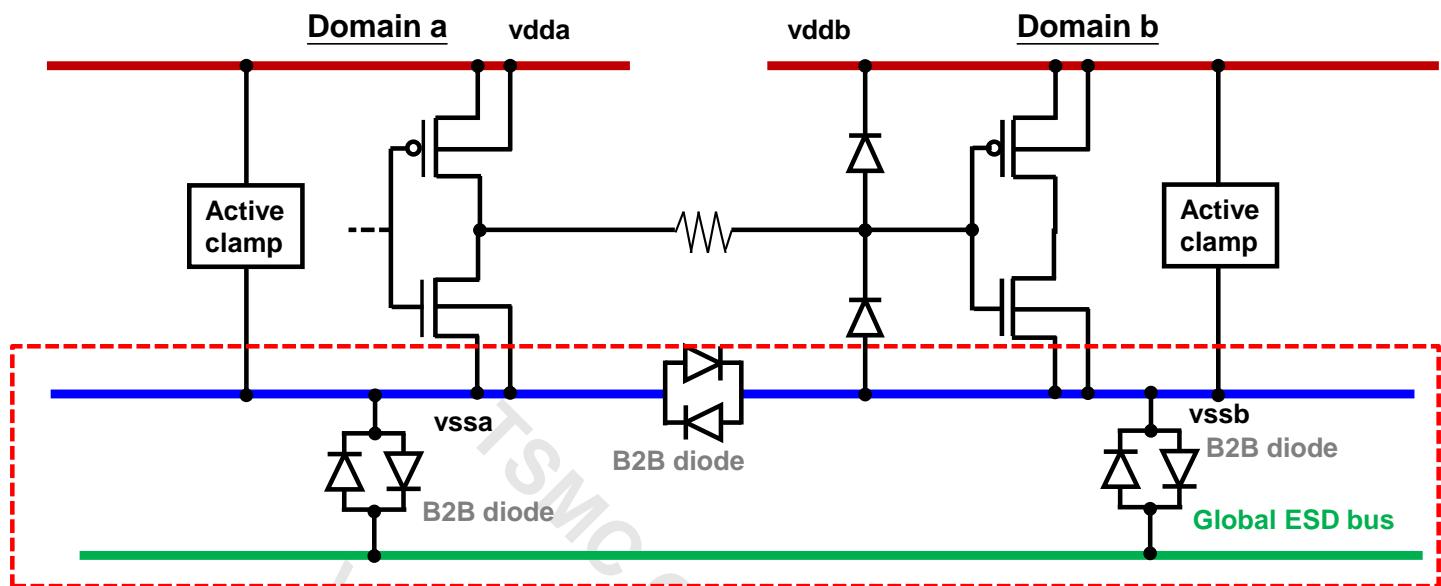


Figure 9.2.38 Back to Back diode for global ESD bus

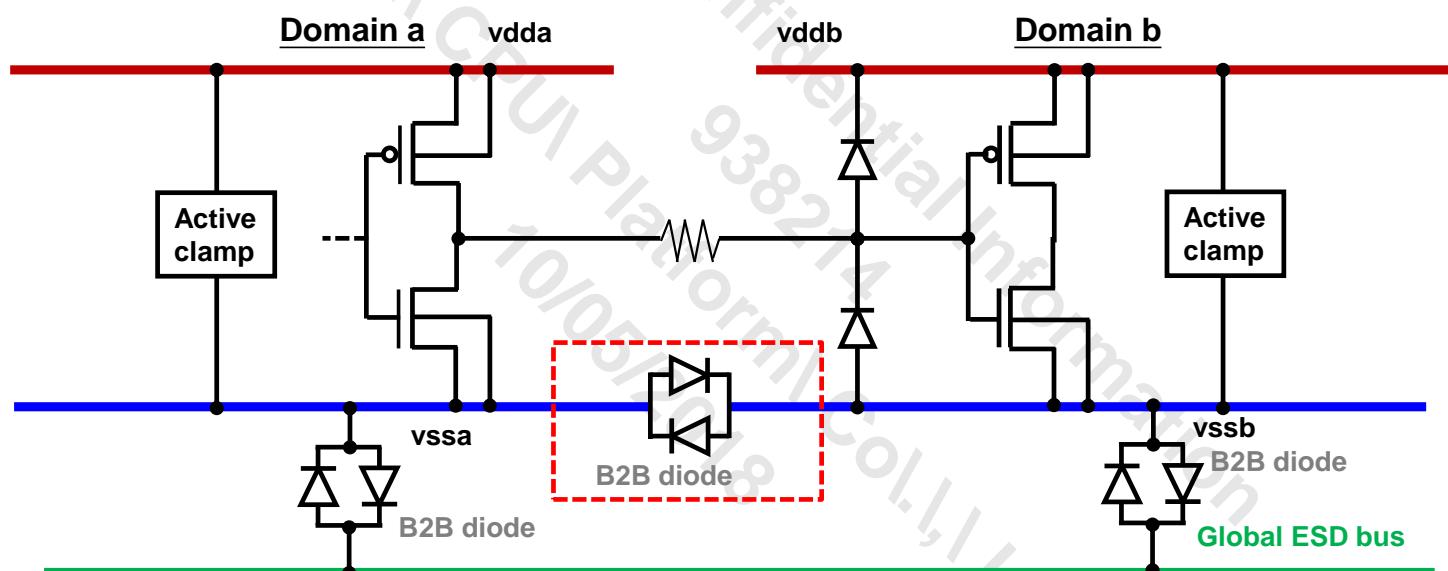


Figure 9.2.38.1 Back to Back diode for cross domain interface

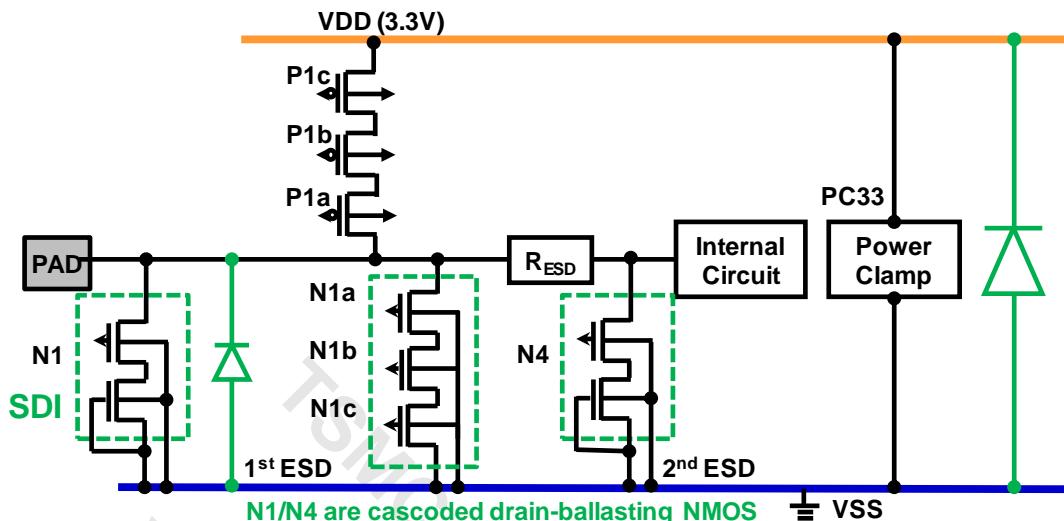


Figure 9.2.39 Power-to-Ground reverse diode for 3.3V power clamp (ESD.CDM.4g) and IO-to-ground reverse n-diode for cascoded snapback based primary protection (ESD.CDM14A.4.1g)

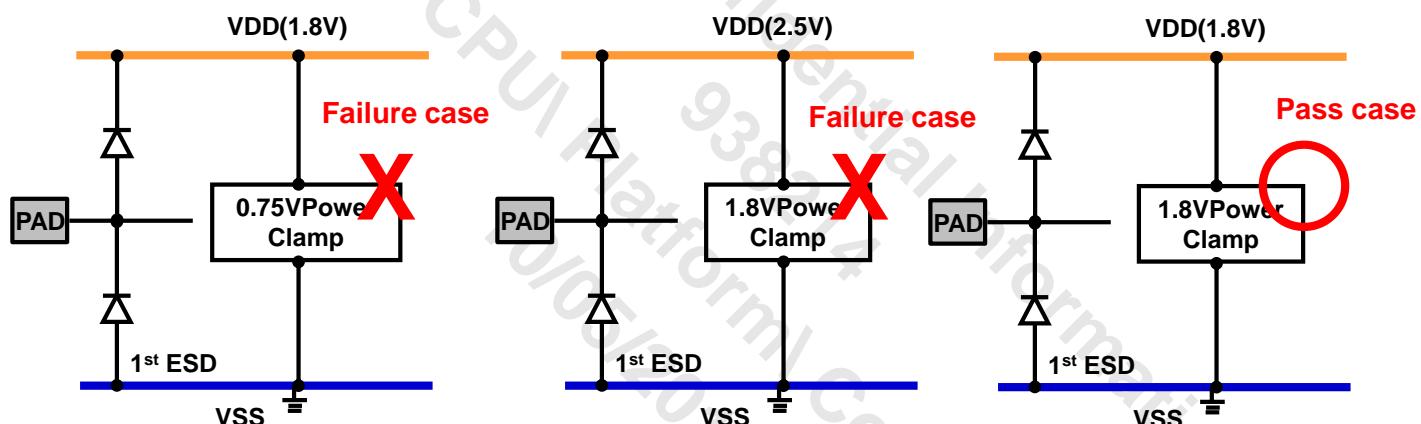
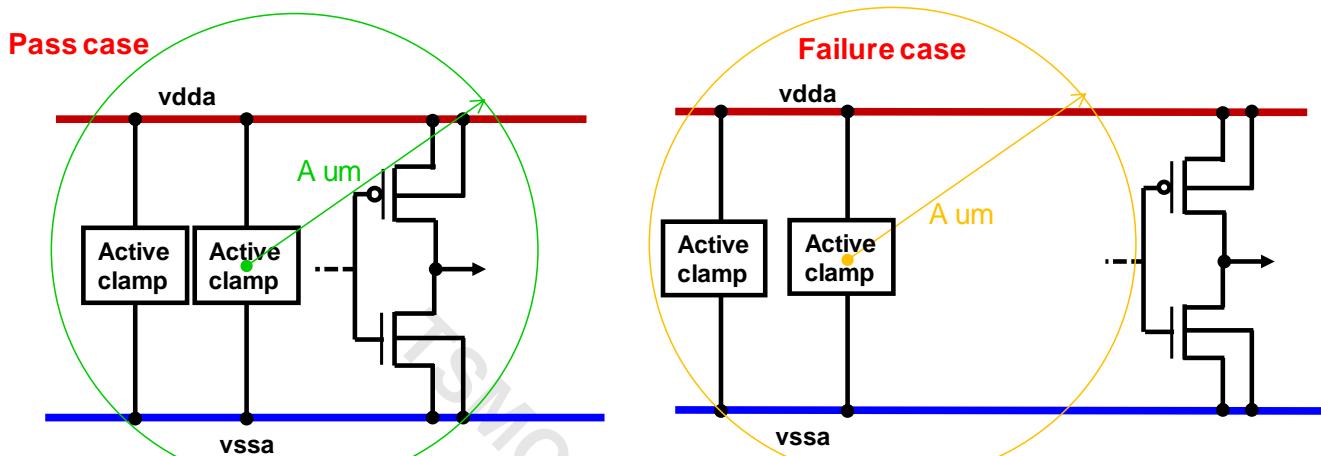
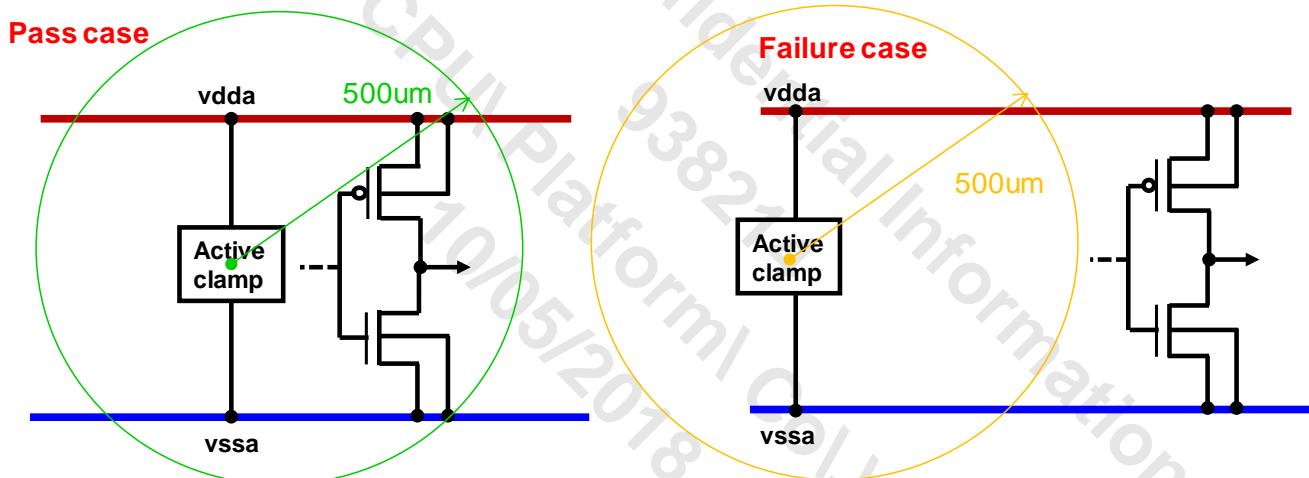
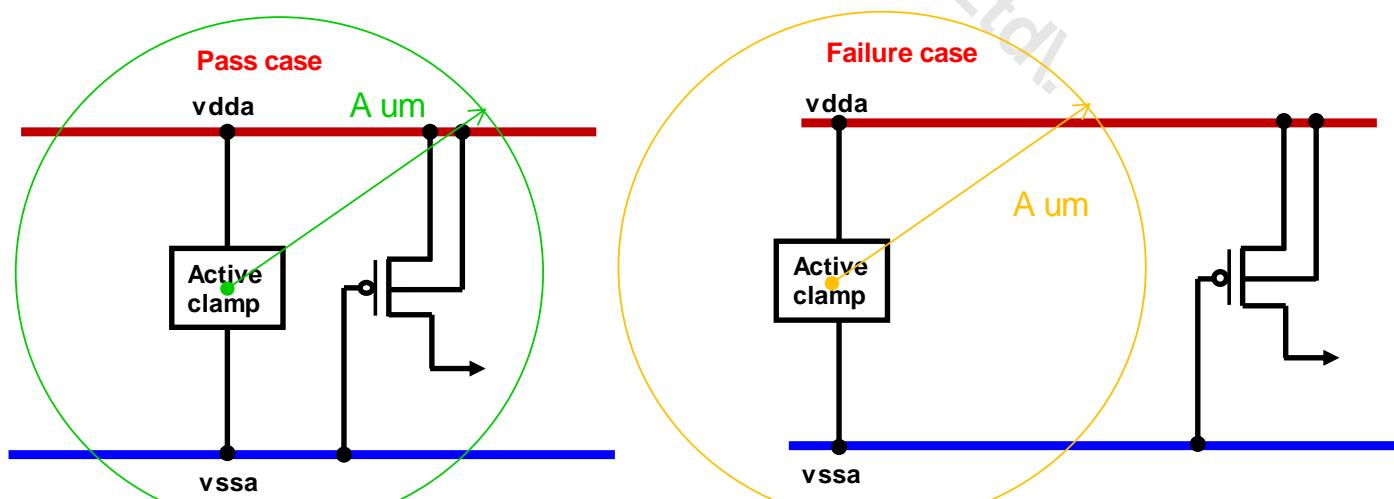


Figure 9.2.40 Power clamp implementation rule

Big power domain (ESD.CDM.C.2g)**Small power domain (ESD.CDM.C.5g)****Figure 9.2.41 Power clamp placement uniformity for all blocks****Figure 9.2.41.1 Power clamp placement uniformity for gate direct tie to P/G design**

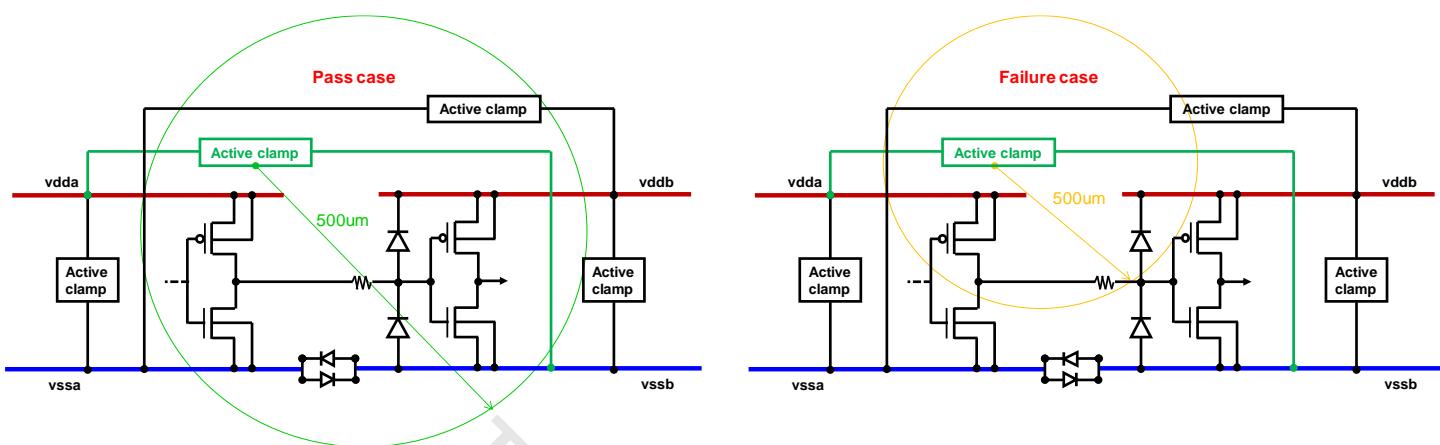


Figure 9.2.42 Power clamp placement uniformity for cross domain interface

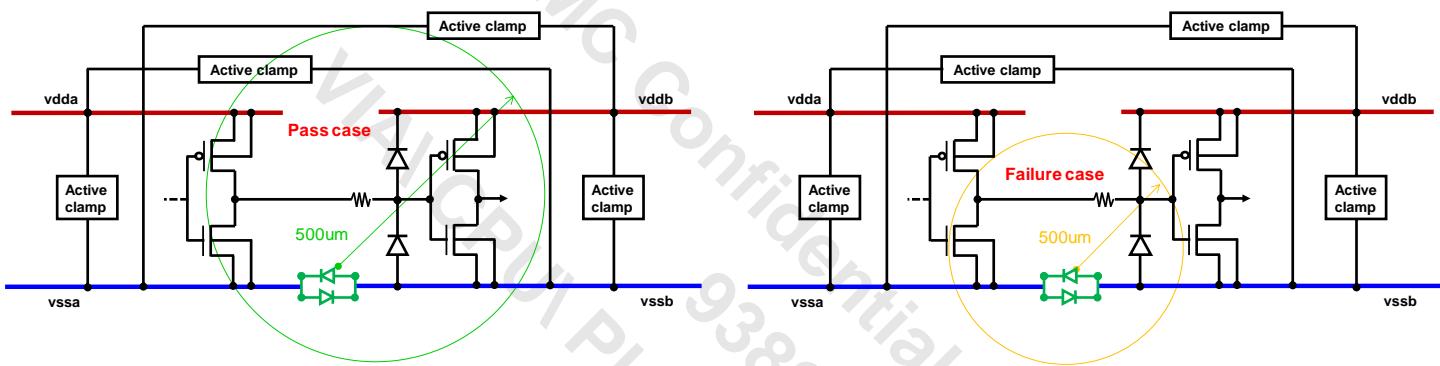


Figure 9.2.42.1 Back-to-Back diode placement uniformity for cross domain interface

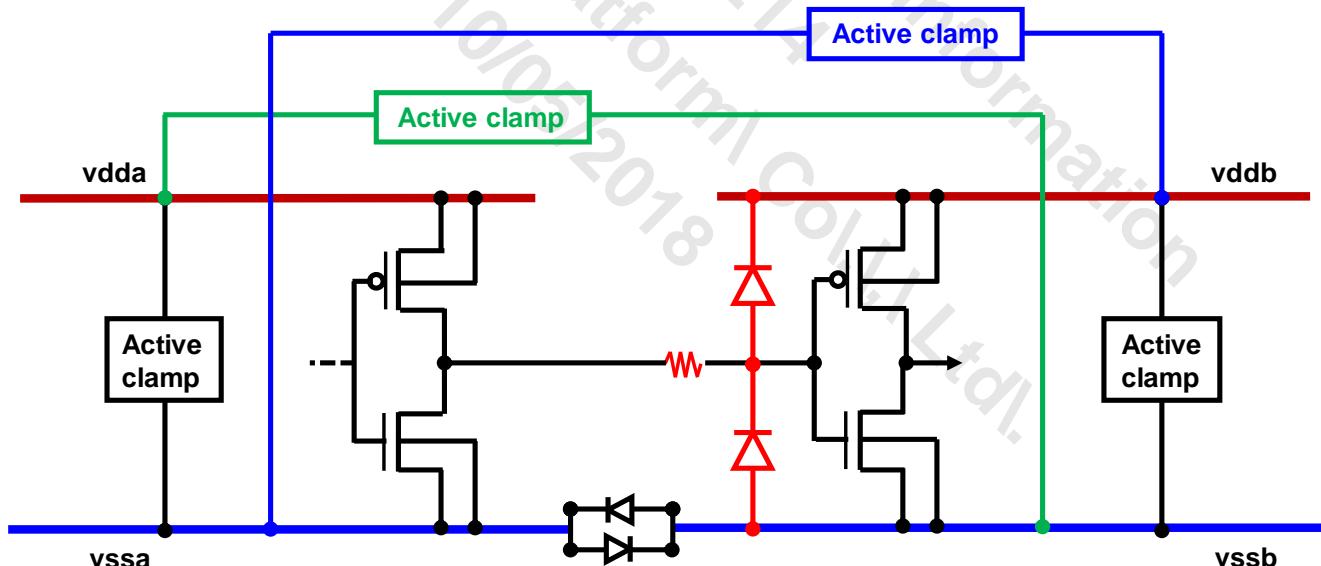


Figure 9.2.43 Cross domain power clamp and secondary ESD

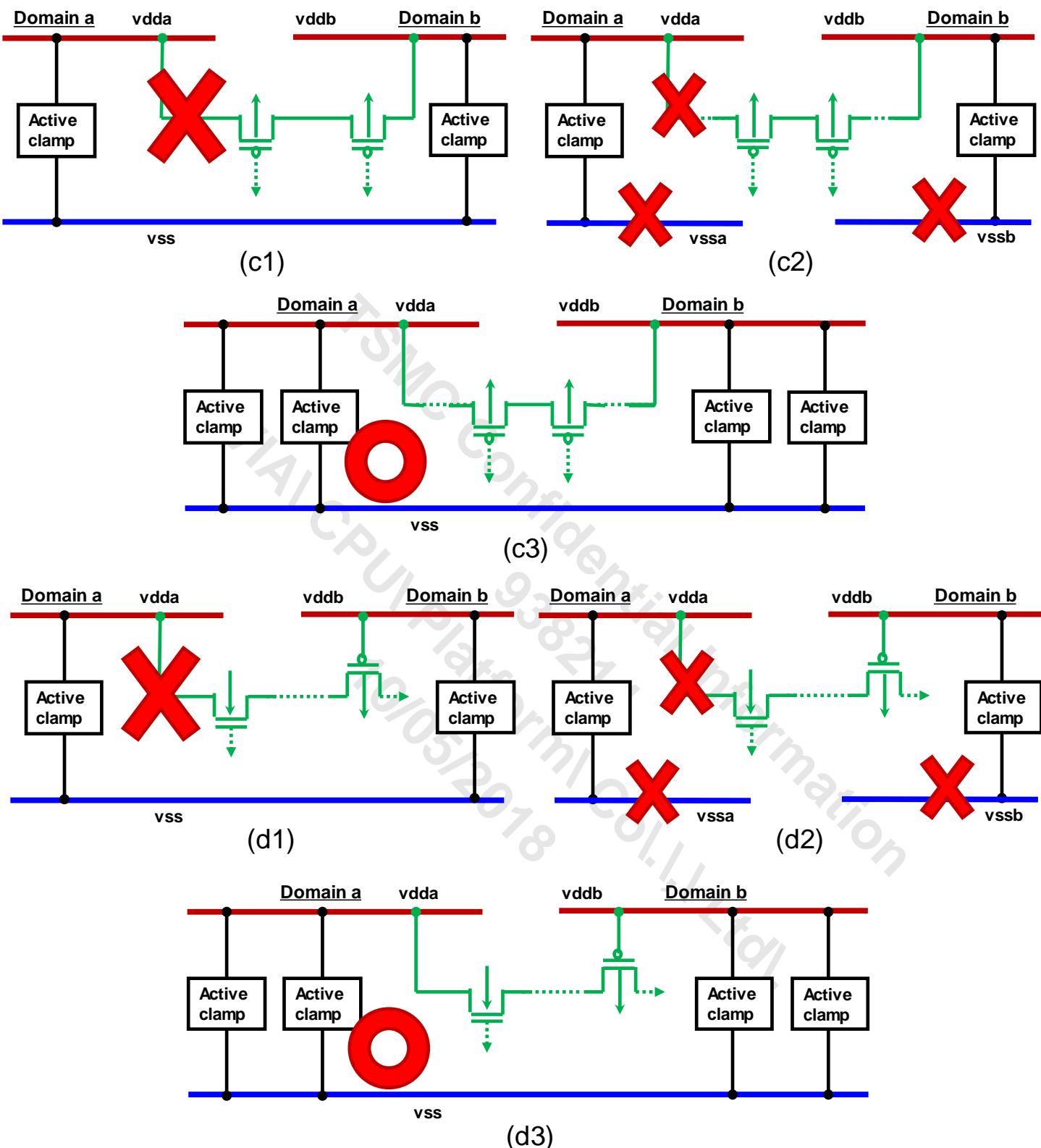


Figure 9.2.44 Cross power domain scheme with high ESD risk

Resistance rules:

Rule No.	Description	Label	Op.	Rule
ESD.CDM.P.1g ^U	Metal Bus resistance of IOPAD to ESD dual diode R1 & R3. (Fig.9.2.50) Metal Bus resistance of IOPAD to ESD snapback NMOS (nch_HIA18) R3. (Fig.9.2.51) No needed to take "R0" into account. (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.1.1g ^U	Metal Bus resistance from primary ESD dual diode to closest Power and Ground bump R1' & R3'. (Fig.9.2.50) Metal Bus resistance from primary snapback NMOS to closest Ground bump R3'. (Fig.9.2.51) No needed to take "R0" into account. (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.2g ^U	Metal Bus resistance of ESD dual diode to "core, IO(1.8V) or cascaded IO (3.3V)" power clamp R1'+R2+R4, R3'+R5+R6. (Fig.9.2.50) Metal Bus resistance of ESD snapback NMOS (nch_HIA18) to "IO (1.8V) or cascaded (3.3V)" power clamp R3' +R5+R6 ≤ 0.3 ohm. (Fig.9.2.51) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.3g ^U	Metal resistance of Rbd/Rbs from Power and Ground bump to core (0.75V) power clamp. (Fig. 9.2.52) No needed to take "R0" into account. (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.4g ^U	Metal resistance of Rbd/Rbs from Power and Ground bump to IO (1.8V) power clamp. (Fig. 9.2.52) No needed to take "R0" into account. (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.5g ^U	Metal resistance of Rbd/Rbs from Power and Ground bump to cascaded (3.3V) power clamp. (Fig. 9.2.52) No needed to take "R0" into account. (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.7g ^U	Max. resistance (Rvdd1+Rvdd2/Rvss1+Rvss2) of metal bus from IO (1.8V) Power clamp to the closest power clamp. (Fig.9.2.53) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.7.1.1g ^U	Max. resistance (Rvdd1+Rvdd2/Rvss1+Rvss2) of metal bus from core (0.75V) Power clamp to the closest power clamp on power net. (Fig.9.2.53) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.7.1.2g ^U	Max. resistance (Rvdd1+Rvdd2/Rvss1+Rvss2) of metal bus from core (0.75V) Power clamp to the closest power clamp on ground net. (Fig.9.2.53) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2
ESD.CDM.P.7.2g ^U	Max. resistance (Rvdd1+Rvdd2/Rvss1+Rvss2) of metal bus from cascaded (3.3V) Power clamp to the closest power clamp. (Fig.9.2.53) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.2

Rule No.	Description	Label	Op.	Rule
ESD.CDM.P.7.3g ^U	Max. resistance ($R_{vdd1}+R_{vdd2}/R_{vss1}+R_{vss2}$) of metal bus from IO (1.8V) Power clamp to the closest cascoded (3.3V) power clamp. (Fig.9.2.53) (ESD Rbus resistance requirements are changed with target CDM level.)		\leq	Table 9.2.7.3.2
ESD.CDM.P.7.4g ^U	Max. resistance ($R_{vdd1}+R_{vdd2}/R_{vss1}+R_{vss2}$) of metal bus from IO (1.8V) Power clamp to the closest core power clamp. (Fig.9.2.53) (ESD Rbus resistance requirements are changed with target CDM level.)		\leq	Table 9.2.7.3.2
ESD.CDM.P.7.5g ^U	Max. resistance ($R_{vdd1}+R_{vdd2}/R_{vss1}+R_{vss2}$) of metal bus from core Power clamp to the closest cascoded (3.3V) power clamp. (Fig.9.2.53) (ESD Rbus resistance requirements are changed with target CDM level.)		\leq	Table 9.2.7.3.2
ESD.CDM.P.8g ^U	Max. resistance of metal bus from back-to-back (B2B) diode to closest Ground bump of both ground domain. (Fig.9.2.54) (ESD Rbus resistance requirements are changed with target CDM level.)		\leq	Table 9.2.7.3.2
ESD.CDM.P.9g ^U	Metal Bus resistance of back-to-back (B2B) diode to closest power clamp of both ground domain. (Fig.9.2.55) (ESD Rbus resistance requirements are changed with target CDM level.)		\leq	Table 9.2.7.3.2
ESD.CDM.P.10g ^U	Metal Bus resistance of guard rings for internal circuits ESD isolation purpose. Guard rings definitions are illustrated in ESD.CDM.1g ^U , ESD.CDM.1.1g ^U , ESD.CDM.2g ^U . N+ guard ring for separated NW PMOS in ESD.CDM.1g ^U and ESD.CDM.1.1g ^U are exempted from this rule check.		\leq	10
ESD.XDM.P.1g ^U	Metal Bus resistance of back-to-back (B2B) diode to local power clamp of cross domain interface on both of ground nets. (Fig.9.2.56) (ESD Rbus resistance requirements are changed with target CDM level.)		\leq	Table 9.2.7.3.2

Table 9.2.7.3.2 ESD Rbus requirement

	CDM 5A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)	CDM 14A (FWHM < 1ns)
ESD.CDM.P.1g ^U (Ω)	0.1	0.07	0.05	0.03
ESD.CDM.P.1.1g ^U (Ω)	1	0.7	0.5	0.3
ESD.CDM.P.2g ^U (Ω)	0.3	0.2	0.15	0.1
ESD.CDM.P.3g ^U (Ω)	0.1	0.07	0.05	0.05
ESD.CDM.P.4g ^U (Ω)	0.4	0.3	0.2	0.2
ESD.CDM.P.5g ^U (Ω)	0.4	0.3	0.2	0.2
ESD.CDM.P.7g ^U (Ω)	4	3	2	1
ESD.CDM.P.7.1.1g ^U (Ω)	1	1	1	1
ESD.CDM.P.7.1.2g ^U (Ω)	1	0.7	0.5	0.5
ESD.CDM.P.7.2g ^U (Ω)	4	3	2	1
ESD.CDM.P.7.3g ^U (Ω)	4	3	2	1
ESD.CDM.P.7.4g ^U (Ω)	4	3	2	1
ESD.CDM.P.7.5g ^U (Ω)	1	0.7	0.5	0.5
ESD.CDM.P.8g ^U (Ω)	0.3	0.2	0.15	0.1
ESD.CDM.P.9g ^U (Ω)	0.3	0.2	0.15	0.1
ESD.CDM.P.10g ^U (Ω)	10	10	10	10
ESD.XDM.P.1g ^U (Ω)	--	0.2	0.15	0.1

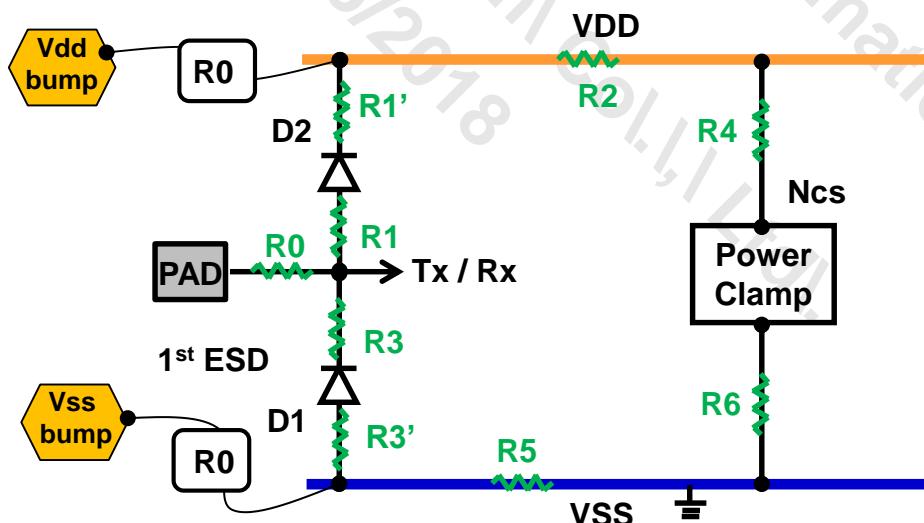


Figure 9.2.50 Primary ESD (dual diode) Rbus network scheme

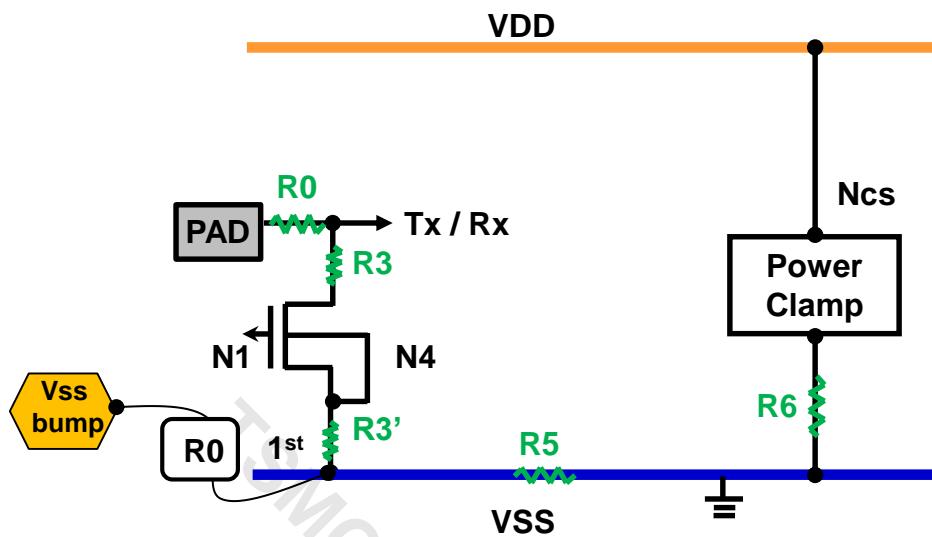


Figure 9.2.51 Primary ESD (snapback) Rbus network scheme

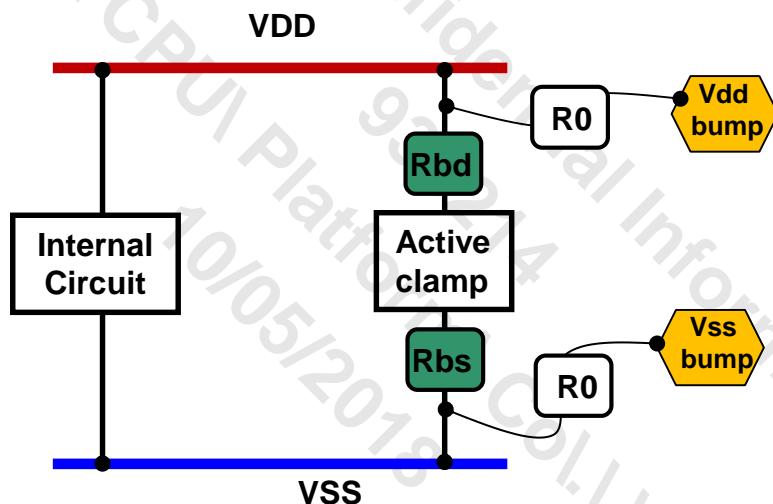


Figure 9.2.52 Metal bus resistance between power/ground bump to power clamp

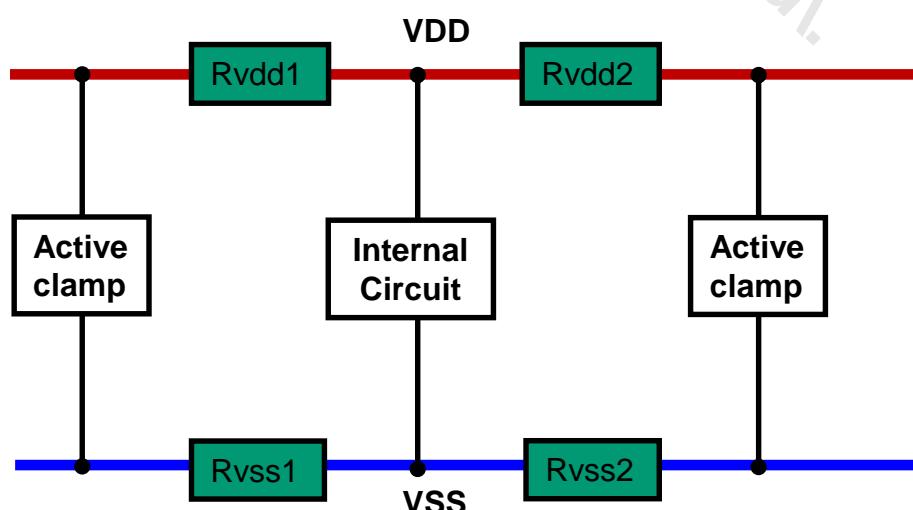


Figure 9.2.53 Metal bus resistance between power clamp to the closest power clamp

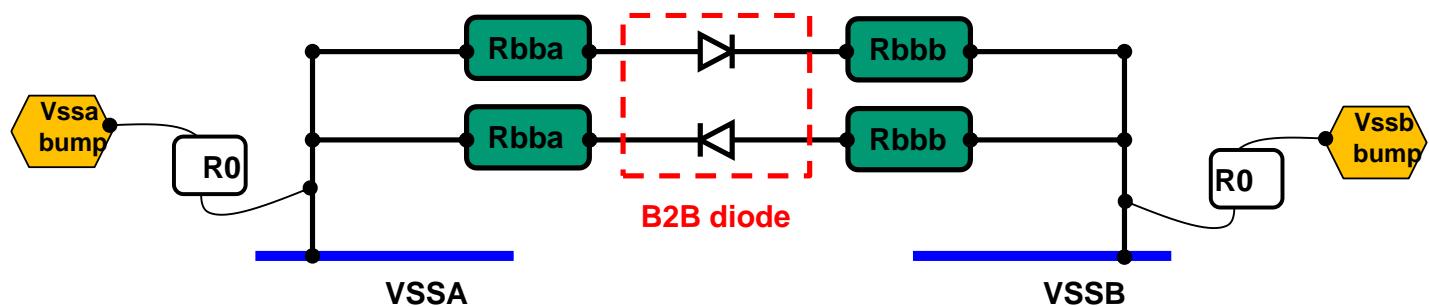


Figure 9.2.54 Metal bus resistance between back-to-back (B2B) diode to the closest ground bump of both ground domain

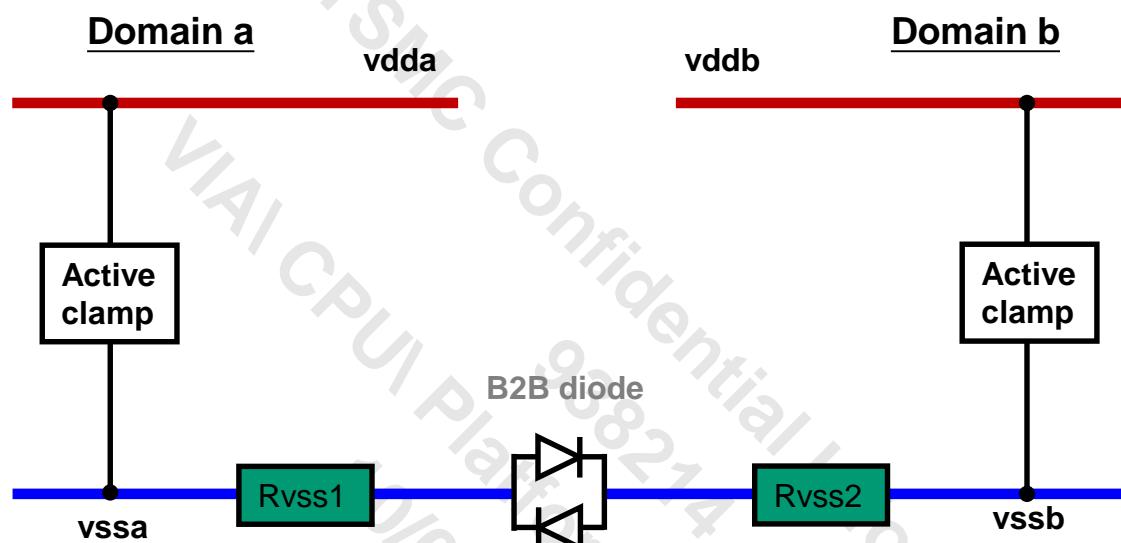


Figure 9.2.55 Metal bus resistance between back-to-back (B2B) diode to the closest power clamp of both ground domain

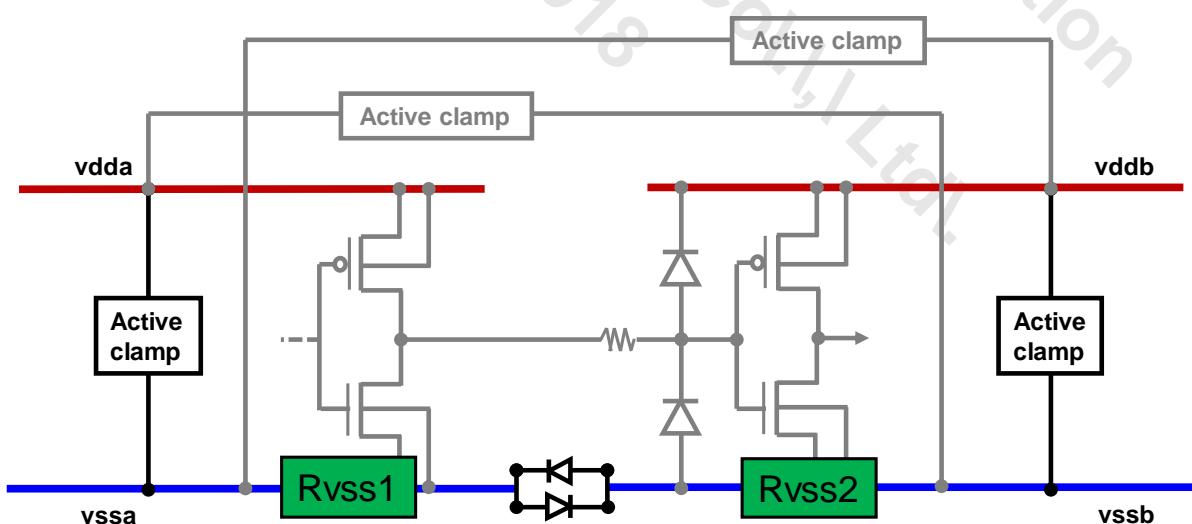


Figure 9.2.56 Metal bus resistance between back-to-back (B2B) diode to the local power clamp of cross domain interface

Resistance rules for distributed power clamp ESD protection network:

Rule No.	Description	Label	Op.	Rule
ESD.DISTP2P.1g ^U	ESD discharging path resistance of ESD dual diode to power/ground bump through core power clamp $\{(R21+Rpc1+R61)/(R22+Rpc2+R62)\},$ $\{(R51+Rpc1+R41)/(R52+Rpc2+R42)\},$ ESD discharging path resistance = Metal bus resistance + power clamp conduction resistance. (Fig.9.2.61) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.3
ESD.DISTP2P.1.1g ^U	ESD discharging path resistance of ESD dual diode to power/ground bump through IO (1.8V) power clamp $\{(R21+Rpc1+R61)/(R22+Rpc2+R62)\},$ $\{(R51+Rpc1+R41)/(R52+Rpc2+R42)\},$ ESD discharging path resistance = Metal bus resistance + power clamp conduction resistance. (Fig.9.2.61) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.3
ESD.DISTP2P.1.2g ^U	ESD discharging path resistance of Low-Cap ESD dual diode to power/ground bump through core power clamp $\{(R21+Rpc1+R61)/(R22+Rpc2+R62)\},$ $\{(R51+Rpc1+R41)/(R52+Rpc2+R42)\},$ ESD discharging path resistance = Metal bus resistance + power clamp conduction resistance. (Fig.9.2.61) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.3
ESD.DISTP2P.1.3g ^U	ESD discharging path resistance of Low-Cap ESD dual diode to power/ground bump through IO (1.8V) power clamp $\{(R21+Rpc1+R61)/(R22+Rpc2+R62)\},$ $\{(R51+Rpc1+R41)/(R52+Rpc2+R42)\},$ ESD discharging path resistance = Metal bus resistance + power clamp conduction resistance. (Fig.9.2.61) (ESD Rbus resistance requirements are changed with target CDM level.)		≤	Table 9.2.7.3.3

Table 9.2.7.3.3 ESD effective discharging resistance requirement

	CDM 5A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)	CDM 14A (FWHM < 1ns)
ESD.DISTP2P.1g ^U (Ω)	0.8	0.52	0.38	0.27
ESD.DISTP2P.1.1g ^U (Ω)	1.3	0.92	0.69	0.54
ESD.DISTP2P.1.2g ^U (Ω)	0.6	0.42	0.33	0.20
ESD.DISTP2P.1.3g ^U (Ω)	1.1	0.82	0.64	0.47

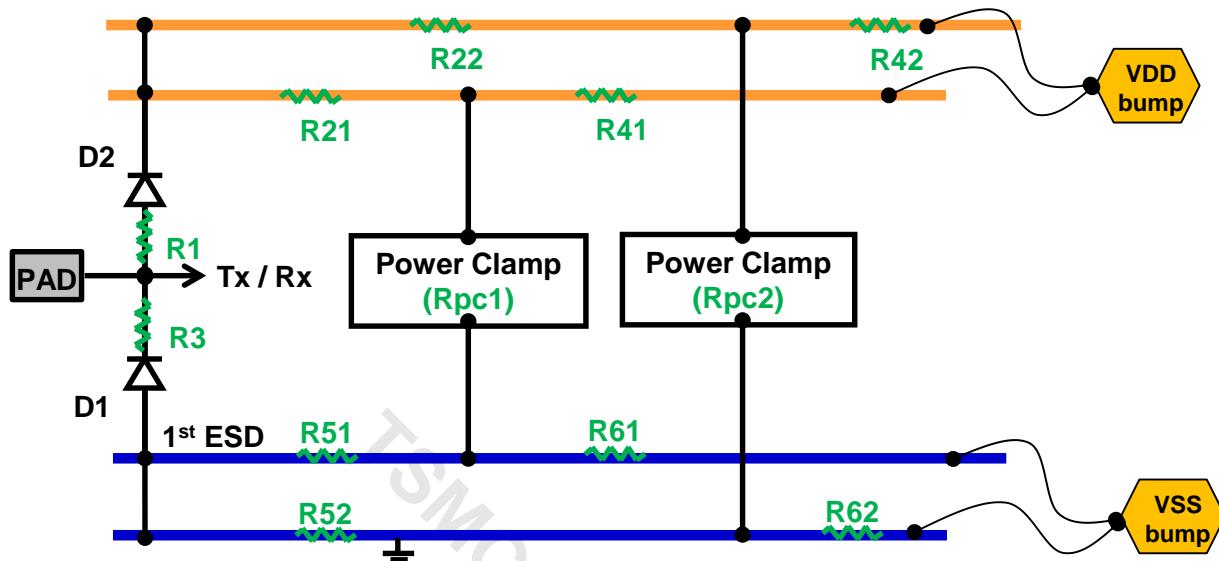


Figure 9.2.61 ESD discharging path resistance of ESD diode to power/ground bump through power clamp

9.2.7.4 HD MIM ESD Protection Design Guidelines

- Resistance of the bus line from the clamp cell to the HD MIM circuitry (R_{vdd}/R_{vss}) needs to be $< 1 \text{ ohm}$.
- If the HD MIM is between VDD and VSS, the max resistance from the power bump (VDD)/ground bump (VSS) to the clamp cell (R_{bd}/R_{bs}) is 0.1 ohm for core voltage power clamp, and 0.4 ohm for IO voltage power clamp for CDM peak current 5A target.
- The metal rails connecting from VDD and VSS bumps to the power clamp must be wide enough and meet ESD backend current density requirement.
- ESD R_{bus} resistance and ESD backend current density requirements are changed with target CDM level. For details, please refer to ESD.CDM.P.3g ~ ESD.CDM.P.5g group and ESD.CD.1g group.

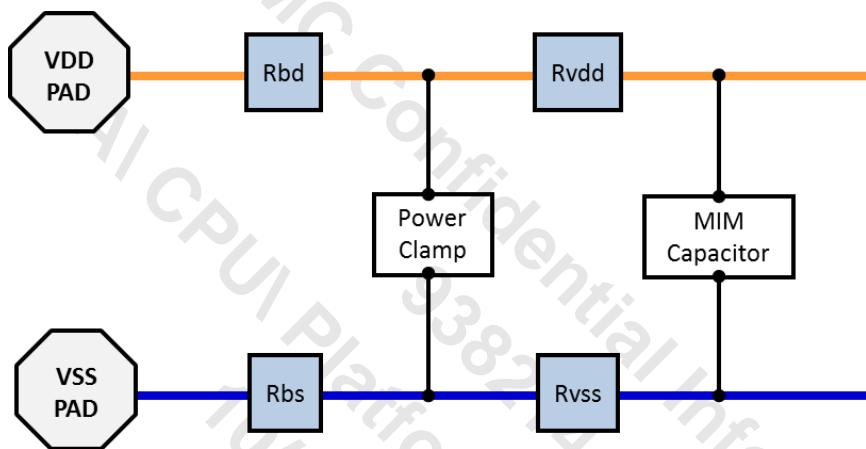


Figure 9.2.70 Power clamp placement and bus resistance requirement for HD MIM capacitor

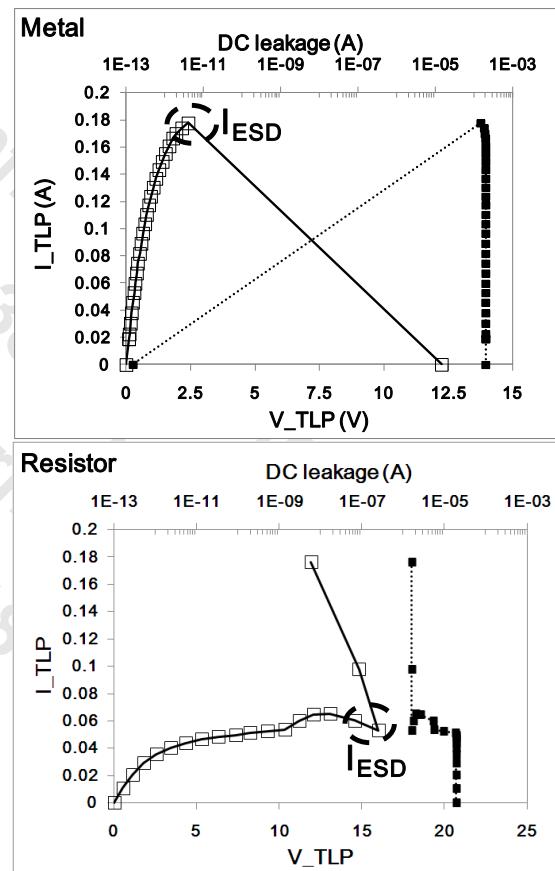
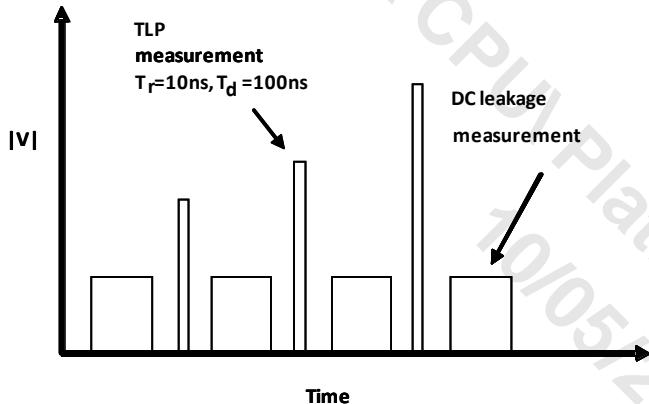
9.3 ESD Back-End Reliability Guideline

Typically the design purpose within a dedicated ESD protection device is that interconnect will not be the limitation for the ESD robustness. This section provides information to evaluate the max. Current density (CD) of metal line, via, M0, and resistor under ESD stress condition. According to the ESD back-end reliability rule, the customer can optimize their layout and get better ESD performance.

9.3.1 Test Methodology

The TLP is used to extract the maximum ESD current density (CD). The pulse width and rise time of TLP are 100ns and 10ns, respectively, to simulate the HBM waveform.

The I_{t_2} can be extracted by TLP. As below figure shown, the I_{t_2} of Metal is about 0.18A and that of Resistor is 0.06A.



9.3.2 Failure Mechanism

The measurement is performed by TLP ($T_d=100\text{ns}$, $T_r=10\text{ns}$) under 25°C using wafer-level probing. The I_{ESD} means the suggested ESD TLP current density (CD) value.

1. For High R resistor, the Resistance will degrade after ESD stress if $I_{ESD} > I_{t_2}$.
The resistance of the resistor will degrade if it goes to snapback after ESD stress. The I_{ESD} is defined as the maximum current before snapback.
2. For M0, via, and metal, the TLP current density (CD) has chance of degradation after ESD stress if $I_{ESD} > 0.5 * I_{t_2}$.

The M0/via/metal ESD failure have the form of an open connection, the change of the sheet resistance, the degradation of electromigration lifetime. The TLP current density (I_{ESD}) is defined as the half of maximum current before open connection.

9.3.3 Maximum ESD Current Density for Resistor

Resistor TLP CD	TLP ($T_r=10\text{ns}$; $T_d=100\text{ns}$)	Specification $I_{ESD}>1.3\text{A}$ (ESD.CD.1g)	Specification $I_{ESD}>12\text{mA}$ (ESD.CD.2g)	Note
	I_{ESD} (Normalized by width)	Suggested resistor width	Suggested resistor width	
High R resistor (rhim)	6.5 mA/ μm	n.a.	1.85 μm	$I_{ESD}=I_{t_2}$

9.3.4 Maximum ESD current density for M0, Via, and Metal

Below table shows the I_{ESD} of via, and Metal and suggested metal width and via number for HBM 2KV specification.

Metal TLP CD	TLP (Tr=10ns; Td=100ns)	Specification $I_{ESD} > 1.3A$ (ESD.CD.1g)	Specification $I_{ESD} > 12mA$ (ESD.CD.2g)	Note
	I_{ESD} (Normalized by width) (mA/um)	Suggested metal width (um)	Suggested metal width (um)	
M0	36.5	35.7	0.330	$I_{ESD} = 0.5 * I_{t2}$
M1	32.3	40.3	0.372	
Mxs	36.5	35.7	0.330	
Mx	36.5	35.7	0.330	
Mxa	36.5	35.7	0.330	
Mya	48.5	26.8	0.248	
My	52.3	24.9	0.230	
Myy	100.0	13.0	0.120	
Myx	150.0	8.7	0.080	
Myz	279.0	4.7	0.044	
Mz	466.0	2.8	0.026	
Mr	656.0	2.0	0.019	
Mu	1743.0	0.8	0.007	
AP	734.0	1.8	0.017	

VIA TLP CD	Via dimension	TLP (Tr=10ns; Td=100ns)		Specification $I_{ESD} > 1.3A$ (ESD.CD.1g)	Specification $I_{ESD} > 12mA$ (ESD.CD.2g)	Note
	Area (W*L) (um ²)	I_{ESD} (Normalized by area)	I_{ESD} (Normalized by via number)	Suggested via number	Suggested via number	
VC	0.02*0.04	4500 mA/um ²	3.6 mA/via	362	4	$I_{ESD} = 0.5 * I_{t2}$
VIA0	0.02*0.02	4500 mA/um ²	1.8 mA/via	723	7	
VIAxs	0.02*0.02	5750 mA/um ²	2.3 mA/via	566	6	
VIAx	0.02*0.02	5750 mA/um ²	2.3 mA/via	566	6	
VIAxa	0.02*0.02	5750 mA/um ²	2.3 mA/via	566	6	
VIAya	0.02*0.02	5750 mA/um ²	2.3 mA/via	566	6	
VIAy	0.038*0.038	3310.2 mA/um ²	4.78 mA/via	272	3	
VIAyy	0.062*0.062	1378.8 mA/um ²	5.3 mA/via	246	3	
VIAyx	0.126*0.126	1050 mA/um ²	16.67 mA/via	78	1	
VIAyz	0.18*0.18	978.4 mA/um ²	31.7 mA/via	42	1	
VIAz	0.324*0.324	1051.7 mA/um ²	110.4 mA/via	12	1	
VIAr	0.414*0.414	1022.8 mA/um ²	175.3 mA/via	8	1	
VIAu	0.324*0.324	729.7 mA/um ²	76.6 mA/via	17	1	
RV	2.7*2.7	0.2 A/um ²	1146 mA/via	2	1	

Below table shows the I_{ESD} of M1/Mx/Mxa/Mya with length/width effect for HBM 2KV specification. For specific length and width, the CD rules can be relaxed. Metal Length is the direction parallel to current direction, and metal width is the direction perpendicular to current direction. The IESD can be further increase by smaller width and length. The detailed results are shown in below table.

N7+ ESD Backend	Metal Length (um)	Unit Metal Width (um)	TLP (Tr=10ns; Td=100ns)		Specification $I_{ESD} > 1.3A$	Note
			factor (predicted)	I_{ESD} (Normalized by width) (mA/um)		
M0/Mxs/Mx/Mxa	$L \leq 0.5$	$W \leq 0.2$	$1.44*1.6$	84.0	15.5	$I_{ESD} = 0.5*It_2$
		$0.2 < W \leq 0.5$	$1.44*1.3$	68.2	19.0	
		$0.5 < W$	1.44	52.5	24.8	
	$0.5 < L \leq 1$	$W \leq 0.2$	$1.3*1.6$	75.8	17.1	
		$0.2 < W \leq 0.5$	$1.3*1.3$	61.6	21.1	
		$0.5 < W$	1.3	47.4	27.4	
	$1 < L$	$W \leq 0.2$	1.6	58.3	22.3	
		$0.2 < W \leq 0.5$	1.3	47.4	27.4	
		$0.5 < W$	1	36.5	35.7	
M1	$L \leq 0.5$	$W \leq 0.2$	$1.44*1.6$	74.4	17.5	$I_{ESD} = 0.5*It_2$
		$0.2 < W \leq 0.5$	$1.44*1.3$	60.5	21.5	
		$0.5 < W$	1.44	46.5	27.9	
	$0.5 < L \leq 1$	$W \leq 0.2$	$1.3*1.6$	67.2	19.3	
		$0.2 < W \leq 0.5$	$1.3*1.3$	54.6	23.8	
		$0.5 < W$	1.3	42.0	31.0	
	$1 < L$	$W \leq 0.2$	1.6	51.7	25.2	
		$0.2 < W \leq 0.5$	1.3	42.0	31.0	
		$0.5 < W$	1	32.3	40.3	
Mya	$L \leq 0.5$	$W \leq 0.2$	$1.44*1.6$	111.8	11.6	$I_{ESD} = 0.5*It_2$
		$0.2 < W \leq 0.5$	$1.44*1.3$	90.9	14.3	
		$0.5 < W$	1.44	69.9	18.6	
	$0.5 < L \leq 1$	$W \leq 0.2$	$1.3*1.6$	100.9	12.9	
		$0.2 < W \leq 0.5$	$1.3*1.3$	82.0	15.8	
		$0.5 < W$	1.3	63.1	20.6	
	$1 < L$	$W \leq 0.2$	1.6	77.7	16.7	
		$0.2 < W \leq 0.5$	1.3	63.1	20.6	
		$0.5 < W$	1	48.5	26.8	

Below table shows the I_{ESD} of via, and Metal and suggested metal width and via number for CDM 5A ($FWHM < 1n\ sec$) specification.

Metal TLP CD	vfTLP (Tr=0.2ns; Td=1ns)	Specification $I_{ESD} > 5A$	Specification $I_{ESD} > 46mA$	Note
	I_{ESD} (Normalized by width) (mA/um)	Suggested metal width (um)	Suggested metal width (um)	
M0	151.9	35.7	0.330	$I_{ESD} = 0.5 * I_{t2}$
M1	134.6	40.3	0.372	
Mxs	151.9	35.7	0.330	
Mx	151.9	35.7	0.330	
Mxa	151.9	35.7	0.330	
Mya	202.2	26.8	0.248	
My	217.7	24.9	0.230	
Myy	416.7	13.0	0.120	
Myx	625.0	8.7	0.080	
Myz	1162.5	4.7	0.044	
Mz	1941.7	2.8	0.026	
Mr	2733.3	2.0	0.019	
Mu	7262.5	0.8	0.007	
AP	3058.3	1.8	0.017	

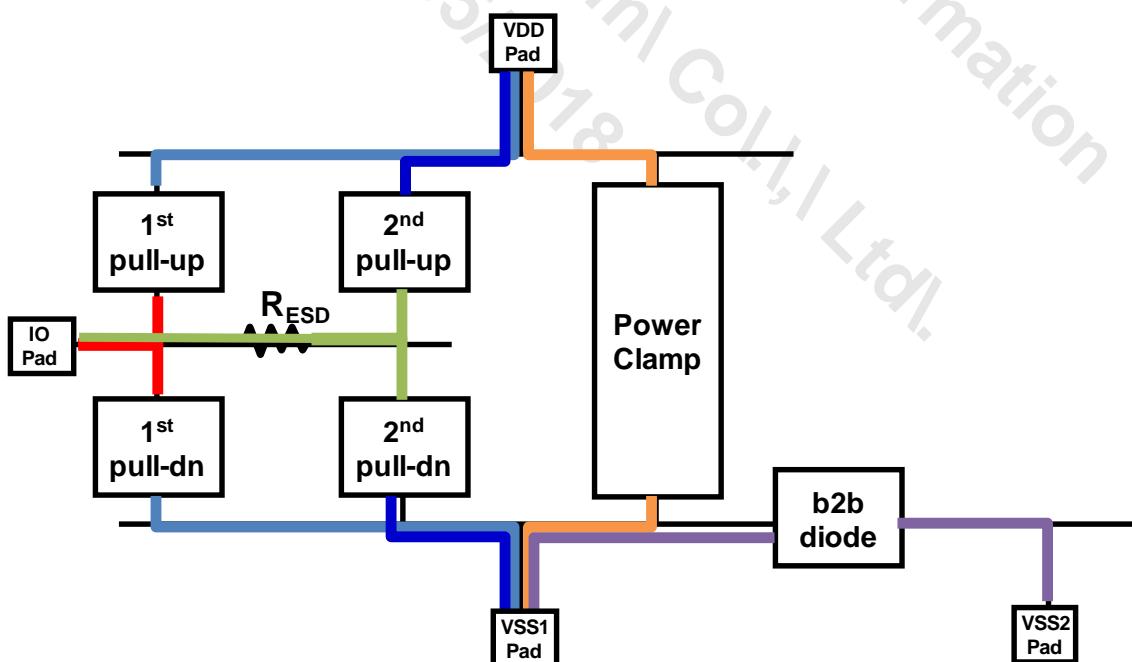
VIA TLP CD	Via dimension	vfTLP (Tr=0.2ns; Td=1ns)		Specification $I_{ESD} > 5A$	Specification $I_{ESD} > 46mA$	Note
	Area ($W*L$) (um 2)	I_{ESD} (Normalized by area)	I_{ESD} (Normalized by via number)	Suggested via number	Suggested via number	
VC	0.02*0.04	17.25 A/um 2	13.8 mA/via	362	4	$I_{ESD} = 0.5 * I_{t2}$
VIA0	0.02*0.02	17.25 A/um 2	6.9 mA/via	723	7	
VIAxs	0.02*0.02	22 A/um 2	8.8 mA/via	566	6	
VIAx	0.02*0.02	22 A/um 2	8.8 mA/via	566	6	
VIAxa	0.02*0.02	22 A/um 2	8.8 mA/via	566	6	
VIAya	0.02*0.02	22 A/um 2	8.8 mA/via	566	6	
VIAy	0.038*0.038	12.74 A/um 2	18.4 mA/via	272	3	
VIAyy	0.062*0.062	5.31 A/um 2	20.4 mA/via	246	3	
VIAyx	0.126*0.126	3.63 A/um 2	57.7 mA/via	78	1	
VIAyz	0.18*0.18	3.76 A/um 2	121.9 mA/via	42	1	
VIAz	0.324*0.324	4.04 A/um 2	424.6 mA/via	12	1	
VIAr	0.414*0.414	3.93 A/um 2	674.2 mA/via	8	1	
VIAu	0.324*0.324	2.81 A/um 2	294.6 mA/via	17	1	
RV	2.7*2.7	0.60 A/um 2	4407.7 mA/via	2	1	

9.3.5 Minimum ESD Current for ESD device

Rule No.	Description	Label	Op.	Rule
ESD.CD.1g ^U	<p>Suggested minimum ESD current (unit: A, IESD) for the primary ESD discharge path. Primary ESD devices include dual-diode, drain-ballasted NMOS, drain-ballasted cascoded NMOS, power clamp and back to back (b2b) diode Primary ESD discharge current path includes:</p> <ol style="list-style-type: none"> 1. Metal line width connecting the “bond pad” and the primary ESD device. 2. The Via number in the primary ESD device. 		≥	Table 9.3.5.1
ESD.CD.2g ^U	<p>Suggested minimum ESD current (Unit: A, IESD) for the secondary ESD discharge path. Secondary ESD devices include ESD resistor, diode based and MOS based secondary protection. Secondary ESD discharge current path includes:</p> <ol style="list-style-type: none"> 1. Metal line width connecting the “bond pad” and the secondary ESD device. 2. The Via number in the secondary ESD device 		≥	Table 9.3.5.1

Table 9.3.5.1 ESD Current density requirement

	CDM 5A (FWHM < 1ns)	CDM 7A (FWHM < 1ns)	CDM 9A (FWHM < 1ns)	CDM 14A (FWHM < 1ns)
ESD.CD.1g ^U (A)	1.3	1.8	2.4	3.5
ESD.CD.2g ^U (A)	0.012	0.02	0.025	0.035



9.3.6 Min. metal width to meet ESD specification

TSMC's N7+ ESD specification is 2KV for Human Body Model (HBM). The suggested I_{ESD} is 1.3A from TLP measurement result. Below show some examples for metal width calculation.

Example

As M1 and M2 is "Mx" type metal

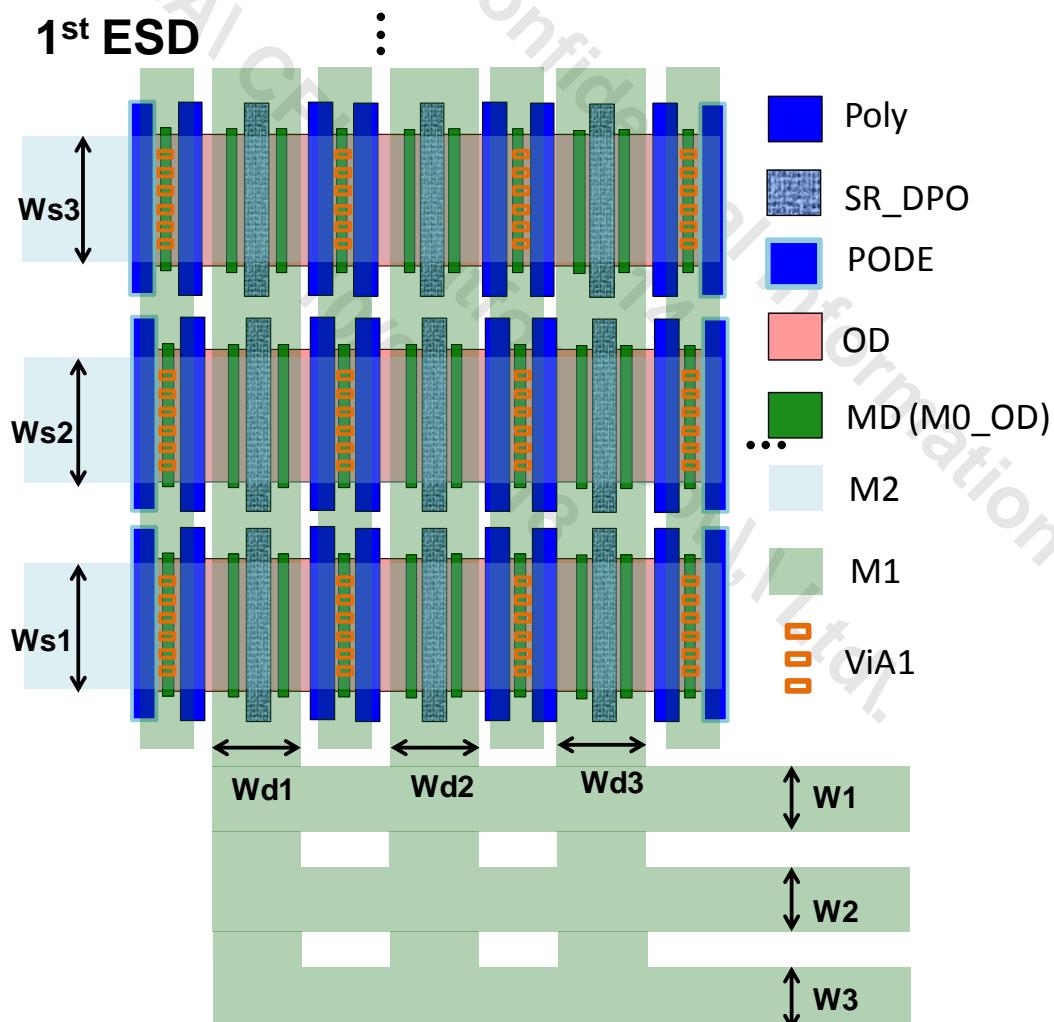
and ViA1 is Viax type

$(W1+W2+W3)*(Mx\ CD\ value) \geq 1.3A$

$(Ws1+Ws2+Ws3)*(Mx\ CD\ value) \geq 1.3A$

$(Wd1+Wd2+Wd3)*(Mx\ CD\ value) \geq 1.3A$

$ViA1\ number*(Viax\ CD\ value) \geq 1.3A$



9.4 Tips for the ESD/Latchup Design

9.4.1 Tips for General Latchup Design

To enhance Latchup immunity, the following guidelines are recommended.

1) Solid guard ring/STRAP connection:

All the guard rings and STRAPS should be connected to VDD/VSS directly with very low parasitic resistance. Use as many MD and VIAs as possible.

2) Large-size capacitor displacement current induced LUP:

A P+ guard-ring should separate a large capacitor and MOS to avoid displacement current induce latch-up. The p+ guard ring width should be enlarger than 0.1 μm.

3) Potential Latchup concern from OD/NW resistor:

If OD/NW resistor is connected to an I/O PAD, this OD/NW resistor may potentially inject substrate current through its parasitic diode or parasitic BJT during LUP over-current tests. Potential latchup issue may exists if this OD/NW resistor is nearby parasitic pnpn (SCR).

9.4.2 Tips for General ESD Design

To enhance ESD immunity, the following guidelines are recommended.

1) Complete ESD protection coverage:

Any Drain/Source/Gate of a transistor connected to a pad should have ESD protection.

2) Solid back-end in the entire ESD discharge path:

MD and VIAs should be as many as possible in all ESD devices and current paths, including the diode and metal connection.

3) Robust victim design with use of drain-ballasted NMOS:

When using drain-ballasted NMOS as I/O ESD protection device, the gate length of post driver should be larger than the gate length of drain-ballasted NMOS.

4) Pass-gate exists between PAD and internal block:

If a pass-gate (IO device) is added between a PAD and core device, take care if the ESD protection device can effectively protect the core device. It is not allowed to use IO device to protect the core device (as shown in below figure). If the pass gate device (I/O device) covered with SDI layer, the DRC will be triggered to check ESD.1g.

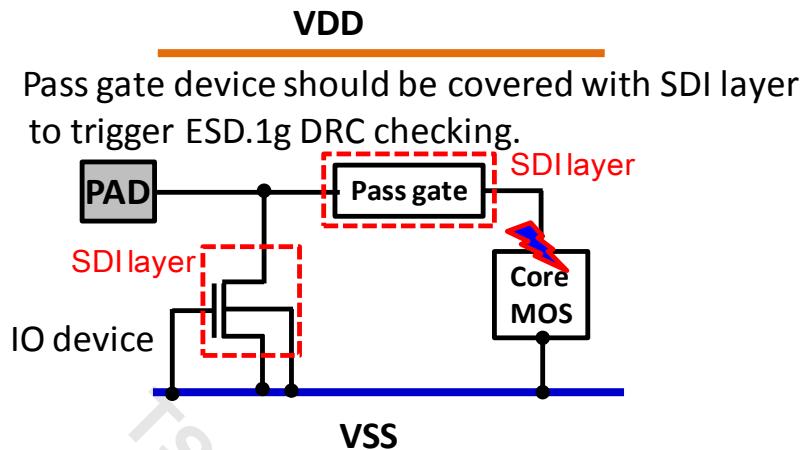


Figure 9.4.2.1

5) Potential ESD concern from OD/NW resistor:

The OD resistor can potentially trigger its parasitic diode /BJT, leading to ESD failure during ESD stress. To reduce this ESD vulnerability:.

- For P+ OD resistor, adopt floating NW design when possible.
- For N+ OD resistor, enclose hot side (connected to I/O PAD) with NW when possible.
- Surround OD/NW resistor with double guard rings. Avoid local high field and current crowding during ESD by layout optimization.
- Have robust ESD network design with low turn-on voltage and low clamping voltage. The aim is to avoid parasitic device turn-on.

9.4.3 Tips for Power-Ground ESD Protection

To avoid ESD damage to internal circuits, it's critical to arrange robust whole chip ESD protection design. Special care should be paid to the digital and analog circuits. In the mixed-mode ICs, separate digital and analog powers are used, and the interface devices between the digital and analog circuits are particularly sensitive to ESD damage. Below are some guidelines for robust power-ground design,

1) Power protection for each Vdd/Vss domain:

Each set of VDD and VSS must have its own power clamp cells to provide direct discharge path between VDD and VSS. The number of power clamp cells should be as many as allowed.

2) Inter-domain power protection design:

Cross-couple power clamps between each power/ground combination are necessary. This includes Vdd(x) to Vss(y) and Vdd(x) to Vdd(y). The x and y denote different power supply combination.

3) Recommended power protection design:

The recommended power ESD protection cell is gate-driven NMOS.

4) Recommended power protection design:

Implement largest total channel width allowed for better ESD immunity. TSMC design rule only represent a bare minimum requirement on size.

5) Evenly distributed power protection design:

Use at least one clamping and/or conduction cell for every 1.0Ω of power line resistance.

6) Power bus design:

Power lines should keep ultra low resistance and avoid disconnection. For different powers or grounds with the same potential, use bi-directional cell such as back to back diodes to link them together.

7) Latchup avoidance:

Each component of power clamp and back to back diode cells must be surrounded by double guard rings to avoid latch up events.

8) Active clamp trigger circuit design:

Avoid mis-trigger due to power noise or glitch by carefully designing the certain aspects in turn-on detector circuit, for example, the RC time constant and the junctions acting as minority collectors.

If the detector circuit is RC-inverter trigger circuit design, the ratio between inverter NMOS and PMOS should be carefully considered to prevent any burn-out issue during reliability (such as burn-in) test period.

9) Robust body diode/parasitic diode design:

Guard rings directly connected to VDD or VSS power pad should be as wide as possible, to avoid silicon burn out on parasitic junction diode during ESD events.

10) Cross domain interface design:

Secondary ESD protection with resistor is necessary for cross domain with core gate oxide interface (without footer/header) in separated ground scenario. For common ground case, total metal routing area of cross domain interface should be less than 32um² or secondary ESD protection with resistor is required. For CDM peak current higher than 9A, the area should be less than 16um².

9.5 ESD test methodology

9.5.1 Stress condition and Measurement condition

The ESD test items include HBM which needs to meet JEDEC standards. The rise time and decay time of HBM are within 10ns and 150ns, respectively. The specification for HBM is 2KV. The peak currents of 2KV HBM is 1.2A-1.48A.

The ESD test is performed at room temperature. The sample size for ESD test is three devices and each device are stressed one time at each voltage level. The DC parametric and functional testing at room temperature is performed on all devices before ESD testing. The test devices need to meet device data sheet requirements and the DC parameters.

The pin zapping combinations depend on the number of power pin groups like VDD1, VDD2, VSS1, VSS2, GND, etc. Please refer to JEDEC standards.

9.5.2 Failure criteria

The DC parametric and functional testing of the device should be characterized after each voltage level to check the device ESD failure threshold. The device will be defined as a failure if, after exposure to ESD pulses, it no longer meets the device data sheet requirements using DC parameter and functional testing.

10 Reliability Rules

This chapter provides information about the following:

- 10.1 Terminology
- 10.2 Front-end process reliability rules and models
- 10.3 Back-end process reliability rules
- 10.4 Current density (EM) specifications

The information in this chapter is to help customers meet their product application needs and their design-in reliability goals. The following sections include descriptions about gate oxide integrity, hot carrier effect injection (HCI), PMOS negative bias temperature instability (NBTI), NMOS positive bias temperature instability (PBTI), Electromigration (EM), Low-k Dielectric Integrity and Stress-migration (SM) specifications.

10.1 Terminology

This section provides definitions for key terms that are included in this chapter.

Table 10.1.1

Term	Definition
MTTF	The lifetime in which 50% of the population has failed
0.1% cumulative failure	The lifetime in which 0.1% of the population has failed

10.2 Front-End Process Reliability Rules and Models

This section provides information about overdrive voltage, gate oxide integrity, HCI degradation, and negative bias temperature instability.

10.3 Back-End Process Reliability Rules

10.3.1 Guidelines for Stress Migration(SM)

The Cu vias are frequently subjected to significant stress. The stress frequently causes voids, commonly referred to stress migration (SM) or stress-induced voids (SIV).

10.3.1.1 Failure Mechanism

The stress result from the different coefficient of thermal expansion (CTE) between Cu and the surrounding material will drive micro-vacancy in Cu to diffuse and agglomerate through interfacial surface and grain boundary. Eventually the stress-induced voids may significantly affect the electrical characteristics and may cause the semiconductor structure to fail.

10.3.1.2 Test Methodology

10.3.1.2.1 Measurement Condition

The measurement is performed under 25°C using wafer-level probing after oven bake. The baking temperature ranges between 125°C and 250°C.

10.3.1.2.2 Failure Criteria

A DUT is considered as failed if 10% resistance increase is reached.

10.3.1.3 SM design rule

Please refer to below rule codes of chapter 4.

VIA0.R.1, VIA0.R.2, VIA0.R.3

VIAx.R.1, VIAx.R.2, VIAx.R.2.1, VIAx.R.3

VIAxa.R.1, VIAxa.R.2, VIAxa.R.2.1, VIAxa.R.3

VIAya.R.1, VIAya.R.2, VIAya.R.2.1, VIAya.R.3, VIAya.R.4, VIAya.R.5, VIAya.R.6, VIAya.R.6.1

Mya.W.5, Mya.L.6, Mya.L.6.1, and Mya.L.6.2

VIAy.R.1, VIAy.R.2, VIAy.R.2.1, VIAy.R.3, VIAy.R.4, VIAy.R.5, VIAy.R.6, VIAy.R.8

My.W.5, My.L.6, My.L.6.1, and My.L.6.2

VIAyy.R.1, VIAyy.R.2, VIAyy.R.3, VIAyy.R.4, VIAyy.R.5, VIAyy.R.6, VIAyy.R.11

VIAyx.R.2, VIAyx.R.3, VIAyx.R.4, VIAyx.R.5, VIAyx.R.6, VIAyx.R.11

VIAyz.R.2, VIAyz.R.3, VIAyz.R.4, VIAyz.R.5, VIAyz.R.6,

VIAz.R.2, VIAz.R.3

VIAr.R.2, VIAr.R.3

10.3.2 Guidelines for Low-k Dielectric Integrity

This section provides information to help customers predict LK dielectric reliability and prevent a time dependent dielectric breakdown (TDDB). IMD TDDB is the breakdown of LK dielectric induced by a combination of operation voltage, temperature, and oxide thickness.

10.3.2.1 Low-k Dielectric Lifetime Prediction Model

$$TTF = A \times \exp(-\gamma^* E^{0.5}) \times \exp(Ea/kT)$$

TTF : Time to Failure

A: a constant, material dependence

γ : field acceleration factor

E: electric field

Ea: Thermal activation energy

k: Boltzmann's constant

T: temperature

10.3.2.2 Failure Mechanism

While a conduction path was formed during constant voltage stress in LK dielectric, it would result in LK dielectric breakdown.

The possible failure mechanisms of IMD-TDDB could be as followings.

1. Dielectric interface breakdown through ESL
2. Dielectric bulk breakdown through barrier

10.3.2.3 Test Methodology

10.3.2.3.1 Measurement Conditions

1. I_g is the leakage current between metal lines at $T=125^\circ C$ under E_s (constant electric field).

2. E_s is set to be $2 \sim 7 \text{ MV/cm}$.

10.3.2.3.2 Failure Criteria

A DUT was failed while $I_g(T_{bd}) > 100 * I_g(T_0)$.

10.3.2.3.3 Lifetime

Lifetime was predicted @ 0.1% Cum, 1.1Vcc, $125^\circ C$

10.3.2.4 Low-k dielectric integrity design rule

Please refer to below rule codes 4.5.46~4.5.63 in chapter 4.

10.4 Current Density (EM) Specifications

This section provides information to evaluate the quality of N7+ Cu process and to determine the EM lifetime of metal line, via, M0, AP RDL, RV and resistor under normal operation condition.

10.4.1 Electromigration Lifetime Prediction Model

$$TTF = A \times J^{-n} \times \exp(Ea/kT)$$

TTF : Time to Failure

A: a constant which contains a factor involving the cross-sectional area of the film

n: exponent of current density (n =1 for Cu process; n=2 for RDL process)

J: current density flowing in metal

Ea: activation energy (Ea =0.9~1.2eV for Cu process; Ea=0.7eV for RDL process)

k: Boltzmann's constant

T: temperature

10.4.2 Failure Mechanism

When a stress current is applied, Cu ions move from cathode to anode under electromigration, vacancy will generate at cathode and it will cause resistance increasing.

10.4.3 Failure Criteria

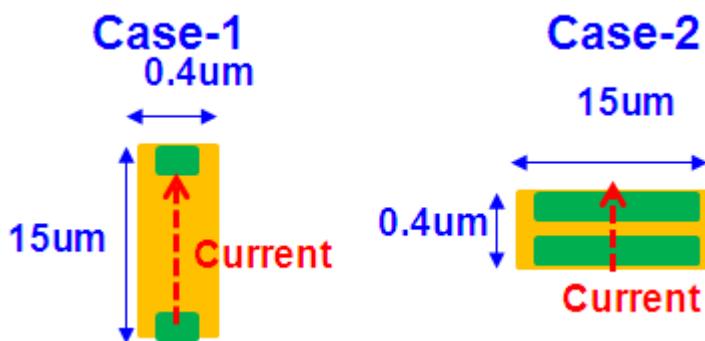
A DUT is considered as failed if 10% resistance increase is reached.

10.4.4 Length and Width Definition in EM Section

10.4.4.1 Length and Width Definition

Length of metal is the direction parallel to current direction, and width of metal is the direction perpendicular to current direction.

For example:



	Length	Width
Case-1	15um	0.4um
Case-2	0.4um	15um

10.4.4.2 M0/Mx/Mxa(Exclude M1 and Mxs) Effective Width for Color-B

The effective widths of M0/Mx/Mxa(Exclude M1 and Mxs) are different in Color-A (CA) and Color-B(CB) due to process bias in width. If Color-B drawn width (W_b) $\geq 0.04 \mu m$, effective width would be equal to drawn width plus bias width as below definitions and conditions in SIGNAL_RAL.

Definitions

W : drawn width

W_a : Color-A drawn width

W_b : Color-B drawn width

Conditions

For Color-A lines (CA), bias width=0, effective $W = W_a$

For Color-B lines (CB), if $W_b < 0.04$, bias width=0, effective $W = W_b$

For Color-B lines (CB), if $W_b \geq 0.04$ AND used for SIGNAL_RAIL, bias width=0.02, effective $W = W_b + 0.02$

For Color-B lines (CB), if $W_b \geq 0.04$ AND used for POWER_RAIL, bias width=0, effective $W = W_b$

10.4.5 Cu Wire Current Density (EM) Specifications ($T_j = 105^\circ\text{C}$)

10.4.5.1 Rating factor for Maximum DC Current

I_{\max} is the maximum DC current allowed for metal lines, vias, or contacts. I_{\max} is based on 0.1% point of measurement data at a 10% resistance increase after 10 years of continuous operation at 105°C . Use the following table to calculate I_{\max} if the junction temperature differs from 105°C .

Table 10.4.1

Temperature	100°C	105°C	110°C	115°C	120°C	125°C	130°C	135°C	140°C	145°C	150°C
Rating factor of VC I_{\max}	1.055	1.000	0.945	0.889	0.833	0.778	0.722	0.667	0.611	0.555	0.500
Rating factor of M0/V0/M1/Vx/Mx/Mxa/ Vxa/Mxs/Vxs I_{\max}	1.448	1.000	0.697	0.673	0.649	0.625	0.605	0.586	0.566	0.548	0.530
Rating factor of Mya/My/Myy/Myx/Myz/ Mz/Mr/Vya/Vy/Vyy/Vyx/ Vyz/Vz/Vr I_{\max}	1.448	1.000	0.697	0.491	0.349	0.250	0.180	0.131	0.096	0.071	0.053

For example, Mya I_{\max} (at 125°C) = $0.250 \times I_{\max}$ (at 105°C).

The rating factor is 1.448 for the case of temperature below 100°C for Joule heating effect consideration.

10.4.5.2 General for pure BEOL

The table provides the maximum allowed DC current, I_{max} for each of the metals and vias at junction temperature of 105°C. In the table, w (in μm) represents the drawn width of the metal line.

MiM VIAz/VIAr will follow same VIAz/VIAr EM rule.

Table 10.4.2

Metal Wiring Level / Interlevel connection	Via landing on Bottom Metal	I_{max} (mA) , effective W
M0		$1.5 \times 1.271 \times (w - 0.003)$
M1		$1.5 \times 1.068 \times (w - 0.003)$
Mx, Mxa, Mxs		$1.5 \times 1.184 \times (w - 0.003)$
Mya		$1.555 \times (w - 0.003)$
My		$2.102 \times (w - 0.004)$
Myy		$4.061 \times (w - 0.008)$
Myx		$4.976 \times (w - 0.02)$
Myz		$8.132 \times (w - 0.02)$
Mz		$14.811 \times (w - 0.02)$
Mr		$18.996 \times (w - 0.02)$
V0	Landing on M0	1.5×0.0403 per via
rectangular V0 ($0.02 \times 0.034 \mu\text{m}^2$)	Landing on M0	$1.5 \times 1.5 \times 0.0403$ per via
rectangular V0 ($0.02 \times 0.05 \mu\text{m}^2$ and $0.02 \times 0.06 \mu\text{m}^2$)	Landing on M0	$1.5 \times 2 \times 0.0403$ per via
V1, Vx, Vxa	Landing on M1/Mx/Mxs/Mxa	1.5×0.0403 per via
rectangular V1,Vx, Vxa ($0.02 \times 0.034 \mu\text{m}^2$)	Landing on M1/Mx/Mxs/Mxa	$1.5 \times 1.5 \times 0.0403$ per via
rectangular V1,Vx,Vxa ($0.02 \times 0.05 \mu\text{m}^2$)	Landing on M1/Mx//MxsMxa	$1.5 \times 2 \times 0.0403$ per via
Vx, Vxa (exclude V1) ($0.038 \times 0.038 \mu\text{m}^2$)	Landing on Mx/Mxs/Mxa	1.5×0.0829 per via
Vya	Landing on Mx/Mxs/Mxa	0.0529 per via
rectangular Vya	Landing on Mx/Mxs/Mxa	2×0.0529 per via
Vya ($0.038 \times 0.038 \mu\text{m}^2$)	Landing on Mx/Mxs/Mxa	0.1089 per via
Vy	Landing on My/Mya	0.143 per via
rectangular Vy	Landing on My/Mya	2×0.143 per via
Vy ($0.058 \times 0.058 \mu\text{m}^2$)	Landing on My/Mya	0.227 per via
Vyy	Landing on My/Myy	0.4386 per via
Vyx	Landing on Myy/Myx	0.5275 per via
Vyz	Landing on Myy/Myx/Myz	1.3012 per via
Vz	Landing on My	2.0726 per via
	Landing on Myy	3.9879 per via
	Landing on Myx	4.8267 per via
	Landing on Myz/Mz	5.0357 per via
Vr	Landing on My	2.6317 per via
	Landing on Myy	5.0356 per via
	Landing on Myx	6.1702 per via
	Landing on Mz/Mr	8.1683 per via

10.4.5.3 Stacked Vias

Stacked via can decompose to single via, and follows single via rule.

TSMC Confidential Information
938214
VIAI CPU Platform\ Col. I Ltd.
10/05/2018

10.4.5.4 Metal I_{max} dependence on metal length & width

For a metal line with a length of less than 3 μm (3 μm for M1/Mx/Mxa, and 4.5 μm for Myy/Mz/Mr), the I_{max} current limit can be further increased at least by a factor of 3. The detailed I_{max} specs for various metal lines are described in Table 10.4.3. In this table, w represents the drawn width of the metal line in μm , while L represents the length of the metal line in μm . The junction temperature for these specs is 105°C.

Table 10.4.3

Metal Wiring Level	Metal Length, L (μm)	Metal Width [drawn], W (μm)	I _{max} (mA) , effective W
M0	L ≤ 1	any width	$9 \times 1.271 \times (w - 0.003)$
	L > 1	$0.04 \leq w \leq 0.12$	$6 \times 1.271 \times (w - 0.003)$
	$1.5 \geq L > 1$	$w > 0.12; w < 0.04$	$6 \times 1.271 \times (w - 0.003)$
	$2 \geq L > 1.5$	$w > 0.12; w < 0.04$	$4.5 \times 1.271 \times (w - 0.003)$
	$2.5 \geq L > 2$	$w > 0.12; w < 0.04$	$3.6 \times 1.271 \times (w - 0.003)$
	$3 \geq L > 2.5$	$w > 0.12; w < 0.04$	$3 \times 1.271 \times (w - 0.003)$
	L > 3	w > 0.12	$3 \times 1.271 \times (w - 0.003)$
	$3.3 \geq L > 3$	w < 0.040	$2.6 \times 1.271 \times (w - 0.003)$
	$4 \geq L > 3.3$	w < 0.040	$2.0 \times 1.271 \times (w - 0.003)$
	$4.5 \geq L > 4$	w < 0.040	$1.8 \times 1.271 \times (w - 0.003)$
M1	L > 4.5	w < 0.040	$1.5 \times 1.271 \times (w - 0.003)$
	L ≤ 1	any width	$9 \times 1.068 \times (w - 0.003)$
	L > 1	$0.037 \leq w \leq 0.12$	$6 \times 1.068 \times (w - 0.003)$
	$1.5 \geq L > 1$	$w > 0.12; w < 0.037$	$6 \times 1.068 \times (w - 0.003)$
	$2 \geq L > 1.5$	$w > 0.12; w < 0.037$	$4.5 \times 1.068 \times (w - 0.003)$
	$2.5 \geq L > 2$	$w > 0.12; w < 0.037$	$3.6 \times 1.068 \times (w - 0.003)$
	$3 \geq L > 2.5$	$w > 0.12; w < 0.037$	$3 \times 1.068 \times (w - 0.003)$
	L > 3	w > 0.12	$3 \times 1.068 \times (w - 0.003)$
	$3.3 \geq L > 3$	w < 0.037	$2.6 \times 1.068 \times (w - 0.003)$
	$4 \geq L > 3.3$	w < 0.037	$2.0 \times 1.068 \times (w - 0.003)$
Mx, Mxa, Mxs	$4.5 \geq L > 4$	w < 0.037	$1.8 \times 1.068 \times (w - 0.003)$
	L > 4.5	w < 0.037	$1.5 \times 1.068 \times (w - 0.003)$
	L ≤ 1	any width	$9 \times 1.184 \times (w - 0.003)$
	L > 1	$0.04 \leq w \leq 0.12$	$6 \times 1.184 \times (w - 0.003)$
	$1.5 \geq L > 1$	$w > 0.12; w < 0.04$	$6 \times 1.184 \times (w - 0.003)$
	$2 \geq L > 1.5$	$w > 0.12; w < 0.04$	$4.5 \times 1.184 \times (w - 0.003)$
	$2.5 \geq L > 2$	$w > 0.12; w < 0.04$	$3.6 \times 1.184 \times (w - 0.003)$
	$3 \geq L > 2.5$	$w > 0.12; w < 0.04$	$3 \times 1.184 \times (w - 0.003)$
	L > 3	w > 0.12	$3 \times 1.184 \times (w - 0.003)$
	$3.3 \geq L > 3$	w < 0.040	$2.6 \times 1.184 \times (w - 0.003)$
Mya	$4 \geq L > 3.3$	w < 0.040	$2.0 \times 1.184 \times (w - 0.003)$
	$4.5 \geq L > 4$	w < 0.040	$1.8 \times 1.184 \times (w - 0.003)$
	L > 4.5	w < 0.040	$1.5 \times 1.184 \times (w - 0.003)$
	L ≤ 1	Any width	$4.5 \times 1.555 \times (w - 0.003)$
	$3 \geq L > 1$	Any width	$3 \times 1.555 \times (w - 0.003)$
My	L > 3	$1 > w \geq 0.058$	$3 \times 1.555 \times (w - 0.003)$
	L > 3	w ≥ 1	$2 \times 1.555 \times (w - 0.003)$
	L > 3	w < 0.058	$1.555 \times (w - 0.003)$
	L ≤ 1	Any width	$4.5 \times 2.102 \times (w - 0.004)$
	$5 \geq L > 1$	Any width	$3 \times 2.102 \times (w - 0.004)$

Metal Wiring Level	Metal Length, L (μm)	Metal Width [drawn], W (μm)	$I_{max} (\text{mA})$, effective W
	L > 5	$w \geq 0.058$	$2 \times 2.102 \times (w - 0.004)$
	L > 5	$w < 0.058$	$2.102 \times (w - 0.004)$
Myy	L ≤ 5	Any width	$3 \times 4.061 \times (w - 0.008)$
	L > 5	$w \geq 0.45$	$2 \times 4.061 \times (w - 0.008)$
	L > 5	$w < 0.45$	$4.061 \times (w - 0.008)$
Myx	L ≤ 4.5	Any width	$4 \times 4.976 \times (w - 0.02)$
	L > 4.5	$w \geq 0.45$	$2 \times 4.976 \times (w - 0.02)$
	$9 \geq L > 4.5$	$w < 0.45$	$1.5 \times 4.976 \times (w - 0.02)$
	L > 9	$w < 0.45$	$4.976 \times (w - 0.02)$
Myz	L ≤ 4.5	Any width	$4 \times 8.132 \times (w - 0.020)$
	L > 4.5	$w \geq 0.45$	$2 \times 8.132 \times (w - 0.020)$
	$9 \geq L > 4.5$	$w < 0.45$	$1.5 \times 8.132 \times (w - 0.020)$
	L > 9	$w < 0.45$	$8.132 \times (w - 0.020)$
Mz	L ≤ 4.5	Any width	$4 \times 14.811 \times (w - 0.020)$
	$9 \geq L > 4.5$	Any width	$1.5 \times 14.811 \times (w - 0.020)$
	L > 9	Any width	$14.811 \times (w - 0.020)$
Mr	L ≤ 4.5	Any width	$4 \times 18.996 \times (w - 0.020)$
	$9 \geq L > 4.5$	Any width	$1.5 \times 18.996 \times (w - 0.020)$
	L > 9	Any width	$18.996 \times (w - 0.020)$

10.4.5.5 Via I_{max} dependence on metal length & width

For vias, when bottom metal layer meets the width rule criterion (e.g., $W \geq 0.04 \mu\text{m}$ for M1/Mx/Mxa) or short-length criterion (e.g., $L \leq 3 \mu\text{m}$) and upper metal also meets the width rule or the short-length criterion, please pick the worst one to follow.

The detailed I_{max} specs for vias are described in Table 10.4.4. In this table, w represents the drawn width of the metal line in μm , while L represents the length of the metal line in μm . The junction temperature for these specs is 105°C.

The maximum allowed current for per via can be raised together with this wide metal EM rule (eg., $w \geq 0.04 \mu\text{m}$ of M1/Mx/Mxa).

Table 10.4.4

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{max} (mA)
V0	Landing on M0	L ≤ 1; Any width	L ≤ 1; Any width	9 × 0.0403 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	6 × 0.0403 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	L > 1.5; 0.037 ≤ w ≤ 0.12	6 × 0.0403 per via
		L > 3; w < 0.04	any length ; any width	1.5 × 0.0403 per via
		any length; any width	L > 3; w < 0.037	1.5 × 0.0403 per via
		Others	Others	3 × 0.0403 per via
rectangular V0 (0.02x0.034 μm^2)	Landing on M0	L ≤ 1; Any width	L ≤ 1; Any width	9 × 0.0605 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	6 × 0.0605 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	L > 1.5; 0.037 ≤ w ≤ 0.12	6 × 0.0605 per via
		L > 3; w < 0.04	any length; any width	1.5 × 0.0605 per via
		any length; any width	L > 3; w < 0.037	1.5 × 0.0605 per via
		Others	Others	3 × 0.0605 per via
rectangular V0 (0.02x0.050 μm^2 and 0.02x0.06 μm^2)	Landing on M0	L ≤ 1; Any width	L ≤ 1; Any width	9 × 0.0806 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	6 × 0.0806 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	L > 1.5; 0.037 ≤ w ≤ 0.12	6 × 0.0806 per via
		L > 3; w < 0.04	any length; any width	1.5 × 0.0806 per via
		any length; any width	L > 3; w < 0.037	1.5 × 0.0806 per via
		Others	Others	3 × 0.0806 per via
V1	Landing on M1	L ≤ 1; Any width	L ≤ 1; Any width	9 × 0.0403 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	6 × 0.0403 per via
		L > 1.5; 0.037 ≤ w ≤ 0.12	L > 1.5; 0.04 ≤ w ≤ 0.12	6 × 0.0403 per via
		L > 3; w < 0.037	any length; any width	1.5 × 0.0403 per via
		any length; any width	L > 3; w < 0.04	1.5 × 0.0403 per via
		Others	Others	3 × 0.0403 per via
Vx, Vxa	Landing on	L ≤ 1; Any width	L ≤ 1; Any width	9 × 0.0403 per via

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{\max} (mA)
rectangular V1 (0.02x0.034 μm^2)	Mx/Mxs/Mxa	1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	6 × 0.0403 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	L > 1.5; 0.04 ≤ w ≤ 0.12	6 × 0.0403 per via
		L > 3; w < 0.04 any length; any width	any length; any width	1.5 × 0.0403 per via
		Others	Others	1.5 × 0.0403 per via
		L ≤ 1; Any width	L ≤ 1; Any width	3 × 0.0403 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	9 × 0.0605 per via
rectangular Vx, Vxa (0.02x0.034 μm^2)	Landing on M1	L > 1.5; 0.037 ≤ w ≤ 0.12	L > 1.5; 0.04 ≤ w ≤ 0.12	6 × 0.0605 per via
		L > 3; w < 0.037 any length; any width	any length; any width	1.5 × 0.0605 per via
		Others	Others	1.5 × 0.0605 per via
		L ≤ 1; Any width	L ≤ 1; Any width	3 × 0.0605 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	9 × 0.0605 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	L > 1.5; 0.04 ≤ w ≤ 0.12	6 × 0.0605 per via
rectangular V1 (0.02x0.05 μm^2)	Landing on Mx/Mxs/Mxa	L > 3; w < 0.04 any length; any width	any length; any width	1.5 × 0.0605 per via
		Others	Others	1.5 × 0.0605 per via
		L ≤ 1; Any width	L ≤ 1; Any width	3 × 0.0605 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	9 × 0.0806 per via
		L > 1.5; 0.037 ≤ w ≤ 0.12	L > 1.5; 0.04 ≤ w ≤ 0.12	6 × 0.0806 per via
		L > 3; w < 0.037 any length; any width	any length; any width	1.5 × 0.0806 per via
rectangular Vx, Vxa (0.02x0.05 μm^2)	Landing on M1	Others	Others	1.5 × 0.0806 per via
		L ≤ 1; Any width	L ≤ 1; Any width	3 × 0.0806 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	9 × 0.0806 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	L > 1.5; 0.04 ≤ w ≤ 0.12	6 × 0.0806 per via
		L > 3; w < 0.04 any length; any width	any length; any width	1.5 × 0.0806 per via
		Others	Others	1.5 × 0.0806 per via
Vx, Vxa (exclude V1) (0.038x0.038 μm^2)	Landing on Mx/Mxs/Mxa	L ≤ 1; Any width	L ≤ 1; Any width	3 × 0.0806 per via
		1 < L ≤ 1.5; Any width	1 < L ≤ 1.5; Any width	9 × 0.0829 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	L > 1.5; 0.04 ≤ w ≤ 0.12	6 × 0.0829 per via
		L > 3; w < 0.04 any length; any width	any length; any width	1.5 × 0.0829 per via
		Others	Others	1.5 × 0.0829 per via
		L ≤ 1; any width	L ≤ 1; any width	3 × 0.0829 per via
Vya	Landing on	L ≤ 1; any width	L ≤ 1; any width	4.5 × 0.0529 per via

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{\max} (mA)
	Mx/Mxs/Mxa	1 < L ≤ 3; any width	1 < L ≤ 3; any width	3 × 0.0529 per via
		L > 3; w ≥ 0.04	1 < L ≤ 3; any width	3 × 0.0529 per via
		1 < L ≤ 3; any width	L > 3; 1 > w ≥ 0.058	3 × 0.0529 per via
		1 < L ≤ 3; any width	L > 3; w ≥ 1	2 × 0.0529 per via
		Others	Others	0.0529 per via
rectangular Vya	Landing on Mx/Mxs/Mxa	L ≤ 1; any width	L ≤ 1; any width	4.5 × 0.1058 per via
		1 < L ≤ 3; any width	1 < L ≤ 3; any width	3 × 0.1058 per via
		L > 3; w ≥ 0.04	1 < L ≤ 3; any width	3 × 0.1058 per via
		1 < L ≤ 3; any width	L > 3; 1 > w ≥ 0.058	3 × 0.1058 per via
		1 < L ≤ 3; any width	L > 3; w ≥ 1	2 × 0.1058 per via
		Others	Others	0.1058 per via
Vya (0.038x0.038 μm^2)	Landing on Mx/Mxs/Mxa	L ≤ 1; any width	L ≤ 1; any width	4.5 × 0.1089 per via
		1 < L ≤ 3; any width	1 < L ≤ 3; any width	3 × 0.1089 per via
		L > 3; w ≥ 0.04	1 < L ≤ 3; any width	3 × 0.1089 per via
		1 < L ≤ 3; any width	L > 3; 1 > w ≥ 0.058	3 × 0.1089 per via
		1 < L ≤ 3; any width	L > 3; w ≥ 1	2 × 0.1089 per via
		Others	Others	0.1089 per via
Vy	Landing on My/Mya	L ≤ 1; any width	L ≤ 1; any width	4.5 × 0.143 per via
		1 < L ≤ 5; w ≤ 0.45	1 < L ≤ 5; w ≤ 0.45	3 × 0.143 per via
		L > 5; 0.45 ≥ w ≥ 0.058	1 < L ≤ 5; w ≤ 0.45	2 × 0.143 per via
		1 < L ≤ 5; w ≤ 0.45	L > 5; 0.45 ≥ w ≥ 0.058	2 × 0.143 per via
		L > 5; 0.45 ≥ w ≥ 0.058	L > 5; 0.45 ≥ w ≥ 0.058	2 × 0.143 per via
		1 < L ≤ 5; w ≤ 0.45	1 < L ≤ 5; w > 0.45	1.5 × 0.143 per via
		1 < L ≤ 5; w > 0.45	1 < L ≤ 5; any width	1.5 × 0.143 per via
		1 < L ≤ 5; w > 0.45	L > 5; 0.45 ≥ w ≥ 0.058	1.5 × 0.143 per via
		L > 5; 0.45 ≥ w ≥ 0.058	1 < L ≤ 5; w > 0.45	1.5 × 0.143 per via
		Others	Others	0.143 per via
rectangular Vy	Landing on My/Mya	L ≤ 1; any width	L ≤ 1; any width	4.5 × 0.286 per via
		1 < L ≤ 5; w ≤ 0.45	1 < L ≤ 5; w ≤ 0.45	3 × 0.286 per via
		L > 5; 0.45 ≥ w ≥ 0.058	1 < L ≤ 5; w ≤ 0.45	2 × 0.286 per via
		1 < L ≤ 5; w ≤ 0.45	L > 5; 0.45 ≥ w ≥ 0.058	2 × 0.286 per via
		L > 5; 0.45 ≥ w ≥ 0.058	L > 5; 0.45 ≥ w ≥ 0.058	2 × 0.286 per via
		1 < L ≤ 5; w ≤ 0.45	1 < L ≤ 5; w > 0.45	1.5 × 0.286 per via
		1 < L ≤ 5; w > 0.45	1 < L ≤ 5; any width	1.5 × 0.286 per via
		1 < L ≤ 5; w > 0.45	L > 5; 0.45 ≥ w ≥ 0.058	1.5 × 0.286 per via
		L > 5; 0.45 ≥ w ≥ 0.058	1 < L ≤ 5; w > 0.45	1.5 × 0.286 per via
		Others	Others	0.286 per via
Vy	Landing on My/Mya	L ≤ 1; any width	L ≤ 1; any width	4.5 × 0.227 per via

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{\max} (mA)
(0.058x0.058 μm^2)		1 < L ≤ 5; w ≤ 0.45	1 < L ≤ 5; w ≤ 0.45	3 × 0.227 per via
		L > 5; 0.45 ≥ w ≥ 0.058	1 < L ≤ 5; w ≤ 0.45	2 × 0.227 per via
		1 < L ≤ 5; w ≤ 0.45	L > 5; 0.45 ≥ w ≥ 0.058	2 × 0.227 per via
		L > 5; 0.45 ≥ w ≥ 0.058	L > 5; 0.45 ≥ w ≥ 0.058	2 × 0.227 per via
		1 < L ≤ 5; w ≤ 0.45	1 < L ≤ 5; w > 0.45	1.5 × 0.227 per via
		1 < L ≤ 5; w > 0.45	1 < L ≤ 5; any width	1.5 × 0.227 per via
		1 < L ≤ 5; w > 0.45	L > 5; 0.45 ≥ w ≥ 0.058	1.5 × 0.227 per via
		L > 5; 0.45 ≥ w ≥ 0.058	1 < L ≤ 5; w > 0.45	1.5 × 0.227 per via
		Others	Others	0.227 per via
Vyy	Landing on My	L ≤ 5; w ≤ 0.45	L ≤ 5; w ≤ 0.45	3 × 0.4386 per via
		L ≤ 5; w ≤ 0.45	L ≤ 5; w > 0.45	1.5 × 0.4386 per via
		L ≤ 5; w > 0.45	L ≤ 5; any width	1.5 × 0.4386 per via
		L > 5; 0.45 ≥ w ≥ 0.058	L ≤ 5; w ≤ 0.45	2 × 0.4386 per via
		L > 5; 0.45 ≥ w ≥ 0.058	L ≤ 5; w > 0.45	1.5 × 0.4386 per via
		Others	Others	0.4386 per via
Vyx	Landing on Myy	L ≤ 5; w ≤ 0.45	L ≤ 5; w ≤ 0.45	3 × 0.4386 per via
		L ≤ 5; w ≤ 0.45	L ≤ 5; w > 0.45	1.5 × 0.4386 per via
		L ≤ 5; w > 0.45	L ≤ 5; any width	1.5 × 0.4386 per via
		Others	Others	0.4386 per via
		L ≤ 4.5; any width	L ≤ 4.5; any width	4 × 0.5275 per via
		L > 4.5; w ≥ 0.45	L ≤ 4.5; any width	2 × 0.5275 per via (array)
Vyz	Landing on Myy/Myx	9 ≥ L > 4.5; w ≥ 0.45	L ≤ 4.5; any width	1.5 × 0.5275 Single via
		L ≤ 4.5; any width	L > 4.5; w ≥ 0.45	2 × 0.5275 per via (array)
		L ≤ 4.5; any width	9 ≥ L > 4.5; w ≥ 0.45	1.5 × 0.5275 Single via
		L > 4.5; w ≥ 0.45	L > 4.5; w ≥ 0.45	2 × 0.5275 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	9 ≥ L > 4.5; w ≥ 0.45	1.5 × 0.5275 Single via
		L ≤ 4.5; any width	9 ≥ L > 4.5; w < 0.45	1.5 × 0.5275 per via
		L > 4.5; w ≥ 0.45	9 ≥ L > 4.5; w < 0.45	1.5 × 0.5275 per via
		9 ≥ L > 4.5; w < 0.45	9 ≥ L > 4.5; w < 0.45	1.5 × 0.5275 per via
		9 ≥ L > 4.5; w < 0.45	L ≤ 4.5; any width	1.5 × 0.5275 per via
		9 ≥ L > 4.5; w < 0.45	L > 4.5; w ≥ 0.45	1.5 × 0.5275 per via
		Others	Others	0.5275 per via
		L ≤ 4.5; any width	L ≤ 4.5; any width	4 × 1.3012 per via
Vyz	Landing on Myy/Myx/Myz	L > 4.5; w ≥ 0.45	L ≤ 4.5; any width	2 × 1.3012 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	L ≤ 4.5; any width	1.5 × 1.3012 Single via
		L > 4.5; w ≥ 0.45	9 ≥ L > 4.5; any width	1.5 × 1.3012 per via
		L ≤ 4.5; any width	9 ≥ L > 4.5; any width	1.5 × 1.3012 per via
		9 ≥ L > 4.5; w < 0.45	9 ≥ L > 4.5; any width	1.5 × 1.3012 per via
		9 ≥ L > 4.5; w < 0.45	L ≤ 4.5; any width	1.5 × 1.3012 per via
		others	Others	1.3012 per via

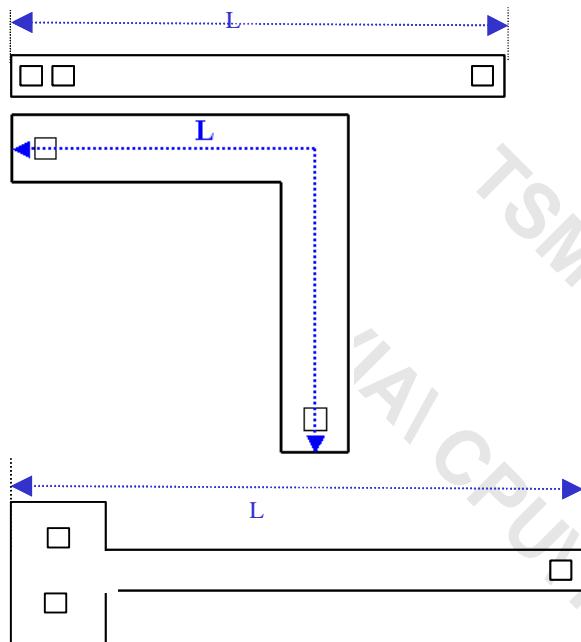
Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{max} (mA)
Vz	Landing on My	L≤5; any width	L≤4.5; any width	3 × 2.0726 per via
		L>5; w≥0.45	L≤4.5; any width	2 × 2.0726 per via (array)
		L>5; w≥0.45	9≥L>4.5; any width	1.5 × 2.0726 per via
		L≤5; any width	9≥L>4.5; any width	1.5 × 2.0726 per via
		Others	Others	2.0726 per via
	Landing on Myy	L ≤ 5; any width	L ≤ 4.5; any width	3 × 3.9879 per via
		L > 5; w ≥ 0.45	L ≤ 4.5; any width	2 × 3.9879 per via (array)
		L > 5; w ≥ 0.45	9 ≥ L > 4.5; any width	1.5 × 3.9879 per via
		L ≤ 5; any width	9 ≥ L > 4.5; any width	1.5 × 3.9879 per via
		Others	Others	3.9879 per via
Vr	Landing on Myx	L≤4.5; any width	L≤4.5; any width	4 × 4.8267 per via
		L>4.5; w≥0.45	L≤4.5; any width	2 × 4.8267 per via (array)
		9≥L>4.5; w≥0.45	L≤4.5; any width	1.5 × 4.8267 Single via
		L>4.5; w≥0.45	9≥L>4.5; any width	1.5 × 4.8267 per via
		L≤4.5; any width	9≥L>4.5; any width	1.5 × 4.8267 per via
		9≥L>4.5; w<0.45	9≥L>4.5; any width	1.5 × 4.8267 per via
		9≥L>4.5; w<0.45	L≤4.5; any width	1.5 × 4.8267 per via
		Others	others	4.8267 per via
	Landing on Myz	L ≤ 4.5; any width	L ≤ 4.5; any width	4 × 5.0357 per via
		L > 4.5; w ≥ 0.45	L ≤ 4.5; any width	2 × 5.0357 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	L ≤ 4.5; any width	1.5 × 5.0357 Single via
		L > 4.5; w ≥ 0.45	9 ≥ L > 4.5; any width	1.5 × 5.0357 per via
		L ≤ 4.5; any width	9 ≥ L > 4.5; any width	1.5 × 5.0357 per via
		9 ≥ L > 4.5; w < 0.45	9 ≥ L > 4.5; any width	1.5 × 5.0357 per via
		9 ≥ L > 4.5; w < 0.45	L ≤ 4.5; any width	1.5 × 5.0357 per via
Vt	Landing on Mz	others	others	5.0357 per via
		L ≤ 4.5; any width	L ≤ 4.5; any width	4 × 5.0357 per via
		L ≤ 4.5; any width	9 ≥ L > 4.5; any width	1.5 × 5.0357 per via
		9 ≥ L > 4.5; any width	9 ≥ L > 4.5; any width	1.5 × 5.0357 per via
		9 ≥ L > 4.5; any width	L ≤ 4.5; any width	1.5 × 5.0357 per via
	Landing on My	Others	Others	5.0357 per via
		L≤5; any width	L≤4.5; any width	3 × 2.6317 per via
		L>5; w≥0.45	L≤4.5; any width	2 × 2.6317 per via (array)
		L>5; w≥0.45	9≥L>4.5; any width	1.5 × 2.6317 per via
		L≤5; any width	9≥L>4.5; any width	1.5 × 2.6317 per via
	Landing on Myy	Others	Others	2.6317 per via
		L ≤ 5; any width	L ≤ 4.5; any width	3 × 5.0356 per via
		L > 5; w ≥ 0.45	L ≤ 4.5; any width	2 × 5.0356 per via (array)
		L > 5; w ≥ 0.45	9 ≥ L > 4.5; any width	1.5 × 5.0356 per via
		L ≤ 5; any width	9 ≥ L > 4.5; any width	1.5 × 5.0356 per via
	Landing on Myx	Others	Others	5.0356 per via
		L ≤ 4.5; any width	L ≤ 4.5; any width	4 × 6.1702 per via
		L > 4.5; w ≥ 0.45	L ≤ 4.5; any width	2 × 6.1702 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	L ≤ 4.5; any width	1.5 × 6.1702 Single via
		L > 4.5; w ≥ 0.45	9 ≥ L > 4.5; any width	1.5 × 6.1702 per via
		L ≤ 4.5; any width	9 ≥ L > 4.5; any width	1.5 × 6.1702 per via

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{\max} (mA)
Landing on Mr/Mz	9 \geq L > 4.5; w < 0.45	9 \geq L > 4.5;any width	L \leq 4.5; any width	1.5 \times 6.1702 per via
		9 \geq L > 4.5; w < 0.45	L \leq 4.5; any width	1.5 \times 6.1702 per via
		Others	Others	6.1702 per via
	L \leq 4.5; any width	L \leq 4.5; any width	L \leq 4.5; any width	4 \times 8.1683 per via
		L \leq 4.5; any width	9 \geq L > 4.5;any width	1.5 \times 8.1683 per via
		9 \geq L > 4.5; any width	9 \geq L > 4.5;any width	1.5 \times 8.1683 per via
		9 \geq L > 4.5; any width	L \leq 4.5; any width	1.5 \times 8.1683 per via
		Others	Others	8.1683 per via

10.4.5.6 Length & Width Definition for EM section (10.4.5.4 & 10.4.5.5 & 10.4.5.7 & 10.4.5.10)

(1) Metal Length Definition (L):

The total length of metal wiring level is from one line-end site to another site line-end site of metal.



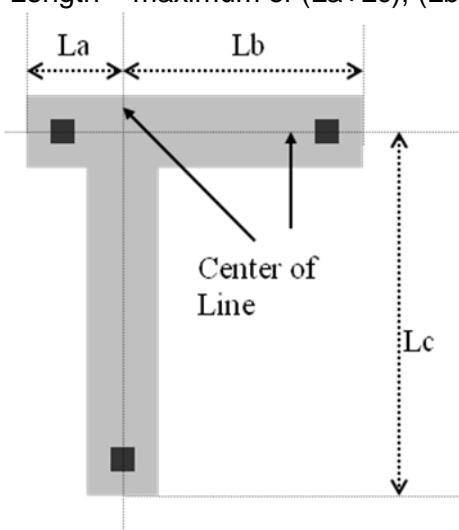
(2) Specific layout

In complex structure, the length should be selected the longest path.

(a) T-shape

The length is (L_a+L_c) or (L_b+L_c) or (L_a+L_b) , select the longest one.

Length = maximum of (L_a+L_c) , (L_b+L_c) , (L_a+L_b)

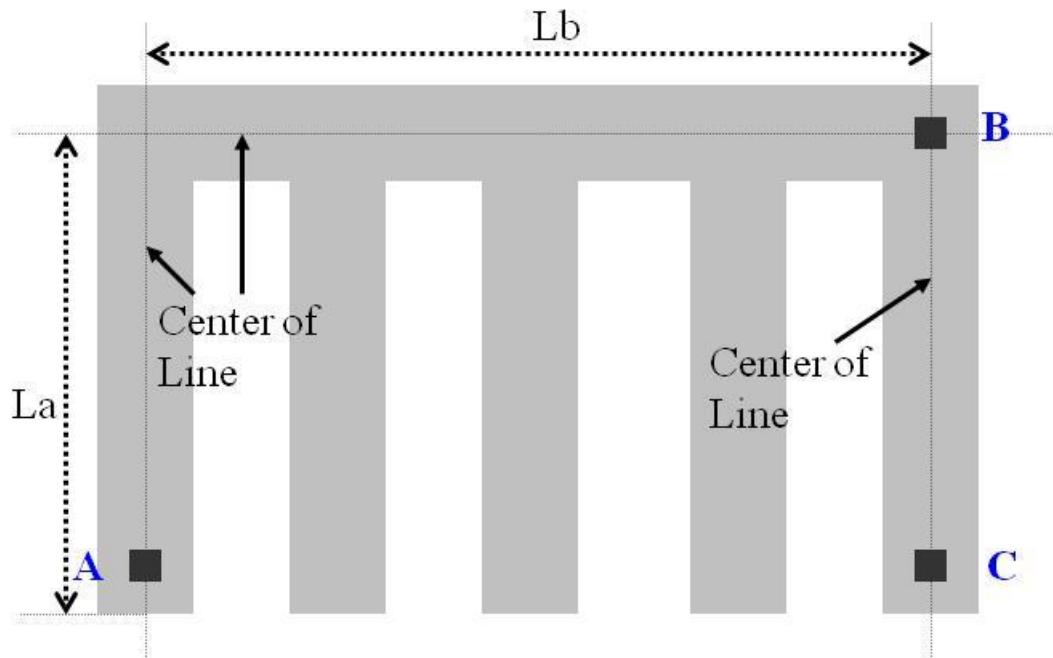


(b) Finger structure:

Current flow from point-A to point-B : Length= La + Lb +La = 2 x La + Lb

The longest path in this structure is from point-A to point-C.

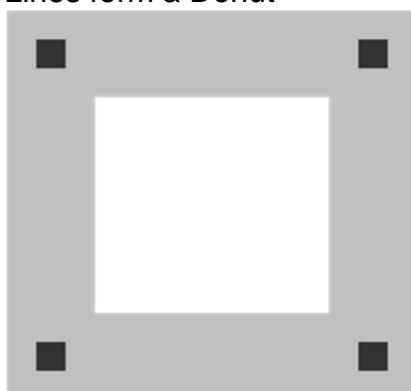
$$\text{Length} = \text{La} + \text{Lb} + \text{La} = 2\text{La} + \text{Lb}$$



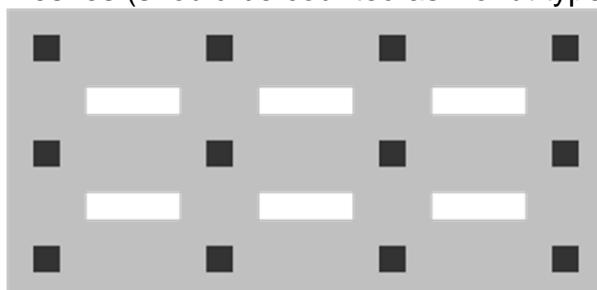
(c) Donut type: it can't apply short length rule.

Meshes need to count as donut type, but wide metal line with slot doesn't count.

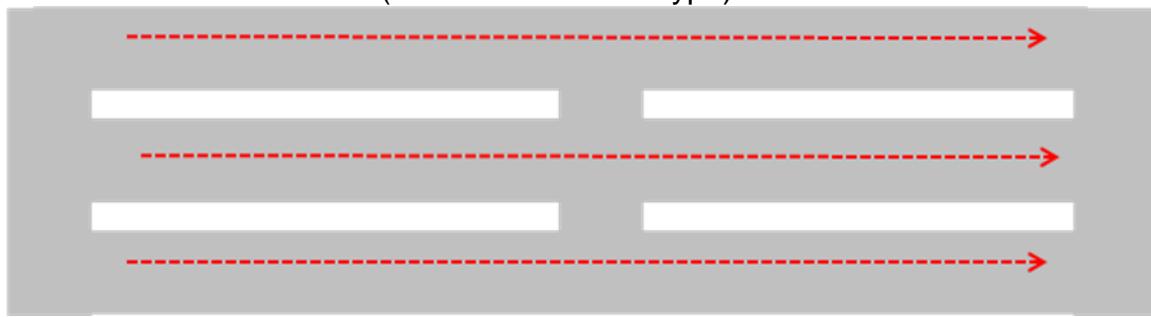
Lines form a Donut



Meshes (should be counted as Donut type structure)



Wide metal lines with slots (no count for Donut type)



(3) Width Definition (W) for via EM rule:

Width definition for the Via width rule, metal width is via location's metal width.

For example, when $W_1 > W_2$

Case-1 (via at W_2): width= W_2



Case-2 (via at W_1): width= W_1



Case-3(via at W_1/W_2 intersection): width= W_2 , select the worst width

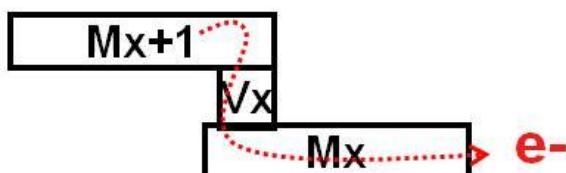


10.4.5.7 Via I_{max} for known electron-current direction

If electron current flow is known direction, via enhanced rule for length/width dependence can be depended on one of metals, not necessary to check both upper-metal and bottom-metal. Guideline as below:

- (a) Down stream current (electron current from M_{x+1} to M_x) : length/width dependence rule based on bottom metal (M_x). Please refer to Table 10.4.5
- (b) Up stream current (electron current from M_x to M_{x+1}) : length/width dependence based on upper metal (M_{x+1}). Please refer to Table 10.4.6.

Downstream



Upstream

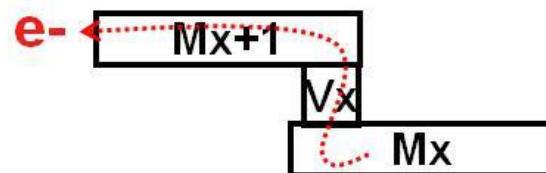


Table 10.4.5 (downstream)

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	I _{max} (mA)
V0	Landing on M0	L ≤ 1; Any width	9× 0.0403 per via
		1 < L ≤ 1.5; Any width	6× 0.0403 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	6× 0.0403 per via
		L > 3; w < 0.04	1.5× 0.0403 per via
		Others	3 × 0.0403 per via
rectangular V0 (0.02x0.034 μm^2)	Landing on M0	L ≤ 1; Any width	9× 0.0605 per via
		1 < L ≤ 1.5; Any width	6× 0.0605 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	6× 0.0605 per via
		L > 3; w < 0.04	1.5× 0.0605 per via
		Others	3 × 0.0605 per via
rectangular V0 (0.02x0.050 μm^2 and 0.02x0.06 μm^2)	Landing on M0	L ≤ 1; Any width	9× 0.0806 per via
		1 < L ≤ 1.5; Any width	6× 0.0806 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	6× 0.0806 per via
		L > 3; w < 0.04	1.5× 0.0806 per via
		Others	3 × 0.0806 per via
V1	Landing on M1	L ≤ 1; Any width	9× 0.0403 per via
		1 < L ≤ 1.5; Any width	6× 0.0403 per via
		L > 1.5; 0.037 ≤ w ≤ 0.12	6× 0.0403 per via
		L > 3; w < 0.037	1.5× 0.0403 per via
		Others	3 × 0.0403 per via
Vx, Vxa	Landing on Mx/Mxs/Mxa	L ≤ 1; Any width	9× 0.0403 per via
		1 < L ≤ 1.5; Any width	6× 0.0403 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	6× 0.0403 per via
		L > 3; w < 0.04	1.5× 0.0403 per via
		Others	3 × 0.0403 per via
rectangular V1 (0.02x0.034 μm^2)	Landing on M1	L ≤ 1; Any width	9× 0.0605 per via
		1 < L ≤ 1.5; Any width	6× 0.0605 per via
		L > 1.5; 0.037 ≤ w ≤ 0.12	6× 0.0605 per via
		L > 3; w < 0.037	1.5× 0.0605 per via
		Others	3 × 0.0605 per via
rectangular Vx, Vxa (0.02x0.034 μm^2)	Landing on Mx/Mxs/Mxa	L ≤ 1; Any width	9× 0.0605 per via
		1 < L ≤ 1.5; Any width	6× 0.0605 per via
		L > 1.5; 0.04 ≤ w ≤ 0.12	6× 0.0605 per via
		L > 3; w < 0.04	1.5× 0.0605 per via
		Others	3 × 0.0605 per via
rectangular V1 (0.02x0.050 μm^2)	Landing on M1	L ≤ 1; Any width	9× 0.0806 per via
		1 < L ≤ 1.5; Any width	6× 0.0806 per via

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	I _{max} (mA)
rectangular Vx, Vxa ($0.02 \times 0.050 \mu\text{m}^2$)	Landing on Mx/Mxs/Mxa	L > 1.5; $0.037 \leq w \leq 0.12$	6×0.0806 per via
		L > 3; w < 0.037	1.5×0.0806 per via
		Others	3×0.0806 per via
Vx, Vxa (exclude V1) ($0.038 \times 0.038 \mu\text{m}^2$)	Landing on Mx/Mxs/Mxa	L ≤ 1; Any width	9×0.0806 per via
		$1 < L \leq 1.5$; Any width	6×0.0806 per via
		L > 1.5; $0.04 \leq w \leq 0.12$	6×0.0806 per via
		L > 3; w < 0.04	1.5×0.0806 per via
		Others	3×0.0806 per via
Vya	Landing on Mx/Mxs/Mxa	L ≤ 1; Any width	9×0.0829 per via
		$1 < L \leq 1.5$; Any width	6×0.0829 per via
		L > 1.5; $0.04 \leq w \leq 0.12$	6×0.0829 per via
		L > 3; w < 0.04	1.5×0.0829 per via
		Others	3×0.0829 per via
rectangular Vya	Landing on Mx/Mxs/Mxa	L ≤ 1; Any width	4.5×0.0529 per via
		$1 < L \leq 3$; any width	3×0.0529 per via
		L > 3; w ≥ 0.04	3×0.0529 per via
		Others	0.0529 per via
Vya ($0.038 \times 0.038 \mu\text{m}^2$)	Landing on Mx/Mxs/Mxa	L ≤ 1; Any width	4.5×0.1058 per via
		$1 < L \leq 3$; any width	3×0.1058 per via
		L > 3; w ≥ 0.04	3×0.1058 per via
		Others	0.1058 per via
		L ≤ 1; Any width	4.5×0.1089 per via
Vy	Landing on My/Mya	$1 < L \leq 3$; any width	3×0.1089 per via
		L > 3; w ≥ 0.04	3×0.1089 per via
		Others	0.1089 per via
		L ≤ 1; Any width	4.5×0.143 per via
		$1 < L \leq 5$; W≤0.45	3×0.143 per via
rectangular Vy	Landing on My/Mya	$1 < L \leq 5$; W>0.45	1.5×0.143 per via
		L > 5; $0.45 \geq w \geq 0.058$	2×0.143 per via
		Others	0.143 per via
		L ≤ 1; Any width	4.5×0.286 per via
		$1 < L \leq 5$; w≤0.45	3×0.286 per via
Vy ($0.058 \times 0.058 \mu\text{m}^2$)	Landing on My/Mya	$1 < L \leq 5$; w>0.45	1.5×0.286 per via
		L > 5; $0.45 \geq w \geq 0.058$	2×0.286 per via
		Others	0.286 per via
		L ≤ 1; Any width	4.5×0.227 per via
		$1 < L \leq 5$; W ≤ 0.45	3×0.227 per via
Vyy	Landing on My	$1 < L \leq 5$; W > 0.45	1.5×0.227 per via
		L > 5; $0.45 \geq w \geq 0.058$	2×0.227 per via
		Others	0.227 per via
		L ≤ 5; w≤0.45	3×0.4386 per via

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn], w (μm)	I _{max} (mA)
V _{yx}		L ≤ 5; W > 0.45	1.5 × 0.4386 per via
		L > 5; 0.45 ≥ w ≥ 0.058	2 × 0.4386 per via
		Others	0.4386 per via
	Landing on Myy	L ≤ 5; w ≤ 0.45	3 × 0.4386 per via
		L ≤ 5; w > 0.45	1.5 × 0.4386 per via
		Others	0.4386 per via
	Landing on Myy/Myx	L ≤ 4.5; any width	4 × 0.5275 per via
		L > 4.5; w ≥ 0.45	2 × 0.5275 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	1.5 × 0.5275 Single via
		9 ≥ L > 4.5; w < 0.45	1.5 × 0.5275 per via
		Others	0.5275 per via
V _{yz}	Landing on Myy/Myx/Myz	L ≤ 4.5; any width	4 × 1.3012 per via
		L > 4.5; w ≥ 0.45	2 × 1.3012 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	1.5 × 1.3012 Single via
		9 ≥ L > 4.5; w < 0.45	1.5 × 1.3012 per via
		Others	1.3012 per via
	Landing on My	L ≤ 5; any width	3 × 2.0726 per via
		L > 5; w ≥ 0.45	2 × 2.0726 per via (array)
		Others	2.0726 per via
	Landing on Myy	L ≤ 5; any width	3 × 3.9879 per via
		L > 5; w ≥ 0.45	2 × 3.9879 per via (array)
		Others	3.9879 per via
V _z	Landing on Myx	L ≤ 4.5; any width	4 × 4.8267 per via
		L > 4.5; w ≥ 0.45	2 × 4.8267 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	1.5 × 4.8267 Single via
		9 ≥ L > 4.5; w < 0.45	1.5 × 4.8267 per via
		others	4.8267 per via
	Landing on Myz	L ≤ 4.5; any width	4 × 5.0357 per via
		L > 4.5; w ≥ 0.45	2 × 5.0357 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	1.5 × 5.0357 Single via
	Landing on Mz	9 ≥ L > 4.5; W < 0.45	1.5 × 5.0357 per via
		others	5.0357 per via
V _r	Landing on My	L ≤ 5; any width	4 × 5.0357 per via
		L > 5; w ≥ 0.45	2 × 5.0357 per via (array)
		Others	2.6317 per via
	Landing on Myy	L ≤ 5; any width	3 × 5.0356 per via
		L > 5; w ≥ 0.45	2 × 5.0356 per via (array)
		Others	5.0356 per via
	Landing on Myx	L ≤ 4.5; any width	4 × 6.1702 per via
		L > 4.5; w ≥ 0.45	2 × 6.1702 per via (array)
		9 ≥ L > 4.5; w ≥ 0.45	1.5 × 6.1702 Single via
		9 ≥ L > 4.5; w < 0.45	1.5 × 6.1702 per via
		Others	6.1702 per via

Interlevel connection	Via landing on Bottom Metal	Bottom Metal Length, L (μm) & Width [drawn] , w (μm)	I _{max} (mA)
Landing on Mr/Mz	L \leq 4.5; any width	4 \times 8.1683 per via	
	9 \geq L $>$ 4.5; any width	1.5 \times 8.1683 per via	
	Others	8.1683 per via	

TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

Table 10.4.6 (upstream)

Interlevel connection	Via landing on Bottom Metal	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{max} (mA)
V0	Landing on M0	L \leq 1; Any width	9×0.0403 per via
		1 $<$ L \leq 1.5; Any width	6×0.0403 per via
		L $>$ 1.5; 0.037 \leq w \leq 0.12	6×0.0403 per via
		L $>$ 3; w $<$ 0.037	1.5×0.0403 per via
		Others	3×0.0403 per via
rectangular V0 (0.02x0.034 μm^2)	Landing on M0	L \leq 1; Any width	9×0.0605 per via
		1 $<$ L \leq 1.5; Any width	6×0.0605 per via
		L $>$ 1.5; 0.037 \leq w \leq 0.12	6×0.0605 per via
		L $>$ 3; w $<$ 0.037	1.5×0.0605 per via
		Others	3×0.0605 per via
rectangular V0 (0.02x0.050 μm^2)	Landing on M0	L \leq 1; Any width	9×0.0806 per via
		1 $<$ L \leq 1.5; Any width	6×0.0806 per via
		L $>$ 1.5; 0.037 \leq w \leq 0.12	6×0.0806 per via
		L $>$ 3; w $<$ 0.037	1.5×0.0806 per via
		Others	3×0.0806 per via
V1, Vx, Vxa	Landing on M1/Mx/Mxs/Mxa	L \leq 1; Any width	9×0.0403 per via
		1 $<$ L \leq 1.5; Any width	6×0.0403 per via
		L $>$ 1.5; 0.04 \leq w \leq 0.12	6×0.0403 per via
		L $>$ 3; w $<$ 0.04	1.5×0.0403 per via
		Others	3×0.0403 per via
rectangular V1, Vx, Vxa (0.02x0.034 μm^2)	Landing on M1/Mx/Mxs/Mxa	L \leq 1; Any width	9×0.0605 per via
		1 $<$ L \leq 1.5; Any width	6×0.0605 per via
		L $>$ 1.5; 0.04 \leq w \leq 0.12	6×0.0605 per via
		L $>$ 3; w $<$ 0.04	1.5×0.0605 per via
		Others	3×0.0605 per via
rectangular V1, Vx, Vxa (0.02x0.050 μm^2)	Landing on M1/Mx/Mxs/Mxa	L \leq 1; Any width	9×0.0806 per via
		1 $<$ L \leq 1.5; Any width	6×0.0806 per via
		L $>$ 1.5; 0.04 \leq w \leq 0.12	6×0.0806 per via
		L $>$ 3; w $<$ 0.04	1.5×0.0806 per via
		Others	3×0.0806 per via
Vx, Vxa (exclude V1) (0.038x0.038 μm^2)	Landing on Mx/Mxs/Mxa	L \leq 1; Any width	9×0.0829 per via
		1 $<$ L \leq 1.5; Any width	6×0.0829 per via
		L $>$ 1.5; 0.04 \leq w \leq 0.12	6×0.0829 per via
		L $>$ 3; w $<$ 0.04	1.5×0.0829 per via
		Others	3×0.0829 per via
Vya	Landing on	L \leq 1; Any width	4.5×0.0529 per via

Interlevel connection	Via landing on Bottom Metal	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{max} (mA)
	Mx/Mxs/Mxa	$1 < L \leq 3$; any width	3×0.0529 per via
		$L > 3$; $1 > w \geq 0.058$	3×0.0529 per via
		$L > 3$; $w \geq 1$	2×0.0529 per via
		Others	0.0529 per via
rectangular Vya	Landing on Mx/Mxs/Mxa	$L \leq 1$; Any width	4.5×0.1058 per via
		$1 < L \leq 3$; any width	3×0.1058 per via
		$L > 3$; $1 > w \geq 0.058$	3×0.1058 per via
		$L > 3$; $w \geq 1$	2×0.1058 per via
		Others	0.1058 per via
Vya ($0.038 \times 0.038 \mu\text{m}^2$)	Landing on Mx/Mxs/Mxa	$L \leq 1$; Any width	4.5×0.1089 per via
		$1 < L \leq 3$; any width	3×0.1089 per via
		$L > 3$; $1 > w \geq 0.058$	3×0.1089 per via
		$L > 3$; $w \geq 1$	2×0.1089 per via
		Others	0.1089 per via
Vy	Landing on My/Mya	$L \leq 1$; Any width	4.5×0.143 per via
		$1 < L \leq 5$; $W \leq 0.45$	3×0.143 per via
		$1 < L \leq 5$; $W > 0.45$	1.5×0.143 per via
		$L > 5$; $0.45 \geq w \geq 0.058$	2×0.143 per via
		Others	0.143 per via
rectangular Vy	Landing on My/Mya	$L \leq 1$; Any width	4.5×0.286 per via
		$1 < L \leq 5$; $W \leq 0.45$	3×0.286 per via
		$1 < L \leq 5$; $W > 0.45$	1.5×0.286 per via
		$L > 5$; $0.45 \geq w \geq 0.058$	2×0.286 per via
		Others	0.286 per via
Vy ($0.058 \times 0.058 \mu\text{m}^2$)	Landing on My/Mya	$L \leq 1$; Any width	4.5×0.227 per via
		$1 < L \leq 5$; $W \leq 0.45$	3×0.227 per via
		$1 < L \leq 5$; $W > 0.45$	1.5×0.227 per via
		$L > 5$; $0.45 \geq w \geq 0.058$	2×0.227 per via
		Others	0.227 per via
Vyy	Landing on My/Myy	$L \leq 5$; $w \leq 0.45$	3×0.4386 per via
		$L \leq 5$; $w > 0.45$	1.5×0.4386 per via
		Others	0.4386 per via
Vyx	Landing on Myy/Myx	$L \leq 4.5$; any width	4×0.5275 per via
		$L > 4.5$; $w \geq 0.45$	2×0.5275 per via (array)
		$9 \geq L > 4.5$; $w \geq 0.45$	1.5×0.5275 Single via
		$9 \geq L > 4.5$; $w < 0.45$	1.5×0.5275 per via
		Others	0.5275 per via
Vyz	Landing on Myy/Myx/Myz	$L \leq 4.5$; any width	4×1.3012 per via
		$L > 4.5$; $w \geq 0.45$	2×1.3012 per via (array)
		$9 \geq L > 4.5$; $w \geq 0.45$	1.5×1.3012 Single via
		$9 \geq L > 4.5$; $w < 0.45$	1.5×1.3012 per via
		others	1.3012 per via

Interlevel connection	Via landing on Bottom Metal	Upper Metal Length, L (μm) & Width [drawn], w (μm)	I_{max} (mA)
Vz	Landing on My	$L \leq 4.5$; any width	4×2.0726 per via
		$9 \geq L > 4.5$; any width	1.5×2.0726 per via
		Others	2.0726 per via
	Landing on Myy	$L \leq 4.5$; any width	4×3.9879 per via
		$9 \geq L > 4.5$; any width	1.5×3.9879 per via
		Others	3.9879 per via
	Landing on Myx	$L \leq 4.5$; any width	4×4.8267 per via
		$9 \geq L > 4.5$; any width	1.5×4.8267 per via
		Others	4.8267 per via
Vr	Landing on Myz/Mz	$L \leq 4.5$; any width	4×5.0357 per via
		$9 \geq L > 4.5$; any width	1.5×5.0357 per via
		Others	5.0357 per via
	Landing on My	$L \leq 4.5$; any width	4×2.6317 per via
		$9 \geq L > 4.5$; any width	1.5×2.6317 per via
		Others	2.6317 per via
	Landing on Myy	$L \leq 4.5$; any width	4×5.0356 per via
		$9 \geq L > 4.5$; any width	1.5×5.0356 per via
		Others	5.0356 per via
	Landing on Myx	$L \leq 4.5$; any width	4×6.1702 per via
		$9 \geq L > 4.5$; any width	1.5×6.1702 per via
		Others	6.1702 per via
	Landing on Mr/Mz	$L \leq 4.5$; any width	4×8.1683 per via
		$9 \geq L > 4.5$; any width	1.5×8.1683 per via
		Others	8.1683 per via

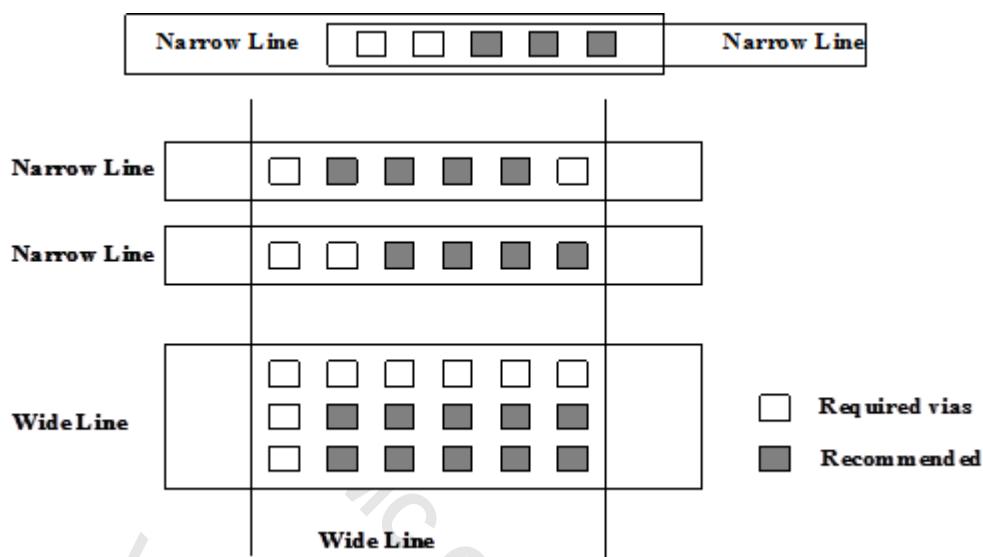
DC Operation, Required Number of Vias

(1) If space permits, it is preferable to have more vias than the EM rules require.

(2) At a minimum rule, the EM current rules require one via.

- (a) Example 1, if M0 is 0.020 μm and the current density is 1.5*1.271 mA/ μm ; that is, the current is $1.5 \times 1.271 \times (0.020 - 0.003) = 0.0324$ mA, only one VIA1 is necessary to ensure the reliability margin.
 - Example 2, if M2 is 0.020 μm and the current density is 1.5*1.184 mA/ μm ; that is, the current is $1.5 \times 1.184 \times (0.020 - 0.003) = 0.0302$ mA, only one VIA1 and one VIA2 are necessary to ensure the reliability margin.
- (3) To determine the required number of vias, please proceed as follow:
- From the DC current given in 10.4.5, determine the necessary line width (W-line);
 - Calculate the Maximum allowed I_{dc_line} for the given line width (W-line).
 - Calculate the required number of contacts or vias to carry line current I_{dc_line} : Number of vias = I_{dc_line} / I_{dc_via} .

Recommended Rule: The number of vias placed across a line (perpendicular to direction of current flow) must be maximized to increase reliability by providing redundancy in the case of blocked or resistive vias. (increases as much as the line width permits).



VIAI CPU Confidential Information
938214
10/05/2018

10.4.5.8 Maximum DC Current for MD/MP/VC

10.4.5.8.1 Maximum DC Current for MD, MP

The table provides the maximum allowed DC current, I_{max} for each of the MD, MP at junction temperature of 105°C and lifetime 10 years. In the table, w (in μm) represents the drawn width of the metal line and La (in μm) represents the overlap between MG(metal-gate) and MP or OD (drawn) and MD.

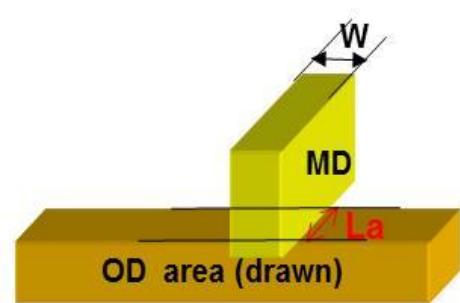
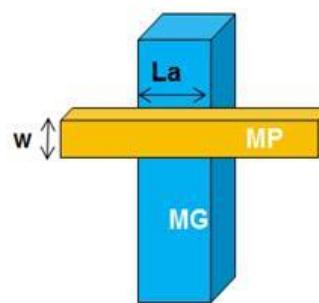
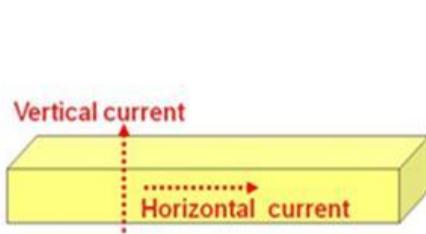
Use the Table 10.4.11 to calculate I_{max} if the junction temperature differs from 105°C.

Table 10.4.11

Temperature	100°C	105°C	110°C	115°C	120°C	125°C	130°C	135°C	140°C	145°C	150°C
Rating factor of I_{max}	1.073	1.000	0.927	0.855	0.782	0.710	0.637	0.565	0.492	0.419	0.347

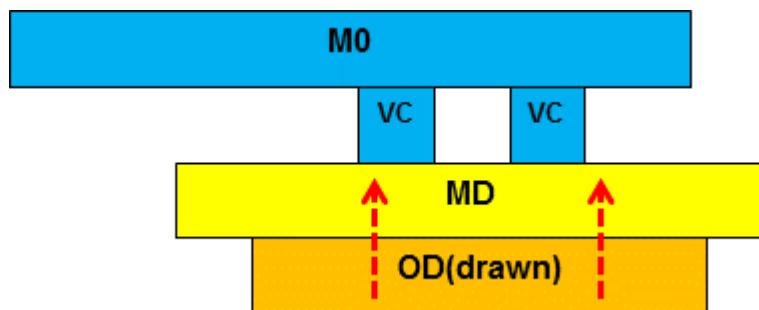
Table 10.4.12

Metal Wiring Level	I_{max} (mA)
MD (Vertical current)	$245.0 \times (w - 0.004) \times (La)$
MD (Horizontal current)	$10.046 \times (w - 0.004)$
MP (Vertical current)	$245.0 \times (w - 0.004) \times (La)$
MP (Horizontal current)	$4.465 \times (w - 0.004)$



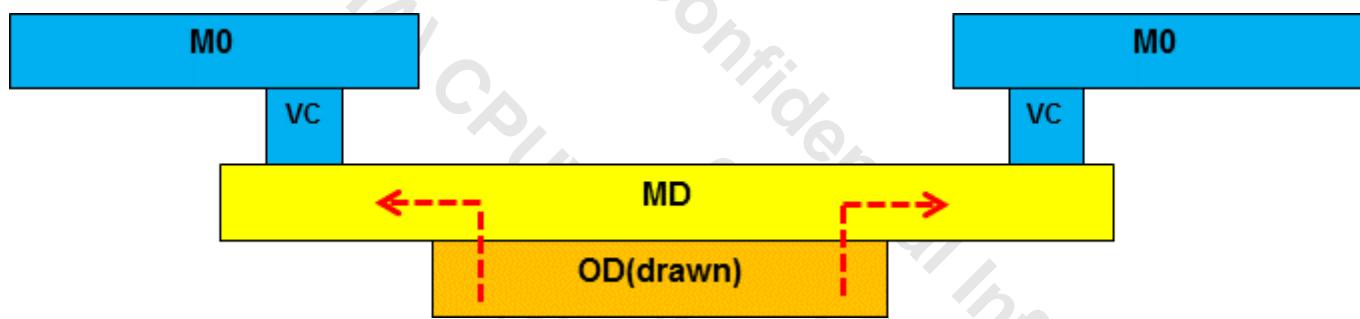
For example about vertical current vs horizontal current:

(1) Case-1



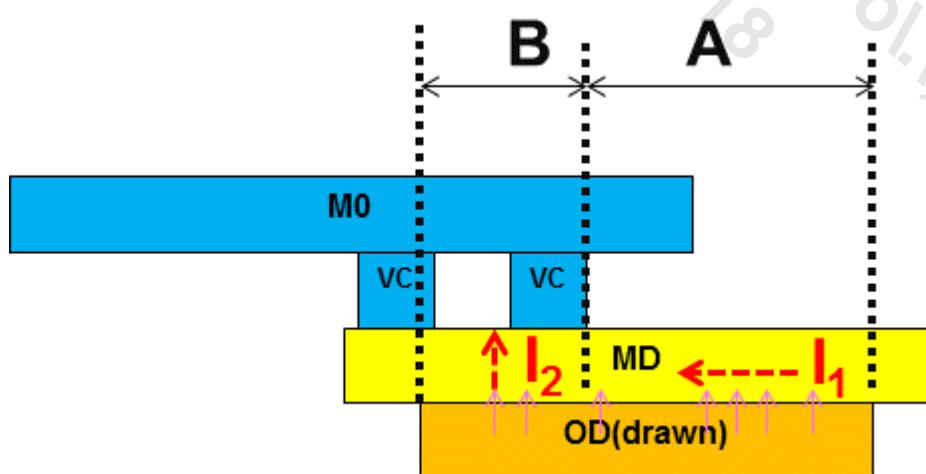
In device area, current from OD:
MD are vertical current.

(2) Case-2



MD is horizontal.

(3) Case-3



In this case, VC and MD are not 100% overlap,
Assume device total current is I_{total} ; MD can divide into two parts (A and B)
 I_1 in part-A (without VC overlap) : horizontal current, $I_1 = I_{total} * A / (A+B)$, follow horizontal rule
 I_2 in part-B (with VC overlap) : vertical current, $I_2 = I_{total}$, follow vertical rule

10.4.5.8.2 Maximum DC Current for VC

The table provides the maximum allowed DC current, I_{max} for VC at junction temperature of 105°C. In the table, w (in μm) represents the drawn width of the metal line L (in μm) represents the length of the metal line. Use the Table 10.4.1 to calculate I_{max} if the junction temperature differs from 105°C.

Table 10.4.13

Metal Wiring Level	MD/MP Length, L (μm), Width, W (μm)	Metal-0 Length, L (μm); Width [drawn], W (μm)	I_{max} (mA)
VC (0.016x0.016 μm^2) (0.020x0.020 μm^2)	Any length; any width	$L \leq 1$; Any width	0.2612 per via
	Any length; any width	$1 < L \leq 1.5$; Any width	0.2612 per via
	Any length; any width	$L > 1.5$; $0.04 \leq w \leq 0.12$	0.2612 per via
	Any length; any width	$L > 3 \mu\text{m}$; $W < 0.04 \mu\text{m}$	1.5×0.0564 per via
	Others	others	3×0.0564 per via
VC (0.02x0.04 μm^2) (0.016x0.056 μm^2)	Any length; any width	$L \leq 1$; Any width	0.2612 per via
	Any length; any width	$1 < L \leq 1.5$; Any width	0.2612 per via
	Any length; any width	$L > 1.5$; $0.04 \leq w \leq 0.12$	0.2612 per via
	Any length; any width	$L > 3 \mu\text{m}$; $W < 0.04 \mu\text{m}$	3×0.0564 per via
	Others	others	0.2612 per via
VC (0.02x0.064 μm^2)	Any length; any width	$L \leq 1$; Any width	0.2612 per via
	Any length; any width	$1 < L \leq 1.5$; Any width	0.2612 per via
	Any length; any width	$L > 1.5$; $0.04 \leq w \leq 0.12$	0.2612 per via
	Any length; any width	$L > 3 \mu\text{m}$; $W < 0.04 \mu\text{m}$	3.75×0.0564 per via
	Others	others	0.2612 per via
VC interact RH_TN (W=0.08 μm ; L=0.388~1.828 μm)			unchecked (EM is limited by RH_TN)

Table 10.4.14 (Downstream)

Metal Wiring Level	MD/MP Length, L (μm), Width, W (μm)	I_{max} (mA)
VC (0.016x0.016 μm^2) (0.020x0.020 μm^2)	Any length; Any width (both vertical & horizontal current)	0.2612 per via
VC (0.02x0.04 μm^2) (0.016x0.056 μm^2)	Any length; Any width (both vertical & horizontal current)	0.2612 per via
VC (0.02x0.064 μm^2)	Any length; Any width (both vertical & horizontal current)	0.2612 per via
VC interact RH_TN (W=0.08 μm ; L=0.388~1.828 μm)		unchecked (EM is limited by RH_TN)

Table 10.4.15 (Upstream)

Metal Wiring Level	Metal-0 Length, L (μm); Width, W [drawn] (μm)	I_{\max} (mA)
VC (0.016x0.016 μm^2) (0.020x0.020 μm^2)	$L \leq 1$; Any width	9×0.0564 per via
	$1 < L \leq 1.5$; Any width	6×0.0564 per via
	$L > 1.5$; $0.04 \leq w \leq 0.12$	6×0.0564 per via
	$L > 3 \mu\text{m}$; $W < 0.04 \mu\text{m}$	1.5×0.0564 per via
	others	3×0.0564 per via
VC (0.02x0.04 μm^2) (0.016x0.056 μm^2)	$L \leq 1$; Any width	18×0.0564 per via
	$1 < L \leq 1.5$; Any width	12×0.0564 per via
	$L > 1.5$; $0.04 \leq w \leq 0.12$	12×0.0564 per via
	$L > 3 \mu\text{m}$; $W < 0.04 \mu\text{m}$	3×0.0564 per via
	others	6×0.0564 per via
VC (0.02x0.064 μm^2)	$L \leq 1$; Any width	22.5×0.0564 per via
	$1 < L \leq 1.5$; Any width	15×0.0564 per via
	$L > 1.5$; $0.04 \leq w \leq 0.12$	15×0.0564 per via
	$L > 3 \mu\text{m}$; $W < 0.04 \mu\text{m}$	3.75×0.0564 per via
	others	7.5×0.0564 per via
VC interact RH_TN (W=0.08 μm ; L=0.388~1.828 μm)		unchecked (EM is limited by RH_TN)

10.4.6 AP RDL Current Density (EM) Specifications

10.4.6.1 Rating factor for maximum DC Current

Jmax is maximum DC current allowed per μm of AP RDL metal line width or per RV via. The number is based on 0.1% point of measurement data at 10% resistance increase after 10 years of continuous operation at 105°C. Use the following table to calculate I_{\max} if the junction temperature differs from 105°C.

Table 10.4.16

Temperature	85°C	90°C	95°C	100°C	105°C	110°C	115°C	120°C	125°C	130°C	135°C	140°C	145°C	150°C
Rating factor of Imax	1.563	1.41	1.273	1.151	1.000	0.872	0.758	0.664	0.583	0.514	0.454	0.403	0.358	0.319

For example, J_{max} (at 125°C) = 0.583 × J_{max} (at 105°C).

If the junction temperature is below 85°C, please use the rating factor (1.563) at 85°C or contact with TSMC reliability.

10.4.6.2 Maximum DC Current for AP RDL Metal Lines ($T_j = 105^\circ\text{C}$)

The table provides the maximum allowed DC current, I_{max} for AP RDL metal wiring at junction temperature of 105°C. In the table, w (in μm) represents the drawn width of the metal line.

Table 10.4.17

Metal Wiring Level	I_{max} (mA)
AP RDL(28kA)	$7.118 \times w$
AP RDL(14.5 kA)	$3.688 \times w$

10.4.6.3 Maximum DC Current for RDL Via (RV) ($T_j = 105^\circ\text{C}$)

The table provides the maximum allowed DC current, I_{max} for RV at junction temperature of 105°C. In the table, the sizes of contact and via are also noted.

Table 10.4.18

Interlevel Connection	I_{max} (mA)	Drawn Size
RV	14.94	per RV

Note : CB layer and CBD layer apply un-check EM rule.

10.4.7 Cu & AP-RDL Metal AC Operation

10.4.7.1 Pulsed Signal Terminology

The general terminology for a pulsed DC or AC signal is:

Period (τ)

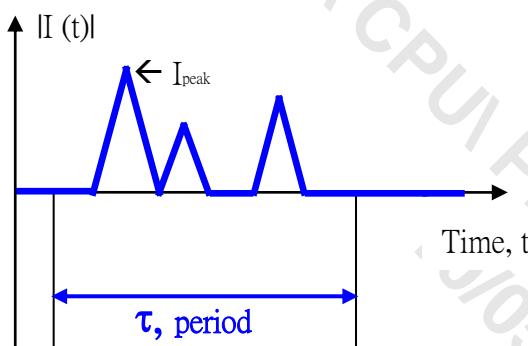
Duration (t_D)

The definition of I_{peak} is:

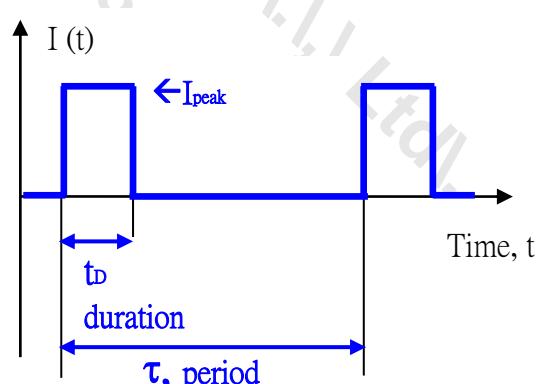
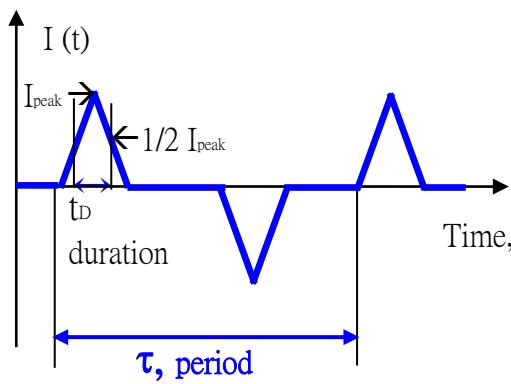
$$I_{peak} = \max (|I(t)|)$$

In general, there are multiple peak current with different peak value in one period. The equivalent duration (t_D) for multiple peak current is defined as:

$$t_D = \left[\left(\int_0^\tau |I(t)| dt \right) / I_{peak} \right]$$



If there is only one pulse in one period, for your convenience, you could measure at half of the I_{peak} to define the duration (t_D).



Average Value of the Current

I_{avg} is the average value of the current, which is the effective DC current. Therefore, I_{avg} rules are identical to I_{max} rules. Please refer to the DC EM sections. The temperature de-rating table is also applicable to the I_{avg} rule for a junction temperature different from 105°C.

The definition of I_{avg} is:

$$I_{avg} = \left[\left(\int_0^{\tau} I(t) dt \right) / \tau \right]$$

If the duration time t_D is longer than 10 ms, we can treat it like the DC case. The period when the signal is “ON” is similar to that of DC EM stress, and the maximum level of the signal should follow the EM maximum DC rule. i.e. for longer duration time t_D , it is similar to the DC case. However, this condition is not applicable to the definition of I_{avg} (average current over the τ period).

10.4.7.1.1 Recommendation of AC EM on short length rule

In the EM short length relaxation rule, the I_{max_DC} increases by 3 times as the metal length becomes $\leq 3 \mu m$ (Table 10.4.3.). However, this short length benefit will be reduced when the maximum current density is very high. So, for additional safety, short length EM relaxation rules are not recommended when AC duty cycle (r) ≤ 0.1 .

10.4.7.2 Root-Mean-Square Current

I_{rms} is the root-mean-square of the current through a metal line. The definition of I_{rms} is:

$$I_{rms} = \left[\left(\int_0^{\tau} I(t)^2 dt \right) / \tau \right]^{1/2}$$

The following tables provide the I_{rms} for each of the metal wiring levels at a junction temperature of 105°C. In the table, w (in μm) represents the drawn width of the metal line and ΔT (°C) is the temperature rise due to Joule heating.

Note to use I_{rms} ΔT limitation:

The I_{rms} rule relates to the heat or Joule-heating of metal lines. Delta_T is the metal line temperature increase and is raised when current passes through it. The more current passes through the metal line, the more heat is generated. This causes the metal line temperatures to increase. As a result, I_{rms} is a factor of delta_T, and $I_{rms}=0$ if delta_T=0 because obviously, no current means no heat. If delta_T increases too much, the heat will flow to neighboring metal lines causing neighboring metal line temperatures to increase. Table 10.4.19 provides a guide to the effects of increases in temperature on neighboring lines, when DC current is applied. These temperature increases will cause degradation in EM lifetime. Consequently, Table 10.4.19 shows DC EM lifetime degradation rather than I_{rms} . EM lifetime is a function of temperature and current density and higher temperatures will cause degradation of EM lifetime. As a result, it is recommended that temperature increase is limited to < 5 °C. As a temperature increase of this amount is sufficient to degrade the EM lifetime by about 30%.

Table 10.4.19

ΔT	Temp	TTF
	105C	1
5C	110C	0.697
10C	115C	0.491
15C	120C	0.349
20C	125C	0.250
30C	135C	0.131

Notes for I_{rms} temperature de-rating factor:

1. No temperature de-rating factor for I_{rms} tables listed below. Please apply the same table for the different environment temperatures $T=90^\circ\text{C}$ or 150°C .
2. The delta_T induced by joule-heating is the local temperature on the metal line when the current passes through it. For example, when delta_T=5°C, caused by joule-heating of the metal line, if the environment temperature=105°C, then the final metal line temperature=105+5=110°C. While the environment temperature=95°C, the final metal line temperature=95+5=100°C.

Please note:

In following I_{rms} tables, the Mx, and Mxa, can be replaced each other because metal thickness is identical.

10.4.7.2.1 Rating factor for I_{rms} current at different Contact/Via spacing

I_{rms} is the rule, which can be used to estimate the joule-heating effect of metal lines (metal line here means M0 or higher than M0, not for MD or MP layers), based on the worst power density and without heat dissipation through via to the lower metal level and Si-substrate. The effect of vias, as efficient heat conduction paths, is considered for realistic situations. Use the following table to calculate the rating factor of I_{rms} if the via to via spacing is less than 10 μm and either two contacts or one side contact connect to substrate.

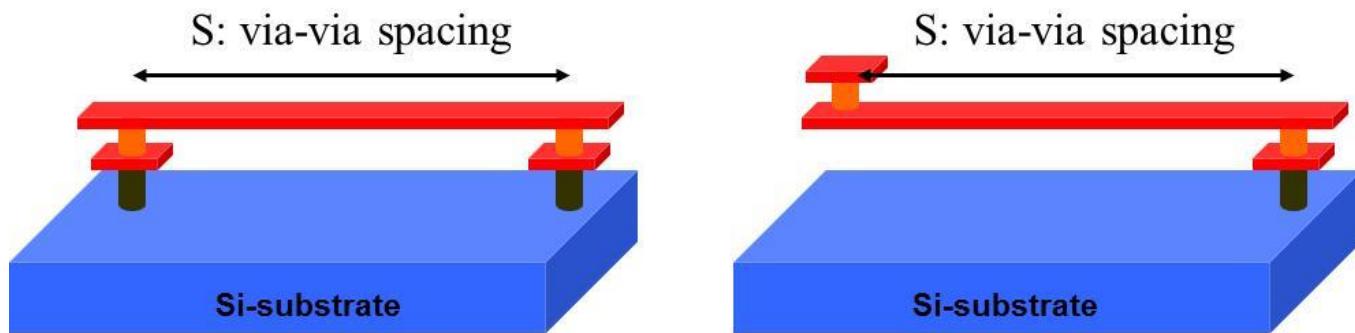


Table 10.4.20

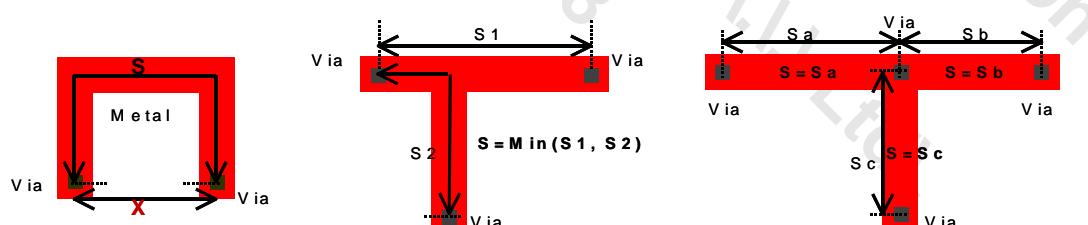
Via-Via spacing (S)	$S \geq 10 \mu\text{m}$	$10 \mu\text{m} > S > 3 \mu\text{m}$	$3 \mu\text{m} \geq S > 1 \mu\text{m}$	$1 \mu\text{m} \geq S > 0.3 \mu\text{m}$	$0.3 \mu\text{m} \geq S$
Rating factor of I_{rms}	1.0	1.05	1.3	2.0	2.2

For example, I_{rms} ($3 > S > 1 \mu\text{m}$) = $1.3 \times I_{rms}$.

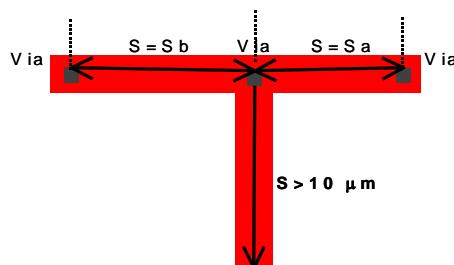
Please note: these rating factors of I_{rms} cannot be applied to MD and MP layers.

For more specific via-via spacing definitions, please refer to below examples.

Examples for via-via spacing.



If the metal wire has only one via, we treat it like via-via spacing $S > 10$, the rating factor=1.

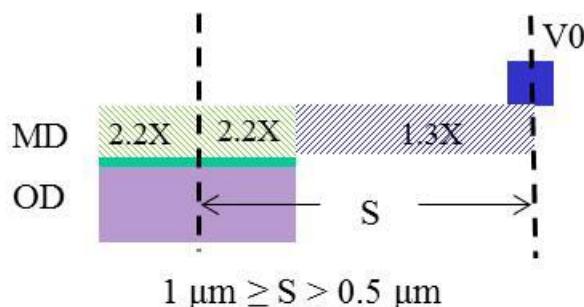
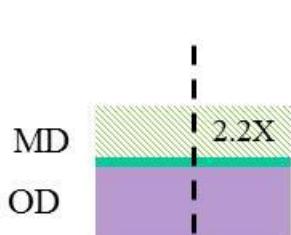
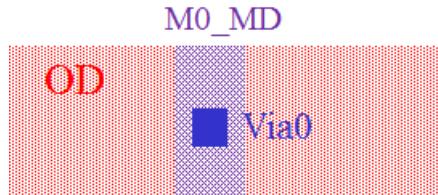
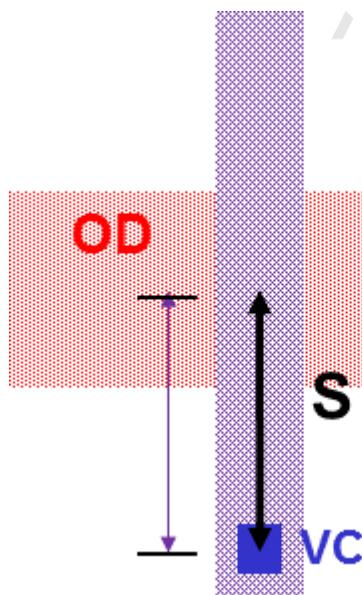


10.4.7.2.2 Rating factor for I_{rms} current at different MD length

If MD connects to OD, heat can be dissipated through OD layer to Si-substrate, as efficient heat conduction paths. Rating factor of I_{rms} of MD on OD is 2.2X as MD within OD. When MD segment locates outside OD, please use the following table to apply the rating factor of I_{rms} if the MD length(S) is less than 4 μm . Length (S) is center of VC to center of OD.

Table 10.4.21

MD length (S)	$4 \mu\text{m} \geq S > 1 \mu\text{m}$	$1 \mu\text{m} \geq S > 0.5 \mu\text{m}$	$0.5 \mu\text{m} \geq S > 0.3 \mu\text{m}$	$0.3 \mu\text{m} \geq S$
Rating factor of I_{rms}	1.0	1.3	2.0	2.2

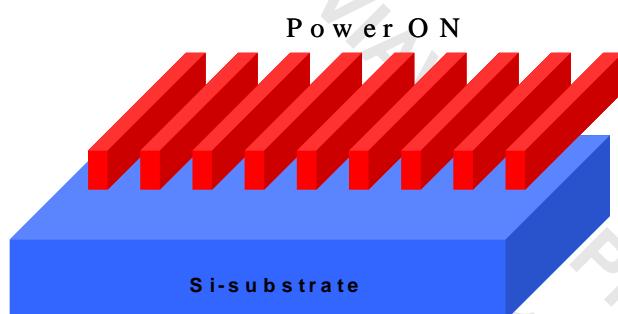


10.4.7.2.3 Rating factors for I_{rms} current at specific metal line number

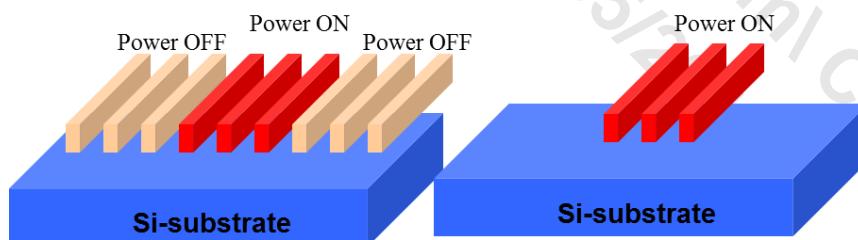
The worst-case scenario of joule-heating is shown when signals' current passes through all metal lines (minimum spacing of each metal line) at the same time. This is due to heat only dissipating through low-k to the substrate and coupling heat generating from surrounding lines. Use the following table to calculate the rating factor of I_{rms} if the metal line number is known (metal line here means M0 or higher than M0, not for MD or MP layers).

The example of rating factor application, check the metal line number for each layer in advance, choose the rating factor based on below table to fit your chip layout conditions, and then use this factor as a global factor in I_{rms} relaxation for specific layer.

Case 1: dense metal lines, metal lines no. N=9



Case 2: dense metal lines, metal lines no. N=3



Case 3: dense metal lines, power ON metal lines no. N=1 or neighboring power ON lines is far away $>12*(W+S)$, we can treat it like N=1.

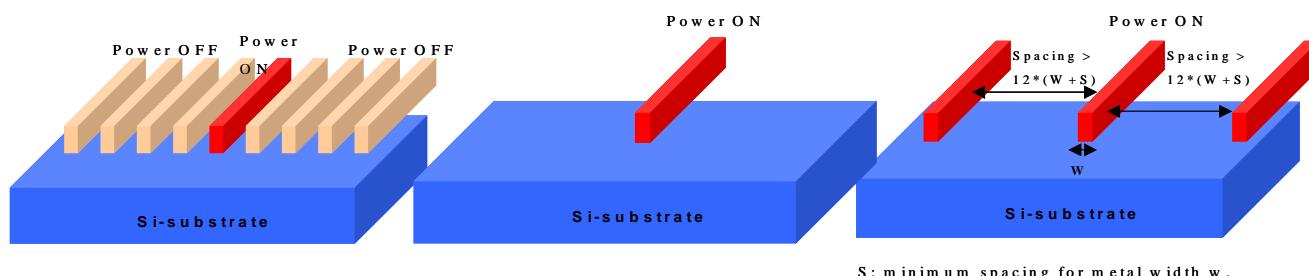


Table 10.4.22

Metal lines no. (N)	$N \geq 9$	$9 > N \geq 5$	$5 > N \geq 3$	$3 > N \geq 1$
Rating factor of I_{rms}	1.0	1.05	1.32	1.5

For example, $I_{rms} (5 > N \geq 3) = 1.32 \times I_{rms}$.

Please note: these rating factors of I_{rms} cannot be applied to MD and MP layers.

Examples for overall I_{rms} rating factor estimation:

The I_{rms} or thermal analysis area has three metal lines flowing current at the same time, $N=3$, rating factor=1.32, via to via spacing for each metal line is less than 3 μm , rating factor=1.3, the total rating factor will be $=1.32*1.3=1.716$.

10.4.7.2.4 Root-Mean-Square Current for LK Dielectrics (1Xs 1Xa 1Ya 5Y 2YY 2Z process)

Table 10.4.24 apply to 1P13M process.

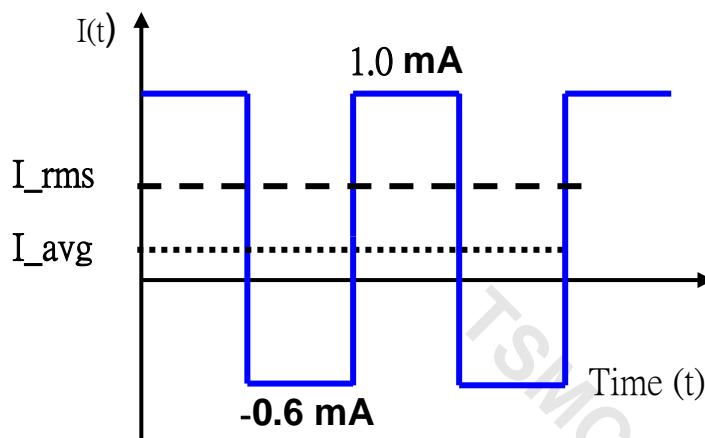
Metal level	Metal process	I_{rms} (mA), effective W
MD	MD	Sqrt [3.01 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.185) / (w - 0.004 + 0.0443)]
MP	MP	Sqrt [1.29 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.216) / (w - 0.004 + 0.0443)]
M0	M0	Sqrt [3.29 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.216) / (w - 0.003 + 0.0443)]
M1	M1	Sqrt [4.16 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.145) / (w - 0.003 + 0.0443)]
M2	Mxs_1	Sqrt [3.06 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.217) / (w - 0.003 + 0.0443)]
M3	Mxa_1	Sqrt [2.27 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.293) / (w - 0.003 + 0.0443)]
M4	Mya_1	Sqrt [2.26 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.383) / (w - 0.003 + 0.0443)]
M5	My_1	Sqrt [2.48 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.499) / (w - 0.004 + 0.0443)]
M6	My_2	Sqrt [1.95 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.635) / (w - 0.004 + 0.0443)]
M7	My_3	Sqrt [1.60 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.771) / (w - 0.004 + 0.0443)]
M8	My_4	Sqrt [1.36 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.908) / (w - 0.004 + 0.0443)]
M9	My_5	Sqrt [1.19 × Δ T × (w - 0.004) ² × (w - 0.004 + 1.044) / (w - 0.004 + 0.0443)]
M10	Myy_1	Sqrt [1.93 × Δ T × (w - 0.008) ² × (w - 0.008 + 1.203) / (w - 0.008 + 0.0443)]
M11	Myy_2	Sqrt [1.63 × Δ T × (w - 0.008) ² × (w - 0.008 + 1.423) / (w - 0.008 + 0.0443)]
M12	Mz_1	Sqrt [7.76 × Δ T × (w - 0.020) ² × (w - 0.020 + 1.694) / (w - 0.020 + 0.0443)]
M13	Mz_2	Sqrt [6.47 × Δ T × (w - 0.020) ² × (w - 0.020 + 2.033) / (w - 0.020 + 0.0443)]

Table 10.4.25 Example Root-Mean-Square Current for $\Delta T = 5^\circ C$

Metal level	Metal process	I_{rms} (mA), effective W
MD	MD	Sqrt [15.05 $\times (w - 0.004)^2 \times (w - 0.004 + 0.185) / (w - 0.004 + 0.0443)$]
MP	MP	Sqrt [6.45 $\times (w - 0.004)^2 \times (w - 0.004 + 0.216) / (w - 0.004 + 0.0443)$]
M0	M0	Sqrt [16.45 $\times (w - 0.003)^2 \times (w - 0.003 + 0.216) / (w - 0.003 + 0.0443)$]
M1	M1	Sqrt [20.80 $\times (w - 0.003)^2 \times (w - 0.003 + 0.145) / (w - 0.003 + 0.0443)$]
M2	Mxs_1	Sqrt [15.30 $\times (w - 0.003)^2 \times (w - 0.003 + 0.217) / (w - 0.003 + 0.0443)$]
M3	Mxa_1	Sqrt [11.35 $\times (w - 0.003)^2 \times (w - 0.003 + 0.293) / (w - 0.003 + 0.0443)$]
M4	Mya_1	Sqrt [11.30 $\times (w - 0.003)^2 \times (w - 0.003 + 0.383) / (w - 0.003 + 0.0443)$]
M5	My_1	Sqrt [12.40 $\times (w - 0.004)^2 \times (w - 0.004 + 0.499) / (w - 0.004 + 0.0443)$]
M6	My_2	Sqrt [9.75 $\times (w - 0.004)^2 \times (w - 0.004 + 0.635) / (w - 0.004 + 0.0443)$]
M7	My_3	Sqrt [8.00 $\times (w - 0.004)^2 \times (w - 0.004 + 0.771) / (w - 0.004 + 0.0443)$]
M8	My_4	Sqrt [6.80 $\times (w - 0.004)^2 \times (w - 0.004 + 0.908) / (w - 0.004 + 0.0443)$]
M9	My_5	Sqrt [5.95 $\times (w - 0.004)^2 \times (w - 0.004 + 1.044) / (w - 0.004 + 0.0443)$]
M10	Myy_1	Sqrt [9.65 $\times (w - 0.008)^2 \times (w - 0.008 + 1.203) / (w - 0.008 + 0.0443)$]
M11	Myy_2	Sqrt [8.15 $\times (w - 0.008)^2 \times (w - 0.008 + 1.423) / (w - 0.008 + 0.0443)$]
M12	Mz_1	Sqrt [38.80 $\times (w - 0.020)^2 \times (w - 0.020 + 1.694) / (w - 0.020 + 0.0443)$]
M13	Mz_2	Sqrt [32.35 $\times (w - 0.020)^2 \times (w - 0.020 + 2.033) / (w - 0.020 + 0.0443)$]

Examples for I_{rms} and I_{avg} estimation:

The wave form in signal line is shown in below fig. (Duty ratio=0.5, duration time << 10 msec, I_{avg} is applicable.)



1. I_{avg} is calculated as follows:

$$I_{avg} = \left(\frac{1.0 \times 0.5 - 0.6 \times 0.5}{1} \right) = 0.2 \text{ mA} . \text{ We assume M2 layer and width}=0.10 \mu\text{m, so the } I_{max} \text{ is}$$

$$I_{max} = 4 \times 1.184 (0.10 - 0.003) = 0.4594 \text{ mA} . I_{avg} < I_{max}, \text{ so the wave form of the signal line meets the } I_{max} \text{ rule.}$$

2. I_{rms} is calculated as follows:

$$I_{rms} = \sqrt{\frac{1^2 \times 0.5 + (-0.6)^2 \times 0.5}{1}} = 0.8246 \text{ mA} . \text{ Knowing that M2 } w=0.10 \mu\text{m and } I_{rms}=0.8246 \text{ mA, put these values in the } I_{rms} \text{ table.}$$

$$I_{rms} = 0.8246 = \sqrt{3.06 \times \Delta T \times (0.1 - 0.003)^2 \times (0.1 - 0.003 + 0.217) / (0.1 - 0.003 + 0.0443)} , \text{ delta_T can be estimated to be } \Delta T=10.63^\circ\text{C.}$$

3. For the EM lifetime of the signal line, the joule-heating-induced degradation needs to be considered because $\Delta T=10.63^\circ\text{C}$ is higher than 5°C . The temperature de-rating factor is 0.47. The lifetime of the signal line will be $10\text{-years} \times (0.47)=4.7\text{-years}$.
4. Since the signal line delta_T increases too much, the heat will flow to neighboring metal lines causing neighboring metal line temperatures to increase. Table 10.4.19 provides a guide to the effects of increases in temperature on neighboring lines when DC current is applied.

10.4.7.2.5 Root-Mean-Square Current for LK Dielectrics (1Xs 1X 1Ya 6Y 2Z process)

Table 10.4.24 apply to 1P13M process.

Metal level	Metal process	I_{rms} (mA), effective W
MD	MD	Sqrt [3.01 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.185) / (w - 0.004 + 0.0443)]
MP	MP	Sqrt [1.29 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.216) / (w - 0.004 + 0.0443)]
M0	M0	Sqrt [3.29 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.216) / (w - 0.003 + 0.0443)]
M1	M1	Sqrt [4.16 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.145) / (w - 0.003 + 0.0443)]
M2	Mxs_1	Sqrt [3.06 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.217) / (w - 0.003 + 0.0443)]
M3	Mx_1	Sqrt [2.27 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.293) / (w - 0.003 + 0.0443)]
M4	Mya_1	Sqrt [2.26 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.383) / (w - 0.003 + 0.0443)]
M5	My_1	Sqrt [2.48 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.499) / (w - 0.004 + 0.0443)]
M6	My_2	Sqrt [1.95 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.635) / (w - 0.004 + 0.0443)]
M7	My_3	Sqrt [1.60 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.771) / (w - 0.004 + 0.0443)]
M8	My_4	Sqrt [1.36 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.908) / (w - 0.004 + 0.0443)]
M9	My_5	Sqrt [1.19 × Δ T × (w - 0.004) ² × (w - 0.004 + 1.044) / (w - 0.004 + 0.0443)]
M10	My_6	Sqrt [1.05 × Δ T × (w - 0.004) ² × (w - 0.004 + 1.181) / (w - 0.004 + 0.0443)]
M11	Mz_1	Sqrt [9.45 × Δ T × (w - 0.020) ² × (w - 0.020 + 1.391) / (w - 0.020 + 0.0443)]
M12	Mz_2	Sqrt [7.60 × Δ T × (w - 0.020) ² × (w - 0.020 + 1.730) / (w - 0.020 + 0.0443)]

10.4.7.2.6 Root-Mean-Square Current for LK Dielectrics (1Xs 1Xa 1Ya 5Y 1YY 2Z process)

Table 10.4.24 apply to 1P13M process.

Metal level	Metal process	I_{rms} (mA), effective W
MD	MD	Sqrt [3.01 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.185) / (w - 0.004 + 0.0443)]
MP	MP	Sqrt [1.29 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.216) / (w - 0.004 + 0.0443)]
M0	M0	Sqrt [3.29 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.216) / (w - 0.003 + 0.0443)]
M1	M1	Sqrt [4.16 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.145) / (w - 0.003 + 0.0443)]
M2	Mxs_1	Sqrt [3.06 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.217) / (w - 0.003 + 0.0443)]
M3	Mxa_1	Sqrt [2.27 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.293) / (w - 0.003 + 0.0443)]
M4	Mya_1	Sqrt [2.26 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.383) / (w - 0.003 + 0.0443)]
M5	My_1	Sqrt [2.48 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.499) / (w - 0.004 + 0.0443)]
M6	My_2	Sqrt [1.95 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.635) / (w - 0.004 + 0.0443)]
M7	My_3	Sqrt [1.60 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.771) / (w - 0.004 + 0.0443)]
M8	My_4	Sqrt [1.36 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.908) / (w - 0.004 + 0.0443)]
M9	My_5	Sqrt [1.19 × Δ T × (w - 0.004) ² × (w - 0.004 + 1.044) / (w - 0.004 + 0.0443)]
M10	Myy_1	Sqrt [1.93 × Δ T × (w - 0.008) ² × (w - 0.008 + 1.203) / (w - 0.008 + 0.0443)]
M11	Mz_1	Sqrt [8.92 × Δ T × (w - 0.020) ² × (w - 0.020 + 1.474) / (w - 0.020 + 0.0443)]
M12	Mz_2	Sqrt [7.25 × Δ T × (w - 0.020) ² × (w - 0.020 + 1.813) / (w - 0.020 + 0.0443)]

10.4.7.2.7 Root-Mean-Square Current for LK Dielectrics (1Xs 1X 1Ya 3Y 2Z process)

Table 10.4.24 apply to 1P9M process.

Metal level	Metal process	I_{rms} (mA), effective W
MD	MD	Sqrt [3.01 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.185) / (w - 0.004 + 0.0443)]
MP	MP	Sqrt [1.29 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.216) / (w - 0.004 + 0.0443)]
M0	M0	Sqrt [3.29 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.216) / (w - 0.003 + 0.0443)]
M1	M1	Sqrt [4.16 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.145) / (w - 0.003 + 0.0443)]
M2	Mxs_1	Sqrt [3.06 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.217) / (w - 0.003 + 0.0443)]
M3	Mx_1	Sqrt [2.27 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.293) / (w - 0.003 + 0.0443)]
M4	Mya_1	Sqrt [2.26 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.383) / (w - 0.003 + 0.0443)]
M5	My_1	Sqrt [2.48 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.499) / (w - 0.004 + 0.0443)]
M6	My_2	Sqrt [1.95 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.635) / (w - 0.004 + 0.0443)]
M7	My_3	Sqrt [1.60 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.771) / (w - 0.004 + 0.0443)]
M8	Mz_1	Sqrt [13.40 × Δ T × (w - 0.020) ² × (w - 0.020 + 0.981) / (w - 0.020 + 0.0443)]
M9	Mz_2	Sqrt [9.96 × Δ T × (w - 0.020) ² × (w - 0.020 + 1.321) / (w - 0.020 + 0.0443)]

10.4.7.2.8 Root-Mean-Square Current for LK Dielectrics (1Xs 1Xa 1Ya 5Y 2 YY 2YX 2R process)

Table 10.4.24 apply to 1P15M process.

Metal level	Metal process	I_{rms} (mA), effective W
MD	MD	Sqrt [3.01 $\times \Delta T \times (w - 0.004)^2 \times (w - 0.004 + 0.185) / (w - 0.004 + 0.0443)]$
MP	MP	Sqrt [1.29 $\times \Delta T \times (w - 0.004)^2 \times (w - 0.004 + 0.216) / (w - 0.004 + 0.0443)]$
M0	M0	Sqrt [3.29 $\times \Delta T \times (w - 0.003)^2 \times (w - 0.003 + 0.216) / (w - 0.003 + 0.0443)]$
M1	M1	Sqrt [4.16 $\times \Delta T \times (w - 0.003)^2 \times (w - 0.003 + 0.145) / (w - 0.003 + 0.0443)]$
M2	Mxs_1	Sqrt [3.06 $\times \Delta T \times (w - 0.003)^2 \times (w - 0.003 + 0.217) / (w - 0.003 + 0.0443)]$
M3	Mxa_1	Sqrt [2.27 $\times \Delta T \times (w - 0.003)^2 \times (w - 0.003 + 0.293) / (w - 0.003 + 0.0443)]$
M4	Mya_1	Sqrt [2.26 $\times \Delta T \times (w - 0.003)^2 \times (w - 0.003 + 0.383) / (w - 0.003 + 0.0443)]$
M5	My_1	Sqrt [2.48 $\times \Delta T \times (w - 0.004)^2 \times (w - 0.004 + 0.499) / (w - 0.004 + 0.0443)]$
M6	My_2	Sqrt [1.95 $\times \Delta T \times (w - 0.004)^2 \times (w - 0.004 + 0.635) / (w - 0.004 + 0.0443)]$
M7	My_3	Sqrt [1.60 $\times \Delta T \times (w - 0.004)^2 \times (w - 0.004 + 0.771) / (w - 0.004 + 0.0443)]$
M8	My_4	Sqrt [1.36 $\times \Delta T \times (w - 0.004)^2 \times (w - 0.004 + 0.908) / (w - 0.004 + 0.0443)]$
M9	My_5	Sqrt [1.19 $\times \Delta T \times (w - 0.004)^2 \times (w - 0.004 + 1.044) / (w - 0.004 + 0.0443)]$
M10	Myy_1	Sqrt [1.93 $\times \Delta T \times (w - 0.008)^2 \times (w - 0.008 + 1.203) / (w - 0.008 + 0.0443)]$
M11	Myy_2	Sqrt [1.63 $\times \Delta T \times (w - 0.008)^2 \times (w - 0.008 + 1.423) / (w - 0.008 + 0.0443)]$
M12	Myx_1	Sqrt [2.86 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 1.409) / (w - 0.020 + 0.0443)]$
M13	Myx_2	Sqrt [2.41 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 1.665) / (w - 0.020 + 0.0443)]$
M14	Mr_1	Sqrt [9.50 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.035) / (w - 0.020 + 0.0443)]$
M15	Mr_2	Sqrt [7.83 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.469) / (w - 0.020 + 0.0443)]$

10.4.7.2.9 Root-Mean-Square Current for LK Dielectrics (1Xs 1X 1Ya 4Y 1Z process)

Table 10.4.25 apply to 1P9M process.

Metal level	Metal process	I_{rms} (mA), effective W
MD	MD	Sqrt [3.01 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.185) / (w - 0.004 + 0.0443)]
MP	MP	Sqrt [1.29 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.216) / (w - 0.004 + 0.0443)]
M0	M0	Sqrt [3.29 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.216) / (w - 0.003 + 0.0443)]
M1	M1	Sqrt [4.16 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.145) / (w - 0.003 + 0.0443)]
M2	Mxs_1	Sqrt [3.06 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.217) / (w - 0.003 + 0.0443)]
M3	Mx_1	Sqrt [2.27 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.293) / (w - 0.003 + 0.0443)]
M4	Mya_1	Sqrt [2.26 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.383) / (w - 0.003 + 0.0443)]
M5	My_1	Sqrt [2.48 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.499) / (w - 0.004 + 0.0443)]
M6	My_2	Sqrt [1.95 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.635) / (w - 0.004 + 0.0443)]
M7	My_3	Sqrt [1.60 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.771) / (w - 0.004 + 0.0443)]
M8	My_4	Sqrt [1.36 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.908) / (w - 0.004 + 0.0443)]
M9	Mz_1	Sqrt [11.76 × Δ T × (w - 0.020) ² × (w - 0.020 + 1.118) / (w - 0.020 + 0.0443)]

10.4.7.2.10 Root-Mean-Square Current for LK Dielectrics (1Xs 1X 1Ya 7Y 2Z process)

Table 10.4.26 apply to 1P13M process.

Metal level	Metal process	I_{rms} (mA), effective W
MD	MD	Sqrt [3.01 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.185) / (w - 0.004 + 0.0443)]
MP	MP	Sqrt [1.29 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.216) / (w - 0.004 + 0.0443)]
M0	M0	Sqrt [3.29 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.216) / (w - 0.003 + 0.0443)]
M1	M1	Sqrt [4.16 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.145) / (w - 0.003 + 0.0443)]
M2	Mxs_1	Sqrt [3.06 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.217) / (w - 0.003 + 0.0443)]
M3	Mx_1	Sqrt [2.27 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.293) / (w - 0.003 + 0.0443)]
M4	Mya_1	Sqrt [2.26 × Δ T × (w - 0.003) ² × (w - 0.003 + 0.383) / (w - 0.003 + 0.0443)]
M5	My_1	Sqrt [2.48 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.499) / (w - 0.004 + 0.0443)]
M6	My_2	Sqrt [1.95 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.635) / (w - 0.004 + 0.0443)]
M7	My_3	Sqrt [1.60 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.771) / (w - 0.004 + 0.0443)]
M8	My_4	Sqrt [1.36 × Δ T × (w - 0.004) ² × (w - 0.004 + 0.908) / (w - 0.004 + 0.0443)]
M9	My_5	Sqrt [1.19 × Δ T × (w - 0.004) ² × (w - 0.004 + 1.044) / (w - 0.004 + 0.0443)]
M10	My_6	Sqrt [1.05 × Δ T × (w - 0.004) ² × (w - 0.004 + 1.181) / (w - 0.004 + 0.0443)]
M11	My_7	Sqrt [0.94 × Δ T × (w - 0.004) ² × (w - 0.004 + 1.317) / (w - 0.004 + 0.0443)]
M12	Mz_1	Sqrt [8.61 × Δ T × (w - 0.020) ² × (w - 0.020 + 1.527) / (w - 0.020 + 0.0443)]

M13

Mz_2

Sqrt [7.05 × Δ T × (w - 0.020)² × (w - 0.020 + 1.866) / (w - 0.020 + 0.0443)]

10.4.7.3 Peak Current

$$I_{\text{peak}} = \max (|I(t)|)$$

I_{peak} is the current at which a metal line undergoes excessive Joule heating and can begin to melt. This current should be used infrequently.

The limit for the peak current, I_{peak} , can be calculated by using the following formula:

$$I_{\text{peak}} = \frac{I_{\text{peak_DC}}}{\sqrt{r}}$$

$$r = \frac{t_D}{\tau}$$

r is the duty ratio, which is equal to the pulse duration divided by the period,

where $I_{\text{peak_DC}}$ is provided in the following table. In the table, w (in μm) represents the drawn width of the metalline and La (in μm) represents the overlap between MG(metal-gate) and MP or OD (drawn) and MD.

Note : the above equation is only applicable for frequency larger than 1 MHz and r larger than 0.01. If r is smaller than 0.01, please let $r=0.01$ in above I_{peak} equation.

Table 10.4.48

Metal process	Pulse duration (t_D)	Duty ratio (r)	$I_{\text{peak}} (\text{mA})$ ($w \geq 0.13 \mu\text{m}$ for dummy MD/MP)	$I_{\text{peak}} (\text{mA})$ ($w [\text{drawn}] < 0.1 \mu\text{m}$)
MD (horizontal)	$t_D \geq 0.5 \mu\text{s}$	any	$7.92 \times (w - 0.004)$	$15.84 \times (w - 0.004)$
	$1 \text{ ns} \leq t_D < 0.5 \mu\text{s}$	$r \geq 0.01$	$7.92 \times (w - 0.004)/(r)^{0.5}$	$15.84 \times (w - 0.004)/(r)^{0.5}$
	$1 \text{ ns} \leq t_D < 0.5 \mu\text{s}$	$r < 0.01$	$7.92 \times (w - 0.004)/(0.01)^{0.5}$	$15.84 \times (w - 0.004)/(0.01)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$19.00 \times (w - 0.004)/(r)^{0.5}$	$57.02 \times (w - 0.004)/(r)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$19.00 \times (w - 0.004)/(0.01)^{0.5}$	$57.02 \times (w - 0.004)/(0.01)^{0.5}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$31.68 \times (w - 0.004)/(r)^{0.5}$	$95.04 \times (w - 0.004)/(r)^{0.5}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$39.60 \times (w - 0.004)/(0.01)^{0.5}$	$158.4 \times (w - 0.004)/(0.01)^{0.5}$
MP (horizontal)	$t_D \geq 0.5 \mu\text{s}$	any	$3.92 \times (w - 0.004)$	$7.92 \times (w - 0.004)$
	$1 \text{ ns} \leq t_D < 0.5 \mu\text{s}$	$r \geq 0.01$	$3.92 \times (w - 0.004)/(r)^{0.5}$	$7.92 \times (w - 0.004)/(r)^{0.5}$
	$1 \text{ ns} \leq t_D < 0.5 \mu\text{s}$	$r < 0.01$	$3.92 \times (w - 0.004)/(0.01)^{0.5}$	$7.92 \times (w - 0.004)/(0.01)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$9.50 \times (w - 0.004)/(r)^{0.5}$	$28.51 \times (w - 0.004)/(r)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$9.50 \times (w - 0.004)/(0.01)^{0.5}$	$28.51 \times (w - 0.004)/(0.01)^{0.5}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$15.84 \times (w - 0.004)/(r)^{0.5}$	$47.52 \times (w - 0.004)/(r)^{0.5}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$19.80 \times (w - 0.004)/(0.01)^{0.5}$	$79.2 \times (w - 0.004)/(0.01)^{0.5}$
MD (vertical)	$t_D \geq 0.5 \mu\text{s}$	any	$220 \times (w - 0.004) \times (\text{La})$	$440 \times (w - 0.004) \times (\text{La})$
	$1 \text{ ns} \leq t_D < 0.5 \mu\text{s}$	$r \geq 0.01$	$220 \times (w - 0.004) \times (\text{La})/(r)^{0.5}$	$440 \times (w - 0.004) \times (\text{La})/(r)^{0.5}$
	$1 \text{ ns} \leq t_D < 0.5 \mu\text{s}$	$r < 0.01$	$220 \times (w - 0.004) \times (\text{La})/(0.01)^{0.5}$	$440 \times (w - 0.004) \times (\text{La})/(0.01)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$352 \times (w - 0.004) \times (\text{La})/(r)^{0.5}$	$1056 \times (w - 0.004) \times (\text{La})/(r)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$352 \times (w - 0.004) \times (\text{La})/(0.01)^{0.5}$	$1056 \times (w - 0.004) \times (\text{La})/(0.01)^{0.5}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$528 \times (w - 0.004) \times (\text{La})/(r)^{0.5}$	$1584 \times (w - 0.004) \times (\text{La})/(r)^{0.5}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$550 \times (w - 0.004) \times (\text{La})/(0.01)^{0.5}$	$2200 \times (w - 0.004) \times (\text{La})/(0.01)^{0.5}$
MP (vertical)	$t_D \geq 0.5 \mu\text{s}$	any	$220 \times (w - 0.004) \times (\text{La})$	$440 \times (w - 0.004) \times (\text{La})$
	$1 \text{ ns} \leq t_D < 0.5 \mu\text{s}$	$r \geq 0.01$	$220 \times (w - 0.004) \times (\text{La})/(r)^{0.5}$	$440 \times (w - 0.004) \times (\text{La})/(r)^{0.5}$

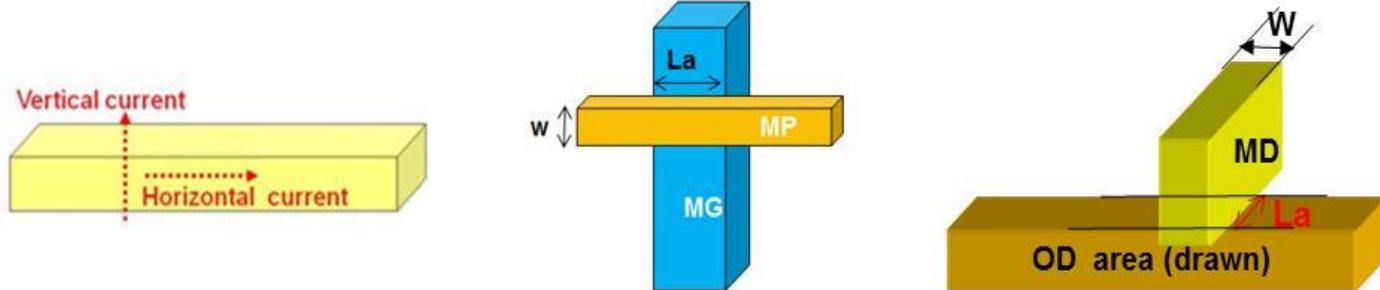
Metal process	Pulse duration (t_D)	Duty ratio (r)	Ipeak (mA) (w ≥ 0.13 μm) for dummy MD/MP	Ipeak (mA) (w [drawn] < 0.1 μm)
M0	1 ns ≤ t_D < 0.5 us	r < 0.01	$220 \times (w-0.004) \times (La)/(0.01)^{0.5}$	$440 \times (w-0.004) \times (La)/(0.01)^{0.5}$
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$352 \times (w-0.004) \times (La)/(r)^{0.5}$	$1056 \times (w-0.004) \times (La)/(r)^{0.5}$
	100 ps ≤ t_D < 1 ns	r < 0.01	$352 \times (w-0.004) \times (La)/(0.01)^{0.5}$	$1056 \times (w-0.004) \times (La)/(0.01)^{0.5}$
	t_D < 100 ps	r ≥ 0.01	$528 \times (w-0.004) \times (La)/(r)^{0.5}$	$1584 \times (w-0.004) \times (La)/(r)^{0.5}$
	t_D < 100 ps	r < 0.01	$550 \times (w-0.004) \times (La)/(0.01)^{0.5}$	$2200 \times (w-0.004) \times (La)/(0.01)^{0.5}$
Metal process	Pulse duration (t_D)	Duty ratio (r)	Ipeak (mA) (w [drawn] ≥ 0.13 μm)	Ipeak (mA) (w [drawn] < 0.1 μm)
M0	t_D ≥ 0.5 us	any	$9.99 \times (w-0.003)$	$19.98 \times (w-0.003)$
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$9.99 \times (w-0.003)/(r)^{0.5}$	$19.98 \times (w-0.003)/(r)^{0.5}$
	1 ns ≤ t_D < 0.5 us	r < 0.01	$9.99 \times (w-0.003)/(0.01)^{0.5}$	$19.98 \times (w-0.003)/(0.01)^{0.5}$
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$13.98 \times (w-0.003)/(r)^{0.5}$	$33.56 \times (w-0.003)/(r)^{0.5}$
	100 ps ≤ t_D < 1 ns	r < 0.01	$13.98 \times (w-0.003)/(0.01)^{0.5}$	$33.56 \times (w-0.003)/(0.01)^{0.5}$
	t_D < 100 ps	r ≥ 0.01	$16.78 \times (w-0.003)/(r)^{0.5}$	$39.95 \times (w-0.003)/(r)^{0.5}$
	t_D < 100 ps	r < 0.01	$33.25 \times (w-0.003)/(0.01)^{0.5}$	$133 \times (w-0.003)/(0.01)^{0.5}$
M1	t_D ≥ 0.5 us	any	$8.40 \times (w-0.003)$	$16.80 \times (w-0.003)$
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$8.40 \times (w-0.003)/(r)^{0.5}$	$16.80 \times (w-0.003)/(r)^{0.5}$
	1 ns ≤ t_D < 0.5 us	r < 0.01	$8.40 \times (w-0.003)/(0.01)^{0.5}$	$16.8 \times (w-0.003)/(0.01)^{0.5}$
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$11.76 \times (w-0.003)/(r)^{0.5}$	$28.22 \times (w-0.003)/(r)^{0.5}$
	100 ps ≤ t_D < 1 ns	r < 0.01	$11.76 \times (w-0.003)/(0.01)^{0.5}$	$28.22 \times (w-0.003)/(0.01)^{0.5}$
	t_D < 100 ps	r ≥ 0.01	$14.11 \times (w-0.003)/(r)^{0.5}$	$33.60 \times (w-0.003)/(r)^{0.5}$
	t_D < 100 ps	r < 0.01	$27.95 \times (w-0.003)/(0.01)^{0.5}$	$111.9 \times (w-0.003)/(0.01)^{0.5}$
Mx/Mxa/Mxs	t_D ≥ 0.5 us	any	$9.31 \times (w-0.003)$	$18.61 \times (w-0.003)$
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$9.31 \times (w-0.003)/(r)^{0.5}$	$18.61 \times (w-0.003)/(r)^{0.5}$
	1 ns ≤ t_D < 0.5 us	r < 0.01	$9.31 \times (w-0.003)/(0.01)^{0.5}$	$18.61 \times (w-0.003)/(0.01)^{0.5}$
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$13.03 \times (w-0.003)/(r)^{0.5}$	$31.27 \times (w-0.003)/(r)^{0.5}$
	100 ps ≤ t_D < 1 ns	r < 0.01	$13.03 \times (w-0.003)/(0.01)^{0.5}$	$31.27 \times (w-0.003)/(0.01)^{0.5}$
	t_D < 100 ps	r ≥ 0.01	$15.64 \times (w-0.003)/(r)^{0.5}$	$37.23 \times (w-0.003)/(r)^{0.5}$
	t_D < 100 ps	r < 0.01	$31.00 \times (w-0.003)/(0.01)^{0.5}$	$124 \times (w-0.003)/(0.01)^{0.5}$
Mya	t_D ≥ 0.5 us	any	$10.22 \times (w-0.003)$	$20.43 \times (w-0.003)$
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$10.22 \times (w-0.003)/(r)^{0.5}$	$20.43 \times (w-0.003)/(r)^{0.5}$
	1 ns ≤ t_D < 0.5 us	r < 0.01	$10.22 \times (w-0.003)/(0.01)^{0.5}$	$20.43 \times (w-0.003)/(0.05)^{0.5}$
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$14.30 \times (w-0.003)/(r)^{0.5}$	$34.33 \times (w-0.003)/(r)^{0.5}$
	100 ps ≤ t_D < 1 ns	r < 0.01	$14.30 \times (w-0.003)/(0.01)^{0.5}$	$34.33 \times (w-0.003)/(0.01)^{0.5}$
	t_D < 100 ps	r ≥ 0.01	$17.16 \times (w-0.003)/(r)^{0.5}$	$48.96 \times (w-0.003)/(r)^{0.5}$
	t_D < 100 ps	r < 0.01	$40.82 \times (w-0.003)/(0.01)^{0.5}$	$163.2 \times (w-0.003)/(0.01)^{0.5}$
My	t_D ≥ 0.5 us	any	$10.27 \times (w-0.004)$	$20.54 \times (w-0.004)$
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$10.27 \times (w-0.004)/(r)^{0.5}$	$20.54 \times (w-0.004)/(r)^{0.5}$
	1 ns ≤ t_D < 0.5 us	r < 0.01	$10.27 \times (w-0.004)/(0.01)^{0.5}$	$20.54 \times (w-0.004)/(0.01)^{0.5}$
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$14.38 \times (w-0.004)/(r)^{0.5}$	$43.13 \times (w-0.004)/(r)^{0.5}$
	100 ps ≤ t_D < 1 ns	r < 0.01	$14.38 \times (w-0.004)/(0.01)^{0.5}$	$43.13 \times (w-0.004)/(0.01)^{0.5}$
	t_D < 100 ps	r ≥ 0.01	$17.26 \times (w-0.004)/(r)^{0.5}$	$51.75 \times (w-0.004)/(r)^{0.5}$
	t_D < 100 ps	r < 0.01	$51.35 \times (w-0.004)/(0.01)^{0.5}$	$205.4 \times (w-0.004)/(0.01)^{0.5}$
Myy	t_D ≥ 0.5 us	any	$12.60 \times (w-0.008)$	$25.20 \times (w-0.008)$
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$12.60 \times (w-0.008)/(r)^{0.5}$	$25.20 \times (w-0.008)/(r)^{0.5}$
	1 ns ≤ t_D < 0.5 us	r < 0.01	$12.60 \times (w-0.008)/(0.01)^{0.5}$	$25.20 \times (w-0.008)/(0.01)^{0.5}$
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$17.64 \times (w-0.008)/(r)^{0.5}$	$35.28 \times (w-0.008)/(r)^{0.5}$

Metal process	Pulse duration (t_D)	Duty ratio (r)	Ipeak (mA) (w ≥ 0.13 μm) for dummy MD/MP	Ipeak (mA) (w [drawn] < 0.1 μm)
	100 ps ≤ t_D < 1 ns	r < 0.01	$17.64 \times (w-0.008)/(0.01)^{0.5}$	$35.28 \times (w-0.008)/(0.01)^{0.5}$
	t_D < 100 ps	r ≥ 0.01	$21.17 \times (w-0.008)/(r)^{0.5}$	$42.34 \times (w-0.008)/(r)^{0.5}$
	t_D < 100 ps	r < 0.01	$63.0 \times (w-0.008)/(0.01)^{0.5}$	$126 \times (w-0.008)/(0.01)^{0.5}$
Myx	t_D ≥ 0.5 us	any	$13.25 \times (w-0.020)$	N/A
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$13.25 \times (w-0.020)/(r)^{0.5}$	N/A
	1 ns ≤ t_D < 0.5 us	r < 0.01	$13.25 \times (w-0.020)/(0.01)^{0.5}$	N/A
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$18.55 \times (w-0.020)/(r)^{0.5}$	N/A
	100 ps ≤ t_D < 1 ns	r < 0.01	$18.55 \times (w-0.020)/(0.01)^{0.5}$	N/A
	t_D < 100 ps	r ≥ 0.01	$22.26 \times (w-0.020)/(r)^{0.5}$	N/A
	t_D < 100 ps	r < 0.01	$66.25 \times (w-0.020)/(0.01)^{0.5}$	N/A
Myz	t_D ≥ 0.5 us	any	$33.81 \times (w-0.020)$	N/A
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$33.81 \times (w-0.020)/(r)^{0.5}$	N/A
	1 ns ≤ t_D < 0.5 us	r < 0.01	$33.81 \times (w-0.020)/(0.01)^{0.5}$	N/A
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$47.33 \times (w-0.020)/(r)^{0.5}$	N/A
	100 ps ≤ t_D < 1 ns	r < 0.01	$47.33 \times (w-0.020)/(0.01)^{0.5}$	N/A
	t_D < 100 ps	r ≥ 0.01	$56.80 \times (w-0.020)/(r)^{0.5}$	N/A
	t_D < 100 ps	r < 0.01	$169.05 \times (w-0.020)/(0.01)^{0.5}$	N/A
Mz	t_D ≥ 0.5 us	any	$58.10 \times (w-0.020)$	N/A
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$58.10 \times (w-0.020)/(r)^{0.5}$	N/A
	1 ns ≤ t_D < 0.5 us	r < 0.01	$58.10 \times (w-0.020)/(0.01)^{0.5}$	N/A
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$81.34 \times (w-0.020)/(r)^{0.5}$	N/A
	100 ps ≤ t_D < 1 ns	r < 0.01	$81.34 \times (w-0.020)/(0.01)^{0.5}$	N/A
	t_D < 100 ps	r ≥ 0.01	$97.61 \times (w-0.020)/(r)^{0.5}$	N/A
	t_D < 100 ps	r < 0.01	$290.5 \times (w-0.020)/(0.01)^{0.5}$	N/A
Mr	t_D ≥ 0.5 us	any	$83.64 \times (w-0.020)$	N/A
	1 ns ≤ t_D < 0.5 us	r ≥ 0.01	$83.64 \times (w-0.020)/(r)^{0.5}$	N/A
	1 ns ≤ t_D < 0.5 us	r < 0.01	$83.64 \times (w-0.020)/(0.01)^{0.5}$	N/A
	100 ps ≤ t_D < 1 ns	r ≥ 0.01	$117.10 \times (w-0.020)/(r)^{0.5}$	N/A
	100 ps ≤ t_D < 1 ns	r < 0.01	$117.10 \times (w-0.020)/(0.01)^{0.5}$	N/A
	t_D < 100 ps	r ≥ 0.01	$140.52 \times (w-0.020)/(r)^{0.5}$	N/A
	t_D < 100 ps	r < 0.01	$418.2 \times (w-0.020)/(0.01)^{0.5}$	N/A

Table 10.4.49

Metal process	Pulse duration (t_D)	Duty ratio (r)	Ipeak (mA) ((0.13 > w >= 0.1 μm) for dummy MD/MP)
MD (horizontal)	$t_D \geq 0.5$ us	any	$12.67 \times (w-0.004)$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r \geq 0.01$	$12.67 \times (w-0.004)/(r)^{0.5}$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r < 0.01$	$12.67 \times (w-0.004)/(0.01)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r \geq 0.01$	$30.40 \times (w-0.004)/(r)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r < 0.01$	$30.40 \times (w-0.004)/(0.01)^{0.5}$
	$t_D < 100\text{ ps}$	$r \geq 0.01$	$50.69 \times (w-0.004)/(r)^{0.5}$
	$t_D < 100\text{ ps}$	$r < 0.01$	$63.36 \times (w-0.004)/(0.01)^{0.5}$
MP (horizontal)	$t_D \geq 0.5$ us	any	$6.27 \times (w-0.004)$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r \geq 0.01$	$6.27 \times (w-0.004)/(r)^{0.5}$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r < 0.01$	$6.27 \times (w-0.004)/(0.01)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r \geq 0.01$	$15.20 \times (w-0.004)/(r)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r < 0.01$	$15.20 \times (w-0.004)/(0.01)^{0.5}$
	$t_D < 100\text{ ps}$	$r \geq 0.01$	$25.34 \times (w-0.004)/(r)^{0.5}$
	$t_D < 100\text{ ps}$	$r < 0.01$	$39.68 \times (w-0.004)/(0.01)^{0.5}$
MD (vertical)	$t_D \geq 0.5$ us	any	$352 \times (w-0.004) \times (La)$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r \geq 0.01$	$352 \times (w-0.004) \times (La)/(r)^{0.5}$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r < 0.01$	$352 \times (w-0.004) \times (La)/(0.01)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r \geq 0.01$	$563.2 \times (w-0.004) \times (La)/(r)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r < 0.01$	$563.2 \times (w-0.004) \times (La)/(0.01)^{0.5}$
	$t_D < 100\text{ ps}$	$r \geq 0.01$	$844.8 \times (w-0.004) \times (La)/(r)^{0.5}$
	$t_D < 100\text{ ps}$	$r < 0.01$	$880 \times (w-0.004) \times (La)/(0.01)^{0.5}$
MP (vertical)	$t_D \geq 0.5$ us	any	$352 \times (w-0.004) \times (La)$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r \geq 0.01$	$352 \times (w-0.004) \times (La)/(r)^{0.5}$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r < 0.01$	$352 \times (w-0.004) \times (La)/(0.01)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r \geq 0.01$	$563.2 \times (w-0.004) \times (La)/(r)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r < 0.01$	$563.2 \times (w-0.004) \times (La)/(0.01)^{0.5}$
	$t_D < 100\text{ ps}$	$r \geq 0.01$	$844.8 \times (w-0.004) \times (La)/(r)^{0.5}$
	$t_D < 100\text{ ps}$	$r < 0.01$	$880 \times (w-0.004) \times (La)/(0.01)^{0.5}$
Metal process	Pulse duration (t_D)	Duty ratio (r)	Ipeak (mA) ((0.13 > w [drawn] >= 0.1 μm)
M0	$t_D \geq 0.5$ us	any	$15.98 \times (w-0.003)$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r \geq 0.01$	$15.98 \times (w-0.003)/(r)^{0.5}$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r < 0.01$	$15.98 \times (w-0.003)/(0.01)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r \geq 0.01$	$22.37 \times (w-0.003)/(r)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r < 0.01$	$22.37 \times (w-0.003)/(0.01)^{0.5}$
	$t_D < 100\text{ ps}$	$r \geq 0.01$	$26.77 \times (w-0.003)/(r)^{0.5}$
	$t_D < 100\text{ ps}$	$r < 0.01$	$53.2 \times (w-0.003)/(0.01)^{0.5}$
M1	$t_D \geq 0.5$ us	any	$13.44 \times (w-0.003)$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r \geq 0.01$	$13.44 \times (w-0.003)/(r)^{0.5}$
	$1\text{ ns} \leq t_D < 0.5\text{ us}$	$r < 0.01$	$13.44 \times (w-0.003)/(0.01)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r \geq 0.01$	$18.81 \times (w-0.003)/(r)^{0.5}$
	$100\text{ ps} \leq t_D < 1\text{ ns}$	$r < 0.01$	$18.81 \times (w-0.003)/(0.01)^{0.5}$
	$t_D < 100\text{ ps}$	$r \geq 0.01$	$22.51 \times (w-0.003)/(r)^{0.5}$
	$t_D < 100\text{ ps}$	$r < 0.01$	$44.76 \times (w-0.003)/(0.01)^{0.5}$

Metal process	Pulse duration (t_D)	Duty ratio (r)	Ipeak (mA) ($0.13 > w \geq 0.1 \mu\text{m}$) for dummy MD/MP
Mx/Mxa/Mxs	$t_D \geq 0.5 \text{ us}$	any	$14.89 \times (w-0.003)$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r \geq 0.01$	$14.89 \times (w-0.003)/(r)^{0.5}$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r < 0.01$	$14.89 \times (w-0.003)/(0.01)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$20.85 \times (w-0.003)/(r)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$20.85 \times (w-0.003)/(0.01)^{0.5}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$24.94 \times (w-0.003)/(r)^{0.5}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$49.76 \times (w-0.003)/(0.01)^{0.5}$
Mya	$t_D \geq 0.5 \text{ us}$	any	$16.35 \times (w-0.003)$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r \geq 0.01$	$16.35 \times (w-0.003)/(r)^{0.5}$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r < 0.01$	$16.35 \times (w-0.003)/(0.01)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$22.89 \times (w-0.003)/(r)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$22.89 \times (w-0.003)/(0.01)^{0.5}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$27.38 \times (w-0.003)/(r)^{0.5}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$65.32 \times (w-0.003)/(0.01)^{0.5}$
My	$t_D \geq 0.5 \text{ us}$	any	$16.43 \times (w-0.004)$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r \geq 0.01$	$16.43 \times (w-0.004)/(r)^{0.5}$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r < 0.01$	$16.43 \times (w-0.004)/(0.01)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$22.59 \times (w-0.004)/(r)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$22.59 \times (w-0.004)/(0.01)^{0.5}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$27.11 \times (w-0.004)/(r)^{0.5}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$82.15 \times (w-0.004)/(0.01)^{0.5}$
Myy	$t_D \geq 0.5 \text{ us}$	any	$20.16 \times (w-0.008)$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r \geq 0.01$	$20.16 \times (w-0.008)/(r)^{0.5}$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r < 0.01$	$20.16 \times (w-0.008)/(0.01)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$28.22 \times (w-0.008)/(r)^{0.5}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$28.22 \times (w-0.008)/(0.01)^{0.5}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$33.86 \times (w-0.008)/(r)^{0.5}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$100.8 \times (w-0.008)/(0.01)^{0.5}$
Myx	$tD \geq 0.5 \text{ us}$	any	$21.2 \times (w-0.020)$
	$1 \text{ ns} \leq tD < 0.5 \text{ us}$	$r \geq 0.01$	$21.2 \times (w-0.020)/(r)^{0.5}$
	$1 \text{ ns} \leq tD < 0.5 \text{ us}$	$r < 0.01$	$21.2 \times (w-0.020)/(0.01)^{0.5}$
	$100 \text{ ps} \leq tD < 1 \text{ ns}$	$r \geq 0.01$	$29.68 \times (w-0.020)/(r)^{0.5}$
	$100 \text{ ps} \leq tD < 1 \text{ ns}$	$r < 0.01$	$29.68 \times (w-0.020)/(0.01)^{0.5}$
	$tD < 100 \text{ ps}$	$r \geq 0.01$	$35.62 \times (w-0.020)/(r)^{0.5}$
	$tD < 100 \text{ ps}$	$r < 0.01$	$106 \times (w-0.020)/(0.01)^{0.5}$



The I_{peak} rule applies to the periodic AC or pulsed DC signals.

For a single event high current pulse or signals, which cannot be specified by duty ratio, please follow the ESD guidelines.

The I_{peak} rules provided in this section are applicable to signals with a pulse width (t_D) of less than $0.5\mu\text{sec}$. No temperature adjustment factor for the I_{rms} and I_{peak} is given.

The contact and vias I_{rms} and I_{peak} are not included because the heating in contacts and vias are negligible and is usually determined by metal or substrate. If the metal width is increased to some extent and only one via is used in that metal, then the heating in the via cannot be considered negligible. However, if the design follows the SM rules, via heating can be negligible. Please follow SM rules to make sure that the via heating is not a problem.

10.4.8 AP RDL AC Operation

The general terminology for AP RDL is the same as Cu interconnects.

The following table provides the I_{rms} for AP RDL at a junction temperature of 105°C. In the table, w (in μm) represents the drawn width of the RDL line and ΔT ($^{\circ}\text{C}$) is the temperature rise due to Joule heating.

Table 10.4.50 I_{rms} rule

Metal level	I_{rms} (mA)
AP RDL (28 kA)	Sqrt [$4.14 \times \Delta T \times w \times (w + 3.326)$]
AP RDL (14.5 kA)	Sqrt [$2.14 \times \Delta T \times w \times (w + 3.326)$]

Table 10.4.51 I_{peak} rule

Metal process	Pulse duration (t_D)	Duty ratio (r)	I_{peak} (mA)
AP RDL (28K)	$t_D \geq 0.5$ us	any	$112 \times w$
	$t_D < 0.5$ us	$r \geq 0.05$	$112 \times w / (r)^{0.5}$
	$t_D < 0.5$ us	$r < 0.05$	$112 \times w / (0.05)^{0.5}$
AP RDL (14.5K)	$t_D \geq 0.5$ us	any	$58 \times w$
	$t_D < 0.5$ us	$r \geq 0.05$	$58 \times w / (r)^{0.5}$
	$t_D < 0.5$ us	$r < 0.05$	$58 \times w / (0.05)^{0.5}$

Note:

If the duration time is smaller than $0.5\mu\text{s}$ (micro sec, 10^{-6}sec), the limit for the peak current, I_{peak} , can be calculated by using the following formula. If r is smaller than 0.05, please let r=0.05

$$I_{peak} = \frac{I_{peak_DC}}{\sqrt{r}}$$

$$r = \frac{t_D}{\tau}$$

If the duration time is longer than $0.5\mu\text{s}$ (micro sec, 10^{-6}sec).

$$I_{peak} = I_{peak_DC}$$

10.4.9 High R Resistor Current Density (EM) Specifications

10.4.9.1 High R resistor current density

For high R resistor, the maximum DC current density is 0.44 mA/ μm at the junction temperature 105°C and lifetime 10 years. This density is calculated using 0.1% point of measurement data at a 5% resistance increase after 10 years of continuous operation. W_p (in μm) represents the drawn width of high R resistor line.

Designers can use Table 10.4.52 to calculate I_{\max} if the junction temperature differs from 105°C. For a junction temperature below 105°C, use the rule at 105°C.

Table 10.4.52

Junction temperature	105°C	110°C	115°C	120°C	125°C	130°C	135°C	140°C	145°C	150°C
Rating factor of J_{\max}	1	0.962	0.933	0.904	0.875	0.852	0.830	0.807	0.784	0.760

For example, I_{\max} (at 125°C) = $0.875 \times I_{\max}$ (at 105°C).

The rating factor is 1 for the case of temperature below 105°C for Joule heating effect consideration.

10.4.9.2 High R Resistor Root-Mean-Square Current (I_{rms})

The following table provides the root-mean-square current (I_{rms}) for high R resistor. In this table, W_p (in μm) represents the drawn width of resistor line and ΔT (°C) is the temperature rise due to Joule heating effect.

Table 10.4.53

Resistor	Root-Mean-Square current (mA)
High R resistor	Sqrt [0.01512 x ΔT x W_p x (W_p + 0.48)]

W_p : resistor line drawn width

10.4.9.3 High R Resistor I_{peak}

The following table provides the I_{peak} for resistors. In the table, W_p (in μm) represents the drawn width of resistor line.

Table 10.4.54

Resistor	Pulse duration (t_D)	Duty ratio (r)	I_{peak} (mA)
High-R	$t_D \geq 0.5 \text{ us}$	any	$2 \times W_p$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r \geq 0.01$	$2 \times W_p / (r)^{0.25}$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r < 0.01$	$2 \times W_p / (0.01)^{0.25}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$2.8 \times W_p / (r)^{0.25}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$2.8 \times W_p / (0.01)^{0.25}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$2.8 \times W_p / (r)^{0.25}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$4 \times W_p / (0.01)^{0.25}$

10.4.10 Metal-Gate Interconnect Current Density (EM) Specifications

10.4.10.1 Metal-Gate Interconnect current density

For metal-gate interconnect, the maximum DC current density is $5.73 \text{ mA}/\mu\text{m}$ at the junction temperature 105°C and lifetime 10 years. This density is calculated using 0.1% point of measurement data at a 5% resistance increase after 10 years of continuous operation. $W_p(\text{in } \mu\text{m})$ represents the drawn width of metal-gate interconnect. Designers can use Table 10.4.55 to calculate I_{\max} if the junction temperature differs from 105°C . For a junction temperature below 100°C , use the rule at 100°C .

Table 10.4.55

Temperature	100°C	105°C	110°C	115°C	120°C	125°C	130°C	135°C	140°C	145°C	150°C
Rating factor of I_{\max}	1.448	1.000	0.697	0.673	0.649	0.625	0.605	0.586	0.566	0.548	0.530

For example, I_{\max} (at 125°C) = $0.625 \times I_{\max}$ (at 105°C).

The rating factor is 1.448 for the case of temperature below 100°C for Joule heating effect consideration.

10.4.10.2 Metal-Gate Interconnect Root-Mean-Square Current (I_{rms})

The following table provides the root-mean-square current (I_{rms}) for metal-gate interconnect. In this table, W_p (in μm) represents the drawn width of Metal-Gate Interconnect and ΔT ($^\circ\text{C}$) is the temperature rise due to Joule heating effect.

Table 10.4.56

Layer	Root-Mean-Square current (mA)
Metal-Gate Interconnect	Sqrt [1.149 x ΔT x W_p x ($W_p + 0.09$)]

W_p : metal-gate interconnect drawn width

10.4.10.3 Metal-Gate Interconnect I_{peak}

The following table provides the I_{peak} for Metal-gate Interconnect. In the table, W_p (in μm) represents the drawn width of metal-gate interconnect line.

Table 10.4.57

Metal process	Pulse duration (t_D)	Duty ratio (r)	I_{peak} (mA) ($0.036 < W_p \leq 0.24$)	I_{peak} (mA) ($0.008 < W_p \leq 0.036$)	I_{peak} (mA) ($W_p=0.008$)
Metal-Gate Interconnect	$t_D \geq 0.5 \text{ us}$	any	$20 \times W_p$	$39 \times W_p$	$60 \times W_p$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r \geq 0.01$	$20 \times W_p / (r)^{0.25}$	$39 \times W_p / (r)^{0.25}$	$60 \times W_p / (r)^{0.25}$
	$1 \text{ ns} \leq t_D < 0.5 \text{ us}$	$r < 0.01$	$20 \times W_p / (0.01)^{0.25}$	$39 \times W_p / (0.01)^{0.25}$	$60 \times W_p / (0.01)^{0.25}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r \geq 0.01$	$28 \times W_p / (r)^{0.25}$	$54.6 \times W_p / (r)^{0.25}$	$84 \times W_p / (r)^{0.25}$
	$100 \text{ ps} \leq t_D < 1 \text{ ns}$	$r < 0.01$	$28 \times W_p / (0.01)^{0.25}$	$54.6 \times W_p / (0.01)^{0.25}$	$84 \times W_p / (0.01)^{0.25}$
	$t_D < 100 \text{ ps}$	$r \geq 0.01$	$28 \times W_p / (r)^{0.25}$	$54.6 \times W_p / (r)^{0.25}$	$84 \times W_p / (r)^{0.25}$
	$t_D < 100 \text{ ps}$	$r < 0.01$	$40 \times W_p / (0.01)^{0.25}$	$78 \times W_p / (0.01)^{0.25}$	$120 \times W_p / (0.01)^{0.25}$

11 Design Information

This chapter is divided into the following topic:

11.1 N7+ Universal Fin Grid

11.1 N7+ Universal FIN Grid

11.1.1 Introduction

For N7+ design, universal fin grid inside whole chip is required for each kind of FinFET_Boundary. Design rules and guidelines to achieve universal fin grid are described in this chapter. Chapter organization is shown below:

- 11.1.2 Design rule requirement of universal fin grid
- 11.1.3 Guidelines of FinFET_Boundary in standard cells
- 11.1.4 Guidelines of design blocks contain multiple types of FinFET_Boundary
- 11.1.5 Guidelines of hierarchical design blocks
- 11.1.6 Guidelines of chip integration

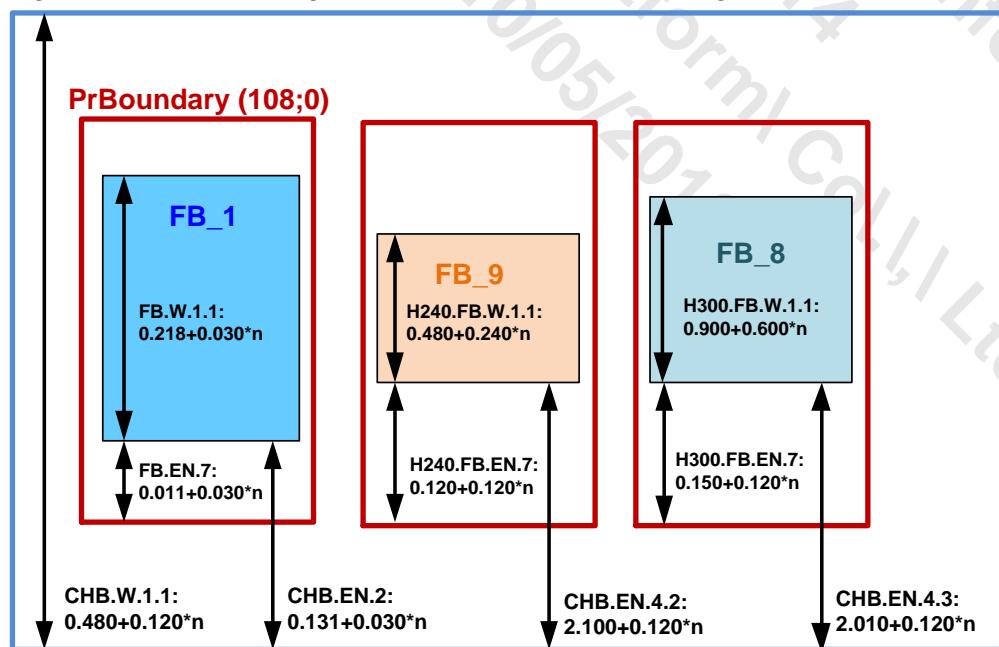
11.1.2 Design Rule Requirement of Universal Fin Grid

Following design rules are required to keep universal fin grid for each type of FinFET_Boundary

FinFET_Boundary	Rule No.	Description	Rule
General	CHB.W.1.1	Width in vertical direction	$0.4800+0.1200*n$
FB_1	CHB.EN.2	Enclosure of FB_1 in vertical direction	$0.1310+0.0300*n$
FB_9	CHB.EN.4.2	Enclosure of FB_9 in vertical direction in chip level	$0.9000+0.1200*n$
FB_8	CHB.EN.4.3	Enclosure of FB_8 in vertical direction in chip level	$0.9300+0.1200*n$
FB_1	FB.W.1.1	Width of FB_1 in vertical direction	$0.2180+0.0300*n$
FB_1	FB.EN.7	prBoundary enclosure of FB_1 in vertical direction in cell level	$0.0110+0.0300*n$
FB_9	H240.FB.W.1.1	Width of FB_9 in vertical direction	$0.4800+0.2400*n$
FB_9	H240.FB.EN.7	prBoundary enclosure of FB_9 in vertical direction in cell level	$0.1200+0.1200*n$
FB_8	H300.FB.W.1.1	Width of FB_8 in vertical direction	$0.9000+0.6000*n$
FB_8	H300.FB.EN.7	prBoundary enclosure of FB_8 in vertical direction in cell level	$0.1500+0.1200*n$

The relation between Chip_Boundary, prBoundary and each type of FinFET_Boundary is shown as following illustrate (Fig. 11.1.1)

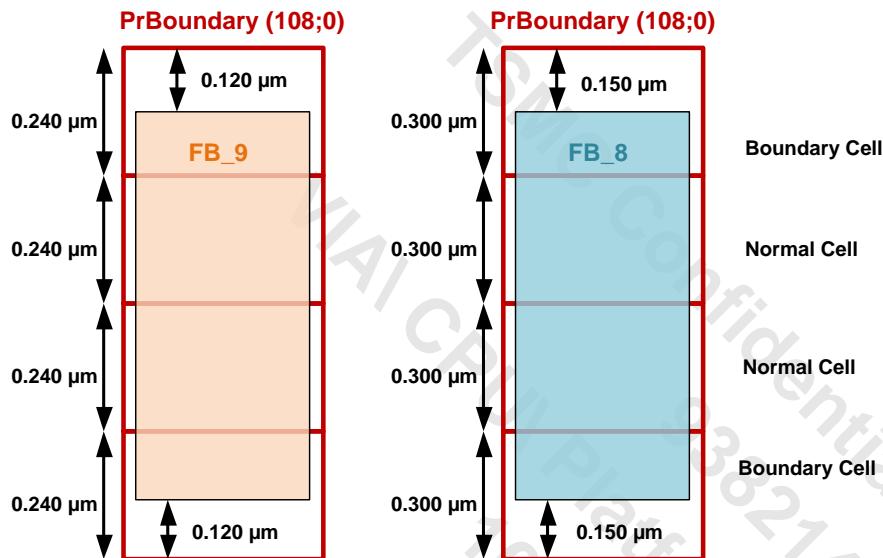
Fig. 11.1.1 Critical design rules related to universal fin grid



11.1.3 Guidelines of FinFET_Boundary in Standard Cells

Due to constraint by standard cell layout rules, prBoundary must enclosure FB_9, FB_8 half cell height in vertical direction. When using standard cells, boundary cells must be placed on top and bottom edges. And FB_9, or FB_8 should only cover half of boundary cells. Example layout is shown in illustrate fig. 11.1.2

Fig. 11.1.2 FB_9 (H240) and FB_8 (H300) scheme with proper standard cell usage

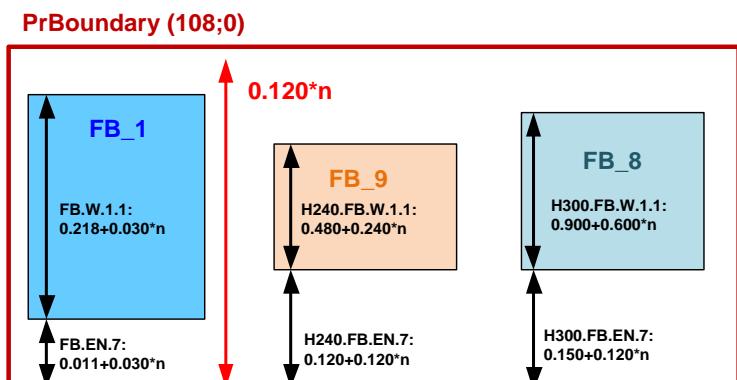


11.1.4 Guidelines of Design Blocks Contain Multiple Types of FinFET_Boundary

For design blocks contain multiple types of FinFET_boundary, width of block in vertical direction should be multiple of 0.120 μm. And block should satisfy requirement of FB.EN.7, H240.FB.EN.7, H300.FB.EN.7, FB.W.1.1, H240.FB.W.1.1, and H300.FB.W.1.1 in IP level.

Following graph (Fig. 11.1.3) shows scheme and dimension to help achieving universal fin grid inside block.

Fig. 11.1.3 Rules related to universal fin grid in block contains multiple type of FinFET_Boundary

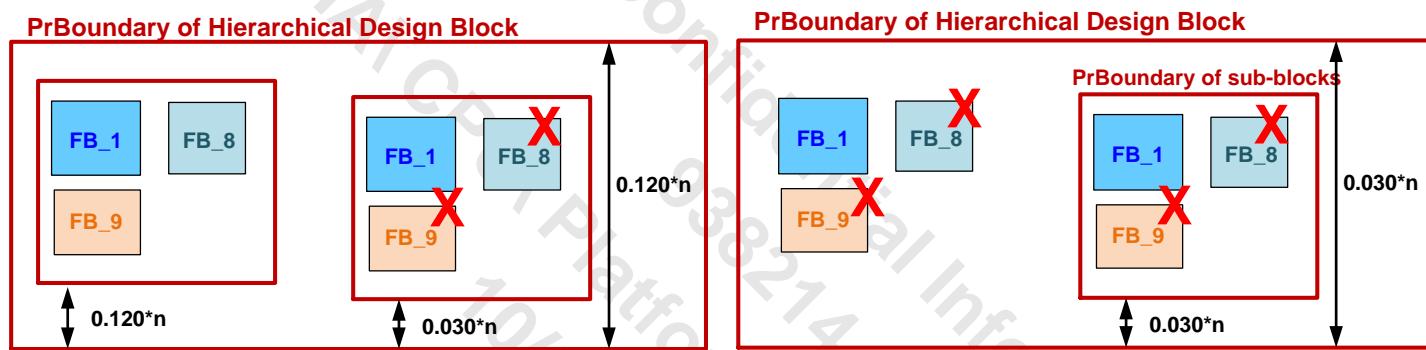


11.1.5 Guidelines of Hierarchical Design Blocks

Design blocks usually built hierarchical. Smaller sub-blocks are placed in design block, and design block may be included in larger blocks. To meet universal fin grid requirement, following guidelines should be followed

1. If FB_9 or FB_8 is used in any sub-blocks, or layout of design block, width of block in vertical direction should be multiple of 0.120 μm
2. If only FB_1 is used in layout of design block and all sub-blocks, width of block in vertical direction should be multiple of 0.030 μm .
3. For sub-blocks contains FB_9 or FB_8, prBoundary of design block should enclosure sub-block multiple of 0.120 μm in vertical direction
4. For sub-blocks contains only FB_1, prBoundary of hierarchical design block should enclosure sub-block multiple of 0.030 μm in vertical direction

Fig. 11.1.4 Suggested enclosure of hierarchical design blocks



11.1.6 Guidelines of Chip Integration

When chip integration, blocks will be placed in chip design. Following guidelines should be followed for universal fin grid

- For blocks contains FB_9 or FB_8, Chip_Boundary (108;250) should enclosure block $0.060+0.120^*n$ μm in vertical direction (Fig. 11.1.5). Please notice the $0.060 \mu\text{m}$ offset only exists in chip integration.
- For blocks contains only FB_1, Chip_Boundary (108;250) should enclosure block $0.030^*n \mu\text{m}$ in vertical direction. (Fig. 11.1.5) as well as hierarchical design block
- Min. Chip_Boundary enclosure fin boundaries (Fig. 11.1.6) need to be satisfied. If FinFET_Boundary location inside block is uncertain, keep Chip_Boundary enclosure prBoundary of block in vertical direction as following table:

Block contains which FinFET_Boundary	Min. Chip_Boundary enclosure FinFET_Boundary in vertical direction(μm)	Chip_Boundary enclosure block prBoundary in vertical direction (μm)	
		Known FB location	Uncertain FB location
FB_1	0.1310	0.0300^*n	$0.1200+0.0300^*n$
FB_8	2.0100	$0.0600+0.1200^*n$	$1.8600+0.1200^*n$
FB_9	2.1000	$0.0600+0.1200^*n$	$1.9800+0.1200^*n$

Fig. 11.1.5 Suggested enclosure in chip integration

Chip_Boundary (108;250)

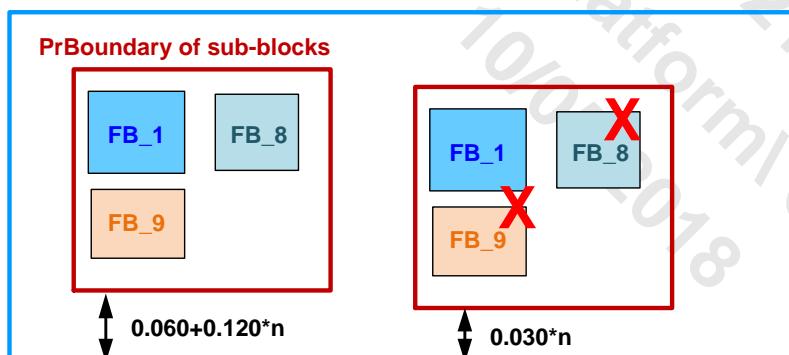
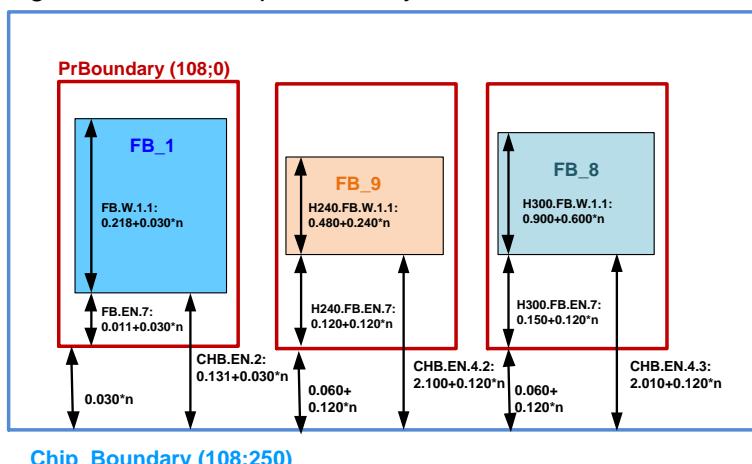


Fig. 11.1.6 Min. Chip_Boundary enclosure FB rules

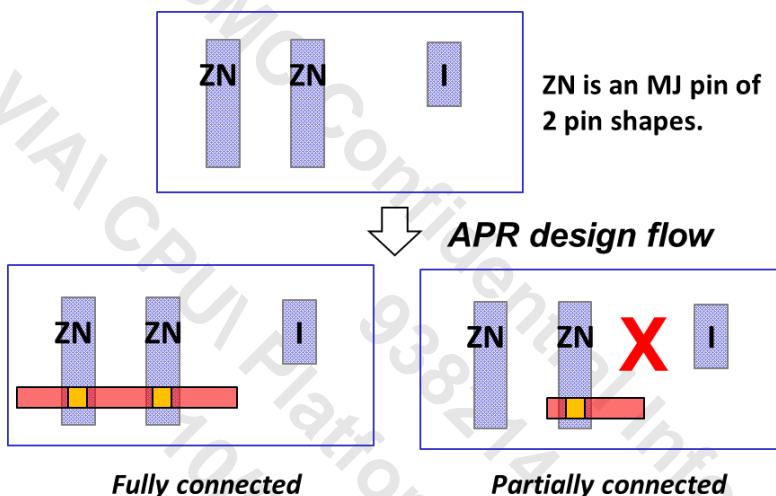


11.2 Must Join Pin

11.2.1 Introduction

To increase the flexibility for automatic placement and routing (APR) tools, must-join pins are adopted in standard cells. A pin is defined as *must-join* if it has more than one pin shape that requires to be connected in the APR flow, not pre-connected in cells.

However, if a must-join pin is not fully connected in the APR flow, timing uncertainty or even cell malfunction may occur. Must-join pin rules herein are used to sign off that all must-join pins are well connected.



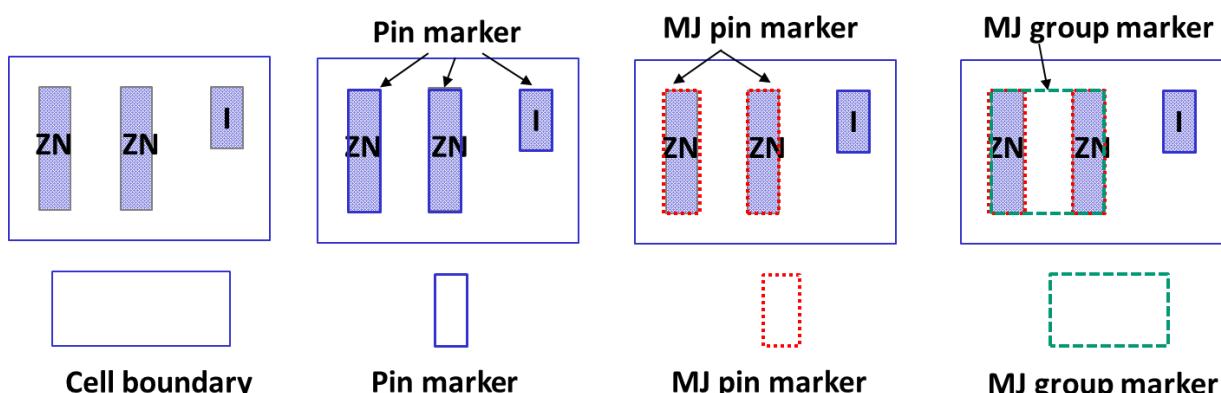
11.2.2 Must-Join Pin Rules

Must-join rules and auxiliary markers are described in this section.

11.2.2.1 Auxiliary Marker Layers

To identify pins and must-join pins in standard cells, additional three types of markers are created:

- Pin marker: Mark all pin shapes.
- MJ pin marker: Mark all pin shapes that belong to MJ pins.
- MJ group marker: Group MJ pin markers that belong to a same MJ pin.



The table below summarizes the CAD layers for required markers. Only M1 and M2 MJ pin rules are supported.

Layer	Layer Name	Layer Number	Data Type
M1	M1_Pin_Mrk	31	300
	M1_MJ_Pin	31	301
	M1_MJ_Grp	31	302
M2	M2_Pin_Mrk	32	410
	M2_MJ_Pin	32	411
	M2_MJ_Grp	32	412

TSMC Confidential Information
938214
VIAI CPU Platform\ Col., I Ltd.
10/05/2018

11.2.2.2 MJ Pin Rules

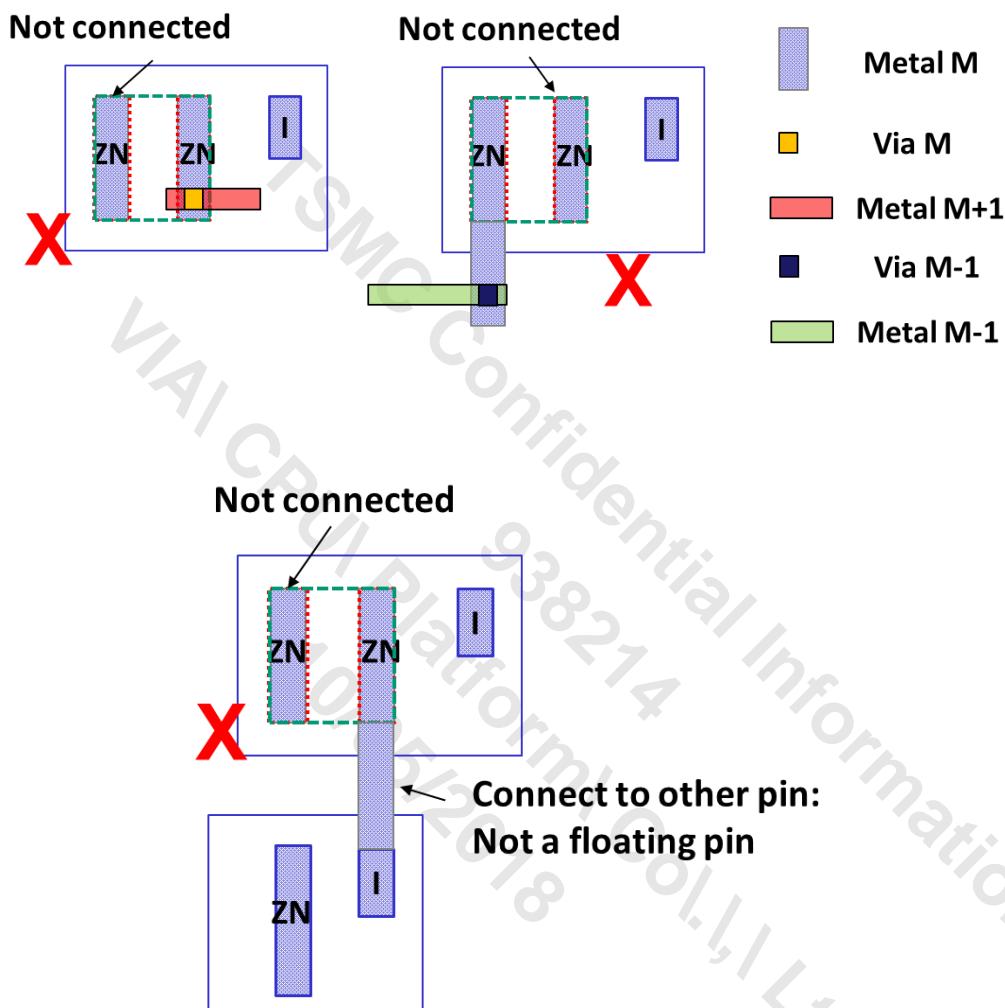
Rule No.	Description	Label	Op.	Rule
MJ_M1.R.1	<p>Each M1_MJ_Pin_Shape must follow either one of the following conditions:</p> <ol style="list-style-type: none"> 1. Interact at least one VIA1 or, 2. Interact at least one VIA0 or, 3. Connection to other M1_Pin_Mrk. <p>(Except following conditions:</p> <ol style="list-style-type: none"> 1. M1_MJ_Pins_Floating) <p>DRC flags:</p> <ol style="list-style-type: none"> 1. {M1_MJ_Pin_Shape_Wo_VIA INTERACT M1_MJ_Grp_Chk_Floating} 2. {M1_MJ_Pin_Shape_Wo_VIA INTERACT one M1_Pin_Mrk} INTERACT {M1_MJ_Grp INTERACT {M1_MJ_Pin_Shape_Wo_VIA INTERACT more than one M1_Pin_Mrk}} <p>Definitions of M1_MJ_Pins_Floating: Each M1_MJ_Pin_Shape not interact VIA1, VIA0, or another M1_Pin_Mrk</p> <p>Definition of M1_MJ_Pin_Shape: M1 (31;420) INTERACT M1_MJ_Pin</p> <p>Definition of M1_MJ_Pin_Shape_Wo_VIA: M1_MJ_Pin_Shape NOT INTERACT {VIA1 OR (VIA0 NOT INSIDE M1_MJ_Pin)}</p> <p>Definition of M1_MJ_Grp_Chk_Floating: M1_MJ_Grp INTERACT {M1_MJ_Pin_Shape INTERACT {VIA1 OR (VIA0 NOT INSIDE M1_MJ_Pin)}}</p>			
MJ_M1.R.2	<p>At least one M2 connecting all M1_MJ_Pin_Shape within M1_MJ_Grp.</p> <p>(Except following conditions:</p> <ol style="list-style-type: none"> 1. M1_MJ_Pins_Floating) <p>DRC flags M1_MJ_Grp_Chk_Floating not interact M2_Checked.</p> <p>Definition of M2_Checked: Counts of {{M2 (32;400) AND M1_MJ_Grp_Chk_Floating} AND {M1 (31;420) AND M1_MJ_Pin}} enclose VIA1} are equal to {M1_MJ_Grp_Chk_Floating AND M1_MJ_Pin}</p> <p>Definition of M1_MJ_Pins_Floating, M1_MJ_Grp_Chk_Floating follows MJ_M1.R.1.</p>			
MJ_M1.R.3	<p>M1_MJ_Pin_Shape interact more than one M1_Pin_Mrk is not allowed</p> <p>Definition of M1_MJ_Pin_Shape follows MJ_M1.R.1.</p>			

Rule No.	Description	Label	Op.	Rule
MJ_M2.R.1	<p>Each M2_MJ_Pin_Shape must follow either one of the following conditions:</p> <ol style="list-style-type: none"> 1. Interact at least one VIA2 or, 2. Interact at least one VIA1 or, 3. Connection to other M2_Pin_Mrk. <p>(Except following conditions:</p> <ol style="list-style-type: none"> 1. M2_MJ_Pins_Floating) <p>DRC flags:</p> <ol style="list-style-type: none"> 1. {M2_MJ_Pin_Shape_Wo_VIA INTERACT M2_MJ_Grp_Chk_Floating} 2. {M2_MJ_Pin_Shape_Wo_VIA INTERACT one M2_Pin_Mrk} INTERACT {M2_MJ_Grp INTERACT {M2_MJ_Pin_Shape_Wo_VIA INTERACT more than one M2_Pin_Mrk}} <p>Definitions of M2_MJ_Pins_Floating: Each M2_MJ_Pin_Shape not interact VIA2, VIA1, or another M2_Pin_Mrk</p> <p>Definition of M2_MJ_Pin_Shape: M2 (32;400) INTERACT M2_MJ_Pin</p> <p>Definition of M2_MJ_Pin_Shape_Wo_VIA: M2_MJ_Pin_Shape NOT INTERACT {VIA2 OR (VIA1 NOT INSIDE M2_MJ_Pin)}</p> <p>Definition of M2_MJ_Grp_Chk_Floating: M2_MJ_Grp INTERACT {M2_MJ_Pin_Shape INTERACT {VIA2 OR (VIA1 NOT INSIDE M2_MJ_Pin)}}</p>			
MJ_M2.R.2	<p>At least one M3 connecting all M2_MJ_Pin_Shape within M2_MJ_Grp.</p> <p>(Except following conditions:</p> <ol style="list-style-type: none"> 1. M2_MJ_Pins_Floating) <p>DRC flags M2_MJ_Grp_Chk_Floating not interact M3_Checked.</p> <p>Definition of M3_Checked: Counts of {{{M3 AND M2_MJ_Grp_Chk_Floating} AND {M2 (32;400) AND M2_MJ_Pin}}} enclose VIA2 are equal to {M2_MJ_Grp_Chk_Floating AND M2_MJ_Pin}</p> <p>Definition of M2_MJ_Pins_Floating, M2_MJ_Grp_Chk_Floating follows MJ_M2.R.1.</p>			
MJ_M2.R.3	<p>M2_MJ_Pin_Shape interact more than one M2_Pin_Mrk is not allowed</p> <p>Definition of M2_MJ_Pin_Shape follows MJ_M2.R.1.</p>			

Three MJ pin rules are defined to make sure MJ pins are fully and well connected.

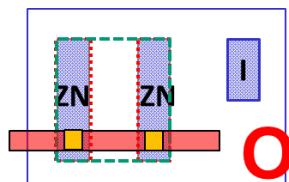
MJ_M*.R.1 : MJ pins must be fully connected except floating pins.

Each pin shape of an MJ pin, except floating pins, must be connected.

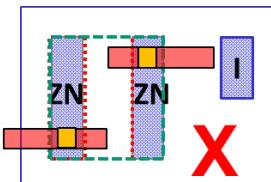


MJ_M*.R.2 : MJ pins must be well connected through at least one upper metal wire.

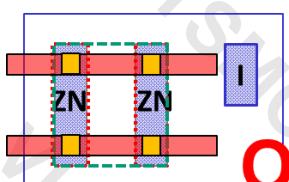
The VIAs connecting pin shapes and the upper metal wire must be within the MJ group marker.



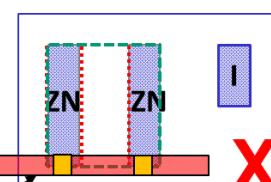
1 upper wire



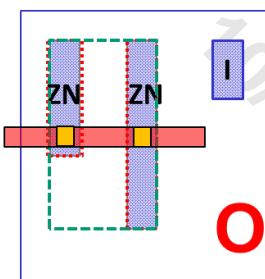
Not a whole wire



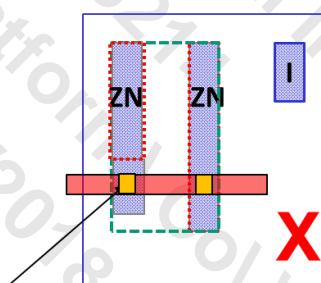
2 upper wires



The VIAs are not within MJ group marker

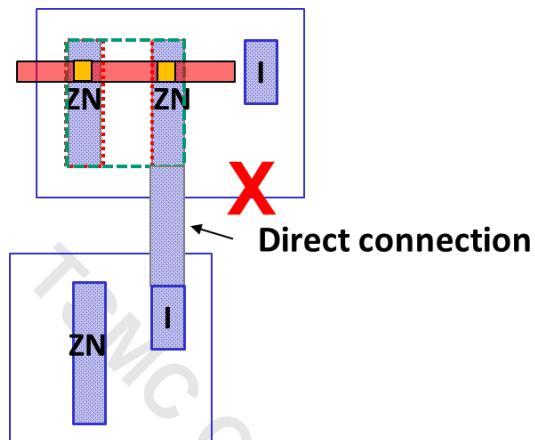
Non-aligned MJ pin shapes

Via is not inside MJ pin marker



MJ_M*.R.3 : Direct connections to other pins through the MJ pin layers are forbidden.

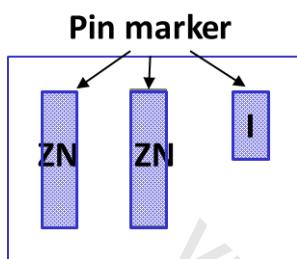
To avoid EM risk and cell timing gap with liberty, such connections are forbidden.



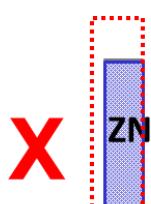
11.2.3 Guidelines of Marker Creation

MJ pin rule detection depends on correctly-created markers. Hard guidelines of marker creation are listed as follows:

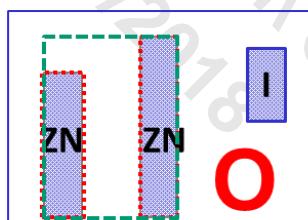
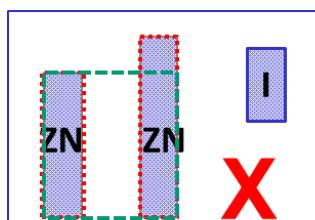
- Pin markers must be added on all pins, including MJ and non-MJ pins, at each MJ pin layer. MJ_M*.R.3 detection relies on correct pin markers.



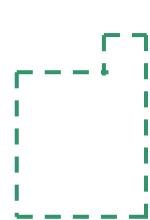
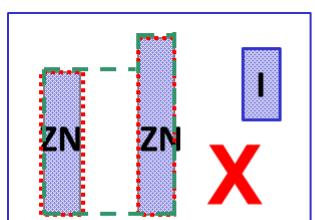
- MJ pin markers must be inside the corresponding pin markers.



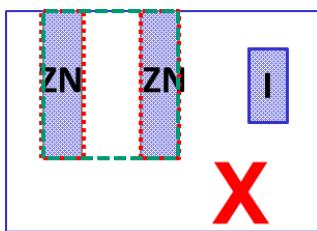
- MJ pin markers must be inside the MJ group marker.



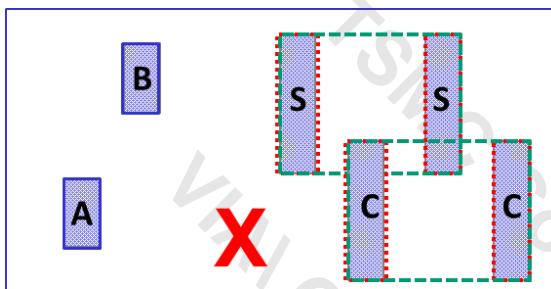
- MJ group markers must be rectangular.



- MJ group markers must be strictly inside the standard cell boundary.



- An MJ group marker can not interact or touch another MJ group marker.
Overlaps between MJ group markers are forbidden in standard cells.



- Standard cell definition files for APR tools such as cell LEF files should have must-join attributes for MJ pins.
APR tools will connect MJ pins according to must-join attributes on standard cell pins. The must-join definitions must be consistent between standard cell GDS and APR definition files.

12 Appendix A Revision History

12.1 A.1 From Version 0.5 to Version 0.9

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
1	G.5	3.6.1	Design Grid Rules	Modify the rule description
2	CHB.W.2	4.5.1	Chip Boundary Layout Rules	Add the new rule
3	CHB.W.2.1	4.5.1	Chip Boundary Layout Rules	Add the new rule
4	CHB.EN.4	4.5.1	Chip Boundary Layout Rules	Modify the rule description
5	CHB.EN.4.0	4.5.1	Chip Boundary Layout Rules	Add the new rule
6	CHB.EN.4.2	4.5.1	Chip Boundary Layout Rules	Modify the rule description
7	CHB.EN.4.3	4.5.1	Chip Boundary Layout Rules	Modify the rule description
8	FB.R.1	4.5.2	FinFET Boundary Layout Rules	Modify the rule description
9	OD.A.9	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Modify the rule description
10	COD_H.W.6.1	4.5.4	Cut-OD (COD) Layout Rules	Modify the rule description
11	COD_H.S.6	4.5.4	Cut-OD (COD) Layout Rules	Modify the rule description
12	COD_H.EN.1.1	4.5.4	Cut-OD (COD) Layout Rules	Add the new rule
13	COD_H.L.4	4.5.4	Cut-OD (COD) Layout Rules	Modify the rule description
14	COD_V.A.2	4.5.4	Cut-OD (COD) Layout Rules	Modify the rule description
15	DNW.R.7.1	4.5.5	Deep N-Well (DNW) Layout Rules [Optional]	Modify the rule description
16	DNW.R.7.2	4.5.5	Deep N-Well (DNW) Layout Rules [Optional]	Add the new rule
17	NWRSTI.R.5	4.5.7	N-Well Under STI (NWRSTI) Layout Rules	Modify the rule description
18	CELL.CMD.S.3	4.5.13	Standard Cell Layout Rules	Modify the rule description
19	CELL.CMD.S.3.1	4.5.13.1	Standard Cell Layout Rules	Modify the rule description
20	CELL.MP.R.12	4.5.13.1	Standard Cell Layout Rules	Add the new rule
21	CELL.M0.A.2.1	4.5.13.1	Standard Cell Layout Rules	Modify the rule description
22	CELL.M0.A.2.2	4.5.13.1	Standard Cell Layout Rules	Add the new rule
23	CELL.M1.A.2	4.5.13.1	Standard Cell Layout Rules	Delete the rule
24	H240.COD_V.A.2	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
25	H240.PO.S.25.5	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
26	H240.CPO.W.1	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
27	H240.VT.A.3	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
28	H240.M0.S.2.3	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
29	H240.M0.CS.1.1	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
30	H240.M0.CS.1.2.1	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
31	H240.CM0A.W.3	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
32	H240.CM0B.W.3	4.5.13.2	Standard Cell Layout Rules	Modify the rule description
33	H300.PO.S.25.5	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
34	H300.PO.S.25.5.1	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
35	H300.CPO.W.1	4.5.13.3	Standard Cell Layout Rules	Modify the rule description

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
36	H300.TPO.W.1	4.5.13.3	Standard Cell Layout Rules	Delete the rule
37	H300.TPO.S.1	4.5.13.3	Standard Cell Layout Rules	Delete the rule
38	H300.TPO.W.1.1.1	4.5.13.3	Standard Cell Layout Rules	Delete the rule
39	H300.TPO.S.1.1.1	4.5.13.3	Standard Cell Layout Rules	Delete the rule
40	H300.TPO.A.1	4.5.13.3	Standard Cell Layout Rules	Delete the rule
41	H300.TPO.A.2	4.5.13.3	Standard Cell Layout Rules	Delete the rule
42	H300.VT.W.2	4.5.13.3	Standard Cell Layout Rules	Delete the rule
43	H300.VT.W.2.2	4.5.13.3	Standard Cell Layout Rules	Delete the rule
44	H300.VT.W.2.3	4.5.13.3	Standard Cell Layout Rules	Delete the rule
45	H300.VT.W.2.4	4.5.13.3	Standard Cell Layout Rules	Delete the rule
46	H300.VT.S.2	4.5.13.3	Standard Cell Layout Rules	Delete the rule
47	H300.VT.S.2.2	4.5.13.3	Standard Cell Layout Rules	Delete the rule
48	H300.VT.S.2.4	4.5.13.3	Standard Cell Layout Rules	Delete the rule
49	H300.VT.S.2.5	4.5.13.3	Standard Cell Layout Rules	Delete the rule
50	H300.VT.S.2.6	4.5.13.3	Standard Cell Layout Rules	Delete the rule
51	H300.VT.S.2.7	4.5.13.3	Standard Cell Layout Rules	Delete the rule
52	H300.VT.A.1	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
53	H300.VT.A.2	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
54	H300.VT.A.2.2	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
55	H300.VT.A.2.4	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
56	H300.VT.A.3	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
57	H300.M0.S.2.3.1	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
58	H300.M0.CS.1.1	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
59	H300.M0.CS.1.3	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
60	H300.CM0B.W.3	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
61	H300.CM0B.W.3.1	4.5.13.3	Standard Cell Layout Rules	Modify the rule description
62	BV_FB.R.5	4.5.14	BV_FB Layout Rules	Modify the rule description
63	PODE.R.3	4.5.16	Poly on OD edge (PODE) Layout Rules	Modify the rule description
64	PODE.R.4	4.5.16	Poly on OD edge (PODE) Layout Rules	Delete the rule
65	PODE.R.5	4.5.16	Poly on OD edge (PODE) Layout Rules	Delete the rule
66	PODE.R.6	4.5.16	Poly on OD edge (PODE) Layout Rules	Delete the rule
67	PODE.R.7	4.5.16	Poly on OD edge (PODE) Layout Rules	Delete the rule
68	PODE.R.8	4.5.16	Poly on OD edge (PODE) Layout Rules	Delete the rule
69	PODE.R.8.1	4.5.16	Poly on OD edge (PODE) Layout Rules	Delete the rule
70	CPODE.W.3	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Add the new rule
71	CPODE.S.1.1	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Modify the rule description
72	CPODE.S.3	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Modify the rule description
73	CPODE.EX.1	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Modify the rule description
74	CPODE.EX.1.1	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Modify the rule description

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
75	CPODE.L.2	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Delete the rule
76	CPODE.L.2®	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Add the new rule
77	CPODE.DN.4	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Add the new rule
78	CPODE.R.2	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Add the new rule
79	CPODE.R.3	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Modify the rule description
80	CPODE.R.5	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Modify the rule description
81	CPODE.R.8.1	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Modify the rule description
82	CPODE.R.10	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Modify the rule description
83	CPODE.R.13.1	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Add the new rule
84	CPODE.R.12	4.5.17	Connected PODE (CPODE) Layout Rules (12N)	Delete the rule
85	PO.S.3.2	4.5.19	Poly (PO) Layout Rules	Modify the rule description
86	PO.S.25.4	4.5.19	Poly (PO) Layout Rules	Modify the rule description
87	PO.EN.1.3	4.5.19	Poly (PO) Layout Rules	Modify the rule description
88	PO.L.4	4.5.19	Poly (PO) Layout Rules	Modify the rule description
89	PO.A.5	4.5.19	Poly (PO) Layout Rules	Modify the rule description
90	PO.A.6	4.5.19	Poly (PO) Layout Rules	Delete the rule
91	PO.A.6.1	4.5.19	Poly (PO) Layout Rules	Delete the rule
92	PO.R.25	4.5.19	Poly (PO) Layout Rules	Modify the rule description
93	PO.R.33	4.5.19	Poly (PO) Layout Rules	Modify the rule description
94	PO.R.34	4.5.19	Poly (PO) Layout Rules	Add the new rule
95	CPO.DN.1.1	4.5.20	Cut-Poly (CPO) Layout Rules	Modify the rule description
96	CPO.DN.2	4.5.20	Cut-Poly (CPO) Layout Rules	Modify the rule description
97	CPO.DN.3	4.5.20	Cut-Poly (CPO) Layout Rules	Modify the rule description
98	CPO.R.1.1	4.5.20	Cut-Poly (CPO) Layout Rules	Modify the rule description
99	TPO.W.1	4.5.21	Trim PO (TPO) Layout Rules	Modify the rule description
100	TPO.S.1	4.5.21	Trim PO (TPO) Layout Rules	Modify the rule description
101	TPO.A.1	4.5.21	Trim PO (TPO) Layout Rules	Modify the rule description
102	TPO.A.2	4.5.21	Trim PO (TPO) Layout Rules	Modify the rule description
103	BPO.W.2	4.5.23	Butted PO (BPO) Layout Rules	Modify the rule description
104	BPO.R.5.1	4.5.23	Butted PO (BPO) Layout Rules	Modify the rule description
105	VT.W.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
106	VT.W.2.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
107	VT.S.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
108	VT.S.2.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
109	VT.S.2.4	4.5.24	VT (VTS_N, VTS_P, VTL_N,	Modify the rule description

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
			VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	
110	VT.EN.3	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
111	VT.EN.3.1	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
112	VT.A.1	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
113	VT.R.5	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
114	PP.S.11.3	4.5.25	P+ Source/Drain Ion Implantation (PP) Layout Rules	Modify the rule description
115	NP.S.11.3	4.5.26	N+ Source/Drain Ion Implantation (NP) Layout Rules	Modify the rule description
116	SSD.DN.1	4.5.27	Layout Rules for Strained S/D Mask Logical Operation	Modify the rule description
117	SSD.DN.2	4.5.27	Layout Rules for Strained S/D Mask Logical Operation	Modify the rule description
118	SSD.DN.5	4.5.27	Layout Rules for Strained S/D Mask Logical Operation	Modify the rule description
119	SSD.DN.6	4.5.27	Layout Rules for Strained S/D Mask Logical Operation	Modify the rule description
120	DIODMY.EN.2	4.5.28	DIODMY Layout Rules	Modify the rule description
121	RH_TN.R.4	4.5.29	High R Resistor Layout Rules	Modify the rule description
122	RH_TN.R.4.2	4.5.29	High R Resistor Layout Rules	Add the new rule
123	RH_TN.R.10	4.5.29	High R Resistor Layout Rules	Modify the rule description
124	MD.R.12.1	4.5.32	MD Layout Rules	Modify the rule description
125	CMD.S.3	4.5.33	Cut-MD (CMD) Layout Rules	Modify the rule description
126	CMD.S.3.1	4.5.33	Cut-MD (CMD) Layout Rules	Modify the rule description
127	CMD.S.3.2	4.5.33	Cut-MD (CMD) Layout Rules	Modify the rule description
128	CMD.R.10	4.5.33	Cut-MD (CMD) Layout Rules	Add the new rule
129	BCMD.R.6	4.5.34	Butted CMD (BCMD) Layout Rules	Modify the rule description
130	MP.DN.2.2	4.5.35	MP Layout Rules	Add the new rule
131	MP.R.3	4.5.35	MP Layout Rules	Modify the rule description
132	M0.W.3	4.5.38	M0 Layout Rules	Modify the rule description
133	M0.S.2.3	4.5.38	M0 Layout Rules	Modify the rule description
134	M0.S.2.3.1	4.5.38	M0 Layout Rules	Modify the rule description
135	M0.S.12	4.5.38	M0 Layout Rules	Modify the rule description
136	M0.S.12.1	4.5.38	M0 Layout Rules	Add the new rule
137	M0.DN.3.3	4.5.38	M0 Layout Rules	Modify the rule description
138	M0.DN.10.1	4.5.38	M0 Layout Rules	Add the new rule
139	M0.R.1	4.5.38	M0 Layout Rules	Modify the rule description
140	M0.R.12	4.5.38	M0 Layout Rules	Delete the rule
141	M0.R.17	4.5.38	M0 Layout Rules	Modify the rule description
142	M0.CS.1.1	4.5.38	M0 Layout Rules	Modify the rule description
143	M0.CS.1.2.1	4.5.38	M0 Layout Rules	Modify the rule description
144	M0.CS.1.3	4.5.38	M0 Layout Rules	Modify the rule description

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
145	M0.CS.3.14.1	4.5.38	M0 Layout Rules	Delete the rule
146	M0.CS.15	4.5.38	M0 Layout Rules	Modify the rule description
147	CM0A.W.1	4.5.39	Cut-M0 (CM0) Layout Rules	Modify the rule description
148	CM0A.L.1	4.5.39	Cut-M0 (CM0) Layout Rules	Modify the rule description
149	CM0B.W.1	4.5.39	Cut-M0 (CM0) Layout Rules	Modify the rule description
150	CM0B.L.1	4.5.39	Cut-M0 (CM0) Layout Rules	Modify the rule description
151	BCM0.R.5	4.5.40	Butted CM0 (BCM0) Layout Rules	Delete the rule
152	VIA0.S.12	4.5.41	VIA0 Layout Rules	Add the new rule
153	VIA0.EN.18	4.5.41	VIA0 Layout Rules	Modify the rule description
154	VIA0.R.14	4.5.41	VIA0 Layout Rules	Delete the rule
155	M1.W.3	4.5.42	M1 Layout Rules	Modify the rule description
156	M1.S.2	4.5.42	M1 Layout Rules	Modify the rule description
157	M1.S.2.0.1	4.5.42	M1 Layout Rules	Modify the rule description
158	M1.S.12	4.5.42	M1 Layout Rules	Modify the rule description
159	M1.S.12.1	4.5.42	M1 Layout Rules	Add the new rule
160	M1.S.37.4.T	4.5.42	M1 Layout Rules	Modify the rule description
161	M1.R.1	4.5.42	M1 Layout Rules	Modify the rule description
162	M1.R.17	4.5.42	M1 Layout Rules	Modify the rule description
163	M1.R.21	4.5.42	M1 Layout Rules	Add the new rule
164	M1.R.21.1	4.5.42	M1 Layout Rules	Add the new rule
165	VIAxs.S.3	4.5.43	VIAxs Layout Rules	Add the new rule
166	VIAxs.S.11	4.5.43	VIAxs Layout Rules	Modify the rule description
167	VIAxs.S.12	4.5.43	VIAxs Layout Rules	Add the new rule
168	VIAxs.S.12.1	4.5.43	VIAxs Layout Rules	Add the new rule
169	VIAxs.R.9®	4.5.43	VIAxs Layout Rules	Add the new rule
170	Mxs.W.1.1.0.1	4.5.44	Mxs Layout Rules	Modify the rule description
171	Mxs.W.3	4.5.44	Mxs Layout Rules	Modify the rule description
172	Mxs.S.12	4.5.44	Mxs Layout Rules	Modify the rule description
173	Mxs.S.12.1	4.5.44	Mxs Layout Rules	Add the new rule
174	Mxs.R.1	4.5.44	Mxs Layout Rules	Modify the rule description
175	Mxs.R.17	4.5.44	Mxs Layout Rules	Modify the rule description
176	Mxs.R.21.1	4.5.44	Mxs Layout Rules	Add the new rule
177	VIAx.S.11	4.5.45	VIAx Layout Rules	Modify the rule description
178	VIAx.R.9®	4.5.45	VIAx Layout Rules	Add the new rule
179	VIAx.R.14	4.5.45	VIAx Layout Rules	Delete the rule
180	Mx.W.3	4.5.46	Mx Layout Rules	Modify the rule description
181	Mx.S.12	4.5.46	Mx Layout Rules	Modify the rule description
182	Mx.S.12.1	4.5.46	Mx Layout Rules	Add the new rule
183	Mx.R.1	4.5.46	Mx Layout Rules	Modify the rule description
184	Mx.R.17	4.5.46	Mx Layout Rules	Modify the rule description
185	VIAxa.S.11	4.5.47	VIAxa Layout Rules	Modify the rule description
186	VIAxa.R.9®	4.5.47	VIAxa Layout Rules	Add the new rule
187	VIAxa.R.14	4.5.47	VIAxa Layout Rules	Delete the rule

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
188	Mxa.W.3	4.5.48	Mxa Layout Rules	Modify the rule description
189	Mxa.S.12	4.5.48	Mxa Layout Rules	Modify the rule description
190	Mxa.S.12.1	4.5.48	Mxa Layout Rules	Add the new rule
191	Mxa.R.1	4.5.48	Mxa Layout Rules	Modify the rule description
192	Mxa.R.17	4.5.48	Mxa Layout Rules	Modify the rule description
193	VIAya.S.12	4.5.49	VIAya Layout Rules	Modify the rule description
194	VIAya.R.14	4.5.49	VIAya Layout Rules	Delete the rule
195	VIAya.EN.31.6.1.T	4.5.49.1	VIAya Layout Rules	Modify the rule description
196	Mya.S.8.0.1	4.5.50	Mya Layout Rules	Modify the rule description
197	Mya.S.18	4.5.50	Mya Layout Rules	Modify the rule description
198	Mya.S.18.1	4.5.50	Mya Layout Rules	Add the new rule
199	Mya.S.27	4.5.50	Mya Layout Rules	Modify the rule description
200	Mya.S.27.1	4.5.50	Mya Layout Rules	Modify the rule description
201	Mya.R.17	4.5.50	Mya Layout Rules	Modify the rule description
202	VIAy.S.12	4.5.51	VIAy Layout Rules	Modify the rule description
203	VIAy.R.14	4.5.51	VIAy Layout Rules	Delete the rule
204	My.S.2.4.4	4.5.52	My Layout Rules	Modify the rule description
205	My.S.2.4.5	4.5.52	My Layout Rules	Modify the rule description
206	My.S.8.0.1	4.5.52	My Layout Rules	Modify the rule description
207	My.S.18	4.5.52	My Layout Rules	Modify the rule description
208	My.S.18.1	4.5.52	My Layout Rules	Add the new rule
209	My.S.27	4.5.52	My Layout Rules	Modify the rule description
210	My.S.27.1	4.5.52	My Layout Rules	Modify the rule description
211	My.R.17	4.5.52	My Layout Rules	Modify the rule description
212	VIAyy.R.14	4.5.53	VIAyy Layout Rules	Delete the rule
213	Myy.R.17	4.5.54	Myy Layout Rules	Modify the rule description
214	VIAyx.R.14	4.5.55	VIAyx Layout Rules	Delete the rule
215	Myx.R.17	4.5.56	Myx Layout Rules	Modify the rule description
216	VIAyz.EN.2	4.5.57	VIAyz Layout Rules	Modify the rule description
217	VIAyz.EN.3	4.5.57	VIAyz Layout Rules	Modify the rule description
218	VIAyz.R.2	4.5.57	VIAyz Layout Rules	Modify the rule description
219	VIAyz.R.3	4.5.57	VIAyz Layout Rules	Modify the rule description
220	VIAyz.R.4	4.5.57	VIAyz Layout Rules	Modify the rule description
221	VIAyz.R.5	4.5.57	VIAyz Layout Rules	Modify the rule description
222	VIAyz.R.6	4.5.57	VIAyz Layout Rules	Modify the rule description
223	VIAyz.R.7	4.5.57	VIAyz Layout Rules	Modify the rule description
224	VIAyz.R.13	4.5.57	VIAyz Layout Rules	Modify the rule description
225	VIAyz.R.14	4.5.57	VIAyz Layout Rules	Delete the rule
226	Myz.R.17	4.5.58	Myz Layout Rules	Modify the rule description
227	VIAz.EN.1	4.5.59	VIAz Layout Rules	Modify the rule description
228	VIAz.R.4	4.5.59	VIAz Layout Rules	Modify the rule description
229	VIAz.R.14	4.5.59	VIAz Layout Rules	Delete the rule
230	Mz.R.17	4.5.60	Mz Layout Rules	Modify the rule description
231	VIAr.EN.1	4.5.61	VIAr Layout Rules	Modify the rule description

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
232	VIA.R.4	4.5.61	VIA Layout Rules	Modify the rule description
233	VIA.R.14	4.5.61	VIA Layout Rules	Delete the rule
234	MR.R.17	4.5.62	MR Layout Rules	Modify the rule description
235	MOM.A.0	4.5.63	MOM Layout Rules	Modify the rule description
236	IND.R.2	4.5.64	INDDMY Layer Identified Inductor Layout Rules	Modify the rule description
237	IND.R.4	4.5.64	INDDMY Layer Identified Inductor Layout Rules	Modify the rule description
238	IND.R.10	4.5.64	INDDMY Layer Identified Inductor Layout Rules	Modify the rule description
239	SRAM.W.1.1	4.5.66	SRAM Layout Rules	Modify the rule description
240	SRAM.S.9	4.5.66	SRAM Layout Rules	Modify the rule description
241	SRAM.R.20	4.5.66	SRAM Layout Rules	Modify the rule description
242	SRAM.OD.R.1	4.5.66	SRAM Layout Rules	Modify the rule description
243	SRAM.COD_H.EX.1	4.5.66	SRAM Layout Rules	Modify the rule description
244	SRAM.COD_V.EX.1	4.5.66	SRAM Layout Rules	Modify the rule description
245	SRAM.COD_V.EX.1.1	4.5.66	SRAM Layout Rules	Modify the rule description
246	SRAM.COD_V.R.1	4.5.66	SRAM Layout Rules	Modify the rule description
247	SRAM.BPO.W.1	4.5.66	SRAM Layout Rules	Add the new rule
248	SRAM.BPO.R.5.1	4.5.66	SRAM Layout Rules	Modify the rule description
249	SRAM.BPO.R.5.2	4.5.66	SRAM Layout Rules	Add the new rule
250	SRAM.BPO.R.5.3	4.5.66	SRAM Layout Rules	Add the new rule
251	SRAM.CMD.R.1	4.5.66	SRAM Layout Rules	Modify the rule description
252	SRAM.MP.S.1	4.5.66	SRAM Layout Rules	Modify the rule description
253	SRAM.VC.R.3	4.5.66	SRAM Layout Rules	Modify the rule description
254	A.R.0	4.5.68	Antenna Effect Prevention (A) Layout Rules	Modify the rule description
255	A.R.6.4	4.5.68	Antenna Effect Prevention (A) Layout Rules	Add the new rule
256	A.R.8.3	4.5.68	Antenna Effect Prevention (A) Layout Rules	Add the new rule
257	A.R.8.4	4.5.68	Antenna Effect Prevention (A) Layout Rules	Add the new rule
258	A.R.8.5	4.5.68	Antenna Effect Prevention (A) Layout Rules	Add the new rule
259	A.R.8.2	4.5.68	Antenna Effect Prevention (A) Layout Rules	Delete the rule
260	A.R.15	4.5.68	Antenna Effect Prevention (A) Layout Rules	Add the new rule
261	AP.S.1	4.5.70	AI Redistribution Layer (AP RDL) Layout Rules [optional]	Modify the rule description
262	AP.R.1	4.5.70	AI Redistribution Layer (AP RDL) Layout Rules [optional]	Modify the rule description
263	SLR.PO.DN.7	4.5.71.1	Seal Ring Rules	Modify the rule description
264	SLR.PO.DN.8	4.5.71.1	Seal Ring Rules	Modify the rule description
265	CSR.R.2	4.5.71.2	Seal Ring Rules	Modify the rule description
266	CSR.R.6	4.5.71.2	Seal Ring Rules	Modify the rule description
267	CSR.DM.W.1	4.5.71.2	Seal Ring Rules	Modify the rule description
268	CSR.DM.S.1	4.5.71.2	Seal Ring Rules	Modify the rule description
269	CSR.DM.S.2	4.5.71.2	Seal Ring Rules	Modify the rule description
270	CSR.DM.O.1	4.5.71.2	Seal Ring Rules	Modify the rule description

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
271	CSR.DV.W.1	4.5.71.2	Seal Ring Rules	Modify the rule description
272	CSR.DV.S.1	4.5.71.2	Seal Ring Rules	Modify the rule description
273	CSR.DV.EN.1	4.5.71.2	Seal Ring Rules	Modify the rule description
274	SR.S.1	4.5.71.3.1	Seal Ring Rules	Delete the rule
275	SR.R.1	4.5.71.3.1	Seal Ring Rules	Modify the rule description
276	SR.R.7	4.5.71.3.1	Seal Ring Rules	Modify the rule description
277	SR.R.10	4.5.71.3.1	Seal Ring Rules	Add the new rule
278	SR.PM.R.3	4.5.71.3.1	Seal Ring Rules	Modify the rule description
279	SR.DM.W.1	4.5.71.3.2	Seal Ring Rules	Modify the rule description
280	SR.DM.S.1	4.5.71.3.2	Seal Ring Rules	Modify the rule description
281	SR.DM.S.2	4.5.71.3.2	Seal Ring Rules	Modify the rule description
282	SR.DM.O.1	4.5.71.3.2	Seal Ring Rules	Modify the rule description
283	SR.DV.W.1	4.5.71.3.2	Seal Ring Rules	Modify the rule description
284	SR.DV.S.1	4.5.71.3.2	Seal Ring Rules	Modify the rule description
285	SR.DV.EN.1	4.5.71.3.2	Seal Ring Rules	Modify the rule description
286	MIM.VIAz.EN.1.1	4.5.73.4.1	HD MIM Layout Rules	Modify the rule description
287	MIM.VIAz.EN.1.2	4.5.73.4.1	HD MIM Layout Rules	Modify the rule description
288	MIM.VIAz.R.3	4.5.73.4.1	HD MIM Layout Rules	Add the new rule
289	MIM.VIAz.R.4	4.5.73.4.1	HD MIM Layout Rules	Add the new rule
290	MIM.VIAr.EN.1.1	4.5.73.4.2	HD MIM Layout Rules	Modify the rule description
291	MIM.VIAr.EN.1.2	4.5.73.4.2	HD MIM Layout Rules	Modify the rule description
292	MIM.VIAr.R.3	4.5.73.4.2	HD MIM Layout Rules	Add the new rule
293	MIM.VIAr.R.4	4.5.73.4.2	HD MIM Layout Rules	Add the new rule
294	KOZ.R.7	4.5.73.6	HD MIM Layout Rules	Add the new rule
295	KOZ.R.8	4.5.73.6	HD MIM Layout Rules	Add the new rule
296	DMn.EN.1	6.2	DUMMY METAL (DM) RULES	Add the new rule
297	DMn.EN.1.1	6.2	DUMMY METAL (DM) RULES	Add the new rule
298	DMn.EN.2	6.2	DUMMY METAL (DM) RULES	Add the new rule
299	DMn.EN.2.1	6.2	DUMMY METAL (DM) RULES	Add the new rule
300	DMn.EN.3	6.2	DUMMY METAL (DM) RULES	Add the new rule
301	DMn.EN.3.1	6.2	DUMMY METAL (DM) RULES	Add the new rule
302	DCPODE.R.4	6.4	DUMMY CPODE (DCPODE) RULES	Modify the rule description
303	DTCD.R.9.1	6.5.1.1	Dummy TCD Rules	Modify the rule description
304	ICOVL.S.1	6.6.1	In Chip Overlay (ICOVL) Introduction	Modify the rule description
305	ICOVL.R.5.1	6.6.1	In Chip Overlay (ICOVL) Introduction	Delete the rule
306	ICOVL.R.50	6.6.1	In Chip Overlay (ICOVL) Introduction	Modify the rule description
307	M0.DN.9.IP_TIGHTEN_LED	6.7.1.1	IP_TIGHTEN_DENSITY Switch	Add the new rule
308	M1.DN.9.IP_TIGHTEN_LED	6.7.1.1	IP_TIGHTEN_DENSITY Switch	Add the new rule
309	Mxs.DN.9.IP_TIGHTEN_LED	6.7.1.1	IP_TIGHTEN_DENSITY Switch	Add the new rule
310	Mx.DN.9.IP_TIGHTEN_LED	6.7.1.1	IP_TIGHTEN_DENSITY Switch	Add the new rule
311	Mxa.DN.9.IP_TIGHTEN_LED	6.7.1.1	IP_TIGHTEN_DENSITY Switch	Add the new rule
312	VIAx.R.9®	7.2.1	Recommendations	Add the new rule

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
313	VIAxs.R.9®	7.2.1	Recommendations	Add the new rule
314	VIAxa.R.9®	7.2.1	Recommendations	Add the new rule
315	MIM.VIAz.S.10®	7.2.1	Recommendations	Add the new rule
316	MIM.VIAz.S.10.2®	7.2.1	Recommendations	Add the new rule
317	MIM.VIAz.R.2®	7.2.1	Recommendations	Add the new rule
318	MIM.VIAz.R.2.1®	7.2.1	Recommendations	Add the new rule
319	MIM.VIAr.S.10®	7.2.1	Recommendations	Add the new rule
320	MIM.VIAr.S.10.2®	7.2.1	Recommendations	Add the new rule
321	MIM.VIAr.R.2®	7.2.1	Recommendations	Add the new rule
322	MIM.VIAr.R.2.1®	7.2.1	Recommendations	Add the new rule
323	LUP.WARN.1	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
324	LUP.WARN.5	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
325	LUP.1	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
326	LUP.1.0.1U	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
327	LUP.1.1	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
328	LUP.2	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
329	LUP.2.0.1U	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
330	LUP.2.1U	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
331	LUP.2.2	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
332	LUP.2.3	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
333	LUP.2.4	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
334	LUP.2.5	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
335	LUP.2.6	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
336	LUP.4.1	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
337	LUP.4.2U	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
338	LUP.4.3U	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Delete the rule
339	LUP.6	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
340	LUP.6.1	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
341	LUP.6.2	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
342	LUP.7.6	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
343	LUP.9U	9.1.2.1	Layout Rules and Guidelines for Latch-up Prevention	Delete the rule
344	LUP.10	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
345	LUP.12	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Delete the rule
346	LUP.13	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
			Latch-up Prevention	
347	LUP.13.0.1	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
348	LUP.13.0.2	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
349	LUP.13.0.3	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
350	LUP.13.0.4	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
351	LUP.13.0.5	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
352	LUP.13.0.6	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
353	LUP.13.1	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
354	LUP.13.1.1	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
355	LUP.13.1.2	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
356	LUP.13.1.3	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
357	LUP.13.1.4	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
358	LUP.13.1.5	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
359	LUP.13.1.6	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
360	LUP.13.2	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
361	LUP.13.2.1	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
362	LUP.13.2.2	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
363	LUP.13.2.3	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
364	LUP.13.2.4	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
365	LUP.13.2.5	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
366	LUP.13.2.6	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Add the new rule
367	LUP.14	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
368	LUP.14.0.1U	9.1.2.2	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
369	SR_ESD.R.3	9.2.3	SR_ESD device Layout Rules	Add the new rule
370	ESD.NET.1gU	9.2.6.1	ESD Guidelines	Modify the rule description
371	ESD.NET.1.1gU	9.2.6.1	ESD Guidelines	Modify the rule description
372	ESD.WARN.3.1gU	9.2.6.1	ESD Guidelines	Modify the rule description
373	ESD.WARN.3.2gU	9.2.6.1	ESD Guidelines	Delete the rule
374	ESD.WARN.4.1gU	9.2.6.1	ESD Guidelines	Delete the rule
375	ESD.1g	9.2.6.1	ESD Guidelines	Modify the rule description
376	ESD.8gU	9.2.6.1	ESD Guidelines	Modify the rule description
377	ESD.9.0gU	9.2.6.1	ESD Guidelines	Modify the rule description
378	ESD.14.7gU	9.2.6.1	ESD Guidelines	Modify the rule description
379	ESD.38	9.2.6.2	ESD Guidelines	Modify the rule description

No.	Rule	Sec. No.	Section Title	V0.9 Revision Description
380	ESD.31g	9.2.6.4	ESD Guidelines	Modify the rule description
381	ESD.40g	9.2.6.5	ESD Guidelines	Modify the rule description
382	ESD.40.1g	9.2.6.5	ESD Guidelines	Modify the rule description
383	ESD.40.2gU	9.2.6.5	ESD Guidelines	Modify the rule description
384	ESD.42.1gU	9.2.6.5	ESD Guidelines	Modify the rule description
385	ESD.LC.3g	9.2.6.7.1.1	ESD Guidelines	Modify the rule description
386	ESD.LC.8gU	9.2.6.7.1.1	ESD Guidelines	Delete the rule
387	ESD.LC.9gU	9.2.6.7.1.1	ESD Guidelines	Delete the rule
388	ESD.LC.9.1gU	9.2.6.7.1.1	ESD Guidelines	Delete the rule
389	ESD.45.0gU	9.2.7.1	CDM Protection for Cross Domain Interface	Modify the rule description
390	ESD.45.0.1gU	9.2.7.1	CDM Protection for Cross Domain Interface	Modify the rule description
391	ESD.45.0.2gU	9.2.7.1	CDM Protection for Cross Domain Interface	Modify the rule description
392	ESD.45.1gU	9.2.7.1	CDM Protection for Cross Domain Interface	Modify the rule description
393	ESD.47gU	9.2.7.1	CDM Protection for Cross Domain Interface	Modify the rule description
394	ESD.CDM.1gU	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
395	ESD.CDM.1.1gU	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
396	ESD.CDM.1.2gU	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
397	ESD.CDM.2gU	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
398	ESD.CDM.6.1g	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
399	ESD.CDM.C.2gU	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
400	ESD.CDM.C.3.1gU	9.2.7.2	CDM Protection for Cross Domain Interface	Add the new rule
401	ESD.CDM.C.3.2gU	9.2.7.2	CDM Protection for Cross Domain Interface	Add the new rule
402	ESD.CDM.P.7.2gU	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
403	ESD.CDM.P.7.3gU	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
404	ESD.CDM.P.7.5gU	9.2.7.2	CDM Protection for Cross Domain Interface	Modify the rule description
405	MJ_M1.R.1	11.2.2.1	Must-Join Pin Rules	Add the new rule
406	MJ_M1.R.2	11.2.2.1	Must-Join Pin Rules	Add the new rule
407	MJ_M1.R.3	11.2.2.1	Must-Join Pin Rules	Add the new rule
408	MJ_M2.R.1	11.2.2.1	Must-Join Pin Rules	Add the new rule
409	MJ_M2.R.2	11.2.2.1	Must-Join Pin Rules	Add the new rule
410	MJ_M2.R.3	11.2.2.1	Must-Join Pin Rules	Add the new rule

12.2 A.2 From Version 0.9 to Version 1.0

No.	Rule	Sec. No.	Section Title	V1.0 Revision Description
1	OPC.R.2g ^U	3.6.2	OPC Recommendations and Guidelines	Delete the rule
2	OD.S.25	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Modify the rule description
3	OD.A.7	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Modify the rule description
4	OD.A.7.1	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Modify the rule description
5	OD.A.8	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Modify the rule description
6	OD.A.8.2	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Modify the rule description
7	OD.A.9	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Modify the rule description
8	OD.R.4 ^U	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Delete the rule
9	OD.R.5.1	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Modify the rule description
10	NW.S.2	4.5.6	N-Well (NW) Layout Rules	Modify the rule description
11	NW.R.2 ^U	4.5.6	N-Well (NW) Layout Rules	Delete the rule
12	H240.VC.EN.1	4.5.13.3	Cell Height 240 (H240) Layout Rules	Modify the rule description
13	H240.VC.EN.1.1	4.5.13.3	Cell Height 240 (H240) Layout Rules	Modify the rule description
14	H240.VC.EN.1.3	4.5.13.3	Cell Height 240 (H240) Layout Rules	Modify the rule description
15	H300.VC.EN.1	4.5.13.4	Cell Height 300 (H300) Layout Rules	Modify the rule description
16	H300.VC.EN.1.1	4.5.13.4	Cell Height 300 (H300) Layout Rules	Modify the rule description
17	H300.VC.EN.1.3	4.5.13.4	Cell Height 300 (H300) Layout Rules	Modify the rule description
18	CPODE.W.3	4.5.17	Connected PODE (CPODE) Layout Rules (172N, 82N)	Modify the rule description
19	CPODE.S.3	4.5.17	Connected PODE (CPODE) Layout Rules (172N, 82N)	Modify the rule description
20	CPODE.L.2	4.5.17	Connected PODE (CPODE) Layout Rules (172N, 82N)	Add the rule
21	CPODE.L.2 [®]	4.5.17	Connected PODE (CPODE) Layout Rules (172N, 82N)	Delete the rule
22	CPODE.R.2	4.5.17	Connected PODE (CPODE) Layout Rules (172N, 82N)	Modify the rule description
23	CPODE.R.8.1	4.5.17	Connected PODE (CPODE) Layout Rules (172N, 82N)	Modify the rule description
24	PO.S.3.2	4.5.19	Poly (PO) Layout Rules	Modify the rule description
25	PO.R.2	4.5.19	Poly (PO) Layout Rules	Modify the rule description
26	PO.R.2.1	4.5.19	Poly (PO) Layout Rules	Add the rule
27	PO.R.20 ^U	4.5.19	Poly (PO) Layout Rules	Delete the rule
28	TPO.W.1	4.5.21	Trim PO (TPO) Layout Rules	Modify the rule description
29	TPO.S.1	4.5.21	Trim PO (TPO) Layout Rules	Modify the rule description
30	BPO.R.5.1	4.5.23	Butted PO (BPO) Layout Rules	Modify the rule description

No.	Rule	Sec. No.	Section Title	V1.0 Revision Description
31	VT.W.1	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
32	VT.W.1.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
33	VT.W.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
34	VT.W.2.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
35	VT.S.1	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
36	VT.S.1.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
37	VT.S.1.4	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
38	VT.S.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
39	VT.S.2.2	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
40	VT.S.2.4	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
41	VT.R.5	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
42	VT.R.11	4.5.24	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Modify the rule description
43	MP.S.3.1	4.5.35	MP Layout Rules	Add the rule
44	MP.R.8.2	4.5.35	MP Layout Rules	Add the rule
45	VC.W.1	4.5.36	VC Layout Rules	Modify the rule description
46	VC.S.5.4	4.5.36	VC Layout Rules	Add the rule
47	VC.EN.1	4.5.36	VC Layout Rules	Modify the rule description
48	VC.EN.1.1	4.5.36	VC Layout Rules	Modify the rule description
49	VC.EN.2	4.5.36	VC Layout Rules	Modify the rule description
50	VC.R.1.2	4.5.36	VC Layout Rules	Modify the rule description
51	VC.R.9.5	4.5.36	VC Layout Rules	Modify the rule description
52	M0.DN.3.3	4.5.38	M0 Layout Rules	Modify the rule description
53	M0.R.4 ^U	4.5.38	M0 Layout Rules	Delete the rule
54	M1.S.35.2.1.T	4.5.42	M1 Layout Rules	Modify the rule description
55	M1.R.4 ^U	4.5.38	M1 Layout Rules	Delete the rule
56	M1.R.31.2	4.5.38	M1 Layout Rules	Modify the rule description
57	Mxs.R.4 ^U	4.5.44	Mxs Layout Rules	Delete the rule
58	Mx.R.4 ^U	4.5.46	Mx Layout Rules	Delete the rule
59	Mxa.R.4 ^U	4.5.48	Mxa Layout Rules	Delete the rule
60	Mya.R.5 ^U	4.5.50	Mya Layout Rules	Delete the rule

No.	Rule	Sec. No.	Section Title	V1.0 Revision Description
61	My.R.5 ^U	4.5.52	My Layout Rules	Delete the rule
62	VIAyy.R.9g ^U	4.5.53	VIAyy Layout Rules	Modify the rule description
63	Myy.R.2g ^U	4.5.54	Myy Layout Rules	Delete the rule
64	Myy.R.4 ^U	4.5.54	Myy Layout Rules	Delete the rule
65	Myy.R.14® ^U	4.5.54	Myy Layout Rules	Delete the rule
66	Myx.R.4 ^U	4.5.56	Myx Layout Rules	Delete the rule
67	Myz.R.5 ^U	4.5.58	Myz Layout Rules	Delete the rule
68	Mz.R.4 ^U	4.5.60	Mz Layout Rules	Delete the rule
69	VIAr.R.5g ^U	4.5.61	VIAr Layout Rules	Delete the rule
70	Mr.R.4 ^U	4.5.62	Mr Layout Rules	Delete the rule
71	IND.R.10	4.5.64	INDDMY Layer Identified Inductor Layout Rules	Modify the rule description
72	SRAM.W.5	4.5.66	SRAM Layout Rules	Modify the rule description
73	SRAM.W.5.1	4.5.66	SRAM Layout Rules	Modify the rule description
74	SRAM.R.38	4.5.66	SRAM Layout Rules	Add the rule
75	SRAM.R.38.1	4.5.66	SRAM Layout Rules	Add the rule
76	SRAM.VC.R.9.1	4.5.66	SRAM Layout Rules	Add the rule
77	SRAM.VIA0.S.31.1	4.5.66	SRAM Layout Rules	Add the rule
78	RV.R.2	4.5.69	RV Layout Rules [optional]	Modify the rule description
79	CSR.W.1	4.5.71.4	Chip Corner Stress Relief (CSR) Pattern	Modify the rule description
80	MIM.VIAz.S.9	4.5.73.4.1	VIAz Layout Rules for HD MIM	Modify the rule description
81	KOZ.R.3	4.5.73.7	Keep-out Zone Layout Rules for HD MIM Capacitor	Modify the rule description
82	KOZ.R.4	4.5.73.7	Keep-out Zone Layout Rules for HD MIM Capacitor	Modify the rule description
83	EFP.M0.EN.1	4.5.74	Extensive Forbidden Pattern (EFP) Rules	Add the rule
84	DC.S.5	6.1	Dummy Cell Rules	Add the rule
85	DC.S.6.T	6.1	Dummy Cell Rules	Add the rule
86	DC.S.6.1.T	6.1	Dummy Cell Rules	Add the rule
87	DC.S.6.2.T	6.1	Dummy Cell Rules	Add the rule
88	DC.S.6.3.T	6.1	Dummy Cell Rules	Add the rule
89	DC.S.6.4.T	6.1	Dummy Cell Rules	Add the rule
90	DC.S.6.5.T	6.1	Dummy Cell Rules	Add the rule
91	DC.S.6.6.T	6.1	Dummy Cell Rules	Add the rule
92	DC.S.7.T	6.1	Dummy Cell Rules	Add the rule
93	DC.S.7.1.T	6.1	Dummy Cell Rules	Add the rule
94	DC.S.7.2.T	6.1	Dummy Cell Rules	Add the rule
95	DC.S.7.3.T	6.1	Dummy Cell Rules	Add the rule
96	DC.S.7.4.T	6.1	Dummy Cell Rules	Add the rule
97	DC.S.8.T	6.1	Dummy Cell Rules	Add the rule
98	DC.S.8.1.T	6.1	Dummy Cell Rules	Add the rule
99	DC.S.9.T	6.1	Dummy Cell Rules	Add the rule
100	DC.S.9.1.T	6.1	Dummy Cell Rules	Add the rule
101	DC.S.9.2.T	6.1	Dummy Cell Rules	Add the rule
102	DC.S.9.3.T	6.1	Dummy Cell Rules	Add the rule

No.	Rule	Sec. No.	Section Title	V1.0 Revision Description
103	DC.R.2.1.T	6.1	Dummy Cell Rules	Add the rule
104	DC.R.2.2.T	6.1	Dummy Cell Rules	Add the rule
105	DC.R.2.3.T	6.1	Dummy Cell Rules	Add the rule
106	DC.R.2.4.T	6.1	Dummy Cell Rules	Add the rule
107	DC.R.2.5.T	6.1	Dummy Cell Rules	Add the rule
108	DC.R.2.6.T	6.1	Dummy Cell Rules	Add the rule
109	DC.R.2.7.T	6.1	Dummy Cell Rules	Add the rule
110	DC.R.2.8.T	6.1	Dummy Cell Rules	Add the rule
111	DC.R.3.1.T	6.1	Dummy Cell Rules	Add the rule
112	DC.R.3.2.T	6.1	Dummy Cell Rules	Add the rule
113	DC.R.4.T	6.1	Dummy Cell Rules	Add the rule
114	DC.R.5.1.T	6.1	Dummy Cell Rules	Add the rule
115	DC.R.5.2.T	6.1	Dummy Cell Rules	Add the rule
116	DC.R.6.T	6.1	Dummy Cell Rules	Add the rule
117	DMn.S.2.6	6.2	Dummy Metal (DM) Rules	Modify the rule description
118	DMn.S.2.7	6.2	Dummy Metal (DM) Rules	Modify the rule description
119	DMn.R.7	6.2	Dummy Metal (DM) Rules	Modify the rule description
120	DMn.R.7.1	6.2	Dummy Metal (DM) Rules	Modify the rule description
121	DVIA.n.EN.1	6.3	Dummy VIA (DVIA) Rules	Modify the rule description
122	DVIA.n.EN.1.0.1	6.3	Dummy VIA (DVIA) Rules	Modify the rule description
123	DVIA.n.EN.1.1	6.3	Dummy VIA (DVIA) Rules	Modify the rule description
124	DTCD.R.11	6.5.1.1	Dummy TCD Rules	Modify the rule description
125	LUP.WARN.3.1U	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Add the rule
126	LUP.WARN.5	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
127	LUP.2	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
128	LUP.2.0.1 ^U	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
129	LUP.2.1 ^U	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
130	LUP.2.2	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
131	LUP.2.3	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
132	LUP.2.4	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
133	LUP.2.5	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
134	LUP.2.6	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
135	LUP.4.1	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
136	LUP.4.2 ^U	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
137	LUP.6	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
138	LUP.6.1	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
139	LUP.6.2	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description

No.	Rule	Sec. No.	Section Title	V1.0 Revision Description
140	LUP.7.6	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify the rule description
141	LUP.10	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
142	LUP.13	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
143	LUP.13.0.1	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
144	LUP.13.0.2	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
145	LUP.13.0.4	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
146	LUP.13.0.5	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
147	LUP.13.1	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
148	LUP.13.1.1	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
149	LUP.13.1.2	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
150	LUP.13.1.4	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
151	LUP.13.1.5	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
152	LUP.13.2	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
153	LUP.13.2.1	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
154	LUP.13.2.2	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
155	LUP.13.2.4	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
156	LUP.13.2.5	9.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Modify the rule description
157	SR_ESD.R.7 ^U	9.2.3	SR_ESD device Layout Rules	Add the rule
158	ESD.NET.1g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
159	ESD.NET.1.1g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
160	ESD.WARN.1	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
161	ESD.WARN.3g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
162	ESD.WARN.3.1g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
163	ESD.1.1g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
164	ESD.8g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
165	ESD.CDM7A.8.1g ^U	9.2.6.2	General Guideline for ESD Protection	Add the rule
166	ESD.CDM9A.8.1g ^U	9.2.6.2	General Guideline for ESD Protection	Add the rule
167	ESD.CDM14A.8.1g ^U	9.2.6.2	General Guideline for ESD Protection	Add the rule
168	ESD.9.0g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
169	ESD.9.0.1g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
170	ESD.9.1g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description

No.	Rule	Sec. No.	Section Title	V1.0 Revision Description
171	ESD.9.1.1g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
	ESD.9.1.2g ^U	9.2.6.2	General Guideline for ESD Protection	Modify the rule description
172	ESD.9.1.3g ^U	9.2.6.2	General Guideline for ESD Protection	Add the rule
173	ESD.9.5g ^U	9.2.6.2	General Guideline for ESD Protection	Add the rule
174	ESD.15g	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Modify the rule description
175	ESD.18g	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Modify the rule description
176	ESD.CDM7A.18g	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Add the rule
177	ESD.CDM9A.18g	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Add the rule
178	ESD.CDM14A.18g	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Add the rule
179	ESD.36	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Modify the rule description
180	ESD.36.1	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Modify the rule description
181	ESD.36.2g	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Add the rule
182	ESD.37	9.2.6.3	1.8V Drain-Ballasted NMOS for ESD	Modify the rule description
183	ESD.27g	9.2.6.4	1.8V Drain-Ballasted 2 stage/3 stage Cascoded NMOS for ESD	Modify the rule description
184	ESD.CDM7A.27g	9.2.6.4	1.8V Drain-Ballasted 2 stage/3 stage Cascoded NMOS for ESD	Add the rule
185	ESD.CDM9A.27g	9.2.6.4	1.8V Drain-Ballasted 2 stage/3 stage Cascoded NMOS for ESD	Add the rule
186	ESD.CDM14A.27g	9.2.6.4	1.8V Drain-Ballasted 2 stage/3 stage Cascoded NMOS for ESD	Add the rule
187	ESD.29g	9.2.6.4	1.8V Drain-Ballasted 2 stage/3 stage Cascoded NMOS for ESD	Modify the rule description
188	ESD.35g ^U	9.2.6.4	1.8V Drain-Ballasted 2 stage/3 stage Cascoded NMOS for ESD	Modify the rule description
189	ESD.CDM7A.40g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
190	ESD.CDM9A.40g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
191	ESD.CDM14A.40g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
192	ESD.CDM7A.40.1g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
193	ESD.CDM9A.40.1g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
194	ESD.CDM14A.40.1g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
195	ESD.CDM7A.40.2g ^U	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
196	ESD.CDM9A.40.2g ^U	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
197	ESD.CDM14A.40.2g ^U	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
198	ESD.CDM7A.40.3g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
199	ESD.CDM9A.40.3g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
200	ESD.CDM14A.40.3g	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
201	ESD.CDM7A.40.3.1g ^U	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
202	ESD.CDM9A.40.3.1g ^U	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
203	ESD.CDM14A.40.3.1g ^U	9.2.6.6	Power Clamp Device (Ncs/Pcs)	Add the rule
204	HIA.CDM7A.3g	9.2.6.7.2.1.2	High current diodes layout guidelines (STI-bounded)	Add the rule

No.	Rule	Sec. No.	Section Title	V1.0 Revision Description
			junction diode)	
205	HIA.CDM9A.3g	9.2.6.7.2.1.2	High current diodes layout guidelines (STI-bounded junction diode)	Add the rule
206	HIA.CDM14A.3g	9.2.6.7.2.1.2	High current diodes layout guidelines (STI-bounded junction diode)	Add the rule
207	HIA.CDM7A.3.1g	9.2.6.7.2.1.2	High current diodes layout guidelines (STI-bounded junction diode)	Add the rule
208	HIA.CDM9A.3.1g	9.2.6.7.2.1.2	High current diodes layout guidelines (STI-bounded junction diode)	Add the rule
209	HIA.CDM14A.3.1g	9.2.6.7.2.1.2	High current diodes layout guidelines (STI-bounded junction diode)	Add the rule
210	ESD.CDM7A.LC.3g	9.2.6.8.1.2	Low Capacitance HIA_DIO Layout Guidelines	Add the rule
211	ESD.CDM9A.LC.3g	9.2.6.8.1.2	Low Capacitance HIA_DIO Layout Guidelines	Add the rule
212	ESD.CDM14A.LC.3g	9.2.6.8.1.2	Low Capacitance HIA_DIO Layout Guidelines	Add the rule
213	ESD.CDM7A.LC.3.1g	9.2.6.8.1.2	Low Capacitance HIA_DIO Layout Guidelines	Add the rule
214	ESD.CDM9A.LC.3.1g	9.2.6.8.1.2	Low Capacitance HIA_DIO Layout Guidelines	Add the rule
215	ESD.CDM14A.LC.3.1g	9.2.6.8.1.2	Low Capacitance HIA_DIO Layout Guidelines	Add the rule
216	ESD.LCP2P.1g ^U	9.2.6.8.1.2	Low Capacitance HIA_DIO Layout Guidelines	Modify the rule description
217	ESD.LCP2P.2g ^U	9.2.6.8.1.2	Low Capacitance HIA_DIO Layout Guidelines	Modify the rule description
218	ESD.CDM.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
219	ESD.CDM.1.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
220	ESD.CDM.1.3g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
221	ESD.CDM.1.2g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
222	ESD.CDM.2g ^U	9.2.7.3	General Guideline for CDM Protection	Delete the rule
223	ESD.CDM.A.1g ^U	9.2.7.3	General Guideline for CDM Protection	Delete the rule
224	ESD.CDM.B.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
225	ESD.CDM.B.2g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
226	ESD.CDM.4g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
227	ESD.CDM14A.4.1g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
228	ESD.CDM.C.2g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
229	ESD.CDM.C.3.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
230	ESD.CDM.C.3.2g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
231	ESD.CDM.C.4g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule

No.	Rule	Sec. No.	Section Title	V1.0 Revision Description
232	ESD.CDM.C.4.1g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
233	ESD.CDM.C.5g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
234	ESD.CDM.X.1g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
235	ESD.XDM.VIC.3g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
236	ESD.XDM.VIC.4g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
237	ESD.CDM.P.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
238	ESD.CDM.P.1.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
239	ESD.CDM.P.2g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
240	ESD.CDM.P.3g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
241	ESD.CDM.P.4g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
242	ESD.CDM.P.5g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
243	ESD.CDM.P.7g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
244	ESD.CDM.P.7.1.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
245	ESD.CDM.P.7.1.2g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
246	ESD.CDM.P.7.2g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
247	ESD.CDM.P.7.3g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
248	ESD.CDM.P.7.4g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
249	ESD.CDM.P.7.5g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
250	ESD.CDM.P.8g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
251	ESD.CDM.P.9g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
252	ESD.CDM.P.10g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
253	ESD.XDM.P.1g ^U	9.2.7.3	General Guideline for CDM Protection	Add the rule
254	ESD.DISTP2P.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
255	ESD.DISTP2P.1.1g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
256	ESD.DISTP2P.1.2g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
257	ESD.DISTP2P.1.3g ^U	9.2.7.3	General Guideline for CDM Protection	Modify the rule description
258	ESD.CD.1g ^U	9.3.5	Minimum ESD Current for ESD device	Modify the rule description
259	ESD.CD.2g ^U	9.3.5	Minimum ESD Current for ESD device	Modify the rule description

12.3 A.3 From Version 1.0 to Version 1.0_1

No.	Rule	Sec. No.	Section Title	V1.0_1 Revision Description
1	DC.S.5	6.1	Dummy Cell Rules	Modify the rule description
2	DC.R.3.1.T	6.1	Dummy Cell Rules	Modify the rule description
3	DC.R.3.2.T	6.1	Dummy Cell Rules	Modify the rule description

TSMC Confidential Information
938214
VIAI CPU Platform Col., I Ltd.
10/05/2018

12.4 A.4 From Version 1.0_1 to Version 1.0_2

No.	Rule	Sec. No.	Section Title	V1.0_2 Revision Description
1	OD.S.1.0.2	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Add the rule
2	OD.S.22.7	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Add the rule
3	OD.S.22.8.1	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Add the rule
4	OD.L.5.0.2	4.5.3	Gate Oxide and Diffusion (OD) Layout Rules	Add the rule
5	CPODE.R.2.1	4.5.17	Connected PODE (CPODE) Layout Rules (72N, 82N)	Modify the rule description
6	PO_P63.R.9	4.5.18	Poly Pitch 0.063 μm (PO_P63) Layout Rules	Modify the rule description
7	PO_P63.R.10	4.5.18	Poly Pitch 0.063 μm (PO_P63) Layout Rules	Add the rule
8	PO_P76.W.1	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
9	PO_P76.S.2	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
10	PO_P76.EN.2	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
11	PO_P76.R.1	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
12	PO_P76.R.2	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
13	PO_P76.R.3	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
14	PO_P76.R.5	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
15	PO_P76.R.7	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
16	PO_P76.R.8	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
17	PO_P76.R.9	4.5.19	Poly Pitch 0.076 μm (PO_P76) Layout Rules	Add the rule
18	PO.W.11	4.5.20	Poly (PO) Layout Rules	Modify the rule description
19	PO.W.11.1	4.5.20	Poly (PO) Layout Rules	Modify the rule description
20	PO.W.12	4.5.20	Poly (PO) Layout Rules	Modify the rule description
21	PO.W.12.1	4.5.20	Poly (PO) Layout Rules	Modify the rule description
22	PO.W.14	4.5.20	Poly (PO) Layout Rules	Modify the rule description
23	PO.S.1.0.2	4.5.20	Poly (PO) Layout Rules	Add the rule
24	PO.S.1.2	4.5.20	Poly (PO) Layout Rules	Modify the rule description
25	PO.S.1.2.3	4.5.20	Poly (PO) Layout Rules	Add the rule
26	PO.S.13.1	4.5.20	Poly (PO) Layout Rules	Modify the rule description
27	PO.S.13.2	4.5.20	Poly (PO) Layout Rules	Modify the rule description
28	PO.S.16	4.5.20	Poly (PO) Layout Rules	Modify the rule description
29	PO.S.16.3	4.5.20	Poly (PO) Layout Rules	Modify the rule description
30	PO.S.16.5	4.5.20	Poly (PO) Layout Rules	Modify the rule description
31	PO.S.19.1	4.5.20	Poly (PO) Layout Rules	Add the rule
32	PO.S.19.2	4.5.20	Poly (PO) Layout Rules	Add the rule

No.	Rule	Sec. No.	Section Title	V1.0_2 Revision Description
33	PO.S.19.3	4.5.20	Poly (PO) Layout Rules	Add the rule
34	PO.S.19.4	4.5.20	Poly (PO) Layout Rules	Add the rule
35	PO.S.19.5	4.5.20	Poly (PO) Layout Rules	Add the rule
36	PO.S.22.1.1	4.5.20	Poly (PO) Layout Rules	Modify the rule description
37	PO.S.22.1.1.2	4.5.20	Poly (PO) Layout Rules	Add the rule
38	PO.S.22.1.2	4.5.20	Poly (PO) Layout Rules	Modify the rule description
39	PO.S.22.1.2.2	4.5.20	Poly (PO) Layout Rules	Add the rule
40	PO.EN.1.4	4.5.20	Poly (PO) Layout Rules	Add the rule
41	PO.L.5	4.5.20	Poly (PO) Layout Rules	Modify the rule description
42	PO.L.5.0.2	4.5.20	Poly (PO) Layout Rules	Add the rule
43	PO.L.5.1	4.5.20	Poly (PO) Layout Rules	Modify the rule description
44	PO.L.5.1.2	4.5.20	Poly (PO) Layout Rules	Add the rule
45	PO.L.5.2	4.5.20	Poly (PO) Layout Rules	Modify the rule description
46	PO.L.5.2.2	4.5.20	Poly (PO) Layout Rules	Add the rule
47	PO.A.7	4.5.20	Poly (PO) Layout Rules	Modify the rule description
48	PO.R.15.2.2	4.5.20	Poly (PO) Layout Rules	Add the rule
49	PO.R.15.7	4.5.20	Poly (PO) Layout Rules	Add the rule
50	CPO.S.2.0.2	4.5.21	Cut-Poly (CPO) Layout Rules	Add the rule
51	CPO.S.2.4.2	4.5.21	Cut-Poly (CPO) Layout Rules	Add the rule
52	CPO.S.4.1.1	4.5.21	Cut-Poly (CPO) Layout Rules	Add the rule
53	CPO.S.4.6	4.5.21	Cut-Poly (CPO) Layout Rules	Add the rule
54	CPO.EX.1	4.5.20	Poly (PO) Layout Rules	Modify the rule description
55	CPO.EX.1.0.2	4.5.20	Poly (PO) Layout Rules	Add the rule
56	CPO.EX.1.5	4.5.20	Poly (PO) Layout Rules	Modify the rule description
57	CPO.R.15.2	4.5.20	Poly (PO) Layout Rules	Add the rule
58	TPO.W.1.2	4.5.22	Trim PO (TPO) Layout Rules	Add the rule
59	TPO.W.2.2	4.5.22	Trim PO (TPO) Layout Rules	Add the rule
60	TPO.S.1.2	4.5.22	Trim PO (TPO) Layout Rules	Add the rule
61	TPO.S.2.0.2	4.5.22	Trim PO (TPO) Layout Rules	Add the rule
62	TPO.S.3.2	4.5.22	Trim PO (TPO) Layout Rules	Add the rule
63	TPO.EN.1.0.2	4.5.22	Trim PO (TPO) Layout Rules	Add the rule
64	TPO.EN.2.2	4.5.22	Trim PO (TPO) Layout Rules	Add the rule
65	TPO.R.2	4.5.22	Trim PO (TPO) Layout Rules	Modify the rule description
66	VT.W.1.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
67	VT.W.1.2.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
68	VT.W.2.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
69	VT.W.2.2.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
70	VT.S.1.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule

No.	Rule	Sec. No.	Section Title	V1.0_2 Revision Description
71	VT.S.1.2.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
72	VT.S.1.4.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
73	VT.S.2.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
74	VT.S.2.2.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
75	VT.S.2.4.1	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
76	VT.S.4.0.2	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
77	VT.S.5.0.2	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
78	VT.S.5.1.2	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
79	VT.S.6.3	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
80	VT.S.9.2	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
81	VT.EN.1.3	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
82	VT.EN.2.2	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
83	VT.EN.3.2	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
84	VT.EX.2.0.2	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
85	VT.EX.2.1.2	4.5.25	VT (VTS_N, VTS_P, VTL_N, VTL_P, VTUL_N, VTUL_P) Layout Rules [Optional]	Add the rule
86	PP.A.1.2	4.5.26	P+ Source/Drain Ion Implantation (PP) Layout Rules	Add the rule
87	PP.A.3.2	4.5.26	P+ Source/Drain Ion Implantation (PP) Layout Rules	Add the rule
88	MD.W.1.1	4.5.33	MD Layout Rules	Add the rule
89	MD.S.2	4.5.33	MD Layout Rules	Modify the rule description
90	MD.S.2.0.1	4.5.33	MD Layout Rules	Add the rule
91	MD.S.2.1	4.5.33	MD Layout Rules	Modify the rule description
92	MD.S.2.2	4.5.33	MD Layout Rules	Add the rule
93	MD.S.6.3	4.5.33	MD Layout Rules	Add the rule
94	MD.S.6.7	4.5.33	MD Layout Rules	Add the rule
95	MD.S.7.0.2	4.5.33	MD Layout Rules	Add the rule
96	MD.S.7.2.1	4.5.33	MD Layout Rules	Add the rule

No.	Rule	Sec. No.	Section Title	V1.0_2 Revision Description
97	MD.S.8.1.2	4.5.33	MD Layout Rules	Add the rule
98	MD.S.25	4.5.33	MD Layout Rules	Add the rule
99	MD.S.25.1®	4.5.33	MD Layout Rules	Add the rule
100	MD.S.26	4.5.33	MD Layout Rules	Add the rule
101	MD.S.26.1	4.5.33	MD Layout Rules	Add the rule
102	MD.EX.1.2	4.5.33	MD Layout Rules	Add the rule
103	MD.EX.7.1	4.5.33	MD Layout Rules	Add the rule
104	MD.R.13.2	4.5.33	MD Layout Rules	Add the rule
105	MD.R.15.2	4.5.33	MD Layout Rules	Add the rule
106	MD.R.25	4.5.33	MD Layout Rules	Modify the rule description
107	MD.R.25.1	4.5.33	MD Layout Rules	Modify the rule description
108	MD.G0.0	4.5.33	MD Layout Rules	Modify the rule description
109	CMD.S.2.1	4.5.34	Cut-MD (CMD) Layout Rules	Modify the rule description
110	CMD.S.2.2	4.5.34	Cut-MD (CMD) Layout Rules	Add the rule
111	CMD.S.3.3	4.5.34	Cut-MD (CMD) Layout Rules	Add the rule
112	CMD.S.4.5	4.5.34	Cut-MD (CMD) Layout Rules	Add the rule
113	CMD.S.4.6	4.5.34	Cut-MD (CMD) Layout Rules	Add the rule
114	CMD.EX.1.1	4.5.34	Cut-MD (CMD) Layout Rules	Modify the rule description
115	CMD.EX.1.2	4.5.34	Cut-MD (CMD) Layout Rules	Add the rule
116	CMD.L.1.1	4.5.34	Cut-MD (CMD) Layout Rules	Modify the rule description
117	CMD.L.1.1.2	4.5.34	Cut-MD (CMD) Layout Rules	Add the rule
118	CMD.R.9.2	4.5.34	Cut-MD (CMD) Layout Rules	Add the rule
119	VC.W.1.4	4.5.37	VC Layout Rules	Modify the rule description
120	VC.W.1.5	4.5.37	VC Layout Rules	Add the rule
121	VC.S.31.16.T	4.5.37	VC Layout Rules	Add the rule
122	VC.S.31.17.T	4.5.37	VC Layout Rules	Add the rule
123	VC.S.31.18.T	4.5.37	VC Layout Rules	Add the rule
124	VC.S.32.16.T	4.5.37	VC Layout Rules	Add the rule
125	VC.S.32.17.T	4.5.37	VC Layout Rules	Add the rule
126	VC.S.32.18.T	4.5.37	VC Layout Rules	Add the rule
127	VC.S.33.7.T	4.5.37	VC Layout Rules	Add the rule
128	VC.S.34.7.T	4.5.37	VC Layout Rules	Add the rule
129	VC.S.35.7.T	4.5.37	VC Layout Rules	Add the rule
130	VC.S.39.1.T	4.5.37	VC Layout Rules	Add the rule
131	VC.S.39.2.T	4.5.37	VC Layout Rules	Add the rule
132	VC.S.39.3.T	4.5.37	VC Layout Rules	Add the rule
133	VC.S.39.4.T	4.5.37	VC Layout Rules	Add the rule
134	VC.S.39.5.T	4.5.37	VC Layout Rules	Add the rule
135	VC.S.39.6.T	4.5.37	VC Layout Rules	Add the rule
136	VC.S.39.9.T	4.5.37	VC Layout Rules	Add the rule
137	VC.S.39.12.T	4.5.37	VC Layout Rules	Add the rule
138	VC.S.39.15.T	4.5.37	VC Layout Rules	Add the rule
139	VC.S.39.16.T	4.5.37	VC Layout Rules	Add the rule
140	VC.S.39.17.T	4.5.37	VC Layout Rules	Add the rule

No.	Rule	Sec. No.	Section Title	V1.0_2 Revision Description
141	VC.S.39.18.T	4.5.37	VC Layout Rules	Add the rule
142	VC.EN.0	4.5.37	VC Layout Rules	Modify the rule description
143	VC.EN.2.1	4.5.37	VC Layout Rules	Add the rule
144	VC.L.4	4.5.37	VC Layout Rules	Add the rule
145	VC.R.9.3.1	4.5.37	VC Layout Rules	Add the rule
146	VC.R.9.7	4.5.37	VC Layout Rules	Add the rule
147	VC.R.18	4.5.37	VC Layout Rules	Modify the rule description
148	M0.W.1.1.3	4.5.39	M0 Layout Rules	Add the rule
149	M0.EN.0	4.5.39	M0 Layout Rules	Modify the rule description
150	M0.EN.5.1	4.5.39	M0 Layout Rules	Add the rule
151	M0.EN.5.2	4.5.39	M0 Layout Rules	Add the rule
152	M0.EN.5.3	4.5.39	M0 Layout Rules	Add the rule
153	DMn.R.7	6.2	Dummy Metal (DM) Rules	Modify the rule description
154	LUP.6.3	9.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Add the rule