

# Impact of CMOS Technology Scaling on SRAM Standby Leakage Reduction techniques

Olivier Thomas<sup>1</sup>, Marc Belleville<sup>1</sup>, François Jacquet<sup>2</sup>, Philippe Flatresse<sup>2</sup>

<sup>1</sup> CEA-LETI, 17, rue des Martyrs, F38054 Grenoble Cedex, France, first.name @cea.fr

<sup>2</sup> STMicroelectronics, 850, rue Jean Monnet, F38921 Crolles Cedex, France, first.name @st.com

**Abstract –** This paper investigates leakage reduction techniques for a conventional 6T SRAM cell in advanced technologies. The most promising leakage reduction techniques that have been proposed are presented and compared for the 130-nm and 65-nm technology nodes. More specifically, the impact of the evolution of the gate tunneling and substrate currents is studied considering the efficiency of those techniques. Finally, the best techniques for leakage reduction in sub 100-nm SRAM cell, and guidelines on how to merge them in order to reach an optimum, are proposed.

## I. Introduction

As the technologies scale down into the nanometer range transistor leakage currents become a major concern. To overcome this problem, advanced control methods become mandatory, especially for low activity circuits such as memory.

Different techniques have been proposed to target leakage control in conventional 6T SRAM cell. Two main approaches exist: a process one, using dual  $V_T$  [1] [2] or a design one, controlling the cell node voltages [3] [4].

采用多國值电压的MOS管或者控制节点电压  
This paper discusses the efficiency of the most promising design techniques for SRAM leakage reduction, in 130-nm and 65-nm technologies. In 65-nm, gate tunneling currents [5] become close to, and can even surpass, sub-threshold and DIBL (Drain Induced Barrier Lowering) currents, while those last ones still dominate the total standby leakage current in 130-nm. Also substrate currents (GIDL: Gate Induced Drain Leakage, JBTBT: Junction Band to Band Tunneling) [6] become less and less negligible.

The gate tunneling and substrate currents impact drastically the efficiency of the SRAM cell leakage reduction techniques. The purpose of this work is to compare all those techniques, and to propose guidelines for sub 100-nm technologies.

The paper is organized as follows. Section II provides an overview of the leakage current contributions in a conventional 6T SRAM cell and compares their distribution in 130-nm and 65-nm. Section III presents the design leakage reduction techniques considered in this work. Section IV details our simulated results and then evaluates the efficiency of each technique versus the gate and substrate currents. Finally, concluding remarks are presented in the last Section.

## II. Leakage in a conventional 6T SRAM cell

For sub 100-nm technologies, gate, sub-threshold and GIDL currents are the dominant leakage mechanisms. Figure 1 illustrates these three contributions in a conventional 6T SRAM cell. In a normal retention mode, the word-line (WL) is connected to ground and the bit-lines ( $BL_{T/F}$ ) are held to VDD. In this example a high logic level ( $T='H'$ ,  $F='L'$ ) is stored. Transistors  $M_{DT}$ ,  $M_{LF}$ ,  $M_{AT}$  and  $M_{AF}$  are in off-state and  $M_{DF}$  and  $M_{LT}$  are in on-state. Sub-threshold current ( $I_{STH}$ ) originates in off-state transistors whose  $V_{DS}$  is VDD ( $M_{DT}$ ,  $M_{LF}$  and  $M_{AF}$ ). Gate current ( $I_G$ ) concerns all the transistor of the cell. Yet, its magnitude is a function of the applied bias (off-state transistor  $\rightarrow I_{GOFF}$ , on-state transistor  $\rightarrow I_{GON}$ ). GIDL current ( $I_{GIDL}$ ) affects all the off-state transistors due to the high electric field in the gate/drain overlap. The access transistor  $M_{AT}$  is also impacted by  $I_{GISL}$  current (Gate Induced Source Leakage) whose  $V_{SG}$  is VDD. Note that PMOS gate current are roughly 10 times smaller than NMOS gate current. Consequently,  $I_{GOFF}$  in  $M_{LF}$  has a low contribution.

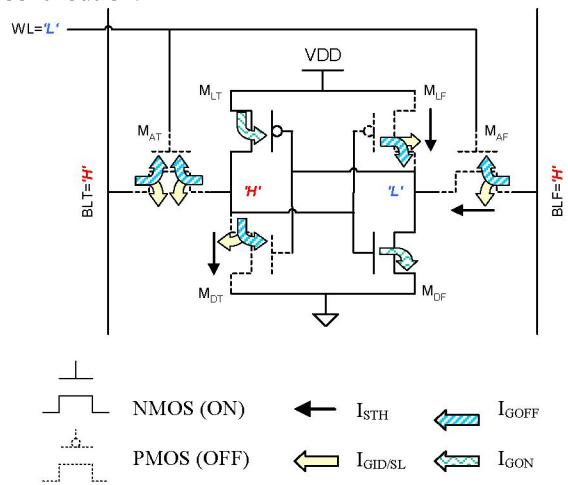


Figure 1, Leakage current contributions

The three leakage contributions ( $I_{STH}$ ,  $I_G$ ,  $I_{GIDL/SL}$ ) lead to three dominant leakage paths in a sub 100-nm cell (Figure 2): (i) the leakage from VDD to ground across the cell inverters, (ii) the leakage from the bit-lines ( $BL_{T/F}$ ) to ground and (iii) the leakage from  $BL_{T/F}$  to the word line (WL). This third leak path which did not affect memory cells for the nodes larger than 100-nm

will modify the strategies regarding leakage reduction techniques in the advanced technologies.

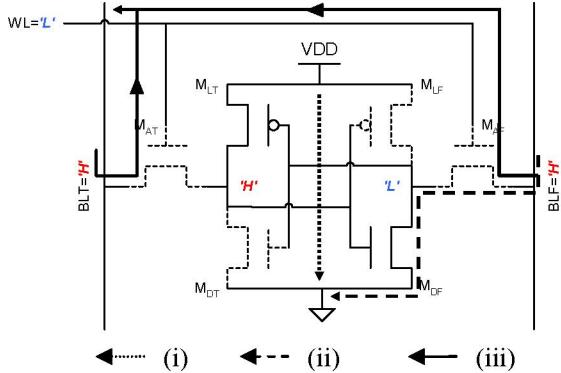


Figure 2, Dominant leakage paths

Figure 3 and Figure 4 presents the leakage distribution of two 6T SRAM cells characterized by a channel length of 130-nm (Cell1) and 65-nm (Cell2), respectively. The simulations have been done for a typical process, where  $T=27^\circ\text{C}$ ,  $VDD_{130\text{-nm}}=1.2\text{V}$  and  $VDD_{65\text{-nm}}=1\text{V}$ .

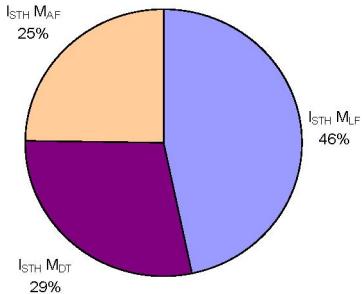


Figure 3, Cell1 (130-nm) leakage distribution

In Cell1,  $I_G$  and  $I_{GIDL}$  are negligible compared to  $I_{STH}$ . The main leak path comes trough VDD to ground across the two cell inverters ( $I_{STH} M_{DF}$  and  $I_{STH} M_{LT}$ ). The leakage through BL to ground ( $I_{STH} M_{AF}$ ) represents 25% of the total standby consumption.

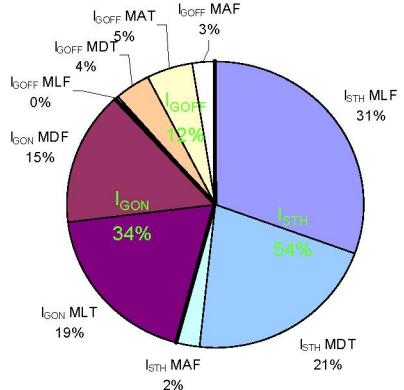


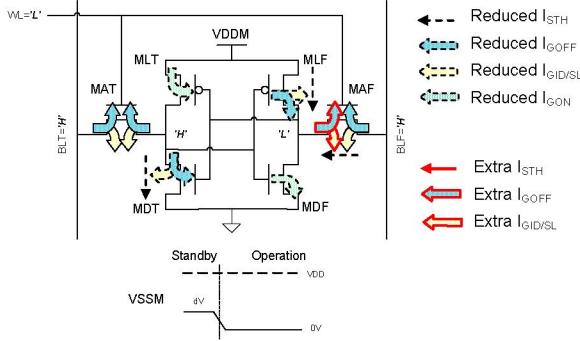
Figure 4, Cell2 (65-nm) leakage distribution

In Cell2,  $I_G$  and  $I_{GIDL}$  impact nearly 50% of the total leakage current. Compared with  $I_{GOFF}$  and  $I_{GON}$ , GID/SL currents are still relatively low (<1%).  $I_{GOFF}$  flowing through the PMOS load transistor  $M_{AF}$  is also negligible. Over-all,  $I_{GOFF}$  through access and drive transistors represents more than 25% of  $I_G$ . The two-thirds of  $I_{GOFF}$  come from the access transistors ( $M_{AT/F}$ ). The balance of the leakage distribution shows that path (i) initiates 90% of the total standby current, whereas path (ii) and (iii) drive 2% and 5%, respectively. Compared with Cell1, the BL leakage is shared between path (ii) and (iii) in Cell2. Furthermore in this example, the leak trough path (iii) is higher than the one through path (ii). The efficiency of the leakage reduction techniques presented in the next section will be strongly affected by the impact of scaling on gate and substrate currents.

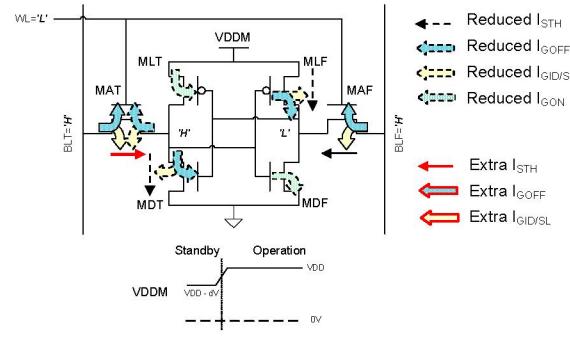
### III. SRAM cell design leakage reduction techniques

Leakage contributions are directly related to the electric fields inside the device. Reducing node voltages drastically decreases leakage power. SRAM cell design leakage reduction techniques consist in controlling the cell nodes voltage. The nodes of a 6T SRAM cell are: WL, BL<sub>TF</sub>, VDD, VSS, VPWELL and VNWELL.

The first two techniques consist in upper VSS node (UVSS) [7] and lower VDD node (LVDD) [8] in retention mode. During normal operation a full supply voltage is applied. Figure 5 and Figure 6 show the impact of UVSS and LVDD approaches on leakage components through different transistors. The increase of VSS induces the rising of storage node F (=L'). While the decrease of VDD leads to the reduction of storage node T (=H'). Regarding the cross-coupled inverters transistors, this results in lower voltages for firstly  $V_{GS}$  of transistors  $M_{DF}$  and  $M_{LT}$ , secondly  $V_{GD}$  of transistors  $M_{DT}$  and  $M_{LF}$ , and finally  $V_{DS}$  of transistors  $M_{DT}$  and  $M_{LF}$ . The electric field reduction related to  $V_{GS}$ ,  $V_{GD}$  and  $V_{DS}$  induces the reduction of gate, GIDL and sub-threshold currents flowing through the cross-coupled inverters transistors. Moreover, for UVSS,  $M_{DT}$  is reverse source biased whereas for LVDD it is  $M_{LF}$ . This results in an extra  $I_{STH}$  reduction of these transistors. Concerning the access transistors, the increase of storage node voltage F, related to the UVSS technique, diminishes  $V_{DS}$  of transistor  $M_{AF}$ . Thereby, there is no improvement of  $I_G$  and  $I_{GIDL}$ , only the  $I_{STH}$  of  $M_{AF}$  is reduced. Furthermore, there are some extra gate and GISL currents from  $M_{AF}$ . Concerning the lower voltage of storage node T, related to LVDD technique,  $V_{SG}$  of transistor  $M_{AT}$  decreases, leading to a reduction of  $I_{GIDL}$  and  $I_G$ . On the other hand,  $V_{DS}$  of transistor  $M_{AT}$  increases ending to an extra sub-threshold current. Besides, there is no improvement of leakage current of transistor  $M_{AF}$ .



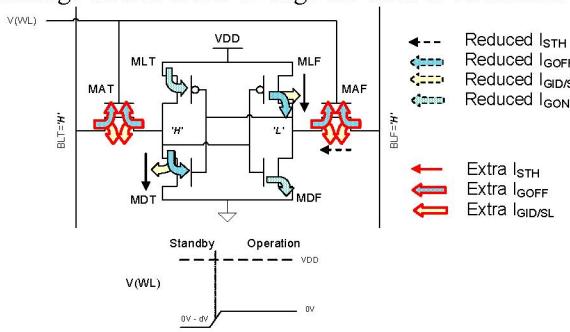
**Figure 5**, Leakage current in 6T SRAM cell including UVSS approach



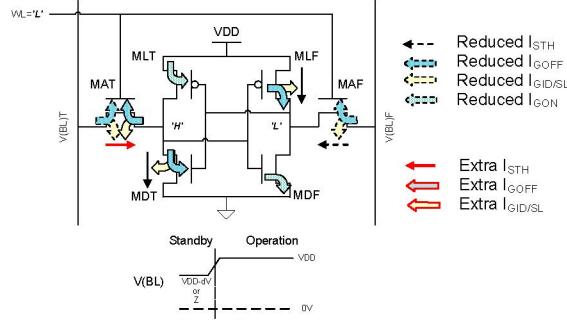
**Figure 6**, Leakage current in 6T SRAM cell including LVDD approach

To summarize, while the leakage components flowing through the cell inverters are reduced, UVSS and LVDD approaches are partially successful in reducing leakage current of access transistors. Moreover, UVSS induces extra gate and GISL currents and LVDD an extra sub-threshold current in access transistors.

The goal of the third and fourth techniques is to reduce the leakage current of the access transistors. The third one consists in lowering the WL below 0V in retention mode (NWL), while WL switches from 0V to VDD in active mode. The fourth one consists in letting the bit-lines float in retention mode (FBL), while they are pre-charged to VDD in active mode. Figure 7 and Figure 8 show the impact of NWL and FBL approaches on leakage contributions through the various transistors.



**Figure 7**, Leakage current in 6T SRAM cell using NWL approach

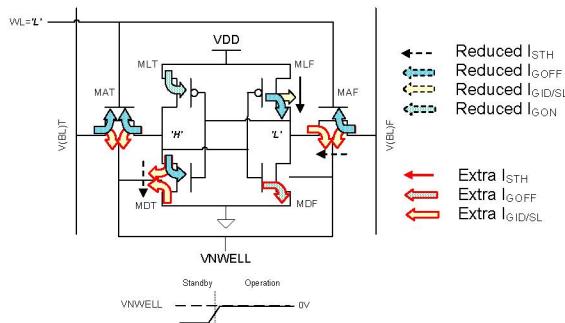


**Figure 8**, Leakage current in 6T SRAM cell using FBL approach

In both techniques, there is no improvement of the leakage current of the cross-coupled transistors. NWL approach results in a negative  $V_{GS}$  polarization of transistor  $M_{AF}$ , decreasing  $I_{STH}$ . The drawbacks are the increase of  $V_{GD}$  of transistor  $M_{AF}$  and of  $V_{GS}$  and  $V_{GD}$  of transistor  $M_{AT}$  leading to some extra  $I_G$  and  $I_{GID/SL}$ . FBL approach results in the reduction of  $V_{DS}$  of transistor  $M_{AF}$ , and of  $V_{GD}$  of transistors  $M_{AT}$  and  $M_{AF}$ . Reduction voltages of  $V_{DS}$  and  $V_{GD}$  leads to diminish  $I_{STH}$ ,  $I_G$  and  $I_{GIDL}$  of the concerned access transistors. The drawback of this technique is the increase of  $V_{DS}$  of transistor  $MAT$  leading to an extra  $I_{STH}$ .

To summarize, NWL and FBL approaches have no effect on leakage contributions of the cross-coupled inverters transistors and are partially successful in reducing the leakage current of the access transistors. In sub 100-nm, NWL approach is seriously limited by gate and GID/SL currents.

Reverse body biasing (RBB) NMOS (VNWELL) or PMOS (VPWELL) devices reduces sub-threshold leakage via body effect. In active mode a zero-body bias is applied. Figure 9 illustrates the impact of RBB approach, applied on NMOS transistors, on the leakage contributions. RBB becomes less and less effective in nanoscale dimensions due to excessive reverse junction leakage (JBTBT) and drain/source-body junction breakdown during burn in [9].



**Figure 9**, Leakage current in 6T SRAM cell using RBB approach for NMOS transistors

#### IV. Simulation results

The leakage reduction techniques must not have a noticeable impact on SRAM cell stability or Soft Error Rate (SER). The cell stability is characterized in read mode by the static-noise margin (SNM) [10]. The sensitivity to SER is characterized by a critical charge ( $Q_{crit}$ ) [11]. To evaluate properly the efficiency of each of the leakage reduction techniques, the criteria to take into account are: the standby power consumption ( $I_{OFF}$ ), the leakage through the access transistors ( $I_{OFF-MA}$ ), the retention noise margin (RNM) and the critical charge ( $Q_{crit}$ ). RNM is similar to SNM, but in that case the access transistors are turned off. The RNM must not be lower than the SNM. Table 1 and Table 2 present the normalized results obtained for each of the reduction techniques for 130-nm and 65-nm nodes, respectively.

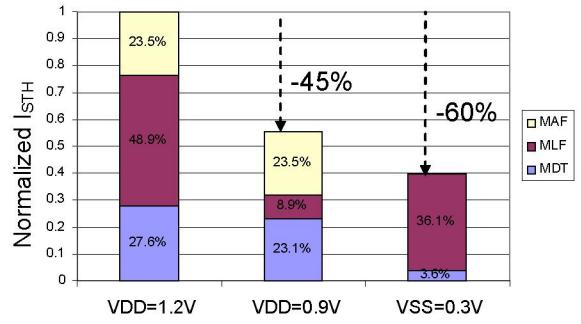
Cell	RNM	$Q_{crit}$	$I_{OFF-MA}$	$I_{OFF}$
Conv. 6T VDD=1.2V	1	1	1	1
LVDD VDD=0.9V	0.82	0.76	1	0.55
UVSS VSS=0.3V	0.82	0.76	<u>0.06</u>	<u>0.40</u>
FBL	1	1	0.64	0.99
NWL VWL=-0.3V	1	1	<u>0.06</u>	0.77
RBB $V_{NWELL}=-0.3V$	1	1	0.14	0.57

**Table 1,** Evaluation of the leakage reduction techniques in 130-nm

Cell	RNM	$Q_{crit}$	$I_{OFF-MA}$	$I_{OFF}$
Conv. 6T VDD=1.0V	1	1	1	1
LVDD VDD=0.7V	0.72	0.67	0.52	0.46
UVSS VSS=0.3V	0.72	0.67	1	<u>0.38</u>
FBL	1	1	<u>0.14</u>	0.92
NWL VWL=-0.3V	1	1	<u>1.31</u>	<u>1.08</u>
RBB $V_{NWELL}=-0.3V$	1	1	<u>1.47</u>	0.98

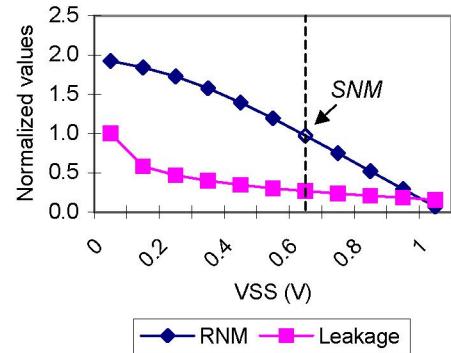
**Table 2,** Evaluation of the leakage reduction techniques in 65-nm

In 130-nm channel length, UVSS leads to the best leakage reduction (Table 1) thanks to the reduction of  $I_{STH}$  of  $M_{AF}$  transistor, as depicted in Figure 10. About the stability of the cell, RNM and  $Q_{crit}$  are both degraded. However in this example, with a modulation of 300-mV of VDD or VSS, the RNM is still 50% higher than the SNM.



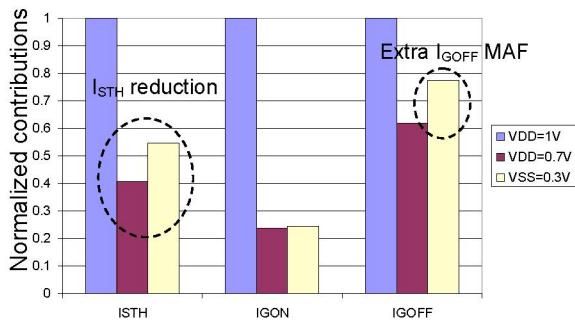
**Figure 10,** Normalized sub-threshold current in 130-nm SRAM cell

Figure 11 shows the variation of the RNM and standby leakage versus VSS. The RNM results have been normalized to the SNM, while the leakage values have been normalized to the leakage value for a full supply voltage. As shown in Figure 11, the VSS node voltage can be up to 600-mV. Then the leakage saving is more than 70%. It can be notified that the leakage decreases exponentially with the increase of VSS. Above 400-mV the leakage saving increase smoothly. Thus, regarding the cell stability, it is not helpful to increase VSS above 400-mV.



**Figure 11,** RNM and leakage versus VSS, in 130-nm

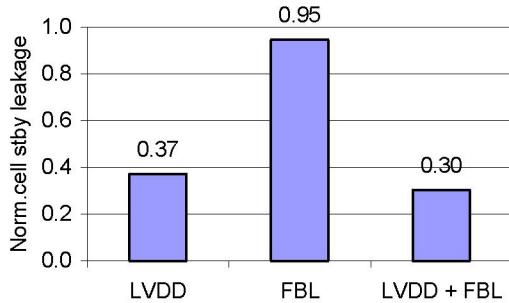
For 65-nm channel length, LVDD leads to the best leakage reduction followed by the UVSS approach (Table 2). Two reasons explain why LVDD is less leaky than UVSS. First, the PMOS ( $M_{LF}$ ) sub-threshold leakage reduction is more important than the NMOS ( $M_{DT}$ ) one (strongly technology dependent). Secondly,  $I_G$  and  $I_{STH}$  are equivalent for a supply voltage of 700-mV. Therefore, the leakage through path (ii) ( $BL_{T/F}$  to ground via  $I_{STH}$  of  $M_{AF}$  transistor) is equal to the leakage through path (iii) ( $BL_{T/F}$  to WL via  $I_G$  of  $M_{AF}$  transistor) (cf. Figure 4). Consequently, the  $I_{STH}$  of  $M_{AF}$  saving is compensated by the extra  $I_G$  of  $M_{AF}$  induced in UVSS approach. To illustrate this, the sub-threshold and gate currents for the latter approaches are compared in Figure 12.



**Figure 12**, Normalized sub-threshold and gate currents in 65-nm SRAM cell

Regarding NWL and RBB approaches, both are discredited by the gate current in 65-nm.

Overall, in sub 100-nm technologies, leakage reduction techniques should target gate current as well as sub-threshold current. The best leakage reduction method is balanced between UVSS and LVDD, depending on the electrical characteristics of the inverters transistors. While the leakage components flowing through the cell inverters are reduced, UVSS and LVDD are only partially successful in reducing leakage current of access transistors. FBL is the most efficient to reduce leakage through BL and can be used as a complementary technique. Accordingly, merging UVSS and/or LVDD and FBL approaches appears to be the best method to solve standby leakage currents in sub 100-nm SRAM cell. However, merging LVDD and FBL is more advantageous than merging UVSS and FBL. The reason is that, with LVDD, the extra  $I_{STH}$  of  $M_{AT}$  transistor due to the increase of  $V_{DS}$  voltage is diminished by letting the bit-lines float. In fact, BLT and BLF reach a steady state determined by the leakage balance between  $M_{AT}$  and  $M_{AF}$ . Figure 13 gives the cell standby leakages of the independent and merged methods. An extra 7% leakage saving is obtained.



**Figure 13**, Normalized 65-nm cell standby leakage versus LVDD and FBL approaches

Below 65-nm, GID/SL current becomes close to and can surpass  $I_G$  [12]. In this case, leakage through BL will be shared between the ground, the word-line and the substrate of the access transistors. Hence GID/SL current will have the same impact on leakage reduction

techniques than  $I_G$ . So the previous conclusions will remain true.

## V. Conclusion

To overcome the leakage problem in sub 100-nm technologies, advanced leakage control methods must take into account the gate and GID/SL currents as well as the sub-threshold currents. As long as  $I_G$  and GIDL currents were negligible, UVSS was the best technique to reduce static consumption thanks to a good impact on  $I_{STH}$  of the access transistors. Below 65-nm,  $I_G$  and GID/SL become as important as  $I_{STH}$ . The leakage through bit-lines is shared between the ground and the word-line. Thus,  $I_{STH}$  saving is compensated by some extra  $I_G$  and  $I_{GIDL}$  induced by the UVSS approach. Besides, the increase of  $I_G$  and  $I_{GIDL}$  discredits NWL and RBB methods. This work conclusion is that the best technique for SRAM cell leakage reduction would be to merge LVDD and FBL approaches.

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