

# Wojciech Kudla

PROGRAMMER · LOW-LATENCY ENGINEERING EXPERT

95 Hawthorne Crescent, SE10 9GA London, United Kingdom

☎ (+44) 7895833903 | ✉ wojciech.kudla@gmail.com | 🏠 bitcharmer.blogspot.co.uk | 📷 bitcharmer | 🐦 @bitcharmer

## Education

### Oskar Lange University of Economics

Wrocław, Poland

MARKETING AND MANAGEMENT

2000 - 2005

- AIESEC Public Relations coordinator, Local committee member

## Skills

**Programming** Java, C, Rust, Golang, Python, Bash

**Linux** Kernel hacking, eBPF, Tracing and performance analysis, IO Offloading, Tuning for high performance

**Design and Architecture** High performance distributed systems, Application resiliency, Event sourcing

**Languages** English, Polish

## Experience

### HSBC

London, UK

SENIOR LOW LATENCY ENGINEER

Feb. 2020 - now

- Delivering high-performance components of application infrastructure (data structures, parsers, shims, etc).
- Tuning software execution stack (HW, OS, JVM) for soft-realtime requirements.
- Leading yearly hardware refresh initiative (working with HW manufacturers, PoC evaluation).
- Designing and implementing tools for extracting and visualizing detailed metrics from the HW, kernel and the JVM.
- Evaluation and research into compiler control, GraalVM, techniques for keeping icache hot, data prefetching, etc.
- Code reviews for performance-critical software components, performance troubleshooting in production.
- Kernel driver- and OpenJDK hacking, replaced JDK's NIO subsystem with more capable and performant native equivalent
- Delivered PCAP replay for all production UDP streams and revolutionized approach to benchmarking application performance in UAT.

### Morgan Stanley

London, UK

HIGH PERFORMANCE SYSTEMS SPECIALIST

Oct. 2018 - Jan. 2020

- Advanced research into high performance systems innovation (PCIe-CPU core affinity, sub- numa, AVX thermals, Intel's CAT).
- Built high resolution event timing solution for realtime latency capture.
- Customizing HW-, OS- and JVM-level configuration to reduce latency and tame platform jitter.
- Implementing high performance native components for latency-sensitive Java code.
- Guiding and mentoring different teams and groups within Institutional Securities Division to help them achieve their performance goals.
- Resolving ongoing performance issues, driving latency-oriented capacity planning and resource partitioning.

### Goldman Sachs

London, UK

EXECUTIVE DIRECTOR

May 2017 - Oct. 2018

- Delivered continuous metrics collection for all layers of software execution stack (built with OSS).
- Implemented perf and raw hardware event counter API for Java to precisely track code execution dynamics.
- Optimized Java code and managed runtime configuration to reduce memory access latency.
- Reduced deoptimization penalty in uncommon code paths with compiler control.
- Tuning hw- and os-level configuration for low latency (bios, openonload, sysctl, irq/workqueue affinity mask, tickless kernel).
- Implemented access to hardware RX timestamps from Java code.

### HSBC

London, UK

LOW LATENCY SOFTWARE SPECIALIST

Apr. 2016 - May 2017

- Delivered infrastructure and software monitoring platform offering insight into metrics for all layers of the technology stack: HW, OS, JVM, apps (InfluxDB, Telegraf, Grafana, Python).
- Implemented and integrated performance-sensitive core components across eFX space (high-resolution event timing, zero-allocation ultra-low latency FIX processor, branch-less numeric parsers, delta compression codecs).
- Evaluating low-latency integrated market access products.
- Performance troubleshooting across the whole estate (ftrace, perf, lttng, Java Mission Control, etc.).
- Tuning environments for low-latency applications (SolarFlare + OpenOnload, tickless kernels, IRQ balancing, optimal component layout vs NUMA topology).

## Nomura International Plc

London, UK

LOW LATENCY JAVA DEVELOPER

Aug. 2013 - Apr. 2016

- Driving HFT innovation by leveraging mechanical sympathy and JVM expertise. Delivering high performance core components within ultra low-latency environment.
- Developed ultra low-overhead latency monitoring with near-realtime reporting.
- Designed and implemented gc-less and lock-free data structures (bytebuffer ring, Java off-heap flyweight objects).
- Developed low overhead latency monitoring with near-realtime reporting.
- Tuned and optimized kernel- and hw-level aspects of production environments in co-location sites.

## Clear2Pay

Warsaw, Poland

JAVA DEVELOPER

Oct. 2012 - Aug. 2013

- Automating payment processing smoke tests (Websphere 7, Jersey REST, Junit, JMS).
- Developing processing logic for Credit Transfer and Direct Debit for Royal Bank of Scotland.

## UBS Investment Bank

Zurich, Switzerland

LOW LATENCY DEVELOPER

Mar. 2012 - Oct. 2012

- Optimizations in the area of low latency communications, applying HPC techniques to implement high frequency trading standards (message processing within microsecond range).
- Developed zero-gc low latency market data and trading gateways based on FIX and/or proprietary protocols.
- Troubleshooting and GC-tuning UBS production environments.

## PriceWaterhouseCoopers (former Outbox)

Warsaw, Poland

MANAGING CONSULTANT

Sep. 2011 - Mar. 2012

- Performance troubleshooting in a whole range of enterprise Java systems from Outbox portfolio (telco industry).
- CPU and memory profiling and optimizations as well as code auditing and general design and implementation level advisory.

## LMAX

London, UK

SENIOR JAVA DEVELOPER

May 2011 - Sep. 2011

- Developing realtime FX trading platform with non-blocking algorithms and data structures.
- Building automated performance scoring solution used in CI
- Researching optimizations for LMAX disruptor.

## PriceWaterhouseCoopers (former Outbox)

Warsaw, Poland

MANAGING CONSULTANT

Jun. 2007 - May 2011

- Key Account Manager - handling day-to-day business relations, team management, procuring RFIs and RFPs, project planning, resolving delivery issues, etc.
- Principal developer for a large portfolio of telco projects across a whole range of clients from France Telecom Group.
- Hands-on approach with contributions to a broad spectrum of systems ranging from Intelligent Network to customer verification to order validation and completion (Jboss, Drools, Hibernate, Spring, WS, SOA).

## Asseco (former ABG)

Warsaw, Poland

LEAD DEVELOPER

Jun. 2007 - May 2011

- System analyst (state and activity flows and process definitions, use cases); implemented automated process definition generation from UML diagrams.
- Senior developer/team leader. Managing a team of 12 engineers, developing core components and business functionality in n-tier system, code reviews (Enterprise Architect, Weblogic, Hibernate)
- Core Team member.

## Extracurricular Activity

---

- Contributing to Linux kernel, OpenJDK and other OSS projects
- Blogging: [bitcharmer.blogspot.co.uk](http://bitcharmer.blogspot.co.uk).
- Sports: Archery GB member.