Design of CMOS LNA with active inductor in 28 nm technology

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***Abstract*—This paper presents a low powered Low Noise Amplifier (LNA) with active inductor instead of passive inductor which can save the size of the chip at a great extent. The LNA is designed in 28nm technology for 2.6 GHz frequency range. The LNA presented here offers a good noise performance. The proposed LNA is simulated in synopsis design tool in 28nm technology.**

Keywords—CMOS, LNA, 28nm, active inductor.

I.Introduction

With the continuous improvement in wireless communication technology and the enormous advancement in the performance of MOSFETs [1] it has enabled the Radio Frequency (RF) applications, the need for highly integrated RF circuits with low noise, high gain and low power dissipation is increasing. One of the crucial block in RF IC is generally made up of Low Noise Amplifier (LNA). It amplifies the received signal with less noise. The LNA is key component in RF industries due to its gain and low noise characteristics and is firmly related to the system sensitivity and dynamic range.One of the main drawbacks in passive inductor is that the component is off-chip, discrete part which restrict the bandwidth. They are even difficult to fabricate the spiral inductor inside the silicon mass. The proposed design uses an active inductor on silicon chip using CMOS technology resulting in improved performance and lower manufacturing costs significantly. The current reuse method can produce the best combination of high power gain, and low noise figure (NF) making it a suitable for use in Ultra Wide Band(UWB) region[2].LNA *w*ith feed forward method the linearity of LNA can be improved very easily.

II.Reference Circuit details

The current reuse technique is used to design LNA with an aim to reduce the chip area for that an active inductor is used in the gate inductance. In LNA the gate inductance is always higher ~7nH which consumes large area, to overcome the issue an active inductor has been placed which consumes relatively lower area. In fig1 C_1 and C_2 are DC block capacitors, L_1 and L_2 are source and drain inductors and the inductor Lm is used to increase the impedance between M1 and M2.

Active Inductor- In fig2 M4 and M5 are current mirror transistors they inverse the conductance value of M3 which is in positive transconductance region and M1 is in negative transconductance region. The three transistors M6,M7,and M8 are used for biasing purpose. And the current Ibias is used for biasing.[3]

III. Reference Circuit

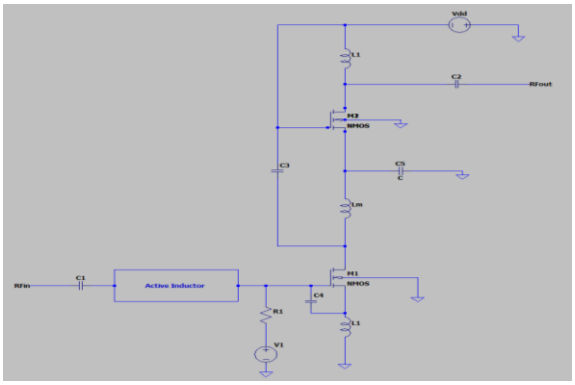

Fig 1: Circuit Diagram of proposed LNA with active inductor.

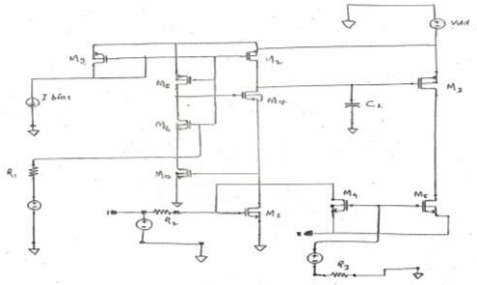
Fig 2:Circuit Diagram of active inductor

IV.Reference Waveforms

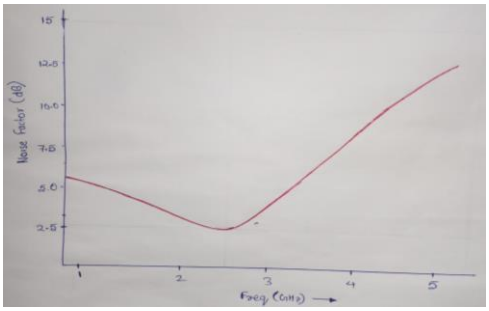

Fig4: Reference Noise Figure at the Output 180nm tech.

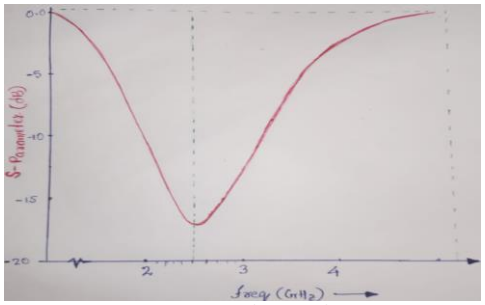

Fig: Scattering Parameter of LNA of S_{11} 180nm tech.

V.References

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