8-BIT EPROM FAMILY

(Am2764A, Am27128A, Am27256, Am27512)

DISTINCTIVE CHARACTERISTICS

- Fast access times — as low as 150 ns
- Low-power dissipation
- Programming voltage — 12.5 V
- Single +5-V power supply
- TTL-compatible inputs and outputs
- ±10% power-supply tolerance available

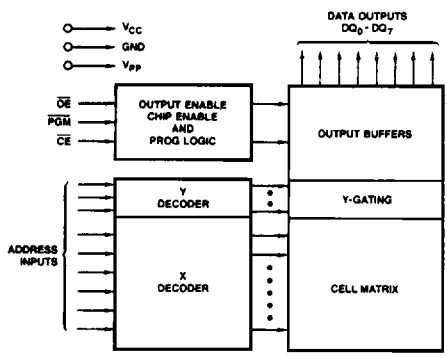
GENERAL DESCRIPTION

The Am2764A, Am27128A, Am27256, and the Am27512 are ultraviolet Erasable Programmable Read-Only Memories (EPROMs) and are organized as 8 bits per word. All standard EPROMs offer access times of 250 ns, allowing operation with high-speed microprocessors without any Wait states. Some of AMD's EPROMs have access times of as fast as 150 ns.

To eliminate bus contention on a multiple-bus microprocessor system, all AMD EPROMs offer separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. To reduce programming time, AMD's EPROMs may be programmed using 1-ms pulses.

BLOCK DIAGRAM



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PRODUCT SELECTOR GUIDE

Family Part No.	Am2764A, Am27128A, Am27256, Am27512					
Ordering Part No.:						
±5% V_{CC} Tolerance	2764A-1 27128A-1 — —	— — 27256-1 —	2764A-2 27128A-2 27256-2 —	2764A 27128A 27256 27512	2764A-3 27128A-3 27256-3 27512-3	2764A-4 27128A-4 27256-4 27512-4
±10% V_{CC} Tolerance	2764A-15 27128A-15 — —	— — 27256-17 —	2764A-20 27128A-20 27256-20 —	2764A-25 27128A-25 27256-25 27512-25	2764A-30 27128A-30 27256-30 27512-30	2764A-45 27128A-45 27256-45 27512-45
t_{ACC} (ns)	150	170	200	250	300	450
t_{CE} (ns)	150	170	200	250	300	450
t_{OE} (ns)	75	75	75	100	110	150

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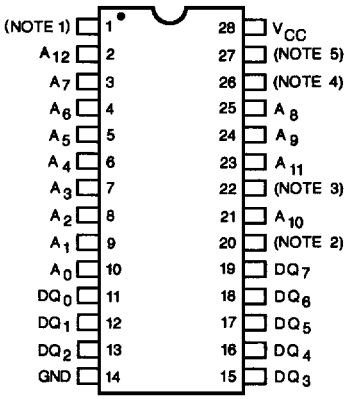
CONNECTION DIAGRAMS
Top View



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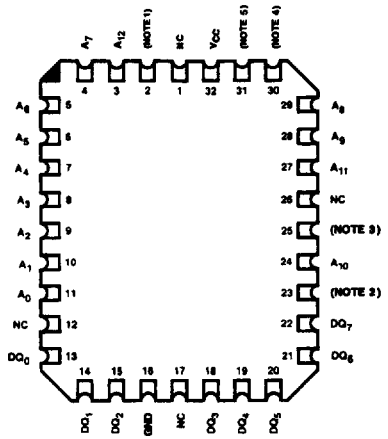

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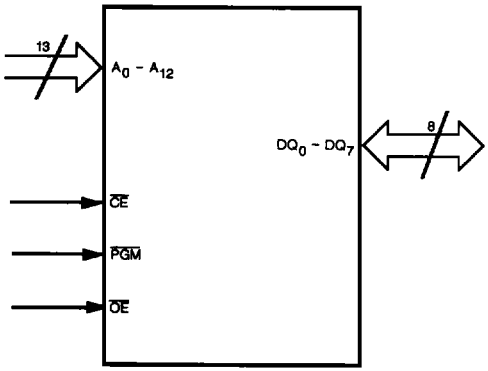
Notes:

	AM2764A	AM27128A	AM27256	AM27512
1	V_{PP}	V_{PP}	V_{PP}	A_{15}
2	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
3	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
4	NC	A_{13}	A_{13}	A_{13}
5	$\overline{PGM}$	$\overline{PGM}$	A_{14}	A_{14}

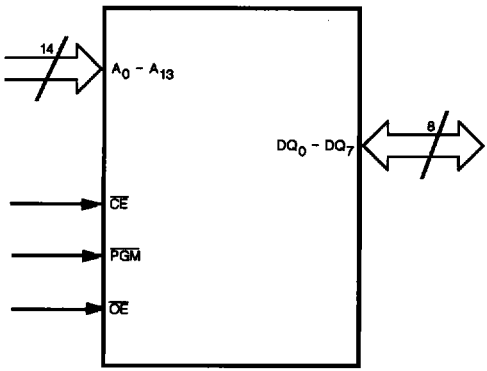
LOGIC SYMBOL

Am2764A



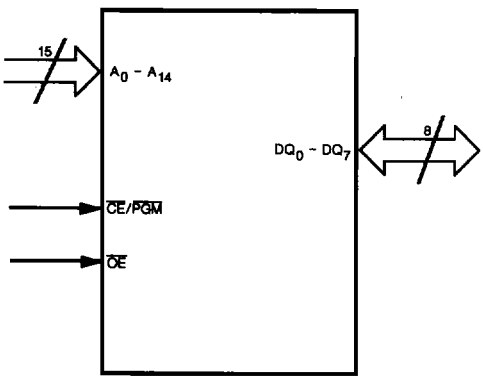
LS002360

Am27128A



LS002370

Am27256



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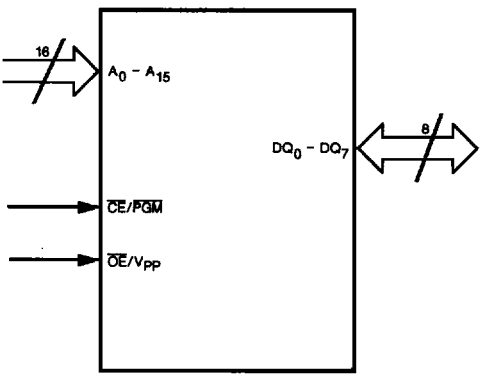
Am27512



LS002530

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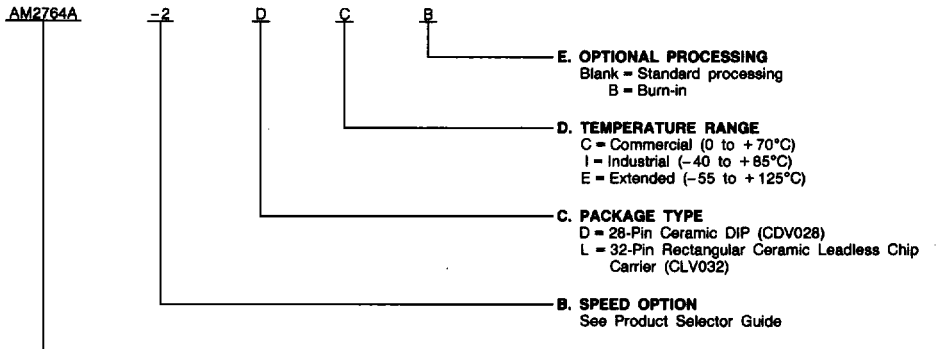
ORDERING INFORMATION (Cont'd.)
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations

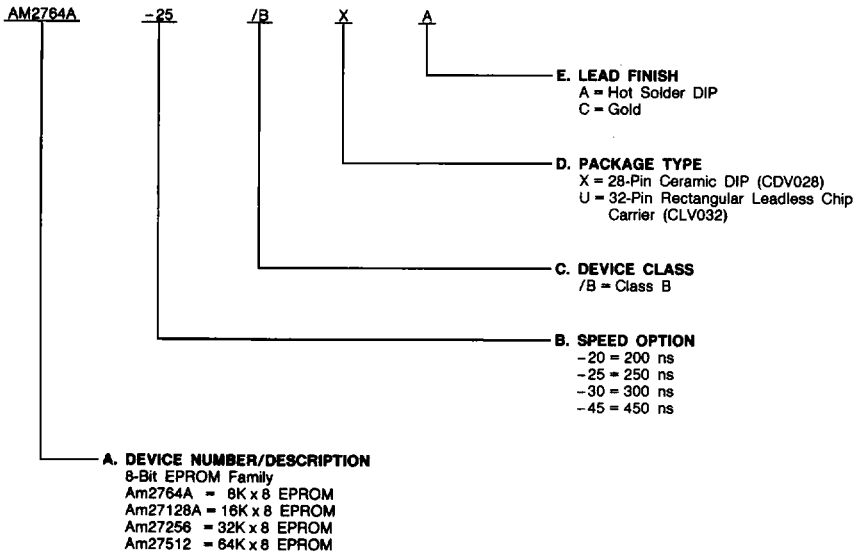
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
±5% V_{CC} Tolerance	
AM2764A-1	DC, DCB, DI, DIB, LC, LCB, LE, LEB
AM2764A-2	
AM2764A	
AM2764A-3	
AM2764A-4	
AM27128A-1	
AM27128A-2	
AM27128A	
AM27128A-3	
AM27128A-4	
AM27256-1	
AM27256-2	
AM27256	
AM27256-3	
AM27256-4	
AM27512	
AM27512-3	
AM27512-4	
±10% V_{CC} Tolerance	
AM2764A-15	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB, LE, LEB
AM2764A-20	
AM2764A-25	
AM2764A-30	
AM2764A-45	
AM27128A-15	
AM27128A-20	
AM27128A-25	
AM27128A-30	
AM27128A-45	
AM27256-17	
AM27256-20	
AM27256-25	
AM27256-30	
AM27256-45	
AM27512-25	DC, DCB, DI, DIB, DE, DEB, LC, LCB, LI, LIB
AM27512-30	
AM27512-45	

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
±10% V_{CC} Tolerance	
AM2764A-20	/BXA, /BUA /BUC
AM2764A-25	
AM2764A-30	
AM2764A-45	
AM27128A-20	
AM27128A-25	
AM27128A-30	
AM27128A-45	
AM27256-20	
AM27256-25	
AM27256-30	
AM27256-45	
AM27512-30	/BXA
AM27512-45	

6

FUNCTIONAL DESCRIPTION

Erasing the 8-Bit EPROMs

In order to clear all locations of their programmed contents, it is necessary to expose the EPROMs to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an EPROM. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Angstroms (Å) — with intensity of 12,000 μW/cm^2 for fifteen to twenty minutes. The EPROM should be about directly under and about one inch from the source and all filters should be removed from the ultraviolet light source prior to erasure.

It is important to note that the EPROMs will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with ultraviolet sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the EPROMs and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the 8-Bit EPROMs

Upon delivery, or after each erasure, the EPROM has all bits in the "1", or HIGH state. Zeros ("0s") are loaded into the EPROM through the procedure of programming.

The programming mode is entered when a voltage greater than 12.0, but less than 13.3 V is applied to the V_{PP} pin ($\overline{OE}/V_{PP}$ for 512K) and $\overline{PGM}$ ($\overline{CE}/\overline{PGM}$ for 256K and 512K) is LOW. The data to be programmed is applied 8 bits in parallel to the Data I/O (DQ_n) pins.

The flowchart (Figure 1) in the Programming section of this document shows the AMD-preferred interactive programming algorithm. Interactive algorithms requires less programming time than most other algorithms. This does not preclude the use of other algorithms, including the conventional 50-ms pulse, as long as the maximum specifications are not violated.

The AMD-preferred algorithm reduces programming time by using short (1 ms) program pulses and giving each address only as many pulses as is necessary in order to reliably program the data. After each pulse is applied to a given address, data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 15 pulses. This process is repeated while sequencing through each address of the EPROM. The interactive section of the algorithm is programmed and verified at V_{CC} = 6.0 V, ±5%.

The overprogram section of the algorithm programs the entire array by cycling through each address and applying an additional 2-ms program pulse. This section is done at V_{CC} = 5.0 V, ±5%.

After the final address is completed, the entire EPROM is verified to the data-sheet specifications of V_{CC} = 5.0 V, ±5%.

Auto Select Mode

The Auto Select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient-temperature range required when programming the EPROMs.

To activate this mode, the programming equipment must force 12.0 V ±0.5 V on address line A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Auto Select mode.

Byte 0 ($A_0 = V_{IL}$, $DQ_0 - DQ_7$) represents the manufacturer code, and byte 1 ($A_0 = V_{IH}$, $DQ_0 - DQ_7$), the device identifier code. These identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the most significant bit (MSB), DQ_7, defined as the parity bit.

Read Mode

AMD EPROMs have two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

AMD EPROMs have a standby mode which reduces the active power dissipation up to 80%. The EPROM is placed in the standby mode by applying a TTL HIGH signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accomodate multiple memory connections, a two-line control function is provided to allow for: 1) low-memory power dissipation, and 2) assurance that output-bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array, and connected to the Read line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

Program Inhibit

Programming of multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ or $\overline{PGM}$, all like inputs (including $\overline{OE}$ and V_{PP}) of the parallel EPROMs may be common. A TTL LOW-level program pulse applied to the $\overline{PGM}$ ($\overline{CE}/\overline{PGM}$ for 256K and 512K) input with V_{PP} between 12.0 and 13.3 V and $\overline{CE}$ LOW, will program that EPROM. A HIGH-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed.

Data for all the EPROMs should be verified t_{OE} after the falling edge of $\overline{OE}$, V_{PP} must be between 12.0 V and 13.3 V for all EPROMs except the Am27512 which requires $\overline{OE}/V_{PP}$ to be at V_{IL}.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these

transient current peaks is dependent on the output capacitance loading of the device. A 0.1-μF ceramic capacitor (high-frequency, low-inherent inductance) should be used on each device between V_{CC} and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit-board traces on EPROM arrays, a 4.7-μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

FUNCTION TABLES

TABLE 1. Am2764A and 27128A MODE SELECT

MODE \ PINS	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	V_{PP}	OUTPUTS
Read	L	L	H	X	V_{CC}	D_{OUT}
Output Disable	L	H	H	X	V_{CC}	Hi-Z
Standby	H	X	X	X	V_{CC}	Hi-Z
Program	L	X	L	X	V_{PP}	D_{IN}
Program Verify	L	L	H	X	V_{PP}	D_{OUT}
Program Inhibit	H	X	X	X	V_{PP}	Hi-Z
Auto Select	L	L	H	V_H	V_{CC}	Code

TABLE 2. Am27256 MODE SELECT

MODE \ PINS	$\overline{CE}$/$\overline{PGM}$	$\overline{OE}$	A_9	V_{PP}	OUTPUTS
Read	L	L	X	V_{CC}	D_{OUT}
Output Disable	L	H	X	V_{CC}	Hi-Z
Standby	H	X	X	V_{CC}	Hi-Z
Program	L	H	X	V_{PP}	D_{IN}
Program Verify	H	L	X	V_{PP}	D_{OUT}
Program Inhibit	H	H	X	V_{PP}	Hi-Z
Auto Select	L	L	V_H	V_{CC}	Code

TABLE 3. Am27512 MODE SELECT

MODE \ PINS	$\overline{CE}$/$\overline{PGM}$	$\overline{OE}$/V_{PP}	A_9	OUTPUTS
Read	L	L	X	D_{OUT}
Output Disable	L	H	X	Hi-Z
Standby	H	X	X	Hi-Z
Program	L	V_{PP}	X	D_{IN}
Program Verify	L	L	X	D_{OUT}
Program Inhibit	H	V_{PP}	X	Hi-Z
Auto Select	L	L	V_H	Code

Key: L = LOW
H = HIGH
X = Can be either LOW or HIGH
V_H = 12.0 V ±0.5 V

6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature with Power Applied . −65 to +135°C
Supply Voltage
with respect to Ground
on all Inputs except A_9 and V_{PP} .....+6.25 to −0.6 V
on A_9 ..... +13.50 to −0.6 V
on V_{PP} ..... +13.50 to −0.6 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Industrial (I) Devices
Temperature (T_C) ..... −40 to +85°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Extended Commercial (E) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... (Notes 1 & 2)

Notes: 1. For −1, −2, blank, −3, and −4 versions, V_{CC} = +4.75 to +5.25 V.
2. For −15, −17, −20, −25, −30, and −45 versions, V_{CC} = +4.50 to +5.50 V.

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1, 2, & 4)*

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 1	V
V_{IL}	Input LOW Voltage			−0.1	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 to +5.5 V			10.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 to −5.5 V			10.0	µA
I_{CC1}	V_{CC} Standby Current (Note 6)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	C/I Devices		25	mA
			E/M Devices		40	
I_{CC2}	V_{CC} Active Current for Am2764A	$\overline{OE}$ = $\overline{CE}$ = V_{IL}	C/I Devices		75	mA
			E/M Devices		100	
	V_{CC} Active Current for Am27128A and Am27256		C, I, E & M Devices		100	
	V_{CC} Active Current for Am27512		C/I Devices		100	
			E/M Devices		120	
I_{PP1}	V_{PP} Read Current (except Am27512) (Notes 1 & 5)	V_{PP} = 5.5 V	C, I, E, & M Devices		5	mA
I_{PP2}	$\overline{OE}$/V_{PP} Read Current for Am27512 (Note 5)	$\overline{OE}$/V_{PP} = 5.5 V	C, I, E, & M Devices		10	mA

Notes: See notes following the Capacitance table on next page.

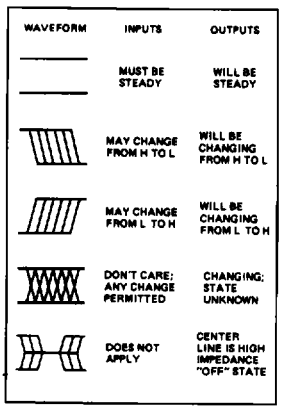
*See the last page of this spec for Group A Subgroup Testing Information.

CAPACITANCE (Notes 2 & 3)

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0 V	4	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0 V	8	12	pF
C_{IN2}	Am27512 $\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0 V	12	20	pF
C_{IN3}	Am27512 $\overline{CE}/\overline{PGM}$ Input Capacitance		9	12	pF

Notes:
1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{CC}.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The EPROMs must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
5. V_{PP} may be connected to V_{CC} directly except during programming. The supply would then be the sum of I_{CC} and I_{PP}.
6. I_{CC1} Max. is 40 mA for −4 and −45 devices.

KEY TO SWITCHING WAVEFORMS



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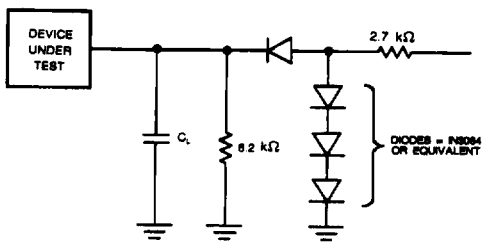
SWITCHING TEST CIRCUITS



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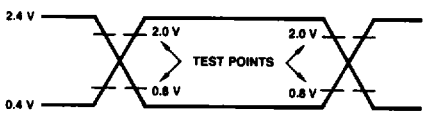
SWITCHING TEST WAVEFORMS



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AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤20 ns.

6

SWITCHING CHARACTERISTICS over operating range unless otherwise specified* (Notes 1 & 3)

(Table 1 of 2)

No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	-1, -15		-1, -17**		-2, -20		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		170		200	ns
2	t_{CE}	Chip Enable to Output Delay			150		170		200	ns
3	t_{OE}	Output Enable to Output Delay			75		75		75	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	60	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

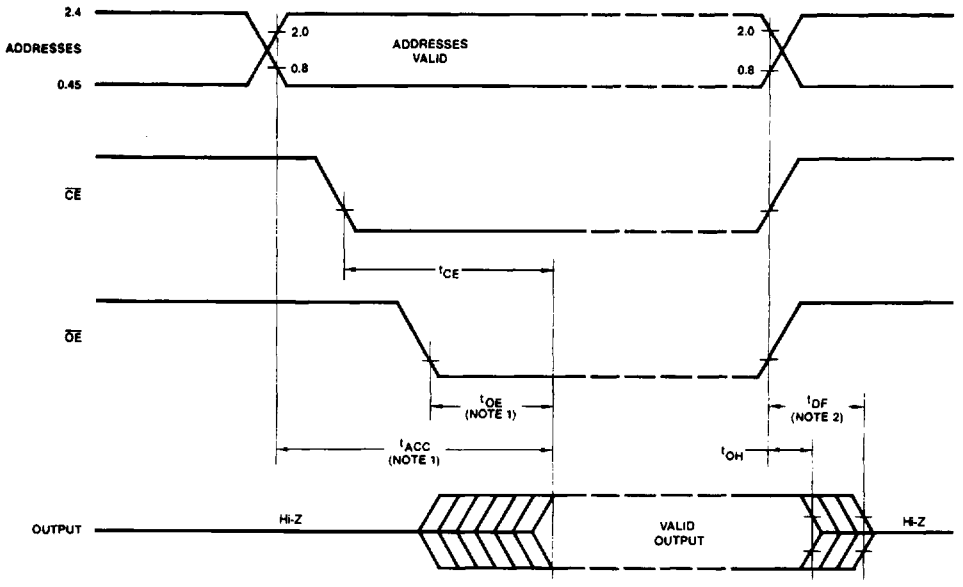
(Table 2 of 2)

No.	Parameter Symbol	Parameter Description	Test Conditions (Note 4)	Blank, -25		-3, -30		-4, -45		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		250		300		450	ns
2	t_{CE}	Chip Enable to Output Delay			250		300		450	ns
3	t_{OE}	Output Enable to Output Delay			100		120		150	ns
4	t_{DF} (Note 2)	Output Enable HIGH to Output Float		0	60	0	60	0	80	ns
5	t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occured first		0		0		0		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and not 100% tested.
3. Caution: The AMD 8-bit EPROM Family must not be removed from or inserted into a socket or board when V_{PP} or V_{CC} is applied.
4. Output Load: 1 TTL gate and $C_L = 100$ pF,
Input Rise and Fall Times: ≤ 20 ns,
Input Pulse Levels: 0.45 to 2.4 V,
Timing Measurement Reference Level — Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V.

*See the last page of this spec for Group A Subgroup Testing information.
**for Am27256 only.

SWITCHING WAVEFORMS



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Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{OE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

6

PROGRAMMING

This section covers Identifier bytes, Interactive Programming Flowchart, and Interactive Programming DC and AC Switching Programming Characteristics.

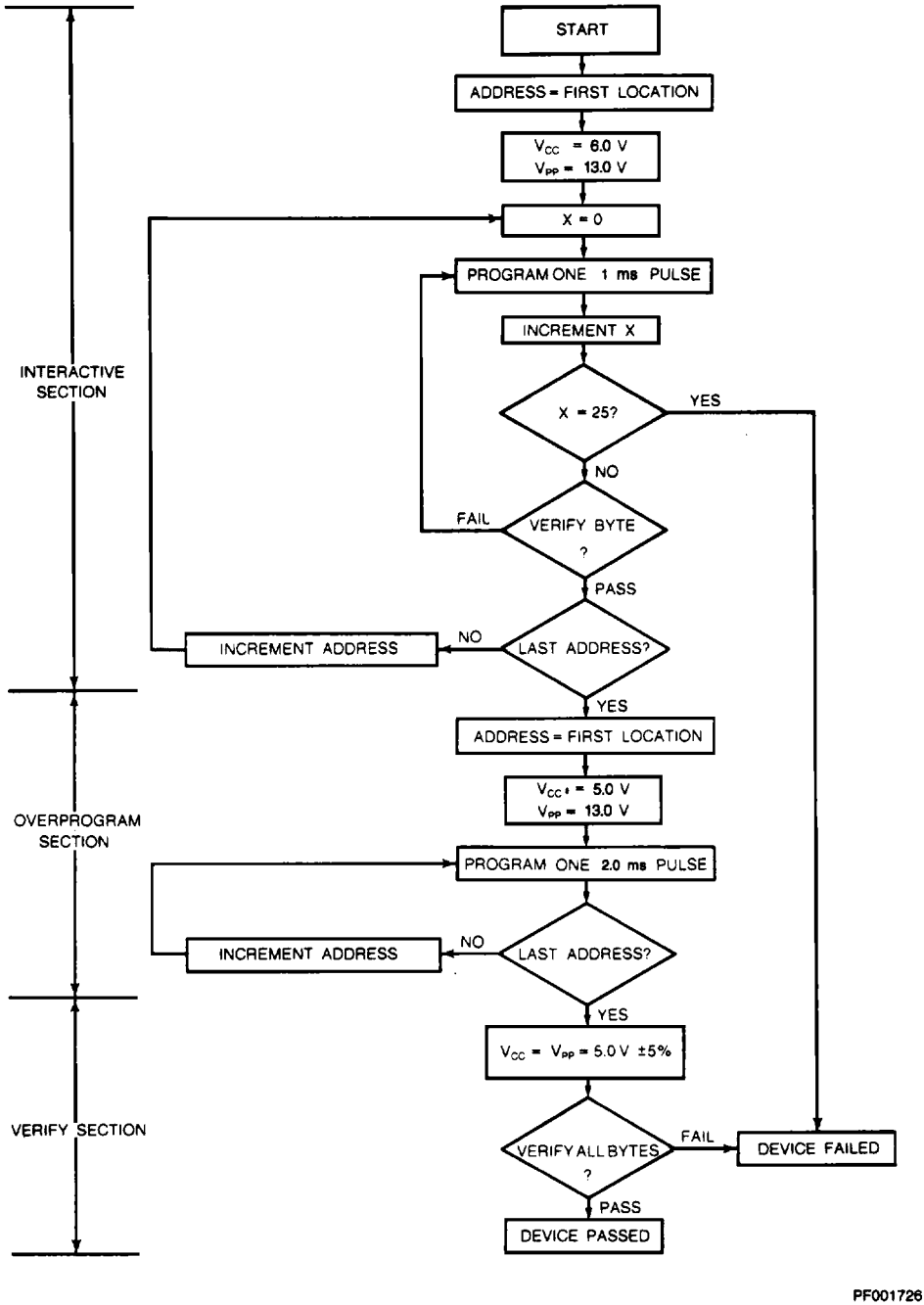

Figure 1. Interactive Programming Flow Chart

TABLE 4. IDENTIFIER BYTES

Identifier \ Pins	A_0	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	0	1	01
Am2764A Device Code	V_{IH}	0	0	0	0	1	0	0	0	08
Am27128A Device Code	V_{IH}	1	0	0	0	1	0	0	1	89
Am27256 Device Code	V_{IH}	0	0	0	0	0	1	0	0	04
Am27512 Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

Notes: 1. $A_9 = 12.0\ V \pm 0.5\ V$
2. All other Address Lines = $\overline{CE} = \overline{OE} = V_{IL}$
3. For Am2764A, $\overline{PGM} = V_{IH}$
4. For Am27256 and Am27512, A_{14} = Don't Care

INTERACTIVE PROGRAMMING ALGORITHM DC CHARACTERISTICS

(Notes 1, 2, and 4)

Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Units
I_{LI}	Input Current (All Inputs)		$V_{IN} = V_{IL}$ or V_{IH}		10.0	μA
V_{IL}	Input LOW Level (All Inputs)			−0.1	0.8	V
V_{IH}	Input HIGH Level			2.0	$V_{CC} + 1$	V
V_{OL}	Output LOW Voltage during Verify		$I_{OL} = 2.1$ mA		.45	V
V_{OH}	Output LOW Voltage during Verify		$I_{OH} = -400$ μA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)	For Am2764A			75	mA
		For Am27128A and Am27256			100	
		For Am27512			150	
I_{PP3}	V_{PP} Supply Current (Program)		$\overline{CE} = V_{IL} = \overline{PGM} = \overline{CE}/\overline{PGM}$		30	mA
V_{ID}	A_9 Auto-Select Voltage			11.5	12.5	V

Notes: See notes following the Interactive Programming Algorithm Switching Programming Characteristics table on next page.

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INTERACTIVE PROGRAMMING ALGORITHM AC SWITCHING PROGRAMMING CHARACTERISTICS

(Notes 1, 2, 3, and 4)

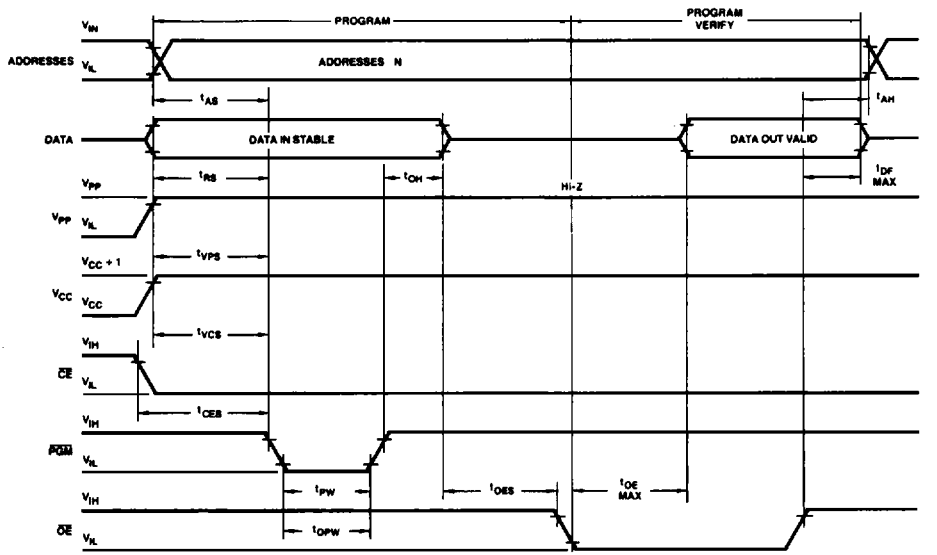
No.	Parameter Symbols	Parameter Description	Min.	Max.	Units
1	t_{AS}	Address Setup Time	2		μs
2	t_{OES}	$\overline{OE}$ Setup Time	2		μs
3	t_{DS}	Data Setup Time	2		μs
4	t_{AH}	Address Hold Time	2		μs
5	t_{DH}	Data Hold Time	2		μs
6	t_{DF}	Chip Enable to Output Float Delay	0	130	μs
7	t_{VPS}	V_{PP} Setup Time	2.0		μs
8	t_{VCS}	V_{CC} Setup Time	2		μs
9	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	.95	1.05	ms
10	t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width (Note 3)	1.95	78.75	ms
11	t_{CES}	$\overline{CE}$ Setup Time	2		μs
12	t_{OE}	Data Valid from $\overline{OE}$		150	ns
13	t_{DV}	Am27512 Data Valid from $\overline{CE}$		450	ns

Notes: 1. $T_A = +25°C \pm 5°C$; $V_{CC} = 6.0\ V \pm 0.25\ V$; $V_{PP} = 12.0$ to $13.3\ V$.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
3. When programming the EPROM family, a 0.1-μF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.
4. Programming characteristics are guidelines which must be followed. They are not 100% tested to worst-case limits.

INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS (Cont'd.)

Am2764A and Am27128A

(Notes 1 and 2)



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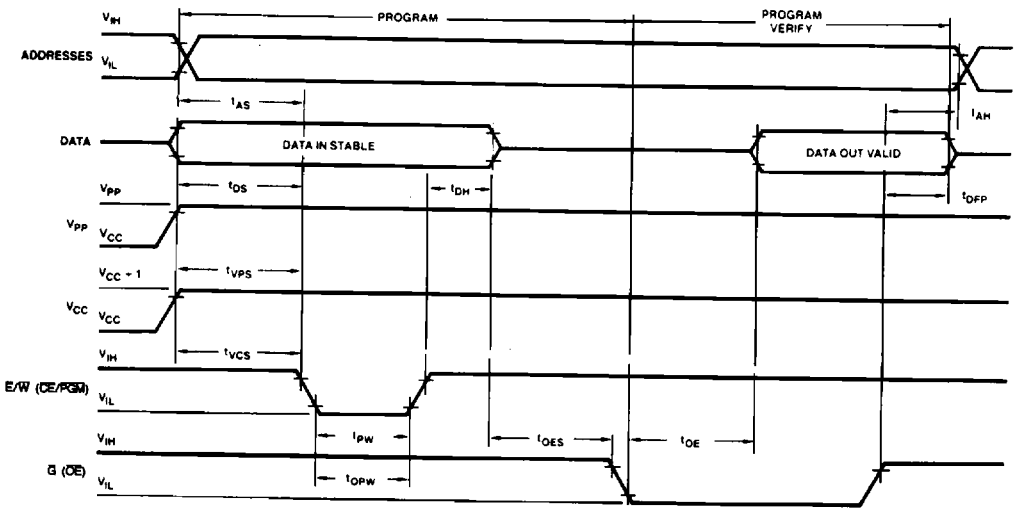
Notes: See notes following the Am27512 Waveform on next page.

Am27256
(Notes 1 and 3)



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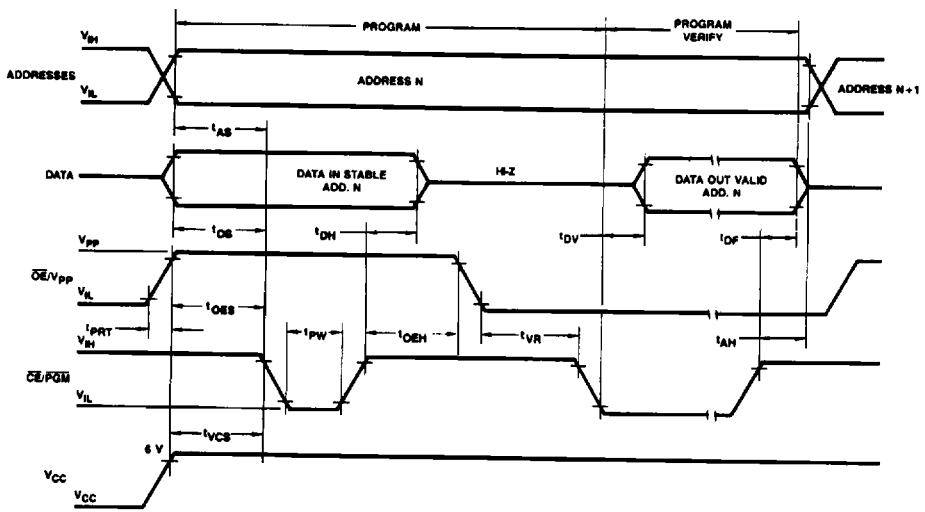
Am27512
(Notes 1 and 2)



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Notes: 1. The input timing reference level is 0.8 V for V_{IL} and 2 V for V_{IH}.
2. t_{OE} and t_{DF} are characteristics of the device, but must be accommodated by the programmer.
3. t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.

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GROUP A SUBGROUP TESTING

DC CHARACTERISTICS

Parameter Symbol	Subgroups*
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{LI}	1, 2, 3
I_{LO}	1, 2, 3
I_{CC1}	1, 2, 3
I_{CC2}	1, 2, 3
I_{PP1}	1, 2, 3
I_{PP2}	1, 2, 3
C_{IN}	4
C_{OUT}	4
C_{IN2}	4
C_{IN3}	4

*For DC Programming Characteristics, only Subgroup 1 applies.

SWITCHING CHARACTERISTICS

No.	Parameter Symbol	Subgroups
1	t_{ACC}	9, 10, 11
2	t_{CE}	9, 10, 11
3	t_{OE}	9, 10, 11
4	t_{DF}	9
5	t_{OH}	9

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.