FEATURES

- CMOS technology
  - –Rev R compatible with MC6845R1, MC6845 and MC146845
  - –Rev S compatible with HD6845S
- Internal refresh address generation
- Light pen interface
- Character clocks up to 8 MHz
- Bus clocks up to 3 MHz
- Single 5 V power supply

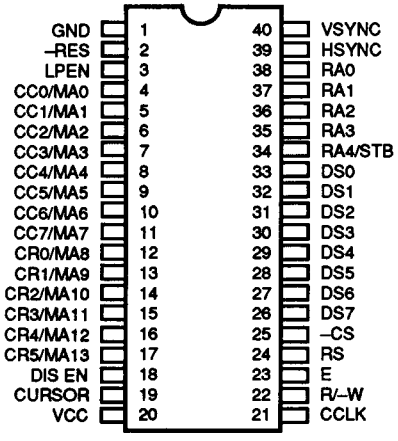
DESCRIPTION

The VL68C45X is a family of CRT controllers that are widely used in both bit-mapped and character-mapped applications for both terminals and personal computers. VL68C45 family allows designs to consume less power through the use of CMOS technology.

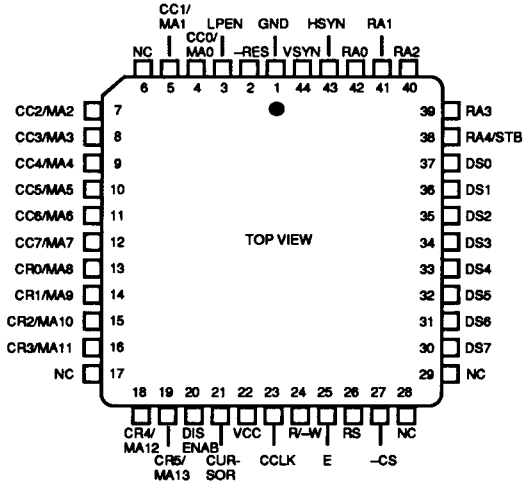
In addition to compatibility with both the Motorola and Hitachi families, the VL68C45R also contains enhancements found in the MC6845R1. These enhancements allow for higher resolution displays without extra external hardware.

PIN DIAGRAMS

VL68C45R/S-PC,CC



VL68C45R/S-QC



ORDER INFORMATION

Part Number	Clock Frequency		Package
	Bus	Character	
VL68C45R-23 VL68C45S-23	2 MHz	3 MHz	To specify package type, add the appropriate suffix to the part number: PC = Plastic DIP CC = Ceramic DIP QC = Plastic Leaded Chip Carrier (PLCC)
VL68C45R-35 VL68C45S-35	3 MHz	5 MHz	
VL68C45R-36 VL68C45S-36		6 MHz	
VL68C45R-38 VL68C45S-38		8 MHz	

Note: Operating temperature range is 0°C to +70°C.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number (DIP)	Signal Description
E	23	Enable - Input that is used as a data strobe; does not have to be a free-running clock. This capability allows the VL68C45 to interface with other non-6800/6500-type microprocessors.
R/–W	22	Read/–Write - Input that, when high, allows the processor to read the data supplied by the VL68C45; when this signal is low, the processor writes into the VL68C45.
–CS	25	–Chip Select - Input that, when high, deselects VL68C45; when this signal is low, the VL68C45 is selected. This signal is typically connected to the system address bus either directly or through an address decoder.
RS	24	Register Select - Input that, when low, selects the Address Register of the VL68C45 for a write operation. When this signal is high, an internal register of the VL68C45 specified by the contents of the address register is selected.
D0 - D7	26 - 33	Data Bus - Eight bidirectional data lines that are used for transferring data between the microprocessor and the VL68C45. These lines are normally high-impedance, except during read and write cycles when the chip is selected.
CC0/MA0 - CC5/MA13	4 - 17	Video Memory Address - Active-high output signals that are used to address the video display memory in binary addressing mode. These memory addresses are generated in a binary sequential fashion. In row/column addressing mode, MA0-MA7 function as column addresses, and MA8-MA13 function as row addresses.
RA0 - RA4/STB	34 - 38	Raster Address - Active-high output signals that are used as address lines to the external character generator ROM. In the transparent addressing mode, RA4 functions as an active-high output strobe.
HSYNC	39	Horizontal Sync - Active-high TTL-compatible output signal that is used to determine the horizontal position of the displayed text. VSYNC may be used to drive a CRT monitor directly or may be used for composite video generation. VSYNC position is fully programmable.
VSYNC	40	Vertical Sync - Active-high, TTL-compatible output signal that is used to determine the vertical position of the displayed text. VSYNC may be used to drive a CRT monitor directly or may be used for composite video generation. VSYNC position is fully programmable.
DISPLAY	18	Display Enable - TTL-compatible output that, when high, indicates that the VL68C45 is generating active display information. The number of horizontal displayed characters and the number of vertical displayed rows are both fully programmable and together are used to generate the Display Enable signal.
CURSOR	19	Cursor - TTL-compatible output that when high, indicates a valid cursor address to the external video processing logic.
LPSTB	3	Light Pen Strobe - high impedance, edge-sensitive input signal that latches the current refresh address into the light pen register. Latching occurs on the low-to-high transition edge.
CCLK	21	Character Clock - Input signals derived from the external dot clock, that is used as the time base for all internal count and control functions.
–RES	2	–Reset - Input signal that when low, resets all internal counters. All scan and video outputs are low and all control registers are unaffected. RES can be used to synchronize display frame timing with the line frequency.
VCC	20	Power Supply Voltage is 5 V.
GND	1	Ground - Supply and signal ground

FUNCTIONAL DESCRIPTION

The VL68C45 CRT Controller (CRTC) consists of programmable horizontal and vertical timing generators, programmable linear address registers, programmable cursor logic, a light pen capture register and control circuitry for interface to a processor bus.

All CRTC timing is derived from the character clock (CCLK), which is usually the output of an external dot rate counter. Coincidence circuits internal to the chip continuously compare counter contents to the programmed register file (R0-R17) for generation of Horizontal Sync, Vertical Sync, Display Enable, Cursor and other signals required to interface to a CRT display.

The linear address generator is also driven by the CCLK and locates the positions of characters of memory. The CRTC addresses the memory in the binary sequential fashion. Using the start address register, hardware scrolling through the 16k character memory is possible. The linear address generator continues to increment during the blanking period, so memory refresh can be performed during the blanking periods. The linear address generator repeats the same sequence of addresses for each scan line of a character row. Although the linear address generator continues to increment during the horizontal and blanking periods, the correct address for the first displayed character or row is always maintained.

The Cursor logic determines the cursor location, size and blink rate on the screen.

The Light Pen Strobe latches the current contents of the address counter into the light pen register on low-to-high transition.

INTERLACE MODE SELECTION

In the normal sync mode (non-interlace), only one field is available, as shown in Figure 1a. Each scan line is refreshed at the VSYNC frequency (50 or 60 Hz).

Two interlace modes are available as shown in Figure 1b and Figure 1c. The frame time is divided between even and odd alternating fields. The horizontal and vertical timing relationship (VSYNC delayed by one-half scan line time) results in the displacement of scan lines in the odd field with respect to the even field.

In the interlace sync mode, the same information is painted in both fields, as shown in Figure 1b. This is a useful mode for filling in a character to enhance readability.

In the interlace sync and video mode, as shown in Figure 1c, alternating lines of the character are displayed in the even field and the odd field. This effectively doubles the given band width of the CRT monitor.

Care must be taken when using either interlace mode to avoid an apparent flicker effect. This flicker effect is due to the doubling of the refresh time for all scan lines since each field is displayed alternately and may be minimized with proper monitor design i.e., longer persistence phosphors.

VL68C45R REGISTER FILE DESCRIPTIONS

The 19 registers of the CRTC may be accessed through the data bus. Only two memory locations are required, as one location is used as a pointer to address one of the remaining 18 registers. These 18 registers control horizontal timing, vertical timing, interlace operation and row address operation. They also define the cursor, cursor address, start address and light pen register. The register addresses and sizes are shown in Table 1.

ADDRESS REGISTER (AR)

The Address Register is a 5-bit write-only register used as an "indirect" or "pointer" register. It contains the address of one of the other 18 registers. When both RS and –CS are low, the Address Register is selected. When –CS is low and RS is high, the register pointed to by the address register is selected.

FIGURE 1a.
NORMAL SYNC

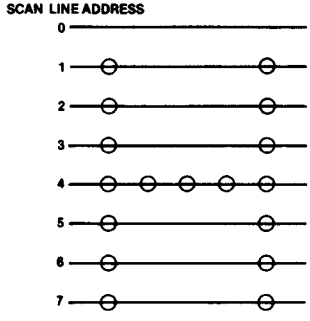


FIGURE 1b.
INTERLACE SYNC

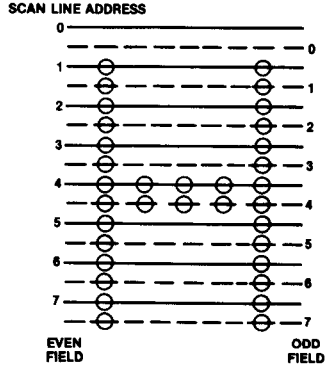
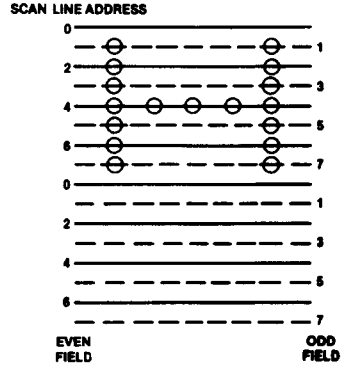


FIGURE 1c.
INTERLACE SYNC AND VIDEO



VL68C45R REGISTER FILE DESCRIPTIONS (Cont.)

HORIZONTAL TOTAL REGISTER (R0)

This 8-bit write-only register determines the horizontal sync (HSYNC) frequency by defining the HSYNC period in character times. It is the total of the displayed characters plus the non-displayed character times (retrace) minus one.

HORIZONTAL DISPLAYED REGISTER (R1)

This 8-bit write-only register determines the number of displayed characters per line. Any 8-bit number may be programmed as long as the contents of R0 are greater than the contents of R1.

HORIZONTAL SYNC POSITION REGISTER (R2)

This 8-bit write-only register controls the HSYNC position, which defines the horizontal sync delay (front porch) and the horizontal scan delay (back porch). When the programmed value of this register is increased, the display on the CRT screen is shifted to the left. When the programmed value is decreased, the display is shifted to the right. Any 8-bit number may be programmed as long as the sum of the contents of R2 and R3 is less than the contents of R0. The contents of R2 must be greater than R1.

SYNC WIDTH REGISTER (R3)

This 8-bit write-only register determines the width of the HSYNC pule. The vertical sync pulse width is fixed at 16 scan-line times. HSYNC pulse width may be programmed from 1 to 15 character clock periods, thus allowing compatibility with the HSYNC pulse width specifications of many different monitors. If zero is written into this register, no horizontal sync is provided.

HORIZONTAL TIMING SUMMARY

The difference between R0 and R1 is the horizontal blanking interval. This interval in the horizontal scan period allows the beam to return (retract) to the left side of the screen. The retrace time is determined by the monitor horizontal scan components. Retrace time is less than the horizontal blanking interval.

A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT. In inexpensive TV receivers the beam over-scans the display screen so that aging of parts does not result in underscanning. Because of this, the retrace time should be about one-third the horizontal scanning period. The horizontal sync delay is typically programmed with a 1:2:2 ratio.

VERTICAL TOTAL REGISTER (R4) AND VERTICAL TOTAL ADJUST REGISTER (R5)

The vertical sync (VSYNC) frequency is determined by both R4 and R5. The calculated number of character row

TABLE 1. VL68C45R INTERNAL REGISTER ASSIGNMENTS

-CS	RS	Address Register					Register #	Register File	Program Unit	Read	Write	Number of Bits							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	—	—	—	—								
0	0	X	X	X	X	X	AR	Address Register	—	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes					H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes							I	I
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes		B	P				(Note 2)	
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	—	No	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	—	No	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	—	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	—	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	—	Yes	No								

Notes:

1. The interlace bits are described in Table 2.
2. Bit 5 of the cursor start raster register is used for blink period, control, and bit 6 is used to select blink or no-blink.
3. Registers R4, R6 and R7 in the VL68C45R are eight bits wide, instead of seven, for compatibility with the Motorola 6845R1.

VL68C45R REGISTER FILE DESCRIPTIONS (Cont.)

times is usually an integer plus a fraction to get exactly a 50 Hz or 60 Hz vertical refresh rate. The integer number of character row times minus one is programmed into the 7-bit write-only vertical total register (R4). The fraction of character line times is programmed into the 5-bit write-only vertical total adjust register (R5) as the number of scan lines required.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit write-only register specifies the number of character rows displayed on the CRT screen, and is programmed in character row times. Any number smaller than contents R4 may be programmed into R6.

VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. When programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased, the display position is shifted down. Any number equal to or less than the contents of R4 and greater than or equal to the R6 may be used.

INTERLACE MODE AND SKEW REGISTER (R8)

The VL68C45R only allows control of the interlace modes as programmed by the low-order two bits of this write-only register. Table 2 shows the interlace modes available to the user. These modes are selected using the two low order bits of this 6-bit write-only register.

TABLE 2: INTERLACE MODE REGISTER

Bit 1	Bit 2	Mode
0	0	Normal Sync Mode
1	0	(Non-interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

There are restrictions on the programming of the VL68C45R registers for interlace operation:

1. The Horizontal Total Register (R0) value must be odd (i.e., and even number of character times).
2. For interlace sync and video mode only, the Maximum Scanline Address Register (R9) value must be odd (i.e., an even number of scan lines).
3. For interlace sync and video mode only, the number (Nvd) programmed in to the Vertical Display Register (R6) must be one-half the actual number required. The even-numbered scan lines are displayed in the even field and the off-numbered scan lines are displayed in the odd field.
4. For interlace sync and video mode only, the Cursor Start Register (R10 and Cursor End Register (R11) must both be even or odd, depending on which field the cursor is to be displayed in. A full block cursor will be displayed in both the even and the odd field when the Cursor End Register (R11) is programmed to a value greater than the value in the Maximum Scan Line Address Register (R9).

MAXIMUM SCAN LINE ADDRESS REGISTER (R9)

This 5-bit write-only register determines the number of scan lines per character row, including the spacing, thus controlling operation of the row address counter. The programmed value is a maximum address and is one less than the number of scan lines.

CURSOR CONTROL REGISTERS

CURSOR START REGISTER (R10) AND CURSOR END REGISTER (R11)

These registers allow a cursor of up to 32 lines in height to be placed on any scan line of the character block. Register R10 is a 7-bit write-only register used to define the start scan line and the cursor blink rate. Bits 5 and 6 of the Cursor Start Address Register control the cursor operation as shown in table 3. Non-display, display, and two blink modes (16 times or 32 times the field period) are available. Register R11 is a 5-bit write-only register that defines the last scan cursor.

When an external blink feature on characters is required, it may be

TABLE 3. CURSOR START REGISTER

Bit 6	Bit 5	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink, 1/16 field rate
1	1	Blink, 1/32 field rate

necessary to perform cursor blink externally so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRT for a blinking cursor and externally inverting the video signal with an exclusive-OR gate.

CURSOR REGISTER (R14-H, R15-L)

This 14-bit read/write register pair is programmed to position the cursor anywhere in the refresh RAM area, thus allowing hardware paging and scrolling through memory without loss of the original cursor position. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register.

START ADDRESS AND LIGHT PEN REGISTERS

START ADDRESS REGISTER (R12-H, R13-L)

This 14-bit write-only register pair controls the first address output by the CRTC after vertical blanking. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register. The start address register determines which portion of the refresh RAM is displayed on the CRT screen. Hardware scrolling by character or page may be accomplished by modifying the contents of this register.

LIGHT PEN REGISTER (R16-H, R17-L)

This 14-bit read-only register pair captures the refresh address output by the CRTC on the positive edge of a pulse input to the LPSTB pin. It consists of an 8-bit low-order (MA0-MA7) register and a 6-bit high-order (MA8-MA13) register. Since the light pen pulse is asynchronous with respect to refresh address timing, an internal synchronizer is designed into the CRTC. Due to delays in this circuit, the value of R16 and R17 will need to be corrected in software. (See the bus timing diagram in the Timing Characteristics section).

TABLE 4. VL68C45S INTERNAL REGISTER ASSIGNMENTS, (Note 1)

–CS	RS	Address Register					Register #	Register Name	Program Unit	READ	WRITE	Data Bit							
		4	3	2	1	0						7	6	5	4	3	2	1	0
1	x	x	x	x	x	x			–	–	–								
0	0	x	x	x	x	x	AR	Address Register	–	×	○								
0	1	0	0	0	0	0	R0	Horizontal Total*	Character	×	○								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Character	×	○								
0	1	0	0	0	1	0	R2	Horizontal Sync* Position	Character	×	○								
0	1	0	0	0	1	1	R3	Sync Width	Vertical-Raster, Horizontal-Character	×	○	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0	0	1	0	0	R4	Vertical Total*	Line	×	○								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	Raster	×	○								
0	1	0	0	1	1	0	R6	Vertical Displayed	Line	×	○								
0	1	0	0	1	1	1	R7	Vertical Sync* Position	Line	×	○								
0	1	0	1	0	0	0	R8	Interlace & Skew	–	×	○	C1	C0	D1	D0			V	S
0	1	0	1	0	0	1	R9	Maximum Raster Address	Raster	×	○								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Raster	×	○		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Raster	×	○								
0	1	0	1	1	0	0	R12	Start Address (H)	–	○	○								
0	1	0	1	1	0	1	R13	Start Address (L)	–	○	○								
0	1	0	1	1	1	0	R14	Cursor (H)	–	○	○								
0	1	0	1	1	1	1	R15	Cursor (L)	–	○	○								
0	1	1	0	0	0	0	R16	Light Pen (H)	–	○	×								
0	1	1	0	0	0	1	R17	Light Pen (L)	–	○	×								

Note:
1. ○ = yes; × = no

VL68C45S REGISTER FILE DESCRIPTIONS (Cont.)

ADDRESS REGISTER (AR)

This is a 5-bit register that is used to select 18 internal control registers (R0-R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0-R17 requires writing the address of the corresponding control register into this register. When RS and CS are LOW, the address is selected.

HORIZONTAL TOTAL REGISTER (R0)

This 8-bit register is used to program the total number of horizontal characters per line, including the retrace period. The data value should be programmed according to the specification of the CRT. When M is the total number of characters, (M-1) must be programmed into this register. When programming for interlace mode, M must be even.

HORIZONTAL DISPLAYED REGISTER (R1)

This 8-bit register is used to program the number of horizontal displayed characters per line. Any 8-bit number that is smaller than that of horizontal total register contents can be programmed.

HORIZONTAL SYNC POSITION REGISTER (R2)

This 8-bit register is used to program horizontal sync position as multiples of the character clock period. Any 8-bit number that is lower than the horizontal total register contents can be programmed. When H is the character number of the horizontal sync position, (H-1) must be programmed into this register. When the programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When the programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

SYNC WIDTH REGISTER (R3)

This 8-bit register is used to program the horizontal sync (HS) pulse width and the vertical sync (VS) pulse width. The horizontal sync pulse width is programmed in the lower four-bits as multiples of the character clock period (see Table 5); a zero cannot be programmed. The vertical sync pulse width is programmed in the higher four bits as multiples of the raster period (see Table 6). When zeroes are programmed in the higher four bits, a 16-raster period is specified.

VERTICAL TOTAL REGISTER (R4)

This 7-bit register is used to program the total number of lines per frame, including vertical retrace period. The data and its value should be programmed according to the specification of the CRTC. When N is the total number of lines, (N-1) must be programmed into this register.

VERTICAL TOTAL ADJUST REGISTER (R5)

This 5-bit register is used to program the optimum number to adjust the total number of rasters per field. This register enables more precise control of the deflection frequency.

VERTICAL DISPLAYED REGISTER (R6)

This 7-bit register is used to program the number of displayed character rows on the CRT screen. Any 7-bit number that is smaller than that of vertical total register contents can be programmed.

VERTICAL SYNC POSITION REGISTER (R7)

This 7-bit register is used to program the vertical sync position on the screen as multiples of the horizontal character line period. Any number that is equal to or less than the vertical total register content can be programmed. When V is the character number of vertical sync position, (V-1) must be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When the programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

INTERLACE AND SKEW REGISTER (R8)

This register is used to program raster scan mode and skew (delay) of the Cursor signal and Display Enable signals.

INTERLACE MODE PROGRAM BITS (V,S)

Raster scan mode is programmed (see Table 7) by the V and S bits of R8. In the non-interlace mode, duplicate scanning is done of the rasters of even number field and odd number field. In the interlace sync mode, the rasters of the odd number field are scanned in the middle of the even number field. The same character pattern is then displayed in two fields. In the interlace sync and video mode, the raster scan method is the same as in the interlace sync mode, but it is controlled to display different character patterns in two fields.

Table 4 Additional Notes:

1. The registers marked*: (written value) = (specified value) –1
2. Written value of R9:
   a) Non-Interlace mode and Interlace Sync Mode (written value Nr) = (specified value) –1
   b) Interlace sync and video mode: (Written value Nr) = (specified value) –2
3. CO and C1 specify skew of CURSOR output signal. DO and D1 specify skew of Display Enable output signal. When S is one, V specifies video mode. S specifies the Interlace sync mode.
4. B specifies cursor blink.
   P specifies the cursor blink period.
5. wv0~wv3 specify the pulse width of the vertical sync signal. wh0 ~ wh3 specify the pulse width of the horizontal sync signal.
6. R0 is normally programmed to be an odd number in interlace mode.

VL68C45S
REGISTER FILE DESCRIPTIONS (Cont.)

TABLE 5: PULSE WIDTH OF HORIZONTAL SYNC SIGNAL

VSW/HSW Register (R3)				HSW Pulse Width (multiples of char clock period)
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	Not Allowed
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

TABLE 6: PULSE WIDTH OF VERTICAL SYNC SIGNAL

VSW/HSW Register (R3)				VSW Pulse Width (multiples of raster period)
Bit 7	Bit 6	Bit 5	Bit 4	
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

TABLE 7: INTERLACE MODE BITS (BITS 1 AND 0 of R8)

V Bit 1	S Bit 2	Mode
0	0	Normal Sync Mode
1	0	(Non-interlace)
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

SKEW PROGRAM BITS (C1,C0,D1,D0)

These bits are used to program the skew (delay) of the Cursor and Display Enable signals.

Skew of these two kinds of signals is programmed separately. The skew function is used to provide an on-chip delay for the output timing of the Cursor and Display Enable Signals to provide the time required to access refresh memory, character generator or pattern generator, and to ensure that they are

TABLE 8: DISPLAY ENABLE SKEW BIT (BITS 5 AND 4 OF R8)

D1 Bit 5	D0 Bit 4	Display Enable Signal
0	0	Non-Skew
0	1	One-character Skew
1	0	Two-character Skew
1	1	Non-output

TABLE 9: CURSOR SKEW BITS (BITS 7 & 6 OF R8)

C1 Bit 7	C0 Bit 6	Display Skew
0	0	Non-Skew
0	1	One-character Skew
1	0	Two-character Skew
1	1	Non-output

VL68C45S REGISTER FILE DESCRIPTIONS (Cont.)

in phase with the serial video signal.

MAXIMUM RASTER ADDRESS REGISTER (R9)

This 5-bit register is used to program the Maximum Raster Address. This register defines total number of rasters per character, including space.

This register is programmed as follows:

1. Non-Interlace Mode,
   Interlace Sync Mode: When the total number of rasters is RN, (RN-1) must be programmed.
2. Interlace Sync and Video Mode: When total number of rasters is RN, (RN-2) must be programmed.

The total number of rasters in non-interlace mode, interlace sync mode and interlace sync and video mode is

TABLE 10: RASTER COUNT IN INTERLACE AND NON-INTERLACE MODES

0 _____ Total number of rasters 5

1 _____ Programmed value Nr = 4

2 _____ (The same as displayed total number of rasters)

3 _____

4 _____

Raster Address

INTERLACE SYNC MODE

0 _____ Total number of rasters 5

_ _ _ _ _ _ _ _ _ _ _ 0 programmed value Nr = 4

1 _____

_ _ _ _ _ _ _ _ _ _ _ 1

2 _____

_ _ _ _ _ _ _ _ _ _ _ 2

3 _____

_ _ _ _ _ _ _ _ _ _ _ 3

In the interlace sync mode, total number of rasters in both the even and odd fields is ten. On programming, the half of it is defined as total number of rasters.

4 _____

_ _ _ _ _ _ _ _ _ _ _ 4

Raster Address

INTERLACE SYNC AND VIDEO MODE

0 _____ Total Number of Rasters 5

_ _ _ _ _ _ _ _ _ _ _ 1 Programmed Value Nr = 3

2 _____

_ _ _ _ _ _ _ _ _ _ _ 3

4 _____

(Total number of rasters displayed in the even field and the odd field)

Raster Address

defined as follows in Table 10.

CURSOR START RASTER REGISTER (R10)

This 7-bit register is used to program the cursor start raster address and the cursor display mode. The lower five bits program the raster address and the higher two bits program the display mode (see table 11).

TABLE 11: CURSOR DISPLAY MODE (BITS 6 AND 5 OF R10)

B Bit 6	P Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate

Note:
The blink sequence is follows:

Light	Dark

(16 x or 32 x the field period)

CURSER END RASTER REGISTER (R11)

This register is used to program the cursor end raster address.

START ADDRESS REGISTER (R12,R13)

This register pair is used to program the first address of refresh memory read out. Paging and scrolling are easily performed using this register. This register can be read but the higher 2-bits of R12 are always zero.

CURSOR REGISTER (R14, R15)

These two read/write registers store the cursor location. The higher 2 bits of R14 are zero.

LIGHT PEN REGISTER (R16, R17)

These read-only registers are used to capture the detection address of the light pen. The higher 2 bits of R16 are always zero. The value of R16 and R17 needs to be corrected by software because there is a time delay from the address output by the CRTC to the signal input to its LPSTB pin that the light pen detects.

CONSIDERATIONS IN UPDATING REGISTERS

The value programmed into the internal registers directly controls the CRT. Consequently, the display may flicker on the screen when the contents of the registers are changed from the bus side asynchronously with display operation.

RESTRICTIONS ON PROGRAMMING INTERNAL REGISTERS

1. $0 \leq Nhd \leq Nht + 1 \leq 256$
2. $0 \leq Nvd \leq Nvt + 1 \leq 128$
3. $0 \leq Nhsp \leq Nht$
4. $0 \leq Nvsp \leq Nvt$, Note 1
5. $0 \leq NCSTART \leq NCEND \leq Nr$ (non-interlace, interlace sync mode)
   $0, NCSTART \leq NCEND \leq Nr + 1$ (interlace and video mode)
6. $2 \leq Nr \leq 30$
7. $3 \leq Nht$ (except non-interlace mode)
   $5 \leq Nht$ (non-interlace mode only)

UPDATING THE CURSOR REGISTER

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace periods.

UPDATING THE START ADDRESS REGISTER

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display periods.

It is desirable to avoid programming any registers besides the cursor and Start Address Register during display operations.

In the interlace mode, pulse width is changed + 1/2 raster time when vertical sync signal extends over two fields.

VL68C45 CHARACTERISTICS

SYSTEM DIAGRAM

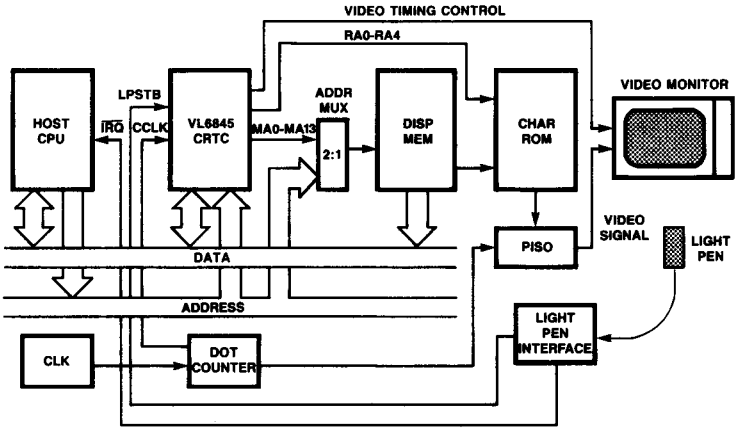
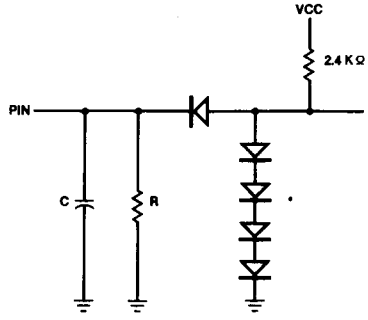


FIGURE 1. TEST LOAD

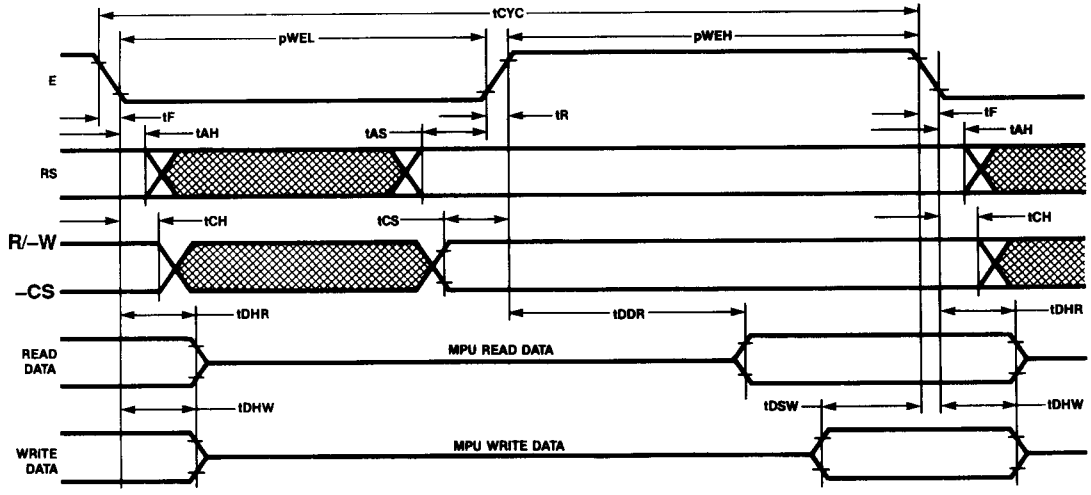


R = 11 KΩ FOR DB0—DB7
R = 24 KΩ FOR ALL OTHER OUTPUTS
C = 130 pF TOTAL FOR DO—D7
C = 30 pF ALL OTHER OUTPUTS

TABLE 12. CRTC BUS TIMING CHARACTERISTICS

Symbol	Parameter	VL68C45R-23 VL68C45S-23		VL68C45R-35 VL68C45S-35 VL68C45R-36 VL68C45S-36 VL68C45R-38 VL68C45S-38		Unit
		Min	Max	Min	Max	
tCYC	Cycle Time	500		333		ns
pWEL	Pulse Width, E Low	190		140		ns
pWEH	Pulse Width, E High	200		150		ns
tR	Clock Rise Time		30		30	ns
tF	Clock Fall Time		30		30	ns
tAH	Address Hold Time (RS)	0		0		ns
tAS	RS Setup Time	40		30		ns
tCS	R/–W, CS Setup	40		30		ns
tCH	R/–W, CS Hold Time	0		0		ns
tDHR	Read Data Hold Time	20	60	20	60	ns
tDHW	Write Data Hold Time	10		10		ns
tDDR	Peripheral Output Delay Time	0	150	0	130	ns
tDSW	Peripheral Setup Time	60		60		ns

FIGURE 2. BUS TIMING

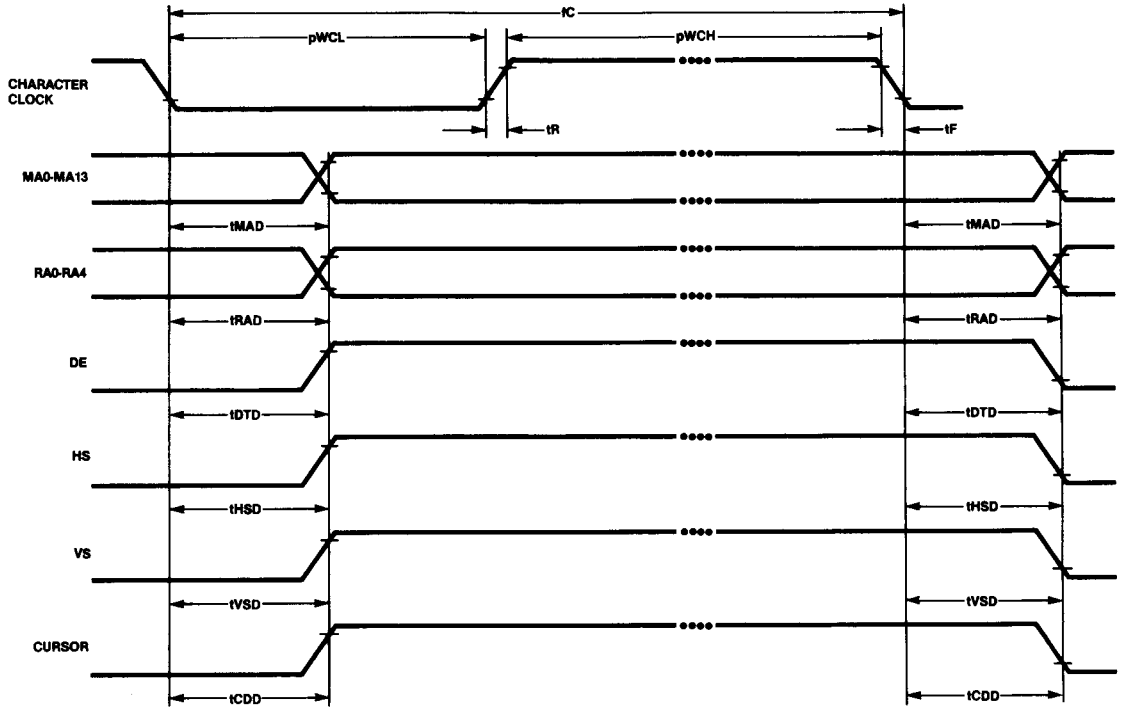


NOTES:
1. VOLTAGE LEVELS SHOWN ARE V1≤ 0.4V, Vh≥ 2.4V
2. MEASUREMENT POINTS SHOWN ARE 0.8V AND 2.0V.

TABLE 13. CRTC VIDEO TIMING CHARACTERISTICS

Symbol	Parameter	VL68C45R-23 VL68C45S-23		VL68C45R-35 VL68C45S-35		VL68C45R-36 VL68C45S-36		VL68C45R-38 VL68C45S-38		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
pWCL	Clock Pulse Width, Low	150		100		66		56		ns
pWCH	Clock Pulse Width, High	150		100		72		56		ns
fC	Clock Frequency		3		5		6		8	MHz
tR	Clock Rise Time		20		20		20		15	ns
tF	Clock Fall Time		20		20		8		8	ns
tMAD	Memory Address Delay Time		160		140		100		100	ns
tRAD	Raster Address Delay Time		160		140		100		100	ns
tDTD	Display Timing Delay Time		250		200		100		100	ns
tHSD	Horizontal Sync Delay Time		250		200		100		100	ns
tVSD	Vertical Sync Delay Time		250		200		100		100	ns
tCDD	Cursor Display Delay Time		250		200		100		100	ns

FIGURE 3. VIDEO TIMING

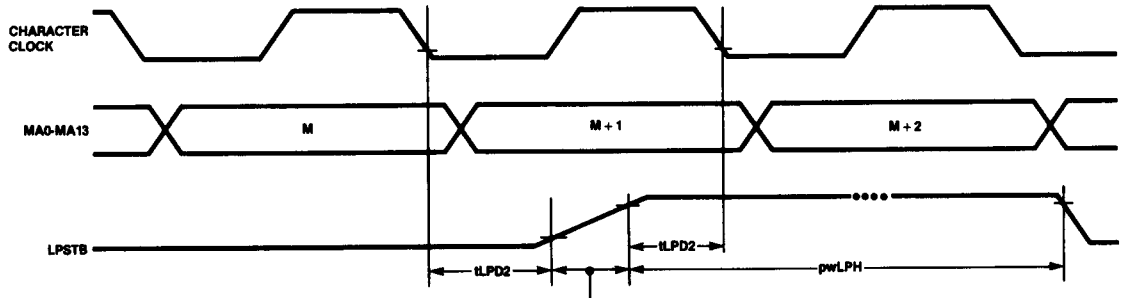


NOTES:
TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS UNLESS OTHERWISE SPECIFIED

TABLE 14. CRTC LIGHT PEN TIMING CHARACTERISTICS

Symbol	Parameter	VL68C45R-23 VL68C45S-23		VL68C45R-35 VL68C45S-35 VL68C45R-36 VL68C45S-36 VL68C45R-38 VL68C45S-38		Unit
		Min	Max	Min	Max	
pwLPH	Light Pen Strobe Pulse Width	80		60		ns
tLPD1	Light Pen Display Time 1		120		70	ns
tLPD2	Light Pen Display Time 2		0		0	ns

FIGURE 4. LIGHT PEN TIMING



NOTES:
1. TIMING MEASUREMENTS ARE REFERENCED TO AND FROM A LOW VOLTAGE OF 0.8 VOLTS AND A HIGH VOLTAGE OF 2.0 VOLTS, UNLESS OTHERWISE NOTED.

2. tLPD1 AND tLPD2 ARE THE PERIODS OF UNCERTAINTY FOR THE REFRESH MEMORY ADDRESS.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to 150°C
Supply Voltage to Ground Potential	–0.3 to +7.0 V
Applied Voltage	–0.3 to +7.0 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to 70°C, VCC = ±5%, unless otherwise specified

Symbol	Parameter	Min.	Typ	Max.	Unit	Conditions
VIH	Input High Voltage	2.0		VCC	V	
VIL	Input Low Voltage	–0.3		0.8	V	
IIN	Input Leakage Current R/–W, RES, RS, CS, LPSTB, CCLK,Ø2			±2.5	µA	
ITSI	Input Leakage Current for Three-State Off DB0 - DB7			±10	µA	VIN = 0.4 V to 2.4 V VCC = 5.25 V
VOH	Output High Voltage ILOAD = –205 µA (DB0 - DB7) ILOAD = –100 µA (All Others)	2.4			V	
VOL	Output Low Voltage ILOAD = 1.6 mA			0.4	V	
ICC	Input Power Supply Current			4.0	mA/MHz	
CI	Input Capacitance Ø2, R/–W, RES, CS, RS, LPSTB, CLK DB0 - DB7			10.0 12.5	pF pF	
CO	Output Capacitance			10.0	pF	