DIGITAL DESIGN

Central Processing Unit (CPU)

Arithmetic/ Logic

Data, information → Input

Control

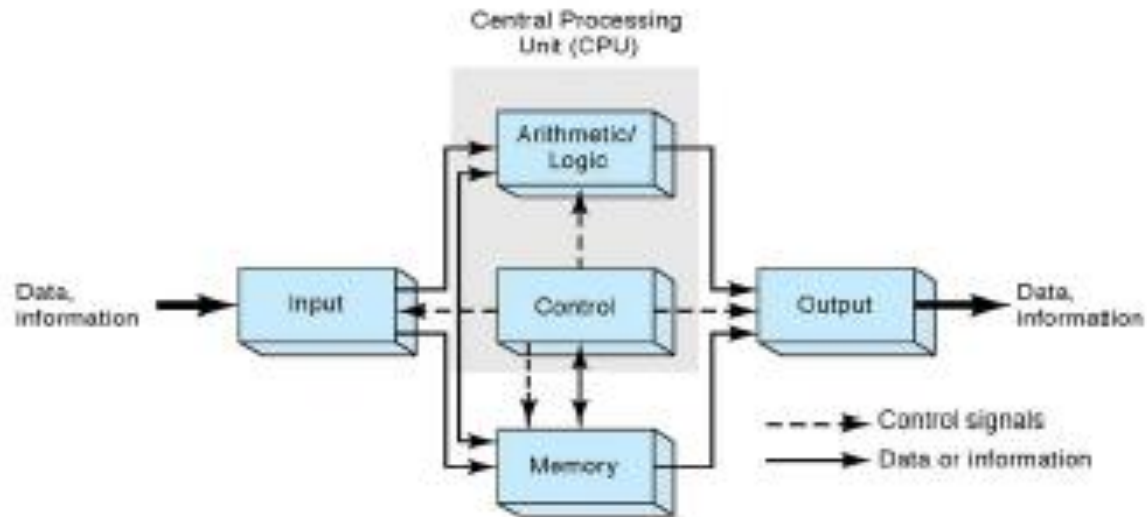Output → Data, information
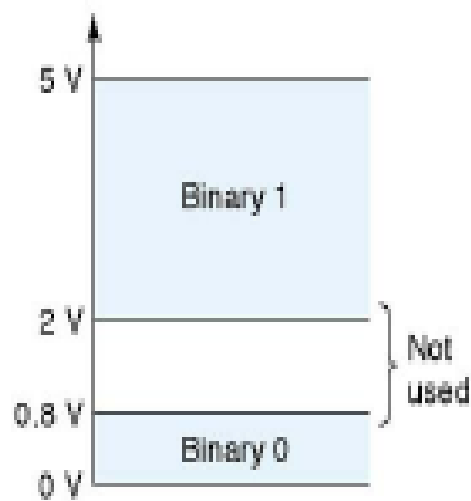
Memory

- - - → Control signals
——→ Data or information

SIGNALS
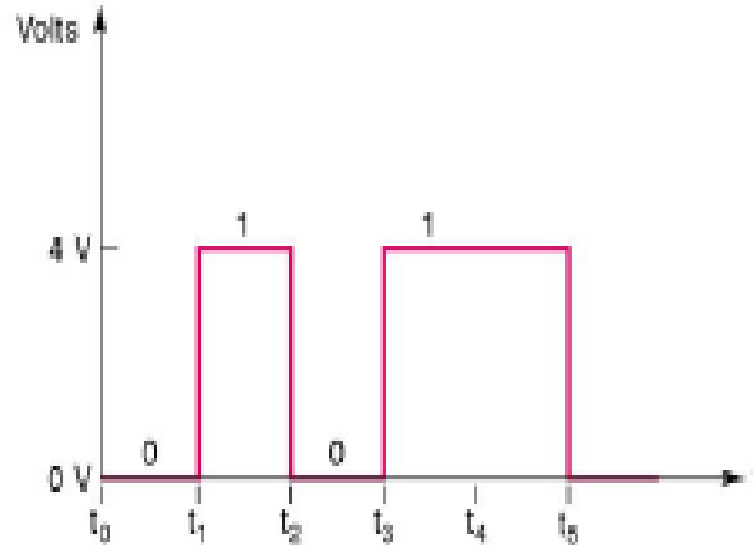
-Continuous

-Discrete

SYSTEMS

-Analog

-Digital

(a) Typical voltage assignments in digital systems

(b) Typical digital signal timing diagram

ADVANTAGES OF DIGITAL SYSTEMS

- Reproducibility of results
- Ease of design
- Programmability
- Speed
- Cost
- Integrated Circuits

DIGITAL CIRCUITS

- COMBINATIONAL

(Outputs depend only on present inputs)

-SEQUENTIAL

(Depends on present & Previous inputs)

Involve timing and memory elements

An Example: To interpret level in a Water tank

Analog System

- **Float to give analog input**

- **Analog Processing (I = V/R)**

- **Analog Output**

Digital System

- **Float to give analog input**

- **A/D converter**

- **Processing (CPU and memory)**

- **Output (Digital Display)**

Ex: Speed control of DC Servo motor in HDD

Processing elements in Digital Systems

- Arithmetic circuits, decoders, encoders, multiplexers, demultiplexers

Storage Elements

- Flip flops, RAM, ROM, PLDs, Registers, Counters

Display elements

LEDs, LCDs

In this course :

- **Combinational circuit design** (Arithmetic circuits, Decoders, Encoders, MUX, DeMUX)

- **Sequential circuit design** (FFs, Synchronous & Asynchronous Circuits)

- **Digital ICs and their characteristics** (TTL, CMOS)

- **Memories , PLDs & FPGAs**

- **Basics of HDL** (Simulation & Synthesis Basics)

- **Computer Organization** (Modular Approach of CPU Design)

Lab Sessions:

Implementation of Boolean Functions
4-bit counter
Adders & Subtractors
BCD Adder
Decoders, MUX & DeMUX
Latches & FFs
Comparators & ALU
Counters & Shift Registers
Memories & FPGAs

* Take Home Assignments using HDLs

EVALUATION COMPONENTS

	MM
MID SEM TEST	100
ASSIGNMENTS (Tutorials)	40
LAB COMPONENTS	40
COMPREHENSIVE EXAMINATION	120

INTEGRATED CIRCUITS

- **LINEAR**

- **DIGITAL**

LEVELS OF INTEGRATION

- SSI

- MSI

- LSI

- VLSI

Digital IC LOGIC FAMILIES

- **RTL, DTL**

- **TTL**

- **ECL**

- **NMOS, PMOS**

- **CMOS**

IC CHARACTERSTICS

- **Fan Out**

- **Propagation Delay**

- **Noise Margin**
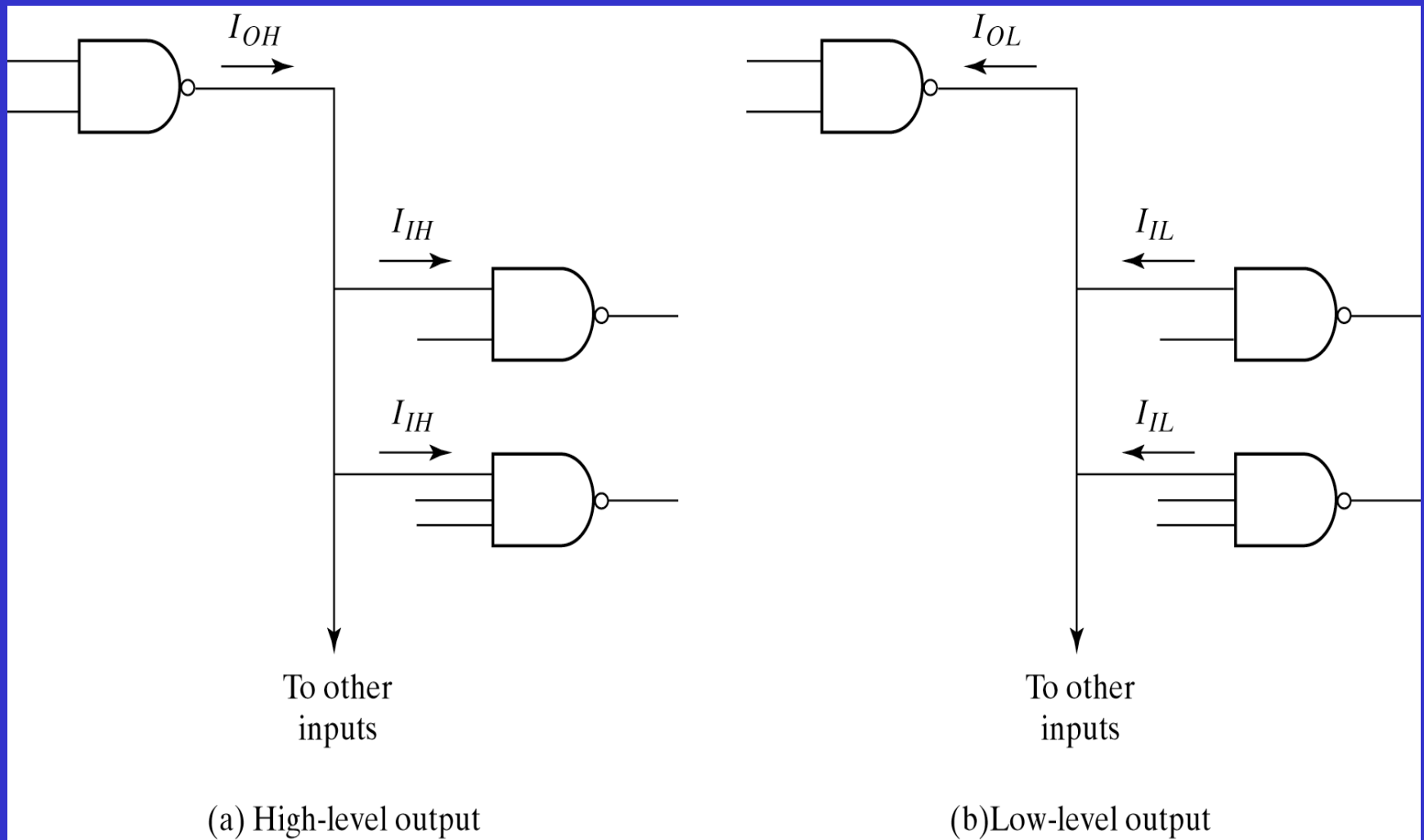
- **Power Dissipation**

Fig. 10-3 Fan-Out Computation

For TTL logic family

I_{IH}=40 microamps

I_{OH}=400 microamps

I_{OL}=16 ma

I_{IL}=1.6 ma

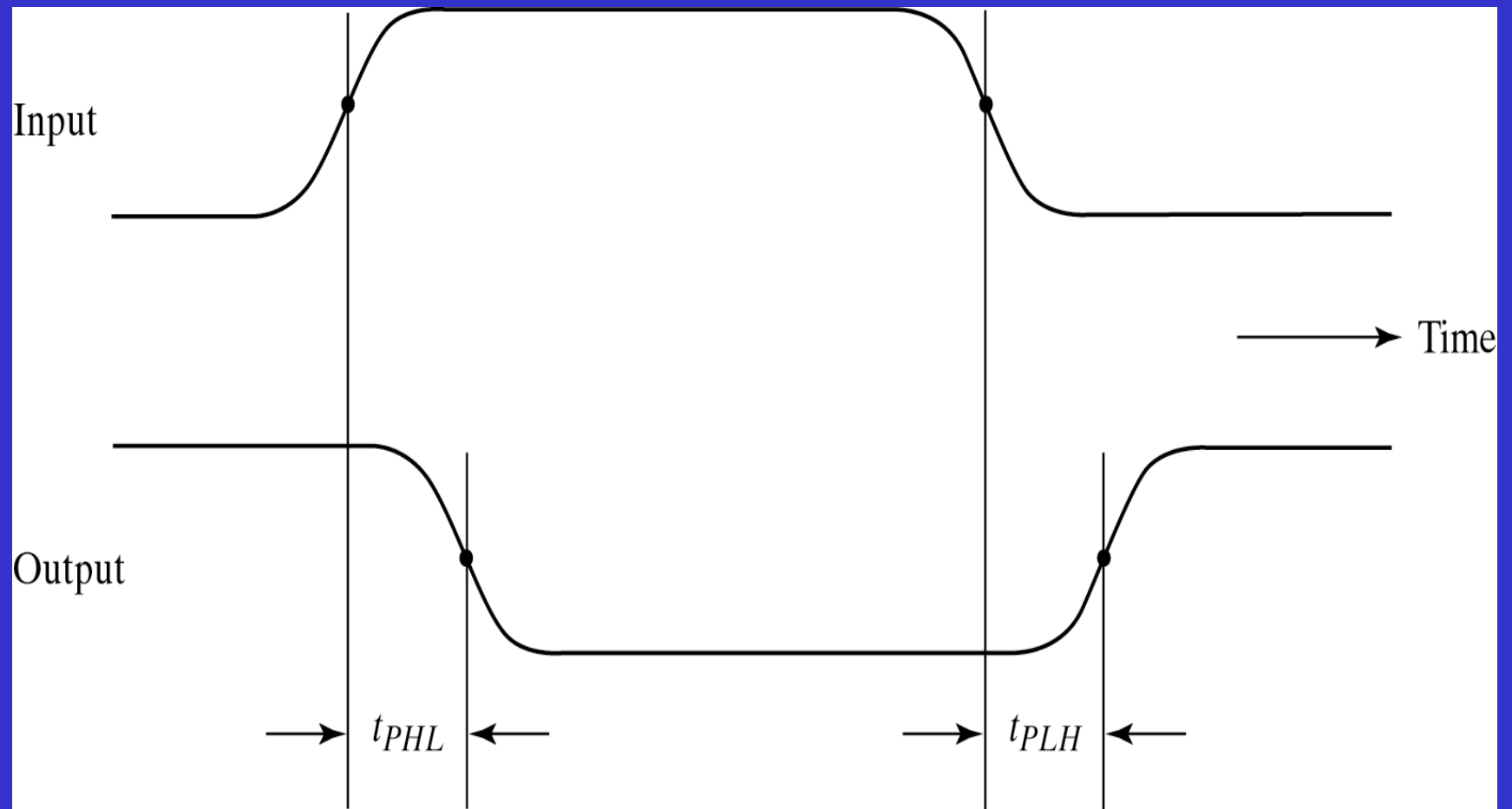Fanout = I_{OH} /I_{IH} OR I_{OL} /I_{IL} = 10

Fig. 10-4 Measurement of Propagation Delay

For TTL logic family

TPHL= 7 ns

TPLH= 11 ns

Depends on loading of gate

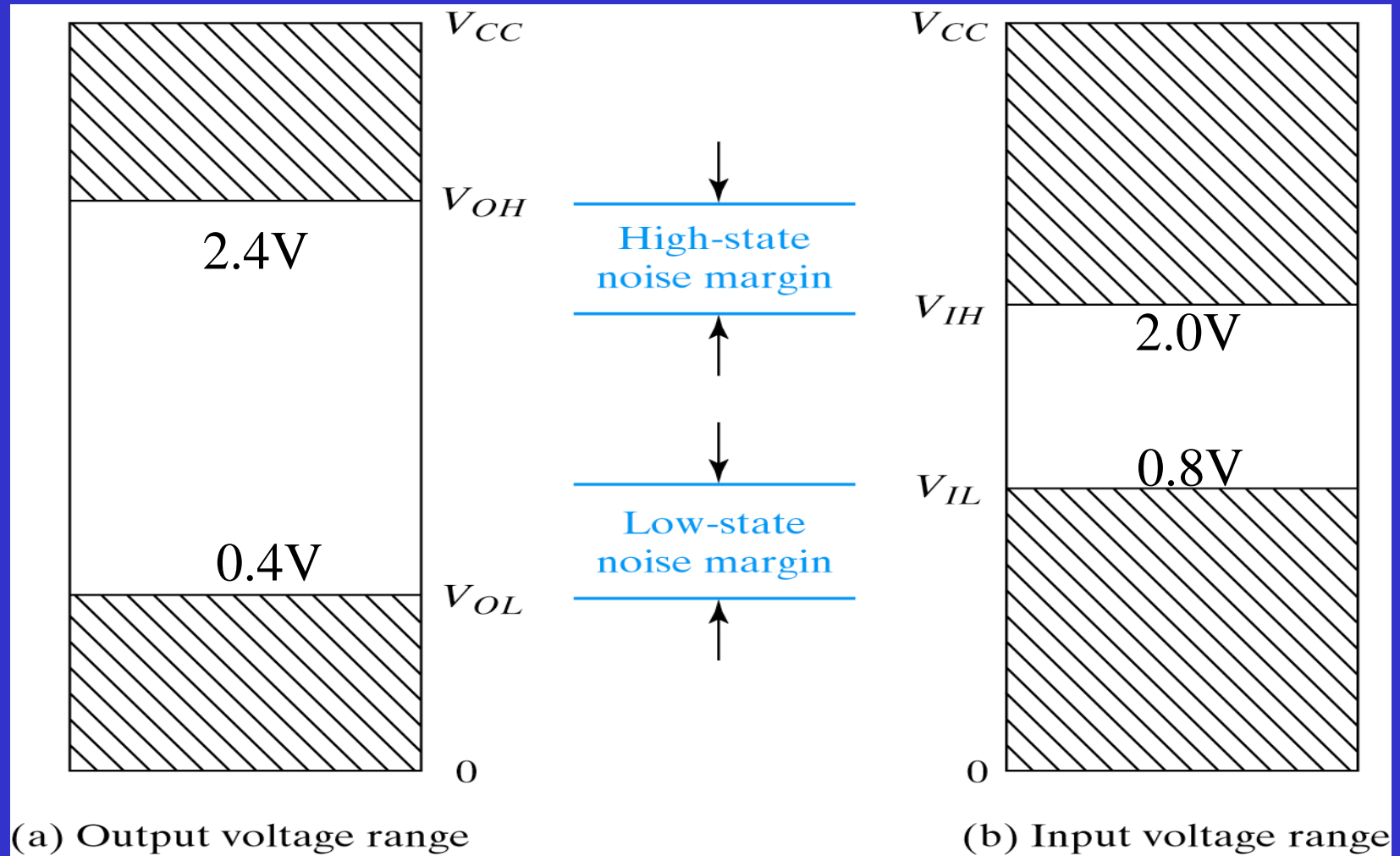Fig. 10-5 Signals for Evaluating Noise Margin

(a) Output voltage range

(b) Input voltage range

2.4V

0.4V

2.0V

0.8V

V_{CC}

V_{OH}

High-state noise margin

V_{OL}

Low-state noise margin

V_{CC}

V_{IH}

V_{IL}

Power Dissipation (P_D)

- **Expressed in Milliwatts**

- **PD= V_{CC} * I_{CC}**

- **$I_{CC}(avg)=(I_{CCH}+I_{CCL})/2$**

- **10mw for TTL NAND gate**

Do you Know ?

- Excess – 3 Code
- Gray Code
- Maxterm
- Minterm
- Canonical form