BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
CS/EEE/INSTR F215 Digital Design
I Semester 2012-13
Mid Semester Test (Closed Book)

03-10-2012 **MM: 100** **Duration: 90 minutes.**

Note: Attempt all parts of a question together

Q1. (a) For the Boolean expression given below

$F(A,B,C,D) = \Sigma (2,3,6,7,9,11,13,15)$

$d(A,B,C,D) = \Sigma (0,4,5)$

(i) Plot the k-Map
(ii) Identify the Prime Implicants
(iii) Identify the essential Prime Implicants
(iv) Obtain the minimal SOP for F
(v) How many different minimal SOPs are possible for F

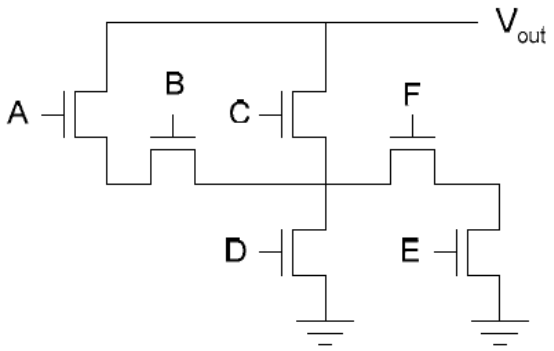
(b) (i) Find the compliment of the Boolean expression (AB'+C)D' + E
(ii) Represent the decimal number 6027 in excess-3 code, 2421 code

[12+5]

Q2. A logic circuit has two 2-bit binary numbers (X_2X_1 and Y_2Y_1) as inputs and a 2-bit binary number (W_2W_1) as output. The output represents the count of number of EVEN numbers in the input (Number zero at input is taken as even).
Design the above logic circuit using minimum number of gates. You can use only among the following gates for your design: EXOR, AND, NOR.

[15]

Q3. (i) Draw the transistor level implementation of a two input EXNOR gate. Use minimum number of transistors. Assume that complimentary inputs are NOT available.
(ii) Draw the corresponding pull-up network for the circuit given below. Also write the Boolean expression for the output. [9+9]



Q4. (a) Using a positive edge triggered JK flip-flop and required logic gates design a flip- flop called AB flip-flop whose characteristic table is as given below. (A and B are the inputs and Q is the output). Also write the characteristic equation of the AB Flip Flop

A	B	Q(t+1)
0	0	0
0	1	Q'(t)
1	0	Q(t)
1	1	1

(b) A D Flip Flop is made of 6 NAND gates having a delay of 7ns each. What are the hold and setup times for the Flip Flop? [10+2]

Q5. (i) For the open collector TTL circuit shown below assume R_L= 4 K, and h_{fe} of all three transistors to be 5. If the inputs ABC are all connected to 1V find the base currents for Q1, Q2 and Q3.

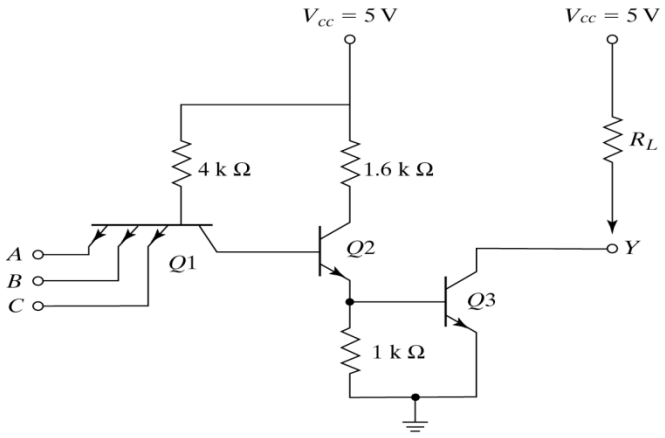


Fig. 10-11 Open-Collector TTL Gate

(ii) Using minimum number of transmission gates implement the function F= (A+B)C

[9+9]

Q6. (a) What is the main advantage of using the BiQuinary code?
(b) Using Quine-McCluskey method, find all essential prime implicants for the function f(A,B,C,D) = $\sum$ (0,1,2,5,6,7,8,9,10,14). Also find the minimsed SOP form. Show all steps.
(c) An Eight bit full adder is made of gates with a delay of 9ns. How much time does it take for the result to be produced if the adder is (i) Ripple (ii) Carry look ahead
(d) Implement F= AB'+AC'+DC+ AD using ONLY minimum number of Half Adders. Assume complements of inputs are not available.

[3+8+3+6]