BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
II SEMESTER 2013-2014
EEE/CS/INSTR F241 MICROPROCESSOR PROGRAMMING AND INTERFACING
QUIZ #1 (OPEN BOOK)

MARKS:10 **29-01-2014** **DURATION: 30 MIN**

	SOLUTIONS	

Note: Each question carries two marks.

Q1. Compute the overall CPI and MIPS (million instructions per second or rate of instruction execution per unit time) for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz. Total number of instructions executed by machine A are 100.

Instruction category	Percentage of occurrence	No of cycles per instruction
ALU	38	1
Load and Store	15	3
Branch	42	4
Others	5	5

Sol. Overall CPI $= \frac{\Sigma^{n}_{i=1} CPI_i \times I_i}{\text{Inst Count}} = \frac{38x1+15x3+42x4+5x5}{100} = 2.76$ **1 M**

$$MIPS = \frac{\text{Clock Rate}}{\text{Overall CPI} \times 10^6} = \frac{200 \times 10^6}{2.76 \times 10^6} = 72.46$$ **1 M**

Q2. A programmer wants to store the following sets of data of variable size into the memory, starting with data1, then data2 and then data3. He loads DS=FF00H and BX=3000H. Compute the physical address of each data and show the memory contents of the data segment in the following table. Write 'X' if the data to be written in memory is unknown.

Data1(byte size): 23H
Data2 (word size or two bytes): 42H
Data3 (double word size or four bytes): 64H

0.25 M each for correct address+data

Physical address	**02000H**	**02001H**	**02002H**	**02003H**	**02004H**	**02005H**	**02006H**	**02007H**
Data	**23H**	**42H**	**00H**	**64H**	**00H**	**00H**	**00H**	**X**

Q3. Identify the addressing mode for the following instructions.

(a) MOV [EAX+EBX], CL
(b) MOV BX, 5678H
(c) MOV AX,[ECX+4]
(d) MOV EBX,[EAX+8*ECX]

Sol (a) Base plus Index Addressing 0.50 M each
(b) Immediate Addressing
(c) Register Relative Addressing
(d) Scaled Index Addressing

Q4. Write the machine code in hex for the following instructions(for 8086):

(a) MOV [BP],DL
(b) MOV WORD PTR [BX+1234H],3456H – (WORD PTR is an assembler directive which ensures that two memory locations are used to store the immediate number)

Sol (a) 885600_H 1 M each
(b) $C78734125634_H$

Q5. For an 80386 (having 32-bit registers and using 32-bit address lines can address 4GB of memory), is operated in real mode of operation and the following instruction is executed:

MOV EAX, [ECX]

The register values are DS=2000H, ECX=12345H. What is the physical address generated (if any)? Can this instruction cause the system/assembler to hang? Why?

1 M

Sol. <u>No physical address would be generated</u>. The system/assembler will hang/close or indicate an addressing error because in the real mode of operation, the offset size, given by ECX register in this case can not be greater than $FFFF_H$ even if it is 80386 and above. Only the rightmost 16 bits of the extended register address a location within the memory segment.

1 M for justification