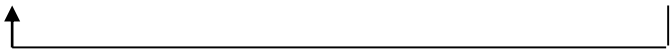
Q. To Detect the sequence ‘111’ from a binary stream (non-overlapping). When the sequence is detected an output will be made as a logic ‘1’ for one clock pulse.The state diagram for the design is as given below. Treat the unused state as a don’t’care condition. Design the circuit using 7474 and 7408 ICs. To test the circuit keep the input at logic 1 and apply a 1kHz clock pulse at the clock input and verify the output using a CRO.

Q. Design a synchronous sequential circuit only using JK FFs(7476) whose state transition is as given below. Verify your operation using a 4kHz clock pulse and showing the waveform at MSB and LSB of the counter.

00-00-00-00-01-01-01-01-10-10-10-10-11-11-11-11



Q. Assume that a *T* flip-flop is available. Construct a *D* flip-flop using a *T* flip-flop and one or more logic gates. Using this *D* flip-flop, construct a Divide-by-2 circuit.

Note: You are provided with a *JK* flip-flop.