BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
CS/EEE/INSTR F215 Digital Design
I Semester 2013-14
Mid Semester Test (Closed Book)

03-10-2013 **MM: 100** **Duration: 90 minutes.**

Note: Attempt all parts of a question together

Q1. (a) For the Boolean expression given below

$F(A,B,C,D) = \Sigma (0,1,2,5,6,7)$

$d(A,B,C,D) = \Sigma (8,9,10,11,12,14,15)$

(i) Plot the k-Map
(ii) Identify the Prime Implicants. Express each PI as product form.
(iii) Identify the essential Prime Implicants. Express each EPI as product form.
(iv) How many different minimal SOPs are possible for F and write down the expression for all the possible expressions.

(b) Find the complement of F(A,B,C,D)= AB+((BC)'(A+D)')

[22+5]

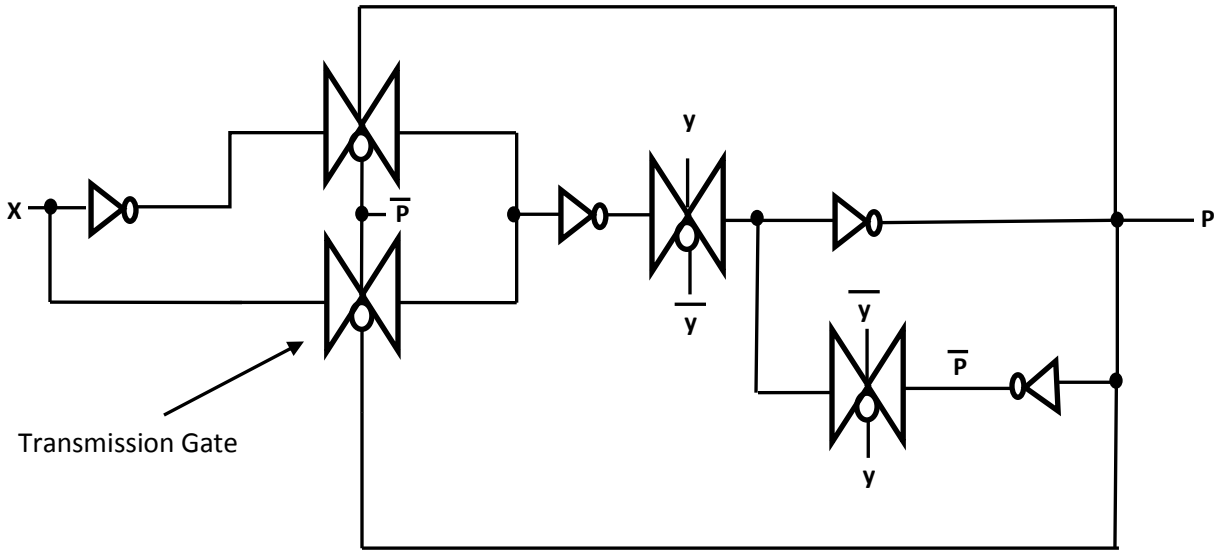
Q2. (a) Implement the function F(A,B,C,D,E) = A'B'C'DE'+ABCD'E only using the required components from the following list:

1. 3:8 decoder with active high outputs and an active high enable input -1 No.
2. 8:3 Priority Encoder with input no. 7 at highest priority with one active high enable which if disabled forces the outputs to logic low – 1 No.
3. 2 input XOR gate – 1 No., 2 input OR gate – 1 No., 2 input AND gate – 1 No.

(b) Design a digital circuit which has a three bit input A2A1A0 and three bit output Y2Y1Y0 to perform the following function:
The circuit takes the input A2A1A0 and produces the one's complement of the input number. This is followed by producing the Gray code of the ones complement output. The gray code is the final output, Y2Y1Y0, of the circuit.
Design the circuit only using not more than 5nos of 2:1 MUXs. [14+14]

Q3. (a) Construct the following using D Flip Flops and basic logic gates:
(i) T Flip Flop (ii) JK Flip Flop

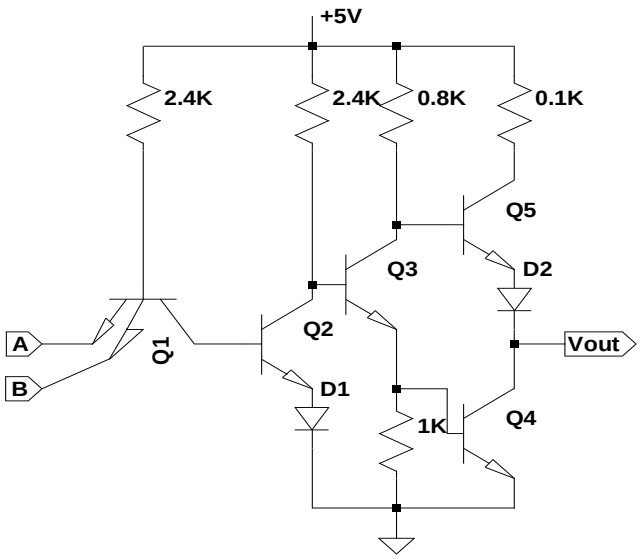
(b) Identify the function implemented by the circuit using transmission gates and inverters as shown below. Write the characteristic table and characteristic equation for the function. [10+13]



Q4. (a) For the TTL circuit shown in figure:

a) Find the logical function of the gate and the states of all transistors and diodes for all input combinations.
b) Find V_{OL}, V_{IL}, V_{IH} and low state noise margin.

Given: $V_{BE(ON)} = 0.7$ V, $V_{BE(SAT)} = 0.8$ V, $V_{CE(SAT)} = 0.2$ V, $V_{BE(OFF/REV)} = V_{D(OFF/REV)} = 0.5$ V, $V_{D(ON)} = V_{BC(ON)} = 0.7$ V



Q4 (b) Implement the following Boolean function using CMOS logic using minimum no of MOS Transistors.

$$Y = \overline{(F\,[A(B + DE) + C\,(E + BD)])}$$

[10+12]