

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
II SEMESTER 2015-2016
EEE/CS/INSTR F241 MICROPROCESSOR PROGRAMMING AND INTERFACING
Comprehensive Exam: Part-A (Closed BOOK)
06-05-2016

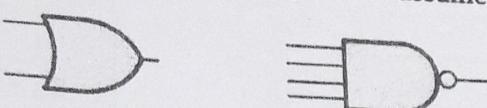
DURATION: 60min

M.M: 40

Note: Attempt all the questions in the separate answer sheet provided. Please start each question on a fresh page. Subparts of a question has to be attempted at the same place.

- Q1. Design an 8086 based system with the following memory requirement.
- 64K bytes of ROM with the following starting address map: F0000H
 - 64K bytes of RAM1 with the following starting address map: D0000H
 - 64K bytes of RAM2 with the following starting address map: E0000H

Note: Following components are provided: RAM 32Kb chips-- 4Nos, ROM 32Kb chips-- 2Nos. For address decoding you can only use the following components: 4 Input NAND gate - 3 Nos, 2 Input OR gate: 6 Nos, Not gate-- 2 Nos, as shown below, you can assume BHE', MEMR', MEMW' are readily available for interfacing.



- (i). Write the entire range (memory map) of RAM/ROM addresses using the given format ?

Memory Type	Hex Address Range	Binary Address

- (ii). Now, draw the complete labelled memory interfacing diagram using absolute addressing using given components. [6+12=18M]

- Q2. Will the following piece of code generate the overflow flag? Justify.

```
MOV AL,70H
MOV BL,60H
ADD AL,BL
```

[3M]

- Q3. Write a set of instructions to generate a square wave of 1KHz frequency on OUT 1 pin of 8253/54. Assume CLK1 frequency is 1MHz and address for control register = 0BH, counter 0 = 05H, counter 1 = 07H and counter 2 = 09H. [6M]

- Q4. Identify, which of the following are valid instructions in 8086 processors. In case if the instruction is invalid mention the reason briefly.

- a. ROL [AX], CL
- b. XCHG [DL], 80H
- c. POP AL
- d. INC BP
- e. JMP 5B00H:2AC0H

[1X5=5M]

- Q5. How does a PCI bus distinguish between a Memory Read or Memory Write operation? [3M]

Q6. Answer this question assuming that the different parts are completely independent. For each part assume that AX contains 5F9CH to start with and determine AX after executing the instruction in hex

a) CMP AX, BX

AX:

b) SUB AL, AH

AX:

c) ROR AH, 3

AX:

d) SAL AL, 4

AX:

e) MOVSX AX, AL

AX:

[1x5=5M]

*****END*****

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II SEMESTER 2015-2016
EEE/CS/INSTR F241 MICROPROCESSOR PROGRAMMING AND INTERFACING
Comprehensive Exam: Part-B (OPEN BOOK)
06-05-2016

M.M:80

DURATION: 120Min.

Note:

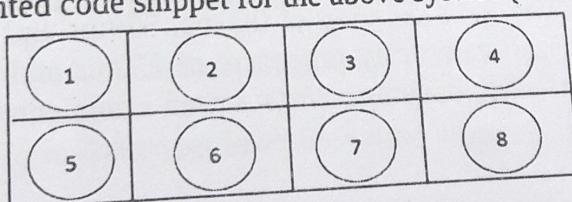
- Q1. For an 80286 microprocessor in protected mode of operation, a logical memory address is described by segment selector:offset as 002Dh:0010h. Also, GDTR = 000000h and LDTR = 0010h. Answer following question by referring to the GDT and LDT as given below.
1. Which table will contain the descriptor for this selector?
 2. Write the 8 Byte descriptor for this selector, LSB First?
 3. What will be the physical address corresponding to this logical address?
 4. Which segment (CS/DS/SS) is represented by this descriptor?
 5. What will be instruction mode (16/32 bit) for this descriptor?

[2+3+3+2+2=12M]

GDT	00 01 02 03 04 05 06 07
000038h	FE 00 00 01 FF D3 00 00
000030h	FF 01 00 00 20 D2 00 00
000028h	01 00 00 F0 11 E1 00 00
000020h	A0 00 00 AA 01 D2 00 00
000018h	D0 00 01 01 01 D2 00 00
000010h	FF FF 00 01 00 93 00 00
000008h	FF FF 00 00 00 D1 00 00
000000h	A4 01 00 FF FF D2 00 00

LDT	00 01 02 03 04 05 06 07
0140h	FF FF 00 00 00 D1 00 00
0138h	FE 00 00 01 FF D3 00 00
0130h	01 00 00 F0 11 E1 00 00
0128h	FF FF 00 00 4A 1E OF 00
0120h	FF 00 00 00 80 1E 00 00
0118h	A0 00 00 AA 01 1E 00 00
0110h	A4 01 00 FF FF D2 00 00
0108h	80 01 00 00 FF D2 00 00
0100h	FF FF 00 00 01 D2 OF 00

- Q2. There are 8 parking lots in an apartment each can accommodate only one car at a time. Each slot is provided with an optical detector which senses the presence/absence of a car. If the slot is vacant the sensor produces a logic high as the output and a logic low when the slot is occupied. A parking assistance system is to be developed using 8086 and 8255 (only one 8255 is available). The optical sensor signals are bundled into an eight bit bus (signals are compatible with 8086). A display board at the entrance of the apartment (has one indicator for each slot, see fig. below) turns on a GREEN LED for a vacancy in the slot and a RED LED for an occupied slot. Use a base address of 70H.
- (i). Show complete interfacing diagram with all necessary signals. [8+6= 14M]
- (ii). Write a well commented code snippet for the above system (use hex-decimal number system)



Q3. The root directory entry is given below:

43 4F 4D 50 52 45 45 58- 4E 45 54 16 18 7B BD 4D
4A 3A 4A 3A 00 00 BD BA-AB AA FD 01 80 36 00 00

1. Write the size of the file.
2. Write name with extension
3. Write File Attributes
4. The time of file modification
5. The date of file modification
6. The starting cluster number

[2+2+2+2+2+2= 12M]

Q4. If the cluster chain of the file is following

Cluster number	0	1	2	3	4	5	6	7	8	9	A	B	C	D
Next cluster member	FF1	FF6	004	009	008	003	006	FFF	00A	004	00B	FFF	011	FFF
Cluster number	E	F	10	11	12	13								
Next cluster member	FFF	FFF	FFF	FFF	FFF	FFF								

[3+3+3+3+2= 14M]

(A). What will be the FAT-12 entry for the above cluster chain?

(B). The Boot Sector of a storage device is the following:
 EB 3C 90 2A 60 59 60 48 - 49 43 0A 00 40 04 01 00
 02 10 01 00 AF F0 09 00 - 0A 00 01 00 00 00 00 00

- (i). What is the size of each sector?
- (ii). What is the number of sectors per cluster?
- (iii). What is the number of root directory entries?
- (iv). What is the number of sectors on disk?

Q5. (i). Write an instruction sequence (ALP snippet) that will cause the priority of an 8259, whose even address is 08H to be IR5, IR6, IR7, IR0, IR1, IR2, IR3, IR4. Solve this problem when the current priority is IR1. Write all the control words in the write sequence. Don't use repetitive rotation commands to change priority and use hex-decimal number system

(ii). Now, repeat the above for IR7

[8M]

(iii). Assuming 16-bit Intel instructions translate (a) from machine to assembly code and (b) translate from assembly code to machine code.

- a) 8AF3H
- b) MOV [SI], AH

[3+3=6M]

Q6. Using 8254 play "Happy Birthday" music. This has to be achieved by playing the notes D3(147Hz), A3(220Hz), A4(440Hz) for a duration of 250ms, 500ms and 500ms respectively. Given input frequency F = 1.1931MHz, software delay procedure of 250ms and base address is 40H. Now, draw the complete labelled interfacing diagram. Write a well commented code & use hex-decimal number system.

[14M]