

Date: 04/5/2013 (FN)

- Bulk of NMOS connected to ground and bulk of PMOS connected to  $V_{DD}$ .
  - Specify your assumptions. Justify your answers. Unless specified, assume all MOSFET are biased in saturation region
  - Label your sketches properly. All symbols have usual meaning
  - *Unless Given specifically, Take :-  $V_{DD} = 3.3V$ ,*
  - For NMOS device ( $\mu_nC_{ox} = 140 \text{ } \mu\text{A/V}^2$ ,  $V_T = 0.7 \text{ V}$ ,  $\lambda = 0.1 \text{ V}^{-1}$ ) and for PMOS device ( $\mu_pC_{ox} = 40 \text{ } \mu\text{A/V}^2$ ,  $V_T = -0.8 \text{ V}$ ,  $\lambda = 0.2 \text{ V}^{-1}$ ).
  - All parts of the same question should be done together. Marks will be deducted for wrong units. Your answers must be justified with proper reasons.

**Q1(A):** For the circuit shown in figure 1,  $|V_A| = 100 \text{ V}$  and  $V_{CE(\text{Sat})} = 0.2 \text{ V}$  (for all transistors),  $I_{REF} = 100 \mu\text{A}$ , transistors Q3, Q4, Q5 and Q6 has  $\beta = \infty$ , while transistors Q1 and Q2 have  $\beta = 100$ ,  $C_L = 1\text{pF}$ ,  $R_o = 10 \text{ K}\Omega$ .

- $R_{sig} = 10 \text{ k}\Omega$ .

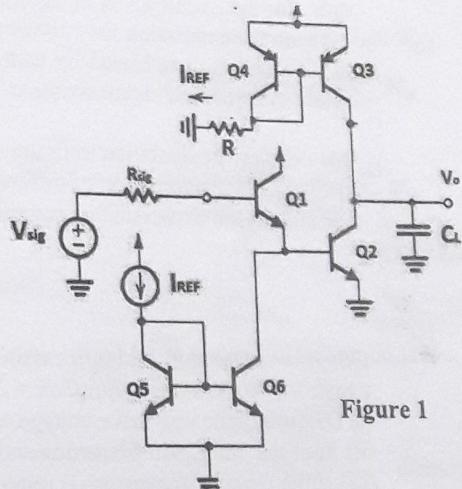
  - Find  $R_{in}$  seen at the base of transistor Q1.
  - Find the low frequency gain ( $V_o/V_{sig}$ ).
  - Find upper and lower voltage swing at  $V_o$ .

$$(3+3+2=8M)$$

Q1(B): (i) For the circuit shown in figure 2, find  $I_{o1}$  and  $I_{o2}$  in terms of  $I_{DSS}$ . Assume all transistors are matched.

- (ii) Use this idea to design a circuit that generates currents of 1 mA, 2 mA, and 4 mA using a reference current source of 7 mA assuming  $\beta = \infty$ . What are the actual values of the currents generated for  $\beta = 50$ ?

$$(3+3+3=9M)$$



**Figure 1**

Q1(C): For the circuit shown in figure 3 assume that for the BJTs  $\beta = 100$  and  $|V_A| = 100$  V,  $|V_{BE}| = 0.7$  V and MOSFET has  $W/L=14.3$ , also  $I = 100 \mu\text{A}$  and  $V_{BIAS} = +1$  V. Assume that the output resistance of current source  $I$  is equal to the output resistance of its connected circuit and current-source  $2I$  is ideal. For this circuit, calculate:

- (i) The voltage at the node between  $Q_1$  and  $Q_2$ .
  - (ii)  $g_m$  and  $r_o$  for each device.
  - (iii) The maximum allowable value of  $v_o$ .
  - (iv) The output resistance.
  - (v) The voltage gain. ( $v_o/v_i$ ).

$$(2+2+1+2+4=11M)$$

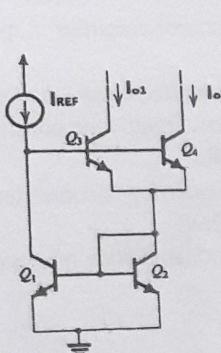
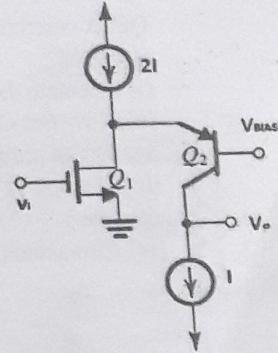


Figure 2



**Figure 3**

Q2: For the circuit given in figure 4,  $W_1=W_2=W_3=W_4=W_5=W_6=10 \mu\text{m}$ ,  $L=1 \mu\text{m}$ . (for all transistors),  $I_{REF}=50 \mu\text{A}$ , (Assume:  $\gamma=0$ )

- Q2: For the circuit given in figure 4.  $W_1=W_2=W_3=W_4=W_5=W_6=1 \mu A$

  - Calculate equivalent transconductance ( $G_m$ ), output resistance ( $R_{out}$ )
  - Calculate voltage gain ( $v_{out}/v_{in}$ ).
  - Also calculate upper and lower signal swing.
  - If  $V_{in}$  and  $V_b$  are interchanged than find expression for voltage gain ( $v_{out}/v_{in}$ ) intuitively.

$$(4+2+2+3=11\text{M})$$

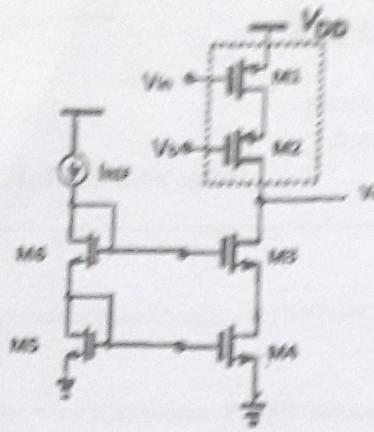


Figure 4

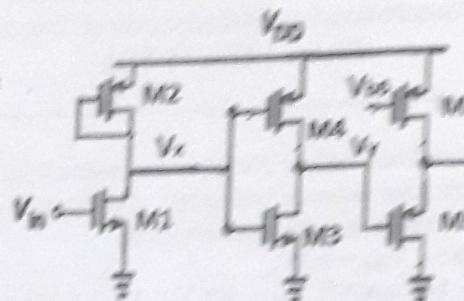


Figure 5

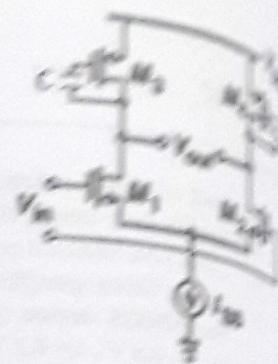


Figure 6

Q3: For the circuit given in figure 5, (Assume:  $\gamma=0$ ,  $V_{DD}=1.8$  V,  $|V_{out}|=|V_{in}|$ )

- Find the expression for voltage gain ( $v_{out}/v_y$ ), ( $v_x/v_y$ ), ( $v_x/v_{in}$ ).
- If this circuit is biased by using an appropriate dc source at  $V_{in}$ , then find the value dc bias voltage  $V_x$  to obtain symmetrical signal swing at  $V_x$ . Also calculate upper and lower signal swing at  $V_x$ .

(6+4+10)

Q4: For the circuit shown in figure 6.

- Find out the expression of differential voltage gain ( $A_d$ ) (intuitively) at very low and high frequency.
- Find out the expression of common mode gain ( $A_{CM}$ ) (intuitively) at very low and high frequency.

(3+3+10)

Q5: It is required to design a cascode amplifier to provide a dc voltage gain of 66 dB and utilizing NMOS transistors which  $V_A=10$  V,  $W/L=10$ ,  $\mu_nC_{ox} = 200 \mu\text{A/V}^2$ ,  $C_{gd}=0.1 \text{ pF}$ ,  $C_L=1 \text{ pF}$ . Assuming that  $R_L=R_{out}$

- Determine the overdrive voltage and drain current at which the MOSFETs should be operated. Neglect the body effect.
- Find the unity gain frequency and 3-db frequency.
- If the cascode transistors are removed and  $R_L$  remains unchanged. What will the dc gain become?

Q6: A common source amplifier is specified to have  $g_m=5 \text{ mA/V}$ ,  $r_o=40 \text{ k}\Omega$ ,  $C_B=2 \text{ pF}$ ,  $C_{BS}=0.1 \text{ pF}$ ,  $C_L=1 \text{ pF}$ ,  $R_{in}=20 \text{ k}\Omega$

- Calculate the low frequency small signal voltage gain ( $A_m$ ) of this amplifier.
- Now use Open circuit time constants to estimate the -3db frequency ( $f_H$ ) of the amplifier. Hence determine the gain bandwidth product.
- If a  $500 \Omega$  resistance is connected in the source lead, find the new values of  $A_m$ ,  $f_H$  and the gain bandwidth product.
- Also sketch and label bode magnitude and phase plot for part (ii) and part (iii) considering only dominant pole.

(3+4+6+3=16)

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**Birla Institute of Technology & Science, Pilani**  
 II<sup>nd</sup> Semester 2012-13  
 EEE F244/INSR F244 Microelectronic Circuits  
 Comprehensive Examination (Open book)

Part-B

Time: 45 Min

Date: 04/5/2013

MM: 28

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- All parts of the same question should be done together. Marks will be deducted for wrong units. Your answers must be justified with proper reasons.

Q1: For the amplifier circuit shown in figure 1, Overall output voltage swing is

1.4 V and total power dissipation is 5 mW.  
 Given:  $(W/L)_{M_7} = 100$  and  $(W/L)_{M_1} = (W/L)_{M_2} = (W/L)_{M_3}$ .

- Calculate the DC bias level of the output ( $V_{out}$ ) and bias voltage  $V_{b1}$  and  $V_{b2}$ .
- Find out (W/L) ratio of transistor M1.
- What are minimum and maximum allowable input CM level.
- Calculate the voltage gain ( $V_{out}/V_{in}$ ), common-mode gain and CMRR.

(6+2+4+8=20M)

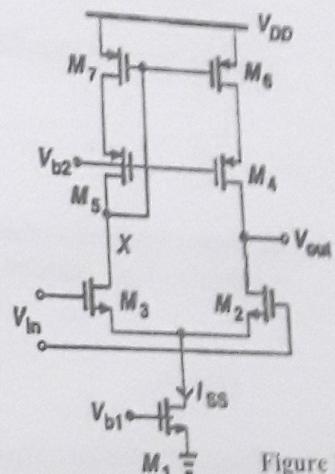


Figure 1

Q2: For the amplifier circuit shown in figure 2,  $R_{D1}=R_F=R_{S1}=R_{D2}=10K$ ,

$g_m=g_{m2}=1mA/V$ .

- Identify the type of feedback topology.
- Find feedback factor  $\beta$ .
- Find voltage gain with feedback ( $A_f=V_o/V_i$ ).
- Find output resistance with feedback ( $R_{of}$ ).

(1+2+3+2=8M)

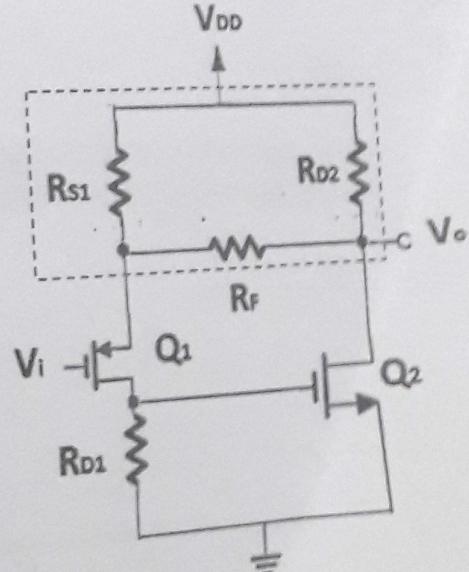


Figure 2

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