BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
II SEMESTER 2013-2014
EEE/CS/INSTR F241 MICROPROCESSOR PROGRAMMING AND INTERFACING
QUIZ #4 (OPEN BOOK)

MARKS:10 **26-02-2014** **DURATION: 30 MIN**

ID:	**NAME:**	**SEC:**

Note: Marks for each question is stated in the question.

Q1. Machine cycles can be memory read, memory write, I/O read or I/O write. For the instruction DEC Word PTR [DX], the machine cycles executed are? Please write them in the right order. **(1 mark)**

MEMR, MEMR, MEMW

Q2. DT/R' signal to the buffer is used for determining the direction of the data transfer with respect to the microprocessor. Instead of DT/R', which control signal from the microprocessor can be used for to determine direction of the data transfer?

(1 mark)

Rd'

Q3. Can the non-maskable interrupt be disabled using interrupt flag bit?

(1 mark)

no

Q4. The 8087 acquires and returns the system bus from 8086 using how many and what type of pulses? **(1 mark)**

Three Low pulses

Q5. Write the number of machine cycles the following instruction would take. The memory is byte organized. The processor in 16 bit mode of operation. State what each machine cycle represents.

(a) `Push ebx` **(2 marks)**

1 for machine code fetch
2 for storing ebx in stack

(b) `cmp [bx], ax` **(2 marks)**

1 for machine code fetch
1 for memory read

Q6. 8086 microprocessor executes 12 data transfer operation. Each data transfer requires one bus cycle. First five data transfer's bus cycle requires 5 – T states. The next 7 bus cycles require 4 - T states. If the clock of the microprocessor is 7.5 MHz, calculate the time the microprocessor takes to carry out the 12 data transfers. (Please note: The difference in number of T-cycles is due to the wait states). **(2 marks)**

Total no of clock cycles = (5 X 5)+ (7 X 4)= 53

Time for on clock cycle = $1/(7.5 \times 10^6)=0.1334 \times 10^{-6}$ seconds

Total Time = $53 \times 0.1334 \times 10^{-6} = 7.067 \times 10^{-6}$ seconds