

MM:90

Time: 1.30 Hrs

Date: 26/2/2013

- Bulk of NMOS connected to ground and bulk of PMOS connected to  $V_{DD}$ .
- Specify your assumptions. Justify your answers. Unless specified, assume all MOSFET are biased in saturation region
- Label your sketches properly. All symbols have usual meaning
- **Unless Given specifically, Take :-**  $V_{DD} = 3.3V$ ,  
**For NMOS device ( $\mu_nC_{ox} = 140 \mu A/V^2$ ,  $V_T = 0.7 V$ ,  $\square = 0.1 V^{-1}$ ) and for PMOS device ( $\mu_pC_{ox} = 40 \mu A/V^2$ ,  $V_T = -0.8 V$ ,  $\square = 0.2 V^{-1}$ ).**

**Q1:** (a) A trans-resistance amplifier model shown in figure 1 with  $R_i=20 K\Omega$ , open circuit trans-resistance gain of  $1 V/mA$  &  $R_o = 300 \Omega$  is driven by a source ' $I_s$ ' with parallel resistance  $R_s = 100 K\Omega$  and drives a load  $R_L$  of  $600 \Omega$ . Find (i) The trans-resistance gain  $V_L/I_s$  (ii) Power gain  $P_L/P_s$  (iii) What should be the open circuit trans-resistance gain to achieve resistance gain  $V_L/I_s$  of  $1 V/mA$ .  $(3+3+4=10M)$

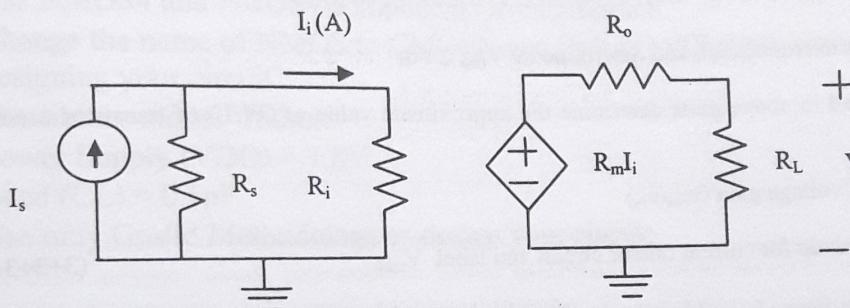


Figure 1

(b) A transconductance amplifier model having  $R_i = 4 k\Omega$ ,  $R_o = 40 K\Omega$ , and short circuit trans-resistance  $G_m = 10 mA/V$ , is driving a load resistance  $R_L$  in parallel with a capacitance  $C_L$ . (10 M)  
 i) What is the lowest value that  $R_L$  can have to obtain a dc gain of at least 40dB?  
 ii) Find out the highest value that  $C_L$  can have to obtain a 3-dB bandwidth of at least 110KHz?  $(4+4=8M)$

**Q2.**

(a) For the circuit as shown in figure 2,  $L = 1 \mu m$  and  $W = 20 \mu m$  for all the NMOS transistors. Find dc values of  $V_2$  and  $I_2$ . Also find the new value of  $I_2$  when  $W = 120 \mu m$ ? (Assume:  $\lambda = \gamma = 0$ )  $(3+3+3=9M)$

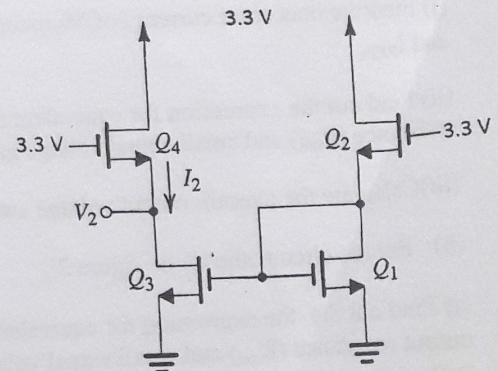


Figure 2

(b) For the circuit given in figure 3.  $W_1 = 10 \mu m$ ,  $W_2 = 1 \mu m$ ,  $L_1 = L_2 = 1 \mu m$ .  
 (i) Design a simple current mirror circuit to generate bias voltage ' $V_b$ ' as indicated in figure 3. Find component values of circuit to generate reference current.

(ii) Calculate equivalent transconductance ( $G_m$ ), output resistance ( $R_{out}$ ) and input resistance  $R_{in}$  and voltage gain ( $v_{out}/v_{in}$ ).

(iii) Identify the topology if M1 is replaced by an NMOS transistor keeping same  $W_1$  and  $L_1$  values. Calculate  $G_m$  and  $R_{out}$  of the modified structure.  $(4+7+4=15M)$

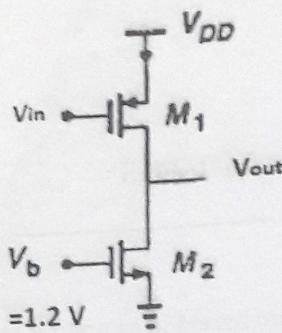


Figure 3

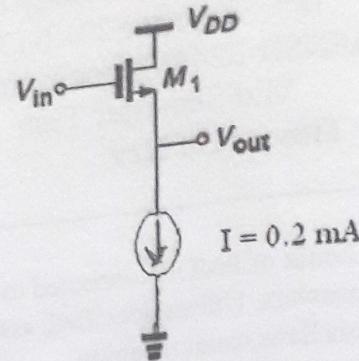


Figure 4

Figures

Q3:

(a) For the circuit shown in figure 4 'I' is implemented using a basic current mirror circuit with  $I_{ref} = 0.3 \text{ mA}$ ,  $(W/L)_{ref} = 10$ ,  $V_A = 100V$ ,  $V_{DD} = 3V$ ,  $V_m = 0.4V$ ,  $V_{ov(M1)} = 0.2V$ ,  $\mu_nCox = 140 \mu\text{A}/\text{v}^2$

(i) Draw the entire current mirror circuit, and determine its  $V_{GS}$ ,  $\lambda = 0$ .

(ii) Using values calculated in above parts determine the approximate value of  $(W/L)$  of transistor used in the mirror here take  $\lambda = 0$

(iii) Calculate small signal voltage gain ( $v_{out}/v_{in}$ )

(iv) Draw  $I$  vs.  $V$  characteristic for current mirror circuit and label  $V_{min}$ . (3+3+3=12M)

(b) For the circuit shown in figure 5 (i) Identify the circuit topology (ii) Now draw the complete small signal model amplifier circuit only (iii) Calculate  $R_{in}$ ,  $R_{out}$  for the circuit (Intuitively) (iv) Write the expression for small signal gain ( $v_{out}/v_{in}$ ). (3+3+3+3)=12M

Q4: (a) For the circuit shown in figure 6. Assume  $\lambda \neq 0$ ,  $\gamma = 0$  and,  $V_{ov}$  (for all transistors) = 0.2.

(i) Find the bias drain current  $I$  of  $M_2$  in terms of  $(W/L)_x$  ratio of transistors and  $I_{REF}$ .

(ii) Find out the expression for equivalent transconductance ( $G_m$ ), output resistance ( $R_{out}$ ) and small signal voltage gain ( $v_{out}/v_{in}$ ) intuitively.

(iii) Calculate the overall output voltage swing obtained above.

(b) For the circuit shown in figure 7.

(i) Find out the expression for equivalent transconductance ( $G_m$ ), output resistance ( $R_{out}$ ) and small signal voltage gain ( $v_{out}/v_{in}$ ). Assume  $\lambda \neq 0$ ,  $\gamma = 0$ .

(ii) Sketch small signal voltage gain  $|v_{out}/v_{in}|$  versus input bias voltage. Assume  $\lambda = 0$ ,  $\gamma = 0$

(iii) Remove transistor  $M_1$  and  $R_D$  from figure 7 and place one ideal current source between  $V_{DD}$  and  $V_{out}$ . Now find out the expression for small signal voltage gain  $v_{out}/v_{in}$ .

Part (a) (3+6+3)=12M, Part (b) (6+3+3)=12M

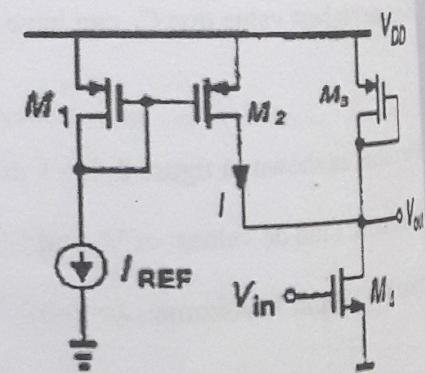
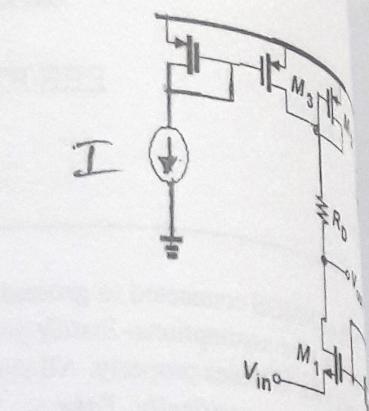


Figure 6

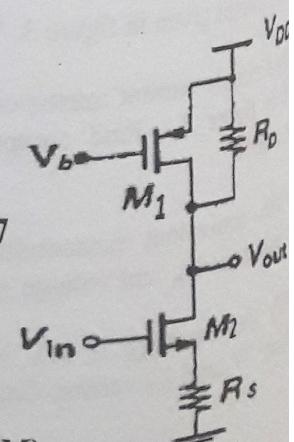


Figure 7