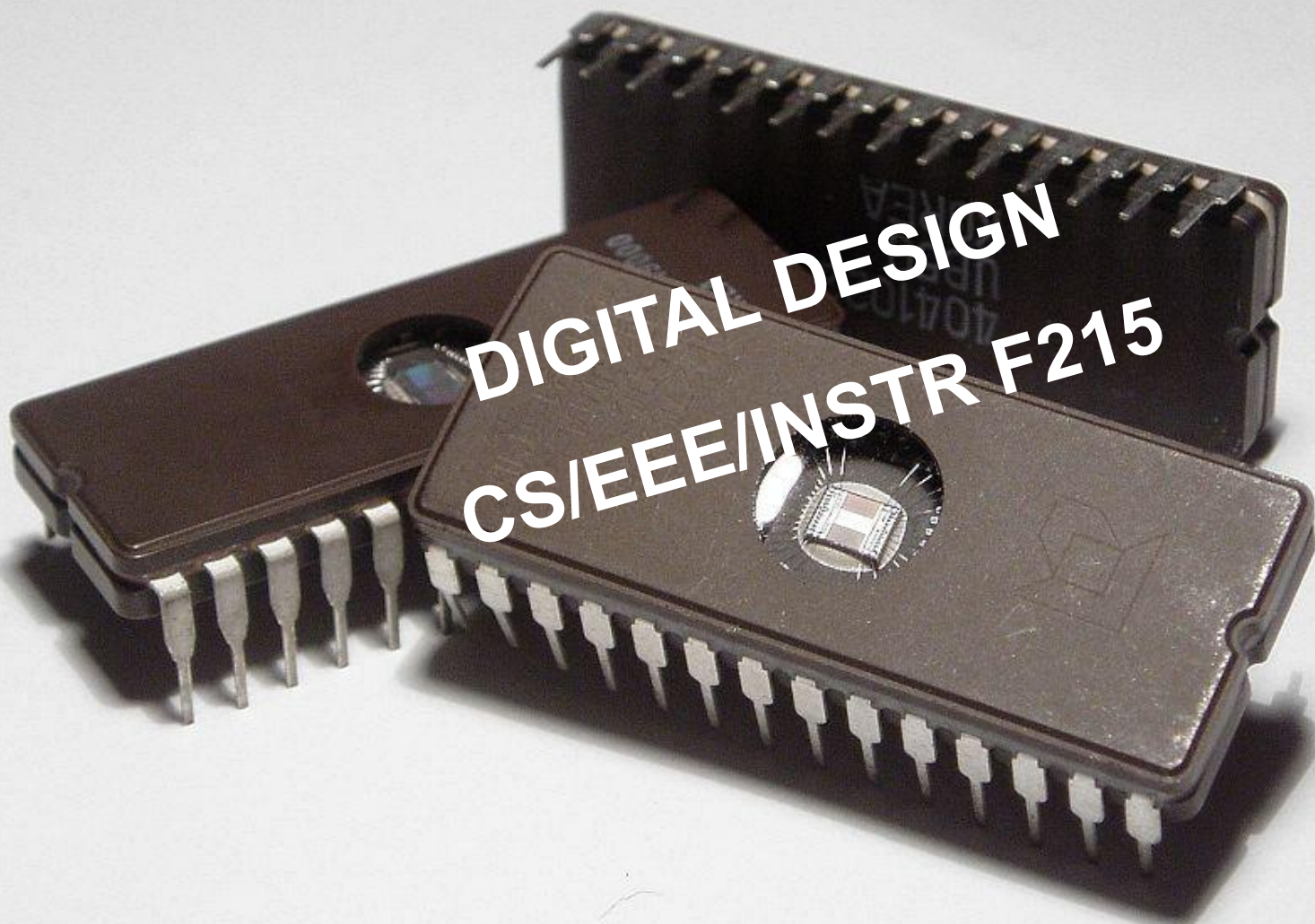


DIGITAL DESIGN
CS/EEE/INSTR F215

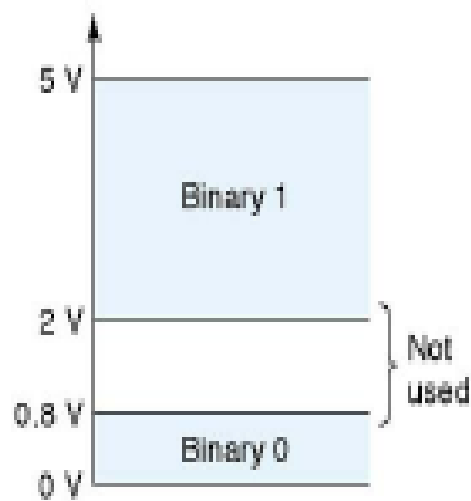


SIGNALS

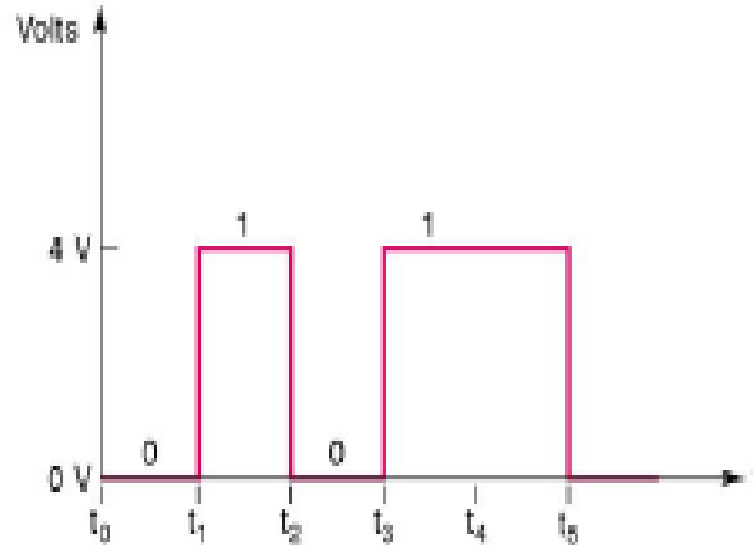
- Continuous
- Discrete

SYSTEMS

- Analog
- Digital



(a)



(b)

(a) Typical voltage assignments in digital systems

(b) Typical digital signal timing diagram

ADVANTAGES OF DIGITAL SYSTEMS

- Reproducibility of results
- Ease of design
- Programmability
- Speed
- Cost
- Integrated Circuits

DIGITAL CIRCUITS

- COMBINATIONAL

(Outputs depend only on present inputs)

- SEQUENTIAL

(Depends on present & Previous inputs)

Involve timing and memory elements

An Example: To interpret level in a Water tank

Analog System

- **Float to give analog input**
- **Analog Processing ($I = V/R$)**
- **Analog Output**

Digital System

- **Float to give analog input**
- **A/D converter**
- **Processing (CPU and memory)**
- **Output (Digital Display)**

Ex: Speed control of DC Servo motor in HDD

Processing elements in Digital Systems

- Arithmetic circuits, decoders, encoders, multiplexers, demultiplexers

Storage Elements

- Flip flops, RAM, ROM, PLDs, Registers, Counters

Display elements

LEDs, LCDs

In this course :

- **Combinational circuit design (Arithmetic circuits, Decoders, Encoders, MUX, DeMUX)**
- **Sequential circuit design (FFs, Synchronous & Asynchronous Circuits)**
- **Digital ICs and their characteristics (TTL, CMOS)**
- **Memories , PLDs & FPGAs**
- **Basics of HDL (Simulation & Synthesis Basics)**
- **Computer Organization (Modular Approach of CPU Design)**

Lab Sessions:

Implementation of Boolean Functions

4-bit counter

Adders & Subtractors

BCD Adder

Decoders, MUX & DeMUX

Latches & FFs

Comparators & ALU

Counters & Shift Registers

Memories & FPGAs

*** Take Home Assignments using HDLs**

EVALUATION COMPONENTS

	MM
MID SEM TEST	90
ASSIGNMENTS (Tutorials)	45
LAB COMPONENTS	45
COMPREHENSIVE EXAMINATION	120

INTEGRATED CIRCUITS

- LINEAR
- DIGITAL

LEVELS OF INTEGRATION

- SSI
- MSI
- LSI
- VLSI

Digital IC LOGIC FAMILIES

- RTL, DTL
- TTL
- ECL
- NMOS, PMOS
- CMOS

IC CHARACTERISTICS

- **Fan Out**
- **Propagation Delay**
- **Noise Margin**
- **Power Dissipation**

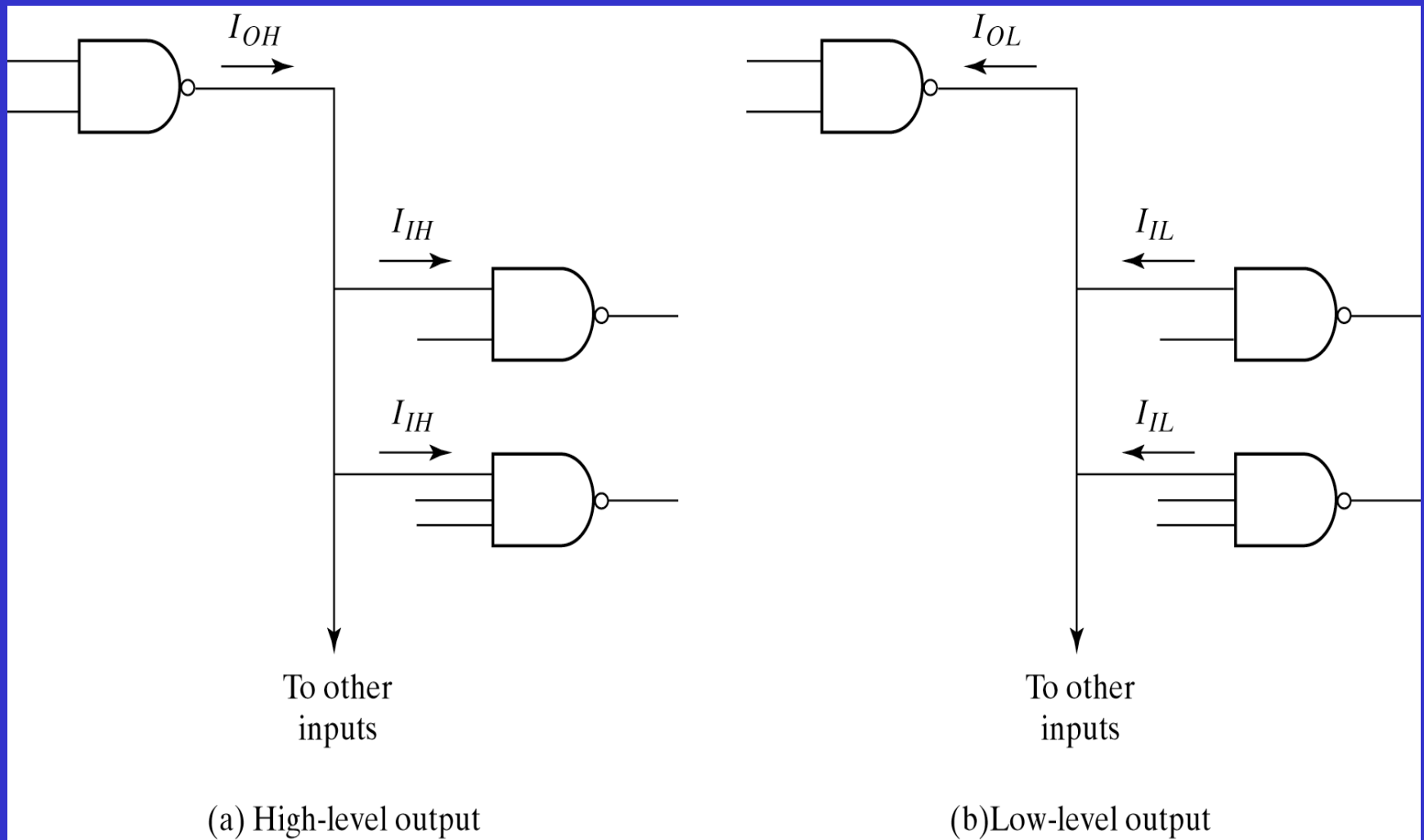


Fig. 10-3 Fan-Out Computation

For TTL logic family

$I_{IH}=40$ microamps

$I_{OH}=400$ microamps

$I_{OL}=16$ ma

$I_{IL}=1.6$ ma

Fanout = I_{OH} / I_{IH} OR $I_{OL} / I_{IL} = 10$

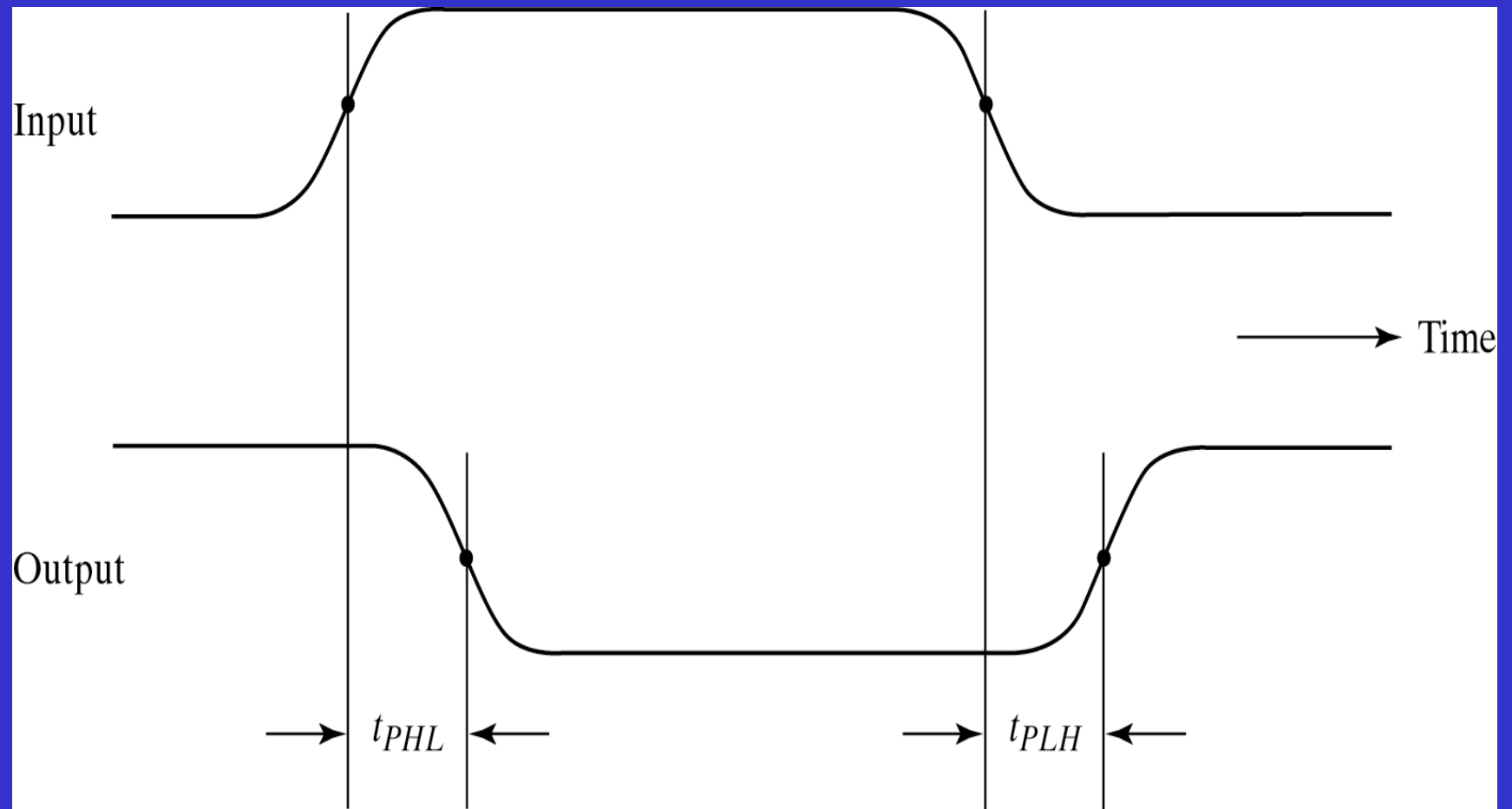


Fig. 10-4 Measurement of Propagation Delay

For TTL logic family

$TPHL = 7 \text{ ns}$

$TPLH = 11 \text{ ns}$

Depends on loading of gate

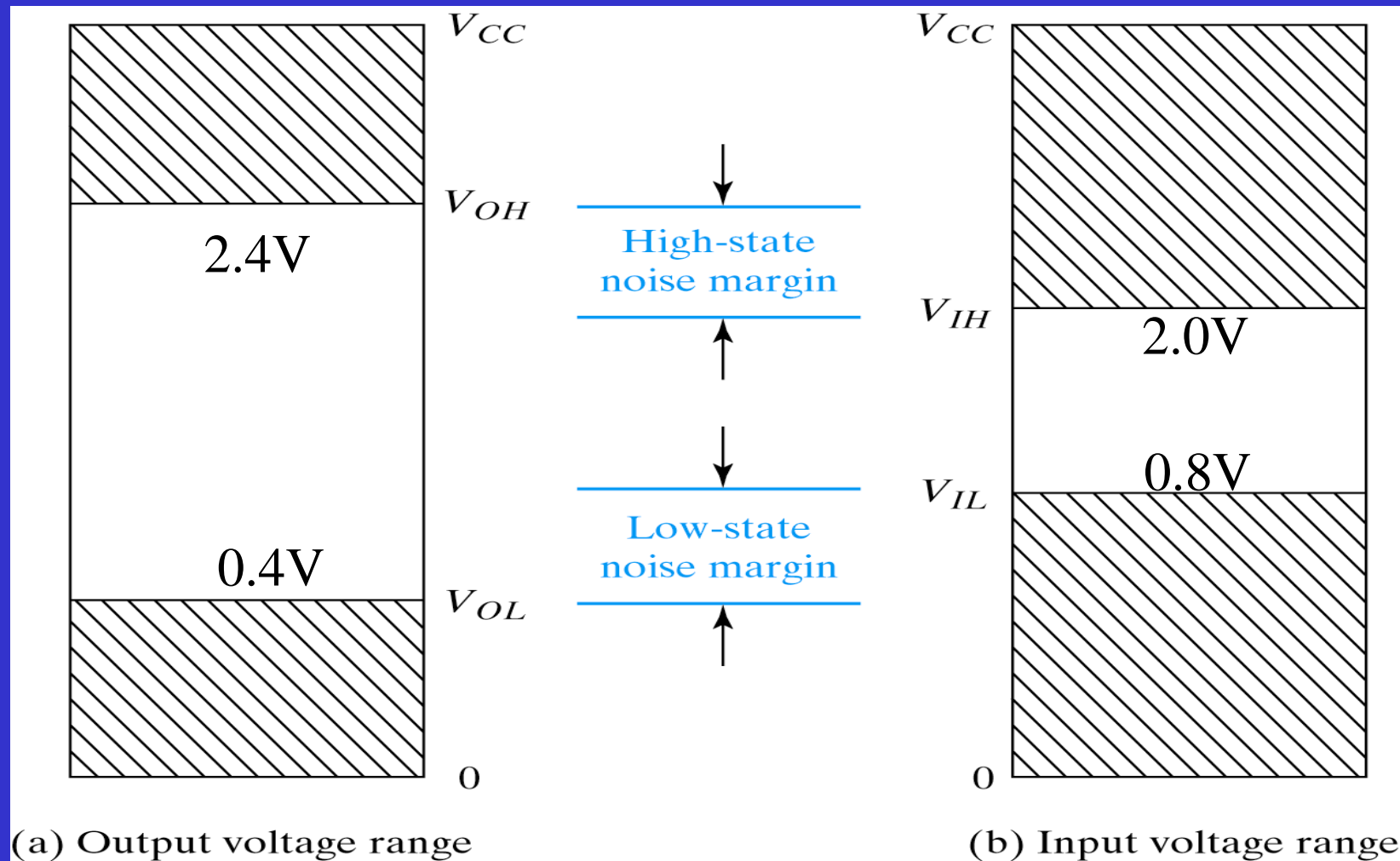


Fig. 10-5 Signals for Evaluating Noise Margin

Power Dissipation (P_D)

- Expressed in Milliwatts
- $PD = V_{CC} * I_{CC}$
- $I_{CC(avg)} = (I_{CCH} + I_{CCL}) / 2$
- 10mw for TTL NAND gate

Do you Know ?

- Excess – 3 Code
- Gray Code
- Maxterm
- Minterm
- Canonical form