Birla Institute of Technology and Science

Ist Semester 2010-2011

Digital Electronics and Computer Organization

CS/ EEE/ INSTR C391

Verilog Assignment

Instructions:

(i) Following are a set of problems prepared to practice Verilog programming. Please go through this and write the verilog code for each of the problem given below. Try to complete this before 15th November. Students can also take help from Instructors in case of any difficulty. The Tutorial Hour on **15th November** will be used to test the students the understanding of Verilog Programming through this exercise. **On 15th November** in the tutorial hour there will be a 30 **Minutes evaluation** component in which problems based on this sheet will be given to students. The Duration of this evaluation component is 30 Minutes and it will be from 8.00 **AM to 8.30 AM on 15th November.** Students coming late on this day to the tutorial hour will not be permitted to appear in the evaluation component. This evaluation component will be considered as a compulsory one for all the students with **Maximum Marks being 8** for this evaluation.

(ii) **Till now 9 Tutorials** have been completed in this course each having a small evaluation component with maximum marks as 5 in each evaluation. We will have two more tutorials which will be one on 22nd November and other on 29th November thus totaling 11 Tutorials with small evaluation component in each. We will be choosing **best 8 out of these 11 for the final total**.

Verilog Assignment Problems

Q1: Write a verilog behavioral code for a synchronous mod-7 counter which will count from 000 to 110. Use asynchronous enable and reset pins. i.e., when reset is logic 0 counter resets and when enable Logic 1 counter enabled for counting.

Q2: Write a verilog behavioral description of 4-bit up-down gray code counter with parallel load features. The counter also has asynchronous preset and clear features.

Q3: Write the verilog code for the Design of a 2×2 binary multiplier using gate-level verilog modeling. Also write a test bench to validate this design.

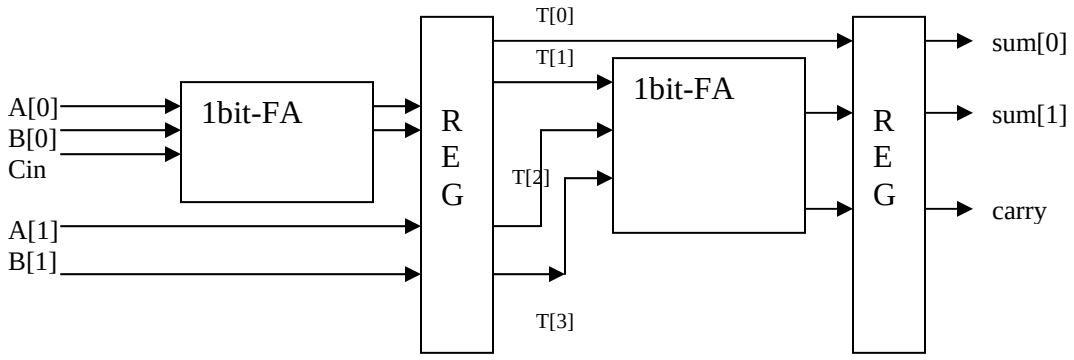
Q4: Design a 4-bit shift register that has the 4 functionalities- shift left, shift right, load and hold. Use gate level modelling to design the multiplexers and behavioural modelling for flip flops. Also write a test bench to check its functionality.

Q5: A divide by 8 frequency divider divides an input clock by 8. Design the circuit using JK FFs and write the verilog code using behavioural modeling.

Q6: A priority encoder can form an integral part of a programmable interrupt controller. Design a 8-input priority encoder using dataflow modeling. The order of Priority is D7 as Highest and D0 the lowest in the decreasing order. If say 3 inputs D_0, D_3, D_7 are asserted, D_7 is given a priority.

Q7: Obtain the state diagram for the synchronous sequential machine that detects a sequence '110'. The output is made '1' whenever the sequence is detected and reset only with subsequent occurrence of '00'. Write a behavioral verilog HDL code to model this synchronous sequential machine. The output must change at positive edge of clock. Write a test bench to verify the code.

Q8: Write a behavioral verilog HDL code for a 2-bit pipelined ripple adder, which must take input every clock cycle and generates the output after 2 clock cycles at positive edge only.



Q9: Write a behavioral verilog code to model the design of a 16-bit 2's complementer circuit using a shift register, a flip-flop and logic gates. The 2's complementer circuit accepts input in shift register through a parallel load operation at positive edge of the clock and generates the output after next 16 clock cycles. The final result must be available in shift register.

Q10: Write verilog code for BCD to 7-segment code generator with common cathode configuration, BCD to 7-segment code generator must accept input every positive clock edge and generates its output in next positive clock edge. Also write a test bench to display a stream '123456789', with one BCD digit in each clock cycle at a clock frequency of 1 Hz.