# [v13,01/12] perf/x86/intel/pt: Move Intel PT MSRs bit defines to global header

| 10654357 | diff (/patch/10654357/raw/) | mbox (/patch/10654357/mbox/) | series (/series/34463/mbox/) |
|---|---|---|---|

| | |
|---|---|
| **Message ID** | 1540368316-12998-2-git-send-email-luwei.kang@intel.com |
| **State** | New |
| **Headers** | show |
| **Series** | Intel Processor Trace virtualization enabling |
| **Related** | show |

## Commit Message

Kang, Luwei (/project/kvm/list/?submitter=168537) Oct. 24, 2018, 8:05 a.m. UTC

```
From: Chao Peng <chao.p.peng@linux.intel.com>

The Intel Processor Trace (PT) MSR bit defines are in a private
header. The upcoming support for PT virtualization requires these defines
to be accessible from KVM code.

Move them to the global MSR header file.

Reviewed-by: Thomas Gleixner <tglx@linutronix.de>
Signed-off-by: Chao Peng <chao.p.peng@linux.intel.com>
Signed-off-by: Luwei Kang <luwei.kang@intel.com>
---
 arch/x86/events/intel/pt.h       | 37 -------------------------------------
 arch/x86/include/asm/msr-index.h | 33 +++++++++++++++++++++++++++++++++
 2 files changed, 33 insertions(+), 37 deletions(-)
```

## Patch

| 10654357 | diff (/patch/10654357/raw/) | mbox (/patch/10654357/mbox/) | series (/series/34463/mbox/) |
|---|---|---|---|

```
diff --git a/arch/x86/events/intel/pt.h b/arch/x86/events/intel/pt.h
index 0eb41d0..0050ca1 100644
--- a/arch/x86/events/intel/pt.h
+++ b/arch/x86/events/intel/pt.h
@@ -20,43 +20,6 @@
 #define __INTEL_PT_H__

 /*
- * PT MSR bit definitions
- */
-#define RTIT_CTL_TRACEEN               BIT(0)
-#define RTIT_CTL_CYCLEACC              BIT(1)
-#define RTIT_CTL_OS                    BIT(2)
-#define RTIT_CTL_USR                   BIT(3)
-#define RTIT_CTL_PWR_EVT_EN            BIT(4)
-#define RTIT_CTL_FUP_ON_PTW            BIT(5)
-#define RTIT_CTL_CR3EN                 BIT(7)
-#define RTIT_CTL_TOPA                  BIT(8)
-#define RTIT_CTL_MTC_EN                        BIT(9)
-#define RTIT_CTL_TSC_EN                        BIT(10)
-#define RTIT_CTL_DISRETC               BIT(11)
-#define RTIT_CTL_PTW_EN                        BIT(12)
-#define RTIT_CTL_BRANCH_EN             BIT(13)
-#define RTIT_CTL_MTC_RANGE_OFFSET      14
-#define RTIT_CTL_MTC_RANGE             (0x0full << RTIT_CTL_MTC_RANGE_OFFSET)
-#define RTIT_CTL_CYC_THRESH_OFFSET     19
-#define RTIT_CTL_CYC_THRESH            (0x0full << RTIT_CTL_CYC_THRESH_OFFSET)
-#define RTIT_CTL_PSB_FREQ_OFFSET       24
-#define RTIT_CTL_PSB_FREQ                      (0x0full << RTIT_CTL_PSB_FREQ_OFFSET)
-#define RTIT_CTL_ADDR0_OFFSET          32
-#define RTIT_CTL_ADDR0                 (0x0full << RTIT_CTL_ADDR0_OFFSET)
-#define RTIT_CTL_ADDR1_OFFSET          36
-#define RTIT_CTL_ADDR1                 (0x0full << RTIT_CTL_ADDR1_OFFSET)
-#define RTIT_CTL_ADDR2_OFFSET          40
-#define RTIT_CTL_ADDR2                 (0x0full << RTIT_CTL_ADDR2_OFFSET)
-#define RTIT_CTL_ADDR3_OFFSET          44
-#define RTIT_CTL_ADDR3                 (0x0full << RTIT_CTL_ADDR3_OFFSET)
-#define RTIT_STATUS_FILTEREN           BIT(0)
-#define RTIT_STATUS_CONTEXTEN          BIT(1)
-#define RTIT_STATUS_TRIGGEREN          BIT(2)
-#define RTIT_STATUS_BUFFOVF            BIT(3)
-#define RTIT_STATUS_ERROR              BIT(4)
-#define RTIT_STATUS_STOPPED            BIT(5)
-
-/*
  * Single-entry ToPA: when this close to region boundary, switch
  * buffers to avoid losing data.
  */
diff --git a/arch/x86/include/asm/msr-index.h b/arch/x86/include/asm/msr-index.h
index 4731f0c..d3a9eb9 100644
```

```
--- a/arch/x86/include/asm/msr-index.h
+++ b/arch/x86/include/asm/msr-index.h
@@ -120,7 +120,40 @@
 #define MSR_PEBS_LD_LAT_THRESHOLD      0x000003f6

 #define MSR_IA32_RTIT_CTL              0x00000570
+#define RTIT_CTL_TRACEEN               BIT(0)
+#define RTIT_CTL_CYCLEACC              BIT(1)
+#define RTIT_CTL_OS                    BIT(2)
+#define RTIT_CTL_USR                   BIT(3)
+#define RTIT_CTL_PWR_EVT_EN            BIT(4)
+#define RTIT_CTL_FUP_ON_PTW            BIT(5)
+#define RTIT_CTL_CR3EN                 BIT(7)
+#define RTIT_CTL_TOPA                  BIT(8)
+#define RTIT_CTL_MTC_EN                        BIT(9)
+#define RTIT_CTL_TSC_EN                        BIT(10)
+#define RTIT_CTL_DISRETC               BIT(11)
+#define RTIT_CTL_PTW_EN                        BIT(12)
+#define RTIT_CTL_BRANCH_EN             BIT(13)
+#define RTIT_CTL_MTC_RANGE_OFFSET      14
+#define RTIT_CTL_MTC_RANGE             (0x0full << RTIT_CTL_MTC_RANGE_OFFSET)
+#define RTIT_CTL_CYC_THRESH_OFFSET     19
+#define RTIT_CTL_CYC_THRESH            (0x0full << RTIT_CTL_CYC_THRESH_OFFSET)
+#define RTIT_CTL_PSB_FREQ_OFFSET       24
+#define RTIT_CTL_PSB_FREQ              (0x0full << RTIT_CTL_PSB_FREQ_OFFSET)
+#define RTIT_CTL_ADDR0_OFFSET          32
+#define RTIT_CTL_ADDR0                 (0x0full << RTIT_CTL_ADDR0_OFFSET)
+#define RTIT_CTL_ADDR1_OFFSET          36
+#define RTIT_CTL_ADDR1                 (0x0full << RTIT_CTL_ADDR1_OFFSET)
+#define RTIT_CTL_ADDR2_OFFSET          40
+#define RTIT_CTL_ADDR2                 (0x0full << RTIT_CTL_ADDR2_OFFSET)
+#define RTIT_CTL_ADDR3_OFFSET          44
+#define RTIT_CTL_ADDR3                 (0x0full << RTIT_CTL_ADDR3_OFFSET)
 #define MSR_IA32_RTIT_STATUS           0x00000571
+#define RTIT_STATUS_FILTEREN           BIT(0)
+#define RTIT_STATUS_CONTEXTEN          BIT(1)
+#define RTIT_STATUS_TRIGGEREN          BIT(2)
+#define RTIT_STATUS_BUFFOVF            BIT(3)
+#define RTIT_STATUS_ERROR              BIT(4)
+#define RTIT_STATUS_STOPPED            BIT(5)
 #define MSR_IA32_RTIT_ADDR0_A          0x00000580
 #define MSR_IA32_RTIT_ADDR0_B          0x00000581
 #define MSR_IA32_RTIT_ADDR1_A          0x00000582
```