[v13,04/12] perf/x86/intel/pt: Add new bit definitions for PT MSRs

10654379	diff (/patch/10654379/raw/)	mbox (/patch/10654379/mbox/)	series (/series/34463/mbox/)

Message ID	1540368316-12998-5-git-send-email-luwei.kang@intel.com
State	New
Headers	show
Series	Intel Processor Trace virtualization enabling
Related	show

Commit Message

Kang, Luwei (/project/kvm/list/?submitter=168537) Oct. 24, 2018, 8:05 a.m. UTC

```
Add bit definitions for Intel PT MSRs to support trace output
directed to the memeory subsystem and holds a count if packet
bytes that have been sent out.

These are required by the upcoming PT support in KVM guests
for MSRs read/write emulation.

Signed-off-by: Luwei Kang <luwei.kang@intel.com>
---
 arch/x86/include/asm/msr-index.h | 3 +++
 1 file changed, 3 insertions(+)
```

Patch

10654379	diff (/patch/10654379/raw/)	mbox (/patch/10654379/mbox/)	series (/series/34463/mbox/)

```
diff --git a/arch/x86/include/asm/msr-index.h b/arch/x86/include/asm/msr-index.h
index d3a9eb9..107818e3 100644
--- a/arch/x86/include/asm/msr-index.h
+++ b/arch/x86/include/asm/msr-index.h
@@ -126,6 +126,7 @@
 #define RTIT_CTL_USR                   BIT(3)
 #define RTIT_CTL_PWR_EVT_EN            BIT(4)
 #define RTIT_CTL_FUP_ON_PTW            BIT(5)
+#define RTIT_CTL_FABRIC_EN             BIT(6)
 #define RTIT_CTL_CR3EN                 BIT(7)
 #define RTIT_CTL_TOPA                  BIT(8)
 #define RTIT_CTL_MTC_EN                        BIT(9)
@@ -154,6 +155,8 @@
 #define RTIT_STATUS_BUFFOVF            BIT(3)
 #define RTIT_STATUS_ERROR              BIT(4)
 #define RTIT_STATUS_STOPPED            BIT(5)
+#define RTIT_STATUS_BYTECNT_OFFSET     32
+#define RTIT_STATUS_BYTECNT            (0x1ffffull << RTIT_STATUS_BYTECNT_OFFSET)
 #define MSR_IA32_RTIT_ADDR0_A          0x00000580
 #define MSR_IA32_RTIT_ADDR0_B          0x00000581
 #define MSR_IA32_RTIT_ADDR1_A          0x00000582
```