

[v13,05/12] perf/x86/intel/pt: add new capability for Intel PT

Message ID 1540368316-12998-6-git-send-email-luwei.kang@intel.com

State New

Headers show

Series Intel Processor Trace virtualization enabling

Related show

10654363

[diff \(/patch/10654363/raw/\)](/patch/10654363/raw/)[mbox \(/patch/10654363/mbox/\)](/patch/10654363/mbox/)[series \(/series/34463/mbox/\)](/series/34463/mbox/)

Commit Message

Kang, Luwei (/project/kvm/list/?submitter=168537)

Oct. 24, 2018, 8:05 a.m. UTC

This adds support for "output to Trace Transport subsystem" capability of Intel PT. It means that PT can output its trace to an MMIO address range rather than system memory buffer.

Acked-by: Song Liu <songliubraving@fb.com>

Signed-off-by: Luwei Kang <luwei.kang@intel.com>

```
arch/x86/events/intel/pt.c | 1 +
arch/x86/include/asm/intel_pt.h | 1 +
2 files changed, 2 insertions(+)
```

Comments

Thomas Gleixner (/project/kvm/list/?submitter=107)

Oct. 30, 2018, 9:57 a.m. UTC | #1 (/comment/22290925/)

On Wed, 24 Oct 2018, Luwei Kang wrote:

```
> This adds support for "output to Trace Transport subsystem"
> capability of Intel PT. It means that PT can output its
> trace to an MMIO address range rather than system memory buffer.
>
> Acked-by: Song Liu <songliubraving@fb.com>
> Signed-off-by: Luwei Kang <luwei.kang@intel.com>
```

For patches 1-5:

Reviewed-by: Thomas Gleixner <tglx@linutronix.de>

Patch

[10654363](#)
[diff \(/patch/10654363/raw/\)](#)
[mbox \(/patch/10654363/mbox/\)](#)
[series \(/series/34463/mbox/\)](#)

```
diff --git a/arch/x86/events/intel/pt.c b/arch/x86/events/intel/pt.c
index 53e481a..9597ea6 100644
--- a/arch/x86/events/intel/pt.c
+++ b/arch/x86/events/intel/pt.c
@@ -68,6 +68,7 @@
     PT_CAP(topa_output,          0, CPUID_ECX, BIT(0)),
     PT_CAP(topa_multiple_entries, 0, CPUID_ECX, BIT(1)),
     PT_CAP(single_range_output,  0, CPUID_ECX, BIT(2)),
+    PT_CAP(output_subsys,         0, CPUID_ECX, BIT(3)),
+    PT_CAP(payloads_lip,          0, CPUID_ECX, BIT(31)),
     PT_CAP(num_address_ranges,    1, CPUID_EAX, 0x3),
     PT_CAP(mtc_periods,          1, CPUID_EAX, 0xffff0000),
diff --git a/arch/x86/include/asm/intel_pt.h b/arch/x86/include/asm/intel_pt.h
index 00f4afb..634f99b 100644
--- a/arch/x86/include/asm/intel_pt.h
+++ b/arch/x86/include/asm/intel_pt.h
@@ -16,6 +16,7 @@ enum pt_capabilities {
     PT_CAP_topa_output,
     PT_CAP_topa_multiple_entries,
     PT_CAP_single_range_output,
+    PT_CAP_output_subsys,
+    PT_CAP_payloads_lip,
     PT_CAP_num_address_ranges,
     PT_CAP_mtc_periods,
```

patchwork (<http://jk.ozlabs.org/projects/patchwork/>) patch tracking system | version v2.1.0 | [about patchwork \(/about/\)](#)