

# Modeling and Control of Bittide Synchronization



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1

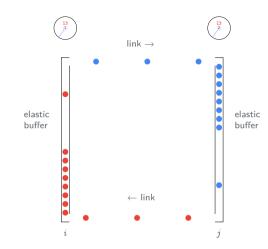
### Overview

- Google research project
  - originated at Princeton: Spalink 2006.
  - broad scope: applications, scheduling, simulation, hardware, theory
- paper
  - problem formulation
  - model well-posedness
  - simulation algorithm
- outline: the mechanism, logical synchrony, controlling frequency

## Overview

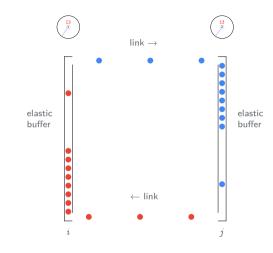
- at each node *i* 
  - clock
  - each incoming link has a queue called the *elastic buffer*

- at each node, with each clock tick
  - a frame is removed from all elastic buffers
  - a frame is sent on all outgoing links

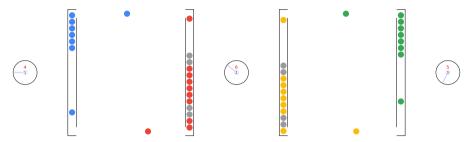


### Mechanism

- ullet if oscillator at node j is faster than that at i
  - j's elastic buffer will drain
  - i's elastic buffer will fill
- nodes observe elastic buffers, adjust frequency



# Logical Synchrony



- $\bullet$  marked frames from nodes 1 and 3 always arrive simultaneously at node 2
- an example of *logical synchrony*
- does not require clocks to be synchronized

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# Abstract frame model

# Modeling frames and phase

$$eta_{i imes j}(t) = \lfloor heta_i(t - l_{i imes j}) 
floor - \lfloor heta_j(t) 
floor + \lambda_{i imes j}$$

- $\bullet$  history of clock phases  $\theta$  determines location of every frame
- ullet  $\lambda_{i ilde{r}j}$  is a constant, determined by clock offsets at boot
- buffer occupancy is (roughly) phase difference between clocks at each end of the link

# Control loop

#### dynamics

$$egin{aligned} rac{d heta_i}{dt} &= \omega_i \ eta_{i + j}(t) &= \left\lfloor heta_i(t - l_{i + j}) 
ight
floor - \left\lfloor heta_j(t) 
ight
floor + \lambda_{i + j} \end{aligned}$$

#### measurements

- at each node i, measure buffer occupancies β<sub>j+i</sub> for all neighbours j (relative to a mid-point value β<sup>off</sup>)
- ullet let  $r_i$  be the sum  $r_i = \sum_{j|j\sim i} (eta_{j ilde{+}i} eta^{\mathsf{off}})$

#### control

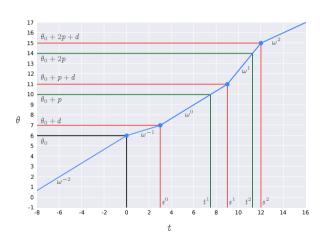
- apply frequency correction:  $\omega_i = c_i + \omega_i^{ t u}$
- $\omega_i^{\rm u}$  is the *uncorrected frequency* of the oscillator, not known
- e.g., proportional control is  $c_i = k_P r_i$

# The abstract frame model

for k > 0 and  $t \in \mathbb{R}$ 

$$\begin{split} \dot{\theta}_i(t) &= \omega_i(t) \\ \beta_{j*i}(t) &= \lfloor \theta_j(t-l) \rfloor - \lfloor \theta_i(t) \rfloor + \lambda_{j*i} \\ \omega_i(t) &= \omega_i^k \quad \text{for } t \in [s_i^k, s_i^{k+1}) \\ t_i^k &= \theta_i^{-1}(\theta_i^0 + kp) \\ s_i^k &= \theta_i^{-1}(\theta_i^0 + kp + d) \\ \omega_i^k &= c_i^k + \omega_i^u \end{split}$$

$$egin{aligned} c_i^k &= \chi_i^k(m_i^0, m_i^1, \ldots, m_i^k) \ m_i^k &= \{eta_{j o i}(t_i^k) \mid j \in \mathcal{V}, j \sim i\} \end{aligned}$$



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- features:
  - ullet sample rate at node i depends on  $\omega_i$
  - no absolute time (integration/differentiation scaled by local clock rate)
  - hybrid: quantization
- existence of solutions? yes, see paper
- exact algorithm for simulation
- software: bittide.googlesource.com

# Control

# Control objectives

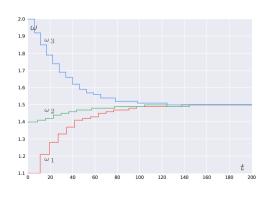
- frequencies cannot remain different for too long, otherwise buffers will over/underflow
- bittide performance requirement: maintain buffer occupancy within limits
- ideally buffer occupancies should be small, and frequencies large
- controller must be decentralized
- no *in-band* signalling
- failure handling, addition and removal of nodes, boot, etc.,

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# Proportional control



- $k_P = 0.01$
- latency = 1.0
- $poll_period = 10$
- uncorrected\_frequency = (1.1, 1.4, 2.0)
- $control_delay = 2$
- varying step width is a consequence of periodic sampling w.r.t. the local clock



# Simpler models

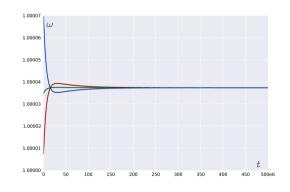
• fluid model

$$egin{aligned} \dot{ar{ heta}} &= \omega \ ar{eta} &= -B^{\mathsf{T}} ar{ heta} \ r &= B ar{eta} \ \omega &= c + \omega^{\mathsf{u}} \end{aligned}$$

• with proportional control

$$\dot{\bar{\theta}} = -k_P B B^{\mathsf{T}} \bar{\theta} + \omega^u$$

the well-known Laplacian dynamics



# Thank you!