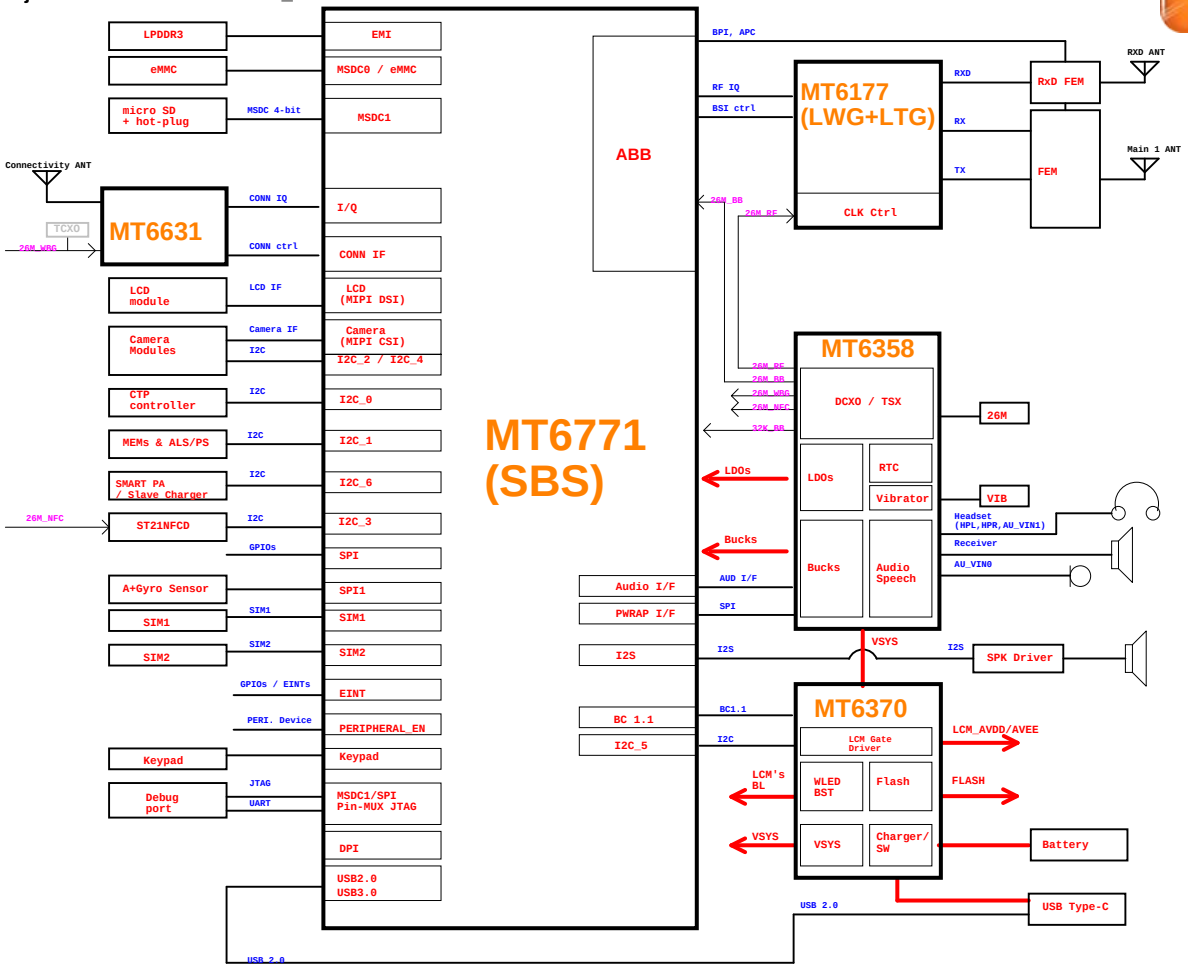
Project : MT6771 LPDDR3 REF_SCH TOP LEVEL



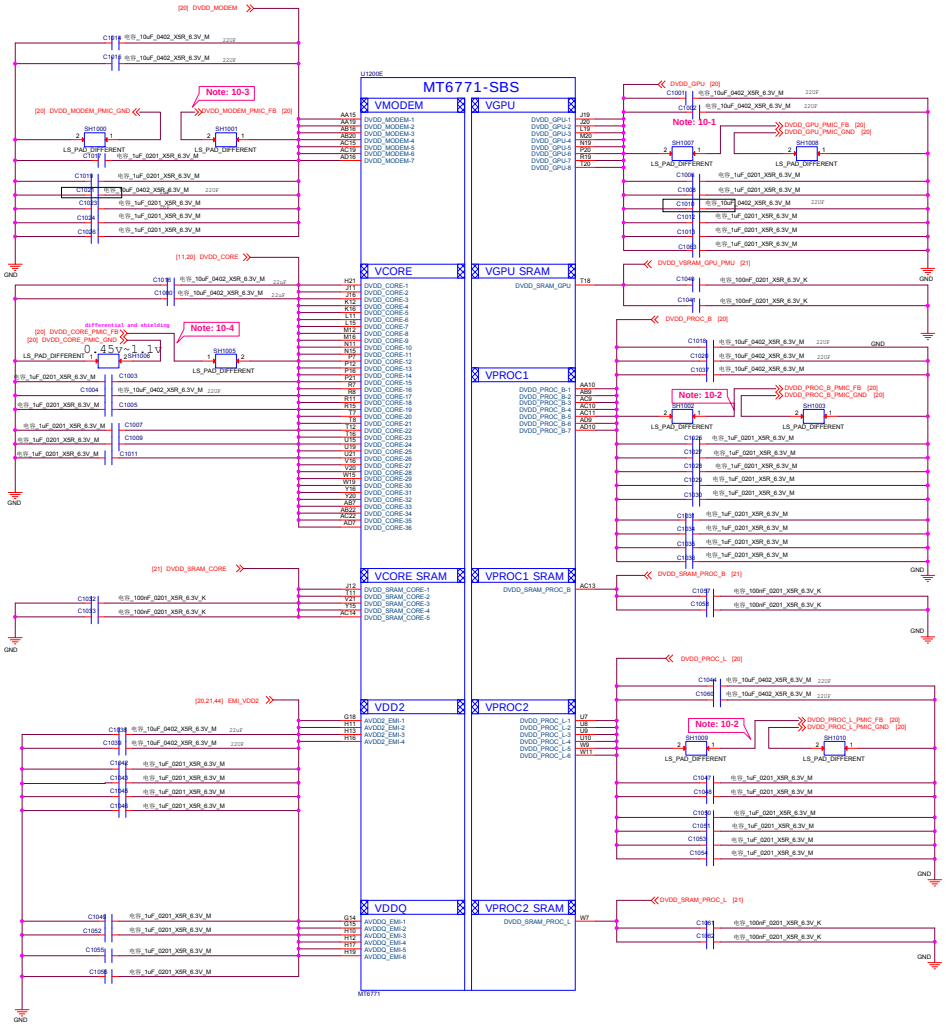
Title	01_Block_Diagram	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 1 of 99	

I2C	AP , SCP, SSPM	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	AP	CTP	400 Kbps	Yes.	GT1151 I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0x14 (Write:0x28, Read:0x29)
I2C-1(I3C)	AP ,SCP	M Sensor	400 Kbps	Yes.	AK09915C / M-Sensor I2C Address 0x0C (Write: 0x18, Read: 0x19)
		RGB / PS Sensor	400 Kbps	Yes.	CM36558 / UV + PS I2C address: 0X51 (Write:0xA2, Read:0xA3) - default CM36652 / RGB + PS I2C address: 0X60 (Write:0xC0, Read:0xC1
		Barometer	400 Kbps	Yes.	BMP280 I2C address: 0X77 (Write:0xEE, Read:0xEF)
I2C-2 (I3C)	AP	Rear Camera - 21M	400 Kbps		Rear camera I2C address: 0X1A (Write:0x34, Read:0x35) AF driver I2C address: 0X0C (Write:0x18, Read:0x19) EEPROM I2C address: 0X50 (Write:0xA0, Read:0xA1)
		Dual camera module Rear Camera - 16M	400 Kbps	Yes.	Rear camera I2C address: 0X (Write:0x, Read:0x) AF driver I2C address: 0X (Write:0x, Read:0x) EEPROM I2C address: 0X (Write:0x, Read:0x)
I2C-3	AP	NFC	400K bps	Yes.	NFC I2C address: 0X08 (Write:0x10, Read:0x11)
I2C-4 (I3C)	AP	Front Camera - 5M	400 Kbps	Yes.	Front camera I2C address:0X35 (Write:0x6A, Read:0x6B) EEPROM I2C address: 0X54 (Write:0xA8, Read:0xA9)
		Dual camera module Rear Camera - 20M	400 Kbps	Yes.	Rear camera I2C address: 0X (Write:0x, Read:0x) AF driver I2C address: 0X (Write:0x, Read:0x) EEPROM I2C address: 0X (Write:0x, Read:0x)
I2C-5	SSPM	MT6370	3.4Mbps	Yes.	MT6370 PD's I2C address: 0X4E (Write:0X9C, Read:0X9D) MT6370 PMU's I2C address: 0X34 (Write:0X68, Read:0X69)
I2C-6	AP ,SCP	Smart PA	400 Kbps	Yes.	RT5509 Speaker AMP I2C Address: 0x34 (Write:0x68, Read:0x69)
		Slave charger	400 Kbps	Yes.	RT9465 / slave charger I2C address: 0X4B (Write:0x96, Read:0x97)

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

Title: 02_I2C_ID_Overview		
Size: C	Project	Rev: V1
Date: Tuesday, November 13, 2018	Sheet 2 of 99	

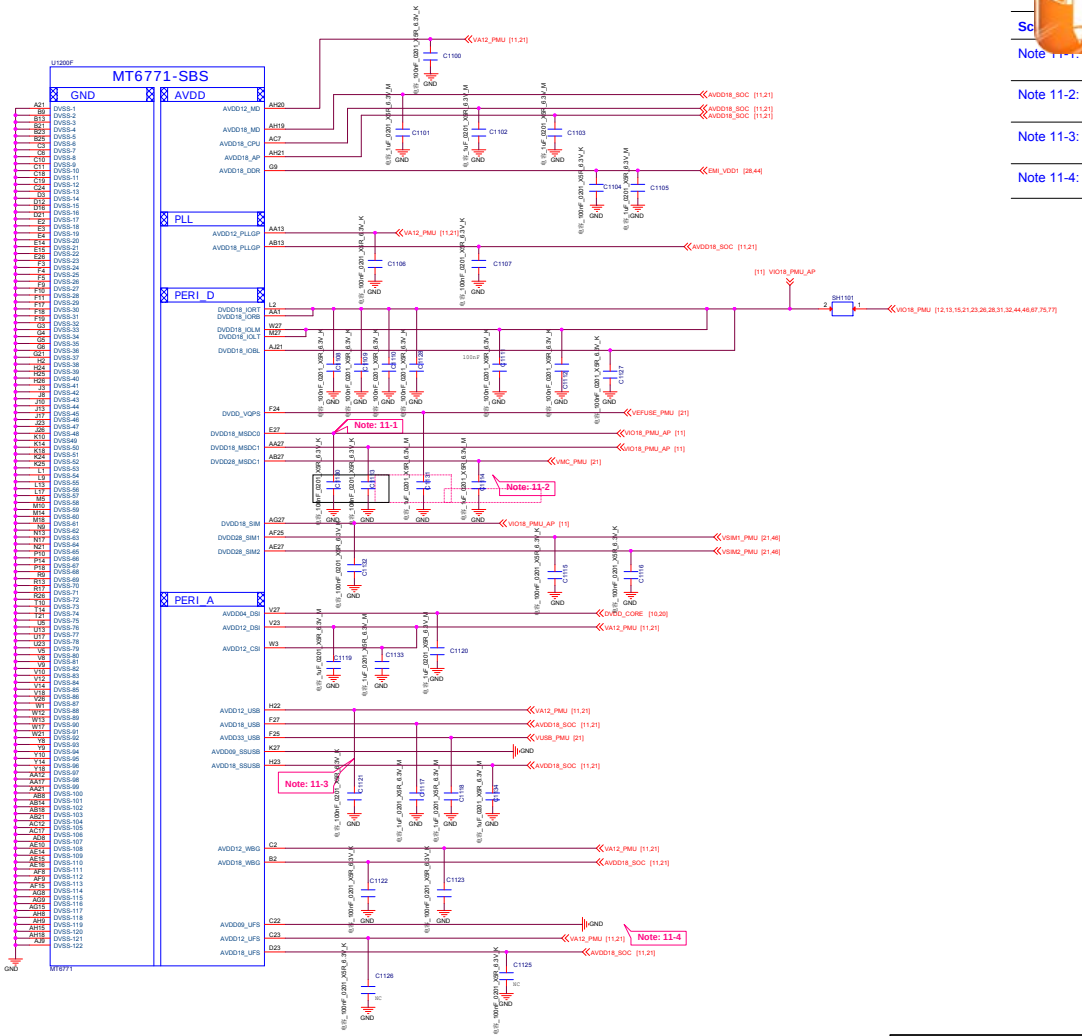
Title	05_Change_Notice	
Size C	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 5 of 99	



Schematic design notice of "10_BB_POWER_PDN" page.

Note 10-1:	Differential pair of DVDD_GPU remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-2:	Differential pair of DVDD_PROC remote sense must be close to BB's ball Remote sense trace with GND shielding to PMIC (Differential)
Note 10-3:	Differential pair of DVDD_MODEM remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-4:	Differential pair of DVDD_CORE remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)

Title	10_BB_POWER_PDN	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 10 of 99	



Sc ce of "11_BB_POWER_IO" page.

Note 11-1: C1130 closed DVDD18_MSDC0 150mil
C1113 closed DVDD18_MSDC1 150mil

Note 11-2: C1114 closed DVDD28_MSDC1 150mil

Note 11-3: Connects "AVDD09_SSUSB" to GND when USB3.0 is not used.

Note 11-4: Connects "AVDD09_UFS" to GND when UFS is not used.

Title	11_BB_POWER_IO	
Size D	Project	Rev V1
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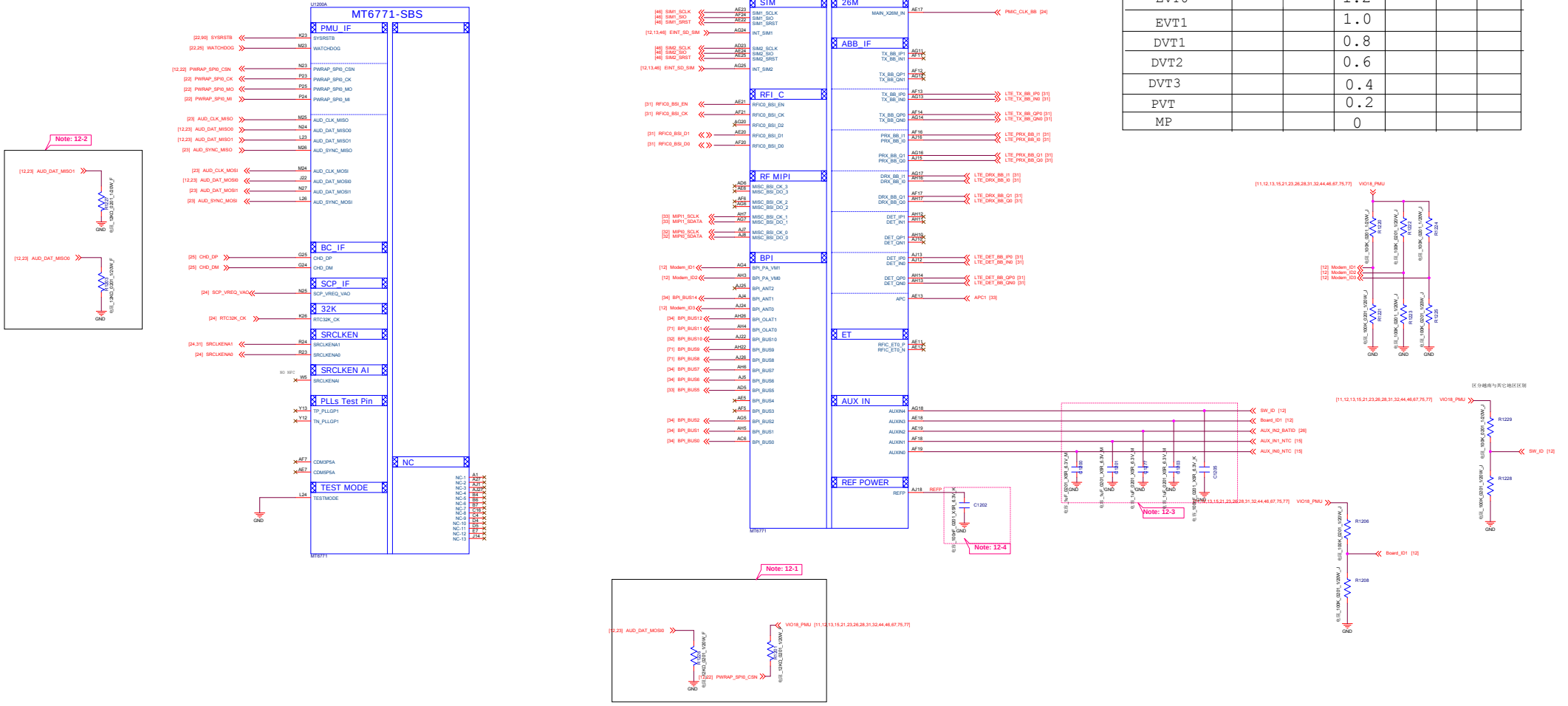
阶段	R1206	R1208	BOARD_ID1(V)	备注		
EVT0			1.2			
EVT1			1.0			
DVT1			0.8			
DVT2			0.6			
DVT3			0.4			
PVT			0.2			
MP			0			



Schematic design notice of "12_BB_1" page.

Note 12-1: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP_JTAG	IO_JTAG
HI	LO	N/A	N/A
HI	HI	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	N/A
LO	LO	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	DPI_11/DPI_HSYNC/DPI_VSYNC/DPI_DE/ DPI_CK/DPI_D8/DPI_D9
LO	HI	MSDC1_CLK/CMD/ DAT0/DAT1/DAT2	N/A

Note 12-2: "AUD_DAT_MISO0" is bootstrap pin to enable serial JTAG output over USB2.0 interface or not.
When "AUD_DAT_MISO0" is pulled to high in system start up and then USB2.0 interface will be switched into serial JTAG mode.

"AUD_DAT_MISO1" is bootstrap pin to select system booting up from eMMC or UFS device.

AUD_DAT_MISO1	Booting device
LO	eMMC
HI	UFS

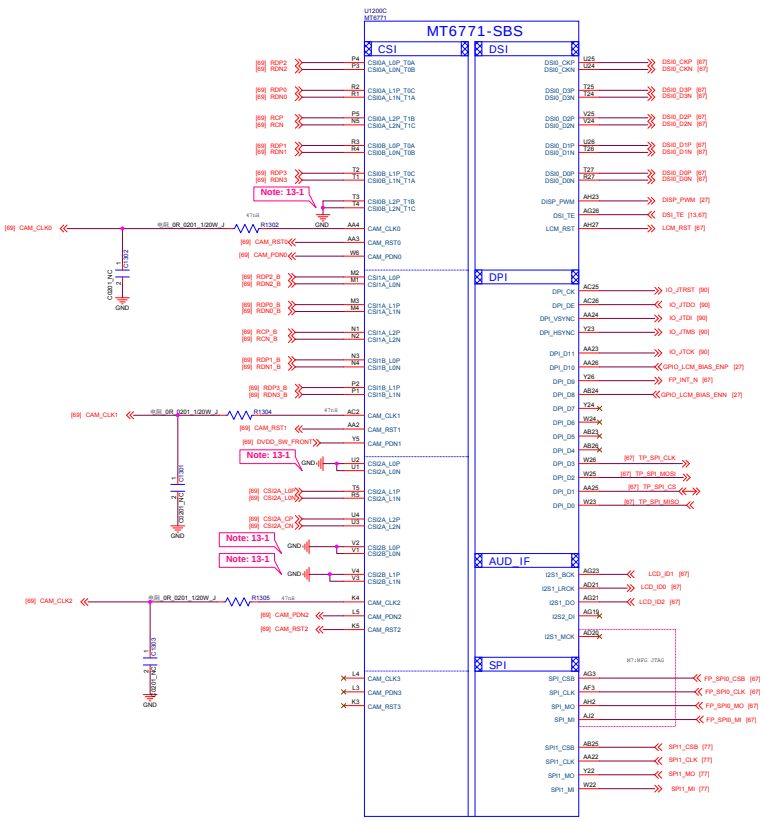
Note 12-3: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

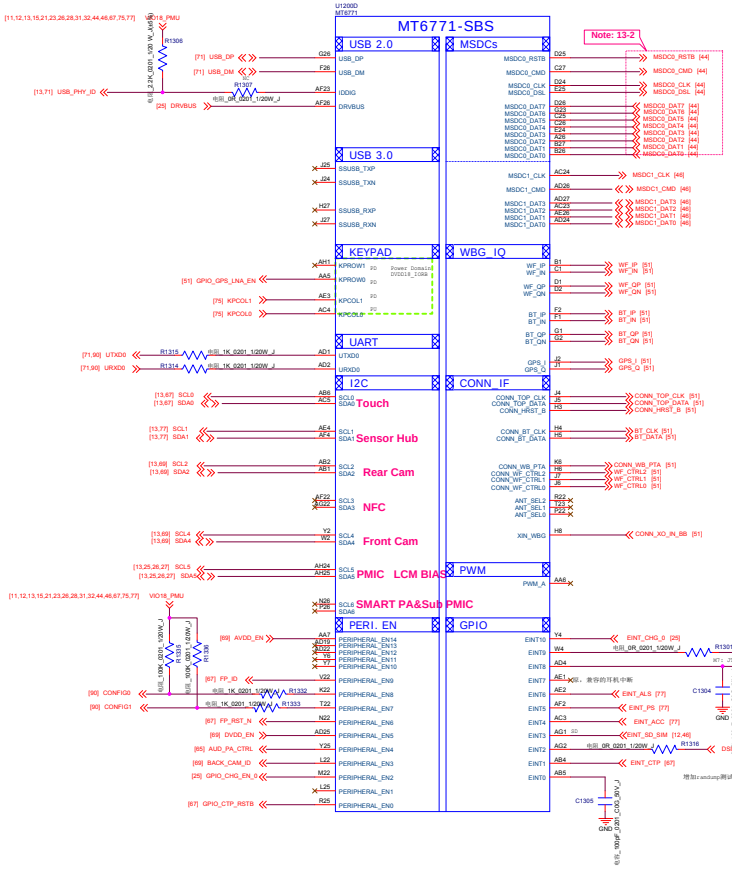
Note 12-4: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

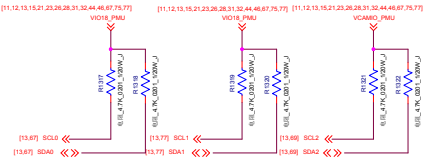
Note 12-5: AUD_SYNC_MISO and AUD_CLK_MISO are DDR type feature in bootstrap

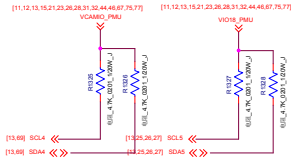
AUD_SYNC_MISO	AUD_CLK_MISO	DDR
LO	LO	LPDDR4X
LO	HI	LPDDR4X(Ext x 2 EN)
HI	LO	LPDDR3
HI	HI	LPDDR4X(Ext x 1 EN)

Title	12_BB_1	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 12 of 99	









Schematic design notice of "13_BB_2" page.

Note 13-1: CSI ports which are no use could be connected to GND or set in NC.
For detail information, please refer to MT6771 Design Notice

Note 13-2: Please check eMCP LP3 and eMCP LP4X pin mux

Title	13_BB_2	
Size D	Project	Rev V1
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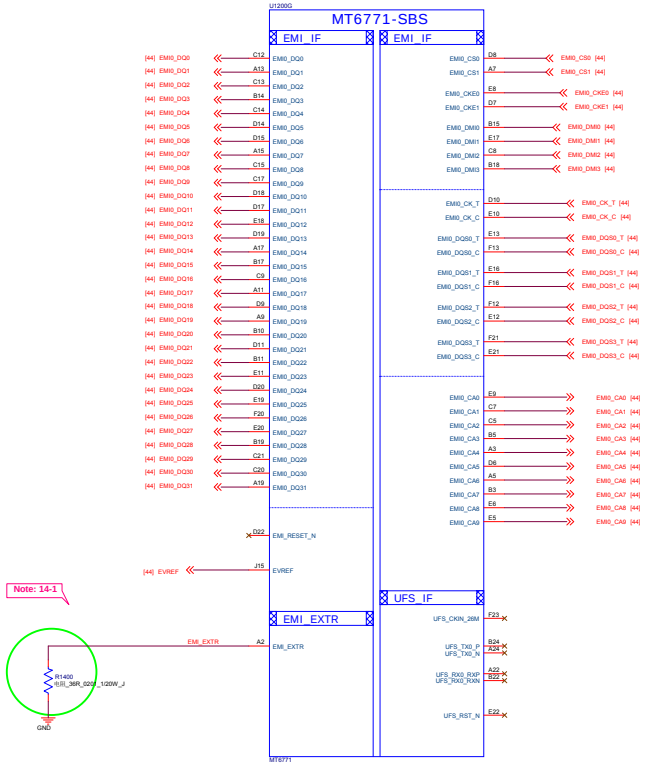
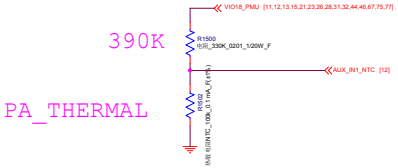


Schematic design notice of "14_BB_3" page.

Note 14-1: The resistor of EMI_EXTR for DRAM has to be placed near to BB as close as possible
R1400 please select 34.8 ohm (1%) resistor

Title	14_BB_3	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 14 of 99	

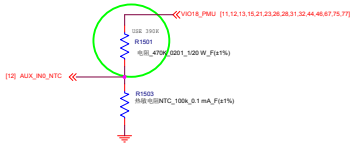


change to NCP03WF104F05RL Murata

Thermistor to sense RF PA temperature

1. NTC1502 must close to LTE Band 7 PA or the hottest PA <2mm.
2. The distance is the shortest distance from package edge to edge.

Thermistor / To sense board level temperature



Distance to AP is 5~7mm and away form other heat resource 10mm~12mm

Title	15_BB_AUXADC_Thermal	
Size D	Project	Rev V1
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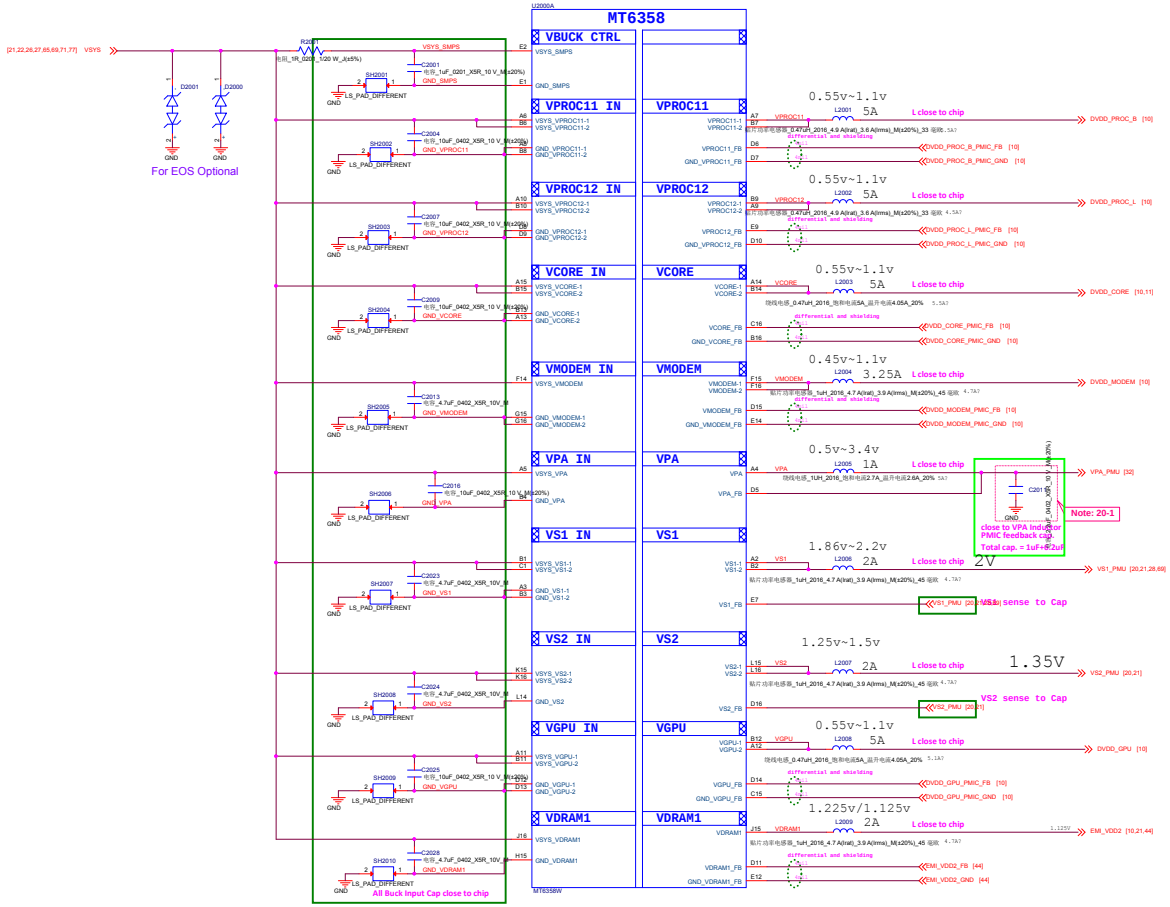


MT6358 BUCK output

Input Power	Power Name	Output Voltage (V)	Output Current	Default Voltage
BUCK from VSYS	VPA	0.5~3.4V	1A	0.5V
	VPROC11	0.55~1.1V	5A	0.8V
	VPROC12	0.55~1.1V	5A	0.8V
	VGPU	0.55~1.1V	5A	0.8V
	VCORE	0.55~1.1V	5A	0.8V
	VMODEM	0.45~1.1V	3.25A	0.8V
	VS1	1.86~2.2V	2A	2V
	VS2	1.25~1.5V	2A	1.35V
	VDRAM1	1.225/1.125	2A	1.225/1.125

IP	Inductance	IDC(A)	
VS1	1	2.6	
VS2	1	2.5	
VDRAM	1	2.5	
VPA	1	4	
VMODEM	1	4	
VPROC11	0.47	5.3	
VPROC12	0.47	3.85	
VCORE	0.47	5.3	
VGPU	0.47	3.9	

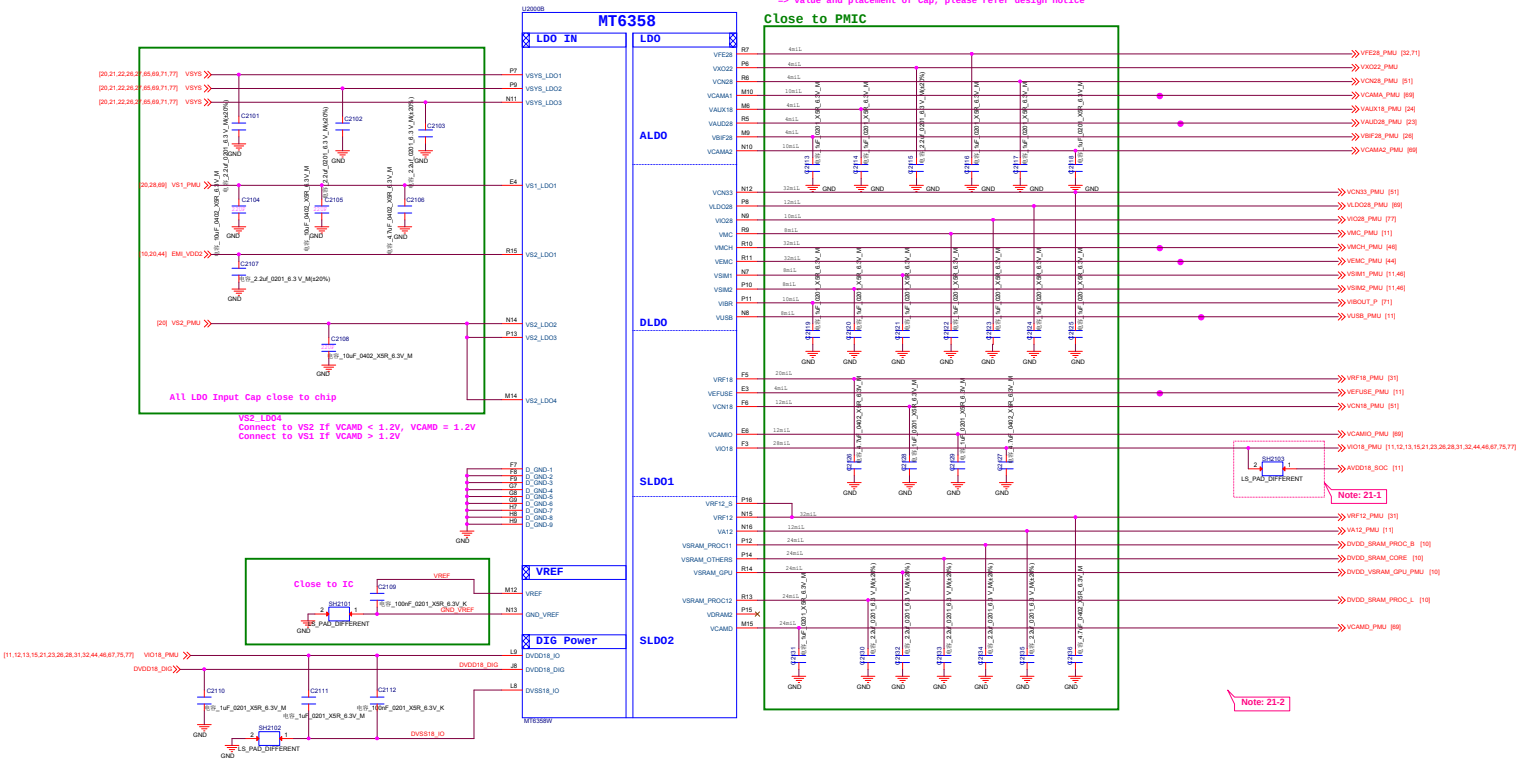
Schematic design notice of "20_POWER_MT6358-Buck" page.

Note 20-1: Please select C2011 with 0402 size

Title	20_POWER_MT6358_Buck	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 20 of 99	

MT6358 LDO output

Input Power	Power Name	Output Voltage (V)	Output Current	Default Voltage
LDO from VSYS	VFE28	2.8	50mA	2.8V
	VXO22	2.24	50mA	2.24V
	VCN28	2.8	50mA	2.8V
	VCAMA	1.8/2.5/2.8	200mA	2.8V
	VAUX18	1.8	20mA	1.8V
	VAUD28	2.8	50mA	2.8V
	VBIF28	2.8	1mA	2.8V
	VCN33	3.3/3.4/3.5/3.6	800mA	3.5V
	VLDO28	2.8/3.0	360mA	2.8V
	VIO28	2.8	200mA	2.8V
	VMC	1.86/2.9/3.0/3.3	200mA	3.0V
	VMCH	2.9/3.0/3.3	800mA	3.0V
	VEMC	2.9/3.0/3.3	800mA	3.3V
	VSIM1	1.7/1.8/1.86/2.76/3.0/3.1	200mA	1.86V
	VSIM2	1.7/1.8/1.86/2.76/3.0/3.1	200mA	1.86V
	VIBR	1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3	200mA	2.8V
	VUSB	3.07	200mA	3.07V
LDO from VS1	VRF18	1.81	450mA	1.81V
	VMIPI	1.71/1.8/1.84	300mA	1.84V
	VCN18	1.8	300mA	1.8V
	VCAMD	1/1.05/1.1/1.2/1.3/1.5/1.8	600mA	1.2V
	VCAMIO	1.8	300mA	1.8V
	VIO18	1.8	700mA	1.8V
LDO from VS2	VRF12	1.2	800mA	1.2V
	VA12	1.2	300mA	1.2V
	VSRAM_PROC11	0.6~1.2	600mA	1.2V
	VSRAM_OTHERS	0.55~1.2	600mA	0.9V
	VSRAM_GPU	0.65~1.2	600mA	0.9V
	VDRAM2	0.6/1.8	600/100mA	NO USE
	VSRAM_PROC12	0.6~1.2	600mA	1.2V



Schematic design notice of "21_POWER_MT6358-LDO" page.

Note 21-1: Please set SH2103 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
Please also refer to MT6358 design notice for further detail design information

Note 21-2: If these power trace can meet LDO layout constraint, these CAP can be NC or removed.
Please refer to MT6358 design notice.

Title	21_POWER_MT6358_LDO	
Size D	Project	Rev V1
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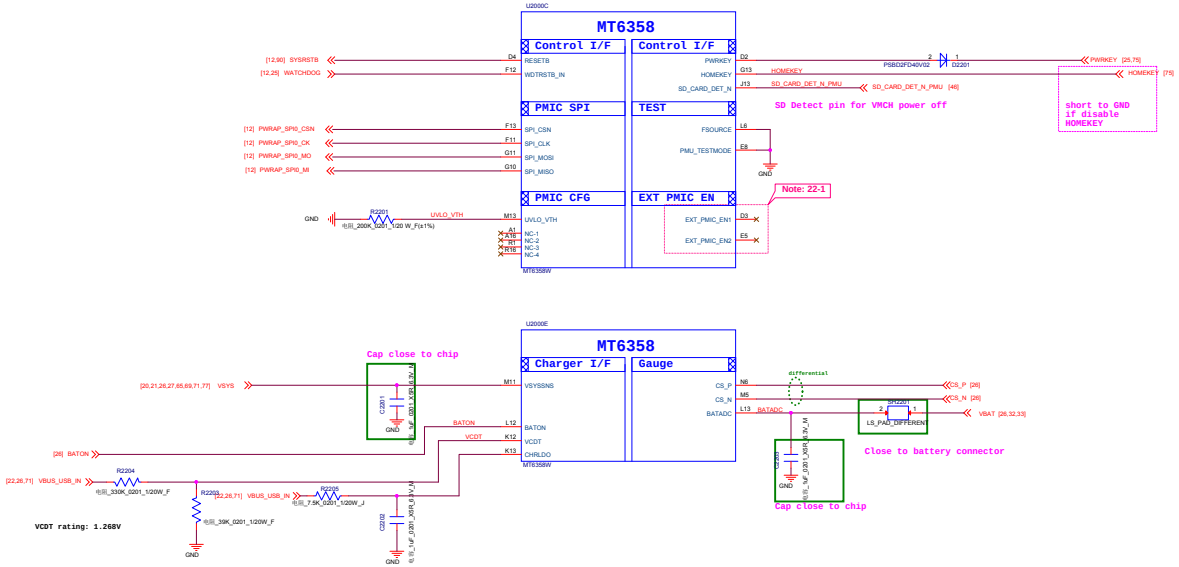
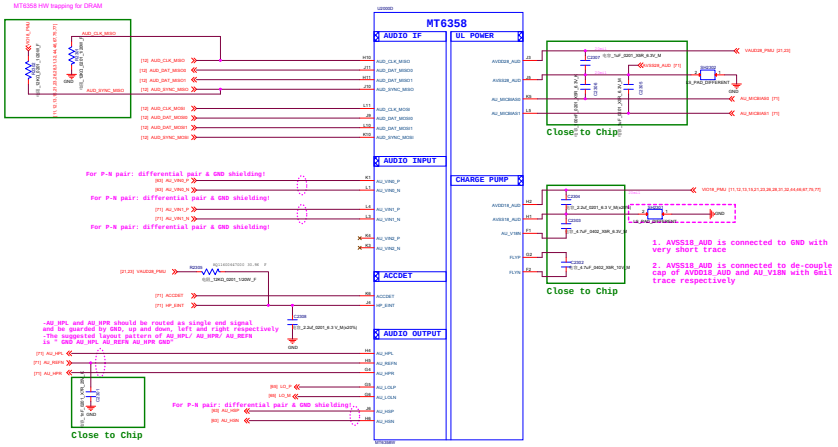


Schematic design notice of "22_POWER_MT6358-General"

Note 22-1: EXT_PMIC_EN1 : For UFS_1V8, and keep floating if it is not used
EXT_PMIC_EN2 : For VA09 of SSUSB/UFS, and keep floating if it is not used

Please connect to battery connector

Title	22_POWER_MT6358_IF	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 22 of 99	

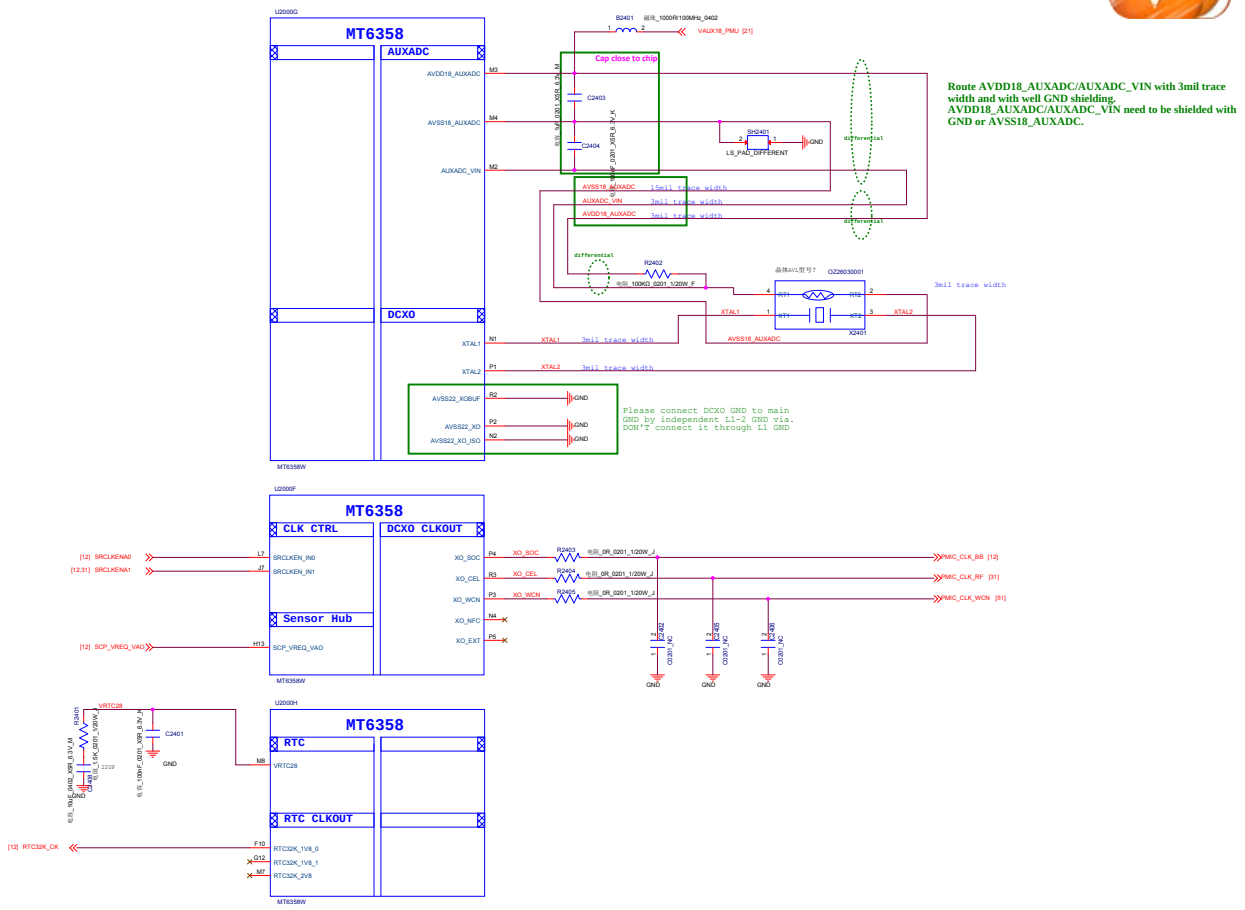


Schematic design notice of "23_POWER_MT6358-Audio"

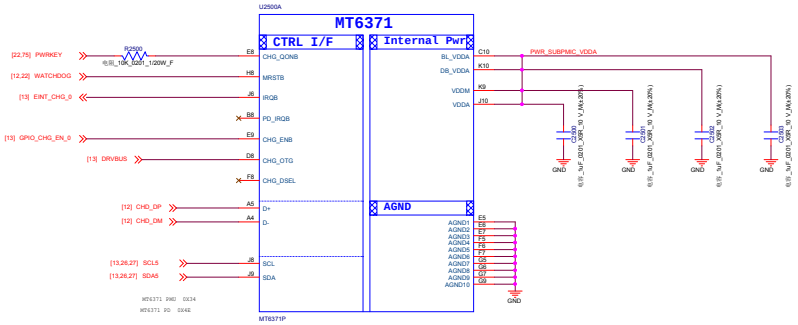
Note 23-1: VDRAM 2 / VDRAM1 output voltage vs. trap pin.

HW GPIO configuration		Trapping Option		DRAM type	VDRAM2 Power source (VS2_LDO1_ball)
AUD_SYNC_MISO	AUD_CLK_MISO	VDRAM1	VDRAM2		
0	0	1.125V	0.6V	LP4X	VDRAM1
0	1	OFF	1.8V	LP4X (Ext x 2 EN)	VS1
1	0	1.225V	OFF	LP3	VDRAM1
1	1	1.125V	1.8V	LP4X (Ext x 1 EN)	VS1

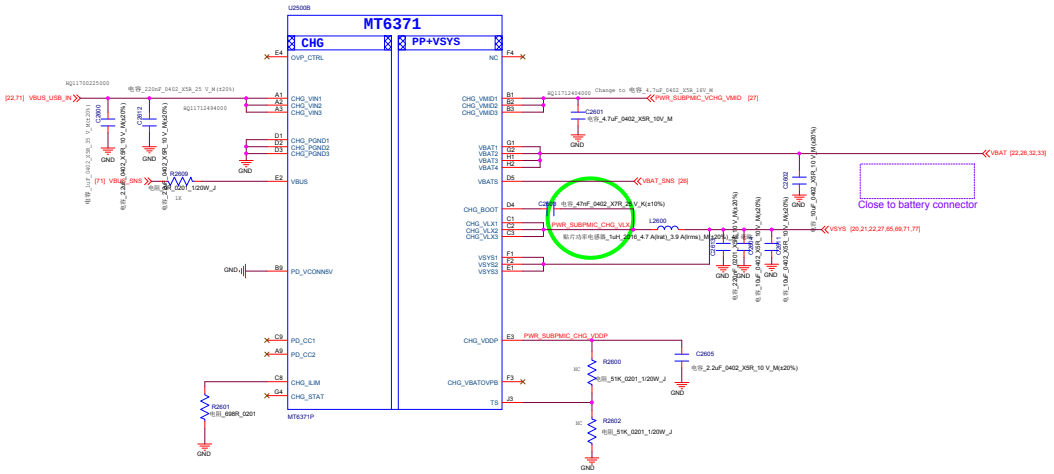
Title	23_POWER_MT6358_Audio	
Size E	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 23 of 99	

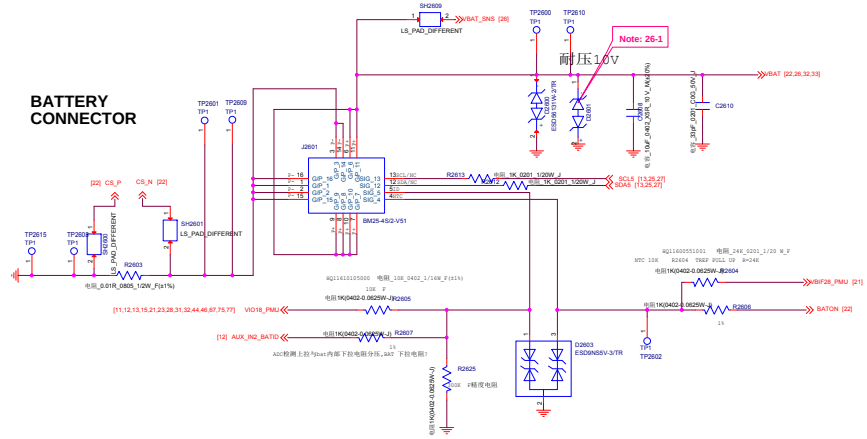


Title	24_POWER_MT6358_Clock	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 24 of 99	



Title	25_POWER_MT6370-General	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 25 of 99	

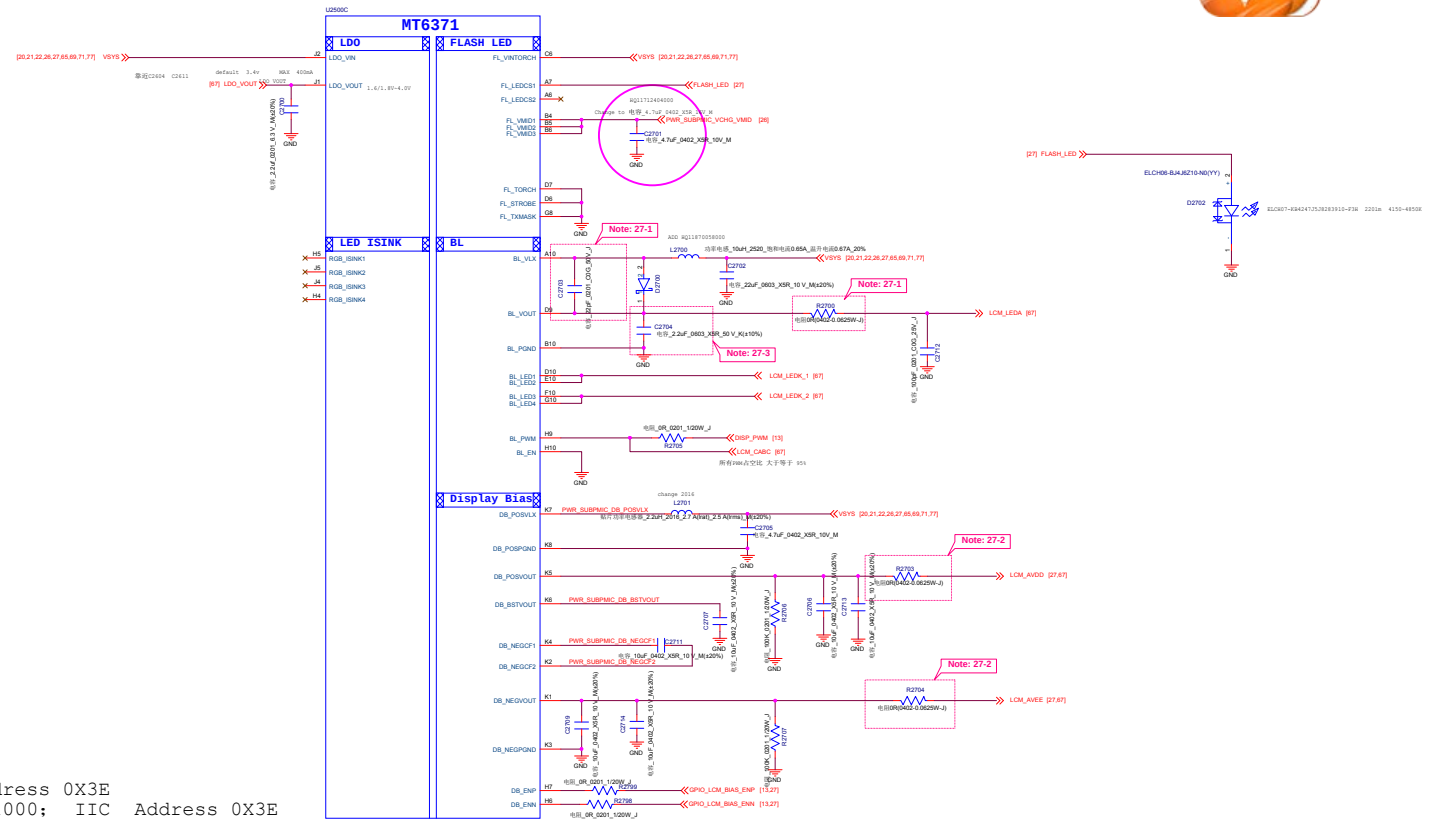




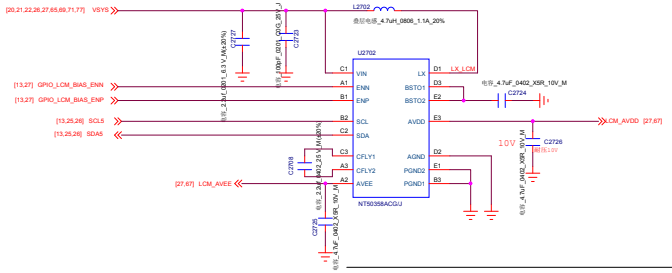
Schematic design notice of "26_POWER_MT6370-Charger + PP" page.

Note 26-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

Title	26_POWER_MT6370-Charger + PP	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 26 of 99	



主供NT50358　　IIC　Address 0X3E
二供SM5109　HQ11150971000;　IIC　Address 0X3E



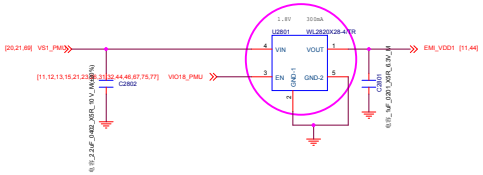
Schematic design notice of "27_POWER_SubPMIC-HV powers" page.

Note 27-1: It is recommended to reserve 0-ohm and cap. for BOM fine tune to minimize RF de-sense.

Note 27-2: It is recommended to reserve 0-ohm for BOM fine tune to minimize RF de-sense.

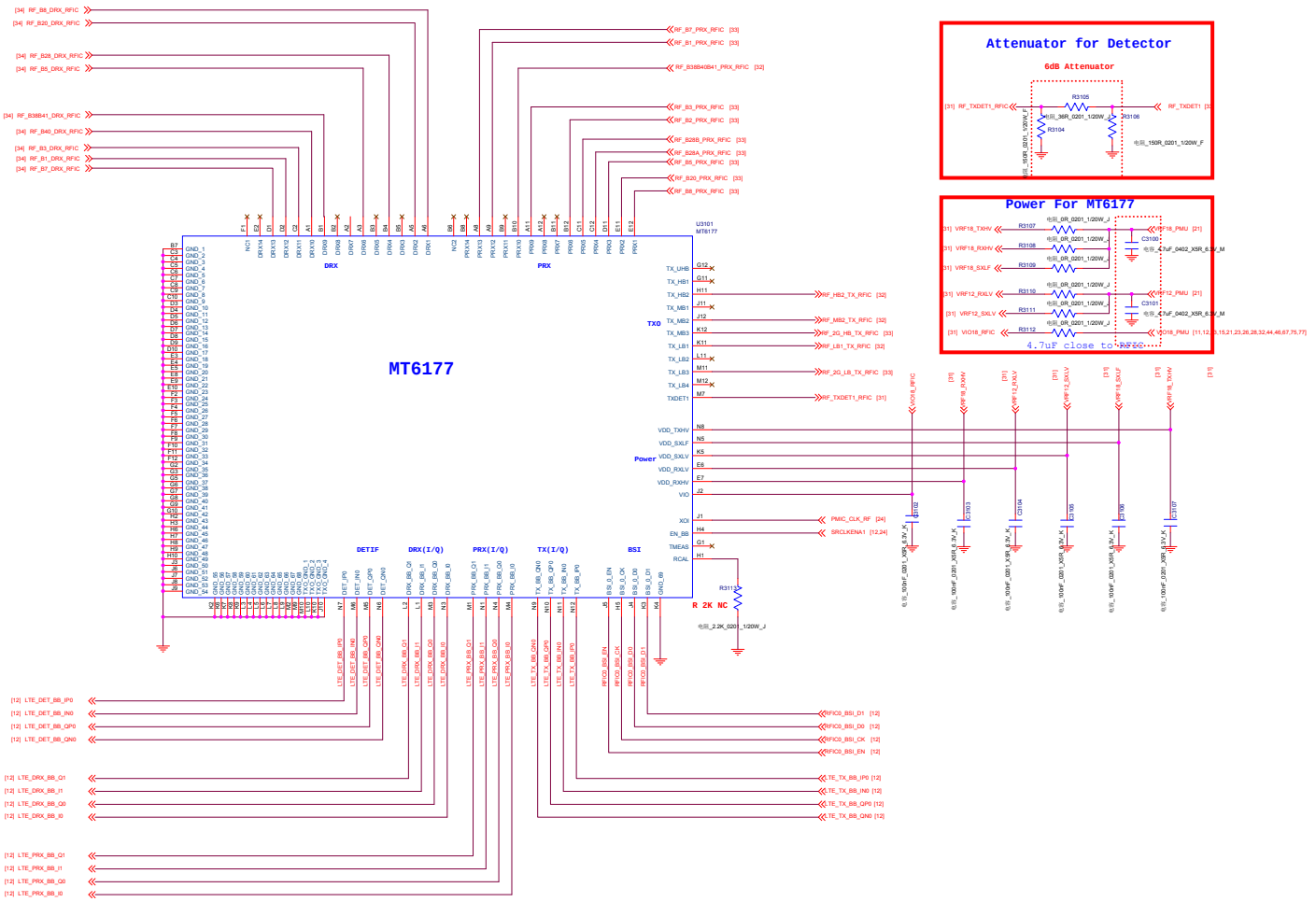
Title	27_Driver+-5V/flash	
Size D	Project 27_POWER_MT6370-HV powers	Rev V1
Date:Tuesday, November 13, 2018	Sheet 27 of 99	

LDO for EMI_VDD1 of LPDDR3 VDD1



Title	28_POWER_ThirdParty_Powers	
Size D	Project	Rev V1
Date: Tuesday, November 13, 2018	Sheet 28 of 99	

PRX/DRX 1-8 For LB/MB:600M-2025M
PRX/DRX 9-12 For HB/MB:1805M-2690M



Title	31_RF_MT6177_Pin_Out		
Size D	Project	_MB_V1	Rev V1
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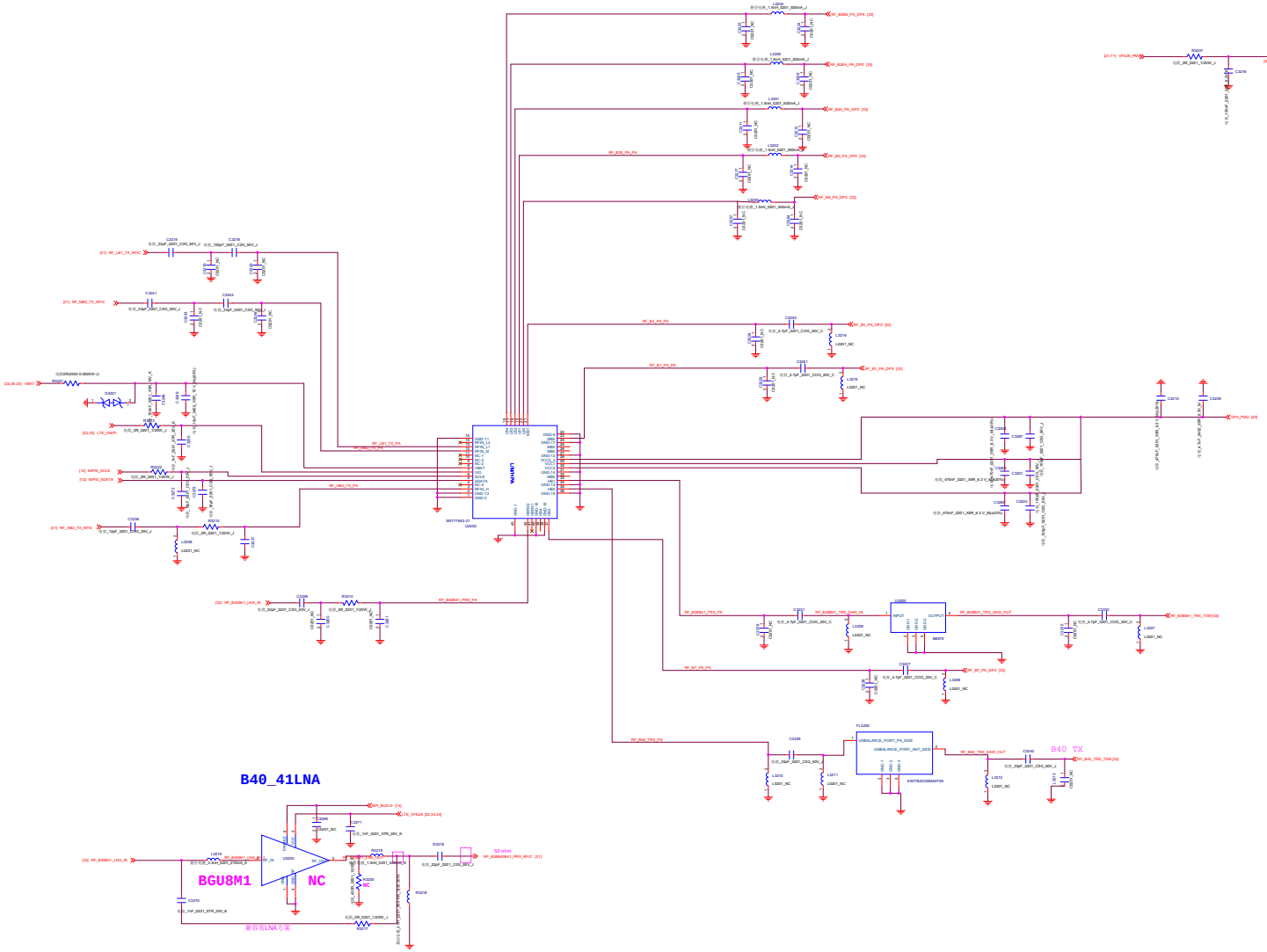
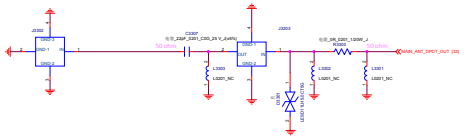
PA & PA THERMAL

REF 3401-3499



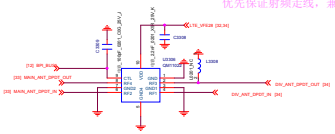
Title	32_RF_MT6177_RF_TX		
Size E	Project	_MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 32 of 99		

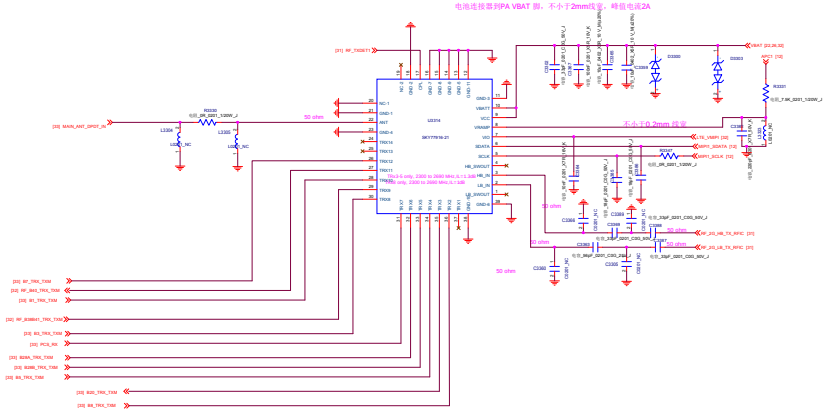
TXM_GSM



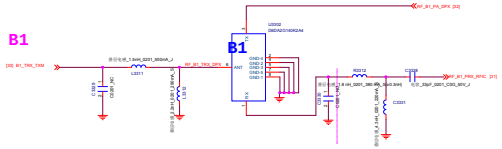
DPDT SWITCH

优先保证射频走线，兼容通路，不要有断头线

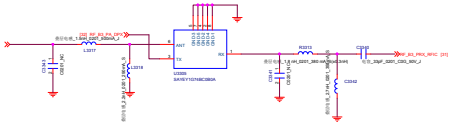




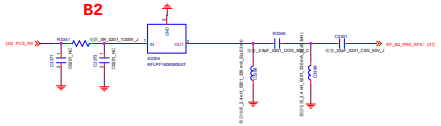
B1



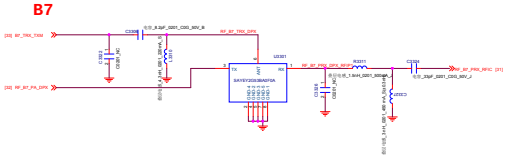
B3



B2

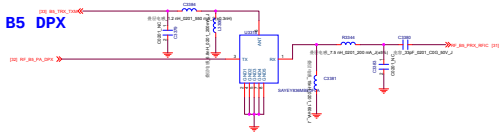


B7

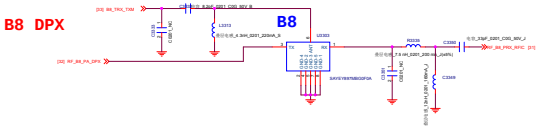


B5

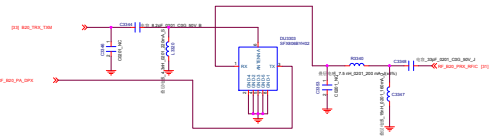
B5 DPX



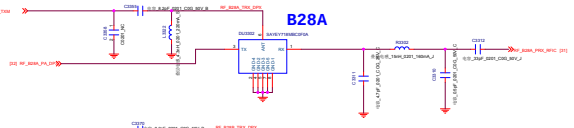
B8 DPX



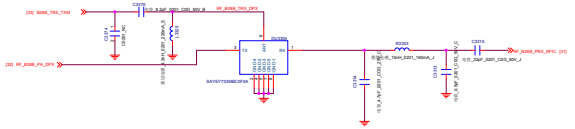
B20



B28A

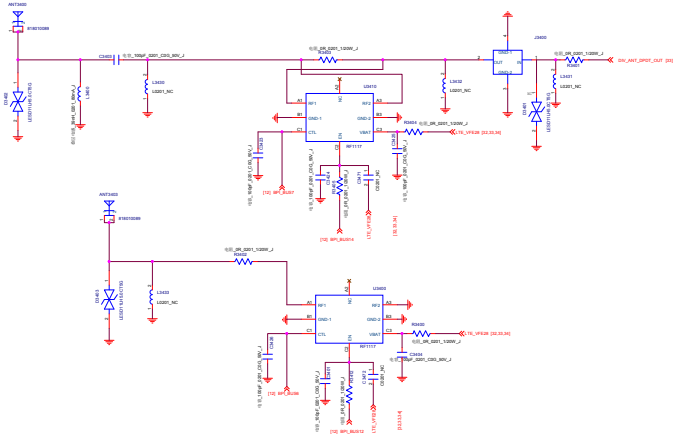


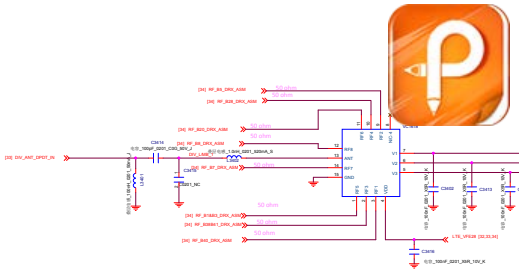
B28B



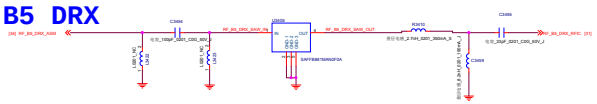
Title	33_RF_MT6177_RF_PRX		
Size E	Project	_MB_V1	Rev V1
Date: Tuesday, November 13, 2018		Sheet 33 of 99	

DIV_ANT

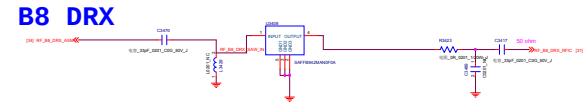




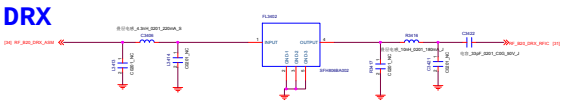
B5 DRX



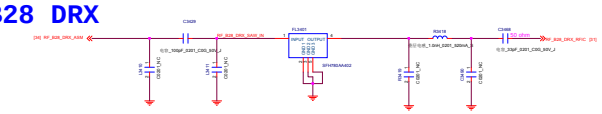
B8 DRX



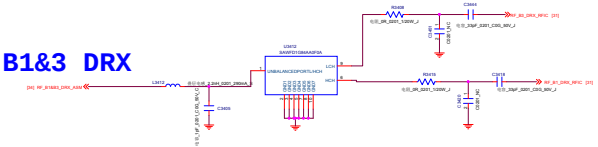
B20 DRX



B28 DRX

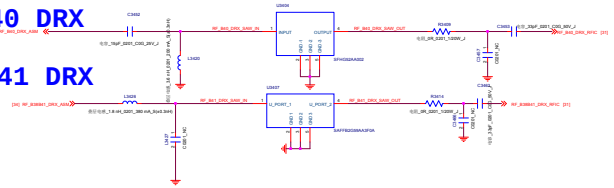


B1&3 DRX

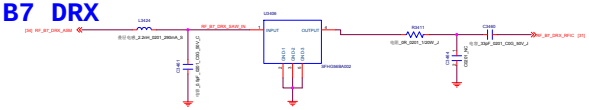


B40 DRX

B38/B41 DRX



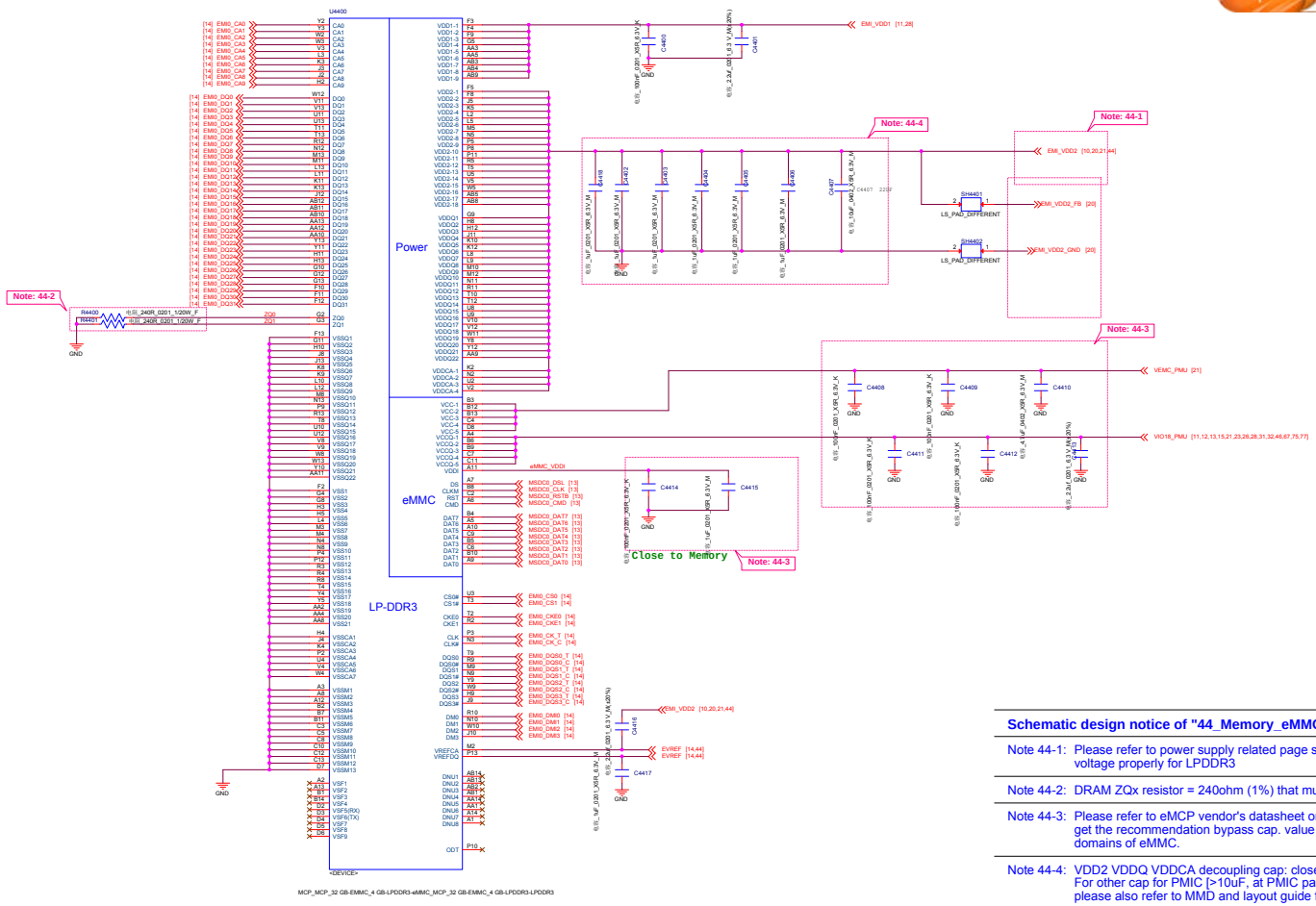
B7 DRX



Title	34_RF_MT6177_RF_DRX		
Size E	Project	_MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 34 of 99		

Title	35_RF_eLNA	
Size C	Project _MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 35 of 99	

Title	36_RF_ANT	
Size C	Project _MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 36 of 99	



Schematic design notice of "44_Memory_eMMC_LPDDR3"

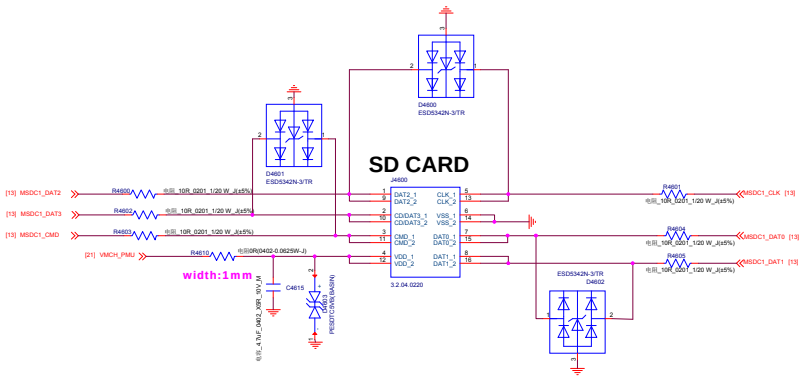
Note 44-1: Please refer to power supply related page select VDRAM1 output voltage properly for LPDDR3

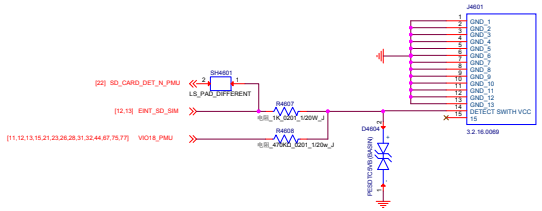
Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to GND

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

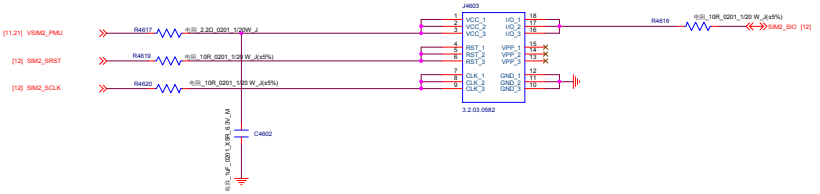
Note 44-4: VDD2 VDDQ VDDCA decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

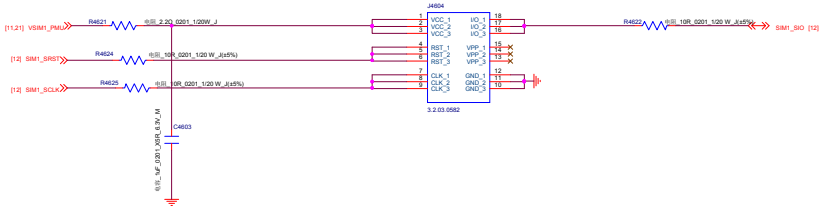
Title	44_Memory_eMMC_LPDDR3	
Size D	Project _MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 44 of 99	





SIM1/SIM2

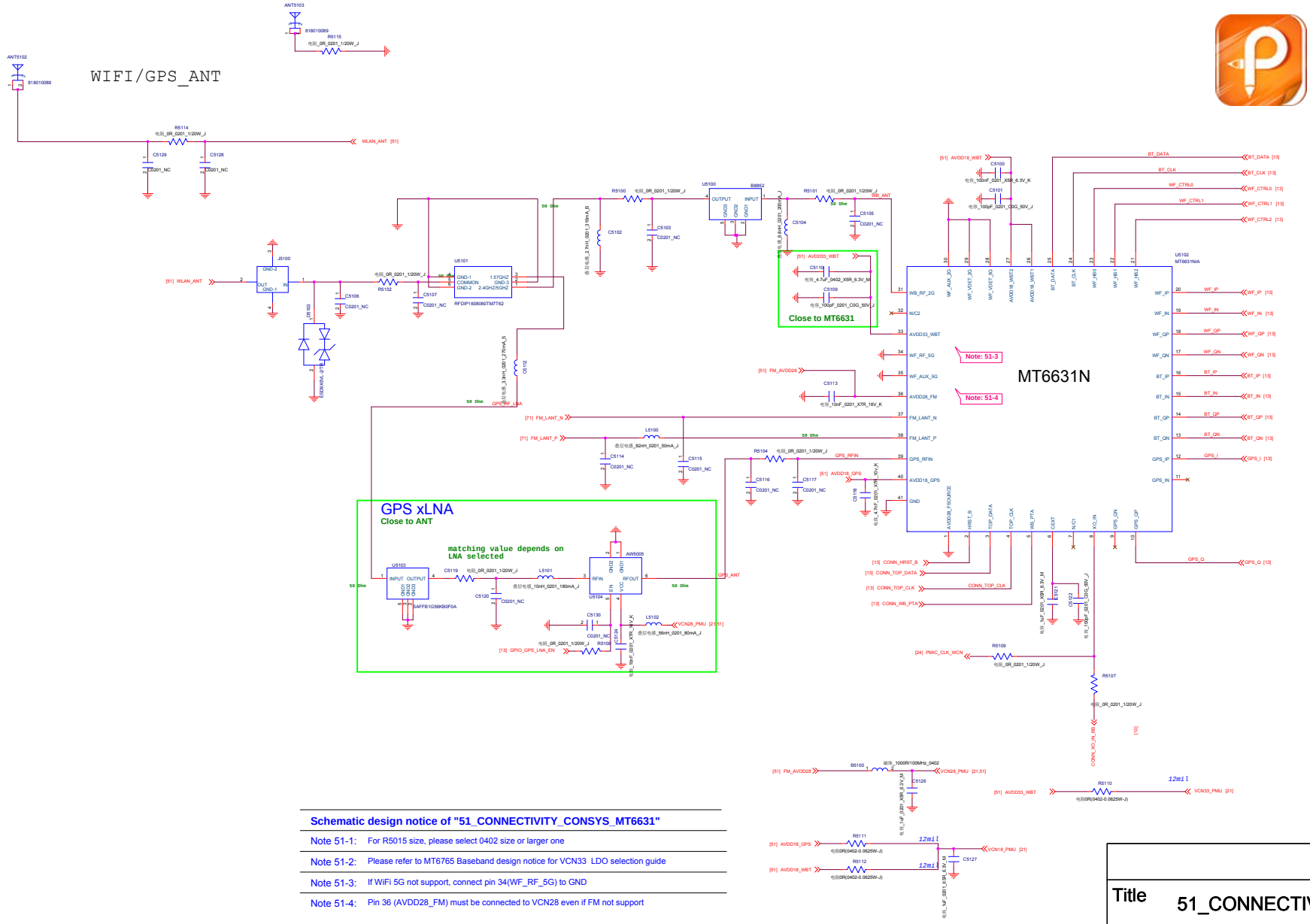




Schematic design notice of "46_MEMORY_SD Card" page.

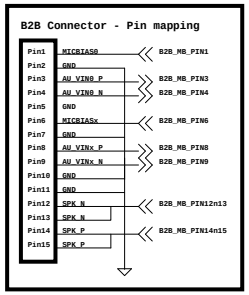
Note 46-1: For better ESD performance, please select suitable components for system protection.

Title	46_Memory_SD	
Size D	Project _MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 46 of 99	

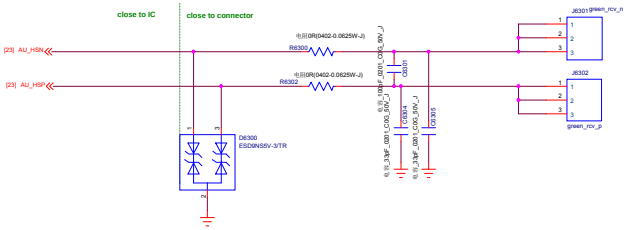


Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"	
Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6765 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support

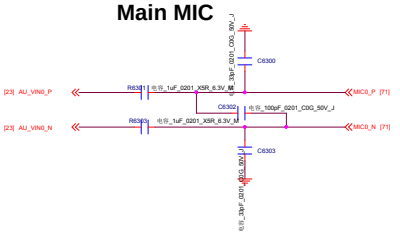
Title	51_CONNECTIVITY_CONSYS_MT6631	
Size D	Project _MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 51 of 99	



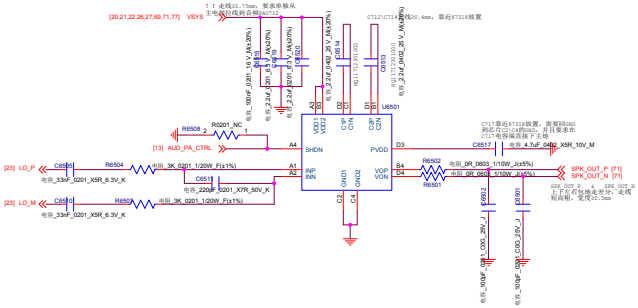
Receiver



Main MIC

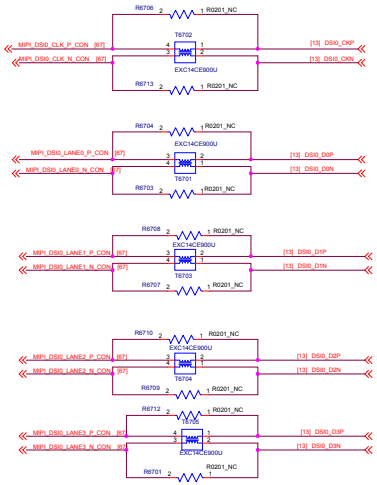


Title	63_PERI_AUDIO_IO2(2 AMIC)	
Size D	Project _MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 63 of 99	



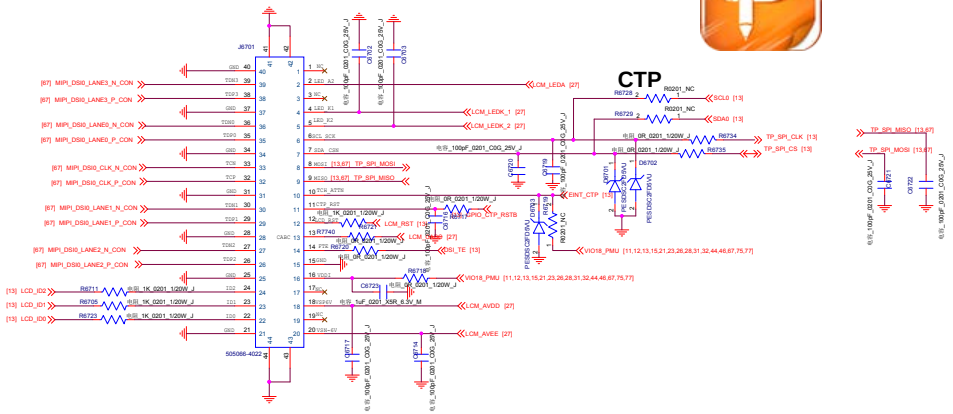
Title	65_PERI_SPEAKER_AMP		
Size D	Project	_MB_V1	Rev V1
Date: Tuesday, November 13, 2018		Sheet 65 of 99	

LCD MIPI Common Mode Filter

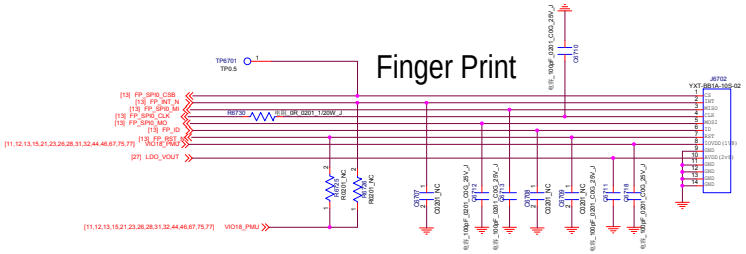


First using 0R ,Second using EMI Filter.

Main LCM+CTP INCELL



Finger Print

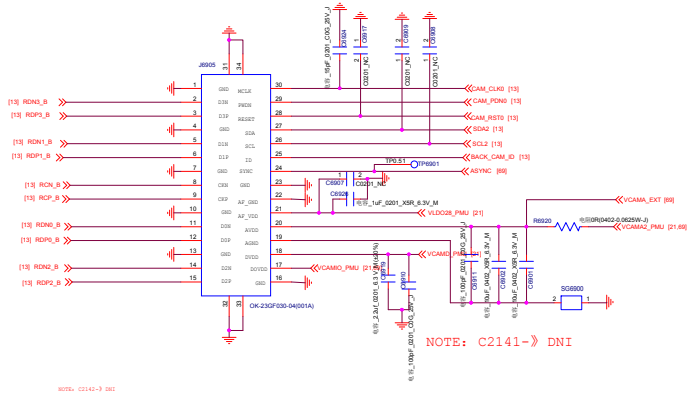


Title	67_PERI_LCD_CTP_FP		
Size D	Project	_MB_V1	Rev V1
Date: Tuesday, November 13, 2018		Sheet 67 of 99	

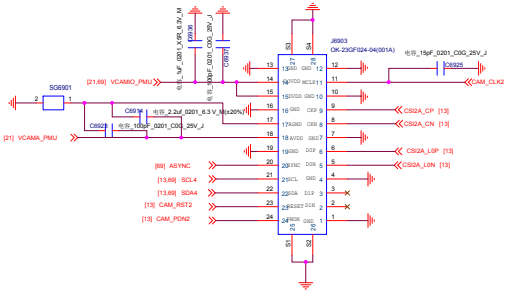
Dual cam

Rear Camera

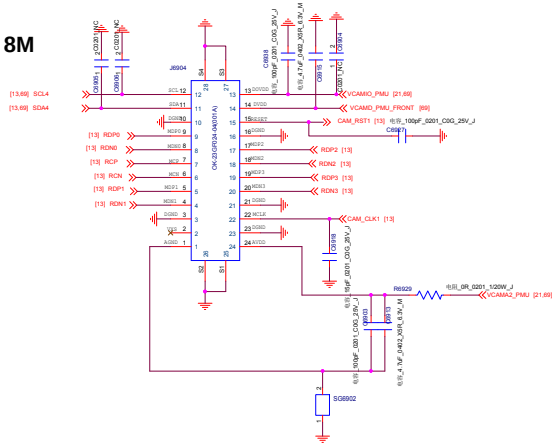
注意：AGND AFGND都要单独下主地

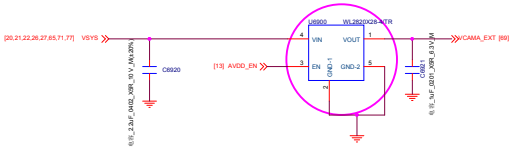


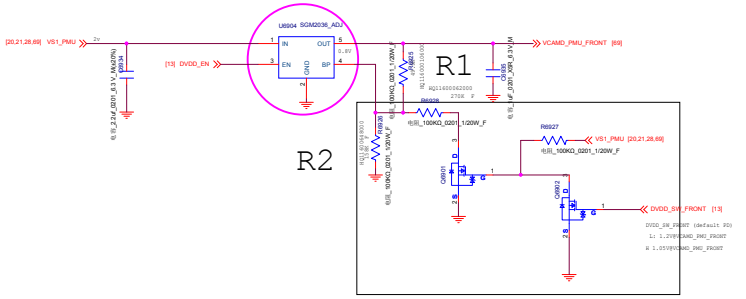
Rear Camera 2



Front Camera - 8M







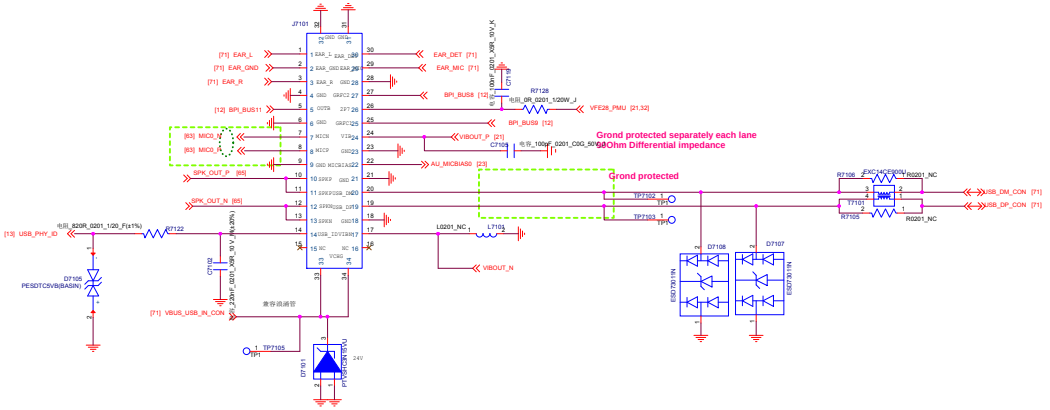
VOUT=0.8X(1+R1/R2)

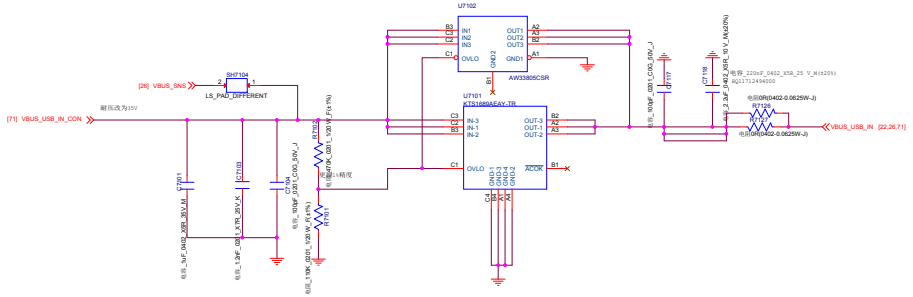
Title	69_PERI_CAMERA		
Size D	Project	_MB_V1	Rev V1
Date: Tuesday, November 13, 2018		Sheet 69 of 99	

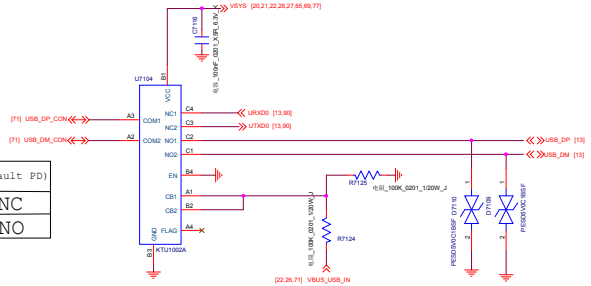
Schematic design notice of "71_PERI_USB 2.0" page.

Note 71-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

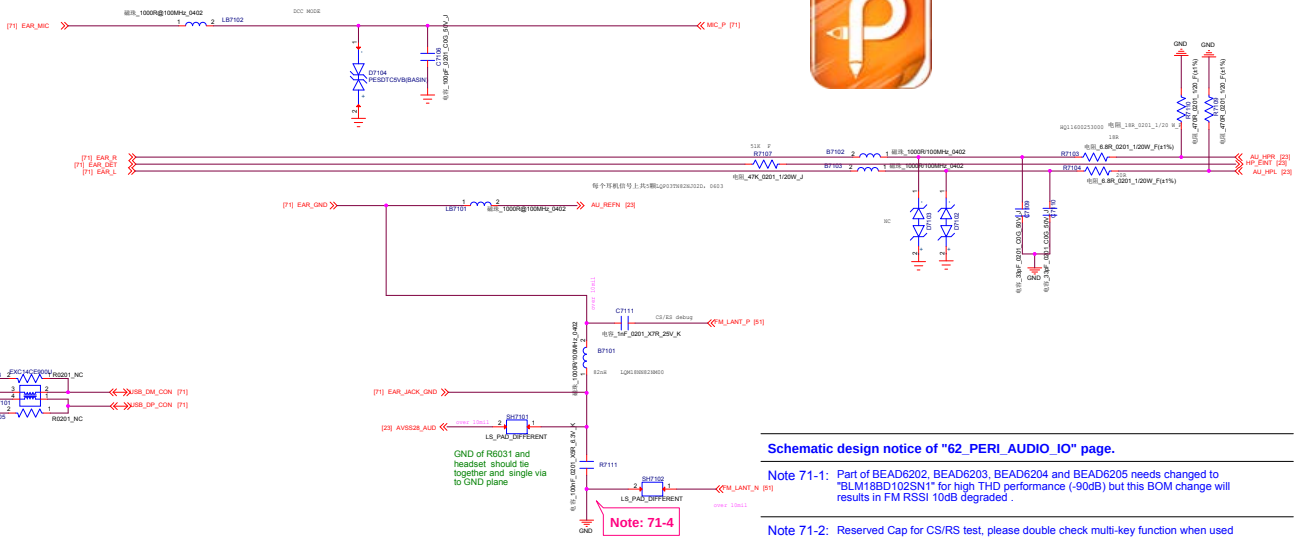
BTB Connector







CB	SELECT(default PD)
0	COM=NC
1	COM=NO



Schematic design notice of "62_PERI_AUDIO_IO" page.

Note 71-1: Part of BEAD6202, BEAD6203, BEAD6204 and BEAD6205 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

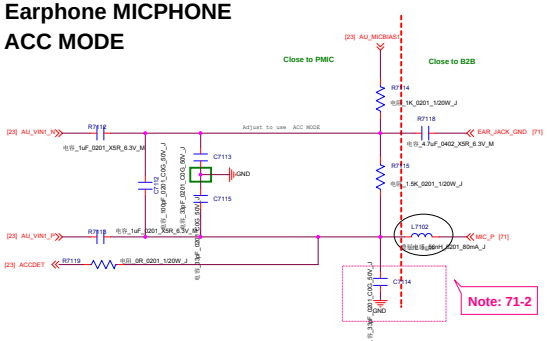
Note 71-2: Reserved Cap for CS/RS test, please double check multi-key function when used

Note 71-3: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

Note 71-4:

	Earphone Jack @ Main board	Earphone Jack @ Sub board
R7111	0 ohm	100nF

Earphone MICPHONE ACC MODE



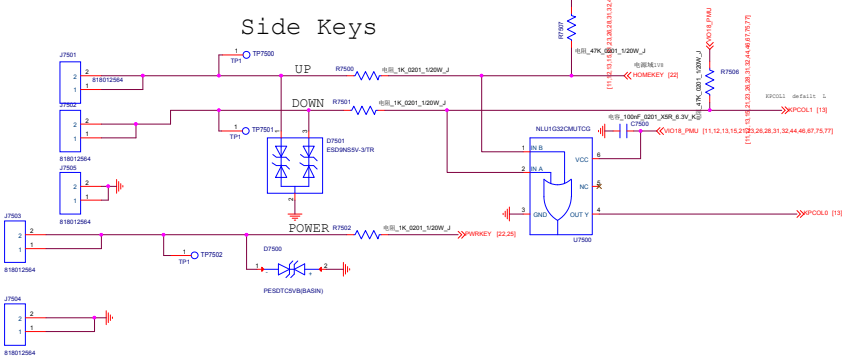
Platform	MT6357	
Mode	ACC mode	DCC mode
EINT	HP_EINT	HP_EINT
Key-Detection	ACCDET	AU_VIN1_P
R7112	1uF	0 ohm
R7113	1uF	0 ohm
R7114	1K	NC
R7115	1.5K	NC
R7116	NC	2.49K
R7118	4.7uF	0 ohm
R7119	0 ohm	NC
R7107	47K ohm	47K ohm

Title	71_B2B_OVP	
Size D	Project _MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 71 of 99	

Power Key / Key Pad

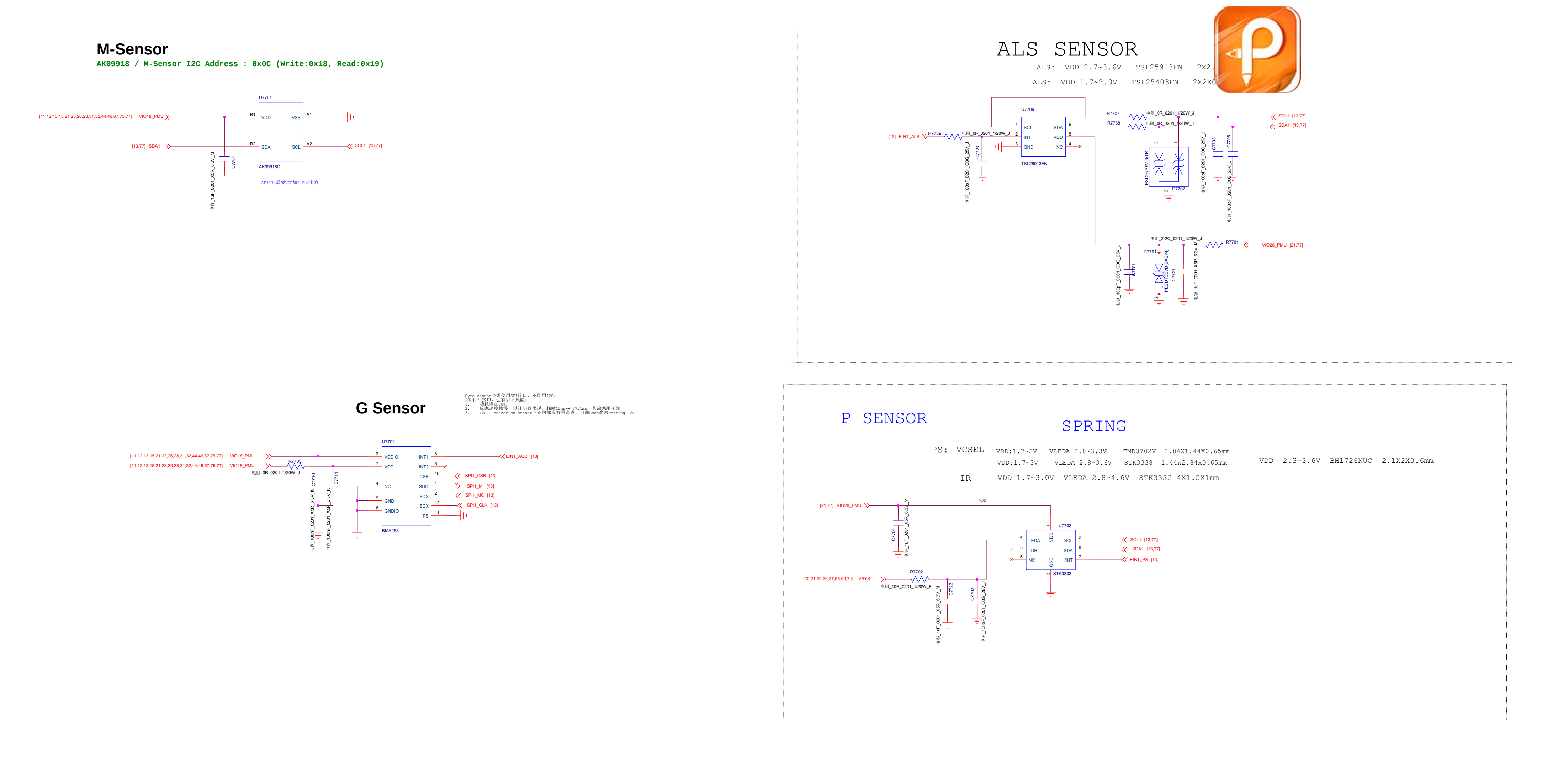
DO NOT put pull-up resistor on PWRKEY

Keys



Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.	
Note 75-1:	DO NOT put pull-up resistor on PWRKEY
Note 75-2:	Volume Up : HOME Key / GND Volume Down : KPROW0/KPCOL0
Note 75-3:	For better ESD performance, please select suitable components for system protection.

Title	75_PERI_KEYPAD	
Size D	Project _MB_V1	Rev V1
Date: Tuesday, November 13, 2018	Sheet 75 of 99	



Title	77_PERI_SENSORS_MEMs_ALS/PS
Size D	Project _MB_V1
Rev	V1
Date:	Tuesday, November 13, 2018
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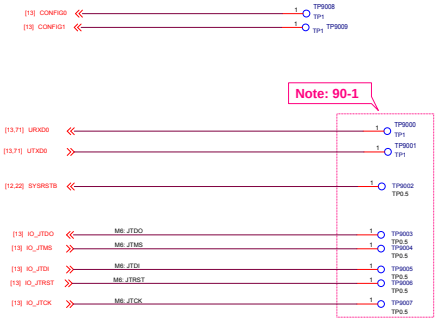

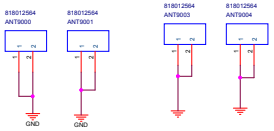

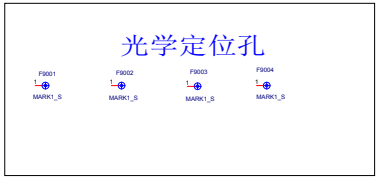

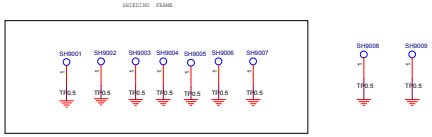

Schematic design notice of "90_DEBUG_IO" page.

Note 90-1: UART Default support : UART0,
JTAG Default support : AP JTAG, MD_IO_JTAG and C2K_JTAG concurrency with MD_SIB_JTAG

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1, 增加DVDD_core反馈PIN
2, 增加R2799,R2798
3, EMI器件T6702,T6705,T7101，为走线顺畅，上下翻转------0908
4, BTB的VBUS大电源PIN旁边不能有地PIN和信号PIN；调整Vbus旁边的信号网络-----0908
5, 更改TP1测试点的网络连接-----0908
6, 增加PWR_SUBPMIC_VBATS网络连接-----0909
7, 更新 LDO U6900的输出VCAMA_EXT的网络连接-----0909
8,C2306更新100nF -----0910
9, 删去C6704 ---0911
10, R6300/2由R0201变更为R0402封装 ---0911
11,J6301/2 变更库封装 ---0911
12,删去R4405 ---0913
13,增加C7723 100PF ---0913
14, C2701更换为25V库 ---0913
15 ,C2004更换为0402 10UF ---0914
16 ,删去R2202_0915
17 ,删去D2704_0916
18.指纹识别SPI口更改为SPI0
19.更改B7 TRX口位由14到13口位，减小通道插损
20.依据客户意见，更改天线地点匹配设计。
21.增加TP6701测试点。
22,C1021/C1004/C1018变更为0402 22UF电容
23,F9001,F9002,F9003,F9004 激光定位点变更菱形库。--0918
24.C2600 换成1UF 0402 35V
25 ,C2601 C2701换C0402 16V电容封装--0919
26 ,C2724 换C0402 4.7uF --0919
27 ,增加SH9008,SH9009,SH9010 罩子及挡筋 --0919
28 ,删去SH9010 罩子 --0920
29,更新L2002,J4601 PCB FOOTPRINT --0920
30,断开J6301 3 pin与REC_N连接 --0920

V3.0

31.修改DRXB40,B41,B1,B3,B7口位
32.修改主集B7 TRX口位变更到TRX12
33, 删去USB/UART CTRL SW网络
34 ,兼容WSA3218与KTU1002设计，量产采用WSA3218
35, D7107/8,D7109/10放置于T7101（R7105/6)前面
36, Config 0/1各增加R1335/6 100K上拉
37, AUD_PA_CTRL上增加一颗R6508 0201 NC电阻
38,TP9000/1改为1.0测试点
39 ,删去TP7100 USB OTG 测试点

V4.0

40, 增加C2308电容 （优化HP_EINT插耳机座POP音）
41, C6304/5与D6300交换位置(增强耦合TDD抑制能力）
42, R7109/R7110靠近PMIC放置（优化耳机电性能）
43, 增加C2613 0201 220nf 10V电容 （USB_ID)
44,C2612更改为0402 220nf 25V电容
45,增加R7126 R7127 和C7117 C7118 （充电干扰）
46,增加R6929 0201（前摄DESENSE）
47,更改J6301 3 PIN (库修改）
48, D7109/10更改到靠近CPU端
49,增加WIFI / GPS天线兼容设计，增加位号R5116,R5117,R5118,C5131,C5132。
50, 删除R5116, 小板端2.8V供电VFE28_PMU增加LC网络就，增加R7128 , C7119.
50, 增加D7111/2(预留CD方案）。

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V5.0

51, OVP更改为独立IC方案，不用WS3218

52, 更改K6L IIC上拉电源域为VCAMIO_PMU，规避漏电问题

53, 增加C6723 1uF 0201电容

54, 增加D3303预留位置

55, 增加C1304 C1305

56, 删去R3346

57, 删去C5131 C5132 R5116 R5117

58, 删去TP9010 TP1301

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