OPT3101 ToF based Long Range Proximity and Distance Sensor AFE

1 Features

- Proximity Sensing and Distance Measurement
- Compatible With a Wide Variety of Photodiodes and Emitters
- 16-bit Distance Output at 15-m Unambiguous Range
- Sample Rate up to 4 kHz
- 200-nA Full-Scale Signal Current
- 88-dB Signal Phase Dynamic Range at 1 kHz
- Supports DC Ambient up to 200 µA, 60-dB Rejection for Ambient at 1 kHz
- Object Reflectivity Independent Distance Measurement
- De-Aliasing to Extend the Distance Range up to 75 m
- Programmable Sequence Generator to Provide Timing Flexibility
- Adaptive HDR to Save Power and Extend the Distance Range
- Configurable Event Detection and Interrupt Output Mechanism
- I^2C Interface for Control and Data
- Integrated Illumination Driver with Programmable Current Control up to 173.6 mA
- Integrated Temperature Sensor for Calibration
- Built-in Crosstalk Calibration
- I^2C Host to Auto Load Register Settings From External EEPROM on Reset
- Typical Power: 25 mW at 100 Hz, Including Illumination Power
- 4 mm × 5 mm, 28-Pin VQFN Package
- Single 3.3-V or 1.8-V and 3.3-V Supply Operation
- Operating Temperature: –40 to +85°C

2 Applications

- Proximity Sensing
  - Kiosk Customer Presence and Behavior Detection
  - Automated Dispensing
  - Car Parking Meter
- Long Range Sensing
  - Obstacle Detection for Autonomous Vehicles
  - Industrial Object Counting
  - Range Finder

3 Description

The OPT3101 device is a high speed, high resolution AFE for continuous wave, time-of-flight based proximity sensing and range finding. The device integrates the complete depth processing pipeline that includes the ADC, timing sequencer, and the digital processing engine. The device also has a built-in illumination driver that covers most of the target applications.

Given the high ambient rejection ratio, the device can support very high ambient conditions, including full sunlight of 130 klux.

The timing sequencer is highly configurable to provide for application-specific trade-offs of power versus performance.

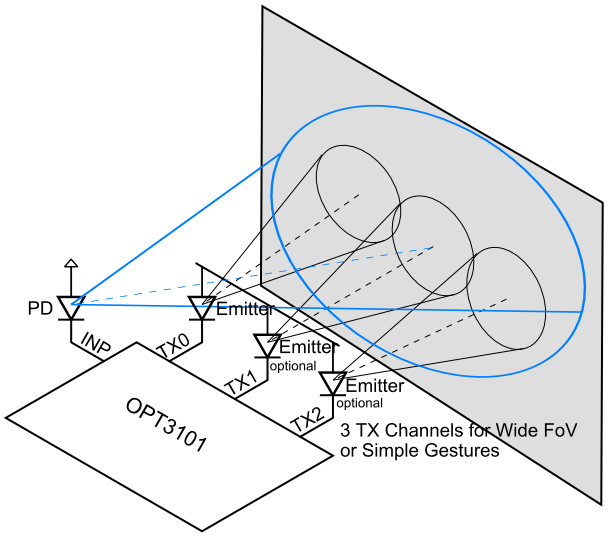
The device provides depth data that consists of phase, amplitude, and ambient measurements. The calibration subsystem supports phase data calibration for inaccuracies resulting from temperature and crosstalk

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPT3101	VQFN (28)	5 mm × 4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Block Diagram



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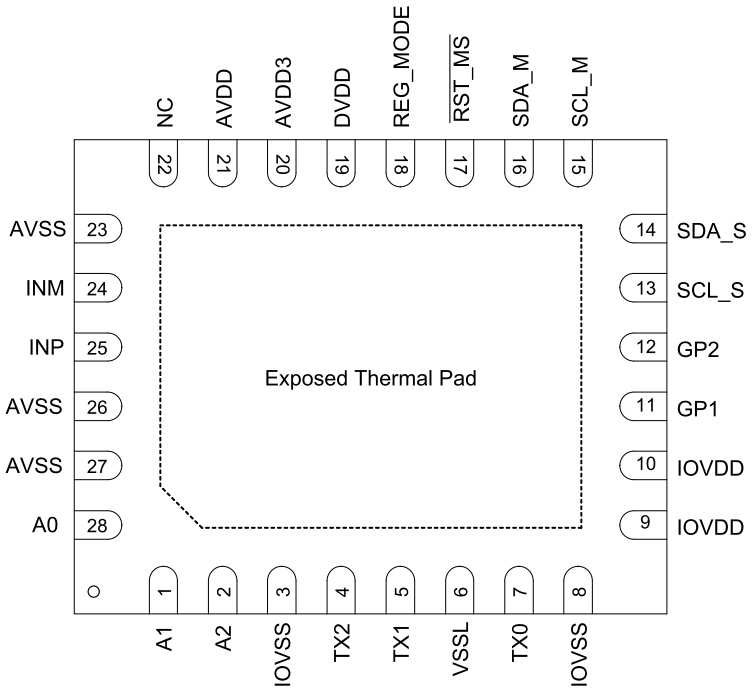
4 Revision History

DATE	REVISION	NOTES
February 2018	*	Advance Information.

5 Pin Configuration and Functions

(RHF Package)
(28-Pin VQFN)
Top View



Pin Functions

PIN		TYPE	I/O VOLTAGE DOMAIN	DESCRIPTION
NAME	NO.			
A0	28	I	AVDD	I^2C slave LSB0 address bit
A1	1	I	AVDD	I^2C slave LSB1 address bit
A2	2	I	AVDD	I^2C slave LSB2 address bit
AVDD	21	Power	—	1.8-V analog supply
AVDD3	20	Power	—	3.3-V analog supply
AVSS	23, 26, 27	—	—	Analog ground
DVDD	19	Power	—	1.8-V digital supply
GP1	11	O	IOVDD	General purpose output
GP2	12	I/O	IOVDD	General purpose output, CLKREF input
INM	24	Analog Input	AVDD	ADC negative input. Connect photodiode equivalent capacitance. Other end of the capacitor should be connected to ground AVSS.
INP	25	Analog Input	AVDD	ADC positive input. Connect photodiode cathode. Anode of the photodiode should be connected to ground AVSS.
IOVDD	9, 10	Power	—	Supply for I/O and illumination driver
IOVSS	3, 8	—	—	Ground for digital and I/O
NC	22		—	
REG_MODE	18	I	IOVDD	Mode to select internal regulator for 1.8-V supplies (AVDD, DVDD)
$\overline{\text{RST\_MS}}$	17	I	IOVDD	Active low global reset, monoshot trigger.
SCL_M	15	O	IOVDD	I^2C master clock. Connect with a 10-kΩ resistor to a 3.3-V supply.
SCL_S	13	I	IOVDD	I^2C slave clock. Connect with a 10-kΩ resistor to a 3.3-V supply.
SDA_M	16	I/O	IOVDD	I^2C master data. Connect with a 10-kΩ resistor to a 3.3-V supply.
SDA_S	14	I/O	IOVDD	I^2C slave data. Connect with a 10-kΩ resistor to a 3.3-V supply.

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Pin Functions (continued)

PIN		TYPE	I/O VOLTAGE DOMAIN	DESCRIPTION
NAME	NO.			
TX0	7	O	IOVDD	Illumination driver output. Connect to LED cathode. Anode should be connected to a supply.
TX1	5	O	IOVDD	Illumination driver output. Connect to LED cathode. Anode should be connected to a supply.
TX2	4	O	IOVDD	Illumination driver output. Connect to LED cathode. Anode should be connected to a supply.
VSSL	6	—	—	Illumination driver ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
IOVDD	Digital I/O supply	–0.3	4	V
AVDD3	Analog supply	–0.3	4	V
AVDD	Analog supply	–0.3	2.2	V
DVDD	Digital supply	–0.3	2.2	V
V_I	Input voltage at input pins	–0.3	VCC + 0.3 (2)	V
T_J	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VCC refers to the I/O bank voltage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IOVDD	Digital I/O supply	1.7	1.8 to 3.3	3.6	V
AVDD3	Analog supply	3	3.3	3.6	V
AVDD	Analog supply	1.7	1.8	1.9	V
DVDD	Digital supply	1.7	1.8	1.9	V
V_{DRV}	TX0, TX1, TX2 pin voltage	0.7		3.6	V
T_A	Ambient temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC (1)		OPT3101 RHF (QFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

All specifications at T_A = 25°C, VAVDD = 1.8 V, VAVDD3 = 3.3 V, VDVDD = 1.8 V, VIOVDD = 3.3 V, IambMax = 20 µA, Photodiode with a capacitance of 2 pF at AFE input unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AFE						
I_{ref}	Full scale signal current at F_{mod}			200		nA
I_{noise}	AFE Input refered current noise			1.5 (1)		pA/√Hz
I_{ambMax}	Maximum ambient DC current at input	AVDD3 = 3.3V		200 (2)		µA
μ_{1000Hz}	Ambient attenuation at 1000 Hz			60		dB
V_R	Bias voltage at INM, INP			1		V
C_{in}	Maximum external photodiode capacitance at input			6		pF
F_{mod}	Modulation frequency			10		MHz
sps	Sample rate				4000	Hz
$tPU_{Deepsleep}$	Deep sleep recovery time	Monoshot mode Only		1		ms
$tPU_{Standby}$	Standby recovery time (3)			50		µs
ILLUMINATION DRIVER						
I_{DRV}	Maximum built-in illumination driver current			173.6		mA
POWER (ACTIVE MODE AT MAXIMUM FRAME RATE)						
I_{AVDD}	1.8-V analog supply current			11.6		mA
I_{DVDD}	1.8-V digital supply current			5.7		mA
I_{AVDD3}	3.3-V analog supply current			0.5		mA
I_{IOVDD}	3.3-V I/O supply current			0.7		mA
POWER (DEEP SLEEP MODE)						
I_{AVDD}	1.8-V analog supply current			1		µA
I_{DVDD}	1.8-V digital supply current			3		µA
I_{AVDD3}	3.3-V analog supply current			1		µA
I_{IOVDD}	3.3-V I/O current			2		µA
POWER (ACTIVE MODE AT MAXIMUM FRAME RATE), INTERNAL LDO MODE						
I_{AVDD3}	3.3-V analog supply current	Internal LDO mode		17.9		mA
I_{IOVDD}	3.3-V I/O supply current	Internal LDO mode		0.7		mA
POWER (DEEP SLEEP MODE), INTERNAL LDO MODE						
I_{AVDD3}	3.3-V analog supply current	Internal LDO mode		80		µA
I_{IOVDD}	3.3-V I/O supply current	Internal LDO mode		2		µA
CMOS I/Os						
V_{IH}	Input high-level threshold		0.7 × VCC			V
V_{IL}	Input low-level threshold				0.3 × VCC	V
V_{OH}	Output high level	I_{OH} = –2 mA		(4) VCC – 0.45		V
		I_{OH} = –8 mA		(4) VCC – 0.5		
V_{OL}	Output low level	I_{OL} = 2 mA		0.35		V
		I_{OL} = 8 mA		0.65		
I_I	Input pin leakage current	Pins with pullup, pulldown resistor		±50		µA

(1) Noise will be higher by 20% with a photodiode capacitance of 6pF at AFE input.
(2) I_{ambMax} is programmable through register setting IAMB_MAX_SEL.
(3) Reference, Oscillator, Ambient Cancellation are not powered down.
(4) VCC is equal to IOVDD or AVDD, based on the I/O bank listed in the Pin Functions table.

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Electrical Characteristics (continued)

All specifications at T_A = 25°C, VAVDD = 1.8 V, VAVDD3 = 3.3 V, VDVDD = 1.8 V, VIOVDD = 3.3 V, IambMax = 20 µA, Photodiode with a capacitance of 2 pF at AFE input unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		Pins without pullup, pulldown resistor			±10	
C_I	Input capacitance			5		pF
I_{OH}	Maximum Output current high level			10		mA
I_{OL}	Maximum Output current low level			10		mA

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
RSTZ_MS Pin					
$t_{PWMonoShot}$	Monoshot trigger pulse width	0.1		1	µs
$t_{PWReset}$	Reset pulse width	30			µs
I^2C Slave					
f_{SCL}	I^2C slave SCL operating frequency			400	kHz

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6.7 Typical Characteristics

All specifications at T_A = 25°C, V_{AVDD} = 1.8 V, V_{AVDD3} = 3.3 V, V_{DVDD} = 1.8 V, V_{IOVDD} = 3.3 V, I_{ambMax} = 20 µA, Photodiode with a capacitance of 2 pF at INP/INM unless otherwise noted.

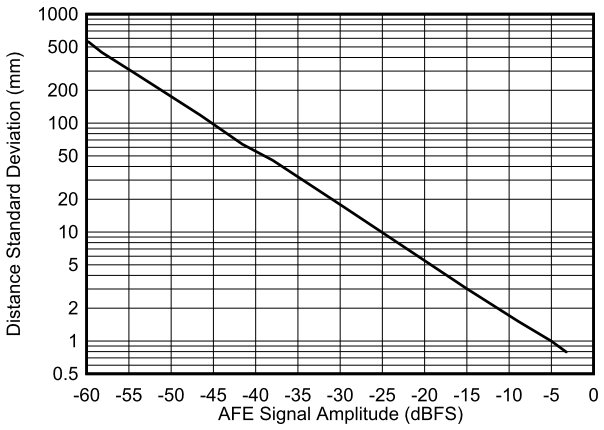

Figure 1. Distance Standard Deviation vs AFE Input Signal

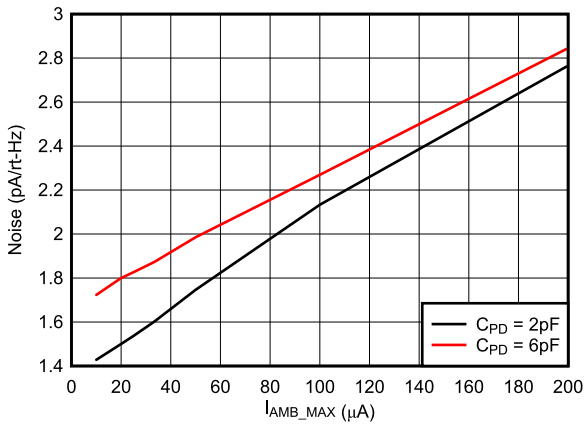

Figure 2. AFE Thermal Noise vs Maximum Ambient Current Supported

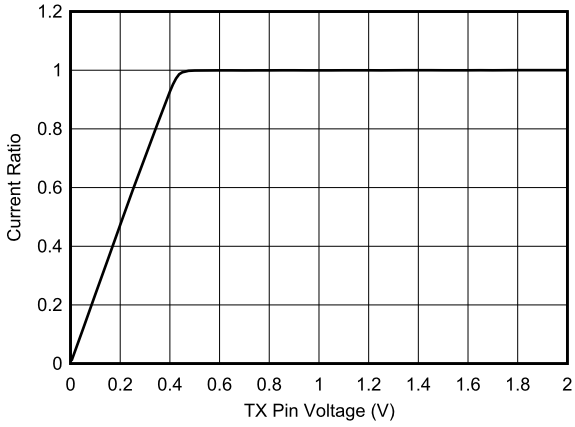

Figure 3. Illumination Driver I-V Characteristics

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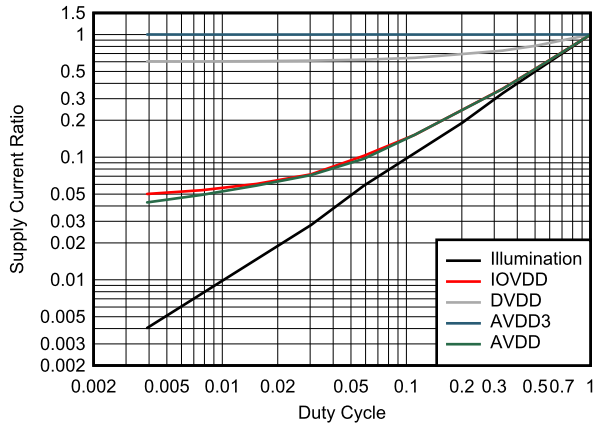
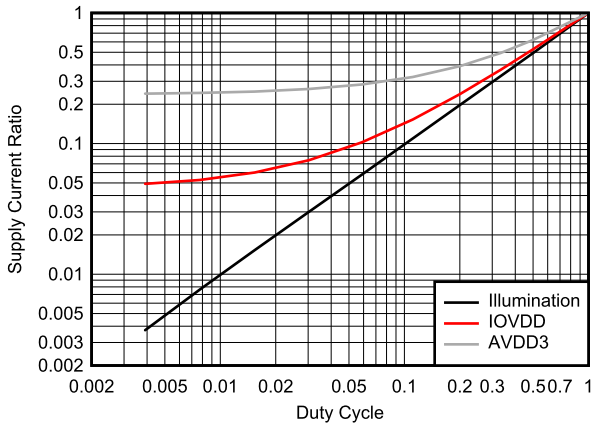
6.7.1 Continuous Mode



Duty Cycle =
(NUM_AVG_SUB_FRAMES + 1) / (NUM_SUB_FRAMES + 1)

Figure 4. Supply Current in Continuous Mode



Duty Cycle =
(NUM_AVG_SUB_FRAMES + 1) / (NUM_SUB_FRAMES + 1)

Figure 5. Supply Current in Continuous Mode with Internal LDO

6.7.2 Monoshot Mode

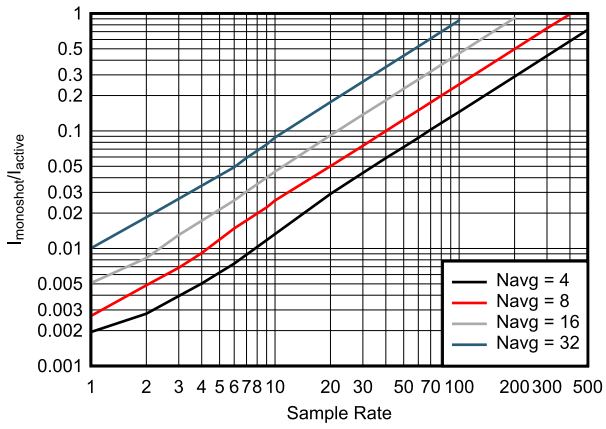


Figure 6. AVDD Supply Current in Monoshot Mode

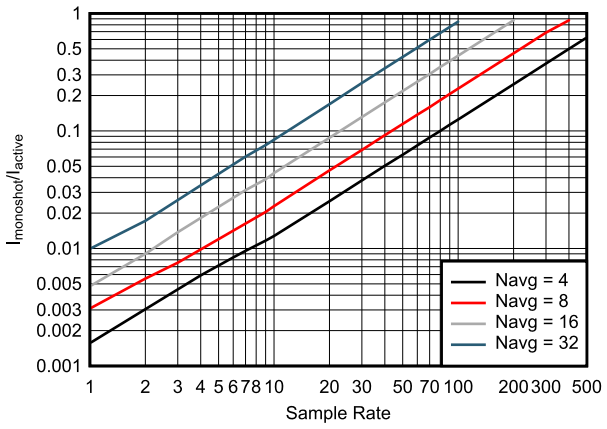


Figure 7. DVDD Supply Current in Monoshot Mode

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Monoshot Mode (continued)

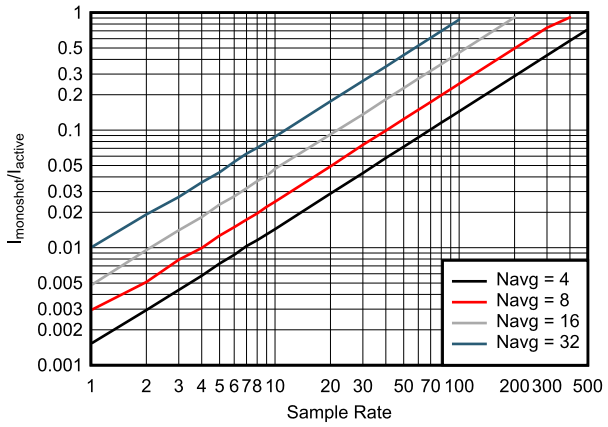

Figure 8. AVDD3 Supply Current in Monoshot Mode

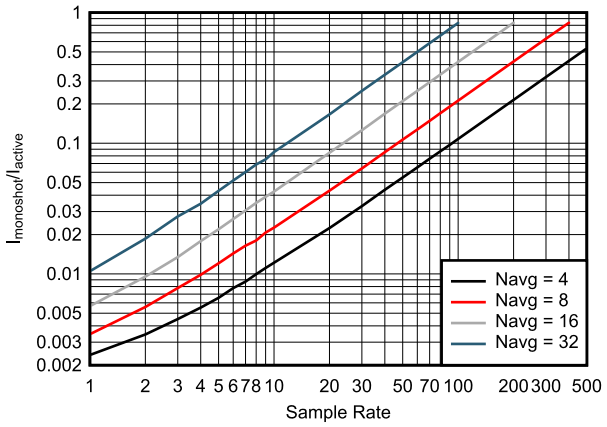

Figure 9. IOVDD Supply Current in Monoshot Mode

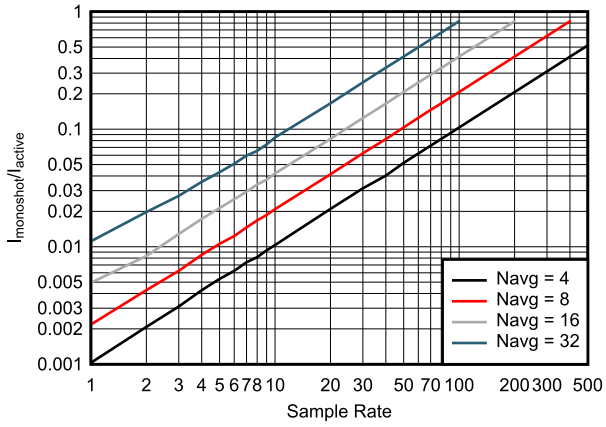

Figure 10. Illumination Supply Current in Monoshot Mode

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6.7.3 Monoshot Mode With Internal LDO

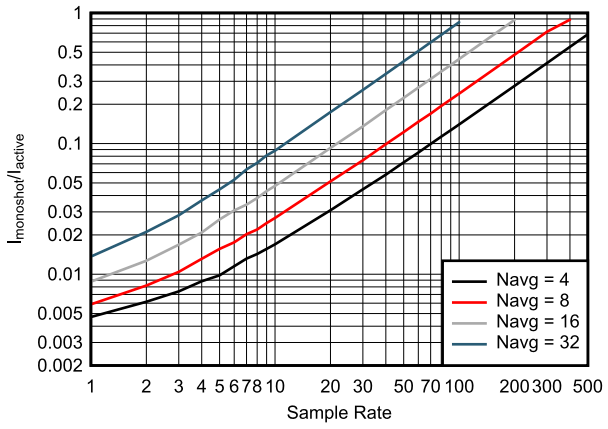

Figure 11. AVDD3 Supply Current in Monoshot Mode with Internal LDO

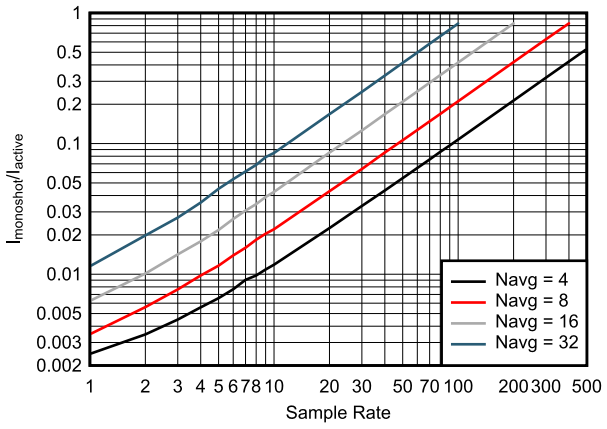

Figure 12. IOVDD Supply Current in Monoshot Mode with Internal LDO

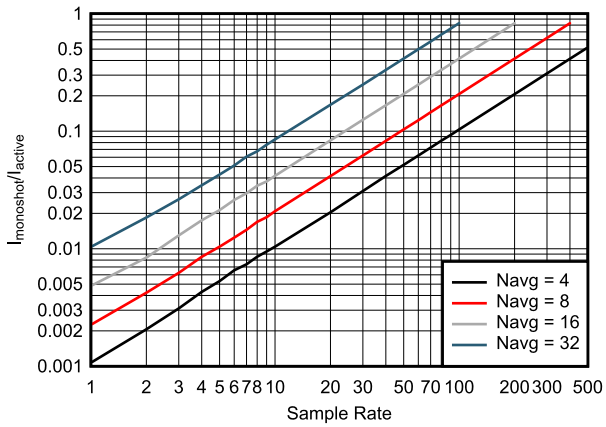

Figure 13. Illumination Supply Current in Monoshot Mode with Internal LDO

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7 Detailed Description

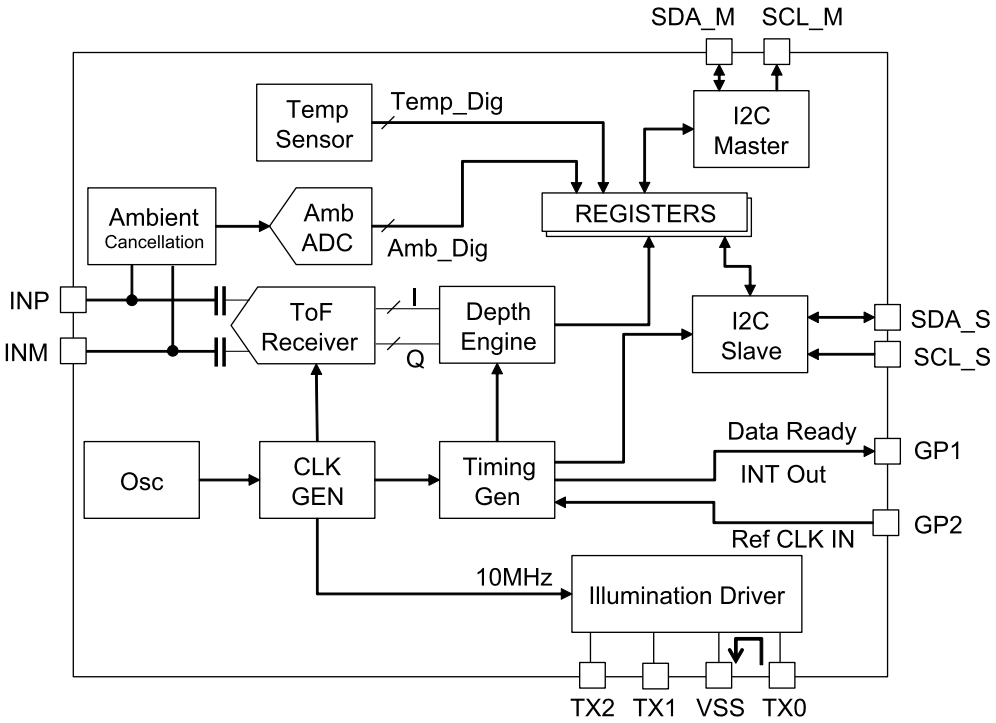
7.1 Overview

The OPT3101 device is a fully integrated Analog Front End (AFE) based on Time-of-Flight (ToF) principle using active illumination. The OPT3101 AFE connects to an external illuminator (LED/VCSEL/LASER) to transmit modulated optical signals and reflected signals is received by external photodiode which connects to input of the AFE. The received signal is converted to amplitude, phase information by the AFE and depth engine. This output is stored in registers, which can be read out through the device I^2C interface.

The OPT3101 AFE has the following blocks:

- Timing generator: generates the sequencing signals for the sensor, illumination, and depth processor
- ToF receiver AFE
- Illumination driver
- Depth engine: calculates phase and amplitude
- I^2C slave for configuration and output data interface of the device registers by the host processor
- I^2C master for external temperature sensing, auto load registers from an external EEPROM

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Timing Generator

The timing generator (TG) generates the timing sequence for each frame. The TG has the following features:

- Frame rate control
- Sequencing

The following are various modes of operation:

- Continuous or mono-shot mode
- Non-HDR mode or auto HDR mode
- Single-LED or multi-LED mode

Feature Description (continued)

Different modes of operation are explained below.

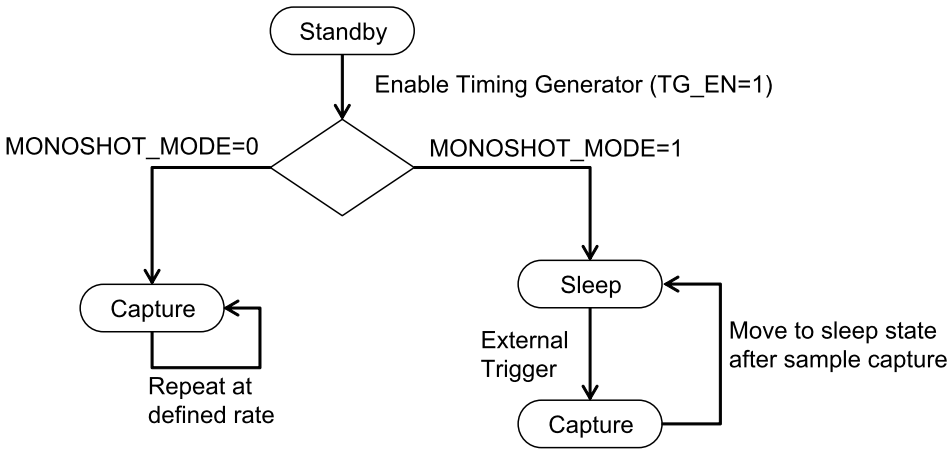


Figure 14. Continuous and Mono-Shot Modes

7.3.1.1 Continuous Operating Mode

In this mode, the device runs continuously at the programmed sample rate. More details about the frame timing are described in Non-HDR Mode and Auto HDR Mode.

7.3.1.2 Mono-Shot Mode

Mono-shot mode is a low power mode. In this mode, the device will be in a deep sleep state and waits for an external trigger. The sample can be initiated by $\overline{\text{RST\_MS}}$ pin (active low) trigger or the register trigger (MONOSHOT_BIT). On trigger, the device comes out of power down, waits for programmed delay (POWERUP_DELAY) to start frame, captures specified number of samples (MONOSHOT_NUMFRAME), then goes into deep sleep state to save power. A new interrupt will be serviced only after completing the current frame capture. Any interrupt during the capture of a frame will be discarded. Figure 15 shows the timing diagram of mono-shot mode with $\overline{\text{RST\_MS}}$ pin trigger. From the trigger, the frame start can be delayed by setting the POWERUP_DELAY register. The delay between trigger and frame VD is (64 × POWERUP_DELAY + 2) × T_{CLK}. A minimum delay of 0.4 ms is required for the device to come out of deep sleep state. A maximum of 26.2 ms delay can be programmed. This mode can also be used for synchronized capture from an external host.

$\overline{\text{RST\_MS}}$ pin is used for dual purpose for reset and mono-shot trigger. For reset, give a pulse width that is > 30 µs. For mono-shot trigger, give a pulse width that is < 1 µs and > 100 ns.

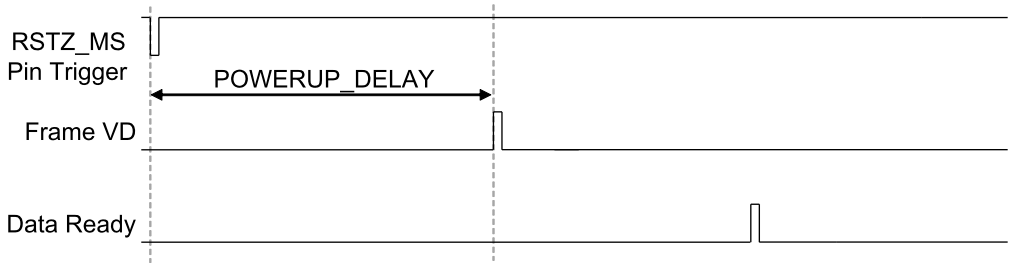


Figure 15. Timing for Pin Triggered Mono-Shot Mode With $\overline{\text{RST\_MS}}$

For register triggered mono-shot mode, the host writes 1 to the interrupt register (MONOSHOT_BIT) to initiate sample capture. Once the data ready of N^{th} sample is available, the device automatically clears the interrupt register bit and goes into deep sleep state.

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Feature Description (continued)

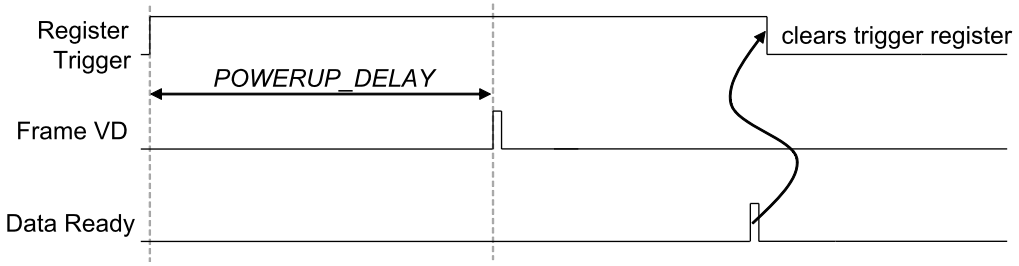

Figure 16. Timing for Register (*MONOSHOT_BIT*) Triggered Mono-Shot Mode,

Table 1. Mono-shot Mode Register Settings

PARAMETER	Address	Description
MONOSHOT_MODE	27h[1:0]	00 – Continuous mode 11 – Mono-shot mode
MONOSHOT_NUMFRAME	27h[7:2]	Number of frames to be captured for every trigger.
POWERUP_DELAY	26h[23:10]	Register to program the delay from the external trigger to start of frame (FRAME_VD). Delay = (64 × POWERUP_DELAY + 2) × Tclk, Tclk = 25 ns
MONOSHOT_BIT	0h[23]	Mono-shot trigger register. Write 1 to start sample capture. Bit will be auto cleared after capture completion.

7.3.1.3 Non-HDR Mode

In this mode a fixed LED current is used for the Illumination driver. Figure 17 shows the frame timing. Each frame is divided into multiple sub-frames, which can be varied from 1 to 2^{12}. Each sub-frame is 10,000 clocks of 40 MHz, which is equal to a 4-kHz sub-frame rate. In each sub-frame, 8192 clocks is the photodiode signal integration time and the remainder of the time is used for processing the signal and computing amplitude phase. The device can be operated at the highest frame rate of 4 kHz by setting the number of sub-frames to 1 (NUM_SUB_FRAMES = 0) in a frame.

$$\text{sample rate} = \frac{4000}{1 + \text{NUM\_SUB\_FRAMES}} \quad (1)$$

Table 2. Sample Rate Configuration Registers

PARAMETER	Address	Description
NUM_SUB_FRAMES	9Fh[11:0]	Total number of sub-frames in a frame. Each sub-frame is 0.25 ms. Number of sub frames in a frame = NUM_SUB_FRAMES + 1. This number must be equal or greater than NUM_AVG_SUB_FRAMES.
NUM_AVG_SUB_FRAMES	9Fh[23:12]	Specifies the number of sub-frames to be averaged in a frame. Averaging sub-frames = NUM_AVG_SUB_FRAMES + 1.

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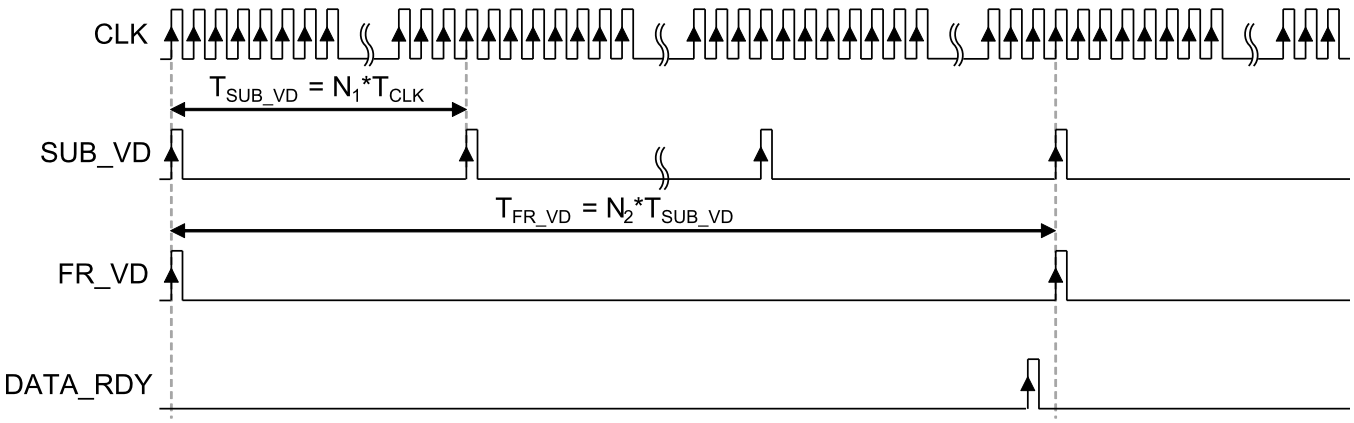


(1) N_1 = 10,000; number of 40-MHz clocks in a sub-frame.

(2) N_2 = NUM_SUB_FRAMES + 1 is the number of sub-frames in a frame, programmable in the range of 1 to 2^{12}.

Figure 17. Frame Timing Diagram

7.3.1.4 Auto HDR Mode

In this mode, the sequencer switches between two illumination driver currents to extend the dynamic range, depending on the signal saturation and lower amplitude threshold. The principle of operation is explained in Figure 18. When the illumination driver current is high, it switches to a lower current if the amplitude exceeds the saturation threshold, HDR_THR_HIGH. When the illumination driver current is low, it switches to higher current if the measured amplitude is below the lower threshold, HDR_THR_LOW.

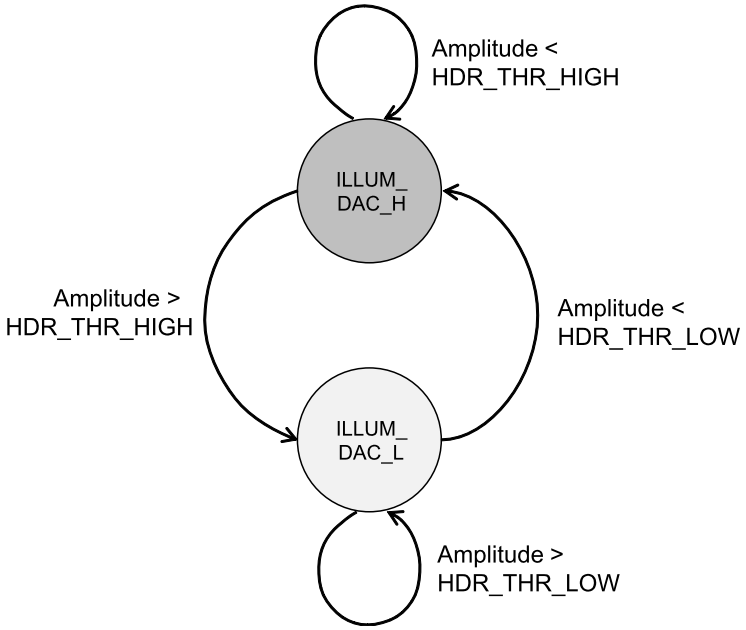
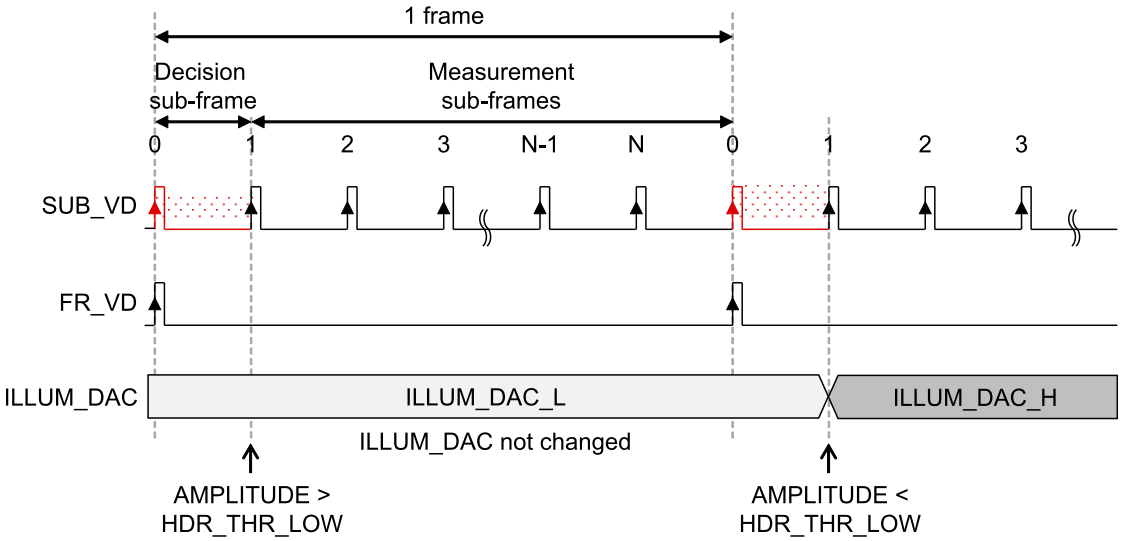


Figure 18. Auto HDR Mode: State Diagram

Figure 19 shows the frame timing diagram for HDR mode. In this mode, the first sub-frame information is used to make a decision about the validity of the output. If the first sub-frame output is valid the same illumination DAC will be used for the rest of the frame, otherwise the illumination driver will be switched to second illumination DAC current.

ADVANCE INFORMATION



(1) The illumination driver DAC switching is shown for a particular scenario.

Figure 19. Auto HDR Mode Frame Timing Diagram

Amplitude thresholds for HDR mode should be chosen according to Equation 2. Choice of the two illumination driver DAC currents depends on the end application.

$$\frac{HDR\_THR\_HIGH}{HDR\_THR\_LOW} > \frac{ILLUM\_DAC\_H}{ILLUM\_DAC\_L} \quad (2)$$

HDR_THR_HIGH is the saturation threshold for the HDR switching, it should be set slightly below the actual saturation amplitude (HDR should trigger before the AFE analog path saturates). HDR_THR_LOW is the accuracy threshold, amplitude below which the distance accuracy will be poor. Figure 20 shows an illustration of the HDR operation with distance. At a distance close to the sensor lower illumination DAC current will be used. As the object moves away from the sensor, ILLUM_DAC switches to a higher value once the amplitude falls below the lower threshold (HDR_THR_LOW). At the switching point, non-saturation is ensured by choosing the DAC currents according to Equation 2. As the object moves towards the sensor, ILLUM_DAC switches to a lower value once the amplitude reaches saturation level (HDR_THR_HIGH). At this transition, the amplitude with ILLUM_DAC_L will be above HDR_THR_LOW.

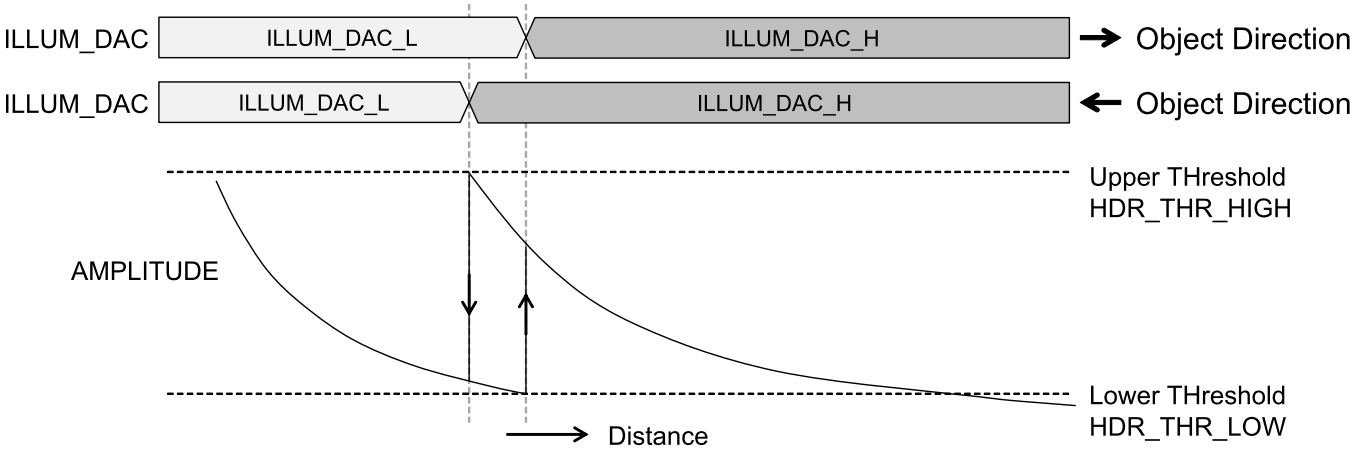


Figure 20. HDR Mode Operation With Distance

Table 3. HDR Mode Configuration Registers

PARAMETER	Address	Description
EN_ADAPTIVE_HDR	2Ah[15]	Enable adaptive HDR mode. Minimum number of sub-frames in a frame in this mode is 2 (NUM_SUB_FRAMES = 1)
SEL_HDR_MODE	2Ah[16]	Choses which current to use when EN_ADAPTIVE_HDR = 0. 0 – ILLUM_DAC_L | 1 – ILLUM_DAC_H
HDR_THR_HIGH	2Bh[15:0]	Saturation amplitude threshold of the auto HDR for high DAC current (ILLUM_DAC_H) Write a value of 27000
HDR_THR_LOW	2Ch[15:0]	Accuracy threshold of the auto HDR for low DAC current (ILLUM_DAC_L) = HDR_THR_HIGH × (ILLUM_DAC_L / ILLUM_DAC_H) × (1 / 1.2)
ILLUM_DAC_L_TX0	29h[4:0]	ILLUM_DAC_L of TX0 Channel
ILLUM_DAC_H_TX0	29h[9:5]	ILLUM_DAC_H of TX0 Channel
ILLUM_DAC_L_TX1	29h[14:10]	ILLUM_DAC_L of TX1 Channel
ILLUM_DAC_H_TX1	29h[19:15]	ILLUM_DAC_H of TX1 Channel
ILLUM_DAC_L_TX2	29h[23:20], 2Ah[23]	ILLUM_DAC_L of TX2 Channel
ILLUM_DAC_H_TX2	2Ah[22:18]	ILLUM_DAC_H of TX2 Channel

7.3.1.5 Multi Channel Mode

The OPT3101 AFE supports up to three separate illumination channels. Only one illumination channel can be activated at a given point of time. In multi channel mode, the illumination driver switches current between different pins (TX0, TX1, and TX2) across samples. The sequence of switching is programmable (TX_SEQ_REG). In single channel mode, the channel to be used can be selected through SEL_TX_CH. Each Illumination channel has separate current programmability, listed in Table 3. This mode can be combined with continuous mode, mono-shot mode, non-HDR mode, or auto HDR mode.

Table 4. Multi LED Configuration Registers

Register	Address	Description
EN_TX_SWITCH	2Ah[0]	Enable switching between Illumination channels TX0, TX1, TX2.
SEL_TX_CH	2Ah[2:1]	Selects the ILLUM channels when switching is disabled.
TX_SEQ_REG	2Ah[14:3]	Stores the sequence of ILLUM channel switching in this register. For example, register value: 2-1-0-2-1-0. The sequence will be 0-1-2-0-1-2

Separate calibration registers are provided for each illumination channel to support different currents for each channel in the same system.

7.3.2 AFE

The diode current is capacitively coupled to the AFE as shown in Figure 21. AFE processes the input signal and produces digitized in-phase and quadrature-phase components of the input signal. The AFE has a full scale current of 200 nA peak-to-peak and supports a photodiode capacitance up to 6 pF.

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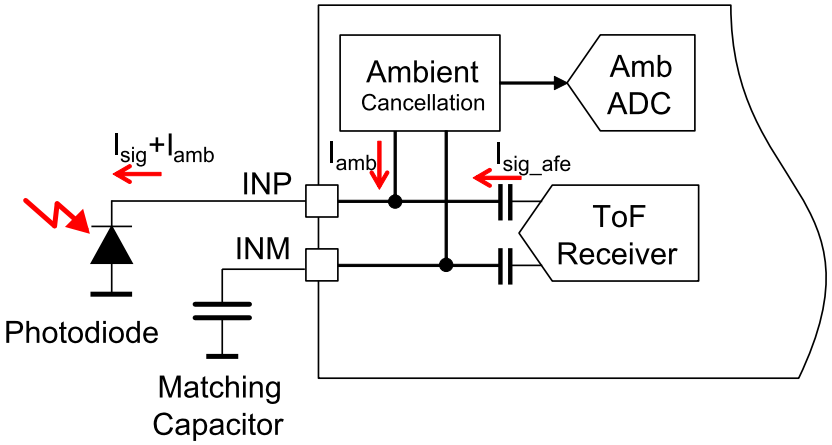

Figure 21. AFE, Photodiode Interface

The signal-to-noise ratio (SNR) for a given signal current and sample rate can be calculated from the following equation.

$$SNR = \frac{I_{SIG\_AFE}}{I_{noise} \times \sqrt{BW}} = \frac{I_{SIG\_AFE}}{94.8pA / \sqrt{(NUM\_AVG\_SUB\_FRAMES + 1)}} \quad (3)$$

where

- I_{sig_afe} = signal current entering the AFE
- I_{noise} = Input referred current noise floor of the AFE
- BW = Signal measurement bandwidth

$$\sigma_{phase} = \frac{1}{SNR} \text{ radians} \quad (4)$$

where

- σ_{phase}= Phase standard deviation in radians
- SNR is calculated from Equation 3

$$\sigma_{distance} = \frac{c/(2f_{MOD})}{2\pi} \times \frac{1}{SNR} \text{ meters} \quad (5)$$

where

- $\sigma_{distance}$= Distance standard deviation in meters
- c = Speed of light
- f_{MOD} = 10 MHz, modulation frequency

For example, with an AFE signal current of 20 nA peak-to-peak (–20 dBFS), frame rate of 125 Hz (NUM_AVG_SUB_FRAMES = 31), SNR = 1193 = 61.5 dB. Depth noise standard deviation for this scenario is $\sigma_{distance}$ = 15 m / (2π) / 1193 = 2 mm.

7.3.3 Ambient Cancellation

Ambient cancellation circuit provides the DC and low-frequency diode current while biasing the diode at 1 V. Figure 22 shows the frequency response of the ambient cancellation circuit. The diode current with frequencies below f_{c2} will see second order rejection. The corner frequency f_{c2} is designed to be at 50 kHz for IAMB_MAX_SEL = 0 (20 uA ambient current support). Below frequency fc1 (approximately at 10 Hz), attenuation will become first order. So for a frequency of 1 kHz, the rejection would be (50 kHz / 1 kHz) × 2 = 2500 = 68 dB.

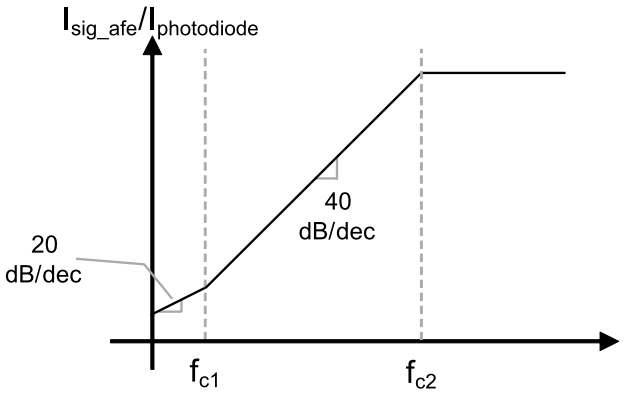

Figure 22. Ambient Cancellation Circuit Frequency Response

The maximum ambient current supported is programmable from 10 μA to 200 uA, listed in Table 5. Noise contribution from ambient cancellation block increases with increase in ambient current support, shown in Figure 2. For low ambient systems, the lower value of maximum ambient support should be used to reduce the noise contribution from the ambient cancellation. Ambient current is also converted to digital using an ADC (AMB_DATA) at the output of the ambient cancellation block. Ambient ADC resolution is 0.104 μA / LSB with 20-μA support. Ambient ADC resolution scales linearly with maximum ambient current supported. Ambient current can be calculated from the AMB_DATA using Equation 6.

$$I_{AMB} = \frac{AMB\_DATA - AMB\_CALIB}{192} \times I_{AMB\_MAX} \quad (6)$$

where

- I_{AMB_MAX}= Maximum ambient current supported. Listed in Table 5
- AMB_CALIB = ambient ADC output in Dark. Typical value is 64, could vary by few codes from device to device.

Table 5. Ambient Cancellation Register Settings

PARAMETER	ADDRESS	DESCRIPTION
IAMB_MAX_SEL	72h[7:4]	Selects the value of maximum ambient current support 0: 20 μA | 5: 10 μA | 10: 33 μA | 11: 50 μA | 12: 100 μA | 14: 200 μA

7.3.4 Oscillator

The system clock is generated using an on-chip oscillator with high stability across temperature. This oscillator is trimmed to a nominal frequency of 80 MHz within ±3%. For accurate distance conversion, this frequency is trimmed digitally to 10-bit accuracy. Additionally, the device can accept external reference clock and correct for the on-chip oscillator variations for continuous background frequency calibration.

7.3.5 CLKGEN

CLKGEN takes the clock from the oscillator and generates clocks required for various blocks. CLKGEN generates a 10-MHz clock for the illumination driver. The phase of the illumination CLK can be changed in 16 steps. This feature is useful for phase non-linearity correction resulting from square wave modulation. Phase non-linearity from ideal square wave demodulation is approximately ±4 degrees. OPT3101 has a filter to reject the higher order harmonics of square wave and the resulting non-linearity is small ±0.5 degrees. For de-aliasing, CLKGEN also generates an additional frequency of 10 × (6 / 7) MHz or 10 × (6 / 5) MHz for illumination clock.

Table 6. Register Settings to Change the Phase of Illumination

PARAMETER	ADDRESS	DESCRIPTION
SHIFT_ILLUM_PHASE	71h[6:3]	Mode to generate different Illumination clock phases. Illumination clock phase = SHIFT_ILLUM_PHASE × 22.5 degrees

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7.3.6 Illumination Driver

Figure 23 shows the illumination driver block diagram. The illumination driver supports three illumination channels. Same current source is multiplexed onto three channels. Only one channel can be used at any given time.

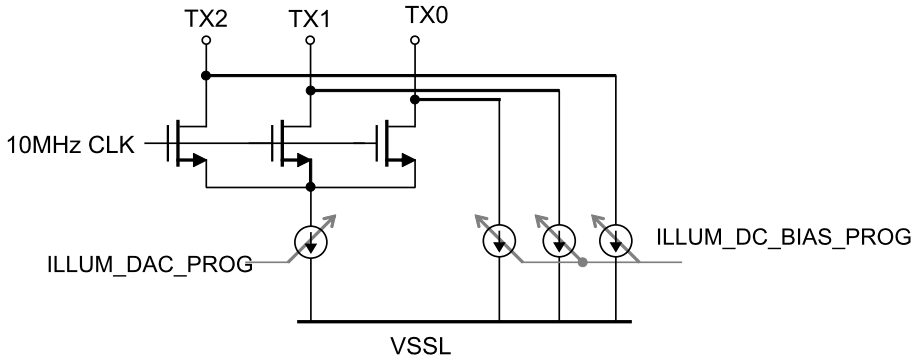

Figure 23. Illumination Driver Block Diagram

Illumination driver current can be programmed using a 5-bit DAC, listed in Table 7. Step size of the DAC can also be scaled from 1.4 mA to 5.6 mA using ILLUM_SCALE. DC bias current option is also provided. DC bias is useful if the system requires very small switching illumination current. This DC bias can be programmed in the range of 0.5 mA to 7.5 mA in steps of 0.5 mA using ILLUM_DC_CURR_DAC.

Table 7. Illumination Driver Register Settings

REGISTER	ADDRESS	DESCRIPTION
EN_LED_DRV	79h[0]	Enable Illumination Driver
ILLUM_DAC_L_TX0	29h[4:0]	Illumination driver current DAC register, ILLUM_DAC_L of TX0 Channel. Illumination current = ILLUM_DAC_L_TX0 × DAC Step
ILLUM_DAC_H_TX0	29h[9:5]	Illumination driver current DAC register, ILLUM_DAC_H of TX0 Channel. Illumination current = ILLUM_DAC_L_TX0 × DAC Step
ILLUM_SCALE_L_TX0	2Bh[18:16]	Scale illumination current DAC step size for ILLUM_DAC_L_TX0 000 – 5.6 mA | 001 – 4.2 mA | 010 – 2.8 mA | 011 – 1.4 mA
ILLUM_SCALE_H_TX0	2Bh[21:19]	Scale illumination current DAC step size for ILLUM_DAC_H_TX0 000 – 5.6 mA | 001 – 4.2 mA | 010 – 2.8 mA | 011 – 1.4 mA
ILLUM_DC_CURR_DAC	79h[11:8]	Program Illumination driver DC bias current DC Current = 0.5 mA* ILLUM_DC_CURR_DAC

7.3.7 Depth Engine

The depth engine computes the phase and amplitude from in-phase and quadrature-phase components of the received signal. Depth engine also performs following calibrations:

- Phase Offset
- Phase Correction with Temperature
- Crosstalk
- Frequency
- Square Wave Non-linearity
- Phase Correction with Ambient

For detailed calibration procedure, refer to *OPT3101 Distance Sensor System Calibration*

Table 8. Phase Offset Correction Registers

PARAMETER	ADDRESS	DESCRIPTION
EN_PHASE_CORR	43h [0]	Enables phase offset correction
PHASE_OFFSET_HDR0_TX0	42h[15:0]	Phase offset for TX0 illumination channel with current of ILLUM_DAC_L_TX0
PHASE_OFFSET_HDR1_TX0	51h[15:0]	Phase offset for TX0 illumination channel with current of ILLUM_DAC_H_TX0

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Table 8. Phase Offset Correction Registers (continued)

PARAMETER	ADDRESS	DESCRIPTION
PHASE_OFFSET_HDR0_TX1	52h[15:0]	Phase offset for TX1 illumination channel with current of ILLUM_DAC_L_TX1
PHASE_OFFSET_HDR1_TX1	53h[15:0]	Phase offset for TX1 illumination channel with current of ILLUM_DAC_H_TX1
PHASE_OFFSET_HDR0_TX2	54h[15:0]	Phase offset for TX2 illumination channel with current of ILLUM_DAC_L_TX2
PHASE_OFFSET_HDR1_TX2	55h[15:0]	Phase offset for TX2 illumination channel with current of ILLUM_DAC_H_TX2

Table 9. Phase Temperature Coefficient Registers

PARAMETER	ADDRESS	DESCRIPTION
EN_TEMP_CORR	43h[1]	Enable temperature correction
SCALE_PHASE_TEMP_COEFF	43h[8:6]	Adjust scale factor for temperature coefficient
TMAIN_CALIB_HDR0_TX0	47h[11:0]	Calibration temperature for sensor offset for TX0 illumination channel with current of ILLUM_DAC_L_TX0
TEMP_COEFF_MAIN_HDR0_TX0	45h[11:0]	Phase temperature coefficient for sensor temperature for TX0 illumination channel with current of ILLUM_DAC_L_TX0
TMAIN_CALIB_HDR1_TX0	48h[11:0]	Calibration temperature for sensor offset for TX0 illumination channel with current of ILLUM_DAC_H_TX0
TEMP_COEFF_MAIN_HDR1_TX0	2Dh[11:0]	Phase temperature coefficient for sensor temperature for TX0 illumination channel with current of ILLUM_DAC_H_TX0
TMAIN_CALIB_HDR0_TX1	49h[11:0]	Calibration temperature for sensor offset for TX1 illumination channel with current of ILLUM_DAC_L_TX1
TEMP_COEFF_MAIN_HDR0_TX1	2Dh[23:12]	Phase temperature coefficient for sensor temperature for TX1 illumination channel with current of ILLUM_DAC_L_TX1
TMAIN_CALIB_HDR1_TX1	41h[23:12]	Calibration temperature for sensor offset for TX1 illumination channel with current of ILLUM_DAC_H_TX1
TEMP_COEFF_MAIN_HDR1_TX1	2Fh[23:16], 30h[23:20]	Phase temperature coefficient for sensor temperature for TX1 illumination channel with current of ILLUM_DAC_H_TX1
TMAIN_CALIB_HDR0_TX2	3Fh[11:0]	Calibration temperature for sensor offset for TX2 illumination channel with current of ILLUM_DAC_L_TX2
TEMP_COEFF_MAIN_HDR0_TX2	31h[23:16], 32h[23:20]	Phase temperature coefficient for sensor temperature for TX2 illumination channel with current of ILLUM_DAC_L_TX2
TMAIN_CALIB_HDR1_TX2	45h[23:12]	Calibration temperature for sensor offset for TX2 illumination channel with current of ILLUM_DAC_H_TX2
TEMP_COEFF_MAIN_HDR1_TX2	33h[23:16], 34h[23:20]	Phase temperature coefficient for sensor temperature for TX2 illumination channel with current of ILLUM_DAC_H_TX2

Table 10. Phase Temperature Coefficient Registers for External Temperature Sensor

PARAMETER	ADDRESS	DESCRIPTION
TILLUM_CALIB_HDR0_TX0	47h[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR0_TX0	46h[11:0]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR1_TX0	48h[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR1_TX0	51h[23:16], 52h[23:20]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR0_TX1	49h[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR0_TX1	53h[23:16], 54h[23:20]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR1_TX1	43h[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR1_TX1	55h[23:16], 56h[23:20]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR0_TX2	3Fh[23:12]	Calibration temperature of external temperature sensor
TEMP_COEFF_ILLUM_HDR0_TX2	57h[23:16], 58h[23:20]	Phase temperature coefficient for illumination using external temperature sensor.
TILLUM_CALIB_HDR1_TX2	46h[23:12]	Calibration temperature of external temperature sensor

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Table 10. Phase Temperature Coefficient Registers for External Temperature Sensor (continued)

PARAMETER	ADDRESS	DESCRIPTION
TEMP_COEFF_ILLUM_HDR1_TX2	59h[23:16], 5Ah[23:20]	Phase temperature coefficient for illumination using external temperature sensor.

Table 11. Ambient dependent Phase Correction Registers

Register	Address	Description
AMB_PHASE_CORR_PWL_X0	B8h[9:0]	First knee point of PWL phase correction with ambient
AMB_PHASE_CORR_PWL_X1	B9h[19:10]	Second knee point of PWL phase correction with ambient
AMB_PHASE_CORR_PWL_X2	B9h[9:0]	Third knee point of PWL phase correction with ambient
AMB_PHASE_CORR_PWL_COEFF0	0Ch[23:16]	Slope of first segment for PWL phase correction with ambient
AMB_PHASE_CORR_PWL_COEFF1	B4h[7:0]	Slope of second segment for PWL phase correction with ambient
AMB_PHASE_CORR_PWL_COEFF2	B4h[15:8]	Slope of third segment for PWL phase correction with ambient
AMB_PHASE_CORR_PWL_COEFF3	B4h[23:16]	Slope of fourth segment for PWL phase correction with ambient
SCALE_AMB_PHASE_CORR_COEFF	B5h[2:0]	Scaling factor for ambient based PWL phase correction.

Table 12. Internal Crosstalk Correction Registers

REGISTER	ADDRESS	DESCRIPTION
INT_XTALK_CALIB	2Eh[4]	The device initializes the internal electrical crosstalk measurement upon setting this bit. Use following sequence: INT_XTALK_CALIB = 1 delay (at least $5 \times 2^{XTALK\_FILT\_TIME\_CONST}$ frames) INT_XTALK_CALIB = 0
XTALK_FILT_TIME_CONST	2Eh[23:20]	Time constant for crosstalk filtering. Time constant $\tau = 2^{XTALK\_FILT\_TIME\_CONST}$ frames. At least 5τ should be allowed for settling of crosstalk measurement.
USE_XTALK_FILT_INT	2Eh[5]	Select filter or direct sampling for internal crosstalk measurement. 0 – Direct sampling, 1 – Filter
USE_XTALK_REG_INT	2Eh[6]	Select register value or internally calibrated value for internal crosstalk 0 – Calibration value, 1 – Register value
IPHASE_XTALK_INT_REG	3D[15:0]	Register for in-phase component of internal crosstalk
QPHASE_XTALK_INT_REG	3E[15:0]	Register for quad-phase component of internal crosstalk
IPHASE_XTALK	3Bh[23:0]	Read-only register. In-phase component. Different values can be selected to be readout with IQ_READ_DATA_SEL
QPHASE_XTALK	3Ch[23:0]	Read-only register. Quadrature phase component. Different values can be selected to be readout with IQ_READ_DATA_SEL
IQ_READ_DATA_SEL	2Eh[11:9]	Mux select for IPHASE_XTALK, QPHASE_XTALK 000 – Internal Crosstalk | 001 – Illum Crosstalk | 010 – Raw I, Q | 011 – 16-bit frame counter
INT_XTALK_REG_SCALE	2E[16:14]	Scale factor for internal crosstalk register (IPHASE_XTALK_INT_REG, QPHASE_XTALK_INT_REG). Scale = $2^{INT\_XTALK\_REG\_SCALE}$

Table 13. Illumination Crosstalk Correction Registers

REGISTER	ADDRESS	DESCRIPTION
ILLUM_XTALK_CALIB	2Eh[12]	The device initializes the Illumination crosstalk measurement upon setting this bit. This measurement should be done with the photodiode masked such that no modulated light is received. Use following sequence: ILLUM_XTALK_CALIB = 1 delay(at least $5 \times 2^{XTALK\_FILT\_TIME\_CONST}$ frame) ILLUM_XTALK_CALIB = 0
USE_XTALK_FILT_ILLUM	2Eh[7]	Select filter or direct sampling for Illumination crosstalk measurement. 0 – Direct sampling, 1 – Filter
USE_XTALK_REG_ ILLUM	2Eh[8]	Select register value or internally calibrated value for illumination crosstalk correction. 0 – Calibration value, 1 – Register value

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Table 13. Illumination Crosstalk Correction Registers (continued)

REGISTER	ADDRESS	DESCRIPTION
ILLUM_XTALK_REG_SCALE	2E[19-17]	Scale factor for Illumination crosstalk register (IPHASE_XTALK_REG_HDR<i>_TX<j>, QPHASE_XTALK_REG_HDR<i>_TX<j>, i=0,1, j=0,1,2). Scale = $2^{INT\_XTALK\_REG\_SCALE}$
IPHASE_XTALK_REG_HDR0_TX0	2Fh[15:0]	Register for illumination crosstalk in-phase component for TX0 channel with ILLUM_DAC_L_TX0 current
QPHASE_XTALK_REG_HDR0_TX0	30h[15:0]	Register for illumination crosstalk quad-phase component for TX0 channel with ILLUM_DAC_L_TX0 current
IPHASE_XTALK_REG_HDR1_TX0	31h[15:0]	Register for illumination crosstalk in-phase component for TX0 channel with ILLUM_DAC_H_TX0 current
QPHASE_XTALK_REG_HDR1_TX0	32h[15:0]	Register for illumination crosstalk quad -phase component for TX0 channel with ILLUM_DAC_H_TX0 current
IPHASE_XTALK_REG_HDR0_TX1	33h[15:0]	Register for illumination crosstalk in-phase component for TX1 channel with ILLUM_DAC_L_TX1 current
QPHASE_XTALK_REG_HDR0_TX1	34h[15:0]	Register for illumination crosstalk in quad-phase component for TX1 channel with ILLUM_DAC_L_TX1 current
IPHASE_XTALK_REG_HDR1_TX1	35h[15:0]	Register for illumination crosstalk in-phase component for TX1 channel with ILLUM_DAC_H_TX1 current
QPHASE_XTALK_REG_HDR1_TX1	36h[15:0]	Register for illumination crosstalk quad-phase component for TX1 channel with ILLUM_DAC_H_TX1 current
IPHASE_XTALK_REG_HDR0_TX2	37h[15:0]	Register for illumination crosstalk in-phase component for TX2 channel with ILLUM_DAC_L_TX2 current
QPHASE_XTALK_REG_HDR0_TX2	38h[15:0]	Register for illumination crosstalk quad -phase component for TX2 channel with ILLUM_DAC_L_TX2 current
IPHASE_XTALK_REG_HDR1_TX2	39h[15:0]	Register for illumination crosstalk in-phase component for TX2 channel with ILLUM_DAC_H_TX2 current
QPHASE_XTALK_REG_HDR1_TX2	3Ah[15:0]	Register for illumination crosstalk quad -phase component for TX2 channel with ILLUM_DAC_H_TX2 current

Table 14. Frequency Correction Registers

REGISTER	ADDRESS	DESCRIPTION
EN_AUTO_FREQ_COUNT	0Fh[21]	Determines which value to be used for frequency correction 0 – Trimmed value 1 – Measured value from frequency calibration
EN_FLOOP	0Fh[22]	Enables the frequency calibration block.
EN_FREQ_CORR	0Fh[23]	Enable frequency correction for the phase output
REF_COUNT_LIMIT	0Fh[14:0]	This sets the limit for ref-clock count. Write this register with value = $(40e6 / 2^{SYS\_CLK\_DIVIDER}) / f_{EXT}$
SYS_CLK_DIVIDER	0Fh[20:17]	Programs system clock divider for frequency calibration. This should be adjusted to get it closer to the external reference frequency. The default is 10, system clock = 40 MHz / 2^{10} = 39.0625 kHz to bring close to 32.768 kHz.
EN_CONT_FCALIB	10h[15]	Enables continuous frequency calibration. 0 – Frequency is measured only when START_FREQ_CALIB = 1 1 – Frequency is continuously measured.
FREQ_COUNT_READ_REG	10h[14:0]	Read register which holds the value of freq_loop.
START_FREQ_CALIB	0Fh[16]	starts the freq_calib

Table 15. Phase Non-Linearity Correction Registers

REGISTER	ADDRESS	DESCRIPTION
EN_NL_CORR	4Ah[0]	Enables square wave non-linearity correction
SCALE_NL_CORR_COEFF	4Ah[19:18]	Scaling factor for non linearity correction coefficients (A*_COEFF_HDR*_TX*)
A0_COEFF_HDR0_TX0	4Ah[17:2]	0th order coefficient for square wave non-linearity correction
A1_COEFF_HDR0_TX0	4Bh[15:0]	1st order coefficient for square wave non-linearity correction
A2_COEFF_HDR0_TX0	4Ch[15:0]	2nd order coefficient for square wave non-linearity correction

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Table 15. Phase Non-Linearity Correction Registers (continued)

REGISTER	ADDRESS	DESCRIPTION
A3_COEFF_HDR0_TX0	4D[15:0]	3rd order coefficient for square wave non-linearity correction
A4_COEFF_HDR0_TX0	4Eh[15:0]	4th order coefficient for square wave non-linearity correction
A0_COEFF_HDR1_TX0	A2[15:0]	0th order coefficient for square wave non-linearity correction
A1_COEFF_HDR1_TX0	A7[15:0]	1st order coefficient for square wave non-linearity correction
A2_COEFF_HDR1_TX0	AC[15:0]	2nd order coefficient for square wave non-linearity correction
A3_COEFF_HDR1_TX0	B1[15:0]	3rd order coefficient for square wave non-linearity correction
A4_COEFF_HDR1_TX0	AA[23:16], AB[23:16]	4th order coefficient for square wave non-linearity correction

7.3.8 Output Data

Phase and amplitude information is stored in registers which can be readout using I^2C interface. Device gives data ready after computation of depth information on general purpose I/O (GP1/GP2) which can be used trigger the host to read the data from the device. Distance can be calculated from the phase using Equation 7. 1 code of PHASE_OUT is 0.2287mm.

$$\text{distance} = \frac{\text{PHASE\_OUT}}{2^{16}} \times \frac{c}{2f_{MOD}} \text{ meters} \quad (7)$$

where

- c = Speed of light
- f_{MOD} =10 MHz, modulation frequency

Along with phase and amplitude of the signal, ambient ADC output and temperature sensor output are also stored in the registers. All the output data is stored in contiguous registers 8, 9, and 10.

Table 16. Output Data Registers

Register	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REG 8	FRAME_COUNT0	AMB_OVL_FLAG	MOD_FREQ	FRAME_STATUS	TX_CHANNEL		HDR_MODE	PHASE_OVER_FLOW	PHASE_OUT [15:8]								PHASE_OUT [7:0]							
REG 9	DEALIAS_BIN[3:0]				PHASE_OVER FLOW_ F2	SIG_O VL_FL AG	FRAME_COUNT 1		AMP_OUT[15:8]								AMP_OUT[7:0]							
REG 10	TMAIN[11:4]								TMAIN[3:0]				AMB_DATA[9:6]				AMB_DATA[5:0]						FRAME_ COUNT 2	

Table 17. Output Data Registers Description

FIELD	BIT	DESCRIPTION
PHASE_OUT	08h[15:0]	Final calibrated phase.
PHASE_OVERFLOW	08h[16]	Phase overflow during frequency correction.
AMP_OUT	09h[15:0]	Amplitude of the signal.

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Table 17. Output Data Registers Description (continued)

FIELD	BIT	DESCRIPTION
SIG_OVL_FLAG	09h[18]	Overload flag to indicate signal saturation
AMB_OVL_FLAG	08h[22]	Overload flag to indicate ambient saturation
HDR_MODE	08h[17]	Indicates the illumination driver DAC current used. 0: ILLUM_DAC_L | 1: ILLUM_DAC_H
TX_CHANNEL	08h[19:18]	Indicates which Illumination channel of TX0/TX1/TX2 is used.
FRAME_STATUS	08h[20]	0= Invalid frame | 1= Valid frame. Frame can be invalid during crosstalk measurement.
MOD_FREQ	08h[21]	Indicates the frequency used. 0: 10 MHz | 1: de-alias frequency (10 MHz × 6 / 7 or 10 MHz × 6 / 5)
FRAME_COUNT0	08h[23]	Frame counter LSB Bit [0]
FRAME_COUNT1	09h[17:16]	Frame counter Bits [2:1]
FRAME_COUNT2	0Ah[1:0]	Frame counter Bits [4:3]. Frame Counter = FRAME_COUNT2 * 8 + FRAME_COUNT1 * 2 + FRAME_COUNT0
DEALIAS_BIN	09h[23:20]	Distance bin in de-alias mode
PHASE_OVER_FLOW_F2	09h[19]	Phase overflow of second modulation frequency during frequency correction.
AMB_DATA	0Ah[11:2]	Ambient ADC output. Indicates the ambient light. In no ambient light condition AMB_DATA will be 64 typically.
TMAIN	0Ah[23:12]	Temperature sensor output temperature (°C)= TMAIN / 8 – 256

7.3.9 General Purpose I/O

There are two general purpose I/Os which can be used to bring out various digital signals like DATA_RDY, FRAME_VD, ILLUM CLK, ILLUM_EN. GP2 can also be used as an input pin for external clock reference for device on-chip oscillator frequency calibration.

Table 18. GPIO Configuration Registers

REGISTER	ADDRESS	DESCRIPTION
GPO1_MUX_SEL	78h[8:6]	0: DVSS | 2: DIG_GPO_0 | 3: DIG_GPO_1 | 7: ILLUM_CLK
GPIO1_OBUF_EN	78h[12]	Enable output buffer of GP1 pin
GPIO2_IBUF_EN	78h[16]	Enable input buffer of GP2 pin. External reference clock should be connected to this pin for frequency calibration.
GPIO2_OBUF_EN	78h[15]	Enable output buffer of GP2 pin
GPO2_MUX_SEL	78h[11:9]	0: DVSS | 2: DIG_GPO_0 | 3: DIG_GPO_1 | 7: ILLUM_EN_TX0
DIG_GPO_SEL0	0Bh[3:0]	Mux selection bits for digital signal dig_gpo_0 which can be brought out on GP1/GP2 0: FRAME VD | 1: SUB-VD | 4: SEQUENCER INTERRUPT 8: COMP_STATUS | 9: DATA_RDY | 10: FRAME_COUNTER_LSB
DIG_GPO_SEL1	0Bh[7:4]	Mux selection bits for digital signal dig_gpo_1 which can be brought out on GP2/GP2 0: FRAME VD | 1: SUB-VD | 4: SEQUENCER INTERRUPT 8: COMP_STATUS | 9: DATA_RDY | 10: FRAME_COUNTER_LSB

7.3.10 Temperature Sensor

The device has an internal temperature sensor to monitor the temperature of the sensor core. The temperature sensor has a range of –25°C to +125°C. The output of this temperature sensor is accessible from a register TMAIN. It can be used for phase temperature compensation.

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7.3.11 On-Chip Regulator

AFE has an internal regulator for generating 1.8-V supplies (AVDD, DVDD) from AVDD3 supply. In this mode only one 3.3 V is sufficient for the device operation. Since the power is drawn from 3.3V supply for AVDD, DVDD, power consumption will be higher. REG_MODE pin controls the regulator. Connect this pin to IOVDD to enable regulator mode. In non-regulator mode REG_MODE pin should be connected to IOVSS. Figure 177 show the block diagram of the regulator. Minimum decoupling capacitor of 100 nF should be connected at the pins AVDD, DVDD. Decoupling capacitor on AVDD should be referred to AVSS, while decoupling capacitor on DVDD should be referred to IOVSS.

7.3.12 Sequencer

AFE has an on chip sequencer which can be used to perform various operations. Sequencer commands are tabulated in Table 19. Each instruction is 12 bits with the first four MSB bits as the opcode and next eight bit as operand. Sequencer can perform comparison of amplitude or phase with register thresholds COMPARE_REG1, COMPARE_REG2 and generate a signal COMP_STATUS, which can be observed on GP1 with DIG_GPO_SEL0 = 8, gpo1_mux_sel = 2 settings. Comparison input type can be selected using COMP_IN_SEL. Sequencer execute one command per sample. The sequencer interrupt to execute a command can be positioned either at the beginning of the sample or at the end of the sample after data is ready and before next sample starts. Sequencer interrupt can be programmed with TG_SEQ_INT_START, TG_SEQ_INT_END, TG_SEQ_INT_MASK_START, TG_SEQ_INT_MASK_END registers. TG_SEQ_INT_START and TG_SEQ_INT_END defines the position of the interrupt pulse with in a sub-frame. TG_SEQ_INT_MASK_START and TG_SEQ_INT_MASK_END define the sub-frame during which the pulse is enabled.

Some of the use cases of the sequencer are

- Switching of transmitter channels
- Generate interrupt based on phase or amplitude comparison with a defined thresholds
- Generate interrupt based on phase or amplitude comparison with hysteresis
- Extending the dynamic range using four illumination driver currents
- De-alias operation to extend the distance range from 15 m to 75 m.

Table 19. Sequencer Commands

OPCODE	FUNCTION	DESCRIPTION
0000	NOP	The operand indicates the number of cycles for which NOP should be executed. 0 means 1 cycle, 1 means 2 cycle, and so on. For example 0000-00001111 indicates next 16 cycles sequencer will not do anything
0001	WRITE	This command writes the operand to STATUS_OUT register. For example 0001-01100110 make the values of STATUS_OUT port as 011001100. The STATUS_OUT is mapped to certain key registers listed in Table 20. STATUS_OUT will be applied only if EN_PROCESSOR_VALUES = 1
0010	GOTO	Programe Counter (PC) goes to the line indicated by the operand. This command is useful for looping. Next command is executed on next frame VD. For example 0010-00000000 sets the PC to the first line of the program memory so that the instructions are executed in a loop.
0011	DGOTO	In this instruction PC goes to the line indicated by the operand only if STATUS_IN_REG bit is '1'. If not the PC stays in the same command till the STATUS_IN_REG register value becomes 1. Next command is executed on next frame VD. For example 0011-00000000 suspends the program until a register STATUS_IN_REG is set to '1'. Once it is set the loop is restarted.
0100	DrGOTO	In this PC goes to the line indicated by operand without any delay. This executes next instruction as well. Next command is executed on the same frame VD.
0101	COMP0	In this command, the CPU compares COMP_IN and COMPARE_REG1. If COMP_IN ≤ COMPARE_REG1, program counter stays where it is and COMP_STATUS port will be 0. If the comparison fails the program counter moves to the line indicated by the operand and COMP_STATUS becomes 1.
0110	COMP0_INV	Similar to COMP but the comparison used is: COMP_IN ≥ COMPARE_REG2
0111	COMP_WINDOW	In this command PC stays there forever. If (COMP_IN ≥ COMPARE_REG1) and (COMP_IN ≤ COMPARE_REG2) then COMP_STATUS becomes 1 else COMP_STATUS = 0.

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Table 19. Sequencer Commands (continued)

OPCODE	FUNCTION	DESCRIPTION
1000	COMP2	If (COMP_IN ≥ COMPARE_REG1) and (COMP_IN ≤ COMPARE_REG2) then COMP_STATUS becomes 1 else COMP_STATUS = 0. If the condition is True the program counter stays there else moves to the line indicated by the operand.
1001	COMP3	Similar to COMP2. The difference is whatever be the comparison result the program counter moves to the instruction pointed to by the operand. If comparison is met COMP_STATUS is set 1 else 0.
1010	COMP_HYST	In this command PC stays there forever. There is hysteresis in the comparison. If (COMP_IN ≤ COMPARE_REG1) then COMP_STATUS = 0 elsif (COMP_IN ≥ COMPARE_REG2) then COMP_STATUS = 1.
1011	COMP1	In this command, the CPU compares COMP_IN and COMPARE_REG1. If COMP_IN ≤ COMPARE_REG1, program counter stays where it is and COMP_STATUS port will be 0. If the comparison fails the program counter moves to the line indicated by the operand and COMP_STATUS becomes 1.
1100	COMP1_INV	Similar to COMP1 but the comparison used is COMP_IN ≥ COMPARE_REG2
1101–1111	Not Valid	

Table 20. Sequencer STATUS_OUT Register Mapping

STATUS_OUT	REGISTER MAPPING
[0]	INT_XTALK_CALIB
[1]	EN_DEALIAS_MEAS
[2]	START_FREQ_CALIB
[4:3]	SEL_TX_CH
[5]	SEL_HDR_MODE
[7:6]	Invalid

Table 21. Sequencer Registers

REGISTER	ADDRESS	DESCRIPTION
COMP_IN_SEL	13h[2:0]	Select the value used for comp_in. 0 = AMP_OUT | 1 = DEALIAS_BIN | 2 = Dealias Phase | 3 = PHASE_OUT
COMPARE_REG1	13h[18:3]	Sequencer comparison threshold1
COMPARE_REG2	14h[15:0]	Sequencer comparison threshold2
EN_SEQUENCER	14h[16]	Enable the sequencer.
EN_PROCESSOR_VALUES	14h[17]	Uses processor values instead of register values.
STATUS_IN_REG	14h[18]	the register is used to control the program flow in CPU
DIS_INTERRUPT	14h[19]	Disables the interrupt which triggers sequencer.
COMMAND0 to COMMAND19	15h[11:0] to 1Eh[23:12]	Sequencer command registers. Total 20 command registers are available.

7.3.12.1 Interrupt Output

Sequencer supports various interrupt output modes using comparison commands listed in Table 19. Register setting to use the sequencer for generating interrupt output using COMP_WINDOW are listed in Table 22 and the corresponding interrupt output is shown in Figure 24. To use a comparison with hysteresis (COMP_HYST) use COMMAND0 = 0xA00 and rest all settings will remain same as COMP_WINDOW.

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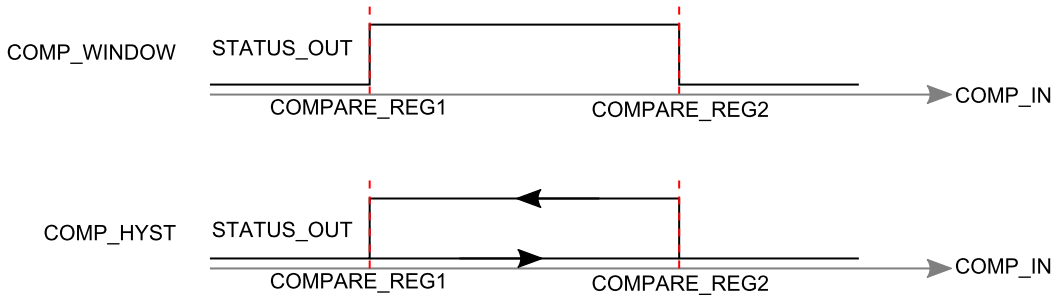

Figure 24. Interrupt Output using different Comparison Commands

Table 22. Register Settings to use Sequencer for Generating Interrupt Output

PARAMETER	VALUE	DESCRIPTION
Sequencer Interrupt Signal		
TG_SEQ_INT_START	9850	Set the sequencer interrupt at the end of the last averaged sub-frame after data ready is available
TG_SEQ_INT_END	9858	
TG_SEQ_INT_MASK_START	NUM_AVG_SUB_FRAMES	
TG_SEQ_INT_MASK_END	NUM_AVG_SUB_FRAMES	
Sequencer Commands		
COMMAND0	0x700	COMP_WINDOW. COMP_STATUS=1 when distance is between the lower (COMPARE_REG1) and upper (COMPARE_REG2) limits else COMP_STATUS=0
Get COMP_STATUS on GP1		
GPIO1_OBUF_EN	1	Enable GP1 Output Buffer.
GPO1_MUX_SEL	3	select DIG_GPO_1 on GP1
GPO_SEL1	8	Select COMP_STATUS on DIG_GPO_1
Comparison Settings		
COMP_IN_SEL	1	Select amplitude PHASE_OUT for comparison input COMP_IN
COMPARE_REG1	PHASE1	Phase corresponding to a lower distance (phase) Threshold
COMPARE_REG2	PHASE2	Phase corresponding to a upper distance (phase) Threshold
Sequencer Enable		
EN_SEQUENCER	1	Enable the sequencer. Sequencer Enable should be only be changed while TG_EN = 0. Before changing this register disable TG (TG_EN = 0), modify this register and then enable TG (TG_EN = 1)
EN_PROCESSOR_VALUES	1	Enable processor values to control the STATUS_OUT register bits.

7.3.12.2 Super-HDR mode using Sequencer

On chip sequencer can be used to extend the dynamic range using four illumination currents. Figure 25 show the state diagram of the super-HDR mode implemented using sequencer. For this example, illumination driver currents should be programmed in the following order: $I_{ILLUM\_H\_TX1}$ > $I_{ILLUM\_L\_TX1}$ > $I_{ILLUM\_H\_TX0}$ > $I_{ILLUM\_L\_TX0}$.Table 23 lists the register settings to operate the device in super HDR mode using the sequencer. HDR_THR_LOW should be determined by the minimum of two adaptive HDR settings listed below.

- HDR_THR_HIGH × ILLUM_DAC_L_TX0/ILLUM_DAC_H_TX0
- HDR_THR_HIGH × ILLUM_DAC_L_TX1/ILLUM_DAC_H_TX1

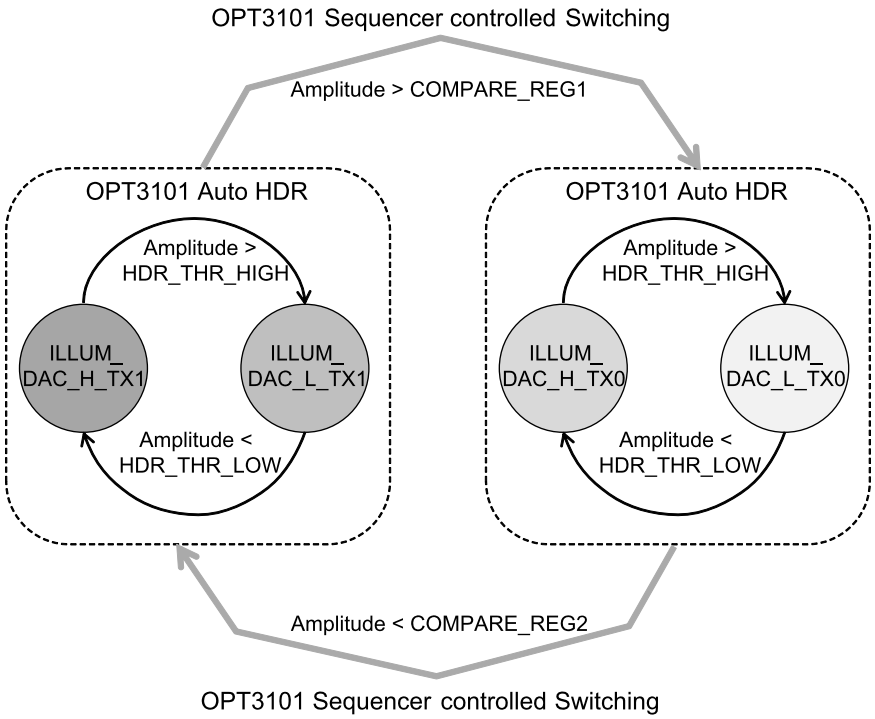

Figure 25. Super-HDR mode using Sequencer: State Diagram

Table 23. Register Settings to use Sequencer for Super HDR Mode

PARAMETER	VALUE	DESCRIPTION
Sequencer Interrupt Signal		
TG_SEQ_INT_START	9850	Set the sequencer interrupt at the end of the last averaged sub-frame after data ready is available
TG_SEQ_INT_END	9858	
TG_SEQ_INT_MASK_START	NUM_AVG_SUB_FRAMES	
TG_SEQ_INT_MASK_END	NUM_AVG_SUB_FRAMES	
Sequencer Commands		
COMMAND0	0x108	Set Illumination to Channel TX1
COMMAND1	0xB02	COMP1 command. If COMP_IN > COMPARE_REG1 move to Command2
COMMAND2	0x100	Set Illumination to Channel TX0
COMMAND3	0xC00	COMP1_INV command. If COMP_IN < COMPARE_REG2 move to Command2
Comparison Settings		
COMP_IN_SEL	0	Select amplitude AMP_OUT for COMP_IN
COMPARE_REG1	HDR_THR_HIGH + 500	should be greater than the hdr High threshold: HDR_THR_HIGH
COMPARE_REG2	HDR_THR_LOW - 500	should be less than the hdr low threshold HDR_THR_LOW.
Sequencer Enable		
EN_SEQUENCER	1	Enable the sequencer. Sequencer Enable should be only be changed while TG_EN = 0. Before changing this register disable TG (TG_EN = 0), modify this register and then enable TG (TG_EN = 1)
EN_PROCESSOR_VALUES	1	Enable processor values to control the STATUS_OUT register bits.

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7.4 Programming

OPT3101 supports I²C interface for register read and write access. Device also has an I²C host which can be used to interface with external temperature sensor or external EEPROM.

7.4.1 I²C Slave

The ²C slave interface can be accessed with SDA_S and SLC_S device pins. The I²C interface supports speeds up to 400 KHz I²C bus speed. The slave address for this device is 1011$A_2A_1A_0$. Using A_0, A_1, A_2 pins, address can be configured. By default A_0, A_1 and A_2 are pulled to AVDD supply and the default address is 1011,111. To change the address connect these pins to either AVDD or AVSS supply. The register access can be single R/W or continuous R/W with auto-increment of register address.

Table 24. I²C Slave Configuration Registers

FIELD	BIT	DESCRIPTION
I2C_CONT_RW	00h[6]	Enable continuous read/write of registers using device I²C slave

The individual registers are 24 bit length in this device. However, the register read/write is in chunks of eight bits. After every 8 bit transfer the slave expects an acknowledgement from the master in the case of read or gives out an acknowledgement in the case of write. Figure 26 shows the I²C timing for register write operation.

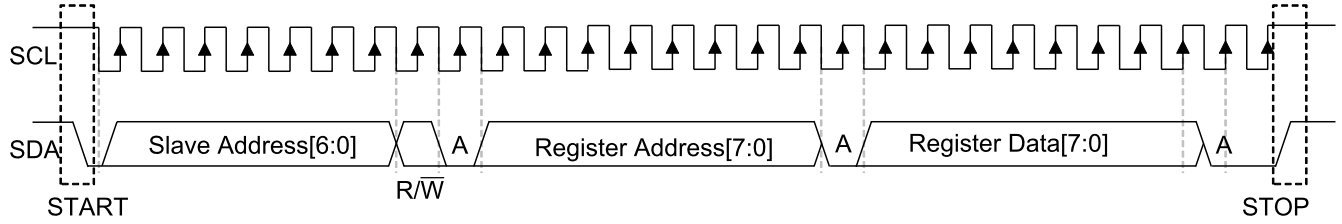

Figure 26. I²C Register Write Example

For example, to write 0x654321 to any register, the data should be split as three bytes and ordered as follows, 0x21, 0x43, 0x65. The same ordering is true for read mode. The first byte of data received corresponds to [7:0], followed by [15:8] and then followed by [23–16]. Figure 27 shows different read/write modes.

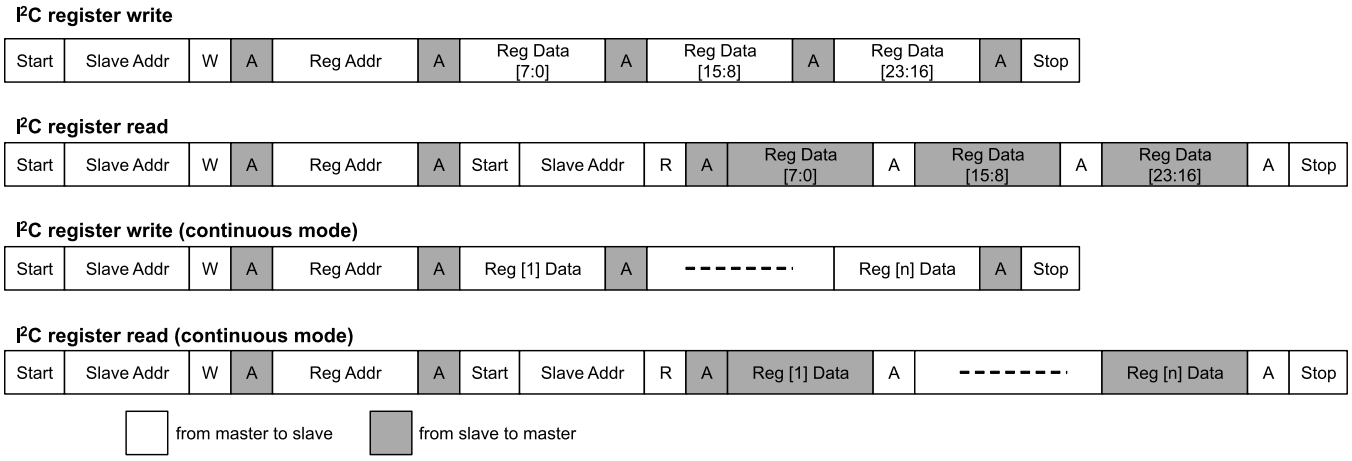

Figure 27. I²C Slave Interface R/W Modes

7.4.2 I²C Master

OPT3101 also has an I²C master, which will be used to read calibration and configuration registers from an external memory with I²C interface (EEPROM with I²C address of 1010000) during power up. It can also read temperature from an external off-chip temperature sensor with I²C interface (default address of 1001000). Table 25 lists the register settings to configure I²C Host.

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Table 25. I²C Master Register Settings

PARAMETER	BIT	DESCRIPTION
TSENS_SLAVE0	02h[6:0]	I²C Slave Address. In multi-channel Illumination operation temperature sensor slave address is selected based on the channel being used for reading external temperature value (TX0: TSENS_SLAVE0, TX1: TSENS_SLAVE1, TX2: TSENS_SLAVE2)
I2C_HOST_EN	01h[19]	Enable I²C Host
FRAME_VD_TRIG	01h[17]	Trigger I²C host operation every frame VD
I2C_TRIG_REG	01h[18]	Manual trigger of I²C host by writing to this register
I2C_NUM_TRAN	03h[17]	0: 1 transactions 1: 2 transactions
I2C_RW	01h[21:20]	'0' – Write, '1' – Read LSB: First Transaction MSB: Second Transaction
I2C_NUM_BYTES_TRAN1	07h[17:16]	00 – 1 byte, 01 – 2 bytes
I2C_NUM_BYTES_TRAN2	05h[23:22]	00 – 1 byte, 01 – 2 bytes
I2C_WRITE_DATA1	03h[16:9]	First byte of I²C write transaction 8bit register address
I2C_WRITE_DATA2	07h[7:0]	Second byte of I²C write transaction 8bit register data to be written
I2C_SEL_READ_BYTES	07h[19:18]	Selects the byte of read data. 00 – 7:0 | 01 – 15:8 | 10 – 23:16 | 11 – 31:24
I2C_READ_DATA	03h[7:0]	I²C host read data can be accessed through this register.

7.4.2.1 External Temperature Sensor

Temperature sensor address can be configured through internal registers (TSENS_SLAVE0, TSENS_SLAVE1, TSENS_SLAVE2) . This sensor can be used for calibrating the system parameters with temperature changes. External temperature sensor is required if an external illumination driver is used. Typically on-die temperature sensor is sufficient if the internal illumination driver is used. The temperature readings are refreshed every frame. Device supports up to three temperature sensors to associate with three illumination channels. A single or two byte read operation is performed on each of the temperature sensors to read the corresponding temperature. TI's TMP102, 12-bit temperature sensor is suggested if accurate temperature correction with smaller jumps at the temperature code changes is required. TMP103, 8-bit temperature sensor can be used if the temperature correction accuracy requirement is less. For temperature calibration of phase, the value read from the temperature sensor is assumed to be linear with the actual temperature. Register settings to configure external temperature sensor read using I²C Host are listed in Table 26.

Table 26. Register Settings to Enable External Temperature Readout Using I²C master

PARAMETER	VALUE for TMP102	VALUE for TMP103A	DESCRIPTION
TSENS_SLAVE0	0x48	0x70	External temperature sensor I²C slave address.
EN_TILLUM_READ	1	1	Enable reading of external temperature sensor using I²C Master
TEMP_AVG_ILLUM	0	2	0: no averaging for TMP102, this is already 12bit data. Futher averaging not required. 2: 4 averages for TMP103A
I2C_HOST_EN	1	1	Enable I²C master
I2C_NUM_TRAN	0	0	One read transaction
I2C_RW	1	1	Read transaction
I2C_NUM_BYTES_TRAN1	1	0	1: Two byte read for TMP102 0: One byte read for TMP103A
FRAME_VD_TRIG	1	1	Trigger temperature read for every frame
CONFIG_TILLUM_MSB	8	0	Mode to select the correct 12 bits from read 16 bits in two byte read for TMP102

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Table 26. Register Settings to Enable External Temperature Readout Using I²C master (continued)

PARAMETER	VALUE for TMP102	VALUE for TMP103A	DESCRIPTION
EN_TILLUM_12B	1	0	Enable 12-bit mode to read 12-bit temperature sensor data from external temperature sensor.

7.4.2.2 External EEPROM

The I²C host of the OPT3101 automatically loads all of the registers (256 bytes) from external EEPROM of 2kb (256 × 8) to configure the device. Of these 256 bytes, 64 bytes are register address, and 192 bytes are data bytes. So from EEPROM, device can auto load up to any 64 device registers of 24 bits each (64 × 24). EEPROM Data should be written in the following format. If only part of the memory is used, rest of the memory should be filled will all 0x00 or 0xFF.

Table 27. External EEPROM Data Format

Address	Data [7:0]
0	Reg Address i
1	Reg Data i[7:0]
2	Reg Data i[15:8]
3	Reg Data i[23:16]
4	Reg Address j
5	Reg Data j[7:0]
6	Reg Data j[15:8]
7	Reg Data j[23:16]
…	…
255	Reg Data k[23:16]

During I²C host auto load, if external host writes to OPT3101 I²C slave, it will respond (acknowledge) but data transfer doesn't happen (write/read). Register address '0' of OPT3101 cannot be loaded from I²C host. It is always reserved for I²C slave. By writing to register bit 0[22] (FORCE_EN_SLAVE) of OPT3101, I²C slave can take control of register access from host auto load. If the device is to be used in Mono-shot mode, I²C host power down disable should be written first (DIS_GLB_PD_I2CHOST) before writing mono-shot mode enable (MONOSHOT_MODE) bit in the EEPROM.

7.4.2.3 External EEPROM Programming

To simplify the EEPROM programming in the end system, OPT3101 supports writing to EEPROM through the device I²C slave . The device auto loads from EEPROM on reset. Before programming EEPROM, this auto load might corrupt the registers. First Erase the EEPROM and follow the flowchart shown in Figure 15. Register settings to write to external EEPROM on OPT3101 I²C Host through OPT3101 I²C slave are listed in Table 28.

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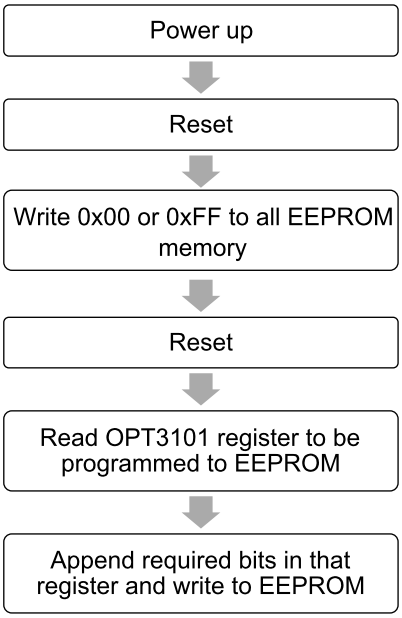

Figure 28. EEPROM Programming Flow Chart

Table 28. Register Settings to Write External EEPROM Using I^2C Master

PARAMETER	VALUE	DESCRIPTION
TSENS_SLAVE0	50h	EEPROM I^2C Address. EEPROM with this I^2C slave address should be used.
I2C_HOST_EN	1	
I2C_NUM_TRAN	0	Number of I^2C Master transactions = 1
I2C_RW	0	Write transaction
I2C_NUM_BYTES_TRAN1	1	2 byte trasaction (Register Address, Register Data)
I2C_WRITE_DATA1		EEPROM Register Address
I2C_WRITE_DATA2		Data to be written
I2C_TRIG_REG	1 → 0	Trigger the I^2C Host write by writing 1 to this register and make it 0

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7.5 Register Maps

7.5.1 Serial Interface Register Map

Table 29. Default Register Map

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	MONO SHOT_ BIT	FORCE _EN_S LAVE	FORCE _EN_B YPASS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	I2C_C ONT_R W	0	0	0	0	0	SOFT_ RST
01h	EN_EE PROM_ READ	0	I2C_RW		I2C_EN	I2C_TR IG_RE G	FRAME _VD_T RIG	EEPROM_START_REG_ADDR								ADDR_SLAVE_EEPROM							SWAP_ READ_ DATA	EEPRO M_REA D_TRI G
02h	TEMP_AVG_ILLU M		EN_TIL LUM_R EAD	TSENS_SLAVE2							TSENS_SLAVE1							TSENS_SLAVE0						
03h	TEMP_AVG_MAI N		0	0	0	EN_TS ENS_R EAD_F VD	I2C_NU M_TRA N	I2C_WRITE_DATA1								INIT_L OAD_D ONE	I2C_READ_DATA							
04h	TILLUM _UNSI GNED	0	0	0	TILLUM												0	0	0	1	0	1	1	1
05h	I2C_NUM_BYTE S_TRAN2		0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
07h	CONFIG_TILLUM_MSB				I2C_SEL_READ_ BYTES		I2C_NUM_BYTE S_TRAN1		0	0	0	0	0	0	0	0	I2C_WRITE_DATA2							
08h	FRAME _COUN T0	AMB_O VL_FL AG	MOD_F REQ	FRAME _STAT US	TX_CHANNEL		HDR_M ODE	PHASE _OVER FLOW	PHASE_OUT															
09h	DEALIAS_BIN				PHASE _OVER FLOW_ F2	SIG_O VL_FL AG	FRAME_COUNT 1		AMP_OUT															
0Ah	TMAIN												AMB_DATA										FRAME_COUNT 2	
0Bh	AMB_CALIB										DIG_GPO_SEL2				0	0	DIG_GPO_SEL1				DIG_GPO_SEL0			
0Ch	AMB_PHASE_CORR_PWL_COEFF0								AMB_XTALK_QPHASE_COEFF								AMB_XTALK_IPHASE_COEFF							
0Dh	EN_TIL LUM_1 2B	0	0	0	0	0	0	AMB_SAT_THR										0	0	0	0	0	0	0
0Fh	EN_FR EQ_CO RR	EN_FL OOP	EN_AU TO_FR EQ_CO UNT	SYS_CLK_DIVIDER			START _FREQ _CALIB	0	REF_COUNT_LIMIT															
10h	AMPLITUDE_MIN_THR[15:8]								EN_CO NT_FC ALIB	FREQ_COUNT_READ_REG														

Table 29. Default Register Map (continued)

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11h	AMPLITUDE_MIN_THR[7:0]								DIS_OVL_GATING	FREQ_COUNT_REG														
13h	0	0	0	0	0	COMPARE_REG1																MUX_SEL_COMPIN		
14h	0	0	0	0	DIS_INTERRUPT	STATUS_IN_REG	EN_PROCESSOR_VALUES	EN_SEQUENCER	COMPARE_REG2															
15h	COMMAND1												COMMAND0											
16h	COMMAND3												COMMAND2											
17h	COMMAND5												COMMAND4											
18h	COMMAND7												COMMAND6											
19h	COMMAND9												COMMAND8											
1Ah	COMMAND11												COMMAND10											
1Bh	COMMAND13												COMMAND12											
1Ch	COMMAND15												COMMAND14											
1Dh	COMMAND17												COMMAND16											
1Eh	COMMAND19												COMMAND18											
26h	POWERUP_DELAY														0	0	0	0	0	0	1	1	1	1
27h	MONOSHOT_FZ_CLKCNT																MONOSHOT_NUMFRAME						MONOSHOT_MODE	
29h	ILLUM_DAC_L_TX2[4:1]				ILLUM_DAC_H_TX1					ILLUM_DAC_L_TX1					ILLUM_DAC_H_TX0					ILLUM_DAC_L_TX0				
2Ah	ILLUM_DAC_L_TX2[0]	ILLUM_DAC_H_TX2					0	SEL_HDR_MODE	EN_ADAPTIVE_HDR	TX_SEQ_REG												SEL_TX_CH		EN_TX_SWITCH
2Bh	0	0	ILLUM_SCALE_H_TX0			ILLUM_SCALE_L_TX0			HDR_THR_HIGH															
2Ch	0	0	ILLUM_SCALE_H_TX1			ILLUM_SCALE_L_TX1			HDR_THR_LOW															
2Dh	TEMP_COEFF_MAIN_HDR0_TX1												TEMP_COEFF_MAIN_HDR1_TX0											
2Eh	XTALK_FILT_TIME_CONST				ILLUM_XTALK_REG_SCALE			INT_XTALK_REG_SCALE			0	ILLUM_XTALK_CALIB	IQ_READ_DATA_SEL		USE_XTALK_REG_ILLUM	USE_XTALK_FILT_ILLUM	USE_XTALK_REG_INT	USE_XTALK_FILT_INT	INT_XTALK_CALIB	DIS_AUTO_SCALE	FORCE_SCALE_VAL			
2Fh	TEMP_COEFF_MAIN_HDR1_TX1[11:4]								IPHASE_XTALK_REG_HDR0_TX0															
30h	TEMP_COEFF_MAIN_HDR1_TX1[3:0]				0	0	0	0	QPHASE_XTALK_REG_HDR0_TX0															
31h	TEMP_COEFF_MAIN_HDR0_TX2[11:4]								IPHASE_XTALK_REG_HDR1_TX0															
32h	TEMP_COEFF_MAIN_HDR0_TX2[3:0]				0	0	0	0	QPHASE_XTALK_REG_HDR1_TX0															
33h	TEMP_COEFF_MAIN_HDR1_TX2[11:4]								IPHASE_XTALK_REG_HDR0_TX1															
34h	TEMP_COEFF_MAIN_HDR1_TX2[3:0]				0	0	0	0	QPHASE_XTALK_REG_HDR0_TX1															
35h	0	0	0	0	0	0	0	0	IPHASE_XTALK_REG_HDR1_TX1															
36h	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX0								QPHASE_XTALK_REG_HDR1_TX1															
37h	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX0								IPHASE_XTALK_REG_HDR0_TX2															

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Table 29. Default Register Map (continued)

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
38h	TEMP_COEFF_XTALK_IPHASE_HDR0_TX0								QPHASE_XTALK_REG_HDR0_TX2															
39h	TEMP_COEFF_XTALK_QPHASE_HDR0_TX0								IPHASE_XTALK_REG_HDR1_TX2															
3Ah	0	SCALE_AMB_XTALK_COEFF			SCALE_TEMP_COEFF_XTALK			EN_TEMP_XTALK_CORR	QPHASE_XTALK_REG_HDR1_TX2															
3Bh	IPHASE_XTALK																							
3Ch	QPHASE_XTALK																							
3Dh	0	0	0	0	0	0	0	0	IPHASE_XTALK_INT_REG															
3Eh	0	0	0	0	0	0	0	0	QPHASE_XTALK_INT_REG															
3Fh	TILLUM_CALIB_HDR0_TX2												TMAIN_CALIB_HDR0_TX2											
40h	0	EN_MULTI_FREQ_PHASE	NCR_CONFIG	BETA0_DEALIAS_SCALE					ALPHA0_DEALIAS_SCALE						1	1	1	1	0	0	0	0	EN_DEALIAS_MEAS	
41h	TMAIN_CALIB_HDR1_TX1												BETA1_DEALIAS_SCALE			ALPHA1_DEALIAS_SCALE								
42h	0	0	0	0	0	0	0	0	PHASE_OFFSET_HDR0_TX0															
43h	TILLUM_CALIB_HDR1_TX1												0	0	0	SCALE_PHASE_TEMP_COEFF			0	0	0	0	EN_TEMP_CORR	EN_PHASE_CORR
44h	0	0	0	0	0	0	0	0	PHASE2_OFFSET_HDR0_TX0															
45h	TMAIN_CALIB_HDR1_TX2												TEMP_COEFF_MAIN_HDR0_TX0											
46h	TILLUM_CALIB_HDR1_TX2												TEMP_COEFF_ILLUM_HDR0_TX0											
47h	TILLUM_CALIB_HDR0_TX0												TMAIN_CALIB_HDR0_TX0											
48h	TILLUM_CALIB_HDR1_TX0												TMAIN_CALIB_HDR1_TX0											
49h	TILLUM_CALIB_HDR0_TX1												TMAIN_CALIB_HDR0_TX1											
4Ah	0	0	0	0	SCALE_NL_CORR_COEFF				A0_COEFF_HDR0_TX0														0	EN_NL_CORR
4Bh	0	0	0	0	0	0	0	0	A1_COEFF_HDR0_TX0															
4Ch	0	0	0	0	0	0	0	0	A2_COEFF_HDR0_TX0															
4Dh	0	0	0	0	0	0	0	0	A3_COEFF_HDR0_TX0															
4Eh	0	0	0	0	0	0	0	0	A4_COEFF_HDR0_TX0															
50h	0	OVERRIDE_CLKGEN_REG	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	CLIP_MODE_OFFSET	CLIP_MODE_TEMP	CLIP_MODE_NL	CLIP_MODE_FC
51h	TEMP_COEFF_ILLUM_HDR1_TX0[11:4]								PHASE_OFFSET_HDR1_TX0															
52h	TEMP_COEFF_ILLUM_HDR1_TX0[3:0]				0	0	0	0	PHASE_OFFSET_HDR0_TX1															
53h	TEMP_COEFF_ILLUM_HDR0_TX1[11:4]								PHASE_OFFSET_HDR1_TX1															
54h	TEMP_COEFF_ILLUM_HDR0_TX1[3:0]				0	0	0	0	PHASE_OFFSET_HDR0_TX2															
55h	TEMP_COEFF_ILLUM_HDR1_TX1[11:4]								PHASE_OFFSET_HDR1_TX2															

Table 29. Default Register Map (continued)

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
56h	TEMP_COEFF_ILLUM_HDR1_TX1[3:0]				0	0	0	0	PHASE2_OFFSET_HDR1_TX0															
57h	TEMP_COEFF_ILLUM_HDR0_TX2[11:4]								PHASE2_OFFSET_HDR0_TX1															
58h	TEMP_COEFF_ILLUM_HDR0_TX2[3:0]				0	0	0	0	PHASE2_OFFSET_HDR1_TX1															
59h	TEMP_COEFF_ILLUM_HDR1_TX2[11:4]								PHASE2_OFFSET_HDR0_TX2															
5Ah	TEMP_COEFF_ILLUM_HDR1_TX2[3:0]				0	0	0	0	PHASE2_OFFSET_HDR1_TX2															
5Bh	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX1								TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX1								TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX0							
5Ch	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX0								TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX2								TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX2							
5Dh	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX2								TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX1								TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX1							
5Eh	TEMP_COEFF_XTALK_IPHASE_HDR0_TX1								TEMP_COEFF_XTALK_IPHASE_HDR1_TX0								TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX2							
5Fh	TEMP_COEFF_XTALK_IPHASE_HDR1_TX2								TEMP_COEFF_XTALK_IPHASE_HDR0_TX2								TEMP_COEFF_XTALK_IPHASE_HDR1_TX1							
60h	TEMP_COEFF_XTALK_QPHASE_HDR1_TX1								TEMP_COEFF_XTALK_QPHASE_HDR0_TX1								TEMP_COEFF_XTALK_QPHASE_HDR1_TX0							
61h	0	0	0	0	0	0	0	0	TEMP_COEFF_XTALK_QPHASE_HDR1_TX2								TEMP_COEFF_XTALK_QPHASE_HDR0_TX2							
64h	PROG_OVLDET_REFM			PROG_OVLDET_REFP			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
65h	DIS_OVLDET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6Eh	0	0	0	0	EN_TEMP_CONV	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
71h	0	0	0	0	0	0	UNMASK_ILLUMEN_INTXTALK	EN_ILLUM_CLK_GPIO	ILLUM_CLK_GPIO_MODE	0	0	DIS_ILLUM_CLK_TX	INVERT_AFE_CLK	0	INVERT_TG_CLK	SHUT_CLOCKS	0	SHIFT_ILLUM_PHASE				DEALIAS_FREQ	DEALIAS_EN	0
72h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IAMB_MAX_SEL				0	0	0	0
76h	0	0	0	0	0	0	0	0	0	0	0	0	PDN_GLOBAL	0	DIS_GLB_PD_I2CHOST	DIS_GLB_PD_OSC	DIS_GLB_PD_TEST_CURR	DIS_GLB_PD_AMB_ADC	DIS_GLB_PD_AMB_DAC	DIS_GLB_PD_AFE_DAC	DIS_GLB_PD_AFE	DIS_GLB_PD_ILLUM_DRV	DIS_GLB_PD_TEMP_SENS	DIS_GLB_PD_REFSYS
77h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EN_DYN_PD_I2CHOST_OSC	EN_DYN_PD_OSC	EN_DYN_PD_TEST_CURR	EN_DYN_PD_AMB_ADC	EN_DYN_PD_AMB_DAC	EN_DYN_PD_AFE_DAC	EN_DYN_PD_AFE	EN_DYN_PD_LED_DRV	EN_DYN_PD_TEMP_SENS	EN_DYN_PD_REFSYS
78h	0	SEL_GP3_ON_SDAM	0	0	0	0	0	GPIO2_IBUF_EN	GPIO2_OBUF_EN	0	GPIO1_IBUF_EN	GPIO1_OBUF_EN	GPO2_MUX_SEL			GPO1_MUX_SEL			0	0	0	GPO3_MUX_SEL		
79h	0	0	0	0	PDN_ILLUM_DRV	0	0	0	0	0	0	PDN_ILLUM_DC_CURR	ILLUM_DC_CURR_DAC				0	0	0	EN_TX_DC_CURR_ALL	SEL_ILLUM_TX0_ON_TX1	EN_TX_CLKZ	0	EN_TX_CLKB
7Ah	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TX0_PIN_CONFIG		TX2_PIN_CONFIG		TX1_PIN_CONFIG	
80h	DIS_TG_ACONF	0	0	0	0	0	0	SUB_VD_CLK_CNT																TG_EN
83h	0	0	0	0	0	0	0	0	TG_AFE_RST_START															

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Table 29. Default Register Map (continued)

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
84h	0	0	0	0	0	0	0	0	TG_AFE_RST_END															
85h	0	0	0	0	0	0	0	0	TG_SEQ_INT_START															
86h	0	0	0	0	0	0	0	0	TG_SEQ_INT_END															
87h	0	0	0	0	0	0	0	0	TG_CAPTURE_START															
88h	0	0	0	0	0	0	0	0	TG_CAPTURE_END															
89h	0	0	0	0	0	0	0	0	TG_OVL_WINDOW_START															
8Ah	0	0	0	0	0	0	0	0	TG_OVL_WINDOW_END															
8Fh	0	0	0	0	0	0	0	0	TG_ILLUMEN_START															
90h	0	0	0	0	0	0	0	0	TG_ILLUMEN_END															
91h	0	0	0	0	0	0	0	0	TG_CALC_START															
92h	0	0	0	0	0	0	0	0	TG_CALC_END															
93h	0	0	0	0	0	0	0	0	TG_DYNPDN_START															
94h	0	0	0	0	0	0	0	0	TG_DYNPDN_END															
97h	TG_SEQ_INT_MASK_END												TG_SEQ_INT_MASK_START											
98h	TG_CAPTURE_MASK_END												TG_CAPTURE_MASK_START											
99h	TG_OVL_WINDOW_MASK_END												TG_OVL_WINDOW_MASK_START											
9Ch	TG_ILLUMEN_MASK_END												TG_ILLUMEN_MASK_START											
9Dh	TG_CALC_MASK_END												TG_CALC_MASK_START											
9Eh	TG_DYNPDN_MASK_END												TG_DYNPDN_MASK_START											
9Fh	NUM_AVG_SUB_FRAMES												NUM_SUB_FRAMES											
A0h	0	0	0	0	0	0	0	0	CAPTURE_CLK_CNT															
A2h	A3_COEFF_HDR0_TX1[15:8]								A0_COEFF_HDR1_TX0															
A3h	A3_COEFF_HDR0_TX1[7:0]								A0_COEFF_HDR0_TX1															
A4h	A3_COEFF_HDR1_TX1[15:8]								A0_COEFF_HDR1_TX1															
A5h	A3_COEFF_HDR1_TX1[7:0]								A0_COEFF_HDR0_TX2															
A6h	A3_COEFF_HDR0_TX2[15:8]								A0_COEFF_HDR1_TX2															
A7h	A3_COEFF_HDR0_TX2[7:0]								A1_COEFF_HDR1_TX0															
A8h	A3_COEFF_HDR1_TX2[15:8]								A1_COEFF_HDR0_TX1															
A9h	A3_COEFF_HDR1_TX2[7:0]								A1_COEFF_HDR1_TX1															
AAh	A4_COEFF_HDR1_TX0[15:8]								A1_COEFF_HDR0_TX2															
ABh	A4_COEFF_HDR1_TX0[7:0]								A1_COEFF_HDR1_TX2															
ACh	A4_COEFF_HDR0_TX1[15:8]								A2_COEFF_HDR1_TX0															
ADh	A4_COEFF_HDR0_TX1[7:0]								A2_COEFF_HDR0_TX1															
AEh	A4_COEFF_HDR1_TX1[15:8]								A2_COEFF_HDR1_TX1															
AFh	A4_COEFF_HDR1_TX1[7:0]								A2_COEFF_HDR0_TX2															
B0h	A4_COEFF_HDR0_TX2[15:8]								A2_COEFF_HDR1_TX2															
B1h	A4_COEFF_HDR0_TX2[7:0]								A3_COEFF_HDR1_TX0															
B2h	0	0	0	0	0	0	0	0	A4_COEFF_HDR1_TX2															
B4h	AMB_PHASE_CORR_PWL_COEFF3								AMB_PHASE_CORR_PWL_COEFF2								AMB_PHASE_CORR_PWL_COEFF1							

Table 29. Default Register Map (continued)

ADDRESS (Hex)	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SCALE_AMB_PHASE_CORR_COEFF		
B8h	0	0	0	GIVE_DEALIAS_DATA	AMB_PHASE_CORR_PWL_X1										AMB_PHASE_CORR_PWL_X0									
B9h	ILLUM_SCALE_H_TX2			ILLUM_SCALE_L_TX2			AMB_ADC_IN_TX2		AMB_ADC_IN_TX1		AMB_ADC_IN_TX0		EN_TX2_ON_TX0	EN_TX1_ON_TX0	AMB_PHASE_CORR_PWL_X2									

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7.5.1.1 Register Descriptions

7.5.1.1.1 Register 0h (Address = 0h) [reset = 0h]

Figure 29. Register 0h

23	22	21	20	19	18	17	16
MONOSHOT_BIT	FORCE_EN_SLAVE	FORCE_EN_BYPASS	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	I2C_CONT_RW	0	0	0	0	0	SOFT_RST

Table 30. Register 00 Field Descriptions

Bit	Field	Type	Reset	Description
23	MONOSHOT_BIT	R/W	0h	Mono-Shot trigger register. Write this bit 1 to start sample capture in monoshot mode. This bit will be auto cleared after the sample capture completion.
22	FORCE_EN_SLAVE	R/W	0h	Force enable device I2C slave register access from device I^2C host for any address.
21	FORCE_EN_BYPASS	R/W	0h	When this bit is set to 1, disables the device I^2C host and shorts the I^2C host bus and I^2C slave bus.
6	I2C_CONT_RW	R/W	0h	Enable continuous read/write of registers using device I^2C slave
0	SOFT_RST	R/W	0h	Generates devices reset upon writing this bit and resets all the register settings to default values including this bit.

7.5.1.1.2 Register 1h (Address = 1h) [reset = 120140h]

Figure 30. Register 1h

23	22	21	20	19	18	17	16
EN_EEPROM_READ	0	I2C_RW		I2C_EN	I2C_TRIG_REG	FRAME_VD_TRIG	EEPROM_START_REG_ADDR
R/W - 0h	R/W - 0h	R/W - 1h		R/W - 0h	R/W - 0h	R/W - 1h	R/W - 0h
15	14	13	12	11	10	9	8
EEPROM_START_REG_ADDR							ADDR_SLAVE_EEPROM
R/W - 0h							R/W - 1h
7	6	5	4	3	2	1	0
ADDR_SLAVE_EEPROM						SWAP_READ_DATA	EEPROM_READ_TRIG
R/W - 10h						R/W - 0h	R/W - 0h

Table 31. Register 01 Field Descriptions

Bit	Field	Type	Reset	Description
23	EN_EEPROM_READ	R/W	0h	Enable the EEPROM read with EEPROM_READ_TRIG
21:20	I2C_RW	R/W	1h	Choses the R/W for I^2C host operation. 0 – Write, 1 – Read LSB: First Transaction, MSB: Second Transaction
19	I2C_EN	R/W	0h	Enables the I^2C host.
18	I2C_TRIG_REG	R/W	0h	The trigger register for I^2C transaction.
17	FRAME_VD_TRIG	R/W	1h	When this bit is 1, the I^2C host is triggered every frame vd. Else it is triggered based on the I2C_TRIG_REG.
16:9	EEPROM_START_REG_ADDR	R/W	0h	The first EEPROM register address while reading from the EEPROM.

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Table 31. Register 01 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8:2	ADDR_SLAVE_EEPROM	R/W	50h	External EEPROM I^2C slave address.
1	SWAP_READ_DATA	R/W	0h	Swaps/reverse the data read by I^2C host.
0	EEPROM_READ_TRIG	R/W	0h	Trigger auto load from EEPROM

7.5.1.1.3 Register 2h (Address = 2h) [reset = 92A4C8h]

Figure 31. Register 2h

23	22	21	20	19	18	17	16
TEMP_AVG_ILLUM		EN_TILLUM_READ	TSENS_SLAVE2				
R/W - 2h		R/W - 0h	R/W - 12h				
15	14	13	12	11	10	9	8
TSENS_SLAVE2		TSENS_SLAVE1					
R/W - 2h		R/W - 24h					
7	6	5	4	3	2	1	0
TSENS_SLAVE1	TSENS_SLAVE0						
R/W - 1h	R/W - 48h						

Table 32. Register 02 Field Descriptions

Bit	Field	Type	Reset	Description
23:22	TEMP_AVG_ILLUM	R/W	2h	Average external temperature sensor reading. 0: No average, 1: 2 sample average, 2: 4 sample average
21	EN_TILLUM_READ	R/W	0h	Enable I^2C read of appropriate external temperature sensor on I^2C host bus.
20:14	TSENS_SLAVE2	R/W	4Ah	Slave address of the external temperature sensor in proximity to TX2 Channel
13:7	TSENS_SLAVE1	R/W	49h	Slave address of the external temperature sensor in proximity to TX1 Channel
6:0	TSENS_SLAVE0	R/W	48h	Slave address of the external temperature sensor in proximity to TX0 Channel

7.5.1.1.4 Register 3h (Address = 3h) [reset = 800000h]

Figure 32. Register 3h

23	22	21	20	19	18	17	16
TEMP_AVG_MAIN		0	0	0	EN_TSENS_READ_FVD	I2C_NUM_TRAN	I2C_WRITE_DATA1
R/W - 2h		R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
I2C_WRITE_DATA1							INIT_LOAD_DONE
R/W - 0h							R - 0h
7	6	5	4	3	2	1	0
I2C_READ_DATA							
R - 0h							

Table 33. Register 03 Field Descriptions

Bit	Field	Type	Reset	Description
23:22	TEMP_AVG_MAIN	R/W	0h	Average on chip temperature sensor reading. 0: No Average, 1: 2 sample average, 2: 4 sample average

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Table 33. Register 03 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18	EN_TSENS_READ_FVD	R/W	0h	If this bit is set TMAIN temperature is read every frame.
17	I2C_NUM_TRAN	R/W	0h	The number of I^2C host transactions. 0: 1, 1: 2.
16:9	I2C_WRITE_DATA1	R/W	0h	The address where the read would start. Normally in temperature sensor read this is not required to be programmed.
8	INIT_LOAD_DONE	R	0h	Can be used to check whether initial auto load from EEPROM is successful or not.
7:0	I2C_READ_DATA	R	0h	The I^2C host read data.

7.5.1.1.5 Register 4h (Address = 4h) [reset = 17h]

Figure 33. Register 4h

23	22	21	20	19	18	17	16
TILLUM_UNSIGNED	0	0	0	TILLUM			
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R - 0h			
15	14	13	12	11	10	9	8
TILLUM							
R - 0h							
7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	1
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h	R/W - 0h	R/W - 1h	R/W - 0h	R/W - 1h

Table 34. Register 04 Field Descriptions

Bit	Field	Type	Reset	Description
23	TILLUM_UNSIGNED	R/W	0h	Set this bit to 1 when temperature given by external temperature sensor is in unsigned format.
22:20	0	R/W	0h	Always read or write 0h.
19:8	TILLUM	R	0h	The temperature value of external temperature sensor.
7:0	23	R/W	17h	Always read or write 17h.

7.5.1.1.6 Register 5h (Address = 5h) [reset = 80000h]

Figure 34. Register 5h

23	22	21	20	19	18	17	16
I2C_NUM_BYTES_TRAN2		0	0	1	0	0	0
R/W-0h		R/W-0h	R/W-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 35. Register 05 Field Descriptions

Bit	Field	Type	Reset	Description
23:22	I2C_NUM_BYTES_TRAN2	R/W	0h	Number of bytes used in the transaction 2 of I^2C host transaction. 00 – 1 byte, 01 – 2 bytes
21:0	0	R/W	0h	Always read or write 0h.

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7.5.1.1.7 Register 7h (Address = 7h) [reset = 0h]

Figure 35. Register 7h

23	22	21	20	19	18	17	16
CONFIG_TILLUM_MSB				I2C_SEL_READ_BYTES		I2C_NUM_BYTES_TRAN1	
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
I2C_WRITE_DATA2							

Table 36. Register 07 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	CONFIG_TILLUM_MSB	R/W	0h	1000 – I^2C host read data[15:4], to support 12-bit external temperature sensor Also set EN_TILLUM_12B = 1
19:18	I2C_SEL_READ_BYTES	R/W	0h	Chooses which byte of I2C_READ register to be read on I2C_READ_DATA register 00 – 7:0 | 01 – 15:8 | 10 – 23:16 | 11 – 31:24
17:16	I2C_NUM_BYTES_TRAN1	R/W	0h	Number of bytes used in the transaction 1 of i2c host transaction. 00 – 1 byte, 01 – 2 bytes
7:0	I2C_WRITE_DATA2	R/W	0h	Second byte of I^2C write transaction. 8-bit register data to be written

7.5.1.1.8 Register 8h (Address = 8h) [reset = 0h]

Figure 36. Register 8h

23	22	21	20	19	18	17	16
FRAME_COUNT0	AMB_OVL_FLAG	MOD_FREQ	FRAME_STATUS	TX_CHANNEL		HDR_MODE	PHASE_OVER_FLOW
15	14	13	12	11	10	9	8
PHASE_OUT							
7	6	5	4	3	2	1	0
PHASE_OUT							

Table 37. Register 08 Field Descriptions

Bit	Field	Type	Reset	Description
23	FRAME_COUNT0	R	0h	Frame counter LSB bit.
22	AMB_OVL_FLAG	R	0h	Overload flag to indicate ambient saturation
21	MOD_FREQ	R	0h	Indicates the frequency used. 0 – 10 MHz, 1 – de-alias frequency (10 MHz × 6 / 7 or 10 MHz × 6 / 5)
20	FRAME_STATUS	R	0h	1 – valid frame; 0 – invalid frame. Frame can be invalid during crosstalk correction frame etc.
19:18	TX_CHANNEL	R	0h	Indicates which Illumination channel of TX0/TX1/TX2 is used.
17	HDR_MODE	R	0h	Indicates the illumination driver DAC current used. 0 = ILLUM_DAC_L, 1 = ILLUM_DAC_H
16	PHASE_OVER_FLOW	R	0h	PHASE_OUT overflow bit during frequency correction
15:0	PHASE_OUT	R	0h	Final calibrated phase.

7.5.1.1.9 Register 9h (Address = 9h) [reset = 0h]

Figure 37. Register 9h

23	22	21	20	19	18	17	16
DEALIAS_BIN				PHASE_OVER_FLOW_F2	SIG_OVL_FLAG	FRAME_COUNT1	
15	14	13	12	11	10	9	8

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AMP_OUT							
7	6	5	4	3	2	1	0
AMP_OUT							

Table 38. Register 09 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	DEALIAS_BIN	R	0h	Distance bin in de-alias mode.
19	PHASE_OVERFLOW_F2	R	0h	Phase overflow of second modulation frequency during frequency correction.
18	SIG_OVL_FLAG	R	0h	Overload flag to indicate signal saturation
17:16	FRAME_COUNT 1	R	0h	Frame Counter Bits [2:1]
15:0	AMP_OUT	R	0h	Amplitude of the signal.

7.5.1.1.10 Register Ah (Address = Ah) [reset = 0h]

Figure 38. Register Ah

23	22	21	20	19	18	17	16
TMAIN							
15	14	13	12	11	10	9	8
TMAIN				AMB_DATA			
7	6	5	4	3	2	1	0
AMB_DATA						FRAME_COUNT2	

Table 39. Register 0A Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TMAIN	R	0h	On chip temperature sensor output temperature (°C)= TMAIN / 8 – 256
11:2	AMB_DATA	R	0h	Ambient ADC output. Indicates the ambient light.
1:0	FRAME_COUNT2	R	0h	Frame counter MSB Bits [4:3].

7.5.1.1.11 Register Bh (Address = Bh) [reset = FC009h]

Figure 39. Register Bh

23	22	21	20	19	18	17	16
AMB_CALIB							
R/W - 0Fh							
15	14	13	12	11	10	9	8
AMB_CALIB			GPO_SEL2			0	0
R/W - 3h			R/W - 0h			R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
DIG_GPO_SEL1				DIG_GPO_SEL0			
R/W - 0h				R/W - 9h			

Table 40. Register 0B Field Descriptions

Bit	Field	Type	Reset	Description
23:14	AMB_CALIB	R/W	3Fh	The ambient ADC value at which device is calibrated for phase offset
13:10	DIG_GPO_SEL2	R/W	0h	Mux selection bits for digital signal DIG_GPO_2 which can be brought out on GP3 (SDA_M)
9:8	0	R/W	0h	Always read or write 0h.
7:4	DIG_GPO_SEL1	R/W	0h	Mux selection bits for digital signal DIG_GPO_1 which can be brought out on GP1/GP2 0: FRAME VD | 1: SUB-VD | 4: SEQUENCER INTERRUPT 8: COMP_STATUS | 9: DATA_RDY | 10: FRAME_COUNTER_LSB

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Table 40. Register 0B Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	DIG_GPO_SEL0	R/W	9h	Mux selection bits for digital signal DIG_GPO_0 which can be brought out on GP1/GP2 0: FRAME VD | 1: SUB-VD | 4: SEQUENCER INTERRUPT 8: COMP_STATUS | 9: DATA_RDY | 10: FRAME_COUNTER_LSB

7.5.1.1.12 Register Ch (Address = Ch) [reset = 0h]

Figure 40. Register Ch

23	22	21	20	19	18	17	16
AMB_PHASE_CORR_PWL_COEFF0							
15	14	13	12	11	10	9	8
AMB_XTALK_QPHASE_COEFF							
7	6	5	4	3	2	1	0
AMB_XTALK_IPHASE_COEFF							

Table 41. Register 0C Field Descriptions

Bit	Field	Type	Reset	Description
23:16	AMB_PHASE_CORR_PWL_COEFF0	R/W	0h	Coefficient 0 for PWL phase correction with ambient
15:8	AMB_XTALK_QPHASE_COEFF	R/W	0h	Coefficient to correct for the crosstalk (Quadrature component) change with ambient.
7:0	AMB_XTALK_IPHASE_COEFF	R/W	0h	Coefficient to correct for the crosstalk (Inpase component) change with ambient.

7.5.1.1.13 Register Dh (Address = Dh) [reset = 6000h]

Figure 41. Register Dh

23	22	21	20	19	18	17	16
EN_TILLUM_12B	0	0	0	0	0	0	AMB_SAT_THR
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
AMB_SAT_THR							
R/W - 60h							
7	6	5	4	3	2	1	0
AMB_SAT_THR	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

Table 42. Register 0D Field Descriptions

Bit	Field	Type	Reset	Description
23	EN_TILLUM_12B	R/W	0h	Enables support for external temperature sensor with more than 8-bit resolution on I^2C host bus. Preferred 12-bit temperature sensor: TMP102:
22:17	0	R/W	0h	Always read or write 0h.
16:7	AMB_SAT_THR	R/W	C0h	Ambient threshold which is used to detect the ambient overload. AMB_DATA - AMB_CALIB is compared against this threshold value and AMB_OVL_FLAG is set to 1 if it exceeds the threshold.
6:0	0	R/W	0h	Always read or write 0h.

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7.5.1.1.14 Register Fh (Address = Fh) [reset = 144C4Bh]

Figure 42. Register Fh

23	22	21	20	19	18	17	16
EN_FREQ_CORR	EN_FLOOP	EN_AUTO_FREQ_COUNT	SYS_CLK_DIVIDER				START_FREQ_CALIB
R/W - 0h	R/W - 0h	R/W - 0h	R/W - Ah				R/W - 0h
15	14	13	12	11	10	9	8
0	REF_COUNT_LIMIT						
R/W - 0h	R/W - 4Ch						
7	6	5	4	3	2	1	0
REF_COUNT_LIMIT							
R/W - 4Bh							

Table 43. Register 0F Field Descriptions

Bit	Field	Type	Reset	Description
23	EN_FREQ_CORR	R/W	0h	Enable frequency correction for the phase output
22	EN_FLOOP	R/W	0h	Enables the frequency calibration block.
21	EN_AUTO_FREQ_COUNT	R/W	0h	Determines which value to be used for frequency correction. 0 – On hip trimmed value, 1 – Measured value from frequency calibration
20:17	SYS_CLK_DIVIDER	R/W	Ah	Programs system clock divider for frequency calibration. This should be adjusted to get it closer to the external reference frequency. The default is 10, system clock = 40 MHz / 2^{10} = 39.0625 kHz to bring close to 32.768 kHz.
16	START_FREQ_CALIB	R/W	0h	starts the frequency calibration.
14:0	REF_COUNT_LIMIT	R/W	4C4Bh	This sets the limit for ref-clock count. Write this register with value = (40e6 / $2^{SYS\_CLK\_DIVIDER}$) / f_{EXT}

7.5.1.1.15 Register 10h (Address = 10h) [reset = 4000h]

Figure 43. Register 10h

23	22	21	20	19	18	17	16
AMPLITUDE_MIN_THR[15:8]							
R/W - 0h							
15	14	13	12	11	10	9	8
EN_CONT_FCALIB	FREQ_COUNT_READ_REG						
R/W - 0h	R/W - 40h						
7	6	5	4	3	2	1	0
FREQ_COUNT_READ_REG							
R/W - 0h							

Table 44. Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	AMPLITUDE_MIN_THR[15:8]	R/W	0h	MSB of minimum amplitude threshold below which phase is made FFFFh.
15	EN_CONT_FCALIB	R/W	0h	Enables continuous frequency calibration. 0 – Frequency is measured only when START_FREQ_CALIB = 1; 1 – Frequency is continuously measured.
14:0	FREQ_COUNT_READ_REG	R	4000h	Read register which holds the value of frequency correction when frequency calibration is enabled. This value will be used for frequency correction when EN_AUTO_FREQ_COUNT = 1.

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7.5.1.1.16 Register 11h (Address = 11h) [reset = 0h]

Figure 44. Register 11h

23	22	21	20	19	18	17	16
AMPLITUDE_MIN_THR[7:0]							
15	14	13	12	11	10	9	8
DIS_OVL_GATING	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 45. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	AMPLITUDE_MIN_THR[7:0]	R/W	0h	LSB of minimum amplitude threshold below which phase is made FFFFh.
15	DIS_OVL_GATING	R/W	0h	Disable gating of phase output when SIG_OVL_FLAG becomes 1.
14:0	FREQ_COUNT_REG	R	0h	Digital frequency correction trim value. This value will be used for frequency correction when EN_AUTO_FREQ_COUNT = 0

7.5.1.1.17 Register 13h (Address = 13h) [reset = 0h]

Figure 45. Register 13h

23	22	21	20	19	18	17	16
0	0	0	0	0	COMPARE_REG1		
15	14	13	12	11	10	9	8
COMPARE_REG1							
7	6	5	4	3	2	1	0
COMPARE_REG1					MUX_SEL_COMPIN		

Table 46. Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
18:3	COMPARE_REG1	R/W	0h	Sequencer comparison threshold1 register
2:0	MUX_SEL_COMPIN	R/W	0h	choses the value used for comparator input register of sequencer. 0 = amplitude | 1 = de-alias bin | 2 = de-alias distance | 3 = phase

7.5.1.1.18 Register 14h (Address = 14h) [reset = 0h]

Figure 46. Register 14h

23	22	21	20	19	18	17	16
0	0	0	0	DIS_INTERRUPT	STATUS_IN_REG	EN_PROCESSOR_VALUES	EN_SEQUENCER
15	14	13	12	11	10	9	8
COMPARE_REG2							
7	6	5	4	3	2	1	0
COMPARE_REG2							

Table 47. Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
19	DIS_INTERRUPT	R/W	0h	Disables the interrupt which triggers sequencer.
18	STATUS_IN_REG	R/W	0h	the register is used to control the program flow in CPU
17	EN_PROCESSOR_VALUES	R/W	0h	Uses processor values instead of register values.
16	EN_SEQUENCER	R/W	0h	Enable the sequencer.

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Table 47. Register 14 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:0]	COMPARE_REG2	R/W	0h	Sequencer comparison threshold2 register

7.5.1.1.19 Register 15h (Address = 15h) [reset = 101063h]

Figure 47. Register 15h

23	22	21	20	19	18	17	16
COMMAND1							
R/W - 10h							
15	14	13	12	11	10	9	8
COMMAND1				COMMAND0			
R/W - 1h				R/W - 0h			
7	6	5	4	3	2	1	0
COMMAND0							
R/W - 63h							

Table 48. Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND1	R/W	101h	Sequencer command 1.
11:0	COMMAND0	R/W	63h	Sequencer command 0.

7.5.1.1.20 Register 16h (Address = 16h) [reset = 400100h]

Figure 48. Register 16h

23	22	21	20	19	18	17	16
COMMAND3							
R/W - 40h							
15	14	13	12	11	10	9	8
COMMAND3				COMMAND2			
R/W - 0h				R/W - 1h			
7	6	5	4	3	2	1	0
COMMAND2							
R/W - 00h							

Table 49. Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND3	R/W	400h	Sequencer command 3.
11:0	COMMAND2	R/W	100h	Sequencer command 2.

7.5.1.1.21 Register 17h (Address = 17h) [reset = 0h]

Figure 49. Register 17h

23	22	21	20	19	18	17	16
COMMAND5							
15	14	13	12	11	10	9	8
COMMAND5				COMMAND4			
7	6	5	4	3	2	1	0
COMMAND4							

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Table 50. Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND5	R/W	0h	Sequencer command 5.
11:0	COMMAND4	R/W	0h	Sequencer command 4.

7.5.1.1.22 Register 18h (Address = 18h) [reset = 0h]

Figure 50. Register 18h

23	22	21	20	19	18	17	16
COMMAND7							
15	14	13	12	11	10	9	8
COMMAND7				COMMAND6			
7	6	5	4	3	2	1	0
COMMAND6							

Table 51. Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND7	R/W	0h	Sequencer command 7.
11:0	COMMAND6	R/W	0h	Sequencer command 6.

7.5.1.1.23 Register 19h (Address = 19h) [reset = 0h]

Figure 51. Register 19h

23	22	21	20	19	18	17	16
COMMAND9							
15	14	13	12	11	10	9	8
COMMAND9				COMMAND8			
7	6	5	4	3	2	1	0
COMMAND8							

Table 52. Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND9	R/W	0h	Sequencer command 9.
11:0	COMMAND8	R/W	0h	Sequencer command 8.

7.5.1.1.24 Register 1Ah (Address = 1Ah) [reset = 0h]

Figure 52. Register 1Ah

23	22	21	20	19	18	17	16
COMMAND11							
15	14	13	12	11	10	9	8
COMMAND11				COMMAND10			
7	6	5	4	3	2	1	0
COMMAND10							

Table 53. Register 1A Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND11	R/W	0h	Sequencer command 11.
11:0	COMMAND10	R/W	0h	Sequencer command 10.

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7.5.1.1.25 Register 1Bh (Address = 1Bh) [reset = 0h]

Figure 53. Register 1Bh

23	22	21	20	19	18	17	16
COMMAND13							
15	14	13	12	11	10	9	8
COMMAND13				COMMAND12			
7	6	5	4	3	2	1	0
COMMAND12							

Table 54. Register 1B Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND13	R/W	0h	Sequencer command 13.
11:0	COMMAND12	R/W	0h	Sequencer command 12.

7.5.1.1.26 Register 1Ch (Address = 1Ch) [reset = 0h]

Figure 54. Register 1Ch

23	22	21	20	19	18	17	16
COMMAND15							
15	14	13	12	11	10	9	8
COMMAND15				COMMAND14			
7	6	5	4	3	2	1	0
COMMAND14							

Table 55. Register 1C Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND15	R/W	0h	Sequencer command 15.
11:0	COMMAND14	R/W	0h	Sequencer command 14.

7.5.1.1.27 Register 1Dh (Address = 1Dh) [reset = 0h]

Figure 55. Register 1Dh

23	22	21	20	19	18	17	16
COMMAND17							
15	14	13	12	11	10	9	8
COMMAND17				COMMAND16			
7	6	5	4	3	2	1	0
COMMAND16							

Table 56. Register 1D Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND17	R/W	0h	Sequencer command 17.
11:0	COMMAND16	R/W	0h	Sequencer command 16.

7.5.1.1.28 Register 1Eh (Address = 1Eh) [reset = 0h]

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Figure 56. Register 1Eh

23	22	21	20	19	18	17	16
COMMAND19							
15	14	13	12	11	10	9	8
COMMAND19				COMMAND18			
7	6	5	4	3	2	1	0
COMMAND18							

Table 57. Register 1E Field Descriptions

Bit	Field	Type	Reset	Description
23:12	COMMAND19	R/W	0h	Sequencer command 19.
11:0	COMMAND18	R/W	0h	Sequencer command 18.

7.5.1.1.29 Register 26h (Address = 26h) [reset = 4000Fh]

Figure 57. Register 26h

23	22	21	20	19	18	17	16
POWERUP_DELAY							
R/W - 04h							
15	14	13	12	11	10	9	8
POWERUP_DELAY						0	0
R/W - 00h						R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h	R/W - 1h	R/W - 1h	R/W - 1h

Table 58. Register 26 Field Descriptions

Bit	Field	Type	Reset	Description
23:10	POWERUP_DELAY	R/W	100h	Register to program the delay from the monoshot trigger to start of frame (FRAME_VD). Delay = (64 × POWERUP_DELAY + 2) × Tclk, Tclk = 25 ns.
9:0	15	R/W	Fh	Always read or write Fh.

7.5.1.1.30 Register 27h (Address = 27h) [reset = 26AC18h]

Figure 58. Register 27h

23	22	21	20	19	18	17	16
MONOSHOT_FZ_CLKCNT							
R/W - 26h							
15	14	13	12	11	10	9	8
MONOSHOT_FZ_CLKCNT							
R/W - ACh							
7	6	5	4	3	2	1	0
MONOSHOT_NUMFRAME		MONOSHOT_NUMFRAME				MONOSHOT_MODE	
		R/W - 6h				R/W - 0h	

Table 59. Register 27 Field Descriptions

Bit	Field	Type	Reset	Description
23:8	MONOSHOT_FZ_CLKCNT	R/W	26ACh	The CLK count at which a monoshot operation freezes.
7:2	MONOSHOT_NUMFRAME	R/W	6h	The number of samples to be captured on every monoshot trigger event.
1:0	MONOSHOT_MODE	R/W	0h	Select monoshot mode. 0 - Continuous Mode | 3 - Monoshot Mode

ADVANCE INFORMATION

7.5.1.1.31 Register 29h (Address = 29h) [reset = 3F0FC3h]

Figure 59. Register 29h

23	22	21	20	19	18	17	16
ILLUM_DAC_L_TX2[4:1]				ILLUM_DAC_H_TX1			
R/W - 3h				R/W - Fh			
15	14	13	12	11	10	9	8
ILLUM_DAC_H_TX1	ILLUM_DAC_L_TX1					ILLUM_DAC_H_TX0	
R/W - 0h	R/W - 03h					R/W - 3h	
7	6	5	4	3	2	1	0
ILLUM_DAC_H_TX0			ILLUM_DAC_L_TX0				
R/W - 6h			R/W - 03h				

Table 60. Register 29 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	ILLUM_DAC_L_TX2[4:1]	R/W	3h	Illumination driver current DAC register, ILLUM_DAC_L[4:1] of TX2 Channel
19:15	ILLUM_DAC_H_TX1	R/W	1Eh	Illumination driver current DAC register, ILLUM_DAC_H of TX1 Channel
14:10	ILLUM_DAC_L_TX1	R/W	3h	Illumination driver current DAC register, ILLUM_DAC_L of TX1 Channel
9:5	ILLUM_DAC_H_TX0	R/W	1Eh	Illumination driver current DAC register, ILLUM_DAC_H of TX0 Channel
4:0	ILLUM_DAC_L_TX0	R/W	3h	Illumination driver current DAC register, ILLUM_DAC_L of TX0 Channel

7.5.1.1.32 Register 2Ah (Address = 2Ah) [reset = 784920h]

Figure 60. Register 2Ah

23	22	21	20	19	18	17	16
ILLUM_DAC_L_TX2[0]	ILLUM_DAC_H_TX2					0	SEL_HDR_MODE
R/W - 0h	R/W - 1Eh					R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
EN_ADAPTIVE_HDR	TX_SEQ_REG						
R/W - 0h	R/W - 49h						
7	6	5	4	3	2	1	0
TX_SEQ_REG						SEL_TX_CH	EN_TX_SWITCH
R/W - 04h						R/W - 0h	R/W - 0h

Table 61. Register 2A Field Descriptions

Bit	Field	Type	Reset	Description
23	ILLUM_DAC_L_TX2[0]	R/W	1h	Illumination driver current DAC register, ILLUM_DAC_L[0] of TX2 Channel
22:18]	ILLUM_DAC_H_TX2	R/W	1Eh	Illumination driver current DAC register, ILLUM_DAC_H of TX2 Channel
16	SEL_HDR_MODE	R/W	0h	Selects which current to use when EN_ADAPTIVE_HDR = 0 0 – ILLUM_DAC_L | 1 – ILLUM_DAC_H
15	EN_ADAPTIVE_HDR	R/W	0h	Enable adaptive HDR to switch between two illumination driver currents (ILLUM_DAC_L and ILLUM_DAC_H) depending on the amplitude of the received signal.
14:3	TX_SEQ_REG	R/W	924h	switching sequence of illumination channels. Up to a sequence of 6 channel configurations. For example, register value: 2-1-0-2-1-0, illumination channel sequence will be 0-1-2-0-1-2
2:1	SEL_TX_CH	R/W	0h	Selects the illumination channel when channel switching is disabled.
0	EN_TX_SWITCH	R/W	0h	Enable switching of illumination channels.

ADVANCE INFORMATION

7.5.1.1.33 Register 2Bh (Address = 2Bh) [reset = 6000h]

Figure 61. Register 2Bh

23	22	21	20	19	18	17	16
0	0	ILLUM_SCALE_H_TX0			ILLUM_SCALE_L_TX0		
R/W - 0h	R/W - 0h	R/W - 0h			R/W - 0h		
15	14	13	12	11	10	9	8
HDR_THR_HIGH							
R/W - 60h							
7	6	5	4	3	2	1	0
HDR_THR_HIGH							
R/W - 00h							

Table 62. Register 2B Field Descriptions

Bit	Field	Type	Reset	Description
23:22	0	R/W	0h	Always read or write 0h.
21:19	ILLUM_SCALE_H_TX0	R/W	0h	Illumination driver current scale register of TX0 Channel with DAC_H current. 0: 5.6 mA | 1: 4.2mA | 2: 2.8 mA | 3: 1.4 mA
18:16	ILLUM_SCALE_L_TX0	R/W	0h	Illumination driver current scale register of TX0 Channel with DAC_L current. 0: 5.6 mA | 1: 4.2mA | 2: 2.8 mA | 3: 1.4 mA
15:0	HDR_THR_HIGH	R/W	6000h	High threshold for the HDR switching. Amplitude is compared against this threshold when the illumination driver current is high (ILLUM_DAC_H) and it will switch to ILLUM_DAC_L if the amplitude exceeds this threshold value.

7.5.1.1.34 Register 2Ch (Address = 2Ch) [reset = 800h]

Figure 62. Register 2Ch

23	22	21	20	19	18	17	16
0	0	ILLUM_SCALE_H_TX1			ILLUM_SCALE_L_TX1		
R/W - 0h	R/W - 0h	R/W - 0h			R/W - 0h		
15	14	13	12	11	10	9	8
HDR_THR_LOW							
R/W - 08h							
7	6	5	4	3	2	1	0
HDR_THR_LOW							
R/W - 00h							

Table 63. Register 2C Field Descriptions

Bit	Field	Type	Reset	Description
23:22	0	R/W	0h	Always read or write 0h.
21:19	ILLUM_SCALE_H_TX0	R/W	0h	Illumination driver current scale register of TX1 Channel with DAC_H current. 0: 5.6 mA | 1: 4.2 mA | 2: 2.8 mA | 3: 1.4 mA
18:16	ILLUM_SCALE_L_TX0	R/W	0h	Illumination driver current scale register of TX1 Channel with DAC_L current. 0: 5.6 mA | 1: 4.2 mA | 2: 2.8 mA | 3: 1.4 mA
15:0	HDR_THR_LOW	R/W	800h	Low threshold for the HDR switching. Amplitude is compared against this threshold when the Illumination driver current is low (ILLUM_DAC_L) and it will switch to ILLUM_DAC_H if the amplitude is lower than this threshold value.

ADVANCE INFORMATION

7.5.1.1.35 Register 2Dh (Address = 2Dh) [reset = 0h]

Figure 63. Register 2Dh

23	22	21	20	19	18	17	16
TEMP_COEFF_MAIN_HDR0_TX1							
15	14	13	12	11	10	9	8
TEMP_COEFF_MAIN_HDR0_TX1				TEMP_COEFF_MAIN_HDR1_TX0			
7	6	5	4	3	2	1	0
TEMP_COEFF_MAIN_HDR1_TX0							

Table 64. Register 2D Field Descriptions

Bit	Field	Type	Reset	Description
23:12]	TEMP_COEFF_MAIN_HDR0_TX1	R/W	0h	Phase temperature coefficient for sensor temperature for TX1 illumination Channel with current of ILLUM_DAC_L_TX1
11:0]	TEMP_COEFF_MAIN_HDR1_TX0	R/W	0h	Phase temperature coefficient for sensor temperature for TX0 illumination Channel with current of ILLUM_DAC_H_TX0

7.5.1.1.36 Register 2Eh (Address = 2Eh) [reset = 8001A0h]

Figure 64. Register 2Eh

23	22	21	20	19	18	17	16
XTALK_FILT_TIME_CONST				ILLUM_XTALK_REG_SCALE			INT_XTALK_REG_SCALE
R/W - 8h				R/W - 0h			R/W - 0h
15	14	13	12	11	10	9	8
INT_XTALK_REG_SCALE		0	ILLUM_XTALK_CALIB	IQ_READ_DATA_SEL			USE_XTALK_REG_ILLUM
R/W - 0h		R/W - 0h	R/W - 0h	R/W - 0h			R/W - 1h
7	6	5	4	3	2	1	0
USE_XTALK_FILT_ILLUM	USE_XTALK_REG_INT	USE_XTALK_FILT_INT	INT_XTALK_CALIB	DIS_AUTO_SCALE	FORCE_SCALE_VAL		
R/W - 1h	R/W - 0h	R/W - 1h	R/W - 0h	R/W - 0h	R/W - 0h		

Table 65. Register 2E Field Descriptions

Bit	Field	Type	Reset	Description
23:20	XTALK_FILT_TIME_CONST	R/W	8h	Time constant for crosstalk filtering. Time constant τ = $2^{XTALK\_FILT\_TIME\_CONST}$ frames. At least 5τ should be allowed for settling of crosstalk measurement
19:17	ILLUM_XTALK_REG_SCALE	R/W	0h	Scale factor illumination crosstalk register (IPHASE_XTALK_REG_HDR<i>_TX<j>, QPHASE_XTALK_REG_HDR<i>_TX<j>, i = 0, 1, j = 0, 1, 2). Scale = $2^{INT\_XTALK\_REG\_SCALE}$
16:14	INT_XTALK_REG_SCALE	R/W	0h	Scale factor internal crosstalk register (IPHASE_XTALK_INT_REG, QPHASE_XTALK_INT_REG). Scale = $2^{INT\_XTALK\_REG\_SCALE}$
13	0	R/W	0h	Always read or write 0.
12	ILLUM_XTALK_CALIB	R/W	0h	The device initializes the Illumination crosstalk measurement upon setting this bit. This measurement should be done with the photodiode masked such that no modulated light is received. Use following sequence: ILLUM_XTALK_CALIB = 1 delay(at least 5*$2^{XTALK\_FILT\_TIME\_CONST}$ frame) ILLUM_XTALK_CALIB = 0
11:9	IQ_READ_DATA_SEL	R/W	0h	Mux selection for IPHASE_XTALK, QPHASE_XTALK registers 000 – Internal Crosstalk | 001 – illumination Crosstalk | 010 – Raw I, Q | 011 - 16-bit frame counter
8	USE_XTALK_REG_ILLUM	R/W	1h	Select register value or internally calibrated value for illumination crosstalk 0 – Calibration value, 1 – Register value

ADVANCE INFORMATION

Table 65. Register 2E Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	USE_XTALK_FILT_ILLUM	R/W	1h	Select filter or direct sampling for Illumination crosstalk measurement. 0 – Direct sampling, 1 – Filter
6	USE_XTALK_REG_INT	R/W	0h	Select register value or internally calibrated value for internal crosstalk 0 – Calibration value, 1 – Register value
5	USE_XTALK_FILT_INT	R/W	1h	Select filter or direct sampling for internal crosstalk measurement. 0 – Direct sampling, 1 – Filter
4	INT_XTALK_CALIB	R/W	0h	The device initializes the internal electrical crosstalk measurement upon setting this bit. Use following sequence: INT_XTALK_CALIB = 1 delay (at least $5 \times 2^{XTALK\_FILT\_TIME\_CONST}$ frames) INT_XTALK_CALIB = 0
3	DIS_AUTO_SCALE	R/W	0h	Disable digital auto scale in the signal path
2:0	FORCE_SCALE_VAL	R/W	0h	Uses this scale value if DIS_AUTO_SCALE = 1. This scale value is also used during any crosstalk calibration even if DIS_AUTO_SCALE is not applied. Scale = $2^{(6-FORCE\_SCALE\_VAL)}$

7.5.1.1.37 Register 2Fh (Address = 2Fh) [reset = 0h]

Figure 65. Register 2Fh

23	22	21	20	19	18	17	16
TEMP_COEFF_MAIN_HDR1_TX1[11:4]							
15	14	13	12	11	10	9	8
IPHASE_XTALK_REG_HDR0_TX0							
7	6	5	4	3	2	1	0
IPHASE_XTALK_REG_HDR0_TX0							

Table 66. Register 2F Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_MAIN_HDR1_TX1[11:4]	R/W	0h	MSB of Phase temperature coefficient for sensor temperature for TX1 illumination Channel with current of ILLUM_DAC_H_TX1
15:0	IPHASE_XTALK_REG_HDR0_TX0	R/W	0h	Register for illumination crosstalk in-phase component for TX0 channel with ILLUM_DAC_L_TX0 current

7.5.1.1.38 Register 30h (Address = 30h) [reset = 0h]

Figure 66. Register 30h

23	22	21	20	19	18	17	16
TEMP_COEFF_MAIN_HDR1_TX1[3:0]				0	0	0	0
15	14	13	12	11	10	9	8
QPHASE_XTALK_REG_HDR0_TX0							
7	6	5	4	3	2	1	0
QPHASE_XTALK_REG_HDR0_TX0							

Table 67. Register 30 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_MAIN_HDR1_TX1[3:0]	R/W	0h	LSB of Phase temperature coefficient for sensor temperature for TX1 illumination Channel with current of ILLUM_DAC_H_TX1
15:0	QPHASE_XTALK_REG_HDR0_TX0	R/W	0h	Quadrature component of the crosstalk for ILLUM_DAC_L of TX0

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7.5.1.1.39 Register 31h (Address = 31h) [reset = 0h]

Figure 67. Register 31h

23	22	21	20	19	18	17	16
TEMP_COEFF_MAIN_HDR0_TX2[11:4]							
15	14	13	12	11	10	9	8
IPHASE_XTALK_REG_HDR1_TX0							
7	6	5	4	3	2	1	0
IPHASE_XTALK_REG_HDR1_TX0							

Table 68. Register 31 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_MAIN_HDR0_TX2[11:4]	R/W	0h	MSB of Phase temperature coefficient for sensor temperature for TX2 illumination Channel with current of ILLUM_DAC_L_TX2
15:0	IPHASE_XTALK_REG_HDR1_TX0	R/W	0h	

7.5.1.1.40 Register 32h (Address = 32h) [reset = 0h]

Figure 68. Register 32h

23	22	21	20	19	18	17	16
TEMP_COEFF_MAIN_HDR0_TX2[3:0]				0	0	0	0
15	14	13	12	11	10	9	8
QPHASE_XTALK_REG_HDR1_TX0							
7	6	5	4	3	2	1	0
QPHASE_XTALK_REG_HDR1_TX0							

Table 69. Register 32 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_MAIN_HDR0_TX2[3:0]	R/W	0h	LSB of Phase temperature coefficient for sensor temperature for TX2 illumination Channel with current of ILLUM_DAC_L_TX2
15:0	QPHASE_XTALK_REG_HDR1_TX0	R/W	0h	Register for illumination crosstalk quad phase component for TX0 channel with ILLUM_DAC_H_TX0 current

7.5.1.1.41 Register 33h (Address = 33h) [reset = 0h]

Figure 69. Register 33h

23	22	21	20	19	18	17	16
TEMP_COEFF_MAIN_HDR1_TX2[11:4]							
15	14	13	12	11	10	9	8
IPHASE_XTALK_REG_HDR0_TX1							
7	6	5	4	3	2	1	0
IPHASE_XTALK_REG_HDR0_TX1							

Table 70. Register 33 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_MAIN_HDR1_TX2[11:4]	R/W	0h	MSB of Phase temperature coefficient for sensor temperature for TX2 illumination Channel with current of ILLUM_DAC_H_TX2
15:0	IPHASE_XTALK_REG_HDR0_TX1	R/W	0h	Register for illumination crosstalk in-phase component for TX1 channel with ILLUM_DAC_L_TX1 current

ADVANCE INFORMATION

7.5.1.1.42 Register 34h (Address = 34h) [reset = 0h]

Figure 70. Register 34h

23	22	21	20	19	18	17	16
TEMP_COEFF_MAIN_HDR1_TX2[3:0]				0	0	0	0
15	14	13	12	11	10	9	8
QPHASE_XTALK_REG_HDR0_TX1							
7	6	5	4	3	2	1	0
QPHASE_XTALK_REG_HDR0_TX1							

Table 71. Register 34 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_MAIN_HDR1_TX2[3:0]	R/W	0h	LSB of Phase temperature coefficient for sensor temperature for TX2 illumination Channel with current of ILLUM_DAC_H_TX2
15:0	QPHASE_XTALK_REG_HDR0_TX1	R/W	0h	Register for illumination crosstalk in quad-phase component for TX1 channel with ILLUM_DAC_L_TX1 current

7.5.1.1.43 Register 35h (Address = 35h) [reset = 0h]

Figure 71. Register 35h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
IPHASE_XTALK_REG_HDR1_TX1							
7	6	5	4	3	2	1	0
IPHASE_XTALK_REG_HDR1_TX1							

Table 72. Register 35 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	IPHASE_XTALK_REG_HDR1_TX1	R/W	0h	Register for illumination crosstalk in-phase component for TX1 channel with ILLUM_DAC_H_TX1 current

7.5.1.1.44 Register 36h (Address = 36h) [reset = 0h]

Figure 72. Register 36h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX0							
15	14	13	12	11	10	9	8
QPHASE_XTALK_REG_HDR1_TX1							
7	6	5	4	3	2	1	0
QPHASE_XTALK_REG_HDR1_TX1							

Table 73. Register 36 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX0	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX0 channel with ILLUM_DAC_L_TX0 current.
15:0	QPHASE_XTALK_REG_HDR1_TX1	R/W	0h	Register for illumination crosstalk quad-phase component for TX1 channel with ILLUM_DAC_H_TX1 current

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7.5.1.1.45 Register 37h (Address = 37h) [reset = 0h]

Figure 73. Register 37h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX0							
15	14	13	12	11	10	9	8
IPHASE_XTALK_REG_HDR0_TX2							
7	6	5	4	3	2	1	0
IPHASE_XTALK_REG_HDR0_TX2							

Table 74. Register 37 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX0	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TILLUM for TX0 channel with ILLUM_DAC_L_TX0 current.
15:0	IPHASE_XTALK_REG_HDR0_TX2	R/W	0h	Register for illumination crosstalk in-phase component for TX2 channel with ILLUM_DAC_L_TX2 current

7.5.1.1.46 Register 38h (Address = 38h) [reset = 0h]

Figure 74. Register 38h

23	22	21	20	19	18	17	16
TEMP_COEFF_XTALK_IPHASE_HDR0_TX0							
15	14	13	12	11	10	9	8
QPHASE_XTALK_REG_HDR0_TX2							
7	6	5	4	3	2	1	0
QPHASE_XTALK_REG_HDR0_TX2							

Table 75. Register 38 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_XTALK_IPHASE_HDR0_TX0	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX0 channel with ILLUM_DAC_L_TX0 current
15:0	QPHASE_XTALK_REG_HDR0_TX2	R/W	0h	Register for illumination crosstalk quad -phase component for TX2 channel with ILLUM_DAC_L_TX2 current

7.5.1.1.47 Register 39h (Address = 39h) [reset = 0h]

Figure 75. Register 39h

23	22	21	20	19	18	17	16
TEMP_COEFF_XTALK_QPHASE_HDR0_TX0							
15	14	13	12	11	10	9	8
IPHASE_XTALK_REG_HDR1_TX2							
7	6	5	4	3	2	1	0
IPHASE_XTALK_REG_HDR1_TX2							

Table 76. Register 39 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_XTALK_QPHASE_HDR0_TX0	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TMAIN for TX0 channel with ILLUM_DAC_L_TX0 current
15:0	IPHASE_XTALK_REG_HDR1_TX2	R/W	0h	Register for illumination crosstalk in-phase component for TX2 channel with ILLUM_DAC_H_TX2 current

ADVANCE INFORMATION

7.5.1.1.48 Register 3Ah (Address = 3Ah) [reset = 0h]

Figure 76. Register 3Ah

23	22	21	20	19	18	17	16
0	SCALE_AMB_XTALK_COEFF			SCALE_TEMP_COEFF_XTALK			EN_TEMP_XTALK_CORR
R/W - 0h	R/W - 4h			R/W - 5h			R/W - 0h
15	14	13	12	11	10	9	8
QPHASE_XTALK_REG_HDR1_TX2							
R/W - 0h							
7	6	5	4	3	2	1	0
QPHASE_XTALK_REG_HDR1_TX2							
R/W - 0h							

Table 77. Register 3A Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Always read or write 0h.
22:20	SCALE_AMB_XTALK_COEFF	R/W	4h	Scaling factor for ambient coefficient of crosstalk (AMB_XTALK_*)
19:17	SCALE_TEMP_COEFF_XTALK	R/W	5h	Scaling factor for temperature coefficient of crosstalk (TEMP_COEFF_XTALK_*PHASE_HDR*_TX*)
16	EN_TEMP_XTALK_CORR	R/W	0h	Enable crosstalk correction with temperature.
15:0	QPHASE_XTALK_REG_HDR1_TX2	R/W	0h	Register for illumination crosstalk quad -phase component for TX2 channel with ILLUM_DAC_H_TX2 current

7.5.1.1.49 Register 3Bh (Address = 3Bh) [reset = 0h]

Figure 77. Register 3Bh

23	22	21	20	19	18	17	16
IPHASE_XTALK							
15	14	13	12	11	10	9	8
IPHASE_XTALK							
7	6	5	4	3	2	1	0
IPHASE_XTALK							

Table 78. Register 3B Field Descriptions

Bit	Field	Type	Reset	Description
23:0	IPHASE_XTALK	R	0h	Read-only register. In-phase component. Different values can be selected to be readout with IQ_READ_DATA_SEL

7.5.1.1.50 Register 3Ch (Address = 3Ch) [reset = 0h]

Figure 78. Register 3Ch

23	22	21	20	19	18	17	16
QPHASE_XTALK							
15	14	13	12	11	10	9	8
QPHASE_XTALK							
7	6	5	4	3	2	1	0
QPHASE_XTALK							

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Table 79. Register 3C Field Descriptions

Bit	Field	Type	Reset	Description
23:0	QPHASE_XTALK	R	0h	Read-only register. Quadrature phase component. Different values can be selected to be readout with IQ_READ_DATA_SEL.

7.5.1.1.51 Register 3Dh (Address = 3Dh) [reset = 0h]

Figure 79. Register 3Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
IPHASE_XTALK_INT_REG							
7	6	5	4	3	2	1	0
IPHASE_XTALK_INT_REG							

Table 80. Register 3D Field Descriptions

Bit	Field	Type	Reset	Description
15:0	IPHASE_XTALK_INT_REG	R/W	0h	Register for in-phase component of internal crosstalk

7.5.1.1.52 Register 3Eh (Address = 3Eh) [reset = 0h]

Figure 80. Register 3Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
QPHASE_XTALK_INT_REG							
7	6	5	4	3	2	1	0
QPHASE_XTALK_INT_REG							

Table 81. Register 3E Field Descriptions

Bit	Field	Type	Reset	Description
15:0	QPHASE_XTALK_INT_REG	R/W	0h	Register for quad-phase component of internal crosstalk

7.5.1.1.53 Register 3Fh (Address = 3Fh) [reset = 0h]

Figure 81. Register 3Fh

23	22	21	20	19	18	17	16
TILLUM_CALIB_HDR0_TX2							
15	14	13	12	11	10	9	8
TILLUM_CALIB_HDR0_TX2				TMAIN_CALIB_HDR0_TX2			
7	6	5	4	3	2	1	0
TMAIN_CALIB_HDR0_TX2							

Table 82. Register 3F Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TILLUM_CALIB_HDR0_TX2	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX2 illumination channel with current of ILLUM_DAC_L_TX2
11:0	TMAIN_CALIB_HDR0_TX2	R/W	0h	Calibration temperature of on chip temperature sensor (TMAIN) for TX2 illumination channel with current of ILLUM_DAC_L_TX2

ADVANCE INFORMATION

7.5.1.1.54 Register 40h (Address = 40h) [reset = 2021E0h]

Figure 82. Register 40h

23	22	21	20	19	18	17	16
0	EN_MULTI_FREQ_PHASE	NCR_CONFIG	BETA0_DEALIAS_SCALE				
R/W - 0h	R/W - 0h	R/W - 1h	R/W - 0h				
15	14	13	12	11	10	9	8
BETA0_DEALIAS_SCALE	ALPHA0_DEALIAS_SCALE						1
R/W - 0h	R/W - 10h						R/W - 1h
7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	EN_DEALIAS_MEAS
R/W - 1h	R/W - 1h	R/W - 1h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

Table 83. Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
22	EN_MULTI_FREQ_PHASE	R/W	0h	With this bit set along with EN_DEALIAS_MEAS = 1, the PHASE_OUT register will give the phase measurement with two frequencies. The frequency of the phase will be indicated in MOD_FREQ status bit.
21	NCR_CONFIG	R/W	1h	Select second frequency for de-alias operation. 0 – 10 × 6 / 7 MHz | or 1 – 10 × 6 / 5 MHz.
20:15	BETA0_DEALIAS_SCALE	R/W	0h	Internal crosstalk scaling for de-alias frequency. β = BETA_DEAL_SCALE / 16.
14:9	ALPHA0_DEALIAS_SCALE	R/W	10h	Internal crosstalk scaling for de-alias frequency. α = ALPHA_DEAL_SCALE / 16.
8:5	15	R/W	Fh	Always read or write Fh.
4:1	0	R/W	0h	Always read or write 0h.
0	EN_DEALIAS_MEAS	R/W	0h	Enables de-alias measurement.

7.5.1.1.55 Register 41h (Address = 41h) [reset = 10h]

Figure 83. Register 41h

23	22	21	20	19	18	17	16
TMAIN_CALIB_HDR1_TX1							
R/W - 0h							
15	14	13	12	11	10	9	8
TMAIN_CALIB_HDR1_TX1				BETA1_DEALIAS_SCALE			
R/W - 0h				R/W - 0h			
7	6	5	4	3	2	1	0
BETA1_DEALIAS_SCALE		ALPHA1_DEALIAS_SCALE					
R/W - 0h		R/W - 10h					

Table 84. Register 41 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TMAIN_CALIB_HDR1_TX1	R/W	0h	Calibration temperature of on chip temperature sensor (TMAIN) for TX1 illumination Channel with current of ILLUM_DAC_H_TX1
11:6	BETA1_DEALIAS_SCALE	R/W	0h	Illumination crosstalk scaling for de-alias frequency. β = BETA_DEAL_SCALE/16
5:0	ALPHA1_DEALIAS_SCALE	R/W	10h	Illumination crosstalk scaling for de-alias frequency. α = ALPHA_DEAL_SCALE/16

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7.5.1.1.56 Register 42h (Address = 42h) [reset = 0h]

Figure 84. Register 42h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PHASE_OFFSET_HDR0_TX0							
7	6	5	4	3	2	1	0
PHASE_OFFSET_HDR0_TX0							

Table 85. Register 42 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	PHASE_OFFSET_HDR0_TX0	R/W	0h	Phase offset for TX0 illumination channel with current of ILLUM_DAC_L_TX0

7.5.1.1.57 Register 43h (Address = 43h) [reset = 81h]

Figure 85. Register 43h

23	22	21	20	19	18	17	16
TILLUM_CALIB_HDR1_TX1							
R/W - 0h							
15	14	13	12	11	10	9	8
TILLUM_CALIB_HDR1_TX1				0	0	0	SCALE_PHASE_TEMP_COEFF
R/W - 0h				R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
SCALE_PHASE_TEMP_COEFF		0	0	0	0	EN_TEMP_CORR	EN_PHASE_CORR
R/W - 2h		R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h

Table 86. Register 43 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TILLUM_CALIB_HDR1_TX1	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
8:6	SCALE_PHASE_TEMP_COEFF	R/W	2h	Adjust scale factor for temperature coefficient.
1	EN_TEMP_CORR	R/W	0h	Enables temperature correction for phase.
0	EN_PHASE_CORR	R/W	1h	Enables phase offset correction.

7.5.1.1.58 Register 44h (Address = 44h) [reset = 0h]

Figure 86. Register 44h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
PHASE2_OFFSET_HDR0_TX0							
7	6	5	4	3	2	1	0
PHASE2_OFFSET_HDR0_TX0							

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Table 87. Register 44 Field Descriptions

Bit	Field	Type	Reset	Description
15:0]	PHASE2_OFFSET_HDR0_TX0	R/W	0h	De-alias frequency phase offset for TX0 Illumination Channel with current of ILLUM_DAC_L_TX0.

7.5.1.1.59 Register 45h (Address = 45h) [reset = 0h]

Figure 87. Register 45h

23	22	21	20	19	18	17	16
TMAIN_CALIB_HDR1_TX2							
15	14	13	12	11	10	9	8
TMAIN_CALIB_HDR1_TX2				TEMP_COEFF_MAIN_HDR0_TX0			
7	6	5	4	3	2	1	0
TEMP_COEFF_MAIN_HDR0_TX0							

Table 88. Register 45 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TMAIN_CALIB_HDR1_TX2	R/W	0h	Calibration temperature of on chip temperature sensor (TMAIN) for TX2 illumination channel with current of ILLUM_DAC_H_TX2
11:0	TEMP_COEFF_MAIN_HDR0_TX0	R/W	0h	Phase temperature coefficient with on chip temperature sensor (TMAIN) for TX0 illumination channel with current of ILLUM_DAC_L_TX0

7.5.1.1.60 Register 46h (Address = 46h) [reset = 0h]

Figure 88. Register 46h

23	22	21	20	19	18	17	16
TILLUM_CALIB_HDR1_TX2							
15	14	13	12	11	10	9	8
TILLUM_CALIB_HDR1_TX2				TEMP_COEFF_ILLUM_HDR0_TX0			
7	6	5	4	3	2	1	0
TEMP_COEFF_ILLUM_HDR0_TX0							

Table 89. Register 46 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TILLUM_CALIB_HDR1_TX2	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX2 illumination channel with current of ILLUM_DAC_H_TX2
11:0	TEMP_COEFF_ILLUM_HDR0_TX0	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX0 illumination channel with current of ILLUM_DAC_L_TX0

7.5.1.1.61 Register 47h (Address = 47h) [reset = 800800h]

Figure 89. Register 47h

23	22	21	20	19	18	17	16
TILLUM_CALIB_HDR0_TX0							
R/W - 80h							
15	14	13	12	11	10	9	8
TILLUM_CALIB_HDR0_TX0				TMAIN_CALIB_HDR0_TX0			
R/W - 0h				R/W - 8h			
7	6	5	4	3	2	1	0
TMAIN_CALIB_HDR0_TX0							
R/W - 0h							

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Table 90. Register 47 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TILLUM_CALIB_HDR0_TX0	R/W	800h	Calibration temperature of external temperature sensor (TILLUM) for TX0 illumination channel with current of ILLUM_DAC_L_TX0
11:0	TMAIN_CALIB_HDR0_TX0	R/W	800h	Calibration temperature of on chip temperature sensor (TMAIN) for TX0 illumination channel with current of ILLUM_DAC_L_TX0

7.5.1.1.62 Register 48h (Address = 48h) [reset = 0h]

Figure 90. Register 48h

23	22	21	20	19	18	17	16
TILLUM_CALIB_HDR1_TX0							
15	14	13	12	11	10	9	8
TILLUM_CALIB_HDR1_TX0				TMAIN_CALIB_HDR1_TX0			
7	6	5	4	3	2	1	0
TMAIN_CALIB_HDR1_TX0							

Table 91. Register 48 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TILLUM_CALIB_HDR1_TX0	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX0 illumination channel with current of ILLUM_DAC_H_TX0
11:0	TMAIN_CALIB_HDR1_TX0	R/W	0h	Calibration temperature of on chip temperature sensor (TMAIN) for TX0 illumination channel with current of ILLUM_DAC_H_TX0

7.5.1.1.63 Register 49h (Address = 49h) [reset = 0h]

Figure 91. Register 49h

23	22	21	20	19	18	17	16
TILLUM_CALIB_HDR0_TX1							
15	14	13	12	11	10	9	8
TILLUM_CALIB_HDR0_TX1				TMAIN_CALIB_HDR0_TX1			
7	6	5	4	3	2	1	0
TMAIN_CALIB_HDR0_TX1							

Table 92. Register 49 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TILLUM_CALIB_HDR0_TX1	R/W	0h	Calibration temperature of external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_L_TX1
11:0	TMAIN_CALIB_HDR0_TX1	R/W	0h	Calibration temperature of on chip temperature sensor (TMAIN) for TX0 illumination channel with current of ILLUM_DAC_L_TX1

7.5.1.1.64 Register 4Ah (Address = 4Ah) [reset = 0h]

Figure 92. Register 4Ah

23	22	21	20	19	18	17	16
0	0	0	0	SCALE_NL_CORR_COEFF		A0_COEFF_HDR0_TX0	
15	14	13	12	11	10	9	8
A0_COEFF_HDR0_TX0							
7	6	5	4	3	2	1	0
A0_COEFF_HDR0_TX0						0	EN_NL_CORR

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Table 93. Register 4A Field Descriptions

Bit	Field	Type	Reset	Description
19:18	SCALE_NL_CORR_COEFF	R/W	0h	Scaling factor for non-linearity correction coefficients (A*_COEFF_HDR*_TX*)
17:2	A0_COEFF_HDR0_TX0	R/W	0h	0th order coefficient for square wave non-linearity correction
0	EN_NL_CORR	R/W	0h	Enables square wave harmonic non-linearity correction

7.5.1.1.65 Register 4Bh (Address = 4Bh) [reset = 407h]

Figure 93. Register 4Bh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
A1_COEFF_HDR0_TX0							
R/W - 04h							
7	6	5	4	3	2	1	0
A1_COEFF_HDR0_TX0							
R/W - 07h							

Table 94. Register 4B Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	A1_COEFF_HDR0_TX0	R/W	407h	1st order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_L_TX0

7.5.1.1.66 Register 4Ch (Address = 4Ch) [reset = F23Eh]

Figure 94. Register 4Ch

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
A2_COEFF_HDR0_TX0							
R/W - F2h							
7	6	5	4	3	2	1	0
A2_COEFF_HDR0_TX0							
R/W - 3Eh							

Table 95. Register 4C Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	A2_COEFF_HDR0_TX0	R/W	F23Eh	Second order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_L_TX0

7.5.1.1.67 Register 4Dh (Address = 4Dh) [reset = 1144h]

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Figure 95. Register 4Dh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
A3_COEFF_HDR0_TX0							
R/W - 11h							
7	6	5	4	3	2	1	0
A3_COEFF_HDR0_TX0							
R/W - 44h							

Table 96. Register 4D Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	A3_COEFF_HDR0_TX0	R/W	1144h	Third order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_L_TX0.

7.5.1.1.68 Register 4Eh (Address = 4Eh) [reset = F881h]

Figure 96. Register 4Eh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
A4_COEFF_HDR0_TX0							
R/W - F8h							
7	6	5	4	3	2	1	0
A4_COEFF_HDR0_TX0							
R/W - 81h							

Table 97. Register 4E Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	A4_COEFF_HDR0_TX0	R/W	F881h	Fourth order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_L_TX0

7.5.1.1.69 Register 50h (Address = 50h) [reset = 200100h]

Figure 97. Register 50h

23	22	21	20	19	18	17	16
0	OVERRIDE_CLKGEN_REG	1	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 1h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	1
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h
7	6	5	4	3	2	1	0
0	0	0	0	CLIP_MODE_OFFSET	CLIP_MODE_TEMP	CLIP_MODE_NL	CLIP_MODE_FC
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

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Table 98. Register 50 Field Descriptions

Bit	Field	Type	Reset	Description
23	0	R/W	0h	Always read or write 0h.
22	OVERRIDE_CLKGEN_REG	R/W	0h	Setting this register 1 allows user to independently control DEALIAS_FREQ, DEALIAS_EN.
21	1	R/W	1h	Always read or write 1h.
20:9	0	R/W	0h	Always read or write 0h.
8	1	R/W	1h	Always read or write 1h.
7:4	0	R/W	0h	Always read or write 0h.
3	CLIP_MODE_OFFSET	R/W	0h	Chooses either clipping or wrap around when applying offset correction for phase. 0 – wrap around | 1 – Clip
2	CLIP_MODE_TEMP	R/W	0h	Chooses either clipping or wrap around when applying temp correction for phase. 0 – wrap around | 1 – Clip
1	CLIP_MODE_NL	R/W	0h	Chooses either clipping or wrap around when applying non-linearity correction for phase. 0 – wrap around | 1 – Clip
0	CLIP_MODE_FC	R/W	0h	Chooses clipping or wrap around when applying freq-correction for phase. 0 – wrap around | 1 – Clip

7.5.1.1.70 Register 51h (Address = 51h) [reset = 0h]

Figure 98. Register 51h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR1_TX0[11:4]							
15	14	13	12	11	10	9	8
PHASE_OFFSET_HDR1_TX0							
7	6	5	4	3	2	1	0
PHASE_OFFSET_HDR1_TX0							

Table 99. Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_HDR1_TX0[11:4]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX0 illumination channel with current of ILLUM_DAC_H_TX0
15:0	PHASE_OFFSET_HDR1_TX0	R/W	0h	Phase offset for TX0 illumination channel with current of ILLUM_DAC_H_TX0

7.5.1.1.71 Register 52h (Address = 52h) [reset = 0h]

Figure 99. Register 52h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR1_TX0[3:0]				0	0	0	0
15	14	13	12	11	10	9	8
PHASE_OFFSET_HDR0_TX1							
7	6	5	4	3	2	1	0
PHASE_OFFSET_HDR0_TX1							

Table 100. Register 52 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_ILLUM_HDR1_TX0[3:0]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX0 illumination channel with current of ILLUM_DAC_H_TX0
15:0	PHASE_OFFSET_HDR0_TX1	R/W	0h	Phase offset for TX1 illumination channel with current of ILLUM_DAC_L_TX1

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7.5.1.1.72 Register 53h (Address = 53h) [reset = 0h]

Figure 100. Register 53h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR0_TX1[11:4]							
15	14	13	12	11	10	9	8
PHASE_OFFSET_HDR1_TX1							
7	6	5	4	3	2	1	0
PHASE_OFFSET_HDR1_TX1							

Table 101. Register 53 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_HDR0_TX1[11:4]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_L_TX1
15:0	PHASE_OFFSET_HDR1_TX1	R/W	0h	Phase offset for TX1 illumination channel with current of ILLUM_DAC_H_TX1

7.5.1.1.73 Register 54h (Address = 54h) [reset = 0h]

Figure 101. Register 54h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR0_TX1[3:0]				0	0	0	0
15	14	13	12	11	10	9	8
PHASE_OFFSET_HDR0_TX2							
7	6	5	4	3	2	1	0
PHASE_OFFSET_HDR0_TX2							

Table 102. Register 54 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_ILLUM_HDR0_TX1[3:0]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_L_TX1
15:0	PHASE_OFFSET_HDR0_TX2	R/W	0h	Phase offset for TX2 illumination channel with current of ILLUM_DAC_L_TX2

7.5.1.1.74 Register 55h (Address = 55h) [reset = 0h]

Figure 102. Register 55h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR1_TX1[11:4]							
15	14	13	12	11	10	9	8
PHASE_OFFSET_HDR1_TX2							
7	6	5	4	3	2	1	0
PHASE_OFFSET_HDR1_TX2							

Table 103. Register 55 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_HDR1_TX1[11:4]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_H_TX1
15:0	PHASE_OFFSET_HDR1_TX2	R/W	0h	Phase offset for TX2 illumination channel with current of ILLUM_DAC_H_TX2

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7.5.1.1.75 Register 56h (Address = 56h) [reset = 0h]

Figure 103. Register 56h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR1_TX1[3:0]				0	0	0	0
15	14	13	12	11	10	9	8
PHASE2_OFFSET_HDR1_TX0							
7	6	5	4	3	2	1	0
PHASE2_OFFSET_HDR1_TX0							

Table 104. Register 56 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_ILLUM_HDR1_TX1[3:0]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_H_TX1
15:0	PHASE2_OFFSET_HDR1_TX0	R/W	0h	De-alias frequency phase offset for TX0 illumination channel with current of ILLUM_DAC_H_TX0

7.5.1.1.76 Register 57h (Address = 57h) [reset = 0h]

Figure 104. Register 57h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR0_TX2[11:4]							
15	14	13	12	11	10	9	8
PHASE2_OFFSET_HDR0_TX1							
7	6	5	4	3	2	1	0
PHASE2_OFFSET_HDR0_TX1							

Table 105. Register 57 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_HDR0_TX2[11:4]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_L_TX2
15:0	PHASE2_OFFSET_HDR0_TX1	R/W	0h	De-alias frequency phase offset for TX1 illumination channel with current of ILLUM_DAC_L_TX1

7.5.1.1.77 Register 58h (Address = 58h) [reset = 0h]

Figure 105. Register 58h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR0_TX2[3:0]				0	0	0	0
15	14	13	12	11	10	9	8
PHASE2_OFFSET_HDR1_TX1							
7	6	5	4	3	2	1	0
PHASE2_OFFSET_HDR1_TX1							

Table 106. Register 58 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_ILLUM_HDR0_TX2[3:0]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_L_TX2
15:0	PHASE2_OFFSET_HDR1_TX1	R/W	0h	De-alias frequency phase offset for TX1 illumination channel with current of ILLUM_DAC_H_TX1

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7.5.1.1.78 Register 59h (Address = 59h) [reset = 0h]

Figure 106. Register 59h

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR1_TX2[11:4]							
15	14	13	12	11	10	9	8
PHASE2_OFFSET_HDR0_TX2							
7	6	5	4	3	2	1	0
PHASE2_OFFSET_HDR0_TX2							

Table 107. Register 59 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_HDR1_TX2[11:4]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_H_TX2
15:0	PHASE2_OFFSET_HDR0_TX2	R/W	0h	De-alias frequency phase offset for TX2 illumination channel with current of ILLUM_DAC_L_TX2

7.5.1.1.79 Register 5Ah (Address = 5Ah) [reset = 0h]

Figure 107. Register 5Ah

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_HDR1_TX2[3:0]				0	0	0	0
15	14	13	12	11	10	9	8
PHASE2_OFFSET_HDR1_TX2							
7	6	5	4	3	2	1	0
PHASE2_OFFSET_HDR1_TX2							

Table 108. Register 5A Field Descriptions

Bit	Field	Type	Reset	Description
23:20	TEMP_COEFF_ILLUM_HDR1_TX2[3:0]	R/W	0h	Phase temperature coefficient with external temperature sensor (TILLUM) for TX1 illumination channel with current of ILLUM_DAC_H_TX2
15:0	PHASE2_OFFSET_HDR1_TX2	R/W	0h	De-alias frequency phase offset for TX2 illumination channel with current of ILLUM_DAC_H_TX2

7.5.1.1.80 Register 5Bh (Address = 5Bh) [reset = 0h]

Figure 108. Register 5Bh

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX1							
15	14	13	12	11	10	9	8
TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX1							
7	6	5	4	3	2	1	0
TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX0							

Table 109. Register 5B Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX1	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX1 channel with ILLUM_DAC_H_TX1 current.
15:8	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX1	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX1 channel with ILLUM_DAC_L_TX1 current.
7:0	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX0	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX0 channel with ILLUM_DAC_H_TX0 current.

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7.5.1.1.81 Register 5Ch (Address = 5Ch) [reset = 0h]

Figure 109. Register 5Ch

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX0							
15	14	13	12	11	10	9	8
TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX2							
7	6	5	4	3	2	1	0
TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX2							

Table 110. Register 5C Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX0	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TILLUM for TX0 channel with ILLUM_DAC_H_TX0 current.
15:8	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR1_TX2	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX2 channel with ILLUM_DAC_H_TX2 current.
7:0	TEMP_COEFF_ILLUM_XTALK_IPHASE_HDR0_TX2	R/W	0h	Temperature coefficient of crosstalk in-phase component with TILLUM for TX2 channel with ILLUM_DAC_H_TX2 current.

7.5.1.1.82 Register 5Dh (Address = 5Dh) [reset = 0h]

Figure 110. Register 5Dh

23	22	21	20	19	18	17	16
TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX2							
15	14	13	12	11	10	9	8
TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX1							
7	6	5	4	3	2	1	0
TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX1							

Table 111. Register 5D Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX2	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TILLUM for TX2 channel with ILLUM_DAC_L_TX2 current.
15:8	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX1	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TILLUM for TX1 channel with ILLUM_DAC_H_TX1 current.
7:0	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR0_TX1	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TILLUM for TX1 channel with ILLUM_DAC_L_TX1 current.

7.5.1.1.83 Register 5Eh (Address = 5Eh) [reset = 0h]

Figure 111. Register 5Eh

23	22	21	20	19	18	17	16
TEMP_COEFF_XTALK_IPHASE_HDR0_TX1							
15	14	13	12	11	10	9	8
TEMP_COEFF_XTALK_IPHASE_HDR1_TX0							
7	6	5	4	3	2	1	0
TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX2							

Table 112. Register 5E Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_XTALK_IPHASE_HDR0_TX1	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX1 channel with ILLUM_DAC_L_TX1 current

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Table 112. Register 5E Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15:8	TEMP_COEFF_XTALK_IPHASE_HDR1_TX0	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX0 channel with ILLUM_DAC_H_TX0 current
7:0	TEMP_COEFF_ILLUM_XTALK_QPHASE_HDR1_TX2	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TILLUM for TX2 channel with ILLUM_DAC_H_TX2 current.

7.5.1.1.84 Register 5Fh (Address = 5Fh) [reset = 0h]

Figure 112. Register 5Fh

23	22	21	20	19	18	17	16
TEMP_COEFF_XTALK_IPHASE_HDR1_TX2							
15	14	13	12	11	10	9	8
TEMP_COEFF_XTALK_IPHASE_HDR0_TX2							
7	6	5	4	3	2	1	0
TEMP_COEFF_XTALK_IPHASE_HDR1_TX1							

Table 113. Register 5F Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_XTALK_IPHASE_HDR1_TX2	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX2 channel with ILLUM_DAC_H_TX2 current
15:8	TEMP_COEFF_XTALK_IPHASE_HDR0_TX2	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX2 channel with ILLUM_DAC_L_TX2 current
7:0	TEMP_COEFF_XTALK_IPHASE_HDR1_TX1	R/W	0h	Temperature coefficient of crosstalk in-phase component with TMAIN for TX1 channel with ILLUM_DAC_H_TX1 current

7.5.1.1.85 Register 60h (Address = 60h) [reset = 0h]

Figure 113. Register 60h

23	22	21	20	19	18	17	16
TEMP_COEFF_XTALK_QPHASE_HDR1_TX1							
15	14	13	12	11	10	9	8
TEMP_COEFF_XTALK_QPHASE_HDR0_TX1							
7	6	5	4	3	2	1	0
TEMP_COEFF_XTALK_QPHASE_HDR1_TX0							

Table 114. Register 60 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	TEMP_COEFF_XTALK_QPHASE_HDR1_TX1	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TMAIN for TX1 channel with ILLUM_DAC_H_TX1 current
15:8	TEMP_COEFF_XTALK_QPHASE_HDR0_TX1	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TMAIN for TX1 channel with ILLUM_DAC_L_TX1 current
7:0	TEMP_COEFF_XTALK_QPHASE_HDR1_TX0	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TMAIN for TX0 channel with ILLUM_DAC_H_TX0 current

7.5.1.1.86 Register 61h (Address = 61h) [reset = 0h]

Figure 114. Register 61h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
TEMP_COEFF_XTALK_QPHASE_HDR1_TX2							
7	6	5	4	3	2	1	0

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TEMP_COEFF_XTALK_QPHASE_HDR0_TX2

Table 115. Register 61 Field Descriptions

Bit	Field	Type	Reset	Description
15:8	TEMP_COEFF_XTALK_QPHASE_HDR1_TX2	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TMAIN for TX2 channel with ILLUM_DAC_H_TX2 current
7:0	TEMP_COEFF_XTALK_QPHASE_HDR0_TX2	R/W	0h	Temperature coefficient of crosstalk quad-phase component with TMAIN for TX2 channel with ILLUM_DAC_L_TX2 current

7.5.1.1.87 Register 64h (Address = 64h) [reset = 280C00h]

Figure 115. Register 64h

23	22	21	20	19	18	17	16
PROG_OVLDET_REFM			PROG_OVLDET_REFP			0	0
R/W - 1h			R/W - 2h			R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
0	0	0	0	1	1	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h	R/W - 1h	R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

Table 116. Register 64 Field Descriptions

Bit	Field	Type	Reset	Description
23:21	PROG_OVLDET_REFM	R/W	1h	Program overload comparator threshold 0: default | 1: +100 mV | 2: +200 mV
20:18	PROG_OVLDET_REFP	R/W	2h	Program overload comparator threshold 0: default | 2: -100 mV
17:16	0	R/W	0h	Always read or write 0h.
15:8	12	R/W	0Ch	Always read or write 0Ch.
7:0	0	R/W	0h	Always read or write 0h.

7.5.1.1.88 Register 65h (Address = 65h) [reset = 0h]

Figure 116. Register 65h

23	22	21	20	19	18	17	16
DIS_OVLDET	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Table 117. Register 65 Field Descriptions

Bit	Field	Type	Reset	Description
23	DIS_OVLDET	R/W	0h	Disables AFE overload detection.
22:0	0	R/W	0h	Always read or write 0h.

7.5.1.1.89 Register 6Eh (Address = 6Eh) [reset = 20000h]

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Figure 117. Register 6Eh

23	22	21	20	19	18	17	16
0	0	0	0	EN_TEMP_CONV	0	1	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h	R/W - 0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

Table 118. Register 6E Field Descriptions

Bit	Field	Type	Reset	Description
19	EN_TEMP_CONV	R/W	0h	Enable temperature sensor conversion
17	1	R/W	1h	Always read or write 1h

7.5.1.1.90 Register 71h (Address = 71h) [reset = 0h]

Figure 118. Register 71h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	UNMASK_ILLUMEN_INTXTALK	EN_ILLUM_CLK_GPIO
15	14	13	12	11	10	9	8
ILLUM_CLK_GPIO_MODE	0	0	DIS_ILLUM_CLK_TX	INVERT_AFE_CLK	0	INVERT_TG_CLK	SHUT_CLOCKS
7	6	5	4	3	2	1	0
0	SHIFT_ILLUM_PHASE				DEALIAS_FREQ	DEALIAS_EN	0

Table 119. Register 71 Field Descriptions

Bit	Field	Type	Reset	Description
17	UNMASK_ILLUMEN_INTXTALK	R/W	0h	Mask/unmask ILLUM_EN_TX0 going to GPIO with internal crosstalk signal 0: ILLUM_EN_TX0 is masked with internal crosstalk correction signal | 1: ILLUM_EN_TX0 is not masked with internal crosstalk correction signal
16	EN_ILLUM_CLK_GPIO	R/W	0h	Enable ILLUM CLK going to GPIO
15	ILLUM_CLK_GPIO_MODE	R/W	0h	Disable ILLUM_EN_TX0 gating ILLUM_CLK going to GPIO. 0: ILLUM_CLK will come on GPIO only when ILLUM_EN high | 1 ILLUM_CLK alive always
12	DIS_ILLUM_CLK_TX	R/W	0h	Disable ILLUM_CLK going to transmitter
11	INVERT_AFE_CLK	R/W	0h	Invert CLK input to AFE
9	INVERT_TG_CLK	R/W	0h	Invert CLK input to timing generation unit.
8	SHUT_CLOCKS	R/W	0h	Shut down all CLK signals at modulation frequency.
6:3	SHIFT_ILLUM_PHASE	R/W	0h	Shift the phase of ILLUM_CLK. PHASE = SHIFT_ILLUM_PHASE × 22.5 deg
2	DEALIAS_FREQ	R/W	0h	Select modulation freq when DEALIAS_EN = 1. This register will work only when OVERRIDE_CLKGEN_REG = 1 0: 10 × 6 / 7 MHz | 1: 10 × 6 / 5 MHz
1	DEALIAS_EN	R/W	0h	Change the modulation frequency. This register will work only when OVERRIDE_CLKGEN_REG = 1

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7.5.1.1.91 Register 72h (Address = 72h) [reset = C0h]

Figure 119. Register 72h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
7	6	5	4	3	2	1	0
IAMB_MAX_SEL				0	0	0	0
R/W - Ch				R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h

Table 120. Register 72 Field Descriptions

Bit	Field	Type	Reset	Description
23:8	0	R/W	0h	Always read or write 0h.
7:4	IAMB_MAX_SEL	R/W	Ch	selects the value of ambient cancellation DAC resistor 0: 20 µA | 5: 10 µA | 10: 33 µA | 11: 50 µA | 12: 100 µA | 14: 200 µA
3:0	0	R/W	0h	Always read or write 0h.

7.5.1.1.92 Register 76h (Address = 76h) [reset = 0h]

Figure 120. Register 76h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	PDN_GLOBAL	0	DIS_GLB_PD_I2CHOST	DIS_GLB_PD_OSC
7	6	5	4	3	2	1	0
0	DIS_GLB_PD_AMB_ADC	DIS_GLB_PD_AMB_DAC	DIS_GLB_PD_AFE_DAC	DIS_GLB_PD_AFE	DIS_GLB_PD_ILLUM_DRV	DIS_GLB_PD_TEMP_SENS	DIS_GLB_PD_REFSYS

Table 121. Register 76 Field Descriptions

Bit	Field	Type	Reset	Description
11	PDN_GLOBAL	R/W	0h	Global power down of all the blocks.
9	DIS_GLB_PD_I2CHOST	R/W	0h	Disable global power down of I2C Host.
8	DIS_GLB_PD_OSC	R/W	0h	Disable global power down of main oscillator.
7	DIS_GLB_PD_TEST_CURR	R/W	0h	Disable global power down of test current source.
6	DIS_GLB_PD_AMB_ADC	R/W	0h	Disable global power down of ambient ADC.
5	DIS_GLB_PD_AMB_DAC	R/W	0h	Disable global power down of ambient cancellation.
4	DIS_GLB_PD_AFE_DAC	R/W	0h	Disable global power down of AFE DAC.
3	DIS_GLB_PD_AFE	R/W	0h	Disable global power down of AFE.
2	DIS_GLB_PD_ILLUM_DRV	R/W	0h	Disable global power down of illumination driver.
1	DIS_GLB_PD_TEMP_SENS	R/W	0h	Disable global power down of temperature sensor.
0	DIS_GLB_PD_REFSYS	R/W	0h	Disable global power down of reference.

7.5.1.1.93 Register 77h (Address = 77h) [reset = 0h]

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Figure 121. Register 77h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	EN_DYN_PD_I2CHOST_OSC	EN_DYN_PD_OSC
7	6	5	4	3	2	1	0
EN_DYN_PD_TEST_CURR	EN_DYN_PD_AMB_ADC	EN_DYN_PD_AMB_DAC	EN_DYN_PD_AFE_DAC	EN_DYN_PD_AFE	EN_DYN_PD_LED_DRV	EN_DYN_PD_TEMP_SENS	EN_DYN_PD_REFSYS

Table 122. Register 77 Field Descriptions

Bit	Field	Type	Reset	Description
9	EN_DYN_PD_I2CHOST_OSC	R/W	0h	Enable dynamic power down of I^2C host oscillator.
8	EN_DYN_PD_OSC	R/W	0h	Enable dynamic power down of main oscillator.
7	EN_DYN_PD_TEST_CURR	R/W	0h	Enable dynamic power down of test current source.
6	EN_DYN_PD_AMB_ADC	R/W	0h	Enable dynamic power down of ambient ADC.
5	EN_DYN_PD_AMB_DAC	R/W	0h	Enable dynamic power down of ambient cancellation.
4	EN_DYN_PD_AFE_DAC	R/W	0h	Enable dynamic power down of AFE DAC.
3	EN_DYN_PD_AFE	R/W	0h	Enable dynamic power down of AFE.
2	EN_DYN_PD_LED_DRV	R/W	0h	Enable dynamic power down of illumination driver.
1	EN_DYN_PD_TEMP_SENS	R/W	0h	Enable dynamic power down of temperature sensor.
0	EN_DYN_PD_REFSYS	R/W	0h	Enable dynamic power down of reference.

7.5.1.1.94 Register 78h (Address = 78h) [reset = 0h]

Figure 122. Register 78h

23	22	21	20	19	18	17	16
0	SEL_GP3_ON_SDAM	0	0	0	0	0	GPIO2_IBUF_EN
15	14	13	12	11	10	9	8
GPIO2_OBUF_EN	0	0	GPIO1_OBUF_EN	GPO2_MUX_SEL			GPO1_MUX_SEL
7	6	5	4	3	2	1	0
GPO1_MUX_SEL		0	0	0	GPO3_MUX_SEL		

Table 123. Register 78 Field Descriptions

Bit	Field	Type	Reset	Description
22	SEL_GP3_ON_SDAM	R/W	0h	Select GP3 on SDA_M pin. This feature can be used when I^2C host is not used in the system. Pull up need to be present on SDA_M pin. To save power the signal on this pin are inverted (active low).
16	GPIO2_IBUF_EN	R/W	0h	Enable input buffer on GP2 pin. Used for reference CLK input.
15	GPIO2_OBUF_EN	R/W	0h	Enable output buffer on GP2 pin.
12	GPIO1_OBUF_EN	R/W	0h	Enable output buffer on GP1 pin.
11:9	GPO2_MUX_SEL	R/W	0h	0 – DVSS | 2 – DIG_GPO_0 | 3 – DIG_GPO_1 | 7 – ILLUM_EN_TX0
8:6	GPO1_MUX_SEL	R/W	0h	0 – DVSS | 2 — DIG_GPO_0 | 3 — DIG_GPO_1 | 7 — ILLUM_CLK
2:0	GPO3_MUX_SEL	R/W	0h	0 – DVSS | 2 — DIG_GPO_0 | 3 — DIG_GPO_1 | 7 — DIG_GPO_2

7.5.1.1.95 Register 79h (Address = 79h) [reset = 1h]

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Figure 123. Register 79h

23	22	21	20	19	18	17	16
0	0	0	0	PDN_ILLUM_DRV	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
0	0	0	PDN_ILLUM_DC_CURR	ILLUM_DC_CURR_DAC			
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h			
7	6	5	4	3	2	1	0
0	0	0	EN_TX_DC_CURR_ALL	SEL_ILLUM_TX0_ON_TX1	EN_TX_CLKZ	0	EN_TX_CLKB
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 1h

Table 124. Register 79 Field Descriptions

Bit	Field	Type	Reset	Description
23:20	0	R/W	0h	Always read or write 0.
19	PDN_ILLUM_DRV	R/W	0h	Test Mode bit to power down illumination Driver
18:14	0	R/W	0h	Always read or write 0.
12	PDN_ILLUM_DC_CURR	R/W	0h	Power down DC bias current through TX pins.
11:8	ILLUM_DC_CURR_DAC	R/W	0h	DC current through TX pin = 0.5mA*ILLUM_DC_CURR_DAC
7:5	0	R/W	0h	Always read or write 0.
4	EN_TX_DC_CURR_ALL	R/W	0h	Enable DC current of all TX channels when TX0 is selected.
3	SEL_ILLUM_TX0_ON_TX1	R/W	0h	Use ILLUM_EN_TX0 for TX1. This mode is required to enable static current drive mode.
2	EN_TX_CLKZ	R/W	0h	Enable inverted modulation CLK.
0	EN_TX_CLKB	R/W	1h	Enable modulation CLK.

7.5.1.1.96 Register 7Ah (Address = 7Ah) [reset = 0h]

Figure 124. Register 7Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	TX0_PIN_CONFIG		TX2_PIN_CONFIG		TX1_PIN_CONFIG	

Table 125. Register 7A Field Descriptions

Bit	Field	Type	Reset	Description
5:4	TX0_PIN_CONFIG	R/W	0h	Configure TX0 pin. 0: CLKB | 2: CLKZ | 3: 1
3:2	TX2_PIN_CONFIG	R/W	0h	Configure TX2 pin. 0: CLKB | 2: CLKZ | 3: 1
1:0	TX1_PIN_CONFIG	R/W	0h	Configure TX1 pin. 0: CLKB | 2: CLKZ | 3: 1

7.5.1.1.97 Register 80h (Address = 80h) [reset = 4E1Eh]

Figure 125. Register 80h

23	22	21	20	19	18	17	16
DIS_TG_ACONF	0	0	0	0	0	0	SUB_VD_CLK_CNT
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
SUB_VD_CLK_CNT							

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R/W - 4Eh							
7	6	5	4	3	2	1	0
SUB_VD_CLK_CNT							TG_EN
R/W - 0Fh							R/W - 0h

Table 126. Register 80 Field Descriptions

Bit	Field	Type	Reset	Description
23	DIS_TG_ACONF	R/W	0h	Disable automatic configuration of TG registers (TG_CAPTURE_MASK*, TG_OVL_WINDOW_MSAK*, TG_ILLUMEN_MASK*, TG_CALC_MASK*, TG_DYNPDN_MASK*, and more) if these signals need to be configured by user this bit may be used as an override.
22:17	0	R/W	0h	Always read or write 0h.
16:1	SUB_VD_CLK_CNT	R/W	270Fh	The number of TG CLKs in a sub-frame.
0	TG_EN	R/W	0h	Enable the timing generation unit.

7.5.1.1.98 Register 83h (Address = 83h) [reset = D0h]

Figure 126. Register 83h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_AFE_RST_START							
R/W - 00h							
7	6	5	4	3	2	1	0
TG_AFE_RST_START							
R/W - D0h							

Table 127. Register 83 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_AFE_RST_START	R/W	D0h	AFE reset TG signal start position (number of TG CLKs) in a sub frame

7.5.1.1.99 Register 84h (Address = 84h) [reset = D8h]

Figure 127. Register 84h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_AFE_RST_END							
R/W - 00h							
7	6	5	4	3	2	1	0
TG_AFE_RST_END							
R/W - D8h							

Table 128. Register 84 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_AFE_RST_END	R/W	D8h	AFE reset TG signal end position (number of TG CLKs) in a sub frame

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7.5.1.1.100 Register 85h (Address = 85h) [reset = 20h]

Figure 128. Register 85h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_SEQ_INT_START							
R/W - 00h							
7	6	5	4	3	2	1	0
TG_SEQ_INT_START							
R/W - 20h							

Table 129. Register 85 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_SEQ_INT_START	R/W	20h	Sequencer interrupt TG signal start position (number of TG CLKs) in a sub frame

7.5.1.1.101 Register 86h (Address = 86h) [reset = 28h]

Figure 129. Register 86h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_SEQ_INT_END							
R/W - 00h							
7	6	5	4	3	2	1	0
TG_SEQ_INT_END							
R/W - 28h							

Table 130. Register 86 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_SEQ_INT_END	R/W	28h	Sequencer interrupt TG signal end position (number of TG CLKs) in a sub frame

7.5.1.1.102 Register 87h (Address = 87h) [reset = 2454h]

Figure 130. Register 87h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_CAPTURE_START							
R/W - 24h							
7	6	5	4	3	2	1	0
TG_CAPTURE_START							
R/W - 54h							

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Table 131. Register 87 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_CAPTURE_START	R/W	2454h	Internal data capture TG signal start position (number of TG CLKs) in a sub frame

7.5.1.1.103 Register 88h (Address = 88h) [reset = 2648h]

Figure 131. Register 88h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_CAPTURE_END							
R/W - 26h							
7	6	5	4	3	2	1	0
TG_CAPTURE_END							
R/W - 48h							

Table 132. Register 88 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_CAPTURE_END	R/W	2648h	Internal data capture TG signal end position (number of TG CLKs) in a sub frame

7.5.1.1.104 Register 89h (Address = 89h) [reset = 3E8h]

Figure 132. Register 89h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_OVL_WINDOW_START							
R/W - 03h							
7	6	5	4	3	2	1	0
TG_OVL_WINDOW_START							
R/W - E8h							

Table 133. Register 89 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_OVL_WINDOW_START	R/W	3E8h	AFE overload observation window TG signal start position (number of TG CLKs) in a sub frame

7.5.1.1.105 Register 8Ah (Address = 8Ah) [reset = 1F40h]

Figure 133. Register 8Ah

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8

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TG_OVL_WINDOW_END							
R/W - 1Fh							
7	6	5	4	3	2	1	0
TG_OVL_WINDOW_END							
R/W - 40h							

Table 134. Register 8A Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_OVL_WINDOW_END	R/W	1F40h	AFE overload observation window TG signal end position (number of TG CLKs) in a sub frame

7.5.1.1.106 Register 8Fh (Address = 8Fh) [reset = 0h]

Figure 134. Register 8Fh

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
TG_ILLUMEN_START							
7	6	5	4	3	2	1	0
TG_ILLUMEN_START							

Table 135. Register 8F Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_ILLUMEN_START	R/W	0h	Illumination enable TG signal start position (number of TG CLKs) in a sub frame

7.5.1.1.107 Register 90h (Address = 90h) [reset = 2134h]

Figure 135. Register 90h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_ILLUMEN_END							
R/W - 21h							
7	6	5	4	3	2	1	0
TG_ILLUMEN_END							
R/W - 34h							

Table 136. Register 90 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_ILLUMEN_END	R/W	2134h	Illumination enable TG signal end position (number of TG CLKs) in a sub frame

7.5.1.1.108 Register 91h (Address = 91h) [reset = 2134h]

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Figure 136. Register 91h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_CALC_START							
R/W - 21h							
7	6	5	4	3	2	1	0
TG_CALC_START							
R/W - 34h							

Table 137. Register 91 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_CALC_START	R/W	2134h	Calculation TG signal start position (number of TG CLKs) in a sub frame

7.5.1.1.109 Register 92h (Address = 92h) [reset = 2EE0h]

Figure 137. Register 92h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_CALC_END							
R/W - 2Eh							
7	6	5	4	3	2	1	0
TG_CALC_END							
R/W - E0h							

Table 138. Register 92 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_CALC_END	R/W	2EE0h	Calculation TG signal end position (number of TG CLKs) in a sub frame

7.5.1.1.110 Register 93h (Address = 93h) [reset = 0h]

Figure 138. Register 93h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
TG_DYNPDN_START							
7	6	5	4	3	2	1	0
TG_DYNPDN_START							

Table 139. Register 93 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_DYNPDN_START	R/W	0h	Dynamic power down TG signal start position (number of TG CLKs) in a sub frame

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7.5.1.1.111 Register 94h (Address = 94h) [reset = FFFFh]

Figure 139. Register 94h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
TG_DYNPDN_END							
R/W - FFh							
7	6	5	4	3	2	1	0
TG_DYNPDN_END							
R/W - FFh							

Table 140. Register 94 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h.
15:0	TG_DYNPDN_END	R/W	FFFFh	Dynamic power down TG signal end position (number of TG CLKs) in a sub frame

7.5.1.1.112 Register 97h (Address = 97h) [reset = 0h]

Figure 140. Register 97h

23	22	21	20	19	18	17	16
TG_SEQ_INT_MASK_END							
15	14	13	12	11	10	9	8
TG_SEQ_INT_MASK_END				TG_SEQ_INT_MASK_START			
7	6	5	4	3	2	1	0
TG_SEQ_INT_MASK_START							

Table 141. Register 97 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TG_SEQ_INT_MASK_END	R/W	0h	Sequencer interrupt TG signal mask end position (number of sub-frame) in frame.
11:0	TG_SEQ_INT_MASK_START	R/W	0h	Sequencer interrupt TG signal mask start position (number of sub-frame) in frame. TG signal will exist between START and END sub-frames.

7.5.1.1.113 Register 98h (Address = 98h) [reset = 0h]

Figure 141. Register 98h

23	22	21	20	19	18	17	16
TG_CAPTURE_MASK_END							
15	14	13	12	11	10	9	8
TG_CAPTURE_MASK_END				TG_CAPTURE_MASK_START			
7	6	5	4	3	2	1	0
TG_CAPTURE_MASK_START							

Table 142. Register 98 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TG_CAPTURE_MASK_END	R/W	0h	Internal data capture TG signal mask end position (number of sub-frame) in frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.

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Table 142. Register 98 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	TG_CAPTURE_MASK_START	R/W	0h	Internal data capture TG signal mask start position (number of sub-frame) in frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1. TG signal will exist between START and END sub-frames.

7.5.1.1.114 Register 99h (Address = 99h) [reset = 1h]

Figure 142. Register 99h

23	22	21	20	19	18	17	16
TG_OVL_WINDOW_MASK_END							
15	14	13	12	11	10	9	8
TG_OVL_WINDOW_MASK_END				TG_OVL_WINDOW_MASK_START			
7	6	5	4	3	2	1	0
TG_OVL_WINDOW_MASK_START							

Table 143. Register 99 Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TG_OVL_WINDOW_MASK_END	R/W	0h	AFE overload observation window TG signal mask end position (number of sub-frame) in frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.
11:0	TG_OVL_WINDOW_MASK_START	R/W	1h	AFE overload observation window TG signal mask start position (number of sub-frame) in frame.TG signal will exist between START and END sub-frames. Write this register 0 when DIS_TG_ACONF=1 and EN_ADAPTIVE_HDR = 0 or 1 when DIS_TG_ACONF = 1 and EN_ADAPTIVE_HDR = 1.

7.5.1.1.115 Register 9Ch (Address = 9Ch) [reset = FFF000h]

Figure 143. Register 9Ch

23	22	21	20	19	18	17	16
TG_ILLUMEN_MASK_END							
R/W - FFh							
15	14	13	12	11	10	9	8
TG_ILLUMEN_MASK_END				TG_ILLUMEN_MASK_START			
R/W - Fh				R/W - 0h			
7	6	5	4	3	2	1	0
TG_ILLUMEN_MASK_START							
R/W - 0h							

Table 144. Register 9C Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TG_ILLUMEN_MASK_END	R/W	FFFh	Illumination enable TG signal mask end position (number of sub-frame) in frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.
11:0	TG_ILLUMEN_MASK_START	R/W	0h	Illumination enable TG signal mask start position (number of sub-frame) in frame. TG signal will exist between START and END sub-frames.

7.5.1.1.116 Register 9Dh (Address = 9Dh) [reset = 0h]

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Figure 144. Register 9Dh

23	22	21	20	19	18	17	16
TG_CALC_MASK_END							
15	14	13	12	11	10	9	8
TG_CALC_MASK_END				TG_CALC_MASK_START			
7	6	5	4	3	2	1	0
TG_CALC_MASK_START							

Table 145. Register 9D Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TG_CALC_MASK_END	R/W	0h	Calculation TG signal mask end position (number of sub-frame) in frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.
11:0	TG_CALC_MASK_START	R/W	0h	Calculation TG signal mask start position (number of sub-frame) in frame. TG signal will exist between START and END sub-frames. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1.

7.5.1.1.117 Register 9Eh (Address = 9Eh) [reset = 0h]

Figure 145. Register 9Eh

23	22	21	20	19	18	17	16
TG_DYNPDN_MASK_END							
15	14	13	12	11	10	9	8
TG_DYNPDN_MASK_END				TG_DYNPDN_MASK_START			
7	6	5	4	3	2	1	0
TG_DYNPDN_MASK_START							

Table 146. Register 9E Field Descriptions

Bit	Field	Type	Reset	Description
23:12	TG_DYNPDN_MASK_END	R/W	0h	Dynamic power down TG signal mask end position (number of sub-frame) in frame. This register should be equal to NUM_AVG_SUB_FRAMES when DIS_TG_ACONF = 1
11:0	TG_DYNPDN_MASK_START	R/W	0h	Dynamic power down TG signal mask start position (number of sub-frame) in frame. TG signal will outside START and END sub-frames.

7.5.1.1.118 Register 9Fh (Address = 9Fh) [reset = 0h]

Figure 146. Register 9Fh

23	22	21	20	19	18	17	16
NUM_AVG_SUB_FRAMES							
15	14	13	12	11	10	9	8
NUM_AVG_SUB_FRAMES				NUM_SUB_FRAMES			
7	6	5	4	3	2	1	0
NUM_SUB_FRAMES							

Table 147. Register 9F Field Descriptions

Bit	Field	Type	Reset	Description
23:12	NUM_AVG_SUB_FRAMES	R/W	0h	Specifies the number of sub-frames to be averaged in a frame. Averaging sub-frames = NUM_AVG_SUB_FRAMES + 1.
11:0	NUM_SUB_FRAMES	R/W	0h	Total number of sub-frames in a frame. Each sub-frame is approximately 0.25 ms (SUB_VD_CLK_CNT × 25 ns) Number of sub frames in a frame = NUM_SUB_FRAMES + 1. This number must be equal or greater than NUM_AVG_SUB_FRAMES.

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7.5.1.1.119 Register A0h (Address = A0h) [reset = 2198h]

Figure 147. Register A0h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h
15	14	13	12	11	10	9	8
CAPTURE_CLK_CNT							
R/W - 21h							
7	6	5	4	3	2	1	0
CAPTURE_CLK_CNT							
R/W - 98h							

Table 148. Register A0 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	0	R/W	0h	Always read or write 0h
15:0	CAPTURE_CLK_CNT	R/W	2198h	Internal data capture position (number of TG CLKs) in a sub frame

7.5.1.1.120 Register A2h (Address = A2h) [reset = 0h]

Figure 148. Register A2h

23	22	21	20	19	18	17	16
A3_COEFF_HDR0_TX1[15:8]							
15	14	13	12	11	10	9	8
A0_COEFF_HDR1_TX0							
7	6	5	4	3	2	1	0
A0_COEFF_HDR1_TX0							

Table 149. Register A2 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR0_TX1[15:8]	R/W	0h	MSB of third order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.
15:0	A0_COEFF_HDR1_TX0	R/W	0h	Constant offset for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.

7.5.1.1.121 Register A3h (Address = A3h) [reset = 0h]

Figure 149. Register A3h

23	22	21	20	19	18	17	16
A3_COEFF_HDR0_TX1[7:0]							
15	14	13	12	11	10	9	8
A0_COEFF_HDR0_TX1							
7	6	5	4	3	2	1	0
A0_COEFF_HDR0_TX1							

Table 150. Register A3 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR0_TX1[7:0]	R/W	0h	LSB of third order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.
15:0	A0_COEFF_HDR0_TX1	R/W	0h	Constant offset for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.

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7.5.1.1.122 Register A4h (Address = A4h) [reset = 0h]

Figure 150. Register A4h

23	22	21	20	19	18	17	16
A3_COEFF_HDR1_TX1[15:8]							
15	14	13	12	11	10	9	8
A0_COEFF_HDR1_TX1							
7	6	5	4	3	2	1	0
A0_COEFF_HDR1_TX1							

Table 151. Register A4 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR1_TX1[15:8]	R/W	0h	MSB of third order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
15:0	A0_COEFF_HDR1_TX1	R/W	0h	Constant offset for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.

7.5.1.1.123 Register A5h (Address = A5h) [reset = 0h]

Figure 151. Register A5h

23	22	21	20	19	18	17	16
A3_COEFF_HDR1_TX1[7:0]							
15	14	13	12	11	10	9	8
A0_COEFF_HDR0_TX2							
7	6	5	4	3	2	1	0
A0_COEFF_HDR0_TX2							

Table 152. Register A5 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR1_TX1[7:0]	R/W	0h	LSB of third order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
15:0	A0_COEFF_HDR0_TX2	R/W	0h	Constant offset for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.

7.5.1.1.124 Register A6h (Address = A6h) [reset = 0h]

Figure 152. Register A6h

23	22	21	20	19	18	17	16
A3_COEFF_HDR0_TX2[15:8]							
15	14	13	12	11	10	9	8
A0_COEFF_HDR1_TX2							
7	6	5	4	3	2	1	0
A0_COEFF_HDR1_TX2							

Table 153. Register A6 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR0_TX2[15:8]	R/W	0h	MSB of third order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.
15:0	A0_COEFF_HDR1_TX2	R/W	0h	Constant offset for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.

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7.5.1.1.125 Register A7h (Address = A7h) [reset = 0h]

Figure 153. Register A7h

23	22	21	20	19	18	17	16
A3_COEFF_HDR0_TX2[7:0]							
15	14	13	12	11	10	9	8
A1_COEFF_HDR1_TX0							
7	6	5	4	3	2	1	0
A1_COEFF_HDR1_TX0							

Table 154. Register A7 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR0_TX2[7:0]	R/W	0h	LSB of third order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.
15:0	A1_COEFF_HDR1_TX0	R/W	0h	First order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.

7.5.1.1.126 Register A8h (Address = A8h) [reset = 0h]

Figure 154. Register A8h

23	22	21	20	19	18	17	16
A3_COEFF_HDR1_TX2[15:8]							
15	14	13	12	11	10	9	8
A1_COEFF_HDR0_TX1							
7	6	5	4	3	2	1	0
A1_COEFF_HDR0_TX1							

Table 155. Register A8 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR1_TX2[15:8]	R/W	0h	MSB of third order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.
15:0	A1_COEFF_HDR0_TX1	R/W	0h	First order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.

7.5.1.1.127 Register A9h (Address = A9h) [reset = 0h]

Figure 155. Register A9h

23	22	21	20	19	18	17	16
A3_COEFF_HDR1_TX2[7:0]							
15	14	13	12	11	10	9	8
A1_COEFF_HDR1_TX1							
7	6	5	4	3	2	1	0
A1_COEFF_HDR1_TX1							

Table 156. Register A9 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A3_COEFF_HDR1_TX2[7:0]	R/W	0h	LSB of third order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.
15:0	A1_COEFF_HDR1_TX1	R/W	0h	First order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.

ADVANCE INFORMATION

7.5.1.1.128 Register AAh (Address = AAh) [reset = 0h]

Figure 156. Register AAh

23	22	21	20	19	18	17	16
A4_COEFF_HDR1_TX0[15:8]							
15	14	13	12	11	10	9	8
A1_COEFF_HDR0_TX2							
7	6	5	4	3	2	1	0
A1_COEFF_HDR0_TX2							

Table 157. Register AA Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR1_TX0[15:8]	R/W	0h	MSB of fourth order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.
15:0	A1_COEFF_HDR0_TX2	R/W	0h	First order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.

7.5.1.1.129 Register ABh (Address = ABh) [reset = 0h]

Figure 157. Register ABh

23	22	21	20	19	18	17	16
A4_COEFF_HDR1_TX0[7:0]							
15	14	13	12	11	10	9	8
A1_COEFF_HDR1_TX2							
7	6	5	4	3	2	1	0
A1_COEFF_HDR1_TX2							

Table 158. Register AB Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR1_TX0[7:0]	R/W	0h	LSB of fourth order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.
15:0	A1_COEFF_HDR1_TX2	R/W	0h	First order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.

7.5.1.1.130 Register ACh (Address = ACh) [reset = 0h]

Figure 158. Register ACh

23	22	21	20	19	18	17	16
A4_COEFF_HDR0_TX1[15:8]							
15	14	13	12	11	10	9	8
A2_COEFF_HDR1_TX0							
7	6	5	4	3	2	1	0
A2_COEFF_HDR1_TX0							

Table 159. Register AC Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR0_TX1[15:8]	R/W	0h	MSB of fourth order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.
15:0	A2_COEFF_HDR1_TX0	R/W	0h	Second order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.

ADVANCE INFORMATION

7.5.1.1.131 Register ADh (Address = ADh) [reset = 0h]

Figure 159. Register ADh

23	22	21	20	19	18	17	16
A4_COEFF_HDR0_TX1[7:0]							
15	14	13	12	11	10	9	8
A2_COEFF_HDR0_TX1							
7	6	5	4	3	2	1	0
A2_COEFF_HDR0_TX1							

Table 160. Register AD Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR0_TX1[7:0]	R/W	0h	LSB of fourth order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.
15:0	A2_COEFF_HDR0_TX1	R/W	0h	Second order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_L_TX1.

7.5.1.1.132 Register AEh (Address = AEh) [reset = 0h]

Figure 160. Register AEh

23	22	21	20	19	18	17	16
A4_COEFF_HDR1_TX1[15:8]							
15	14	13	12	11	10	9	8
A2_COEFF_HDR1_TX1							
7	6	5	4	3	2	1	0
A2_COEFF_HDR1_TX1							

Table 161. Register AE Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR1_TX1[15:8]	R/W	0h	MSB of fourth order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
15:0	A2_COEFF_HDR1_TX1	R/W	0h	Second order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.

7.5.1.1.133 Register AFh (Address = AFh) [reset = 0h]

Figure 161. Register AFh

23	22	21	20	19	18	17	16
A4_COEFF_HDR1_TX1[7:0]							
15	14	13	12	11	10	9	8
A2_COEFF_HDR0_TX2							
7	6	5	4	3	2	1	0
A2_COEFF_HDR0_TX2							

Table 162. Register AF Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR1_TX1[7:0]	R/W	0h	LSB of fourth order coefficient for square wave non-linearity correction for TX1 illumination channel with current of ILLUM_DAC_H_TX1.
15:0	A2_COEFF_HDR0_TX2	R/W	0h	Second order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.

ADVANCE INFORMATION

7.5.1.1.134 Register B0h (Address = B0h) [reset = 0h]

Figure 162. Register B0h

23	22	21	20	19	18	17	16
A4_COEFF_HDR0_TX2[15:8]							
15	14	13	12	11	10	9	8
A2_COEFF_HDR1_TX2							
7	6	5	4	3	2	1	0
A2_COEFF_HDR1_TX2							

Table 163. Register B0 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR0_TX2[15:8]	R/W	0h	MSB of fourth order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.
15:0	A2_COEFF_HDR1_TX2	R/W	0h	Second order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.

7.5.1.1.135 Register B1h (Address = B1h) [reset = 0h]

Figure 163. Register B1h

23	22	21	20	19	18	17	16
A4_COEFF_HDR0_TX2[7:0]							
15	14	13	12	11	10	9	8
A3_COEFF_HDR1_TX0							
7	6	5	4	3	2	1	0
A3_COEFF_HDR1_TX0							

Table 164. Register B1 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	A4_COEFF_HDR0_TX2[7:0]	R/W	0h	LSB of fourth order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_L_TX2.
15:0	A3_COEFF_HDR1_TX0	R/W	0h	Third order coefficient for square wave non-linearity correction for TX0 illumination channel with current of ILLUM_DAC_H_TX0.

7.5.1.1.136 Register B2h (Address = B2h) [reset = 0h]

Figure 164. Register B2h

23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0
15	14	13	12	11	10	9	8
A4_COEFF_HDR1_TX2							
7	6	5	4	3	2	1	0
A4_COEFF_HDR1_TX2							

Table 165. Register B2 Field Descriptions

Bit	Field	Type	Reset	Description
15:0	A4_COEFF_HDR1_TX2	R/W	0h	Fourth order coefficient for square wave non-linearity correction for TX2 illumination channel with current of ILLUM_DAC_H_TX2.

7.5.1.1.137 Register B4h (Address = B4h) [reset = 0h]

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Figure 165. Register B4h

23	22	21	20	19	18	17	16
AMB_PHASE_CORR_PWL_COEFF3							
15	14	13	12	11	10	9	8
AMB_PHASE_CORR_PWL_COEFF2							
7	6	5	4	3	2	1	0
AMB_PHASE_CORR_PWL_COEFF1							

Table 166. Register B4 Field Descriptions

Bit	Field	Type	Reset	Description
23:16	AMB_PHASE_CORR_PWL_COEFF3	R/W	0h	Coefficient 3 for PWL phase correction with ambient.
15:8	AMB_PHASE_CORR_PWL_COEFF2	R/W	0h	Coefficient 2 for PWL phase correction with ambient.
7:0	AMB_PHASE_CORR_PWL_COEFF1	R/W	0h	Coefficient 1 for PWL phase correction with ambient.

7.5.1.1.138 Register B5h (Address = B5h) [reset = 0h]

Figure 166. Register B5h

23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8
7	6	5	4	3	2	1	0
					SCALE_AMB_PHASE_CORR_COEFF		

Table 167. Register B5 Field Descriptions

Bit	Field	Type	Reset	Description
23:3	0	R/W	0h	Always read or write 0h.
2:0	SCALE_AMB_PHASE_CORR_COEFF	R/W	0h	Scaling factor for ambient based PWL phase correction.

7.5.1.1.139 Register B8h (Address = B8h) [reset = 7FDFFh]

Figure 167. Register B8h

23	22	21	20	19	18	17	16
0	0	0	GIVE_DEAL_DATA	AMB_PHASE_CORR_PWL_X1			
R/W - 0h	R/W - 0h	R/W - 0h	R/W - 0h	R/W - 7h			
15	14	13	12	11	10	9	8
AMB_PHASE_CORR_PWL_X1						AMB_PHASE_CORR_PWL_X0	
R/W - 3Fh						R/W - 1h	
7	6	5	4	3	2	1	0
AMB_PHASE_CORR_PWL_X0							
R/W - FFh							

Table 168. Register B8 Field Descriptions

Bit	Field	Type	Reset	Description
23:21	0	R/W	0h	Always read or write 0h.
20	GIVE_DEALIAS_DATA	R/W	0h	When this register is set to 1, de-aliased phase will be given out on PHASE_OUT.
19:10	AMB_PHASE_CORR_PWL_X1	R/W	1FFh	Second knee point of PWL phase correction with ambient.

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Table 168. Register B8 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9:0	AMB_PHASE_CORR_PWL_X0	R/W	1FFh	First knee point of PWL phase correction with ambient.

7.5.1.1.140 Register B8h (Address = B9h) [reset = 1FFh]

Figure 168. Register B9h

23	22	21	20	19	18	17	16
ILLUM_SCALE_H_TX2			ILLUM_SCALE_L_TX2			AMB_ADC_IN_TX2	
R/W - 0h			R/W - 0h			R/W - 0h	
15	14	13	12	11	10	9	8
AMB_ADC_IN_TX1		AMB_ADC_IN_TX0		EN_TX2_ON_TX0	EN_TX1_ON_TX0	AMB_PHASE_CORR_PWL_X2	
R/W - 0h		R/W - 0h		R/W - 0h	R/W - 0h	R/W - 1h	
7	6	5	4	3	2	1	0
AMB_PHASE_CORR_PWL_X2							
R/W - FFh							

Table 169. Register B9 Field Descriptions

Bit	Field	Type	Reset	Description
23:21	ILLUM_SCALE_H_TX2	R/W	0h	Illumination driver current scale register of TX2 Channel with DAC_H current. 0: 5.6 mA | 1: 4.2 mA | 2: 2.8 mA | 3: 1.4 mA
20:18	ILLUM_SCALE_L_TX2	R/W	0h	Illumination driver current scale register of TX2 Channel with DAC_L current. 0: 5.6 mA | 1: 4.2 mA | 2: 2.8 mA | 3: 1.4 mA
17:16	AMB_ADC_IN_TX2	R/W	0h	Select ambient ADC input when TX2 channel is selected. 0 = DACP - DACM | 1 = DACP - REFP | 2 = DACM - DACP | 3 = DACM - REFM
15:14	AMB_ADC_IN_TX1	R/W	0h	Select ambient ADC input when TX1 channel is selected. 0 = DACP - DACM | 1 = DACP - REFP | 2 = DACM - DACP | 3 = DACM - REFM
13:12	AMB_ADC_IN_TX0	R/W	0h	Select ambient ADC input when TX0 channel is selected. 0 = DACP - DACM | 1 = DACP - REFP | 2 = DACM - DACP | 3 = DACM - REFM
11	EN_TX2_ON_TX0	R/W	0h	If this bit is 1, when TX2 is selected, the illumination driver current will flow through TX0.
10	EN_TX1_ON_TX0	R/W	0h	If this bit is 1, when TX1 is selected, the illumination driver current will flow through TX0.
9:0	AMB_PHASE_CORR_PWL_X2	R/W	1FFh	Third knee point of PWL phase correction with ambient

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

OPT3101 AFE is a fully integrated analog front end with integrated illumination driver for measuring distance. The device interfaces external photodiode and LED/VCSEL/LASER. Device has I^2C interface for the data output. External MCU can readout the distance data from the device directly and no computation is required on the external MCU. All the computation and corrections for crosstalk, phase offset, temperature dependent phase drift and ambient dependent phase drift are done on the chip. The device also provides temperature output from the on-chip temperature sensor. It can operate up to a speed of 4000 sps in non-HDR mode and 2000 sps in auto HDR mode.

8.2 Typical Application

Obstacle avoidance for autonomous vehicle navigation is a typical application which can be implemented using this AFE. System can be optimized to meet the application requirements by optimizing various parameters like illumination current, sub-frame averaging, auto HDR mode which are explained in below sections. Figure 169 shows the interface between OPT3101 and external MCU.

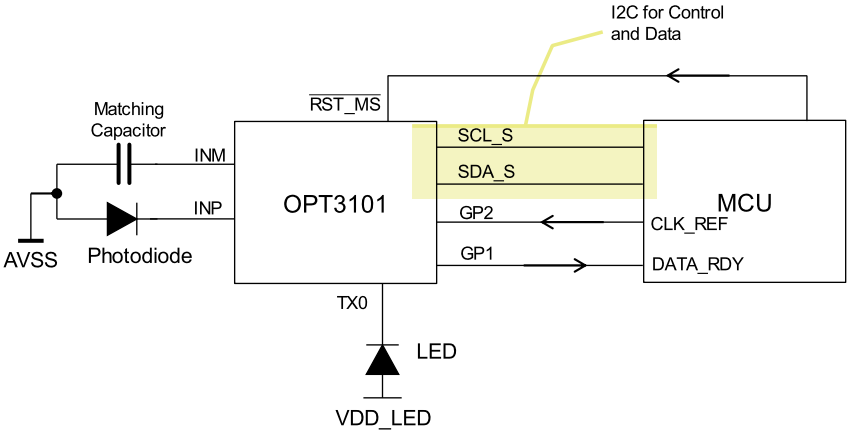

Figure 169. Typical Application Block Diagram

8.2.1 Design Requirements

Table 170 lists the application requirements for obstacle avoidance system.

Table 170. Application Specifications

Specification	Value	Units	Comments
Minimum Distance	0.3	m	
Maximum Distance	5	m	
Distance Accuracy	2	%	For an object with 18% reflectivity.
Ambient Light	130	kLux	Sunlight condition
Field of View	±3	degrees	
Wavelength	850	nm	Infrared wavelength for illumination.
Sample Rate	30	sps	
Supply	3.3	V	Single supply for the system

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8.2.2 Detailed Design Procedure

8.2.2.1 Sample Rate

Sample rate can be adjusted by programming the number of sub-frames in a frame. To meet the application requirement of 30 sps, 128 sub-frame averaging can be used from Equation 1. Set the register NUM_SUB_FRAME = 127 and NUM_AVG_SUB_FRAMES = 127, which will give a samples rate of 31.25 sps.

8.2.2.2 Photo diode and LED

OSRAM SFH4550 LED meets the required field of view specification and has peak of spectral emission at 860 nm. Even though LED is specified for an half angle ±3 degrees, significant amount of the optical power will be outside the half angle. Figure 170 shows the radiation characteristics of the LED. Photodiode should have a field of view greater than the field of view of LED to effectively collect all the optical power thrown from the LED and reflected by the object. Photodiode should also have peak sensitivity matching the LEDs peak spectral emission. Most of the photodiodes come in two variants;

- With day light filter, which has a very broad spectrum; example: SFH213
- Narrow band IR spectrum spectrum; example: SFH213FA.

Photiode with narrow band IR filter should be selected as it will collect lower ambient signal. Photodiode SFH213FA meets these requirements. This photodiode has a capacitance of 5.8 pF at 1-V reverse bias, which is within the supported capacitance range of the AFE. Photodiode characterisitcs are shown in Figure 171 and Figure 172

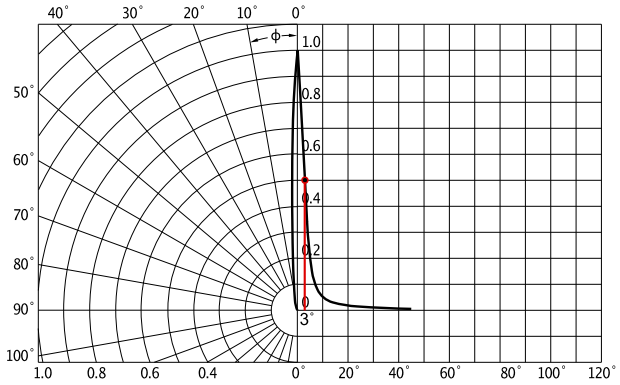

Figure 170. SFH4550 LED Radiation Characteristics

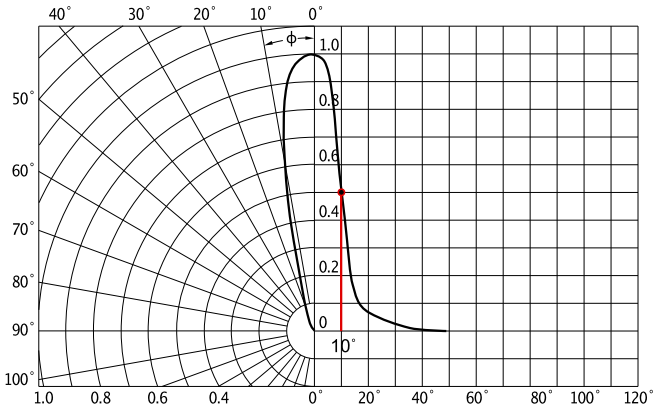

Figure 171. SFH213FA Photodiode Directional Characteristics

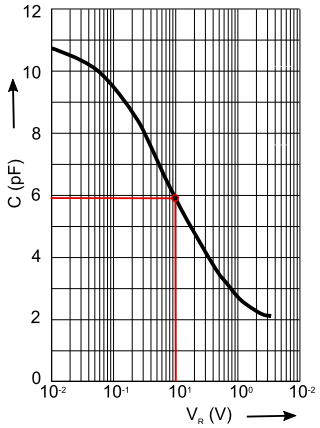

Figure 172. SFH213FA Photodiode Reverse Bias Capacitance

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8.2.2.3 Ambient Support

The photodiode has an IR filter centered at 900 nm as shown in Figure 173, the sunlight spectral irradiance within the spectral bandwidth of the photodiode is also shown in the same figure. The total sunlight power with in the spectral bandwidth of photodiode is 176 Watts/m^2. The ambient sun light power received by the photodiode can be calculated using Equation 8. Total ambient current for this photodiode is 49.2 µA. Accounting for variations in reflectivity IAMB_MAX_SEL = 12 setting should be selected, which corresponds to 100 µA ambient current support.

$$P_{r,amb} = P_{AMB} \times A_{scene} \times \frac{\Omega_{lens}}{\Omega_{semi-sphere}} \text{ in Watts} \quad (8)$$

where

- P_{AMB} = Total ambient light power in the photodiode spectral bandwidth in W/m^2
- A_{scene} = Area covered by photodiode FoV
- Ω_{lens} = Solid angle from a point on target object to the photodiode lens
- $\Omega_{semi\text{-}sphere} = 2\pi$

$$P_{r,amb} \sim \frac{P_{AMB} \times [\tan(\varphi_{PD})]^2}{2} \text{ in Watts/m}^2 \quad (9)$$

where

- φ_{PD} = Photodiode field of view = 20° for SFH213FA

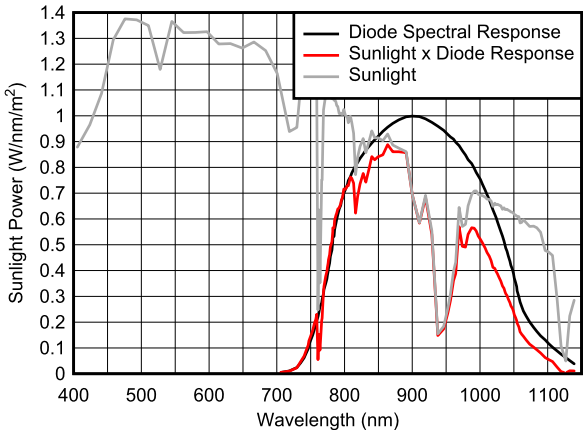

Figure 173. SFH213FA Photodiode Spectral Response and Sunlight Power Within Photodiode Spectral Bandwidth

Table 171. Photodiode Specifications

Parameter	Value	Units	Comments
Photo current with 1mW/cm^2	90	µA	Photodiode specification
Half angle	±10	degrees	Photodiode specification
Total Sunlight Power in photo diode spectral bandwidth falling on the object	175	W/m^2	Calculated from Sunlight spectra (see Figure 173)
Total power received at the photodiode	0.2736	mW/cm^2	Calculated using Equation 9
Ambient current	49.2	µA	Calculated from 0.2736 mW/cm^2 × 90µA/(1 mW/cm^2). Additional factor of 2 should be added to account for the photodiode response outside specified half angle of ±10 degrees.
Reverse bias capacitance at V_R = 1V	5.8	pF	AFE supports a maximum capacitance of 6 pF.

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8.2.2.4 Distance Accuracy

For 30 sps operation, 128 sub-frames can be averaged to improve the noise performance by settings NUM_SUB_FRAMES = 127 and NUM_AVG_SUB_FRAMES = 127. AFE noise with 6pF photodiode capacitance and 100 µA ambient current support can be extracted from Figure 2 as 2.25 pA/rt-Hz. Total noise at 31.25 sps operation with above settings is 12.6 pA. Minimum SNR required to meet the distance accuracy of 2%, (10 cm at 5 m) can be calculated using Equation 5 as 23.8. So minimum signal current required is 12.6 pA × 23.8 = 300 pA. The photodiode current required to get a signal current of 300pA can be calculated from Equation 10 as 720pA. With a diode responsivity of 0.5A/W, the optical power required is 720pA/(0.5A/W) = 1.44nW. Illumination power required with 18% reflective target can be calculated from Equation 11 as 64mW. SFH4550 produces 70mW of optical power for a current of 100mA. From this, the required illumination current can be calculated as 91.5mA

$$I_{SIG\_AFE} = \frac{I_{PD}}{2} \times \frac{30}{(30 + C_{PD})} \quad (10)$$

where

- I_{PD} = Photodiode Signal Current.
- I_{SIG_AFE} = Signal current entering the AFE.
- C_{PD} = Photodiode Capacitance at a reverse bias voltage of 1V.

$$P_{r,sig} = P_{LED} \times \frac{\Omega_{lens}}{\Omega_{semi-sphere}} \times R \text{ in Watts} \quad (11)$$

where

- $P_{r,sig}$ = Signal power received by the photodiode
- P_{LED} = LED output power
- R = Object Reflectivity
- Ω_{lens} = Solid angle from a point on target object to the photodiode lens
- $\Omega_{semi\text{-}sphere} = 2\pi$

$$\Omega_{lens} = 4\pi \sin^2\left(\frac{1}{2}\tan^{-1}\left(\frac{D_{lens}}{2d}\right)\right) \sim \pi \frac{D_{lens}^2}{4d^2} \quad (12)$$

where

- D_{lens} = Diameter of the lens over the photodiode = 5mm for SFH213FA
- d = Object distance

Chose 100 mA as illumination current for meeting the SNR requirement for the 18% reflective target at 5 m distance. With this illumination current, 90% reflective object will give a signal current of 1.5 nA for an object at 5m and AFE saturates at an object at a distance of 5 m/sqrt(200 nA/1.5nA) = 0.43 m. Since required minimum distance is lower than this, on chip adaptive HDR should be used by setting ENABLE_ADAPTIVE_HDR = 1, ILLUM_DAC_L_TX0 = 2 and ILLUM_DAC_H_TX0 = 20. HDR switching thresholds can be set at HDR_THR_HIGH = 27000 and HDR_THR_LOW = 27000/10/1.2 = 2250.

8.2.2.5 Supply Voltage

Since the system need to operate with a single supply, OPT3101 can be used in LDO mode where required 1.8V supplies AVDD and DVDD are generated by the device it self using internal LDO. To operate in this mode, connect REG_MODE pin to IOVDD supply (3.3 V).

8.2.3 Application Curves

Figure 174 and Figure 175 shows simulated received signal and distance standard deviation with object distance

ADVANCE INFORMATION

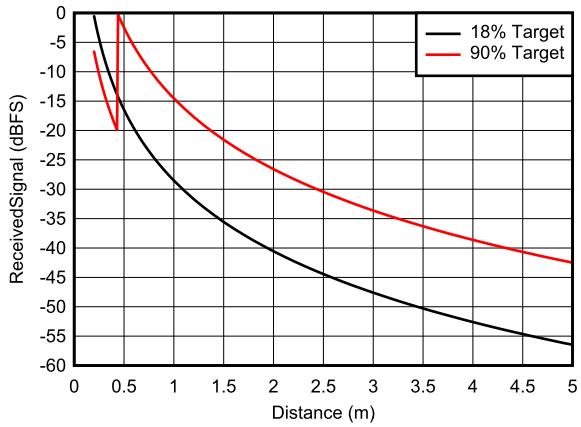

Figure 174. Received Signal vs Object Distance

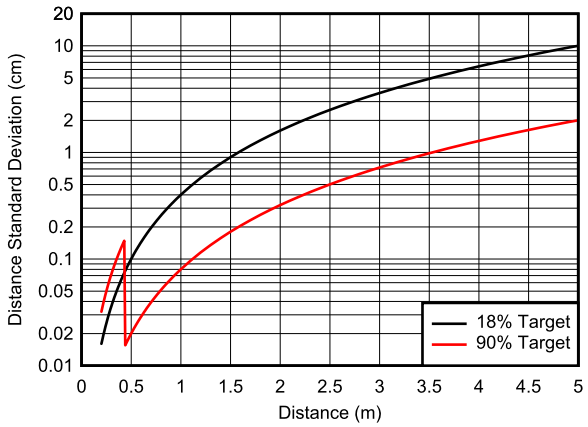

Figure 175. Distance Standard Deviation vs Object Distance

8.3 Initialization Set Up

After device power up, apply device reset by applying an active low pulse of duration > 30 µs.

Write the following registers to set the device running in required condition

- Write NUM_SUB_FRAMES, NUM_AVG_SUB_FRAMES registers to set the device to operate at the required sample rate.
- Select the maximum ambient current to be supported by writing IAMB_MAX_SEL
- Enable adaptive HDR mode if required: EN_ADAPTIVE_HDR.
- Write Illumination DAC currents ILLUM_DAC_L_TX0 and ILLUM_DAC_H_TX0.
- Program adaptive HDR thresholds: HDR_THR_LOW and HDR_THR_HIGH.
- Load all the calibration settings: Illumination crosstalk, Phase offset, Phase temperature coefficient and phase ambient coefficient.
- Enable frequency calibration if external reference CLK is connected to GP2: EN_AUTO_FREQ_COUNT = 1, EN_FLOOP=1, EN_FREQ_CORR=1, SYS_CLK_DIVIDER = round($\log_2(40e^6/f_{EXT})$), REF_COUNT_LIMIT = 2^{14}x($40e^6/2^{SYS\_CLK\_DIV}$)/f_{EXT}, EN_CONT_FCALIB = 1
- Enable on chip temperature conversion: EN_TEMP_CONV = 1
- Write I^2C Host settings to read the external temperature sensor if it is present in the system. Register settings are listed in Table 26
- Enable Timing Generator TG_EN = 1
- Perform internal crosstalk correction by making INT_XTALK_CALIB = 1 and followed by INT_XTALK_CALIB = 0.

ADVANCE INFORMATION

9 Power Supply Recommendations

OPT3101 requires 1.8-V and 3.3-V supplies. There are two 1.8-V supplies (AVDD and DVDD) and two 3.3-V supplies (AVDD3 and IOVDD). AVDD and AVDD3 are analog supplies, DVDD and IOVDD are digital and I/O supplies. VDD_LED is not a device pin, but the supply connecting to the anode of the LED (Illumination source). Minimum voltage of the VDD_LED supply is 0.7 V (V_{DRV}) + Forward voltage drop of the LED at the maximum illumination driver current (1.8-V typical for 850-nm LED with 100 mA) + IR drop across the series elements (beads, PCB routing) in the supply (VDD_LED) – ground (VSSL) path. The transmitter and receiver of OPT3101 operate at the same modulation frequency (10 MHz). Any coupling from the transmitter switching to the AFE will result in crosstalk signal which will affect the performance of the distance measurement. Achieving lowest possible crosstalk is critical for an accurate distance measurement system. Care should be taken to isolate all analog and switching supplies. VDD_LED will have the highest switching current at the modulation frequency, f_{MOD}. DVDD and IOVDD will also have switching current at the modulation frequency f_{MOD} but much lower than VDD_LED. Use ferrite beads with highest impedance at 10 MHz (> 500 Ω) in the series path of the supplies and decoupling capacitors with low impedance at f_{MOD} on the supplies very close to the device.

9.1 System With Off-Chip 1.8-V Regulator

Figure 176 shows the supply network with 1.8 V generated using an off chip regulator. REG_MODE pin of OPT3101 should be connected to IOVSS in this mode. One external regulator can be used to generate 1.8-V supply and use beads to isolate AVDD and DVDD. External regulator mode will be useful only when on chip regulator mode cannot meet the power down state current requirement. For example, In systems where the sample rate is very low and kept in power down state most of the time.

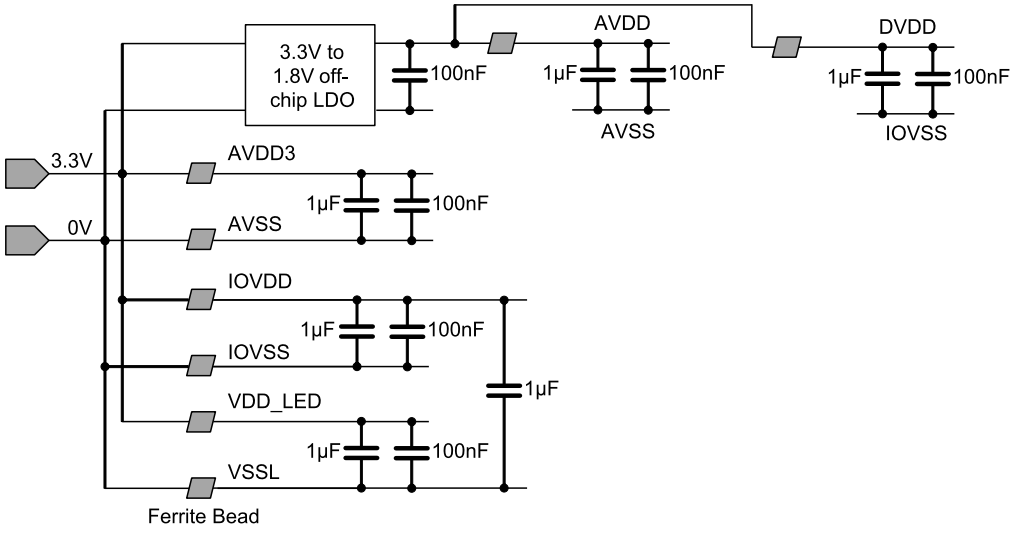

Figure 176. Power Supply Network in System With External 1.8-V Regulator

9.2 System With On-Chip 1.8-V Regulator

Figure 177 shows the supply network with 1.8 V generated using on-chip regulators. There are two regulators one each for AVDD and DVDD with input supply as AVDD3. Only decoupling capacitors need to be placed on AVDD and DVDD supplies. All other supplies should have beads in series path. REG_MODE pin of OPT3101 should be connected to IOVDD in this mode.

ADVANCE INFORMATION

System With On-Chip 1.8-V Regulator (continued)

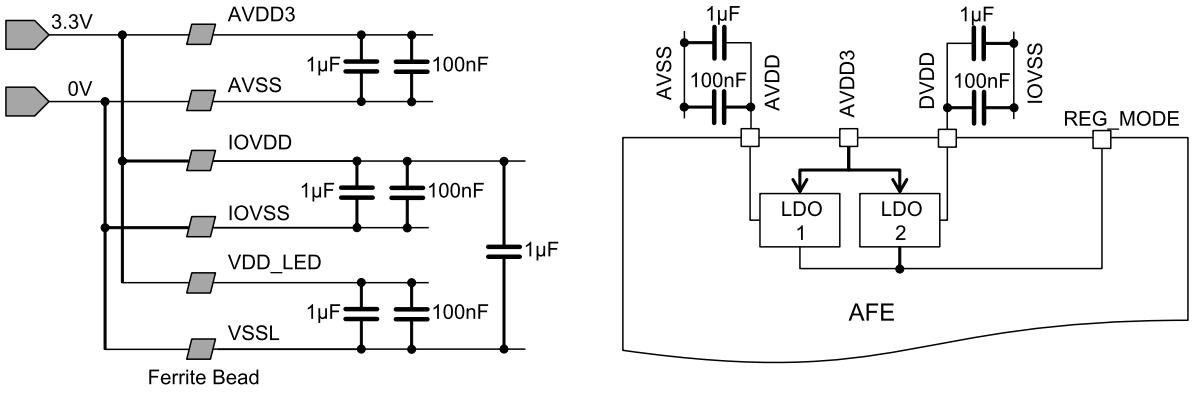

Figure 177. Power Supply Network With On-Chip 1.8-V Regulator

10 Layout

10.1 Layout Guidelines

Reducing coupling between transmitter and receiver is very critical to achieve good system performance. Area of transmitter current carrying loop through LED supply decoupling capacitor, LED and the AFE pins TX*, VSSL should be minimized. Similarly receiver loop involving the photodiode, matching capacitor and the AFE pins INP, INM should be minimized.Figure 178 shows the transmitter and receiver loops.

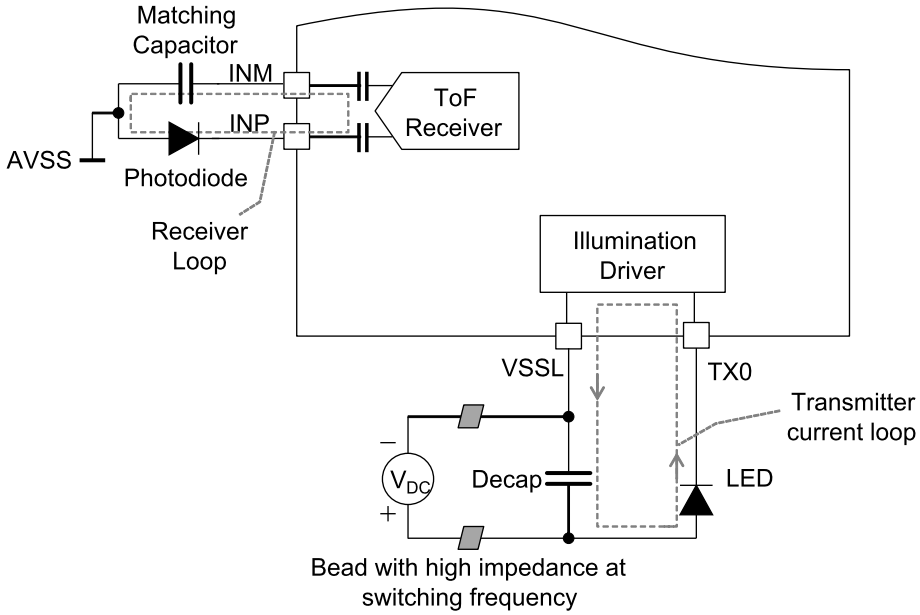

Figure 178. AFE Interface With Photodiode and LED

10.2 Layout Example

Layout of a system involving 5-mm radial through hole photodiode and LED is shown in Figure 179. Following guidelines should be followed to keep the crosstalk between transmitter and receiver low.

- Use a 4 layer board, so that all the analog and digital supplies can be well isolated from each other.
- Place photodiode and LED oriented orthogonal to each other .
- Minimize the area of the transmitter current carrying loop involving LED, VDD_LED to VSSL decoupling

Layout Example (continued)

capacitor, and AFE.

- Minimize the area of the receiver loop involving photodiode, matching capacitor and AFE.
- Shield the receiver loop using AVSS ground in TOP and bottom PCB layers. Also place a shielding ring around the photodiode and connect the shielding ring to AVSS. This shielding ring will help in reducing the electrical and optical crosstalk.
- Shield the transmitter loop using IOVSS ground in all the PCB layers. Also place a shielding ring around the LED and connect the shielding ring to IOVSS.
- LED terminals should not see the photodiode terminals directly. Any small amount of capacitive coupling between photodiode and LED terminals result in huge crosstalk. Grounded metal rings around photodiode and LED will help in shielding.
- Use vias around the transmitter and receiver loops in respective ground planes to improve the shielding.
- Connect the device thermal pad to AVSS.
- Do not overlap different ground planes, keep them well isolated.

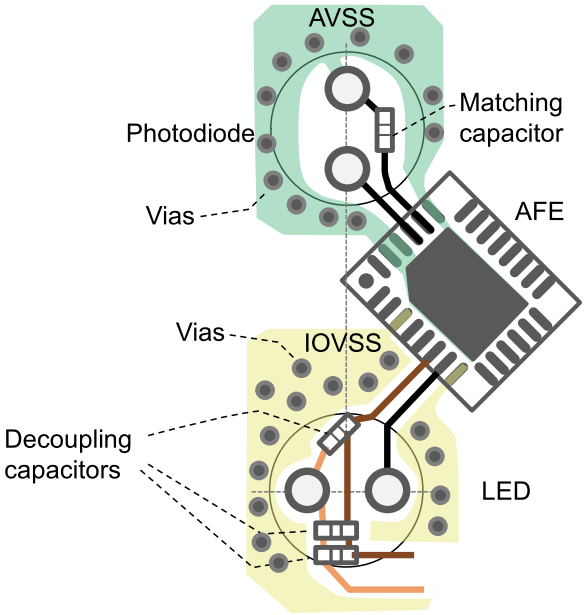

Figure 179. PCB Layout example

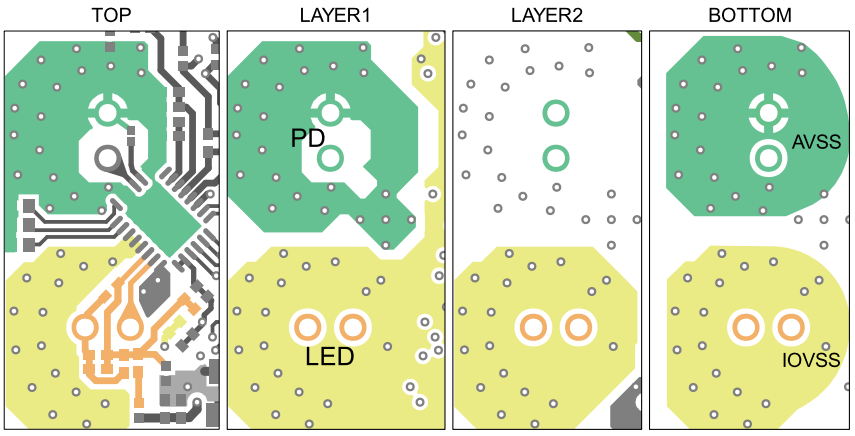

Figure 180. Ground isolation between AVSS and IOVSS in a four layer PCB

ADVANCE INFORMATION

Layout Example (continued)

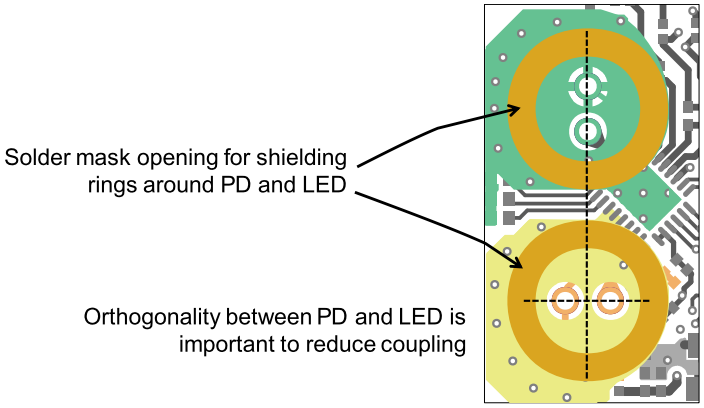

Figure 181. Photodiode and LED placement on PCB

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
POPT3101RHFR	PREVIEW	VQFN	RHF	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	–40 to +85	OPT3101

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

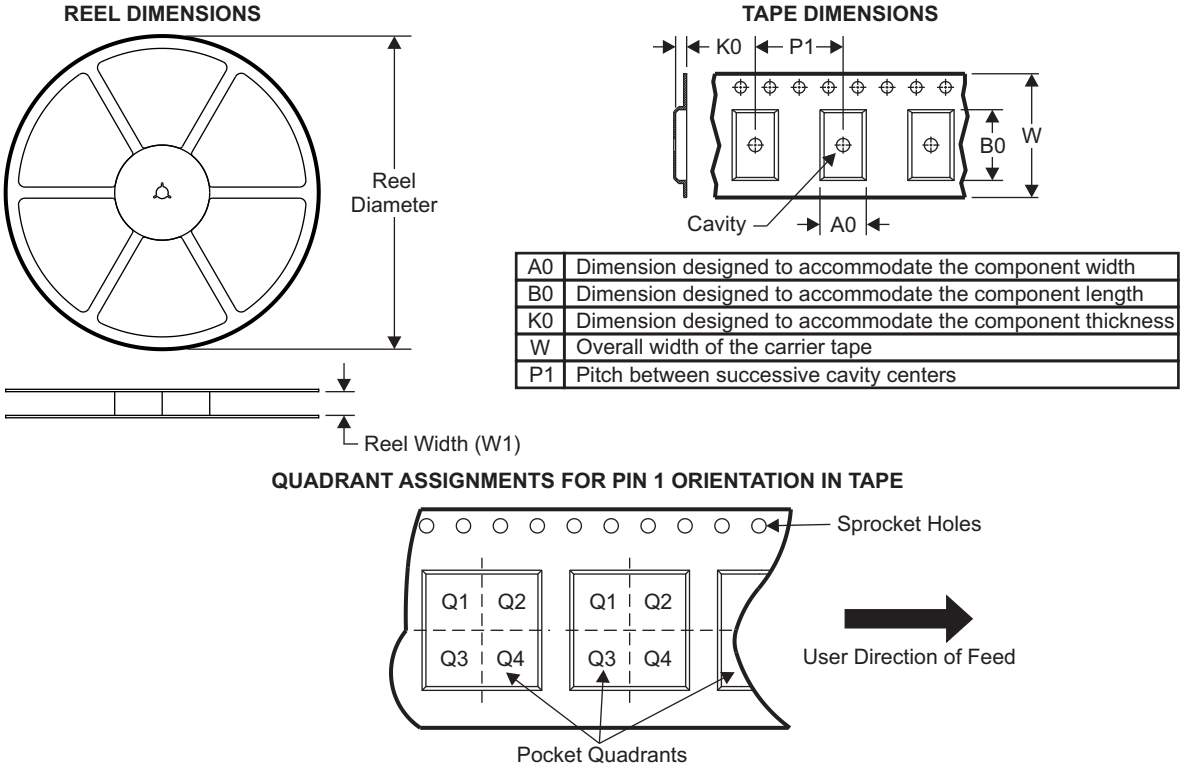
(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

12.1.2 Tape and Reel Information



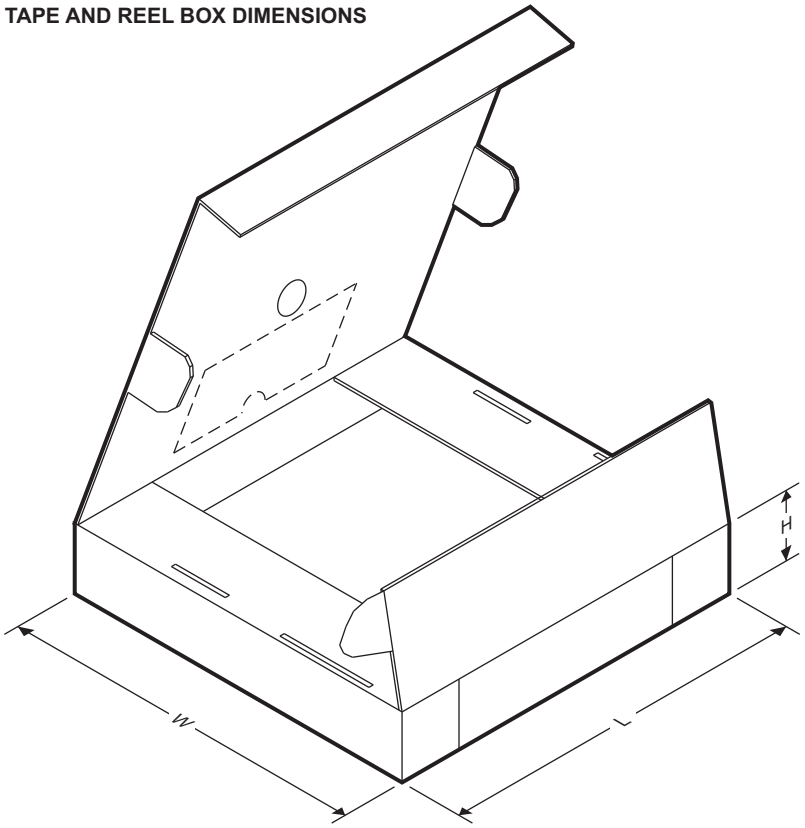
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
POPT3101RHFR	VQFN	RHF	28	3000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



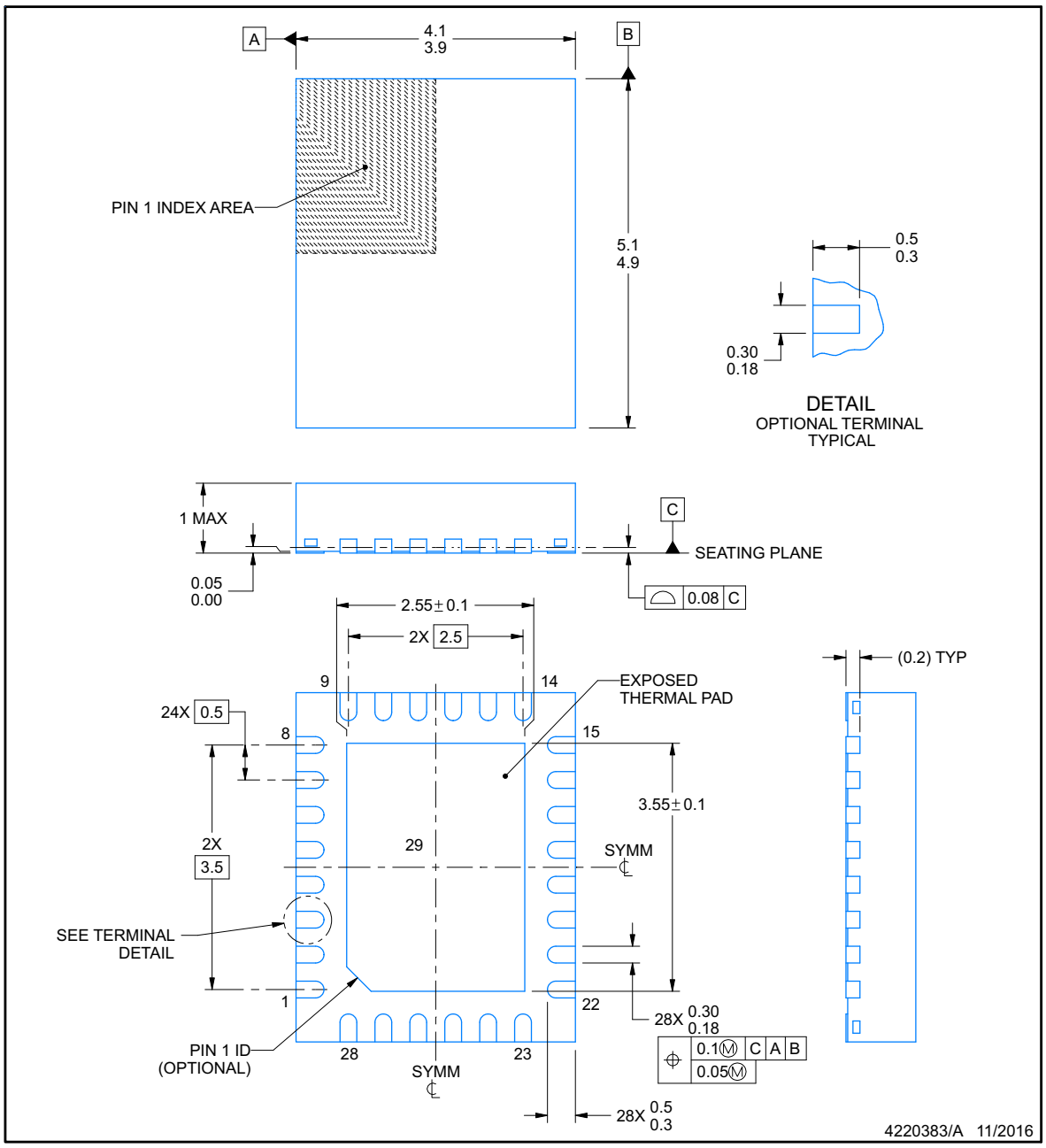
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
POPT3101RHFR	VQFN	RHF	28	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RHF0028A

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

ADVANCE INFORMATION

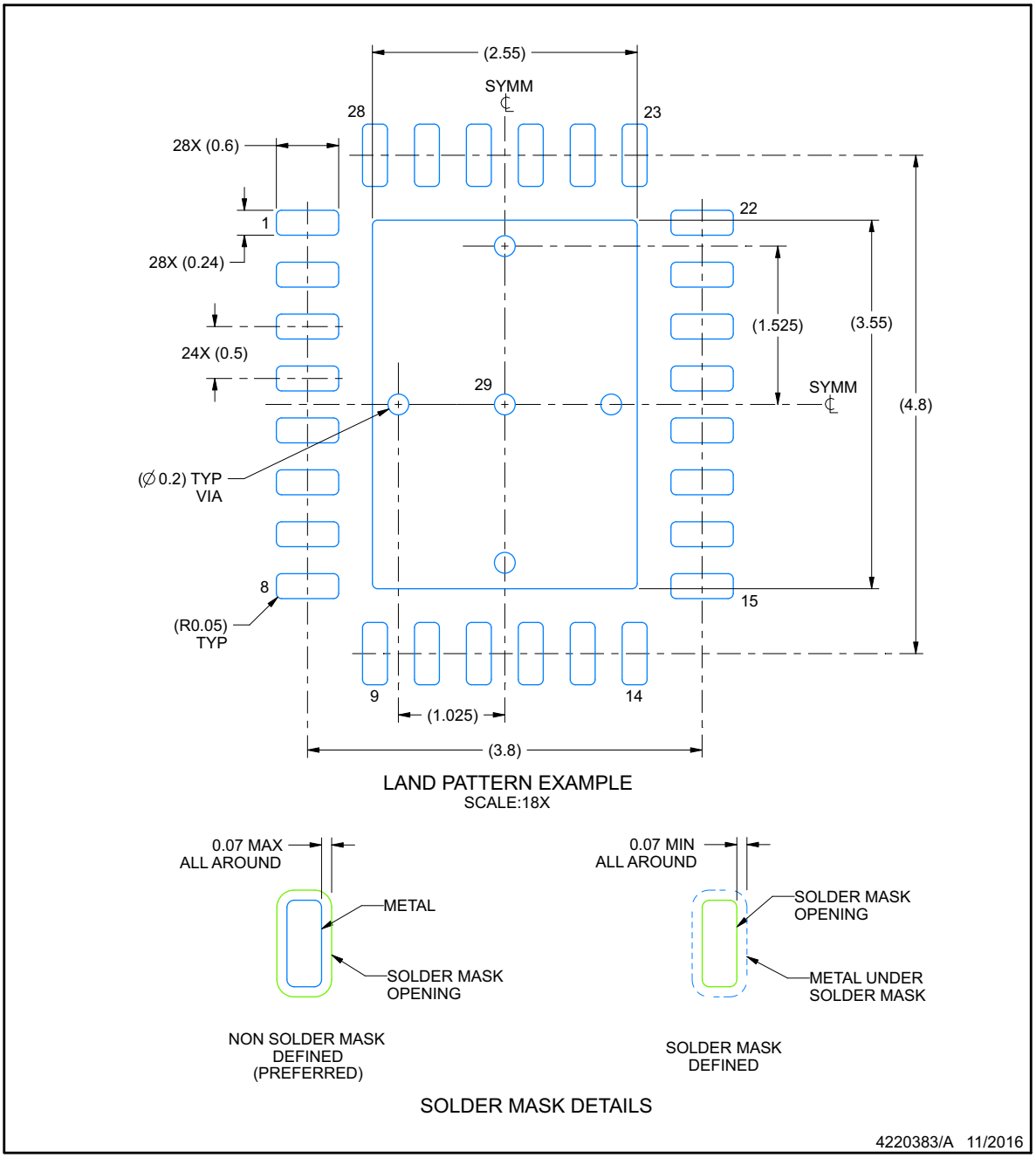
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RHF0028A

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

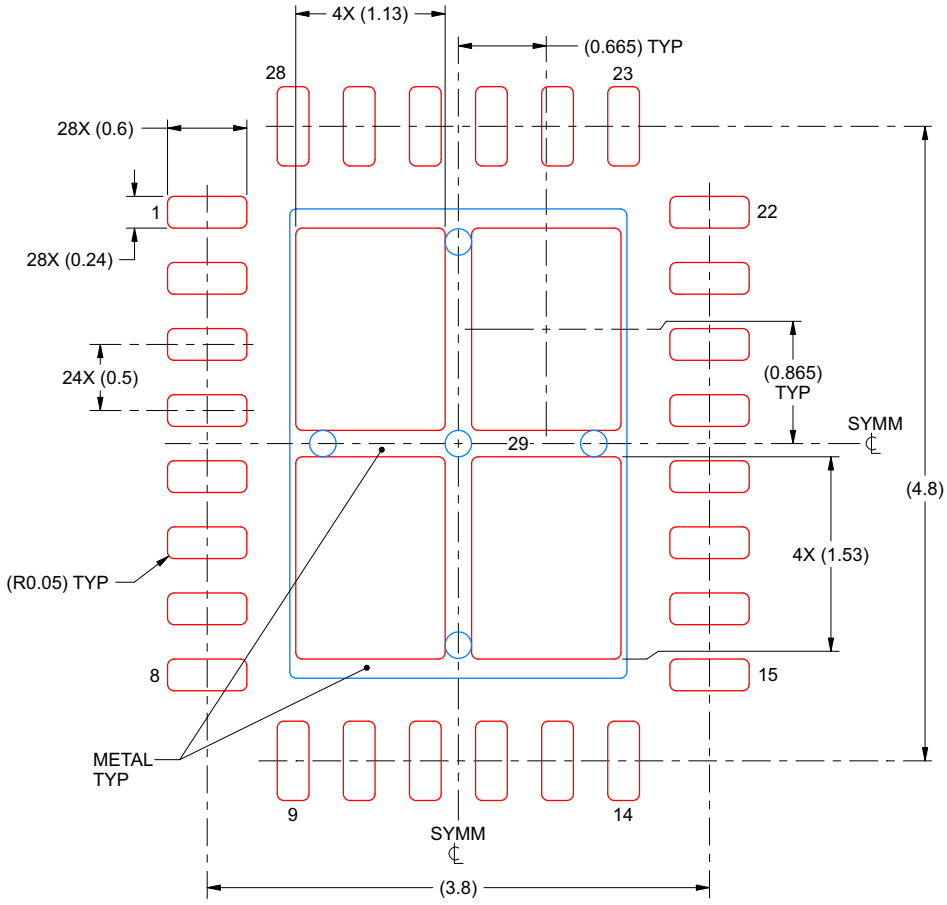
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHF0028A

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4220383/A 11/2016

NOTES: (continued)

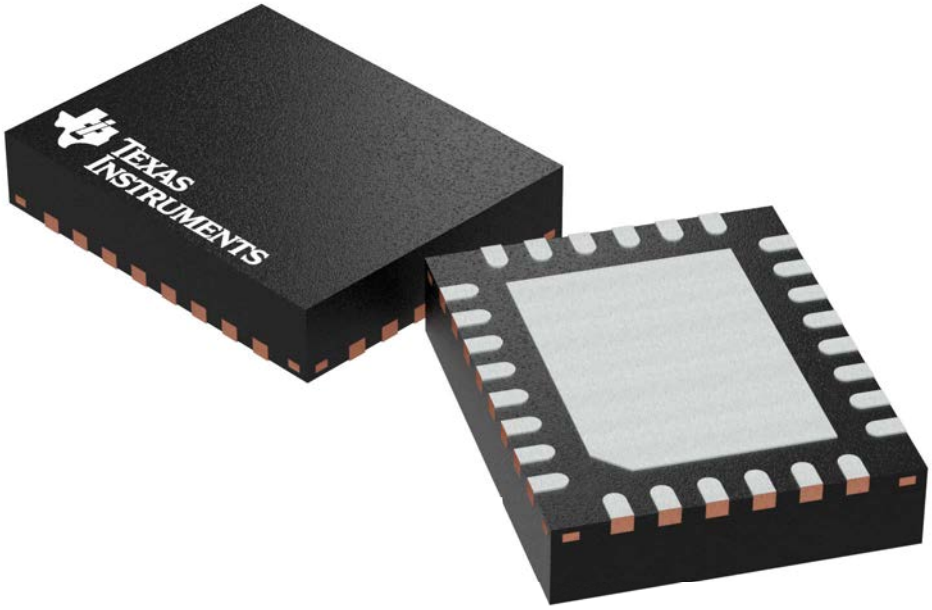
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

RHF 28

VQFN - 1.0 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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