TRINITY
REV 1.01
FAB G RETAIL

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[10]	GCPU, DECOUPLING
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[23]	HANA, VIDEO + FAN + AUDIO
[24]	HANA, POWER + DECOUPLING
[25]	HANA, POWER + DECOUPLING
[26]	PSB, PCIEX + SMM GPIO + JTAG
[27]	PSB, SMC
[28]	PSB, FLASH + USB + SPI
[29]	PSB, ETHERNET + AUDIO + SATA
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[35]	INFRARED+SWITCHES+ACCELEROMETER+AUDIBLE F/B
[36]	CONN, FAN
[37]	CONN, AVIP
[38]	CONN, RJ45 USB AUX COMBO + BORON + PWR
[39]	CONN, USB + MEM PORTS + TOSLINK + WAVEPORT
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[50]	VREGS, VMEM
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[54]	BOARD, DECOUPLING
[55]	MARGIN, VMEM + VEDRAM
[56]	MARGIN, V3P3 + V5P0
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RULES: (APPLIED WHEN POSSIBLE)
1.) MSB TO LSB IS TOP TO BOTTOM
2.) WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3.) ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4.) AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5.) LANED SIGNALS ARE GROUPED ON SYMBOLS
6.) TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7.) SUFFIX V_ IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8.) SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9.) UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10.) SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12.) SUFFIX _P FOR P JUNCTION
13.) SUFFIX _EN FOR ENABLE
14.) 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15.) PWRGD FOR POWER GOOD
16.) REV AND FAB ARE SET USING CUSTOM VARIABLES. TOOLS>OPTIONS>VARIABLES

[PAGE_TITLE=COVER PAGE]

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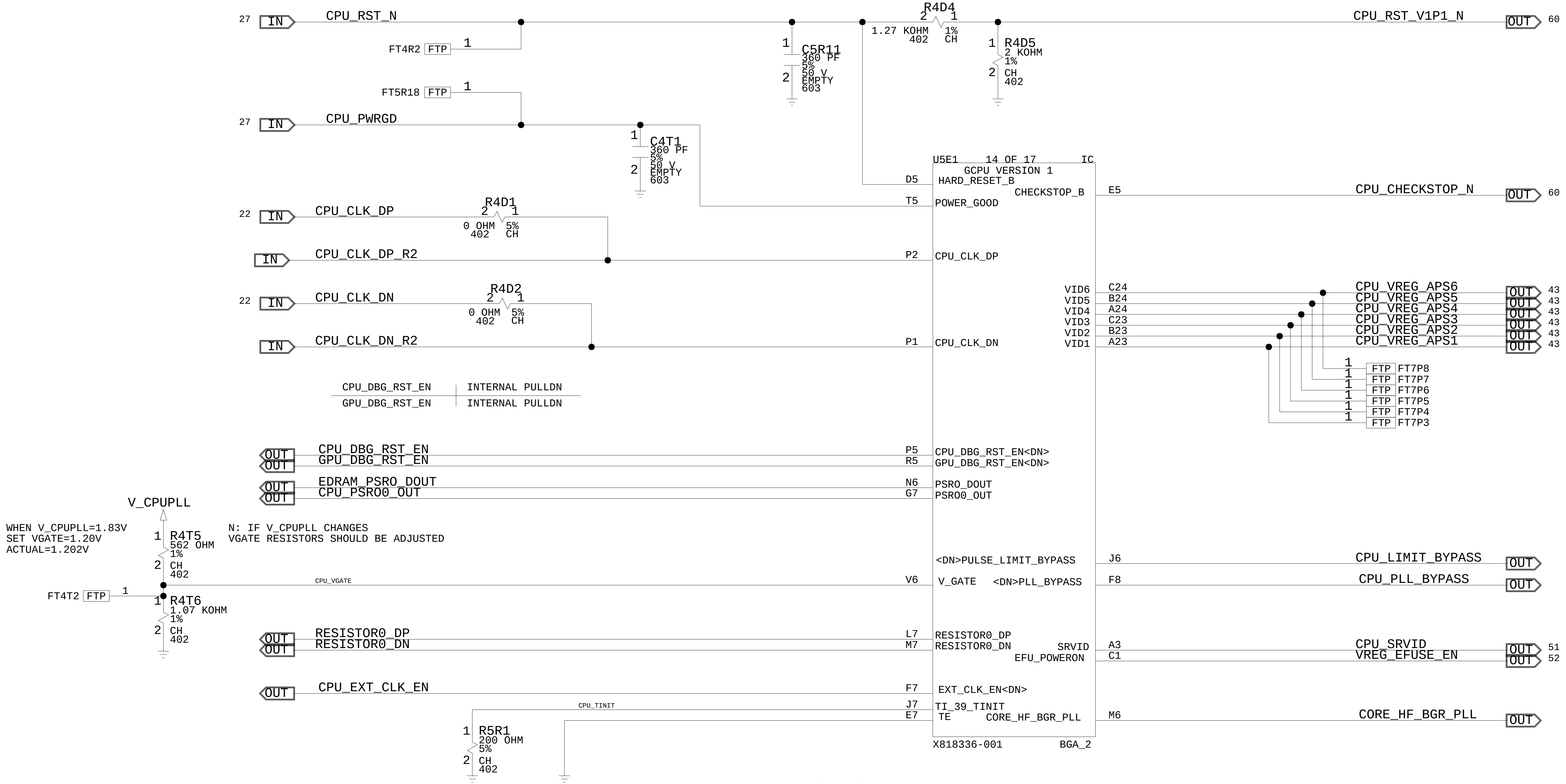
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	1/81	G	1.01

GCPU SETUP


27 IN CPU_RST_N
FT4R2 FTP 1
FT5R18 FTP 1
27 IN CPU_PWRGD
C5R11 360 PF 5% 50 V EMPTY 603
C4T1 360 PF 5% 50 V EMPTY 603
R4D4 1.27 KOHM 402 1% CH
R4D5 2 KOHM 1% CH 402
CPU_RST_V1P1_N OUT 60
22 IN CPU_CLK_DP
R4D1 0 OHM 402 5% CH
IN CPU_CLK_DP_R2
22 IN CPU_CLK_DN
R4D2 0 OHM 402 5% CH
IN CPU_CLK_DN_R2
U5E1 14 OF 17 IC
GCPU VERSION 1
D5 HARD_RESET_B
T5 POWER_GOOD
CHECKSTOP_B E5
CPU_CHECKSTOP_N OUT 60
P2 CPU_CLK_DP
P1 CPU_CLK_DN
VID6 C24 CPU_VREG_APS6 OUT 43
VID5 B24 CPU_VREG_APS5 OUT 43
VID4 A24 CPU_VREG_APS4 OUT 43
VID3 C23 CPU_VREG_APS3 OUT 43
VID2 B23 CPU_VREG_APS2 OUT 43
VID1 A23 CPU_VREG_APS1 OUT 43
FTP FT7P8
FTP FT7P7
FTP FT7P6
FTP FT7P5
FTP FT7P4
FTP FT7P3
OUT CPU_DBG_RST_EN P5 CPU_DBG_RST_EN<DN>
OUT GPU_DBG_RST_EN R5 GPU_DBG_RST_EN<DN>
OUT EDRAM_PSRO_DOUT N6 PSRO_DOUT
OUT CPU_PSRO0_OUT G7 PSRO0_OUT
V_CPUPLL
WHEN V_CPUPLL=1.83V
SET VGATE=1.20V
ACTUAL=1.202V
N: IF V_CPUPLL CHANGES
VGATE RESISTORS SHOULD BE ADJUSTED
R4T5 562 OHM 1% CH 402
R4T6 1.07 KOHM 1% CH 402
FT4T2 FTP 1
CPU_VGATE
V6 V_GATE
<DN>PULSE_LIMIT_BYPASS J6 CPU_LIMIT_BYPASS OUT
<DN>PLL_BYPASS F8 CPU_PLL_BYPASS OUT
OUT RESISTOR0_DP L7 RESISTOR0_DP
OUT RESISTOR0_DN M7 RESISTOR0_DN
SRVID A3 CPU_SRVID OUT 51
EFU_POWERON C1 VREG_EFUSE_EN OUT 52
OUT CPU_EXT_CLK_EN F7 EXT_CLK_EN<DN>
CPU_TINIT
J7 TI_39_TINIT
E7 TE
CORE_HF_BGR_PLL M6 CORE_HF_BGR_PLL OUT
R5R1 200 OHM 5% CH 402
X818336-001 BGA_2

CPU_DBG_RST_EN	INTERNAL PULLDN
GPU_DBG_RST_EN	INTERNAL PULLDN

6 LAYER ONLY SIGNALS

CORE_HF_BGR_PLL	6 LAYER ONLY; TP ONLY
CPU_LIMIT_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_PLL_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_CORE_HF_CLKOUT_DN	6 LAYER ONLY; TP ONLY
CPU_CORE_HF_CLKOUT_DP	6 LAYER ONLY; TP ONLY
CPU_EXT_CLK_EN	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_DLL_SNIF_OUT	6 LAYER ONLY; TP ONLY
CPU_VDDS0_DP	6 LAYER ONLY
CPU_VDDS0_DN	6 LAYER ONLY
CPU_VDDS1_DP	6 LAYER ONLY
CPU_VDDS1_DN	6 LAYER ONLY
RESISTOR0_DP	6 LAYER ONLY
RESISTOR0_DN	6 LAYER ONLY
EDRAM_PSRO_DOUT	6 LAYER ONLY

[PAGE_TITLE=GCPU SETUP]

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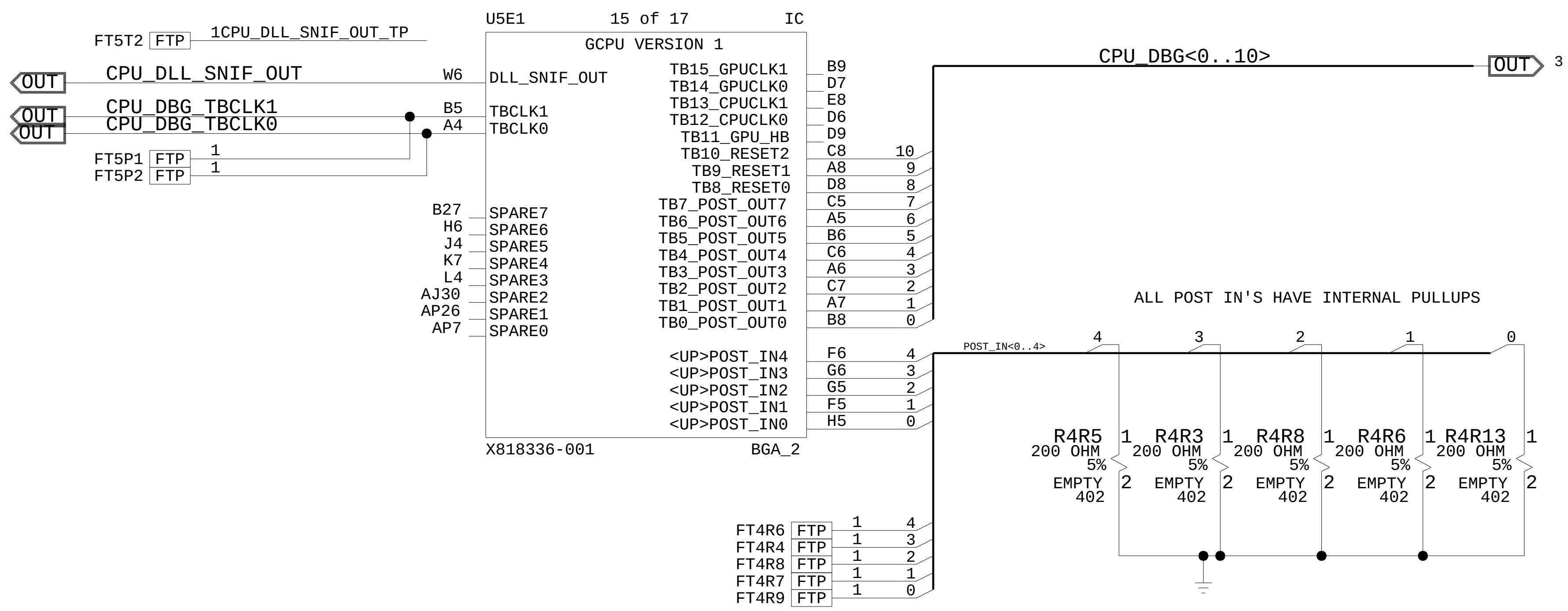
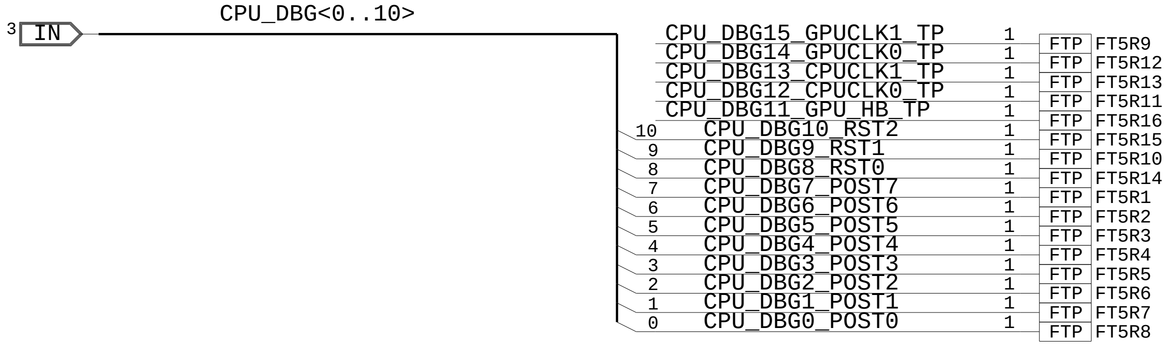
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	2/81	G	1.01

GCPU, DEBUG BUS


U5E1
15 of 17
IC
GCPU VERSION 1
X818336-001
BGA_2
FT5T2 FTP 1CPU_DLL_SNIF_OUT_TP
OUT CPU_DLL_SNIF_OUT W6 DLL_SNIF_OUT
OUT CPU_DBG_TBCLK1 B5 TBCLK1
OUT CPU_DBG_TBCLK0 A4 TBCLK0
FT5P1 FTP 1
FT5P2 FTP 1
B27 SPARE7
H6 SPARE6
J4 SPARE5
K7 SPARE4
L4 SPARE3
AJ30 SPARE2
AP26 SPARE1
AP7 SPARE0
TB15_GPUCLK1 B9
TB14_GPUCLK0 D7
TB13_CPUCLK1 E8
TB12_CPUCLK0 D6
TB11_GPU_HB D9
TB10_RESET2 C8 10
TB9_RESET1 A8 9
TB8_RESET0 D8 8
TB7_POST_OUT7 C5 7
TB6_POST_OUT6 A5 6
TB5_POST_OUT5 B6 5
TB4_POST_OUT4 C6 4
TB3_POST_OUT3 A6 3
TB2_POST_OUT2 C7 2
TB1_POST_OUT1 A7 1
TB0_POST_OUT0 B8 0
CPU_DBG<0..10>
OUT 3
<UP>POST_IN4 F6 4
<UP>POST_IN3 G6 3
<UP>POST_IN2 G5 2
<UP>POST_IN1 F5 1
<UP>POST_IN0 H5 0
POST_IN<0..4>
ALL POST IN'S HAVE INTERNAL PULLUPS
4 3 2 1 0
R4R5 1 200 OHM 5% EMPTY 402 2
R4R3 1 200 OHM 5% EMPTY 402 2
R4R8 1 200 OHM 5% EMPTY 402 2
R4R6 1 200 OHM 5% EMPTY 402 2
R4R13 1 200 OHM 5% EMPTY 402 2
FT4R6 FTP 1 4
FT4R4 FTP 1 3
FT4R8 FTP 1 2
FT4R7 FTP 1 1
FT4R9 FTP 1 0


3 IN
CPU_DBG<0..10>
CPU_DBG15_GPUCLK1_TP 1 FTP FT5R9
CPU_DBG14_GPUCLK0_TP 1 FTP FT5R12
CPU_DBG13_CPUCLK1_TP 1 FTP FT5R13
CPU_DBG12_CPUCLK0_TP 1 FTP FT5R11
CPU_DBG11_GPU_HB_TP 1 FTP FT5R16
10 CPU_DBG10_RST2 1 FTP FT5R15
9 CPU_DBG9_RST1 1 FTP FT5R10
8 CPU_DBG8_RST0 1 FTP FT5R14
7 CPU_DBG7_POST7 1 FTP FT5R1
6 CPU_DBG6_POST6 1 FTP FT5R2
5 CPU_DBG5_POST5 1 FTP FT5R3
4 CPU_DBG4_POST4 1 FTP FT5R4
3 CPU_DBG3_POST3 1 FTP FT5R5
2 CPU_DBG2_POST2 1 FTP FT5R6
1 CPU_DBG1_POST1 1 FTP FT5R7
0 CPU_DBG0_POST0 1 FTP FT5R8

[PAGE_TITLE=GCPU, DEBUG BUS]

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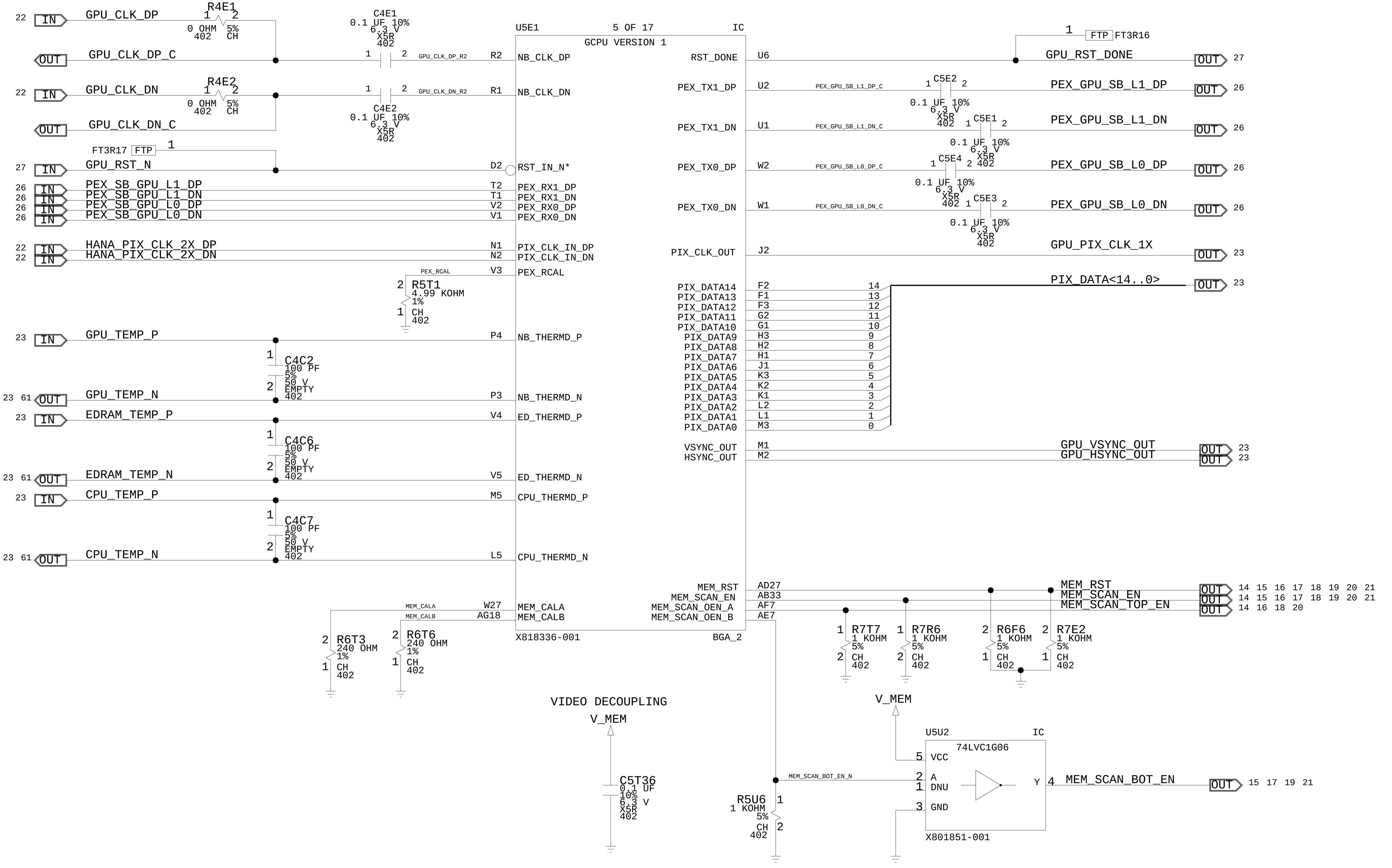
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	3/81	G	1.01

GCPU, VIDEO + PCIEX



22 IN GPU_CLK_DP
R4E1 1 2 0 OHM 5% 402 CH
OUT GPU_CLK_DP_C
22 IN GPU_CLK_DN
R4E2 1 2 0 OHM 5% 402 CH
OUT GPU_CLK_DN_C
C4E1 0.1 UF 10% 6.3 V X5R 402
C4E2 0.1 UF 10% 6.3 V X5R 402
GPU_CLK_DP_R2
GPU_CLK_DN_R2
FT3R17 FTP 1
27 IN GPU_RST_N
26 IN PEX_SB_GPU_L1_DP
26 IN PEX_SB_GPU_L1_DN
26 IN PEX_SB_GPU_L0_DP
26 IN PEX_SB_GPU_L0_DN
22 IN HANA_PIX_CLK_2X_DP
22 IN HANA_PIX_CLK_2X_DN
PEX_RCAL
R5T1 4.99 KOHM 1% CH 402
23 IN GPU_TEMP_P
C4C2 100 PF 5% 50 V EMPTY 402
23 61 OUT GPU_TEMP_N
23 IN EDRAM_TEMP_P
C4C6 100 PF 5% 50 V EMPTY 402
23 61 OUT EDRAM_TEMP_N
23 IN CPU_TEMP_P
C4C7 100 PF 5% 50 V EMPTY 402
23 61 OUT CPU_TEMP_N
MEM_CALA
MEM_CALB
R6T3 240 OHM 1% CH 402
R6T6 240 OHM 1% CH 402
U5E1 5 OF 17 IC
GCPU VERSION 1
R2 NB_CLK_DP
R1 NB_CLK_DN
D2 RST_IN_N*
T2 PEX_RX1_DP
T1 PEX_RX1_DN
V2 PEX_RX0_DP
V1 PEX_RX0_DN
N1 PIX_CLK_IN_DP
N2 PIX_CLK_IN_DN
V3 PEX_RCAL
P4 NB_THERMD_P
P3 NB_THERMD_N
V4 ED_THERMD_P
V5 ED_THERMD_N
M5 CPU_THERMD_P
L5 CPU_THERMD_N
W27 MEM_CALA
AG18 MEM_CALB
X818336-001
BGA_2
RST_DONE U6
PEX_TX1_DP U2
PEX_TX1_DN U1
PEX_TX0_DP W2
PEX_TX0_DN W1
PIX_CLK_OUT J2
PIX_DATA14 F2
PIX_DATA13 F1
PIX_DATA12 F3
PIX_DATA11 G2
PIX_DATA10 G1
PIX_DATA9 H3
PIX_DATA8 H2
PIX_DATA7 H1
PIX_DATA6 J1
PIX_DATA5 K3
PIX_DATA4 K2
PIX_DATA3 K1
PIX_DATA2 L2
PIX_DATA1 L1
PIX_DATA0 M3
VSYNC_OUT M1
HSYNC_OUT M2
MEM_RST AD27
MEM_SCAN_EN AB33
MEM_SCAN_OEN_A AF7
MEM_SCAN_OEN_B AE7
1 FTP FT3R16
GPU_RST_DONE OUT 27
PEX_GPU_SB_L1_DP_C
C5E2 0.1 UF 10% 6.3 V X5R 402
PEX_GPU_SB_L1_DP OUT 26
PEX_GPU_SB_L1_DN_C
C5E1 0.1 UF 10% 6.3 V X5R 402
PEX_GPU_SB_L1_DN OUT 26
PEX_GPU_SB_L0_DP_C
C5E4 0.1 UF 10% 6.3 V X5R 402
PEX_GPU_SB_L0_DP OUT 26
PEX_GPU_SB_L0_DN_C
C5E3 0.1 UF 10% 6.3 V X5R 402
PEX_GPU_SB_L0_DN OUT 26
GPU_PIX_CLK_1X OUT 23
PIX_DATA<14..0> OUT 23
14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
GPU_VSYNC_OUT OUT 23
GPU_HSYNC_OUT OUT 23
MEM_RST OUT 14 15 16 17 18 19 20 21
MEM_SCAN_EN OUT 14 15 16 17 18 19 20 21
MEM_SCAN_TOP_EN OUT 14 16 18 20
R7T7 1 KOHM 5% CH 402
R7R6 1 KOHM 5% CH 402
R6F6 1 KOHM 5% CH 402
R7E2 1 KOHM 5% CH 402
VIDEO DECOUPLING
V_MEM
C5T36 0.1 UF 10% 6.3 V X5R 402
MEM_SCAN_BOT_EN_N
R5U6 1 KOHM 5% CH 402
V_MEM
U5U2 IC
74LVC1G06
5 VCC
2 A
1 DNU
3 GND
Y 4
X801851-001
MEM_SCAN_BOT_EN OUT 15 17 19 21

[PAGE_TITLE=GCPU, VIDEO + PCIEX]

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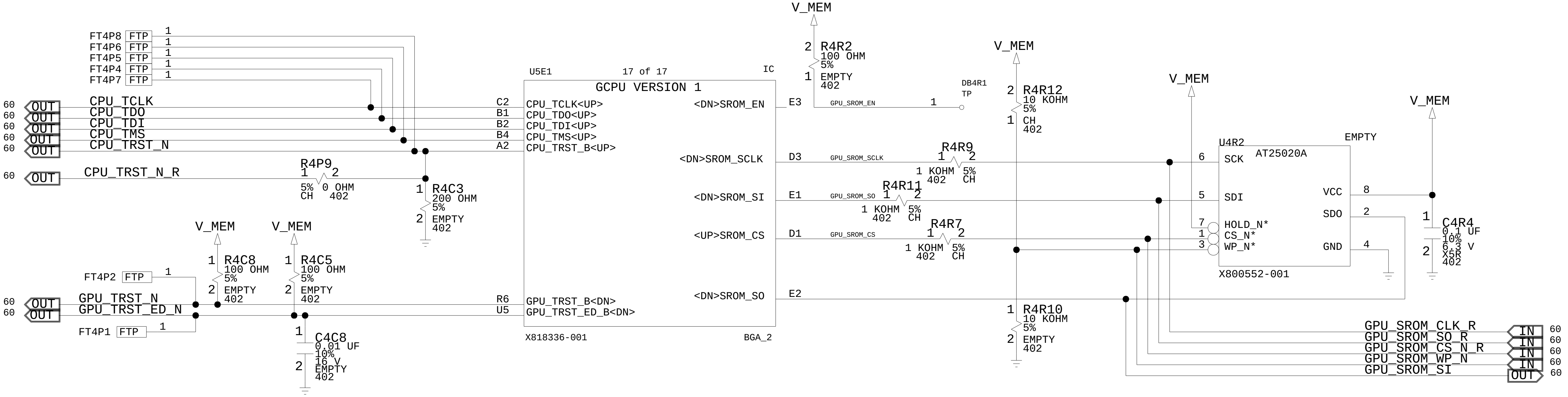
GCPU, EEPROM + JTAG


FT4P8 FTP 1
FT4P6 FTP 1
FT4P5 FTP 1
FT4P4 FTP 1
FT4P7 FTP 1
60 OUT CPU_TCLK
60 OUT CPU_TDO
60 OUT CPU_TDI
60 OUT CPU_TMS
60 OUT CPU_TRST_N
60 OUT CPU_TRST_N_R
R4P9 1 2 5% 0 OHM CH 402
R4C3 1 2 200 OHM 5% EMPTY 402
V_MEM
R4C8 1 2 100 OHM 5% EMPTY 402
V_MEM
R4C5 1 2 100 OHM 5% EMPTY 402
FT4P2 FTP 1
60 OUT GPU_TRST_N
60 OUT GPU_TRST_ED_N
FT4P1 FTP 1
C4C8 1 2 0.01 UF 10% 16 V EMPTY 402
U5E1
17 of 17
IC
GCPU VERSION 1
C2 CPU_TCLK<UP>
B1 CPU_TDO<UP>
B2 CPU_TDI<UP>
B4 CPU_TMS<UP>
A2 CPU_TRST_B<UP>
R6 GPU_TRST_B<DN>
U5 GPU_TRST_ED_B<DN>
X818336-001
BGA_2
<DN>SROM_EN E3
<DN>SROM_SCLK D3
<DN>SROM_SI E1
<UP>SROM_CS D1
<DN>SROM_SO E2
V_MEM
R4R2 2 1 100 OHM 5% EMPTY 402
GPU_SROM_EN
DB4R1 TP 1
V_MEM
R4R12 2 1 10 KOHM 5% CH 402
GPU_SROM_SCLK
R4R9 1 2 1 KOHM 5% 402 CH
GPU_SROM_SO
R4R11 1 2 1 KOHM 5% 402 CH
GPU_SROM_CS
R4R7 1 2 1 KOHM 5% 402 CH
R4R10 1 2 10 KOHM 5% EMPTY 402
V_MEM
U4R2
AT25020A
EMPTY
6 SCK
5 SDI
7 HOLD_N*
1 CS_N*
3 WP_N*
8 VCC
2 SDO
4 GND
X800552-001
V_MEM
C4R4 1 2 0.1 UF 10% 6.3 V X5R 402
GPU_SROM_CLK_R IN 60
GPU_SROM_SO_R IN 60
GPU_SROM_CS_N_R IN 60
GPU_SROM_WP_N IN 60
GPU_SROM_SI OUT 60

[PAGE_TITLE=GCPU, EEPROM + JTAG]

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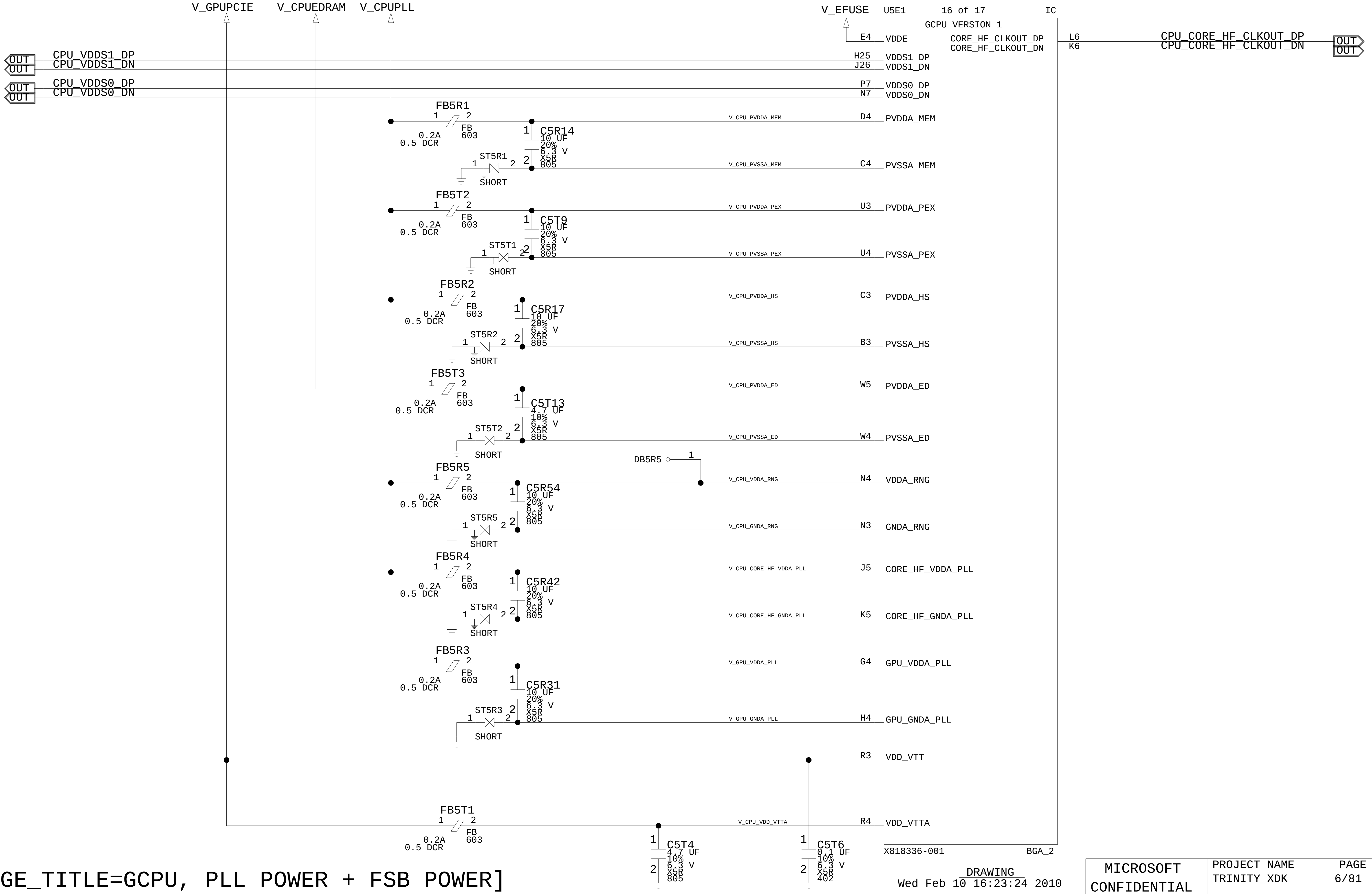
GCPU, PLL POWER + FSB POWER


V_GPUPCIE
V_CPUEDRAM
V_CPUPLL
V_EFUSE
U5E1
16 of 17
IC
GCPU VERSION 1
E4 VDDE
CORE_HF_CLKOUT_DP
CORE_HF_CLKOUT_DN
L6
K6
CPU_CORE_HF_CLKOUT_DP
CPU_CORE_HF_CLKOUT_DN
OUT
OUT
CPU_VDDS1_DP
CPU_VDDS1_DN
H25 VDDS1_DP
J26 VDDS1_DN
CPU_VDDS0_DP
CPU_VDDS0_DN
P7 VDDS0_DP
N7 VDDS0_DN
FB5R1
FB 603
0.2A 0.5 DCR
C5R14 10 UF 20% 6.3 V X5R 805
ST5R1 SHORT
V_CPU_PVDDA_MEM
D4 PVDDA_MEM
V_CPU_PVSSA_MEM
C4 PVSSA_MEM
FB5T2
C5T9 10 UF 20% 6.3 V X5R 805
ST5T1 SHORT
V_CPU_PVDDA_PEX
U3 PVDDA_PEX
V_CPU_PVSSA_PEX
U4 PVSSA_PEX
FB5R2
C5R17 10 UF 20% 6.3 V X5R 805
ST5R2 SHORT
V_CPU_PVDDA_HS
C3 PVDDA_HS
V_CPU_PVSSA_HS
B3 PVSSA_HS
FB5T3
C5T13 4.7 UF 10% 6.3 V X5R 805
ST5T2 SHORT
V_CPU_PVDDA_ED
W5 PVDDA_ED
V_CPU_PVSSA_ED
W4 PVSSA_ED
DB5R5
FB5R5
C5R54 10 UF 20% 6.3 V X5R 805
ST5R5 SHORT
V_CPU_VDDA_RNG
N4 VDDA_RNG
V_CPU_GNDA_RNG
N3 GNDA_RNG
FB5R4
C5R42 10 UF 20% 6.3 V X5R 805
ST5R4 SHORT
V_CPU_CORE_HF_VDDA_PLL
J5 CORE_HF_VDDA_PLL
V_CPU_CORE_HF_GNDA_PLL
K5 CORE_HF_GNDA_PLL
FB5R3
C5R31 10 UF 20% 6.3 V X5R 805
ST5R3 SHORT
V_GPU_VDDA_PLL
G4 GPU_VDDA_PLL
V_GPU_GNDA_PLL
H4 GPU_GNDA_PLL
R3 VDD_VTT
FB5T1
V_CPU_VDD_VTTA
R4 VDD_VTTA
C5T4 4.7 UF 10% 6.3 V X5R 805
C5T6 0.1 UF 10% 6.3 V X5R 402
X818336-001
BGA_2

[PAGE_TITLE=GCPU, PLL POWER + FSB POWER]

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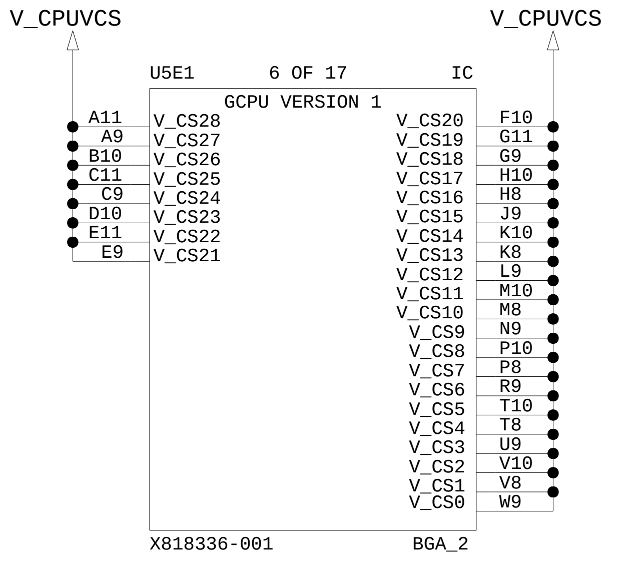
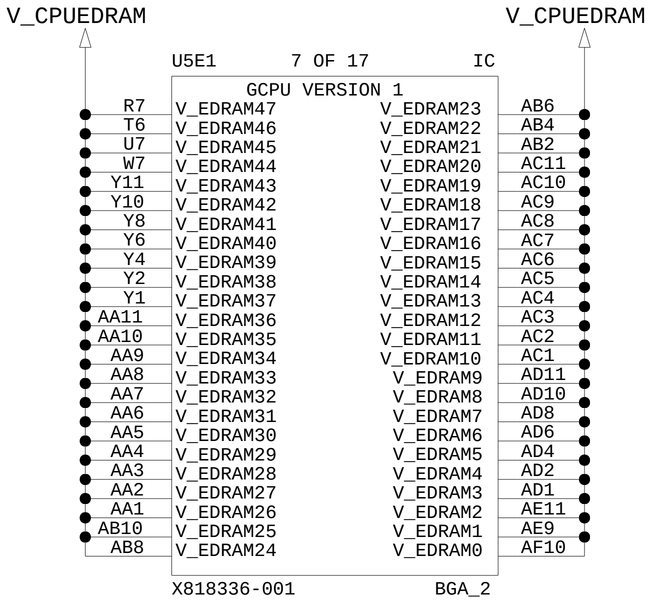
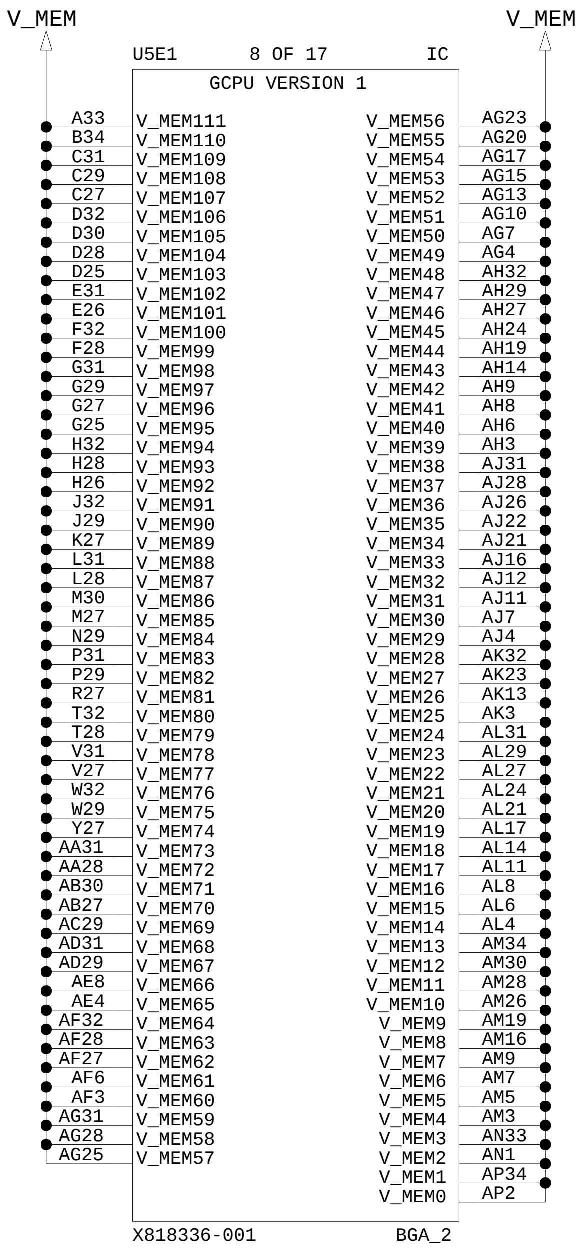
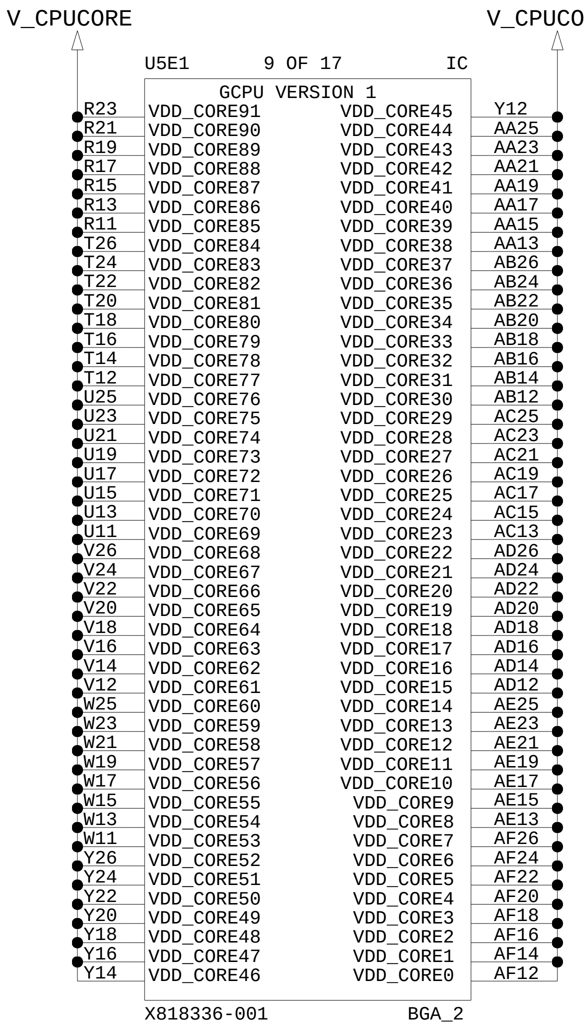
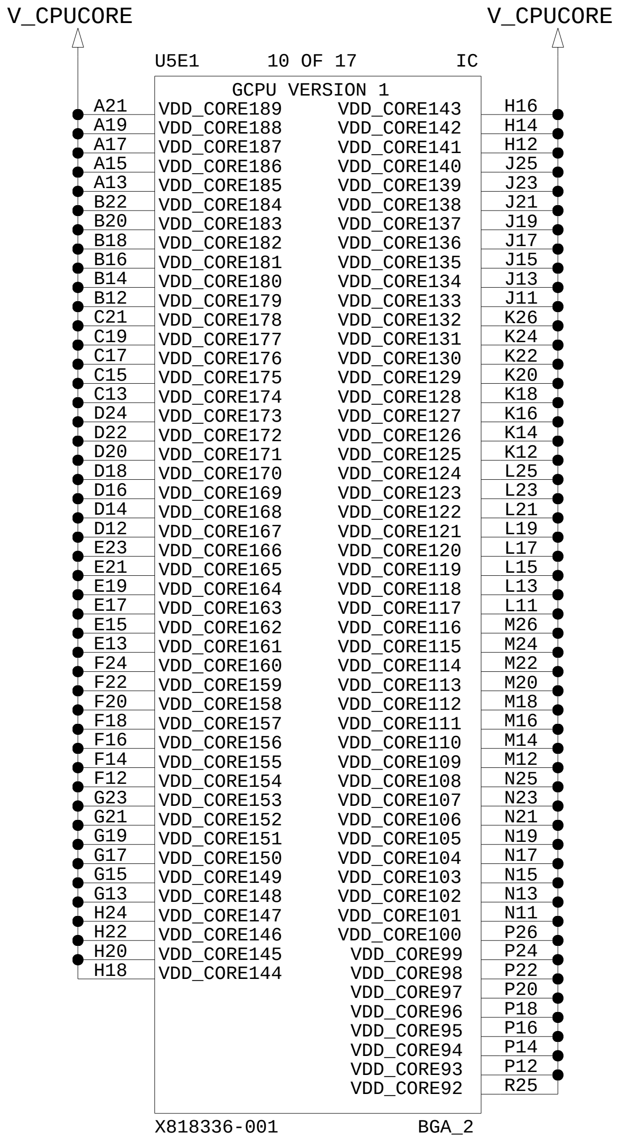
GCPU, POWER


V_CPUVCS
V_CPUVCS
U5E1
6 OF 17
IC
GCPU VERSION 1
A11 V_CS28
A9 V_CS27
B10 V_CS26
C11 V_CS25
C9 V_CS24
D10 V_CS23
E11 V_CS22
E9 V_CS21
V_CS20 F10
V_CS19 G11
V_CS18 G9
V_CS17 H10
V_CS16 H8
V_CS15 J9
V_CS14 K10
V_CS13 K8
V_CS12 L9
V_CS11 M10
V_CS10 M8
V_CS9 N9
V_CS8 P10
V_CS7 P8
V_CS6 R9
V_CS5 T10
V_CS4 T8
V_CS3 U9
V_CS2 V10
V_CS1 V8
V_CS0 W9
X818336-001
BGA_2


V_CPUEDRAM
V_CPUEDRAM
U5E1
7 OF 17
IC
GCPU VERSION 1
R7 V_EDRAM47
T6 V_EDRAM46
U7 V_EDRAM45
W7 V_EDRAM44
Y11 V_EDRAM43
Y10 V_EDRAM42
Y8 V_EDRAM41
Y6 V_EDRAM40
Y4 V_EDRAM39
Y2 V_EDRAM38
Y1 V_EDRAM37
AA11 V_EDRAM36
AA10 V_EDRAM35
AA9 V_EDRAM34
AA8 V_EDRAM33
AA7 V_EDRAM32
AA6 V_EDRAM31
AA5 V_EDRAM30
AA4 V_EDRAM29
AA3 V_EDRAM28
AA2 V_EDRAM27
AA1 V_EDRAM26
AB10 V_EDRAM25
AB8 V_EDRAM24
V_EDRAM23 AB6
V_EDRAM22 AB4
V_EDRAM21 AB2
V_EDRAM20 AC11
V_EDRAM19 AC10
V_EDRAM18 AC9
V_EDRAM17 AC8
V_EDRAM16 AC7
V_EDRAM15 AC6
V_EDRAM14 AC5
V_EDRAM13 AC4
V_EDRAM12 AC3
V_EDRAM11 AC2
V_EDRAM10 AC1
V_EDRAM9 AD11
V_EDRAM8 AD10
V_EDRAM7 AD8
V_EDRAM6 AD6
V_EDRAM5 AD4
V_EDRAM4 AD2
V_EDRAM3 AD1
V_EDRAM2 AE11
V_EDRAM1 AE9
V_EDRAM0 AF10
X818336-001
BGA_2


V_MEM
V_MEM
U5E1
8 OF 17
IC
GCPU VERSION 1
A33 V_MEM111
B34 V_MEM110
C31 V_MEM109
C29 V_MEM108
C27 V_MEM107
D32 V_MEM106
D30 V_MEM105
D28 V_MEM104
D25 V_MEM103
E31 V_MEM102
E26 V_MEM101
F32 V_MEM100
F28 V_MEM99
G31 V_MEM98
G29 V_MEM97
G27 V_MEM96
G25 V_MEM95
H32 V_MEM94
H28 V_MEM93
H26 V_MEM92
J32 V_MEM91
J29 V_MEM90
K27 V_MEM89
L31 V_MEM88
L28 V_MEM87
M30 V_MEM86
M27 V_MEM85
N29 V_MEM84
P31 V_MEM83
P29 V_MEM82
R27 V_MEM81
T32 V_MEM80
T28 V_MEM79
V31 V_MEM78
V27 V_MEM77
W32 V_MEM76
W29 V_MEM75
Y27 V_MEM74
AA31 V_MEM73
AA28 V_MEM72
AB30 V_MEM71
AB27 V_MEM70
AC29 V_MEM69
AD31 V_MEM68
AD29 V_MEM67
AE8 V_MEM66
AE4 V_MEM65
AF32 V_MEM64
AF28 V_MEM63
AF27 V_MEM62
AF6 V_MEM61
AF3 V_MEM60
AG31 V_MEM59
AG28 V_MEM58
AG25 V_MEM57
V_MEM56 AG23
V_MEM55 AG20
V_MEM54 AG17
V_MEM53 AG15
V_MEM52 AG13
V_MEM51 AG10
V_MEM50 AG7
V_MEM49 AG4
V_MEM48 AH32
V_MEM47 AH29
V_MEM46 AH27
V_MEM45 AH24
V_MEM44 AH19
V_MEM43 AH14
V_MEM42 AH9
V_MEM41 AH8
V_MEM40 AH6
V_MEM39 AH3
V_MEM38 AJ31
V_MEM37 AJ28
V_MEM36 AJ26
V_MEM35 AJ22
V_MEM34 AJ21
V_MEM33 AJ16
V_MEM32 AJ12
V_MEM31 AJ11
V_MEM30 AJ7
V_MEM29 AJ4
V_MEM28 AK32
V_MEM27 AK23
V_MEM26 AK13
V_MEM25 AK3
V_MEM24 AL31
V_MEM23 AL29
V_MEM22 AL27
V_MEM21 AL24
V_MEM20 AL21
V_MEM19 AL17
V_MEM18 AL14
V_MEM17 AL11
V_MEM16 AL8
V_MEM15 AL6
V_MEM14 AL4
V_MEM13 AM34
V_MEM12 AM30
V_MEM11 AM28
V_MEM10 AM26
V_MEM9 AM19
V_MEM8 AM16
V_MEM7 AM9
V_MEM6 AM7
V_MEM5 AM5
V_MEM4 AM3
V_MEM3 AN33
V_MEM2 AN1
V_MEM1 AP34
V_MEM0 AP2
X818336-001
BGA_2


V_CPUCORE
V_CPUCORE
U5E1
9 OF 17
IC
GCPU VERSION 1
R23 VDD_CORE91
R21 VDD_CORE90
R19 VDD_CORE89
R17 VDD_CORE88
R15 VDD_CORE87
R13 VDD_CORE86
R11 VDD_CORE85
T26 VDD_CORE84
T24 VDD_CORE83
T22 VDD_CORE82
T20 VDD_CORE81
T18 VDD_CORE80
T16 VDD_CORE79
T14 VDD_CORE78
T12 VDD_CORE77
U25 VDD_CORE76
U23 VDD_CORE75
U21 VDD_CORE74
U19 VDD_CORE73
U17 VDD_CORE72
U15 VDD_CORE71
U13 VDD_CORE70
U11 VDD_CORE69
V26 VDD_CORE68
V24 VDD_CORE67
V22 VDD_CORE66
V20 VDD_CORE65
V18 VDD_CORE64
V16 VDD_CORE63
V14 VDD_CORE62
V12 VDD_CORE61
W25 VDD_CORE60
W23 VDD_CORE59
W21 VDD_CORE58
W19 VDD_CORE57
W17 VDD_CORE56
W15 VDD_CORE55
W13 VDD_CORE54
W11 VDD_CORE53
Y26 VDD_CORE52
Y24 VDD_CORE51
Y22 VDD_CORE50
Y20 VDD_CORE49
Y18 VDD_CORE48
Y16 VDD_CORE47
Y14 VDD_CORE46
VDD_CORE45 Y12
VDD_CORE44 AA25
VDD_CORE43 AA23
VDD_CORE42 AA21
VDD_CORE41 AA19
VDD_CORE40 AA17
VDD_CORE39 AA15
VDD_CORE38 AA13
VDD_CORE37 AB26
VDD_CORE36 AB24
VDD_CORE35 AB22
VDD_CORE34 AB20
VDD_CORE33 AB18
VDD_CORE32 AB16
VDD_CORE31 AB14
VDD_CORE30 AB12
VDD_CORE29 AC25
VDD_CORE28 AC23
VDD_CORE27 AC21
VDD_CORE26 AC19
VDD_CORE25 AC17
VDD_CORE24 AC15
VDD_CORE23 AC13
VDD_CORE22 AD26
VDD_CORE21 AD24
VDD_CORE20 AD22
VDD_CORE19 AD20
VDD_CORE18 AD18
VDD_CORE17 AD16
VDD_CORE16 AD14
VDD_CORE15 AD12
VDD_CORE14 AE25
VDD_CORE13 AE23
VDD_CORE12 AE21
VDD_CORE11 AE19
VDD_CORE10 AE17
VDD_CORE9 AE15
VDD_CORE8 AE13
VDD_CORE7 AF26
VDD_CORE6 AF24
VDD_CORE5 AF22
VDD_CORE4 AF20
VDD_CORE3 AF18
VDD_CORE2 AF16
VDD_CORE1 AF14
VDD_CORE0 AF12
X818336-001
BGA_2


V_CPUCORE
V_CPUCORE
U5E1
10 OF 17
IC
GCPU VERSION 1
A21 VDD_CORE189
A19 VDD_CORE188
A17 VDD_CORE187
A15 VDD_CORE186
A13 VDD_CORE185
B22 VDD_CORE184
B20 VDD_CORE183
B18 VDD_CORE182
B16 VDD_CORE181
B14 VDD_CORE180
B12 VDD_CORE179
C21 VDD_CORE178
C19 VDD_CORE177
C17 VDD_CORE176
C15 VDD_CORE175
C13 VDD_CORE174
D24 VDD_CORE173
D22 VDD_CORE172
D20 VDD_CORE171
D18 VDD_CORE170
D16 VDD_CORE169
D14 VDD_CORE168
D12 VDD_CORE167
E23 VDD_CORE166
E21 VDD_CORE165
E19 VDD_CORE164
E17 VDD_CORE163
E15 VDD_CORE162
E13 VDD_CORE161
F24 VDD_CORE160
F22 VDD_CORE159
F20 VDD_CORE158
F18 VDD_CORE157
F16 VDD_CORE156
F14 VDD_CORE155
F12 VDD_CORE154
G23 VDD_CORE153
G21 VDD_CORE152
G19 VDD_CORE151
G17 VDD_CORE150
G15 VDD_CORE149
G13 VDD_CORE148
H24 VDD_CORE147
H22 VDD_CORE146
H20 VDD_CORE145
H18 VDD_CORE144
VDD_CORE143 H16
VDD_CORE142 H14
VDD_CORE141 H12
VDD_CORE140 J25
VDD_CORE139 J23
VDD_CORE138 J21
VDD_CORE137 J19
VDD_CORE136 J17
VDD_CORE135 J15
VDD_CORE134 J13
VDD_CORE133 J11
VDD_CORE132 K26
VDD_CORE131 K24
VDD_CORE130 K22
VDD_CORE129 K20
VDD_CORE128 K18
VDD_CORE127 K16
VDD_CORE126 K14
VDD_CORE125 K12
VDD_CORE124 L25
VDD_CORE123 L23
VDD_CORE122 L21
VDD_CORE121 L19
VDD_CORE120 L17
VDD_CORE119 L15
VDD_CORE118 L13
VDD_CORE117 L11
VDD_CORE116 M26
VDD_CORE115 M24
VDD_CORE114 M22
VDD_CORE113 M20
VDD_CORE112 M18
VDD_CORE111 M16
VDD_CORE110 M14
VDD_CORE109 M12
VDD_CORE108 N25
VDD_CORE107 N23
VDD_CORE106 N21
VDD_CORE105 N19
VDD_CORE104 N17
VDD_CORE103 N15
VDD_CORE102 N13
VDD_CORE101 N11
VDD_CORE100 P26
VDD_CORE99 P24
VDD_CORE98 P22
VDD_CORE97 P20
VDD_CORE96 P18
VDD_CORE95 P16
VDD_CORE94 P14
VDD_CORE93 P12
VDD_CORE92 R25
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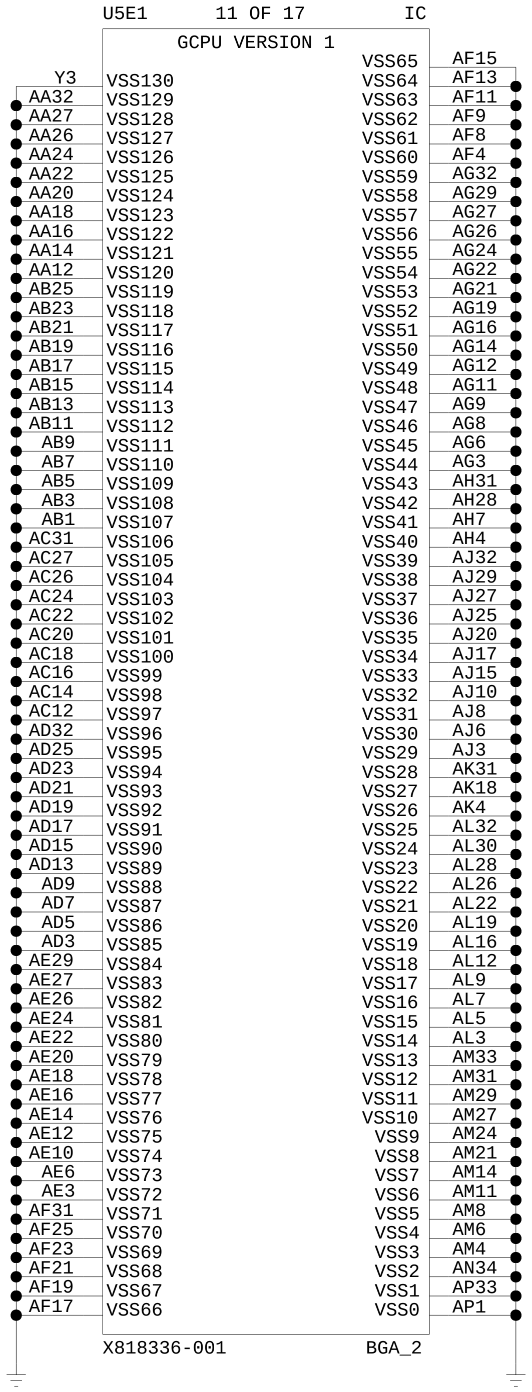
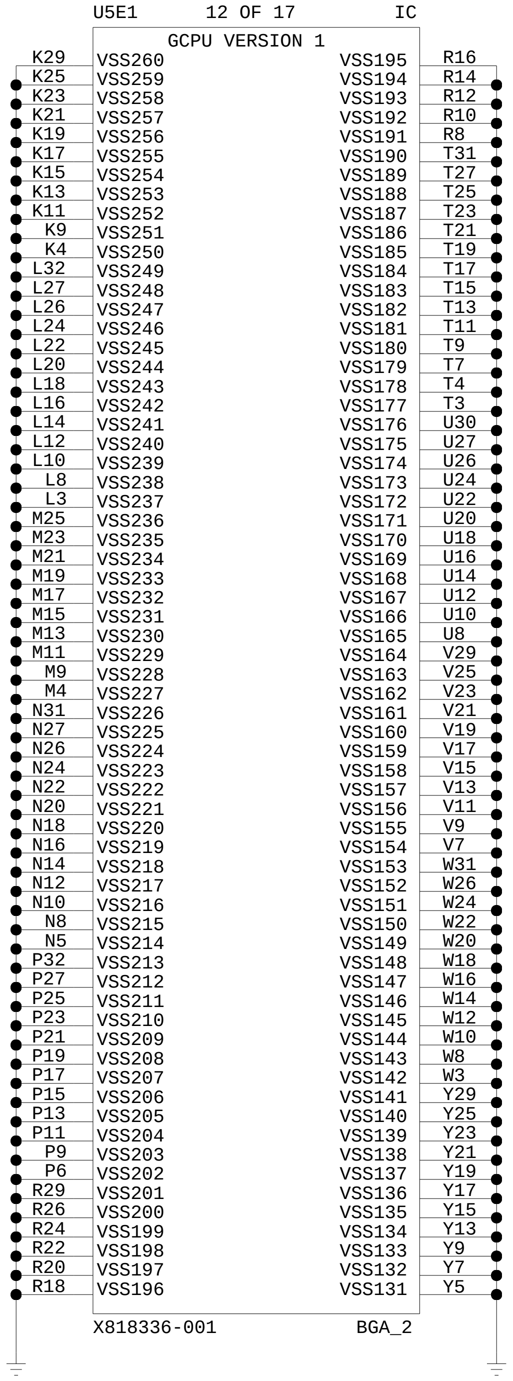
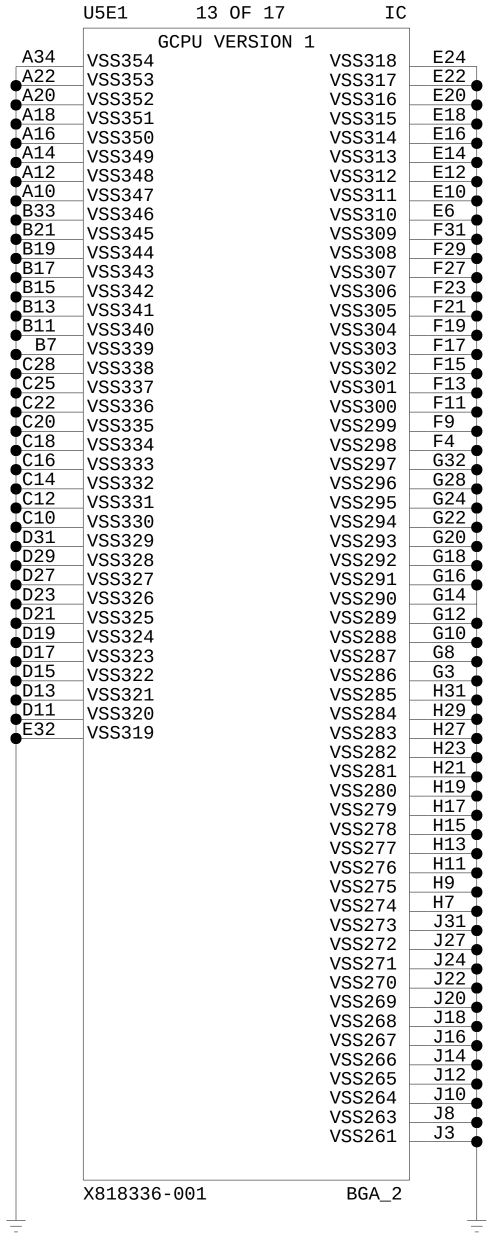
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	7/81	G	1.01

GCPU, POWER


U5E1
11 OF 17
IC
GCPU VERSION 1
Y3 VSS130
AA32 VSS129
AA27 VSS128
AA26 VSS127
AA24 VSS126
AA22 VSS125
AA20 VSS124
AA18 VSS123
AA16 VSS122
AA14 VSS121
AA12 VSS120
AB25 VSS119
AB23 VSS118
AB21 VSS117
AB19 VSS116
AB17 VSS115
AB15 VSS114
AB13 VSS113
AB11 VSS112
AB9 VSS111
AB7 VSS110
AB5 VSS109
AB3 VSS108
AB1 VSS107
AC31 VSS106
AC27 VSS105
AC26 VSS104
AC24 VSS103
AC22 VSS102
AC20 VSS101
AC18 VSS100
AC16 VSS99
AC14 VSS98
AC12 VSS97
AD32 VSS96
AD25 VSS95
AD23 VSS94
AD21 VSS93
AD19 VSS92
AD17 VSS91
AD15 VSS90
AD13 VSS89
AD9 VSS88
AD7 VSS87
AD5 VSS86
AD3 VSS85
AE29 VSS84
AE27 VSS83
AE26 VSS82
AE24 VSS81
AE22 VSS80
AE20 VSS79
AE18 VSS78
AE16 VSS77
AE14 VSS76
AE12 VSS75
AE10 VSS74
AE6 VSS73
AE3 VSS72
AF31 VSS71
AF25 VSS70
AF23 VSS69
AF21 VSS68
AF19 VSS67
AF17 VSS66
VSS65 AF15
VSS64 AF13
VSS63 AF11
VSS62 AF9
VSS61 AF8
VSS60 AF4
VSS59 AG32
VSS58 AG29
VSS57 AG27
VSS56 AG26
VSS55 AG24
VSS54 AG22
VSS53 AG21
VSS52 AG19
VSS51 AG16
VSS50 AG14
VSS49 AG12
VSS48 AG11
VSS47 AG9
VSS46 AG8
VSS45 AG6
VSS44 AG3
VSS43 AH31
VSS42 AH28
VSS41 AH7
VSS40 AH4
VSS39 AJ32
VSS38 AJ29
VSS37 AJ27
VSS36 AJ25
VSS35 AJ20
VSS34 AJ17
VSS33 AJ15
VSS32 AJ10
VSS31 AJ8
VSS30 AJ6
VSS29 AJ3
VSS28 AK31
VSS27 AK18
VSS26 AK4
VSS25 AL32
VSS24 AL30
VSS23 AL28
VSS22 AL26
VSS21 AL22
VSS20 AL19
VSS19 AL16
VSS18 AL12
VSS17 AL9
VSS16 AL7
VSS15 AL5
VSS14 AL3
VSS13 AM33
VSS12 AM31
VSS11 AM29
VSS10 AM27
VSS9 AM24
VSS8 AM21
VSS7 AM14
VSS6 AM11
VSS5 AM8
VSS4 AM6
VSS3 AM4
VSS2 AN34
VSS1 AP33
VSS0 AP1
X818336-001
BGA_2


U5E1
12 OF 17
IC
GCPU VERSION 1
K29 VSS260
K25 VSS259
K23 VSS258
K21 VSS257
K19 VSS256
K17 VSS255
K15 VSS254
K13 VSS253
K11 VSS252
K9 VSS251
K4 VSS250
L32 VSS249
L27 VSS248
L26 VSS247
L24 VSS246
L22 VSS245
L20 VSS244
L18 VSS243
L16 VSS242
L14 VSS241
L12 VSS240
L10 VSS239
L8 VSS238
L3 VSS237
M25 VSS236
M23 VSS235
M21 VSS234
M19 VSS233
M17 VSS232
M15 VSS231
M13 VSS230
M11 VSS229
M9 VSS228
M4 VSS227
N31 VSS226
N27 VSS225
N26 VSS224
N24 VSS223
N22 VSS222
N20 VSS221
N18 VSS220
N16 VSS219
N14 VSS218
N12 VSS217
N10 VSS216
N8 VSS215
N5 VSS214
P32 VSS213
P27 VSS212
P25 VSS211
P23 VSS210
P21 VSS209
P19 VSS208
P17 VSS207
P15 VSS206
P13 VSS205
P11 VSS204
P9 VSS203
P6 VSS202
R29 VSS201
R26 VSS200
R24 VSS199
R22 VSS198
R20 VSS197
R18 VSS196
VSS195 R16
VSS194 R14
VSS193 R12
VSS192 R10
VSS191 R8
VSS190 T31
VSS189 T27
VSS188 T25
VSS187 T23
VSS186 T21
VSS185 T19
VSS184 T17
VSS183 T15
VSS182 T13
VSS181 T11
VSS180 T9
VSS179 T7
VSS178 T4
VSS177 T3
VSS176 U30
VSS175 U27
VSS174 U26
VSS173 U24
VSS172 U22
VSS171 U20
VSS170 U18
VSS169 U16
VSS168 U14
VSS167 U12
VSS166 U10
VSS165 U8
VSS164 V29
VSS163 V25
VSS162 V23
VSS161 V21
VSS160 V19
VSS159 V17
VSS158 V15
VSS157 V13
VSS156 V11
VSS155 V9
VSS154 V7
VSS153 W31
VSS152 W26
VSS151 W24
VSS150 W22
VSS149 W20
VSS148 W18
VSS147 W16
VSS146 W14
VSS145 W12
VSS144 W10
VSS143 W8
VSS142 W3
VSS141 Y29
VSS140 Y25
VSS139 Y23
VSS138 Y21
VSS137 Y19
VSS136 Y17
VSS135 Y15
VSS134 Y13
VSS133 Y9
VSS132 Y7
VSS131 Y5
X818336-001
BGA_2


U5E1
13 OF 17
IC
GCPU VERSION 1
A34 VSS354
A22 VSS353
A20 VSS352
A18 VSS351
A16 VSS350
A14 VSS349
A12 VSS348
A10 VSS347
B33 VSS346
B21 VSS345
B19 VSS344
B17 VSS343
B15 VSS342
B13 VSS341
B11 VSS340
B7 VSS339
C28 VSS338
C25 VSS337
C22 VSS336
C20 VSS335
C18 VSS334
C16 VSS333
C14 VSS332
C12 VSS331
C10 VSS330
D31 VSS329
D29 VSS328
D27 VSS327
D23 VSS326
D21 VSS325
D19 VSS324
D17 VSS323
D15 VSS322
D13 VSS321
D11 VSS320
E32 VSS319
VSS318 E24
VSS317 E22
VSS316 E20
VSS315 E18
VSS314 E16
VSS313 E14
VSS312 E12
VSS311 E10
VSS310 E6
VSS309 F31
VSS308 F29
VSS307 F27
VSS306 F23
VSS305 F21
VSS304 F19
VSS303 F17
VSS302 F15
VSS301 F13
VSS300 F11
VSS299 F9
VSS298 F4
VSS297 G32
VSS296 G28
VSS295 G24
VSS294 G22
VSS293 G20
VSS292 G18
VSS291 G16
VSS290 G14
VSS289 G12
VSS288 G10
VSS287 G8
VSS286 G3
VSS285 H31
VSS284 H29
VSS283 H27
VSS282 H23
VSS281 H21
VSS280 H19
VSS279 H17
VSS278 H15
VSS277 H13
VSS276 H11
VSS275 H9
VSS274 H7
VSS273 J31
VSS272 J27
VSS271 J24
VSS270 J22
VSS269 J20
VSS268 J18
VSS267 J16
VSS266 J14
VSS265 J12
VSS264 J10
VSS263 J8
VSS261 J3
X818336-001
BGA_2

[PAGE_TITLE=GCPU, POWER]

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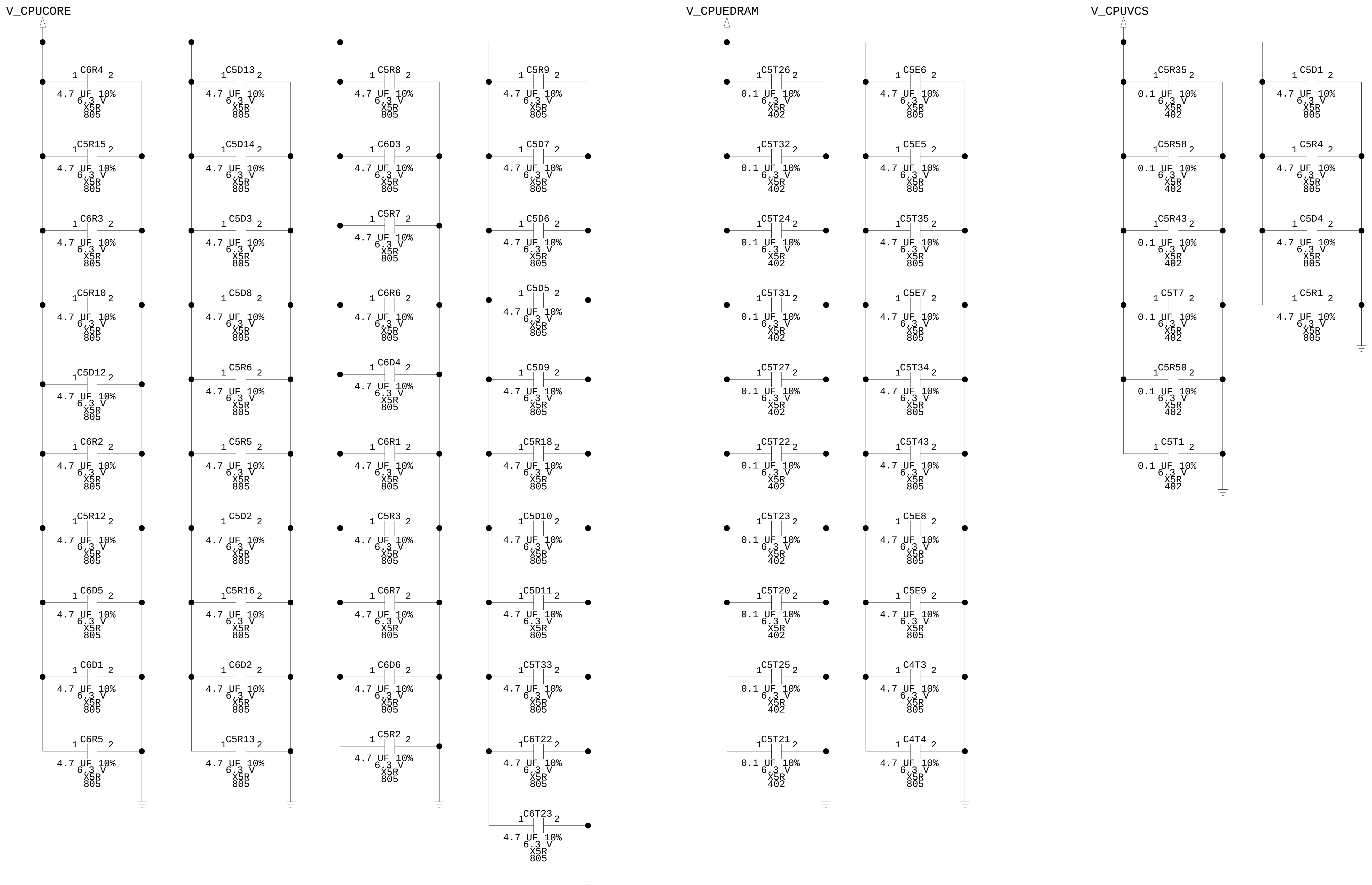
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	8/81	G	1.01

GCPU, DECOUPLING


V_CPUCORE
1 C6R4 2
4.7 UF 10% 6.3 V X5R 805
1 C5R15 2
4.7 UF 10% 6.3 V X5R 805
1 C6R3 2
4.7 UF 10% 6.3 V X5R 805
1 C5R10 2
4.7 UF 10% 6.3 V X5R 805
1 C5D12 2
4.7 UF 10% 6.3 V X5R 805
1 C6R2 2
4.7 UF 10% 6.3 V X5R 805
1 C5R12 2
4.7 UF 10% 6.3 V X5R 805
1 C6D5 2
4.7 UF 10% 6.3 V X5R 805
1 C6D1 2
4.7 UF 10% 6.3 V X5R 805
1 C6R5 2
4.7 UF 10% 6.3 V X5R 805
1 C5D13 2
4.7 UF 10% 6.3 V X5R 805
1 C5D14 2
4.7 UF 10% 6.3 V X5R 805
1 C5D3 2
4.7 UF 10% 6.3 V X5R 805
1 C5D8 2
4.7 UF 10% 6.3 V X5R 805
1 C5R6 2
4.7 UF 10% 6.3 V X5R 805
1 C5R5 2
4.7 UF 10% 6.3 V X5R 805
1 C5D2 2
4.7 UF 10% 6.3 V X5R 805
1 C5R16 2
4.7 UF 10% 6.3 V X5R 805
1 C6D2 2
4.7 UF 10% 6.3 V X5R 805
1 C5R13 2
4.7 UF 10% 6.3 V X5R 805
1 C5R8 2
4.7 UF 10% 6.3 V X5R 805
1 C6D3 2
4.7 UF 10% 6.3 V X5R 805
1 C5R7 2
4.7 UF 10% 6.3 V X5R 805
1 C6R6 2
4.7 UF 10% 6.3 V X5R 805
1 C6D4 2
4.7 UF 10% 6.3 V X5R 805
1 C6R1 2
4.7 UF 10% 6.3 V X5R 805
1 C5R3 2
4.7 UF 10% 6.3 V X5R 805
1 C6R7 2
4.7 UF 10% 6.3 V X5R 805
1 C6D6 2
4.7 UF 10% 6.3 V X5R 805
1 C5R2 2
4.7 UF 10% 6.3 V X5R 805
1 C5R9 2
4.7 UF 10% 6.3 V X5R 805
1 C5D7 2
4.7 UF 10% 6.3 V X5R 805
1 C5D6 2
4.7 UF 10% 6.3 V X5R 805
1 C5D5 2
4.7 UF 10% 6.3 V X5R 805
1 C5D9 2
4.7 UF 10% 6.3 V X5R 805
1 C5R18 2
4.7 UF 10% 6.3 V X5R 805
1 C5D10 2
4.7 UF 10% 6.3 V X5R 805
1 C5D11 2
4.7 UF 10% 6.3 V X5R 805
1 C5T33 2
4.7 UF 10% 6.3 V X5R 805
1 C6T22 2
4.7 UF 10% 6.3 V X5R 805
1 C6T23 2
4.7 UF 10% 6.3 V X5R 805
V_CPUEDRAM
1 C5T26 2
0.1 UF 10% 6.3 V X5R 402
1 C5T32 2
0.1 UF 10% 6.3 V X5R 402
1 C5T24 2
0.1 UF 10% 6.3 V X5R 402
1 C5T31 2
0.1 UF 10% 6.3 V X5R 402
1 C5T27 2
0.1 UF 10% 6.3 V X5R 402
1 C5T22 2
0.1 UF 10% 6.3 V X5R 402
1 C5T23 2
0.1 UF 10% 6.3 V X5R 402
1 C5T20 2
0.1 UF 10% 6.3 V X5R 402
1 C5T25 2
0.1 UF 10% 6.3 V X5R 402
1 C5T21 2
0.1 UF 10% 6.3 V X5R 402
1 C5E6 2
4.7 UF 10% 6.3 V X5R 805
1 C5E5 2
4.7 UF 10% 6.3 V X5R 805
1 C5T35 2
4.7 UF 10% 6.3 V X5R 805
1 C5E7 2
4.7 UF 10% 6.3 V X5R 805
1 C5T34 2
4.7 UF 10% 6.3 V X5R 805
1 C5T43 2
4.7 UF 10% 6.3 V X5R 805
1 C5E8 2
4.7 UF 10% 6.3 V X5R 805
1 C5E9 2
4.7 UF 10% 6.3 V X5R 805
1 C4T3 2
4.7 UF 10% 6.3 V X5R 805
1 C4T4 2
4.7 UF 10% 6.3 V X5R 805
V_CPUVCS
1 C5R35 2
0.1 UF 10% 6.3 V X5R 402
1 C5R58 2
0.1 UF 10% 6.3 V X5R 402
1 C5R43 2
0.1 UF 10% 6.3 V X5R 402
1 C5T7 2
0.1 UF 10% 6.3 V X5R 402
1 C5R50 2
0.1 UF 10% 6.3 V X5R 402
1 C5T1 2
0.1 UF 10% 6.3 V X5R 402
1 C5D1 2
4.7 UF 10% 6.3 V X5R 805
1 C5R4 2
4.7 UF 10% 6.3 V X5R 805
1 C5D4 2
4.7 UF 10% 6.3 V X5R 805
1 C5R1 2
4.7 UF 10% 6.3 V X5R 805

[PAGE_TITLE=GCPU, DECOUPLING]

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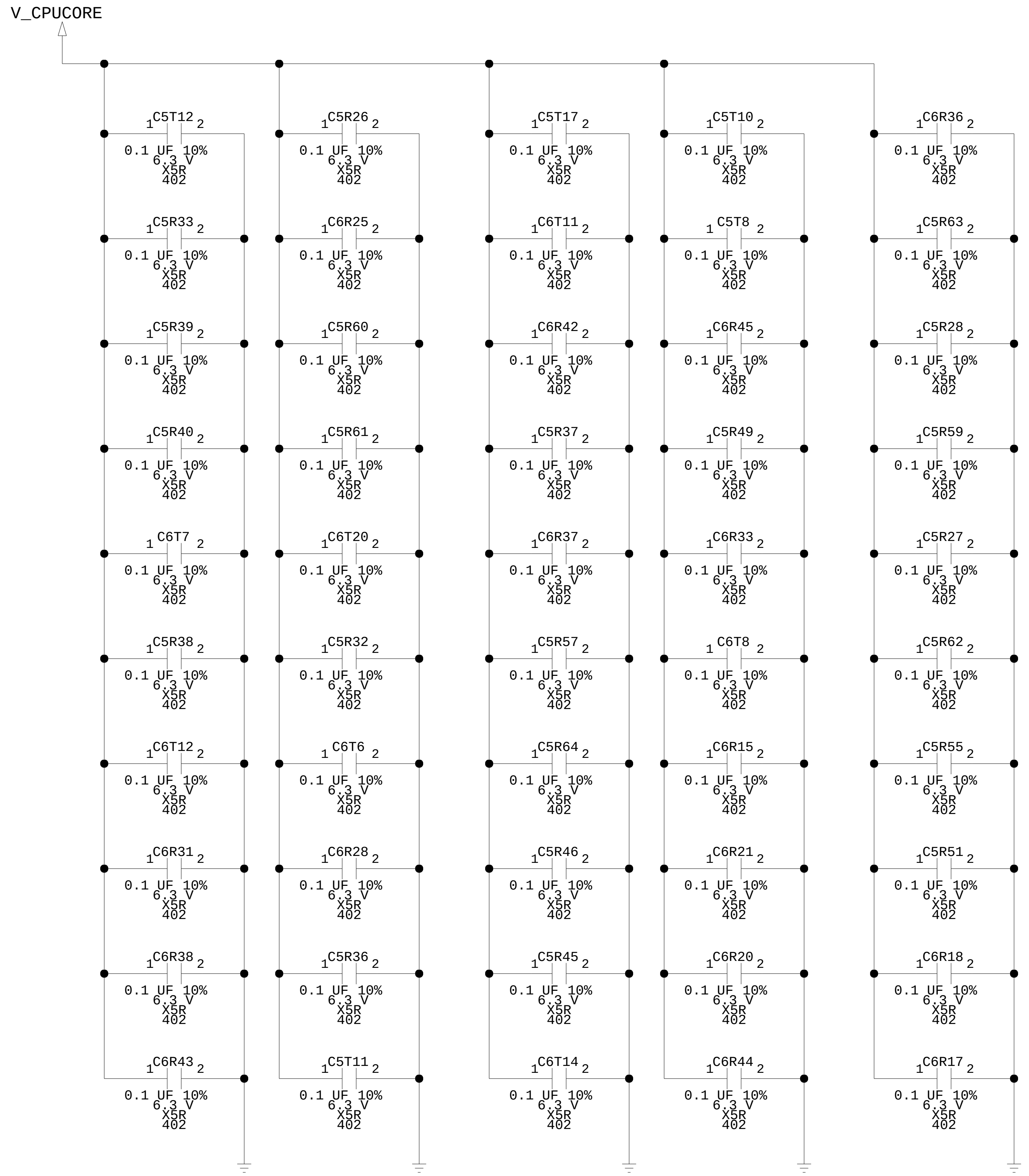
PROJECT NAME	PAGE	FAB	REV
TRINITY_XDK	9/81	G	1.01

GCPU, DECOUPLING


V_CPUCORE
C5T12
C5R33
C5R39
C5R40
C6T7
C5R38
C6T12
C6R31
C6R38
C6R43
C5R26
C6R25
C5R60
C5R61
C6T20
C5R32
C6T6
C6R28
C5R36
C5T11
C5T17
C6T11
C6R42
C5R37
C6R37
C5R57
C5R64
C5R46
C5R45
C6T14
C5T10
C5T8
C6R45
C5R49
C6R33
C6T8
C6R15
C6R21
C6R20
C6R44
C6R36
C5R63
C5R28
C5R59
C5R27
C5R62
C5R55
C5R51
C6R18
C6R17
1
2
0.1 UF 10%
6.3 V
X5R
402

[PAGE_TITLE=GCPU, DECOUPLING]

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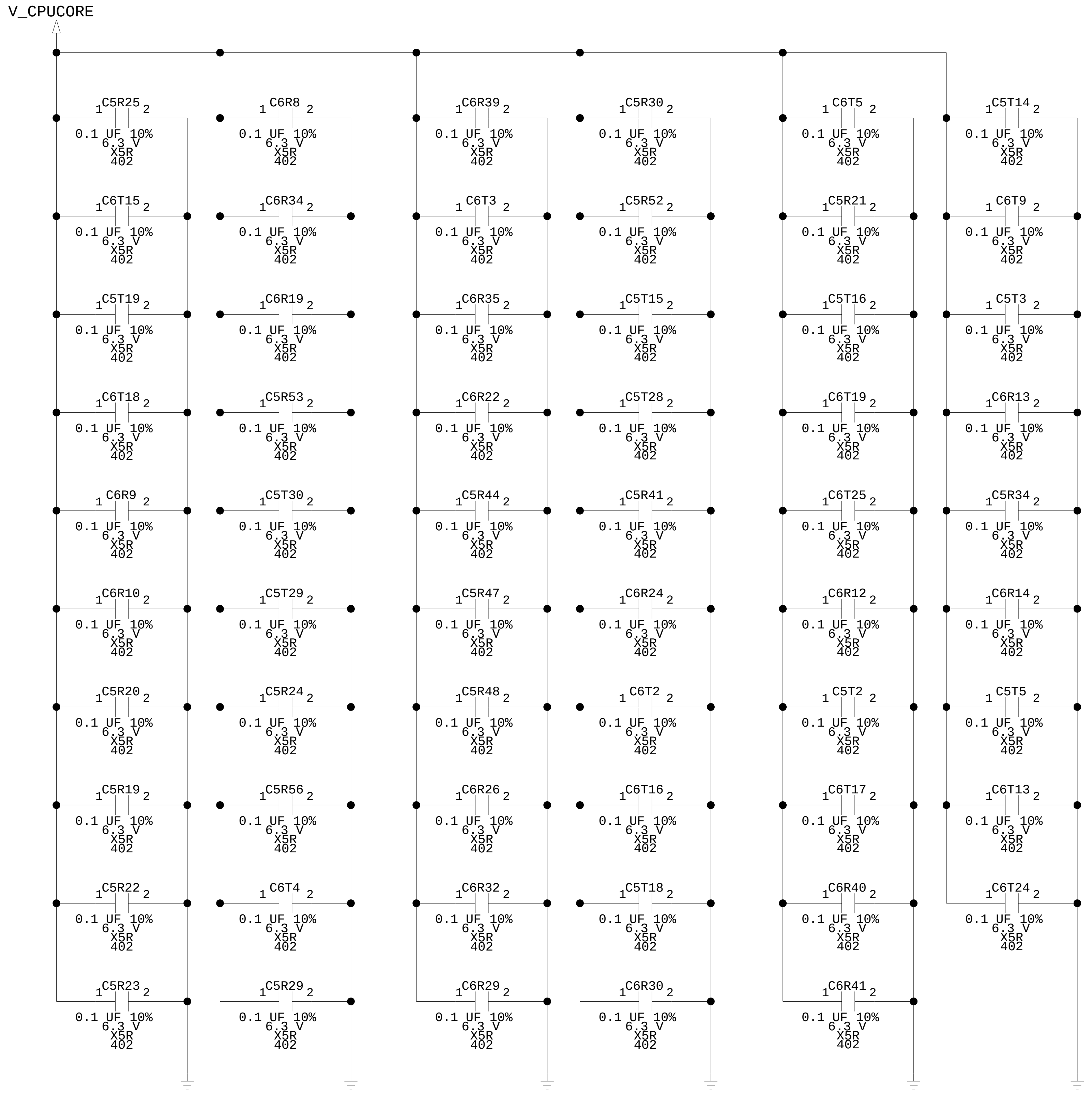
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 10/81	FAB G	REV 1.01

GCPU, DECOUPLING


V_CPUCORE
C5R25 0.1 UF 10% 6.3 V X5R 402
C6T15 0.1 UF 10% 6.3 V X5R 402
C5T19 0.1 UF 10% 6.3 V X5R 402
C6T18 0.1 UF 10% 6.3 V X5R 402
C6R9 0.1 UF 10% 6.3 V X5R 402
C6R10 0.1 UF 10% 6.3 V X5R 402
C5R20 0.1 UF 10% 6.3 V X5R 402
C5R19 0.1 UF 10% 6.3 V X5R 402
C5R22 0.1 UF 10% 6.3 V X5R 402
C5R23 0.1 UF 10% 6.3 V X5R 402
C6R8 0.1 UF 10% 6.3 V X5R 402
C6R34 0.1 UF 10% 6.3 V X5R 402
C6R19 0.1 UF 10% 6.3 V X5R 402
C5R53 0.1 UF 10% 6.3 V X5R 402
C5T30 0.1 UF 10% 6.3 V X5R 402
C5T29 0.1 UF 10% 6.3 V X5R 402
C5R24 0.1 UF 10% 6.3 V X5R 402
C5R56 0.1 UF 10% 6.3 V X5R 402
C6T4 0.1 UF 10% 6.3 V X5R 402
C5R29 0.1 UF 10% 6.3 V X5R 402
C6R39 0.1 UF 10% 6.3 V X5R 402
C6T3 0.1 UF 10% 6.3 V X5R 402
C6R35 0.1 UF 10% 6.3 V X5R 402
C6R22 0.1 UF 10% 6.3 V X5R 402
C5R44 0.1 UF 10% 6.3 V X5R 402
C5R47 0.1 UF 10% 6.3 V X5R 402
C5R48 0.1 UF 10% 6.3 V X5R 402
C6R26 0.1 UF 10% 6.3 V X5R 402
C6R32 0.1 UF 10% 6.3 V X5R 402
C6R29 0.1 UF 10% 6.3 V X5R 402
C5R30 0.1 UF 10% 6.3 V X5R 402
C5R52 0.1 UF 10% 6.3 V X5R 402
C5T15 0.1 UF 10% 6.3 V X5R 402
C5T28 0.1 UF 10% 6.3 V X5R 402
C5R41 0.1 UF 10% 6.3 V X5R 402
C6R24 0.1 UF 10% 6.3 V X5R 402
C6T2 0.1 UF 10% 6.3 V X5R 402
C6T16 0.1 UF 10% 6.3 V X5R 402
C5T18 0.1 UF 10% 6.3 V X5R 402
C6R30 0.1 UF 10% 6.3 V X5R 402
C6T5 0.1 UF 10% 6.3 V X5R 402
C5R21 0.1 UF 10% 6.3 V X5R 402
C5T16 0.1 UF 10% 6.3 V X5R 402
C6T19 0.1 UF 10% 6.3 V X5R 402
C6T25 0.1 UF 10% 6.3 V X5R 402
C6R12 0.1 UF 10% 6.3 V X5R 402
C5T2 0.1 UF 10% 6.3 V X5R 402
C6T17 0.1 UF 10% 6.3 V X5R 402
C6R40 0.1 UF 10% 6.3 V X5R 402
C6R41 0.1 UF 10% 6.3 V X5R 402
C5T14 0.1 UF 10% 6.3 V X5R 402
C6T9 0.1 UF 10% 6.3 V X5R 402
C5T3 0.1 UF 10% 6.3 V X5R 402
C6R13 0.1 UF 10% 6.3 V X5R 402
C5R34 0.1 UF 10% 6.3 V X5R 402
C6R14 0.1 UF 10% 6.3 V X5R 402
C5T5 0.1 UF 10% 6.3 V X5R 402
C6T13 0.1 UF 10% 6.3 V X5R 402
C6T24 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

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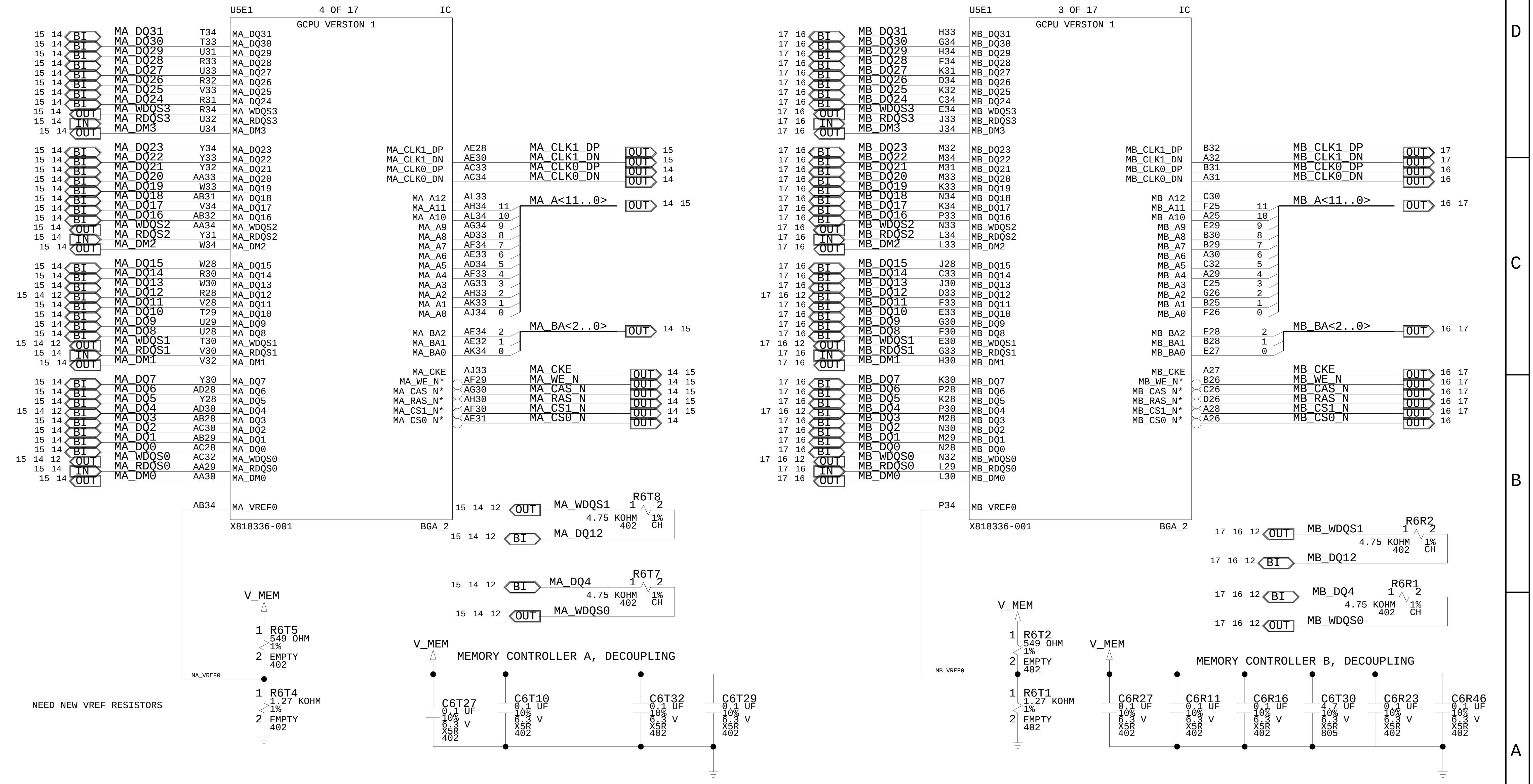
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 11/81	FAB G	REV 1.01

GPU, MEMORY CONTROLLER 0 PARTITION A & B


U5E1 4 OF 17 IC
GCPU VERSION 1
15 14 BI MA_DQ31 T34 MA_DQ31
15 14 BI MA_DQ30 T33 MA_DQ30
15 14 BI MA_DQ29 U31 MA_DQ29
15 14 BI MA_DQ28 R33 MA_DQ28
15 14 BI MA_DQ27 U33 MA_DQ27
15 14 BI MA_DQ26 R32 MA_DQ26
15 14 BI MA_DQ25 V33 MA_DQ25
15 14 BI MA_DQ24 R31 MA_DQ24
15 14 OUT MA_WDQS3 R34 MA_WDQS3
15 14 IN MA_RDQS3 U32 MA_RDQS3
15 14 OUT MA_DM3 U34 MA_DM3
15 14 BI MA_DQ23 Y34 MA_DQ23
15 14 BI MA_DQ22 Y33 MA_DQ22
15 14 BI MA_DQ21 Y32 MA_DQ21
15 14 BI MA_DQ20 AA33 MA_DQ20
15 14 BI MA_DQ19 W33 MA_DQ19
15 14 BI MA_DQ18 AB31 MA_DQ18
15 14 BI MA_DQ17 V34 MA_DQ17
15 14 BI MA_DQ16 AB32 MA_DQ16
15 14 OUT MA_WDQS2 AA34 MA_WDQS2
15 14 IN MA_RDQS2 Y31 MA_RDQS2
15 14 OUT MA_DM2 W34 MA_DM2
15 14 BI MA_DQ15 W28 MA_DQ15
15 14 BI MA_DQ14 R30 MA_DQ14
15 14 BI MA_DQ13 W30 MA_DQ13
15 14 12 BI MA_DQ12 R28 MA_DQ12
15 14 BI MA_DQ11 V28 MA_DQ11
15 14 BI MA_DQ10 T29 MA_DQ10
15 14 BI MA_DQ9 U29 MA_DQ9
15 14 BI MA_DQ8 U28 MA_DQ8
15 14 12 OUT MA_WDQS1 T30 MA_WDQS1
15 14 IN MA_RDQS1 V30 MA_RDQS1
15 14 OUT MA_DM1 V32 MA_DM1
15 14 BI MA_DQ7 Y30 MA_DQ7
15 14 BI MA_DQ6 AD28 MA_DQ6
15 14 BI MA_DQ5 Y28 MA_DQ5
15 14 12 BI MA_DQ4 AD30 MA_DQ4
15 14 BI MA_DQ3 AB28 MA_DQ3
15 14 BI MA_DQ2 AC30 MA_DQ2
15 14 BI MA_DQ1 AB29 MA_DQ1
15 14 BI MA_DQ0 AC28 MA_DQ0
15 14 12 OUT MA_WDQS0 AC32 MA_WDQS0
15 14 IN MA_RDQS0 AA29 MA_RDQS0
15 14 OUT MA_DM0 AA30 MA_DM0
AB34 MA_VREF0
X818336-001 BGA_2
MA_CLK1_DP AE28 MA_CLK1_DP OUT 15
MA_CLK1_DN AE30 MA_CLK1_DN OUT 15
MA_CLK0_DP AC33 MA_CLK0_DP OUT 14
MA_CLK0_DN AC34 MA_CLK0_DN OUT 14
MA_A12 AL33
MA_A11 AH34 11
MA_A10 AL34 10
MA_A9 AG34 9
MA_A8 AD33 8
MA_A7 AF34 7
MA_A6 AE33 6
MA_A5 AD34 5
MA_A4 AF33 4
MA_A3 AG33 3
MA_A2 AH33 2
MA_A1 AK33 1
MA_A0 AJ34 0
MA_A<11..0> OUT 14 15
MA_BA2 AE34 2
MA_BA1 AE32 1
MA_BA0 AK34 0
MA_BA<2..0> OUT 14 15
MA_CKE AJ33 MA_CKE OUT 14 15
MA_WE_N* AF29 MA_WE_N OUT 14 15
MA_CAS_N* AG30 MA_CAS_N OUT 14 15
MA_RAS_N* AH30 MA_RAS_N OUT 14 15
MA_CS1_N* AF30 MA_CS1_N OUT 14 15
MA_CS0_N* AE31 MA_CS0_N OUT 14
15 14 12 OUT MA_WDQS1
R6T8 1 2
4.75 KOHM 402 1% CH
15 14 12 BI MA_DQ12
15 14 12 BI MA_DQ4
R6T7 1 2
4.75 KOHM 402 1% CH
15 14 12 OUT MA_WDQS0
V_MEM
R6T5 1 549 OHM 1% 2 EMPTY 402
MA_VREF0
R6T4 1 1.27 KOHM 1% 2 EMPTY 402
NEED NEW VREF RESISTORS
V_MEM
MEMORY CONTROLLER A, DECOUPLING
C6T27 0.1 UF 10% 6.3 V X5R 402
C6T10 0.1 UF 10% 6.3 V X5R 402
C6T32 0.1 UF 10% 6.3 V X5R 402
C6T29 0.1 UF 10% 6.3 V X5R 402
U5E1 3 OF 17 IC
GCPU VERSION 1
17 16 BI MB_DQ31 H33 MB_DQ31
17 16 BI MB_DQ30 G34 MB_DQ30
17 16 BI MB_DQ29 H34 MB_DQ29
17 16 BI MB_DQ28 F34 MB_DQ28
17 16 BI MB_DQ27 K31 MB_DQ27
17 16 BI MB_DQ26 D34 MB_DQ26
17 16 BI MB_DQ25 K32 MB_DQ25
17 16 BI MB_DQ24 C34 MB_DQ24
17 16 OUT MB_WDQS3 E34 MB_WDQS3
17 16 IN MB_RDQS3 J33 MB_RDQS3
17 16 OUT MB_DM3 J34 MB_DM3
17 16 BI MB_DQ23 M32 MB_DQ23
17 16 BI MB_DQ22 M34 MB_DQ22
17 16 BI MB_DQ21 M31 MB_DQ21
17 16 BI MB_DQ20 M33 MB_DQ20
17 16 BI MB_DQ19 K33 MB_DQ19
17 16 BI MB_DQ18 N34 MB_DQ18
17 16 BI MB_DQ17 K34 MB_DQ17
17 16 BI MB_DQ16 P33 MB_DQ16
17 16 OUT MB_WDQS2 N33 MB_WDQS2
17 16 IN MB_RDQS2 L34 MB_RDQS2
17 16 OUT MB_DM2 L33 MB_DM2
17 16 BI MB_DQ15 J28 MB_DQ15
17 16 BI MB_DQ14 C33 MB_DQ14
17 16 BI MB_DQ13 J30 MB_DQ13
17 16 12 BI MB_DQ12 D33 MB_DQ12
17 16 BI MB_DQ11 F33 MB_DQ11
17 16 BI MB_DQ10 E33 MB_DQ10
17 16 BI MB_DQ9 G30 MB_DQ9
17 16 BI MB_DQ8 F30 MB_DQ8
17 16 12 OUT MB_WDQS1 E30 MB_WDQS1
17 16 IN MB_RDQS1 G33 MB_RDQS1
17 16 OUT MB_DM1 H30 MB_DM1
17 16 BI MB_DQ7 K30 MB_DQ7
17 16 BI MB_DQ6 P28 MB_DQ6
17 16 BI MB_DQ5 K28 MB_DQ5
17 16 12 BI MB_DQ4 P30 MB_DQ4
17 16 BI MB_DQ3 M28 MB_DQ3
17 16 BI MB_DQ2 N30 MB_DQ2
17 16 BI MB_DQ1 M29 MB_DQ1
17 16 BI MB_DQ0 N28 MB_DQ0
17 16 12 OUT MB_WDQS0 N32 MB_WDQS0
17 16 IN MB_RDQS0 L29 MB_RDQS0
17 16 OUT MB_DM0 L30 MB_DM0
P34 MB_VREF0
X818336-001 BGA_2
MB_CLK1_DP B32 MB_CLK1_DP OUT 17
MB_CLK1_DN A32 MB_CLK1_DN OUT 17
MB_CLK0_DP B31 MB_CLK0_DP OUT 16
MB_CLK0_DN A31 MB_CLK0_DN OUT 16
MB_A12 C30
MB_A11 F25 11
MB_A10 A25 10
MB_A9 E29 9
MB_A8 B30 8
MB_A7 B29 7
MB_A6 A30 6
MB_A5 C32 5
MB_A4 A29 4
MB_A3 E25 3
MB_A2 G26 2
MB_A1 B25 1
MB_A0 F26 0
MB_A<11..0> OUT 16 17
MB_BA2 E28 2
MB_BA1 B28 1
MB_BA0 E27 0
MB_BA<2..0> OUT 16 17
MB_CKE A27 MB_CKE OUT 16 17
MB_WE_N* B26 MB_WE_N OUT 16 17
MB_CAS_N* C26 MB_CAS_N OUT 16 17
MB_RAS_N* D26 MB_RAS_N OUT 16 17
MB_CS1_N* A28 MB_CS1_N OUT 16 17
MB_CS0_N* A26 MB_CS0_N OUT 16
17 16 12 OUT MB_WDQS1
R6R2 1 2
4.75 KOHM 402 1% CH
17 16 12 BI MB_DQ12
17 16 12 BI MB_DQ4
R6R1 1 2
4.75 KOHM 402 1% CH
17 16 12 OUT MB_WDQS0
V_MEM
R6T2 1 549 OHM 1% 2 EMPTY 402
MB_VREF0
R6T1 1 1.27 KOHM 1% 2 EMPTY 402
V_MEM
MEMORY CONTROLLER B, DECOUPLING
C6R27 0.1 UF 10% 6.3 V X5R 402
C6R11 0.1 UF 10% 6.3 V X5R 402
C6R16 0.1 UF 10% 6.3 V X5R 402
C6T30 4.7 UF 10% 6.3 V X5R 805
C6R23 0.1 UF 10% 6.3 V X5R 402
C6R46 0.1 UF 10% 6.3 V X5R 402

TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=GPU, MEMORY CONTROLLER A + B]

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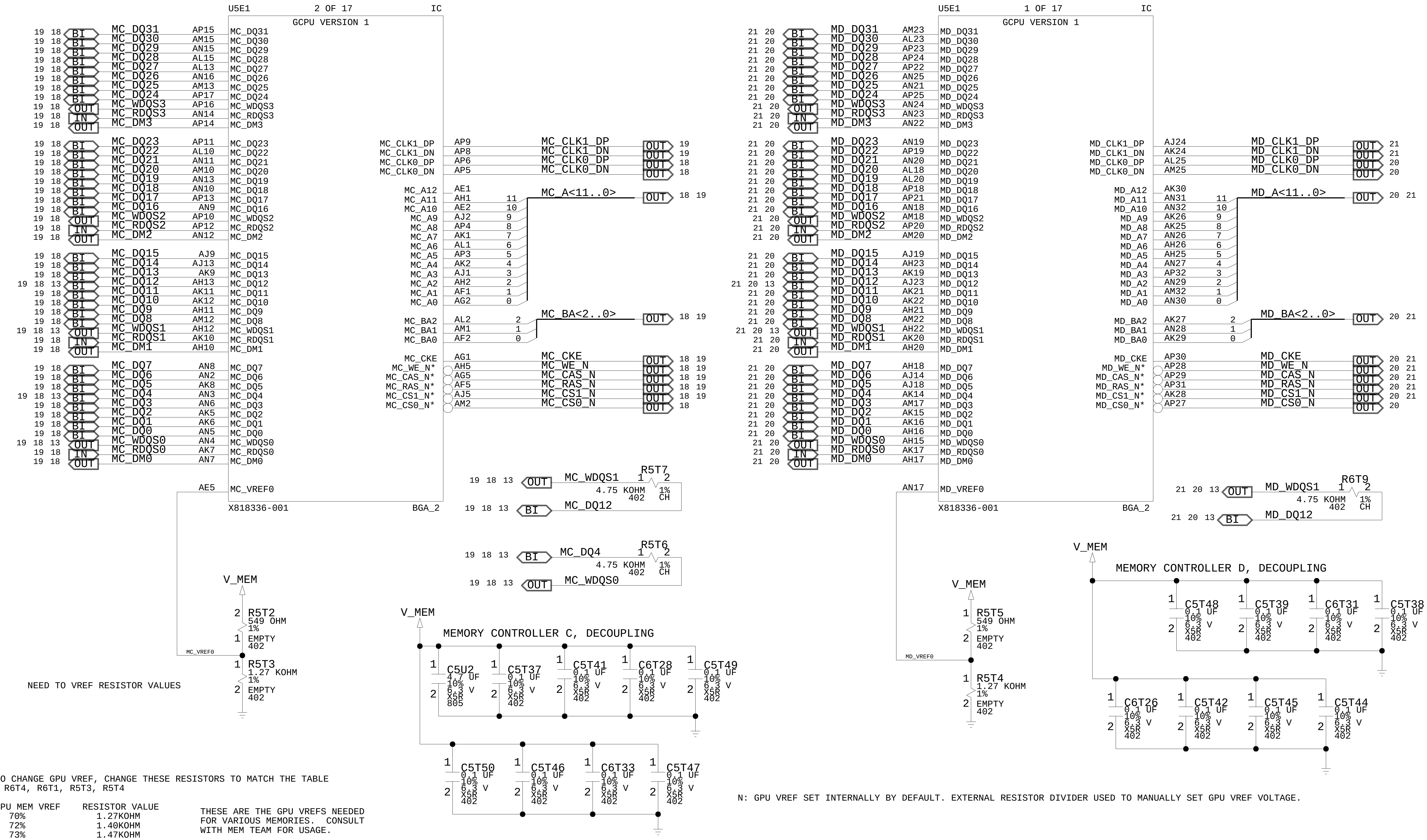
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	12/81	G	1.01

GPU, MEMORY CONTROLLER 1 PARTITION C & D


U5E1 2 OF 17 IC
GCPU VERSION 1
19 18 BI MC_DQ31 AP15 MC_DQ31
19 18 BI MC_DQ30 AM15 MC_DQ30
19 18 BI MC_DQ29 AN15 MC_DQ29
19 18 BI MC_DQ28 AL15 MC_DQ28
19 18 BI MC_DQ27 AL13 MC_DQ27
19 18 BI MC_DQ26 AN16 MC_DQ26
19 18 BI MC_DQ25 AM13 MC_DQ25
19 18 BI MC_DQ24 AP17 MC_DQ24
19 18 OUT MC_WDQS3 AP16 MC_WDQS3
19 18 IN MC_RDQS3 AN14 MC_RDQS3
19 18 OUT MC_DM3 AP14 MC_DM3
19 18 BI MC_DQ23 AP11 MC_DQ23
19 18 BI MC_DQ22 AL10 MC_DQ22
19 18 BI MC_DQ21 AN11 MC_DQ21
19 18 BI MC_DQ20 AM10 MC_DQ20
19 18 BI MC_DQ19 AN13 MC_DQ19
19 18 BI MC_DQ18 AN10 MC_DQ18
19 18 BI MC_DQ17 AP13 MC_DQ17
19 18 BI MC_DQ16 AN9 MC_DQ16
19 18 OUT MC_WDQS2 AP10 MC_WDQS2
19 18 IN MC_RDQS2 AP12 MC_RDQS2
19 18 OUT MC_DM2 AN12 MC_DM2
19 18 BI MC_DQ15 AJ9 MC_DQ15
19 18 BI MC_DQ14 AJ13 MC_DQ14
19 18 BI MC_DQ13 AK9 MC_DQ13
19 18 13 BI MC_DQ12 AH13 MC_DQ12
19 18 BI MC_DQ11 AK11 MC_DQ11
19 18 BI MC_DQ10 AK12 MC_DQ10
19 18 BI MC_DQ9 AH11 MC_DQ9
19 18 BI MC_DQ8 AM12 MC_DQ8
19 18 13 OUT MC_WDQS1 AH12 MC_WDQS1
19 18 IN MC_RDQS1 AK10 MC_RDQS1
19 18 OUT MC_DM1 AH10 MC_DM1
19 18 BI MC_DQ7 AN8 MC_DQ7
19 18 BI MC_DQ6 AN2 MC_DQ6
19 18 BI MC_DQ5 AK8 MC_DQ5
19 18 13 BI MC_DQ4 AN3 MC_DQ4
19 18 BI MC_DQ3 AN6 MC_DQ3
19 18 BI MC_DQ2 AK5 MC_DQ2
19 18 BI MC_DQ1 AK6 MC_DQ1
19 18 BI MC_DQ0 AN5 MC_DQ0
19 18 13 OUT MC_WDQS0 AN4 MC_WDQS0
19 18 IN MC_RDQS0 AK7 MC_RDQS0
19 18 OUT MC_DM0 AN7 MC_DM0
AE5 MC_VREF0
X818336-001 BGA_2
MC_CLK1_DP AP9 MC_CLK1_DP OUT 19
MC_CLK1_DN AP8 MC_CLK1_DN OUT 19
MC_CLK0_DP AP6 MC_CLK0_DP OUT 18
MC_CLK0_DN AP5 MC_CLK0_DN OUT 18
MC_A12 AE1
MC_A11 AH1 11
MC_A10 AE2 10
MC_A9 AJ2 9
MC_A8 AP4 8
MC_A7 AK1 7
MC_A6 AL1 6
MC_A5 AP3 5
MC_A4 AK2 4
MC_A3 AJ1 3
MC_A2 AH2 2
MC_A1 AF1 1
MC_A0 AG2 0
MC_A<11..0> OUT 18 19
MC_BA2 AL2 2
MC_BA1 AM1 1
MC_BA0 AF2 0
MC_BA<2..0> OUT 18 19
MC_CKE AG1 MC_CKE OUT 18 19
MC_WE_N* AH5 MC_WE_N OUT 18 19
MC_CAS_N* AG5 MC_CAS_N OUT 18 19
MC_RAS_N* AF5 MC_RAS_N OUT 18 19
MC_CS1_N* AJ5 MC_CS1_N OUT 18 19
MC_CS0_N* AM2 MC_CS0_N OUT 18
19 18 13 OUT MC_WDQS1
R5T7 1 2
4.75 KOHM 1%
402 CH
19 18 13 BI MC_DQ12
19 18 13 BI MC_DQ4
R5T6 1 2
4.75 KOHM 1%
402 CH
19 18 13 OUT MC_WDQS0
V_MEM
2 R5T2 549 OHM 1%
1 EMPTY 402
MC_VREF0
1 R5T3 1.27 KOHM 1%
2 EMPTY 402
V_MEM
MEMORY CONTROLLER C, DECOUPLING
C5U2 4.7 UF 10% 6.3 V X5R 805
C5T37 0.1 UF 10% 6.3 V X5R 402
C5T41 0.1 UF 10% 6.3 V X5R 402
C6T28 0.1 UF 10% 6.3 V X5R 402
C5T49 0.1 UF 10% 6.3 V X5R 402
C5T50 0.1 UF 10% 6.3 V X5R 402
C5T46 0.1 UF 10% 6.3 V X5R 402
C6T33 0.1 UF 10% 6.3 V X5R 402
C5T47 0.1 UF 10% 6.3 V X5R 402
U5E1 1 OF 17 IC
GCPU VERSION 1
21 20 BI MD_DQ31 AM23 MD_DQ31
21 20 BI MD_DQ30 AL23 MD_DQ30
21 20 BI MD_DQ29 AP23 MD_DQ29
21 20 BI MD_DQ28 AP24 MD_DQ28
21 20 BI MD_DQ27 AP22 MD_DQ27
21 20 BI MD_DQ26 AN25 MD_DQ26
21 20 BI MD_DQ25 AN21 MD_DQ25
21 20 BI MD_DQ24 AP25 MD_DQ24
21 20 OUT MD_WDQS3 AN24 MD_WDQS3
21 20 IN MD_RDQS3 AN23 MD_RDQS3
21 20 OUT MD_DM3 AN22 MD_DM3
21 20 BI MD_DQ23 AN19 MD_DQ23
21 20 BI MD_DQ22 AP19 MD_DQ22
21 20 BI MD_DQ21 AN20 MD_DQ21
21 20 BI MD_DQ20 AL18 MD_DQ20
21 20 BI MD_DQ19 AL20 MD_DQ19
21 20 BI MD_DQ18 AP18 MD_DQ18
21 20 BI MD_DQ17 AP21 MD_DQ17
21 20 BI MD_DQ16 AN18 MD_DQ16
21 20 OUT MD_WDQS2 AM18 MD_WDQS2
21 20 IN MD_RDQS2 AP20 MD_RDQS2
21 20 OUT MD_DM2 AM20 MD_DM2
21 20 BI MD_DQ15 AJ19 MD_DQ15
21 20 BI MD_DQ14 AH23 MD_DQ14
21 20 BI MD_DQ13 AK19 MD_DQ13
21 20 13 BI MD_DQ12 AJ23 MD_DQ12
21 20 BI MD_DQ11 AK21 MD_DQ11
21 20 BI MD_DQ10 AK22 MD_DQ10
21 20 BI MD_DQ9 AH21 MD_DQ9
21 20 BI MD_DQ8 AM22 MD_DQ8
21 20 13 OUT MD_WDQS1 AH22 MD_WDQS1
21 20 IN MD_RDQS1 AK20 MD_RDQS1
21 20 OUT MD_DM1 AH20 MD_DM1
21 20 BI MD_DQ7 AH18 MD_DQ7
21 20 BI MD_DQ6 AJ14 MD_DQ6
21 20 BI MD_DQ5 AJ18 MD_DQ5
21 20 BI MD_DQ4 AK14 MD_DQ4
21 20 BI MD_DQ3 AM17 MD_DQ3
21 20 BI MD_DQ2 AK15 MD_DQ2
21 20 BI MD_DQ1 AK16 MD_DQ1
21 20 BI MD_DQ0 AH16 MD_DQ0
21 20 OUT MD_WDQS0 AH15 MD_WDQS0
21 20 IN MD_RDQS0 AK17 MD_RDQS0
21 20 OUT MD_DM0 AH17 MD_DM0
AN17 MD_VREF0
X818336-001 BGA_2
MD_CLK1_DP AJ24 MD_CLK1_DP OUT 21
MD_CLK1_DN AK24 MD_CLK1_DN OUT 21
MD_CLK0_DP AL25 MD_CLK0_DP OUT 20
MD_CLK0_DN AM25 MD_CLK0_DN OUT 20
MD_A12 AK30
MD_A11 AN31 11
MD_A10 AN32 10
MD_A9 AK26 9
MD_A8 AK25 8
MD_A7 AN26 7
MD_A6 AH26 6
MD_A5 AH25 5
MD_A4 AH27 4
MD_A3 AP32 3
MD_A2 AP29 2
MD_A1 AM32 1
MD_A0 AN30 0
MD_A<11..0> OUT 20 21
MD_BA2 AK27 2
MD_BA1 AN28 1
MD_BA0 AK29 0
MD_BA<2..0> OUT 20 21
MD_CKE AP30 MD_CKE OUT 20 21
MD_WE_N* AP28 MD_WE_N OUT 20 21
MD_CAS_N* AP29 MD_CAS_N OUT 20 21
MD_RAS_N* AP31 MD_RAS_N OUT 20 21
MD_CS1_N* AK28 MD_CS1_N OUT 20 21
MD_CS0_N* AP27 MD_CS0_N OUT 20
21 20 13 OUT MD_WDQS1
R6T9 1 2
4.75 KOHM 1%
402 CH
21 20 13 BI MD_DQ12
V_MEM
1 R5T5 549 OHM 1%
2 EMPTY 402
MD_VREF0
1 R5T4 1.27 KOHM 1%
2 EMPTY 402
V_MEM
MEMORY CONTROLLER D, DECOUPLING
C5T48 0.1 UF 10% 6.3 V X5R 402
C5T39 0.1 UF 10% 6.3 V X5R 402
C6T31 0.1 UF 10% 6.3 V X5R 402
C5T38 0.1 UF 10% 6.3 V X5R 402
C6T26 0.1 UF 10% 6.3 V X5R 402
C5T42 0.1 UF 10% 6.3 V X5R 402
C5T45 0.1 UF 10% 6.3 V X5R 402
C5T44 0.1 UF 10% 6.3 V X5R 402

NEED TO VREF RESISTOR VALUES

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

GPU MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED
FOR VARIOUS MEMORIES. CONSULT
WITH MEM TEAM FOR USAGE.

[PAGE_TITLE=[GPU, MEMORY CONTROLLER C + D]

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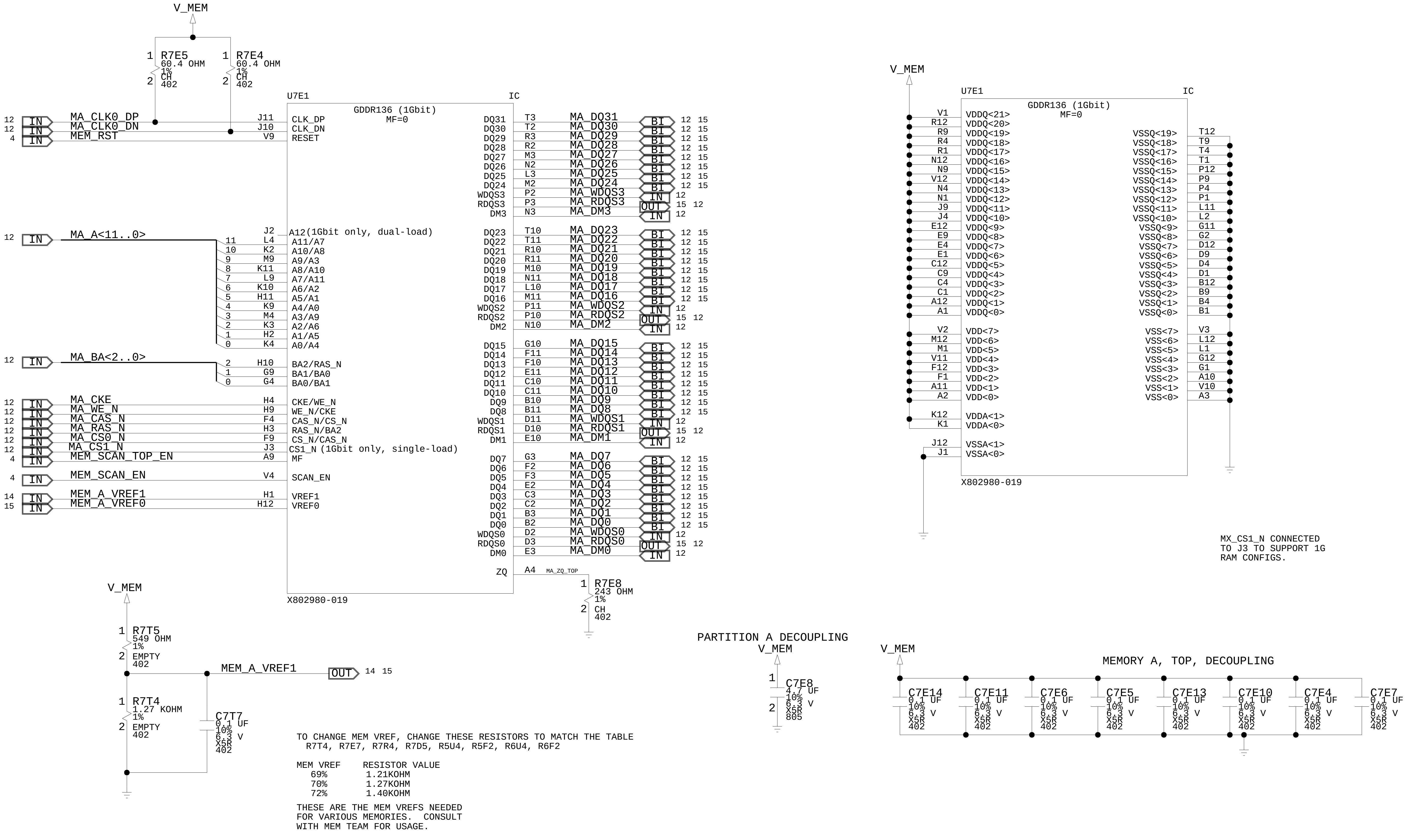
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 13/81	FAB G	REV 1.01

MEMORY PARTITION A, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0


V_MEM
R7E5
60.4 OHM
1%
CH
402
R7E4
60.4 OHM
1%
CH
402
U7E1
IC
GDDR136 (1Gbit)
MF=0
MA_CLK0_DP
MA_CLK0_DN
MEM_RST
CLK_DP
CLK_DN
RESET
MA_A<11..0>
A12(1Gbit only, dual-load)
MA_BA<2..0>
BA2/RAS_N
BA1/BA0
BA0/BA1
MA_CKE
MA_WE_N
MA_CAS_N
MA_RAS_N
MA_CS0_N
MA_CS1_N
MEM_SCAN_TOP_EN
MEM_SCAN_EN
MEM_A_VREF1
MEM_A_VREF0
CS1_N (1Gbit only, single-load)
SCAN_EN
VREF1
VREF0
IN
OUT
BI
MA_DQ0 … MA_DQ31
MA_WDQS0 … MA_WDQS3
MA_RDQS0 … MA_RDQS3
MA_DM0 … MA_DM3
ZQ
MA_ZQ_TOP
R7E8
243 OHM
1%
CH
402
X802980-019
VDDQ<21> … VDDQ<0>
VSSQ<19> … VSSQ<0>
VDD<7> … VDD<0>
VSS<7> … VSS<0>
VDDA<1>
VDDA<0>
VSSA<1>
VSSA<0>
R7T5
549 OHM
1%
EMPTY
402
R7T4
1.27 KOHM
1%
EMPTY
402
C7T7
0.1 UF
10%
6.3 V
X5R
402
MEM_A_VREF1
PARTITION A DECOUPLING
C7E8
4.7 UF
10%
6.3 V
X5R
805
MEMORY A, TOP, DECOUPLING
C7E14
C7E11
C7E6
C7E5
C7E13
C7E10
C7E4
C7E7
0.1 UF
10%
6.3 V
X5R
402

MX_CS1_N CONNECTED
TO J3 TO SUPPORT 1G
RAM CONFIGS.

TO CHANGE MEM VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R7T4, R7E7, R7R4, R7D5, R5U4, R5F2, R6U4, R6F2

MEM VREF	RESISTOR VALUE
69%	1.21KOHM
70%	1.27KOHM
72%	1.40KOHM

THESE ARE THE MEM VREFS NEEDED
FOR VARIOUS MEMORIES. CONSULT
WITH MEM TEAM FOR USAGE.

[PAGE_TITLE=MEMORY PARTITION A, TOP]

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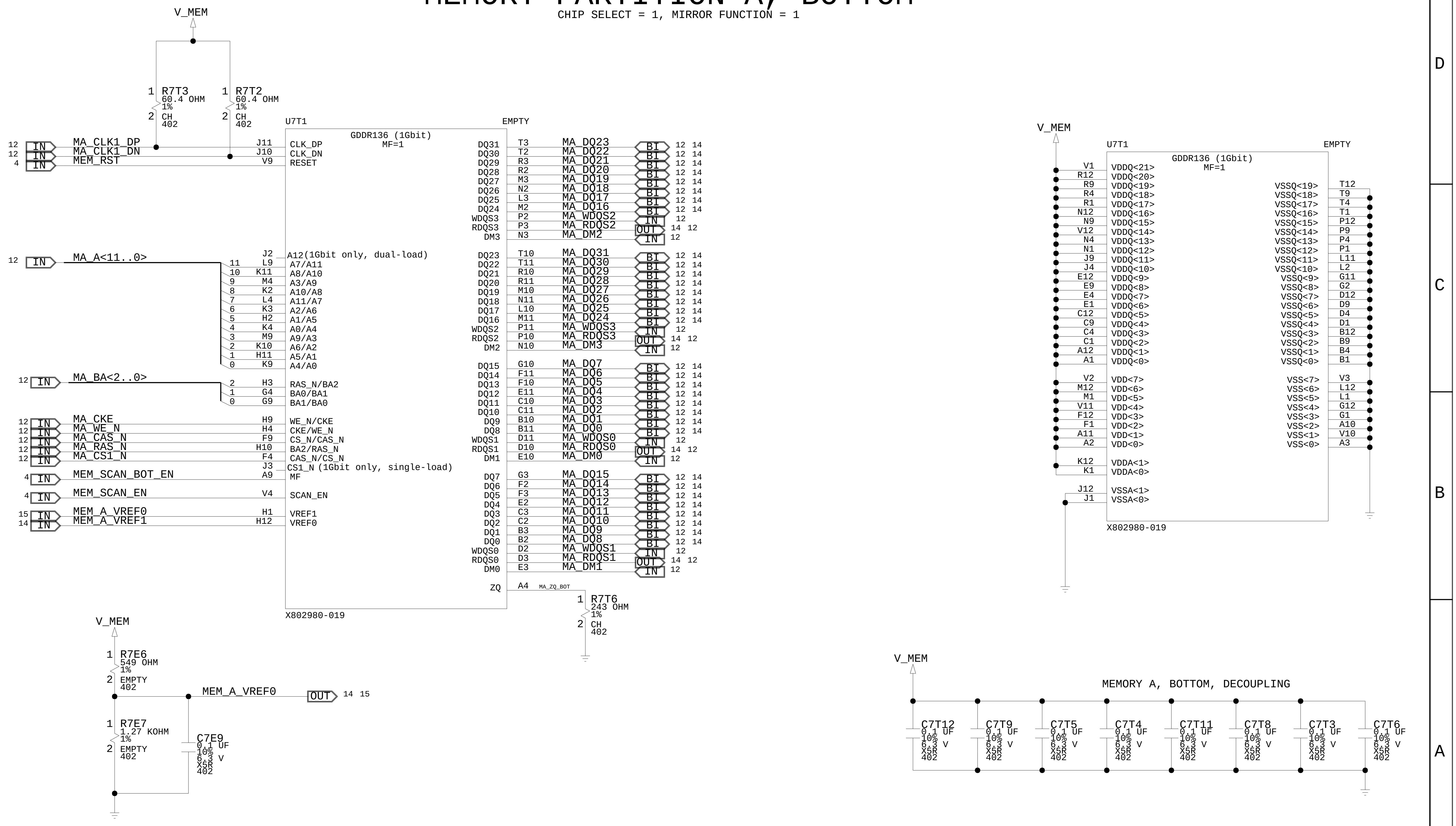
MICROSOFT
CONFIDENTIAL

PROJECT NAME	PAGE	FAB	REV
TRINITY_XDK	14/81	G	1.01

MEMORY PARTITION A, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1


V_MEM
R7T3 60.4 OHM 1% CH 402
R7T2 60.4 OHM 1% CH 402
U7T1 EMPTY
GDDR136 (1Gbit) MF=1
MA_CLK1_DP J11 CLK_DP
MA_CLK1_DN J10 CLK_DN
MEM_RST V9 RESET
MA_A<11..0> J2 A12(1Gbit only, dual-load)
L9 A7/A11, K11 A8/A10, M4 A3/A9, K2 A10/A8, L4 A11/A7, K3 A2/A6, H2 A1/A5, K4 A0/A4, M9 A9/A3, K10 A6/A2, H11 A5/A1, K9 A4/A0
MA_BA<2..0> H3 RAS_N/BA2, G4 BA0/BA1, G9 BA1/BA0
MA_CKE H9 WE_N/CKE
MA_WE_N H4 CKE/WE_N
MA_CAS_N F9 CS_N/CAS_N
MA_RAS_N H10 BA2/RAS_N
MA_CS1_N F4 CAS_N/CS_N
J3 CS1_N (1Gbit only, single-load)
MEM_SCAN_BOT_EN A9 MF
MEM_SCAN_EN V4 SCAN_EN
MEM_A_VREF0 H1 VREF1
MEM_A_VREF1 H12 VREF0
DQ31 T3 MA_DQ23; DQ30 T2 MA_DQ22; DQ29 R3 MA_DQ21; DQ28 R2 MA_DQ20; DQ27 M3 MA_DQ19; DQ26 N2 MA_DQ18; DQ25 L3 MA_DQ17; DQ24 M2 MA_DQ16; WDQS3 P2 MA_WDQS2; RDQS3 P3 MA_RDQS2; DM3 N3 MA_DM2
DQ23 T10 MA_DQ31; DQ22 T11 MA_DQ30; DQ21 R10 MA_DQ29; DQ20 R11 MA_DQ28; DQ19 M10 MA_DQ27; DQ18 N11 MA_DQ26; DQ17 L10 MA_DQ25; DQ16 M11 MA_DQ24; WDQS2 P11 MA_WDQS3; RDQS2 P10 MA_RDQS3; DM2 N10 MA_DM3
DQ15 G10 MA_DQ7; DQ14 F11 MA_DQ6; DQ13 F10 MA_DQ5; DQ12 E11 MA_DQ4; DQ11 C10 MA_DQ3; DQ10 C11 MA_DQ2; DQ9 B10 MA_DQ1; DQ8 B11 MA_DQ0; WDQS1 D11 MA_WDQS0; RDQS1 D10 MA_RDQS0; DM1 E10 MA_DM0
DQ7 G3 MA_DQ15; DQ6 F2 MA_DQ14; DQ5 F3 MA_DQ13; DQ4 E2 MA_DQ12; DQ3 C3 MA_DQ11; DQ2 C2 MA_DQ10; DQ1 B3 MA_DQ9; DQ0 B2 MA_DQ8; WDQS0 D2 MA_WDQS1; RDQS0 D3 MA_RDQS1; DM0 E3 MA_DM1
ZQ A4 MA_ZQ_BOT
R7T6 243 OHM 1% CH 402
X802980-019
VDDQ<21..0>: V1 R12 R9 R4 R1 N12 N9 V12 N4 N1 J9 J4 E12 E9 E4 E1 C12 C9 C4 C1 A12 A1
VDD<7..0>: V2 M12 M1 V11 F12 F1 A11 A2
VDDA<1> K12, VDDA<0> K1
VSSA<1> J12, VSSA<0> J1
VSSQ<19..0>: T12 T9 T4 T1 P12 P9 P4 P1 L11 L2 G11 G2 D12 D9 D4 D1 B12 B9 B4 B1
VSS<7..0>: V3 L12 L1 G12 G1 A10 V10 A3
R7E6 549 OHM 1% EMPTY 402
R7E7 1.27 KOHM 1% EMPTY 402
C7E9 0.1 UF 10% 6.3 V X5R 402
MEM_A_VREF0 OUT 14 15
MEMORY A, BOTTOM, DECOUPLING
C7T12, C7T9, C7T5, C7T4, C7T11, C7T8, C7T3, C7T6 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARTITION A, BOTTOM]

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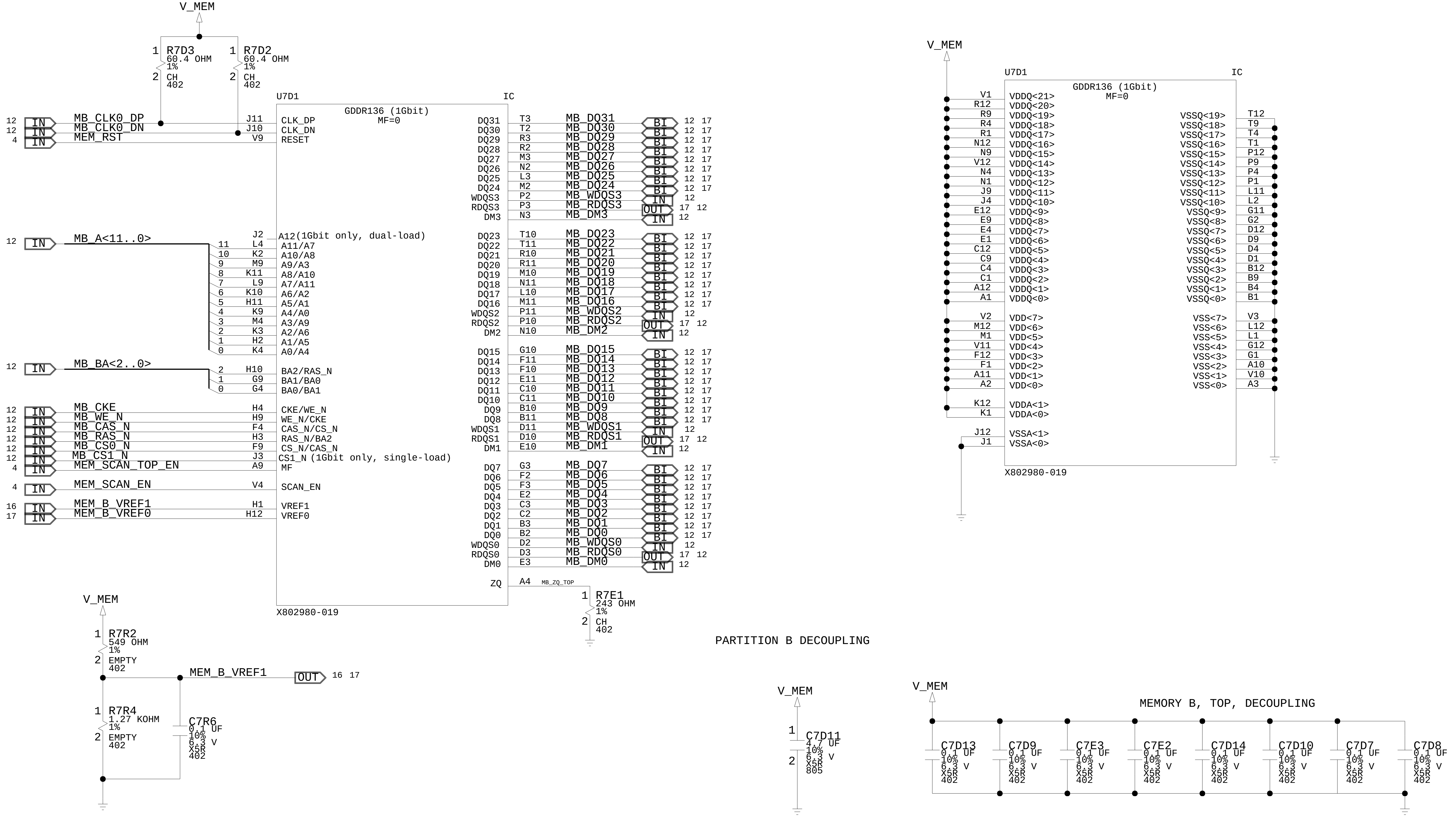
MICROSOFT CONFIDENTIAL

PROJECT NAME	PAGE	FAB	REV
TRINITY_XDK	15/81	G	1.01

MEMORY PARTITION B, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0


V_MEM
R7D3 60.4 OHM 1% CH 402
R7D2 60.4 OHM 1% CH 402
U7D1
IC
GDDR136 (1Gbit)
MF=0
MB_CLK0_DP J11 CLK_DP
MB_CLK0_DN J10 CLK_DN
MEM_RST V9 RESET
MB_A<11..0>
J2 A12(1Gbit only, dual-load)
L4 A11/A7
K2 A10/A8
M9 A9/A3
K11 A8/A10
L9 A7/A11
K10 A6/A2
H11 A5/A1
K9 A4/A0
M4 A3/A9
K3 A2/A6
H2 A1/A5
K4 A0/A4
MB_BA<2..0>
H10 BA2/RAS_N
G9 BA1/BA0
G4 BA0/BA1
MB_CKE H4 CKE/WE_N
MB_WE_N H9 WE_N/CKE
MB_CAS_N F4 CAS_N/CS_N
MB_RAS_N H3 RAS_N/BA2
MB_CS0_N F9 CS_N/CAS_N
MB_CS1_N J3 CS1_N (1Gbit only, single-load)
MEM_SCAN_TOP_EN A9 MF
MEM_SCAN_EN V4 SCAN_EN
MEM_B_VREF1 H1 VREF1
MEM_B_VREF0 H12 VREF0
IN
DQ31 T3 MB_DQ31
DQ30 T2 MB_DQ30
DQ29 R3 MB_DQ29
DQ28 R2 MB_DQ28
DQ27 M3 MB_DQ27
DQ26 N2 MB_DQ26
DQ25 L3 MB_DQ25
DQ24 M2 MB_DQ24
WDQS3 P2 MB_WDQS3
RDQS3 P3 MB_RDQS3
DM3 N3 MB_DM3
DQ23 T10 MB_DQ23
DQ22 T11 MB_DQ22
DQ21 R10 MB_DQ21
DQ20 R11 MB_DQ20
DQ19 M10 MB_DQ19
DQ18 N11 MB_DQ18
DQ17 L10 MB_DQ17
DQ16 M11 MB_DQ16
WDQS2 P11 MB_WDQS2
RDQS2 P10 MB_RDQS2
DM2 N10 MB_DM2
DQ15 G10 MB_DQ15
DQ14 F11 MB_DQ14
DQ13 F10 MB_DQ13
DQ12 E11 MB_DQ12
DQ11 C10 MB_DQ11
DQ10 C11 MB_DQ10
DQ9 B10 MB_DQ9
DQ8 B11 MB_DQ8
WDQS1 D11 MB_WDQS1
RDQS1 D10 MB_RDQS1
DM1 E10 MB_DM1
DQ7 G3 MB_DQ7
DQ6 F2 MB_DQ6
DQ5 F3 MB_DQ5
DQ4 E2 MB_DQ4
DQ3 C3 MB_DQ3
DQ2 C2 MB_DQ2
DQ1 B3 MB_DQ1
DQ0 B2 MB_DQ0
WDQS0 D2 MB_WDQS0
RDQS0 D3 MB_RDQS0
DM0 E3 MB_DM0
BI
OUT
12 17
ZQ A4 MB_ZQ_TOP
R7E1 243 OHM 1% CH 402
X802980-019
V_MEM
U7D1
IC
GDDR136 (1Gbit)
MF=0
V1 VDDQ<21>
R12 VDDQ<20>
R9 VDDQ<19>
R4 VDDQ<18>
R1 VDDQ<17>
N12 VDDQ<16>
N9 VDDQ<15>
V12 VDDQ<14>
N4 VDDQ<13>
N1 VDDQ<12>
J9 VDDQ<11>
J4 VDDQ<10>
E12 VDDQ<9>
E9 VDDQ<8>
E4 VDDQ<7>
E1 VDDQ<6>
C12 VDDQ<5>
C9 VDDQ<4>
C4 VDDQ<3>
C1 VDDQ<2>
A12 VDDQ<1>
A1 VDDQ<0>
V2 VDD<7>
M12 VDD<6>
M1 VDD<5>
V11 VDD<4>
F12 VDD<3>
F1 VDD<2>
A11 VDD<1>
A2 VDD<0>
K12 VDDA<1>
K1 VDDA<0>
J12 VSSA<1>
J1 VSSA<0>
VSSQ<19> T12
VSSQ<18> T9
VSSQ<17> T4
VSSQ<16> T1
VSSQ<15> P12
VSSQ<14> P9
VSSQ<13> P4
VSSQ<12> P1
VSSQ<11> L11
VSSQ<10> L2
VSSQ<9> G11
VSSQ<8> G2
VSSQ<7> D12
VSSQ<6> D9
VSSQ<5> D4
VSSQ<4> D1
VSSQ<3> B12
VSSQ<2> B9
VSSQ<1> B4
VSSQ<0> B1
VSS<7> V3
VSS<6> L12
VSS<5> L1
VSS<4> G12
VSS<3> G1
VSS<2> A10
VSS<1> V10
VSS<0> A3
X802980-019
V_MEM
R7R2 549 OHM 1% EMPTY 402
MEM_B_VREF1
OUT 16 17
R7R4 1.27 KOHM 1% EMPTY 402
C7R6 0.1 UF 10% 6.3 V X5R 402
PARTITION B DECOUPLING
V_MEM
C7D11 4.7 UF 10% 6.3 V X5R 805
V_MEM
MEMORY B, TOP, DECOUPLING
C7D13 0.1 UF 10% 6.3 V X5R 402
C7D9 0.1 UF 10% 6.3 V X5R 402
C7E3 0.1 UF 10% 6.3 V X5R 402
C7E2 0.1 UF 10% 6.3 V X5R 402
C7D14 0.1 UF 10% 6.3 V X5R 402
C7D10 0.1 UF 10% 6.3 V X5R 402
C7D7 0.1 UF 10% 6.3 V X5R 402
C7D8 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARITION B, TOP]

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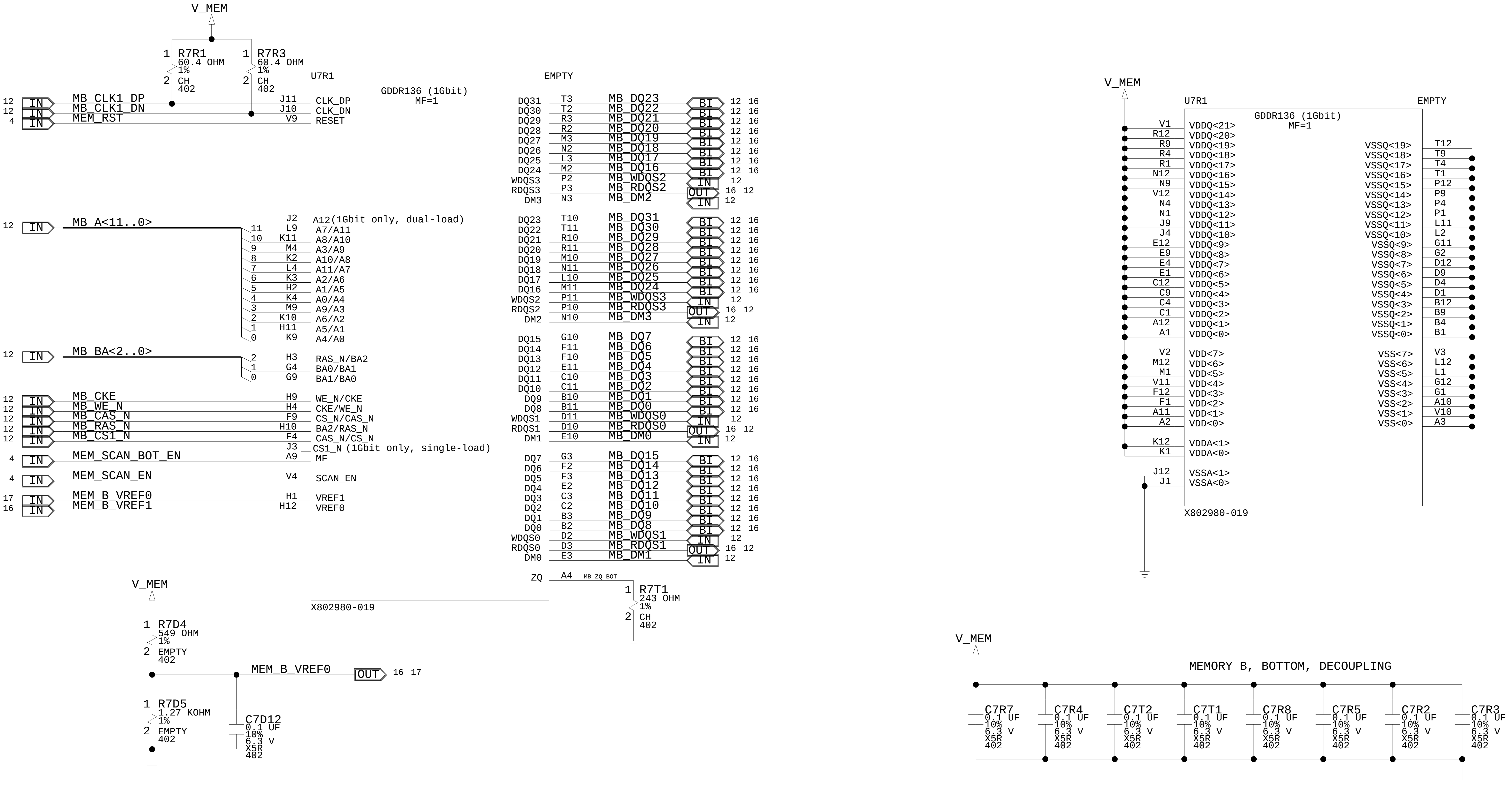
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	16/81	G	1.01

MEMORY PARTITION B, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1

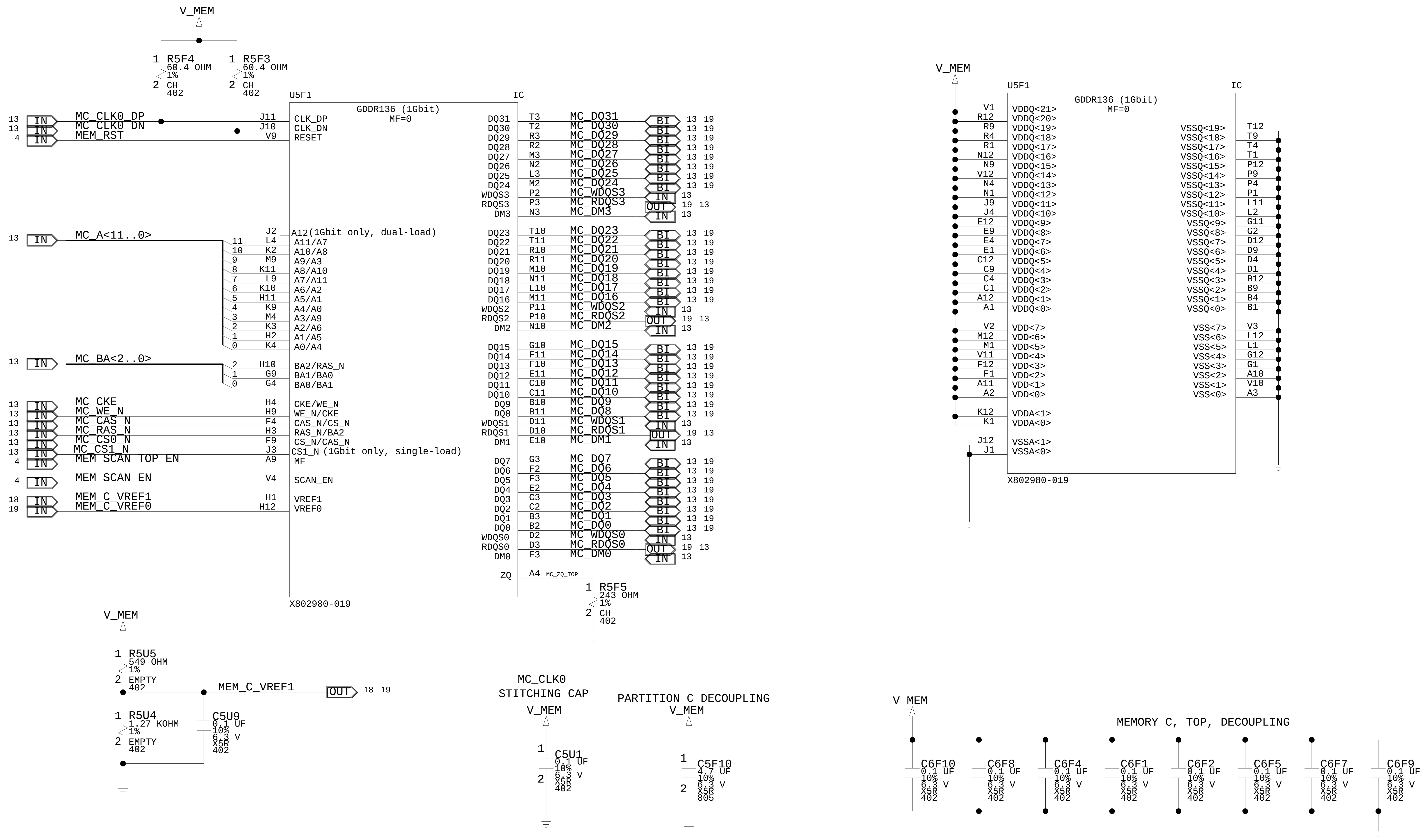

V_MEM
R7R1 60.4 OHM 1% CH 402
R7R3 60.4 OHM 1% CH 402
U7R1
EMPTY
GDDR136 (1Gbit) MF=1
12 IN MB_CLK1_DP J11 CLK_DP
12 IN MB_CLK1_DN J10 CLK_DN
4 IN MEM_RST V9 RESET
12 IN MB_A<11..0>
J2 A12(1Gbit only, dual-load)
11 L9 A7/A11
10 K11 A8/A10
9 M4 A3/A9
8 K2 A10/A8
7 L4 A11/A7
6 K3 A2/A6
5 H2 A1/A5
4 K4 A0/A4
3 M9 A9/A3
2 K10 A6/A2
1 H11 A5/A1
0 K9 A4/A0
12 IN MB_BA<2..0>
2 H3 RAS_N/BA2
1 G4 BA0/BA1
0 G9 BA1/BA0
12 IN MB_CKE H9 WE_N/CKE
12 IN MB_WE_N H4 CKE/WE_N
12 IN MB_CAS_N F9 CS_N/CAS_N
12 IN MB_RAS_N H10 BA2/RAS_N
12 IN MB_CS1_N F4 CAS_N/CS_N
J3 CS1_N (1Gbit only, single-load)
4 IN MEM_SCAN_BOT_EN A9 MF
4 IN MEM_SCAN_EN V4 SCAN_EN
17 IN MEM_B_VREF0 H1 VREF1
16 IN MEM_B_VREF1 H12 VREF0
DQ31 T3 MB_DQ23 BI 12 16
DQ30 T2 MB_DQ22 BI 12 16
DQ29 R3 MB_DQ21 BI 12 16
DQ28 R2 MB_DQ20 BI 12 16
DQ27 M3 MB_DQ19 BI 12 16
DQ26 N2 MB_DQ18 BI 12 16
DQ25 L3 MB_DQ17 BI 12 16
DQ24 M2 MB_DQ16 BI 12 16
WDQS3 P2 MB_WDQS2 IN 12
RDQS3 P3 MB_RDQS2 OUT 16 12
DM3 N3 MB_DM2 IN 12
DQ23 T10 MB_DQ31 BI 12 16
DQ22 T11 MB_DQ30 BI 12 16
DQ21 R10 MB_DQ29 BI 12 16
DQ20 R11 MB_DQ28 BI 12 16
DQ19 M10 MB_DQ27 BI 12 16
DQ18 N11 MB_DQ26 BI 12 16
DQ17 L10 MB_DQ25 BI 12 16
DQ16 M11 MB_DQ24 BI 12 16
WDQS2 P11 MB_WDQS3 IN 12
RDQS2 P10 MB_RDQS3 OUT 16 12
DM2 N10 MB_DM3 IN 12
DQ15 G10 MB_DQ7 BI 12 16
DQ14 F11 MB_DQ6 BI 12 16
DQ13 F10 MB_DQ5 BI 12 16
DQ12 E11 MB_DQ4 BI 12 16
DQ11 C10 MB_DQ3 BI 12 16
DQ10 C11 MB_DQ2 BI 12 16
DQ9 B10 MB_DQ1 BI 12 16
DQ8 B11 MB_DQ0 BI 12 16
WDQS1 D11 MB_WDQS0 IN 12
RDQS1 D10 MB_RDQS0 OUT 16 12
DM1 E10 MB_DM0 IN 12
DQ7 G3 MB_DQ15 BI 12 16
DQ6 F2 MB_DQ14 BI 12 16
DQ5 F3 MB_DQ13 BI 12 16
DQ4 E2 MB_DQ12 BI 12 16
DQ3 C3 MB_DQ11 BI 12 16
DQ2 C2 MB_DQ10 BI 12 16
DQ1 B3 MB_DQ9 BI 12 16
DQ0 B2 MB_DQ8 BI 12 16
WDQS0 D2 MB_WDQS1 IN 12
RDQS0 D3 MB_RDQS1 OUT 16 12
DM0 E3 MB_DM1 IN 12
ZQ A4 MB_ZQ_BOT
R7T1 243 OHM 1% CH 402
X802980-019
V_MEM
R7D4 549 OHM 1% EMPTY 402
MEM_B_VREF0 OUT 16 17
R7D5 1.27 KOHM 1% EMPTY 402
C7D12 0.1 UF 10% 6.3 V X5R 402
V_MEM
U7R1
EMPTY
GDDR136 (1Gbit) MF=1
V1 VDDQ<21>
R12 VDDQ<20>
R9 VDDQ<19>
R4 VDDQ<18>
R1 VDDQ<17>
N12 VDDQ<16>
N9 VDDQ<15>
V12 VDDQ<14>
N4 VDDQ<13>
N1 VDDQ<12>
J9 VDDQ<11>
J4 VDDQ<10>
E12 VDDQ<9>
E9 VDDQ<8>
E4 VDDQ<7>
E1 VDDQ<6>
C12 VDDQ<5>
C9 VDDQ<4>
C4 VDDQ<3>
C1 VDDQ<2>
A12 VDDQ<1>
A1 VDDQ<0>
V2 VDD<7>
M12 VDD<6>
M1 VDD<5>
V11 VDD<4>
F12 VDD<3>
F1 VDD<2>
A11 VDD<1>
A2 VDD<0>
K12 VDDA<1>
K1 VDDA<0>
J12 VSSA<1>
J1 VSSA<0>
VSSQ<19> T12
VSSQ<18> T9
VSSQ<17> T4
VSSQ<16> T1
VSSQ<15> P12
VSSQ<14> P9
VSSQ<13> P4
VSSQ<12> P1
VSSQ<11> L11
VSSQ<10> L2
VSSQ<9> G11
VSSQ<8> G2
VSSQ<7> D12
VSSQ<6> D9
VSSQ<5> D4
VSSQ<4> D1
VSSQ<3> B12
VSSQ<2> B9
VSSQ<1> B4
VSSQ<0> B1
VSS<7> V3
VSS<6> L12
VSS<5> L1
VSS<4> G12
VSS<3> G1
VSS<2> A10
VSS<1> V10
VSS<0> A3
X802980-019
V_MEM
MEMORY B, BOTTOM, DECOUPLING
C7R7 0.1 UF 10% 6.3 V X5R 402
C7R4 0.1 UF 10% 6.3 V X5R 402
C7T2 0.1 UF 10% 6.3 V X5R 402
C7T1 0.1 UF 10% 6.3 V X5R 402
C7R8 0.1 UF 10% 6.3 V X5R 402
C7R5 0.1 UF 10% 6.3 V X5R 402
C7R2 0.1 UF 10% 6.3 V X5R 402
C7R3 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARITION B, BOTTOM]

DRAWING	MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
Wed Feb 10 16:23:27 2010		TRINITY_XDK	17/81	G	1.01

MEMORY PARTITION C, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0


V_MEM
R5F4 60.4 OHM 1% CH 402
R5F3 60.4 OHM 1% CH 402
U5F1 IC
GDDR136 (1Gbit) MF=0
MC_CLK0_DP J11 CLK_DP
MC_CLK0_DN J10 CLK_DN
MEM_RST V9 RESET
MC_A<11..0>
A12(1Gbit only, dual-load)
A11/A7 A10/A8 A9/A3 A8/A10 A7/A11 A6/A2 A5/A1 A4/A0 A3/A9 A2/A6 A1/A5 A0/A4
MC_BA<2..0>
BA2/RAS_N BA1/BA0 BA0/BA1
MC_CKE H4 CKE/WE_N
MC_WE_N H9 WE_N/CKE
MC_CAS_N F4 CAS_N/CS_N
MC_RAS_N H3 RAS_N/BA2
MC_CS0_N F9 CS_N/CAS_N
MC_CS1_N J3 CS1_N (1Gbit only, single-load)
MEM_SCAN_TOP_EN A9 MF
MEM_SCAN_EN V4 SCAN_EN
MEM_C_VREF1 H1 VREF1
MEM_C_VREF0 H12 VREF0
IN
BI
OUT
MC_DQ31 … MC_DQ0
MC_WDQS3 MC_RDQS3 MC_DM3
MC_WDQS2 MC_RDQS2 MC_DM2
MC_WDQS1 MC_RDQS1 MC_DM1
MC_WDQS0 MC_RDQS0 MC_DM0
ZQ A4 MC_ZQ_TOP
R5F5 243 OHM 1% CH 402
X802980-019
VDDQ<21>…VDDQ<0>
VSSQ<19>…VSSQ<0>
VDD<7>…VDD<0>
VSS<7>…VSS<0>
VDDA<1> VDDA<0>
VSSA<1> VSSA<0>
R5U5 549 OHM 1% EMPTY 402
R5U4 1.27 KOHM 1% EMPTY 402
C5U9 0.1 UF 10% 6.3 V X5R 402
MEM_C_VREF1 OUT 18 19
MC_CLK0
STITCHING CAP
C5U1 0.1 UF 10% 6.3 V X5R 402
PARTITION C DECOUPLING
C5F10 4.7 UF 10% 6.3 V X5R 805
MEMORY C, TOP, DECOUPLING
C6F10 C6F8 C6F4 C6F1 C6F2 C6F5 C6F7 C6F9 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARTITION C, TOP]

DRAWING
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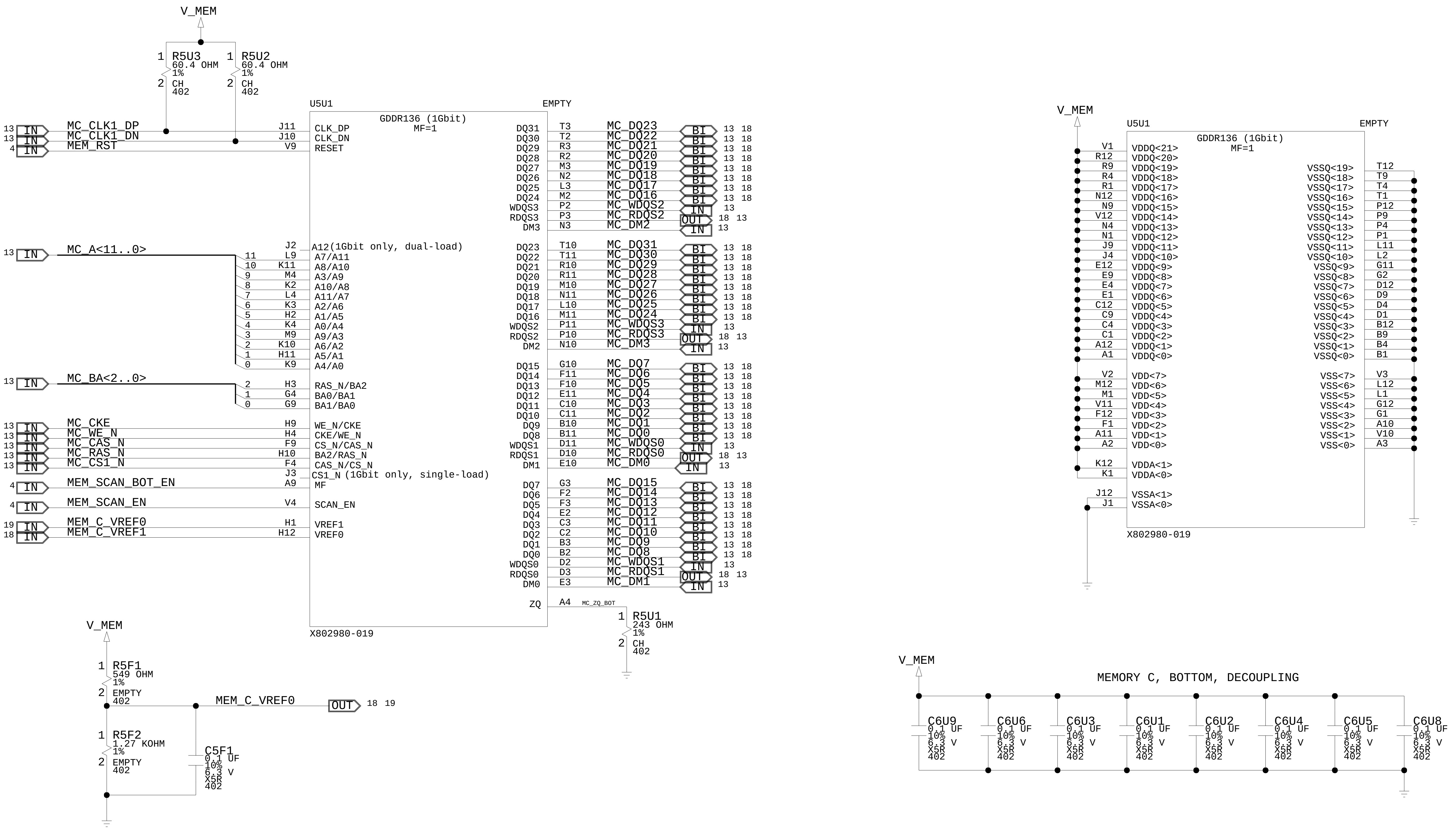
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	18/81	G	1.01

MEMORY PARTITION C, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1


V_MEM
R5U3
60.4 OHM
1%
CH
402
R5U2
60.4 OHM
1%
CH
402
U5U1
EMPTY
GDDR136 (1Gbit)
MF=1
13 IN MC_CLK1_DP J11 CLK_DP
13 IN MC_CLK1_DN J10 CLK_DN
4 IN MEM_RST V9 RESET
13 IN MC_A<11..0>
J2 A12(1Gbit only, dual-load)
11 L9 A7/A11
10 K11 A8/A10
9 M4 A3/A9
8 K2 A10/A8
7 L4 A11/A7
6 K3 A2/A6
5 H2 A1/A5
4 K4 A0/A4
3 M9 A9/A3
2 K10 A6/A2
1 H11 A5/A1
0 K9 A4/A0
13 IN MC_BA<2..0>
2 H3 RAS_N/BA2
1 G4 BA0/BA1
0 G9 BA1/BA0
13 IN MC_CKE H9 WE_N/CKE
13 IN MC_WE_N H4 CKE/WE_N
13 IN MC_CAS_N F9 CS_N/CAS_N
13 IN MC_RAS_N H10 BA2/RAS_N
13 IN MC_CS1_N F4 CAS_N/CS_N
J3 CS1_N (1Gbit only, single-load)
4 IN MEM_SCAN_BOT_EN A9 MF
4 IN MEM_SCAN_EN V4 SCAN_EN
19 IN MEM_C_VREF0 H1 VREF1
18 IN MEM_C_VREF1 H12 VREF0
X802980-019
DQ31 T3 MC_DQ23 BI 13 18
DQ30 T2 MC_DQ22 BI 13 18
DQ29 R3 MC_DQ21 BI 13 18
DQ28 R2 MC_DQ20 BI 13 18
DQ27 M3 MC_DQ19 BI 13 18
DQ26 N2 MC_DQ18 BI 13 18
DQ25 L3 MC_DQ17 BI 13 18
DQ24 M2 MC_DQ16 BI 13 18
WDQS3 P2 MC_WDQS2 IN 13
RDQS3 P3 MC_RDQS2 OUT 18 13
DM3 N3 MC_DM2 IN 13
DQ23 T10 MC_DQ31 BI 13 18
DQ22 T11 MC_DQ30 BI 13 18
DQ21 R10 MC_DQ29 BI 13 18
DQ20 R11 MC_DQ28 BI 13 18
DQ19 M10 MC_DQ27 BI 13 18
DQ18 N11 MC_DQ26 BI 13 18
DQ17 L10 MC_DQ25 BI 13 18
DQ16 M11 MC_DQ24 BI 13 18
WDQS2 P11 MC_WDQS3 IN 13
RDQS2 P10 MC_RDQS3 OUT 18 13
DM2 N10 MC_DM3 IN 13
DQ15 G10 MC_DQ7 BI 13 18
DQ14 F11 MC_DQ6 BI 13 18
DQ13 F10 MC_DQ5 BI 13 18
DQ12 E11 MC_DQ4 BI 13 18
DQ11 C10 MC_DQ3 BI 13 18
DQ10 C11 MC_DQ2 BI 13 18
DQ9 B10 MC_DQ1 BI 13 18
DQ8 B11 MC_DQ0 BI 13 18
WDQS1 D11 MC_WDQS0 IN 13
RDQS1 D10 MC_RDQS0 OUT 18 13
DM1 E10 MC_DM0 IN 13
DQ7 G3 MC_DQ15 BI 13 18
DQ6 F2 MC_DQ14 BI 13 18
DQ5 F3 MC_DQ13 BI 13 18
DQ4 E2 MC_DQ12 BI 13 18
DQ3 C3 MC_DQ11 BI 13 18
DQ2 C2 MC_DQ10 BI 13 18
DQ1 B3 MC_DQ9 BI 13 18
DQ0 B2 MC_DQ8 BI 13 18
WDQS0 D2 MC_WDQS1 IN 13
RDQS0 D3 MC_RDQS1 OUT 18 13
DM0 E3 MC_DM1 IN 13
ZQ A4 MC_ZQ_BOT
R5U1
243 OHM
1%
CH
402
V_MEM
R5F1
549 OHM
1%
EMPTY
402
MEM_C_VREF0 OUT 18 19
R5F2
1.27 KOHM
1%
EMPTY
402
C5F1
0.1 UF
10%
6.3 V
X5R
402
V_MEM
U5U1
EMPTY
GDDR136 (1Gbit)
MF=1
V1 VDDQ<21>
R12 VDDQ<20>
R9 VDDQ<19>
R4 VDDQ<18>
R1 VDDQ<17>
N12 VDDQ<16>
N9 VDDQ<15>
V12 VDDQ<14>
N4 VDDQ<13>
N1 VDDQ<12>
J9 VDDQ<11>
J4 VDDQ<10>
E12 VDDQ<9>
E9 VDDQ<8>
E4 VDDQ<7>
E1 VDDQ<6>
C12 VDDQ<5>
C9 VDDQ<4>
C4 VDDQ<3>
C1 VDDQ<2>
A12 VDDQ<1>
A1 VDDQ<0>
V2 VDD<7>
M12 VDD<6>
M1 VDD<5>
V11 VDD<4>
F12 VDD<3>
F1 VDD<2>
A11 VDD<1>
A2 VDD<0>
K12 VDDA<1>
K1 VDDA<0>
J12 VSSA<1>
J1 VSSA<0>
VSSQ<19> T12
VSSQ<18> T9
VSSQ<17> T4
VSSQ<16> T1
VSSQ<15> P12
VSSQ<14> P9
VSSQ<13> P4
VSSQ<12> P1
VSSQ<11> L11
VSSQ<10> L2
VSSQ<9> G11
VSSQ<8> G2
VSSQ<7> D12
VSSQ<6> D9
VSSQ<5> D4
VSSQ<4> D1
VSSQ<3> B12
VSSQ<2> B9
VSSQ<1> B4
VSSQ<0> B1
VSS<7> V3
VSS<6> L12
VSS<5> L1
VSS<4> G12
VSS<3> G1
VSS<2> A10
VSS<1> V10
VSS<0> A3
X802980-019
V_MEM
MEMORY C, BOTTOM, DECOUPLING
C6U9 0.1 UF 10% 6.3 V X5R 402
C6U6 0.1 UF 10% 6.3 V X5R 402
C6U3 0.1 UF 10% 6.3 V X5R 402
C6U1 0.1 UF 10% 6.3 V X5R 402
C6U2 0.1 UF 10% 6.3 V X5R 402
C6U4 0.1 UF 10% 6.3 V X5R 402
C6U5 0.1 UF 10% 6.3 V X5R 402
C6U8 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARITION C, BOTTOM]

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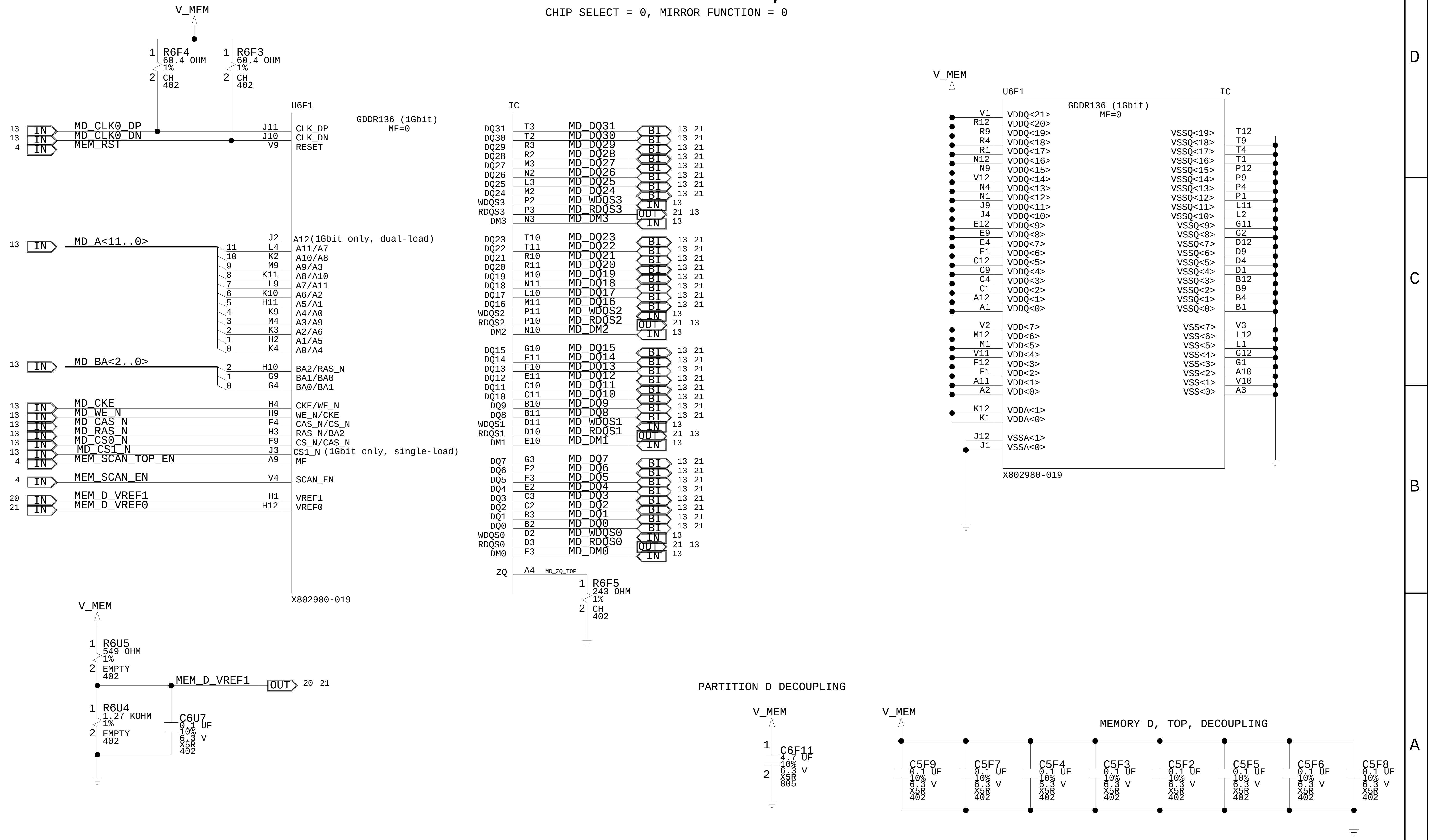
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 19/81	FAB G	REV 1.01

MEMORY PARTITION D, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0


V_MEM
R6F4 60.4 OHM 1% CH 402
R6F3 60.4 OHM 1% CH 402
U6F1
IC
GDDR136 (1Gbit)
MF=0
13 IN MD_CLK0_DP J11 CLK_DP
13 IN MD_CLK0_DN J10 CLK_DN
4 IN MEM_RST V9 RESET
13 IN MD_A<11..0>
J2 A12(1Gbit only, dual-load)
11 L4 A11/A7
10 K2 A10/A8
9 M9 A9/A3
8 K11 A8/A10
7 L9 A7/A11
6 K10 A6/A2
5 H11 A5/A1
4 K9 A4/A0
3 M4 A3/A9
2 K3 A2/A6
1 H2 A1/A5
0 K4 A0/A4
13 IN MD_BA<2..0>
2 H10 BA2/RAS_N
1 G9 BA1/BA0
0 G4 BA0/BA1
13 IN MD_CKE H4 CKE/WE_N
13 IN MD_WE_N H9 WE_N/CKE
13 IN MD_CAS_N F4 CAS_N/CS_N
13 IN MD_RAS_N H3 RAS_N/BA2
13 IN MD_CS0_N F9 CS_N/CAS_N
13 IN MD_CS1_N J3 CS1_N (1Gbit only, single-load)
4 IN MEM_SCAN_TOP_EN A9 MF
4 IN MEM_SCAN_EN V4 SCAN_EN
20 IN MEM_D_VREF1 H1 VREF1
21 IN MEM_D_VREF0 H12 VREF0
X802980-019
DQ31 T3 MD_DQ31 BI 13 21
DQ30 T2 MD_DQ30 BI 13 21
DQ29 R3 MD_DQ29 BI 13 21
DQ28 R2 MD_DQ28 BI 13 21
DQ27 M3 MD_DQ27 BI 13 21
DQ26 N2 MD_DQ26 BI 13 21
DQ25 L3 MD_DQ25 BI 13 21
DQ24 M2 MD_DQ24 BI 13 21
WDQS3 P2 MD_WDQS3 IN 13
RDQS3 P3 MD_RDQS3 OUT 21 13
DM3 N3 MD_DM3 IN 13
DQ23 T10 MD_DQ23 BI 13 21
DQ22 T11 MD_DQ22 BI 13 21
DQ21 R10 MD_DQ21 BI 13 21
DQ20 R11 MD_DQ20 BI 13 21
DQ19 M10 MD_DQ19 BI 13 21
DQ18 N11 MD_DQ18 BI 13 21
DQ17 L10 MD_DQ17 BI 13 21
DQ16 M11 MD_DQ16 BI 13 21
WDQS2 P11 MD_WDQS2 IN 13
RDQS2 P10 MD_RDQS2 OUT 21 13
DM2 N10 MD_DM2 IN 13
DQ15 G10 MD_DQ15 BI 13 21
DQ14 F11 MD_DQ14 BI 13 21
DQ13 F10 MD_DQ13 BI 13 21
DQ12 E11 MD_DQ12 BI 13 21
DQ11 C10 MD_DQ11 BI 13 21
DQ10 C11 MD_DQ10 BI 13 21
DQ9 B10 MD_DQ9 BI 13 21
DQ8 B11 MD_DQ8 BI 13 21
WDQS1 D11 MD_WDQS1 IN 13
RDQS1 D10 MD_RDQS1 OUT 21 13
DM1 E10 MD_DM1 IN 13
DQ7 G3 MD_DQ7 BI 13 21
DQ6 F2 MD_DQ6 BI 13 21
DQ5 F3 MD_DQ5 BI 13 21
DQ4 E2 MD_DQ4 BI 13 21
DQ3 C3 MD_DQ3 BI 13 21
DQ2 C2 MD_DQ2 BI 13 21
DQ1 B3 MD_DQ1 BI 13 21
DQ0 B2 MD_DQ0 BI 13 21
WDQS0 D2 MD_WDQS0 IN 13
RDQS0 D3 MD_RDQS0 OUT 21 13
DM0 E3 MD_DM0 IN 13
ZQ A4 MD_ZQ_TOP
R6F5 243 OHM 1% CH 402
V_MEM
U6F1
IC
GDDR136 (1Gbit)
MF=0
V1 VDDQ<21>
R12 VDDQ<20>
R9 VDDQ<19>
R4 VDDQ<18>
R1 VDDQ<17>
N12 VDDQ<16>
N9 VDDQ<15>
V12 VDDQ<14>
N4 VDDQ<13>
N1 VDDQ<12>
J9 VDDQ<11>
J4 VDDQ<10>
E12 VDDQ<9>
E9 VDDQ<8>
E4 VDDQ<7>
E1 VDDQ<6>
C12 VDDQ<5>
C9 VDDQ<4>
C4 VDDQ<3>
C1 VDDQ<2>
A12 VDDQ<1>
A1 VDDQ<0>
V2 VDD<7>
M12 VDD<6>
M1 VDD<5>
V11 VDD<4>
F12 VDD<3>
F1 VDD<2>
A11 VDD<1>
A2 VDD<0>
K12 VDDA<1>
K1 VDDA<0>
J12 VSSA<1>
J1 VSSA<0>
VSSQ<19> T12
VSSQ<18> T9
VSSQ<17> T4
VSSQ<16> T1
VSSQ<15> P12
VSSQ<14> P9
VSSQ<13> P4
VSSQ<12> P1
VSSQ<11> L11
VSSQ<10> L2
VSSQ<9> G11
VSSQ<8> G2
VSSQ<7> D12
VSSQ<6> D9
VSSQ<5> D4
VSSQ<4> D1
VSSQ<3> B12
VSSQ<2> B9
VSSQ<1> B4
VSSQ<0> B1
VSS<7> V3
VSS<6> L12
VSS<5> L1
VSS<4> G12
VSS<3> G1
VSS<2> A10
VSS<1> V10
VSS<0> A3
X802980-019
V_MEM
R6U5 549 OHM 1% EMPTY 402
MEM_D_VREF1 OUT 20 21
R6U4 1.27 KOHM 1% EMPTY 402
C6U7 0.1 UF 10% 6.3 V X5R 402
PARTITION D DECOUPLING
V_MEM
C6F11 4.7 UF 10% 6.3 V X5R 805
V_MEM
MEMORY D, TOP, DECOUPLING
C5F9 0.1 UF 10% 6.3 V X5R 402
C5F7 0.1 UF 10% 6.3 V X5R 402
C5F4 0.1 UF 10% 6.3 V X5R 402
C5F3 0.1 UF 10% 6.3 V X5R 402
C5F2 0.1 UF 10% 6.3 V X5R 402
C5F5 0.1 UF 10% 6.3 V X5R 402
C5F6 0.1 UF 10% 6.3 V X5R 402
C5F8 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARTITION D, TOP]

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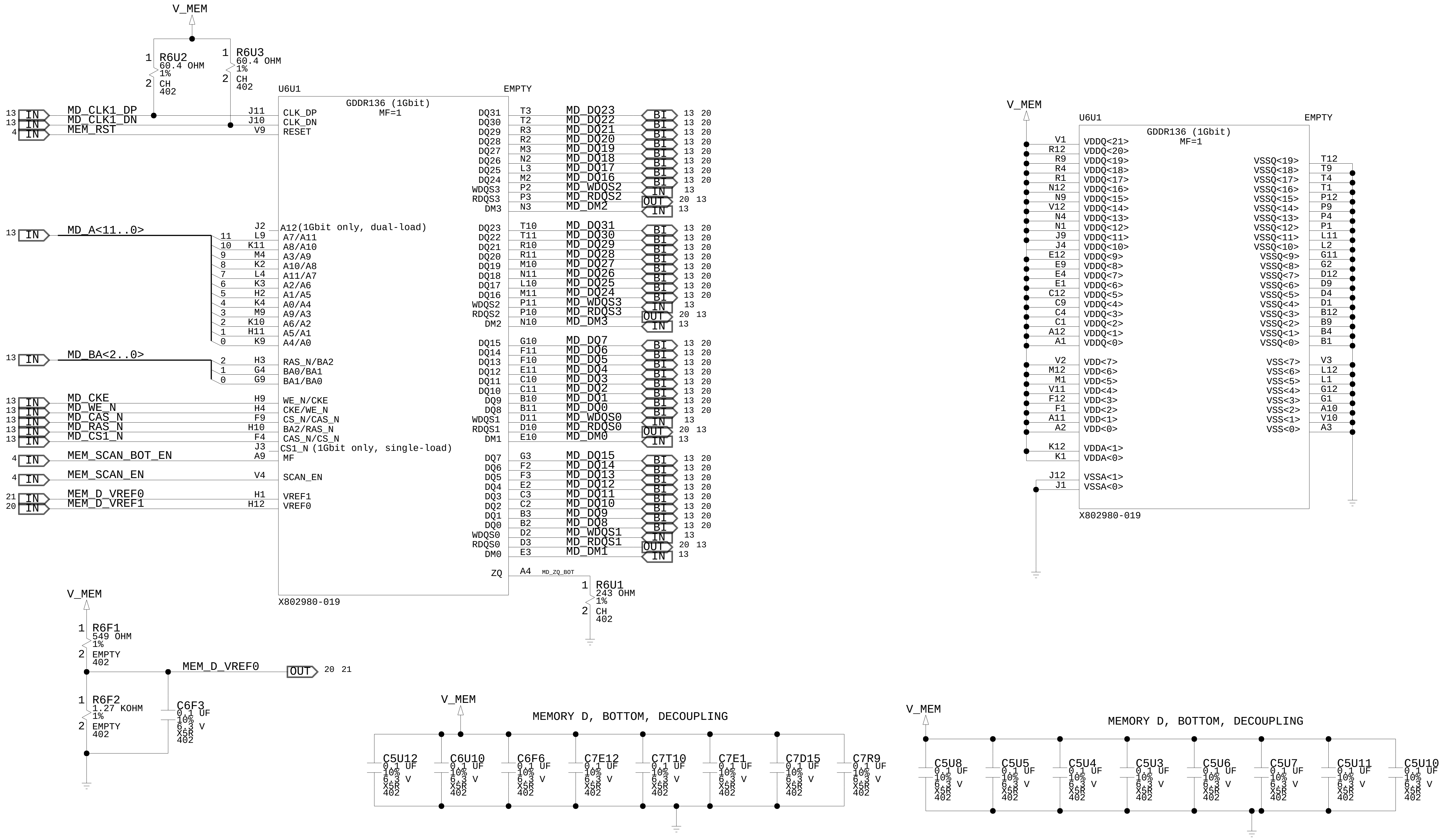
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	20/81	G	1.01

MEMORY PARTITION D, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1


V_MEM
R6U2 60.4 OHM 1% CH 402
R6U3 60.4 OHM 1% CH 402
U6U1
EMPTY
GDDR136 (1Gbit)
MF=1
MD_CLK1_DP
MD_CLK1_DN
MEM_RST
CLK_DP
CLK_DN
RESET
MD_A<11..0>
A12(1Gbit only, dual-load)
A7/A11
A8/A10
A3/A9
A10/A8
A11/A7
A2/A6
A1/A5
A0/A4
A9/A3
A6/A2
A5/A1
A4/A0
MD_BA<2..0>
RAS_N/BA2
BA0/BA1
BA1/BA0
MD_CKE
MD_WE_N
MD_CAS_N
MD_RAS_N
MD_CS1_N
WE_N/CKE
CKE/WE_N
CS_N/CAS_N
BA2/RAS_N
CAS_N/CS_N
CS1_N (1Gbit only, single-load)
MEM_SCAN_BOT_EN
MF
MEM_SCAN_EN
SCAN_EN
MEM_D_VREF0
MEM_D_VREF1
VREF1
VREF0
X802980-019
MD_DQ23
MD_DQ22
MD_DQ21
MD_DQ20
MD_DQ19
MD_DQ18
MD_DQ17
MD_DQ16
MD_WDQS2
MD_RDQS2
MD_DM2
MD_DQ31
MD_DQ30
MD_DQ29
MD_DQ28
MD_DQ27
MD_DQ26
MD_DQ25
MD_DQ24
MD_WDQS3
MD_RDQS3
MD_DM3
MD_DQ7
MD_DQ6
MD_DQ5
MD_DQ4
MD_DQ3
MD_DQ2
MD_DQ1
MD_DQ0
MD_WDQS0
MD_RDQS0
MD_DM0
MD_DQ15
MD_DQ14
MD_DQ13
MD_DQ12
MD_DQ11
MD_DQ10
MD_DQ9
MD_DQ8
MD_WDQS1
MD_RDQS1
MD_DM1
ZQ
MD_ZQ_BOT
R6U1 243 OHM 1% CH 402
VDDQ<21>…VDDQ<0>
VSSQ<19>…VSSQ<0>
VDD<7>…VDD<0>
VSS<7>…VSS<0>
VDDA<1>
VDDA<0>
VSSA<1>
VSSA<0>
R6F1 549 OHM 1% EMPTY 402
R6F2 1.27 KOHM 1% EMPTY 402
C6F3 0.1 UF 10% 6.3 V X5R 402
MEM_D_VREF0
OUT 20 21
MEMORY D, BOTTOM, DECOUPLING
C5U12
C6U10
C6F6
C7E12
C7T10
C7E1
C7D15
C7R9
0.1 UF 10% 6.3 V X5R 402
MEMORY D, BOTTOM, DECOUPLING
C5U8
C5U5
C5U4
C5U3
C5U6
C5U7
C5U11
C5U10
0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARTITION D, BOTTOM]

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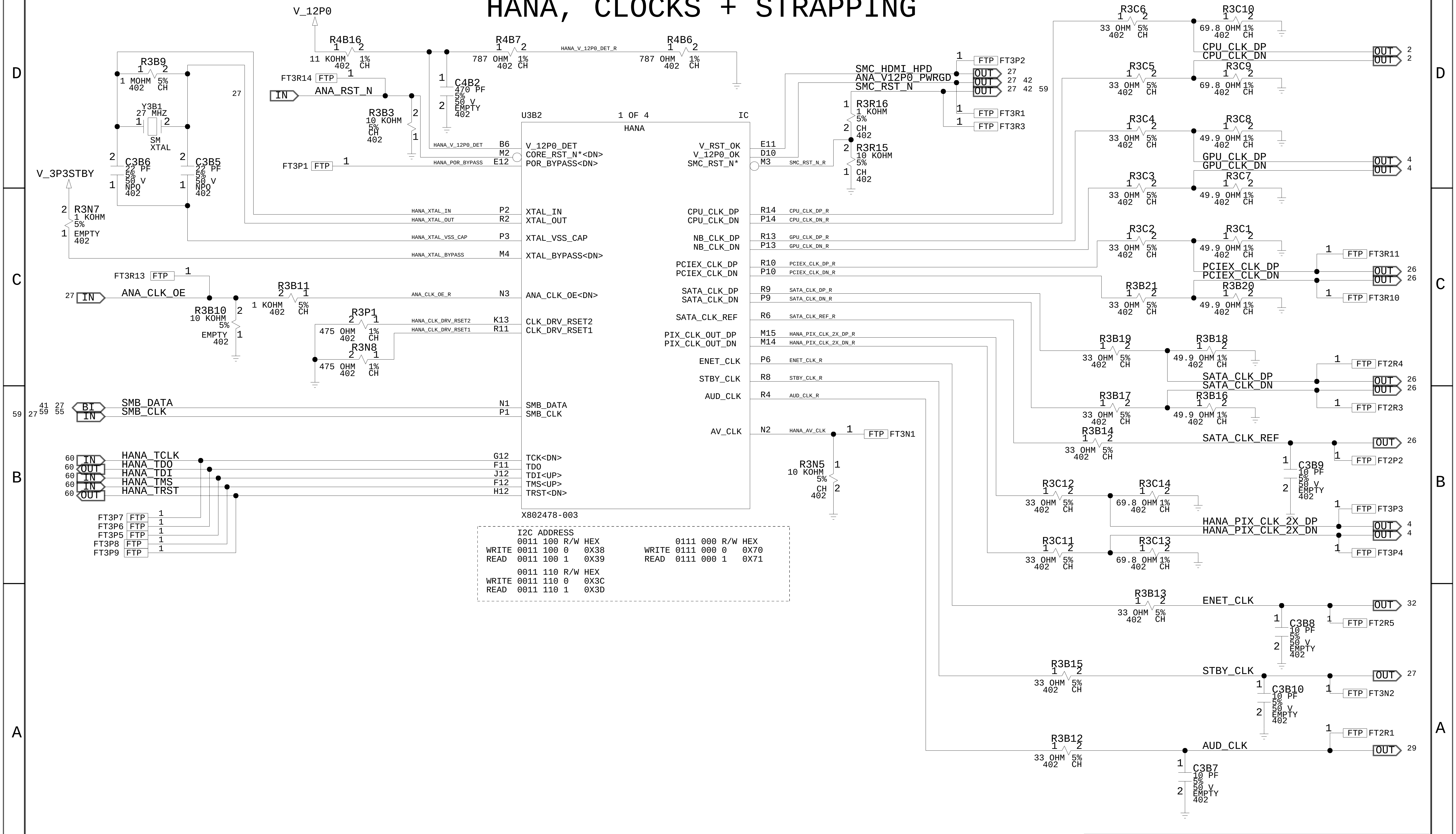
MICROSOFT CONFIDENTIAL

PROJECT NAME	PAGE	FAB	REV
TRINITY_XDK	21/81	G	1.01

HANA, CLOCKS + STRAPPING


V_12P0
R4B16
11 KOHM 1% 402 CH
R4B7
787 OHM 1% 402 CH
HANA_V_12P0_DET_R
R4B6
787 OHM 1% 402 CH
C4B2
470 PF 5% 50 V EMPTY 402
FT3R14 FTP
IN ANA_RST_N
R3B3
10 KOHM 5% CH 402
R3B9
1 MOHM 5% 402 CH
Y3B1
27 MHZ
SM XTAL
C3B6
22 PF 5% 50 V NPO 402
C3B5
22 PF 5% 50 V NPO 402
V_3P3STBY
R3N7
1 KOHM 5% EMPTY 402
FT3P1 FTP
U3B2
1 OF 4
IC
HANA
HANA_V_12P0_DET B6 V_12P0_DET
M2 CORE_RST_N*<DN>
HANA_POR_BYPASS E12 POR_BYPASS<DN>
HANA_XTAL_IN P2 XTAL_IN
HANA_XTAL_OUT R2 XTAL_OUT
HANA_XTAL_VSS_CAP P3 XTAL_VSS_CAP
HANA_XTAL_BYPASS M4 XTAL_BYPASS<DN>
ANA_CLK_OE_R N3 ANA_CLK_OE<DN>
HANA_CLK_DRV_RSET2 K13 CLK_DRV_RSET2
HANA_CLK_DRV_RSET1 R11 CLK_DRV_RSET1
N1 SMB_DATA
P1 SMB_CLK
G12 TCK<DN>
F11 TDO
J12 TDI<UP>
F12 TMS<UP>
H12 TRST<DN>
X802478-003
V_RST_OK E11
V_12P0_OK D10
SMC_RST_N* M3 SMC_RST_N_R
CPU_CLK_DP R14 CPU_CLK_DP_R
CPU_CLK_DN P14 CPU_CLK_DN_R
NB_CLK_DP R13 GPU_CLK_DP_R
NB_CLK_DN P13 GPU_CLK_DN_R
PCIEX_CLK_DP R10 PCIEX_CLK_DP_R
PCIEX_CLK_DN P10 PCIEX_CLK_DN_R
SATA_CLK_DP R9 SATA_CLK_DP_R
SATA_CLK_DN P9 SATA_CLK_DN_R
SATA_CLK_REF R6 SATA_CLK_REF_R
PIX_CLK_OUT_DP M15 HANA_PIX_CLK_2X_DP_R
PIX_CLK_OUT_DN M14 HANA_PIX_CLK_2X_DN_R
ENET_CLK P6 ENET_CLK_R
STBY_CLK R8 STBY_CLK_R
AUD_CLK R4 AUD_CLK_R
AV_CLK N2 HANA_AV_CLK
FTP FT3N1
R3N5
10 KOHM 5% CH 402
SMC_HDMI_HPD OUT 27
ANA_V12P0_PWRGD OUT 27 42
SMC_RST_N OUT 27 42 59
FTP FT3P2
FTP FT3R1
FTP FT3R3
R3R16
1 KOHM 5% CH 402
R3R15
10 KOHM 5% CH 402
FT3R13 FTP
27 IN ANA_CLK_OE
R3B11
1 KOHM 5% 402 CH
R3B10
10 KOHM 5% EMPTY 402
R3P1
475 OHM 1% 402 CH
R3N8
475 OHM 1% 402 CH
59 27 41 27 59 55 BI SMB_DATA
IN SMB_CLK
60 IN HANA_TCLK
60 OUT HANA_TDO
60 IN HANA_TDI
60 IN HANA_TMS
60 OUT HANA_TRST
FT3P7 FTP
FT3P6 FTP
FT3P5 FTP
FT3P8 FTP
FT3P9 FTP
R3C6
33 OHM 5% 402 CH
R3C10
69.8 OHM 1% 402 CH
CPU_CLK_DP OUT 2
CPU_CLK_DN OUT 2
R3C5
33 OHM 5% 402 CH
R3C9
69.8 OHM 1% 402 CH
R3C4
33 OHM 5% 402 CH
R3C8
49.9 OHM 1% 402 CH
GPU_CLK_DP OUT 4
GPU_CLK_DN OUT 4
R3C3
33 OHM 5% 402 CH
R3C7
49.9 OHM 1% 402 CH
R3C2
33 OHM 5% 402 CH
R3C1
49.9 OHM 1% 402 CH
FTP FT3R11
PCIEX_CLK_DP OUT 26
PCIEX_CLK_DN OUT 26
R3B21
33 OHM 5% 402 CH
R3B20
49.9 OHM 1% 402 CH
FTP FT3R10
R3B19
33 OHM 5% 402 CH
R3B18
49.9 OHM 1% 402 CH
FTP FT2R4
SATA_CLK_DP OUT 26
SATA_CLK_DN OUT 26
R3B17
33 OHM 5% 402 CH
R3B16
49.9 OHM 1% 402 CH
FTP FT2R3
R3B14
33 OHM 5% 402 CH
SATA_CLK_REF OUT 26
C3B9
10 PF 5% 50 V EMPTY 402
FTP FT2P2
R3C12
33 OHM 5% 402 CH
R3C14
69.8 OHM 1% 402 CH
FTP FT3P3
HANA_PIX_CLK_2X_DP OUT 4
HANA_PIX_CLK_2X_DN OUT 4
R3C11
33 OHM 5% 402 CH
R3C13
69.8 OHM 1% 402 CH
FTP FT3P4
R3B13
33 OHM 5% 402 CH
ENET_CLK OUT 32
C3B8
10 PF 5% 50 V EMPTY 402
FTP FT2R5
R3B15
33 OHM 5% 402 CH
STBY_CLK OUT 27
C3B10
10 PF 5% 50 V EMPTY 402
FTP FT3N2
R3B12
33 OHM 5% 402 CH
AUD_CLK OUT 29
FTP FT2R1
C3B7
10 PF 5% 50 V EMPTY 402

```
      I2C ADDRESS
      0011 100 R/W HEX           0111 000 R/W HEX
WRITE 0011 100 0   0X38    WRITE 0111 000 0   0X70
READ  0011 100 1   0X39    READ  0111 000 1   0X71

      0011 110 R/W HEX
WRITE 0011 110 0   0X3C
READ  0011 110 1   0X3D
```

[PAGE_TITLE=HANA, CLOCKS + STRAPING, JTAG]

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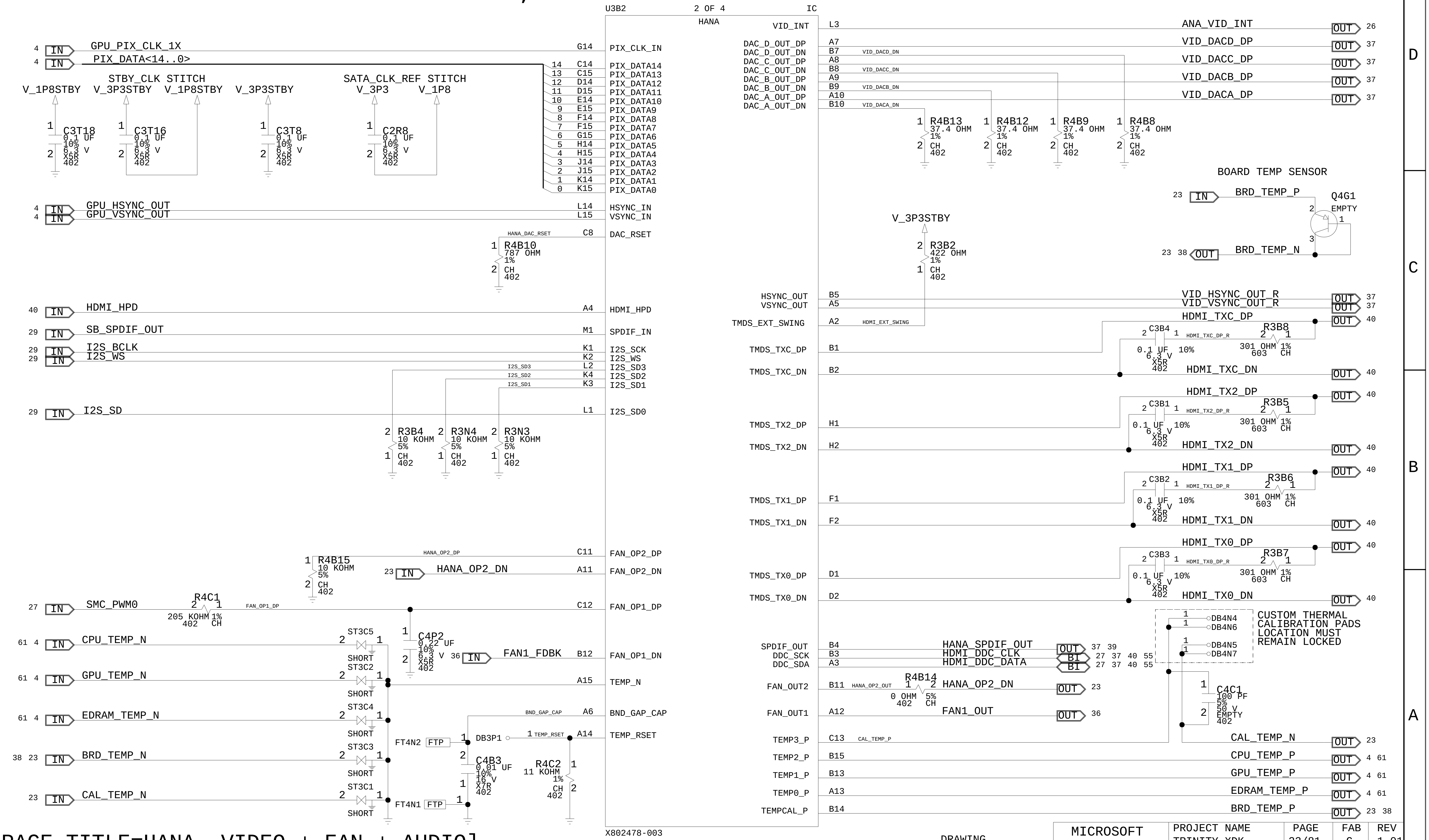
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 22/81	FAB G	REV 1.01

HANA, VIDEO + FAN + AUDIO


U3B2
2 OF 4
IC
HANA
X802478-003
GPU_PIX_CLK_1X
PIX_DATA<14..0>
STBY_CLK STITCH
SATA_CLK_REF STITCH
V_1P8STBY
V_3P3STBY
V_1P8STBY
V_3P3STBY
V_3P3
V_1P8
C3T18 0.1 UF 10% 6.3 V X5R 402
C3T16 0.1 UF 10% 6.3 V X5R 402
C3T8 0.1 UF 10% 6.3 V X5R 402
C2R8 0.1 UF 10% 6.3 V X5R 402
G14 PIX_CLK_IN
C14 PIX_DATA14
C15 PIX_DATA13
D14 PIX_DATA12
D15 PIX_DATA11
E14 PIX_DATA10
E15 PIX_DATA9
F14 PIX_DATA8
F15 PIX_DATA7
G15 PIX_DATA6
H14 PIX_DATA5
H15 PIX_DATA4
J14 PIX_DATA3
J15 PIX_DATA2
K14 PIX_DATA1
K15 PIX_DATA0
GPU_HSYNC_OUT
GPU_VSYNC_OUT
L14 HSYNC_IN
L15 VSYNC_IN
HANA_DAC_RSET
C8 DAC_RSET
R4B10 787 OHM 1% CH 402
HDMI_HPD
A4 HDMI_HPD
SB_SPDIF_OUT
M1 SPDIF_IN
I2S_BCLK
I2S_WS
K1 I2S_SCK
K2 I2S_WS
L2 I2S_SD3
K4 I2S_SD2
K3 I2S_SD1
I2S_SD
L1 I2S_SD0
R3B4 10 KOHM 5% CH 402
R3N4 10 KOHM 5% CH 402
R3N3 10 KOHM 5% CH 402
R4B15 10 KOHM 5% CH 402
HANA_OP2_DP
C11 FAN_OP2_DP
HANA_OP2_DN
A11 FAN_OP2_DN
SMC_PWM0
R4C1 205 KOHM 1% 402 CH
FAN_OP1_DP
C12 FAN_OP1_DP
C4P2 0.22 UF 10% 6.3 V X5R 402
FAN1_FDBK
B12 FAN_OP1_DN
CPU_TEMP_N
GPU_TEMP_N
EDRAM_TEMP_N
BRD_TEMP_N
CAL_TEMP_N
ST3C5 SHORT
ST3C2 SHORT
ST3C4 SHORT
ST3C3 SHORT
ST3C1 SHORT
A15 TEMP_N
BND_GAP_CAP
A6 BND_GAP_CAP
FT4N2 FTP
FT4N1 FTP
DB3P1
TEMP_RSET
A14 TEMP_RSET
C4B3 0.01 UF 10% 16 V X7R 402
R4C2 11 KOHM 1% CH 402
VID_INT L3
DAC_D_OUT_DP A7
DAC_D_OUT_DN B7
DAC_C_OUT_DP A8
DAC_C_OUT_DN B8
DAC_B_OUT_DP A9
DAC_B_OUT_DN B9
DAC_A_OUT_DP A10
DAC_A_OUT_DN B10
VID_DACD_DN
VID_DACC_DN
VID_DACB_DN
VID_DACA_DN
ANA_VID_INT 26
VID_DACD_DP 37
VID_DACC_DP 37
VID_DACB_DP 37
VID_DACA_DP 37
R4B13 37.4 OHM 1% CH 402
R4B12 37.4 OHM 1% CH 402
R4B9 37.4 OHM 1% CH 402
R4B8 37.4 OHM 1% CH 402
BOARD TEMP SENSOR
BRD_TEMP_P
Q4G1 EMPTY
BRD_TEMP_N
V_3P3STBY
R3B2 422 OHM 1% CH 402
HSYNC_OUT B5
VSYNC_OUT A5
TMDS_EXT_SWING A2
HDMI_EXT_SWING
VID_HSYNC_OUT_R 37
VID_VSYNC_OUT_R 37
TMDS_TXC_DP B1
TMDS_TXC_DN B2
HDMI_TXC_DP 40
C3B4 0.1 UF 10% 6.3 V X5R 402
HDMI_TXC_DP_R
R3B8 301 OHM 1% 603 CH
HDMI_TXC_DN 40
TMDS_TX2_DP H1
TMDS_TX2_DN H2
HDMI_TX2_DP 40
C3B1 0.1 UF 10% 6.3 V X5R 402
HDMI_TX2_DP_R
R3B5 301 OHM 1% 603 CH
HDMI_TX2_DN 40
TMDS_TX1_DP F1
TMDS_TX1_DN F2
HDMI_TX1_DP 40
C3B2 0.1 UF 10% 6.3 V X5R 402
HDMI_TX1_DP_R
R3B6 301 OHM 1% 603 CH
HDMI_TX1_DN 40
TMDS_TX0_DP D1
TMDS_TX0_DN D2
HDMI_TX0_DP 40
C3B3 0.1 UF 10% 6.3 V X5R 402
HDMI_TX0_DP_R
R3B7 301 OHM 1% 603 CH
HDMI_TX0_DN 40
DB4N4
DB4N6
DB4N5
DB4N7
CUSTOM THERMAL CALIBRATION PADS LOCATION MUST REMAIN LOCKED
SPDIF_OUT B4
DDC_SCK B3
DDC_SDA A3
HANA_SPDIF_OUT 37 39
HDMI_DDC_CLK 27 37 40 55
HDMI_DDC_DATA 27 37 40 55
FAN_OUT2 B11
HANA_OP2_OUT
R4B14 0 OHM 5% 402 CH
HANA_OP2_DN 23
FAN_OUT1 A12
FAN1_OUT 36
C4C1 100 PF 5% 50 V EMPTY 402
TEMP3_P C13
CAL_TEMP_P
TEMP2_P B15
TEMP1_P B13
TEMP0_P A13
TEMPCAL_P B14
CAL_TEMP_N 23
CPU_TEMP_P 4 61
GPU_TEMP_P 4 61
EDRAM_TEMP_P 4 61
BRD_TEMP_P 23 38
IN
OUT
BI

[PAGE_TITLE=HANA, VIDEO + FAN + AUDIO]

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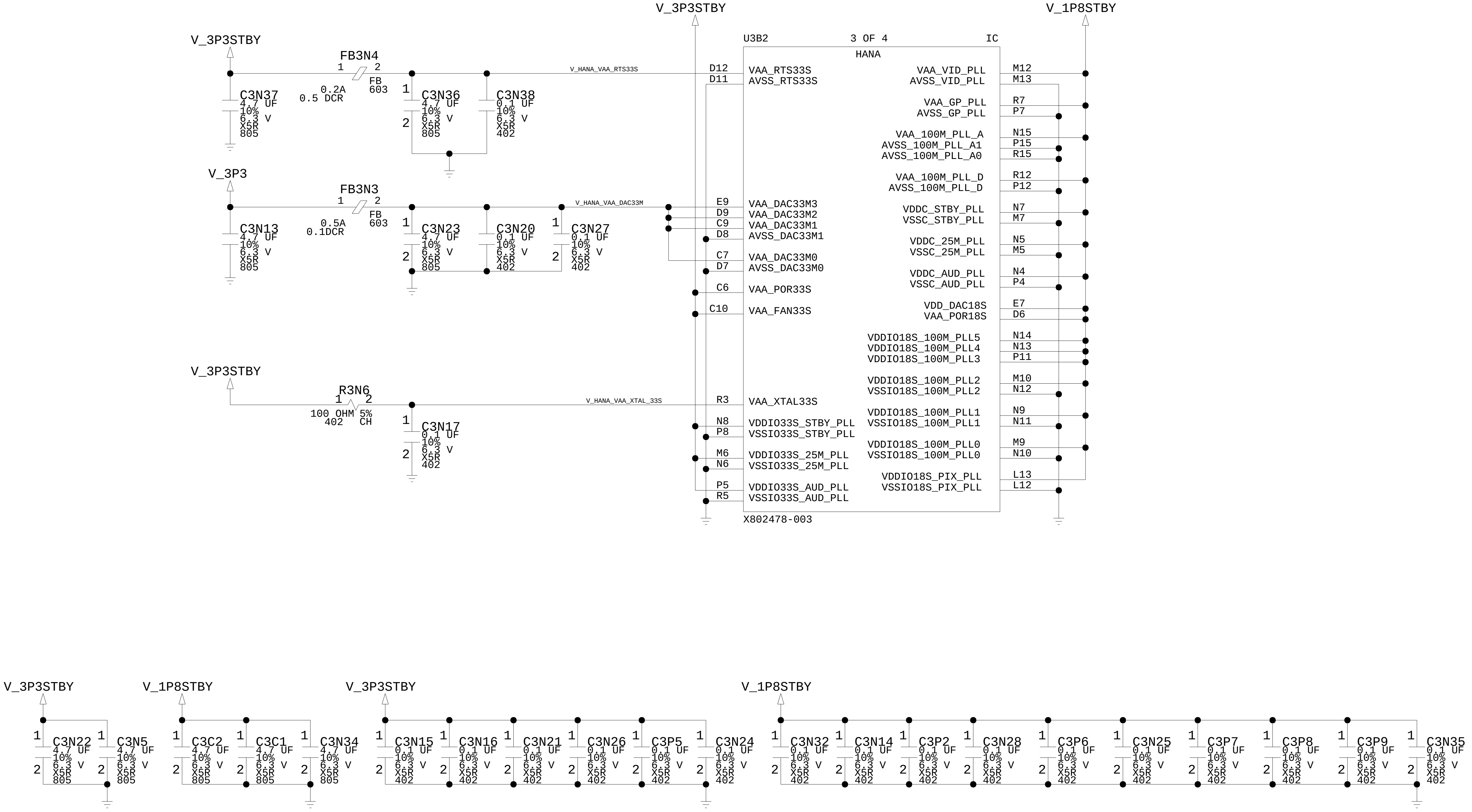
PROJECT NAME	PAGE	FAB	REV
TRINITY_XDK	23/81	G	1.01

HANA, POWER + DECOUPLING


V_3P3STBY
FB3N4
1 2
FB
603
0.2A
0.5 DCR
C3N37
4.7 UF
10%
6.3 V
X5R
805
C3N36
4.7 UF
10%
6.3 V
X5R
805
C3N38
0.1 UF
10%
6.3 V
X5R
402
V_HANA_VAA_RTS33S
V_3P3
FB3N3
FB
603
0.5A
0.1DCR
C3N13
4.7 UF
10%
6.3 V
X5R
805
C3N23
4.7 UF
10%
6.3 V
X5R
805
C3N20
0.1 UF
10%
6.3 V
X5R
402
C3N27
0.1 UF
10%
6.3 V
X5R
402
V_HANA_VAA_DAC33M
V_3P3STBY
R3N6
1 2
100 OHM 5%
402 CH
C3N17
0.1 UF
10%
6.3 V
X5R
402
V_HANA_VAA_XTAL_33S
V_3P3STBY
V_1P8STBY
U3B2
3 OF 4
IC
HANA
D12 VAA_RTS33S
D11 AVSS_RTS33S
E9 VAA_DAC33M3
D9 VAA_DAC33M2
C9 VAA_DAC33M1
D8 AVSS_DAC33M1
C7 VAA_DAC33M0
D7 AVSS_DAC33M0
C6 VAA_POR33S
C10 VAA_FAN33S
R3 VAA_XTAL33S
N8 VDDIO33S_STBY_PLL
P8 VSSIO33S_STBY_PLL
M6 VDDIO33S_25M_PLL
N6 VSSIO33S_25M_PLL
P5 VDDIO33S_AUD_PLL
R5 VSSIO33S_AUD_PLL
VAA_VID_PLL M12
AVSS_VID_PLL M13
VAA_GP_PLL R7
AVSS_GP_PLL P7
VAA_100M_PLL_A N15
AVSS_100M_PLL_A1 P15
AVSS_100M_PLL_A0 R15
VAA_100M_PLL_D R12
AVSS_100M_PLL_D P12
VDDC_STBY_PLL N7
VSSC_STBY_PLL M7
VDDC_25M_PLL N5
VSSC_25M_PLL M5
VDDC_AUD_PLL N4
VSSC_AUD_PLL P4
VDD_DAC18S E7
VAA_POR18S D6
VDDIO18S_100M_PLL5 N14
VDDIO18S_100M_PLL4 N13
VDDIO18S_100M_PLL3 P11
VDDIO18S_100M_PLL2 M10
VSSIO18S_100M_PLL2 N12
VDDIO18S_100M_PLL1 N9
VSSIO18S_100M_PLL1 N11
VDDIO18S_100M_PLL0 M9
VSSIO18S_100M_PLL0 N10
VDDIO18S_PIX_PLL L13
VSSIO18S_PIX_PLL L12
X802478-003
V_3P3STBY
C3N22 4.7 UF 10% 6.3 V X5R 805
C3N5 4.7 UF 10% 6.3 V X5R 805
V_1P8STBY
C3C2 4.7 UF 10% 6.3 V X5R 805
C3C1 4.7 UF 10% 6.3 V X5R 805
C3N34 4.7 UF 10% 6.3 V X5R 805
V_3P3STBY
C3N15 0.1 UF 10% 6.3 V X5R 402
C3N16 0.1 UF 10% 6.3 V X5R 402
C3N21 0.1 UF 10% 6.3 V X5R 402
C3N26 0.1 UF 10% 6.3 V X5R 402
C3P5 0.1 UF 10% 6.3 V X5R 402
C3N24 0.1 UF 10% 6.3 V X5R 402
V_1P8STBY
C3N32 0.1 UF 10% 6.3 V X5R 402
C3N14 0.1 UF 10% 6.3 V X5R 402
C3P2 0.1 UF 10% 6.3 V X5R 402
C3N28 0.1 UF 10% 6.3 V X5R 402
C3P6 0.1 UF 10% 6.3 V X5R 402
C3N25 0.1 UF 10% 6.3 V X5R 402
C3P7 0.1 UF 10% 6.3 V X5R 402
C3P8 0.1 UF 10% 6.3 V X5R 402
C3P9 0.1 UF 10% 6.3 V X5R 402
C3N35 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=HANA, POWER + DECOUPLING]

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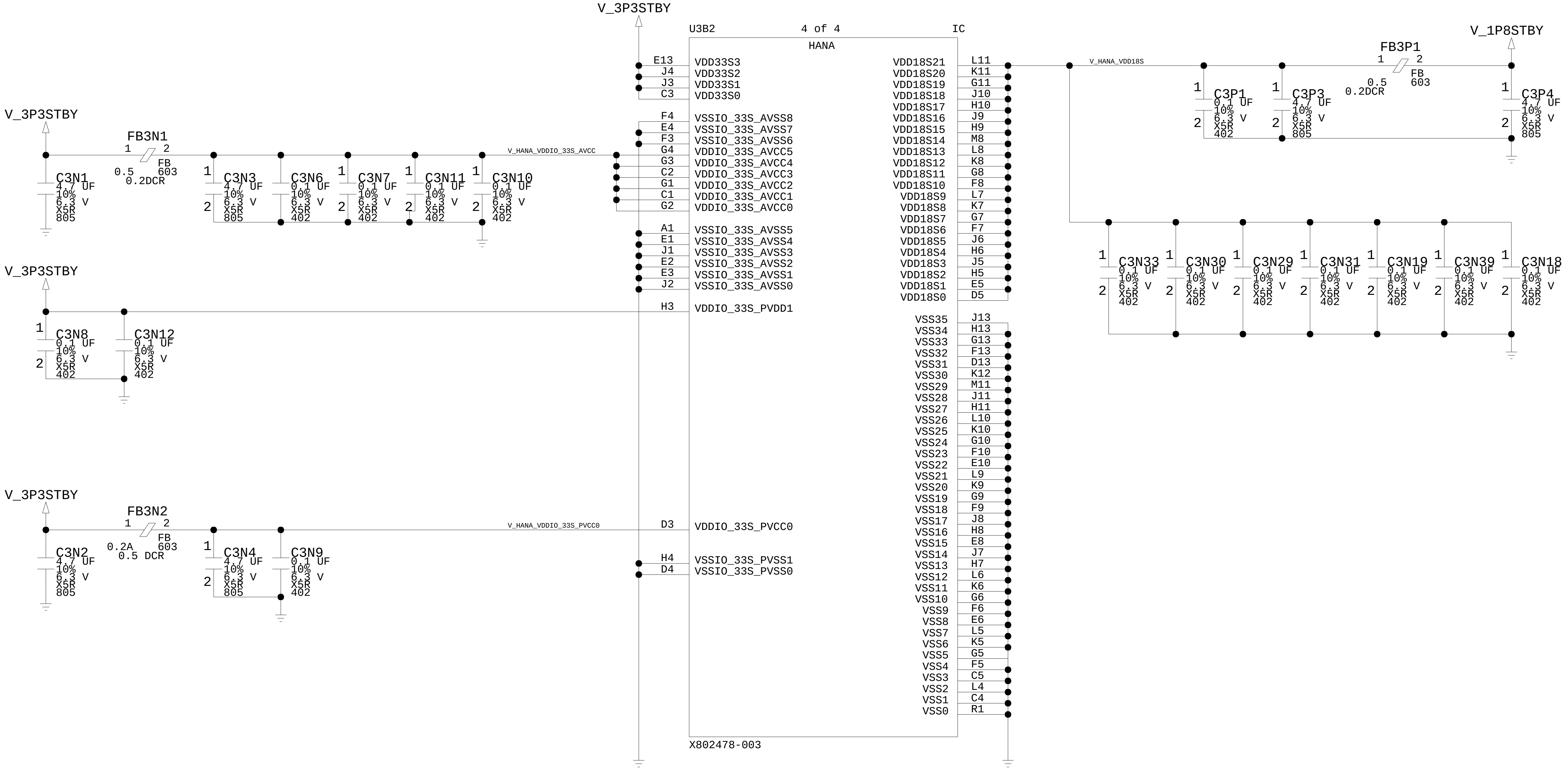
TRINITY_XDK	24/81	G	1.01

HANA, POWER + DECOUPLING


V_3P3STBY
U3B2
4 of 4
IC
HANA
E13 VDD33S3
J4 VDD33S2
J3 VDD33S1
C3 VDD33S0
F4 VSSIO_33S_AVSS8
E4 VSSIO_33S_AVSS7
F3 VSSIO_33S_AVSS6
G4 VDDIO_33S_AVCC5
G3 VDDIO_33S_AVCC4
C2 VDDIO_33S_AVCC3
G1 VDDIO_33S_AVCC2
C1 VDDIO_33S_AVCC1
G2 VDDIO_33S_AVCC0
A1 VSSIO_33S_AVSS5
E1 VSSIO_33S_AVSS4
J1 VSSIO_33S_AVSS3
E2 VSSIO_33S_AVSS2
E3 VSSIO_33S_AVSS1
J2 VSSIO_33S_AVSS0
H3 VDDIO_33S_PVDD1
D3 VDDIO_33S_PVCC0
H4 VSSIO_33S_PVSS1
D4 VSSIO_33S_PVSS0
X802478-003
VDD18S21 L11
VDD18S20 K11
VDD18S19 G11
VDD18S18 J10
VDD18S17 H10
VDD18S16 J9
VDD18S15 H9
VDD18S14 M8
VDD18S13 L8
VDD18S12 K8
VDD18S11 G8
VDD18S10 F8
VDD18S9 L7
VDD18S8 K7
VDD18S7 G7
VDD18S6 F7
VDD18S5 J6
VDD18S4 H6
VDD18S3 J5
VDD18S2 H5
VDD18S1 E5
VDD18S0 D5
VSS35 J13
VSS34 H13
VSS33 G13
VSS32 F13
VSS31 D13
VSS30 K12
VSS29 M11
VSS28 J11
VSS27 H11
VSS26 L10
VSS25 K10
VSS24 G10
VSS23 F10
VSS22 E10
VSS21 L9
VSS20 K9
VSS19 G9
VSS18 F9
VSS17 J8
VSS16 H8
VSS15 E8
VSS14 J7
VSS13 H7
VSS12 L6
VSS11 K6
VSS10 G6
VSS9 F6
VSS8 E6
VSS7 L5
VSS6 K5
VSS5 G5
VSS4 F5
VSS3 C5
VSS2 L4
VSS1 C4
VSS0 R1
V_3P3STBY
FB3N1
1 2
FB
0.5 603
0.2DCR
V_HANA_VDDIO_33S_AVCC
C3N1 4.7 UF 10% 6.3 V X5R 805
C3N3 4.7 UF 10% 6.3 V X5R 805
C3N6 0.1 UF 10% 6.3 V X5R 402
C3N7 0.1 UF 10% 6.3 V X5R 402
C3N11 0.1 UF 10% 6.3 V X5R 402
C3N10 0.1 UF 10% 6.3 V X5R 402
V_3P3STBY
C3N8 0.1 UF 10% 6.3 V X5R 402
C3N12 0.1 UF 10% 6.3 V X5R 402
V_3P3STBY
FB3N2
1 2
FB
0.2A 603
0.5 DCR
V_HANA_VDDIO_33S_PVCC0
C3N2 4.7 UF 10% 6.3 V X5R 805
C3N4 4.7 UF 10% 6.3 V X5R 805
C3N9 0.1 UF 10% 6.3 V X5R 402
V_HANA_VDD18S
FB3P1
1 2
FB
0.5 603
0.2DCR
V_1P8STBY
C3P1 0.1 UF 10% 6.3 V X5R 402
C3P3 4.7 UF 10% 6.3 V X5R 805
C3P4 4.7 UF 10% 6.3 V X5R 805
C3N33 0.1 UF 10% 6.3 V X5R 402
C3N30 0.1 UF 10% 6.3 V X5R 402
C3N29 0.1 UF 10% 6.3 V X5R 402
C3N31 0.1 UF 10% 6.3 V X5R 402
C3N19 0.1 UF 10% 6.3 V X5R 402
C3N39 0.1 UF 10% 6.3 V X5R 402
C3N18 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=HANA, POWER + DECOUPLING]

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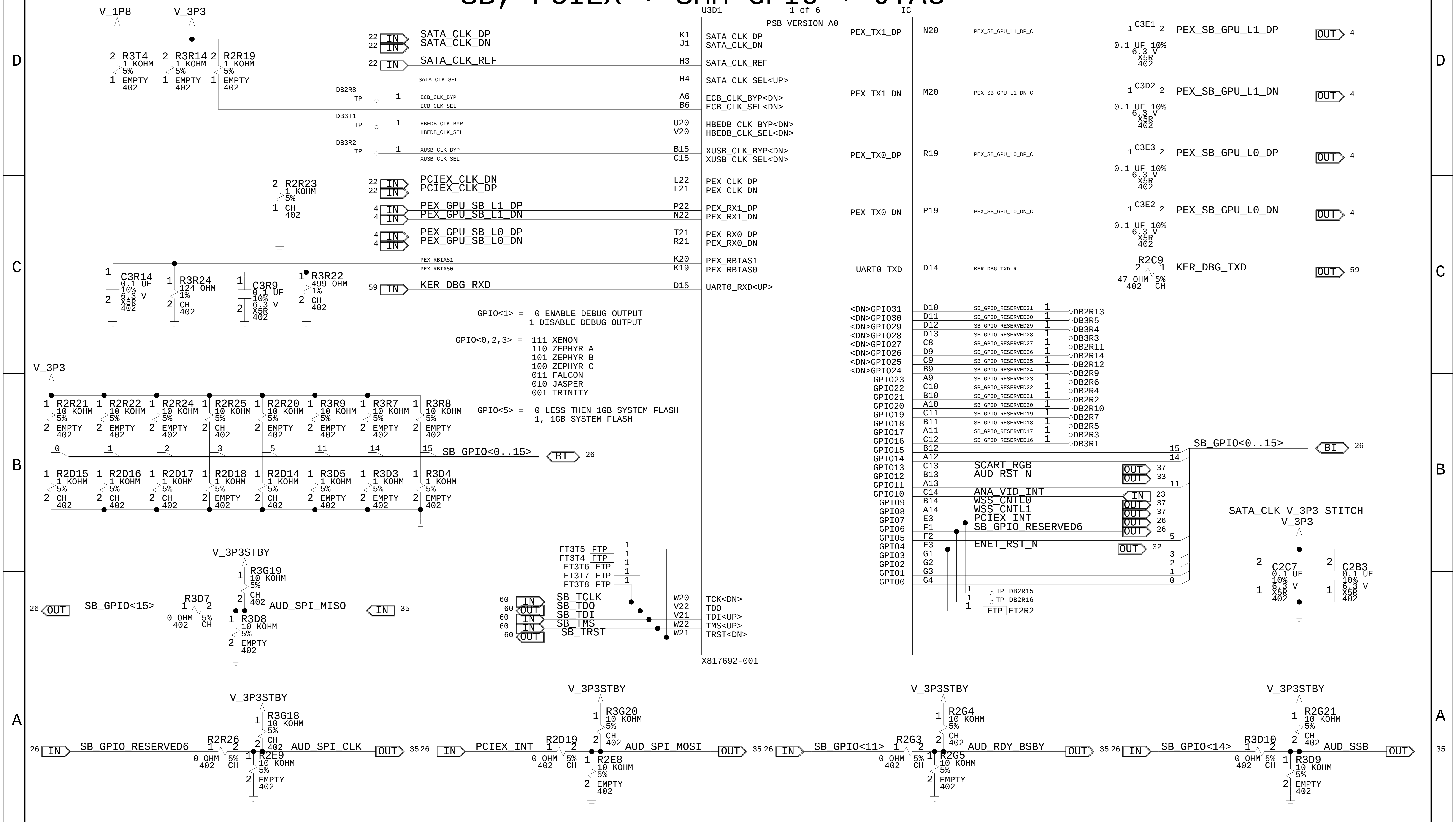
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 25/81	FAB G	REV 1.01

SB, PCIEX + SMM GPIO + JTAG


V_1P8
V_3P3
R3T4 1 KOHM 5% EMPTY 402
R3R14 1 KOHM 5% EMPTY 402
R2R19 1 KOHM 5% EMPTY 402
U3D1 1 of 6 IC
PSB VERSION A0
SATA_CLK_DP
SATA_CLK_DN
SATA_CLK_REF
SATA_CLK_SEL<UP>
ECB_CLK_BYP<DN>
ECB_CLK_SEL<DN>
HBEDB_CLK_BYP<DN>
HBEDB_CLK_SEL<DN>
XUSB_CLK_BYP<DN>
XUSB_CLK_SEL<DN>
DB2R8 TP
DB3T1 TP
DB3R2 TP
R2R23 1 KOHM 5% CH 402
PCIEX_CLK_DN
PCIEX_CLK_DP
PEX_CLK_DP
PEX_CLK_DN
PEX_GPU_SB_L1_DP
PEX_GPU_SB_L1_DN
PEX_GPU_SB_L0_DP
PEX_GPU_SB_L0_DN
PEX_RX1_DP
PEX_RX1_DN
PEX_RX0_DP
PEX_RX0_DN
PEX_RBIAS1
PEX_RBIAS0
C3R14 0.1 UF 10% 6.3 V X5R 402
R3R24 124 OHM 1% CH 402
C3R9 0.1 UF 10% 6.3 V X5R 402
R3R22 499 OHM 1% CH 402
KER_DBG_RXD
UART0_RXD<UP>
PEX_TX1_DP
PEX_TX1_DN
PEX_TX0_DP
PEX_TX0_DN
C3E1 C3D2 C3E3 C3E2 0.1 UF 10% 6.3 V X5R 402
PEX_SB_GPU_L1_DP
PEX_SB_GPU_L1_DN
PEX_SB_GPU_L0_DP
PEX_SB_GPU_L0_DN
UART0_TXD
R2C9 47 OHM 5% 402 CH
KER_DBG_TXD
<DN>GPIO31 <DN>GPIO30 <DN>GPIO29 <DN>GPIO28 <DN>GPIO27 <DN>GPIO26 <DN>GPIO25 <DN>GPIO24
GPIO23 GPIO22 GPIO21 GPIO20 GPIO19 GPIO18 GPIO17 GPIO16 GPIO15 GPIO14 GPIO13 GPIO12 GPIO11 GPIO10 GPIO9 GPIO8 GPIO7 GPIO6 GPIO5 GPIO4 GPIO3 GPIO2 GPIO1 GPIO0
SB_GPIO_RESERVED31 SB_GPIO_RESERVED30 SB_GPIO_RESERVED29 SB_GPIO_RESERVED28 SB_GPIO_RESERVED27 SB_GPIO_RESERVED26 SB_GPIO_RESERVED25 SB_GPIO_RESERVED24 SB_GPIO_RESERVED23 SB_GPIO_RESERVED22 SB_GPIO_RESERVED21 SB_GPIO_RESERVED20 SB_GPIO_RESERVED19 SB_GPIO_RESERVED18 SB_GPIO_RESERVED17 SB_GPIO_RESERVED16
DB2R13 DB3R5 DB3R4 DB3R3 DB2R11 DB2R14 DB2R12 DB2R9 DB2R6 DB2R4 DB2R2 DB2R10 DB2R7 DB2R5 DB2R3 DB3R1
SB_GPIO<0..15>
SCART_RGB
AUD_RST_N
ANA_VID_INT
WSS_CNTL0
WSS_CNTL1
PCIEX_INT
SB_GPIO_RESERVED6
ENET_RST_N
TP DB2R15
TP DB2R16
FTP FT2R2
SATA_CLK V_3P3 STITCH
C2C7 0.1 UF 10% 6.3 V X5R 402
C2B3 0.1 UF 10% 6.3 V X5R 402
R2R21 R2R22 R2R24 R2R25 R2R20 R3R9 R3R7 R3R8 10 KOHM 5%
R2D15 R2D16 R2D17 R2D18 R2D14 R3D5 R3D3 R3D4 1 KOHM 5%
V_3P3STBY
R3G19 10 KOHM 5% CH 402
R3D7 0 OHM 5% 402 CH
SB_GPIO<15>
AUD_SPI_MISO
R3D8 10 KOHM 5% EMPTY 402
FT3T5 FT3T4 FT3T6 FT3T7 FT3T8 FTP
SB_TCLK
SB_TDO
SB_TDI
SB_TMS
SB_TRST
TCK<DN>
TDO
TDI<UP>
TMS<UP>
TRST<DN>
X817692-001
SB_GPIO_RESERVED6
R2R26 0 OHM 5% 402 CH
R3G18 10 KOHM 5% CH 402
R2E9 10 KOHM 5% EMPTY 402
AUD_SPI_CLK
PCIEX_INT
R2D19 0 OHM 5% 402 CH
R3G20 10 KOHM 5% CH 402
R2E8 10 KOHM 5% EMPTY 402
AUD_SPI_MOSI
SB_GPIO<11>
R2G3 0 OHM 5% 402 CH
R2G4 10 KOHM 5% CH 402
R2G5 10 KOHM 5% EMPTY 402
AUD_RDY_BSBY
SB_GPIO<14>
R3D10 0 OHM 5% 402 CH
R2G21 10 KOHM 5% CH 402
R3D9 10 KOHM 5% EMPTY 402
AUD_SSB
IN
OUT
BI

GPIO<1> = 0 ENABLE DEBUG OUTPUT
1 DISABLE DEBUG OUTPUT

GPIO<0,2,3> = 111 XENON
110 ZEPHYR A
101 ZEPHYR B
100 ZEPHYR C
011 FALCON
010 JASPER
001 TRINITY

GPIO<5> = 0 LESS THEN 1GB SYSTEM FLASH
1, 1GB SYSTEM FLASH

[PAGE_TITLE=SB, PCIEX + SMM GPIO + JTAG]

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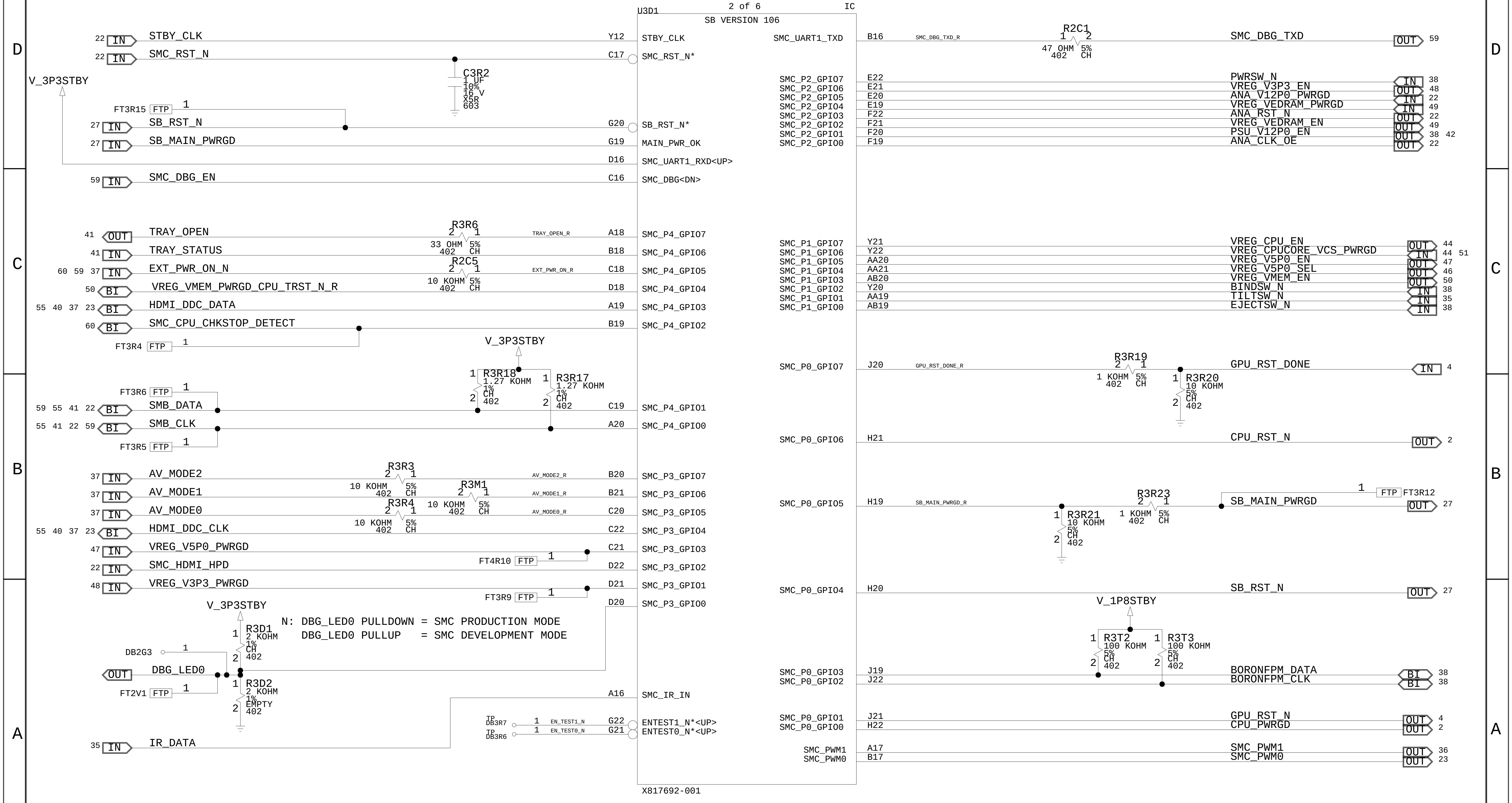
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	26/81	G	1.01

SB, SMC


U3D1
2 of 6
IC
SB VERSION 106
22 IN STBY_CLK Y12 STBY_CLK
22 IN SMC_RST_N C17 SMC_RST_N*
C3R2 1 UF 10% 16 V X5R 603
V_3P3STBY
FT3R15 FTP 1
27 IN SB_RST_N G20 SB_RST_N*
27 IN SB_MAIN_PWRGD G19 MAIN_PWR_OK
D16 SMC_UART1_RXD<UP>
59 IN SMC_DBG_EN C16 SMC_DBG<DN>
41 OUT TRAY_OPEN
R3R6 2 1 33 OHM 5% 402 CH
TRAY_OPEN_R A18 SMC_P4_GPIO7
41 IN TRAY_STATUS B18 SMC_P4_GPIO6
60 59 37 IN EXT_PWR_ON_N
R2C5 2 1 10 KOHM 5% 402 CH
EXT_PWR_ON_R C18 SMC_P4_GPIO5
50 BI VREG_VMEM_PWRGD_CPU_TRST_N_R D18 SMC_P4_GPIO4
55 40 37 23 BI HDMI_DDC_DATA A19 SMC_P4_GPIO3
60 BI SMC_CPU_CHKSTOP_DETECT B19 SMC_P4_GPIO2
FT3R4 FTP 1
V_3P3STBY
R3R18 1.27 KOHM 1% CH 402
R3R17 1.27 KOHM 1% CH 402
FT3R6 FTP 1
59 55 41 22 BI SMB_DATA C19 SMC_P4_GPIO1
55 41 22 59 BI SMB_CLK A20 SMC_P4_GPIO0
FT3R5 FTP 1
37 IN AV_MODE2
R3R3 2 1 10 KOHM 5% 402 CH
AV_MODE2_R B20 SMC_P3_GPIO7
37 IN AV_MODE1
R3M1 2 1 10 KOHM 5% 402 CH
AV_MODE1_R B21 SMC_P3_GPIO6
37 IN AV_MODE0
R3R4 2 1 10 KOHM 5% 402 CH
AV_MODE0_R C20 SMC_P3_GPIO5
55 40 37 23 BI HDMI_DDC_CLK C22 SMC_P3_GPIO4
47 IN VREG_V5P0_PWRGD C21 SMC_P3_GPIO3
FT4R10 FTP 1
22 IN SMC_HDMI_HPD D22 SMC_P3_GPIO2
48 IN VREG_V3P3_PWRGD D21 SMC_P3_GPIO1
FT3R9 FTP 1
D20 SMC_P3_GPIO0
V_3P3STBY
R3D1 2 KOHM 1% CH 402
DB2G3 1
OUT DBG_LED0
FT2V1 FTP 1
R3D2 2 KOHM 1% EMPTY 402
A16 SMC_IR_IN
TP DB3R7 1 EN_TEST1_N G22 ENTEST1_N*<UP>
TP DB3R6 1 EN_TEST0_N G21 ENTEST0_N*<UP>
35 IN IR_DATA
X817692-001
SMC_UART1_TXD B16 SMC_DBG_TXD_R
R2C1 1 2 47 OHM 5% 402 CH
SMC_DBG_TXD OUT 59
SMC_P2_GPIO7 E22 PWRSW_N IN 38
SMC_P2_GPIO6 E21 VREG_V3P3_EN OUT 48
SMC_P2_GPIO5 E20 ANA_V12P0_PWRGD IN 22
SMC_P2_GPIO4 E19 VREG_VEDRAM_PWRGD IN 49
SMC_P2_GPIO3 F22 ANA_RST_N OUT 22
SMC_P2_GPIO2 F21 VREG_VEDRAM_EN OUT 49
SMC_P2_GPIO1 F20 PSU_V12P0_EN OUT 38 42
SMC_P2_GPIO0 F19 ANA_CLK_OE OUT 22
SMC_P1_GPIO7 Y21 VREG_CPU_EN OUT 44
SMC_P1_GPIO6 Y22 VREG_CPUCORE_VCS_PWRGD IN 44 51
SMC_P1_GPIO5 AA20 VREG_V5P0_EN OUT 47
SMC_P1_GPIO4 AA21 VREG_V5P0_SEL OUT 46
SMC_P1_GPIO3 AB20 VREG_VMEM_EN OUT 50
SMC_P1_GPIO2 Y20 BINDSW_N IN 38
SMC_P1_GPIO1 AA19 TILTSW_N IN 35
SMC_P1_GPIO0 AB19 EJECTSW_N IN 38
SMC_P0_GPIO7 J20 GPU_RST_DONE_R
R3R19 2 1 1 KOHM 5% 402 CH
R3R20 10 KOHM 5% CH 402
GPU_RST_DONE IN 4
SMC_P0_GPIO6 H21 CPU_RST_N OUT 2
SMC_P0_GPIO5 H19 SB_MAIN_PWRGD_R
R3R21 10 KOHM 5% CH 402
R3R23 2 1 1 KOHM 5% 402 CH
1 FTP FT3R12
SB_MAIN_PWRGD OUT 27
SMC_P0_GPIO4 H20 SB_RST_N OUT 27
V_1P8STBY
R3T2 100 KOHM 5% CH 402
R3T3 100 KOHM 5% CH 402
SMC_P0_GPIO3 J19 BORONFPM_DATA BI 38
SMC_P0_GPIO2 J22 BORONFPM_CLK BI 38
SMC_P0_GPIO1 J21 GPU_RST_N OUT 4
SMC_P0_GPIO0 H22 CPU_PWRGD OUT 2
SMC_PWM1 A17 SMC_PWM1 OUT 36
SMC_PWM0 B17 SMC_PWM0 OUT 23

N: DBG_LED0 PULLDOWN = SMC PRODUCTION MODE
DBG_LED0 PULLUP = SMC DEVELOPMENT MODE

[PAGE_TITLE=SB, SMC]

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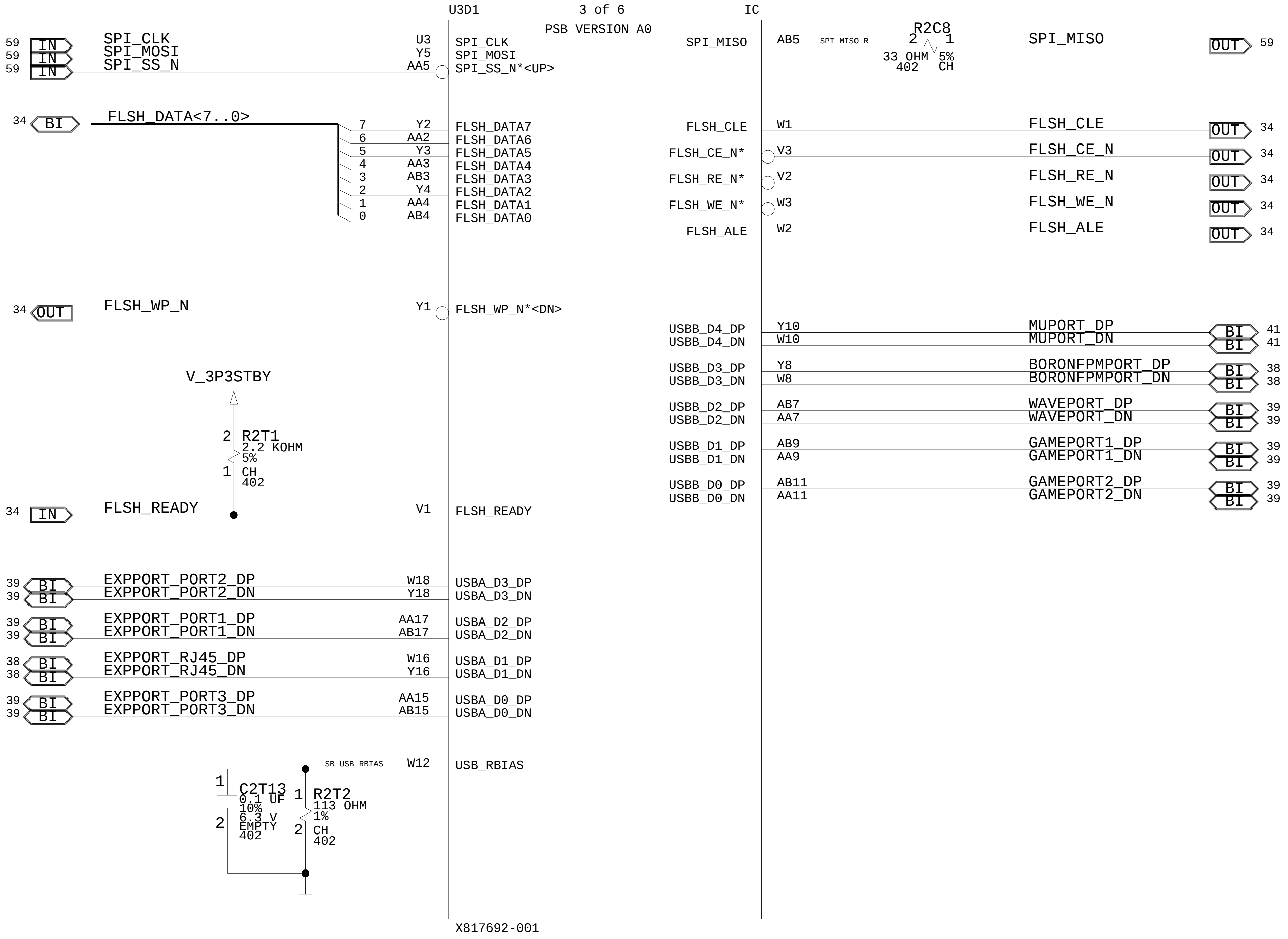
SB, FLASH + USB + SPI

N: ALL PORTS ARE DIFFERENTIAL USB PAIRS ON THIS PAGE


U3D1
3 of 6
IC
PSB VERSION A0
59 IN SPI_CLK U3 SPI_CLK
59 IN SPI_MOSI Y5 SPI_MOSI
59 IN SPI_SS_N AA5 SPI_SS_N*<UP>
SPI_MISO AB5 SPI_MISO_R
R2C8
2 1
33 OHM 5%
402 CH
SPI_MISO OUT 59
34 BI FLSH_DATA<7..0>
7 Y2 FLSH_DATA7
6 AA2 FLSH_DATA6
5 Y3 FLSH_DATA5
4 AA3 FLSH_DATA4
3 AB3 FLSH_DATA3
2 Y4 FLSH_DATA2
1 AA4 FLSH_DATA1
0 AB4 FLSH_DATA0
FLSH_CLE W1 FLSH_CLE OUT 34
FLSH_CE_N* V3 FLSH_CE_N OUT 34
FLSH_RE_N* V2 FLSH_RE_N OUT 34
FLSH_WE_N* W3 FLSH_WE_N OUT 34
FLSH_ALE W2 FLSH_ALE OUT 34
34 OUT FLSH_WP_N Y1 FLSH_WP_N*<DN>
USBB_D4_DP Y10 MUPORT_DP BI 41
USBB_D4_DN W10 MUPORT_DN BI 41
USBB_D3_DP Y8 BORONFPMPORT_DP BI 38
USBB_D3_DN W8 BORONFPMPORT_DN BI 38
USBB_D2_DP AB7 WAVEPORT_DP BI 39
USBB_D2_DN AA7 WAVEPORT_DN BI 39
USBB_D1_DP AB9 GAMEPORT1_DP BI 39
USBB_D1_DN AA9 GAMEPORT1_DN BI 39
USBB_D0_DP AB11 GAMEPORT2_DP BI 39
USBB_D0_DN AA11 GAMEPORT2_DN BI 39
V_3P3STBY
2 R2T1
2.2 KOHM
5%
1 CH
402
34 IN FLSH_READY V1 FLSH_READY
39 BI EXPPORT_PORT2_DP W18 USBA_D3_DP
39 BI EXPPORT_PORT2_DN Y18 USBA_D3_DN
39 BI EXPPORT_PORT1_DP AA17 USBA_D2_DP
39 BI EXPPORT_PORT1_DN AB17 USBA_D2_DN
38 BI EXPPORT_RJ45_DP W16 USBA_D1_DP
38 BI EXPPORT_RJ45_DN Y16 USBA_D1_DN
39 BI EXPPORT_PORT3_DP AA15 USBA_D0_DP
39 BI EXPPORT_PORT3_DN AB15 USBA_D0_DN
SB_USB_RBIAS W12 USB_RBIAS
1 C2T13
0.1 UF
10%
6.3 V
2 EMPTY
402
1 R2T2
113 OHM
1%
2 CH
402
X817692-001

[PAGE_TITLE=SB, FLASH + USB + SPI]

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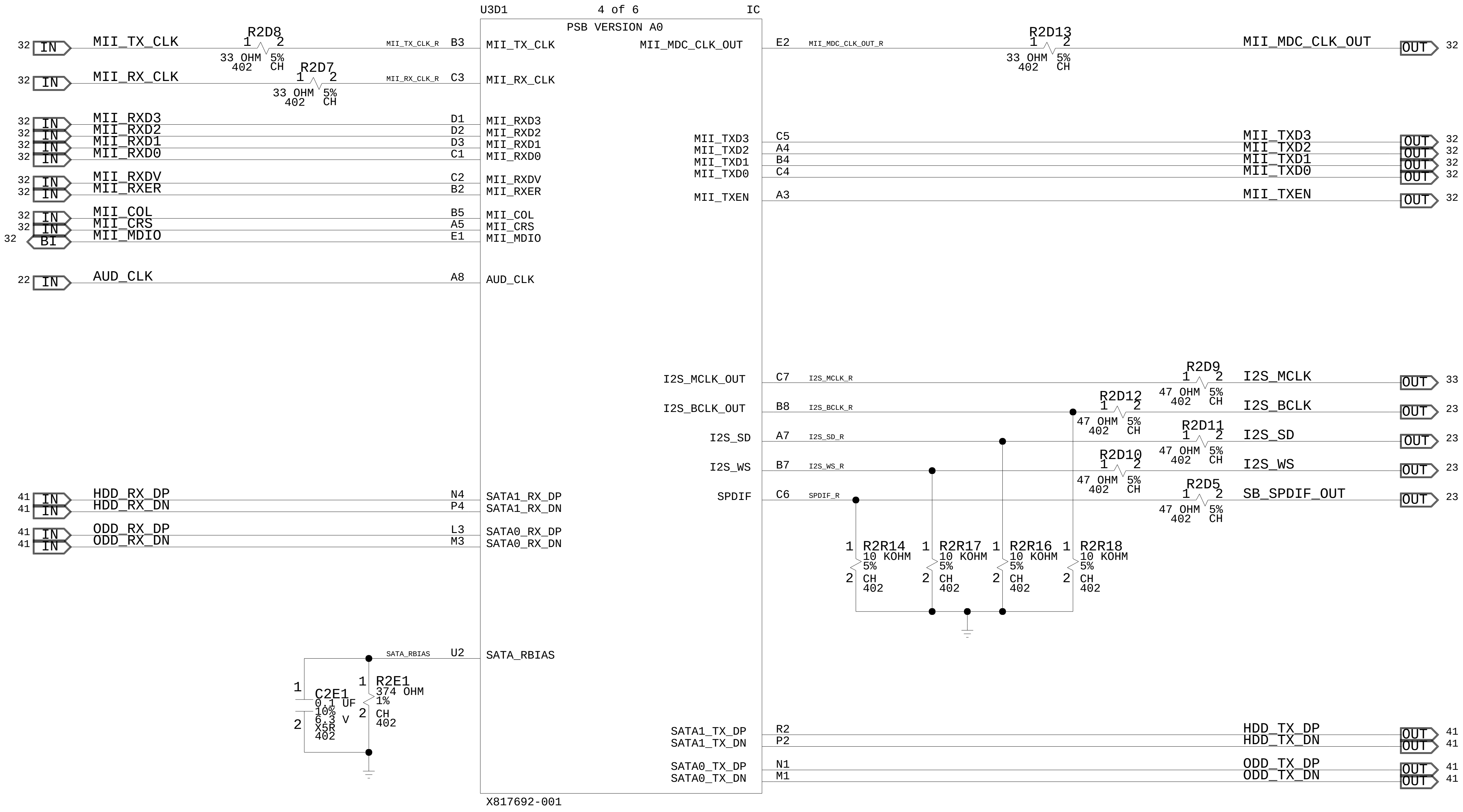
MICROSOFT
CONFIDENTIAL

PROJECT NAME	PAGE	FAB	REV
TRINITY_XDK	28/81	G	1.01

SB, ETHERNET + AUDIO + SATA


U3D1
4 of 6
IC
PSB VERSION A0
X817692-001
32 IN MII_TX_CLK
R2D8 1 2 33 OHM 5% 402 CH
MII_TX_CLK_R B3 MII_TX_CLK
32 IN MII_RX_CLK
R2D7 1 2 33 OHM 5% 402 CH
MII_RX_CLK_R C3 MII_RX_CLK
32 IN MII_RXD3 D1 MII_RXD3
32 IN MII_RXD2 D2 MII_RXD2
32 IN MII_RXD1 D3 MII_RXD1
32 IN MII_RXD0 C1 MII_RXD0
32 IN MII_RXDV C2 MII_RXDV
32 IN MII_RXER B2 MII_RXER
32 IN MII_COL B5 MII_COL
32 IN MII_CRS A5 MII_CRS
32 BI MII_MDIO E1 MII_MDIO
22 IN AUD_CLK A8 AUD_CLK
41 IN HDD_RX_DP N4 SATA1_RX_DP
41 IN HDD_RX_DN P4 SATA1_RX_DN
41 IN ODD_RX_DP L3 SATA0_RX_DP
41 IN ODD_RX_DN M3 SATA0_RX_DN
SATA_RBIAS U2 SATA_RBIAS
C2E1 1 2 0.1 UF 10% 6.3 V X5R 402
R2E1 1 2 374 OHM 1% CH 402
MII_MDC_CLK_OUT E2 MII_MDC_CLK_OUT_R
R2D13 1 2 33 OHM 5% 402 CH
MII_MDC_CLK_OUT OUT 32
MII_TXD3 C5 MII_TXD3 OUT 32
MII_TXD2 A4 MII_TXD2 OUT 32
MII_TXD1 B4 MII_TXD1 OUT 32
MII_TXD0 C4 MII_TXD0 OUT 32
MII_TXEN A3 MII_TXEN OUT 32
I2S_MCLK_OUT C7 I2S_MCLK_R
R2D9 1 2 47 OHM 5% 402 CH
I2S_MCLK OUT 33
I2S_BCLK_OUT B8 I2S_BCLK_R
R2D12 1 2 47 OHM 5% 402 CH
I2S_BCLK OUT 23 33
I2S_SD A7 I2S_SD_R
R2D11 1 2 47 OHM 5% 402 CH
I2S_SD OUT 23 33
I2S_WS B7 I2S_WS_R
R2D10 1 2 47 OHM 5% 402 CH
I2S_WS OUT 23 33
SPDIF C6 SPDIF_R
R2D5 1 2 47 OHM 5% 402 CH
SB_SPDIF_OUT OUT 23
R2R14 1 2 10 KOHM 5% CH 402
R2R17 1 2 10 KOHM 5% CH 402
R2R16 1 2 10 KOHM 5% CH 402
R2R18 1 2 10 KOHM 5% CH 402
SATA1_TX_DP R2 HDD_TX_DP OUT 41
SATA1_TX_DN P2 HDD_TX_DN OUT 41
SATA0_TX_DP N1 ODD_TX_DP OUT 41
SATA0_TX_DN M1 ODD_TX_DN OUT 41

[PAGE_TITLE=SB, ETHERNET + AUDIO + SATA]

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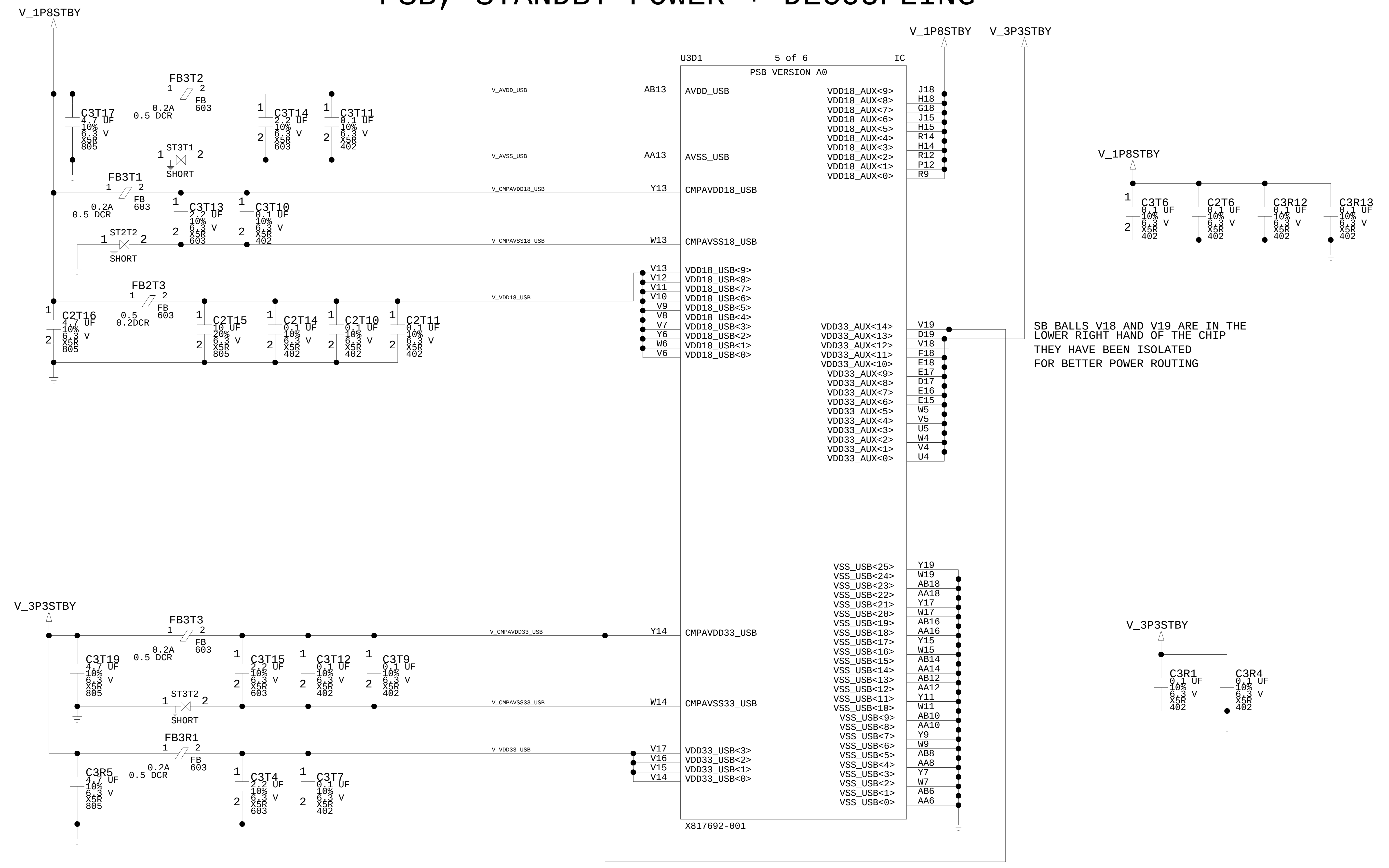
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 29/81	FAB G	REV 1.01

PSB, STANDBY POWER + DECOUPLING


V_1P8STBY
FB3T2 1 2 FB 603 0.2A 0.5 DCR
C3T17 4.7 UF 10% 6.3 V X5R 805
C3T14 2.2 UF 10% 6.3 V X5R 603
C3T11 0.1 UF 10% 6.3 V X5R 402
ST3T1 1 2 SHORT
FB3T1 1 2 FB 603 0.2A 0.5 DCR
C3T13 2.2 UF 10% 6.3 V X5R 603
C3T10 0.1 UF 10% 6.3 V X5R 402
ST2T2 1 2 SHORT
FB2T3 1 2 FB 603 0.5 0.2DCR
C2T16 4.7 UF 10% 6.3 V X5R 805
C2T15 10 UF 20% 6.3 V X5R 805
C2T14 0.1 UF 10% 6.3 V X5R 402
C2T10 0.1 UF 10% 6.3 V X5R 402
C2T11 0.1 UF 10% 6.3 V X5R 402
V_AVDD_USB
V_AVSS_USB
V_CMPAVDD18_USB
V_CMPAVSS18_USB
V_VDD18_USB
U3D1 5 of 6 IC
PSB VERSION A0
AB13 AVDD_USB
AA13 AVSS_USB
Y13 CMPAVDD18_USB
W13 CMPAVSS18_USB
V13 VDD18_USB<9>
V12 VDD18_USB<8>
V11 VDD18_USB<7>
V10 VDD18_USB<6>
V9 VDD18_USB<5>
V8 VDD18_USB<4>
V7 VDD18_USB<3>
Y6 VDD18_USB<2>
W6 VDD18_USB<1>
V6 VDD18_USB<0>
Y14 CMPAVDD33_USB
W14 CMPAVSS33_USB
V17 VDD33_USB<3>
V16 VDD33_USB<2>
V15 VDD33_USB<1>
V14 VDD33_USB<0>
X817692-001
V_1P8STBY V_3P3STBY
VDD18_AUX<9> J18
VDD18_AUX<8> H18
VDD18_AUX<7> G18
VDD18_AUX<6> J15
VDD18_AUX<5> H15
VDD18_AUX<4> R14
VDD18_AUX<3> H14
VDD18_AUX<2> R12
VDD18_AUX<1> P12
VDD18_AUX<0> R9
VDD33_AUX<14> V19
VDD33_AUX<13> D19
VDD33_AUX<12> V18
VDD33_AUX<11> F18
VDD33_AUX<10> E18
VDD33_AUX<9> E17
VDD33_AUX<8> D17
VDD33_AUX<7> E16
VDD33_AUX<6> E15
VDD33_AUX<5> W5
VDD33_AUX<4> V5
VDD33_AUX<3> U5
VDD33_AUX<2> W4
VDD33_AUX<1> V4
VDD33_AUX<0> U4
VSS_USB<25> Y19
VSS_USB<24> W19
VSS_USB<23> AB18
VSS_USB<22> AA18
VSS_USB<21> Y17
VSS_USB<20> W17
VSS_USB<19> AB16
VSS_USB<18> AA16
VSS_USB<17> Y15
VSS_USB<16> W15
VSS_USB<15> AB14
VSS_USB<14> AA14
VSS_USB<13> AB12
VSS_USB<12> AA12
VSS_USB<11> Y11
VSS_USB<10> W11
VSS_USB<9> AB10
VSS_USB<8> AA10
VSS_USB<7> Y9
VSS_USB<6> W9
VSS_USB<5> AB8
VSS_USB<4> AA8
VSS_USB<3> Y7
VSS_USB<2> W7
VSS_USB<1> AB6
VSS_USB<0> AA6
V_1P8STBY
C3T6 0.1 UF 10% 6.3 V X5R 402
C2T6 0.1 UF 10% 6.3 V X5R 402
C3R12 0.1 UF 10% 6.3 V X5R 402
C3R13 0.1 UF 10% 6.3 V X5R 402
V_3P3STBY
FB3T3 1 2 FB 603 0.2A 0.5 DCR
C3T19 4.7 UF 10% 6.3 V X5R 805
C3T15 2.2 UF 10% 6.3 V X5R 603
C3T12 0.1 UF 10% 6.3 V X5R 402
C3T9 0.1 UF 10% 6.3 V X5R 402
ST3T2 1 2 SHORT
FB3R1 1 2 FB 603 0.2A 0.5 DCR
C3R5 4.7 UF 10% 6.3 V X5R 805
C3T4 2.2 UF 10% 6.3 V X5R 603
C3T7 0.1 UF 10% 6.3 V X5R 402
V_CMPAVDD33_USB
V_CMPAVSS33_USB
V_VDD33_USB
V_3P3STBY
C3R1 0.1 UF 10% 6.3 V X5R 402
C3R4 0.1 UF 10% 6.3 V X5R 402

SB BALLS V18 AND V19 ARE IN THE LOWER RIGHT HAND OF THE CHIP
THEY HAVE BEEN ISOLATED
FOR BETTER POWER ROUTING

[PAGE_TITLE=PSB, STANDBY POWER + DECOUPLING]

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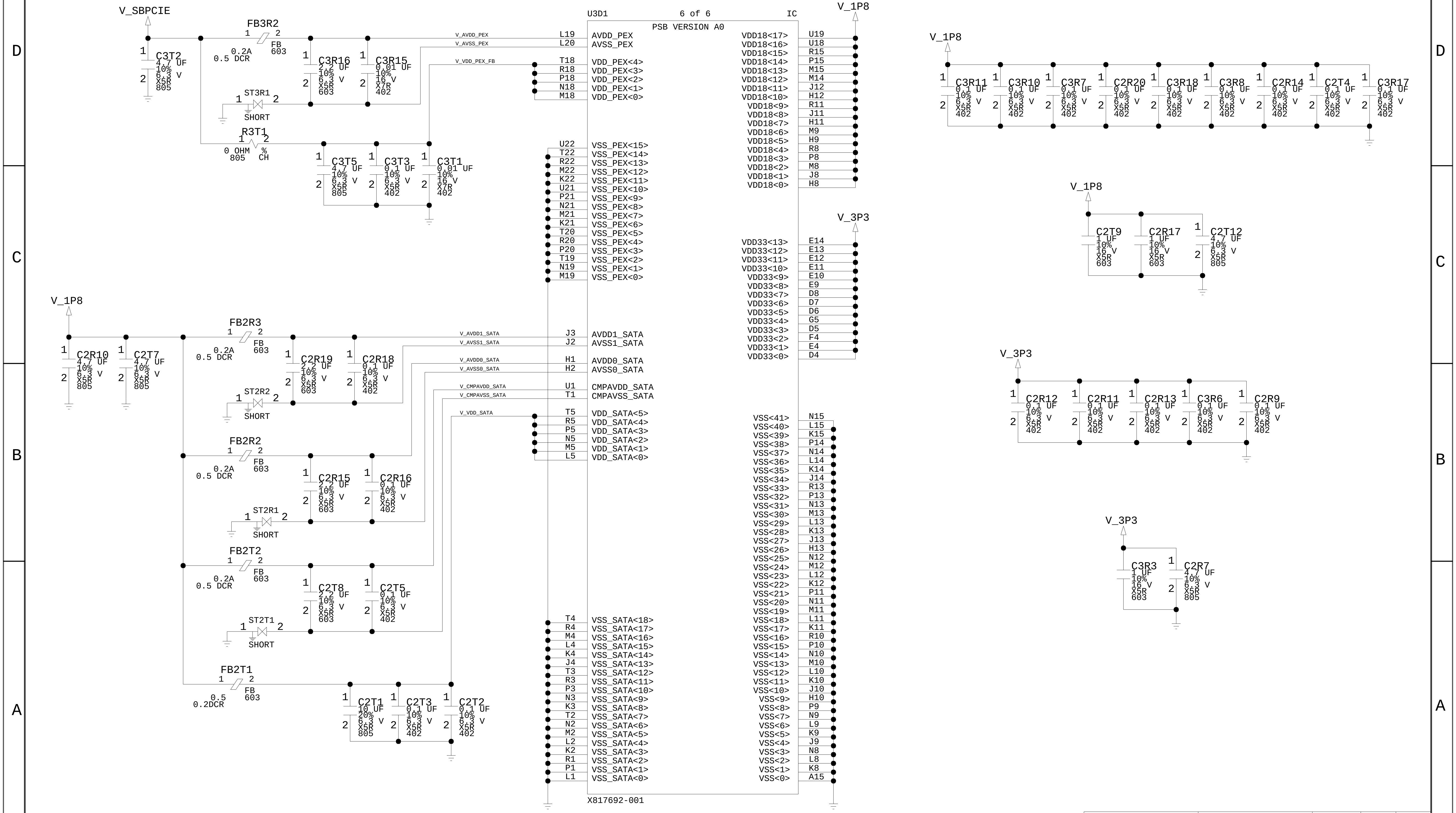
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 30/81	FAB G	REV 1.01

PSB, MAIN POWER + DECOUPLING


V_SBPCIE
FB3R2
FB 603
0.2A 0.5 DCR
C3T2 4.7 UF 10% 6.3 V X5R 805
C3R16 2.2 UF 10% 6.3 V X5R 603
C3R15 0.01 UF 10% 16 V X7R 402
ST3R1 SHORT
R3T1 0 OHM 805 % CH
C3T5 4.7 UF 10% 6.3 V X5R 805
C3T3 0.1 UF 10% 6.3 V X5R 402
C3T1 0.01 UF 10% 16 V X7R 402
V_AVDD_PEX
V_AVSS_PEX
V_VDD_PEX_FB
U3D1
6 of 6
IC
PSB VERSION A0
L19 AVDD_PEX
L20 AVSS_PEX
T18 VDD_PEX<4>
R18 VDD_PEX<3>
P18 VDD_PEX<2>
N18 VDD_PEX<1>
M18 VDD_PEX<0>
U22 VSS_PEX<15>
T22 VSS_PEX<14>
R22 VSS_PEX<13>
M22 VSS_PEX<12>
K22 VSS_PEX<11>
U21 VSS_PEX<10>
P21 VSS_PEX<9>
N21 VSS_PEX<8>
M21 VSS_PEX<7>
K21 VSS_PEX<6>
T20 VSS_PEX<5>
R20 VSS_PEX<4>
P20 VSS_PEX<3>
T19 VSS_PEX<2>
N19 VSS_PEX<1>
M19 VSS_PEX<0>
V_1P8
VDD18<17> U19
VDD18<16> U18
VDD18<15> R15
VDD18<14> P15
VDD18<13> M15
VDD18<12> J12
VDD18<11> H12
VDD18<10> R11
VDD18<9> J11
VDD18<8> H11
VDD18<7> M9
VDD18<6> H9
VDD18<5> R8
VDD18<4> P8
VDD18<3> M8
VDD18<2> J8
VDD18<1> H8
VDD18<0>
V_3P3
VDD33<13> E14
VDD33<12> E13
VDD33<11> E12
VDD33<10> E11
VDD33<9> E10
VDD33<8> E9
VDD33<7> D8
VDD33<6> D7
VDD33<5> D6
VDD33<4> G5
VDD33<3> D5
VDD33<2> F4
VDD33<1> E4
VDD33<0> D4
C3R11 C3R10 C3R7 C3R20 C3R18 C3R8 C2R14 C2T4 C3R17 0.1 UF 10% 6.3 V X5R 402
C2T9 1 UF 10% 16 V X5R 603
C2R17 1 UF 10% 16 V X5R 603
C2T12 4.7 UF 10% 6.3 V X5R 805
C2R12 C2R11 C2R13 C3R6 C2R9 0.1 UF 10% 6.3 V X5R 402
C3R3 1 UF 10% 16 V X5R 603
C2R7 4.7 UF 10% 6.3 V X5R 805
C2R10 4.7 UF 10% 6.3 V X5R 805
C2T7 4.7 UF 10% 6.3 V X5R 805
FB2R3 FB 603 0.2A 0.5 DCR
C2R19 2.2 UF 10% 6.3 V X5R 603
C2R18 0.1 UF 10% 6.3 V X5R 402
ST2R2 SHORT
FB2R2 FB 603 0.2A 0.5 DCR
C2R15 2.2 UF 10% 6.3 V X5R 603
C2R16 0.1 UF 10% 6.3 V X5R 402
ST2R1 SHORT
FB2T2 FB 603 0.2A 0.5 DCR
C2T8 2.2 UF 10% 6.3 V X5R 603
C2T5 0.1 UF 10% 6.3 V X5R 402
ST2T1 SHORT
FB2T1 FB 603 0.5 0.2DCR
C2T1 10 UF 20% 6.3 V X5R 805
C2T3 0.1 UF 10% 6.3 V X5R 402
C2T2 0.1 UF 10% 6.3 V X5R 402
V_AVDD1_SATA
V_AVSS1_SATA
V_AVDD0_SATA
V_AVSS0_SATA
V_CMPAVDD_SATA
V_CMPAVSS_SATA
V_VDD_SATA
J3 AVDD1_SATA
J2 AVSS1_SATA
H1 AVDD0_SATA
H2 AVSS0_SATA
U1 CMPAVDD_SATA
T1 CMPAVSS_SATA
T5 VDD_SATA<5>
R5 VDD_SATA<4>
P5 VDD_SATA<3>
N5 VDD_SATA<2>
M5 VDD_SATA<1>
L5 VDD_SATA<0>
T4 VSS_SATA<18>
R4 VSS_SATA<17>
M4 VSS_SATA<16>
L4 VSS_SATA<15>
K4 VSS_SATA<14>
J4 VSS_SATA<13>
T3 VSS_SATA<12>
R3 VSS_SATA<11>
P3 VSS_SATA<10>
N3 VSS_SATA<9>
K3 VSS_SATA<8>
T2 VSS_SATA<7>
N2 VSS_SATA<6>
M2 VSS_SATA<5>
L2 VSS_SATA<4>
K2 VSS_SATA<3>
R1 VSS_SATA<2>
P1 VSS_SATA<1>
L1 VSS_SATA<0>
VSS<41> N15
VSS<40> L15
VSS<39> K15
VSS<38> P14
VSS<37> N14
VSS<36> L14
VSS<35> K14
VSS<34> J14
VSS<33> R13
VSS<32> P13
VSS<31> N13
VSS<30> M13
VSS<29> L13
VSS<28> K13
VSS<27> J13
VSS<26> H13
VSS<25> N12
VSS<24> M12
VSS<23> L12
VSS<22> K12
VSS<21> P11
VSS<20> N11
VSS<19> M11
VSS<18> L11
VSS<17> K11
VSS<16> R10
VSS<15> P10
VSS<14> N10
VSS<13> M10
VSS<12> L10
VSS<11> K10
VSS<10> J10
VSS<9> H10
VSS<8> P9
VSS<7> N9
VSS<6> L9
VSS<5> K9
VSS<4> J9
VSS<3> N8
VSS<2> L8
VSS<1> K8
VSS<0> A15
X817692-001

[PAGE_TITLE=PSB, MAIN POWER + DECOUPLING]

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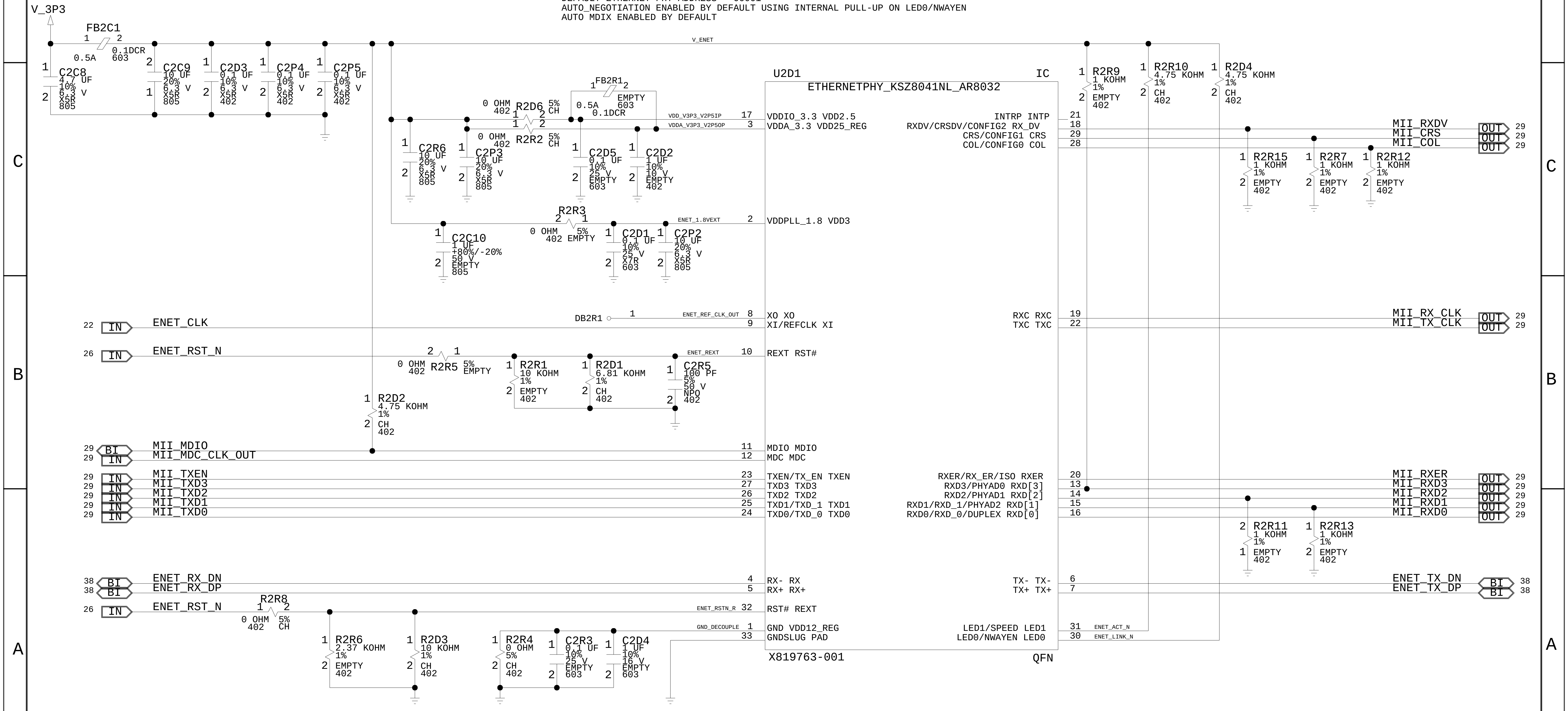
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 31/81	FAB G	REV 1.01

PSB OUT, ETHERNET

MICREL AND ATHEROS ENET PHY

NOTE : THIS PAGE OF THE SCHEMATIC DISPLAYS ONLY THE MICREL PART AND ITS ASSOCIATED STUFFING OPTIONS.
THE NO STUFF PARTS WILL BE STUFFED ALONG WITH THE ATHEROS PHY AND WILL BE IMPLEMENTED AS A BOM STUFFING OPTION..

DEFAULT ETHERNET PHY ADDRESS = 00001
AUTO_NEGOTIATION ENABLED BY DEFAULT USING INTERNAL PULL-UP ON LED0/NWAYEN
AUTO MDIX ENABLED BY DEFAULT


V_3P3
FB2C1 1 2 0.5A 0.1DCR 603
C2C8 4.7 UF 10% 6.3 V X5R 805
C2C9 10 UF 20% 6.3 V X5R 805
C2D3 0.1 UF 10% 6.3 V X5R 402
C2P4 0.1 UF 10% 6.3 V X5R 402
C2P5 0.1 UF 10% 6.3 V X5R 402
V_ENET
R2D6 0 OHM 402 5% CH
R2R2 0 OHM 402 5% CH
FB2R1 0.5A 0.1DCR EMPTY 603
C2R6 10 UF 20% 6.3 V X5R 805
C2P3 10 UF 20% 6.3 V X5R 805
C2D5 0.1 UF 10% 25 V EMPTY 603
C2D2 1 UF 10% 10 V EMPTY 402
VDD_V3P3_V2P5IP
VDDA_V3P3_V2P5OP
R2R3 0 OHM 402 5% EMPTY
C2C10 1 UF +80%/-20% 50 V EMPTY 805
C2D1 0.1 UF 10% 25 V X7R 603
C2P2 10 UF 20% 6.3 V X5R 805
ENET_1.8VEXT
U2D1 IC
ETHERNETPHY_KSZ8041NL_AR8032
17 VDDIO_3.3 VDD2.5
3 VDDA_3.3 VDD25_REG
2 VDDPLL_1.8 VDD3
8 XO XO
9 XI/REFCLK XI
10 REXT RST#
11 MDIO MDIO
12 MDC MDC
23 TXEN/TX_EN TXEN
27 TXD3 TXD3
26 TXD2 TXD2
25 TXD1/TXD_1 TXD1
24 TXD0/TXD_0 TXD0
4 RX- RX
5 RX+ RX+
32 RST# REXT
1 GND VDD12_REG
33 GNDSLUG PAD
21 INTRP INTP
18 RXDV/CRSDV/CONFIG2 RX_DV
29 CRS/CONFIG1 CRS
28 COL/CONFIG0 COL
19 RXC RXC
22 TXC TXC
20 RXER/RX_ER/ISO RXER
13 RXD3/PHYAD0 RXD[3]
14 RXD2/PHYAD1 RXD[2]
15 RXD1/RXD_1/PHYAD2 RXD[1]
16 RXD0/RXD_0/DUPLEX RXD[0]
6 TX- TX-
7 TX+ TX+
31 LED1/SPEED LED1
30 LED0/NWAYEN LED0
X819763-001
QFN
R2R9 1 KOHM 1% EMPTY 402
R2R10 4.75 KOHM 1% CH 402
R2D4 4.75 KOHM 1% CH 402
MII_RXDV OUT 29
MII_CRS OUT 29
MII_COL OUT 29
R2R15 1 KOHM 1% EMPTY 402
R2R7 1 KOHM 1% EMPTY 402
R2R12 1 KOHM 1% EMPTY 402
22 IN ENET_CLK
DB2R1
ENET_REF_CLK_OUT
MII_RX_CLK OUT 29
MII_TX_CLK OUT 29
26 IN ENET_RST_N
R2R5 0 OHM 402 5% EMPTY
R2R1 10 KOHM 1% EMPTY 402
R2D1 6.81 KOHM 1% CH 402
C2R5 100 PF 5% 50 V NPO 402
ENET_REXT
R2D2 4.75 KOHM 1% CH 402
29 BI MII_MDIO
29 IN MII_MDC_CLK_OUT
29 IN MII_TXEN
29 IN MII_TXD3
29 IN MII_TXD2
29 IN MII_TXD1
29 IN MII_TXD0
MII_RXER OUT 29
MII_RXD3 OUT 29
MII_RXD2 OUT 29
MII_RXD1 OUT 29
MII_RXD0 OUT 29
R2R11 1 KOHM 1% EMPTY 402
R2R13 1 KOHM 1% EMPTY 402
38 BI ENET_RX_DN
38 BI ENET_RX_DP
ENET_TX_DN BI 38
ENET_TX_DP BI 38
26 IN ENET_RST_N
R2R8 0 OHM 402 5% CH
ENET_RSTN_R
GND_DECOUPLE
R2R6 2.37 KOHM 1% EMPTY 402
R2D3 10 KOHM 1% CH 402
R2R4 0 OHM 5% CH 402
C2R3 0.1 UF 10% 25 V EMPTY 603
C2D4 1 UF 10% 16 V EMPTY 603
ENET_ACT_N
ENET_LINK_N

[PAGE_TITLE=PSB OUT, ETHERNET]

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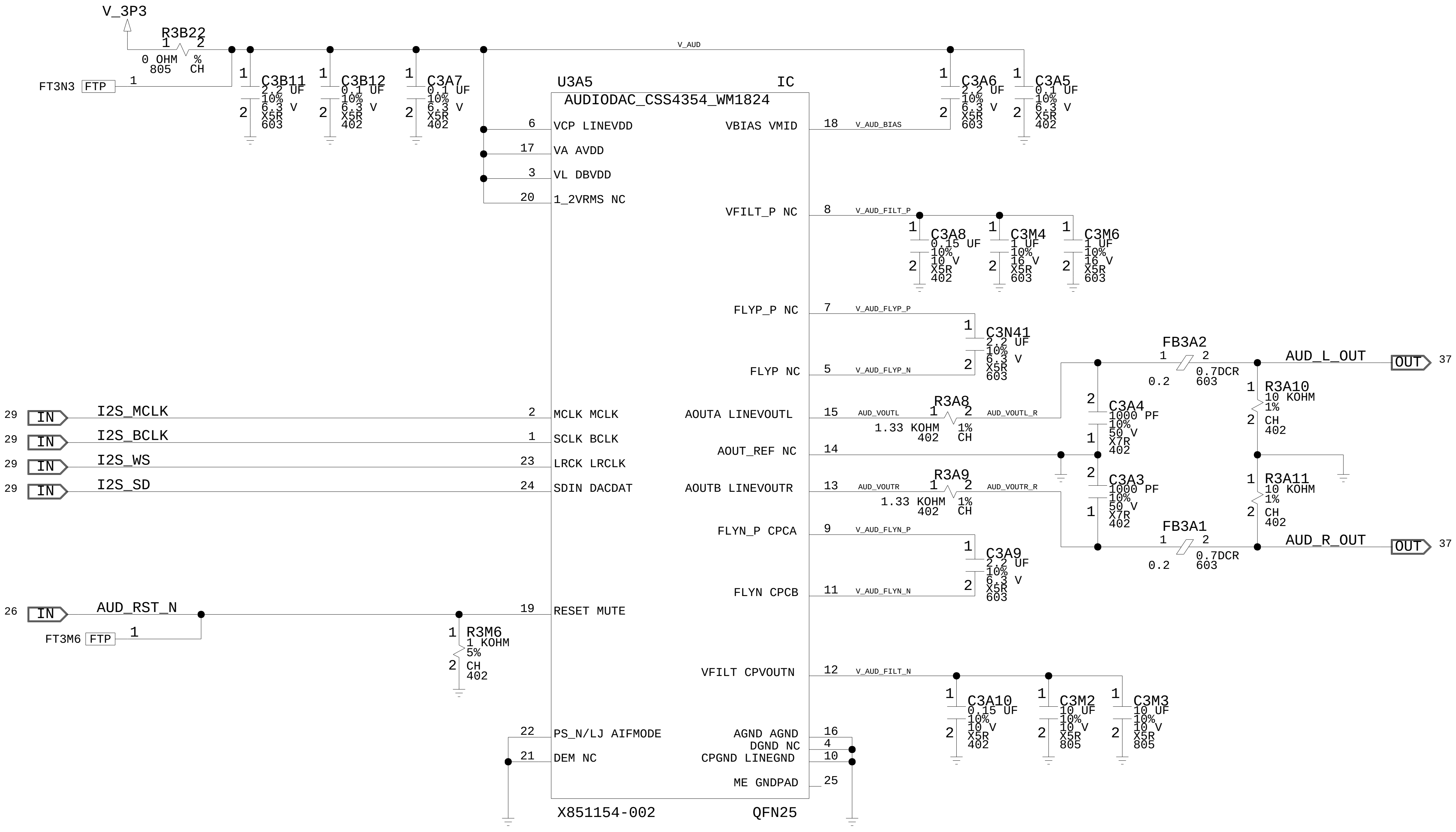
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	32/81	G	1.01

PSB OUT, AUDIO


V_3P3
R3B22
0 OHM % 805 CH
FT3N3 FTP
V_AUD
C3B11 2.2 UF 10% 6.3 V X5R 603
C3B12 0.1 UF 10% 6.3 V X5R 402
C3A7 0.1 UF 10% 6.3 V X5R 402
U3A5 IC
AUDIODAC_CSS4354_WM1824
6 VCP LINEVDD
17 VA AVDD
3 VL DBVDD
20 1_2VRMS NC
2 MCLK MCLK
1 SCLK BCLK
23 LRCK LRCLK
24 SDIN DACDAT
19 RESET MUTE
22 PS_N/LJ AIFMODE
21 DEM NC
X851154-002
QFN25
VBIAS VMID 18 V_AUD_BIAS
VFILT_P NC 8 V_AUD_FILT_P
FLYP_P NC 7 V_AUD_FLYP_P
FLYP NC 5 V_AUD_FLYP_N
AOUTA LINEVOUTL 15 AUD_VOUTL
AOUT_REF NC 14
AOUTB LINEVOUTR 13 AUD_VOUTR
FLYN_P CPCA 9 V_AUD_FLYN_P
FLYN CPCB 11 V_AUD_FLYN_N
VFILT CPVOUTN 12 V_AUD_FILT_N
AGND AGND 16
DGND NC 4
CPGND LINEGND 10
ME GNDPAD 25
C3A6 2.2 UF 10% 6.3 V X5R 603
C3A5 0.1 UF 10% 6.3 V X5R 402
C3A8 0.15 UF 10% 10 V X5R 402
C3M4 1 UF 10% 16 V X5R 603
C3M6 1 UF 10% 16 V X5R 603
C3N41 2.2 UF 10% 6.3 V X5R 603
R3A8 1.33 KOHM 402 1% CH AUD_VOUTL_R
R3A9 1.33 KOHM 402 1% CH AUD_VOUTR_R
C3A4 1000 PF 10% 50 V X7R 402
C3A3 1000 PF 10% 50 V X7R 402
FB3A2 0.2 0.7DCR 603
FB3A1 0.2 0.7DCR 603
R3A10 10 KOHM 1% CH 402
R3A11 10 KOHM 1% CH 402
AUD_L_OUT OUT 37
AUD_R_OUT OUT 37
C3A9 2.2 UF 10% 6.3 V X5R 603
C3A10 0.15 UF 10% 10 V X5R 402
C3M2 10 UF 10% 10 V X5R 805
C3M3 10 UF 10% 10 V X5R 805
29 IN I2S_MCLK
29 IN I2S_BCLK
29 IN I2S_WS
29 IN I2S_SD
26 IN AUD_RST_N
FT3M6 FTP
R3M6 1 KOHM 5% CH 402

[PAGE_TITLE=PSB OUT, AUDIO]

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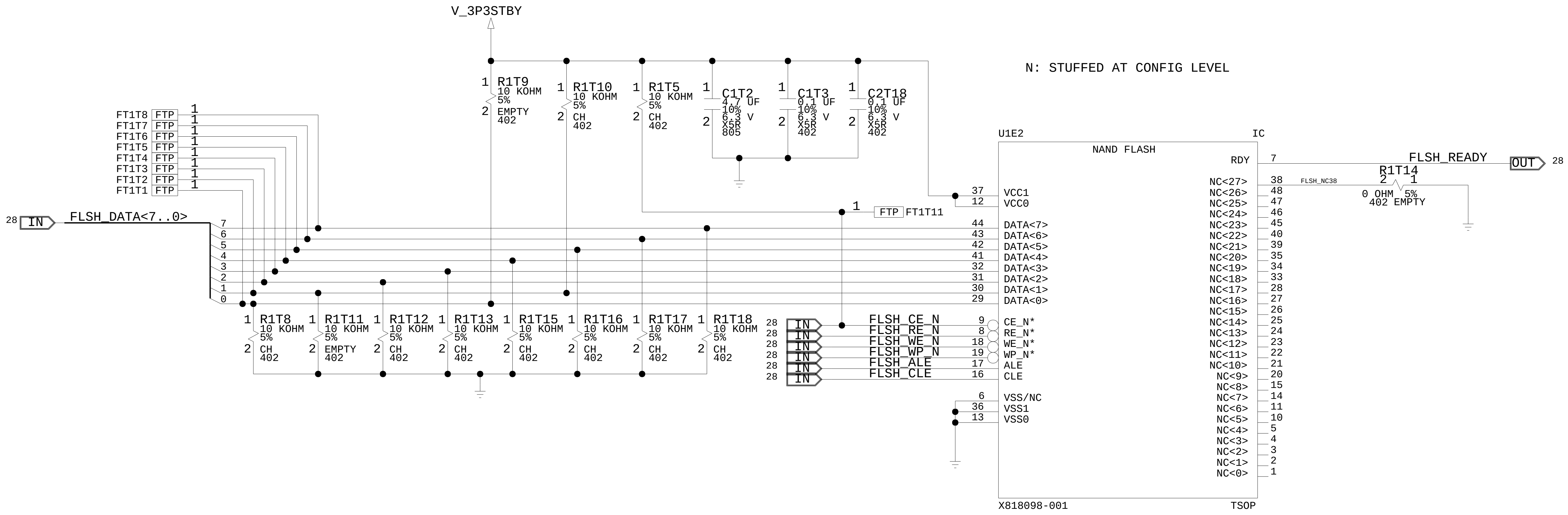
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 33/81	FAB G	REV 1.01

PSB OUT, FLASH


V_3P3STBY
R1T9 10 KOHM 5% EMPTY 402
R1T10 10 KOHM 5% CH 402
R1T5 10 KOHM 5% CH 402
C1T2 4.7 UF 10% 6.3 V X5R 805
C1T3 0.1 UF 10% 6.3 V X5R 402
C2T18 0.1 UF 10% 6.3 V X5R 402
N: STUFFED AT CONFIG LEVEL
FT1T8 FTP
FT1T7 FTP
FT1T6 FTP
FT1T5 FTP
FT1T4 FTP
FT1T3 FTP
FT1T2 FTP
FT1T1 FTP
28 IN FLSH_DATA<7..0>
FTP FT1T11
R1T8 10 KOHM 5% CH 402
R1T11 10 KOHM 5% EMPTY 402
R1T12 10 KOHM 5% CH 402
R1T13 10 KOHM 5% CH 402
R1T15 10 KOHM 5% CH 402
R1T16 10 KOHM 5% CH 402
R1T17 10 KOHM 5% CH 402
R1T18 10 KOHM 5% CH 402
28 IN FLSH_CE_N
28 IN FLSH_RE_N
28 IN FLSH_WE_N
28 IN FLSH_WP_N
28 IN FLSH_ALE
28 IN FLSH_CLE
U1E2 IC
NAND FLASH
37 VCC1
12 VCC0
44 DATA<7>
43 DATA<6>
42 DATA<5>
41 DATA<4>
32 DATA<3>
31 DATA<2>
30 DATA<1>
29 DATA<0>
9 CE_N*
8 RE_N*
18 WE_N*
19 WP_N*
17 ALE
16 CLE
6 VSS/NC
36 VSS1
13 VSS0
RDY 7
NC<27> 38
NC<26> 48
NC<25> 47
NC<24> 46
NC<23> 45
NC<22> 40
NC<21> 39
NC<20> 35
NC<19> 34
NC<18> 33
NC<17> 28
NC<16> 27
NC<15> 26
NC<14> 25
NC<13> 24
NC<12> 23
NC<11> 22
NC<10> 21
NC<9> 20
NC<8> 15
NC<7> 14
NC<6> 11
NC<5> 10
NC<4> 5
NC<3> 4
NC<2> 3
NC<1> 2
NC<0> 1
X818098-001 TSOP
FLSH_READY OUT 28
FLSH_NC38
R1T14 0 OHM 5% 402 EMPTY

XSB SOUTHBRIDGE

N: RETAIL=16MB
N: XDK=64MB

		FLSH_DATA0	
		0	1
FLSH_DATA1	0	8MB	16MB
	1	32MB	64MB

PSB SOUTHBRIDGE

FLSH_DATA[1:0]	FLASH CONFIGURATION	
0X0	0.5KB, 16KB BLOCKS, 16MB	
0X1	0.5KB, 16KB BLOCKS, 16MB	RETAIL
0X2	2KB PAGES, 128KB BLOCKS, VARIOUS SIZES (256MB)	XDK
0X3	4KB PAGES, 256KB BLOCKS, VARIOUS SIZES	

[PAGE_TITLE=PSB OUT, FLASH]

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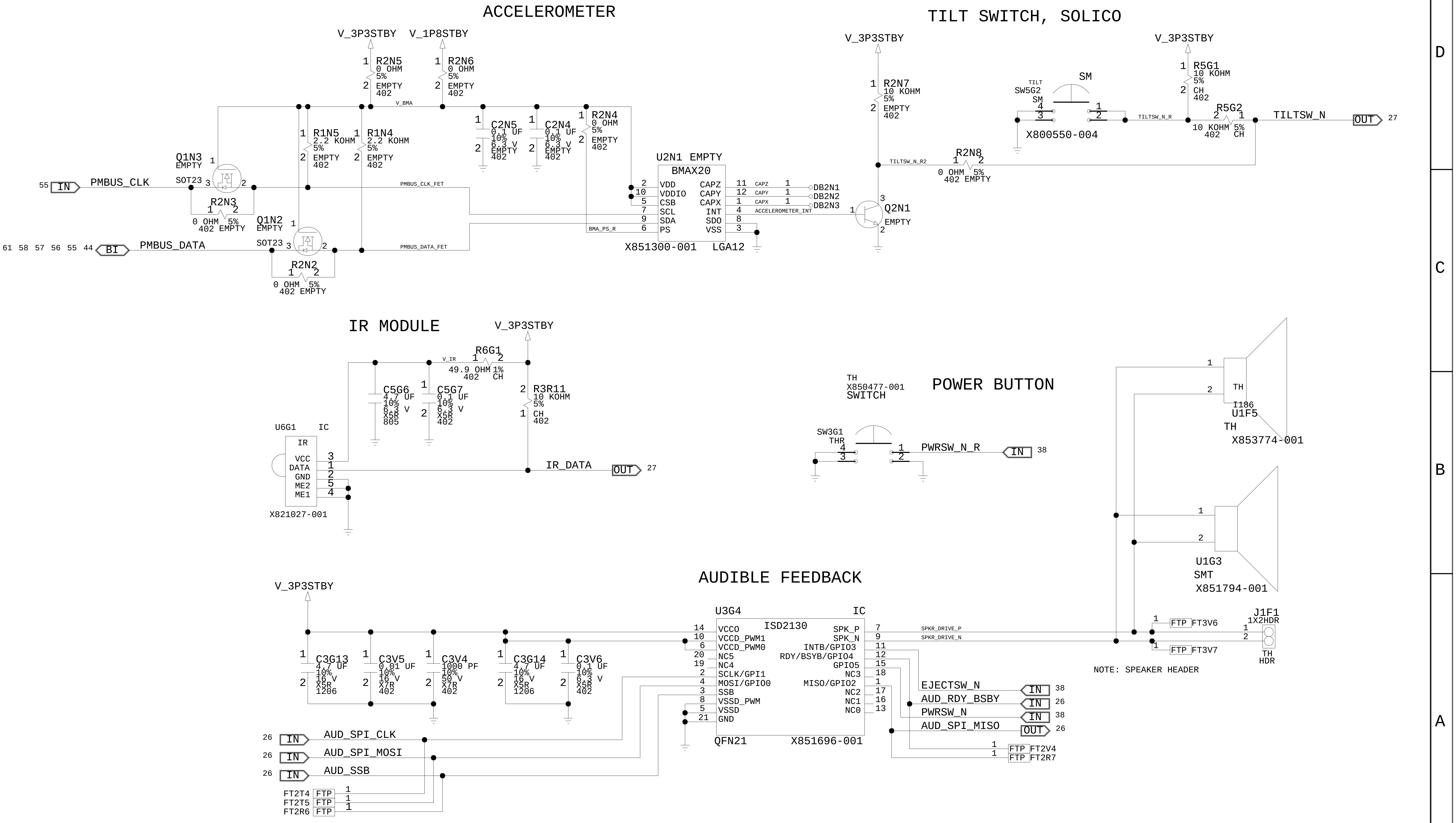
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 34/81	FAB G	REV 1.01

CONN, INFARED + ACCELEROMETER + SWITCHES + AUDIBLE F/B


ACCELEROMETER
V_3P3STBY
V_1P8STBY
R2N5 0 OHM 5% EMPTY 402
R2N6 0 OHM 5% EMPTY 402
V_BMA
C2N5 0.1 UF 10% 6.3 V EMPTY 402
C2N4 0.1 UF 10% 6.3 V EMPTY 402
R2N4 0 OHM 5% EMPTY 402
R1N5 2.2 KOHM 5% EMPTY 402
R1N4 2.2 KOHM 5% EMPTY 402
Q1N3 EMPTY SOT23
55 IN PMBUS_CLK
R2N3 0 OHM 5% 402 EMPTY
Q1N2 EMPTY SOT23
61 58 57 56 55 44 BI PMBUS_DATA
R2N2 0 OHM 5% 402 EMPTY
PMBUS_CLK_FET
PMBUS_DATA_FET
BMA_PS_R
U2N1 EMPTY
BMAX20
VDD VDDIO CSB SCL SDA PS
CAPZ CAPY CAPX INT SDO VSS
X851300-001 LGA12
CAPZ CAPY CAPX ACCELEROMETER_INT
DB2N1 DB2N2 DB2N3
Q2N1 EMPTY
TILT SWITCH, SOLICO
V_3P3STBY
R2N7 10 KOHM 5% EMPTY 402
TILTSW_N_R2
R2N8 0 OHM 5% 402 EMPTY
TILT SW5G2 SM
SM
X800550-004
TILTSW_N_R
V_3P3STBY
R5G1 10 KOHM 5% CH 402
R5G2 10 KOHM 402 5% CH
TILTSW_N
OUT 27
IR MODULE
V_3P3STBY
R6G1 49.9 OHM 1% 402 CH
V_IR
C5G6 4.7 UF 10% 6.3 V X5R 805
C5G7 0.1 UF 10% 6.3 V X5R 402
R3R11 10 KOHM 5% CH 402
U6G1 IC
IR VCC DATA GND ME2 ME1
X821027-001
IR_DATA
OUT 27
TH X850477-001 SWITCH
POWER BUTTON
SW3G1 THR
PWRSW_N_R
IN 38
TH I186 U1F5 TH X853774-001
U1G3 SMT X851794-001
AUDIBLE FEEDBACK
V_3P3STBY
C3G13 4.7 UF 10% 16 V X5R 1206
C3V5 0.01 UF 10% 16 V X7R 402
C3V4 1000 PF 10% 50 V X7R 402
C3G14 4.7 UF 10% 16 V X5R 1206
C3V6 0.1 UF 10% 6.3 V X5R 402
U3G4 IC ISD2130
VCCO VCCD_PWM1 VCCD_PWM0 NC5 NC4 SCLK/GPI1 MOSI/GPIO0 SSB VSSD_PWM VSSD GND
SPK_P SPK_N INTB/GPIO3 RDY/BSYB/GPIO4 GPIO5 NC3 MISO/GPIO2 NC2 NC1 NC0
QFN21 X851696-001
SPKR_DRIVE_P
SPKR_DRIVE_N
FTP FT3V6
FTP FT3V7
J1F1 1X2HDR TH HDR
NOTE: SPEAKER HEADER
EJECTSW_N IN 38
AUD_RDY_BSBY IN 26
PWRSW_N IN 38
AUD_SPI_MISO OUT 26
FTP FT2V4
FTP FT2R7
26 IN AUD_SPI_CLK
26 IN AUD_SPI_MOSI
26 IN AUD_SSB
FT2T4 FTP
FT2T5 FTP
FT2R6 FTP

[PAGE_TITLE=CONN,INFRARED+ACCELEROMETER+SWITCHES+AUDIBLE F/B]

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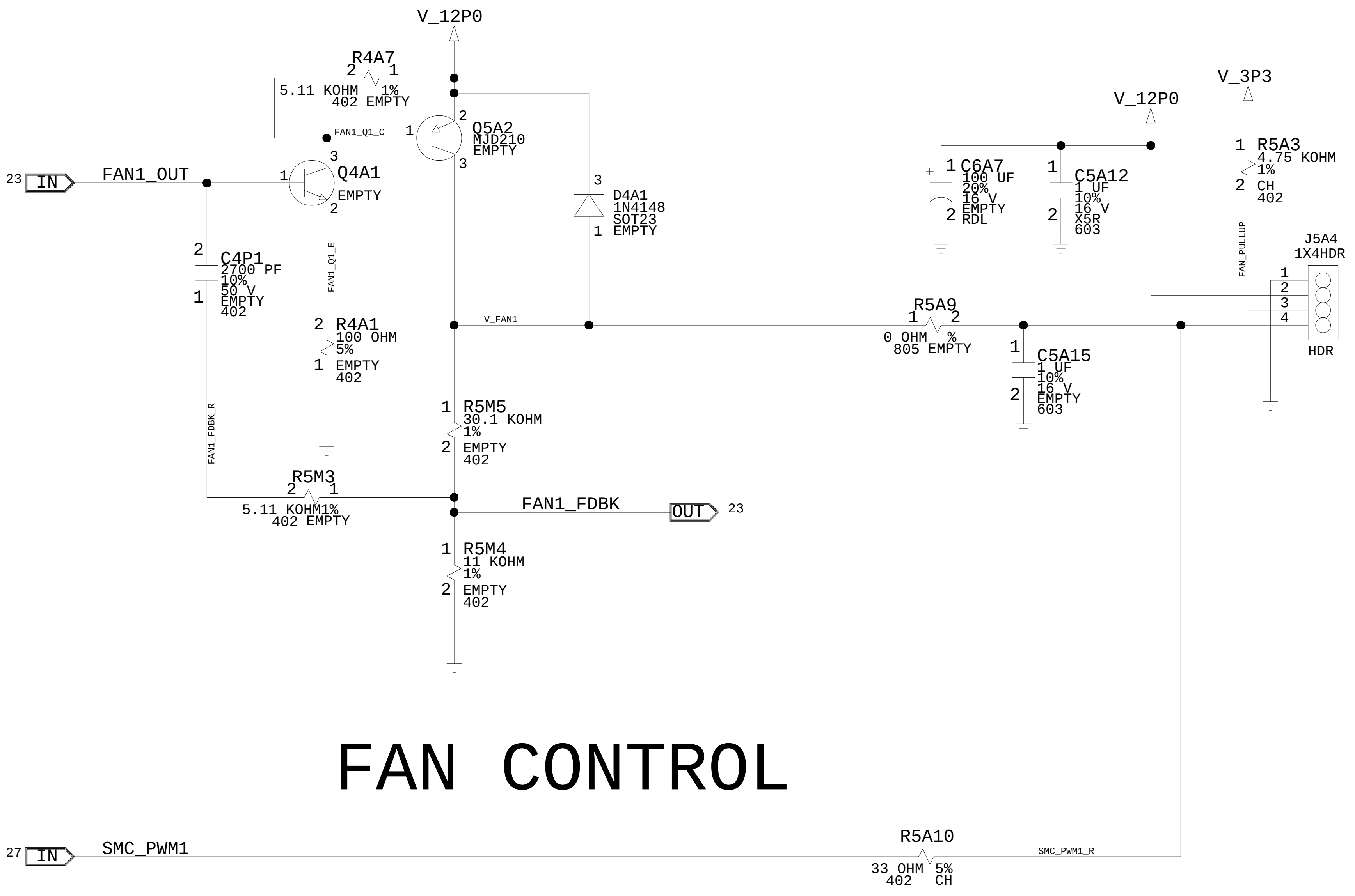
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	35/81	G	1.01

CONN, FAN


V_12P0
R4A7
2 1
5.11 KOHM 1%
402 EMPTY
FAN1_Q1_C
1
2
Q5A2
MJD210
EMPTY
3
23 IN
FAN1_OUT
1
3
Q4A1
EMPTY
2
3
D4A1
1N4148
SOT23
1 EMPTY
2
C4P1
2700 PF
10%
50 V
EMPTY
1
402
FAN1_Q1_E
2 R4A1
100 OHM
5%
1 EMPTY
402
V_FAN1
FAN1_FDBK_R
1 R5M5
30.1 KOHM
1%
2 EMPTY
402
R5M3
2 1
5.11 KOHM1%
402 EMPTY
FAN1_FDBK
OUT 23
1 R5M4
11 KOHM
1%
2 EMPTY
402
V_12P0
V_3P3
1 C6A7
100 UF
20%
16 V
2 EMPTY
RDL
1 C5A12
1 UF
10%
16 V
2 X5R
603
1 R5A3
4.75 KOHM
1%
2 CH
402
FAN_PULLUP
J5A4
1X4HDR
1
2
3
4
HDR
R5A9
1 2
0 OHM %
805 EMPTY
1 C5A15
1 UF
10%
16 V
2 EMPTY
603
27 IN
SMC_PWM1
R5A10
33 OHM 5%
402 CH
SMC_PWM1_R

FAN CONTROL

[PAGE_TITLE= CONN, FAN]

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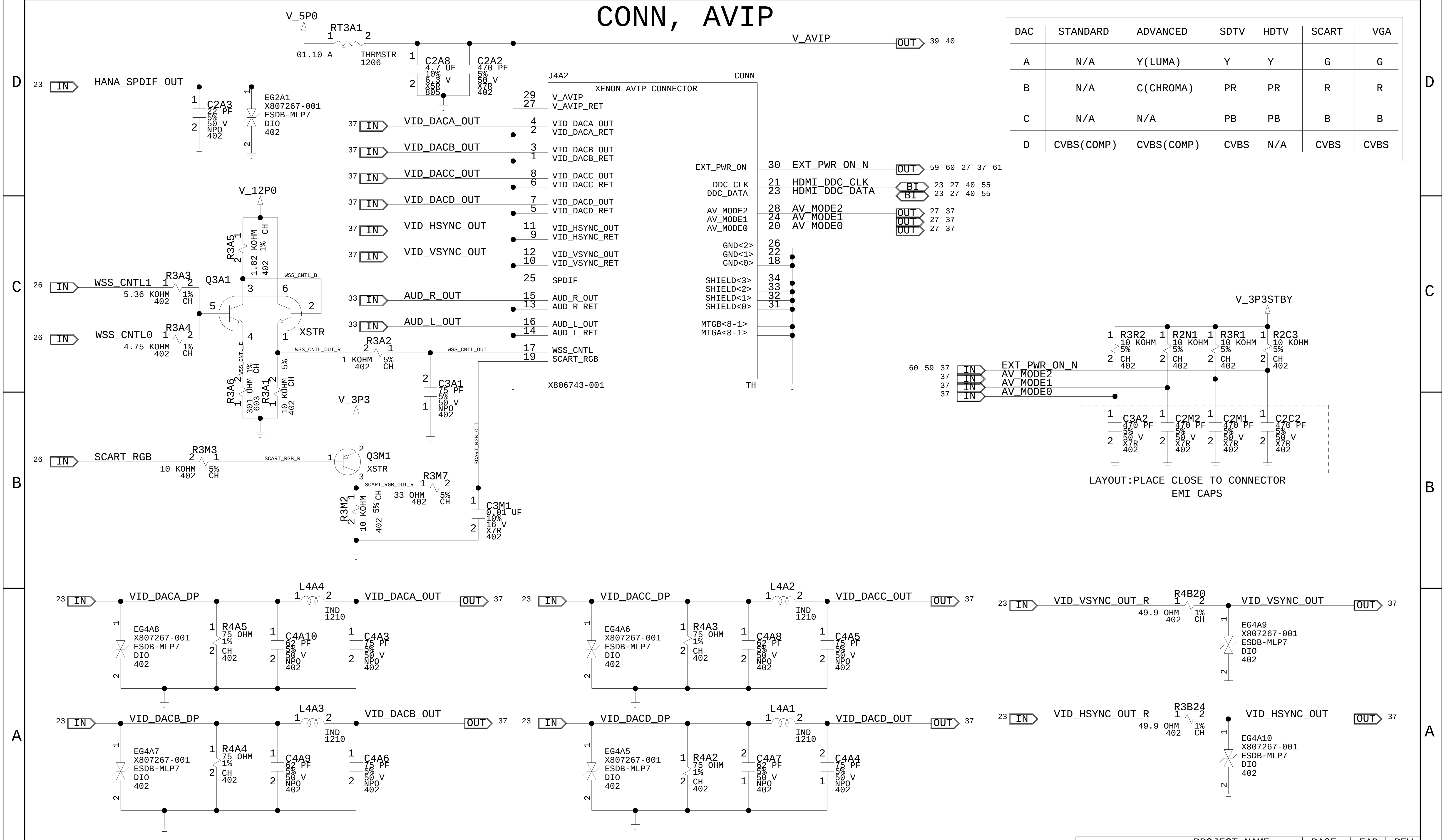
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 36/81	FAB G	REV 1.01

CONN, AVIP

DAC	STANDARD	ADVANCED	SDTV	HDTV	SCART	VGA
A	N/A	Y(LUMA)	Y	Y	G	G
B	N/A	C(CHROMA)	PR	PR	R	R
C	N/A	N/A	PB	PB	B	B
D	CVBS(COMP)	CVBS(COMP)	CVBS	N/A	CVBS	CVBS


V_5P0
RT3A1
THRMSTR 1206
01.10 A
C2A8 4.7 UF 10% 6.3 V X5R 805
C2A2 470 PF 5% 50 V X7R 402
V_AVIP
OUT 39 40
HANA_SPDIF_OUT
C2A3 22 PF 5% 50 V NPO 402
EG2A1 X807267-001 ESDB-MLP7 DIO 402
J4A2
XENON AVIP CONNECTOR
CONN
V_AVIP
V_AVIP_RET
VID_DACA_OUT
VID_DACA_RET
VID_DACB_OUT
VID_DACB_RET
VID_DACC_OUT
VID_DACC_RET
VID_DACD_OUT
VID_DACD_RET
VID_HSYNC_OUT
VID_HSYNC_RET
VID_VSYNC_OUT
VID_VSYNC_RET
SPDIF
AUD_R_OUT
AUD_R_RET
AUD_L_OUT
AUD_L_RET
WSS_CNTL
SCART_RGB
X806743-001
TH
EXT_PWR_ON
DDC_CLK
DDC_DATA
AV_MODE2
AV_MODE1
AV_MODE0
GND<2>
GND<1>
GND<0>
SHIELD<3>
SHIELD<2>
SHIELD<1>
SHIELD<0>
MTGB<8-1>
MTGA<8-1>
EXT_PWR_ON_N
OUT 59 60 27 37 61
HDMI_DDC_CLK
HDMI_DDC_DATA
BI 23 27 40 55
AV_MODE2
AV_MODE1
AV_MODE0
OUT 27 37
V_12P0
R3A5 1.82 KOHM 1% CH 402
WSS_CNTL_B
WSS_CNTL1
R3A3 5.36 KOHM 1% CH 402
Q3A1
XSTR
WSS_CNTL0
R3A4 4.75 KOHM 1% CH 402
R3A2 1 KOHM 5% CH 402
WSS_CNTL_OUT_R
WSS_CNTL_OUT
WSS_CNTL_E
R3A6 301 OHM 1% CH 603
R3A1 10 KOHM 5% CH 402
C3A1 75 PF 5% 50 V NPO 402
V_3P3
SCART_RGB
R3M3 10 KOHM 5% CH 402
SCART_RGB_R
Q3M1
XSTR
SCART_RGB_OUT_R
R3M7 33 OHM 5% CH 402
SCART_RGB_OUT
R3M2 10 KOHM 5% CH 402
C3M1 0.01 UF 10% 16 V X7R 402
V_3P3STBY
R3R2 10 KOHM 5% CH 402
R2N1 10 KOHM 5% CH 402
R3R1 10 KOHM 5% CH 402
R2C3 10 KOHM 5% CH 402
EXT_PWR_ON_N
AV_MODE2
AV_MODE1
AV_MODE0
C3A2 470 PF 5% 50 V X7R 402
C2M2 470 PF 5% 50 V X7R 402
C2M1 470 PF 5% 50 V X7R 402
C2C2 470 PF 5% 50 V X7R 402
LAYOUT:PLACE CLOSE TO CONNECTOR
EMI CAPS
VID_DACA_DP
EG4A8 X807267-001 ESDB-MLP7 DIO 402
R4A5 75 OHM 1% CH 402
L4A4 IND 1210
C4A10 62 PF 5% 50 V NPO 402
C4A3 75 PF 5% 50 V NPO 402
VID_DACA_OUT
VID_DACB_DP
EG4A7 X807267-001 ESDB-MLP7 DIO 402
R4A4 75 OHM 1% CH 402
L4A3 IND 1210
C4A9 62 PF 5% 50 V NPO 402
C4A6 75 PF 5% 50 V NPO 402
VID_DACB_OUT
VID_DACC_DP
EG4A6 X807267-001 ESDB-MLP7 DIO 402
R4A3 75 OHM 1% CH 402
L4A2 IND 1210
C4A8 62 PF 5% 50 V NPO 402
C4A5 75 PF 5% 50 V NPO 402
VID_DACC_OUT
VID_DACD_DP
EG4A5 X807267-001 ESDB-MLP7 DIO 402
R4A2 75 OHM 1% CH 402
L4A1 IND 1210
C4A7 62 PF 5% 50 V NPO 402
C4A4 75 PF 5% 50 V NPO 402
VID_DACD_OUT
VID_VSYNC_OUT_R
R4B20 49.9 OHM 1% CH 402
VID_VSYNC_OUT
EG4A9 X807267-001 ESDB-MLP7 DIO 402
VID_HSYNC_OUT_R
R3B24 49.9 OHM 1% CH 402
VID_HSYNC_OUT
EG4A10 X807267-001 ESDB-MLP7 DIO 402

[PAGE_TITLE=[CONN, AVIP]

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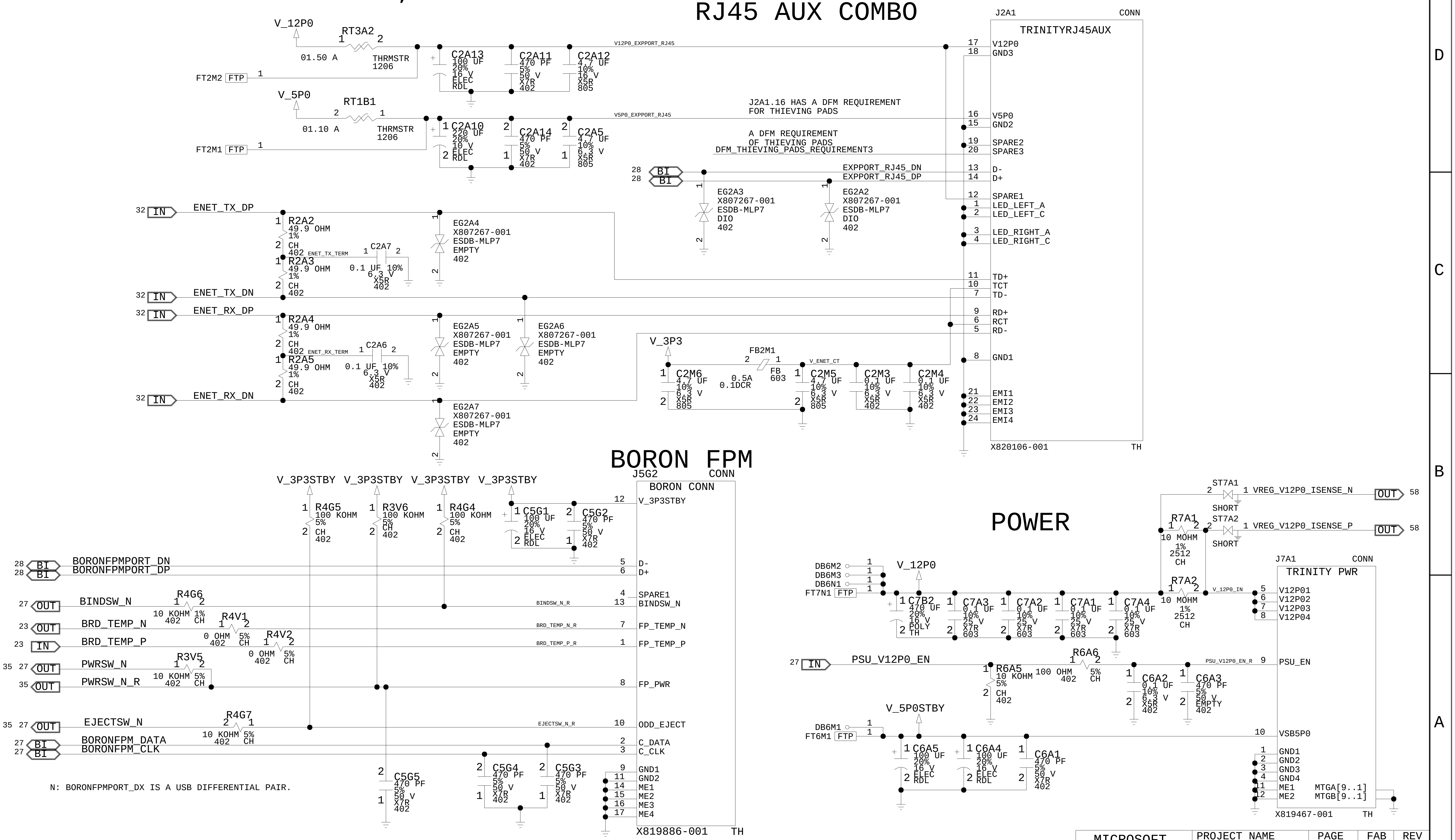
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	37/81	G	1.01

CONN, RJ45 USB AUX COMBO + BORON + PWR


RJ45 AUX COMBO
V_12P0
RT3A2
01.50 A
THRMSTR
1206
FT2M2 FTP
C2A13 100 UF 20% 16 V ELEC RDL
C2A11 470 PF 5% 50 V X7R 402
C2A12 4.7 UF 10% 16 V X5R 805
V12P0_EXPPORT_RJ45
V_5P0
RT1B1
01.10 A
THRMSTR
1206
FT2M1 FTP
C2A10 220 UF 20% 10 V ELEC RDL
C2A14 470 PF 5% 50 V X7R 402
C2A5 4.7 UF 10% 6.3 V X5R 805
V5P0_EXPPORT_RJ45
J2A1.16 HAS A DFM REQUIREMENT
FOR THIEVING PADS
A DFM REQUIREMENT
OF THIEVING PADS
DFM_THIEVING_PADS_REQUIREMENT3
28 BI
28 BI
EXPPORT_RJ45_DN
EXPPORT_RJ45_DP
EG2A3 X807267-001 ESDB-MLP7 DIO 402
EG2A2 X807267-001 ESDB-MLP7 DIO 402
J2A1 CONN
TRINITYRJ45AUX
17 V12P0
18 GND3
16 V5P0
15 GND2
19 SPARE2
20 SPARE3
13 D-
14 D+
12 SPARE1
1 LED_LEFT_A
2 LED_LEFT_C
3 LED_RIGHT_A
4 LED_RIGHT_C
11 TD+
10 TCT
7 TD-
9 RD+
6 RCT
5 RD-
8 GND1
21 EMI1
22 EMI2
23 EMI3
24 EMI4
X820106-001 TH
32 IN ENET_TX_DP
R2A2 49.9 OHM 1% CH 402
ENET_TX_TERM
C2A7 0.1 UF 10% 6.3 V X5R 402
R2A3 49.9 OHM 1% CH 402
EG2A4 X807267-001 ESDB-MLP7 EMPTY 402
32 IN ENET_TX_DN
32 IN ENET_RX_DP
R2A4 49.9 OHM 1% CH 402
ENET_RX_TERM
C2A6 0.1 UF 10% 6.3 V X5R 402
R2A5 49.9 OHM 1% CH 402
EG2A5 X807267-001 ESDB-MLP7 EMPTY 402
EG2A6 X807267-001 ESDB-MLP7 EMPTY 402
32 IN ENET_RX_DN
EG2A7 X807267-001 ESDB-MLP7 EMPTY 402
V_3P3
FB2M1
FB 603
0.5A 0.1DCR
V_ENET_CT
C2M6 4.7 UF 10% 6.3 V X5R 805
C2M5 4.7 UF 10% 6.3 V X5R 805
C2M3 0.1 UF 10% 6.3 V X5R 402
C2M4 0.1 UF 10% 6.3 V X5R 402
BORON FPM
J5G2 CONN
BORON CONN
V_3P3STBY
V_3P3STBY
V_3P3STBY
V_3P3STBY
R4G5 100 KOHM 5% CH 402
R3V6 100 KOHM 5% CH 402
R4G4 100 KOHM 5% CH 402
C5G1 100 UF 20% 16 V ELEC RDL
C5G2 470 PF 5% 50 V X7R 402
12 V_3P3STBY
28 BI BORONFPMPORT_DN
28 BI BORONFPMPORT_DP
5 D-
6 D+
4 SPARE1
13 BINDSW_N
27 OUT BINDSW_N
R4G6 10 KOHM 1% 402 CH
BINDSW_N_R
23 OUT BRD_TEMP_N
R4V1 0 OHM 5% 402 CH
BRD_TEMP_N_R
7 FP_TEMP_N
23 IN BRD_TEMP_P
R4V2 0 OHM 5% 402 CH
BRD_TEMP_P_R
1 FP_TEMP_P
35 27 OUT PWRSW_N
R3V5 10 KOHM 5% 402 CH
35 OUT PWRSW_N_R
8 FP_PWR
35 27 OUT EJECTSW_N
R4G7 10 KOHM 5% 402 CH
EJECTSW_N_R
10 ODD_EJECT
27 BI BORONFPM_DATA
27 BI BORONFPM_CLK
2 C_DATA
3 C_CLK
9 GND1
11 GND2
14 ME1
15 ME2
16 ME3
17 ME4
X819886-001 TH
C5G5 470 PF 5% 50 V X7R 402
C5G4 470 PF 5% 50 V X7R 402
C5G3 470 PF 5% 50 V X7R 402
N: BORONFPMPORT_DX IS A USB DIFFERENTIAL PAIR.
POWER
ST7A1 SHORT
1 VREG_V12P0_ISENSE_N OUT 58
ST7A2 SHORT
1 VREG_V12P0_ISENSE_P OUT 58
R7A1 10 MOHM 1% 2512 CH
R7A2 10 MOHM 1% 2512 CH
V_12P0_IN
DB6M2
DB6M3
DB6N1
FT7N1 FTP
V_12P0
C7B2 470 UF 20% 16 V POLY TH
C7A3 0.1 UF 10% 25 V X7R 603
C7A2 0.1 UF 10% 25 V X7R 603
C7A1 0.1 UF 10% 25 V X7R 603
C7A4 0.1 UF 10% 25 V X7R 603
J7A1 CONN
TRINITY PWR
5 V12P01
6 V12P02
7 V12P03
8 V12P04
27 IN PSU_V12P0_EN
R6A6 100 OHM 5% 402 CH
R6A5 10 KOHM 5% CH 402
PSU_EN_R
C6A2 0.1 UF 10% 6.3 V X5R 402
C6A3 470 PF 5% 50 V EMPTY 402
9 PSU_EN
V_5P0STBY
DB6M1
FT6M1 FTP
C6A5 100 UF 20% 16 V ELEC RDL
C6A4 100 UF 20% 16 V ELEC RDL
C6A1 470 PF 5% 50 V X7R 402
10 VSB5P0
1 GND1
2 GND2
3 GND3
4 GND4
11 ME1
12 ME2
MTGA[9..1]
MTGB[9..1]
X819467-001 TH

[PAGE_TITLE=CONN, RJ45 AUX COMBO + BORON + PWR]

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MICROSOFT
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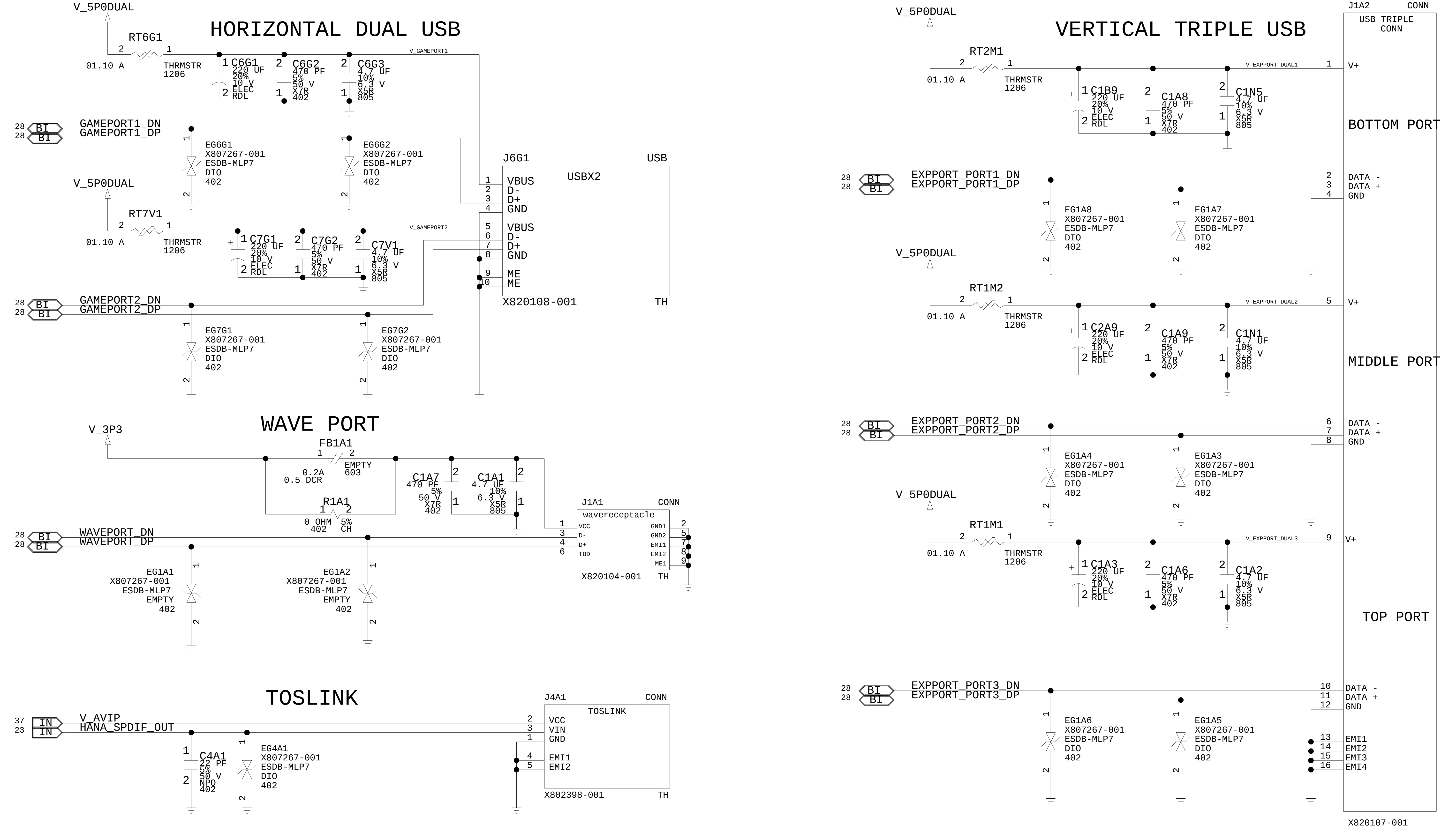
TRINITY_XDK	38/81	G	1.01

CONN, USB + MEM PORTS + TOSLINK + WAVEPORT

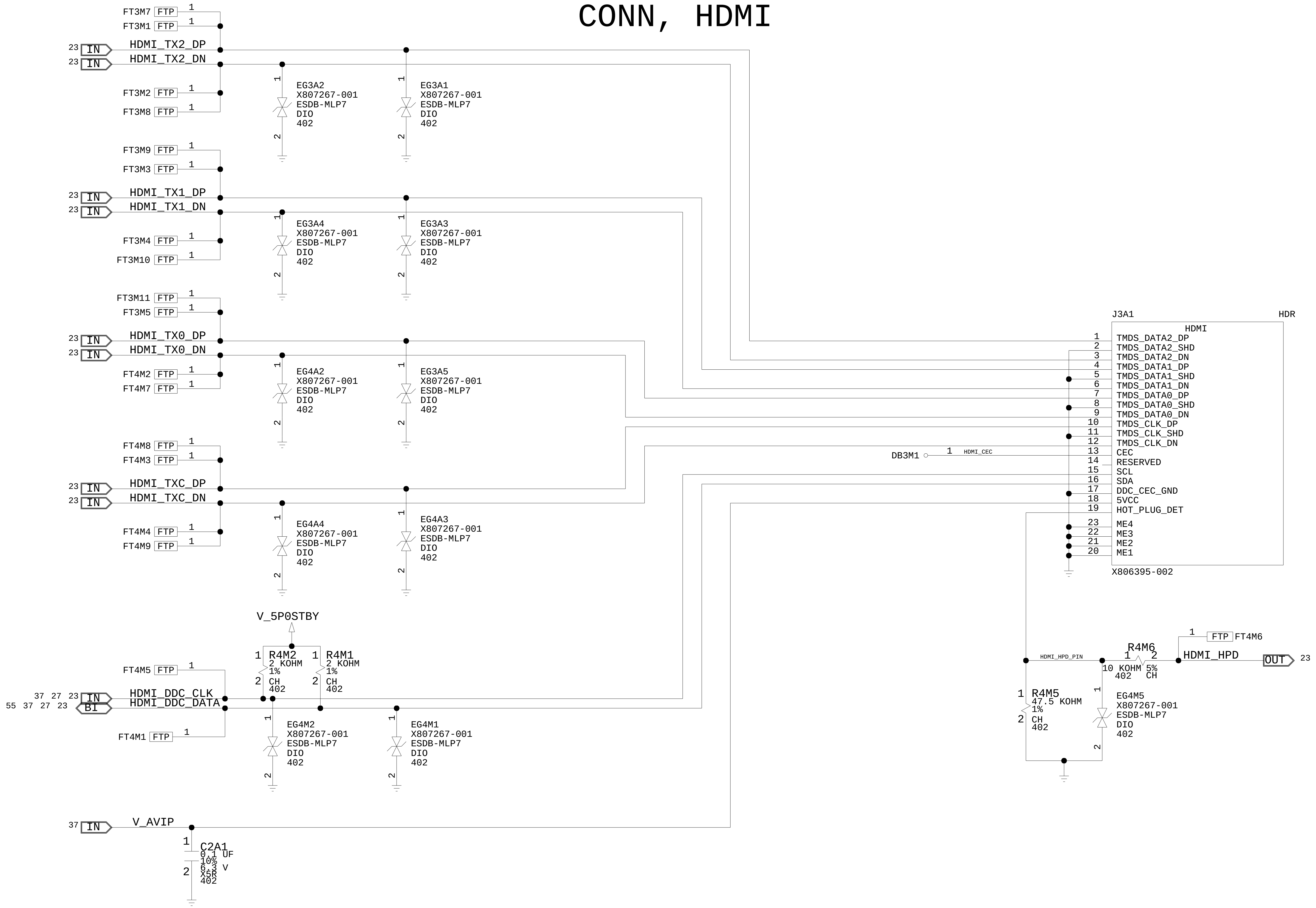
N: ALL DIFFERENTIAL PAIRS ON THIS PAGE ARE USB DIFFERENTIAL PAIRS.


HORIZONTAL DUAL USB
V_5P0DUAL
RT6G1
01.10 A
THRMSTR 1206
C6G1 220 UF 20% 10 V ELEC RDL
C6G2 470 PF 5% 50 V X7R 402
C6G3 4.7 UF 10% 6.3 V X5R 805
V_GAMEPORT1
GAMEPORT1_DN
GAMEPORT1_DP
EG6G1 X807267-001 ESDB-MLP7 DIO 402
EG6G2 X807267-001 ESDB-MLP7 DIO 402
RT7V1
C7G1 220 UF 20% 10 V ELEC RDL
C7G2 470 PF 5% 50 V X7R 402
C7V1 4.7 UF 10% 6.3 V X5R 805
V_GAMEPORT2
GAMEPORT2_DN
GAMEPORT2_DP
EG7G1 X807267-001 ESDB-MLP7 DIO 402
EG7G2 X807267-001 ESDB-MLP7 DIO 402
J6G1 USB
USBX2
VBUS
D-
D+
GND
ME
X820108-001 TH
BI
28
WAVE PORT
V_3P3
FB1A1
0.2A 0.5 DCR
EMPTY 603
R1A1 0 OHM 402 5% CH
C1A7 470 PF 5% 50 V X7R 402
C1A1 4.7 UF 10% 6.3 V X5R 805
WAVEPORT_DN
WAVEPORT_DP
EG1A1 X807267-001 ESDB-MLP7 EMPTY 402
EG1A2 X807267-001 ESDB-MLP7 EMPTY 402
J1A1 CONN
wavereceptacle
VCC
TBD
GND1
GND2
EMI1
EMI2
ME1
X820104-001 TH
TOSLINK
IN
37
23
V_AVIP
HANA_SPDIF_OUT
C4A1 22 PF 5% 50 V NPO 402
EG4A1 X807267-001 ESDB-MLP7 DIO 402
J4A1 CONN
TOSLINK
VIN
X802398-001 TH
VERTICAL TRIPLE USB
RT2M1
C1B9 220 UF 20% 10 V ELEC RDL
C1A8 470 PF 5% 50 V X7R 402
C1N5 4.7 UF 10% 6.3 V X5R 805
V_EXPPORT_DUAL1
J1A2 CONN TH
USB TRIPLE CONN
V+
BOTTOM PORT
EXPPORT_PORT1_DN
EXPPORT_PORT1_DP
DATA -
DATA +
EG1A8 X807267-001 ESDB-MLP7 DIO 402
EG1A7 X807267-001 ESDB-MLP7 DIO 402
RT1M2
C2A9 220 UF 20% 10 V ELEC RDL
C1A9 470 PF 5% 50 V X7R 402
C1N1 4.7 UF 10% 6.3 V X5R 805
V_EXPPORT_DUAL2
MIDDLE PORT
EXPPORT_PORT2_DN
EXPPORT_PORT2_DP
EG1A4 X807267-001 ESDB-MLP7 DIO 402
EG1A3 X807267-001 ESDB-MLP7 DIO 402
RT1M1
C1A3 220 UF 20% 10 V ELEC RDL
C1A6 470 PF 5% 50 V X7R 402
C1A2 4.7 UF 10% 6.3 V X5R 805
V_EXPPORT_DUAL3
TOP PORT
EXPPORT_PORT3_DN
EXPPORT_PORT3_DP
EG1A6 X807267-001 ESDB-MLP7 DIO 402
EG1A5 X807267-001 ESDB-MLP7 DIO 402
EMI3
EMI4
X820107-001

[PAGE_TITLE=CONN, MEMORY PORTS + GAME PORTS]

DRAWING	MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
Wed Feb 10 16:23:31 2010		TRINITY_XDK	39/81	G	1.01

CONN, HDMI


FT3M7 FTP 1
FT3M1 FTP 1
23 IN HDMI_TX2_DP
23 IN HDMI_TX2_DN
FT3M2 FTP 1
FT3M8 FTP 1
EG3A2 X807267-001 ESDB-MLP7 DIO 402
EG3A1 X807267-001 ESDB-MLP7 DIO 402
FT3M9 FTP 1
FT3M3 FTP 1
23 IN HDMI_TX1_DP
23 IN HDMI_TX1_DN
FT3M4 FTP 1
FT3M10 FTP 1
EG3A4 X807267-001 ESDB-MLP7 DIO 402
EG3A3 X807267-001 ESDB-MLP7 DIO 402
FT3M11 FTP 1
FT3M5 FTP 1
23 IN HDMI_TX0_DP
23 IN HDMI_TX0_DN
FT4M2 FTP 1
FT4M7 FTP 1
EG4A2 X807267-001 ESDB-MLP7 DIO 402
EG3A5 X807267-001 ESDB-MLP7 DIO 402
FT4M8 FTP 1
FT4M3 FTP 1
23 IN HDMI_TXC_DP
23 IN HDMI_TXC_DN
FT4M4 FTP 1
FT4M9 FTP 1
EG4A4 X807267-001 ESDB-MLP7 DIO 402
EG4A3 X807267-001 ESDB-MLP7 DIO 402
V_5P0STBY
R4M2 2 KOHM 1% CH 402
R4M1 2 KOHM 1% CH 402
FT4M5 FTP 1
37 27 23 IN HDMI_DDC_CLK
55 37 27 23 BI HDMI_DDC_DATA
FT4M1 FTP 1
EG4M2 X807267-001 ESDB-MLP7 DIO 402
EG4M1 X807267-001 ESDB-MLP7 DIO 402
37 IN V_AVIP
C2A1 0.1 UF 10% 6.3 V X5R 402
J3A1 HDR
HDMI
1 TMDS_DATA2_DP
2 TMDS_DATA2_SHD
3 TMDS_DATA2_DN
4 TMDS_DATA1_DP
5 TMDS_DATA1_SHD
6 TMDS_DATA1_DN
7 TMDS_DATA0_DP
8 TMDS_DATA0_SHD
9 TMDS_DATA0_DN
10 TMDS_CLK_DP
11 TMDS_CLK_SHD
12 TMDS_CLK_DN
13 CEC
14 RESERVED
15 SCL
16 SDA
17 DDC_CEC_GND
18 5VCC
19 HOT_PLUG_DET
23 ME4
22 ME3
21 ME2
20 ME1
X806395-002
DB3M1 1 HDMI_CEC
HDMI_HPD_PIN
R4M6 10 KOHM 5% 402 CH
FTP FT4M6
HDMI_HPD OUT 23
R4M5 47.5 KOHM 1% CH 402
EG4M5 X807267-001 ESDB-MLP7 DIO 402

[PAGE_TITLE=CONN, HDMI]

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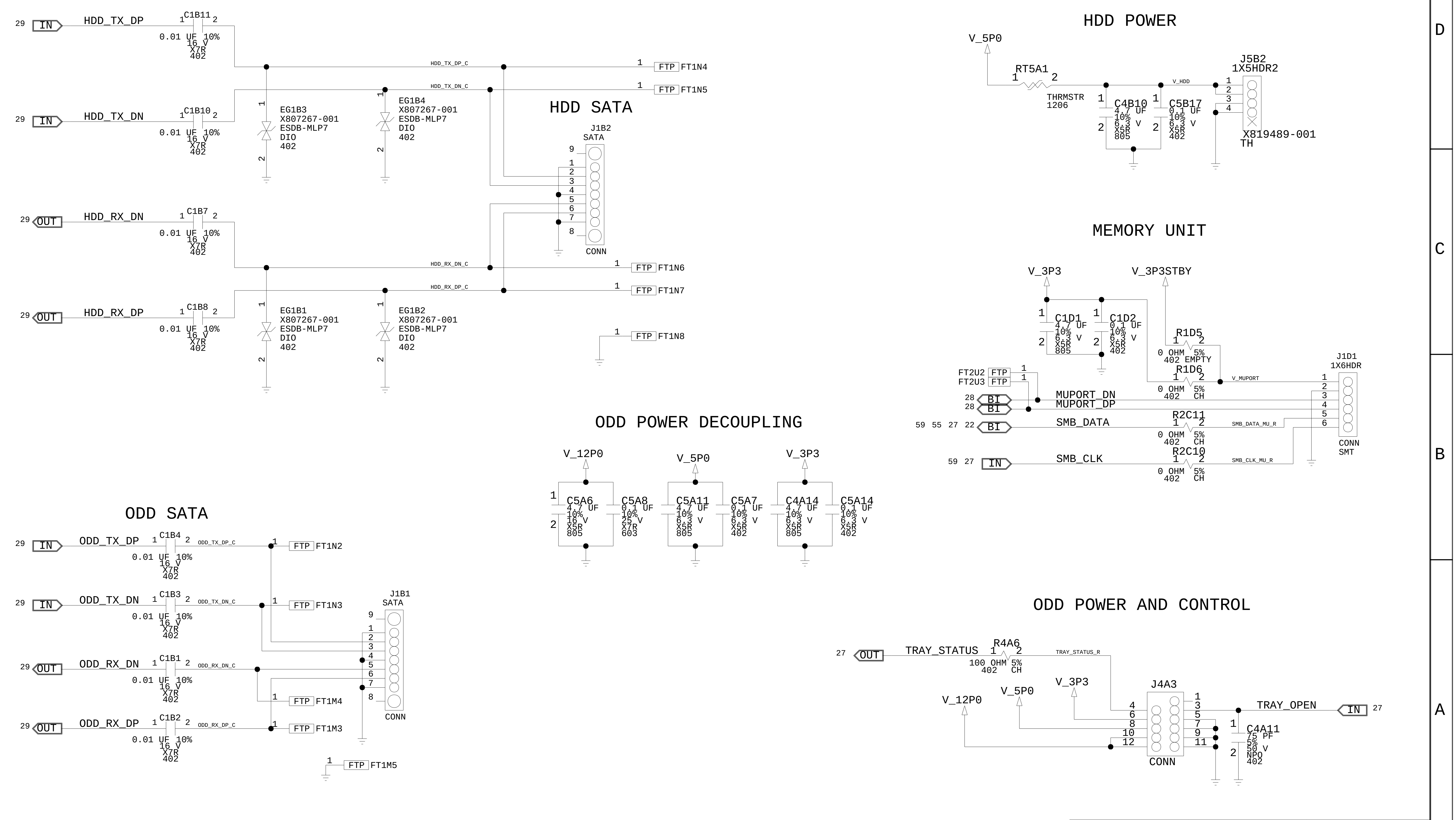
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 40/81	FAB G	REV 1.01

CONN, ODD + HDD + MU


HDD SATA
HDD POWER
MEMORY UNIT
ODD POWER DECOUPLING
ODD SATA
ODD POWER AND CONTROL
29 IN HDD_TX_DP
29 IN HDD_TX_DN
29 OUT HDD_RX_DN
29 OUT HDD_RX_DP
C1B11 C1B10 C1B7 C1B8 0.01 UF 10% 16 V X7R 402
HDD_TX_DP_C
HDD_TX_DN_C
HDD_RX_DN_C
HDD_RX_DP_C
FTP FT1N4
FTP FT1N5
FTP FT1N6
FTP FT1N7
FTP FT1N8
EG1B3 X807267-001 ESDB-MLP7 DIO 402
EG1B4 X807267-001 ESDB-MLP7 DIO 402
EG1B1 X807267-001 ESDB-MLP7 DIO 402
EG1B2 X807267-001 ESDB-MLP7 DIO 402
J1B2 SATA CONN
V_5P0
RT5A1 THRMSTR 1206
V_HDD
C4B10 4.7 UF 10% 6.3 V X5R 805
C5B17 0.1 UF 10% 6.3 V X5R 402
J5B2 1X5HDR2 X819489-001 TH
V_3P3
V_3P3STBY
C1D1 4.7 UF 10% 6.3 V X5R 805
C1D2 0.1 UF 10% 6.3 V X5R 402
R1D5 0 OHM 5% 402 EMPTY
R1D6 0 OHM 5% 402 CH
V_MUPORT
J1D1 1X6HDR CONN SMT
FT2U2 FTP
FT2U3 FTP
28 BI MUPORT_DN
28 BI MUPORT_DP
59 55 27 22 BI SMB_DATA
R2C11 0 OHM 5% 402 CH
SMB_DATA_MU_R
59 27 IN SMB_CLK
R2C10 0 OHM 5% 402 CH
SMB_CLK_MU_R
V_12P0
C5A6 4.7 UF 10% 16 V X5R 805
C5A8 0.1 UF 10% 25 V X7R 603
V_5P0
C5A11 4.7 UF 10% 6.3 V X5R 805
C5A7 0.1 UF 10% 6.3 V X5R 402
V_3P3
C4A14 4.7 UF 10% 6.3 V X5R 805
C5A14 0.1 UF 10% 6.3 V X5R 402
29 IN ODD_TX_DP
29 IN ODD_TX_DN
29 OUT ODD_RX_DN
29 OUT ODD_RX_DP
C1B4 C1B3 C1B1 C1B2 0.01 UF 10% 16 V X7R 402
ODD_TX_DP_C
ODD_TX_DN_C
ODD_RX_DN_C
ODD_RX_DP_C
FTP FT1N2
FTP FT1N3
FTP FT1M4
FTP FT1M3
FTP FT1M5
J1B1 SATA CONN
27 OUT TRAY_STATUS
R4A6 100 OHM 5% 402 CH
TRAY_STATUS_R
V_12P0 V_5P0 V_3P3
J4A3 CONN
TRAY_OPEN IN 27
C4A11 75 PF 5% 50 V NPO 402

[PAGE_TITLE=CONN, ODD + HDD + MU]

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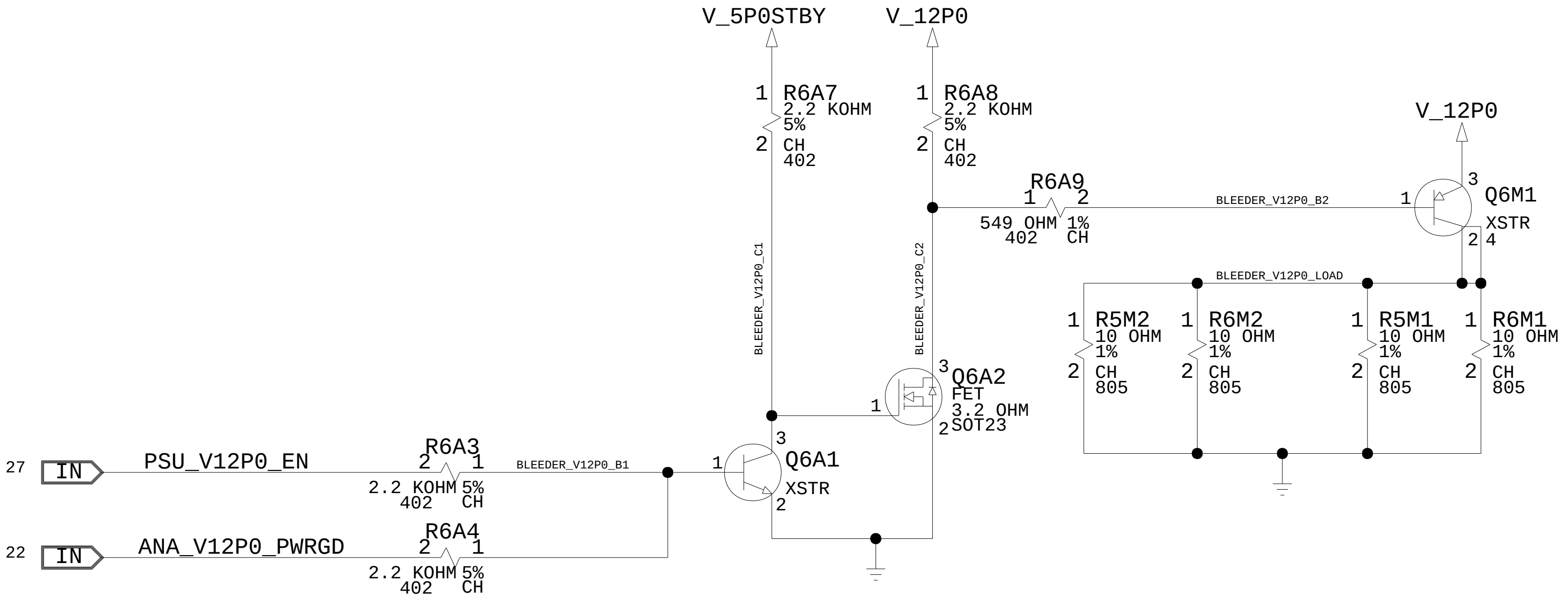
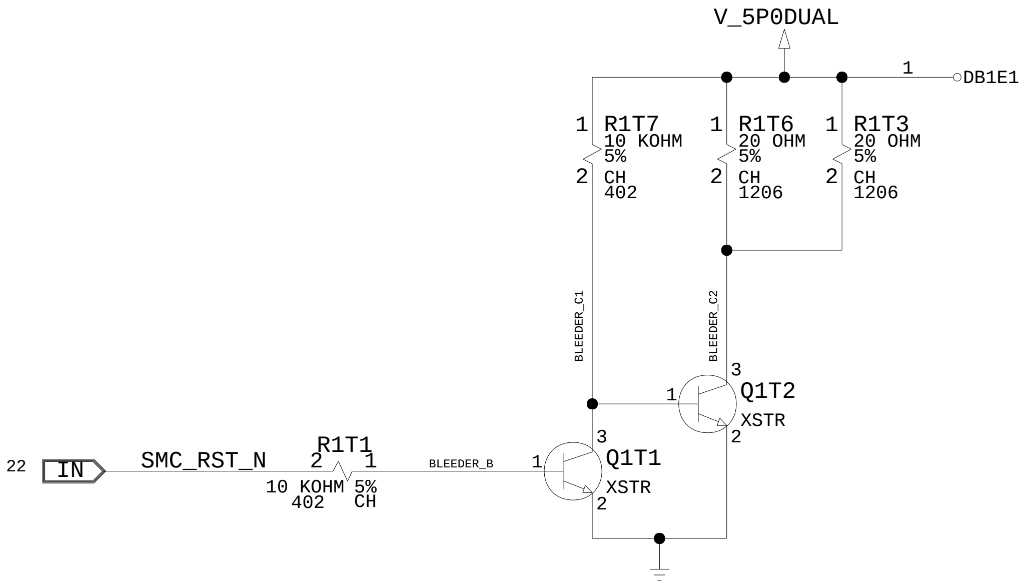
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 41/81	FAB G	REV 1.01

VREG, BLEEDERS


V_5P0STBY
V_12P0
1 R6A7 2.2 KOHM 5% 2 CH 402
1 R6A8 2.2 KOHM 5% 2 CH 402
R6A9 1 2 549 OHM 1% 402 CH
BLEEDER_V12P0_B2
V_12P0
3 Q6M1 1 XSTR 2 4
BLEEDER_V12P0_LOAD
1 R5M2 10 OHM 1% 2 CH 805
1 R6M2 10 OHM 1% 2 CH 805
1 R5M1 10 OHM 1% 2 CH 805
1 R6M1 10 OHM 1% 2 CH 805
BLEEDER_V12P0_C1
BLEEDER_V12P0_C2
3 Q6A2 1 FET 3.2 OHM 2 SOT23
27 IN PSU_V12P0_EN
R6A3 2 1 2.2 KOHM 5% 402 CH
BLEEDER_V12P0_B1
1 3 Q6A1 XSTR 2
22 IN ANA_V12P0_PWRGD
R6A4 2 1 2.2 KOHM 5% 402 CH

V_12P0 & V_5P0 BLEEDERS


V_5P0DUAL
1 DB1E1
1 R1T7 10 KOHM 5% 2 CH 402
1 R1T6 20 OHM 5% 2 CH 1206
1 R1T3 20 OHM 5% 2 CH 1206
BLEEDER_C1
BLEEDER_C2
3 1 Q1T2 XSTR 2
22 IN SMC_RST_N
R1T1 2 1 10 KOHM 5% 402 CH
BLEEDER_B
1 3 Q1T1 XSTR 2

V_5P0DUAL BLEEDER

[PAGE_TITLE= VREGS,_BLEEDERS]

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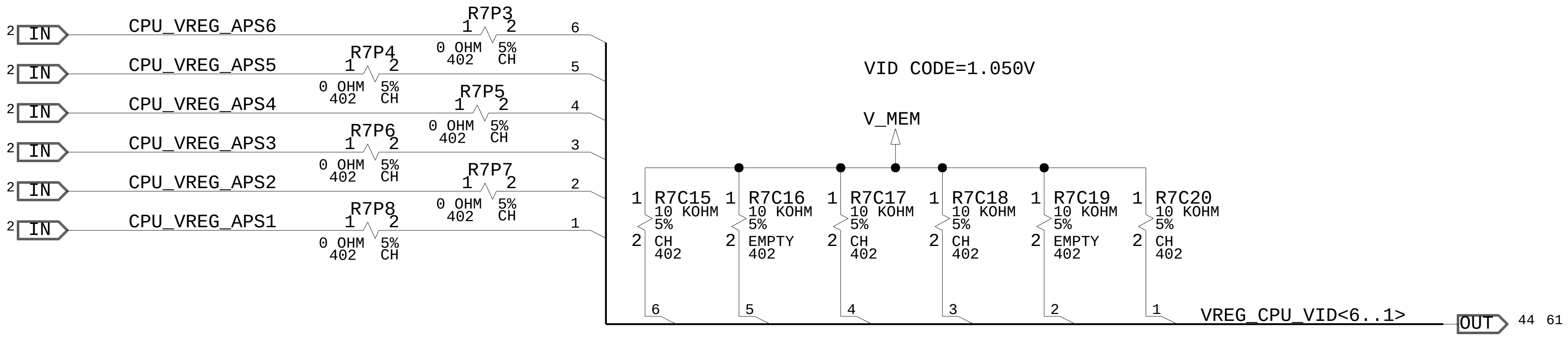
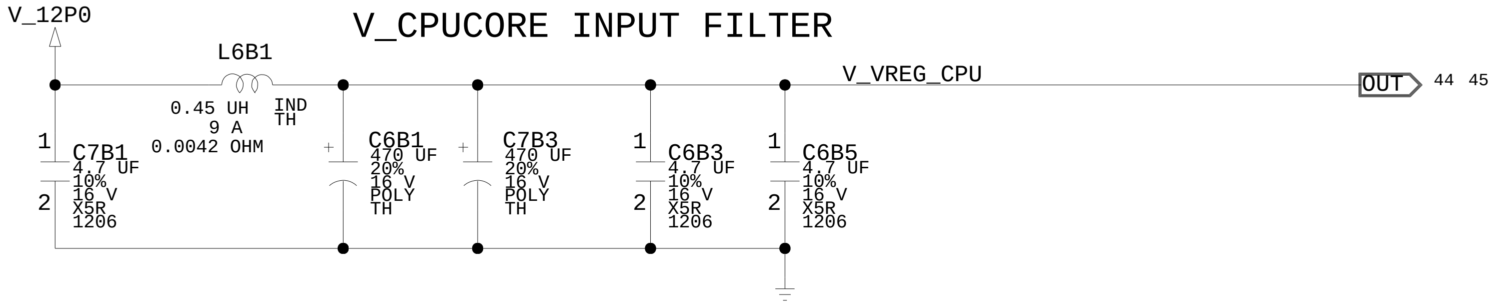
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	42/81	G	1.01

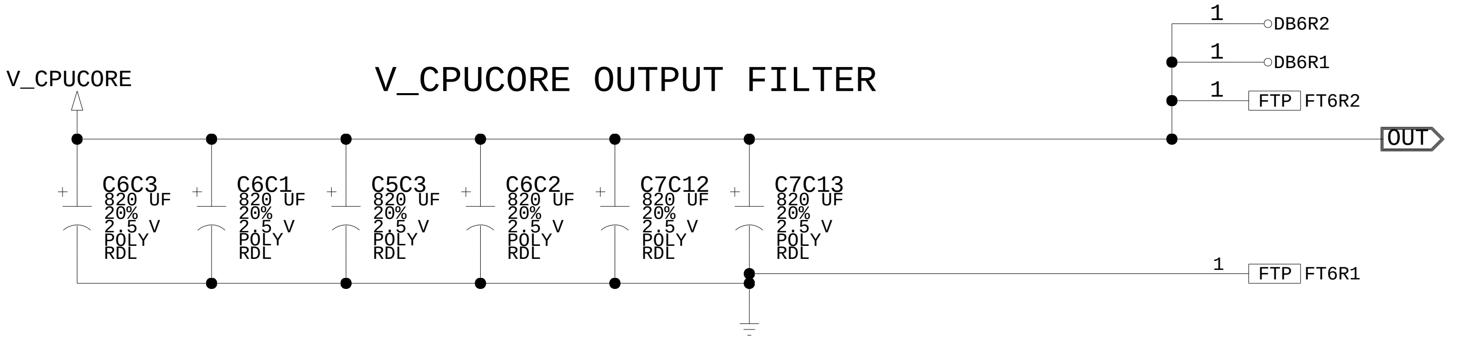
VREGS, INPUT + OUTPUT FILTERS


VID CODE=1.050V
V_MEM
2 IN CPU_VREG_APS6
2 IN CPU_VREG_APS5
2 IN CPU_VREG_APS4
2 IN CPU_VREG_APS3
2 IN CPU_VREG_APS2
2 IN CPU_VREG_APS1
R7P3 1 2 0 OHM 5% 402 CH
R7P4 1 2 0 OHM 5% 402 CH
R7P5 1 2 0 OHM 5% 402 CH
R7P6 1 2 0 OHM 5% 402 CH
R7P7 1 2 0 OHM 5% 402 CH
R7P8 1 2 0 OHM 5% 402 CH
6
5
4
3
2
1
R7C15 10 KOHM 5% CH 402
R7C16 10 KOHM 5% EMPTY 402
R7C17 10 KOHM 5% CH 402
R7C18 10 KOHM 5% CH 402
R7C19 10 KOHM 5% EMPTY 402
R7C20 10 KOHM 5% CH 402
VREG_CPU_VID<6..1>
OUT 44 61

V_CPUCORE INPUT FILTER


V_12P0
L6B1
0.45 UH 9 A 0.0042 OHM
IND TH
V_VREG_CPU
OUT 44 45
C7B1 4.7 UF 10% 16 V X5R 1206
C6B1 470 UF 20% 16 V POLY TH
C7B3 470 UF 20% 16 V POLY TH
C6B3 4.7 UF 10% 16 V X5R 1206
C6B5 4.7 UF 10% 16 V X5R 1206

V_CPUCORE OUTPUT FILTER


V_CPUCORE
1 DB6R2
1 DB6R1
1 FTP FT6R2
OUT
C6C3 820 UF 20% 2.5 V POLY RDL
C6C1 820 UF 20% 2.5 V POLY RDL
C5C3 820 UF 20% 2.5 V POLY RDL
C6C2 820 UF 20% 2.5 V POLY RDL
C7C12 820 UF 20% 2.5 V POLY RDL
C7C13 820 UF 20% 2.5 V POLY RDL
1 FTP FT6R1

[PAGE_TITLE=VREGS, INPUT + OUTPUT FILTERS]

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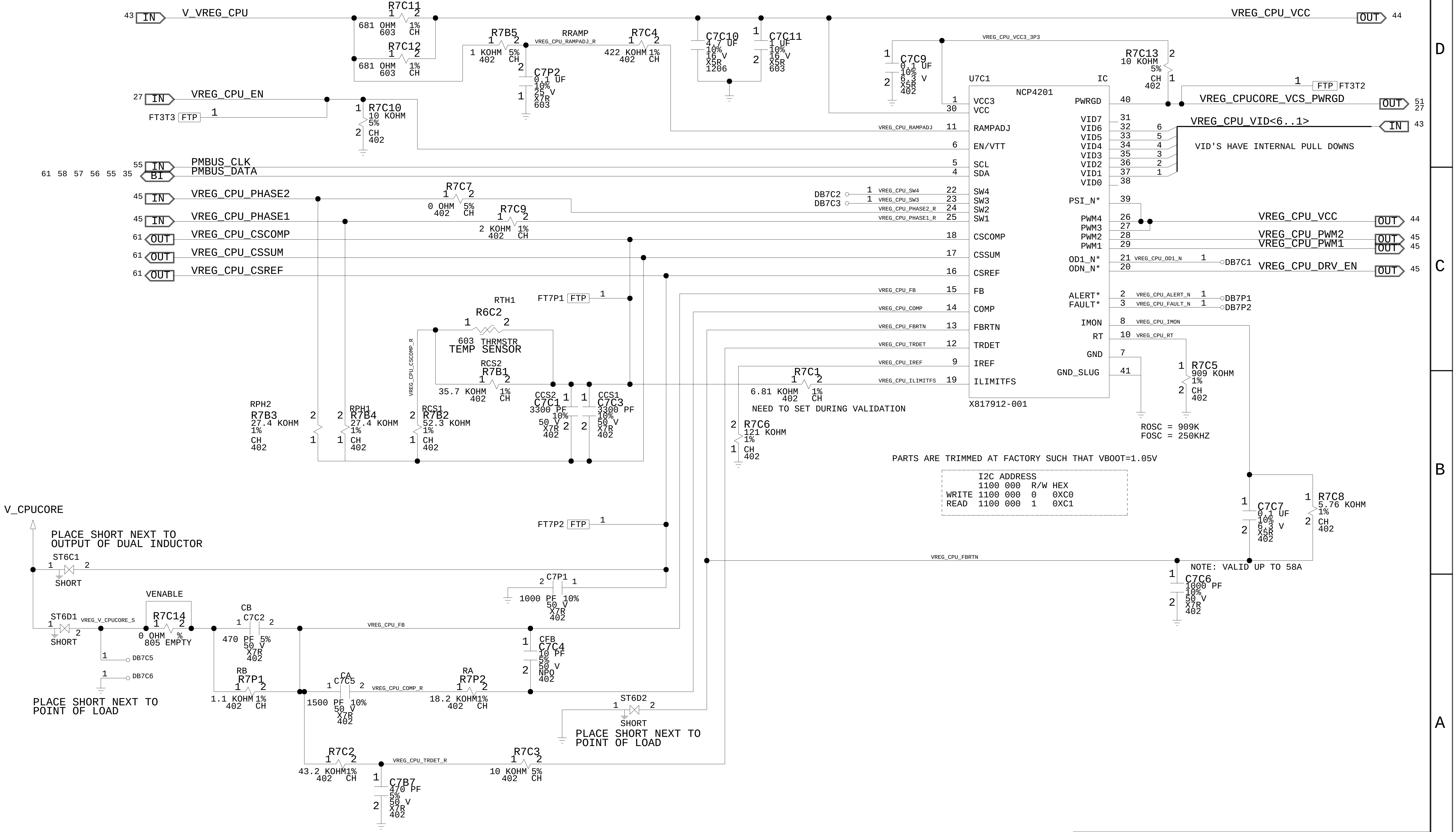
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	43/81	G	1.01

VREGS, CPU CONTROLLER



43 IN V_VREG_CPU
R7C11 1 2 681 OHM 1% 603 CH
R7C12 1 2 681 OHM 1% 603 CH
R7B5 1 2 1 KOHM 5% 402 CH
RRAMP VREG_CPU_RAMPADJ_R
R7C4 1 2 422 KOHM 1% 402 CH
C7P2 2 0.1 UF 10% 25 V X7R 603 1
C7C10 4.7 UF 10% 16 V X5R 1206
C7C11 1 1 UF 10% 16 V X5R 603 2
C7C9 1 0.1 UF 10% 6.3 V X5R 402 2
VREG_CPU_VCC3_3P3
R7C13 2 10 KOHM 5% CH 402 1
VREG_CPU_VCC OUT 44
1 FTP FT3T2
27 IN VREG_CPU_EN
FT3T3 FTP 1
R7C10 1 10 KOHM 5% 2 CH 402
U7C1 NCP4201 IC
1 VCC3
30 VCC
VREG_CPU_RAMPADJ 11 RAMPADJ
6 EN/VTT
5 SCL
4 SDA
22 SW4
23 SW3
24 SW2
25 SW1
18 CSCOMP
17 CSSUM
16 CSREF
VREG_CPU_FB 15 FB
VREG_CPU_COMP 14 COMP
VREG_CPU_FBRTN 13 FBRTN
VREG_CPU_TRDET 12 TRDET
VREG_CPU_IREF 9 IREF
VREG_CPU_ILIMITFS 19 ILIMITFS
X817912-001
PWRGD 40
VREG_CPUCORE_VCS_PWRGD OUT 51 27
VID7 31
VID6 32 6
VID5 33 5
VID4 34 4
VID3 35 3
VID2 36 2
VID1 37 1
VID0 38
VREG_CPU_VID<6..1> IN 43
VID'S HAVE INTERNAL PULL DOWNS
PSI_N* 39
PWM4 26
PWM3 27
PWM2 28
PWM1 29
VREG_CPU_VCC OUT 44
VREG_CPU_PWM2 OUT 45
VREG_CPU_PWM1 OUT 45
OD1_N* 21 VREG_CPU_OD1_N 1 DB7C1
ODN_N* 20
VREG_CPU_DRV_EN OUT 45
ALERT* 2 VREG_CPU_ALERT_N 1 DB7P1
FAULT* 3 VREG_CPU_FAULT_N 1 DB7P2
IMON 8 VREG_CPU_IMON
RT 10 VREG_CPU_RT
GND 7
GND_SLUG 41
R7C5 1 909 KOHM 1% 2 CH 402
ROSC = 909K
FOSC = 250KHZ
55 IN PMBUS_CLK
61 58 57 56 55 35 BI PMBUS_DATA
45 IN VREG_CPU_PHASE2
45 IN VREG_CPU_PHASE1
61 OUT VREG_CPU_CSCOMP
61 OUT VREG_CPU_CSSUM
61 OUT VREG_CPU_CSREF
R7C7 1 2 0 OHM 5% 402 CH
R7C9 1 2 2 KOHM 1% 402 CH
DB7C2 1 VREG_CPU_SW4
DB7C3 1 VREG_CPU_SW3
VREG_CPU_PHASE2_R
VREG_CPU_PHASE1_R
FT7P1 FTP 1
RTH1 R6C2 1 2 603 THRMSTR TEMP SENSOR
RCS2 R7B1 1 2 35.7 KOHM 1% 402 CH
VREG_CPU_CSCOMP_R
CCS2 C7C1 1 3300 PF 10% 50 V 2 X7R 402
CCS1 C7C3 1 3300 PF 10% 50 V 2 X7R 402
R7C1 1 2 6.81 KOHM 1% 402 CH
NEED TO SET DURING VALIDATION
RPH2 R7B3 2 27.4 KOHM 1% 1 CH 402
RPH1 R7B4 2 27.4 KOHM 1% 1 CH 402
RCS1 R7B2 2 52.3 KOHM 1% 1 CH 402
R7C6 2 121 KOHM 1% 1 CH 402
PARTS ARE TRIMMED AT FACTORY SUCH THAT VBOOT=1.05V
I2C ADDRESS
1100 000 R/W HEX
WRITE 1100 000 0 0XC0
READ 1100 000 1 0XC1
C7C7 1 0.1 UF 10% 6.3 V 2 X5R 402
R7C8 1 5.76 KOHM 1% 2 CH 402
VREG_CPU_FBRTN
NOTE: VALID UP TO 58A
C7C6 1 1000 PF 10% 50 V 2 X7R 402
V_CPUCORE
PLACE SHORT NEXT TO OUTPUT OF DUAL INDUCTOR
ST6C1 1 2 SHORT
FT7P2 FTP 1
C7P1 2 1 1000 PF 10% 50 V X7R 402
ST6D1 1 2 SHORT VREG_V_CPUCORE_S
VENABLE R7C14 1 2 0 OHM % 805 EMPTY
1 DB7C5
1 DB7C6
PLACE SHORT NEXT TO POINT OF LOAD
CB C7C2 1 2 470 PF 5% 50 V X7R 402
VREG_CPU_FB
CFB C7C4 1 10 PF 5% 50 V 2 NPO 402
RB R7P1 1 2 1.1 KOHM 1% 402 CH
CA C7C5 1 2 1500 PF 10% 50 V X7R 402
VREG_CPU_COMP_R
RA R7P2 1 2 18.2 KOHM 1% 402 CH
ST6D2 1 2 SHORT
PLACE SHORT NEXT TO POINT OF LOAD
R7C2 1 2 43.2 KOHM 1% 402 CH
VREG_CPU_TRDET_R
R7C3 1 2 10 KOHM 5% 402 CH
C7B7 1 470 PF 5% 50 V 2 X7R 402

[PAGE_TITLE=VREGS, CPU CONTROLLER]

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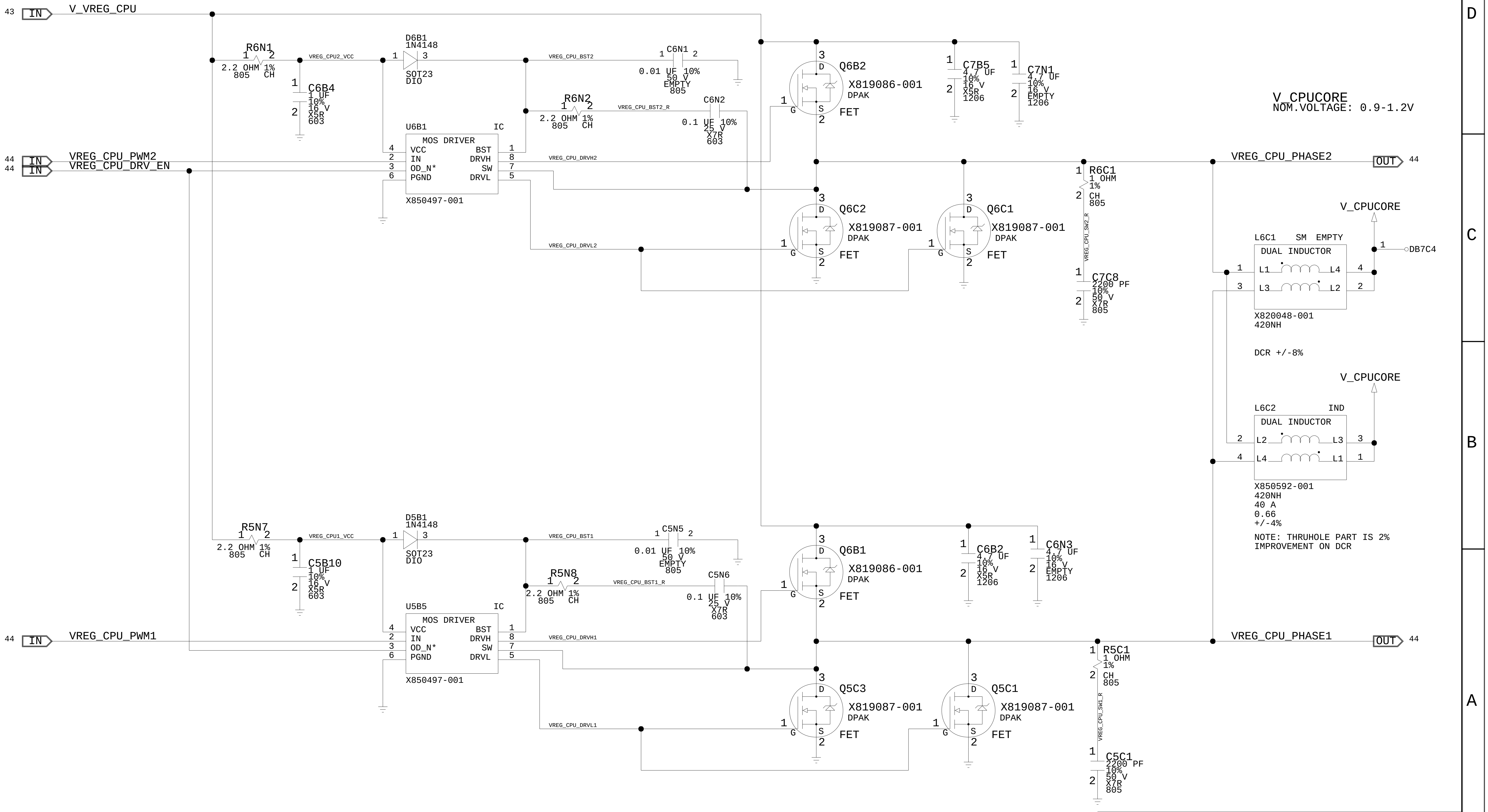
MICROSOFT CONFIDENTIAL

PROJECT NAME	PAGE	FAB	REV
TRINITY_XDK	44/81	G	1.01

VREG, CPU OUTPUT PHASE 1 & 2


43 IN V_VREG_CPU
R6N1 1 2 2.2 OHM 1% 805 CH
VREG_CPU2_VCC
C6B4 1 UF 10% 16 V X5R 603
D6B1 1N4148 SOT23 DIO
VREG_CPU_BST2
C6N1 0.01 UF 10% 50 V EMPTY 805
R6N2 2.2 OHM 1% 805 CH
VREG_CPU_BST2_R
C6N2 0.1 UF 10% 25 V X7R 603
U6B1 IC MOS DRIVER
VCC BST IN DRVH OD_N* SW PGND DRVL
X850497-001
44 IN VREG_CPU_PWM2
44 IN VREG_CPU_DRV_EN
VREG_CPU_DRVH2
VREG_CPU_DRVL2
Q6B2 X819086-001 DPAK FET
C7B5 4.7 UF 10% 16 V X5R 1206
C7N1 4.7 UF 10% 16 V EMPTY 1206
V_CPUCORE
NOM.VOLTAGE: 0.9-1.2V
Q6C2 X819087-001 DPAK FET
Q6C1 X819087-001 DPAK FET
R6C1 1 OHM 1% CH 805
VREG_CPU_SW2_R
C7C8 2200 PF 10% 50 V X7R 805
VREG_CPU_PHASE2 OUT 44
V_CPUCORE
L6C1 SM EMPTY
DUAL INDUCTOR
L1 L4 L3 L2
X820048-001
420NH
1 DB7C4
DCR +/-8%
V_CPUCORE
L6C2 IND
DUAL INDUCTOR
L2 L3 L4 L1
X850592-001
420NH
40 A
0.66
+/-4%
NOTE: THRUHOLE PART IS 2%
IMPROVEMENT ON DCR
R5N7 2.2 OHM 1% 805 CH
VREG_CPU1_VCC
C5B10 1 UF 10% 16 V X5R 603
D5B1 1N4148 SOT23 DIO
VREG_CPU_BST1
C5N5 0.01 UF 10% 50 V EMPTY 805
R5N8 2.2 OHM 1% 805 CH
VREG_CPU_BST1_R
C5N6 0.1 UF 10% 25 V X7R 603
U5B5 IC MOS DRIVER
VCC BST IN DRVH OD_N* SW PGND DRVL
X850497-001
44 IN VREG_CPU_PWM1
VREG_CPU_DRVH1
VREG_CPU_DRVL1
Q6B1 X819086-001 DPAK FET
C6B2 4.7 UF 10% 16 V X5R 1206
C6N3 4.7 UF 10% 16 V EMPTY 1206
Q5C3 X819087-001 DPAK FET
Q5C1 X819087-001 DPAK FET
R5C1 1 OHM 1% CH 805
VREG_CPU_SW1_R
C5C1 2200 PF 10% 50 V X7R 805
VREG_CPU_PHASE1 OUT 44

[PAGE_TITLE=VREGS, CPU OUTPUT PHASE 1,2]

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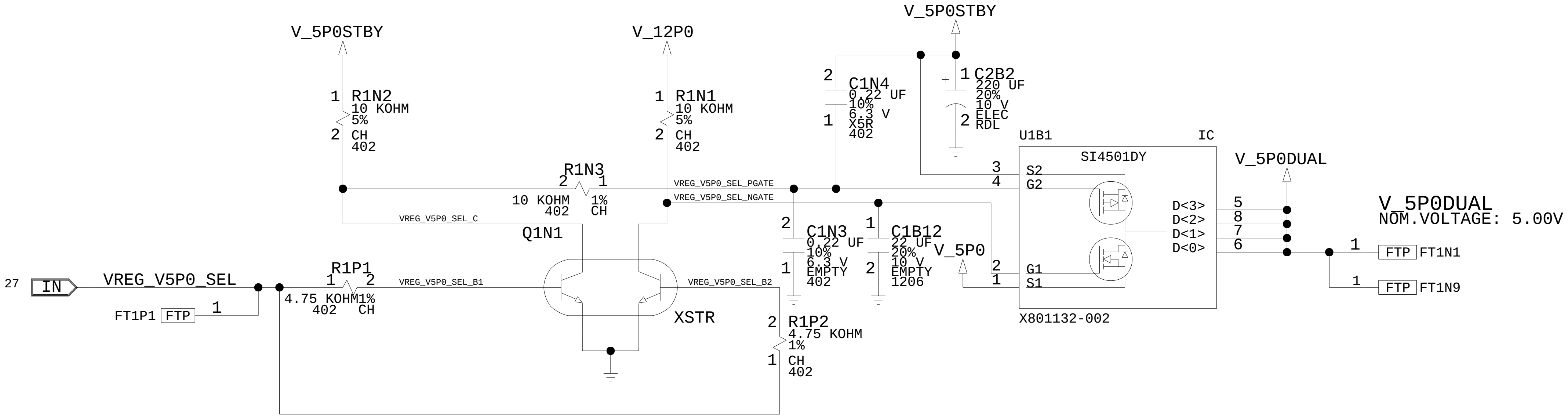
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	45/81	G	1.01

VREGS, V5P0 DUAL


V_5P0STBY
V_12P0
V_5P0STBY
R1N2
10 KOHM
5%
CH
402
R1N1
10 KOHM
5%
CH
402
R1N3
10 KOHM 1%
402 CH
VREG_V5P0_SEL_PGATE
VREG_V5P0_SEL_NGATE
VREG_V5P0_SEL_C
Q1N1
XSTR
VREG_V5P0_SEL_B1
VREG_V5P0_SEL_B2
27 IN VREG_V5P0_SEL
FT1P1 FTP
R1P1
4.75 KOHM 1%
402 CH
R1P2
4.75 KOHM
1%
CH
402
C1N4
0.22 UF
10%
6.3 V
X5R
402
C2B2
220 UF
20%
10 V
ELEC
RDL
C1N3
0.22 UF
10%
6.3 V
EMPTY
402
C1B12
22 UF
20%
10 V
EMPTY
1206
V_5P0
U1B1
SI4501DY
IC
S2
G2
G1
S1
D<3>
D<2>
D<1>
D<0>
X801132-002
V_5P0DUAL
V_5P0DUAL
NOM.VOLTAGE: 5.00V
FTP FT1N1
FTP FT1N9

VREG_5P0_SEL	VREG_5P0_SEL NGATE/PGATE	V_5P0DUAL
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0

[PAGE_TITLE=VREGS, V5P0 DUAL]

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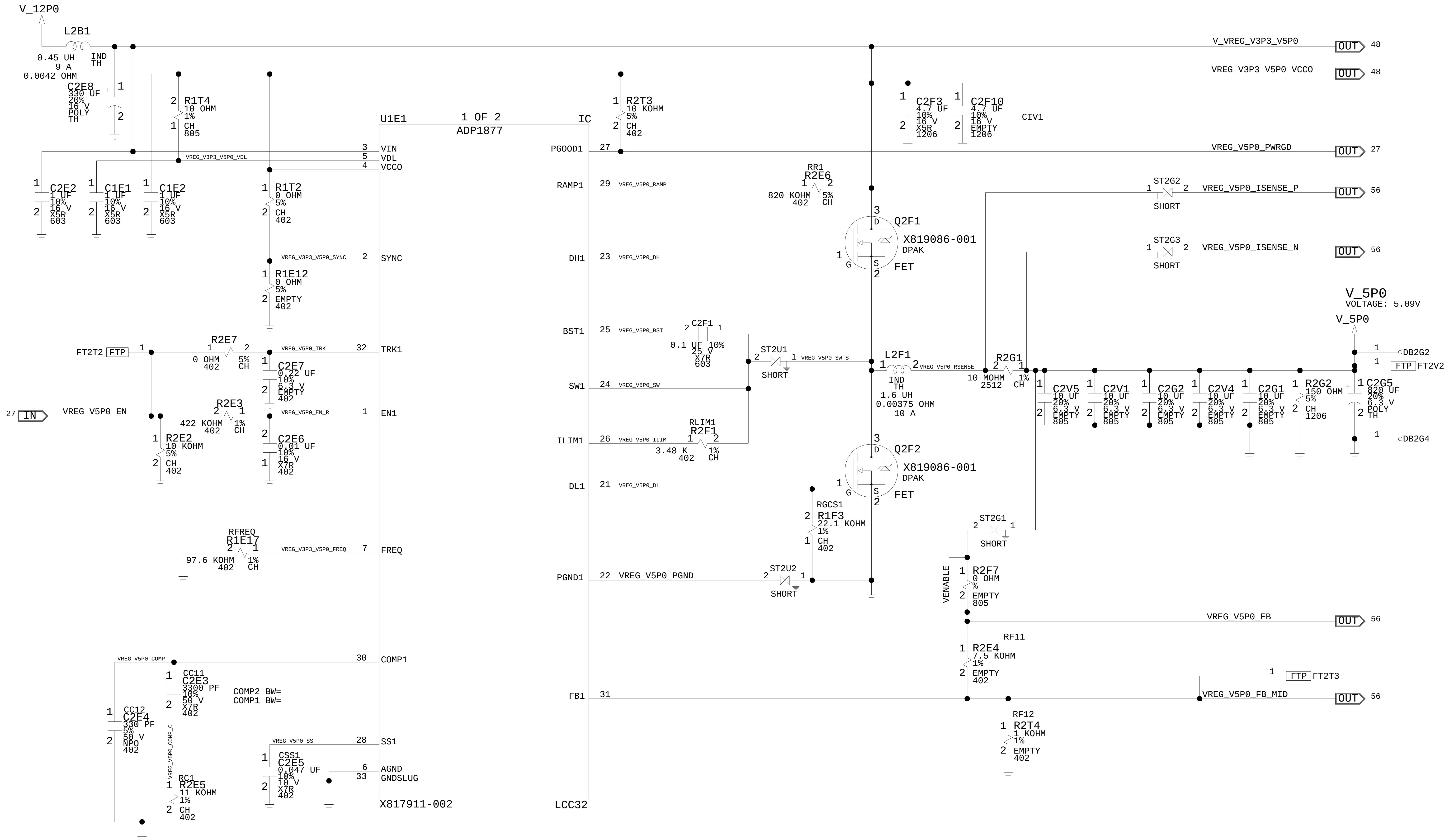
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 46/81	FAB G	REV 1.01

VREGS, V5P0


V_12P0
L2B1
0.45 UH IND TH
9 A
0.0042 OHM
C2E8 330 UF 20% 16 V POLY TH
R1T4 10 OHM 1% CH 805
R2T3 10 KOHM 5% CH 402
V_VREG_V3P3_V5P0
VREG_V3P3_V5P0_VCCO
C2F3 4.7 UF 10% 16 V X5R 1206
C2F10 4.7 UF 10% 16 V EMPTY 1206
CIV1
U1E1
1 OF 2
ADP1877
IC
VIN
VDL
VCCO
VREG_V3P3_V5P0_VDL
PGOOD1
VREG_V5P0_PWRGD
C2E2 1 UF 10% 16 V X5R 603
C1E1 1 UF 10% 16 V X5R 603
C1E2 1 UF 10% 16 V X5R 603
R1T2 0 OHM 5% CH 402
RAMP1
VREG_V5P0_RAMP
RR1
R2E6
820 KOHM 402
5% CH
ST2G2 SHORT
VREG_V5P0_ISENSE_P
Q2F1
X819086-001
DPAK
FET
SYNC
VREG_V3P3_V5P0_SYNC
DH1
VREG_V5P0_DH
ST2G3 SHORT
VREG_V5P0_ISENSE_N
R1E12 0 OHM 5% EMPTY 402
V_5P0
VOLTAGE: 5.09V
BST1
VREG_V5P0_BST
C2F1
0.1 UF 10% 25 V X7R 603
ST2U1 SHORT
VREG_V5P0_SW_S
L2F1
IND TH
1.6 UH
0.00375 OHM
10 A
VREG_V5P0_RSENSE
R2G1
10 MOHM 2512
1% CH
DB2G2
FTP FT2V2
FT2T2 FTP
R2E7
0 OHM 402
5% CH
TRK1
VREG_V5P0_TRK
C2E7 0.22 UF 10% 6.3 V EMPTY 402
SW1
VREG_V5P0_SW
C2V5 10 UF 20% 6.3 V EMPTY 805
C2V1 10 UF 20% 6.3 V EMPTY 805
C2G2 10 UF 20% 6.3 V EMPTY 805
C2V4 10 UF 20% 6.3 V EMPTY 805
C2G1 10 UF 20% 6.3 V EMPTY 805
R2G2 150 OHM 5% CH 1206
C2G5 820 UF 20% 6.3 V POLY TH
IN
VREG_V5P0_EN
R2E3
422 KOHM 402
1% CH
EN1
VREG_V5P0_EN_R
R2E2 10 KOHM 5% CH 402
C2E6 0.01 UF 10% 16 V X7R 402
ILIM1
VREG_V5P0_ILIM
RLIM1
R2F1
3.48 K 402
1% CH
Q2F2
X819086-001
DPAK
FET
DB2G4
DL1
VREG_V5P0_DL
RGCS1
R1F3 22.1 KOHM 1% CH 402
ST2G1 SHORT
RFREQ
R1E17
97.6 KOHM 402
1% CH
FREQ
VREG_V3P3_V5P0_FREQ
R2F7 0 OHM % EMPTY 805
VENABLE
PGND1
VREG_V5P0_PGND
ST2U2 SHORT
VREG_V5P0_FB
RF11
R2E4 7.5 KOHM 1% EMPTY 402
COMP1
VREG_V5P0_COMP
CC11
C2E3 3300 PF 10% 50 V X7R 402
COMP2 BW=
COMP1 BW=
FTP FT2T3
FB1
VREG_V5P0_FB_MID
CC12
C2E4 330 PF 5% 50 V NPO 402
VREG_V5P0_COMP_C
RF12
R2T4 1 KOHM 1% EMPTY 402
SS1
VREG_V5P0_SS
CSS1
C2E5 0.047 UF 10% 10 V X7R 402
AGND
GNDSLUG
RC1
R2E5 11 KOHM 1% CH 402
X817911-002
LCC32
OUT 48
OUT 27
OUT 56

[PAGE_TITLE=VREGS, V5P0]

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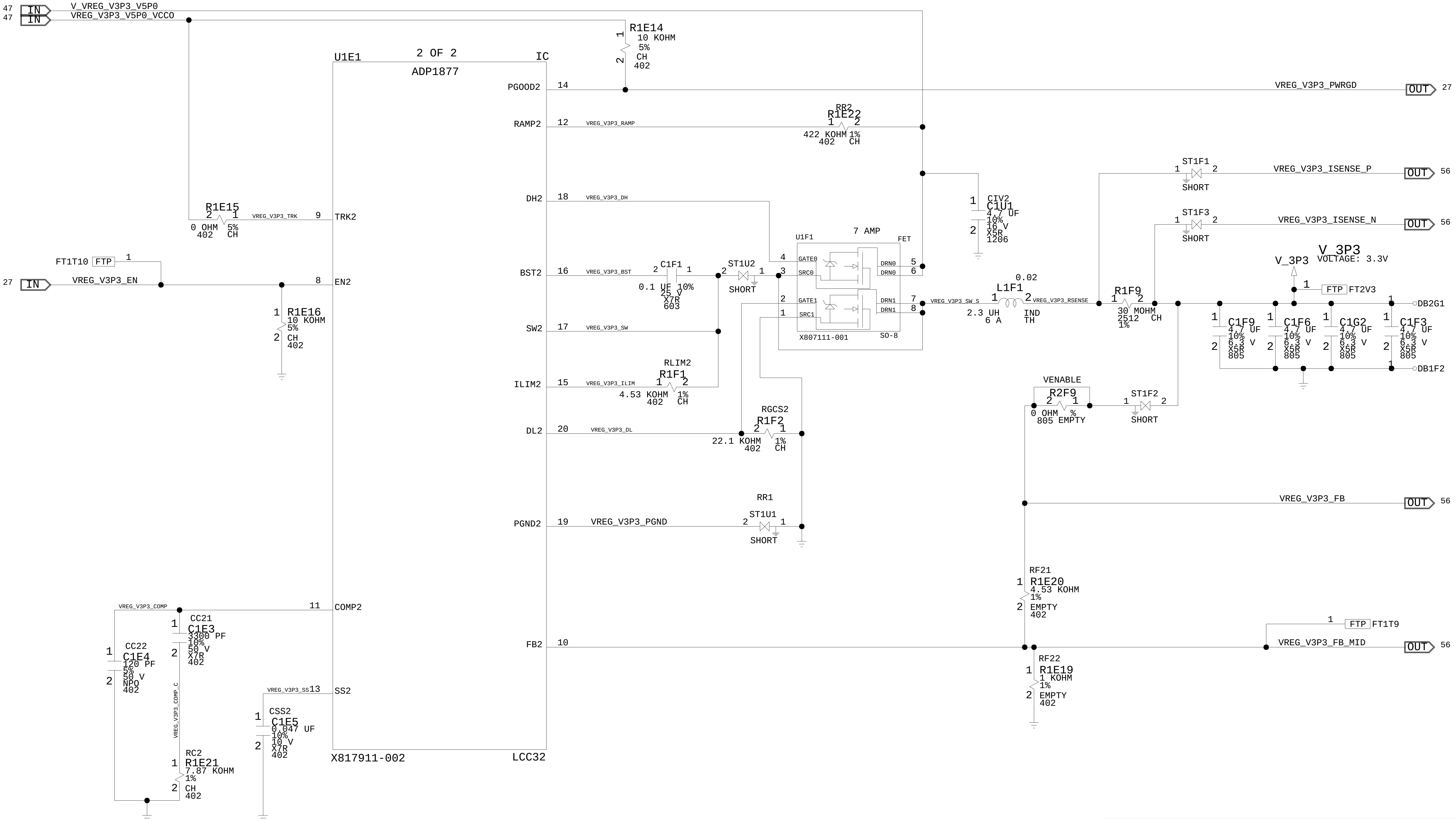
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 47/81	FAB G	REV 1.01

VREGS, V3P3


47 IN V_VREG_V3P3_V5P0
47 IN VREG_V3P3_V5P0_VCCO
R1E14 10 KOHM 5% CH 402
U1E1 2 OF 2 IC
ADP1877
PGOOD2 14
VREG_V3P3_PWRGD OUT 27
RAMP2 12 VREG_V3P3_RAMP
RR2 R1E22 422 KOHM 1% 402 CH
DH2 18 VREG_V3P3_DH
CIV2 C1U1 4.7 UF 10% 16 V X5R 1206
ST1F1 SHORT VREG_V3P3_ISENSE_P OUT 56
ST1F3 SHORT VREG_V3P3_ISENSE_N OUT 56
R1E15 0 OHM 5% 402 CH VREG_V3P3_TRK 9 TRK2
U1F1 7 AMP FET
GATE0 SRC0 DRN0 DRN0 GATE1 SRC1 DRN1 DRN1
X807111-001 SO-8
FT1T10 FTP
27 IN VREG_V3P3_EN 8 EN2
BST2 16 VREG_V3P3_BST
C1F1 0.1 UF 10% 25 V X7R 603
ST1U2 SHORT
R1E16 10 KOHM 5% CH 402
SW2 17 VREG_V3P3_SW
L1F1 0.02 2.3 UH 6 A IND TH
VREG_V3P3_SW_S VREG_V3P3_RSENSE
R1F9 30 MOHM 2512 CH 1%
V_3P3 VOLTAGE: 3.3V
V_3P3
FTP FT2V3
DB2G1
C1F9 4.7 UF 10% 6.3 V X5R 805
C1F6 4.7 UF 10% 6.3 V X5R 805
C1G2 4.7 UF 10% 6.3 V X5R 805
C1F3 4.7 UF 10% 6.3 V X5R 805
DB1F2
ILIM2 15 VREG_V3P3_ILIM
RLIM2 R1F1 4.53 KOHM 1% 402 CH
VENABLE R2F9 0 OHM % 805 EMPTY
ST1F2 SHORT
DL2 20 VREG_V3P3_DL
RGCS2 R1F2 22.1 KOHM 1% 402 CH
VREG_V3P3_FB OUT 56
PGND2 19 VREG_V3P3_PGND
RR1 ST1U1 SHORT
RF21 R1E20 4.53 KOHM 1% EMPTY 402
FTP FT1T9
VREG_V3P3_COMP 11 COMP2
CC21 C1E3 3300 PF 10% 50 V X7R 402
CC22 C1E4 120 PF 5% 50 V NPO 402
FB2 10
VREG_V3P3_FB_MID OUT 56
RF22 R1E19 1 KOHM 1% EMPTY 402
VREG_V3P3_SS 13 SS2
CSS2 C1E5 0.047 UF 10% 10 V X7R 402
VREG_V3P3_COMP_C
RC2 R1E21 7.87 KOHM 1% CH 402
X817911-002 LCC32

[PAGE_TITLE=VREGS, V3P3]

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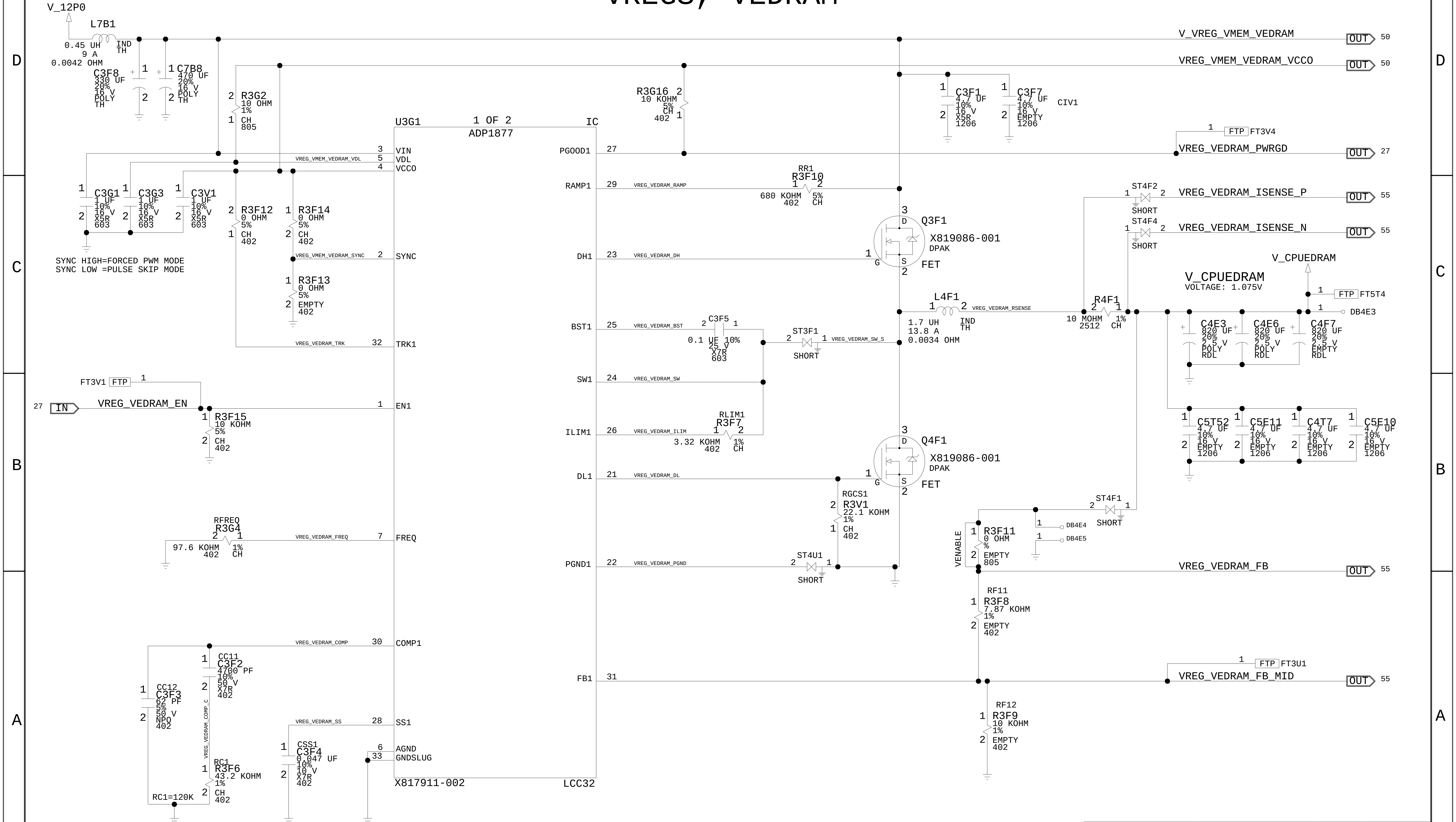
VREGS, VEDRAM


V_12P0
L7B1
0.45 UH IND
9 A TH
0.0042 OHM
C3F8
330 UF
20%
16 V
POLY
TH
C7B8
470 UF
20%
16 V
POLY
TH
R3G2
10 OHM
1%
CH
805
R3G16
10 KOHM
5%
CH
402
U3G1
1 OF 2
ADP1877
IC
VIN
VDL
VCCO
SYNC
TRK1
EN1
FREQ
COMP1
SS1
AGND
GNDSLUG
X817911-002
LCC32
PGOOD1
RAMP1
DH1
BST1
SW1
ILIM1
DL1
PGND1
FB1
VREG_VMEM_VEDRAM_VDL
VREG_VMEM_VEDRAM_SYNC
VREG_VEDRAM_TRK
VREG_VEDRAM_FREQ
VREG_VEDRAM_COMP
VREG_VEDRAM_SS
VREG_VEDRAM_RAMP
VREG_VEDRAM_DH
VREG_VEDRAM_BST
VREG_VEDRAM_SW
VREG_VEDRAM_ILIM
VREG_VEDRAM_DL
VREG_VEDRAM_PGND
VREG_VEDRAM_SW_S
VREG_VEDRAM_RSENSE
C3G1 1 UF 10% 16 V X5R 603
C3G3 1 UF 10% 16 V X5R 603
C3V1 1 UF 10% 16 V X5R 603
R3F12 0 OHM 5% CH 402
R3F14 0 OHM 5% CH 402
R3F13 0 OHM 5% EMPTY 402
SYNC HIGH=FORCED PWM MODE
SYNC LOW =PULSE SKIP MODE
FT3V1 FTP
27 IN VREG_VEDRAM_EN
R3F15 10 KOHM 5% CH 402
RFREQ R3G4 97.6 KOHM 402 1% CH
CC11 C3F2 4700 PF 10% 50 V X7R 402
CC12 C3F3 62 PF 5% 50 V NPO 402
VREG_VEDRAM_COMP_C
RC1 R3F6 43.2 KOHM 1% CH 402
RC1=120K
CSS1 C3F4 0.047 UF 10% 10 V X7R 402
V_VREG_VMEM_VEDRAM OUT 50
VREG_VMEM_VEDRAM_VCCO OUT 50
C3F1 4.7 UF 10% 16 V X5R 1206
C3F7 4.7 UF 10% 16 V EMPTY 1206
CIV1
FTP FT3V4
VREG_VEDRAM_PWRGD OUT 27
RR1 R3F10 680 KOHM 402 5% CH
Q3F1 X819086-001 DPAK FET
Q4F1 X819086-001 DPAK FET
D G S
C3F5 0.1 UF 10% 25 V X7R 603
ST3F1 SHORT
RLIM1 R3F7 3.32 KOHM 402 1% CH
RGCS1 R3V1 22.1 KOHM 1% CH 402
ST4U1 SHORT
L4F1 1.7 UH IND 13.8 A TH 0.0034 OHM
R4F1 10 MOHM 2512 1% CH
ST4F2 SHORT
VREG_VEDRAM_ISENSE_P OUT 55
ST4F4 SHORT
VREG_VEDRAM_ISENSE_N OUT 55
V_CPUEDRAM
V_CPUEDRAM
VOLTAGE: 1.075V
FTP FT5T4
DB4E3
C4E3 820 UF 20% 2.5 V POLY RDL
C4E6 820 UF 20% 2.5 V POLY RDL
C4F7 820 UF 20% 2.5 V EMPTY RDL
C5T52 4.7 UF 10% 16 V EMPTY 1206
C5E11 4.7 UF 10% 16 V EMPTY 1206
C4T7 4.7 UF 10% 16 V EMPTY 1206
C5E10 4.7 UF 10% 16 V EMPTY 1206
ST4F1 SHORT
DB4E4
DB4E5
VENABLE
R3F11 0 OHM % EMPTY 805
VREG_VEDRAM_FB OUT 55
RF11 R3F8 7.87 KOHM 1% EMPTY 402
FTP FT3U1
VREG_VEDRAM_FB_MID OUT 55
RF12 R3F9 10 KOHM 1% EMPTY 402

[PAGE_TITLE=[VREGS, VEDRAM]

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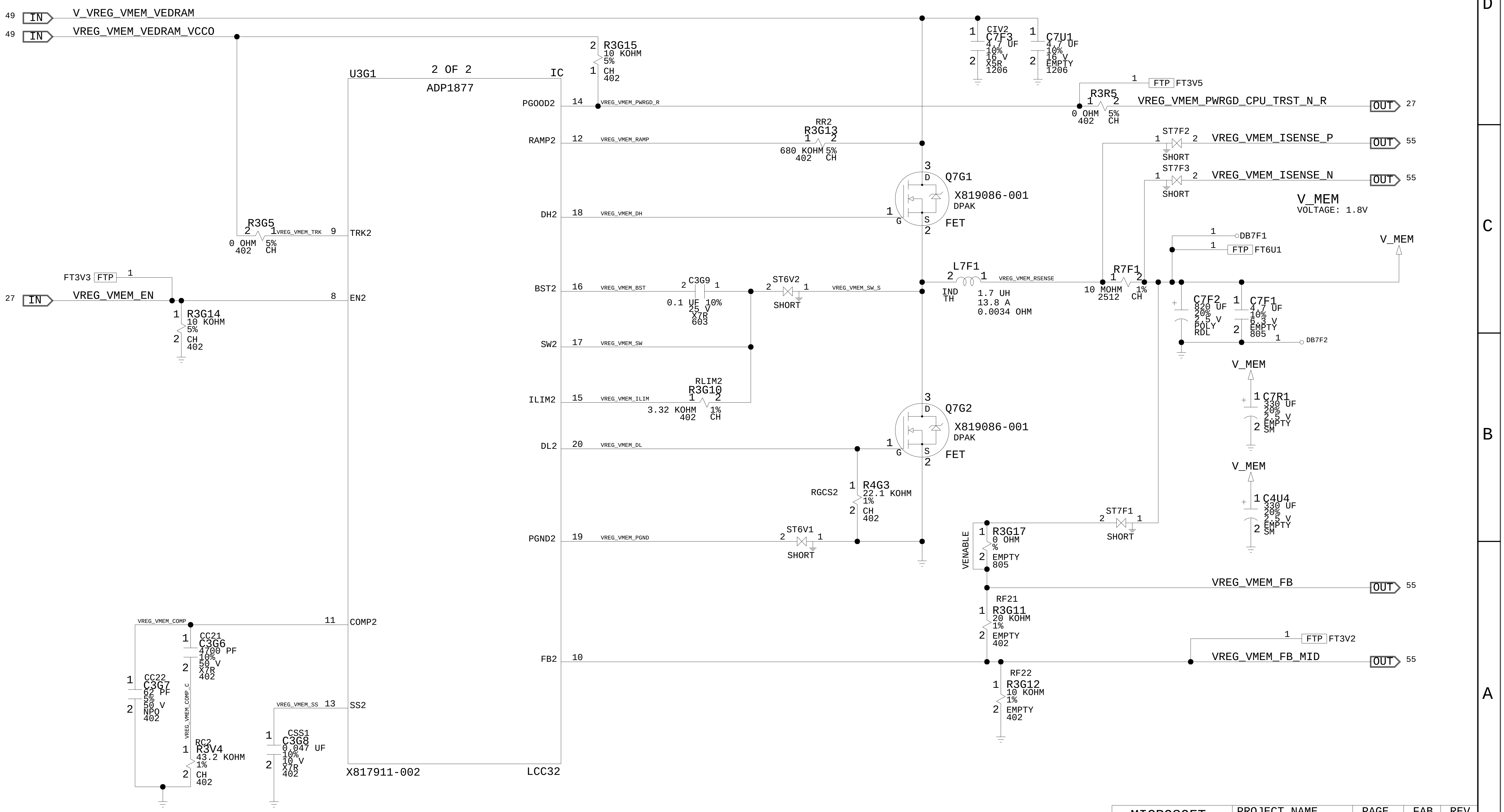
PROJECT NAME	PAGE	FAB	REV
TRINITY_XDK	49/81	G	1.01

VREGS, VMEM


49 IN V_VREG_VMEM_VEDRAM
49 IN VREG_VMEM_VEDRAM_VCCO
27 IN VREG_VMEM_EN
FT3V3 FTP 1
R3G14 10 KOHM 5% CH 402
R3G5 0 OHM 5% 402 CH
VREG_VMEM_TRK
U3G1 2 OF 2 IC ADP1877
X817911-002 LCC32
9 TRK2
8 EN2
11 COMP2
13 SS2
14 PGOOD2
12 RAMP2
18 DH2
16 BST2
17 SW2
15 ILIM2
20 DL2
19 PGND2
10 FB2
VREG_VMEM_PWRGD_R
VREG_VMEM_RAMP
VREG_VMEM_DH
VREG_VMEM_BST
VREG_VMEM_SW
VREG_VMEM_ILIM
VREG_VMEM_DL
VREG_VMEM_PGND
R3G15 10 KOHM 5% CH 402
RR2 R3G13 680 KOHM 5% 402 CH
C3G9 0.1 UF 10% 25 V X7R 603
ST6V2 SHORT
VREG_VMEM_SW_S
RLIM2 R3G10 3.32 KOHM 1% 402 CH
RGCS2 R4G3 22.1 KOHM 1% CH 402
ST6V1 SHORT
Q7G1 X819086-001 DPAK FET
Q7G2 X819086-001 DPAK FET
D G S
CIV2 C7F3 4.7 UF 10% 16 V X5R 1206
C7U1 4.7 UF 10% 16 V EMPTY 1206
FTP FT3V5
R3R5 0 OHM 5% 402 CH
VREG_VMEM_PWRGD_CPU_TRST_N_R OUT 27
ST7F2 SHORT
VREG_VMEM_ISENSE_P OUT 55
ST7F3 SHORT
VREG_VMEM_ISENSE_N OUT 55
V_MEM VOLTAGE: 1.8V
L7F1 IND TH 1.7 UH 13.8 A 0.0034 OHM
VREG_VMEM_RSENSE
R7F1 10 MOHM 1% 2512 CH
DB7F1
FTP FT6U1
V_MEM
C7F2 820 UF 20% 2.5 V POLY RDL
C7F1 4.7 UF 10% 6.3 V EMPTY 805
DB7F2
V_MEM
C7R1 330 UF 20% 2.5 V EMPTY SM
V_MEM
C4U4 330 UF 20% 2.5 V EMPTY SM
ST7F1 SHORT
VENABLE
R3G17 0 OHM % EMPTY 805
VREG_VMEM_FB OUT 55
RF21 R3G11 20 KOHM 1% EMPTY 402
FTP FT3V2
VREG_VMEM_FB_MID OUT 55
RF22 R3G12 10 KOHM 1% EMPTY 402
VREG_VMEM_COMP
CC21 C3G6 4700 PF 10% 50 V X7R 402
CC22 C3G7 62 PF 5% 50 V NPO 402
VREG_VMEM_COMP_C
RC2 R3V4 43.2 KOHM 1% CH 402
VREG_VMEM_SS
CSS1 C3G8 0.047 UF 10% 10 V X7R 402

[PAGE_TITLE=[VREGS, VMEM]

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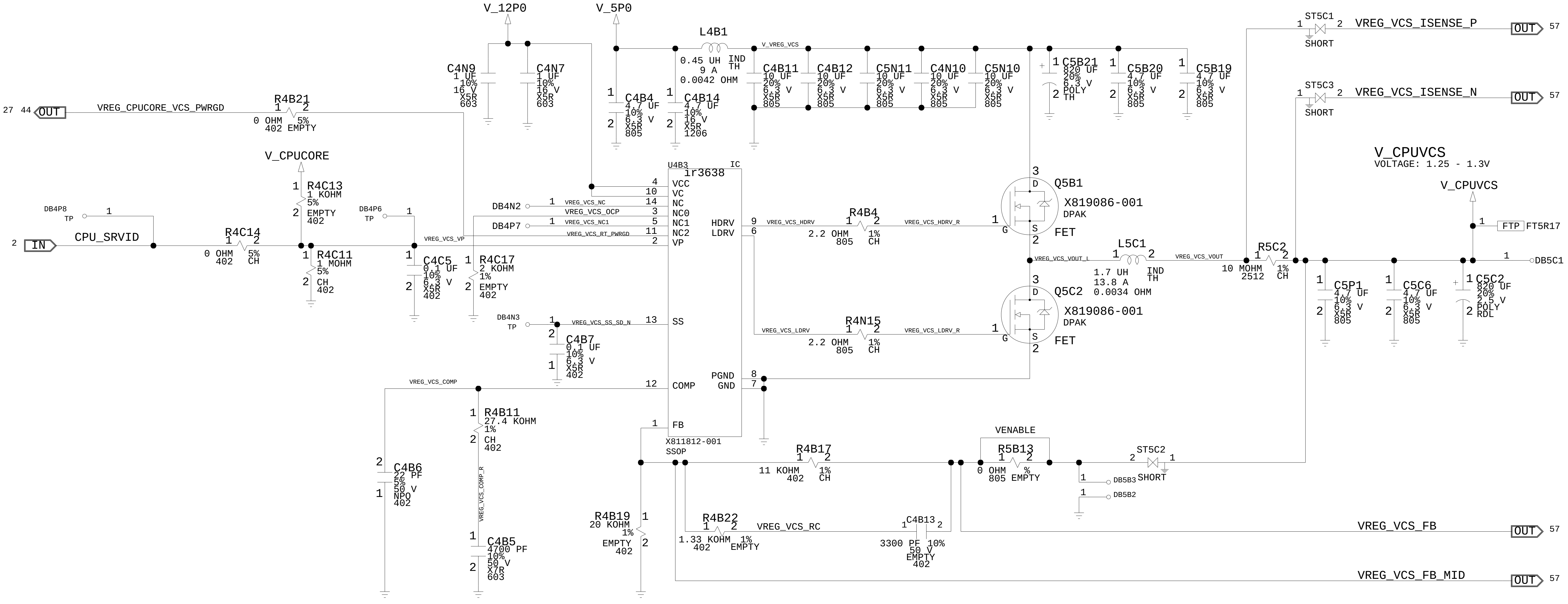
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	50/81	G	1.01

VREGS, VCS


V_12P0
V_5P0
L4B1
0.45 UH IND TH
9 A
0.0042 OHM
V_VREG_VCS
C4N9 1 UF 10% 16 V X5R 603
C4N7 1 UF 10% 16 V X5R 603
C4B4 4.7 UF 10% 6.3 V X5R 805
C4B14 4.7 UF 10% 16 V X5R 1206
C4B11 10 UF 20% 6.3 V X5R 805
C4B12 10 UF 20% 6.3 V X5R 805
C5N11 10 UF 20% 6.3 V X5R 805
C4N10 10 UF 20% 6.3 V X5R 805
C5N10 10 UF 20% 6.3 V X5R 805
C5B21 820 UF 20% 6.3 V POLY TH
C5B20 4.7 UF 10% 6.3 V X5R 805
C5B19 4.7 UF 10% 6.3 V X5R 805
27 44 OUT
VREG_CPUCORE_VCS_PWRGD
R4B21 0 OHM 5% 402 EMPTY
V_CPUCORE
R4C13 1 KOHM 5% EMPTY 402
DB4P8 TP
DB4P6 TP
2 IN CPU_SRVID
R4C14 0 OHM 5% 402 CH
R4C11 1 MOHM 5% CH 402
C4C5 0.1 UF 10% 6.3 V X5R 402
R4C17 2 KOHM 1% EMPTY 402
VREG_VCS_VP
DB4N2
DB4P7
VREG_VCS_NC
VREG_VCS_OCP
VREG_VCS_NC1
VREG_VCS_RT_PWRGD
U4B3 IC ir3638
4 VCC
10 VC
14 NC
3 NC0
5 NC1
11 NC2
2 VP
9 HDRV
6 LDRV
13 SS
12 COMP
1 FB
8 PGND
7 GND
X811812-001 SSOP
DB4N3 TP
VREG_VCS_SS_SD_N
C4B7 0.1 UF 10% 6.3 V X5R 402
VREG_VCS_COMP
R4B11 27.4 KOHM 1% CH 402
VREG_VCS_COMP_R
C4B6 22 PF 5% 50 V NPO 402
C4B5 4700 PF 10% 50 V X7R 603
VREG_VCS_HDRV
R4B4 2.2 OHM 805 1% CH
VREG_VCS_HDRV_R
VREG_VCS_LDRV
R4N15 2.2 OHM 805 1% CH
VREG_VCS_LDRV_R
Q5B1 X819086-001 DPAK FET
Q5C2 X819086-001 DPAK FET
D G S
VREG_VCS_VOUT_L
L5C1 1.7 UH IND TH
13.8 A
0.0034 OHM
VREG_VCS_VOUT
R5C2 10 MOHM 2512 1% CH
ST5C1 SHORT
VREG_VCS_ISENSE_P OUT 57
ST5C3 SHORT
VREG_VCS_ISENSE_N OUT 57
V_CPUVCS
VOLTAGE: 1.25 - 1.3V
V_CPUVCS
FTP FT5R17
DB5C1
C5P1 4.7 UF 10% 6.3 V X5R 805
C5C6 4.7 UF 10% 6.3 V X5R 805
C5C2 820 UF 20% 2.5 V POLY RDL
R4B17 11 KOHM 402 1% CH
VENABLE
R5B13 0 OHM % 805 EMPTY
ST5C2 SHORT
DB5B3
DB5B2
R4B19 20 KOHM 1% EMPTY 402
R4B22 1.33 KOHM 402 1% EMPTY
VREG_VCS_RC
C4B13 3300 PF 10% 50 V EMPTY 402
VREG_VCS_FB OUT 57
VREG_VCS_FB_MID OUT 57

GAIN=0.4 WITH R4B17 = 11K, R4B19 = 27.4K
OUTPUT = CPU_SRVID(1+GAIN)

[PAGE_TITLE=VREGS, VCS]

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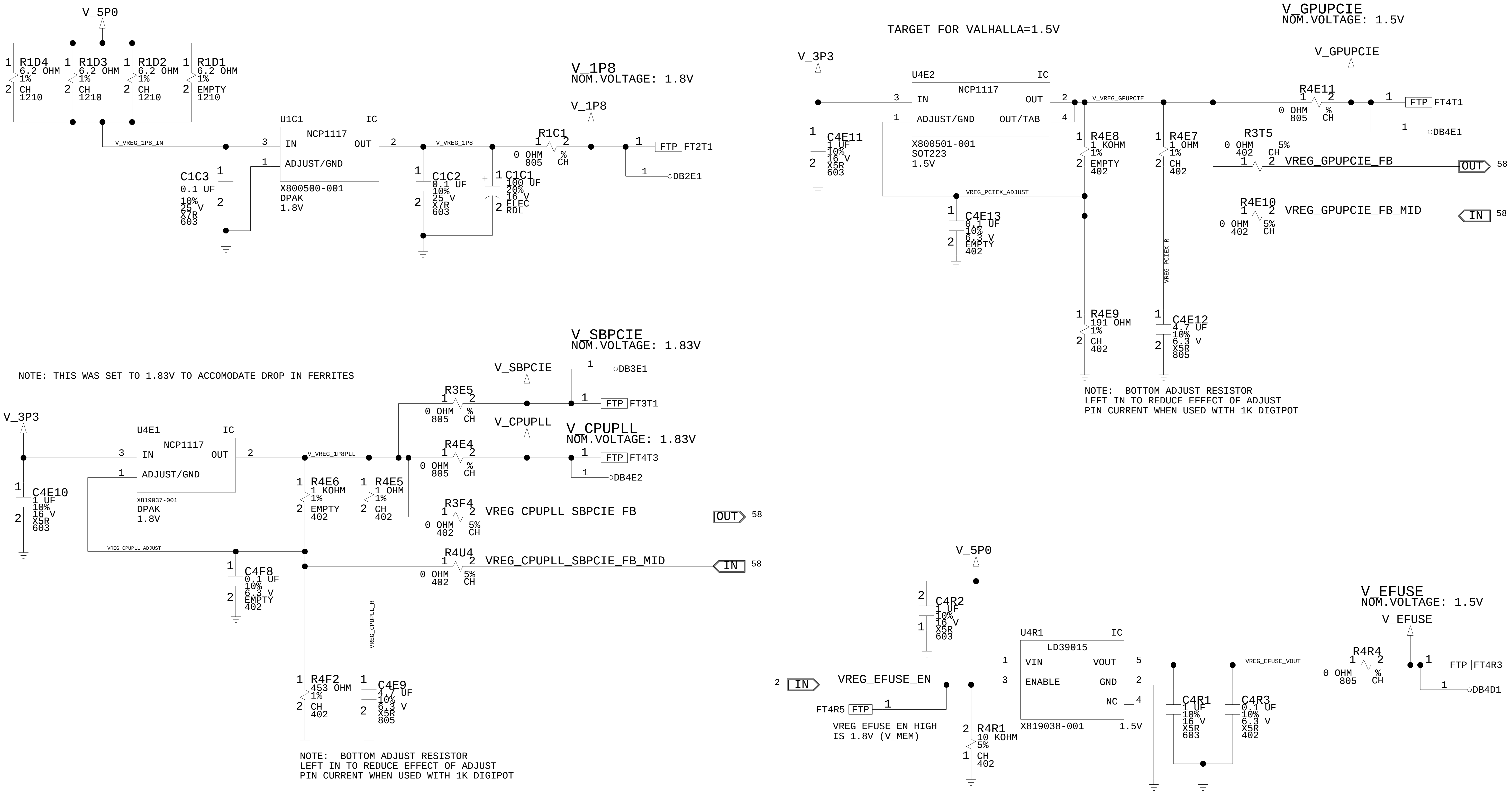
VREGS, 1P8+GPUPCIE+SBPCIE+CPUPLL+EFUSE


V_5P0
R1D4 6.2 OHM 1% CH 1210
R1D3 6.2 OHM 1% CH 1210
R1D2 6.2 OHM 1% CH 1210
R1D1 6.2 OHM 1% EMPTY 1210
V_VREG_1P8_IN
C1C3 0.1 UF 10% 25 V X7R 603
U1C1 IC
NCP1117
IN
OUT
ADJUST/GND
X800500-001
DPAK
1.8V
V_VREG_1P8
C1C2 0.1 UF 10% 25 V X7R 603
C1C1 100 UF 20% 16 V ELEC RDL
R1C1 0 OHM 805 % CH
V_1P8
NOM.VOLTAGE: 1.8V
V_1P8
FTP FT2T1
DB2E1
TARGET FOR VALHALLA=1.5V
V_3P3
C4E11 1 UF 10% 16 V X5R 603
U4E2 IC
NCP1117
IN
OUT
ADJUST/GND
OUT/TAB
X800501-001
SOT223
1.5V
V_VREG_GPUPCIE
VREG_PCIEX_ADJUST
C4E13 0.1 UF 10% 6.3 V EMPTY 402
R4E8 1 KOHM 1% EMPTY 402
R4E7 1 OHM 1% CH 402
VREG_PCIEX_R
R4E9 191 OHM 1% CH 402
C4E12 4.7 UF 10% 6.3 V X5R 805
V_GPUPCIE
NOM.VOLTAGE: 1.5V
V_GPUPCIE
R4E11 0 OHM 805 % CH
FTP FT4T1
DB4E1
R3T5 0 OHM 402 5% CH
VREG_GPUPCIE_FB
OUT 58
R4E10 0 OHM 402 5% CH
VREG_GPUPCIE_FB_MID
IN 58
NOTE: BOTTOM ADJUST RESISTOR
LEFT IN TO REDUCE EFFECT OF ADJUST
PIN CURRENT WHEN USED WITH 1K DIGIPOT
V_SBPCIE
NOM.VOLTAGE: 1.83V
NOTE: THIS WAS SET TO 1.83V TO ACCOMODATE DROP IN FERRITES
V_3P3
C4E10 1 UF 10% 16 V X5R 603
U4E1 IC
NCP1117
IN
OUT
ADJUST/GND
X819037-001
DPAK
1.8V
V_VREG_1P8PLL
VREG_CPUPLL_ADJUST
C4F8 0.1 UF 10% 6.3 V EMPTY 402
R4E6 1 KOHM 1% EMPTY 402
R4E5 1 OHM 1% CH 402
VREG_CPUPLL_R
R4F2 453 OHM 1% CH 402
C4E9 4.7 UF 10% 6.3 V X5R 805
R3E5 0 OHM 805 % CH
V_SBPCIE
DB3E1
FTP FT3T1
V_CPUPLL
V_CPUPLL
NOM.VOLTAGE: 1.83V
R4E4 0 OHM 805 % CH
FTP FT4T3
DB4E2
R3F4 0 OHM 402 5% CH
VREG_CPUPLL_SBPCIE_FB
OUT 58
R4U4 0 OHM 402 5% CH
VREG_CPUPLL_SBPCIE_FB_MID
IN 58
NOTE: BOTTOM ADJUST RESISTOR
LEFT IN TO REDUCE EFFECT OF ADJUST
PIN CURRENT WHEN USED WITH 1K DIGIPOT
V_5P0
C4R2 1 UF 10% 16 V X5R 603
2 IN
VREG_EFUSE_EN
FT4R5 FTP
VREG_EFUSE_EN HIGH
IS 1.8V (V_MEM)
R4R1 10 KOHM 5% CH 402
U4R1 IC
LD39015
VIN
ENABLE
VOUT
GND
NC
X819038-001
1.5V
C4R1 1 UF 10% 16 V X5R 603
C4R3 0.1 UF 10% 6.3 V X5R 402
VREG_EFUSE_VOUT
V_EFUSE
NOM.VOLTAGE: 1.5V
V_EFUSE
R4R4 0 OHM 805 % CH
FTP FT4R3
DB4D1

[PAGE_TITLE=VREGS, 1P8+GPUPCIE+SBPCIE+CPUPLL+EFUSE]

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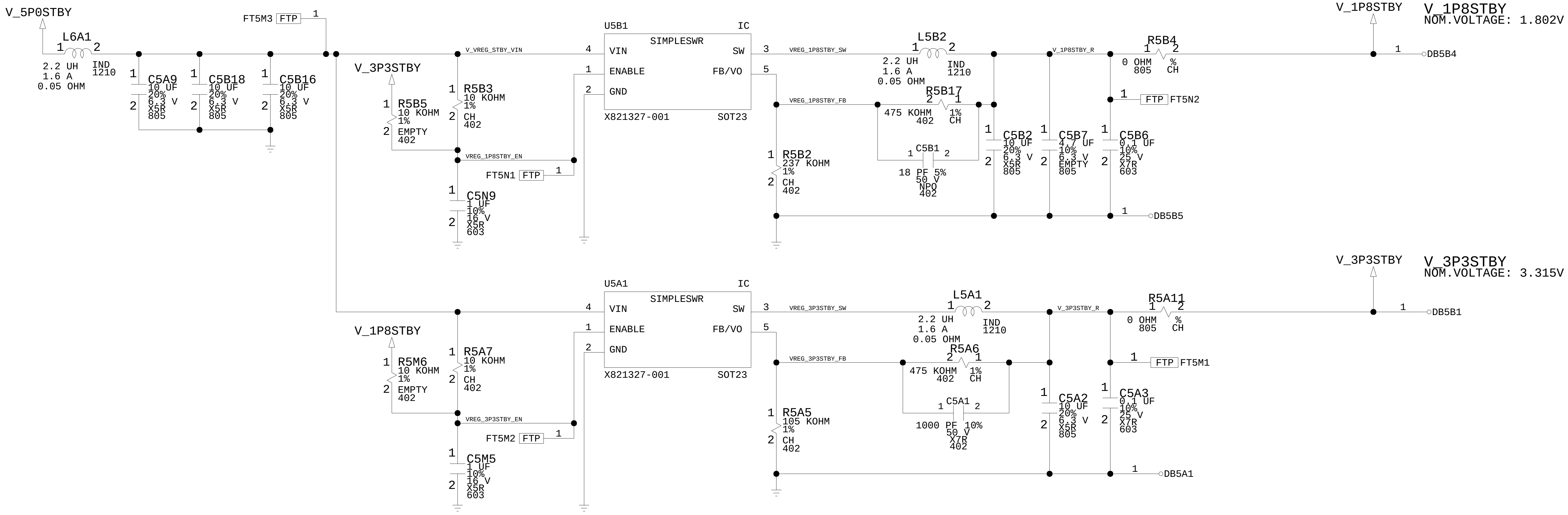
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 52/81	FAB G	REV 1.01

VREGS, STANDBY SWITCHERS


V_5P0STBY
L6A1
1 2
2.2 UH
1.6 A
0.05 OHM
IND
1210
C5A9
10 UF
20%
6.3 V
X5R
805
C5B18
10 UF
20%
6.3 V
X5R
805
C5B16
10 UF
20%
6.3 V
X5R
805
FT5M3 FTP 1
V_3P3STBY
R5B5
10 KOHM
1%
EMPTY
402
V_VREG_STBY_VIN
R5B3
10 KOHM
1%
CH
402
VREG_1P8STBY_EN
FT5N1 FTP 1
C5N9
1 UF
10%
16 V
X5R
603
U5B1
IC
SIMPLESWR
VIN
ENABLE
GND
SW
FB/VO
X821327-001
SOT23
VREG_1P8STBY_SW
VREG_1P8STBY_FB
L5B2
2.2 UH
1.6 A
0.05 OHM
IND
1210
R5B17
475 KOHM
402
1%
CH
C5B1
18 PF 5%
50 V
NPO
402
R5B2
237 KOHM
1%
CH
402
C5B2
10 UF
20%
6.3 V
X5R
805
C5B7
4.7 UF
10%
6.3 V
EMPTY
805
C5B6
0.1 UF
10%
25 V
X7R
603
V_1P8STBY_R
R5B4
0 OHM
805
%
CH
FTP FT5N2
DB5B5
V_1P8STBY
V_1P8STBY
NOM.VOLTAGE: 1.802V
DB5B4
V_1P8STBY
R5M6
10 KOHM
1%
EMPTY
402
R5A7
10 KOHM
1%
CH
402
VREG_3P3STBY_EN
FT5M2 FTP 1
C5M5
1 UF
10%
16 V
X5R
603
U5A1
IC
SIMPLESWR
VIN
ENABLE
GND
SW
FB/VO
X821327-001
SOT23
VREG_3P3STBY_SW
VREG_3P3STBY_FB
L5A1
2.2 UH
1.6 A
0.05 OHM
IND
1210
R5A6
475 KOHM
402
1%
CH
C5A1
1000 PF 10%
50 V
X7R
402
R5A5
105 KOHM
1%
CH
402
C5A2
10 UF
20%
6.3 V
X5R
805
C5A3
0.1 UF
10%
25 V
X7R
603
V_3P3STBY_R
R5A11
0 OHM
805
%
CH
FTP FT5M1
DB5A1
V_3P3STBY
V_3P3STBY
NOM.VOLTAGE: 3.315V
DB5B1

[PAGE_TITLE=VREGS, STANDBY SWITCHERS]

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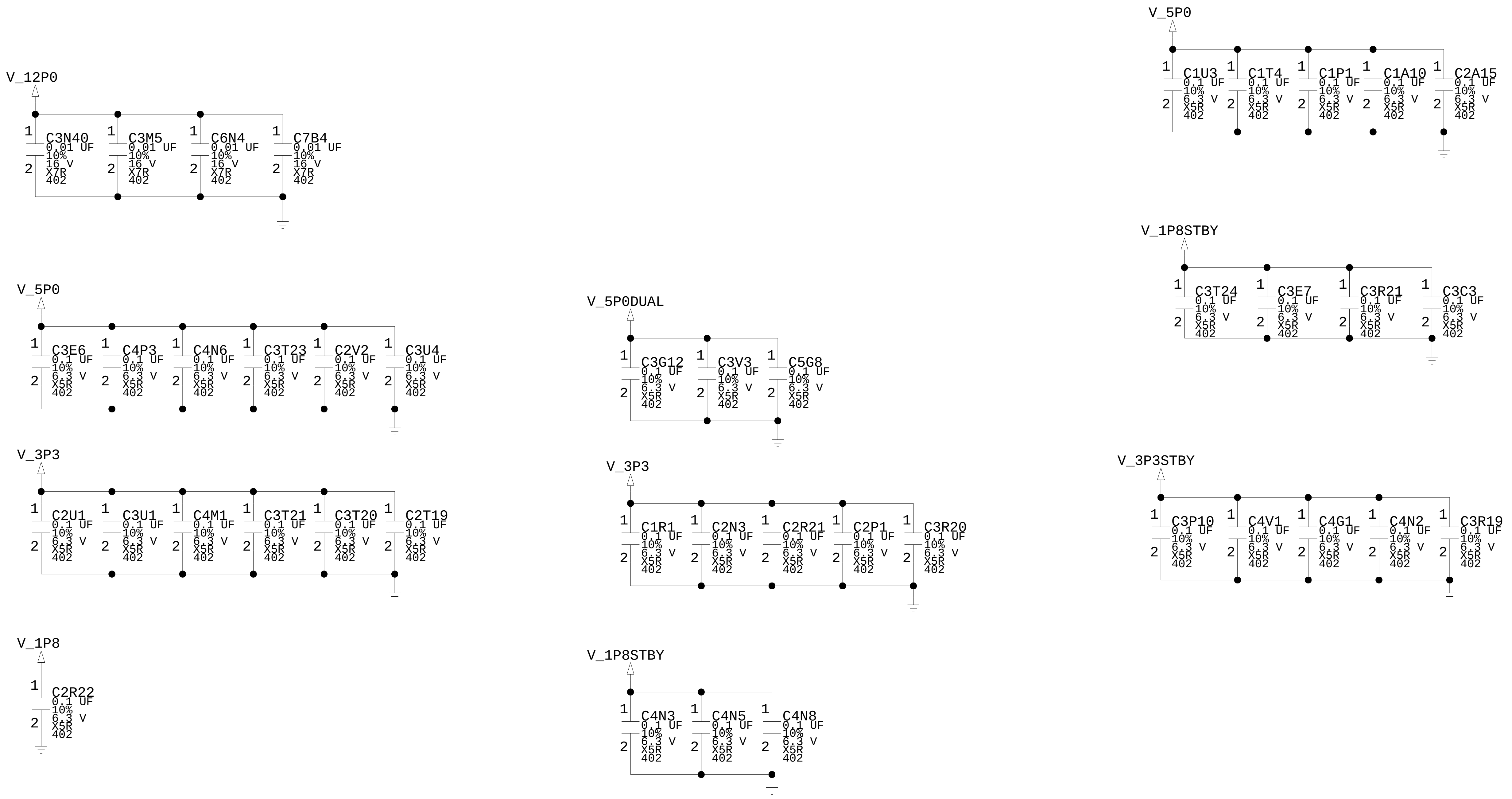
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 53/81	FAB G	REV 1.01

BOARD LEVEL DECOUPLING


V_12P0
C3N40 0.01 UF 10% 16 V X7R 402
C3M5 0.01 UF 10% 16 V X7R 402
C6N4 0.01 UF 10% 16 V X7R 402
C7B4 0.01 UF 10% 16 V X7R 402
V_5P0
C3E6 0.1 UF 10% 6.3 V X5R 402
C4P3 0.1 UF 10% 6.3 V X5R 402
C4N6 0.1 UF 10% 6.3 V X5R 402
C3T23 0.1 UF 10% 6.3 V X5R 402
C2V2 0.1 UF 10% 6.3 V X5R 402
C3U4 0.1 UF 10% 6.3 V X5R 402
V_3P3
C2U1 0.1 UF 10% 6.3 V X5R 402
C3U1 0.1 UF 10% 6.3 V X5R 402
C4M1 0.1 UF 10% 6.3 V X5R 402
C3T21 0.1 UF 10% 6.3 V X5R 402
C3T20 0.1 UF 10% 6.3 V X5R 402
C2T19 0.1 UF 10% 6.3 V X5R 402
V_1P8
C2R22 0.1 UF 10% 6.3 V X5R 402
V_5P0DUAL
C3G12 0.1 UF 10% 6.3 V X5R 402
C3V3 0.1 UF 10% 6.3 V X5R 402
C5G8 0.1 UF 10% 6.3 V X5R 402
V_3P3
C1R1 0.1 UF 10% 6.3 V X5R 402
C2N3 0.1 UF 10% 6.3 V X5R 402
C2R21 0.1 UF 10% 6.3 V X5R 402
C2P1 0.1 UF 10% 6.3 V X5R 402
C3R20 0.1 UF 10% 6.3 V X5R 402
V_1P8STBY
C4N3 0.1 UF 10% 6.3 V X5R 402
C4N5 0.1 UF 10% 6.3 V X5R 402
C4N8 0.1 UF 10% 6.3 V X5R 402
V_5P0
C1U3 0.1 UF 10% 6.3 V X5R 402
C1T4 0.1 UF 10% 6.3 V X5R 402
C1P1 0.1 UF 10% 6.3 V X5R 402
C1A10 0.1 UF 10% 6.3 V X5R 402
C2A15 0.1 UF 10% 6.3 V X5R 402
V_1P8STBY
C3T24 0.1 UF 10% 6.3 V X5R 402
C3E7 0.1 UF 10% 6.3 V X5R 402
C3R21 0.1 UF 10% 6.3 V X5R 402
C3C3 0.1 UF 10% 6.3 V X5R 402
V_3P3STBY
C3P10 0.1 UF 10% 6.3 V X5R 402
C4V1 0.1 UF 10% 6.3 V X5R 402
C4G1 0.1 UF 10% 6.3 V X5R 402
C4N2 0.1 UF 10% 6.3 V X5R 402
C3R19 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=BOARD, DECOUPLE]

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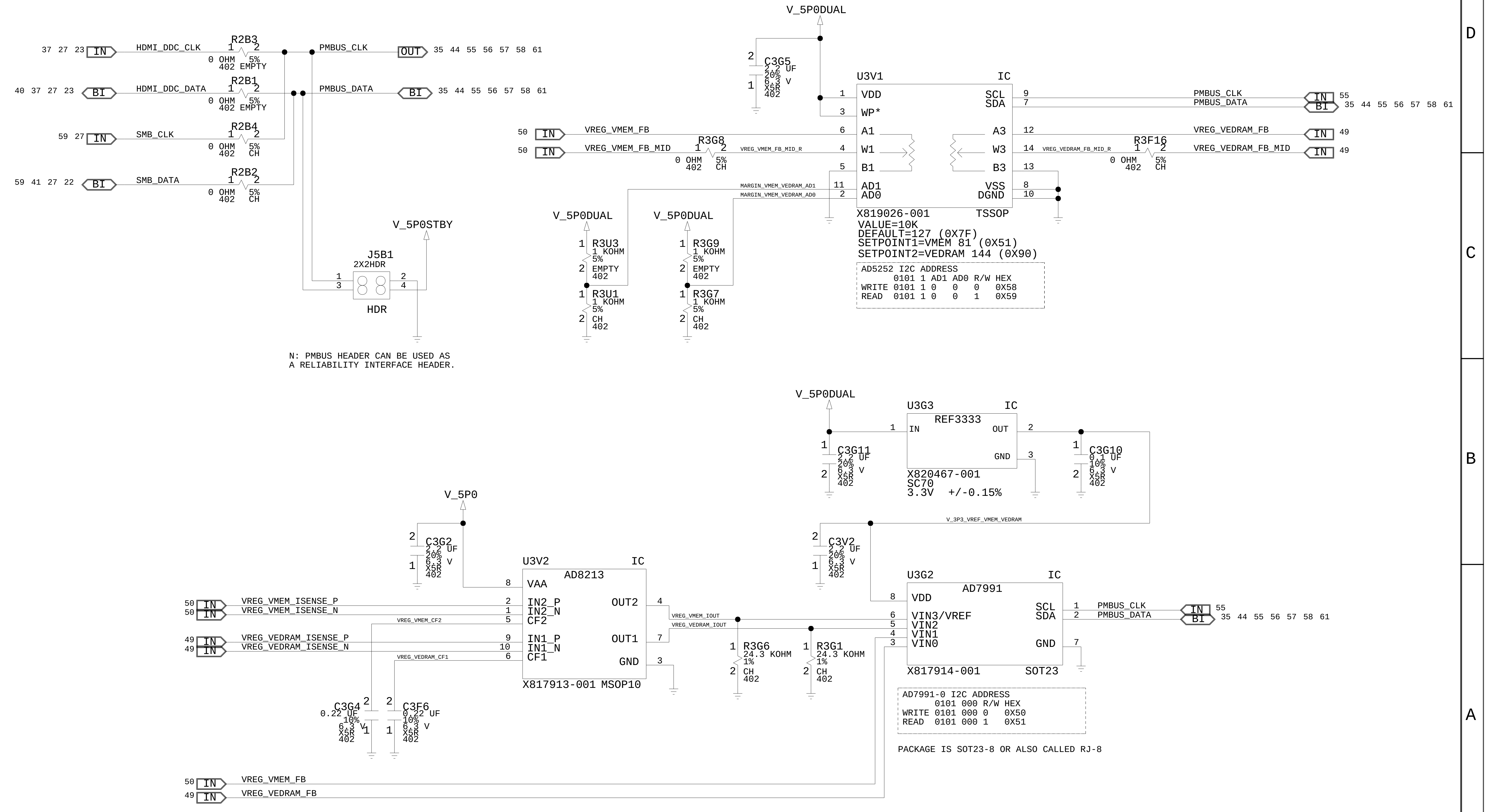
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	54/81	G	1.01

MARGIN, VMEM + VEDRAM



V_5P0DUAL
37 27 23 IN HDMI_DDC_CLK
R2B3 1 2 0 OHM 5% 402 EMPTY
PMBUS_CLK OUT 35 44 55 56 57 58 61
40 37 27 23 BI HDMI_DDC_DATA
R2B1 1 2 0 OHM 5% 402 EMPTY
PMBUS_DATA BI 35 44 55 56 57 58 61
59 27 IN SMB_CLK
R2B4 1 2 0 OHM 5% 402 CH
59 41 27 22 BI SMB_DATA
R2B2 1 2 0 OHM 5% 402 CH
C3G5 2.2 UF 20% 6.3 V X5R 402
U3V1 IC
VDD WP* A1 W1 B1 AD1 AD0
SCL SDA A3 W3 B3 VSS DGND
X819026-001 TSSOP
VALUE=10K
DEFAULT=127 (0X7F)
SETPOINT1=VMEM 81 (0X51)
SETPOINT2=VEDRAM 144 (0X90)
PMBUS_CLK IN 55
PMBUS_DATA BI 35 44 55 56 57 58 61
50 IN VREG_VMEM_FB
50 IN VREG_VMEM_FB_MID
R3G8 1 2 0 OHM 5% 402 CH
VREG_VMEM_FB_MID_R
VREG_VEDRAM_FB IN 49
VREG_VEDRAM_FB_MID IN 49
R3F16 1 2 0 OHM 5% 402 CH
VREG_VEDRAM_FB_MID_R
MARGIN_VMEM_VEDRAM_AD1
MARGIN_VMEM_VEDRAM_AD0
V_5P0DUAL
R3U3 1 KOHM 5% EMPTY 402
R3U1 1 KOHM 5% CH 402
V_5P0DUAL
R3G9 1 KOHM 5% EMPTY 402
R3G7 1 KOHM 5% CH 402
V_5P0STBY
J5B1 2X2HDR HDR
V_5P0DUAL
U3G3 IC REF3333 IN OUT GND
X820467-001 SC70 3.3V +/-0.15%
C3G11 2.2 UF 20% 6.3 V X5R 402
C3G10 0.1 UF 10% 6.3 V X5R 402
V_3P3_VREF_VMEM_VEDRAM
C3V2 2.2 UF 20% 6.3 V X5R 402
V_5P0
C3G2 2.2 UF 20% 6.3 V X5R 402
U3V2 IC AD8213
VAA IN2_P IN2_N CF2 IN1_P IN1_N CF1 OUT2 OUT1 GND
X817913-001 MSOP10
50 IN VREG_VMEM_ISENSE_P
50 IN VREG_VMEM_ISENSE_N
VREG_VMEM_CF2
49 IN VREG_VEDRAM_ISENSE_P
49 IN VREG_VEDRAM_ISENSE_N
VREG_VEDRAM_CF1
C3G4 0.22 UF 10% 6.3 V X5R 402
C3F6 0.22 UF 10% 6.3 V X5R 402
VREG_VMEM_IOUT
VREG_VEDRAM_IOUT
R3G6 24.3 KOHM 1% CH 402
R3G1 24.3 KOHM 1% CH 402
U3G2 IC AD7991
VDD VIN3/VREF VIN2 VIN1 VIN0 SCL SDA GND
X817914-001 SOT23
PMBUS_CLK IN 55
PMBUS_DATA BI 35 44 55 56 57 58 61
50 IN VREG_VMEM_FB
49 IN VREG_VEDRAM_FB

AD5252 I2C ADDRESS

```
      0101 1 AD1 AD0 R/W HEX
WRITE 0101 1 0   0   0   0X58
READ  0101 1 0   0   1   0X59
```

N: PMBUS HEADER CAN BE USED AS
A RELIABILITY INTERFACE HEADER.

AD7991-0 I2C ADDRESS

```
      0101 000 R/W HEX
WRITE 0101 000 0   0X50
READ  0101 000 1   0X51
```

PACKAGE IS SOT23-8 OR ALSO CALLED RJ-8

[PAGE_TITLE=MARGIN, VMEM + VEDRAM]

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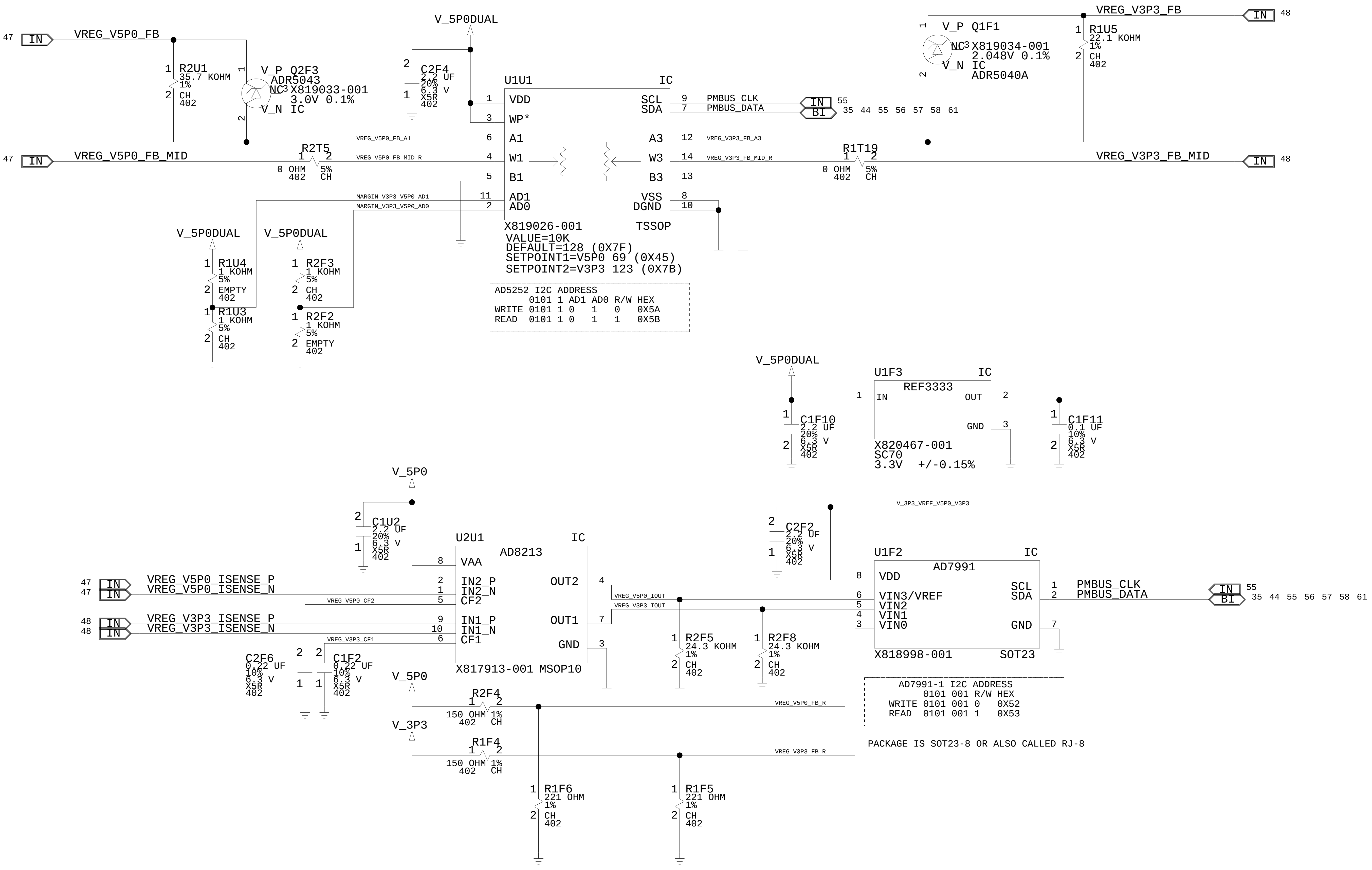
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 55/81	FAB G	REV 1.01

MARGIN, V3P3 + V5P0


47 IN VREG_V5P0_FB
47 IN VREG_V5P0_FB_MID
R2U1 35.7 KOHM 1% CH 402
V_P Q2F3 ADR5043 NC X819033-001 3.0V 0.1% V_N IC
R2T5 0 OHM 402 5% CH
V_5P0DUAL
C2F4 2.2 UF 20% 6.3 V X5R 402
U1U1 IC
VDD WP* A1 W1 B1 AD1 AD0
SCL SDA A3 W3 B3 VSS DGND
VREG_V5P0_FB_A1
VREG_V5P0_FB_MID_R
MARGIN_V3P3_V5P0_AD1
MARGIN_V3P3_V5P0_AD0
X819026-001 TSSOP
PMBUS_CLK
PMBUS_DATA
IN 55
BI 35 44 55 56 57 58 61
VREG_V3P3_FB_A3
VREG_V3P3_FB_MID_R
R1T19 0 OHM 402 5% CH
V_P Q1F1 NC X819034-001 2.048V 0.1% V_N IC ADR5040A
R1U5 22.1 KOHM 1% CH 402
VREG_V3P3_FB IN 48
VREG_V3P3_FB_MID IN 48
R1U4 1 KOHM 5% EMPTY 402
R1U3 1 KOHM 5% CH 402
R2F3 1 KOHM 5% CH 402
R2F2 1 KOHM 5% EMPTY 402
U1F3 IC REF3333 IN OUT GND
X820467-001 SC70 3.3V +/-0.15%
C1F10 2.2 UF 20% 6.3 V X5R 402
C1F11 0.1 UF 10% 6.3 V X5R 402
V_3P3_VREF_V5P0_V3P3
C2F2 2.2 UF 20% 6.3 V X5R 402
U1F2 IC AD7991 VDD VIN3/VREF VIN2 VIN1 VIN0 SCL SDA GND
X818998-001 SOT23
V_5P0
C1U2 2.2 UF 20% 6.3 V X5R 402
U2U1 IC AD8213 VAA IN2_P IN2_N CF2 IN1_P IN1_N CF1 OUT2 OUT1 GND
X817913-001 MSOP10
47 IN VREG_V5P0_ISENSE_P
47 IN VREG_V5P0_ISENSE_N
48 IN VREG_V3P3_ISENSE_P
48 IN VREG_V3P3_ISENSE_N
VREG_V5P0_CF2
VREG_V3P3_CF1
VREG_V5P0_IOUT
VREG_V3P3_IOUT
C2F6 0.22 UF 10% 6.3 V X5R 402
C1F2 0.22 UF 10% 6.3 V X5R 402
R2F5 24.3 KOHM 1% CH 402
R2F8 24.3 KOHM 1% CH 402
R2F4 150 OHM 402 1% CH
R1F4 150 OHM 402 1% CH
V_3P3
VREG_V5P0_FB_R
VREG_V3P3_FB_R
R1F6 221 OHM 1% CH 402
R1F5 221 OHM 1% CH 402

VALUE=10K
DEFAULT=128 (0X7F)
SETPOINT1=V5P0 69 (0X45)
SETPOINT2=V3P3 123 (0X7B)

AD5252 I2C ADDRESS

			AD1	AD0	R/W	HEX
	0101	1	AD1	AD0	R/W	HEX
WRITE	0101	1	0	1	0	0X5A
READ	0101	1	0	1	1	0X5B

AD7991-1 I2C ADDRESS

	0101	001	R/W	HEX
WRITE	0101	001	0	0X52
READ	0101	001	1	0X53

PACKAGE IS SOT23-8 OR ALSO CALLED RJ-8

[PAGE_TITLE=MARGIN, V3P3 + VP50]

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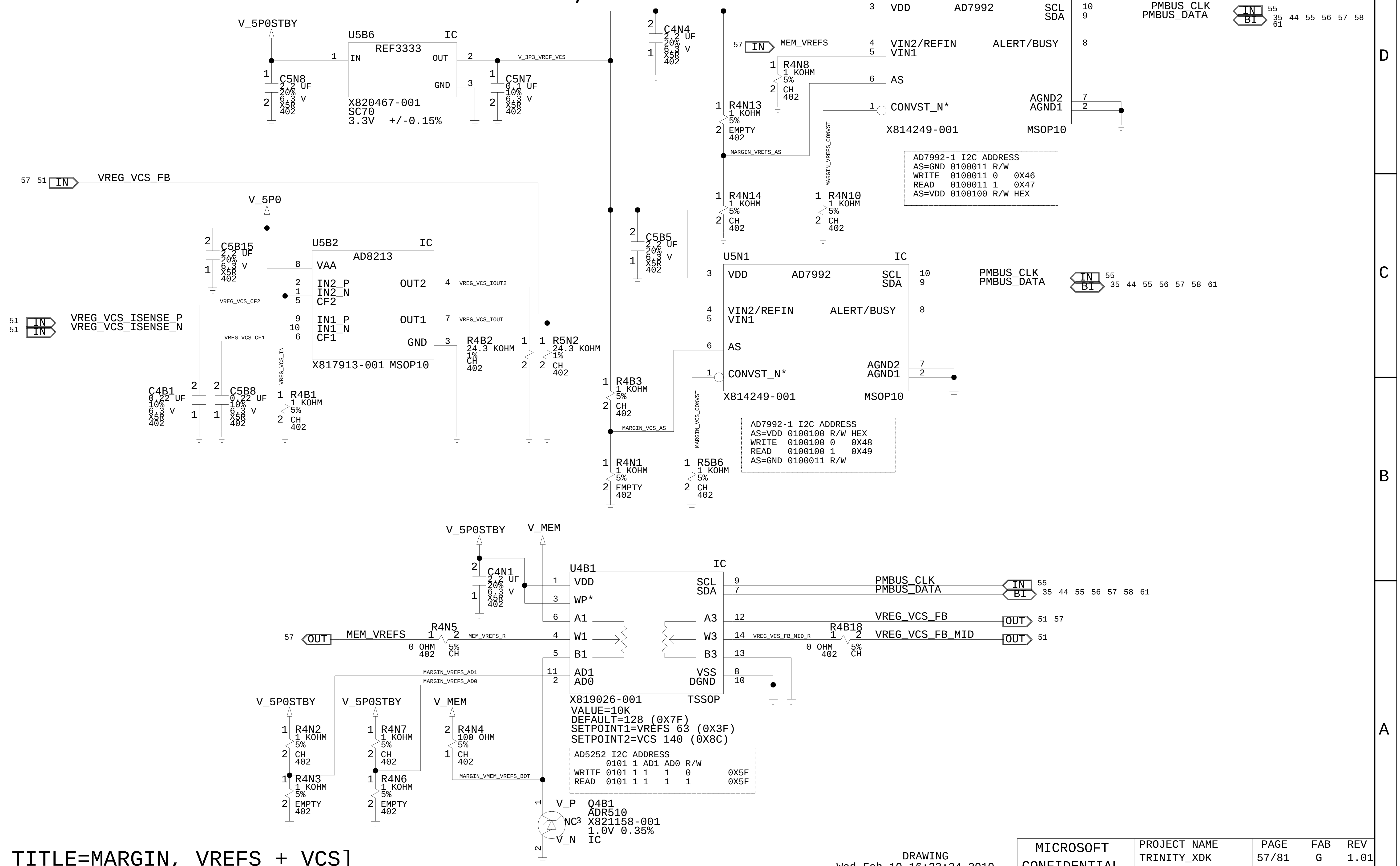
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	56/81	G	1.01

MARGIN, VREFS + VCS


V_5P0STBY
U5B6 IC
REF3333
IN OUT GND
X820467-001
SC70
3.3V +/-0.15%
C5N8 2.2 UF 20% 6.3 V X5R 402
C5N7 0.1 UF 10% 6.3 V X5R 402
V_3P3_VREF_VCS
C4N4 2.2 UF 20% 6.3 V X5R 402
U4B2 IC
AD7992
VDD SCL SDA
VIN2/REFIN ALERT/BUSY
VIN1
AS
CONVST_N*
AGND2 AGND1
X814249-001 MSOP10
MEM_VREFS
R4N8 1 KOHM 5% CH 402
R4N13 1 KOHM 5% EMPTY 402
MARGIN_VREFS_AS
MARGIN_VREFS_CONVST
R4N14 1 KOHM 5% CH 402
R4N10 1 KOHM 5% CH 402
PMBUS_CLK
PMBUS_DATA
IN 55
BI 35 44 55 56 57 58 61
VREG_VCS_FB
57 51 IN
V_5P0
C5B15 2.2 UF 20% 6.3 V X5R 402
U5B2 IC
AD8213
VAA
IN2_P IN2_N CF2
IN1_P IN1_N CF1
OUT2 OUT1 GND
X817913-001 MSOP10
VREG_VCS_IOUT2
VREG_VCS_IOUT
VREG_VCS_CF2
VREG_VCS_CF1
VREG_VCS_IN
51 IN VREG_VCS_ISENSE_P
51 IN VREG_VCS_ISENSE_N
C4B1 0.22 UF 10% 6.3 V X5R 402
C5B8 0.22 UF 10% 6.3 V X5R 402
R4B1 1 KOHM 5% CH 402
R4B2 24.3 KOHM 1% CH 402
R5N2 24.3 KOHM 1% CH 402
C5B5 2.2 UF 20% 6.3 V X5R 402
U5N1 IC
AD7992
VDD SCL SDA
VIN2/REFIN ALERT/BUSY
VIN1
AS
CONVST_N*
AGND2 AGND1
X814249-001 MSOP10
R4B3 1 KOHM 5% CH 402
MARGIN_VCS_AS
MARGIN_VCS_CONVST
R4N1 1 KOHM 5% EMPTY 402
R5B6 1 KOHM 5% CH 402
V_5P0STBY
V_MEM
C4N1 2.2 UF 20% 6.3 V X5R 402
U4B1 IC
VDD WP* A1 W1 B1 AD1 AD0
SCL SDA A3 W3 B3 VSS DGND
X819026-001 TSSOP
57 OUT MEM_VREFS
R4N5 0 OHM 5% 402 CH
MEM_VREFS_R
VREG_VCS_FB OUT 51 57
VREG_VCS_FB_MID_R
R4B18 0 OHM 5% 402 CH
VREG_VCS_FB_MID OUT 51
MARGIN_VREFS_AD1
MARGIN_VREFS_AD0
VALUE=10K
DEFAULT=128 (0X7F)
SETPOINT1=VREFS 63 (0X3F)
SETPOINT2=VCS 140 (0X8C)
V_5P0STBY
V_5P0STBY
V_MEM
R4N2 1 KOHM 5% CH 402
R4N7 1 KOHM 5% CH 402
R4N4 100 OHM 5% CH 402
R4N3 1 KOHM 5% EMPTY 402
R4N6 1 KOHM 5% EMPTY 402
MARGIN_VMEM_VREFS_BOT
V_P Q4B1
ADR510
NC X821158-001
1.0V 0.35%
V_N IC

AD7992-1 I2C ADDRESS
AS=GND 0100011 R/W
WRITE 0100011 0 0X46
READ 0100011 1 0X47
AS=VDD 0100100 R/W HEX

AD7992-1 I2C ADDRESS
AS=VDD 0100100 R/W HEX
WRITE 0100100 0 0X48
READ 0100100 1 0X49
AS=GND 0100011 R/W

AD5252 I2C ADDRESS
0101 1 AD1 AD0 R/W
WRITE 0101 1 1 1 0 0X5E
READ 0101 1 1 1 1 0X5F

[PAGE_TITLE=MARGIN, VREFS + VCS]

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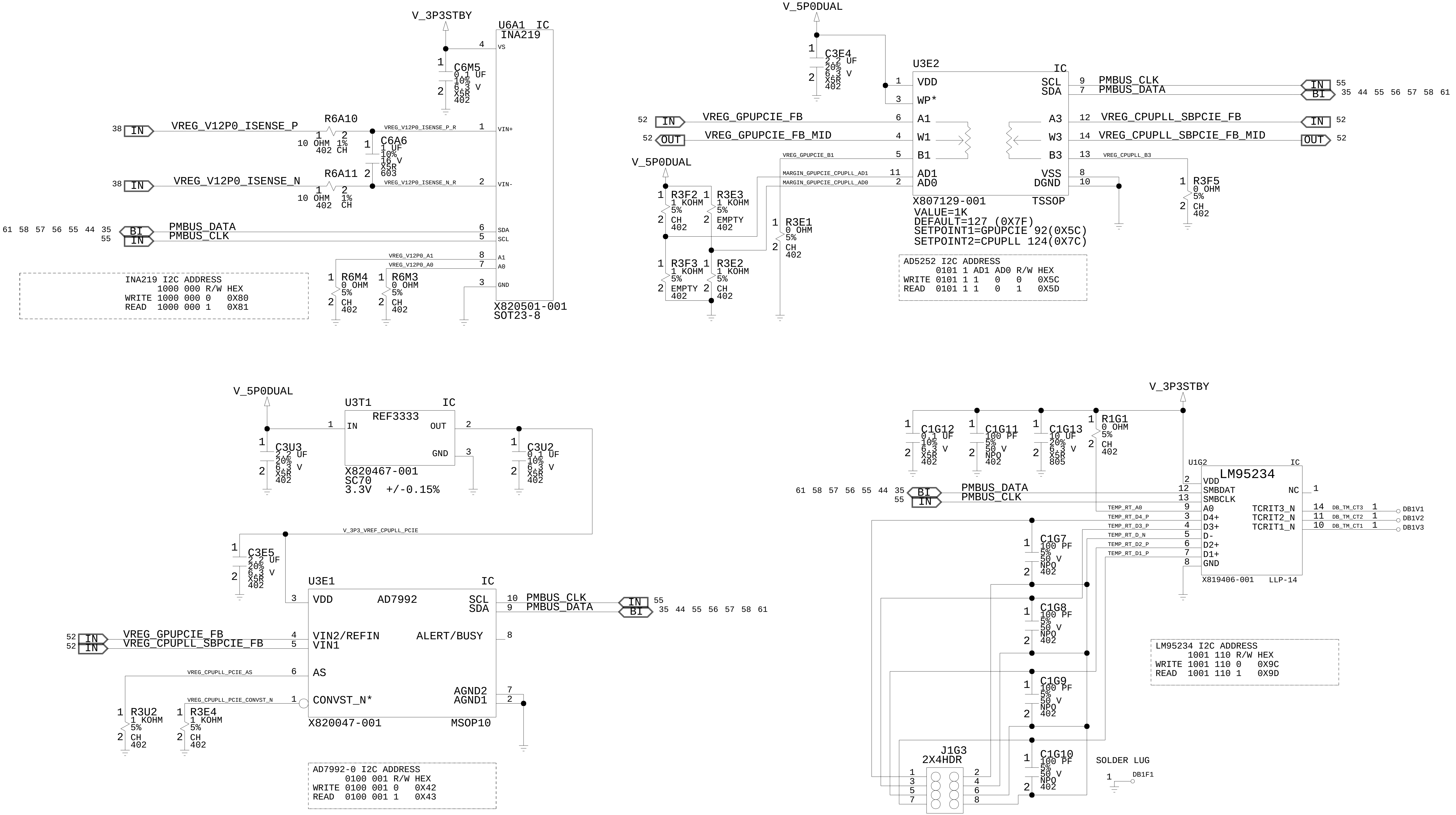
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	57/81	G	1.01

MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP


V_3P3STBY
U6A1 IC
INA219
C6M5 0.1 UF 10% 6.3 V X5R 402
R6A10 10 OHM 1% 402 CH
VREG_V12P0_ISENSE_P
VREG_V12P0_ISENSE_P_R
C6A6 1 UF 10% 16 V X5R 603
R6A11 10 OHM 1% 402 CH
VREG_V12P0_ISENSE_N
VREG_V12P0_ISENSE_N_R
VS
VIN+
VIN-
SDA
SCL
A1
A0
GND
38 IN
61 58 57 56 55 44 35 BI PMBUS_DATA
55 IN PMBUS_CLK
VREG_V12P0_A1
VREG_V12P0_A0
R6M4 0 OHM 5% CH 402
R6M3 0 OHM 5% CH 402
X820501-001
SOT23-8
V_5P0DUAL
C3E4 2.2 UF 20% 6.3 V X5R 402
U3E2 IC
VDD
WP*
A1
W1
B1
AD1
AD0
SCL
SDA
A3
W3
B3
VSS
DGND
PMBUS_CLK IN 55
PMBUS_DATA BI 35 44 55 56 57 58 61
52 IN VREG_GPUPCIE_FB
52 OUT VREG_GPUPCIE_FB_MID
VREG_GPUPCIE_B1
MARGIN_GPUPCIE_CPUPLL_AD1
MARGIN_GPUPCIE_CPUPLL_AD0
VREG_CPUPLL_SBPCIE_FB IN 52
VREG_CPUPLL_SBPCIE_FB_MID OUT 52
VREG_CPUPLL_B3
X807129-001 TSSOP
VALUE=1K
DEFAULT=127 (0X7F)
SETPOINT1=GPUPCIE 92(0X5C)
SETPOINT2=CPUPLL 124(0X7C)
R3F5 0 OHM 5% CH 402
R3F2 1 KOHM 5% CH 402
R3E3 1 KOHM 5% EMPTY 402
R3F3 1 KOHM 5% EMPTY 402
R3E2 1 KOHM 5% CH 402
R3E1 0 OHM 5% CH 402
U3T1 IC
REF3333
IN
OUT
GND
X820467-001
SC70
3.3V +/-0.15%
C3U3 2.2 UF 20% 6.3 V X5R 402
C3U2 0.1 UF 10% 6.3 V X5R 402
V_3P3_VREF_CPUPLL_PCIE
C3E5 2.2 UF 20% 6.3 V X5R 402
U3E1 IC
AD7992
VDD
VIN2/REFIN
VIN1
AS
CONVST_N*
SCL
SDA
ALERT/BUSY
AGND2
AGND1
PMBUS_CLK IN 55
PMBUS_DATA BI 35 44 55 56 57 58 61
52 IN VREG_GPUPCIE_FB
52 IN VREG_CPUPLL_SBPCIE_FB
VREG_CPUPLL_PCIE_AS
VREG_CPUPLL_PCIE_CONVST_N
R3U2 1 KOHM 5% CH 402
R3E4 1 KOHM 5% CH 402
X820047-001
MSOP10
C1G12 0.1 UF 10% 6.3 V X5R 402
C1G11 100 PF 5% 50 V NPO 402
C1G13 10 UF 20% 6.3 V X5R 805
R1G1 0 OHM 5% CH 402
U1G2 IC
LM95234
VDD
SMBDAT
SMBCLK
A0
D4+
D3+
D-
D2+
D1+
GND
NC
TCRIT3_N
TCRIT2_N
TCRIT1_N
61 58 57 56 55 44 35 BI PMBUS_DATA
55 IN PMBUS_CLK
TEMP_RT_A0
TEMP_RT_D4_P
TEMP_RT_D3_P
TEMP_RT_D_N
TEMP_RT_D2_P
TEMP_RT_D1_P
DB_TM_CT3
DB_TM_CT2
DB_TM_CT1
DB1V1
DB1V2
DB1V3
X819406-001 LLP-14
C1G7 100 PF 5% 50 V NPO 402
C1G8 100 PF 5% 50 V NPO 402
C1G9 100 PF 5% 50 V NPO 402
C1G10 100 PF 5% 50 V NPO 402
J1G3
2X4HDR
HDR
SOLDER LUG
DB1F1

INA219 I2C ADDRESS

	1000 000	R/W	HEX
WRITE	1000 000	0	0X80
READ	1000 000	1	0X81

AD5252 I2C ADDRESS

	0101	1	AD1	AD0	R/W	HEX
WRITE	0101	1	1	0	0	0X5C
READ	0101	1	1	0	1	0X5D

AD7992-0 I2C ADDRESS

	0100 001	R/W	HEX
WRITE	0100 001	0	0X42
READ	0100 001	1	0X43

LM95234 I2C ADDRESS

	1001 110	R/W	HEX
WRITE	1001 110	0	0X9C
READ	1001 110	1	0X9D

[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

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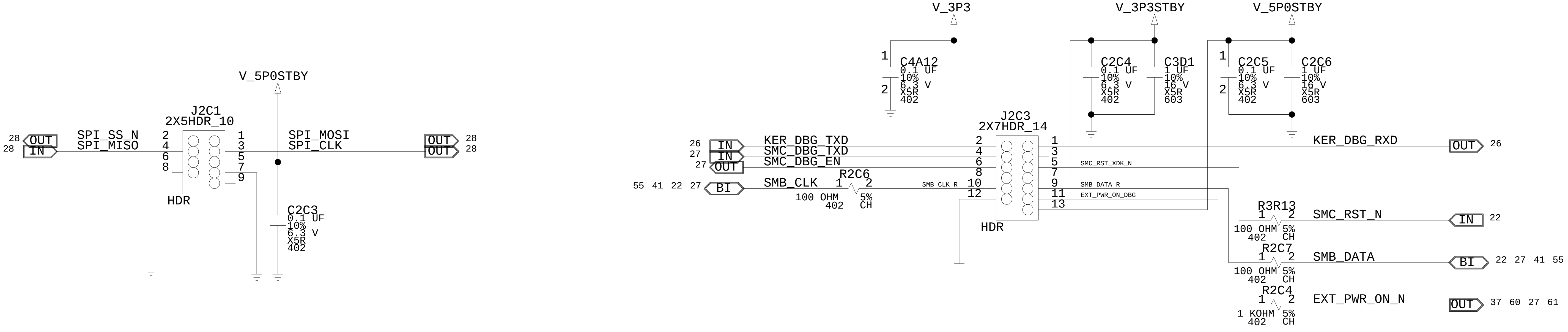
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	58/81	G	1.01

XDK, DEBUG CONNECTORS


V_5P0STBY
J2C1
2X5HDR_10
HDR
28 OUT SPI_SS_N 2
28 IN SPI_MISO 4
6
8
1 SPI_MOSI OUT 28
3 SPI_CLK OUT 28
5
7
9
C2C3
0.1 UF
10%
6.3 V
X5R
402
V_3P3
C4A12
0.1 UF
10%
6.3 V
X5R
402
V_3P3STBY
C2C4
0.1 UF
10%
6.3 V
X5R
402
C3D1
1 UF
10%
16 V
X5R
603
V_5P0STBY
C2C5
0.1 UF
10%
6.3 V
X5R
402
C2C6
1 UF
10%
16 V
X5R
603
J2C3
2X7HDR_14
HDR
26 IN KER_DBG_TXD 2
27 IN SMC_DBG_TXD 4
27 OUT SMC_DBG_EN 6
8
55 41 22 27 BI SMB_CLK
R2C6
100 OHM 402 5% CH
SMB_CLK_R 10
12
1 KER_DBG_RXD OUT 26
3
5 SMC_RST_XDK_N
7
9 SMB_DATA_R
11 EXT_PWR_ON_DBG
13
R3R13
100 OHM 5% 402 CH
SMC_RST_N IN 22
R2C7
100 OHM 5% 402 CH
SMB_DATA BI 22 27 41 55
R2C4
1 KOHM 5% 402 CH
EXT_PWR_ON_N OUT 37 60 27 61

[PAGE_TITLE=XDK. DEBUG CONN]

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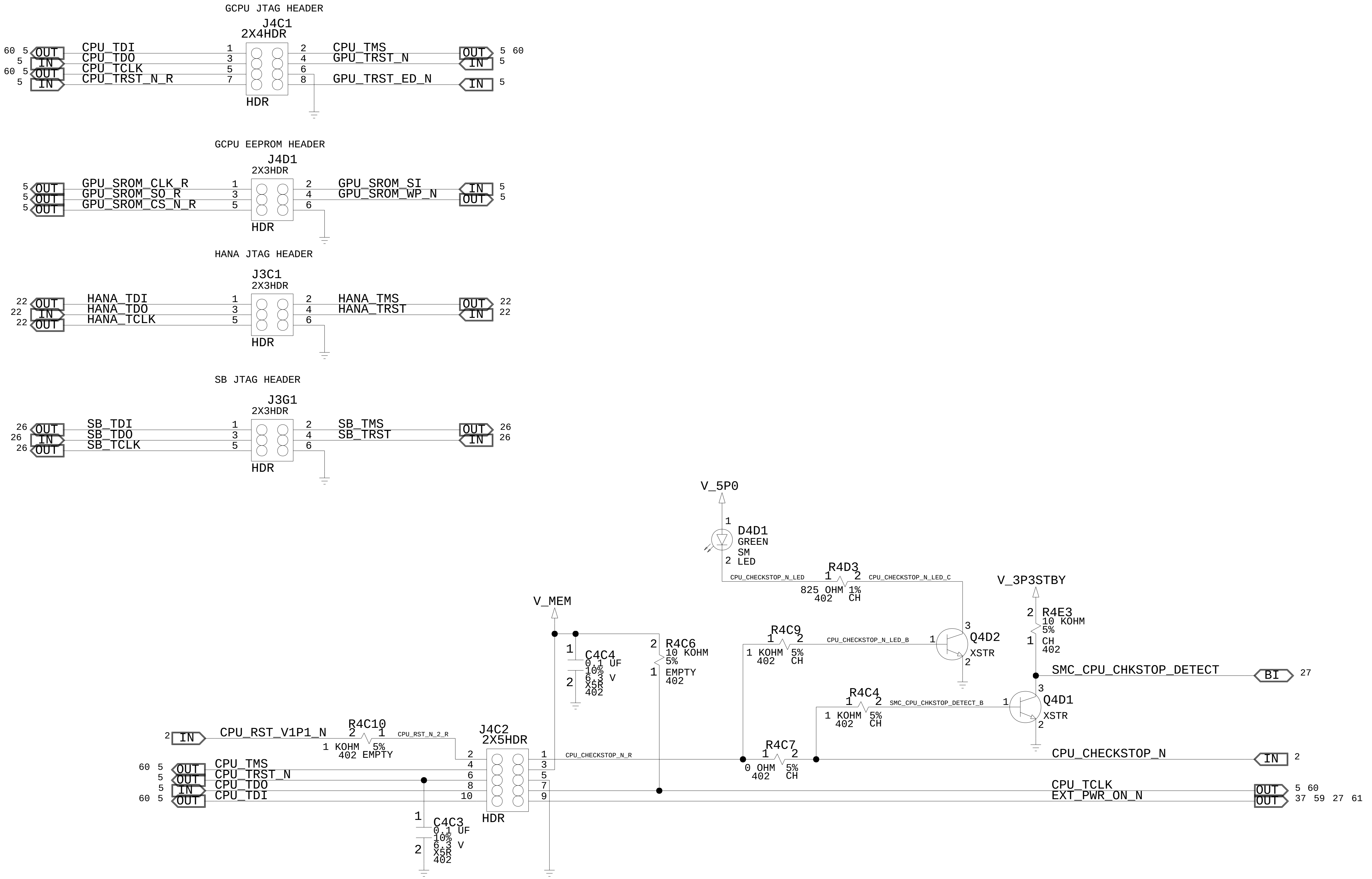
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 59/81	FAB G	REV 1.01

XDK DEBUG


GCPU JTAG HEADER
J4C1
2X4HDR
HDR
CPU_TDI
CPU_TDO
CPU_TCLK
CPU_TRST_N_R
CPU_TMS
GPU_TRST_N
GPU_TRST_ED_N
OUT
IN
60 5
5
5 60
GCPU EEPROM HEADER
J4D1
2X3HDR
GPU_SROM_CLK_R
GPU_SROM_SO_R
GPU_SROM_CS_N_R
GPU_SROM_SI
GPU_SROM_WP_N
HANA JTAG HEADER
J3C1
2X3HDR
HANA_TDI
HANA_TDO
HANA_TCLK
HANA_TMS
HANA_TRST
22
SB JTAG HEADER
J3G1
2X3HDR
SB_TDI
SB_TDO
SB_TCLK
SB_TMS
SB_TRST
26
V_5P0
D4D1
GREEN
SM
LED
CPU_CHECKSTOP_N_LED
R4D3
825 OHM 1%
402 CH
CPU_CHECKSTOP_N_LED_C
V_3P3STBY
R4E3
10 KOHM
5%
CH
402
V_MEM
C4C4
0.1 UF
10%
6.3 V
X5R
402
R4C6
10 KOHM
5%
EMPTY
402
R4C9
1 KOHM 5%
402 CH
CPU_CHECKSTOP_N_LED_B
Q4D2
XSTR
SMC_CPU_CHKSTOP_DETECT
BI
27
R4C4
1 KOHM 5%
402 CH
SMC_CPU_CHKSTOP_DETECT_B
Q4D1
XSTR
CPU_RST_V1P1_N
R4C10
1 KOHM 5%
402 EMPTY
CPU_RST_N_2_R
J4C2
2X5HDR
HDR
CPU_CHECKSTOP_N_R
R4C7
0 OHM 5%
402 CH
CPU_CHECKSTOP_N
CPU_TMS
CPU_TRST_N
CPU_TDO
CPU_TDI
CPU_TCLK
EXT_PWR_ON_N
5 60
37 59 27 61
C4C3
0.1 UF
10%
6.3 V
X5R
402

[PAGE_TITLE=XDK, DEBUG TITAN]

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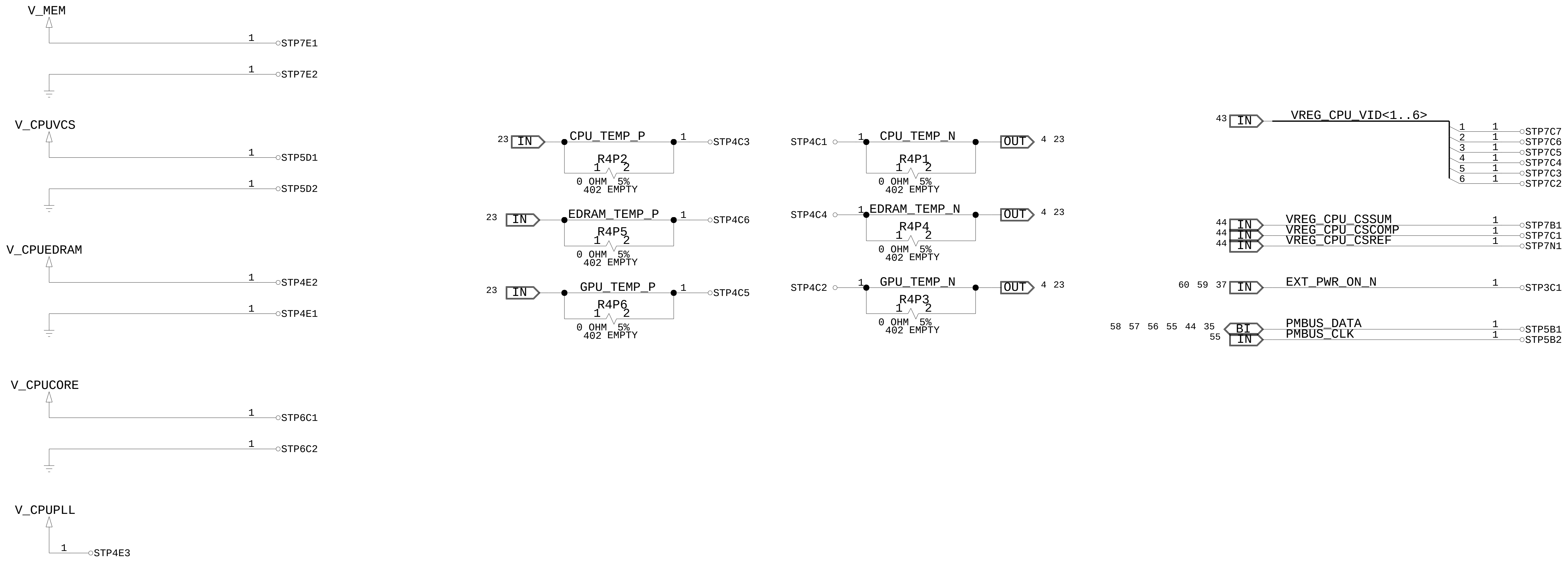
Wed Feb 10 16:23:35 2010		TRINITY_XDK	60/81	G	1.01

DEBUG BOARD, SPYDER CONN

ALL STP POINTS SHALL BE ADDED TO TOP SIDE IN LAYOUT


V_MEM
1 STP7E1
1 STP7E2
V_CPUVCS
1 STP5D1
1 STP5D2
V_CPUEDRAM
1 STP4E2
1 STP4E1
V_CPUCORE
1 STP6C1
1 STP6C2
V_CPUPLL
1 STP4E3
23 IN CPU_TEMP_P
R4P2 1 2
0 OHM 5%
402 EMPTY
1 STP4C3
23 IN EDRAM_TEMP_P
R4P5 1 2
0 OHM 5%
402 EMPTY
1 STP4C6
23 IN GPU_TEMP_P
R4P6 1 2
0 OHM 5%
402 EMPTY
1 STP4C5
STP4C1 1 CPU_TEMP_N
R4P1 1 2
0 OHM 5%
402 EMPTY
OUT 4 23
STP4C4 1 EDRAM_TEMP_N
R4P4 1 2
0 OHM 5%
402 EMPTY
OUT 4 23
STP4C2 1 GPU_TEMP_N
R4P3 1 2
0 OHM 5%
402 EMPTY
OUT 4 23
43 IN VREG_CPU_VID<1..6>
1 1 STP7C7
2 1 STP7C6
3 1 STP7C5
4 1 STP7C4
5 1 STP7C3
6 1 STP7C2
44 IN VREG_CPU_CSSUM 1 STP7B1
44 IN VREG_CPU_CSCOMP 1 STP7C1
44 IN VREG_CPU_CSREF 1 STP7N1
60 59 37 IN EXT_PWR_ON_N 1 STP3C1
58 57 56 55 44 35 BI PMBUS_DATA 1 STP5B1
55 IN PMBUS_CLK 1 STP5B2

[PAGE_TITLE=DEBUG BOARD, SPYDER CONN]

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MICROSOFT
CONFIDENTIAL

PROJECT NAME	PAGE	FAB	REV
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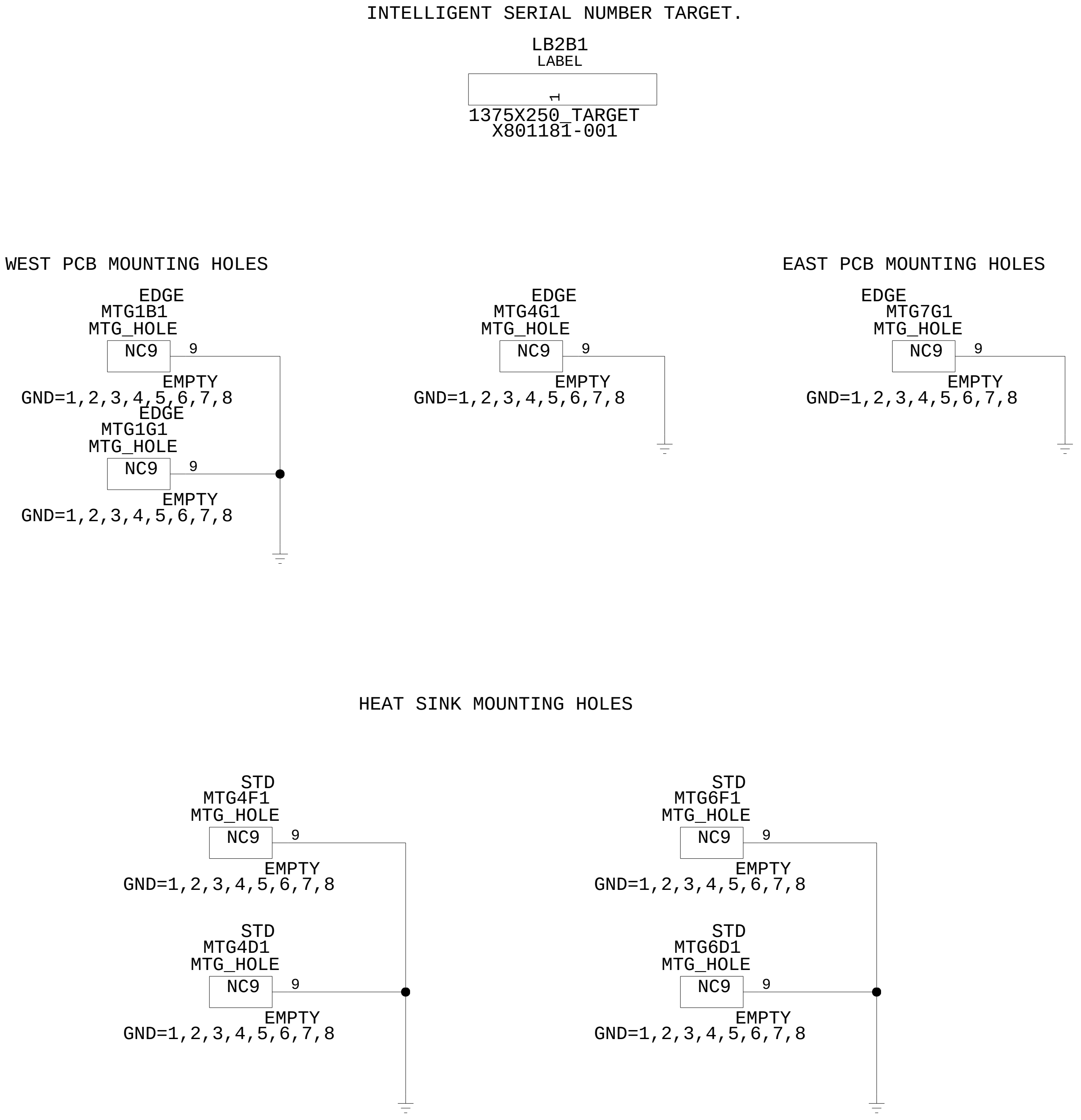
LABELS AND MOUNTING


INTELLIGENT SERIAL NUMBER TARGET.
LB2B1
LABEL
1
1375X250_TARGET
X801181-001
WEST PCB MOUNTING HOLES
EDGE
MTG1B1
MTG_HOLE
NC9
9
EMPTY
GND=1,2,3,4,5,6,7,8
EDGE
MTG1G1
MTG_HOLE
NC9
9
EMPTY
GND=1,2,3,4,5,6,7,8
EDGE
MTG4G1
MTG_HOLE
NC9
9
EMPTY
GND=1,2,3,4,5,6,7,8
EAST PCB MOUNTING HOLES
EDGE
MTG7G1
MTG_HOLE
NC9
9
EMPTY
GND=1,2,3,4,5,6,7,8
HEAT SINK MOUNTING HOLES
STD
MTG4F1
MTG_HOLE
NC9
9
EMPTY
GND=1,2,3,4,5,6,7,8
STD
MTG4D1
MTG_HOLE
NC9
9
EMPTY
GND=1,2,3,4,5,6,7,8
STD
MTG6F1
MTG_HOLE
NC9
9
EMPTY
GND=1,2,3,4,5,6,7,8
STD
MTG6D1
MTG_HOLE
NC9
9
EMPTY
GND=1,2,3,4,5,6,7,8

[PAGE_TITLE=LABELS AND MOUNTING]

DRAWING
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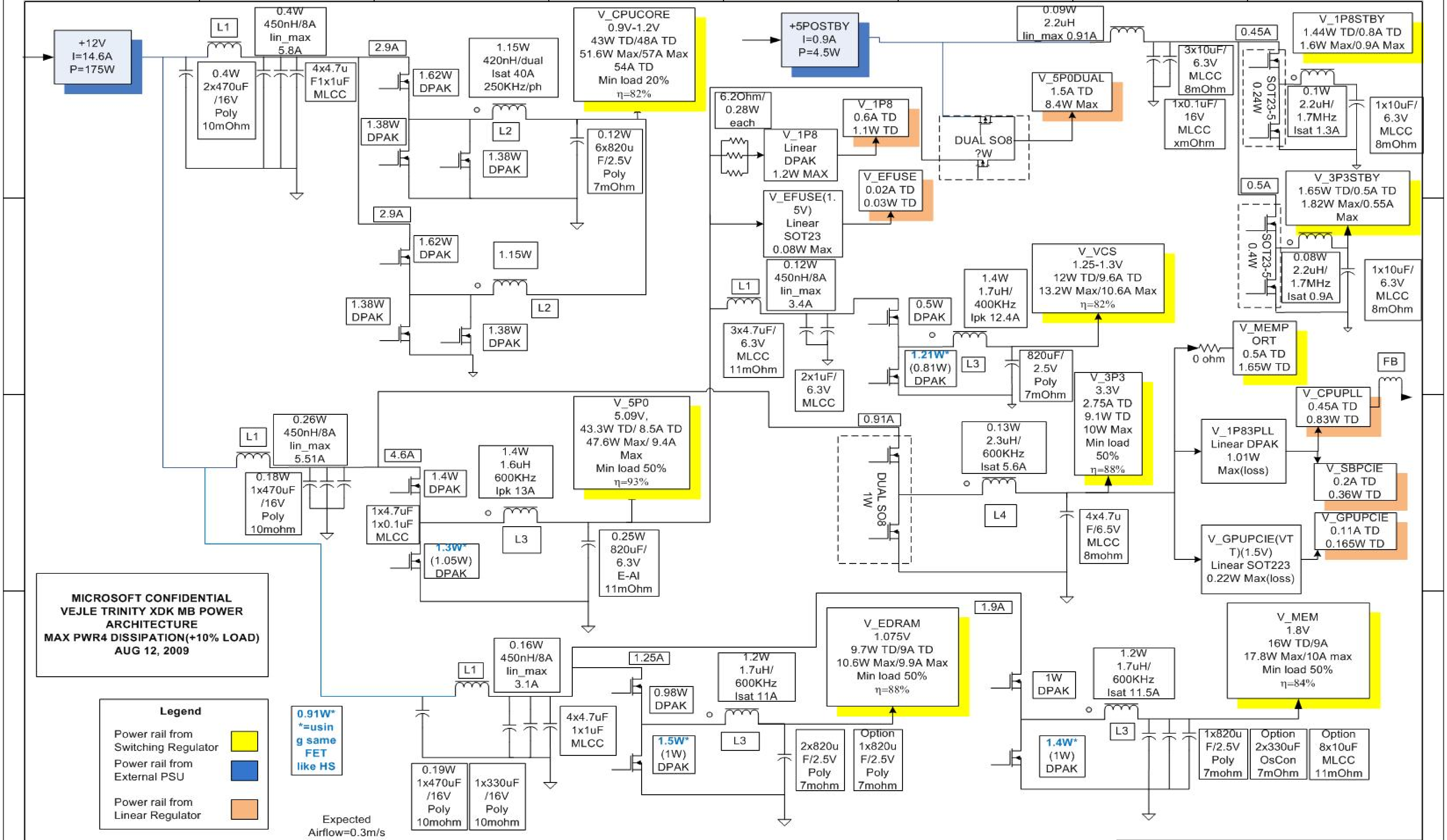
MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 62/81	FAB G	REV 1.01


+12V
I=14.6A
P=175W
L1
0.4W
450nH/8A
lin_max
5.8A
0.4W
2x470uF
/16V
Poly
10mOhm
4x4.7u
F1x1uF
MLCC
2.9A
1.62W
DPAK
1.38W
DPAK
1.15W
420nH/dual
Isat 40A
250KHz/ph
L2
1.38W
DPAK
V_CPUCORE
0.9V-1.2V
43W TD/48A TD
51.6W Max/57A Max
54A TD
Min load 20%
η=82%
0.12W
6x820u
F/2.5V
Poly
7mOhm
2.9A
1.62W
DPAK
1.15W
1.38W
DPAK
L2
1.38W
DPAK
+5POSTBY
I=0.9A
P=4.5W
0.09W
2.2uH
lin_max 0.91A
0.45A
V_1P8STBY
1.44W TD/0.8A TD
1.6W Max/0.9A Max
3x10uF/
6.3V
MLCC
8mOhm
1x0.1uF/
16V
MLCC
xmOhm
SOT23-5
0.24W
0.1W
2.2uH/
1.7MHz
Isat 1.3A
1x10uF/
6.3V
MLCC
8mOhm
6.2Ohm/
0.28W
each
V_1P8
Linear
DPAK
1.2W MAX
V_1P8
0.6A TD
1.1W TD
DUAL SO8
?W
V_5P0DUAL
1.5A TD
8.4W Max
V_EFUSE(1.5V)
Linear
SOT23
0.08W Max
V_EFUSE
0.02A TD
0.03W TD
0.5A
V_3P3STBY
1.65W TD/0.5A TD
1.82W Max/0.55A
Max
SOT23-5
0.4W
0.08W
2.2uH/
1.7MHz
Isat 0.9A
1x10uF/
6.3V
MLCC
8mOhm
L1
0.12W
450nH/8A
lin_max
3.4A
3x4.7uF/
6.3V
MLCC
11mOhm
2x1uF/
6.3V
MLCC
0.5W
DPAK
1.4W
1.7uH/
400KHz
Ipk 12.4A
V_VCS
1.25-1.3V
12W TD/9.6A TD
13.2W Max/10.6A Max
η=82%
1.21W*
(0.81W)
DPAK
L3
820uF/
2.5V
Poly
7mOhm
V_MEMPORT
0.5A TD
1.65W TD
0 ohm
FB
V_CPUPLL
0.45A TD
0.83W TD
V_3P3
3.3V
2.75A TD
9.1W TD
10W Max
Min load
50%
η=88%
0.91A
DUAL SO8
1W
0.13W
2.3uH/
600KHz
Isat 5.6A
L4
4x4.7u
F/6.5V
MLCC
8mohm
V_1P83PLL
Linear DPAK
1.01W
Max(loss)
V_SBPCIE
0.2A TD
0.36W TD
V_GPUPCIE(VT
T)(1.5V)
Linear SOT223
0.22W Max(loss)
V_GPUPCIE
0.11A TD
0.165W TD
L1
0.26W
450nH/8A
lin_max
5.51A
0.18W
1x470uF
/16V
Poly
10mohm
4.6A
1.4W
DPAK
1.4W
1.6uH
600KHz
Ipk 13A
V_5P0
5.09V,
43.3W TD/ 8.5A TD
47.6W Max/ 9.4A
Max
Min load 50%
η=93%
1x4.7uF
1x0.1uF
MLCC
L3
1.3W*
(1.05W)
DPAK
0.25W
820uF/
6.3V
E-Al
11mOhm
1.9A
V_EDRAM
1.075V
9.7W TD/9A TD
10.6W Max/9.9A Max
Min load 50%
η=88%
V_MEM
1.8V
16W TD/9A
17.8W Max/10A max
Min load 50%
η=84%
L1
0.16W
450nH/8A
lin_max
3.1A
1.25A
0.98W
DPAK
1.2W
1.7uH/
600KHz
Isat 11A
4x4.7uF
1x1uF
MLCC
1.5W*
(1W)
DPAK
L3
2x820u
F/2.5V
Poly
7mohm
Option
1x820u
F/2.5V
Poly
7mohm
1W
DPAK
1.2W
1.7uH/
600KHz
Isat 11.5A
L3
1.4W*
(1W)
DPAK
1x820u
F/2.5V
Poly
7mohm
Option
2x330uF
OsCon
7mOhm
Option
8x10uF
MLCC
11mOhm
0.19W
1x470uF
/16V
Poly
10mohm
1x330uF
/16V
Poly
10mohm
0.91W*
*=using same FET like HS
Expected
Airflow=0.3m/s

MICROSOFT CONFIDENTIAL
VEJLE TRINITY XDK MB POWER ARCHITECTURE
MAX PWR4 DISSIPATION(+10% LOAD)
AUG 12, 2009

Legend

Power rail from Switching Regulator	🟨
Power rail from External PSU	🟦
Power rail from Linear Regulator	🟧

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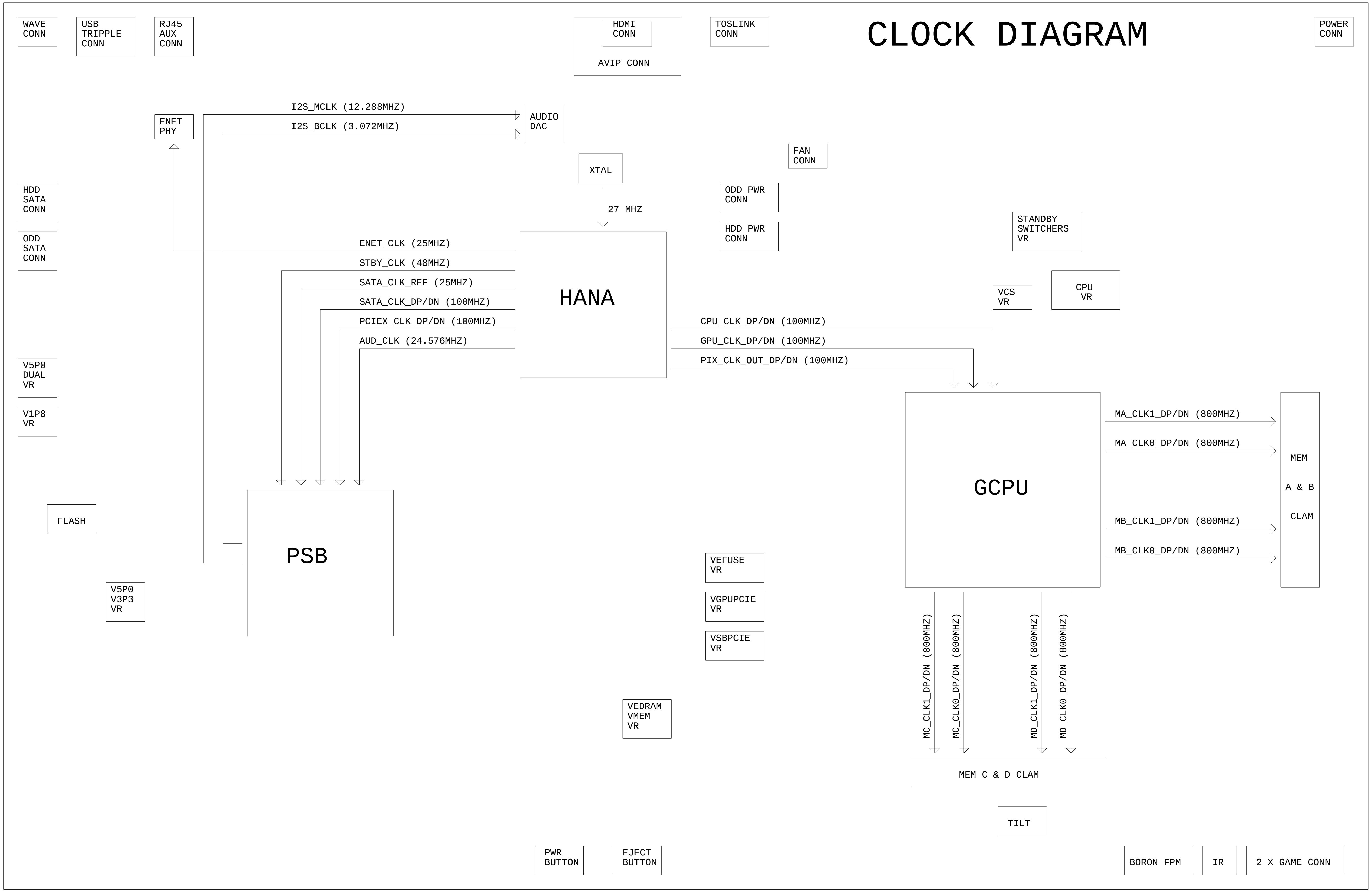
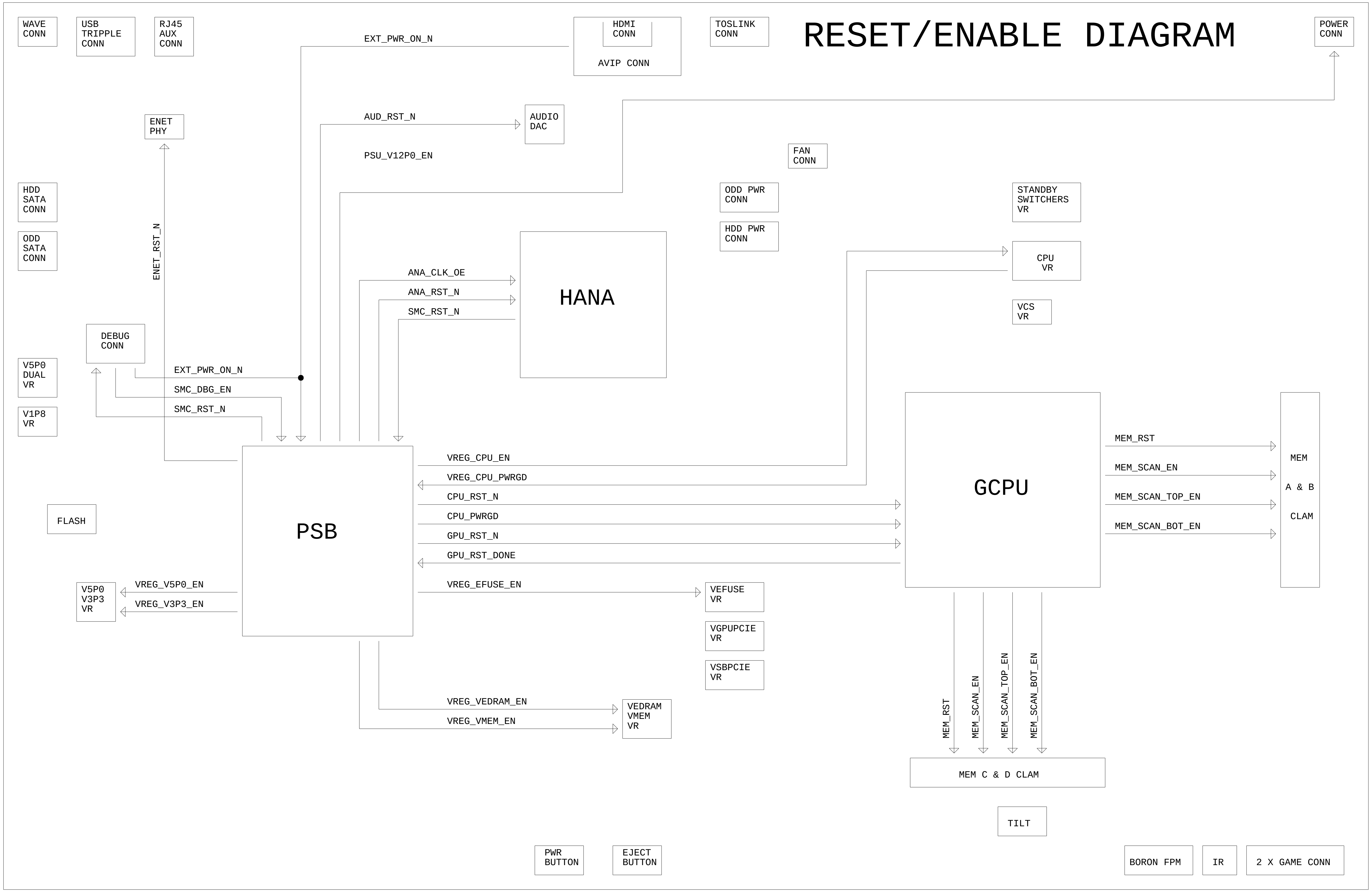
CLOCK DIAGRAM


WAVE CONN
USB TRIPPLE CONN
RJ45 AUX CONN
HDMI CONN
AVIP CONN
TOSLINK CONN
POWER CONN
ENET PHY
I2S_MCLK (12.288MHZ)
I2S_BCLK (3.072MHZ)
AUDIO DAC
XTAL
27 MHZ
FAN CONN
ODD PWR CONN
HDD PWR CONN
STANDBY SWITCHERS VR
HDD SATA CONN
ODD SATA CONN
ENET_CLK (25MHZ)
STBY_CLK (48MHZ)
SATA_CLK_REF (25MHZ)
SATA_CLK_DP/DN (100MHZ)
PCIEX_CLK_DP/DN (100MHZ)
AUD_CLK (24.576MHZ)
HANA
VCS VR
CPU VR
CPU_CLK_DP/DN (100MHZ)
GPU_CLK_DP/DN (100MHZ)
PIX_CLK_OUT_DP/DN (100MHZ)
V5P0 DUAL VR
V1P8 VR
GCPU
MA_CLK1_DP/DN (800MHZ)
MA_CLK0_DP/DN (800MHZ)
MB_CLK1_DP/DN (800MHZ)
MB_CLK0_DP/DN (800MHZ)
MEM A & B CLAM
FLASH
PSB
V5P0 V3P3 VR
VEFUSE VR
VGPUPCIE VR
VSBPCIE VR
MC_CLK1_DP/DN (800MHZ)
MC_CLK0_DP/DN (800MHZ)
MD_CLK1_DP/DN (800MHZ)
MD_CLK0_DP/DN (800MHZ)
MEM C & D CLAM
VEDRAM VMEM VR
TILT
PWR BUTTON
EJECT BUTTON
BORON FPM
IR
2 X GAME CONN

RESET/ENABLE DIAGRAM


WAVE CONN
USB TRIPPLE CONN
RJ45 AUX CONN
EXT_PWR_ON_N
HDMI CONN
AVIP CONN
TOSLINK CONN
POWER CONN
ENET PHY
AUD_RST_N
AUDIO DAC
PSU_V12P0_EN
FAN CONN
HDD SATA CONN
ODD SATA CONN
ENET_RST_N
ODD PWR CONN
HDD PWR CONN
STANDBY SWITCHERS VR
CPU VR
ANA_CLK_OE
ANA_RST_N
SMC_RST_N
HANA
VCS VR
DEBUG CONN
V5P0 DUAL VR
EXT_PWR_ON_N
SMC_DBG_EN
V1P8 VR
SMC_RST_N
GCPU
MEM_RST
MEM_SCAN_EN
MEM_SCAN_TOP_EN
MEM_SCAN_BOT_EN
MEM A & B CLAM
VREG_CPU_EN
VREG_CPU_PWRGD
CPU_RST_N
CPU_PWRGD
GPU_RST_N
GPU_RST_DONE
FLASH
PSB
V5P0 V3P3 VR
VREG_V5P0_EN
VREG_V3P3_EN
VREG_EFUSE_EN
VEFUSE VR
VGPUPCIE VR
VSBPCIE VR
VREG_VEDRAM_EN
VREG_VMEM_EN
VEDRAM VMEM VR
MEM_RST
MEM_SCAN_EN
MEM_SCAN_TOP_EN
MEM_SCAN_BOT_EN
MEM C & D CLAM
TILT
PWR BUTTON
EJECT BUTTON
BORON FPM
IR
2 X GAME CONN

<PAGE_TITLE=CLOCK DIAGRAM>

DRAWING
TRINITY_FAB_A
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MICROSOFT CONFIDENTIAL	PROJECT NAME TRINITY_XDK	PAGE 65/81	REV 1.01

REFERENCE TABLE

N: MICREL STUFFED BY DEFAULT

REF DES TO STUFF

MICREL	ATHEROS
C2C8	C2C8
C2C9	C2C9
C2D1	C2C10
C2D3	C2D2
C2P2	C2D3
C2P3	C2D4
C2P4	C2D5
C2P5	C2P2
C2R5	C2P4
C2R6	C2P5
FB2C1	C2R3
R2D1	FB2C1
R2D2	FB2R1
R2D3	R2D2
R2D4	R2D4
R2D6	R2R1
R2R10	R2R10
R2R2	R2R11
R2R4	R2R12
R2R8	R2R13
U2D1	R2R15
	R2R3
	R2R5
	R2R6
	R2R7
	R2R9
	U2D1

N: FOR MICREL U2D1 IS P/N X819763-001
N: FOR ATHEROS U2D1 IS P/N X820024-001

DIGITAL POTENTIOMETERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESSES
VMEM	256	0.007031V	W: 01011000 0X58, R: 01011001 0X59
VEDRAM	256	0.004199V	W: 01011000 0X58, R: 01011001 0X59
V5P0	256	0.011719V	W: 01011010 0X5A, R: 01011011 0X5B
V3P3	256	0.008V	W: 01011010 0X5A, R: 01011011 0X5B
VREF	256	0.007031V	W: 01011110 0X5E, R: 01011111 0X5F
VCS	256	?V	W: 01011110 0X5E, R: 01011111 0X5F
GPUPCIE	256	0.005859V	W: 01011100 0X5C, R: 01011101 0X5D
CPUPLL_SBPCIE	256	0.007148V	W: 01011100 0X5C, R: 01011101 0X5D

ANALOG TO DIGITAL CONVERTERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESSES
VMEM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
VEDRAM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
V5P0	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
V3P3	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
VCS	4096	0.000806V	W: 01001000 0X48, R: 01001001 0X49
MEM_VREF	4096	0.000806V	W: 01000110 0X46, R: 01000111 0X47
GPUPCIE	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43
CPUPLL_SBPCIE	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43

[PAGE_TITLE=REFERENCE TABLES]

TRINITY DOC TRACKER

DOC #	DESCRIPTION
H08752	TRINITY CONSOLE MONITORING AND MARGINING
H08772	TRINITY CONSOLE FAN DRIVER / THERMAL ALGORITHM
H09297	TRINITY HS PWM FAN SPECIFICATION
H07617	TRINITY VEJLE THERMAL DESIGN AND QUAL SPECIFICATION
H05204	TRINITY PCB TECHNOLOGY SPECIFICATION
H08753	TRINITY CONSOLE HDD SPECIFICATION
H08938	ODD COMP SPEC
H08939	ODD ATA INTERFACE SPEC
H02235	ODD AP MEDIA SPECIFICATION
H08771	TRINITY CONSOLE TEST HOOK SPECIFICATION
	DFM GUIDELINES
H08756	TRINITY CONSOLE USB SPECIFICATION
H08762	TRINITY CONSOLE V_5P0 REGULATOR SPECIFICATION
	TRINITY CONSOLE V_5P0DUAL SPECIFICATION
	TRINITY CONSOLE BLEEDER SPECIFICATION
H08759	TRINITY CONSOLE V_CPUVCS REGULATOR SPECIFICATION
H08760	TRINITY CONSOLE V_3P3STBY REGULATOR SPECIFICATION
H08761	TRINITY CONSOLE V_1P8STBY REGULATOR SPECIFICATION
H08763	TRINITY CONSOLE V_3P3 REGULATOR SPECIFICATION
H08764	TRINITY CONSOLE V_MEM REGULATOR SPECIFICATION
H08765	TRINITY CONSOLE V_EDRAM REGULATOR SPECIFICATION
H08766	TRINITY CONSOLE LINEAR REGULATOR SPECIFICATION
H08767	TRINITY CONSOLE VR ARCHITECTURE
H08758	TRINITY CONSOLE V_CPUCORE REGULATOR SPECIFICATION
	SMC POR FLOWCHART
H08768	TRINITY CONSOLE SYSTEM MANAGEMENT SPECIFICATION
H08773	TRINITY CONSOLE DVD EJECT CAPACITIVE TOUCH SPECIFICATION
H09553	TRINITY CONSOLE WIFI MODULE SPECIFICATION
H08777	TRINITY CONSOLE SPECIFICATION TEMPLATE
H08776	TRINITY CONSOLE FPM REQUIREMENTS DOCUMENT
H08754	TRINITY CONSOLE AUDIO / VIDEO SPECIFICATION
H08757	TRINITY CONSOLE IR SPECIFICATION
H08770	TRINITY CONSOLE TILT SWITCH SPECIFICATION
H08775	TRINITY CONSOLE FPM LED DISPLAY SPECIFICATION
H08774	TRINITY CONSOLE EMI/ESD/SAFETY SPECIFICATION
H08676	CONSOLE USAGE MODEL AND RELIABILITY BUDGET
H08750	TRINITY CONSOLE PLATFORM DESIGN GUIDE
H08778	TRINITY CONSOLE POWER BUDGET
H08780	TRINITY CONSOLE ACOUSTICS MODEL
H09169	TRINITY RJ45 + AUX INTERFACE AND CONNECTOR SPEC
	CONSOLE RELIABILITY SPECIFICATION
H08751	TRINITY CONSOLE FLASH SPECIFICATION
H08769	TRINITY CONSOLE PLL SPECIFICATION
H08755	TRINITY CONSOLE ETHERNET SPECIFICATION
H08945	TRINITY DC CABLE AND CONNECTOR SPEC H08945
H08946	TRINITY PSU SPECS H08946

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	TRINITY_XDK	67/81	G	1.01

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Title:       Basenet Report
Design:      trinity
Date:        Feb 10 16:21:00 2010

Base nets and synonyms for
trinity_lib.TRINITY(@trinity_lib.trinity(
sch_1))
Base Signal
 Location([Zone][dir])

ACCELEROMETER_INT      35C4
ANA_CLK_OE             27D1 22C8
ANA_CLK_OE_R           22C6
ANA_RST_N              27D1 22D7
ANA_V12P0_PWRGD        22D3 27D1 42B8
ANA_VID_INT            23D1 26B2
AUD_CLK                22A1 29C7
AUD_CLK_R              22B4
AUD_L_OUT              33C1 37C7
AUD_RDY_BSBY           26A2 35A3
AUD_RST_N              26B2 33B7
AUD_R_OUT              33B1 37C7
AUD_SPI_CLK            26A6 35A7
AUD_SPI_MISO           35A3 26A6
AUD_SPI_MOSI           26A4 35A7
AUD_SSB                26A1 35A7
AUD_VOUTL              33B4
AUD_VOUTL_R            33B3
AUD_VOUTR              33B4
AUD_VOUTR_R            33B3
AV_MODE0               37C3 27B8 37B3
AV_MODE0_R             27B6
AV_MODE1               37C3 27B8 37C3
AV_MODE1_R             27B6
AV_MODE2               37C3 27B8 37C3
AV_MODE2_R             27B6
BINDSW_N               38A8 27C1
BINDSW_N_R             38A6
BLEEDER_B              42B2
BLEEDER_C1             42B2
BLEEDER_C2             42B2
BLEEDER_V12P0_B1       42B7
BLEEDER_V12P0_B2       42C5
BLEEDER_V12P0_C1       42B6
BLEEDER_V12P0_C2       42B6
BLEEDER_V12P0_LOAD     42B5
BMA_PS_R               35C5
BND_GAP_CAP            23A5
BORONFPMPORT_DN        28C2 38B8
BORONFPMPORT_DP        28C2 38B8
BORONFPM_CLK           27A1 38A8
BORONFPM_DATA          27A1 38A8
BRD_TEMP_N             23C2 38A8 23A8
BRD_TEMP_N_R           38A6
BRD_TEMP_P             23A1 23C2 38A8
BRD_TEMP_P_R           38A6
CAL_TEMP_N             23A1 23A8
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CAL_TEMP_P             23A4
CAPX                   35C4
CAPY                   35C4
CAPZ                   35C4
CORE_HF_BGR_PLL        2A1
CPU_CHECKSTOP_N        2D1 60A2
CPU_CHECKSTOP_N_LED    60B5
CPU_CHECKSTOP_N_LED_B   60A4
CPU_CHECKSTOP_N_LED_C   60B4
CPU_CHECKSTOP_N_R      60A5
CPU_CLK_DN             22D1 2C7
CPU_CLK_DN_R           22C4
CPU_CLK_DN_R2          2C7
CPU_CLK_DP             22D1 2C7
CPU_CLK_DP_R           22C4
CPU_CLK_DP_R2          2C7
CPU_CORE_HF_CLKOUT_DN   6D1
CPU_CORE_HF_CLKOUT_DP   6D1
CPU_DBG0_POST0         3A5
CPU_DBG1_POST1         3A5
CPU_DBG2_POST2         3A5
CPU_DBG3_POST3         3A5
CPU_DBG4_POST4         3A5
CPU_DBG5_POST5         3A5
CPU_DBG6_POST6         3A5
CPU_DBG7_POST7         3A5
CPU_DBG8_RST0          3A5
CPU_DBG9_RST1          3A5
CPU_DBG10_RST2         3A5
CPU_DBG11_GPU_HB_TP    3A5
CPU_DBG12_CPUCLK0_TP   3A5
CPU_DBG13_CPUCLK1_TP   3A5
CPU_DBG14_GPUCLK0_TP   3A5
CPU_DBG15_GPUCLK1_TP   3A5
CPU_DBG_RST_EN         2B7
CPU_DBG_TBCLK0         3D7
CPU_DBG_TBCLK1         3D7
CPU_DLL_SNIF_OUT       3D7
CPU_DLL_SNIF_OUT_TP    3D5
CPU_EXT_CLK_EN         2B7
CPU_LIMIT_BYPASS       2B1
CPU_PLL_BYPASS         2B1
CPU_PSRO0_OUT          2B7
CPU_PWRGD              27A1 2D7
CPU_RST_N              27B1 2D7
CPU_RST_N_2_R          60A6
CPU_RST_V1P1_N         2D1 60A7
CPU_SRVID              2B1 51B8
CPU_TCLK               5C8 60A2 60D8
CPU_TDI                5C8 60A7 60D8
CPU_TDO                5C8 60A7 60D8
CPU_TEMP_N             4B8 61C3 23A8
CPU_TEMP_P             23A1 4B8 61C6
CPU_TINIT              2A6
CPU_TMS                5C8 60A7 60D6
CPU_TRST_N             5C8 60A7
CPU_TRST_N_R           5C8 60D8
```

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CPU_VDDS0_DN           6D8
CPU_VDDS0_DP           6D8
CPU_VDDS1_DN           6D8
CPU_VDDS1_DP           6D8
CPU_VGATE              2B7
CPU_VREG_APS1          2C1 43C7
CPU_VREG_APS2          2C1 43D7
CPU_VREG_APS3          2C1 43D7
CPU_VREG_APS4          2C1 43D7
CPU_VREG_APS5          2C1 43D7
CPU_VREG_APS6          2C1 43D7
DBG_LED0               27A8
DB_TM_CT1              58B1
DB_TM_CT2              58B1
DB_TM_CT3              58B1
DFM_THIEVING_PADS_REQUIREMENT3  38D5
ECB_CLK_BYP            26D6
ECB_CLK_SEL            26D6
EDRAM_PSRO_DOUT        2B7
EDRAM_TEMP_N           4B8 61B3 23A8
EDRAM_TEMP_P           23A1 4B8 61B6
EJECTSW_N              38A8 27C1 35A3
EJECTSW_N_R            38A6
ENET_1.8VEXT           32C5
ENET_ACT_N             32A3
ENET_CLK               22A1 32B8
ENET_CLK_R             22C4
ENET_LINK_N            32A3
ENET_REF_CLK_OUT       32B5
ENET_REXT              32B5
ENET_RSTN_R            32A5
ENET_RST_N             26B2 32A8 32B8
ENET_RX_DN             32A8 38B8
ENET_RX_DP             32A8 38C8
ENET_RX_TERM           38C7
ENET_TX_DN             32A1 38C8
ENET_TX_DP             32A1 38C8
ENET_TX_TERM           38C7
EN_TEST0_N             27A6
EN_TEST1_N             27A6
EXPPORT_PORT1_DN       28B7 39C4
EXPPORT_PORT1_DP       28B7 39C4
EXPPORT_PORT2_DN       28B7 39B4
EXPPORT_PORT2_DP       28B7 39B4
EXPPORT_PORT3_DN       28A7 39A4
EXPPORT_PORT3_DP       28B7 39A4
EXPPORT_RJ45_DN        28B7 38C5
EXPPORT_RJ45_DP        28B7 38C5
EXT_PWR_ON_DBG         59C3
EXT_PWR_ON_N           37D3 59C1 60A2 27C8
37C3 61B2
EXT_PWR_ON_R           27C6
FAN1_FDBK              36B4 23A6
FAN1_FDBK_R            36B6
FAN1_OUT               23A2 36C6
FAN1_Q1_C              36C5
FAN1_Q1_E              36C5
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FAN_OP1_DP             23A7
FAN_PULLUP             36C2
FLSH_ALE               28C2 34B5
FLSH_CE_N              28C2 34B5
FLSH_CLE               28C2 34B5
FLSH_DATA<7..0>        28C7 34C8
FLSH_NC38              34C2
FLSH_READY             34C1 28B7
FLSH_RE_N              28C2 34B5
FLSH_WE_N              28C2 34B5
FLSH_WP_N              28C7 34B5
GAMEPORT1_DN           28B2 39D8
GAMEPORT1_DP           28B2 39D8
GAMEPORT2_DN           28B2 39C8
GAMEPORT2_DP           28B2 39C8
GND_DECOUPLE           32A5
GPU_CLK_DN             22D1 4D8
GPU_CLK_DN_C           4C8
GPU_CLK_DN_R           22C4
GPU_CLK_DN_R2          4D6
GPU_CLK_DP             22D1 4D8
GPU_CLK_DP_C           4D8
GPU_CLK_DP_R           22C4
GPU_CLK_DP_R2          4D6
GPU_DBG_RST_EN         2B7
GPU_HSYNC_OUT          4B1 23C8
GPU_PIX_CLK_1X         4C2 23D8
GPU_RST_DONE           4D2 27C1
GPU_RST_DONE_R         27C4
GPU_RST_N              27A1 4C8
GPU_SROM_CLK_R         60C8 5B1
GPU_SROM_CS            5C4
GPU_SROM_CS_N_R        60C8 5B1
GPU_SROM_EN            5C4
GPU_SROM_SCLK          5C4
GPU_SROM_SI            5B1 60C6
GPU_SROM_SO            5C4
GPU_SROM_SO_R          60C8 5B1
GPU_SROM_WP_N          60C6 5B1
GPU_TEMP_N             4B8 61B3 23A8
GPU_TEMP_P             23A1 4C8 61B6
GPU_TRST_ED_N          5B8 60D6
GPU_TRST_N             5B8 60D6
GPU_VSYNC_OUT          4B1 23C8
HANA_AV_CLK            22B4
HANA_CLK_DRV_RSET1     22C6
HANA_CLK_DRV_RSET2     22C6
HANA_DAC_RSET          23C6
HANA_OP2_DN            23A2 23B6
HANA_OP2_DP            23B6
HANA_OP2_OUT           23A4
HANA_PIX_CLK_2X_DN     22B1 4C8
HANA_PIX_CLK_2X_DN_R   22C4
HANA_PIX_CLK_2X_DP     22B1 4C8
HANA_PIX_CLK_2X_DP_R   22C4
HANA_POR_BYPASS        22D6
HANA_SPDIF_OUT         23A2 37D8 39A8
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HANA_TCLK	60C8 22B8
HANA_TDI	60C8 22B8
HANA_TDO	22B8 60C8
HANA_TMS	60C6 22B8
HANA_TRST	22B8 60C6
HANA_V_12P0_DET	22D6
HANA_V_12P0_DET_R	22D5
HANA_XTAL_BYPASS	22C6
HANA_XTAL_IN	22C6
HANA_XTAL_OUT	22C6
HANA_XTAL_VSS_CAP	22C6
HBEDB_CLK_BYP	26D6
HBEDB_CLK_SEL	26D6
HDD_RX_DN	41C8 29B7
HDD_RX_DN_C	41C6
HDD_RX_DP	41C8 29B7
HDD_RX_DP_C	41C6
HDD_TX_DN	29A1 41D8
HDD_TX_DN_C	41D6
HDD_TX_DP	29A1 41D8
HDD_TX_DP_C	41D6
HDMI_CEC	40B3
HDMI_DDC_CLK	23A2 27B8 37D3 40A8 55D8
HDMI_DDC_DATA	23A2 27C8 37C3 40A8 55D8
HDMI_EXT_SWING	23C4
HDMI_HPD	40A1 23C8
HDMI_HPD_PIN	40A3
HDMI_TX0_DN	23A1 40C8
HDMI_TX0_DP	23B1 40C8
HDMI_TX0_DP_R	23B2
HDMI_TX1_DN	23B1 40C8
HDMI_TX1_DP	23B1 40D8
HDMI_TX1_DP_R	23B2
HDMI_TX2_DN	23B1 40D8
HDMI_TX2_DP	23B1 40D8
HDMI_TX2_DP_R	23B2
HDMI_TXC_DN	23B1 40B8
HDMI_TXC_DP	23C1 40B8
HDMI_TXC_DP_R	23C2
I2S_BCLK	29B1 23C8 33B7
I2S_BCLK_R	29B4
I2S_MCLK	29B1 33B7
I2S_MCLK_R	29B4
I2S_SD	29B1 23B8 33B7
I2S_SD1	23B6
I2S_SD2	23B6
I2S_SD3	23B6
I2S_SD_R	29B4
I2S_WS	29B1 23C8 33B7
I2S_WS_R	29B4
IR_DATA	35B5 27A8
KER_DBG_RXD	59C1 26C7
KER_DBG_TXD	26C1 59C5
KER_DBG_TXD_R	26C3
LVLCNT	37C7

MARGIN_GPUPCIE_CPUPLL_AD0	58C4
MARGIN_GPUPCIE_CPUPLL_AD1	58C4
MARGIN_V3P3_V5P0_AD0	56C6
MARGIN_V3P3_V5P0_AD1	56C6
MARGIN_VCS_AS	57B5
MARGIN_VCS_CONVST	57B4
MARGIN_VMEM_VEDRAM_AD0	55C4
MARGIN_VMEM_VEDRAM_AD1	55C4
MARGIN_VMEM_VREFS_BOT	57A6
MARGIN_VREFS_AD0	57A6
MARGIN_VREFS_AD1	57A6
MARGIN_VREFS_AS	57D4
MARGIN_VREFS_CONVST	57C4
MA_A<11..0>	12C5 14C8 15C8
MA_BA<2..0>	12C5 14C8 15C8
MA_CAS_N	12B5 14B8 15B8
MA_CKE	12B5 14B8 15B8
MA_CLK0_DN	12C5 14D8
MA_CLK0_DP	12C5 14D8
MA_CLK1_DN	12C5 15D8
MA_CLK1_DP	12C5 15D8
MA_CS0_N	12B5 14B8
MA_CS1_N	12B5 14B8 15B8
MA_DM0	12B8 14B4 15B5
MA_DM1	12C8 14B4 15B5
MA_DM2	12C8 14C4 15C5
MA_DM3	12D8 14C4 15C5
MA_DQ0	12B8 14B4 15B5
MA_DQ1	12B8 14B4 15B5
MA_DQ2	12B8 14B4 15B5
MA_DQ3	12B8 14B4 15B5
MA_DQ4	12B6 12B8 14B4 15B5
MA_DQ5	12B8 14B4 15C5
MA_DQ6	12B8 14B4 15C5
MA_DQ7	12B8 14B4 15C5
MA_DQ8	12C8 14B4 15B5
MA_DQ9	12C8 14B4 15B5
MA_DQ10	12C8 14B4 15B5
MA_DQ11	12C8 14B4 15B5
MA_DQ12	12B6 12C8 14B4 15B5
MA_DQ13	12C8 14B4 15B5
MA_DQ14	12C8 14C4 15B5
MA_DQ15	12C8 14C4 15B5
MA_DQ16	12C8 14C4 15C5
MA_DQ17	12C8 14C4 15C5
MA_DQ18	12C8 14C4 15C5
MA_DQ19	12C8 14C4 15C5
MA_DQ20	12C8 14C4 15D5
MA_DQ21	12C8 14C4 15D5
MA_DQ22	12C8 14C4 15D5
MA_DQ23	12C8 14C4 15D5
MA_DQ24	12D8 14C4 15C5
MA_DQ25	12D8 14C4 15C5
MA_DQ26	12D8 14C4 15C5
MA_DQ27	12D8 14C4 15C5
MA_DQ28	12D8 14C4 15C5
MA_DQ29	12D8 14D4 15C5

MA_DQ30	12D8 14D4 15C5
MA_DQ31	12D8 14D4 15C5
MA_RAS_N	12B5 14B8 15B8
MA_RDQS0	14B4 15B5 12B8
MA_RDQS1	14B4 15B5 12C8
MA_RDQS2	14C4 15C5 12C8
MA_RDQS3	14C4 15C5 12D8
MA_VREF0	12A7
MA_WDQS0	12A6 12B8 14B4 15B5
MA_WDQS1	12B6 12C8 14B4 15B5
MA_WDQS2	12C8 14C4 15C5
MA_WDQS3	12D8 14C4 15C5
MA_WE_N	12B5 14B8 15B8
MA_ZQ_BOT	15B5
MA_ZQ_TOP	14B5
MB_A<11..0>	12C1 16C8 17C8
MB_BA<2..0>	12C1 16B8 17B8
MB_CAS_N	12B1 16B8 17B8
MB_CKE	12B1 16B8 17B8
MB_CLK0_DN	12C1 16C8
MB_CLK0_DP	12C1 16D8
MB_CLK1_DN	12C1 17C8
MB_CLK1_DP	12C1 17D8
MB_CS0_N	12B1 16B8
MB_CS1_N	12B1 16B8 17B8
MB_DM0	12B4 16B5 17B5
MB_DM1	12C4 16B5 17B5
MB_DM2	12C4 16C5 17C5
MB_DM3	12D4 16C5 17C5
MB_DQ0	12B4 16B5 17B5
MB_DQ1	12B4 16B5 17B5
MB_DQ2	12B4 16B5 17B5
MB_DQ3	12B4 16B5 17B5
MB_DQ4	12B2 12B4 16B5 17B5
MB_DQ5	12B4 16B5 17B5
MB_DQ6	12B4 16B5 17B5
MB_DQ7	12B4 16B5 17B5
MB_DQ8	12C4 16B5 17B5
MB_DQ9	12C4 16B5 17B5
MB_DQ10	12C4 16B5 17B5
MB_DQ11	12C4 16B5 17B5
MB_DQ12	12B2 12C4 16B5 17B5
MB_DQ13	12C4 16B5 17B5
MB_DQ14	12C4 16B5 17B5
MB_DQ15	12C4 16B5 17B5
MB_DQ16	12C4 16C5 17C5
MB_DQ17	12C4 16C5 17C5
MB_DQ18	12C4 16C5 17C5
MB_DQ19	12C4 16C5 17C5
MB_DQ20	12C4 16C5 17C5
MB_DQ21	12C4 16C5 17C5
MB_DQ22	12C4 16C5 17C5
MB_DQ23	12C4 16C5 17D5
MB_DQ24	12D4 16C5 17C5
MB_DQ25	12D4 16C5 17C5
MB_DQ26	12D4 16C5 17C5
MB_DQ27	12D4 16C5 17C5

MB_DQ28	12D4 16C5 17C5
MB_DQ29	12D4 16C5 17C5
MB_DQ30	12D4 16C5 17C5
MB_DQ31	12D4 16D5 17C5
MB_RAS_N	12B1 16B8 17B8
MB_RDQS0	16B5 17B5 12B4
MB_RDQS1	16B5 17B5 12C4
MB_RDQS2	16C5 17C5 12C4
MB_RDQS3	16C5 17C5 12D4
MB_VREF0	12A3
MB_WDQS0	12A2 12B4 16B5 17B5
MB_WDQS1	12B2 12C4 16B5 17B5
MB_WDQS2	12C4 16C5 17C5
MB_WDQS3	12D4 16C5 17C5
MB_WE_N	12B1 16B8 17B8
MB_ZQ_BOT	17A5
MB_ZQ_TOP	16A5
MC_A<11..0>	13C5 18C8 19C8
MC_BA<2..0>	13C5 18B8 19B8
MC_CAS_N	13B5 18B8 19B8
MC_CKE	13C5 18B8 19B8
MC_CLK0_DN	13C5 18D8
MC_CLK0_DP	13C5 18D8
MC_CLK1_DN	13C5 19D8
MC_CLK1_DP	13D5 19D8
MC_CS0_N	13B5 18B8
MC_CS1_N	13B5 18B8 19B8
MC_DM0	13B8 18B4 19B4
MC_DM1	13C8 18B4 19B4
MC_DM2	13C8 18C4 19C4
MC_DM3	13D8 18C4 19C4
MC_DQ0	13B8 18B4 19B4
MC_DQ1	13B8 18B4 19B4
MC_DQ2	13B8 18B4 19B4
MC_DQ3	13B8 18B4 19B4
MC_DQ4	13B6 13B8 18B4 19B4
MC_DQ5	13B8 18B4 19B4
MC_DQ6	13B8 18B4 19B4
MC_DQ7	13B8 18B4 19C4
MC_DQ8	13C8 18B4 19B4
MC_DQ9	13C8 18B4 19B4
MC_DQ10	13C8 18B4 19B4
MC_DQ11	13C8 18B4 19B4
MC_DQ12	13B6 13C8 18B4 19B4
MC_DQ13	13C8 18B4 19B4
MC_DQ14	13C8 18C4 19B4
MC_DQ15	13C8 18C4 19B4
MC_DQ16	13C8 18C4 19C4
MC_DQ17	13C8 18C4 19C4
MC_DQ18	13C8 18C4 19C4
MC_DQ19	13C8 18C4 19C4
MC_DQ20	13C8 18C4 19C4
MC_DQ21	13C8 18C4 19C4
MC_DQ22	13C8 18C4 19D4
MC_DQ23	13D8 18C4 19D4
MC_DQ24	13D8 18C4 19C4
MC_DQ25	13D8 18C4 19C4

MC_DQ26	13D8 18C4 19C4
MC_DQ27	13D8 18C4 19C4
MC_DQ28	13D8 18C4 19C4
MC_DQ29	13D8 18D4 19C4
MC_DQ30	13D8 18D4 19C4
MC_DQ31	13D8 18D4 19C4
MC_RAS_N	13B5 18B8 19B8
MC_RDQS0	18B4 19B4 13B8
MC_RDQS1	18B4 19B4 13C8
MC_RDQS2	18C4 19C4 13C8
MC_RDQS3	18C4 19C4 13D8
MC_VREF0	13A7
MC_WDQS0	13B5 13B8 18B4 19B4
MC_WDQS1	13B5 13C8 18B4 19B4
MC_WDQS2	13C8 18C4 19C4
MC_WDQS3	13D8 18C4 19C4
MC_WE_N	13B5 18B8 19B8
MC_ZQ_BOT	19B5
MC_ZQ_TOP	18B5
MD_A<11..0>	13C1 20C8 21C8
MD_BA<2..0>	13C1 20C8 21B8
MD_CAS_N	13B1 20B8 21B8
MD_CKE	13C1 20B8 21B8
MD_CLK0_DN	13C1 20D8
MD_CLK0_DP	13C1 20D8
MD_CLK1_DN	13C1 21D8
MD_CLK1_DP	13D1 21D8
MD_CS0_N	13B1 20B8
MD_CS1_N	13B1 20B8 21B8
MD_DM0	13B4 20B4 21B5
MD_DM1	13C4 20B4 21B5
MD_DM2	13C4 20C4 21C5
MD_DM3	13D4 20C4 21C5
MD_DQ0	13B4 20B4 21B5
MD_DQ1	13B4 20B4 21B5
MD_DQ2	13B4 20B4 21B5
MD_DQ3	13B4 20B4 21B5
MD_DQ4	13B4 20B4 21B5
MD_DQ5	13B4 20B4 21B5
MD_DQ6	13B4 20B4 21C5
MD_DQ7	13B4 20B4 21C5
MD_DQ8	13C4 20B4 21B5
MD_DQ9	13C4 20B4 21B5
MD_DQ10	13C4 20B4 21B5
MD_DQ11	13C4 20B4 21B5
MD_DQ12	13B2 13C4 20C4 21B5
MD_DQ13	13C4 20C4 21B5
MD_DQ14	13C4 20C4 21B5
MD_DQ15	13C4 20C4 21B5
MD_DQ16	13C4 20C4 21C5
MD_DQ17	13C4 20C4 21C5
MD_DQ18	13C4 20C4 21C5
MD_DQ19	13C4 20C4 21C5
MD_DQ20	13C4 20C4 21C5
MD_DQ21	13C4 20C4 21D5
MD_DQ22	13C4 20C4 21D5
MD_DQ23	13D4 20C4 21D5
MD_DQ24	13D4 20C4 21C5
MD_DQ25	13D4 20C4 21C5
MD_DQ26	13D4 20C4 21C5
MD_DQ27	13D4 20D4 21C5
MD_DQ28	13D4 20D4 21C5
MD_DQ29	13D4 20D4 21C5
MD_DQ30	13D4 20D4 21C5
MD_DQ31	13D4 20D4 21C5
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MD_VREF0	13A3
MD_WDQS0	13B4 20B4 21B5
MD_WDQS1	13B2 13C4 20B4 21B5
MD_WDQS2	13C4 20C4 21C5
MD_WDQS3	13D4 20C4 21C5
MD_WE_N	13B1 20B8 21B8
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MEM_A_VREF0	15A6 14B8 15B8
MEM_A_VREF1	14A6 14B8 15B8
MEM_B_VREF0	17A6 16B8 17B8
MEM_B_VREF1	16A6 16B8 17B8
MEM_CALA	4A6
MEM_CALB	4A6
MEM_C_VREF0	19A6 18B8 19B8
MEM_C_VREF1	18A6 18B8 19B8
MEM_D_VREF0	21A6 20B8 21B8
MEM_D_VREF1	20A6 20B8 21B8
MEM_RST	4B1 14D8 15D8 16C8 17C8 18D8 19C8 20D8 21D8
MEM_SCAN_BOT_EN	4A1 15B8 17B8 19B8 21B8
MEM_SCAN_BOT_EN_N	4A4
MEM_SCAN_EN	4A1 14B8 15B8 16B8 17B8 18B8 19B8 20B8 21B8
MEM_SCAN_TOP_EN	4A1 14B8 16B8 18B8 20B8
MEM_VREFS	57A6 57D4
MEM_VREFS_R	57A6
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MII_CRS	32C1 29C7
MII_MDC_CLK_OUT	29D1 32B8
MII_MDC_CLK_OUT_R	29D4
MII_MDIO	29C8 32B8
MII_RXD0	32A1 29C7
MII_RXD1	32A1 29C7
MII_RXD2	32A1 29C7
MII_RXD3	32B1 29C7
MII_RXDV	32C1 29C7
MII_RXER	32B1 29C7
MII_RX_CLK	32B1 29D7
MII_RX_CLK_R	29D6
MII_TXD0	29C1 32A8
MII_TXD1	29C1 32A8
MII_TXD2	29C1 32A8
MII_TXD3	29C1 32B8
MII_TXEN	29C1 32B8
MII_TX_CLK	32B1 29D7
MII_TX_CLK_R	29D6
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ODD_RX_DP	41A8 29B7
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PEX_GPU_SB_L0_DN_C	4C4
PEX_GPU_SB_L0_DP	4C2 26C7
PEX_GPU_SB_L0_DP_C	4C4
PEX_GPU_SB_L1_DN	4C2 26C7
PEX_GPU_SB_L1_DN_C	4C4
PEX_GPU_SB_L1_DP	4D2 26C7
PEX_GPU_SB_L1_DP_C	4D4
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PEX_SB_GPU_L0_DN_C	26C3
PEX_SB_GPU_L0_DP	26D1 4C8
PEX_SB_GPU_L0_DP_C	26D3
PEX_SB_GPU_L1_DN	26D1 4C8
PEX_SB_GPU_L1_DN_C	26D3
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SB_GPIO_RESERVED17	26B3
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SB_GPIO_RESERVED19	26B3
SB_GPIO_RESERVED20	26B3
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SB_TDI	60B8 26A6
SB_TDO	26A6 60B8
SB_TMS	60B6 26A6
SB_TRST	26A6 60B6
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SMC_PWM1	27A1 36A6
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VREG_CPU_BST2	45D5
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VREG_CPU_DRVL1	45A5
VREG_CPU_DRVL2	45C5
VREG_CPU_DRV_EN	44C1 45C8
VREG_CPU_EN	27C1 44D8
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VREG_CPU_PHASE1_R	44C4
VREG_CPU_PHASE2	45C1 44C8
VREG_CPU_PHASE2_R	44C4
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VREG_CPU_SW2_R	45C3
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VREG_V3P3_COMP	48A8
VREG_V3P3_COMP_C	48A7
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VREG_V3P3_DL	48B5
VREG_V3P3_EN	27D1 48C8
VREG_V3P3_FB	48B1 56D1
VREG_V3P3_FB_A3	56D4
VREG_V3P3_FB_MID	48A1 56C1
VREG_V3P3_FB_MID_R	56C4
VREG_V3P3_FB_R	56A4
VREG_V3P3_ILIM	48B5
VREG_V3P3_IOUT	56A5
VREG_V3P3_ISENSE_N	48C1 56A7
VREG_V3P3_ISENSE_P	48C1 56A7
VREG_V3P3_PGND	48B5
VREG_V3P3_PWRGD	48D1 27A8
VREG_V3P3_RAMP	48D5
VREG_V3P3_RSENSE	48C3
VREG_V3P3_SS	48A7
VREG_V3P3_SW	48C5
VREG_V3P3_SW_S	48C3
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VREG_V3P3_V5P0_VDL	47D7
VREG_V5P0_BST	47C5
VREG_V5P0_CF2	56A6
VREG_V5P0_COMP	47A8
VREG_V5P0_COMP_C	47A8
VREG_V5P0_DH	47C5
VREG_V5P0_DL	47B5
VREG_V5P0_EN	27C1 47B8
VREG_V5P0_EN_R	47B7
VREG_V5P0_FB	47A1 56D8
VREG_V5P0_FB_A1	56D6
VREG_V5P0_FB_MID	47A1 56C8
VREG_V5P0_FB_MID_R	56C6
VREG_V5P0_FB_R	56A4
VREG_V5P0_ILIM	47B5
VREG_V5P0_IOUT	56B5
VREG_V5P0_ISENSE_N	47C1 56B7
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VREG_V5P0_RAMP	47C5
VREG_V5P0_RSENSE	47C3
VREG_V5P0_SEL	27C1 46C7
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VREG_V5P0_SEL_B2	46C5
VREG_V5P0_SEL_C	46C6
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VREG_V5P0_SS	47A7
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VREG_V12P0_ISENSE_N_R	58C6
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VREG_VCS_FB	51A1 57A2 57C8
VREG_VCS_FB_MID	51A1 57A2
VREG_VCS_FB_MID_R	57A4
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VREG_VEDRAM_FB_MID_R	55C3
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VREG_VMEM_EN	27C1 50C8
VREG_VMEM_FB	50A1 55A7 55D6
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VREG_VMEM_RSENSE	50C3
VREG_VMEM_SS	50A7
VREG_VMEM_SW	50B5
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WSS_CNTL0	26B2 37C8
WSS_CNTL1	26B2 37C8
WSS_CNTL_B	37C7
WSS_CNTL_E	37C7
WSS_CNTL_OUT	37C6
WSS_CNTL_OUT_R	37C7
XUSB_CLK_BYP	26D6
XUSB_CLK_SEL	26D6

Title: Cref Part Report
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C1A1	CAPN_805	[39B6]
C1A2	CAPN_805	[39B2]
C1A3	CAP_P_RDL	[39B3]
C1A6	CAPN_402	[39B2]
C1A7	CAPN_402	[39B6]
C1A8	CAPN_402	[39D2]
C1A9	CAPN_402	[39C2]
C1A10	CAPN_402	[54D2]
C1B1	CAPN_402	[41A7]
C1B2	CAPN_402	[41A7]
C1B3	CAPN_402	[41A7]
C1B4	CAPN_402	[41B7]
C1B7	CAPN_402	[41C7]
C1B8	CAPN_402	[41C7]
C1B9	CAP_P_RDL	[39D3]
C1B10	CAPN_402	[41D7]
C1B11	CAPN_402	[41D7]
C1B12	CAPN_1206	[46C4]
C1C1	CAP_P_RDL	[52C6]
C1C2	CAPN_603	[52C6]
C1C3	CAPN_603	[52C7]
C1D1	CAPN_805	[41C3]
C1D2	CAPN_402	[41C2]
C1E1	CAPN_603	[47C8]
C1E2	CAPN_603	[47C8]
C1E3	CAPN_402	[48A7]
C1E4	CAPN_402	[48A8]
C1E5	CAPN_402	[48A7]
C1F1	CAPN_603	[48C5]
C1F2	CAPN_402	[56A6]
C1F3	CAPN_805	[48C1]
C1F6	CAPN_805	[48C2]
C1F9	CAPN_805	[48C2]
C1F10	CAPN_402	[56B4]
C1F11	CAPN_402	[56B2]
C1G2	CAPN_805	[48C1]
C1G7	CAPN_402	[58B3]
C1G8	CAPN_402	[58A3]
C1G9	CAPN_402	[58A3]
C1G10	CAPN_402	[58A3]
C1G11	CAPN_402	[58B3]
C1G12	CAPN_402	[58B4]
C1G13	CAPN_805	[58B3]
C1N1	CAPN_805	[39C2]
C1N3	CAPN_402	[46C5]
C1N4	CAPN_402	[46C4]
C1N5	CAPN_805	[39D2]
C1P1	CAPN_402	[54D2]
C1R1	CAPN_402	[54B5]
C1T2	CAPN_805	[34C5]
C1T3	CAPN_402	[34C5]
C1T4	CAPN_402	[54D2]
C1U1	CAPN_1206	[48C3]
C1U2	CAPN_402	[56B6]
C1U3	CAPN_402	[54D3]
C2A1	CAPN_402	[40A7]
C2A2	CAPN_402	[37D6]
C2A3	CAPN_402	[37D8]
C2A5	CAPN_805	[38D5]
C2A6	CAPN_402	[38C6]
C2A7	CAPN_402	[38C6]
C2A8	CAPN_805	[37D6]
C2A9	CAP_P_RDL	[39C3]
C2A10	CAP_P_RDL	[38D6]
C2A11	CAPN_402	[38D6]
C2A12	CAPN_805	[38D5]
C2A13	CAP_P_RDL	[38D6]
C2A14	CAPN_402	[38D6]
C2A15	CAPN_402	[54D1]
C2B2	CAP_P_RDL	[46C4]
C2B3	CAPN_402	[26B1]
C2C2	CAPN_402	[37B1]
C2C3	CAPN_402	[59C7]
C2C4	CAPN_402	[59D3]
C2C5	CAPN_402	[59D2]
C2C6	CAPN_603	[59D2]
C2C7	CAPN_402	[26B1]
C2C8	CAPN_805	[32C8]
C2C9	CAPN_805	[32C8]
C2C10	CAPN_805	[32C6]
C2D1	CAPN_603	[32C5]
C2D2	CAPN_402	[32C5]
C2D3	CAPN_402	[32C8]
C2D4	CAPN_603	[32A5]
C2D5	CAPN_603	[32C6]
C2E1	CAPN_402	[29A6]
C2E2	CAPN_603	[47C8]
C2E3	CAPN_402	[47A8]
C2E4	CAPN_402	[47A8]
C2E5	CAPN_402	[47A7]
C2E6	CAPN_402	[47B7]
C2E7	CAPN_402	[47B7]
C2E8	CAP_P_TH	[47D8]
C2F1	CAPN_603	[47C5]
C2F2	CAPN_402	[56B4]
C2F3	CAPN_1206	[47D4]
C2F4	CAPN_402	[56D6]
C2F6	CAPN_402	[56A6]
C2F10	CAPN_1206	[47D3]
C2G1	CAPN_805	[47B2]
C2G2	CAPN_805	[47B2]
C2G5	CAP_P_TH	[47B1]
C2M1	CAPN_402	[37B2]
C2M2	CAPN_402	[37B2]
C2M3	CAPN_402	[38B4]
C2M4	CAPN_402	[38B3]
C2M5	CAPN_805	[38B4]
C2M6	CAPN_805	[38B5]
C2N3	CAPN_402	[54B5]
C2N4	CAPN_402	[35D5]
C2N5	CAPN_402	[35D6]
C2P1	CAPN_402	[54B4]
C2P2	CAPN_805	[32C5]
C2P3	CAPN_805	[32C6]
C2P4	CAPN_402	[32C7]
C2P5	CAPN_402	[32C7]
C2R3	CAPN_603	[32A6]
C2R5	CAPN_402	[32B5]
C2R6	CAPN_805	[32C6]
C2R7	CAPN_805	[31A2]
C2R8	CAPN_402	[23D6]
C2R9	CAPN_402	[31B2]
C2R10	CAPN_805	[31B8]
C2R11	CAPN_402	[31B3]
C2R12	CAPN_402	[31B3]
C2R13	CAPN_402	[31B2]
C2R14	CAPN_402	[31D1]
C2R15	CAPN_603	[31B7]
C2R16	CAPN_402	[31B7]
C2R17	CAPN_603	[31C2]
C2R18	CAPN_402	[31B7]
C2R19	CAPN_603	[31B7]
C2R20	CAPN_402	[31D2]
C2R21	CAPN_402	[54B4]
C2R22	CAPN_402	[54B7]
C2T1	CAPN_805	[31A7]
C2T2	CAPN_402	[31A6]
C2T3	CAPN_402	[31A6]
C2T4	CAPN_402	[31D1]
C2T5	CAPN_402	[31A7]
C2T6	CAPN_402	[30C2]
C2T7	CAPN_805	[31B8]
C2T8	CAPN_603	[31A7]
C2T9	CAPN_603	[31C2]
C2T10	CAPN_402	[30C6]
C2T11	CAPN_402	[30C6]
C2T12	CAPN_805	[31C2]
C2T13	CAPN_402	[28A6]
C2T14	CAPN_402	[30C7]
C2T15	CAPN_805	[30C7]
C2T16	CAPN_805	[30C8]
C2T18	CAPN_402	[34C4]
C2T19	CAPN_402	[54B6]
C2U1	CAPN_402	[54B7]
C2V1	CAPN_805	[47B2]
C2V2	CAPN_402	[54C6]
C2V4	CAPN_805	[47B2]
C2V5	CAPN_805	[47B3]
C3A1	CAPN_402	[37B6]
C3A2	CAPN_402	[37B2]
C3A3	CAPN_402	[33B3]
C3A4	CAPN_402	[33B3]
C3A5	CAPN_402	[33D3]
C3A6	CAPN_603	[33D3]
C3A7	CAPN_402	[33D6]
C3A8	CAPN_402	[33C3]
C3A9	CAPN_603	[33B3]
C3A10	CAPN_402	[33A3]
C3B1	CAPN_402	[23B2]
C3B2	CAPN_402	[23B2]
C3B3	CAPN_402	[23B2]
C3B4	CAPN_402	[23C2]
C3B5	CAPN_402	[22D8]
C3B6	CAPN_402	[22D8]
C3B7	CAPN_402	[22A2]
C3B8	CAPN_402	[22A1]
C3B9	CAPN_402	[22B1]
C3B10	CAPN_402	[22A1]
C3B11	CAPN_603	[33D6]
C3B12	CAPN_402	[33D6]
C3C1	CAPN_805	[24A7]
C3C2	CAPN_805	[24A7]
C3C3	CAPN_402	[54C1]
C3D1	CAPN_603	[59D3]
C3D2	CAPN_402	[26D2]
C3E1	CAPN_402	[26D2]
C3E2	CAPN_402	[26C2]
C3E3	CAPN_402	[26D2]
C3E4	CAPN_402	[58D4]
C3E5	CAPN_402	[58B7]
C3E6	CAPN_402	[54C7]
C3E7	CAPN_402	[54C2]
C3F1	CAPN_1206	[49D3]
C3F2	CAPN_402	[49A7]
C3F3	CAPN_402	[49A8]
C3F4	CAPN_402	[49A7]
C3F5	CAPN_603	[49C5]
C3F6	CAPN_402	[55A6]
C3F7	CAPN_1206	[49D3]
C3F8	CAP_P_TH	[49D8]
C3G1	CAPN_603	[49C8]
C3G2	CAPN_402	[55B6]
C3G3	CAPN_603	[49C8]
C3G4	CAPN_402	[55A6]
C3G5	CAPN_402	[55D4]
C3G6	CAPN_402	[50A7]
C3G7	CAPN_402	[50A8]
C3G8	CAPN_402	[50A7]
C3G9	CAPN_603	[50C5]
C3G10	CAPN_402	[55B3]
C3G11	CAPN_402	[55B4]
C3G12	CAPN_402	[54C5]
C3G13	CAPN_1206	[35A7]
C3G14	CAPN_1206	[35A6]
C3M1	CAPN_402	[37B6]
C3M2	CAPN_805	[33A3]
C3M3	CAPN_805	[33A3]
C3M4	CAPN_603	[33C3]
C3M5	CAPN_402	[54D7]
C3M6	CAPN_603	[33C3]
C3N1	CAPN_805	[25C8]
C3N2	CAPN_805	[25B8]
C3N3	CAPN_805	[25C7]

C3N4	CAPN_805	[25B7]
C3N5	CAPN_805	[24A7]
C3N6	CAPN_402	[25C7]
C3N7	CAPN_402	[25C7]
C3N8	CAPN_402	[25C8]
C3N9	CAPN_402	[25B7]
C3N10	CAPN_402	[25C6]
C3N11	CAPN_402	[25C6]
C3N12	CAPN_402	[25C8]
C3N13	CAPN_805	[24C7]
C3N14	CAPN_402	[24A4]
C3N15	CAPN_402	[24A6]
C3N16	CAPN_402	[24A6]
C3N17	CAPN_402	[24B6]
C3N18	CAPN_402	[25C1]
C3N19	CAPN_402	[25C2]
C3N20	CAPN_402	[24C6]
C3N21	CAPN_402	[24A5]
C3N22	CAPN_805	[24A8]
C3N23	CAPN_805	[24C6]
C3N24	CAPN_402	[24A5]
C3N25	CAPN_402	[24A3]
C3N26	CAPN_402	[24A5]
C3N27	CAPN_402	[24C5]
C3N28	CAPN_402	[24A3]
C3N29	CAPN_402	[25C3]
C3N30	CAPN_402	[25C3]
C3N31	CAPN_402	[25C2]
C3N32	CAPN_402	[24A4]
C3N33	CAPN_402	[25C3]
C3N34	CAPN_805	[24A6]
C3N35	CAPN_402	[24A1]
C3N36	CAPN_805	[24C6]
C3N37	CAPN_805	[24C7]
C3N38	CAPN_402	[24C6]
C3N39	CAPN_402	[25C2]
C3N40	CAPN_402	[54D7]
C3N41	CAPN_603	[33C3]
C3P1	CAPN_402	[25D3]
C3P2	CAPN_402	[24A4]
C3P3	CAPN_805	[25D2]
C3P4	CAPN_805	[25D1]
C3P5	CAPN_402	[24A5]
C3P6	CAPN_402	[24A3]
C3P7	CAPN_402	[24A2]
C3P8	CAPN_402	[24A2]
C3P9	CAPN_402	[24A2]
C3P10	CAPN_402	[54B3]
C3R1	CAPN_402	[30A2]
C3R2	CAPN_603	[27D6]
C3R3	CAPN_603	[31A2]
C3R4	CAPN_402	[30A2]
C3R5	CAPN_805	[30A8]
C3R6	CAPN_402	[31B2]
C3R7	CAPN_402	[31D3]
C3R8	CAPN_402	[31D2]
C3R9	CAPN_402	[26C7]

C3R10	CAPN_402	[31D3]
C3R11	CAPN_402	[31D3]
C3R12	CAPN_402	[30C2]
C3R13	CAPN_402	[30C1]
C3R14	CAPN_402	[26C8]
C3R15	CAPN_402	[31D7]
C3R16	CAPN_603	[31D7]
C3R17	CAPN_402	[31D1]
C3R18	CAPN_402	[31D2]
C3R19	CAPN_402	[54B1]
C3R20	CAPN_402	[54B4]
C3R21	CAPN_402	[54C2]
C3T1	CAPN_402	[31C6]
C3T2	CAPN_805	[31D8]
C3T3	CAPN_402	[31C7]
C3T4	CAPN_603	[30A7]
C3T5	CAPN_805	[31C7]
C3T6	CAPN_402	[30C2]
C3T7	CAPN_402	[30A7]
C3T8	CAPN_402	[23D7]
C3T9	CAPN_402	[30A6]
C3T10	CAPN_402	[30C7]
C3T11	CAPN_402	[30D6]
C3T12	CAPN_402	[30A7]
C3T13	CAPN_603	[30C7]
C3T14	CAPN_603	[30D7]
C3T15	CAPN_603	[30A7]
C3T16	CAPN_402	[23D8]
C3T17	CAPN_805	[30D8]
C3T18	CAPN_402	[23D8]
C3T19	CAPN_805	[30A8]
C3T20	CAPN_402	[54B6]
C3T21	CAPN_402	[54B6]
C3T23	CAPN_402	[54C6]
C3T24	CAPN_402	[54C3]
C3U1	CAPN_402	[54B7]
C3U2	CAPN_402	[58B6]
C3U3	CAPN_402	[58B7]
C3U4	CAPN_402	[54C6]
C3V1	CAPN_603	[49C8]
C3V2	CAPN_402	[55B4]
C3V3	CAPN_402	[54C5]
C3V4	CAPN_402	[35A6]
C3V5	CAPN_402	[35A6]
C3V6	CAPN_402	[35A5]
C4A1	CAPN_402	[39A7]
C4A3	CAPN_402	[37A7]
C4A4	CAPN_402	[37A4]
C4A5	CAPN_402	[37A4]
C4A6	CAPN_402	[37A7]
C4A7	CAPN_402	[37A4]
C4A8	CAPN_402	[37A4]
C4A9	CAPN_402	[37A7]
C4A10	CAPN_402	[37A7]
C4A11	CAPN_402	[41A2]
C4A12	CAPN_402	[59D4]
C4A14	CAPN_805	[41B4]

C4B1	CAPN_402	[57B7]
C4B2	CAPN_402	[22D6]
C4B3	CAPN_402	[23A6]
C4B4	CAPN_805	[51C5]
C4B5	CAPN_603	[51A6]
C4B6	CAPN_402	[51A7]
C4B7	CAPN_402	[51B6]
C4B10	CAPN_805	[41D2]
C4B11	CAPN_805	[51C5]
C4B12	CAPN_805	[51C4]
C4B13	CAPN_402	[51A4]
C4B14	CAPN_1206	[51C5]
C4C1	CAPN_402	[23A2]
C4C2	CAPN_402	[4B6]
C4C3	CAPN_402	[60A6]
C4C4	CAPN_402	[60A5]
C4C5	CAPN_402	[51B6]
C4C6	CAPN_402	[4B6]
C4C7	CAPN_402	[4B6]
C4C8	CAPN_402	[5B7]
C4E1	CAPN_402	[4D6]
C4E2	CAPN_402	[4D6]
C4E3	CAP_P_RDL	[49C2]
C4E6	CAP_P_RDL	[49C2]
C4E9	CAPN_805	[52A6]
C4E10	CAPN_603	[52B8]
C4E11	CAPN_603	[52C4]
C4E12	CAPN_805	[52C2]
C4E13	CAPN_402	[52C3]
C4F7	CAP_P_RDL	[49C1]
C4F8	CAPN_402	[52A7]
C4G1	CAPN_402	[54B2]
C4M1	CAPN_402	[54B7]
C4N1	CAPN_402	[57B5]
C4N2	CAPN_402	[54B2]
C4N3	CAPN_402	[54B5]
C4N4	CAPN_402	[57D4]
C4N5	CAPN_402	[54B5]
C4N6	CAPN_402	[54C7]
C4N7	CAPN_603	[51C6]
C4N8	CAPN_402	[54B4]
C4N9	CAPN_603	[51C6]
C4N10	CAPN_805	[51C4]
C4P1	CAPN_402	[36C6]
C4P2	CAPN_402	[23A6]
C4P3	CAPN_402	[54C7]
C4R1	CAPN_603	[52A2]
C4R2	CAPN_603	[52A4]
C4R3	CAPN_402	[52A2]
C4R4	CAPN_402	[5C1]
C4T1	CAPN_603	[2D5]
C4T3	CAPN_805	[9A3]
C4T4	CAPN_805	[9A3]
C4T7	CAPN_1206	[49B1]
C4U4	CAP_P_SM	[50B2]
C4V1	CAPN_402	[54B2]
C5A1	CAPN_402	[53B4]

C5A2	CAPN_805	[53B3]
C5A3	CAPN_603	[53B3]
C5A6	CAPN_805	[41B5]
C5A7	CAPN_402	[41B4]
C5A8	CAPN_603	[41B5]
C5A9	CAPN_805	[53C8]
C5A11	CAPN_805	[41B5]
C5A12	CAPN_603	[36C3]
C5A14	CAPN_402	[41B4]
C5A15	CAPN_603	[36C3]
C5B1	CAPN_402	[53C4]
C5B2	CAPN_805	[53C3]
C5B5	CAPN_402	[57C5]
C5B6	CAPN_603	[53C3]
C5B7	CAPN_805	[53C3]
C5B8	CAPN_402	[57B7]
C5B10	CAPN_603	[45A7]
C5B15	CAPN_402	[57C7]
C5B16	CAPN_805	[53C7]
C5B17	CAPN_402	[41D2]
C5B18	CAPN_805	[53C7]
C5B19	CAPN_805	[51C2]
C5B20	CAPN_805	[51C3]
C5B21	CAP_P_TH	[51C3]
C5C1	CAPN_805	[45A2]
C5C2	CAP_P_RDL	[51B1]
C5C3	CAP_P_RDL	[43A5]
C5C6	CAPN_805	[51B1]
C5D1	CAPN_805	[9D1]
C5D2	CAPN_805	[9B7]
C5D3	CAPN_805	[9C7]
C5D4	CAPN_805	[9C1]
C5D5	CAPN_805	[9C5]
C5D6	CAPN_805	[9C5]
C5D7	CAPN_805	[9C5]
C5D8	CAPN_805	[9C7]
C5D9	CAPN_805	[9B5]
C5D10	CAPN_805	[9B5]
C5D11	CAPN_805	[9B5]
C5D12	CAPN_805	[9B8]
C5D13	CAPN_805	[9D7]
C5D14	CAPN_805	[9C7]
C5E1	CAPN_402	[4C3]
C5E2	CAPN_402	[4D3]
C5E3	CAPN_402	[4C3]
C5E4	CAPN_402	[4C3]
C5E5	CAPN_805	[9C3]
C5E6	CAPN_805	[9D3]
C5E7	CAPN_805	[9C3]
C5E8	CAPN_805	[9B3]
C5E9	CAPN_805	[9B3]
C5E10	CAPN_1206	[49B1]
C5E11	CAPN_1206	[49B2]
C5F1	CAPN_402	[19A7]
C5F2	CAPN_402	[20A2]
C5F3	CAPN_402	[20A2]
C5F4	CAPN_402	[20A3]

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C5F5	CAPN_402	[20A1]
C5F6	CAPN_402	[20A1]
C5F7	CAPN_402	[20A3]
C5F8	CAPN_402	[20A1]
C5F9	CAPN_402	[20A3]
C5F10	CAPN_805	[18A4]
C5G1	CAP_P_RDL	[38B6]
C5G2	CAPN_402	[38B5]
C5G3	CAPN_402	[38A5]
C5G4	CAPN_402	[38A6]
C5G5	CAPN_402	[38A6]
C5G6	CAPN_805	[35B6]
C5G7	CAPN_402	[35B6]
C5G8	CAPN_402	[54C4]
C5M5	CAPN_603	[53A6]
C5N5	CAPN_805	[45B5]
C5N6	CAPN_603	[45A5]
C5N7	CAPN_402	[57D5]
C5N8	CAPN_402	[57D7]
C5N9	CAPN_603	[53C6]
C5N10	CAPN_805	[51C4]
C5N11	CAPN_805	[51C4]
C5P1	CAPN_805	[51B2]
C5R1	CAPN_805	[9C1]
C5R2	CAPN_805	[9A6]
C5R3	CAPN_805	[9B6]
C5R4	CAPN_805	[9C1]
C5R5	CAPN_805	[9B7]
C5R6	CAPN_805	[9B7]
C5R7	CAPN_805	[9C6]
C5R8	CAPN_805	[9D6]
C5R9	CAPN_805	[9D5]
C5R10	CAPN_805	[9C8]
C5R11	CAPN_603	[2D5]
C5R12	CAPN_805	[9B8]
C5R13	CAPN_805	[9A7]
C5R14	CAPN_805	[6D5]
C5R15	CAPN_805	[9C8]
C5R16	CAPN_805	[9B7]
C5R17	CAPN_805	[6C5]
C5R18	CAPN_805	[9B5]
C5R19	CAPN_402	[11A6]
C5R20	CAPN_402	[11B6]
C5R21	CAPN_402	[11C3]
C5R22	CAPN_402	[11A6]
C5R23	CAPN_402	[11A6]
C5R24	CAPN_402	[11B5]
C5R25	CAPN_402	[11D6]
C5R26	CAPN_402	[10D5]
C5R27	CAPN_402	[10C3]
C5R28	CAPN_402	[10C3]
C5R29	CAPN_402	[11A5]
C5R30	CAPN_402	[11D4]
C5R31	CAPN_805	[6A6]
C5R32	CAPN_402	[10B5]
C5R33	CAPN_402	[10C6]
C5R34	CAPN_402	[11B3]

C5R35	CAPN_402	[9D2]
C5R36	CAPN_402	[10A5]
C5R37	CAPN_402	[10C4]
C5R38	CAPN_402	[10B6]
C5R39	CAPN_402	[10C6]
C5R40	CAPN_402	[10C6]
C5R41	CAPN_402	[11B4]
C5R42	CAPN_805	[6B6]
C5R43	CAPN_402	[9C2]
C5R44	CAPN_402	[11B5]
C5R45	CAPN_402	[10A4]
C5R46	CAPN_402	[10B4]
C5R47	CAPN_402	[11B5]
C5R48	CAPN_402	[11B5]
C5R49	CAPN_402	[10C4]
C5R50	CAPN_402	[9B2]
C5R51	CAPN_402	[10B3]
C5R52	CAPN_402	[11C4]
C5R53	CAPN_402	[11C5]
C5R54	CAPN_805	[6B6]
C5R55	CAPN_402	[10B3]
C5R56	CAPN_402	[11A5]
C5R57	CAPN_402	[10B4]
C5R58	CAPN_402	[9C2]
C5R59	CAPN_402	[10C3]
C5R60	CAPN_402	[10C5]
C5R61	CAPN_402	[10C5]
C5R62	CAPN_402	[10B3]
C5R63	CAPN_402	[10C3]
C5R64	CAPN_402	[10B4]
C5T1	CAPN_402	[9B2]
C5T2	CAPN_402	[11B3]
C5T3	CAPN_402	[11C3]
C5T4	CAPN_805	[6A5]
C5T5	CAPN_402	[11B3]
C5T6	CAPN_402	[6A4]
C5T7	CAPN_402	[9C2]
C5T8	CAPN_402	[10C4]
C5T9	CAPN_805	[6C5]
C5T10	CAPN_402	[10D4]
C5T11	CAPN_402	[10A5]
C5T12	CAPN_402	[10D6]
C5T13	CAPN_805	[6B5]
C5T14	CAPN_402	[11D3]
C5T15	CAPN_402	[11C4]
C5T16	CAPN_402	[11C3]
C5T17	CAPN_402	[10D4]
C5T18	CAPN_402	[11A4]
C5T19	CAPN_402	[11C6]
C5T20	CAPN_402	[9B4]
C5T21	CAPN_402	[9A4]
C5T22	CAPN_402	[9B4]
C5T23	CAPN_402	[9B4]
C5T24	CAPN_402	[9C4]
C5T25	CAPN_402	[9A4]
C5T26	CAPN_402	[9D4]
C5T27	CAPN_402	[9B4]

C5T28	CAPN_402	[11C4]
C5T29	CAPN_402	[11B5]
C5T30	CAPN_402	[11B5]
C5T31	CAPN_402	[9C4]
C5T32	CAPN_402	[9C4]
C5T33	CAPN_805	[9A5]
C5T34	CAPN_805	[9B3]
C5T35	CAPN_805	[9C3]
C5T36	CAPN_402	[4A5]
C5T37	CAPN_402	[13A6]
C5T38	CAPN_402	[13A1]
C5T39	CAPN_402	[13A2]
C5T41	CAPN_402	[13A5]
C5T42	CAPN_402	[13A2]
C5T43	CAPN_805	[9B3]
C5T44	CAPN_402	[13A1]
C5T45	CAPN_402	[13A2]
C5T46	CAPN_402	[13A5]
C5T47	CAPN_402	[13A5]
C5T48	CAPN_402	[13A2]
C5T49	CAPN_402	[13A5]
C5T50	CAPN_402	[13A6]
C5T52	CAPN_1206	[49B2]
C5U1	CAPN_402	[18A5]
C5U2	CAPN_805	[13A6]
C5U3	CAPN_402	[21A2]
C5U4	CAPN_402	[21A3]
C5U5	CAPN_402	[21A3]
C5U6	CAPN_402	[21A2]
C5U7	CAPN_402	[21A2]
C5U8	CAPN_402	[21A3]
C5U9	CAPN_402	[18A7]
C5U10	CAPN_402	[21A1]
C5U11	CAPN_402	[21A1]
C5U12	CAPN_402	[21A6]
C6A1	CAPN_402	[38A3]
C6A2	CAPN_402	[38A2]
C6A3	CAPN_402	[38A2]
C6A4	CAP_P_RDL	[38A3]
C6A5	CAP_P_RDL	[38A3]
C6A6	CAPN_603	[58C6]
C6A7	CAP_P_RDL	[36C3]
C6B1	CAP_P_TH	[43B5]
C6B2	CAPN_1206	[45A3]
C6B3	CAPN_1206	[43B4]
C6B4	CAPN_603	[45D7]
C6B5	CAPN_1206	[43B4]
C6C1	CAP_P_RDL	[43A6]
C6C2	CAP_P_RDL	[43A5]
C6C3	CAP_P_RDL	[43A6]
C6D1	CAPN_805	[9A8]
C6D2	CAPN_805	[9A7]
C6D3	CAPN_805	[9C6]
C6D4	CAPN_805	[9C6]
C6D5	CAPN_805	[9B8]
C6D6	CAPN_805	[9A6]
C6F1	CAPN_402	[18A2]

C6F2	CAPN_402	[18A2]
C6F3	CAPN_402	[21A7]
C6F4	CAPN_402	[18A3]
C6F5	CAPN_402	[18A2]
C6F6	CAPN_402	[21A5]
C6F7	CAPN_402	[18A1]
C6F8	CAPN_402	[18A3]
C6F9	CAPN_402	[18A1]
C6F10	CAPN_402	[18A3]
C6F11	CAPN_805	[20A4]
C6G1	CAP_P_RDL	[39D7]
C6G2	CAPN_402	[39D7]
C6G3	CAPN_805	[39D7]
C6M5	CAPN_402	[58D6]
C6N1	CAPN_805	[45D5]
C6N2	CAPN_603	[45D5]
C6N3	CAPN_1206	[45B3]
C6N4	CAPN_402	[54D7]
C6R1	CAPN_805	[9B6]
C6R2	CAPN_805	[9B8]
C6R3	CAPN_805	[9C8]
C6R4	CAPN_805	[9D8]
C6R5	CAPN_805	[9A8]
C6R6	CAPN_805	[9C6]
C6R7	CAPN_805	[9B6]
C6R8	CAPN_402	[11D5]
C6R9	CAPN_402	[11B6]
C6R10	CAPN_402	[11B6]
C6R11	CAPN_402	[12A2]
C6R12	CAPN_402	[11B3]
C6R13	CAPN_402	[11C3]
C6R14	CAPN_402	[11B3]
C6R15	CAPN_402	[10B4]
C6R16	CAPN_402	[12A2]
C6R17	CAPN_402	[10A3]
C6R18	CAPN_402	[10A3]
C6R19	CAPN_402	[11C5]
C6R20	CAPN_402	[10A4]
C6R21	CAPN_402	[10B4]
C6R22	CAPN_402	[11C5]
C6R23	CAPN_402	[12A1]
C6R24	CAPN_402	[11B4]
C6R25	CAPN_402	[10C5]
C6R26	CAPN_402	[11A5]
C6R27	CAPN_402	[12A3]
C6R28	CAPN_402	[10B5]
C6R29	CAPN_402	[11A5]
C6R30	CAPN_402	[11A4]
C6R31	CAPN_402	[10B6]
C6R32	CAPN_402	[11A5]
C6R33	CAPN_402	[10C4]
C6R34	CAPN_402	[11C5]
C6R35	CAPN_402	[11C5]
C6R36	CAPN_402	[10D3]
C6R37	CAPN_402	[10C4]
C6R38	CAPN_402	[10A6]
C6R39	CAPN_402	[11D5]

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C6R40	CAPN_402	[11A3]
C6R41	CAPN_402	[11A3]
C6R42	CAPN_402	[10C4]
C6R43	CAPN_402	[10A6]
C6R44	CAPN_402	[10A4]
C6R45	CAPN_402	[10C4]
C6R46	CAPN_402	[12A1]
C6T2	CAPN_402	[11B4]
C6T3	CAPN_402	[11C5]
C6T4	CAPN_402	[11A5]
C6T5	CAPN_402	[11D3]
C6T6	CAPN_402	[10B5]
C6T7	CAPN_402	[10C6]
C6T8	CAPN_402	[10B4]
C6T9	CAPN_402	[11C3]
C6T10	CAPN_402	[12A6]
C6T11	CAPN_402	[10C4]
C6T12	CAPN_402	[10B6]
C6T13	CAPN_402	[11A3]
C6T14	CAPN_402	[10A4]
C6T15	CAPN_402	[11C6]
C6T16	CAPN_402	[11A4]
C6T17	CAPN_402	[11A3]
C6T18	CAPN_402	[11C6]
C6T19	CAPN_402	[11C3]
C6T20	CAPN_402	[10C5]
C6T22	CAPN_805	[9A5]
C6T23	CAPN_805	[9A5]
C6T24	CAPN_402	[11A3]
C6T25	CAPN_402	[11B3]
C6T26	CAPN_402	[13A2]
C6T27	CAPN_402	[12A6]
C6T28	CAPN_402	[13A5]
C6T29	CAPN_402	[12A5]
C6T30	CAPN_805	[12A2]
C6T31	CAPN_402	[13A1]
C6T32	CAPN_402	[12A5]
C6T33	CAPN_402	[13A5]
C6U1	CAPN_402	[19A2]
C6U2	CAPN_402	[19A2]
C6U3	CAPN_402	[19A3]
C6U4	CAPN_402	[19A2]
C6U5	CAPN_402	[19A1]
C6U6	CAPN_402	[19A3]
C6U7	CAPN_402	[20A7]
C6U8	CAPN_402	[19A1]
C6U9	CAPN_402	[19A3]
C6U10	CAPN_402	[21A6]
C7A1	CAPN_603	[38A3]
C7A2	CAPN_603	[38A3]
C7A3	CAPN_603	[38A3]
C7A4	CAPN_603	[38A2]
C7B1	CAPN_1206	[43B6]
C7B2	CAP_P_TH	[38A3]
C7B3	CAP_P_TH	[43B5]
C7B4	CAPN_402	[54D6]
C7B5	CAPN_1206	[45D3]
C7B7	CAPN_402	[44A6]
C7B8	CAP_P_TH	[49D8]
C7C1	CAPN_402	[44B5]
C7C2	CAPN_402	[44A7]
C7C3	CAPN_402	[44B5]
C7C4	CAPN_402	[44A5]
C7C5	CAPN_402	[44A7]
C7C6	CAPN_402	[44A2]
C7C7	CAPN_402	[44B2]
C7C8	CAPN_805	[45C3]
C7C9	CAPN_402	[44D3]
C7C10	CAPN_1206	[44D5]
C7C11	CAPN_603	[44D4]
C7C12	CAP_P_RDL	[43A4]
C7C13	CAP_P_RDL	[43A4]
C7D7	CAPN_402	[16A1]
C7D8	CAPN_402	[16A1]
C7D9	CAPN_402	[16A3]
C7D10	CAPN_402	[16A2]
C7D11	CAPN_805	[16A4]
C7D12	CAPN_402	[17A7]
C7D13	CAPN_402	[16A3]
C7D14	CAPN_402	[16A2]
C7D15	CAPN_402	[21A4]
C7E1	CAPN_402	[21A4]
C7E2	CAPN_402	[16A2]
C7E3	CAPN_402	[16A3]
C7E4	CAPN_402	[14A1]
C7E5	CAPN_402	[14A2]
C7E6	CAPN_402	[14A3]
C7E7	CAPN_402	[14A1]
C7E8	CAPN_805	[14A4]
C7E9	CAPN_402	[15A7]
C7E10	CAPN_402	[14A2]
C7E11	CAPN_402	[14A3]
C7E12	CAPN_402	[21A5]
C7E13	CAPN_402	[14A2]
C7E14	CAPN_402	[14A3]
C7F1	CAPN_805	[50C2]
C7F2	CAP_P_RDL	[50C2]
C7F3	CAPN_1206	[50D3]
C7G1	CAP_P_RDL	[39C7]
C7G2	CAPN_402	[39C7]
C7N1	CAPN_1206	[45D3]
C7P1	CAPN_402	[44A5]
C7P2	CAPN_603	[44D6]
C7R1	CAP_P_SM	[50B2]
C7R2	CAPN_402	[17A1]
C7R3	CAPN_402	[17A1]
C7R4	CAPN_402	[17A3]
C7R5	CAPN_402	[17A2]
C7R6	CAPN_402	[16A7]
C7R7	CAPN_402	[17A3]
C7R8	CAPN_402	[17A2]
C7R9	CAPN_402	[21A4]
C7T1	CAPN_402	[17A2]
C7T2	CAPN_402	[17A3]
C7T3	CAPN_402	[15A1]
C7T4	CAPN_402	[15A2]
C7T5	CAPN_402	[15A3]
C7T6	CAPN_402	[15A1]
C7T7	CAPN_402	[14A7]
C7T8	CAPN_402	[15A2]
C7T9	CAPN_402	[15A3]
C7T10	CAPN_402	[21A5]
C7T11	CAPN_402	[15A2]
C7T12	CAPN_402	[15A3]
C7U1	CAPN_1206	[50D3]
C7V1	CAPN_805	[39C7]
D4A1	DIODE_SOT23	[36C5]
D4D1	LED_SM	[60B5]
D5B1	DIODE_SOT23	[45B6]
D6B1	DIODE_SOT23	[45D6]
DB1E1	DBPAD_TP	[42C1]
DB1F1	DBPAD_TP	[58A2]
DB1F2	DBPAD_TP	[48B1]
DB1V1	DBPAD_TP	[58B1]
DB1V2	DBPAD_TP	[58B1]
DB1V3	DBPAD_TP	[58B1]
DB2E1	DBPAD_TP	[52C5]
DB2G1	DBPAD_TP	[48C1]
DB2G2	DBPAD_TP	[47C1]
DB2G3	DBPAD_TP	[27A8]
DB2G4	DBPAD_TP	[47B1]
DB2N1	DBPAD_TP	[35C4]
DB2N2	DBPAD_TP	[35C4]
DB2N3	DBPAD_TP	[35C4]
DB2R1	DBPAD_TP	[32B5]
DB2R2	DBPAD_TP	[26B3]
DB2R3	DBPAD_TP	[26B3]
DB2R4	DBPAD_TP	[26B3]
DB2R5	DBPAD_TP	[26B3]
DB2R6	DBPAD_TP	[26B3]
DB2R7	DBPAD_TP	[26B3]
DB2R8	DBPAD_TP	[26D6]
DB2R9	DBPAD_TP	[26B3]
DB2R10	DBPAD_TP	[26B3]
DB2R11	DBPAD_TP	[26C3]
DB2R12	DBPAD_TP	[26C3]
DB2R13	DBPAD_TP	[26C3]
DB2R14	DBPAD_TP	[26C3]
DB2R15	DBPAD_TP	[26A3]
DB2R16	DBPAD_TP	[26A3]
DB3E1	DBPAD_TP	[52B5]
DB3M1	DBPAD_TP	[40B3]
DB3P1	DBPAD_TP	[23A6]
DB3R1	DBPAD_TP	[26B3]
DB3R2	DBPAD_TP	[26D6]
DB3R3	DBPAD_TP	[26C3]
DB3R4	DBPAD_TP	[26C3]
DB3R5	DBPAD_TP	[26C3]
DB3R6	DBPAD_TP	[27A6]
DB3R7	DBPAD_TP	[27A6]
DB3T1	DBPAD_TP	[26D6]
DB4D1	DBPAD_TP	[52A1]
DB4E1	DBPAD_TP	[52C1]
DB4E2	DBPAD_TP	[52B5]
DB4E3	DBPAD_TP	[49C1]
DB4E4	DBPAD_TP	[49B3]
DB4E5	DBPAD_TP	[49B3]
DB4N2	DBPAD_TP	[51C6]
DB4N3	DBPAD_TP	[51B6]
DB4N4	DBPAD_TP	[23A2]
DB4N5	DBPAD_TP	[23A2]
DB4N6	DBPAD_TP	[23A2]
DB4N7	DBPAD_TP	[23A2]
DB4P6	DBPAD_TP	[51C6]
DB4P7	DBPAD_TP	[51C6]
DB4P8	DBPAD_TP	[51C8]
DB4R1	DBPAD_TP	[5C4]
DB5A1	DBPAD_TP	[53A3]
DB5B1	DBPAD_TP	[53B1]
DB5B2	DBPAD_TP	[51A3]
DB5B3	DBPAD_TP	[51A3]
DB5B4	DBPAD_TP	[53C1]
DB5B5	DBPAD_TP	[53C3]
DB5C1	DBPAD_TP	[51B1]
DB5R5	DBPAD_TP	[6B5]
DB6M1	DBPAD_TP	[38A4]
DB6M2	DBPAD_TP	[38B4]
DB6M3	DBPAD_TP	[38B4]
DB6N1	DBPAD_TP	[38A4]
DB6R1	DBPAD_TP	[43B3]
DB6R2	DBPAD_TP	[43B3]
DB7C1	DBPAD_TP	[44C2]
DB7C2	DBPAD_TP	[44C4]
DB7C3	DBPAD_TP	[44C4]
DB7C4	DBPAD_TP	[45C1]
DB7C5	DBPAD_TP	[44A8]
DB7C6	DBPAD_TP	[44A8]
DB7F1	DBPAD_TP	[50C2]
DB7F2	DBPAD_TP	[50B2]
DB7P1	DBPAD_TP	[44C2]
DB7P2	DBPAD_TP	[44C2]
EG1A1	ESDGUARD_402	[39A7]
EG1A2	ESDGUARD_402	[39A7]
EG1A3	ESDGUARD_402	[39B2]
EG1A4	ESDGUARD_402	[39B3]
EG1A5	ESDGUARD_402	[39A2]
EG1A6	ESDGUARD_402	[39A3]
EG1A7	ESDGUARD_402	[39C2]
EG1A8	ESDGUARD_402	[39C3]
EG1B1	ESDGUARD_402	[41C7]
EG1B2	ESDGUARD_402	[41C6]
EG1B3	ESDGUARD_402	[41D7]
EG1B4	ESDGUARD_402	[41D6]
EG2A1	ESDGUARD_402	[37D7]
EG2A2	ESDGUARD_402	[38C4]
EG2A3	ESDGUARD_402	[38C5]
EG2A4	ESDGUARD_402	[38C6]
EG2A5	ESDGUARD_402	[38C6]

EG2A6	ESDGUARD_402	[38C6]
EG2A7	ESDGUARD_402	[38B6]
EG3A1	ESDGUARD_402	[40D6]
EG3A2	ESDGUARD_402	[40D7]
EG3A3	ESDGUARD_402	[40C6]
EG3A4	ESDGUARD_402	[40C7]
EG3A5	ESDGUARD_402	[40C6]
EG4A1	ESDGUARD_402	[39A7]
EG4A2	ESDGUARD_402	[40C7]
EG4A3	ESDGUARD_402	[40B6]
EG4A4	ESDGUARD_402	[40B7]
EG4A5	ESDGUARD_402	[37A5]
EG4A6	ESDGUARD_402	[37A5]
EG4A7	ESDGUARD_402	[37A8]
EG4A8	ESDGUARD_402	[37A8]
EG4A9	ESDGUARD_402	[37A2]
EG4A10	ESDGUARD_402	[37A2]
EG4M1	ESDGUARD_402	[40A6]
EG4M2	ESDGUARD_402	[40A7]
EG4M5	ESDGUARD_402	[40A2]
EG6G1	ESDGUARD_402	[39C7]
EG6G2	ESDGUARD_402	[39C7]
EG7G1	ESDGUARD_402	[39C7]
EG7G2	ESDGUARD_402	[39C7]
FB1A1	FERRITE_603	[39B7]
FB2C1	FERRITE_603	[32D8]
FB2M1	FERRITE_603	[38C4]
FB2R1	FERRITE_603	[32C5]
FB2R2	FERRITE_603	[31B7]
FB2R3	FERRITE_603	[31C7]
FB2T1	FERRITE_603	[31A7]
FB2T2	FERRITE_603	[31B7]
FB2T3	FERRITE_603	[30C7]
FB3A1	FERRITE_603	[33B2]
FB3A2	FERRITE_603	[33C2]
FB3N1	FERRITE_603	[25C8]
FB3N2	FERRITE_603	[25B8]
FB3N3	FERRITE_603	[24C6]
FB3N4	FERRITE_603	[24C6]
FB3P1	FERRITE_603	[25D2]
FB3R1	FERRITE_603	[30A7]
FB3R2	FERRITE_603	[31D7]
FB3T1	FERRITE_603	[30C8]
FB3T2	FERRITE_603	[30D7]
FB3T3	FERRITE_603	[30A7]
FB5R1	FERRITE_603	[6D6]
FB5R2	FERRITE_603	[6C6]
FB5R3	FERRITE_603	[6A6]
FB5R4	FERRITE_603	[6B6]
FB5R5	FERRITE_603	[6B6]
FB5T1	FERRITE_603	[6A6]
FB5T2	FERRITE_603	[6C6]
FB5T3	FERRITE_603	[6B6]
FT1M3	FTPAD_TP	[41A7]
FT1M4	FTPAD_TP	[41A7]
FT1M5	FTPAD_TP	[41A6]
FT1N1	FTPAD_TP	[46C2]
FT1N2	FTPAD_TP	[41B7]
FT1N3	FTPAD_TP	[41A7]
FT1N4	FTPAD_TP	[41D5]
FT1N5	FTPAD_TP	[41D5]
FT1N6	FTPAD_TP	[41C5]
FT1N7	FTPAD_TP	[41C5]
FT1N8	FTPAD_TP	[41C5]
FT1N9	FTPAD_TP	[46C2]
FT1P1	FTPAD_TP	[46B7]
FT1T1	FTPAD_TP	[34C8]
FT1T2	FTPAD_TP	[34C8]
FT1T3	FTPAD_TP	[34C8]
FT1T4	FTPAD_TP	[34C8]
FT1T5	FTPAD_TP	[34C8]
FT1T6	FTPAD_TP	[34C8]
FT1T7	FTPAD_TP	[34C8]
FT1T8	FTPAD_TP	[34C8]
FT1T9	FTPAD_TP	[48A1]
FT1T10	FTPAD_TP	[48C8]
FT1T11	FTPAD_TP	[34C4]
FT2M1	FTPAD_TP	[38D7]
FT2M2	FTPAD_TP	[38D7]
FT2P2	FTPAD_TP	[22B1]
FT2R1	FTPAD_TP	[22A1]
FT2R2	FTPAD_TP	[26A3]
FT2R3	FTPAD_TP	[22B1]
FT2R4	FTPAD_TP	[22C1]
FT2R5	FTPAD_TP	[22A1]
FT2R6	FTPAD_TP	[35A7]
FT2R7	FTPAD_TP	[35A3]
FT2T1	FTPAD_TP	[52C5]
FT2T2	FTPAD_TP	[47C8]
FT2T3	FTPAD_TP	[47A1]
FT2T4	FTPAD_TP	[35A7]
FT2T5	FTPAD_TP	[35A7]
FT2U2	FTPAD_TP	[41B3]
FT2U3	FTPAD_TP	[41B3]
FT2V1	FTPAD_TP	[27A8]
FT2V2	FTPAD_TP	[47C1]
FT2V3	FTPAD_TP	[48C1]
FT2V4	FTPAD_TP	[35A3]
FT3M1	FTPAD_TP	[40D7]
FT3M2	FTPAD_TP	[40D7]
FT3M3	FTPAD_TP	[40D7]
FT3M4	FTPAD_TP	[40C7]
FT3M5	FTPAD_TP	[40C7]
FT3M6	FTPAD_TP	[33B7]
FT3M7	FTPAD_TP	[40D7]
FT3M8	FTPAD_TP	[40D7]
FT3M9	FTPAD_TP	[40D7]
FT3M10	FTPAD_TP	[40C7]
FT3M11	FTPAD_TP	[40C7]
FT3N1	FTPAD_TP	[22B4]
FT3N2	FTPAD_TP	[22A1]
FT3N3	FTPAD_TP	[33D7]
FT3P1	FTPAD_TP	[22D7]
FT3P2	FTPAD_TP	[22D3]
FT3P3	FTPAD_TP	[22B1]
FT3P4	FTPAD_TP	[22B1]
FT3P5	FTPAD_TP	[22B8]
FT3P6	FTPAD_TP	[22B8]
FT3P7	FTPAD_TP	[22B8]
FT3P8	FTPAD_TP	[22B8]
FT3P9	FTPAD_TP	[22B8]
FT3R1	FTPAD_TP	[22D3]
FT3R3	FTPAD_TP	[22D3]
FT3R4	FTPAD_TP	[27C8]
FT3R5	FTPAD_TP	[27B8]
FT3R6	FTPAD_TP	[27B8]
FT3R9	FTPAD_TP	[27A6]
FT3R10	FTPAD_TP	[22C1]
FT3R11	FTPAD_TP	[22C1]
FT3R12	FTPAD_TP	[27B1]
FT3R13	FTPAD_TP	[22C8]
FT3R14	FTPAD_TP	[22D7]
FT3R15	FTPAD_TP	[27D8]
FT3R16	FTPAD_TP	[4D2]
FT3R17	FTPAD_TP	[4C7]
FT3T1	FTPAD_TP	[52B5]
FT3T2	FTPAD_TP	[44D1]
FT3T3	FTPAD_TP	[44D8]
FT3T4	FTPAD_TP	[26B5]
FT3T5	FTPAD_TP	[26B5]
FT3T6	FTPAD_TP	[26B5]
FT3T7	FTPAD_TP	[26B5]
FT3T8	FTPAD_TP	[26A5]
FT3U1	FTPAD_TP	[49A1]
FT3V1	FTPAD_TP	[49B8]
FT3V2	FTPAD_TP	[50A1]
FT3V3	FTPAD_TP	[50C8]
FT3V4	FTPAD_TP	[49D2]
FT3V5	FTPAD_TP	[50D2]
FT3V6	FTPAD_TP	[35A2]
FT3V7	FTPAD_TP	[35A2]
FT4M1	FTPAD_TP	[40A7]
FT4M2	FTPAD_TP	[40C7]
FT4M3	FTPAD_TP	[40B7]
FT4M4	FTPAD_TP	[40B7]
FT4M5	FTPAD_TP	[40A7]
FT4M6	FTPAD_TP	[40B2]
FT4M7	FTPAD_TP	[40C7]
FT4M8	FTPAD_TP	[40B7]
FT4M9	FTPAD_TP	[40B7]
FT4N1	FTPAD_TP	[23A6]
FT4N2	FTPAD_TP	[23A6]
FT4P1	FTPAD_TP	[5B7]
FT4P2	FTPAD_TP	[5B7]
FT4P4	FTPAD_TP	[5C7]
FT4P5	FTPAD_TP	[5C7]
FT4P6	FTPAD_TP	[5C7]
FT4P7	FTPAD_TP	[5C7]
FT4P8	FTPAD_TP	[5C7]
FT4R2	FTPAD_TP	[2D6]
FT4R3	FTPAD_TP	[52A1]
FT4R4	FTPAD_TP	[3B4]
FT4R5	FTPAD_TP	[52A4]
FT4R6	FTPAD_TP	[3B4]
FT4R7	FTPAD_TP	[3B4]
FT4R8	FTPAD_TP	[3B4]
FT4R9	FTPAD_TP	[3B4]
FT4R10	FTPAD_TP	[27B6]
FT4T1	FTPAD_TP	[52D1]
FT4T2	FTPAD_TP	[2B8]
FT4T3	FTPAD_TP	[52B5]
FT5M1	FTPAD_TP	[53B3]
FT5M2	FTPAD_TP	[53B6]
FT5M3	FTPAD_TP	[53C7]
FT5N1	FTPAD_TP	[53C6]
FT5N2	FTPAD_TP	[53C3]
FT5P1	FTPAD_TP	[3C6]
FT5P2	FTPAD_TP	[3C6]
FT5R1	FTPAD_TP	[3A4]
FT5R2	FTPAD_TP	[3A4]
FT5R3	FTPAD_TP	[3A4]
FT5R4	FTPAD_TP	[3A4]
FT5R5	FTPAD_TP	[3A4]
FT5R6	FTPAD_TP	[3A4]
FT5R7	FTPAD_TP	[3A4]
FT5R8	FTPAD_TP	[3A4]
FT5R9	FTPAD_TP	[3A4]
FT5R10	FTPAD_TP	[3A4]
FT5R11	FTPAD_TP	[3A4]
FT5R12	FTPAD_TP	[3A4]
FT5R13	FTPAD_TP	[3A4]
FT5R14	FTPAD_TP	[3A4]
FT5R15	FTPAD_TP	[3A4]
FT5R16	FTPAD_TP	[3A4]
FT5R17	FTPAD_TP	[51C1]
FT5R18	FTPAD_TP	[2D6]
FT5T2	FTPAD_TP	[3D6]
FT5T4	FTPAD_TP	[49C1]
FT6M1	FTPAD_TP	[38A4]
FT6R1	FTPAD_TP	[43A3]
FT6R2	FTPAD_TP	[43A3]
FT6U1	FTPAD_TP	[50C2]
FT7N1	FTPAD_TP	[38A4]
FT7P1	FTPAD_TP	[44C5]
FT7P2	FTPAD_TP	[44B5]
FT7P3	FTPAD_TP	[2C2]
FT7P4	FTPAD_TP	[2C2]
FT7P5	FTPAD_TP	[2C2]
FT7P6	FTPAD_TP	[2C2]
FT7P7	FTPAD_TP	[2C2]
FT7P8	FTPAD_TP	[2C2]
J1A1	WAVERECEPTACLE_TH	[39B5]
J1A2	USBTRIPLE_TH	[39C1]
J1B1	1X7SATA_TH	[41A6]
J1B2	1X7SATA_TH	[41C5]
J1D1	1X6HDR_SMT	[41B1]
J1F1	1X2HDR_TH	[35A1]
J1G3	2X4HDR_TH	[58A3]

J2A1	TRINITYRJ45AUX_TH	[38B3]
J2C1	2X5HDR10_TH	[59C7]
J2C3	2X7HDR14_TH	[59C3]
J3A1	HDMI_1X19HDR	[40B2]
J3C1	2X3HDR_TH	[60C7]
J3G1	2X3HDR_TH	[60B7]
J4A1	TOSLINK_TX_TH	[39A5]
J4A2	XENONAVIP_TH	[37C5]
J4A3	2X6HDR2_TH	[41A2]
J4C1	2X4HDR_TH	[60D7]
J4C2	2X5HDR_TH	[60A6]
J4D1	2X3HDR_TH	[60C7]
J5A4	1X4HDR_TH	[36C2]
J5B1	2X2HDR_TH	[55C6]
J5B2	1X5HDR2_TH	[41D1]
J5G2	XENONRF_BORON_TH	[38A5]
J6G1	USBDUALHORIZONTAL_TH	[39C5]
J7A1	TRINITYPWR_TH	[38A1]
L1F1	INDUCTOR_TH	[48C3]
L2B1	INDUCTOR_TH	[47D8]
L2F1	INDUCTOR_TH	[47C4]
L4A1	INDUCTOR_1210	[37A4]
L4A2	INDUCTOR_1210	[37A4]
L4A3	INDUCTOR_1210	[37A7]
L4A4	INDUCTOR_1210	[37A7]
L4B1	INDUCTOR_TH	[51C5]
L4F1	INDUCTOR_TH	[49C3]
L5A1	INDUCTOR_1210	[53B4]
L5B2	INDUCTOR_1210	[53C4]
L5C1	INDUCTOR_TH	[51B3]
L6A1	INDUCTOR_1210	[53C8]
L6B1	INDUCTOR_TH	[43B5]
L6C1	IND_2MODE_SM	[45C1]
L6C2	IND_2MODE_TH	[45B1]
L7B1	INDUCTOR_TH	[49D8]
L7F1	INDUCTOR_TH	[50C3]
LB2B1	LABEL_SM	[62D5]
MTG1B1	STD_MTG_HOLE_TH	[62C6]
MTG1G1	STD_MTG_HOLE_TH	[62C6]
MTG4D1	STD_MTG_HOLE_TH	[62A6]
MTG4F1	STD_MTG_HOLE_TH	[62B6]
MTG4G1	STD_MTG_HOLE_TH	[62C5]
MTG6D1	STD_MTG_HOLE_TH	[62A4]
MTG6F1	STD_MTG_HOLE_TH	[62B4]
MTG7G1	STD_MTG_HOLE_TH	[62C3]
Q1F1	SHUNT_3PIN_SOT23	[56D3]
Q1N1	MBT3904DUAL_SOT	[46C5]
Q1N2	FET_SOT23	[35C7]
Q1N3	FET_SOT23	[35C7]
Q1T1	NPN_SOT23	[42B2]
Q1T2	NPN_SOT23	[42B2]
Q2F1	FET_VREG_DPAK	[47C4]
Q2F2	FET_VREG_DPAK	[47B4]
Q2F3	SHUNT_3PIN_SOT23	[56D7]
Q2N1	NPN_SOT23	[35C4]
Q3A1	MBT3904DUAL_SOT	[37C7]
Q3F1	FET_VREG_DPAK	[49C4]
Q3M1	PNP_SOT23	[37B7]
Q4A1	NPN_SOT23	[36C5]
Q4B1	ADR510_SOT23	[57A5]
Q4D1	NPN_SOT23	[60A3]
Q4D2	NPN_SOT23	[60A4]
Q4F1	FET_VREG_DPAK	[49B4]
Q4G1	PNP_SOT23	[23C1]
Q5A2	PNP_DPAK	[36C5]
Q5B1	FET_VREG_DPAK	[51C3]
Q5C1	FET_VREG_DPAK	[45A3]
Q5C2	FET_VREG_DPAK	[51B3]
Q5C3	FET_VREG_DPAK	[45A4]
Q6A1	NPN_SOT23	[42B6]
Q6A2	FET_SOT23	[42B6]
Q6B1	FET_VREG_DPAK	[45A4]
Q6B2	FET_VREG_DPAK	[45D4]
Q6C1	FET_VREG_DPAK	[45C3]
Q6C2	FET_VREG_DPAK	[45C4]
Q6M1	PNP_2C_SOT223	[42C4]
Q7G1	FET_VREG_DPAK	[50C4]
Q7G2	FET_VREG_DPAK	[50B4]
R1A1	RESN_402	[39B7]
R1C1	RESN_805	[52C6]
R1D1	RESN_1210	[52D7]
R1D2	RESN_1210	[52D8]
R1D3	RESN_1210	[52D8]
R1D4	RESN_1210	[52D8]
R1D5	RESN_402	[41C2]
R1D6	RESN_402	[41B2]
R1E12	RESN_402	[47C7]
R1E14	RESN_402	[48D5]
R1E15	RESN_402	[48C7]
R1E16	RESN_402	[48C7]
R1E17	RESN_402	[47B7]
R1E19	RESN_402	[48A3]
R1E20	RESN_402	[48A3]
R1E21	RESN_402	[48A7]
R1E22	RESN_402	[48D4]
R1F1	RESN_402	[48B5]
R1F2	RESN_402	[48B4]
R1F3	RESN_402	[47B4]
R1F4	RESN_402	[56A5]
R1F5	RESN_402	[56A4]
R1F6	RESN_402	[56A5]
R1F9	RESN_2512	[48C2]
R1G1	RESN_402	[58B3]
R1N1	RESN_402	[46C5]
R1N2	RESN_402	[46C6]
R1N3	RESN_402	[46C5]
R1N4	RESN_402	[35D6]
R1N5	RESN_402	[35D7]
R1P1	RESN_402	[46C6]
R1P2	RESN_402	[46B5]
R1T1	RESN_402	[42B3]
R1T2	RESN_402	[47C7]
R1T3	RESN_1206	[42C1]
R1T4	RESN_805	[47D8]
R1T5	RESN_402	[34C5]
R1T6	RESN_1206	[42C2]
R1T7	RESN_402	[42C2]
R1T8	RESN_402	[34B7]
R1T9	RESN_402	[34C6]
R1T10	RESN_402	[34C6]
R1T11	RESN_402	[34B7]
R1T12	RESN_402	[34B6]
R1T13	RESN_402	[34B6]
R1T14	RESN_402	[34C2]
R1T15	RESN_402	[34B6]
R1T16	RESN_402	[34B6]
R1T17	RESN_402	[34B5]
R1T18	RESN_402	[34B5]
R1T19	RESN_402	[56C3]
R1U3	RESN_402	[56C7]
R1U4	RESN_402	[56C7]
R1U5	RESN_402	[56D2]
R2A2	RESN_402	[38C7]
R2A3	RESN_402	[38C7]
R2A4	RESN_402	[38C7]
R2A5	RESN_402	[38B7]
R2B1	RESN_402	[55D7]
R2B2	RESN_402	[55C7]
R2B3	RESN_402	[55D7]
R2B4	RESN_402	[55D7]
R2C1	RESN_402	[27D3]
R2C3	RESN_402	[37C1]
R2C4	RESN_402	[59C2]
R2C5	RESN_402	[27C6]
R2C6	RESN_402	[59C4]
R2C7	RESN_402	[59C2]
R2C8	RESN_402	[28D3]
R2C9	RESN_402	[26C2]
R2C10	RESN_402	[41B2]
R2C11	RESN_402	[41B2]
R2D1	RESN_402	[32B6]
R2D2	RESN_402	[32B7]
R2D3	RESN_402	[32A6]
R2D4	RESN_402	[32C2]
R2D5	RESN_402	[29B2]
R2D6	RESN_402	[32C6]
R2D7	RESN_402	[29D6]
R2D8	RESN_402	[29D6]
R2D9	RESN_402	[29B2]
R2D10	RESN_402	[29B3]
R2D11	RESN_402	[29B2]
R2D12	RESN_402	[29B3]
R2D13	RESN_402	[29D3]
R2D14	RESN_402	[26B7]
R2D15	RESN_402	[26B8]
R2D16	RESN_402	[26B8]
R2D17	RESN_402	[26B8]
R2D18	RESN_402	[26B7]
R2D19	RESN_402	[26A5]
R2E1	RESN_402	[29A6]
R2E2	RESN_402	[47B8]
R2E3	RESN_402	[47B7]
R2E4	RESN_402	[47A3]
R2E5	RESN_402	[47A8]
R2E6	RESN_402	[47C4]
R2E7	RESN_402	[47C7]
R2E8	RESN_402	[26A5]
R2E9	RESN_402	[26A7]
R2F1	RESN_402	[47B5]
R2F2	RESN_402	[56C6]
R2F3	RESN_402	[56C6]
R2F4	RESN_402	[56A5]
R2F5	RESN_402	[56A4]
R2F7	RESN_805	[47A3]
R2F8	RESN_402	[56A4]
R2F9	RESN_805	[48B3]
R2G1	RESN_2512	[47C3]
R2G2	RESN_1206	[47B1]
R2G3	RESN_402	[26A3]
R2G4	RESN_402	[26A3]
R2G5	RESN_402	[26A3]
R2G21	RESN_402	[26A1]
R2N1	RESN_402	[37C2]
R2N2	RESN_402	[35C7]
R2N3	RESN_402	[35C7]
R2N4	RESN_402	[35D5]
R2N5	RESN_402	[35D6]
R2N6	RESN_402	[35D6]
R2N7	RESN_402	[35D4]
R2N8	RESN_402	[35C3]
R2R1	RESN_402	[32B6]
R2R2	RESN_402	[32C6]
R2R3	RESN_402	[32C6]
R2R4	RESN_402	[32A6]
R2R5	RESN_402	[32B6]
R2R6	RESN_402	[32A7]
R2R7	RESN_402	[32C2]
R2R8	RESN_402	[32A7]
R2R9	RESN_402	[32C3]
R2R10	RESN_402	[32C3]
R2R11	RESN_402	[32A2]
R2R12	RESN_402	[32C1]
R2R13	RESN_402	[32A2]
R2R14	RESN_402	[29B4]
R2R15	RESN_402	[32C2]
R2R16	RESN_402	[29B3]
R2R17	RESN_402	[29B4]
R2R18	RESN_402	[29B3]
R2R19	RESN_402	[26D7]
R2R20	RESN_402	[26B7]
R2R21	RESN_402	[26B8]
R2R22	RESN_402	[26B8]
R2R23	RESN_402	[26C7]
R2R24	RESN_402	[26B8]
R2R25	RESN_402	[26B7]
R2R26	RESN_402	[26A7]
R2T1	RESN_402	[28B6]

R2T2	RESN_402	[28A6]
R2T3	RESN_402	[47D5]
R2T4	RESN_402	[47A3]
R2T5	RESN_402	[56C6]
R2U1	RESN_402	[56D7]
R3A1	RESN_402	[37C7]
R3A2	RESN_402	[37C6]
R3A3	RESN_402	[37C8]
R3A4	RESN_402	[37C8]
R3A5	RESN_402	[37C7]
R3A6	RESN_603	[37C7]
R3A8	RESN_402	[33B3]
R3A9	RESN_402	[33B3]
R3A10	RESN_402	[33B2]
R3A11	RESN_402	[33B2]
R3B2	RESN_402	[23C3]
R3B3	RESN_402	[22D6]
R3B4	RESN_402	[23B6]
R3B5	RESN_603	[23B1]
R3B6	RESN_603	[23B1]
R3B7	RESN_603	[23B1]
R3B8	RESN_603	[23C1]
R3B9	RESN_402	[22D8]
R3B10	RESN_402	[22C7]
R3B11	RESN_402	[22C7]
R3B12	RESN_402	[22A3]
R3B13	RESN_402	[22A2]
R3B14	RESN_402	[22B2]
R3B15	RESN_402	[22A3]
R3B16	RESN_402	[22B2]
R3B17	RESN_402	[22B2]
R3B18	RESN_402	[22C2]
R3B19	RESN_402	[22C2]
R3B20	RESN_402	[22C2]
R3B21	RESN_402	[22C2]
R3B22	RESN_805	[33D6]
R3B24	RESN_402	[37A2]
R3C1	RESN_402	[22C2]
R3C2	RESN_402	[22C2]
R3C3	RESN_402	[22C2]
R3C4	RESN_402	[22D2]
R3C5	RESN_402	[22D2]
R3C6	RESN_402	[22D2]
R3C7	RESN_402	[22C2]
R3C8	RESN_402	[22D2]
R3C9	RESN_402	[22D2]
R3C10	RESN_402	[22D2]
R3C11	RESN_402	[22B3]
R3C12	RESN_402	[22B3]
R3C13	RESN_402	[22B2]
R3C14	RESN_402	[22B2]
R3D1	RESN_402	[27A7]
R3D2	RESN_402	[27A7]
R3D3	RESN_402	[26B7]
R3D4	RESN_402	[26B6]
R3D5	RESN_402	[26B7]
R3D7	RESN_402	[26A8]
R3D8	RESN_402	[26A7]
R3D9	RESN_402	[26A1]
R3D10	RESN_402	[26A1]
R3E1	RESN_402	[58C4]
R3E2	RESN_402	[58C5]
R3E3	RESN_402	[58C5]
R3E4	RESN_402	[58A7]
R3E5	RESN_805	[52B6]
R3F2	RESN_402	[58C5]
R3F3	RESN_402	[58C5]
R3F4	RESN_402	[52B6]
R3F5	RESN_402	[58C2]
R3F6	RESN_402	[49A7]
R3F7	RESN_402	[49B4]
R3F8	RESN_402	[49A3]
R3F9	RESN_402	[49A3]
R3F10	RESN_402	[49C4]
R3F11	RESN_805	[49B3]
R3F12	RESN_402	[49C7]
R3F13	RESN_402	[49C7]
R3F14	RESN_402	[49C7]
R3F15	RESN_402	[49B7]
R3F16	RESN_402	[55C2]
R3G1	RESN_402	[55A4]
R3G2	RESN_805	[49D7]
R3G4	RESN_402	[49B7]
R3G5	RESN_402	[50C7]
R3G6	RESN_402	[55A4]
R3G7	RESN_402	[55C5]
R3G8	RESN_402	[55C5]
R3G9	RESN_402	[55C5]
R3G10	RESN_402	[50B5]
R3G11	RESN_402	[50A3]
R3G12	RESN_402	[50A3]
R3G13	RESN_402	[50C4]
R3G14	RESN_402	[50B8]
R3G15	RESN_402	[50D5]
R3G16	RESN_402	[49D5]
R3G17	RESN_805	[50A3]
R3G18	RESN_402	[26A7]
R3G19	RESN_402	[26A7]
R3G20	RESN_402	[26A5]
R3M1	RESN_402	[27B6]
R3M2	RESN_402	[37B7]
R3M3	RESN_402	[37B7]
R3M6	RESN_402	[33B5]
R3M7	RESN_402	[37B6]
R3N3	RESN_402	[23B6]
R3N4	RESN_402	[23B6]
R3N5	RESN_402	[22B4]
R3N6	RESN_402	[24B6]
R3N7	RESN_402	[22C8]
R3N8	RESN_402	[22C7]
R3P1	RESN_402	[22C7]
R3R1	RESN_402	[37C2]
R3R2	RESN_402	[37C2]
R3R3	RESN_402	[27B6]
R3R4	RESN_402	[27B6]
R3R5	RESN_402	[50D3]
R3R6	RESN_402	[27C6]
R3R7	RESN_402	[26B7]
R3R8	RESN_402	[26B6]
R3R9	RESN_402	[26B7]
R3R11	RESN_402	[35B6]
R3R13	RESN_402	[59C2]
R3R14	RESN_402	[26D8]
R3R15	RESN_402	[22D4]
R3R16	RESN_402	[22D4]
R3R17	RESN_402	[27B6]
R3R18	RESN_402	[27B6]
R3R19	RESN_402	[27C2]
R3R20	RESN_402	[27B2]
R3R21	RESN_402	[27B3]
R3R22	RESN_402	[26C7]
R3R23	RESN_402	[27B2]
R3R24	RESN_402	[26C8]
R3T1	RESN_805	[31D7]
R3T2	RESN_402	[27A3]
R3T3	RESN_402	[27A2]
R3T4	RESN_402	[26D8]
R3T5	RESN_402	[52C2]
R3U1	RESN_402	[55C5]
R3U2	RESN_402	[58A8]
R3U3	RESN_402	[55C5]
R3V1	RESN_402	[49B4]
R3V4	RESN_402	[50A7]
R3V5	RESN_402	[38A7]
R3V6	RESN_402	[38B6]
R4A1	RESN_402	[36C5]
R4A2	RESN_402	[37A5]
R4A3	RESN_402	[37A5]
R4A4	RESN_402	[37A7]
R4A5	RESN_402	[37A7]
R4A6	RESN_402	[41A3]
R4A7	RESN_402	[36C5]
R4B1	RESN_402	[57B7]
R4B2	RESN_402	[57C5]
R4B3	RESN_402	[57B5]
R4B4	RESN_805	[51C4]
R4B6	RESN_402	[22D5]
R4B7	RESN_402	[22D6]
R4B8	RESN_402	[23D2]
R4B9	RESN_402	[23D2]
R4B10	RESN_402	[23C6]
R4B11	RESN_402	[51B6]
R4B12	RESN_402	[23D3]
R4B13	RESN_402	[23D3]
R4B14	RESN_402	[23A3]
R4B15	RESN_402	[23A7]
R4B16	RESN_402	[22D7]
R4B17	RESN_402	[51B4]
R4B18	RESN_402	[57A3]
R4B19	RESN_402	[51A5]
R4B20	RESN_402	[37A2]
R4B21	RESN_402	[51C7]
R4B22	RESN_402	[51A5]
R4C1	RESN_402	[23A7]
R4C2	RESN_402	[23A5]
R4C3	RESN_402	[5C6]
R4C4	RESN_402	[60A4]
R4C5	RESN_402	[5B7]
R4C6	RESN_402	[60A5]
R4C7	RESN_402	[60A4]
R4C8	RESN_402	[5B7]
R4C9	RESN_402	[60A4]
R4C10	RESN_402	[60A6]
R4C11	RESN_402	[51B7]
R4C13	RESN_402	[51C7]
R4C14	RESN_402	[51B7]
R4C17	RESN_402	[51B6]
R4D1	RESN_402	[2C6]
R4D2	RESN_402	[2C6]
R4D3	RESN_402	[60B4]
R4D4	RESN_402	[2D4]
R4D5	RESN_402	[2D4]
R4E1	RESN_402	[4D7]
R4E2	RESN_402	[4D7]
R4E3	RESN_402	[60A3]
R4E4	RESN_805	[52B6]
R4E5	RESN_402	[52B6]
R4E6	RESN_402	[52B7]
R4E7	RESN_402	[52C2]
R4E8	RESN_402	[52C3]
R4E9	RESN_402	[52C3]
R4E10	RESN_402	[52C2]
R4E11	RESN_805	[52D2]
R4F1	RESN_2512	[49C2]
R4F2	RESN_402	[52A7]
R4G3	RESN_402	[50B4]
R4G4	RESN_402	[38B6]
R4G5	RESN_402	[38B7]
R4G6	RESN_402	[38A7]
R4G7	RESN_402	[38A7]
R4M1	RESN_402	[40A6]
R4M2	RESN_402	[40A7]
R4M5	RESN_402	[40A3]
R4M6	RESN_402	[40A2]
R4N1	RESN_402	[57B5]
R4N2	RESN_402	[57A7]
R4N3	RESN_402	[57A7]
R4N4	RESN_402	[57A6]
R4N5	RESN_402	[57A6]
R4N6	RESN_402	[57A6]
R4N7	RESN_402	[57A6]
R4N8	RESN_402	[57D4]
R4N10	RESN_402	[57C4]
R4N13	RESN_402	[57D4]
R4N14	RESN_402	[57C4]
R4N15	RESN_805	[51B4]
R4P1	RESN_402	[61C4]
R4P2	RESN_402	[61C5]

R4P3	RESN_402	[61B4]
R4P4	RESN_402	[61B4]
R4P5	RESN_402	[61B5]
R4P6	RESN_402	[61B5]
R4P9	RESN_402	[5C7]
R4R1	RESN_402	[52A3]
R4R2	RESN_402	[5C4]
R4R3	RESN_402	[3C3]
R4R4	RESN_805	[52A1]
R4R5	RESN_402	[3C3]
R4R6	RESN_402	[3C3]
R4R7	RESN_402	[5C4]
R4R8	RESN_402	[3C3]
R4R9	RESN_402	[5C4]
R4R10	RESN_402	[5B3]
R4R11	RESN_402	[5C4]
R4R12	RESN_402	[5C3]
R4R13	RESN_402	[3C2]
R4T5	RESN_402	[2B8]
R4T6	RESN_402	[2B8]
R4U4	RESN_402	[52B6]
R4V1	RESN_402	[38A7]
R4V2	RESN_402	[38A7]
R5A3	RESN_402	[36C2]
R5A5	RESN_402	[53B5]
R5A6	RESN_402	[53B4]
R5A7	RESN_402	[53B6]
R5A9	RESN_805	[36C3]
R5A10	RESN_402	[36A3]
R5A11	RESN_805	[53B3]
R5B2	RESN_402	[53C5]
R5B3	RESN_402	[53C6]
R5B4	RESN_805	[53C3]
R5B5	RESN_402	[53C6]
R5B6	RESN_402	[57B4]
R5B13	RESN_805	[51B3]
R5B17	RESN_402	[53C4]
R5C1	RESN_805	[45A2]
R5C2	RESN_2512	[51B2]
R5F1	RESN_402	[19A7]
R5F2	RESN_402	[19A7]
R5F3	RESN_402	[18D7]
R5F4	RESN_402	[18D7]
R5F5	RESN_402	[18A5]
R5G1	RESN_402	[35D2]
R5G2	RESN_402	[35D2]
R5M1	RESN_805	[42B5]
R5M2	RESN_805	[42B5]
R5M3	RESN_402	[36B5]
R5M4	RESN_402	[36B5]
R5M5	RESN_402	[36B5]
R5M6	RESN_402	[53B6]
R5N2	RESN_402	[57C5]
R5N7	RESN_805	[45B7]
R5N8	RESN_805	[45A5]
R5R1	RESN_402	[2A6]
R5T1	RESN_402	[4C6]
R5T2	RESN_402	[13A7]
R5T3	RESN_402	[13A7]
R5T4	RESN_402	[13A3]
R5T5	RESN_402	[13A3]
R5T6	RESN_402	[13B5]
R5T7	RESN_402	[13B5]
R5U1	RESN_402	[19A5]
R5U2	RESN_402	[19D7]
R5U3	RESN_402	[19D7]
R5U4	RESN_402	[18A7]
R5U5	RESN_402	[18A7]
R5U6	RESN_402	[4A4]
R6A3	RESN_402	[42B7]
R6A4	RESN_402	[42B7]
R6A5	RESN_402	[38A3]
R6A6	RESN_402	[38A2]
R6A7	RESN_402	[42C6]
R6A8	RESN_402	[42C6]
R6A9	RESN_402	[42C5]
R6A10	RESN_402	[58D7]
R6A11	RESN_402	[58C7]
R6C1	RESN_805	[45C3]
R6C2	THERMISTOR_603	[44C6]
R6F1	RESN_402	[21A8]
R6F2	RESN_402	[21A8]
R6F3	RESN_402	[20D7]
R6F4	RESN_402	[20D7]
R6F5	RESN_402	[20A5]
R6F6	RESN_402	[4A3]
R6G1	RESN_402	[35C6]
R6M1	RESN_805	[42B4]
R6M2	RESN_805	[42B5]
R6M3	RESN_402	[58C6]
R6M4	RESN_402	[58C7]
R6N1	RESN_805	[45D7]
R6N2	RESN_805	[45D5]
R6R1	RESN_402	[12B1]
R6R2	RESN_402	[12B1]
R6T1	RESN_402	[12A3]
R6T2	RESN_402	[12A3]
R6T3	RESN_402	[4A6]
R6T4	RESN_402	[12A7]
R6T5	RESN_402	[12A7]
R6T6	RESN_402	[4A6]
R6T7	RESN_402	[12B5]
R6T8	RESN_402	[12B5]
R6T9	RESN_402	[13B1]
R6U1	RESN_402	[21A5]
R6U2	RESN_402	[21D7]
R6U3	RESN_402	[21D7]
R6U4	RESN_402	[20A8]
R6U5	RESN_402	[20A8]
R7A1	RESN_2512	[38B2]
R7A2	RESN_2512	[38A2]
R7B1	RESN_402	[44B6]
R7B2	RESN_402	[44B6]
R7B3	RESN_402	[44B7]
R7B4	RESN_402	[44B7]
R7B5	RESN_402	[44D6]
R7C1	RESN_402	[44B4]
R7C2	RESN_402	[44A7]
R7C3	RESN_402	[44A5]
R7C4	RESN_402	[44D5]
R7C5	RESN_402	[44B2]
R7C6	RESN_402	[44B4]
R7C7	RESN_402	[44C6]
R7C8	RESN_402	[44B1]
R7C9	RESN_402	[44C6]
R7C10	RESN_402	[44D6]
R7C11	RESN_603	[44D6]
R7C12	RESN_603	[44D6]
R7C13	RESN_402	[44D2]
R7C14	RESN_805	[44A7]
R7C15	RESN_402	[43C5]
R7C16	RESN_402	[43C5]
R7C17	RESN_402	[43C4]
R7C18	RESN_402	[43C4]
R7C19	RESN_402	[43C4]
R7C20	RESN_402	[43C3]
R7D2	RESN_402	[16D7]
R7D3	RESN_402	[16D7]
R7D4	RESN_402	[17A7]
R7D5	RESN_402	[17A7]
R7E1	RESN_402	[16A5]
R7E2	RESN_402	[4A2]
R7E4	RESN_402	[14D7]
R7E5	RESN_402	[14D7]
R7E6	RESN_402	[15A8]
R7E7	RESN_402	[15A8]
R7E8	RESN_402	[14A5]
R7F1	RESN_2512	[50C2]
R7P1	RESN_402	[44A7]
R7P2	RESN_402	[44A6]
R7P3	RESN_402	[43D6]
R7P4	RESN_402	[43D6]
R7P5	RESN_402	[43D6]
R7P6	RESN_402	[43D6]
R7P7	RESN_402	[43D6]
R7P8	RESN_402	[43C6]
R7R1	RESN_402	[17D7]
R7R2	RESN_402	[16A8]
R7R3	RESN_402	[17D7]
R7R4	RESN_402	[16A8]
R7R6	RESN_402	[4A3]
R7T1	RESN_402	[17A5]
R7T2	RESN_402	[15D7]
R7T3	RESN_402	[15D7]
R7T4	RESN_402	[14A7]
R7T5	RESN_402	[14A7]
R7T6	RESN_402	[15A5]
R7T7	RESN_402	[4A3]
RT1B1	THERMISTOR_1206	[38D6]
RT1M1	THERMISTOR_1206	[39B3]
RT1M2	THERMISTOR_1206	[39C3]
RT2M1	THERMISTOR_1206	[39D3]
RT3A1	THERMISTOR_1206	[37D7]
RT3A2	THERMISTOR_1206	[38D6]
RT5A1	THERMISTOR_1206	[41D3]
RT6G1	THERMISTOR_1206	[39D8]
RT7V1	THERMISTOR_1206	[39C8]
ST1F1	SHORT_SM	[48C2]
ST1F2	SHORT_SM	[48B2]
ST1F3	SHORT_SM	[48C2]
ST1U1	SHORT_SM	[48B4]
ST1U2	SHORT_SM	[48C4]
ST2G1	SHORT_SM	[47B3]
ST2G2	SHORT_SM	[47C2]
ST2G3	SHORT_SM	[47C2]
ST2R1	SHORT_SM	[31B7]
ST2R2	SHORT_SM	[31B7]
ST2T1	SHORT_SM	[31A7]
ST2T2	SHORT_SM	[30C8]
ST2U1	SHORT_SM	[47C4]
ST2U2	SHORT_SM	[47B4]
ST3C1	SHORT_SM	[23A6]
ST3C2	SHORT_SM	[23A6]
ST3C3	SHORT_SM	[23A6]
ST3C4	SHORT_SM	[23A6]
ST3C5	SHORT_SM	[23A6]
ST3F1	SHORT_SM	[49C4]
ST3R1	SHORT_SM	[31D7]
ST3T1	SHORT_SM	[30D7]
ST3T2	SHORT_SM	[30A7]
ST4F1	SHORT_TRACE	[49B2]
ST4F2	SHORT_SM	[49C2]
ST4F4	SHORT_SM	[49C2]
ST4U1	SHORT_TRACE	[49B4]
ST5C1	SHORT_SM	[51C2]
ST5C2	SHORT_TRACE	[51B3]
ST5C3	SHORT_SM	[51C2]
ST5R1	SHORT_SM	[6C6]
ST5R2	SHORT_SM	[6C6]
ST5R3	SHORT_SM	[6A6]
ST5R4	SHORT_SM	[6A6]
ST5R5	SHORT_SM	[6B6]
ST5T1	SHORT_SM	[6C6]
ST5T2	SHORT_SM	[6B6]
ST6C1	SHORT_SM	[44B8]
ST6D1	SHORT_SM	[44A8]
ST6D2	SHORT_SM	[44A5]
ST6V1	SHORT_TRACE	[50B4]
ST6V2	SHORT_TRACE	[50C4]
ST7A1	SHORT_SM	[38B2]
ST7A2	SHORT_SM	[38B2]
ST7F1	SHORT_SM	[50B2]
ST7F2	SHORT_SM	[50C2]
ST7F3	SHORT_SM	[50C2]
STP3C1	STP_TP	[61B1]
STP4C1	STP_TP	[61C4]
STP4C2	STP_TP	[61B4]
STP4C3	STP_TP	[61C5]

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STP4C4	STP_TP	[61B4]
STP4C5	STP_TP	[61B5]
STP4C6	STP_TP	[61B5]
STP4E1	STP_TP	[61B7]
STP4E2	STP_TP	[61B7]
STP4E3	STP_TP	[61A8]
STP5B1	STP_TP	[61B1]
STP5B2	STP_TP	[61B1]
STP5D1	STP_TP	[61C7]
STP5D2	STP_TP	[61C7]
STP6C1	STP_TP	[61B7]
STP6C2	STP_TP	[61A7]
STP7B1	STP_TP	[61B1]
STP7C1	STP_TP	[61B1]
STP7C2	STP_TP	[61C1]
STP7C3	STP_TP	[61C1]
STP7C4	STP_TP	[61C1]
STP7C5	STP_TP	[61C1]
STP7C6	STP_TP	[61C1]
STP7C7	STP_TP	[61C1]
STP7E1	STP_TP	[61C7]
STP7E2	STP_TP	[61C7]
STP7N1	STP_TP	[61B1]
U1B1	SI4501DY_SO8	[46C3]
U1C1	NCP1117_DPAK	[52C7]
U1E1	ADP1877_LCC32	[47A6]
U1E1	ADP1877_LCC32	[48A7]
U1E2	NAND_TSOP	[34B3]
U1F1	FET_VREG_DUAL_1_SO-8	[48C4]
U1F2	AD7991_SOT23	[56B3]
U1F3	REF3333_SC70	[56B3]
U1F5	TRSET_9920_TH	[35B1]
U1G2	LM95234_LLP-14	[58B2]
U1G3	TRSET_9920_SMT	[35B1]
U1U1	AD5252_TSSOP	[56C5]
U2D1	ETHERNETPHY_KSZ8041NL_AR8032_QFN	[32A5]
U2N1	BMAX20_LGA12	[35C5]
U2U1	AD8213_MSOP10	[56B5]
U3A5	AUDIODAC_CSS4354_WM1824_QFN25	[33A5]
U3B2	HANA_BGA225	[22C5]
U3B2	HANA_BGA225	[23C4]
U3B2	HANA_BGA225	[24C4]
U3B2	HANA_BGA225	[25B4]
U3D1	SB_BGA	[26C4]
U3D1	SB_BGA	[27C5]
U3D1	SB_BGA	[28C5]
U3D1	SB_BGA	[29C5]
U3D1	SB_BGA	[30C4]
U3D1	SB_BGA	[31B5]
U3E1	AD7992_MSOP10	[58A6]
U3E2	AD5252_TSSOP	[58C4]
U3G1	ADP1877_LCC32	[49A6]
U3G1	ADP1877_LCC32	[50A7]
U3G2	AD7991_SOT23	[55A3]

U3G3	REF3333_SC70	[55B4]
U3G4	ISD2130_QFN21	[35A4]
U3T1	REF3333_SC70	[58B7]
U3V1	AD5252_TSSOP	[55C4]
U3V2	AD8213_MSOP10	[55A5]
U4B1	AD5252_TSSOP	[57A5]
U4B2	AD7992_MSOP10	[57D3]
U4B3	IR3638_SSOP	[51B5]
U4E1	NCP1117_DPAK	[52B7]
U4E2	NCP1117_SOT223	[52D3]
U4R1	LD39015_SOT23-5	[52A3]
U4R2	AT25020A_SOI8	[5C2]
U5A1	SIMPLESWR_SOT23	[53B5]
U5B1	SIMPLESWR_SOT23	[53C5]
U5B2	AD8213_MSOP10	[57C6]
U5B5	MOSDRIVER_SOI8	[45A6]
U5B6	REF3333_SC70	[57D6]
U5E1	VALHALLA_1_BGA_2	[2C4]
U5E1	VALHALLA_1_BGA_2	[3C5]
U5E1	VALHALLA_1_BGA_2	[4A5]
U5E1	VALHALLA_1_BGA_2	[5C5]
U5E1	VALHALLA_1_BGA_2	[6C3]
U5E1	VALHALLA_1_BGA_2	[7B6 7A8 7C8 7B4 7B1]
U5E1	VALHALLA_1_BGA_2	[8B2 8B4 8B7]
U5E1	VALHALLA_1_BGA_2	[12C3 12C7]
U5E1	VALHALLA_1_BGA_2	[13C6 13C3]
U5F1	GDDR136_1GBIT_BGA136	[18C2 18C6]
U5N1	AD7992_MSOP10	[57C4]
U5U1	GDDR136_1GBIT_BGA136	[19C6 19C2]
U5U2	74LVC1G06_SC70	[4A3]
U6A1	INA219_SOT23-8	[58C6]
U6B1	MOSDRIVER_SOI8	[45C6]
U6F1	GDDR136_1GBIT_BGA136	[20C6 20C2]
U6G1	IR_WHOLDER_TH	[35B7]
U6U1	GDDR136_1GBIT_BGA136	[21C6 21C2]
U7C1	NCP4201_LCC40	[44C3]
U7D1	GDDR136_1GBIT_BGA136	[16C2 16B6]
U7E1	GDDR136_1GBIT_BGA136	[14C2 14C6]
U7R1	GDDR136_1GBIT_BGA136	[17B6 17C2]
U7T1	GDDR136_1GBIT_BGA136	[15C6 15C2]
Y3B1	CRYSTAL_SM	[22D8]