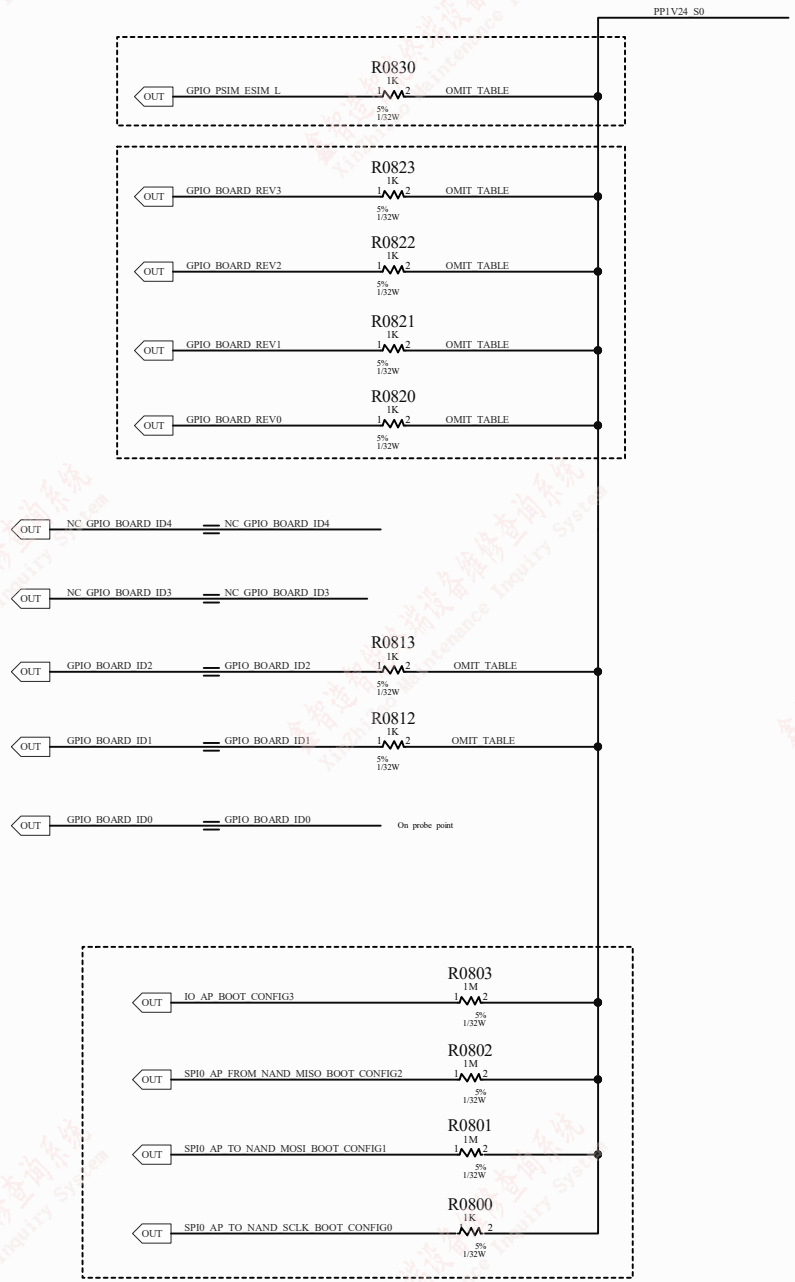

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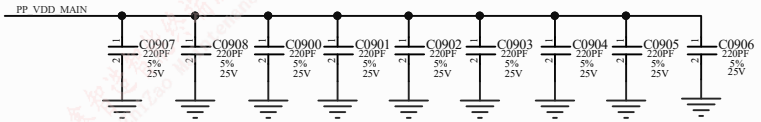
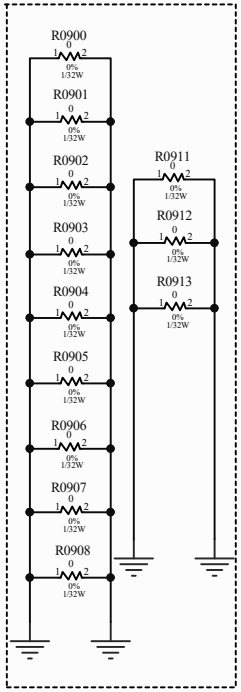


DOTARA UF



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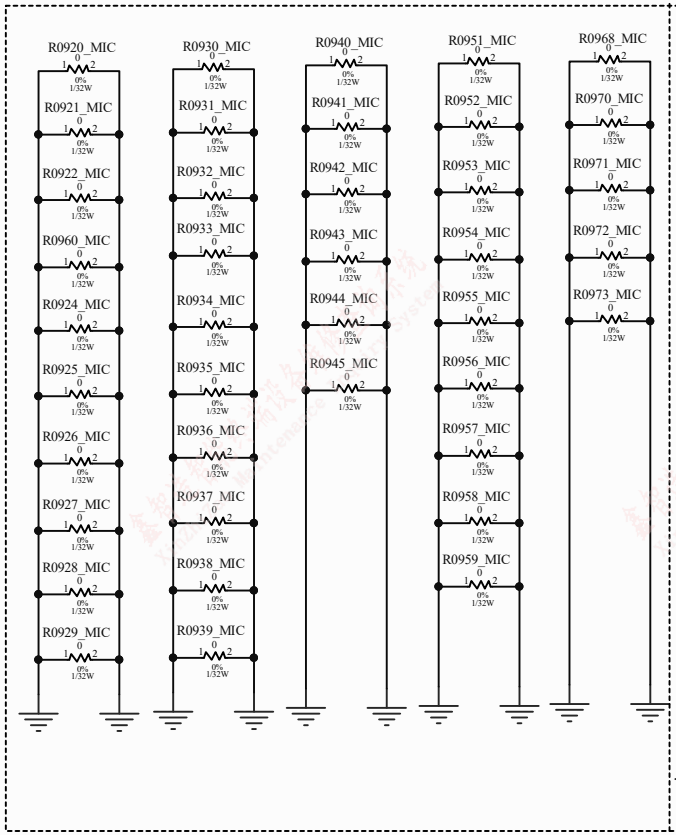

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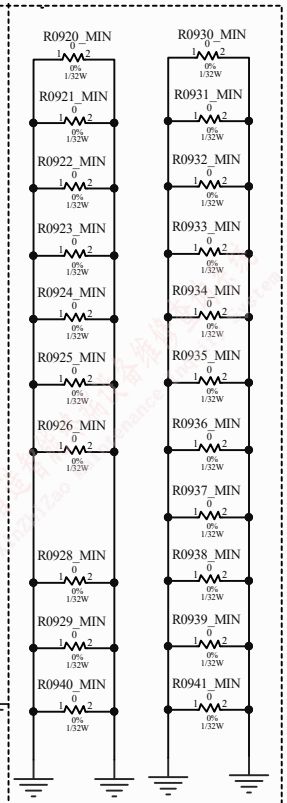

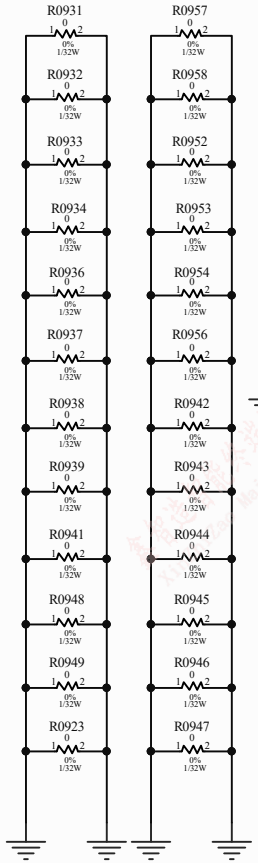

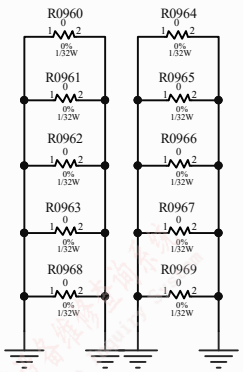

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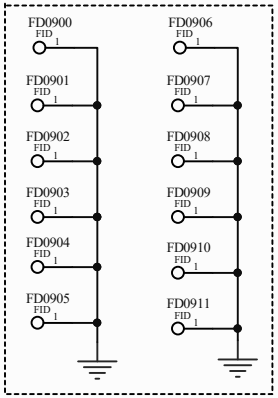
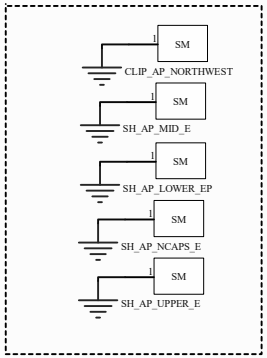
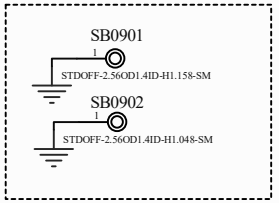


SHIELDS & CLIP



STANDOFFS



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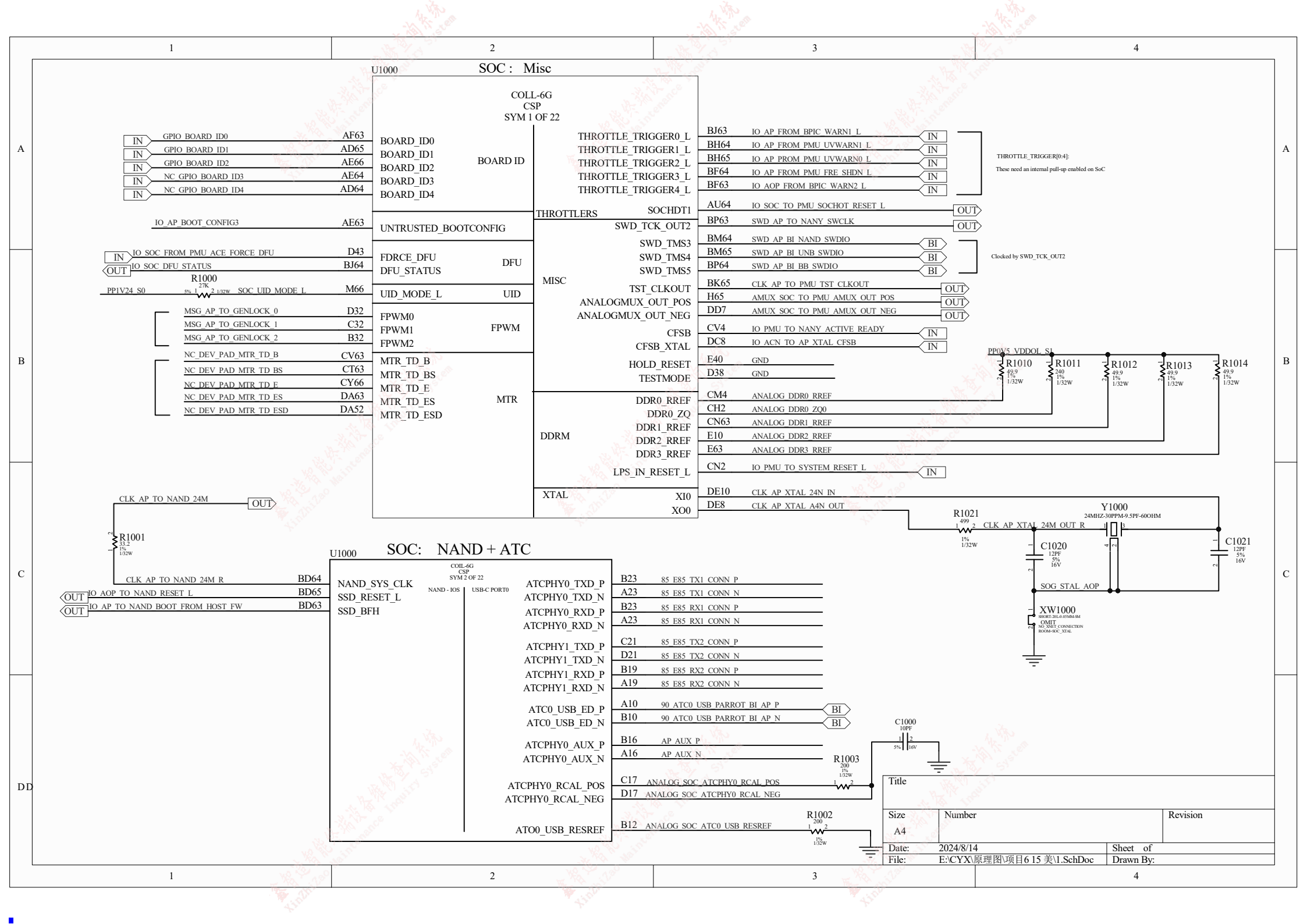
SOC : Misc
U1000
COLL-6G
CSP
SYM 1 OF 22
BOARD ID
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
BOARD_ID4
GPIO_BOARD_ID0
GPIO_BOARD_ID1
GPIO_BOARD_ID2
NC_GPIO_BOARD_ID3
NC_GPIO_BOARD_ID4
AF63
AD65
AE66
AE64
AD64
UNTRUSTED_BOOTCONFIG
IO_AP_BOOT_CONFIG3
AE63
DFU
FDRCE_DFU
DFU_STATUS
IO_SOC_FROM_PMU_ACE_FORCE_DFU
IO_SOC_DFU_STATUS
D43
BJ64
UID
UID_MODE_L
SOC_UID_MODE_L
M66
R1000
27K
PP1V24_S0
FPWM
FPWM0
FPWM1
FPWM2
MSG_AP_TO_GENLOCK_0
MSG_AP_TO_GENLOCK_1
MSG_AP_TO_GENLOCK_2
D32
C32
B32
MTR
MTR_TD_B
MTR_TD_BS
MTR_TD_E
MTR_TD_ES
MTR_TD_ESD
NC_DEV_PAD_MTR_TD_B
NC_DEV_PAD_MTR_TD_BS
NC_DEV_PAD_MTR_TD_E
NC_DEV_PAD_MTR_TD_ES
NC_DEV_PAD_MTR_TD_ESD
CV63
CT63
CY66
DA63
DA52
THROTTLERS
THROTTLE_TRIGGER0_L
THROTTLE_TRIGGER1_L
THROTTLE_TRIGGER2_L
THROTTLE_TRIGGER3_L
THROTTLE_TRIGGER4_L
BJ63
BH64
BH65
BF64
BF63
IO_AP_FROM_BPIC_WARN1_L
IO_AP_FROM_PMU_UVWARN1_L
IO_AP_PROM_PMU_UVWARN0_L
IO_AP_FROM_PMU_FRE_SHDN_L
IO_AOP_FROM_BPIC_WARN2_L
THROTTLE_TRIGGER[0:4]:
These need an internal pull-up enabled on SoC
SOCHDT1
AU64
IO_SOC_TO_PMU_SOCHOT_RESET_L
SWD_TCK_OUT2
BP63
SWD_AP_TO_NANY_SWCLK
MISC
SWD_TMS3
SWD_TMS4
SWD_TMS5
BM64
BM65
BP64
SWD_AP_BI_NAND_SWDIO
SWD_AP_BI_UNB_SWDIO
SWD_AP_BI_BB_SWDIO
Clocked by SWD_TCK_OUT2
TST_CLKOUT
ANALOGMUX_OUT_POS
ANALOGMUX_OUT_NEG
BK65
H65
DD7
CLK_AP_TO_PMU_TST_CLKOUT
AMUX_SOC_TO_PMU_AMUX_OUT_POS
AMUX_SOC_TO_PMU_AMUX_OUT_NEG
CFSB
CFSB_XTAL
CV4
DC8
IO_PMU_TO_NANY_ACTIVE_READY
IO_ACN_TO_AP_XTAL_CFSB
HOLD_RESET
TESTMODE
E40
D38
GND
GND
DDRM
DDR0_RREF
DDR0_ZQ
DDR1_RREF
DDR2_RREF
DDR3_RREF
CM4
CH2
CN63
E10
E63
ANALOG_DDR0_RREF
ANALOG_DDR0_ZQ0
ANALOG_DDR1_RREF
ANALOG_DDR2_RREF
ANALOG_DDR3_RREF
LPS_IN_RESET_L
CN2
IO_PMU_TO_SYSTEM_RESET_L
PP0V5_VDDQL_S1
R1010
R1011
R1012
R1013
R1014
49.9
240
XTAL
XI0
XO0
DE10
DE8
CLK_AP_XTAL_24N_IN
CLK_AP_XTAL_A4N_OUT
R1021
499
CLK_AP_XTAL_24M_OUT_R
Y1000
24MHZ-30PPM-9.5PF-60OHM
C1020
C1021
12PF
SOG_STAL_AOP
XW1000
OMIT
CLK_AP_TO_NAND_24M
R1001
33.2
SOC: NAND + ATC
U1000
COIL-6G
CSP
SYM 2 OF 22
NAND - IOS
USB-C PORT0
NAND_SYS_CLK
SSD_RESET_L
SSD_BFH
CLK_AP_TO_NAND_24M_R
IO_AOP_TO_NAND_RESET_L
IO_AP_TO_NAND_BOOT_FROM_HOST_FW
BD64
BD65
BD63
ATCPHY0_TXD_P
ATCPHY0_TXD_N
ATCPHY0_RXD_P
ATCPHY0_RXD_N
ATCPHY1_TXD_P
ATCPHY1_TXD_N
ATCPHY1_RXD_P
ATCPHY1_RXD_N
ATC0_USB_ED_P
ATC0_USB_ED_N
ATCPHY0_AUX_P
ATCPHY0_AUX_N
ATCPHY0_RCAL_POS
ATCPHY0_RCAL_NEG
ATO0_USB_RESREF
B23
A23
B23
A23
C21
D21
B19
A19
A10
B10
B16
A16
C17
D17
B12
85_E85_TX1_CONN_P
85_E85_TX1_CONN_N
85_E85_RX1_CONN_P
85_E85_RX1_CONN_N
85_E85_TX2_CONN_P
85_E85_TX2_CONN_N
85_E85_RX2_CONN_P
85_E85_RX2_CONN_N
90_ATC0_USB_PARROT_BI_AP_P
90_ATC0_USB_PARROT_BI_AP_N
AP_AUX_P
AP_AUX_N
ANALOG_SOC_ATCPHY0_RCAL_POS
ANALOG_SOC_ATCPHY0_RCAL_NEG
ANALOG_SOC_ATC0_USB_RESREF
C1000
10PF
R1003
200
R1002
200
Title
Size
A4
Number
Revision
Date:
2024/8/14
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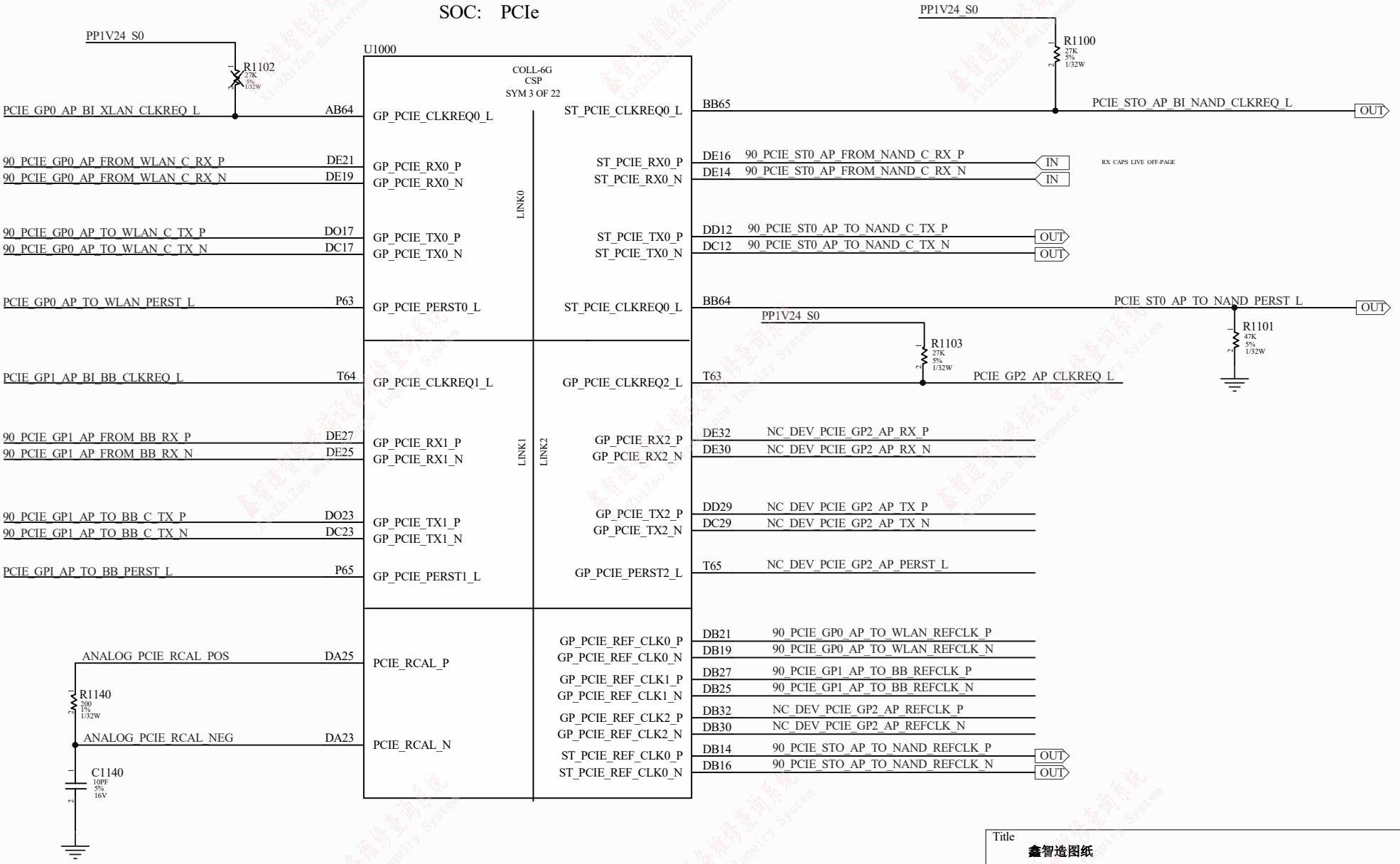
Drawn By:

SOC: PCIe



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File: E:\CYX\原理图\项目6 15 美\2.SchDoc		Drawn By:

SOC: ISP

U1000

COLL-6G
CSP
SYM 4 OF 22

IN	90_LPDP_ISP_FROM_FCAM_RX_D0_P	DD42	LPDPRX_RX_D0_P		
IN	90_LPDP_ISP_FROM_FCAM_RX_D0_N	DC42	LPDPRX_RX_D0_N		
IN	90_LPDP_ISP_FROM_FCAM_RX_D1_P	DE43	LPDPRX_RX_D1_P		
IN	90_LPDP_ISP_FROM_FCAM_RX_D1_N	DD43	LPDPRX_RX_D1_N		
IN	90_LPDP_ISP_FROM_TELE_RX_D0_P	DD45	LPDPRX_RX_D2_P		
IN	90_LPDP_ISP_FROM_TELE_RX_D0_N	DC45	LPDPRX_RX_D2_N		
IN	90_LPDP_ISP_FROM_SWIDE_RX_D2_N	DC49	LPDPRX_RX_D3_P		
IN	90_LPDP_ISP_FROM_SWIDE_RX_D2_P	DD49	LPDPRX_RX_D3_N		
IN	90_LPDP_ISP_FROM_SWIDE_RX_D0_N	DD51	LPDPRX_RX_D4_P		
IN	90_LPDP_ISP_FROM_SWIDE_RX_D0_P	DE51	LPDPRX_RX_D4_N		
IN	90_LPDP_ISP_FROM_SWIDE_RX_D1_N	DC53	LPDPRX_RX_D5_P		
IN	90_LPDP_ISP_FROM_SWIDE_RX_D1_P	DD53	LPDPRX_RX_D5_N		
IN	90_LPDP_ISP_FROM_TELE_RX_D1_N	DD55	LPDPRX_RX_D6_P		
IN	90_LPDP_ISP_FROM_TELE_RX_D1_P	DE55	LPDPRX_RX_D6_N		
IN	90_LPDP_ISP_FROM_TELE_RX_D2_N	DC56	LPDPRX_RX_D7_P		
IN	90_LPDP_ISP_FROM_TELE_RX_D2_P	DD56	LPDPRX_RX_D7_N		
IN	90_LPDP_ISP_FROM_TELE_RX_D3_N	DD58	LPDPRX_RX_D8_P		
IN	90_LPDP_ISP_FROM_TELE_RX_D3_P	DE58	LPDPRX_RX_D8_N		
IN	90_LPDP_ISP_FROM_WIDE_RX_D0_P	DD61	LPDPRX_RX_D9_P		
IN	90_LPDP_ISP_FROM_WIDE_RX_D0_N	DE61	LPDPRX_RX_D9_N		
IN	90_LPDP_ISP_FROM_WIDE_RX_D1_N	DC62	LPDPRX_RX_D10_P		
IN	90_LPDP_ISP_FROM_WIDE_RX_D1_P	DD62	LPDPRX_RX_D10_N		
IN	90_LPDP_ISP_FROM_RDEPTH_RX_D0_P	DD63	LPDPRX_RX_D11_P		
IN	90_LPDP_ISP_FROM_RDEPTH_RX_D0_N	DE63	LPDPRX_RX_D11_N		
	ANALOG_LPDP_ISP_RX0_RCAL_POS	DE47	LPDPRX0_RCAL_POS		
	ANALOG_LPDP_ISP_RX0_RCAL_NEG	DD47	LPDPRX0_RCAL_NEG		
	ANALOG_LPDP_ISP_RX1_RCAL_POS	DD60	LPDPRX1_RCAL_POS		
	ANALOG_LPDP_ISP_RX1_RCAL_NEG	DC60	LPDPRX1_RCAL_NEG		
BI	NC_LPDP_ISP_AUX_RX_D0P	DA42	LPDPRX_AUX_D0_P		
BI	NC_LPDP_ISP_AUX_RX_D1P	DB43	LPDPRX_AUX_D1_P		
BI	NC_LPDP_ISP_AUX_RX_D2P	DA45	LPDPRX_AUX_D2_P		
BI	NC_LPDP_ISP_AUX_RX_D3P	DB47	LPDPRX_AUX_D3_P		
BI	NC_LPDP_ISP_AUX_RX_D4P	DA49	LPDPRX_AUX_D4_P		
BI	NC_LPDP_ISP_AUX_RX_D5P	DB51	LPDPRX_AUX_D5_P		
BI	NC_LPDP_ISP_AUX_RX_D6P	DB55	LPDPRX_AUX_D6_P		
BI	NC_LPDP_ISP_AUX_RX_D7P	DA53	LPDPRX_AUX_D7_P		
BI	NC_LPDP_ISP_AUX_RX_D8P	DA56	LPDPRX_AUX_D8_P		
BI	NC_LPDP_ISP_AUX_RX_D9P	DB58	LPDPRX_AUX_D9_P		
BI	NC_LPDP_ISP_AUX_RX_D10P	DA60	LPDPRX_AUX_D10_P		
BI	NC_LPDP_ISP_AUX_RX_D11P	DB61	LPDPRX_AUX_D11_P		

LPDP-RX

MIPI-C

MIPIC0_CLK_P	DB38	90_MIPI_ISP_FROM_IRCAM_CLK_P	IN
MIPIC0_CLK_N	DA38	90_MIPI_ISP_FROM_IRCAM_CLK_N	IN
MIPIC0_DATA0_P	DD38	90_MIPI_ISP_FROM_IRCAM_D0_P	IN
MIPIC0_DATA0_N	DE38	90_MIPI_ISP_FROM_IRCAM_D0_N	IN
MIPIC0_DATA1_P	DD35	90_MIPI_ISP_FROM_IRCAM_D1_P	IN
MIPIC0_DATA1_N	DE36	90_MIPI_ISP_FROM_IRCAM_D1_N	IN
MIPIC0_REXT	DA36	ANALOG_MIPI_ISP_REXT	

R1250 200 1% 1/32W

I2C

ISP_I2C0_SCL	BY63	NC_I2C0_ISP_SCL	
ISP_I2C0_SDA	CA55	NC_I2C0_ISP_SDA	
ISP_I2C1_SCL	CA64	NC_I2C1_ISP_SCL	
ISP_I2C1_SDA	CA63	NC_I2C1_ISP_SDA	

PP (dev board only)

ISP_SPMI

GPIO

ISP_GPIO_0	AT65	GPIO_ISP_TO_CAM_PMU1_CAM_PMU2_RESET_L	OUT
ISP_GPIO_1	AT64	NC_ISP_GPIO_1	
ISP_GPIO_2	AT63	GPIO_ISP_TO_GENLOCK_LS_DIR	
ISP_GPIO_3	AP65	GPIO_ISP_CAMS_TO_STROBE_ACE_FLASH_TRIG	IN

SENSOR CLK

SENSOR0_CLK	C40	CLK_ISP_TO_CAM_PMU1_24M_R	R1240 33.2 1% 1/32W	CLK_ISP_TO_CAM_PMU1_24M	OUT
SENSOR1_CLK	C38	CLK_ISP_TO_CAM_PMU2_24M_R	R1260 33.2 1% 1/32W	CLK_ISP_TO_CAM_PMU2_24M	OUT

R1200 200 1% 1/32W

C1200 10PF 5% 16V

R1210 200 1% 1/32W

C1210 10PF 5% 16V

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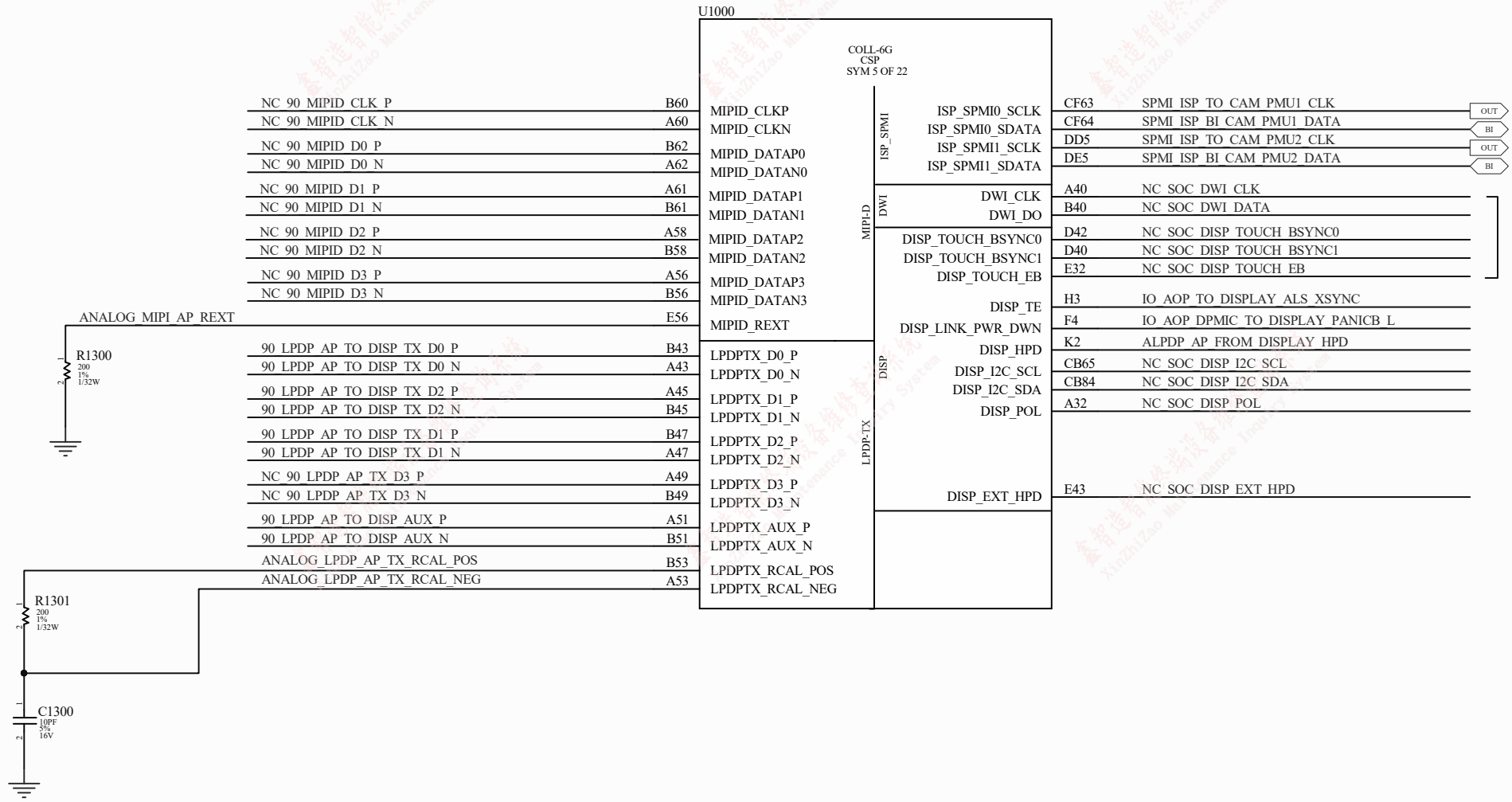

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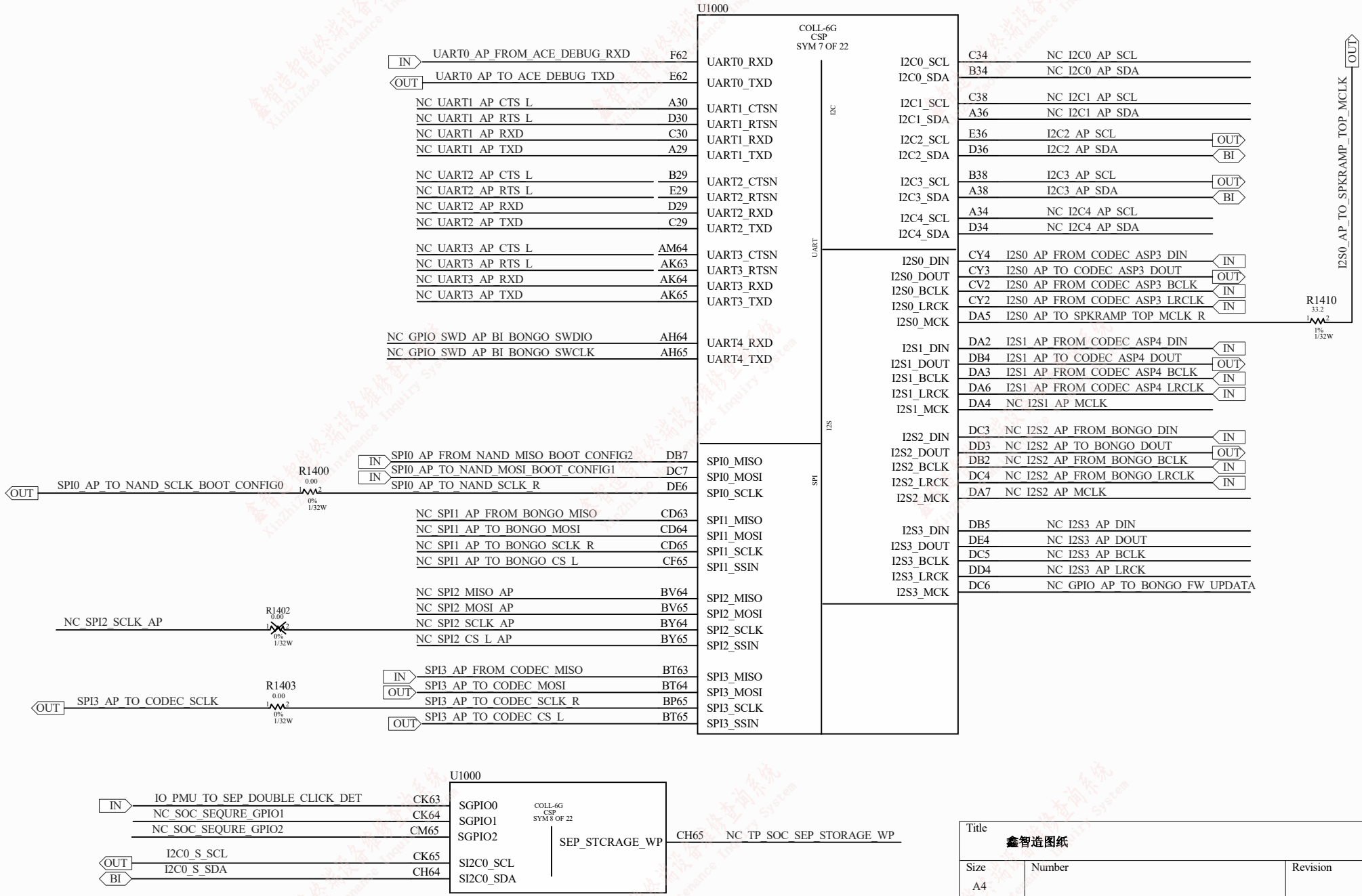
U1000
COLL-6G
CSP
SYM 7 OF 22
UART0_AP_FROM_ACE_DEBUG_RXD F62
UART0_AP_TO_ACE_DEBUG_TXD E62
NC_UART1_AP_CTS_L A30
NC_UART1_AP_RTS_L D30
NC_UART1_AP_RXD C30
NC_UART1_AP_TXD A29
NC_UART2_AP_CTS_L B29
NC_UART2_AP_RTS_L E29
NC_UART2_AP_RXD D29
NC_UART2_AP_TXD C29
NC_UART3_AP_CTS_L AM64
NC_UART3_AP_RTS_L AK63
NC_UART3_AP_RXD AK64
NC_UART3_AP_TXD AK65
NC_GPIO_SWD_AP_BI_BONGO_SWDIO AH64
NC_GPIO_SWD_AP_BI_BONGO_SWCLK AH65
UART0_RXD
UART0_TXD
UART1_CTSN
UART1_RTSN
UART1_RXD
UART1_TXD
UART2_CTSN
UART2_RTSN
UART2_RXD
UART2_TXD
UART3_CTSN
UART3_RTSN
UART3_RXD
UART3_TXD
UART4_RXD
UART4_TXD
I2C
UART
I2S
SPI
I2C0_SCL C34 NC_I2C0_AP_SCL
I2C0_SDA B34 NC_I2C0_AP_SDA
I2C1_SCL C38 NC_I2C1_AP_SCL
I2C1_SDA A36 NC_I2C1_AP_SDA
I2C2_SCL E36 I2C2_AP_SCL
I2C2_SDA D36 I2C2_AP_SDA
I2C3_SCL B38 I2C3_AP_SCL
I2C3_SDA A38 I2C3_AP_SDA
I2C4_SCL A34 NC_I2C4_AP_SCL
I2C4_SDA D34 NC_I2C4_AP_SDA
I2S0_DIN CY4 I2S0_AP_FROM_CODEC_ASP3_DIN
I2S0_DOUT CY3 I2S0_AP_TO_CODEC_ASP3_DOUT
I2S0_BCLK CV2 I2S0_AP_FROM_CODEC_ASP3_BCLK
I2S0_LRCK CY2 I2S0_AP_FROM_CODEC_ASP3_LRCLK
I2S0_MCK DA5 I2S0_AP_TO_SPKRAMP_TOP_MCLK_R
I2S1_DIN DA2 I2S1_AP_FROM_CODEC_ASP4_DIN
I2S1_DOUT DB4 I2S1_AP_TO_CODEC_ASP4_DOUT
I2S1_BCLK DA3 I2S1_AP_FROM_CODEC_ASP4_BCLK
I2S1_LRCK DA6 I2S1_AP_FROM_CODEC_ASP4_LRCLK
I2S1_MCK DA4 NC_I2S1_AP_MCLK
I2S2_DIN DC3 NC_I2S2_AP_FROM_BONGO_DIN
I2S2_DOUT DD3 NC_I2S2_AP_TO_BONGO_DOUT
I2S2_BCLK DB2 NC_I2S2_AP_FROM_BONGO_BCLK
I2S2_LRCK DC4 NC_I2S2_AP_FROM_BONGO_LRCLK
I2S2_MCK DA7 NC_I2S2_AP_MCLK
I2S3_DIN DB5 NC_I2S3_AP_DIN
I2S3_DOUT DE4 NC_I2S3_AP_DOUT
I2S3_BCLK DC5 NC_I2S3_AP_BCLK
I2S3_LRCK DD4 NC_I2S3_AP_LRCK
I2S3_MCK DC6 NC_GPIO_AP_TO_BONGO_FW_UPDATA
I2S0_AP_TO_SPKRAMP_TOP_MCLK
R1410 33.2 1% 1/32W
SPI0_AP_FROM_NAND_MISO_BOOT_CONFIG2 DB7
SPI0_AP_TO_NAND_MOSI_BOOT_CONFIG1 DC7
SPI0_AP_TO_NAND_SCLK_R DE6
SPI0_AP_TO_NAND_SCLK_BOOT_CONFIG0
R1400 0.00 0% 1/32W
NC_SPI1_AP_FROM_BONGO_MISO CD63
NC_SPI1_AP_TO_BONGO_MOSI CD64
NC_SPI1_AP_TO_BONGO_SCLK_R CD65
NC_SPI1_AP_TO_BONGO_CS_L CF65
NC_SPI2_MISO_AP BV64
NC_SPI2_MOSI_AP BV65
NC_SPI2_SCLK_AP BY64
NC_SPI2_CS_L_AP BY65
NC_SPI2_SCLK_AP
R1402 0.00 0% 1/32W
SPI3_AP_FROM_CODEC_MISO BT63
SPI3_AP_TO_CODEC_MOSI BT64
SPI3_AP_TO_CODEC_SCLK_R BP65
SPI3_AP_TO_CODEC_CS_L BT65
SPI3_AP_TO_CODEC_SCLK
R1403 0.00 0% 1/32W
SPI0_MISO
SPI0_MOSI
SPI0_SCLK
SPI1_MISO
SPI1_MOSI
SPI1_SCLK
SPI1_SSIN
SPI2_MISO
SPI2_MOSI
SPI2_SCLK
SPI2_SSIN
SPI3_MISO
SPI3_MOSI
SPI3_SCLK
SPI3_SSIN
U1000
COLL-6G
CSP
SYM 8 OF 22
IO_PMU_TO_SEP_DOUBLE_CLICK_DET CK63
NC_SOC_SEQURE_GPIO1 CK64
NC_SOC_SEQURE_GPIO2 CM65
I2C0_S_SCL CK65
I2C0_S_SDA CH64
SGPIO0
SGPIO1
SGPIO2
SI2C0_SCL
SI2C0_SDA
SEP_STCRAGE_WP
CH65 NC_TP_SOC_SEP_STORAGE_WP
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Revision
Date: 2024/8/14
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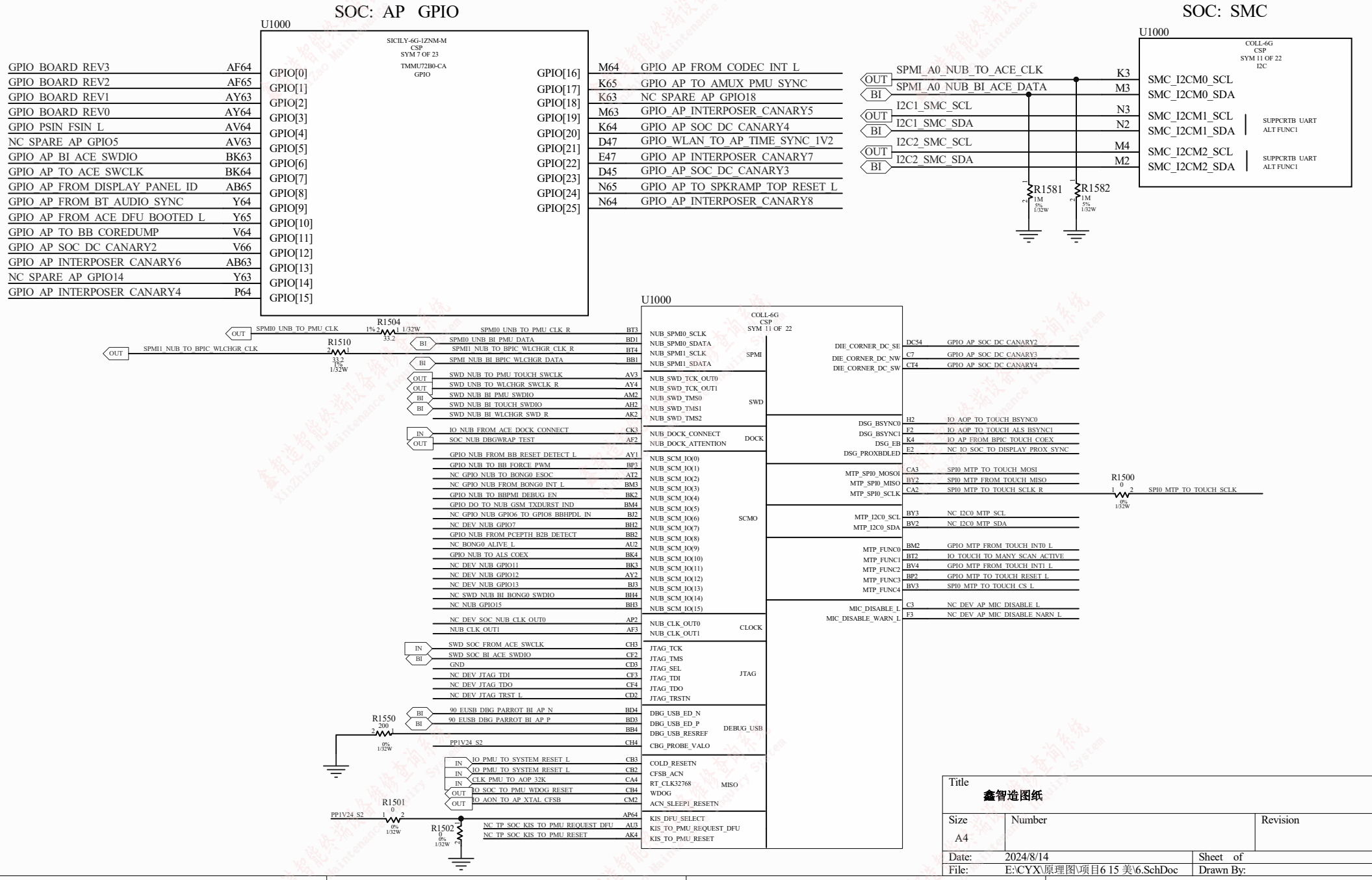
SOC: AP GPIO
U1000
SICILY-6G-IZNM-M
CSP
SYM 7 OF 23
TMMU72B0-CA
GPIO
GPIO_BOARD_REV3 AF64
GPIO_BOARD_REV2 AF65
GPIO_BOARD_REV1 AY63
GPIO_BOARD_REV0 AY64
GPIO_PSIN_FSIN_L AV64
NC_SPARE_AP_GPIO5 AV63
GPIO_AP_BI_ACE_SWDIO BK63
GPIO_AP_TO_ACE_SWCLK BK64
GPIO_AP_FROM_DISPLAY_PANEL_ID AB65
GPIO_AP_FROM_BT_AUDIO_SYNC Y64
GPIO_AP_FROM_ACE_DFU_BOOTED_L Y65
GPIO_AP_TO_BB_COREDUMP V64
GPIO_AP_SOC_DC_CANARY2 V66
GPIO_AP_INTERPOSER_CANARY6 AB63
NC_SPARE_AP_GPIO14 Y63
GPIO_AP_INTERPOSER_CANARY4 P64
GPIO[0] GPIO[1] GPIO[2] GPIO[3] GPIO[4] GPIO[5] GPIO[6] GPIO[7] GPIO[8] GPIO[9] GPIO[10] GPIO[11] GPIO[12] GPIO[13] GPIO[14] GPIO[15]
GPIO[16] GPIO[17] GPIO[18] GPIO[19] GPIO[20] GPIO[21] GPIO[22] GPIO[23] GPIO[24] GPIO[25]
M64 GPIO_AP_FROM_CODEC_INT_L
K65 GPIO_AP_TO_AMUX_PMU_SYNC
K63 NC_SPARE_AP_GPIO18
M63 GPIO_AP_INTERPOSER_CANARY5
K64 GPIO_AP_SOC_DC_CANARY4
D47 GPIO_WLAN_TO_AP_TIME_SYNC_1V2
E47 GPIO_AP_INTERPOSER_CANARY7
D45 GPIO_AP_SOC_DC_CANARY3
N65 GPIO_AP_TO_SPKRAMP_TOP_RESET_L
N64 GPIO_AP_INTERPOSER_CANARY8
SOC: SMC
U1000
COLL-6G
CSP
SYM 11 OF 22
I2C
OUT SPMI_A0_NUB_TO_ACE_CLK K3
BI SPMI_A0_NUB_BI_ACE_DATA M3
OUT I2C1_SMC_SCL N3
BI I2C1_SMC_SDA N2
OUT I2C2_SMC_SCL M4
BI I2C2_SMC_SDA M2
SMC_I2CM0_SCL
SMC_I2CM0_SDA
SMC_I2CM1_SCL
SMC_I2CM1_SDA
SUPPCRTB UART
ALT FUNC1
SMC_I2CM2_SCL
SMC_I2CM2_SDA
SUPPCRTB UART
ALT FUNC1
R1581 1M 5% 1/32W
R1582 1M 5% 1/32W
U1000
COLL-6G
CSP
SYM 11 OF 22
SPMI
SWD
DOCK
SCMO
CLOCK
JTAG
DEBUG_USB
MISO
R1504 33.2 1% 1/32W
R1510 33.2 1% 1/32W
R1550 200 0% 1/32W
R1501 0 0% 1/32W
R1502 0 0% 1/32W
R1500 0 0% 1/32W
SPMI0_UNB_TO_PMU_CLK
SPMI1_NUB_TO_BPIC_WLCHGR_CLK
SPMI0_UNB_TO_PMU_CLK_R BT3
SPMI0_UNB_BI_PMU_DATA BD1
SPMI1_NUB_TO_BPIC_WLCHGR_CLK_R BT4
SPMI_NUB_BI_BPIC_WLCHGR_DATA BB1
SWD_NUB_TO_PMU_TOUCH_SWCLK AV3
SWD_UNB_TO_WLCHGR_SWCLK_R AY4
SWD_NUB_BI_PMU_SWDIO AM2
SWD_NUB_BI_TOUCH_SWDIO AH2
SWD_NUB_BI_WLCHGR_SWD_R AK2
IO_NUB_FROM_ACE_DOCK_CONNECT CK3
SOC_NUB_DBGWRAP_TEST AF2
GPIO_NUB_FROM_BB_RESET_DETECT_L AY1
GPIO_NUB_TO_BB_FORCE_PWM BP3
NC_GPIO_NUB_TO_BONG0_ESOC AT2
NC_GPIO_NUB_FROM_BONG0_INT_L BM3
GPIO_NUB_TO_BBPMI_DEBUG_EN BK2
GPIO_DO_TO_NUB_GSM_TXDURST_IND BM4
NC_GPIO_NUB_GPIO6_TO_GPIO8_BBHPDL_IN BJ2
NC_DEV_NUB_GPIO7 BH2
GPIO_NUB_FROM_PCEPTH_B2B_DETECT BB2
NC_BONG0_ALIVE_L AU2
GPIO_NUB_TO_ALS_COEX BK4
NC_DEV_NUB_GPIO11 BK3
NC_DEV_NUB_GPIO12 AY2
NC_DEV_NUB_GPIO13 BJ3
NC_SWD_NUB_BI_BONG0_SWDIO BH4
NC_NUB_GPIO15 BH3
NC_DEV_SOC_NUB_CLK_OUT0 AP2
NUB_CLK_OUT1 AF3
SWD_SOC_FROM_ACE_SWCLK CH3
SWD_SOC_BI_ACE_SWDIO CF2
GND CD3
NC_DEV_JTAG_TDI CF3
NC_DEV_JTAG_TDO CF4
NC_DEV_JTAG_TRST_L CD2
90_EUSB_DBG_PARROT_BI_AP_N BD4
90_EUSB_DBG_PARROT_BI_AP_P BD3
BB4
PP1V24_S2 CH4
IO_PMU_TO_SYSTEM_RESET_L CB3
IO_PMU_TO_SYSTEM_RESET_L CB2
CLK_PMU_TO_AOP_32K CA4
IO_SOC_TO_PMU_WDOG_RESET CB4
IO_AON_TO_AP_XTAL_CFSB CM2
PP1V24_S2 AP64
NC_TP_SOC_KIS_TO_PMU_REQUEST_DFU AU3
NC_TP_SOC_KIS_TO_PMU_RESET AK4
NUB_SPMI0_SCLK
NUB_SPMI0_SDATA
NUB_SPMI1_SCLK
NUB_SPMI1_SDATA
NUB_SWD_TCK_OUT0
NUB_SWD_TCK_OUT1
NUB_SWD_TMS0
NUB_SWD_TMS1
NUB_SWD_TMS2
NUB_DOCK_CONNECT
NUB_DOCK_ATTENTION
NUB_SCM_IO(0)
NUB_SCM_IO(1)
NUB_SCM_IO(2)
NUB_SCM_IO(3)
NUB_SCM_IO(4)
NUB_SCM_IO(5)
NUB_SCM_IO(6)
NUB_SCM_IO(7)
NUB_SCM_IO(8)
NUB_SCM_IO(9)
NUB_SCM_IO(10)
NUB_SCM_IO(11)
NUB_SCM_IO(12)
NUB_SCM_IO(13)
NUB_SCM_IO(14)
NUB_SCM_IO(15)
NUB_CLK_OUT0
NUB_CLK_OUT1
JTAG_TCK
JTAG_TMS
JTAG_SEL
JTAG_TDI
JTAG_TDO
JTAG_TRSTN
DBG_USB_ED_N
DBG_USB_ED_P
DBG_USB_RESREF
CBG_PROBE_VALO
COLD_RESETN
CFSB_ACN
RT_CLK32768
WDOG
ACN_SLEEP1_RESETN
KIS_DFU_SELECT
KIS_TO_PMU_REQUEST_DFU
KIS_TO_PMU_RESET
DIE_CORNER_DC_SE DC54 GPIO_AP_SOC_DC_CANARY2
DIE_CORNER_DC_NW C7 GPIO_AP_SOC_DC_CANARY3
DIE_CORNER_DC_SW CT4 GPIO_AP_SOC_DC_CANARY4
DSG_BSYNC0 H2 IO_AOP_TO_TOUCH_BSYNC0
DSG_BSYNC1 F2 IO_AOP_TO_TOUCH_ALS_BSYNC1
DSG_EB K4 IO_AP_FROM_BPIC_TOUCH_COEX
DSG_PROXBDLED E2 NC_IO_SOC_TO_DISPLAY_PROX_SYNC
MTP_SPI0_MOSOI CA3 SPI0_MTP_TO_TOUCH_MOSI
MTP_SPI0_MISO BY2 SPI0_MTP_FROM_TOUCH_MISO
MTP_SPI0_SCLK CA2 SPI0_MTP_TO_TOUCH_SCLK_R
SPI0_MTP_TO_TOUCH_SCLK
MTP_I2C0_SCL BY3 NC_I2C0_MTP_SCL
MTP_I2C0_SDA BV2 NC_I2C0_MTP_SDA
MTP_FUNC0 BM2 GPIO_MTP_FROM_TOUCH_INT0_L
MTP_FUNC1 BT2 IO_TOUCH_TO_MANY_SCAN_ACTIVE
MTP_FUNC2 BV4 GPIO_MTP_FROM_TOUCH_INT1_L
MTP_FUNC3 BP2 GPIO_MTP_TO_TOUCH_RESET_L
MTP_FUNC4 BV3 SPI0_MTP_TO_TOUCH_CS_L
MIC_DISABLE_L C3 NC_DEV_AP_MIC_DISABLE_L
MIC_DISABLE_WARN_L F3 NC_DEV_AP_MIC_DISABLE_NARN_L
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鑫智造图纸
Size A4
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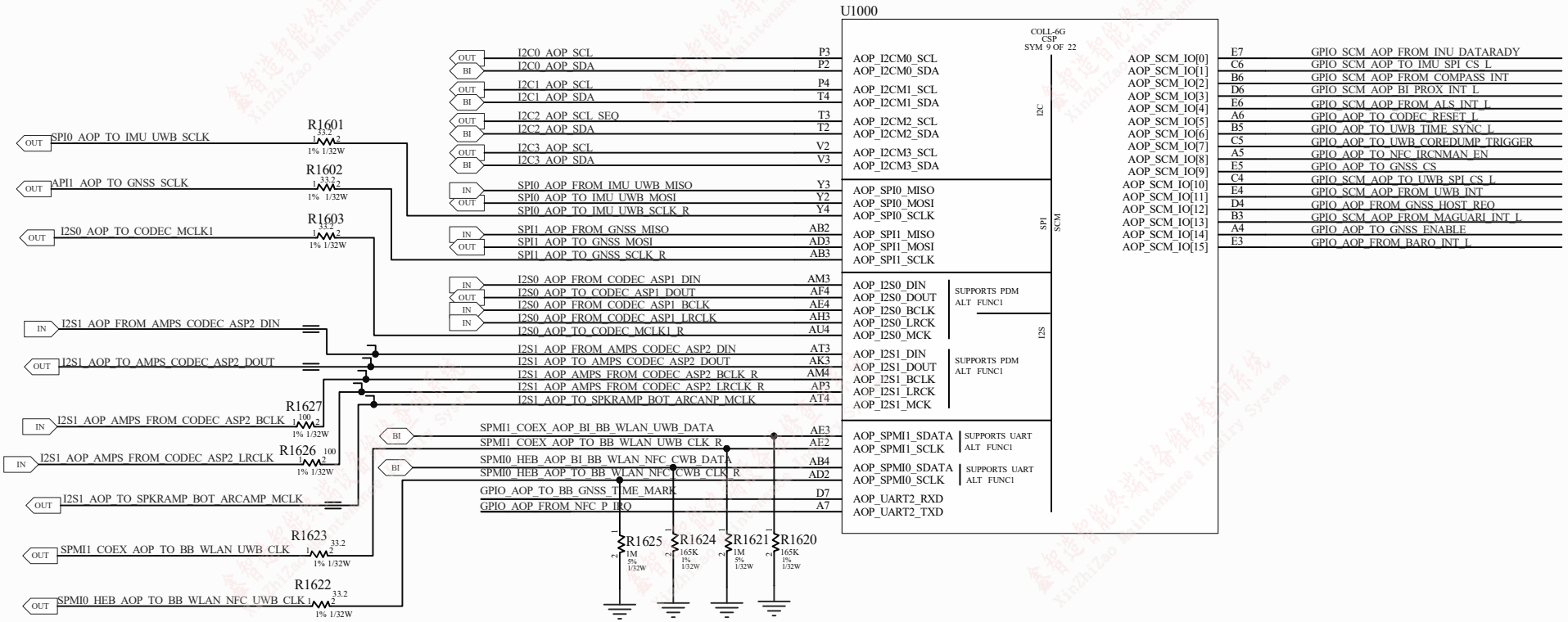

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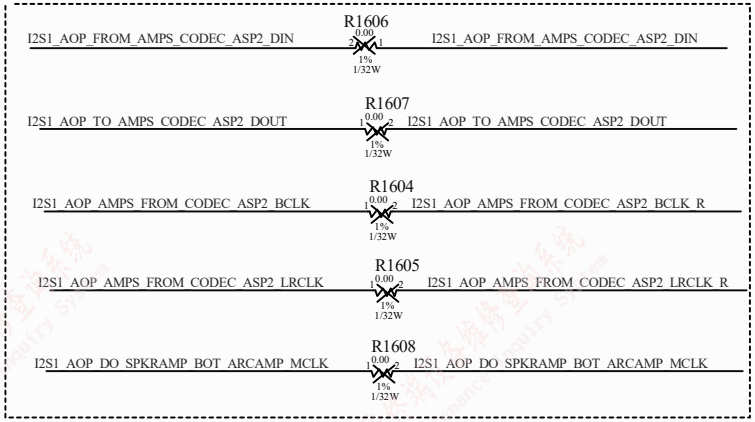

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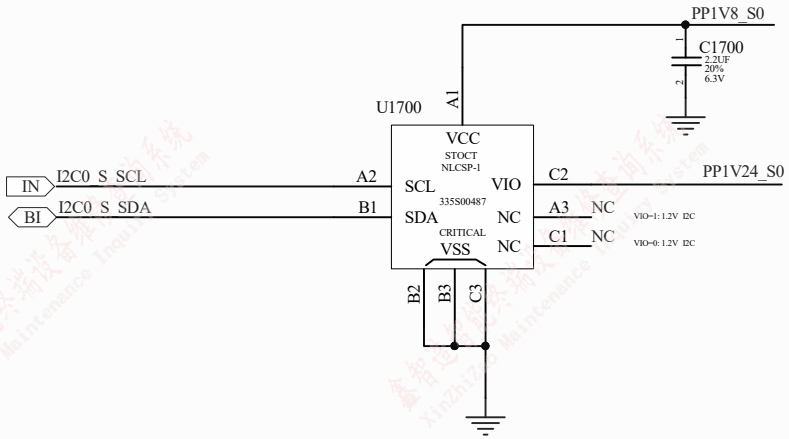
鑫智造智能终端设备维修查询系统 Xinzhizao Maintenance Inquiry System

OCELOT



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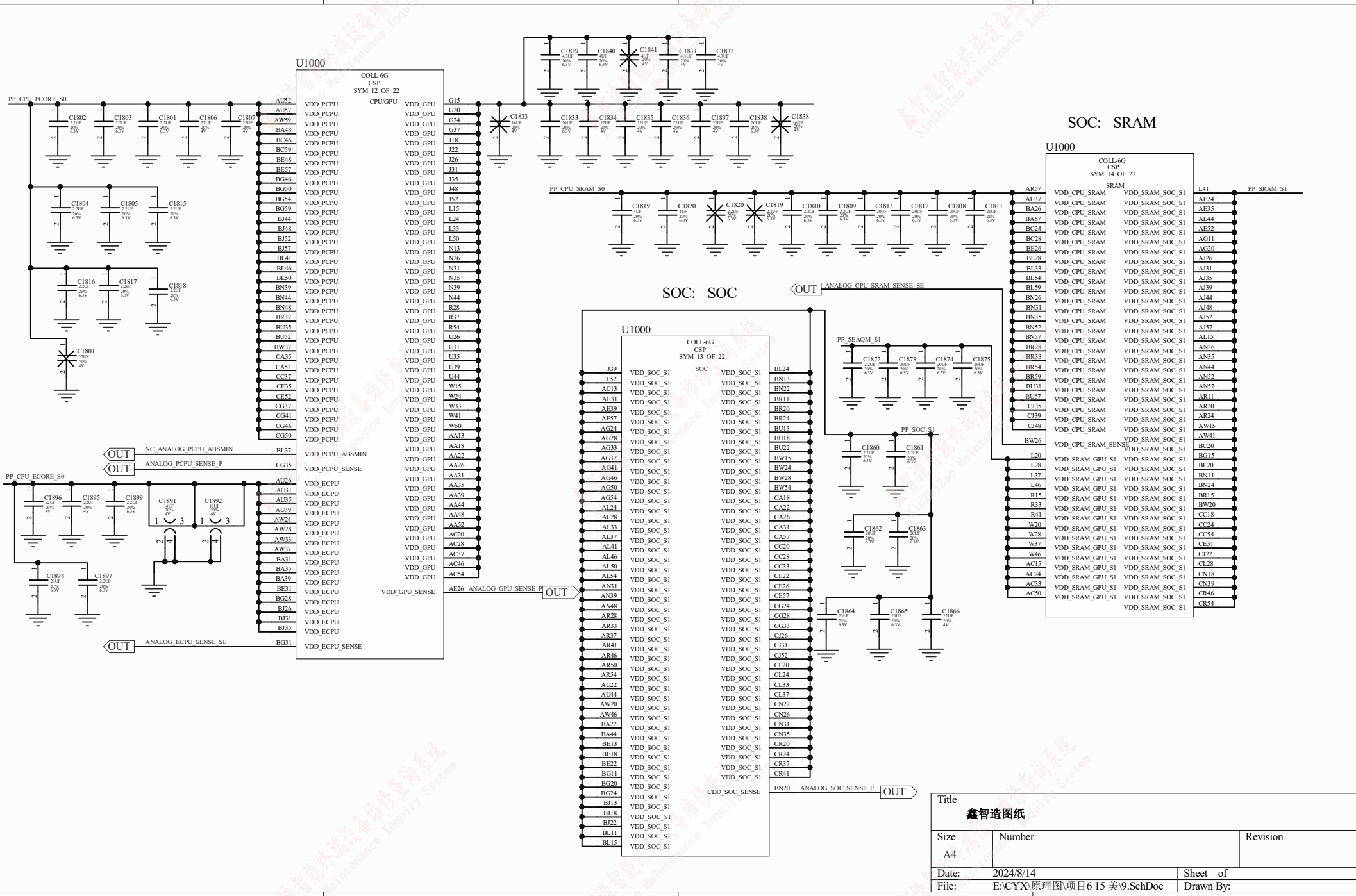

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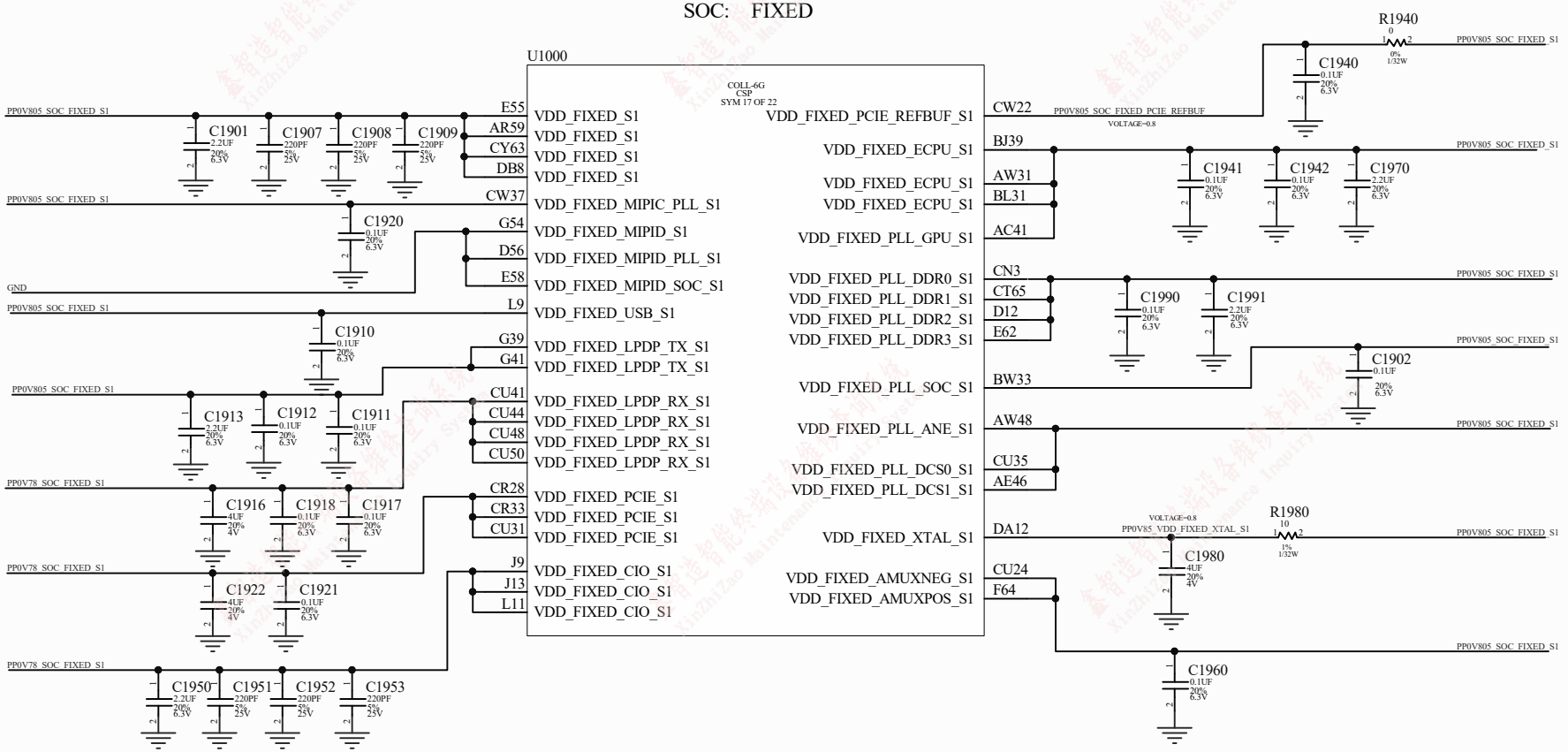

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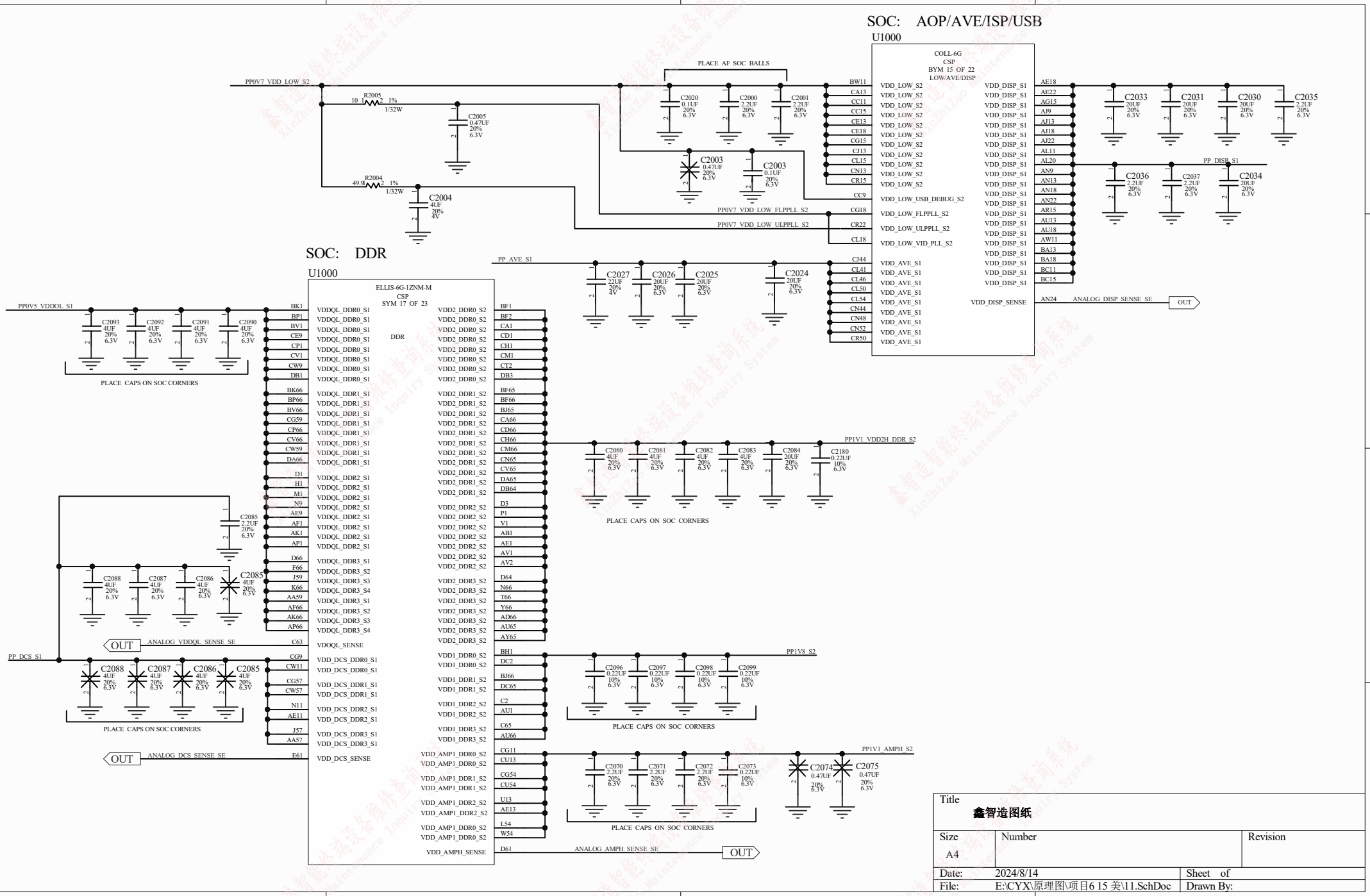
SOC: AOP/AVE/ISP/USB
U1000
COLL-6G
CSP
BYM 15 OF 22
LOW/AVE/DISP
PLACE AF SOC BALLS
PP0V7_VDD_LOW_S2
R2005
10_1
1%
1/32W
R2004
49.9
1%
1/32W
C2005
0.47UF
20%
6.3V
C2004
4UF
20%
4V
C2020
0.1UF
20%
6.3V
C2000
2.2UF
20%
6.3V
C2001
2.2UF
20%
6.3V
C2003
0.47UF
20%
6.3V
C2003
0.1UF
20%
6.3V
BW11
CA13
CC11
CC15
CE13
CE18
CG15
CJ13
CL15
CN13
CR15
CC9
CG18
CR22
CL18
VDD_LOW_S2
VDD_LOW_USB_DEBUG_S2
VDD_LOW_FLPPLL_S2
VDD_LOW_ULPPLL_S2
VDD_LOW_VID_PLL_S2
PP0V7_VDD_LOW_FLPPLL_S2
PP0V7_VDD_LOW_ULPPLL_S2
PP_AVE_S1
C2027
22UF
20%
4V
C2026
20UF
20%
6.3V
C2025
20UF
20%
6.3V
C2024
20UF
20%
6.3V
CJ44
CL41
CL46
CL50
CL54
CN44
CN48
CN52
CR50
VDD_AVE_S1
AE18
AE22
AG15
AJ9
AJ13
AJ18
AJ22
AL11
AL20
AN9
AN13
AN18
AN22
AR15
AU13
AU18
AW11
BA13
BA18
BC11
BC15
VDD_DISP_S1
VDD_DISP_SENSE
AN24
ANALOG_DISP_SENSE_SE
OUT
C2033
20UF
20%
6.3V
C2031
20UF
20%
6.3V
C2030
20UF
20%
6.3V
C2035
2.2UF
20%
6.3V
PP_DISP_S1
C2036
2.2UF
20%
6.3V
C2037
2.2UF
20%
6.3V
C2034
20UF
20%
6.3V
SOC: DDR
U1000
ELLIS-6G-1ZNM-M
CSP
SYM 17 OF 23
DDR
PP0V5_VDDQL_S1
C2093
4UF
20%
6.3V
C2092
4UF
20%
6.3V
C2091
4UF
20%
6.3V
C2090
4UF
20%
6.3V
PLACE CAPS ON SOC CORNERS
BK1
BP1
BV1
CE9
CP1
CV1
CW9
DB1
BK66
BP66
BV66
CG59
CP66
CV66
CW59
DA66
D1
H1
M1
N9
AE9
AF1
AK1
AP1
D66
F66
J59
K66
AA59
AF66
AK66
AP66
VDDQL_DDR0_S1
VDDQL_DDR1_S1
VDDQL_DDR2_S1
VDDQL_DDR3_S1
VDDQL_DDR3_S2
VDDQL_DDR3_S3
VDDQL_DDR3_S4
C2085
2.2UF
20%
6.3V
C2088
4UF
20%
6.3V
C2087
4UF
20%
6.3V
C2086
4UF
20%
6.3V
C2085
4UF
20%
6.3V
OUT
ANALOG_VDDQL_SENSE_SE
C63
VDDQL_SENSE
PP_DCS_S1
C2088
4UF
20%
6.3V
C2087
4UF
20%
6.3V
C2086
4UF
20%
6.3V
C2085
4UF
20%
6.3V
PLACE CAPS ON SOC CORNERS
CG9
CW11
CG57
CW57
N11
AE11
J57
AA57
VDD_DCS_DDR0_S1
VDD_DCS_DDR1_S1
VDD_DCS_DDR2_S1
VDD_DCS_DDR3_S1
OUT
ANALOG_DCS_SENSE_SE
E61
VDD_DCS_SENSE
BF1
BF2
CA1
CD1
CH1
CM1
CT2
DB3
BF65
BF66
BJ65
CA66
CD66
CH66
CM66
CN65
CV65
DA65
DB64
D3
P1
V1
AB1
AE1
AV1
AV2
D64
N66
T66
Y66
AD66
AU65
AY65
VDD2_DDR0_S2
VDD2_DDR1_S2
VDD2_DDR2_S2
VDD2_DDR3_S2
PP1V1_VDD2H_DDR_S2
C2080
4UF
20%
6.3V
C2081
4UF
20%
6.3V
C2082
4UF
20%
6.3V
C2083
4UF
20%
6.3V
C2084
20UF
20%
6.3V
C2180
0.22UF
10%
6.3V
PLACE CAPS ON SOC CORNERS
BH1
DC2
BJ66
DC65
C2
AU1
C65
AU66
VDD1_DDR0_S2
VDD1_DDR1_S2
VDD1_DDR2_S2
VDD1_DDR3_S2
PP1V8_S2
C2096
0.22UF
10%
6.3V
C2097
0.22UF
10%
6.3V
C2098
0.22UF
10%
6.3V
C2099
0.22UF
10%
6.3V
PLACE CAPS ON SOC CORNERS
CG11
CU13
CG54
CU54
U13
AE13
L54
W54
VDD_AMP1_DDR0_S2
VDD_AMP1_DDR1_S2
VDD_AMP1_DDR2_S2
VDD_AMP1_DDR0_S2
VDD_AMPH_SENSE
D61
ANALOG_AMPH_SENSE_SE
OUT
PP1V1_AMPH_S2
C2070
2.2UF
20%
6.3V
C2071
2.2UF
20%
6.3V
C2072
2.2UF
20%
6.3V
C2073
0.22UF
10%
6.3V
C2074
0.47UF
20%
6.3V
C2075
0.47UF
20%
6.3V
PLACE CAPS ON SOC CORNERS
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鑫智造图纸
Size
A4
Number
Revision
Date:
2024/8/14
Sheet of
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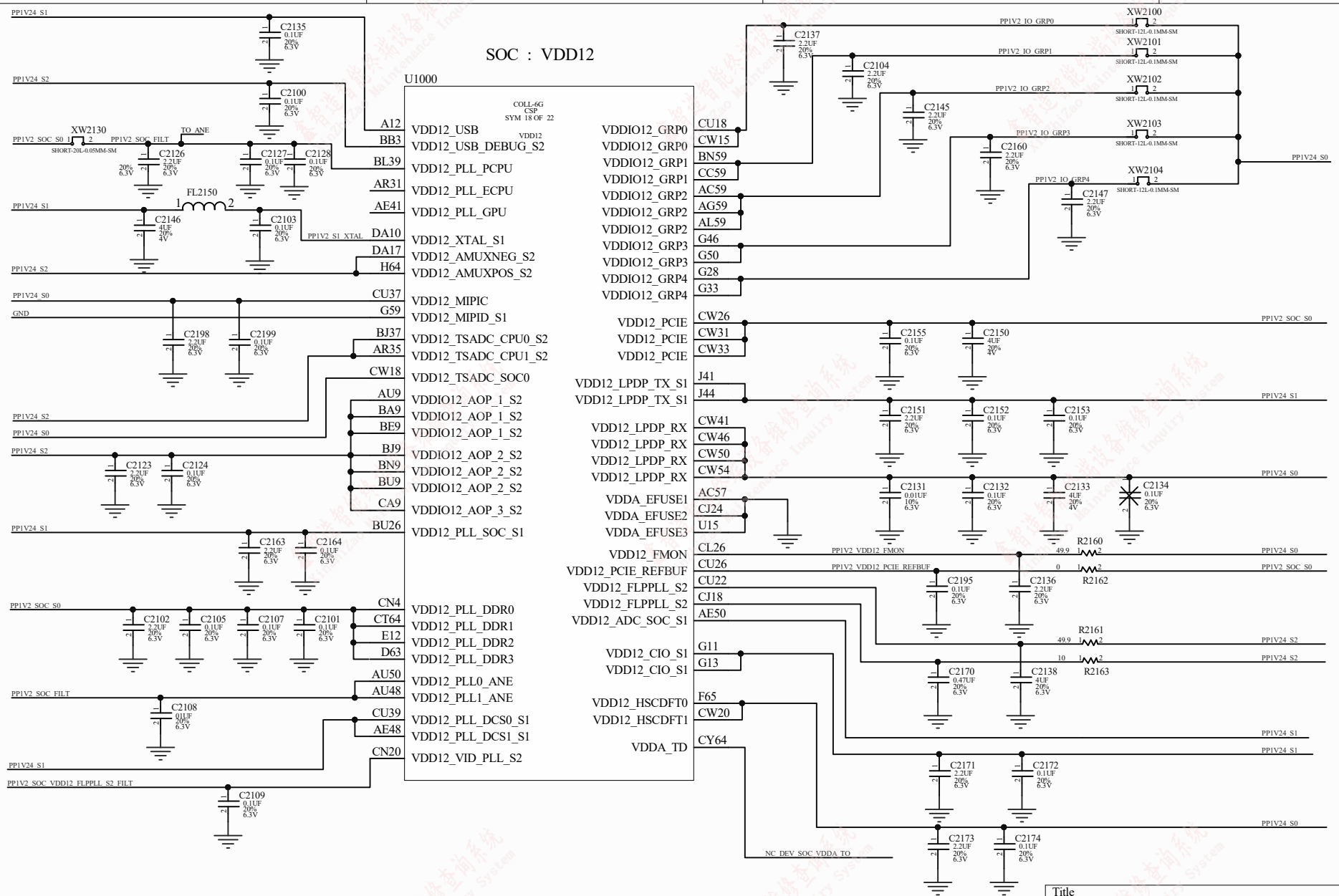

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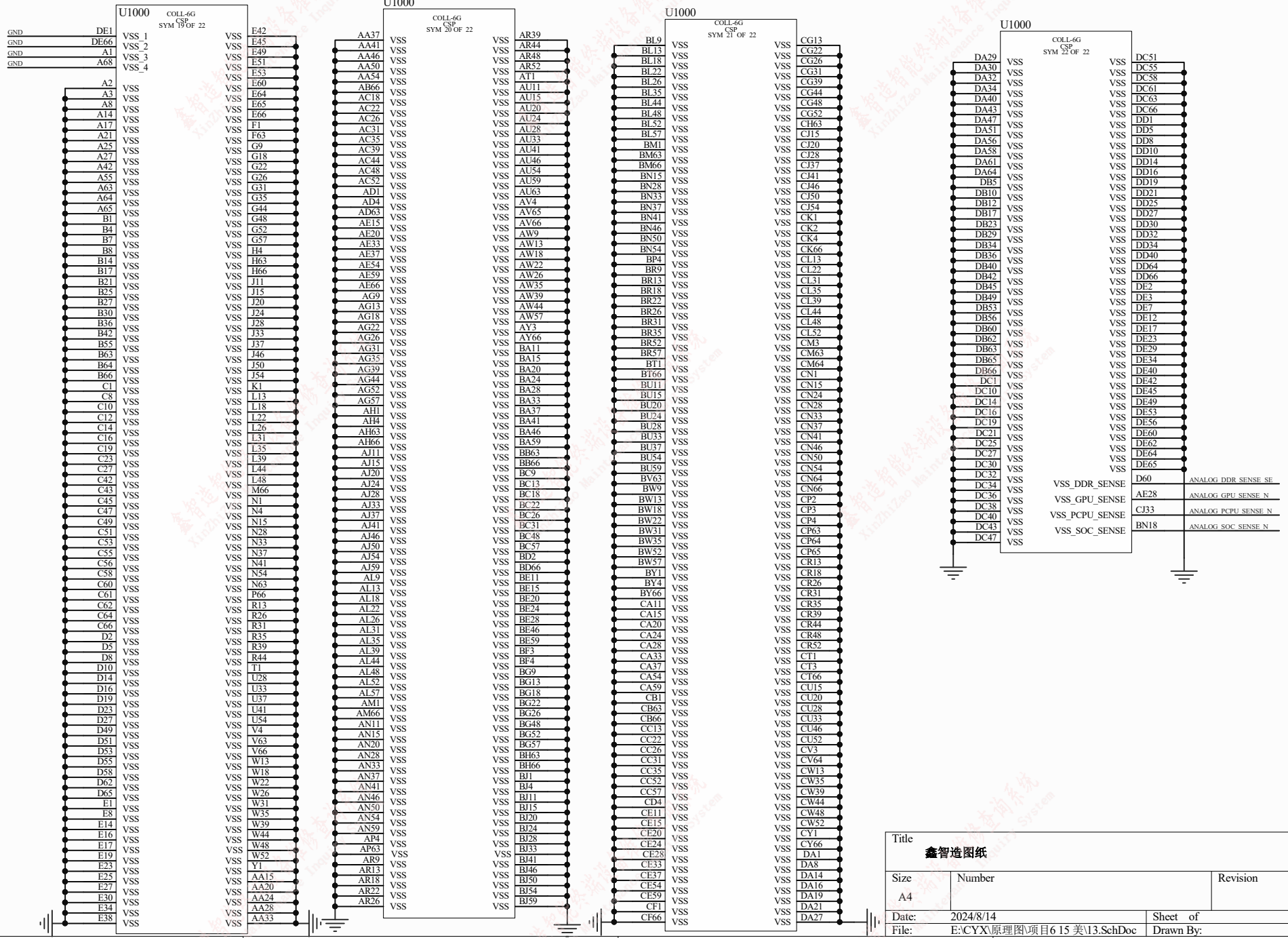

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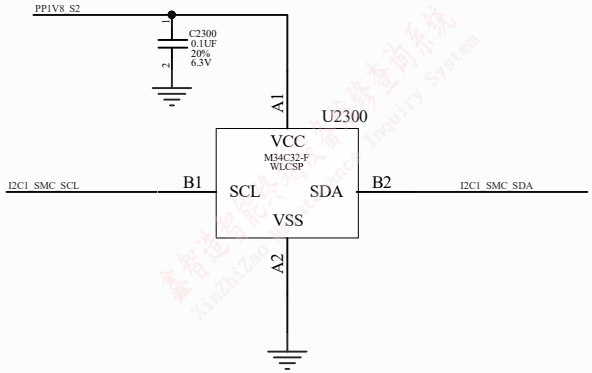

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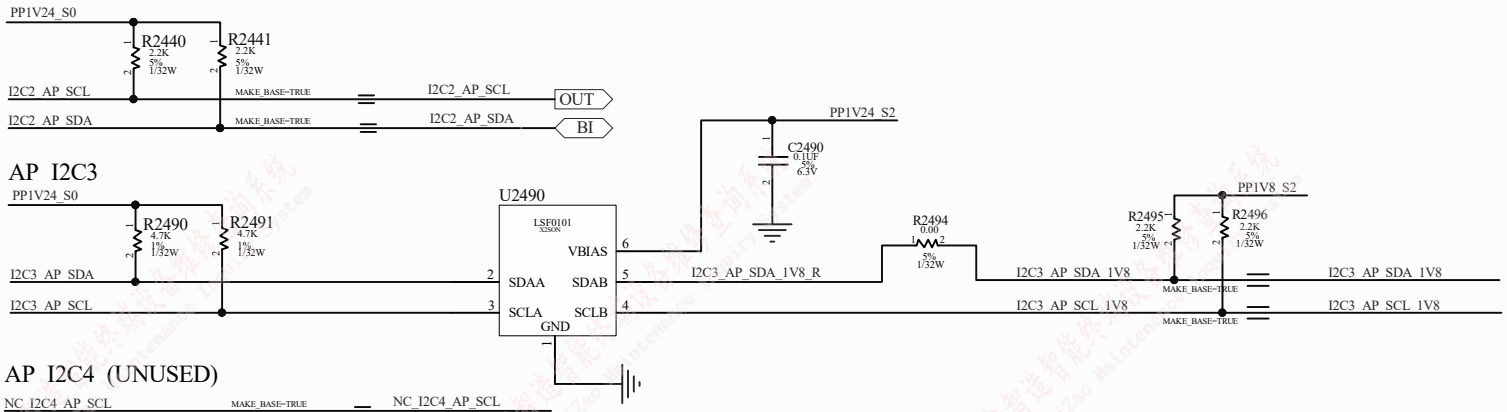

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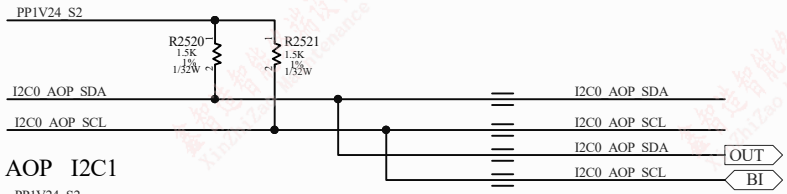
AOP I2C0



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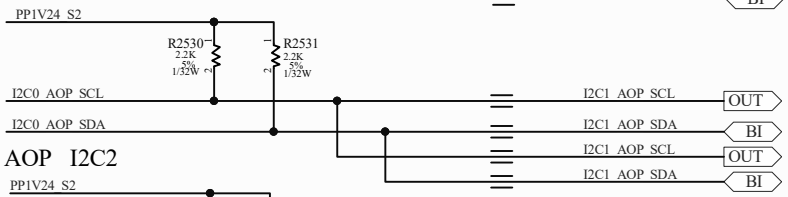

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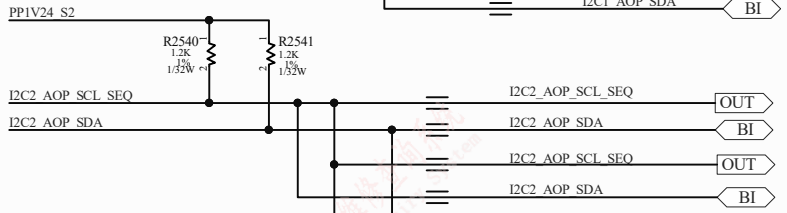
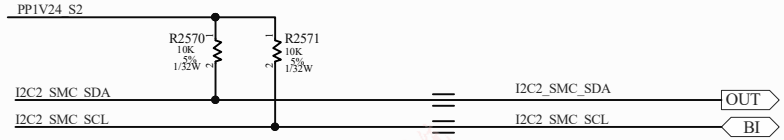


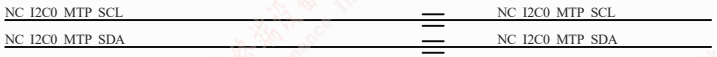
AOP I2C3

SMC I2C1

SMC I2C2



MTP I2C0 (Unused)



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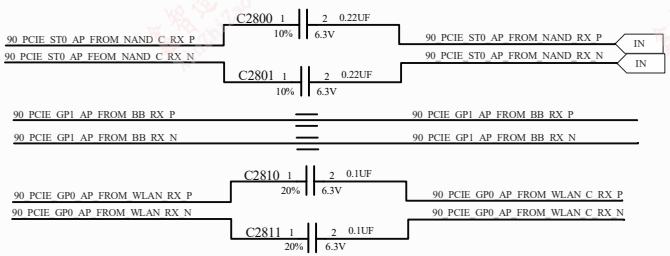
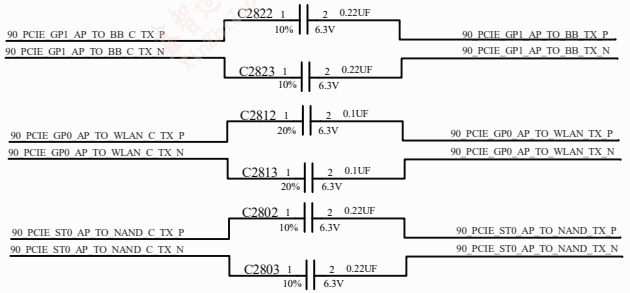
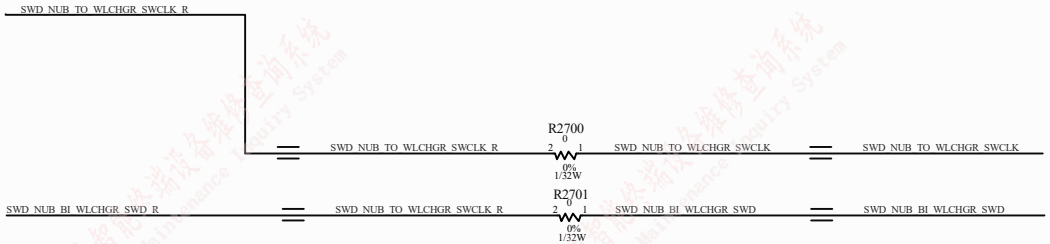
File: E:\CYX\原理图\项目6 15 美\15.SchDoc		Drawn By:







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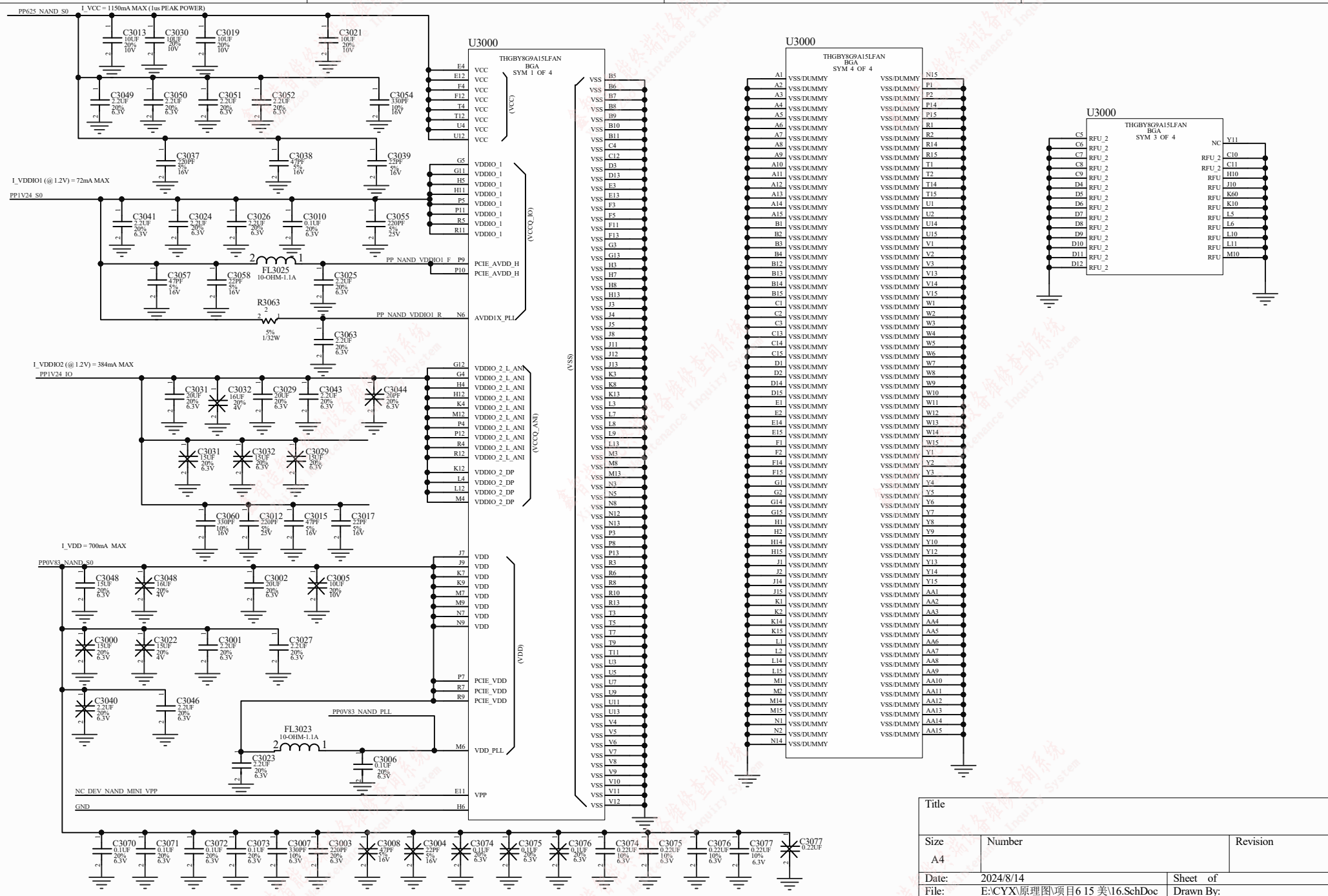

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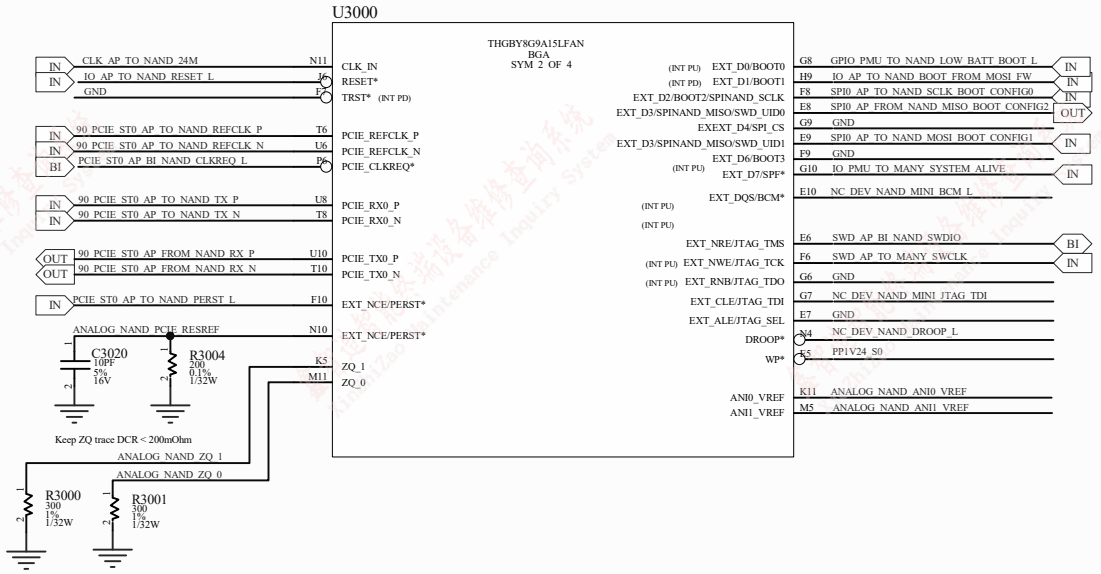

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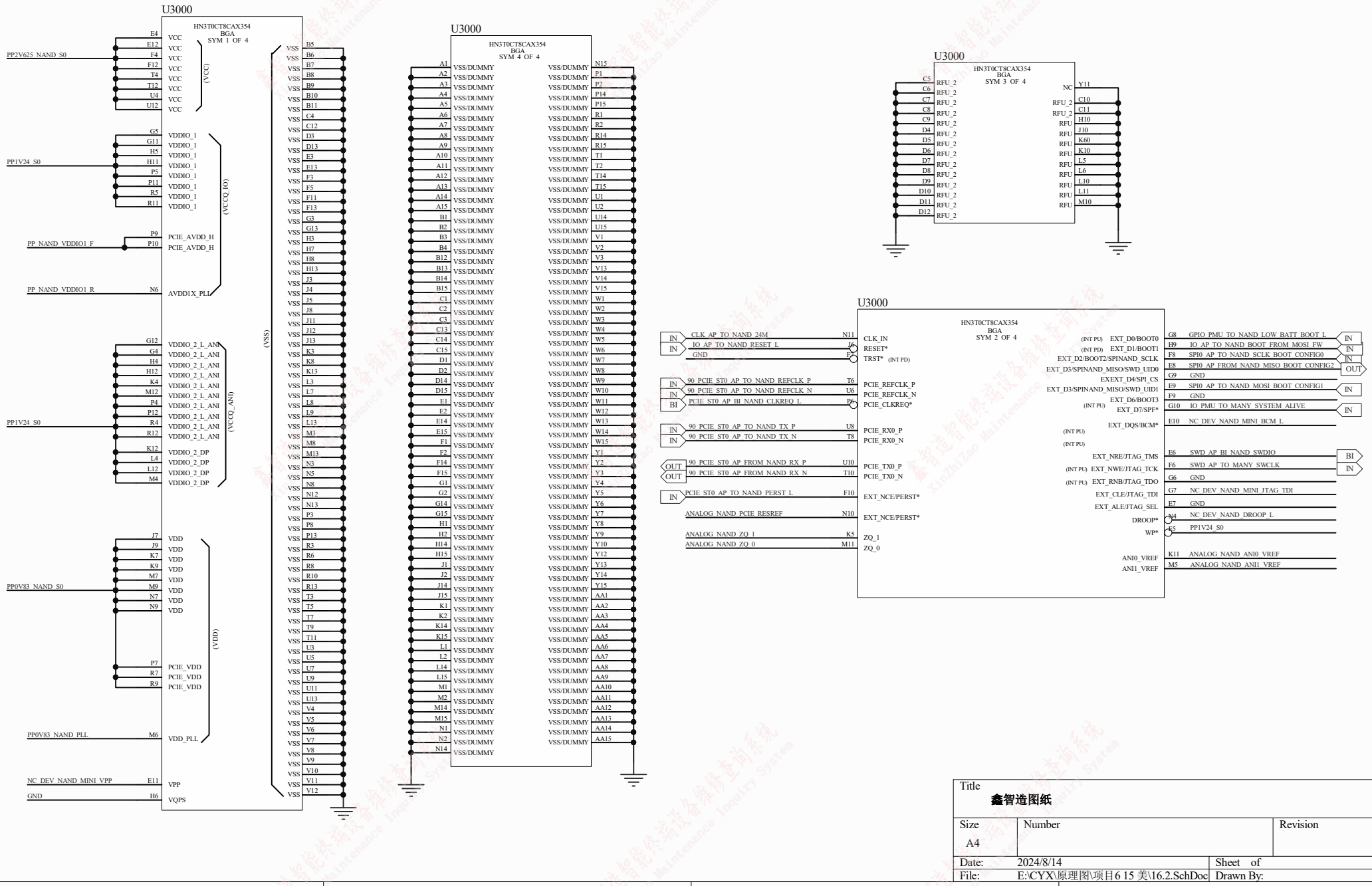
U3000
HN3T0CT8CAX354
BGA
SYM 1 OF 4
PP2V625_NAND_S0
PP1V24_S0
PP_NAND_VDDIO1_F
PP_NAND_VDDIO1_R
PP1V24_S0
PP0V83_NAND_S0
PP0V83_NAND_PLL
NC_DEV_NAND_MINI_VPP
GND
VCC
VDDIO_1
PCIE_AVDD_H
AVDD1X_PLL
VDDIO_2_L_ANI
VDDIO_2_DP
VDD
PCIE_VDD
VDD_PLL
VPP
VQPS
VSS
(VCC)
(VCCQ_IO)
(VCCQ_ANI)
(VDD)
U3000
HN3T0CT8CAX354
BGA
SYM 4 OF 4
VSS/DUMMY
U3000
HN3T0CT8CAX354
BGA
SYM 3 OF 4
RFU_2
RFU
NC
U3000
HN3T0CT8CAX354
BGA
SYM 2 OF 4
CLK_AP_TO_NAND_24M
IO_AP_TO_NAND_RESET_L
GND
CLK_IN
RESET*
TRST*
90_PCIE_ST0_AP_TO_NAND_REFCLK_P
90_PCIE_ST0_AP_TO_NAND_REFCLK_N
PCIE_ST0_AP_BI_NAND_CLKREQ_L
PCIE_REFCLK_P
PCIE_REFCLK_N
PCIE_CLKREQ*
90_PCIE_ST0_AP_TO_NAND_TX_P
90_PCIE_ST0_AP_TO_NAND_TX_N
PCIE_RX0_P
PCIE_RX0_N
90_PCIE_ST0_AP_FROM_NAND_RX_P
90_PCIE_ST0_AP_FROM_NAND_RX_N
PCIE_TX0_P
PCIE_TX0_N
PCIE_ST0_AP_TO_NAND_PERST_L
EXT_NCE/PERST*
ANALOG_NAND_PCIE_RESREF
EXT_NCE/PERST*
ANALOG_NAND_ZQ_1
ANALOG_NAND_ZQ_0
ZQ_1
ZQ_0
EXT_D0/BOOT0
EXT_D1/BOOT1
EXT_D2/BOOT2/SPINAND_SCLK
EXT_D3/SPINAND_MISO/SWD_UID0
EXT_D4/SPI_CS
EXT_D3/SPINAND_MISO/SWD_UID1
EXT_D6/BOOT3
EXT_D7/SPF*
EXT_DQS/BCM*
EXT_NRE/JTAG_TMS
EXT_NWE/JTAG_TCK
EXT_RNB/JTAG_TDO
EXT_CLE/JTAG_TDI
EXT_ALE/JTAG_SEL
DROOP*
WP*
ANI0_VREF
ANI1_VREF
GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L
IO_AP_TO_NAND_BOOT_FROM_MOSI_FW
SPI0_AP_TO_NAND_SCLK_BOOT_CONFIG0
SPI0_AP_FROM_NAND_MISO_BOOT_CONFIG2
SPI0_AP_TO_NAND_MOSI_BOOT_CONFIG1
IO_PMU_TO_MANY_SYSTEM_ALIVE
NC_DEV_NAND_MINI_BCM_L
SWD_AP_BI_NAND_SWDIO
SWD_AP_TO_MANY_SWCLK
NC_DEV_NAND_MINI_JTAG_TDI
NC_DEV_NAND_DROOP_L
PP1V24_S0
ANALOG_NAND_ANI0_VREF
ANALOG_NAND_ANI1_VREF
IN
OUT
BI
Title
鑫智造图纸
Size
A4
Number
Revision
Date:
2024/8/14
Sheet of
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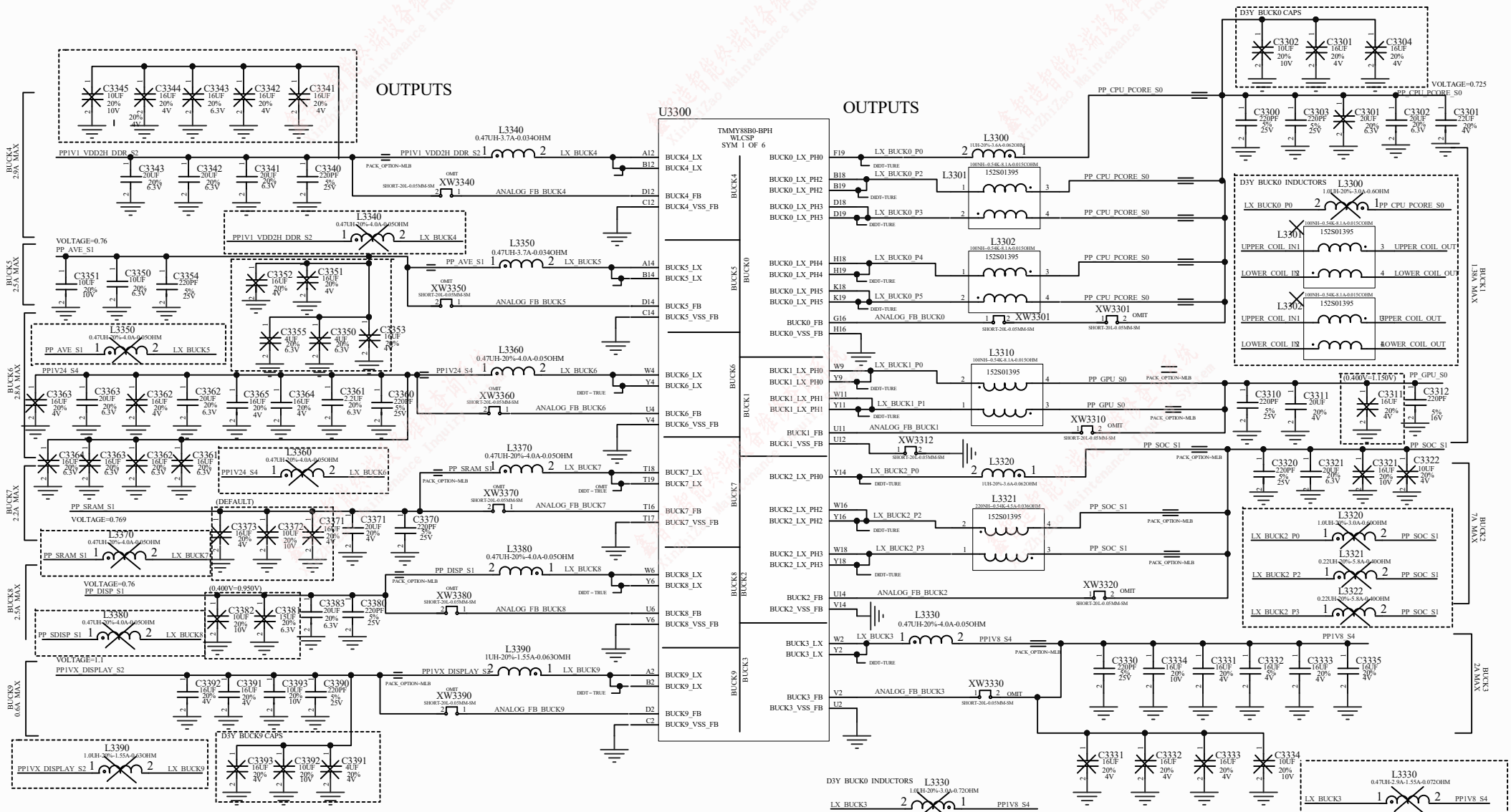

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Date:	2024/8/14	Sheet of	
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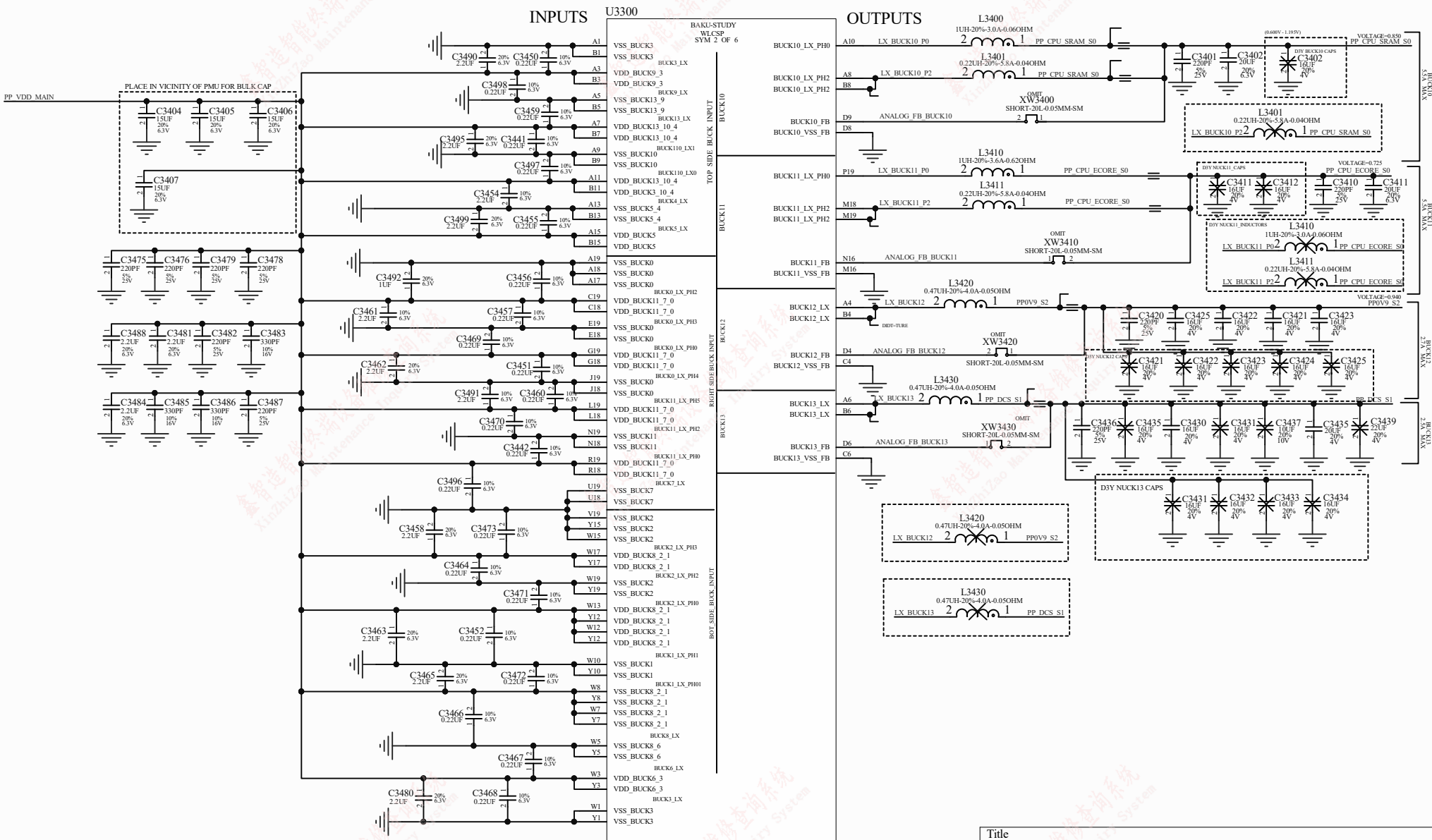
INPUTS
U3300
BAKU-STUDY
WLCSP
SYM 2 OF 6
OUTPUTS
PLACE IN VICINITY OF PMU FOR BULK CAP
PP_VDD_MAIN
C3404 15UF
C3405 15UF
C3406 15UF
C3407 15UF
C3475 220PF
C3476 220PF
C3479 220PF
C3478 220PF
C3488 2.2UF
C3481 2.2UF
C3482 220PF
C3483 330PF
C3484 2.2UF
C3485 330PF
C3486 330PF
C3487 220PF
C3490 2.2UF
C3450 0.22UF
C3498 0.22UF
C3459 0.22UF
C3495 2.2UF
C3441 0.22UF
C3497 0.22UF
C3454 2.2UF
C3499 2.2UF
C3455 0.22UF
C3492 1UF
C3456 0.22UF
C3461 2.2UF
C3457 0.22UF
C3469 0.22UF
C3462 2.2UF
C3451 0.22UF
C3491 2.2UF
C3460 0.22UF
C3470 0.22UF
C3442 0.22UF
C3496 0.22UF
C3458 2.2UF
C3473 0.22UF
C3464 0.22UF
C3471 0.22UF
C3463 2.2UF
C3452 0.22UF
C3465 2.2UF
C3472 0.22UF
C3466 0.22UF
C3467 0.22UF
C3480 2.2UF
C3468 0.22UF
VSS_BUCK3
VDD_BUCK9_3
VSS_BUCK13_9
VDD_BUCK13_10_4
VSS_BUCK10
VDD_BUCK3_10_4
VSS_BUCK5_4
VDD_BUCK5
VSS_BUCK0
VDD_BUCK11_7_0
VDD_BUCK8_2_1
VSS_BUCK2
VSS_BUCK1
VSS_BUCK8_2_1
VSS_BUCK8_6
VDD_BUCK6_3
BUCK3_LX
BUCK9_LX
BUCK13_LX
BUCK110_LX1
BUCK110_LX0
BUCK4_LX
BUCK5_LX
BUCK0_LX_PH2
BUCK0_LX_PH3
BUCK0_LX_PH0
BUCK0_LX_PH4
BUCK11_LX_PH5
BUCK11_LX_PH2
BUCK11_LX_PH0
BUCK7_LX
BUCK2_LX_PH3
BUCK2_LX_PH2
BUCK2_LX_PH0
BUCK1_LX_PH1
BUCK1_LX_PH01
BUCK8_LX
BUCK6_LX
TOP SIDE BUCK INPUT
BUCK10
BUCK11
BUCK12
RIGHT SIDE BUCK INPUT
BUCK13
BOT SIDE BUCK INPUT
BUCK10_LX_PH0
BUCK10_LX_PH2
BUCK10_LX_PH2
BUCK10_FB
BUCK10_VSS_FB
BUCK11_LX_PH0
BUCK11_LX_PH2
BUCK11_LX_PH2
BUCK11_FB
BUCK11_VSS_FB
BUCK12_LX
BUCK12_LX
BUCK12_FB
BUCK12_VSS_FB
BUCK13_LX
BUCK13_LX
BUCK13_FB
BUCK13_VSS_FB
L3400 1UH-20%-3.0A-0.06OHM
L3401 0.22UH-20%-5.8A-0.04OHM
L3410 1UH-20%-3.6A-0.62OHM
L3411 0.22UH-20%-5.8A-0.04OHM
L3420 0.47UH-20%-4.0A-0.05OHM
L3430 0.47UH-20%-4.0A-0.05OHM
LX_BUCK10_P0
LX_BUCK10_P2
LX_BUCK11_P0
LX_BUCK11_P2
LX_BUCK12
LX_BUCK13
PP_CPU_SRAM_S0
PP_CPU_ECORE_S0
PP0V9_S2
PP_DCS_S1
ANALOG_FB_BUCK10
ANALOG_FB_BUCK11
ANALOG_FB_BUCK12
ANALOG_FB_BUCK13
OMIT
XW3400 SHORT-20L-0.05MM-SM
XW3410 SHORT-20L-0.05MM-SM
XW3420 SHORT-20L-0.05MM-SM
XW3430 SHORT-20L-0.05MM-SM
DIDT=TURE
VOLTAGE=0.850
VOLTAGE=0.725
VOLTAGE=0.940
D3Y BUCK10 CAPS
D3Y NUCK11_CAPS
D3Y NUCK11_INDUCTORS
D3Y NUCK12 CAPS
D3Y NUCK13 CAPS
BUCK10 5.5A MAX
BUCK11 5.5A MAX
BUCK12 2.5A MAX
BUCK13 2.5A MAX
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鑫智造图纸
Size
A4
Number
Revision
Date: 2024/8/14
Sheet of
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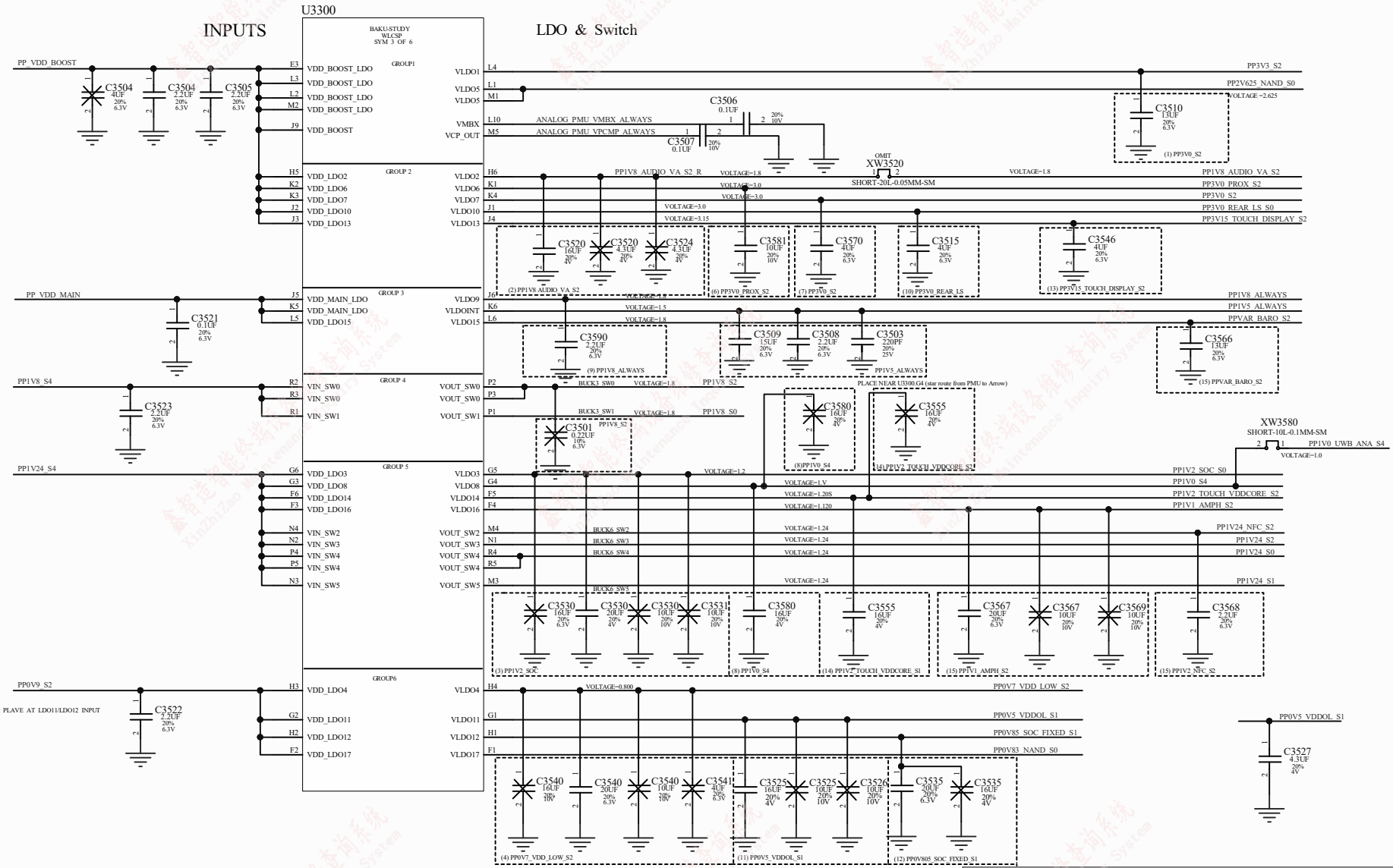
U3300
INPUTS
LDO & Switch
BAKU-STUDY
WLCSP
SYM 3 OF 6
PP_VDD_BOOST
PP_VDD_MAIN
PP1V8_S4
PP1V24_S4
PP0V9_S2
PLAVE AT LDO11/LDO12 INPUT
VDD_BOOST_LDO
VDD_BOOST
VDD_LDO2
VDD_LDO6
VDD_LDO7
VDD_LDO10
VDD_LDO13
VDD_MAIN_LDO
VDD_LDO15
VIN_SW0
VIN_SW1
VIN_SW2
VIN_SW3
VIN_SW4
VIN_SW5
VDD_LDO3
VDD_LDO8
VDD_LDO14
VDD_LDO16
VDD_LDO4
VDD_LDO11
VDD_LDO12
VDD_LDO17
VLDO1
VLDO5
VMBX
VCP_OUT
VLDO2
VLDO6
VLDO7
VLDO10
VLDO13
VLDO9
VLDOINT
VLDO15
VOUT_SW0
VOUT_SW1
VOUT_SW2
VOUT_SW3
VOUT_SW4
VOUT_SW5
VLDO3
VLDO8
VLDO14
VLDO16
VLDO4
VLDO11
VLDO12
VLDO17
ANALOG_PMU_VMBX_ALWAYS
ANALOG_PMU_VPCMP_ALWAYS
PP1V8_AUDIO_VA_S2_R
BUCK3_SW0
BUCK3_SW1
BUCK6_SW2
BUCK6_SW3
BUCK6_SW4
BUCK6_SW5
PP3V3_S2
PP2V625_NAND_S0
PP1V8_AUDIO_VA_S2
PP3V0_PROX_S2
PP3V0_S2
PP3V0_REAR_LS_S0
PP3V15_TOUCH_DISPLAY_S2
PP1V8_ALWAYS
PP1V5_ALWAYS
PPVAR_BARO_S2
PP1V8_S2
PP1V8_S0
PP1V0_S4
PP1V2_TOUCH_VDDCORE_S2
PP1V2_SOC_S0
PP1V0_S4
PP1V2_TOUCH_VDDCORE_S2
PP1V1_AMPH_S2
PP1V24_NFC_S2
PP1V24_S2
PP1V24_S0
PP1V24_S1
PP0V7_VDD_LOW_S2
PP0V5_VDDOL_S1
PP0V85_SOC_FIXED_S1
PP0V83_NAND_S0
PP0V5_VDDOL_S1
PP1V0_UWB_ANA_S4
XW3520
SHORT-20L-0.05MM-SM
XW3580
SHORT-10L-0.1MM-SM
PLACE NEAR U3300.G4 (star route from PMU to Arrow)
Title
鑫智造图纸
Size
A4
Number
Revision
Date: 2024/8/14
Sheet of
File: E:\CYX\原理图\项目6 15 美\19.SchDoc
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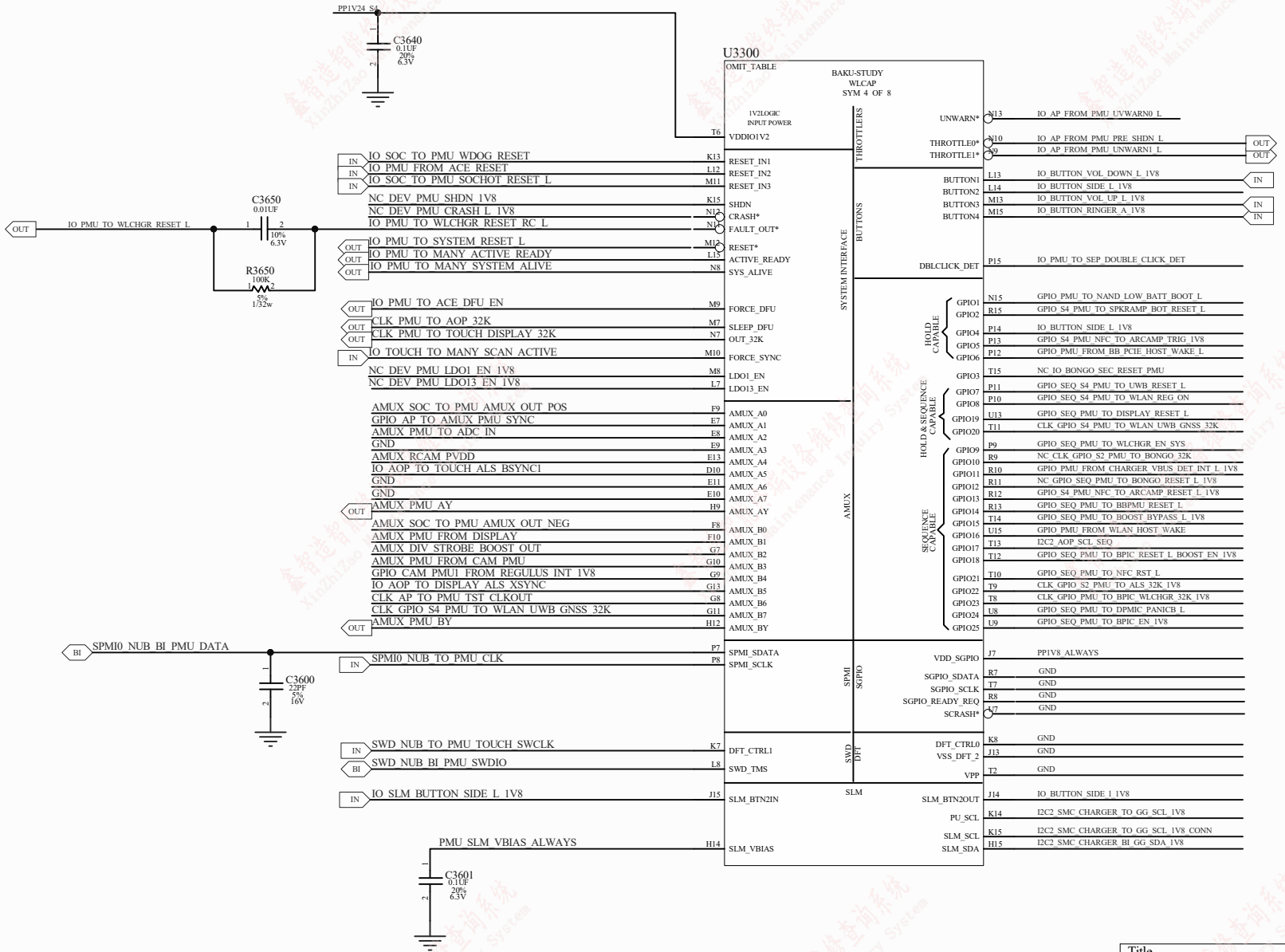

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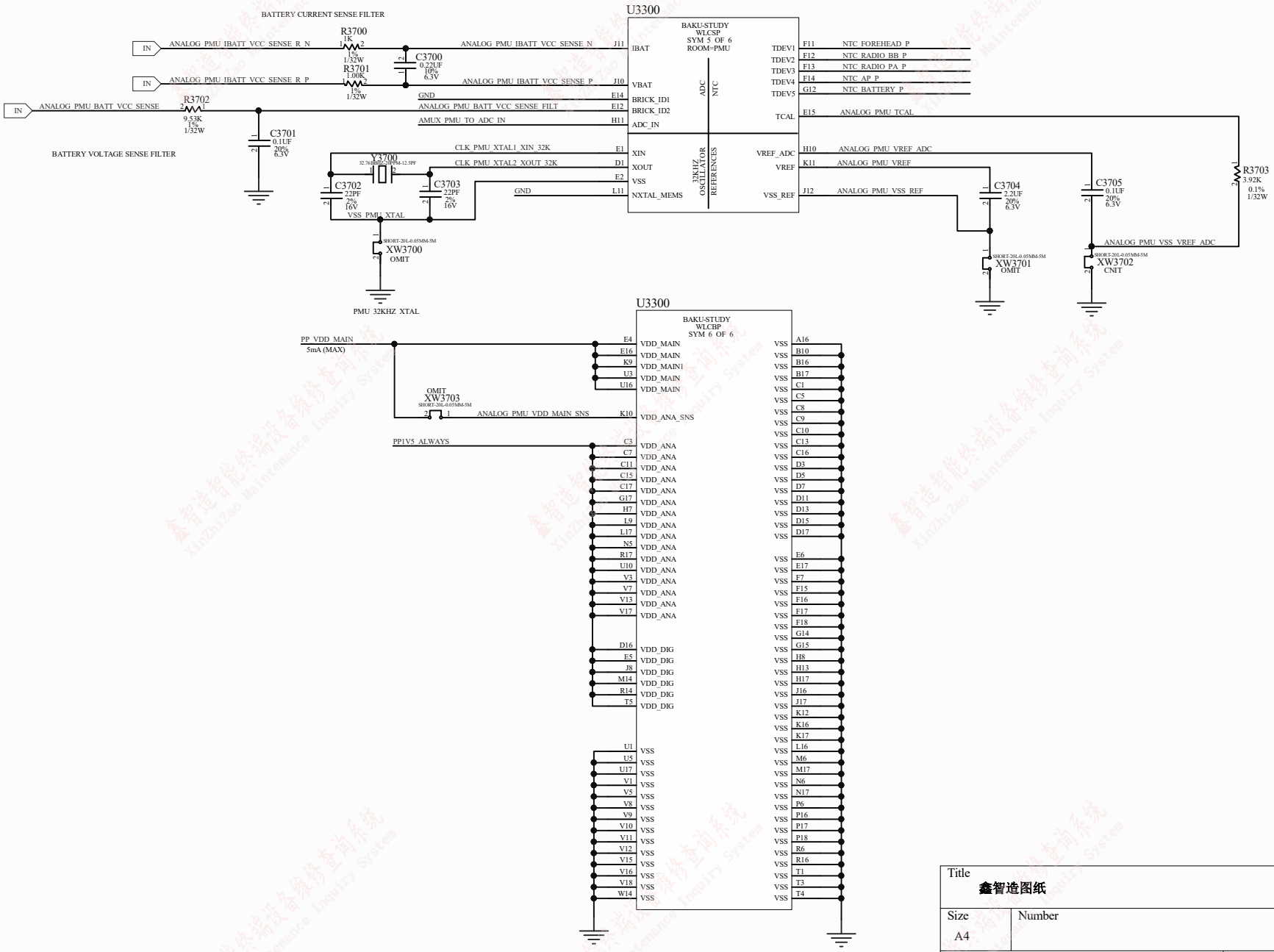

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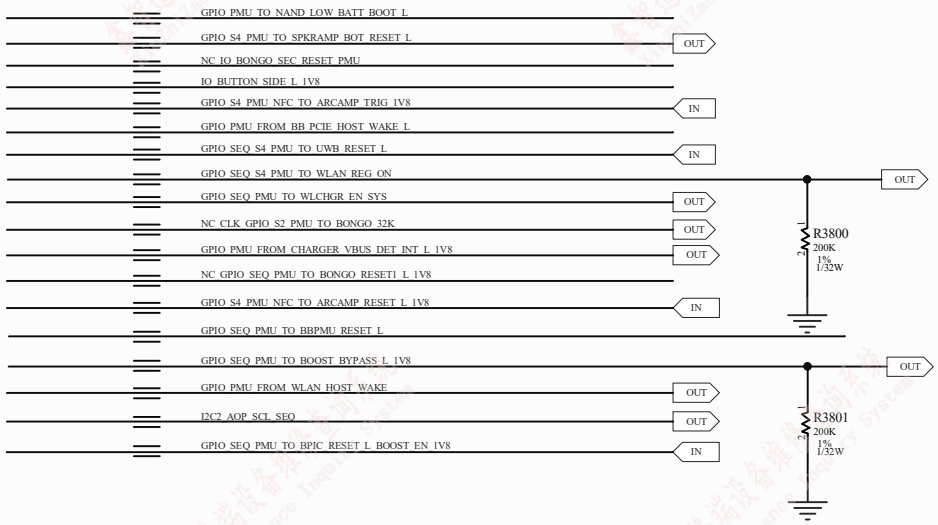

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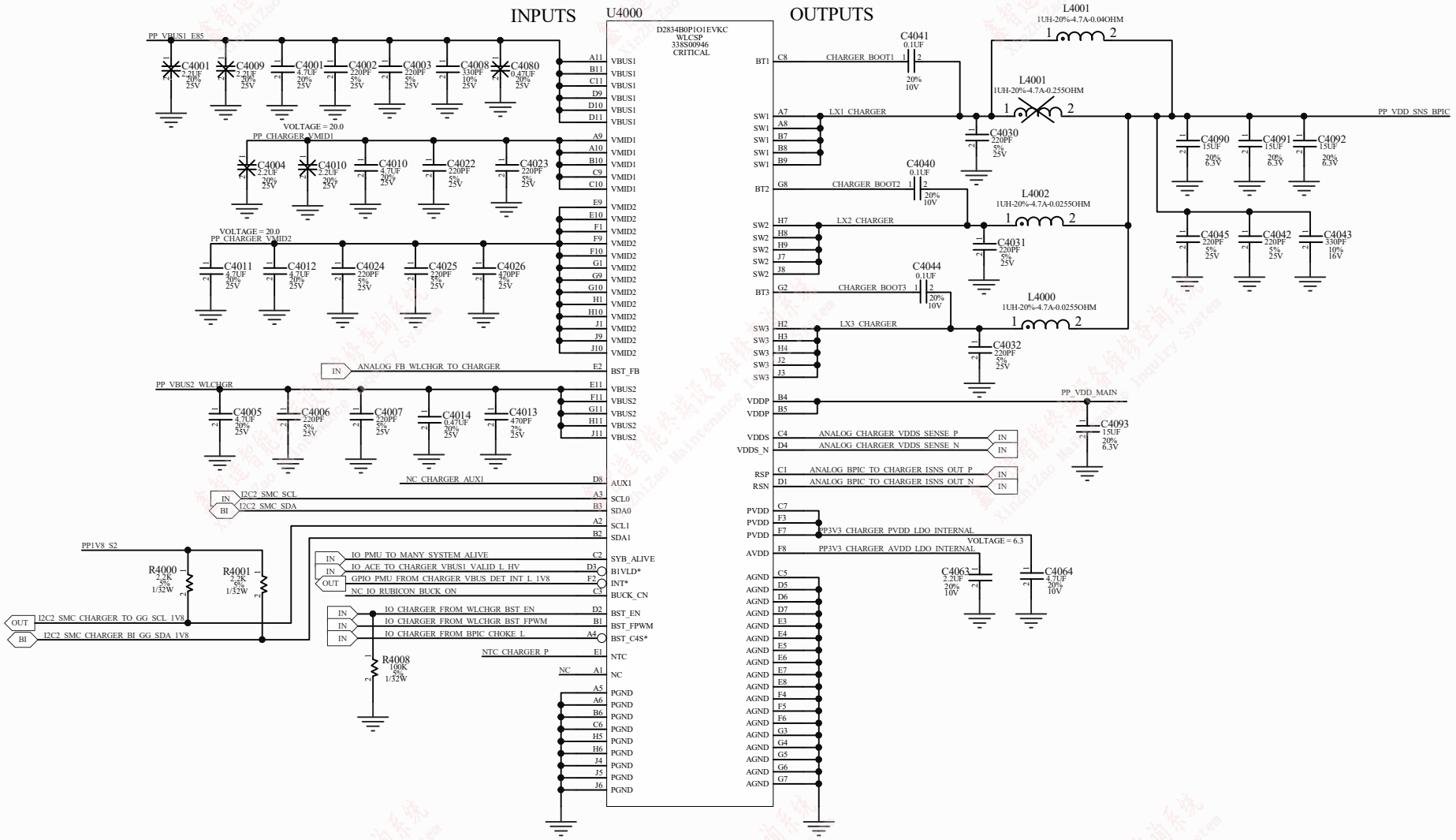

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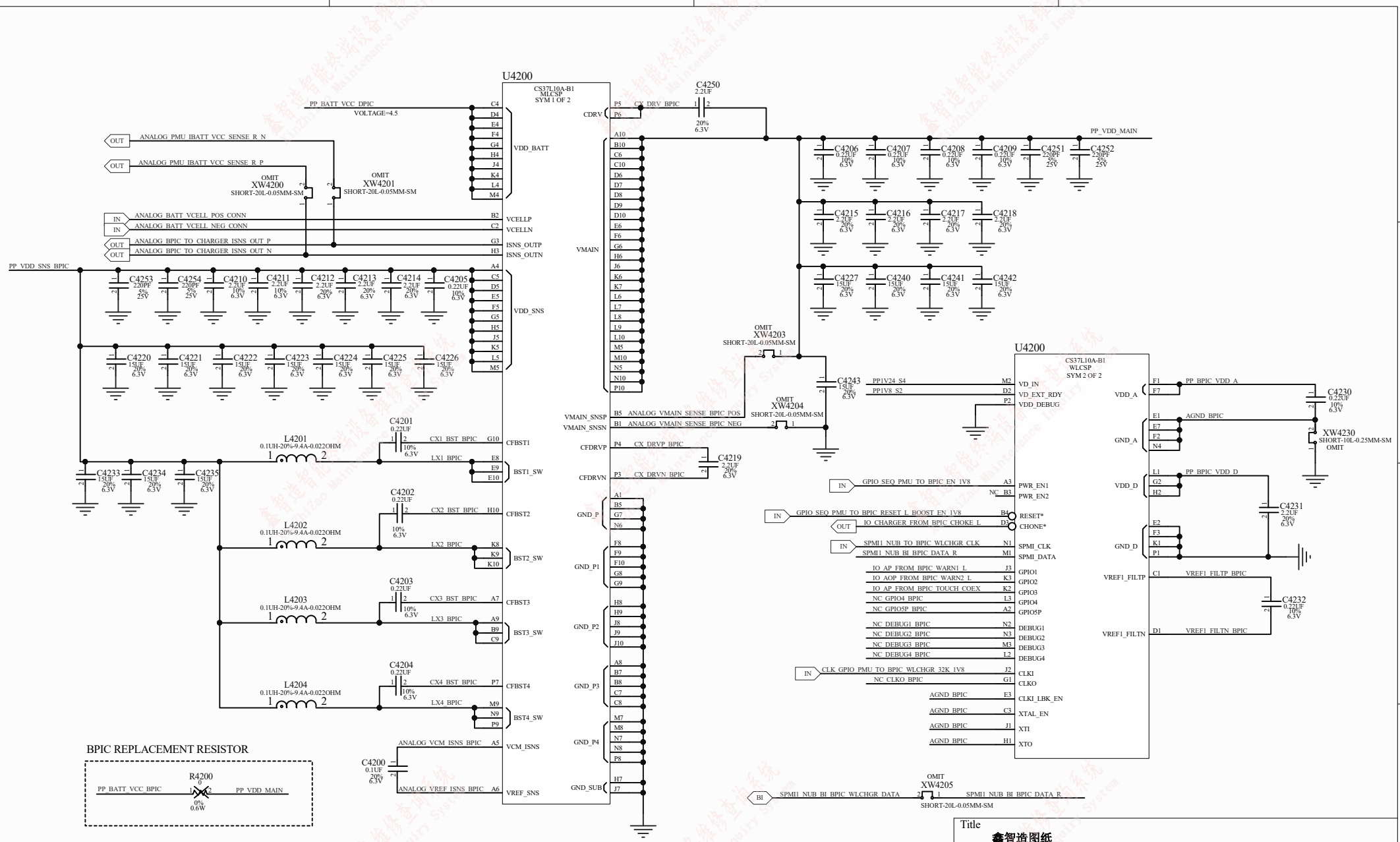

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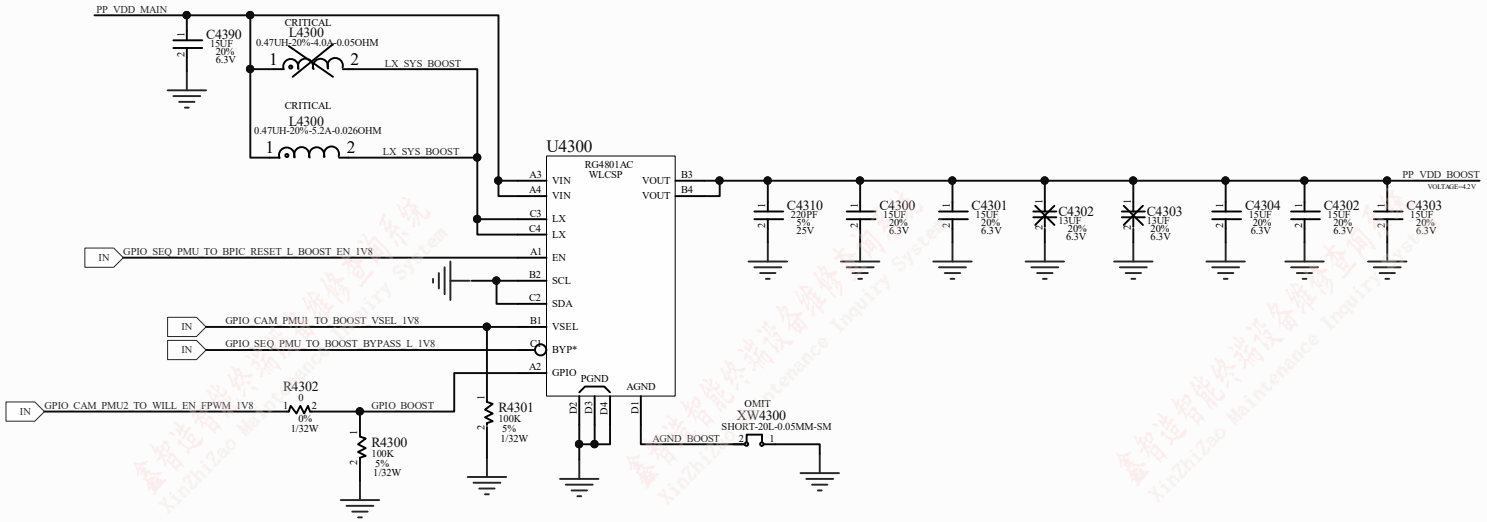

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Size A4	Number	Revision
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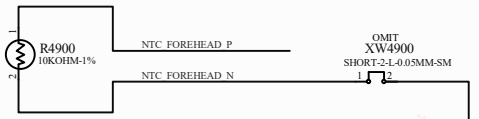
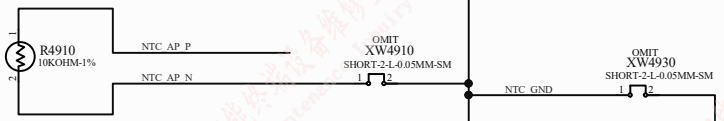
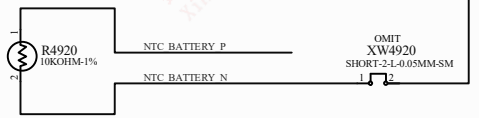
FOREHEAD NTC



AP NTC



BATTERY NTC



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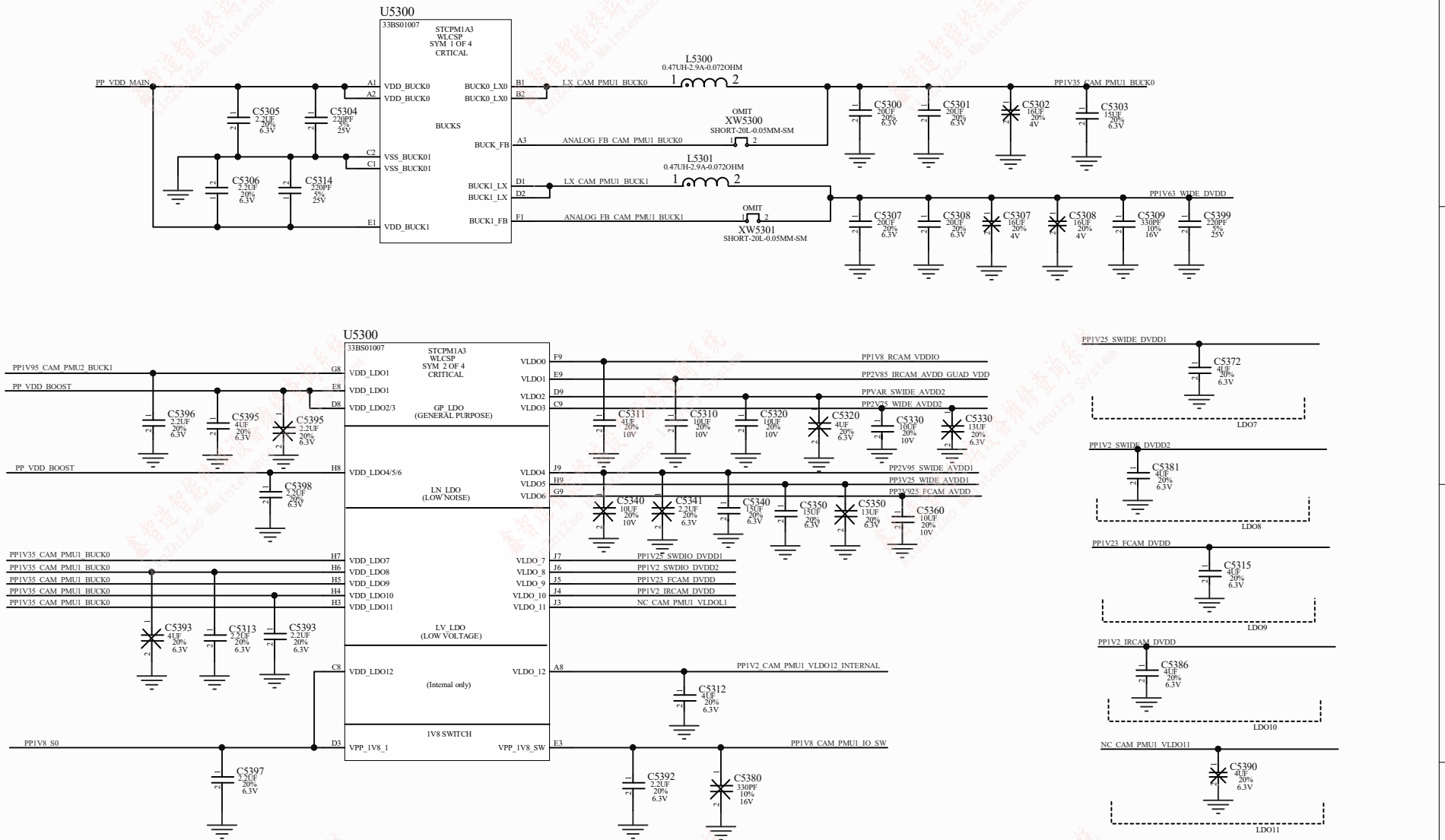

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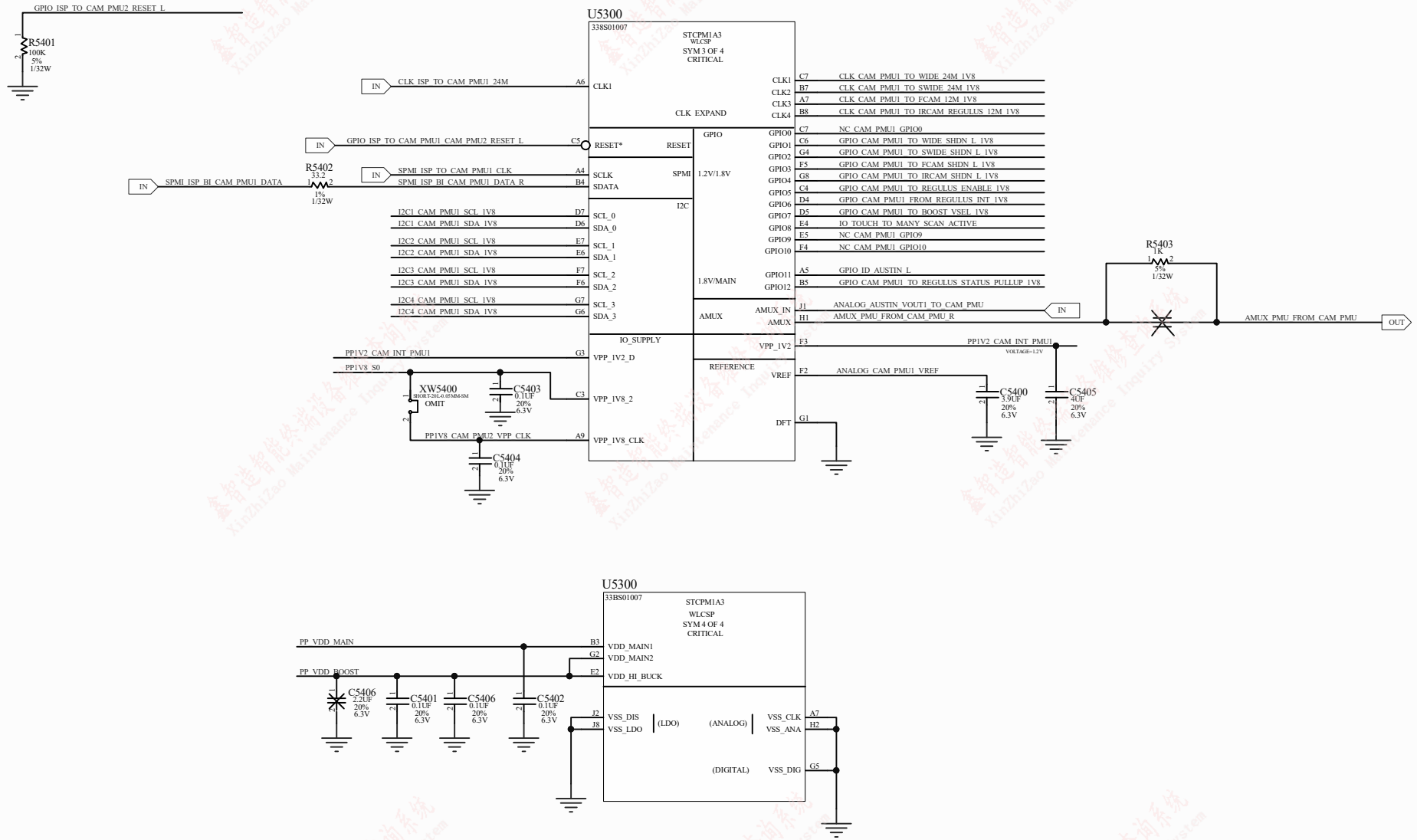

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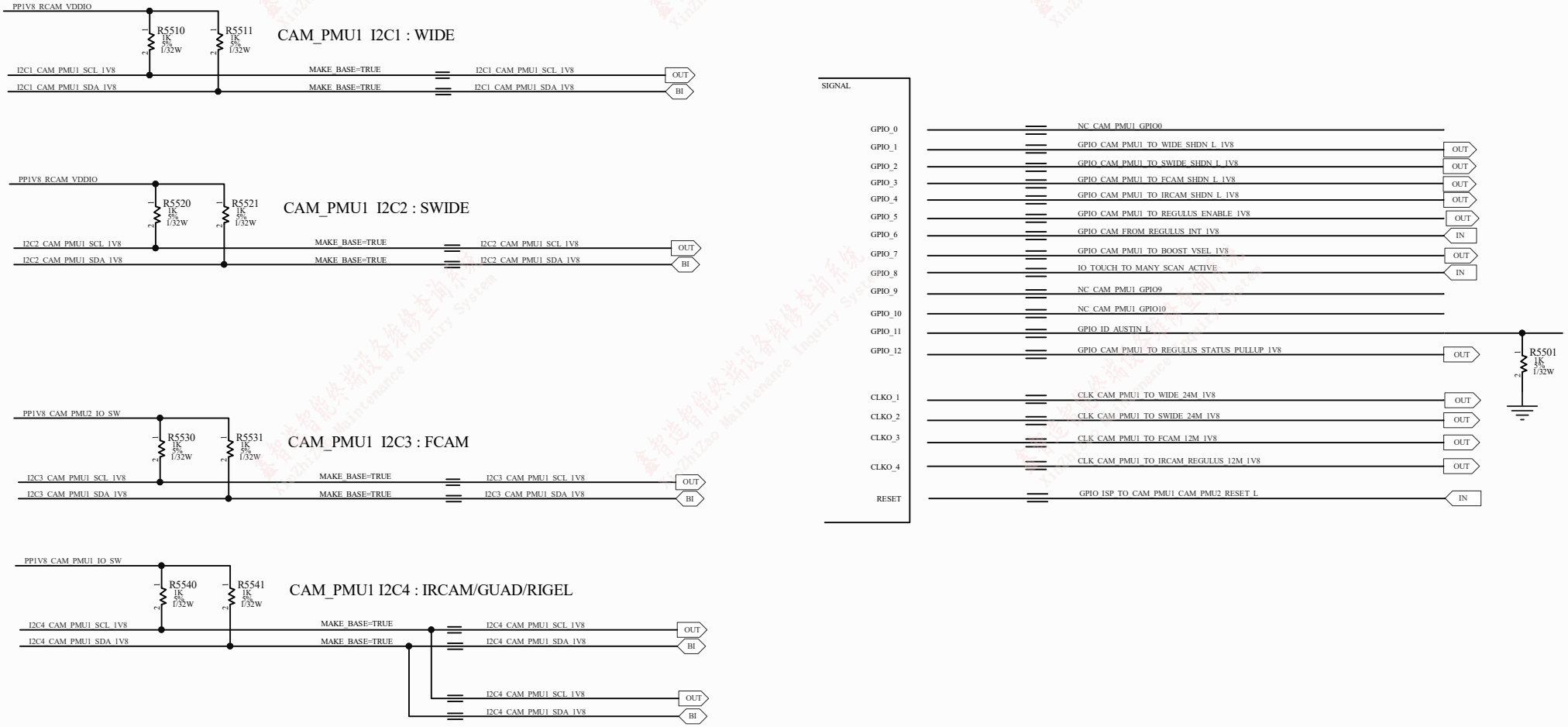

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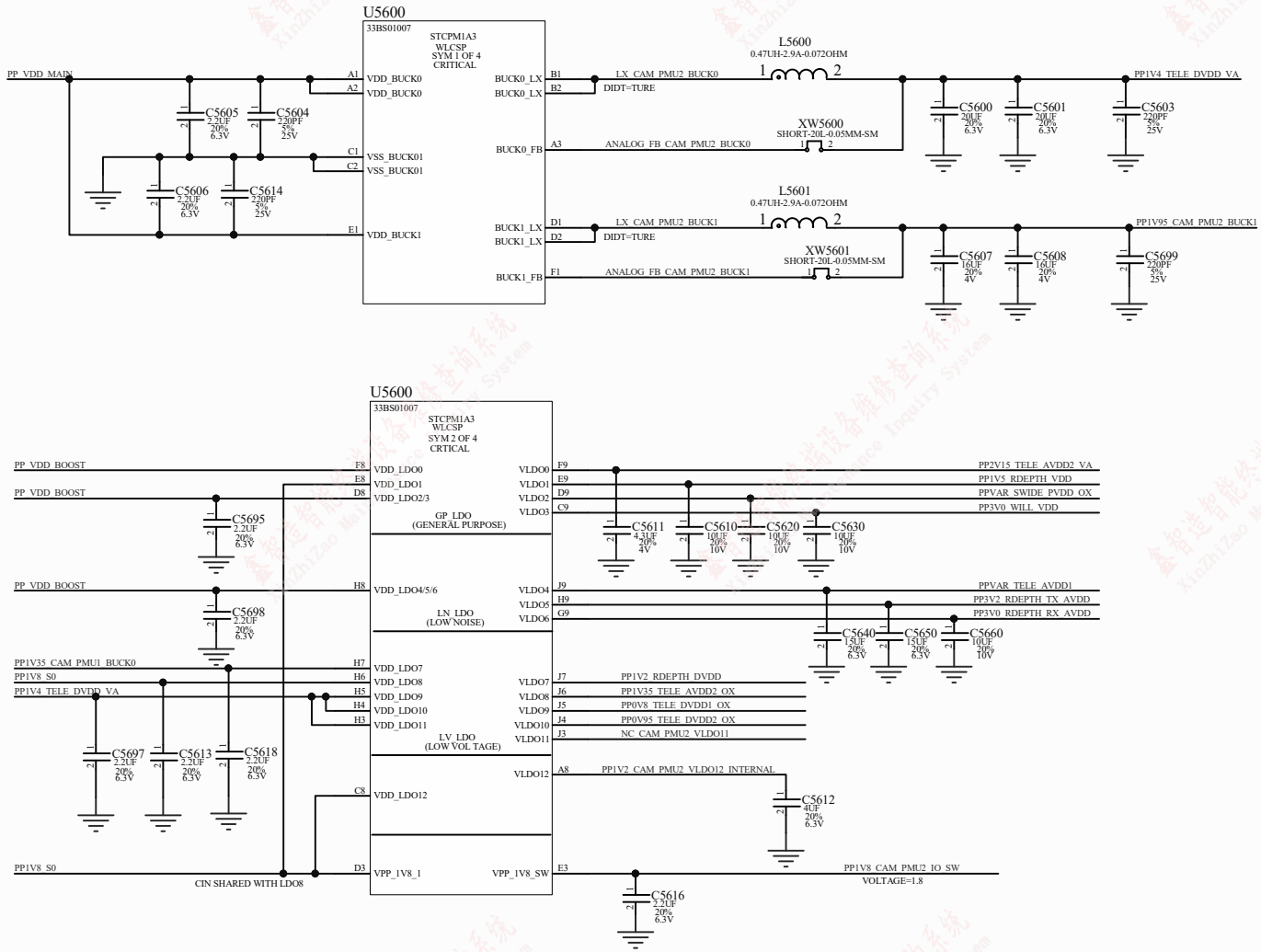

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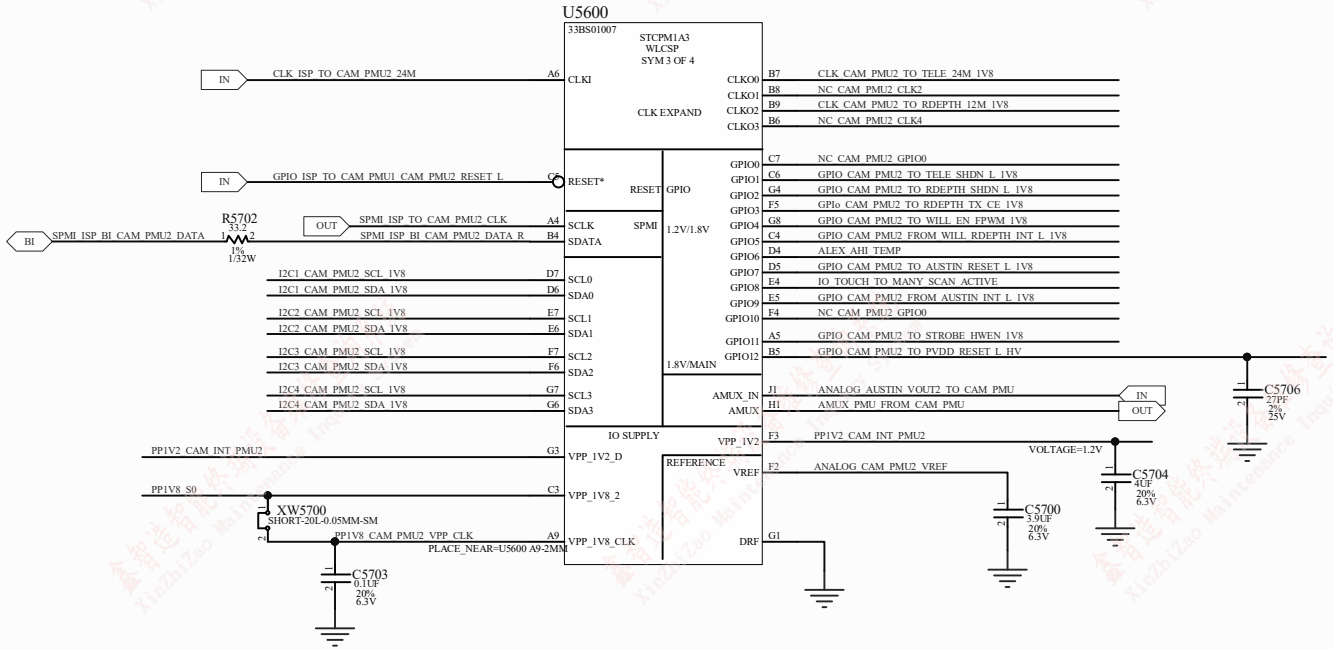

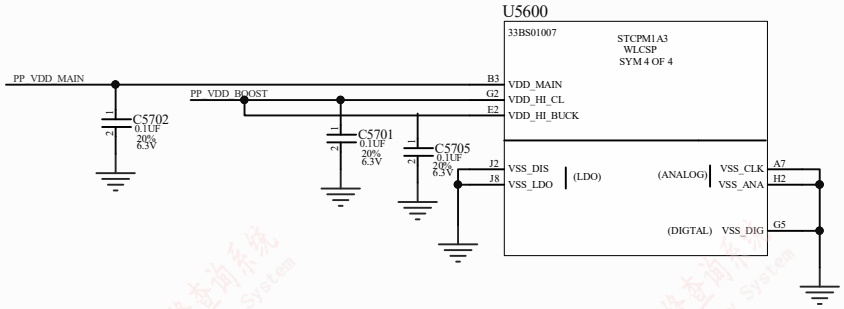

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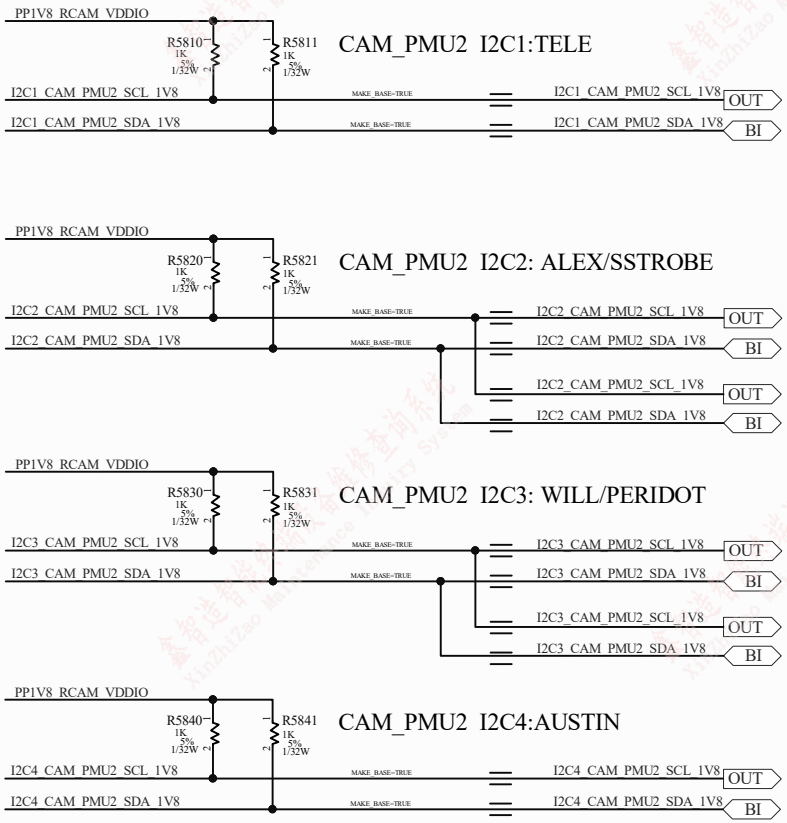

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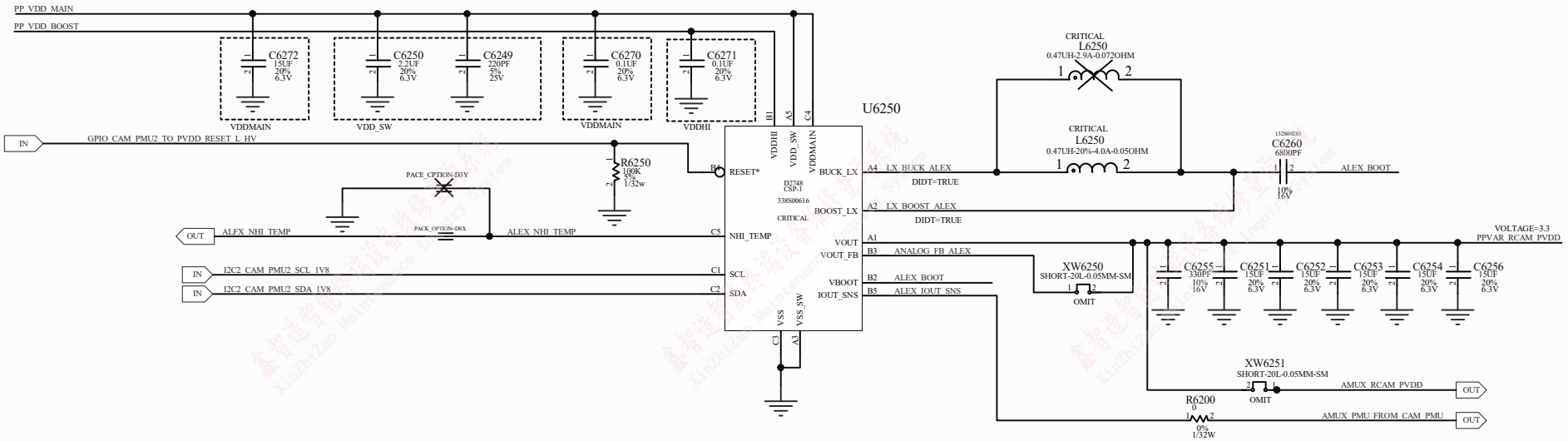

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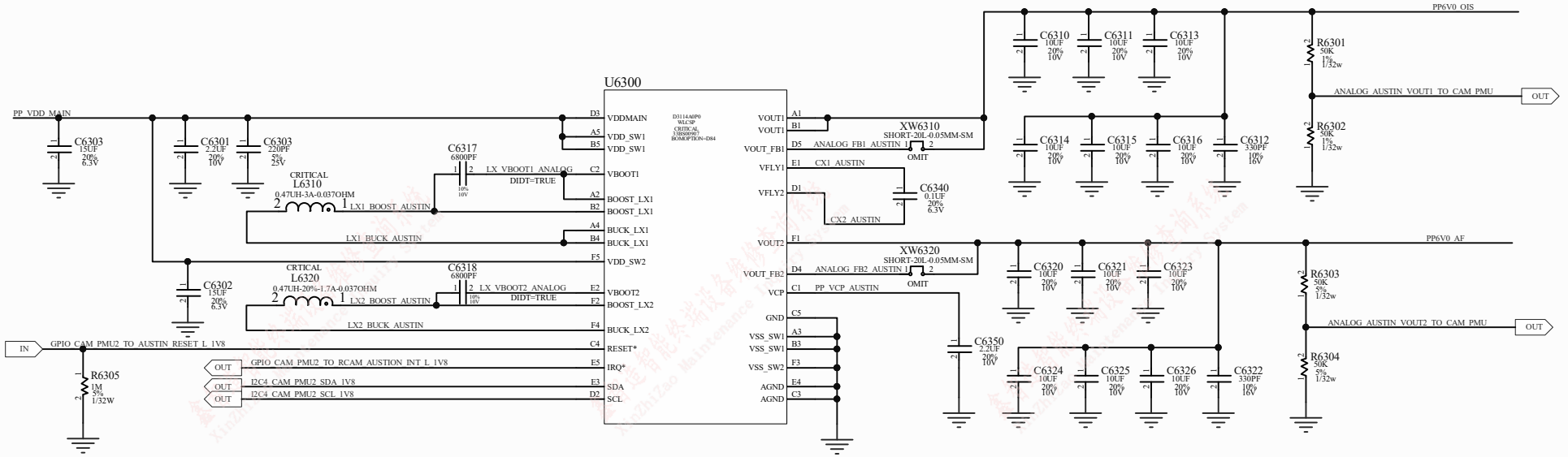

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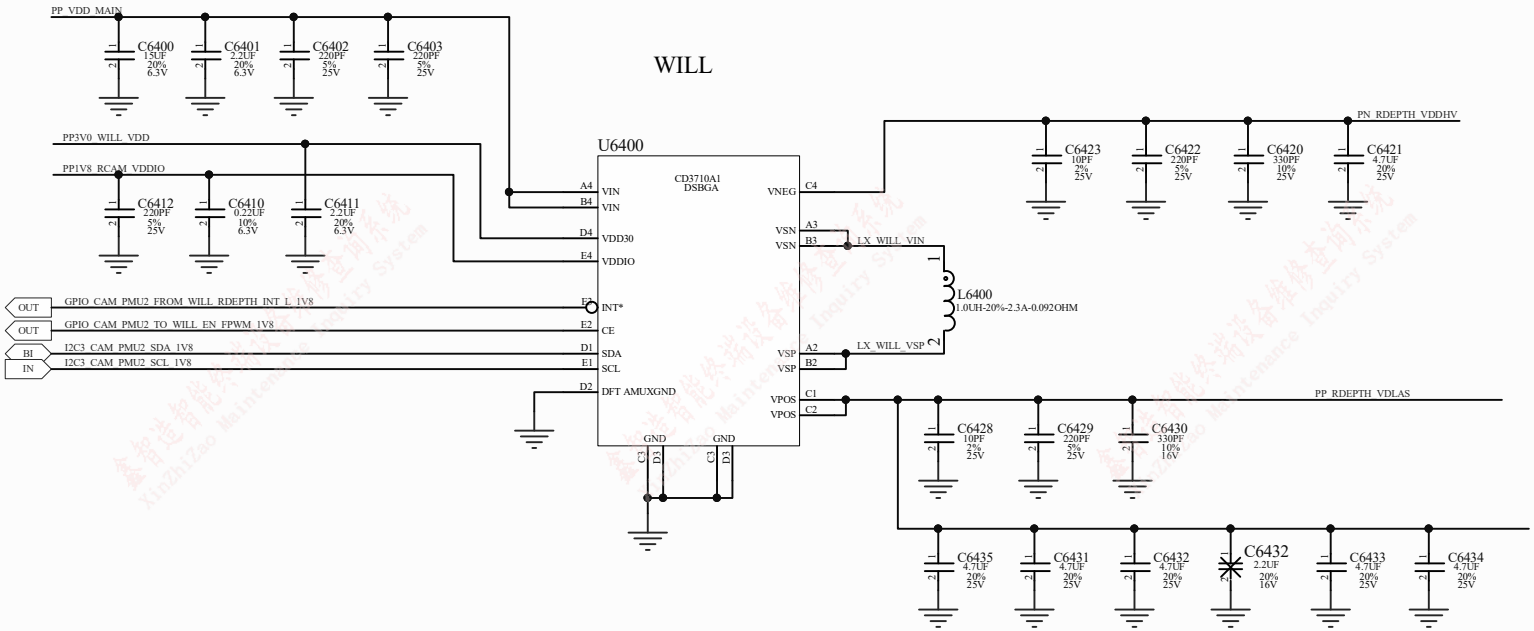

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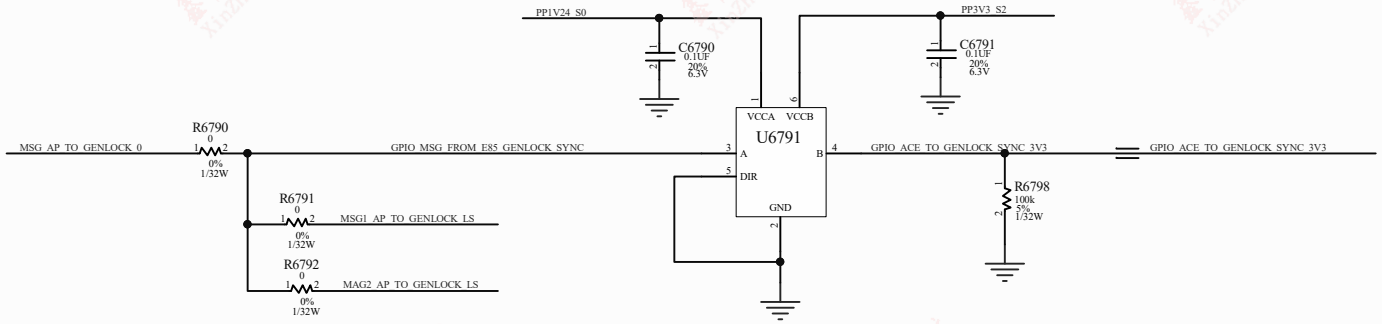

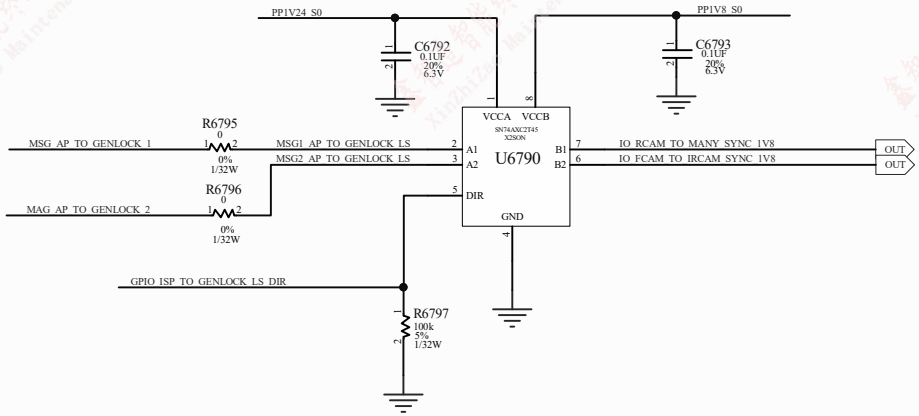

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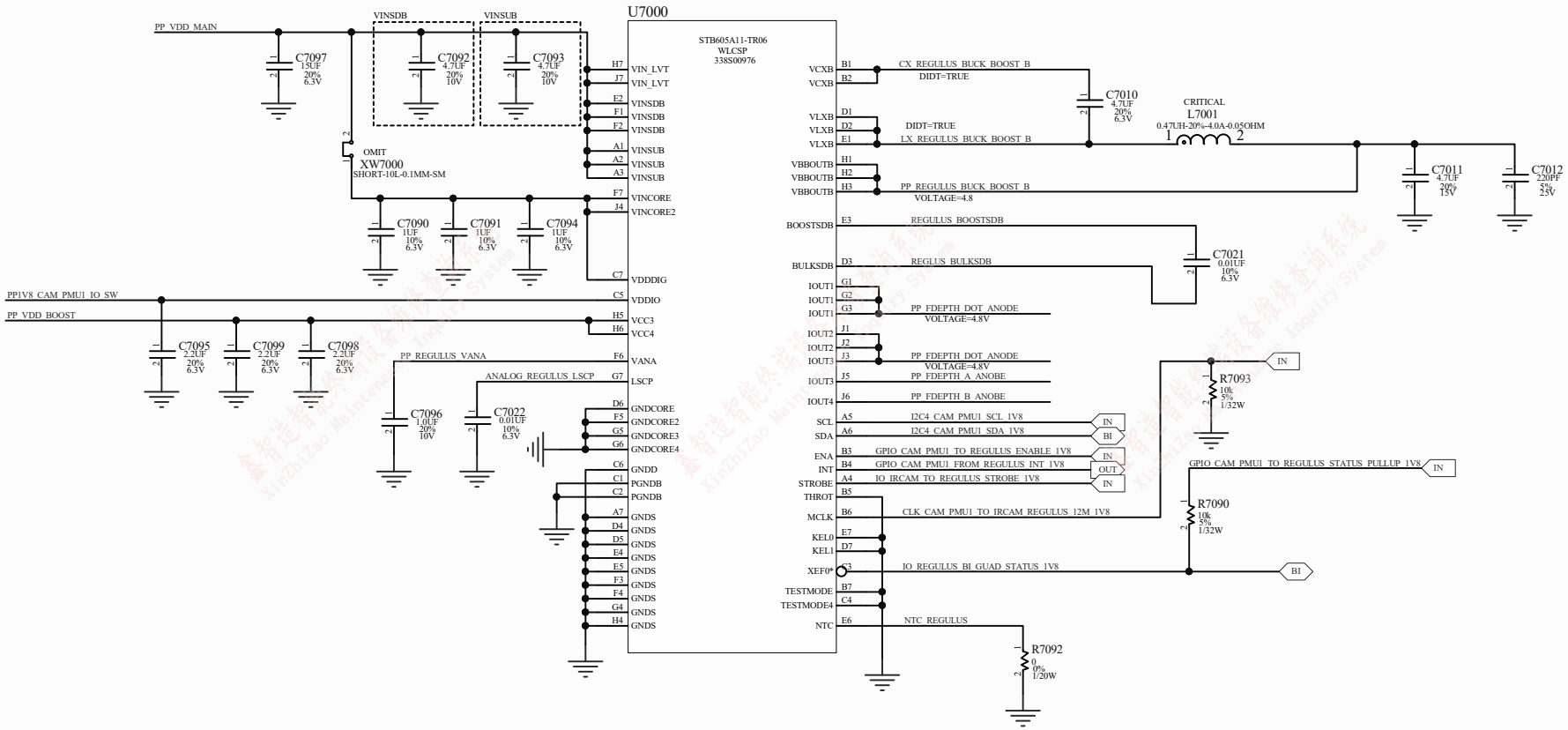

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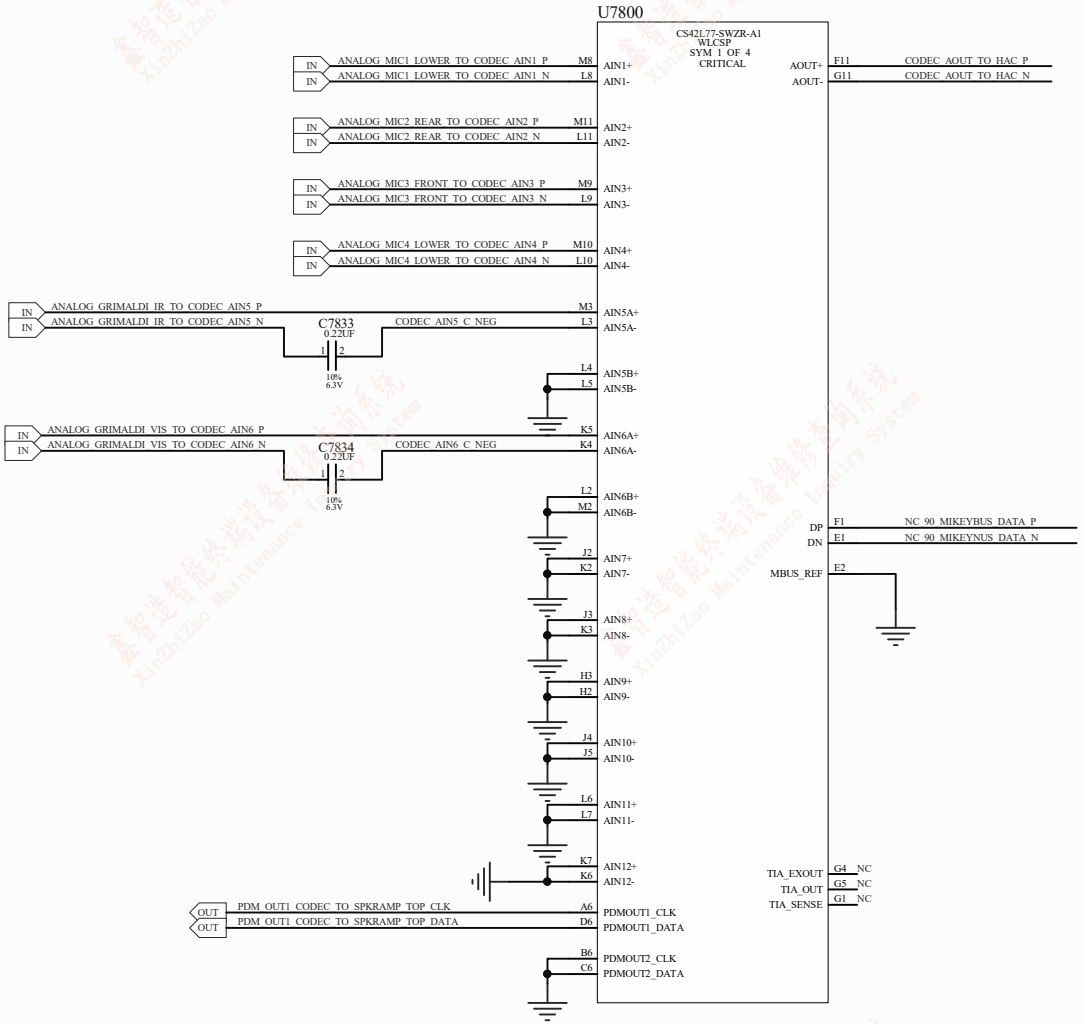

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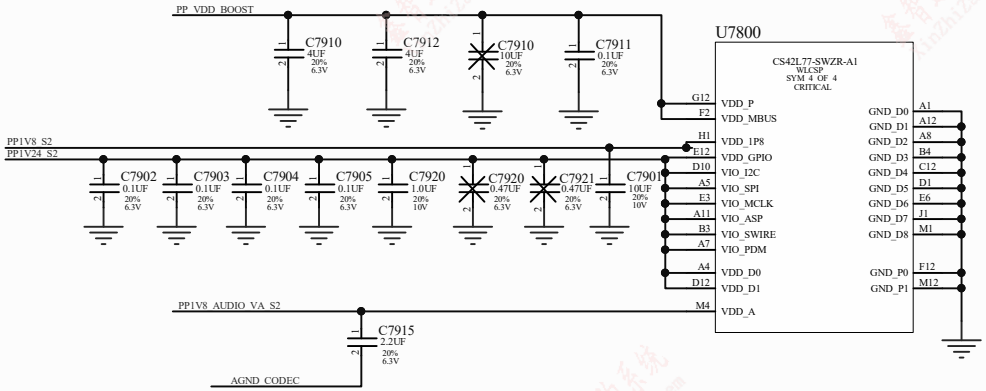

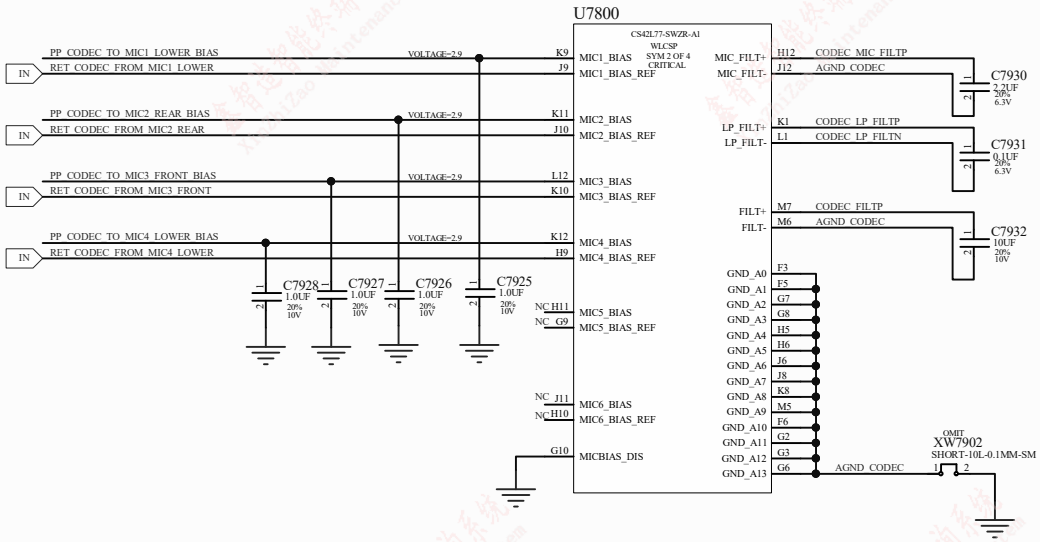

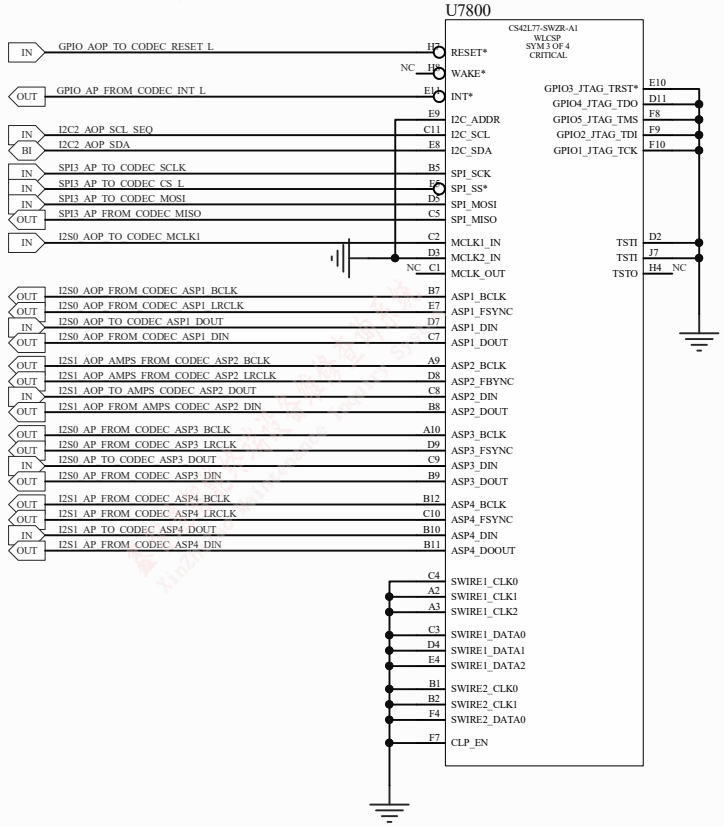

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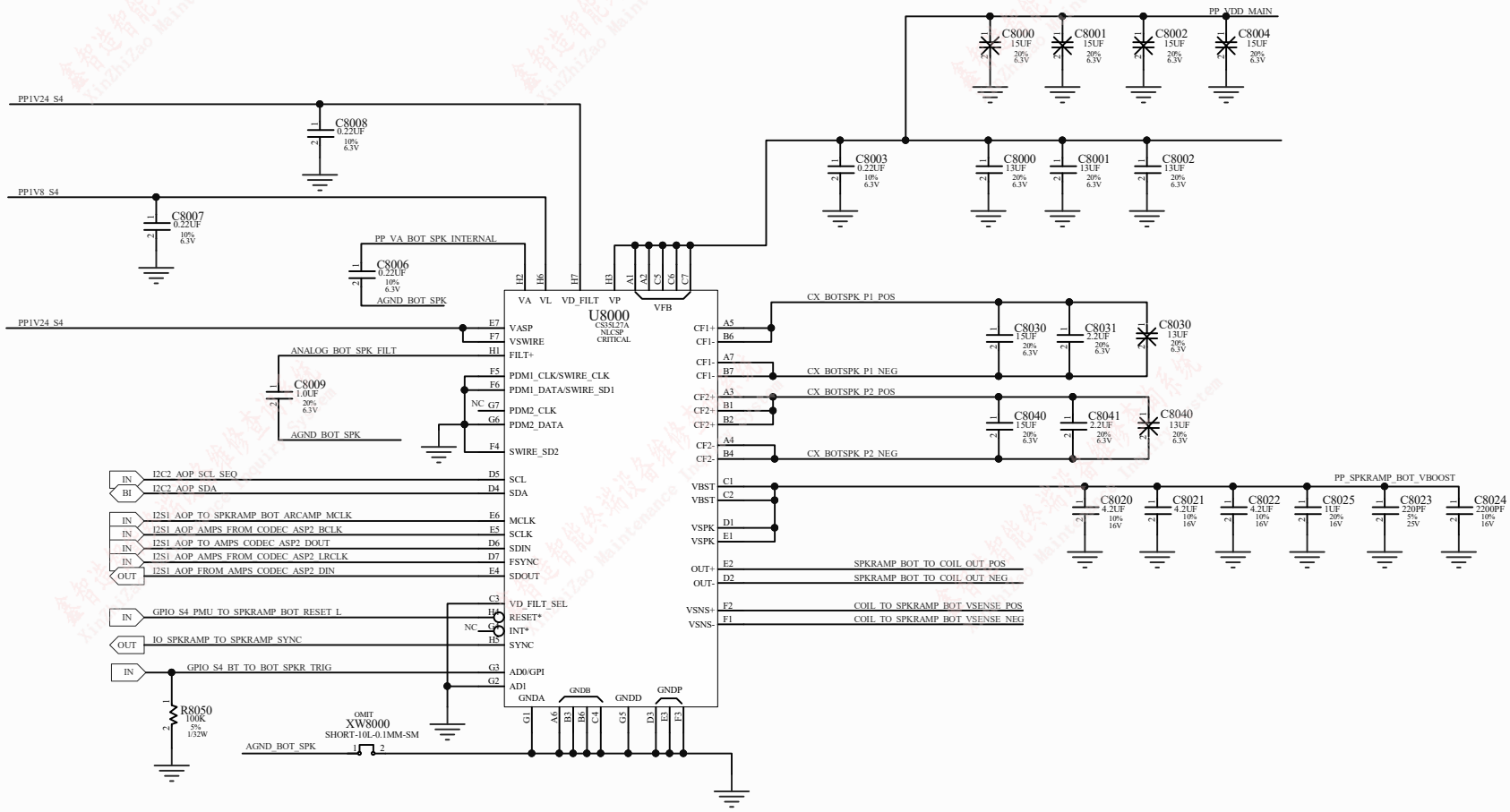

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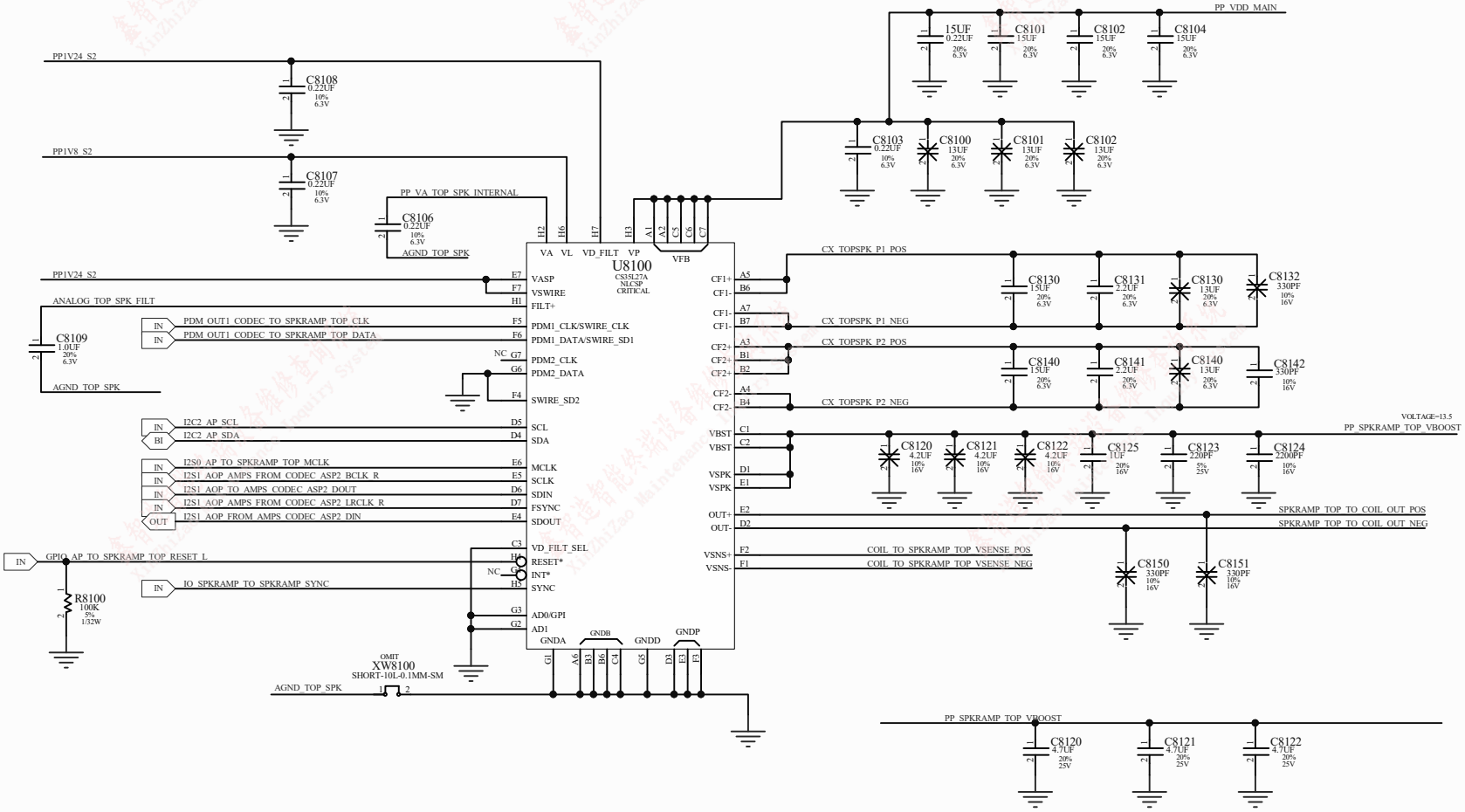

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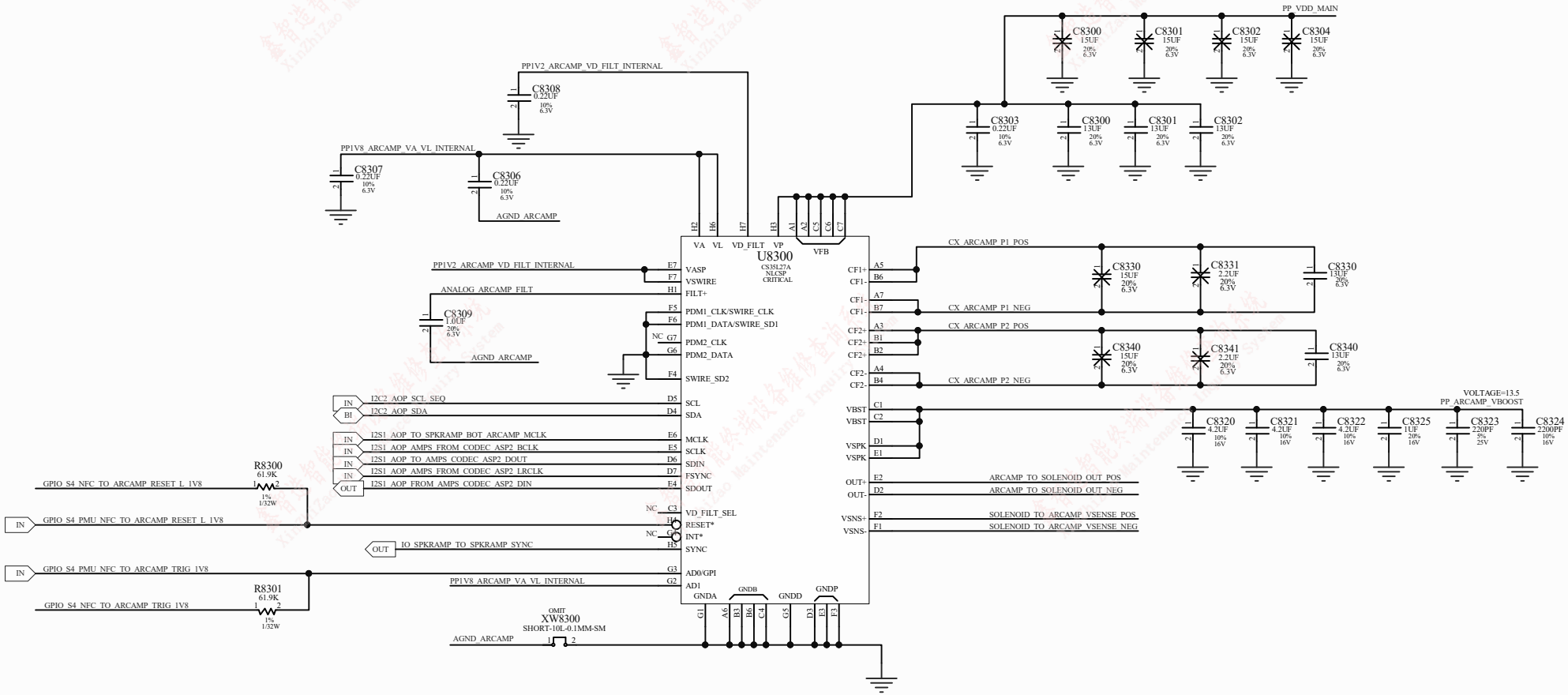

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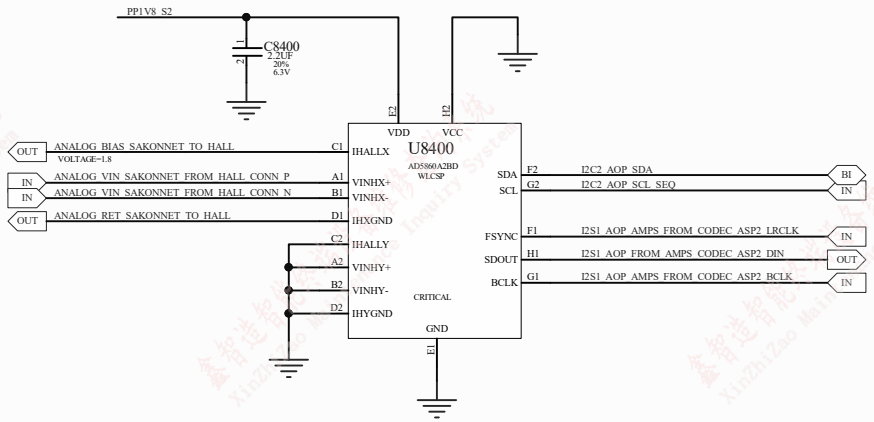

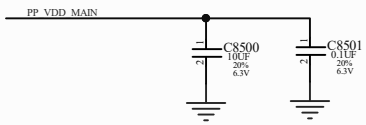

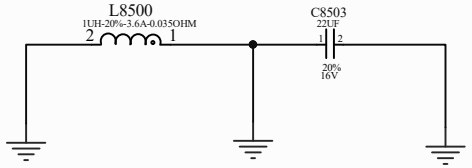

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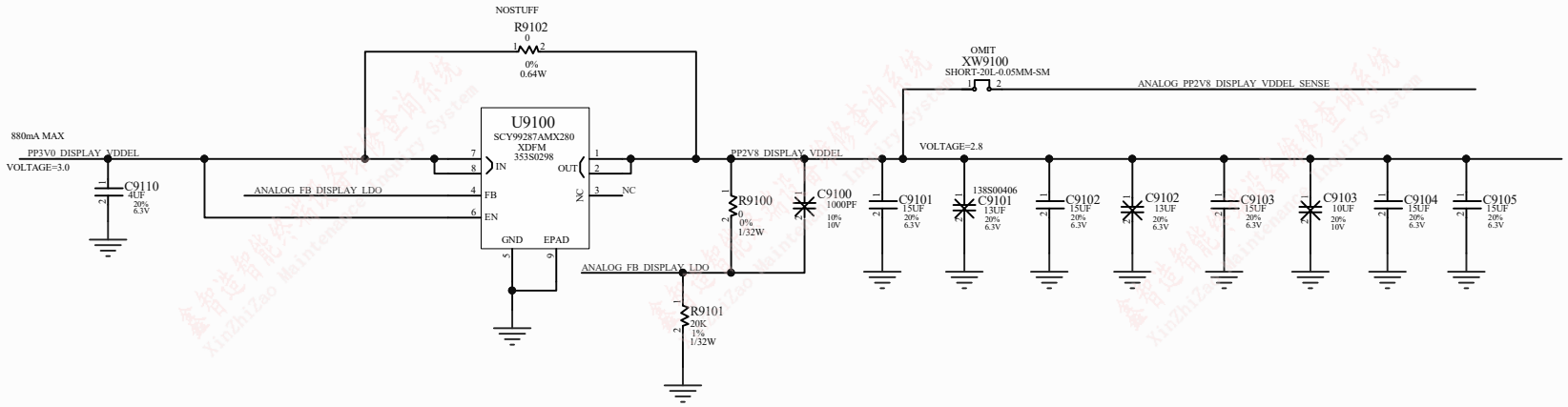

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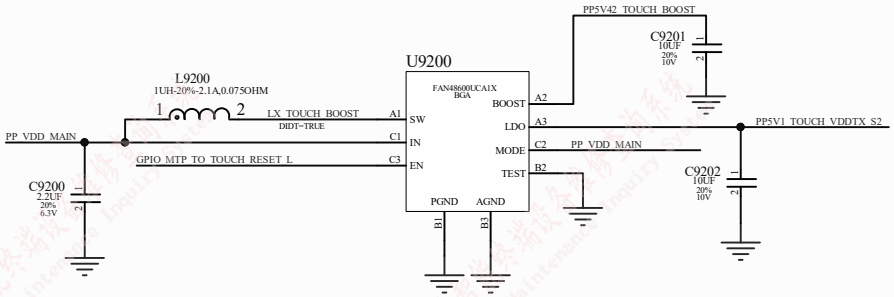

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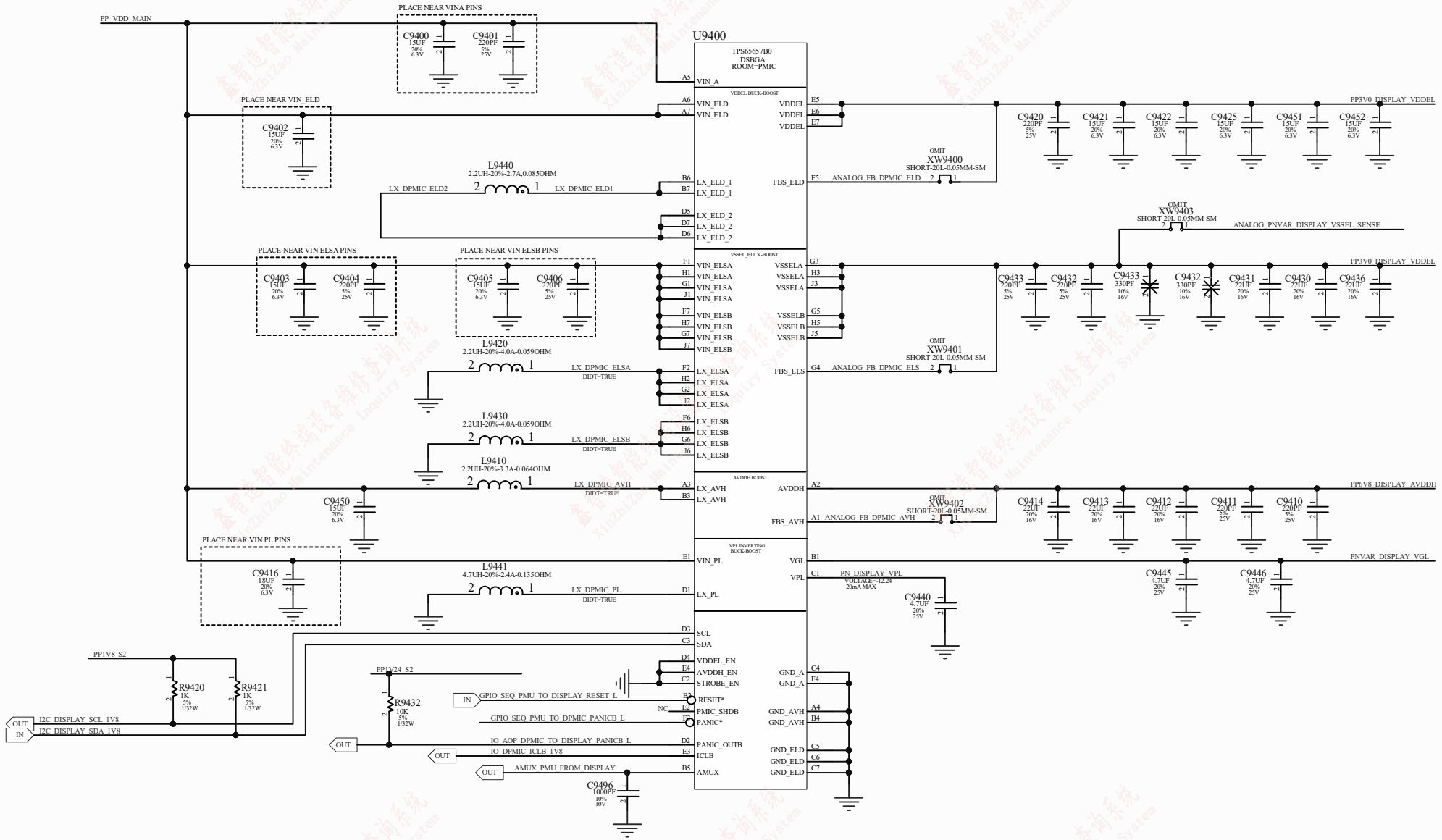

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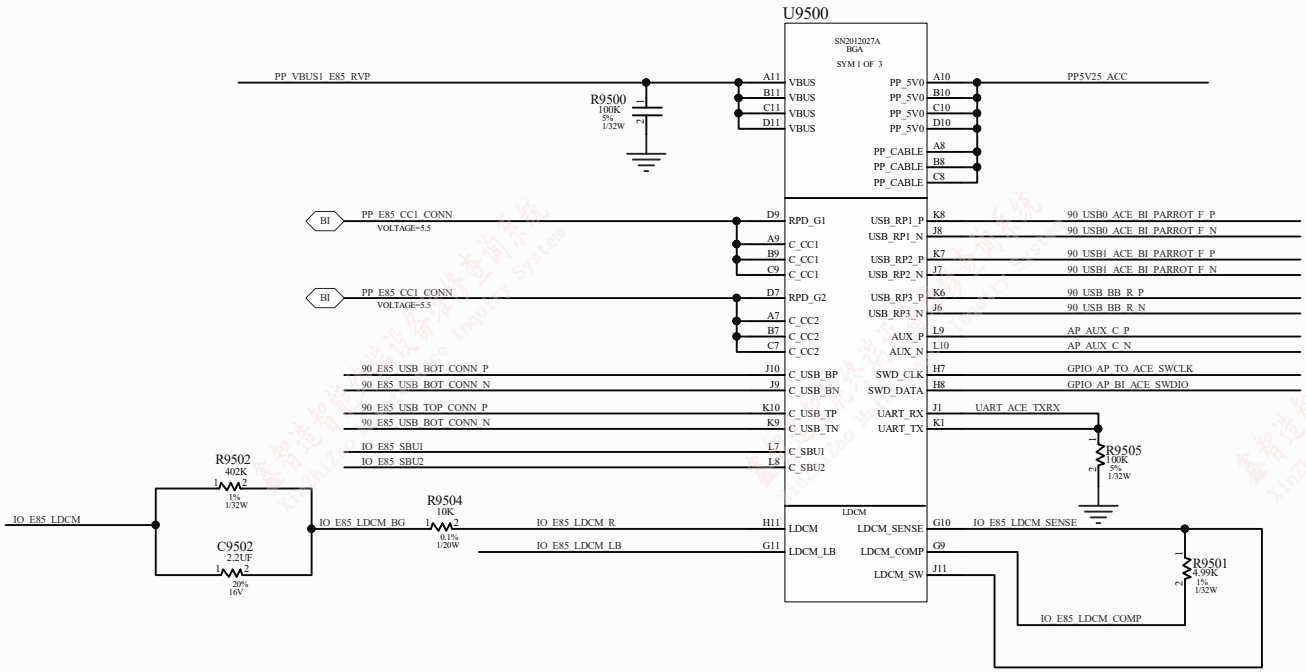

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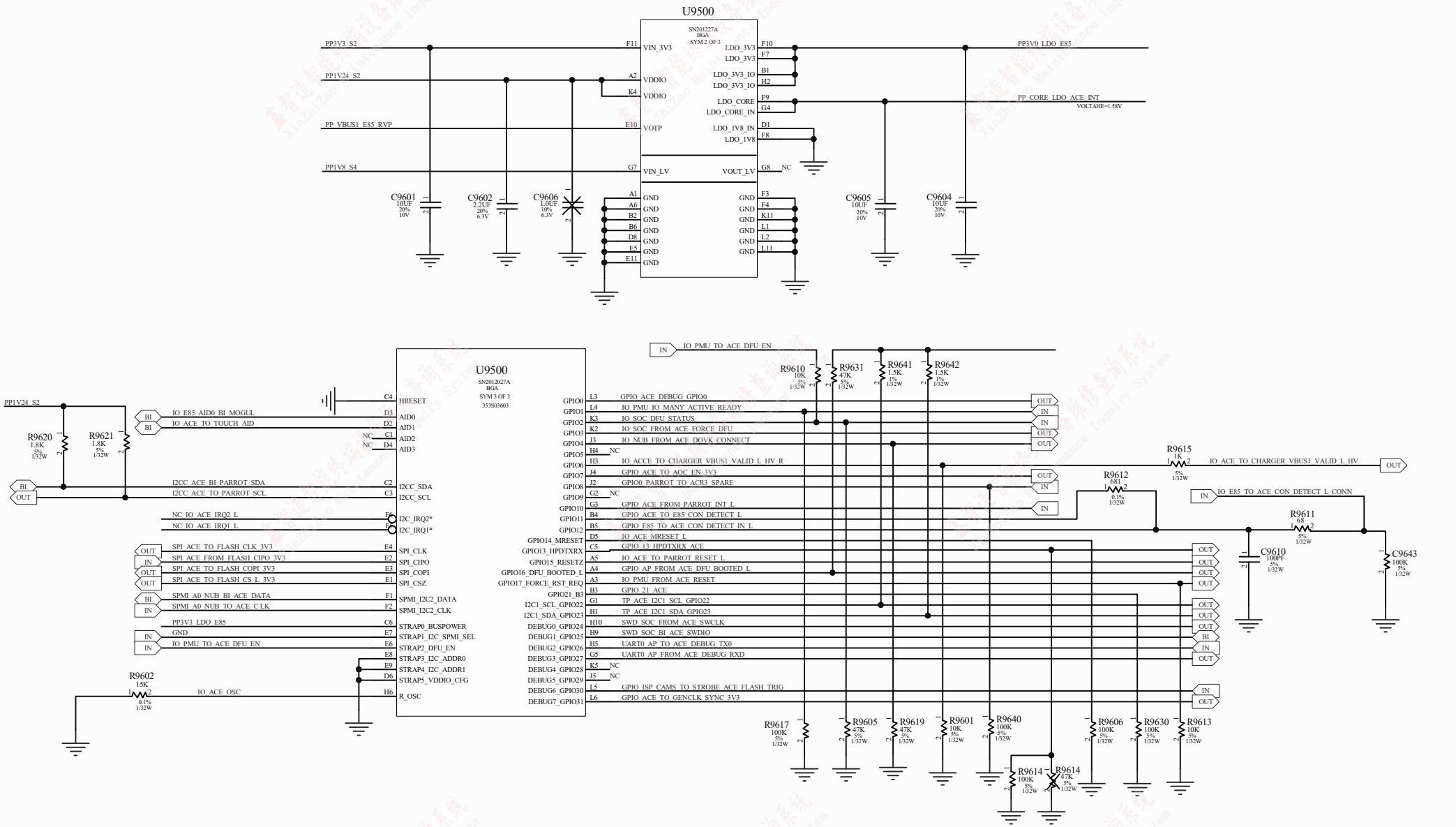
U9500
SN201227A
BGA
SYM 2 OF 3
PP3V3_S2
PP1V24_S2
PP_VBUS1_E85_RVP
PP1V8_S4
VIN_3V3
VDDIO
VDDIO
VOTP
VIN_LV
VOUT_LV
LDO_3V3
LDO_3V3_IO
LDO_CORE
LDO_CORE_IN
LDO_1V8_IN
LDO_1V8
GND
PP3V0_LDO_E85
PP_CORE_LDO_ACE_INT
VOLTAHE=1.58V
C9601 10UF 20% 10V
C9602 2.2UF 20% 6.3V
C9606 1.0UF 10% 6.3V
C9605 10UF 20% 10V
C9604 10UF 20% 10V
U9500
SN201227A
BGA
SYM 3 OF 3
353S03603
HRESET
AID0
AID1
AID2
AID3
I2CC_SDA
I2CC_SCL
I2C_IRQ2*
I2C_IRQ1*
SPI_CLK
SPI_CIPO
SPI_COPI
SPI_CSZ
SPMI_I2C2_DATA
SPMI_I2C2_CLK
STRAP0_BUSPOWER
STRAP1_I2C_SPMI_SEL
STRAP2_DFU_EN
STRAP3_I2C_ADDR0
STRAP4_I2C_ADDR1
STRAP5_VDDIO_CFG
R_OSC
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO14_MRESET
GPIO13_HPDTXRX
GPIO15_RESETZ
GPIO16_DFU_BOOTED_L
GPIO17_FORCE_RST_REQ
GPIO21_B3
I2C1_SCL_GPIO22
I2C1_SDA_GPIO23
DEBUG0_GPIO24
DEBUG1_GPIO25
DEBUG2_GPIO26
DEBUG3_GPIO27
DEBUG4_GPIO28
DEBUG5_GPIO29
DEBUG6_GPIO30
DEBUG7_GPIO31
IO_PMU_TO_ACE_DFU_EN
GPIO_ACE_DEBUG_GPIO0
IO_PMU_IO_MANY_ACTIVE_READY
IO_SOC_DFU_STATUS
IO_SOC_FROM_ACE_FORCE_DFU
IO_NUB_FROM_ACE_DOVK_CONNECT
IO_ACCE_TO_CHARGER_VBUS1_VALID_L_HV_R
GPIO_ACE_TO_AOC_EN_3V3
GPIO0_PARROT_TO_ACR3_SPARE
GPIO_ACE_FROM_PARROT_INT_L
GPIO_ACE_TO_E85_CON_DETECT_L
GPIO_E85_TO_ACE_CON_DETECT_IN_L
IO_ACE_MRESET_L
GPIO_13_HPDTXRX_ACE
IO_ACE_TO_PARROT_RESET_L
GPIO_AP_FROM_ACE_DFU_BOOTED_L
IO_PMU_FROM_ACE_RESET
GPIO_21_ACE
TP_ACE_I2C1_SCL_GPIO22
TP_ACE_I2C1_SDA_GPIO23
SWD_SOC_FROM_ACE_SWCLK
SWD_SOC_BI_ACE_SWDIO
UART0_AP_TO_ACE_DEBUG_TX0
UART0_AP_FROM_ACE_DEBUG_RXD
GPIO_ISP_CAMS_TO_STROBE_ACE_FLASH_TRIG
GPIO_ACE_TO_GENCLK_SYNC_3V3
IO_E85_AID0_BI_MOGUL
IO_ACE_TO_TOUCH_AID
I2CC_ACE_BI_PARROT_SDA
I2CC_ACE_TO_PARROT_SCL
NC_IO_ACE_IRQ2_L
NC_IO_ACE_IRQ1_L
SPI_ACE_TO_FLASH_CLK_3V3
SPI_ACE_FROM_FLASH_CIPO_3V3
SPI_ACE_TO_FLASH_COPI_3V3
SPI_ACE_TO_FLASH_CS_L_3V3
SPMI_A0_NUB_BI_ACE_DATA
SPMI_A0_NUB_TO_ACE_CLK
PP3V3_LDO_E85
GND
IO_PMU_TO_ACE_DFU_EN
IO_ACE_OSC
IO_ACE_TO_CHARGER_VBUS1_VALID_L_HV
IO_E85_TO_ACE_CON_DETECT_L_CONN
R9620 1.8K 5% 1/32W
R9621 1.8K 5% 1/32W
R9602 1.5K 0.1% 1/32W
R9610 10K 5% 1/32W
R9631 47K 5% 1/32W
R9641 1.5K 1% 1/32W
R9642 1.5K 1% 1/32W
R9615 1K 5% 1/32W
R9612 681 0.1% 1/32W
R9611 68 5% 1/32W
C9610 100PF 5% 1/32W
C9643 100K 5% 1/32W
R9617 100K 5% 1/32W
R9605 47K 5% 1/32W
R9619 47K 5% 1/32W
R9601 10K 5% 1/32W
R9640 100K 5% 1/32W
R9606 100K 5% 1/32W
R9630 100K 5% 1/32W
R9613 10K 5% 1/32W
R9614 100K 5% 1/32W
R9614 47K 5% 1/32W
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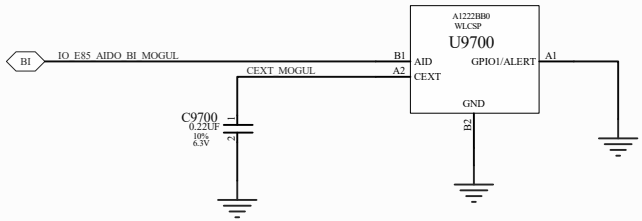

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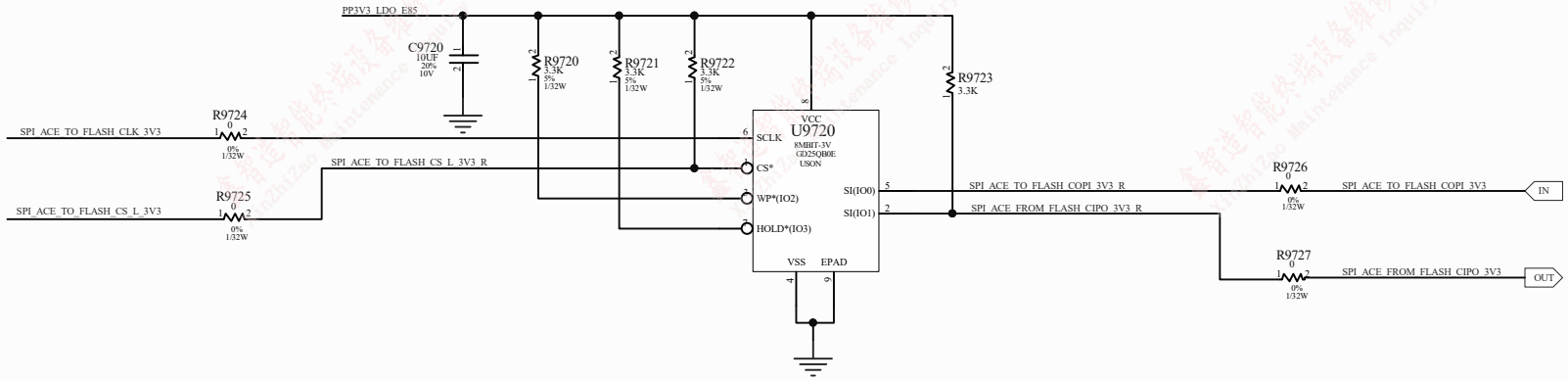

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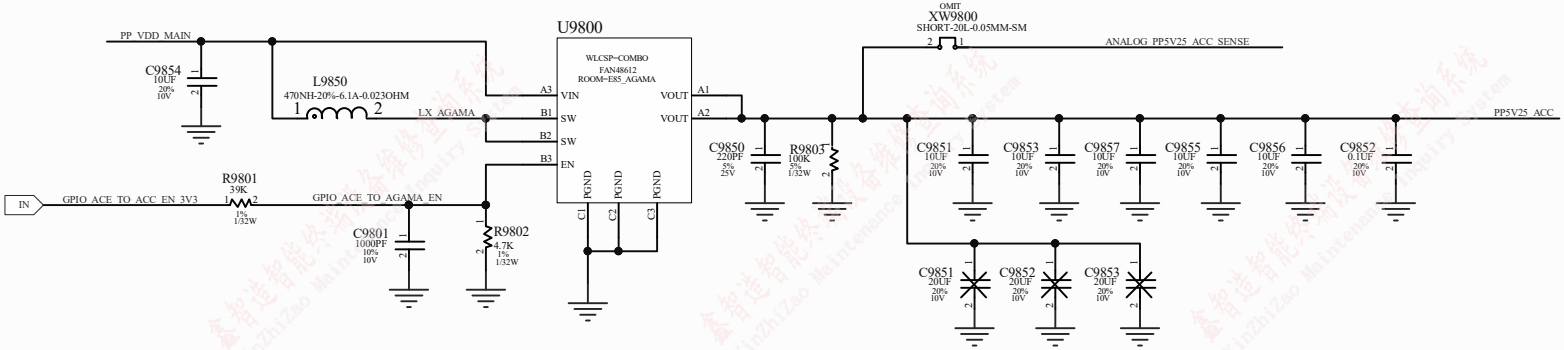

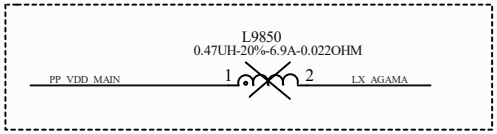

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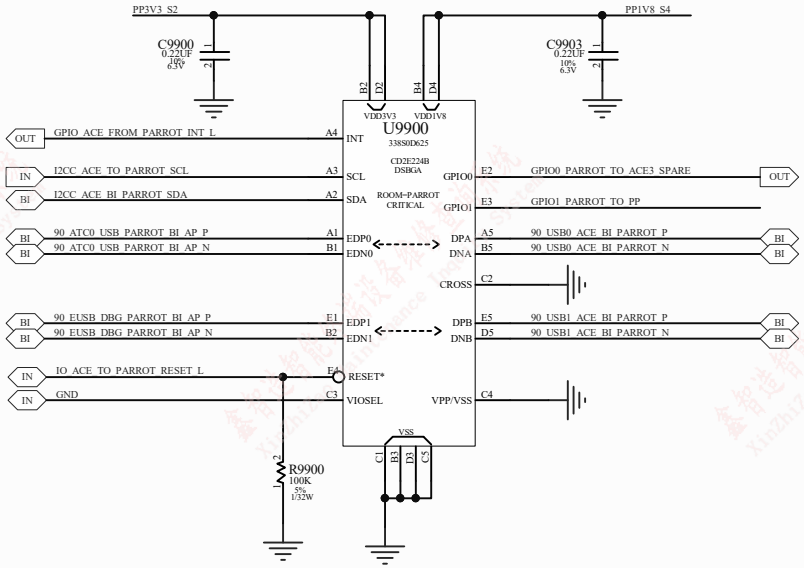

PLACE PARROT NEAR SOC

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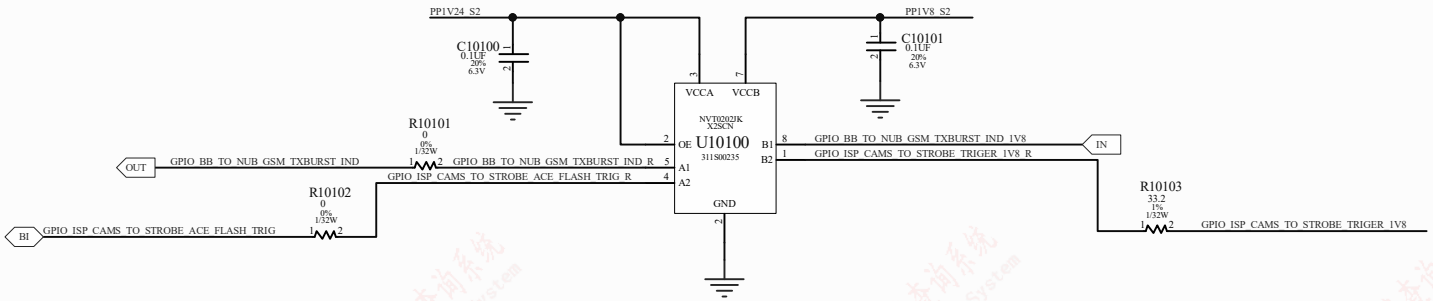

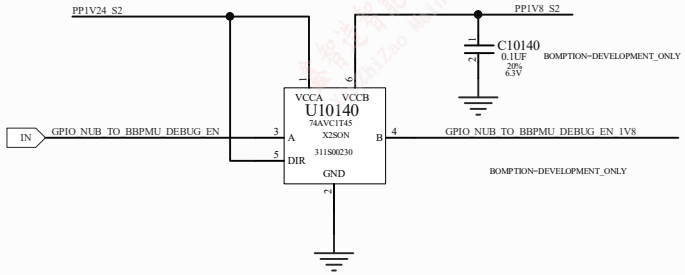

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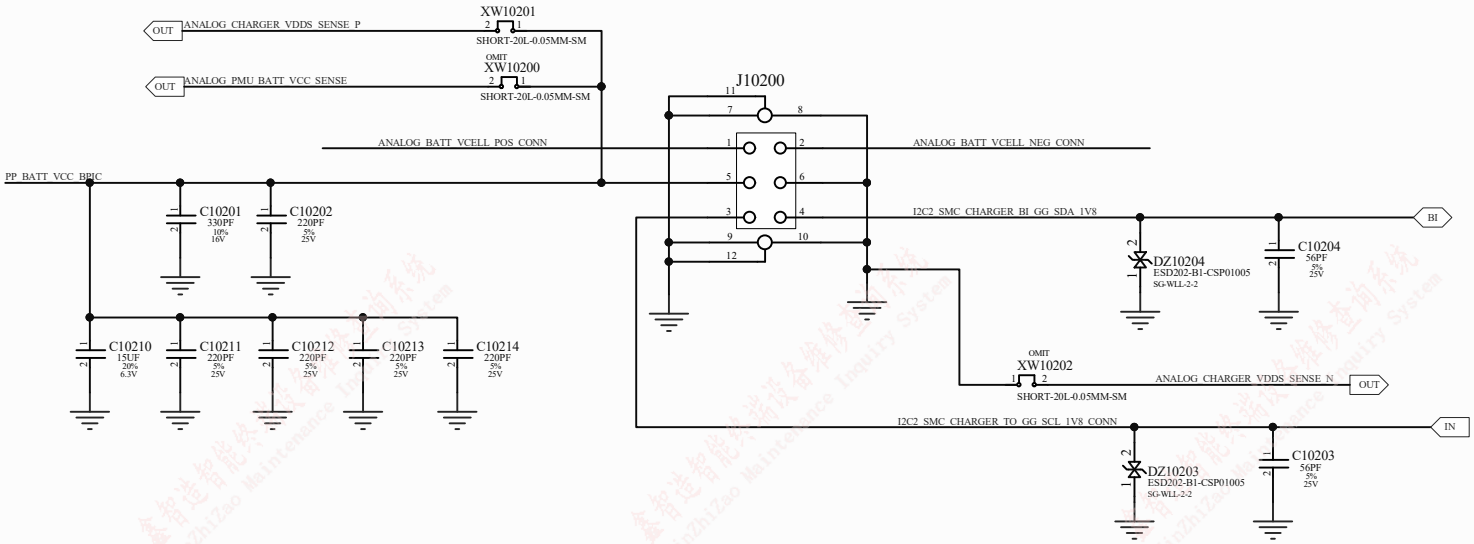
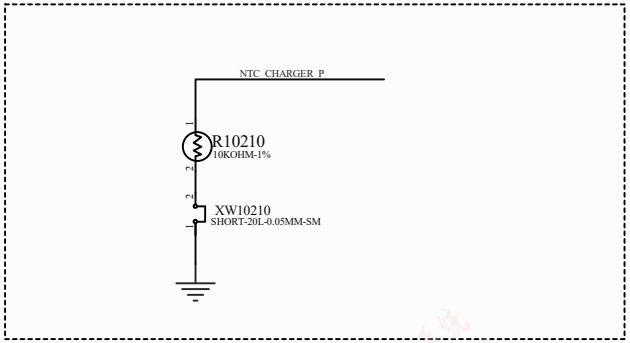


Rubicon NTC



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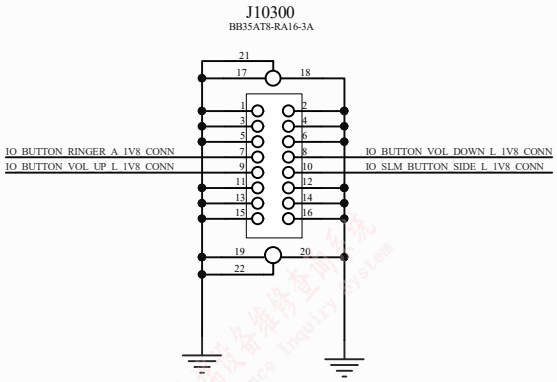

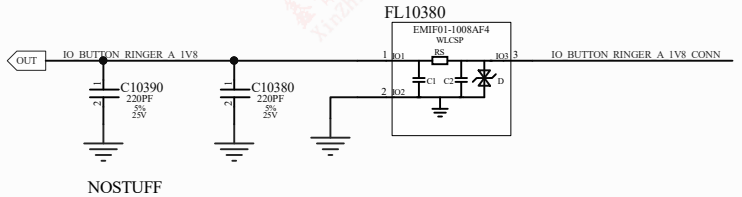

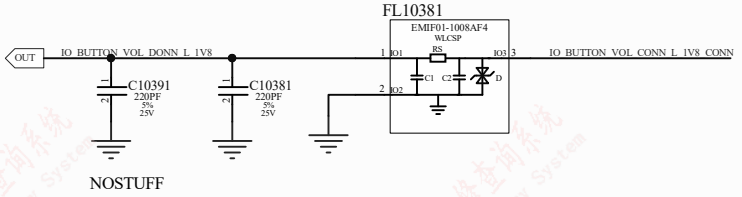

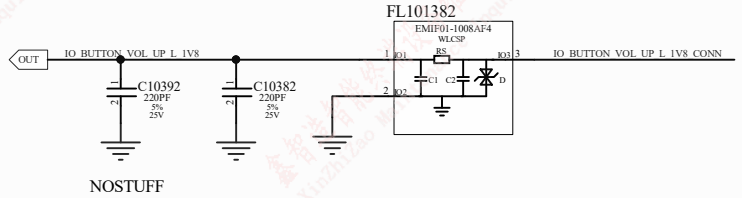

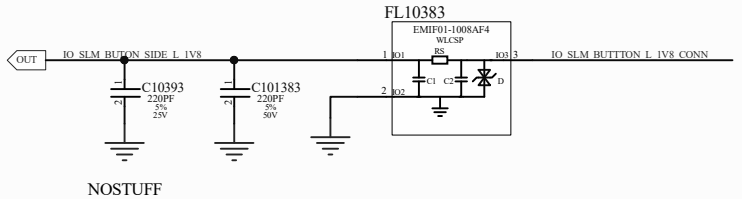

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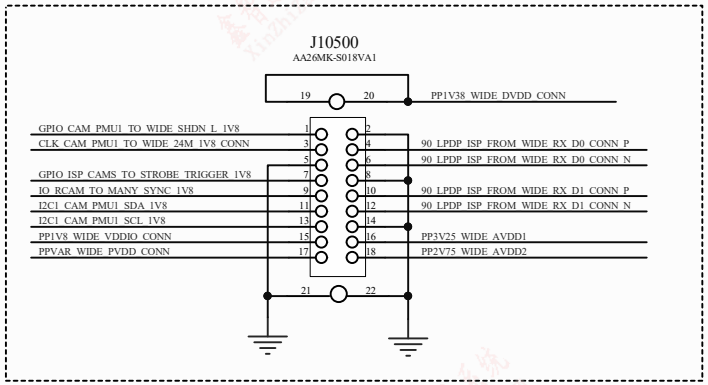

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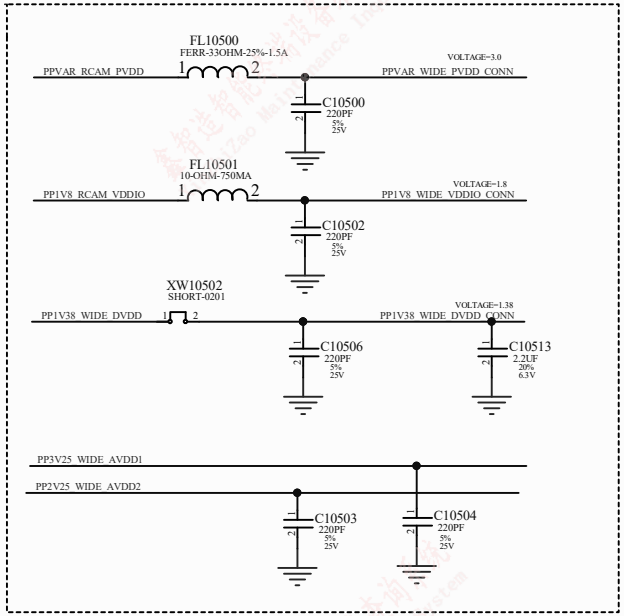

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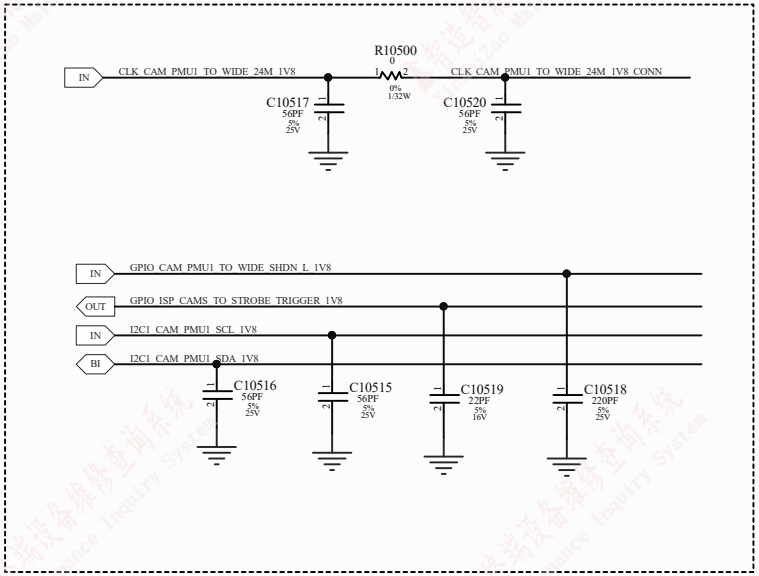

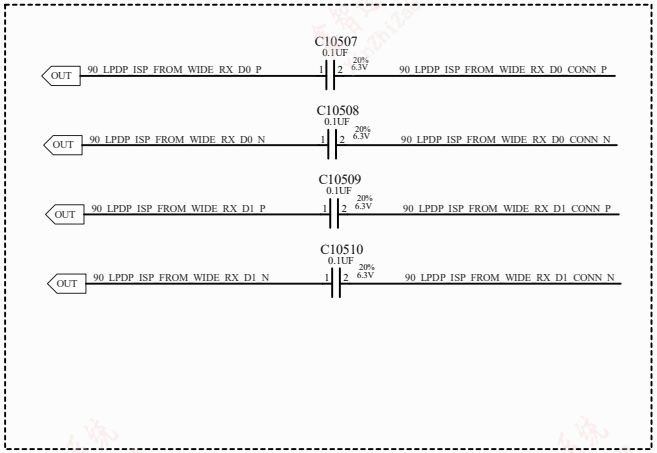

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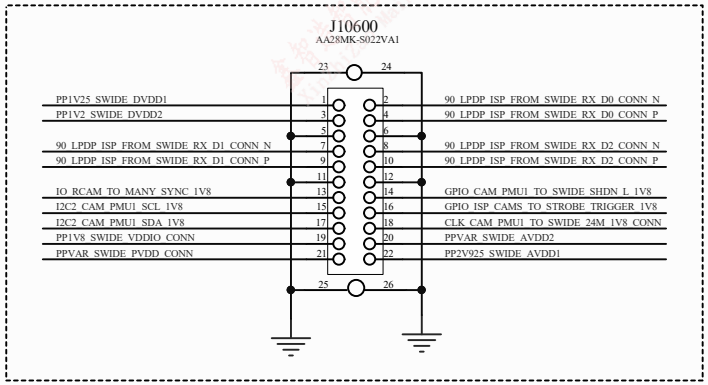

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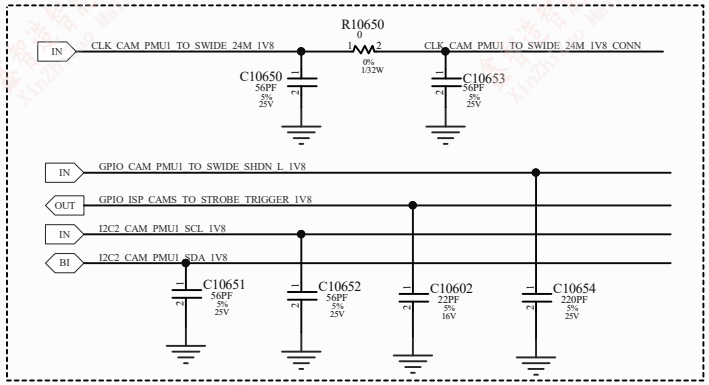

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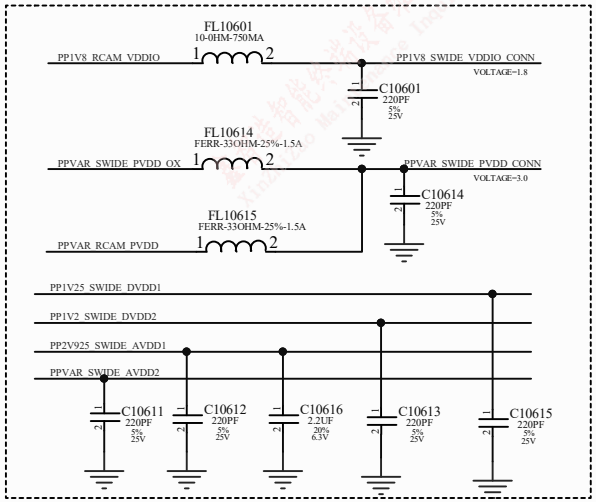

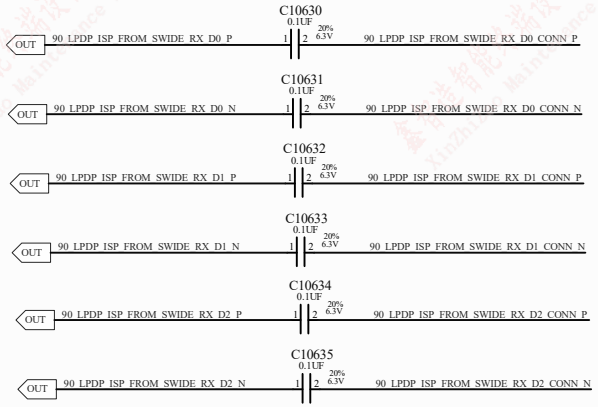

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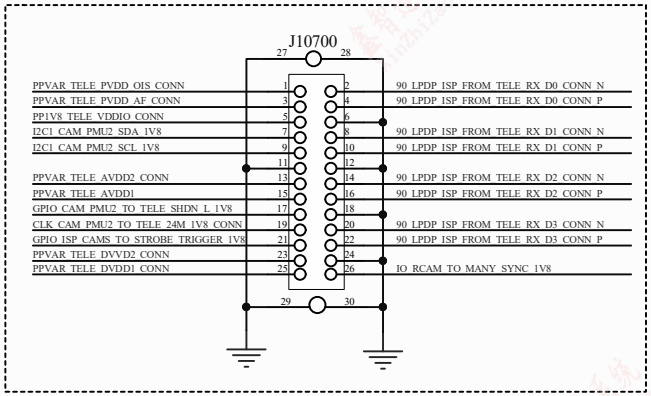

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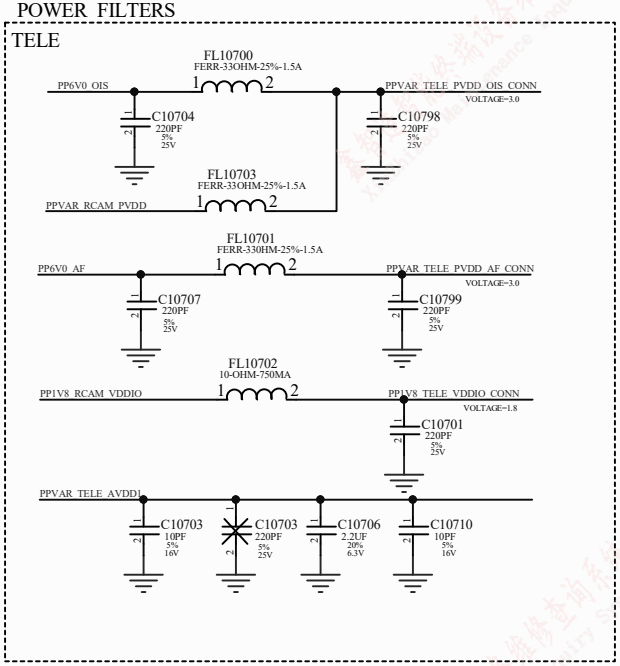

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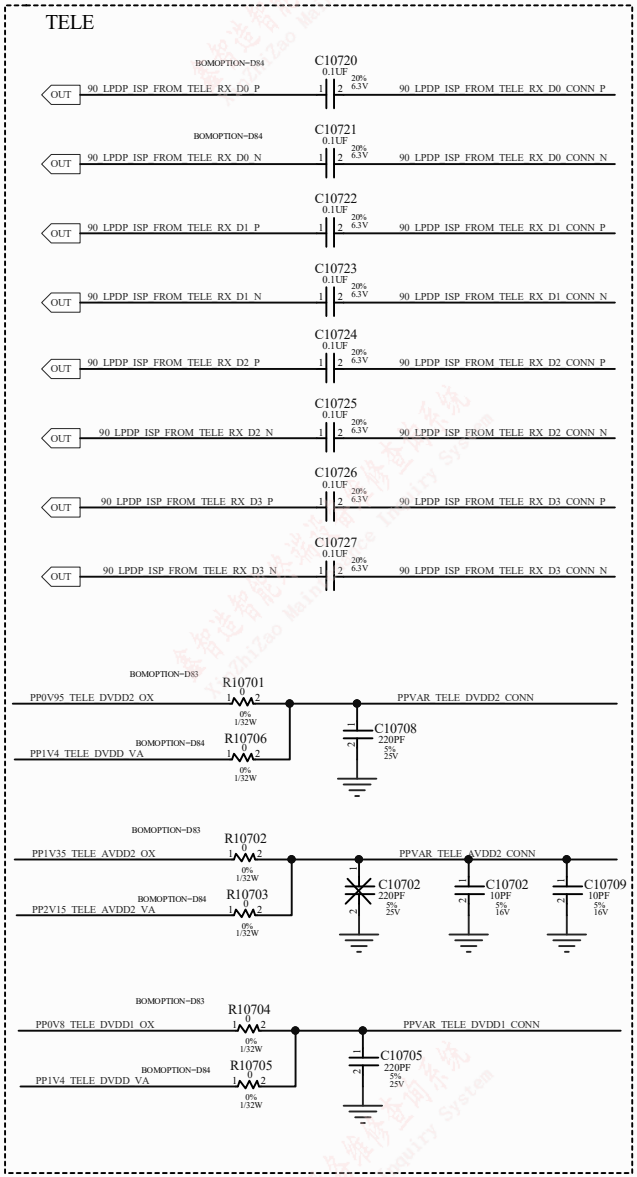

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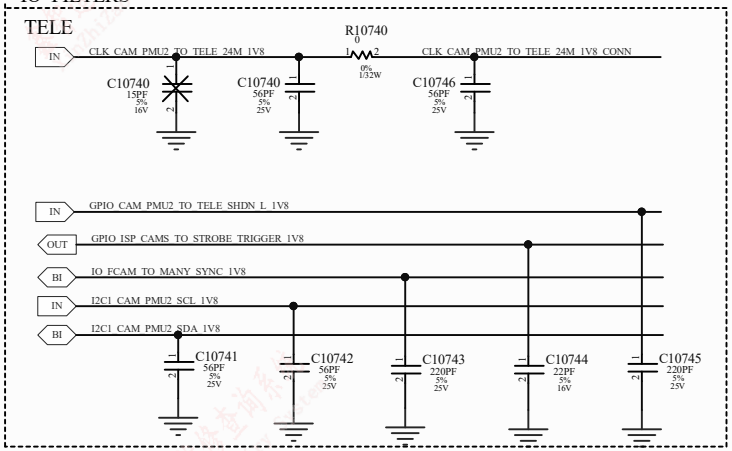

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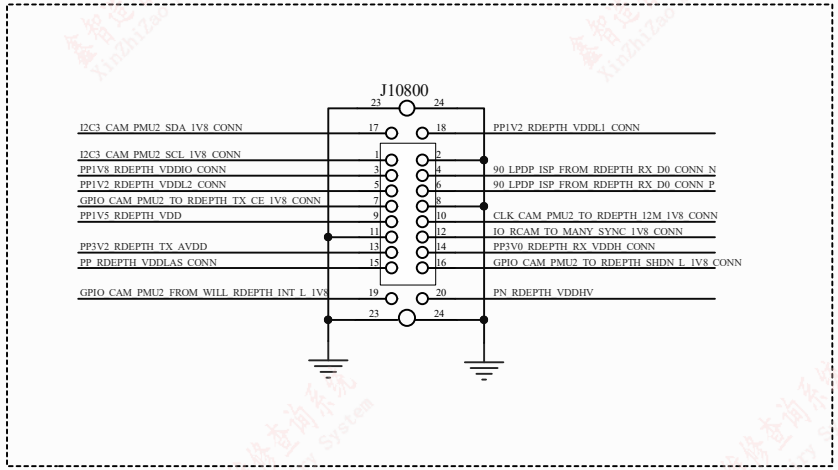

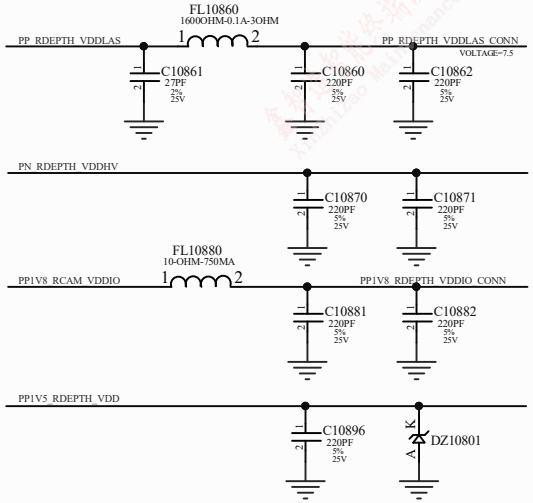

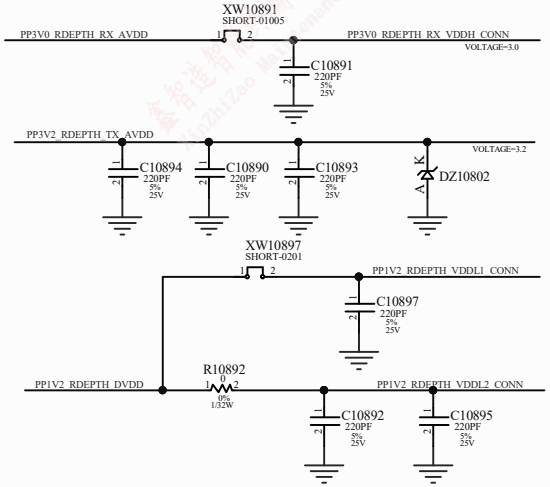

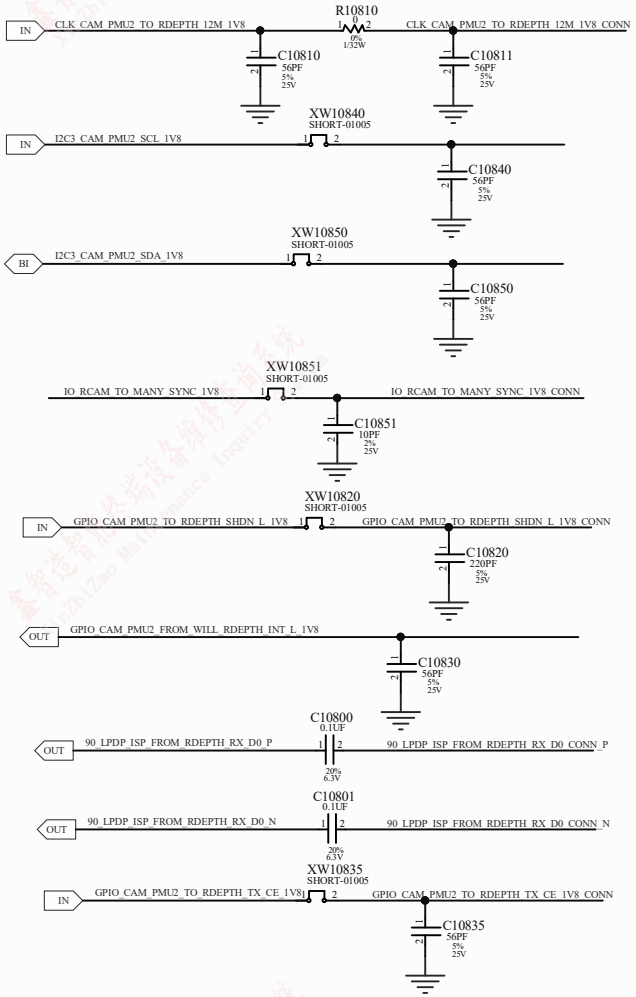

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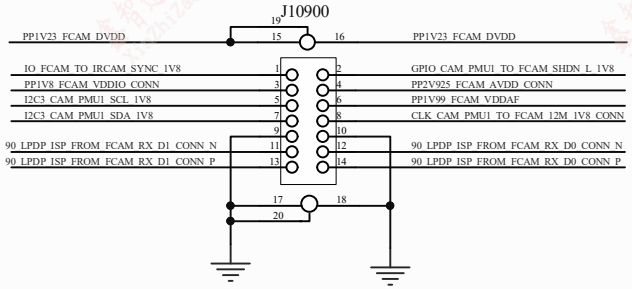

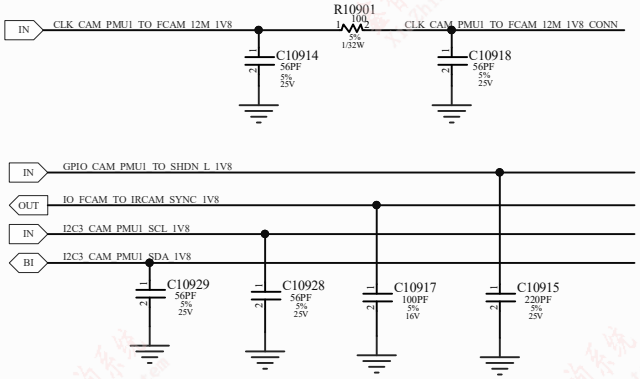

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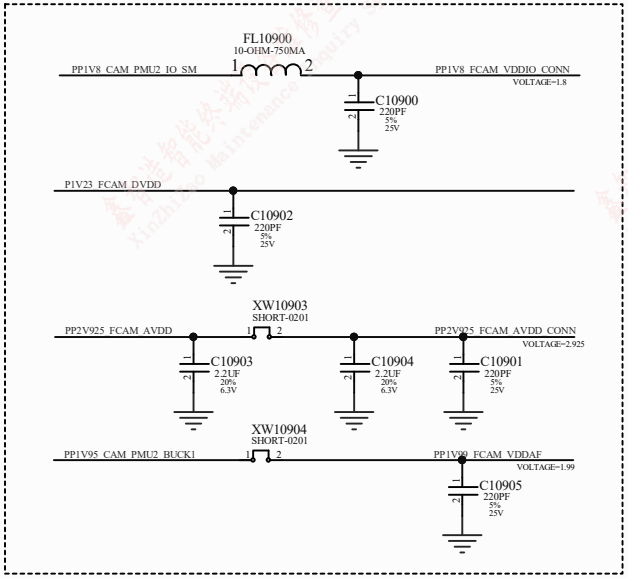

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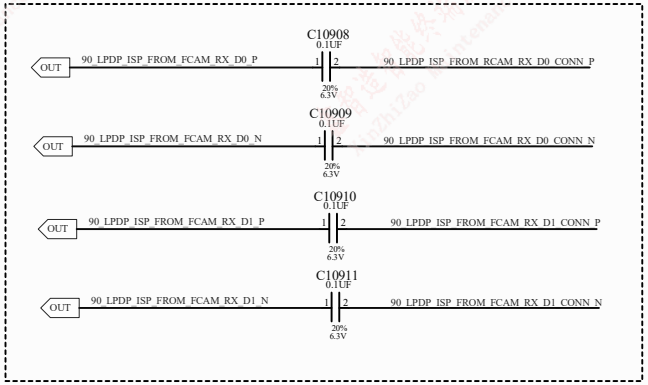

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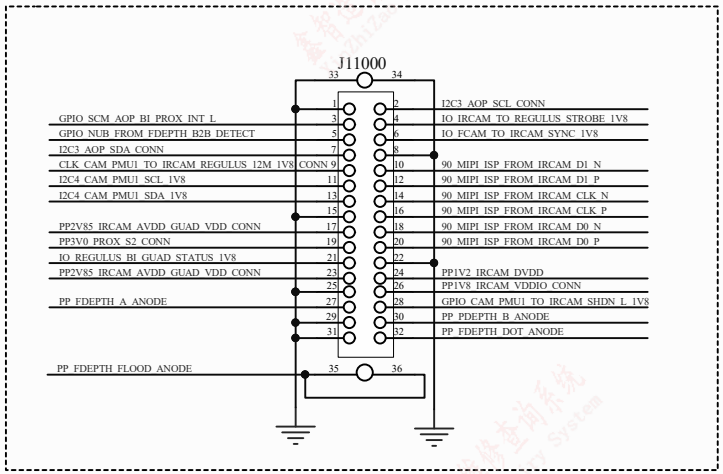

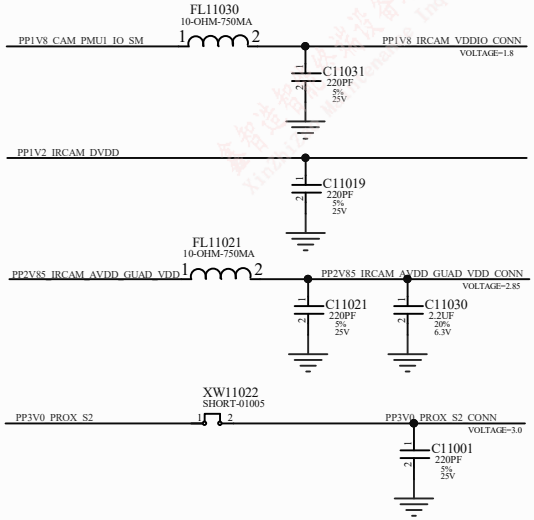

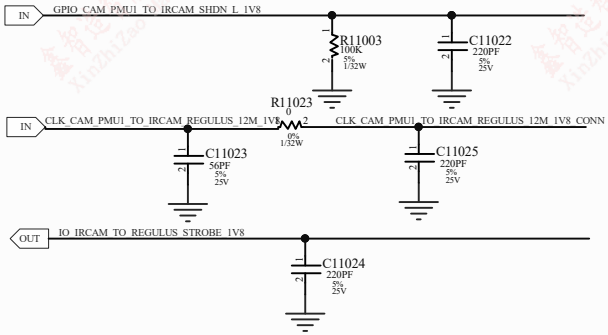

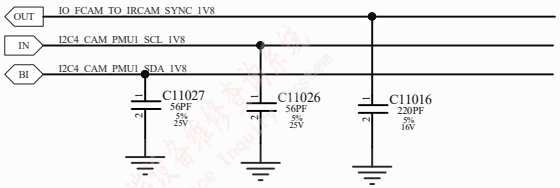

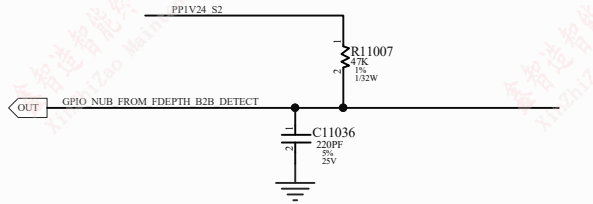

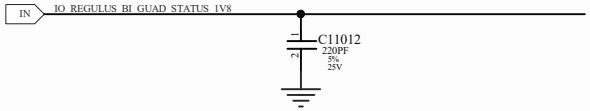

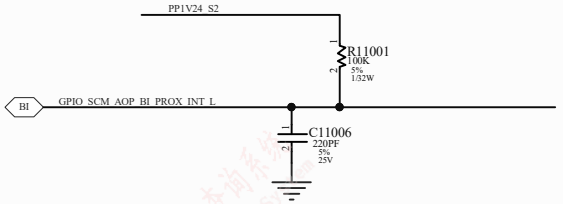

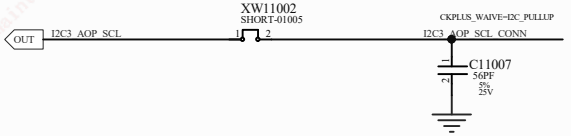

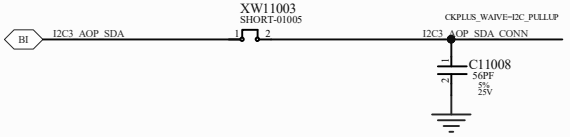

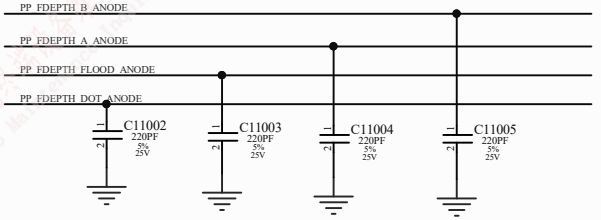

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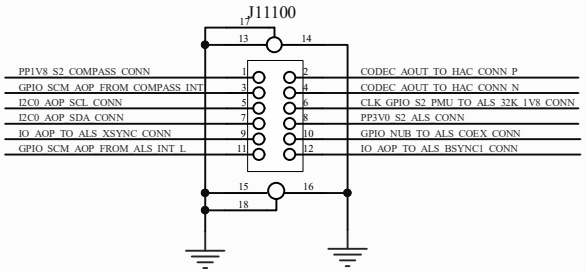

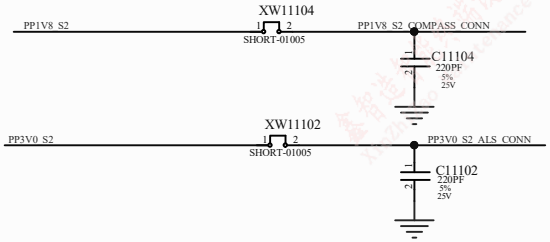

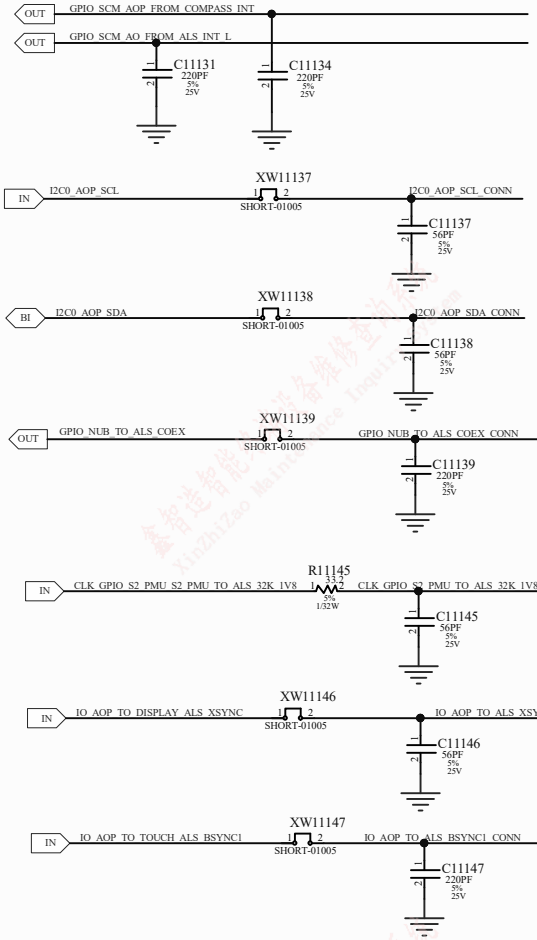

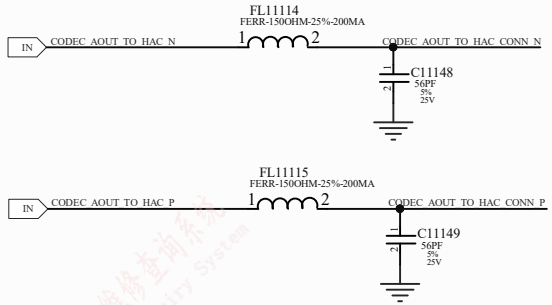

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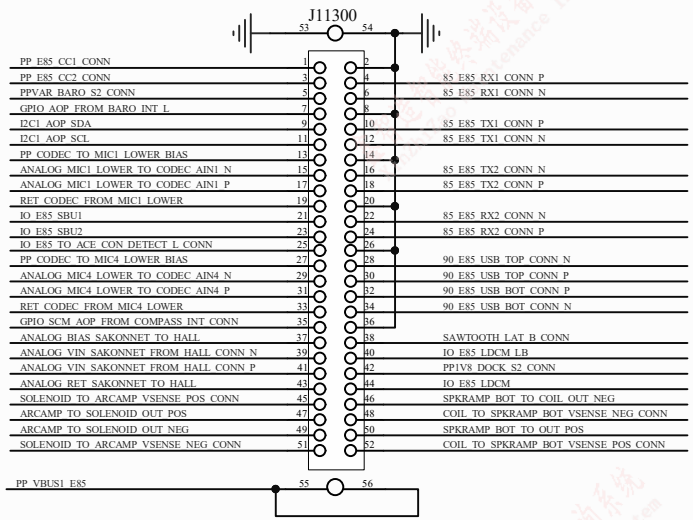

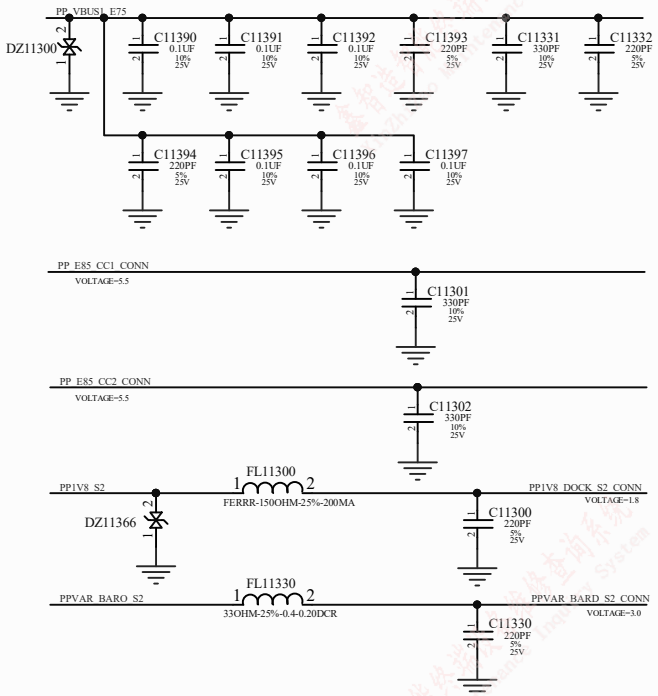

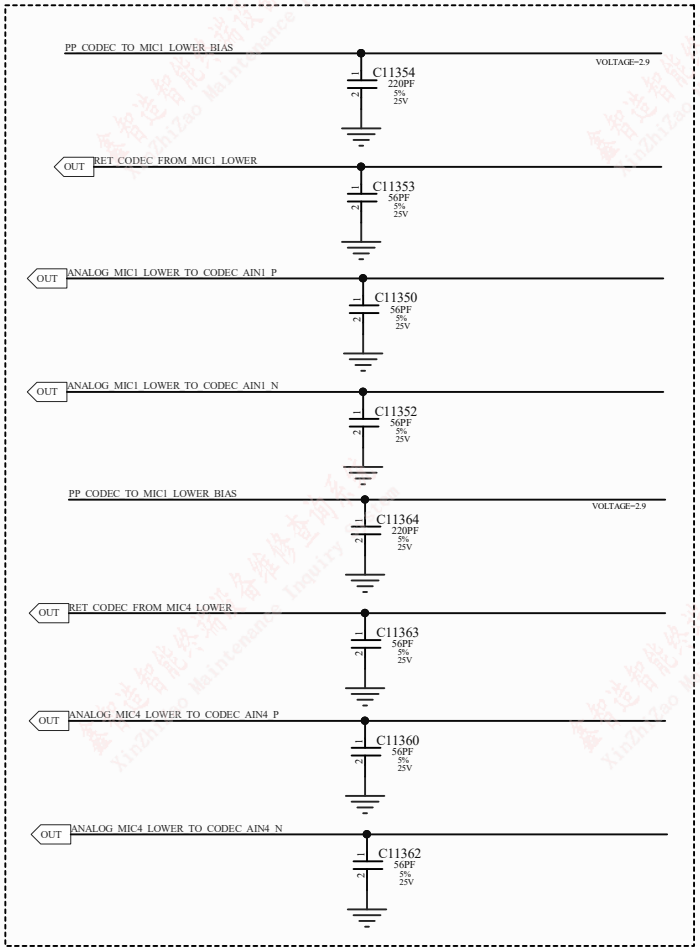

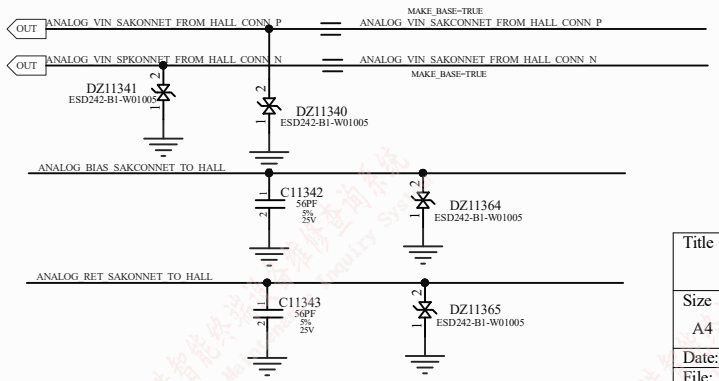

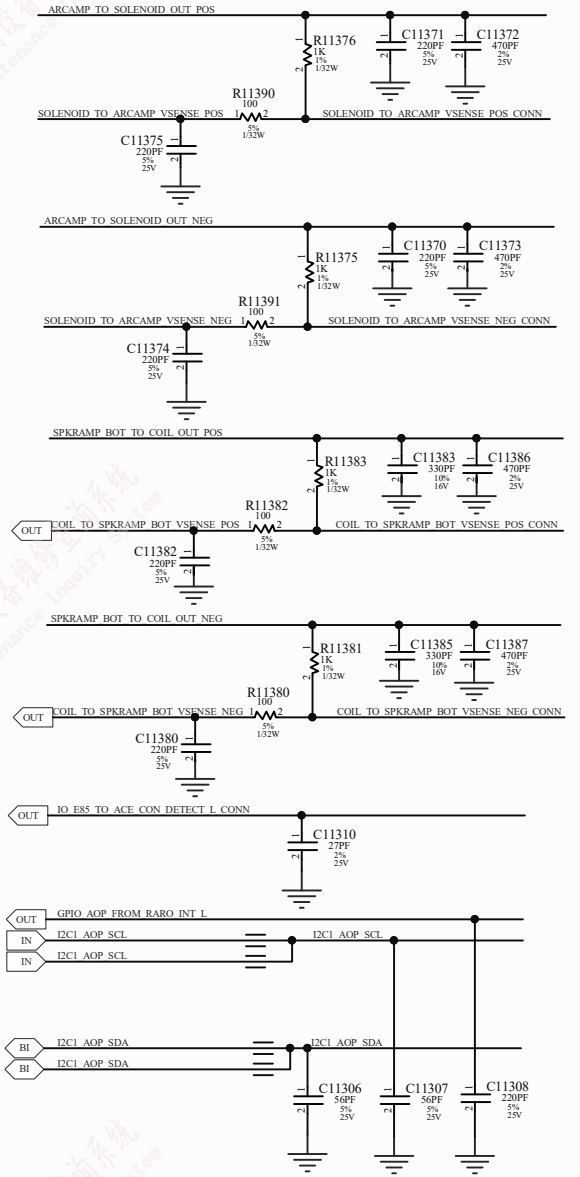

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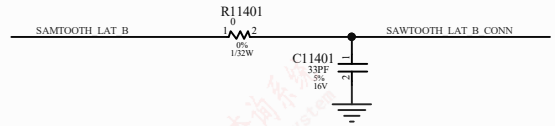

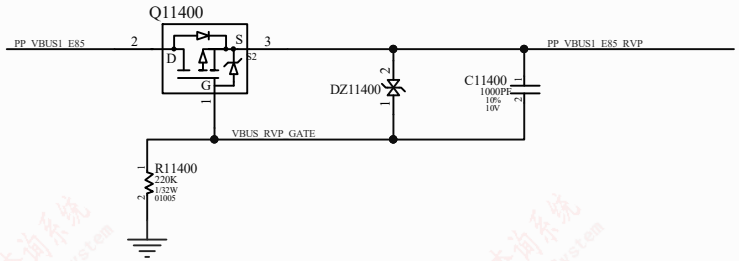

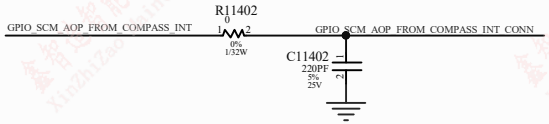

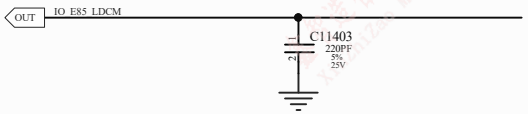

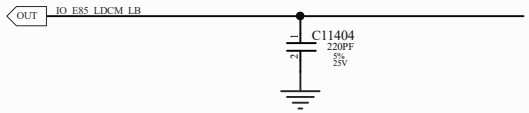

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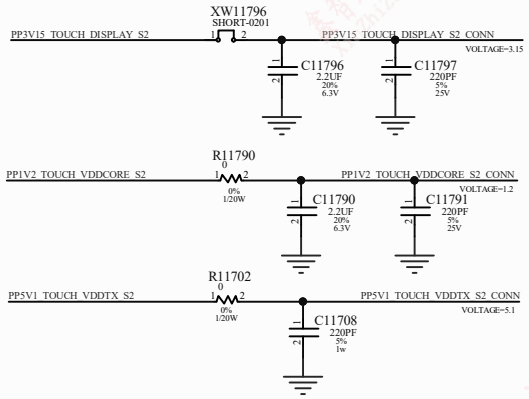

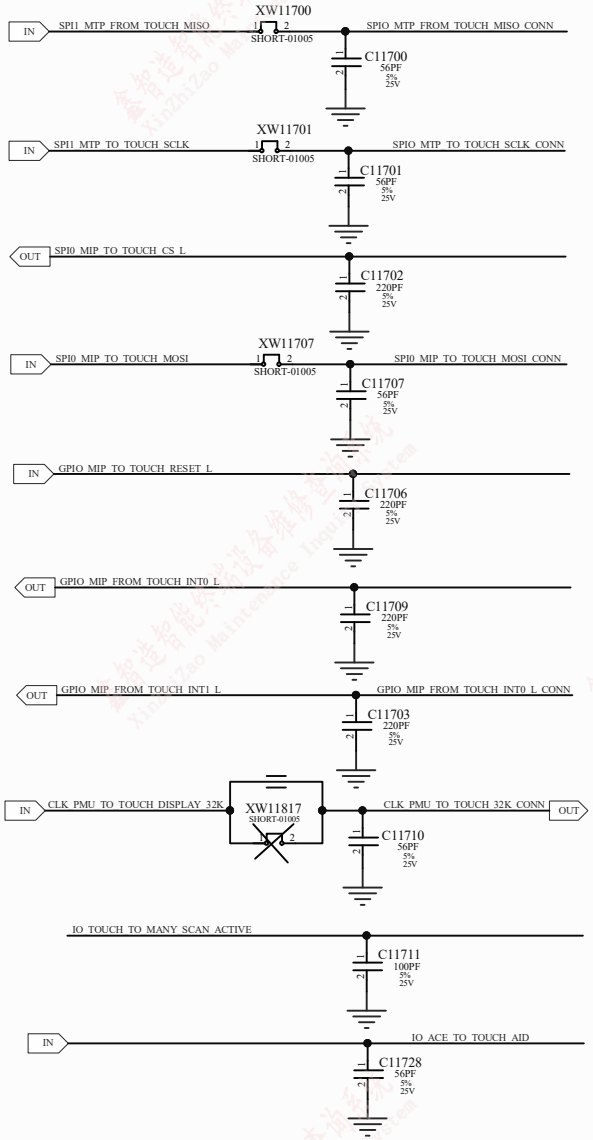

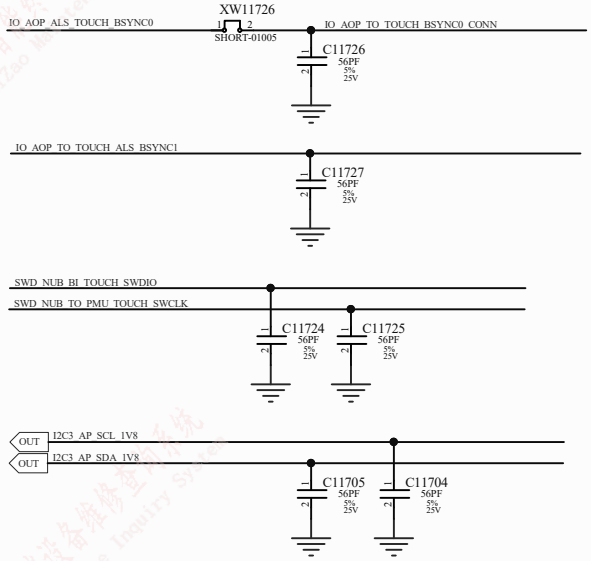

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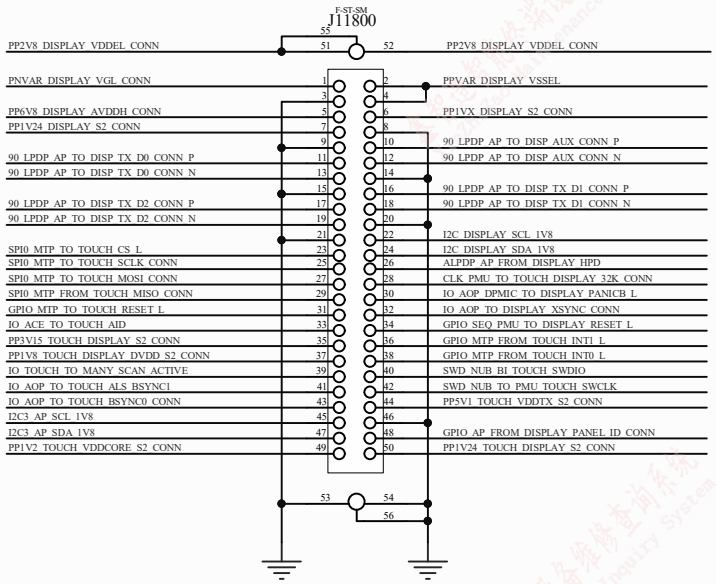

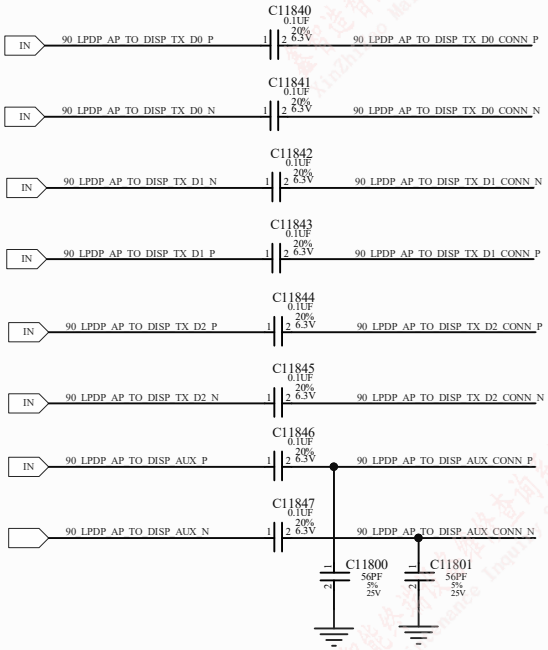

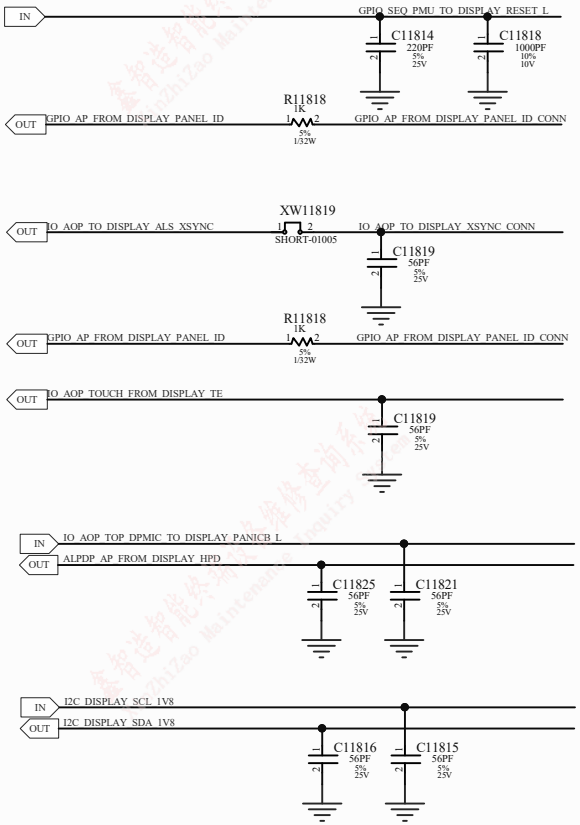

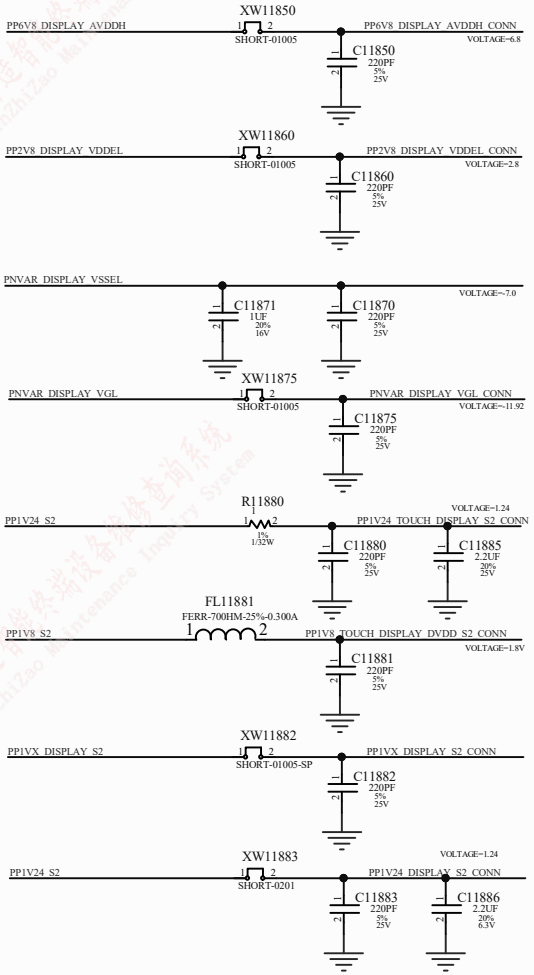

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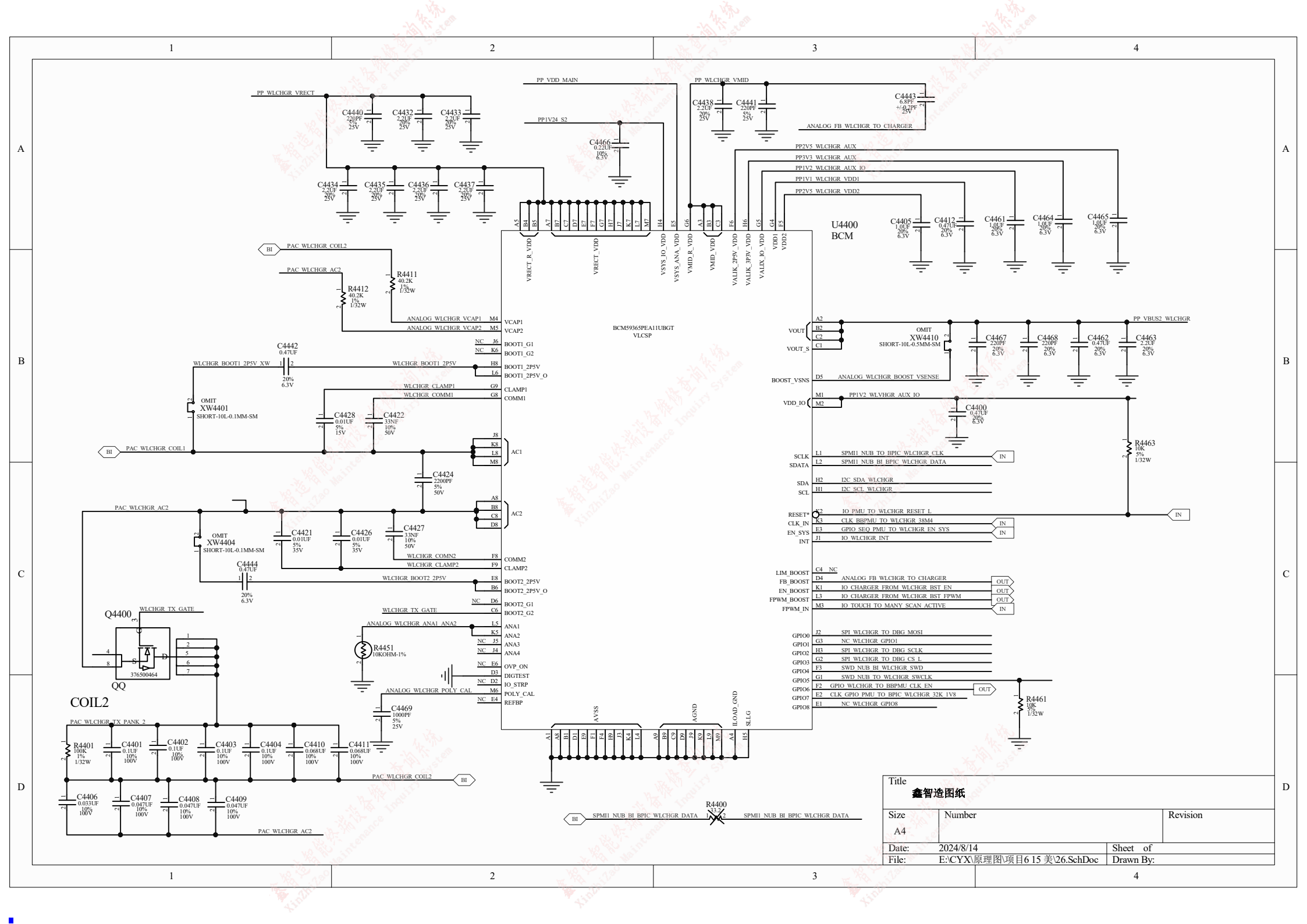
PP_WLCHGR_VRECT
PP_VDD_MAIN
PP_WLCHGR_VMID
PP1V24_S2
ANALOG_FB_WLCHGR_TO_CHARGER
PP2V5_WLCHGR_AUX
PP3V3_WLCHGR_AUX
PP1V2_WLCHGR_AUX_IO
PP1V1_WLCHGR_VDD1
PP2V5_WLCHGR_VDD2
U4400
BCM
BCM59365PEA11UBGT
VLCSP
PAC_WLCHGR_COIL2
PAC_WLCHGR_AC2
ANALOG_WLCHGR_VCAP1
ANALOG_WLCHGR_VCAP2
WLCHGR_BOOT1_2P5V_XW
WLCHGR_BOOT1_2P5V
WLCHGR_CLAMP1
WLCHGR_COMM1
PAC_WLCHGR_COIL1
WLCHGR_COMN2
WLCHGR_CLAMP2
WLCHGR_BOOT2_2P5V
WLCHGR_TX_GATE
ANALOG_WLCHGR_ANA1_ANA2
ANALOG_WLCHGR_POLY_CAL
Q4400
QQ
COIL2
PAC_WLCHGR_TX_PANK_2
PP_VBUS2_WLCHGR
BOOST_VSNS
ANALOG_WLCHGR_BOOST_VSENSE
VDD_IO
PP1V2_WLVHGR_AUX_IO
SCLK
SDATA
SPMI1_NUB_TO_BPIC_WLCHGR_CLK
SPMI1_NUB_BI_BPIC_WLCHGR_DATA
SDA
SCL
I2C_SDA_WLCHGR
I2C_SCL_WLCHGR
RESET*
CLK_IN
EN_SYS
INT
IO_PMU_TO_WLCHGR_RESET_L
CLK_BBPMU_TO_WLCHGR_38M4
GPIO_SEQ_PMU_TO_WLCHGR_EN_SYS
IO_WLCHGR_INT
LIM_BOOST
FB_BOOST
EN_BOOST
FPWM_BOOST
FPWM_IN
ANALOG_FB_WLCHGR_TO_CHARGER
IO_CHARGER_FROM_WLCHGR_BST_EN
IO_CHARGER_FROM_WLCHGR_BST_FPWM
IO_TOUCH_TO_MANY_SCAN_ACTIVE
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
SPI_WLCHGR_TO_DBG_MOSI
NC_WLCHGR_GPIO1
SPI_WLCHGR_TO_DBG_SCLK
SPI_WLCHGR_TO_DBG_CS_L
SWD_NUB_BI_WLCHGR_SWD
SWD_NUB_TO_WLCHGR_SWCLK
GPIO_WLCHGR_TO_BBPMU_CLK_EN
CLK_GPIO_PMU_TO_BPIC_WLCHGR_32K_1V8
NC_WLCHGR_GPIO8
OMIT
XW4401
SHORT-10L-0.1MM-SM
XW4404
SHORT-10L-0.1MM-SM
XW4410
SHORT-10L-0.5MM-SM
376500464
C4400
C4402
C4403
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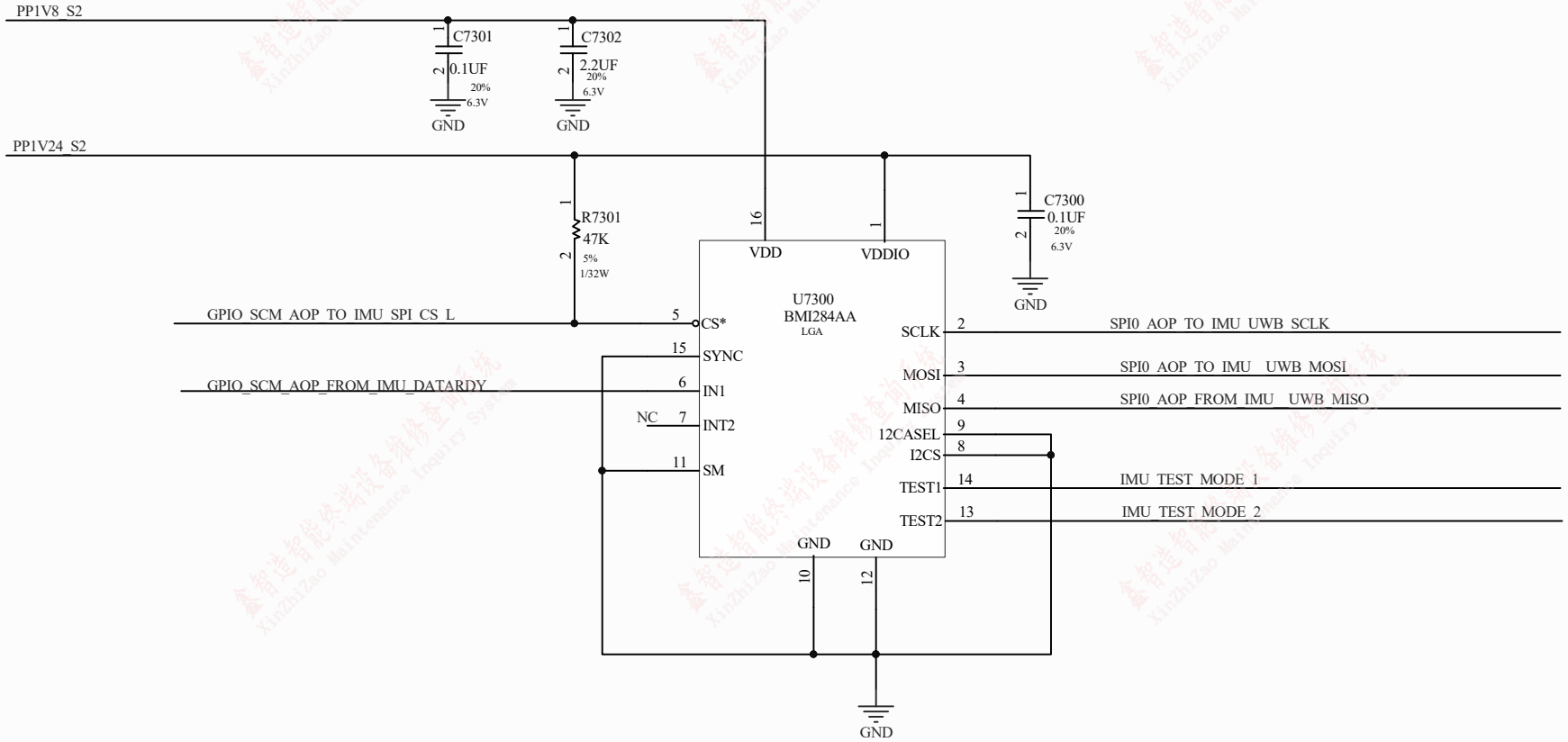

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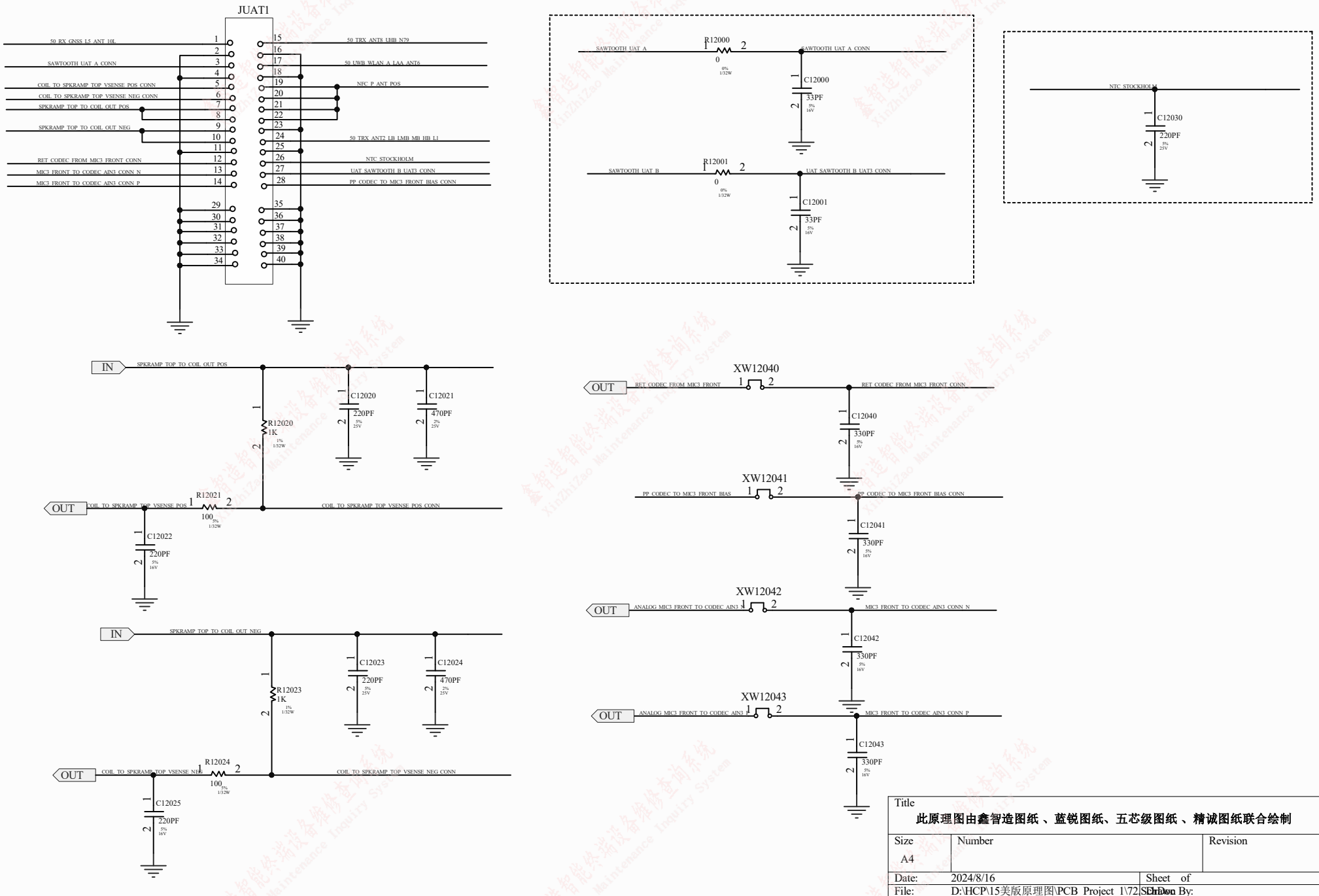

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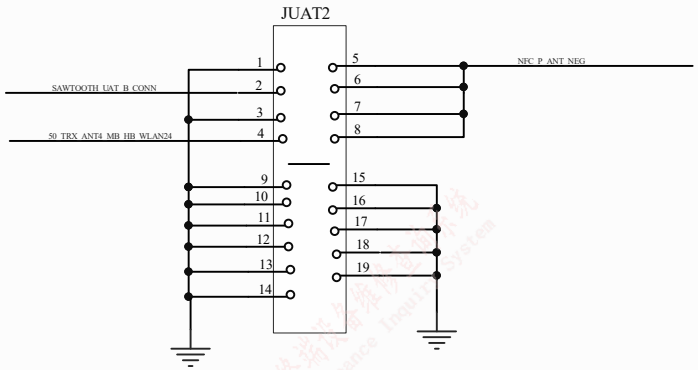
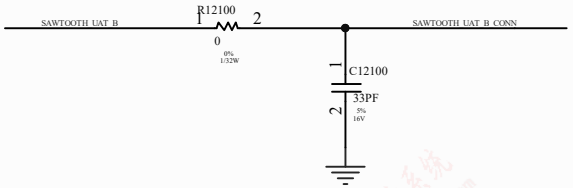


SUBUS FILTERS



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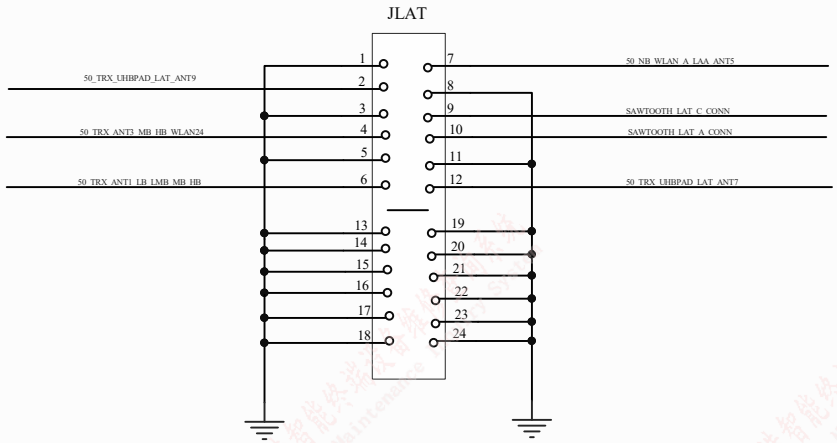

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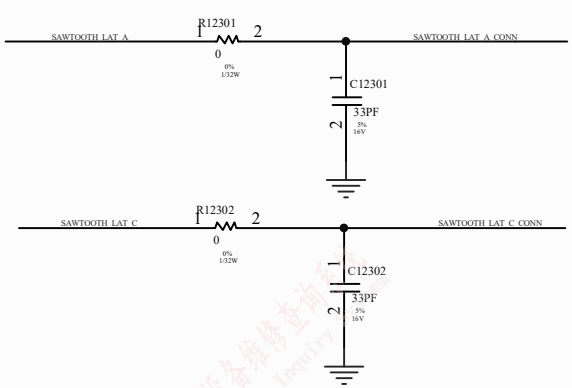

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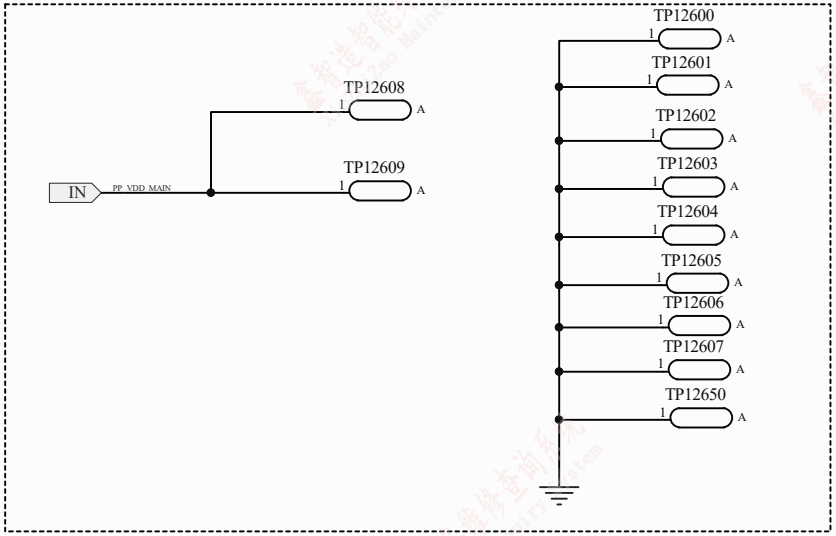
鑫智造智能终端设备维修查询系统 Xinzhizao Maintenance Inquiry System

Power +GND



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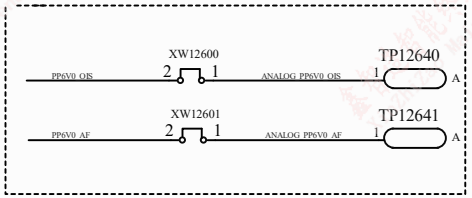

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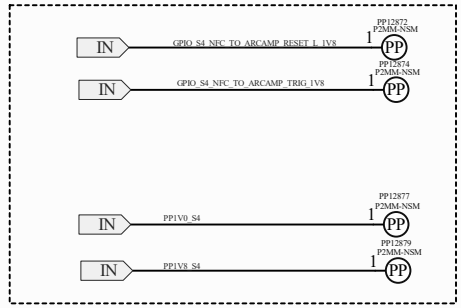

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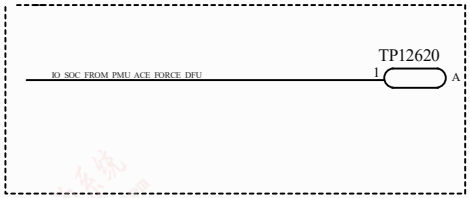
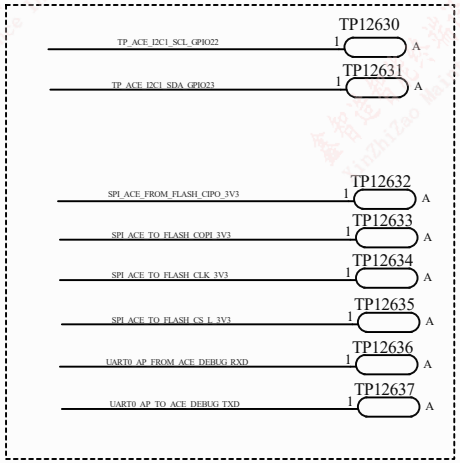


E85



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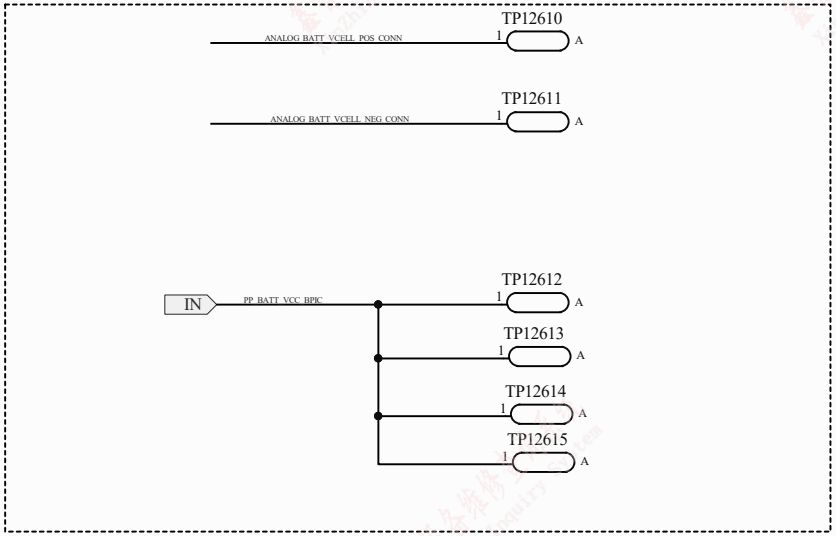

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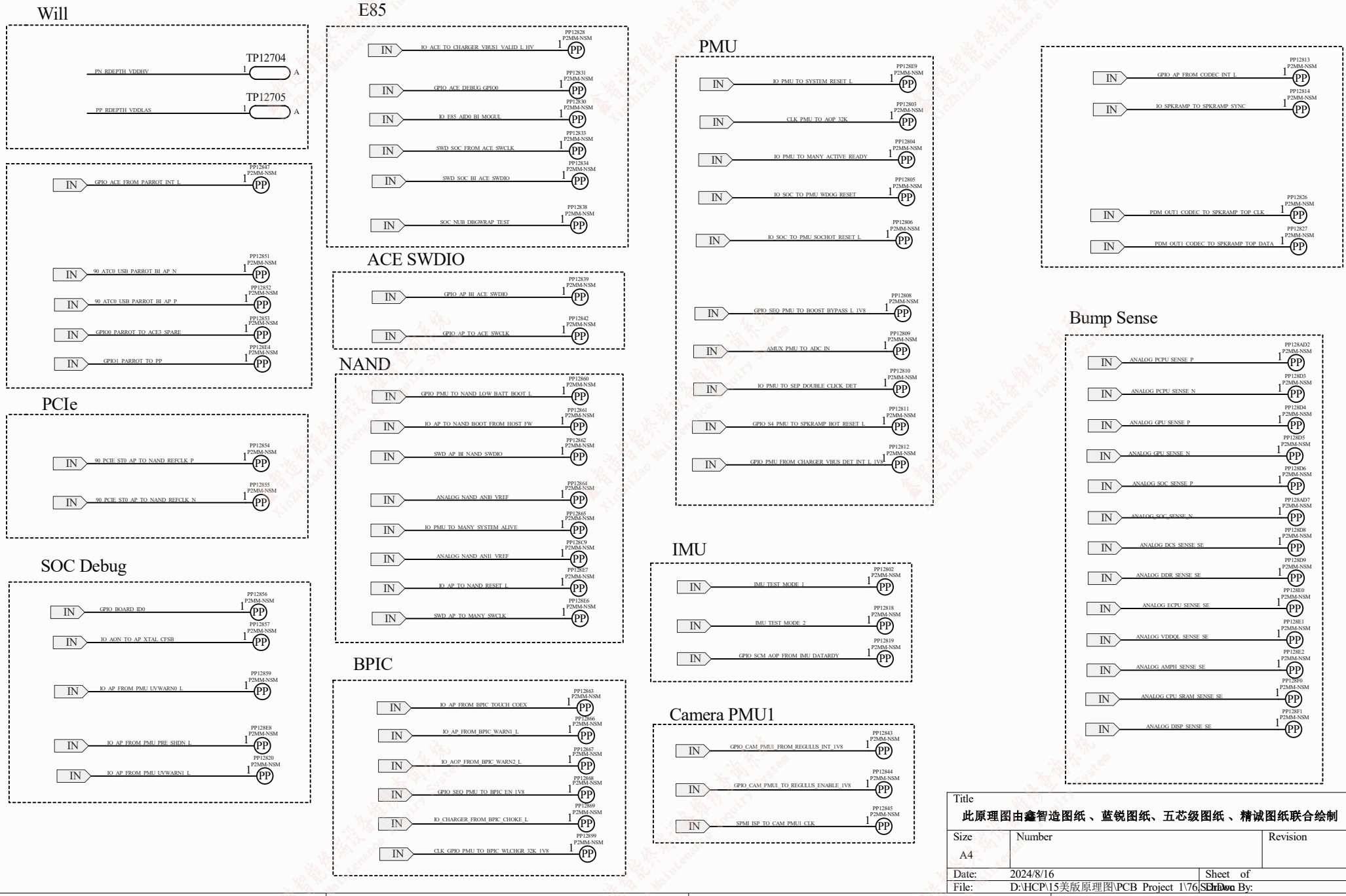
鑫智造智能终端设备维修查询系统 Xinzhizao Maintenance Inquiry System


Will
TP12704
PN_RDEPTH_VDDHV
TP12705
PP_RDEPTH_VDDLAS
GPIO_ACE_FROM_PARROT_INT_L
90_ATC0_USB_PARROT_BI_AP_N
90_ATC0_USB_PARROT_BI_AP_P
GPIO0_PARROT_TO_ACE3_SPARE
GPIO1_PARROT_TO_PP
PCIe
90_PCIE_ST0_AP_TO_NAND_REFCLK_P
90_PCIE_ST0_AP_TO_NAND_REFCLK_N
SOC Debug
GPIO_BOARD_ID0
IO_AON_TO_AP_XTAL_CFSB
IO_AP_FROM_PMU_UVWARN0_L
IO_AP_FROM_PMU_PRE_SHDN_L
IO_AP_FROM_PMU_UVWARN1_L
E85
IO_ACE_TO_CHARGER_VBUS1_VALID_L_HV
GPIO_ACE_DEBUG_GPIO0
IO_E85_AID0_BI_MOGUL
SWD_SOC_FROM_ACE_SWCLK
SWD_SOC_BI_ACE_SWDIO
SOC_NUB_DBGWRAP_TEST
ACE SWDIO
GPIO_AP_BI_ACE_SWDIO
GPIO_AP_TO_ACE_SWCLK
NAND
GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L
IO_AP_TO_NAND_BOOT_FROM_HOST_FW
SWD_AP_BI_NAND_SWDIO
ANALOG_NAND_AN0_VREF
IO_PMU_TO_MANY_SYSTEM_ALIVE
ANALOG_NAND_AN1_VREF
IO_AP_TO_NAND_RESET_L
SWD_AP_TO_MANY_SWCLK
BPIC
IO_AP_FROM_BPIC_TOUCH_COEX
IO_AP_FROM_BPIC_WARN1_L
IO_AOP_FROM_BPIC_WARN2_L
GPIO_SEQ_PMU_TO_BPIC_EN_1V8
IO_CHARGER_FROM_BPIC_CHOKE_L
CLK_GPIO_PMU_TO_BPIC_WLCHGR_32K_1V8
PMU
IO_PMU_TO_SYSTEM_RESET_L
CLK_PMU_TO_AOP_32K
IO_PMU_TO_MANY_ACTIVE_READY
IO_SOC_TO_PMU_WDOG_RESET
IO_SOC_TO_PMU_SOCHOT_RESET_L
GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8
AMUX_PMU_TO_ADC_IN
IO_PMU_TO_SEP_DOUBLE_CLICK_DET
GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L
GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8
IMU
IMU_TEST_MODE_1
IMU_TEST_MODE_2
GPIO_SCM_AOP_FROM_IMU_DATARDY
Camera PMU1
GPIO_CAM_PMU1_FROM_REGULUS_INT_1V8
GPIO_CAM_PMU1_TO_REGULUS_ENABLE_1V8
SPMI_ISP_TO_CAM_PMU1_CLK
GPIO_AP_FROM_CODEC_INT_L
IO_SPKRAMP_TO_SPKRAMP_SYNC
PDM_OUT1_CODEC_TO_SPKRAMP_TOP_CLK
PDM_OUT1_CODEC_TO_SPKRAMP_TOP_DATA
Bump Sense
ANALOG_PCPU_SENSE_P
ANALOG_PCPU_SENSE_N
ANALOG_GPU_SENSE_P
ANALOG_GPU_SENSE_N
ANALOG_SOC_SENSE_P
ANALOG_SOC_SENSE_N
ANALOG_DCS_SENSE_SE
ANALOG_DDR_SENSE_SE
ANALOG_ECPU_SENSE_SE
ANALOG_VDDQL_SENSE_SE
ANALOG_AMPH_SENSE_SE
ANALOG_CPU_SRAM_SENSE_SE
ANALOG_DISP_SENSE_SE
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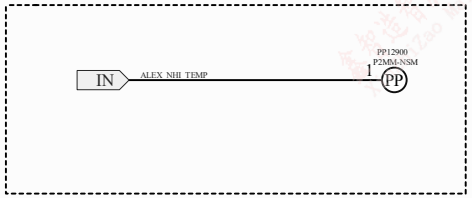

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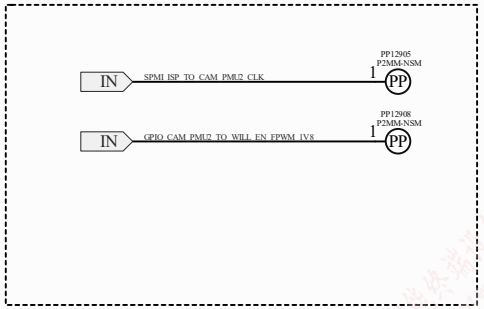

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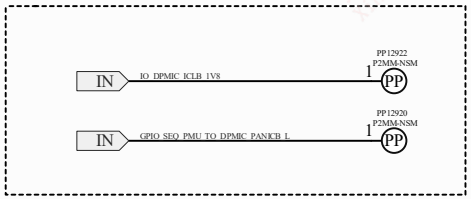

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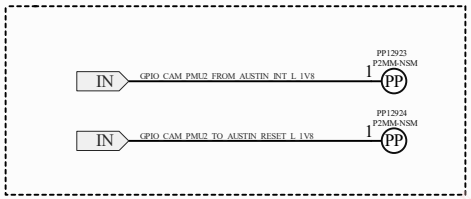

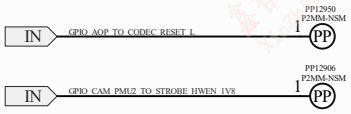

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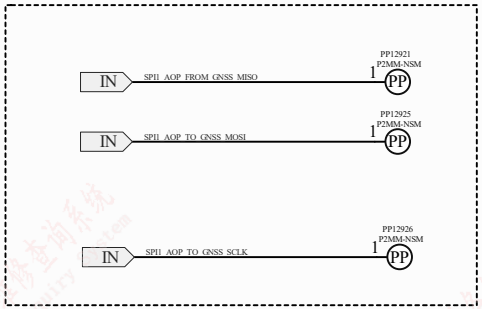

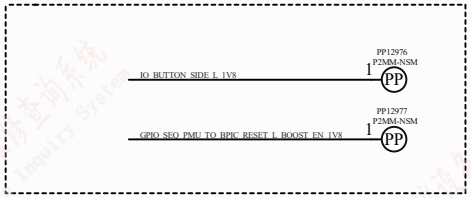

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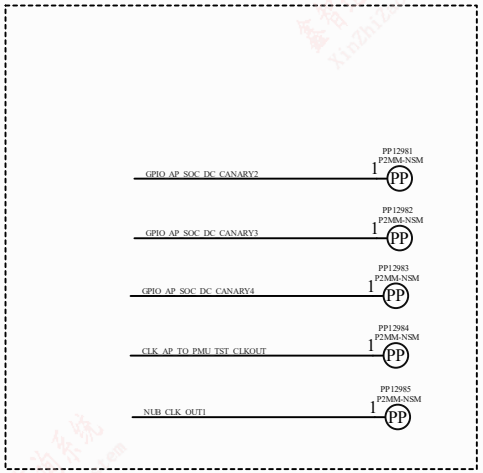

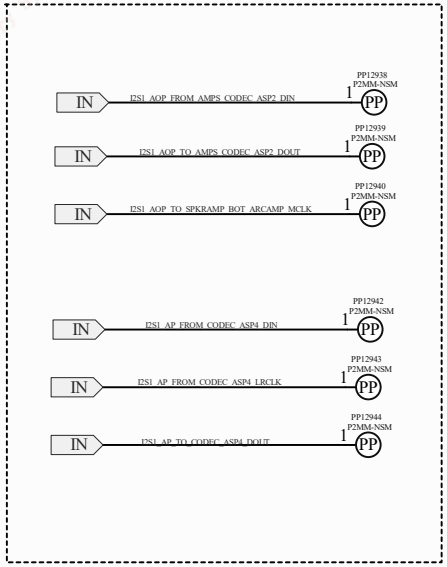

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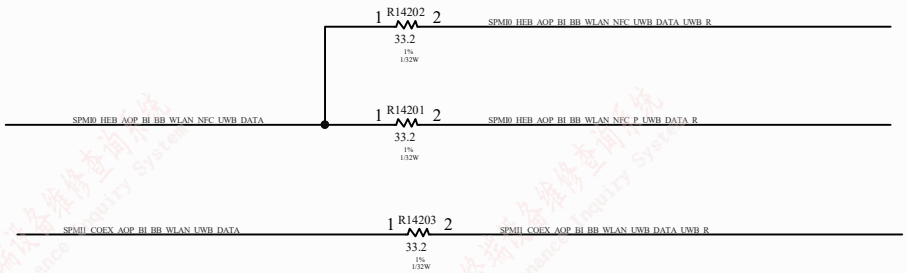
鑫智造智能终端设备维修查询系统 Xinzhizao Maintenance Inquiry System



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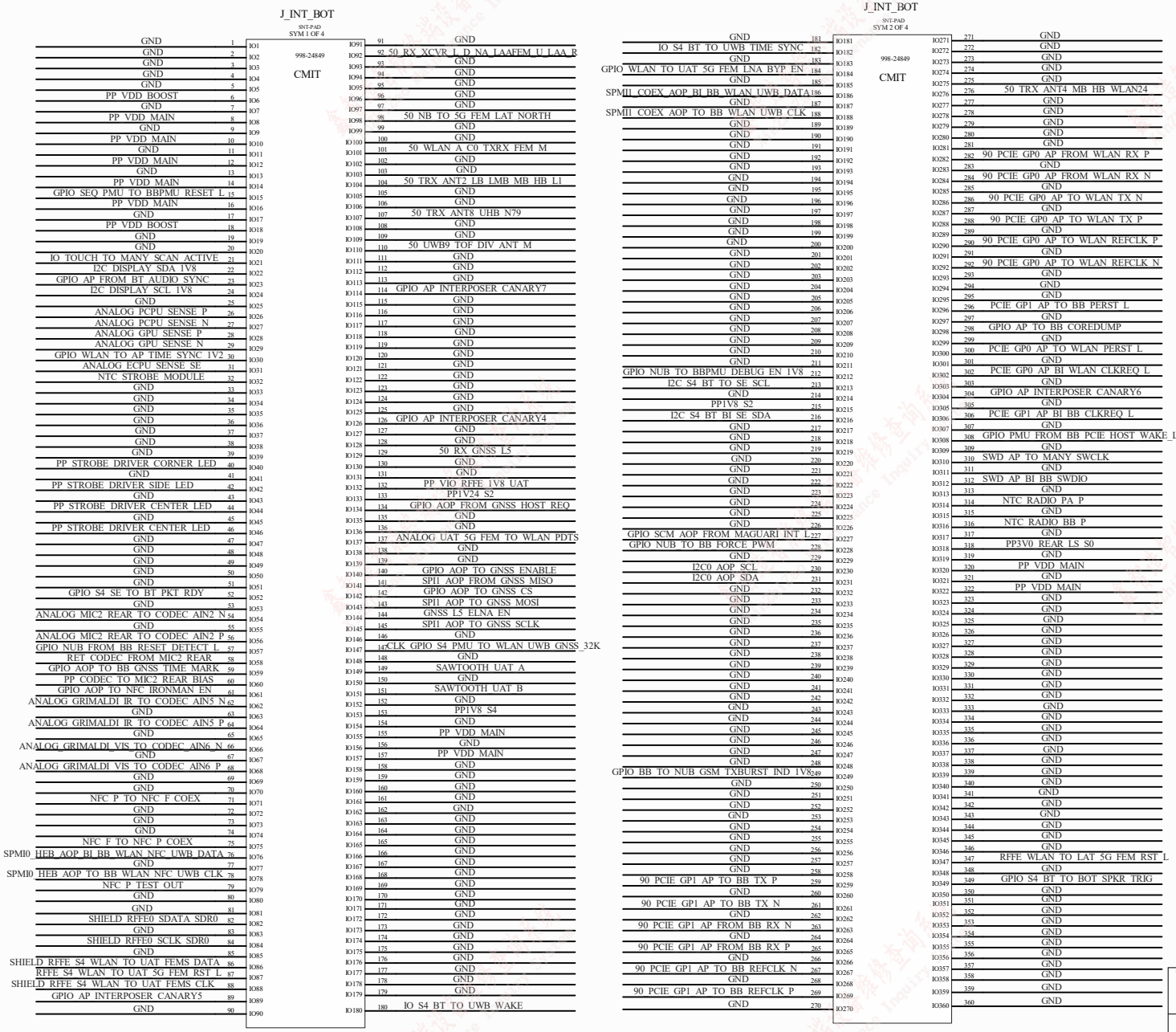

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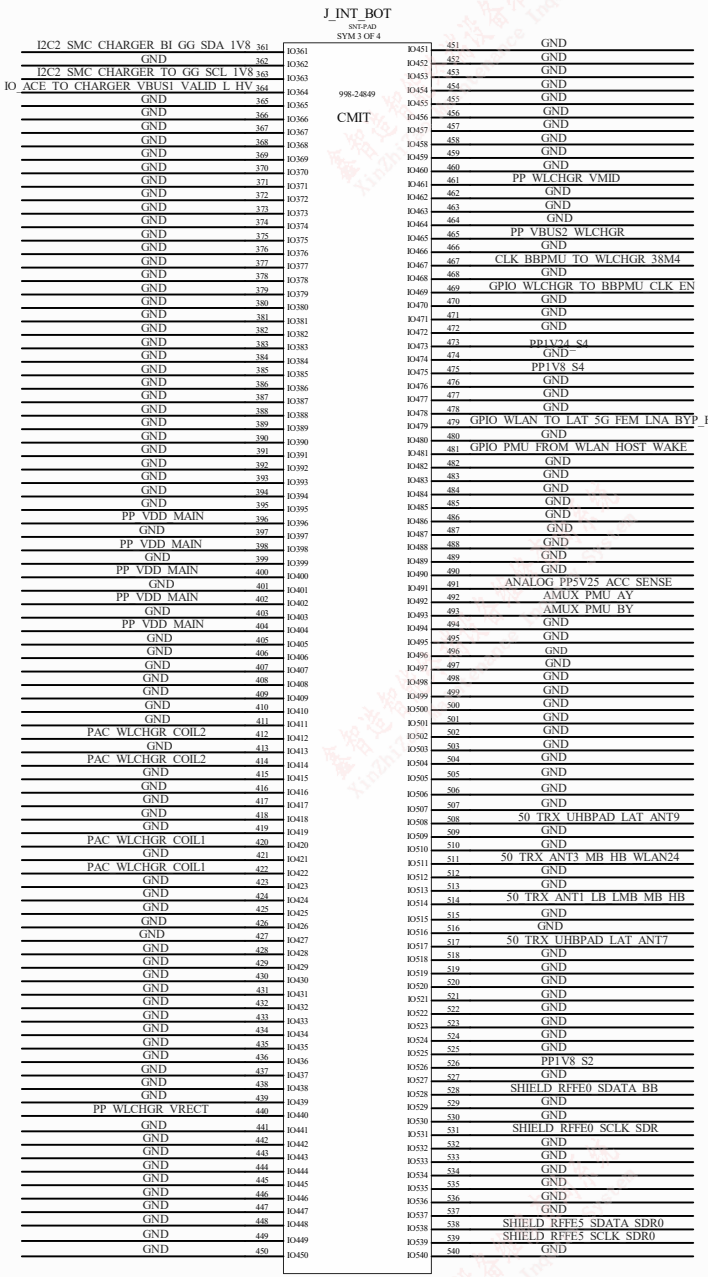

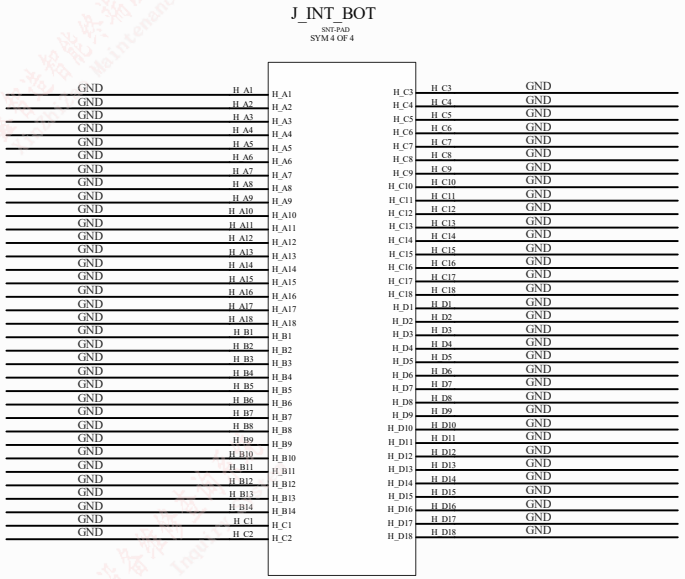

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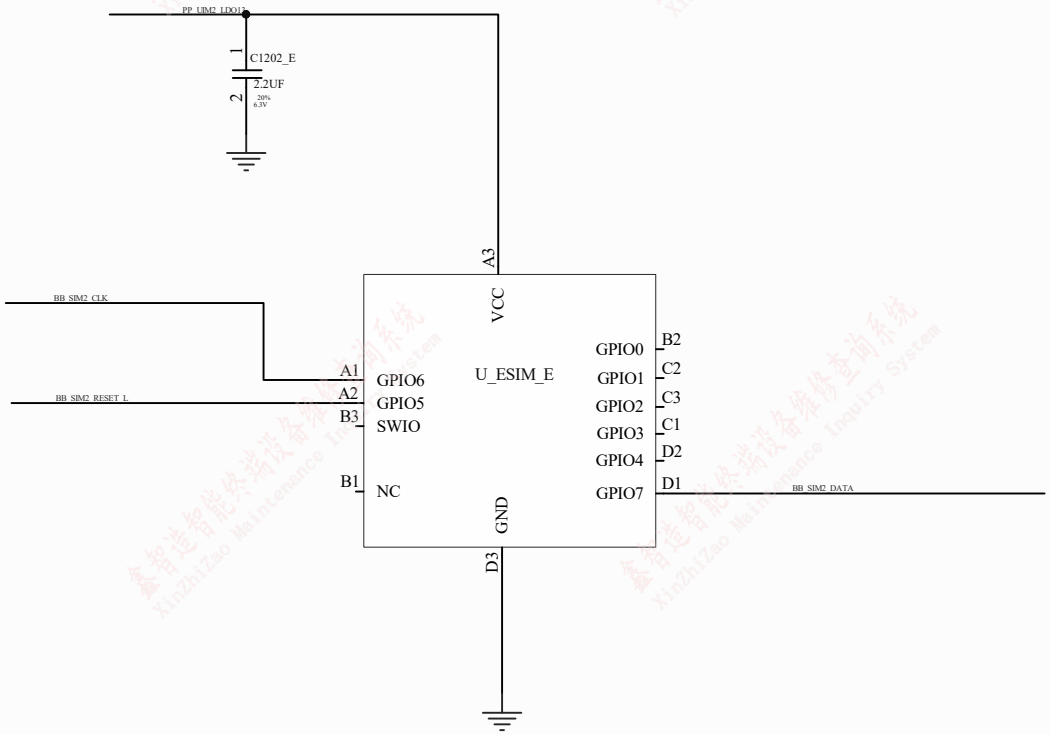

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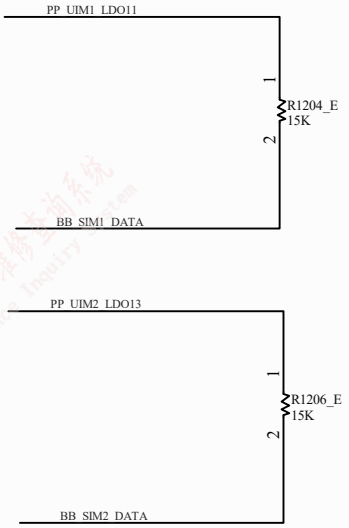
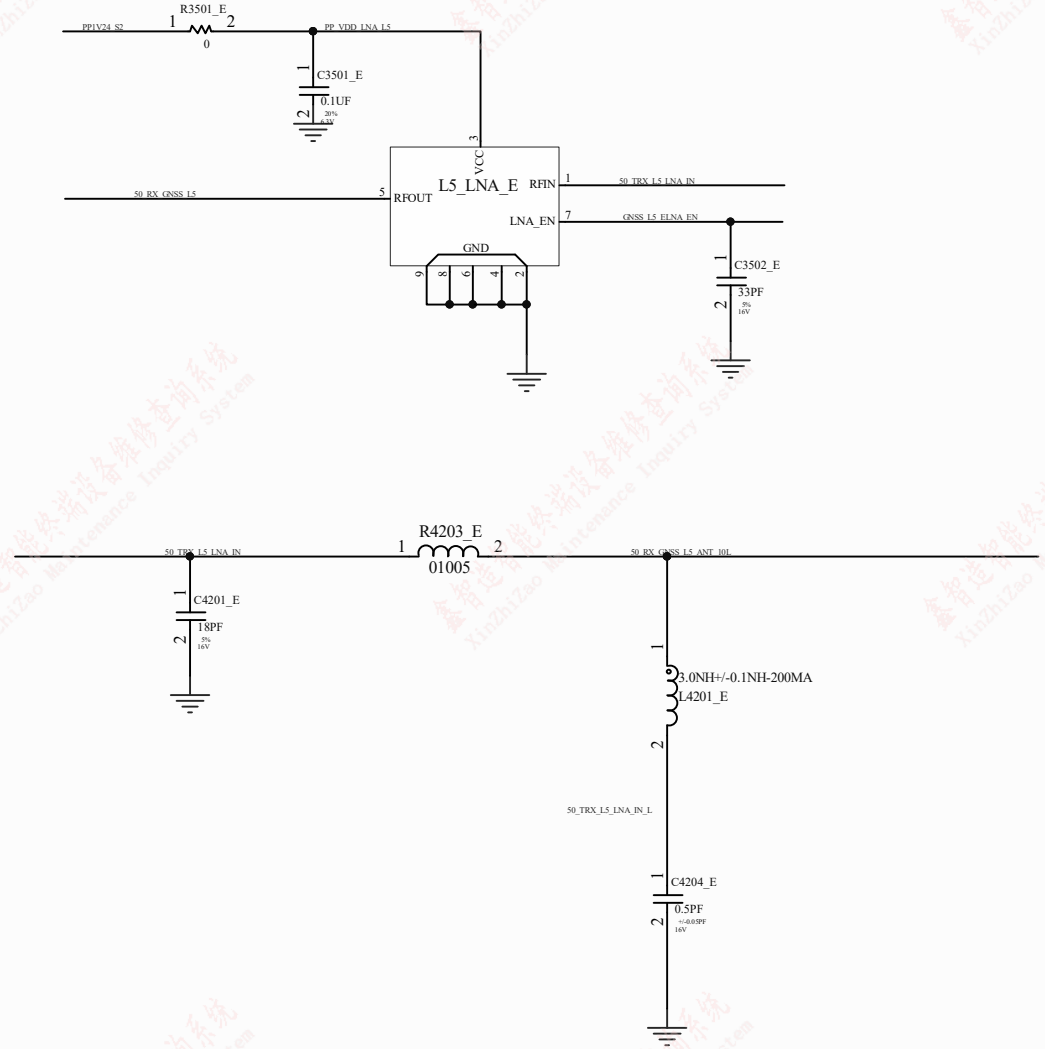


Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\81.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
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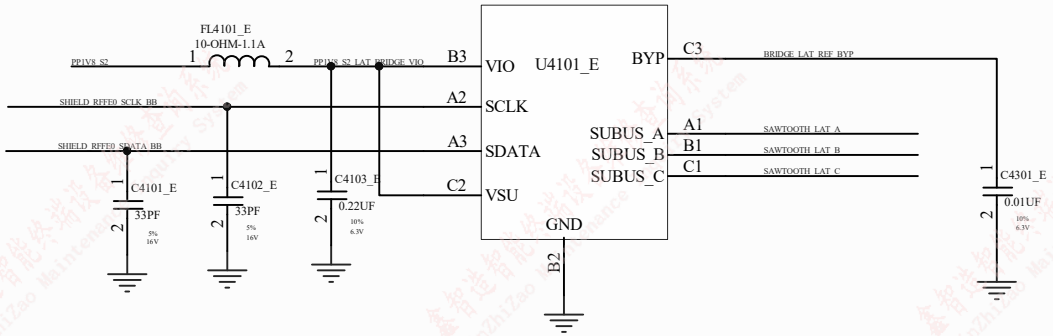

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Size A4	Number	Revision
Date: 2024/8/16		Sheet of
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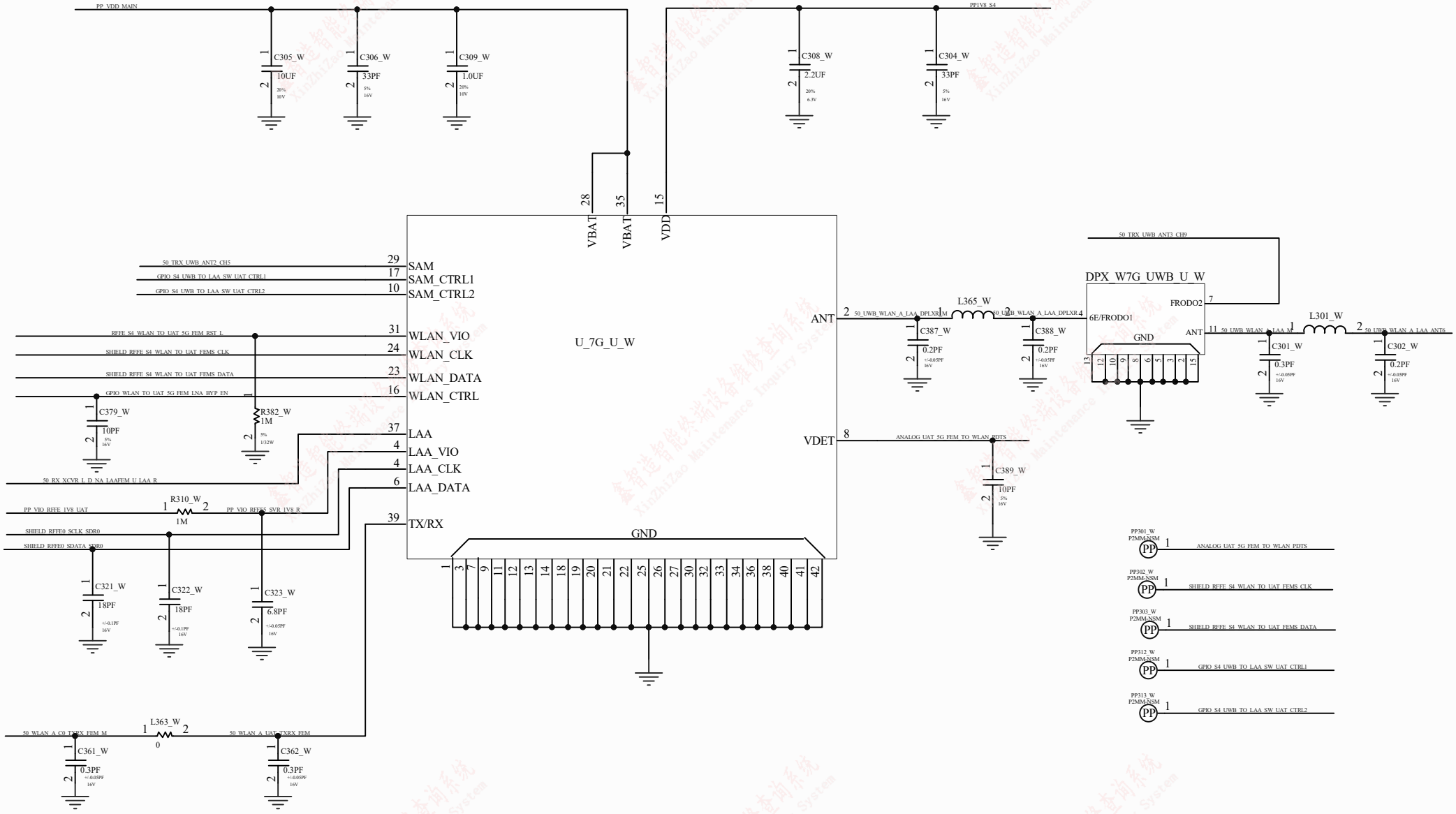

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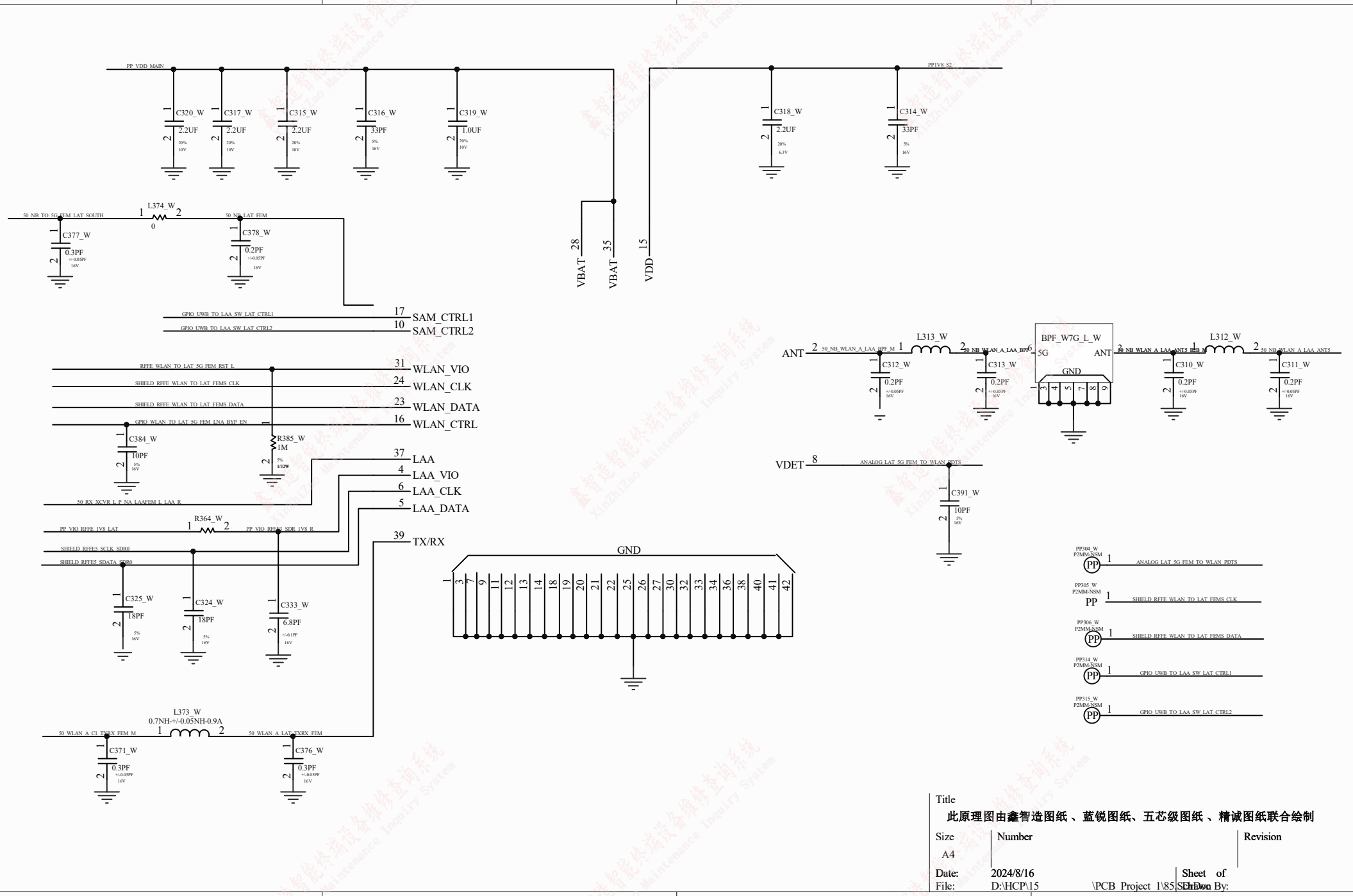
Size	Number	Revision
A4		

Date: 2024/8/16 Sheet of

File: D:\HCP\15美版原理图\PCB Project 1\84.SchDoc Drawn By:



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Size	Number	Revision
A4		

Date: 2024/8/16 Sheet of

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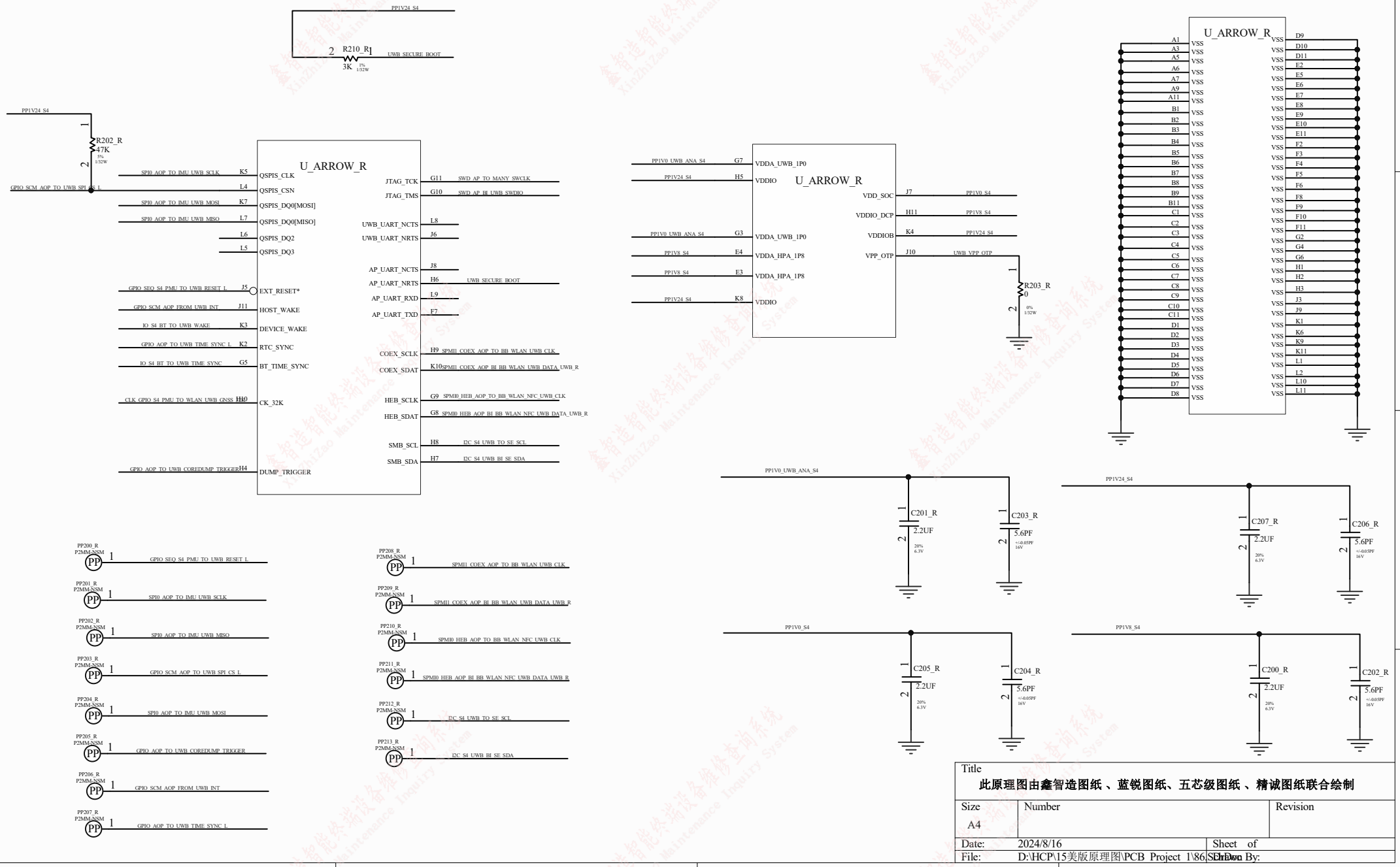
PP1V24_S4
R210_R
3K
UWB_SECURE_BOOT
R202_R
47K
U_ARROW_R
SPI0_AOP_TO_IMU_UWB_SCLK
GPIO_SCM_AOP_TO_UWB_SPI_CS_L
SPI0_AOP_TO_IMU_UWB_MOSI
SPI0_AOP_TO_IMU_UWB_MISO
QSPIS_CLK
QSPIS_CSN
QSPIS_DQ0[MOSI]
QSPIS_DQ0[MISO]
QSPIS_DQ2
QSPIS_DQ3
GPIO_SEQ_S4_PMU_TO_UWB_RESET_L
GPIO_SCM_AOP_FROM_UWB_INT
IO_S4_BT_TO_UWB_WAKE
GPIO_AOP_TO_UWB_TIME_SYNC_L
IO_S4_BT_TO_UWB_TIME_SYNC
CLK_GPIO_S4_PMU_TO_WLAN_UWB_GNSS
GPIO_AOP_TO_UWB_COREDUMP_TRIGGER
EXT_RESET*
HOST_WAKE
DEVICE_WAKE
RTC_SYNC
BT_TIME_SYNC
CK_32K
DUMP_TRIGGER
JTAG_TCK
JTAG_TMS
UWB_UART_NCTS
UWB_UART_NRTS
AP_UART_NCTS
AP_UART_NRTS
AP_UART_RXD
AP_UART_TXD
SWD_AP_TO_MANY_SWCLK
SWD_AP_BI_UWB_SWDIO
UWB_SECURE_BOOT
COEX_SCLK
COEX_SDAT
HEB_SCLK
HEB_SDAT
SMB_SCL
SMB_SDA
I2C_S4_UWB_TO_SE_SCL
I2C_S4_UWB_BI_SE_SDA
SPMI1_COEX_AOP_TO_BB_WLAN_UWB_CLK
SPMI1_COEX_AOP_BI_BB_WLAN_UWB_DATA_UWB_R
SPMI0_HEB_AOP_TO_BB_WLAN_NFC_UWB_CLK
SPMI0_HEB_AOP_BI_BB_WLAN_NFC_UWB_DATA_UWB_R
PP200_R
PP201_R
PP202_R
PP203_R
PP204_R
PP205_R
PP206_R
PP207_R
PP208_R
PP209_R
PP210_R
PP211_R
PP212_R
PP213_R
P2MM-NSM
PP1V0_UWB_ANA_S4
PP1V8_S4
VDDA_UWB_1P0
VDDIO
VDDA_HPA_1P8
VDD_SOC
VDDIO_DCP
VDDIOB
VPP_OTP
UWB_VPP_OTP
R203_R
0
C201_R
2.2UF
C203_R
5.6PF
C207_R
C206_R
C205_R
C204_R
C200_R
C202_R
VSS
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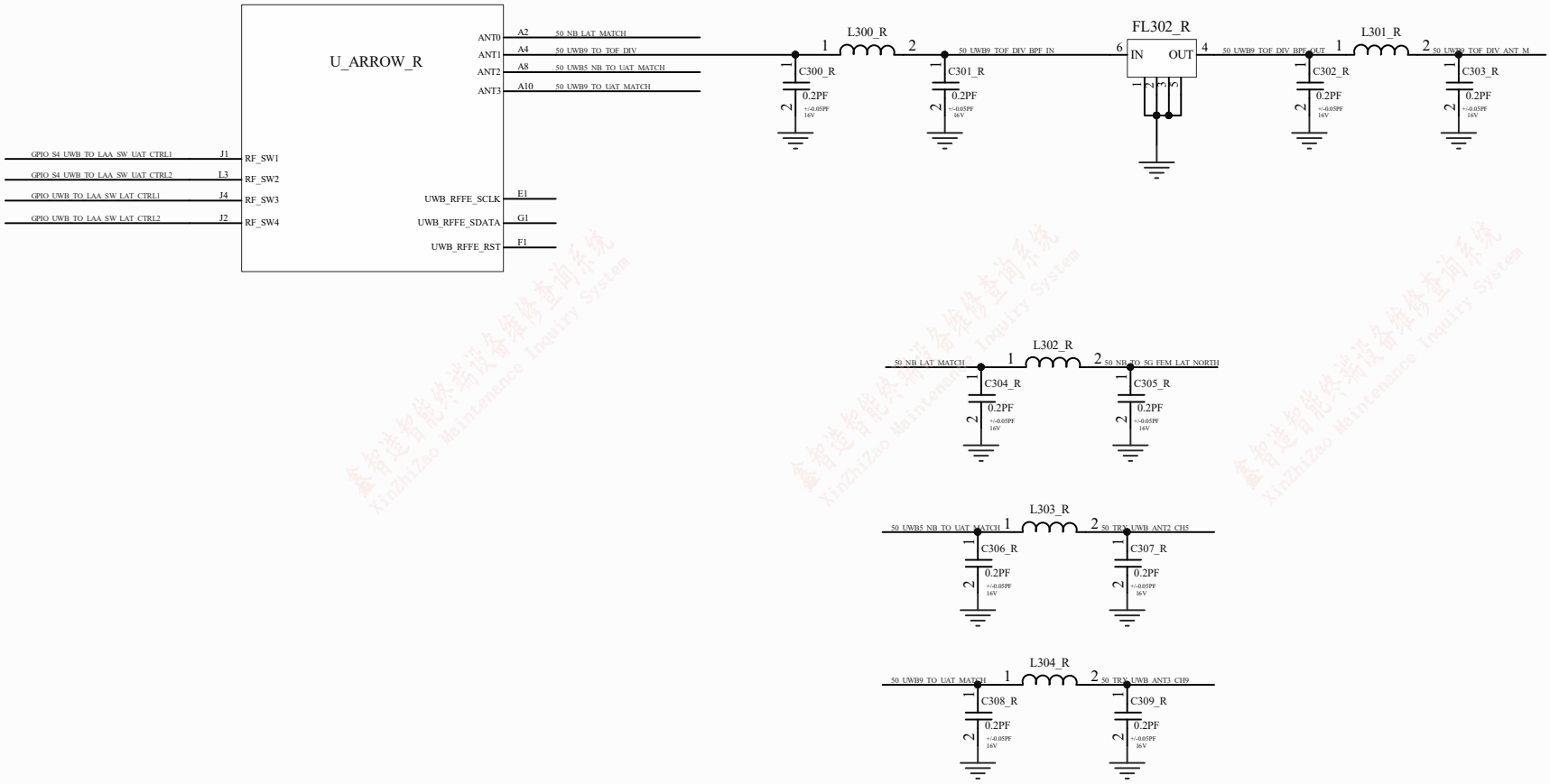

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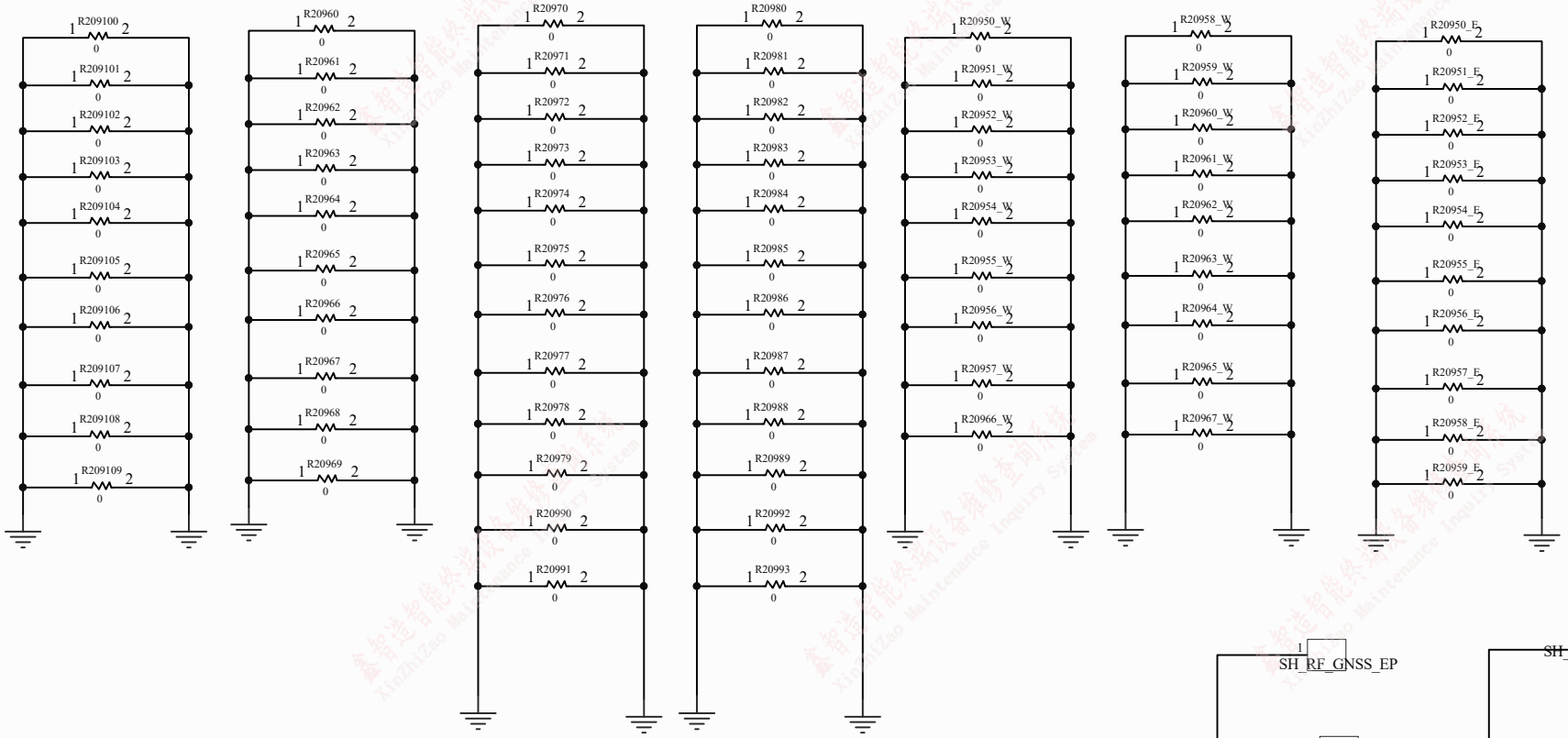
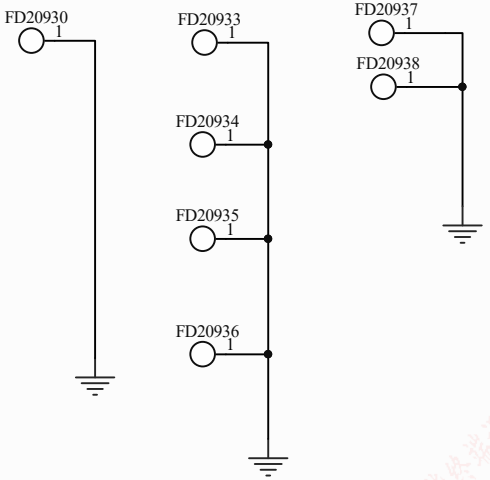
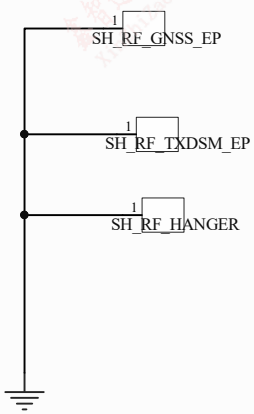
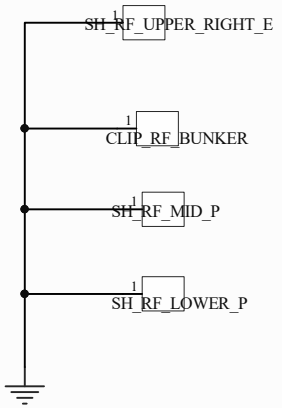
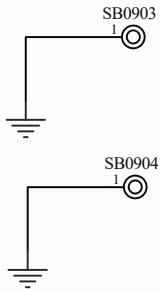
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\87	Drawn By:	











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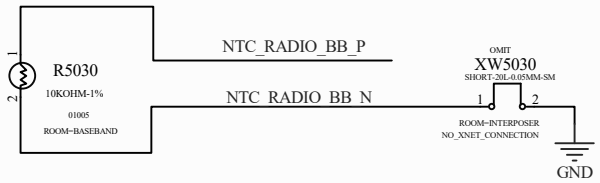
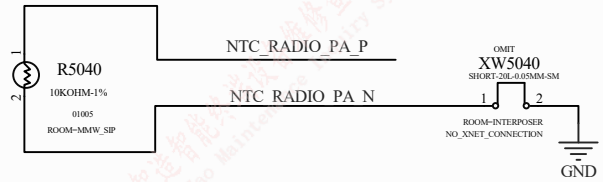
Size	Number	Revision
A4		
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\88.SchDoc	Drawn By:	

鑫智造智能终端设备维修查询系统 Xinzhizao Maintenance Inquiry System

Baseband/BB PMU NTC



Cassata/UAT PA NTC



Title: 此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制		
Size: A4	Number	Revision
Date: 2024/8/16		Sheet of
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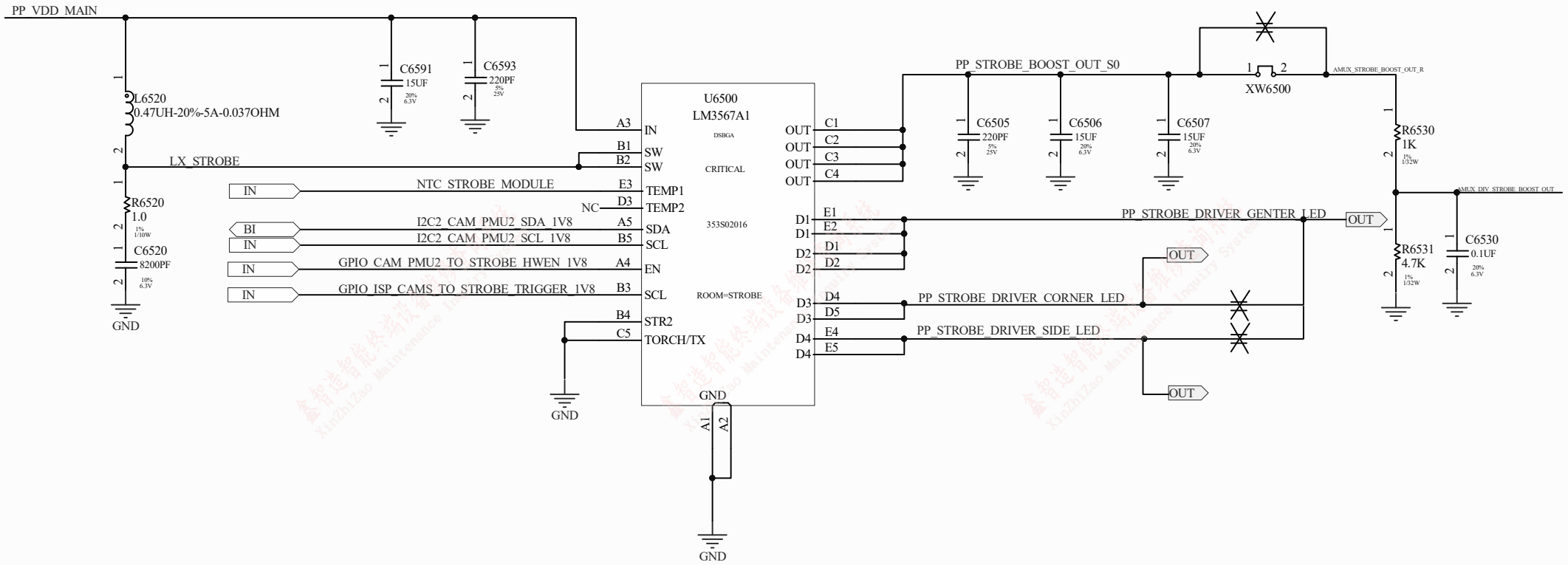

Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
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Date: 2024/8/16	Sheet of	
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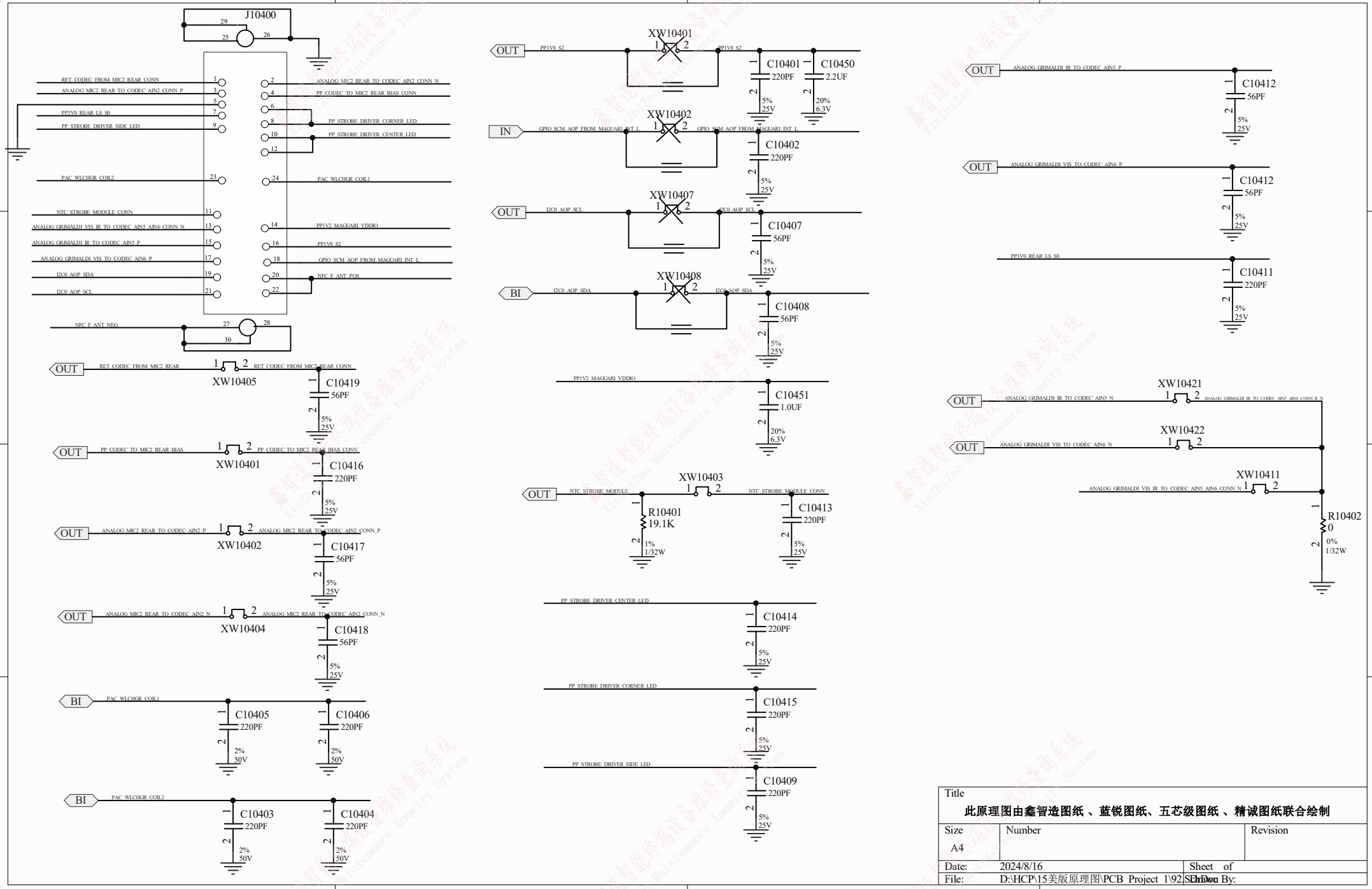

Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制
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Revision	
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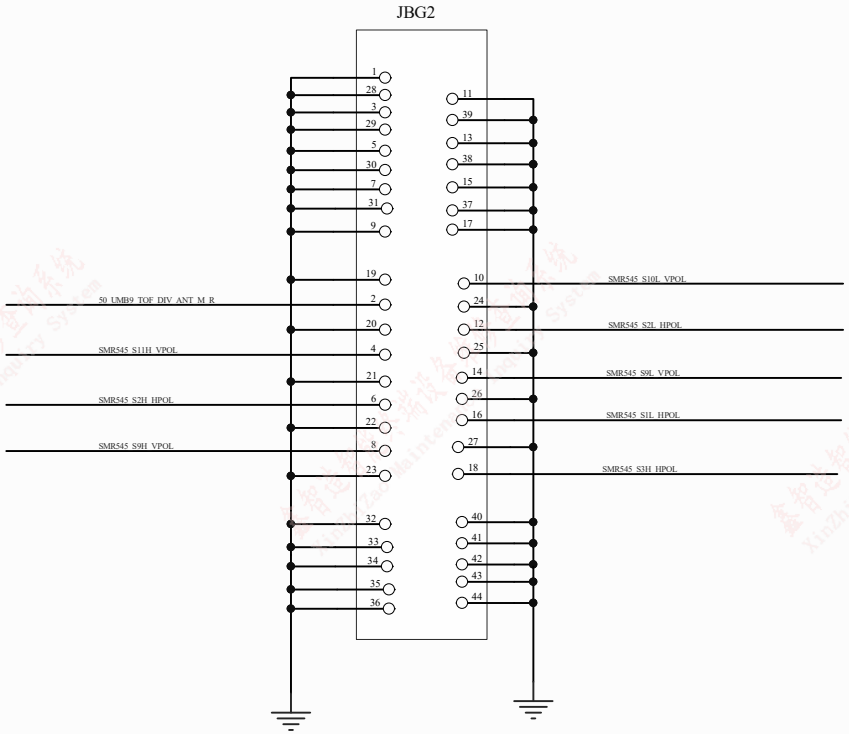

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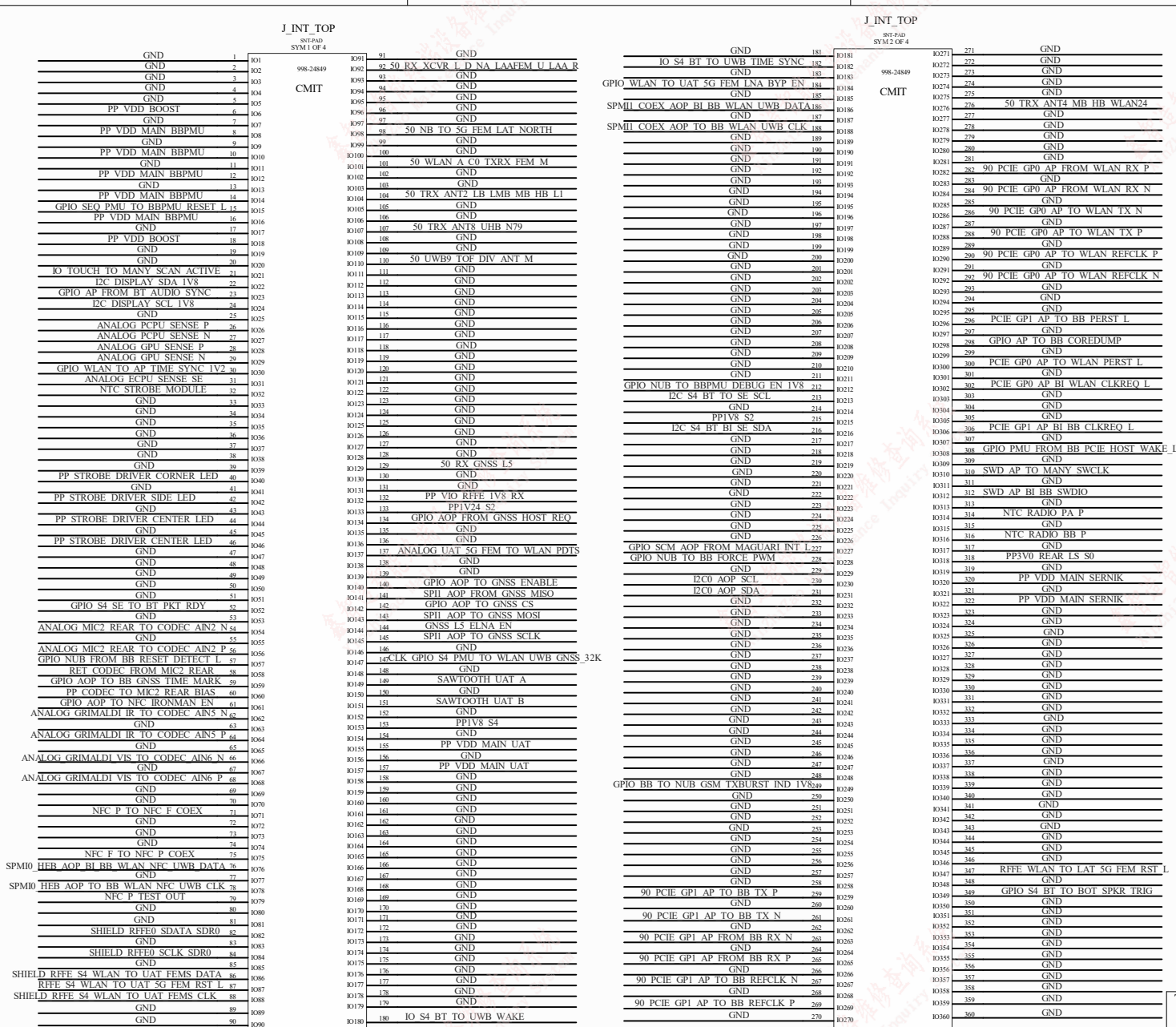

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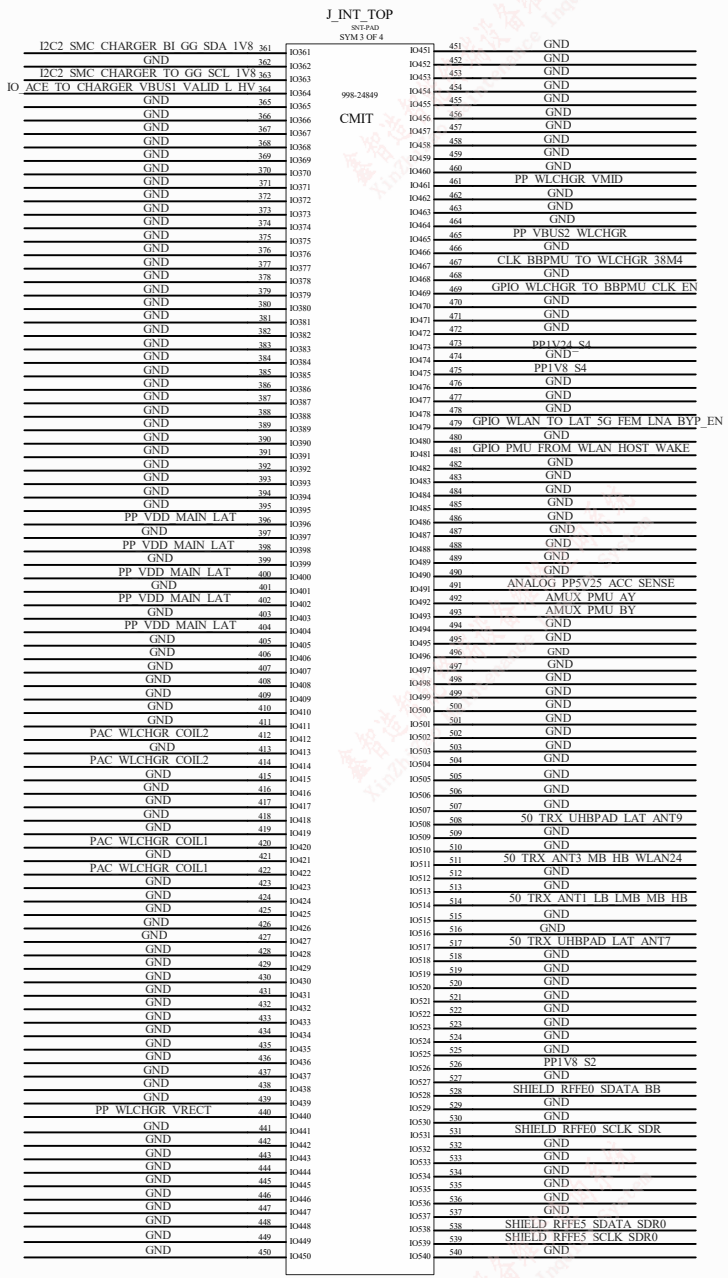

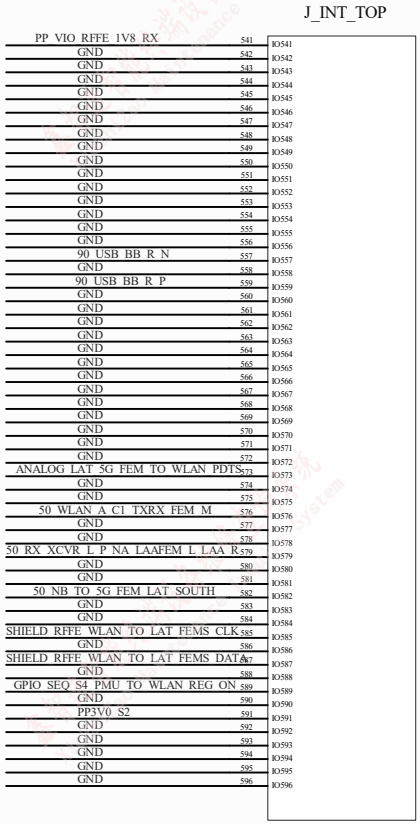

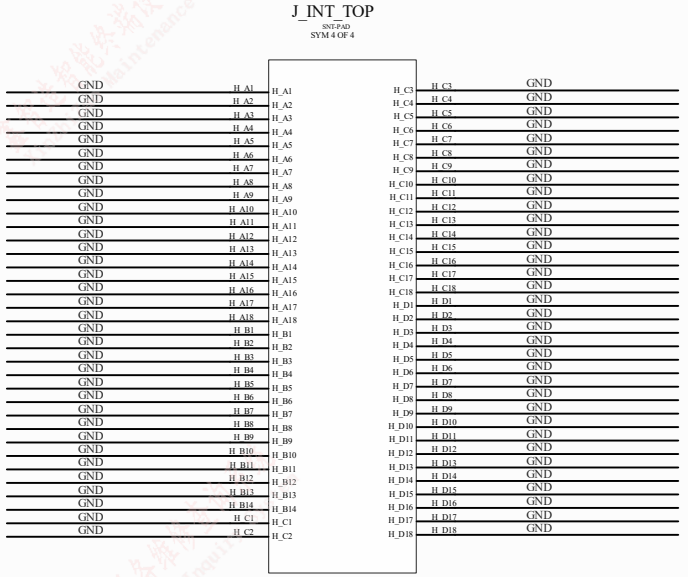

Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制		
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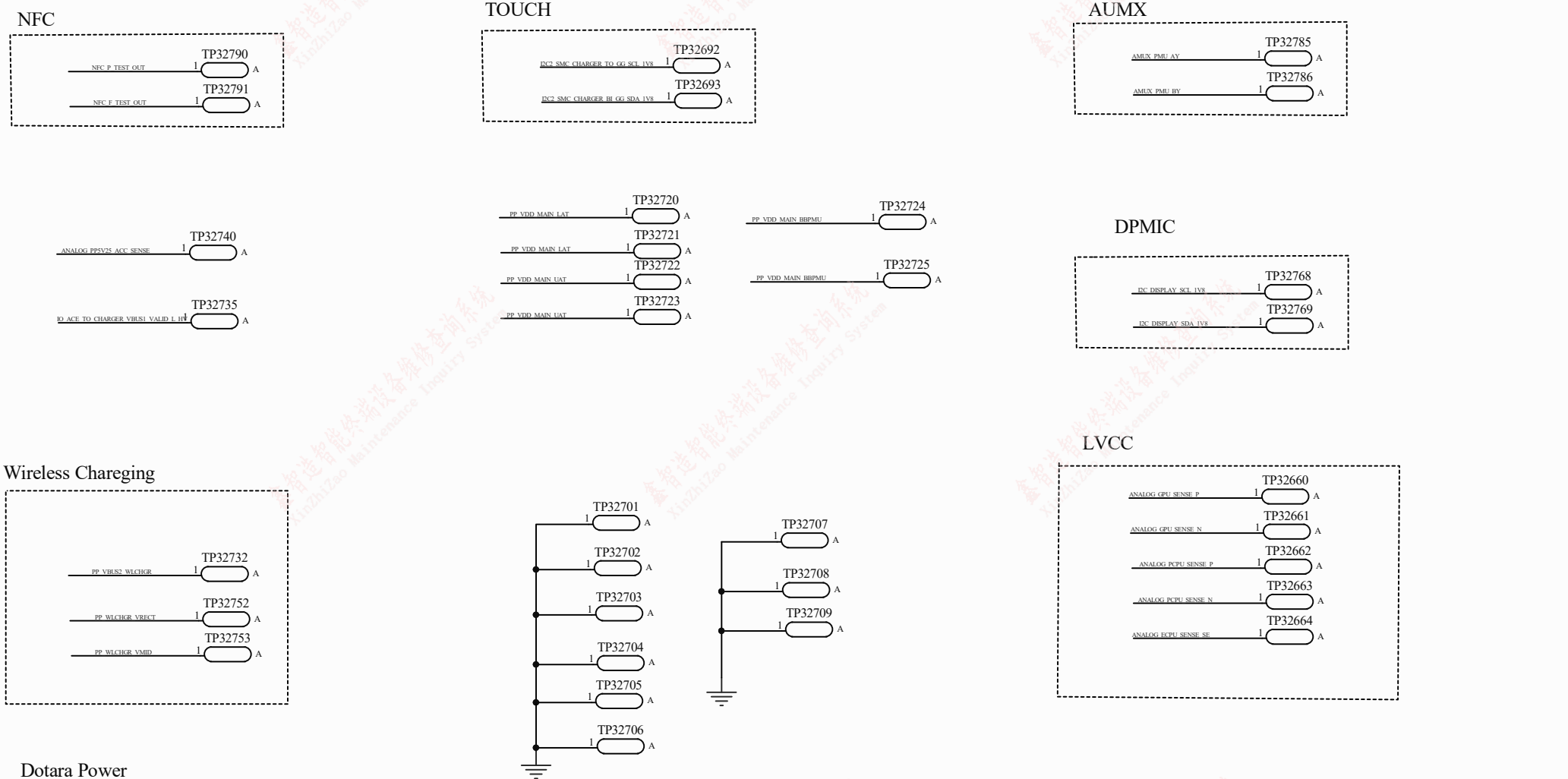

Title
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Size	Number	Revision
A4		

Date: 2024/8/16 Sheet of

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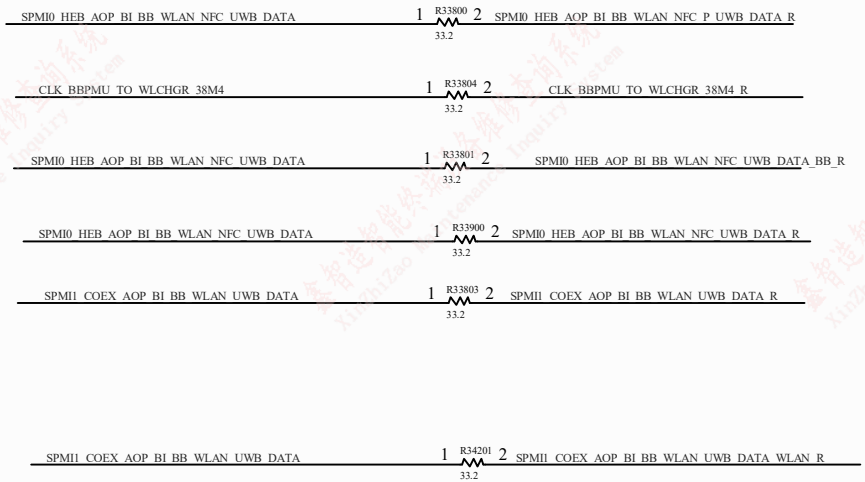

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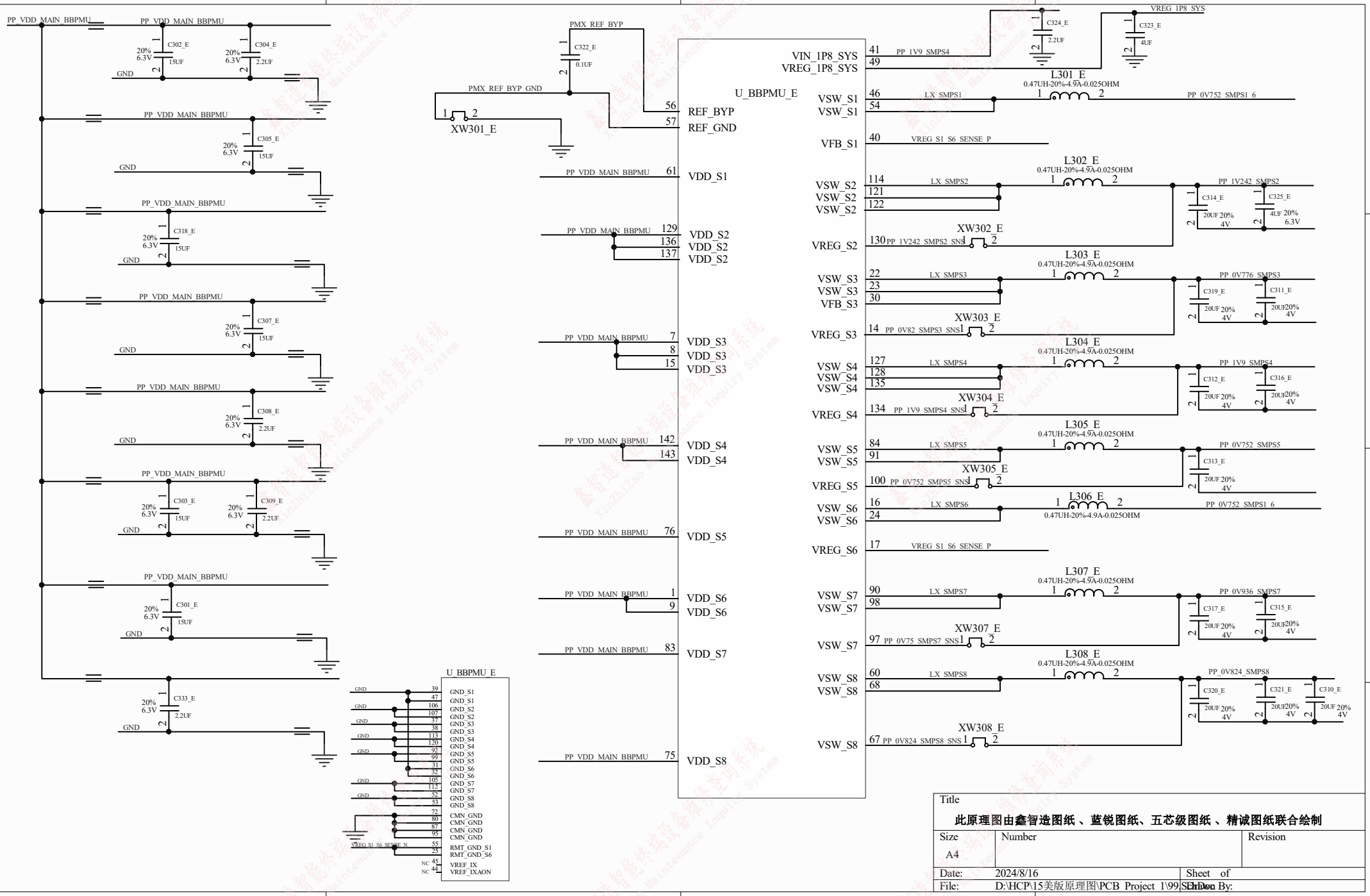
PP_VDD_MAIN_BBPMU
C302_E 20% 6.3V 15UF
C304_E 20% 6.3V 2.2UF
C305_E 20% 6.3V 15UF
C318_E 20% 6.3V 15UF
C307_E 20% 6.3V 15UF
C308_E 20% 6.3V 2.2UF
C303_E 20% 6.3V 15UF
C309_E 20% 6.3V 2.2UF
C301_E 20% 6.3V 15UF
C333_E 20% 6.3V 2.2UF
GND
PMX_REF_BYP
C322_E 0.1UF
PMX_REF_BYP_GND
XW301_E
U_BBPMU_E
REF_BYP
REF_GND
VDD_S1
VDD_S2
VDD_S3
VDD_S4
VDD_S5
VDD_S6
VDD_S7
VDD_S8
VIN_1P8_SYS
VREG_1P8_SYS
PP_1V9_SMPS4
C324_E 2.2UF
C323_E 4UF
VREG_1P8_SYS
L301_E 0.47UH-20%-4.9A-0.025OHM
LX_SMPS1
PP_0V752_SMPS1_6
VSW_S1
VFB_S1
VREG_S1_S6_SENSE_P
L302_E 0.47UH-20%-4.9A-0.025OHM
LX_SMPS2
PP_1V242_SMPS2
C314_E 20UF 20% 4V
C325_E 4UF 20% 6.3V
XW302_E
PP_1V242_SMPS2_SNS
VSW_S2
VREG_S2
L303_E 0.47UH-20%-4.9A-0.025OHM
LX_SMPS3
PP_0V776_SMPS3
C319_E 20UF 20% 4V
C311_E 20UF 20% 4V
XW303_E
PP_0V82_SMPS3_SNS
VSW_S3
VREG_S3
L304_E 0.47UH-20%-4.9A-0.025OHM
LX_SMPS4
PP_1V9_SMPS4
C312_E 20UF 20% 4V
C316_E 20UF 20% 4V
XW304_E
PP_1V9_SMPS4_SNS
VSW_S4
VREG_S4
L305_E 0.47UH-20%-4.9A-0.025OHM
LX_SMPS5
PP_0V752_SMPS5
C313_E 20UF 20% 4V
XW305_E
PP_0V752_SMPS5_SNS
VSW_S5
VREG_S5
L306_E 0.47UH-20%-4.9A-0.025OHM
LX_SMPS6
PP_0V752_SMPS1_6
VSW_S6
VREG_S6
VREG_S1_S6_SENSE_P
L307_E 0.47UH-20%-4.9A-0.025OHM
LX_SMPS7
PP_0V936_SMPS7
C317_E 20UF 20% 4V
C315_E 20UF 20% 4V
XW307_E
PP_0V75_SMPS7_SNS
VSW_S7
L308_E 0.47UH-20%-4.9A-0.025OHM
LX_SMPS8
PP_0V824_SMPS8
C320_E 20UF 20% 4V
C321_E 20UF 20% 4V
C310_E 20UF 20% 4V
XW308_E
PP_0V824_SMPS8_SNS
VSW_S8
U_BBPMU_E
GND_S1
GND_S2
GND_S3
GND_S4
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GND_S6
GND_S7
GND_S8
CMN_GND
RMT_GND_S1
RMT_GND_S6
VREF_IX
VREF_IXAON
VREG_S1_S6_SENSE_N
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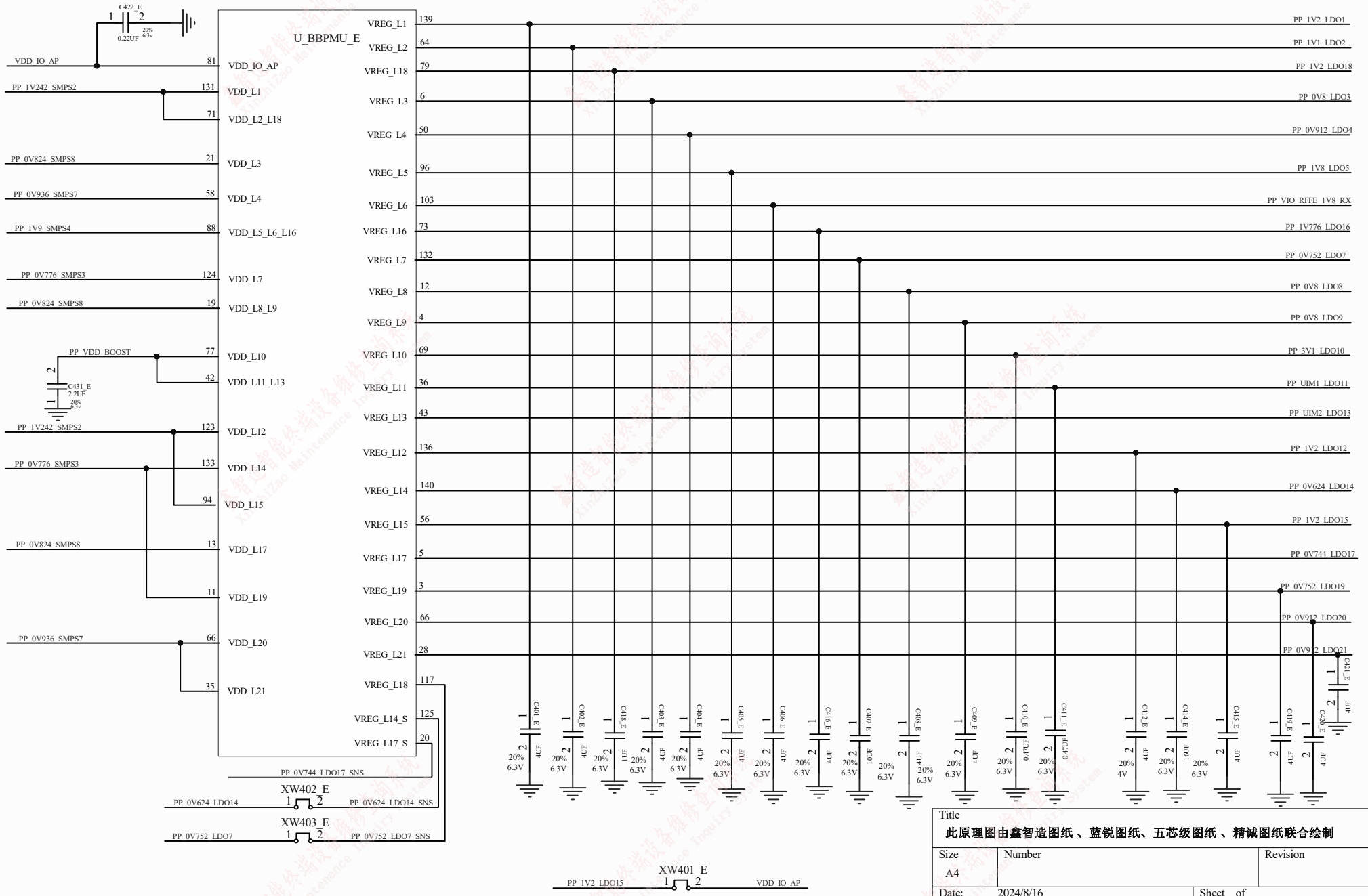
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PP_0V824_SMPS8
PP_0V936_SMPS7
PP_1V9_SMPS4
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VDD_L1
VDD_L2_L18
VDD_L3
VDD_L4
VDD_L5_L6_L16
VDD_L7
VDD_L8_L9
VDD_L10
VDD_L11_L13
VDD_L12
VDD_L14
VDD_L15
VDD_L17
VDD_L19
VDD_L20
VDD_L21
VREG_L1
VREG_L2
VREG_L18
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VREG_L4
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VREG_L6
VREG_L16
VREG_L7
VREG_L8
VREG_L9
VREG_L10
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VREG_L14_S
VREG_L17_S
PP_1V2_LDO1
PP_1V1_LDO2
PP_1V2_LDO18
PP_0V8_LDO3
PP_0V912_LDO4
PP_1V8_LDO5
PP_VIO_RFFE_1V8_RX
PP_1V776_LDO16
PP_0V752_LDO7
PP_0V8_LDO8
PP_0V8_LDO9
PP_3V1_LDO10
PP_UIM1_LDO11
PP_UIM2_LDO13
PP_1V2_LDO12
PP_0V624_LDO14
PP_1V2_LDO15
PP_0V744_LDO17
PP_0V752_LDO19
PP_0V912_LDO20
PP_0V912_LDO21
PP_0V744_LDO17_SNS
PP_0V624_LDO14
PP_0V624_LDO14_SNS
PP_0V752_LDO7
PP_0V752_LDO7_SNS
XW401_E
XW402_E
XW403_E
Title
此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制
Size
A4
Number
Revision
Date: 2024/8/16
Sheet of
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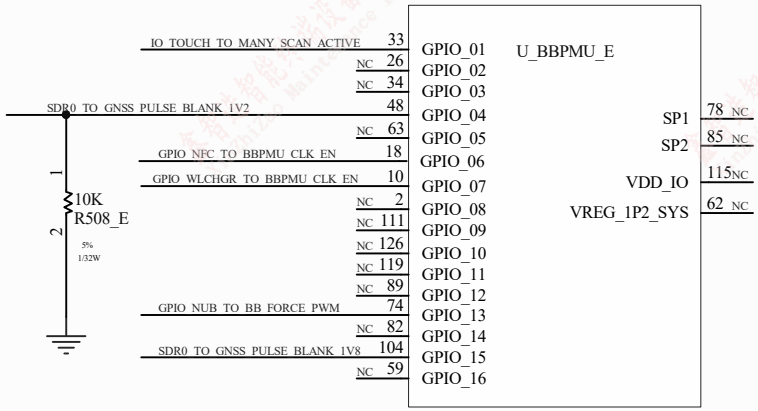
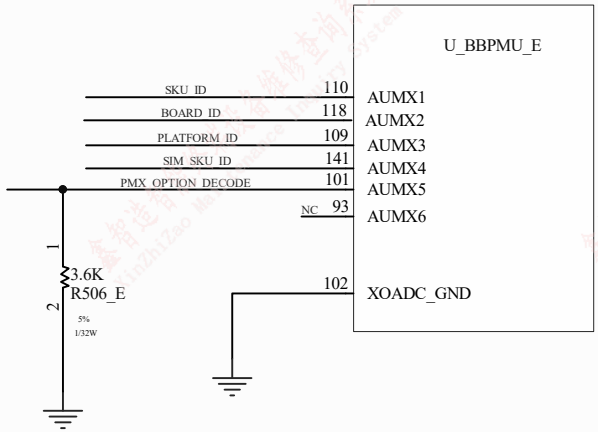
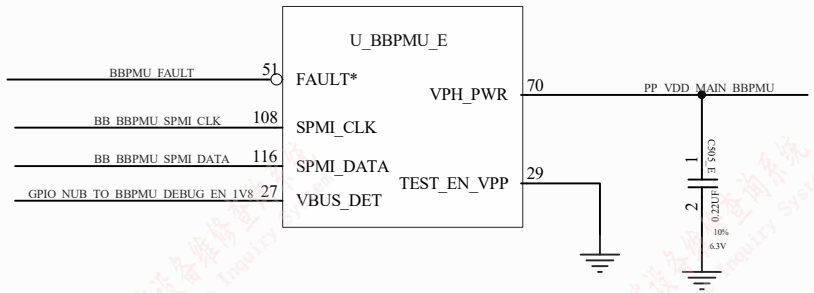
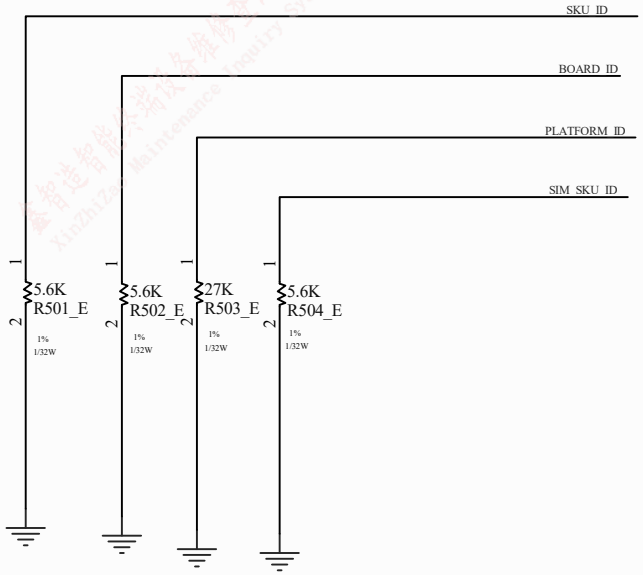
Drawn By:









Title
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Size	Number	Revision
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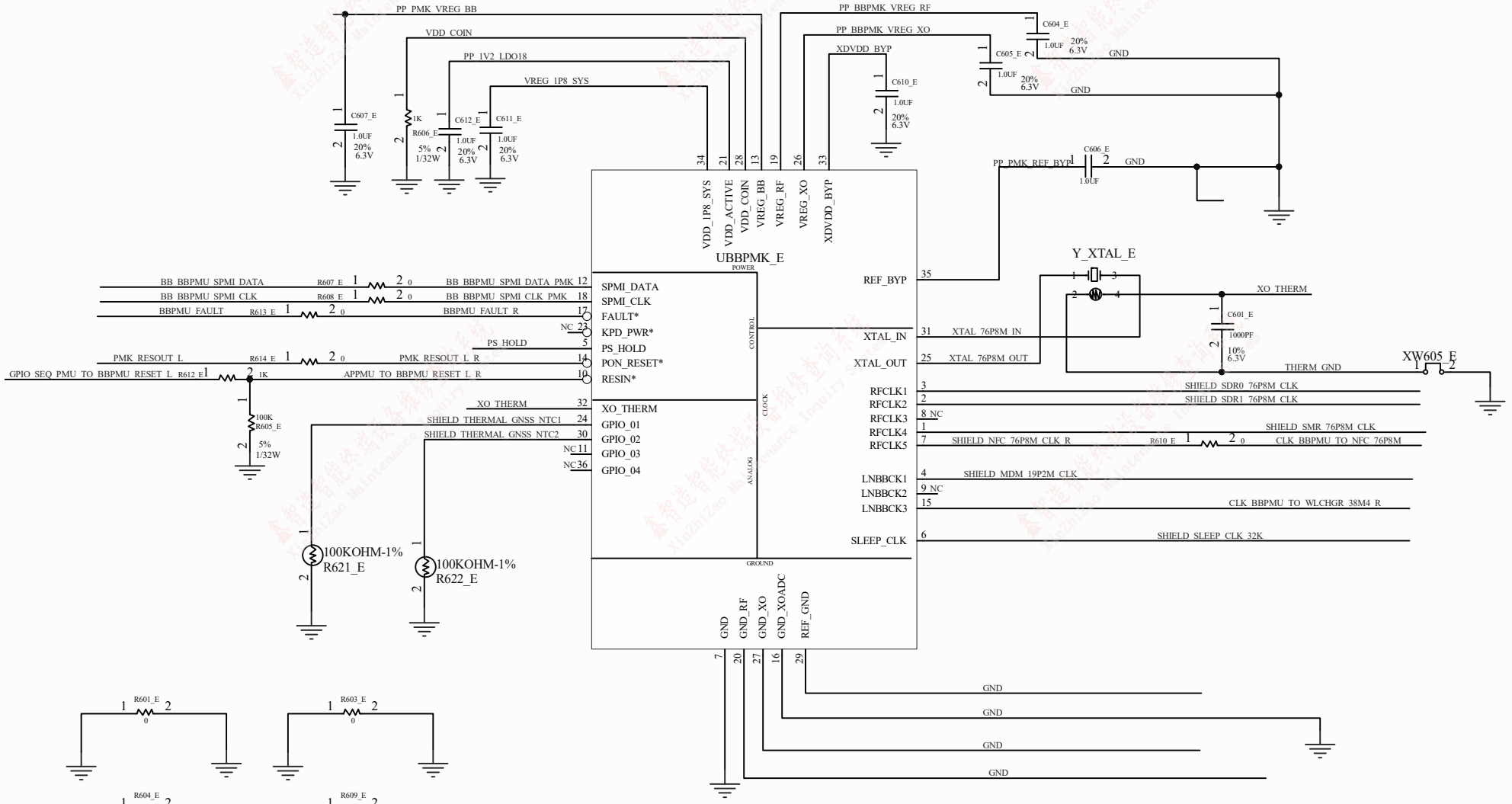

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Date: 2024/8/16	Sheet of	
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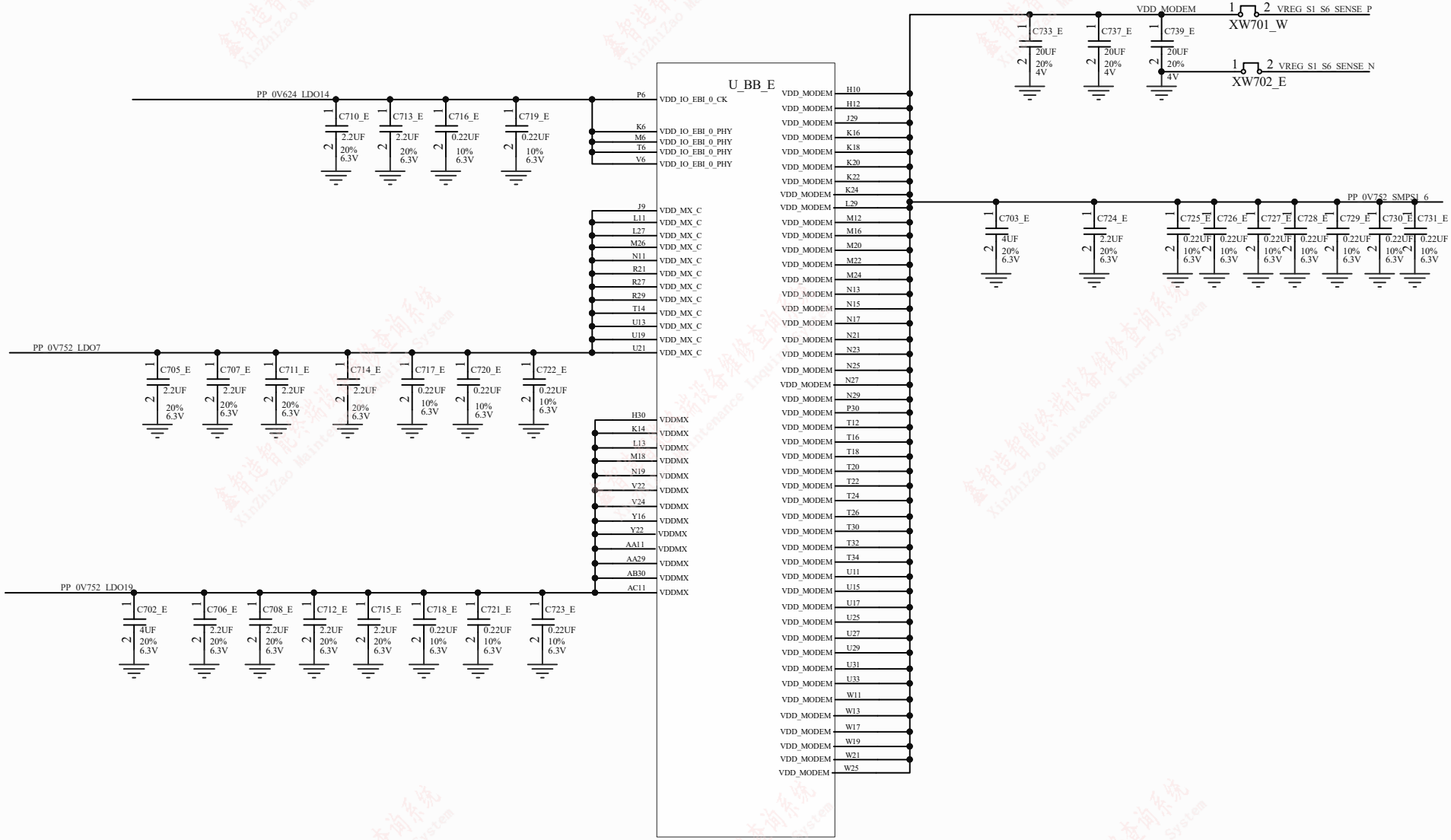

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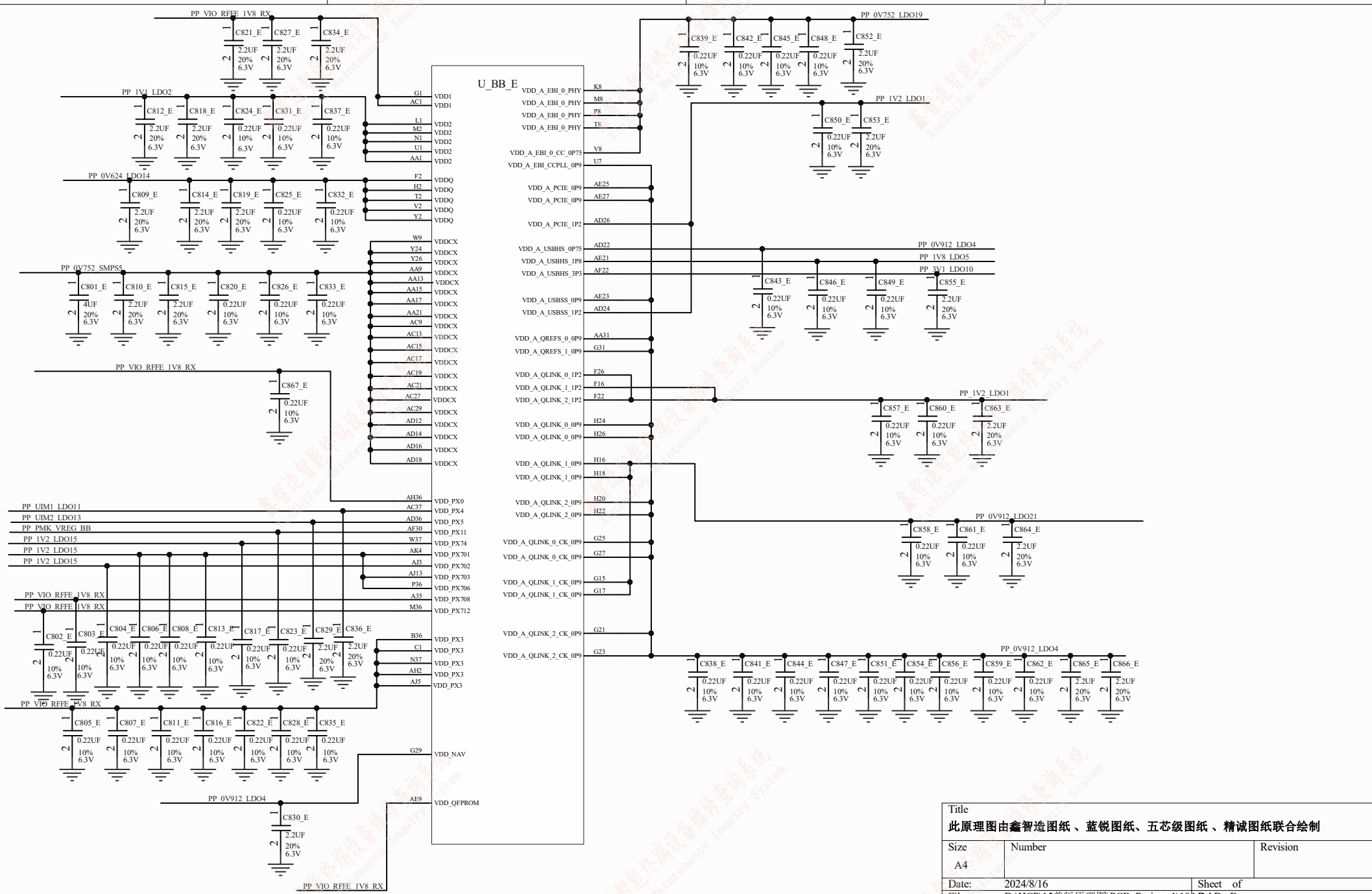

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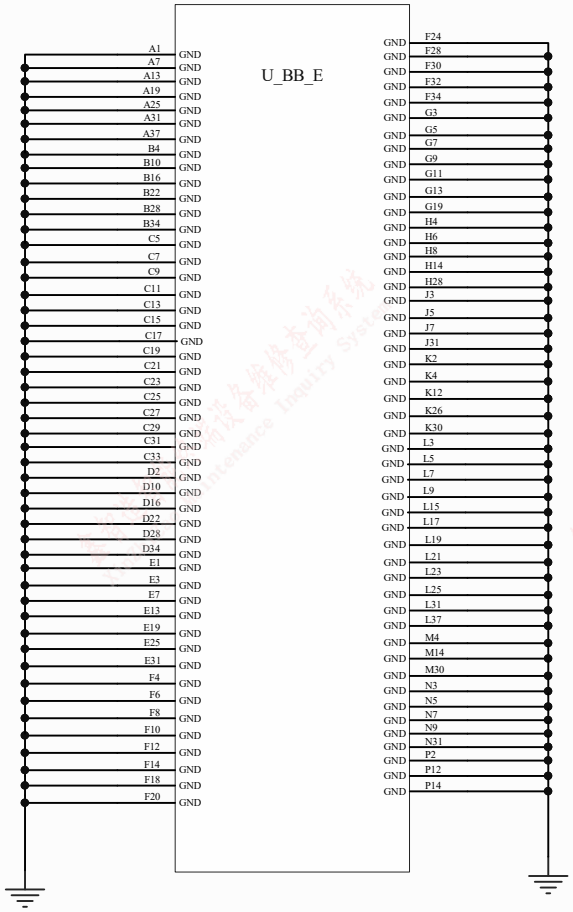

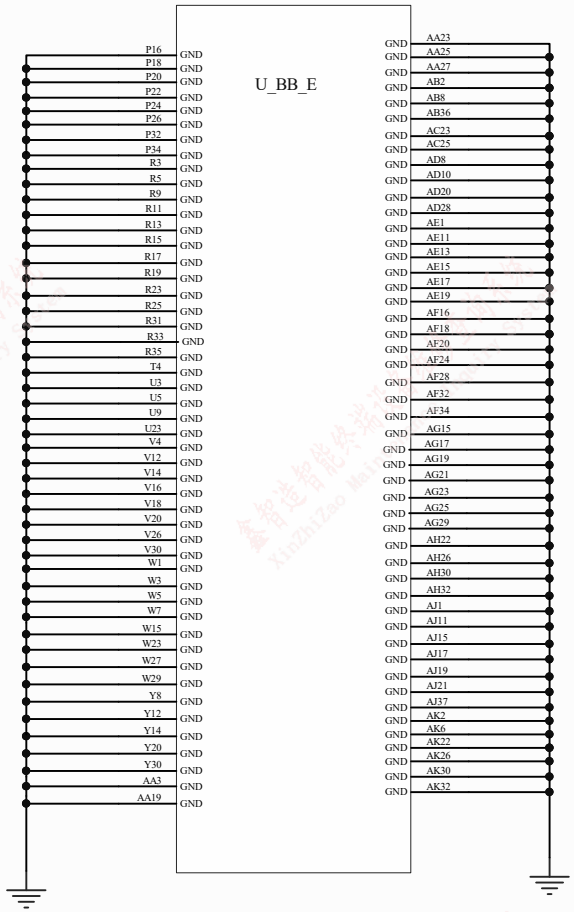

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Date: 2024/8/16		Sheet of
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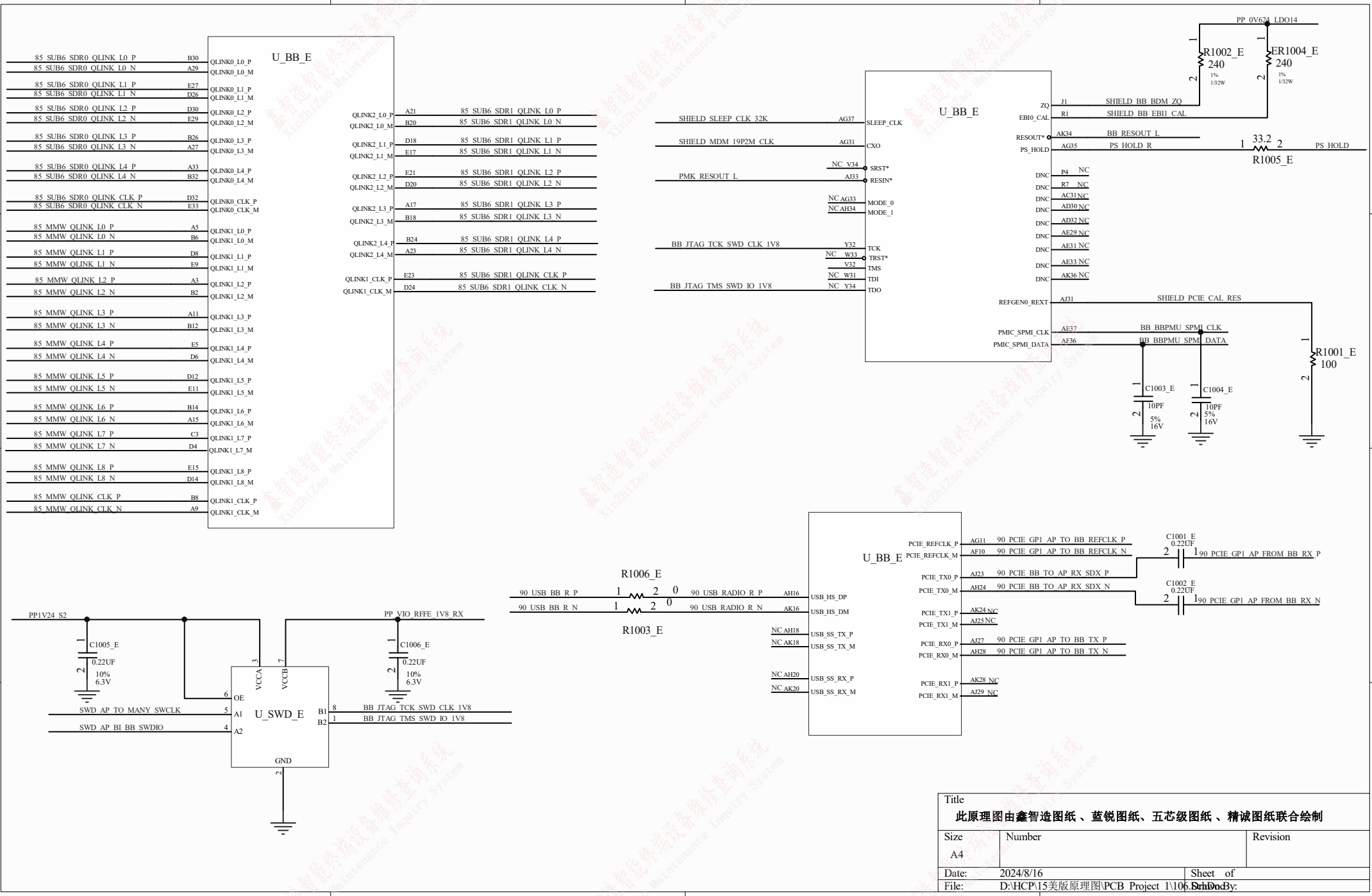
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85_SUB6_SDR0_QLINK_L2_P
85_SUB6_SDR0_QLINK_L2_N
85_SUB6_SDR0_QLINK_L3_P
85_SUB6_SDR0_QLINK_L3_N
85_SUB6_SDR0_QLINK_L4_P
85_SUB6_SDR0_QLINK_L4_N
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85_SUB6_SDR0_QLINK_CLK_N
85_MMW_QLINK_L0_P
85_MMW_QLINK_L0_N
85_MMW_QLINK_L1_P
85_MMW_QLINK_L1_N
85_MMW_QLINK_L2_P
85_MMW_QLINK_L2_N
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85_MMW_QLINK_L3_N
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85_MMW_QLINK_CLK_N
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85_SUB6_SDR1_QLINK_CLK_N
SHIELD_SLEEP_CLK_32K
SHIELD_MDM_19P2M_CLK
PMK_RESOUT_L
BB_JTAG_TCK_SWD_CLK_1V8
BB_JTAG_TMS_SWD_IO_1V8
PP_0V624_LDO14
R1002_E 240 1% 1/32W
ER1004_E 240 1% 1/32W
SHIELD_BB_BDM_ZQ
SHIELD_BB_EBI1_CAL
BB_RESOUT_L
PS_HOLD_R
33.2
R1005_E
PS_HOLD
SHIELD_PCIE_CAL_RES
BB_BBPMU_SPMI_CLK
BB_BBPMU_SPMI_DATA
R1001_E 100
C1003_E 10PF 5% 16V
C1004_E 10PF 5% 16V
R1006_E
R1003_E
90_USB_BB_R_P
90_USB_BB_R_N
90_USB_RADIO_R_P
90_USB_RADIO_R_N
90_PCIE_GP1_AP_TO_BB_REFCLK_P
90_PCIE_GP1_AP_TO_BB_REFCLK_N
90_PCIE_BB_TO_AP_RX_SDX_P
90_PCIE_BB_TO_AP_RX_SDX_N
90_PCIE_GP1_AP_TO_BB_TX_P
90_PCIE_GP1_AP_TO_BB_TX_N
C1001_E 0.22UF
C1002_E 0.22UF
90_PCIE_GP1_AP_FROM_BB_RX_P
90_PCIE_GP1_AP_FROM_BB_RX_N
PP1V24_S2
PP_VIO_RFFE_1V8_RX
C1005_E 0.22UF 10% 6.3V
C1006_E 0.22UF 10% 6.3V
U_SWD_E
SWD_AP_TO_MANY_SWCLK
SWD_AP_BI_BB_SWDIO
BB_JTAG_TCK_SWD_CLK_1V8
BB_JTAG_TMS_SWD_IO_1V8
Title
此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制
Size A4
Number
Revision
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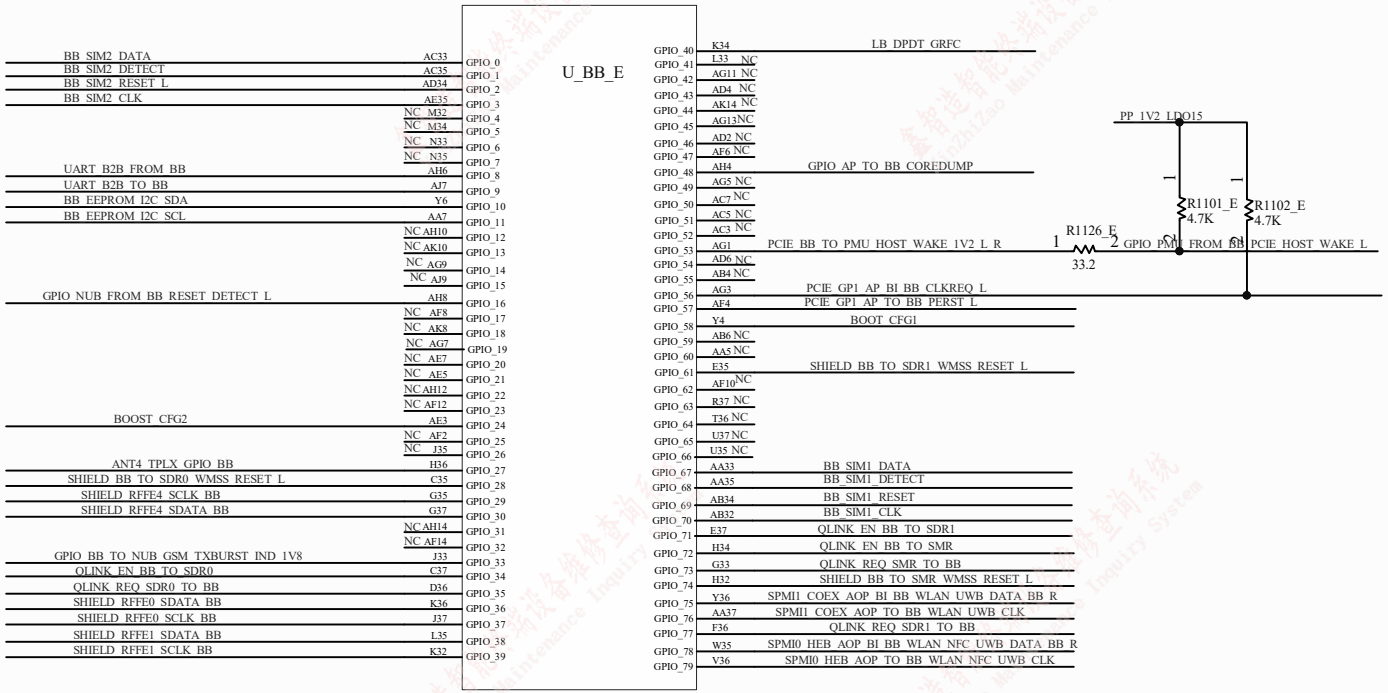
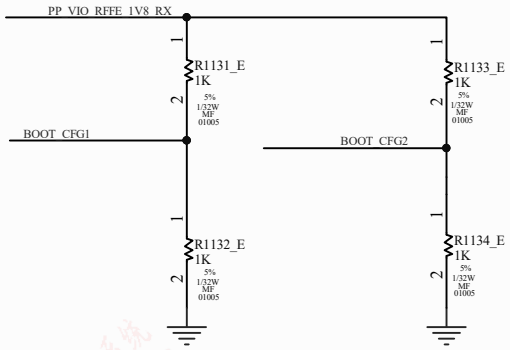
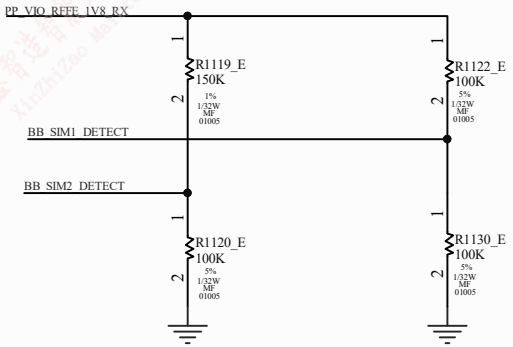
Drawn By:







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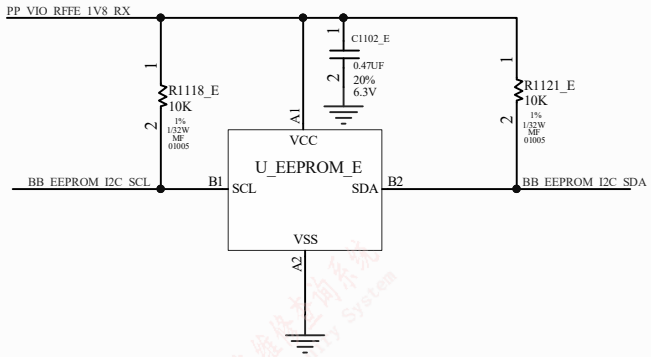
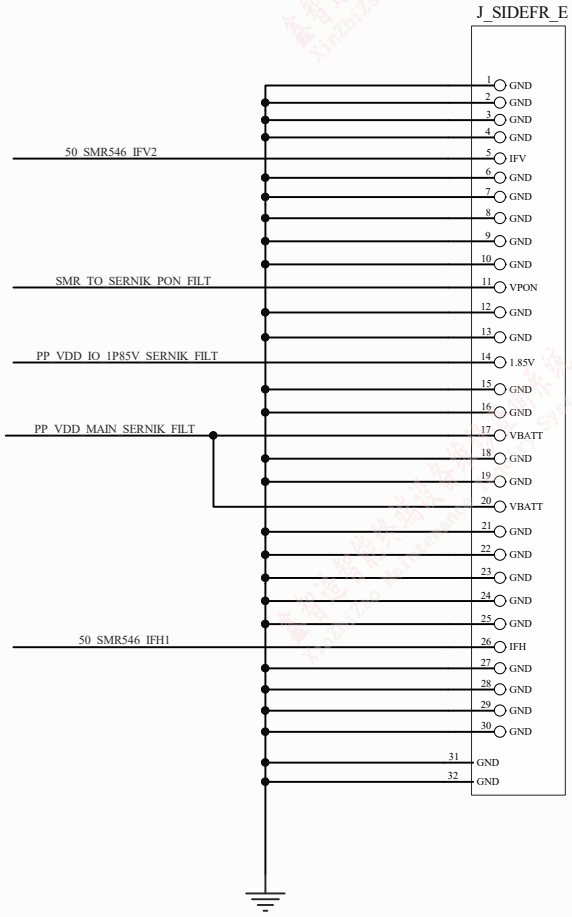
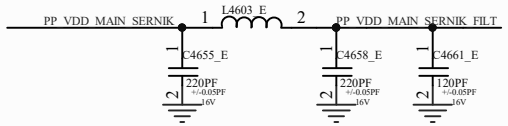
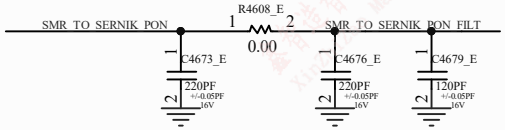


Title: 此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制		
Size: A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\107.SchDoc	Drawn By:	







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Size A4	Number	Revision
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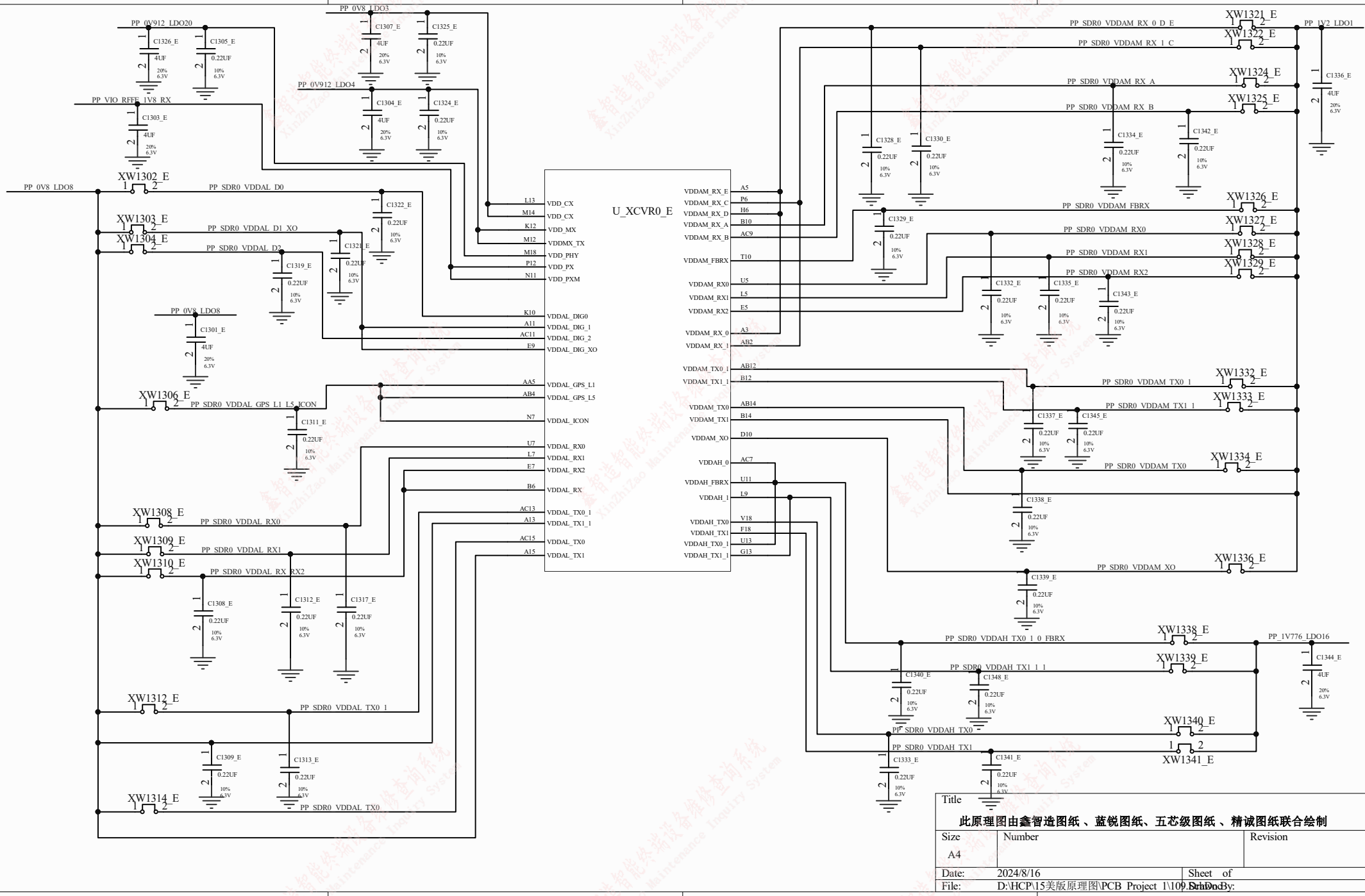
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PP_VIO_RFFE_1V8_RX
PP_0V8_LDO8
PP_0V8_LDO8
PP_SDR0_VDDAL_D0
PP_SDR0_VDDAL_D1_XO
PP_SDR0_VDDAL_D2
PP_SDR0_VDDAL_GPS_L1_L5_ICON
PP_SDR0_VDDAL_RX0
PP_SDR0_VDDAL_RX1
PP_SDR0_VDDAL_RX_RX2
PP_SDR0_VDDAL_TX0_1
PP_SDR0_VDDAL_TX0
PP_SDR0_VDDAM_RX_0_D_E
PP_SDR0_VDDAM_RX_1_C
PP_SDR0_VDDAM_RX_A
PP_SDR0_VDDAM_RX_B
PP_SDR0_VDDAM_FBRX
PP_SDR0_VDDAM_RX0
PP_SDR0_VDDAM_RX1
PP_SDR0_VDDAM_RX2
PP_SDR0_VDDAM_TX0_1
PP_SDR0_VDDAM_TX1_1
PP_SDR0_VDDAM_TX0
PP_SDR0_VDDAM_XO
PP_SDR0_VDDAH_TX0_1_0_FBRX
PP_SDR0_VDDAH_TX1_1_1
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PP_SDR0_VDDAH_TX1
PP_1V2_LDO1
PP_1V776_LDO16
Title
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Size
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Number
Revision
Date: 2024/8/16
Sheet of
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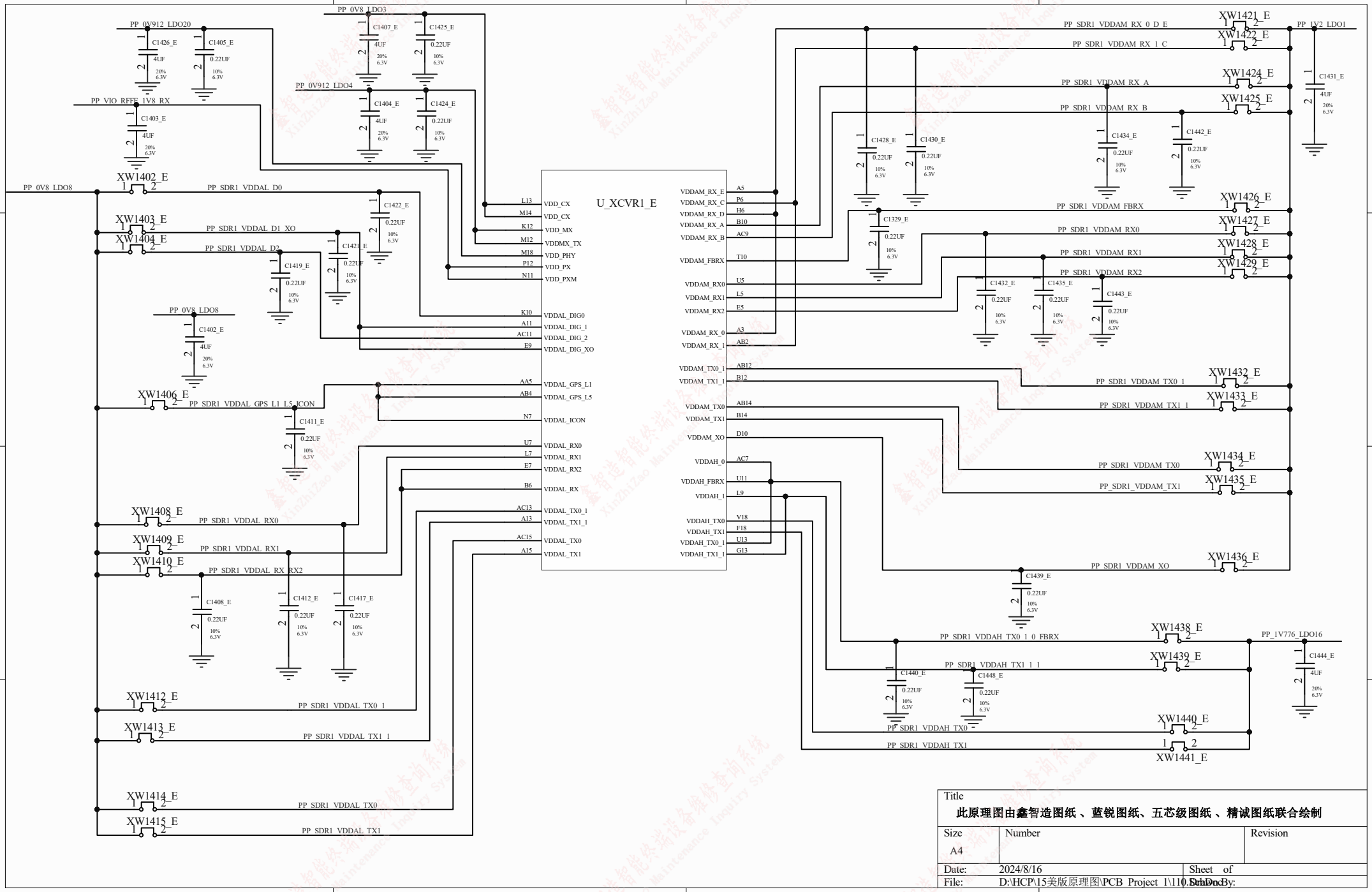
Drawn By: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PP_0V8_LDO3
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PP_VIO_RFFE_1V8_RX
PP_0V8_LDO8
PP_SDR1_VDDAL_D0
PP_SDR1_VDDAL_D1_XO
PP_SDR1_VDDAL_D2
PP_SDR1_VDDAL_GPS_L1_L5_ICON
PP_SDR1_VDDAL_RX0
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PP_SDR1_VDDAL_RX_RX2
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PP_SDR1_VDDAL_TX0
PP_SDR1_VDDAL_TX1
PP_SDR1_VDDAM_RX_0_D_E
PP_SDR1_VDDAM_RX_1_C
PP_SDR1_VDDAM_RX_A
PP_SDR1_VDDAM_RX_B
PP_SDR1_VDDAM_FBRX
PP_SDR1_VDDAM_RX0
PP_SDR1_VDDAM_RX1
PP_SDR1_VDDAM_RX2
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PP_SDR1_VDDAM_TX1
PP_SDR1_VDDAM_XO
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PP_SDR1_VDDAH_TX0
PP_SDR1_VDDAH_TX1
PP_1V2_LDO1
PP_1V776_LDO16
VDD_CX
VDD_CX
VDD_MX
VDDMX_TX
VDD_PHY
VDD_PX
VDD_PXM
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VDDAL_DIG_1
VDDAL_DIG_2
VDDAL_DIG_XO
VDDAL_GPS_L1
VDDAL_GPS_L5
VDDAL_ICON
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Title
此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制
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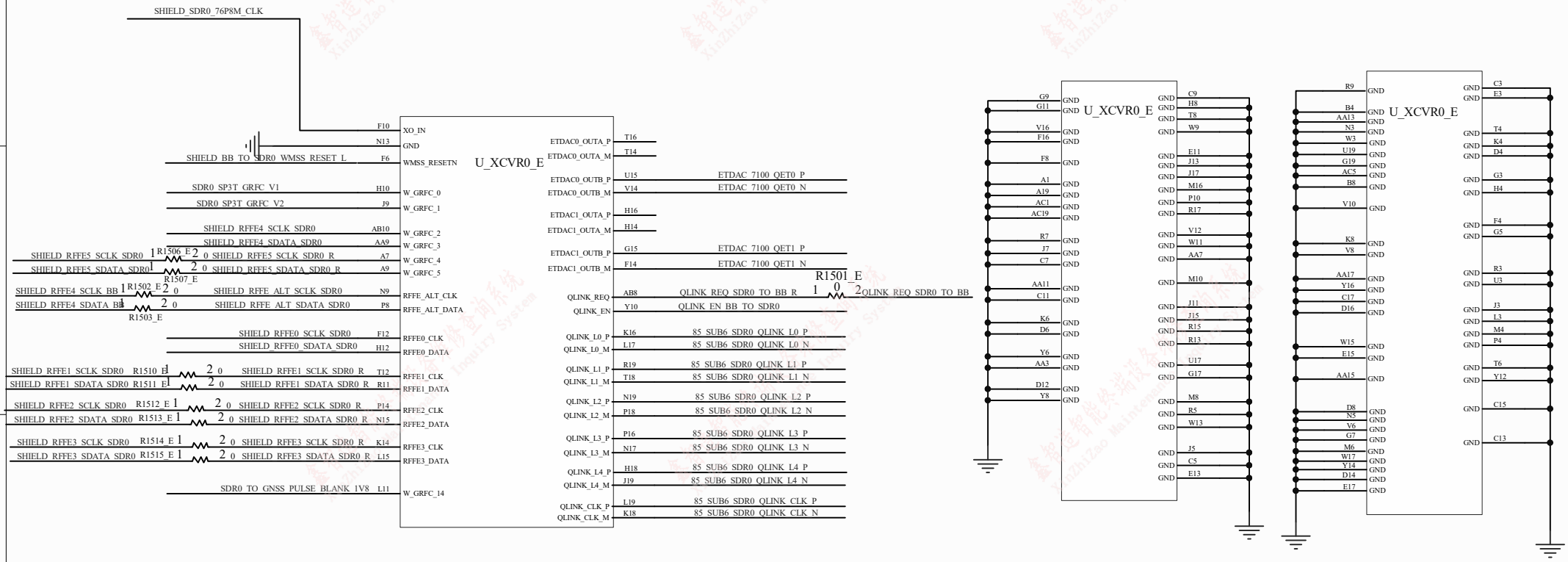

Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制
Size	A4
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Revision	
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Sheet of	
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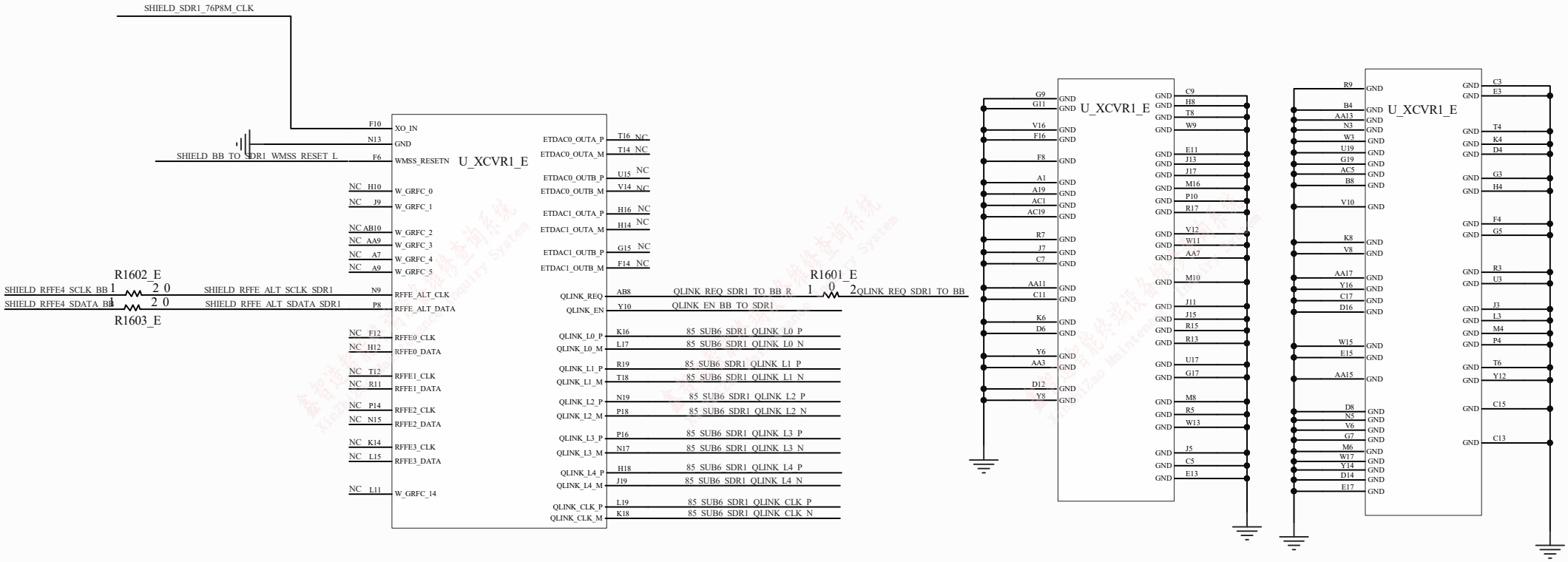

Title

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Size	Number	Revision
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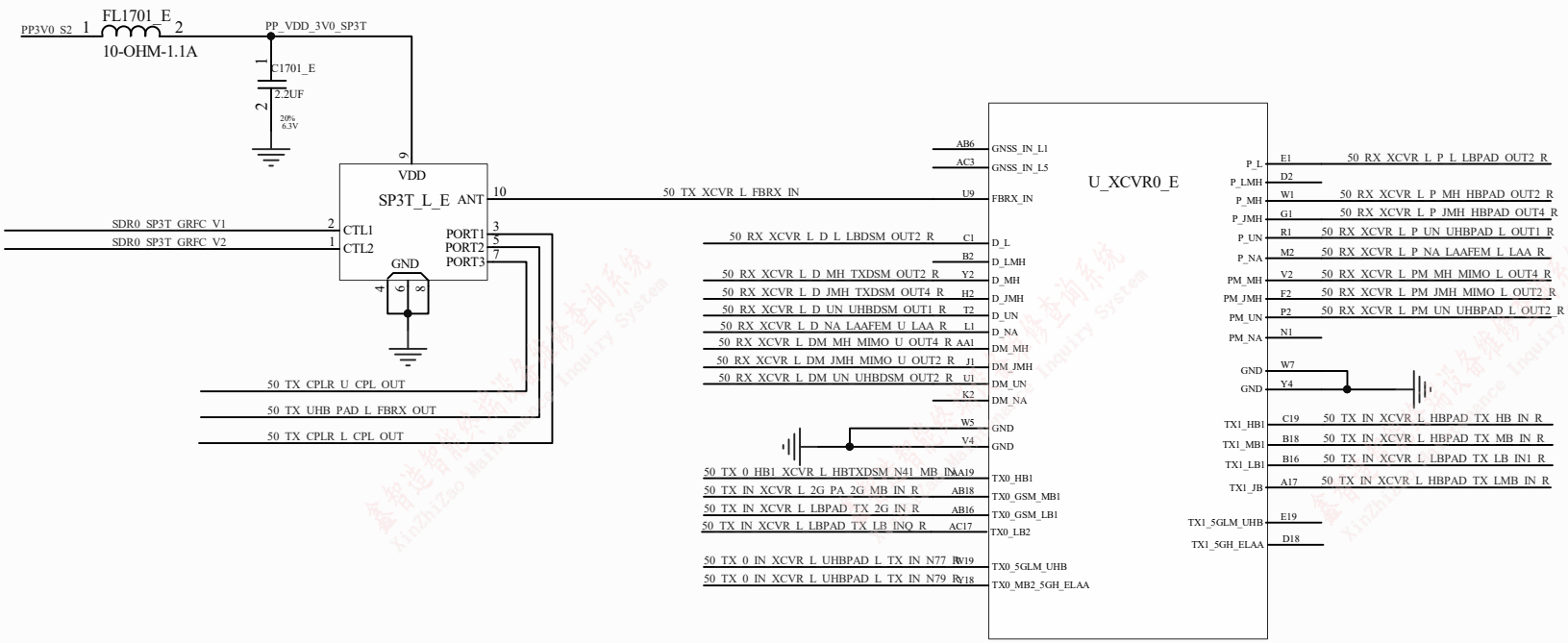
File: D:\HCP\15美版原理图\PCB Project 1\112.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
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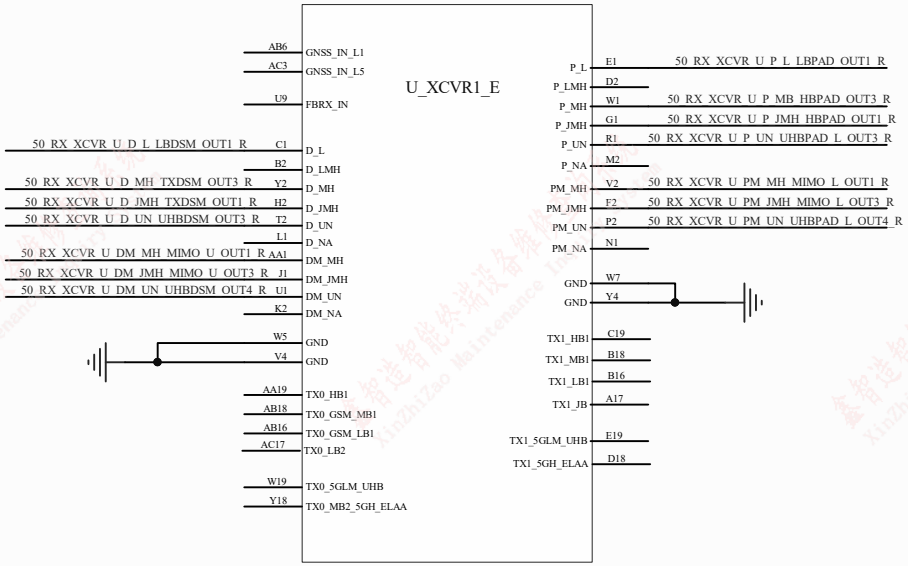
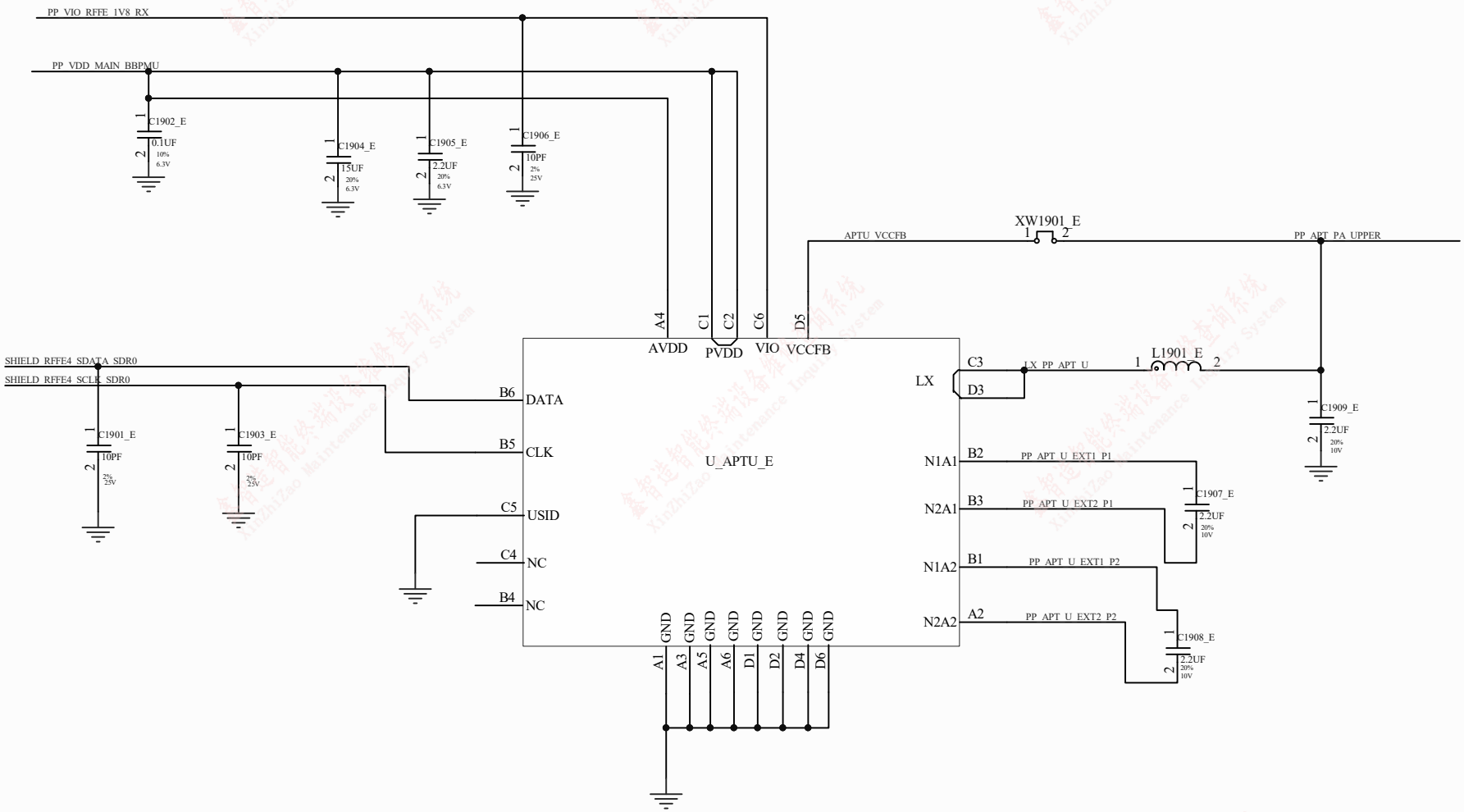


Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\114.SchDoc	Drawn By:	



Title

此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制

Size	Number	Revision
A4		

Date:	2024/8/16	Sheet of	
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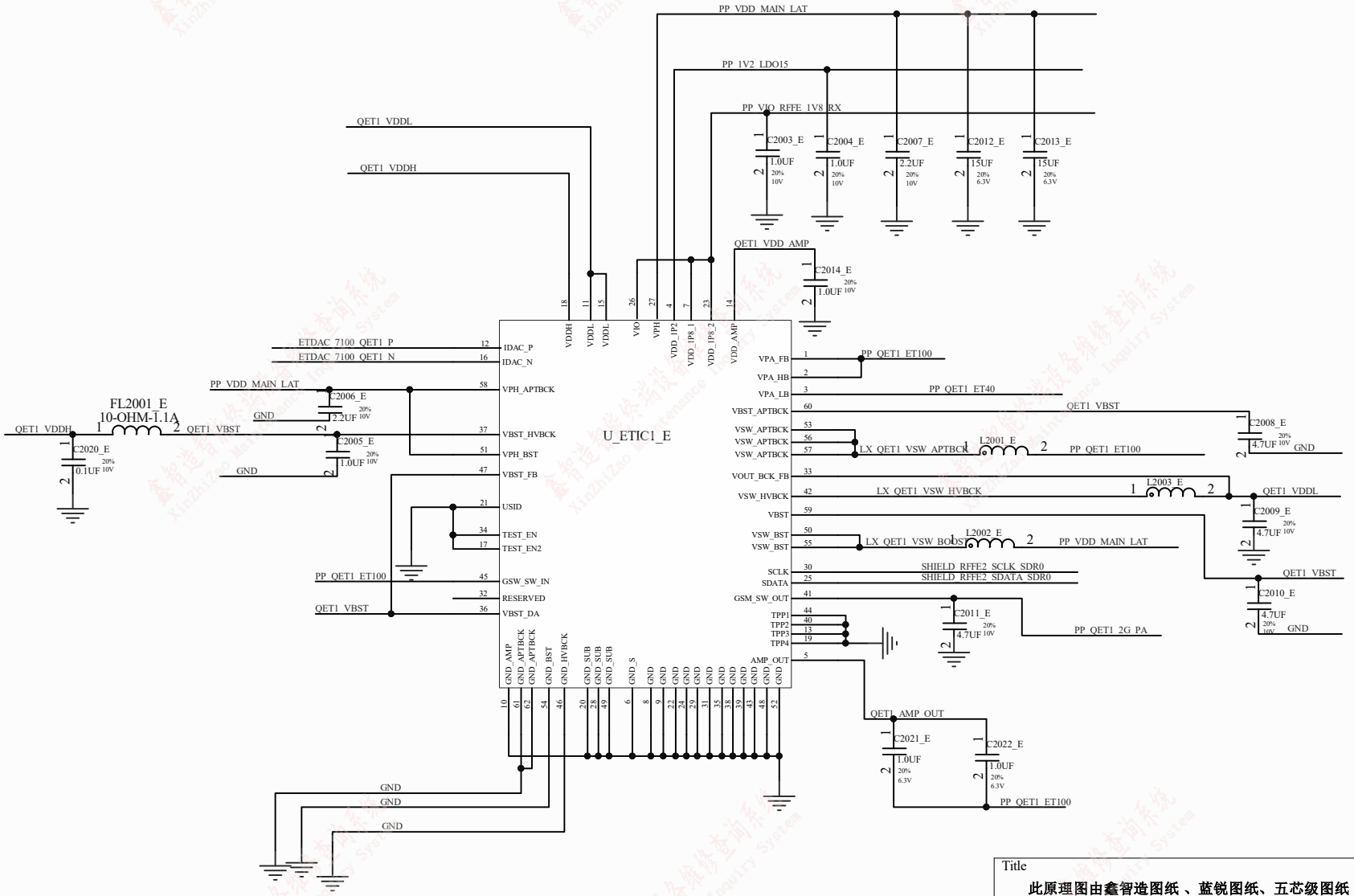
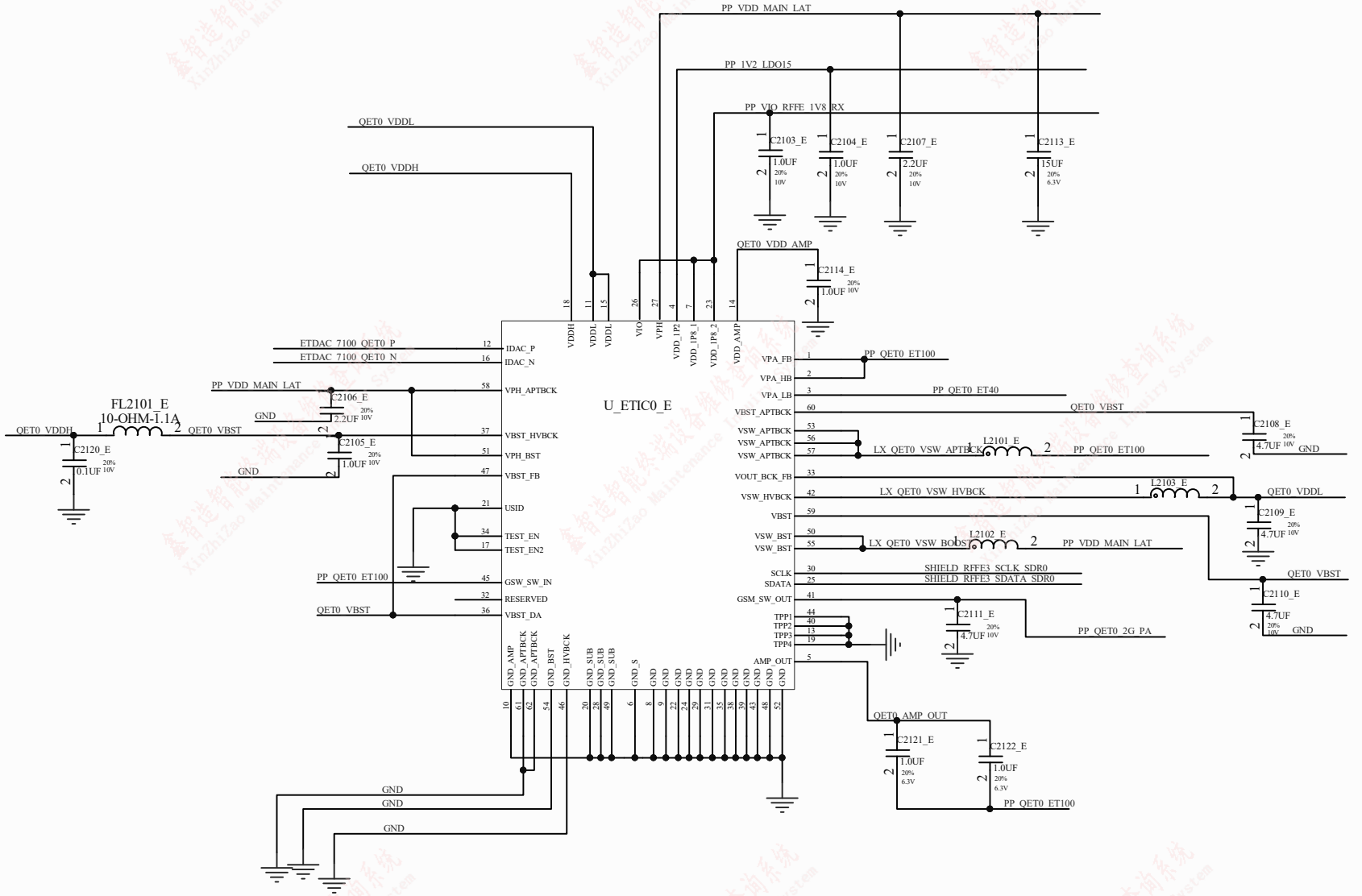


Title

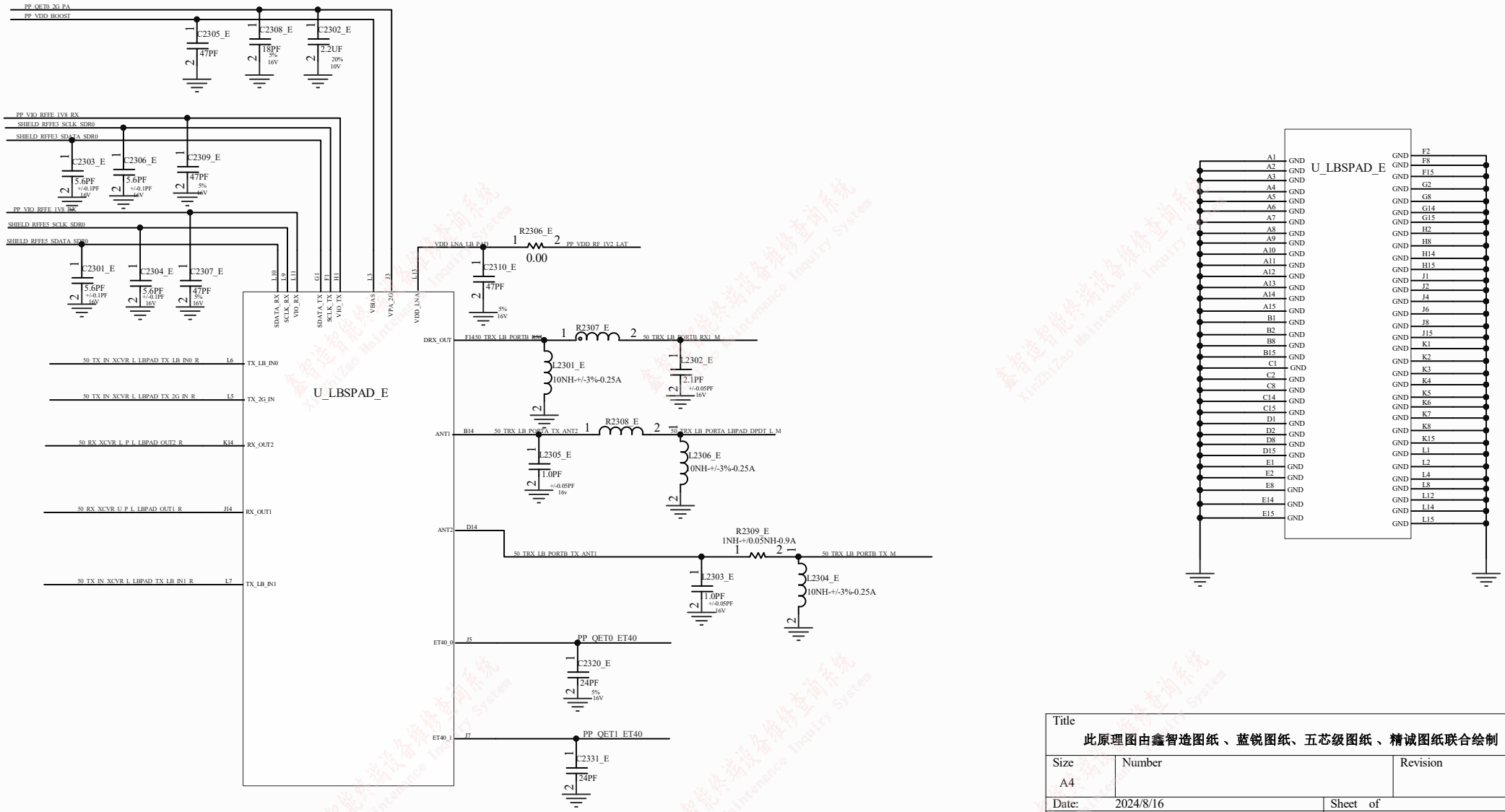
此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制

Size	Number	Revision
A4		

Date:	2024/8/16	Sheet of	
File:	D:\HCP\15美版原理图\PCB Project 1\116.SchDoc	Drawn By:	

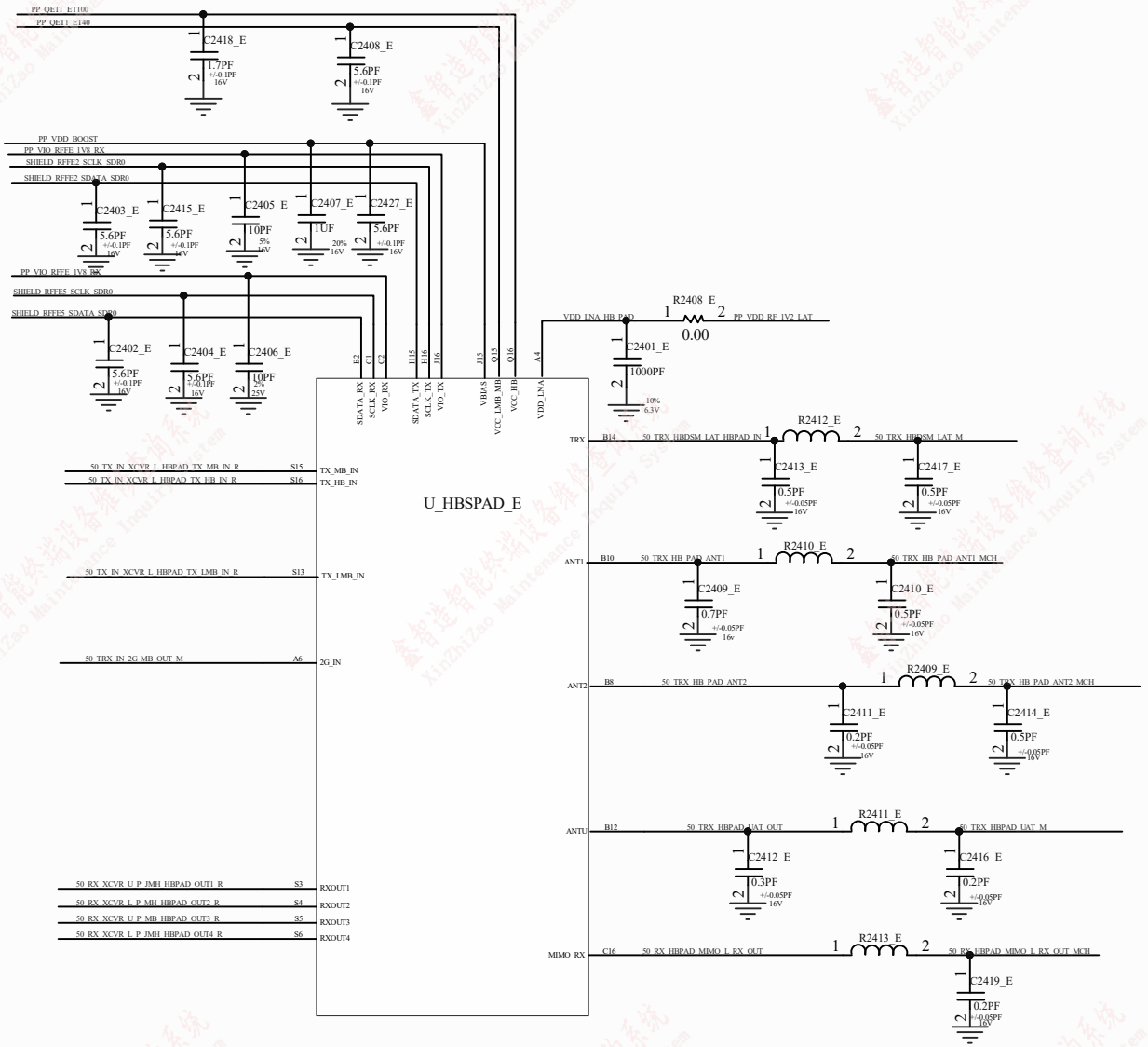


Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\117.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制
Size	A4
Number	
Revision	
Date:	2024/8/16
Sheet	of
File:	D:\HCP\15美版原理图\PCB_Project_1\118.SchDoc
Drawn By:	

鑫智造智能终端设备维修查询系统 Xinzhizao Maintenance Inquiry System



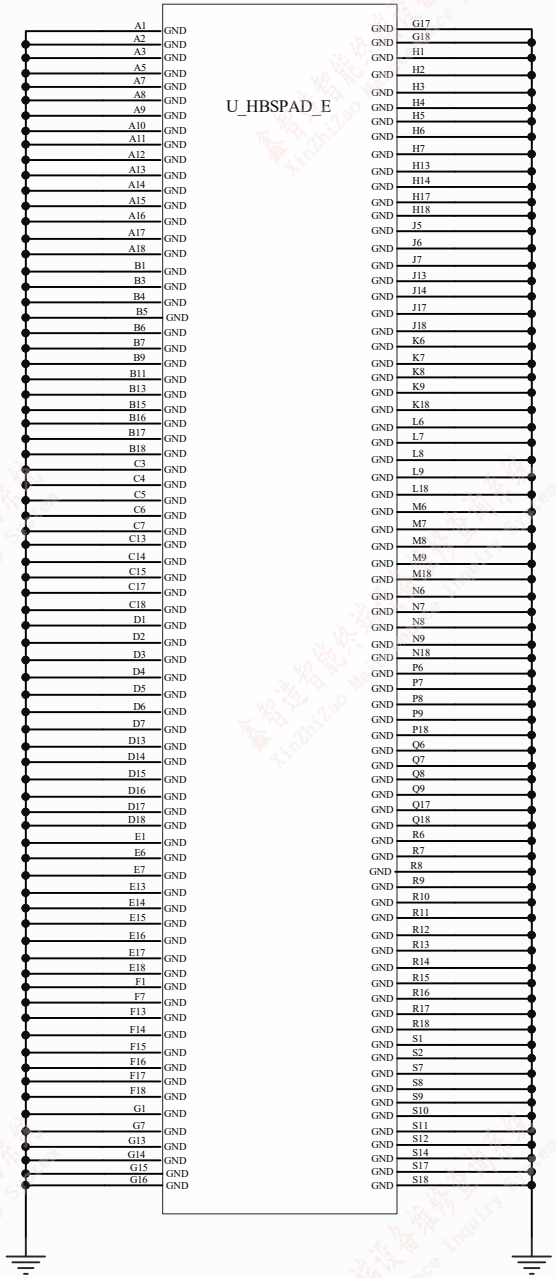
Title

此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制

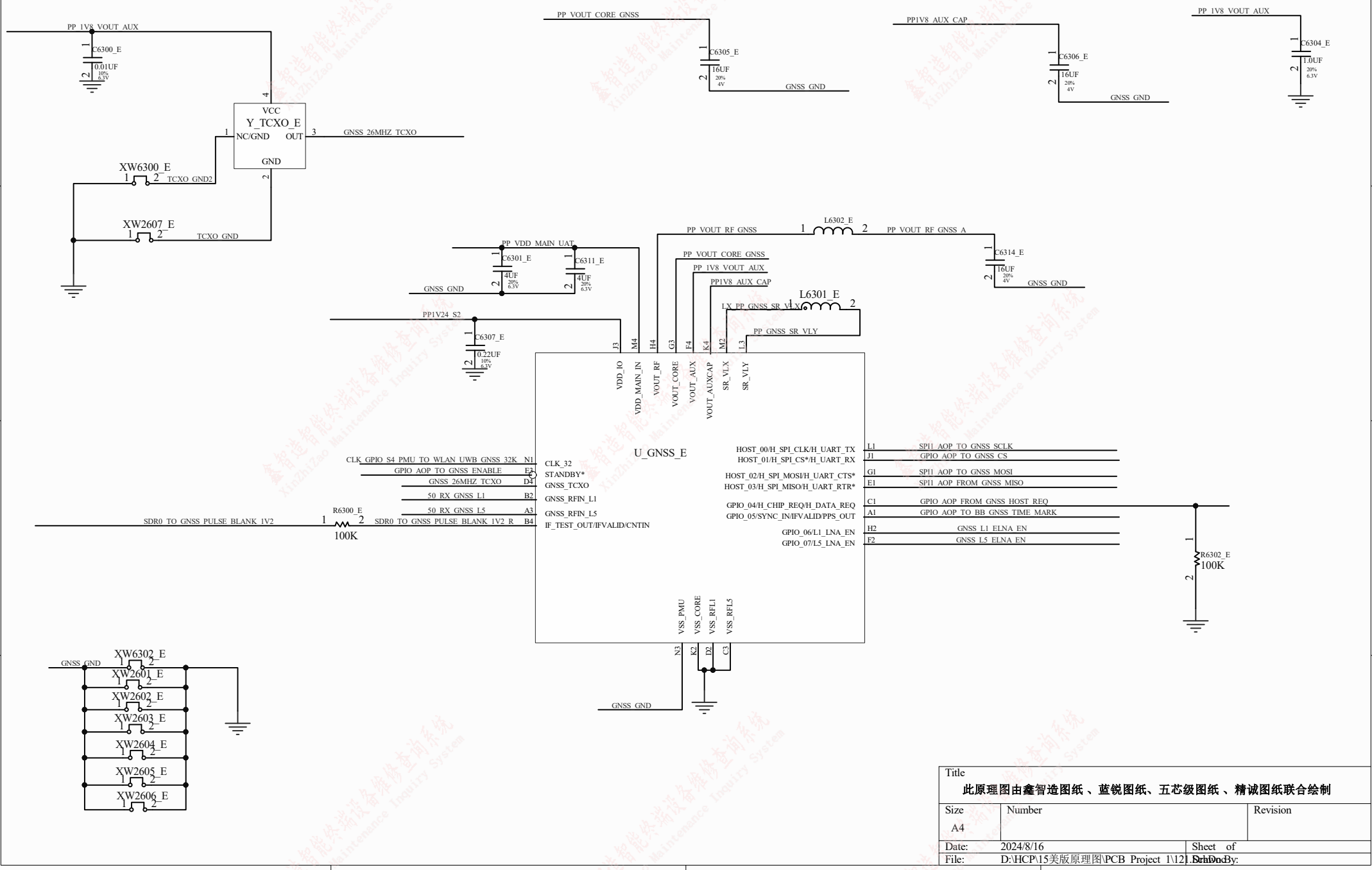
Size	Number	Revision
A4		

Date: 2024/8/16 Sheet of

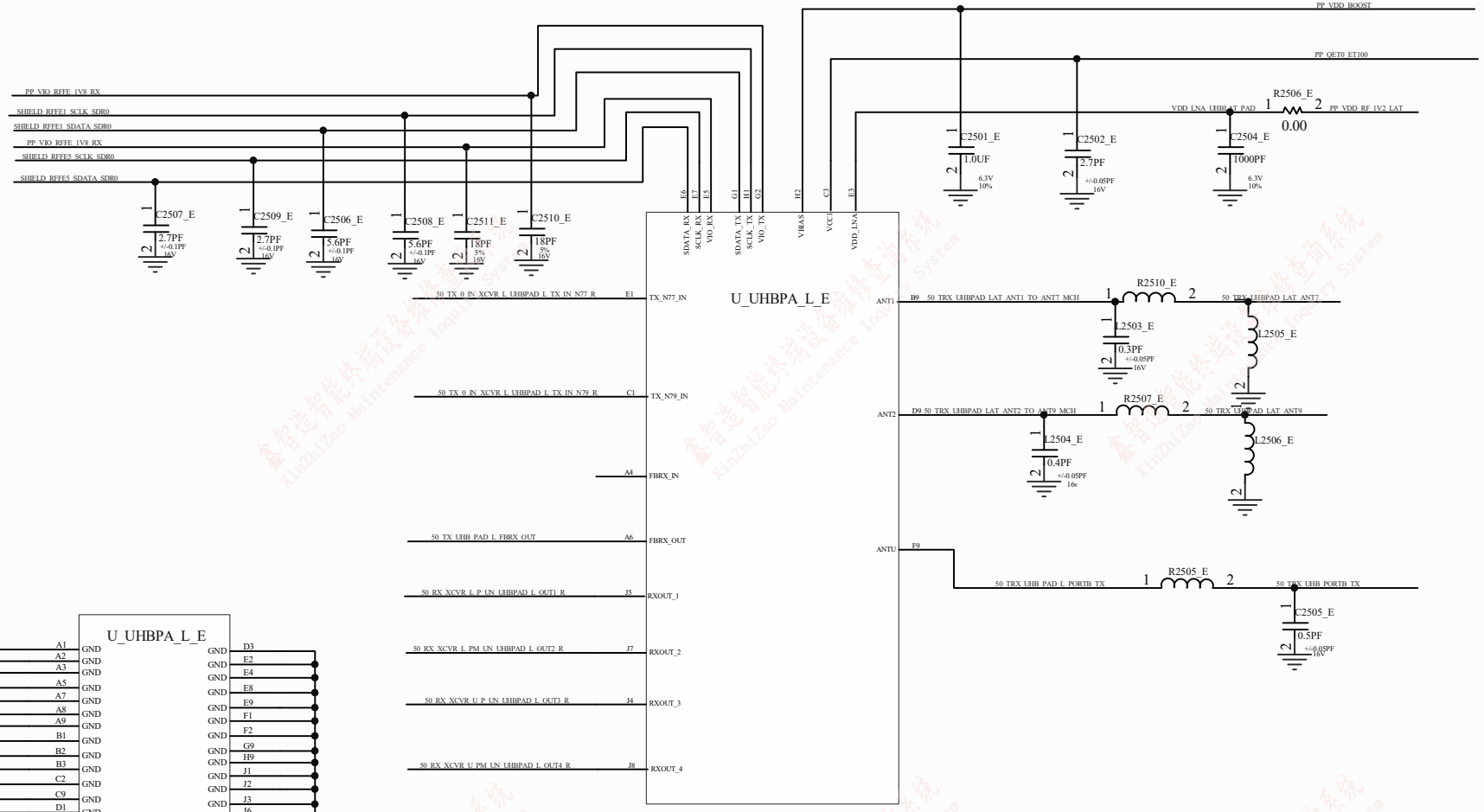
File: D:\HCP\15美版原理图\PCB Project 1\119.SchDoc Drawn By:



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16		Sheet of
File: D:\HCP\15美版原理图\PCB_Project_1\120.SchDoc		Drawn By:



Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\12[illegible].SchDoc	Drawn By:	

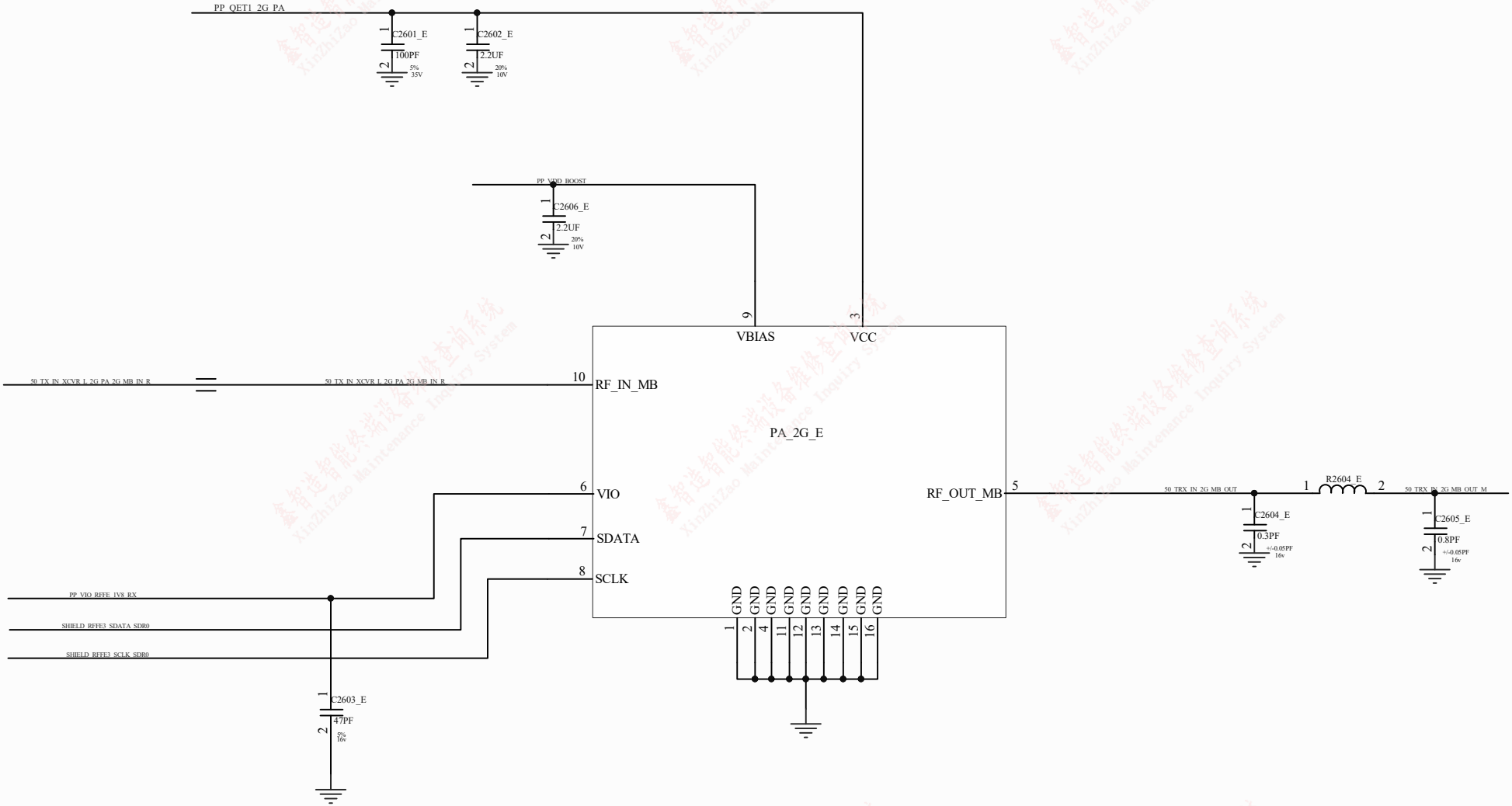


Title

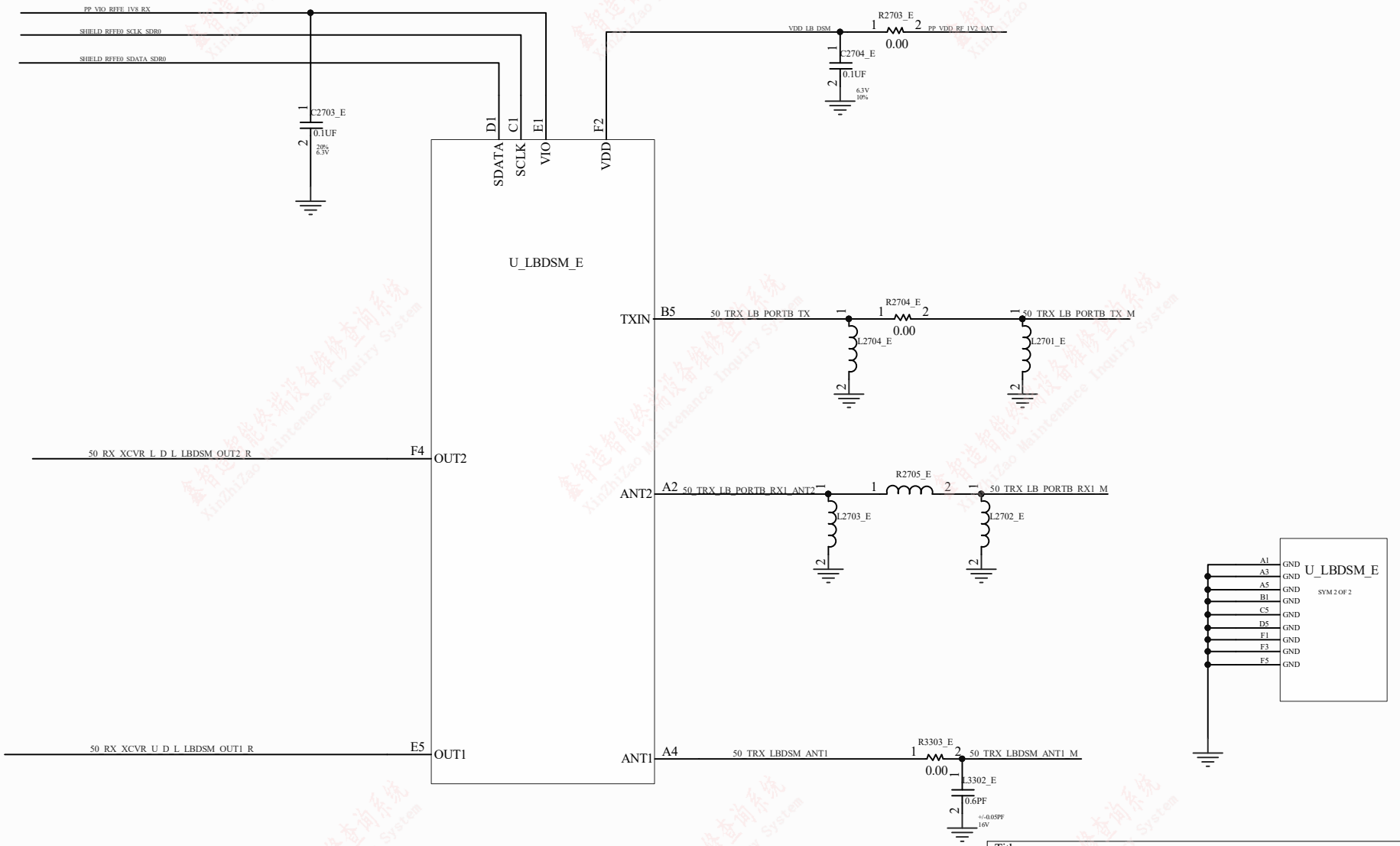
此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制

Size	Number	Revision
A4		

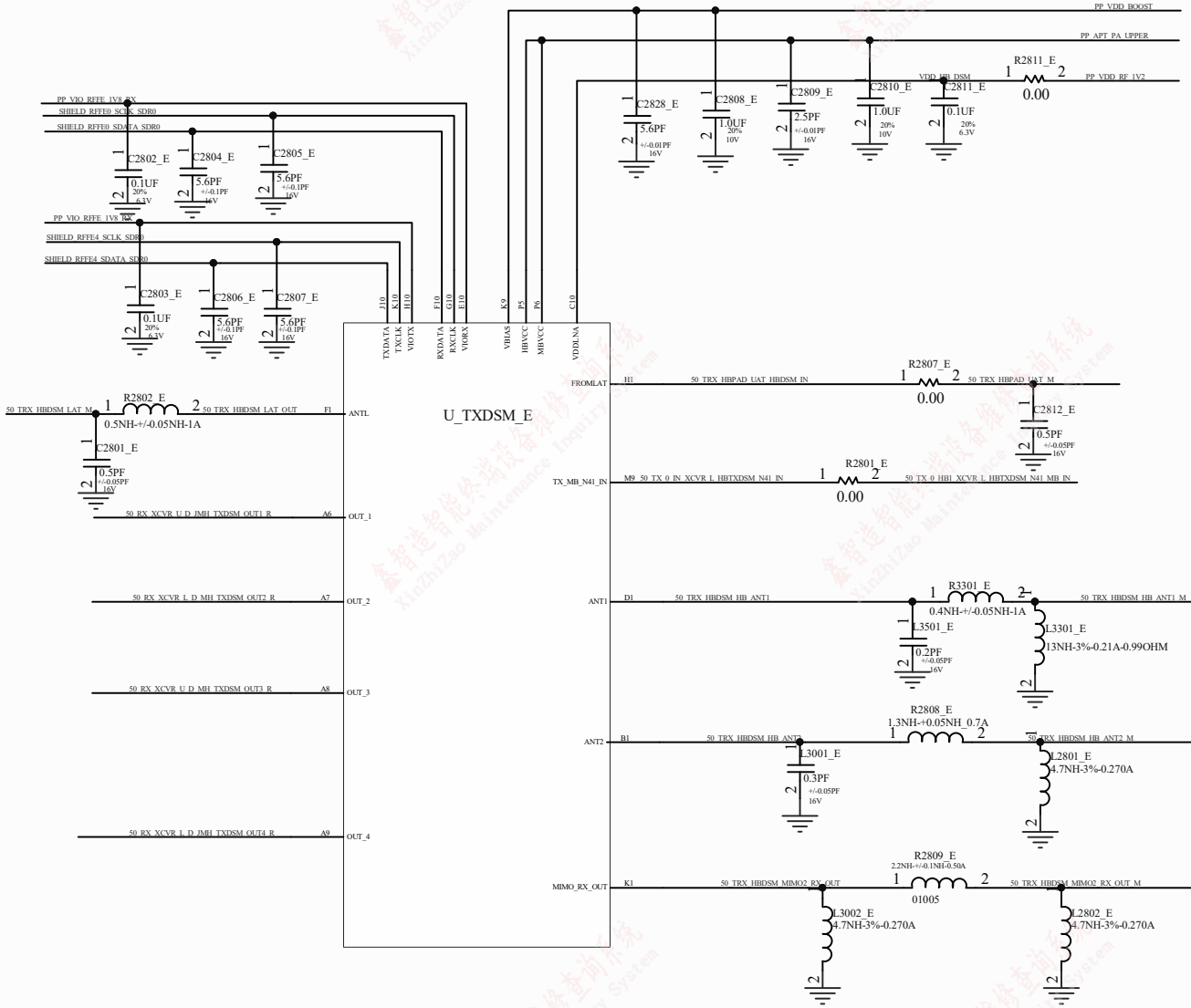
Date:	2024/8/16	Sheet of	
File:	D:\HCP\15美版原理图\PCB Project 1\122.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\123.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB_Project_1\124.SchDoc	Drawn By:	



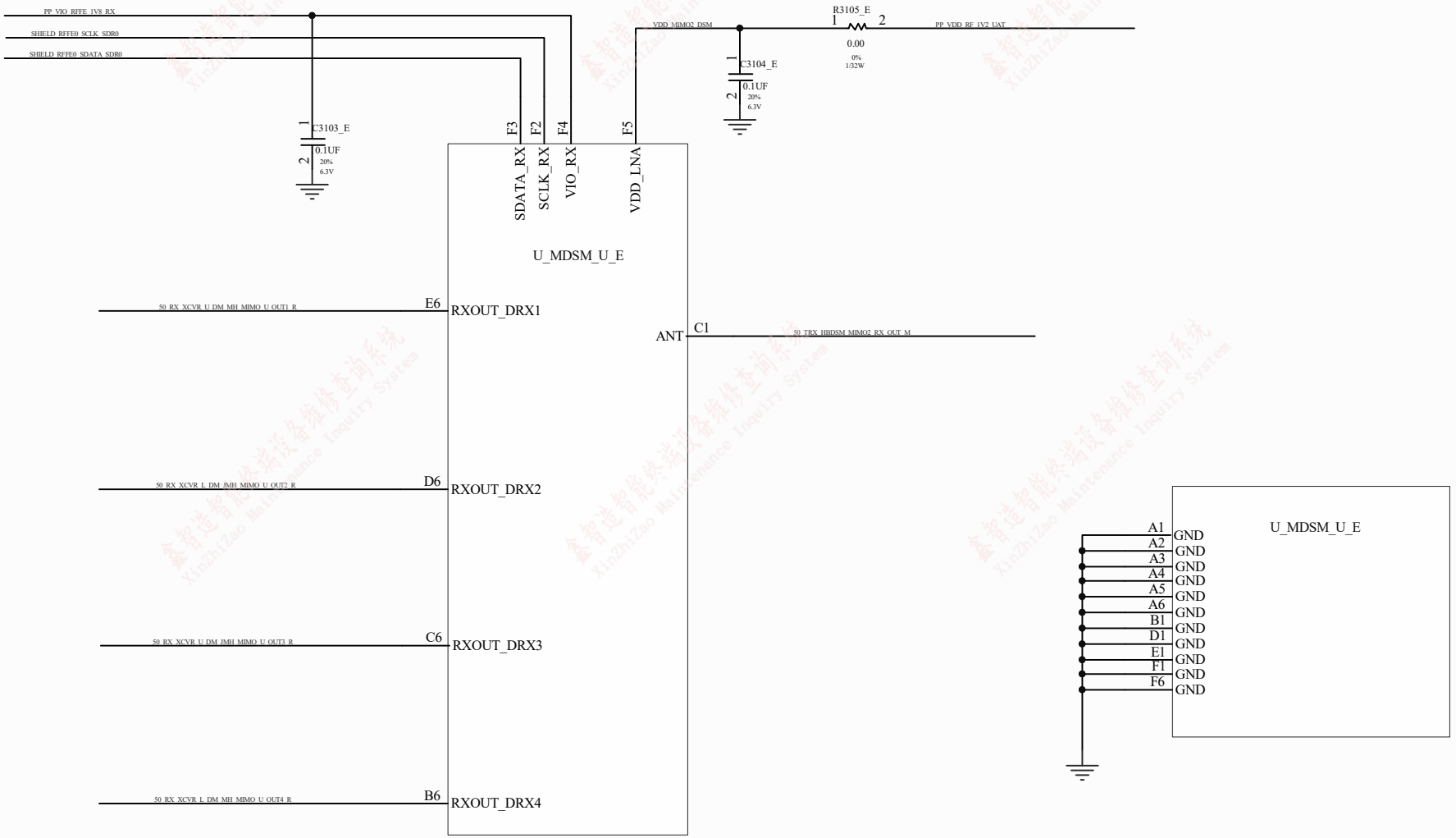
Title

此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制

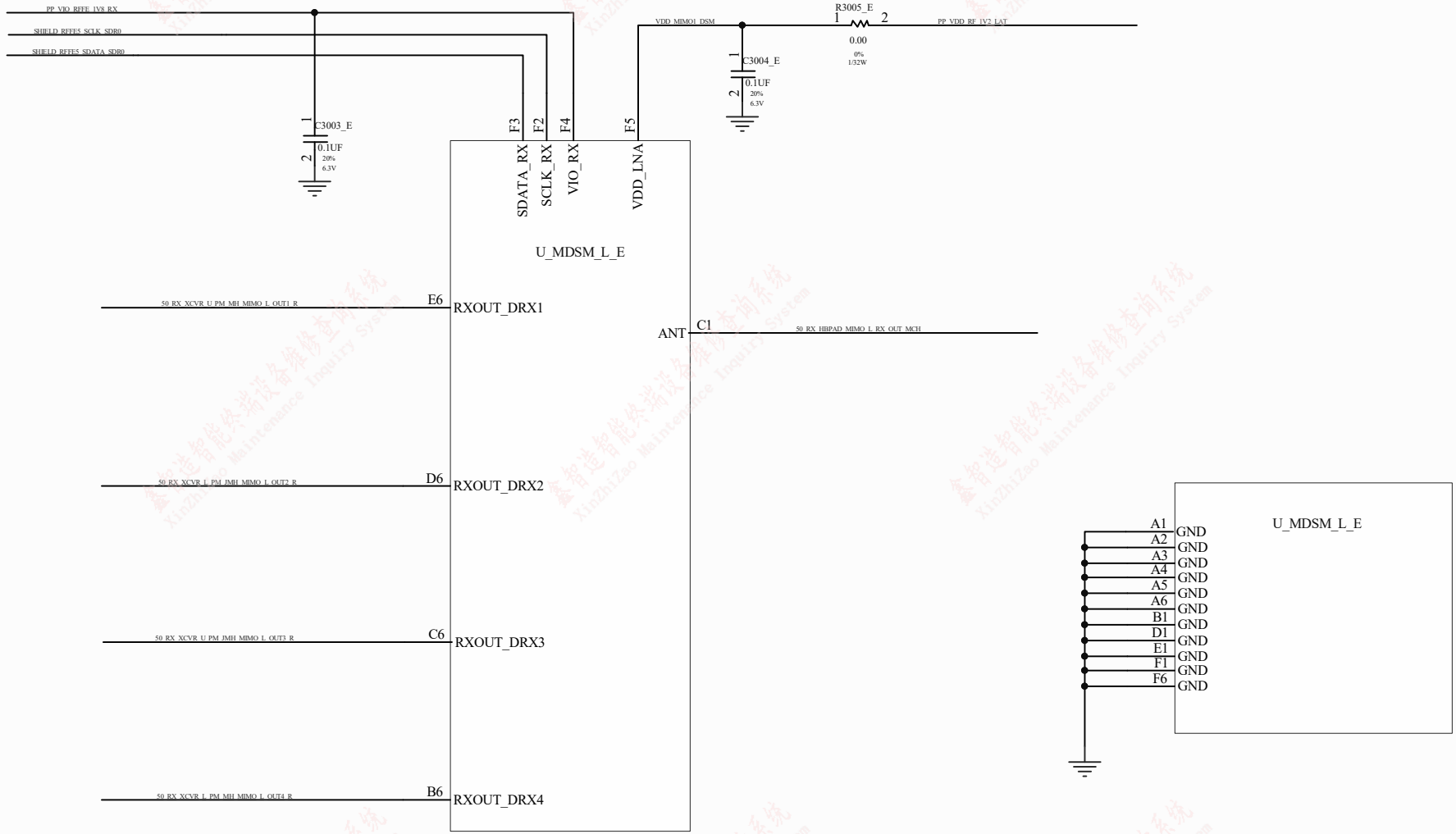
Size	Number	Revision
A4		

Date: 2024/8/16 Sheet of

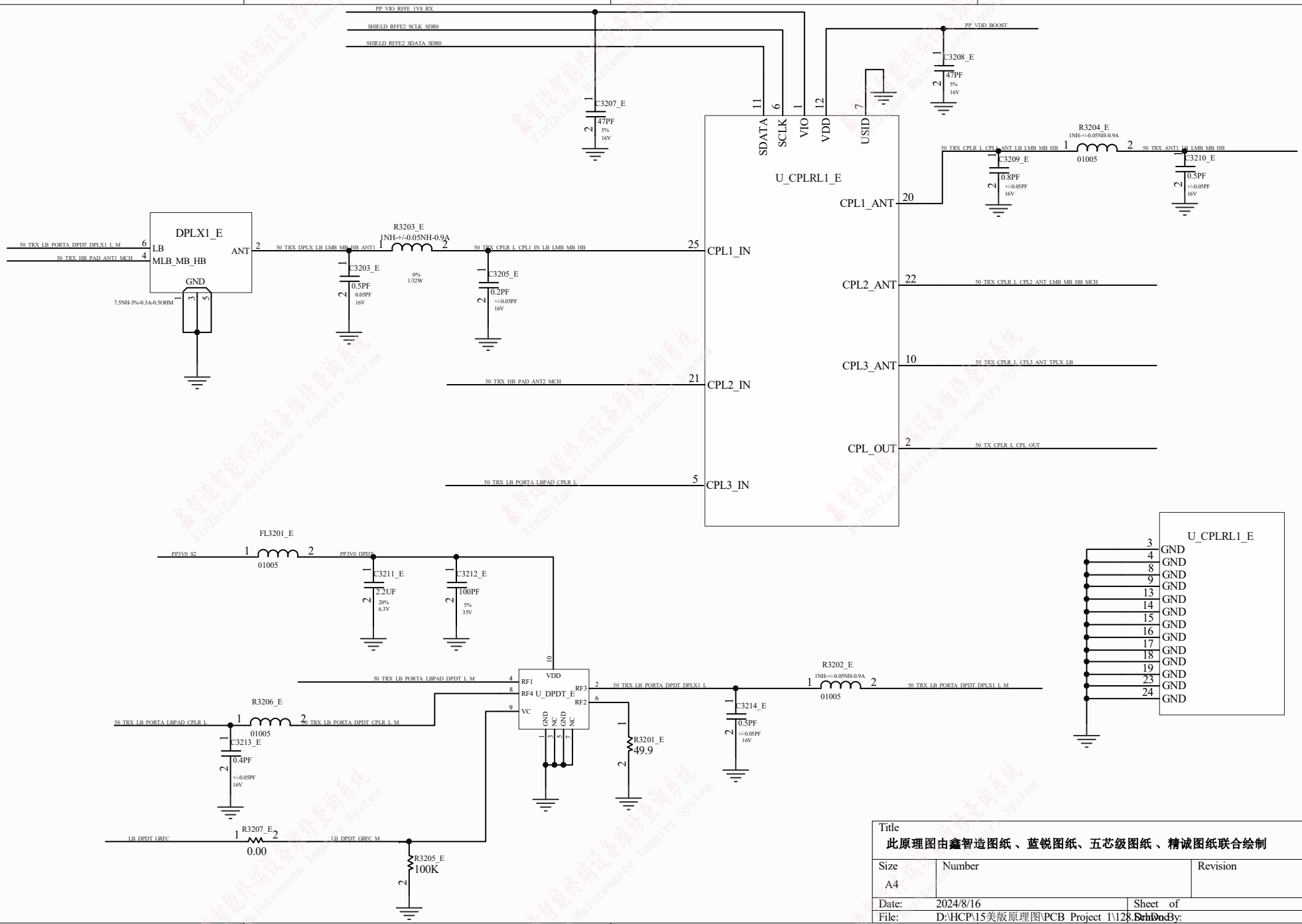
File: D:\HCP\15美版原理图\PCB Project 1\125.SchDoc Drawn By:



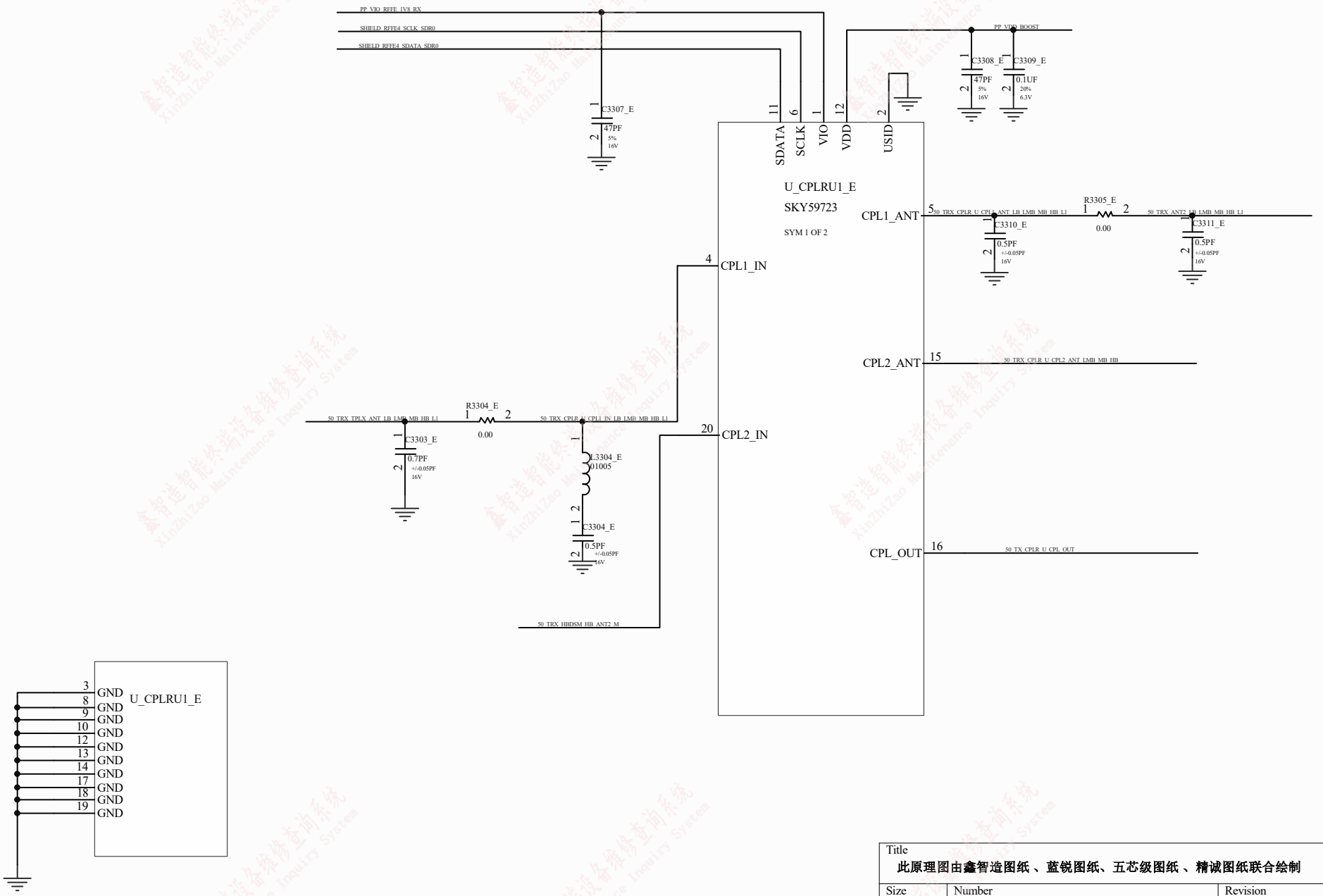
Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\126.SchDoc	Drawn By:	



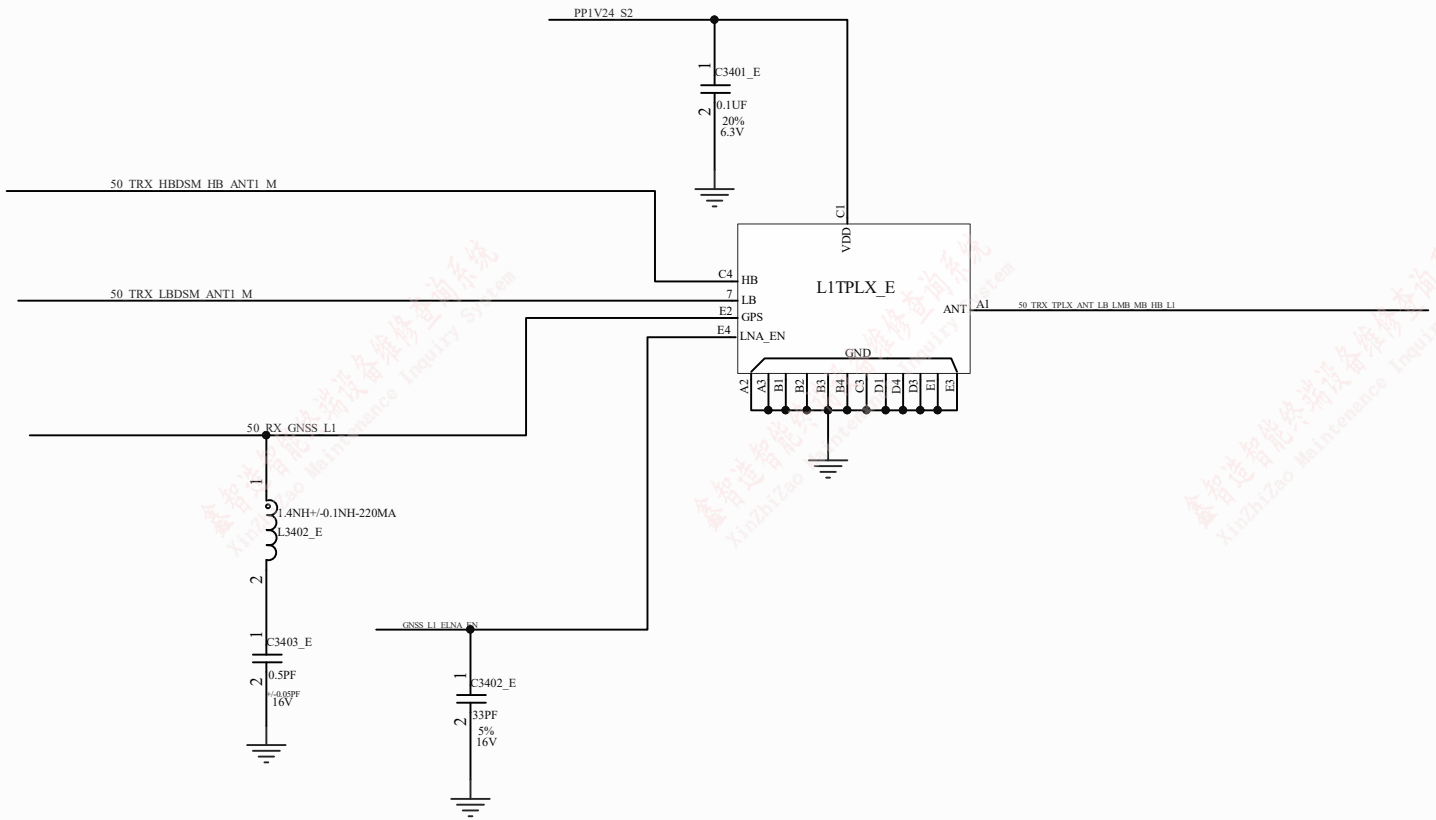
Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB_Project_1\127.SchDoc	Drawn By:	



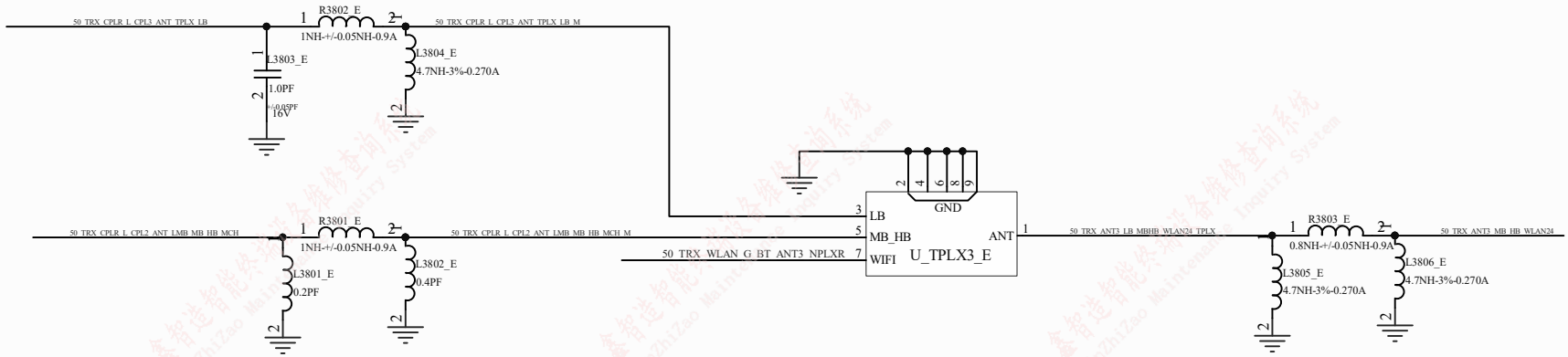
Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB_Project_1\128.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB_Project_1\129.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制		
Size A4	Number		Revision
Date:	2024/8/16	Sheet of	
File:	D:\HCP\15美版原理图\PCB Project 1\130.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
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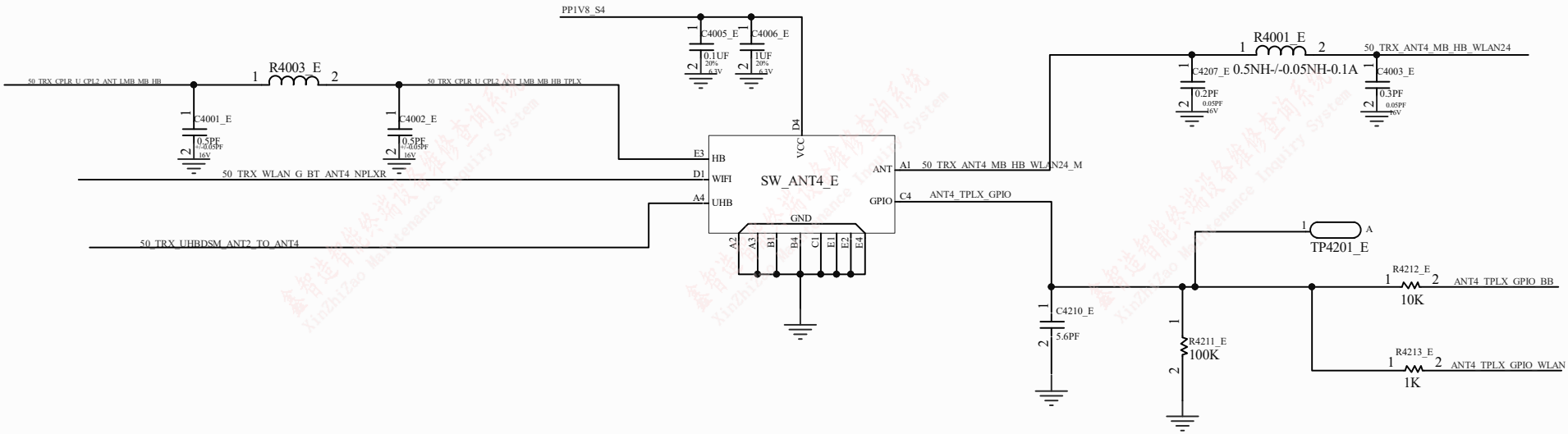
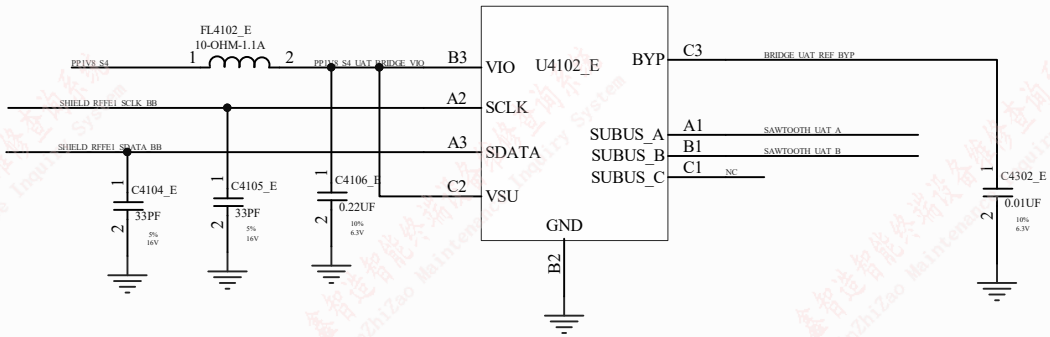
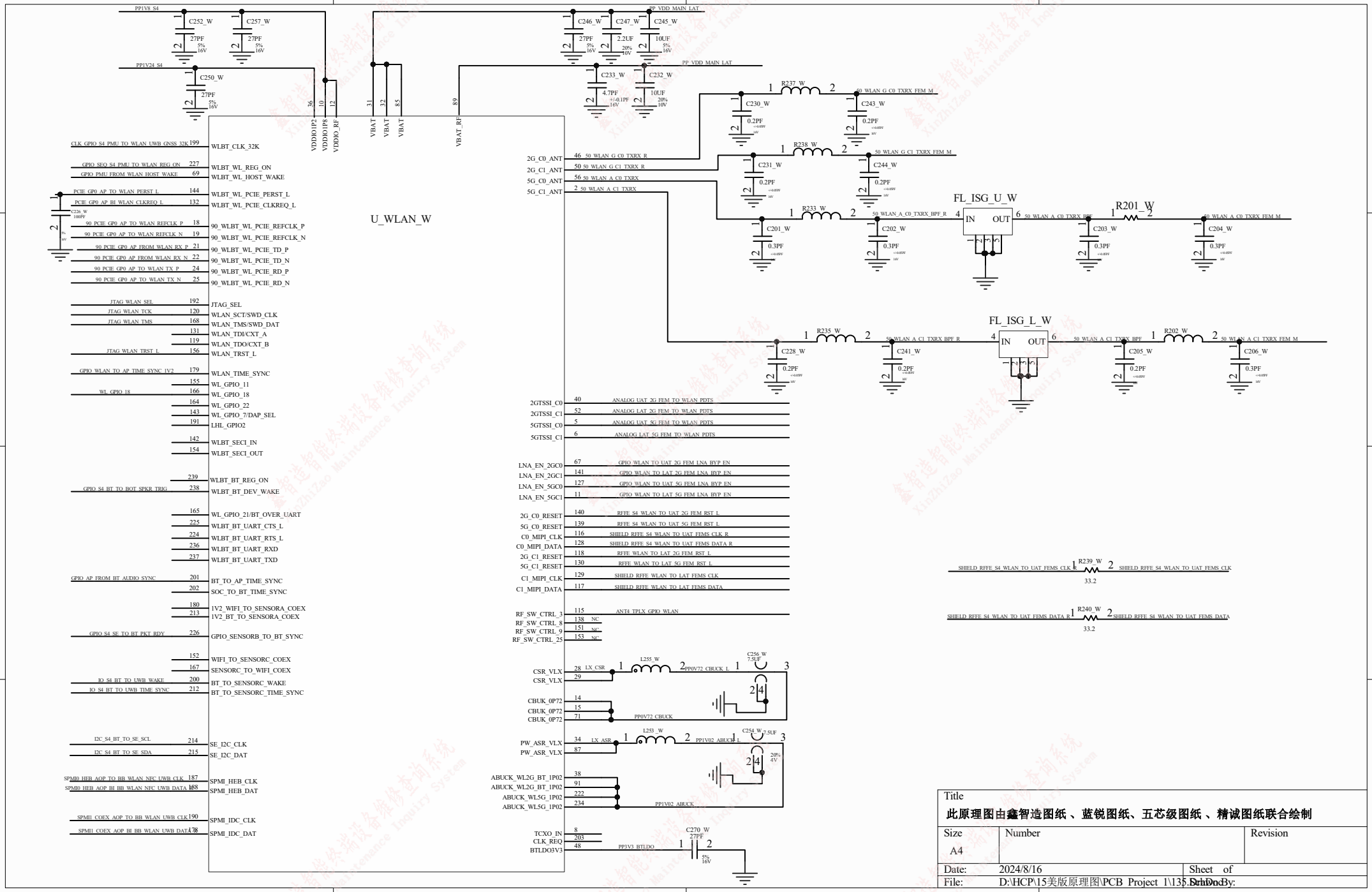


Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\132.SchDoc	Drawn By:	



鑫智造智能终端设备维修查询系统 Xinzhizao Maintenance Inquiry System

Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\133.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
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Date: 2024/8/16		Sheet of
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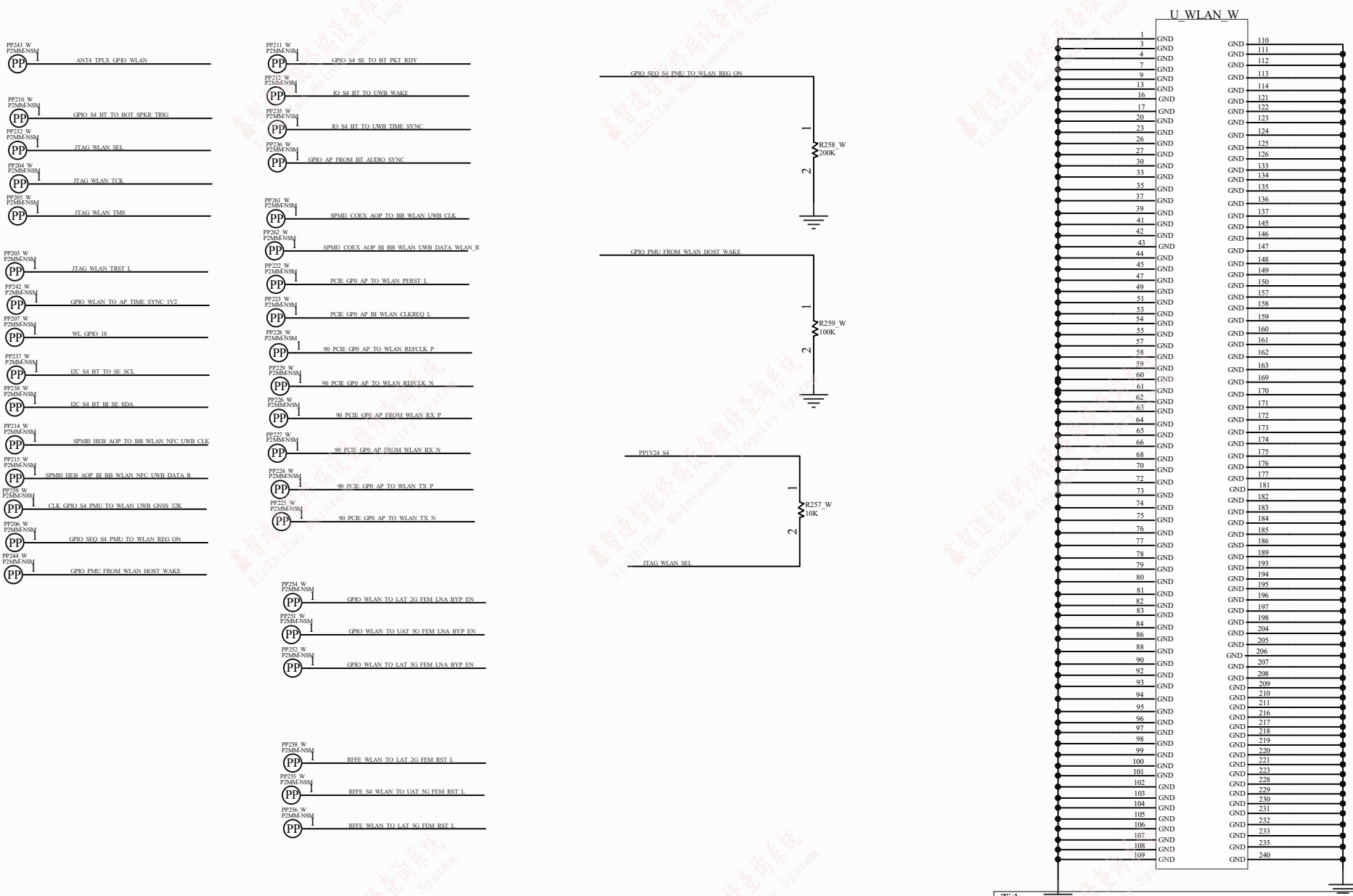

Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制
Size A4	Number
Revision	
Date: 2024/8/16	Sheet of
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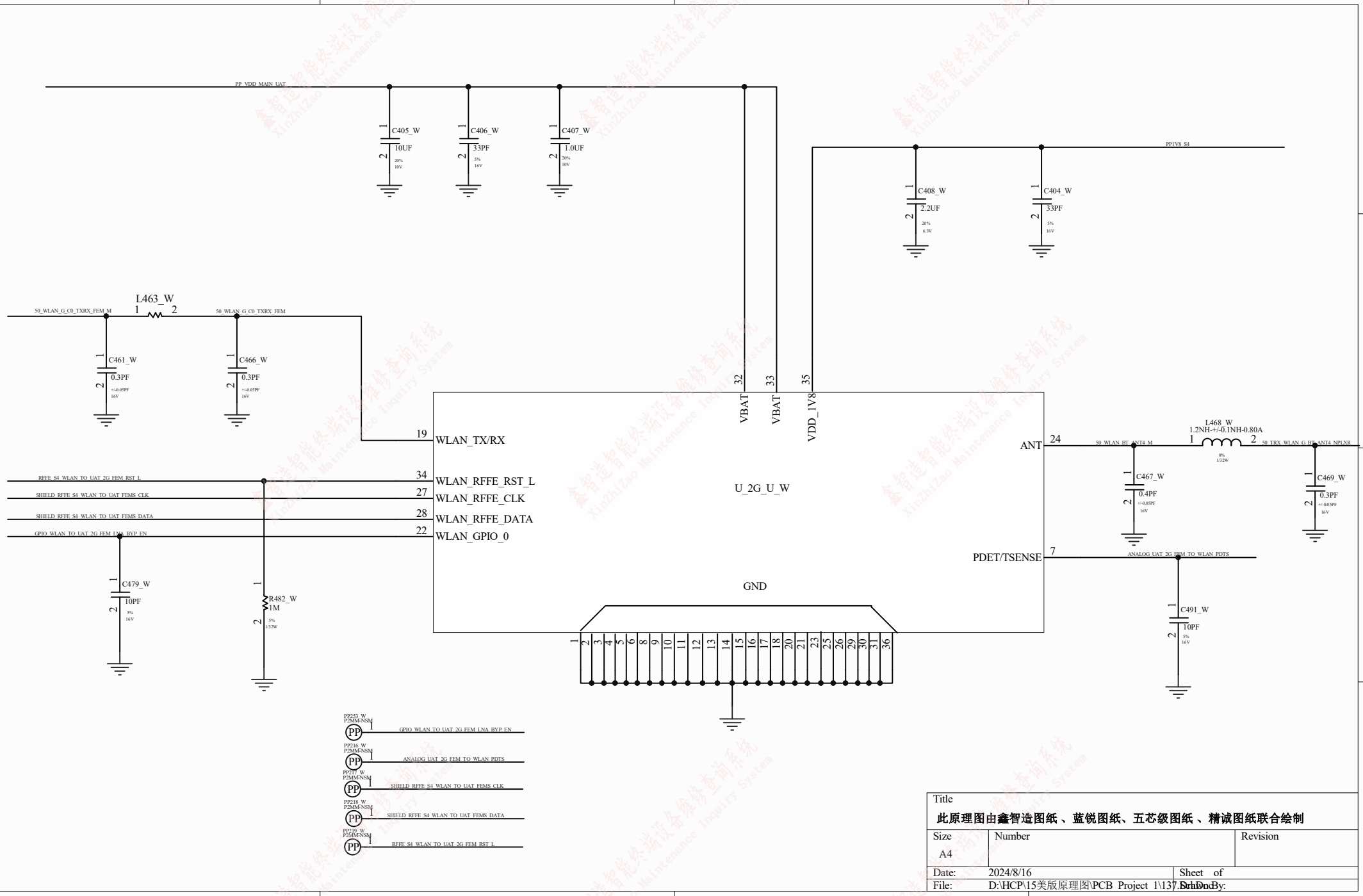

Title

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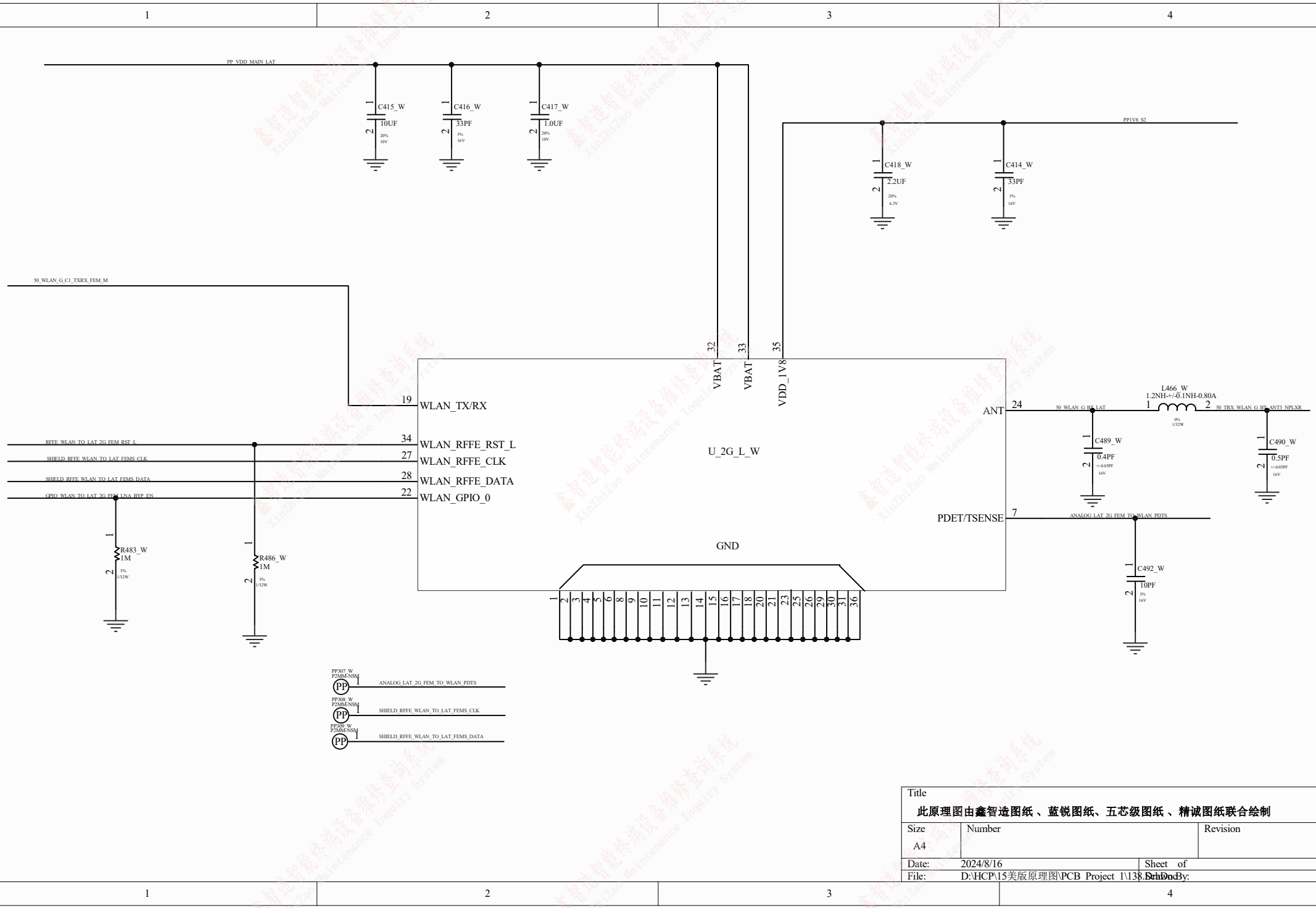
Size	Number	Revision
A4		

Date: 2024/8/16 Sheet of

File: D:\HCP\15美版原理图\PCB_Project_1\137.SchDoc Drawn By:



Title

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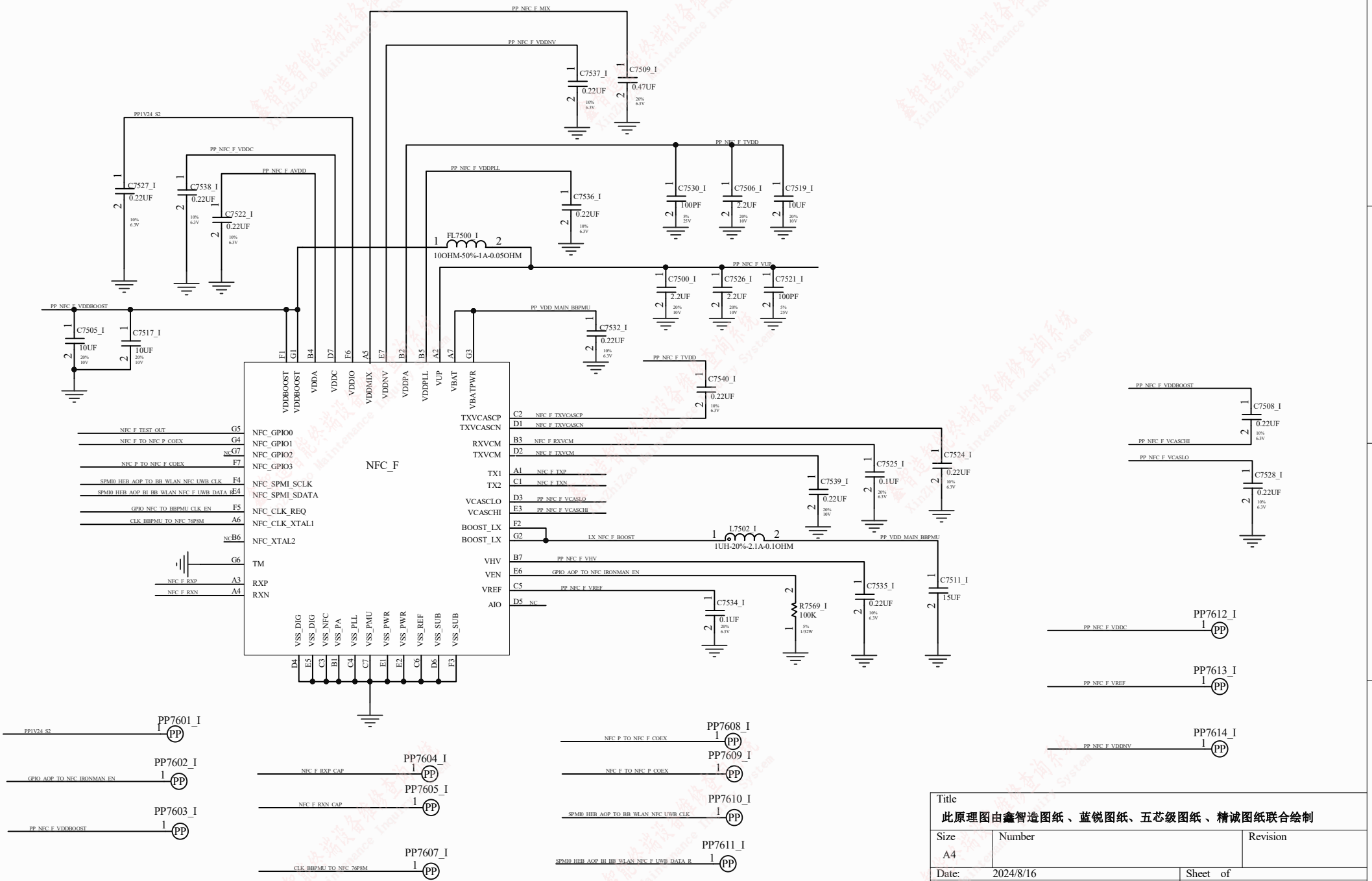
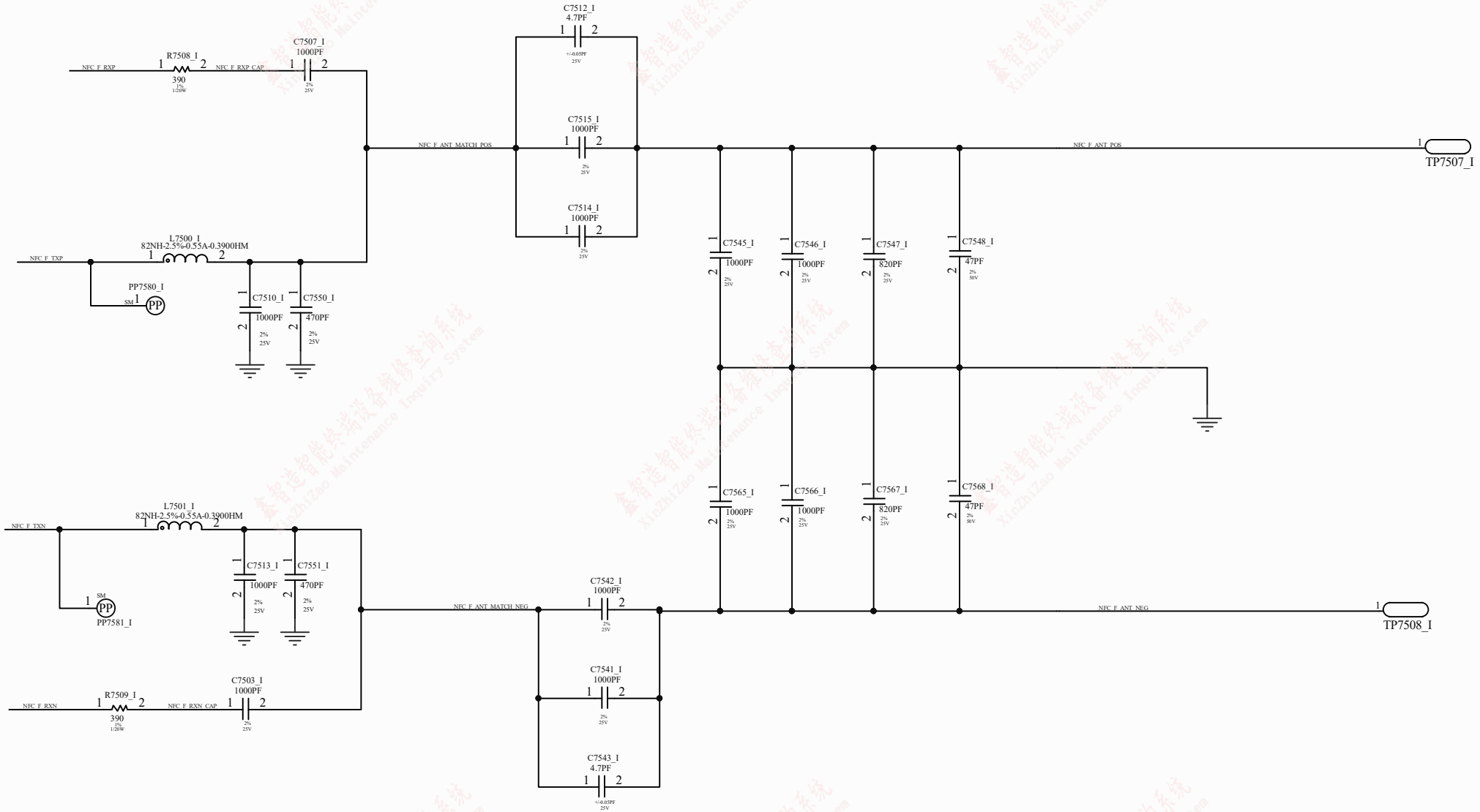
Size	Number	Revision
A4		

Date: 2024/8/16 Sheet of

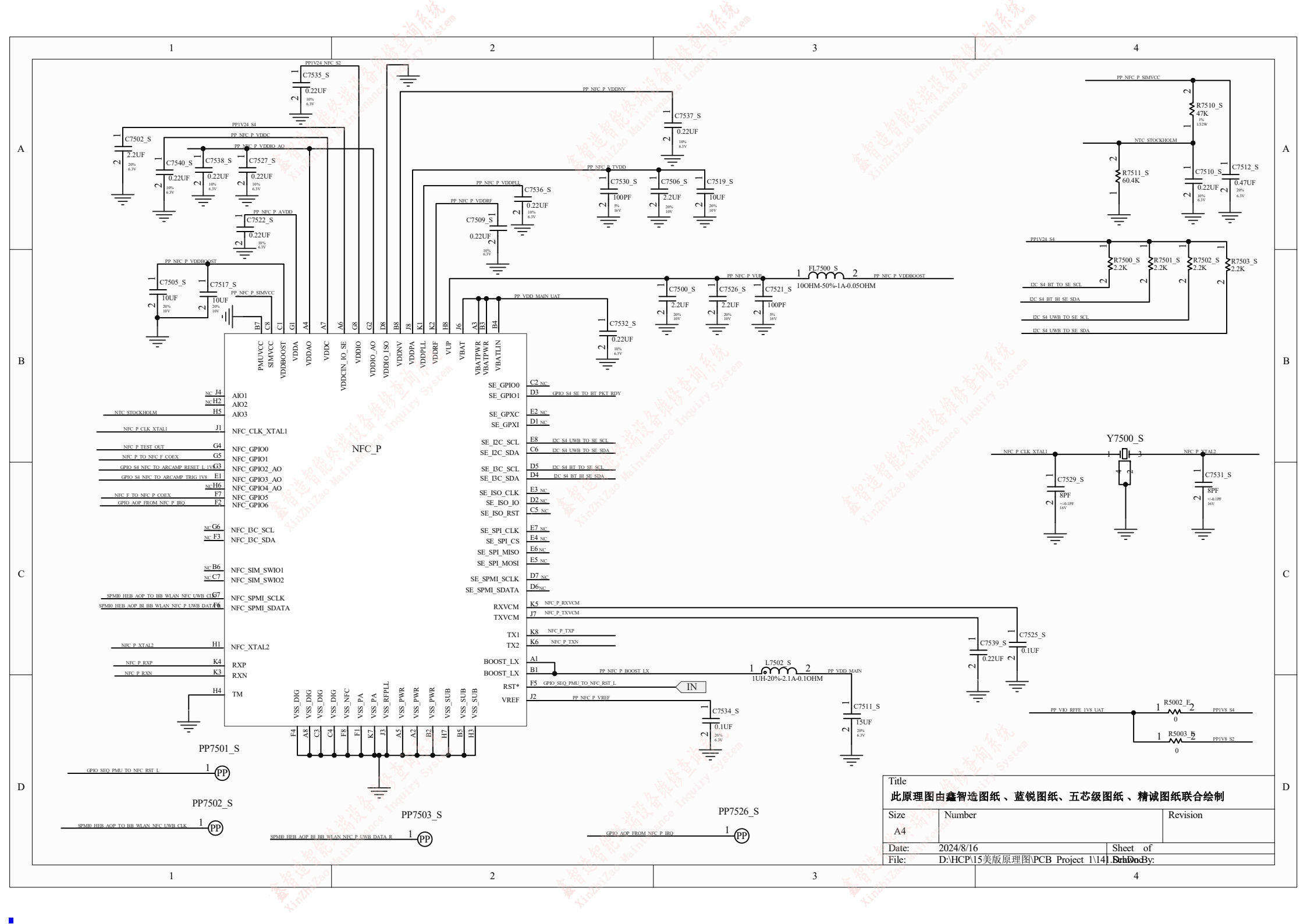
File: D:\HCP\15美版原理图\PCB_Project_1\138.SchDoc Drawn By:



Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB_Project_1\139.SchDoc	Drawn By:	



Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB Project 1\140.SchDoc	Drawn By:	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PP7501_S
PP7502_S
PP7503_S
PP7526_S
Y7500_S
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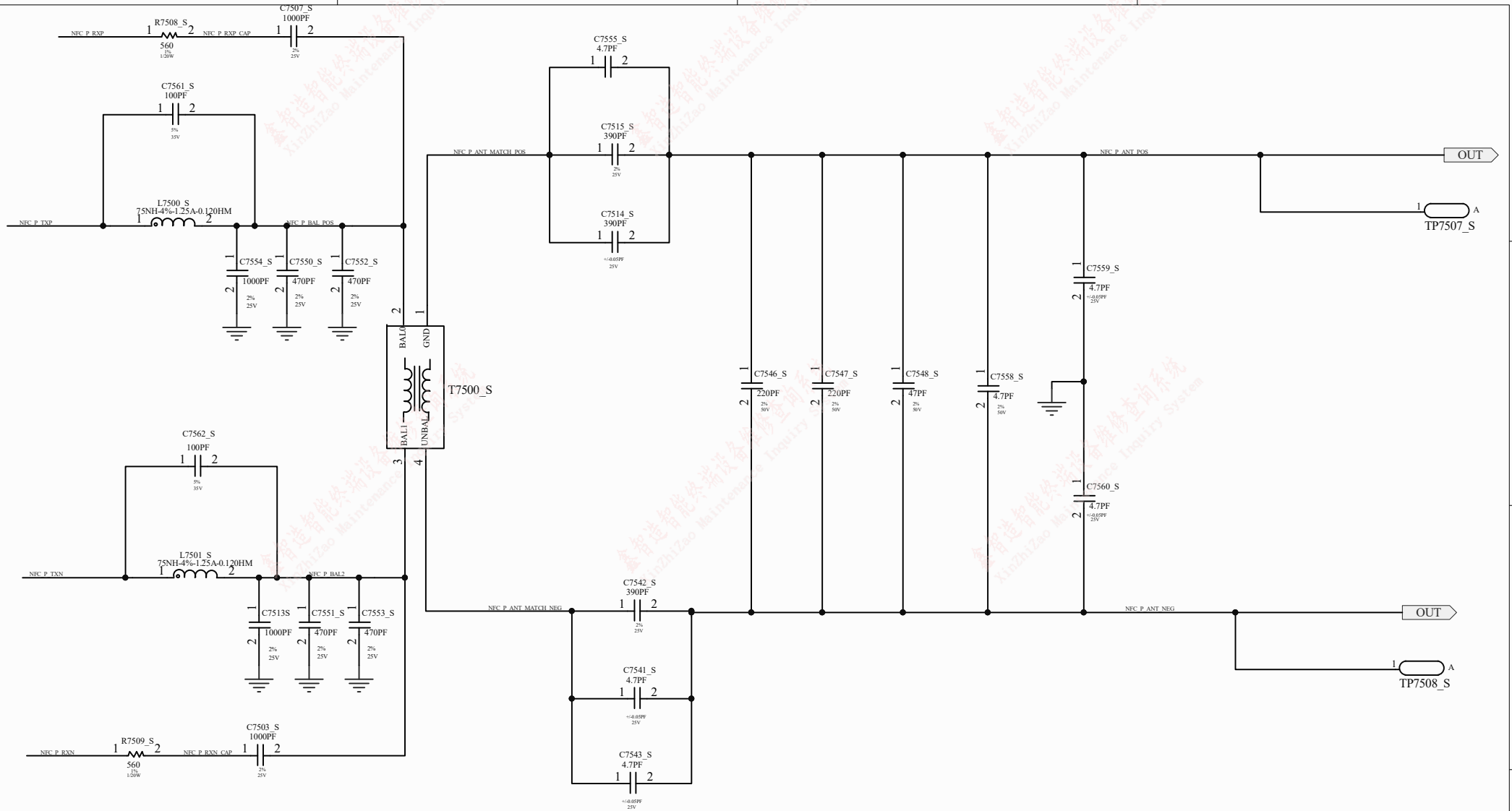
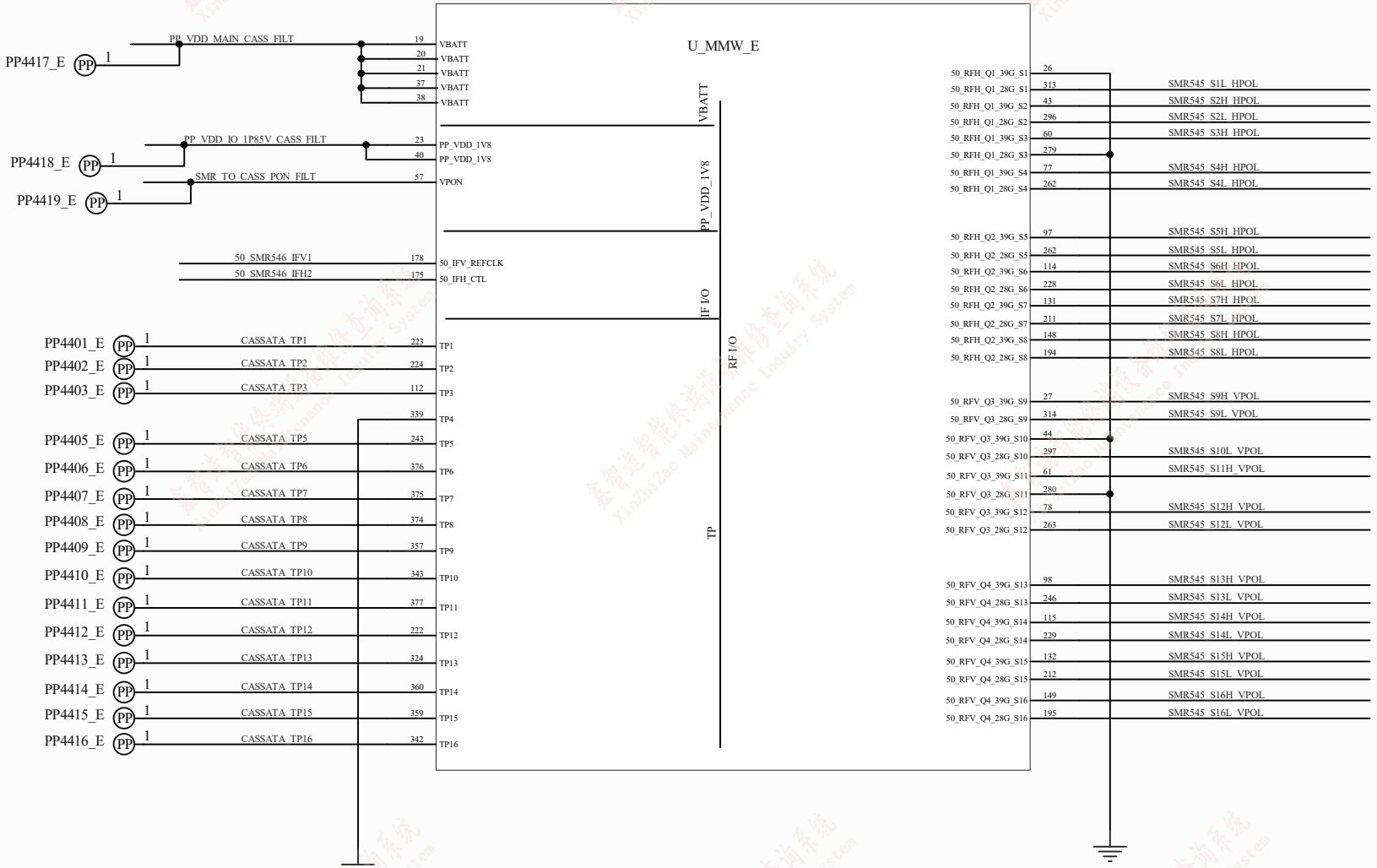
1UH-20%-2.1A-0.1OHM
FL7500_S
10OHM-50%-1A-0.05OHM
R5002_E
R5003_E
Title
此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制
Size
A4
Number
Revision
Date: 2024/8/16
Sheet of
File: D:\HCP\15美版原理图\PCB_Project_1\141...
Drawn By:



Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16		Sheet of
File: D:\HCP\15美版原理图\PCB_Project_1\142.SchDoc		Drawn By:



Title
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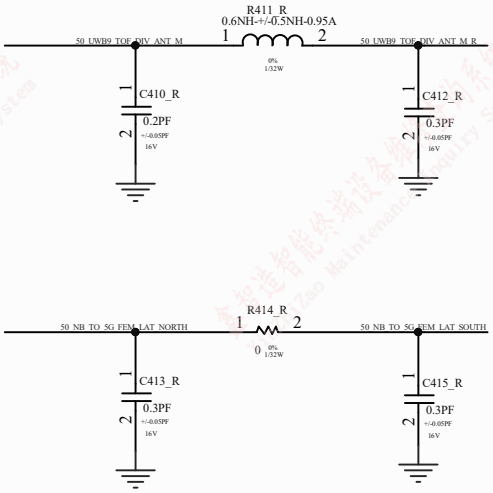
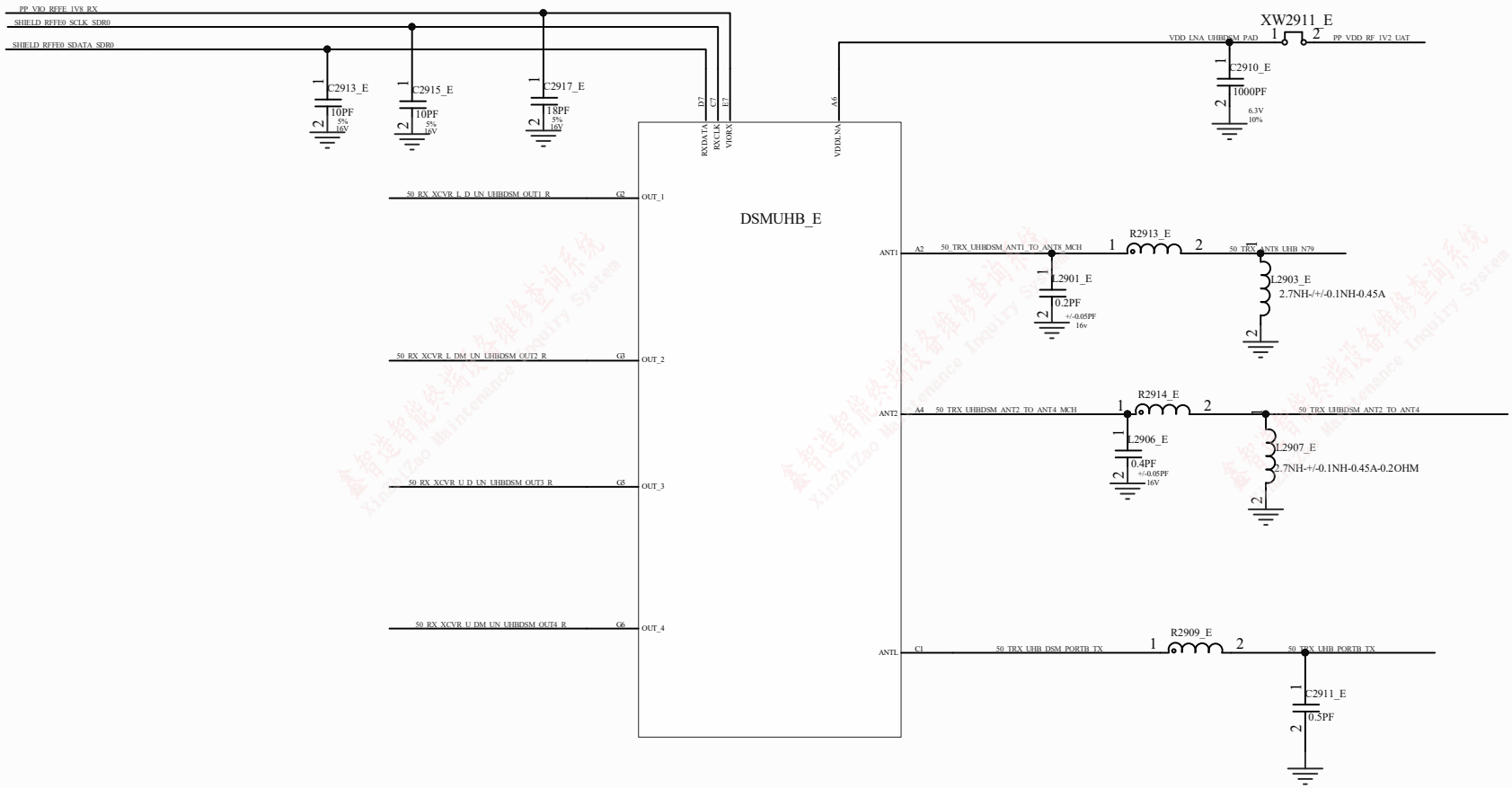
Size	Number	Revision
A4		

Date: 2024/8/16 Sheet of

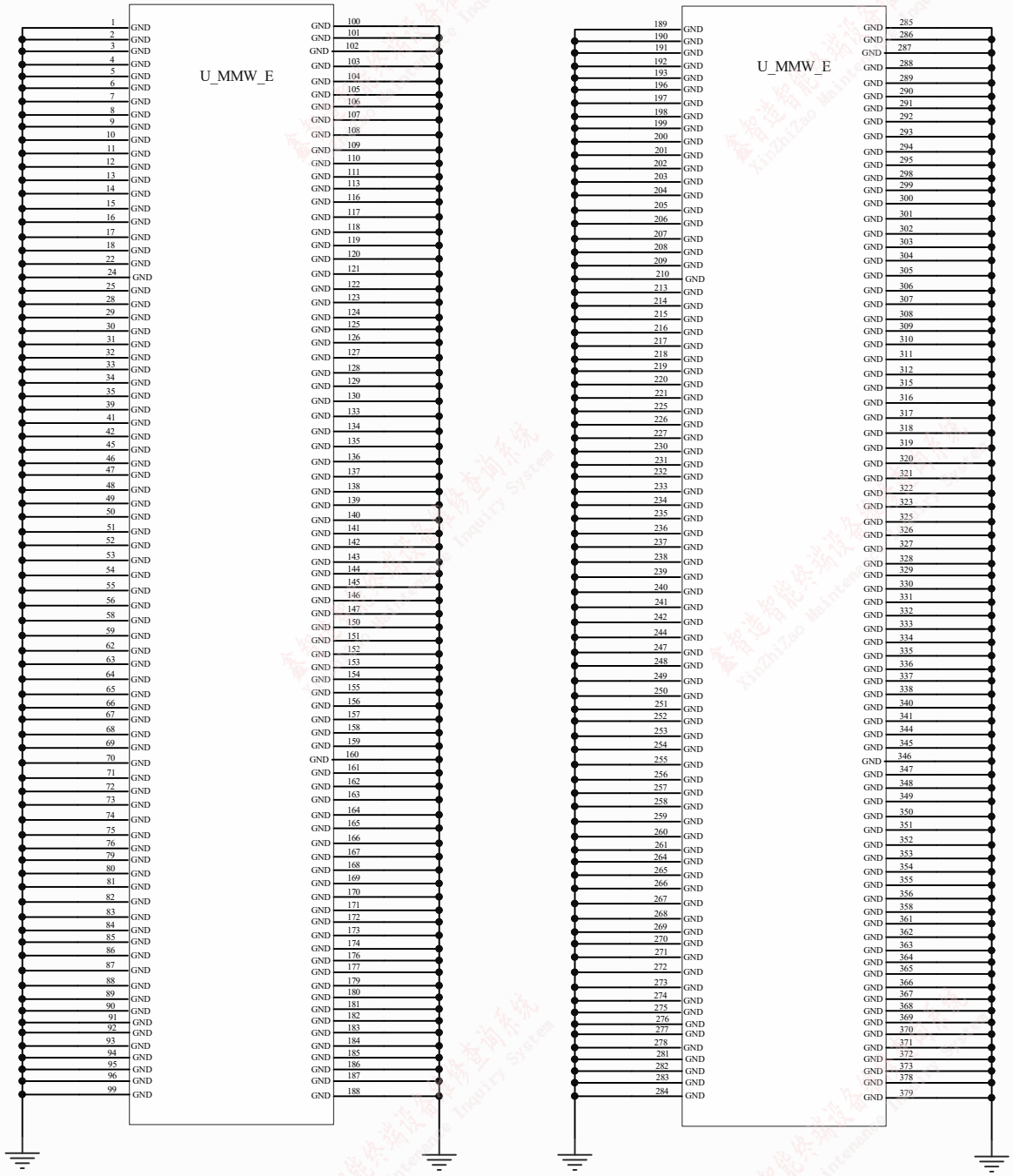
File: D:\HCP\15美版原理图\PCB Project 1\146.SchDoc Drawn By:

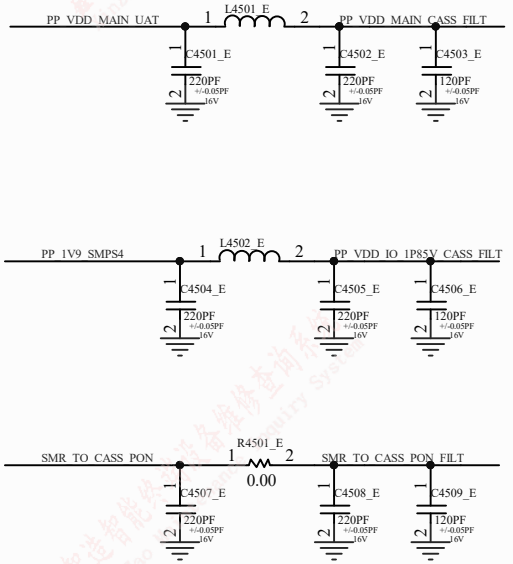


Title			
Size A4	Number		Revision
Date:	2024/8/16	Sheet of	
File:	D:\HCP\15美版原理图\PCB Project 1\144.SchDoc	Drawn By:	

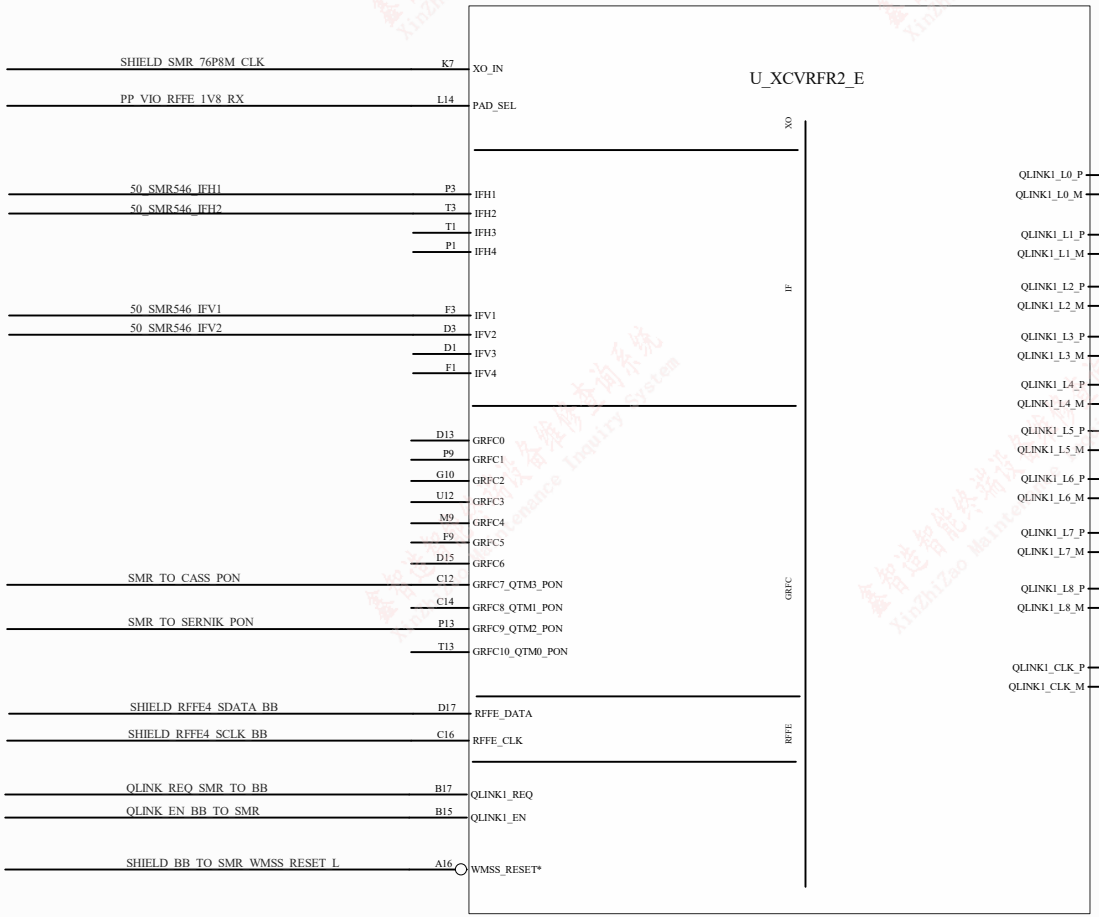


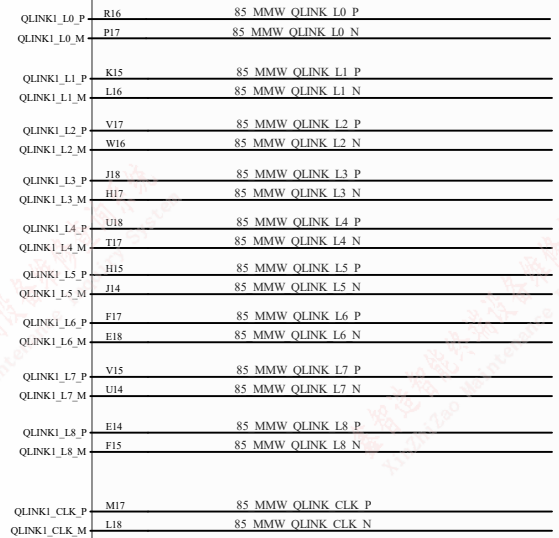
Title		
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB_Project_1\145.SchDoc	Drawn By:	

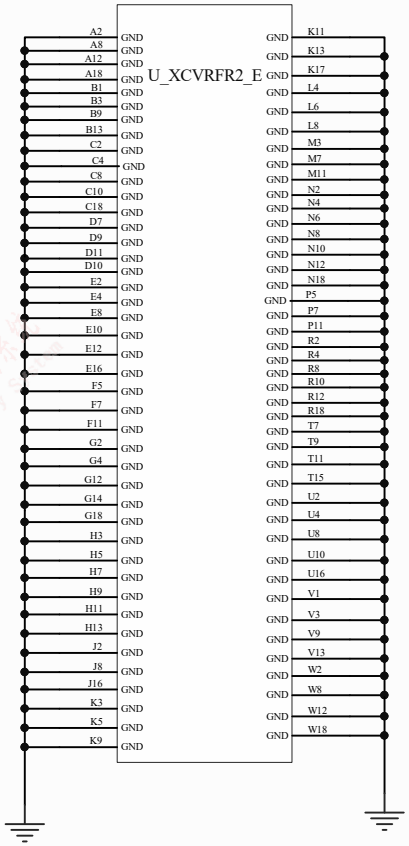




Title	此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16	Sheet of	
File: D:\HCP\15美版原理图\PCB_Project_1\147.SchDoc	Drawn By:	





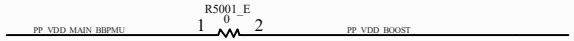


Title

此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制

Size	Number	Revision
A4		

Date:	2024/8/16	Sheet of	
File:	D:\HCP\15美版原理图\PCB Project 1\148.SchDoc	Drawn By:	



鑫智造智能终端设备维修查询系统 Xinzhizao Maintenance Inquiry System

Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制	
Size A4	Number	Revision
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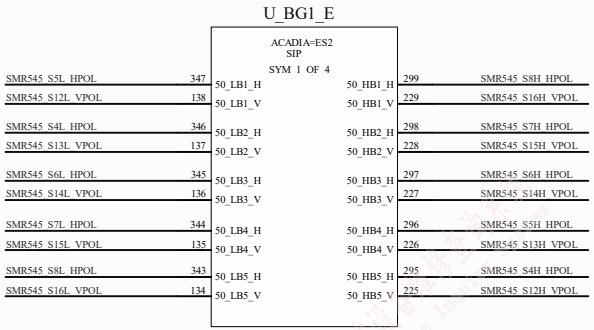
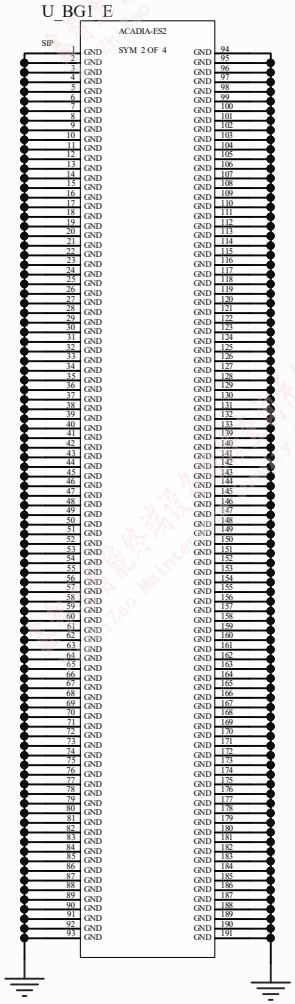
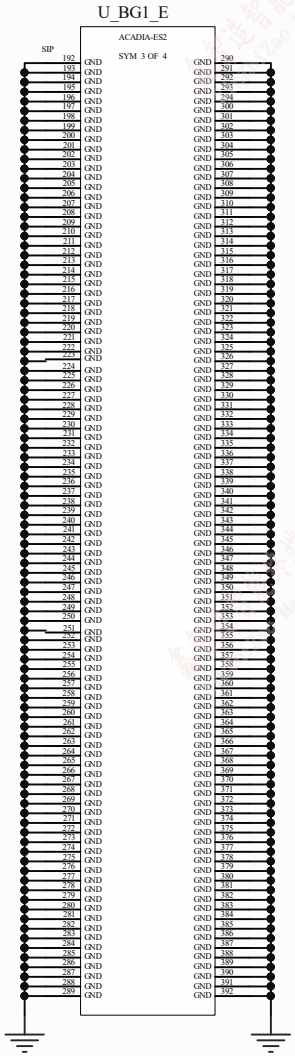
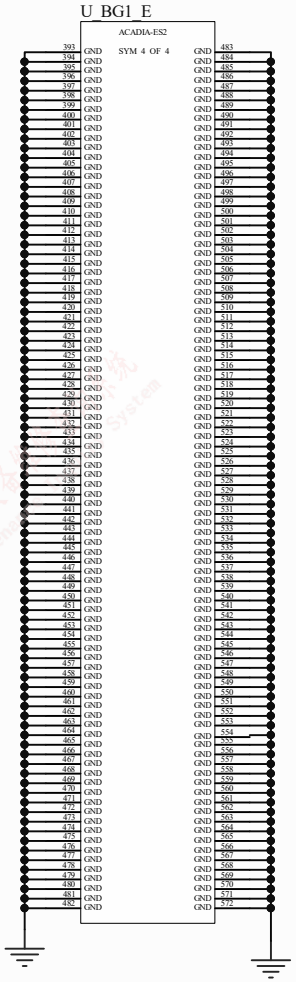
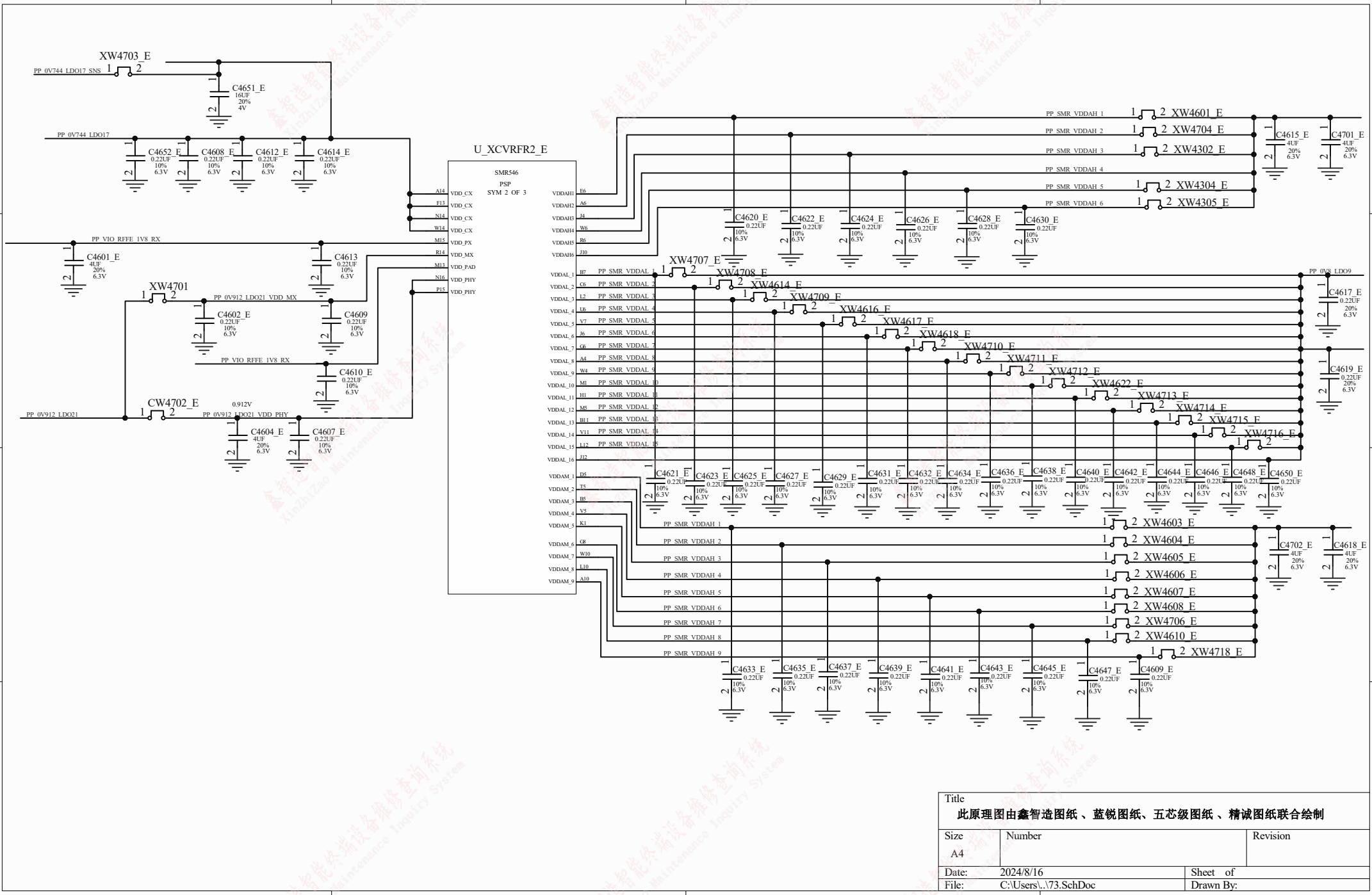








Title: 此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制		
Size: A4	Number	Revision
Date: 2024/8/16		Sheet of
File: C:\Users\..\72.SchDoc		Drawn By:



Title	此原理图由鑫智造图纸 、蓝锐图纸、五芯级图纸 、精诚图纸联合绘制	
Size A4	Number	Revision
Date: 2024/8/16		Sheet of
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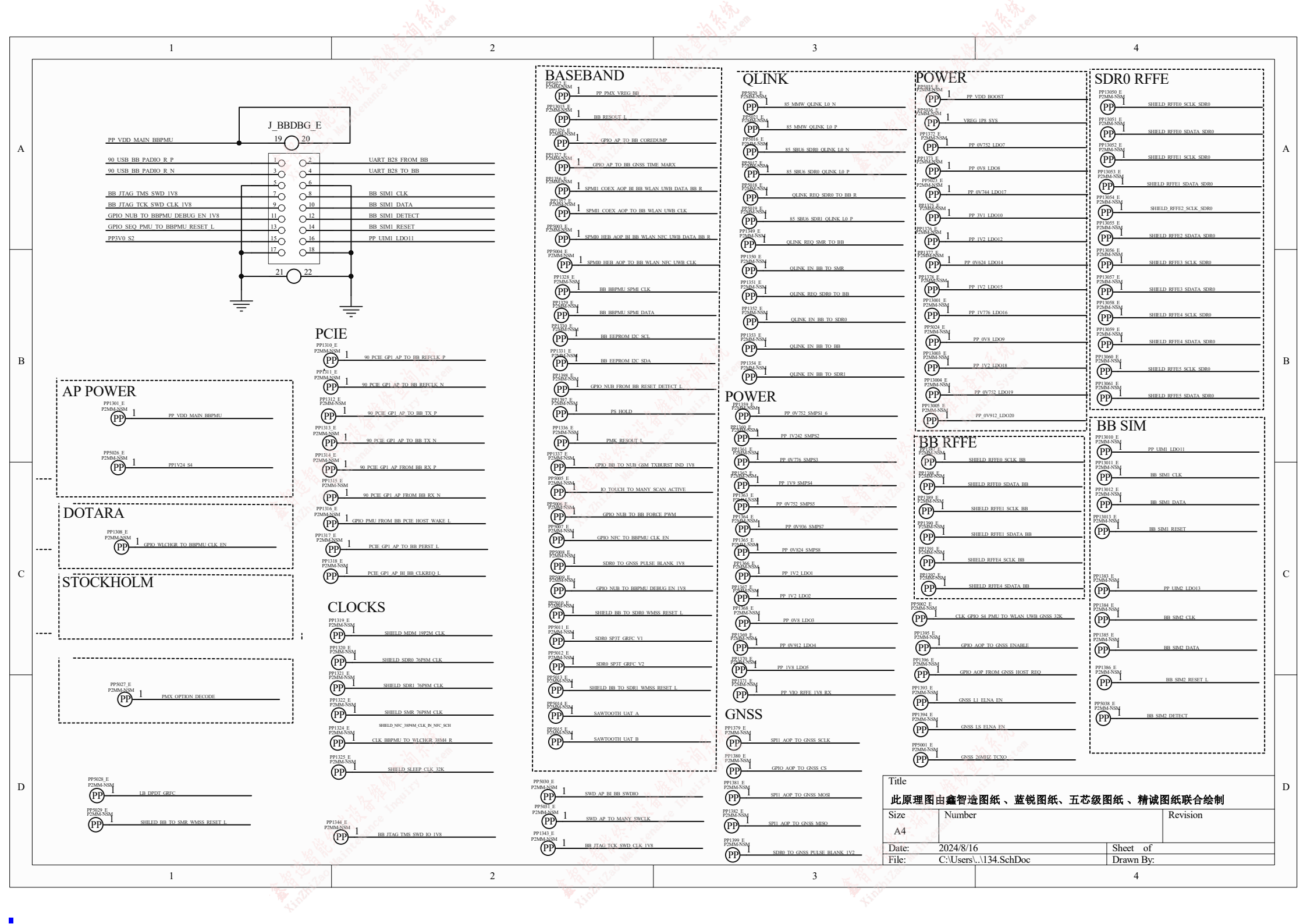
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90_USB_BB_PADIO_R_N
BB_JTAG_TMS_SWD_1V8
BB_JTAG_TCK_SWD_CLK_1V8
GPIO_NUB_TO_BBPMU_DEBUG_EN_1V8
GPIO_SEQ_PMU_TO_BBPMU_RESET_L
PP3V0_S2
UART_B28_FROM_BB
UART_B28_TO_BB
BB_SIM1_CLK
BB_SIM1_DATA
BB_SIM1_DETECT
BB_SIM1_RESET
PP_UIM1_LDO11
AP POWER
DOTARA
STOCKHOLM
PCIE
CLOCKS
BASEBAND
QLINK
POWER
GNSS
SDR0 RFFE
BB SIM
BB RFFE
Title
此原理图由鑫智造图纸、蓝锐图纸、五芯级图纸、精诚图纸联合绘制
Size
A4
Number
Revision
Date: 2024/8/16
File: C:\Users\..\134.SchDoc
Sheet of
Drawn By: