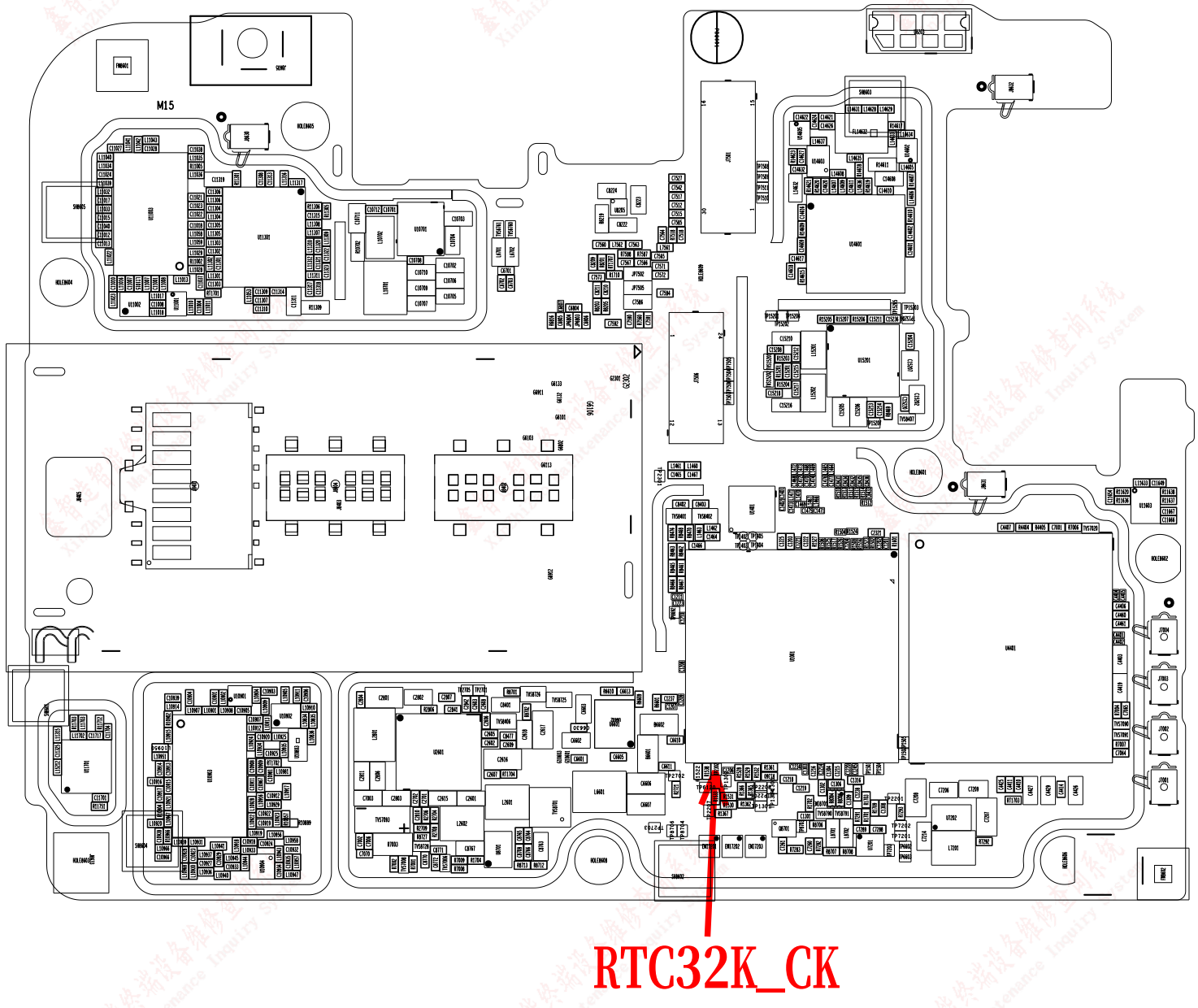
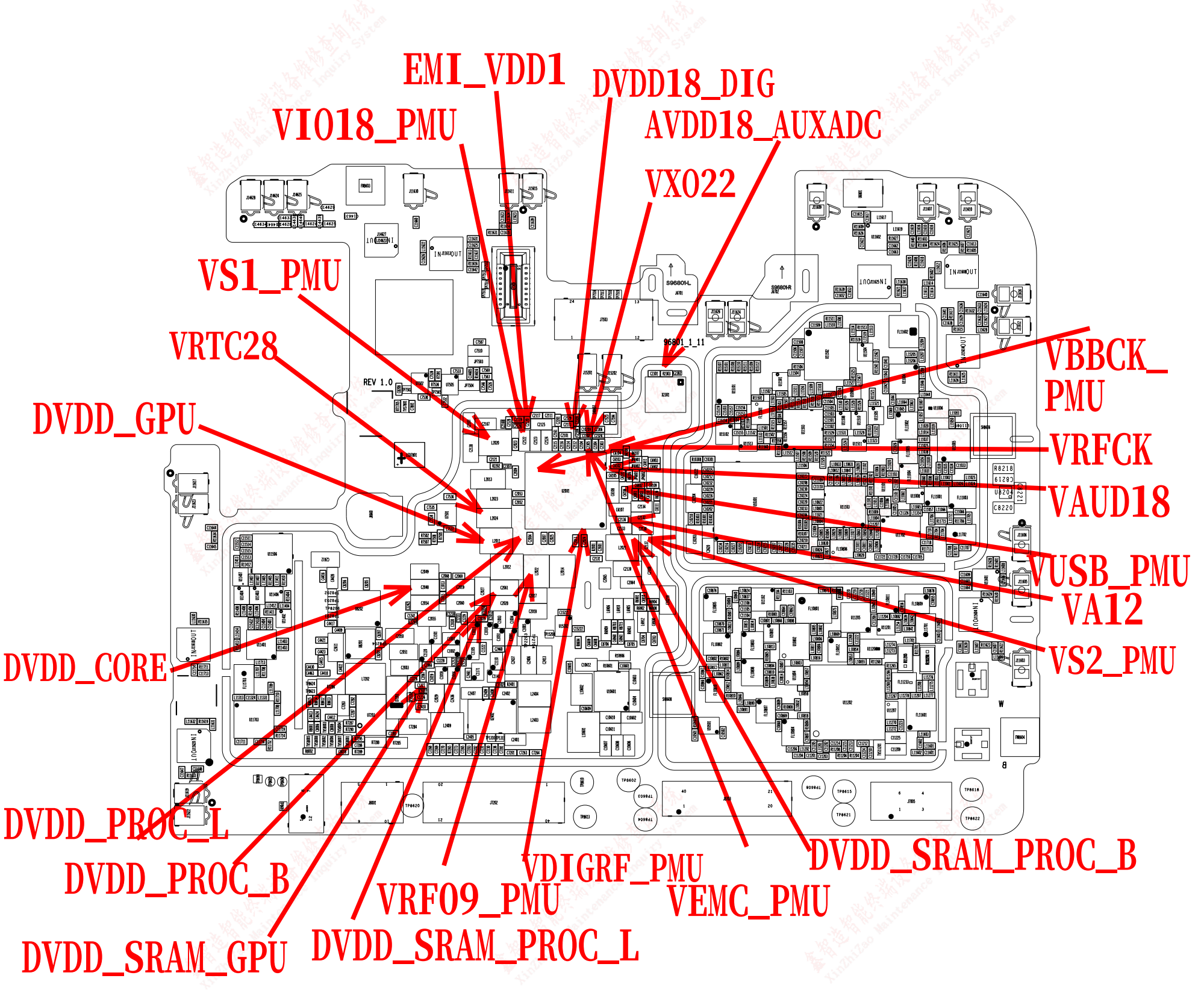

M15
RTC32K_CK


EMI_VDD1
DVDD18_DIG
VIO18_PMU
AVDD18_AUXADC
VXO22
VS1_PMU
VRTC28
VBBCK_
PMU
DVDD_GPU
VRFCK
VAUD18
VUSB_PMU
VA12
VS2_PMU
DVDD_CORE
DVDD_PROC_L
DVDD_PROC_B
VDIGRF_PMU
DVDD_SRAM_PROC_B
VRF09_PMU
VEMC_PMU
DVDD_SRAM_GPU
DVDD_SRAM_PROC_L

BB

RF

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DEPARTMENT: BB	DESIGNER: liufengjei	
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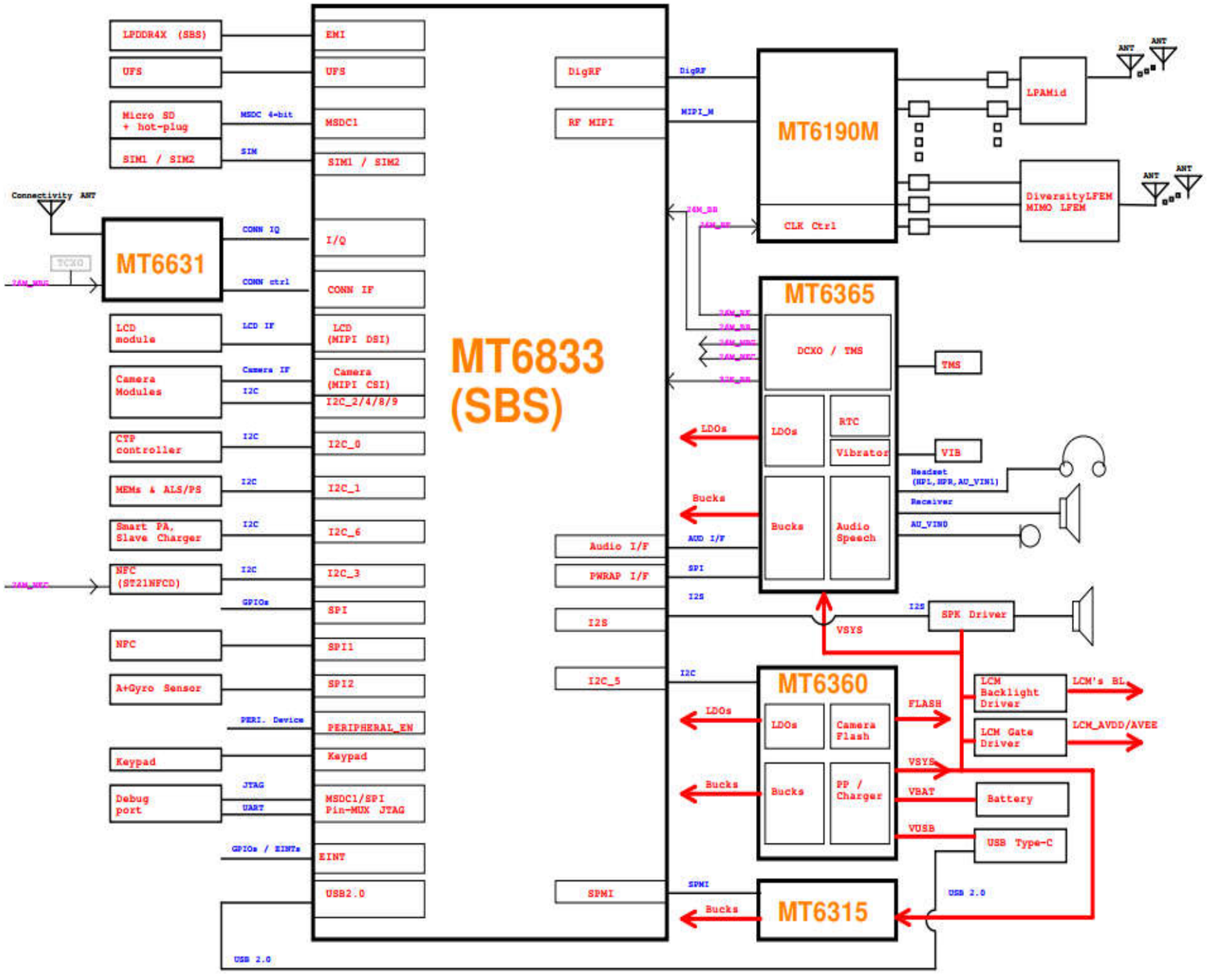
02_Block_Diagram



Title	002_Block_Diagram	REV: V10
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DEPARTMENT:	BB	DESIGNER: liufenglei
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03_I2C_ID_Overview

I2C	AP, SCP, SSPM	Function	I2C/I3C Spec.	I2C Slave Address (7-bit mode)
I2C-0			I2C	
I2C-1	SCP	M Sensor	I2C	MMC5603NJL I2C address: 0x0C (Read:0x61 Write:0x60)
		ALS+PS Sensor		AK09918C 0x46 I2C address: 0x46 (Read:0x19 Write:0x18)
I2C-2	AP	Main CAM **M	I2C	Hi1336： I2C address :0x1A (Read:0x41 Write:0x40) ； OV13B： I2C address :0x6C (Read:0x6D Write:0x6C) ； IMX258 I2C address: 0x50 (Read:0x21 Write:0x20) S5K3L6 I2C address: 0x50 (Read:0x21 Write:0x20)
I2C-3	AP	NFC	I2C	
		SAR		A96T346DFP I2C Address 0x20 (Read:0x41 Write:0x40)
I2C-4	AP	Front Camera	I2C	S5K4H7 I2C Address : (Read:0x5B Write:0x5A) Hi846 I2C Address：（Read:0x41 Write:0x40) GC8054 2C Address：（Read:0x6F Write:0x6E)
		Macro 2 M CAM		GC2375 I2C Address (Read:0X2F Write:0X2E) OV02A10 I2C Address (Read:0x7B Write:0x7A)
I2C-5	AP	MT6360	I2C	MT6360 PD's I2C address: 0X4E (Read:0x9D Write:0x9C) MT6360 PMIC's I2C address: 0x1A (Read:0x35 Write:0x34) MT6360 PMU's I2C address: 0x34 (Read:0x69 Write:0x68) MT6360 LDO's I2C address:0x64 (Read:0xC9 Write:0xC8)
I2C-6	AP	Smart PA	I2C	AW88264CSR Speaker AMP I2C Address: 0x34(Read:0x69 Write:0x68)
		LCM Gate Driver		SM5109 I2C address:0X3E (Read:0x7D Write:0x7C)
		LCM BACKLINGHT		AW99703 I2C address:0x36 (Read:0x6D Write:0x6C)
I2C-7	AP		I2C	TBD
I2C-8	AP	Depth 2 M CAM	I2C	OV02B1B I2C address: (Read:0x78 Write:0x79)
				GC2375B I2C address: (Read:0x2F Write:0x2E)
I2C-9	AP		I2C	

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

Title	003_I2C_ID_Overview		REV: V10
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04_Change_Notice

Date	Version	Page	Change notice
20120.10.15			Changed from 5G-C HW
20120.10.16			1st release

Title	004_Change_Notice		REV: V10
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DEPARTMENT:	BB	DESIGNER:	liufenglei
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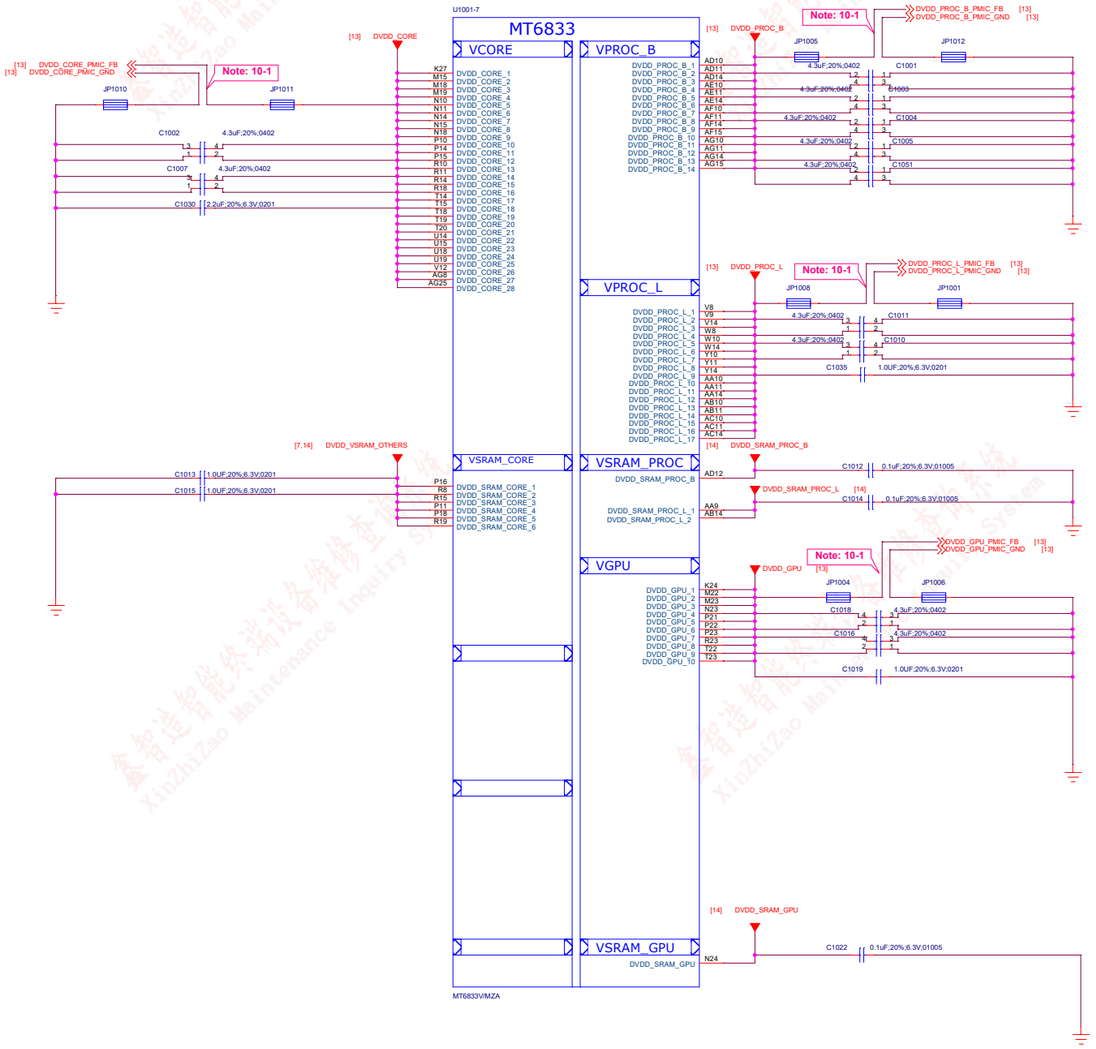
10_BB_POWER_PDN



Schematic design notice of "10_BB_POWER_PDN" page.

Note 10-1: Differential pair of PMIC remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Title: 010_BB_POWER_PDN		REV: V10
DOCUMENT NO.: 98812_1_12M13_20210317_2112		Size: D
DEPARTMENT: BB	DESIGNER: liufengjei	
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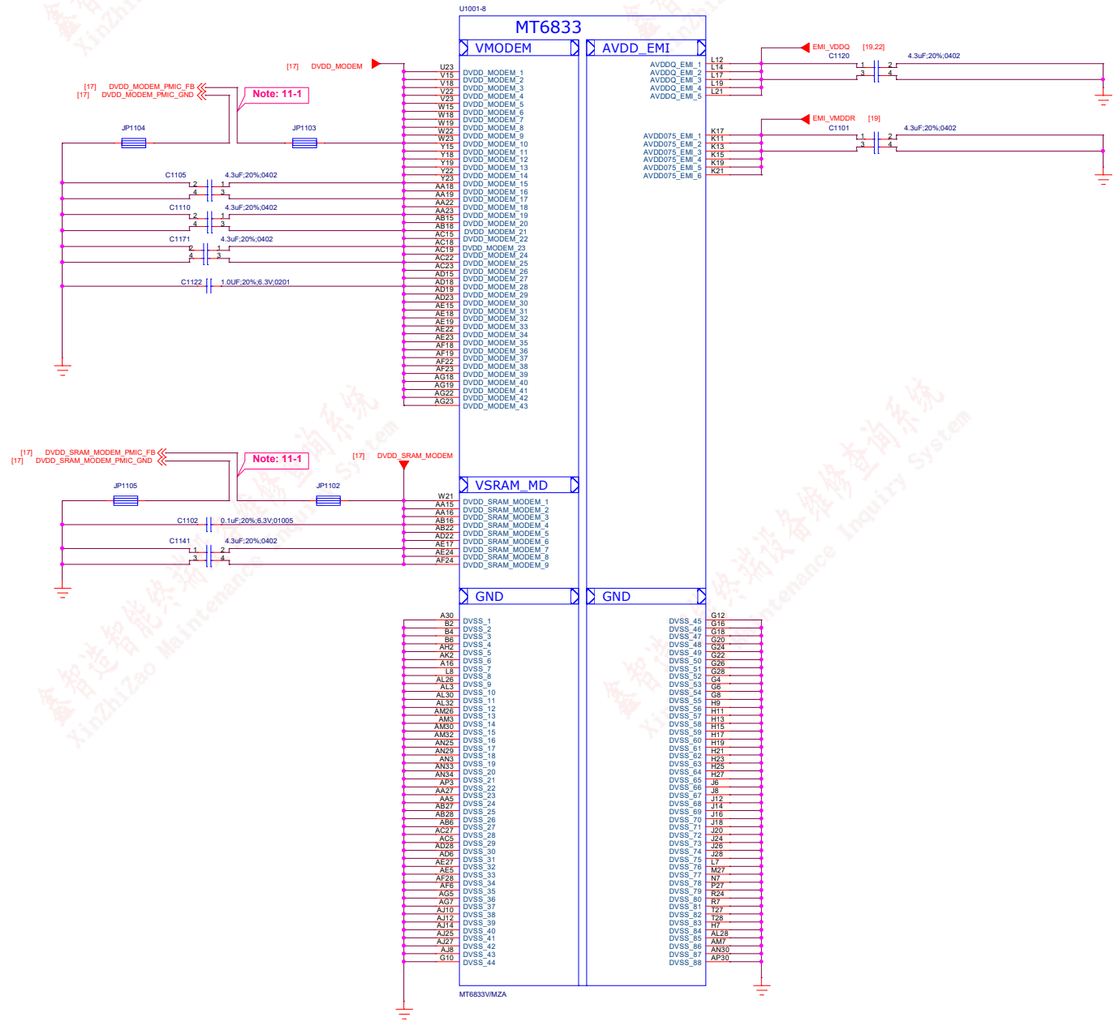
11_BB_POWER_PDN



Schematic design notice of "11_BB_POWER_PDN" page.

Note 11-1: Differential pair of PMIC remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Title	011_BB_POWER_PDN		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	BB	DESIGNER:	liufenglei
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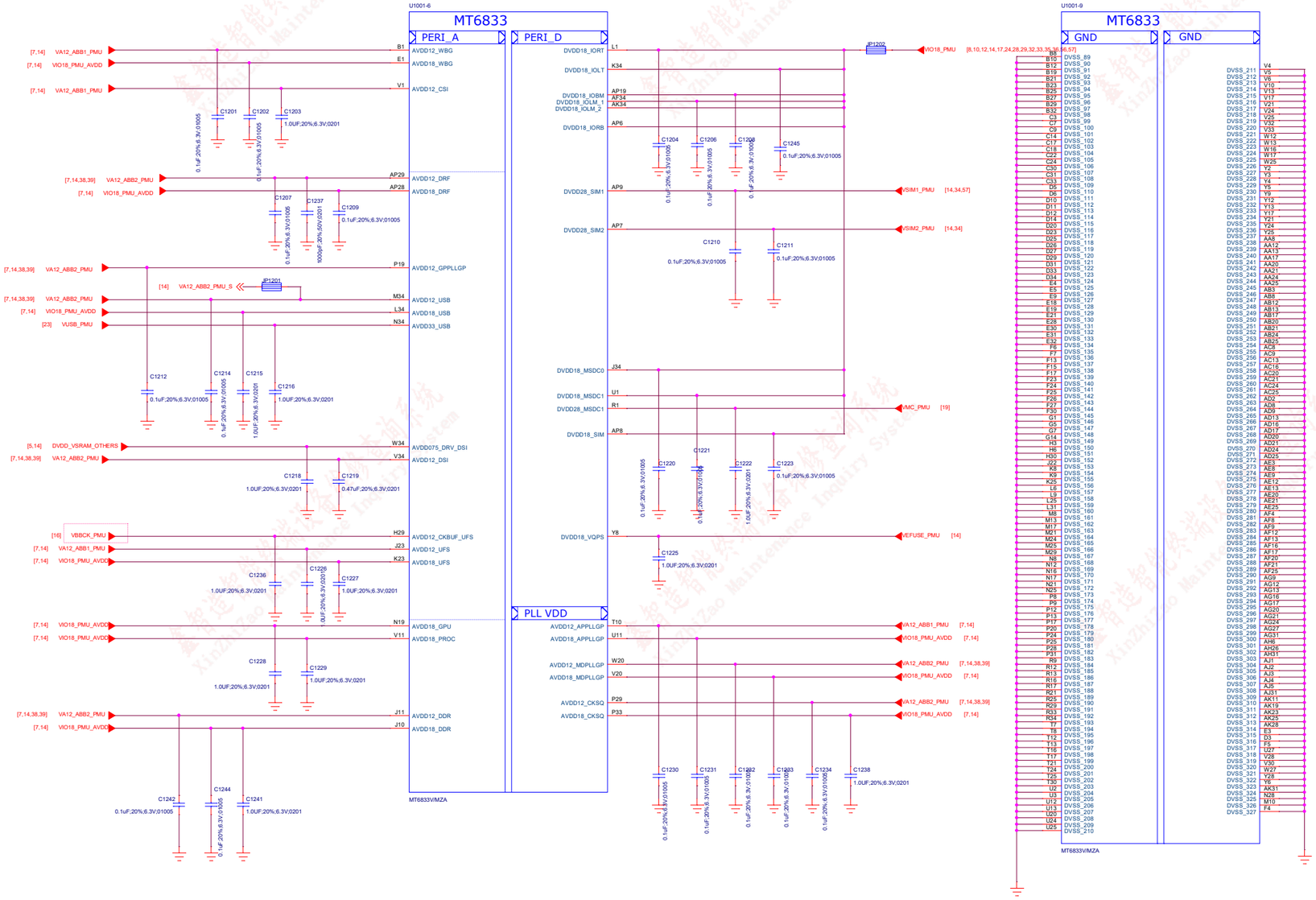
12_BB_POWER_IO



Title	012_BB_POWER_IO	REV: V10	
DOCUMENT NO.:	98812_1_12M13_20210317_2112	Size D	
DEPARTMENT:	BB	DESIGNER: liufengjei	
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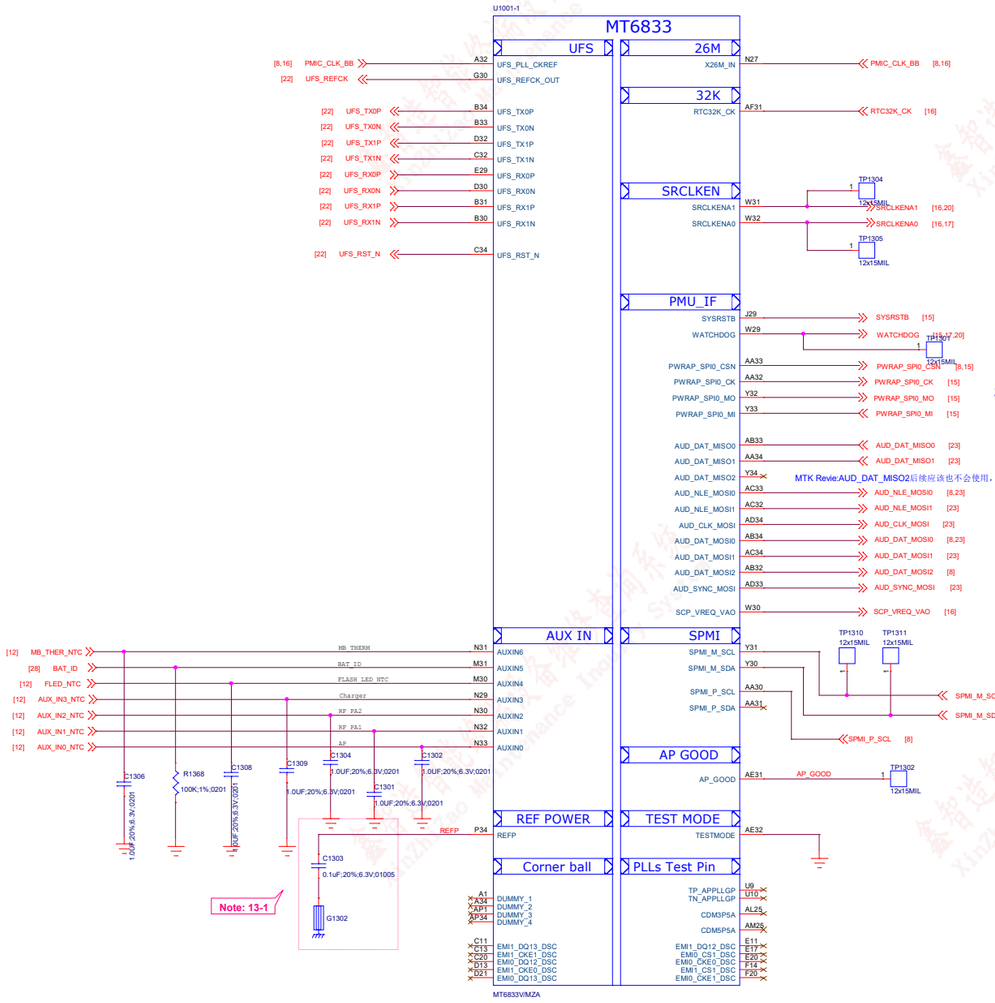
13_BB_1



Note 13-6: "AUD_DAT_MISO1" is trapping pin to select VEMC Voltage.

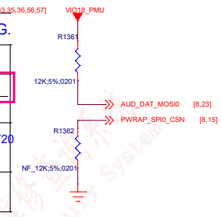
AUD_DAT_MISO1	VEMC Voltage
L (Default)	VEMC=3.0V
H (by external PU)	VEMC=2.5V

Schematic design notice:

Note 13-1: The load cap. have to be placed as close to REFP ball as possible.

Note 13-2: "PWRAP_SPI0_CSN" and "AUD_DAT_MOS0"I pin features in trapping pin to enable JTAG.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP JTAG	IO JTAG
H (Default)	L (Default)	N/A	N/A
H	H (by external PU)	SPI0+EINT8	N/A
L (by external PD)	L	SPI0+EINT8	EINT16/EINT17/EINT18/EINT19/EINT20 EINT21/EINT22/I2C7
L (by external PD)	H (by external PU)	MSDC1_CLK, MSDC1_CMD, MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2	N/A



Note 13-3: "AUD_NLE_MOSI1" features in trapping pin to enable JTAG over USB 2.0 port.

AUD_NLE_MOSI1	USB JTAG
L (Default)	USB 2.0
H (by external PU)	DP/DM output JTAG

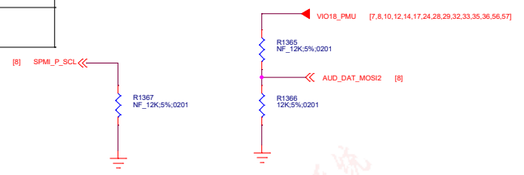
Note 13-4: "AUD_SYNC_MOSI" and "AUD_NLE_MOSI0" pin features in trapping pin to booting (eMMC/UFS/SPI NOR).

AUD_SYNC_MOSI	AUD_NLE_MOSI0	Storage Booting
L (Default)	L (Default)	Only UFS boot
L	H (by external PU)	Only eMMC boot
H (by external PU)	L	Reserved
H (by external PU)	H (by external PU)	Reserved

Note 13-5: "AUD_DAT_MOSI1" and "AUD_DAT_MOSI2" pin features in trapping pin to enable DDR.

AUD_DAT_MOSI1	AUD_DAT_MOSI2	SPMI_P_SCL	DDR
L (Default)	L (Default)	L (Default)	LP4x-MCP-4266Mbps
L	H (by external PU)	L (Default)	LP4x-Discrete-4266Mbps
H (by external PU)	L	L (Default)	Reserved
H (by external PU)	H (by external PU)	L (Default)	Reserved

Note : SPMI_P_SCL for DDR
4266Mbps/3733Mbps Co-load,
'L' = 4266Mbps,
'H(by external PU)' = 3733Mbps



Title	013_BB_1_ADC/CLK		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	BB	DESIGNER:	liufenglei
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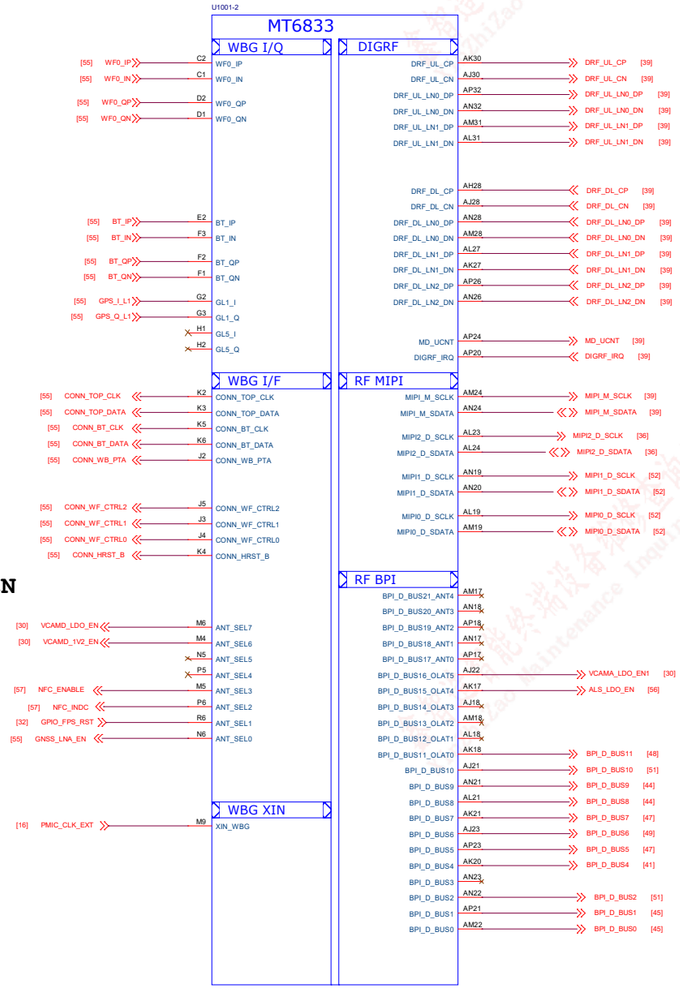
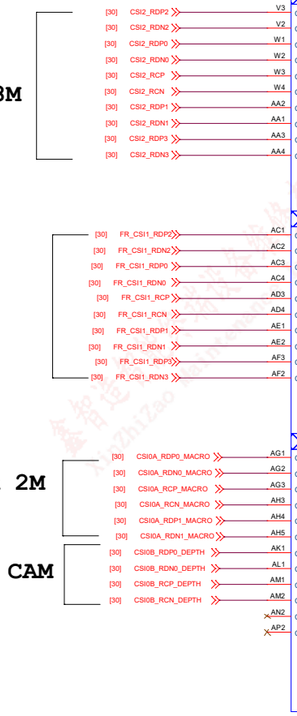
14_BB_2



NA WCN

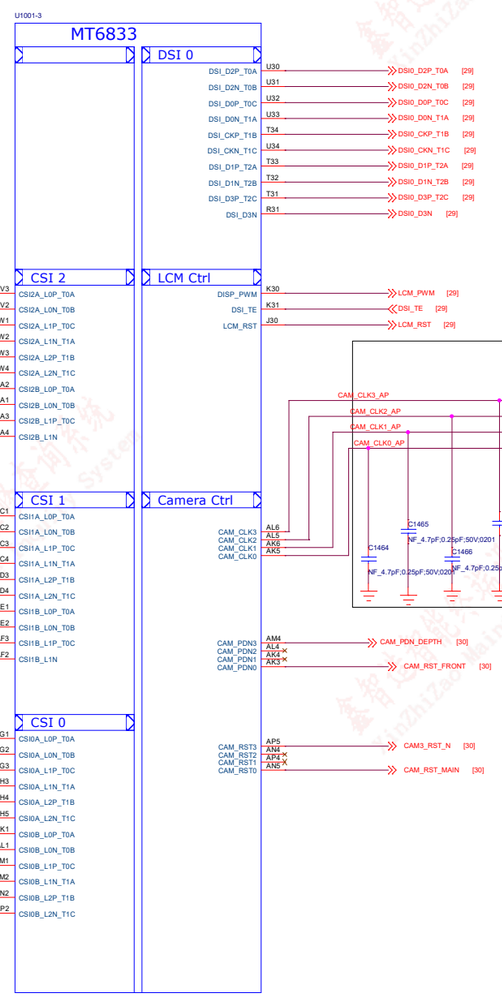
Main Cam 48M



Front

Marco Cam 2M

Depth CAM



RF BOM

close the SoC

Title	014_BB_2_MIPI		REV: V10
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DEPARTMENT:	BB	DESIGNER:	liufenglei
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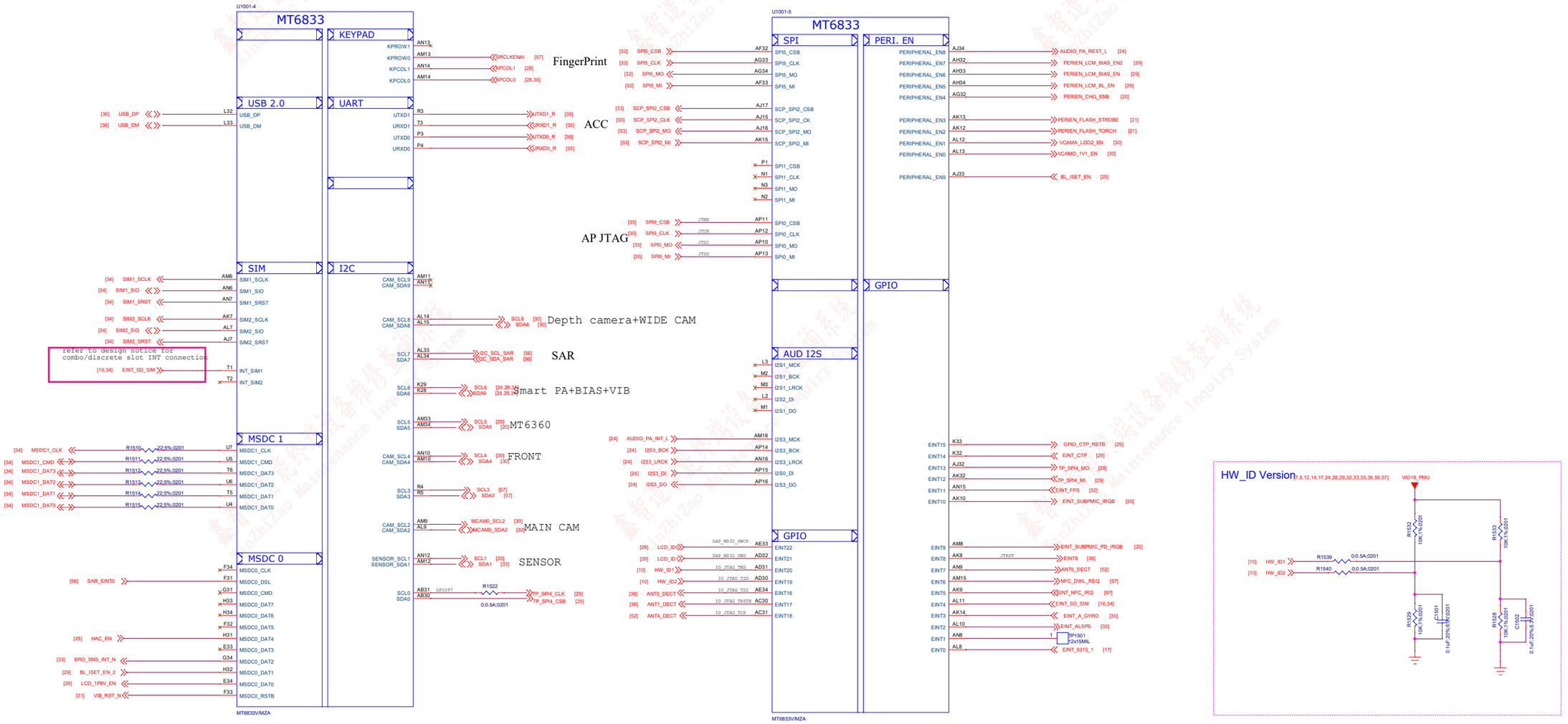
15_BB_3



Title	015_BB_3_MISC		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	BB	DESIGNER:	liufengjel
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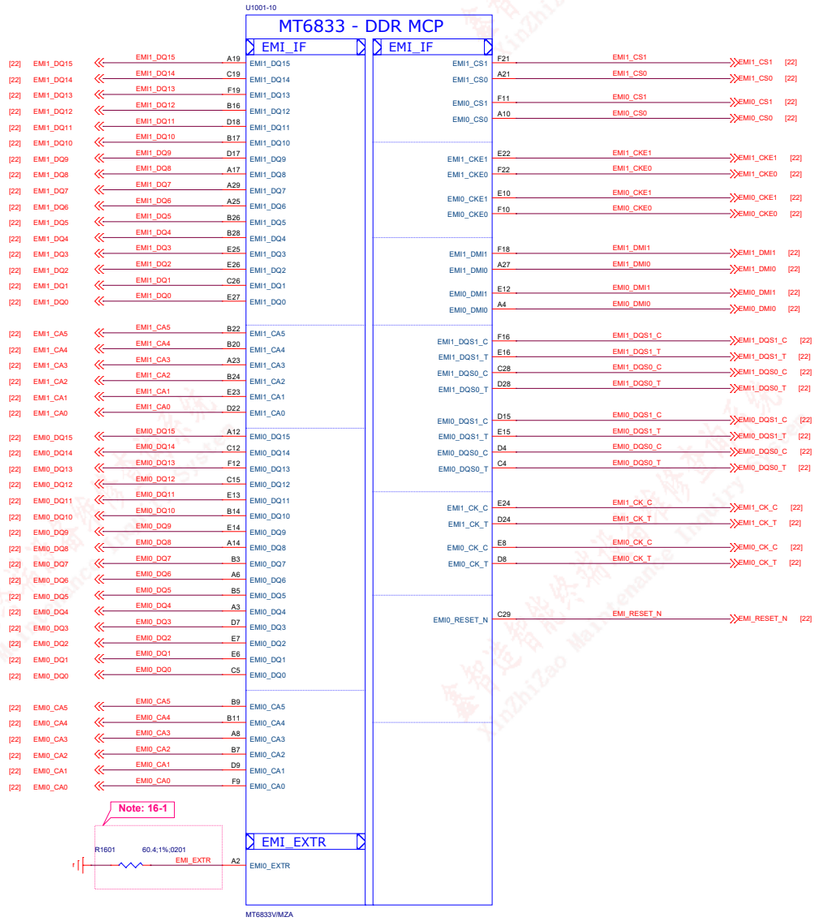
16_BB_4



Schematic design notice of "16_BB_4_Interface" page:

Note 16-1: R4001 please select 60.4 ohm (1%) resistor

Title	016_BB_4_EMI	REV: V10
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DEPARTMENT: BB	DESIGNER: liufengjei	
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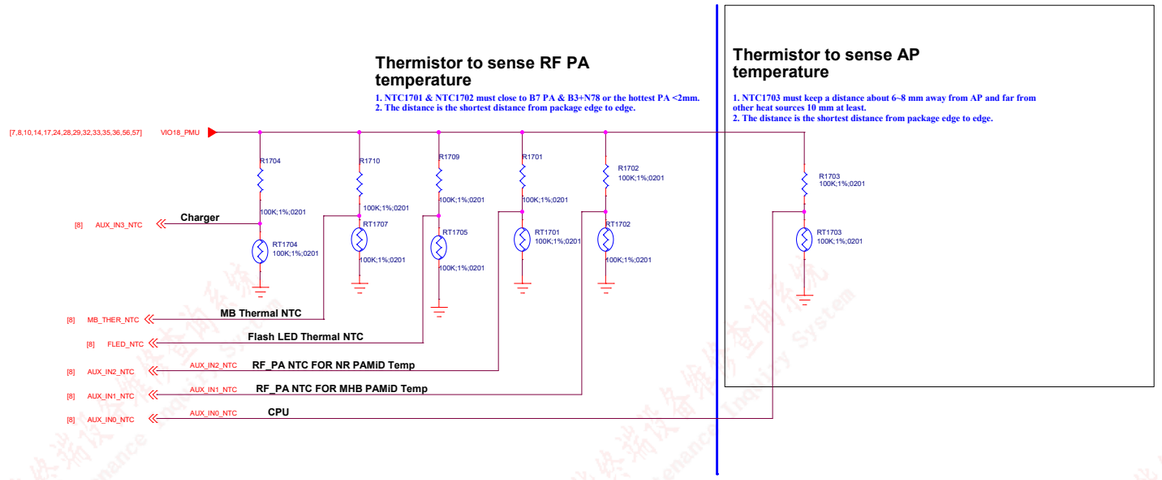
17_BB_AUXADC_Thermal



Title	017_BB_AUXADC_Thermal	REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112	Size D
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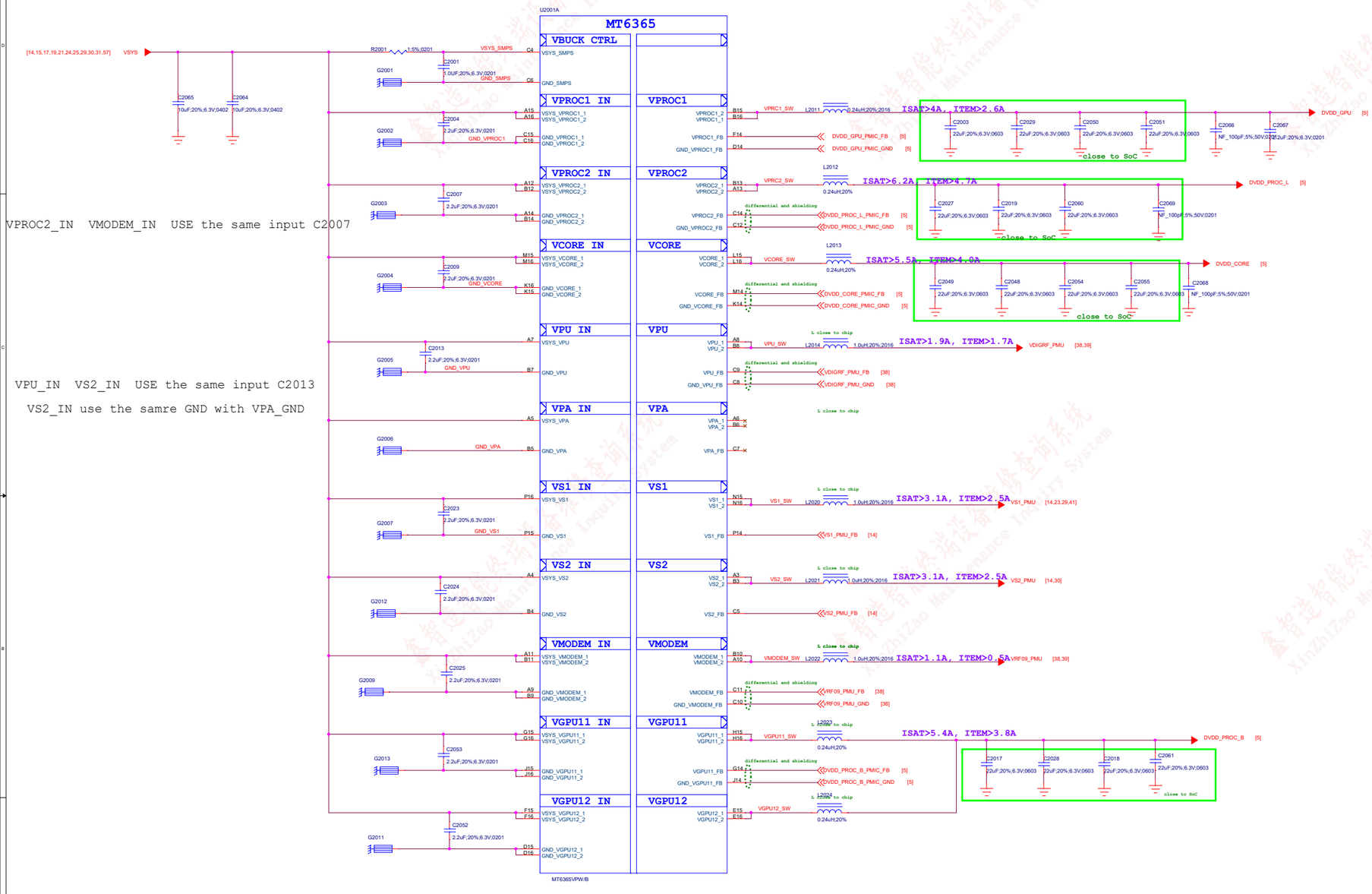
20_POWER_MT6365-Buck



VPROC2_IN VMODEM_IN USE the same input C2007

VPU_IN VS2_IN USE the same input C2013

VS2_IN use the samre GND with VPA_GND

Circuit Type	BUCK Name (Application name)	Output Voltage Range(V)	BOOT Defalut	Iout max(mA)
Buck	VPROC1 (DVDD_GPU)	0.40~1.19 (6.25mV/step)	ON(0.75)	4800
	VPROC2 (DVDD_PROC_L)	0.40~1.19 (6.25mV/step)	ON(0.75)	4800
	VGP11+12 (DVDD_PROC_B)	0.40~1.19 (6.25mV/step)	ON(0.75)	4800*2
	VCORE (DVDD_CORE)	0.40~1.3 (6.25mV/step)	ON(0.75)	4800
	VMODEM （VRF09_PMU）	0.50~1.10 (6.25mV/step)	OFF	4800
	VPU (VDIGRF_PMU)	0.40~1.19 (12.5mV/step)	ON(0.7)	2400
	VS1 (VS1_PMU)	1.86~2.20 (12.5mV/step)	ON(2.0)	2200
	VS2 (VS2_PMU)	1.20~1.50 (12.5mV/step)	ON(1.35)	2500
	VPA (VPA_PMU)	0.50~3.40 (50mV/step)	OFF	1000

Title	020_POWER_MT6365_Buck	REV: V10	
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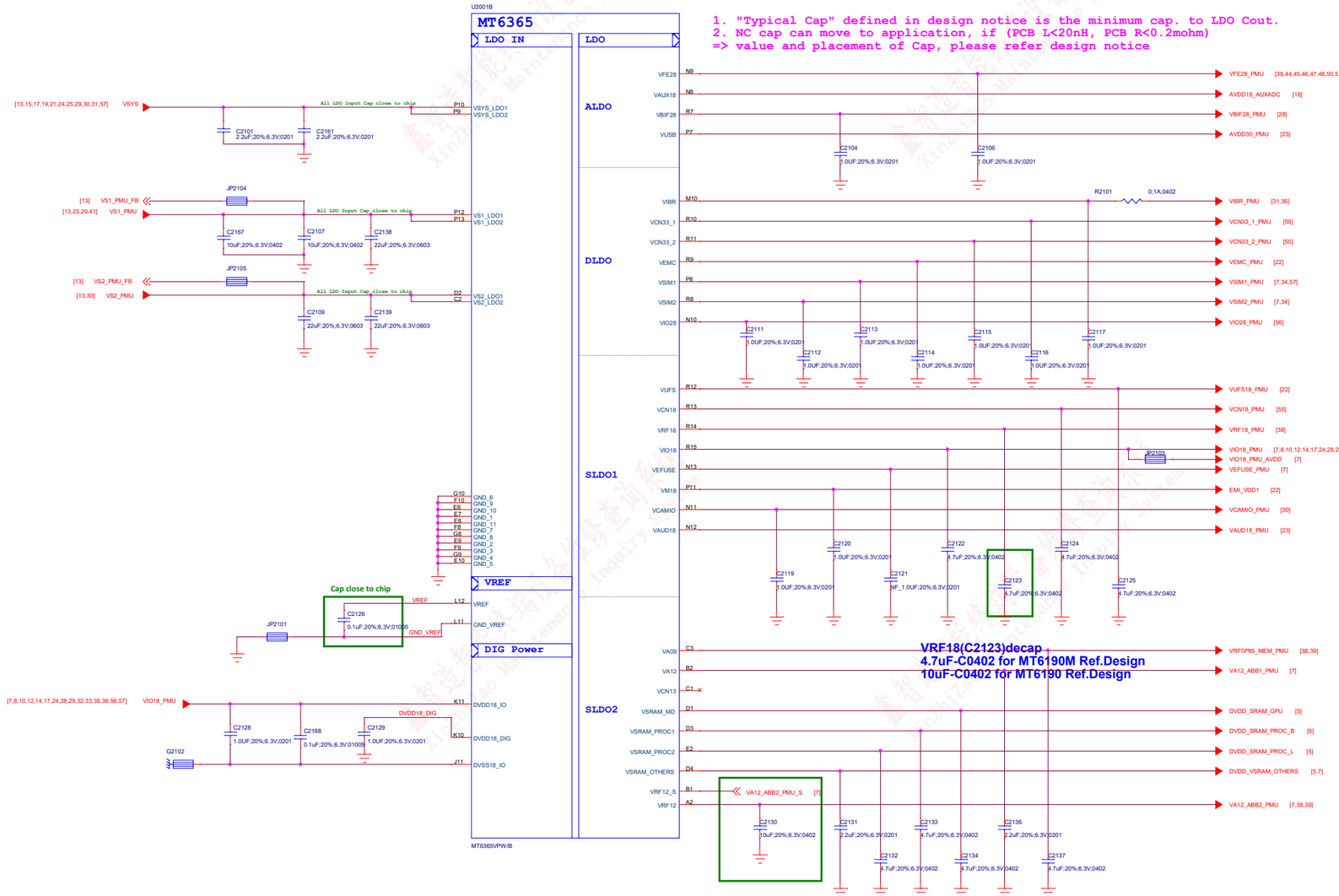
21_POWER_MT6365-LDO



LDO Name	Output Voltage(V)	BOOT Defalut	Iout max(mA)	Expected use
VEF28	2.80	OFF(2.8)	200	RFFE
VUSB	3.07	ON(3.07)	200	USB
VAUX18	1.84	ON(1.84)	50	AUXADC
VXO22	2.24	ON(2.24)	25	DCXO
VRFCK	1.4@boot 1.6@work	ON(1.4)	10	DCXO
VBIF28	2.80	OFF(2.8)	50	Battery Interface
VRTC	2.80	ON(2.8)	2	RTC
DVDD18_DIG	1.80	ON(1.8)	10	PMIC Digital
VSIM1	1.7/1.8/1.86/2.76/3.0/3.1	OFF(1.86)	200	SIM
VSIM2	1.7/1.8/1.86/2.76/3.0/3.1	OFF(1.86)	200	SIM
VCN33_1	3.3/3.4/3.5/3.6	OFF(3.3)	800	Connectivity
VCN33_2	3.3/3.4/3.5/3.6	OFF(3.3)	800	Connectivity
VEMC	2.55/2.9/3.0/3.3	ON(3.0)	800	eMMC/UFS
VIO28	2.8/2.9/3.0/3.1/3.2/3.3	OFF(2.8)	200	IO&Sensor
VIBR	2.7/2.8/3/3.3	OFF(2.8)	200	Vibrator
VEFUSE	1.80	OFF(1.8)	300	EFUSE
VAUD18	1.80	ON(1.8)	300	Audio
VCAMIO	1.80	OFF(1.8)	300	Camera IO
VM18	1.80	ON(1.8)	300	DRAM
VRF18	1.80	OFF(1.8)	450	RF
VIO18	1.80	ON(1.8)	600	IO&Sensor
VCN18	1.80	OFF(1.8)	1200	Connectivity
VUFS	1.86	ON(1.86)	1200	eMMC/UFS
VBBCK	1.24	ON(1.24)	10	DCXO
VA09	0.85	ON(0.85)	300	DIGRF SRAM (VRF0P85_MEM_PMU)
VA12	1.2	ON(1.2)	300	AP Analog Module
VCN13	1.3	OFF(1.3)	350	Connectivity
VSRAM_PROC1	0.60~1.2 （6.25mV/step）	ON(0.85)	600	CPUB SRAM
VSRAM_PROC2	0.60~1.2 （6.25mV/step）	ON(0.85)	600	CPUL SRAM
VSRAM_OTHERS	0.60~1.2 （6.25mV/step）	ON(0.75)	600	OTHERS SRAM
VSRAM_MD	0.60~1.2 （6.25mV/step）	ON(0.85)	600	GPU SRAM
VRF12	1.2	ON(1.2)	800	AP Analog Module

Title	021_POWER_MT6365_LDO	REV: V10	
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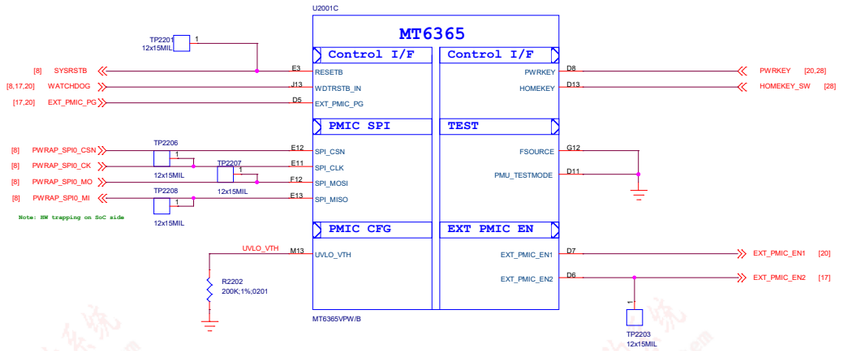
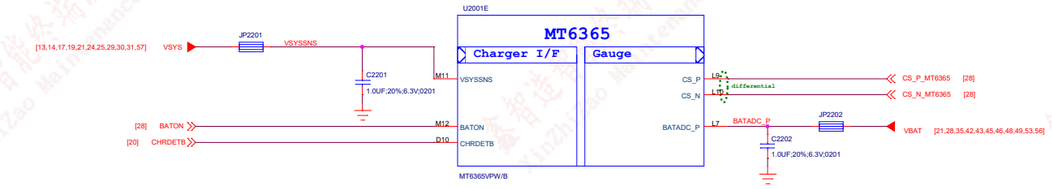
22_POWER_MT6365-General





Title	022_POWER_MT6365_General	REV:	V10
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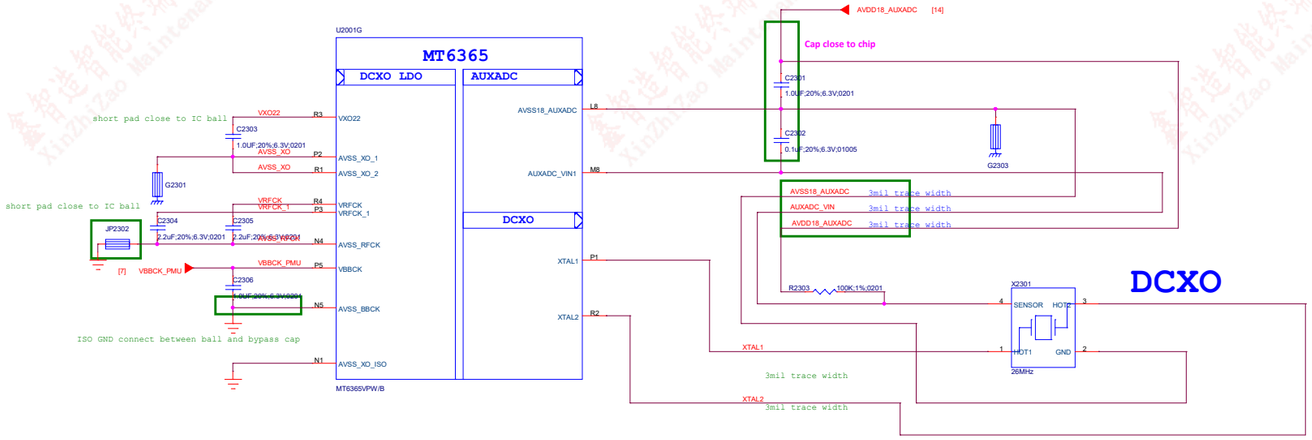
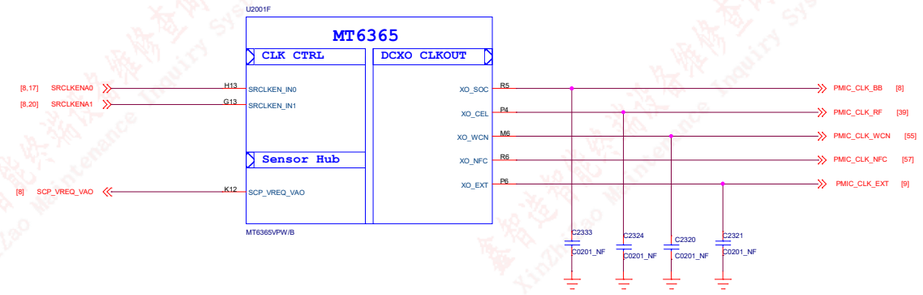
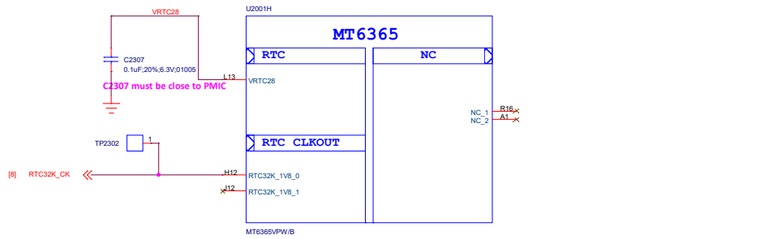
23_POWER_MT6365_Clock



Route XTAL1/ XTAL2/ AVDD18_AUXADC/ AUXADC_VIN/ AVSS18_AUXADC with 3mils width traces and well GND shielding.





Title	023_POWER_MT6365_Clock		REV: V10
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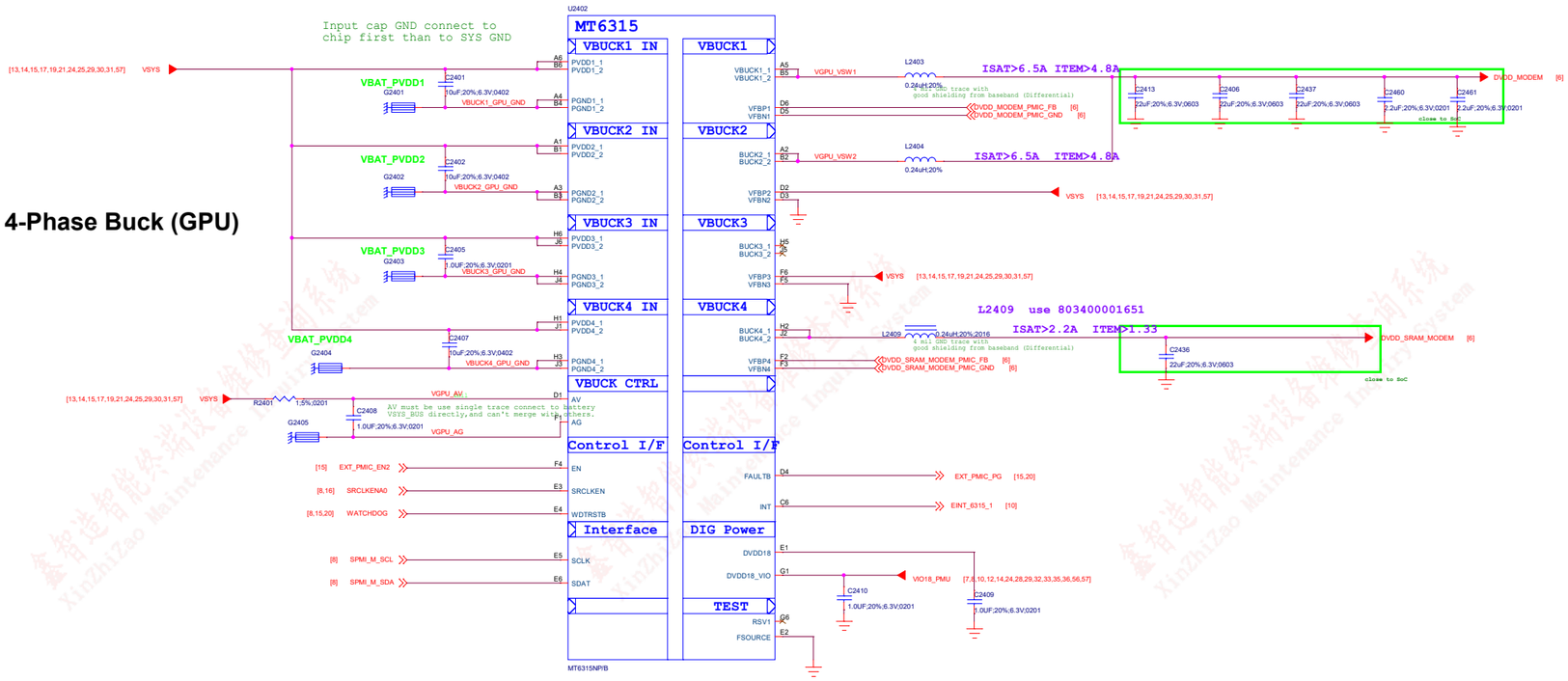
MT6315 4-Phase Buck (GPU)



Title 024_POWER_MT6315_BUCK		REV: V10
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Title	025_Reserved	REV: V10
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DEPARTMENT:	BB	DESIGNER: liufenglei
	WINGTECH	
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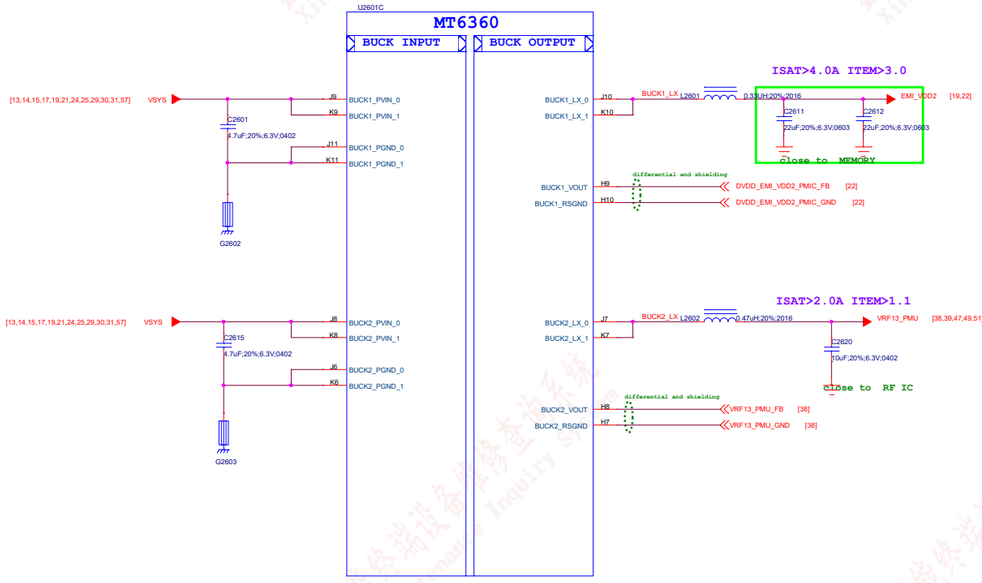
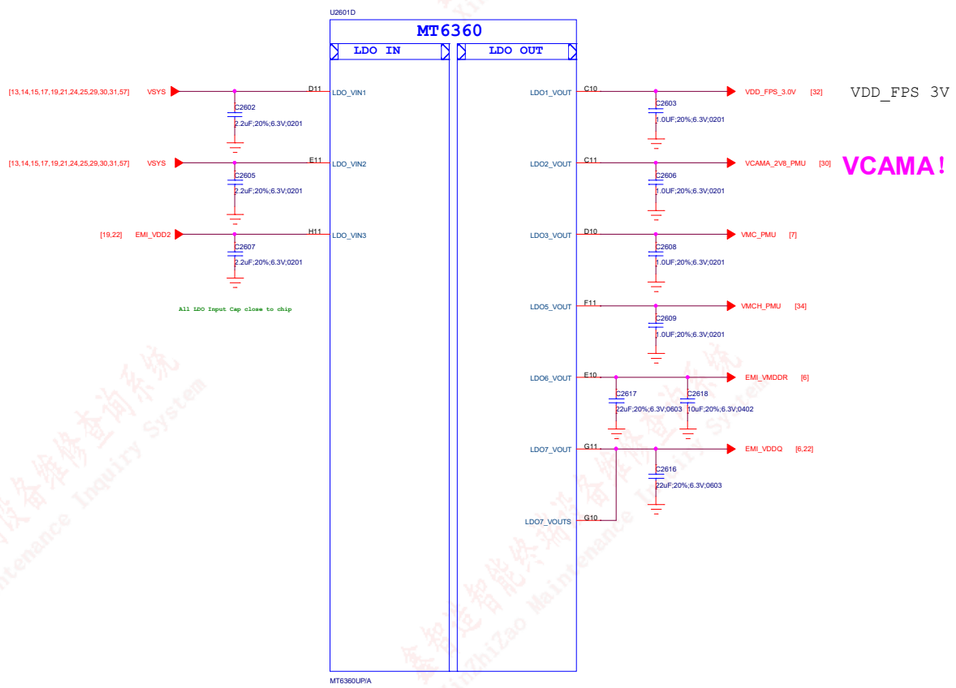
26_POWER_MT6360_BUCK_LDO





Circuit Type	Name	Output Voltage Range(V)	BOOT Defalut	Iout max(mA)	Expected use
Buck	BUCK1	0.3~1.3 (5mV/step)	ON(1.125)	3000	VDRAM1
	BUCK2	0.3~1.3 (5mV/step)	ON(0.75)	3000	VSRAM_CORE+ADSP
LDO	LDO1	1.8/2/2.1/2.5/2.7/ 2.8/2.9/3/3.1/3.3	OFF(1.8)	150	Fingerprint
	LDO2	1.8/2/2.1/2.5/2.7/ 2.8/2.9/3/3.1/3.3	OFF(1.8)	200	CAM AVDD
	LDO3	1.8/2.9/3/3.3	OFF(3.0)	200	SD Card
	LDO5	2.9/3/3.3	OFF(3.0)	800	SD Card
	LDO6	0.75	ON(0.75)	300	EMI_VMDDR
	LDO7	0.6	ON(0.6)	600	EMI_VDDQ

Title	026_POWER_MT6360_LDO_BUCK	Rev 1.0
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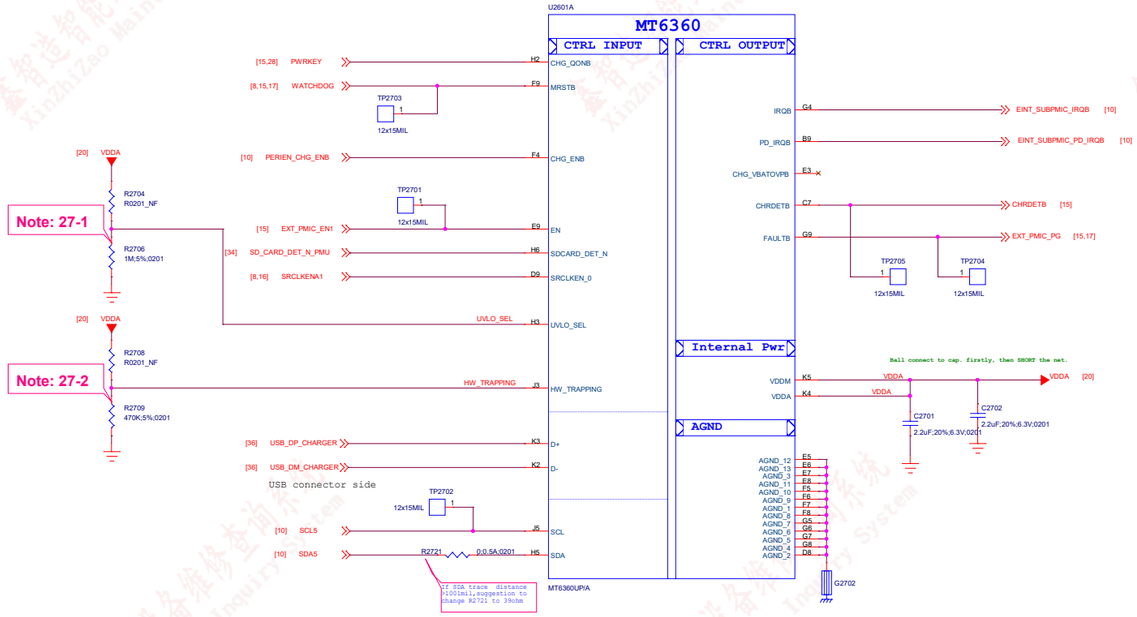
27_POWER_MT6360_General



Note 27-1: UVLO_SEL pin is define difference UVLO power configuration.The power configuration is used to Ruvlosel (R2706) to select.

Note 27-2: HW_TRAPPING is define difference power configuration.The power configuration is used to Rhw_trapping (R2709&R2704) to select.

REG_PMU0x04[7:5] : HW_SYSUV_SEL[2:0]	RUVLO_SEL Range(Ω)		
	Min	Typ	Max
000（2.8V）	Short to VDDA		
001（2.9V）	936K	1.8M	---
010（3.0V）	234K	430K	663K
011（3.1V）	58K	100K	165K
100（3.2V）	14K	28K	41K
101~111（3.3V）	---	7.5K	10K

REG_PMU0x99[2:0] : HW_TRAPPING[2:0]	Rhw_trapping Range(Ω)			BUCK1	BUCK2	LDO6	LDO7
	Min	Typ	Max				
000	Short to VDDA			0.725V	1.125V	0.75V	0.6V
001	936K	1.8M	---	0.725V	1.125V	X	1.8V
010 (Default)	234K	430K	663K	1.125V	0.725V	0.75V	0.6V
011	58K	100K	165K	1.125V	0.725V	X	1.8V
100	14K	28K	41K	0.725V	1.225V	X	X
101	3.8K	7.5K	10K	1.225V	0.725V	X	X
110	0.96K	1.6K	2.4K	0.725V	1.125V	X	X
111	---	422	603	0.725V	0.725V	X	X

Title	027_POWER_MT6360_General		REV: V10
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DEPARTMENT:	BB	DESIGNER:	liufengfei
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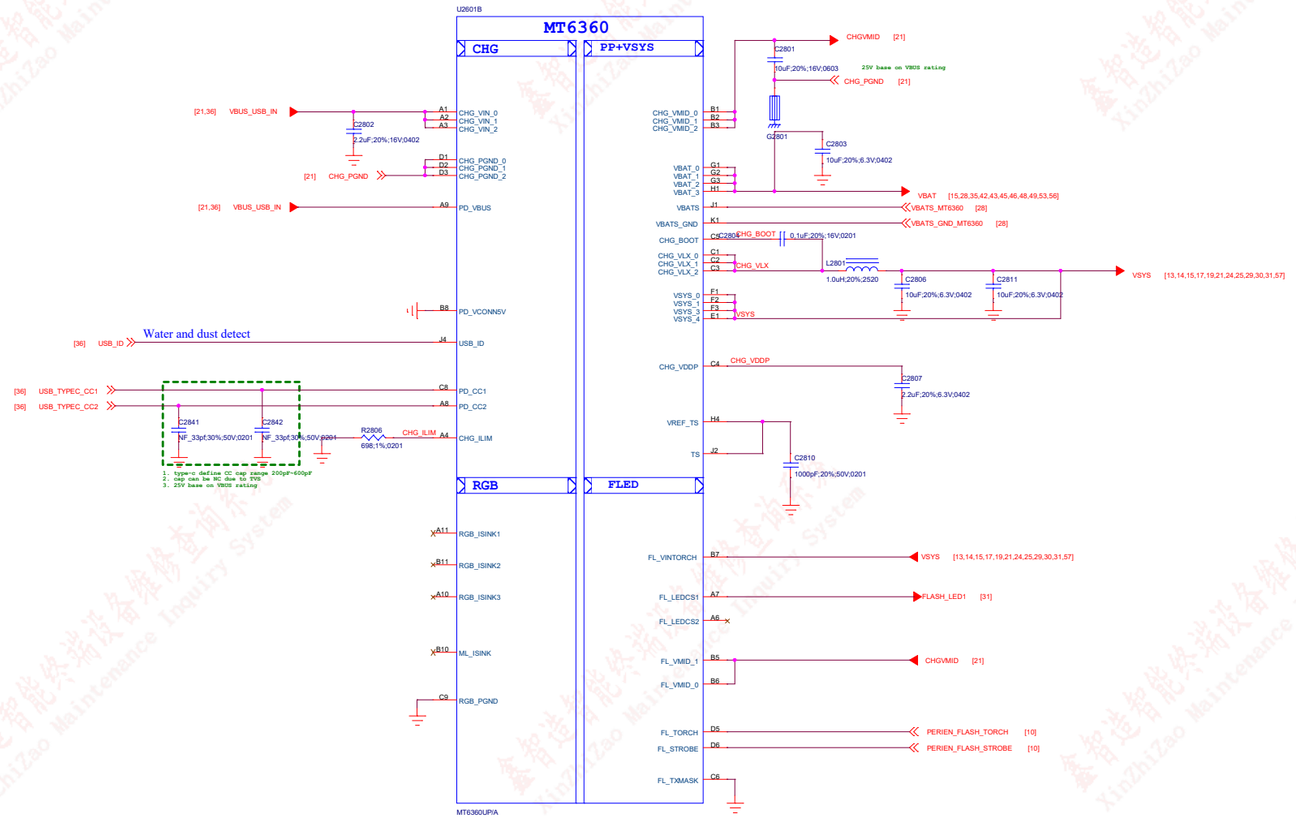
28_POWER_MT6360_Charger



Title	028_POWER_MT6360_Charger		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	BB	DESIGNER:	liufenglei
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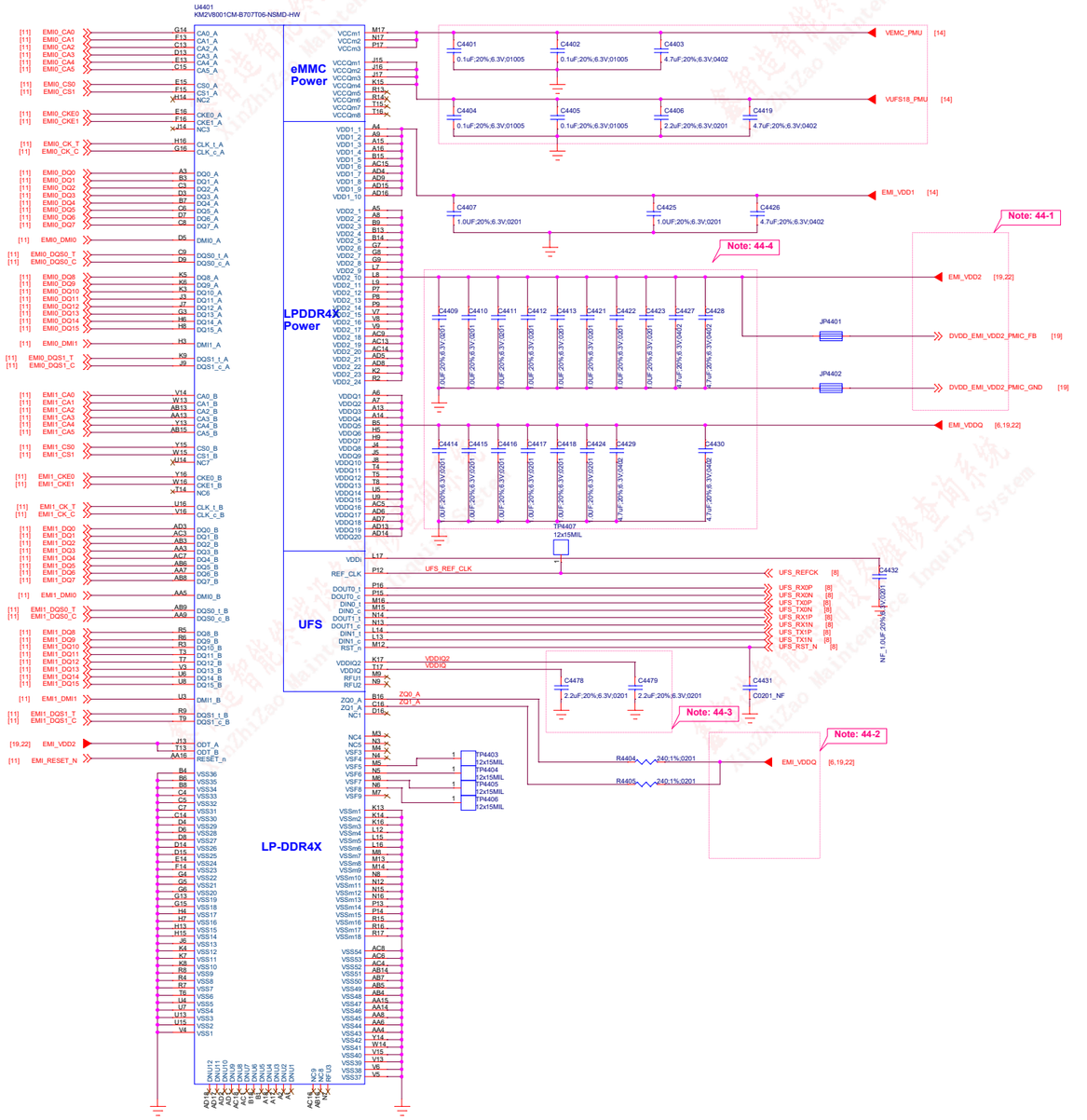
44_Memory_UFS_LPDDR4X



Schematic design notice of "44_Memory_UFS_LPDDR4X" page.

Note 44-1: Please refer to power supply related page select LDO7_VOUT / BUCK1_LX output voltage properly for LPDDR4X

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

Note 44-3: Please refer to uMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of UFS.

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

Title	044_Memory_UFS_LPDDR4X	REV:	V10
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DEPARTMENT:	BB	DESIGNER:	liufenglei
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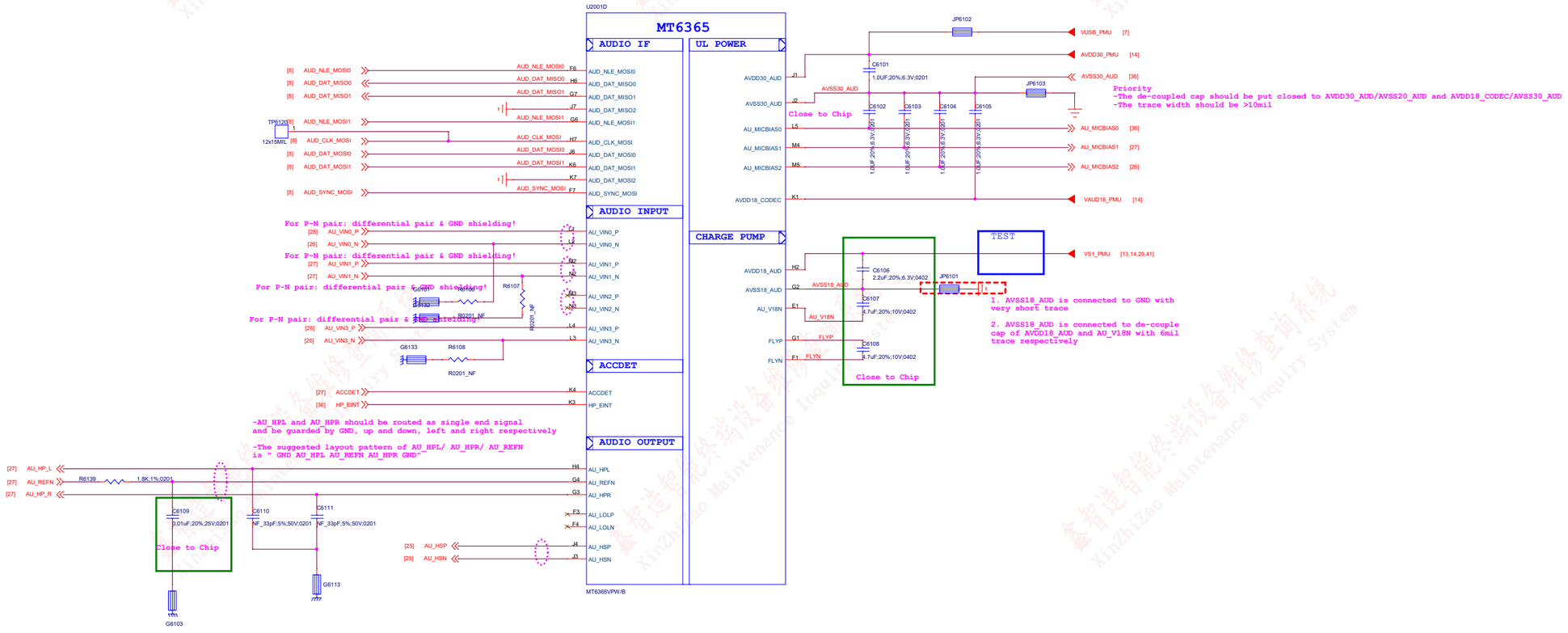
61_POWER_MT6365_AUDIO



Title	061_PERI_6365_AUDIO_PMIC_IF		V10
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DEPARTMENT:	BB	DESIGNER:	liufenglei
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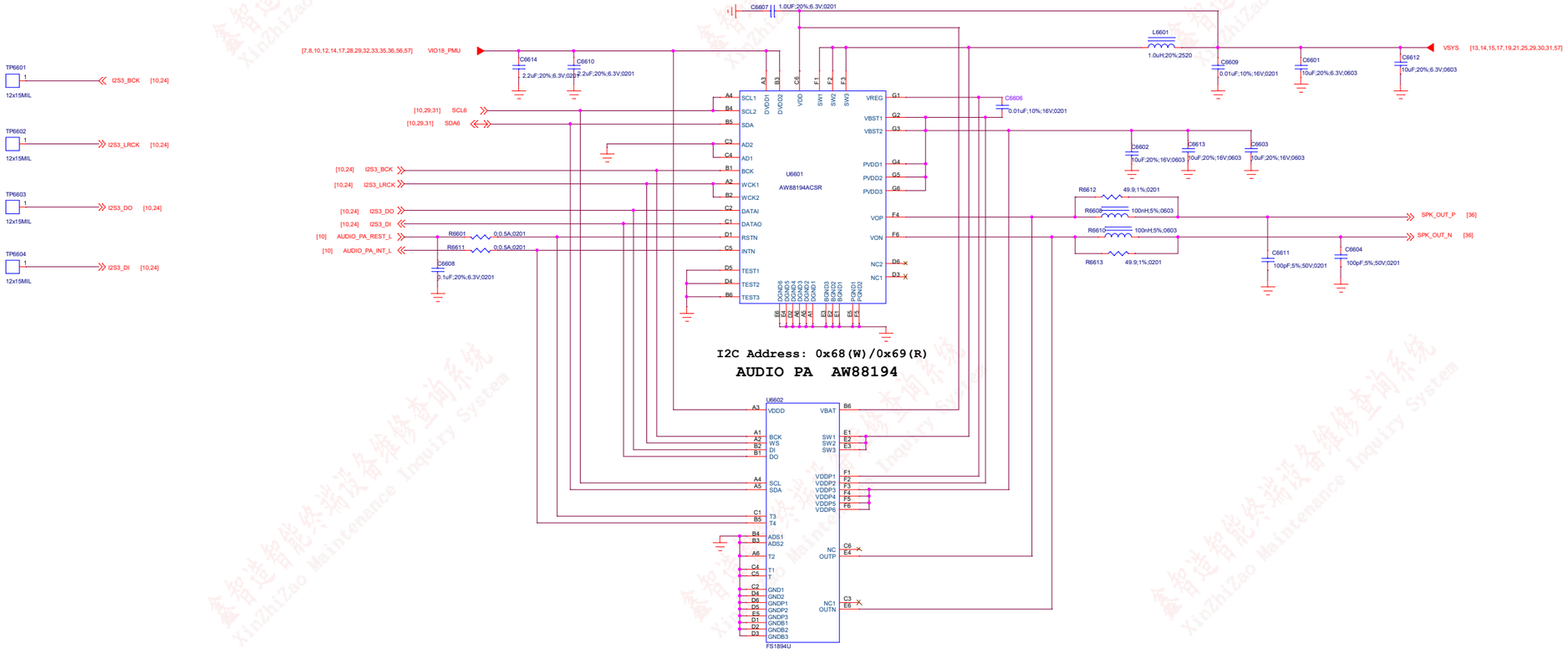
066_SPK



Title	066_SPK	REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112	Size D
DEPARTMENT:	BB	DESIGNER: Ning Xinwu
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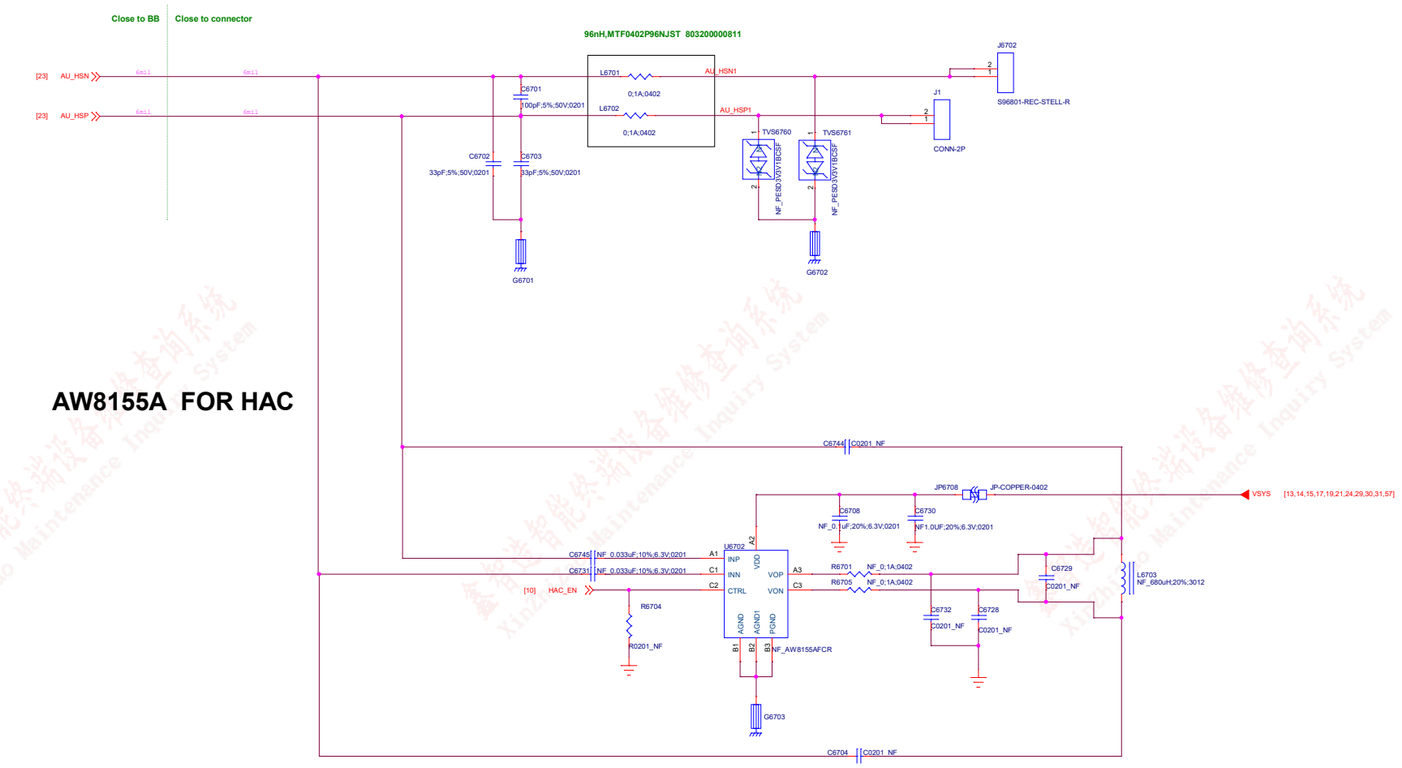
067_Receiver

Receiver



Title	067_Receiver		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	BB	DESIGNER:	liufenglei
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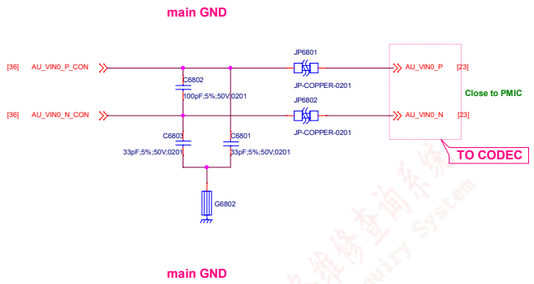
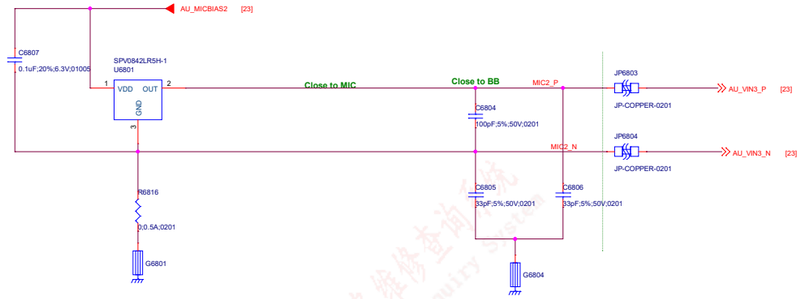
068_MIC

MAIN MIC



second Microphone



Title	068_MIC		REV: V10
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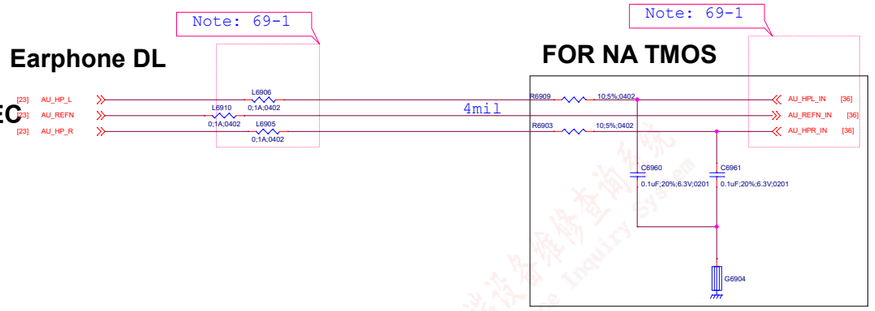
069_Earphone

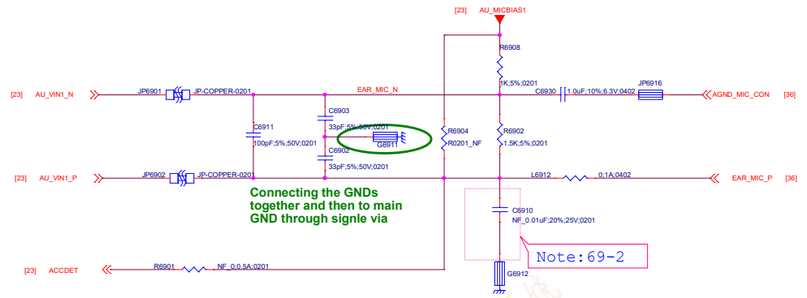
Earphone DL

TO CODEC

L6905,L6906,L6910 上磁珠803340000181 debug



Earphone Microphone



Schematic design notice of "62_PERI_AUDIO_IO" page.

Note 69-1: Part # of BEAD6202, BEAD6203, BEAD6204 and BEAD6205 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

Note 69-2: Reserved Cap C6910 for CS/RS test, please double check multi-key function when used

Note 4-3:

	Earphone Jack @ Main board	Earphone Jack @ Sub board
R413	0 ohm	100nF

Note 4-4: 1. Need do SW configuration for DCC mode
2. Analog input 阻抗 impedance is as below, please customer check the detail requirement with mic vendor if the mic used has special requirement on the input impedance of analog input

MT6357	UL Mode	MIN	TYP	MAX	Unit
C	DCC	-	-	11p	F

Note 4-5: Please select R6231 with 0402 size

Title	069_Earphone		REV: V10
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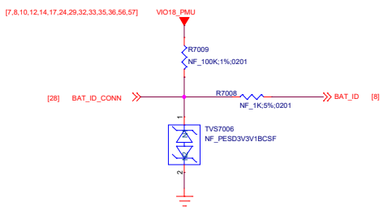
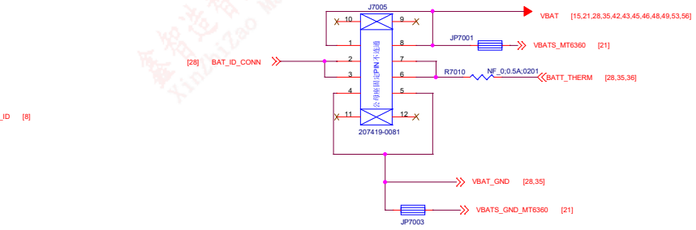
070_Battery/Sidekey

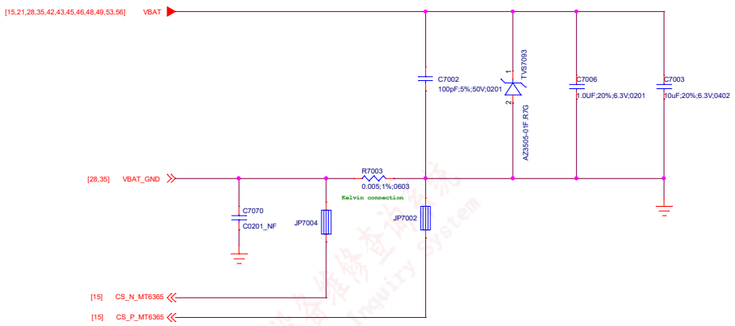
BATTERY CONNECTOR

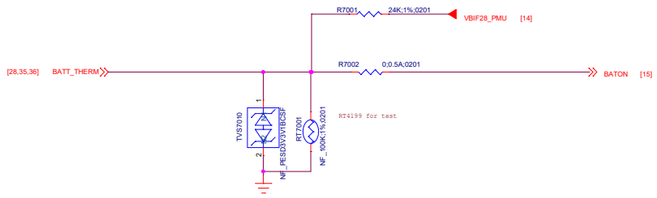
BAT ID



BATTERY CONN

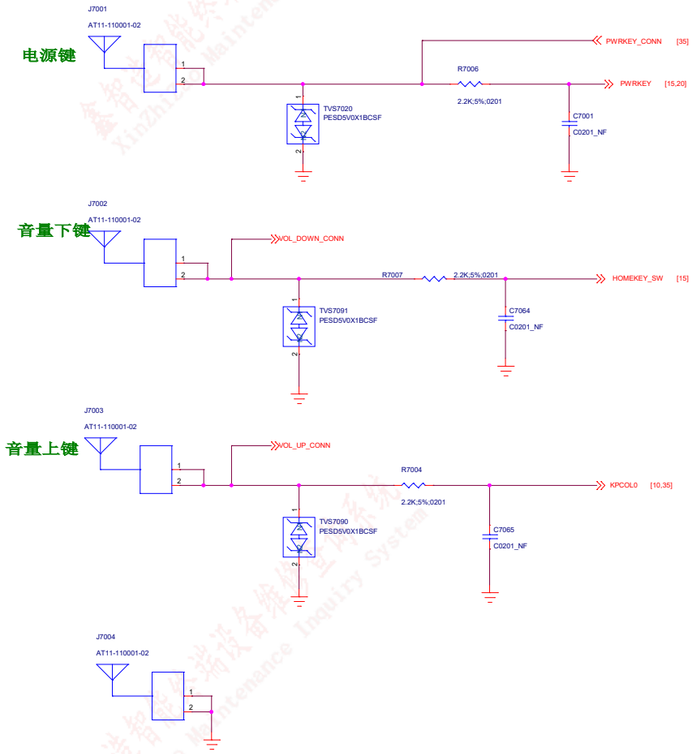


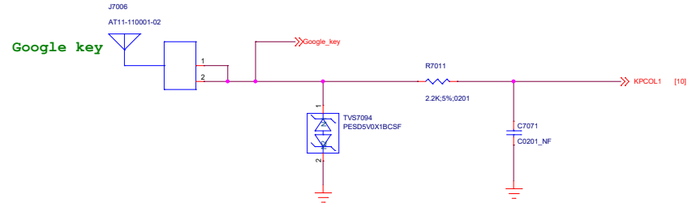




Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY





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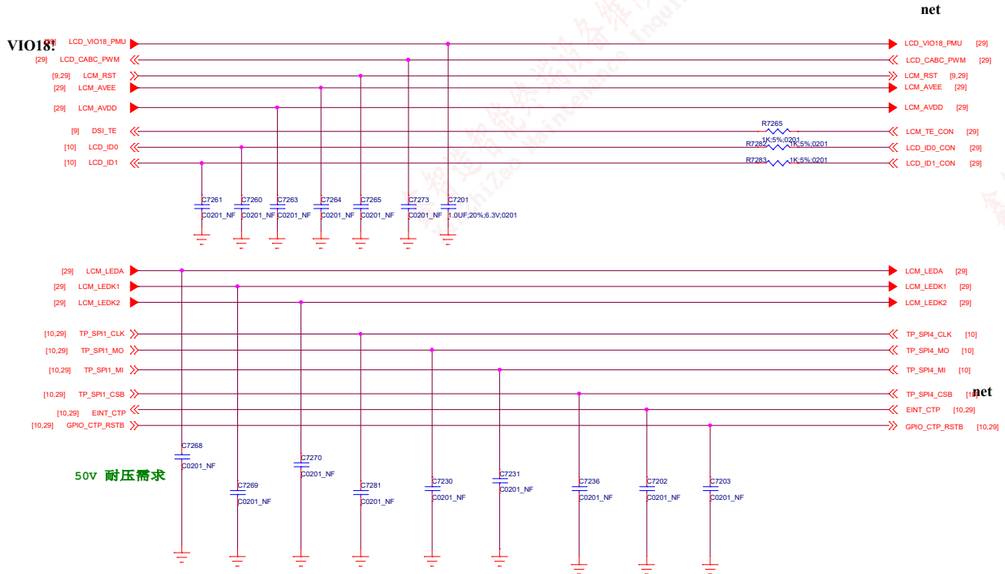
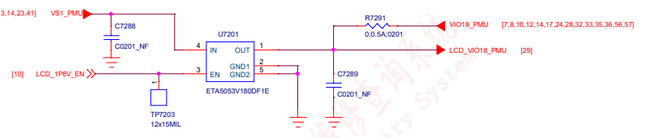
072_LCD/CTP IF

LCM Gate Drive

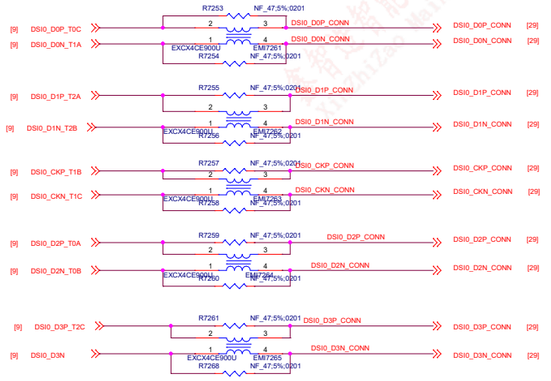


Reserve for ESD

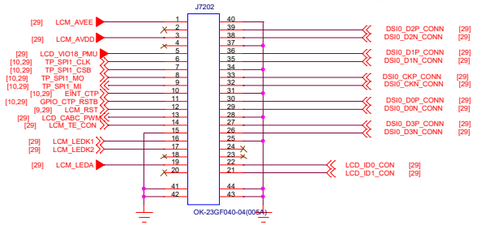


Main LCM

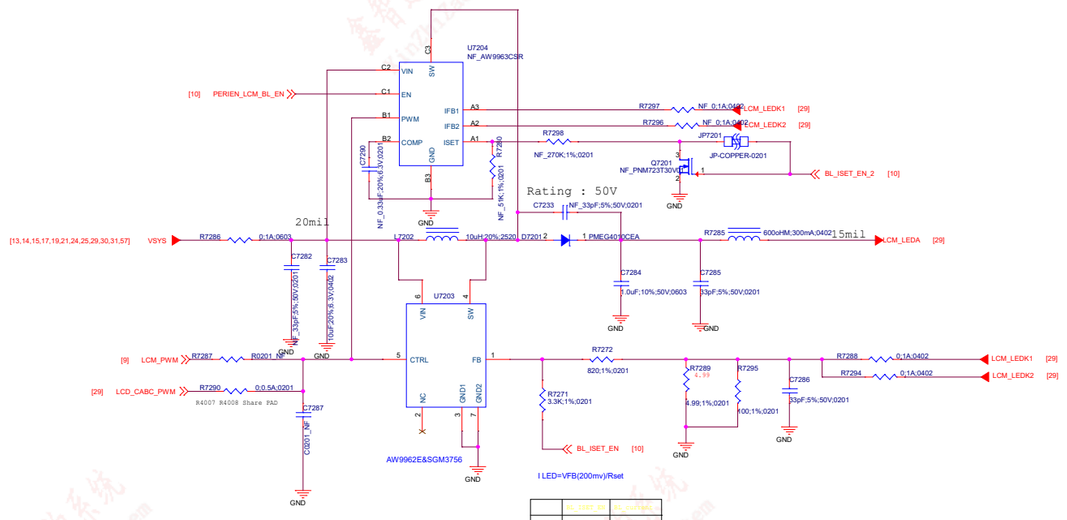
Main LCM



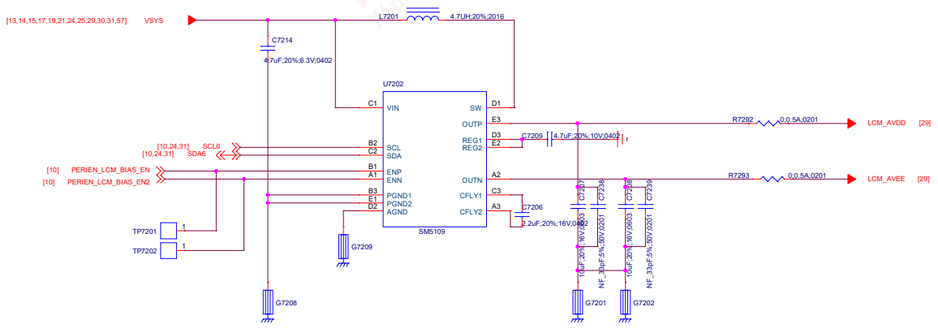
Customer P/N_change!



LCD-BACKLIGHT



SM5109/OCP2130 LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)



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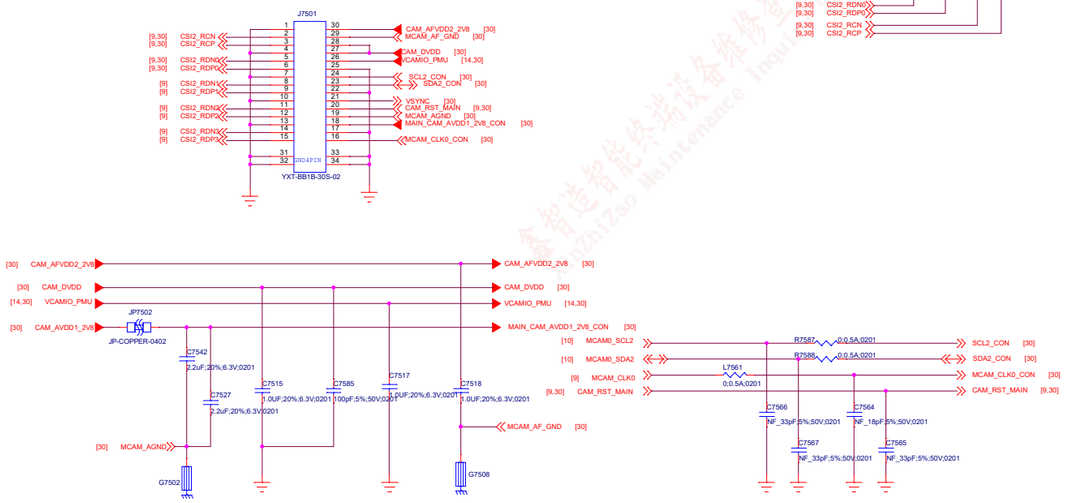
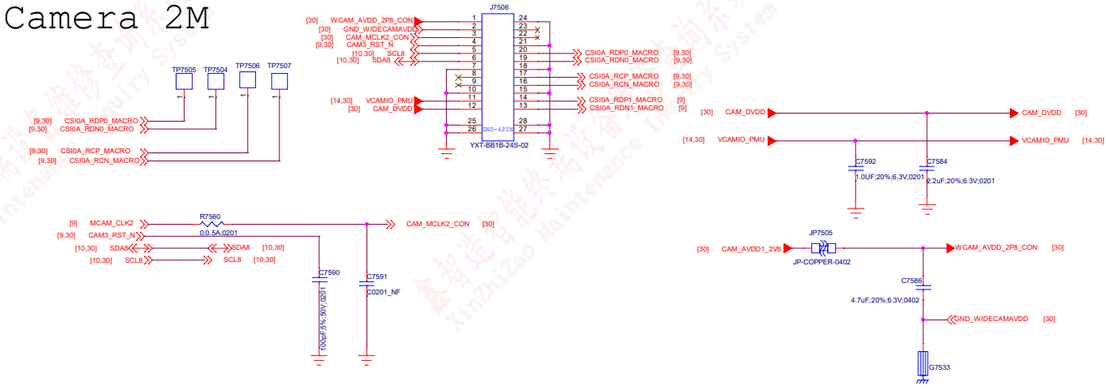
075_CAMERA IF

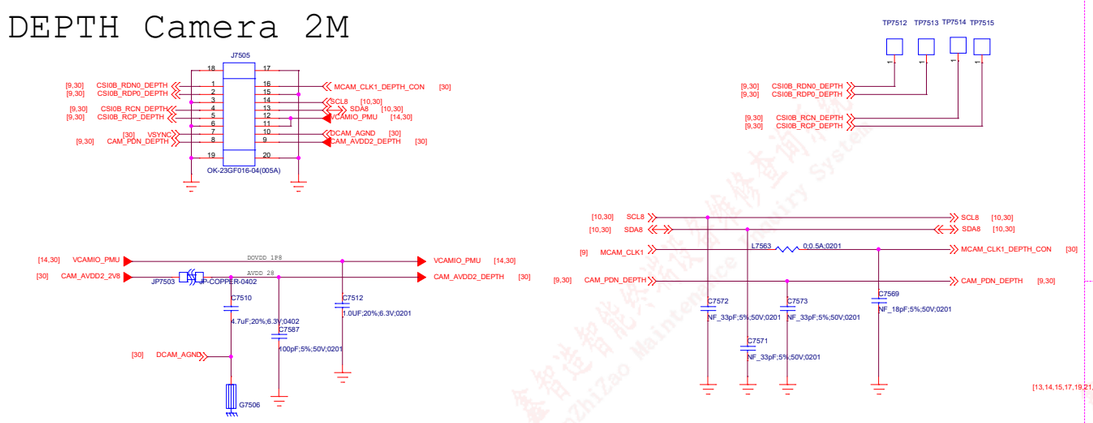
Main Camera 48M



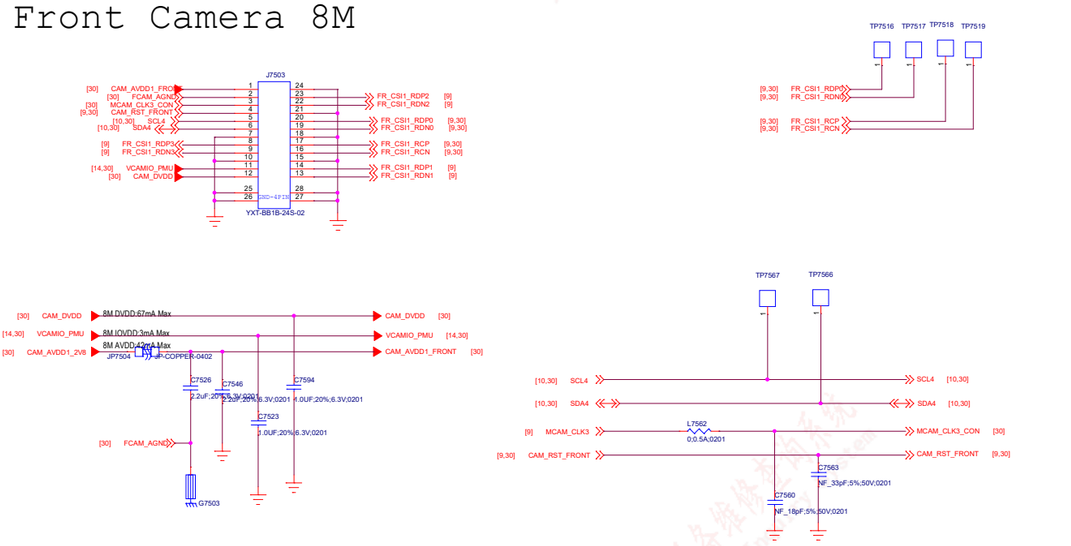
Macro Camera 2M



DEPTH Camera 2M

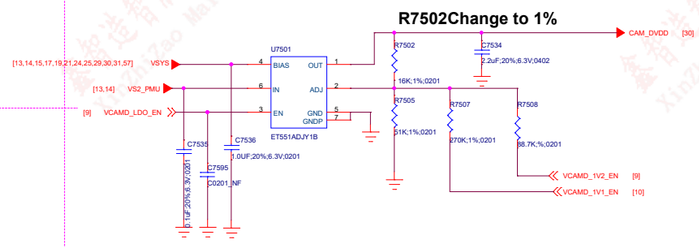


Front Camera 8M



LDO for Main Camera 48M DVDD and Front Camera DVDD

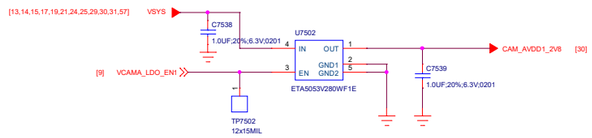
R7502Change to 1%

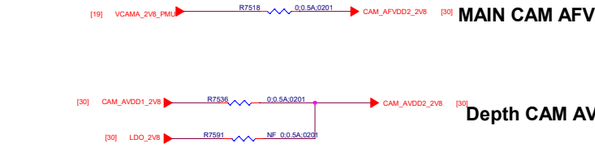


Vout=0.8V*(R1+R2)/R2 RT9081AQSA(2)

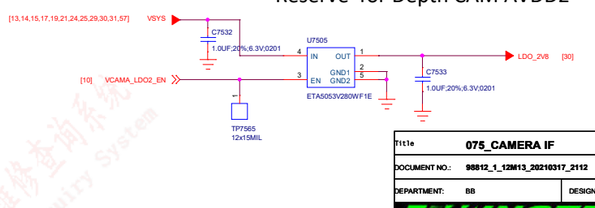
VCAMD_1V2_EN	VCAMD_1V1_EN	Voltage/V
high Z	high Z	1.1v
high Z	LOW	1.15v
LOW	high Z	1.20V

LDO1 for CAMERA AVDD 2.8V 0.3A





Reserve for Depth CAM AVDD2



	SOURCE	SENSOR	Operation Current(mA)	Choose Power	Software set
Main 48M	Main Source	S5KGM2SP	1.05V	1.05V	Q75xx:CHANGE_ENx ----Disable
	Second Source	IMX582-AAJH5-C	1.05V(710mA)	1.05V	Q75xx:CHANGE_ENx ----Disable
	Thirdly Source	OV48B2Q	1.15V(280mA)	1.15V	Q7502:CHANGE_EN1 ----Enable
Front 8M	Main Source	HI846	1.2V(67mA)	1.2V	Q7503:CHANGE_EN2 ----Enable
	Second Source	GC8034	1.2V(140mA)	1.2V	Q7503:CHANGE_EN2 ----Enable
WIDE5M	Main Source	HI846	1.2V(67mA)	1.2V	Q7503:CHANGE_EN2 ----Enable
	Second Source	GC8034	1.2V(140mA)	1.2V	Q7503:CHANGE_EN2 ----Enable

Title	075_CAMERA IF		REV: V10
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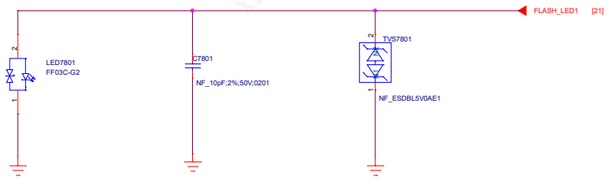
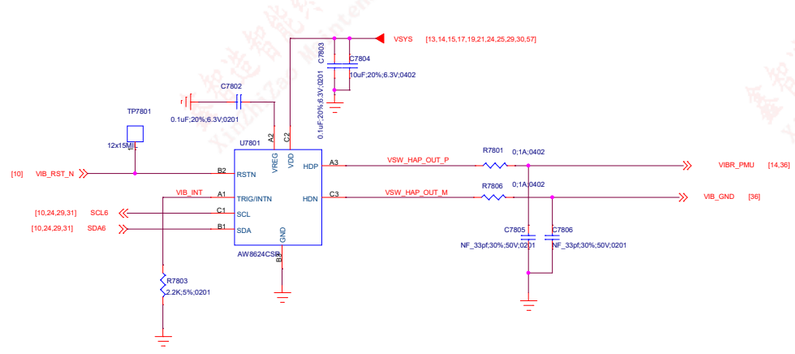
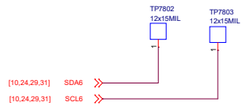
078_Flash/RGB/Vibrator

Flash LED



HAPTIC & ERM





Title	078_Flash/Vibrator		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
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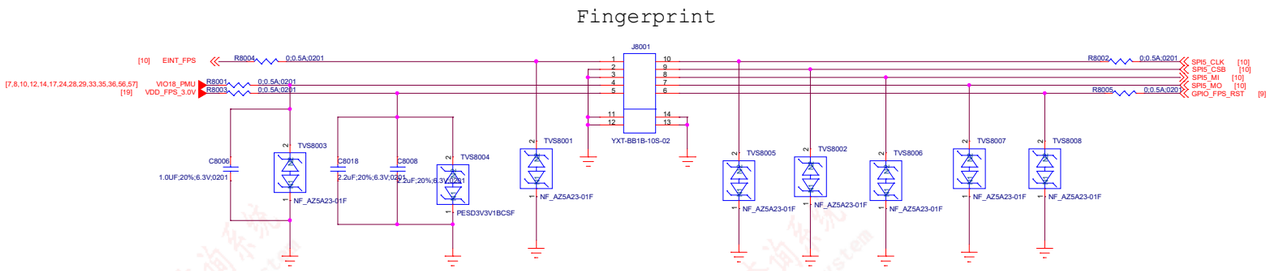
080_FingerPrint



Title	080_FingerPrint	REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112	Size D
DEPARTMENT:	BB	DESIGNER: liufenglei
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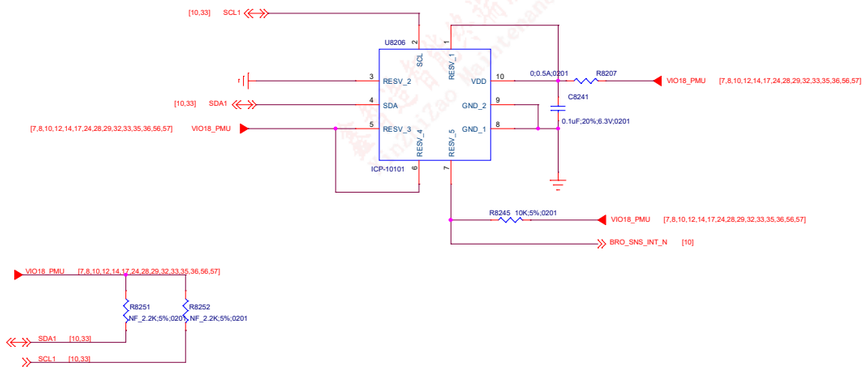
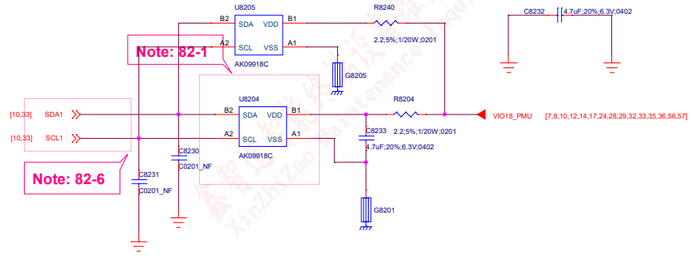
082_SENSORS

Barometer

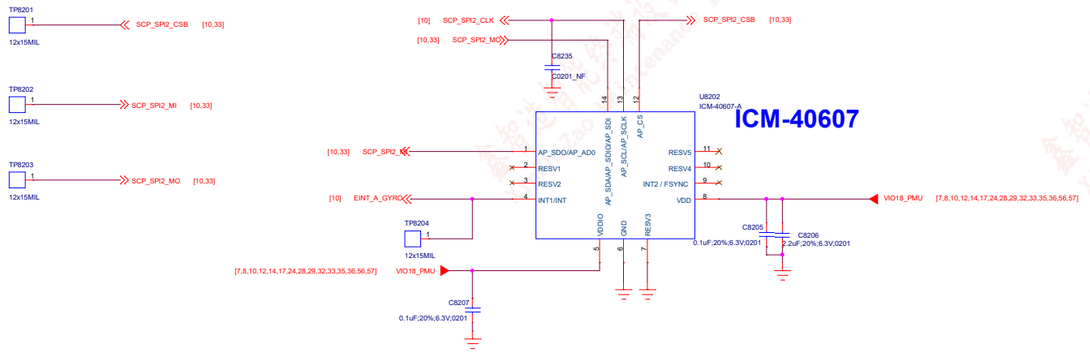


M-Sensor

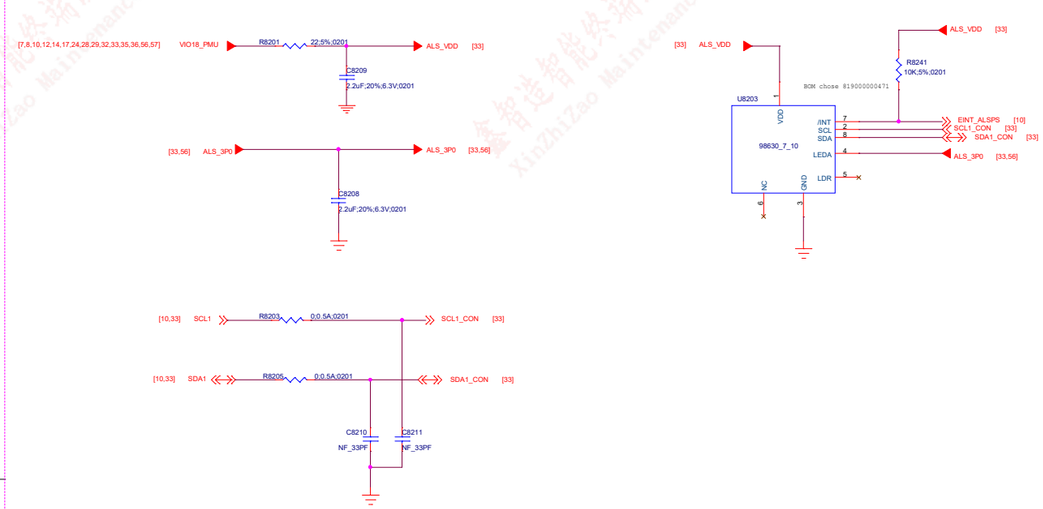
Compatible with BMP380



Accerometer + Gyro Sensor Optional



ALS+PS STK33562



Vendor	Manufacture PN	Slave Address (7-bit)	I2C Address(8-bit)	Remark
Sensortek	STK33562	0X46	Read:0X8C Write:0X8D	

Schematic design notice of "82_PERI_SENSORS_MEMs_ALS/PS" page.

Note 82-1: [M sensor] Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail

Note 82-2: [A+G] For optmized GPS performance, please check HW design notice for Sensor selection guide

Note 82-3: [A+G] MUST use SPI for optmized sensor hub performance **DO NOT USE i2C**

Note 82-4: [A+G] Suggest choose sensor support FIFO watermark interrupt otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse.

Note 82-5: [Baro] Reserve Baro sensor for LPPe feautre (Must for North America Operator / NA SKU)

Note 82-6: DO NOT share Sensor hub i2C to other non-SCP device

Note 82-7: Interrupt pin of MEMS sensor must be assign to ball EINT[12:0]

Title	082_SENSORS		REV: V10
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DEPARTMENT:	BB	DESIGNER:	liufengjel
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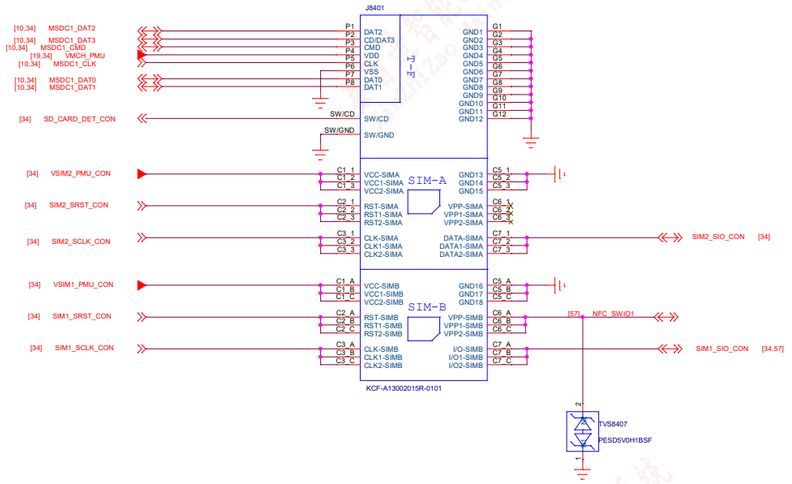
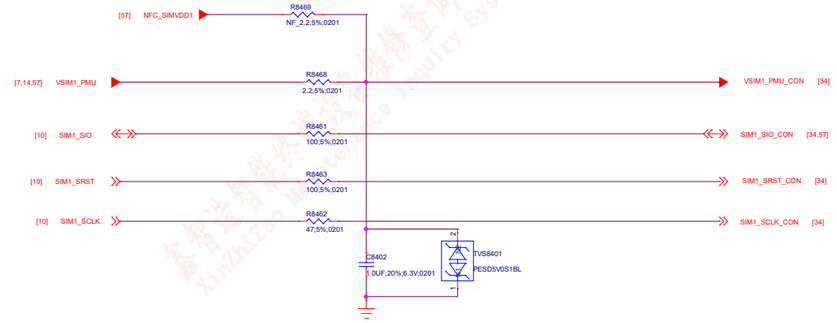
084_SIM/SD IF

CONNECTOR

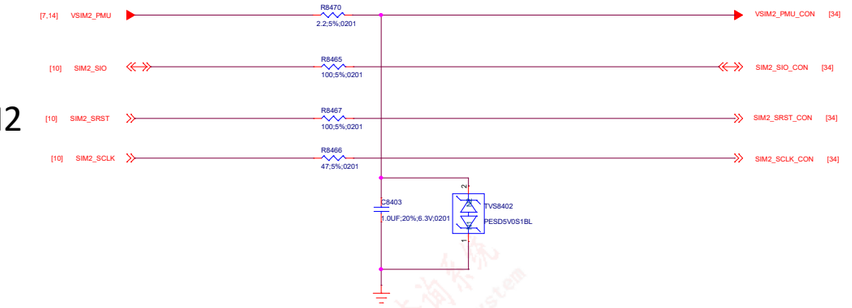


SIM CARD

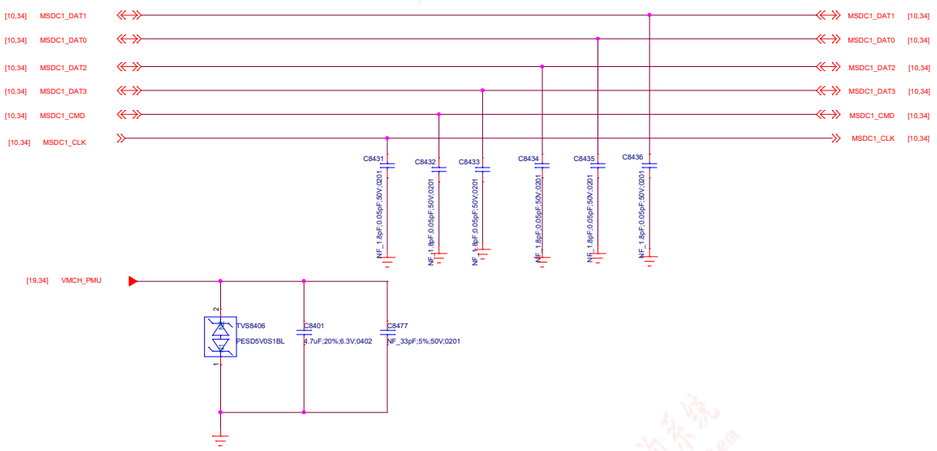
SIM1



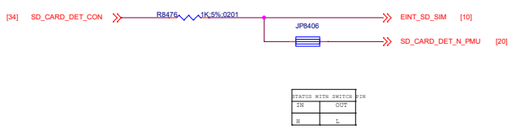
SIM2



T_Card



DETECT



Title	084_SIM/SD IF		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	BB	DESIGNER:	liufenglei
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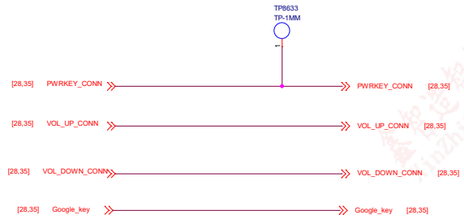
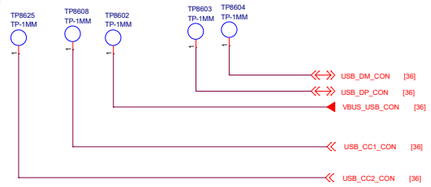
086_Testpoint/Shielding/GND

SIDEKEY

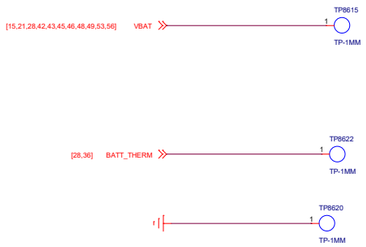


FORCE DOWNLOAD

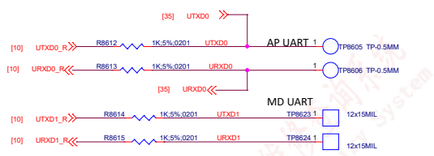
USB



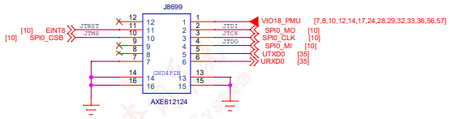
Battery



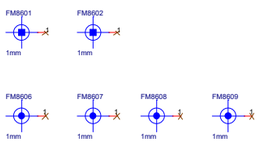
UART

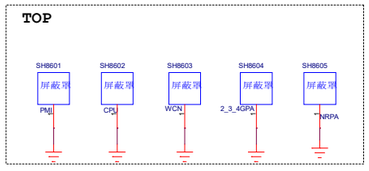


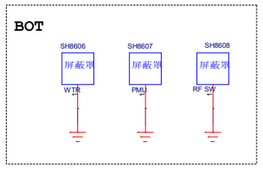
JTAG



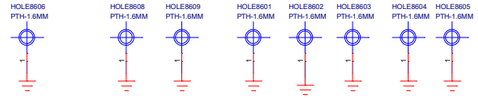
MARK/Shield/Lable/PCB



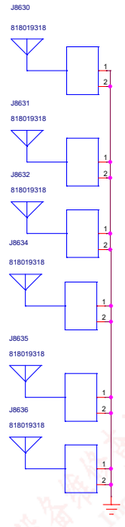


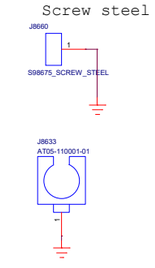


Hole



Spring GND





Title	086_Testpoint/Shielding/GND	REV:	V10
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DEPARTMENT:	BB	DESIGNER:	liufengtei
WINGTECH			
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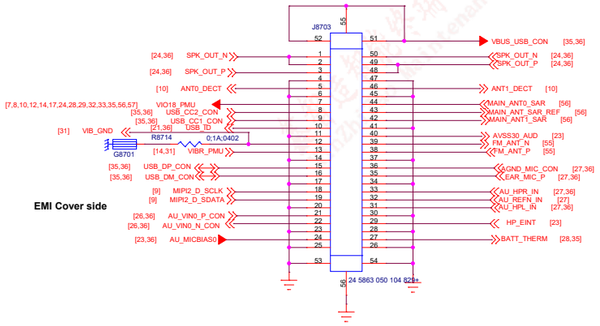
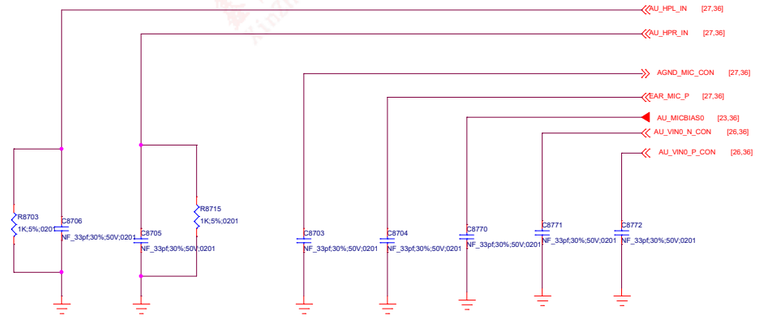
087_Sub PCB IF / USB IF

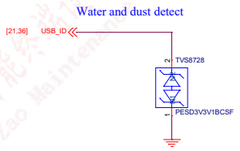
Customer P/N

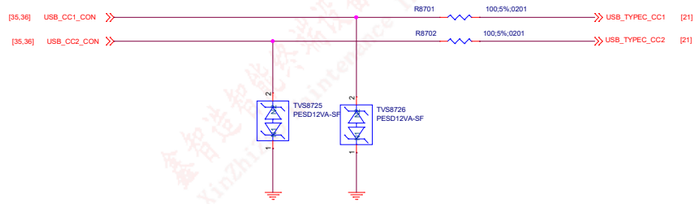


AUDIO CAP

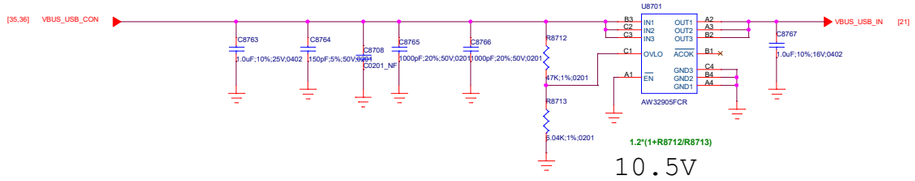


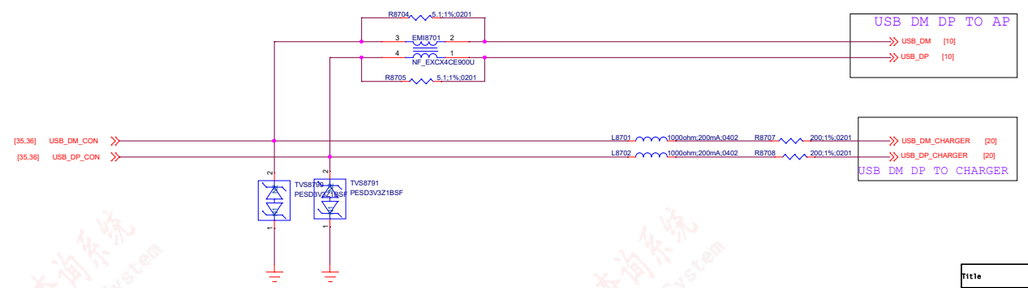
OVP





OVP





Title	087_Sub PCB IF / USB IF		REV: V10
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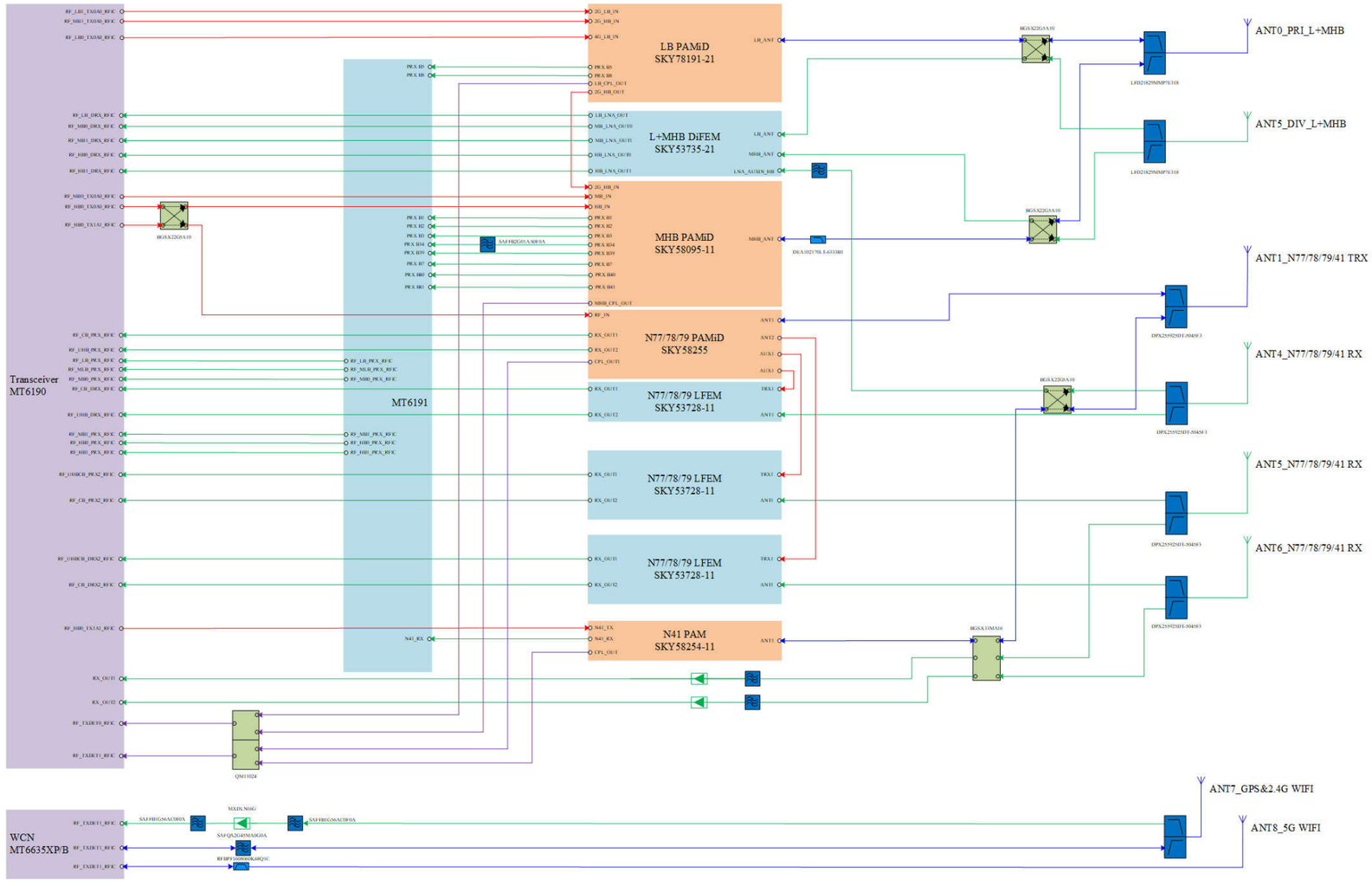
101.RF_Block

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

RF Block Diagram



Title	101.RF_Block		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size Custom
DEPARTMENT:	RF	DESIGNER:	Xue Wei
	WINGTECH		
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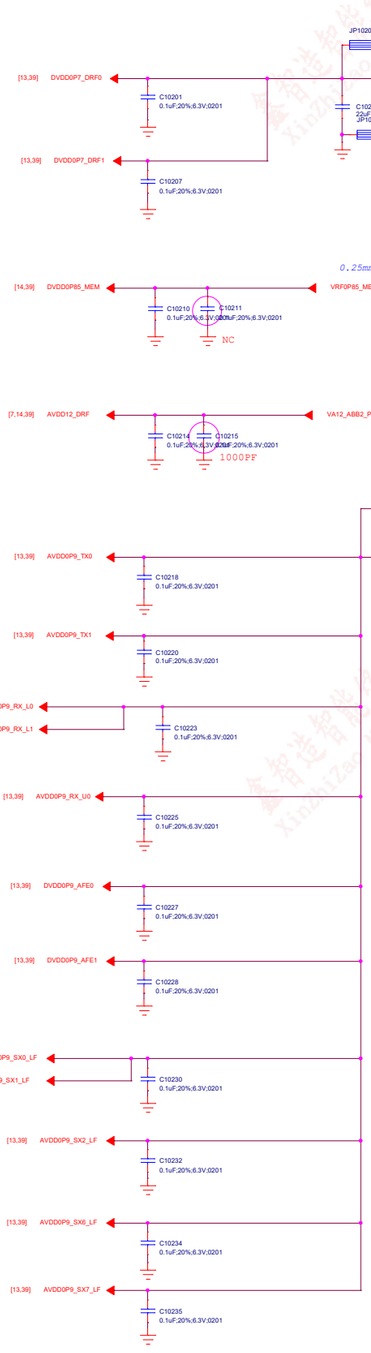
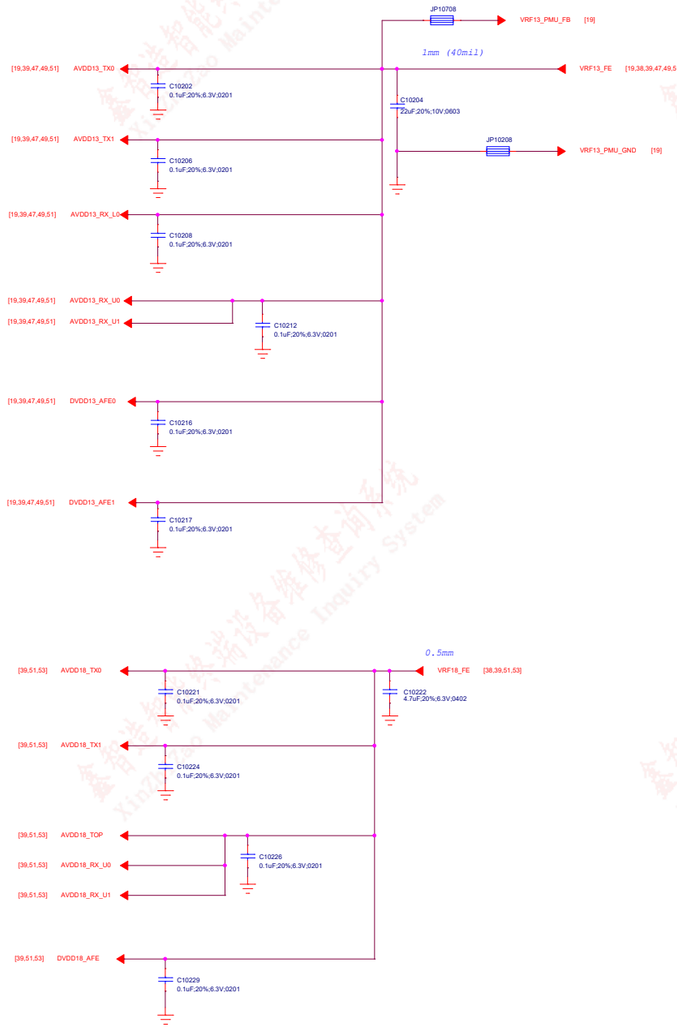
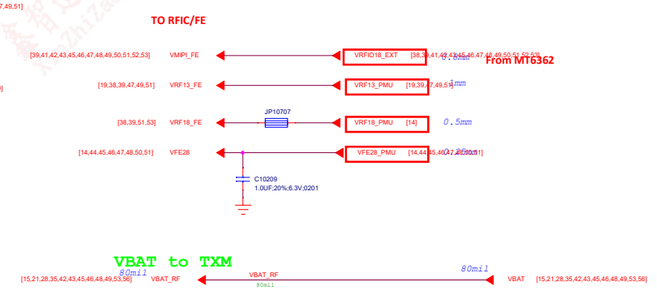
102.RF_Transceiver_MT6190M_Power

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

Power Supply of Transceiver







Title	102.RF_Transceiver_MT6190M_Power
DOCUMENT NO.:	98812_1_12M13_20210317_2112
DEPARTMENT:	RF
DESIGNER:	Xiao Wei
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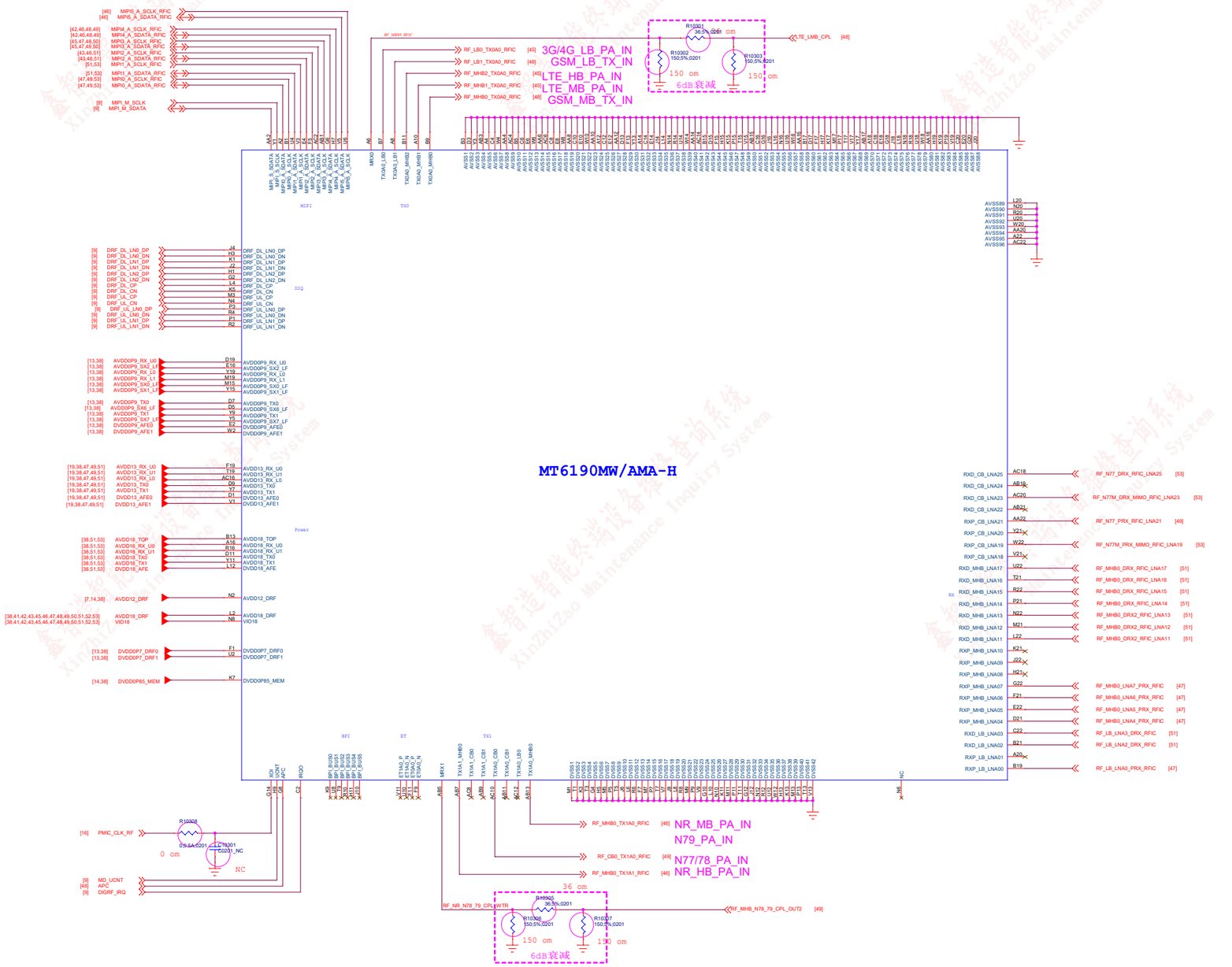
1	LAST_EDITOR	2-23-2007_10:06

103.RF_Transceiver_MT6190M

Transceiver MT6190M

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		



Title	103.RF_Transceiver_MT6190M		V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112	Size	Custom
DEPARTMENT:	RF	DESIGNER:	Xue Wei
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104.RF interface

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

Title	104.RF interface		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size Custom
DEPARTMENT:	RF	DESIGNER:	Xue Wei
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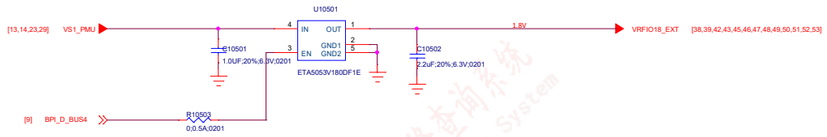
105_POWER_EXT

External VRFIO18_LDO



Title	105_POWER_EXT		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	BB	DESIGNER:	Ning Xinwu
WINGTECH			
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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
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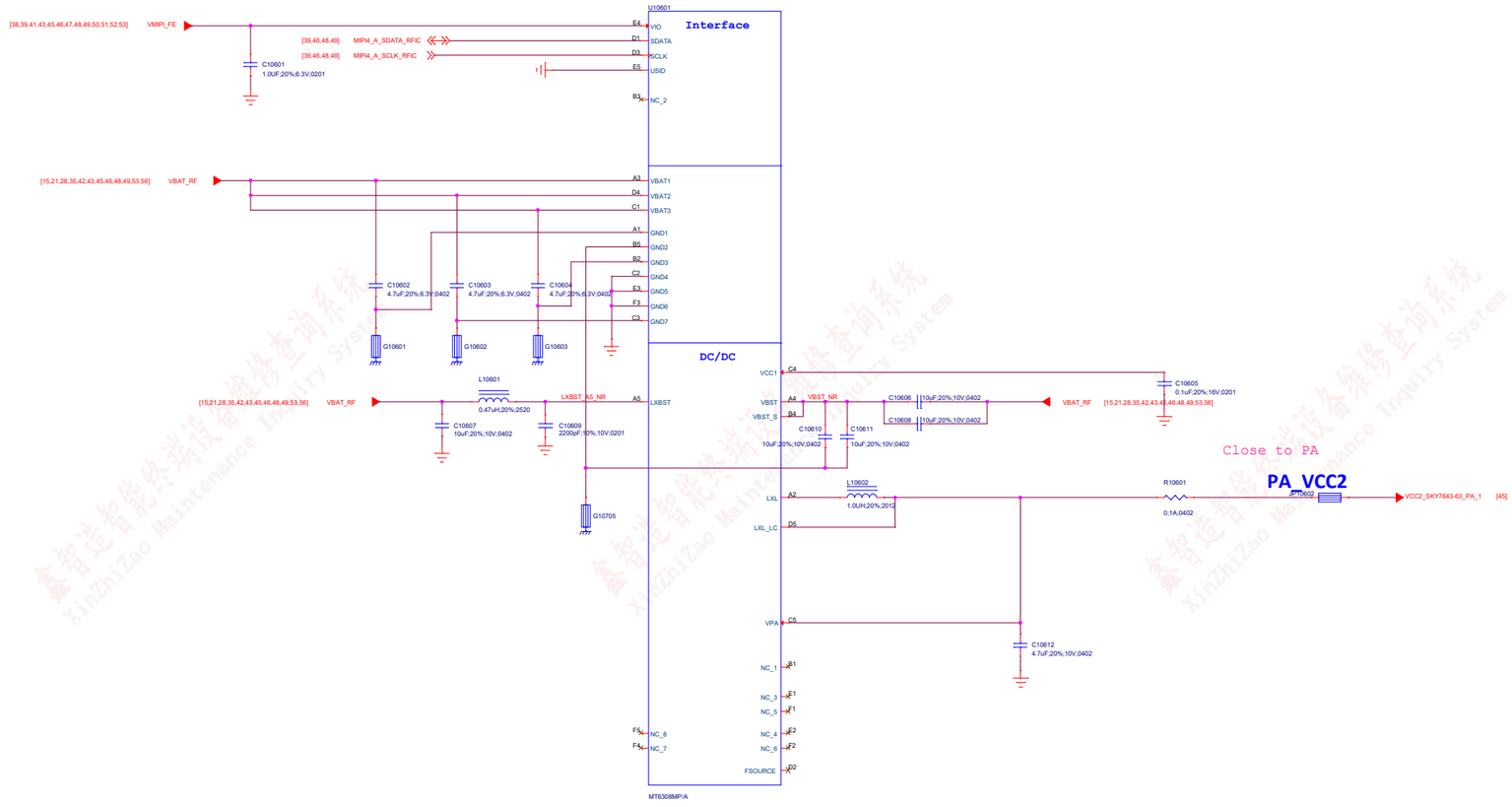
6308M_APT _1#



Title	106.APT/ET_Module_1	REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112	Size Custom
DEPARTMENT: RF		DESIGNER: Xue Wei
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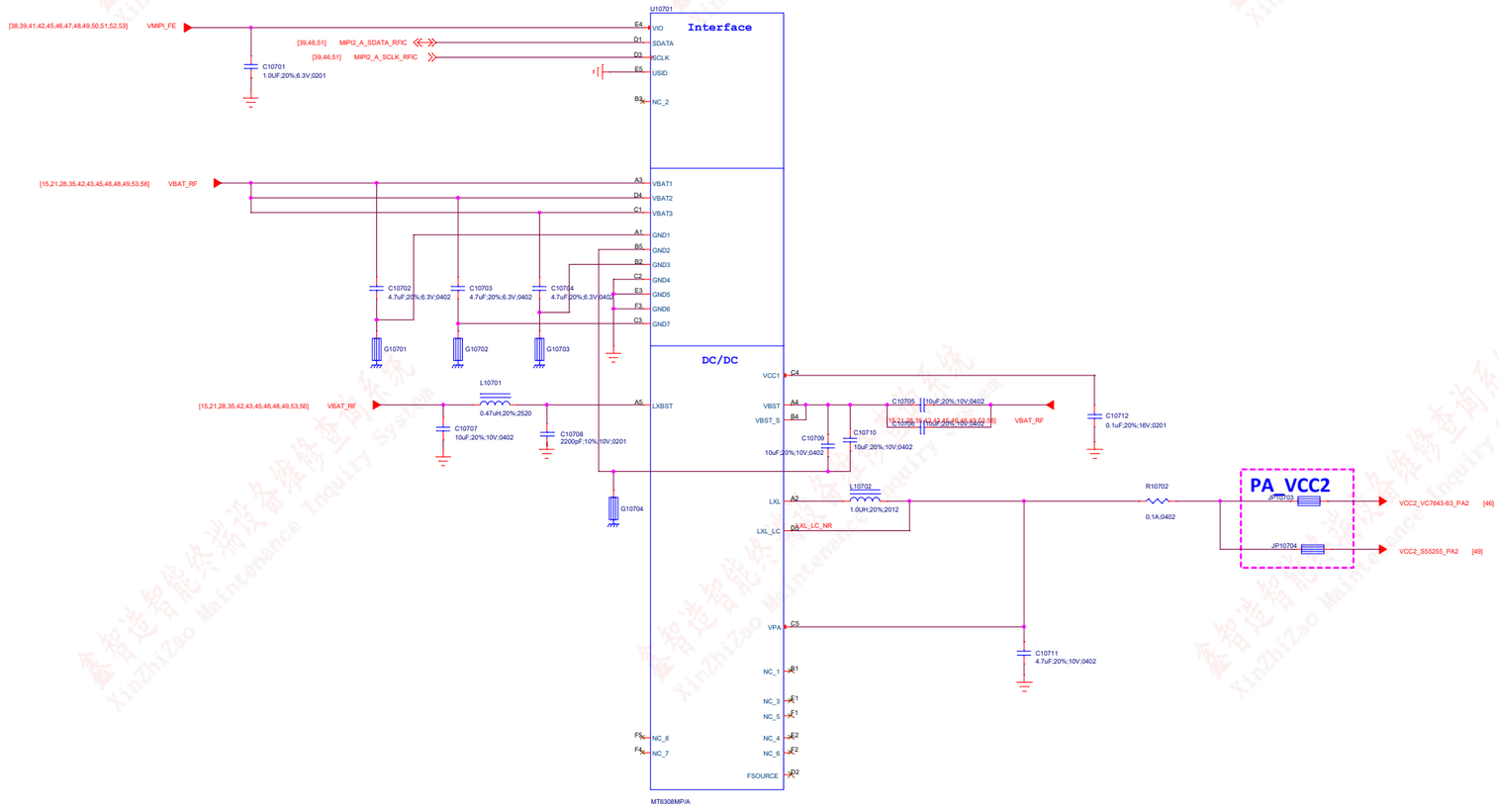
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		

6308M_APT _2#



Title	107.APT/ET_Module_2	REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112	Size Custom
DEPARTMENT: RF	DESIGNER: Xue Wei	
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B29 RX

B28A

change to B28B

B26

B5 双工

B12/17

B8

B13

B20

B13/14/29_TRX

Co_pad

B25/66

B1/3

B34/39_RX

B34/39

B7

B30

Title	108.VC7643-63P1_LTE_LMHF_TRX
DOCUMENT NO.:	96812_1_I2M13_20210517_2112
Size	E
DEPARTMENT:	RF
DESIGNER:	Xue Wei
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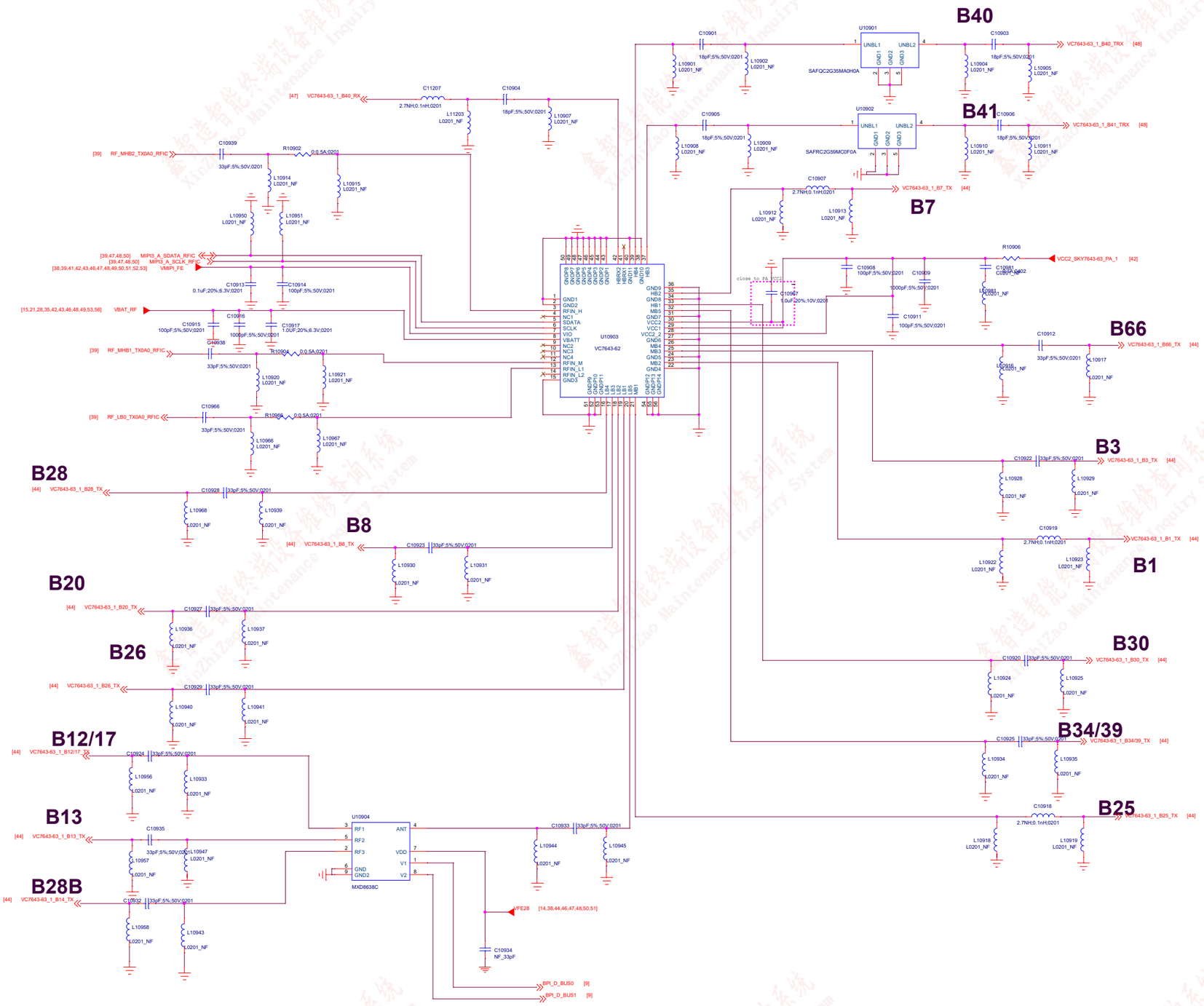
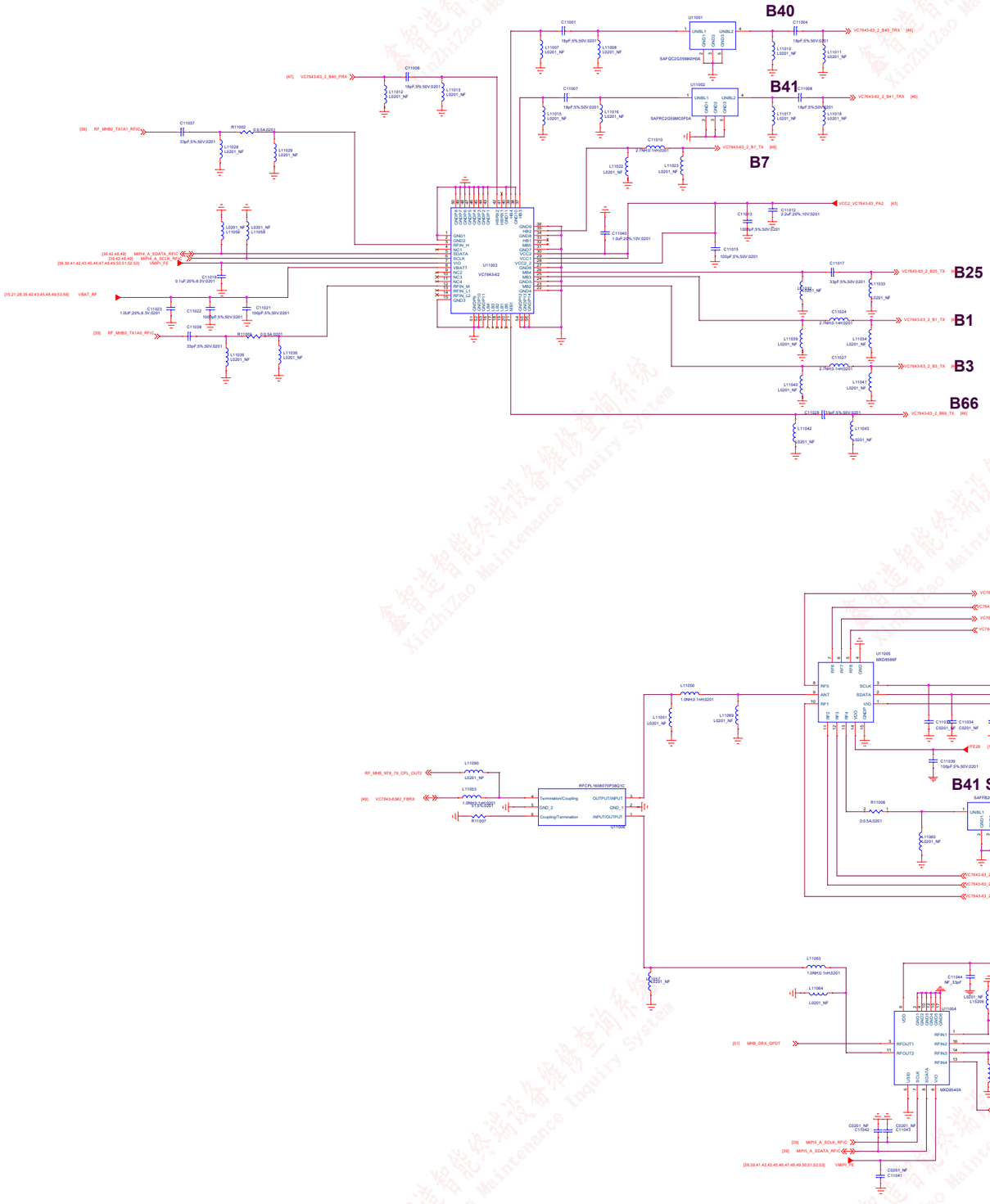
109.VC7643-62#1



110.VC7643-63#2



Title	110.VC7643-63#2_NR_MHB_TRX		REV:X10
DOCUMENT NO.:	98812_1_t3m13_20210512_2112	Size	E
DEPARTMENT:	RF	DESIGNER:	Ran shuping
WINGTECH			
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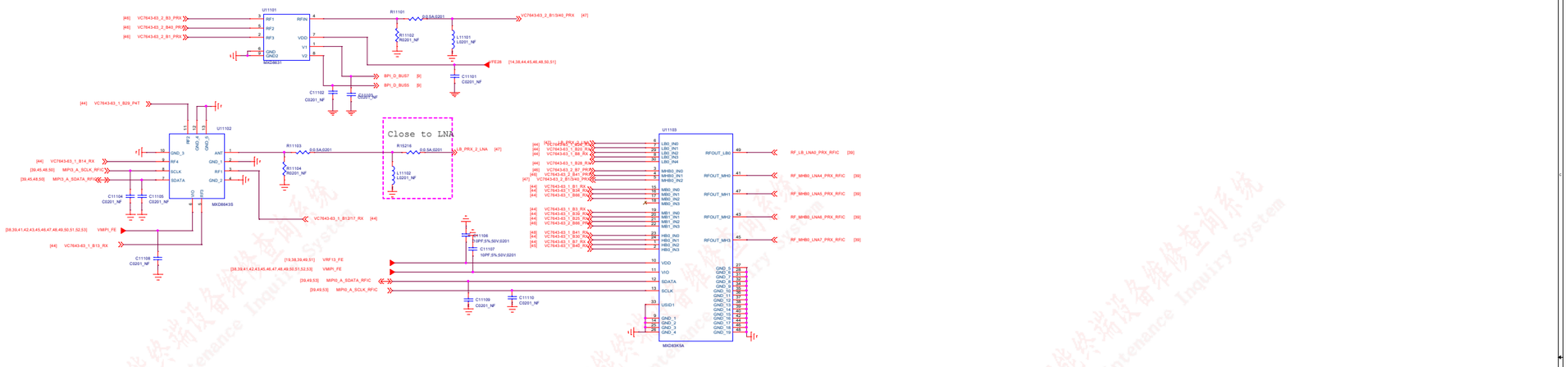
PRX_MXD83K5A



Title	111.PRX_LNA_BANK	REV: V10
DOCUMENT NO.:	96812_1_t3M13_20210517_2112	Size: E
DEPARTMENT:	RF	DESIGNER: Ren shuping
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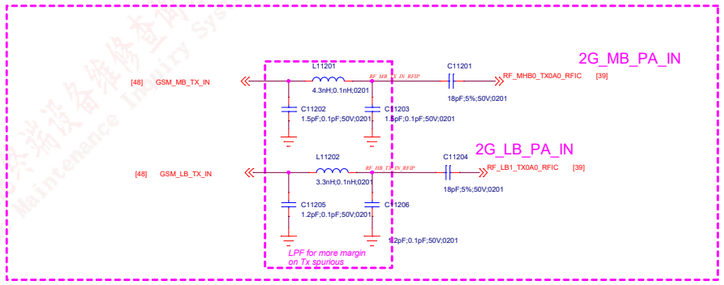
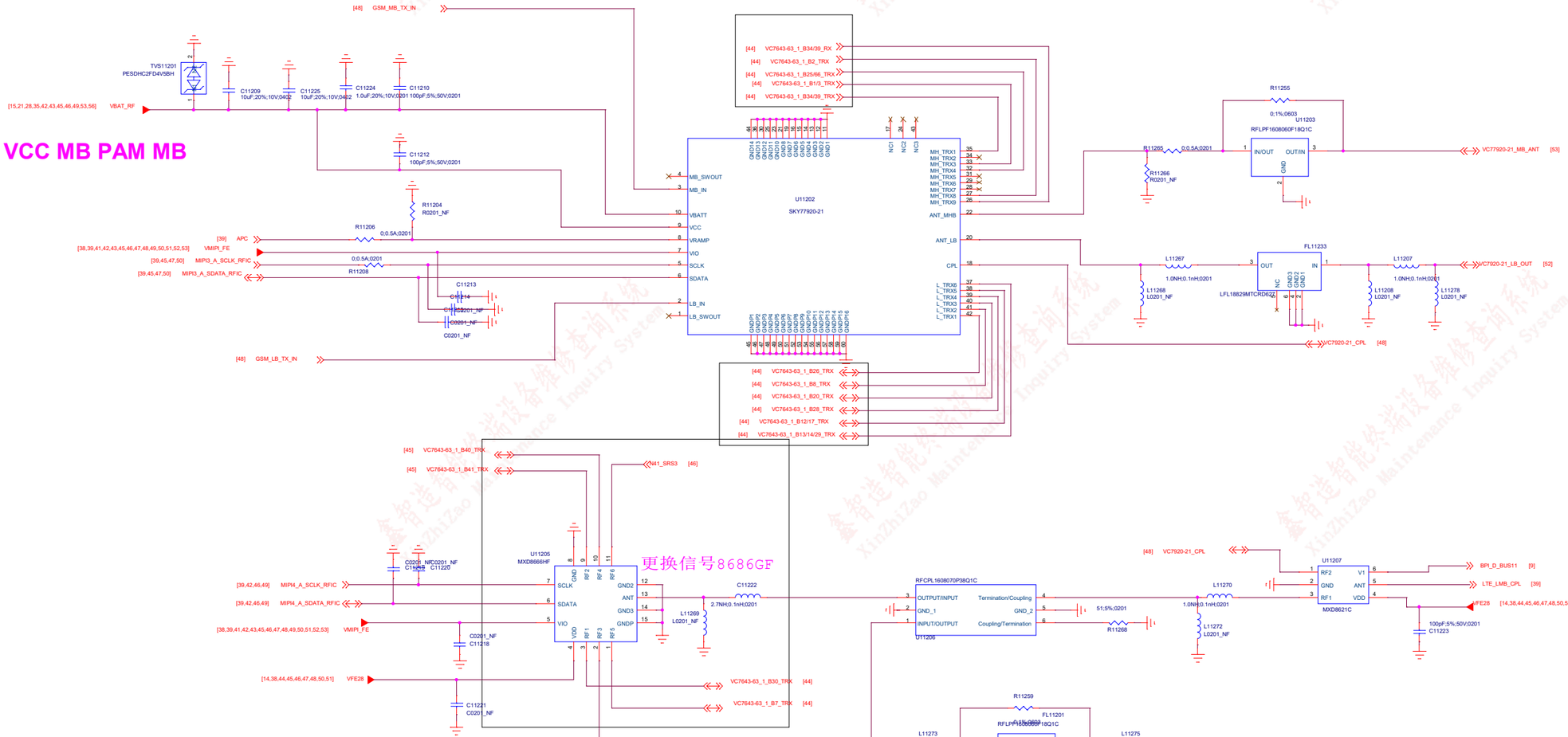
VC7920-21

TXM PA IN



VCC MB PAM MB



B41_PRX

Title	112.VC7920-21		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	RF	DESIGNER:	Ren shuping
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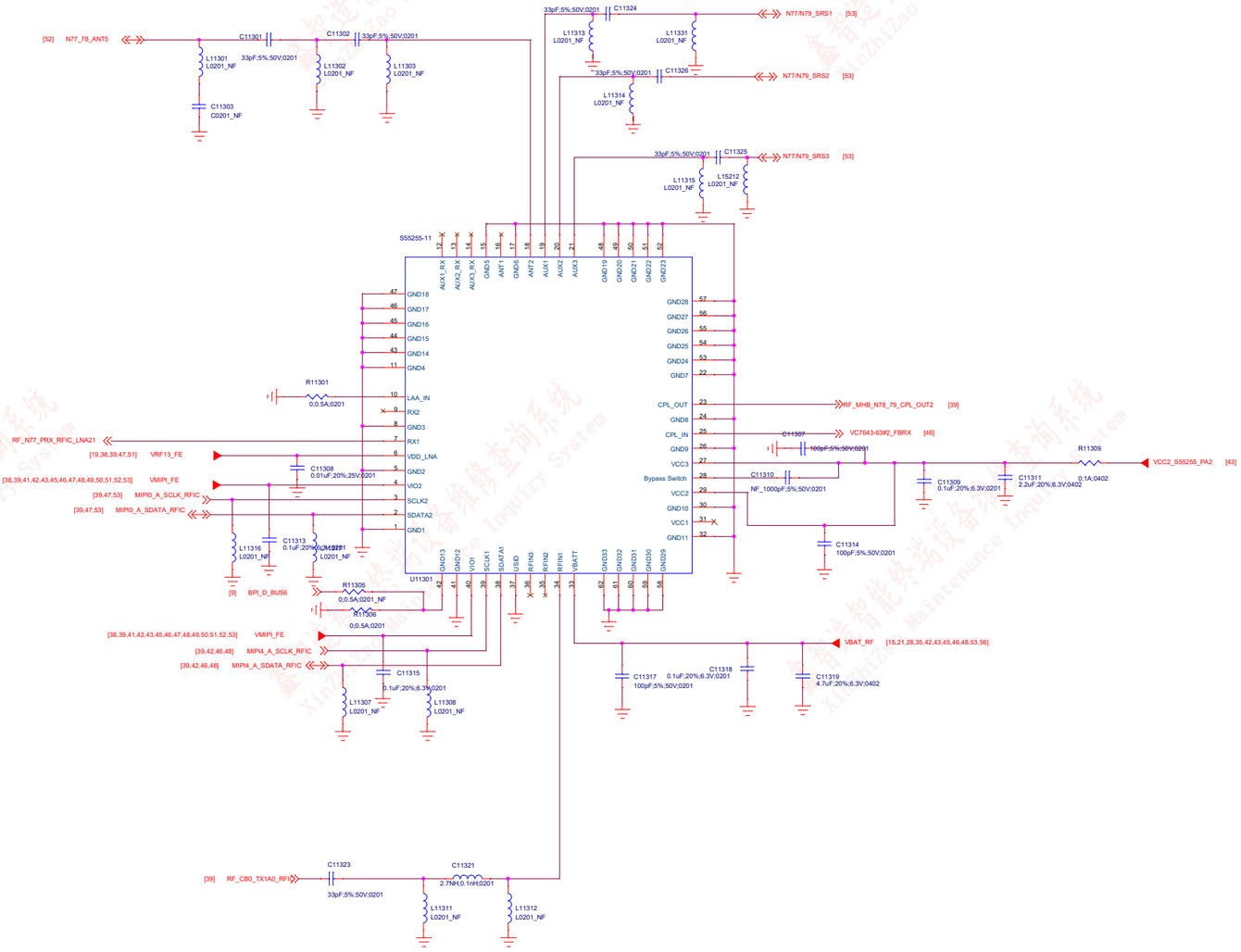
B48/N77/79_TRX



Title	113.N77/78 TRX		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	RF	DESIGNER:	Ren shuping
WINGTECH			
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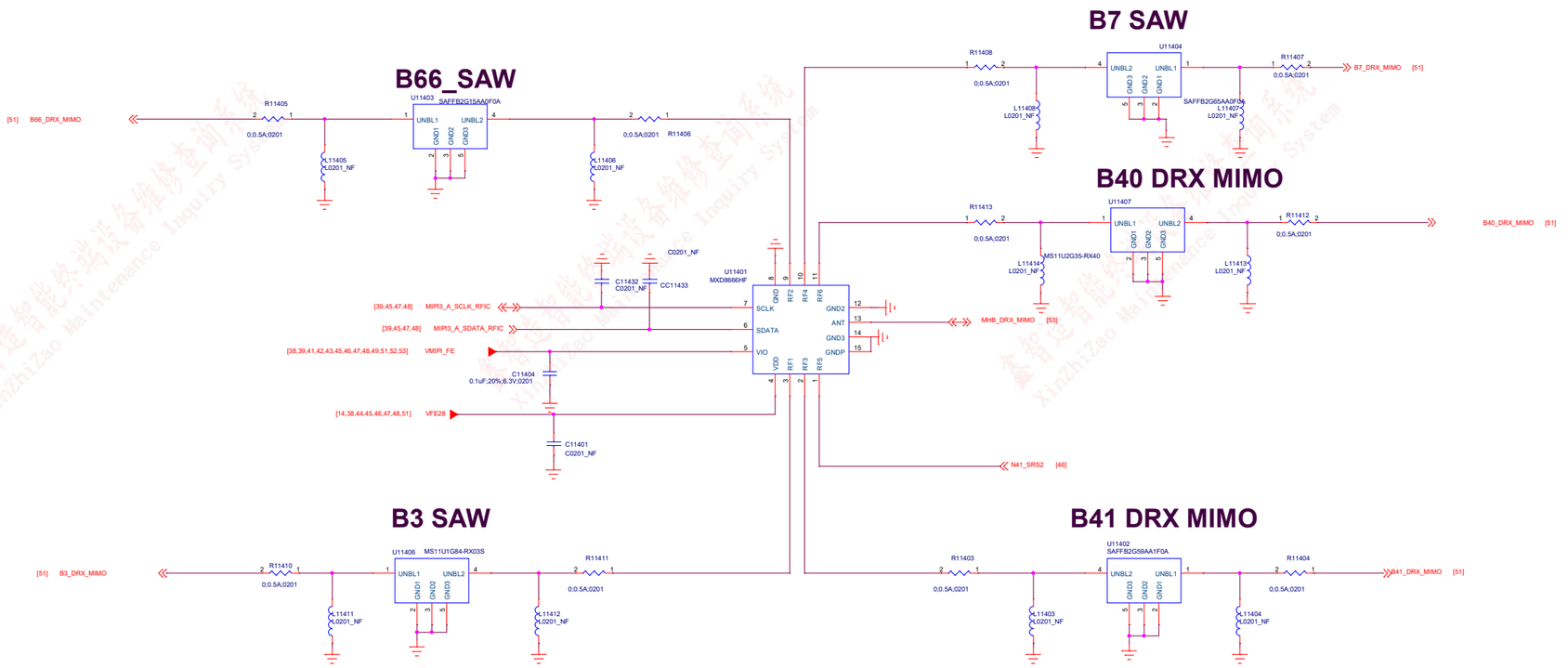
MHB_DRX_MIMO



Title	114.MHB_DRX_MIMO		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	RF	DESIGNER:	Ren shuping
WINGTECH			
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B25/66_DRX

B2_DRX

Co_PAD

Co_PAD

B30_DRX

B28/B71_DRX

B20_DRX

B12/13_DRX

B14_DRX

B29_DRX

Title	115.DRX
REV:	V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112
Size	D
DEPARTMENT:	RF
DESIGNER:	Ren shuping
Date:	Wednesday, March 17, 2021
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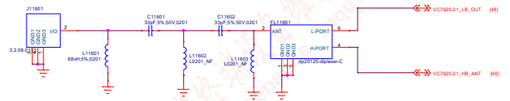
ANT0



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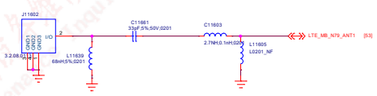

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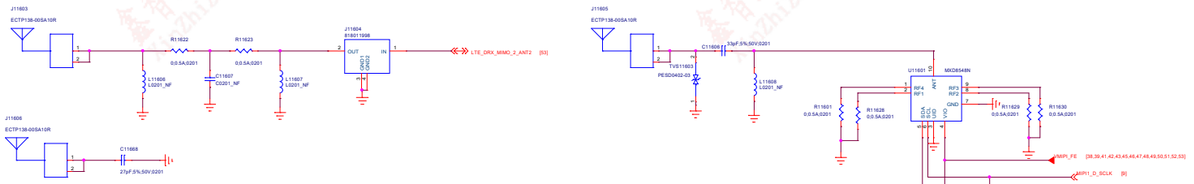

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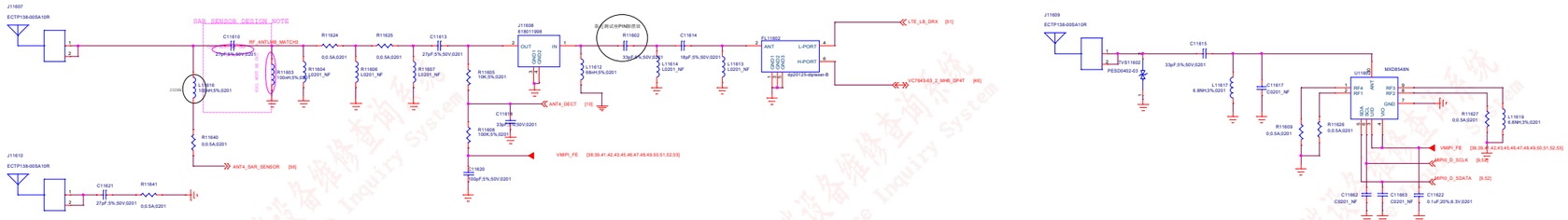

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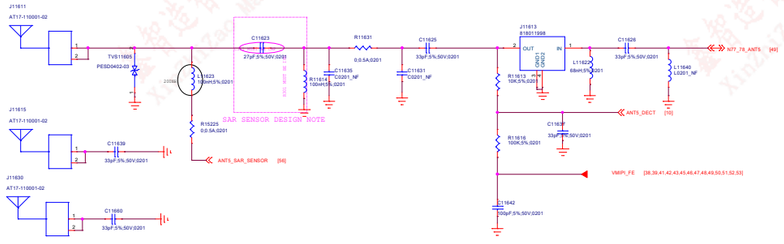

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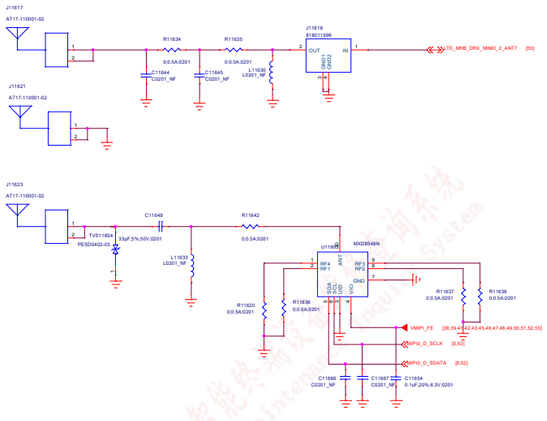

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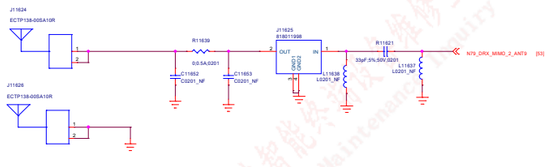

Title	116.ANT	REV:	V10
DOCUMENT NO.:	98012_1_120413_20210517_2112	Size:	E
DEPARTMENT:	RF	DESIGNER:	Ren shuping
WINGTECH			
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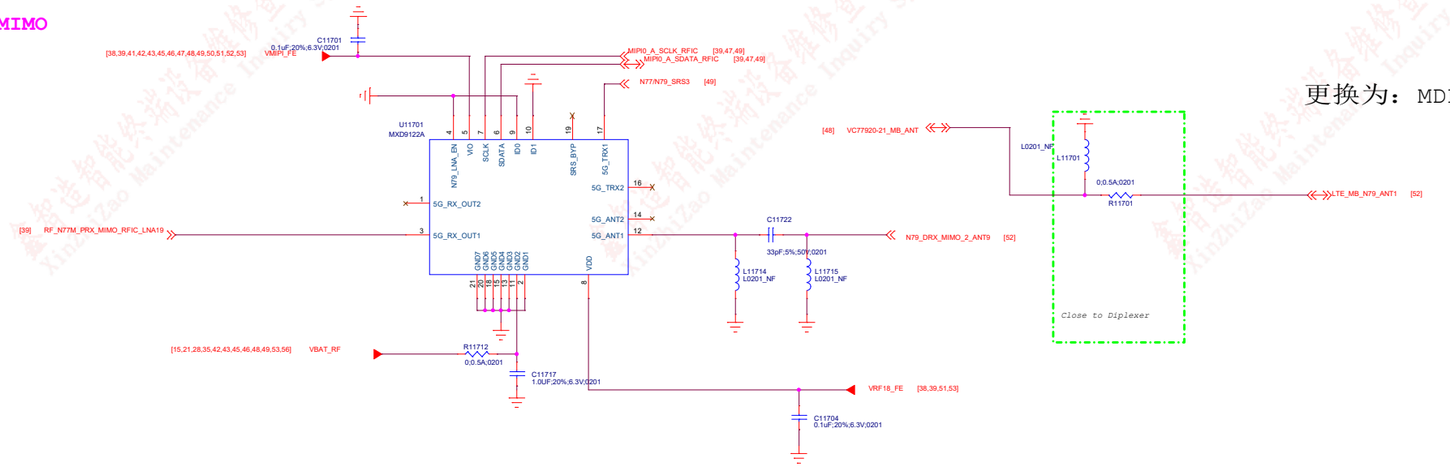
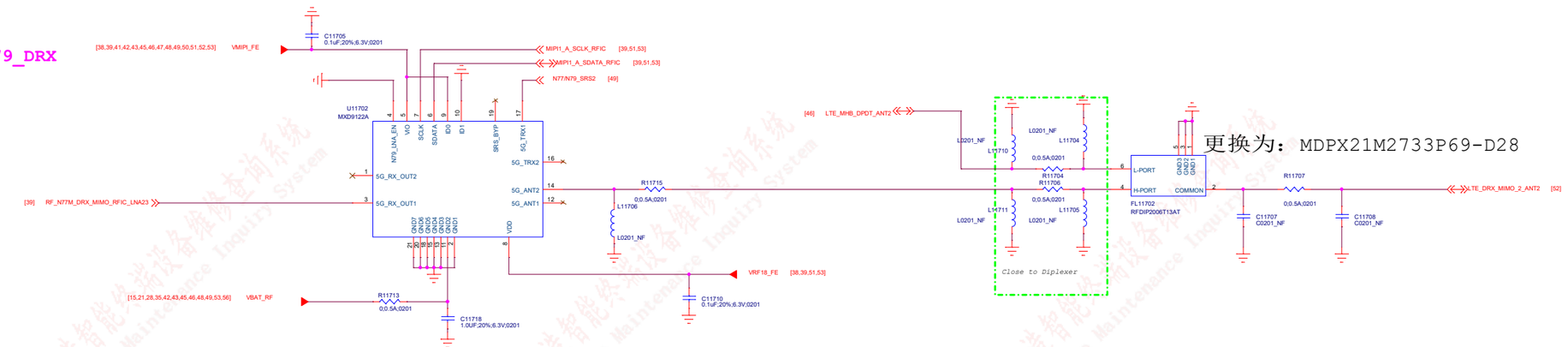
N77\79_PRX_MIMO



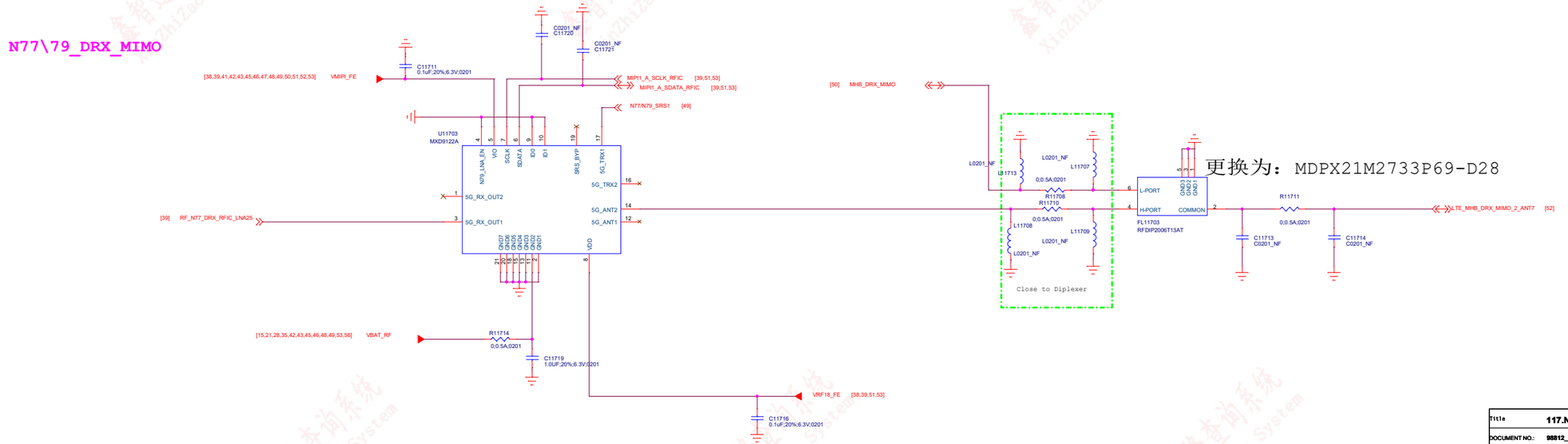
更换为：MDPX21M2733P69-D28

N77\79_DRX



更换为：MDPX21M2733P69-D28

N77\79_DRX_MIMO



更换为：MDPX21M2733P69-D28

Title	117.N77/79_MIMO		REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112		Size D
DEPARTMENT:	RF	DESIGNER:	Ren shuping
WINGTECH			
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Title	118.XXXXXX	REV: V10
DOCUMENT NO.:	98812_1_12M13_20210317_2112	Size D
DEPARTMENT: RF	DESIGNER: Xue Wei	
WINGTECH		
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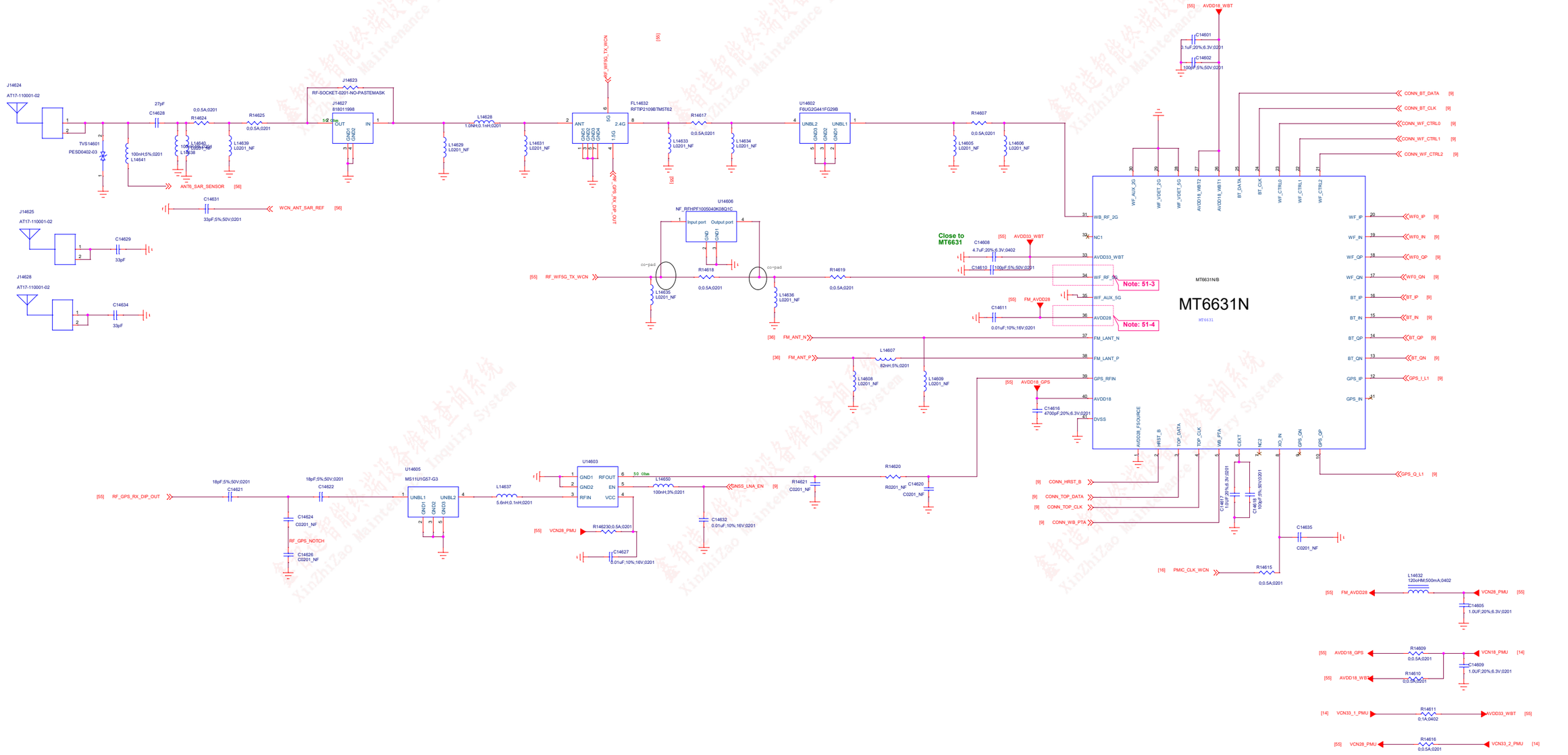
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	INITIAL RELEASE		



Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"

Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6762 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support
Note 51-5:	If WiFi 5G were no need, VCN33 could be chosen from PMIC output (VCN33_PMU)

Title	146.WCN_MT6631		REV: V10
DOCUMENT NO.:	98812_1_12813_20210317_2112		Size: Custom
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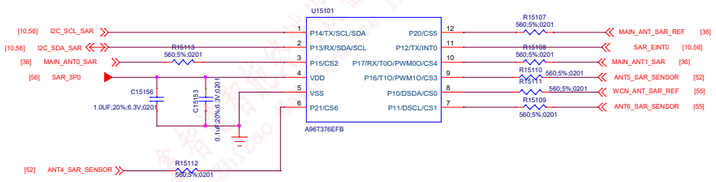
VERSION	EDITED BY	LAST EDIT DATE
1	LAST_EDITOR	2-23-2007_10:06

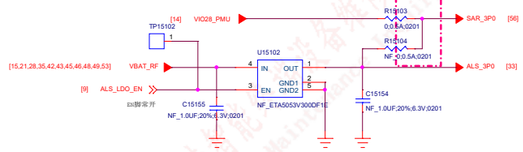
151.Sar_sensor

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE		

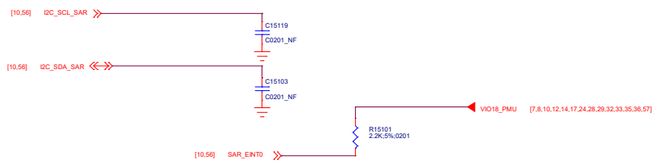
SAR SENSOR



CO-PAD



SAR_Control & Pull-up



Title: 151.Sar_sensor		REV: V10
DOCUMENT NO.: 98812_1_12M13_20210317_2112		Size: Custom
DEPARTMENT: WINGTECH-XA	DESIGNER: Xue Wei	
WINGTECH		
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1	LAST_EDITOR	2-23-2007_10:06

NFC

NFC Indication

NFC Config	NFC RID
NO NFC	R1538
With NFC	R1522

SIM Voltage Configuration

For 1st SIM	For eSM	For 2st SIM
SIMVDD1 EXT	SIMVDD2 EXT	SIMVDD3 EXT
SIMVDD1	SIMVDD2	SIMVDD3

Title	82_NFC
REV:	V10
DOCUMENT NO.:	Design Name
Size	D
DEPARTMENT:	WINGTECH-SH
DESIGNER:	liufenglei
Date:	Wednesday, March 17, 2021
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