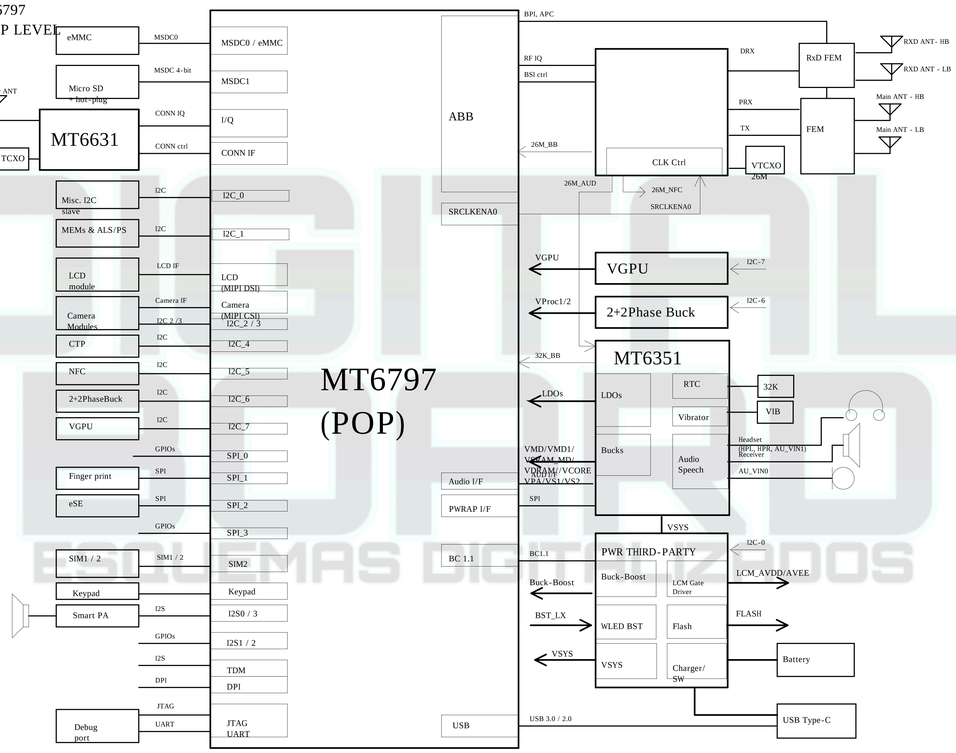
CX880

REVISION RECORD			
LTR	ECO NO.:	APPROVED:	DATE:

Project : MT6797
REF_SCH TOP LEVEL



猎人电子图

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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 1 OF 20	

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I2C	Function	I2C Spec.[1]	Budgeted Timing	I2C Slave Address (7-bit mode)
I2C-0 *[2]	SW charger	400 Kbps		bq25896 / SW charger I2C address: 0X6B (Write:0xD6, Read:0xD7)
	LCM Gate Driver	400 Kbps		NT50358 / LCM Gate Driver I2C address: 0X3E (Write:0x7C, Read:0x7D)
	Buck-boost	400 Kbps		FAN49101 / Buck-boost I2C address: 0X70 (Write:0xE0, Read:0xE1)
	Flash LED Driver	400 Kbps		LM3643 / Flash LED I2C address: 0X63 (Write:0xC6, Read:0xC7)
	Speaker Amp.	400 Kbps		MAX98926EWV+T / Speaker AMP I2C Address: 0x31 (Write:0x62, Read:0x63) when ADDR = GND. MAX98926EWV+T / Speaker AMP I2C Address: 0x34 (Write:0x68, Read:0x69) when ADDR = VIO18.
	USB Type-C CC	400 Kbps		FUSB302 / USB Type-C channel configure I2C Slave Address:0x22, write:0x44, read:0x45) or FUSB302 / USB Type-C channel configure I2C Slave Address:0x23, write:0x46, read:0x47)
	MHL	400 Kbps		SI8348 / CI2CA Low:MHL I2C Address =0x39/3D/4D/64/48/60.(Write:0x72/7A/9A/C8/92/C0, Read:0x73/7B/9B/C9/93/C1)
I2C-1 *[2]	M Sensor	400 Kbps		AK09912 / M-Sensor I2C Address 0xOC (Write: 0x18, Read: 0x19)
	A+Gyro Sensor	400 Kbps	Yes.	ICM-20645 / A+Gyro I2C Address: 0x68 (Write:0xD0, Read:0xD1)
	Baro Sensor	400 Kbps		BMP280 / Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)
	RGB / PS Sensor	400 Kbps		CM36558 / ALPS + UV I2C address: 0X51 (Write:0xA2, Read:0xA3)
	Humidity Sensor	400 Kbps		HTS221 / Humidity I2C address: 0X5F (Write:0xBE, Read:0xBF)
I2C-2	Rear camera	400 Kbps	Yes.	OV23850 / Rear camera I2C address: 0X36 (Write:0x6C, Read:0x6D) if SID = low. OV23850 / Rear camera I2C address: 0X10 (Write:0x20, Read:0x21) if SID = high.
	Rear camera's AF	400 Kbps		LC898212XD-SH / AF driver I2C address: 0X72 (Write:0xE4 Read:0xE5)
I2C-3	2nd front camera (Fixed Focus)	400 Kbps	Yes.	S5K5E2 / Rear camera I2C address: 0X10 (Write:0x20, Read:0x21); It can be changed by register[7:1] of addr 0x0107.
	Front camera	400 Kbps	Yes.	S5K3M2XXM3 / Front camera I2C address:0X2D (Write:0x5A, Read:0x5B);
	Front camera's AF	400 Kbps	Yes.	DW9714A / AF driver I2C address: 0X0C (Write:0x18, Read:0x19)
I2C-4	CTP	400 Kbps	Yes.	GT1511 / CTP I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0X14 (Write:0x28, Read:0x29)
I2C-5	NFC	1.3 Mbps	Yes.	MT6605 / NFC I2C address: 0X28 (Write:0x50, Read:0x51)
I2C-6	VPROC buck	3.4 Mbps	Yes.	MT6313 / 2+2Phase Buck I2C address: 0X6B (Write:0xD6, Read:0xD7)
I2C-7	VGPU Buck	3.4 Mbps	Yes.	FAN53555 / Buck I2C address: 0X60 (Write:0xC0, Read:0xC1)

Note 1: I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

Note 2: For MEMs sensor/sensor hub application, these I2C slave devices must be connected to I2C0 or I2C-1.

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Schematic design notice of "10_BB_POWER_1" page.

Note 10-1:
Note 10-2:
Note 10-3: Differential pairs of buck's remote sense must be placed at PCB back side right beneath MT6797 chip.
Note 10-4:

Note 10-5: For PCB layout, the star connection should be implemented in the MT6351's VIO18 output.

The purpose of this symbol is used for including POP LPDDR3 in BOM.

POP_DDR_
U - H9CKNNNDATMBPR

Schematic design notice of "11_BB_POWER" page.

Note 11-1: Reserve 1uF capacitor in VCC18IO0 for MHL.

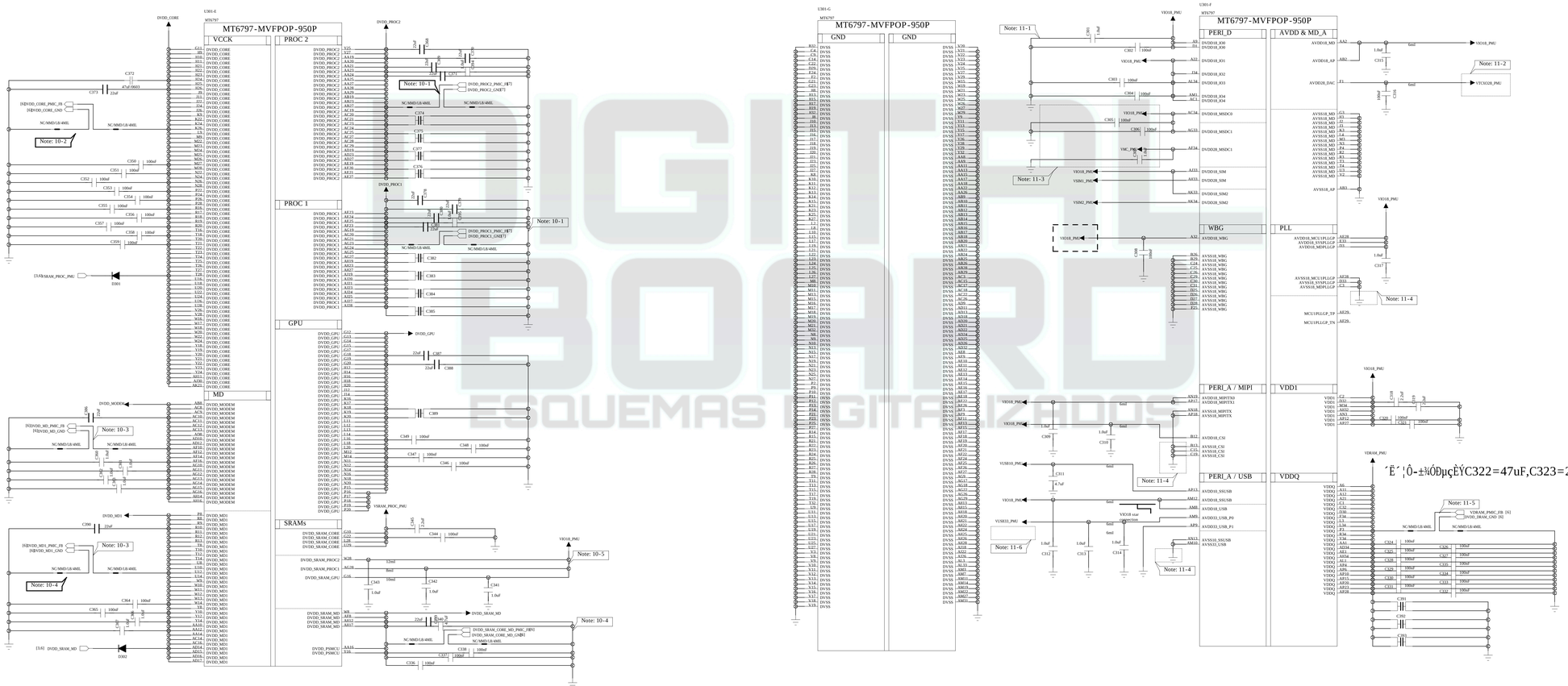
Note 11-2: AVDD28_DAC (F1 ball) must be powered by "VTCXO28_PMU".

Note 11-3: The placement of power/de-coupling capacitors of DVDD18_MSDC0/1 &DVDD28_MSDC1should be placed as close to power ball as possible and connect to GND directly.

Note 11-4: Connect AVDD33_USB_P1 to "VUSB33_PMU" for USB application; Connect AVDD33_USB_P1 to "VSIM1_PMU" for IC-USB / Samrt card application.

Note 11-5: Differential pair of VDRAM_PMU remote sense should be placed in the farest power plane from MT6351 point of view.

Note 11-6: Connect AVDD33_USB_P1 to "VUSB33_PMU" for USB application; Connect AVDD33_USB_P1 to "VSIM1_PMU" for IC-USB / Samrt card application.



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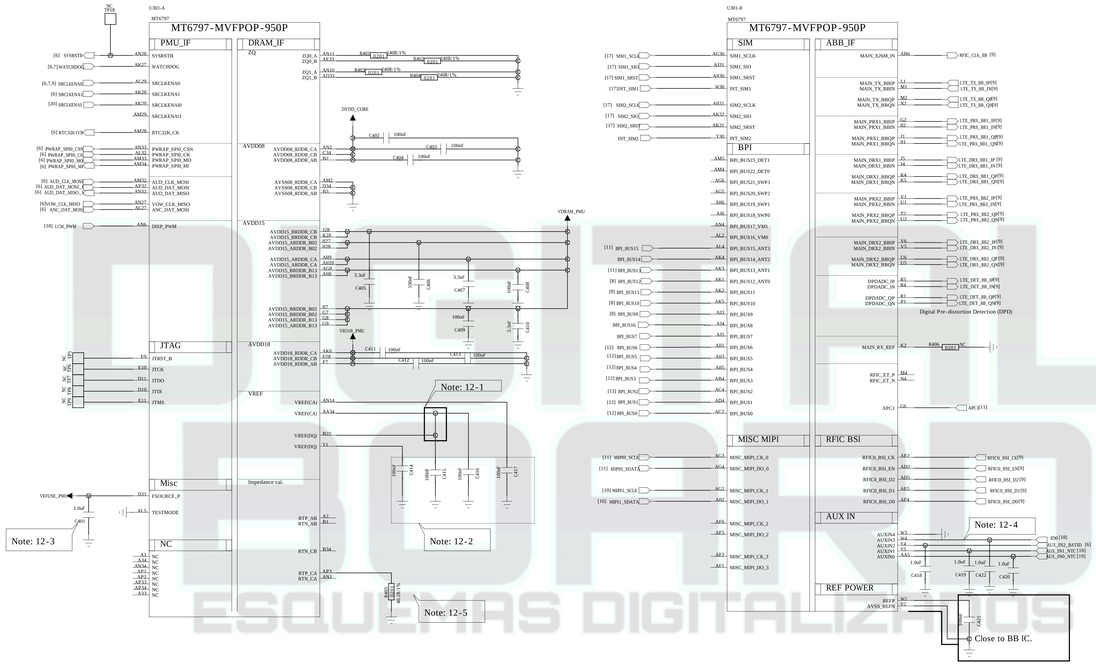

Schematic design notice of "11_BB_11" page.

Note 12-1:	The DRAM's VREF(CA)(AA34 ball) must connect to VREF(DQ)(B22 ball).
Note 12-2:	The de-coupling cap. of DRAM VREF have to be placed as close to BB as possible.
Note 12-3:	Apply 1.8V to FSOURCE_P (D31) for eFuse programming.
Note 12-4:	To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.
Note 12-5:	For impedance calibration of DDRPHY

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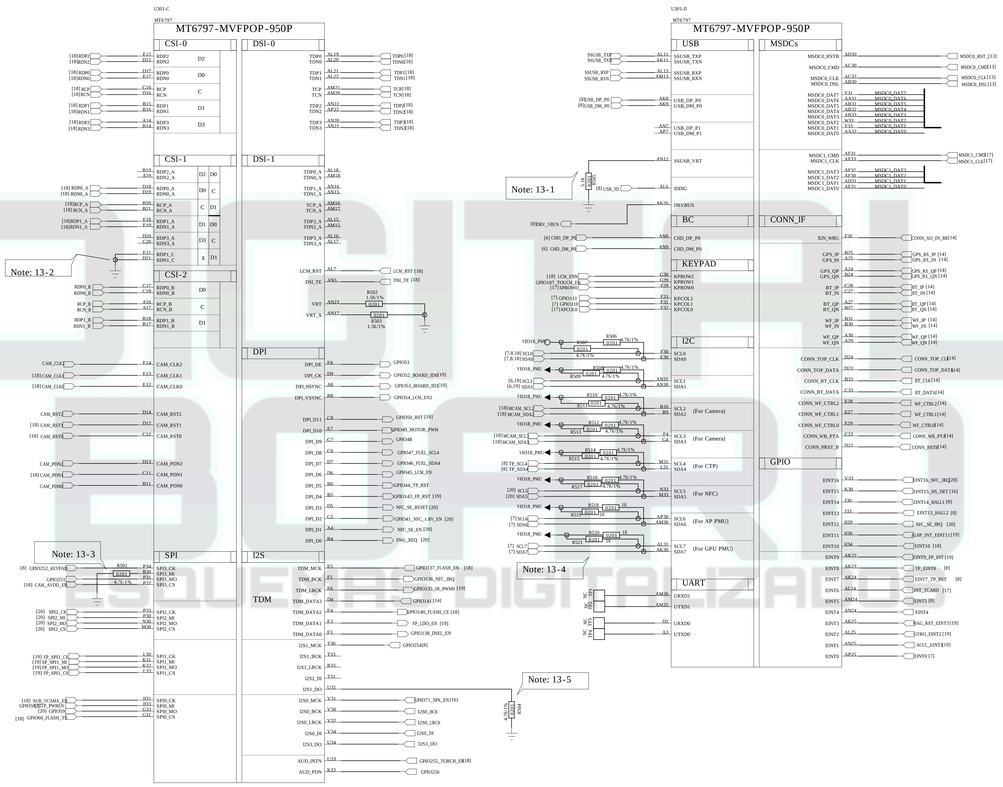

Schematic design notice of "12_BB_2" page.

Note 13-1:	Default resistor of "SSUSB_VRT" can be NC if internal USB VRT is applied.
Note 13-2:	Connect the the NC pins of CSI to GND
Note 13-3:	The GPIO250 can't have external pull-up. "C2K DROP_ZONE" output indicator is not allow to have external pull-up.
Note 13-4:	The I/O type of I2C6/7 is push-pull; External pull-up is required if I2C6/7 slave devices can only support open-drain.
Note 13-5:	The GPIO249 features I/O trap in system bootup that must be pulled down.

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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 5 OF 20

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VMODEM:0.5V~1.4V/1.2A

VGPU (to VDRAM):0.5V~1.4V/3A

VCORE:0.5V~1.4V/3A

VMD1:1V/1.2A

VSRAM_MD:0.8V~0.9V/1.2A

VS1:2V/2A

VS2:1.4V/2A

VPA:0.5V~3.4V/800mA

Schematic design notice of '21_POWER_MT6351_2' page.

Note 21-1:
Reserve 1.5K in order to give additional power to turn on charger LED driver while low battery.

Close to MT6351

Close to PMIC

Rfg > 0.5W

BATTERY CONNECTOR

ESD suggest <5pf

Read Address 0xCS
WriteAddress 0xC4

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CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
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SCALE: <Scale>	SHEET: 6 OF 20		

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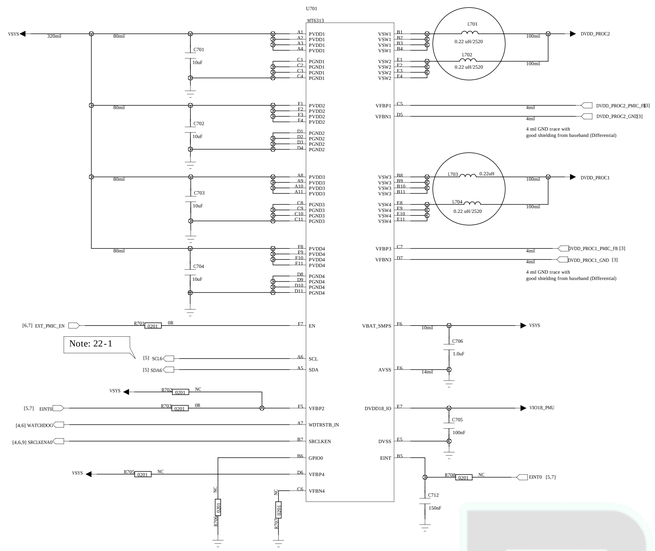
VPROC Buck

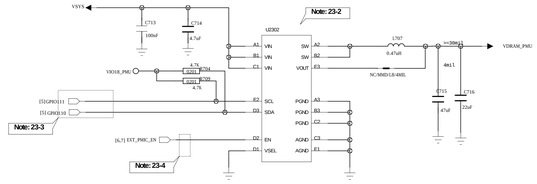


Schematic design notice of "22_POWER_2+2PHASE_BUCK" page.

Note 22-1: Buck EN is controlled by SRCLKEN0 or I2C

Buck for VDRAM

FAN53526 / Buck I2C address: 0X60 (Write:0xC0, Read:0xC1)



Schematic design notice of "23_POWER_VGPU_VM" page.

Note 23-2: BOM option to select MT6351's VGPU or 3rd party PMIC as VDRAM (1.2V) power

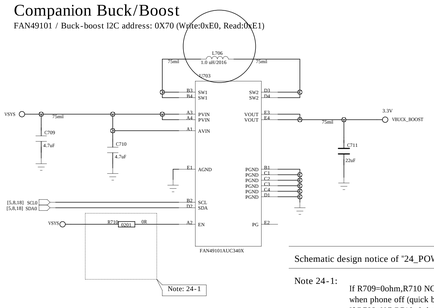
	U2302	PL2302	C2303	C2304	R2301	R2302
MT6351's VGPU as VDRAM	NC / DNI	NC / DNI	NC / DNI	NC / DNI	NC / DNI	NC / DNI
3rd party PMIC as VDRAM	FAN53526	0.47uF	0.1uF	4.7uF	4.7K	4.7K
Note: NC / DNI = No connect / Do not install.						

Note 23-3: Use pin muxed I2C-1 to control FAN53526 since its I2C base address is 0x60 same as VGPU and MHL.

Note 23-4: FAN53526's EN pin is driven by MT6351.

Companion Buck/Boost

FAN49101 / Buck-boost I2C address: 0X70 (Write:0xE0, Read:0xE1)

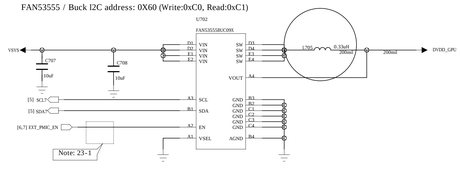


Schematic design notice of "24_POWER_THIRD-PARTY" page.

Note 24-1: If R709=0ohm,R710 NC,R5109=0ohm: MT6605 can't support card mode function when phone off (quick boot disable)
If R709=NC,R710=0ohm,R5109=0ohm: MT6605 can support card mode function when phone off(quick boot disable)

2-Phase Buck

FAN53555 / Buck I2C address: 0X60 (Write:0xC0, Read:0xC1)



Schematic design notice of "23_POWER_VGPU" page.

Note 23-1: FAN53555's EN pin is driven by MT6351.

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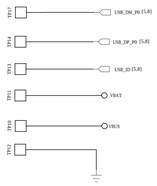
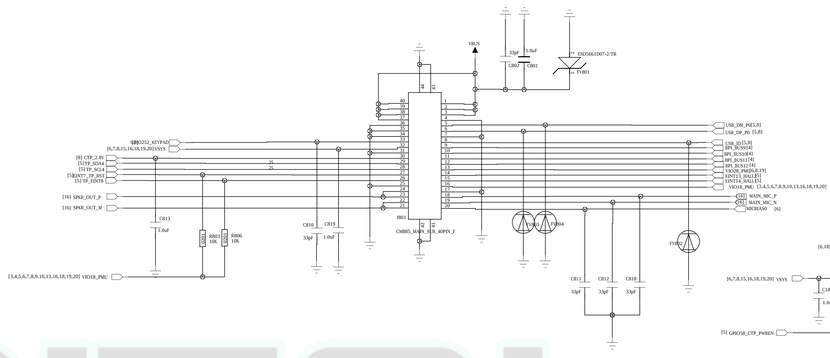
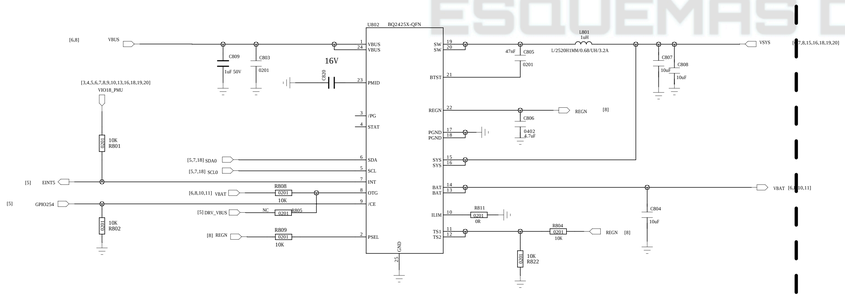




SW Charger / Power Path



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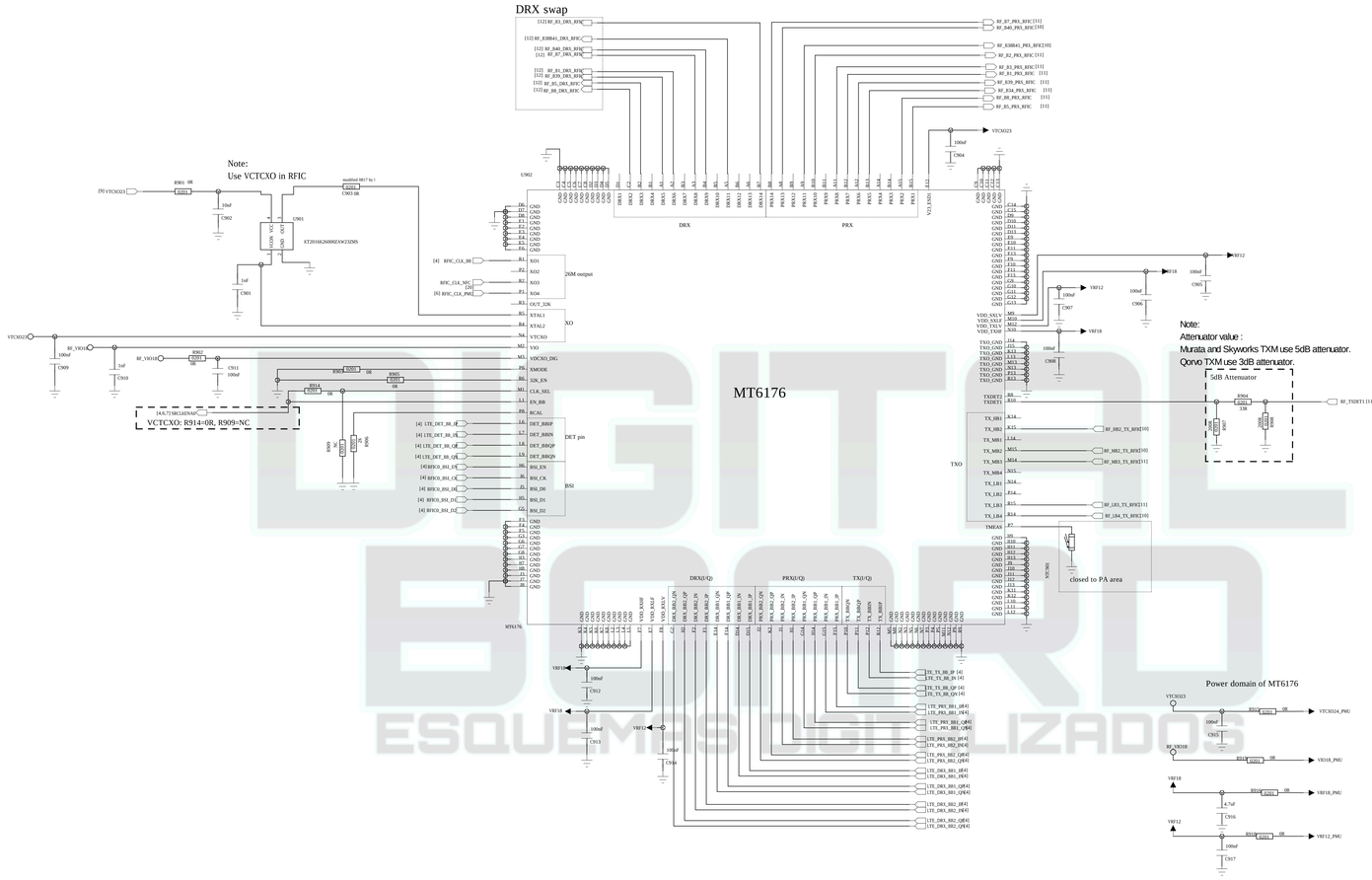

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B1/B2/B3/B5/B8/B28/ B7 / B34 / B39 / B38 / B40/ B41PA

B5

B8

B3

B2

B1

NO CA by xiaozhanglong

B41 TRX

B40 TRX

B7 TX

B38/B40/B41 BYPASS

4G PA input need LPF for harmonic rejection

3/4G_PAIN_LB

3/4G_PAIN_MB

3/4G_PAIN_HB

LPF for more margin on Tx spurious

Power Net Connection

VPA_VCC1 and VPA PMU need to be connected after Cap

VPA_VCC1 and VPA PMU need to be connected after Cap

For power LTE_VMIPI star connection

Thermister / To sense board level temperature

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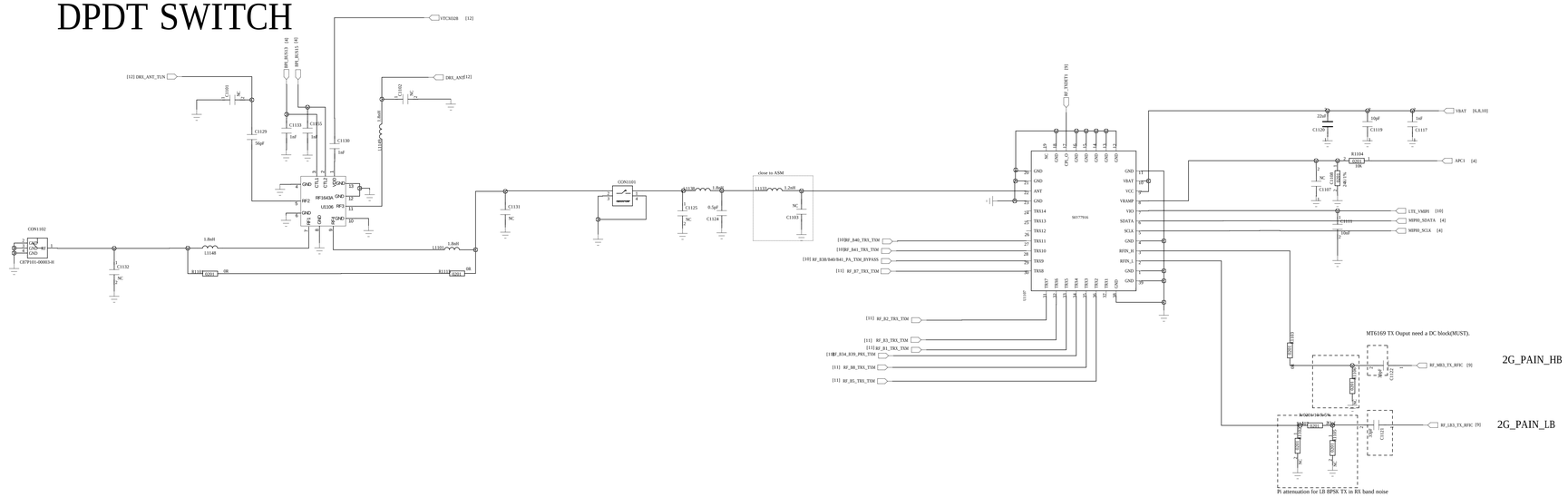
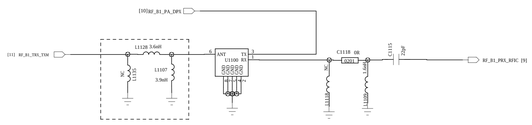
DPDT SWITCH



B1 TRX

no CA by xiaozhanglong

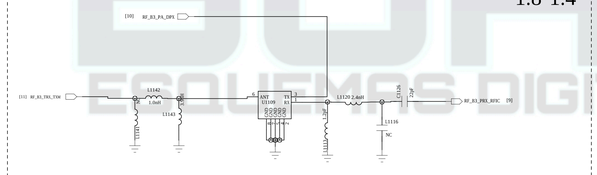


no CA new 20160413

B3 TRX

no CA by xiaozhanglong

1.8*1.4



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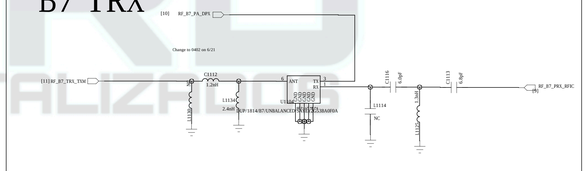

B2 TRX

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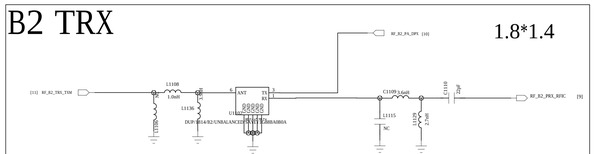

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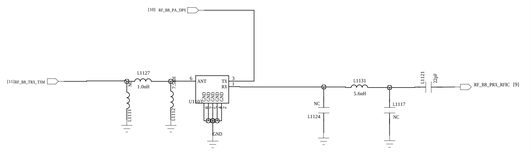

B5 TRX

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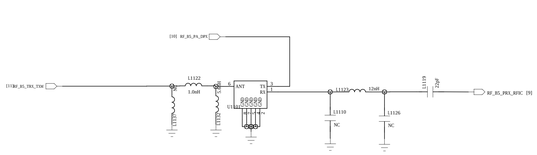
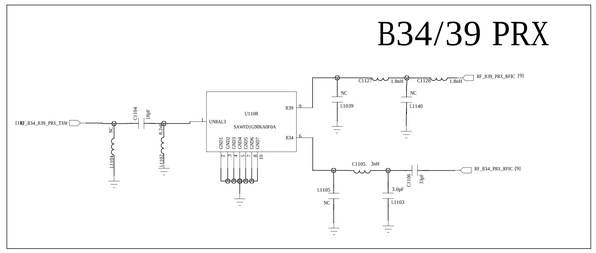


NO CA by xiaozhanglong

B34/39 PRX



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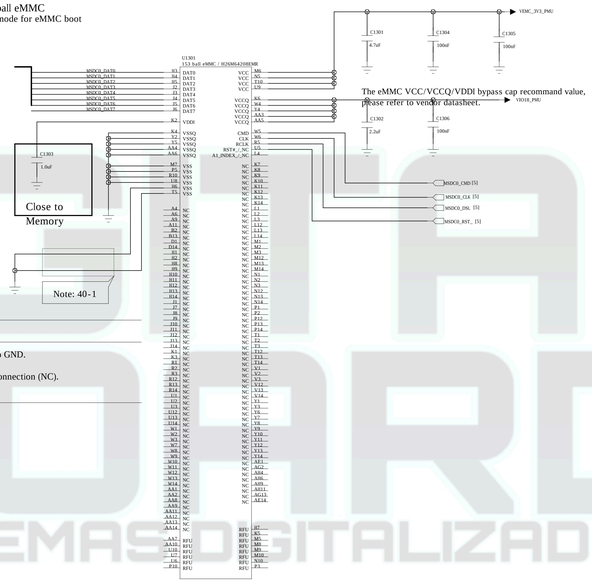
LTR	ECO NOs	APPROVED:	DATE:

169 ball eMMC
1 bit mode for eMMC boot



Schematic design notice of '40_MEMORY_eMMC" page.

Note 40-1: For eMMC 5.0/5.1, connect eMMC's H6 & T5 pin to GND.

For eMMC 4.5, check eMMC's H6 & T5 is real no connection (NC).

DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: LC	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: CX880	
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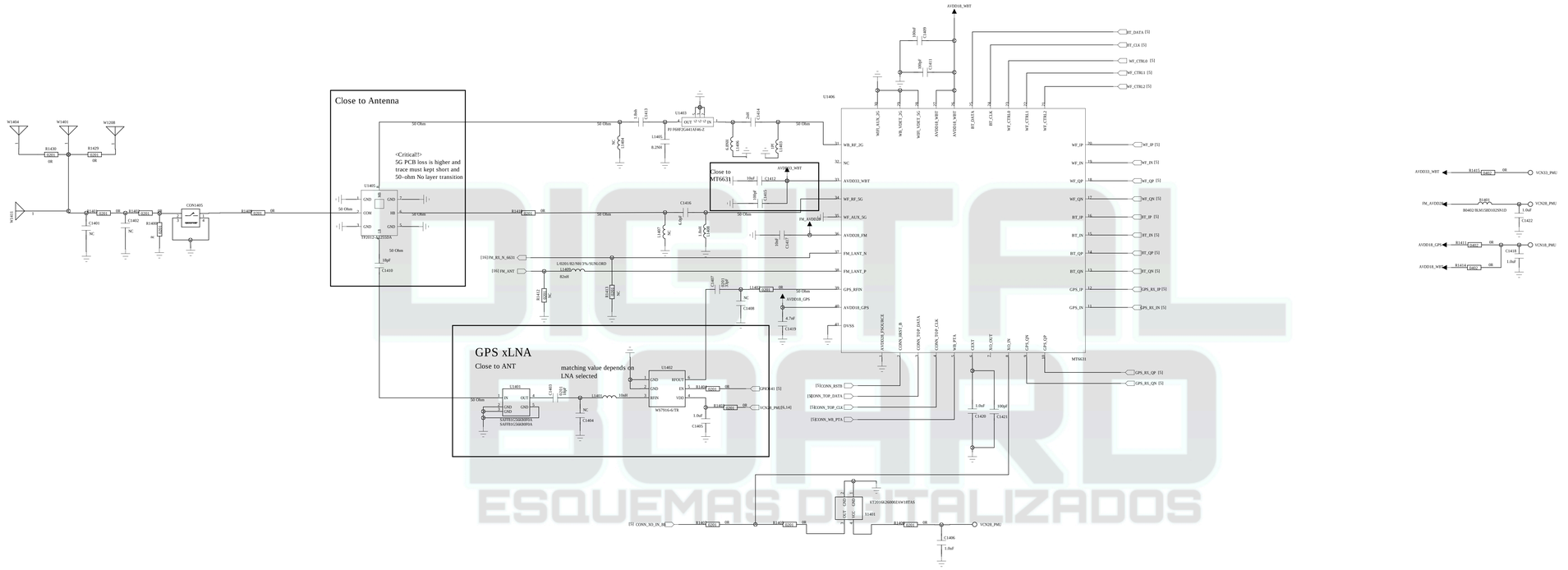
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
		SCALE: <Scale>	SHEET: 48 20

Wifi & GPS & FM

REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE:



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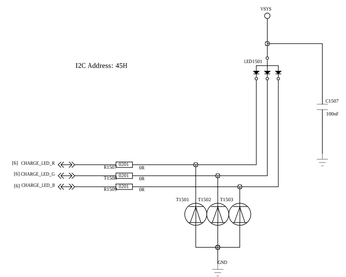
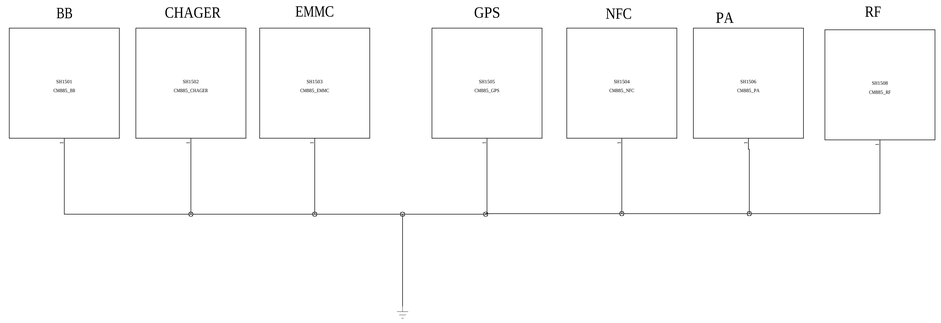
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 64 20

REVISION RECORD			
LTR	ECO NO.:	APPROVED:	DATE:

RGB LED

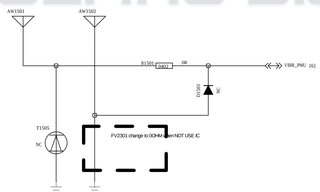
BlinkLED Driver





MOTOR DRIVER CIRCUIT

MOTOR CONTACT



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		TITLE: CX880				
DRAWN: <Drawn By>	DATED: <Drawn Date>					
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RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 46 20		

REVISION RECORD			
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MIC

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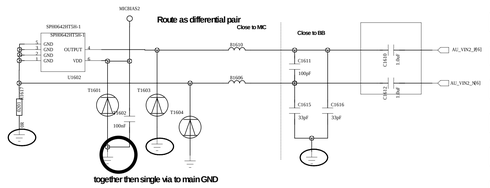
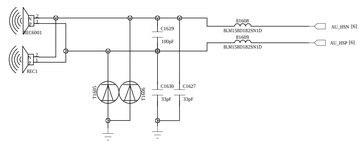
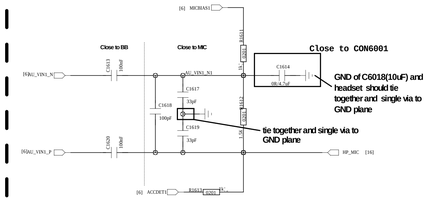


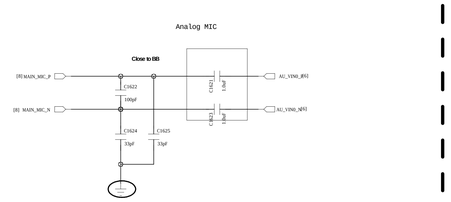
REC



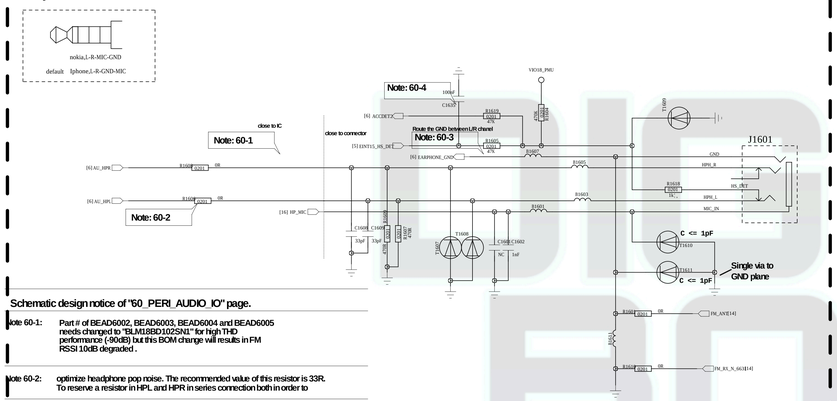
Earphone MIC



Main microphone



Earphone Audio



Schematic design notice of "60_PERI_AUDIO_IO" page.

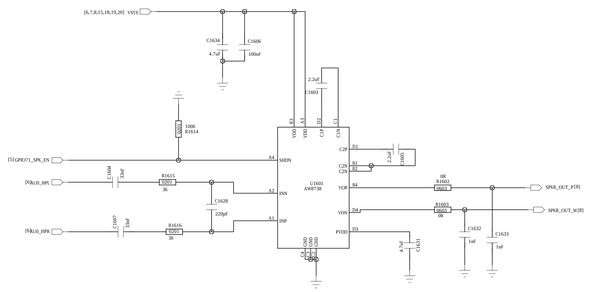
Note 60-1: Part # of BEAD6002, BEAD6003, BEAD6004 and BEAD6005 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

Note 60-2: optimize headphone pop noise. The recommended value of this resistor is 33R. To reserve a resistor in HPL and HPR in series connection both in order to

Note 60-3: TO Reduce cross talk, Please route the Earfpone_GND between L/R chanel

Note 60-3: To eliminate Plug in and out Recognize issue C6049 should be 100nF

Speaker PA



C836 £ ° when use AW8145 please use 1uF CAP;when use AW8155 or AW8155A please use 0 ohm res

COMPANY:	LC		
TITLE:	CX880		
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		
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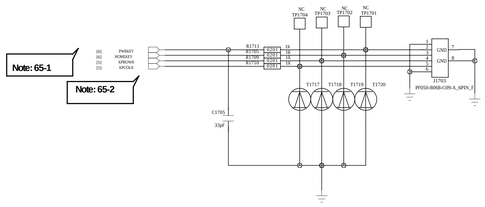
SCALE: <Scale>		SHEET: 16 20	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

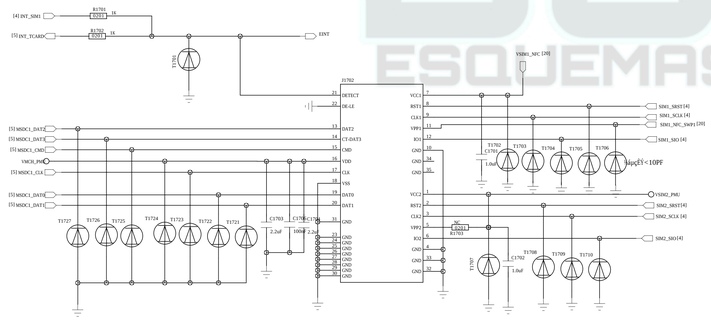
Power Key



Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.

Note 65-1:	DO NOT put pull-up resistor on PWRKEY
Note 65-2:	Volume Up : HOME key / GND Volume Down : (KPROW0/KPCOL0) or KPCOL0 / GND

SIM1& T Card



Switch

COMPANY:	LC		
TITLE:	CX880		
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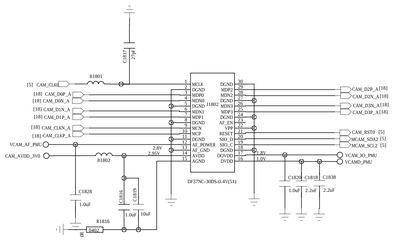
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 67 20

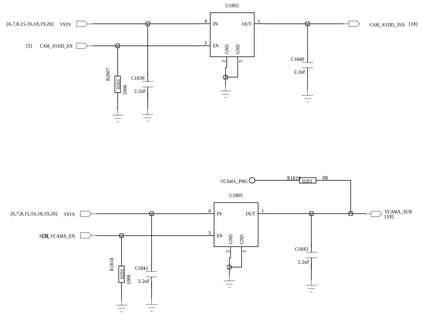
REVISION RECORD			
LTR	ECO NO.:	APPROVED:	DATE:

Main Camera

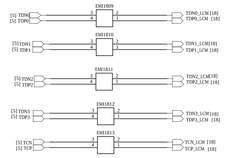
Main Camera A

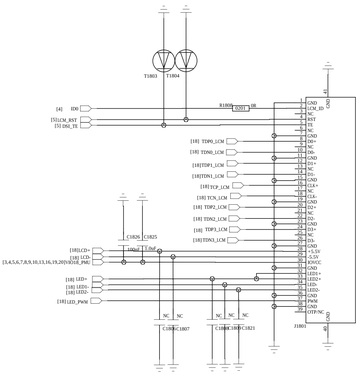


Main Camera AVDD

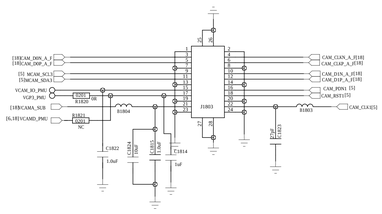


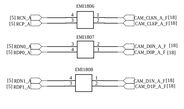
LCM





Front Camera

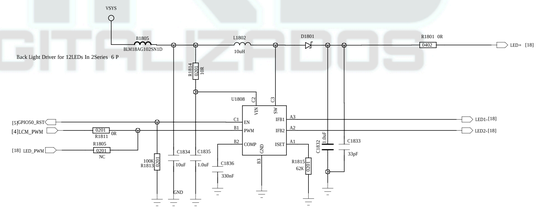


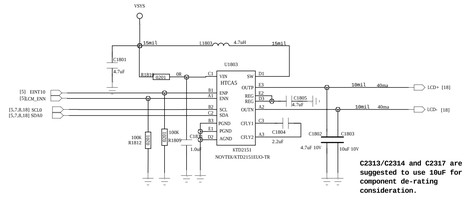


Schematic design notice of "63_PERI_CAMERA_KEYPAD" page.

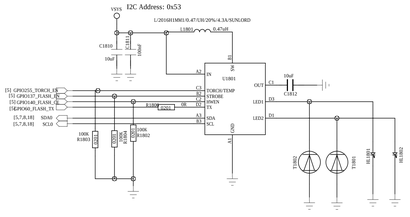
Note 62-1:	The VCC of I2C_0 is pulled to "VCAM_IO_PMU".
Note 62-2:	I2C control interface of front camera (with AF) must be assigned to I2C-2 bus when PIP/VIV feature be supported.
Note 62-3:	Reserve a capacitor (27pF) on camera's MCLK and shunt it to GND to prevent GPS de-sense.

Black Light





Flash



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TITLE:	CX880		
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CHECKED: <Checked By>	DATED: <Checked Date>		
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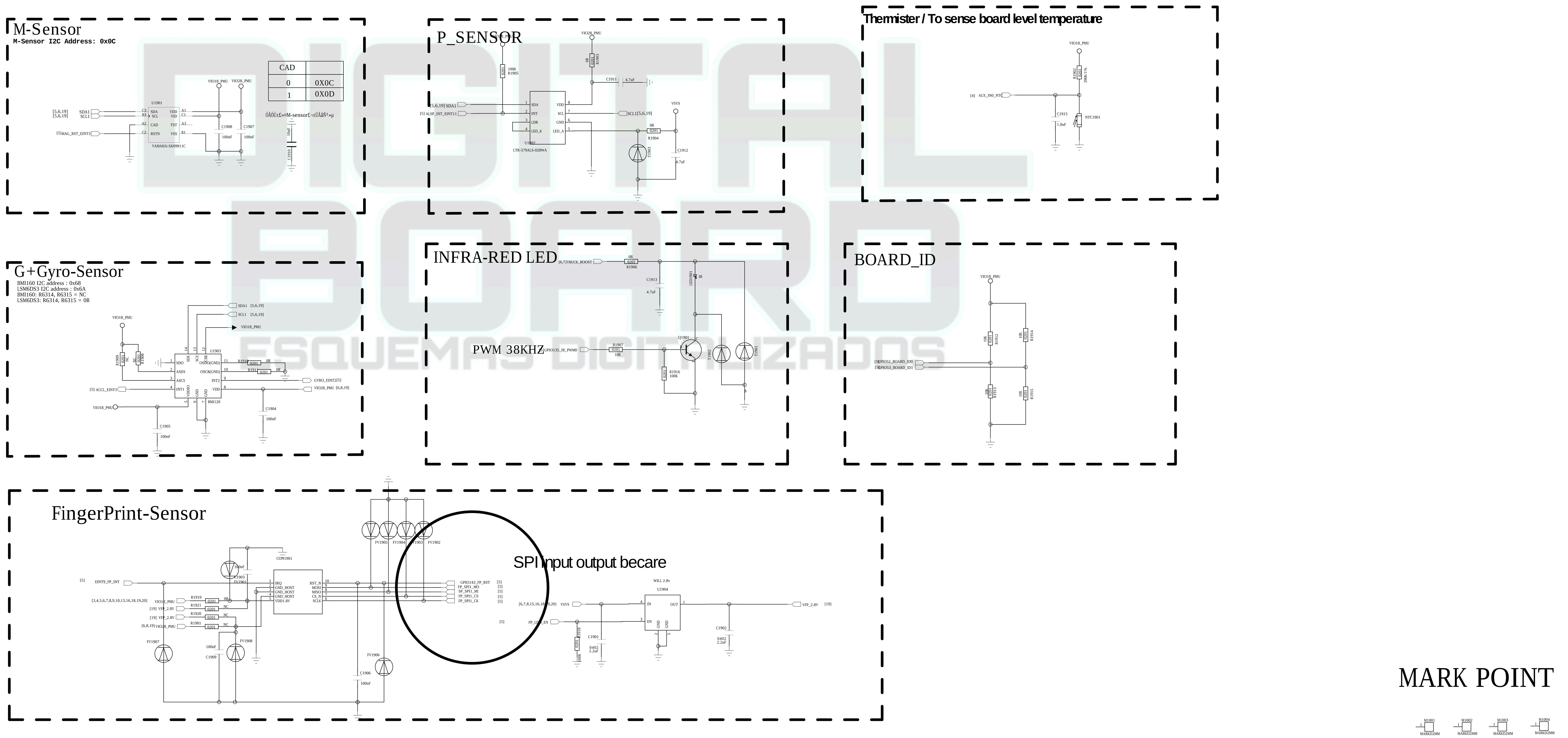

REVISION RECORD

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REVISION RECORD			
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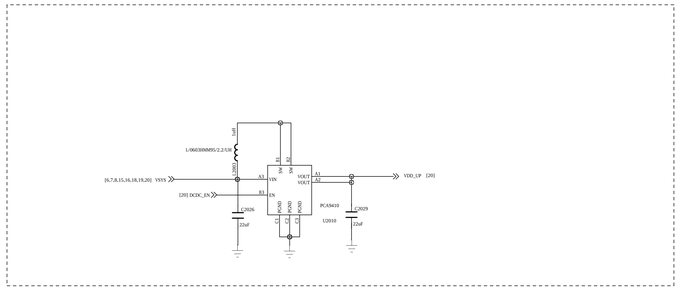
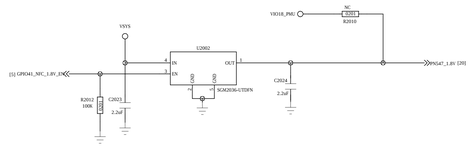
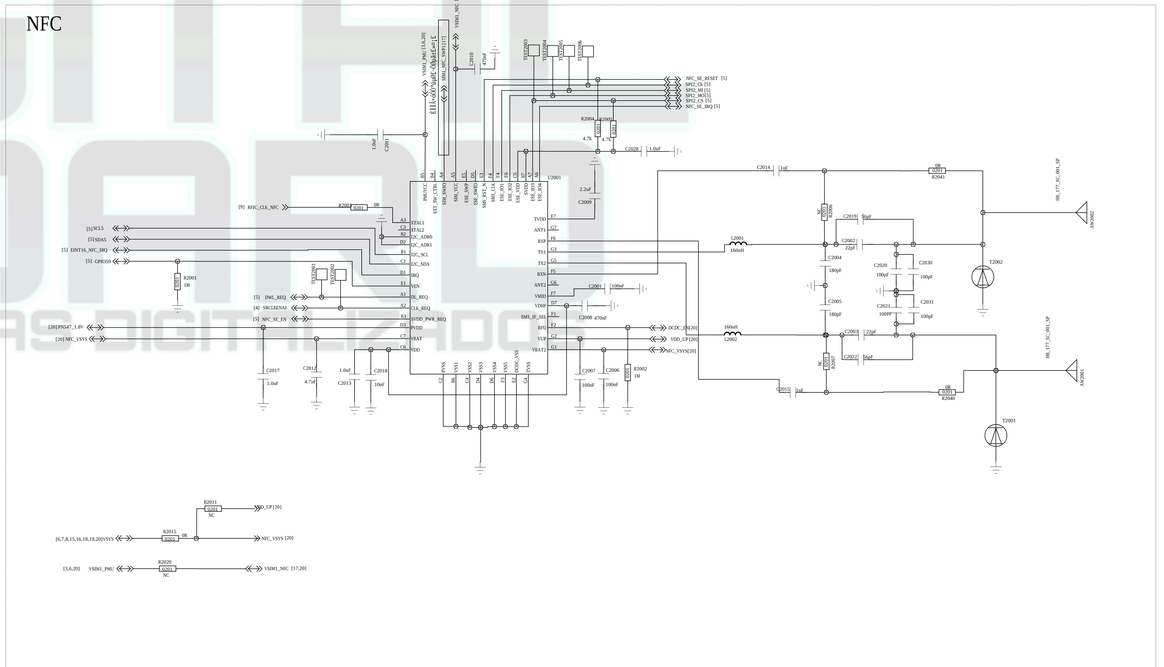


NFC power



I2C_ADR1	I2C_ADR0	WRITE	READ
0	0	0X50	0X51
0	1	0X52	0X53
1	0	0X54	0X55
1	1	0X56	0X57

NFC



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