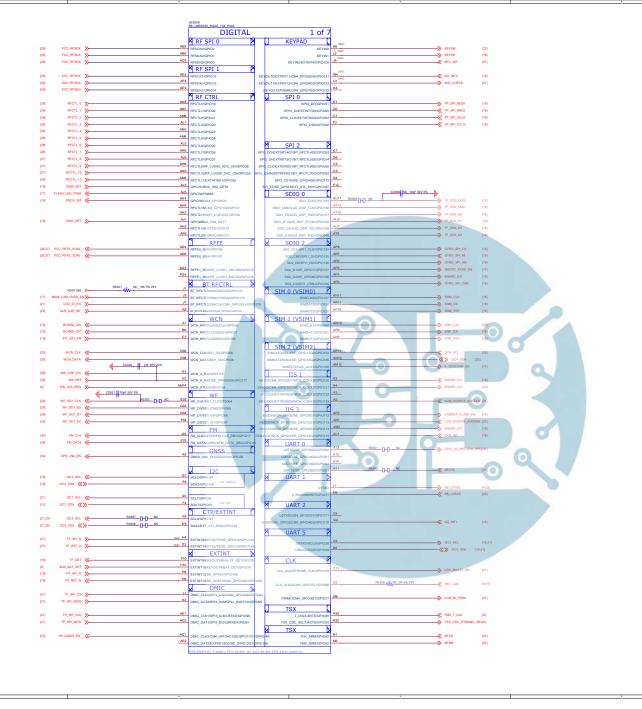
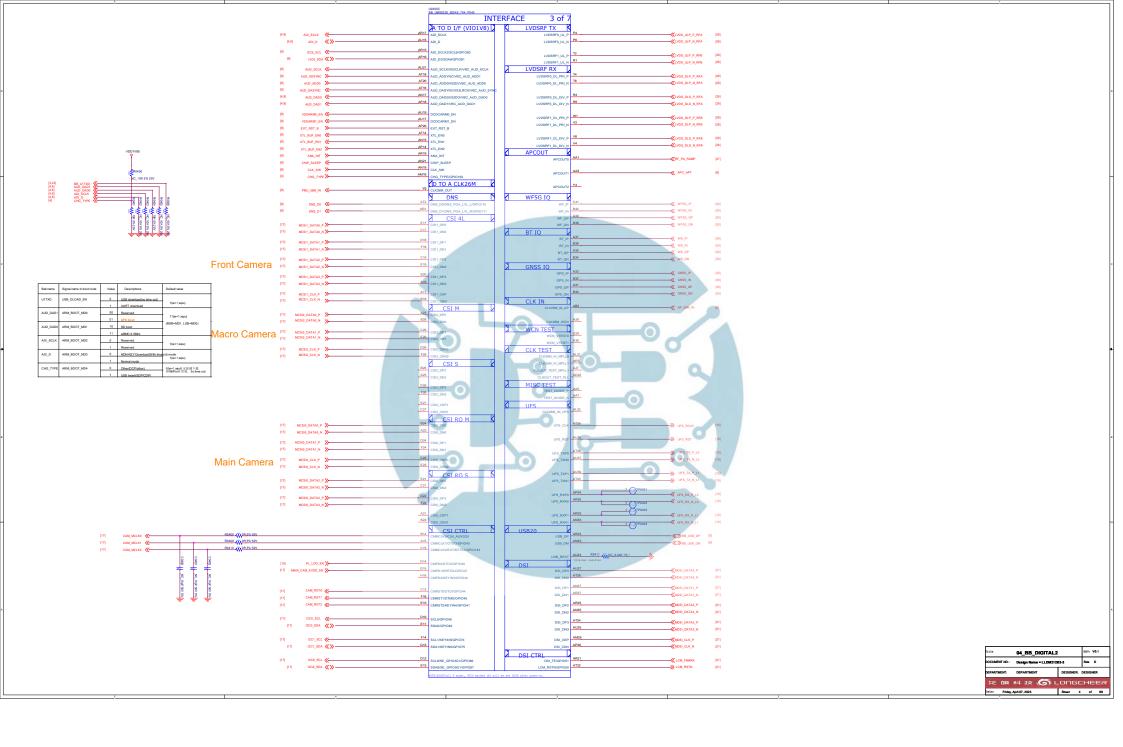
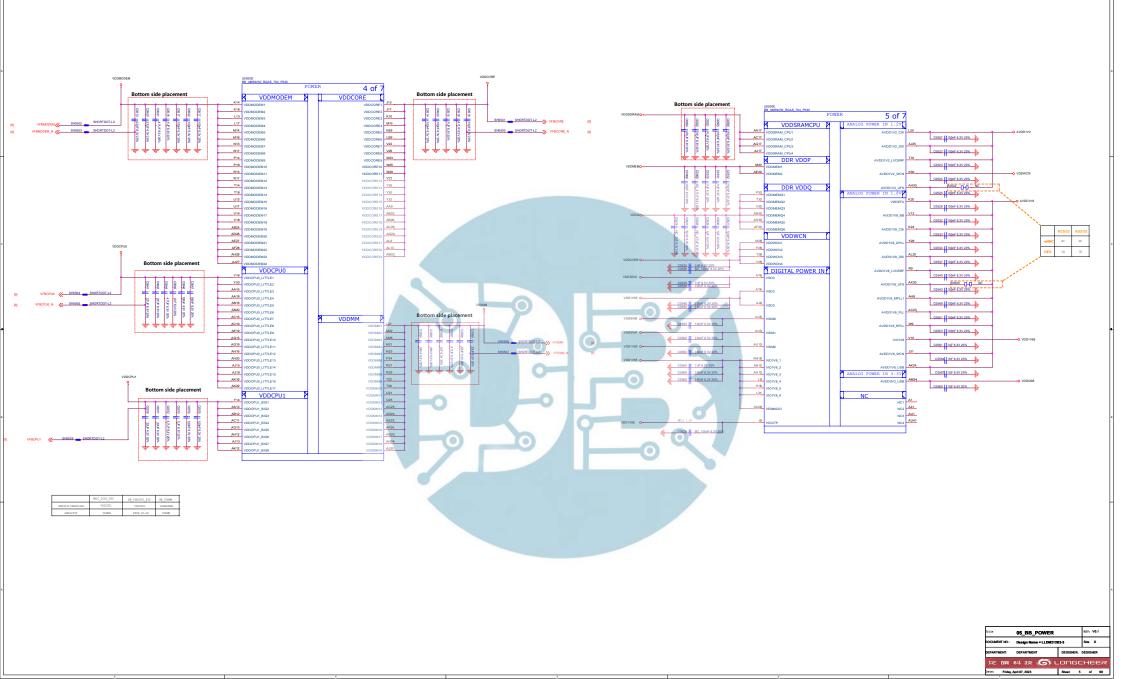
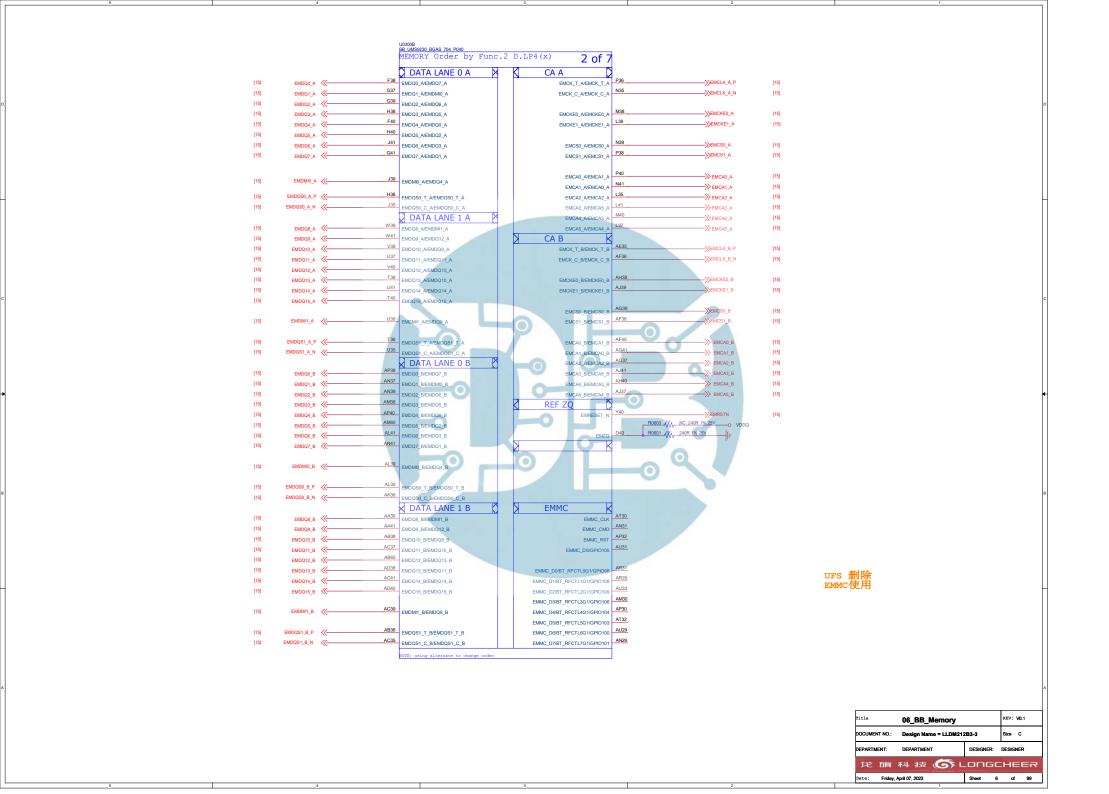


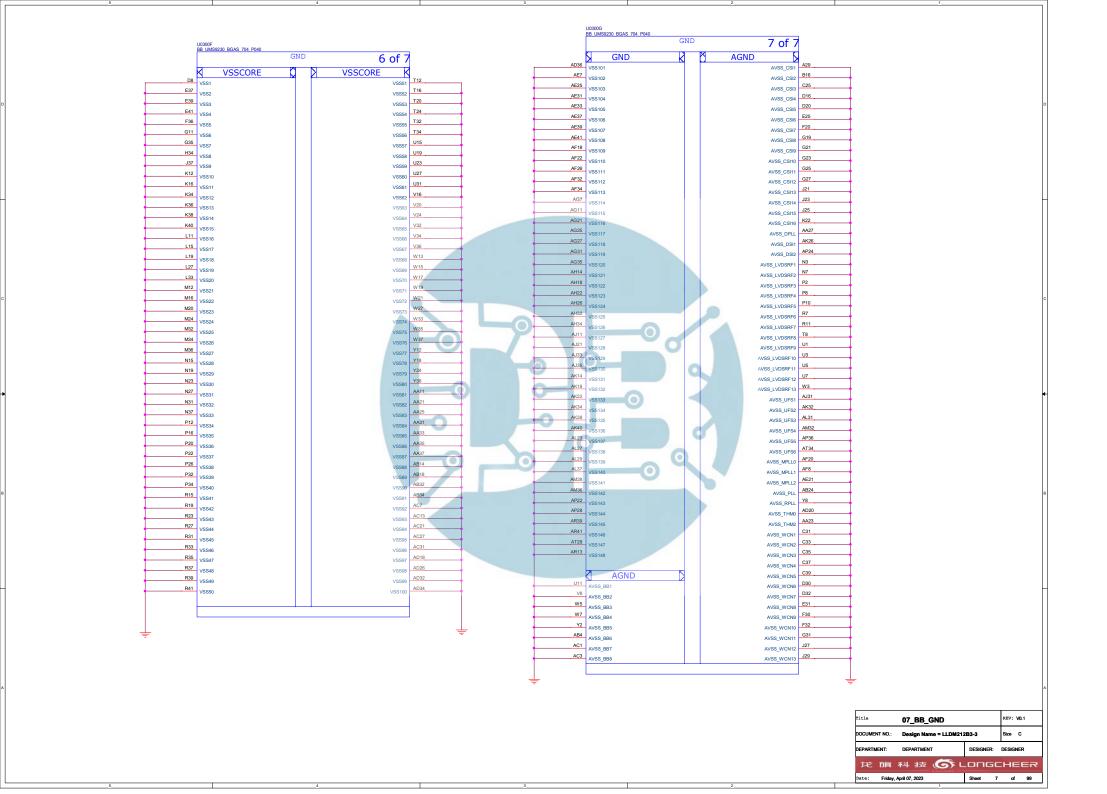
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PMU ANALOG TSX (PMU) Only 1 80810 100K 1% 50V PMU_TSEN_VREFP [8] ANALOG AUDIO A TO D INTERFACE —≪≫ ADI_D MAIN_MIC_N >> C0820 1UF 8.3V 20% R0837 WA 1K.5% AUD_SCLK A11 ✓ AUD_SCLK AUXINC P C0851 10F63V30% R0839 TK5% H2 MIC2, P AUXINC N C0815 10F63V20% R0839 TK5% G2 MIC2, N →S AUD ADD0 ALID DASYNO AUD_DADO B8 AUD_DADO HEADMIC_P >> R0804 WW 1K5% K5 HEADMIC_P HEADMIC_N > RISSO IK 5% J5 HEADMIC_N (20) HEADMIC_IN_DET >> R0802 W 1K 5% HEADMIC_IN_DET →>> EXT_RST_B →S ANA_INT CHIP_SLEEP C11 PICC输入、CPI输出、高有效 H5 GND_DET DCDC_CPU_EN B10 — ≪ XTL_BUF_EN2 PTESTO E1 M4 RCV_N >>> DNS_D0 DNS_D1 M7 A TO D INTERFACE CLK26M CLK26M DCXO LOWCUR **Board ID** DCXO_LOWCUR U5 CLK C0805 2.2UF 6.3V 20% XO_N REF_OUT0 U2 REF_OUT1 V1 R0813 XXA 0R 5% 25V CLASS G RTC C0808 470+F 6 3V 20% C0807 10UF 6 3V 20% RTC_32K_KI W6 系统的32KHz 时钟,默认由26MHz 时钟在PMIC 内部分频产生 RTC_32K_KO V6 C0812 4 7UE 6 3V 20% R0 24 D-D NC C0813 NC 4 7UF 6 3V 20% RF_TEMP_ADC CHG_TEMP_ADC C0814 22UF 6.3V 20% K1 CP_CAP_P -≪≫ USB0_HS_DP [16,2 Option1 Option2 RGB LED Qogir L6+UMP510G 0 0 SYSTEM 1 Qogir L6+UMP510G+DCDC 1 0 T11 RGB_IB1 SINK27mA T12 RGB_IB2 SINK27mA TSX Scenario Option3(264/52H) Option4(TCXC_MODIf)Option5(TSX_MODE) Option6(RTC_MODE) 26M TCXO+32K Crystal C0818 | 100pF 50V 5%/10% 26M TSX+32K Crystal EXT_XTL_EN_0 --> 26M TSX+32K-less from PMIC internal 0 0 1 1 PMU_T_DIG R0831 D-D NC B2 T_DIG T_DIG → BUA_BAT_DET ≪ XTL_BUF_EN1 EXT XTL EN 1 A2 26M DCXO+32K-less from PMIC Internal 0 EXT_XTL_EN_2 B1 26M DCXO+32K Crystal OPTION

✓ OPTION_TSX_MODE (8)

✓ OPTION RTC MODE BI

T2 V8S_T8X_A_1
T4 V8S_T8X_A_2
U84 V8S_T8X_A_3
V82 V8S_T8X_A_4

T1 VSS_TSX_B

OPTION_4 R5

OPTION_6 U7

litle	08_UMP510G_D	igital	REV: VO.		
DOCUMENT NO.:	Design Name = LLDM2	1283-3	Size D		
DEPARTMENT:	DEPARTMENT	DESIGNER:	DESIGNER: DESIGNER		
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The DCDCGPU controlled by UMP510G ADI interface signal DCDC_GPU_EN. The typical application of DCDCGPU is Unisoc BB chip

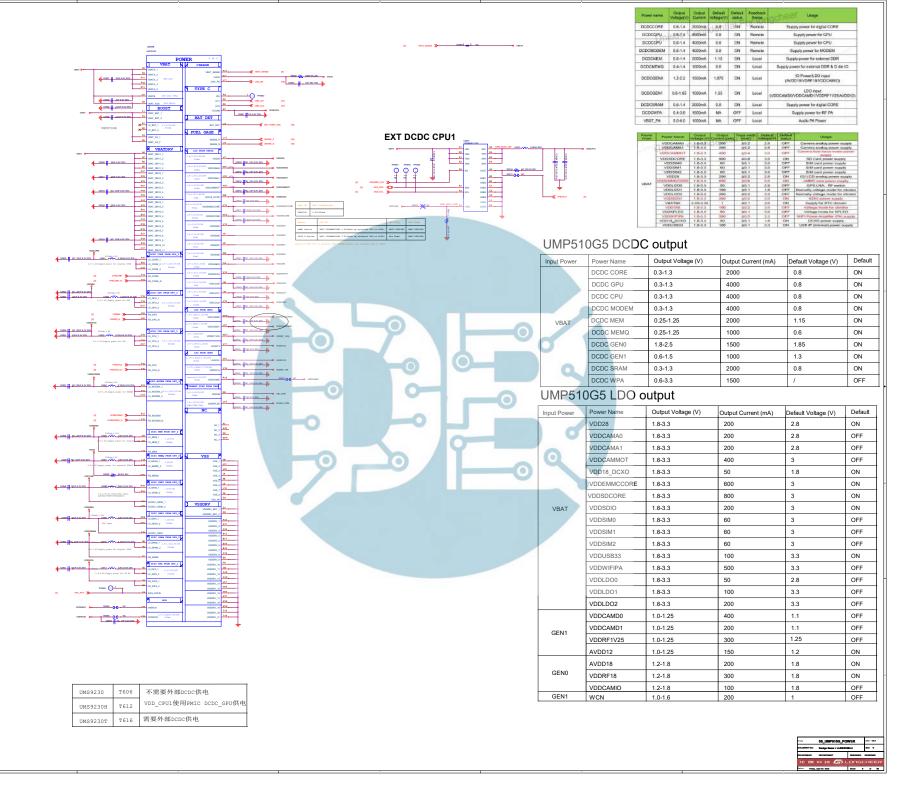
The DCDCGPU default on and uncontrollable by UMP510G ADI interface signal DCDC_GPU_EN

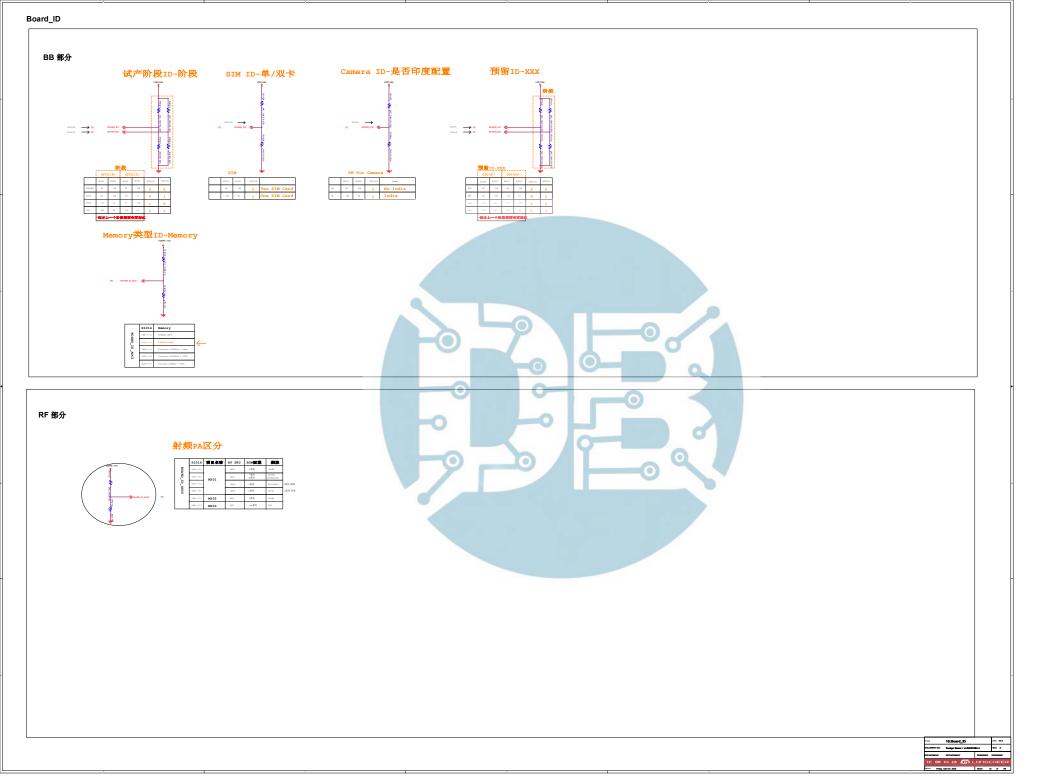
The DCDCMEMQ controlled by UMP510G ADI interface signal DCDC_GPU_EN. The typical application of DCDCMEMQ is Unisoc BB chip

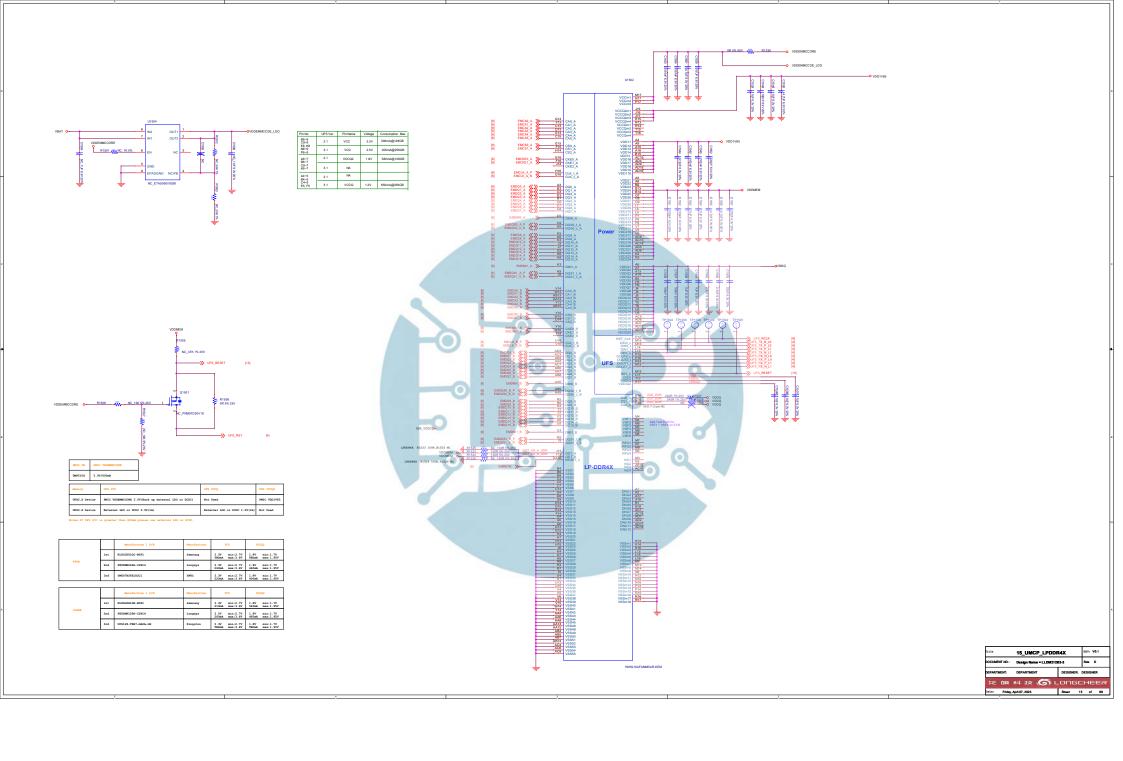
dual rail SRAM power supply.

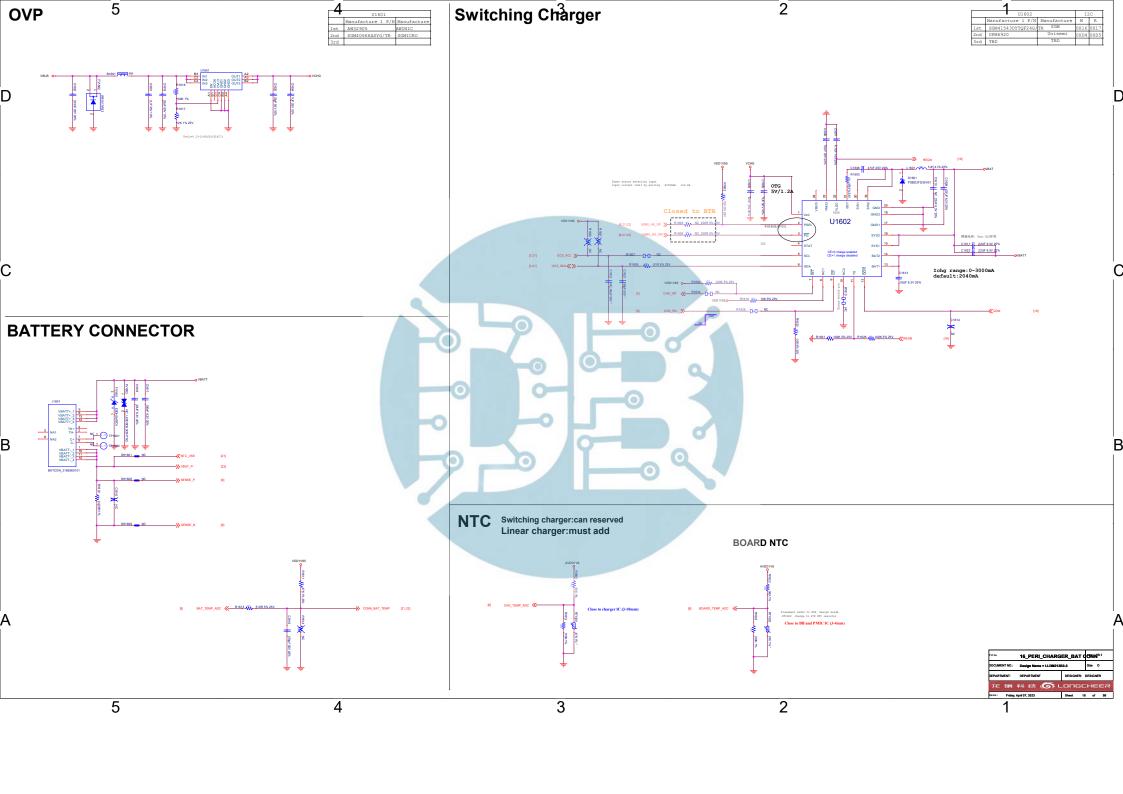
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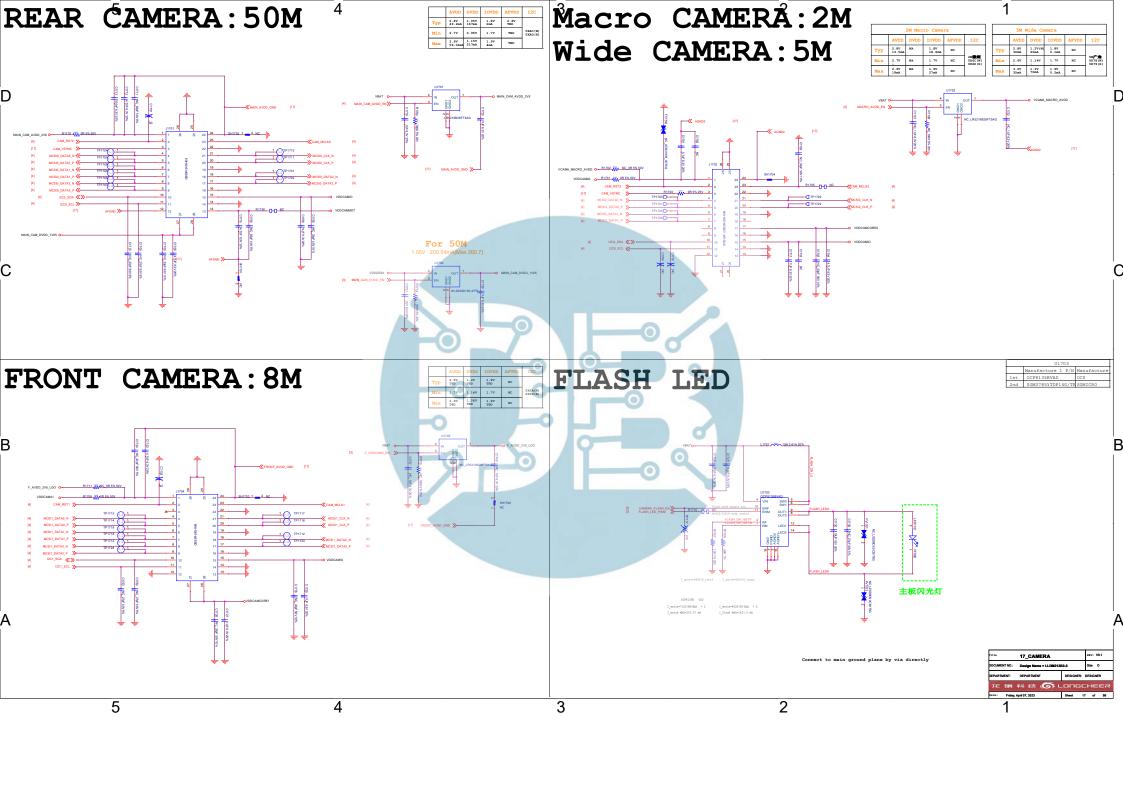
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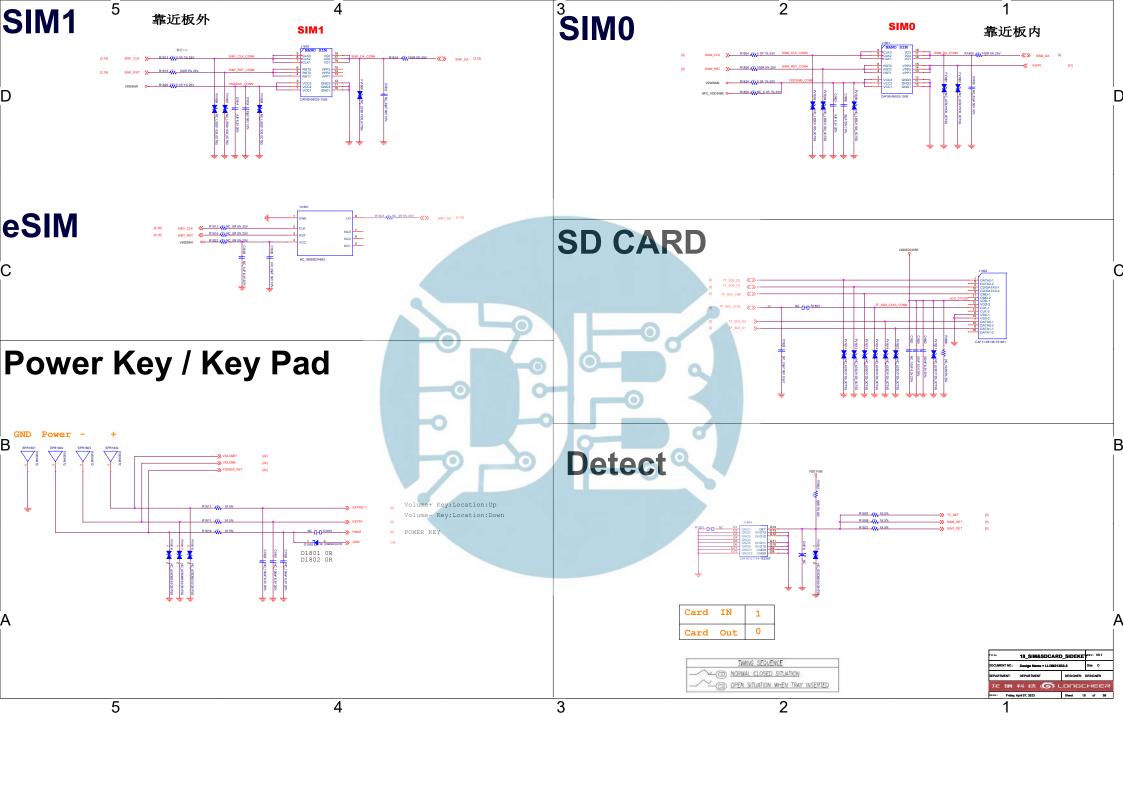


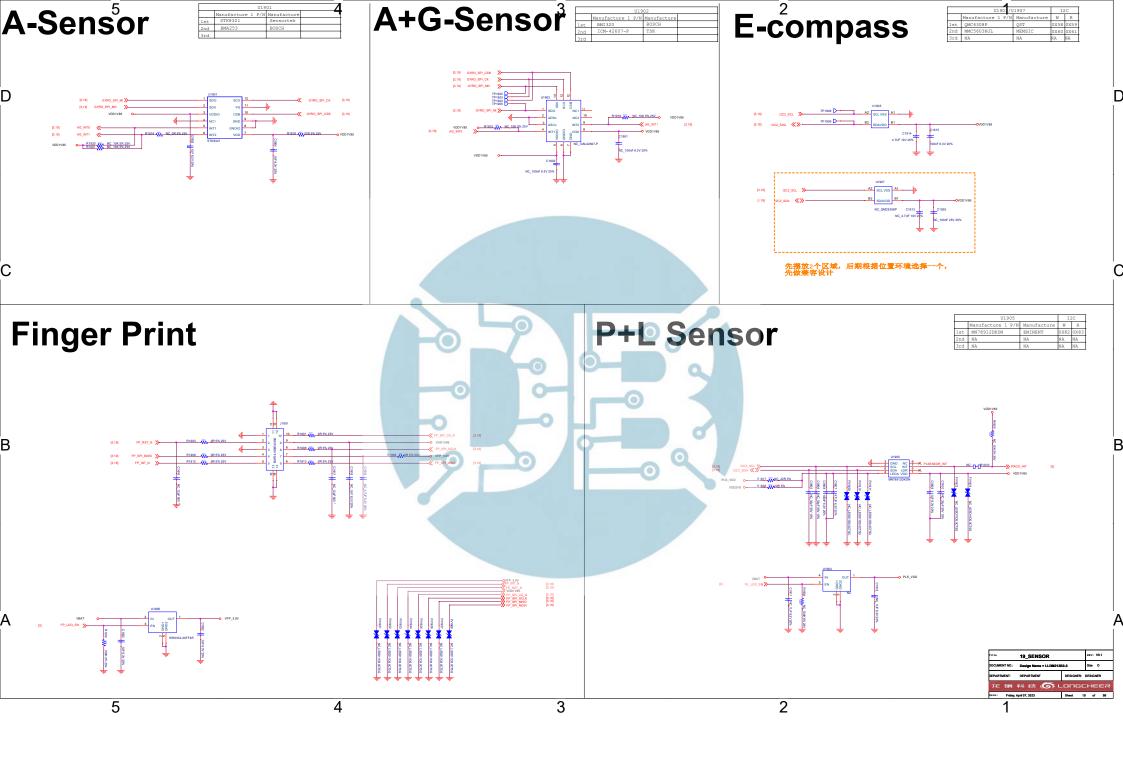


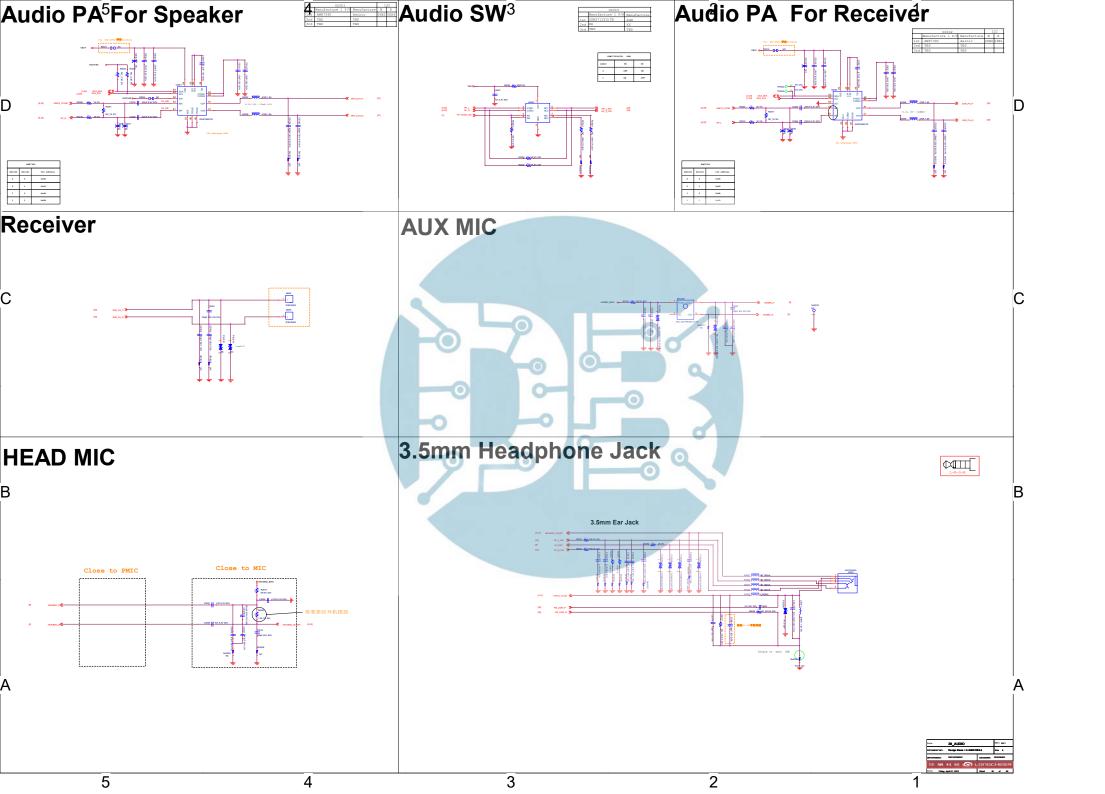


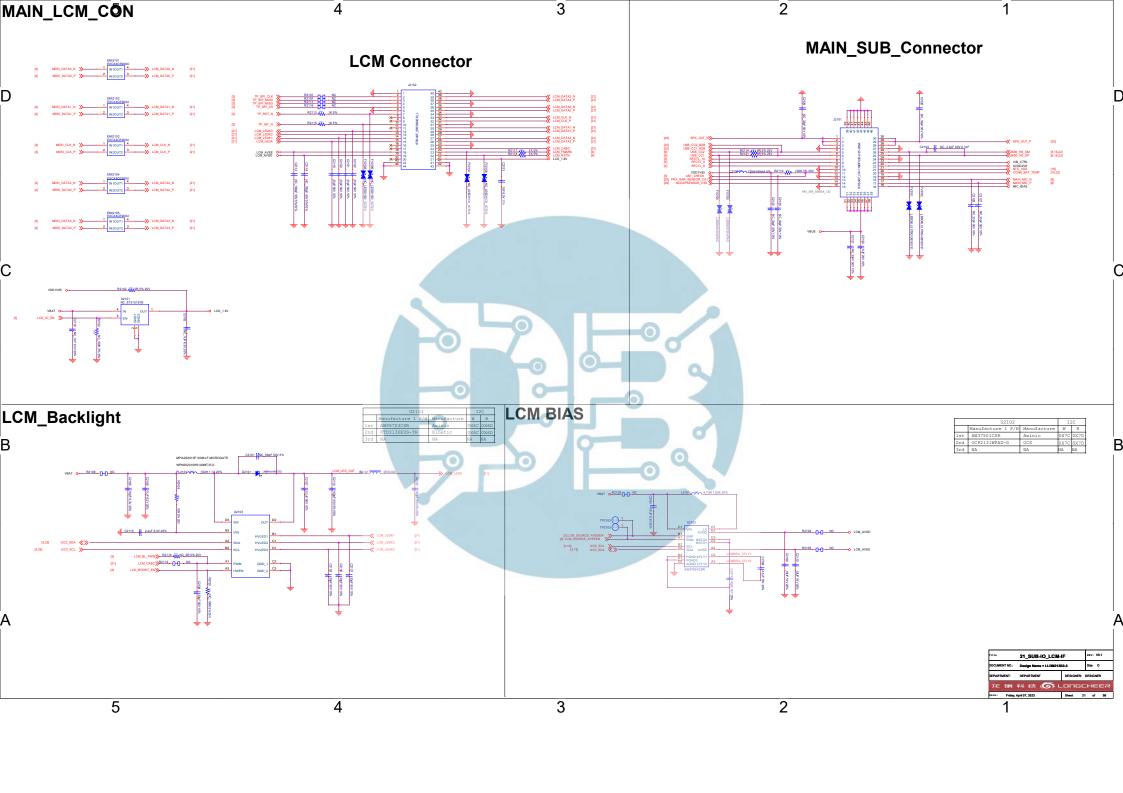


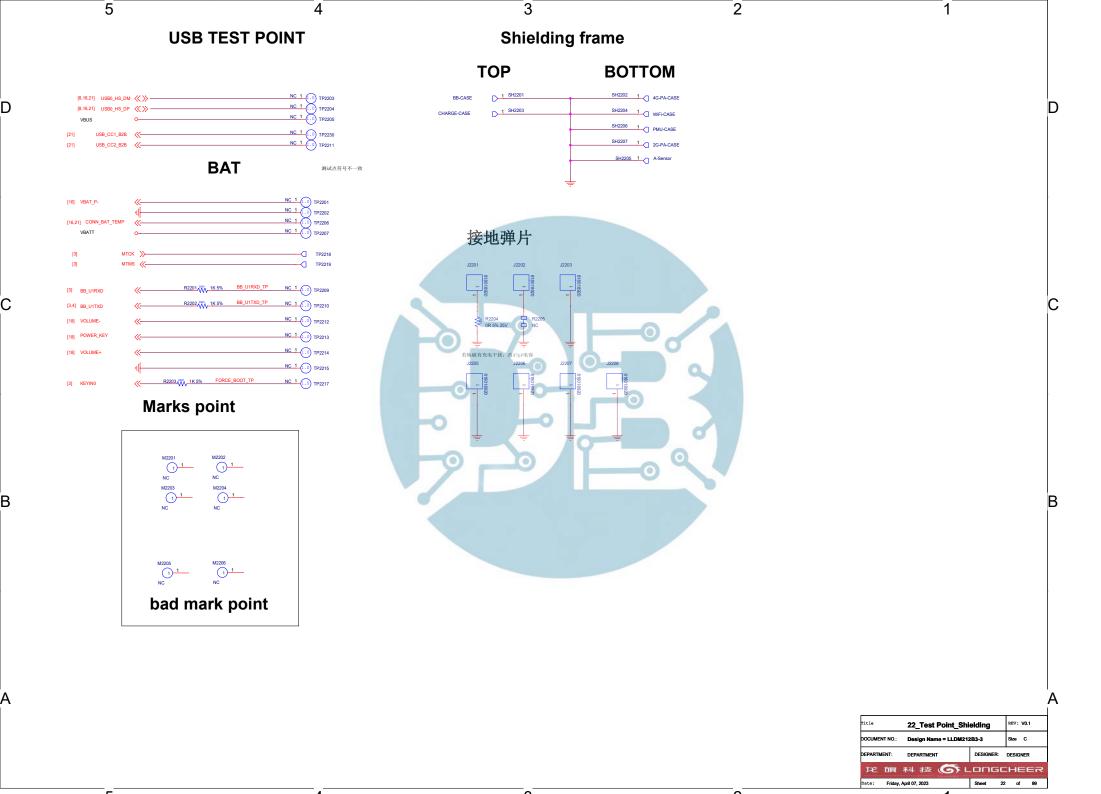








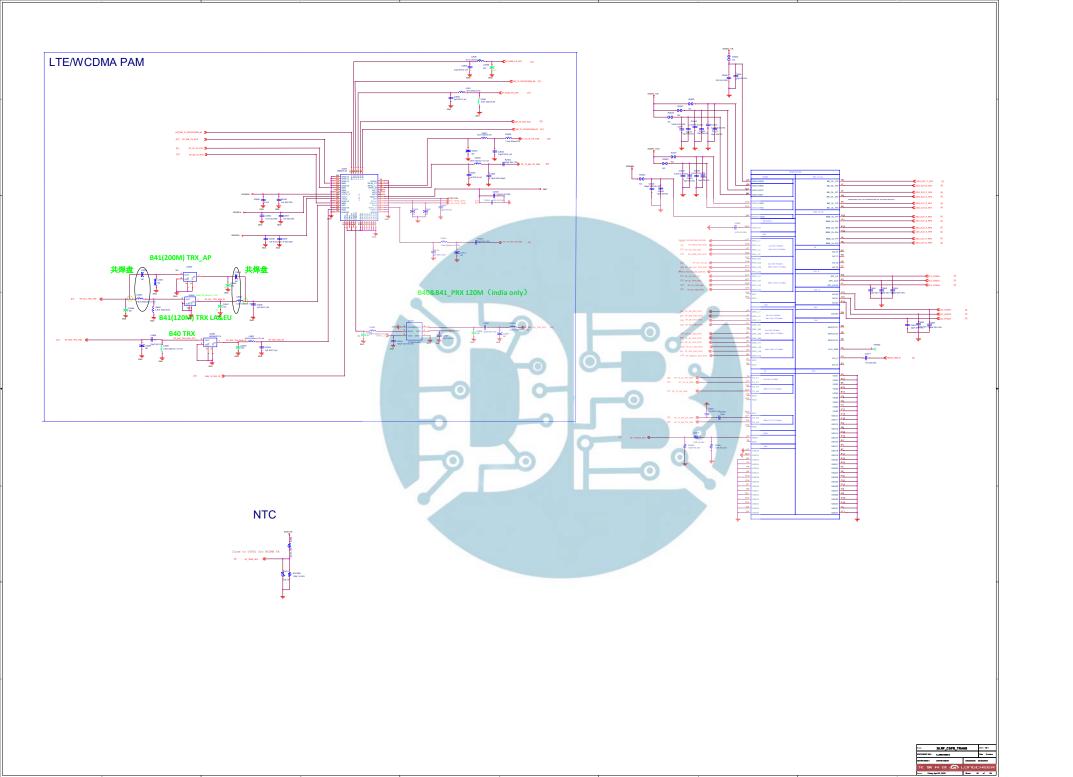


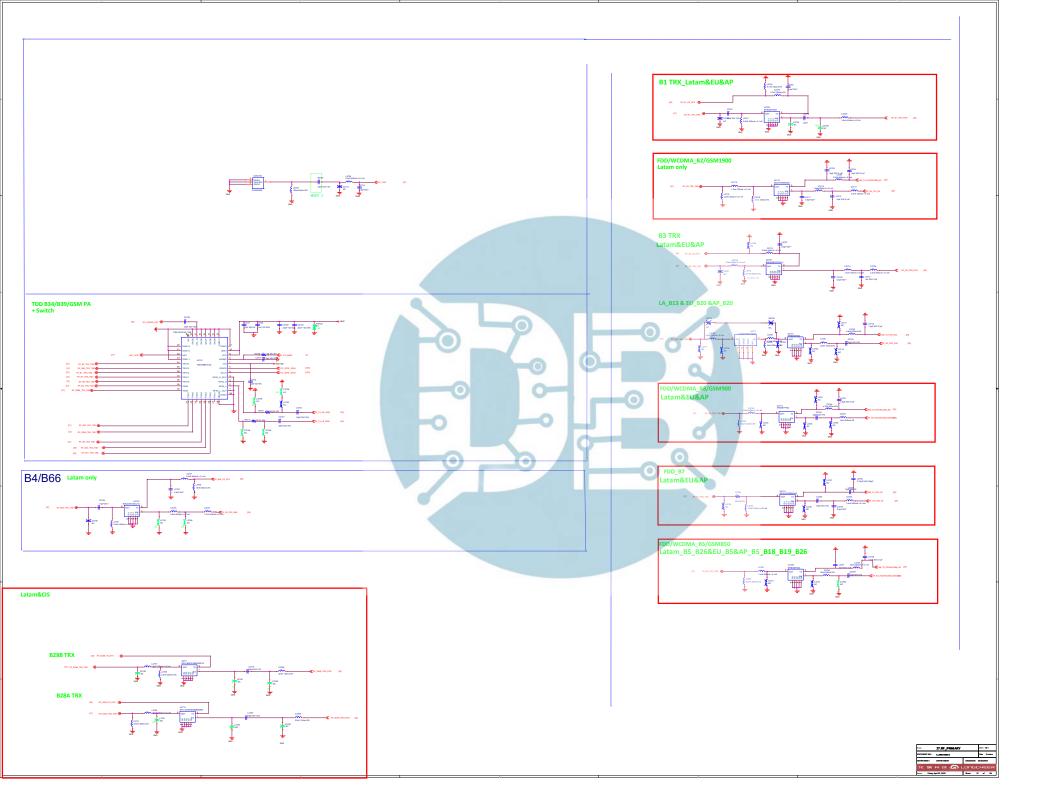


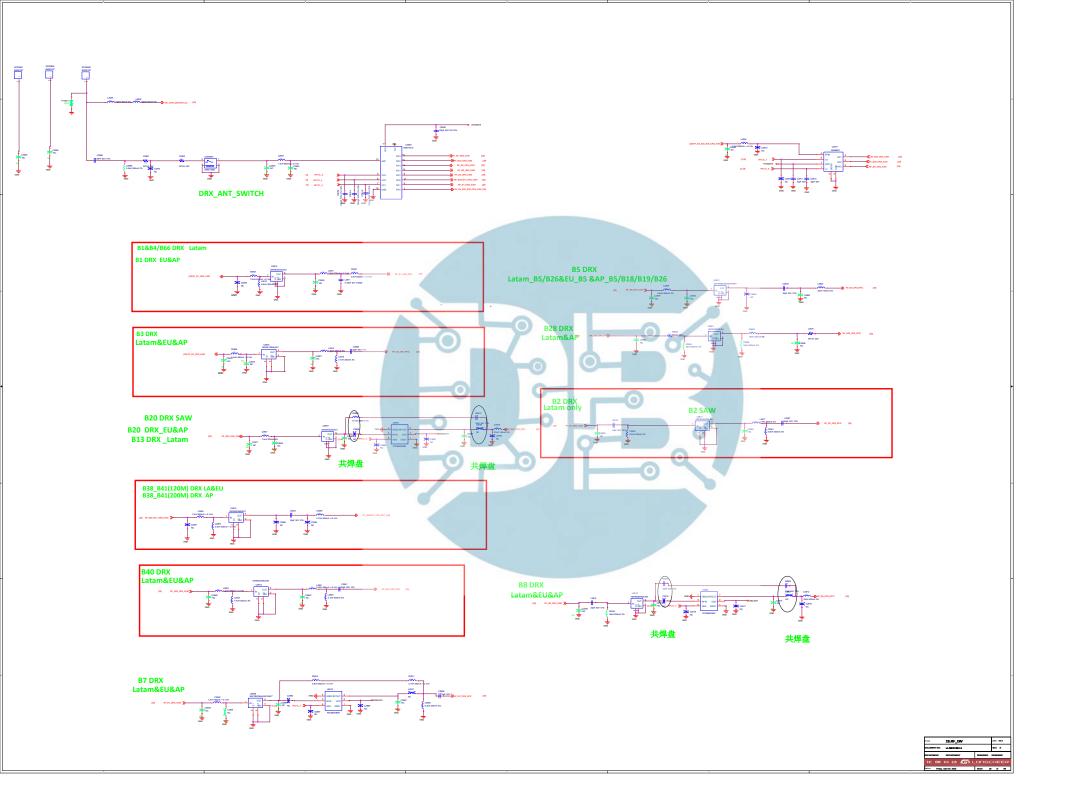
Modify List: 1:SAR Sense I2C Port change:I2C5--->I2C3.Reference Design remand 2:TXM TRX Port change:TRX4/6, TRX8/9 3:NFC Transciver change from NXP PN557 to SAMS S3NRN4V 4: LTE MB Tx PA out port adjust 1/3/66 for good routing 5:去除2908/2907 6:WCN VDDFU接地 7:去除R3001,GPS LNA R3018供电由VDD2.8换VDD SIM2 8:RFCTL0/1/2原本连接到TUNNERU2901变更为连接到U2818/U2819/U2802 9:网络名RFCTL17/18名字更换为RFCTL19/20连接到U2901 10:U2607/U2818/U2819/U2802的供电从VDD2V8换成VDDLD01 11:U2804/U2817供电由VDDSIM2换成AVDD2V8 12:新增C3052 13:RF_B1_TRX_TXM RF_B66_TRX_TXM端口调换 14:U2818控制网络改成RFCTL_16 15:+C3053 16:删除物料R1801、R1802 17:调换C3109、C3119至NFC芯片端的网络

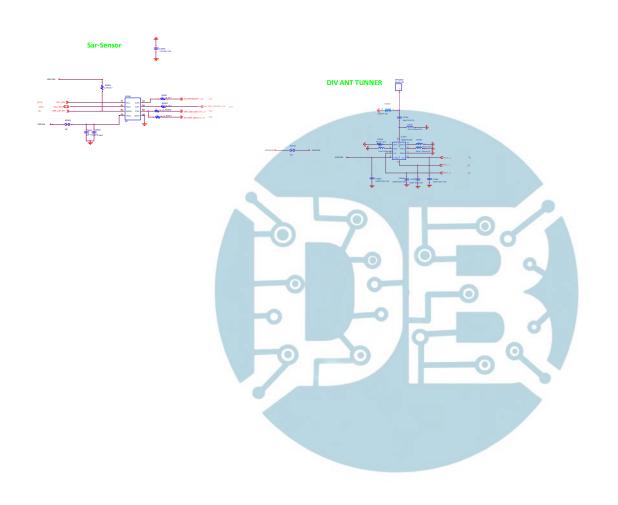
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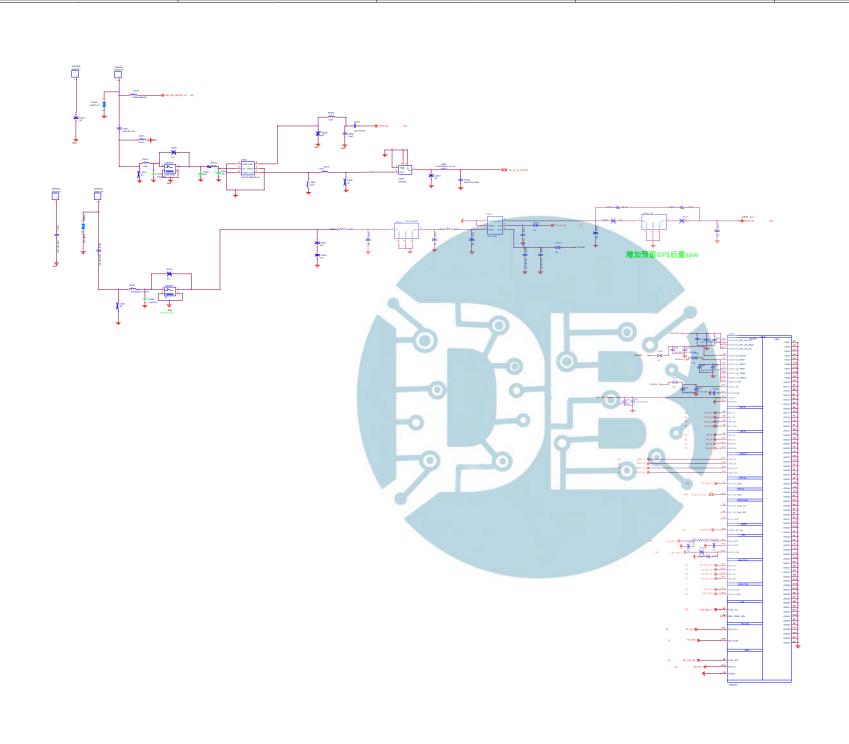




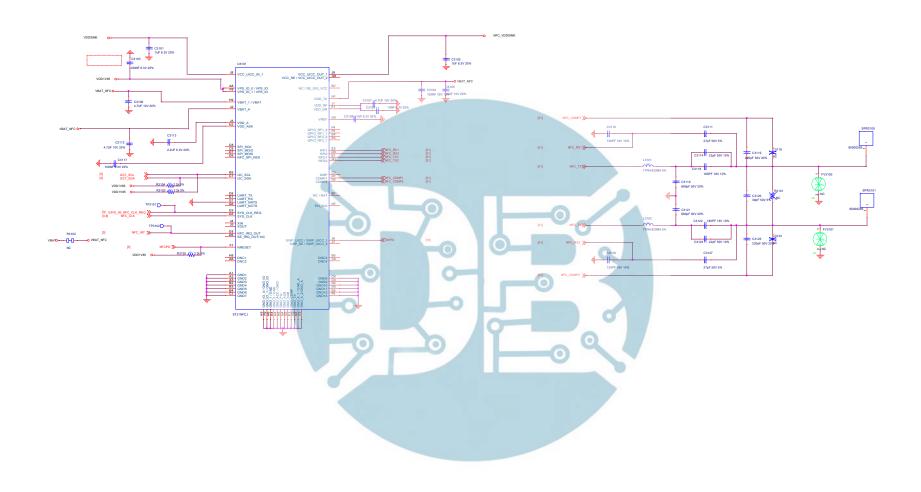












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