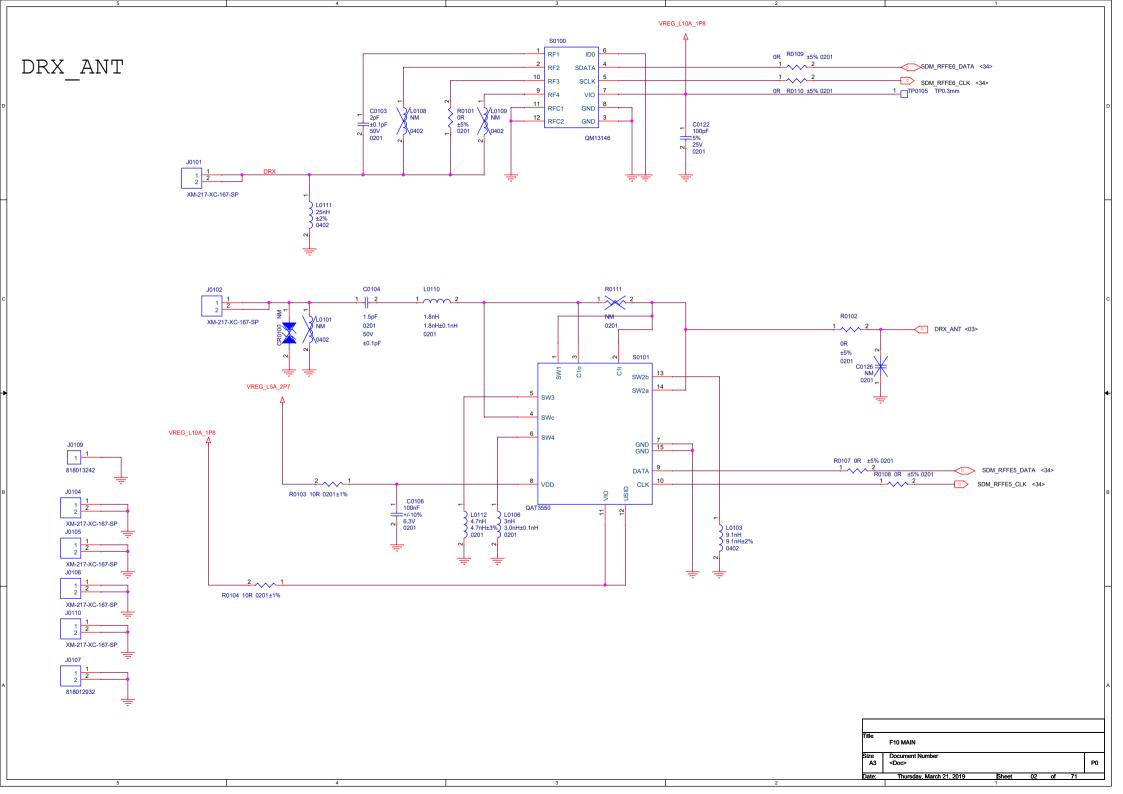
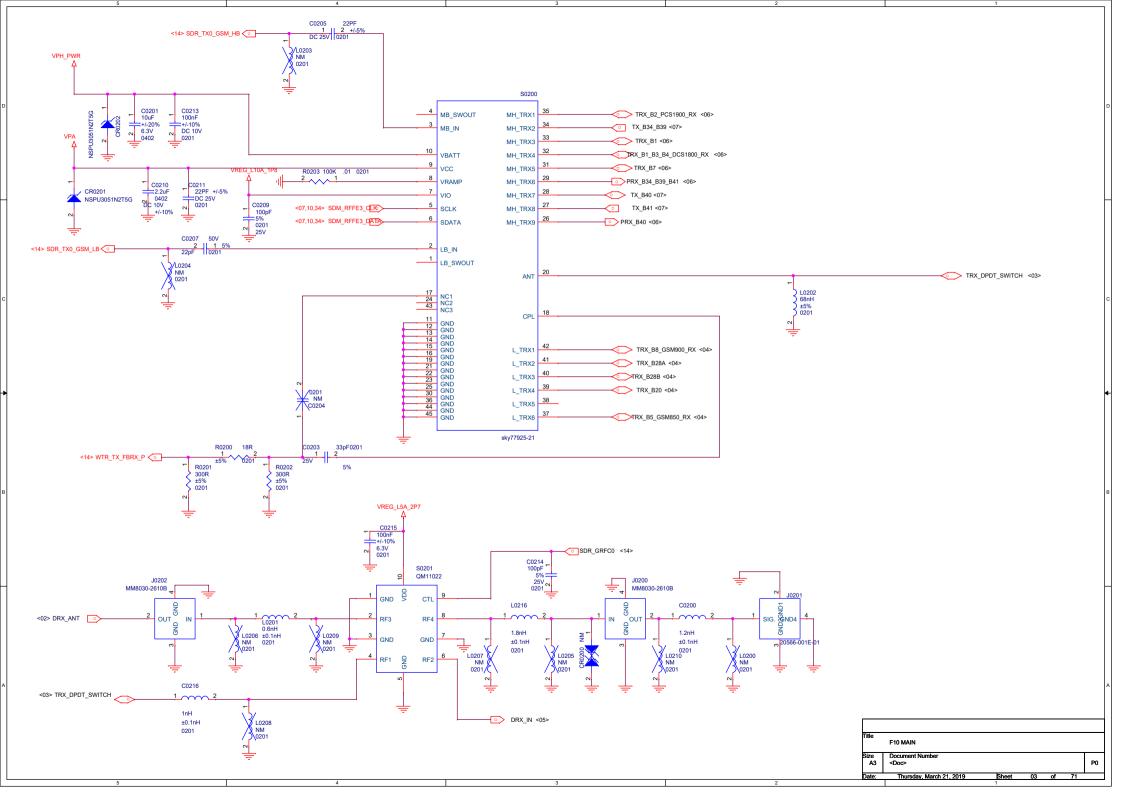
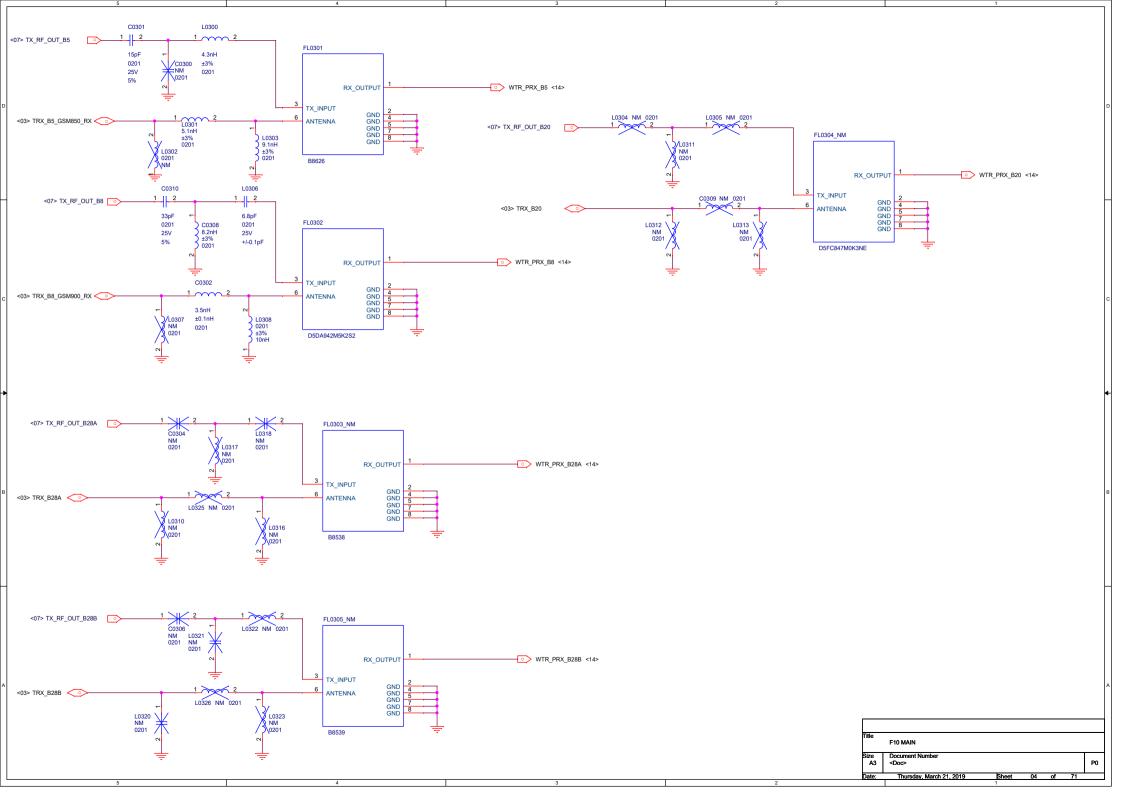
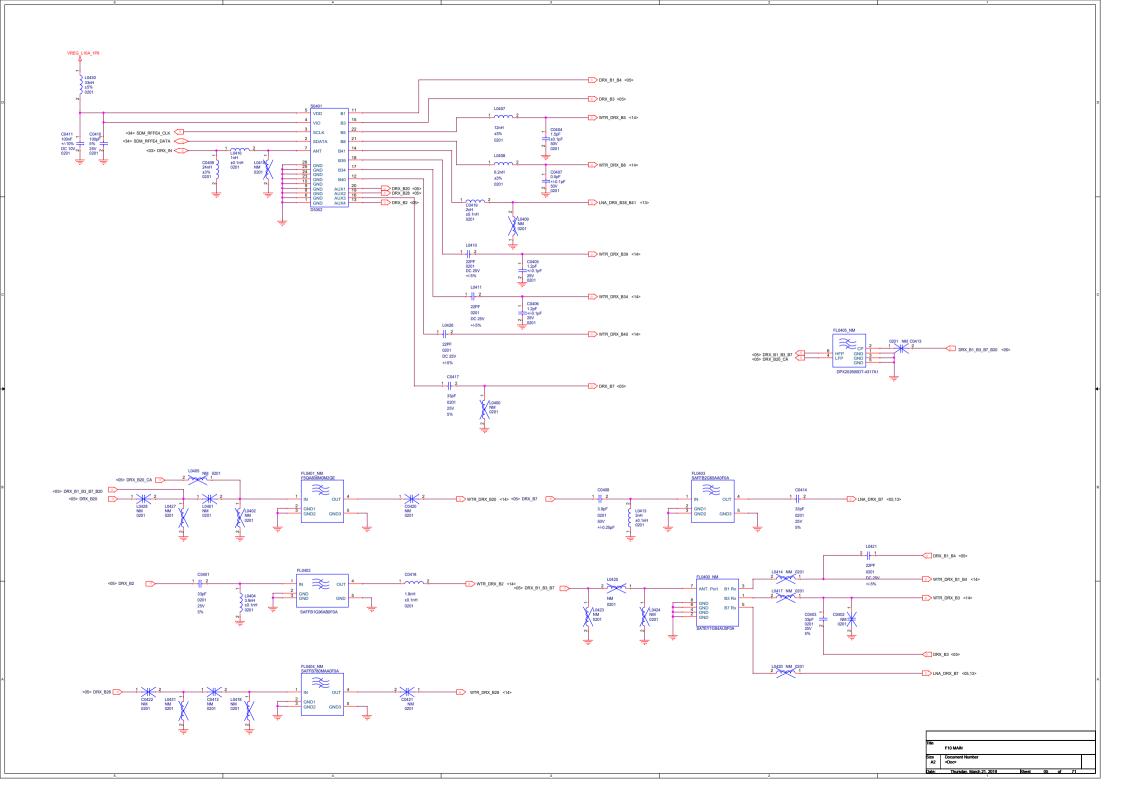


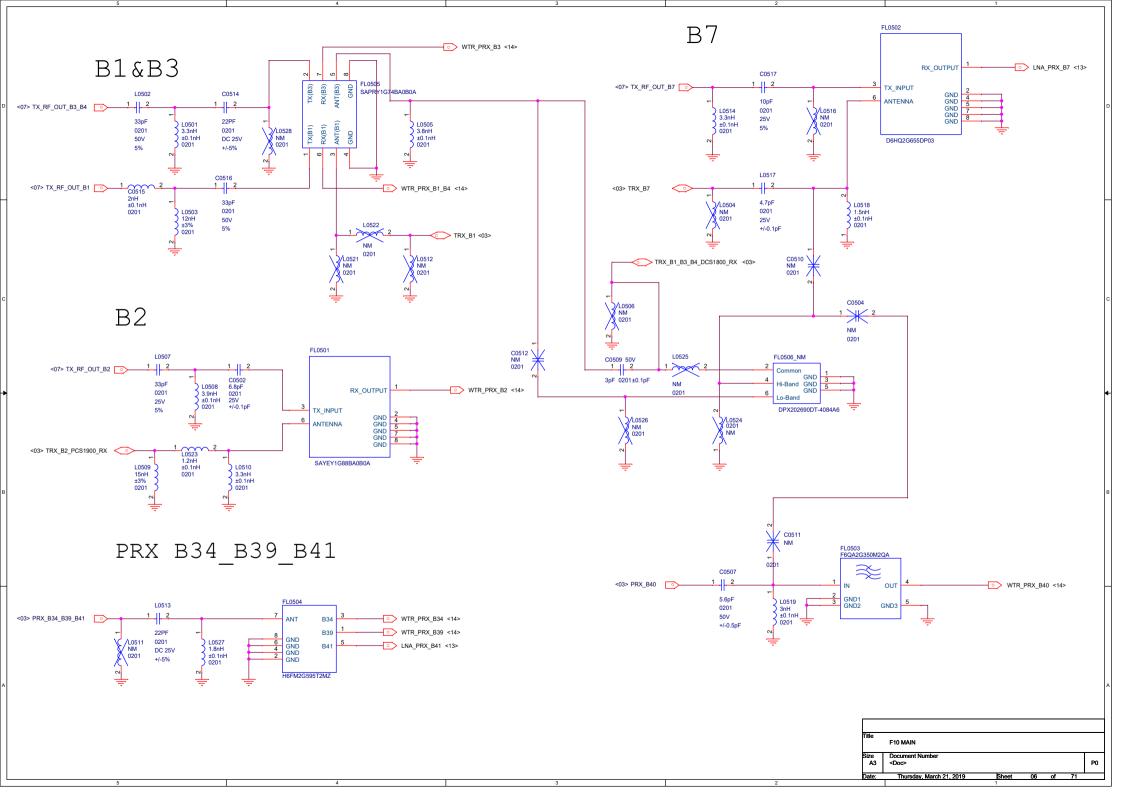
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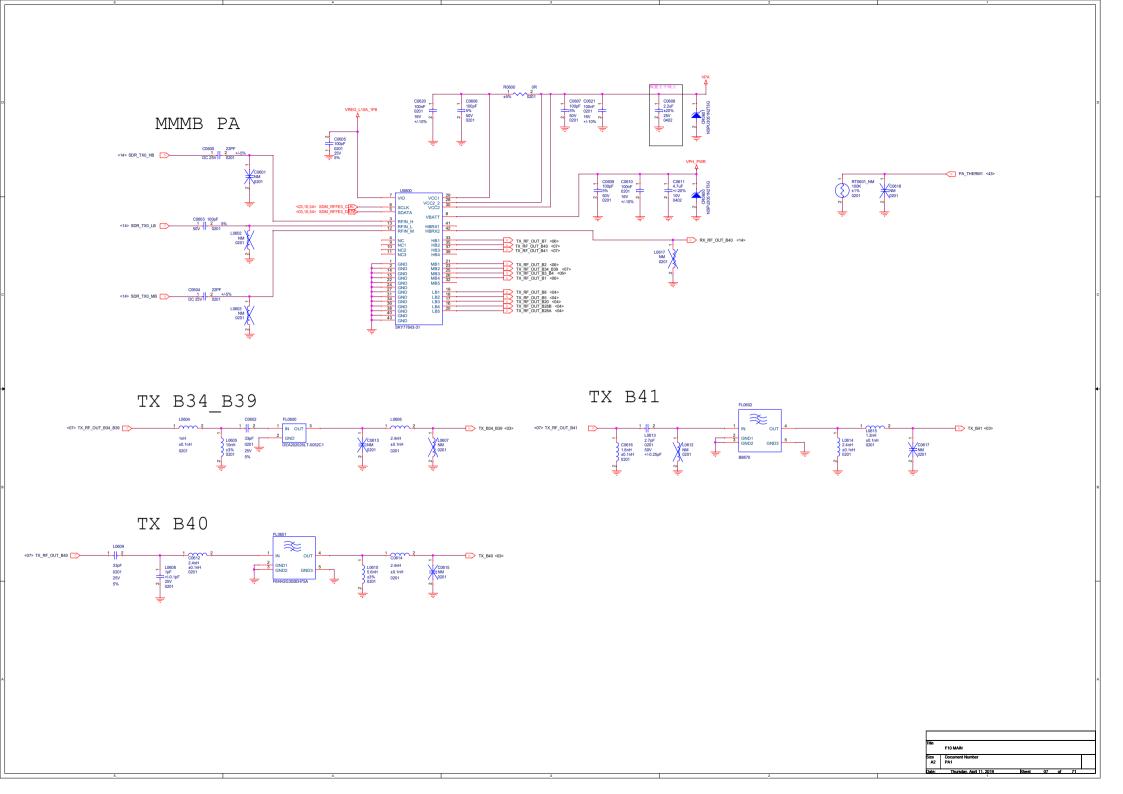


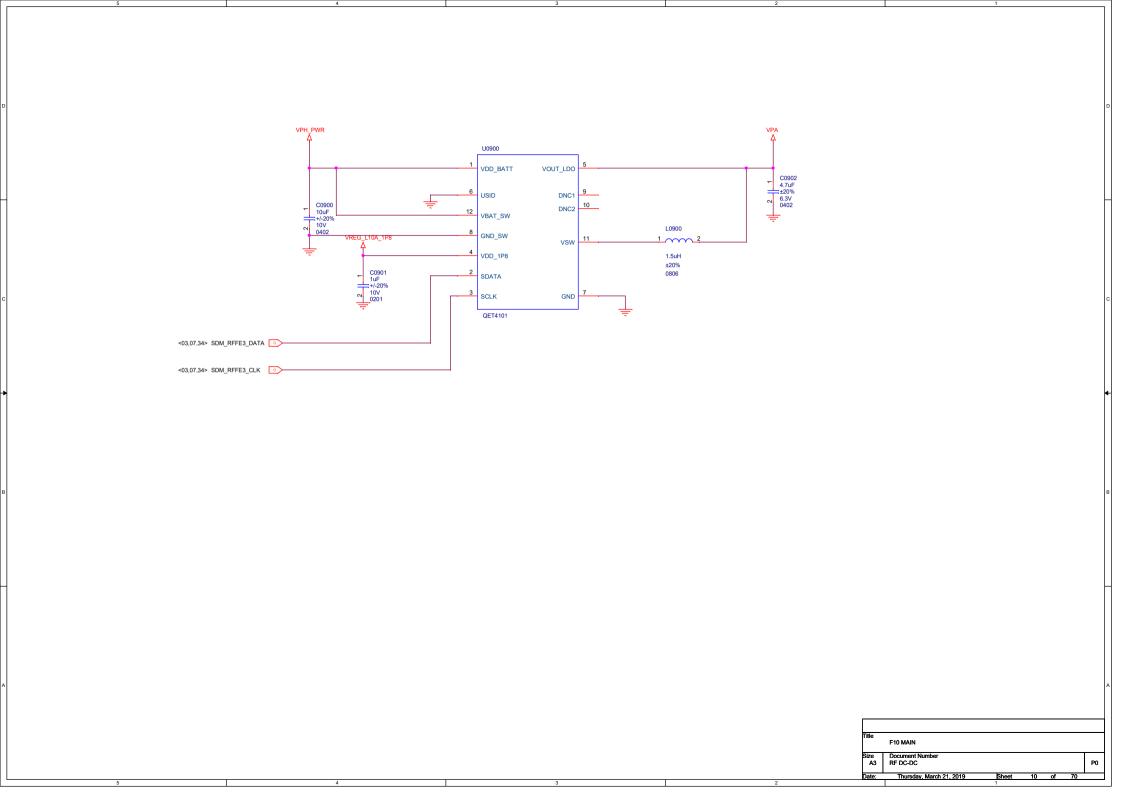


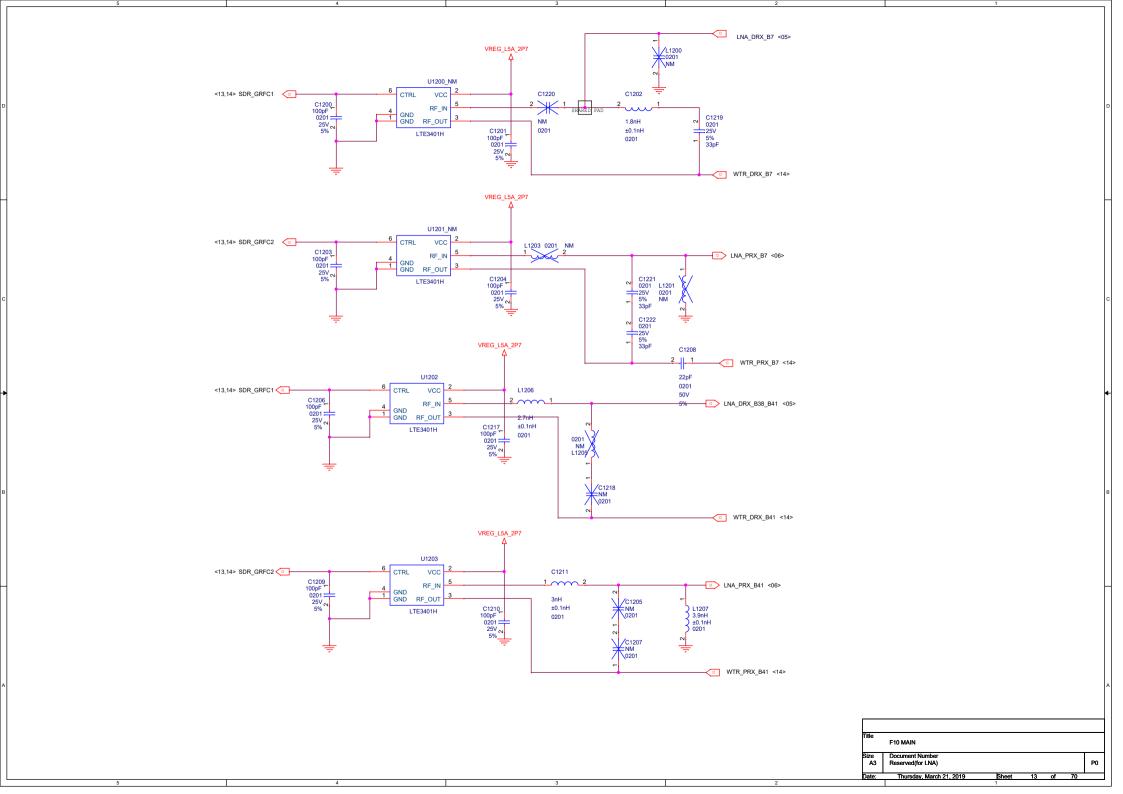


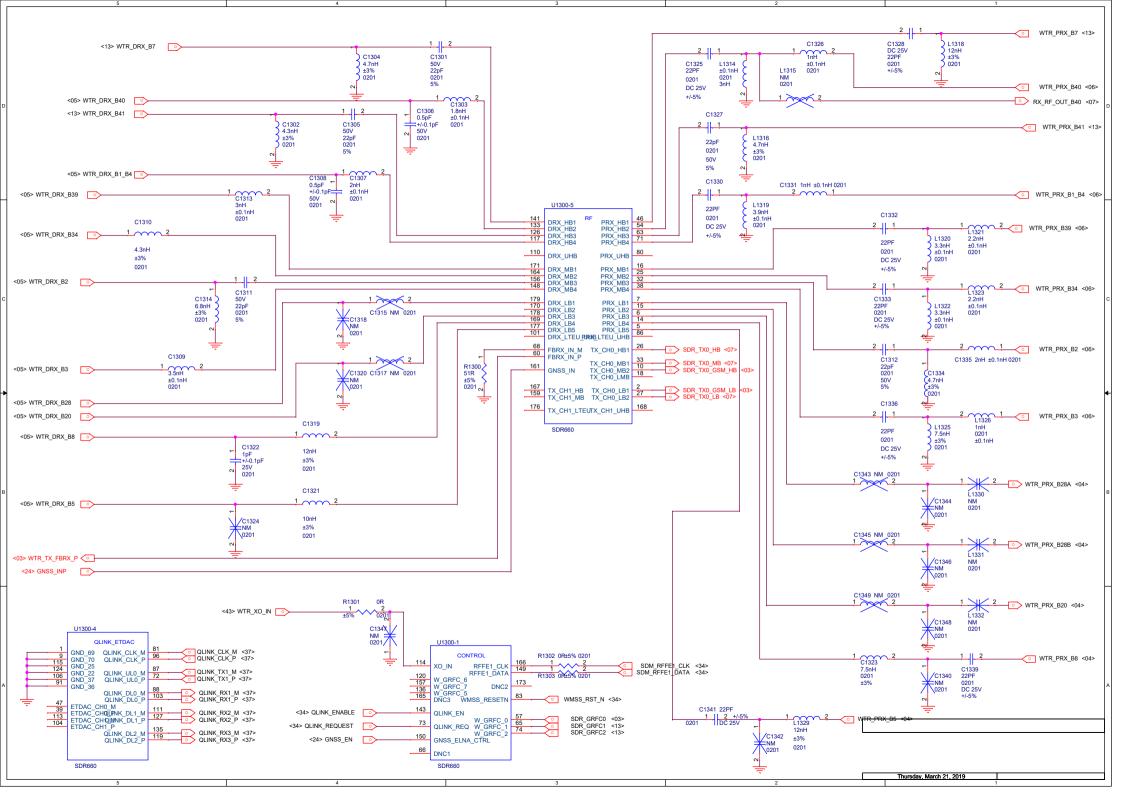


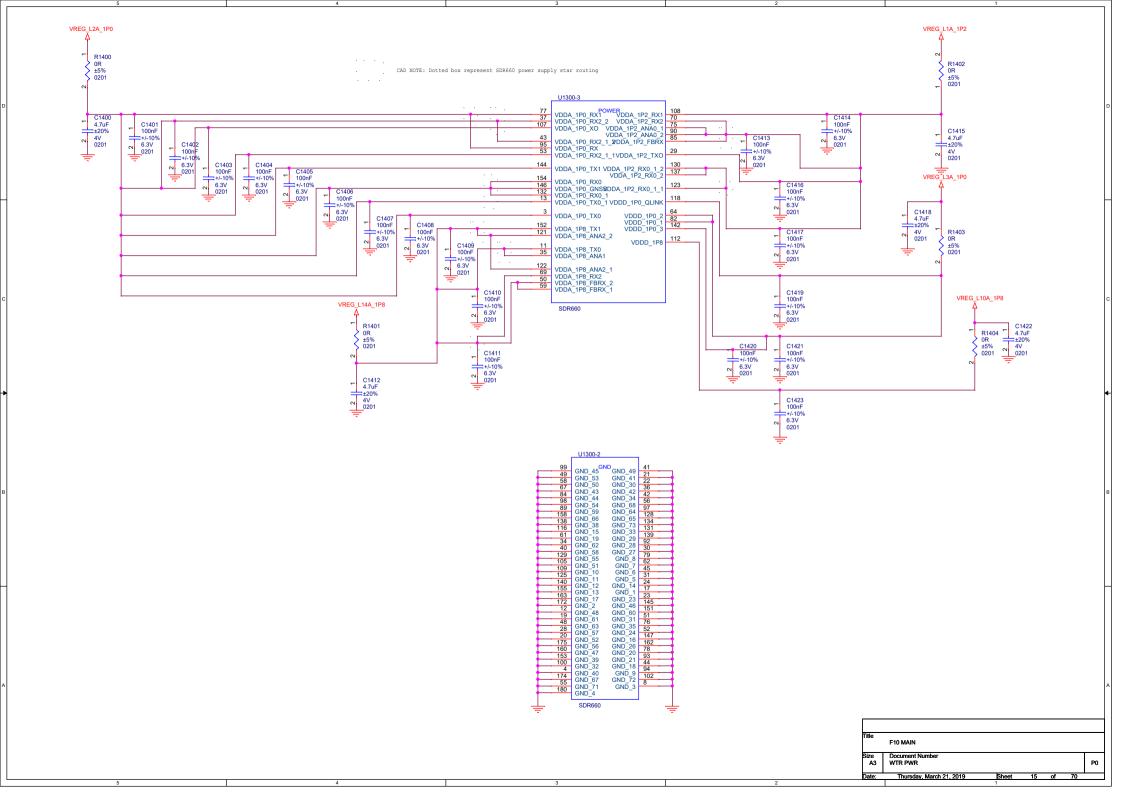


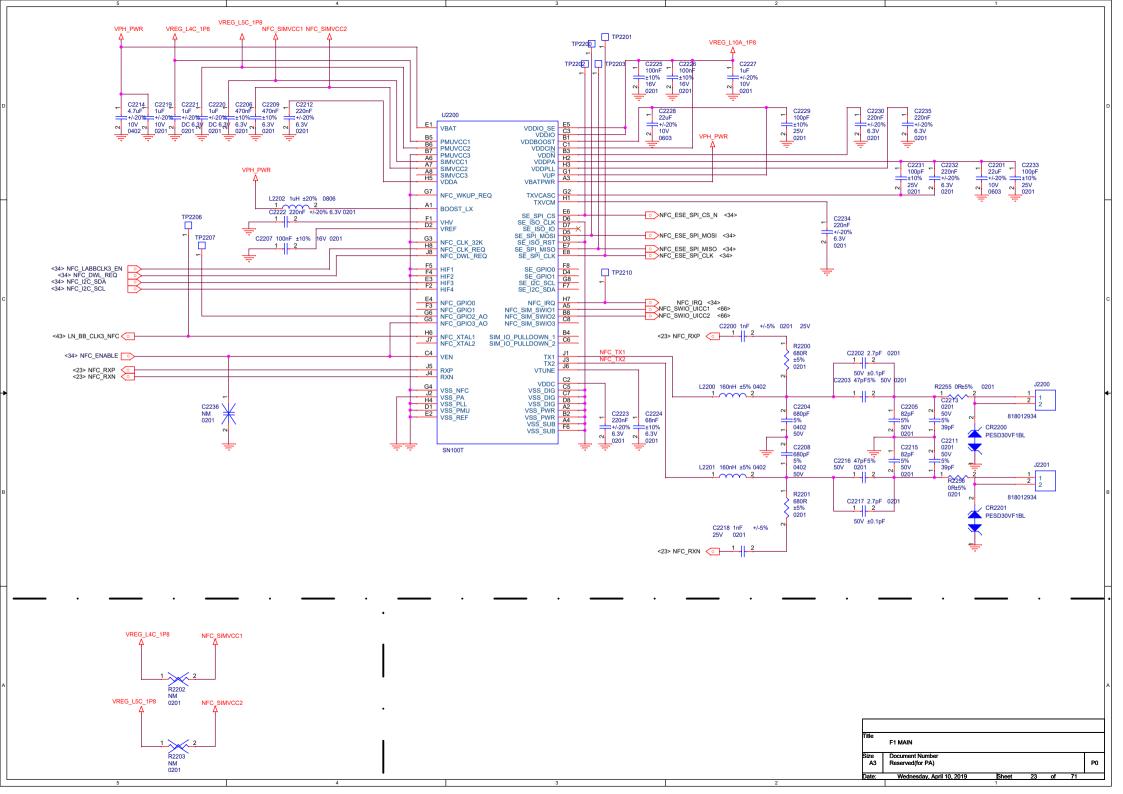


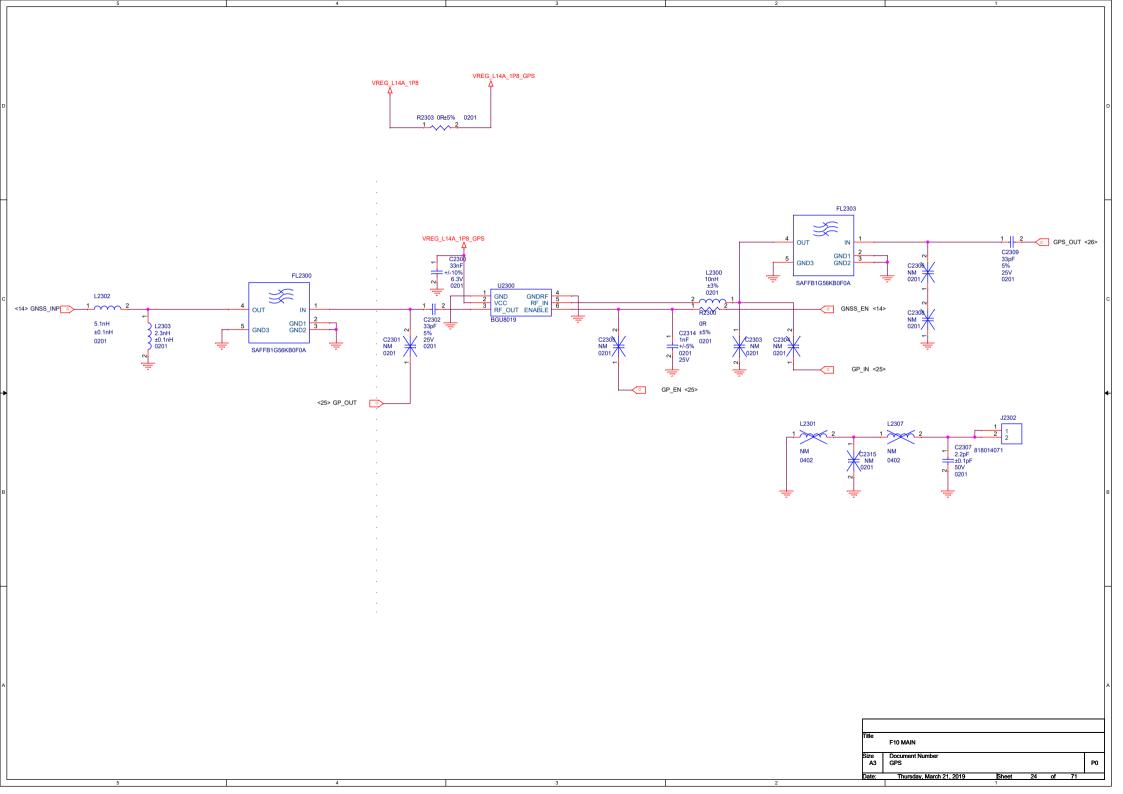


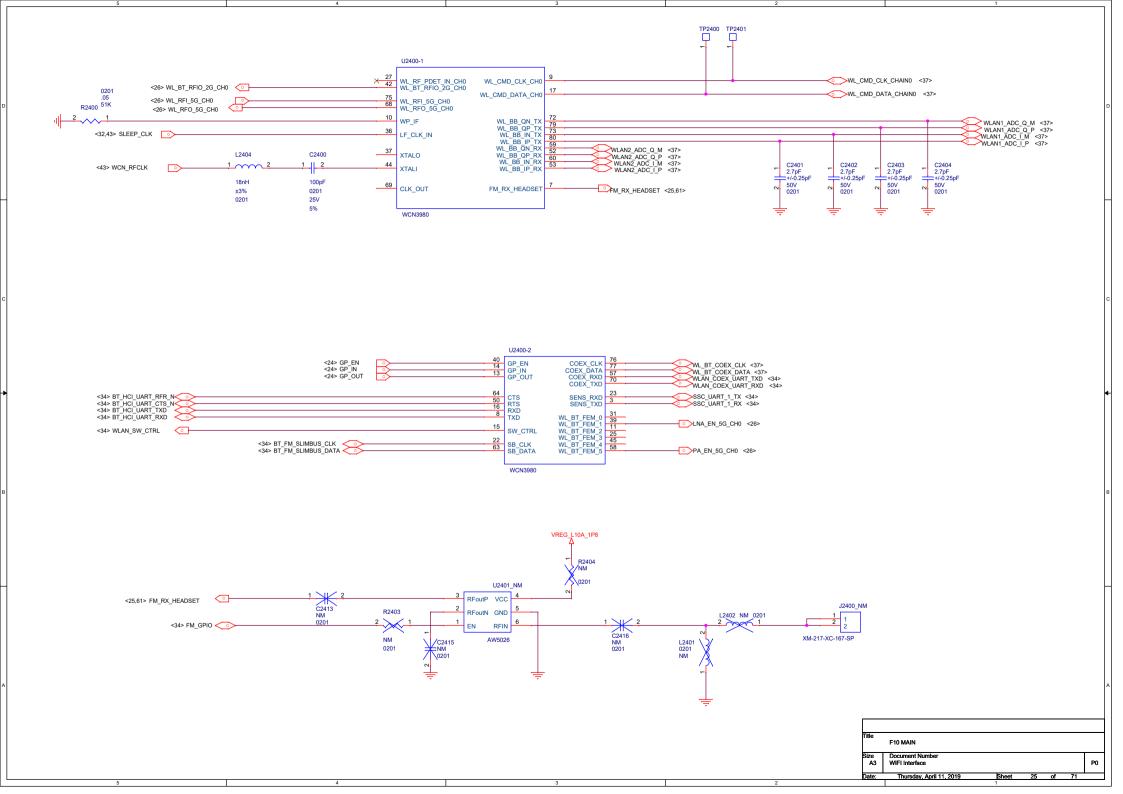


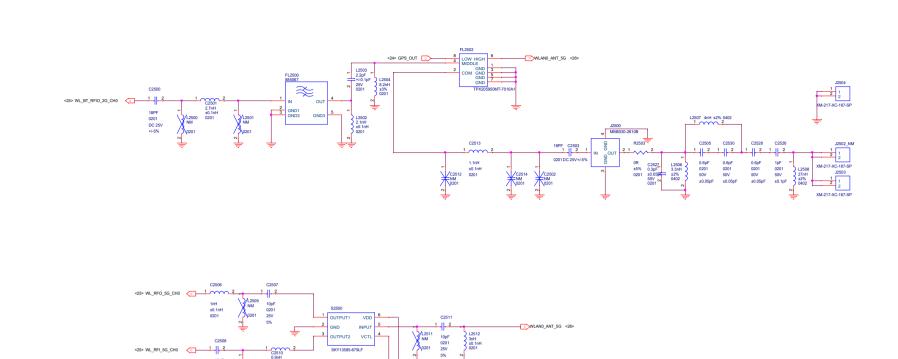












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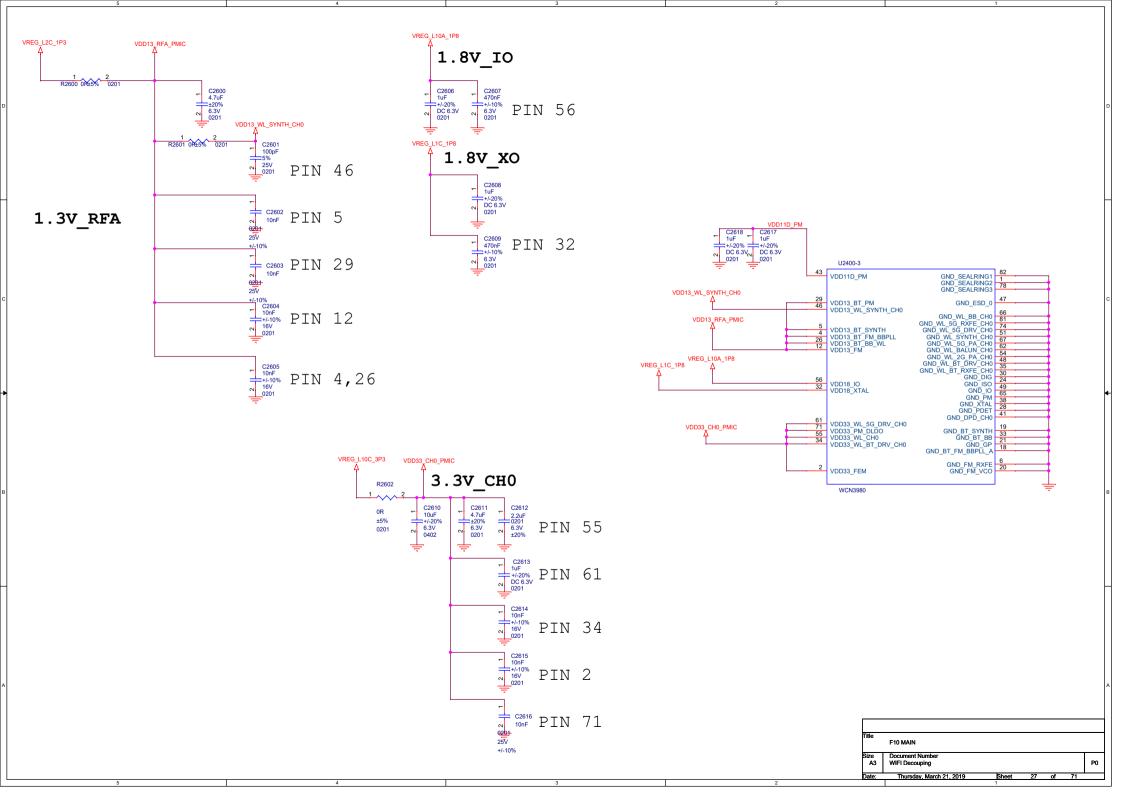
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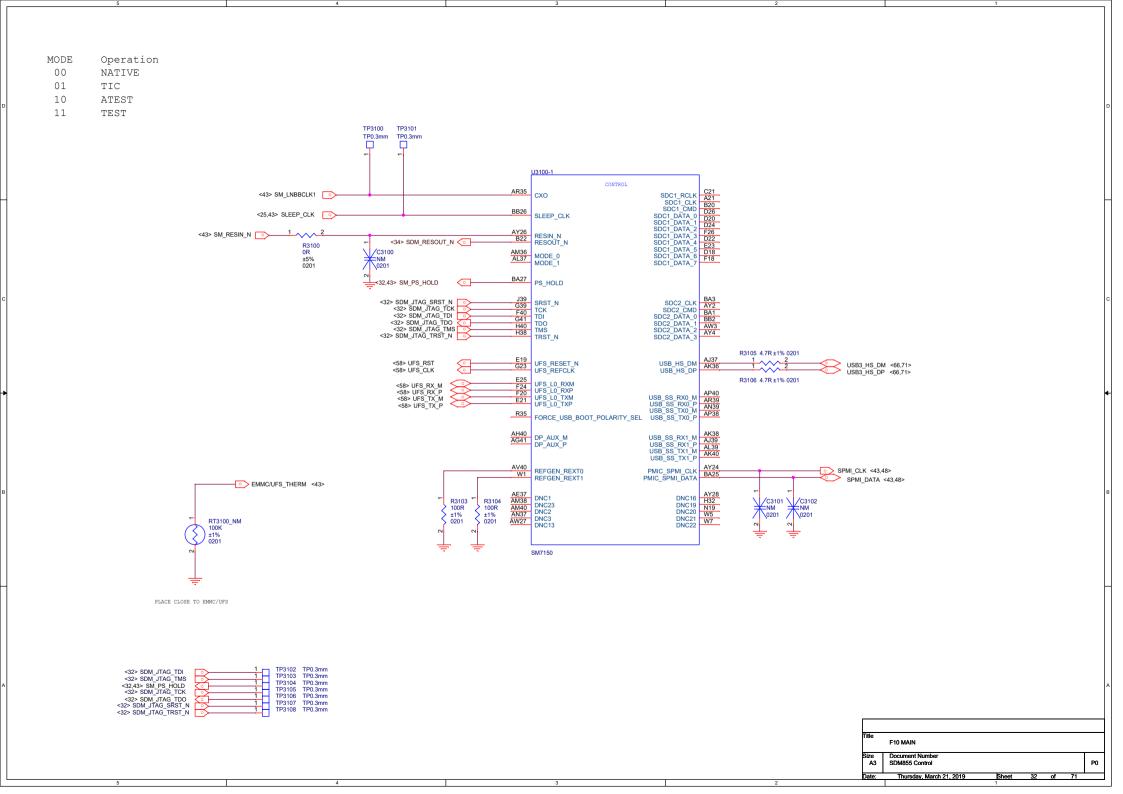
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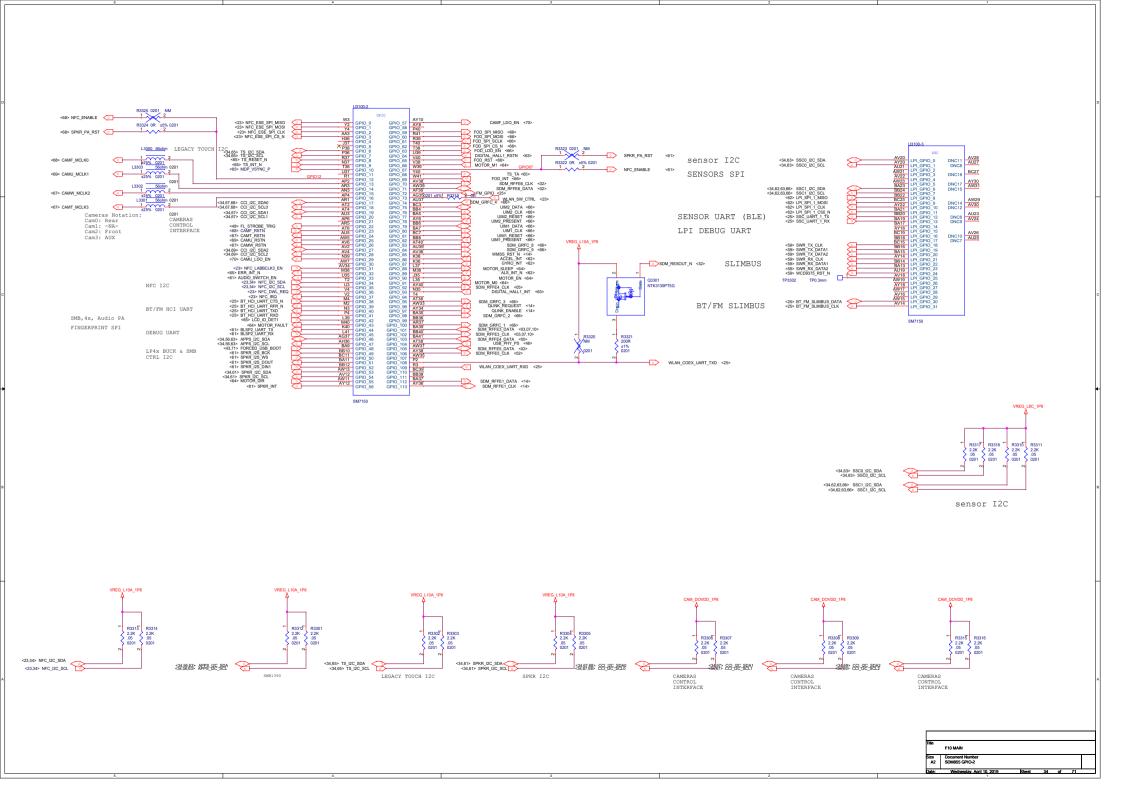


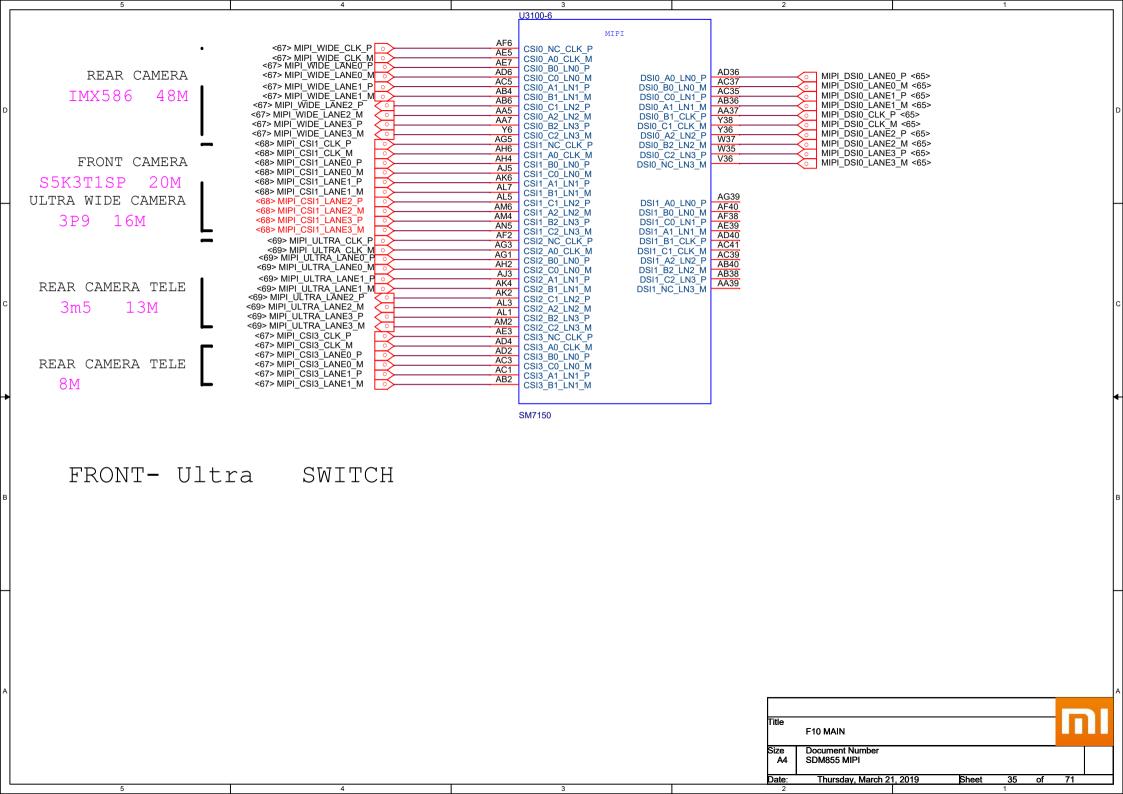


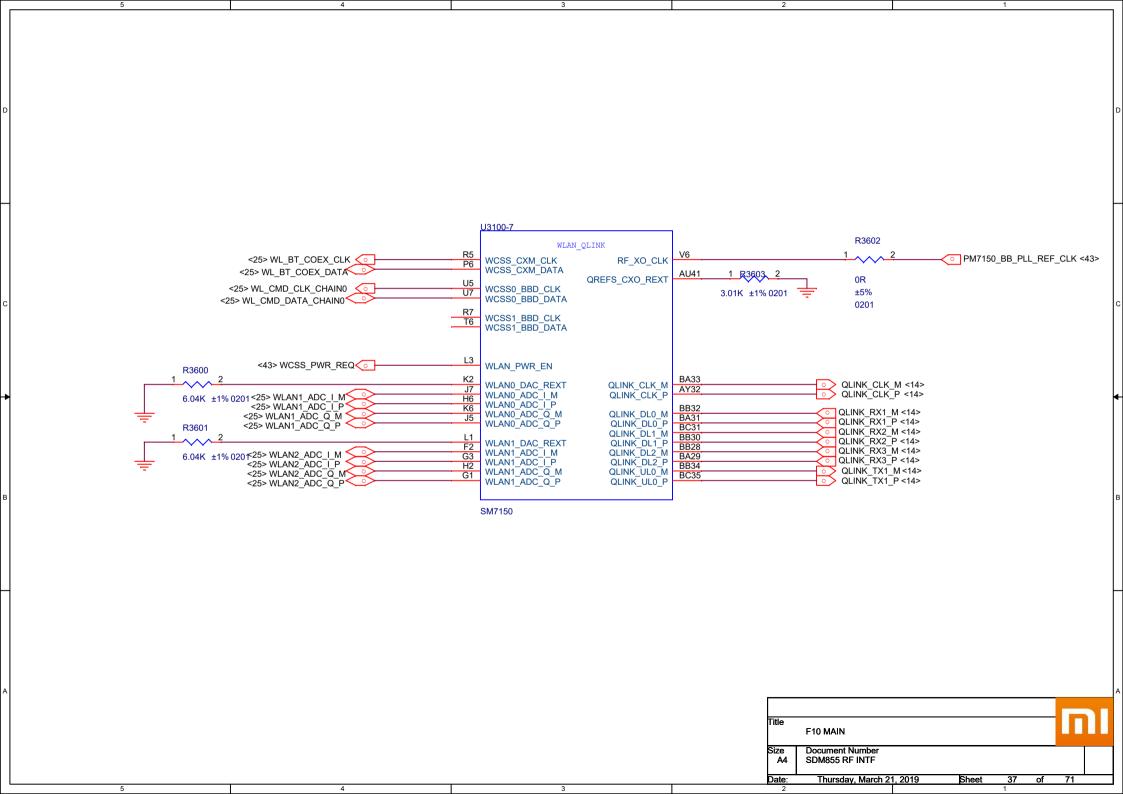
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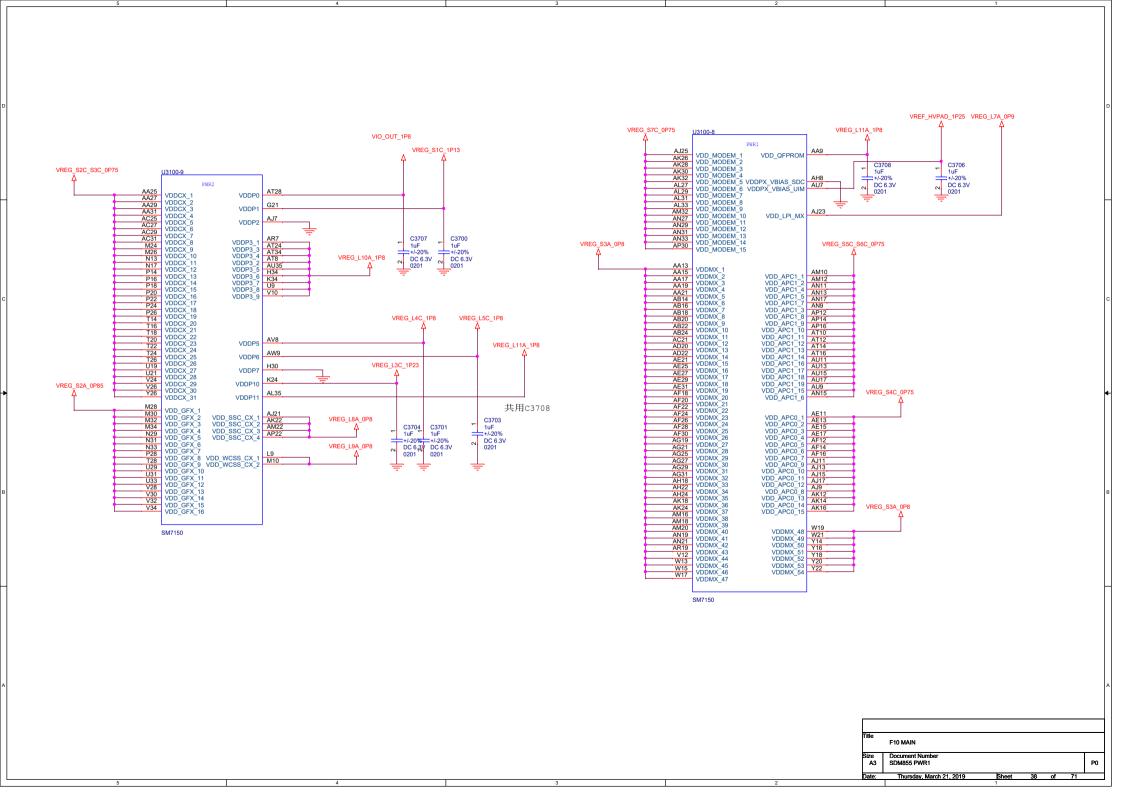
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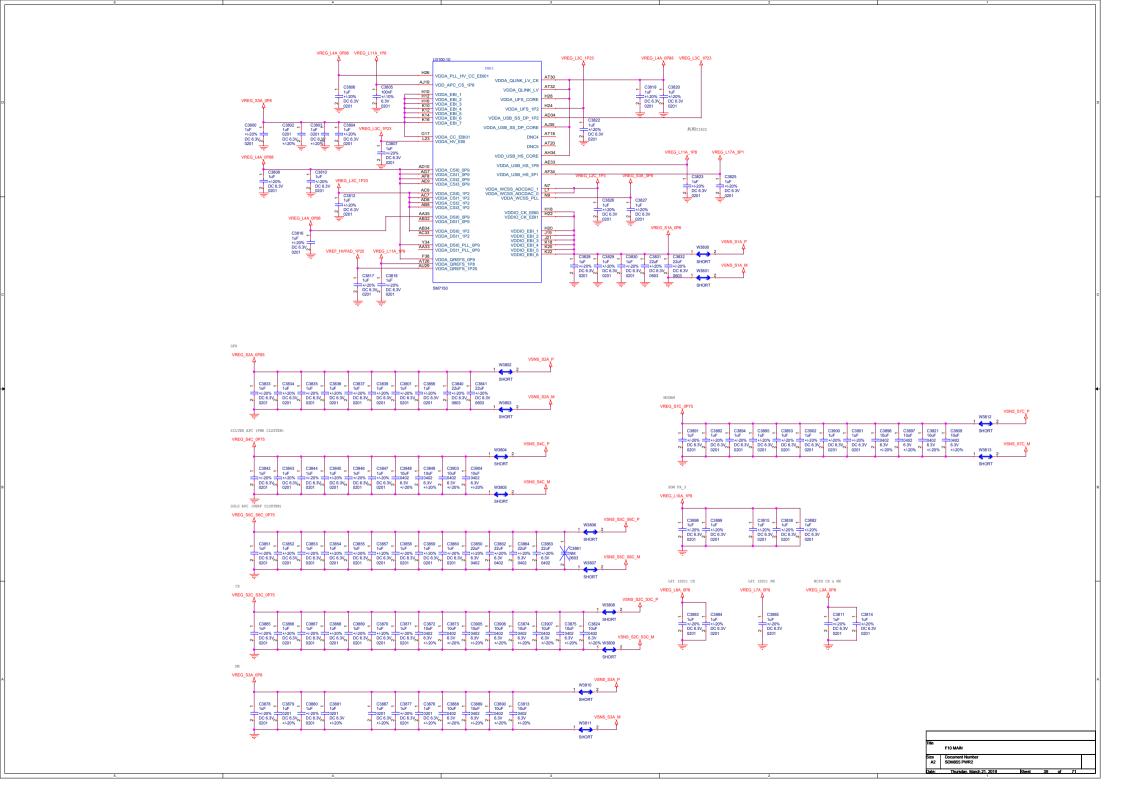
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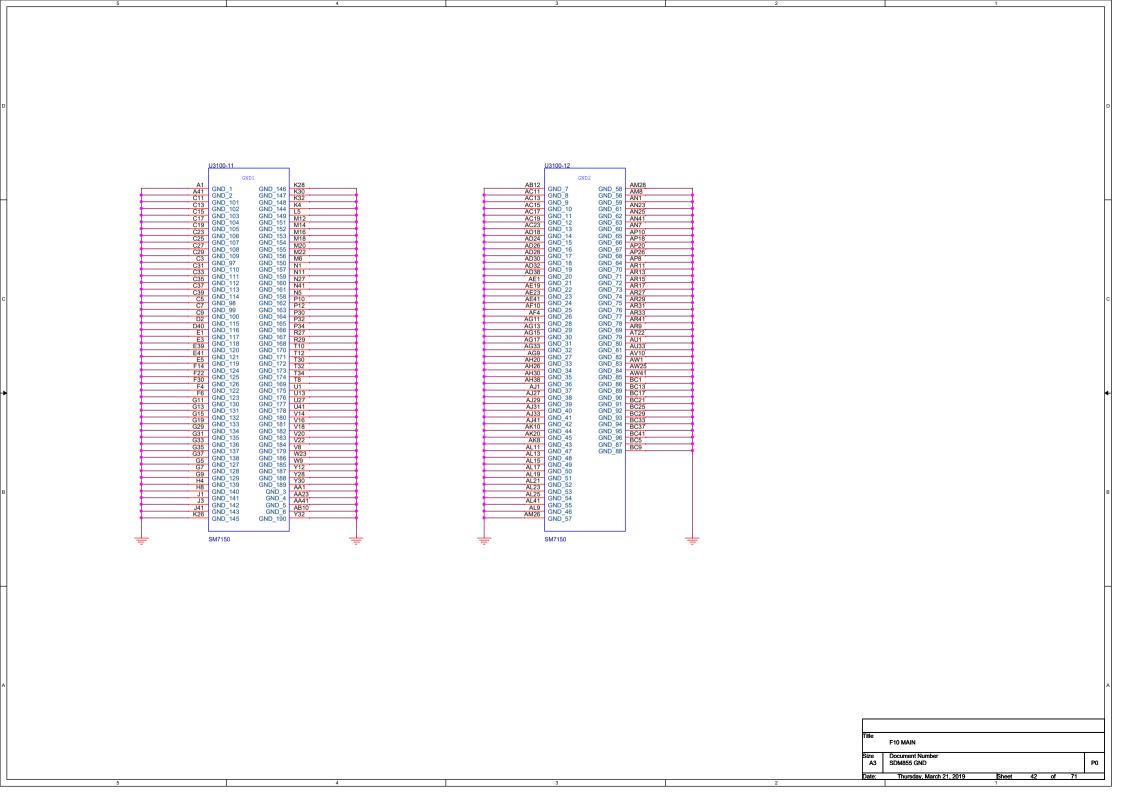


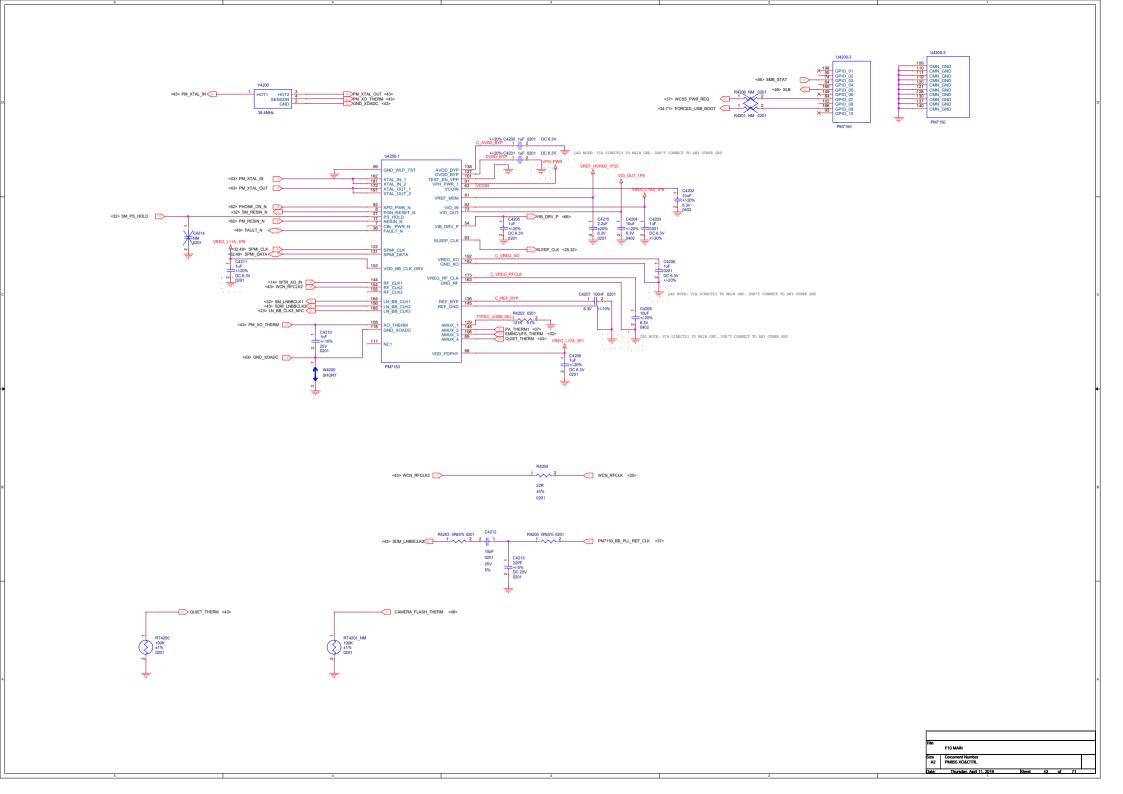


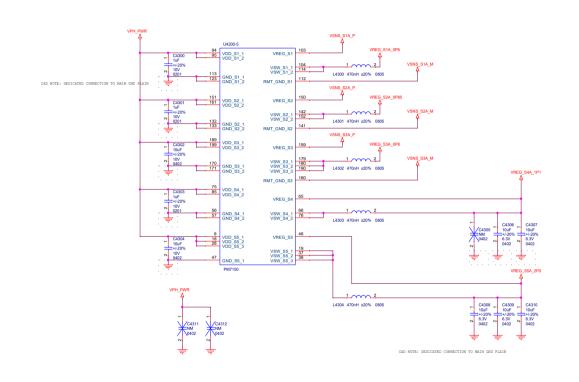




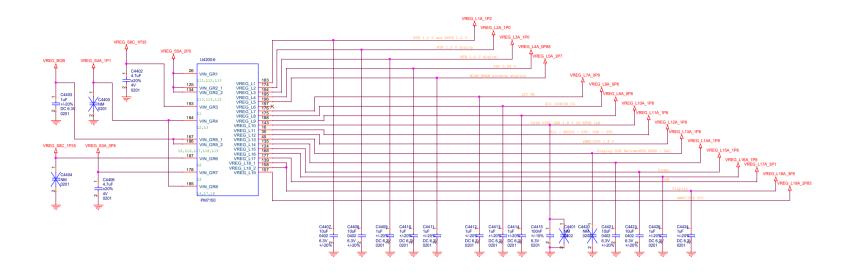






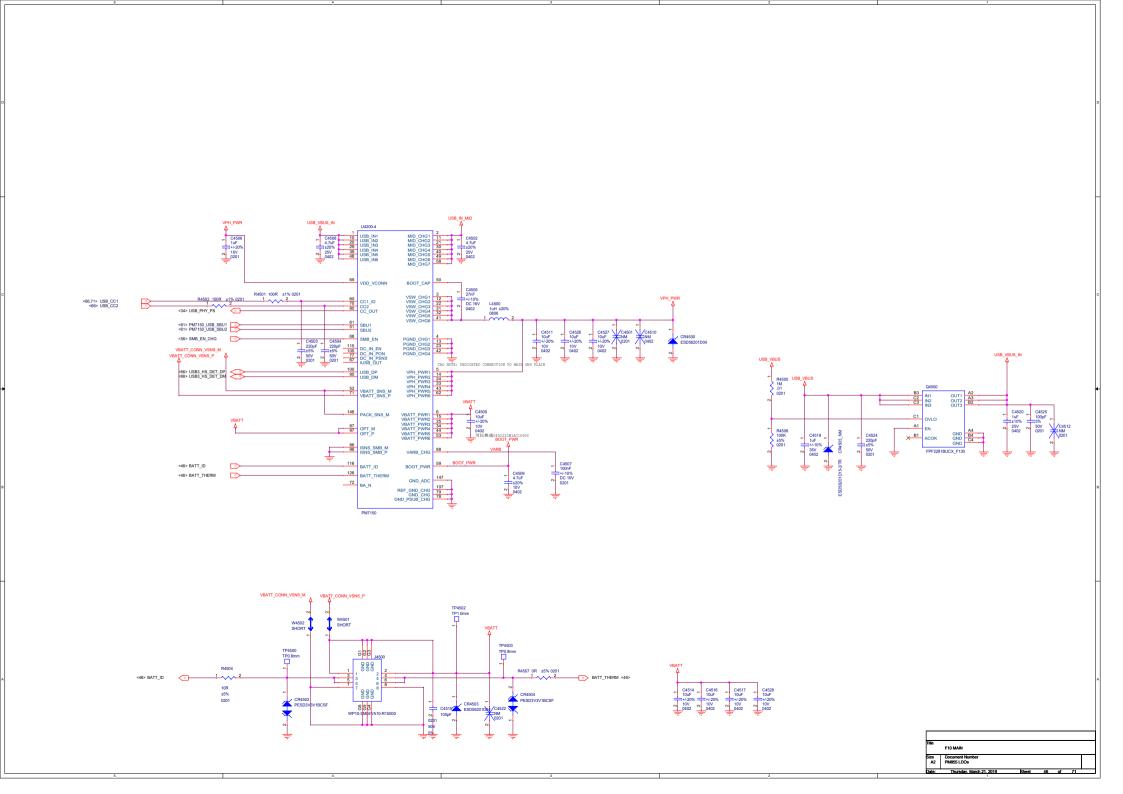


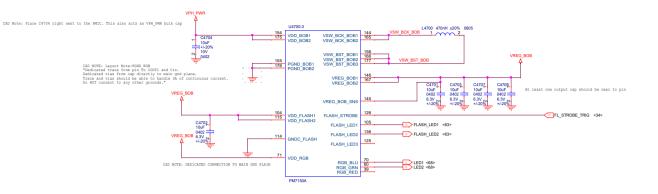
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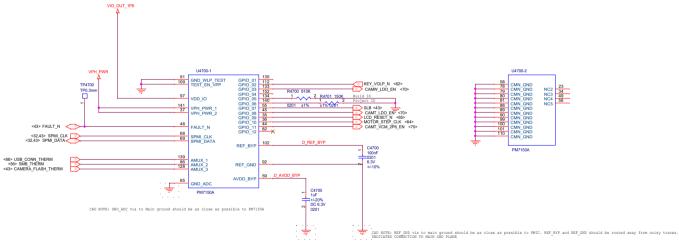




PSEUDO CAPLESS LDOs For CAPLESS LDOs: If decaps on the load side do not add up to LDO spec, then install the cap close to the PMIC

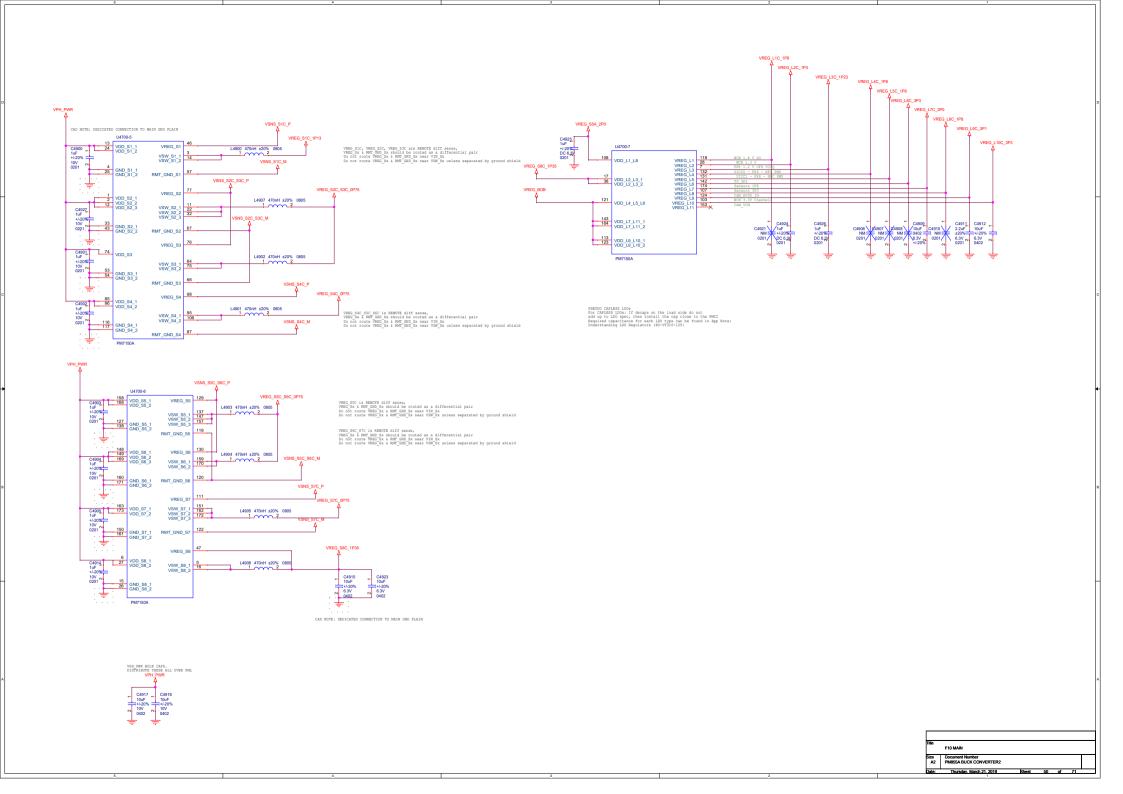


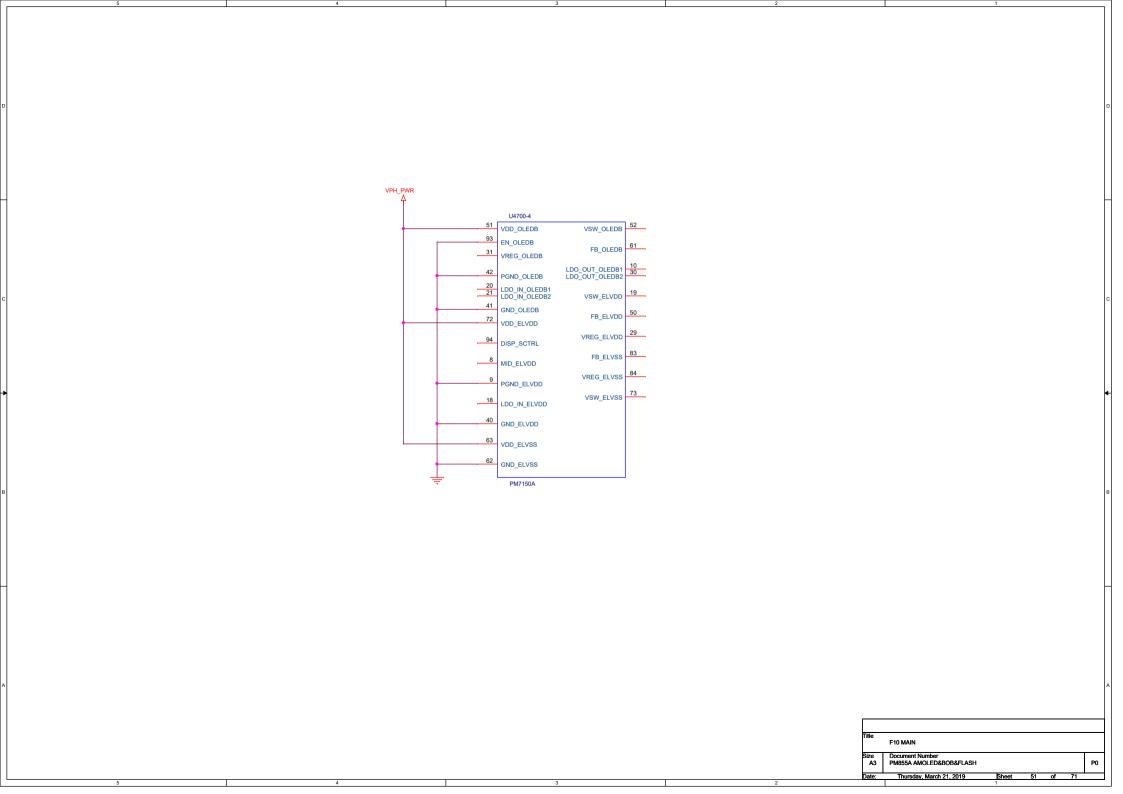


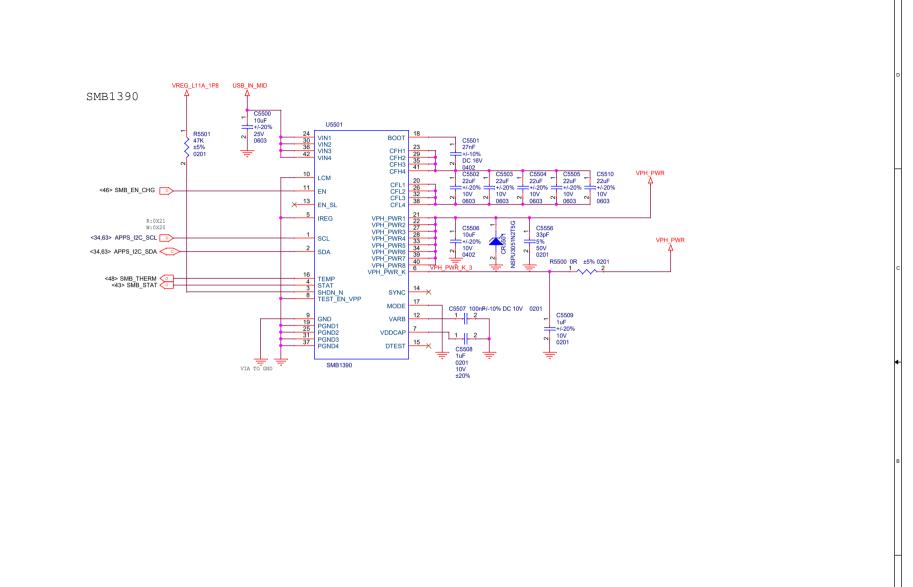


CAD NOTE: AVDD\_BYP should be routed away from noisy traces . DEDICATED CONNECTION TO MAIN GND PLANE

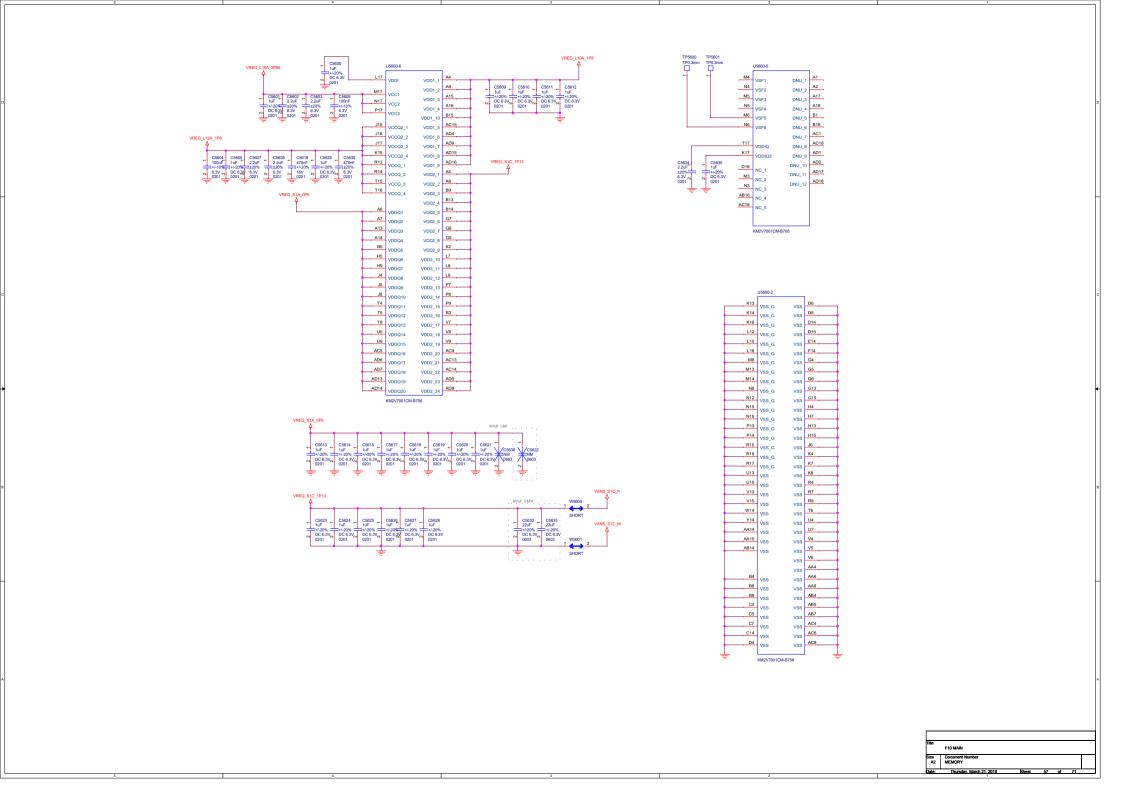
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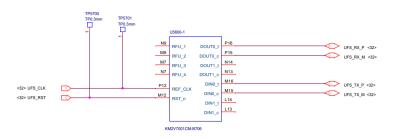




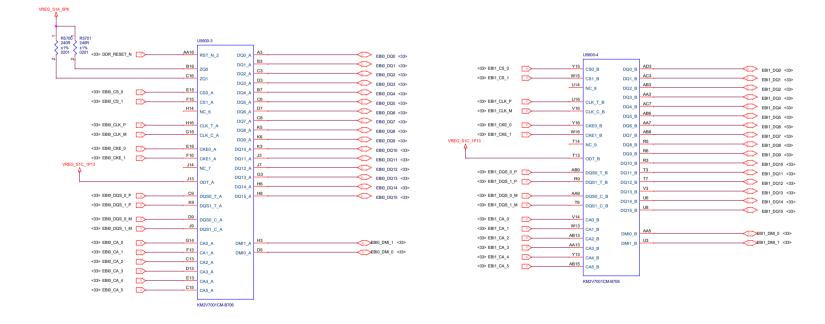
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## **eMMC**



## LPDDR4/4x



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