Current as of D11 MCO 056-01585 rev. 63

Contained in radio_mlb pages

BS0415
2.70R1.80-NSP
UP_RFFE

BS0401
2.70R1.80-NSP
CHASSIS_GND_BS401

BS0402
STDOFF-2.90D0.888H-SM
CHASSIS_GND_BS402

BS0403
STDOFF-2.90D0.81H-SM
CHASSIS_GND_BS403

NEO Stiffener

NORTH_SCREW_EXPOSED

#25046211

C0413 220PF 5% 10V C0G-CERM 01005
C0414 56PF 5% 25V NP0-C0G-CERM 01005
C0415 18PF 2% 16V CERM 01005
C0416 4PF +/-0.1PF 16V NP0-C0G 01005

PTH per Rev63 for 1.8mm Drill

CHASSIS_GND_BS401
C0401 220PF 5% 10V C0G-CERM 01005
C0402 220PF 5% 10V C0G-CERM 01005
C0403 100PF 5% 16V NP0-C0G 01005
C0404 56PF 5% 25V NP0-C0G-CERM 01005
C0405 18PF 2% 16V CERM 01005
C0406 4PF +/-0.1PF 16V NP0-C0G 01005

CHASSIS_GND_BS402
C0407 220PF 5% 10V C0G-CERM 01005
C0408 220PF 5% 10V C0G-CERM 01005
C0409 100PF 5% 16V NP0-C0G 01005
C0410 56PF 5% 25V NP0-C0G-CERM 01005
C0411 18PF 2% 16V CERM 01005
C0412 4PF +/-0.1PF 16V NP0-C0G 01005

CHASSIS_GND_BS403
C0417 220PF 5% 10V C0G-CERM 01005
C0418 220PF 5% 10V C0G-CERM 01005
C0419 100PF 5% 16V NP0-C0G 01005
C0420 56PF 5% 25V NP0-C0G-CERM 01005
C0421 18PF 2% 16V CERM 01005
C0422 4PF +/-0.1PF 16V NP0-C0G 01005

Front Shields

SH0401 SM — SHLD-UP-FRT-D11

SH0403 SM — SHLD-LOWER-FRT-D11

BS0404
2.70R1.80-NSP

Back Shields

SH0400 SM — SHLD-SOFT-UP-BK-D11

SH0402 SM — SHLD-SOFT-LOWER-BK-D11

BS0405
STDOFF-2.90D0.888H-SM

BS0406
STDOFF-2.90D1.9ID-0.85H-SM

CLIP-COAX-RETENTION-D11
CL0401 SM

TESTPOINTS

POWER

TP0420 TP-P55 ROOM=TEST — POWER GROUND

PP5V0_USB → TP0421 TP-P55 ROOM=TEST — VBUS

PP_BATT_VCC → TP0415 TP-P55 ROOM=TEST — VBATT

TP0422 TP-P55 ROOM=TEST

PP_VDD_MAIN → TP0408 TP-P55 ROOM=TEST — VDD_MAIN

FD0408 FID 0P5SM1P0SQ-NSP ROOM=TEST
Note: Fiducial used as test point

DFU

PMU_TO_AP_FORCE_DFU → TP0414 TP-P55 ROOM=TEST — FORCE DFU

E75

90_TRISTAR_DP1_CONN_P → TP0402 TP-P55 ROOM=TEST

90_TRISTAR_DP1_CONN_N → TP0403 TP-P55 ROOM=TEST

90_TRISTAR_DP2_CONN_P → TP0404 TP-P55 ROOM=TEST

90_TRISTAR_DP2_CONN_N → TP0405 TP-P55 ROOM=TEST

PP_TRISTAR_ACC1 → TP0406 TP-P55 ROOM=TEST

PP_TRISTAR_ACC2 → TP0407 TP-P55 ROOM=TEST — ACCESSORY ID AND POWER

TP0416 TP-P55 ROOM=TEST — TP IS TO HELP WITH USB SI IN THE FACTORY FIXTURE.

TRISTAR_CON_DETECT_L → TP0412 TP-P55 ROOM=TEST — FOR DIAGS

AMUX

PMU_AMUX_AY → TP0413 TP-P55 ROOM=TEST — ANALOG MUX A OUTPUT

#25244799
100k to 200k
R0413 200K 1% 1/32W MF 01005 ROOM=SOC

PMU_AMUX_BY → TP0423 TP-P55 ROOM=TEST — ANALOG MUX B OUTPUT
Note: Fiducial used as test point

MOJAVE

MESA_TO_BOOST_EN → TP0400 TP-P55 ROOM=TEST

PP16V0_MESA → TP0401 TP-P55 ROOM=TEST

LCM

PP_LCM_BL_CAT1_CONN → TP0409 TP-P55 ROOM=TEST — LCM BACKLIGHT SINK1

PP_LCM_BL_CAT2_CONN → TP0410 TP-P55 ROOM=TEST — LCM BACKLIGHT SINK2

PP_LCM_BL_ANODE_CONN → TP0411 TP-P55 ROOM=TEST — LCM BACKLIGHT SOURCE

PP_LCM_BL34_CAT1_CONN → TP0417 TP-P55 ROOM=TEST — LCM BACKLIGHT SINK3

PP_LCM_BL34_CAT2_CONN → TP0419 TP-P55 ROOM=TEST — LCM BACKLIGHT SINK4

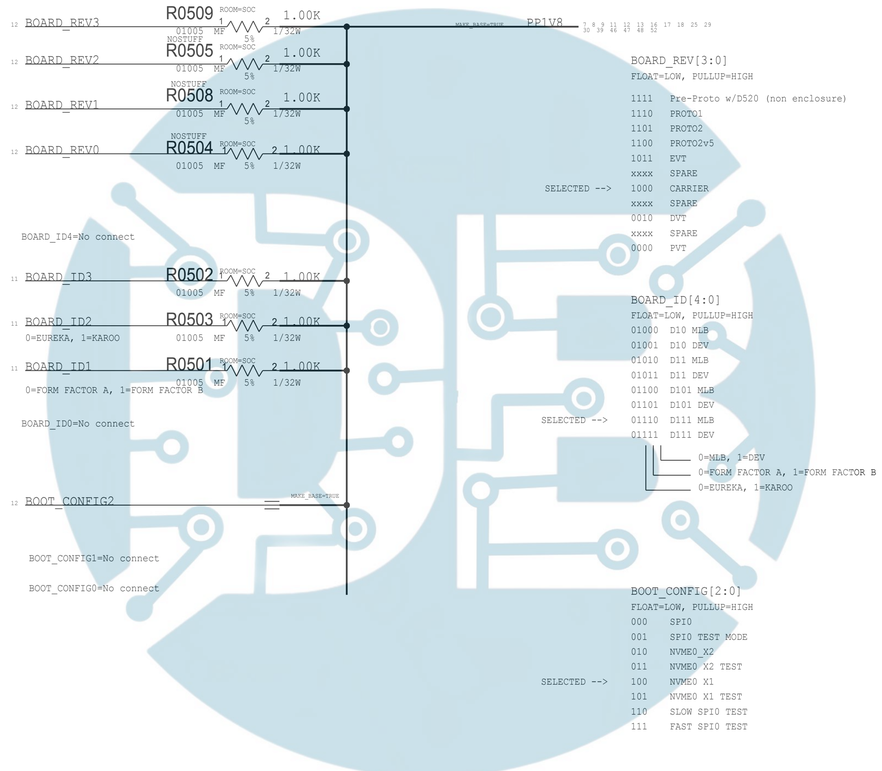
PP_LCM_BL34_ANODE_CONN → TP0418 TP-P55 ROOM=TEST — LCM BACKLIGHT SOURCE (3/4)

FIDUCIALS

FD0410 FID 0P5SM1P0SQ-NSP ROOM=ASSEMBLY
FD0409 FID 0P5SM1P0SQ-NSP ROOM=ASSEMBLY
FD0405 FID 0P5SM1P0SQ-NSP ROOM=ASSEMBLY
FD0406 FID 0P5SQ-SMP3SQ-NSP ROOM=ASSEMBLY
FD0404 FID 0P5SQ-SMP3SQ-NSP ROOM=ASSEMBLY
FD0403 FID 0P5SQ-SMP3SQ-NSP ROOM=ASSEMBLY
FD0402 FID 0P5SQ-SMP3SQ-NSP ROOM=ASSEMBLY
FD0401 FID 0P5SQ-SMP3SQ-NSP ROOM=ASSEMBLY
FD0400 FID 0P5SQ-SMP3SQ-NSP ROOM=ASSEMBLY
FD0407 FID 0P5SM1P0SQ-NSP ROOM=TEST
FD0411 FID 0P5SQ-SMP3SQ-NSP

TOP SIDE

BOOTSTRAPPING:BOARD REV
BOARD ID
BOOT CONFIG



SOC - USB, JTAG, XTAL

VDD18_USB: 1.71-1.89V @20mA MAX

PP1V8

C0700
0.1UF
20%
2.3V
X5R-CERM
01005
ROOM=SOC

FL0700
240-OHM-25%-0.20A-0.9DCR
01005
ROOM=SOC

VDD11_XTAL:1.06-1.17V @TBD mA MAX

PP1V1_XTAL

C0704
0.1UF
20%
2.3V
X5R-CERM
01005
ROOM=SOC

PP1V1

C0705
2.2UF
20%
2.3V
X5R-CERM
0201-1
ROOM=SOC

VDD18_AMUX: 1.62-1.98V @1mA MAX

PP1V8

PP3V3_USB

C0701
0.1UF
20%
2.3V
X5R-CERM
01005
ROOM=SOC

3.14-3.46V @20mA MAX

CKPLUS_WAIVE=PWRTERM2GND

PP0V9_SOC_FIXED

tbd - tbd V @5mA MAX

U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 1 OF 16

CL20 VDD12_UH1_HSIC0
AJ60 VDD18_AMUX
CE25 VDD18_USB
CG50 VDD11_XTAL
CG26 VDD33_USB
CC25 VDD_FIXED_USB

Dev ONLY

PP0701
P2MM-NSM
SM

NC CM22 UH1_HSIC0_DATA
NC CM20 UH1_HSIC0_STB

CL31 JTAG_SEL
NC CL29 JTAG_TRST*
NC CJ37 JTAG_TDO
NC CJ35 JTAG_TDI
NC CK33 JTAG_TMS
CH37 JTAG_TCK
CM14 COLD_RESET*
BJ3 CFSB
BJ2 TST_CLKOUT
BL65 S3E_RESET*
BJ4 HOLD_RESET
BL3 TESTMODE

SWD_DOCK_BI_AP_SWDIO
SWD_DOCK_TO_AP_SWCLK
PMU_TO_SYSTEM_COLD_RESET_L
PMU_TO_AOP_TRISTAR_ACTIVE_READY
AP_TO_PMU_TEST_CLKOUT
AP_TO_NAND_RESET_L

ANALOGMUX_OUT N64 AP_TO_PMU_AMUX_OUT

USB_DP CM26 90_USB_AP_DATA_P
USB_DM CL26 90_USB_AP_DATA_N

USB_VBUS CH26 USB_VBUS_DETECT

USB_ID CJ26 NC

USB_REXT CK26 AP_USB_REXT

R0700
200
1%
1/32W
MF
01005
ROOM=SOC

WDOG CK35 AP_TO_PMU_WDOG_RESET

XI0 CM42 XTAL_AP_24M_IN
XO0 CL42 XTAL_AP_24M_OUT

R0701
511K
1%
1/32W
MF
01005
ROOM=SOC

R0702
0.00
0%
1/32W
MF
01005
ROOM=SOC

CRITICAL
ROOM=SOC
Y0700
1.60X1.20MM-SM
24.000MHZ-30PPM-9.5PF-60OHM

SOC_24M_Q

C0702
12PF
5%
16V
CERM
01005
ROOM=SOC

C0703
12PF
5%
16V
CERM
01005
ROOM=SOC

SOC - PCIE INTERFACES

R0804 0.00 0% 1/32W MF 01005 ROOM=SOC
VDD12_PCIE_REFBUF:1.08-1.26V @40mA MAX
PP1V2_SOC_PCIE_REFBUF
C0802 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
VDD_FIXED_PCIE_xxx:0.855-0.990V @225mA MAX
PP0V9_SOC_FIXED
R0803 0.00 0% 1/32W MF 01005 ROOM=SOC
C0803 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C0800 1.0UF 20% 6.3V X5R 0201-1 ROOM=SOC
C0806 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
PP0V9_SOC_FIXED_PCIE_REFBUF
C0804 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
PP1V2_SOC
VDD12_PCIE: 1.14-1.26V @10mA MAX
C0805 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C0801 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
CE58 VDD12_PCIE
CC49 CE49 VDD12_PCIE_REFBUF
CA55 CA60 VDD_FIXED_PCIE_CLK
CC53 CC62 CE55 CE60 VDD_FIXED_PCIE_ANA
BW55 CC47 VDD_FIXED_PCIE_REFBUF
PP1V8
R0805 100K 5% 1/32W MF 01005 ROOM=SOC

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SYM 2 OF 16

PCIE_NAND_BI_AP_CLKREQ_L → BC64 PCIE_CLKREQ0*
90_PCIE_AP_TO_NAND_REFCLK_P → CJ48 PCIE_REF_CLK0_P
90_PCIE_AP_TO_NAND_REFCLK_N → CK48 PCIE_REF_CLK0_N

#24557655:replace with 20% caps. SI no negative impact

C0807 0.22UF 20% X5R 6.3V 01005 GND_VOID=TRUE ROOM=SOC
90_PCIE_NAND_TO_AP_RXD_P → CM46 PCIE_RX0_P
C0808 0.22UF 20% X5R 6.3V 01005 GND_VOID=TRUE ROOM=SOC
90_PCIE_NAND_TO_AP_RXD_N → CL46 PCIE_RX0_N

D10 NAND is now Gen3 (was Gen2). Caps intentionally 0.22uF

C0809 0.22UF 20% X5R 6.3V 01005 GND_VOID=TRUE ROOM=SOC
90_PCIE_AP_TO_NAND_TXD_P → CK44 PCIE_TX0_P
C0810 0.22UF 20% X5R 6.3V 01005 GND_VOID=TRUE ROOM=SOC
90_PCIE_AP_TO_NAND_TXD_N → CJ44 PCIE_TX0_N
PCIE_AP_TO_NAND_RESET_L → BJ65 PCIE_PERST0*
R0802 100K 5% 1/32W MF 01005 ROOM=SOC

LINK0 LINK3

NC BG66 PCIE_CLKREQ1*
NC CL54 PCIE_REF_CLK1_P
NC CJ54 PCIE_REF_CLK1_N
NC CK52 PCIE_RX1_P
NC CJ52 PCIE_RX1_N
NC CM50 PCIE_TX1_P
NC CL50 PCIE_TX1_N
NC BG64 PCIE_PERST1*

LINK1 LINK2

CH57 PCIE_EXT_REF_CLK_P
CG57 PCIE_EXT_REF_CLK_N

PCIE_CLKREQ3* BE66 AP_PCIE_CLKREQ3_L
PCIE_REF_CLK3_P CL64 90_AP_PCIE3_REFCLK_P
PCIE_REF_CLK3_N CM64 90_AP_PCIE3_REFCLK_N
PCIE_RX3_P CM61 90_AP_PCIE3_RXD_C_P
PCIE_RX3_N CL61 90_AP_PCIE3_RXD_C_N
PCIE_TX3_P CK63 90_AP_PCIE3_TXD_C_P
PCIE_TX3_N CJ63 90_AP_PCIE3_TXD_C_N
PCIE_PERST3* BJ66 AP_PCIE_RESET3_L
R0806 100K 5% 1/32W MF 01005 ROOM=SOC

PCIE_CLKREQ2* BE65 AP_PCIE_CLKREQ2_L
PCIE_REF_CLK2_P CK59 90_AP_PCIE2_REFCLK_P
PCIE_REF_CLK2_N CJ59 90_AP_PCIE2_REFCLK_N

WLAN RX PP's are now managed on Page 52

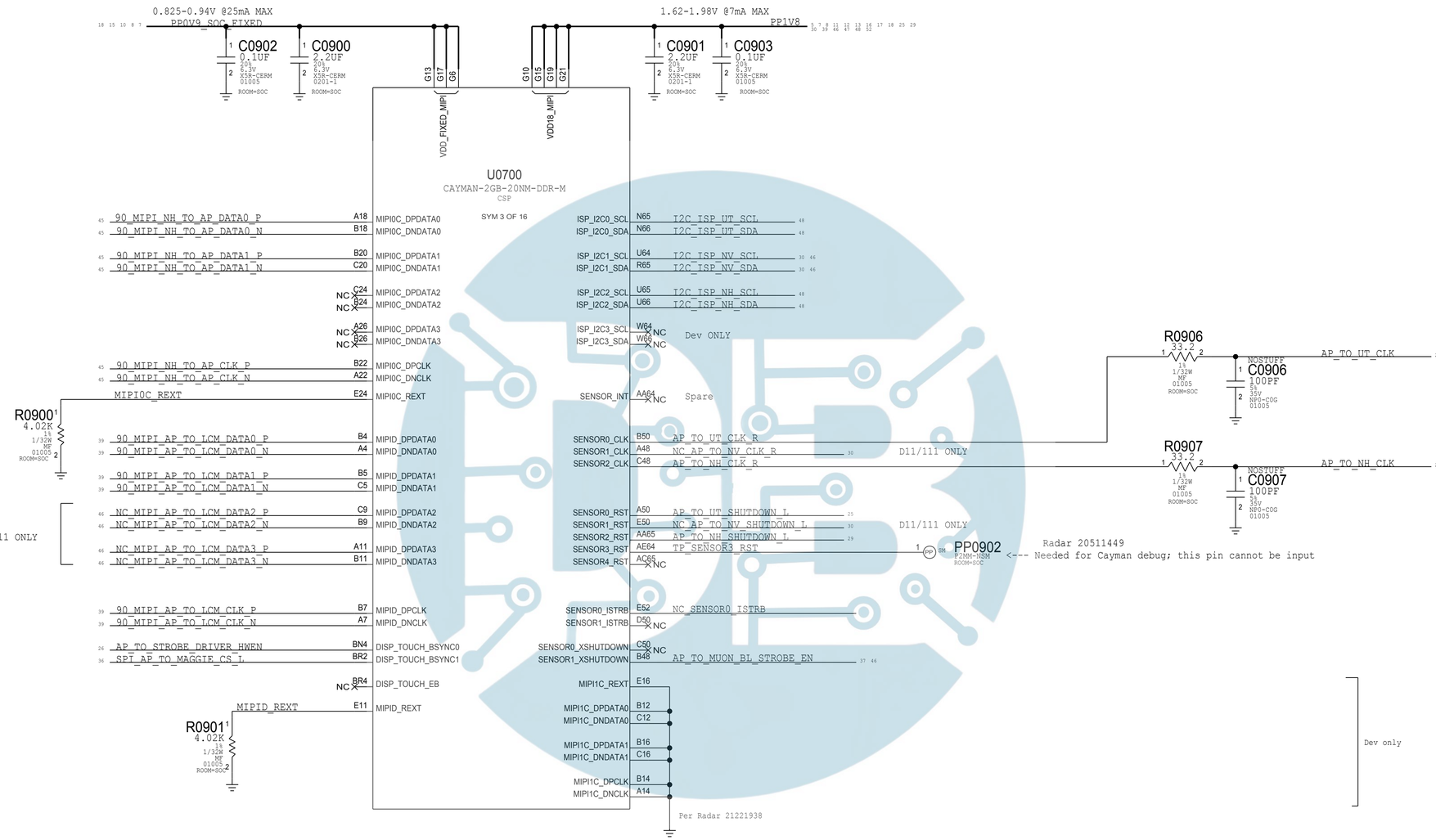
PCIE_RX2_P CK56 90_AP_PCIE2_RXD_C_P
PCIE_RX2_N CJ56 90_AP_PCIE2_RXD_C_N
PCIE_TX2_P CM57 90_AP_PCIE2_TXD_C_P
PCIE_TX2_N CL57 90_AP_PCIE2_TXD_C_N
PCIE_PERST2* BE64 AP_PCIE_RESET2_L
R0801 100K 5% 1/32W MF 01005 ROOM=SOC

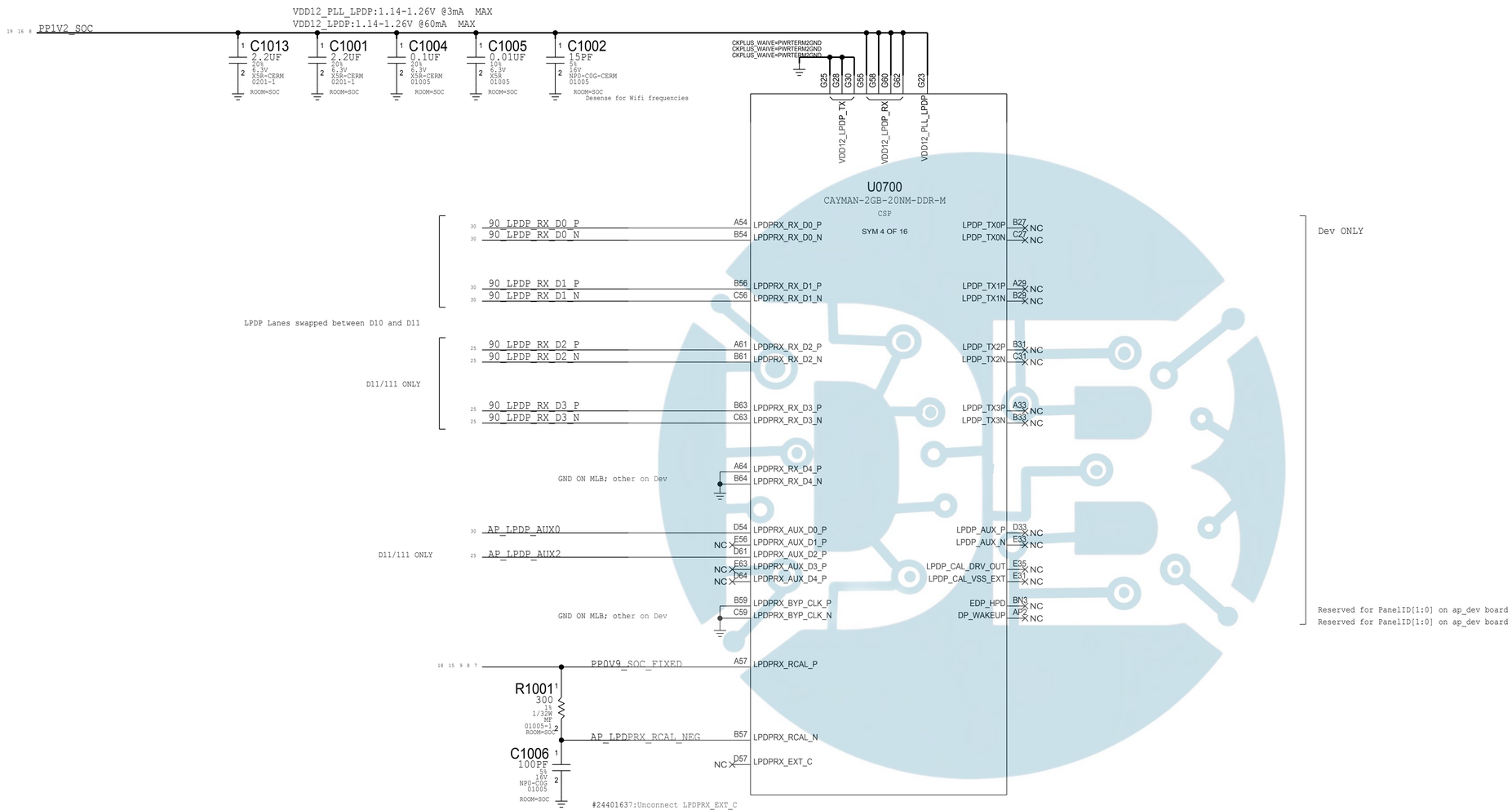
PCIE_REXT CG63 AP_PCIE_RCAL
R0800 9.31K 1% 1/32W MF 01005 ROOM=SOC

PCIE LINK 0
PCIE LINK 1
PCIE LINK 2
PCIE LINK 3

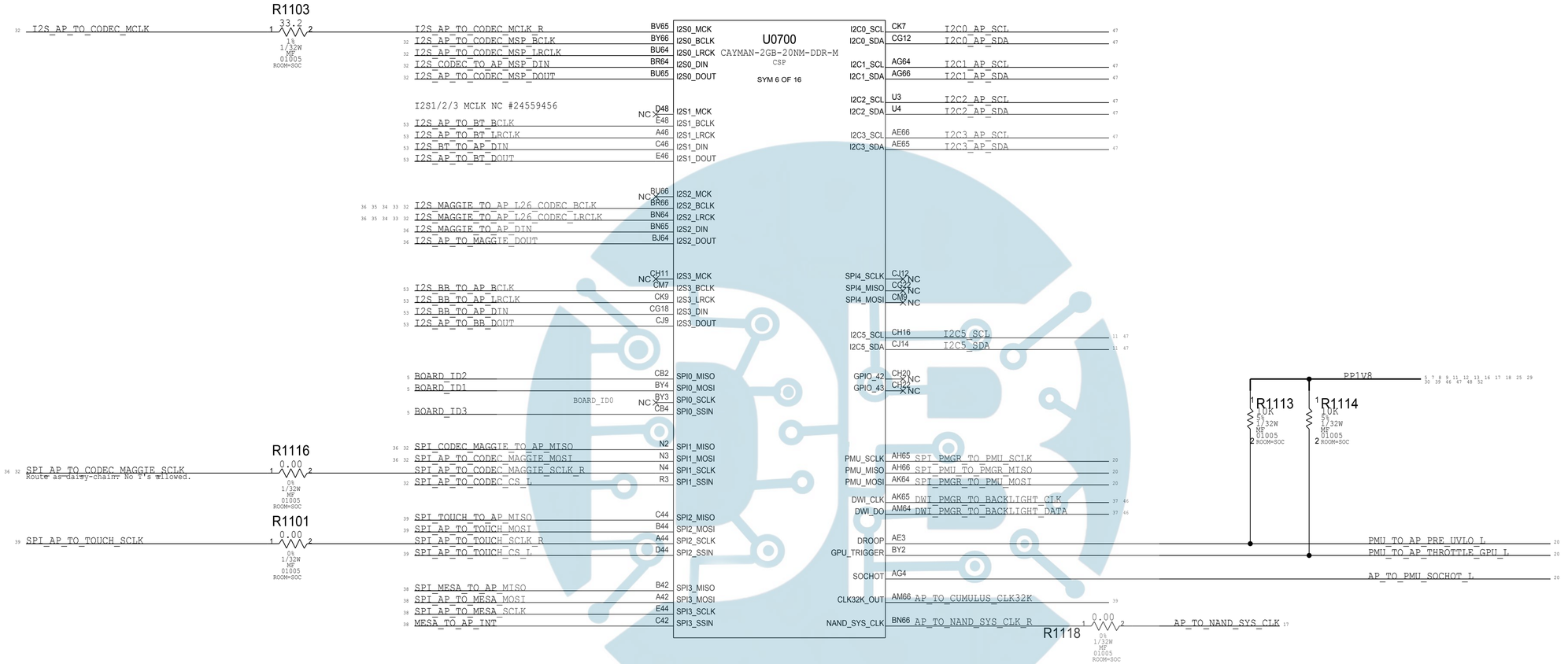
LINK 1 USED ON AP_DEV ONLY

SOC - MIPI & ISP INTERFACES



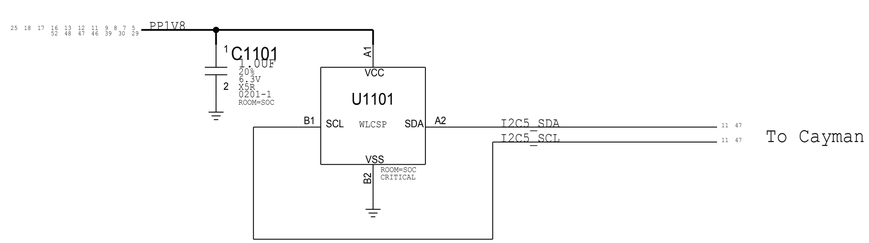

VDD12_PLL_LPDP:1.14-1.26V @3mA MAX
VDD12_LPDP:1.14-1.26V @60mA MAX
PP1V2_SOC
C1013 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1001 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1004 0.1UF 10% 6.3V X5R 01005 ROOM=SOC
C1005 0.01UF 10% 6.3V X5R 01005 ROOM=SOC
C1002 15PF 5% 16V NP0-C0G-CERM 01005 ROOM=SOC
Desense for Wifi frequencies
CKPLUS_WAIVE=PWRTERM2GND
CKPLUS_WAIVE=PWRTERM2GND
CKPLUS_WAIVE=PWRTERM2GND
G25 G28 G30 G55 G58 G60 G62 G23
VDD12_LPDP_TX
VDD12_LPDP_RX
VDD12_PLL_LPDP
U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 4 OF 16
90_LPDP_RX_D0_P A54 LPDPRX_RX_D0_P
90_LPDP_RX_D0_N B54 LPDPRX_RX_D0_N
90_LPDP_RX_D1_P B56 LPDPRX_RX_D1_P
90_LPDP_RX_D1_N C56 LPDPRX_RX_D1_N
LPDP Lanes swapped between D10 and D11
90_LPDP_RX_D2_P A61 LPDPRX_RX_D2_P
90_LPDP_RX_D2_N B61 LPDPRX_RX_D2_N
D11/111 ONLY
90_LPDP_RX_D3_P B63 LPDPRX_RX_D3_P
90_LPDP_RX_D3_N C63 LPDPRX_RX_D3_N
A64 LPDPRX_RX_D4_P
B64 LPDPRX_RX_D4_N
GND ON MLB; other on Dev
AP_LPDP_AUX0 D54 LPDPRX_AUX_D0_P
NC E56 LPDPRX_AUX_D1_P
D11/111 ONLY AP_LPDP_AUX2 D61 LPDPRX_AUX_D2_P
NC E63 LPDPRX_AUX_D3_P
NC D64 LPDPRX_AUX_D4_P
B59 LPDPRX_BYP_CLK_P
C59 LPDPRX_BYP_CLK_N
GND ON MLB; other on Dev
PP0V9_SOC_FIXED A57 LPDPRX_RCAL_P
R1001 300 1% 1/32W MF 01005-1 ROOM=SOC
AP_LPDPRX_RCAL_NEG B57 LPDPRX_RCAL_N
C1006 100PF 5% 16V NP0-C0G 01005 ROOM=SOC
NC D57 LPDPRX_EXT_C
#24401637:Unconnect LPDPRX_EXT_C
LPDP_TX0P B27 NC
LPDP_TX0N C27 NC
LPDP_TX1P A29 NC
LPDP_TX1N B29 NC
LPDP_TX2P B31 NC
LPDP_TX2N C31 NC
LPDP_TX3P A33 NC
LPDP_TX3N B33 NC
LPDP_AUX_P D33 NC
LPDP_AUX_N E33 NC
LPDP_CAL_DRV_OUT E35 NC
LPDP_CAL_VSS_EXT E31 NC
EDP_HPD BN3 NC
DP_WAKEUP AP2 NC
Dev ONLY
Reserved for PanelID[1:0] on ap_dev board
Reserved for PanelID[1:0] on ap_dev board
PP_VDD_MAIN
C1010 33PF 5% 16V NP0-C0G-CERM 01005 ROOM=SOC
C1011 33PF 5% 16V NP0-C0G-CERM 01005 ROOM=SOC
AC return path for LCM LPDP which is referenced to GND and VDD_MAIN

SOC - SERIAL INTERFACES

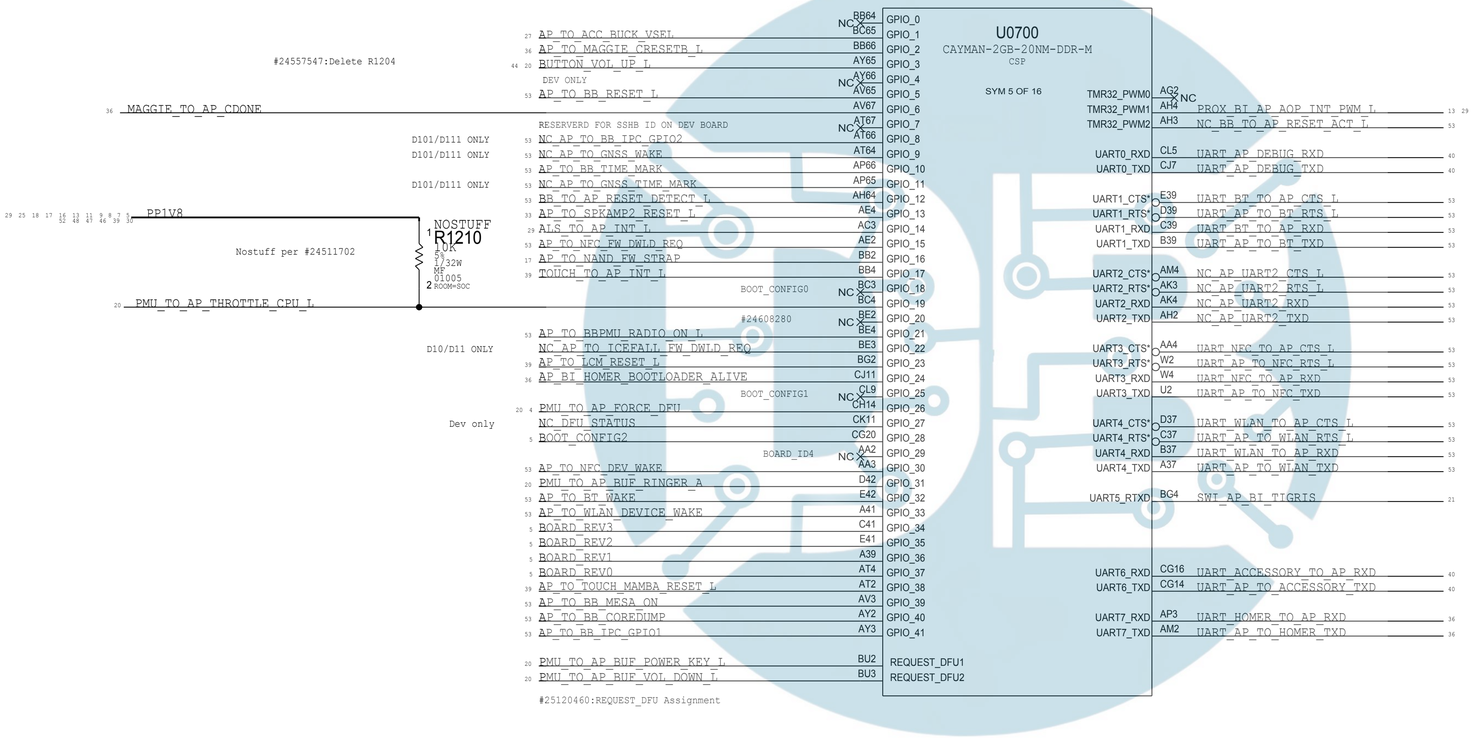


I2C5

See Radar#25316444 for Details



SOC - GPIO INTERFACES



SOC - AOP

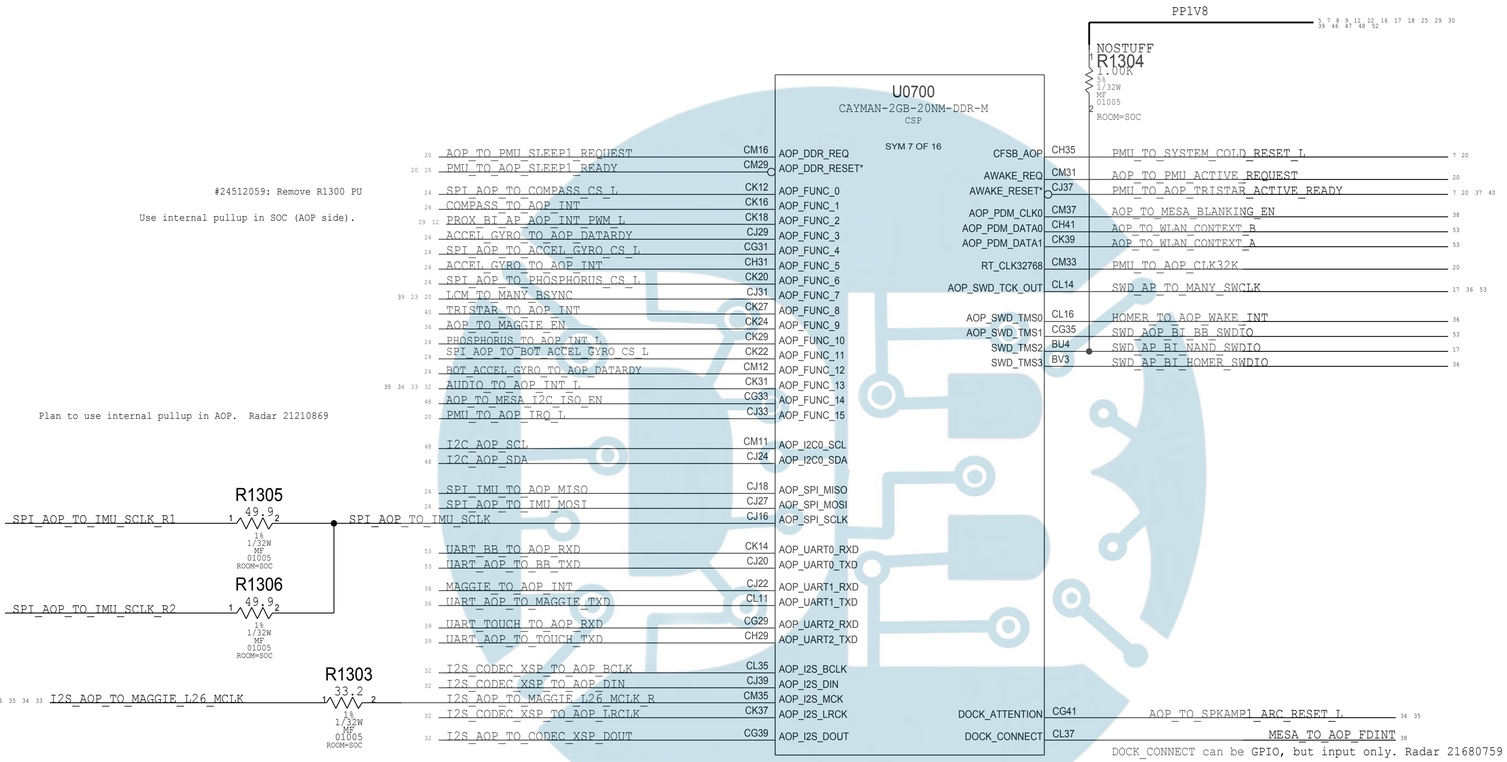
#24512059: Remove R1300 PU

Use internal pullup in SOC (AOP side).

Plan to use internal pullup in AOP. Radar 21210869

#25756894:North Carbon R1

#25756894:South Carbon R2



BB_SWDIO has pullup in Radio_MLB pages

DOCK_CONNECT can be GPIO, but input only. Radar 21680759

SOC - CPU, GPU & SOC RAILS

PP_CPU_VAR
1.06V @17.4A MAX
0.99V @tbd A MAX
0.625V @tbd A MAX

C1401 15UF 20% 6.3V X5R 0402-1
C1408 15UF 20% 6.3V X5R 0402-1
C1434 15UF 20% 6.3V X5R 0402-1
C1449 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC

C1404 7.5UF 20% 4V CERM 0402
C1411 7.5UF 20% 4V CERM 0402
C1417 7.5UF 20% 4V CERM 0402
C1422 4.3UF 20% 4V CERM 0402
C1427 4.3UF 20% 4V CERM 0402
C1430 4.3UF 20% 4V CERM 0402

C1405 4.3UF 20% 4V CERM 0402
C1412 4.3UF 20% 4V CERM 0402
C1418 1UF 20% 4V CERM 0402
C1423 1UF 20% 4V CERM 0402
C1428 1UF 20% 4V CERM 0402
C1431 1UF 20% 4V CERM 0402

C1406 0.47UF 20% 6.3V CERM 0402
C1413 0.47UF 20% 6.3V CERM 0402
C1419 0.47UF 20% 6.3V CERM 0402
C1424 0.47UF 20% 6.3V CERM 0402
C1460 7.5UF 20% 4V CERM 0402
C1461 7.5UF 20% 4V CERM 0402

OMIT
XW1402 SHORT-20L-0.05MM-SM
BUCK0_PP_CPU_FB
ROOM=SOC NO_XNET_CONNECTION

1.06V @1.0A MAX
0.80V @TBDA MAX

PP_CPU_SRAM_VAR
C1407 7.5UF 20% 4V CERM 0402
C1435 7.5UF 20% 4V CERM 0402
C1433 7.5UF 20% 4V CERM 0402
C1458 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC

1.03V @1.44A MAX
0.92V @1.50A MAX
0.80V @TBD A MAX

PP_GPU_SRAM_VAR
C1439 7.5UF 20% 4V CER 0402
C1437 7.5UF 20% 4V CERM 0402
C1459 1.0UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC

U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 8 OF 16

AD10 AD15 AD19 AD23 AF13 AF17 AJ23 AL21 AL8 AN10 AN19 AN23 AR13 AR17 AR21 AU10 AU15 AW13 AW17 AW21 BA10 BA23 BD21 BD8 BF10 BF23 BH13 BH17 BH21 BK10 BK15 AJ10 → VDD_CPU

AF8 AN15 AR8 AU19 AW8 BA15 BA19 BH8 → VDD_CPU_SRAM

AF43 AF47 AF51 P17 P21 P25 P30 P34 P38 P43 P47 P51 Y15 Y19 Y23 Y40 Y45 Y49 Y53 → VDD_GPU_SRAM

AB13 AB17 AB21 AB25 AB43 AB47 AB51 AB55 AD40 AD45 AD49 AD53 AF55 AJ40 AJ49 AJ53 J25 J30 J38 J43 J47 J51 L15 L19 L23 L28 L32 L36 L40 L45 L49 L53 P13 T15 T36 T40 T53 V13 V25 V34 V38 V51 V55 Y28 → VDD_GPU

PP1401 P2MM-NSM ROOM=SOC
PP_GPU_VAR

PP1402 P2MM-NSM ROOM=SOC
PP_CPU_VAR

XW1401 SHORT-20L-0.05MM-SM
OMIT ROOM=SOC NO_XNET_CONNECTION
BUCK1_PP_GPU_FB

1.03V @12.9A MAX
0.92V @10.7A MAX
0.80V @TBD A MAX
0.67V @TBD A MAX
PP_GPU_VAR

C1414 15UF 20% 6.3V X5R 0402-1
C1466 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1448 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC

C1402 4.3UF 20% 4V CERM 0402
C1409 4.3UF 20% 4V CERM 0402
C1452 4.3UF 20% 4V CERM 0402
C1454 4.3UF 20% 4V CERM 0402
C1416 7.5UF 20% 4V CERM 0402
C1421 7.5UF 20% 4V CERM 0402
C1426 7.5UF 20% 4V CERM 0402
C1432 7.5UF 20% 4V CERM 0402

C1410 1UF 20% 4V CERM 0402
C1415 1UF 20% 4V CERM 0402
C1420 1UF 20% 4V CERM 0402
C1425 0.47UF 20% 6.3V CERM 0402
C1429 0.47UF 20% 6.3V CERM 0402
C1456 0.47UF 20% 6.3V CERM 0402
C1457 0.47UF 20% 6.3V CERM 0402

VDD_CPU_SENSE BK23 → AP_VDD_CPU_SENSE → PP1408 P2MM-NSM ROOM=SOC
VSS_CPU_SENSE BK21 TP_AP_VSS_CPU_SENSE → PP1403 P2MM-NSM ROOM=SOC
VDD_GPU_SENSE AJ45 → AP_VDD_GPU_SENSE → PP1409 P2MM-NSM ROOM=SOC
VDD_SOC_SENSE AL47 TP_VDD_SOC_SENSE → PP1410 P2MM-NSM ROOM=SOC
VSS_SENSE AJ47 TP_VSS_SENSE → PP1411 P2MM-NSM ROOM=SOC

PP_SOC_VAR
0.80V @4.1A MAX
0.67V @TBDA MAX

C1436 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1444 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1403 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC

OMIT
XW1403 SHORT-20L-0.05MM-SM
BUCK2_PP_SOC_FB
ROOM=SOC NO_XNET_CONNECTION

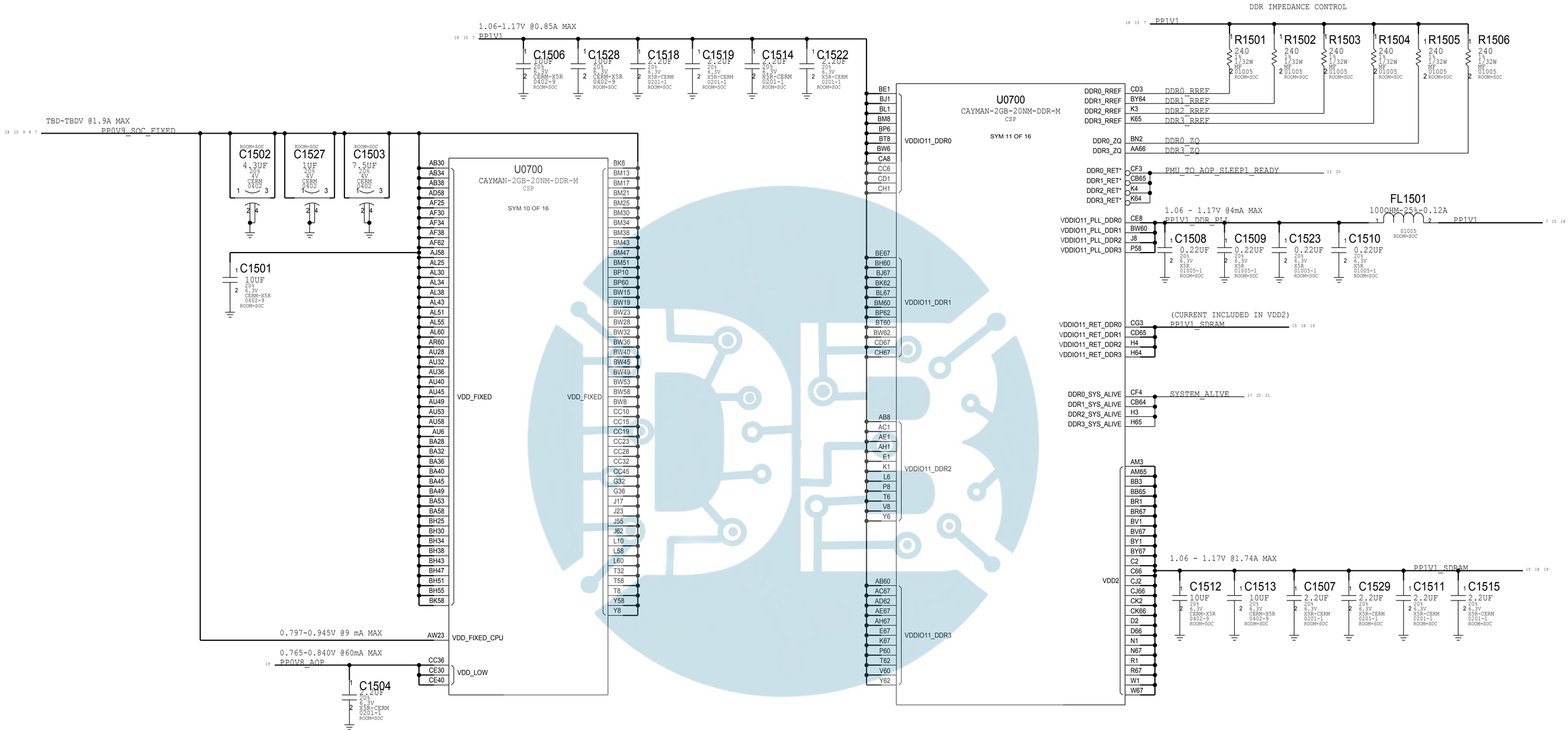
C1465 4.3UF 20% 4V CERM 0402
C1438 1UF 20% 4V CERM 0402
C1440 7.5UF 20% 4V CERM 0402
C1442 0.47UF 20% 6.3V CERM 0402

U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 9 OF 16

AD28 AD32 AF60 AJ28 AJ32 AJ36 AL6 AN28 AN32 AN36 AN40 AN45 AN49 AN53 AN58 AR25 AR30 AR34 AR38 AR43 AR47 AR51 AR55 AW30 AW34 AW38 AW43 AW47 AW51 AW55 AW60 BD25 BD30 BD34 BD38 BD43 BD47 BD51 BD55 BD6 BD60 BF28 BF32 BF36 BF45 BF49 BF53 BF58 BK28 BK32 BK36 BK40 → VDD_SOC

BK45 BK49 BK53 BM55 BP15 BP19 BP23 BP28 BP32 BP36 BP40 BP45 BP49 BP53 BP58 BT13 BT17 BT21 BT25 BT30 BT34 BT38 BT43 BT47 BT51 BT55 BW10 CA13 CA17 CA21 CA25 CA30 CA34 CA38 CA43 CA47 CE13 CE17 CE45 J13 J21 J34 P55 T10 T60 V30 Y10 Y36 Y60 BF40 J60 AW25 → VDD_SOC

SOC - POWER SUPPLIES



SOC - POWER SUPPLIES

U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 13 OF 16

U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 14 OF 16

U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 15 OF 16

U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 16 OF 16

U0700
CAYMAN-2GB-20NM-DDR-M
CSP
SYM 12 OF 16

1.70-1.95V @134mA MAX
PP1V8_SDRAM
C1615 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1605 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1608 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1612 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
VDD1

1.62-1.98V @43mA MAX
PP1V8
C1602 100UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1607 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1610 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1614 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
VDDIO18_GRP1
VDDIO18_GRP2
VDDIO18_GRP3
VDDIO18_GRP4

PP1V8_SDRAM
C1603 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1601 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
1.62-1.98V @10mA MAX
VDDIO18_GRP10

1.62-1.98V @2mA MAX
VDD18_TSADC0
VDD18_TSADC1
VDD18_TSADC2
VDD18_TSADC3
VDD18_TSADC4
VDD18_TSADC5

1.62-1.98V @1mA MAX
VDD18_FMON

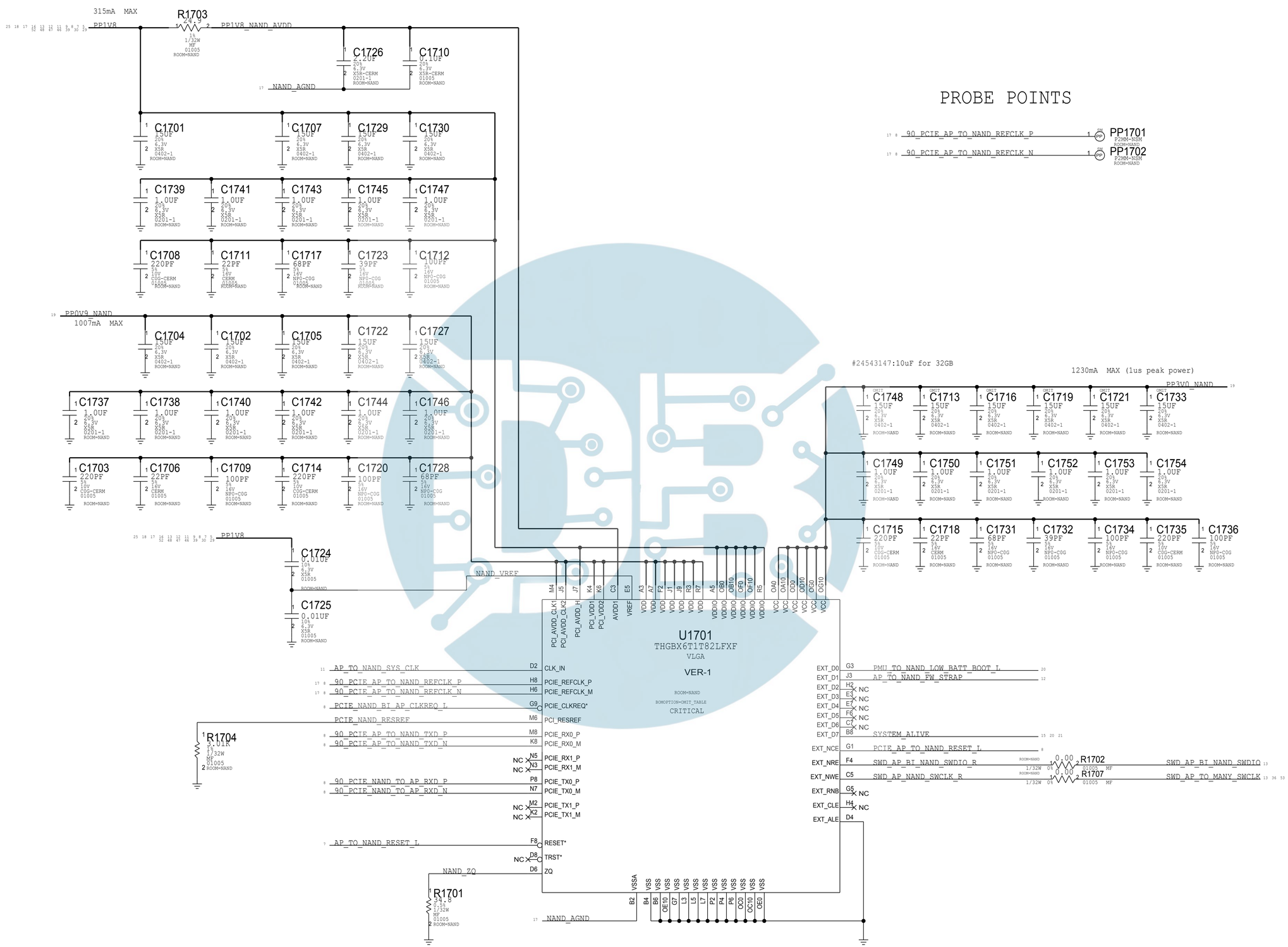
1.62-1.98V @1mA MAX
VDD18_LPOSC

TBD-TBDV @30mA MAX
PP1V2_REF
C1611 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
VDD12_CPU_UVD
VDD12_GPU_UVD
VDD12_SOC_UVD

VDD12_PLL_CPU
R1602 0.00 0% 1/32W MF 01005 ROOM=SOC
VDD12_PLL_CPU:1.14-1.26V @13mA MAX
PP1V2_PLL_CPU
C1606 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC

PP1V2_SOC
R1601 0.00 0% 1/32W MF 01005 ROOM=SOC
VDD12_PLL_SOC:1.14-1.26V @31mA MAX
PP1V2_PLL_SOC
VDD12_PLL_SOC
C1604 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SOC
C1609 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC
C1613 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC

VDD18_EFUSE1
VDD18_EFUSE2
CG7
G34
CKPLUS_WAIVE=PWRTERM2GND
CKPLUS_WAIVE=PWRTERM2GND


315mA MAX
PP1V8
R1703
24.9
1% 1/32W MF 01005 ROOM=NAND
PP1V8_NAND_AVDD
C1726 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=NAND
C1710 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
NAND_AGND
C1701 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1707 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1729 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1730 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1739 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1741 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1743 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1745 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1747 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1708 220PF 5% 10V C0G-CERM 01005 ROOM=NAND
C1711 22PF 5% 16V CERM 01005 ROOM=NAND
C1717 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1723 39PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1712 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
PP0V9_NAND
1007mA MAX
C1704 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1702 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1705 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1722 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1727 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1737 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1738 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1740 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1742 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1744 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1746 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1703 220PF 5% 10V C0G-CERM 01005 ROOM=NAND
C1706 22PF 5% 16V CERM 01005 ROOM=NAND
C1709 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1714 220PF 5% 10V C0G-CERM 01005 ROOM=NAND
C1720 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1728 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
PP1V8
C1724 0.01UF 10% 6.3V X5R 01005 ROOM=NAND
C1725 0.01UF 10% 6.3V X5R 01005 ROOM=NAND
NAND_VREF
R1704 3.01K 1% 1/32W MF 01005 ROOM=NAND
R1701 34.8 0.5% 1/32W MF 01005 ROOM=NAND
U1701
THGBX6T1T82LFXF
VLGA
VER-1
ROOM=NAND
BOMOPTION=OMIT_TABLE
CRITICAL
PCIE_CLKREQ*
PCI_RESREF
PCIE_REFCLK_P
PCIE_REFCLK_M
PCIE_RX0_P
PCIE_RX0_M
PCIE_RX1_P
PCIE_RX1_M
PCIE_TX0_P
PCIE_TX0_M
PCIE_TX1_P
PCIE_TX1_M
RESET*
TRST*
ZQ
AP_TO_NAND_SYS_CLK
90_PCIE_AP_TO_NAND_REFCLK_P
90_PCIE_AP_TO_NAND_REFCLK_N
PCIE_NAND_BI_AP_CLKREQ_L
90_PCIE_AP_TO_NAND_TXD_P
90_PCIE_AP_TO_NAND_TXD_N
90_PCIE_NAND_TO_AP_RXD_P
90_PCIE_NAND_TO_AP_RXD_N
AP_TO_NAND_RESET_L
NAND_AGND
PROBE POINTS
90_PCIE_AP_TO_NAND_REFCLK_P
PP1701 F2MM=NSM ROOM=NAND
90_PCIE_AP_TO_NAND_REFCLK_N
PP1702 F2MM=NSM ROOM=NAND
#24543147:10uF for 32GB
1230mA MAX (1us peak power)
PP3V0_NAND
C1748 1.5UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1713 1.5UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1716 1.5UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1719 1.5UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1721 1.5UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1733 1.5UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1749 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1750 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1751 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1752 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1753 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1754 1.0UF 20% 6.3V X5R 0201-1 ROOM=NAND
C1715 220PF 5% 10V C0G-CERM 01005 ROOM=NAND
C1718 22PF 5% 16V CERM 01005 ROOM=NAND
C1731 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1732 39PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1734 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1735 220PF 5% 10V C0G-CERM 01005 ROOM=NAND
C1736 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
EXT_D0 PMU_TO_NAND_LOW_BATT_BOOT_L
EXT_D1 AP_TO_NAND_FW_STRAP
EXT_D2 NC
EXT_D3 NC
EXT_D4 NC
EXT_D5 NC
EXT_D6 NC
EXT_D7 SYSTEM_ALIVE
EXT_NCE PCIE_AP_TO_NAND_RESET_L
EXT_NRE SWD_AP_BI_NAND_SWDIO_R
EXT_NWE SWD_AP_NAND_SWCLK_R
EXT_RNB NC
EXT_CLE NC
EXT_ALE
R1702 0.0 1/32W MF 01005 ROOM=NAND
SWD_AP_BI_NAND_SWDIO
R1707 0.0 1/32W MF 01005 ROOM=NAND
SWD_AP_TO_MANY_SWCLK

Voltages per Cayman Power Spec, Sec. 2.2, rev 0.9.2, #24557869

U1801
D2333A1
WLCSP
SYM 2 OF 4
ROOM=PMU

19 VDD_MAIN_SNS → M8 VDD_MAIN_SNS
N7 VDD_MAIN
H6 VDD_MAIN_E
E11 VDD_MAIN_N
R13 VDD_MAIN_SW
H14 VDD_MAIN_W
H13 VDD_MAIN_W

PP_VDD_MAIN

C1846 10UF 20% 6.3V CERM-X5R 0402-9
C1850 10UF 20% 6.3V CERM-X5R 0402-9
C1853 10UF 20% 6.3V CERM-X5R 0402-9
C1857 10UF 20% 6.3V CERM-X5R 0402-9
C1875 2.2UF 20% 6.3V X5R-CERM 0201-1
C1847 2.2UF 20% 6.3V X5R-CERM 0201-1
C1851 2.2UF 20% 6.3V X5R-CERM 0201-1
C1854 2.2UF 20% 6.3V X5R-CERM 0201-1
C1858 2.2UF 20% 6.3V X5R-CERM 0201-1
C1876 2.2UF 20% 6.3V X5R-CERM 0201-1
C1848 2.2UF 20% 6.3V X5R-CERM 0201-1
C1852 2.2UF 20% 6.3V X5R-CERM 0201-1
C1855 2.2UF 20% 6.3V X5R-CERM 0201-1
C1859 2.2UF 20% 6.3V X5R-CERM 0201-1
C1877 2.2UF 20% 6.3V X5R-CERM 0201-1
C1849 2.2UF 20% 6.3V X5R-CERM 0201-1
C1856 2.2UF 20% 6.3V X5R-CERM 0201-1
(all ROOM=PMU)

BAT/USB

VDD_BUCK0_01: A5 B5 C5 D5
VDD_BUCK0_23: A9 B9 C9 D9
VDD_BUCK1_01: A17 B17 C17 D17
VDD_BUCK1_23: A13 B13 C13 D13
VDD_BUCK2: H1 H2 H3
VDD_BUCK3: T2 T3
VDD_BUCK4: M1 M2 M3
VDD_BUCK5: B1 C1 D1
VDD_BUCK6: K18 K19
VDD_BUCK7: U6 V6
VDD_BUCK8: F18 F19
VDD_BUCK9: L18 L19

BUCK INPUT

BUCK0 — 13.4A MAX

BUCK0_LX0: B4 C4 D4 A4
BUCK0_LX1: A6 B6 C6 D6
BUCK0_LX2: A8 B8 C8 D8
BUCK0_LX3: A10 B10 C10 D10

L1806 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM ROOM=PMU
L1807 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM ROOM=PMU
L1808 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM ROOM=PMU
L1809 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM ROOM=PMU
(BUCK0_LX0 NO_XNET_CONNECTION=1; CRITICAL)

BUCK0_FB: F10 BUCK0_PP_CPU_FB (14)

PP_CPU_VAR (14) 0.625V - 1.06V

C1818 C1825 C1831 C1837 C1842 C1844 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1819 C1826 C1832 C1838 C1843 C1845 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1872 220PF 5% 10V C0G-CERM 01005 ROOM=PMU

BUCK1 — 13.4A MAX

BUCK1_LX0: B18 C18 D18 A18
BUCK1_LX1: A16 B16 C16 D16
BUCK1_LX2: A14 B14 C14 D14
BUCK1_LX3: A12 B12 C12 D12

L1810 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM ROOM=PMU
L1811 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM ROOM=PMU
L1812 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM ROOM=PMU
L1813 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM ROOM=PMU
(BUCK1_LX0 NO_XNET_CONNECTION=1; CRITICAL)

BUCK1_FB: F12 BUCK1_PP_GPU_FB (14)

PP_GPU_VAR (14) 0.67V - 0.92V
1.03V for overdrive only

C1813 C1820 C1827 C1833 C1839 C1865 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1814 C1821 C1828 C1834 C1866 C1873 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1873: 220PF 5% 10V C0G-CERM 01005 ROOM=PMU

BUCK2 — 4.7A MAX

BUCK2_LX0: G1 G2 G3
BUCK2_LX1: J1 J2 J3

L1814 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM ROOM=PMU
L1815 0.47UH-20%-3.8A-0.048OHM PIQA20121T-SM ROOM=PMU
(BUCK2_LX0 NO_XNET_CONNECTION=1; CRITICAL)

BUCK2_FB: J5 BUCK2_PP_SOC_FB (14)

PP_SOC_VAR (14) 0.67V/0.80V

C1822 C1829 C1835 C1841 C1864 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1871 220PF 5% 10V C0G-CERM 01005 ROOM=PMU

BUCK3 — 1.7A MAX (pending vendor qual)

BUCK3_LX0: R2 R3 R1
BUCK3_FB: R7
VBUCK3_SW: U2 V2

L1816 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM ROOM=PMU
(BUCK3_LX0 NO_XNET_CONNECTION=1; CRITICAL)

XW1804 OMIT SHORT-20L-0.05MM-SM ROOM=SOC
BUCK3_FB NO_XNET_CONNECTION=1

PP1V8_SDRAM (16 20 21 32 36 37 40 41 46 47 48 53)

C1816 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1823 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1860 220PF 5% 10V C0G-CERM 01005 ROOM=PMU

BUCK4 — 4.7A MAX

BUCK4_LX0: N1 N2 N3
BUCK4_LX1: L1 L2 L3
BUCK4_FB: K5
VBUCK4_SW: U5 V5

L1817 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM ROOM=PMU
(BUCK4_LX0 NO_XNET_CONNECTION=1; CRITICAL)

L1818 0.47UH-20%-3.8A-0.048OHM PIQA20121T-SM ROOM=PMU
(BUCK4_LX1 NO_XNET_CONNECTION=1; CRITICAL)

XW1805 OMIT SHORT-20L-0.05MM-SM ROOM=SOC
BUCK4_FB NO_XNET_CONNECTION=1

PP1V1_SDRAM (15 19)

C1830 C1836 C1802 C1874 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1861 220PF 5% 10V C0G-CERM 01005 ROOM=PMU

BUCK5 — 3.2A MAX

PP0V9_SOC_FIXED (15 10 9 8 7)
C1867 220PF 5% 10V C0G-CERM 01005 ROOM=PMU
C1840 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C1801 C1803 C1807 15UF 20% 6.3V X5R 0402-1 ROOM=PMU

D10/D101:#24681501,TY ONLY, D11/D11: Both Vendor
L1803 CRITICAL 1.0UH-3.6A-0.060HM MEKK2016T-SM ROOM=PMU NO_XNET_CONNECTION=1
BUCK5_LX0: B2 C2 D2 A2
XW1802 OMIT SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION=1
BUCK5_FB: F5 BUCK5_FB

BUCK6 — 1.5A MAX

PP1V25_BUCK (19)
C1811 220PF 5% 10V C0G-CERM 01005 ROOM=PMU
C1804 C1808 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
L1804 CRITICAL 1UH-20%-2.1A-0.12OHM PIQA20121T-SM ROOM=PMU
BUCK6_LX0: J18 J19
XW1807 OMIT SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION=1
BUCK6_FB: H16 BUCK6_FB

BUCK7 — 1.5A MAX

PP_CPU_SRAM_VAR (14)
0.80V - 1.06V
C1868 220PF 5% 10V C0G-CERM 01005 ROOM=PMU
C1805 C1809 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
L1805 CRITICAL 1.0UH-20%-2.25A-0.086OHM MCFE2016T-SM ROOM=PMU
BUCK7_LX0: U7 V7
XW1803 OMIT SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION=1
BUCK7_FB: R8 BUCK7_FB

BUCK8 — 1.5A MAX

PP_GPU_SRAM_VAR (14)
0.80V - 0.92V
C1869 220PF 5% 10V C0G-CERM 01005 ROOM=PMU
C1806 C1810 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
L1801 CRITICAL 1UH-20%-2.1A-0.12OHM PIQA20121T-SM ROOM=PMU
BUCK8_LX0: G18 G19
XW1801 OMIT SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION=1
BUCK8_FB: H15 BUCK8_FB

BUCK9 — 0.75A MAX

PP2V8_UT_AF_VAR (30 25)
C1870 220PF 5% 10V C0G-CERM 01005 ROOM=PMU
C1862 C1863 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
L1802 CRITICAL 1.0UH-20%-1.5A-0.161OHM 0603
BUCK9_LX0: M18 M19
XW1806 OMIT SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION=1
BUCK9_FB: P16 BUCK9_FB

SWITCH OUTPUTS

BUCK3_SW1: T1 U1 → PP1V8 (4 7 8 9 11 12 13 16 17 25 29 30 39 46 47 48 52)
BUCK3_SW2: U3 → PP1V8_TOUCH (38 39 47)
BUCK3_SW3: V3 → PP1V8_MAGGIE_TMU (24 36)
BUCK4_SW1: U4 V4 → PP1V1 (7 15)

ADELYN LDO SPECS

LDO#	ADJ.RANGE, LOW	ADJ.RANGE, HI	ACCURACY	MAX.CURRENT
LDO1 (Ca)	1.2-2.475V	2.4-3.675V	+/-1.4%	50mA
LDO2 (Ca)	1.2-2.475V	2.4-3.675V	+/-2.5%	50mA
LDO3 (Ca)	1.2-2.475V	2.4-3.675V	+/-2.5%	50mA
LDO4 (D)	0.7-1.2V		+/-2.5%	60mA
LDO5 (F)	2.5-3.6V(tbc)		+/-75mV	1000mA
LDO6 (Cb)	1.2-2.475V	2.4-3.675V	+/-2.5%	250mA (500/100mA in bypass)
LDO7 (Cb)	1.2-2.475V	2.4-3.675V	+/-30mV	250mA
LDO8 (Cb)	1.2-2.475V	2.4-3.675V	+/-30mV	250mA
LDO9 (Cb)	1.2-2.475V	2.4-3.675V	+/-25mV	250mA
LDO10 (Ga)	0.7-1.2V		+/-4.5%	1150mA

LDO#	ADJ.RANGE, LOW	ADJ.RANGE, HI	ACCURACY	MAX.CURRENT
LDO11 (Cb)	1.2-2.475V	2.4-3.675V	+/-30mV	250mA
LDO12 (E)	1.8V		+/-5%	10mA
LDO13 (Cb)	1.2-2.475V	2.4-3.675V	+/-30mV	250mA
LDO14 (Gb)	0.7-1.4V		+/-3.0%	400mA
LDO15 (Ca)	1.2-2.475V	2.4-3.675V	+/-2.5%	50mA
LDO16 (Cb)	1.2-2.475V	2.4-3.675V	+/-30mV	250mA
LDO17 (Ca)	1.2-2.475V	2.4-3.675V	+/-2.5%	50mA
LDO18 (Gb)	0.7-1.4V		+/-3.0%	400mA
LDO19 (Gb)	0.7-1.4V		+/-3.0%	400mA
LDO_RTC	2.5V		+/-2.0%	10mA
BUF_1V2	1.2V		+/-5.0%	10mA

PP_VDD_MAIN
OMIT XW1901 SHORT-VIA-0.05MM-SM VDD_MAIN_SNS
OMIT XW1902 SHORT-20L-0.05MM-SM PMU_PRE_UVLO_DET
C1901 15UF 20% 6.3V X5R 0402-1
C1910 10UF 20% 6.3V CERM-X5R 0402-9
C1914 10UF 20% 6.3V CERM-X5R 0402-9
C1911 10UF 20% 6.3V CERM-X5R 0402-9
C1907 10UF 20% 6.3V CERM-X5R 0402-9
C1915 15UF 20% 6.3V X5R 0402-1
C1912 15UF 20% 6.3V X5R 0402-1
C1908 2.2UF 20% 6.3V X5R-CERM 0201-1
C1913 2.2UF 20% 6.3V X5R-CERM 0201-1
PP1V1_SDRAM
PP1V25_BUCK

U1801 D2333A1 WLCSP SYM 1 OF 4 (LDO INPUT / LDO)

R12	VDD_LDO1
V11	VDD_LDO2_15
R10	VDD_LDO3_17
R16	VDD_LDO4
V9	VDD_LDO5
V10	
R14	VDD_LDO6_BYP
P19	VDD_LDO7_8
R19	VDD_LDO9
R9	VDD_LDO10
V13	VDD_LDO11_13
V16	VDD_LDO14
T19	VDD_LDO16
V17	VDD_LDO18
V18	VDD_LDO19
V19	
G15	VPP_OTP
J6	TP_DET

VLDO1	T12	PP3V3_USB	LDO1
VLDO2	U11	PP1V8_VA	LDO2
VLDO3	T10	PP3V0_ALS_APS_CONVOY	LDO3
VLDO4	T16	PP0V8_AOP	LDO4
VLDO5_0	U9	PP3V0_NAND	LDO5
VLDO5_1	U10		
VLDO6	T14	PP_ACC_VAR	LDO6
VBYPASS	R15		
VLDO7	T17	PP3V0_TRISTAR_ANT_PROX	LDO7
VLDO8	P18	PP2V9_NH_AVDD	LDO8
VLDO9	R18	PP1V8_HAWKING	LDO9
VLDO9_FB	P17		
VLDO10	T9	PP0V9_NAND	LDO10
VLDO11	U13	NC	LDO11
VLDO12	P7	PP1V8_ALWAYS	LDO12
VLDO13	U14	PP3V0_MESA	LDO13
VLDO14	U16	PP1V2_SOC	LDO14
VLDO15	U12	PP1V8_MESA	LDO15
VLDO16	T18	#24989262 R1901 1/20W 1% 0.00 0201 MF NOSTUFF	LDO16
VLDO17	T11	PP_LDO17	LDO17
VLDO18	U17	PP1V2_UT_DVDD	LDO18
VLDO19	U18	PP1V2_NH_NV_DVDD	LDO19
VBUF_1V2	P8	PP1V2_REF	VBUF_1V2
VPUMP	R5		

New for ADELYN

C1918 2.2UF 20% 6.3V X5R-CERM 0201-1
C1933 1.0UF 20% 6.3V X5R 0201-1
C1923 2.2UF 20% 6.3V X5R-CERM 0201-1
C1926 2.2UF 20% 6.3V X5R-CERM 0201-1
C1935 1.0UF 20% 6.3V X5R 0201-1
C1930 2.2UF 20% 6.3V X5R-CERM 0201-1
C1932 0.22UF 20% 6.3V X5R 01005-1
C1916 2.2UF 20% 6.3V X5R-CERM 0201-1
C1921 2.2UF 20% 6.3V X5R-CERM 0201-1
C1922 2.2UF 20% 6.3V X5R-CERM 0201-1
C1925 1.0UF 20% 6.3V X5R 0201-1
C1927 2.2UF 20% 6.3V X5R-CERM 0201-1
C1904 2.2UF 20% 6.3V X5R-CERM 0201-1
C1919 2.2UF 20% 6.3V X5R-CERM 0201-1
PMU_VPUMP
C1902 47NF 20% 6.3V X5R-CERM 01005

VPUMP: 10nF min. @4.6V

#24989262:OTP-AO LDO17 default off,50mA Iout_max

U1801 D2333A1 WLCSP SYM 4 OF 4

A1			G17
A11			G4
A15			H17
H8			H18
A19			H19
P13			H4
A3			J17
P14			J4
A7			J8
B11			K1
B15			K17
B19			K2
B3			K3
B7			K4
C11			K8
C15			L17
C19			L4
C3			L8
C7			M17
D11			M4
D15			N17
D19			N18
D3			N19
D7	VSS	VSS	N4
E1			P1
E10			P2
E11			P3
E12			P4
E13			P15
E14			R17
E15			R4
E16			T5
E17			T15
E18			T4
E19			T6
E2			T7
E3			T8
E4			U15
E5			T13
E6			U8
E7			V1
E8			V12
E9			V19
F1			V8
F17			
F2			
F3			
F4			

PP_VDD_MAIN
C1905 33PF 5% 16V NPO-COG-CERM 01005
C1909 220PF 5% 10V C0G-CERM 01005
PMU_VSS_RTC
U15 = PMU XTAL GND

BUTTON PULL-UP RESISTORS

PP1V8_SDRAM
R2008 100K 5% 1/32W MF 01005 ROOM=PMU
BUTTON_RINGER_A

PP1V8_ALWAYS
R2007 220K 5% 1/32W MF 01005 ROOM=PMU
BUTTON_POWER_KEY_L

PP1V8_SDRAM
R2015 220K 5% 1/32W MF 01005 ROOM=PMU
BUTTON_VOL_DOWN_L

NOTE:VDROOP_DET filtering is now inside Adelyn

Button for two-finger reset: 20711463 and 21196187

PP1V8_SDRAM
R2012 10K 5% 1/32W MF 01005 ROOM=PMU
NO_XNET_CONNECTION

PP1V8_ALWAYS
R2006 100K 5% 1/32W MF 01005 ROOM=PMU
R2005 100K 5% 1/32W MF 01005 ROOM=PMU

C2001 1000PF 10% 10V X5R 01005 ROOM=PMU PLACE_NEAR=U1801:2mm

PP2001 P2MM-NSM ROOM=SOC
PP2002 P2MM-NSM ROOM=SOC
PP2003 P2MM-NSM ROOM=PMU

U1801 D2333A1 WLCSP SYM 3 OF 4

	P9	RESET_IN1	RESETS	
AP_TO_PMU_WDOG_RESET	P10	RESET_IN2		
TRISTAR_TO_PMU_HOST_RESET	P11	RESET_IN3		
AP_TO_PMU_SOCHOT_L	M5	RESET*		
PMU_TO_SYSTEM_COLD_RESET_L	P12	SHDN		
	R11	SLEEP1_REQ		
Active high with int 200k PD	L11	SLEEP1_RDY		
AOP_TO_PMU_SLEEP1_REQUEST	L12	ACTIVE_REQ		
PMU_TO_AOP_SLEEP1_READY	J12	ACTIVE_RDY		
AOP_TO_PMU_ACTIVE_REQUEST	M9	SLEEP_32K		
PMU_TO_AOP_TRISTAR_ACTIVE_READY	M10	OUT_32K		
PMU_TO_AOP_CLK32K	H5	SYS_ALIVE		
SYSTEM_ALIVE	L13	FORCE_SYNC		
LCM_TO_MANY_BSYNC (HIGH=FORCE_PWM_MODE)	L10	CRASH*		
	G5	IRQ*		
PMU_TO_AOP_IRQ_L	N13	SCL		
=I2C_PMU_SCL	M13	SDA		
=I2C_PMU_SDA	N6	SCLK	PMGR	
I2C_PMU_SDA_R	N5	MOSI		
SPI_PMGR_TO_PMU_SCLK	P5	MISO		
SPI_PMGR_TO_PMU_MOSI	J14	AMUX_A0	ADC	
SPI_PMU_TO_PMGR_MISO	J15	AMUX_A1		
AP_TO_PMU_AMUX_OUT	J16	AMUX_A2		
PMU_ADC_IN	K16	AMUX_A3	AMUX BUTTONS	
BUTTON_VOL_UP_L	K15	AMUX_A4		
	K14	AMUX_A5		
LCM_TO_CHESTNUT_PWR_EN	J13	AMUX_A6		
TRISTAR_TO_PMU_USB_BRICK_ID	K13	AMUX_A7		
PP1V2_MAGGIE	K12	AMUX_AY		
PMU_AMUX_AY	L14	AMUX_B0		
BBPMU_TO_PMU_AMUX1	L15	AMUX_B1		
BBPMU_TO_PMU_AMUX2	L16	AMUX_B2		
	M16	AMUX_B3		
ACC_BUCK_TO_PMU_AMUX	M15	AMUX_B4		
PMUGPIO_TO_WLAN_CLK32K	M14	AMUX_B5		
CHESTNUT_TO_PMU_ADCMUX	N16	AMUX_B6		
AP_TO_PMU_TEST_CLKOUT	N15	AMUX_B7		
BBPMU_TO_PMU_AMUX3	N14	AMUX_BY		
PMU_AMUX_BY	R6	TDEV1	NTC GPIO	
FOREHEAD_NTC	M6	TDEV2		
REAR_CAMERA_NTC	P6	TDEV3		
RADIO_PA_NTC	L5	TDEV4		
AP_NTC	L6	TDEV5		
	G16	TCAL		
PMU_TCAL	V14	XTAL1	XTAL	
PMU_XTAL1	V15	XTAL2		
PMU_XTAL2	N9	VDD_RTC		
PMU_VDD_RTC				

IREF	K6	PMU_IREF
VREF	J7	PMU_VREF
PRE_UVLO*	N10	PMU_TO_AP_PRE_UVLO_L
VDROOP0*	G6	PMU_TO_AP_THROTTLE_CPU_L
VDROOP1*	G7	PMU_TO_AP_THROTTLE_GPU_L
VDROOP0_DET	F6	AP_VDD_CPU_SENSE
VDROOP1_DET	F7	AP_VDD_GPU_SENSE
PRE_UVLO_DET	N8	PMU_PRE_UVLO_DET
IBAT	L7	NC
VBAT	M7	NC
BRICK_ID	H7	TRISTAR_TO_PMU_USB_BRICK_ID
ADC_IN	K7	PMU_ADC_IN
BUTTON1	M12	BUTTON_VOL_DOWN_L
BUTTON2	N12	BUTTON_POWER_KEY_L
BUTTON3	M11	BUTTON_RINGER_A
BUTTON4	N13	NC Reserved for MENU key on dev board
BUTTONO1	H11	PMU_TO_AP_BUF_VOL_DOWN_L
BUTTONO2	J11	PMU_TO_AP_BUF_POWER_KEY_L
BUTTONO3	K11	PMU_TO_AP_BUF_RINGER_A
GPIO1	F16	TIGRIS_TO_PMU_INT_L
GPIO2	F15	BB_TO_PMU_PCIE_HOST_WAKE_L
GPIO3	G14	PMU_TO_BBPMU_RESET_R_L
GPIO4	F14	WLAN_TO_PMU_HOST_WAKE
GPIO5	F13	NFC_TO_PMU_HOST_WAKE
GPIO6	G13	PMU_TO_NAND_LOW_BATT_BOOT_L
GPIO7	G12	NC_PMU_TO_GNSS_EN
GPIO8	H12	PMUGPIO_TO_WLAN_CLK32K
GPIO9	G11	PMU_TO_BT_REG_ON
GPIO10	G10	NC_GNSS_TO_PMU_HOST_WAKE
GPIO11	F9	PMU_TO_WLAN_REG_ON
GPIO12	G9	BT_TO_PMU_HOST_WAKE
GPIO13	F8	PMU_TO_CODEC_DIGLDO_PULLDN
GPIO14	G8	PMU_TO_ACC_BUCK_SW_EN
GPIO15	H9	PMU_TO_BB_USB_VBUS_DETECT
GPIO16	H10	PMU_TO_NFC_EN
GPIO17	J9	PMU_TO_AP_FORCE_DFU_R
GPIO18	J10	PMU_TO_BOOST_EN
GPIO19	K9	PMU_TO_LCM_PANICB
GPIO20	K10	PMU_TO_HOMER_RESET_L
GPIO21	L9	=I2C_CHESTNUT_SCL

GPIO21 = I2C SCL is for Chestnut dark current mitigation

C2006 0.22UF 20% 6.3V X5R 0201 ROOM=PMU
R2011 200K 1% 1/20W MF 201 ROOM=PMU

R2000 1.00K 5% 1/32W MF 01005 ROOM=PMU
PMU_TO_BBPMU_RESET_L

#24511807: Stuff for Carrier
R2009 0.0D 5% 1/32W MF 01005
PMU_TO_AP_FORCE_DFU
RS = Sequencer controllable
RS = requires sequencer

R2020 33.2 1% 1/32W MF 01005 ROOM=PMU
#24825674: Add R2020 to meet timing spec

FOREHEAD NTC
C2007 100PF 5% 16V NP0-C0G 01005 ROOM=PMU
R2001 10KOHM-1% 01005 ROOM=PMU
FOREHEAD_NTC_RETURN

REAR CAMERA NTC
C2008 100PF 5% 16V NP0-C0G 01005 ROOM=PMU
R2002 10KOHM-1% 01005 ROOM=PMU
RCAM_NTC_RETURN

RADIO PA NTC
C2009 100PF 5% 16V NP0-C0G 01005 ROOM=PMU
R2003 10KOHM-1% 01005 ROOM=PMU
PA_NTC_RETURN

AP NTC
C2010 100PF 5% 16V NP0-C0G 01005 ROOM=PMU
R2004 10KOHM-1% 01005 ROOM=PMU
AP_NTC_RETURN

XW2002 OMIT SHORT-20L-0.05MM-SM ROOM=SOC
XW2003 OMIT SHORT-20L-0.05MM-SM ROOM=SOC
XW2004 OMIT SHORT-20L-0.05MM-SM ROOM=SOC
XW2005 OMIT SHORT-20L-0.05MM-SM ROOM=SOC

C2011 470PF 5% 16V NP0-C0G 01005 ROOM=PMU
R2010 3.92K 0.1% 1/20W MF 0201 ROOM=PMU

C2013 1000PF 10% 10V X5R 01005 ROOM=PMU PLACE_NEAR=U1801:2mm

C2002 0.22UF 20% 6.3V X5R 0201 ROOM=PMU

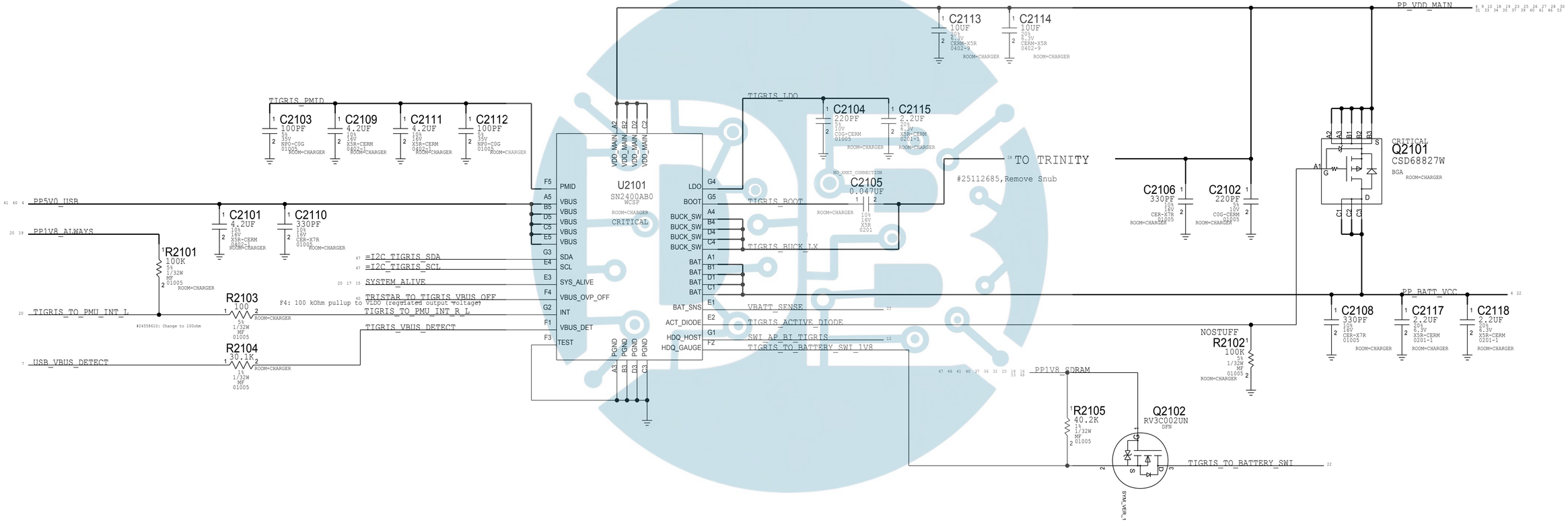
CRITICAL
Y2001 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM ROOM=PMU

C2003 22PF 5% 16V CERM 01005 ROOM=PMU
C2004 22PF 5% 16V CERM 01005 ROOM=PMU

XW2001 SHORT-20L-0.05MM-SM ROOM=PMU OMIT

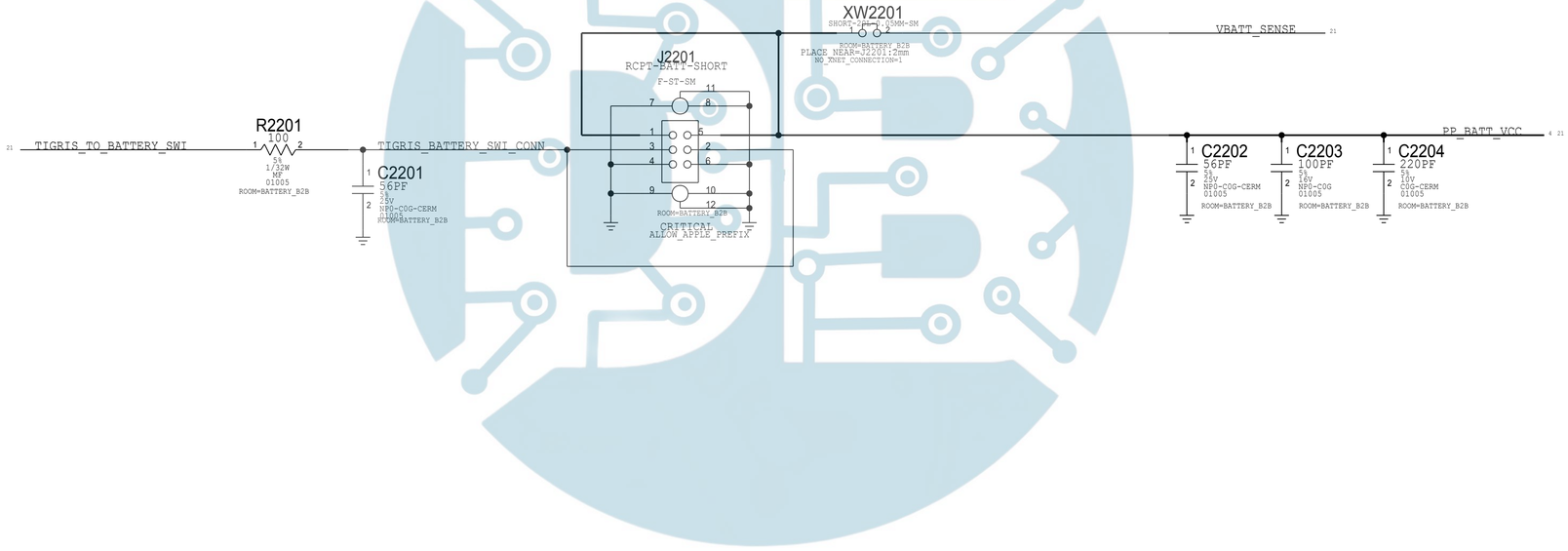
NOTE:100PF CAPS ARE THE SAMPLING CAPS FOR PMU ADC

TIGRIS CHARGER

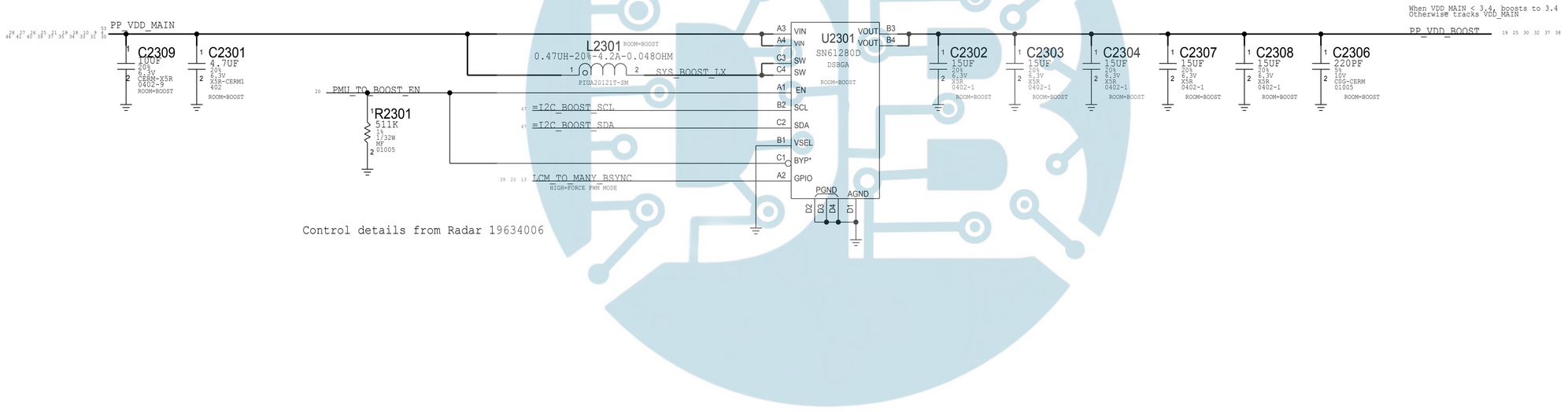


BATTERY CONNECTOR

THIS ONE ON MLB ---> 516S00172 (matches d10 mlb MCO rev 27)



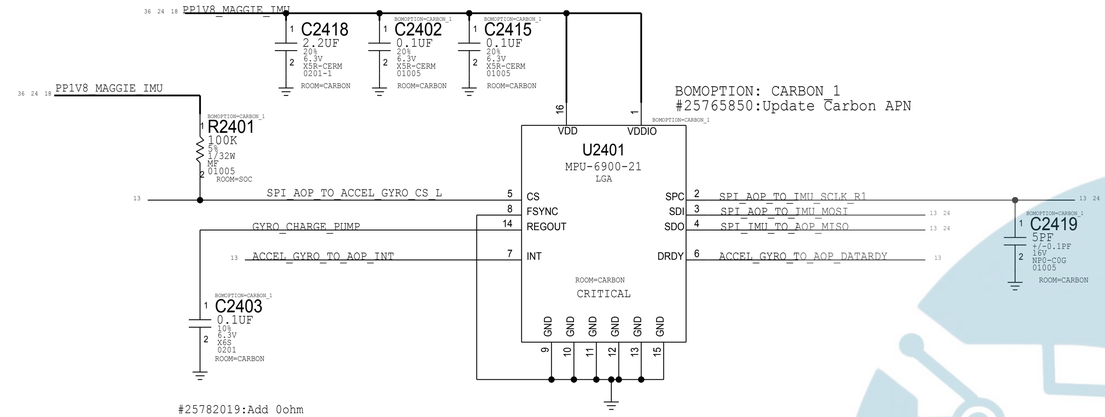
BOOST



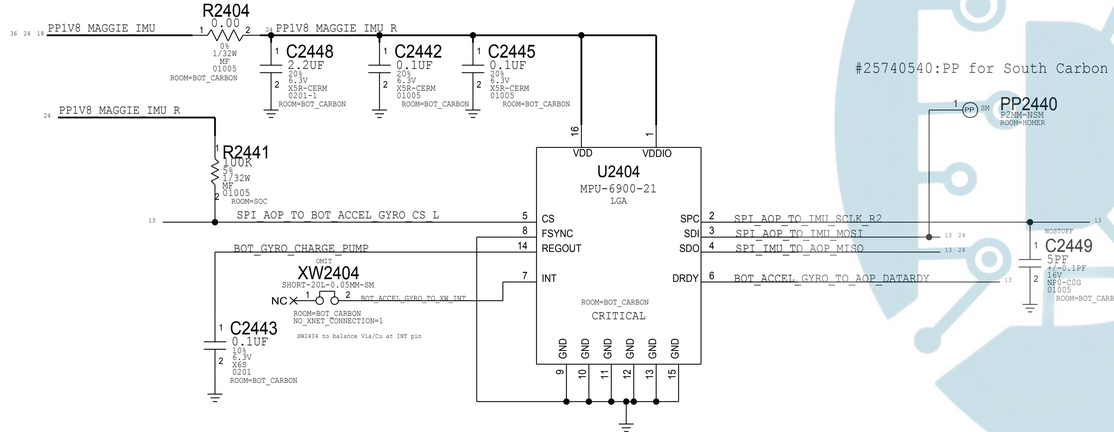
Control details from Radar 19634006

CARBON - ACCEL & GYRO

INVENSENSE, MPU-6800: C2403=0.1UF

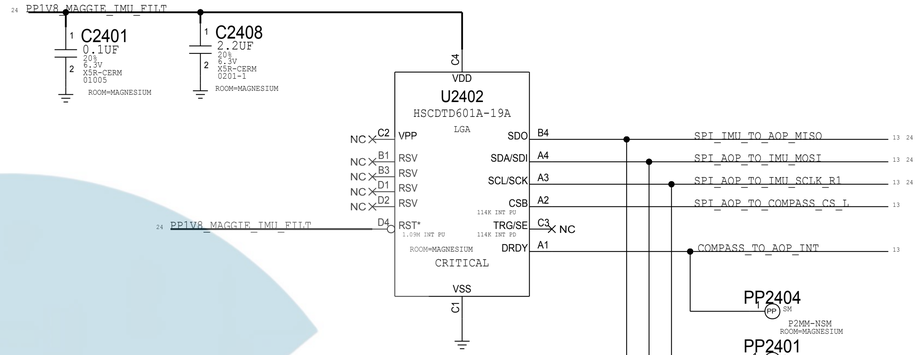


#25782019:Add 0ohm



#25740540:PP for South Carbon MOSI

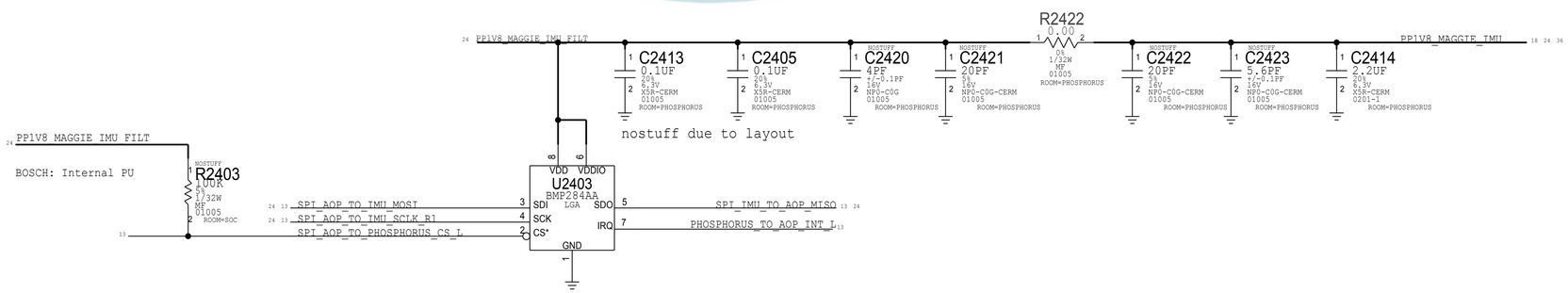
MAGNESIUM - COMPASS



PHOSPHORUS

#24593845

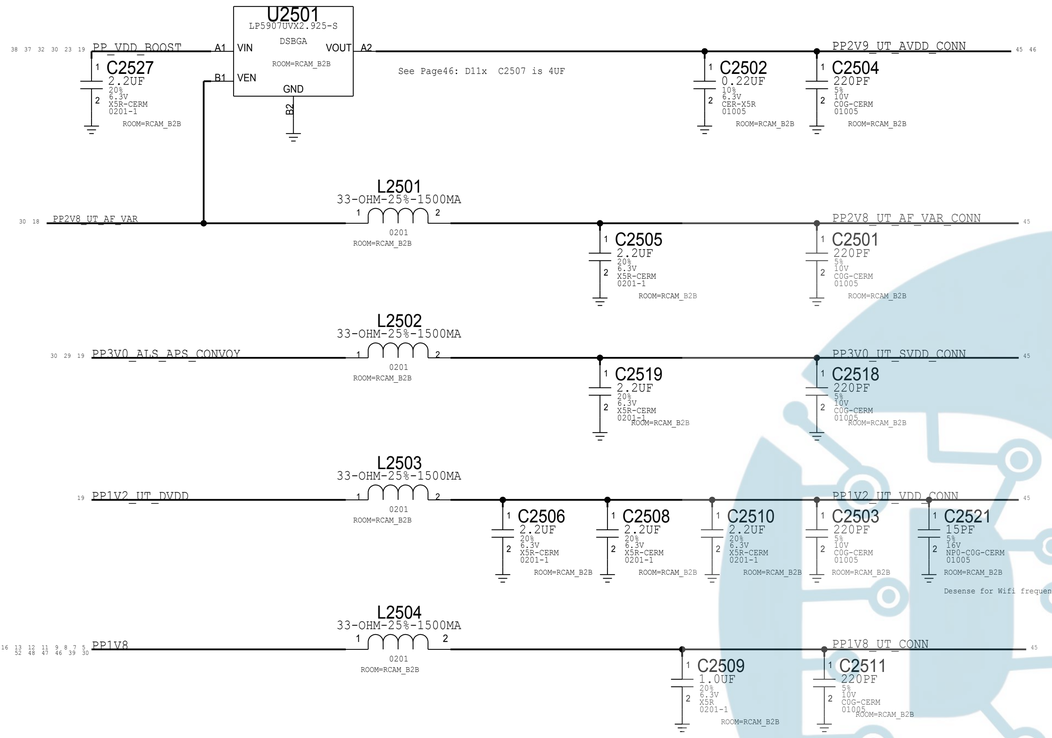
BOSCH (APN:338S00188): nostuff C2420/C2421/C2422/C2423 and R2403 PU
ST (APN:338S00230): stuff C2420-C2423, C2420R2422 with 155S00017, stuff R2403 PU
C2420=4pF(131S0253),C2405=3pF(131S0251) per #25691124



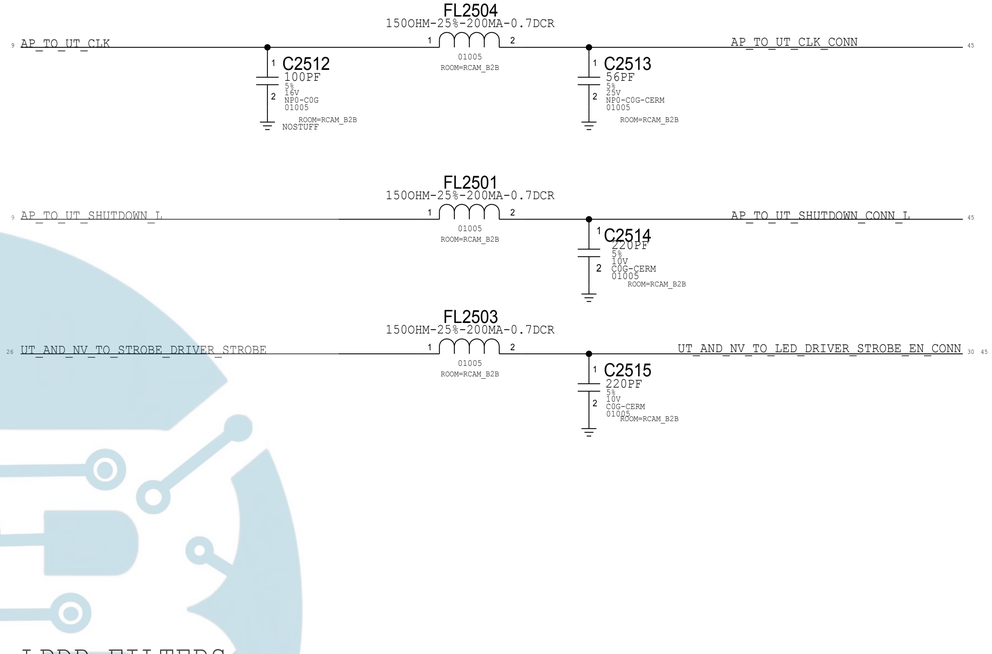
UTAH POWER

NOTE: OUTPUT IMPDEANCE MUST BE >0.005-OHM
IN ORDER TO MEET CAP ESR REQUIREMENT PER LDO SPEC.
VENDOR ALSO RECOMMENDS CIN = COUT FOR STABILITY

Scrub voltage selection

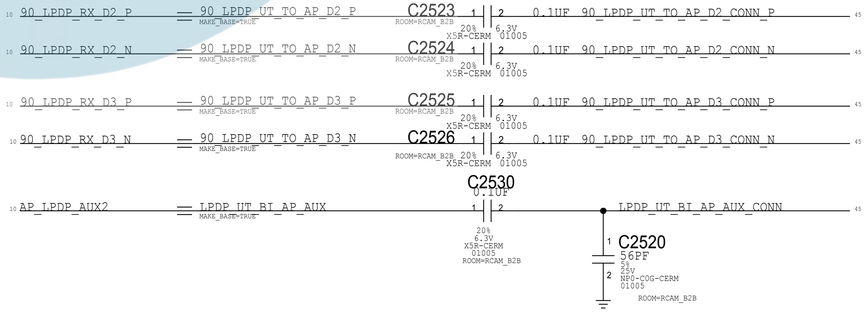


IO FILTERS



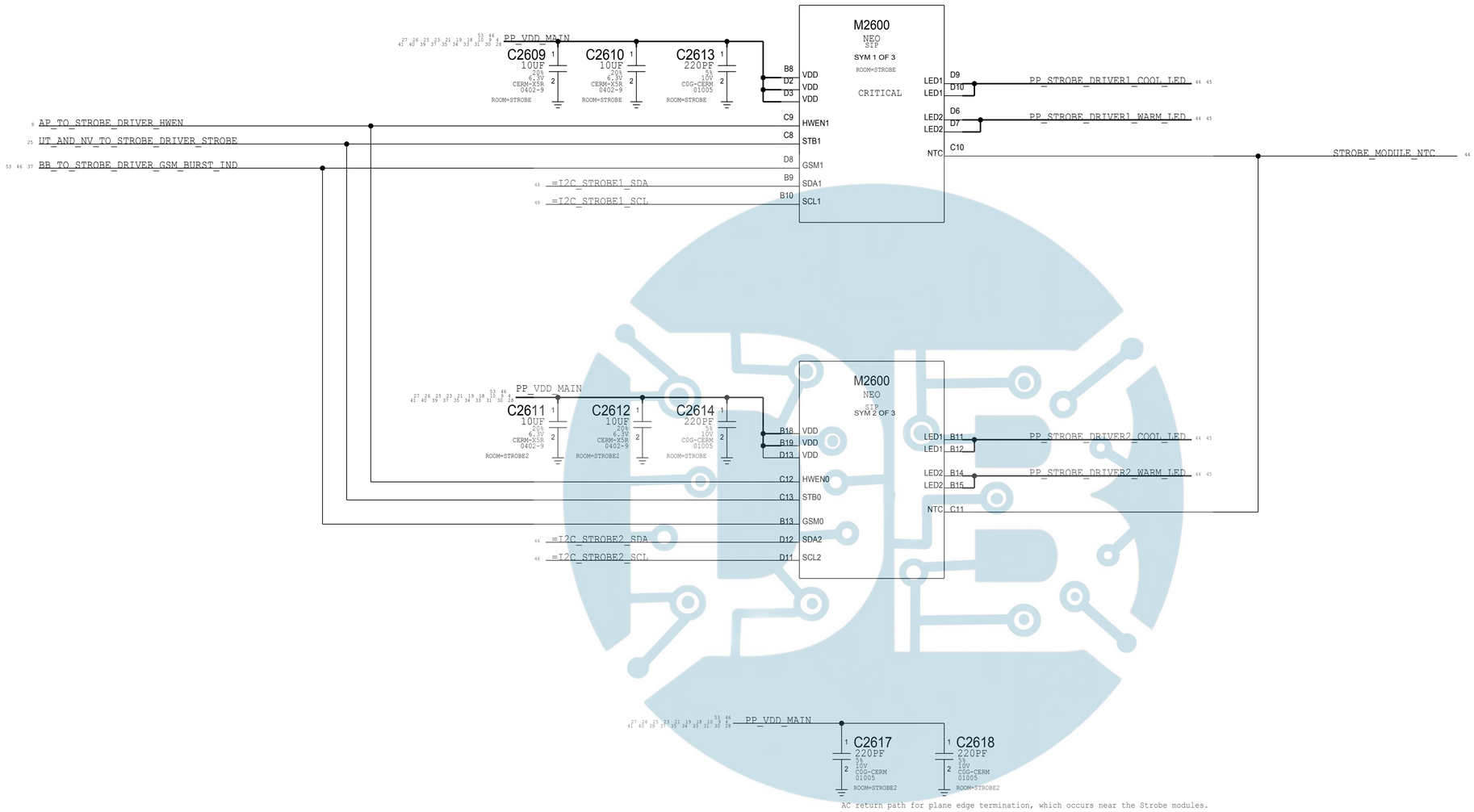
LPDP FILTERS

AC return path for LPDP which is referenced to GND and VDD_MAIN

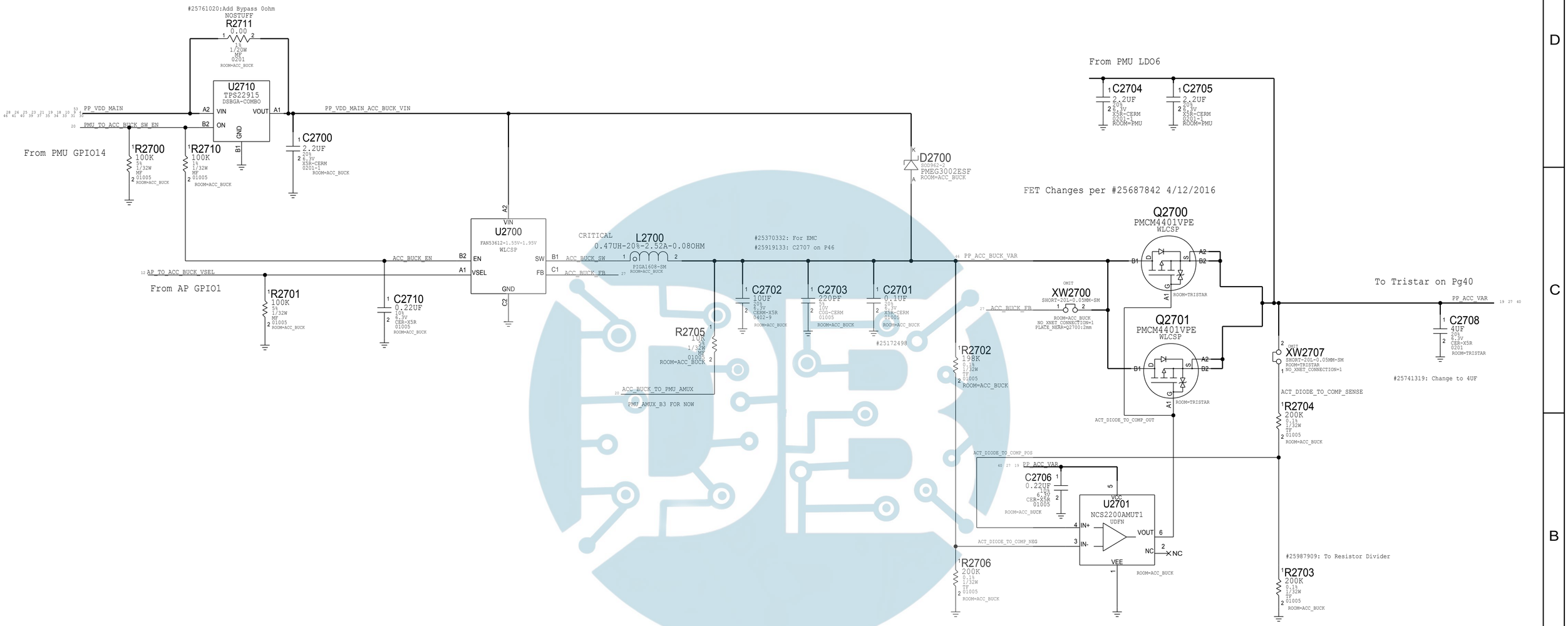


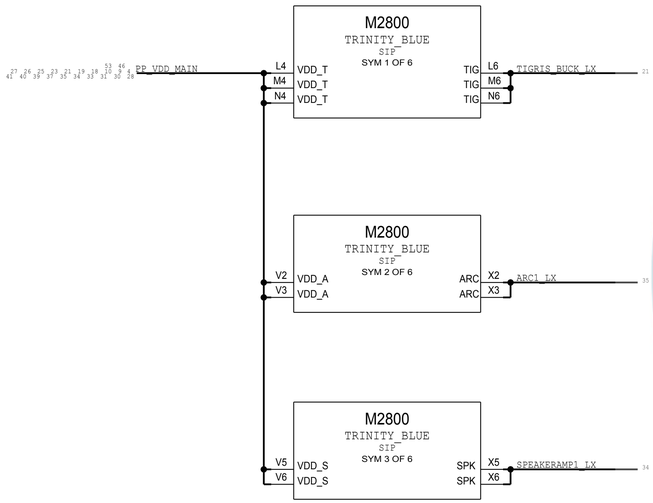
STROBE DRIVERS INSIDE NEO SIP MODULE

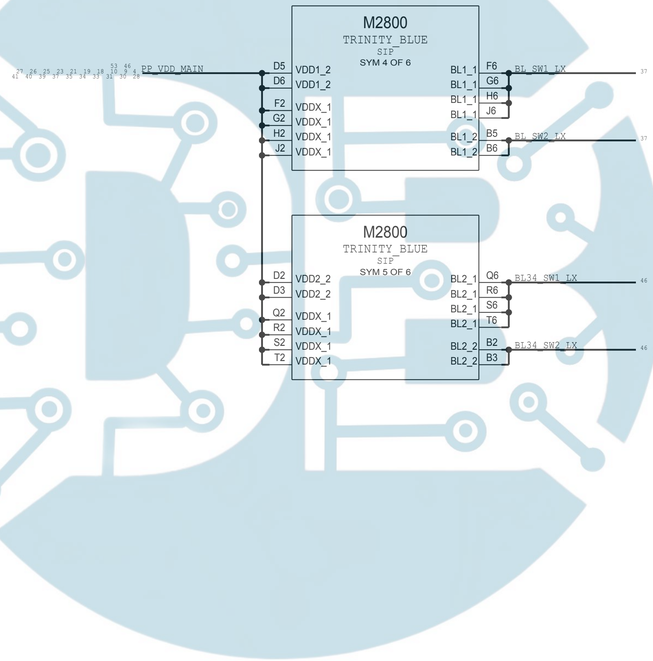
D10/sip_neo

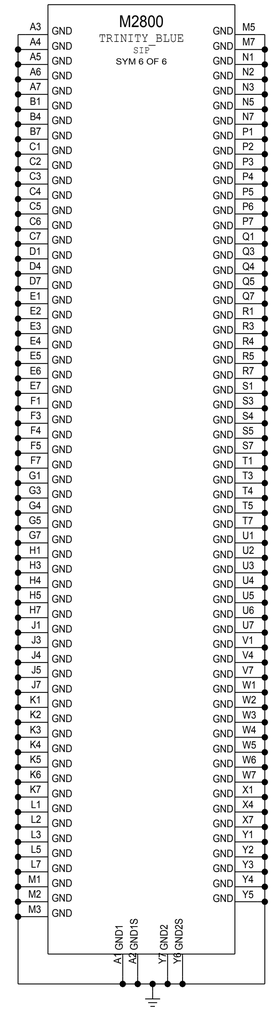


ACCESSORY BUCK

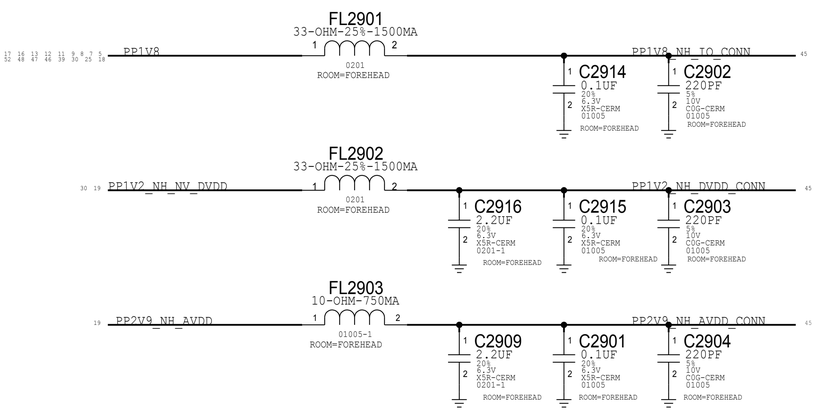



M2800
TRINITY_BLUE
SIP
SYM 1 OF 6
PP_VDD_MAIN
L4 VDD_T
M4 VDD_T
N4 VDD_T
TIG L6
TIG M6
TIG N6
TIGRIS_BUCK_LX
M2800
TRINITY_BLUE
SIP
SYM 2 OF 6
V2 VDD_A
V3 VDD_A
ARC X2
ARC X3
ARC1_LX
M2800
TRINITY_BLUE
SIP
SYM 3 OF 6
V5 VDD_S
V6 VDD_S
SPK X5
SPK X6
SPEAKERAMP1_LX

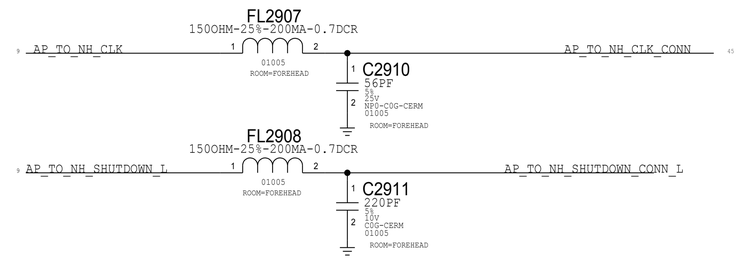

M2800
TRINITY_BLUE
SIP
SYM 4 OF 6
PP_VDD_MAIN
D5 VDD1_2
D6 VDD1_2
F2 VDDX_1
G2 VDDX_1
H2 VDDX_1
J2 VDDX_1
BL1_1 F6
BL1_1 G6
BL1_1 H6
BL1_1 J6
BL1_2 B5
BL1_2 B6
BL_SW1_LX
BL_SW2_LX
M2800
TRINITY_BLUE
SIP
SYM 5 OF 6
D2 VDD2_2
D3 VDD2_2
Q2 VDDX_1
R2 VDDX_1
S2 VDDX_1
T2 VDDX_1
BL2_1 Q6
BL2_1 R6
BL2_1 S6
BL2_1 T6
BL2_2 B2
BL2_2 B3
BL34_SW1_LX
BL34_SW2_LX


M2800
TRINITY_BLUE
SIP
SYM 6 OF 6
A3 GND
A4 GND
A5 GND
A6 GND
A7 GND
B1 GND
B4 GND
B7 GND
C1 GND
C2 GND
C3 GND
C4 GND
C5 GND
C6 GND
C7 GND
D1 GND
D4 GND
D7 GND
E1 GND
E2 GND
E3 GND
E4 GND
E5 GND
E6 GND
E7 GND
F1 GND
F3 GND
F4 GND
F5 GND
F7 GND
G1 GND
G3 GND
G4 GND
G5 GND
G7 GND
H1 GND
H3 GND
H4 GND
H5 GND
H7 GND
J1 GND
J3 GND
J4 GND
J5 GND
J7 GND
K1 GND
K2 GND
K3 GND
K4 GND
K5 GND
K6 GND
K7 GND
L1 GND
L2 GND
L3 GND
L5 GND
L7 GND
M1 GND
M2 GND
M3 GND
M5 GND
M7 GND
N1 GND
N2 GND
N3 GND
N5 GND
N7 GND
P1 GND
P2 GND
P3 GND
P4 GND
P5 GND
P6 GND
P7 GND
Q1 GND
Q3 GND
Q4 GND
Q5 GND
Q7 GND
R1 GND
R3 GND
R4 GND
R5 GND
R7 GND
S1 GND
S3 GND
S4 GND
S5 GND
S7 GND
T1 GND
T3 GND
T4 GND
T5 GND
T7 GND
U1 GND
U2 GND
U3 GND
U4 GND
U5 GND
U6 GND
U7 GND
V1 GND
V4 GND
V7 GND
W1 GND
W2 GND
W3 GND
W4 GND
W5 GND
W6 GND
W7 GND
X1 GND
X4 GND
X7 GND
Y1 GND
Y2 GND
Y3 GND
Y4 GND
Y5 GND
A1 GND1
A2 GND1S
Y7 GND2
Y6 GND2S

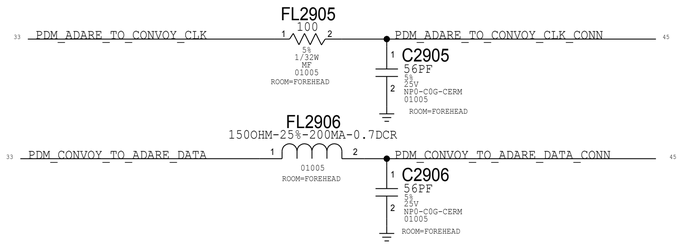
NEW HAMPSHIRE POWER



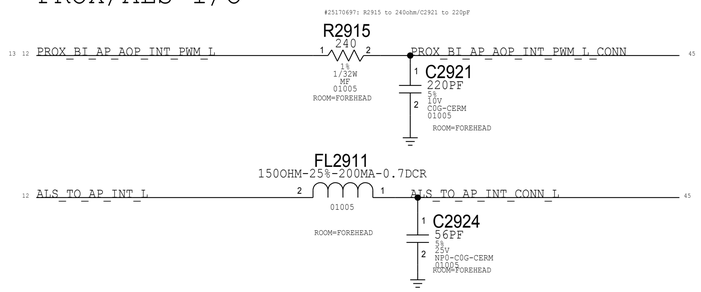
NEW HAMPSHIRE I/O



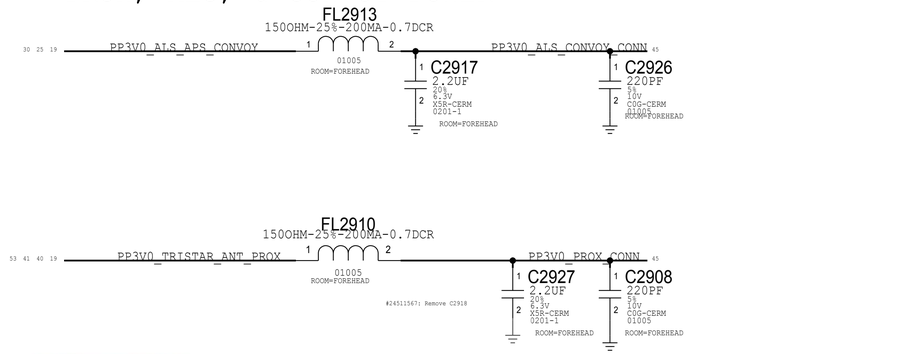
CONVOY I/O



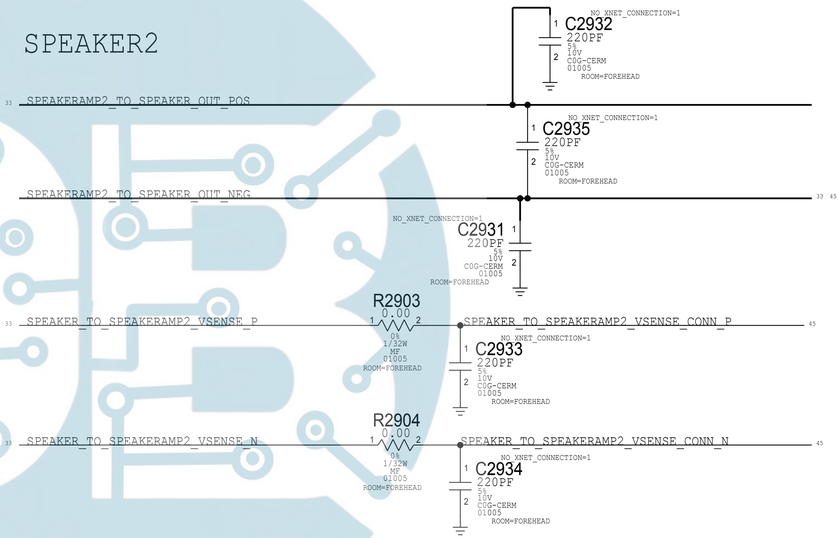
PROX/ALS I/O



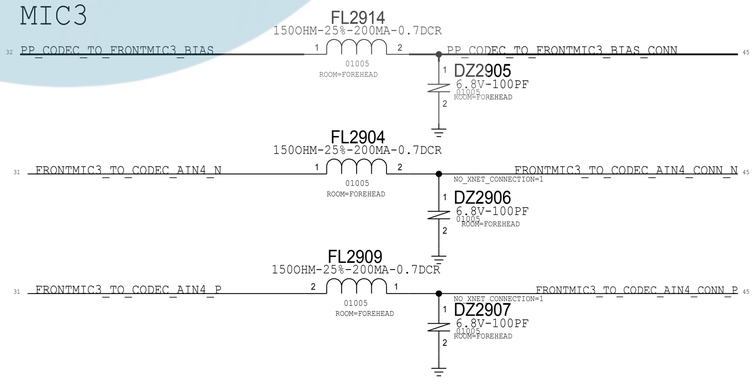
PROX, ALS, & CONVOY POWER



SPEAKER2



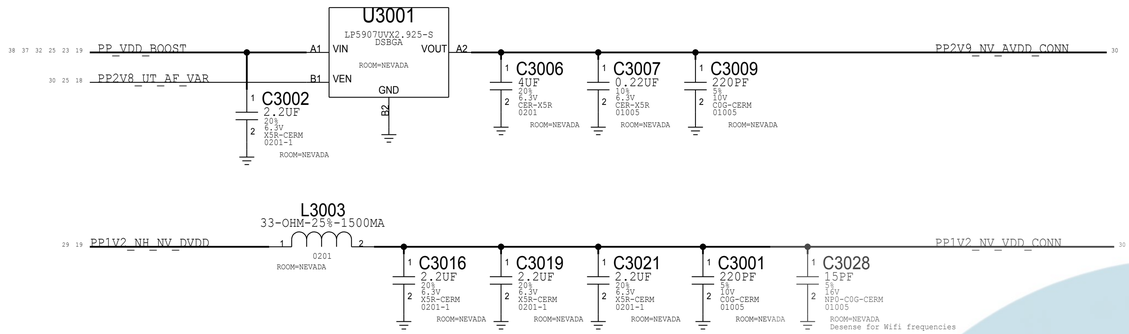
MIC3



NEVADA POWER

NOTE: OUTPUT IMPDEANCE MUST BE 50.005-OHM

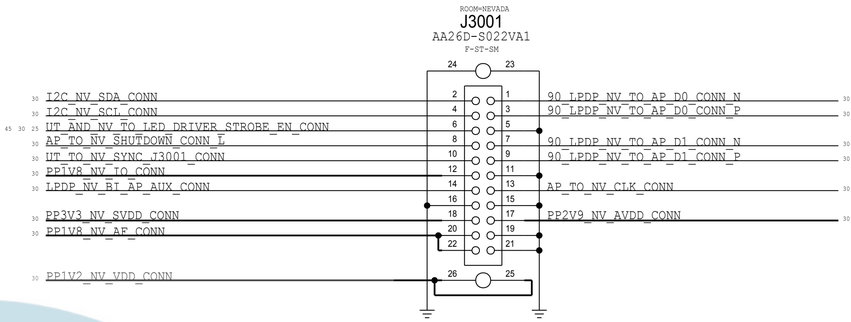
IN ORDER TO MEET CAP ESR REQUIREMENT PER LDO SPEC.
VENDOR ALSO RECOMMENDS CIN = COUT FOR STABILITY



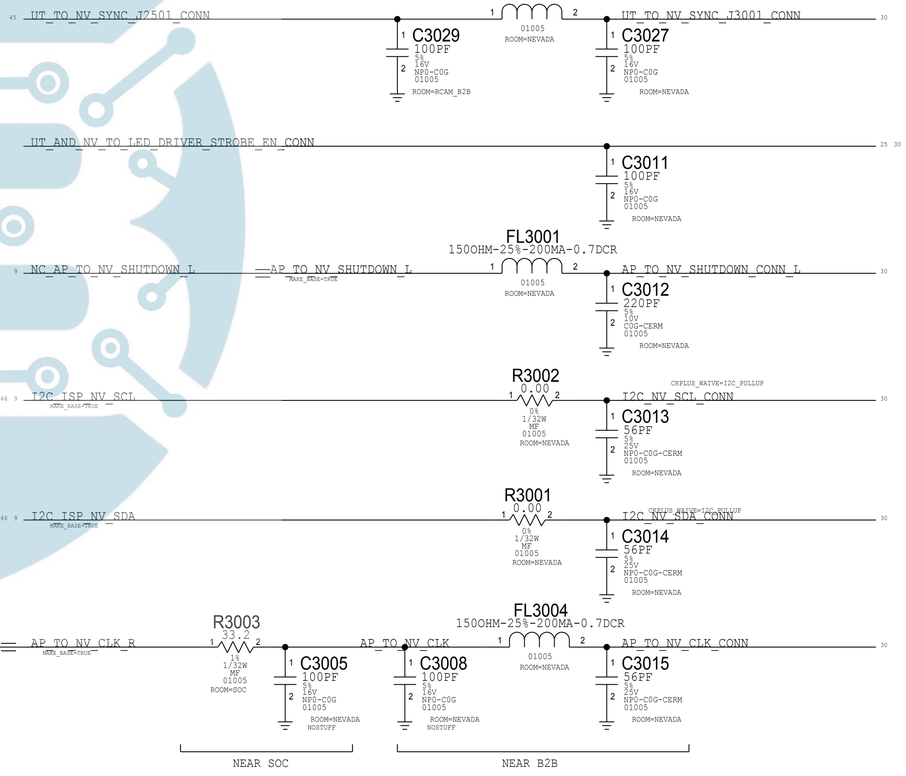
NEVADA CONNECTOR

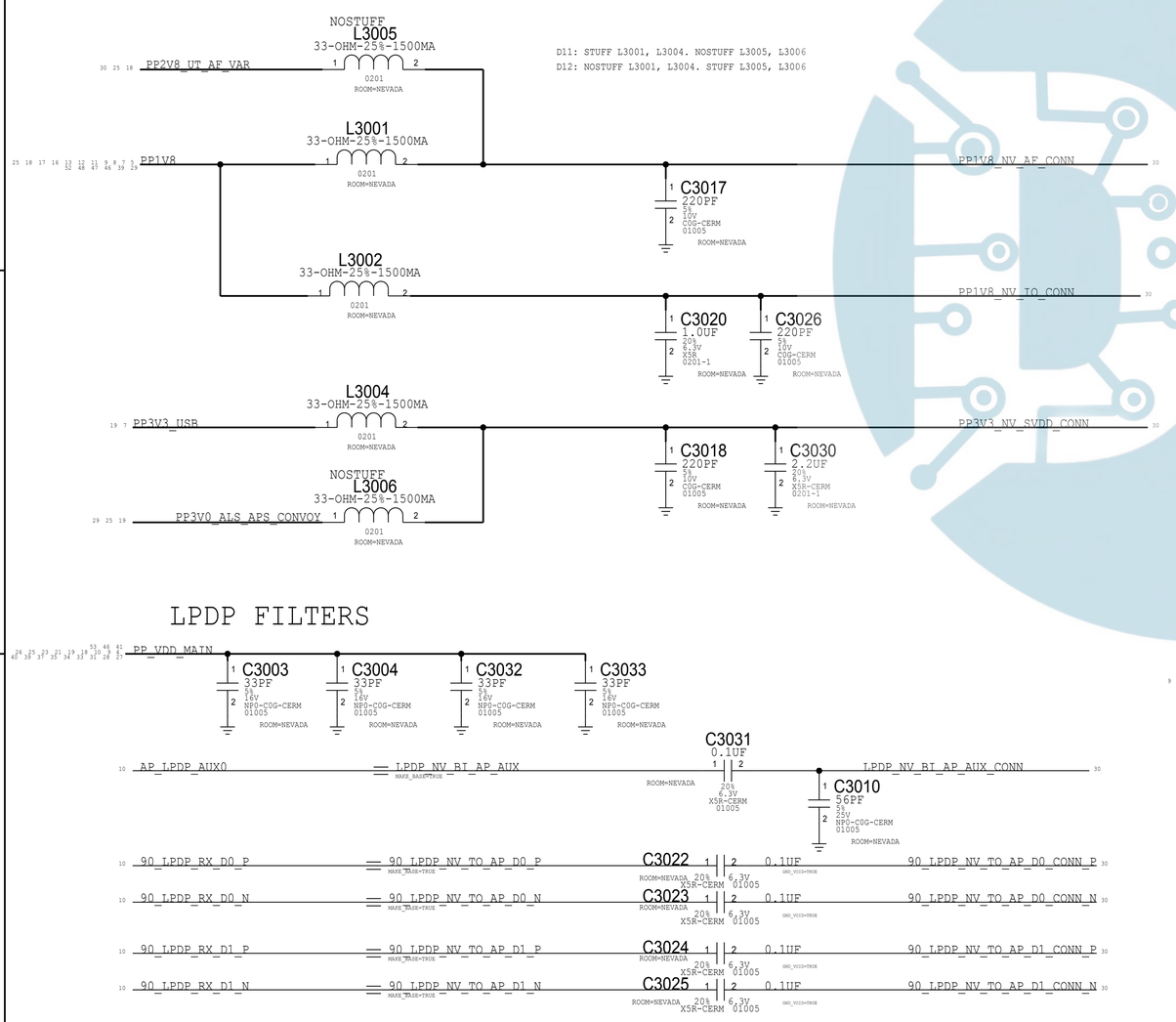
THIS ONE ---> 516S00152 RCPT (USED ON MLB)
516S00151 PLUG

THIS PAGE UNIQUE TO LARGE FORM FACTOR
OTHER FORM FACTOR SPECIFIC PAGES:
4 - Mechanical
46 - FF Specific



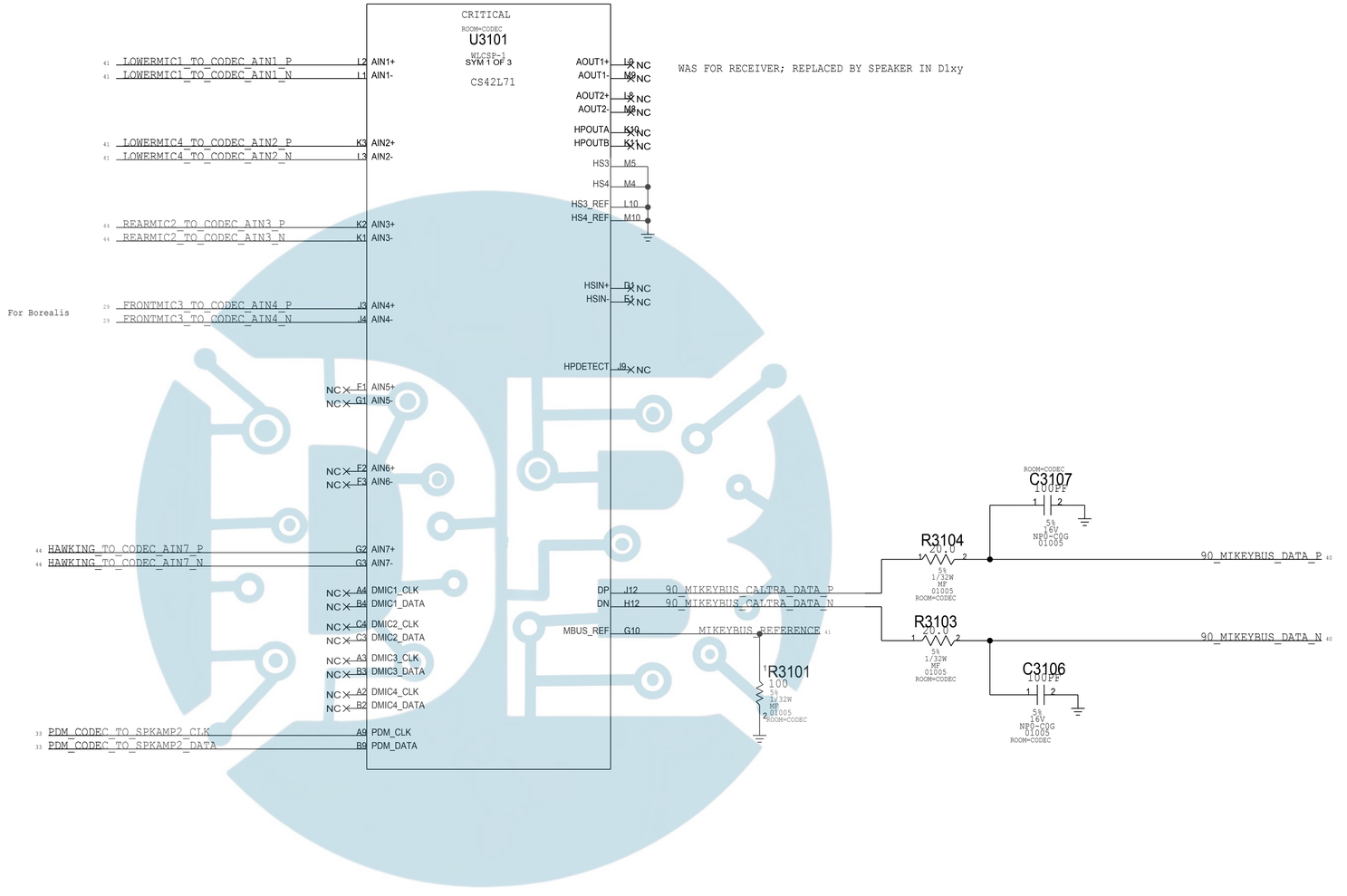
GPIO FILTERS

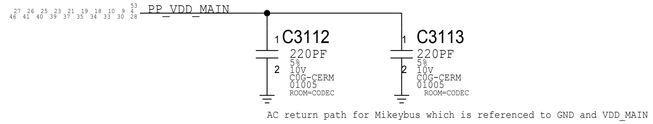




LPDP FILTERS

CALTRA AUDIO CODEC (ANALOG INPUTS & OUTPUTS)

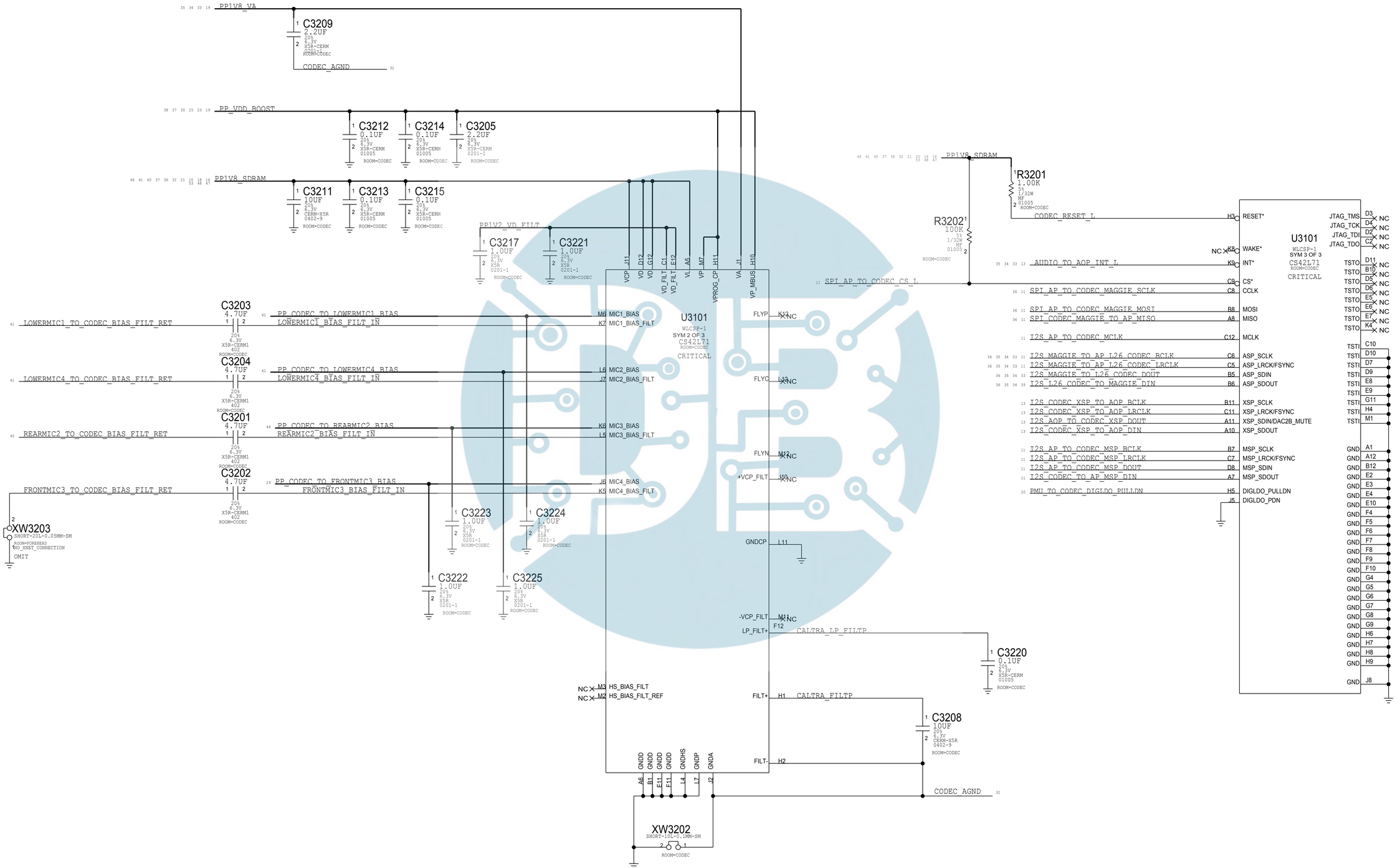




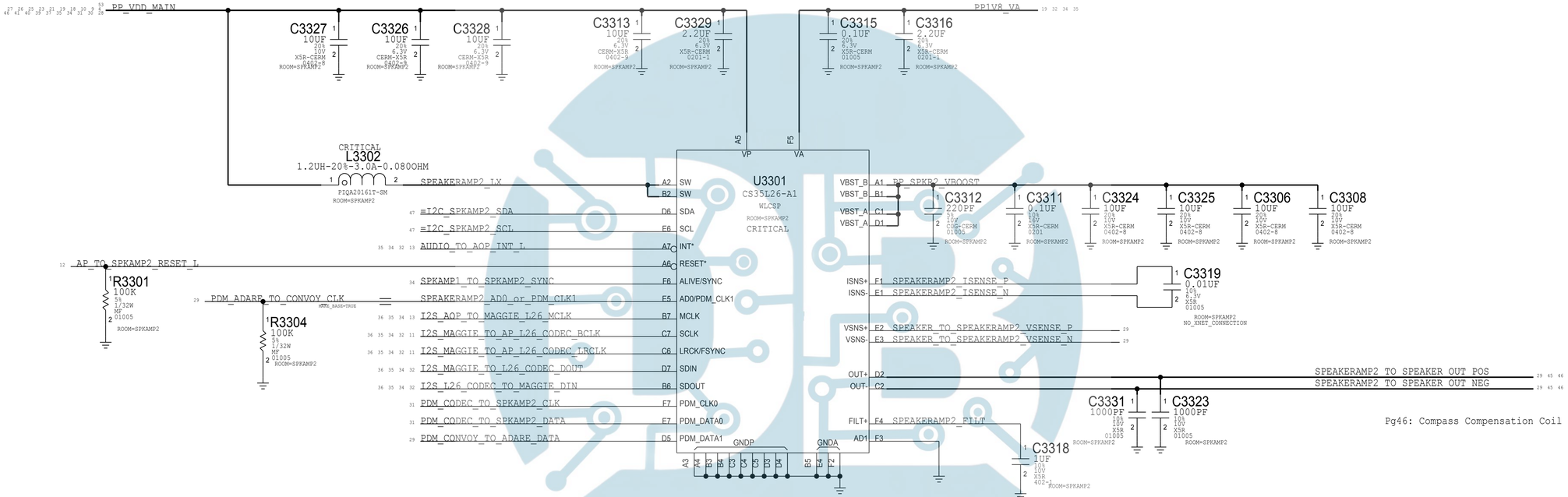
AC return path for Mikeybus which is referenced to GND and VDD_MAIN

Radar 21203307

CALTRA AUDIO CODEC (POWER & I/O)



SPEAKER AMPLIFIER 2 (North)



Pg46: Compass Compensation Coil

SPEAKER AMPLIFIER 1 (South)

#25112685,Remove C3414

PP_VDD_MAIN

C3407 10UF 20% 10V X5R-CERM 0402-8 ROOM=SPKAMP1

C3405 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SPKAMP1

C3424 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SPKAMP1

C3425 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SPKAMP1

C3426 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SPKAMP1

PP1V8_VA

U3402
CS35L26-A1
WLCSP
ROOM=SPKAMP1
CRITICAL

VP A5
VA F5

TO TRINITY

SPEAKERAMP1_LX	A2, B2	SW
=I2C_SPKAMP1_SDA	D6	SDA
=I2C_SPKAMP1_SCL	E6	SCL
AUDIO_TO_AOP_INT_L	A7	INT*
AOP_TO_SPKAMP1_ARC_RESET_L	A6	RESET*
SPKAMP1_TO_SPKAMP2_SYNC	F6	ALIVE/SYNC
SPEAKERAMP1_AD0	E5	AD0/PDM_CLK1
I2S_AOP_TO_MAGGIE_L26_MCLK	B7	MCLK
I2S_MAGGIE_TO_AP_L26_CODEC_BCLK	C7	SCLK
I2S_MAGGIE_TO_AP_L26_CODEC_LRCLK	C6	LRCK/FSYNC
I2S_MAGGIE_TO_L26_CODEC_DOUT	D7	SDIN
I2S_L26_CODEC_TO_MAGGIE_DIN	B6	SDOUT
NC	F7	PDM_CLK0
NC	E7	PDM_DATA0
NC	D5	PDM_DATA1
	A1, B1	VBST_B
	C1, D1	VBST_A
	F1	ISNS+
	E1	ISNS-
	E2	VSNS+
	E3	VSNS-
	D2	OUT+
	C2	OUT-
	F4	FILT+
	F3	AD1
	A3, A4, B3, B4, C3, C4, C5, D3, D4, B5, E4, F2	GNDP / GNDA

PULLED LOW ON PG 35

MAKE_BASE=TRUE

C3427 220PF 5% 10V C0G-CERM 01005 ROOM=SPKAMP1

C3428 0.1UF 10% 10V X5R-CERM 0201 ROOM=SPKAMP1

C3403 10UF 20% 10V X5R-CERM 0402-8 ROOM=SPKAMP1

C3404 10UF 20% 10V X5R-CERM 0402-8 ROOM=SPKAMP1

C3431 10UF 20% 10V X5R-CERM 0402-8 ROOM=SPKAMP1

C3432 10UF 20% 10V X5R-CERM 0402-8 ROOM=SPKAMP1

C3430 0.01UF 10% 6.3V X5R 01005 ROOM=SPKAMP1 NO_XNET_CONNECTION

SPEAKERAMP1_ISENSE_P

SPEAKERAMP1_ISENSE_N

SPEAKER_TO_SPEAKERAMP1_VSENSE_P

SPEAKER_TO_SPEAKERAMP1_VSENSE_N

SPEAKERAMP1_TO_SPEAKER_OUT_POS

SPEAKERAMP1_TO_SPEAKER_OUT_NEG

SPEAKERAMP1_FILT

C3429 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=SPKAMP1

C3422 1000PF 10% 10V X5R 01005 ROOM=SPKAMP1

C3434 1000PF 10% 10V X5R 01005 ROOM=SPKAMP1

ARC DRIVER

#25742582,Add back C3531 for D10x at Pg46

PP_VDD_MAIN

C3530 10UF 20% 10V X5R-CERM 0402-8 ROOM=ARC1

C3525 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=ARC1

C3532 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=ARC1

PP1V8_VA

C3527 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=ARC1

C3534 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=ARC1

TO TRINITY

ARC1_LX

=I2C_ARC1_SDA

=I2C_ARC1_SCL

AUDIO_TO_AOP_INT_L

AOP_TO_SPKAMP1_ARC_RESET_L

R3508 100K 5% 1/32W MF 01005 ROOM=ARC1

NC FROM HOMER PER #25452686

PP1V8_VA

ARC1_AD0

I2S_AOP_TO_MAGGIE_L26_MCLK

I2S_MAGGIE_TO_AP_L26_CODEC_BCLK

I2S_MAGGIE_TO_AP_L26_CODEC_LRCLK

I2S_MAGGIE_TO_L26_CODEC_DOUT

I2S_L26_CODEC_TO_MAGGIE_DIN

NOSTUFF C3501 10PF 5% 16V CERM 01005 ROOM=ARC1

U3502 CS35L26-A1 WLCSP ROOM=SPKAMP2 CRITICAL

A2	SW	VP	A5
B2	SW	VA	F5
D6	SDA	VBST_B	A1
E6	SCL	VBST_B	B1
A7	INT*	VBST_A	C1
A6	RESET*	VBST_A	D1
F6	ALIVE/SYNC	ISNS+	F1
E5	AD0/PDM_CLK1	ISNS-	E1
B7	MCLK	VSNS+	E2
C7	SCLK	VSNS-	E3
C6	LRCK/FSYNC	OUT+	D2
D7	SDIN	OUT-	C2
B6	SDOUT	FILT+	F4
F7	PDM_CLK0	AD1	F3
E7	PDM_DATA0		
D5	PDM_DATA1		
A3 A4 B3 B4 C3 C4 C5 D3 D4	GNDP	B5 E4 F2	GNDA

PP_ARC1_VBOOST

C3526 220PF 5% 10V C0G-CERM 01005 ROOM=ARC1

C3535 0.1UF 10% 6.3V X5R-CERM 0201 ROOM=ARC1

C3537 10UF 20% 10V X5R-CERM 0402-8 ROOM=ARC1

C3524 10UF 20% 10V X5R-CERM 0402-8 ROOM=ARC1

C3538 10UF 20% 10V X5R-CERM 0402-8 ROOM=ARC1

C3539 10UF 20% 10V X5R-CERM 0402-8 ROOM=ARC1

ARC1_ISENSE_P

ARC1_ISENSE_N

C3528 0.01UF 10% 6.3V X5R 01005 ROOM=ARC1 NO_XNET_CONNECTION

SOLENOID1_TO_ARC1_VSENSE_POS

SOLENOID1_TO_ARC1_VSENSE_NEG

ARC1_TO_SOLENOID1_OUT_POS

ARC1_TO_SOLENOID1_OUT_NEG

C3529 1000PF 10% 10V X5R 01005 ROOM=ARC1

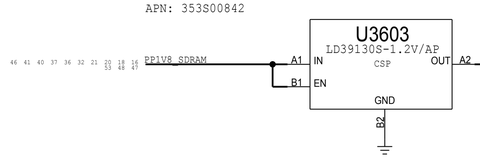
C3542 1000PF 10% 10V X5R 01005 ROOM=ARC1

ARC1_FILT

C3536 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=ARC1

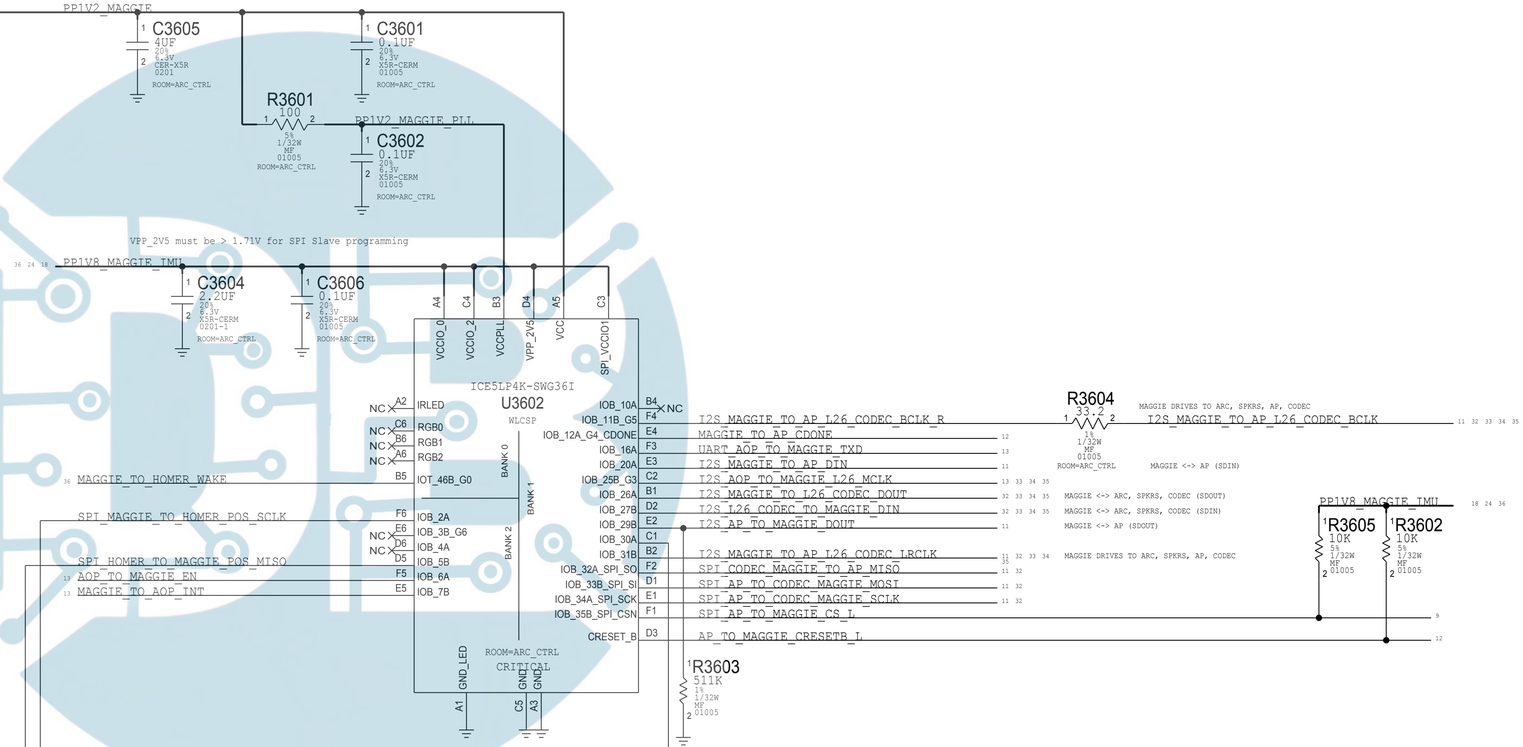
MAGGIE LDO

APN: 353S00842



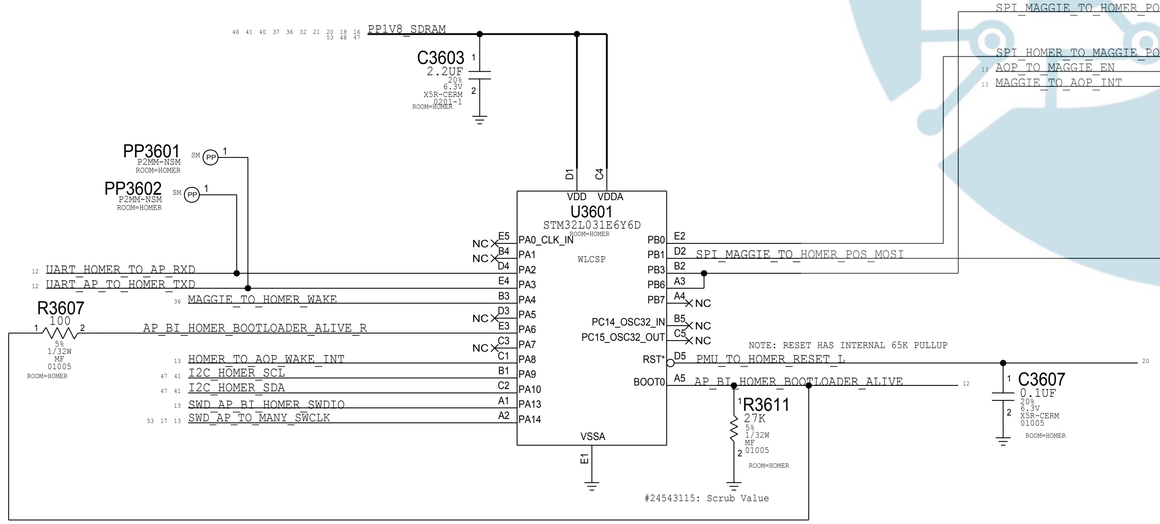
MAGGIE

APN: 336S00020



HOMER STM32L0 MICRO

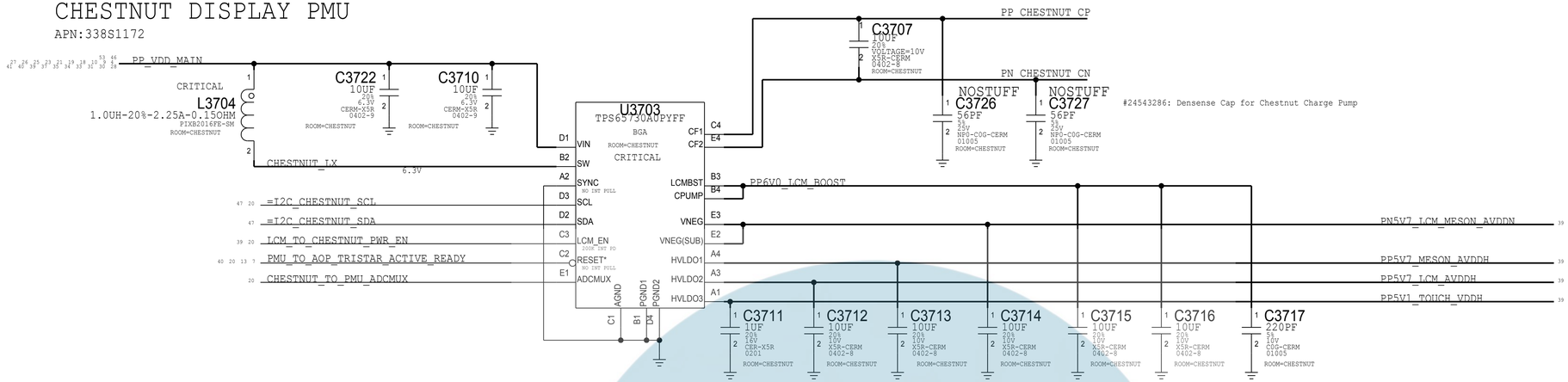
STM32L03 APN: 337S00231



DISPLAY & TOUCH - POWER SUPPLIES

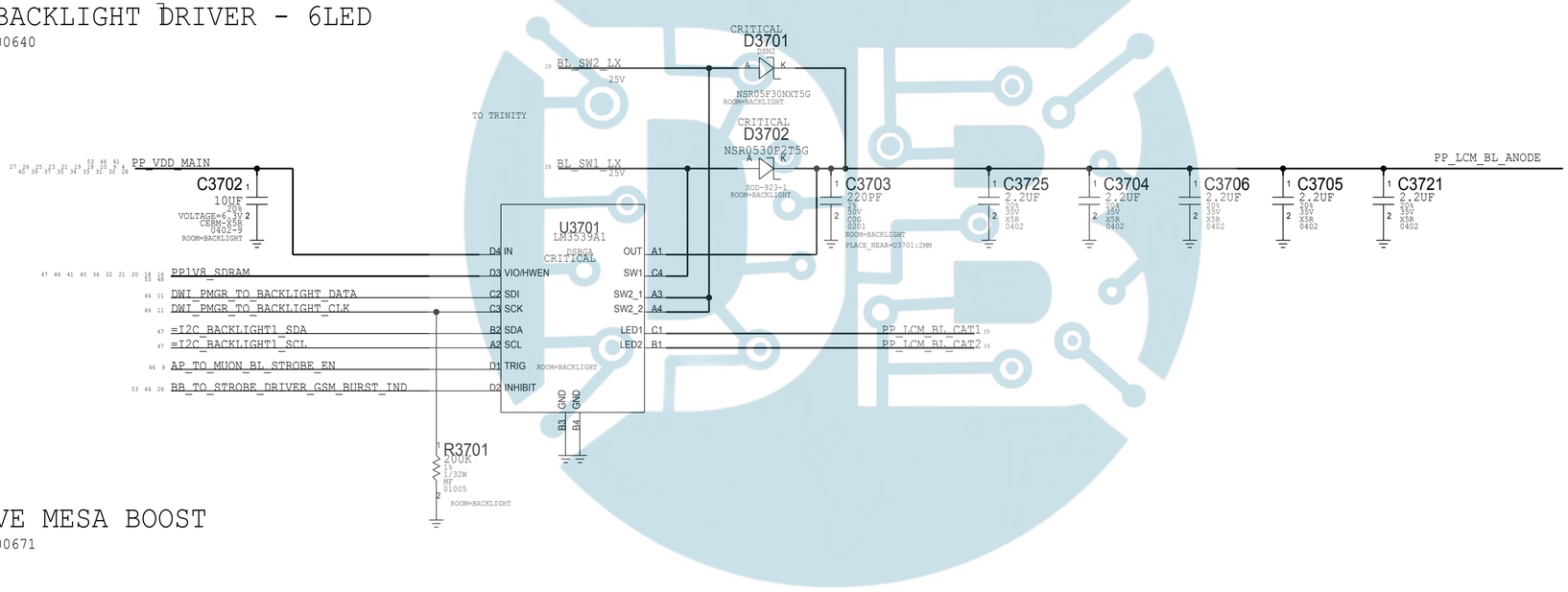
CHESTNUT DISPLAY PMU

APN:338S1172



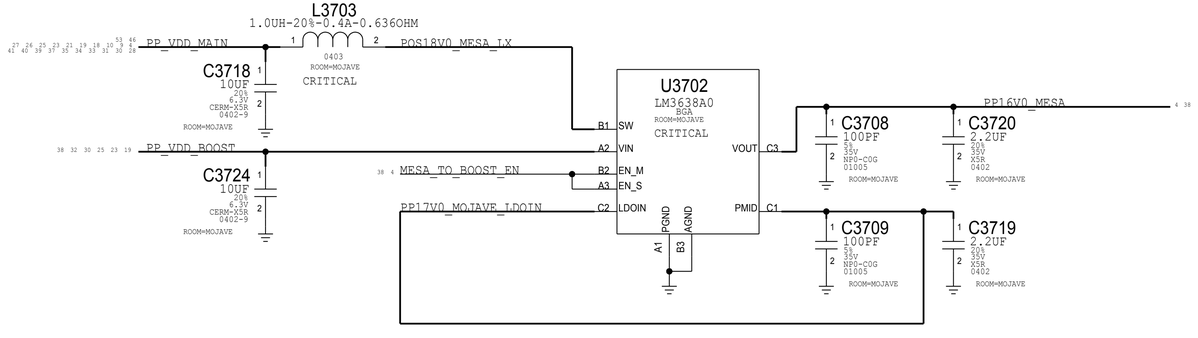
LED BACKLIGHT DRIVER - 6LED

APN:353s00640



MOJAVE MESA BOOST

APN:353S00671



MESA POWER

FL3803
80-OHM-25%-0.52A-0.17OHM
0201
ROOM=MAMBA_MESA

PP3V0_MESA → PP3V0_MESA_CONN

C3813 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=MAMBA_MESA
C3815 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=MAMBA_MESA
C3821 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=MAMBA_MESA
C3822 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MAMBA_MESA
C3804 220PF 5% 10V C0G-CERM 01005 ROOM=MAMBA_MESA

FL3801
150OHM-25%-200MA-0.7DCR
01005
ROOM=MAMBA_MESA

PP1V8_MESA → PP1V8_MESA_CONN

C3814 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=MAMBA_MESA
C3802 220PF 5% 10V C0G-CERM 01005 ROOM=MAMBA_MESA

FL3802
150OHM-25%-200MA-0.7DCR
01005
ROOM=MAMBA_MESA

PP1V6_MESA → PP1V6_MESA_CONN

C3803 100PF 5% 16V NP0-C0G 01005 ROOM=MAMBA_MESA

MESA DIGITAL I/O

FL3807
150OHM-25%-200MA-0.7DCR
01005
ROOM=MAMBA_MESA

SPI_AP_TO_MESA_MOSI → SPI_AP_TO_MESA_MOSI_CONN

R3807 511K 1% 1/32W MF 01005 ROOM=MAMBA_MESA
C3816 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

R3809 0.00 0% 1/32W MF 01005 ROOM=MAMBA_MESA

SPI_AP_TO_MESA_SCLK → SPI_AP_TO_MESA_SCLK_CONN

R3808 511K 1% 1/32W MF 01005 ROOM=MAMBA_MESA
C3817 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

R3811 33.2 1% 1/32W MF 01005 ROOM=MAMBA_MESA

SPI_MESA_TO_AP_MISO → SPI_MESA_TO_AP_MISO_CONN

C3818 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

R3801 681 1% 1/32W MF 01005 ROOM=MAMBA_MESA

MESA_TO_AP_INT → MESA_TO_AP_INT_CONN

C3819 100PF 5% 16V NP0-C0G 01005 ROOM=MAMBA_MESA

R3802 681 1% 1/32W MF 01005 ROOM=MAMBA_MESA

MESA_TO_BOOST_EN → MESA_TO_BOOST_EN_CONN

C3801 100PF 5% 16V NP0-C0G 01005 ROOM=MAMBA_MESA

FL3811
150OHM-25%-200MA-0.7DCR
01005

AOP_TO_MESA_BLANKING_EN → AOP_TO_MESA_BLANKING_EN_CONN

C3825 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

MAMBA AND MESA CONNECTOR

MLB: 516S00141 (RCPT)
FLEX: 516S00142 (PLUG)

CRITICAL
J3801
BB35C-RA24-3A
F-ST-SM
ROOM=MAMBA_MESA

Matches flex_x452_acf, schematic revision 1.5.0 pinout

PP3V0_MESA_CONN	2	1	PP1V8_MESA_CONN
	4	3	
	6	5	MESA_TO_AOP_FDINT_CONN
PP1V6_MESA_CONN	8	7	I2C_MESA_TURTLE_SDA_CONN
GUARD	10	9	I2C_MESA_TURTLE_SCL_CONN
MAMBA_TO_LCM_MDRIVE_CONN_MESA	12	11	MESA_TO_BOOST_EN_CONN
	14	13	MESA_TO_AP_INT_CONN
AP_TO_TOUCH_MAMBA_RESET_CONN_L	16	15	SPI_AP_TO_MESA_SCLK_CONN
TP_MAMBA_HINT_L	18	17	SPI_AP_TO_MESA_MOSI_CONN
=I2C_MAMBA_SDA	20	19	AOP_TO_MESA_BLANKING_EN_CONN
=I2C_MAMBA_SCL	22	21	SPI_MESA_TO_AP_MISO_CONN
PP1V8_TOUCH_TO_MAMBA_CONN	24	23	PP2V75_MAMBA_CONN
	28	27	
		30	

LCM_TO_MAMBA_MSYNC_CONN → C3807 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

P2MM-NSM SM
PP3801

MAMBA_POWER

NOTE: OUTPUT IMPEDANCE MUST BE >0.005-OHM
IN ORDER TO MEET CAP ESR REQUIREMENT PER LDO SPEC.
VENDOR ALSO RECOMMENDS CIN = COUT FOR STABILITY

TI:353S00576
ST:353S00932

PP_VDD_BOOST → C3828 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=MAMBA_MESA

XW3801
SHORT-20L-0.05MM-SM
ROOM=PMU
OMIT

PP1V8_TOUCH → MAMBA_LDO_EN

U3801
LP5907SNX-2.75
X2SON
ROOM=MAMBA_MESA
VIN, VOUT, EN, GND EPAD

C3823 10UF 20% 10V X5R-CERM 0402-8 ROOM=MAMBA_MESA
C3812 220PF 5% 10V C0G-CERM 01005 ROOM=MAMBA_MESA

PP2V75_MAMBA_CONN

R3805 0.00 0% 1/32W MF 01005 ROOM=MAMBA_MESA

PP1V8_TOUCH → PP1V8_TOUCH_TO_MAMBA_CONN

C3824 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=MAMBA_MESA
C3811 220PF 5% 10V C0G-CERM 01005 ROOM=MAMBA_MESA

MAMBA DIGITAL I/O

FL3804
150OHM-25%-200MA-0.7DCR
01005
ROOM=MAMBA_MESA

MAMBA_TO_LCM_MDRIVE → MAMBA_TO_LCM_MDRIVE_CONN_MESA

C3805 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

NOSTUFF
C3806 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

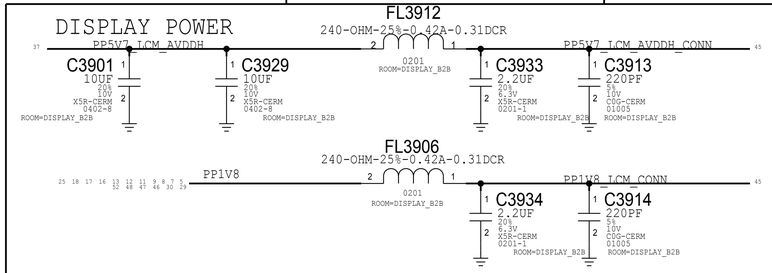
FL3806
150OHM-25%-200MA-0.7DCR
01005
ROOM=MAMBA_MESA

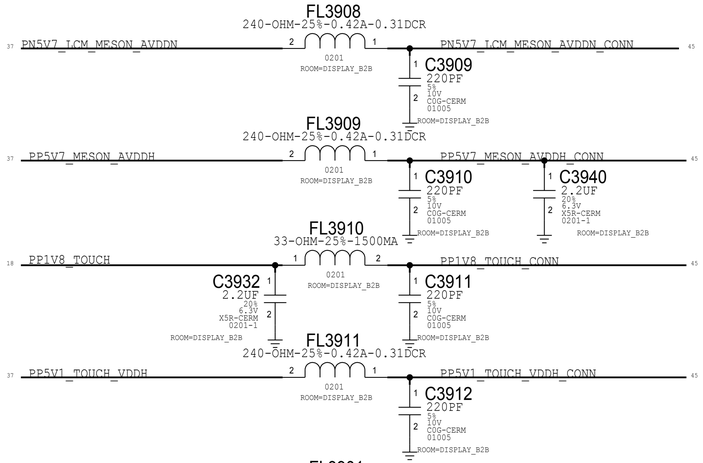
MESA_TO_AOP_FDINT → MESA_TO_AOP_FDINT_CONN

C3826 100PF 5% 16V NP0-C0G 01005 ROOM=MAMBA_MESA

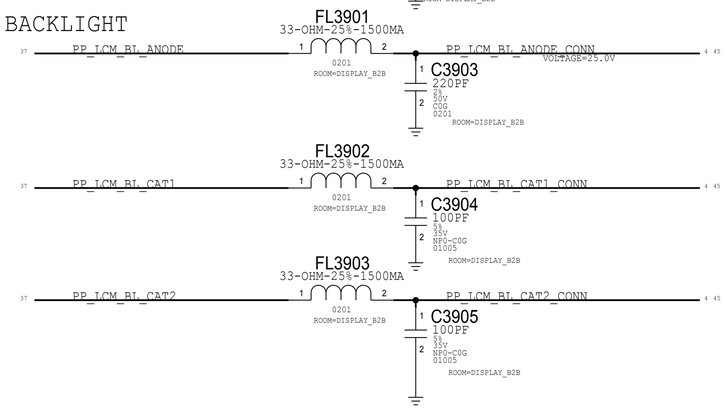
#24543342: stuff 100pF

DISPLAY POWER





BACKLIGHT

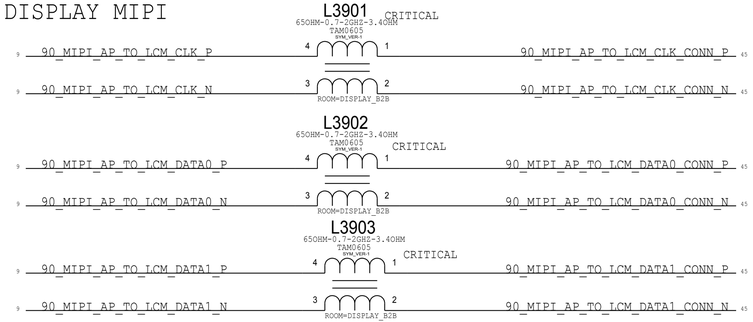


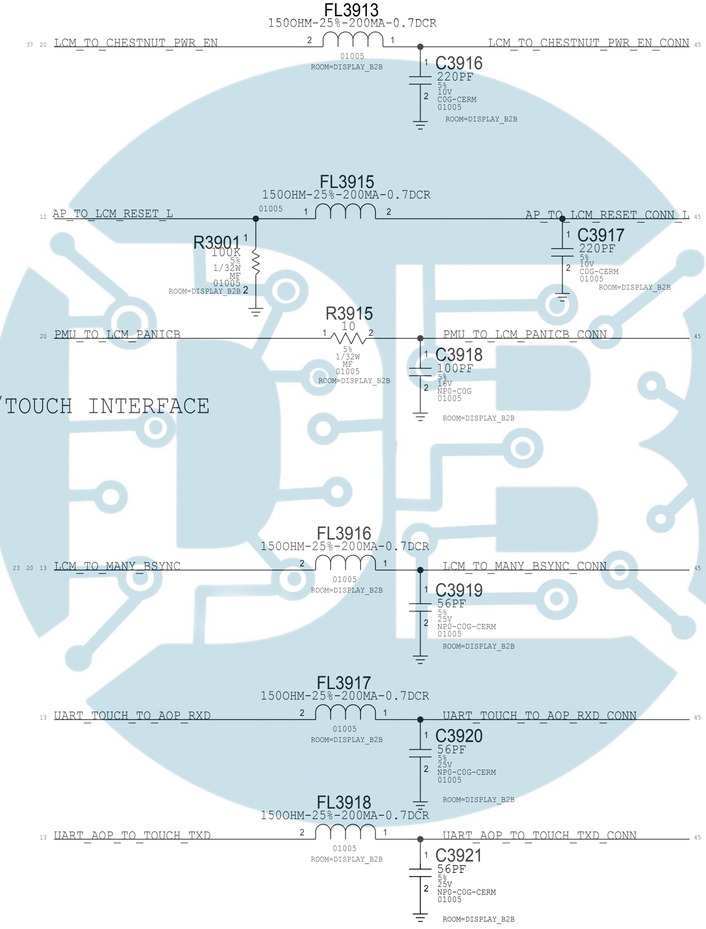
AC Coupling Caps

AC return path for LCM MIPI which is referenced to GND and VDD_MAIN

For placement "along the way" as we route from SOC to B2B.

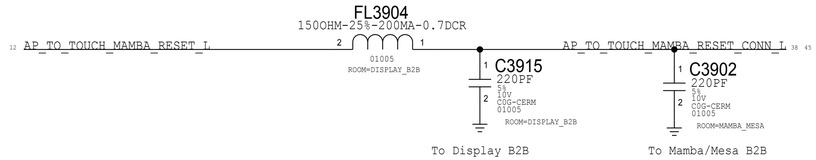
DISPLAY MIPI

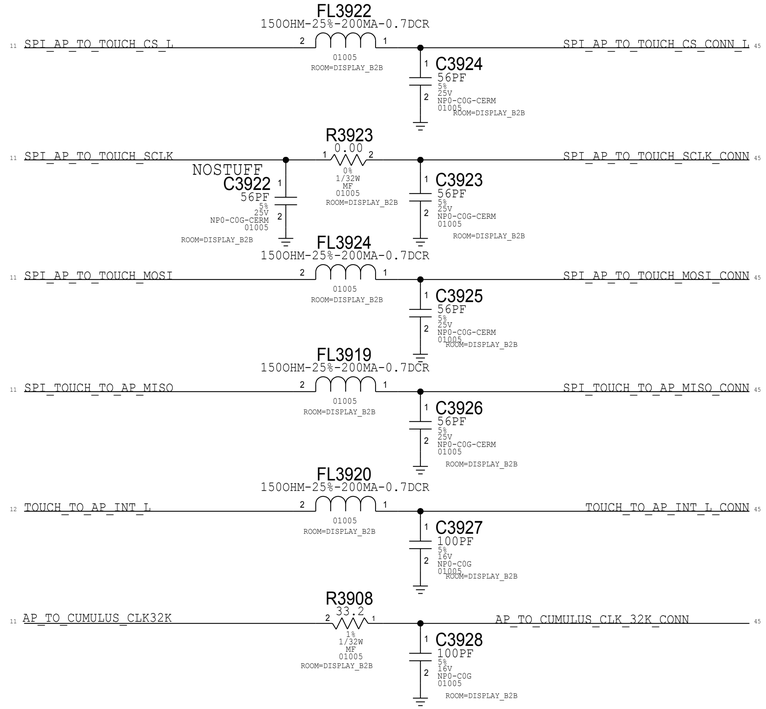




AOP/TOUCH INTERFACE

AP/TOUCH INTERFACE

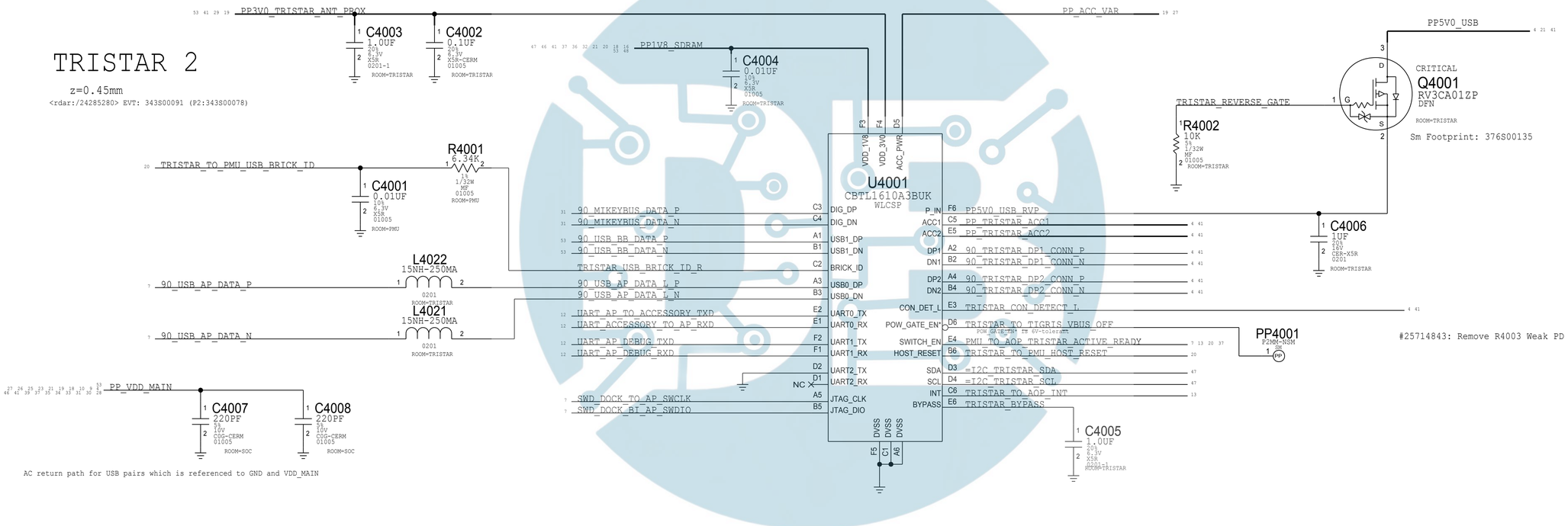




TRISTAR 2

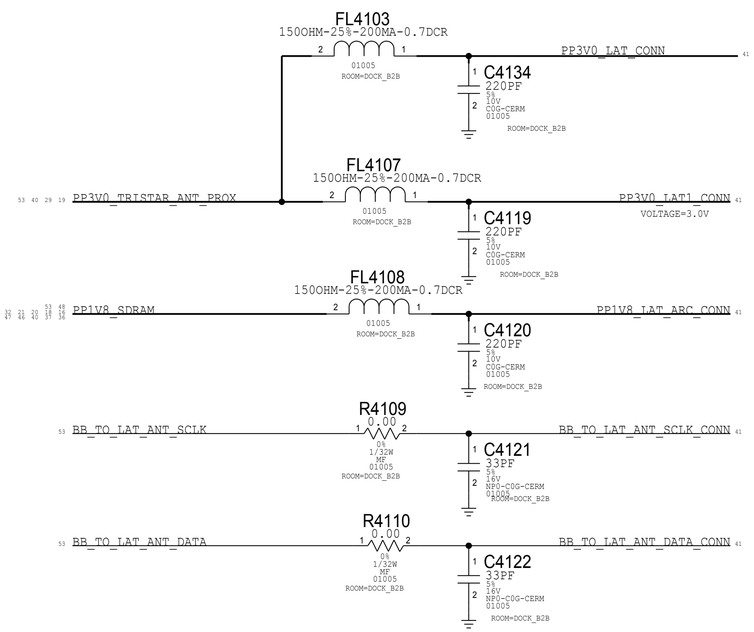
z=0.45mm

<rdar:/24285280> EVT: 343S00091 (P2:343S00078)

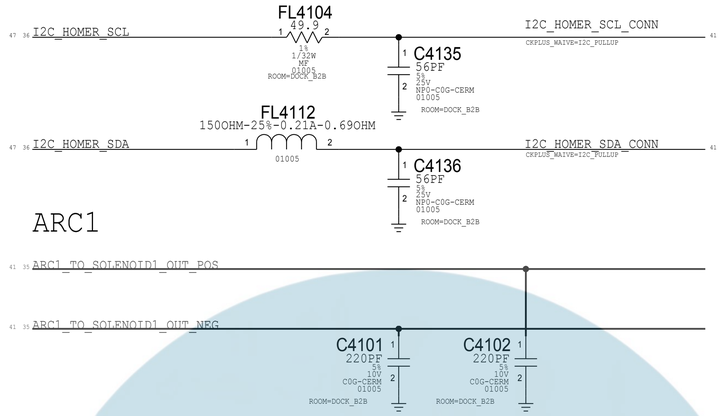


ANTENNA

Please loop in Matt Mow (Antenna Team)
when changing these components!

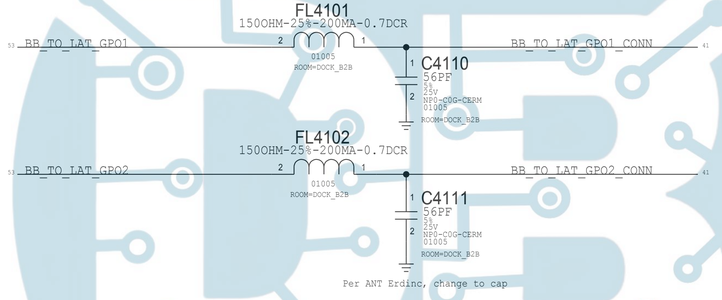


ARC CONTROL

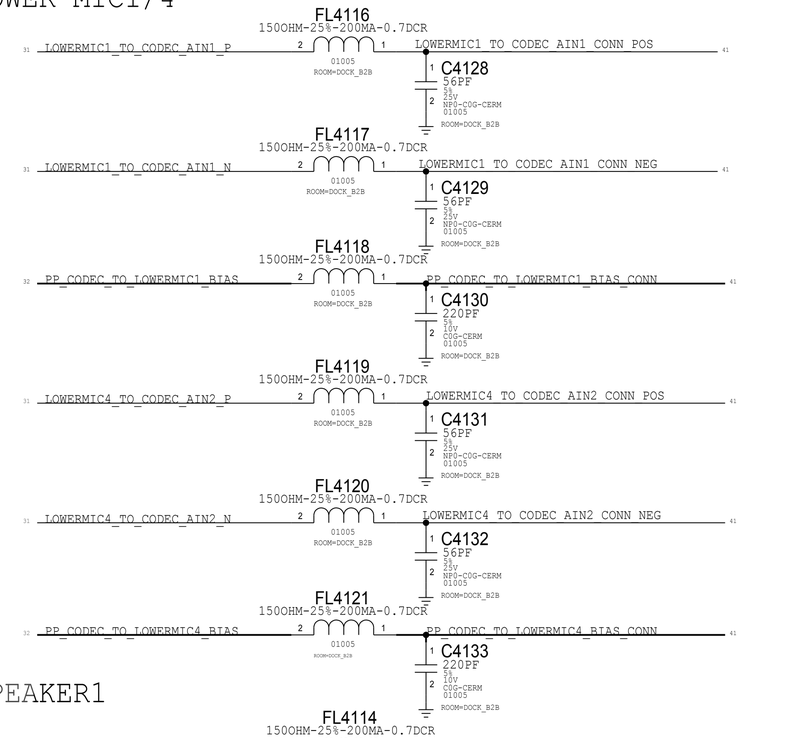


ARC1

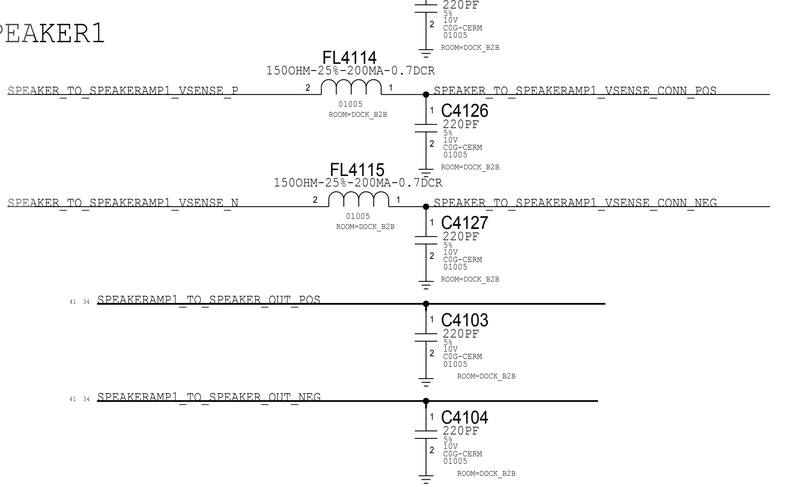
Antenna GPIO



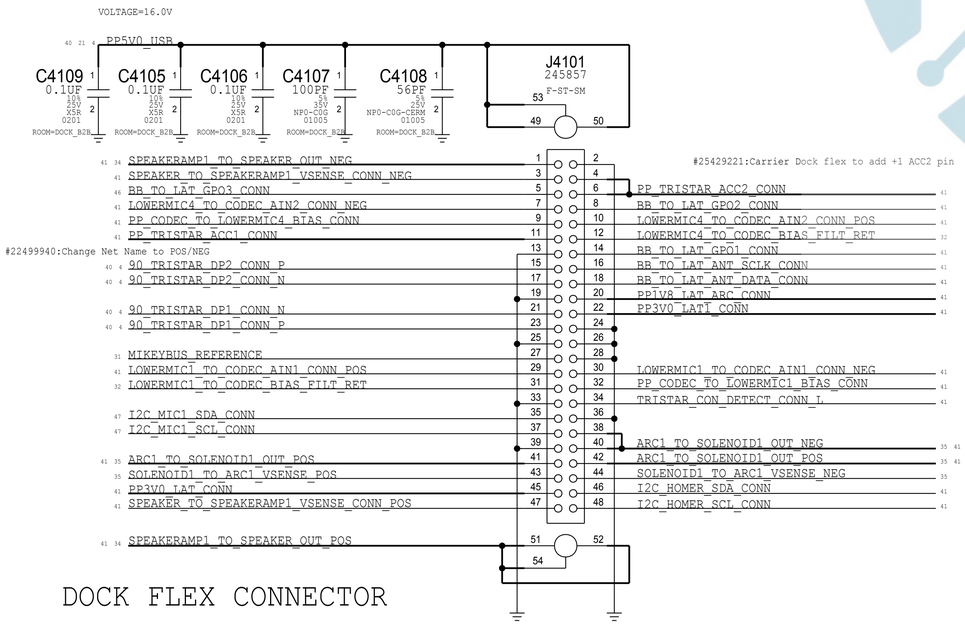
LOWER MIC1/4



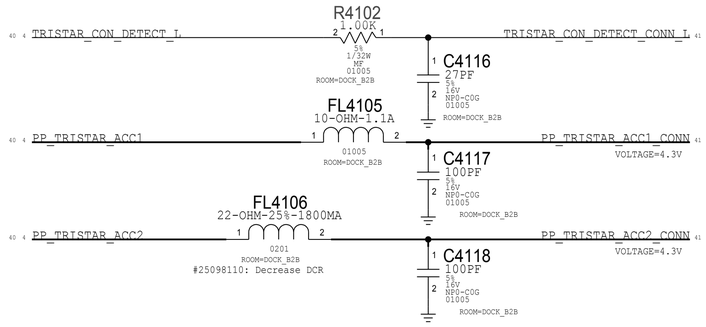
SPEAKER1



DOCK FLEX CONNECTOR

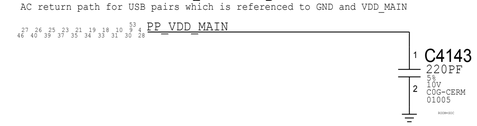


TRISTAR



USB AC Coupling

AC return path for USB pairs which is referenced to GND and VDD_MAIN



STROBE1

PP_STROBE_DRIVER1_WARM_LED

C4402 220PF 5% 10V COG-CERM 01005 ROOM=RIGHT_BUTTON

C4409 27PF 5% 16V NP0-C0G 01005 ROOM=RIGHT_BUTTON

PP_STROBE_DRIVER1_COOL_LED

C4406 220PF 5% 10V COG-CERM 01005 ROOM=RIGHT_BUTTON

C4408 27PF 5% 16V NP0-C0G 01005 ROOM=RIGHT_BUTTON

FL4404 150OHM-25%-200MA-0.7DCR 01005 ROOM=RIGHT_BUTTON

STROBE_MODULE_NTC → R4401 27K 0.5% 1/32W MF 01005 ROOM=RIGHT_BUTTON → STROBE_MODULE_NTC_CONN

C4407 220PF 5% 10V COG-CERM 01005 ROOM=RIGHT_BUTTON

#24544474: Can R4401 be changed to 5%?

STROBE2

PP_STROBE_DRIVER2_WARM_LED

C4410 220PF 5% 10V COG-CERM 01005 ROOM=RIGHT_BUTTON

C4413 27PF 5% 16V NP0-C0G 01005 ROOM=RIGHT_BUTTON

PP_STROBE_DRIVER2_COOL_LED

C4411 220PF 5% 10V COG-CERM 01005 ROOM=RIGHT_BUTTON

C4412 27PF 5% 16V NP0-C0G 01005 ROOM=RIGHT_BUTTON

BUTTONS

R4402 100 5% 1/32W MF 01005 ROOM=RIGHT_BUTTON

BUTTON_POWER_KEY_L → BUTTON_POWER_KEY_CONN_L

C4401 27PF 5% 6.3V NPO-C0G 0201 ROOM=RIGHT_BUTTON

DZ4401 0201 6.8V-6.2PF ROOM=RIGHT_BUTTON → CHASSIS_GND_BS401

FL4407 120-OHM-0.220A 01005 ROOM=LEFT_BUTTON

BUTTON_RINGER_A → BUTTON_RINGER_A_CONN

C4418 27PF 5% 6.3V NPO-C0G 0201 ROOM=LEFT_BUTTON

DZ4402 0201 6.8V-6.2PF ROOM=LEFT_BUTTON → CHASSIS_GND_BS401

R4405 100 5% 1/32W MF 01005 ROOM=LEFT_BUTTON

BUTTON_VOL_DOWN_L → BUTTON_VOL_DOWN_CONN_L

C4419 100PF 5% 16V NPO-C0G 01005 ROOM=LEFT_BUTTON

DZ4403 12V-33PF 01005-1 ROOM=LEFT_BUTTON → CHASSIS_GND_BS401

R4406 100 5% 1/32W MF 01005 ROOM=LEFT_BUTTON

BUTTON_VOL_UP_L → BUTTON_VOL_UP_CONN_L

C4420 100PF 5% 16V NPO-C0G 01005 ROOM=LEFT_BUTTON

DZ4404 12V-33PF 01005-1 ROOM=LEFT_BUTTON → CHASSIS_GND_BS401

HAWKING

#24678255:DOE with 10% and/20% cap

HAWKING_TO_CODEC_AIN7_N → C4417 0.22UF 20% 6.3V X5R 01005 ROOM=RIGHT_BUTTON → HAWKING_TO_CODEC_AIN7_N_CONN

C4421 0.22UF 20% 6.3V X5R 01005 ROOM=RIGHT_BUTTON

HAWKING_TO_CODEC_AIN7_P → FL4405 150OHM-25%-200MA-0.7DCR 01005 ROOM=RIGHT_BUTTON → HAWKING_TO_CODEC_AIN7_C_P (CKPLUS_WAIVE=MISS_N_DIFFPAIR) → HAWKING_TO_CODEC_AIN7_P_CONN

C4415 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=RIGHT_BUTTON

C4422 NOSTUFF 180PF 10% 10V CERM 01005 ROOM=RIGHT_BUTTON

FL4406 150OHM-25%-200MA-0.7DCR 01005 ROOM=RIGHT_BUTTON

PP1V8_HAWKING → PP1V8_HAWKING_CONN

C4416 2.2UF 20% 6.3V X5R-CERM 0201-1 ROOM=RIGHT_BUTTON

C4414 220PF 10% 10V C0G-CERM 01005 ROOM=RIGHT_BUTTON

MIC2 (ANC REF)

FL4403 150OHM-25%-200MA-0.7DCR 01005 ROOM=RIGHT_BUTTON

PP_CODEC_TO_REARMIC2_BIAS → PP_CODEC_TO_REARMIC2_BIAS_CONN

C4403 220PF 5% 10V C0G-CERM 01005 ROOM=RIGHT_BUTTON

FL4401 150OHM-25%-200MA-0.7DCR 01005 ROOM=RIGHT_BUTTON

REARMIC2_TO_CODEC_AIN3_P → REARMIC2_TO_CODEC_AIN3_CONN_P

C4404 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=RIGHT_BUTTON

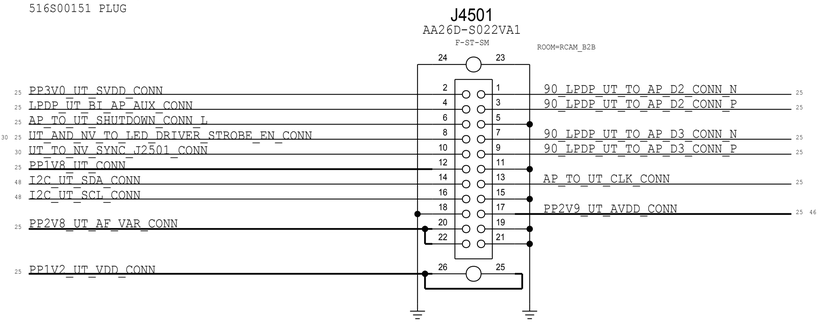
FL4402 150OHM-25%-200MA-0.7DCR 01005 ROOM=RIGHT_BUTTON

REARMIC2_TO_CODEC_AIN3_N → REARMIC2_TO_CODEC_AIN3_CONN_N

C4405 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=RIGHT_BUTTON

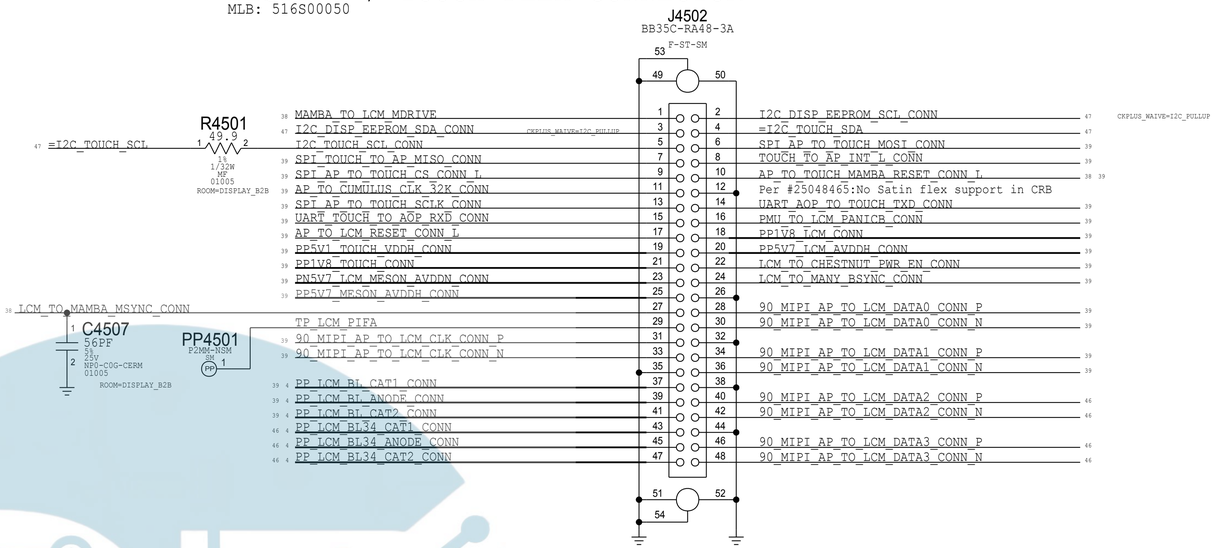
UTAH-D FLEX CONNECTOR

516S00152 RCPT (USED ON MLB) <-- THIS ONE
516S00151 PLUG



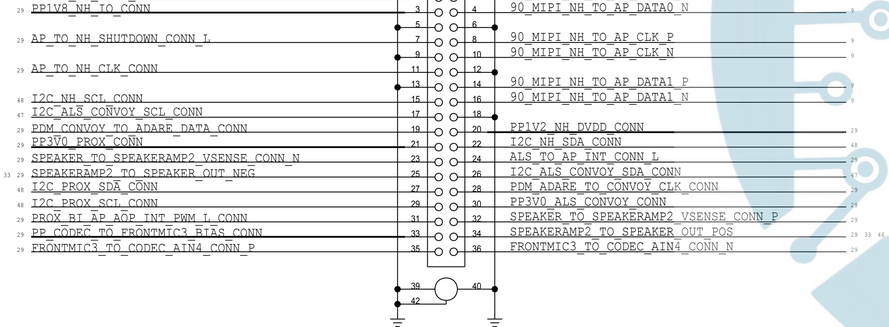
DISPLAY / TOUCH FLEX CONNECTOR

MLB: 516S00050



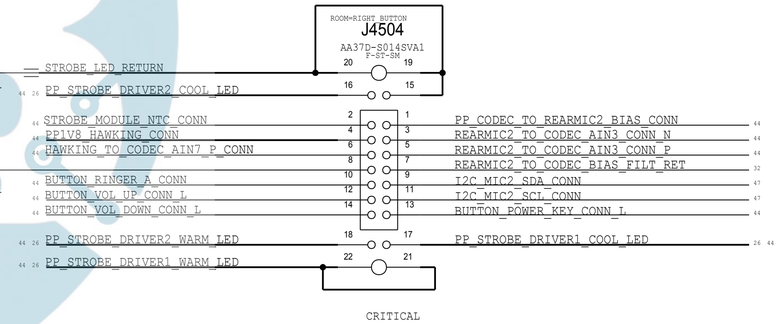
FOREHEAD FLEX CONNECTOR

MLB: 516S00146 (MCO REV 27)



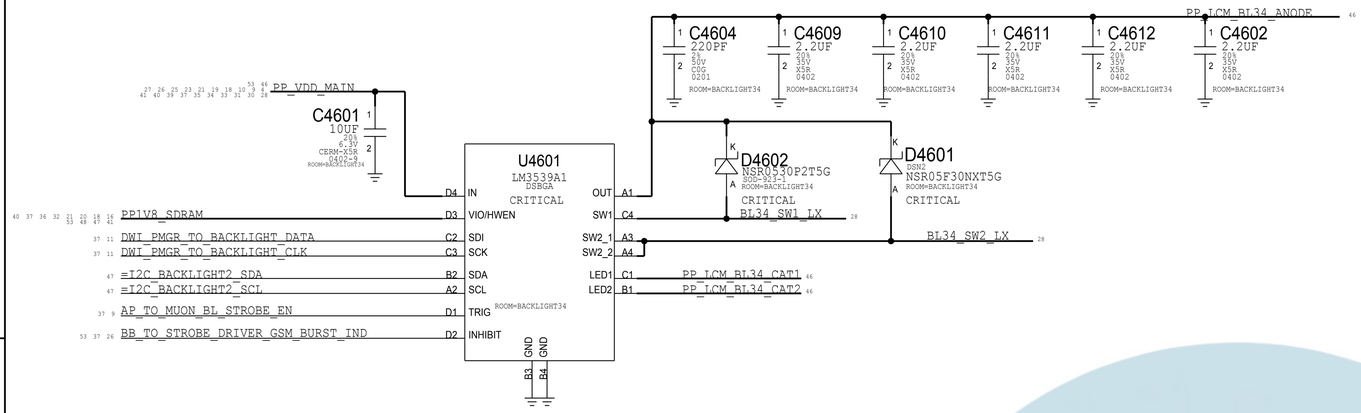
COMBO BUTTON FLEX CONNECTOR

APPLE APN: 516S00150 <-- THIS ONE ON MLB (matched MCO rev 27)
APPLE APN: 516S00149

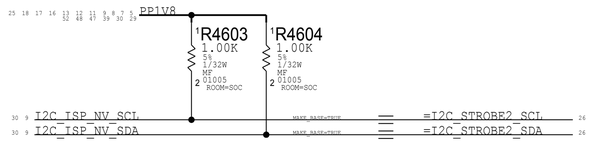


THIS PAGE UNIQUE TO LARGE FORM FACTOR

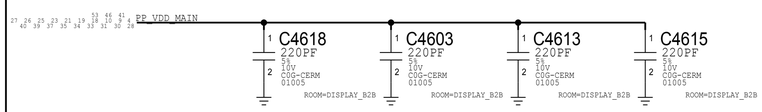
2ND BACKLIGHT DRIVER - 4LED



ISP I2C1

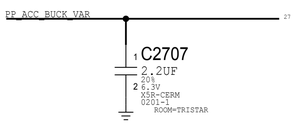


AC Coupling Caps

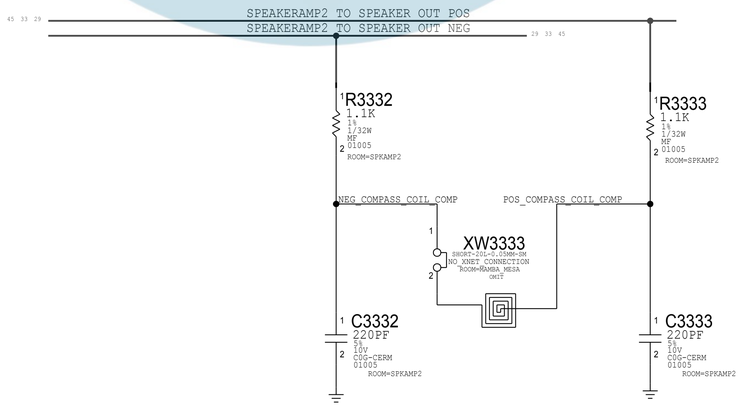


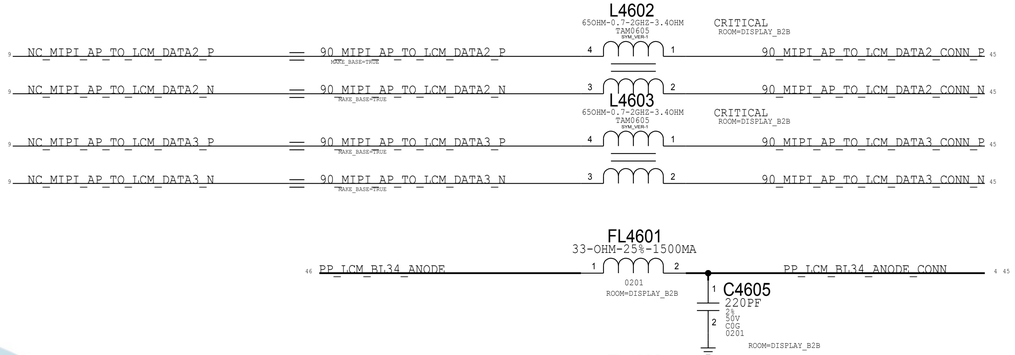
AC return path for LCM MIPI which is referenced to GND and VDD_MAIN

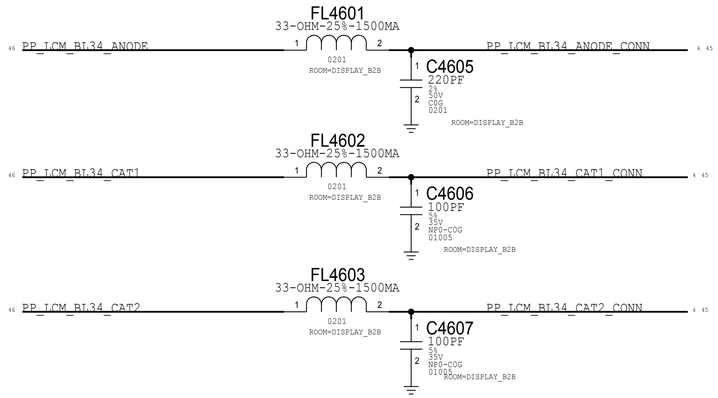
ACC Buck Caps



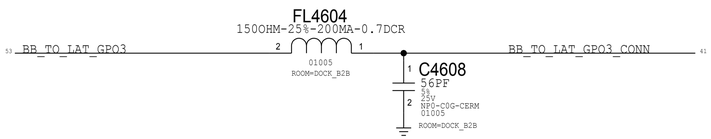
Top Speaker Compass Coil





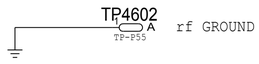


Dock B2B (Pg 41)



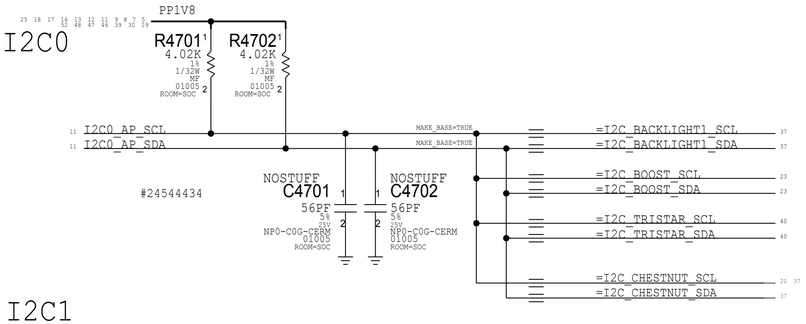
UT B2B

Extra RF GND

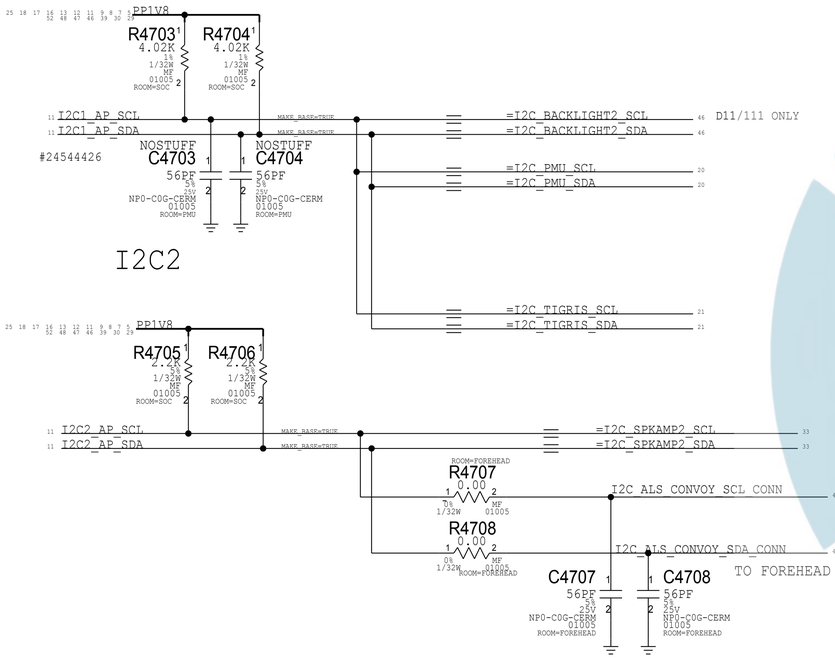


AP

I2C0

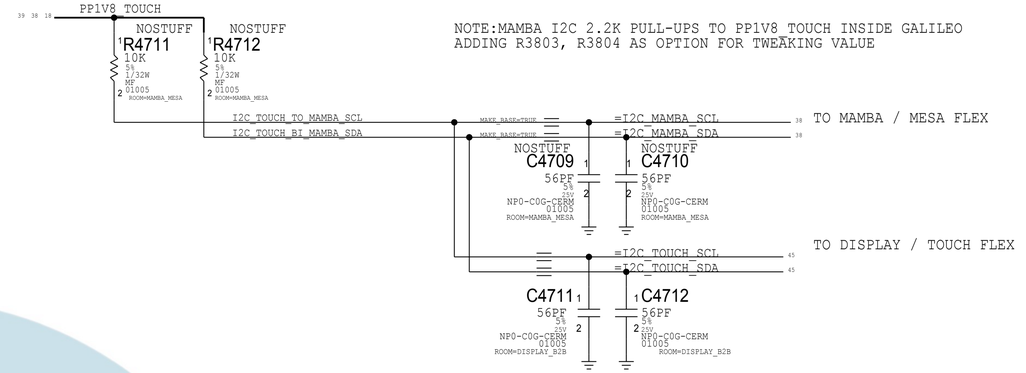


I2C1

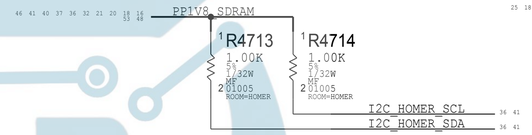


I2C2

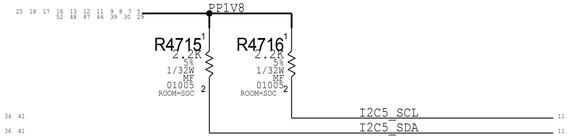
TOUCH



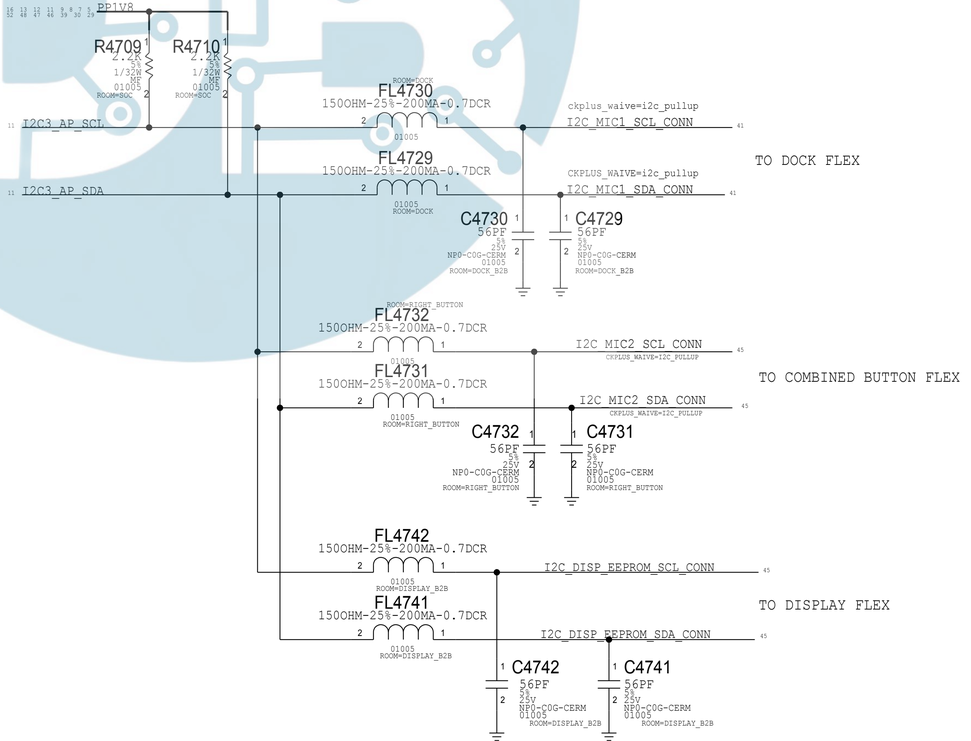
HOMER



I2C5



I2C3



AOP

I2C

PP1V8_SDRAM

R4801 2.2K 5% 1/32W MF 01005

R4802 2.2K 5% 1/32W MF 01005

C4807 0.1UF 20% 6.3V X5S-CERM 01005 ROOM=SOC

U4802 MAX20312 WLP ROOM=SOC

VCC B1

IOVCC1 A2

IOVCC2 B2

GND A1

#24544699: Support 1MHz

I2C_AOP_SCL MAKE_BASE=TRUE

I2C_AOP_SDA MAKE_BASE=TRUE

=I2C_SPKAMP1_SCL

=I2C_SPKAMP1_SDA

=I2C_ARC1_SCL

=I2C_ARC1_SDA

FL4815 1500HM-25%-200MA-0.7DCR 01005 ROOM=FOREHEAD

TO FCAM FLEX

I2C_PROX_SCL_CONN CKPLUS_WAIVE=I2C_PULLUP

I2C_PROX_SDA_CONN CKPLUS_WAIVE=I2C_PULLUP

#24958320:Intentional R4815 Change
Reduce undershoot when Prox Driving

R4815 33.2 1% 1/32W MF 01005 ROOM=FOREHEAD

Intentional R4815 Change

C4803 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=FOREHEAD

C4804 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=FOREHEAD

PP1V8_MESA

PP1V8_SDRAM

U4805 74LVC1G3157GX X2SON6 VCC GND S Z Y0 Y1 NC

R4803 4.7K 1% 1/32W MF 01005 ROOM=MAMBA_MESA

R4804 4.7K 1% 1/32W MF 01005 ROOM=MAMBA_MESA

I2C_AOP_SCL_ISO

R4806 0.00 0% 1/32W MF 01005 ROOM=MAMBA_MESA

I2C_MESA_TURTLE_SCL_CONN

C4809 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

AOP_TO_MESA_I2C_ISO_EN

R4805 511K 1% 1/32W MF 01005

PP1V8_SDRAM

U4806 74LVC1G3157GX X2SON6 VCC GND S Z Y0 Y1 NC

I2C_AOP_SDA_ISO

R4807 0.00 0% 1/32W MF 01005 ROOM=MAMBA_MESA

I2C_MESA_TURTLE_SDA_CONN

C4810 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=MAMBA_MESA

TO MAMBA/MESA FLEX

ISP

I2C0

PP1V8

#24550735: ISP I2C0 PU

R4808 1.00K 5% 1/32W MF 01005 ROOM=SOC

R4809 1.00K 5% 1/32W MF 01005 ROOM=SOC

I2C_ISP_UT_SCL MAKE_BASE=TRUE

I2C_ISP_UT_SDA MAKE_BASE=TRUE

=I2C_STROBE1_SCL

=I2C_STROBE1_SDA

I2C1

See page 46

I2C2

PP1V8

R4810 2.2K 5% 1/32W MF 01005 ROOM=SOC

R4811 2.2K 5% 1/32W MF 01005 ROOM=SOC

I2C_ISP_NH_SCL MAKE_BASE=TRUE

I2C_ISP_NH_SDA MAKE_BASE=TRUE

R4816 0.00 0% 1/32W MF 01005 ROOM=RCAM_B2B

C4817 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=RCAM_B2B

I2C_UT_SCL_CONN CKPLUS_WAIVE=I2C_PULLUP

R4817 0.00 0% 1/32W MF 01005 ROOM=RCAM_B2B

C4816 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=RCAM_B2B

I2C_UT_SDA_CONN CKPLUS_WAIVE=I2C_PULLUP

R4812 0.00 0% 1/32W MF 01005 ROOM=FOREHEAD

C4812 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=FOREHEAD

I2C_NH_SCL_CONN CKPLUS_WAIVE=I2C_PULLUP

R4813 0.00 0% 1/32W MF 01005 ROOM=FOREHEAD

C4813 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=FOREHEAD

I2C_NH_SDA_CONN CKPLUS_WAIVE=I2C_PULLUP

D1x I2C Table

Bus	Device	Binary	7-bit Address	8-bit Address	Max Speed
ISP I2C0 *1MHz*	SALT LAKE (PRIMARY)	0010000X	0x10	0x20	1 MHz
	SALT LAKE (SECONDARY)	0110000X	0x30	0x60	1 MHz
	GRUNBERG (STANDARD)	0011100X	0x1C	0x38	1 MHz
	GRUNBERG (SPECIAL ABSOLUTE R/W)	0011101X	0x1D	0x3A	1 MHz
	GRUNBERG (SPECIAL DELTA READ)	0011110X	0x1E	0x3C	1 MHz
	STROBE 1	1100011X	0x63	0xC6	1 MHz
ISP I2C1 *1MHz*	LAS VEGAS (PRIMARY)	0100000X	0x20	0x40	1 MHz
	LAS VEGAS (SECONDARY)	0110000X	0x30	0x60	1 MHz
	EDWIN	1100011X	0x63	0xC6	400 kHz
	STROBE 2	0000110X	0x06	0x0C	1 MHz
ISP I2C2 *400kHz*	CONCORD	0010000X	0x10	0x20	1 MHz
AOP I2C *1MHz*	ARC DRIVER 1	100000YX	0x41	0x82	1 MHz
	PROX	1011000X	0x58	0xB0	1 MHz
	SPKAMP1 (L26)	100000YX	0x40	0x80	1 MHz
	TURTLE	0101100X	0x2c	0x58	400 kHz
	MESA	1100001X	0x61	0xC2	400 kHz
Touch I2C *600kHz*	MAMBA	1100000X	0x60	0xC0	1 MHz
	MESON	1000000X	0x40	0x80	510 kHz
EEPROM I2C	EEPROM	1010001X	0x51	0xA2	400 kHz
AP I2C0 *400kHz*	BOOST	1110101X	0x75	0xEA	3.4 MHz
	TRISTAR	0011010X	0x1A	0x34	400 kHz
	BACKLIGHT 1	1100010X	0x62	0xC4	1 MHz
	CHESTNUT	0100111X	0x27	0x4E	400 kHz
AP I2C1 *400kHz*	ADELYN	1110100X	0x74	0xE8	400 kHz
	TIGRIS	1110101X	0x75	0xEA	400 kHz
	BACKLIGHT 2	1100010X	0x62	0xC4	1 MHz
AP I2C2 *400kHz*	ALS	0101001X	0x29	0x52	400 kHz
	CONVOY	0100001X	0x21	0x42	3.4 MHz
		0100010X	0x22	0x44	400 kHz
	SPKAMP 2 (L26)	10000ZYX	0x40	0x80	400 MHz
AP I2C3 *100kHz*	DOCK FLEX (MIC1)	1010100X	0x54	0xA8	1 MHz
	COMBINED BUTTON FLEX (MIC2)	1010100X	0x56	0xAC	1 MHz
	DISP EEPROM	1010001X	0x51	0xA2	400kHz
Homer I2C *1MHz*	SCHRODINGER (STANDARD)	0001110X	0xE	0x1C	1 MHz
	SCHRODINGER (CAL REG'S)	0001111X	0xF	0x1D	1 MHz
	EEPROM (STANDARD)	1010000X	0x50	0xA0	
	EEPROM (CONFIG)	1010000X	0x50	0xA0	

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

This page controls elements different accross all MLBs

PCIe Lanes

8 90_AP_PCIE2_RXD_C_P — C0816 1 2 0.1UF ROOM=SOC 20% 6.3V X5R-CERM 01005 GND_VCC=TRUE — 90_PCIE_WLAN_TO_AP_RXD_P 53 MAKE_BASE=TRUE

8 90_AP_PCIE2_RXD_C_N — C0817 1 2 0.1UF ROOM=SOC 20% 6.3V X5R-CERM 01005 GND_VCC=TRUE — 90_PCIE_WLAN_TO_AP_RXD_N 53 MAKE_BASE=TRUE

8 90_AP_PCIE2_TXD_C_P — C0815 1 2 0.1UF ROOM=SOC 20% 6.3V X5R-CERM 01005 GND_VCC=TRUE — 90_PCIE_AP_TO_WLAN_TXD_P 53 MAKE_BASE=TRUE

8 90_AP_PCIE2_TXD_C_N — C0818 1 2 0.1UF ROOM=SOC 20% 6.3V X5R-CERM 01005 GND_VCC=TRUE — 90_PCIE_AP_TO_WLAN_TXD_N 53 MAKE_BASE=TRUE

25 18 17 16 13 12 11 9 8 7 5 48 47 46 39 30 29 PP1V8 — R0807 1 100K 5% 1/32W MF 01005 2 ROOM=SOC

53 52 PCIE_WLAN_BI_AP_CLKREQ_L

8 90_AP_PCIE3_RXD_C_P — C0811 1 2 0.1UF ROOM=SOC 20% 6.3V X5R-CERM 01005 GND_VCC=TRUE — 90_PCIE_BB_TO_AP_RXD_P 53 MAKE_BASE=TRUE

8 90_AP_PCIE3_RXD_C_N — C0812 1 2 0.1UF ROOM=SOC 20% 6.3V X5R-CERM 01005 GND_VCC=TRUE — 90_PCIE_BB_TO_AP_RXD_N 53 MAKE_BASE=TRUE

8 90_AP_PCIE3_TXD_C_P — C0814 1 2 0.1UF ROOM=SOC 20% 6.3V X5R-CERM 01005 GND_VCC=TRUE — 90_PCIE_AP_TO_BB_TXD_P 53 MAKE_BASE=TRUE

8 90_AP_PCIE3_TXD_C_N — C0813 1 2 0.1UF ROOM=SOC 20% 6.3V X5R-CERM 01005 GND_VCC=TRUE — 90_PCIE_AP_TO_BB_TXD_N 53 MAKE_BASE=TRUE

8 90_AP_PCIE3_REFCLK_P — 90_PCIE_AP_TO_BB_REFCLK_P 53 MAKE_BASE=TRUE

8 90_AP_PCIE3_REFCLK_N — 90_PCIE_AP_TO_BB_REFCLK_N 53 MAKE_BASE=TRUE

8 90_AP_PCIE2_REFCLK_P — 90_PCIE_AP_TO_WLAN_REFCLK_P 53 MAKE_BASE=TRUE

8 90_AP_PCIE2_REFCLK_N — 90_PCIE_AP_TO_WLAN_REFCLK_N 53 MAKE_BASE=TRUE

8 AP_PCIE_RESET3_L — PCIE_AP_TO_BB_RESET_L 53 MAKE_BASE=TRUE

8 AP_PCIE_RESET2_L — PCIE_AP_TO_WLAN_RESET_L 53 MAKE_BASE=TRUE

8 AP_PCIE_CLKREQ3_L — PCIE_BB_BI_AP_CLKREQ_L 53 MAKE_BASE=TRUE

8 AP_PCIE_CLKREQ2_L — PCIE_WLAN_BI_AP_CLKREQ_L 52 53 MAKE_BASE=TRUE

Wifi/BT

I306

PP_VDD_MAIN
PP1V8_SDRAM
PMUGPIO_TO_WLAN_CLK32K
PMU_TO_WLAN_REG_ON
PMU_TO_BT_REG_ON
BT_TO_PMU_HOST_WAKE
AP_TO_BT_WAKE
90_PCIE_AP_TO_WLAN_REFCLK_P
90_PCIE_AP_TO_WLAN_REFCLK_N
90_PCIE_AP_TO_WLAN_TXD_P
90_PCIE_AP_TO_WLAN_TXD_N
90_PCIE_WLAN_TO_AP_RXD_P
90_PCIE_WLAN_TO_AP_RXD_N
PCIE_AP_TO_WLAN_RESET_L
PCIE_WLAN_BI_AP_CLKREQ_L
WLAN_TO_PMU_HOST_WAKE
AP_TO_WLAN_DEVICE_WAKE
UART_AP_TO_WLAN_TXD
UART_WLAN_TO_AP_RXD
UART_AP_TO_WLAN_RTS_L
UART_WLAN_TO_AP_CTS_L
UART_AP_TO_BT_TXD
UART_BT_TO_AP_RXD
UART_AP_TO_BT_RTS_L
UART_BT_TO_AP_CTS_L
AOP_TO_WLAN_CONTEXT_A
AOP_TO_WLAN_CONTEXT_B
I2S_AP_TO_BT_BCLK
I2S_AP_TO_BT_LRCLK
I2S_BT_TO_AP_DIN
I2S_AP_TO_BT_DOUT
UART_BB_TO_WLAN_COEX
UART_WLAN_TO_BB_COEX
50_UAT_WLAN_5G_WEST
50_UAT_WLAN_2G_EAST
50_UAT_WLAN_5G_EAST
50_WLAN_G_1
50_WLAN_A_1
50_UAT2_M

WIFI_MLB

Cellular

Aliases used to correct name for Karoo radio system

PP_VDD_MAIN
PP1V8_SDRAM
BBPMU_TO_PMU_AMUX1
BBPMU_TO_PMU_AMUX2
BBPMU_TO_PMU_AMUX3

Opposite polarity on Eureka -->
AP_TO_BBPMU_RADIO_ON_L
PMU_TO_BBPMU_RESET_L
Eureka names
NC_BB_TO_AP_RESET_ACT_L

MAKE_BASE=TRUE
AP_TO_BBPMU_SDWN_L
PMU_TO_BBPMU_ON
AP_TO_BB_RESET_L
BB_TO_AP_RESET_ACT_L
BB_TO_AP_RESET_DETECT_L
BB_TO_STROBE_DRIVER_GSM_BURST_IND
AP_TO_BB_MESA_ON
AP_TO_BB_TIME_MARK
AP_TO_BB_COREDUMP
AP_TO_BB_IPC_GPIO1
NC_AP_TO_BB_IPC_GPIO2
AP_TO_BB_IPC_GPIO2
90_PCIE_AP_TO_BB_REFCLK_P
90_PCIE_AP_TO_BB_REFCLK_N
90_PCIE_AP_TO_BB_TXD_P
90_PCIE_AP_TO_BB_TXD_N
90_PCIE_BB_TO_AP_RXD_P
90_PCIE_BB_TO_AP_RXD_N
PCIE_AP_TO_BB_RESET_L
PCIE_BB_BI_AP_CLKREQ_L
BB_TO_PMU_PCIE_HOST_WAKE_L
NC
UART_AP_TO_BB_TXD
UART_BB_TO_AP_RXD
UART_AOP_TO_BB_TXD
UART_BB_TO_AOP_RXD
I2S_BB_TO_AP_BCLK
I2S_BB_TO_AP_LRCLK
I2S_AP_TO_BB_DOUT
I2S_BB_TO_AP_DIN
UART_BB_TO_WLAN_COEX
UART_WLAN_TO_BB_COEX
SIM1_SWP
NFC_TO_BB_CLK_REQ
BB_TO_NFC_CLK
NC_PMU_TO_GNSS_EN
NC_AP_UART2_TXD
NC_AP_UART2_RXD
NC_AP_UART2_RTS_L
NC_AP_UART2_CTS_L
NC_GNSS_TO_PMU_HOST_WAKE
NC_AP_TO_GNSS_TIME_MARK
NC_AP_TO_GNSS_WAKE
PMU_TO_GNSS_EN
UART_AP_TO_GNSS_TXD
UART_GNSS_TO_AP_RXD
UART_AP_TO_GNSS_RTS_L
UART_GNSS_TO_AP_CTS_L
GNSS_TO_PMU_HOST_WAKE
AP_TO_GNSS_TIME_MARK
AP_TO_GNSS_WAKE
SWD_AP_TO_MANY_SWCLK
SWD_AOP_BI_BB_SWDIO
PMU_TO_BB_USB_VBUS_DETECT
90_USB_BB_DATA_P
90_USB_BB_DATA_N

RADIO_MLB

NFC

PP_VDD_MAIN
PP1V8_SDRAM
PMU_TO_NFC_EN
BB_TO_NFC_CLK
NFC_TO_BB_CLK_REQ
AP_TO_NFC_FW_DWLD_REQ
AP_TO_NFC_DEV_WAKE
NFC_TO_PMU_HOST_WAKE
UART_AP_TO_NFC_TXD
UART_NFC_TO_AP_RXD
UART_AP_TO_NFC_RTS_L
UART_NFC_TO_AP_CTS_L
SIM1_SWP
NC_SE2_READY
NC_SE2_PWR_REQ
NC_SE2_PRESENT
NC_NFC_SWP_MUX
NC_ICEFALL_LDO_ENABLE

STOCKHOLM_MLB

FF SPECIFIC

50_WLAN_A_1
50_WLAN_G_1
50_UAT_WLAN_5G_EAST
50_UAT_WLAN_2G_EAST
50_UAT_WLAN_5G_WEST
50_UAT2_M
PP_VDD_MAIN

RADIO_MLB_FF
50_WLAN_A_1
50_WLAN_G_1
50_UAT_WLAN_5G_EAST
50_UAT_WLAN_2G_EAST
50_UAT_WLAN_5G_WEST
50_UAT2_M
PP_VDD_MAIN
50_UAT_WLAN_2G_WEST
50_UAT_LB_NORTH
50_UAT_LB_SOUTH
50_UAT_MB_HB_SOUTH
50_UAT_MB_HB_WEST
50_UAT1_TUNER
PP3V0_TRISTAR
VDD_TUNER_RFFE_VIO_1V8
UAT_TUNER_RFFE_CLK
UAT_TUNER_RFFE_DATA
UAT_TUNER_GPO

P2MM-NSM SM ROOM=UAT_DEBUG
PP5304
PP5301
PP5302
PP5303

50_UAT_WLAN_2G_WEST
50_UAT_LB_NORTH
50_UAT_LB_SOUTH
50_UAT_MB_HB_SOUTH
50_UAT_MB_HB_WEST
50_UAT1_TUNER
PP3V0_TRISTAR_ANT_PROX
PP1V8_SDRAM
BB_TO_UAT_ANT_SCLK
BB_TO_UAT_ANT_DATA
BB_TO_UAT_TUNER_GPO

BB_TO_LAT_ANT_SCLK
BB_TO_LAT_ANT_DATA
BB_TO_UAT_TUNER_GPO
BB_TO_UAT_ANT_SCLK
BB_TO_UAT_ANT_DATA
BB_TO_LAT_GPO1
BB_TO_LAT_GPO2
BB_TO_LAT_GPO3

LAT_TUNER_RFFE_CLK
LAT_TUNER_RFFE_DATA
UAT_TUNER_GPO
UAT_TUNER_RFFE_CLK
UAT_TUNER_RFFE_DATA
LAT_TUNER_GPO1
LAT_TUNER_GPO2
LAT_TUNER_GPO3

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
5	0006232160	ENGINEERING RELEASED	2016-05-16

ICE16 RADIO MLB

Mon May 16 14:17:24 2016

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
197S00040	197S00044	VTCXO_RF	AVX VC-TCXO	?
197S00042	197S00044	VTCXO_RF	NDK VC-TCXO	?
197S00039	197S00043	GTCXO_RF	AVX VC-TCXO	?
197S00041	197S00043	GTCXO_RF	NDK VC-TCXO	?
335S00013	335S0894	EPROM_RF	ON SEMI EEPROM	?
138S0719	138S1103	C5820_RF	MURATA	?
138S0706	138S0739	C5811_RF, C5813_RF, C5815_RF, C5905_RF, C5913_RF	MURATA	?
138S0945	138S0739	C5811_RF, C5813_RF, C5815_RF, C5905_RF, C5913_RF	KYOCERA	?

BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
998-03730	1	BASEBAND, UNFUSED	BB_RF	BB_UNFUSED
998-03731	1	BASEBAND, LOCAL FUSED	BB_RF	BB_LOCAL_FUSED
998-03732	1	BASEBAND, DEV FUSED	BB_RF	BB_DEV_FUSED
337S00127	1	BASEBAND, PRODUCTION FUSED	BB_RF	BB_PROD_FUSED

SCH: 951-00673
BOM: 939-00555

RADIO MLB PORTS

POWER
- IN PP_VDD_MAIN
- IN PP1V8_SDRAM

AMUX
- OUT BBPMU_TO_PMU_AMUX1
- OUT BBPMU_TO_PMU_AMUX2
- OUT BBPMU_TO_PMU_AMUX3

BB CONTROL
- AP_TO_BBPMU_RADIO_ON_L
- PMU_TO_BBPMU_RESET_L
- IN AP_TO_BB_RESET_L
- OUT BB_TO_AP_RESET_ACT_L
- OUT BB_TO_AP_RESET_DETECT_L
- OUT BB_TO_AP_GSM_TXBURST
- IN AP_TO_BB_MESA_ON
- IN AP_TO_BB_TIME_MARK
- IN AP_TO_BB_COREDUMP_TRIG
- TOUCH_TO_BBPMU_FORCE_PWM
- IN AP_TO_BB_IPC_GPIO
- IN AP_TO_BB_IPC_GPIO2

AP_TO_BBPMU_SDWN_L — OUT
PMU_TO_BBPMU_ON — OUT

PCIE
- IN 100_PCIE_AP_TO_BB_REFCLK_P
- IN 100_PCIE_AP_TO_BB_REFCLK_N
- IN 100_PCIE_AP_TO_BB_TX_P
- IN 100_PCIE_AP_TO_BB_TX_N
- OUT 100_PCIE_BB_TO_AP_RX_P
- OUT 100_PCIE_BB_TO_AP_RX_N
- IN PCIE_AP_TO_BB_PERST_L
- IO PCIE_AP_BI_BB_CLKREQ_L
- OUT PCIE_BB_TO_PMU_WAKE_L
- AP_TO_BB_DEVICE_WAKE

UART
- IN UART_AP_TO_BB_TXD
- OUT UART_BB_TO_AP_RXD

AOP
- IN UART_AOP_TO_BB_TXD
- OUT UART_BB_TO_AOP_RXD

AUDIO
- IN I2S_AP_TO_BB_BCLK
- IN I2S_AP_TO_BB_LRCLK
- IN I2S_AP_TO_BB_DOUT
- OUT I2S_BB_TO_AP_DIN

WLAN
- IN UART_BB_TO_WLAN_COEX
- OUT UART_WLAN_TO_BB_COEX

NFC
- IO SIM1_SWP
- SIM2_SWP
- IN NFC_TO_BB_CLKREQ
- OUT BB_TO_NFC_CLK

GNSS
- IN PMU_TO_GNSS_EN
- IN UART_AP_TO_GNSS_TXD
- OUT UART_GNSS_TO_AP_RXD
- IN UART_AP_TO_GNSS_RTS_L
- OUT UART_GNSS_TO_AP_CTS_L
- OUT GNSS_TO_PMU_HOST_WAKE
- IN AP_TO_GNSS_TIME_MARK
- IN AP_TO_GNSS_DEVICE_WAKE

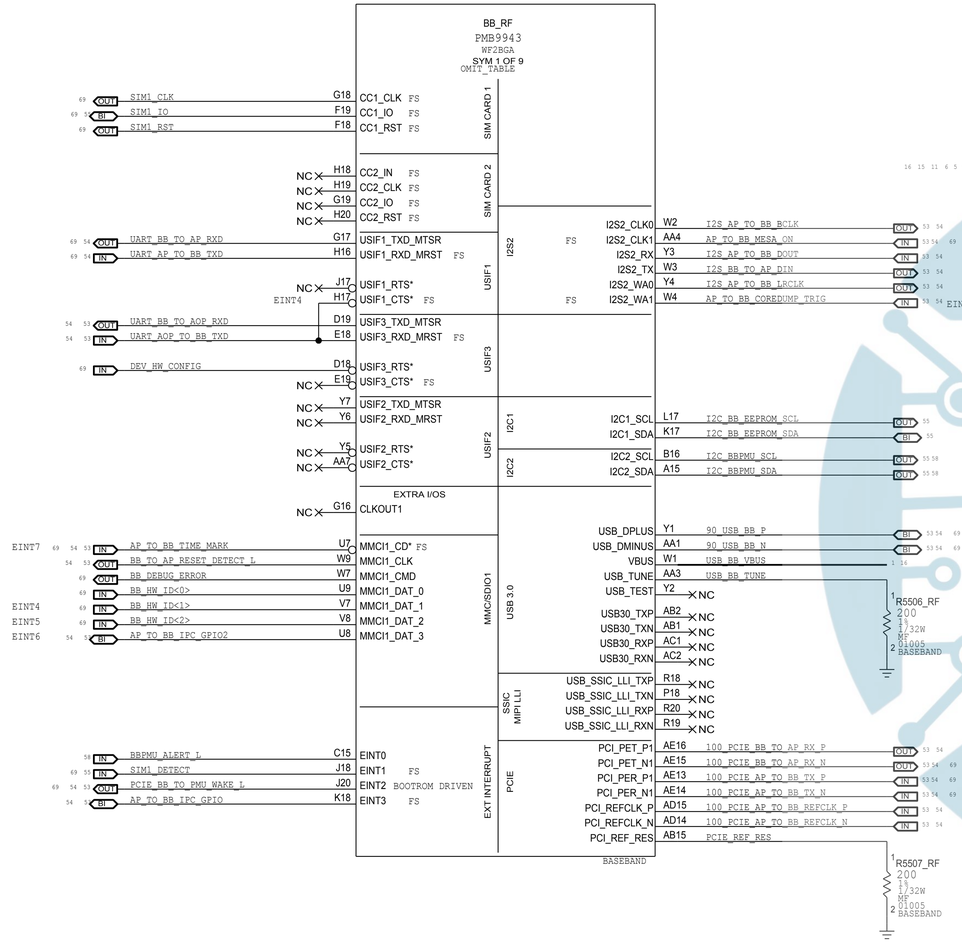
DEBUG
- IN SWD_AP_TO_BB_CLK
- IO SWD_AP_BI_BB_IO
- IN USB_BB_VBUS
- IO 90_USB_BB_P
- IO 90_USB_BB_N

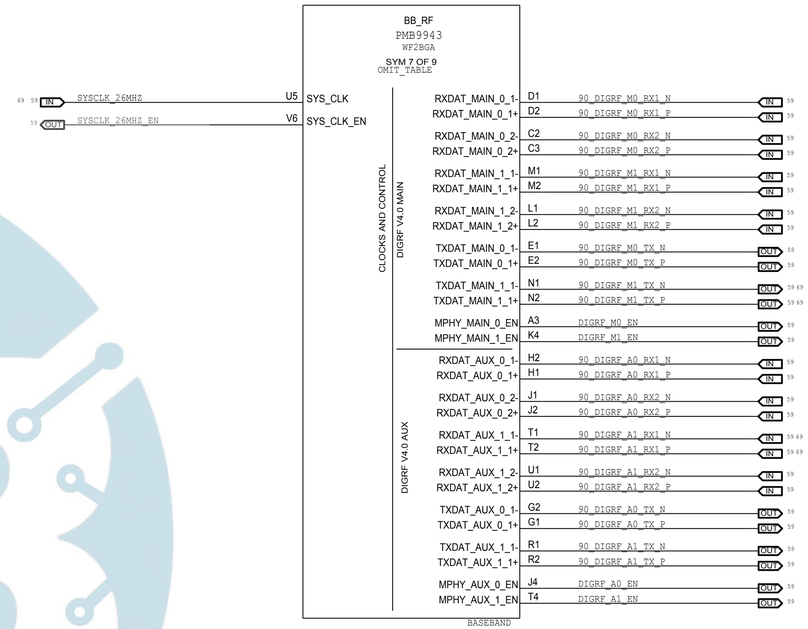
ANTENNA
- IO 50_UAT_WLAN_2G_WEST
- IO 50_UAT_LB_NORTH
- IO 50_UAT_LB_SOUTH
- IO 50_UAT_MB_HB_SOUTH
- IO 50_UAT_MB_HB_WEST
- IO 50_UAT1_TUNER

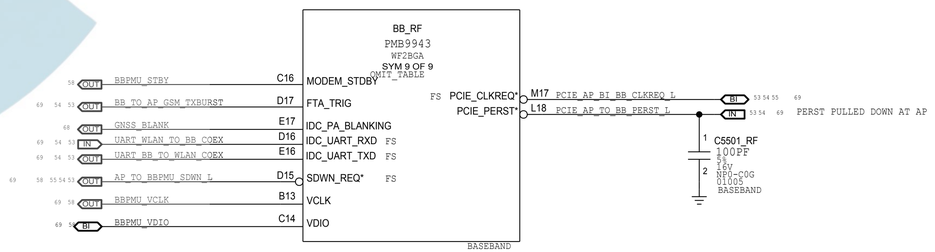
TUNER
- OUT LAT_TUNER_RFFE_CLK = RFFE1_CLK_FILT
- IO LAT_TUNER_RFFE_DATA = RFFE1_DATA_FILT
- OUT UAT_TUNER_GPO
- OUT UAT_TUNER_RFFE_CLK
- IO UAT_TUNER_RFFE_DATA

- OUT LAT_TUNER_GPO1
- OUT LAT_TUNER_GPO2
- OUT LAT_TUNER_GPO3

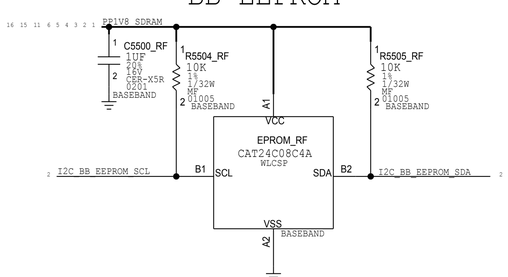
BASEBAND



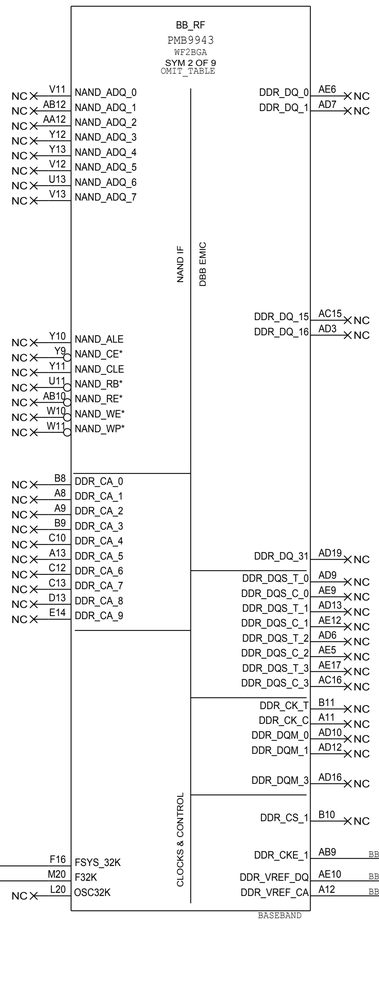


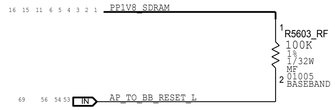


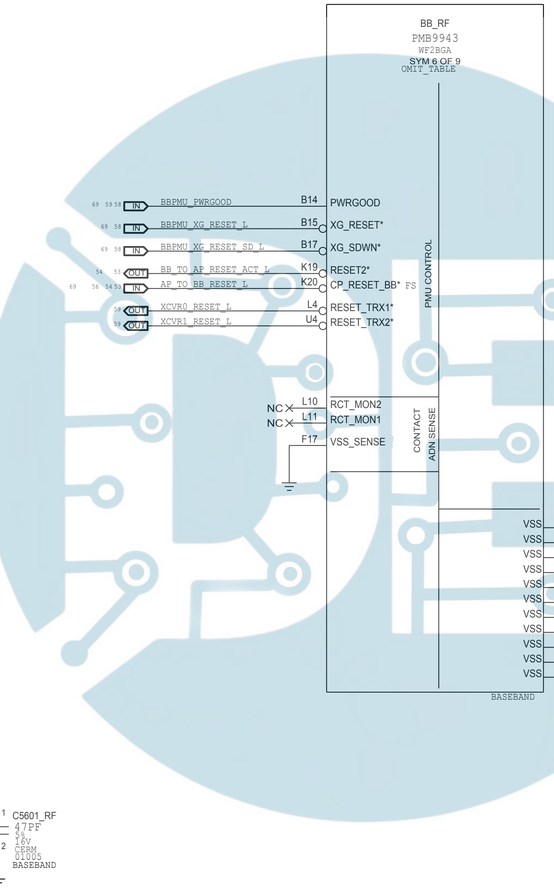
BB EEPROM

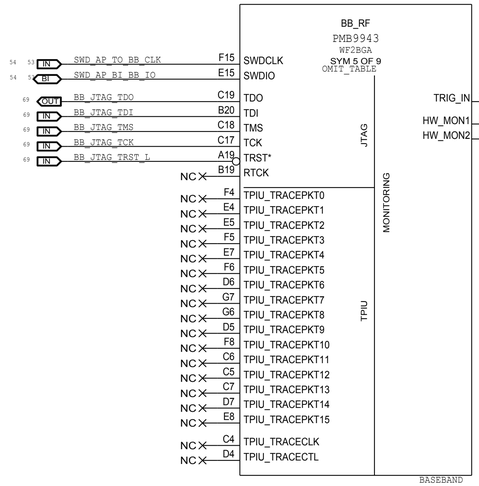


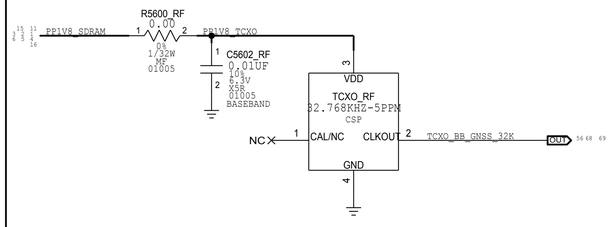
BASEBAND MEMORY/DEBUG

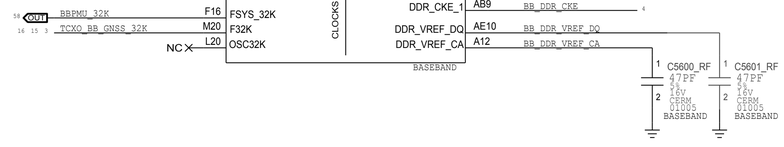




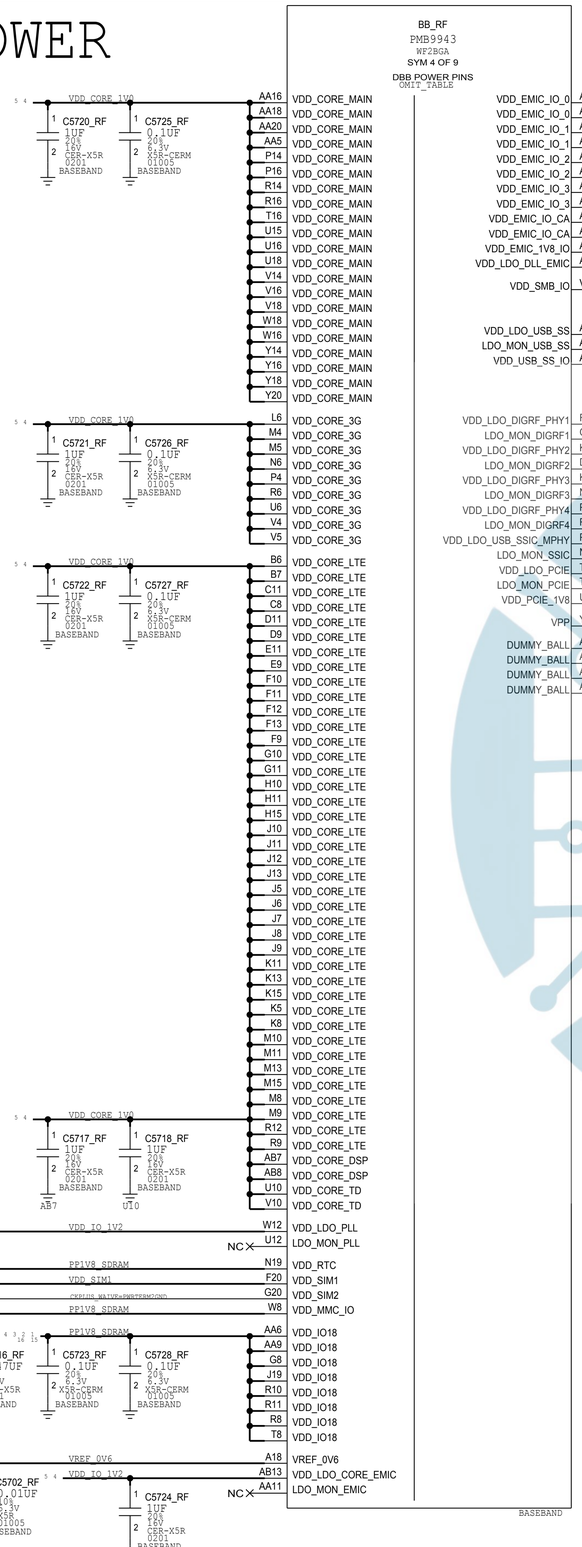


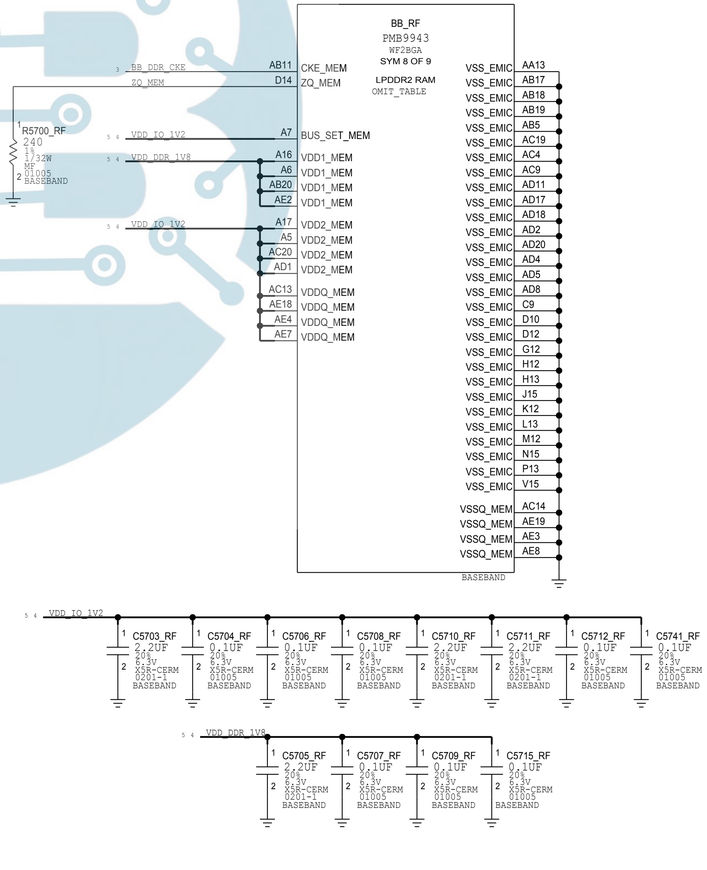


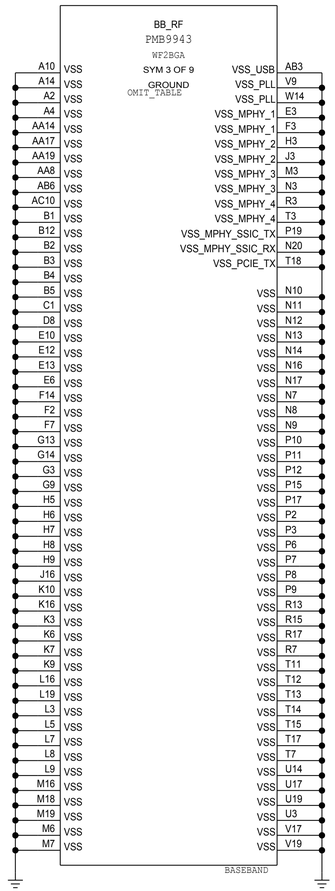




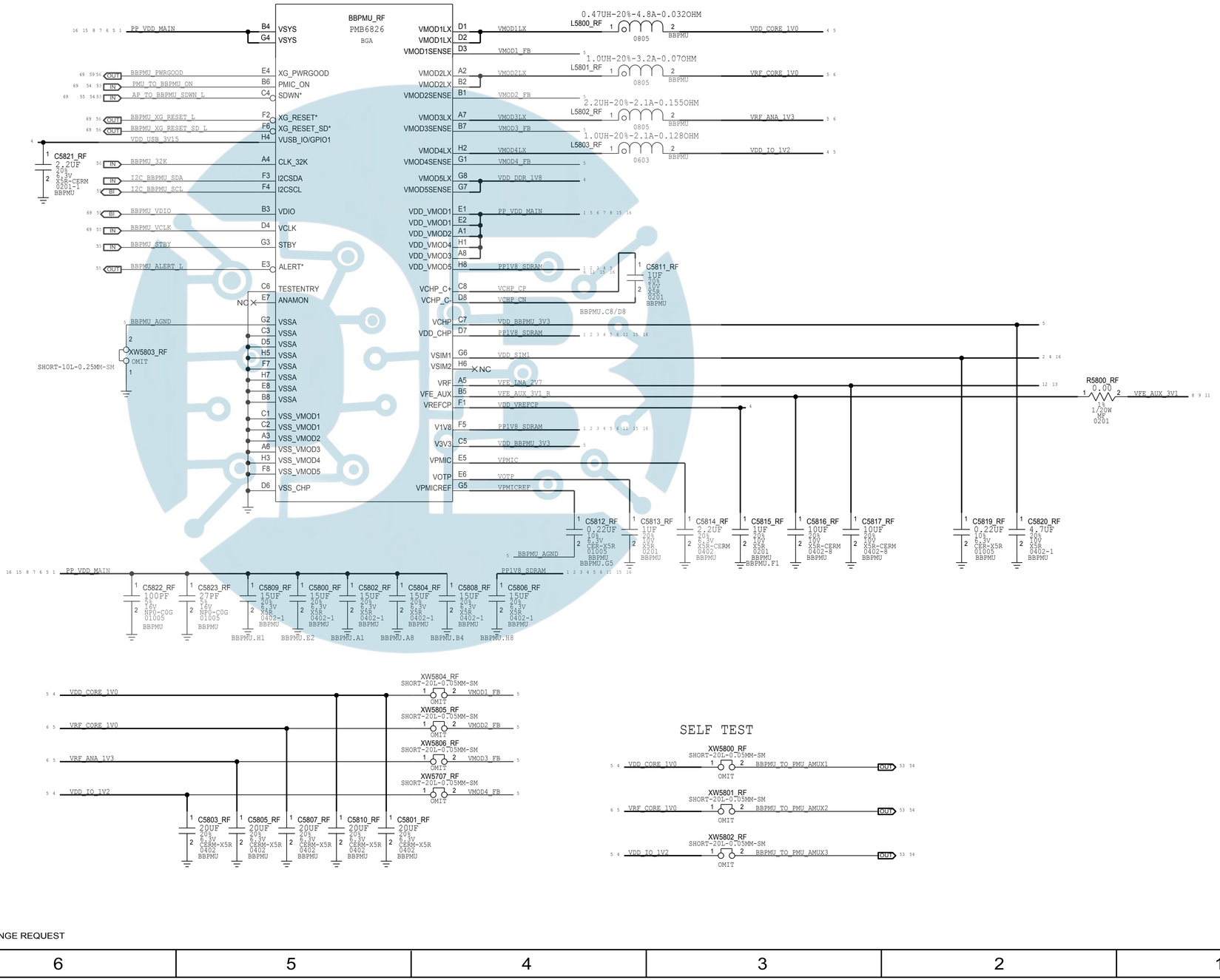
BASEBAND POWER



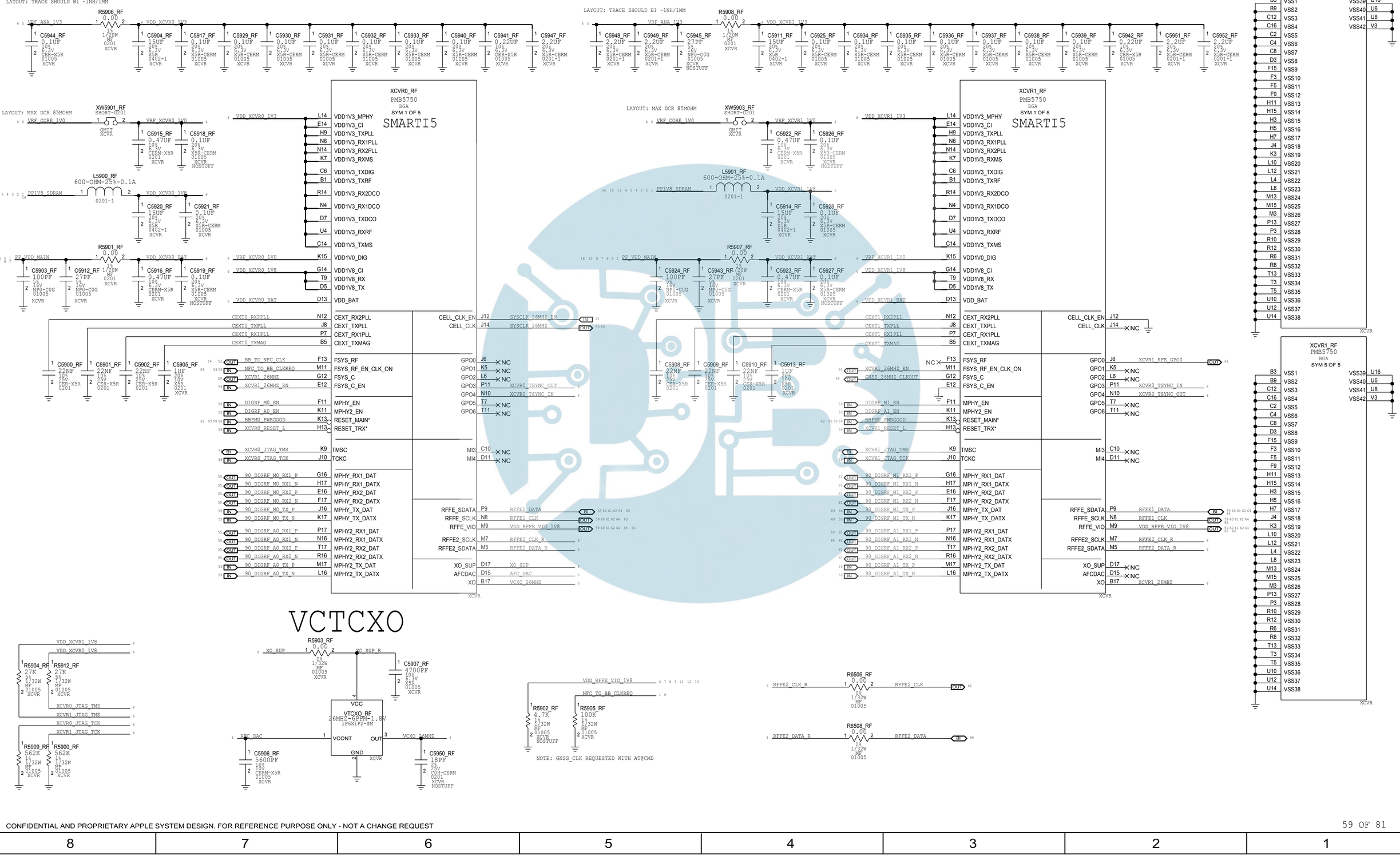




BASEBAND PMIC



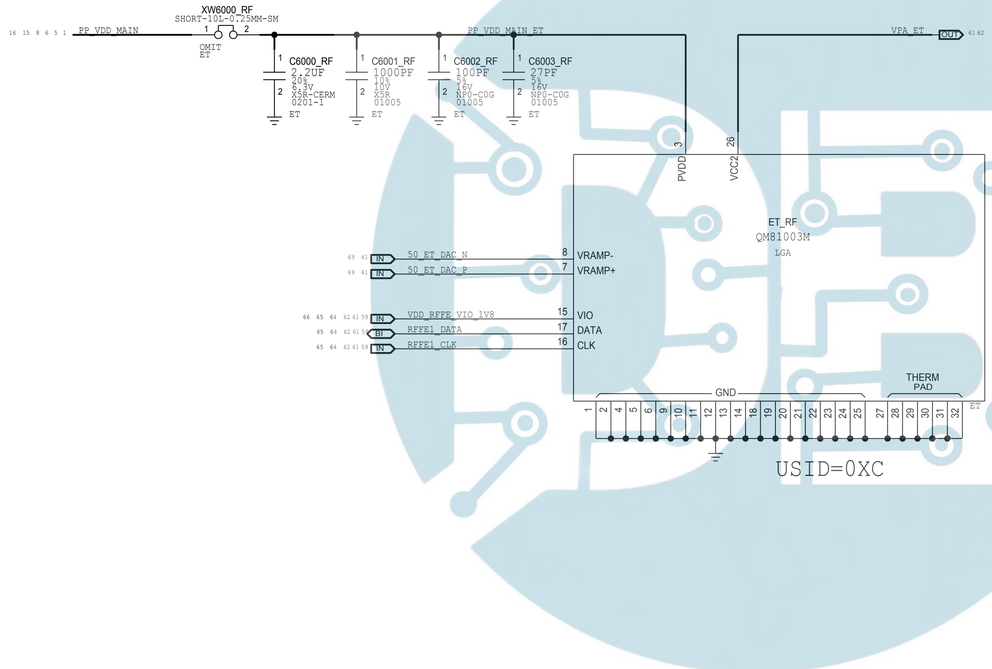
TRANSCEIVERS



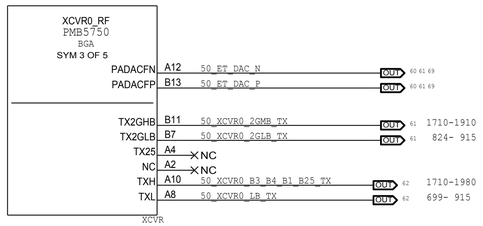
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE PURPOSE ONLY - NOT A CHANGE REQUEST

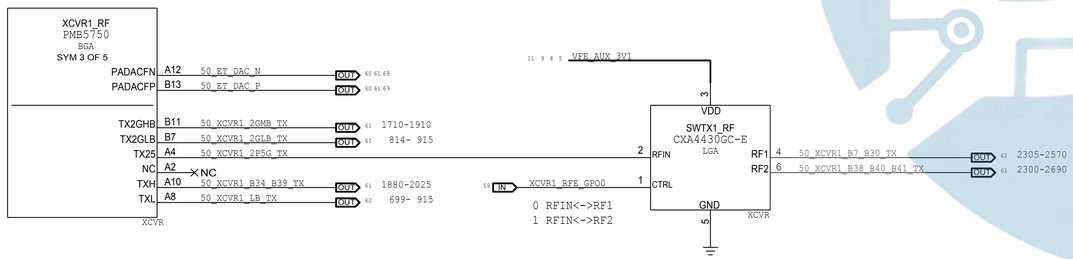
ET MODULATOR

ALPES II ES2

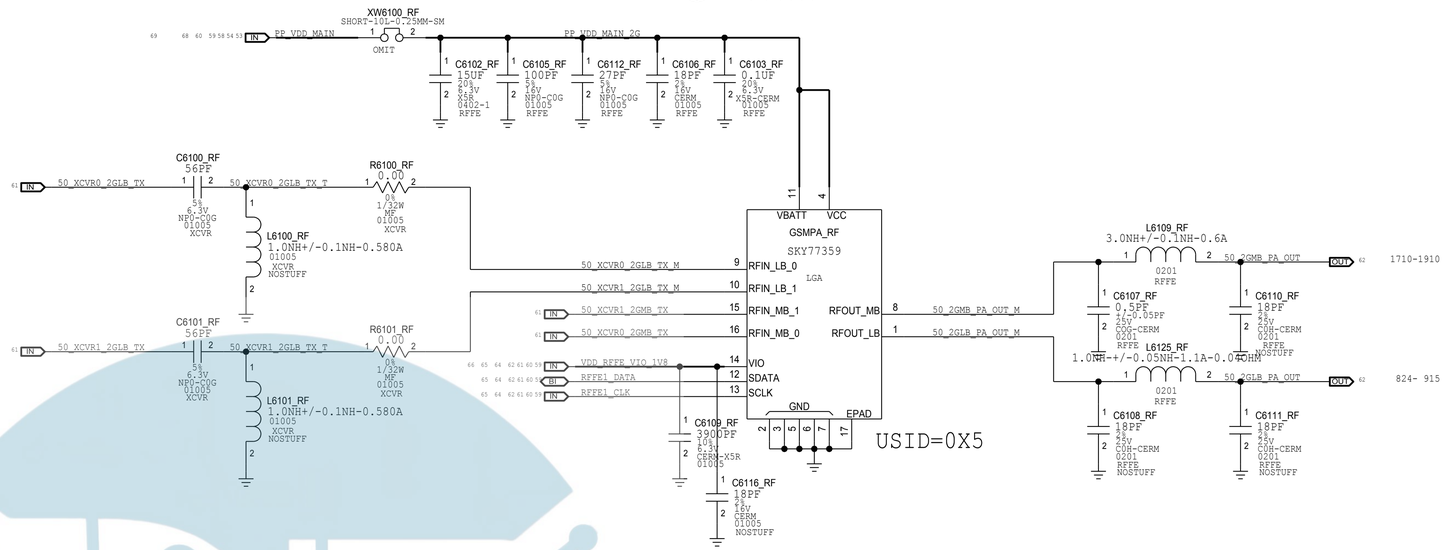


TDD TRANSMIT

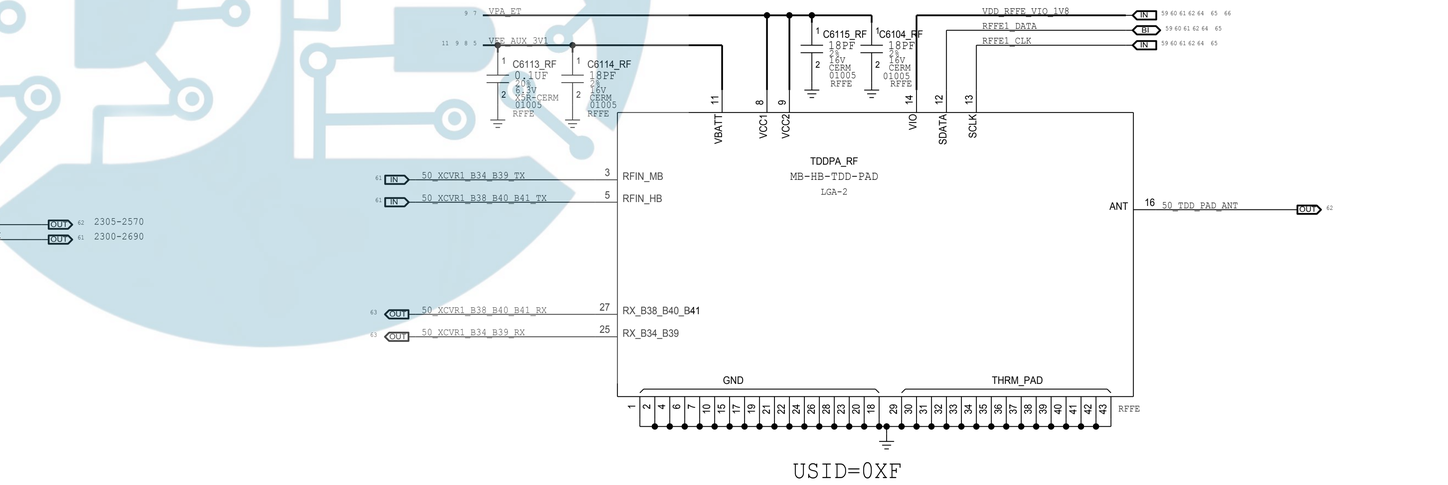




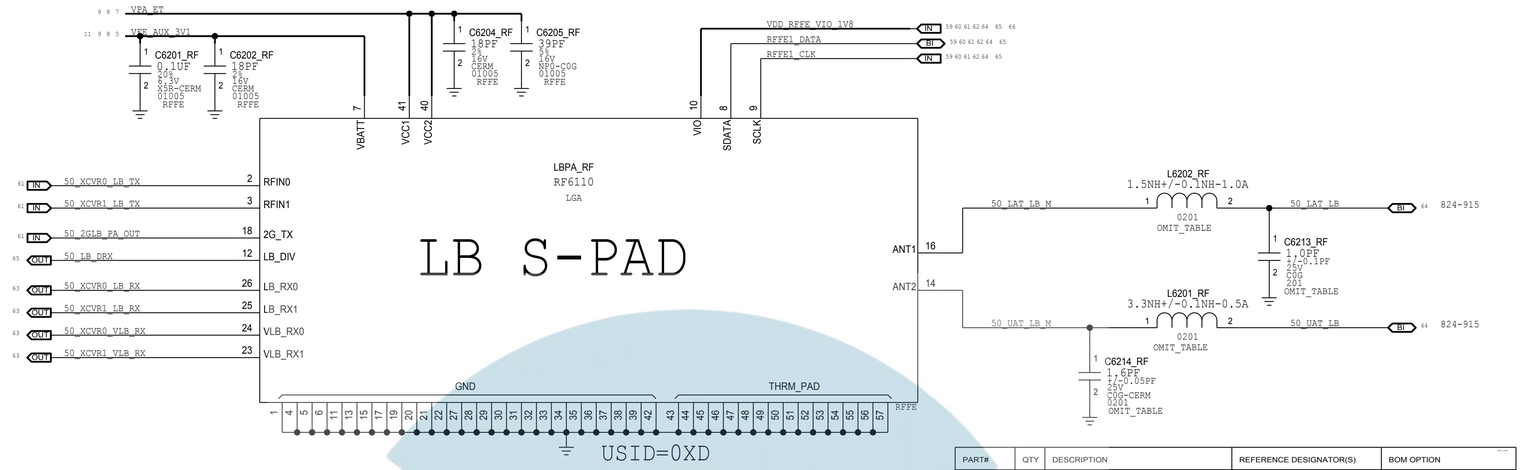
2G PA



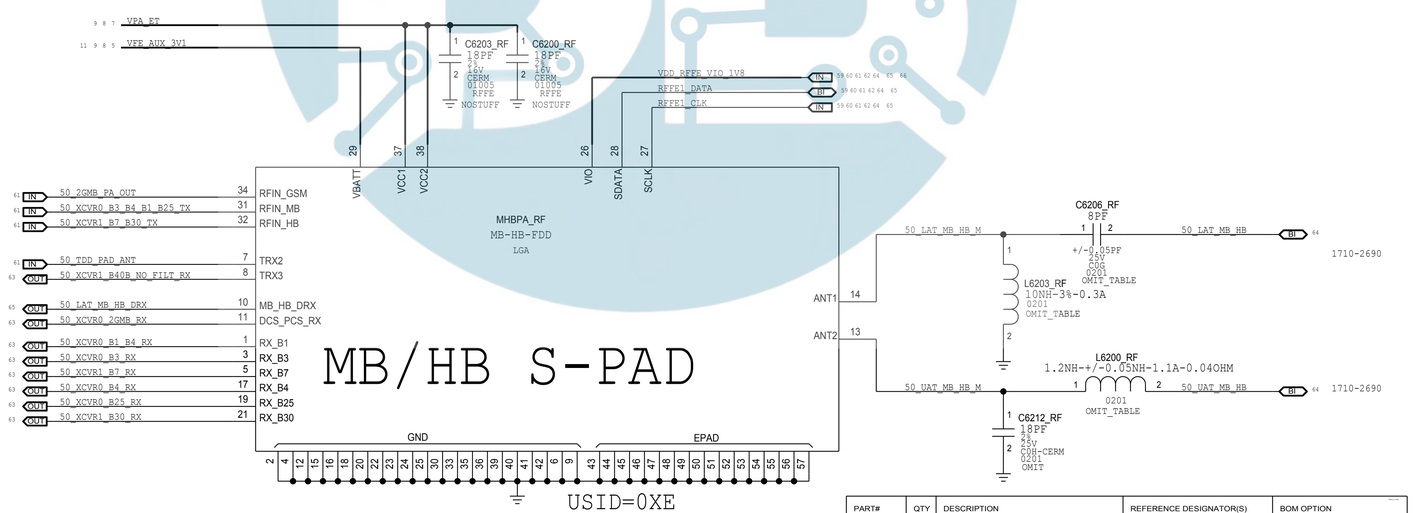
MB HB TDD S-PAD



FDD TRANSMIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S2021	1	IND, 1.5NH, 0201, UH-Q	L6202_RF	D101
131S0278	1	CAP, 1.0PF, 0201, HQ	C6213_RF	D101
152S2004	1	IND, 3.3NH, 0201, UH-Q	L6201_RF	D101
131S0338	1	CAP, 1.6PF, 0201, HF	C6214_RF	D101
152S00151	1	IND, 0.8NH, 0201, UH-Q	L6202_RF	D111
131S0312	1	CAP, 1.2PF, 0201, HQ	C6213_RF	D111
152S2002	1	IND, 2.7NH, 0201, UH-Q	L6201_RF	D111
131S0338	1	CAP, 1.6PF, 0201, HF	C6214_RF	D111



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
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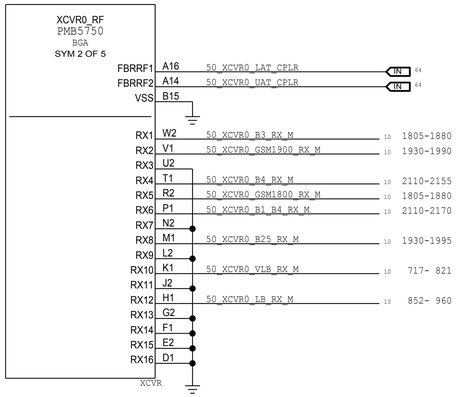
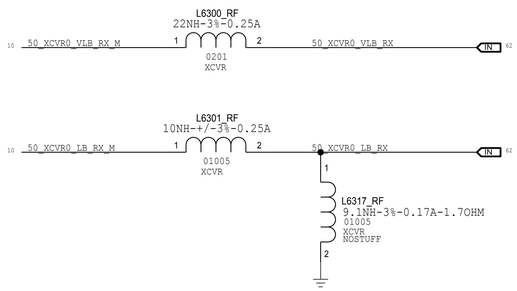
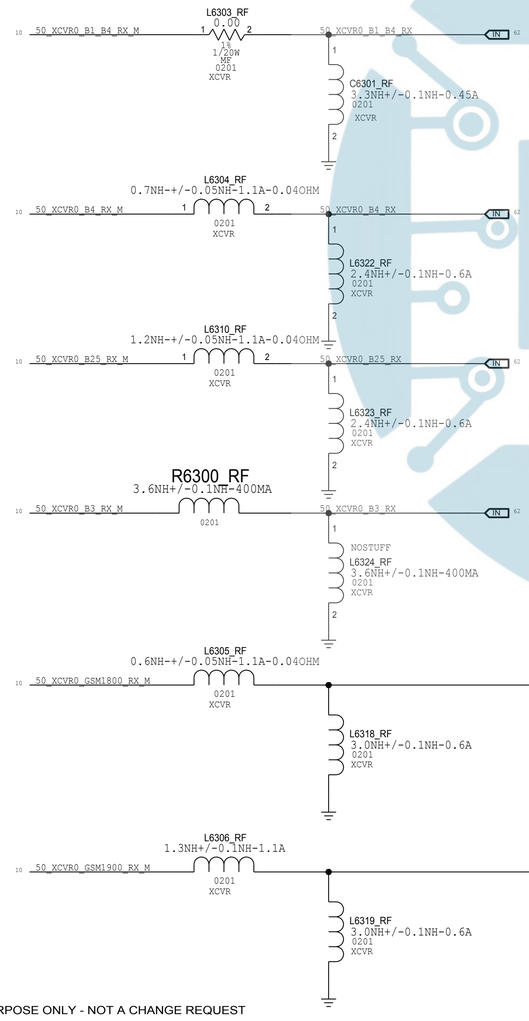
152S2041	1	IND, 10NH, 0201, UH-Q	L6203_RF	D101
152S00157	1	IND, 1.2NH, 0201, UH-Q	L6200_RF	D101
		NOSTUFF	C6212_RF	D101
131S00068	1	CAP, 8.0PF, 0201, HQ	C6206_RF	D111
152S00020	1	IND, 12NH, 0201, UH-Q	L6203_RF	D111
152S2021	1	IND, 1.5NH, 0201, UH-Q	L6200_RF	D111
		NOSTUFF	C6212_RF	D111

PRIMARY RECIEVE

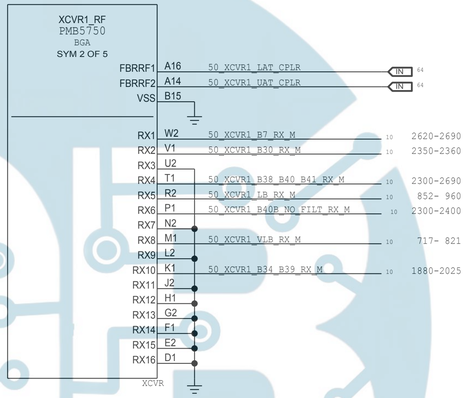
XCVR PRX

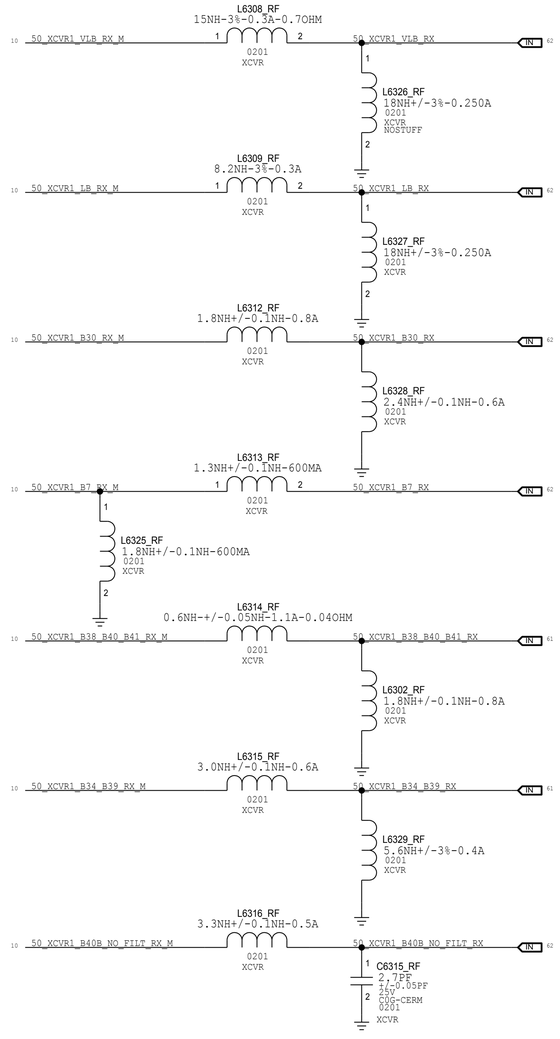






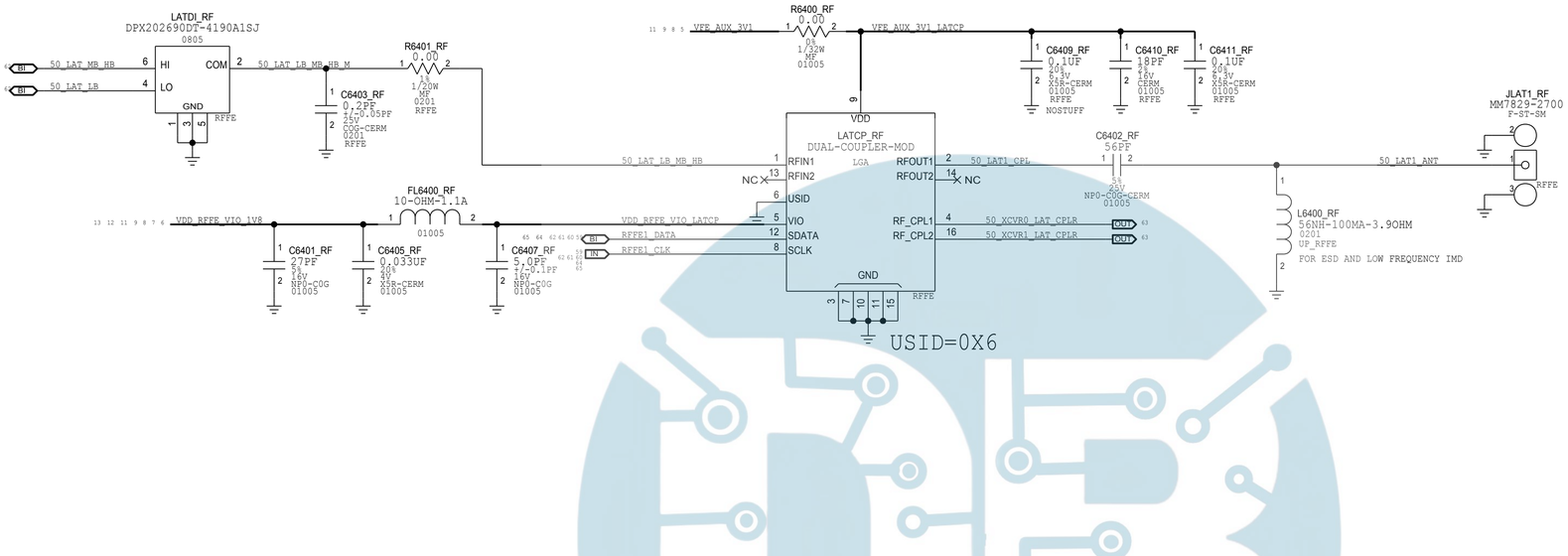
XCVR PRX



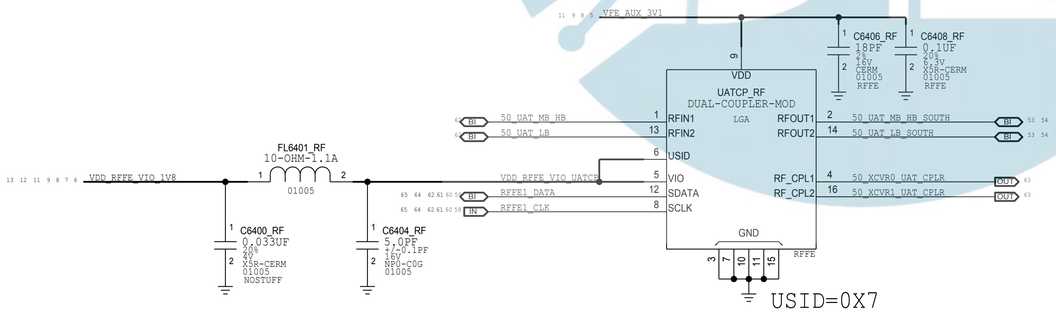


LOWER ANTENNA AND COUPLER

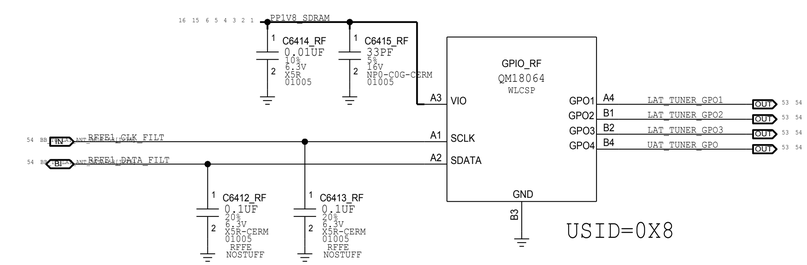
LOWER ANTENNA COUPLER



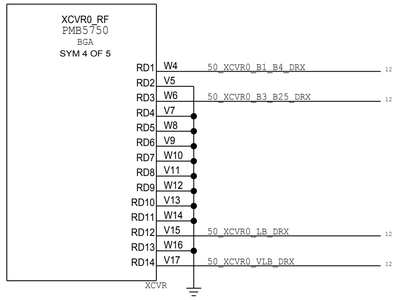
UPPER ANTENNA COUPLER

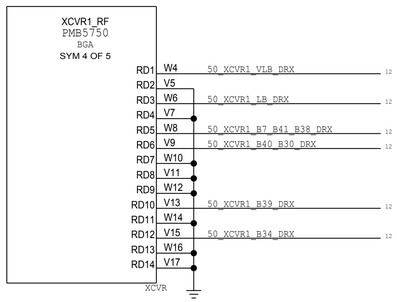


TUNER GPO

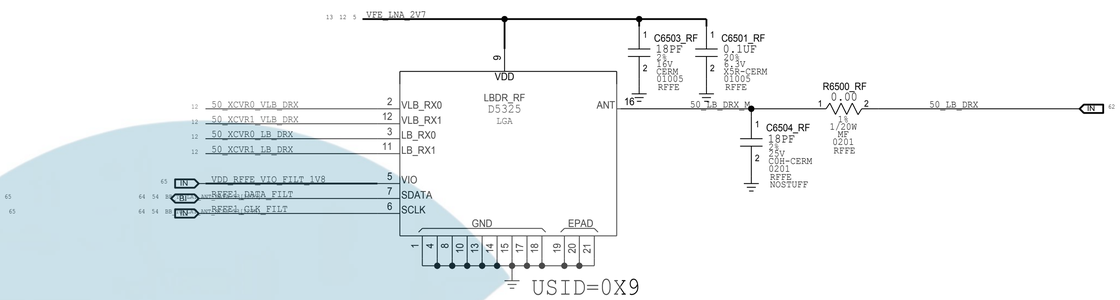


DIVERSITY RECEIVE ASM'S

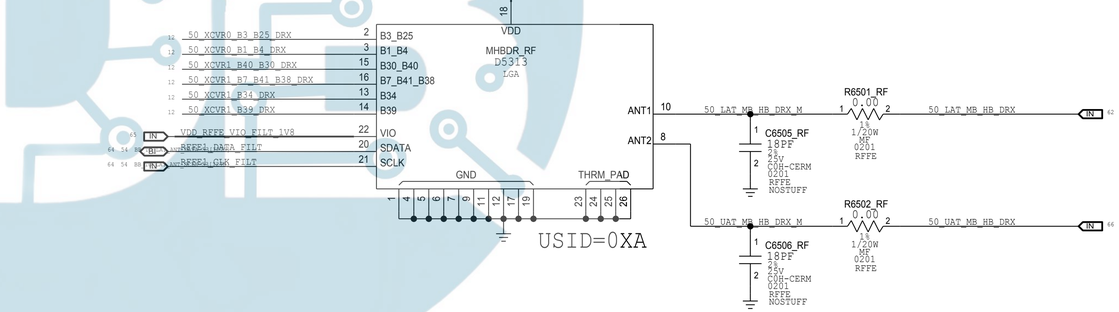




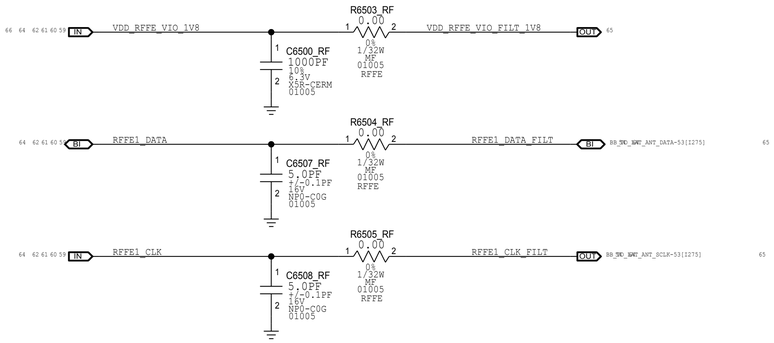
LB DRX ASM



MB HB DRX ASM

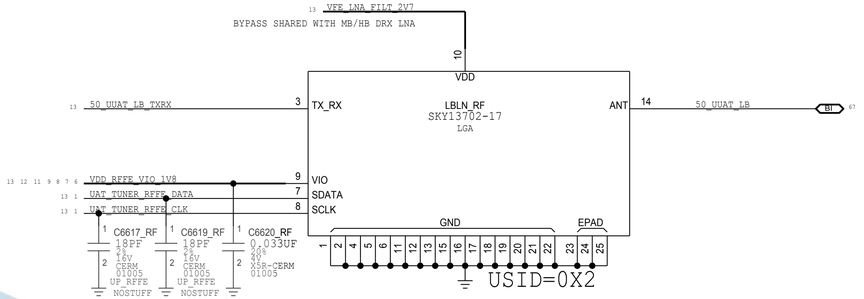


RFFE FILTERING

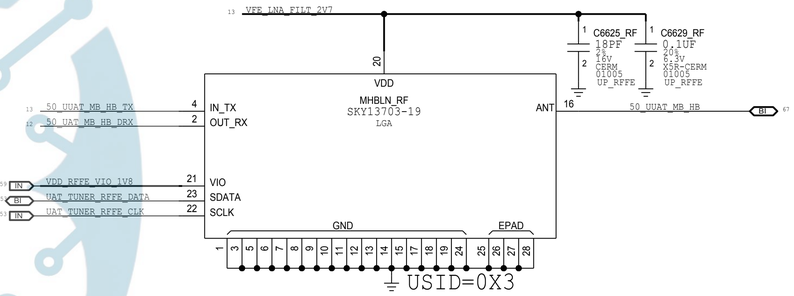


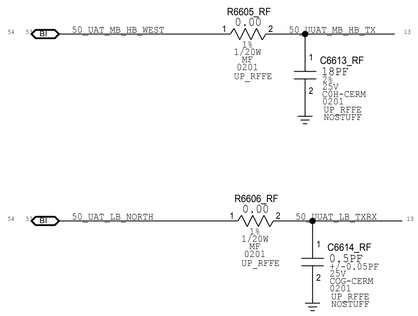
DIVERSITY RECEIVE LNAS

LB DRX LNA

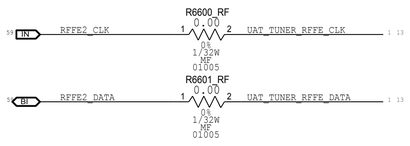


MB/HB DRX LNA



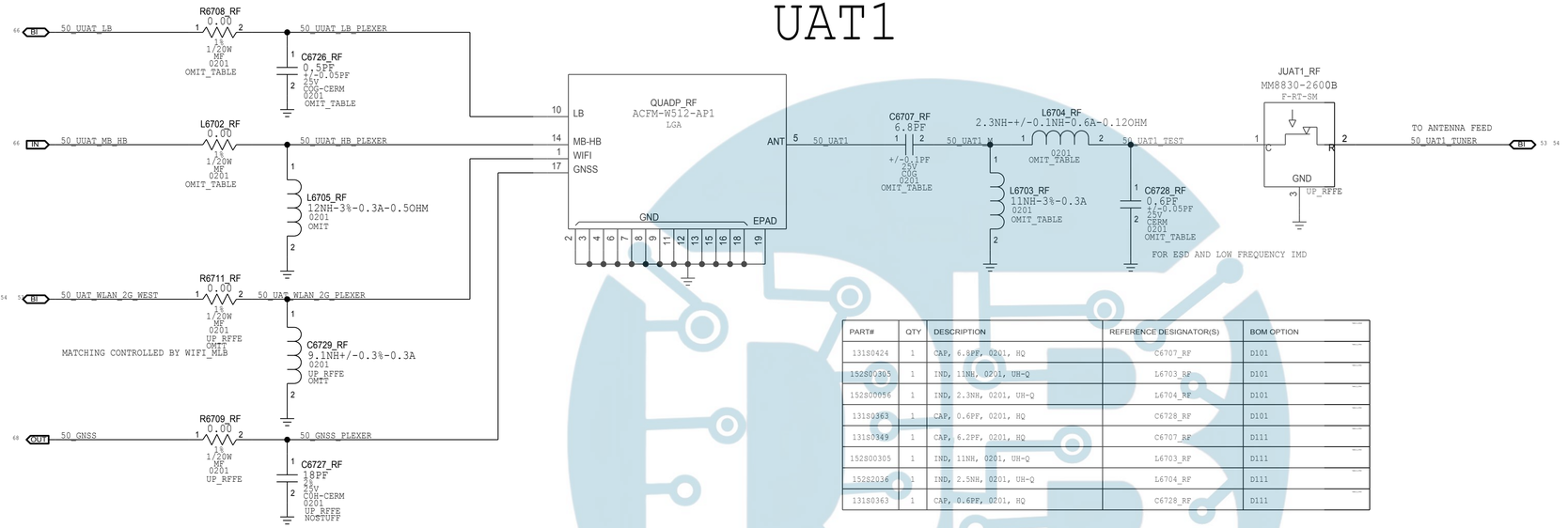


RFFE2 IMPEDANCE MATCHING



UPPER ANTENNA FEEDS

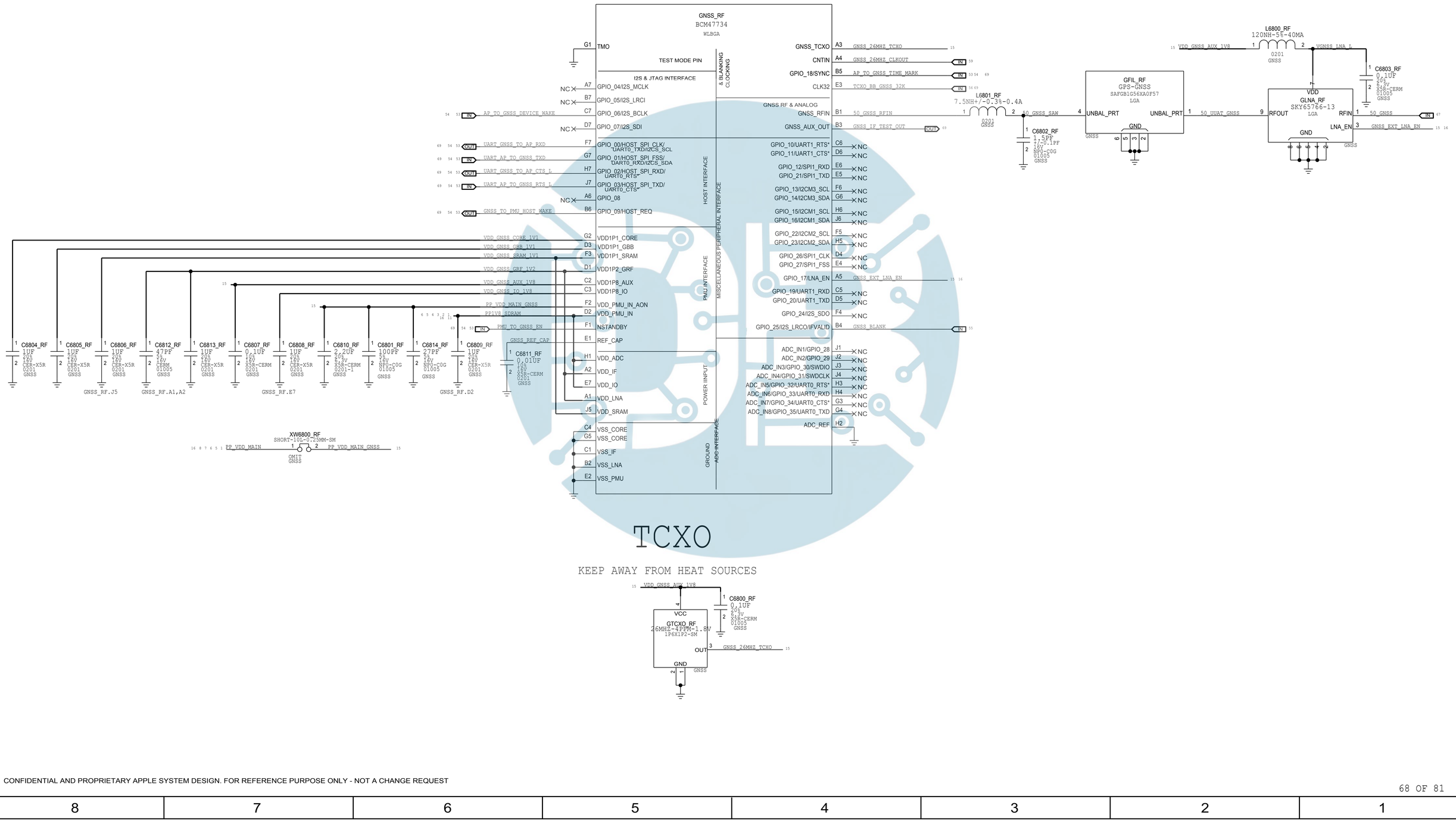
UAT1



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0724	1	RES, 0OHM, 0201	R6708_RF	D101
131S0425	1	CAP, 0.5PF, 0201, HQ	C6726_RF	D101
118S0724	1	RES, 0OHM, 0201	L6702_RF	D101
152S00020	1	IND, 12NH, 0201, UH-Q	L6705_RF	D101
118S0724	1	RES, 0OHM, 0201	R6708_RF	D111
131S0425	1	CAP, 0.5PF, 0201, HQ	C6726_RF	D111
118S0724	1	RES, 0OHM, 0201	L6702_RF	D111
152S00020	1	IND, 12NH, 0201, UH-Q	L6705_RF	D111

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0424	1	CAP, 6.8PF, 0201, HQ	C6707_RF	D101
152S00305	1	IND, 11NH, 0201, UH-Q	L6703_RF	D101
152S00056	1	IND, 2.3NH, 0201, UH-Q	L6704_RF	D101
131S0363	1	CAP, 0.6PF, 0201, HQ	C6728_RF	D101
131S0349	1	CAP, 6.2PF, 0201, HQ	C6707_RF	D111
152S00305	1	IND, 11NH, 0201, UH-Q	L6703_RF	D111
152S2036	1	IND, 2.5NH, 0201, UH-Q	L6704_RF	D111
131S0363	1	CAP, 0.6PF, 0201, HQ	C6728_RF	D111

GNSS LNA + RECEIVER



MLB TEST POINTS

BASEBAND

PP6901_RF P2MM-NSM SM 1 AP_TO_BBPMU_SDWN_L 1 2 5 OMIT
PP6903_RF P2MM-NSM SM 1 BBPMU_PWRGOOD 3 5 6 OMIT
PP6904_RF P2MM-NSM SM 1 BBPMU_XG_RESET_L 3 5 OMIT
PP6905_RF P2MM-NSM SM 1 BBPMU_XG_RESET_SD_L 3 5 OMIT
PP6906_RF P2MM-NSM SM 1 TCXO_BB_GNSS_32K 3 15 OMIT
PP6909_RF P2MM-NSM SM 1 BB_DEBUG_ERROR 2 OMIT
PP6961_RF P2MM-NSM SM 1 AP_TO_BB_MESA_ON 1 2 OMIT
PP6962_RF P2MM-NSM SM 1 BB_TO_AP_GSM_TXBURST 1 2 OMIT
PP6963_RF P2MM-NSM SM 1 AP_TO_BB_TIME_MARK 1 2 OMIT

XCVR

PP6931_RF P2MM-NSM SM 1 SYSCLK_26MHZ 2 4 OMIT

ETIC

PP6932_RF P2MM-NSM SM 1 50_ET_DAC_P 7 8 OMIT
PP6933_RF P2MM-NSM SM 1 50_ET_DAC_N 7 8 OMIT

GNSS

PP6937_RF P2MM-NSM SM 1 GNSS_EXT_LNA_EN 15 OMIT
PP6936_RF P2MM-NSM SM 1 PMU_TO_GNSS_EN 1 15 OMIT
PP6938_RF P2MM-NSM SM 1 UART_GNSS_TO_AP_RXD 1 15 OMIT
PP6939_RF P2MM-NSM SM 1 UART_AP_TO_GNSS_TXD 1 15 OMIT
PP6964_RF P2MM-NSM SM 1 UART_GNSS_TO_AP_CTS_L 1 15 OMIT
PP6965_RF P2MM-NSM SM 1 UART_AP_TO_GNSS_RTS_L 1 15 OMIT
PP6966_RF P2MM-NSM SM 1 AP_TO_GNSS_TIME_MARK 1 15 OMIT
PP6940_RF P2MM-NSM SM 1 GNSS_IF_TEST_OUT 15 OMIT
PP6945_RF P2MM-NSM SM 1 GNSS_TO_PMU_HOST_WAKE 1 15 OMIT

BBPMU

PP6935_RF P2MM-NSM SM 1 BBPMU_VCLK 2 5 OMIT
PP6954_RF P2MM-NSM SM 1 BBPMU_VDIO 2 5 OMIT

DIGRF

PP6950_RF P2MM-NSM SM 1 90_DIGRF_M1_TX_P 2 6 OMIT
PP6951_RF P2MM-NSM SM 1 90_DIGRF_M1_TX_N 2 6 OMIT
PP6952_RF P2MM-NSM SM 1 90_DIGRF_A1_RX1_P 2 6 OMIT
PP6953_RF P2MM-NSM SM 1 90_DIGRF_A1_RX1_N 2 6 OMIT

PCIE

PP6915_RF P2MM-NSM SM 1 100_PCIE_AP_TO_BB_TX_P 1 2 OMIT
PP6916_RF P2MM-NSM SM 1 100_PCIE_AP_TO_BB_TX_N 1 2 OMIT
PP6918_RF P2MM-NSM SM 1 100_PCIE_BB_TO_AP_RX_N 1 2 OMIT
PP6919_RF P2MM-NSM SM 1 PCIE_AP_TO_BB_PERST_L 1 2 16 OMIT
PP6920_RF P2MM-NSM SM 1 PCIE_AP_BI_BB_CLKREQ_L 1 2 OMIT
PP6921_RF P2MM-NSM SM 1 PCIE_BB_TO_PMU_WAKE_L 1 2 OMIT

PCIE GND

PP6948_RF P2MM-NSM SM 1 OMIT
PP6949_RF P2MM-NSM SM 1 OMIT

SIM CARD CONNECTOR

SIM_DETECT_GND 9
CLK 3 — SIM1_CLK (69 55 IN)
RESET 2 — SIM1_RST (69 55 IN)
VCC 1 — VDD_SIM1 (16 5 4 2)
J_SIM_RF RCPT-WIDE-HSG-THICK-PIVOT F-RT-SM
SIM_DETECT 8 — SIM1_DETECT (OUT 55 69)
IO 7 — SIM1_IO (BI 55 69)
SWP 6 — SIM1_SWP (BI 33 54 69)
GND 5 10 11 12 13 14 15 16

C6900_RF 2.2UF 20% 6.3V X5R-CERM 0201-1 SIM
DZ6901_RF 10V-33PF 01005-1 SIM
DZ6900_RF 5.5V-6.2PF 0201 SIM
C6901_RF 100PF 5% 25V NPO-C0G 01005 BASEBAND

SIM1_IO (16 2)
SIM1_CLK (16 2)
SIM1_RST (16 2)
SIM1_SWP (16 1)

DZ6902_RF SG-WLL-2-2 ESD202-B1-CSP01005
DZ6904_RF SG-WLL-2-2 ESD202-B1-CSP01005
DZ6903_RF SG-WLL-2-2 ESD202-B1-CSP01005
DZ6905_RF SG-WLL-2-2 ESD202-B1-CSP01005

HARDWARE ID

PP1V8_SDRAM (16 15 11 6 5 4 3 2 1)

R6901_RF 1.00K 1% 1/32W MF 01005 BASEBAND OMIT
R6903_RF 1.00K 1% 1/32W MF 01005 BASEBAND OMIT
R6906_RF 1.00K 1% 1/32W MF 01005 BASEBAND OMIT
R6902_RF 1.00K 1% 1/32W MF 01005 BASEBAND OMIT
R6904_RF 1.00K 1% 1/32W MF 01005 BASEBAND OMIT
R6907_RF 1.00K 1% 1/32W MF 01005 BASEBAND OMIT

BB_HW_ID<0> (55 OUT)
BB_HW_ID<1> (55 OUT)
BB_HW_ID<2> (55 OUT)

NOTE: STUFFING FOR HWID IS IN RADIO_MLB_FF SUB-DESIGN

HARDWARE	HW_ID<2:0>	HARDWARE	HW_ID<2:0>	HARDWARE	HW_ID<2:0>
RF DEV2	0 0 Z	ICE16 PROTO0	0 0 0	ICE16.1 PROTO1	Z Z 1
RF DEV2.1	0 Z 0	ICE16 PROTO0 ES2	0 0 1	ICE16.1 PROTO2	Z 1 Z
RF DEV3	0 Z Z	ICE16 PROTO1	0 1 0	ICE16.1 EVT	Z 1 1
RF DEV4	Z 0 0	ICE16 PROTO2	0 1 1	ICE16.2 EVT	1 Z Z
RF DEV4.1	Z 0 Z	ICE16 PROTO2 ES2.2	1 0 0	ICE16.1 EVT2	1 Z 1
RF DEV4.2	Z Z 0	ICE16 EVT	1 0 1	ICE16.2 EVT2	1 1 Z
RF DEV5	Z Z Z	ICE16 EVT2 CARRIER	1 1 0	ICE16.1 DVT/PVT	0 1 Z
RF DEV5.1	0 Z 1	ICE16 DVT/PVT	1 1 1	ICE16.2 DVT/PVT	Z 0 1

DEV CONFIG

PP1V8_SDRAM (16 15 11 6 5 4 3 2 1)

R6909_RF 1.00K 1% 1/32W MF 01005 BASEBAND NOSTUFF
R6910_RF 1.00K 1% 1/32W MF 01005 BASEBAND NOSTUFF

DEV_HW_CONFIG (55 OUT)

HW_CONFIG	DEV_HW_CONFIG
RESERVED	Z
RESERVED	0
RESERVED	1

BOOTCFG

PP1V8_SDRAM (16 15 11 6 5 4 3 2 1)

R6905_RF 1.00K 1% 1/32W MF 01005 BASEBAND
R6908_RF 1.00K 1% 1/32W MF 01005 BASEBAND

HW_MON1 (56 OUT)
HW_MON2 (56 OUT)

R6911_RF 1.00K 1% 1/32W MF 01005 BASEBAND NOSTUFF

PCIE_AP_TO_BB_PERST_L (69 55 54 53 OUT)

STUFF FOR VENDOR CONFIG ONLY

	HW_MON1	HW_MON2	TRIG_IN
NAND	0	0	1
FLASHLESS	1	0	1
FLASHLESS_WDOG_DIS	1	1	0
NAND	1	1	1

BOOTSTRAPS ARE INTERNALLY PULLED DOWN

DEBUG CONNECTOR

MLB 516S1185
FLEX 516S1184

J_DEBUG 20-5857-036-001-829 F-ST-SM

PP_VDD_MAIN (16 15 8 7 6 5 1) — pin 41 / 37 / 38

USB_BB_VBUS (2 1)	1	2	VDD_SIM1 (2 4 5 16)
90_USB_BB_P (2 1)	3	4	SIM1_RST (2 16)
90_USB_BB_N (2 1)	5	6	SIM1_CLK (2 16)
PMU_TO_BBPMU_ON (5 1)	7	8	SIM1_IO (2 16)
PP1V8_SDRAM (16 15 11 6 5 4 3 2 1)	9	10	SIM1_SWP (1 16)
BB_JTAG_TDO (3)	11	12	SIM1_DETECT (2 16)
BB_JTAG_TDI (3)	13	14	VDD_SIM2
BB_JTAG_TRST_L (3)	15	16	SIM2_RST
AP_TO_BB_RESET_L (3 1)	17	18	SIM2_CLK
BB_JTAG_TCK (3)	19	20	SIM2_IO
BB_JTAG_TMS (3)	21	22	SIM2_SWP
PP_VDD_MAIN (SELECT 16 15 8 7 6 5 1)	23	24	SIM2_DETECT
SIM2_IO_R	25	26	BB_JTAG_RESET_L
UART_BB_TO_AP_RXD (2 1)	27	28	UART_BB_TO_WLAN_COEX (1 2)
UART_AP_TO_BB_TXD (2 1)	29	30	UART_WLAN_TO_BB_COEX (1 2)
PP_VDD_BOOST	31	32	
NC	33	34	
	35	36	
	39	40	
	42		

NOSTUFF

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

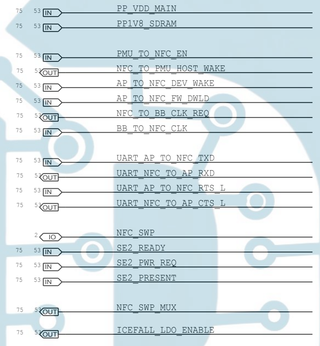
8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
5	0006232160	ENGINEERING RELEASED	2016-05-16

STOCKHOLM MLB
APRIL 11, 2016



ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
132S0436	132S0400	C7504_RF	0.22UF 20% 6.3V 01005	?

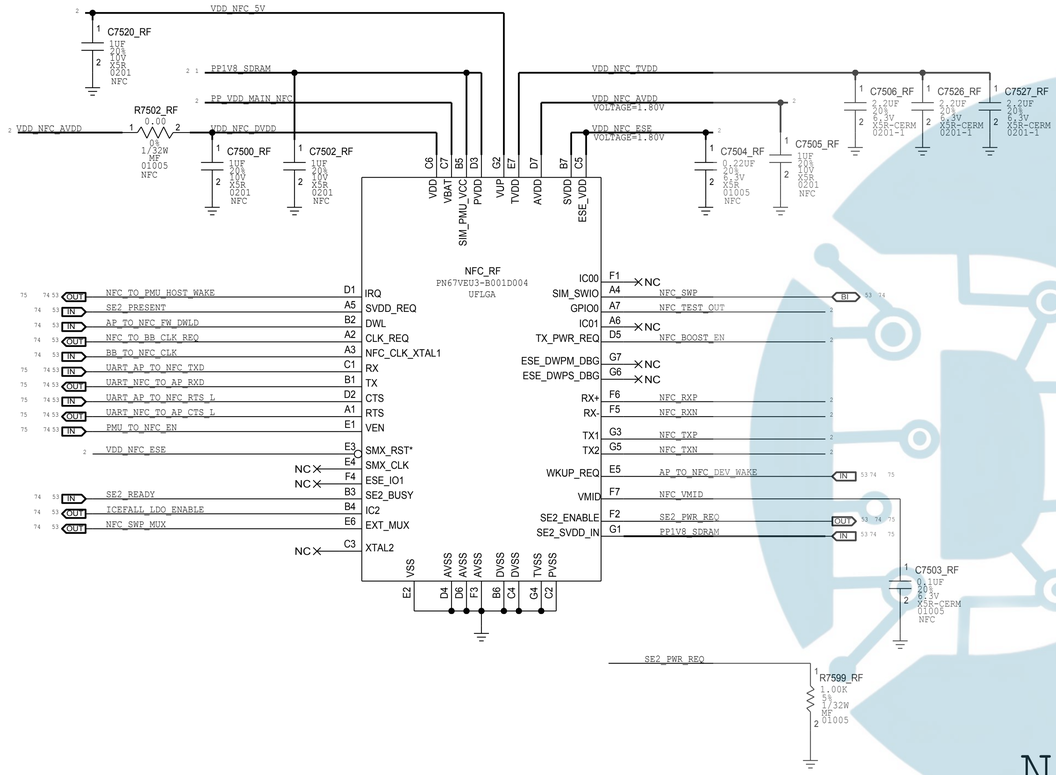
BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0883	1	220PF, 0201 2% 50V	C7514_RF	D101
131S00055	1	22PF, 0201 2% 50V	C7512_RF	D101
131S00117	1	120PF, 0201 2% 50V	C7518_RF	D101
131S00026	1	820PF, 0201 2% 50V	C7516_RF	D101
131S0883	1	220PF, 0201 2% 50V	C7514_RF	D10_JP
131S00055	1	22PF, 0201 2% 50V	C7512_RF	D10_JP
131S00017	1	47PF, 0201 2% 50V	C7518_RF	D10_JP
131S0825	1	560PF, 0201 2% 50V	C7516_RF	D10_JP
131S0883	1	220PF, 0201 2% 50V	C7514_RF	D10_ROW
131S00055	1	22PF, 0201 2% 50V	C7512_RF	D10_ROW
131S00117	1	120PF, 0201 2% 50V	C7518_RF	D10_ROW
131S00026	1	820PF, 0201 2% 50V	C7516_RF	D10_ROW

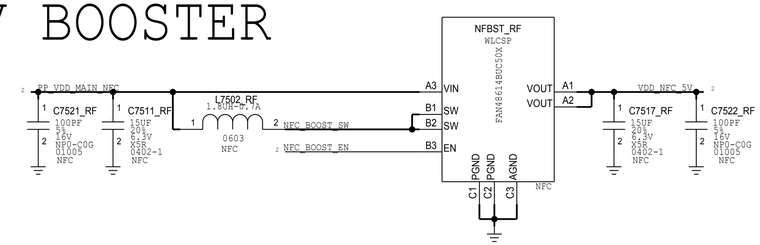
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00081	1	270PF, 0201 2% 25V	C7514_RF	D111
131S0883	1	220PF, 0201 2% 50V	C7518_RF	D111
131S00026	1	820PF, 0201 2% 50V	C7516_RF	D111
131S00081	1	270PF, 0201 2% 25V	C7514_RF	D11_JP
131S0731	1	100PF, 0201 2% 50V	C7518_RF	D11_JP
131S00033	1	680PF, 0201 2% 50V	C7516_RF	D11_JP
131S00081	1	270PF, 0201 2% 25V	C7514_RF	D11_ROW
131S0883	1	220PF, 0201 2% 50V	C7518_RF	D11_ROW
131S00026	1	820PF, 0201 2% 50V	C7516_RF	D11_ROW

STOCKHOLM

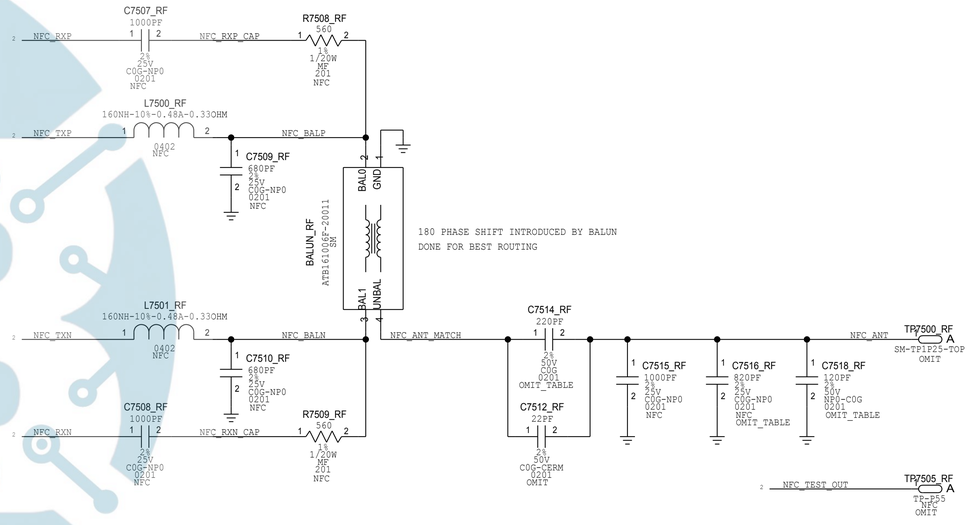
NFC CONTROLLER



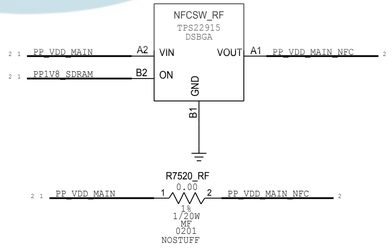
5V BOOSTER

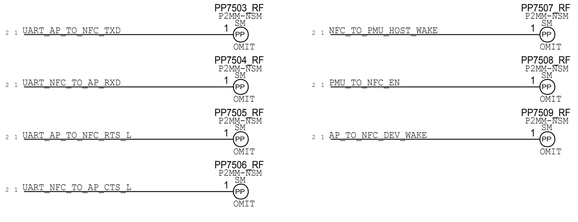


NFC FRONT END



NFC LOAD SWITCH





1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
5	0006232160	ENGINEERING RELEASED	2016-05-16

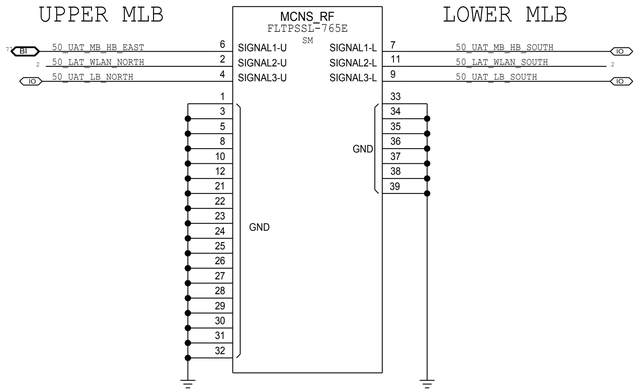
D111 RADIO MLB FF
Mon May 16 17:43:10 2016

PDF PAGE	CONTENTS
2	METROCIRC

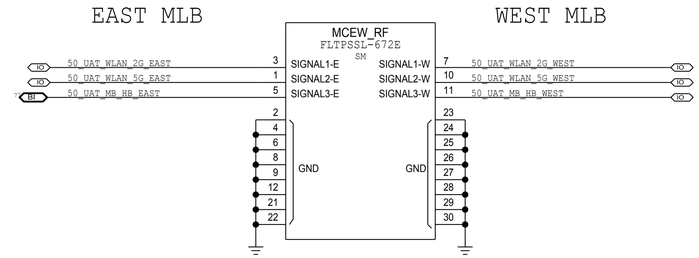
SCH: 951-02180
BOM: 939-01837
PCB: 920-XXXXX

METROCIRC

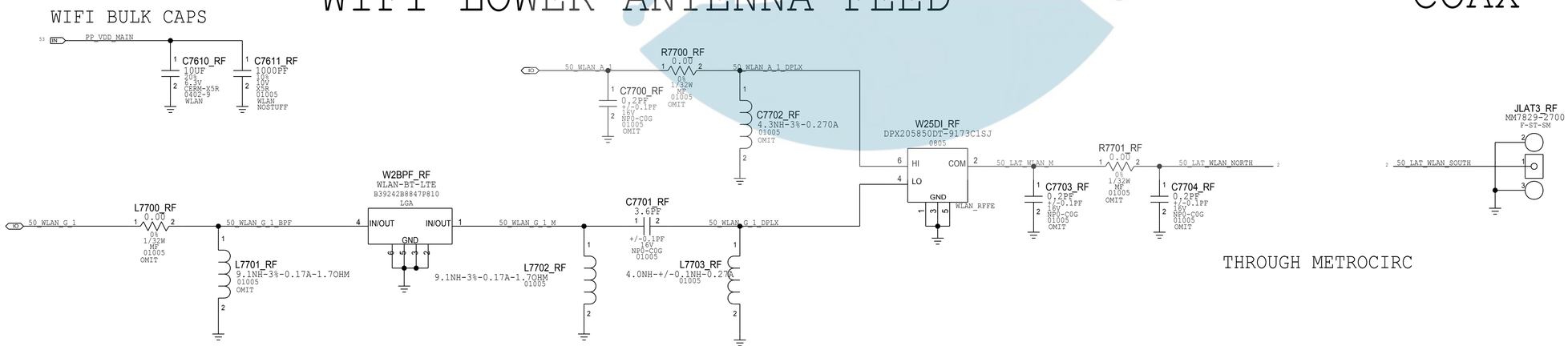
D111 NORTH-SOUTH METROCIRC
339S00147



D111 EAST-WEST METROCIRC
339S00146



WIFI LOWER ANTENNA FEED



COAX

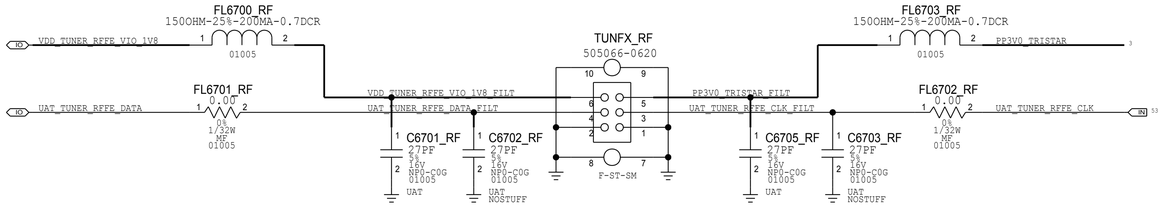
THROUGH METROCIRC

MATCHING CONTROLLED BY WIFI_MLB

ICE16.1/2 EVT2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11880608	2	RES, MF, 1K OHM, 1%, 1/32W, 01005	R6901_RF, R6906_RF	

UAT TUNER FLEX



PINOUT IS ROTATED 180 COMPARED TO D101

UAT TUNER

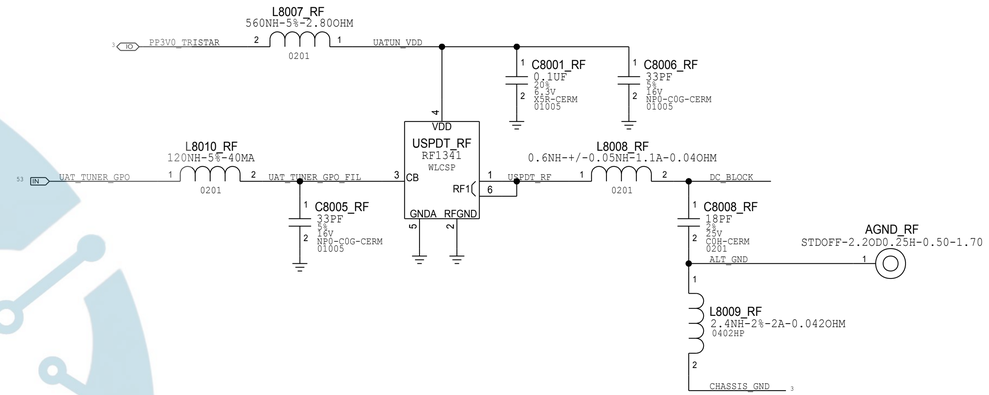
REMOVED

USID=0XC

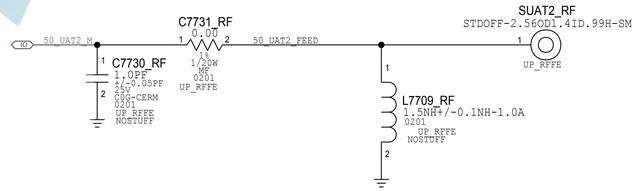
ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00482	152S00490	ALTERNATE	L8007_RF	MURATA LQW03CAR56J00

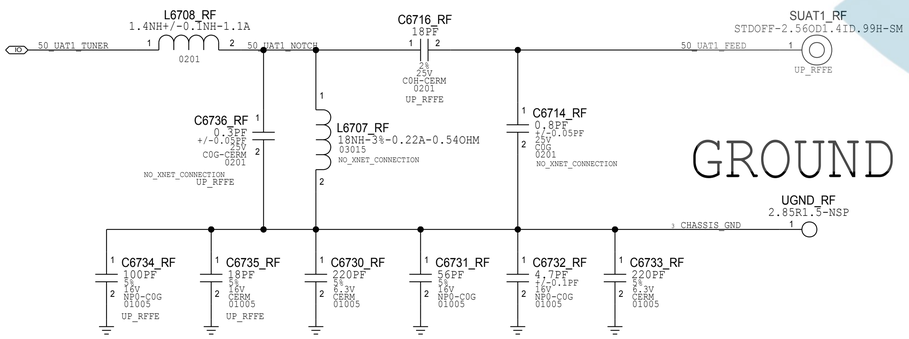
ALT UAT1 GND



5G WIFI STANDOFF



LB/MLB/GNSS/MB/HB STANDOFF



GROUND RING

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
5	0006232160	ENGINEERING RELEASED	2016-05-16

D1X WIFI MLB (PERENNIAL)
FEBRUARY 1, 2016

PDF PAGE	CSA PAGE	CONTENTS
2	76	PERENNIAL
3	77	WIFI FRONT-END

BOM OPTIONS:

D10_JP:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S0648	1	CAP,CER,0.3PF,+/-0.05,01005	C7705_RF	CRITICAL	D10_JP
152S00029	1	IND,1.1NH,UH-Q,01005	R7703_RF	CRITICAL	D10_JP
131S0893	1	CAP,CER,0.2PF,+/-0.05,01005	C7706_RF	CRITICAL	D10_JP
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7711_RF	CRITICAL	D10_JP
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7702_RF	CRITICAL	D10_JP
152S1980	1	IND,1.0NH,UH-Q,01005	R7704_RF	CRITICAL	D10_JP
131S0404	1	CAP,3.9PF,+/-1.0PF,01005	R6711_RF	CRITICAL	D10_JP
152S2061	1	IND,7.5NH,UH-Q,01005	C6729_RF	CRITICAL	D10_JP
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7700_RF	CRITICAL	D10_JP
152S2043	1	IND,6.2NH,UH-Q,01005	C7702_RF	CRITICAL	D10_JP
152S1998	1	IND, 0.8NH,UH-Q,01005	L7700_RF	CRITICAL	D10_JP
152S2043	1	IND,6.2NH,UH-Q,01005	L7701_RF	CRITICAL	D10_JP
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7701_RF	CRITICAL	D10_JP

NOSTUFF:C7729_RF,C7711_RF,C7709_RF,C7710_RF, C7707_RF, C7708_RF
C7700_RF, C7703_RF,C7704_RF

D10_ROW:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S0648	1	CAP,CER,0.3PF,+/-0.05,01005	C7705_RF	CRITICAL	D10_ROW
152S00029	1	IND,1.1NH,UH-Q,01005	R7703_RF	CRITICAL	D10_ROW
131S0893	1	CAP,CER,0.2PF,+/-0.05,01005	C7706_RF	CRITICAL	D10_ROW
117S0161	TRUE	RES,MF,0 OHM,1/32W,01005	R7711_RF	CRITICAL	D10_ROW
117S0161	TRUE	RES,MF,0 OHM,1/32W,01005	R7702_RF	CRITICAL	D10_ROW
152S1988	TRUE	IND,2.4NH,UH-Q,01005	R7704_RF	CRITICAL	D10_ROW
117S0161	TRUE	RES,MF,0 OHM,1/32W,01005	R6711_RF	CRITICAL	D10_ROW
152S1853	TRUE	IND,9.1NH,UH-Q,01005	C6729_RF	CRITICAL	D10_ROW
117S0161	TRUE	RES,MF,0 OHM,1/32W,01005	R7700_RF	CRITICAL	D10_ROW
152S2043	1	IND,6.2NH,UH-Q,01005	C7702_RF	CRITICAL	D10_ROW
152S1998	1	IND, 0.8NH,UH-Q,01005	L7700_RF	CRITICAL	D10_ROW
152S2043	TRUE	IND,6.2NH,UH-Q,01005	L7701_RF	CRITICAL	D10_ROW
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7701_RF	CRITICAL	D10_ROW

NOSTUFF:C7729_RF,C7711_RF,C7709_RF,C7710_RF, C7707_RF, C7708_RF
C7700_RF, C7703_RF,C7704_RF

D101_WIFI:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S0648	1	CAP,CER,0.3PF,+/-0.05,01005	C7705_RF	CRITICAL	D101
152S00029	1	IND,1.1NH,UH-Q,01005	R7703_RF	CRITICAL	D101
131S0893	1	CAP,CER,0.2PF,+/-0.05,01005	C7706_RF	CRITICAL	D101
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7711_RF	CRITICAL	D101
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7702_RF	CRITICAL	D101
152S1988	TRUE 1	IND,2.4NH,UH-Q,01005	R7704_RF	CRITICAL	D101
131S0648	TRUE 1	CAP,CER,0.3PF,+/-0.05PF,01005	C7708_RF	CRITICAL	D101
118S0724	TRUE 1	RES,MF, 0 OHM,1/20W, 0201	R6711_RF	CRITICAL	D101
152S2054	TRUE 1	IND,9.1NH,UH-Q,0201	C6729_RF	CRITICAL	D101
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7700_RF	CRITICAL	D101
152S2043	TRUE 1	IND,6.2NH,UH-Q,01005	C7702_RF	CRITICAL	D101
152S1998	1	IND, 0.8NH,UH-Q,01005	L7700_RF	CRITICAL	D101
152S2043	1	IND,6.2NH,UH-Q,01005	L7701_RF	CRITICAL	D101
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7701_RF	CRITICAL	D101

NOSTUFF: C7729_RF,C7711_RF,C7709_RF,C7710_RF, C7707_RF
C7700_RF, C7703_RF,C7704_RF

D11_JP:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S00273	TRUE 1	IND,0.6NH,UH-Q,01005	R7703_RF	CRITICAL	D11_JP
152S1976	TRUE 1	IND,0.7NH,UH-Q,01005	R7711_RF	CRITICAL	D11_JP
131S0400	TRUE 1	CAP,CER,3.5PF+/-0.1,01005	R7702_RF	CRITICAL	D11_JP
152S1986	TRUE 1	IND,FILM,2.2NH,UH-Q,01005	R7704_RF	CRITICAL	D11_JP
131S0648	TRUE 1	CAP,CER,0.3PF,+/-0.05PF,01005	C7708_RF	CRITICAL	D11_JP
131S0593	TRUE 1	CAP,3.9PF,+/-1.0PF,0201,HI-Q	R6711_RF	CRITICAL	D11_JP
152S2055	TRUE 1	IND,7.5NH,UH-Q,0201	C6729_RF	CRITICAL	D11_JP
117S0161	TRUE 1	RES,MF,0 OHM,1/32W,01005	R7700_RF	CRITICAL	D11_JP
117S0161	TRUE 1	RES,MF,0 OHM,1/32W,01005	L7700_RF	CRITICAL	D11_JP
152S1853	TRUE 1	IND,9.1NH,UH-Q,01005	L7701_RF	CRITICAL	D11_JP
117S0161	TRUE 1	RES,MF,0 OHM,1/32W,01005	R7701_RF	CRITICAL	D11_JP
131S0893	TRUE 1	CAP,CER,0.2PF,+/-0.05PF,01005	C7729_RF	CRITICAL	D11_JP

NOSTUFF:C7706_RF, C7711_RF,C7709_RF,C7710_RF, C7707_RF
C7700_RF,C7702_RF, C7703_RF,C7704_RF

D11_ROW:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S00273	1	IND,0.6NH,UH-Q,01005	R7703_RF	CRITICAL	D11_ROW
152S1976	1	IND,0.7NH,UH-Q,01005	R7711_RF	CRITICAL	D11_ROW
131S0400	1	CAP,CER,3.5PF+/-0.1,01005	R7702_RF	CRITICAL	D11_ROW
152S1986	TRUE 1	IND,FILM,2.2NH,UH-Q,01005	R7704_RF	CRITICAL	D11_ROW
118S0724	TRUE 1	RES,MF,0 OHM,1/20W,0201	R6711_RF	CRITICAL	D11_ROW
152S2054	TRUE 1	IND,9.1NH,UH-Q,0201	C6729_RF	CRITICAL	D11_ROW
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7700_RF	CRITICAL	D11_ROW
117S0161	1	RES,MF,0 OHM,1/32W,01005	L7700_RF	CRITICAL	D11_ROW
152S1853	1	IND,9.1NH,UH-Q,01005	L7701_RF	CRITICAL	D11_ROW
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7701_RF	CRITICAL	D11_ROW
131S0893	1	CAP,CER,0.2PF,+/-0.05PF,01005	C7705_RF	CRITICAL	D11_ROW
131S0893	1	CAP,CER,0.2PF,+/-0.05PF,01005	C7729_RF	CRITICAL	D11_ROW

NOSTUFF:C7706_RF,C7711_RF,C7709_RF,C7710_RF, C7707_RF, C7708_RF
C7700_RF,C7702_RF, C7703_RF,C7704_RF

D111_WIFI:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S00273	1	IND,0.6NH,UH-Q,01005	R7703_RF	CRITICAL	D111
152S1976	1	IND,0.7NH,UH-Q,01005	R7711_RF	CRITICAL	D111
131S0400	1	CAP,CER,3.5PF+/-0.1,01005	R7702_RF	CRITICAL	D111
152S1986	TRUE 1	IND,FILM,2.2NH,UH-Q,01005	R7704_RF	CRITICAL	D111
118S0724	TRUE 1	RES,MF, 0 OHM,1/20W, 0201	R6711_RF	CRITICAL	D111
152S2054	TRUE 1	IND,9.1NH,UH-Q,0201	C6729_RF	CRITICAL	D111
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7700_RF	CRITICAL	D111
117S0161	1	RES,MF,0 OHM,1/32W,01005	L7700_RF	CRITICAL	D111
152S1853	1	IND,9.1NH,UH-Q,01005	L7701_RF	CRITICAL	D111
117S0161	1	RES,MF,0 OHM,1/32W,01005	R7701_RF	CRITICAL	D111
131S0893	1	CAP,CER,0.2PF,+/-0.05PF,01005	C7705_RF	CRITICAL	D111
131S0893	1	CAP,CER,0.2PF,+/-0.05PF,01005	C7729_RF	CRITICAL	D111

NOSTUFF:C7706_RF,C7711_RF,C7709_RF,C7710_RF, C7707_RF, C7708_RF
C7700_RF,C7702_RF, C7703_RF,C7704_RF

POWER
80 53 IN PP_VDD_MAIN
80 53 IN PP1V8_SDRAM

CLOCKS
80 53 IN PMU_TO_WLAN_32K

CONTROL
80 53 IN PMU_TO_WLAN_REG_ON
80 53 IN PMU_TO_BT_REG_ON
80 4 OUT BT_TO_PMU_HOST_WAKE
80 53 IN AP_TO_BT_WAKE

WLAN PCIE
80 53 IN 100_PCIE_AP_TO_WLAN_REFCLK_P
80 53 IN 100_PCIE_AP_TO_WLAN_REFCLK_N
80 53 IN 100_PCIE_AP_TO_WLAN_TX_P
80 53 IN 100_PCIE_AP_TO_WLAN_TX_N
80 4 OUT 100_PCIE_WLAN_TO_AP_RX_P
80 4 OUT 100_PCIE_WLAN_TO_AP_RX_N
80 53 IN PCIE_AP_TO_WLAN_PERST_L
4 IO PCIE_AP_BI_WLAN_CLKREQ_L
80 4 OUT PCIE_WLAN_TO_PMU_WAKE
80 53 IN AP_TO_WLAN_DEV_WAKE

WLAN UART
80 4 OUT UART_WLAN_TO_AP_RXD
80 53 IN UART_AP_TO_WLAN_TXD
80 4 OUT UART_WLAN_TO_AP_CTS_L
80 53 IN UART_AP_TO_WLAN_RTS_L

BLUETOOTH UART
80 53 IN UART_AP_TO_BT_TXD
80 4 OUT UART_BT_TO_AP_RXD
80 53 IN UART_AP_TO_BT_RTS_L
80 4 OUT UART_BT_TO_AP_CTS_L

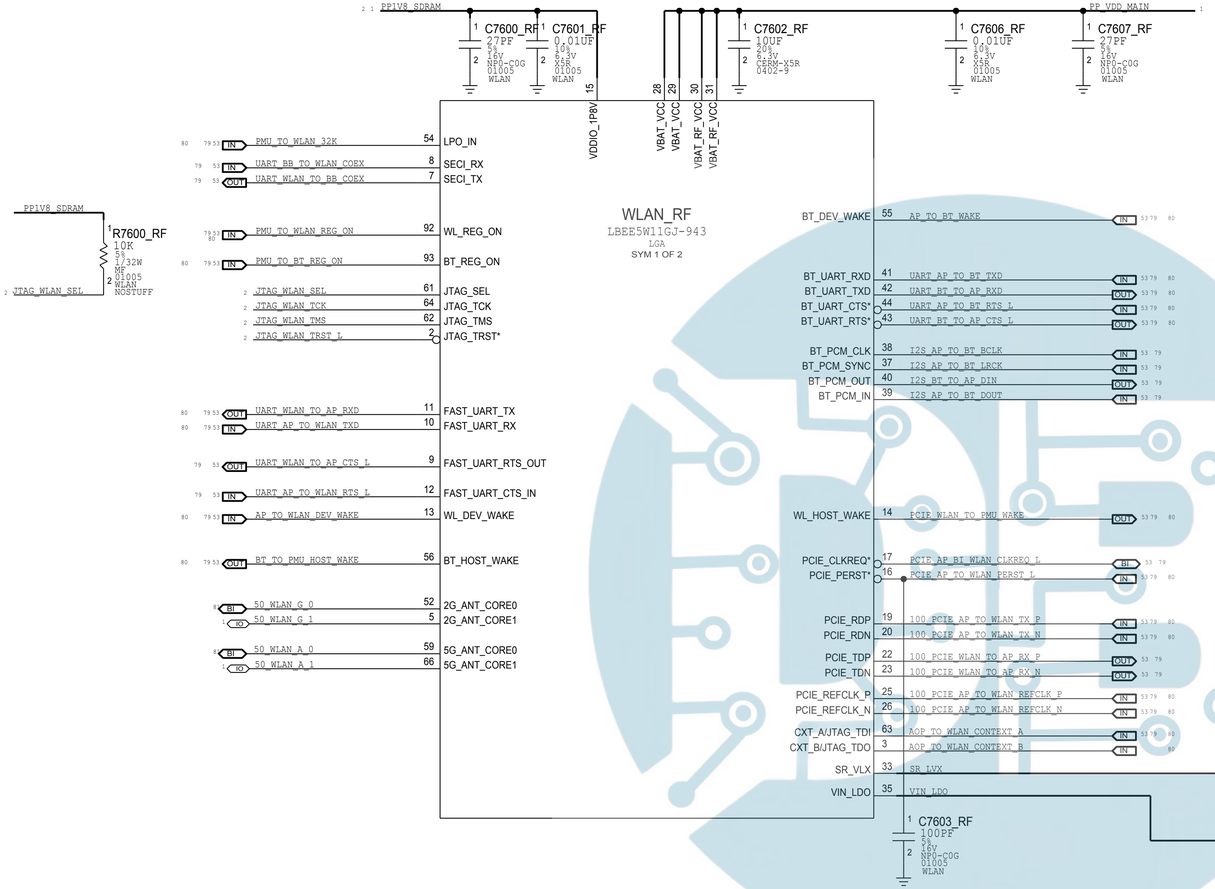
AOP
80 53 IN AOP_TO_WLAN_CONTEXT_A
80 53 IN AOP_TO_WLAN_CONTEXT_B

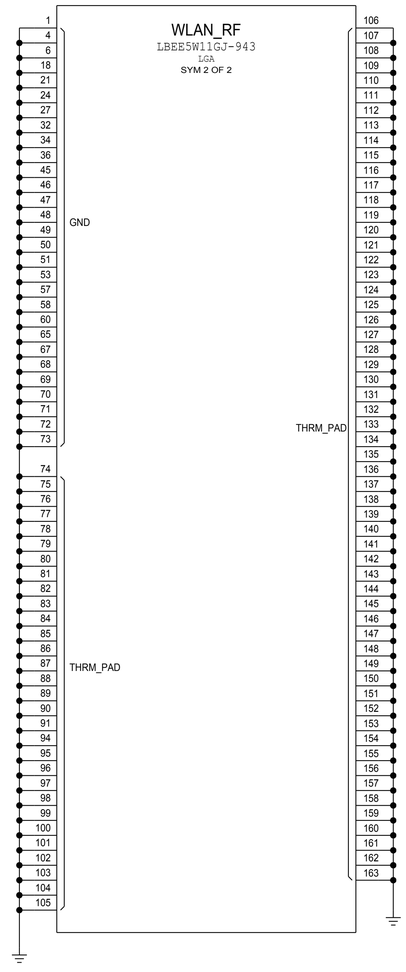
AUDIO
80 53 IN I2S_AP_TO_BT_BCLK
80 53 IN I2S_AP_TO_BT_LRCK
80 4 OUT I2S_BT_TO_AP_DIN
80 53 IN I2S_AP_TO_BT_DOUT

COEX
80 53 IN UART_BB_TO_WLAN_COEX
80 4 OUT UART_WLAN_TO_BB_COEX

ANTENNA
3 IO 50_UAT_WLAN_5G_WEST
3 IO 50_UAT_WLAN_2G_EAST
3 IO 50_UAT_WLAN_5G_EAST
3 IO 50_WLAN_G_1
3 IO 50_WLAN_A_1
3 IO 50_UAT2_M

WIFI/BT





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00201	339S00199	ALTERNATE	WLAN_RF	ALT WIFI/BT MODULE

PP7600_RF P2MM-NSM OMIT SM — AOP_TO_WLAN_CONTEXT_A TDI
PP7601_RF P2MM-NSM OMIT SM — AOP_TO_WLAN_CONTEXT_B TDO
PP7603_RF P2MM-NSM OMIT SM — UART_WLAN_TO_AP_RXD
PP7604_RF P2MM-NSM OMIT SM — UART_AP_TO_WLAN_TXD
PP7605_RF P2MM-NSM OMIT SM — JTAG_WLAN_TCK
PP7606_RF P2MM-NSM OMIT SM — JTAG_WLAN_TMS
PP7607_RF P2MM-NSM OMIT SM — JTAG_WLAN_TRST_L
PP7608_RF P2MM-NSM OMIT SM — AP_TO_WLAN_DEV_WAKE
PP7609_RF P2MM-NSM OMIT SM — BT_TO_PMU_HOST_WAKE
PP7610_RF P2MM-NSM OMIT SM — PMU_TO_WLAN_32K
PP7611_RF P2MM-NSM OMIT SM — PCIE_WLAN_TO_PMU_WAKE
PP7612_RF P2MM-NSM OMIT SM — 100_PCIE_AP_TO_WLAN_REFCLK_P
PP7613_RF P2MM-NSM OMIT SM — 100_PCIE_AP_TO_WLAN_REFCLK_N
PP7614_RF P2MM-NSM OMIT SM — 100_PCIE_AP_TO_WLAN_TX_P
PP7615_RF P2MM-NSM OMIT SM — 100_PCIE_AP_TO_WLAN_TX_N
PP7616_RF P2MM-NSM OMIT SM — PCIE_AP_TO_WLAN_PERST_L
PP7617_RF P2MM-NSM OMIT SM — JTAG_WLAN_SEL
PP7618_RF P2MM-NSM OMIT SM — PMU_TO_WLAN_REG_ON
PP7619_RF P2MM-NSM OMIT SM — PMU_TO_BT_REG_ON
PP7620_RF P2MM-NSM OMIT SM — UART_AP_TO_BT_TXD
PP7621_RF P2MM-NSM OMIT SM — UART_BT_TO_AP_RXD
PP7622_RF P2MM-NSM OMIT SM — UART_AP_TO_BT_RTS_L
PP7623_RF P2MM-NSM OMIT SM — UART_BT_TO_AP_CTS_L
PP7624_RF P2MM-NSM OMIT SM — AP_TO_BT_WAKE

WIFI UPPER ANTENNA FEEDS