1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

D54 TOP

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0024125573	ENGINEERING RELEASED	2020-07-01

LAST_MODIFICATION=Wed Jul 1 16:52:56 2020

EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-08572	MPYK	CRITICAL	EEEE:08572
825-7691	1	EEEE FOR 639-10112	NY8W	CRITICAL	EEEE:10112
825-7691	1	EEEE FOR 639-10113	NY9G	CRITICAL	EEEE:10113
825-7691	1	EEEE FOR 639-10115	NY9Y	CRITICAL	EEEE:10115
825-7691	1	EEEE FOR 639-10116	NYC9	CRITICAL	EEEE:10116
825-7691	1	EEEE FOR 639-10117	NYCN	CRITICAL	EEEE:10117

APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-05170	1	SCH,TOP,D54	SCH	CRITICAL ?	
820-01940	1	PCB,TOP,D54	PCB	CRITICAL ?	

Sub-designs

Hierarchies

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/SOFT	SYNC_DATE/TIME	FORCE SUBDESIGN
D52	HIER_ARROW	0.49.0	S	2020_06_30_13:39:10	N
D54	HIER_RADIO_MAV_TOP	3.25.0	S	2020_06_30_13:38:18	N
D54	HIER_NFC_TOP	0.19.0	S	2020_06_30_13:40:07	N
D54	HIER_WIFI_TOP	0.15.0	S	2020_06_30_13:37:33	N

Pages

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/SOFT	SYNC_DATE/TIME
D52	AP_MASTER	2,7,10-21,23-26,28,31,32-40,42,44-47,49,53-54,58-59,62,64-65,70-71,73-74,78-83,84,90-91,93-97,99	3.91.0	S	2020_07_01_16:41:16

Packaging Options

PACK_OPTIONS TO INCLUDE IN NETLIST
D54

TABLE OF CONTENTS

DRAWING TITLE: SCH,TOP,D54

DRAWING NUMBER: 051-05170 SIZE: D
REVISION: 10.0.0
BRANCH:
PAGE: 1 OF 138
SHEET: 1 OF 117

Multi-Vendor Criticals

Capacitors

In descending order of value, then package size

CRITICAL PART#	COMMENT
138S0979	CAP,CER,X5R,10UF,20%,10V,0402,H=0.65MM
138S0652	CAP,CER,X5R,4.7UF,20%,6.3V,H=0.65MM,0402
138S00070	CAP,X5R,4.7UF,20%,25V,0402
132S0663	CAP,CER,X5R,1UF,10%,25V,0402
138S0683	CAP,CER,X5R,1UF,10%,25V,0402
138S0692	CAP,CER,X5R,1UF,20%,6.3V,0201
138S00014	CAP,CER,1UF,20%,16V,X5R,0201,H=0.39MM
132S0304	CAP,CER,X5R,0.22UF,20%,6.3V,0201
132S00008	CAP,CER,0.1UF,10%,50V,X7R,0402
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0534	CAP,CER,X5R,0.1UF,10%,25V,0201
132S0664	CAP,CER,0.047UF,10%,25V,X5R,0201
132S00025	CAP,CER,X5R,0.047UF,20%,6.3V,01005
132S00093	CAP,X5R,0.022UF,20%,6.3V,01005
132S0245	CAP,CER,X5R,0.01UF,10%,6.3V,01005
132S0396	CAP,CER,X5R,1000PF,10%,10V,01005
132S0296	CAP,CER,X5R,1000PF,10%,6.3V,01005
132S0318	CAP,CER,X5R,820PF,10%,10V,01005
132S0275	CAP,CER,X5R,470PF,10%,10V,01005
131S0883	CAP,CER,NP0/C0G,220PF,2%,50V,0201
131S00170	CAP,CER,C0G,220PF,5%,25V,01005
131S00053	CAP,CER,C0G,220PF,5%,10V,01005
132S0249	CAP,CER,X7R,220PF,10%,10V,01005
131S0307	CAP,CER,NP0/C0G,100PF,5%,16V,01005

Capacitors (cont'd)

CRITICAL PART#	COMMENT
131S00303	CAP,CER,NPO/C0G,100PF,5%,16V,01005
131S00323	CAP,CER,NPO/C0G,56PF,5%,25V,01005
131S0643	CAP,CER,NP0/C0G,56PF,5%,25V,01005
131S0216	CAP,CER,NP0/C0G,47PF,5%,16V,01005
131S0804	CAP,CER,27PF,5%,C0G,25V,0201
131S0223	CAP,CER,NP0/C0G,27PF,5%,16V,01005
131S0215	CAP,CER,NPO/C0G,22PF,5%,16V,01005
131S0225	CAP,CER,NP0/C0G,15PF,5%,16V,01005
131S0220	CAP,CER,NP0/C0G,12PF,5%,16V,01005
131S00353	CAP,CER,NPO/C0G,10PF,5%,16V,01005

Ferrites

CRITICAL PART#	COMMENT
155S0576	FERR BD,10 OHM,50%,750MA,0.07 DCR,01005
155S00168	FLTR,NOISE,65 OHMZ,3.4OHM,0.7-2GHZ,0605

Resistors

CRITICAL PART#	COMMENT
118S00068	RES,MF,1.3 MOHM,1%,200PPM,1/20W,0201
117S0055	RES,MF,1/20W,2M OHM,5,0201,SMD

Misc.

CRITICAL PART#	COMMENT
377S0106	SUPPR,TRANS,VARISTOR,12V,33PF,01005
107S0257	THERMISTOR,NTC,10K OHM,1%,B=3435,01005

2020 MLCCs

16uF, 0402, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00316	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402
138S00314	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402
138S00315	138S00313	?	ALL	CAP,X5R,16UF,20%,4V,M,0402

Primary: Murata
Taiyo
Kyocera
Samsung

11uF, 0402, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00318	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T
138S00319	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T
138S00320	138S00317	?	ALL	CAP,X5R,11UF,20%,4V,M,0402-3T

Primary: Murata
Kyocera
Samsung
Taiyo

2.7uF, 0201, 6.3V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00326	138S00325	80403_ID:0528A0403_ID:864	ALL	CAP,X5R,2.7UF,20%,6.3V,M,0201
138S00327	138S00325	?	ALL	CAP,X5R,2.7UF,20%,6.3V,M,0201

Primary: Murata
Kyocera (61184814)
Samsung

2.7uF, 0201, 4V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00324	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201
138S00322	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201
138S00323	138S00321	?	ALL	CAP,X5R,2.7UF,20%,4V,M,0201

Primary: Murata
Taiyo
Kyocera
Samsung

MAV20 PDN Single-source

0.22uF, 01005

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Taiyo
132S00304	132S00014	?	[SEE BELOW]	01005,0.22uF,6.3V,Kyocera

(C746,C747,C751,C753,C757,C758,C761,C762,C764,C765,C766,C767,C768,C770,C772,C774,C776,C778,C780,E1)
(C746,C747,C757,C758,C761,C762,C764,C765,C766,C767,C768,C770,C772,C774,C776,C778,C780,E1)

2.2uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?	[SEE BELOW]	CAP,CER,X5R,2.2UF,20%,6.3V,0201

(C701,C704,C705,C715,C721,C722,C725,C726,C728,C732,C734,C736,C742,C744,C746,C748,C750,C752,C754,C756,C758,C760,C762,C764,C766,C768,C770,C772,C774,C776,E1)

4uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C511,E-C518,E-C522,E-C524,E-C526,E-C702,E-C704,E-C708,E-C777,E-C787,E-C788,E-C1130,E-C1142,E-C1210,E-C1727,E-C5001,E-C5002,E-C5023,E-C5027,E-C5028,E)
(C511,E-C518,E-C522,E-C524,E-C526,E-C702,E-C704,E-C708,E-C777,E-C787,E-C788,E-C1130,E-C1142,E-C1210,E-C1727,E-C5001,E-C5002,E-C5023,E-C5027,E-C5028,E)

Capacitor Alternates

0.1uF, 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00185	132S0316	?	ALL	CAP,CER,X5R,0.1UF,20%,6.3V,01005

CRITICAL PART#	COMMENT
132S0316	01005,0.1uF, 6.3V

0.22uF, 01005

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?		01005,0.22uF,6.3V,Taiyo
132S00304	132S00014	?		01005,0.22uF,6.3V,Kyocera

CRITICAL PART#	COMMENT
132S00014	01005,0.22uF, 6.3V

0.47uF, 01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00133	138S00128	?	ALL	01005,0.47uF,6.3V,Murata
138S00269	138S00128	?	ALL	01005,0.47uF,6.3V,Taiyo
138S00269	138S00133	?	ALL	01005,0.47uF,6.3V,Taiyo

CRITICAL PART#	COMMENT
138S00128	01005,0.47uF,6.3V,Kyocera
138S00133	01005,0.47uF,6.3V,Murata

1uF, 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S0945	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,KYOCERA

CRITICAL PART#	COMMENT
138S0706	CAP,X5R,1UF,20%,10V,0201

2.2uF, 0201

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?		CAP,CER,X5R,2.2UF,20%,6.3V,0201

CRITICAL PART#	COMMENT
138S0831	CAP,CER,X5R,2.2UF,20%,6.3V,0201

3uF @ 1V, 0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00138	138S00139	?	ALL	0201,3uF@1V,KYOCERA
138S00164	138S00139	?	ALL	0201,3uF@1V,TAIYO
138S00280	138S00139	?	ALL	0201,3uF@1V,SAMSUNG

CRITICAL PART#	COMMENT
138S00139	0201,3uF@1V

4uF, 0201

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?		CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?		CAP,X5R,4UF,0201,0.55MM,KYOCERA

CRITICAL PART#	COMMENT
138S00071	0201,X5R,4UF,0201,0.55MM,MURATA

4.7uF, 0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1103	138S0719	?	ALL	CAP,CER,X5R,4.7UF,20%,10V,0402

CRITICAL PART#	COMMENT
138S0719	0402,4.7uF,10V

15uF, 0402

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?		0402,15uF,6.3V, Kyocera

(C1805,C3321,C1872,C3371,C3382)

CRITICAL PART#	COMMENT
138S00003	0402,15uF,6.3V

18uF, 0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00221	138S00146	?	ALL	CAP,CER,X5R,18UF,20%,6.3V,MUR,0402

CRITICAL PART#	COMMENT
138S00146	CAP,CER,X5R,18UF,20%,6.3V,MUR,0402

20uF, 0402

All parts are single-sourced except for approved parts (listed below)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00339	138S0884	?		Taiyo

C3302,C3312,C3333,C3350,C3364,C3393,C3412,C3423,C3525,C3535,C3403,C1807,C1866,C5174,C2630

Kyocera ALT removed due to 63646020

CRITICAL PART#	COMMENT
138S0884	CAP,CER,X5R,20UF,20%,6.3V,0402,H=0.7MM

22uF, 0402

All RefDes in ( ) do not include Kyocera ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00144	138S00279	?	ALL	CAP,X5R,20UF,20%,4V,MURATA,0402
138S00143	138S00279	?	(C489,E-C431,E)	CAP,X5R,22UF,20%,4V,KYOCERA,0402

CRITICAL PART#	COMMENT
138S00279	CAP,X5R,26UF,20%,4V,SEMCO,0402

10uF @ 1V, 4-Term

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00148	138S00149	?	ALL	0402-3T,10.5uF@1V, Kyocera
138S00150	138S00149	?	ALL	0402-3T,10.5uF@1V, SEMCO
138S00151	138S00149	?	ALL	0402-3T,10.5uF@1V, TY

CRITICAL PART#	COMMENT
138S00149	0402-3T,10.5uF@1V

22uF, 0402 3T (WiFi)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00024	138S0966	?	ALL	CAP,CER,3-TERM,7.5UF,20%,4V,0402

CRITICAL PART#	COMMENT
138S0986	CAP,CER,3-TERM,7.5UF,20%,4V,0402

Display Choke Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00415	155S00524	?	ALL	FLTR,NOISE,35-50OHZ,3 OHM,7GHZ,50MA,0403

CRITICAL PART#	COMMENT
155S00524	FLTR,NOISE,35 OHMZ,3 OHM,7GHZ,50MA,0403

Level Shifter Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S00231	311S00232	?	ALL	IC,74AVC2T45,XCVR,2 BIT,2 SPLY,X2SON8
311S00230	311S00212	?	ALL	IC,74AVC1T45,XCVR,1 BIT,2 SPLY,X2SON6
311S00261	311S00233	?	ALL	IC,LSF0101,XCVR,2 BIT CFG,2 SPLY,X2SON6

CRITICAL PART#	COMMENT
311S00232	IC,74AVC2T45,XCVR,2 BIT,2 SPLY,X2SON8
311S00212	IC,74AVC1T45,XCVR,1 BIT,2 SPLY,X2SON6
311S00233	IC,LSF0101,XCVR,2 BIT CFG,2 SPLY,X2SON6
311S00235	IC,NVT0202,XCVR,2 BIT, 2 SPLY,BIDI,DFN8

Power Inductor Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00721	152S00876	?	ALL	Taiyo,IND,MLD,1UH,3.6A,60MΩ,2016
152S00930	152S00897	?	ALL	Cyntec,IND,CPLD,0.33M,0.1A,67MΩ,2016
152S00826	152S00821	?	ALL	Taiyo,IND,MLD,1UH,2.3A,60MΩ,2012
152S00831	152S00818	?	ALL	Taiyo,IND,MLD,0.22UH,5.3A,49MΩ,1608
152S00991	152S00984	?	ALL	Taiyo,IND,MLD,0.47UH,3.5A,34MΩ,1614
152S00992	152S00985	?	ALL	Taiyo,IND,MLD,0.47UH,4.0A,45MΩ,2012
152S00989	152S00982	?	ALL	Taiyo,IND,MULT,0.47UH,2.8A,79MΩ,1608
152S00872	152S00918	?	ALL	TDK,IND,MLD,0.47UH,5.6A,30MΩ,H=0.8,2016
152S00847	152S00918	?	ALL	CYNTEC,IND,MLD,0.47UH,5.9A,29MΩ,H=0.8,2016
152S01282	152S01255	?	ALL	TAIYO,IND,MLD,0.47UH,5A,30MΩ,H=0.65,2117

CRITICAL PART#	COMMENT
152S00876	Cyntec,IND
152S00897	Taiyo,IND
152S00821	Cyntec,IND
152S00818	Cyntec,IND
152S00984	Cyntec,IND
152S00985	Cyntec,IND
152S00982	Cyntec,IND

Boost/Yeti (2117/0.8mm)

Boost/Yeti (2117/0.65mm)

Misc. Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00437	155S00402	?	ALL	FERR BD,330HM,25%,1.5A,55MOHM DCR,0201
155S00194	155S00400	?	ALL	FERR BD,150OHM,25%,200MA,0.75OHM DCR,01005
155S00414	155S0876	?	ALL	FERR BD,180HM,50%,1.1A,0.05OHM DCR,01005
155S00131	155S0755	?	ALL	FERR BD,2400HM,25%,200MA,1.0OHM DCR,01005
155S00583	155S00140	?	ALL	FERR BD,330HM,25%,400MA,0.20DCR,01005
377S00070	377S00001	?	ALL	TVS,BIDIR,5.8V,6PF,01005
377S00140	377S00001	?	ALL	TVS,BIDIR,5V,6PF,01005
377S0168	377S00129	?	ALL	SUPPRESS,TRANS,6.8V,100PF,HYDTECH,01005
107S0245	107S0244	?	ALL	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

CRITICAL PART#	COMMENT
155S00402	FERR BD,330HM,25%,1.5A,55MOHM DCR,0201
155S00400	FERR BD,150OHM,25%,200MA,0.70HM DCR,01005
155S0876	FERR BD,180HM,50%,1.1A,0.05OHM DCR,01005
155S0755	FERR BD,240 OHM,25%,200MA,1.0 DCR,01005
155S00140	FERR BD,330HM,25%,400MA,0.20DCR,01005
377S00001	TVS,BIDIR,5.8V,6PF,01005
377S00129	SUPRESS,TRANS,6.8V,100PF,01005
107S0244	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

ZRB Cap ALTs

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00240	138S00187	?	ALL	CAP,X5R,4.7UF,20%,25V,0402

CRITICAL PART#	COMMENT
138S00175	CAP,X5R,4.7UF,20%,25V,0402

0-ohm, 0201, 4.5A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
117S00040	117S00012	?	ALL	RES,MF,0 OHM,1/10W,4.5A,0201

CRITICAL PART#	COMMENT
117S00012	RES,MF,0 OHM,1/10W,4.5A,0201

Low-noise, 0201, 2.2uF

RefDes field intentionally left blank to allow selective single-sourcing

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00185	138S00246	?		CAP,X5R,2.2UF,20%,25V,0402

22uF, 0704

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00347	138S00296	?	ALL	CAP,X5R,22UF,20%,16V,TA1,H=0.8MM,0704

CRITICAL PART#	COMMENT
138S00296	CAP,X5R,22UF,20%,16V,MUR,H=0.8MM,0704

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90-ohm Diff Pair Constraints

Electrical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	E_LPDP_WIDE	E	DIFF_PAIR	DP:DP_90_LPDP*_WIDE*	Y
	E_LPDP_SWIDE	E	DIFF_PAIR	DP:DP_90_LPDP*_SWIDE*	Y
	E_LPDP_TELE	E	DIFF_PAIR	DP:DP_90_LPDP*_TELE*	Y
	E_LPDP_FCAM	E	DIFF_PAIR	DP:DP_90_LPDP*_FCAM*	Y
	E_LPDP_JASPER	E	DIFF_PAIR	DP:DP_90_LPDP*_JASPER*	Y
MIPI	E_MIPI_DISPLAY	E	DIFF_PAIR_MIPI-D	DP:DP_90_MIPI*DISPLAY*	N
	E_MIPI_IRCAM	E	DIFF_PAIR_MIPI-C	DP:DP_90_MIPI*_IRCAM*	N
PCIE	E_PCIE_NAND	E	DIFF_PAIR	DP:DP_90_PCIE*_NAND*	Y
	E_PCIE_WLAN	E	DIFF_PAIR	DP:DP_90_PCIE*_WLAN*	Y
	E_PCIE_BB	E	DIFF_PAIR	DP:DP_90_PCIE*_BB*	Y
USB	E_KRAKEN_DP	E	DIFF_PAIR	DP:DP_90_KRAKEN*	Y
	E_MIKEYBUS_DP	E	DIFF_PAIR	DP:DP_90_MIKEYBUS*	Y
	E_USB_DP	E	DIFF_PAIR	DP:DP_90_USB*	Y
	E_EUSB_DP	E	DIFF_PAIR	DP:DP_90_EUSB*	Y

Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	90_LPDP_WIDE	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_WIDE*	Y
	90_LPDP_SWIDE	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_SWIDE*	Y
	90_LPDP_TELE	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_TELE*	Y
	90_LPDP_FCAM	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_FCAM*	Y
	90_LPDP_JASPER	P	A_90_OHM_DIFF	DP:DP_90_LPDP*_JASPER*	Y
MIPI-D	90_MIPI_DISPLAY	P	A_90_OHM_DIFF	DP:DP_90_MIPI*DISPLAY*	Y
MIPI-C	90_MIPI_IRCAM	P	A_90_OHM_DIFF	DP:DP_90_MIPI*_IRCAM*	Y
PCIE (Gen4)	90_PCIE_NAND	P	A_90_OHM_DIFF	DP:DP_90_PCIE*_NAND*	Y
	90_PCIE_BB	P	A_90_OHM_DIFF	DP:DP_90_PCIE*_BB*	Y
PCIE (Gen2)	90_PCIE_WLAN	P	A_90_OHM_DIFF	DP:DP_90_PCIE*_WLAN*	Y
USB	90_KRAKEN_DP	P	A_90_OHM_DIFF	DP:DP_90_KRAKEN*	Y
	90_USB_DP	P	A_90_OHM_DIFF	DP:DP_90_USB*	Y
	90_EUSB_DP	P	A_90_OHM_DIFF	DP:DP_90_EUSB*	Y
MIKEYBUS	90_MIKEYBUS_DP	P	A_90_OHM_DIFF	DP:DP_90_MIKEYBUS*	Y

Spacing

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LPDP	90_LPDP_WIDE	S	A_DIELECTRIC_3X	=	Y
	90_LPDP_SWIDE	S	A_DIELECTRIC_3X	=	Y
	90_LPDP_TELE	S	A_DIELECTRIC_3X	=	Y
	90_LPDP_FCAM	S	A_DIELECTRIC_3X	=	Y
	90_LPDP_JASPER	S	A_DIELECTRIC_3X	=	Y
MIPI-D	90_MIPI_DISPLAY	S	A_DIELECTRIC_3X	=	Y
MIPI-C	90_MIPI_IRCAM	S	A_DIELECTRIC_2X	=	Y
PCIE (Gen4)	90_PCIE_NAND	S	A_DIELECTRIC_3X	=	Y
	90_PCIE_BB	S	A_DIELECTRIC_3X	=	Y
PCIE (Gen2)	90_PCIE_WLAN	S	A_DIELECTRIC_3X	=	Y
USB	90_KRAKEN_DP	S	A_DIELECTRIC_3X	=	Y
	90_USB_DP	S	A_DIELECTRIC_3X	=	Y
	90_EUSB_DP	S	A_DIELECTRIC_3X	=	Y
MIKEYBUS	90_MIKEYBUS_DP	S	A_DIELECTRIC_2X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING			
	CLASS NAME	CLASS NAME	CONSTRAINT SET
LPDP <-> LPDP	90_LPDP_WIDE	90_LPDP_WIDE	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_SWIDE	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_TELE	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_WIDE	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_SWIDE	90_LPDP_SWIDE	A_DIELECTRIC_2X
	90_LPDP_SWIDE	90_LPDP_TELE	A_DIELECTRIC_2X
	90_LPDP_SWIDE	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_SWIDE	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_TELE	90_LPDP_TELE	A_DIELECTRIC_2X
	90_LPDP_TELE	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_TELE	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_FCAM	90_LPDP_FCAM	A_DIELECTRIC_2X
	90_LPDP_FCAM	90_LPDP_JASPER	A_DIELECTRIC_2X
	90_LPDP_JASPER	90_LPDP_JASPER	A_DIELECTRIC_2X
MIPI-D	90_MIPI_DISPLAY	90_MIPI_DISPLAY	A_DIELECTRIC_2X
PCIE (Gen2)	90_PCIE_WLAN	90_PCIE_WLAN	A_DIELECTRIC_2X
USB	90_KRAKEN_DP	90_KRAKEN_DP	A_DIELECTRIC_2X
	90_KRAKEN_DP	90_USB_DP	A_DIELECTRIC_2X
	90_KRAKEN_DP	90_EUSB_DP	A_DIELECTRIC_2X
	90_USB_DP	90_USB_DP	A_DIELECTRIC_2X
	90_USB_DP	90_EUSB_DP	A_DIELECTRIC_2X
	90_EUSB_DP	90_EUSB_DP	A_DIELECTRIC_2X

Spacing CSet Definitions

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from reference shortest distance is used unless "L" is defined	EXAMPLE: 1,0.5,7L,9L,10L 1.5,2,2.5,3,4
A_DIELECTRIC_(N)XO.XV.XVL.X Calculates dielectric distance from hybrid Table and lookup, shortest distance is used unless "L" defined	EXAMPLE: 2.0X,3VL,4.5VL PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from reference shortest distance is used unless "L" is defined	EXAMPLE: 1.2_4.5L,3L ?

Pin Delay Check

PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	PIN DELAY CSV FILE NAME
U1000	SicilyPinDelay.csv
J10800	D54_JulietPinDelay.csv

*Location: /physical/rule/pindelays

SYNC_MASTER=temp SYNC_DATE=07/01/2019

PAGE TITLE
CONSTRAINTS: 90-Ohm

DRAWING NUMBER 051-05170 SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 3 OF 138
SHEET 3 OF 117

Power Constraints

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LX/CX Nodes	PWR_SHAPE_LX	P	PWR_SHAPE	LX*,!LX_CHARGER_BOOT*,!LX_DPMIC*	Y
	PWR_SHAPE_LX_DPMIC	P	PWR_SHAPE	LX_DPMIC*	Y
	PWR_SHAPE_LX	P	PWR_SHAPE	CX*	Y
System-Wide	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAIN	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_BOOST*	Y
	PWR_50UM	P	PWR_50UM	PP3V0_S2	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_IO	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_S2	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_S4	Y
	PWR_200UM	P	PWR_200UM	PP1V2_IO	Y
	PWR_200UM	P	PWR_200UM	PP1V2_S2	Y
	PWR_200UM	P	PWR_200UM	PP1V2_S4	Y
SoC:CPU/GPU	PWR_SHAPE	P	PWR_SHAPE	PP_CPU_PCORE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_CPU_ECORE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_GPU	Y
SoC:SRAM/SOC	PWR_SHAPE	P	PWR_SHAPE	PP_CPU_SRAM	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_SRAM_S1	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_SOC_S1	Y
SoC:Fixed	PWR_SHAPE	P	PWR_SHAPE	PP0V78_SOC_FIXED_S1	Y
	PWR_80UM	P	PWR_80UM	PP0V78_VDD_FIXED_XTAL	Y
	PWR_80UM	P	PWR_80UM	PP0V78_SOC_FIXED_PCIE_REFBUF	Y
SoC:VDD12	PWR_80UM	P	PWR_80UM	PP1V2_S1	Y
	PWR_80UM	P	PWR_80UM	PP1V2_S1_XTAL	Y
	PWR_200UM	P	PWR_200UM	PP1V2_SOC	Y
	PWR_80UM	P	PWR_80UM	PP1V2_SOC_FILT	Y
	PWR_80UM	P	PWR_80UM	PP1V2_VDD12_FMON	Y
	PWR_80UM	P	PWR_80UM	PP1V2_VDD12_ULPPLL_S2	Y
	PWR_80UM	P	PWR_80UM	PP1V2_IO_GRP*	Y
SoC:DDR	PWR_SHAPE	P	PWR_SHAPE	PP_DCS_S1	Y
	PWR_200UM	P	PWR_200UM	PP0V6_VDDQL_S1	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V06_S2	Y
SoC:Misc.	PWR_SHAPE	P	PWR_SHAPE	PP0V7_VDD_LOW_S2	Y
	PWR_80UM	P	PWR_80UM	PP0V7_VDD_LOW_*LPPLL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_AVE_S1	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_DISP_S1	Y
	PWR_200UM	P	PWR_200UM	PP0V6_VDDIO06_GRP1_*	Y
NAND	PWR_100UM	P	PWR_100UM	PP_NAND_VDDIO1_R	Y
	PWR_300UM	P	PWR_300UM	PP_NAND_VDDIO1_F	Y
	PWR_SHAPE	P	PWR_SHAPE	PP0V83_NAND	Y
	PWR_100UM	P	PWR_100UM	PP0V83_NAND_PLL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP2V625_NAND	Y
PMU	PWR_SHAPE	P	PWR_SHAPE	PP1V5_VLDOINT	Y
	PWR_SHAPE	P	PWR_SHAPE	PP0V9_S1	Y
Yangtze	PWR_SHAPE	P	PWR_SHAPE	PP_VBUS1_E75	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VBUS2_DOTARA	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_CHARGER_PMID	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_BATT_VCC_YANGTZE	Y
	PWR_100UM_LX	P	PWR_100UM	LX_CHARGER_BOOT*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP6V0_CHARGER_LDO_INTERNAL	Y
	PWR_80UM	P	PWR_80UM	PP1V8_ALWAYS	Y
Dotara	PWR_SHAPE	P	PWR_SHAPE	PAC_DOTARA_COIL1	Y
	PWR_SHAPE	P	PWR_SHAPE	PAC_DOTARA_AC2	Y
	PWR_SHAPE	P	PWR_SHAPE	DOTARA_TX_BANK_2	Y
	PWR_SHAPE	P	PWR_SHAPE	PAC_DOTARA_COIL2	Y
	PWR_100UM	P	PWR_100UM	DOTARA_COMM*	Y
	PWR_200UM	P	PWR_200UM	DOTARA_CLAMP*	Y
	PWR_200UM	P	PWR_200UM	DOTARA_BOOT*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_DOTARA_VMID	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_DOTARA_VRECT	Y
	PWR_200UM	P	PWR_200UM	PP1V8_DOTARA_LDO	Y
	PWR_100UM	P	PWR_100UM	PP5V0_VDD_DOTARA	Y
	PWR_100UM	P	PWR_100UM	PP5V0_DOTARA_VMID	Y
	PWR_80UM	P	PWR_80UM	PP1V2_DOTARA_S2	Y
Camera PMUs	PWR_SHAPE	P	PWR_SHAPE	PP1V3_CAM_PMU*_BUCK0	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAX_CAM_PMU*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_RTC_CAM_PMU*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_CAM_PMU1_IO_SW	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V2_INT_CAM_PMU*	Y
Will/Jasper	PWR_100UM	P	PWR_100UM	PP3V0_WILL_VDD	Y
	PWR_100UM	P	PWR_100UM	PP1V8_CAM_PMU2_IO_SW	Y
	PWR_100UM_HV	P	PWR_100UM	PN_JASPER_VDDHV*	Y
	PWR_100UM	P	PWR_100UM	PP_JASPER_VDDLAS*	Y
Strobe	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_DRIVER_COOL_LED	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_DRIVER_WARM_LED	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_STROBE_BOOST_OUT	Y
Rigel/Pearl	PWR_SHAPE	P	PWR_SHAPE	PP_VANA	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_VINCORE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_BUCK_BOOST_A	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_RIGEL_BUCK_BOOST_B	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_CATHODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_DENSE_ANODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_SPARSE_ANODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_A_ANODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ROMEO_B_ANODE	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_BANE_ANODE	Y
	PWR_100UM	P	PWR_100UM	PP3V3_MAMABEAR_VDD	Y
Audio	PWR_50UM	P	PWR_50UM	PP1V8_AUDIO_VA_S2	Y
Codec	PWR_200UM	P	PWR_200UM	AGND_CODEC	Y
BotSpk	PWR_50UM	P	PWR_50UM	PP_VA_BOT_SPK_INTERNAL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_SPKRAMP_BOT_VBOOST	Y
	PWR_SHAPE	P	PWR_SHAPE	SPKRAMP_BOT_TO_COIL_OUT_*	Y
	PWR_80UM	P	PWR_80UM	AGND_BOT_SPK	Y
TopSpk	PWR_50UM	P	PWR_50UM	PP_VA_TOP_SPK_INTERNAL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_SPKRAMP_TOP_VBOOST	Y
	PWR_SHAPE	P	PWR_SHAPE	SPKRAMP_TOP_TO_COIL_OUT_*	Y
	PWR_80UM	P	PWR_80UM	AGND_TOP_SPK	Y

Physical (continued)

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Arc	PWR_50UM	P	PWR_50UM	PP1V2_ARCAMP_VD_FILT_INTERNAL	Y
	PWR_50UM	P	PWR_50UM	PP1V8_ARCAMP_VA_VL_INTERNAL	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_ARCAMP_VBOOST	Y
	PWR_SHAPE	P	PWR_SHAPE	ARCAMP_TO_SOLENOID_OUT*	Y
	PWR_80UM	P	PWR_80UM	AGND_ARCAMP	Y
Touch	PWR_100UM	P	PWR_100UM	PP1V2_TOUCH_S2*	Y
	PWR_80UM	P	PWR_80UM	PP3V1_TOUCH_S2*	Y
	PWR_200UM	P	PWR_200UM	PP1V8_TOUCH_S2*	Y
Display PMIC	PWR_SHAPE	P	PWR_SHAPE	PP7V3_DISPLAY_AVDDH*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP4V6_DISPLAY_VDDEL*	Y
	PWR_SHAPE	P	PWR_SHAPE	PNVAR_DISPLAY_VSSEL*	Y
Kraken	PWR_SHAPE	P	PWR_SHAPE	PP_ACC_VAR	Y
	PWR_80UM	P	PWR_80UM	PP_VAR_USB_RVP	Y
	PWR_200UM	P	PWR_200UM	PP_KRAKEN_ACC1*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_KRAKEN_ACC2*	Y
	PWR_80UM	P	PWR_80UM	ANALOG_VDD_MAIN_OV_R	Y
Parrot	PWR_80UM	P	PWR_80UM	PP3V3_USB_S2	Y
AF/OIS (Shared)	PWR_SHAPE	P	PWR_SHAPE	PPVAR_RCAM_PVDD	Y
Wide RCAM	PWR_100UM	P	PWR_100UM	PPVAR_WIDE_PVDD_CONN	Y
	PWR_100UM	P	PWR_100UM	PP3V2_WIDE_AVDD1	Y
	PWR_200UM	P	PWR_200UM	PPVAR_WIDE_AVDD2	Y
	PWR_100UM	P	PWR_100UM	PP1V6_WIDE_DVDD*	Y
SWide RCAM	PWR_100UM	P	PWR_100UM	PP2V85_SWIDE_AVDD1	Y
	PWR_200UM	P	PWR_200UM	PPVAR_SWIDE_AVDD2	Y
	PWR_100UM	P	PWR_100UM	PP1V2_SWIDE_DVDD	Y
Camera VDDIO	PWR_80UM	P	PWR_80UM	PP1V8_*VDDIO*	Y
Tele RCAM	PWR_100UM	P	PWR_100UM	PPVAR_TELE_PVDD_CONN	Y
	PWR_100UM	P	PWR_100UM	PP0V8_TELE_DVDD1	Y
	PWR_100UM	P	PWR_100UM	PP0V975_TELE_DVDD2	Y
	PWR_100UM	P	PWR_100UM	PP2V85_TELE_AVDD1	Y
	PWR_200UM	P	PWR_200UM	PP1V35_TELE_AVDD2	Y
FCAM	PWR_200UM	P	PWR_200UM	PP1V1_FCAM_DVDD	Y
	PWR_200UM	P	PWR_200UM	PP2V85_FCAM_AVDD*	Y
Juliet IRCAM	PWR_80UM	P	PWR_80UM	PP2V85_IRCAM_AVDD	Y
	PWR_80UM	P	PWR_80UM	PP1V2_IRCAM_DVDD	Y
Jasper	PWR_80UM	P	PWR_80UM	PP3V0_JASPER_RX_AVDD*	Y
	PWR_80UM	P	PWR_80UM	PP3V3_JASPER_TX_AVDD*	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V1_JASPER_DVDD*	Y
B2B	PWR_DEFAULT	P	PWR_DEFAULT	PP1V8_ALS_S2	Y
	PWR_80UM	P	PWR_80UM	PP1V8_COMPASS_S2_CONN	Y
Kobol	PWR_80UM	P	PWR_80UM	PP_VDDIO_IMU	Y
Penrose	PWR_80UM	P	PWR_80UM	PP3V0_PENROSE_SVDD*	Y
Dock	PWR_80UM	P	PWR_80UM	PP1V8_DOCK_S2_CONN	Y
	PWR_200UM	P	PWR_200UM	PPVAR_EIGER_S2*	Y
Display	PWR_80UM	P	PWR_80UM	PP1V2_DISPLAY_S2_CONN	Y
	PWR_80UM	P	PWR_80UM	PP1V8_DISPLAY_DVDD_CONN	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1VX_DISPLAY_S2*	Y
	PWR_80UM	P	PWR_80UM	PP3V0_DISPLAY_S2*	Y
NFC/Ironman NFC	PWR_80UM	P	PWR_80UM	PP1V2_NFC_S2	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*_VDDBOOST	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDC	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_MIX	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDNV	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_TVDD	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VDDPLL	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VHV	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_MIX,PP_NFC_*_VCASCHI,PP_NFC_*_VCASLO	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_VREF	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_AVDD	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*_VUP	Y
	PWR_SHAPE	P	PWR_SHAPE	NFC_P_ANT_POS, NFC_P_ANT_NEG	Y
	PWR_SHAPE	P	PWR_SHAPE	NFC_P_ANT_POS, NFC_P_ANT_NEG	Y
Arrow	PWR_SHAPE	P	PWR_SHAPE	PP1V8_S4	Y
	PWR_SHAPE	P	PWR_SHAPE	PP1V8_R1_ANA_S4	Y
QETs/APTs	PWR_SHAPE	P	PWR_SHAPE	PP_APT_L_PA	Y
Radio	PWR_100UM	P	PWR_100UM	PP_VDD_RF_1V2	Y
	PWR_100UM	P	PWR_100UM	PP_VIO_RFFE*_1V8*,PP_RFFE*1V8*	Y
	PWR_80UM	P	PWR_80UM	PP_1V8_LDO6	Y
	PWR_80UM	P	PWR_80UM	PP_UIM1_LDO11	Y
	PWR_80UM	P	PWR_80UM	PP_UIM2_LDO13	Y
	PWR_100UM	P	PWR_100UM	PP_QET1_VDD_AMP*	Y
	PWR_100UM	P	PWR_100UM	PP_QET1_VAUX_S	Y
	PWR_100UM	P	PWR_100UM	PP_QET1_PA_VBAT_LDO	Y
	PWR_100UM	P	PWR_100UM	PP_QET1_AMP_OUT	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_QET1_PA	Y
	PWR_100UM	P	PWR_100UM	SUBUS_UAT_A*	Y
	PWR_100UM	P	PWR_100UM	SUBUS_UAT_B*	Y
	PWR_100UM	P	PWR_100UM	SUBUS_LAT_B*	Y
	PWR_100UM	P	PWR_100UM	SUBUS_LAT_C*	Y

DOMAIN	NET RULE ASSIGNMENT	
B.P.SI	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	ANALOG_NAND_ZQ*

SYNC_MASTER=temp SYNC_DATE=07/01/2019

PAGE TITLE

CONSTRAINTS: Power

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SIZE	D
REVISION	10.0.0
BRANCH	1
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Power Spacing

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GND	S	MSAP_YIELD	GND	Y
PWR_DEFAULT	S	DEFAULT	=	Y
PWR_50UM	S	DEFAULT	=	Y
PWR_80UM	S	DEFAULT	=	Y
PWR_100UM	S	DEFAULT	=	Y
PWR_200UM	S	DEFAULT	=	Y
PWR_300UM	S	DEFAULT	=	Y
PWR_SHAPE	S	DEFAULT	=	Y
PWR_100UM_HV	S	HV_SPACING	=	Y
PWR_SHAPE_LX	S	NA_DIELECTRIC_2X_LX	=	Y
PWR_100UM_LX	S	NA_DIELECTRIC_2X_LX	=	Y
PWR_SHAPE_LX_DPMIC	S	NA_DIELECTRIC_2X_LX	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_100UM	GND	100UM-249UM_SPACING
PWR_100UM	PWR_100UM	100UM-249UM_SPACING
PWR_100UM	PWR_200UM	100UM-249UM_SPACING
PWR_100UM	PWR_300UM	100UM-249UM_SPACING
PWR_100UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_200UM	GND	100UM-249UM_SPACING
PWR_200UM	PWR_200UM	100UM-249UM_SPACING
PWR_200UM	PWR_300UM	100UM-249UM_SPACING
PWR_200UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_300UM	GND	250UM+_SPACING
PWR_300UM	PWR_300UM	250UM+_SPACING
PWR_SHAPE	GND	250UM+_SPACING
PWR_SHAPE	PWR_SHAPE	250UM+_SPACING
PWR_100UM_HV	GND	DEFAULT

Diff Pair Constraints

Electrical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
E_DP_GENERIC	E	GENERIC_DP	DP:DP_CODEC_AOUT*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_MIC*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_PENROSE*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_NTC_*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_*MTR*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_ANALOG*SENSE*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_ANALOG_VIN_SAKONNET_FROM_HALL*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_PMU_VDD_MAIN_SENSE*	Y
E_DP_NC	E	GENERIC_DP	DP:DP_NC*	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_PWR	P	PWR_DP	DP:DP_CODEC_AOUT*	Y
DP_MIC	P	GENERIC_DP	DP:DP_*MIC*	Y
DP_PENROSE	P	GENERIC_DP	DP:DP_PENROSE*	Y
DP_NTC	P	GENERIC_DP	DP:DP_NTC_*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_*MTR*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_ANALOG*GPU_SENSE*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_ANALOG*SOC_SENSE*	Y
DP_PCPU_SENSE	P	GENERIC_DP	DP:DP_ANALOG*PCPU_SENSE*	Y
DP_SAKONNET	P	GENERIC_DP	DP:DP_ANALOG_VIN_SAKONNET_FROM_HALL*	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_PMU_VDD_MAIN_SENSE*	Y
DP_NC	P	GENERIC_DP	DP:DP_NC*	Y
DP_ETDAC_QET1	P	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_PWR	S	DEFAULT	=	Y
DP_MIC	S	A_DIELECTRIC_1.5X	=	Y
DP_PENROSE	S	A_DIELECTRIC_1.5X	=	Y
DP_NTC	S	A_DIELECTRIC_1.5X	=	Y
DP_SAKONNET	S	A_DIELECTRIC_1.5X	=	Y
DP_PCPU_SENSE	S	A_DIELECTRIC_1.5X	=	Y
DP_GENERIC	S	DEFAULT	=	Y
DP_NC	S	DEFAULT	=	Y
DP_ETDAC_QET1	S	A_DIELECTRIC_1.5X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
DP_MIC	DP_MIC	DEFAULT
DP_MIC	GND	DEFAULT
DP_MIC	PWR_MIC	DEFAULT
DP_MIC	DP_SAKONNET	DEFAULT
DP_MIC	ANALOG_SAKONNET	DEFAULT
DP_SAKONNET	DP_SAKONNET	DEFAULT
DP_SAKONNET	ANALOG_SAKONNET	DEFAULT
DP_SAKONNET	GND	DEFAULT
CLK	GND	DEFAULT
ANALOG	GND	DEFAULT
ANALOG_NTC	GND	DEFAULT
ANALOG_SAKONNET	GND	DEFAULT
ANALOG_AMP_FILT	GND	DEFAULT

Clocks

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	P	DEFAULT	CLK_*	Y
CLK	P	DEFAULT	SPMI*CLK*	Y
CLK	P	DEFAULT	I2S*MCLK*	Y
CLK	P	DEFAULT	SPI*SCLK*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	S	A_DIELECTRIC_1.5X	=	Y

Sensitive Analog

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG_SAKONNET	P	DEFAULT	ANALOG*SAKONNET_TO_HALL*	Y
ANALOG	P	DEFAULT	ANALOG*DOTARA*	Y
ANALOG	P	DEFAULT	ANALOG*DOMBRA*	Y
ANALOG	P	DEFAULT	ANALOG*SENSE,ANALOG*SENSE_SE,ANALOG*SENSE_FILT	Y
ANALOG	P	DEFAULT	ANALOG*ZQ*	Y
ANALOG	P	DEFAULT	ANALOG*REXT*	Y
ANALOG	P	DEFAULT	ANALOG*CAL*	Y
ANALOG	P	DEFAULT	ANALOG_*REF*	Y
ANALOG	P	DEFAULT	ANALOG_FB*	Y
ANALOG	P	DEFAULT	ANALOG*PDTS*	Y
ANALOG	P	DEFAULT	ANALOG_KRAKEN_BYPASS	Y
GRP_GPIO	P	DEFAULT	ANALOG_KRAKEN_BI_CCG2B_CC	Y
ANALOG	P	DEFAULT	ANALOG_RIGEL_LSCP	Y
ANALOG_AMP_FILT	P	PWR_80UM	ANALOG_*_SPK_FILT,ANALOG_ARC_FILT	Y
ANALOG	P	DEFAULT	VSS_PMU_XTAL	Y
ANALOG	P	DEFAULT	AMUX*	Y
ANALOG_NTC	P	DEFAULT	NTC_STROBE_MODULE*	Y
ANALOG_NTC	P	DEFAULT	NTC_PEARL_VCSEL_TO_RIGEL	Y
ANALOG_NTC	P	DEFAULT	NTC_STOCKHOLM	Y
ANALOG	P	DEFAULT	COIL_TO_SPKRAMP_*_VSENSE_*, SOLENOID_TO_ARCAMP_VSENSE_*	Y
PWR_MIC	P	PWR_DEFAULT	PP_CODEC_TO_MIC*_BIAS*,RET_CODEC_FROM_MIC*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_AMP_FILT	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_NTC	S	A_DIELECTRIC_1.5X	=	Y
ANALOG_SAKONNET	S	A_DIELECTRIC_1.5X	=	Y
PWR_MIC	S	DEFAULT	=	Y

Grouping Constraints

Physical

Used to clean up CM

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	P	DEFAULT	GPIO*, IO_*	Y
GRP_NC	P	DEFAULT	NC_*	Y
GRP_I2C	P	DEFAULT	I2C*	Y
GRP_I2S	P	DEFAULT	I2S*LRCLK*, I2S*BCLK*, I2S*DOUT*, I2S*DIN*	Y
GRP_SPI	P	DEFAULT	SPI*MOSI*, SPI*MISO*, SPI*CS*	Y
GRP_UART	P	DEFAULT	UART*	Y
GRP_SWD	P	DEFAULT	SWD*	Y
GRP_SPMI_DATA	P	DEFAULT	SPMI*DATA*	Y
GRP_PCIE_SIDE	P	DEFAULT	PCIE*CLKREQ*, PCIE*PERST*	Y
GRP_LPDP_AUX	P	DEFAULT	LPDP*AUX*	Y
GRP_RFFE_WLAN	P	DEFAULT	RFFE_WLAN_*	Y
GRP_RFFE_BB	P	DEFAULT	SHIELD_RFFE*	Y
GRP_CODEC_FILT	P	PWR_200UM	CODEC_*FILTP,CODEC_*FILTN	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	S	DEFAULT	=	Y
GRP_NC	S	DEFAULT	=	Y
GRP_I2C	S	DEFAULT	=	Y
GRP_I2S	S	DEFAULT	=	Y
GRP_SPI	S	DEFAULT	=	Y
GRP_UART	S	DEFAULT	=	Y
GRP_SWD	S	DEFAULT	=	Y
GRP_SPMI_DATA	S	DEFAULT	=	Y
GRP_PCIE_SIDE	S	DEFAULT	=	Y
GRP_LPDP_AUX	S	DEFAULT	=	Y
GRP_RFFE_WLAN	S	DEFAULT	=	Y
GRP_RFFE_BB	S	DEFAULT	=	Y
GRP_CODEC_FILT	S	DEFAULT	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_SHAPE_LX	GND	DEFAULT
PWR_SHAPE_LX	PWR_SHAPE_LX	DEFAULT
PWR_SHAPE_LX	ANALOG	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_AMP_FILT	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_NTC	A_DIELECTRIC_3X
PWR_SHAPE_LX	ANALOG_SAKONNET	A_DIELECTRIC_3X
PWR_SHAPE_LX	CLK	A_DIELECTRIC_3X
PWR_100UM_LX	GND	DEFAULT
PWR_SHAPE_LX_DPMIC	GND	A_DIELECTRIC_3X

SYNC_MASTER=temp SYNC_DATE=07/01/2019

PAGE TITLE

CONSTRAINTS: Misc.

DRAWING NUMBER 051-05170 SIZE D

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50 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
ISL2	TOP,ISL3	50	0.029
ISL6	ISL7,ISL5	50	0.038
ISL8	ISL9,ISL7	50	0.029
BOTTOM	ISL9	50	0.057

50 Wide

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
ISL6	ISL4,ISL8	50	0.098
ISL7	ISL9,ISL5	50	0.092
ISL8	BOTTOM,ISL6	50	0.085
BOTTOM	ISL8	50	0.167

50 Wide, External Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_SURFACE_THIN		ZONE NAME= PRIMARY	
ISL6	ISL4,ISL8	50	0.098
ISL7	ISL9,ISL5	50	0.092
ISL8	BOTTOM,ISL6	50	0.085
BOTTOM	ISL9	50	0.057

50 Wide, L8 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_L8_THIN		ZONE NAME= PRIMARY	
ISL6	ISL4,ISL8	50	0.098
ISL7	ISL9,ISL5	50	0.092
ISL8	ISL9,ISL7	50	0.029
BOTTOM	ISL8	50	0.167

50 Wide, L6 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_L6_THIN		ZONE NAME= PRIMARY	
ISL6	ISL7,ISL5	50	0.038
ISL7	ISL9,ISL5	50	0.092
ISL8	BOTTOM,ISL6	50	0.085
BOTTOM	ISL8	50	0.167

50-ohm (Wide) Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Cellular	P	A_50_WIDE_SE	50_TRX_ANT4*	Y
	P	A_50_WIDE_SE	50_TRX_ANT7*	Y
	P	A_50_WIDE_SE	50_TRX_ANT9*	Y
	P	A_50_WIDE_SE	50_TRX_LB_PAD_*	Y
	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	Y
	P	A_50_WIDE_SE	50_TRX_LB_PORTB_RX1	Y
	P	A_50_WIDE_SE	50_TRX_LB_PORTB_RX1_M	Y
	P	A_50_WIDE_SE	50_TRX_LB_PORTB_TX_M	Y
	P	A_50_WIDE_SE	50_TRX_L5_LNA_IN,50_TRX_ANT3_L5	Y
	P	A_50_WIDE_SE	50_TRX_PAUHBL_UHB_ANT1_TO_ANT7_M	Y
	P	A_50_WIDE_SE	50_TRX_PAUHBL_N79_ANT2_TO_ANT9*	Y
	P	A_50_WIDE_SE	50_TRX_PAUHBL_N79_ANT1_TO_ANT7*	Y
	P	A_50_WIDE_SE	50_TRX_UHB_PAD_PORTB_TX_M	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_UHB_PAD_N79_PORTB_TX_M	Y
	P	A_50_WIDE_SE	50_TRX_UHB_PAD_PORTB_TX	Y
	P	A_50_WIDE_SE	50_TRX_CPLR_L_CPL2_IN_LB_LMB_MB_HB	Y
	P	A_50_WIDE_SE	50_TRX_HB_PAD_ANT1_M	Y
Arrow	P	A_50_WIDE_SE	50_TRX_R1_AOA1	Y
	P	A_50_WIDE_SE	50_TRX_R1_AOA2	Y
	P	A_50_WIDE_SE	50_R1_ANT*	Y
	P	A_50_WIDE_SE	50_UWB_ANT*	Y
	P	A_50_WIDE_SE	50_TRX_ANT6_WLAN_A_LAA	Y
WiFi	P	A_50_WIDE_SE	50_R1_WLAN_A_LAA_M	Y
	P	A_50_WIDE_SE	50_TRX_ANT5_WLAN_A_LAA	Y
	P	A_50_WIDE_SE	50_WLAN_A_LAA_DPLXR	Y
	P	A_50_WIDE_SE	50_WLAN_A_LAA_BPF_M	Y
	P	A_50_WIDE_SE	50_WLAN_A_LAA_BPF	Y
	P	A_50_WIDE_SE	50_TRX_PAUHBU_N79_ANT2_TO_ANT8*	Y
	P	A_50_WIDE_SE	50_TRX_PAUHBL_N79_ANT2_TO_ANT8*	Y
	P	A_50_WIDE_SE	50_TRX_PAUHBL_N77_ANT2_TO_ANT8*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_WIDE	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_TRX_WIDE	GND	NA_DIELECTRIC_2X_50_WIDE_SE
50_TRX_WIDE_SURFACE_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_SURFACE_THIN_SE
50_TRX_WIDE_L8_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_L8_THIN_SE
50_TRX_WIDE_L6_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_L6_THIN_SE

50-ohm (Thin) Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
Wildcards	P	A_50_THIN_SE	50_RX_*	Y
50_RX_THIN	P	A_50_THIN_SE	50_LAA_RX_XCVR_PRX12	Y
Direct Net	P	A_50_THIN_SE	50_TX_IN_XCVR_TX0_LB	Y
50_TX0_THIN	P	A_50_THIN_SE	50_TX_IN_TX0_LB_PAD_TX_LB_IN	Y
50_TX0_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_XCVR_TX1_LB_JB	Y
50_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_XCVR_TX1_LB_JB_M	Y
50_TX2_THIN	P	A_50_THIN_SE	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	Y
50_TX2_THIN	P	A_50_THIN_SE	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	Y
50_RX_THIN	P	A_50_THIN_SE	50_L5_LNA_NOTCH1	Y
50_TRX_THIN	P	A_50_THIN_SE	50_UHB_L_CPLR_OUT	Y
50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_C0_TXRX_FEM_M	Y
50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_UAT_TXRX_FEM	Y
50_TRX_THIN	P	A_50_THIN_SE	50_TRX_ANT2_LB_LMB_MB_HB_L1	Y
50_TRX_THIN	P	A_50_THIN_SE	50_TRX_R1_AOA3	Y
50_TRX_THIN	P	A_50_THIN_SE	50_TRX_UHB_PAD_N79_PORTB_TX	Y
50_TRX_THIN	P	A_50_THIN_SE	50_WLAN_A_LAA_ANT5_B2B_M	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TX_IN_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX0_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX0_TX1_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX1_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TX2_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_RX_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
50_TRX_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y

50-ohm Thin Overrides

DOMAIN, B.P.S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_TRX_LB_PAD_ANT1_M
P	A_50_THIN_SE	50_TRX_ANT3_L5
P	A_50_THIN_SE	50_TRX_DPLX_LB_LMB_MB_HB_ANT1
P	A_50_THIN_SE	50_TRX_ANT7_UHB_N79_M
P	A_50_THIN_SE	50_TRX_ANT7_UHB_N79_L
P	A_50_THIN_SE	50_TRX_ANT7_UHB_N79_NOTCH
P	A_50_THIN_SE	50_TRX_ANT8_UHB_N79_L
P	A_50_THIN_SE	50_TRX_ANT8_UHB_N79_NOTCH
P	A_50_THIN_SE	50_TRX_ANT9_UHB_N79_L
P	A_50_THIN_SE	50_TRX_ANT9_UHB_N79_NOTCH
P	A_50_THIN_SE	50_TRX_CPLR_L_CPL2_ANT_LMB_MB_HB_M

DOMAIN, B.P.S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_LB_PAD_ANT1_M
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT3_L5
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_DPLX_LB_LMB_MB_HB_ANT1
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT7_UHB_N79_M
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT7_UHB_N79_L
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT7_UHB_N79_NOTCH
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT8_UHB_N79_L
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT8_UHB_N79_NOTCH
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT9_UHB_N79_L
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_ANT9_UHB_N79_NOTCH
S	NA_DIELECTRIC_4XV_50_THIN_SE	50_TRX_CPLR_L_CPL2_ANT_LMB_MB_HB_M

50-ohm (Hybrid) Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_PAUHBL_UHB_ANT1_TO_ANT7	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_A_C1_TXRX_FEM_M	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_WLAN_G_BT_ANT3_NPLXR	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9_M	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_CPLR_L_CPL2_ANT_LB_LMB_MB_HB	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_WLAN_G_BT_ANT3_NPLXR_M	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_R1_ANT2_CH9	Y
50_TRX_WIDE_SURFACE_THIN	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_ANT8_UHB_N79_M	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_CPLR_L_CPL3_ANT_LMB_MB_HB	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_LB_PORTB_TX_ANT2	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_WLAN_A_LAT_TXRX_FEM	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_ANT1_LB_LMB_MB_HB	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_ANT8_R1_UHB_N79	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_WLAN_A_LAA_DPLXR_M	Y
50_TRX_WIDE_L8_THIN	P	A_50_WIDE_L8_THIN_SE	50_TRX_R1_ANT2_CH5	Y
50_TRX_WIDE_L6_THIN	P	A_50_WIDE_L6_THIN_SE	50_LAA_RX_XCVR_DRX10	Y
50_TRX_WIDE_L6_THIN	P	A_50_WIDE_L6_THIN_SE	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_TRX_WIDE_SURFACE_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_SURFACE_THIN_SE	=	Y
50_TRX_WIDE_L8_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_L8_THIN_SE	=	Y
50_TRX_WIDE_L6_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_L6_THIN_SE	=	Y

(Thin) Class-Class Spacing

	CLASS TO CLASS SPACING		
	CLASS NAME	CLASS NAME	CONSTRAINT SET
Same Class	50_TX0_THIN	50_TX0_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX0_TX1_THIN	50_TX0_TX1_THIN	DEFAULT
	50_TX1_THIN	50_TX1_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	50_TX2_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	50_RX_THIN	NA_DIELECTRIC_2X_50_THIN_SE
GND	50_TX0_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX0_TX1_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TRX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
TX <-> TX	50_TX0_THIN	50_TX0_TX1_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX0_THIN	50_TX1_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX0_THIN	50_TX2_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX1_THIN	50_TX0_TX1_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX1_THIN	50_TX2_THIN	NA_DIELECTRIC_4XV_50_THIN_SE
	50_TX2_THIN	50_TX0_TX1_THIN	NA_DIELECTRIC_4XV_50_THIN_SE

SYNC_DATE=07/01/2019

PAGE TITLE: CONSTRAINTS: 50-Ohm

DRAWING NUMBER: 051-05170 | SIZE: D

REVISION: 10.0.0

BRANCH: 1

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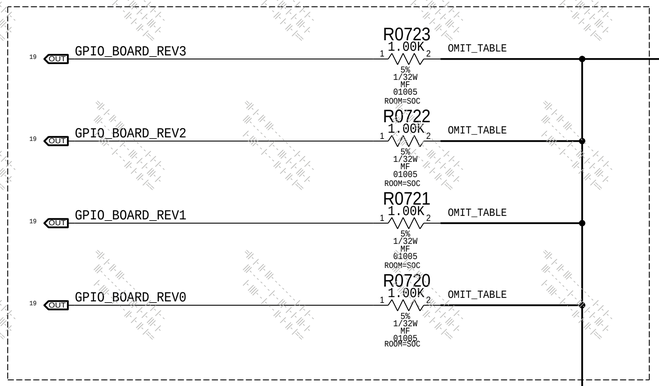
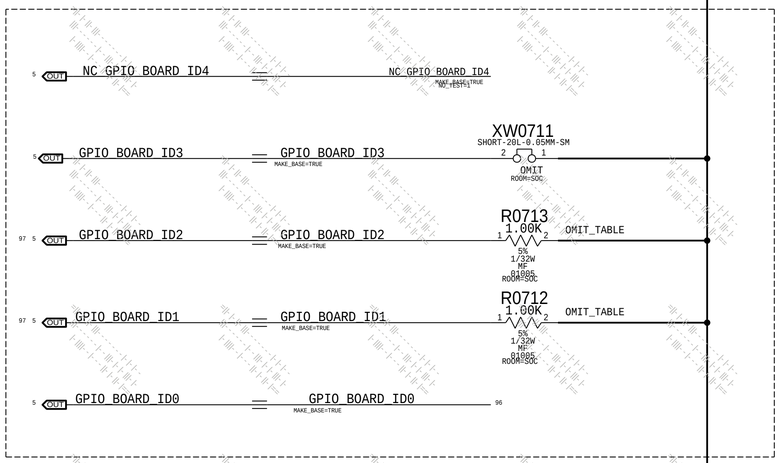
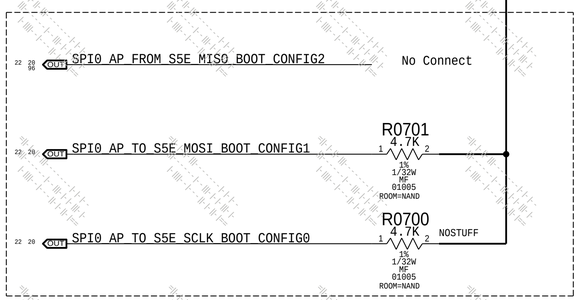
BOOTSTRAPPING

BOARD REV + BOARD ID + BOOT CONFIG







Board Rev [3:0]

* Float = 0 | PU = 1

Note: iBoot uses the inverse of BOARD_REV[3:0], so that it counts up (Pre-Proto = 0x0, PVT = 0xF)

	BOARD_REV[3:0]	[3]	[2]	[1]	[0]
Pre-Proto	4'b1111	1	1	1	1
Proto 1	4'b1110	1	1	1	0
Proto 1.5	4'b1101	1	1	0	1
Proto 2	4'b1100	1	1	0	0
Proto 2.5	4'b1011	1	0	1	1
Pre-EVT	4'b1010	1	0	1	0
EVT	4'b1001	1	0	0	1
Carrier	4'b1000	1	0	0	0

(Allocate more as necessary in descending order)

DVT	4'b0001	0	0	0	1
PVT	4'b0000	0	0	0	0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
117S0156	4	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0721,R0720	BOARD_REV:PROTO0	PROTO0
117S0156	3	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0721	BOARD_REV:PROTO1	PROTO1
117S0156	3	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722,R0720	BOARD_REV:PROTO1.5	PROTO1.5
117S0156	2	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0722	BOARD_REV:PROTO2	PROTO2
117S0156	3	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0721,R0720	BOARD_REV:PROTO2.5	PROTO2.5
117S0156	2	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0721	BOARD_REV:PRE-EVT	PRE-EVT
117S0156	2	RES,MF,1K OHM,5%,1/32W,01005	R0723,R0720	BOARD_REV:EVT	EVT
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0723	BOARD_REV	
		RES,MF,1K OHM,5%,1/32W,01005	R0720	BOARD_REV:DVT	DVT

(PVT NOSTUFF ALL)

Board ID [4:0]

* Float = 0 | PU = 1

	BOARD_ID[4:0]	[4] Unused	[3] 1=MAV20	[2]	[1]	[0] 0=, 1=DEV
D52G	5'b01010	0	1	0	1	0
DEV D52G	5'b01011	0	1	0	1	1
D53G	5'b01100	0	1	1	0	0
DEV D53G	5'b01101	0	1	1	0	1
D53P	5'b01110	0	1	1	1	0
DEV D53P	5'b01111	0	1	1	1	1
D54P	5'b01000	0	1	0	0	0
DEV D54P	5'b01001	0	1	0	0	1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0712	BOARD_ID:D52	D52 = 01
117S0156	1	RES,MF,1K OHM,5%,1/32W,01005	R0713	BOARD_ID:D53G	D53G = 10
117S0156	2	RES,MF,1K OHM,5%,1/32W,01005	R0713,R0712	BOARD_ID:D53P	D53P = 11
(D54 both NOSTUFF)					D54 = 00

Boot Config [2:0]

* Float = 0 | PU = 1

	USAGE	SPEED	TEST	[2]	[1]	[0]	
SPI1 NOR	--	12MHz	--	0	0	0	
SPI1 NOR	--	12MHz	Test	0	0	1	
SPI0 NAND	POR	12MHz	--	0	1	0	<-- POR
SPI0 NAND	Proto	12MHz	Test	0	1	1	<-- Proto Builds
SPI1 NOR	--	24MHz	--	1	0	0	
SPI1 NOR	--	24MHz	Test	1	0	1	
SPI1 NOR	--	6MHz	--	1	1	0	
SPI1 NOR	--	6MHz	Test	1	1	1	

<--- Remove at EVT

PAGE TITLE
SYSTEM: Bootstrapping

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Conventions:

1. Nets which are not connected on FFs but probed out on dev board should start with "NC_DEV_"
2. Nets that contain "_1V8" are 1.8V logic, all other nets are implied 1.2V logic
3. Components with PACK_IGNORE=TRUE will not be included in the netlist

SB0801
STDOFF-2.560D1.4ID-0.855H-SM
860-01491
ROOM=MECHANICAL

SB0802
STDOFF-2.560D1.4ID-0.855H-SM
860-01491
ROOM=MECHANICAL

SB0803
STDOFF-2.560D1.4ID-0.855H-SM
860-01491
ROOM=MECHANICAL

SB0804
STDOFF-2.560D1.4ID-0.855H-SM
860-01491
ROOM=MECHANICAL

SB0805
STDOFF-2.560D1.4ID-0.855H-SM
860-01491
ROOM=MECHANICAL

FD0800
FID
0P5SQ-CROSS-NSP
998-04808
ROOM=ASSEMBLY

FD0801
FID
0P5SQ-CROSS-NSP
998-04808
ROOM=ASSEMBLY

FD0802
FID
0P5SQ-CROSS-NSP
998-04808
ROOM=ASSEMBLY

FD0803
FID
0P5SQ-CROSS-NSP
998-04808
ROOM=ASSEMBLY

FD0804
FID
0P5SQ-CROSS-NSP
998-04808
ROOM=ASSEMBLY

FD0805
FID
0P5SQ-CROSS-NSP
998-04808
ROOM=ASSEMBLY

FD0810
FID
0P5SQ-SMP3SQ-NSP
998-00557
ROOM=ASSEMBLY

FD0811
FID
0P5SQ-SMP3SQ-NSP
998-00557
ROOM=ASSEMBLY

FD0812
FID
0P5SQ-SMP3SQ-NSP
998-00557
ROOM=ASSEMBLY

FD0813
FID
0P5SQ-SMP3SQ-NSP
998-00557
ROOM=ASSEMBLY

FD0814
FID
0P5SQ-SMP3SQ-NSP
998-00557
ROOM=ASSEMBLY

FD0815
FID
0P5SQ-SMP3SQ-NSP
998-00557
ROOM=ASSEMBLY

SHIELDS

CRITICAL
SH0800
SM
806-23495
SHLD-TTS-SOUTH-D54

CRITICAL
SH0801
SM
806-26434
SHLD-TTS-MID-TALL-D54

CRITICAL
SH0802
SM
806-23493
SHLD-TTS-NORTH-D54

SOC UF

R0800 0.00 0% 1/32W MF 01005 ROOM=DFM
R0801 0.00 0% 1/32W MF 01005 ROOM=DFM
R0802 0.00 0% 1/32W MF 01005 ROOM=DFM
R0803 0.00 0% 1/32W MF 01005 ROOM=DFM
R0804 0.00 0% 1/32W MF 01005 ROOM=DFM
R0805 0.00 0% 1/32W MF 01005 ROOM=DFM
R0806 0.00 0% 1/32W MF 01005 ROOM=DFM
R0809 0.00 0% 1/32W MF 01005 ROOM=DFM
R0810 0.00 0% 1/32W MF 01005 ROOM=DFM

NAND UF

R0807 0.00 0% 1/32W MF 01005 ROOM=DFM
R0808 0.00 0% 1/32W MF 01005 ROOM=DFM

Interposer Spacers

RefDes called out below

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-03604	20	SPACER,INTERPOSER,SMALL,X891		CRITICAL	?

SP0801, SP0802, SP0803, SP0804, SP0805, SP0806, SP0807, SP0808, SP0809, SP0810, SP0811, SP0812, SP0813, SP0814, SP0815, SP0816, SP0817, SP0818, SP0819, SP0820

PAGE TITLE
SYSTEM: Mechanical

DRAWING NUMBER 051-05170 SIZE D
REVISION 10.0.0
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SOC

4GB DRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22473	1	Sicily,B1,4GB,M	U1000	CRITICAL	BOARD_ID:0528BOARD_ID:0536

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-22472	998-22473	BOARD_ID:0528BOARD_ID:0536	U1000	Sicily,B1,4GB,H
998-22471	998-22473	BOARD_ID:0528BOARD_ID:0536	U1000	Sicily,B1,4GB,S

6GB DRAM

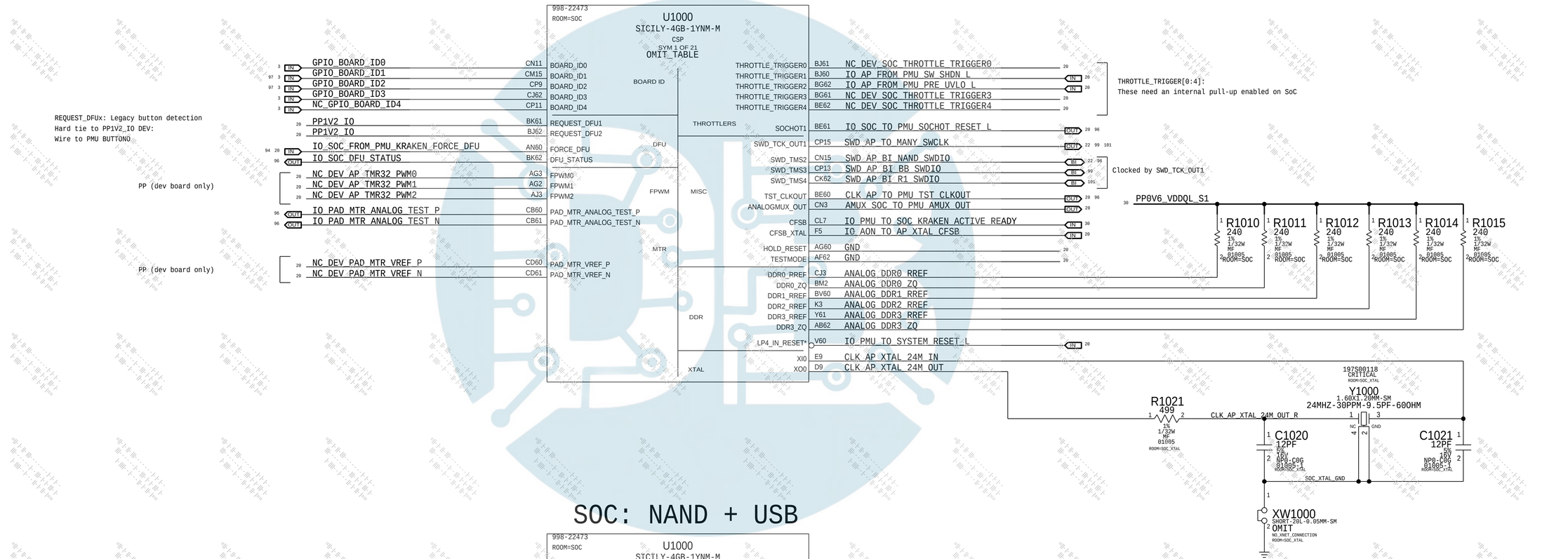
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22474	1	Sicily,B1,6GB,M	U1000	CRITICAL	BOARD_ID:053FBOARD_ID:054

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-22475	998-22474	BOARD_ID:053FBOARD_ID:054	U1000	Sicily,B1,6GB,H
998-22476	998-22474	BOARD_ID:053FBOARD_ID:054	U1000	Sicily,B1,6GB,S

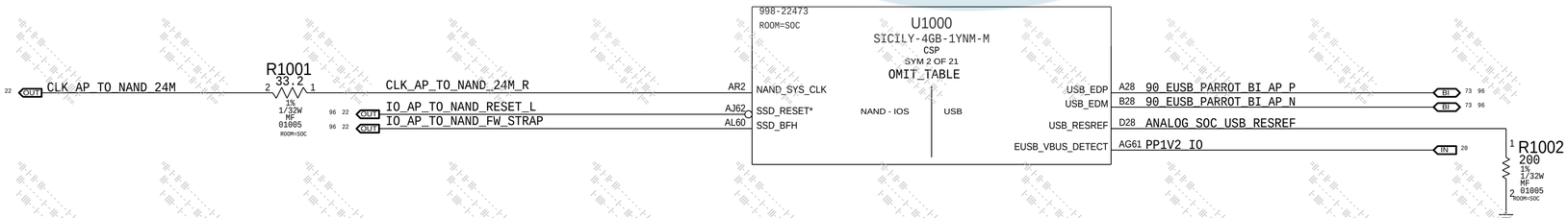
24M XTAL Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0612	197S00118	?	Y1000	XTAL, 24M, 1612
197S00120	197S00118	?	Y1000	XTAL, 24M, 1612

SOC: Misc



SOC: NAND + USB



SYNCING: D52, D53, D54

PAGE TITLE
SOC: NAND + USB & Misc

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BRANCH 1
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SOC: PCIe

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 3 OF 21
OMIT_TABLE

LINK0 | LINK1 | LINK2

PCIE GEN4 - ST LINK 0

- NC_DEV_PCIE_GP0_AP_CLKREQ_L → GP_PCIE_CLKREQ0* (CB3)
- ST_PCIE_CLKREQ0* (CB2) → PCIE_ST0_AP_BI_NAND_CLKREQ_L
- R1100 47.0K 5% 1/32W MF 01005 ROOM=SOC (PP1V2_IO → PCIE_ST0_AP_BI_NAND_CLKREQ_L)
- NC_DEV_PCIE_GP0_AP_RX_P (B15) / NC_DEV_PCIE_GP0_AP_RX_N (A15) → GP_PCIE_RX0_P / GP_PCIE_RX0_N
- ST_PCIE_RX0_P (B11) / ST_PCIE_RX0_N (A11) ← 90_PCIE_ST0_AP_FROM_NAND_C_RX_P / _N
- RX CAPS LIVE OFF-PAGE
- NC_DEV_PCIE_GP0_AP_TX_P (C17) / NC_DEV_PCIE_GP0_AP_TX_N (D17) ← GP_PCIE_TX0_P / GP_PCIE_TX0_N
- ST_PCIE_TX0_P (C13) / ST_PCIE_TX0_N (D13) → 90_PCIE_ST0_AP_TO_NAND_C_TX_P / _N
- C1102 0.22UF CER-X5R 10% 6.3V 01005 GND_VOID ROOM=SOC (90_PCIE_ST0_AP_TO_NAND_C_TX_P → 90_PCIE_ST0_AP_TO_NAND_TX_P)
- C1103 0.22UF CER-X5R 10% 6.3V 01005 GND_VOID ROOM=SOC (90_PCIE_ST0_AP_TO_NAND_C_TX_N → 90_PCIE_ST0_AP_TO_NAND_TX_N)
- NC_DEV_PCIE_GP0_AP_RESET_L (CF2) → GP_PCIE_PERST0*
- ST_PCIE_PERST0* (CD3) → PCIE_ST0_AP_TO_NAND_PERST_L
- R1101 47.0K 5% 1/32W MF 01005 ROOM=SOC (PCIE_ST0_AP_TO_NAND_PERST_L → PP1V2_IO)
- R1130 47.0K 5% 1/32W MF 01005 ROOM=SOC (PP1V2_IO → PCIE_GP1_AP_BI_WLAN_CLKREQ_L)
- PCIE_GP1_AP_BI_WLAN_CLKREQ_L (CB4) → GP_PCIE_CLKREQ1*
- GP_PCIE_CLKREQ2* (CD2) → PCIE_GP2_AP_BI_BB_CLKREQ_L
- BB CLKREQ PULL-UP LIVES IN RADIO HIERARCHY

PCIE GEN2 - LINK 1

- RX CAPS LIVE OFF-PAGE
- 90_PCIE_GP1_AP_FROM_WLAN_C_RX_P (B19) / _N (A19) → GP_PCIE_RX1_P / GP_PCIE_RX1_N
- GP_PCIE_RX2_P (B22) / GP_PCIE_RX2_N (A22) ← 90_PCIE_GP2_AP_FROM_BB_RX_P / _N
- RX CAPS LIVE OFF-PAGE
- C1112 0.1UF X5R-CERM 20% 6.3V 01005 GND_VOID ROOM=SOC (90_PCIE_GP1_AP_TO_WLAN_C_TX_P → 90_PCIE_GP1_AP_TO_WLAN_TX_P)
- C1113 0.1UF X5R-CERM 20% 6.3V 01005 GND_VOID ROOM=SOC (90_PCIE_GP1_AP_TO_WLAN_C_TX_N → 90_PCIE_GP1_AP_TO_WLAN_TX_N)
- GP_PCIE_TX1_P (C21) / GP_PCIE_TX1_N (D21) → 90_PCIE_GP1_AP_TO_WLAN_C_TX_P / _N
- GP_PCIE_TX2_P (C24) / GP_PCIE_TX2_N (D24) ← 90_PCIE_GP2_AP_TO_BB_C_TX_P / _N
- C1122 0.22UF CER-X5R 10% 6.3V 01005 GND_VOID ROOM=SOC (90_PCIE_GP2_AP_TO_BB_C_TX_P → 90_PCIE_GP2_AP_TO_BB_TX_P)
- C1123 0.22UF CER-X5R 10% 6.3V 01005 GND_VOID ROOM=SOC (90_PCIE_GP2_AP_TO_BB_C_TX_N → 90_PCIE_GP2_AP_TO_BB_TX_N)
- PCIE_GP1_AP_TO_WLAN_PERST_L (CF4) → GP_PCIE_PERST1*
- GP_PCIE_PERST2* (CF3) → PCIE_GP2_AP_TO_BB_PERST_L
- R1131 100K 5% 1/32W MF 01005 ROOM=SOC (PCIE_GP1_AP_TO_WLAN_PERST_L → GND)
- R1121 100K 5% 1/32W MF 01005 ROOM=SOC (PCIE_GP2_AP_TO_BB_PERST_L → GND)

PCIE GEN4 - LINK 2

- ANALOG_PCIE_RCAL_POS (E19) → PCIE_RCAL_P
- R1140 200 1% 1/32W MF 01005 ROOM=SOC NO_XNET_CONNECTION=1 (PCIE_RCAL_P → PCIE_RCAL_N)
- ANALOG_PCIE_RCAL_NEG (F19) → PCIE_RCAL_N
- C1140 10PF 5% 10V NP0/C0G 01005 ROOM=SOC (PCIE_RCAL_N → GND)
- GP_PCIE_REF_CLK0_P (A7) / GP_PCIE_REF_CLK0_N (B7) → NC_DEV_PCIE_GP0_AP_REFCLK_P / _N
- GP_PCIE_REF_CLK1_P (B5) / GP_PCIE_REF_CLK1_N (A5) → 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P / _N
- GP_PCIE_REF_CLK2_P (B4) / GP_PCIE_REF_CLK2_N (A4) → 90_PCIE_GP2_AP_TO_BB_REFCLK_P / _N
- ST_PCIE_REF_CLK0_P (B6) / ST_PCIE_REF_CLK0_N (A6) → 90_PCIE_ST0_AP_TO_NAND_REFCLK_P / _N

SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: PCIE
DRAWING NUMBER	051-05170
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SOC: ISP

DO NOT SWIZZLE LPDP LANES UNLESS ROUTING NECESSITATES IT
LPDP Swizzle Options:
-P/N can be switched
-Non-sequential lanes can be grouped
(e.g. FCAM 0 -> SOC 5, FCAM 1 -> SOC 2)
-AUX pin (one per device) doesn't have to match lane numbers

Note: LPDP RX and AUX lanes need a series 0.1uF cap

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 4 OF 21
OMIT_TABLE

LPDP-RX

21 IN	90_LPDP_ISP_FROM_WIDE_RX_D0_N	CP19	LPDPRX_RX_D0_P
21 IN	90_LPDP_ISP_FROM_WIDE_RX_D0_P	CN19	LPDPRX_RX_D0_N
21 IN	90_LPDP_ISP_FROM_WIDE_RX_D1_N	CN21	LPDPRX_RX_D1_P
21 IN	90_LPDP_ISP_FROM_WIDE_RX_D1_P	CM21	LPDPRX_RX_D1_N
21 IN	90_LPDP_ISP_FROM_WIDE_RX_D2_N	CP22	LPDPRX_RX_D2_P
21 IN	90_LPDP_ISP_FROM_WIDE_RX_D2_P	CN22	LPDPRX_RX_D2_N
21 IN	90_LPDP_ISP_FROM_FCAM_RX_D0_N	CP26	LPDPRX_RX_D3_P
21 IN	90_LPDP_ISP_FROM_FCAM_RX_D0_P	CN26	LPDPRX_RX_D3_N
21 IN	90_LPDP_ISP_FROM_FCAM_RX_D1_N	CN28	LPDPRX_RX_D4_P
21 IN	90_LPDP_ISP_FROM_FCAM_RX_D1_P	CM28	LPDPRX_RX_D4_N
21 IN	90_LPDP_ISP_FROM_TELE_RX_D0_P	CP30	LPDPRX_RX_D5_P
21 IN	90_LPDP_ISP_FROM_TELE_RX_D0_N	CN30	LPDPRX_RX_D5_N
21 IN	90_LPDP_ISP_FROM_TELE_RX_D1_P	CN32	LPDPRX_RX_D6_P
21 IN	90_LPDP_ISP_FROM_TELE_RX_D1_N	CM32	LPDPRX_RX_D6_N
21 IN	90_LPDP_ISP_FROM_TELE_RX_D2_P	CP34	LPDPRX_RX_D7_P
21 IN	90_LPDP_ISP_FROM_TELE_RX_D2_N	CN34	LPDPRX_RX_D7_N
21 IN	90_LPDP_ISP_FROM_SWIDE_RX_D2_N	CN36	LPDPRX_RX_D8_P
21 IN	90_LPDP_ISP_FROM_SWIDE_RX_D2_P	CM36	LPDPRX_RX_D8_N
21 IN	90_LPDP_ISP_FROM_SWIDE_RX_D0_P	CN40	LPDPRX_RX_D9_P
21 IN	90_LPDP_ISP_FROM_SWIDE_RX_D0_N	CM40	LPDPRX_RX_D9_N
21 IN	90_LPDP_ISP_FROM_SWIDE_RX_D1_N	CP42	LPDPRX_RX_D10_P
21 IN	90_LPDP_ISP_FROM_SWIDE_RX_D1_P	CN42	LPDPRX_RX_D10_N
21 IN	90_LPDP_ISP_FROM_JASPER_RX_D0_P	CN43	LPDPRX_RX_D11_P
21 IN	90_LPDP_ISP_FROM_JASPER_RX_D0_N	CM43	LPDPRX_RX_D11_N

ANALOG_LPDP_ISP_RX0_RCAL_POS — CM24 — LPDPRX0_RCAL_P
ANALOG_LPDP_ISP_RX0_RCAL_NEG — CN24 — LPDPRX0_RCAL_N
ANALOG_LPDP_ISP_RX1_RCAL_POS — CN38 — LPDPRX1_RCAL_P
ANALOG_LPDP_ISP_RX1_RCAL_NEG — CP38 — LPDPRX1_RCAL_N

R1200 200 1% 1/32W MF 01005 ROOM=SOC
C1200 10PF 5% 16V NP0/C0G 01005 ROOM=SOC
R1210 200 1% 1/32W MF 01005 ROOM=SOC
C1210 10PF 5% 16V NP0/C0G 01005 ROOM=SOC

I2C

21 BI	NC_LPDP_ISP_AUX_RX_D0P	CL22	LPDPRX_AUX_D0_P
21 BI	NC_LPDP_ISP_AUX_RX_D1P	CK24	LPDPRX_AUX_D1_P
21 BI	LPDP_ISP_BI_SWIDE_AUX_RX_D2P	CL26	LPDPRX_AUX_D2_P
21 BI	NC_LPDP_ISP_AUX_RX_D3P	CK28	LPDPRX_AUX_D3_P
21 BI	NC_LPDP_ISP_AUX_RX_D4P	CL30	LPDPRX_AUX_D4_P
21 BI	NC_LPDP_ISP_AUX_RX_D5P	CK32	LPDPRX_AUX_D5_P
21 BI	NC_LPDP_ISP_AUX_RX_D6P	CL34	LPDPRX_AUX_D6_P
21 BI	NC_LPDP_ISP_AUX_RX_D7P	CK36	LPDPRX_AUX_D7_P
21 BI	NC_LPDP_ISP_AUX_RX_D8P	CL38	LPDPRX_AUX_D8_P
21 BI	NC_LPDP_ISP_AUX_RX_D9P	CK40	LPDPRX_AUX_D9_P
21 BI	NC_LPDP_ISP_AUX_RX_D10P	CL42	LPDPRX_AUX_D10_P
21 BI	NC_LPDP_ISP_AUX_RX_D11P	CK43	LPDPRX_AUX_D11_P

GPIO

SENSOR CLK

MIPI-C

MIPI0C_DPCLK	CP60	90_MIPI_ISP_FROM_IRCAM_CLK_P	IN 82
MIPI0C_DNCLK	CN60	90_MIPI_ISP_FROM_IRCAM_CLK_N	IN 82
MIPI0C_DPDATA0	CN58	90_MIPI_ISP_FROM_IRCAM_D0_P	BI 82
MIPI0C_DNDATA0	CP58	90_MIPI_ISP_FROM_IRCAM_D0_N	BI 82
MIPI0C_DPDATA1	CN59	90_MIPI_ISP_FROM_IRCAM_D1_P	IN 82
MIPI0C_DNDATA1	CP59	90_MIPI_ISP_FROM_IRCAM_D1_N	IN 82
MIPI0C_REXT	CL55	ANALOG_MIPI_ISP_REXT	

R1250 200 1% 1/32W MF 01005 ROOM=SOC

ISP_I2C0_SCL	CL58	NC_I2C0_ISP_SCL	17
ISP_I2C0_SDA	CL57	NC_I2C0_ISP_SDA	17
ISP_I2C1_SCL	CM6	NC_I2C1_ISP_SCL	17
ISP_I2C1_SDA	CM4	NC_I2C1_ISP_SDA	17

PP (dev board only)

ISP_GPIO_0	CK59	GPIO_ISP_TO_CAM_PMU1_CAM_PMU2_RESET_L	OUT 43 46
ISP_GPIO_1	CM7	NC_ISP_GPIO_1	20
ISP_GPIO_2	CL59	NC_ISP_GPIO_2	20
ISP_GPIO_3	CN5	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	OUT 70 75 98

External flash trigger:
Kraken sends signal to Lightning accessory

SENSOR0_CLK	AL2	CLK_ISP_TO_CAM_PMU1_24M_R	R1240 33.2 1% 1/32W MF 01005 ROOM=SOC	CLK_ISP_TO_CAM_PMU1_24M OUT 43
SENSOR1_CLK	AN4	CLK_ISP_TO_CAM_PMU2_24M_R	R1260 33.2 1% 1/32W MF 01005 ROOM=SOC	CLK_ISP_TO_CAM_PMU2_24M OUT 46

PACK_OPTION=D53,D54,DEV
BOMOPTION=PRO

SENSOR2_CLK	AN3	NC_SENSOR2_CLK_AP	20
SENSOR3_CLK	AR3	NC_SENSOR3_CLK_AP	20

SYNCING: D52, D53, D54, DEV

PAGE TITLE: SOC: ISP

DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: 1
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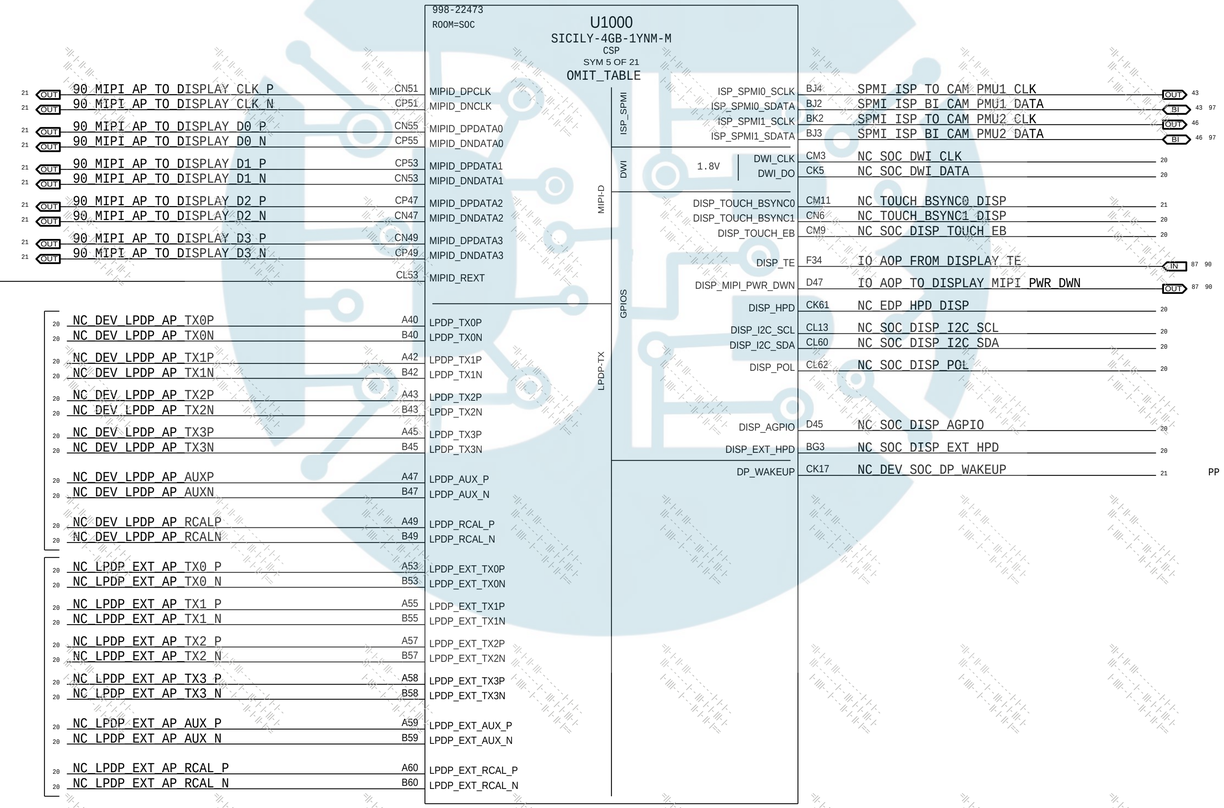
SOC: DISPLAY / ISP



Dev breaks out to baseboard LPDP header

LPDP_RCAL_P/N are for LPDP TX, NC if unused

External LPDP not used

DISPLAY_TE also provides WDG functionality

PP (dev board only)

SPMI Address Map

BUS	DEVICE	ADDR	LOCATION
SPMI0 ISP	Adams1	0x09	Top
SPMI1 ISP	Adams2	0x09	Top

NOTE: SPMI1 ISP is for D53P/D54 only

SYNCING: D52, D53, D54, DEV

PAGE TITLE: SOC: Display

DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: 1
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SOC: AP Serial

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 7 OF 21
OMIT_TABLE

UART0_RXD CH62 ← 96 20 IN UART0_AP_FROM_KRAKEN_DEBUG_RXD
UART0_TXD CP5 → 96 20 OUT UART0_AP_TO_KRAKEN_DEBUG_TXD
UART1_CTS* BP2 ← 20 NC_UART1_AP_CTS_L
UART1_RTS* BM3 ← 20 NC_UART1_AP_RTS_L
UART1_RXD BK4 ← 20 NC_UART1_AP_RXD
UART1_TXD BK3 → 20 NC_UART1_AP_TXD
UART2_CTS* BT4 ← 20 NC_UART2_AP_CTS_L
UART2_RTS* BT2 → 20 NC_UART2_AP_RTS_L
UART2_RXD BP4 ← 20 NC_UART2_AP_RXD
UART2_TXD BP3 → 20 NC_UART2_AP_TXD
UART3_CTS* CJ61 ← 20 NC_UART3_AP_CTS_L
UART3_RTS* CM13 → 21 NC_UART3_AP_RTS_L
UART3_RXD CP6 ← 20 NC_UART3_AP_RXD
UART3_TXD CL15 → 21 NC_UART3_AP_TXD
UART4_RXD AL61 ← 96 20 IN UART4_AP_FROM_KRAKEN_ACC_RXD
UART4_TXD AL62 → 96 20 OUT UART4_AP_TO_KRAKEN_ACC_TXD
UART6_RXD CK6 ← 20 NC_UART6_AP_RXD_1V8
UART6_TXD CL2 → 88 68 OUT GPIO_AP_TO_TOUCH_RESET_L_1V8
1.8V
Use UART6_TXD as 1.8V GPIO

I2C0_SCL AG62 NC_I2C0_AP_SCL 21
I2C0_SDA AJ61 NC_I2C0_AP_SDA 21
I2C1_SCL AG4 NC_I2C1_AP_SCL 21
I2C1_SDA AF2 NC_I2C1_AP_SDA 21
I2C2_SCL AF3 → OUT I2C2_AP_SCL 17
I2C2_SDA AD2 ↔ BI I2C2_AP_SDA 17
I2C3_SCL CL5 → OUT I2C3_AP_SCL_1V8 17
I2C3_SDA CL49 ↔ BI I2C3_AP_SDA_1V8 17
I2C4_SCL CL4 → OUT I2C_DISPLAY_SCL_1V8 17
I2C4_SDA CL47 ↔ BI I2C_DISPLAY_SDA_1V8 17
1.8V
Alt AP UART7

I2S0_DIN P2 ← IN I2S0_AP_FROM_CODEC_ASP3_DIN 61 96
I2S0_DOUT T4 → OUT I2S0_AP_TO_CODEC_ASP3_DOUT 61 96
I2S0_BCLK P4 ← IN I2S0_AP_FROM_CODEC_ASP3_BCLK 61 96
I2S0_LRCK M2 ← IN I2S0_AP_FROM_CODEC_ASP3_LRCLK 61 96
I2S0_MCK P3 I2S0_AP_TO_SPKRAMP_TOP_MCLK_R
I2S1_DIN AB4 ← IN I2S1_AP_FROM_CODEC_ASP4_DIN 61 96
I2S1_DOUT AD3 → OUT I2S1_AP_TO_CODEC_ASP4_DOUT 61 96
I2S1_BCLK Y3 ← IN I2S1_AP_FROM_CODEC_ASP4_BCLK 61 96
I2S1_LRCK Y2 ← IN I2S1_AP_FROM_CODEC_ASP4_LRCLK 61 96
I2S1_MCK AB3 NC_I2S1_AP_MCLK 20
I2S2_DIN V2 ← IN I2S2_AP_FROM_BB_DIN 99
I2S2_DOUT Y4 → OUT I2S2_AP_TO_BB_DOUT 99
I2S2_BCLK T2 ← IN I2S2_AP_FROM_BB_BCLK 99
I2S2_LRCK T3 ← IN I2S2_AP_FROM_BB_LRCLK 99
I2S2_MCK V3 NC_I2S2_AP_MCLK 20
1.8V

R1410 33.2 1% 1/32W MF 01005 ROOM=SOC
I2S0_AP_TO_SPKRAMP_TOP_MCLK → OUT 63

NOTE:
I2S DIN/DOUT are SOC-centric,
SOC DIN routes to load DOUT and vice-versa

AP I2S0
Used for MikeyBus
(MCLK to Top Spk)

AP I2S1
Used for Mics

SPI0: NAND
20 OUT SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0 — R1400 0.00 0% 1/32W MF 01005 ROOM=SOC

SPI1: Cumulus
D53 only
21 OUT NC_SPI1_SCLK_1V8_R — R1401 0.00 0% 1/32W MF 01005 ROOM=SOC
PACK_IGNORE=TRUE
PACK_OPTION=D53,DEV

SPI2: Ada
D52/D54 only
21 OUT SPI2_AP_TO_TOUCH_SCLK — R1402 0.00 0% 1/32W MF 01005 ROOM=SOC
XW1402 SHORT-01005-SP
PACK_OPTION=D54,DEV
998-23033
PACK_IGNORE=TRUE
PACK_OPTION=D52

SPI3: Brighton
20 OUT SPI3_AP_TO_CODEC_SCLK — R1403 0.00 0% 1/32W MF 01005 ROOM=SOC
XW1403 SHORT-01005-SP
PACK_OPTION=D52,D54,DEV
998-23033
PACK_IGNORE=TRUE
PACK_OPTION=D53
PP (dev board only)

SPI0_MISO AL3 ← 20 IN SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2
SPI0_MOSI AJ2 → 20 OUT SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1
SPI0_SCLK AL4 → SPI0_AP_TO_NAND_SCLK_R
SPI1_MISO CK47 ← 21 IN NC_SPI1_MISO_1V8
SPI1_MOSI CK49 → 21 OUT NC_SPI1_MOSI_1V8
SPI1_SCLK CL6 → NC_SPI1_SCLK_1V8_R
SPI1_SSIN CL51 → 21 OUT NC_SPI1_CS_L_1V8
SPI2_MISO BE2 ← 21 IN SPI2_AP_FROM_TOUCH_MISO
SPI2_MOSI BC2 → 21 OUT SPI2_AP_TO_TOUCH_MOSI
SPI2_SCLK BC3 → SPI2_SCLK_AP_R
SPI2_SSIN BA3 → 21 OUT SPI2_AP_TO_TOUCH_CS_L
SPI3_MISO BG2 ← 20 IN SPI3_AP_FROM_CODEC_MISO
SPI3_MOSI BE4 → 20 OUT SPI3_AP_TO_CODEC_MOSI
SPI3_SCLK BE3 → SPI3_SCLK_AP_R
SPI3_SSIN BC4 → 20 OUT SPI3_AP_TO_CODEC_CS_L
1.8V
Place series terminations close to SoC Pins

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 8 OF 21
OMIT_TABLE

SGPIO0 AW3 ← 30 IN GPIO_PMU_TO_SOC_DOUBLE_CLICK_DET_L
SGPIO1 AW4 ← 20 NC_SOC_S_GPIO1
SI2C0_SCL AU1 → 17 OUT I2C0_S_SCL
SI2C0_SDA AU2 ↔ 17 BI I2C0_S_SDA

SSPI0_MISO AW2 NC_SSPI0_MISO_AP 20
SSPI0_MOSI AU4 NC_SSPI0_MOSI_AP 20
SSPI0_SCLK AU3 NC_SSPI0_SCLK_AP 20

SYNCING: D52, D53, D54, DEV

PAGE TITLE: SOC: Serial
DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: 1
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SOC: AP GPIO

998-22473
ROOM=SOC

U1000
SICILY-4GB-1YNM-M
CSP
SYM 6 OF 21
OMIT_TABLE
GPIO

19	GPIO_BOARD_REV3	BT3	GPIO0
19	GPIO_BOARD_REV2	BV2	GPIO1
19	GPIO_BOARD_REV1	BY2	GPIO2
19	GPIO_BOARD_REV0	BV3	GPIO3
19	GPIO_AP_CANARY1	BY3	GPIO4
19	GPIO_AP_CANARY2	BY4	GPIO5
19	GPIO_AP_BI_CCG2B_SWDIO	CK58	GPIO6
19	GPIO_AP_TO_CCG2B_SWCLK	CL11	GPIO7
19	GPIO_AP_FROM_DISPLAY_PANEL_ID	CM5	GPIO8
19	GPIO_AP_FROM_WLAN_TIME_SYNC	CK15	GPIO9
19	GPIO_AP_TO_BB_PEAK_PWR_IND	CN9	GPIO10
19	GPIO_AP_TO_BB_COREDUMP	CP7	GPIO11
19	GPIO_AP_FROM_BB_RESET_DETECT_L	CK19	GPIO12
19	GPIO_AP_FROM_CODEC_INT_L	CL17	GPIO13
19	NC_AP_GPIO14	CJ60	GPIO14
19	GPIO_AP_TO_SPKRAMP_TOP_RESET_L	BC62	GPIO15

GPIO16	BC61	GPIO_AP_FROM_BT_AUDIO_SYNC	19
GPIO17	BC60	GPIO_AP_TO_AMUX_PMU_SYNC	19
GPIO18	AW62	NC_DEV_AP_GPIO18	19
GPIO19	AW61	NC_DEV_AP_GPIO19	19
GPIO20	AW60	NC_DEV_AP_GPIO20	19
GPIO21	AU62	NC_DEV_AP_GPIO21	19
GPIO22	AU61	NC_DEV_AP_GPIO22	19
GPIO23	AU60	NC_DEV_AP_GPIO23	19
GPIO24	AR62	NC_DEV_AP_GPIO24	19
GPIO25	AR61	GPIO_AP_TO_BB_TIME_MARK	19
GPIO26	AN61	NC_DEV_AP_GPIO26	19

SYNCING: D52, D53, D54, DEV

PAGE TITLE
SOC: GPIO

DRAWING NUMBER 051-05170
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NOTE:
I2S DIN/DOUT are SOC-centric,
SOC DIN routes to load DOUT and vice-versa

SOC: AOP

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 9 OF 21
OMIT_TABLE

I2C0_AOP_SCL	F61	AOP_I2CM0_SCL		I2C	
I2C0_AOP_SDA	F62	AOP_I2CM0_SDA			
I2C1_AOP_SCL	F45	AOP_I2CM1_SCL			
I2C1_AOP_SDA	D42	AOP_I2CM1_SDA			
SPI0_AOP_FROM_IMU_R1_MISO	H60	AOP_SPI0_MISO		SPI	GPIO
SPI0_AOP_TO_IMU_R1_MOSI	H62	AOP_SPI0_MOSI			
SPI0_AOP_TO_IMU_R1_SCLK_R	G62	AOP_SPI0_SCLK			
I2C2_AOP_SCL	D55	AOP_SPI1_MISO	AOP I2C2 SCL		
I2C2_AOP_SDA	D57	AOP_SPI1_MOSI	AOP I2C2 SDA		
GPIO_AOP_TO_WLAN_CONTEXT_B	D58	AOP_SPI1_SCLK			
GPIO_AOP_TO_WLAN_CONTEXT_A	E34	AOP_SPI1_SSIN			
I2S0_AOP_FROM_CODEC_ASP1_DIN	D59	AOP_I2S0_DIN			
I2S0_AOP_TO_CODEC_ASP1_DOUT	E49	AOP_I2S0_DOUT			
I2S0_AOP_FROM_CODEC_ASP1_BCLK	D36	AOP_I2S0_BCLK		I2S	
I2S0_AOP_FROM_CODEC_ASP1_LRCLK	E36	AOP_I2S0_LRCK			
I2S0_AOP_TO_CODEC_MCLK1_R	F36	AOP_I2S0_MCK			
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN_R	C36	AOP_I2S1_DIN			
I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT_R_SOC	B36	AOP_I2S1_DOUT			
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK	E53	AOP_I2S1_BCLK			
I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK	E51	AOP_I2S1_LRCK			
I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK_R	E47	AOP_I2S1_MCK			
UART1_AOP_FROM_BB_RXD	K62	AOP_SPMI1_SDATA	SUPPORTS UART	UART	
UART1_AOP_TO_BB_TXD	G61	AOP_SPMI1_SCLK	ALT FUNC1		
SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	D43	AOP_SPMI0_SDATA	SUPPORTS UART		
SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK_R	F47	AOP_SPMI0_SCLK	ALT FUNC1		
UART2_AOP_FROM_TOUCH_RXD	G60	AOP_UART2_RXD			
UART2_AOP_TO_TOUCH_TXD	E45	AOP_UART2_TXD			

AOP_FUNC0	E62	GPIO_SCM_AOP_FROM_IMU_DATARDY
AOP_FUNC1	F60	GPIO_SCM_AOP_TO_IMU_SPI_CS_L
AOP_FUNC2	E43	GPIO_AOP_FROM_PEARL_B2B_DETECT
AOP_FUNC3	E60	NC_DEV_AOP_FUNC3
AOP_FUNC4	K61	GPIO_SCM_AOP_FROM_R1_INT
AOP_FUNC5	D60	GPIO_AOP_TO_R1_COREDUMP_TRIGGER
AOP_FUNC6	D62	GPIO_AOP_TO_R1_TIME_SYNC_L
AOP_FUNC7	A36	GPIO_AOP_TO_CODEC_RESET_L
AOP_FUNC8	E42	GPIO_AOP_TO_BB_FORCE_PWM
AOP_FUNC9	E59	GPIO_AOP_FROM_IRCAM_B2B_DETECT
AOP_FUNC10	F57	GPIO_SCM_AOP_TO_R1_SPI_CS_L
AOP_FUNC11	F42	NC_AOP_FUNC11
AOP_FUNC12	D40	GPIO_AOP_TO_ALS_COEX
AOP_FUNC13	F58	GPIO_AOP_TO_NFC_IRONMAN_EN
AOP_FUNC14	F53	NC_GPIO_AOP_FROM_TOUCH_CTS
AOP_FUNC15	E58	GPIO_SCM_AOP_BI_PROX_INT_L
AOP_FUNC16	E40	GPIO_SCM_AOP_FROM_ALS_INT_L
AOP_FUNC17	F51	GPIO_SCM_AOP_FROM_EIGER_INT_L
AOP_FUNC18	E57	GPIO_SCM_AOP_FROM_COMPASS_INT
AOP_FUNC19	F40	GPIO_SCM_AOP_FROM_JARVIS_INT
AOP_FUNC20	D38	GPIO_AOP_FROM_TOUCH_INT_L
AOP_FUNC21	E55	NC_AOP_FUNC21
AOP_FUNC22	E38	NC_DEV_AOP_FUNC22

SPI1_SCLK/SSIN: Use as AOP GPIO

AOP I2S0
Penrose, LDCM,
Borealis
(MCLK to Codec)

AOP I2S1
Out to BotSpk,
TopSpk, Arc,
in from Sak.
(MCLK to Arc
and BotSpk)

R1601 33.2 1% 1/32W MF 01005 ROOM=SOC
R1603 33.2 1% 1/32W MF 01005 ROOM=SOC
R1606 0.00 0% 1/32W MF 01005 ROOM=SOC
R1607 0.00 0% 1/32W MF 01005 ROOM=SOC
R1608 0.00 0% 1/32W MF 01005 ROOM=SOC
R1622 33.2 1% 1/32W MF 01005 ROOM=SOC

Touch UART
D52/D54: WIRED TO ADA
D53: WIRED TO TOUCH B2B

R1621 1.00M 5% 1/32W MF 01005
R1620 1.00M 5% 1/32W MF 01005

SPMI Address Map

BUS	DEVICE	ADDR	LOCATION
SPMI0 AOP	WLAN	0x0E	Bottom
SPMI0 AOP	Ceres (P)	0x0C	D52/D53: Top D54: Bottom
SPMI0 AOP	Ceres (F)	0x0B	D53/D54: Top D52: Bottom

NOTE: Ceres (F) default address is 0x0C, programmed to 0x0B on SMT line

BUS	DEVICE	ADDR	LOCATION
SPMI0 NUB	Cota	0x0F	Top
SPMI0 NUB	DotaraLV	0x0E	Top

SOC: SMC

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 10 OF 21
OMIT_TABLE

I2C0_SMC_SCL	G4	SMC_I2CM0_SCL	I2C
I2C0_SMC_SDA	F26	SMC_I2CM0_SDA	
I2C1_SMC_SCL	G2	SMC_I2CM1_SCL	
I2C1_SMC_SDA	H2	SMC_I2CM1_SDA	
I2C2_SMC_SCL	G3	SMC_I2CM2_SCL	
I2C2_SMC_SDA	F2	SMC_I2CM2_SDA	

SOC: NUB

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 11 OF 21
OMIT_TABLE

SPMI0_NUB_TO_PMU_DOTARA_CLK_R	D32	NUB_SPMI0_SCLK	SPMI
SPMI0_NUB_BI_PMU_DOTARA_DATA	D4	NUB_SPMI0_SDATA	
SWD_NUB_TO_PMU_TOUCH_SWCLK	F6	NUB_SWD_TCK_OUT0	SWD
SWD_NUB_BI_PMU_SWDIO	F13	NUB_SWD_TMS0	
SWD_NUB_BI_TOUCH_SWDIO	F11	NUB_SWD_TMS1	
IO_NUB_FROM_KRAKEN_DOCK_CONNECT	F30	NUB_DOCK_CONNECT	DOCK
IO_NUB_FROM_KRAKEN_INT	E30	NUB_DOCK_ATTENTION	
GPIO_NUB_FROM_CCG2B_INT_L	D2	NUB_GPIO_0	GPIO
GPIO_NUB_FROM_GECKO_IRQ_L	E4	NUB_GPIO_1	
GPIO_NUB_FROM_PARROT_INT_L	E3	NUB_GPIO_2	
GPIO_NUB_TO_GECKO_RESET_L	F28	NUB_GPIO_3	
GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	E2	NUB_GPIO_4	
NC_NUB_GPIO5	F3	NUB_GPIO_5	
NC_NUB_GPIO6	E28	NUB_GPIO_6	
SWD_DOCK_TO_AP_SWCLK	E5	JTAG_TCK	JTAG
SWD_DOCK_BI_AP_SWDIO	C34	JTAG_TMS	
GND	D6	JTAG_SEL	
NC_DEV_JTAG_TDI	B34	JTAG_TDI	
NC_DEV_JTAG_TDO	E6	JTAG_TDO	
NC_DEV_JTAG_TRST_L	D5	JTAG_TRST*	
90_EUSB_DBG_PARROT_BI_AP_N	B30	DBG_USB_EDM	DEBUG USB
90_EUSB_DBG_PARROT_BI_AP_P	A30	DBG_USB_EDP	
ANALOG_DBG_USB_RESREF	D30	DBG_USB_RESREF	
PP1V2_S2	E32	DBG_PROBE_VALID	
IO_PMU_TO_SYSTEM_RESET_L	D51	COLD_RESET*	MISC
IO_PMU_TO_SYSTEM_RESET_L	D53	CFSB_AON	
CLK_PMU_TO_AOP_32K	D49	RT_CLK32768	
IO_SOC_TO_PMU_WDOG_RESET	D34	WDOG	
IO_AON_TO_AP_XTAL_CFSB	A34	AON_SLEEP1_RESET*	
CLK_NUB_TO_TOUCH_24M_R	F15	NUB_CLK_OUT0	
GND	CP4	KIS_DFU_SELECT	

Touch SWDIO: Wired to Touch B2B (D52/D54)
Touch SWDIO: No connect (D53)

Gecko IRQ needs SOC weak internal PU
Parrot INT needs external or SOC pull-up

Can use Dotara GPIO for BBPMU Clock EN

R1610 33.2 1% 1/32W MF 01005 ROOM=SOC

R1650 200 1% 1/32W MF 01005 ROOM=SOC

XW1660 SHORT-01005-SP
R1660 0.00 0% 1/32W MF 01005 ROOM=SOC

PACK_OPTION=D52,DEV
PACK_OPTION=D54,DEV
PACK_OPTION=RE-TRUE

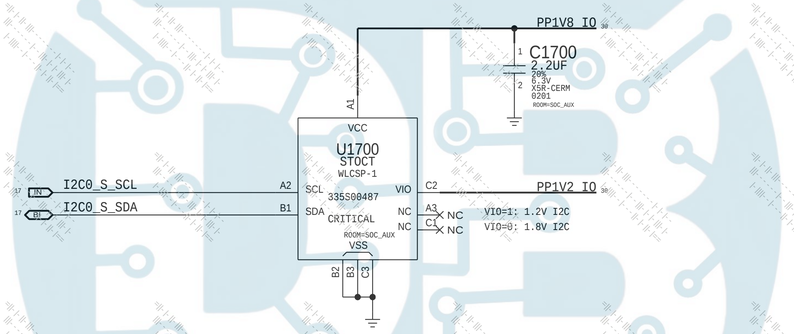
KIS_DFU_SELECT:
POR = 0 (GND): USB0 for DFU (legacy)
Debug = 1 (1V2): USB1 for DFU (Ranzi-in-System)

SYNCING: D52, D53, D54, DEV

PAGE TITLE
SOC: AOP & SMC & NUB

DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 16 OF 138
SHEET 15 OF 117

OCELOT



SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Ocelot
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	17 OF 138
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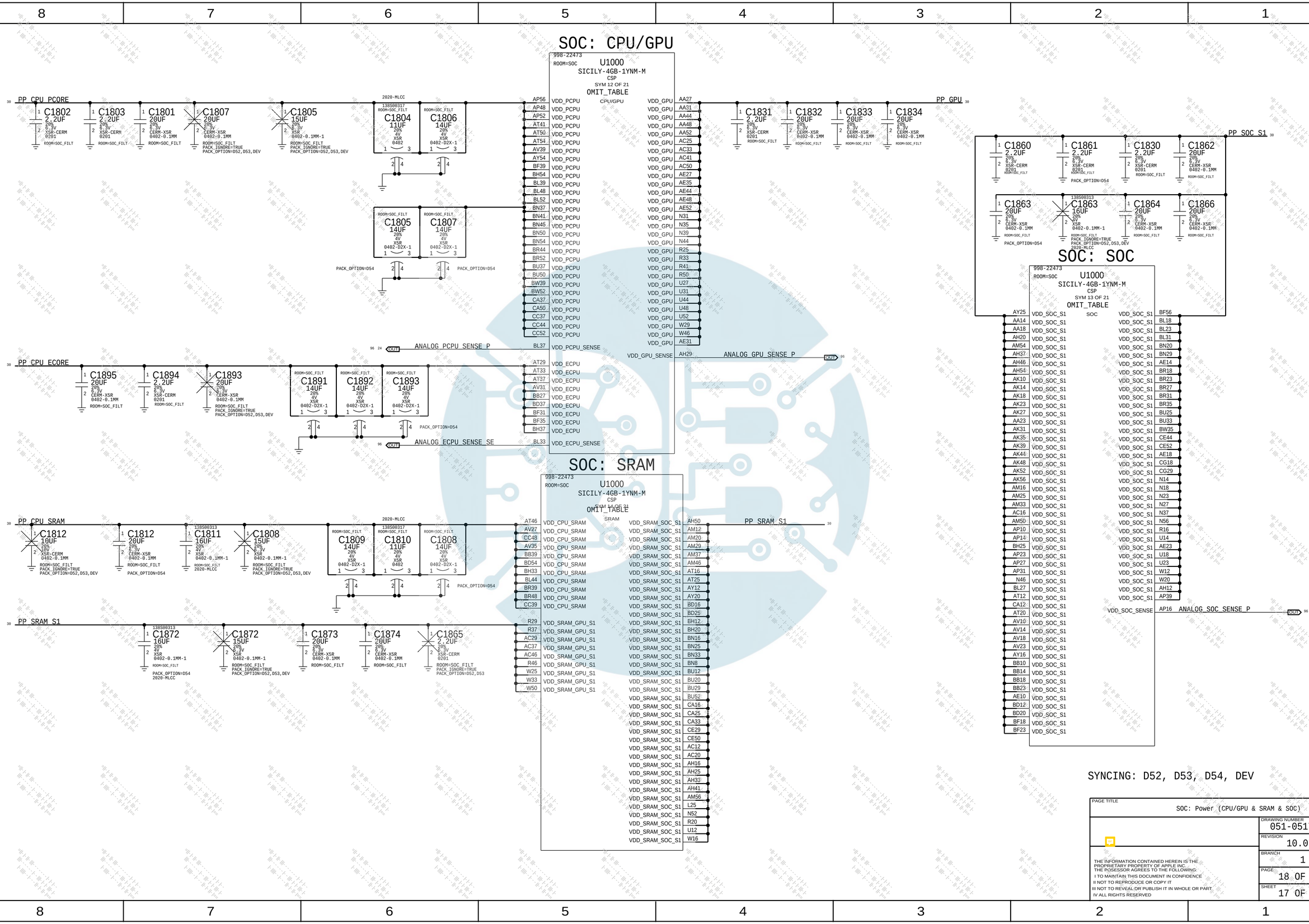
SOC: CPU/GPU
998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 12 OF 21
OMIT_TABLE
CPU/GPU
PP_CPU_PCORE
C1802 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1803 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1801 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1807 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C1805 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
2020-MLCC
138S00317
C1804 11UF 20% 4V X5R 0402 ROOM=SOC_FILT
C1806 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1805 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1807 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
PACK_OPTION=D54
PACK_OPTION=D54
PP_CPU_ECORE
C1895 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1894 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1893 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C1891 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1892 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1893 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
PACK_OPTION=D54
ANALOG_PCPU_SENSE_P
ANALOG_ECPU_SENSE_SE
PP_GPU
C1831 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1832 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1833 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1834 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
ANALOG_GPU_SENSE_P
VDD_PCPU
VDD_GPU
VDD_ECPU
VDD_PCPU_SENSE
VDD_GPU_SENSE
VDD_ECPU_SENSE
SOC: SRAM
998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 14 OF 21
OMIT_TABLE
SRAM
PP_CPU_SRAM
C1812 10UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C1812 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_OPTION=D54
138S00313
C1811 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=SOC_FILT 2020-MLCC
C1808 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
2020-MLCC
138S00317
C1809 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1810 11UF 20% 4V X5R 0402 ROOM=SOC_FILT
C1808 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
PACK_OPTION=D54
PP_SRAM_S1
138S00313
C1872 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_OPTION=D54 2020-MLCC
C1872 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C1873 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1874 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1865 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53
VDD_CPU_SRAM
VDD_SRAM_GPU_S1
VDD_SRAM_SOC_S1
PP_SRAM_S1
PP_SOC_S1
C1860 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1861 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT PACK_OPTION=D54
C1830 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1862 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1863 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT PACK_OPTION=D54
138S00313
C1863 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV 2020-MLCC
C1864 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C1866 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
SOC: SOC
998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 13 OF 21
OMIT_TABLE
SOC
VDD_SOC_S1
VDD_SOC_SENSE
ANALOG_SOC_SENSE_P
SYNCING: D52, D53, D54, DEV
PAGE TITLE
SOC: Power (CPU/GPU & SRAM & SOC)
DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 18 OF 138
SHEET 17 OF 117
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SUBSYSTEM SPECIFIC BOM TABLES

2.2uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?	(C1970)	CAP,CER,X5R,2.2UF,20%,6.3V,0201

SOC: FIXED

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 17 OF 21
OMIT_TABLE

FIXED

AP8 VDD_FIXED_S1
AV56 VDD_FIXED_S1
CA52 VDD_FIXED_S1
CE16 VDD_FIXED_S1
CG31 VDD_FIXED_S1
CG52 VDD_FIXED_MIPID_S1
CG56 VDD_FIXED_MIPIC_S1
CK55 VDD_FIXED_MIPID_PLL_S1
J20 VDD_FIXED_USB_S1
J52 VDD_FIXED_LPDP_TX_S1
J56 VDD_FIXED_LPDP_TX_S1
CE33 VDD_FIXED_LPDP_RX_S1
CE37 VDD_FIXED_LPDP_RX_S1
CE41 VDD_FIXED_LPDP_RX_S1
CE46 VDD_FIXED_LPDP_RX_S1
L16 VDD_FIXED_PCIE_S1
L20 VDD_FIXED_PCIE_S1
N16 VDD_FIXED_PCIE_S1

VDD_FIXED_PCIE_REFBUF_S1 J12 PP0V78_SOC_FIXED_PCIE_REFBUF VOLTAGE=0.8
VDD_FIXED_PCPU_S1 AP46
VDD_FIXED_ECPU_S1 AY39
VDD_FIXED_MTR_S1 CF60
VDD_FIXED_PLL_GPU_S1 AE41
VDD_FIXED_PLL_DDR0_S1 CE12
VDD_FIXED_PLL_DDR1_S1 BP60
VDD_FIXED_PLL_DDR2_S1 AC10
VDD_FIXED_PLL_DDR3_S1 P60
VDD_FIXED_PLL_SOC_S1 BH27
VDD_FIXED_PLL_ANE_S1 CA35
VDD_FIXED_XTAL_S1 F9 PP0V78_VDD_FIXED_XTAL VOLTAGE=0.8

PP0V78_SOC_FIXED_S1 (30)
GND (30)
(Not used for s)

C1901 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1907 220PF 5% 25V C0G 01005 ROOM=SOC_FILT
C1908 220PF 5% 25V C0G 01005 ROOM=SOC_FILT
C1909 220PF 5% 25V C0G 01005 ROOM=SOC_FILT
C1906 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1905 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1910 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1916 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1918 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1917 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1922 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1921 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1920 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

OMIT
XW1940
SHORT-20L-0.05MM-SM
ROOM=SOC_FILT
C1940 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1941 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1942 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1902 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
R1970 20.0 5% 1/32W MF 01005 ROOM=SOC_FILT
C1970 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT [SS] MURATA

PP1V2_IO
Place cap near pin
C1935 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

SOC: VDD12

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 18 OF 21
OMIT_TABLE

F22 VDD12_USB
F24 VDD12_USB_DEBUG_S2
AP44 VDD12_PLL_PCPU
AY37 VDD12_PLL_ECPU
AE39 VDD12_PLL_GPU
F7 VDD12_XTAL_S1
CL9 VDD12_AMUX_S2
CG54 VDD12_MIPIC
CK53 VDD12_MIPID_S1
AM41 VDD12_TSADC_CPU0
AT39 VDD12_TSADC_CPU1
AP35 VDD12_TSADC_SOC0
AC52 VDD12_TSADC_SOC1
R12 VDD12_TSADC_SOC2
J27 VDDIO12_AOP_S2
J31 VDDIO12_AOP_S2
J35 VDDIO12_AOP_S2
J39 VDDIO12_AOP_S2
J44 VDDIO12_AOP_S2
J48 VDDIO12_AOP_S2
BF27 VDD12_PLL_SOC_S1
BH29 VDD12_PLL_SOC_S1
CE14 VDDIO12_PLL_DDR0_S1
BM60 VDDIO12_PLL_DDR1_S1
AC8 VDDIO12_PLL_DDR2_S1
M60 VDDIO12_PLL_DDR3_S1
CC35 VDD12_PLL_ANE

VDDIO12_GRP1_S2 CG12
VDDIO12_GRP3 AY56
VDDIO12_GRP3 BD56
VDDIO12_GRP3 BL56
VDDIO12_GRP4 CG16
VDDIO12_GRP4 CG20
VDDIO12_GRP4 CG23
VDDIO12_GRP5 AH8
VDDIO12_GRP5 AM8
VDDIO12_GRP5 AT8
VDDIO12_GRP5 AY8
VDDIO12_GRP5 BD8
VDD12_PCIE J14
VDD12_PCIE J18
VDD12_MTR CH60
VDD12_LPDP_TX L50
VDD12_LPDP_TX L54
VDD12_LPDP_RX CG35
VDD12_LPDP_RX CG39
VDD12_LPDP_RX CG44
VDD12_LPDP_RX CG48
VDD12_LPDP_RX CG37
VDD12_EFUSE1 N50
VDD12_EFUSE2 W18
VDD12_EFUSE3 AM39
VDD12_EFUSE4 N48
VDD12_EFUSE5 AP37
VDD12_FMON R14 PP1V2_VDD12_FMON VOLTAGE=1.2
VDD12_PCIE_REFBUF L12
VDD12_ULPPLL_S2 L33 PP1V2_VDD12_ULPPLL_S2 VOLTAGE=1.2
VDD12_ADC_SOC_S1 K60

PP1V2_S2
Place cap near pin
PP1V2_SOC
PP1V2_S1
PP1V2_IO
Place cap near pins
Shares decap with other S1 rails

RADAR #: 54364908
PLACE NEAR SOC
OMIT
XW1930
SHORT-20L-0.05MM-SM
ROOM=SOC_FILT
To ANE
VOLTAGE=1.2
PP1V2_SOC_FILT
Place 01005 caps near pins (incl. ANE)
FL1950 240-OHM-25%-0.20A-1.0DCR 0100S ROOM=SOC_FILT 155S0755
PP1V2_S1_XTAL VOLTAGE=1.2
Share cap with VDD12_PLL_ECPU/_PCPU/_GPU

C1900 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1926 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1927 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1928 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1946 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1903 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1998 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1999 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1997 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1996 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1923 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1924 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1963 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1964 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

[LAYOUT] VDDIO12_GRPx: Isolation >= 2.5nH from other nets on the same domain
OMIT
XW1901
SHORT-10L-0.1MM-SM
ROOM=SOC_FILT
NO_XNET_CONNECTION
PP1V2_IO_GRP3 VOLTAGE=1.2
OMIT
XW1902
SHORT-10L-0.1MM-SM
ROOM=SOC_FILT
NO_XNET_CONNECTION
PP1V2_IO_GRP4 VOLTAGE=1.2
C1904 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1945 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1947 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1948 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1937 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1955 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1950 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1931 0.01UF 10% 6.3V X5R 01005 ROOM=SOC_FILT
C1932 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1933 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
Used for SoC fusing
GND on all systems
R1960 49.9 1% MF 1/32W 01005 ROOM=SOC_FILT
R1961 49.9 1% MF 1/32W 01005 ROOM=SOC_FILT
C1938 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1995 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1936 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
[LAYOUT] VDD12_PCIE_REFBUF: Inductance from C1995.1 to PP1V2_SOC plane >1.5nH @ 100MHz

SYNCING: D52, D53, D54, DEV

PP0V78_SOC_FIXED_S1 (30)
PP1V2_S2 (30)
PP1V2_IO (30)
PP1V2_SOC (30)
PP1V2_S1 (30)
GND (30)

PAGE TITLE: SOC: Power (Fixed & 1V2)
DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: 1
PAGE: 19 OF 138
SHEET: 18 OF 117

SOC: DDR

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 16 OF 21
OMIT_TABLE
DDR

30 PP_DCS_S1

C2088 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2087 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2086 2.7UF 20% 4V X5R 0201 ROOM=SOC_FILT 138S00321 2020-MLCC
C2085 2.7UF 20% 4V X5R 0201 ROOM=SOC_FILT 138S00321 2020-MLCC
PLACE CAPS ON SOC CORNERS

BR10 VDD_DCS_DDR0_S1
CE10 VDD_DCS_DDR0_S1
BR54 VDD_DCS_DDR1_S1
CE54 VDD_DCS_DDR1_S1
AA10 VDD_DCS_DDR2_S1
L10 VDD_DCS_DDR2_S1
AC54 VDD_DCS_DDR3_S1
R54 VDD_DCS_DDR3_S1

96 OUT ANALOG_DCS_SENSE_SE
AD62 VDD_DCS_SENSE

30 PP0V6_VDDQL_S1

C2093 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2092 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2091 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2090 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
PLACE CAPS ON SOC CORNERS

BE1 VDDQL_DDR0_S1
BJ1 VDDQL_DDR0_S1
BM1 VDDQL_DDR0_S1
BU8 VDDQL_DDR0_S1
CE8 VDDQL_DDR0_S1
CF1 VDDQL_DDR0_S1
CJ1 VDDQL_DDR0_S1
CL1 VDDQL_DDR0_S1
BC63 VDDQL_DDR1_S1
BG63 VDDQL_DDR1_S1
BK63 VDDQL_DDR1_S1
BR56 VDDQL_DDR1_S1
CC56 VDDQL_DDR1_S1
CD63 VDDQL_DDR1_S1
CH63 VDDQL_DDR1_S1
CK63 VDDQL_DDR1_S1
AD1 VDDQL_DDR2_S1
AG1 VDDQL_DDR2_S1
AL1 VDDQL_DDR2_S1
E1 VDDQL_DDR2_S1
G1 VDDQL_DDR2_S1
K1 VDDQL_DDR2_S1
L8 VDDQL_DDR2_S1
W8 VDDQL_DDR2_S1
AB63 VDDQL_DDR3_S1
AE56 VDDQL_DDR3_S1
AF63 VDDQL_DDR3_S1
AJ63 VDDQL_DDR3_S1
D63 VDDQL_DDR3_S1
F63 VDDQL_DDR3_S1
H63 VDDQL_DDR3_S1
R56 VDDQL_DDR3_S1

96 OUT ANALOG_VDDQL_SENSE_SE
AD60 VDDQL_SENSE

VDD2_DDR0_S2 BA2
VDD2_DDR0_S2 BP1
VDD2_DDR0_S2 BV1
VDD2_DDR0_S2 CB1
VDD2_DDR0_S2 CL3
VDD2_DDR1_S2 BA62
VDD2_DDR1_S2 BM63
VDD2_DDR1_S2 BT63
VDD2_DDR1_S2 BY63
VDD2_DDR1_S2 CL61
VDD2_DDR2_S2 AB1
VDD2_DDR2_S2 AN2
VDD2_DDR2_S2 D3
VDD2_DDR2_S2 P1
VDD2_DDR2_S2 V1
VDD2_DDR3_S2 AN62
VDD2_DDR3_S2 D61
VDD2_DDR3_S2 M63
VDD2_DDR3_S2 T63
VDD2_DDR3_S2 Y63
VDDIO11_RET_DDR0_S2 CJ4
VDDIO11_RET_DDR1_S2 BT60
VDDIO11_RET_DDR2_S2 K4
VDDIO11_RET_DDR3_S2 Y60

PP1V06_S2 30
C2080 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2081 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2082 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2083 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
PLACE CAPS ON SOC CORNERS

VDD1_DDR0_S2 BA1
VDD1_DDR0_S2 CM2
VDD1_DDR1_S2 BA63
VDD1_DDR1_S2 CM62
VDD1_DDR2_S2 AN1
VDD1_DDR2_S2 C2
VDD1_DDR3_S2 AN63
VDD1_DDR3_S2 C62

PP1V8_S2 30
C2096 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SOC_FILT
C2097 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SOC_FILT
C2098 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SOC_FILT
C2099 0.22UF 10% 6.3V CER-X5R 01005 ROOM=SOC_FILT
PLACE CAPS ON SOC CORNERS

SOC: AOP/AVE/ISP/USB

998-22473
ROOM=SOC
U1000
SICILY-4GB-1YNM-M
CSP
SYM 15 OF 21
OMIT_TABLE
LOW/AVE/DISP

30 PP0V7_VDD_LOW_S2

R2021 10 1% 1/32W MF 01005 ROOM=SOC_FILT
R2022 49.9 1% 1/32W MF 01005 ROOM=SOC_FILT
C2050 0.47UF 20% 6.3V X5R 01005 ROOM=SOC_FILT
C2020 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C2052 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2000 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C2001 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
PLACE AT SOC BALLS

J25 VDD_LOW_S2
L29 VDD_LOW_S2
L37 VDD_LOW_S2
L41 VDD_LOW_S2
L46 VDD_LOW_S2
J23 VDD_LOW_USB_DEBUG_S2
J33 VDD_LOW_FLPPLL_S2
L31 VDD_LOW_ULPPLL_S2

PP0V7_VDD_LOW_FLPPLL VOLTAGE=0.7
PP0V7_VDD_LOW_ULPPLL VOLTAGE=0.7

VDDIO18_GRP1 CG10
VDDIO06_GRP1_1 CK9 PP0V6_VDDIO06_GRP1_1 VOLTAGE=0.6
VDDIO06_GRP1_2 CK11 PP0V6_VDDIO06_GRP1_2 VOLTAGE=0.6

PP1V8_IO 30
C2073 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2010 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C2011 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

VDDIO06_GRPx RADAR #: 48907718
Cmin = 4.7uF
Loop R < 0.2 ohm
Loop L < 1nH

30 PP_AVE_S1

C2026 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C2025 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C2024 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT PACK_OPTION=D54

BW23 VDD_AVE_S1
BW27 VDD_AVE_S1
BW31 VDD_AVE_S1
CA29 VDD_AVE_S1
CC23 VDD_AVE_S1
CC27 VDD_AVE_S1
CC31 VDD_AVE_S1
CE20 VDD_AVE_S1
CE25 VDD_AVE_S1
CG27 VDD_AVE_S1

30 PP_DISP_S1

C2033 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C2030 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=SOC_FILT
C2032 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT

BF10 VDD_DISP_S1
BF14 VDD_DISP_S1
BH16 VDD_DISP_S1
BH8 VDD_DISP_S1
BL10 VDD_DISP_S1
BL14 VDD_DISP_S1
BN12 VDD_DISP_S1
BR14 VDD_DISP_S1
BU16 VDD_DISP_S1
BW14 VDD_DISP_S1
BW18 VDD_DISP_S1
CA20 VDD_DISP_S1
CC14 VDD_DISP_S1
CC18 VDD_DISP_S1

SYNCING: D52, D53, D54, DEV

PAGE TITLE
SOC: Power (DDR & AOP/AVE/ISP/USB)

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REVISION 10.0.0
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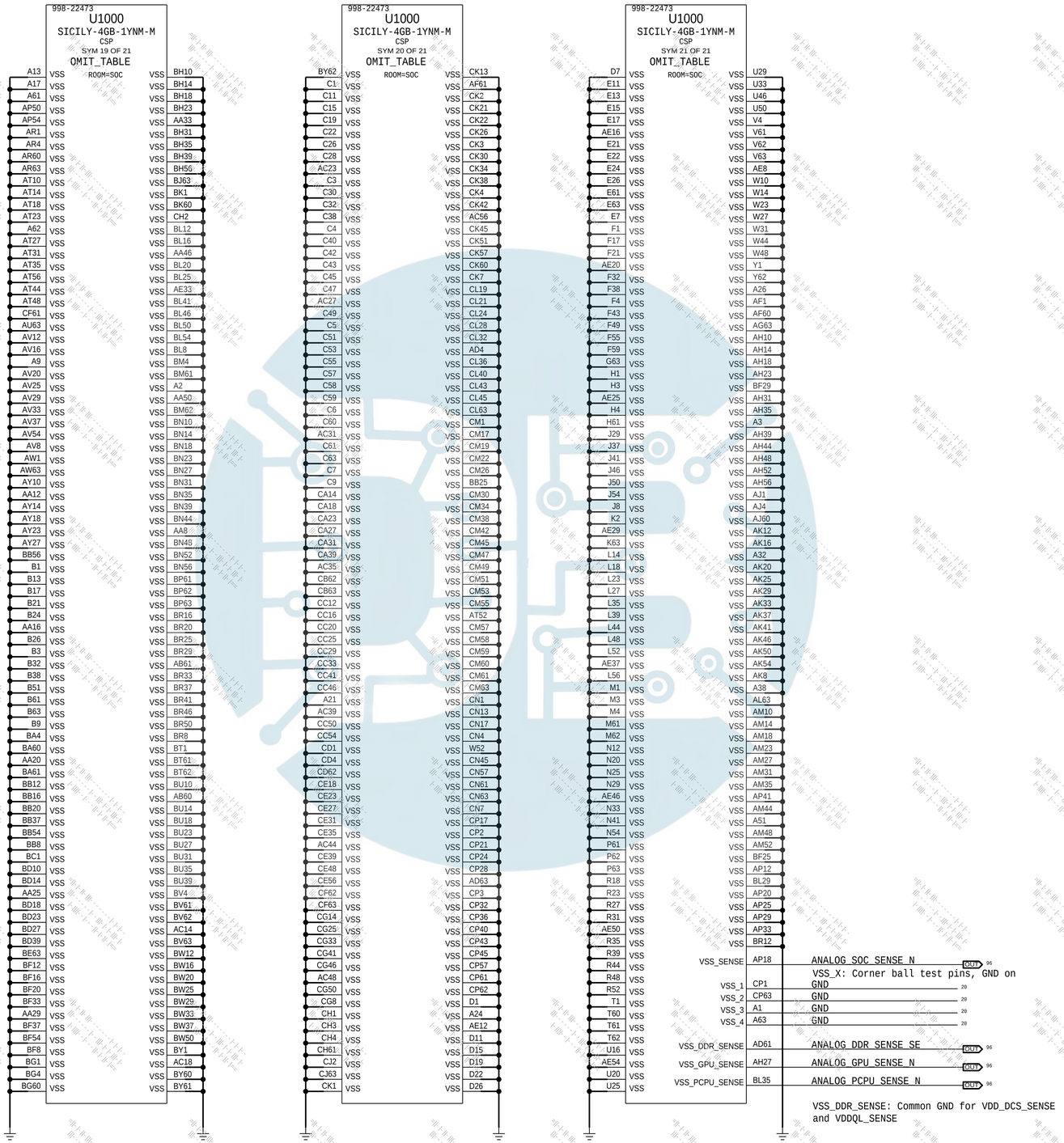
SOC: GND



SYNCING: D52, D53, D54, DEV

PAGE TITLE	SOC: Power (GND)
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REVISION	10.0.0
BRANCH	1
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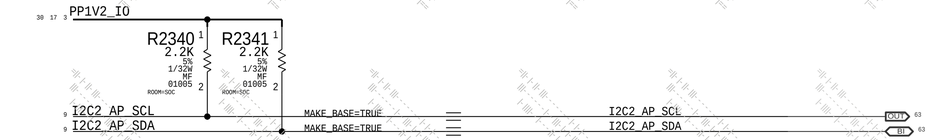
AP/ISP I2C

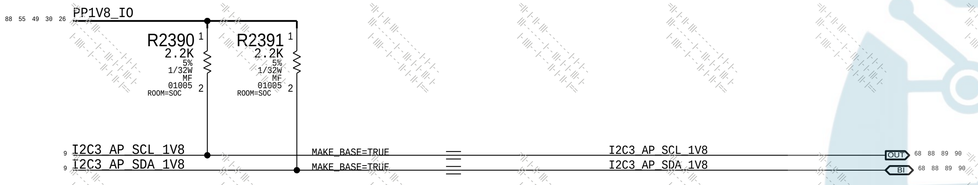
AP I2C0 (Unused)

AP I2C1 (Unused)

AP I2C2

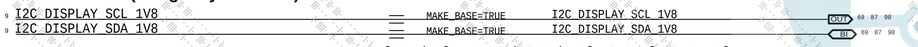


MASTER	AP	NUMBER	I2C2	DIAGS NUMBER	2	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Top Spk Amp	1.2V	0x40	0x80, 0x81	1MHz			



MASTER	AP	NUMBER	I2C3	DIAGS NUMBER	3	SPEED	400kHz	
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION			
Touch EEPROM	1.8V	0x51	0xA2, 0xA3	400kHz	Touch Flex			
Babbage (TFE)	1.8V	0x4B	0x96, 0x97	1MHz	Touch Flex	D52/D54 only		
NOTE: For D52/D54, bus can either be mastered by SoC or Ada								
Roswell	1.8V	0x10	0x20, 0x21	400kHz	Touch Flex	D53 only		
NOTE: Roswell is I2C for D53-only (AID for D52/D54)								

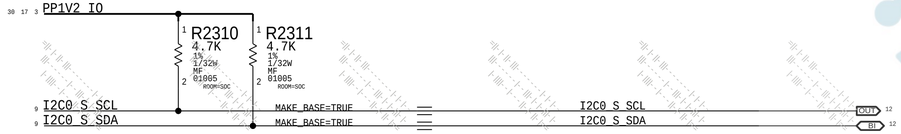
AP I2C4 (Legacy 1.8V)



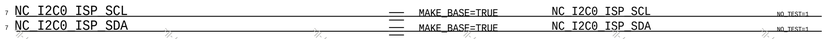
MAKE_BASE for Display PMIC intentional, test feature only

MASTER	AP	NUMBER	I2C4	DIAGS NUMBER	4	SPEED	400kHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Display PMIC	1.8V	0x50	0xA0, 0xA1	400kHz	SoC		
NOTE: is master for FCT "ONLY", DDIC is master for normal operation							

SI2C0



ISP I2C0



ISP I2C1 (Unused)

SYNCING: D52, D53, D54

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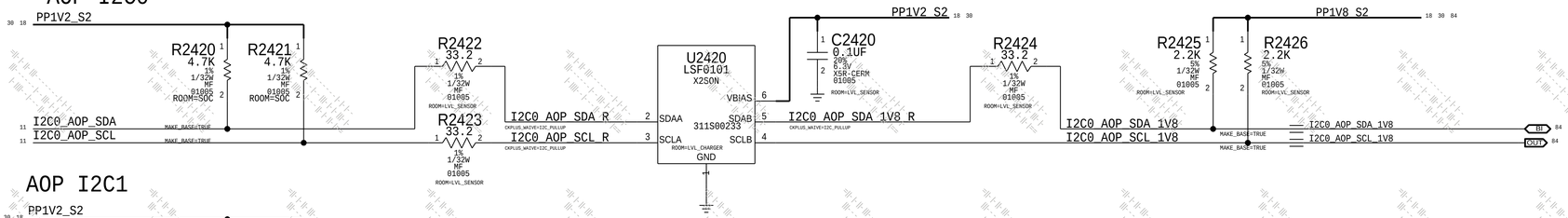
AOP/SMC I2C

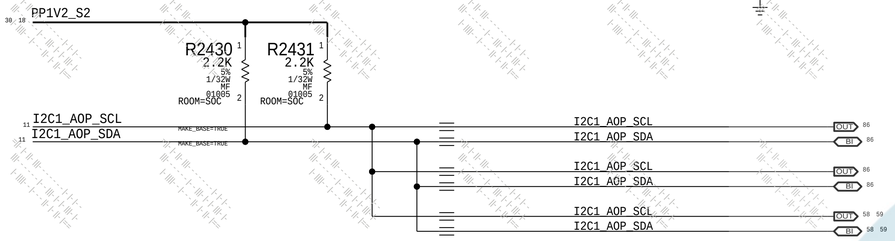
AOP I2C0



MASTER	AOP	NUMBER	I2C0	DIAGS NUMBER	5	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Prox	1.8V	0x58	0xB0, 0xB1	1MHz	Sensor Flex
ALS	1.8V	0x29	0x52, 0x53	1MHz	Sensor Flex
Grievous	1.8V	0x33	0x66, 0x67	1MHz	Sensor Flex
Compass	1.8V	0x0E	0x1C, 0x1D	1MHz	Sensor Flex

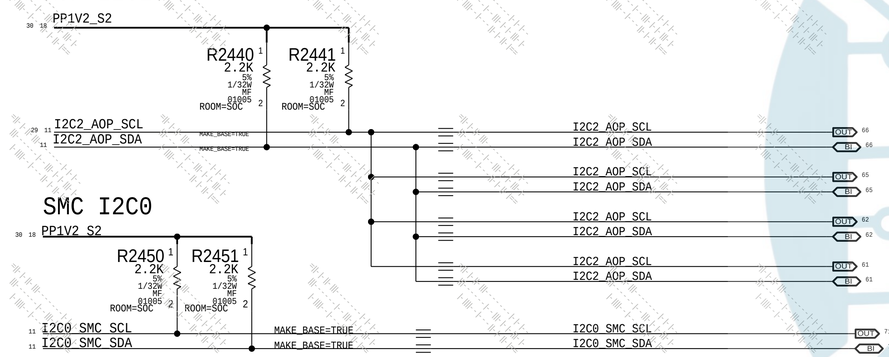
AOP I2C1



MASTER	AOP	NUMBER	I2C1	DIAGS NUMBER	6	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Eiger	1.2V	0x76	0xEC, 0xED	1MHz	Dock
Arc EEPROM	1.2V	0x50	0xA0, 0xA1	1MHz	Arc Flex
Jarvis	1.2V	0x0F	0x1E, 0x1F	1MHz	

AOP I2C2



MASTER	AOP	NUMBER	I2C2	DIAGS NUMBER	7	SPEED	1MHz

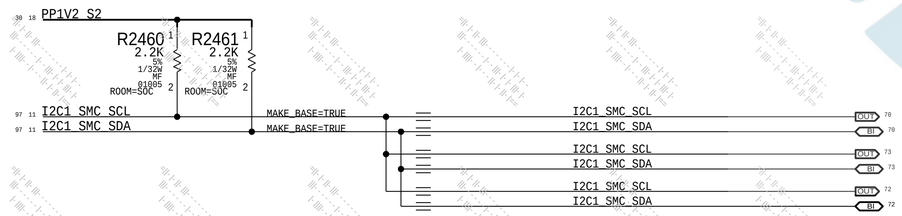
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Sakonnet	1.2V	0x08	0x10, 0x11	1MHz	
Codec	1.2V	0x4A	0x94, 0x95	1MHz	Arc
Amp	1.2V	0x42	0x84, 0x85	1MHz	
Bot Spk Amp	1.2V	0x40	0x80, 0x81	1MHz	

SMC I2C0

MASTER	SMC	NUMBER	I2C0	DIAGS NUMBER	8	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
CCG2B	1.2V	0x12	0x24, 0x25	1MHz	

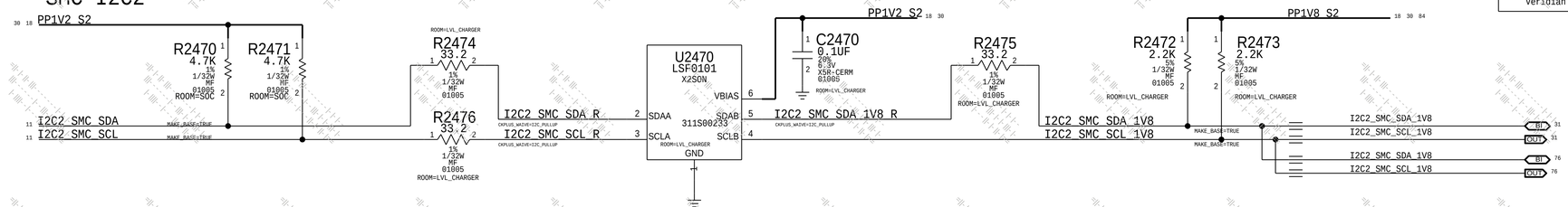
SMC I2C1



MASTER	SMC	NUMBER	I2C1	DIAGS NUMBER	9	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Kraken	1.2V	0x1A	0x34, 0x35	1MHz	
Parrot	1.2V	0x21	0x42, 0x43	1MHz	
Gecko2	1.2V	0x52	0xA4, 0xA5	1MHz	

SMC I2C2



MASTER	SMC	NUMBER	I2C2	DIAGS NUMBER	10	SPEED	400kHz

DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION
Yangtze	1.8V	0x71	0xE2, 0xE3	400kHz	
Veridian	1.8V	0x0B	0x16, 0x17	400kHz	Battery Flex

SYNCING: D52, D53, D54

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SOC: Aliases: I2C AOP/SMC

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AOP GPIOs

* All AOP GPIOs tie into SCM block

SPMI0	SPI	AOP_FUNC0
SPMI0	SPI	AOP_FUNC1
SPMI0	SPI	AOP_FUNC2
SPMI0	SPI	AOP_FUNC3
SPMI1	SPI	AOP_FUNC4
SPMI1	SPI	AOP_FUNC5
SPMI1	SPI	AOP_FUNC6
SPMI1	SPI	AOP_FUNC7
	SPI	AOP_FUNC8
	SPI	AOP_FUNC9
	SPI	AOP_FUNC10
	SPI	AOP_FUNC11
I2C0	SPI	AOP_FUNC12
I2C0	SPI	AOP_FUNC13
I2C0	SPI	AOP_FUNC14
I2C1, I2C0	SPI	AOP_FUNC15
I2C1	I2C0	AOP_FUNC16
I2C1	I2C0	AOP_FUNC17
I2C1	I2C0	AOP_FUNC18
	I2C1	AOP_FUNC19
	I2C1	AOP_FUNC20
	I2C1	AOP_FUNC21
	I2C1	AOP_FUNC22

11	GPIO_SCM_AOP_FROM_IMU_DATARDY	=	GPIO_SCM_AOP_FROM_IMU_DATARDY	MAKE_BASE=TRUE IN	57
11	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	=	GPIO_SCM_AOP_TO_IMU_SPI_CS_L	MAKE_BASE=TRUE OUT	57
11	GPIO_AOP_FROM_PEARL_B2B_DETECT	=	GPIO_AOP_FROM_PEARL_B2B_DETECT	MAKE_BASE=TRUE IN	83
11	NC_DEV_AOP_FUNC3	=	NC_DEV_AOP_FUNC3		21
11	GPIO_SCM_AOP_FROM_R1_INT	=	GPIO_SCM_AOP_FROM_R1_INT	MAKE_BASE=TRUE IN	101
11	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	=	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	MAKE_BASE=TRUE OUT	101
11	GPIO_AOP_TO_R1_TIME_SYNC_L	=	GPIO_AOP_TO_R1_TIME_SYNC_L	MAKE_BASE=TRUE OUT	101
11	GPIO_AOP_TO_CODEC_RESET_L	=	GPIO_AOP_TO_CODEC_RESET_L	MAKE_BASE=TRUE OUT	61 96
11	GPIO_AOP_TO_BB_FORCE_PWM	=	GPIO_AOP_TO_BB_FORCE_PWM	MAKE_BASE=TRUE OUT	99
11	GPIO_AOP_FROM_IRCAM_B2B_DETECT	=	GPIO_AOP_FROM_IRCAM_B2B_DETECT	MAKE_BASE=TRUE IN	82
11	GPIO_SCM_AOP_TO_R1_SPI_CS_L	=	GPIO_SCM_AOP_TO_R1_SPI_CS_L	MAKE_BASE=TRUE OUT	101
11	NC_AOP_FUNC11	=	NC_AOP_FUNC11		20
11	GPIO_AOP_TO_ALS_COEX	=	GPIO_AOP_TO_ALS_COEX	MAKE_BASE=TRUE OUT	84
11	GPIO_AOP_TO_NFC_IRONMAN_EN	=	GPIO_AOP_TO_NFC_IRONMAN_EN	MAKE_BASE=TRUE OUT	100
11	NC_GPIO_AOP_FROM_TOUCH_CTS	=	NC_GPIO_AOP_FROM_TOUCH_CTS	IN	21 88
11	GPIO_SCM_AOP_BI_PROX_INT_L	=	GPIO_SCM_AOP_BI_PROX_INT_L	MAKE_BASE=TRUE IN	75
11	GPIO_SCM_AOP_FROM_ALS_INT_L	=	GPIO_SCM_AOP_FROM_ALS_INT_L	MAKE_BASE=TRUE IN	84
11	GPIO_SCM_AOP_FROM_EIGER_INT_L	=	GPIO_SCM_AOP_FROM_EIGER_INT_L	MAKE_BASE=TRUE IN	86
11	GPIO_SCM_AOP_FROM_COMPASS_INT	=	GPIO_SCM_AOP_FROM_COMPASS_INT	MAKE_BASE=TRUE IN	75
11	GPIO_SCM_AOP_FROM_JARVIS_INT	=	GPIO_SCM_AOP_FROM_JARVIS_INT	MAKE_BASE=TRUE IN	58 59 96
11	GPIO_AOP_FROM_TOUCH_INT_L	=	GPIO_AOP_FROM_TOUCH_INT_L	MAKE_BASE=TRUE IN	68 88
11	NC_AOP_FUNC21	=	NC_AOP_FUNC21		20
11	NC_DEV_AOP_FUNC22	=	NC_DEV_AOP_FUNC22		21

AP GPIOs

AP_GPIO0	10 GPIO_BOARD_REV3	=	GPIO_BOARD_REV3	MAKE_BASE=TRUE IN	3
AP_GPIO1	10 GPIO_BOARD_REV2	=	GPIO_BOARD_REV2	MAKE_BASE=TRUE IN	3
AP_GPIO2	10 GPIO_BOARD_REV1	=	GPIO_BOARD_REV1	MAKE_BASE=TRUE IN	3
AP_GPIO3	10 GPIO_BOARD_REV0	=	GPIO_BOARD_REV0	MAKE_BASE=TRUE IN	3
AP_GPIO4	10 GPIO_AP_CANARY1	=	GPIO_AP_CANARY1	MAKE_BASE=TRUE IN	98
AP_GPIO5	10 GPIO_AP_CANARY2	=	GPIO_AP_CANARY2	MAKE_BASE=TRUE IN	98
AP_GPIO6	10 GPIO_AP_BI_CCG2B_SWDIO	=	GPIO_AP_BI_CCG2B_SWDIO	MAKE_BASE=TRUE BI	71 96
AP_GPIO7	10 GPIO_AP_TO_CCG2B_SWCLK	=	GPIO_AP_TO_CCG2B_SWCLK	MAKE_BASE=TRUE OUT	71 96
AP_GPIO8	10 GPIO_AP_FROM_DISPLAY_PANEL_ID	=	GPIO_AP_FROM_DISPLAY_PANEL_ID	MAKE_BASE=TRUE IN	87 90
AP_GPIO9	10 GPIO_AP_FROM_WLAN_TIME_SYNC	=	GPIO_AP_FROM_WLAN_TIME_SYNC	MAKE_BASE=TRUE IN	98
AP_GPIO10	10 GPIO_AP_TO_BB_PEAK_PWR_IND	=	GPIO_AP_TO_BB_PEAK_PWR_IND	MAKE_BASE=TRUE OUT	99
AP_GPIO11	10 GPIO_AP_TO_BB_COREDUMP	=	GPIO_AP_TO_BB_COREDUMP	MAKE_BASE=TRUE OUT	99
AP_GPIO12	10 GPIO_AP_FROM_BB_RESET_DETECT_L	=	GPIO_AP_FROM_BB_RESET_DETECT_L	MAKE_BASE=TRUE IN	99
AP_GPIO13	10 GPIO_AP_FROM_CODEC_INT_L	=	GPIO_AP_FROM_CODEC_INT_L	MAKE_BASE=TRUE IN	61 96
AP_GPIO14	10 NC_AP_GPIO14	=	NC_AP_GPIO14		20
AP_GPIO15	10 GPIO_AP_TO_SPKRAMP_TOP_RESET_L	=	GPIO_AP_TO_SPKRAMP_TOP_RESET_L	MAKE_BASE=TRUE OUT	63
AP_GPIO16	10 GPIO_AP_FROM_BT_AUDIO_SYNC	=	GPIO_AP_FROM_BT_AUDIO_SYNC	MAKE_BASE=TRUE IN	98
AP_GPIO17	10 GPIO_AP_TO_AMUX_PMU_SYNC	=	GPIO_AP_TO_AMUX_PMU_SYNC	OUT	21
AP_GPIO18	10 NC_DEV_AP_GPIO18	=	NC_DEV_AP_GPIO18		21
AP_GPIO19	10 NC_DEV_AP_GPIO19	=	NC_DEV_AP_GPIO19		21
AP_GPIO20	10 NC_DEV_AP_GPIO20	=	NC_DEV_AP_GPIO20		21
AP_GPIO21	10 NC_DEV_AP_GPIO21	=	NC_DEV_AP_GPIO21		21
AP_GPIO22	10 NC_DEV_AP_GPIO22	=	NC_DEV_AP_GPIO22		21
AP_GPIO23	10 NC_DEV_AP_GPIO23	=	NC_DEV_AP_GPIO23		21
AP_GPIO24	10 NC_DEV_AP_GPIO24	=	NC_DEV_AP_GPIO24		21
AP_GPIO25	10 GPIO_AP_TO_BB_TIME_MARK	=	GPIO_AP_TO_BB_TIME_MARK	MAKE_BASE=TRUE OUT	99
AP_GPIO26	10 NC_DEV_AP_GPIO26	=	NC_DEV_AP_GPIO26		21

Great Dane

SYNCING: D52, D53, D54, DEV

PAGE TITLE
SOC: Aliases: GPIOs

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Misc. SoC Aliases

NAND + USB & MISC

5 PP1V2_IO — PP1V2_IO (MAKE_BASE=TRUE) 20 26 30
5 PP1V2_IO —

94 5 IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU (MAKE_BASE=TRUE) — IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU 27
IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU 70

5 NC_DEV_AP_TMR32_PWM0 — NC_DEV_AP_TMR32_PWM0 (MAKE_BASE=TRUE, NO_TEST=1)
5 NC_DEV_AP_TMR32_PWM1 — NC_DEV_AP_TMR32_PWM1 (MAKE_BASE=TRUE, NO_TEST=1)
5 NC_DEV_AP_TMR32_PWM2 — NC_DEV_AP_TMR32_PWM2 (MAKE_BASE=TRUE, NO_TEST=1)
5 NC_DEV_PAD_MTR_VREF_P — NC_DEV_PAD_MTR_VREF_P (MAKE_BASE=TRUE, NO_TEST=1)
5 NC_DEV_PAD_MTR_VREF_N — NC_DEV_PAD_MTR_VREF_N (MAKE_BASE=TRUE, NO_TEST=1)

5 PP1V2_IO — PP1V2_IO (MAKE_BASE=TRUE) 20 26 30

94 27 IO_PMU_TO_SYSTEM_RESET_L (MAKE_BASE=TRUE) — IO_PMU_TO_SYSTEM_RESET_L 5
IO_PMU_TO_SYSTEM_RESET_L 11
IO_PMU_TO_SYSTEM_RESET_L 11

NC_DEV_SOC_THROTTLE_TRIGGER0 (MAKE_BASE=TRUE, NO_TEST=1) — NC_DEV_SOC_THROTTLE_TRIGGER0 5
NC_DEV_PMU_CPU_TRIGGER0 (MAKE_BASE=TRUE, NO_TEST=1) — NC_DEV_PMU_CPU_TRIGGER0 27

96 IO_AP_FROM_PMU_SW_SHDN_L (MAKE_BASE=TRUE) — IO_AP_FROM_PMU_SW_SHDN_L 5
IO_AP_FROM_PMU_SW_SHDN_L 27
96 IO_AP_FROM_PMU_PRE_UVLO_L (MAKE_BASE=TRUE) — IO_AP_FROM_PMU_PRE_UVLO_L 5
IO_AP_FROM_PMU_PRE_UVLO_L 27

NC_DEV_SOC_THROTTLE_TRIGGER3 (MAKE_BASE=TRUE, NO_TEST=1) — NC_DEV_SOC_THROTTLE_TRIGGER3 5
NC_DEV_PMU_GPU_TRIGGER0 (MAKE_BASE=TRUE, NO_TEST=1) — NC_DEV_PMU_GPU_TRIGGER0 27
NC_DEV_SOC_THROTTLE_TRIGGER4 (MAKE_BASE=TRUE, NO_TEST=1) — NC_DEV_SOC_THROTTLE_TRIGGER4 5
NC_DEV_PMU_GPU_TRIGGER1 (MAKE_BASE=TRUE, NO_TEST=1) — NC_DEV_PMU_GPU_TRIGGER1 27

96 5 IO_SOC_TO_PMU_SOCHOT_RESET_L (MAKE_BASE=TRUE) — IO_SOC_TO_PMU_SOCHOT_RESET_L 27
96 5 CLK_AP_TO_PMU_TST_CLKOUT (MAKE_BASE=TRUE) — CLK_AP_TO_PMU_TST_CLKOUT 27
5 AMUX_SOC_TO_PMU_AMUX_OUT (MAKE_BASE=TRUE) — AMUX_SOC_TO_PMU_AMUX_OUT 27

11 GND
5 GND
5 GND

96 11 IO_AON_TO_AP_XTAL_CFSB (MAKE_BASE=TRUE, CKPLUS_WAIVE=SINGLE_COMP_NET) — IO_AON_TO_AP_XTAL_CFSB 5

96 73 90_EUSB_DBG_PARROT_BI_AP_N (MAKE_BASE=TRUE) — 90_EUSB_DBG_PARROT_BI_AP_N 11
96 73 90_EUSB_DBG_PARROT_BI_AP_P (MAKE_BASE=TRUE) — 90_EUSB_DBG_PARROT_BI_AP_P 11

9 NC_SOC_S_GPIO1 — NC_SOC_S_GPIO1 (MAKE_BASE=TRUE, NO_TEST=1)

VSS CORNER BALLS

16 GND
16 GND
16 GND
16 GND

UART: KRAKEN

70 UART0_AP_TO_KRAKEN_DEBUG_TXD — UART0_AP_TO_KRAKEN_DEBUG_TXD (MAKE_BASE=TRUE) 9 96
70 UART0_AP_FROM_KRAKEN_DEBUG_RXD — UART0_AP_FROM_KRAKEN_DEBUG_RXD (MAKE_BASE=TRUE) 9 96
70 UART4_AP_TO_KRAKEN_ACC_TXD — UART4_AP_TO_KRAKEN_ACC_TXD (MAKE_BASE=TRUE) 9 96
70 UART4_AP_FROM_KRAKEN_ACC_RXD — UART4_AP_FROM_KRAKEN_ACC_RXD (MAKE_BASE=TRUE) 9 96

DISPLAY

8 NC_SOC_DWI_CLK — NC_SOC_DWI_CLK (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_SOC_DWI_DATA — NC_SOC_DWI_DATA (MAKE_BASE=TRUE, NO_TEST=1)

8 NC_TOUCH_BSYNC1_DISP — NC_TOUCH_BSYNC1_DISP
8 NC_EDP_HPD_DISP — NC_EDP_HPD_DISP (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_SOC_DISP_I2C_SCL — NC_SOC_DISP_I2C_SCL (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_SOC_DISP_I2C_SDA — NC_SOC_DISP_I2C_SDA (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_SOC_DISP_POL — NC_SOC_DISP_POL (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_SOC_DISP_AGPIO — NC_SOC_DISP_AGPIO (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_SOC_DISP_EXT_HPD — NC_SOC_DISP_EXT_HPD (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_SOC_DISP_TOUCH_EB — NC_SOC_DISP_TOUCH_EB (MAKE_BASE=TRUE, NO_TEST=1)

8 NC_DEV_LPDP_AP_TX0P — NC_DEV_LPDP_AP_TX0P
8 NC_DEV_LPDP_AP_TX0N — NC_DEV_LPDP_AP_TX0N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_LPDP_AP_TX1P — NC_DEV_LPDP_AP_TX1P
8 NC_DEV_LPDP_AP_TX1N — NC_DEV_LPDP_AP_TX1N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_LPDP_AP_TX2P — NC_DEV_LPDP_AP_TX2P
8 NC_DEV_LPDP_AP_TX2N — NC_DEV_LPDP_AP_TX2N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_LPDP_AP_TX3P — NC_DEV_LPDP_AP_TX3P
8 NC_DEV_LPDP_AP_TX3N — NC_DEV_LPDP_AP_TX3N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_LPDP_AP_AUXP — NC_DEV_LPDP_AP_AUXP
8 NC_DEV_LPDP_AP_AUXN — NC_DEV_LPDP_AP_AUXN (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_LPDP_AP_RCALP — NC_DEV_LPDP_AP_RCALP (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_DEV_LPDP_AP_RCALN — NC_DEV_LPDP_AP_RCALN (MAKE_BASE=TRUE, NO_TEST=1)

8 NC_LPDP_EXT_AP_TX0_P — NC_LPDP_EXT_AP_TX0_P
8 NC_LPDP_EXT_AP_TX0_N — NC_LPDP_EXT_AP_TX0_N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_LPDP_EXT_AP_TX1_P — NC_LPDP_EXT_AP_TX1_P
8 NC_LPDP_EXT_AP_TX1_N — NC_LPDP_EXT_AP_TX1_N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_LPDP_EXT_AP_TX2_P — NC_LPDP_EXT_AP_TX2_P
8 NC_LPDP_EXT_AP_TX2_N — NC_LPDP_EXT_AP_TX2_N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_LPDP_EXT_AP_TX3_P — NC_LPDP_EXT_AP_TX3_P
8 NC_LPDP_EXT_AP_TX3_N — NC_LPDP_EXT_AP_TX3_N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_LPDP_EXT_AP_AUX_P — NC_LPDP_EXT_AP_AUX_P
8 NC_LPDP_EXT_AP_AUX_N — NC_LPDP_EXT_AP_AUX_N (MAKE_BASE=TRUE, NO_TEST=1)
8 NC_LPDP_EXT_AP_RCAL_P — NC_LPDP_EXT_AP_RCAL_P
8 NC_LPDP_EXT_AP_RCAL_N — NC_LPDP_EXT_AP_RCAL_N (MAKE_BASE=TRUE, NO_TEST=1)

ISP

7 NC_ISP_GPIO_1 — NC_ISP_GPIO_1 (MAKE_BASE=TRUE, NO_TEST=1)
7 NC_ISP_GPIO_2 — NC_ISP_GPIO_2 (MAKE_BASE=TRUE, NO_TEST=1)
7 NC_SENSOR2_CLK_AP — NC_SENSOR2_CLK_AP (MAKE_BASE=TRUE, NO_TEST=1)
7 NC_SENSOR3_CLK_AP — NC_SENSOR3_CLK_AP (MAKE_BASE=TRUE, NO_TEST=1)

SPI (AP)

9 SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2 — SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2 (MAKE_BASE=TRUE) 3 22 96
9 SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1 — SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1 (MAKE_BASE=TRUE) 3 22
9 SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0 — SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0 (MAKE_BASE=TRUE) 3 22

9 SPI3_AP_FROM_CODEC_MISO — SPI3_AP_FROM_CODEC_MISO (MAKE_BASE=TRUE) 61 96
9 SPI3_AP_TO_CODEC_MOSI — SPI3_AP_TO_CODEC_MOSI (MAKE_BASE=TRUE) 61 96
9 SPI3_AP_TO_CODEC_SCLK — SPI3_AP_TO_CODEC_SCLK (MAKE_BASE=TRUE) 61
9 SPI3_AP_TO_CODEC_CS_L — SPI3_AP_TO_CODEC_CS_L (MAKE_BASE=TRUE) 61 96

SOC: PCIe

6 NC_DEV_PCIE_GP0_AP_CLKREQ_L — NC_DEV_PCIE_GP0_AP_CLKREQ_L (MAKE_BASE=TRUE, NO_TEST=1)
6 NC_DEV_PCIE_GP0_AP_REFCLK_P — NC_DEV_PCIE_GP0_AP_REFCLK_P (MAKE_BASE=TRUE, NO_TEST=1)
6 NC_DEV_PCIE_GP0_AP_REFCLK_N — NC_DEV_PCIE_GP0_AP_REFCLK_N (MAKE_BASE=TRUE, NO_TEST=1)
6 NC_DEV_PCIE_GP0_AP_RX_P — NC_DEV_PCIE_GP0_AP_RX_P (MAKE_BASE=TRUE, NO_TEST=1)
6 NC_DEV_PCIE_GP0_AP_RX_N — NC_DEV_PCIE_GP0_AP_RX_N (MAKE_BASE=TRUE, NO_TEST=1)
6 NC_DEV_PCIE_GP0_AP_TX_P — NC_DEV_PCIE_GP0_AP_TX_P (MAKE_BASE=TRUE, NO_TEST=1)
6 NC_DEV_PCIE_GP0_AP_TX_N — NC_DEV_PCIE_GP0_AP_TX_N (MAKE_BASE=TRUE, NO_TEST=1)
6 NC_DEV_PCIE_GP0_AP_RESET_L — NC_DEV_PCIE_GP0_AP_RESET_L (MAKE_BASE=TRUE, NO_TEST=1)

SOC: Serial

9 NC_UART1_AP_CTS_L — NC_UART1_AP_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART1_AP_RTS_L — NC_UART1_AP_RTS_L (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART1_AP_RXD — NC_UART1_AP_RXD (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART1_AP_TXD — NC_UART1_AP_TXD (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART2_AP_CTS_L — NC_UART2_AP_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART2_AP_RTS_L — NC_UART2_AP_RTS_L (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART2_AP_RXD — NC_UART2_AP_RXD (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART2_AP_TXD — NC_UART2_AP_TXD (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART3_AP_CTS_L — NC_UART3_AP_CTS_L (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART3_AP_RXD — NC_UART3_AP_RXD (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_I2S1_AP_MCLK — NC_I2S1_AP_MCLK (MAKE_BASE=TRUE, NO_TEST=1)
10 NC_AP_GPIO14 — NC_AP_GPIO14 (MAKE_BASE=TRUE, NO_TEST=1)

9 NC_I2S2_AP_MCLK — NC_I2S2_AP_MCLK (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_SSPI0_MISO_AP — NC_SSPI0_MISO_AP (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_SSPI0_SCLK_AP — NC_SSPI0_SCLK_AP (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_SSPI0_MOSI_AP — NC_SSPI0_MOSI_AP (MAKE_BASE=TRUE, NO_TEST=1)
9 NC_UART6_AP_RXD_1V8 — NC_UART6_AP_RXD_1V8 (MAKE_BASE=TRUE, NO_TEST=1)

SOC: AOP

11 GPIO_AOP_TO_WLAN_CONTEXT_A — GPIO_AOP_TO_WLAN_CONTEXT_A (MAKE_BASE=TRUE) 98
11 GPIO_AOP_TO_WLAN_CONTEXT_B — GPIO_AOP_TO_WLAN_CONTEXT_B (MAKE_BASE=TRUE) 98
19 NC_AOP_FUNC11 — NC_AOP_FUNC11 (MAKE_BASE=TRUE, NO_TEST=1)
19 NC_AOP_FUNC21 — NC_AOP_FUNC21 (MAKE_BASE=TRUE, NO_TEST=1)

NUB

11 NC_NUB_GPIO5 — NC_NUB_GPIO5 (MAKE_BASE=TRUE)

11 GND
11 NC_DEV_JTAG_TDI — NC_DEV_JTAG_TDI (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_JTAG_TDO — NC_DEV_JTAG_TDO (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_DEV_JTAG_TRST_L — NC_DEV_JTAG_TRST_L (MAKE_BASE=TRUE, NO_TEST=1)
11 PP1V2_S2 — PP1V2_S2 (MAKE_BASE=TRUE) 26 30 57 72 82 83 87 88 90 99 100

96 68 11 SWD_NUB_TO_PMU_TOUCH_SWCLK (MAKE_BASE=TRUE) — SWD_NUB_TO_PMU_TOUCH_SWCLK 27

SYNCING: D52, D53, D54

PAGE TITLE: SOC: Aliases: Misc

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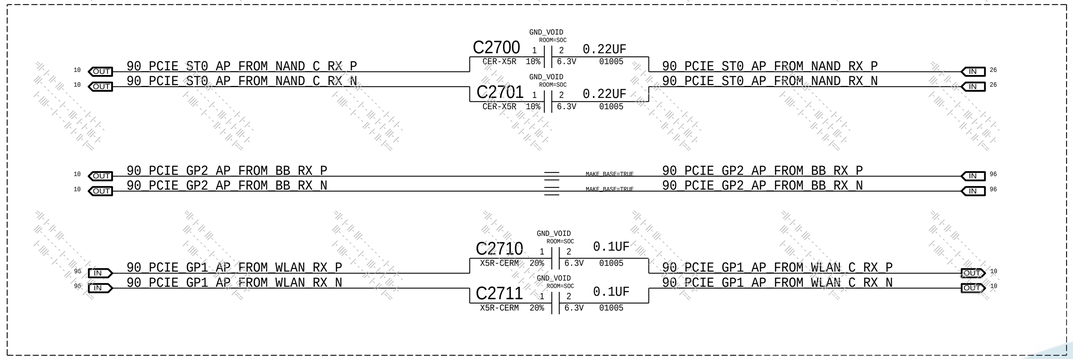
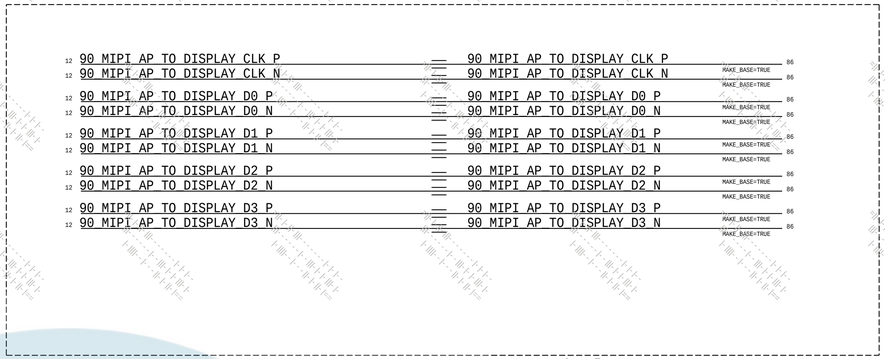




AP I2C0 (Unused)

13 NC_I2C0_AP_SCL — NC_I2C0_AP_SCL (MAKE_BASE=TRUE, NO_TEST=1)
13 NC_I2C0_AP_SDA — NC_I2C0_AP_SDA (MAKE_BASE=TRUE, NO_TEST=1)

AP I2C1 (Unused)

13 NC_I2C1_AP_SCL — NC_I2C1_AP_SCL (MAKE_BASE=TRUE, NO_TEST=1)
13 NC_I2C1_AP_SDA — NC_I2C1_AP_SDA (MAKE_BASE=TRUE, NO_TEST=1)

AP SPMI2

13 NC_DEV_AP_SPMI2_SCLK — NC_DEV_AP_SPMI2_SCLK (MAKE_BASE=TRUE, NO_TEST=1)
13 NC_DEV_AP_SPMI2_SDATA — NC_DEV_AP_SPMI2_SDATA (MAKE_BASE=TRUE, NO_TEST=1)

SPI (AP)

13 NC_SPI1_MISO_1V8 — NC_SPI1_MISO_1V8 (NO_TEST=1)
13 NC_SPI1_MOSI_1V8 — NC_SPI1_MOSI_1V8 (MAKE_BASE=TRUE, NO_TEST=1)
13 NC_SPI1_CS_L_1V8 — NC_SPI1_CS_L_1V8 (MAKE_BASE=TRUE, NO_TEST=1)
13 NC_SPI1_SCLK_1V8_R — NC_SPI1_SCLK_1V8_R (MAKE_BASE=TRUE, NO_TEST=1)
13 NC_SPI1_SCLK_1V8_R — CKPLUS_WAIVE=MULTI_PIN_NC_NETS (MAKE_BASE=TRUE)

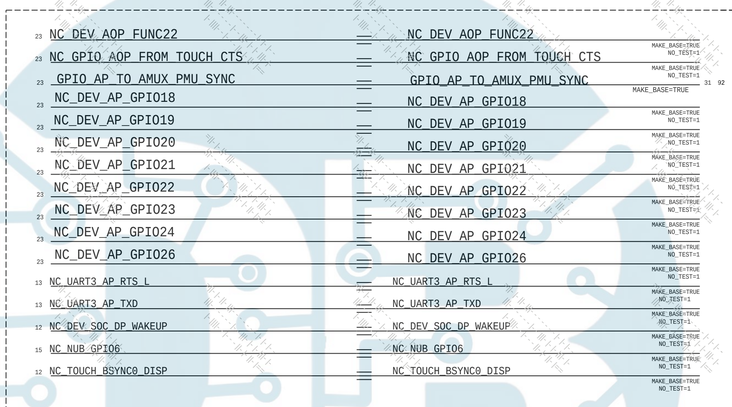
13 SPI2_AP_FROM_TOUCH_MISO — SPI2_AP_FROM_TOUCH_MISO (65 92)
13 SPI2_AP_TO_TOUCH_MOSI — SPI2_AP_TO_TOUCH_MOSI (MAKE_BASE=TRUE, 65 92)
13 SPI2_AP_TO_TOUCH_SCLK — SPI2_AP_TO_TOUCH_SCLK (MAKE_BASE=TRUE, 65 92)
13 SPI2_AP_TO_TOUCH_CS_L — SPI2_AP_TO_TOUCH_CS_L (MAKE_BASE=TRUE, 65 92)

LPDP

ISP: LPDP Lanes

11 90 LPDP_ISP_FROM_WIDE_RX_D0_N — 90 LPDP_ISP_FROM_WIDE_RX_D0_N (75)
11 90 LPDP_ISP_FROM_WIDE_RX_D0_P — 90 LPDP_ISP_FROM_WIDE_RX_D0_P (75)
11 90 LPDP_ISP_FROM_WIDE_RX_D1_N — 90 LPDP_ISP_FROM_WIDE_RX_D1_N (75)
11 90 LPDP_ISP_FROM_WIDE_RX_D1_P — 90 LPDP_ISP_FROM_WIDE_RX_D1_P (75)
11 90 LPDP_ISP_FROM_WIDE_RX_D2_N — 90 LPDP_ISP_FROM_WIDE_RX_D2_N (75)
11 90 LPDP_ISP_FROM_WIDE_RX_D2_P — 90 LPDP_ISP_FROM_WIDE_RX_D2_P (75)
11 90 LPDP_ISP_FROM_FCAM_RX_D0_N — 90 LPDP_ISP_FROM_FCAM_RX_D0_N (78)
11 90 LPDP_ISP_FROM_FCAM_RX_D0_P — 90 LPDP_ISP_FROM_FCAM_RX_D0_P (78)
11 90 LPDP_ISP_FROM_FCAM_RX_D1_N — 90 LPDP_ISP_FROM_FCAM_RX_D1_N (78)
11 90 LPDP_ISP_FROM_FCAM_RX_D1_P — 90 LPDP_ISP_FROM_FCAM_RX_D1_P (78)
11 90 LPDP_ISP_FROM_TELE_RX_D0_P — 90 LPDP_ISP_FROM_TELE_RX_D0_P (76)
11 90 LPDP_ISP_FROM_TELE_RX_D0_N — 90 LPDP_ISP_FROM_TELE_RX_D0_N (76)
11 90 LPDP_ISP_FROM_TELE_RX_D1_P — 90 LPDP_ISP_FROM_TELE_RX_D1_P (76)
11 90 LPDP_ISP_FROM_TELE_RX_D1_N — 90 LPDP_ISP_FROM_TELE_RX_D1_N (76)
11 90 LPDP_ISP_FROM_TELE_RX_D2_P — 90 LPDP_ISP_FROM_TELE_RX_D2_P (76)
11 90 LPDP_ISP_FROM_TELE_RX_D2_N — 90 LPDP_ISP_FROM_TELE_RX_D2_N (76)
11 90 LPDP_ISP_FROM_SWIDE_RX_D2_N — 90 LPDP_ISP_FROM_SWIDE_RX_D2_N (76)
11 90 LPDP_ISP_FROM_SWIDE_RX_D2_P — 90 LPDP_ISP_FROM_SWIDE_RX_D2_P (76)
11 90 LPDP_ISP_FROM_SWIDE_RX_D0_P — 90 LPDP_ISP_FROM_SWIDE_RX_D0_P (76)
11 90 LPDP_ISP_FROM_SWIDE_RX_D0_N — 90 LPDP_ISP_FROM_SWIDE_RX_D0_N (76)
11 90 LPDP_ISP_FROM_SWIDE_RX_D1_N — 90 LPDP_ISP_FROM_SWIDE_RX_D1_N (76)
11 90 LPDP_ISP_FROM_SWIDE_RX_D1_P — 90 LPDP_ISP_FROM_SWIDE_RX_D1_P (76)
11 90 LPDP_ISP_FROM_JASPER_RX_D0_P — 90 LPDP_ISP_FROM_JASPER_RX_D0_P (77)
11 90 LPDP_ISP_FROM_JASPER_RX_D0_N — 90 LPDP_ISP_FROM_JASPER_RX_D0_N (77)

CKPLUS_WAIVE=DIFFPAIR_BADTERM, MAKE_BASE=TRUE

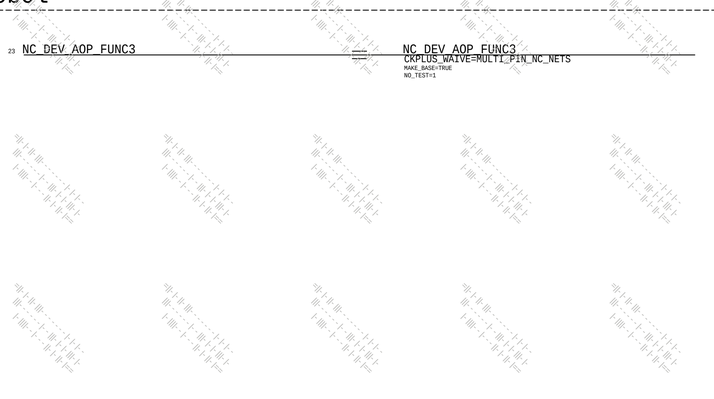


LPDP

ISP: LPDP Aux

11 NC_LPDP_ISP_AUX_RX_D0P — NC_LPDP_ISP_AUX_RX_D0P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D1P — NC_LPDP_ISP_AUX_RX_D1P (MAKE_BASE=TRUE, NO_TEST=1)
11 LPDP_ISP_BI_SWIDE_AUX_RX_D2P — LPDP_ISP_BI_SWIDE_AUX_RX_D2P (MAKE_BASE=TRUE, 76)
11 NC_LPDP_ISP_AUX_RX_D3P — NC_LPDP_ISP_AUX_RX_D3P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D4P — NC_LPDP_ISP_AUX_RX_D4P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D5P — NC_LPDP_ISP_AUX_RX_D5P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D6P — NC_LPDP_ISP_AUX_RX_D6P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D7P — NC_LPDP_ISP_AUX_RX_D7P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D8P — NC_LPDP_ISP_AUX_RX_D8P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D9P — NC_LPDP_ISP_AUX_RX_D9P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D10P — NC_LPDP_ISP_AUX_RX_D10P (MAKE_BASE=TRUE, NO_TEST=1)
11 NC_LPDP_ISP_AUX_RX_D11P — NC_LPDP_ISP_AUX_RX_D11P (MAKE_BASE=TRUE, NO_TEST=1)

Kobol



SYNCING: NONE

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S5E NAND

SUBSYSTEM SPECIFIC BOM TABLES

ZQ Resistor

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0784	1	RES,3000HM,1%,1/32W,01005	R2901	CRITICAL	S5E

Note: Dev Board adds an S4E option

I_VCC = 1150mA MAX (1us PEAK POWER)
PP2V625_NAND

C2913 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2916 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2919 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2921 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2949 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2950 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2951 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2952 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2953 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2954 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2936 220PF 5% 25V C0G 01005 ROOM=NAND
C2937 220PF 5% 25V C0G 01005 ROOM=NAND
C2934 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2938 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2935 22PF 5% 16V C0G 01005 ROOM=NAND
C2939 22PF 5% 16V C0G 01005 ROOM=NAND

I_VDDIO1 (@ 1.2V) = 72mA MAX
PP1V2_IO

C2941 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2924 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2926 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2910 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
C2911 220PF 5% 25V C0G 01005 ROOM=NAND
C2955 220PF 5% 25V C0G 01005 ROOM=NAND
FL2925 10-OHM-1.1A 01005 ROOM=NAND 155S0876
C2956 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2957 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2958 22PF 5% 16V C0G 01005 ROOM=NAND
C2925 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
R2963 2.0 5% 1/32W MF 01005 ROOM=NAND
C2963 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

I_VDDI02 (@ 1.2V) = 384mA MAX
PP1V2_IO

C2931 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2929 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2943 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2945 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2947 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2959 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2960 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2912 220PF 5% 25V C0G 01005 ROOM=NAND
C2915 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2917 22PF 5% 16V C0G 01005 ROOM=NAND
C2961 220PF 5% 25V C0G 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3
C2918 47PF 5% 16V NP0-C0G 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3
C2914 22PF 5% 16V C0G 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3
C2962 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2

I_VDD_= 820mA MAX
PP0V83_NAND

C2948 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2902 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2905 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
FL2923 10-OHM-1.1A 01005 ROOM=NAND 155S0876
C2923 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

C2900 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2901 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2922 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2927 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2940 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2942 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2944 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2946 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2907 330PF 10% 16V CER-X7R 01005 ROOM=NAND
C2903 220PF 5% 25V C0G 01005 ROOM=NAND
C2908 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2904 22PF 5% 16V C0G 01005 ROOM=NAND
C2909 330PF 10% 16V CER-X7R 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3
C2906 220PF 5% 25V C0G 01005 ROOM=NAND PACK_IGNORE=TRUE PACK_OPTION=DS2,DS3

U2900
H23BFG8127AEQ-BC
LGA
SYM 2 OF 2
335S00436
ROOM=NAND
OMIT_TABLE

D3 VCC
E12 VCC
G4 VCC
L12 VCC
R2 VCC
J2 VDDIO_1
K9 VDDIO_1
T5 VDDIO_1
J6 PCIE_AVDD_H
L2 AVDD1X_PLL
E10 VDDIO_2
E2 VDDIO_2
N2 VDDIO_2
P9 VDDIO_2
G6 VDD
G8 VDD
L6 VDD
L8 VDD
R6 VDD
R8 VDD
J8 PCIE_VDD
M9 PCIE_VDD
N6 PCIE_VDD
N8 PCIE_VDD
R4 VDD_PLL
(VCCQ_IO)
(VCCQ_ANI)
(VDD)
VSS
VSS_R
VPP F3 NC_DEV_NAND_VPP 23
VQPS F5 GND 23
VQPS used for fuse programming, GND in system

A12 A2 B1 B13 C12 C2 D1 D13 F1 F11 F13 F7 F9 H1 H11 H13 H3 H5 H9 J10 K1 K13 K5 K7 L10 M1 M13 M5 M7 N10 N4 P1 P11 P13 P3 P7 R10 T1 T13 T7 T9 U12 U2 A10 A4 A6 A8 U10 U4 U6 U8

NOTES:
INT_PU = internal pull up to VDDIO_1
INT_PD = internal pull down to VSS
Internal pulls are 40kOhm (min), 80kOhm (typ), 165kOhm (max)

5 IN CLK_AP_TO_NAND_24M
96 5 IN IO_AP_TO_NAND_RESET_L
23 GND
96 6 IN 90_PCIE_ST0_AP_TO_NAND_REFCLK_P
96 6 IN 90_PCIE_ST0_AP_TO_NAND_REFCLK_N
6 BI PCIE_ST0_AP_BI_NAND_CLKREQ_L
6 IN 90_PCIE_ST0_AP_TO_NAND_TX_P
6 IN 90_PCIE_ST0_AP_TO_NAND_TX_N
21 OUT 90_PCIE_ST0_AP_FROM_NAND_RX_P
21 OUT 90_PCIE_ST0_AP_FROM_NAND_RX_N
6 IN PCIE_ST0_AP_TO_NAND_PERST_L

ANALOG_NAND_PCIE_RESREF (for dev)
C2920 10PF 5% 16V NP0/C0G 01005 ROOM=NAND
R2904 200 0.5% 1/32W TK 01005 ROOM=NAND
Keep ZQ trace DCR < 200mOhm
ANALOG_NAND_ZQ_0
ANALOG_NAND_ZQ_1 (for dev)
R2900 300 1% 1/32W MF 01005-1 ROOM=NAND
R2901 300 1% 1/32W MF 01005-1 ROOM=NAND
OMIT_TABLE

U2900
H23BFG8127AEQ-BC
LGA
SYM 1 OF 2
335S00436
ROOM=NAND
OMIT_TABLE

CLK_IN M3
RESET* L4
TRST* (INT PD) G10
PCIE_REFCLK_P K11
PCIE_REFCLK_N J12
PCIE_CLKREQ* P5
PCIE_RX0_P M11
PCIE_RX0_N N12
PCIE_TX0_P R12
PCIE_TX0_N T11
EXT_NCE/PERST* E8
PCIE_RESREF H7
ZQ_0 C10
ZQ_1 K3

(INT PU) EXT_D0/BOOT0 B3 GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L IN 29 96
(INT PD) EXT_D1/BOOT1 C4 IO_AP_TO_NAND_FW_STRAP IN 5 96
EXT_D2/BOOT2/SPINAND_SCLK/SPI_SCLK B5 SPI0_AP_TO_S5E_SCLK_BOOT_CONFIG0 IN 3 20
EXT_D3/SPINAND_MISO/SPI_MISO/SWD_UID C6 SPI0_AP_FROM_S5E_MISO_BOOT_CONFIG2 OUT 3 20 96
EXT_D4/SPI_CS B7 GND 23
EXT_D5/SPINAND_MOSI/SPI_MOSI/SWD_UID1 C8 SPI0_AP_TO_S5E_MOSI_BOOT_CONFIG1 IN 3 20
EXT_D6/BOOT3 B9 GND 23
EXT_D7/SPF_N B11 IO_PMU_TO_NAND_SYSTEM_ALIVE IN 27 96
(INT PU) EXT_DQS/BCM_N D11 NC_DEV_NAND_BCM_L 23
(INT PU) EXT_NRE/JTAG_TMS D7 SWD_AP_BI_NAND_SWDIO BI 5 96
(INT PU) EXT_NWE/JTAG_TCK E6 SWD_AP_TO_MANY_SWCLK IN 5 99 101
EXT_RNB/JTAG_TDO E4 GND 23
(INT PU) EXT_CLE/JTAG_TDI D5 NC_DEV_NAND_JTAG_TDI 23
(INT PU) EXT_ALE/JTAG_SEL D9 GND 23
DROOP* T3
WP* G2 PP1V2_IO 23
ANI0_VREF G12 ANALOG_NAND_ANI0_VREF 96
ANI1_VREF J4 ANALOG_NAND_ANI1_VREF 96

NAND Capacities

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00436	1	HYNIX,3Dv5,64Gb,Ultimate	U2900	CRITICAL	NAND:ULTIMATE
335S00437	1	HYNIX,3Dv5,128Gb,Supreme	U2900	CRITICAL	NAND:SUPREME
335S00438	1	HYNIX,3Dv5,256Gb,Extreme	U2900	CRITICAL	NAND:EXTREME
335S00439	1	HYNIX,3Dv5,512Gb,Max	U2900	CRITICAL	NAND:MAX

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00461	335S00436	NAND:ULTIMATE	U2900	KIOXIA,BiCS4.5,64Gb,Ultimate
335S00469	335S00436	NAND:ULTIMATE	U2900	WD,BiCS4.5,64Gb,Ultimate
335S00462	335S00437	NAND:SUPREME	U2900	KIOXIA,BiCS4.5,128Gb,Supreme
335S00470	335S00437	NAND:SUPREME	U2900	WD,BiCS4.5,128Gb,Supreme
335S00464	335S00438	NAND:EXTREME	U2900	KIOXIA,BiCS6.5,256Gb,Extreme
335S00472	335S00438	NAND:EXTREME	U2900	WD,BiCS4.5,256Gb,Extreme
335S00467	335S00439	NAND:MAX	U2900	KIOXIA,BiCS4.5,512Gb,Max
335S00475	335S00439	NAND:MAX	U2900	WD,BiCS4.5,512Gb,Max

SYNCING: D52, D53, D54

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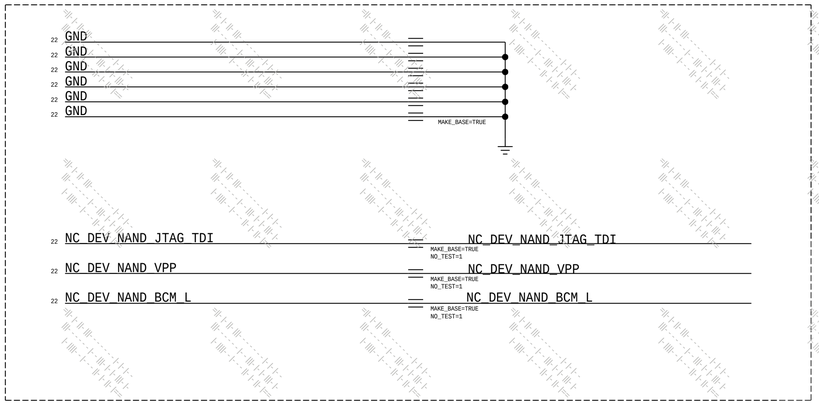
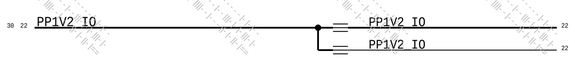
DEV BOARD COMPATIBILITY



VDDIO2



SYNCING: D52, D53, D54

PAGE TITLE
NAND: Aliases

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PMU DOCUMENTS RADAR #: 62945546

BUCK4 — 2.2A MAX

VOLTAGE=1.0625 (DEFAULT, DVC = 0.98V - 1.1V)
PP1V06_S2

C3343 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3342 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3341 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3340 220PF 5% 25V C0G 01005 ROOM=PMU

L3340 0.47UH-3.7A-0.034OHM PIJD16140H-SM ROOM=PMU 152S00984

LX_BUCK4 → A10, B10 → BUCK4_LX

OMIT XW3340 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

ANALOG_FB_BUCK4 → D10 → BUCK4_FB
C10 → BUCK4_VSS_FB

LOCAL FEEDBACK

BUCK5 — 2.0A MAX

VOLTAGE=0.763 (0.614V - 0.763V)
PP_AVE_S1
I_LOAD = 1.7A (MAX)

C3351 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU PACK_OPTION=D54
C3350 20UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU PACK_OPTION=D54
C3354 220PF 5% 25V C0G 01005 ROOM=PMU

C3351 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C3350 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV

L3350 0.47UH-3.7A-0.034OHM PIJD16140H-SM ROOM=PMU 152S00984

LX_BUCK5 → A12, B12 → BUCK5_LX

OMIT XW3350 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

ANALOG_FB_BUCK5 → D12 → BUCK5_FB
C12 → BUCK5_VSS_FB

MID-PLANE FEEDBACK

BUCK6 — 2.1A MAX

VOLTAGE=1.2 (DEFAULT)
PP1V2_S4

C3364 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3363 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3362 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3361 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C3360 220PF 5% 25V C0G 01005 ROOM=PMU

L3360 0.47UH-3.7A-0.034OHM PIJD16140H-SM ROOM=PMU 152S00984

LX_BUCK6 → A2, B2 → BUCK6_LX

OMIT XW3360 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

ANALOG_FB_BUCK6 → D2 → BUCK6_FB
C2 → BUCK6_VSS_FB

LOCAL FEEDBACK

BUCK7 — 2.2A MAX

VOLTAGE=0.769 (DEFAULT)
PP_SRAM_S1

C3371 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV
C3371 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU PACK_OPTION=D54
C3370 220PF 5% 25V C0G 01005 ROOM=PMU

L3370 0.47UH-20%-4.0A-0.05OHM PIJD2012-SM ROOM=PMU 152S00985

LX_BUCK7 → T17, T18 → BUCK7_LX

OMIT XW3370 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

ANALOG_FB_BUCK7 → T15 → BUCK7_FB
T16 → BUCK7_VSS_FB

MID-PLANE FEEDBACK

BUCK8 — 2.2A MAX

VOLTAGE=0.75 (0.585V - 0.75V)
PP_DISP_S1

C3382 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU
C3381 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3380 220PF 5% 25V C0G 01005 ROOM=PMU

L3380 0.47UH-2.9A-0.072OHM PIJD1608FE-SM ROOM=PMU 152S00982

LX_BUCK8 → A14, B14 → BUCK8_LX

OMIT XW3380 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

ANALOG_FB_BUCK8 → D14 → BUCK8_FB
C14 → BUCK8_VSS_FB

MID-PLANE FEEDBACK

BUCK9 — 0.6A MAX

VOLTAGE=1.1
PP1VX_DISPLAY_S2
I_LOAD = 0.2A (MAX)

C3392 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3391 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU
C3390 220PF 5% 25V C0G 01005 ROOM=PMU

L3390 1UH-20%-2.2A-0.06OHM PIJR20120H-SM ROOM=PMU 152S00821

LX_BUCK9 → Y5 → BUCK9_LX

OMIT XW3390 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

ANALOG_FB_BUCK9 → V5 → BUCK9_FB
W5 → BUCK9_VSS_FB

LOCAL FEEDBACK

BUCK9 NOTES:
1. Output is default OFF
2. Voltage adjusts dynamically based on display vendor and mode (~1.0V to ~1.15V)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	(C3391)	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

U3300 TMLL69A0 WLCSP SYM 2 OF 5

998-19244 CRITICAL

BUCK4_LX, BUCK4_FB, BUCK4_VSS_FB
BUCK5_LX, BUCK5_FB, BUCK5_VSS_FB
BUCK6_LX, BUCK6_FB, BUCK6_VSS_FB
BUCK7_LX, BUCK7_FB, BUCK7_VSS_FB
BUCK8_LX, BUCK8_FB, BUCK8_VSS_FB
BUCK9_LX, BUCK9_FB, BUCK9_VSS_FB

BUCK0 — 13.8A MAX

L3300 1UH-20%-3.6A-0.062OHM PIWE20160H-SM ROOM=PMU 152S00876

BUCK0_LX0 ← F18 ← LX_BUCK0_P0

L3301 0.1UH-20%-6.1A-0.019OHM ROOM=PMU MTFE2016-2SM 152S00897

BUCK0_LX1 ← B17, B18 ← LX_BUCK0_P1 (UPPER_COIL_IN → 1, UPPER_COIL_OUT → 3)
BUCK0_LX3 ← D17, D18 ← LX_BUCK0_P3 (LOWER_COIL_IN → 2, LOWER_COIL_OUT → 4)

L3302 0.1UH-20%-6.1A-0.019OHM ROOM=PMU MTFE2016-2SM 152S00897

BUCK0_LX2 ← H17, H18 ← LX_BUCK0_P2 (UPPER_COIL_IN → 1, UPPER_COIL_OUT → 3)
BUCK0_LX4 ← K17, K18 ← LX_BUCK0_P4 (LOWER_COIL_IN → 2, LOWER_COIL_OUT → 4)

BUCK0_FB ← H15 ← ANALOG_FB_BUCK0
BUCK0_VSS_FB ← J16

(0.528V - 1.061V) VOLTAGE=1.061 PP_CPU_PCORE

C3300 220PF 5% 25V C0G 01005 ROOM=PMU
C3301 16UF 20% 4V X5R 0402-0.1MM-1 ROOM=PMU 2020-MLCC (138S00313)
C3302 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

OMIT XW3301 SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION

<--- ANALOG_FB_BUCK0_R

R3300 499 1% 1/32W MF 01005 ROOM=PMU (110S00026)

OMIT XW3300 SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION

ANALOG_PCPU_SENSE_P → IN

DIE SENSE; PLACE XW NEAR U1000.BL37

BUCK1 — 10.0A MAX

L3310 1UH-20%-3.6A-0.062OHM PIWE20160H-SM ROOM=PMU 152S00876

BUCK1_LX0 ← Y13 ← LX_BUCK1_P0

L3311 0.1UH-20%-6.1A-0.019OHM ROOM=PMU MTFE2016-2SM 152S00897

BUCK1_LX1 ← W17, Y17 ← LX_BUCK1_P1 (UPPER_COIL_IN → 1, UPPER_COIL_OUT → 3)
BUCK1_LX2 ← W15, Y15 ← LX_BUCK1_P2 (LOWER_COIL_IN → 2, LOWER_COIL_OUT → 4)

BUCK1_FB ← U13 ← ANALOG_FB_BUCK1
BUCK1_VSS_FB ← V13

OMIT XW3310 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

REMOTE FEEDBACK; PLACE NEAR SOC

(0.542V - 1.044V) VOLTAGE=1.044 PP_GPU

C3310 220PF 5% 25V C0G 01005 ROOM=PMU
C3311 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3312 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK2 — 4.9A MAX

L3320 1UH-20%-2.2A-0.06OHM PIJR20120H-SM ROOM=PMU 152S00821

BUCK2_LX0 ← Y9 ← LX_BUCK2_P0

L3321 0.22UH-20%-5.8A-0.04OHM 1608 ROOM=PMU 152S00818

BUCK2_LX1 ← W11, Y11 ← LX_BUCK2_P1

BUCK2_FB ← U9 ← ANALOG_FB_BUCK2
BUCK2_VSS_FB ← V9

OMIT XW3320 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

MID-PLANE FEEDBACK

(0.612V - 0.79V) VOLTAGE=0.79 PP_SOC_S1

C3320 220PF 5% 25V C0G 01005 ROOM=PMU
C3321 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU

BUCK3 — 1.2A MAX

L3330 1UH-20%-2.2A-0.06OHM PIJR20120H-SM ROOM=PMU 152S00821

BUCK3_LX ← V3, W3, Y3 ← LX_BUCK3

BUCK3_FB ← W1 ← ANALOG_FB_BUCK3
BUCK3_VSS_FB ← V1

OMIT XW3330 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

LOCAL FEEDBACK

VOLTAGE=1.8 PP1V8_S4

C3330 220PF 5% 25V C0G 01005 ROOM=PMU
C3331 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3332 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3333 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3334 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

SYNCING: D52, D53, D54

PAGE TITLE: SYS PWR: PMU: Bucks (1/5)
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PMU DOCUMENTS RADAR #: 62945546

PP_VDD_MAIN

PLACE IN VICINITY OF PMU FOR BULK CAP

C3404 15UF 20% 6.3V X6R 0402-0.1MM-1 ROOM=PMU
C3405 15UF 20% 6.3V X6R 0402-0.1MM-1 ROOM=PMU
C3406 15UF 20% 6.3V X6R 0402-0.1MM-1 ROOM=PMU
C3407 15UF 20% 6.3V X6R 0402-0.1MM-1 ROOM=PMU
C3408 15UF 20% 6.3V X6R 0402-0.1MM-1 ROOM=PMU

PLACE ON PMU CORNERS TO FILL 01005 RING AROUND PMU

C3480 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3481 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3482 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU
C3483 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU

Buck0
C3490 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C3491 2.7UF 20% 6.3V X5R 0201 ROOM=PMU 2020-MLCC

Buck1
138S00325
C3492 2.7UF 20% 6.3V X5R 0201 ROOM=PMU 2020-MLCC

Buck11
C3493 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

998-19244
CRITICAL
U3300 TMLL69A0 WLCSP SYM 3 OF 5 ROOM=PMU

C3450 0.22UF	A1	VDD_BUCK13_10_6_4
	B1	VDD_BUCK13_10_6_4
C3451 0.22UF	A3	VSS_BUCK13_6
	B3	VSS_BUCK13_6
C3452 0.22UF	A5	VDD_BUCK13_10_6_4
	B5	VDD_BUCK13_10_6_4
C3459 0.22UF	A7	VSS_BUCK10
	B7	VSS_BUCK10
C3453 0.22UF	A9	VDD_BUCK13_10_6_4
	B9	VDD_BUCK13_10_6_4
C3454 0.22UF	A11	VSS_BUCK5_4
	B11	VSS_BUCK5_4
C3455 0.22UF	A13	VDD_BUCK8_5
	B13	VDD_BUCK8_5
C3456 0.22UF	A15	VSS_BUCK8
	B15	VSS_BUCK8
	A16	VSS_BUCK0
	A17	VSS_BUCK0
	A18	VSS_BUCK0
C3457 0.22UF	C17	VDD_BUCK11_7_0
	C18	VDD_BUCK11_7_0
C3469 0.22UF	E17	VSS_BUCK0
	E18	VSS_BUCK0
C3458 0.22UF	G17	VDD_BUCK11_7_0
	G18	VDD_BUCK11_7_0
C3460 0.22UF	J17	VSS_BUCK0
	J18	VSS_BUCK0
C3470 0.22UF	L17	VDD_BUCK11_7_0
	L18	VDD_BUCK11_7_0
C3461 0.22UF	N17	VSS_BUCK11
	N18	VSS_BUCK11
C3462 0.22UF	R17	VDD_BUCK11_7_0
	R18	VDD_BUCK11_7_0
C3463 0.22UF	U17	VSS_BUCK7
	U18	VSS_BUCK7
	V18	VSS_BUCK1
	W18	VSS_BUCK1
	Y18	VSS_BUCK1
C3464 0.22UF	W16	VDD_BUCK12_2_1
	Y16	VDD_BUCK12_2_1
C3471 0.22UF	W14	VSS_BUCK1
	Y14	VSS_BUCK1
C3465 0.22UF	W12	VDD_BUCK12_2_1
	Y12	VDD_BUCK12_2_1
C3472 0.22UF	W10	VSS_BUCK2
	Y10	VSS_BUCK2
C3466 0.22UF	W8	VDD_BUCK12_2_1
	Y8	VDD_BUCK12_2_1
C3467 0.22UF	W6	VSS_BUCK12_9
	Y6	VSS_BUCK12_9
C3468 0.22UF	W4	VDD_BUCK9_3
	Y4	VDD_BUCK9_3
	V4	VDD_BUCK9_3
	V2	VSS_BUCK3
	W2	VSS_BUCK3
	Y1	VSS_BUCK3
	Y2	VSS_BUCK3

BUCK10 BUCK11 BUCK12 BUCK13 BUCK INPUT

BUCK10_LX0 A8 LX_BUCK10_P0
BUCK10_LX1 A6 LX_BUCK10_P1
BUCK10_LX1 B6
BUCK10_FB D8 ANALOG_FB_BUCK10
BUCK10_VSS_FB C8

L3400 1UH-20%-2.2A-0.060HM PIJR20120H-SM ROOM=PMU 152S00021
L3401 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU 152S00818
OMIT XW3400 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
MID-PLANE FEEDBACK

(0.765V - 1.099V) VOLTAGE=1.099 PP_CPU_SRAM 30
C3401 220PF 5% 25V C0G 01005 ROOM=PMU
C3402 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3403 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK10 4.2A MAX

BUCK11_LX0 M18 LX_BUCK11_P0
BUCK11_LX1 P17
BUCK11_LX1 P18
BUCK11_FB M15 ANALOG_FB_BUCK11
BUCK11_VSS_FB M16

L3410 1UH-20%-2.2A-0.060HM PIJR20120H-SM ROOM=PMU 152S00821
L3411 0.22UH-20%-5.8A-0.040HM 1608 ROOM=PMU 152S00818
OMIT XW3410 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
REMOTE FEEDBACK

(0.519V - 0.828V) VOLTAGE=0.828 PP_CPU_ECORE 30
C3410 220PF 5% 25V C0G 01005 ROOM=PMU
C3411 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3412 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU PACK_OPTION=D54
C3412 15UF 20% 6.3V X6R 0402-0.1MM-1 ROOM=PMU PACK_IGNORE=TRUE PACK_OPTION=D52,D53,DEV

BUCK11 3.8A MAX

BUCK12_LX W7 LX_BUCK12
BUCK12_LX V7
BUCK12_FB U7 ANALOG_FB_BUCK12
BUCK12_VSS_FB V7

L3420 0.47UH-3.7A-0.034OHM PIJD1614OH-SM ROOM=PMU 152S00984
OMIT XW3420 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
LOCAL FEEDBACK; PLACE NEAR U3300.N1

(DEFAULT) VOLTAGE=0.88 PP0V9_S1 30
C3420 220PF 5% 25V C0G 01005 ROOM=PMU
C3421 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3422 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3423 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK12 2.1A MAX

BUCK13_LX A4 LX_BUCK13
BUCK13_FB C4 ANALOG_FB_BUCK13
BUCK13_VSS_FB B4

L3430 0.47UH-2.9A-0.072OHM PIJD1608FE-SM ROOM=PMU 152S00982
OMIT XW3430 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION
MID-PLANE FEEDBACK

(0.615V - 0.842V) VOLTAGE=0.842 PP_DCS_S1 30
C3432 220PF 5% 25V C0G 01005 ROOM=PMU
C3430 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU
C3431 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=PMU

BUCK13 1.0A MAX

SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: PMU: Bucks (2/5)
DRAWING NUMBER	051-05170
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REVISION	10.0.0
BRANCH	1
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PMU:LDOs

PMU DOCUMENTS RADAR #: 62945546

SUBSYSTEM SPECIFIC BOM TABLES

4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	(C3515)	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	(C3515)	CAP,X5R,4UF,0201,0.55MM,KYOCERA

15uF 0402 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	[SEE BELOW]	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

(C3509,C3510,C3520,C3530,C3540,C3545,C3555,C3566,C3570)

NOTES:
1. PP1V2_SOC is low noise SOC rail, PP1V2_IO is its noisy cousin
2. PPVAR_EIGER_S2 typical output is 1.8V, max 3.275V during calibration
3. LDO3 and LDO8 are operating near-dropout by design (1.24Vin, 1.2Vout)
4. Max system load currents provided in power tree, radar # 43311246
5. OTP will disable LDO13 and LDO14 for all programs. Software must enable them for D52 and D54.
6. LDO6 is OTP programmed to be a load switch

998-19244
CRITICAL

U3300
TMLL69A0
WLCSP
SYM 1 OF 5
ROOM=PMU

PP_VDD_BOOST	F5,H4,J2,J4,J5,K1,K2,K3	VDD_BOOST_LDO	LDO GROUP 1
PP_VDD_MAIN	K5	VDD_MAIN_LDO	LDO GROUP 2 & INTERNAL POWER
PP_VDD_BOOST	H5	VDD_LDO2	LDO GROUP 3
PP_VDD_MAIN	G5	VDD_LDO15	
PP1V2_S4	L5	VDD_LDO14_3	LDO GROUP 4
PP1V06_S2	H2	VDD_LDO4	LDO GROUP 5
PP1V2_S4	F3	VDD_LDO6	
PP1V2_S4	F2	VDD_LDO8	
PP0V9_S1	G2	VDD_LDO11	
PP0V9_S1	G3	VDD_LDO12	
PP1V8_S4	N4	VIN_SW2_1_0	BUCK3 SWITCHES
	N5	VIN_SW2_1_0	
	P4	VIN_SW2_1_0	
	P5	VIN_SW2_1_0	
PP1V2_S4	N3	VIN_SW5_4_3	BUCK6 SWITCHES
	P1	VIN_SW5_4_3	
	P2	VIN_SW5_4_3	
	P3	VIN_SW5_4_3	
PP0V9_S1	N1	VIN_SW6	BUCK12 SWITCHES
	N2	VIN_SW6	

VLDO1	J6	PP3V3_USB_S2	VOLTAGE=3.3
VLDO5	L1	PP2V625_NAND	VOLTAGE=2.625
VLDO5	L2		
VLDO5	L3		
VLDO7	H3	PP3V0_S2	VOLTAGE=3.0
VLDO10	J1	PP3V0_DISPLAY_S2	VOLTAGE=3.0
VLDO13	J3	PP3V1_TOUCH_S2	VOLTAGE=3.15
VLDO9	K6	PP1V8_ALWAYS	VOLTAGE=1.8
VLDOINT	K4	PP1V5_VLDOINT	VOLTAGE=1.5
VMBX	L9	PMU_VMBX	
VCP_OUT	N6	PMU_VPUMP	
VLDO2	H6	PP1V8_AUDIO_VA_S2	VOLTAGE=1.8
VLDO15	G6	PPVAR_EIGER_S2	VOLTAGE=3.0
VLDO3	L4	PP1V2_SOC	VOLTAGE=1.2
VLDO14	L6	PP1V2_TOUCH_S2	VOLTAGE=1.22
VLDO4	H1	PP0V7_VDD_LOW_S2	VOLTAGE=0.7
VLDO6	F4	PP1V2_NFC_S2	VOLTAGE=1.2
VLDO8	F1	PP1V0_S4	VOLTAGE=1V
VLDO11	G1	PP0V6_VDDQL_S1	VOLTAGE=0.6
VLDO12	G4	PP0V78_SOC_FIXED_S1	VOLTAGE=0.78

PMU LDO Capability:

LDO1	200 mA MAX	PP3V3_USB_S2
LDO5	1200 mA MAX	PP2V625_NAND
LDO7	250 mA MAX	PP3V0_S2
LDO10	50 mA MAX	PP3V0_DISPLAY_S2
LDO13	150 mA MAX	PP3V1_TOUCH_S2
LDO9	10 mA MAX	PP1V8_ALWAYS
LDO2	50 mA MAX	PP1V8_AUDIO_VA_S2
LDO15	100 mA MAX	PPVAR_EIGER_S2
LDO3	400 mA MAX	PP1V2_SOC
LDO14	150 mA MAX	PP1V2_TOUCH_S2
LDO4	300 mA MAX	PP0V7_VDD_LOW_S2
LDO6	250 mA MAX	PP1V2_NFC_S2
LDO8	600 mA MAX	PP1V0_S4
LDO11	700 mA MAX	PP0V6_VDDQL_S1
LDO12	580 mA MAX	PP0V78_SOC_FIXED_S1

R4	BUCK3_SW0	PP1V8_S2	VOLTAGE=1.8
R5			VOLTAGE=1.8
M4	BUCK3_SW1	PP1V8_IO	VOLTAGE=1.8
M5	BUCK3_SW2	PP1V8_TOUCH_S2	VOLTAGE=1.8
R1	BUCK6_SW0	PP1V2_S2	VOLTAGE=1.2
R2	BUCK6_SW1	PP1V2_IO	VOLTAGE=1.2
R3			VOLTAGE=1.2
M3	BUCK6_SW2	PP1V2_S1	VOLTAGE=1.2
M1	BUCK12_SW0	PP0V83_NAND	VOLTAGE=0.83
M2			

BUCK_SW0: 700 mA MAX, 50mOhm MAX
BUCK_SW1: 350 mA MAX, 50mOhm MAX
BUCK_SW2: 200 mA MAX, 125mOhm MAX
BUCK_SW3: 200 mA MAX, 125mOhm MAX
BUCK_SW4: 890 mA MAX, 25mOhm MAX
BUCK_SW5: 50 mA MAX, 125mOhm MAX
BUCK_SW6: 820 mA MAX, 50mOhm MAX

Place XW3580 near U3300.F1
(star route from PMU to Arrow)

SYNCING: D52, D53, D54, DEV

DCR Requirement: <50mOhm MAX (30mOhm NOM) for Rin + Rout
Rin = DCR from XW3420 (PP0V9_S1 feedback) to U3300.N1 (SW6 input)
Rout = DCR from U3300.M1 (SW6 output) to U2900.G6 (NAND VDD)

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PMU DOCUMENTS RADAR #: 62945546

PMU - GPIOs + DIOs

See 50000123 for IO settings

AMUX CAPS

AMUX RCAM PVDD — 27 50 51

C3673 8PF ±0.5PF 16V NP0/C0G 01005 ROOM=PMU

AMUX PMU FROM CAM PMU — 27 43 46 50

BOMOPTION:AGAIN_23:054

C3671 8PF ±0.5PF 16V NP0/C0G 01005 ROOM=PMU

30 PP1V2_S2

R3661 20.0K 5% 1/32W MF 01005 ROOM=PMU

998-19244 CRITICAL

U3300 TMLL69A0 WLCSP SYM 4 OF 5 ROOM=PMU

RESET_IN3: Enabled only in PMU awake state

VBUS_DETECT: OTP programmed to be active low

FORCE_SYNC: SCAN_ACTIVE can tap into 1.2V or 1.8V side, whichever is easier

LDO13_EN: Wired to Ada (D52/D54)
LDO13_EN: GND (D53)

C3660: PMU Buck Noise

AMUX_A7 tied to GND for AMUX calibration

96 11	IN	IO_SOC_TO_PMU_WDOG_RESET	L12	RESET_IN1		
96 70	IN	IO_PMU_FROM_KRAKEN_RESET	M11	RESET_IN2		
20	IN	IO_SOC_TO_PMU_SOCHOT_RESET_L	L11	RESET_IN3		
30		NC_DEV_PMU_SHDN_1V8	L10	SHDN		
30		NC_DEV_PMU_CRASH_L_1V8	M10	CRASH*		
70 35 29	OUT	IO_PMU_KRAKEN_TO_DOTARA_RESET_L_1V8	L7	FAULT_OUT*		
94 20	OUT	IO_PMU_TO_SYSTEM_RESET_L	N9	RESET*		
30 29	OUT	IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY	L8	ACTIVE_READY		
96 22	OUT	IO_PMU_TO_NAND_SYSTEM_ALIVE	M9	SYS_ALIVE		
30	IN	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	R14	VBUS_DETECT	SYSTEM INTERFACE	
30		NC_DEV_PMU_REQUEST_DFU	K13	REQUEST_DFU		
20	OUT	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	N15	FORCE_DFU		
29 11	OUT	CLK_PMU_TO_AOP_32K	T5	SLEEP_32K		
89 88	OUT	CLK_PMU_TO_TOUCH_32K_1V8	R7	OUT_32K		
90 89 88 75 68 46 43 35 33	IN	IO_TOUCH_TO_MANY_SCAN_ACTIVE_1V8	T13	FORCE_SYNC		
96 73 70	IN	IO_KRAKEN_TO_PARROT_PMU_USB_EN	N13	LDO1_EN		
68	IN	GPIO_PMU_FROM_TOUCH_LDO_EN	P6	LDO13_EN		
20	IN	AMUX_SOC_TO_PMU_AMUX_OUT	F9	AMUX_A0	AMUX	
90 87 69	IN	IO_DISPLAY_TO_DPMIC_VOUT3_EN_1V8	E11	AMUX_A1		
27		AMUX_PMU_TO_ADC_IN	E10	AMUX_A2		
72	IN	AMUX_PMU_FROM_GECKO	F12	AMUX_A3		
51 50 27	IN	AMUX_RCAM_PVDD	E8	AMUX_A4		
70 60 27	IN	IO_PMU_FROM_KRAKEN_USB_BRICK_ID_TIA	F13	AMUX_A5		
30		GND	E9	AMUX_A6		
30	IN	GND	E12	AMUX_A7		
94	OUT	AMUX_PMU_AY	G13	AMUX_AY		
96 21	IN	GPIO_AP_TO_AMUX_PMU_SYNC	E7	AMUX_B0		
69	IN	AMUX_PMU_FROM_DISPLAY	F10	AMUX_B1		
96 35	IN	DOTARA_SUPER_GPIO_1V8	F8	AMUX_B2		
50 46 43 27	IN	AMUX_PMU_FROM_CAM_PMU	G11	AMUX_B3		
96 55 44	IN	GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	G8	AMUX_B4		
29	IN	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	G9	AMUX_B5		
20	IN	CLK_AP_TO_PMU_TST_CLKOUT	H9	AMUX_B6		
101 98 96 29	IN	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	H8	AMUX_B7		
94	OUT	AMUX_PMU_BY	G12	AMUX_BY		
30		GND	M7	DFT_CTRL0	DFT	
20	IN	SWD_NUB_TO_PMU_TOUCH_SWCLK	M6	DFT_CTRL1		
30		GND	T2	VSS_DFT_2		
30		GND	E5	VPP		
35 11	IN	SPMI0_NUB_TO_PMU_DOTARA_CLK	P14	SPMI_SCLK	SPMI	
35 11	BI	SPMI0_NUB_BI_PMU_DOTARA_DATA	N14	SPMI_SDATA		
		CLK_PMU_XTAL1_XIN_32K	T1	XIN	32KHZ OSCILLATOR	
		CLK_PMU_XTAL2_XOUT_32K	U1	XOUT		
		VSS_PMU_XTAL	U3	VSS		
		GND	T3	NXTAL_MEMS		
30		PP1V2_S4	P13	VDDIO1V2	1V2 LOGIC INPUT POWER	

VDD_MAIN_SNS: Drop single via to VDD_MAIN plane, place XW3650 directly at the via to the plane

NO_XNET_CONNECTION ROOM=PMU OMIT XW3650 SHORT-28L-0.05MM-SM

K9		PMU_VDD_MAIN_SNS		VDD_MAIN_SNS	
P8	OUT 20	IO_AP_FROM_PMU_PRE_UVLO_L		UVWARN*	
T7	OUT 30	NC_DEV_PMU_VDD_BOOST_UVLO_L		VDD_BOOST_UVLO*	
U15	OUT 29	NC_DEV_PMU_CPU_TRIGGER0		CPU_TRIGGER0*	THROTTLERS
T14	OUT 29	IO_AP_FROM_PMU_SW_SHDN_L		CPU_TRIGGER1*	
R13	OUT 26	NC_DEV_PMU_GPU_TRIGGER0		GPU_TRIGGER0*	
U14	OUT 20	NC_DEV_PMU_GPU_TRIGGER1		GPU_TRIGGER1*	
J9		PMU_VDD_MAIN_SENSE_N		IBAT	
J10		PMU_VDD_MAIN_SENSE_P		VBAT	ADC
F11	IN 27 60 70	IO_PMU_FROM_KRAKEN_USB_BRICK_ID_TIA		BRICK_ID1	
G14		ANALOG_PMU_VDD_MAIN_SENSE_FILT		BRICK_ID2	
H10		AMUX_PMU_TO_ADC_IN CKPLUS_WAIVE=SINGLE_COMP_NET		ADC_IN	
K15	IN 77	IO_BUTTON_VOL_DOWN_L_1V8		BUTTON1	
M13	IN 77	IO_BUTTON_SIDE_L_1V8		BUTTON2	
N12	IN 77	IO_BUTTON_VOL_UP_L_1V8		BUTTON3	BUTTONS
M12	IN 77	IO_BUTTON_RINGER_A_1V8		BUTTON4	
L14	30	NC_DEV_PMU_DOWN_BUTTONO_L		BUTTONO1	
L13	30	NC_DEV_PMU_SIDE_BUTTONO_L		BUTTONO2	
M14	OUT 30 96	GPIO_PMU_TO_SOC_DOUBLE_CLICK_DET_L		DBLCLICK_DET	
P7	29	NC_DEV_PMU_GPIO_1		GPIO1	HV,HLD (S4)
R12	29	GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L		GPIO2	HLD (S4)
P12	29	SWD_NUB_BI_PMU_SWDIO		GPIO3	SWDIO
P11	29	GPIO_S4_PMU_TO_R1_RESET_L		GPIO4	
U12	29	GPIO_S4_PMU_TO_WLAN_REG_ON		GPIO5	
T12	29	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K		GPIO6	HLD (S4)
R11	29	NC_DEV_PMU_GPIO_7		GPIO7	
N11	29	GPIO_PMU_FROM_WLAN_HOST_WAKE		GPIO8	
N10	29	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L		GPIO9	
T11	29	GPIO_PMU_TO_CCG2B_RESET_L		GPIO10	
U11	29	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8		GPIO11	
U10	29	GPIO_PMU_FROM_CODEC_WAKE_L		GPIO12	
T10	29	GPIO_PMU_TO_AMUX_PMU_SUPER_TP		GPIO13	
R10	29	GPIO_PMU_NFC_TO_ARCAMP_RESET_L		GPIO14	
N8	29	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L		GPIO15	
M8	29	GPIO_PMU_NFC_TO_ARCAMP_TRIG		GPIO16	
P10	29	I2C2_AOP_SCL		GPIO17	
T9	29	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8		GPIO18	
R9	29	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8		GPIO19	
R8	29	GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8		GPIO20	
P9	29	GPIO_SEQ_PMU_TO_BBPMU_RESET_L		GPIO21	SEQ
T8	29	GPIO_SEQ_PMU_TO_NFC_EN		GPIO22	
U5	29	GPIO_SEQ_PMU_TO_BOOST_EN_1V8		GPIO23	
T6	29	GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8		GPIO24	
R6	29	GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8 GPIO25 requires 200k PD if used (glitch mitigation)		GPIO25	HV,SEQ
H13	39	NTC_FOREHEAD_P		TDEV1	
H12	40	NTC_RADIO_BB_SE		TDEV2	
J13	40	NTC_RADIO_PA_SE		TDEV3	NTC
J12	39	NTC_AP_P		TDEV4	
H11	39	NTC_BATTERY_P		TDEV5	
G10		ANALOG_PMU_TCAL		TCAL	
J8		ANALOG_PMU_VREF_ADC		VREF_ADC	
K10		ANALOG_PMU_VREF		VREF	
J11		ANALOG_PMU_VSS_REF		IREF	REFERENCES
K11		ANALOG_PMU_VSS_REF		VSS_REF	

GPIO1 requires 200k PD if used (glitch mitigation)

HLD (S4) = Hold Capable
HV = High Voltage
SEQ = Sequenced

BATTERY CURRENT SENSE FILTER

R3671 1.00K 1% 1/32W MF 01005 ROOM=PMU — PMU_VDD_MAIN_SENSE_R_N — IN 32

NO_XNET_CONNECTION C3670 0.22UF 10% 6.3V CER-X5R 01005 ROOM=PMU

R3670 1.00K 1% 1/32W MF 01005 ROOM=PMU — PMU_VDD_MAIN_SENSE_R_P — IN 32

BATTERY VOLTAGE SENSE FILTER

CRITICAL R3603 9.53K 1% 1/32W MF 01005 ROOM=PMU — ANALOG_PMU_VDD_MAIN_SENSE — IN 76

C3603 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

48731558

PMU GPIO Pulls

30 PP1V8_ALWAYS

R3610 100K 5% 1/32W MF 01005 ROOM=PMU — 96 31 30 29 GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8

33 29 GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8

R3600 200K 1% 1/32W MF 01005 ROOM=PMU

REFERENCE PIN LAYOUT NOTES

1. Surface route IREF (U3300.J11) to VSS_REF (U3300.K11)
2. Drop via under VSS_REF (U3300.K11) to XW3646
3. Tie XW3646 directly from via to GND plane
4. Place XW3647 near U3300.J7

MEMS Oscillator #1 (Active)

PP1V8_ALWAYS 26 27 30 77

C3653 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

Y3601 32.768KHZ-50PPM CSP 197S00228 — NC, CLKOUT, VDD, GND

PACK_IGNORE=TRUE PACK_OPTION=D53,DEV BOMOPTION=32K:MEMS1

MEMS Oscillator #2 (Active)

PP1V8_ALWAYS 26 27 30 77

C3654 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

Y3602 32.768KHZ-50PPM CSP 197S00228 — NC, CLKOUT, VDD, GND — CLK_PMU_XTAL2_XOUT_32K_R

R3652 200 1% 1/32W MF 01005 ROOM=SOC

PACK_IGNORE=TRUE PACK_OPTION=D53 BOMOPTION=32K:MEMS2

PACK_IGNORE=TRUE PACK_OPTION=D53 BOMOPTION=32K:MEMS2

XTAL Oscillator (Passive)

OMIT_TABLE Y3600 32.768KHZ-20PPM-12.5PF 1.6X1.00-SM CRITICAL ROOM=PMU

OMIT_TABLE C3651 22PF 2% 16V C0G 01005 ROOM=PMU

OMIT_TABLE C3652 22PF 2% 16V C0G 01005 ROOM=PMU

ROOM=PMU SHORT-20L-0.05MM-SM XW3600 2 OMIT NO_XNET_CONNECTION

RADAR #: 50214461

Note: only 1 32K option may be stuffed at once

XTAL LAYOUT NOTES

1. Flood plane of VSS_PMU_XTAL on the layer beneath the XTAL (Y3600)
2. Drop via for VSS42 (U3300.U3) directly to the VSS_PMU_XTAL plane
3. Drop 2nd via under U3300.U3 from VSS_PMU_XTAL to XW3600
4. Tie XW3600 directly from via to GND plane

C3640 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

MEMS vs XTAL Select

30 26 PP1V5_VLDOINT

XTAL Select:

1V5 = MEMS (Active)
GND = XTAL (Passive)

R3650 0.00 0% 1/32W MF 01005 ROOM=SOC PACK_IGNORE=TRUE PACK_OPTION=D53,DEV BOMOPTION=32K:MEMS1&32K:MEMS2

R3651 0.00 0% 1/32W MF 01005 ROOM=SOC PACK_IGNORE=TRUE PACK_OPTION=D53,DEV BOMOPTION=32K:XTAL&32K:XTAL_NEWFLOW

PACK_OPTION=D52,D54

MAKE_BASE=TRUE

32K Sub-BOMs & XTAL new KDS flow

Population of sub-BOMs (685) is done in d55/top bomtool

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
685-00409	1	SUBBOM,32K,XTAL,Y3600,D53	SUBBOM_32K	CRITICAL	32K:ALL
197S00013	1	XTAL,32.768KHZ,20PPM,12.5PF,1610	Y3600	CRITICAL	32K:XTAL
197S00291	1	XTAL,32.768KHZ,20PPM,12.5PF,1610	Y3600	CRITICAL	32K:XTAL_NEWFLOW
131S00378	2	CAP,C0G,22PF,2%,16V,01005	C3651, C3652	CRITICAL	32K:XTAL&32K:XTAL_NEWFLOW
117S0161	1	RES,MF,0 OHM,1/32W,01005	C3651	CRITICAL	32K:MEMS1&32K:MEMS2
131S00342	1	CAP,CER,NP0/C0G,1PF,+/-0.1PF,16V,01005	C3652	CRITICAL	32K:MEMS1&32K:MEMS2

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00410	685-00409	32K:ALL	ALL	SUBBOM_32K,MEMS1,Y3601,D53
685-00411	685-00409	32K:ALL	ALL	SUBBOM_32K,MEMS2,Y3602,D53
132S00185	132S0316	32K:MEMS1&32K:MEMS2	ALL	CAP,C0G,NP0,0.1UF,10%,6.3V,01005

R3620 3.92K 0.1% 1/32W TF 01005 ROOM=PMU — TCAL RESISTOR MUST BE 0.1%

C3610 2.2UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

C3699 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU — ANALOG_PMU_VSS_VREF_ADC

MAKE_BASE=TRUE

ROOM=PMU OMIT XW3646 SHORT-20L-0.05MM-SM

ROOM=PMU OMIT XW3647 SHORT-20L-0.05MM-SM

SYNCING: D52, D53, D54, DEV

PAGE TITLE: SYS PWR: PMU: GPIO (4/5)

DRAWING NUMBER 051-05170 SIZE D

REVISION 10.0.0

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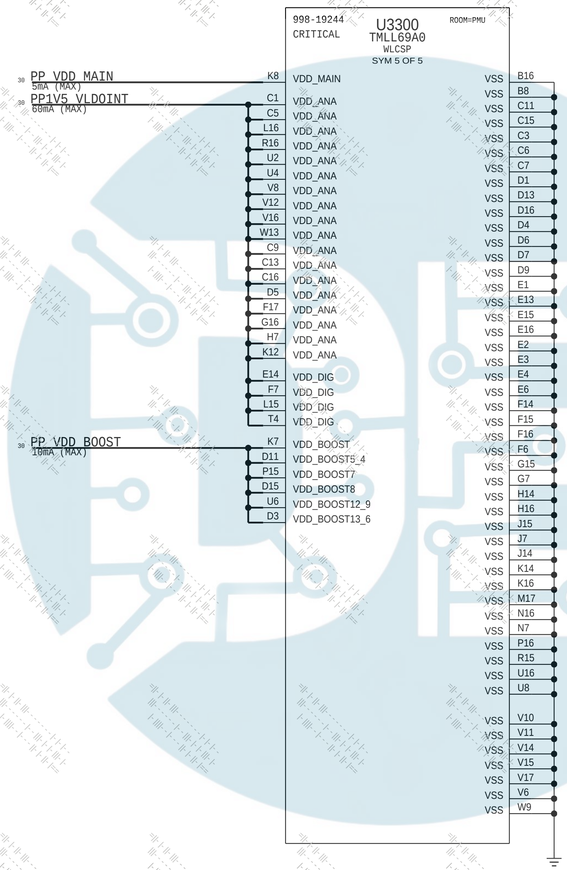

SYNCING: D52, D53, D54, DEV

PAGE TITLE
SYS PWR: PMU: Misc (5/5)

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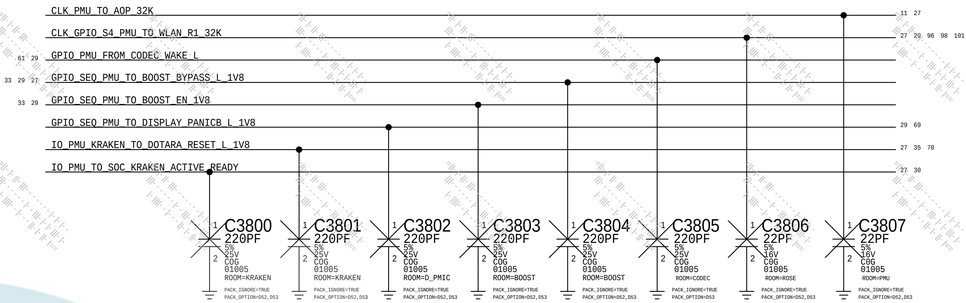
PMU GPIOs

PMU_GPIO1	27	NC_DEV_PMU_GPIO_1	NC DEV PMU GPIO 1			30
PMU_GPIO2	27	GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L	GPIO S4 PMU TO SPKRAMP BOT RESET L MAKE_BASE=TRUE	OUT		62 96
PMU_GPIO3	27	SWD_NUB_BI_PMU_SWDIO	SWD NUB BI PMU SWDIO MAKE_BASE=TRUE	OUT		30
PMU_GPIO4	27	GPIO_S4_PMU_TO_R1_RESET_L	GPIO S4 PMU TO R1 RESET L MAKE_BASE=TRUE	OUT		101
PMU_GPIO5	27	GPIO_S4_PMU_TO_WLAN_REG_ON	GPIO S4 PMU TO WLAN REG ON MAKE_BASE=TRUE	OUT		98
PMU_GPIO6	27	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	CLK GPIO S4 PMU TO WLAN R1 32K CXPLUS_WAIVE=SINGLE_COMP_NET MAKE_BASE=TRUE	OUT		27 29 96 98 101
PMU_GPIO7	27	NC_DEV_PMU_GPIO_7	NC DEV PMU GPIO 7			30
PMU_GPIO8	27	GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO PMU FROM WLAN HOST WAKE MAKE_BASE=TRUE	IN		98
PMU_GPIO9	27	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	GPIO PMU FROM BB PCIE HOST WAKE L MAKE_BASE=TRUE	IN		99
PMU_GPIO10	27	GPIO_PMU_TO_CCG2B_RESET_L	GPIO PMU TO CCG2B RESET L MAKE_BASE=TRUE	OUT		71 96
PMU_GPIO11	27	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	GPIO PMU FROM CHARGER VBUS DET INT L 1V8 MAKE_BASE=TRUE	IN		27 30 31 96
PMU_GPIO12	27	GPIO_PMU_FROM_CODEC_WAKE_L	GPIO PMU FROM CODEC WAKE L MAKE_BASE=TRUE	IN		29 61
PMU_GPIO13	27	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	GPIO PMU TO AMUX PMU SUPER TP CXPLUS_WAIVE=SINGLE_COMP_NET MAKE_BASE=TRUE	OUT		27
PMU_GPIO14	27	GPIO_PMU_NFC_TO_ARCAMP_RESET_L	GPIO PMU NFC TO ARCAMP RESET L MAKE_BASE=TRUE	OUT		65
PMU_GPIO15	27	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	GPIO PMU TO NAND LOW BATT BOOT L MAKE_BASE=TRUE	OUT		22 96
PMU_GPIO16	27	GPIO_PMU_NFC_TO_ARCAMP_TRIG	GPIO PMU NFC TO ARCAMP TRIG MAKE_BASE=TRUE	OUT		65
PMU_GPIO17	27	I2C2_AOP_SCL	I2C2 AOP SCL MAKE_BASE=TRUE	IN		11 18
PMU_GPIO18	27	CLK_GPIO_SEQ_PMU_TO_DISPLAY_32K_1V8	CLK GPIO SEQ PMU TO DISPLAY 32K 1V8 MAKE_BASE=TRUE	OUT		87 90
PMU_GPIO19	27	GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8	GPIO SEQ PMU TO DISPLAY RESET L 1V8 MAKE_BASE=TRUE	OUT		69 87 90
PMU_GPIO20	27	GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8	GPIO SEQ PMU TO DOTARA EN EXT 1V8 MAKE_BASE=TRUE	OUT		35 96
PMU_GPIO21	27	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	GPIO SEQ PMU TO BBPMU RESET L MAKE_BASE=TRUE	OUT		99
PMU_GPIO22	27	GPIO_SEQ_PMU_TO_NFC_EN	GPIO SEQ PMU TO NFC EN MAKE_BASE=TRUE	OUT		100
PMU_GPIO23	27	GPIO_SEQ_PMU_TO_BOOST_EN_1V8	GPIO SEQ PMU TO BOOST EN 1V8 MAKE_BASE=TRUE	OUT		29 33
PMU_GPIO24	27	GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8	GPIO SEQ PMU TO DISPLAY PANICB L 1V8 MAKE_BASE=TRUE	OUT		29 69
PMU_GPIO25	27	GPIO_SEQ_PMU_TO_BOOST_BYPASS_L_1V8	GPIO SEQ PMU TO BOOST BYPASS L 1V8 MAKE_BASE=TRUE	OUT		27 29 33

PMU DOCUMENTS RADAR #: 62945546

Buck Noise Mitigation



SYNCING: D52, D53, D54, DEV

PAGE TITLE
SYS PWR: PMU: Aliases: GPIO

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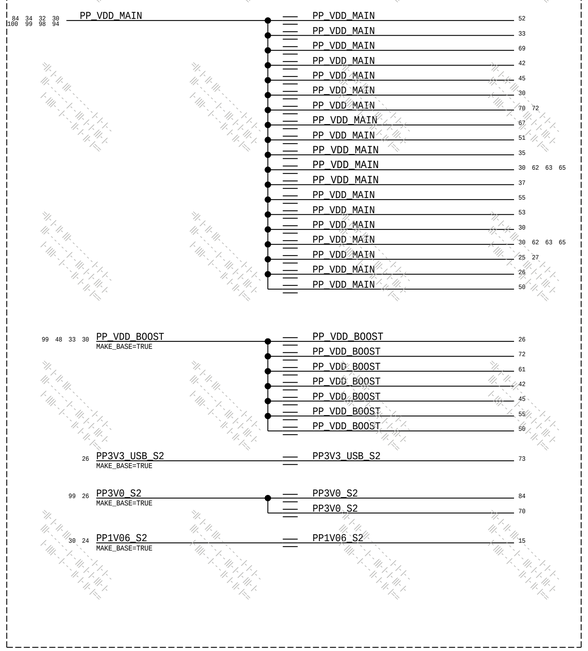
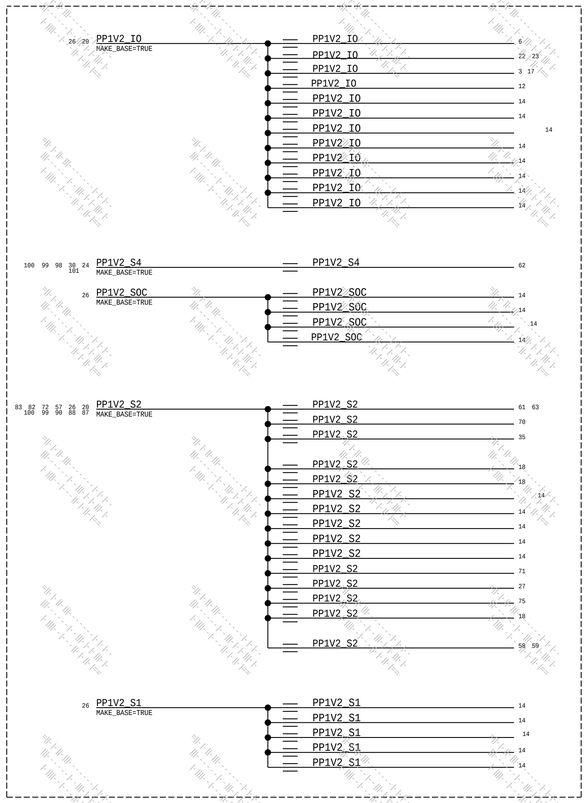
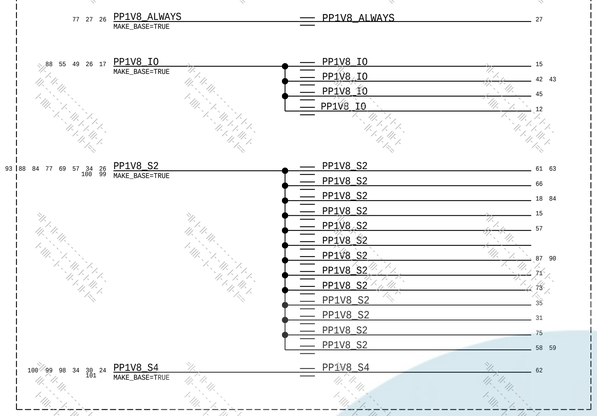
PP Misc Domains



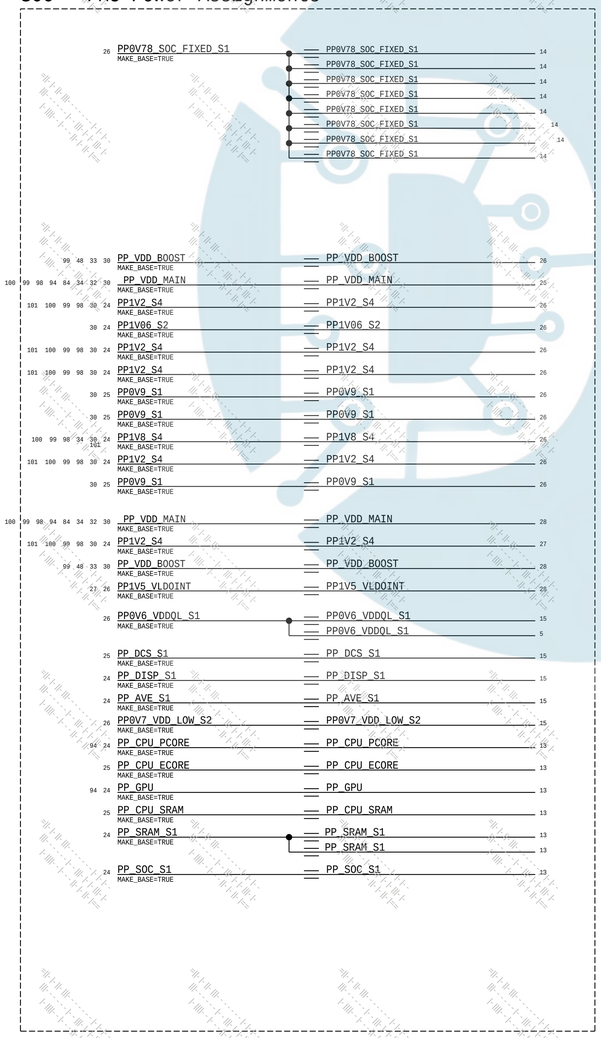
PP1V2 Domains



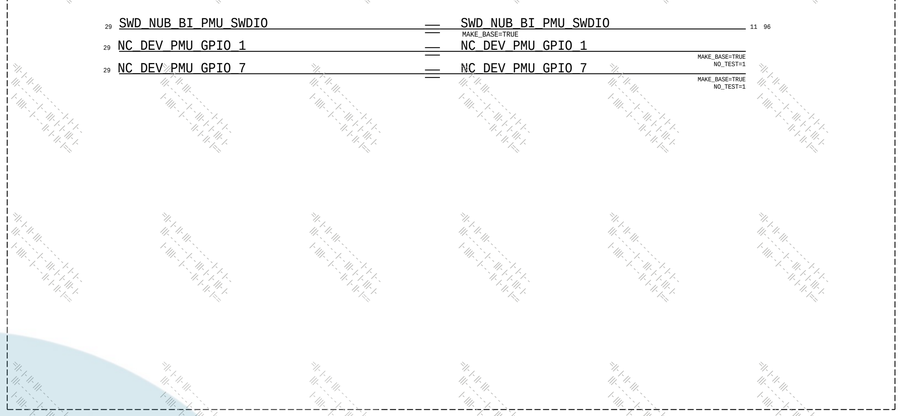
PP1V8 Domains



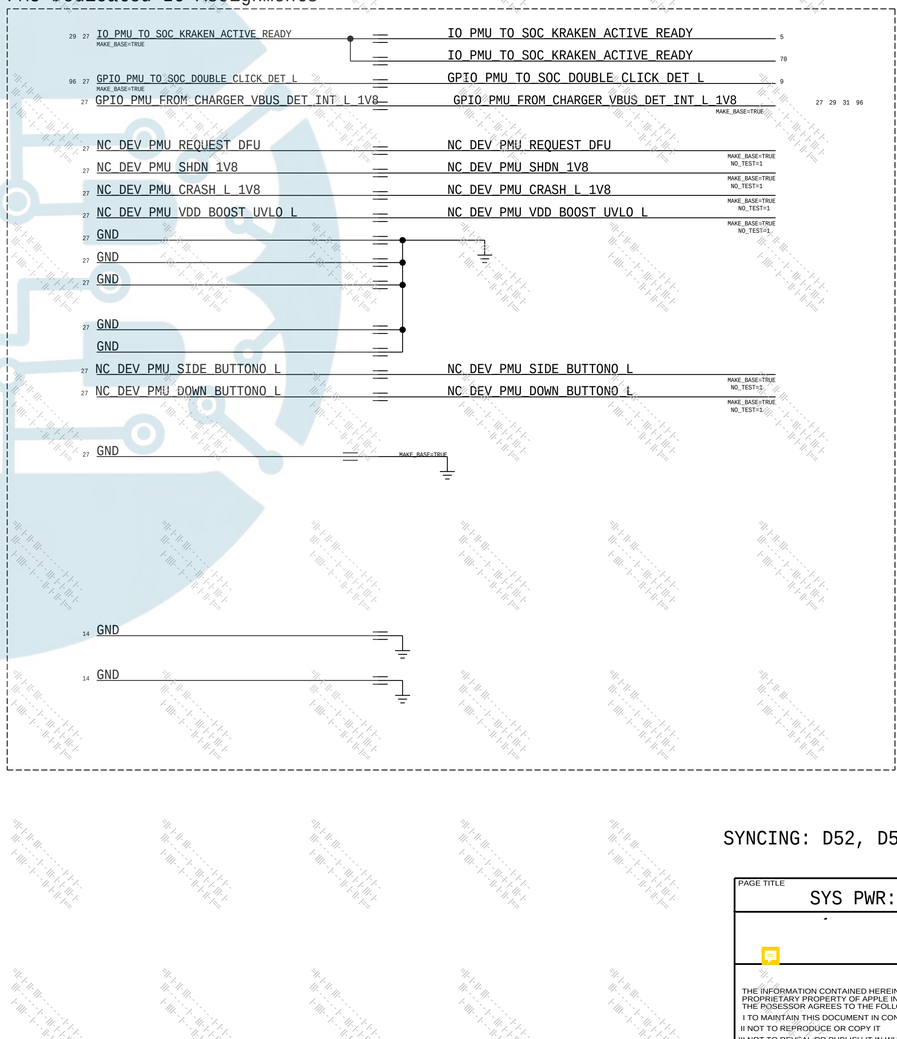
SOC + PMU Power Assignments



DEV Board Compatability



PMU Dedicated IO Assignments



SYNCING: D52, D53, D54

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YANGTZE CHARGER
(Veridian Charger Control)

SUBSYSTEM SPECIFIC BOM TABLES

Inductors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
152S01341	152S01241	BOARD_ID:D54	L4000,L4001	IND,1.0UH,20%,5.6A,28MO,H=0.90,3030	[D54 ALT]
152S01292	152S01229	BOARD_ID:D52,D53	L4000,L4001	IND,1.0UH,20%,5.2A,34MO,H=0.69,3225	[D52/D53 ALT]

Low Noise Cap

All RefDes in ( ) do not include Murata ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00185	138S00246	BOARD_ID:D54	(C4005)	CAP,X5R,2.2UF,20%,25V,0402

76 IN ANALOG_CHARGER_BAT_VDD_MAIN_SENSE

94 86 PP_VBUS1_E75
VOLTAGE=20.0

96 35 PP_VBUS2_DOTARA
VOLTAGE=20.0

C4001 1UF 20% 25V X5R 402 — 138S0683 — ROOM=CHARGER
C4041 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4003 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4004 220PF 5% 25V C0G 01005 — NOSTUFF — ROOM=CHARGER

C4005 2.2UF 20% 25V X5R 0402_0P1MM — OMIT_TABLE — ROOM=CHARGER
C4006 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4007 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4008 220PF 5% 25V C0G 01005 — NOSTUFF — ROOM=CHARGER

PP_CHARGER_PMID
C4010 4.7UF 20% 25V CER-X5R 0402 — CRITICAL 138S00187 — ROOM=CHARGER
C4011 4.7UF 20% 25V CER-X5R 0402 — CRITICAL 138S00187 — ROOM=CHARGER
C4012 4.7UF 20% 25V CER-X5R 0402 — CRITICAL 138S00187 — VOLTAGE=20.0 — ROOM=CHARGER

C4022 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4023 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4024 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4025 220PF 5% 25V C0G 01005 — ROOM=CHARGER

96 71 70 OUT PP_VAR_USB_RVP
18 BI I2C2_SMC_SDA_1V8
18 IN I2C2_SMC_SCL_1V8
RADAR #: 51315970
30 PP1V8_S2
VBUS1_VALID: Internal PU
70 96 IN IO_KRAKEN_TO_CHARGER_VBUS1_VALID_L_1V8
96 30 29 27 OUT GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8

U4000
SN2611A0-2C
DSBGA
ROOM=CHARGER
353S02307
CRITICAL

A1 BAT, B1 BAT, C1 BAT, D1 BAT, E1 BAT, F1 BAT, G1 BAT_SNS, A2 VDD_MAIN, B2 VDD_MAIN, C2 VDD_MAIN, D2 VDD_MAIN, E2 VDD_MAIN, F2 VDD_MAIN

A5 VBUS1, B5 VBUS1, C5 VBUS1, D5 VBUS1, E5 VBUS1
G5 VBUS2, H5 VBUS2, J5 VBUS2
A6 PMID, B6 PMID, C6 PMID, D6 PMID, E6 PMID, F5 PMID, F6 PMID, G6 PMID, H6 PMID, J6 PMID
A3 AUX1
H3 SDA
G3 SCL
G4 SYS_ALIVE*
C3 VBUS1_VALID*
B3 VBUS2_VALID*
F3 INT*
J3 VBUS1_DET — NC
A8 GND, B8 GND, C8 GND, D8 GND, E8 GND, F8 GND, G8 GND, H8 GND, J8 GND

BOOT1 A4, BOOT2 J4
SW1 A7, B7, C7, D7
SW2 F7, G7, H7, J7
TEST1 H1, TEST2 J1, TEST3 J2
ACT_DIODE* E3 — NC
LDO_IN E7, H4, B4
LDO_OUT F4
NC D4, C4, E4, G2
NTC H2 — NC

NO_XNET_CONNECTION
C4040 0.1UF 20% 10V X5R 01005-1 — LX_CHARGER_BOOT1 — ROOM=CHARGER
NO_XNET_CONNECTION
C4044 0.1UF 20% 10V X5R 01005-1 — LX_CHARGER_BOOT2 — ROOM=CHARGER

LX_CHARGER_P1
LX_CHARGER_P2

PACK_OPTION=D54_DEV
CRITICAL L4001 1.0UH-20%-5.6A-0.028OHM — PIPB030S-SM 152S01241 — ROOM=CHARGER
PACK_OPTION=D54_DEV

PACK_IGNORE=TRUE
PACK_OPTION=D52,D53
CRITICAL L4001 1.0UH-20%-5.2A-0.034OHM — PIJF22250H-SM 152S01229 — ROOM=CHARGER

CRITICAL L4000 1.0UH-20%-5.2A-0.034OHM — PIJF22250H-SM 152S01229 — ROOM=CHARGER

PACK_IGNORE=TRUE
PACK_OPTION=D52,D53
CRITICAL L4000 1.0UH-20%-5.6A-0.028OHM — PIPB030S-SM 152S01241 — ROOM=CHARGER
PACK_OPTION=D54_DEV

PP_BATT_VCC_YANGTZE

C4045 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4042 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4043 330PF 10% 16V CER-X7R 01005 — ROOM=CHARGER

CRITICAL C4090 15UF 20% 6.3V X5R 0402-0.1MM-1 — ROOM=CHARGER
CRITICAL C4091 15UF 20% 6.3V X5R 0402-0.1MM-1 — ROOM=CHARGER
CRITICAL C4092 15UF 20% 6.3V X5R 0402-0.1MM-1 — ROOM=CHARGER

PP5V0_CHARGER_LDO_INTERNAL
VOLTAGE=5.0
C4060 220PF 5% 25V C0G 01005 — ROOM=CHARGER
C4061 2.2UF 20% 10V X5R 0201 — ROOM=CHARGER
C4062 2.2UF 20% 10V X5R 0201 — ROOM=CHARGER

SYNCING: D52, D53, D54

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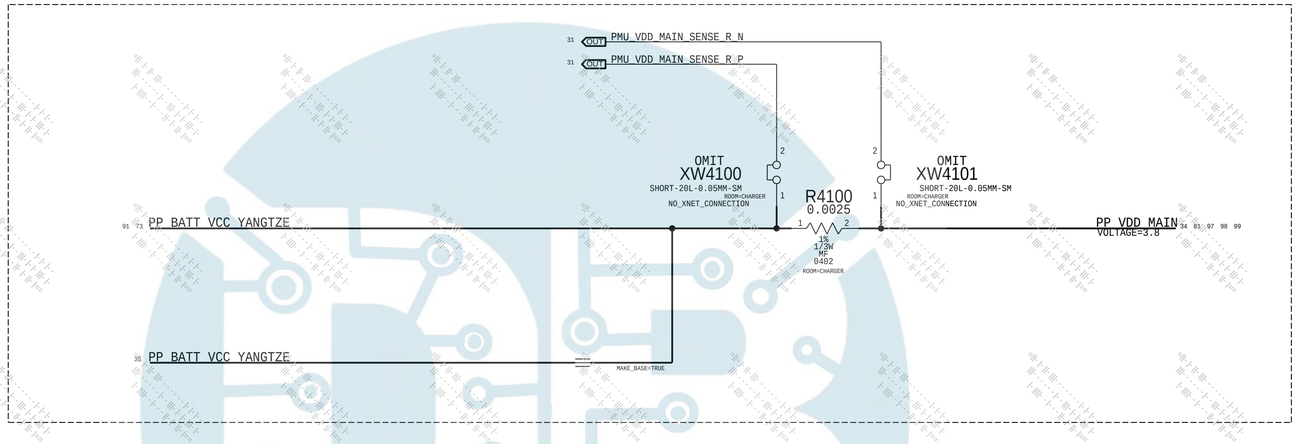
CHARGER SENSE RESISTOR



SYNCING: D52, D53

PAGE TITLE
SYS PWR: Charger/Boost: Aliases

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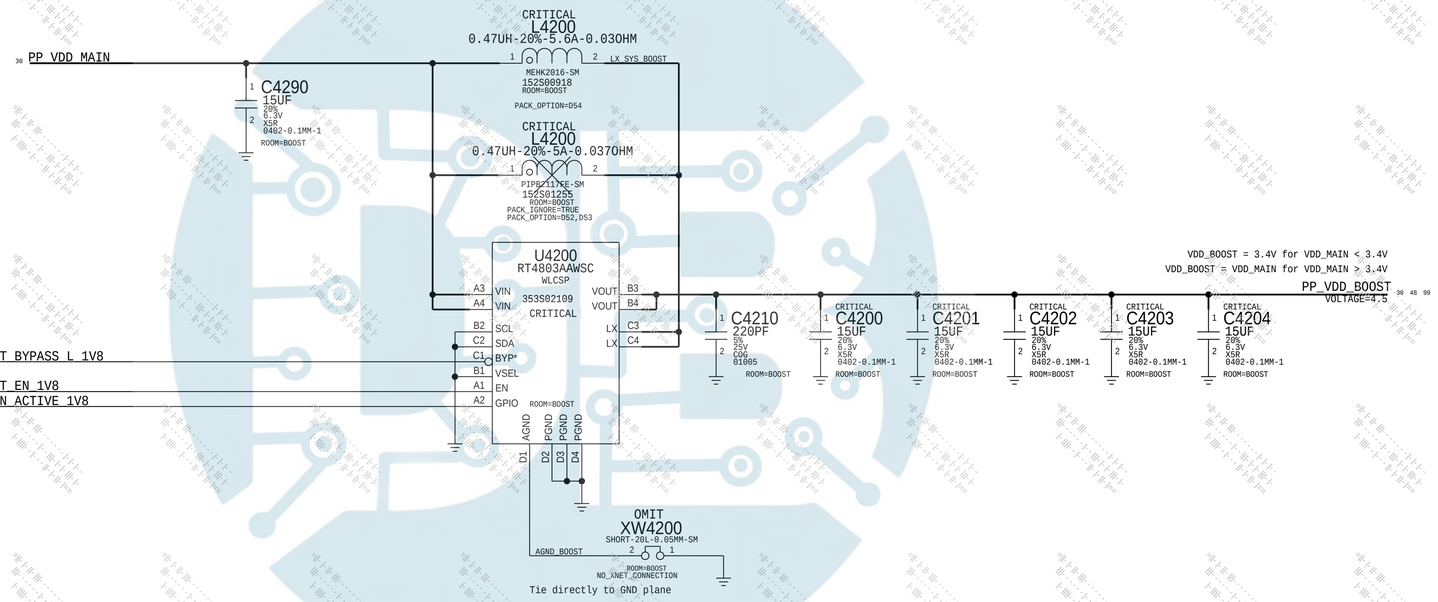
BOOST

SUBSYSTEM SPECIFIC BOM TABLES

Boost

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01124	353S02109	?	U4200	IC,SN61280E,BOOST,3.6V,4.5A,CSP16



SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: Boost
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Dotara

SUBSYSTEM SPECIFIC BOM TABLES

Dotara FET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00362	376S00295	?	Q4400	NFET,120V,OnSemi

Dotara OTP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00678	1	DotaraLV, MTP V2.0.9	U4400	CRITICAL	?

SUBSYSTEM SPECIFIC BOM TABLES

Low Noise Cap

OMIT_Table changes primary to SEMCO because Murata has desired footprint, but some locations require single-source on SEMCO

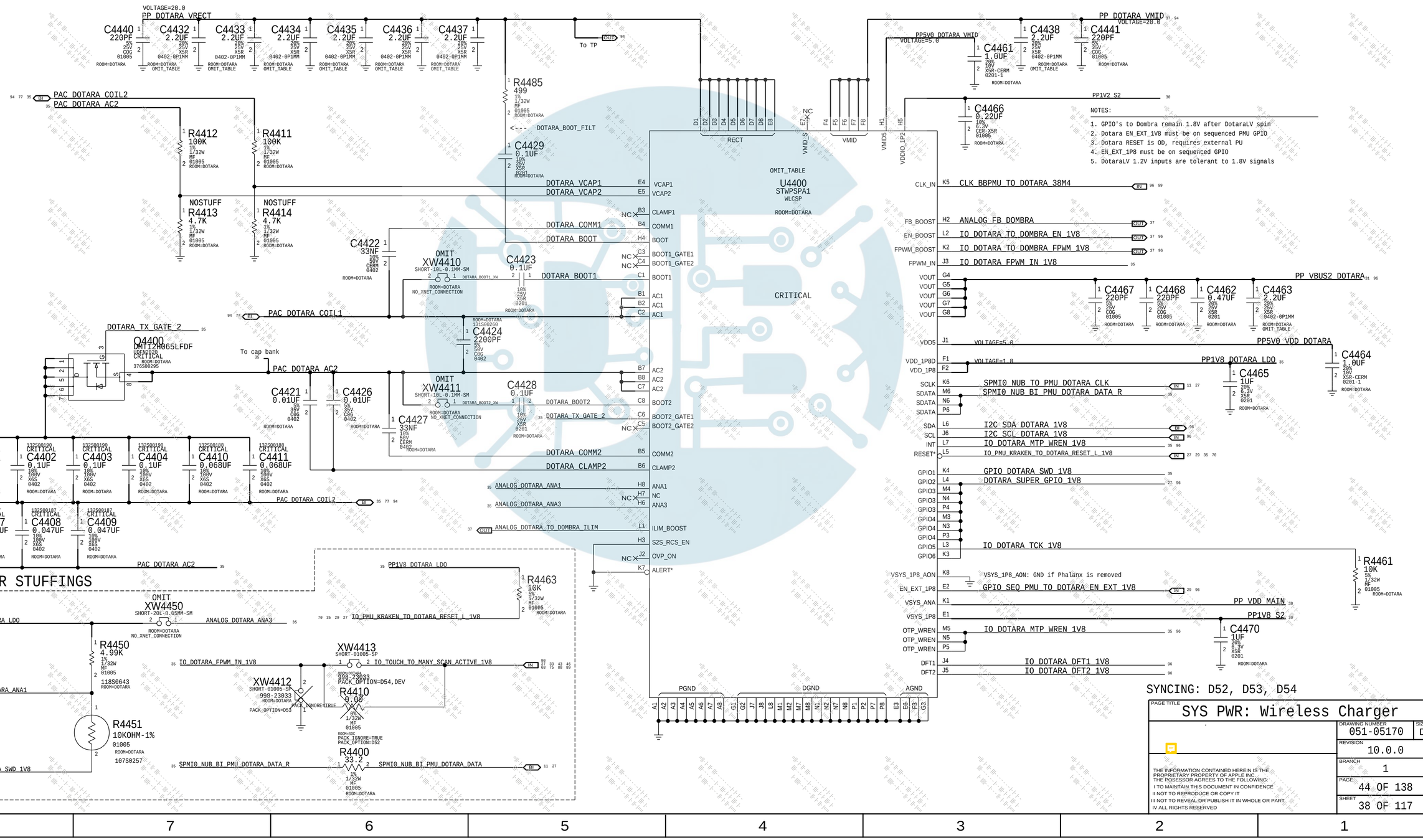
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S00246	10	CAP,X5R,2.2UF,20%,25V,0402	C4400,C4402,C4410,C4403,C4404,C4436,C4437,C4438,C4461,C4441	CRITICAL	?

All RefDes in ( ) do not include Murata ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00185	138S00246	BOARD_ID:0X36&BOARD_ID:0X3F	[SEE BELOW]	CAP,X5R,2.2UF,20%,25V,0402
138S00185	138S00246	BOARD_ID:0X4	[SEE BELOW]	CAP,X5R,2.2UF,20%,25V,0402

DS3 Single-Source: (C4433,C4434,C4435,C4436,C4438,C4463)

DS4 Single-Source: (C4433,C4434,C4436)



PAGE TITLE

SYS PWR: Wireless Charger

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DOTARA ALIASES

SYNCING: D52, D53, D54, DEV

PAGE TITLE
SYS PWR: Wireless Charger: Level Shifters

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SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

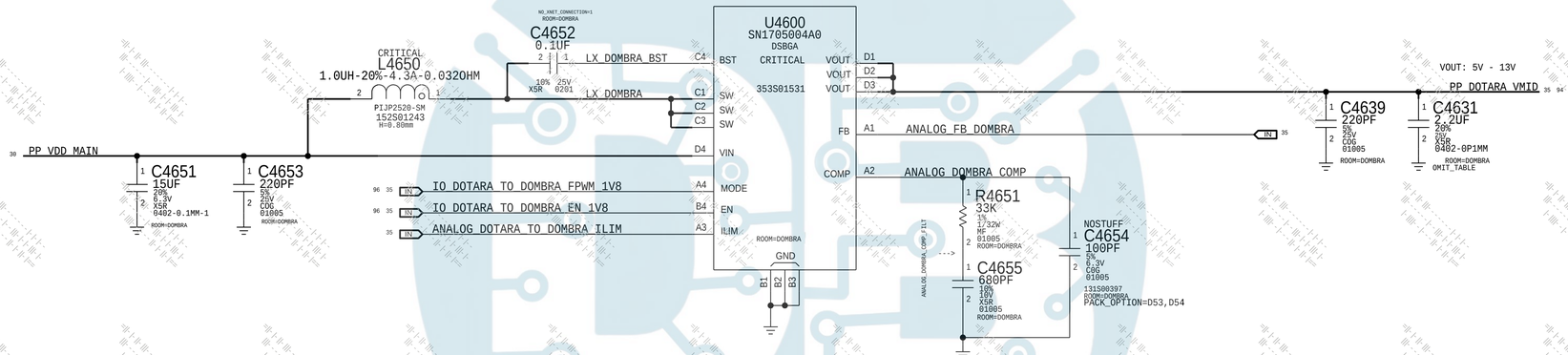
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

Low Noise Cap

All RefDes in ( ):do not include Murata ALT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00185	138S00246	BOARD_ID:D54	(C4631)	CAP,X5R,2.2UF,20%,25V,0402

Dombra



SYNCING: D52, D53, D54

PAGE TITLE	SYS PWR: Wireless Charger: Boost
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SYNCING: D52, D53, D54

PAGE TITLE
SYS PWR: Wireless Charger: Aliases

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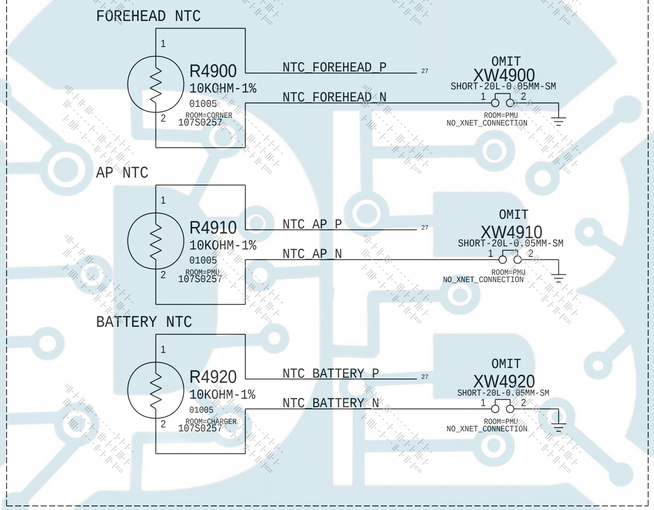
Top NTCs

Place NTC XWs near PMU, route P/N differentially



PAGE TITLE: SYS PWR: NTCs (Top)

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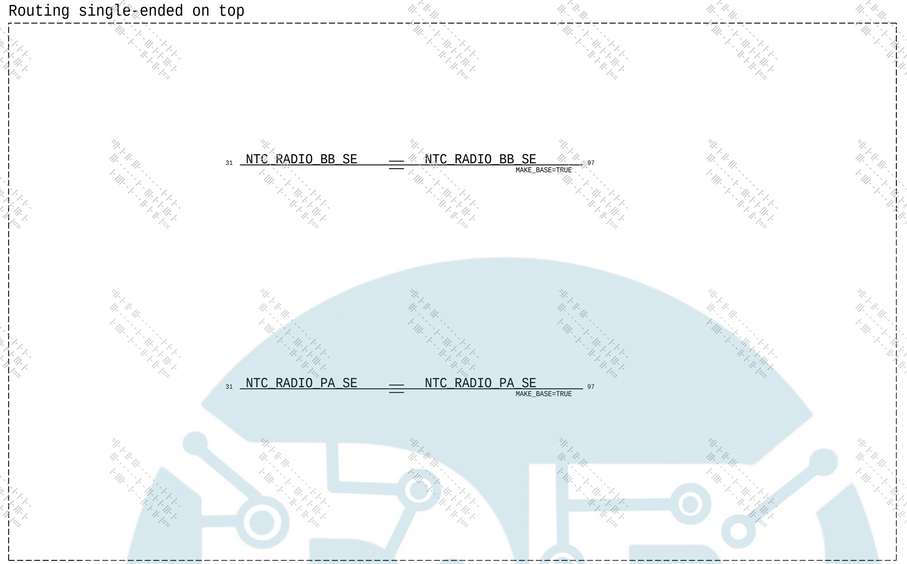
Bottom NTCs

Routing single-ended on top



SYNC_DATE=09/03/2019

PAGE TITLE

SYS PWR: NTCs (Bottom)

-

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SUBSYSTEM SPECIFIC BOM TABLES

4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C5310,C5330,C5340,C5350,C5360,C5370,C5380,C5390)

(C5310,C5330,C5340,C5350,C5360,C5370,C5380,C5390)

CAMERA PMU1

30 PP_VDD_MAIN

C5304 220PF 5% 25V COG 01005 ROOM=CAM_PMU1

C5305 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU1

338S00564 U5300 D2657B0N0VNAV WLCSP SYM 1 OF 4 CRITICAL ROOM=CAM_PMU1

A3 VDD_BUCK0_0
B3 VDD_BUCK0_1
B6 VDD_MAIN_1
F5 VDD_MAIN_2

VCC MAIN | BUCKS

BUCK0_LX0_0
BUCK0_LX0_1
BUCK0_FB

A2 LX_CAM_PMU1_BUCK
B2
D1 ANALOG_FB_CAM_PMU1_BUCK

L5300 0.47UH-2.9A-0.072OHM PIID1608FE-SM 152500982 ROOM=CAM_PMU1

OMIT XW5300 SHORT-20L-0.05MM-SM ROOM=CAM_PMU1 NO_XNET_CONNECTION=1

C5300 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=CAM_PMU1 CRITICAL

C5301 20UF 20% 6.3V CERM-X5R 0402-0.1MM ROOM=CAM_PMU1 CRITICAL

C5302 330PF 10% 16V CER-X7R 01005 ROOM=CAM_PMU1

C5303 220PF 5% 25V COG 01005 ROOM=CAM_PMU1

PP1V3_CAM_PMU1_BUCK0 44

Adams LDO Design Guidelines

LDO1-7: Need 1uF effective Cout
LDO8-9: Need 2uF effective Cout

42 30 PP_VDD_BOOST

C5395 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU1

338S00564 U5300 D2657B0N0VNAV WLCSP SYM 2 OF 4 CRITICAL ROOM=CAM_PMU1

H8 VDD_LDO1_2
F8 VDD_LDO3_4
D8 VDD_LDO5_6_7
B8 VDD_LDO8_9

LDO INPUT | LDO OUTPUT

VLDO1 H7 PP2V85_IRCAM_AVDD 44
VLDO2 G7 PP3V3_MAMABEAR_VDD 44
VLDO3 G8 PP1V8_WIDE_VDDIO 44
VLDO4 F7 PP2V85_FCAM_AVDD 44
VLDO5 E8 PPVAR_SWIDE_AVDD2 44
VLDO6 E7 PP3V0_PENROSE_SVDD 44
VLDO7 D7 PPVAR_WIDE_AVDD2 44
VLDO8 C8 PP1V1_FCAM_DVDD 44
VLDO9 C7 PP1V2_IRCAM_DVDD 44
VLDO10 E5 PP1V2_INT_CAM_PMU1 VOLTAGE=1.2

C5310 4UF 20% 6.3V CER-X5R 0201 ROOM=CAM_PMU1

C5320 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=CAM_PMU1

C5330 4UF 20% 6.3V CER-X5R 0201 ROOM=CAM_PMU1

C5340 4UF 20% 6.3V CER-X5R 0201 ROOM=CAM_PMU1

C5350 4UF 20% 6.3V CER-X5R 0201 ROOM=CAM_PMU1

C5360 4UF 20% 6.3V CER-X5R 0201 ROOM=CAM_PMU1

C5370 4UF 20% 6.3V CER-X5R 0201 ROOM=CAM_PMU1

C5380 4UF 20% 6.3V CER-X5R 0201 ROOM=CAM_PMU1

C5390 4UF 20% 6.3V CER-X5R 0201 ROOM=CAM_PMU1

C5311 0.22UF 10% 6.3V CER-X5R 01005 ROOM=CAM_PMU1

44 PP1V3_CAM_PMU1_BUCK0

C5393 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU1

42 30 PP_VDD_BOOST
43 30 PP1V8_IO

PLACE NEAR PIN G3

C5397 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=CAM_PMU1

SW INPUT | SW OUTPUT

A7 VDD_HI
A5 VPP_1V8_1
G3 VPP_1V8_2

PP_1V8_SW
VDD_MAX
VDD_RTC
VDD_RTC_DIG

A4 PP1V8_CAM_PMU1_IO_SW 44 81 82 VOLTAGE=1.8

A6 PP_VDD_MAX_CAM_PMU1 VOLTAGE=4.5
E4 PP_VDD_RTC_CAM_PMU1 VOLTAGE=1.5
F4

VDD_MAX: INTERNAL SUPPLY
POWER-OR OF VDD_HI OR VDD_MAIN

C5391 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=CAM_PMU1

C5392 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=CAM_PMU1

SYNCING: D52, D53, D54

PAGE TITLE: CAMERA: PMU 1: Power (1/2)

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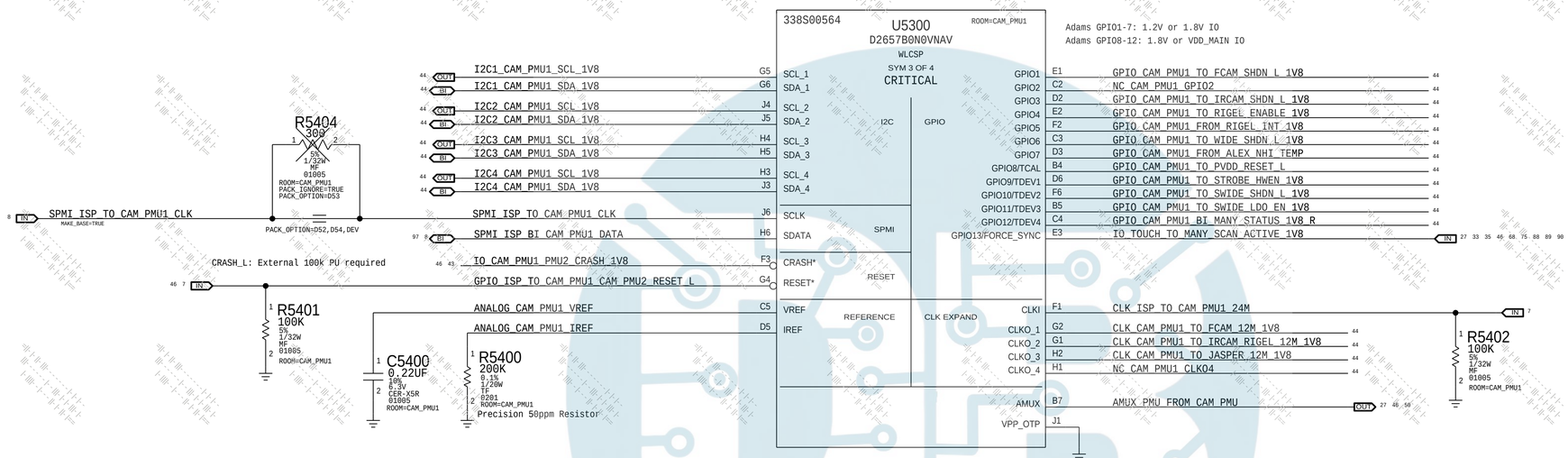
CAMERA PMU1



SYNCING: D52, D53, D54

PAGE TITLE	CAMERA: PMU 1: I/O (2/2)
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ADAMS #1 ALIASES

CAM_PMU1 I2C1: FCAM

79 78 46 44 PP1V8_CAM_PMU1_IO_SW

R5510 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

R5511 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

45 I2C1_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C1_CAM_PMU1_SCL_1V8 OUT 78

45 I2C1_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C1_CAM_PMU1_SDA_1V8 BI 78

MASTER	CAM PMU1	NUMBER	I2C1	DIAGS NUMBER	4	SPEED	1MHz
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION	
FCAM	1.8V		0x10	0x20,0x21	1MHz	FCAM MD Flex	

CAM_PMU1 I2C2: IRCAM/ROMEO/RIGEL

79 78 46 44 PP1V8_CAM_PMU1_IO_SW

R5520 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

R5521 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

45 I2C2_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C2_CAM_PMU1_SCL_1V8 OUT 79

45 I2C2_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C2_CAM_PMU1_SDA_1V8 BI 79

I2C2_CAM_PMU1_SCL_1V8 OUT 80

I2C2_CAM_PMU1_SDA_1V8 BI 80

I2C2_CAM_PMU1_SCL_1V8 OUT 54

I2C2_CAM_PMU1_SDA_1V8 BI 54

MASTER	CAM PMU1	NUMBER	I2C2	DIAGS NUMBER	5	SPEED	1MHz
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION	
IRCAM	1.8V		0x18	0x30,0x31	1MHz	Juliet Flex	
Romeo	1.8V		0x66	0xCC,0xCD	1MHz	Romeo Flex	
Rigel	1.8V		0x55	0xAA,0xAB	1MHz	Top	

CAM_PMU1 I2C3: WIDE

75 46 PP1V8_WIDE_VDDIO

R5530 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

R5531 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

45 I2C3_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C3_CAM_PMU1_SCL_1V8 OUT 75

45 I2C3_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C3_CAM_PMU1_SDA_1V8 BI 75

MASTER	CAM PMU1	NUMBER	I2C3	DIAGS NUMBER	6	SPEED	1MHz
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION	
Wide	1.8V		0x10	0x20,0x21	1MHz	RCAM WI Flex	
Lorentz	1.8V		0x74	0xE8,0xE9	1MHz	RCAM WI Flex	

CAM_PMU1 I2C4: SWIDE/ALEX/STROBE

76 51 49 PP1V8_TELE_SWIDE_VDDIO

R5540 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

R5541 1.00K 5% 1/32W MF 01005 ROOM=CAM_PMU1

45 I2C4_CAM_PMU1_SCL_1V8 — MAKE_BASE=TRUE — I2C4_CAM_PMU1_SCL_1V8 OUT 76

45 I2C4_CAM_PMU1_SDA_1V8 — MAKE_BASE=TRUE — I2C4_CAM_PMU1_SDA_1V8 BI 76

I2C4_CAM_PMU1_SCL_1V8 OUT 51

I2C4_CAM_PMU1_SDA_1V8 BI 51

I2C4_CAM_PMU1_SCL_1V8 OUT 53

I2C4_CAM_PMU1_SDA_1V8 BI 53

MASTER	CAM PMU1	NUMBER	I2C4	DIAGS NUMBER	7	SPEED	1MHz
DEVICE	VOLTAGE		7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION	
Super Wide	1.8V		0x20	0x40,0x41	1MHz	RCAM Superflex	
Alex	1.8V		0x76	0xEC,0xED	1MHz	Top	
Strobe	1.8V		0x65	0xCA,0xCB	1MHz	Top	

SIGNAL

GPIO_1	45 GPIO_CAM_PMU1_TO_FCAM_SHDN_L_1V8	GPIO_CAM_PMU1_TO_FCAM_SHDN_L_1V8	MAKE_BASE=TRUE OUT 78
GPIO_2	45 NC_CAM_PMU1_GPIO2	NC_CAM_PMU1_GPIO2	NO_TEST=1 MAKE_BASE=TRUE
GPIO_3	45 GPIO_CAM_PMU1_TO_IRCAM_SHDN_L_1V8	GPIO_CAM_PMU1_TO_IRCAM_SHDN_L_1V8	MAKE_BASE=TRUE OUT 79
GPIO_4	45 GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	MAKE_BASE=TRUE OUT 54 92
GPIO_5	45 GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	MAKE_BASE=TRUE IN 31 54 92
GPIO_6	45 GPIO_CAM_PMU1_TO_WIDE_SHDN_L_1V8	GPIO_CAM_PMU1_TO_WIDE_SHDN_L_1V8	MAKE_BASE=TRUE OUT 75
GPIO_7	45 GPIO_CAM_PMU1_FROM_ALEX_NHI_TEMP	GPIO_CAM_PMU1_FROM_ALEX_NHI_TEMP	MAKE_BASE=TRUE IN 55
GPIO_8	45 GPIO_CAM_PMU1_TO_PVDD_RESET_L	GPIO_CAM_PMU1_TO_PVDD_RESET_L	MAKE_BASE=TRUE OUT 51
GPIO_9	45 GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	MAKE_BASE=TRUE OUT 53 92
GPIO_10	45 GPIO_CAM_PMU1_TO_SWIDE_SHDN_L_1V8	GPIO_CAM_PMU1_TO_SWIDE_SHDN_L_1V8	MAKE_BASE=TRUE OUT 76
GPIO_11	45 GPIO_CAM_PMU1_TO_SWIDE_LDO_EN_1V8	GPIO_CAM_PMU1_TO_SWIDE_LDO_EN_1V8	MAKE_BASE=TRUE OUT 50 92
GPIO_12	45 GPIO_CAM_PMU1_BI_MANY_STATUS_1V8_R	GPIO_CAM_PMU1_BI_MANY_STATUS_1V8_R	MAKE_BASE=TRUE
GPIO_13	Camera PMU1 GPIO13 intentionally not aliased		
CLKO_1	45 CLK_CAM_PMU1_TO_FCAM_12M_1V8	CLK_CAM_PMU1_TO_FCAM_12M_1V8	MAKE_BASE=TRUE OUT 78
CLKO_2	45 CLK_CAM_PMU1_TO_IRCAM_RIGEL_12M_1V8	CLK_CAM_PMU1_TO_IRCAM_RIGEL_12M_1V8	MAKE_BASE=TRUE OUT 54 79
CLKO_3	45 CLK_CAM_PMU1_TO_JASPER_12M_1V8	CLK_CAM_PMU1_TO_JASPER_12M_1V8	MAKE_BASE=TRUE OUT 77
CLKO_4	45 NC_CAM_PMU1_CLKO4	NC_CAM_PMU1_CLKO4	NO_TEST=1 MAKE_BASE=TRUE

D52/D53: PVDD Reset -> Lex
D54: PVDD Reset -> Alex

R5505 10K 5% 1/32W MF 01005 ROOM=CAM_PMU1 — IO_RIGEL_BI_GRIEVOUS_STATUS_1V8 BI 54 81

R5506 10K 5% 1/32W MF 01005 ROOM=CAM_PMU1 — IO_RIGEL_BI_MAMABEAR_STATUS_1V8 BI 54 80

POWER

VLDO1	44 PP2V85_IRCAM_AVDD	PP2V85_IRCAM_AVDD	VOLTAGE=2.9 MAKE_BASE=TRUE 79
VLDO2	44 PP3V3_MAMABEAR_VDD	PP3V3_MAMABEAR_VDD	VOLTAGE=3.3 MAKE_BASE=TRUE 80
VLDO3	44 PP1V8_WIDE_VDDIO	PP1V8_WIDE_VDDIO	VOLTAGE=1.8 MAKE_BASE=TRUE 46 75
VLDO4	44 PP2V85_FCAM_AVDD	PP2V85_FCAM_AVDD	VOLTAGE=2.9 MAKE_BASE=TRUE 78
VLDO5	44 PPVAR_SWIDE_AVDD2	PPVAR_SWIDE_AVDD2	VOLTAGE=3.0 MAKE_BASE=TRUE 76
VLDO6	44 PP3V0_PENROSE_SVDD	PP3V0_PENROSE_SVDD	VOLTAGE=3.0 MAKE_BASE=TRUE 50 82
VLDO7	44 PPVAR_WIDE_AVDD2	PPVAR_WIDE_AVDD2	VOLTAGE=3.0 MAKE_BASE=TRUE 75
VLDO8	44 PP1V1_FCAM_DVDD	PP1V1_FCAM_DVDD	VOLTAGE=1.1 MAKE_BASE=TRUE 78
VLDO9	44 PP1V2_IRCAM_DVDD	PP1V2_IRCAM_DVDD	VOLTAGE=1.2 MAKE_BASE=TRUE 79
VLDO10	Camera PMU1 LDO10 used as internal VREF		
BUCK0	44 PP1V3_CAM_PMU1_BUCK0	PP1V3_CAM_PMU1_BUCK0	VOLTAGE=1.3 MAKE_BASE=TRUE 50
(PMU1) VDD_LDO8_9	44 PP1V3_CAM_PMU1_BUCK0		
(PMU2) VDD_LDO8_9	47 PP1V3_CAM_PMU1_BUCK0		

SYNCING: D52, D53, D54

SYNC_MASTER=0.143.0 SYNC_DATE=05/14/2019

PAGE TITLE

CAMERA: PMU 1: Aliases

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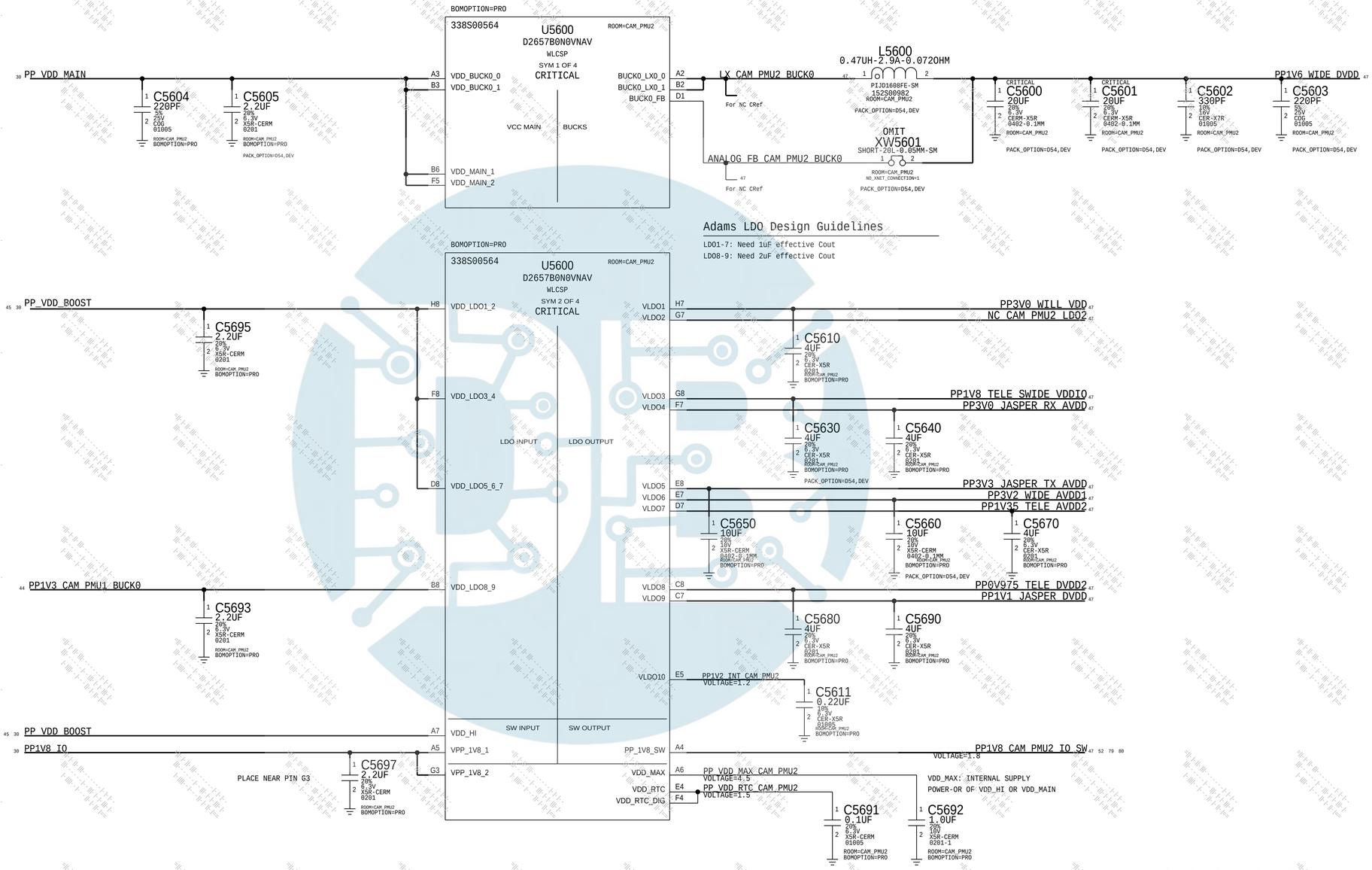
SUBSYSTEM SPECIFIC BOM TABLES

4uF 0201 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

(C5610,C5630,C5640,C5660,C5670,C5680,C5690)
(C5610,C5630,C5640,C5660,C5670,C5680,C5690)

CAMERA PMU2



SYNCING: D53, D54

PAGE TITLE
CAMERA: PMU 2: Power (1/2)

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CAMERA PMU2

BOMOPTION=PRO

338S00564 U5600 D2657B0N0VNAV WLCSP SYM 3 OF 4 CRITICAL ROOM=CAM_PMU2

I2C1_CAM_PMU2_SCL_1V8	G5	SCL_1		
I2C1_CAM_PMU2_SDA_1V8	G6	SDA_1		
I2C2_CAM_PMU2_SCL_1V8	J4	SCL_2	I2C	GPIO
I2C2_CAM_PMU2_SDA_1V8	J5	SDA_2		
NC_I2C3_CAM_PMU2_SCL_1V8 (NO_TEST=1)	H4	SCL_3		
NC_I2C3_CAM_PMU2_SDA_1V8 (NO_TEST=1)	H5	SDA_3		
NC_I2C4_CAM_PMU2_SCL_1V8 (NO_TEST=1)	H3	SCL_4		
NC_I2C4_CAM_PMU2_SDA_1V8 (NO_TEST=1)	J3	SDA_4		
SPMI_ISP_TO_CAM_PMU2_CLK	J6	SCLK	SPMI	
SPMI_ISP_BI_CAM_PMU2_DATA	H6	SDATA		
IO_CAM_PMU1_PMU2_CRASH_1V8	F3	CRASH*	RESET	
GPIO_ISP_TO_CAM_PMU1_CAM_PMU2_RESET_L	G4	RESET*		
ANALOG_CAM_PMU2_VREF	C5	VREF	REFERENCE	CLK EXPAND
ANALOG_CAM_PMU2_IREF	D5	IREF		
		CLKI		F1 CLK_ISP_TO_CAM_PMU2_24M
		CLKO_1		G2 CLK_CAM_PMU2_TO_TELE_24M_1V8
		CLKO_2		G1 CLK_CAM_PMU2_TO_WIDE_24M_1V8
		CLKO_3		H2 CLK_CAM_PMU2_TO_SWIDE_24M_1V8
		CLKO_4		H1 NC_CAM_PMU2_CLKO4
		AMUX		B7 AMUX_PMU_FROM_CAM_PMU
		VPP_OTP		J1

Adams GPIO1-7: 1.2V or 1.8V IO
Adams GPIO8-12: 1.8V or VDD_MAIN IO

GPIO1	E1	GPIO_CAM_PMU2_TO_TELE_SHDN_L_1V8
GPIO2	C2	GPIO_CAM_PMU2_TO_TELE_LDO_EN_1V8
GPIO3	D2	GPIO_CAM_PMU2_TO_JASPER_SHDN_L_1V8
GPIO4	E2	NC_CAM_PMU2_GPIO4
GPIO5	F2	GPIO_CAM_PMU2_FROM_WILL_JASPER_INT_L_1V8
GPIO6	C3	GPIO_CAM_PMU2_TO_WILL_EN_1V8
GPIO7	D3	NC_CAM_PMU2_GPIO7
GPIO8/TCAL	B4	NC_CAM_PMU2_GPIO8
GPIO9/TDEV1	D6	NC_CAM_PMU2_GPIO9
GPIO10/TDEV2	F6	NC_CAM_PMU2_GPIO10
GPIO11/TDEV3	B5	NC_CAM_PMU2_GPIO11
GPIO12/TDEV4	C4	NC_CAM_PMU2_GPIO12
GPIO13/FORCE_SYNC	E3	IO_TOUCH_TO_MANY_SCAN_ACTIVE_1V8

IN 27 33 35 43 68 75 88 89 90

R5704 300 5% 1/32W MF 01005 ROOM=CAM_PMU2 PACK_IGNORE=TRUE PACK_OPTION=D53

8 IN SPMI_ISP_TO_CAM_PMU2_CLK MAKE_BASE=TRUE

PACK_OPTION=D52,D54,DEV

97 8 BI SPMI_ISP_BI_CAM_PMU2_DATA

CRASH_L PU shared w/ Adams1

43 BI IO_CAM_PMU1_PMU2_CRASH_1V8

RESET PD shared w/ Adams1

43 7 IN GPIO_ISP_TO_CAM_PMU1_CAM_PMU2_RESET_L

C5700 0.22UF 10% 6.3V CER-X5R 01005 ROOM=CAM_PMU2 BOMOPTION=PRO

R5710 200K 0.1% 1/20W TF 0201 ROOM=CAM_PMU2 BOMOPTION=PRO Precision 50ppm Resistor

R5720 100K 5% 1/32W MF 01005 ROOM=CAM_PMU2 BOMOPTION=PRO

R5720: Place near F1

Advanced Test Mode (OTP rewrite)

BOMOPTION=PRO

338S00564 U5600 D2657B0N0VNAV WLCSP SYM 4 OF 4 CRITICAL ROOM=CAM_PMU2

A8	VSS	VSS_BUCK0	A1
C1	VSS	VSS_BUCK0	B1
C6	VSS		
D4	VSS		
E6	VSS		
J2	VSS		
J7	VSS		
J8	VSS		

SYNCING: D53, D54

PAGE TITLE: CAMERA: PMU 2: I/O (2/2)

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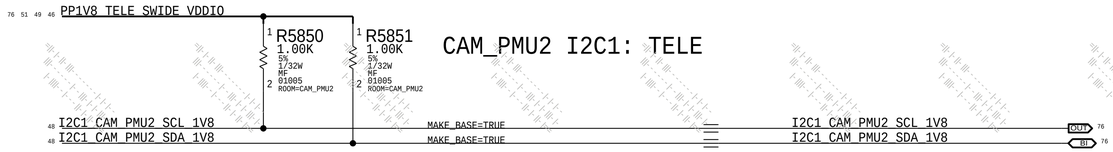
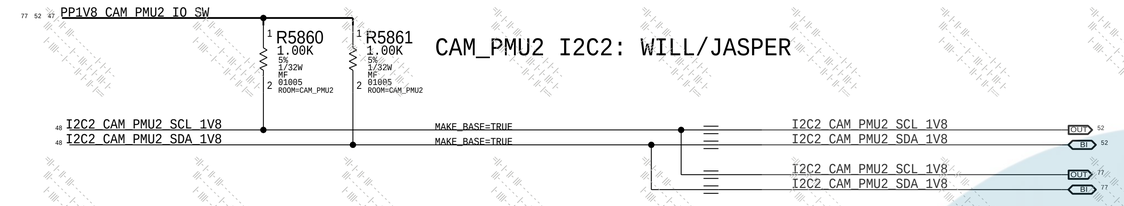
ADAMS #2 ALIASES





MASTER	CAM PMU2	NUMBER	I2C1	DIAGS NUMBER	8	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Tele	1.8V	0x10	0x20,0x21	1MHz	RCAM Superflex		
Lorentz	1.8V	0x74	0xE8,0xE9	1MHz	RCAM Superflex		

MASTER	CAM PMU2	NUMBER	I2C2	DIAGS NUMBER	9	SPEED	1MHz
DEVICE	VOLTAGE	7-BIT ADDR	8-BIT ADDR	MAX SPEED	LOCATION		
Will	1.8V	0x40	0x80,0x81	1MHz	Top		
Periscope	1.8V	0x10	0x20,0x21	1MHz	Jasper Flex		
Riker (Main Core)	1.8V	0x33	0x66,0x67	1MHz	Jasper Flex		
Riker (OVP Core)	1.8V	0x34	0x68,0x69	1MHz	Jasper Flex		
Jasper (EEPROM)	1.8V	0x51	0xA2,0xA3	1MHz	Jasper Flex		

SIGNAL

GPIO_1	48 GPIO_CAM_PMU2_TO_TELE_SHDN_L_1V8	GPIO_CAM_PMU2_TO_TELE_SHDN_L_1V8	MAKE_BASE=TRUE OUT 76
GPIO_2	48 GPIO_CAM_PMU2_TO_TELE_LDO_EN_1V8	GPIO_CAM_PMU2_TO_TELE_LDO_EN_1V8	MAKE_BASE=TRUE OUT 58 92
GPIO_3	48 GPIO_CAM_PMU2_TO_JASPER_SHDN_L_1V8	GPIO_CAM_PMU2_TO_JASPER_SHDN_L_1V8	MAKE_BASE=TRUE OUT 77
GPIO_4	48 NC_CAM_PMU2_GPIO4	NC_CAM_PMU2_GPIO4	MAKE_BASE=TRUE
GPIO_5	GPIO_CAM_PMU2_FROM_WILL_JASPER_INT_L_1V8	GPIO_CAM_PMU2_FROM_WILL_JASPER_INT_L_1V8	NO_TEST=1 MAKE_BASE=TRUE IN 52 77 92
GPIO_6	48 GPIO_CAM_PMU2_TO_WILL_EN_1V8	GPIO_CAM_PMU2_TO_WILL_EN_1V8	MAKE_BASE=TRUE OUT 52 92
GPIO_7	48 NC_CAM_PMU2_GPIO7	NC_CAM_PMU2_GPIO7	MAKE_BASE=TRUE NO_TEST=1
GPIO_8	48 NC_CAM_PMU2_GPIO8	NC_CAM_PMU2_GPIO8	MAKE_BASE=TRUE NO_TEST=1
GPIO_9	48 NC_CAM_PMU2_GPIO9	NC_CAM_PMU2_GPIO9	MAKE_BASE=TRUE NO_TEST=1
GPIO_10	48 NC_CAM_PMU2_GPIO10	NC_CAM_PMU2_GPIO10	MAKE_BASE=TRUE NO_TEST=1
GPIO_11	48 NC_CAM_PMU2_GPIO11	NC_CAM_PMU2_GPIO11	MAKE_BASE=TRUE NO_TEST=1
GPIO_12	48 NC_CAM_PMU2_GPIO12	NC_CAM_PMU2_GPIO12	MAKE_BASE=TRUE NO_TEST=1
GPIO_13	Camera PMU2 GPIO13 intentionally not aliased		
CLKO_1	48 CLK_CAM_PMU2_TO_TELE_24M_1V8	CLK_CAM_PMU2_TO_TELE_24M_1V8	MAKE_BASE=TRUE OUT 76
CLKO_2	48 CLK_CAM_PMU2_TO_WIDE_24M_1V8	CLK_CAM_PMU2_TO_WIDE_24M_1V8	MAKE_BASE=TRUE OUT 75
CLKO_3	48 CLK_CAM_PMU2_TO_SWIDE_24M_1V8	CLK_CAM_PMU2_TO_SWIDE_24M_1V8	MAKE_BASE=TRUE OUT 76
CLKO_4	48 NC_CAM_PMU2_CLKO4	NC_CAM_PMU2_CLKO4	NO_TEST=1 MAKE_BASE=TRUE

POWER

VLDO1	47 PP3V0_WILL_VDD	PP3V0_WILL_VDD	VOLTAGE=3.0 MAKE_BASE=TRUE 62
VLDO2	47 NC_CAM_PMU2_LDO2	NC_CAM_PMU2_LDO2	[D53 only] CKPLUS_WAIVE=MULTI_PIN_NC_NETS MAKE_BASE=TRUE
VLDO3	47 PP1V8_TELE_SWIDE_VDDIO	PP1V8_TELE_SWIDE_VDDIO	VOLTAGE=1.8 MAKE_BASE=TRUE 46 49 51 76
VLDO4	47 PP3V0_JASPER_RX_AVDD	PP3V0_JASPER_RX_AVDD	VOLTAGE=3.0 MAKE_BASE=TRUE 77
VLDO5	47 PP3V3_JASPER_TX_AVDD	PP3V3_JASPER_TX_AVDD	VOLTAGE=3.3 MAKE_BASE=TRUE 77
VLDO6	47 PP3V2_WIDE_AVDD1	PP3V2_WIDE_AVDD1	VOLTAGE=3.2 MAKE_BASE=TRUE 75
VLDO7	47 PP1V35_TELE_AVDD2	PP1V35_TELE_AVDD2	VOLTAGE=1.4 MAKE_BASE=TRUE 76
VLDO8	47 PP0V975_TELE_DVDD2	PP0V975_TELE_DVDD2	VOLTAGE=1.0 MAKE_BASE=TRUE 76
VLDO9	47 PP1V1_JASPER_DVDD	PP1V1_JASPER_DVDD	VOLTAGE=1.1 MAKE_BASE=TRUE 77
VLDO10	Camera PMU2 LDO10 used as internal VREF		
BUCK0	47 PP1V6_WIDE_DVDD	PP1V6_WIDE_DVDD	VOLTAGE=1.6 MAKE_BASE=TRUE 75

SYNCING: D53, D54

SYNC_MASTER=0.143.0	SYNC_DATE=05/14/2019
PAGE TITLE	CAMERA: PMU 2: Aliases
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	58 OF 138
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SUBSYSTEM SPECIFIC BOM TABLES

2.925V LDO

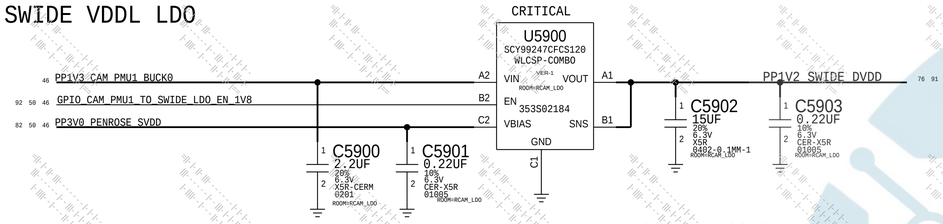
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S02185	353S00015	?	ALL	IC,LDO,REG,2.925V,250MA,ONSEMI

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02185	1	IC,LDO,REG,2.925V,250MA,ONSEMI	U5950	CRITICAL	?

1.2V LDO

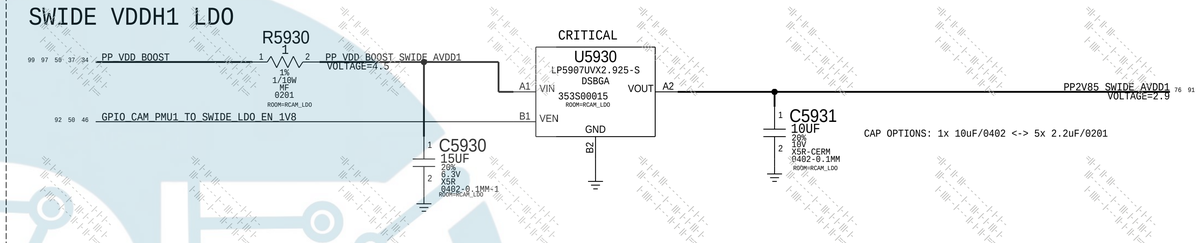
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S02127	353S02184	?	ALL	IC,LDO,REG,1.20V,1000MA,RICHTEK

SWIDE VDDL LDO

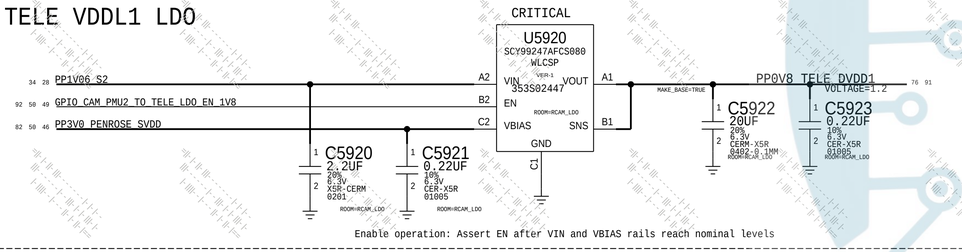


Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

SWIDE VDDH1 LDO



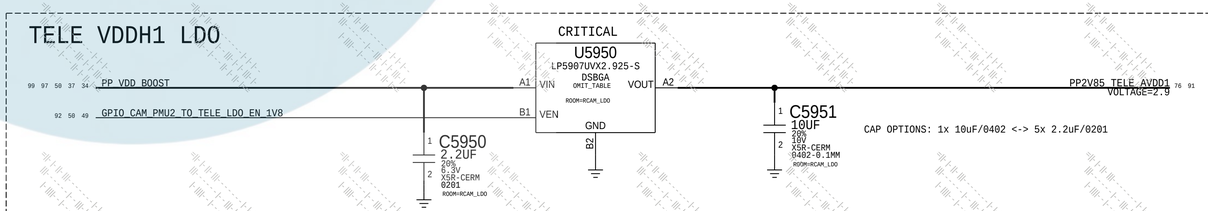
TELE VDDL1 LDO



Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

Misc Aliases

TELE VDDH1 LDO



SYNCING: D52, D53, D54

SYNC_MASTER=0.143.0 SYNC_DATE=05/14/2019

PAGE TITLE

CAMERA: Discrete LDOs + Misc

DRAWING NUMBER 051-05170 SIZE D

REVISION 10.0.0

BRANCH 1

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SHEET 50 OF 117

SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00965	152S00640	?	ALL	Taiyo

15uF 0402 Capacitors (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	[SEE BELOW]	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

(C6251,C6252,C6253,C6254,C6256)

Alex

30 PP_VDD_MAIN
30 PP_VDD_BOOST

C6272 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX — VDDMAIN
C6250 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=RCAM_ALEX — VDD_SW
C6249 220PF 5% 25V C0G 01005 ROOM=RCAM_ALEX — VDD_SW
C6270 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=RCAM_ALEX — VDDMAIN
C6271 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=RCAM_ALEX — VDDHI

RESET*: Req external PD, VDD_MAIN logic level
51 44 IN GPIO_CAM_PMU1_TO_PVDD_RESET_L
49 PP1V8_TELE_SWIDE_VDDIO
R6251 100K 5% 1/32W MF 01005 ROOM=RCAM_ALEX
R6250 100K 5% 1/32W MF 01005 ROOM=RCAM_ALEX
49 OUT GPIO_CAM_PMU1_FROM_ALEX_NHI_TEMP
51 44 IN I2C4_CAM_PMU1_SCL_1V8
51 44 BI I2C4_CAM_PMU1_SDA_1V8

U6250 D2748 CSP-1 338S00616 CRITICAL ROOM=RCAM_ALEX
B1 VDDHI, A5 VDD_SW, C4 VDDMAIN
B4 RESET*
C5 NHI_TEMP
C1 SCL
C2 SDA
C3 VSS, A3 VSS_SW
BUCK_LX A4 — LX_BUCK_ALEX
BOOST_LX A2 — LX_BOOST_ALEX
VOUT A1
VOUT_FB B3 — ANALOG_FB_ALEX
VBOOT B2 — ALEX_BOOT 50
IOUT_SNS B5 — ALEX_IOUT_SNS

CRITICAL L6250 0.47UH-20%-4A-0.048OHM PIWA20120H-SM 152S00640 ROOM=RCAM_ALEX
132S00283 C6260 6800PF 10% 16V X5R 01005 ROOM=RCAM_ALEX NO_VNET_CONNECTION
ALEX_BOOT 50

XW6250 SHORT-20L-0.05MM-SM OMITT ROOM=RCAM_ALEX
[LAYOUT] IOUT_SNS: <14pF max parasitic cap

PPVAR_RCAM_PVDD: I_Load = 900mA (MAX)
VOLTAGE=3.3
PPVAR_RCAM_PVDD 51 78 79

C6255 330PF 10% 16V C0G-X7R 01005 ROOM=RCAM_ALEX
C6251 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
C6252 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
C6253 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
C6254 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX
C6256 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=RCAM_ALEX

XW6251 SHORT-20L-0.05MM-SM OMIT ROOM=RCAM_ALEX
AMUX_RCAM_PVDD OUT 27 51

XW6200 SHORT-01005-SP ROOM=RCAM_ALEX 609-28853 PACK_OPTION=D52,D54
AMUX_PMU_FROM_CAM_PMU OUT 27 43 46

SYNCING: D54

PAGE TITLE
CAMERA: Actuator Supply (Alex)

DRAWING NUMBER 051-05170 — SIZE D
REVISION 10.0.0
BRANCH 1
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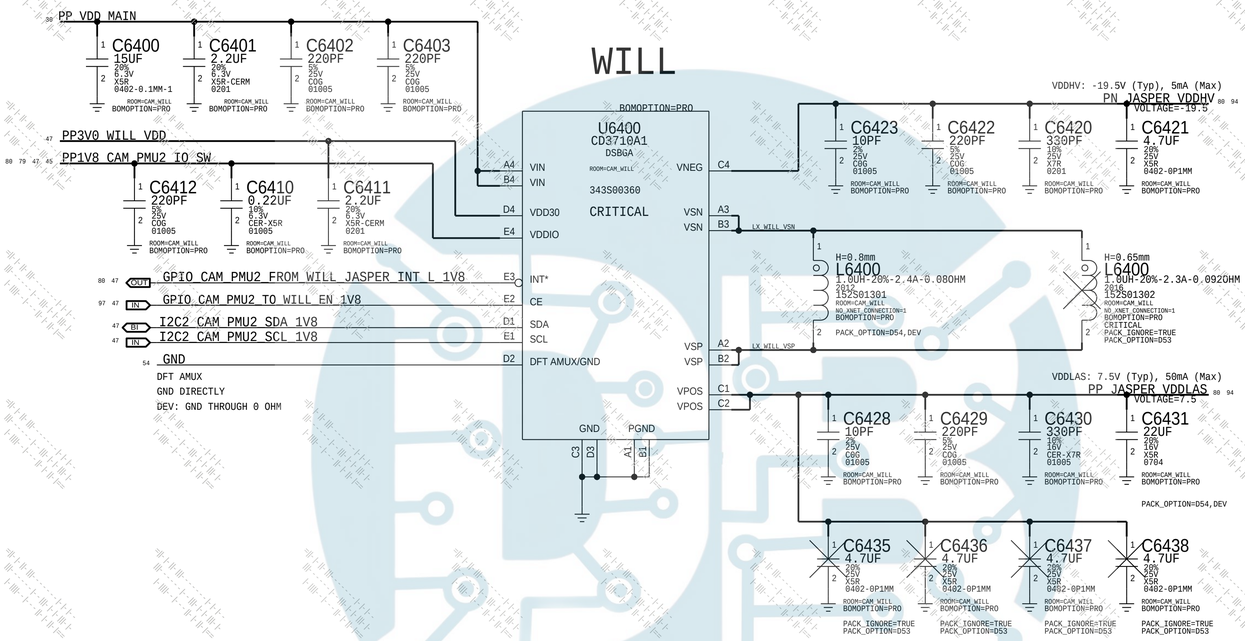
SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01343	152S01301	?	ALL	IND,MLD,1.0UH,20%,2.3A,52MOHM,H=0.8,2012

CRITICAL PART#	COMMENT
152S01301	IND,MLD,1.0UH,20%,2.3A,52MOHM,H=0.8,2012



PAGE TITLE	CAMERA: Will
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	64 OF 138
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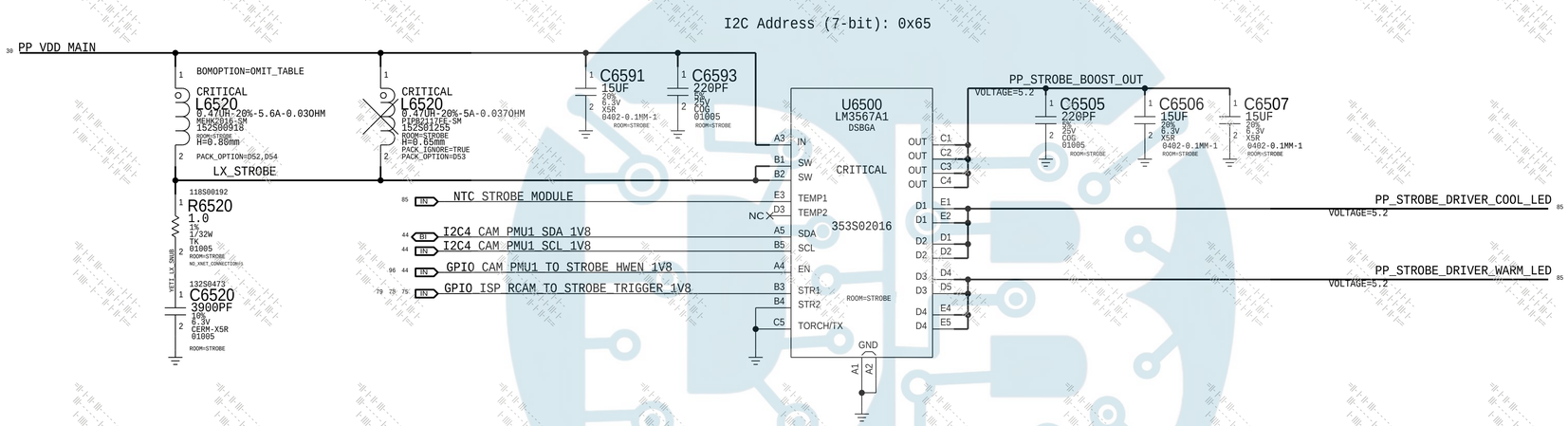
Yeti Inductor

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00872	152S00847	BOARD_ID:D54	L6520	IND,0.47UH,20%,5.6A,30MO,H=0.80,2016,TDK

LED STROBE DRIVER (YETI)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S00918	1	IND,MLD,0.47UH,20%,5.6A,30MO,H=0.80,2016,IAIYO	L6520	CRITICAL	BOARD_ID:D52
152S00847	1	IND,MLD,0.47UH,20%,5.6A,26MO,H=0.80,2016,CYNTEC	L6520	CRITICAL	BOARD_ID:D54



SYNCING: D52, D53, D54

PAGE TITLE	CAMERA: Strobe Driver
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	65 OF 138
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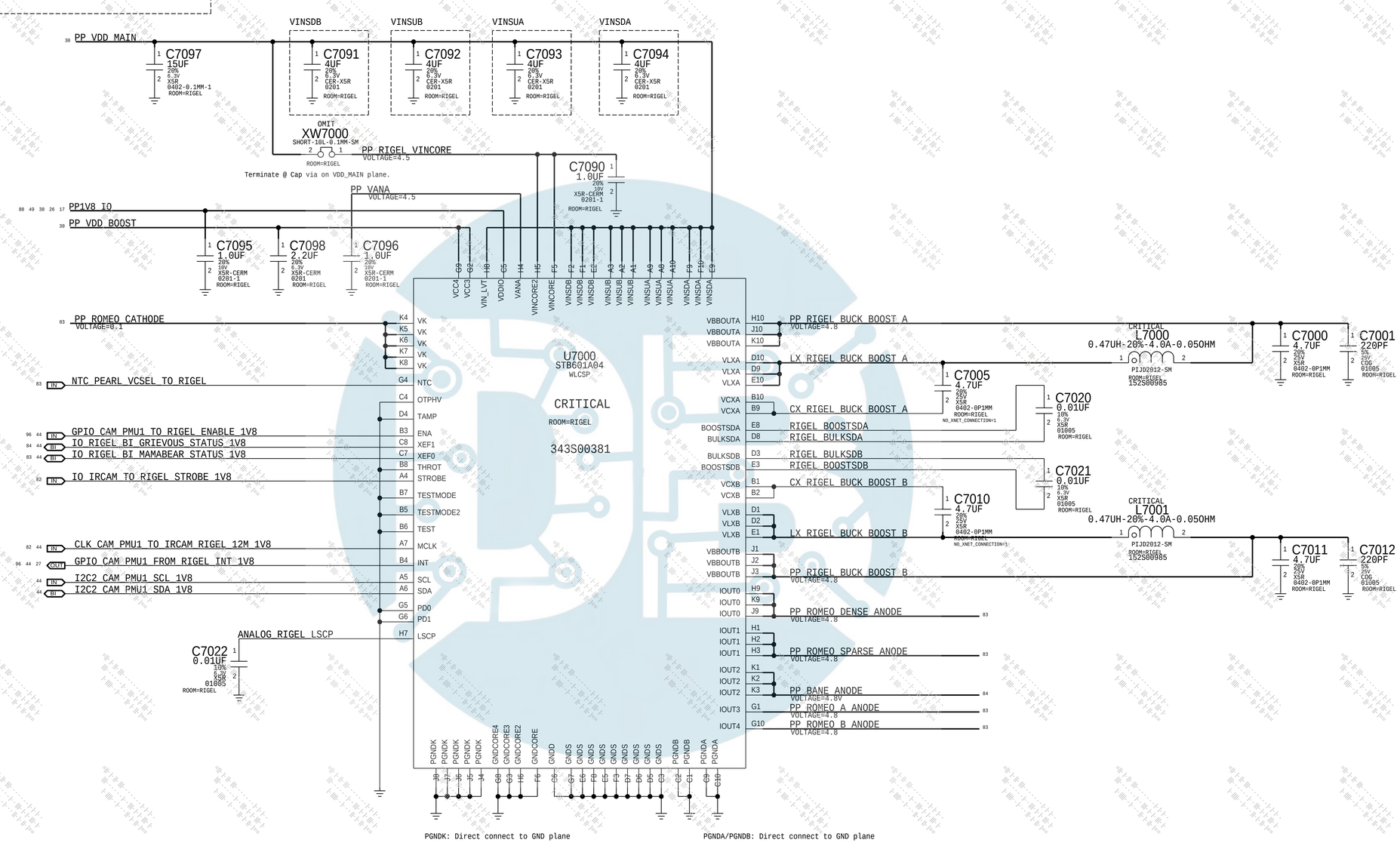
VCSEL DRIVER

RIGEL

SUBSYSTEM SPECIFIC BOM TABLES

INDUCTOR: Alt covered with PMU inductor BOM table



SYNCING: D52, D53, D54

PAGE TITLE	PEARL: VCSEL Driver
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
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SYNCING: D52, D53, D54

PAGE TITLE

PEARL: Aliases

DRAWING NUMBER 051-05170

SIZE D

REVISION 10.0.0

BRANCH 1

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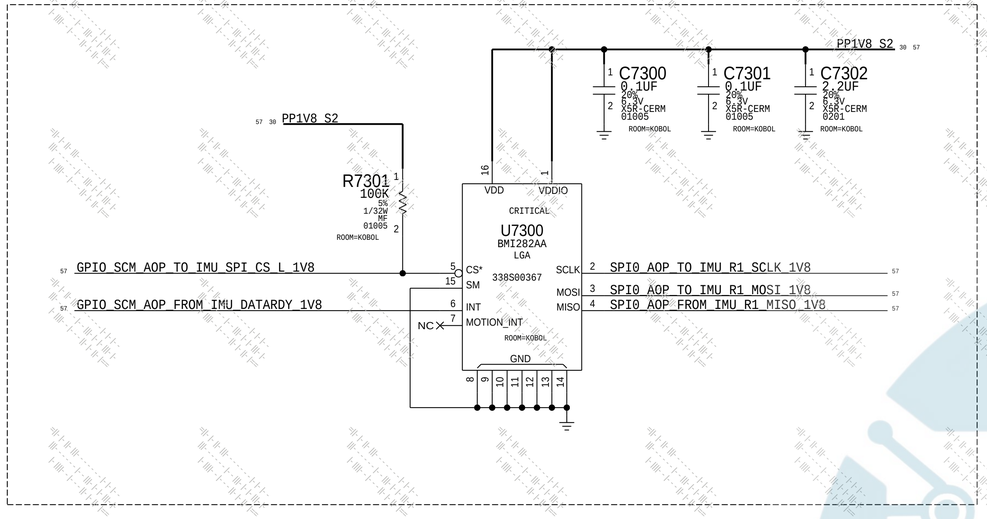
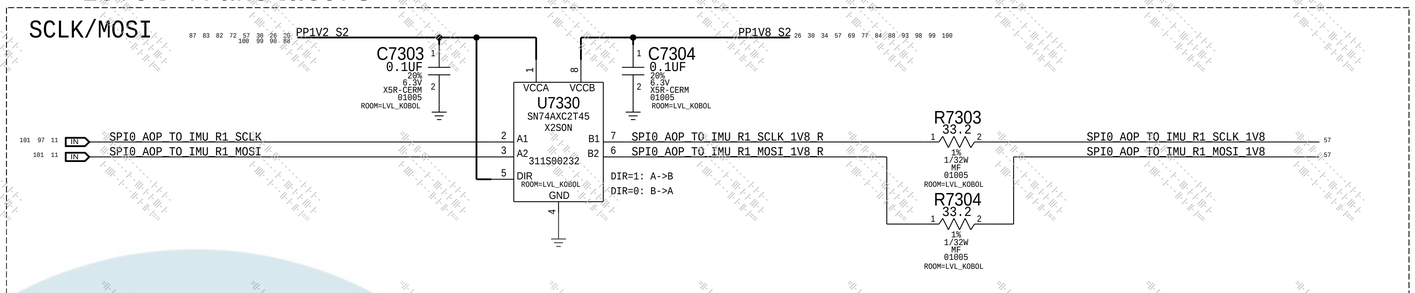
KOBOL - ACCEL & GYRO

IMU

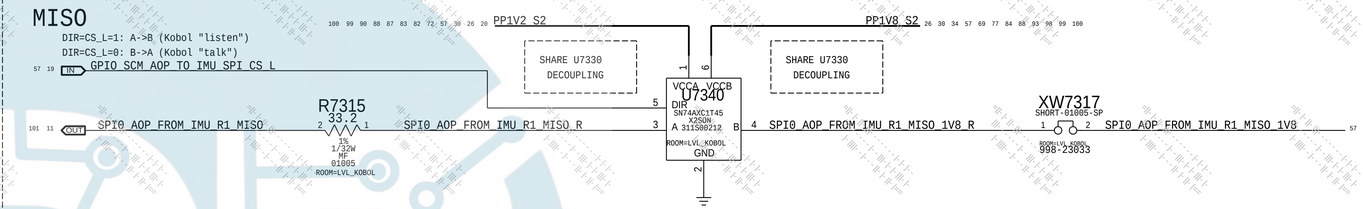


Level Translators

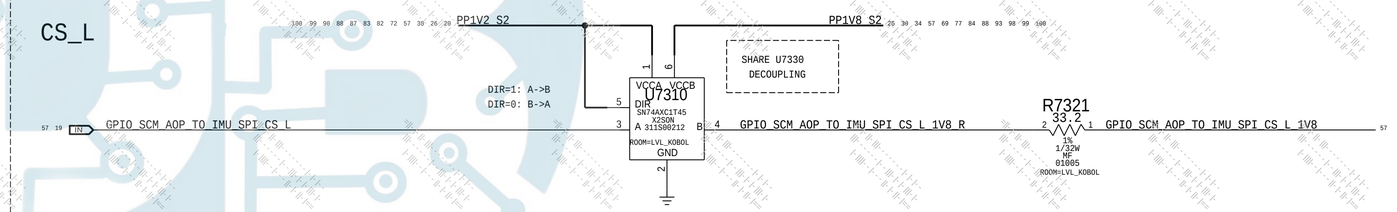
SCLK/MOSI



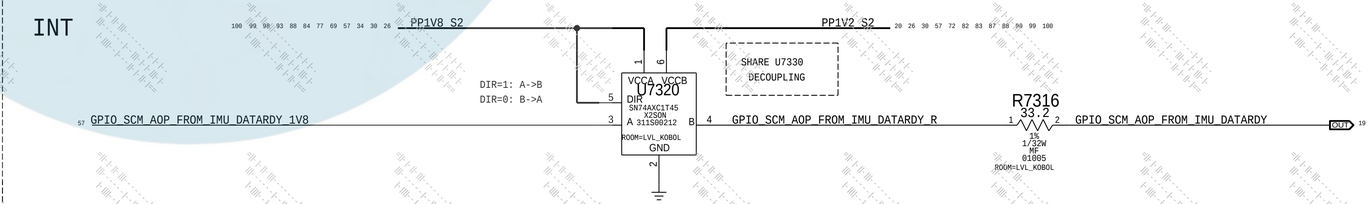
MISO



CS_L



INT



SYNCING: D52, D53, D54

PAGE TITLE	SENSORS: Accel / Gyro
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
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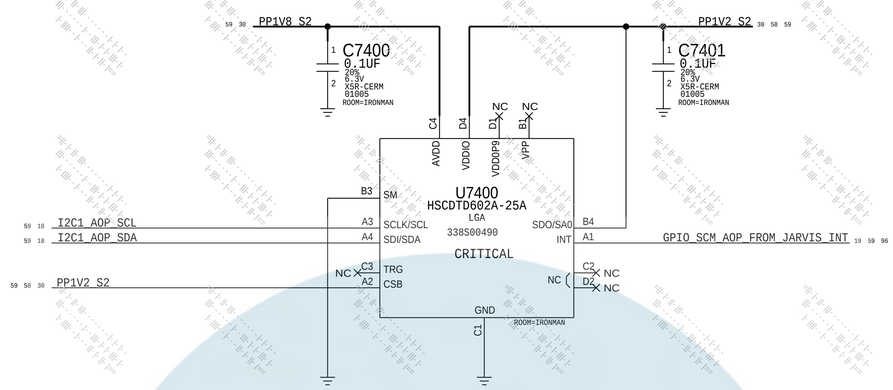
Jarvis (Top)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00665	338S00490	?	U7400	IC,COMPASS,MOL9DEN&MQ-,2SA,I2C,FLGA14



SYNCING: D52, D53, D54

PAGE TITLE
SENSORS: Jarvis (Top)

DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 74 OF 138
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BRIGHTON AUDIO CODEC
(ANALOG INPUTS & OUTPUTS)

SUBSYSTEM SPECIFIC BOM TABLE

Codec

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00631	338S00509	?	U7800	IC,CODEC,BRIGHTON,CS42L77,A1,WLCSP144

CRITICAL PART#	COMMENT
338S00509	IC,CODEC,BRIGHTON,CS42L77,A1,WLCSP144

U7800
CS42L77A1
WLCSP
SYM 1 OF 4
CRITICAL
ROOM=CODEC
338S00509

86 IN MIC1_LOWER_TO_CODEC_AIN1_P — M8 AIN1+
86 IN MIC1_LOWER_TO_CODEC_AIN1_N — L8 AIN1-

85 IN MIC2_REAR_TO_CODEC_AIN2_P — M11 AIN2+
85 IN MIC2_REAR_TO_CODEC_AIN2_N — L11 AIN2-

84 IN MIC3_FRONT_TO_CODEC_AIN3_P — M9 AIN3+
84 IN MIC3_FRONT_TO_CODEC_AIN3_N — L9 AIN3-

86 IN MIC4_LOWER_TO_CODEC_AIN4_P — M10 AIN4+
86 IN MIC4_LOWER_TO_CODEC_AIN4_N — L10 AIN4-

86 IN PENROSE_IR_TO_CODEC_AIN5_P — M3 AIN5A+
86 IN PENROSE_IR_TO_CODEC_AIN5_N — L3 AIN5A-

L4 AIN5B+
L5 AIN5B-

85 IN PENROSE_VIS_TO_CODEC_AIN6_P — K5 AIN6A+
85 IN PENROSE_VIS_TO_CODEC_AIN6_N — K4 AIN6A-

L2 AIN6B+
M2 AIN6B-

J2 AIN7+
K2 AIN7-

J3 AIN8+
K3 AIN8-

H3 AIN9+
H2 AIN9-

J4 AIN10+
J5 AIN10-

L6 AIN11+
L7 AIN11-

K7 AIN12+
K6 AIN12-

96 63 OUT PDM_OUT1_CODEC_TO_SPKRAMP_TOP_CLK — A6 PDMOUT1_CLK
96 63 OUT PDM_OUT1_CODEC_TO_SPKRAMP_TOP_DATA — D6 PDMOUT1_DATA

B6 PDMOUT2_CLK
C6 PDMOUT2_DATA

AOUT+ F11 — CODEC_AOUT_TO_HAC_P 84
AOUT- G11 — CODEC_AOUT_TO_HAC_N 84

DP F1 — 90_MIKEYBUS_DATA_P_R
DN E1 — 90_MIKEYBUS_DATA_N_R
MBUS_REF E2 — ANALOG_MIKEYBUS_REFERENCE IN 86

R7810 100 5% 1/32W MF 01005 ROOM=CODEC
Can be placed near Dock Connector

C7800 100PF 1 2 5% 16V NP0-C0G 01005-1 ROOM=CODEC
R7800 20.0 1 2 5% 1/32W MF 01005 ROOM=CODEC
90_MIKEYBUS_DATA_P — B1 70

R7801 20.0 1 2 5% 1/32W MF 01005 ROOM=CODEC
C7801 100PF 1 2 5% 16V NP0-C0G 01005-1 ROOM=CODEC
90_MIKEYBUS_DATA_N — B1 70

LDCM

TIA_EXOUT G4 NC
TIA_OUT G5
TIA_SENSE G1 — HALOGEN_TIA_IN

HALOGEN_TIA_IOUT
C7820 220PF 5% 25V C0G 01005 ROOM=CODEC

R7821 200K 1% 1/32W MF 01005 ROOM=CODEC NO_ANET_CONNECTION=1
C7821 10UF 1 2 20% 10V X5R-CERM 0402-0.1MM ROOM=CODEC NO_ANET_CONNECTION=1

IO_PMU_FROM_KRAKEN_USB_BRICK_ID_TIA — IN 27 70

SYNCING: D52, D53, D54

PAGE TITLE
AUDIO: Codec: Analog (1/2)

DRAWING NUMBER 051-05170 SIZE D
REVISION 10.0.0
BRANCH 1
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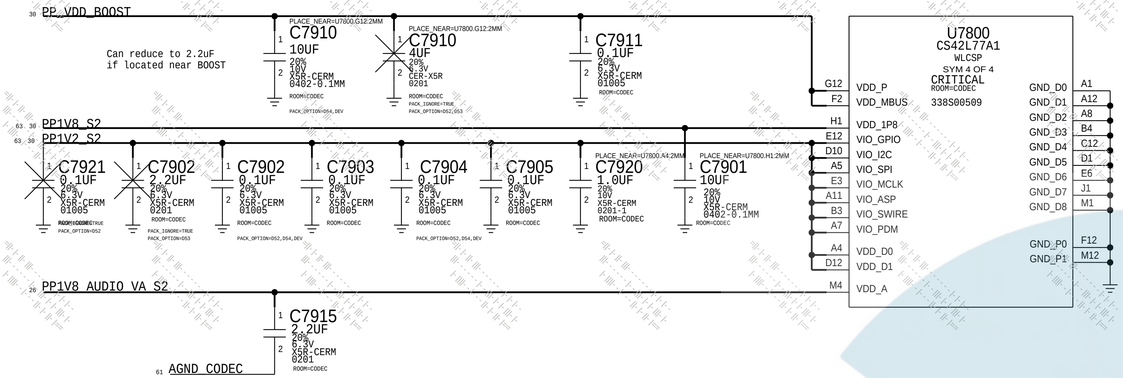
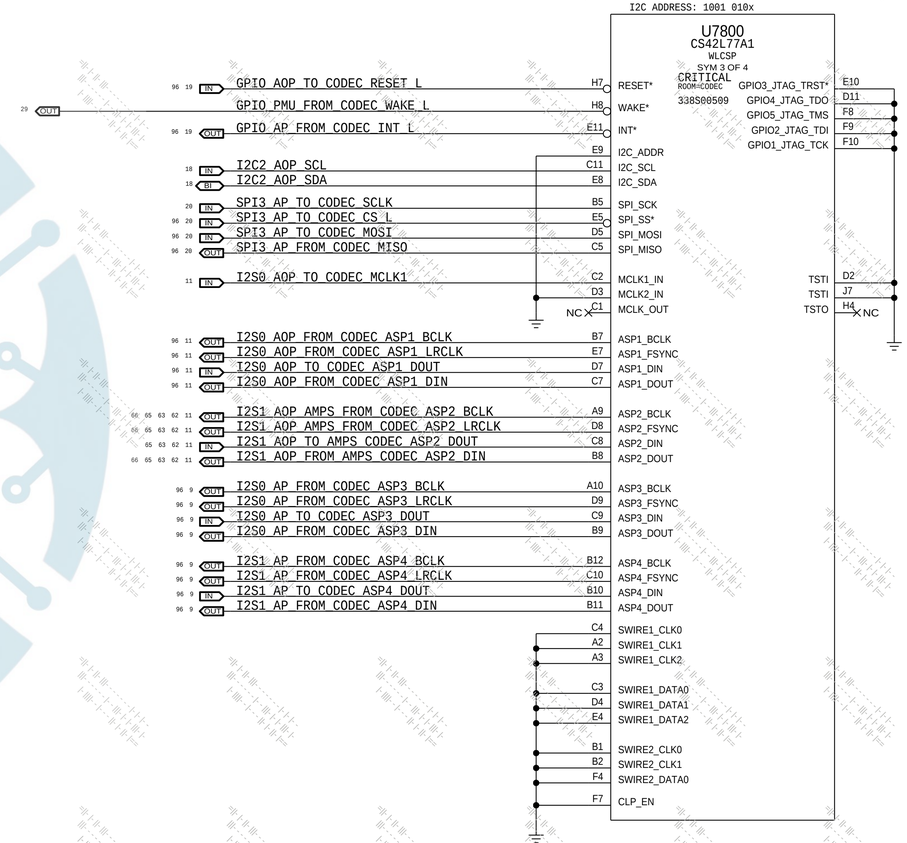
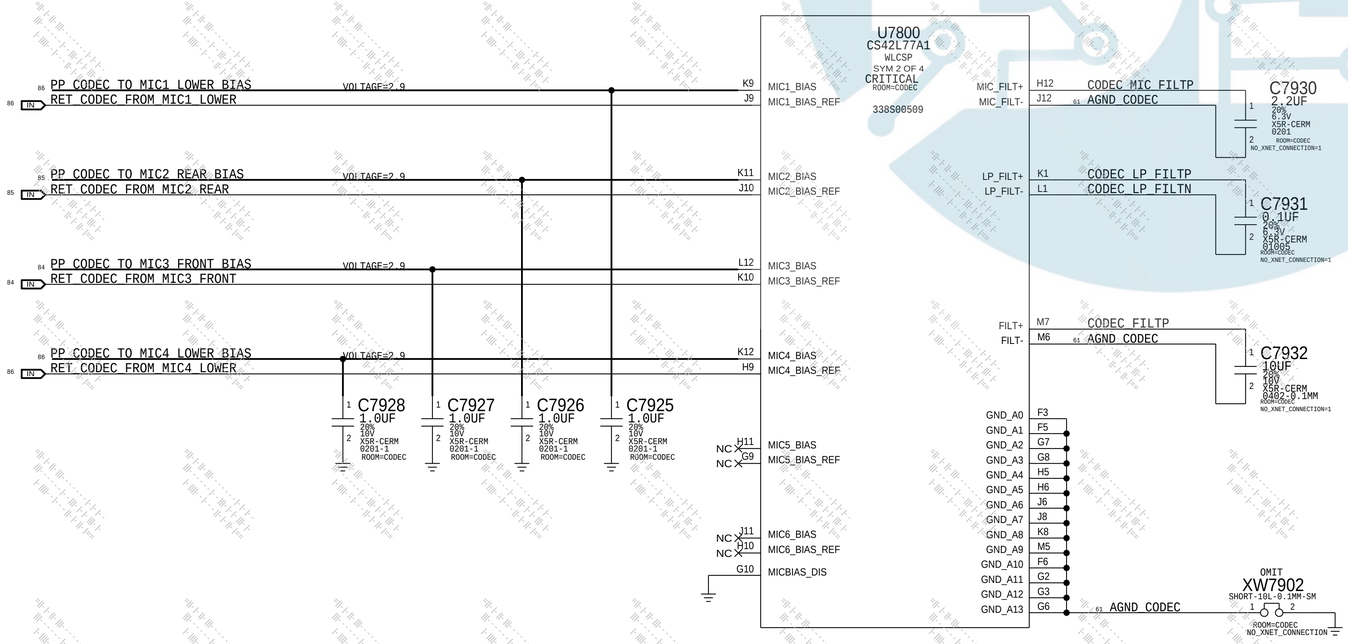
BRIGHTON AUDIO CODEC
(POWER & I/O)







SYNCING: D52, D53, D54

PAGE TITLE	AUDIO: Codec: Power & I/O (2/2)
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REVISION	10.0.0
BRANCH	1
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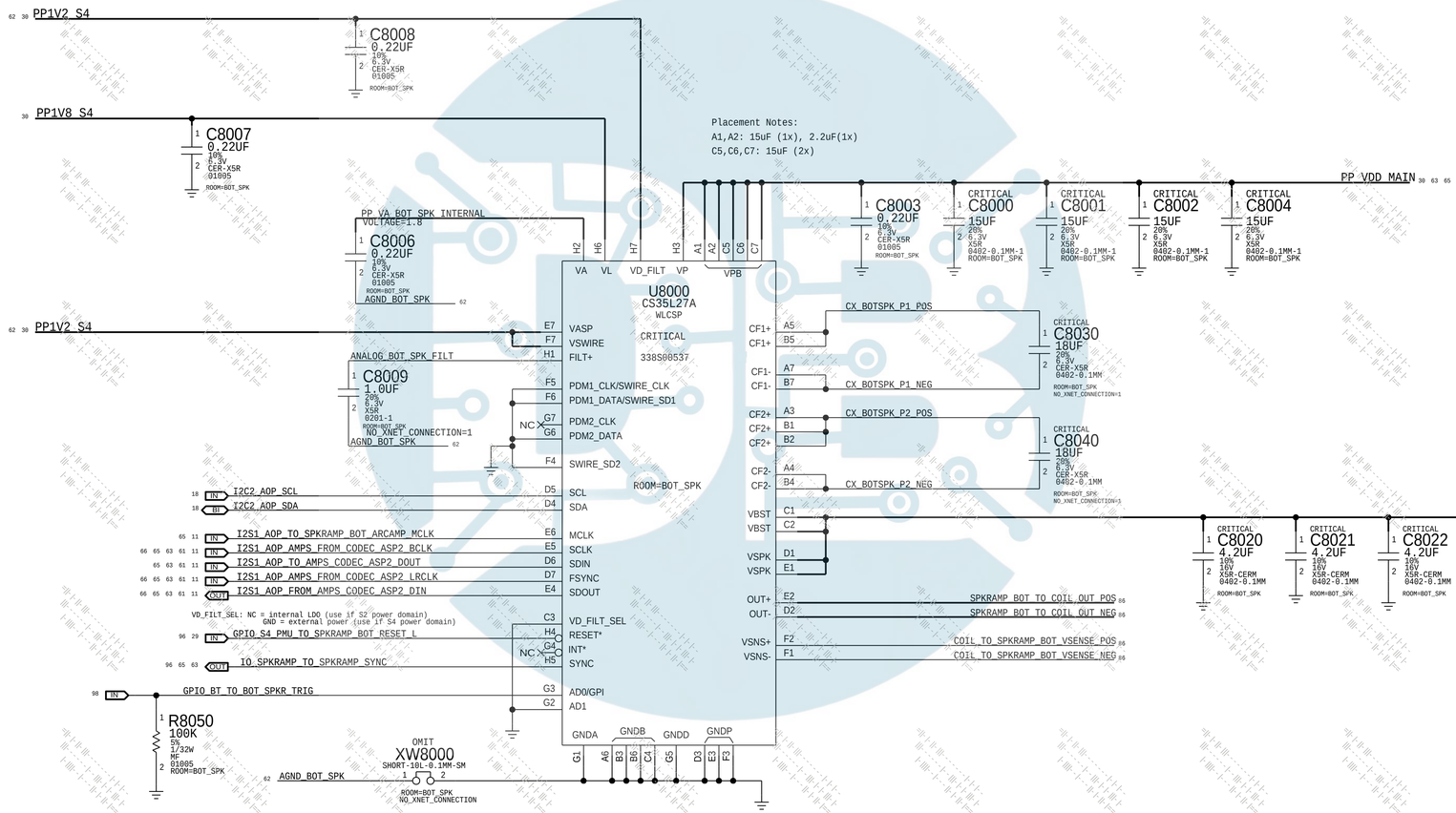
BOT SPEAKER AMP

ALLSTON

POWER DOMAIN NOTES:
1. Use S4 domain if possible, then GND VD_FILT_SEL
2. Can use S2 domain if routing constrained, then NC VD_FILT_SEL



SYNCING: D52, D53, D54

PAGE TITLE	AUDIO: Bot Speaker Amp
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
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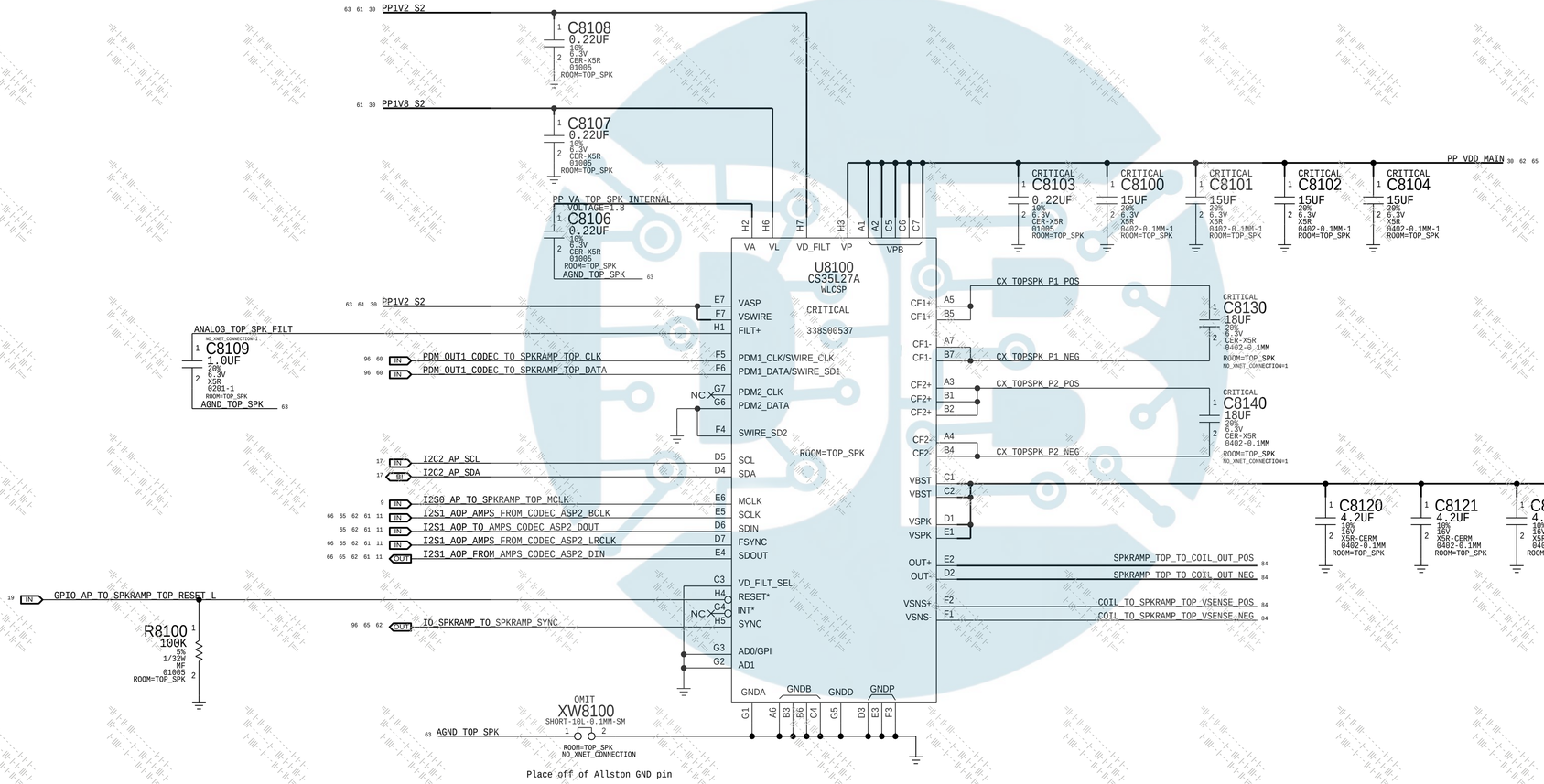
TOP SPEAKER AMP

ALLSTON



SYNCING: D52, D53, D54

PAGE TITLE

AUDIO: Top Speaker Amp

-

DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
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SYNCING: D52, D53, D54

SYNC_MASTER=0.143.0 SYNC_DATE=05/14/2019

PAGE TITLE

AUDIO: Aliases

DRAWING NUMBER 051-05170 SIZE D

REVISION 10.0.0

BRANCH 1

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ARC SPEAKER AMP

ALLSTON

PLACEMENT NOTES:
C8308: Place near VD_FILT
C8307: Place near VL
C8306: Place near VA

65 PP1V2_ARCAMP_VD_FILT_INTERNAL VOLTAGE=1.2

C8308 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC

65 PP1V8_ARCAMP_VA_VL_INTERNAL VOLTAGE=1.8

C8307 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC

C8306 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC

AGND_ARCAMP 65

PLACEMENT NOTES:
A1,A2: 15uF (1x), 2.2uF(1x)
C5,C6,C7: 15uF (3x)

C8303 0.22UF 10% 6.3V CER-X5R 01005 ROOM=ARC

CRITICAL C8300 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=ARC

CRITICAL C8301 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=ARC

CRITICAL C8302 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=ARC

CRITICAL C8304 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=ARC

PP_VDD_MAIN 30 62 63

U8300
CS35L27A
WLCSP

H2	VA		
H6	VL		
H7	VD_FILT		
H3	VP		
A1,A2,C5,C6,C7	VPB		
E7	VASP	CRITICAL	
F7	VSWIRE		
H1	FILT+	338S00537	
F5	PDM1_CLK/SWIRE_CLK		
F6	PDM1_DATA/SWIRE_SD1		
G7	PDM2_CLK		
G6	PDM2_DATA		
F4	SWIRE_SD2		
D5	SCL	ROOM=ARC	
D4	SDA		
E6	MCLK		
E5	SCLK		
D6	SDIN		
D7	FSYNC		
E4	SDOUT		
C3	VD_FILT_SEL		
H4	RESET*		
G4	INT*		
H5	SYNC		
G3	AD0/GPI		
G2	AD1		
G1	GNDA		
A6,B3,B6,C4	GNDB		
G5	GNDD		
D3,E3,F3	GNDP		

65 PP1V2_ARCAMP_VD_FILT_INTERNAL

ANALOG_ARCAMP_FILT

C8309 1.0UF 20% 6.3V X5R 0201-1 ROOM=ARC

AGND_ARCAMP 65
NO_XNET_CONNECTION=1

18 IN I2C2_AOP_SCL
18 BI I2C2_AOP_SDA

62 11 IN I2S1_AOP_TO_SPKRAMP_BOT_ARCAMP_MCLK
66 63 62 61 11 IN I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK
63 62 61 11 IN I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT
66 63 62 61 11 IN I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK
66 63 62 61 11 OUT I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN

VDD_FILT_SEL: NC = Internal VD_FILT LDO

96 63 62 OUT IO_SPKRAMP_TO_SPKRAMP_SYNC
Option to remove SYNC connection

65 PP1V8_ARCAMP_VA_VL_INTERNAL

OMIT
XW8300
SHORT-10L-0.1MM-SM
ROOM=ARC
NO_XNET_CONNECTION

65 AGND_ARCAMP

Place off of Allston GND pin

CF1+ A5 CX_ARCAMP_P1_POS
CF1+ B5
CF1- A7
CF1- B7 CX_ARCAMP_P1_NEG

CRITICAL C8330 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC NO_XNET_CONNECTION=1

CF2+ A3 CX_ARCAMP_P2_POS
CF2+ B1
CF2+ B2
CF2- A4
CF2- B4 CX_ARCAMP_P2_NEG

CRITICAL C8340 18UF 20% 6.3V CER-X5R 0402-0.1MM ROOM=ARC NO_XNET_CONNECTION=1

VBST C1
VBST C2
VSPK D1
VSPK E1

OUT+ E2 ARCAMP_TO_SOLENOID_OUT_POS 96
OUT- D2 ARCAMP_TO_SOLENOID_OUT_NEG 96

VSNS+ F2 SOLENOID_TO_ARCAMP_VSENSE_POS 96
VSNS- F1 SOLENOID_TO_ARCAMP_VSENSE_NEG 96

VOLTAGE=12.0
PP_ARCAMP_VBOOST

CRITICAL C8320 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC

CRITICAL C8321 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC

CRITICAL C8322 4.2UF 10% 16V X5R-CERM 0402-0.1MM ROOM=ARC

C8325 1UF 20% 16V CER-X5R 0201 ROOM=ARC

C8323 220PF 5% 25V C0G 01005 ROOM=ARC

C8324 2200PF 10% 16V X5R-CERM 01005 ROOM=ARC

100 IN GPIO_NFC_TO_ARCAMP_RESET_L

R8300 61.9K 1% 1/32W MF 01005 ROOM=ARC

29 IN GPIO_PMU_NFC_TO_ARCAMP_RESET_L

See Radar # 50911384 for R8300/R8301 values

29 IN GPIO_PMU_NFC_TO_ARCAMP_TRIG

100 IN GPIO_NFC_TO_ARCAMP_TRIG

R8301 61.9K 1% 1/32W MF 01005 ROOM=ARC

R8310 200K 1% 1/32W MF 01005 ROOM=ARC

R8311 200K 1% 1/32W MF 01005 ROOM=ARC

SYNCING: D52, D53, D54

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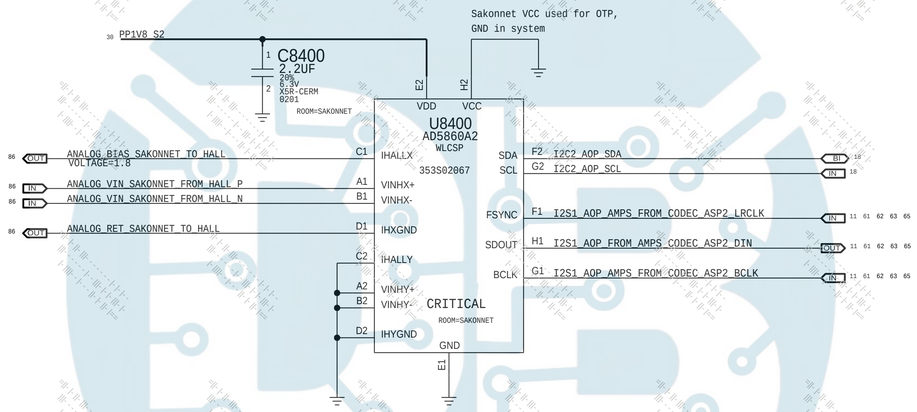
HALL SENSOR

SAKONNET



SYNCING: D52, D53, D54

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ADA

89 88 68 26 PP1V8_TOUCH_S2
89 26 PP3V1_TOUCH_S2
68 26 PP1V2_TOUCH_S2

VDD_CORE_1V2: C9000 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=TOUCH; C9001 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=TOUCH
VDDIO_1V2: C9030 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=TOUCH
VDD_OTP_3V3: C9010 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=TOUCH
VDDIO_1V8_AON: C9020 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=TOUCH; C9022 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=TOUCH
VDDIO_1V8: C9021 1.0UF 10% 10V X5R-CERM 0201-1 ROOM=TOUCH

*PP1V2_TOUCH_S2: DCR from PMU LDO (U3300.L6) to Ada (~U9000.D4) must be <85mOhm

11 IN CLK_NUB_TO_TOUCH_24M

89 88 68 26 PP1V8_TOUCH_S2

68 26 PP1V2_TOUCH_S2

88 19 OUT GPIO_AOP_FROM_TOUCH_INT_L

RADAR #: 50377970
C9040 for glitch mitigation, can remove if channel loading exceeds 20pF
C9040 22PF 5% 16V C0G 01005 ROOM=TOUCH

23 IN SPI2_AP_TO_TOUCH_CS_L
23 IN SPI2_AP_TO_TOUCH_SCLK
21 IN SPI2_AP_TO_TOUCH_MOSI
21 OUT SPI2_AP_FROM_TOUCH_MISO

27 OUT GPIO_PMU_FROM_TOUCH_LDO_EN

89 88 68 26 PP1V8_TOUCH_S2

89 IN SPI_TOUCH_FROM_TFE_MISO_1V8
89 68 OUT SPI_TOUCH_TO_TFE_SCLK_1V8
90 89 68 OUT SPI_TOUCH_TO_TFE_CS_L_1V8
89 OUT GPIO_TOUCH_TO_TFE_INT_L_1V8
89 68 OUT SPI_TOUCH_TO_TFE_MOSI_1V8
90 89 OUT GPIO_TOUCH_TO_TFE_RESET_L_1V8

HIFA = BSYNC0
89 IN GPIO_DISPLAY_TO_TOUCH_HIFA_1V8
90 88 87 IN GPIO_DISPLAY_TO_TOUCH_BSYNC1_1V8

90 89 88 17 IN I2C3_AP_SCL_1V8
90 89 88 17 BI I2C3_AP_SDA_1V8

U9000 BCM15960A0 WLCSP 343S00344 CRITICAL ROOM=TOUCH

F1	VDDIO_1V8_CPLL	JTAG_VDDIO_1V2_1V8_EXT	J6
NC E1	O_AVDD_LDO1P1	JTAG_TCK	H6
F2	REF_CLK_IN	JTAG_TDI	G7 NC
		JTAG_TDO	H7 NC
D2	VDD_OTP_3V3	JTAG_TMS	F6
D4	VDD_CORE_1V2_0	JTAG_TRST*	F7 NC
G3	VDD_CORE_1V2_1	MISC_VDDIO_1V2_1V8_EXT	J5
G1	O_VDD_CORE_1V2	RESET*	F5
H1	VDDCORE_1V6	BOOT_CFG_0	G5
H3	VDDIO_1V8_AON	BOOT_CFG_1	G4
NC J2	VOUT_AON_TEST	TEST_MODE	H5 NC
J1	CORELDO_ENB	PD*	G6
C2	HSPI_VDDIO_1V2_1V8_EXT	GPIO_VDDIO_1V2_1V8_EXT	A6
F4	H_INT*	GPIO_07	E7
E3	H_CS_L1	GPIO_08	D7
NC D1	H_CS_L2	GPIO_09	C7 NC
A3	H_SCLK	SPMI_VDDIO_1V8_EXT	A1
A2	H_SDI	GPIO_10	C1
B2	H_SDO	GPIO_11	B1 NC
NC E4	GPIO_00	I2C_VDDIO_1V2_1V8_EXT	H4
NC C4	GPIO_01	I2C_SCL_1	J4 NC
D3	GPIO_02	I2C_SDA_1	J3 NC
NC B3	GPIO_03	AVSS_CPLL_DIG	E2
B6	ASPI_VDDIO_1V2_1V8_EXT	AVSS_PMU	G2
C6	GPIO_12/A_SDI	VSS	A7
E5	GPIO_13/A_SCLK	VSS	C3
D5	GPIO_14/A_CS_L	VSS	F3
C5	GPIO_15/A_INT_L	VSS	J7
B5	GPIO_16/A_SDO		
A5	GPIO_17/A_ALT_CS_L		
NC B7	GPIO_04		
E6	GPIO_05		
D6	GPIO_06		
B4	I2C_SCL_2		
A4	I2C_SDA_2		

PP1V8_TOUCH_S2 (26 68 88 89) → R9000 20.0K 5% 1/32W MF 01005 ROOM=TOUCH

PP1V2_TOUCH_S2 (26 88)
SWD_NUB_TO_PMU_TOUCH_SWCLK → IN 11 20 96
SWD_NUB_BI_TOUCH_SWDIO → BI 11
PP1V8_TOUCH_S2 (26 68 88 89)
GPIO_AP_TO_TOUCH_RESET_L_1V8 → IN 9 88
BOOT_CONFIG[1:0] = 0b10 (Master in depedendent boot mode on HSPI)
PP1V2_TOUCH_S2 (26 68)
UART2_AOP_TO_TOUCH_TXD → IN 11 88 96
UART2_AOP_FROM_TOUCH_RXD → OUT 11 88
PP1V8_TOUCH_S2 (26 68 88 89)
IO_TOUCH_TO_MANY_SCAN_ACTIVE_1V8 → IN 27 33 35 43 46 75 88 89 90
PP1V8_TOUCH_S2 (26 68 88 89)

89 88 68 26 PP1V8_TOUCH_S2
R9020 10K 5% 1/32W MF 01005 ROOM=TOUCH; R9021 10K 5% 1/32W MF 01005 ROOM=TOUCH; R9022 10K 5% 1/32W MF 01005 ROOM=TOUCH
89 68 SPI_TOUCH_TO_TFE_SCLK_1V8
90 89 68 SPI_TOUCH_TO_TFE_CS_L_1V8
89 68 SPI_TOUCH_TO_TFE_MOSI_1V8

SYNCING: D52, D54

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DISPLAY PMIC

GALENA/CHELAN

Galena vs. Chelan2

D52/D53P = Chelan2 , D53G/D54 = Galena A2E1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00655	1	Galena A2 OTP-1 (A2E1)	U9100	CRITICAL	BOARD_ID:D53G&BOARD_ID:D54
338S00578	1	Chelan	U9100	CRITICAL	BOARD_ID:D52&BOARD_ID:D53P

Inductors

D52/D53P = Taiyo on VOUT3, D53G = no Taiyo, D54 = all Taiyo

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S01355	1	Cyntec VOUT3 Inductor (6.8uH 2520 0.95mm)	L9100	CRITICAL	BOARD_ID:D52
152S01347	1	Cyntec VOUT3 Inductor (6.8uH 2520 1.0mm)	L9100	CRITICAL	BOARD_ID:D53P
152S01313	1	Cyntec VOUT3 Inductor (4.7uH 2520 1.0mm)	L9100	CRITICAL	BOARD_ID:D53G&BOARD_ID:D54
152S01237	1	Cyntec VOUT1/2 Inductor (2.2uH 3030 0.8mm)	L9110	CRITICAL	BOARD_ID:D52
152S01357	2	Cyntec VOUT1/2 Inductor (2.2uH 3030 0.95mm)	L9120, L9130	CRITICAL	BOARD_ID:D52
152S01314	3	Cyntec VOUT1/2 Inductor (2.2uH 3030 1.0mm)	L9110, L9120, L9130	CRITICAL	BOARD_ID:D53G&BOARD_ID:D53P&BOARD_ID:D54

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01356	152S01355	BOARD_ID:D52	L9100	Taiyo 6.8uH 2520 0.95mm
152S01346	152S01347	BOARD_ID:D53P	L9100	Taiyo 6.8uH 2520 1.0mm
152S01339	152S01313	BOARD_ID:D54	L9100	Taiyo 4.7uH 2520 1.0mm
152S01340	152S01314	BOARD_ID:D54	L9110,L9120,L9130	Taiyo 2.2uH 3030 1.0mm

PP_VDD_MAIN

PLACE NEAR VINP2A PINS

C9104 CRITICAL 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=D_PMIC

C9194 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=D_PMIC

C9100 220PF 5% 25V C0G 01005 ROOM=D_PMIC

PLACE NEAR VINP2B PINS

C9101 220PF 5% 25V C0G 01005 ROOM=D_PMIC

C9193 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=D_PMIC

C9103 CRITICAL 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=D_PMIC

PLACE NEAR L9110

C9192 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=D_PMIC

PLACE NEAR L9100

C9195 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=D_PMIC

PLACE NEAR VINA PINS

C9105 CRITICAL 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=D_PMIC

C9102 CRITICAL 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=D_PMIC

C9106 220PF 5% 25V C0G 01005 ROOM=D_PMIC

PP1V8_S2

OMIT_TABLE
CRITICAL
L9100
4.7UH-20%-2.0A-0.19OHM
PIJA2520-SM
152S01240
ROOM=D_PMIC

R9121 2.2K 5% 1/32W MF 01005 ROOM=D_PMIC

R9120 2.2K 5% 1/32W MF 01005 ROOM=D_PMIC

R9122 33.2 1% 1/32W MF 01005 ROOM=D_PMIC

I2C_DISPLAY_SCL_1V8 (OUT)

I2C_DISPLAY_SDA_1V8 (BI)

I2C_DISPLAY_SDA_1V8_R

CKPLUS_WAIVE=I2C_PULLUP

IO_DISPLAY_TO_DPMIC_VOUT12_EN_1V8 (IN)

IO_DISPLAY_TO_DPMIC_VOUT3_EN_1V8 (IN)

GPIO_SEQ_PMU_TO_DISPLAY_RESET_L_1V8 (IN)

GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8 (IN)

LX_DPMIC_VOUT3

PP7V3_DISPLAY_AVDDH

VOLTAGE=7.3

C9112 22UF 20% 16V X5R 0704 ROOM=D_PMIC

C9111 220PF 5% 25V C0G 01005 ROOM=D_PMIC

C9110 220PF 5% 25V C0G 01005 ROOM=D_PMIC

R9102 511K 1% 1/32W MF 01005 ROOM=D_PMIC

R9101 511K 1% 1/32W MF 01005 ROOM=D_PMIC

R9100 511K 1% 1/32W MF 01005 ROOM=D_PMIC

U9100
CHELAN2-GAL-STUDY
BGA
998-20509
OMIT_TABLE
CRITICAL

VINA	C7		
VINP2A	E1, F1, G1		
VINP2B	E7, F7, G7		
SCL	D4	PMU_SHD*	D2
SDA	D5	PANIC_OUT*	D3
STROBE_EN	B6	ICLB	D1
VOUT12_EN	D6	AMUX	C6
VOUT3_EN	C5	VLDO1	A4 NC
RESET*	D7	VLDO1	B4 NC
PANIC*	E4	FB1	C4
LX3	A6	LX1	A2
VOUT3	A5	LX1	B2
		LX1	C2
		VOUT1	A3
		VOUT1	B3
		VOUT1	C3
		LX2B	E6
		LX2B	F6
		LX2B	G6
		VOUT2B	E5
		VOUT2B	F5
		VOUT2B	G5
		VOUT2A	E3
		VOUT2A	F3
		VOUT2A	G3
		LX2A	E2
		LX2A	F2
		LX2A	G2
GNDA	B5		
GNDP1	B7, A1, B1, C1		
GNDP2	F4, G4		
GNDP3	A7		

ROOM=D_PMIC

Tie GNDP1/GNDP2/GNDP3 directly to GND plane

PP9100 P2MM-NSM SM (PP) ROOM=TEST

PP9101 P2MM-NSM SM (PP) ROOM=TEST

IO_DPMIC_SHDB_L_1V8

IO_DPMIC_TO_DISPLAY_PANICB_L_1V8 (OUT)

IO_DPMIC_ICLB_1V8

AMUX_PMU_FROM_DISPLAY (OUT)

ANALOG_FB_DPMIC

LX_DPMIC_VOUT1

LX_DPMIC_VOUT2B

LX_DPMIC_VOUT2A

118S00200 NOSTUFF R9116 2.2 1% 1/32W MF 01005 ROOM=D_PMIC NO_XNET_CONNECTION=1 PACK_OPTION=D52,D54,DEV

NOSTUFF C9116 220PF 5% 25V C0G 01005 ROOM=D_PMIC PACK_OPTION=D52,D54,DEV

OMIT_TABLE
CRITICAL
L9130
2.2UH-20%-3.7A-0.071OHM
PIJF030H
152S01237
ROOM=D_PMIC

118S00200 NOSTUFF R9115 2.2 1% 1/32W MF 01005 ROOM=D_PMIC NO_XNET_CONNECTION=1 PACK_OPTION=D52,D54,DEV

NOSTUFF C9115 220PF 5% 25V C0G 01005 ROOM=D_PMIC PACK_OPTION=D52,D54,DEV

OMIT_TABLE
CRITICAL
L9120
2.2UH-20%-3.7A-0.071OHM
PIJF030H
152S01237
ROOM=D_PMIC

AMUX_PMU_FROM_DISPLAY

C9117 1000PF 10% 6.3V X5R-CERM 01005 ROOM=D_PMIC

OMIT_TABLE
CRITICAL
L9110
2.2UH-20%-3.7A-0.071OHM
PIJF030H
152S01237
ROOM=D_PMIC

NOTES:
1. Galena: wire FB to VOUT (stuff R9131, NOSTUFF R9130)
2. Chelan: wire FB to GND (stuff R9130, NOSTUFF R9131)

BOMOPTION=BOARD_ID:D52&BOARD_ID:D53P

R9130 0.00 0% 1/32W MF 01005 ROOM=D_PMIC

PACK_IGNORE=TRUE
PACK_OPTION=D52,D53,DEV

BOMOPTION=BOARD_ID:D53G&BOARD_ID:D54

R9131 0.00 0% 1/32W MF 01005 ROOM=D_PMIC

VOLTAGE=4.6
PP4V6_DISPLAY_VDDEL

C9125 220PF 5% 25V C0G 01005 ROOM=D_PMIC

C9120 220PF 5% 25V C0G 01005 ROOM=D_PMIC

C9121 22UF 20% 10V X5R 0603 ROOM=D_PMIC

C9122 22UF 20% 10V X5R 0603 ROOM=D_PMIC

C9123 22UF 20% 10V X5R 0603 ROOM=D_PMIC

C9124 22UF 20% 10V X5R 0603 ROOM=D_PMIC

VOLTAGE=-7.0
PNVAR_DISPLAY_VSSEL

C9134 220PF 5% 25V C0G 01005 ROOM=D_PMIC

C9130 220PF 5% 25V C0G 01005 ROOM=D_PMIC

C9131 22UF 20% 10V X5R 0704 ROOM=D_PMIC

C9132 22UF 20% 10V X5R 0704 ROOM=D_PMIC

C9133 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=D_PMIC

VOUT2X
Target voltage: -6V to -3V
Max operational: -7V
Max capable: -9V

SYNCING: D52, D53, D54

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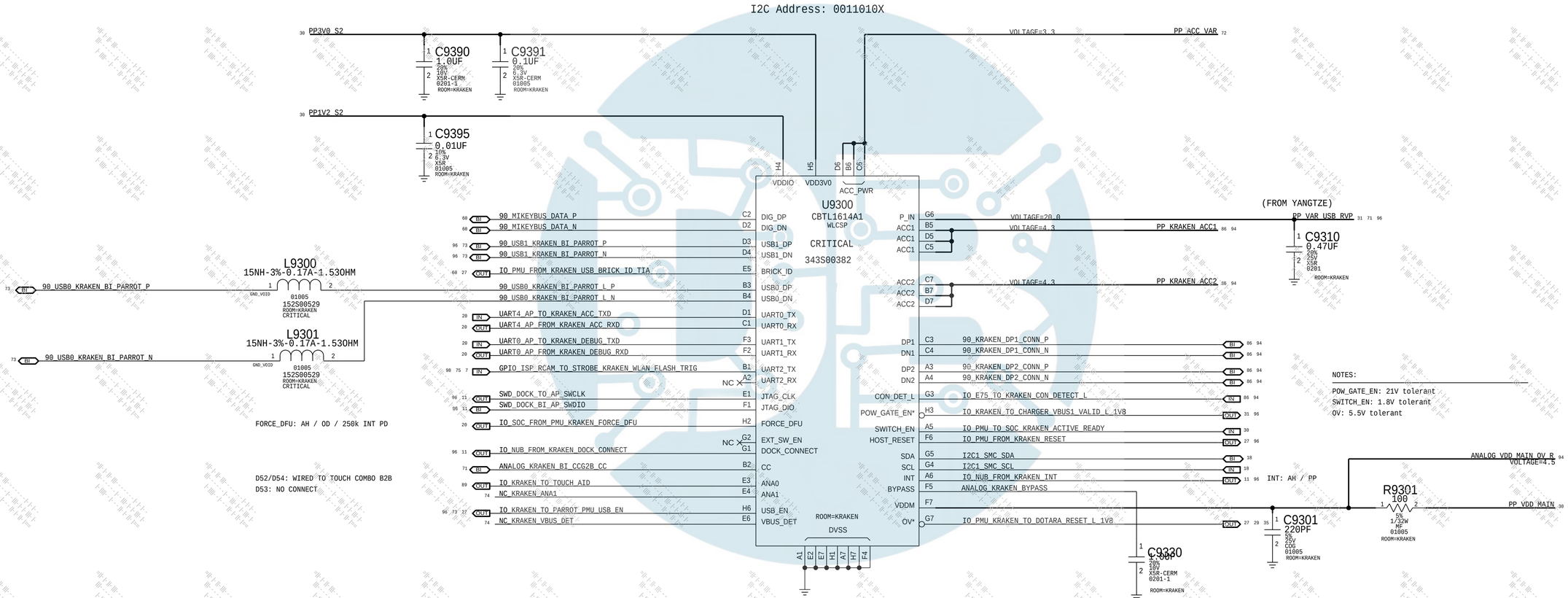
SUBSYSTEM SPECIFIC BOM TABLES

LIGHTNING CONTROLLER

KRAKEN

I2C Address: 0011010X



PAGE TITLE: LIGHTNING: Lightning Controller

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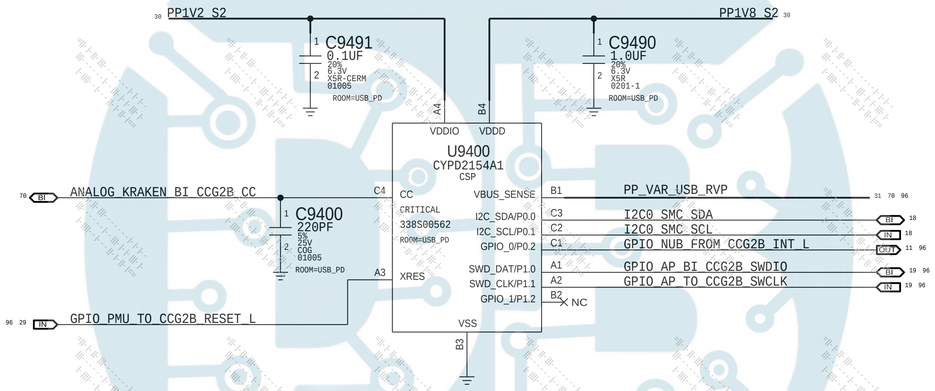
USB-PD

CCG2B



SYNCING: D52, D53, D54

PAGE TITLE

LIGHTNING: USB-PD

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ACCESSORY POWER

GECKO2

SUBSYSTEM SPECIFIC BOM TABLES

Inductor

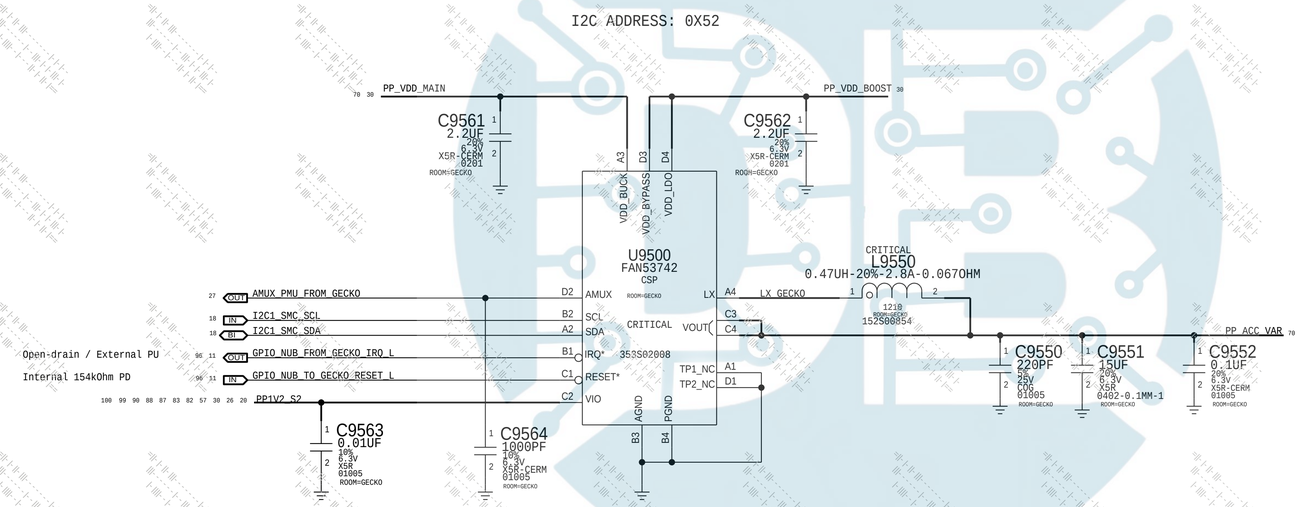
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01279	152S00854	?	L9550	IND,PWR,0.47UH,20%,2.7A,TY

Output Capacitor (single-source Murata)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	(C9551)	0402,15uF,6.3V, Kyocera

All RefDes in ( ) are single-sourced from Murata

I2C ADDRESS: 0X52



SYNCING: D52, D53, D54

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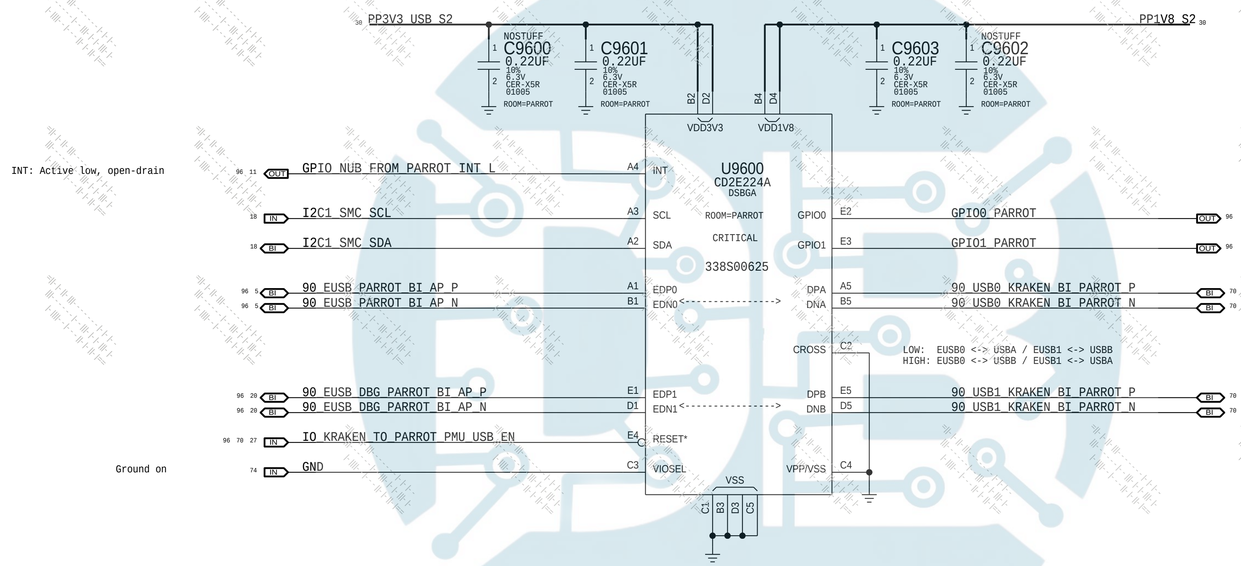
USB REPEATER

PARROT

[LAYOUT] Parrot layout guidelines:
1. 3.3V power pins are shorted together internally, as are 1.8V pins
2. Keep decoupling cap <3mm from power pin
3. Minimize coupling between 1.8V and 3.3V rails



SYNCING: D52, D53, D54, DEV

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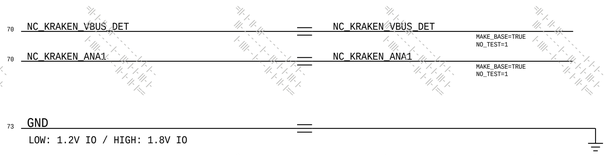

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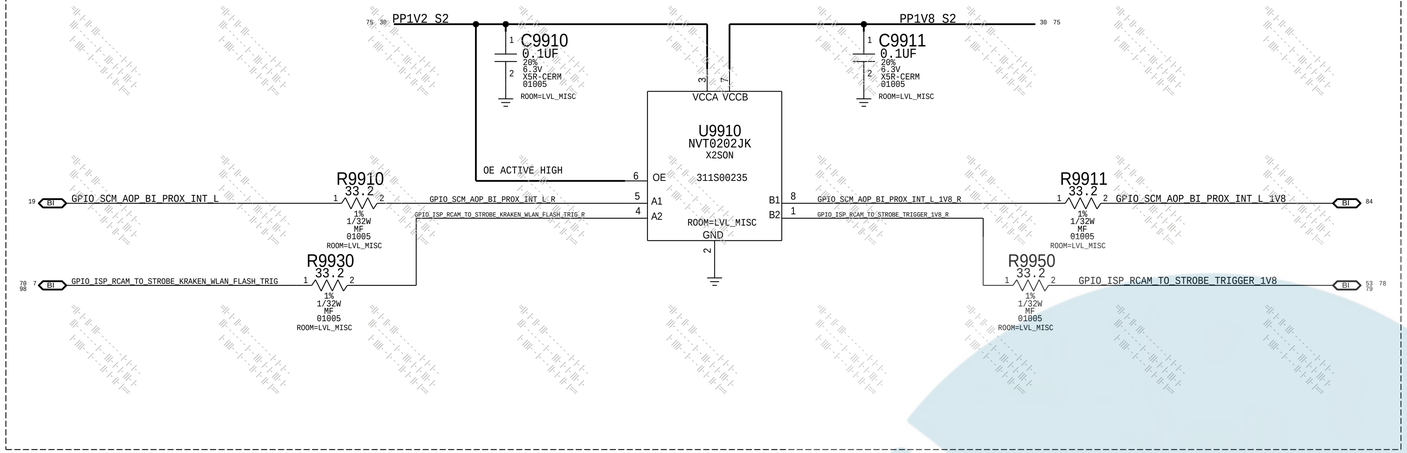
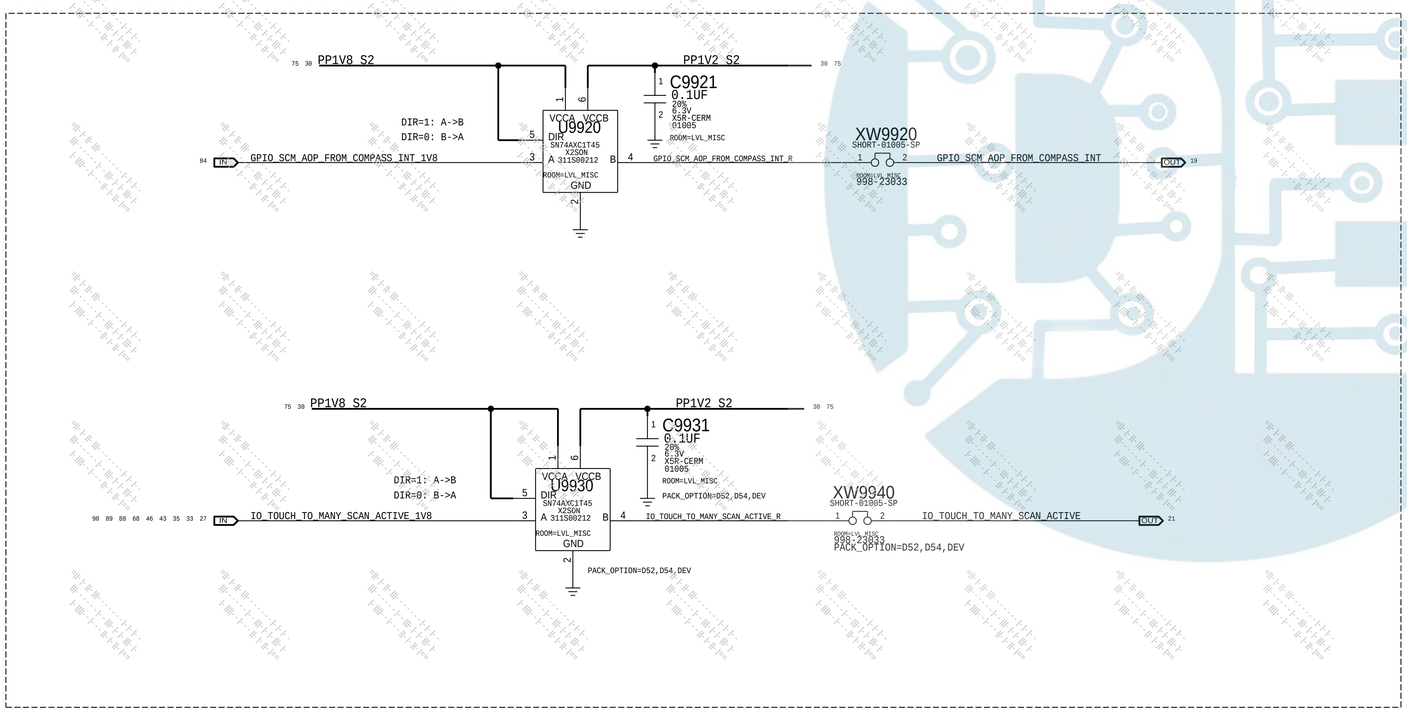
MISCELLANEOUS LEVEL TRANSLATORS

PROX INTERRUPT + STROBE TRIGGER



TOUCH SCAN ACTIVE + COMPASS INTERRUPT



SYNCING: D52, D53, D54, DEV

PAGE TITLE: LVL SHIFT: Misc Nets

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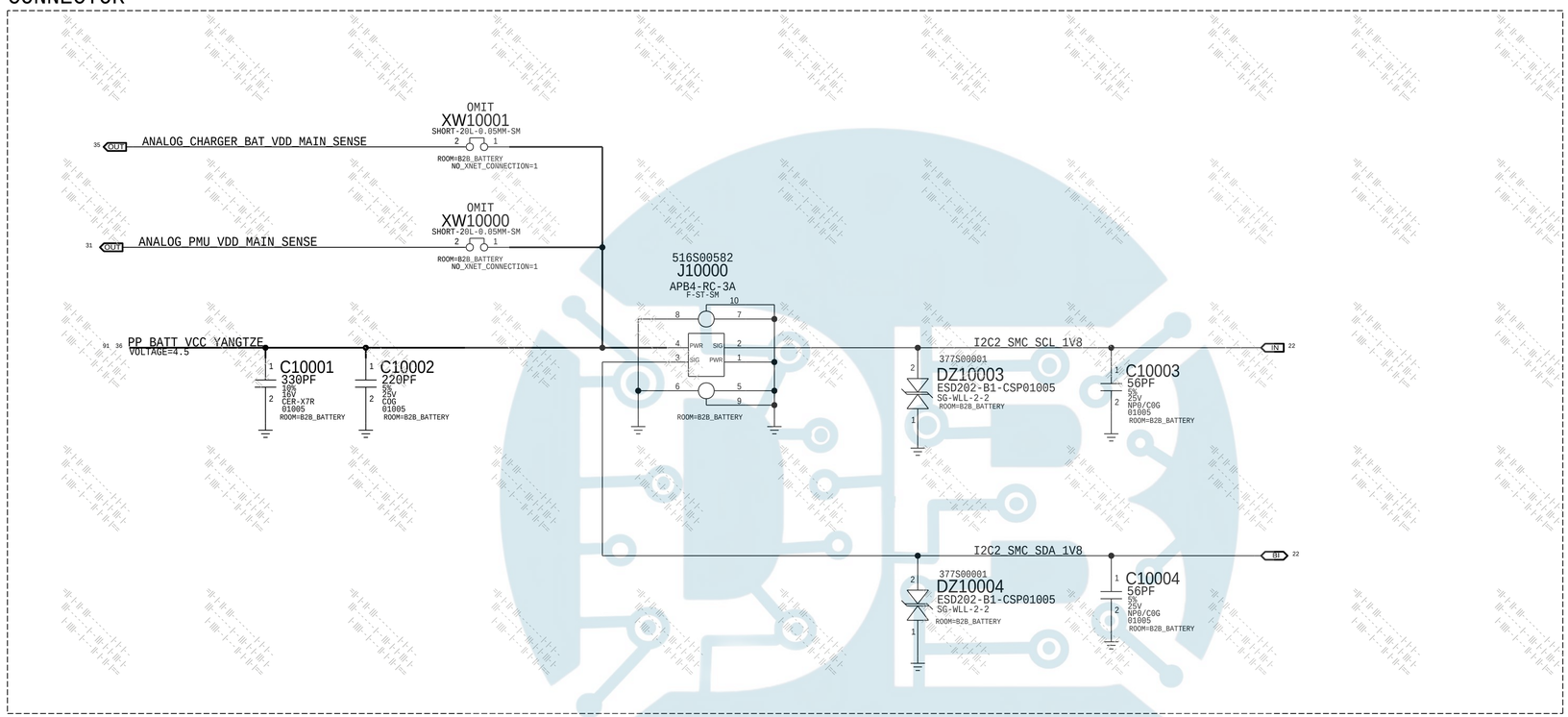
BATTERY B2B

CONNECTOR

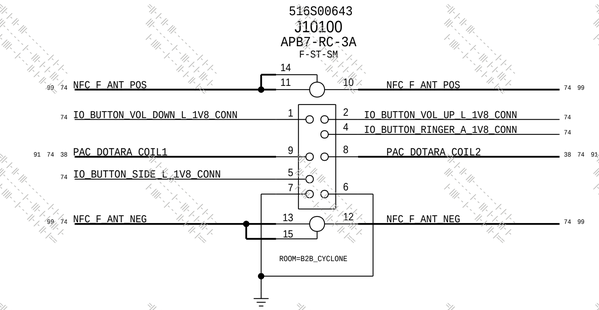


NOT SYNCING

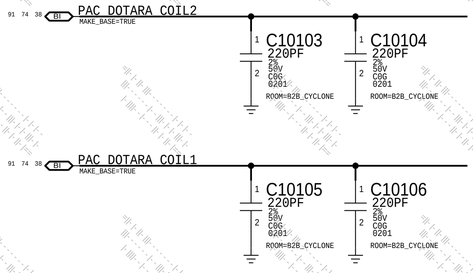
PAGE TITLE	B2B: Battery
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	100 OF 138
SHEET	73 OF 117

CYCLONE B2B

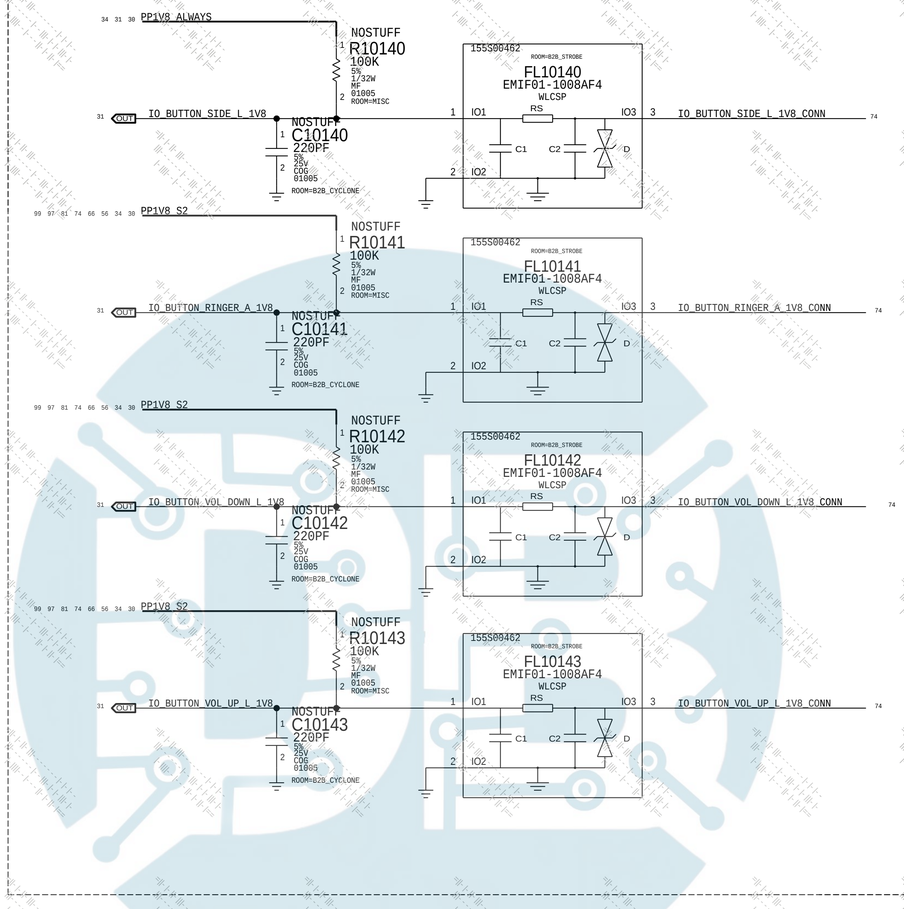
CONNECTOR



POWER FILTERS



IO FILTERS

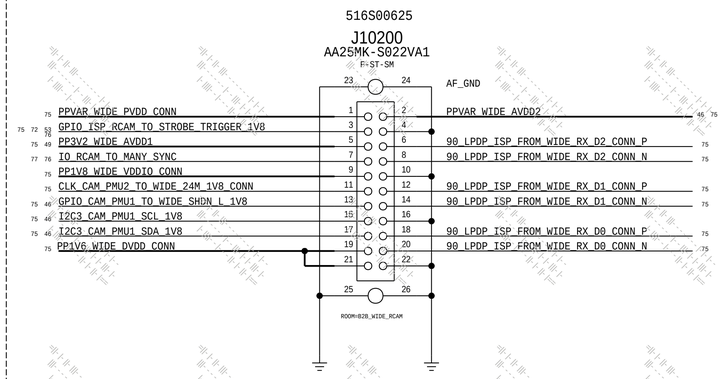


NOT SYNCING

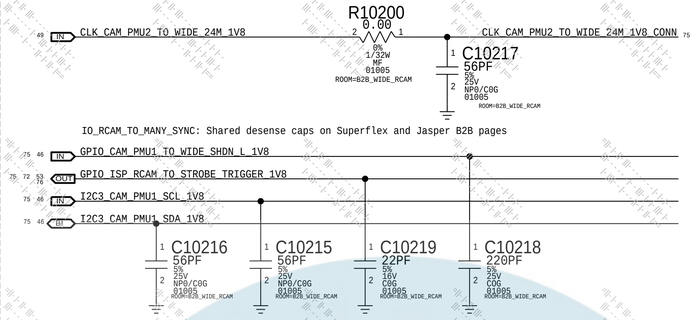
PAGE TITLE	B2B: Cyclone
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	101 OF 138
SHEET	74 OF 117

WIDE CAMERA B2B

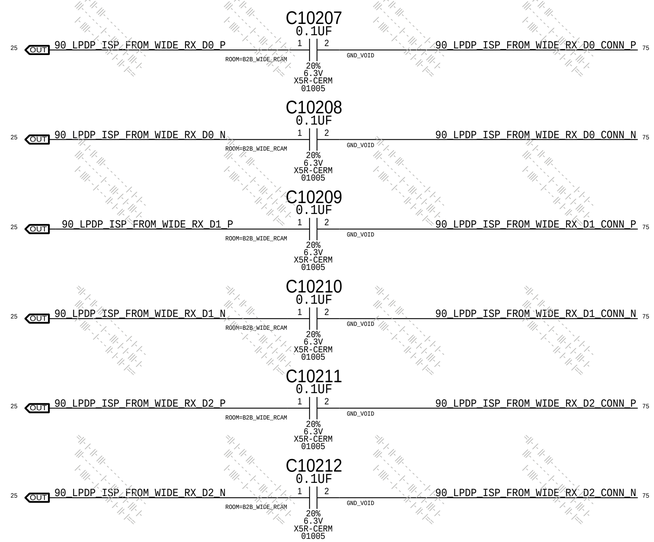
CONNECTOR



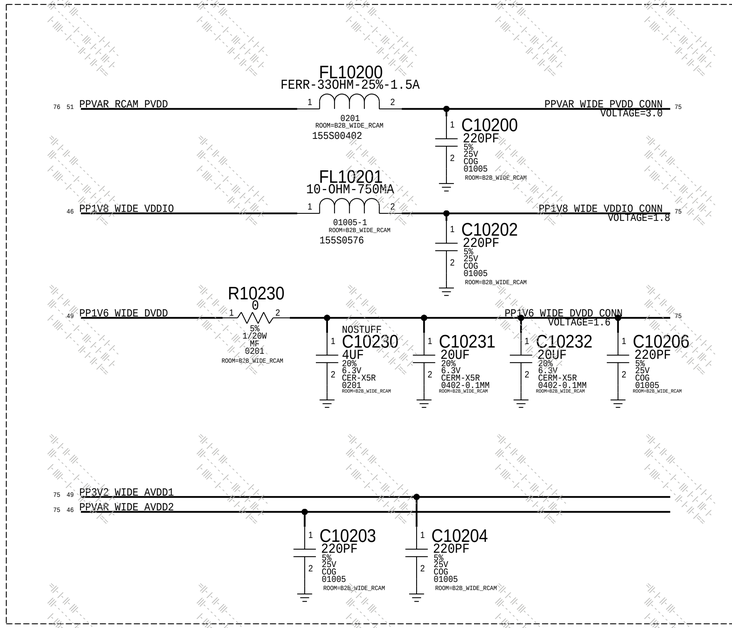
IO FILTERS



LPDP FILTERS



POWER FILTERS

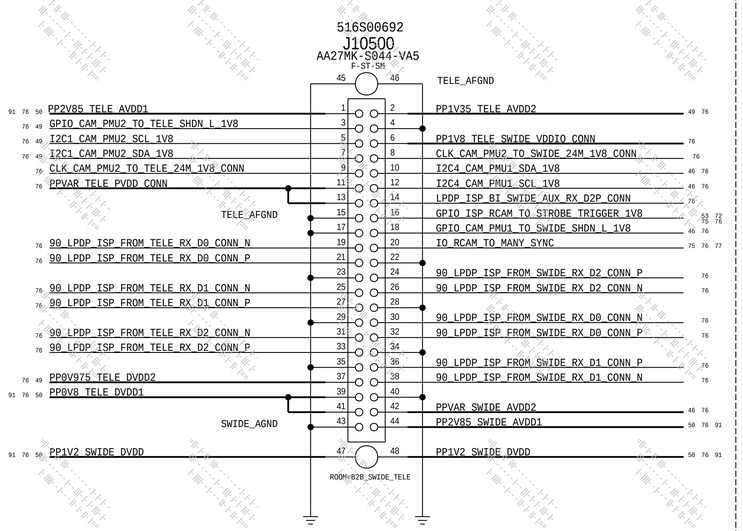


NOT SYNCING

PAGE TITLE	B2B: Camera Wide
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	102 OF 138
SHEET	75 OF 117

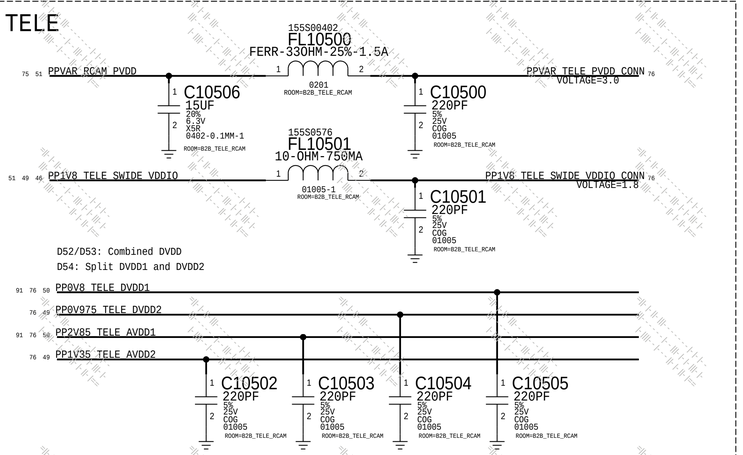
SUPERFLEX B2B
SWIDE + TELE COMBO

CONNECTOR

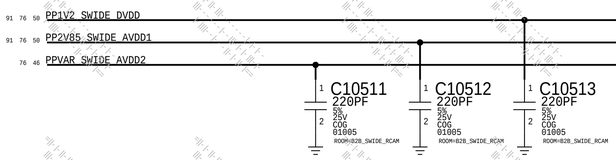


POWER FILTERS

TELE

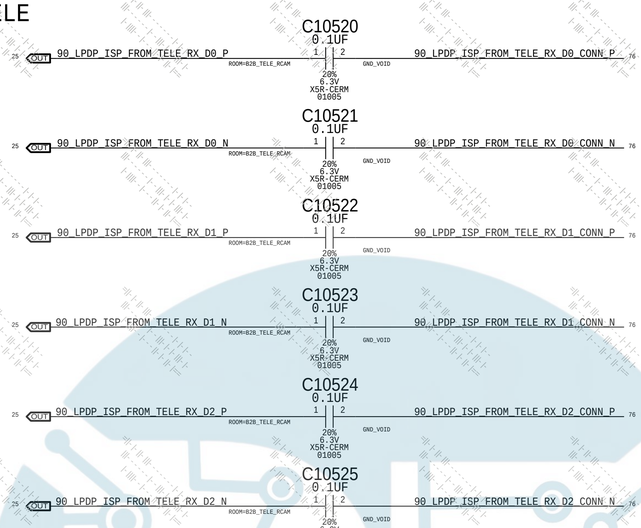


SWIDE

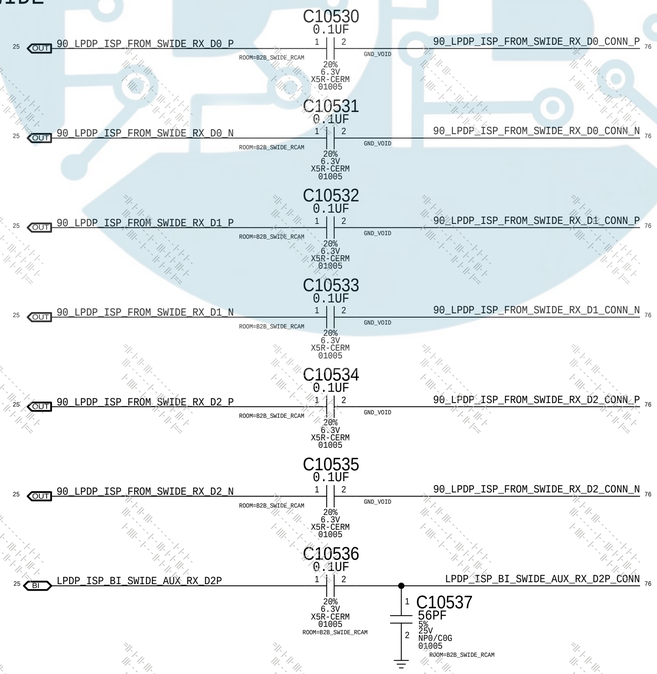


LPDP FILTERS

TELE

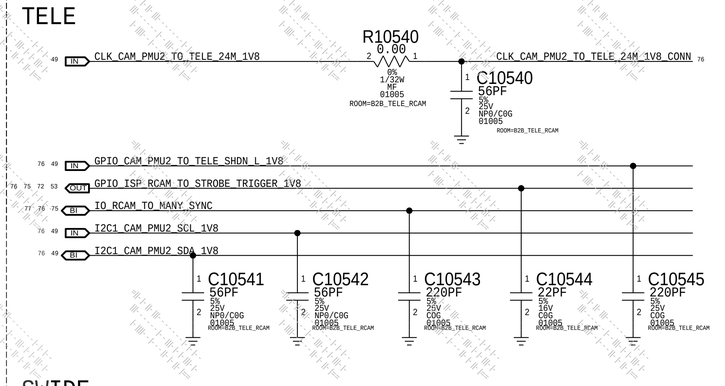


SWIDE

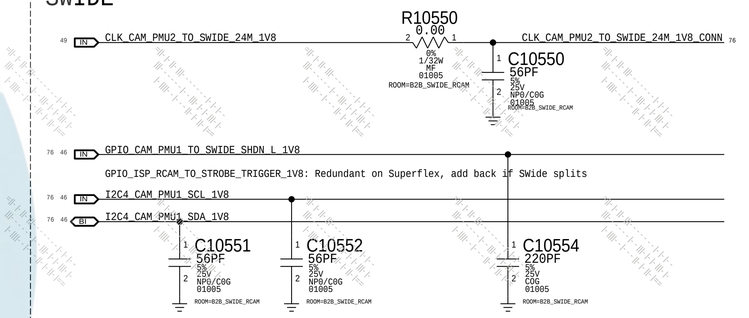


IO FILTERS

TELE



SWIDE

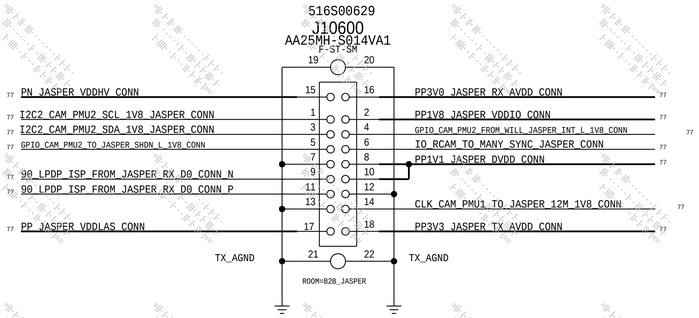


NOT SYNCING

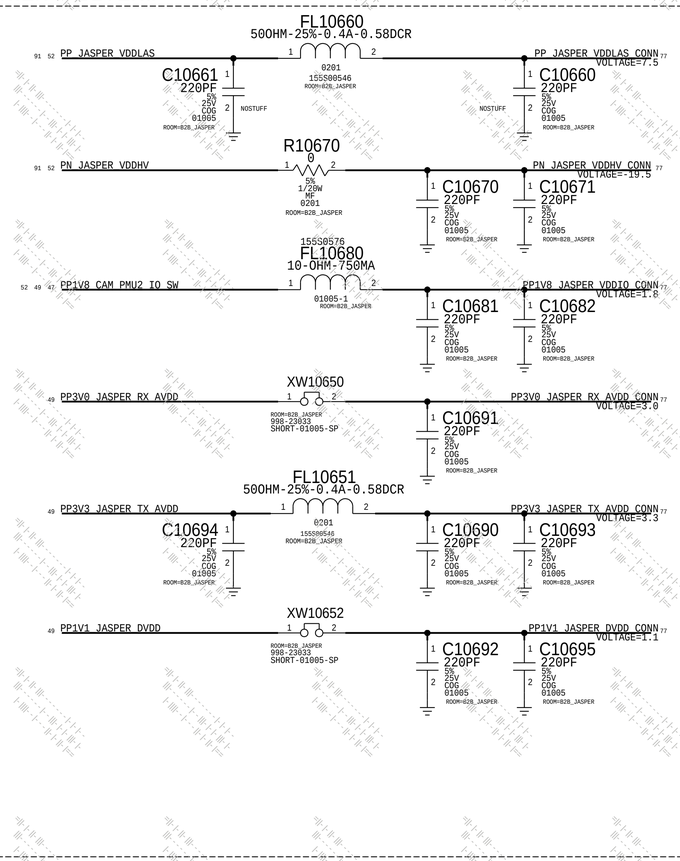
PAGE TITLE	B2B: Camera Superflex
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	105 OF 138
SHEET	76 OF 117

JASPER CAMERA B2B

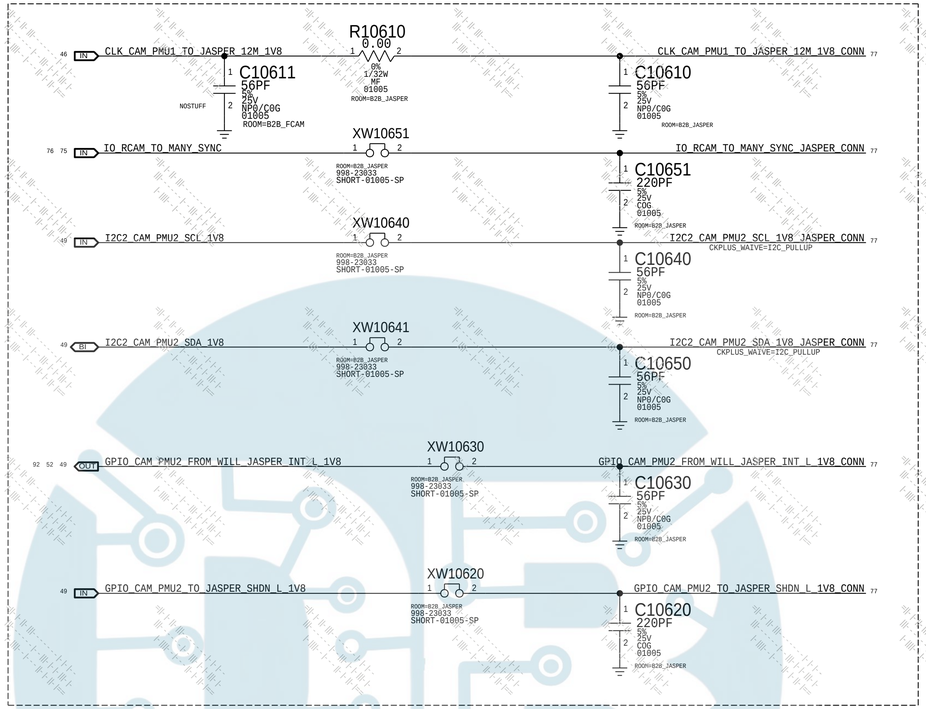
JASPER CONNECTOR



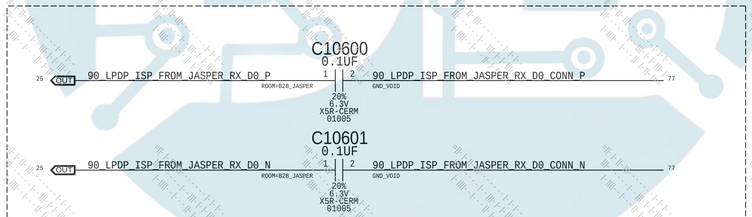
POWER FILTERS



IO FILTERS



LPDP FILTERS

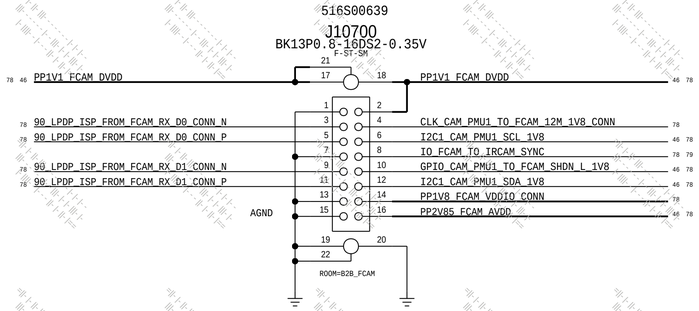


NOT SYNCING

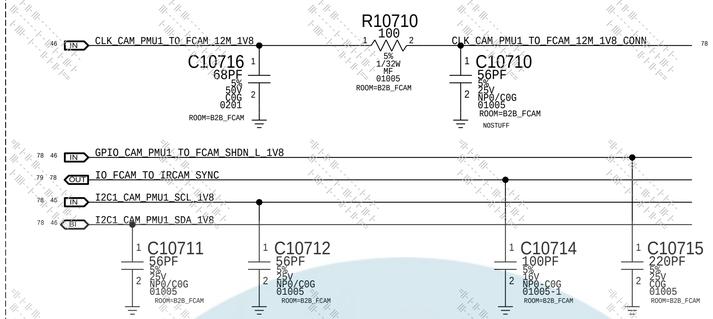
PAGE TITLE	B2B: Jasper
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	106 OF 138
SHEET	77 OF 117

FCAM B2B

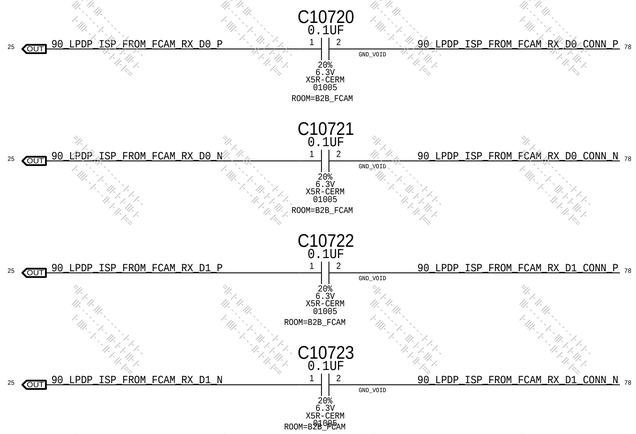
CONNECTORS



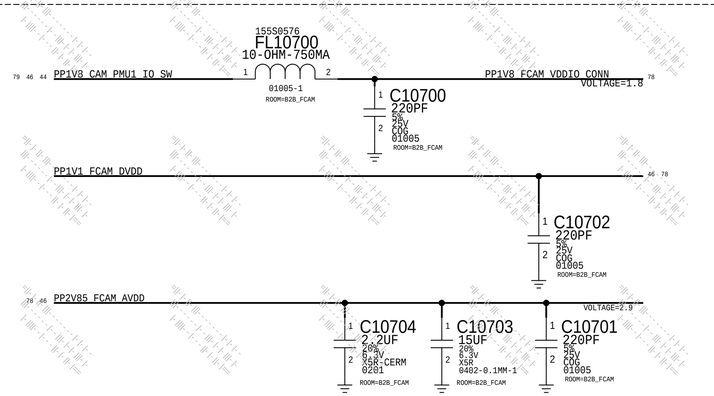
IO FILTERS



LPDP FILTERS



POWER FILTERS



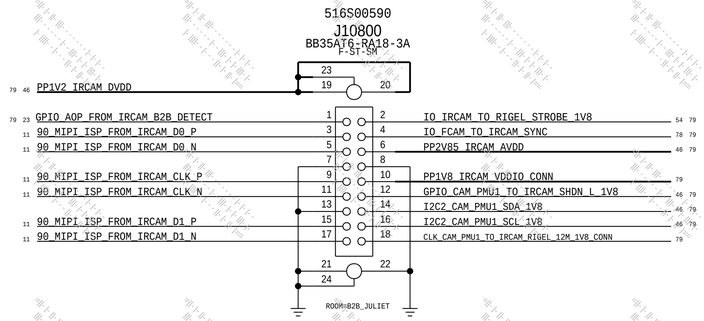
NOT SYNCING

PAGE TITLE: B2B: FCAM

DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: 1
PAGE: 107 OF 138
SHEET: 78 OF 117

JULIET B2B

CONNECTOR



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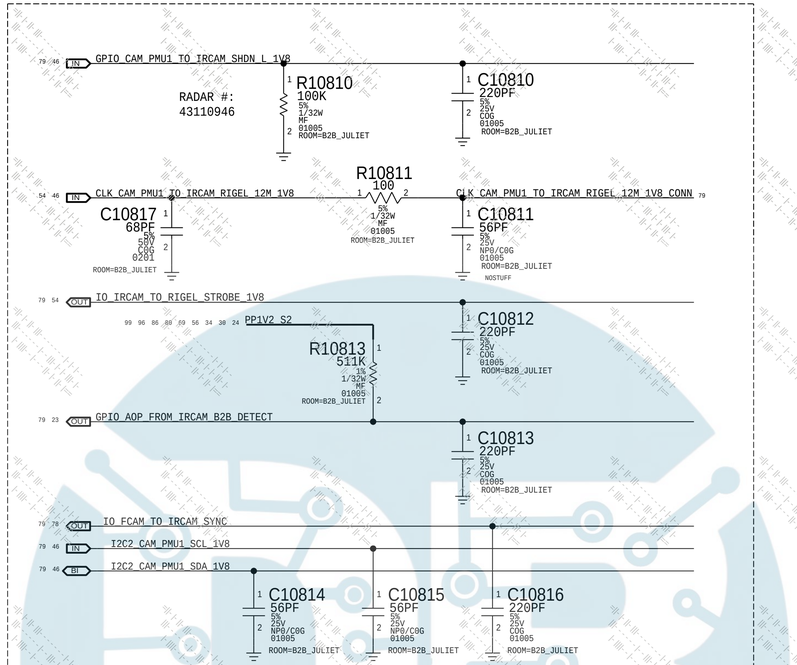
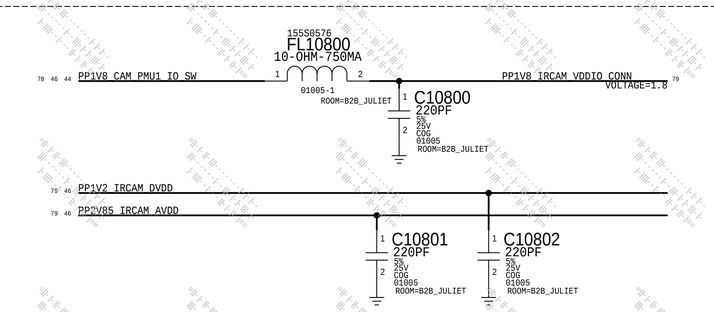


POWER FILTERS

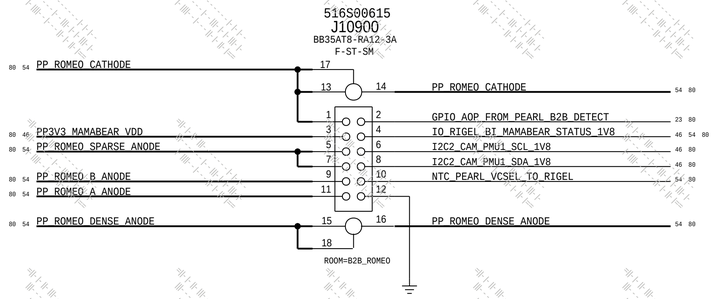


NOT SYNCING

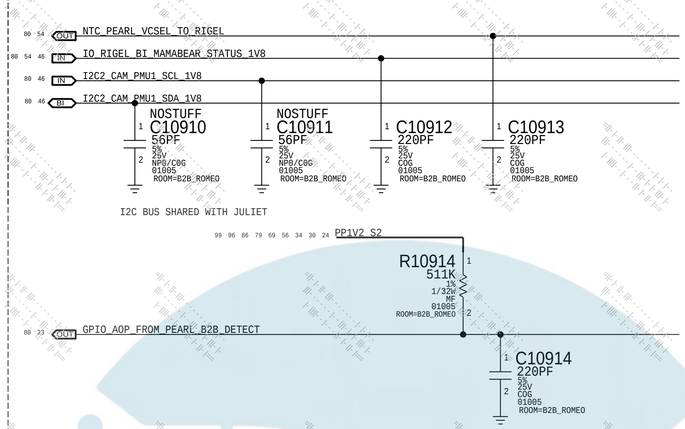
PAGE TITLE	B2B: Juliet
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	108 OF 138
SHEET	79 OF 117

ROMEO B2B

CONNECTOR

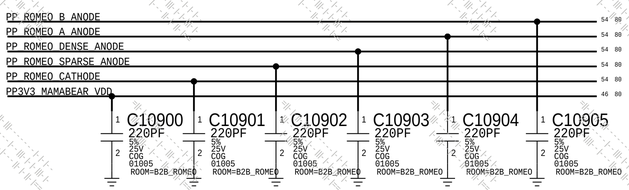


IO FILTERS



LPDP FILTERS

POWER FILTERS



NOT SYNCING

SYNC_MASTER=0.99.0 SYNC_DATE=04/03/2019

PAGE TITLE: B2B: Romeo

DRAWING NUMBER: 051-05170 SIZE: D

REVISION: 10.0.0

BRANCH: 1

PAGE: 109 OF 138

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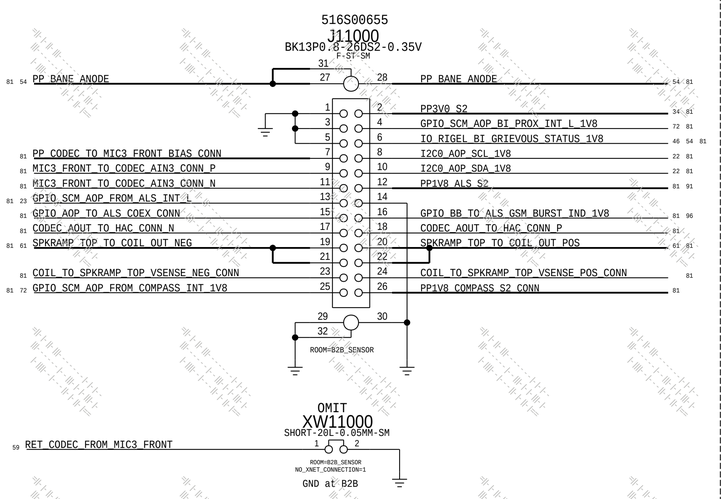
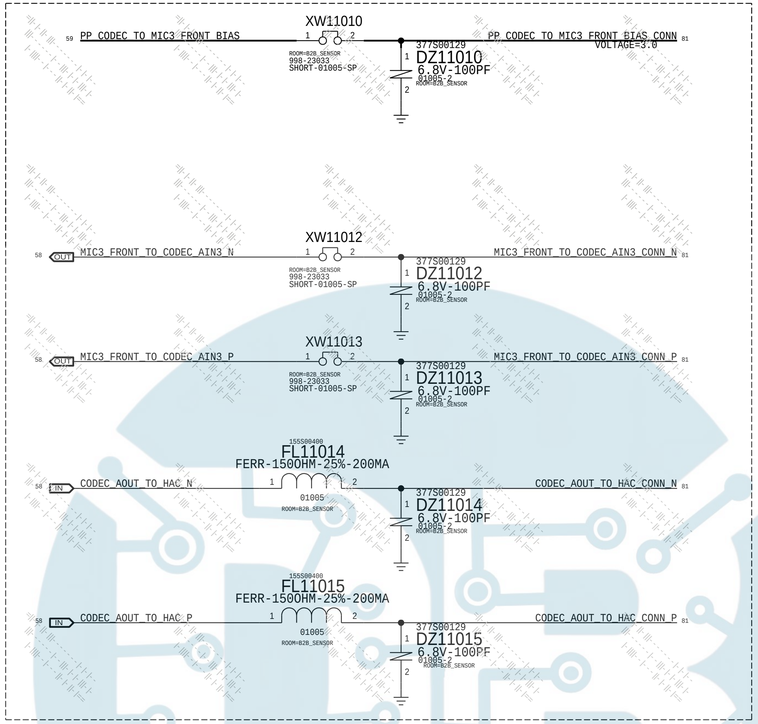
SENSOR B2B

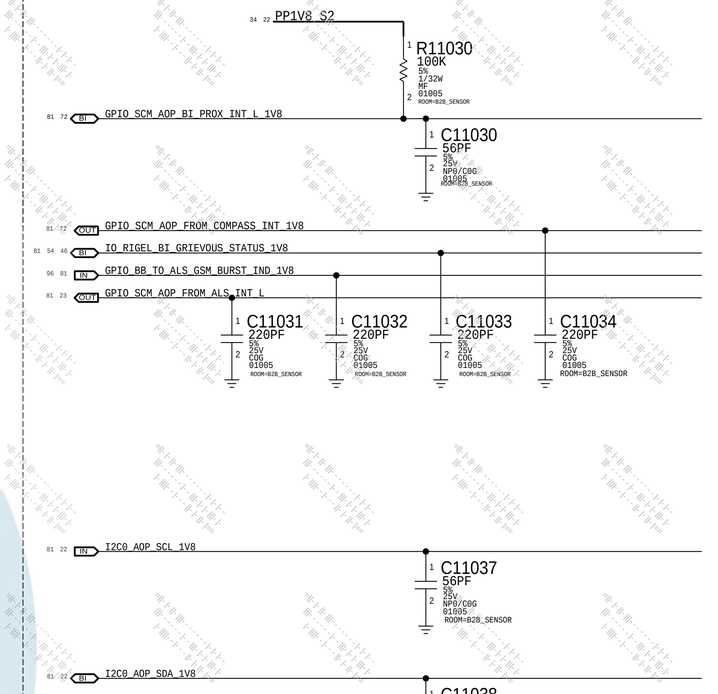
CONNECTOR



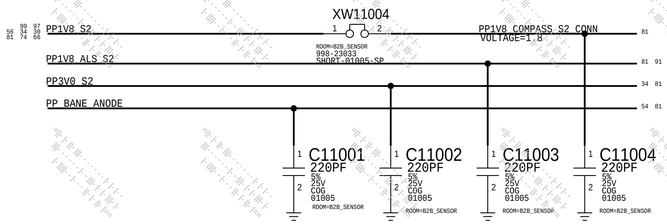
MIC3



IO FILTERS

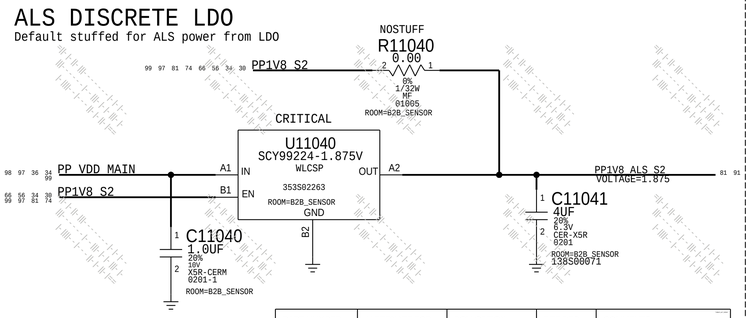


POWER FILTERS



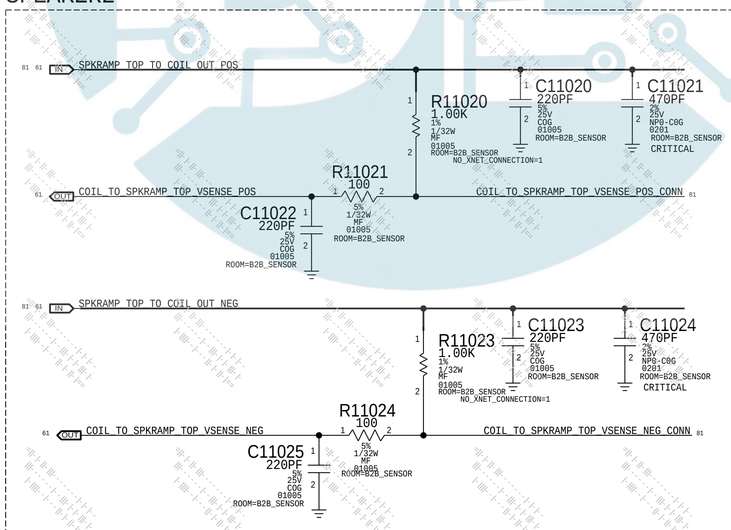
ALS DISCRETE LDO

Default stuffed for ALS power from LDO



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S00816	353S02263	?	U11040	IC,LDO,REG,1.875V,200MA

SPEAKER2

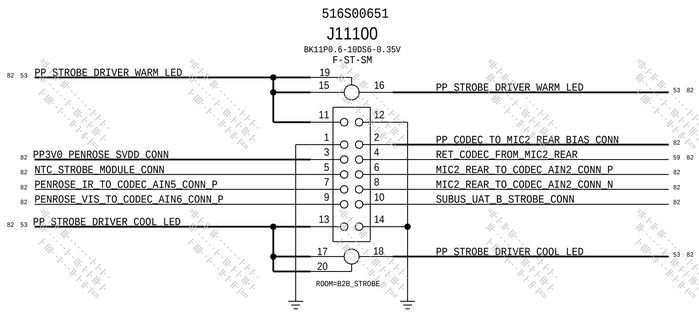


NOT SYNCING

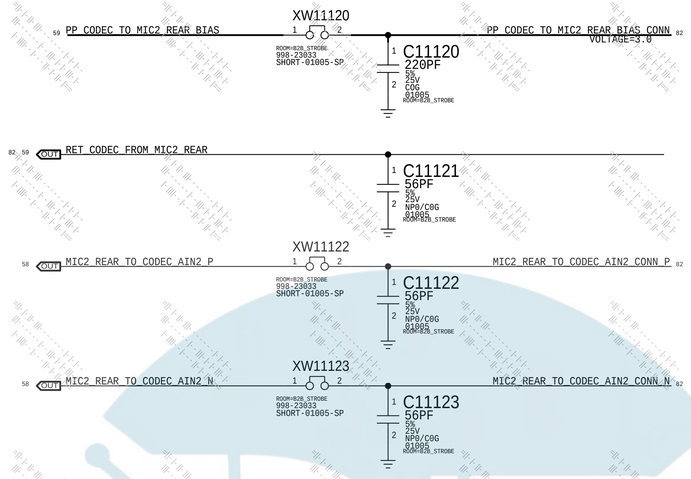
PAGE TITLE	B2B: Sensor
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	110 OF 138
SHEET	81 OF 117

STROBE B2B

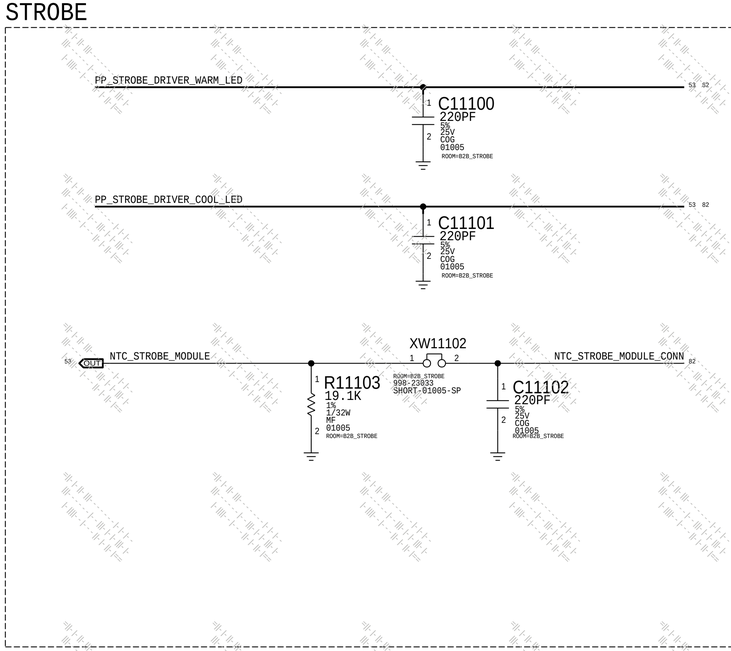
CONNECTOR



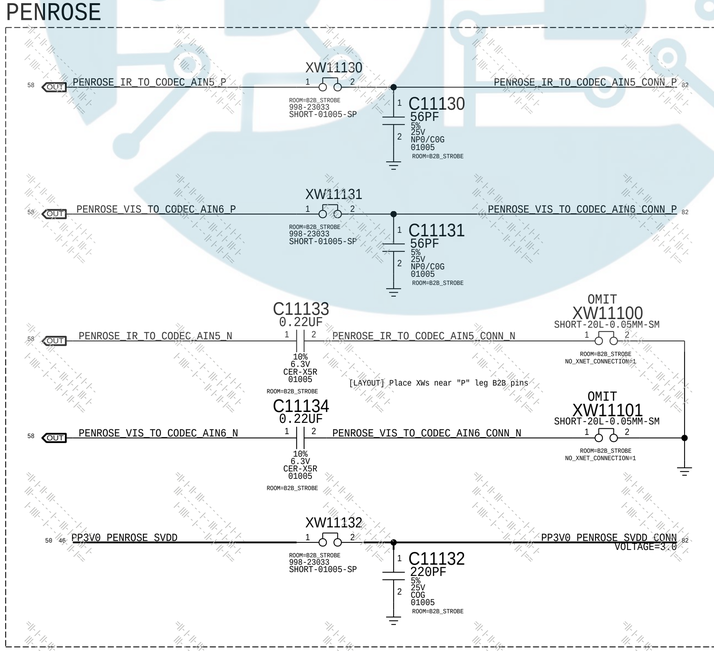
MIC2



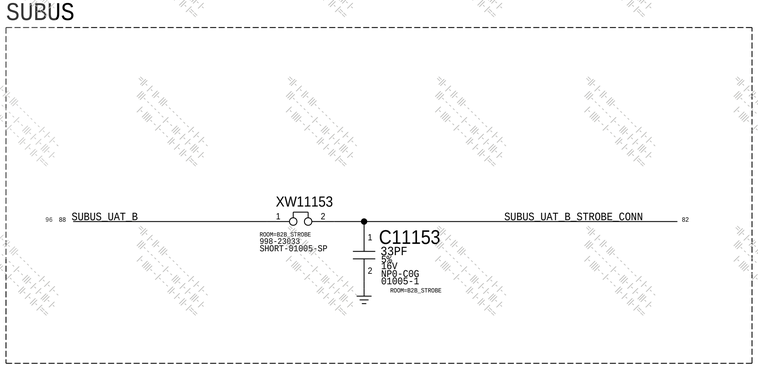
STROBE



PENROSE



SUBUS



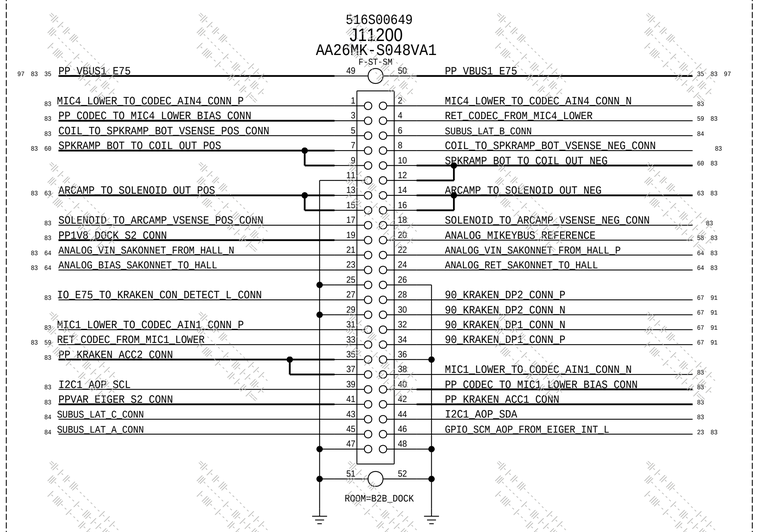
NOT SYNCING

PAGE TITLE
B2B: Strobe

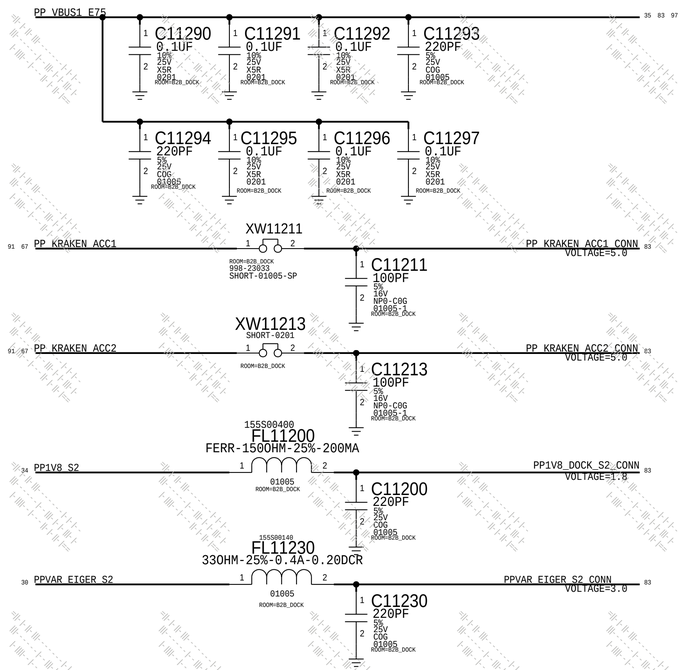
DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 111 OF 138
SHEET 82 OF 117

DOCK B2B

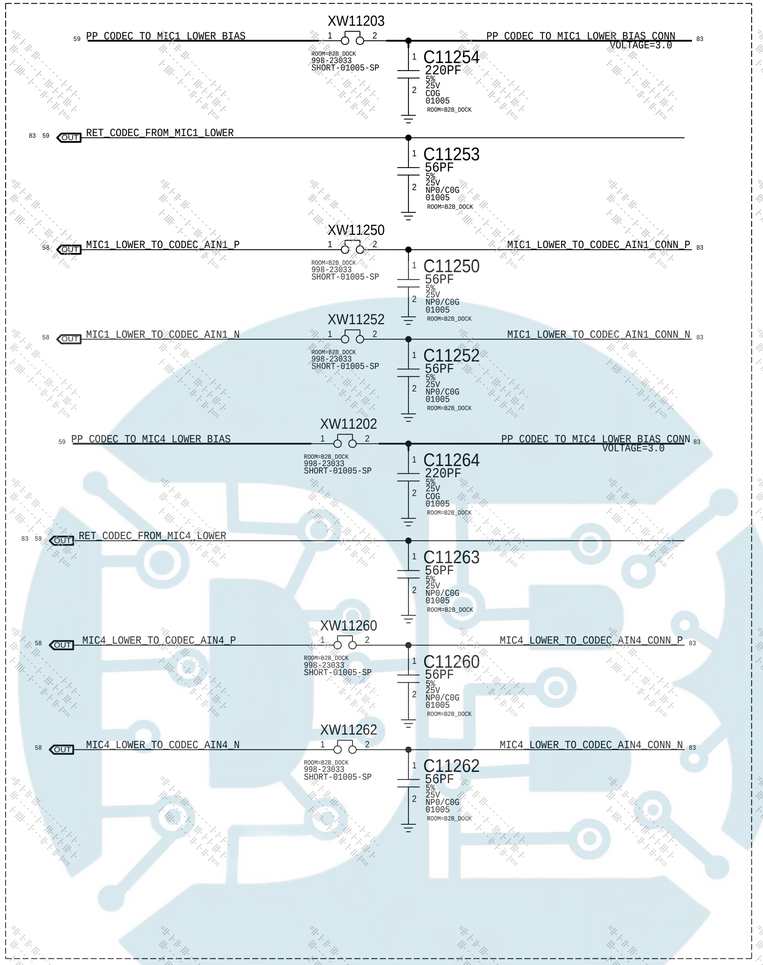
CONNECTOR



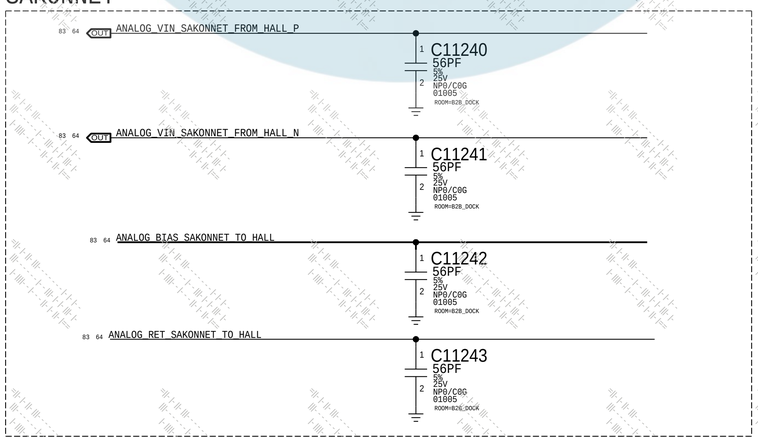
POWER FILTERS



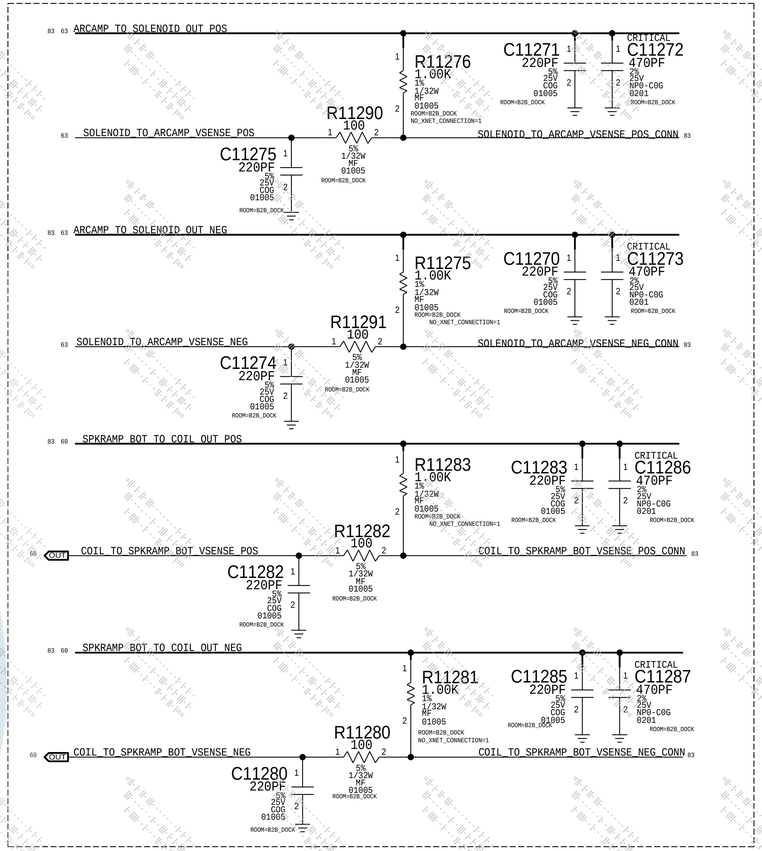
MIC1 + MIC4



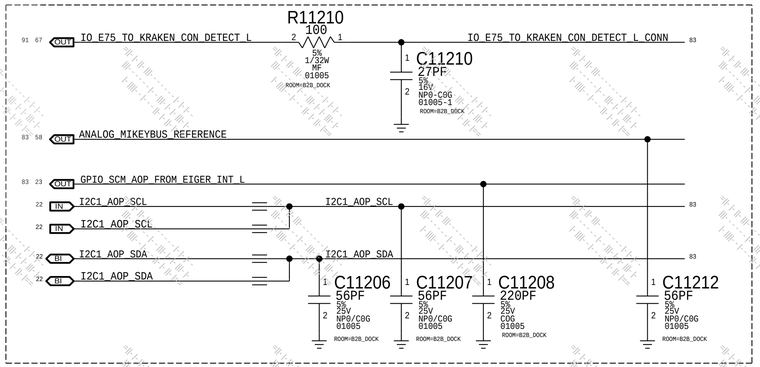
SAKONNET



ARC + BOT SPEAKER



IO FILTERS

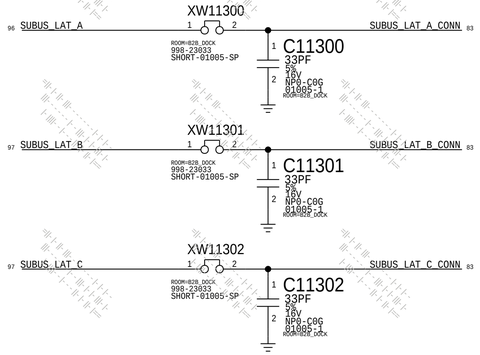


NOT SYNCING

PAGE TITLE	B2B: Dock
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	112 OF 138
SHEET	83 OF 117

DOCK B2B FILTERS (CONT)

DOCK SUBUS FILTERS



PAGE TITLE: B2B: Dock (Cont)

DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: 1
PAGE: 113 OF 138
SHEET: 84 OF 117

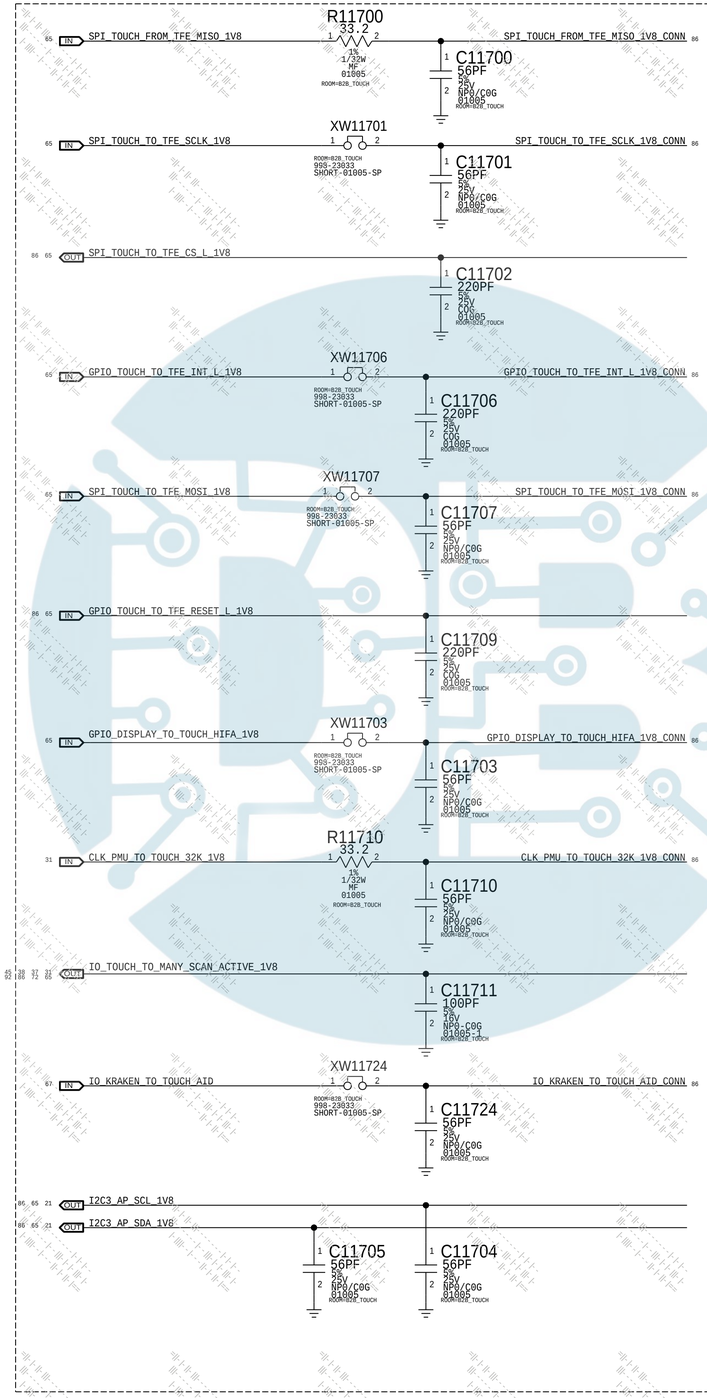
TOUCH B2B

CONNECTOR

DISPLAY/TOUCH COMBO B2B
MAINTAINED ON NEXT PAGE

POWER FILTERS

IO FILTERS

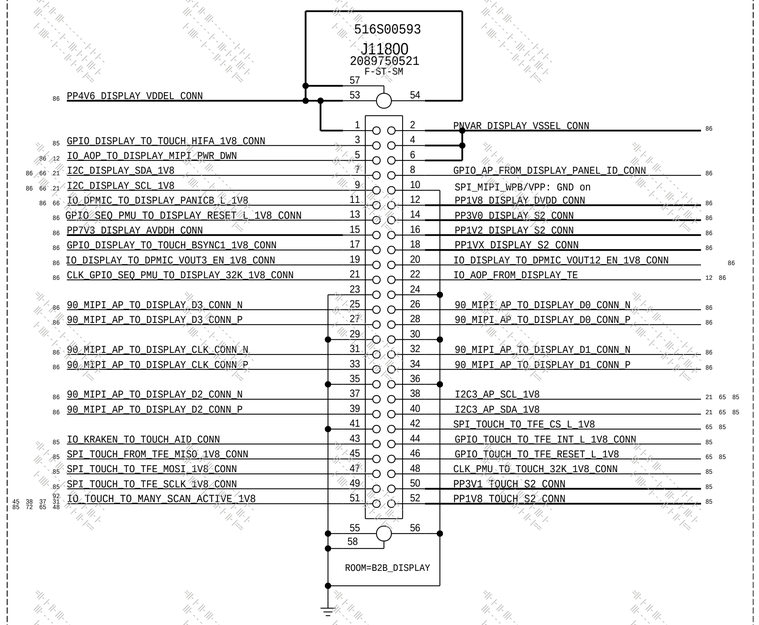


NOT SYNCING

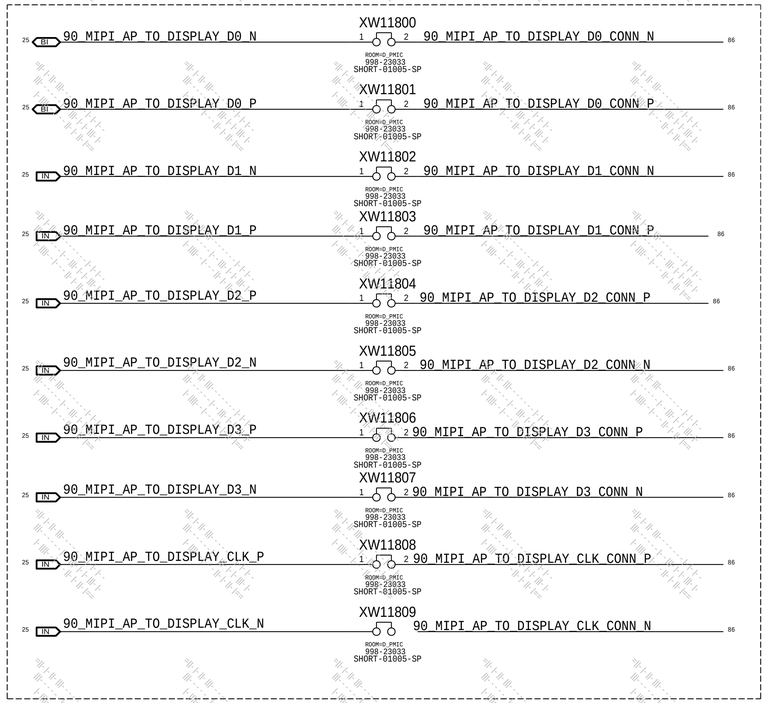
SYNC_MASTER=0.99.0	SYNC_DATE=04/03/2019
PAGE TITLE	B2B: Display/Touch Combo (1/2)
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	117 OF 138
SHEET	85 OF 117

DISPLAY B2B

CONNECTOR



MIPI FILTERS



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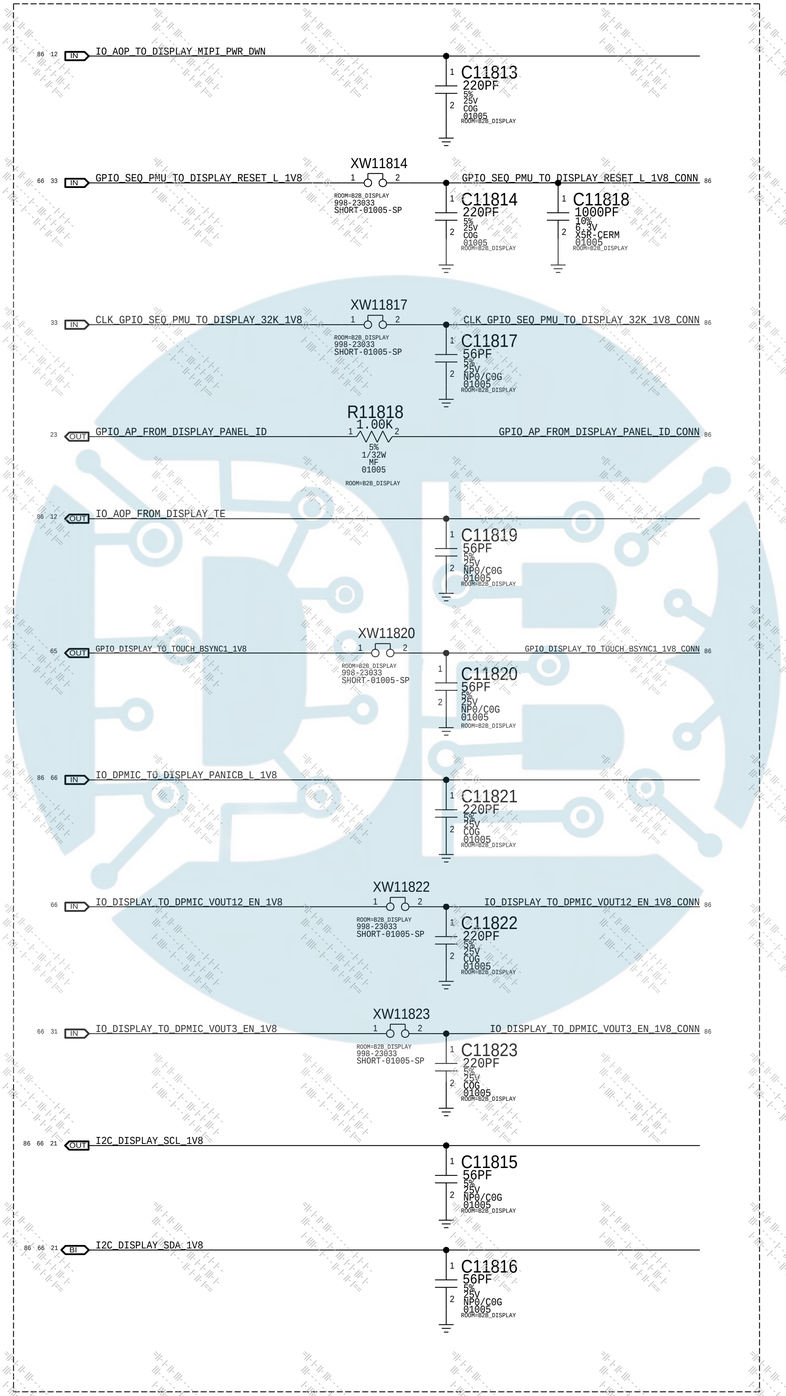

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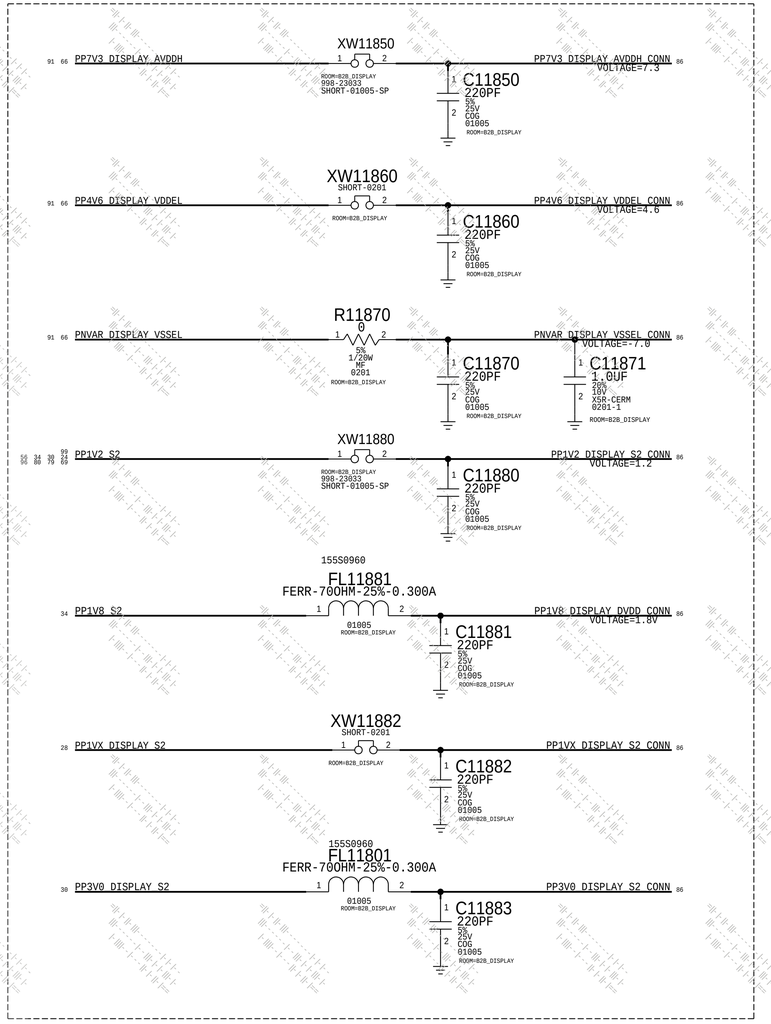

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UAT1 B2B

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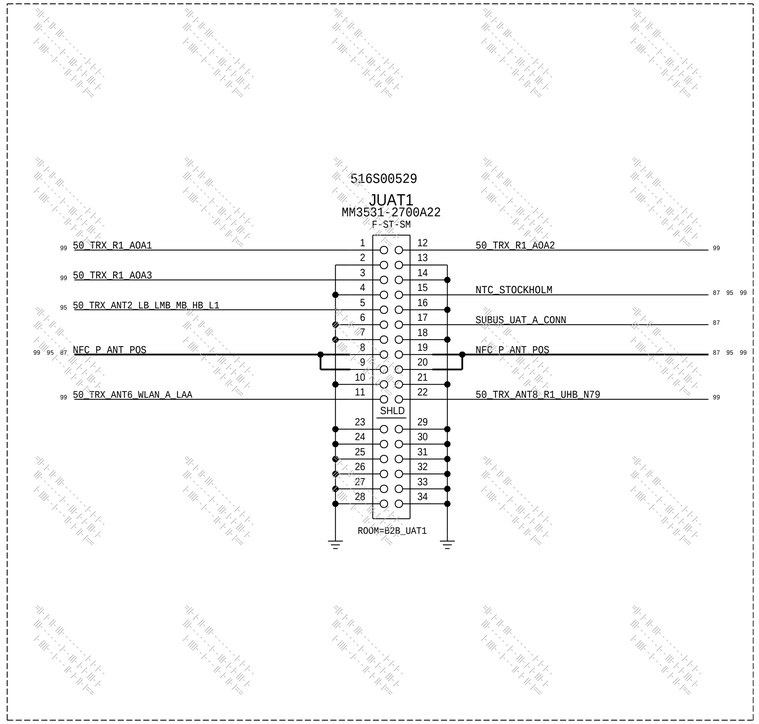

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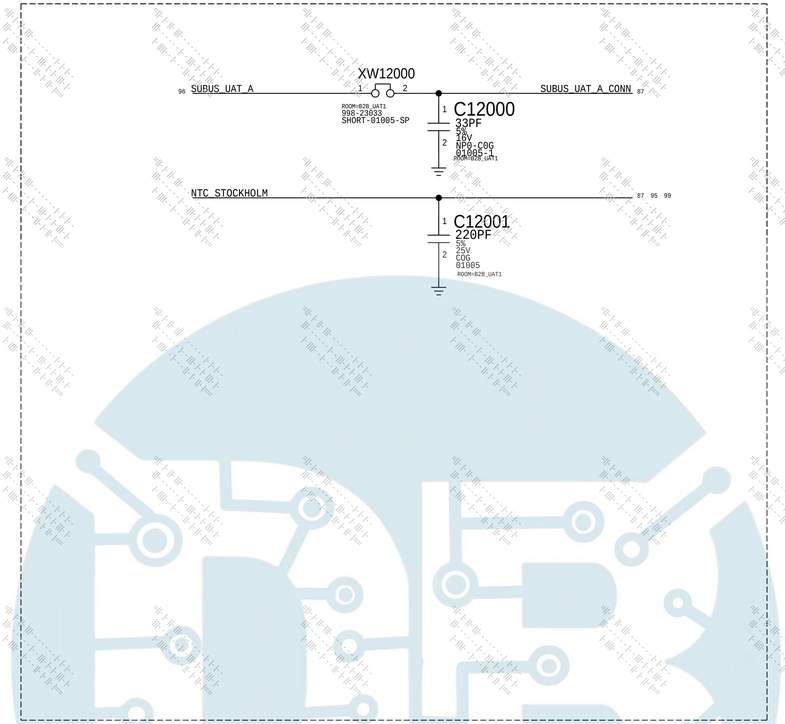

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UAT2 B2B

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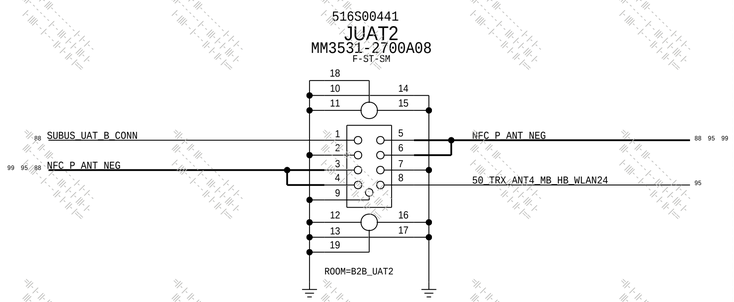

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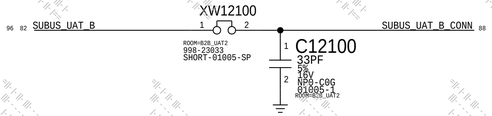

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LAT B2B

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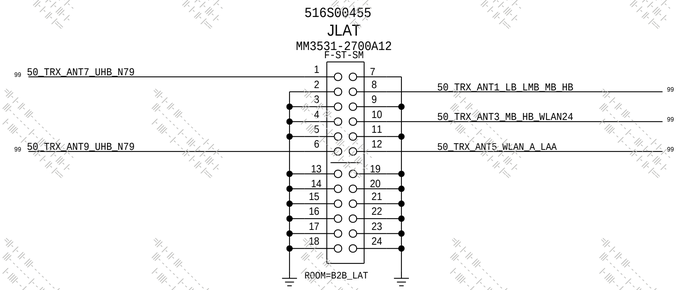

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SIM B2B

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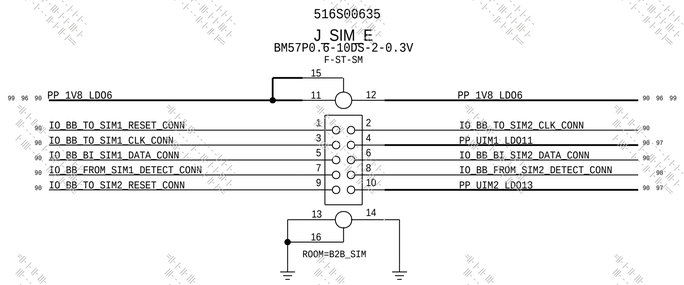

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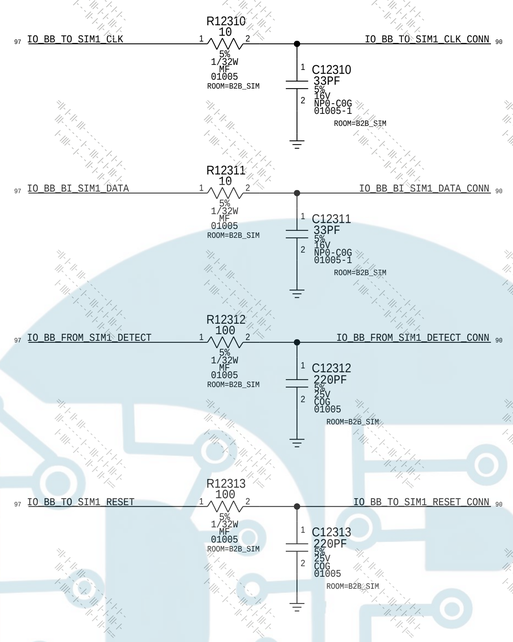

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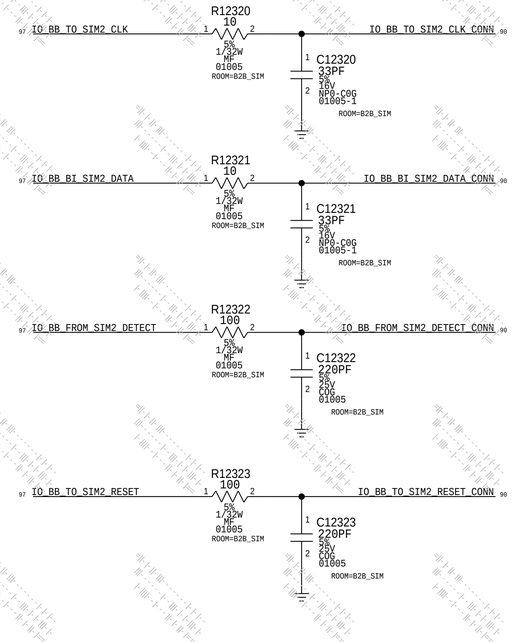
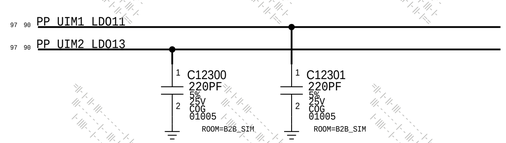


SIM POWER + DETECT



PAGE TITLE
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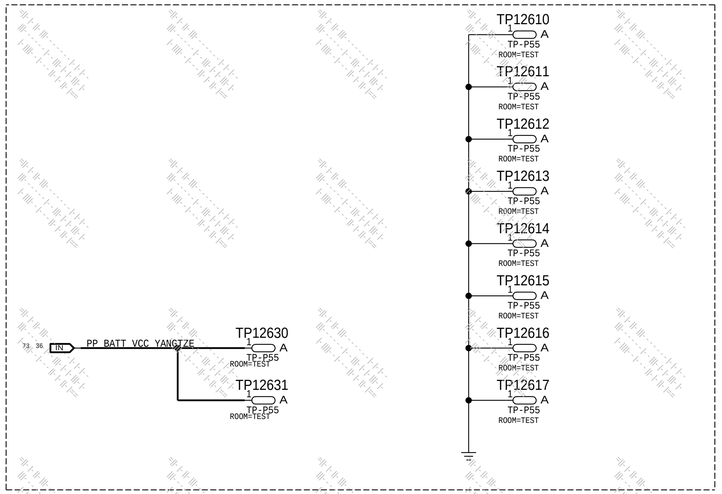
Test Points

Power + GND



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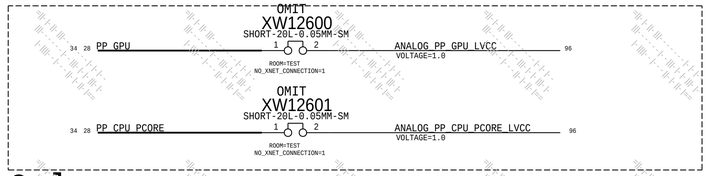
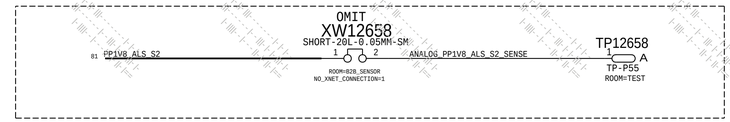


ALS Discrete LDO



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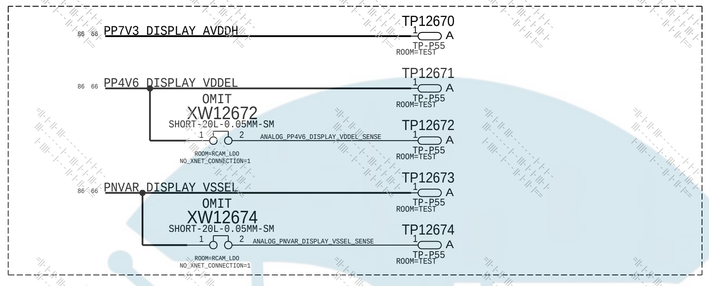

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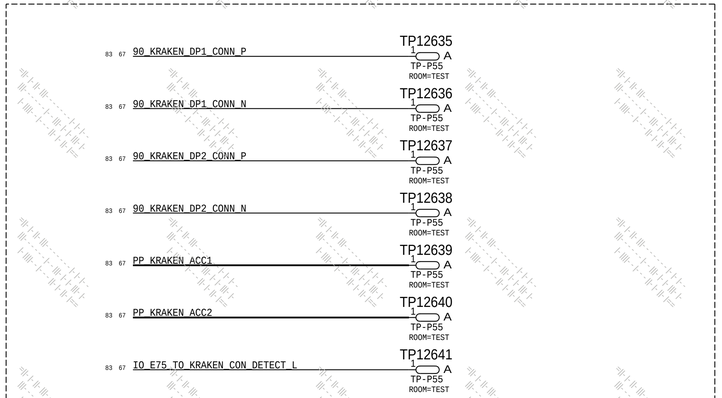

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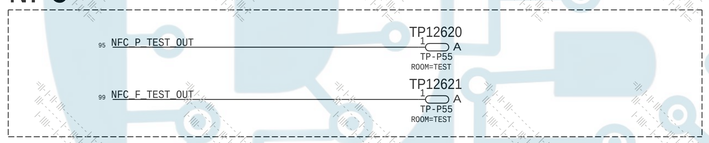
NFC



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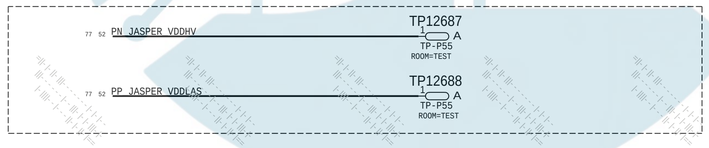
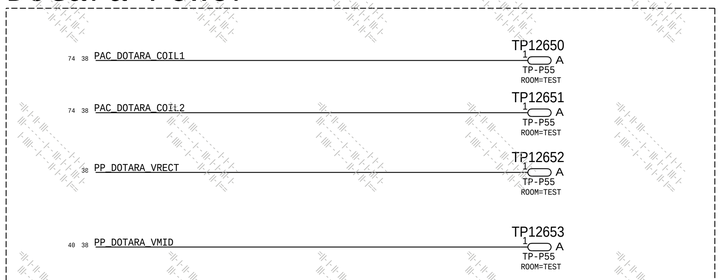


Dotara Power



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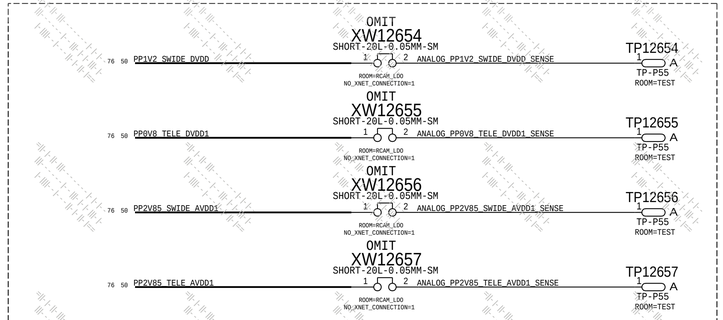

PAGE TITLE
TESTING: Test Points

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Probe Points

99	96	33	31	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	PP12800
	57	23		GPIO_SCM_AOP_FROM_JARVIS_INT	PP12801
61	60	59	15 64 63	I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK	PP12869
	59	23		GPIO_AOP_TO_CODEC_RESET_L	PP12803
	68	23		GPIO_AP_BI_CCG2B_SWDIO	PP12804
	59	23		GPIO_AP_FROM_CODEC_INT_L	PP12805
				GPIO_BOARD_ID0 (PLACE_SIDE=TOP)	PP12806
	31	25		GPIO_AP_TO_AMUX_PMU_SYNC	PP12807
	54	46	31	GPIO_CAM_PMU1_FROM_RIGEL_INT_1V8	PP12808
	54	46		GPIO_CAM_PMU1_TO_RIGEL_ENABLE_1V8	PP12809
	53	46		GPIO_CAM_PMU1_TO_STROBE_HWEN_1V8	PP12810
	68	15		GPIO_NUB_FROM_CCG2B_INT_L	PP12811
	69	15		GPIO_NUB_FROM_GECKO_IRQ_L	PP12812
	70	15		GPIO_NUB_FROM_PARROT_INT_L	PP12813
	69	15		GPIO_NUB_TO_GECKO_RESET_L	PP12814
	59	33		GPIO_PMU_FROM_CODEC_WAKE_L	PP12815
	33	31		GPIO_PMU_TO_AMUX_PMU_SUPER_TP	PP12816
	68	33		GPIO_PMU_TO_CCG2B_RESET_L	PP12817
	33	26		GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	PP12818
	34	31		GPIO_PMU_TO_SOC_DOUBLE_CLICK_DET_L	PP12819
	60	33		GPIO_S4_PMU_TO_SPKRAMP_BOT_RESET_L	PP12820
	37	33		GPIO_SEQ_PMU_TO_BOOST_EN_1V8	PP12821
	66	33		GPIO_SEQ_PMU_TO_DISPLAY_PANICB_L_1V8	PP12822
	59	15		I2S0_AOP_FROM_CODEC_ASP1_BCLK	PP12823
	59	15		I2S0_AOP_FROM_CODEC_ASP1_DIN	PP12824
	59	15		I2S0_AOP_FROM_CODEC_ASP1_LRCLK	PP12825
	59	15		I2S0_AOP_TO_CODEC_ASP1_DOUT	PP12826
	65	31		GPIO_PMU_FROM_TOUCH_LDO_EN	PP12827
	67	35		IO_KRAKEN_TO_CHARGER_VBUS1_VALID_L_1V8	PP12828
	70	67	31	IO_KRAKEN_TO_PARROT_PMU_USB_EN	PP12829
	67	15		IO_NUB_FROM_KRAKEN_DOCK_CONNECT	PP12830
	67	31		IO_PMU_FROM_KRAKEN_RESET	PP12831
	63	61	60	IO_SPKRAMP_TO_SPKRAMP_SYNC	PP12832
	68	67	35	PP_VAR_USB_RVP	PP12833
	59	24		SPI3_AP_FROM_CODEC_MISO	PP12834
	59	24		SPI3_AP_TO_CODEC_CS_L	PP12835
	59	24		SPI3_AP_TO_CODEC_MOSI	PP12836
	65	24	15	SWD_NUB_TO_PMU_TOUCH_SWCLK	PP12837
	65	15		UART2_AOP_TO_TOUCH_TXD	PP12838
	24	13		UART4_AP_FROM_KRAKEN_ACC_RXD	PP12839
	24	13		UART4_AP_TO_KRAKEN_ACC_TXD	PP12840
	65	15		UART2_AOP_FROM_TOUCH_RXD	PP12863

70	24			90_EUSB_DBG_PARROT_BI_AP_N	PP12841
70	24			90_EUSB_DBG_PARROT_BI_AP_P	PP12842
70	9			90_EUSB_PARROT_BI_AP_N	PP12843
70	9			90_EUSB_PARROT_BI_AP_P	PP12844
70	67			90_USB1_KRAKEN_BI_PARROT_N	PP12845
70	67			90_USB1_KRAKEN_BI_PARROT_P	PP12846
	24			IO_AP_FROM_PMU_SW_SHDN_L	PP12847
59	13			I2S0_AP_FROM_CODEC_ASP3_BCLK	PP12848
59	13			I2S0_AP_FROM_CODEC_ASP3_DIN	PP12849
59	13			I2S0_AP_FROM_CODEC_ASP3_LRCLK	PP12850
59	13			I2S0_AP_TO_CODEC_ASP3_DOUT	PP12851
59	13			I2S1_AP_FROM_CODEC_ASP4_BCLK	PP12852
59	13			I2S1_AP_FROM_CODEC_ASP4_DIN	PP12853
59	13			I2S1_AP_FROM_CODEC_ASP4_LRCLK	PP12854
59	13			I2S1_AP_TO_CODEC_ASP4_DOUT	PP12855
26	9			IO_AP_TO_NAND_FW_STRAP	PP12856
67	15			IO_NUB_FROM_KRAKEN_INT	PP12857
34	33	31	35	GPIO_PMU_FROM_CHARGER_VBUS_DET_INT_L_1V8	PP12858
61	58			PDM_OUT1_CODEC_TO_SPKRAMP_TOP_CLK	PP12859
61	58			PDM_OUT1_CODEC_TO_SPKRAMP_TOP_DATA	PP12860
24	13			UART0_AP_FROM_KRAKEN_DEBUG_RXD	PP12861
24	13			UART0_AP_TO_KRAKEN_DEBUG_TXD	PP12862
67	15			SWD_DOCK_TO_AP_SWCLK	PP12864
67	15			SWD_DOCK_BI_AP_SWDIO	PP12865

NAND

26	9			IN SWD_AP_BI_NAND_SWDIO	PP12866
26	24	7		IN SPI0_AP_FROM_SSE_MISO_BOOT_CONFIG2	PP12867
26	9			IN IO_AP_TO_NAND_RESET_L	PP12868
26				IN ANALOG_NAND_ANI1_VREF	PP12870
26				IN ANALOG_NAND_ANI0_VREF	PP12871
31	26			IN IO_PMU_TO_NAND_SYSTEM_ALIVE	PP12872

Buck3 Load Testing

99	96	34	28	PP1V8_S4 (PLACE_SIDE=TOP)	PP12894

9				IO_SOC_DFU_STATUS = IO_SOC_DFU_STATUS (MAKE_BASE=TRUE)	PP12873
9				IO_PAD_MTR_ANALOG_TEST_P = IO_PAD_MTR_ANALOG_TEST_P (MAKE_BASE=TRUE)	PP12874
9				IO_PAD_MTR_ANALOG_TEST_N = IO_PAD_MTR_ANALOG_TEST_N (MAKE_BASE=TRUE)	PP12875

Miscellaneous

68	23			IN GPIO_AP_TO_CCG2B_SWCLK	PP12876

Parrot

70				IN GPIO0_PARROT	PP12877
70				IN GPIO1_PARROT	PP12878

Bump Sense

28	17			IN ANALOG_PCPU_SENSE_P	PP12879
20				IN ANALOG_PCPU_SENSE_N	PP12880
17				IN ANALOG_GPU_SENSE_P	PP12881
20				IN ANALOG_GPU_SENSE_N	PP12882
17				IN ANALOG_SOC_SENSE_P	PP12883
20				IN ANALOG_SOC_SENSE_N	PP12884
19				IN ANALOG_DCS_SENSE_SE	PP12885
20				IN ANALOG_DDR_SENSE_SE	PP12886
17				IN ANALOG_ECPU_SENSE_SE	PP12887
19				IN ANALOG_VDDQL_SENSE_SE	PP12888

SOC Debug

24	15			IN IO_AON_TO_AP_XTAL_CFSB	PP12889
24	9			IN CLK_AP_TO_PMU_TST_CLKOUT	PP12890
24				IN IO_AP_FROM_PMU_PRE_UVLO_L	PP12891

Dotara

38				GPIO_DOTARA_SWD_1V8	PP12892
38	31			DOTARA_SUPER_GPIO_1V8 (MAKE_BASE=TRUE)	PP12893
38				I2C_SDA_DOTARA_1V8 (CKPLUS_WAIVE=I2C_PULLUP)	PP12895
38				I2C_SCL_DOTARA_1V8 (CKPLUS_WAIVE=I2C_PULLUP)	PP12896
38				IO_DOTARA_DFT1_1V8	PP12897
38				IO_DOTARA_DFT2_1V8	PP12898
40	38			IO_DOTARA_TO_DOMBRA_EN_1V8	PP12899
38	33			GPIO_SEQ_PMU_TO_DOTARA_EN_EXT_1V8	PP128A0
85	72	65	48 45 38 37 31 86	IO_TOUCH_TO_MANY_SCAN_ACTIVE_1V8	PP128A1
38				IO_DOTARA_MTP_WREN_1V8	PP128A2
40	38			IO_DOTARA_TO_DOMBRA_FPWM_1V8	PP128A3
38				PP1V8_DOTARA_LDO	PP128A4
95	38			CLK_BBPMU_TO_DOTARA_38M4 (PLACE_SIDE=TOP)	PP12802

TOUCH

65	25			SPI2_AP_TO_TOUCH_CS_L	PP128C0
65	25			SPI2_AP_TO_TOUCH_SCLK	PP128C1
65	25			SPI2_AP_FROM_TOUCH_MISO	PP128C2
65	25			SPI2_AP_TO_TOUCH_MOSI	PP128C3

PMU

33	31	15		IN CLK_PMU_TO_AOP_32K	PP128A5
34	33	31		IN IO_PMU_TO_SOC_KRAKEN_ACTIVE_READY	PP128A6
31	15			IN IO_SOC_TO_PMU_WDOG_RESET	PP128A7
24	9			IN IO_SOC_TO_PMU_SOCHOT_RESET_L	PP128A8
34	15			IN SWD_NUB_BI_PMU_SWDIO	PP128A9

Adams

52	49			IN GPIO_CAM_PMU2_TO_WILL_EN_1V8	PP128B2
50	46			IN GPIO_CAM_PMU1_TO_SWIDE_LDO_EN_1V8	PP128B3
50	49			IN GPIO_CAM_PMU2_TO_TELE_LDO_EN_1V8	PP128B4
77	52	49		IN GPIO_CAM_PMU2_FROM_WILL_JASPER_INT_L_1V8	PP128B5
45	12			IN SPMI_ISP_TO_CAM_PMU1_CLK	PP128B6
45	12			IN SPMI_ISP_BI_CAM_PMU1_DATA	PP128B7
48	12			IN SPMI_ISP_TO_CAM_PMU2_CLK	PP128B8
48	12			IN SPMI_ISP_BI_CAM_PMU2_DATA	PP128B9

PAGE TITLE: TESTING: Probe Points

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J INT BOT
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SYM 1 OF 4

998-21759
OMIT

95	GND	1	IO1	IO91	91	IO_BT_TO_R1_WAKE	95
95	GND	2	IO2	IO92	92	GPIO_R1_TO_BB_LAA_SW_CTRL	95
95	GND	3	IO3	IO93	93	GND	95
95	GND	4	IO4	IO94	94	GPIO_AP_FROM_WLAN_TIME_SYNC	95
95	NFC_P_ANT_NEG	5	IO5	IO95	95	GPIO_BB_TO_R1_COEX	95
95	GND	6	IO6	IO96	96	GND	95
95	NFC_P_ANT_NEG	7	IO7	IO97	97	GND	95
95	GND	8	IO8	IO98	98	IO_BT_TO_R1_TIME_SYNC	95
95	NFC_P_ANT_NEG	9	IO9	IO99	99	GPIO_R1_TO_WLAN_COEX	95
95	GND	10	IO10	IO100	100	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	95
95	NFC_P_ANT_NEG	11	IO11	IO101	101	GND	95
95	GPIO_NFC_F_NFC_P_SYNC2	12	IO12	IO102	102	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	95
95	GND	13	IO13	IO103	103	GPIO_WLAN_TO_R1_COEX	95
95	GND	14	IO14	IO104	104	GND	95
95	50_TRX_ANT4_MB_HB_WLAN24	15	IO15	IO105	105	GND	95
95	GND	16	IO16	IO106	106	NFC_P_ANT_POS	95
95	GND	17	IO17	IO107	107	GND	95
95	PCIE_GP1_AP_TO_WLAN_PERST_L	18	IO18	IO108	108	NFC_P_ANT_POS	95
95	GPIO_AP_TO_BB_PEAK_PWR_IND	19	IO19	IO109	109	GND	95
95	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	20	IO20	IO110	110	NFC_P_ANT_POS	95
95	SWD_AP_BI_BB_SWDIO	21	IO21	IO111	111	GND	95
95	NTC_STOCKHOLM	22	IO22	IO112	112	NFC_P_ANT_POS	95
95	GPIO_R1_TO_BB_CH9_COEX	23	IO23	IO113	113	GND	95
95	GPIO_NFC_F_NFC_P_SYNC1	24	IO24	IO114	114	CLK_BBPMU_TO_DOTARA_38M4	95
95	GND	25	IO25	IO115	115	GND	95
95	GND	26	IO26	IO116	116	GND	95
95	PP1V2_S4	27	IO27	IO117	117	GND	95
95	GND	28	IO28	IO118	118	GND	95
95	I2C_R1_TO_NFC_SCL	29	IO29	IO119	119	50_WLAN_A_C0_TXRX_FEM_M	95
95	GND	30	IO30	IO120	120	GND	95
95	I2C_R1_TO_NFC_SDA	31	IO31	IO121	121	GND	95
95	GND	32	IO32	IO122	122	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	95
95	NFC_P_TEST_OUT	33	IO33	IO123	123	GND	95
95	GND	34	IO34	IO124	124	GND	95
95	GND	35	IO35	IO125	125	50_TRX_ANT2_LB_LMB_MB_HB_L1	95
95	GND	36	IO36	IO126	126	GND	95
95	GND	37	IO37	IO127	127	GND	95
95	GND	38	IO38	IO128	128	50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M	95
95	GND	39	IO39	IO129	129	GND	95
95	GND	40	IO40	IO130	130	GND	95
95	GND	41	IO41	IO131	131	50_LAA_RX_XCVR_DRX10	95
95	GND	42	IO42	IO132	132	GND	95
95	GND	43	IO43	IO133	133	GND	95
95	GND	44	IO44	IO134	134	GND	95
95	GND	45	IO45	IO135	135	IO_TOUCH_TO_MANY_SCAN_ACTIVE	95
95	GND	46	IO46	IO136	136	GND	95
95	GND	47	IO47	IO137	137	GND	95
95	GND	48	IO48	IO138	138	GND	95
95	GND	49	IO49	IO139	139	GPIO_CANARY_1B_TO_1C	95
95	GND	50	IO50	IO140	140	GND	95
95	GND	51	IO51	IO141	141	GND	95
95	GND	52	IO52	IO142	142	GND	95
95	GND	53	IO53	IO143	143	GND	95
95	GND	54	IO54	IO144	144	GND	95
95	GND	55	IO55	IO145	145	GND	95
95	GND	56	IO56	IO146	146	GND	95
95	GND	57	IO57				
95	GND	58	IO58				
95	GND	59	IO59	IO149	149	GND	95
95	GND	60	IO60	IO150	150	GND	95
95	GND	61	IO61	IO151	151	GND	95
95	GND	62	IO62	IO152	152	GND	95
95	GND	63	IO63	IO153	153	GND	95
95	GND	64	IO64	IO154	154	GND	95
95	GND	65	IO65	IO155	155	GND	95
95	GND	66	IO66	IO156	156	GND	95
95	GND	67	IO67	IO157	157	GND	95
95	GND	68	IO68	IO158	158	GND	95
95	GND	69	IO69	IO159	159	GND	95
95	GND	70	IO70	IO160	160	GND	95
95	GND	71	IO71	IO161	161	GND	95
95	GND	72	IO72	IO162	162	GND	95
95	GND	73	IO73	IO163	163	GND	95
95	GND	74	IO74	IO164	164	GND	95
95	GND	75	IO75	IO165	165	GND	95
95	GND	76	IO76	IO166	166	GND	95
95	GND	77	IO77	IO167	167	GND	95
95	GND	78	IO78	IO168	168	GND	95
95	GND	79	IO79	IO169	169	GND	95
95	GND	80	IO80	IO170	170	GND	95
95	GND	81	IO81	IO171	171	GND	95
95	GND	82	IO82	IO172	172	GPIO_CANARY_1B_TO_1C	95
95	GND	83	IO83	IO173	173	GND	95
95	GND	84	IO84	IO174	174	GND	95
95	GND	85	IO85	IO175	175	GND	95
95	GPIO_BB_TO_R1_CH9_REQ	86	IO86	IO176	176	SHIELD_RFFE5_SCLK_SDR	95
95	GND	87	IO87	IO177	177	GND	95
95	SWD_AP_TO_MANY_SWCLK	88	IO88	IO178	178	SHIELD_RFFE5_SDATA_SDR	95
95	GND	89	IO89	IO179	179	GND	95
95	UAT_TUNER_TO_R1_STATE	90	IO90	IO180	180	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	95

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96	GPIO_AP_CANARY1	181	IO181	IO271	271	GPIO_S4_PMU_TO_WLAN_REG_ON	96
96	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	182	IO182	IO272	272	GND	96
96	GND	183	IO183	IO273	273	GND	96
96	CLK_BBPMU_TO_NFC_38M	184	IO184	IO274	274	GPIO_PMU_FROM_WLAN_HOST_WAKE	96
96	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	185	IO185	IO275	275	GND	96
96	GND	186	IO186	IO276	276	PP1V8_S4	96
96	GND	187	IO187	IO277	277	PP_1V8_LDO6	96
96	I2S2_AP_TO_BB_DOUT	188	IO188	IO278	278	GND	96
96	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	189	IO189	IO279	279	PP_APT_L_PA	96
96	I2S2_AP_FROM_BB_DIN	190	IO190	IO280	280	GND	96
96	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	191	IO191	IO281	281	PP_APT_L_PA	96
96	I2S2_AP_FROM_BB_BCLK	192	IO192	IO282	282	IO_TOUCH_TO_MANY_SCAN_ACTIVE	96
96	GND	193	IO193	IO283	283	GND	96
96	I2S2_AP_FROM_BB_LRCLK	194	IO194	IO284	284	GND	96
96	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	195	IO195	IO285	285	SHIELD_ETDAC_QET1_N	96
96	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	196	IO196	IO286	286	GND	96
96	GPIO_NFC_TO_BBPMU_CLK_EN	197	IO197	IO287	287	SHIELD_ETDAC_QET1_P	96
96	GND	198	IO198	IO288	288	GND	96
96	GND	199	IO199	IO289	289	SUBUS_LAT_A	96
96	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	200	IO200	IO290	290	GND	96
96	GND	201	IO201	IO291	291	SHIELD_RFFE8_SCLK_SDR	96
96	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	202	IO202	IO292	292	GND	96
96	GND	203	IO203	IO293	293	SHIELD_RFFE8_SDATA_SDR	96
96	GND	204	IO204	IO294	294	GND	96
96	GND	205	IO205	IO295	295	GND	96
96	90_PCIE_GP2_AP_TO_BB_REFCLK_N	206	IO206	IO296	296	GND	96
96	GND	207	IO207	IO297	297	GND	96
96	90_PCIE_GP2_AP_TO_BB_REFCLK_P	208	IO208	IO298	298	GND	96
96	GND	209	IO209	IO299	299	GND	96
96	GND	210	IO210	IO300	300	GND	96
96	GND	211	IO211	IO301	301	GND	96
96	GND	212	IO212	IO302	302	GND	96
96	GND	213	IO213	IO303	303	GND	96
96	GND	214	IO214	IO304	304	GND	96
96	GND	215	IO215	IO305	305	GND	96
96	GND	216	IO216	IO306	306	50_RX_XCVR_PRX14_N79_RX_OUT1	96
96	GND	217	IO217	IO307	307	GND	96
96	GND	218	IO218	IO308	308	GND	96
96	GND	219	IO219	IO309	309	50_RX_XCVR_PRX16_UHB_RX_OUT1	96
96	GND	220	IO220	IO310	310	GND	96
96	GND	221	IO221	IO311	311	GND	96
96	GND	222	IO222	IO312	312	50_TRX_UHB_PAD_PORTB_TX_M	96
96	90_PCIE_GP1_AP_FROM_WLAN_RX_N	223	IO223	IO313	313	GND	96
96	GND	224	IO224	IO314	314	GND	96
96	90_PCIE_GP1_AP_FROM_WLAN_RX_P	225	IO225	IO315	315	50_TRX_UHB_PAD_N79_PORTB_TX_M	96
96	GND	226	IO226	IO316	316	GND	96
96	GND	227	IO227	IO317	317	GND	96
96	GND	228	IO228	IO318	318	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	96
96	90_PCIE_GP1_AP_TO_WLAN_TX_P	229	IO229	IO319	319	GND	96
96	GND	230	IO230	IO320	320	GND	96
96	90_PCIE_GP1_AP_TO_WLAN_TX_N	231	IO231	IO321	321	50_RX_XCVR_PRX15_N79_RX_OUT2	96
96	GND	232	IO232	IO322	322	GND	96
96	GND	233	IO233	IO323	323	GND	96
96	GND	234	IO234	IO324	324	50_TX_IN_XCVR_TX1_LB_JB	96
96	90_PCIE_GP2_AP_FROM_BB_RX_N	235	IO235	IO325	325	50_TX_IN_XCVR_TX0_LB	96
96	GND	236	IO236	IO326	326	GND	96
96	90_PCIE_GP2_AP_FROM_BB_RX_P	237	IO237	IO327	327	GND	96
96	GND	238	IO238	IO328	328	50_RX_XCVR_PRX6_LB_A_RX0	96
96	GND	239	IO239	IO329	329	50_RX_XCVR_PRX10_LB_PRX_OUT2	96
96	GND	240	IO240	IO330	330	GND	96
96	90_PCIE_GP2_AP_TO_BB_TX_P	241	IO241	IO331	331	GND	96
96	GND	242	IO242	IO332	332	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	96
96	90_PCIE_GP2_AP_TO_BB_TX_N	243	IO243	IO333	333	GND	96
96	GND	244	IO244	IO334	334	GND	96
96	GND	245	IO245	IO335	335	50_RX_XCVR_PRX17_UHB_RX_OUT2	96
96	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	246	IO246	IO336	336	GND	96
96	GND	247	IO247	IO337	337	GND	96
96	GND	248	IO248	IO338	338	50_UHB_L_CPLR_OUT	96
96	GPIO_AOP_TO_WLAN_CONTEXT_A	249	IO249	IO339	339	GND	96
96	GPIO_AOP_TO_BB_FORCE_PWM	250	IO250	IO340	340	GND	96
96	GPIO_AOP_TO_WLAN_CONTEXT_B	251	IO251	IO341	341	GND	96
96	GND	252	IO252	IO342	342	GND	96
96	ANALOG_PP_GPU_LVCC	253	IO253	IO343	343	GND	96
96	IO_PMU_TO_SYSTEM_RESET_L	254	IO254	IO344	344	GND	96
96	GND	255	IO255	IO345	345	GND	96
96	GND	256	IO256	IO346	346	GND	96
96	SUBUS_UAT_B	257	IO257	IO347	347	GND	96
96	ANALOG_PP_CPU_PCORE_LVCC	258	IO258	IO348	348	GND	96
96	SUBUS_UAT_A	259	IO259	IO349	349	GND	96
96	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	260	IO260	IO350	350	GND	96
96	ANALOG_LAT_5G_FEM_TO_WLAN_PDTS	261	IO261	IO351	351	GND	96
96	GND	262	IO262	IO352	352	GND	96
96	GND	263	IO263	IO353	353	GND	96
96	GND	264	IO264	IO354	354	GND	96
96	GND	265	IO265	IO355	355	GND	96
96	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	266	IO266	IO356	356	GND	96
96	GND	267	IO267	IO357	357	GND	96
96	GND	268	IO268	IO358	358	GND	96
96	GND	269	IO269	IO359	359	GND	96
96	PP1V2_S2	270	IO270	IO360	360	GND	96

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97	GND	362	IO362	IO452	452	GND
97	GND	363	IO363	IO453	453	SHIELD_RFFE3_SDATA_SDR
97	GND	364	IO364	IO454	454	GND
97	GND	365	IO365	IO455	455	SHIELD_RFFE2_SCLK_SDR
97	GND	366	IO366	IO456	456	GND
97	GND	367	IO367	IO457	457	SHIELD_RFFE2_SDATA_SDR
97	GND	368	IO368	IO458	458	GND
97	GND	369	IO369	IO459	459	GND
97	GND	370	IO370	IO460	460	GND
97	GND	371	IO371	IO461	461	GND
97	GND	372	IO372	IO462	462	PP_VBUS1_E75
97	GND	373	IO373	IO463	463	PP_VBUS1_E75
97	GND	374	IO374	IO464	464	GND
97	GND	375	IO375	IO465	465	PP_UIM1_LDO11
97	GND	376	IO376	IO466	466	IO_BB_FROM_SIM2_DETECT
97	GND	377	IO377	IO467	467	PP_UIM2_LDO13
97	GND	378	IO378	IO468	468	GND
97	GND	379	IO379	IO469	469	IO_BB_TO_SIM2_CLK
97	GND	380	IO380	IO470	470	IO_BB_TO_SIM2_RESET
97	GND	381	IO381	IO471	471	IO_BB_BI_SIM2_DATA
97	50_TRX_LB_PORTB_RX1_M	382	IO382	IO472	472	GND
97	GND	383	IO383	IO473	473	GND
97	GND	384	IO384	IO474	474	GND
97	50_TRX_LB_PORTB_TX_M	385	IO385	IO475	475	GND
97	GND	386	IO386	IO476	476	GND
97	GND	387	IO387	IO477	477	IO_BB_FROM_SIM1_DETECT
97	PP_VDD_RF_1V2	388	IO388	IO478	478	IO_BB_TO_SIM1_RESET
97	SUBUS_LAT_C	389	IO389	IO479	479	IO_BB_BI_SIM1_DATA
97	GND	390	IO390	IO480	480	GND
97	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	391	IO391	IO481	481	IO_BB_TO_SIM1_CLK
97	SUBUS_LAT_B	392	IO392	IO482	482	GPIO_SEQ_PMU_TO_NFC_EN
97	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	393	IO393	IO483	483	GND
97	GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN	394	IO394	IO484	484	GND
97	GND	395	IO395	IO485	485	AMUX_PMU_BY
97	GND	396	IO396	IO486	486	AMUX_PMU_AY
97	50_TRX_L5_LNA_IN	397	IO397	IO487	487	NTC_RADIO_BB_SE
97	GND	398	IO398	IO488	488	GND
97	GND	399	IO399	IO489	489	NTC_RADIO_PA_SE
97	GND	400	IO400	IO490	490	PP1V2_NFC_S2
97	50_TRX_WLAN_G_BT_ANT3_NPLXR	401	IO401	IO491	491	GND
97	GND	402	IO402	IO492	492	GND
97	GND	403	IO403	IO493	493	GND
97	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	404	IO404	IO494	494	GPIO_SEQ_PMU_TO_BBPMU_RESET_L
97	GND	405	IO405	IO495	495	GND
97	GND	406	IO406	IO496	496	GND
97	50_WLAN_A_C1_TXRX_FEM_M	407	IO407	IO497	497	GND
97	GND	408	IO408			
97	GND	409	IO409	IO499	499	GND
97	50_LAA_RX_XCVR_PRX12	410	IO410	IO500	500	GND
97	GND	411	IO411	IO501	501	GND
97	GND	412	IO412	IO502	502	GND
97	50_TRX_HB_PAD_ANT1	413	IO413	IO503	503	GND
97	RFFE_WLAN_TO_LAT_5G_FEM_RST_L	414	IO414	IO504	504	GND
97	GND	415	IO415	IO505	505	GND
97	GND	416	IO416	IO506	506	PP3V0_S2
97	SHIELD_RFFE1_SCLK_SDR	417	IO417	IO507	507	UART1_AOP_FROM_BB_RXD
97	GND	418	IO418	IO508	508	GND
97	SHIELD_RFFE1_SDATA_SDR	419	IO419	IO509	509	GND
97	GND	420	IO420	IO510	510	GPIO_NFC_TO_ARCAMP_RESET_L
97	GND	421	IO421	IO511	511	UART1_AOP_TO_BB_TXD
97	GND	422	IO422	IO512	512	GND
97	GND	423	IO423	IO513	513	GPIO_AP_TO_BB_TIME_MARK
97	GND	424	IO424	IO514	514	GPIO_NFC_TO_ARCAMP_TRIG
97	GND	425	IO425	IO515	515	GPIO_AP_FROM_BT_AUDIO_SYNC
97	GND	426	IO426	IO516	516	GND
97	GND	427	IO427	IO517	517	PP1V8_S2
97	GND	428	IO428	IO518	518	GPIO_AP_TO_BB_COREDUMP
97	PP_VDD_BOOST	429	IO429	IO519	519	GPIO_BT_TO_BOT_SPKR_TRIG
97	GND	430	IO430	IO520	520	GND
97	GND	431	IO431	IO521	521	GND
97	GND	432	IO432	IO522	522	GND
97	50_TRX_HB_PAD_ANT2_M	433	IO433	IO523	523	PP_VDD_MAIN
97	GND	434	IO434	IO524	524	GND
97	GND	435	IO435	IO525	525	PP_VDD_MAIN
97	GND	436	IO436	IO526	526	GND
97	GND	437	IO437	IO527	527	PP_VDD_MAIN
97	GND	438	IO438	IO528	528	GND
97	50_CPLR_L_CPL1_LAT_OUT	439	IO439	IO529	529	PP_VDD_MAIN
97	GND	440	IO440	IO530	530	GND
97	GND	441	IO441	IO531	531	PP_VDD_MAIN
97	GND	442	IO442	IO532	532	GND
97	GND	443	IO443	IO533	533	GND
97	GND	444	IO444	IO534	534	GND
97	GND	445	IO445	IO535	535	PP_VDD_MAIN
97	GND	446	IO446	IO536	536	GND
97	GND	447	IO447	IO537	537	PP_VDD_MAIN
97	GND	448	IO448	IO538	538	GND
97	GND	449	IO449	IO539	539	PP_VDD_MAIN
97	GND	450	IO450	IO540	540	GND

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98	GND	542	IO542
98	PP_VDD_MAIN	543	IO543
98	GPIO_AP_CANARY2	544	IO544
98	GND	545	IO545
98	GND	546	IO546
98	PP_VDD_MAIN	547	IO547
98	GND	548	IO548
98	GND	549	IO549
98	GND	550	IO550
98	GND	551	IO551
98	GND	552	IO552
98	GND	553	IO553
98	GND	554	IO554
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98	GND	556	IO556
98	GND	557	IO557
98	GND	558	IO558
98	GND	559	IO559
98	GND	560	IO560
98	GND	561	IO561
98	GPIO_CANARY_2B_TO_2C	562	IO562
98	GND	563	IO563
98	GND	564	IO564
98	GND	565	IO565
98	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	566	IO566
98	GND	567	IO567
98	GPIO_AP_FROM_BB_RESET_DETECT_L	568	IO568
98	GND	569	IO569
98	PCIE_GP2_AP_TO_BB_PERST_L	570	IO570
98	GND	571	IO571
98	GND	572	IO572
98	GND	573	IO573
98	PCIE_GP2_AP_BT_BB_CLKREQ_L	574	IO574
98	GND	575	IO575
98	GND	576	IO576
98	GND	577	IO577
98	GPIO_CANARY_2B_TO_2C	578	IO578
98	GND	579	IO579
98	GND	580	IO580
98	GND	581	IO581
98	GND	582	IO582
98	GND	583	IO583
98	GND	584	IO584
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98	GND	600	IO600
98	GND	601	IO601
98	GND	602	IO602
98	GND	603	IO603
98	GND	604	IO604
98	GND	605	IO605

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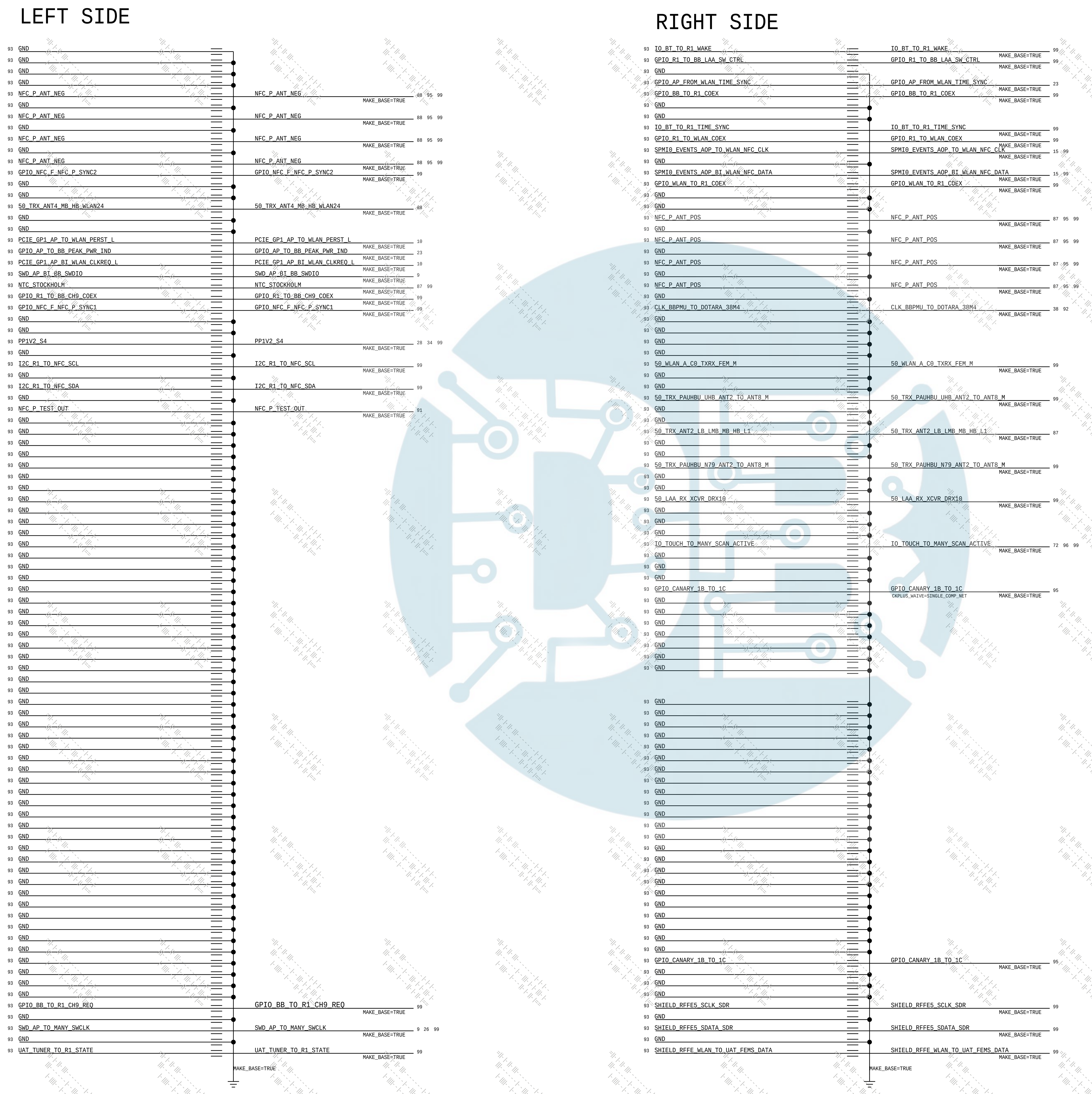

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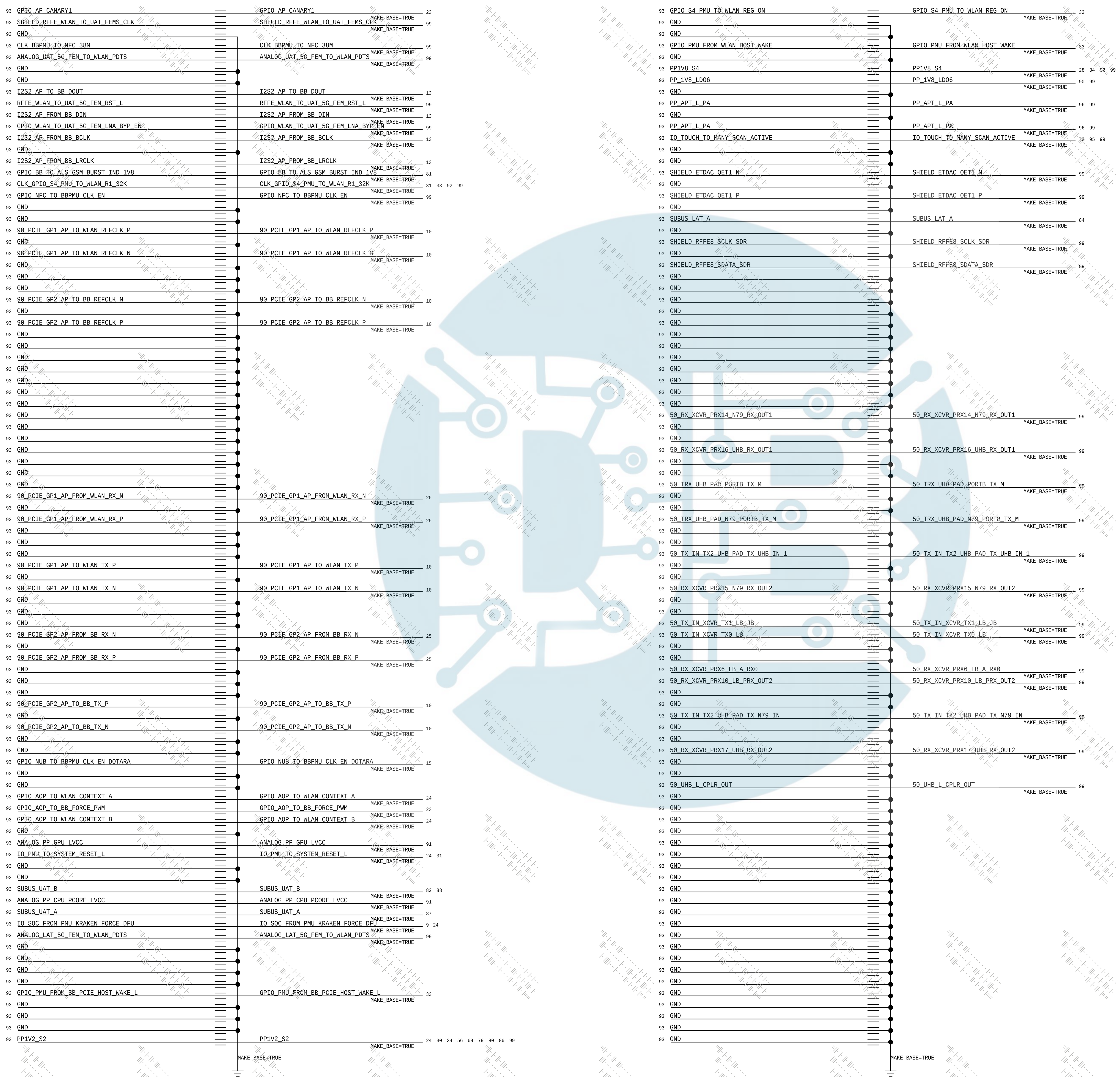

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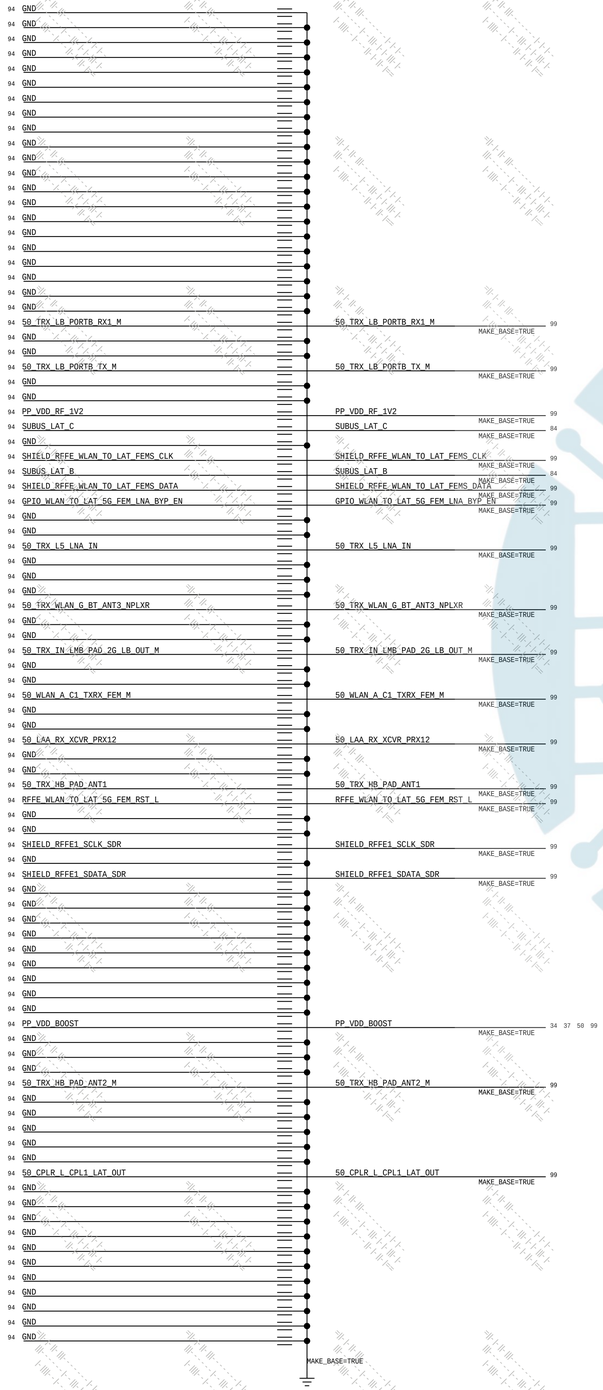

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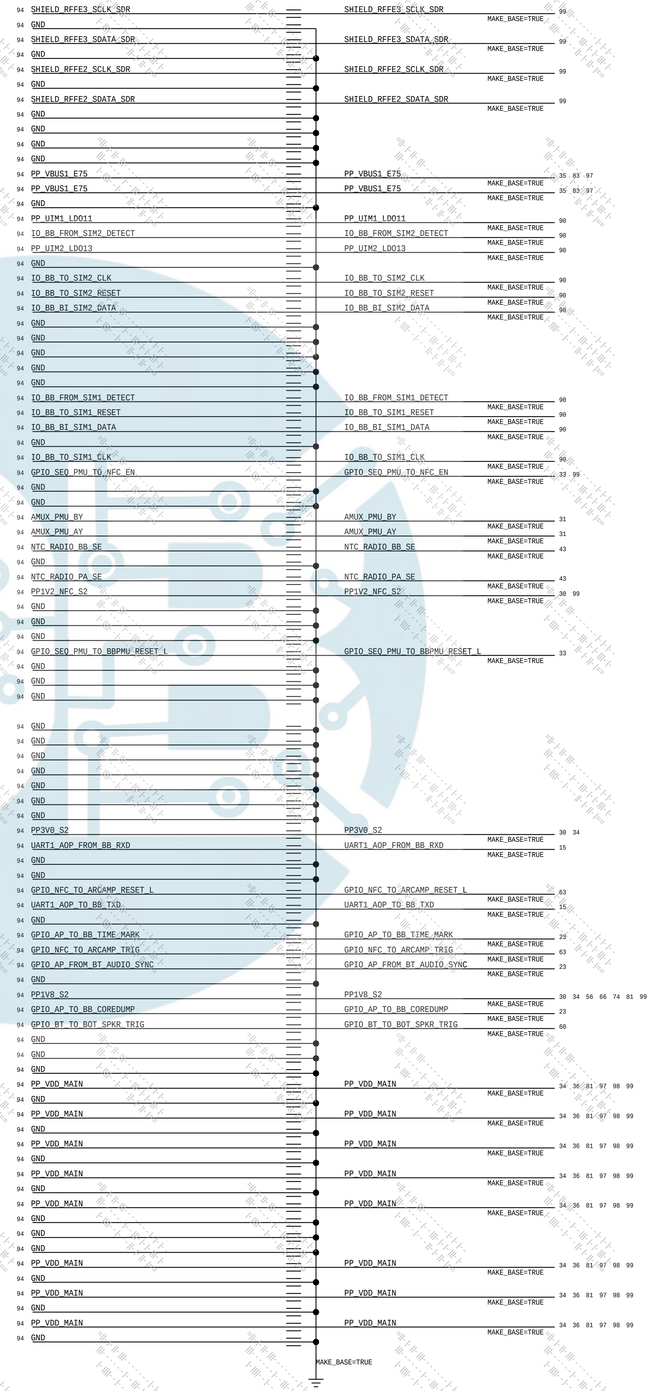

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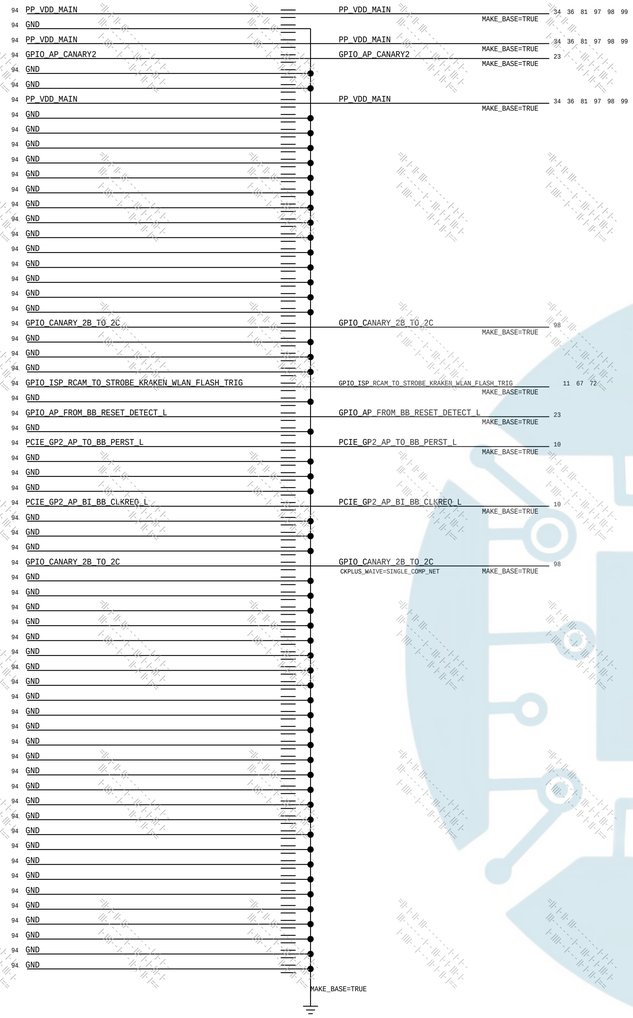
Interposer: Symbol 4 Aliases

LEFT SIDE



PAGE TITLE	INTERPOSER: Aliases (4/4)
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
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SHEET	98 OF 117

HIERARCHY BLOCKS

POWER

117 116 113 104 99 98 97 81 36 34 PP_VDD_MAIN
105 97 50 37 34 PP_VDD_BOOST
105 97 PP_VDD_RF_1V2
117 116 104 99 96 90 PP_1V8_LDO6

RFFE

107 97 SHIELD_RFFE1_SCLK_SDR
107 97 SHIELD_RFFE1_SDATA_SDR
106 97 SHIELD_RFFE2_SCLK_SDR
106 97 SHIELD_RFFE2_SDATA_SDR
117 105 99 97 SHIELD_RFFE3_SCLK_SDR
117 105 99 97 SHIELD_RFFE3_SDATA_SDR
104 96 SHIELD_RFFE8_SCLK_SDR
104 96 SHIELD_RFFE8_SDATA_SDR

ET/APT IC

PP_APT_L_PA — PP_APT_L_PA — 96 106
SHIELD_ETDAC_QET1_P — SHIELD_ETDAC_QET1_P — 96 104
SHIELD_ETDAC_QET1_N — SHIELD_ETDAC_QET1_N — 96 104

LB PAD

50_RX_XCVR_PRX6_LB_A_RX0 — 50_RX_XCVR_PRX6_LB_A_RX0 — 96 105
50_RX_XCVR_PRX10_LB_PRX_OUT2 — 50_RX_XCVR_PRX10_LB_PRX_OUT2 — 96 105
50_TX_IN_XCVR_TX1_LB_JB — 50_TX_IN_XCVR_TX1_LB_JB — 96 105
50_TX_IN_XCVR_TX0_LB — 50_TX_IN_XCVR_TX0_LB — 96 105
50_TRX_IN_LMB_PAD_2G_LB_OUT_M — 50_TRX_IN_LMB_PAD_2G_LB_OUT_M — 97 105
50_TRX_LB_PORTB_RX1_M — 50_TRX_LB_PORTB_RX1_M — 97 105
50_TRX_LB_PORTB_TX_M — 50_TRX_LB_PORTB_TX_M — 97 105

UHB PA

50_RX_XCVR_PRX14_N79_RX_OUT1 — 50_RX_XCVR_PRX14_N79_RX_OUT1 — 96 106
50_RX_XCVR_PRX15_N79_RX_OUT2 — 50_RX_XCVR_PRX15_N79_RX_OUT2 — 96 106
50_RX_XCVR_PRX16_UHB_RX_OUT1 — 50_RX_XCVR_PRX16_UHB_RX_OUT1 — 96 106
50_RX_XCVR_PRX17_UHB_RX_OUT2 — 50_RX_XCVR_PRX17_UHB_RX_OUT2 — 96 106
50_TX_IN_TX2_UHB_PAD_TX_N79_IN — 50_TX_IN_TX2_UHB_PAD_TX_N79_IN — 96 106
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 — 50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 — 96 106
50_UHB_L_CPLR_OUT — 50_UHB_L_CPLR_OUT — 96 106
50_TRX_UHB_PAD_PORTB_TX_M — 50_TRX_UHB_PAD_PORTB_TX_M — 96 106
50_TRX_UHB_PAD_N79_PORTB_TX_M — 50_TRX_UHB_PAD_N79_PORTB_TX_M — 96 106

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LAT

50_TRX_HB_PAD_ANT1 — 50_TRX_HB_PAD_ANT1 — 97 107
50_CPLR_L_CPL1_LAT_OUT — 50_CPLR_L_CPL1_LAT_OUT — 97 107
50_TRX_L5_LNA_IN — 50_TRX_L5_LNA_IN — 97 108
50_TRX_ANT1_LB_LMB_MB_HB — 50_TRX_ANT1_LB_LMB_MB_HB — 89 107
50_TRX_ANT3_MB_HB_WLAN24 — 50_TRX_ANT3_MB_HB_WLAN24 — 89 108
50_TRX_ANT7_UHB_N79 — 50_TRX_ANT7_UHB_N79 — 89 109
50_TRX_ANT9_UHB_N79 — 50_TRX_ANT9_UHB_N79 — 89 110
50_TRX_HB_PAD_ANT2_M — 50_TRX_HB_PAD_ANT2_M — 97 107

LAA

50_TRX_WLAN_G_BT_ANT3_NPLXR — 50_TRX_WLAN_G_BT_ANT3_NPLXR — 97 108

UAT

50_TRX_ANT8_R1_UHB_N79 — 50_TRX_ANT8_R1_UHB_N79 — 87 111
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M — 50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M — 95 111
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M — 50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M — 95 111
50_R1_ANT2_CH5 — 50_TRX_R1_ANT2_CH5 — 99 102 111
50_R1_ANT2_CH9 — 50_TRX_R1_ANT2_CH9 — 99 102 111

HIER_WIFI_TOP

117 116 113 104 99 98 97 81 36 34 PP_VDD_MAIN
116 113 99 97 81 74 66 56 34 30 PP1V8_S2
116 101 99 96 92 34 28 PP1V8_S4

POWER

PP_VDD_MAIN_5GFEMU
PP_VDD_MAIN_5GFEML
PP1V8_S2
PP1V8_S4

5 GHZ rFEM (UAT)

WLAN
116 95 50_WLAN_A_C0_TXRX_FEM_M
116 96 RFFE_WLAN_TO_UAT_5G_FEM_RST_L
116 96 SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
116 95 SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
116 96 GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN
116 96 ANALOG_UAT_5G_FEM_TO_WLAN_PDTS
117 116 104 99 96 90 PP_1V8_LDO6
116 95 SHIELD_RFFE5_SCLK_SDR
116 95 SHIELD_RFFE5_SDATA_SDR
116 95 50_LAA_RX_XCVR_DRX10

ANT
50_WLAN_A_C0_TXRX_FEM_M
RFFE_WLAN_TO_UAT_5G_FEM_RST_L
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN
ANALOG_UAT_5G_FEM_TO_WLAN_PDTS
LAA
PP_VIO_RFFE1_XCVR_VIO
RFFE1_XCVR_SCLK
RFFE1_XCVR_SDATA
50_LAA_RX_XCVR_DRX10

50_WLAN_A_LAA_ANT6 — 50_TRX_ANT6_WLAN_A_LAA — 87 116

5 GHZ rFEM (LAT)

WLAN
117 97 50_WLAN_A_C1_TXRX_FEM_M
117 97 RFFE_WLAN_TO_LAT_5G_FEM_RST_L
117 97 SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK
117 97 SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA
117 97 GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN
117 96 ANALOG_LAT_5G_FEM_TO_WLAN_PDTS
117 116 104 99 96 90 PP_1V8_LDO6
117 105 99 97 SHIELD_RFFE3_SCLK_SDR
117 105 99 97 SHIELD_RFFE3_SDATA_SDR
117 97 50_LAA_RX_XCVR_PRX12

ANT
50_WLAN_A_C1_TXRX_FEM_M
RFFE_WLAN_TO_LAT_5G_FEM_RST_L
SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK
SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA
GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN
ANALOG_LAT_5G_FEM_TO_WLAN_PDTS
LAA
PP_VIO_RFFE0_XCVR_VIO
RFFE0_XCVR_SCLK
RFFE0_XCVR_SDATA
50_LAA_RX_XCVR_PRX12

50_WLAN_A_LAA_ANT5 — 50_TRX_ANT5_WLAN_A_LAA — 89 117

hier_arrow

101 95 34 28 PP1V2_S4 — PP1V2_S4
116 101 99 96 92 34 28 PP1V8_S4 — PP1V8_S4
101 38 PP1V0_R1_ANA_S4 — PP1V0_R1_ANA
101 38 PP1V0_S4 — PP1V0_R1_SOC
101 33 GPIO_S4_PMU_TO_R1_RESET_L — APPMU_TO_R1_RESET_L
101 96 92 33 31 CLK_GPIO_S4_PMU_TO_WLAN_R1_32K — APPMU_TO_WLAN_32K_CLK
101 23 GPIO_AOP_TO_R1_COREDUMP_TRIGGER — AOP_TO_R1_COREDUMP_TRIG
101 23 GPIO_SCM_AOP_TO_R1_SPI_CS_L — SPI_AOP_TO_R1_CS_L
101 56 15 SPI0_AOP_TO_IMU_R1_SCLK — SPI_AOP_TO_R1_SCLK
101 56 15 SPI0_AOP_TO_IMU_R1_MOSI — SPI_AOP_TO_R1_MOSI
101 56 15 SPI0_AOP_FROM_IMU_R1_MISO — SPI_R1_TO_AOP_MISO
101 23 GPIO_SCM_AOP_FROM_R1_INT — R1_TO_AOP_INT
114 101 99 95 I2C_R1_TO_NFC_SCL (CKPLUS_WATVE=I2C_PULLUP) — I2C_R1_TO_SE_SCL
114 101 99 95 I2C_R1_TO_NFC_SDA (CKPLUS_WATVE=I2C_PULLUP) — I2C_R1_TO_SE_SDA
101 95 GPIO_BB_TO_R1_CH9_REQ — BB_TO_R1_CH9_REQ
101 95 GPIO_WLAN_TO_R1_COEX — WLAN_TO_R1_COEX
101 95 GPIO_R1_TO_BB_CH9_COEX — R1_TO_BB_GRANT
101 95 GPIO_R1_TO_WLAN_COEX — R1_TO_WLAN_COEX
101 95 GPIO_BB_TO_R1_COEX — BB_TO_R1_LAA_REQ
101 23 GPIO_AOP_TO_R1_TIME_SYNC_L — AOP_TO_R1_TIME_SYNC
101 95 IO_BT_TO_R1_TIME_SYNC — BT_TO_R1_TIME_SYNC
101 95 IO_BT_TO_R1_WAKE — BT_TO_R1_WAKE
101 9 SWD_AP_BI_R1_SWDIO — SWD_AOP_BI_R1_SWDIO
101 95 26 9 SWD_AP_TO_MANY_SWCLK — SWD_AOP_TO_MANY_SWCLK
102 87 50_TRX_R1_AOA1 — 50_R1_ANT0
102 87 50_TRX_R1_AOA2 — 50_R1_ANT1
102 87 50_TRX_R1_AOA3 — 50_R1_ANT3
111 102 99 50_TRX_R1_ANT2_CH9 — 50_R1_ANT_CH9
111 102 99 50_TRX_R1_ANT2_CH5 — 50_LAA_TO_R1
101 95 UAT_TUNER_TO_R1_STATE — TUNER_TO_R1_STATE
101 95 GPIO_R1_TO_BB_LAA_SW_CTRL — R1_TO_BB_LAA_SW_CTRL

95 15 SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA — R13801 33.2 1% 1/32W MF 01005 ROOM=IRONMAN_NFC — SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA_NFC_F_R — 99 113

hier_nfc_top

POWER

117 116 113 104 99 98 97 81 36 34 PP_VDD_MAIN
116 113 99 97 81 74 66 56 34 30 PP1V8_S2
113 96 86 80 79 69 56 34 30 24 PP1V2_S2
114 97 30 PP1V2_NFC_S2

CONTROL

113 NC_NFC_F_DEV_WAKE (NO_TEST=1) — AOP_TO_NFC_F_DEV_WAKE
113 23 GPIO_AOP_TO_NFC_IRONMAN_EN — AOP_TO_NFC_F_EN
113 96 GPIO_NFC_TO_BBPMU_CLK_EN — NFC_F_TO_BBPMU_CLK_EN

NFC RF

114 95 87 NFC_P_ANT_POS — NFC_P_ANT_POS
114 95 88 NFC_P_ANT_NEG — NFC_P_ANT_NEG
113 74 NFC_F_ANT_POS — NFC_F_ANT_POS
113 74 NFC_F_ANT_NEG — NFC_F_ANT_NEG

NFC SPMI

113 95 15 SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK — SPMI_AOP_TO_RADIOS_CLK
113 99 SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA_NFC_F_R — SPMI_AOP_TO_RADIOS_DATA

MISC

113 96 CLK_BBPMU_TO_NFC_38M — 50_BBPMU_TO_NFC_F_CLK_38MHZ
113 91 NFC_F_TEST_OUT — NFC_F_TEST_OUT
114 97 33 GPIO_SEQ_PMU_TO_NFC_EN — PMU_TO_NFC_P_EN
114 63 33 GPIO_PMU_NFC_TO_ARCAMP_TRIG — NFC_P_TO_ARC_TRIG
114 63 33 GPIO_PMU_NFC_TO_ARCAMP_RESET_L — NFC_P_TO_ARC_RESET_L
114 101 99 95 I2C_R1_TO_NFC_SCL — I2C_R1_TO_SE_SCL
114 101 99 95 I2C_R1_TO_NFC_SDA — I2C_R1_TO_SE_SDA
114 95 87 NTC_STOCKHOLM — NFC_P_THERMISTOR_UAT2
113 95 GPIO_NFC_F_NFC_P_SYNC1 — NFC_F_TO_NFC_P_COEX
113 95 GPIO_NFC_F_NFC_P_SYNC2 — NFC_P_TO_NFC_F_COEX
113 96 95 72 IO_TOUCH_TO_MANY_SCAN_ACTIVE — TOUCH_TO_NFC_SCAN_ACTIVE

SYNC_MASTER=D53_ice_0.19.0 SYNC_DATE=02/01/2019

PAGE TITLE: HIERARCHIES

DRAWING NUMBER 051-05170 SIZE D
REVISION 10.0.0
BRANCH 1
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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0024125573	ENGINEERING RELEASED	2020-07-01

ARROW

LAST_MODIFICATION=Wed Jul 1 16:52:56 2020

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101	2	MODULE		
102	3	FILTERS MATCHING		

FRONT PAGE

POWER
- PP1V2_S4
- PP1V8_S4
- PP1V0_R1_ANA_S4
- PP1V0_S4

HOST IPC
- SPI0_AOP_TO_IMU_R1_SCLK
- GPIO_SCM_AOP_TO_R1_SPI_CS_L
- SPI0_AOP_FROM_IMU_R1_MISO
- SPI0_AOP_TO_IMU_R1_MOSI
- GPIO_AOP_TO_R1_COREDUMP_TRIGGER
- GPIO_SCM_AOP_FROM_R1_INT

RESET/CLOCK
- GPIO_S4_PMU_TO_R1_RESET_L
- CLK_GPIO_S4_PMU_TO_WLAN_R1_32K
- GPIO_AOP_TO_R1_TIME_SYNC_L

DEBUG
- SWD_AP_TO_MANY_SWCLK
- SWD_AP_BI_R1_SWDIO

SPMI/COEX GPIOS
- GPIO_WLAN_TO_R1_COEX
- GPIO_R1_TO_BB_CH9_COEX
- GPIO_R1_TO_WLAN_COEX
- GPIO_BB_TO_R1_COEX
- GPIO_BB_TO_R1_CH9_REQ

SE IPC
- I2C_R1_TO_NFC_SCL
- I2C_R1_TO_NFC_SDA

BT TIME SYNC / WAKE
- IO_BT_TO_R1_TIME_SYNC
- IO_BT_TO_R1_WAKE

ANTENNA SWITCH CTRL
- UAT_TUNER_TO_R1_STATE
- GPIO_R1_TO_BB_LAA_SW_CTRL

ANTENNA
- 50_TRX_R1_AOA1
- 50_TRX_R1_AOA2
- 50_TRX_R1_AOA3
- 50_TRX_R1_ANT2_CH9
- 50_TRX_R1_ANT2_CH5

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES:	COMMENTS:
339S00790	339S00774	?	U_ROSE_R	USI STRIDER2 MODULE

SCH #: 951-09582
PCB #: 920-05369
BOM #: 939-05686

FRONT PAGE

DRAWING TITLE: SCH,TOP,D54
DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH:
PAGE: 1 OF 3
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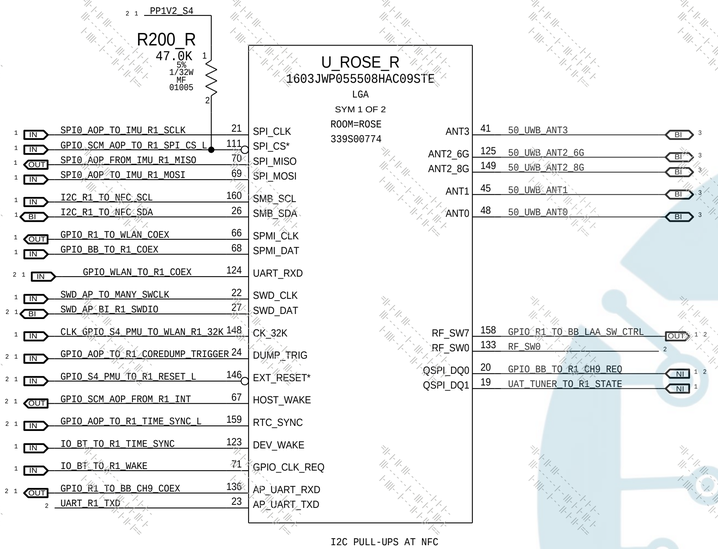
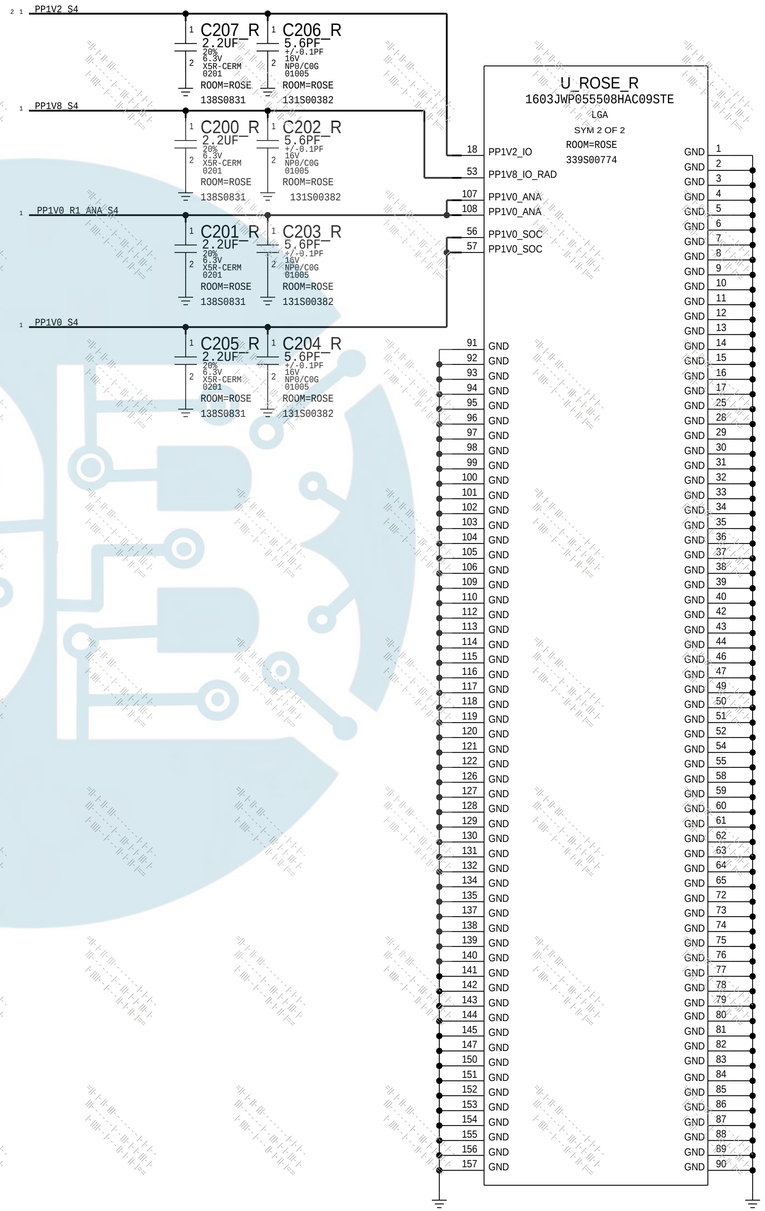
MODULE



I2C PULL-UPS AT NFC



PP200_R P2MM-NSM OMIT — GPIO_S4_PMU_TO_R1_RESET_L

PP203_R P2MM-NSM OMIT — GPIO_R1_TO_BB_CH9_COEX

PP206_R P2MM-NSM OMIT — GPIO_WLAN_TO_R1_COEX

PP209_R P2MM-NSM OMIT — RF_SW0

PP209_R P2MM-NSM OMIT — GPIO_BB_TO_R1_CH9_REQ

PP221_R P2MM-NSM OMIT — GPIO_R1_TO_BB_LAA_SW_CTRL

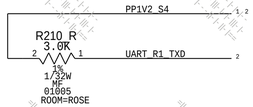
PP211_R P2MM-NSM OMIT — SWD_AP_BI_R1_SWDIO

PP212_R P2MM-NSM OMIT — GPIO_AOP_TO_R1_COREDUMP_TRIGGER

PP213_R P2MM-NSM OMIT — GPIO_SCM_AOP_FROM_R1_INT

PP214_R P2MM-NSM OMIT — GPIO_AOP_TO_R1_TIME_SYNC_L

UNSECURE BOOT BOOTSTRAP PULLUP



PAGE TITLE: MODULE

DRAWING NUMBER: 051-05170 | SIZE: D
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BRANCH: 1
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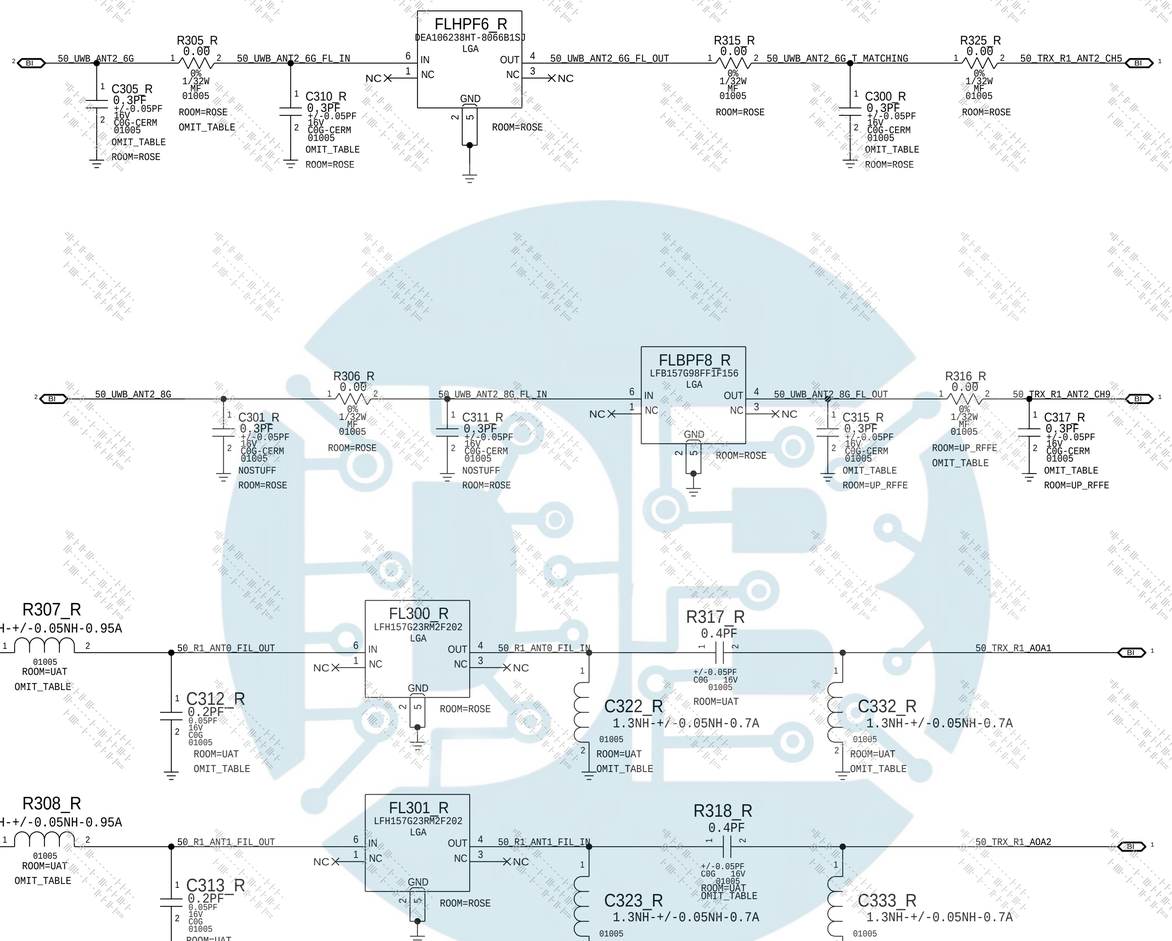
FILTERS/MATCHING AND ANTENNA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0893	1	0.2PF	C305_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0369	1	0.5PF	C305_R	BOARD_ID:D54
131S0369	1	0.5PF	C305_R	BOARD_ID:D52
152S00493	1	0.9NH	R305_R	BOARD_ID:D53&B0ARD_ID:D53P
152S01247	1	1.0NH	R305_R	BOARD_ID:D54
152S01246	1	0.8NH	R305_R	BOARD_ID:D52
131S0893	1	0.2PF	C310_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0369	1	0.5PF	C310_R	BOARD_ID:D54
131S00030	1	0.4PF	C310_R	BOARD_ID:D52
152S00430	1	2.3NH	C300_R	BOARD_ID:D52
131S0893	1	0.2PF	C315_R	BOARD_ID:D54
131S0893	1	0.2PF	C315_R	BOARD_ID:D52
152S01109	1	0.6NH	R316_R	BOARD_ID:D53&B0ARD_ID:D53P
152S01246	1	0.8NH	R316_R	BOARD_ID:D54
152S01109	1	0.6NH	R316_R	BOARD_ID:D52
131S0893	1	0.2PF	C317_R	BOARD_ID:D53&B0ARD_ID:D53P

Note: C300_R, C315_R are NOSTUFF for D53
NOTE: C300_R IS NOSTUFF FOR D54
Note: C317_R is NOSTUFF for D52/D54



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0648	1	0.3PF	C302_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0648	1	0.3PF	C302_R	BOARD_ID:D54
131S00030	1	0.4PF	C302_R	BOARD_ID:D52
152S00494	1	0.8NH	R307_R	BOARD_ID:D53&B0ARD_ID:D53P
152S00493	1	0.9NH	R307_R	BOARD_ID:D54
152S01246	1	0.8NH	R307_R	BOARD_ID:D52
131S0648	1	0.3PF	C312_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0893	1	0.2PF	C312_R	BOARD_ID:D54
131S0648	1	0.3PF	C312_R	BOARD_ID:D52
152S00421	1	1.4NH	C322_R	BOARD_ID:D53&B0ARD_ID:D53P
152S01110	1	1.3NH	C322_R	BOARD_ID:D54
152S00416	1	1.2NH	C322_R	BOARD_ID:D52
152S00421	1	1.4NH	C332_R	BOARD_ID:D53&B0ARD_ID:D53P
152S01110	1	1.3NH	C332_R	BOARD_ID:D54
152S00423	1	1.6NH	C332_R	BOARD_ID:D52
131S0648	1	0.3PF	C303_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0893	1	0.2PF	C303_R	BOARD_ID:D54
131S0648	1	0.3PF	C303_R	BOARD_ID:D52
152S00494	1	0.8NH	R308_R	BOARD_ID:D53&B0ARD_ID:D53P
152S01247	1	1.0NH	R308_R	BOARD_ID:D54
152S00493	1	0.9NH	R308_R	BOARD_ID:D52
131S0648	1	0.3PF	C313_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0893	1	0.2PF	C313_R	BOARD_ID:D54
131S0893	1	0.2PF	C313_R	BOARD_ID:D52
152S00493	1	0.9NH	C323_R	BOARD_ID:D53&B0ARD_ID:D53P
152S01110	1	1.3NH	C323_R	BOARD_ID:D54
152S00416	1	1.2NH	C323_R	BOARD_ID:D52
131S0648	1	0.3PF	R318_R	BOARD_ID:D53&B0ARD_ID:D53P
131S00030	1	0.4PF	R318_R	BOARD_ID:D54
131S0616	1	0.6PF	R318_R	BOARD_ID:D52
152S00493	1	0.9NH	C333_R	BOARD_ID:D53&B0ARD_ID:D53P
152S00423	1	1.6NH	C333_R	BOARD_ID:D54
152S00421	1	1.4NH	C333_R	BOARD_ID:D52
131S0648	1	0.3PF	C304_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0893	1	0.2PF	C304_R	BOARD_ID:D54
131S00030	1	0.4PF	C304_R	BOARD_ID:D52
152S01247	1	1.0NH	R309_R	BOARD_ID:D53&B0ARD_ID:D53P
152S00419	1	1.1NH	R309_R	BOARD_ID:D54
152S00493	1	0.9NH	R309_R	BOARD_ID:D52
131S0648	1	0.3PF	C314_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0893	1	0.2PF	C314_R	BOARD_ID:D54
131S0648	1	0.3PF	C314_R	BOARD_ID:D52
152S00421	1	1.4NH	C324_R	BOARD_ID:D53&B0ARD_ID:D53P
152S01110	1	1.3NH	C324_R	BOARD_ID:D54
152S00419	1	1.1NH	C324_R	BOARD_ID:D52
131S0648	1	0.3PF	R319_R	BOARD_ID:D53&B0ARD_ID:D53P
131S0617	1	0.9PF	R319_R	BOARD_ID:D54
131S00030	1	0.4PF	R319_R	BOARD_ID:D52
152S00421	1	1.4NH	C334_R	BOARD_ID:D53&B0ARD_ID:D53P
152S01110	1	1.3NH	C334_R	BOARD_ID:D54
152S00423	1	1.6NH	C334_R	BOARD_ID:D52

PAGE TITLE
FILTERS MATCHING

DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 3 OF 3
SHEET 102 OF 117

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0024125573	ENGINEERING RELEASED	2020-07-01

MAV20 HIER_RADIO_MAV_TOP

LAST_MODIFICATION=Wed Jul 1 16:52:55 2020

X1804

PAGE	CSA	CONTENTS	SYNC	DATE
103	1	FRONT PAGE		
104	17	QET_DISCRETE_1		08/01/2019
105	20	LB PAD		08/01/2019
106	22	UHB LAT PAD		08/01/2019
107	30	COUPLER LOWER		08/01/2019
108	35	LOWER ANTENNA FEEDS_ANT3		08/01/2019
109	36	LOWER ANTENNA FEEDS_ANT7		08/01/2019
110	38	LOWER ANTENNA FEEDS_ANT9		08/01/2019
111	40	UPPER ANTENNA FEEDS_ANT8		10/02/2019

POWER

PP_VDD_MAIN	VOLTAGE=3.8	IN 2
PP_VDD_BOOST	VOLTAGE=4.5	IN 3 4 5
PP_VDD_RF_1V2	VOLTAGE=1.2	IN 3 4
PP_1V8_LDO6	VOLTAGE=1.8	IN 2 3 4 5

ET/APT IC

PP_APT_L_PA	VOLTAGE=5.5	IN 4
SHIELD_ETDAC_QET1_P		IN 2
SHIELD_ETDAC_QET1_N		IN 2

RF RFFE

SHIELD_RFFE1_SCLK_SDR		IN 5
SHIELD_RFFE1_SDATA_SDR		IO 5
SHIELD_RFFE2_SCLK_SDR		IN 4
SHIELD_RFFE2_SDATA_SDR		IO 4
SHIELD_RFFE3_SCLK_SDR		IN 3 4
SHIELD_RFFE3_SDATA_SDR		IO 3 4
SHIELD_RFFE8_SCLK_SDR		IN 2 3
SHIELD_RFFE8_SDATA_SDR		IO 2 3

LB PAD

50_RX_XCVR_PRX6_LB_A_RX0		OUT 3
50_RX_XCVR_PRX10_LB_PRX_OUT2		OUT 3
50_TX_IN_XCVR_TX1_LB_JB		IN 3
50_TX_IN_XCVR_TX0_LB		IN 3
50_TRX_IN_LMB_PAD_2G_LB_OUT_M		IN 3
50_TRX_LB_PORTB_RX1_M		OUT 3
50_TRX_LB_PORTB_TX_M		IO 3

UHB PA (LAT)

50_RX_XCVR_PRX14_N79_RX_OUT1		OUT 4
50_RX_XCVR_PRX15_N79_RX_OUT2		OUT 4
50_RX_XCVR_PRX16_UHB_RX_OUT1		OUT 4
50_RX_XCVR_PRX17_UHB_RX_OUT2		OUT 4
50_TX_IN_TX2_UHB_PAD_TX_N79_IN		IN 4
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1		IN 4
50_UHB_L_CPLR_OUT		IN 4
50_TRX_UHB_PAD_PORTB_TX_M		OUT 4
50_TRX_UHB_PAD_N79_PORTB_TX_M		OUT 4

LAT

50_TRX_HB_PAD_ANT1		IO 5
50_CPLR_L_CPL1_LAT_OUT		IN 5
50_TRX_L5_LNA_IN		OUT 6
50_TRX_ANT1_LB_LMB_MB_HB		IO 5
50_TRX_ANT3_MB_HB_WLAN24		IO 6
50_TRX_ANT7_UHB_N79		IO 7
50_TRX_ANT9_UHB_N79		IO 8
50_TRX_HB_PAD_ANT2_M		IO 5

LAA

50_TRX_WLAN_G_BT_ANT3_NPLXR		IO 6

UAT

50_TRX_ANT8_R1_UHB_N79		IO 9
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M		IO 9
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M		IO 9
50_TRX_R1_ANT2_CH5		IO 9
50_TRX_R1_ANT2_CH9		IO 9

SCH #: 951-11456

FRONT PAGE

DRAWING TITLE: SCH,TOP,D54

DRAWING NUMBER: 051-05170 SIZE: D

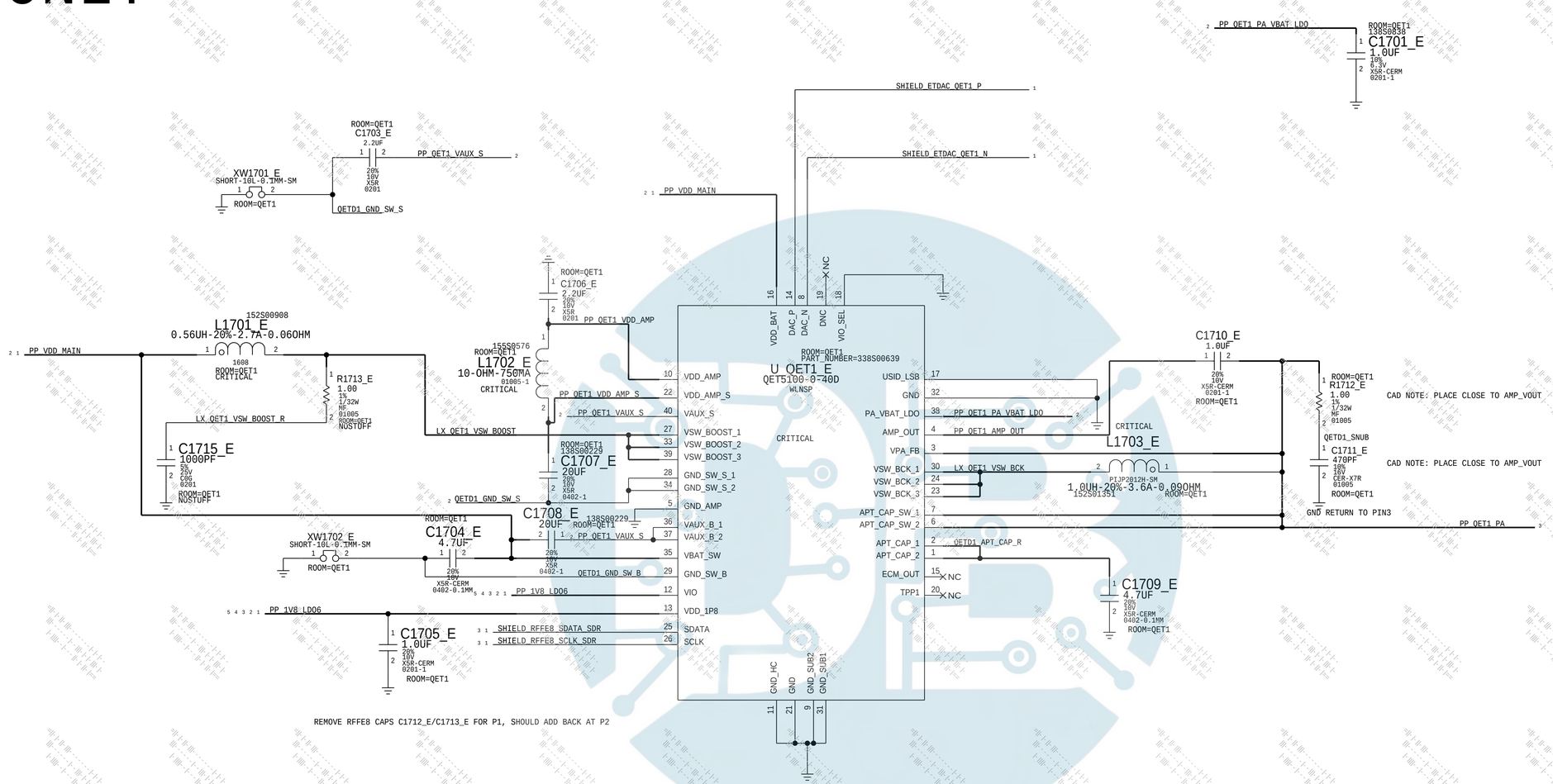
REVISION: 10.0.0

BRANCH:

PAGE: 1 OF 40

SHEET: 103 OF 117

DISCRETE QET5100 1
LB ONLY



REMOVE RFFE8 CAPS C1712_E/C1713_E FOR P1, SHOULD ADD BACK AT P2

USID=0X4 WHEN UISD PIN IS GND
USID=0X5 WHEN UISD PIN IS HIGH

SYNC_DATE=08/01/2019

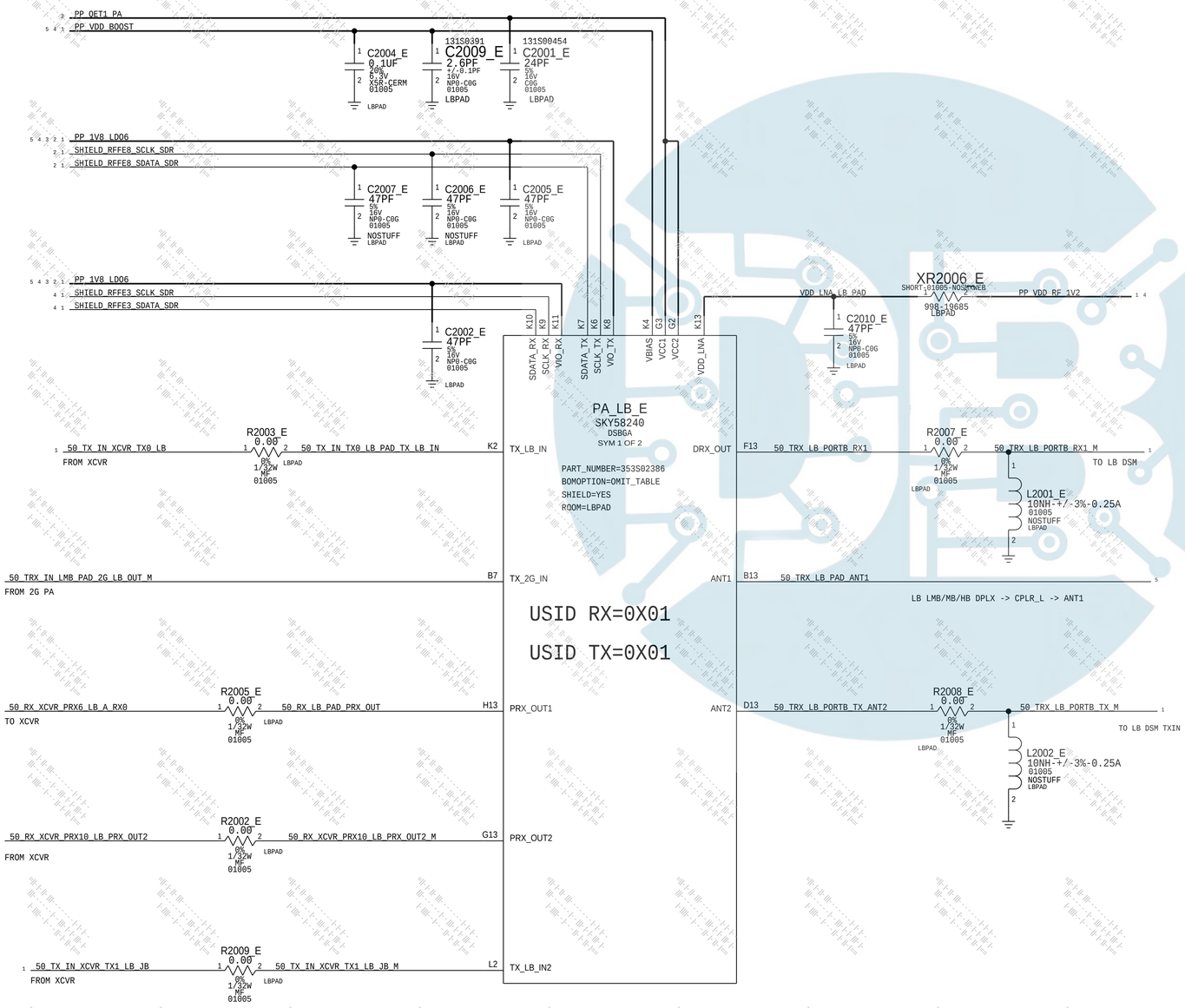
PAGE TITLE: QET_DISCRETE_1

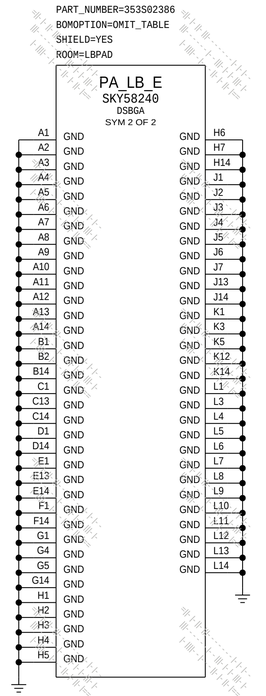
DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: 1
PAGE: 17 OF 40
SHEET: 104 OF 117

LB PAD

OMIT TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02386	1	IC,LB PAD,SKY58240,WW,DSMBGA84	PA_LB_E	CRITICAL	RF_SKU:NAJPARF_SKU:NAMM
353S02387	1	IC,LB PAD,SKY58241,ROW,DSMBGA84	PA_LB_E	CRITICAL	RF_SKU:ROW





SYNC_DATE=08/01/2019

PAGE TITLE: LB PAD

DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
BRANCH: 1
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UHB LAT PAD

PP_1V8_LDO6
SHIELD_RFFE2_SCLK_SDR
SHIELD_RFFE2_SDATA_SDR
PP_1V8_LDO6
SHIELD_RFFE3_SCLK_SDR
SHIELD_RFFE3_SDATA_SDR

PP_VDD_BOOST
PP_APT_L_PA
VDD_LNA_UHB_PAD
XR2207_E SHORT-01005-NOSTUFF
PP_VDD_RF_1V2
998-19685 UHB_LAT

C2211_E 1.0UF 20% 10V X5R-CERM 0201-1 UHB_LAT
131S0383 C2212_E 1.8PF +/-0.1PF 16V NP0-C0G 01005-1 UHB_LAT
131S0585 C2208_E 4.9PF +/-0.05PF 25V C0G-CERM 0201 UHB_LAT
C2207_E 1000PF 10% 6.3V X5R-CERM 01005 UHB_LAT

PAUHBL_E
SKY58245-17
DSBGA
SYM 1 OF 2
PART_NUMBER=353S02389
SHIELD=YES
ROOM=UHB_LAT

USID RX=0X06
USID TX=0X06

CRITICAL

50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	FROM XCVR	B1	TX_UHB_IN1	TO UHBPAD
50_TX_IN_TX2_UHB_PAD_TX_N79_IN	FROM XCVR	B12	TX_N79_IN1	TO UHBPAD
50_UHB_L_CPLR_OUT	TO XCVR	E12	FBRX1	

50_RX_XCVR_PRX16_UHB_RX_OUT1	TO XCVR	A3	RX_OUT1	50_RX_UHB_PAD_UHB_RX_OUT_1
50_RX_XCVR_PRX14_N79_RX_OUT1	TO XCVR	A4	RX_OUT2	50_RX_UHB_PAD_N79_RX_OUT_1
50_RX_XCVR_PRX17_UHB_RX_OUT2	TO XCVR	A8	RX_OUT3	50_RX_UHB_PAD_UHB_RX_OUT_2
50_RX_XCVR_PRX15_N79_RX_OUT2	TO XCVR	A9	RX_OUT4	50_RX_UHB_PAD_N79_RX_OUT_2

R2204_E 0.00 0% 1/32W MF 01005 UHB_LAT
R2205_E 0.00 0% 1/32W MF 01005 UHB_LAT
R2203_E 0.00 0% 1/32W MF 01005 UHB_LAT
R2206_E 0.00 0% 1/32W MF 01005 UHB_LAT

UHB_ANT1	M2	50_TRX_PAUHBL_UHB_ANT1_TO_ANT7
UHB_ANT2	M3	50_TRX_PAUHBL_UHB_ANT2_TO_ANT9
UHB_ANT4	M5	50_TRX_UHB_PAD_PORTB_TX
N79_ANT1	M7	50_TRX_PAUHBL_N79_ANT1_TO_ANT7
N79_ANT2	M8	50_TRX_PAUHBL_N79_ANT2_TO_ANT9
N79_ANT4	M10	50_TRX_UHB_PAD_N79_PORTB_TX

TO UHB/N79 DPLX -> ANT7

UHB_LAT 152S00496 R2209_E 0.6NH-+/-0.1NH-0.95A-0.05OHM 01005
50_TRX_UHB_PAD_PORTB_TX_M
TO UHB UAT PAD UHB ANT 4
UHB_LAT C2210_E 3.0NH-+/-0.1NH-0.45A-0.20HM 01005 NOSTUFF

R2208_E 0.00 0% 1/32W MF 01005 UHB_LAT
50_TRX_UHB_PAD_N79_PORTB_TX_M
TO UHB UAT PAD N79 ANT4
152S00428 C2209_E 2.1NH-+/-0.1NH-0.65A 01005 UHB_LAT

EXT_CPL1 J12 NC
EXT_CPL2 L12 NC

PP_1V8_LDO6
C2202_E 18PF 5% 16V NP0/C0G 01005 UHB_LAT

PAUHBL_E
SKY58245-17
DSBGA
SYM 2 OF 2
PART_NUMBER=353S02389
SHIELD=YES
ROOM=UHB_LAT

CRITICAL

A1	GND	GND	E6
A2	GND	GND	E7
A5	GND	GND	E8
A6	GND	GND	E10
A7	GND	GND	E11
A11	GND	GND	F1
A10	GND	GND	F2
A12	GND	GND	F3
B2	GND	GND	F4
B3	GND	GND	F5
B4	GND	GND	F6
B5	GND	GND	F8
B6	GND	GND	F9
B7	GND	GND	F10
B8	GND	GND	F11
B9	GND	GND	F12
B10	GND	GND	G1
B11	GND	GND	G2
C1	GND	GND	G3
C2	GND	GND	G4
C3	GND	GND	G5
C5	GND	GND	G6
C8	GND	GND	G8
C10	GND	GND	G9
C11	GND	GND	G10
C12	GND	GND	G11
D1	GND	GND	G12
D2	GND	GND	H1
D3	GND	GND	H12
D5	GND	GND	J1
D6	GND	GND	K1
D7	GND	GND	K12
D8	GND	GND	L1
D10	GND	GND	M1
D11	GND	GND	M4
D12	GND	GND	M6
E1	GND	GND	M9
E2	GND	GND	M11
E3	GND	GND	M12
E5	GND		

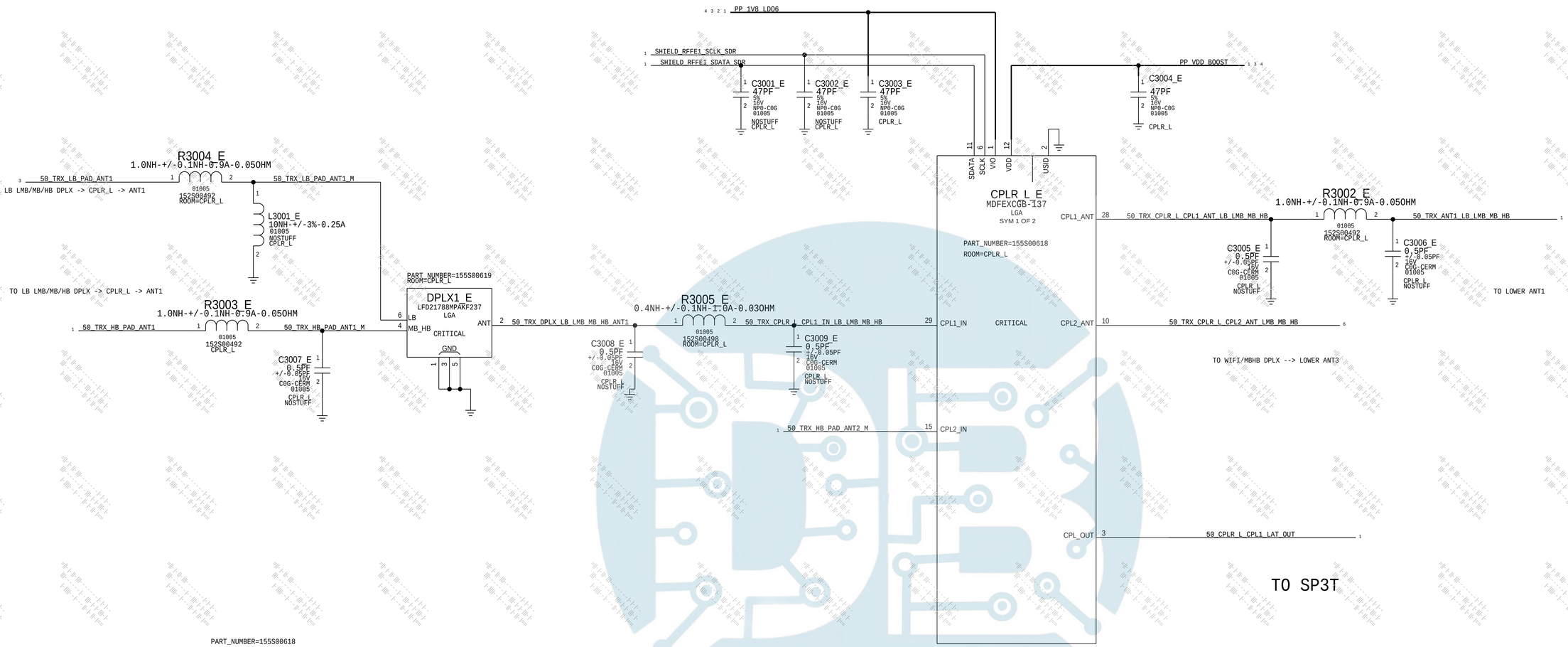
CDS_LIB=apple

SYNC_DATE=08/01/2019

PAGE TITLE	UHB LAT PAD
DRAWING NUMBER	
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	22 OF 40
SHEET	106 OF 117

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE ONLY - NOT A CHANGE REQUEST

LOWER COUPLER



SYNC_DATE=08/01/2019

PAGE TITLE
COUPLER LOWER

DRAWING NUMBER 051-05170
SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 30 OF 40
SHEET 107 OF 117

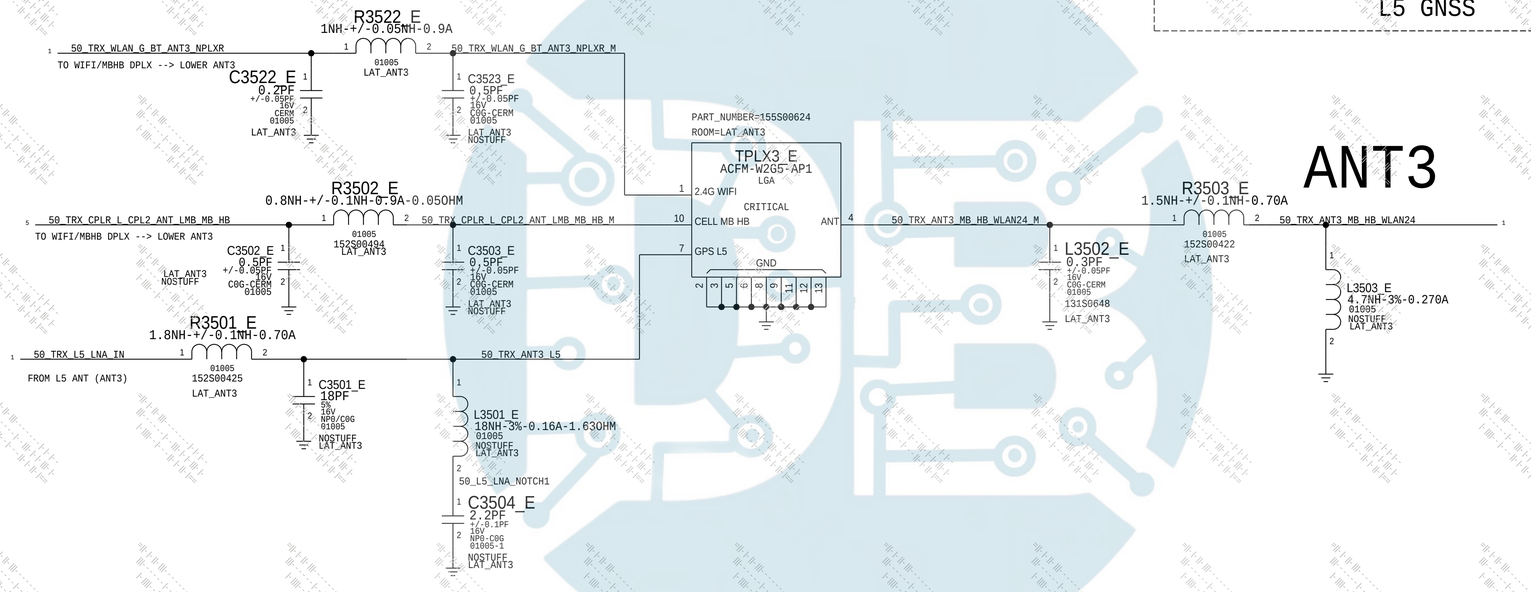
LOWER ANTENNA FEEDS: ANT3

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

SYNC_DATE=08/01/2019

PAGE TITLE
LOWER ANTENNA FEEDS_ANT3

DRAWING NUMBER 051-05170 | SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 35 OF 40
SHEET 108 OF 117

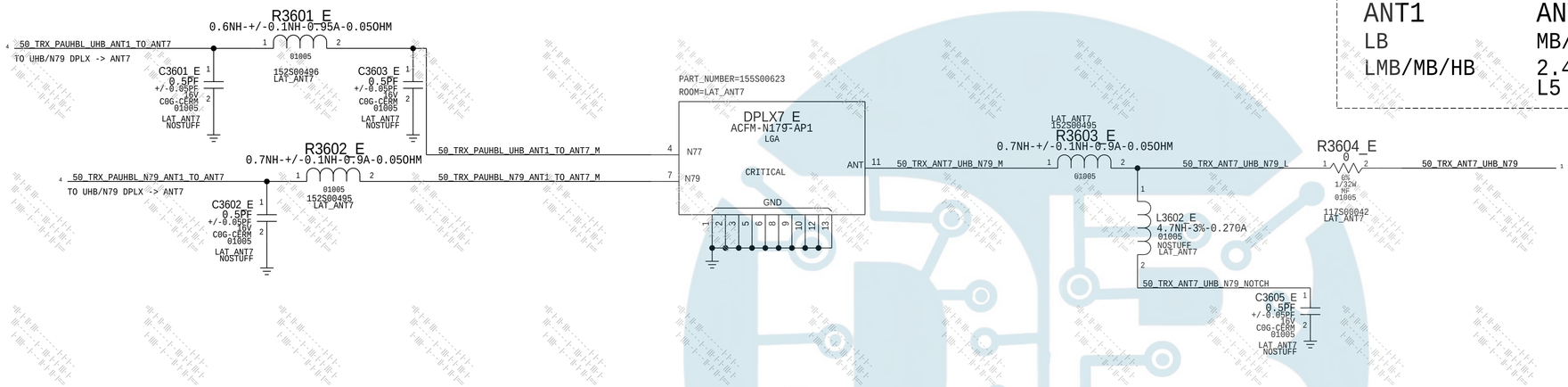
LOWER ANTENNA FEEDS: ANT7

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



ANT7

5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

SYNC_DATE=08/01/2019

PAGE TITLE
LOWER ANTENNA FEEDS_ANT7

DRAWING NUMBER 051-05170 | SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 36 OF 40
SHEET 109 OF 117

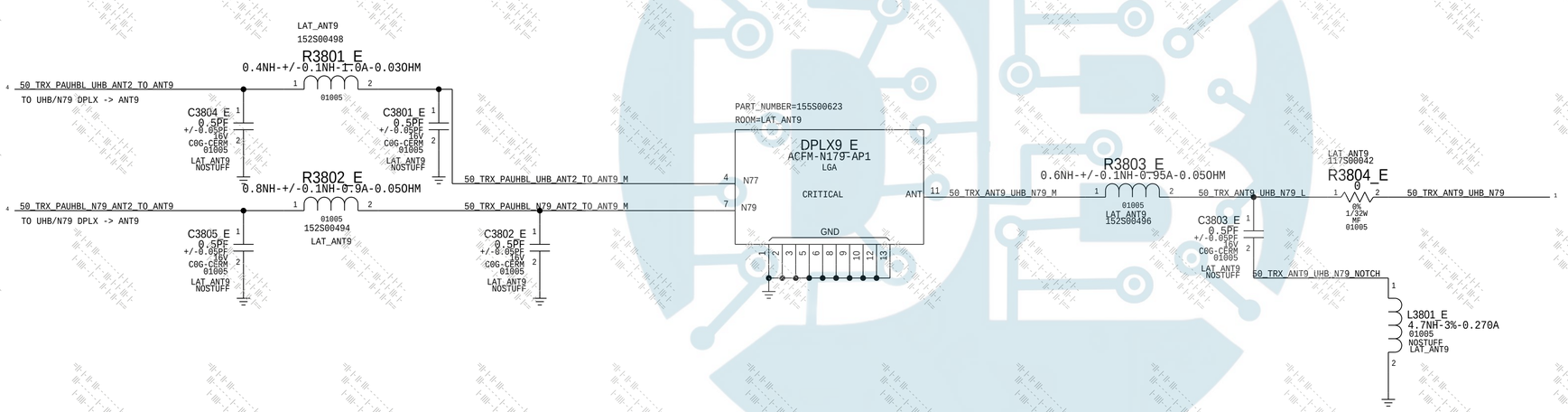
LOWER ANTENNA FEEDS: ANT9

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



ANT9

5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

SYNC_DATE=08/01/2019

PAGE TITLE

LOWER ANTENNA FEEDS_ANT9

DRAWING NUMBER 051-05170 | SIZE D

REVISION 10.0.0

BRANCH 1

PAGE 38 OF 40

SHEET 110 OF 117

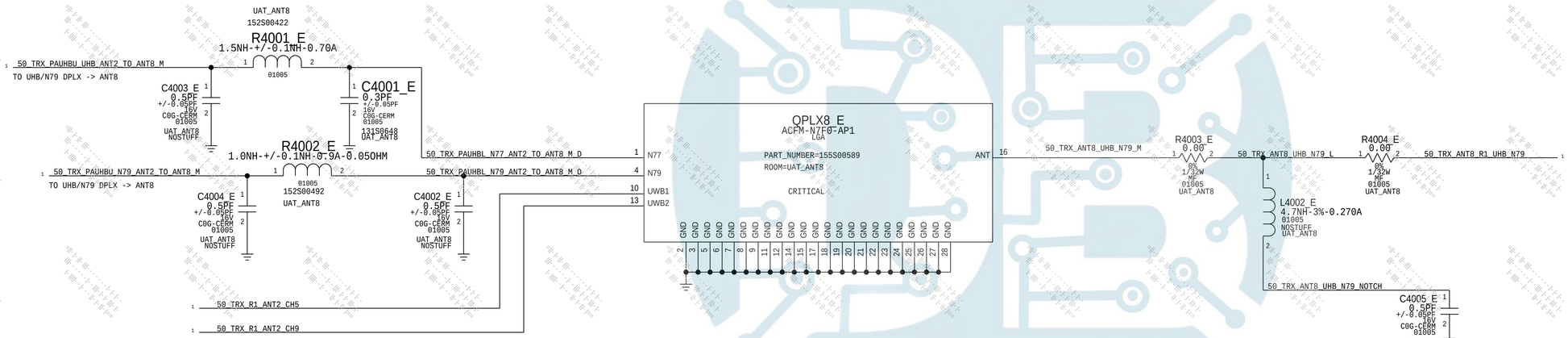
UPPER ANTENNA FEEDS: ANT8

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ L5 GNSS		N79	N79



ANT8

5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

SYNC_DATE=10/02/2019

PAGE TITLE
UPPER ANTENNA FEEDS_ANT8

DRAWING NUMBER 051-05170 | SIZE D
REVISION 10.0.0
BRANCH 1
PAGE 40 OF 40
SHEET 111 OF 117

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

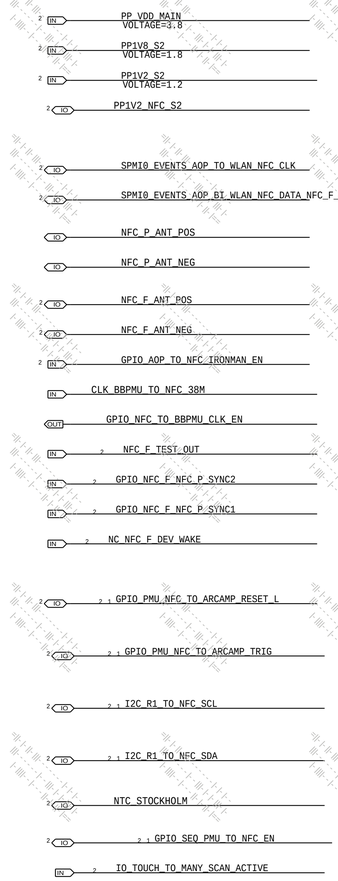
REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0024125573	ENGINEERING RELEASED	2020-07-01

HIER_NFC D54 TOP

LAST_MODIFICATION=Wed Jul 1 16:52:55 2020

D54 FURY MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00019	2	CAP,CER,C0G,150PF,2%, 50V,0201	C7510_I,C7513_I	?
131S0882	2	CAP,CER,C0G,390PF,2%25V,0201	C7550_I,C7551_I	?
152S01116	2	IND,82NH,2.5%,0.55A,0402	L7500_I,L7501_I	?
131S0825	2	CAP,CER,C0G,560PF,2%,25V,0201	C7515_I,C7543_I	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7514_I,C7542_I	?
131S0883	2	CAP,CER,C0G,220PF,2%,25V,0201	C7512_I,C7541_I	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7545_I,C7565_I	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7546_I,C7566_I	?
131S00026	2	CAP,CER,C0G,820PF,2%,25V,0201	C7547_I,C7567_I	?
131S00026	2	CAP,CER,C0G,820PF,2%,50V,0201	C7548_I,C7568_I	?



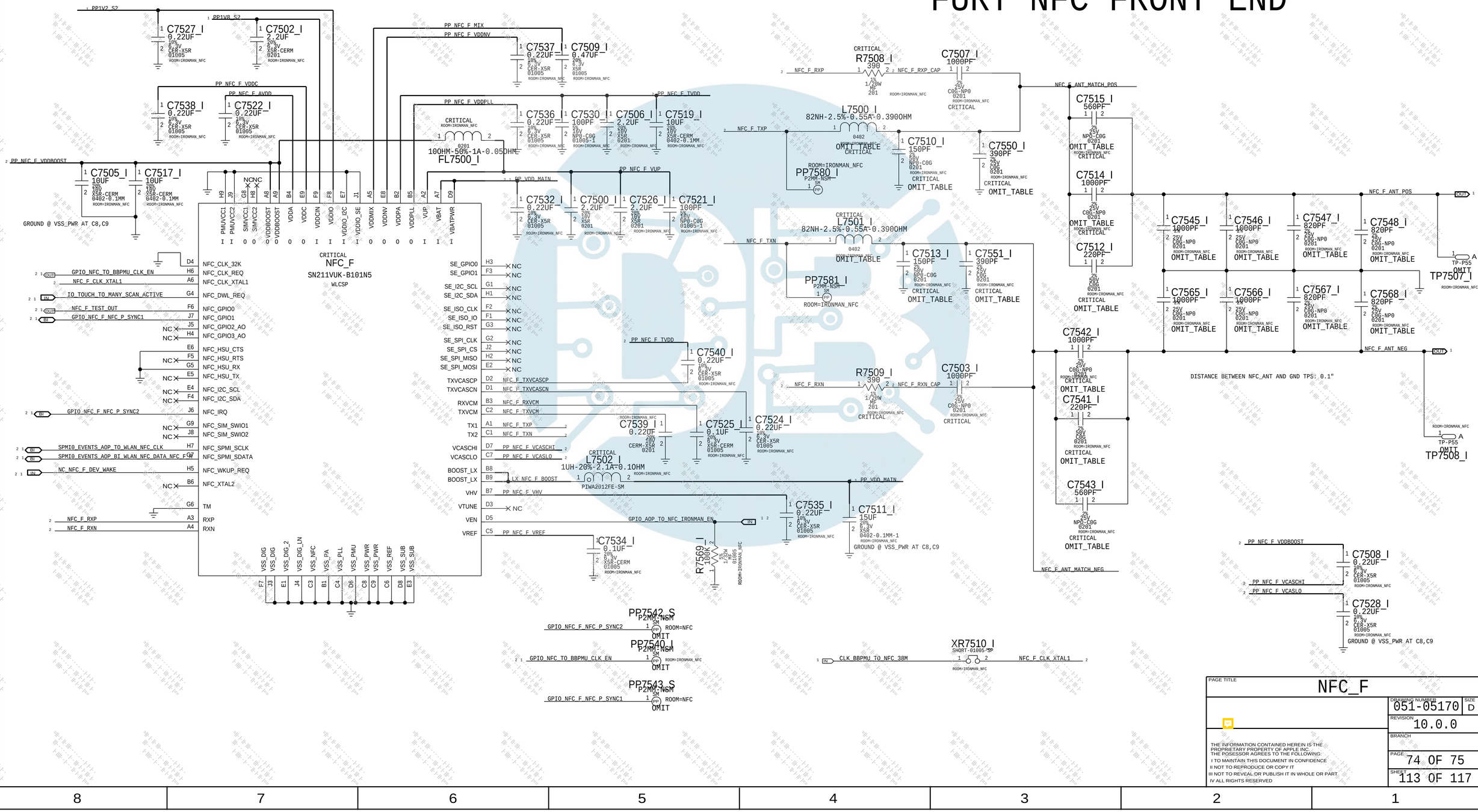
NFC: TABLE OF CONTENTS

DRAWING TITLE	SCH,TOP,D54
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	
PAGE	1 OF 75
SHEET	112 OF 117

STOCKHOLM

FURY NFC CONTROLLER

FURY NFC FRONT END



PAGE TITLE	NFC_F
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	
PAGE	74 OF 75
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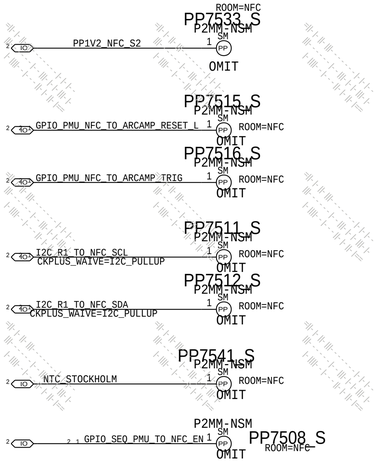

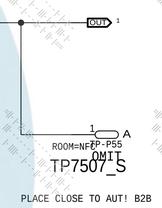

PAGE TITLE	NFC_P_CP
DRAWING NUMBER	051-05170
SIZE	D
REVISION	10.0.0
BRANCH	1
PAGE	75 OF 75
SHEET	114 OF 117

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0024125573	ENGINEERING RELEASED	2020-07-01

D54 / HIER_WIFI_TOP

LAST_MODIFICATION=Wed Jul 1 16:52:54 2020

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/SOFT	SYNC_DATE/TIME
D52	WIFI_MASTER	4,5	0.17.0	S	2019_09_04_14:14:04

WLAN SYMBOL IO PORTS

POWER

- PP_VDD_MAIN — VOLTAGE=3.8
- PP1V8_S4 — VOLTAGE=1.8
- PP_VDD_MAIN — VOLTAGE=3.8
- PP1V8_S2 — VOLTAGE=1.8

5GHz rFEM (UAT)

- 50_WLAN_A_C0_TXRX_FEM_M
- 50_LAA_RX_XCVR_DRX10
- SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
- SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
- RFFE_WLAN_TO_UAT_5G_FEM_RST_L
- GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN
- SHIELD_RFFE5_SCLK_SDR
- SHIELD_RFFE5_SDATA_SDR
- PP_1V8_LDO6
- ANALOG_UAT_5G_FEM_TO_WLAN_PDTS
- 50_TRX_ANT6_WLAN_A_LAA

5GHz rFEM (LAT)

- 50_WLAN_A_C1_TXRX_FEM_M
- 50_LAA_RX_XCVR_PRX12
- SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK
- SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA
- RFFE_WLAN_TO_LAT_5G_FEM_RST_L
- GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN
- SHIELD_RFFE3_SCLK_SDR
- SHIELD_RFFE3_SDATA_SDR
- PP_1V8_LDO6
- ANALOG_LAT_5G_FEM_TO_WLAN_PDTS
- 50_TRX_ANT5_WLAN_A_LAA

SCHEMATIC APN: 951-10744

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SYNC_DATE=05/08/2018

DRAWING TITLE: SCH,TOP,D54

DRAWING NUMBER: 051-05170 | SIZE: D

REVISION: 10.0.0

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PAGE: 1 OF 5

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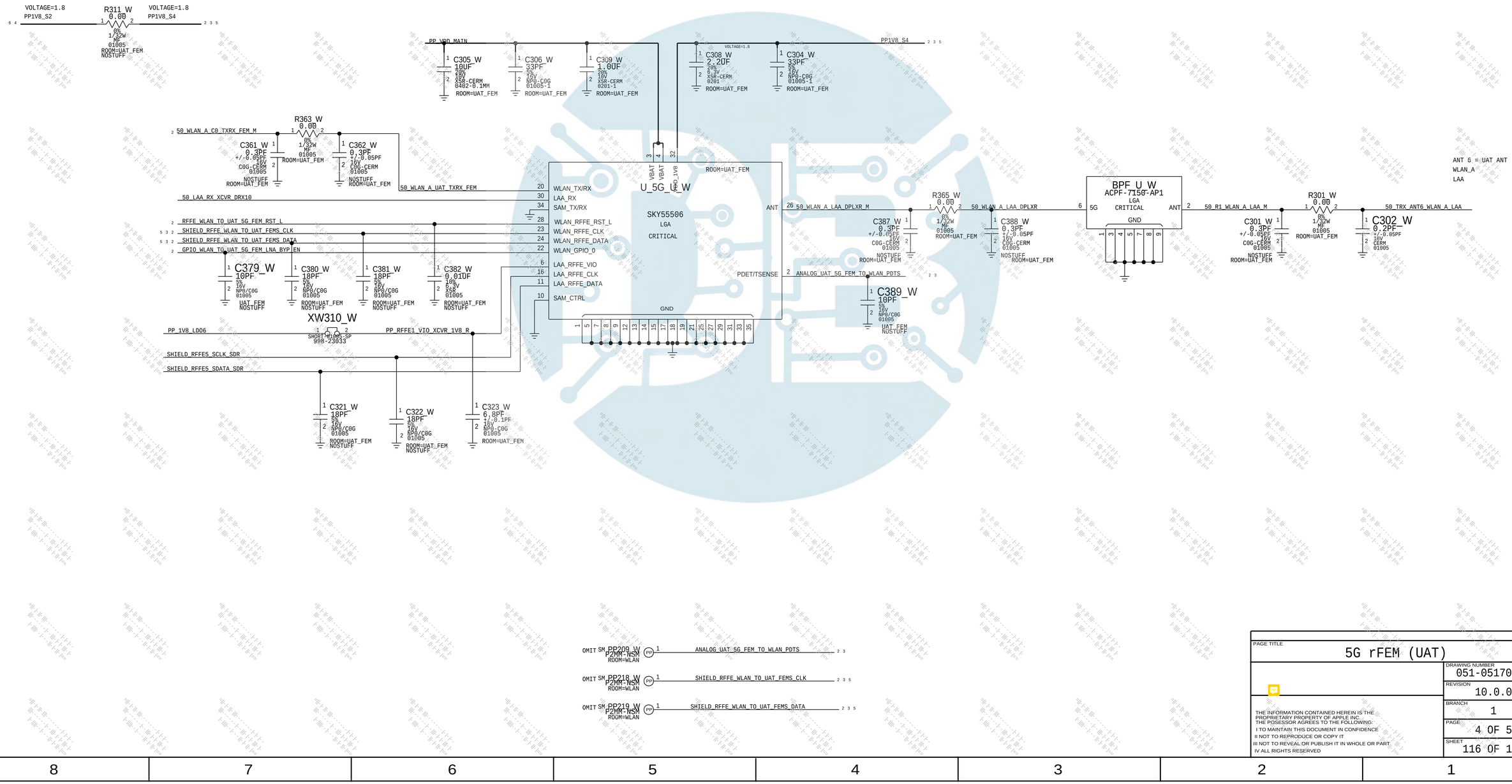
UAT 5GHZ RFEM



PAGE TITLE: 5G rFEM (UAT)

DRAWING NUMBER: 051-05170
SIZE: D
REVISION: 10.0.0
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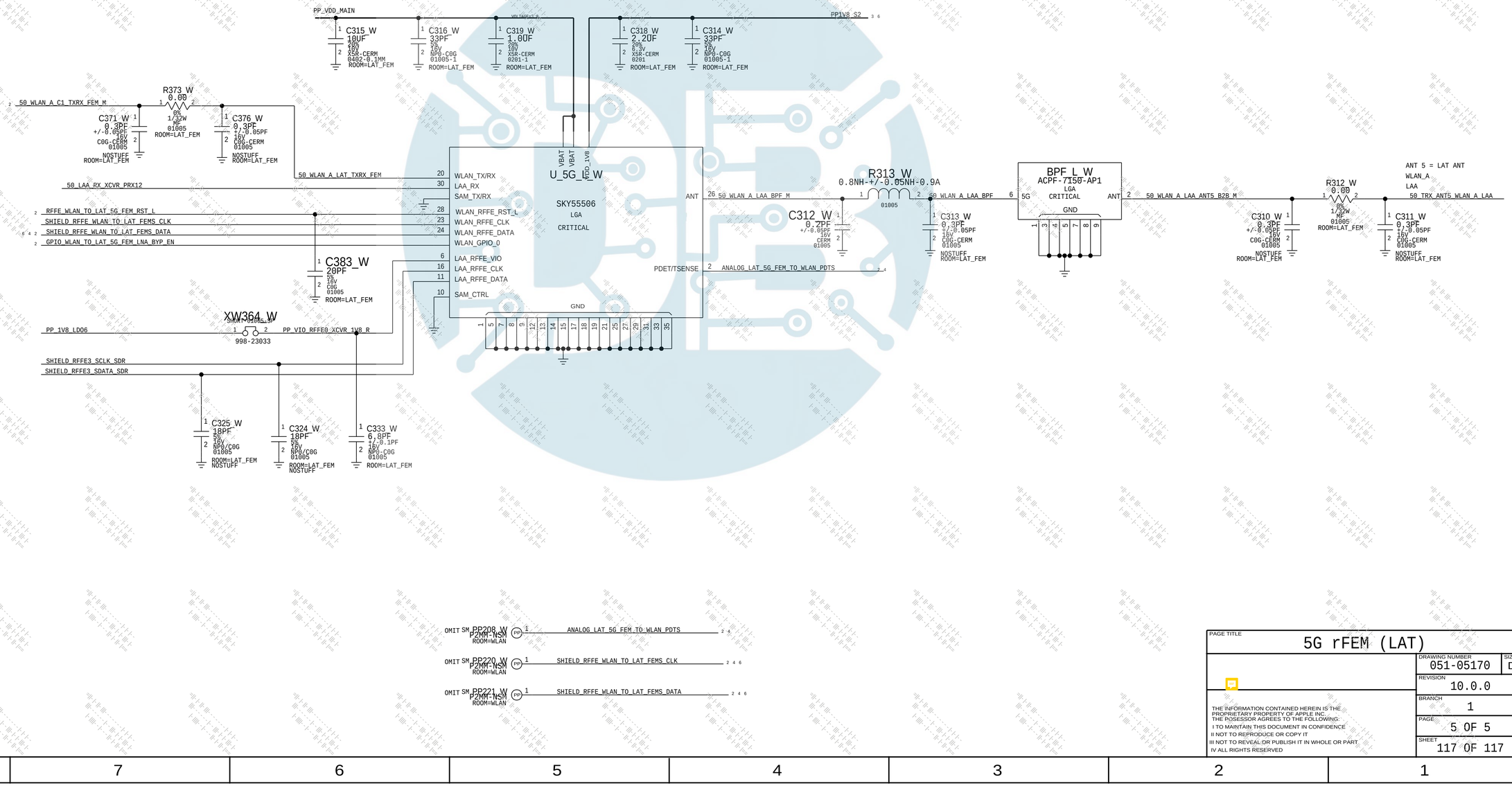
SHEET: 116 OF 117

LAT 5GHZ RFEM



PAGE TITLE: 5G rFEM (LAT)

DRAWING NUMBER: 051-05170
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BRANCH: 1
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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

D54 BOT MAV

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0024124377	ENGINEERING RELEASED	2020-07-01

LAST_MODIFICATION=Wed Jul 1 15:22:42 2020

APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-05263	1	SCH,BOT,MAV,D54	SCH	CRITICAL ?	
820-01971	1	PCB,BOT,MAV,D54	PCB	CRITICAL ?	

Sub-designs

Hierarchies

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/ SOFT	SYNC_DATE/TIME	FORCE SUBDESIGN
D54	HIER_RADIO_MAV_BOT	3.61.0	S	2020_06_26_15:43:07	N
D54	HIER_NFC_BOT	0.23.0	S	2020_06_26_12:24:47	N
D54	HIER_WIFI_BOT	0.12.0	S	2020_06_26_12:33:04	N

Pages

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D52	AP_MASTER	50	tmp	S	2020_07_01_14:57:41

Packaging Options

PACK_OPTIONS TO INCLUDE IN NETLIST
D54

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SYNC_MASTER=doe_panini SYNC_DATE=05/15/2018

DRAWING TITLE: SCH,BOT,MAV,D54

DRAWING NUMBER: 051-05263 SIZE: D

REVISION: 9.0.0

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Global Capacitors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1103	138S0719	?	ALL	CAP,X5R,4.7UF,20%,10V,0402,TAIYO

CRITICAL PART#	COMMENT
138S0719	CAP,X5R,4.7UF,20%,10V,0402,MURATA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00133	138S00128	?	ALL	CAP,X5R,0.47UF,20%,6.3V,01005,MURATA
138S00269	138S00128	?	ALL	CAP,X5R,0.47UF,20%,6.3V,01005,TAIYO
138S00269	138S00133	?	ALL	CAP,X5R,0.47UF,20%,6.3V,01005,TAIYO

CRITICAL PART#	COMMENT
138S00128	CAP,X5R,0.47UF,20%,6.3V,01005,KYOCERA
138S00133	CAP,X5R,0.47UF,20%,6.3V,01005,MURATA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00185	132S0316	?	ALL	CAP,X5R,0.1UF,20%,6.3V,01005

CRITICAL PART#	COMMENT
132S0316	CAP,X5R,0.1UF,20%,6.3V,01005

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	?	ALL	CAP,X5R,15UF,20%,6.3V,0402,KYOCERA

CRITICAL PART#	COMMENT
138S00003	CAP,X5R,15UF,20%,6.3V,0402,MURATA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S0945	138S0706	?	ALL	CAP,CER,X5R,1UF,20%,10V,0201,KYOCERA

CRITICAL PART#	COMMENT
138S0706	CAP,X5R,1UF,20%,10V,0201

22uF, 0402 3T (WiFi)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00024	138S0986	?	ALL	CAP,CER,3-TERM,7.5UF,20%,4V,0402

CRITICAL PART#	COMMENT
138S0986	CAP,CER,3-TERM,7.5UF,20%,4V,0402

33PF, 0201 (NFC)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
131S00377	131S0823	?	ALL	CAP,CER,3-TERM,7.5UF,20%,4V,0402

CRITICAL PART#	COMMENT
131S0823	CAP,CER,NP0/C0G,33PF,+/-2%,25V,0201

MAV20 PDN Single-source

0.22uF, 01005

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00233	132S00014	?	[SEE BELOW]	01005,0.22UF,6.3V,Taiyo
132S00304	132S00014	?	[SEE BELOW]	01005,0.22UF,6.3V,Kyocera

CRITICAL PART#	COMMENT
132S00014	01005,0.22UF, 6.3V

(C706,E-C720,E-C723,E-C725,E-C727,E-C730,E-C731,E-C734,C-C736,E-C742,E-C744,E-C749,E-C751,E-C754,E-C760,E-C766,E-C767,E-C770,E-C772,E-C774,E-C776,E-C778,E-C780,E)
(C706,E-C720,E-C723,E-C725,E-C727,E-C730,E-C731,E-C734,E-C736,E-C742,E-C744,E-C749,E-C751,E-C754,E-C760,E-C766,E-C767,E-C770,E-C772,E-C774,E-C776,E-C778,E-C780,E)

2.2uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00049	138S0831	?	[SEE BELOW]	CAP,CER,X5R,2.2UF,20%,6.3V,0201

CRITICAL PART#	COMMENT
138S0831	CAP,CER,X5R,2.2UF,20%,6.3V,0201

(C701,E-C702,E-C704,E-C723,E-C732,E-C735,E-C728,E-C729,E-C732,E-C733,E-C739,E-C743,E-C745,E-C746,E-C747,E-C748,E-C752,E-C760,E-C768,E-C769,E-C773,E-C777,E-C785,E)

4uF, 0201

All RefDes in ( ) are single-sourced from Murata

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,TAIYO
138S00117	138S00071	?	[SEE BELOW]	CAP,X5R,4UF,0201,0.55MM,KYOCERA

CRITICAL PART#	COMMENT
138S00071	CAP,X5R,4UF,20%,6.3V,0201,MURATA

(C435,E,C511,E-C518,E,C522,E,C524,E-C526,E,C702,E,C760,E,C769,E,C777,E,C787,E,C788,E,C1135,E-C1142,E,C1226,E,C1227,E,C5801,E-C5803,E,C5823,E,C5827,E,C5828,E)
(C435,E,C511,E-C518,E,C522,E,C524,E-C526,E,C702,E,C760,E,C769,E,C777,E,C787,E,C788,E,C1135,E-C1142,E,C1226,E,C1227,E,C5801,E-C5803,E,C5823,E,C5827,E,C5828,E)

22uF, 0201

All RefDes in ( ) are single-sourced from Samsung

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00144	138S00279	?	ALL	CAP,X5R,22UF,0402,20%,4V,MURATA
138S00143	138S00279	?	[SEE BELOW]	CAP,X5R,22UF,0402,20%,4V,KYOCERA

CRITICAL PART#	COMMENT
138S00279	CAP,X5R,22UF,20%,4V,0402,SAMSUNG

(C499,E,C429,E-C434,E,C523,E)

EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR 639-08664	MVW3	CRITICAL	EEEE:08664
825-7691	1	EEEE FOR 639-10114	NY9L	CRITICAL	EEEE:10114
825-7691	1	EEEE FOR 639-10759	PP6P	CRITICAL	EEEE:10759

Global Inductors/Diodes

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00437	155S00402	?	ALL	FERR BD,330HM,25%,1.5A,55MOHM DCR,0201
155S00400	155S00200	?	ALL	FERR BD,150OHM,25%,200MA,0.7OHM DCR,01005
371S00062	371S00101	?	ALL	DIODE,SCHOTTKY,30V,250MW,0201
377S00061	377S0183	?	ALL	TVS,BIDIR,5.0V,0201
377S00173	377S0183	?	ALL	TVS,BIDIR,5.0V,0201
377S0168	377S00129	?	ALL	SUPRESS,TRANS,6.8V,100PF,AMOTECH,01005
152S00872	152S00918	?	ALL	IDE,INC-MLD,0.47UH,5.6A,30MO,2016
152S00847	152S00918	?	ALL	CYNTEC,INC-MLD,0.47UH,5.6A,20MO,2016

CRITICAL PART#	COMMENT
155S00402	FERR BD,33OHM,25%,1.5A,55MOHM DCR,0201
155S00200	FERR BD,150OHM,25%,200MA,0.7OHM DCR,01005
371S00101	DIODE,SCHOTTKY,30V,100MA,250MW,0201
377S0183	TVS,BIDIR,5.0V,0201
CRITICAL PART#	COMMENT
377S00129	SUPRESS,TRANS,6.8V,100PF,01005

Thermistor

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0245	107S0244	?	ALL	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

CRITICAL PART#	COMMENT
107S0244	THERMISTOR,NTC,100K OHM,1%,B=4250,01005

Multi-Vendor Criticals

CRITICAL PART#	COMMENT
377S0106	SUPPR,TRANS,VARISTOR,12V,33PF,01005
197S0446	XTAL,24MHZ,30PPM,9.5PF,60 OHM MAX,1612
155S0576	FERR BD,10 OHM,50%,750MA,0.07 DCR,01005
155S00168	FLTR,NOISE,65 OHMZ,3.4OHM,0.7-2GHZ,0605
138S0979	CAP,CER,X5R,10UF,20%,10V,0402,H=0.65MM
138S0692	CAP,CER,X5R,1UF,20%,6.3V,0201
138S0683	CAP,CER,X5R,1UF,10%,25V,0402
138S0652	CAP,CER,X5R,4.7UF,20%,6.3V,H=0.65MM,0402
138S00070	CAP,X5R,4.7UF,20%,25V,0402
138S00014	CAP,CER,1UF,20%,16V,X5R,0201,H=0.39MM
132S0064	CAP,CER,0.047UF,10%,25V,X5R,0201
132S0663	CAP,CER,X5R,1UF,10%,25V,0402
132S0534	CAP,CER,X5R,0.1UF,10%,25V,0201
132S0396	CAP,CER,X5R,1000PF,10%,10V,01005

CRITICAL PART#	COMMENT
132S0288	CAP,CER,X5R,0.1UF,10%,16V,0201
132S0275	CAP,CER,X5R,470PF,10%,10V,01005
132S0249	CAP,CER,X7R,220PF,10%,10V,01005
132S0245	CAP,CER,X5R,0.01UF,10%,6.3V,01005
132S00093	CAP,X5R,0.022UF,20%,6.3V,01005
132S00025	CAP,CER,X5R,0.047UF,20%,6.3V,01005
132S00008	CAP,CER,0.1UF,10%,50V,X7R,0402
131S0883	CAP,CER,NP0/C0G,220PF,2%,50V,0201
131S0804	CAP,CER,27PF,5%,C0G,25V,0201
131S0307	CAP,CER,NP0/C0G,100PF,5%,16V,01005
131S0225	CAP,CER,NP0/C0G,15PF,5%,16V,01005
131S0223	CAP,CER,NP0/C0G,27PF,5%,16V,01005
131S0220	CAP,CER,NP0/C0G,12PF,5%,16V,01005
131S0216	CAP,CER,NP0/C0G,47PF,5%,16V,01005

CRITICAL PART#	COMMENT
155S00341	FERR BD,240 OHM,25%,200MA,0.9 DCR,01005
131S00170	CAP,CER,C0G,220PF,5%,25V,01005
131S0215	CAP,CER,NP0/C0G,22PF,5%,16V,01005
131S0643	CAP,CER,NP0/C0G,56PF,5%,25V,01005
107S0257	THERMISTOR,NTC,10K OHM,1%,B=3435,01005
132S0318	CAP,CER,X5R,820PF,10%,10V,01005
117S0055	RES,MF,1/20W,2M OHM,5,0201,SMD
132S0296	CAP,CER,X5R,1000PF,10%,6.3V,01005
118S00068	RES,MF,1.3 MOHM,1%,200PPM,1/20W,0201
132S0304	CAP,CER,X5R,0.22UF,20%,6.3V,0201
131S00053	CAP,CER,C0G,220PF,5%,10V,01005
131S00323	CAP,CER,NP0/C0G,56PF,5%,25V,01005
131S00303	CAP,CER,NP0/C0G,100PF,5%,16V,01005
131S00353	CAP,CER,NP0/C0G,10PF,5%,16V,01005

PAGE TITLE

SYSTEM: BOM Tables

DRAWING NUMBER 051-05263 | SIZE D

REVISION 9.0.0

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90-ohm Diff Pair Constraints

Electrical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
QLINK (RF)	E_QLINK_SUB6	E	DIFF_PAIR_QLINK-SUB6	DP:DP_85_SUB6_QLINK_*	Y
	E_QLINK_MMW	E	DIFF_PAIR_QLINK-MMW	DP:DP_85_MMW_QLINK_*	Y
PCIe	E_PCIE_BB	E	DIFF_PAIR	DP:DP_90_PCIE_GP2_AP_*_BB_*	Y
	E_PCIE_WLAN	E	DIFF_PAIR	DP:DP_90_PCIE_GP1_AP_*_WLAN_*	Y
	E_USB_BB	E	DIFF_PAIR	DP:DP_90_USB_BB	Y

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
85-ohm	85_QLINK_SUB6	P	A_85_OHM_DIFF	DP:DP_85_SUB6_QLINK_*	Y
	85_QLINK_MMW	P	A_85_OHM_DIFF	DP:DP_85_MMW_QLINK_*	Y
	90_PCIE_BB	P	A_90_OHM_DIFF	DP:DP_90_PCIE_GP2_AP_*_BB_*	Y
90-ohm	90_PCIE_WLAN	P	A_90_OHM_DIFF	DP:DP_90_PCIE_GP1_AP_*_WLAN_*	Y
	90_USB_BB	P	A_90_OHM_DIFF	DP:DP_90_USB_BB	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
85-ohm	85_QLINK_SUB6	S	A_DIELECTRIC_3X	=	Y
	85_QLINK_MMW	S	A_DIELECTRIC_3X	=	Y
	90_PCIE_BB	S	A_DIELECTRIC_3X	=	Y
90-ohm	90_PCIE_WLAN	S	A_DIELECTRIC_3X	=	Y
	90_USB_BB	S	A_DIELECTRIC_3X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
90_PCIE_BB	GND	A_DIELECTRIC_2X
90_PCIE_WLAN	GND	A_DIELECTRIC_2X

Custom mmW Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
mmW IF	50_MMW_IF	P	50_OHM_MMW_IF_SE	50_MMW_*IFH*, 50_MMW_*IFV*	Y
mmW RF	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S1H_HPOL,50_MMW_SMR525_S1L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S2H_HPOL,50_MMW_SMR525_S2L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S5H_HPOL,50_MMW_SMR525_S5L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S6H_HPOL,50_MMW_SMR525_S6L_HPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S7H_HPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S7L_HPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S9H_VPOL,50_MMW_SMR525_S9L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S10H_VPOL,50_MMW_SMR525_S10L_VPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S11H_VPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S11L_VPOL	Y
	50_MMW_SMYRNA_HB_RF	P	50_OHM_MMW_SMYRNA_HB_SE	50_MMW_SMR525_S12H_VPOL	Y
	50_MMW_SMYRNA_LB_RF	P	50_OHM_MMW_SMYRNA_LB_SE	50_MMW_SMR525_S12L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S13H_VPOL,50_MMW_SMR525_S13L_VPOL	Y
	50_MMW_RF	P	50_OHM_MMW_SE	50_MMW_SMR525_S14H_VPOL,50_MMW_SMR525_S14L_VPOL	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
mmW IF	50_MMW_IF	S	DIELECTRIC_4XV_50_MMW_IF_SE	=	Y
mmW RF	50_MMW_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y
	50_MMW_SMYRNA_HB_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y
	50_MMW_SMYRNA_LB_RF	S	DIELECTRIC_4XV_50_WIDE_MMW_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_MMW_IF	GND	DIELECTRIC_2X_50_MMW_IF_SE
50_MMW_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SE
50_MMW_SMYRNA_HB_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SMYRNA_HB_SE
50_MMW_SMYRNA_LB_RF	GND	DIELECTRIC_2X_50_WIDE_MMW_SMYRNA_LB_SE

Spacing CSet Definitions

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_{N}X Calculates dielectric distance from stackup, shortest distance is used unless 'L' is defined	EXAMPLE: 1,2.5,3,8; 0A; 10A 1.5,2,2.5,3,8
A_DIELECTRIC_{N}XD XV,XVL,X Calculates dielectric distance from Hybrid Table and stackup, shortest distance is used unless 'L' defined	EXAMPLE: 2 GHz, 3GHz, 5 GHz PLEASE USE HYBRID TABLE
A_DIELECTRIC_{N}XIN_{N}XOUT Calculates dielectric distance from stackup, shortest distance is used unless 'L' is defined	EXAMPLE: 1_4.5A_3L ?

AP Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
LX/CX Nodes	PWR_SHAPE	P	PWR_SHAPE	LX*	Y
System-Wide	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_MAIN	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_VDD_BOOST	Y
	PWR_200UM	P	PWR_200UM	PP1V8_S2	?
	PWR_200UM	P	PWR_200UM	PP1V8_S4	Y
	PWR_100UM	P	PWR_100UM	PP1V2_S2	Y
	PWR_100UM	P	PWR_100UM	PP1V2_S4	Y
	PWR_100UM	P	PWR_100UM	PP3V0_S2*	Y
	PWR_100UM	P	PWR_100UM	PP_VBUS1_E75	Y

RF Physical

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
WiFi/Misc.	PWR_100UM	P	PWR_100UM	PP_VDD_BTPA3V3	Y
	PWR_100UM	P	PWR_100UM	PP1V8_LAT_2G_FEM	Y
	PWR_100UM	P	PWR_100UM	PP3V0_DEBUG	Y
SMPS 1/6	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS1_6	Y
SMPS 2	PWR_SHAPE	P	PWR_SHAPE	PP_1V22_SMPS2	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_1V24_SMPS2_SNS	Y
SMPS 3	PWR_SHAPE	P	PWR_SHAPE	PP_0V82_SMPS3	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V82_SMPS3_SNS	Y
SMPS 4	PWR_SHAPE	P	PWR_SHAPE	PP_1V9_SMPS4	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_1V9_SMPS4_SNS	Y
SMPS 5	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS5	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V75_SMPS5_SNS	Y
SMPS 7	PWR_SHAPE	P	PWR_SHAPE	PP_0V75_SMPS7	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V75_SMPS7_SNS	Y
LDO1	PWR_SHAPE	P	PWR_SHAPE	PP_1V2_LDO1	Y
	PWR_500UM	P	PWR_500UM	PP_1V2_LDO1_SDR_VDDAM_RP, PP_1V2_LDO1_SDR_VDDAM_RX	Y
	PWR_300UM	P	PWR_300UM	PP_LDO1_SDR_VDDAM_BBRX_BOT_215	Y
	PWR_200UM	P	PWR_200UM	PP_1V2_LDO1_SDR_VDDAM_TX	Y
	PWR_200UM	P	PWR_200UM	PP_LDO1_SDR_VDDAM_RX0_171, PP_LDO1_SDR_VDDAM_RX5_138	Y
	PWR_100UM	P	PWR_100UM	PP_1V2_LDO1_SDR_VDDAM_TP, PP_LDO1_SDR_VDDAM_BBRX_TOP_97	Y
	PWR_80UM	P	PWR_80UM	PP_LDO1_SDR_VDDAM_RP*_57, PP_LDO1_SDR_VDDAM_TX*_40	Y
	PWR_50UM	P	PWR_50UM	PP_LDO1_SDR_VDDAM_*P*_30	Y
LDO2	PWR_500UM	P	PWR_500UM	PP_1V1_LDO2	Y
LDO3	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO3	Y
	PWR_500UM	P	PWR_500UM	PP_0V8_LDO3_SDR_VDDAL_DIG	Y
	PWR_500UM	P	PWR_500UM	PP_0V8_LDO3_SDR_VDDAL_RP*, PP_0V8_LDO3_SDR_VDDAL_RX_*	Y
	PWR_300UM	P	PWR_300UM	PP_LDO3_SDR_VDDAL_DIG1_171	Y
	PWR_200UM	P	PWR_200UM	PP_LDO3_SDR_VDDAL_DIG2_124	Y
	PWR_100UM	P	PWR_100UM	PP_0V8_LDO3_SDR_VDDAL_RXLO*	Y
	PWR_100UM	P	PWR_100UM	PP_0V8_LDO3_SDR_VDDAL_TP, PP_0V8_LDO3_SDR_VDDAL_TX	Y
	PWR_100UM	P	PWR_100UM	PP_LDO3_SDR_VDDAL_RP*_57	Y
	PWR_100UM	P	PWR_100UM	PP_LDO3_SDR_VDDAL_RX0_67, PP_LDO3_SDR_VDDAL_RX6_90	Y
	PWR_80UM	P	PWR_80UM	PP_0V8_LDO3_SDR_VDDAL_DIG_RP*	Y
	PWR_50UM	P	PWR_50UM	PP_0V8_LDO3_SDR_VDDAL_DIG_TP	Y
	PWR_50UM	P	PWR_50UM	PP_0V8_LDO3_SDR_VDDAL_ICON	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_DIG_*	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_FBRX_20	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_GNSS_40	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_ICON*	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_RX*_22	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_RXLO*_27	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_TP*_30	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_TX*_20	Y
	PWR_50UM	P	PWR_50UM	PP_LDO3_SDR_VDDAL_XO_18	Y
LDO4	PWR_SHAPE	P	PWR_SHAPE	PP_0V875_LDO4	Y
	PWR_200UM	P	PWR_200UM	PP_LDO4_SMR_*, PP_LDO4_VDD_*	Y
LDO5	PWR_300UM	P	PWR_300UM	PP_1V8_LDO5	Y
	PWR_200UM	P	PWR_200UM	PP_LDO5_SMR_VDDAH_2_*	Y
	PWR_50UM	P	PWR_50UM	PP_LDO5_SMR_VDDAH_1_*, PP_LDO5_SMR_VDDAH_3_*, PP_LDO5_SMR_VDDAH_4_*	Y
LDO6	PWR_300UM	P	PWR_300UM	PP_1V8_LDO6	Y
	PWR_50UM	P	PWR_50UM	PP_LDO6_SMR_VDD_PX_20	Y
	PWR_50UM	P	PWR_50UM	PP_LDO6_SDR_VDD_PX_20	Y
	PWR_50UM	P	PWR_50UM	PP_LDO6_SDR_VDD_PXM_20	Y
LDO7	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO7	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_LDO7_SMR_CX_*_300	Y
LDO8	PWR_SHAPE	P	PWR_SHAPE	PP_0V8_LDO8	Y
LDO9	PWR_500UM	P	PWR_500UM	PP_0V8_LDO9	Y
	PWR_200UM	P	PWR_200UM	PP_LDO9_SMR_VDDAL_3_140	Y
	PWR_100UM	P	PWR_100UM	PP_LDO9_SMR_VDDAL_4_90	Y
	PWR_80UM	P	PWR_80UM	PP_LDO9_SMR_VDDAL_1_50	Y
	PWR_50UM	P	PWR_50UM	PP_LDO9_SMR_VDDAL_*_10	Y
LDO10	PWR_100UM	P	PWR_100UM	PP_3V1_LDO10	Y
LDO11	PWR_100UM	P	PWR_100UM	PP_UIM1_LDO11	Y
LDO12	PWR_SHAPE	P	PWR_SHAPE	PP_1V2_LDO12	Y
	PWR_300UM	P	PWR_300UM	PP_LDO12_SMR_VDDAM_4_240	Y
	PWR_200UM	P	PWR_200UM	PP_LDO12_SMR_VDDAM_2_120	Y
	PWR_100UM	P	PWR_100UM	PP_LDO12_SMR_VDDAM_*_70	Y
	PWR_100UM	P	PWR_100UM	PP_LDO12_SMR_VDDAM_5_240	Y
LDO13	PWR_100UM	P	PWR_100UM	PP_UIM2_LDO13	Y
LDO14	PWR_500UM	P	PWR_500UM	PP_0V6_LDO14	Y
	PWR_DEFAULT	P	PWR_DEFAULT	PP_0V6_LDO14_SNS	Y
LDO15	PWR_100UM	P	PWR_100UM	PP_1V2_LDO15	Y
	PWR_50UM	P	PWR_50UM	PP_LDO15_SDR_VDD_PX_20	Y
LDO16	PWR_750UM	P	PWR_750UM	PP_1V7_LDO16	Y
	PWR_200UM	P	PWR_200UM	PP_1V7_LDO16_SDR_VDDAH_RP	Y
	PWR_200UM	P	PWR_200UM	PP_1V7_LDO16_SDR_VDDAH_TX	Y
	PWR_100UM	P	PWR_100UM	PP_1V7_LDO16_SDR_VDDAH_TP	Y
	PWR_80UM	P	PWR_80UM	PP_1V7_LDO16_SDR_VDDAH_TXDAC	Y
	PWR_50UM	P	PWR_50UM	PP_LDO16_SDR_VDDAH_*	Y
BB_PMK	PWR_80UM	P	PWR_80UM	PP_BBPMK_VREG_RF	Y
	PWR_80UM	P	PWR_80UM	PP_BBPMK_VREG_XO	Y
	PWR_80UM	P	PWR_80UM	PP_PMK_REF_BYP	Y

RF Physical (continued)

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
QET0	PWR_500UM	P	PWR_500UM	PP_QET0_PA	Y
	PWR_500UM	P	PWR_500UM	PP_QET0_2G_PA	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_PA_VBAT_LDO	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_AMP_OUT	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_VAUX_S	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_VDD_AMP	Y
	PWR_100UM	P	PWR_100UM	PP_QET0_VDD_AMP_S	Y
APT (Lower)	PWR_500UM	P	PWR_500UM	PP_APT_L_PA	Y
	PWR_200UM	P	PWR_200UM	PP_APT_L_N*A*	Y
	PWR_200UM	P	PWR_200UM	PP_APT_L_LXA	Y
APT (Upper)	PWR_500UM	P	PWR_500UM	PP_APT_U_PA	Y
	PWR_200UM	P	PWR_200UM	PP_APT_U_N*A*	Y
	PWR_200UM	P	PWR_200UM	PP_APT_U_LXA	Y
PAD/DSM VDDs	PWR_50UM	P	PWR_50UM	VDD_HB_DSM	Y
	PWR_50UM	P	PWR_50UM	VDD_LB_DSM	Y
	PWR_50UM	P	PWR_50UM	VDD_LNA_HB_PAD	Y
	PWR_50UM	P	PWR_50UM	VDD_MIMO1_DSM	Y
	PWR_50UM	P	PWR_50UM	VDD_MIMO2_DSM	Y
	PWR_50UM	P	PWR_50UM	VDD_UHB_DSM	Y
Misc Radio	PWR_100UM	P	PWR_100UM	PP_PMX_VIO_OUT	Y
	PWR_300UM	P	PWR_300UM	PP_VDD_RF_1V2	Y
	PWR_50UM	P	PWR_50UM	PP_VDD_SIM_DETECT	Y
	PWR_80UM	P	PWR_80UM	PP_VIO_RFFE_1V8	Y
	PWR_100UM	P	PWR_100UM	PP_VREF_SDX	Y
	PWR_80UM	P	PWR_80UM	PP1V8_S4_UAT_BRIDGE_VIO	Y
	PWR_80UM	P	PWR_80UM	PP1V8_S2_LAT_BRIDGE_VIO	Y
WiFi	PWR_100UM	P	PWR_100UM	PP0V72_CBUCK*	Y
	PWR_100UM	P	PWR_100UM	PP1V02_ABUCK*	Y
	PWR_100UM	P	PWR_100UM	PP3V3_BTLDO	Y
Fez	PWR_SHAPE	P	PWR_SHAPE	PP_VBAT_FEZ	Y
	PWR_100UM	P	PWR_100UM	PP_1V85_FEZ	Y
NFC	PWR_80UM	P	PWR_80UM	PP1V2_NFC_S2	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*VDDBOOST	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VDDC	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*MIX	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VDDNV	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*TVDD	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VDDPLL	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*_MIX,PP_NFC_*_VCASCHI,PP_NFC_*_VCASLO	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VREF	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*AVDD	Y
	PWR_SHAPE	P	PWR_SHAPE	PP_NFC_*VUP	Y
	PWR_SHAPE	P	PWR_SHAPE	NFC_P_ANT_POS,NFC_P_ANT_NEG,NFC_*_ANT_MATCH_*	Y
	PWR_SHAPE	P	PWR_SHAPE	NFC_*_TXP,NFC_*_TXN,NFC_*_BAL*,NFC_*_PROBE_*	Y
	PWR_100UM	P	PWR_100UM	PP_NFC_*VHV	Y
	PWR_80UM	P	PWR_80UM	PP_SIMVCC1	Y

Spacing

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GND	GND	S	MSAP_YIELD	GND	Y
Power	PWR_DEFAULT	S	DEFAULT	=	Y
	PWR_50UM	S	DEFAULT	=	Y
	PWR_80UM	S	DEFAULT	=	Y
	PWR_100UM	S	DEFAULT	=	Y
	PWR_200UM	S	DEFAULT	=	Y
	PWR_300UM	S	DEFAULT	=	Y
	PWR_500UM	S	DEFAULT	=	Y
	PWR_750UM	S	DEFAULT	=	Y
	PWR_SHAPE	S	DEFAULT	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
PWR_100UM	GND	100UM-249UM_SPACING
PWR_100UM	PWR_100UM	100UM-249UM_SPACING
PWR_100UM	PWR_200UM	100UM-249UM_SPACING
PWR_100UM	PWR_300UM	100UM-249UM_SPACING
PWR_100UM	PWR_500UM	100UM-249UM_SPACING
PWR_100UM	PWR_750UM	100UM-249UM_SPACING
PWR_100UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_200UM	GND	100UM-249UM_SPACING
PWR_200UM	PWR_200UM	100UM-249UM_SPACING
PWR_200UM	PWR_300UM	100UM-249UM_SPACING
PWR_200UM	PWR_500UM	100UM-249UM_SPACING
PWR_200UM	PWR_750UM	100UM-249UM_SPACING
PWR_200UM	PWR_SHAPE	100UM-249UM_SPACING
PWR_300UM	GND	250UM+_SPACING
PWR_300UM	PWR_300UM	250UM+_SPACING
PWR_300UM	PWR_500UM	250UM+_SPACING
PWR_300UM	PWR_750UM	250UM+_SPACING
PWR_300UM	PWR_SHAPE	250UM+_SPACING
PWR_500UM	GND	250UM+_SPACING
PWR_500UM	PWR_500UM	250UM+_SPACING
PWR_500UM	PWR_750UM	250UM+_SPACING
PWR_500UM	PWR_SHAPE	250UM+_SPACING
PWR_750UM	GND	250UM+_SPACING
PWR_750UM	PWR_750UM	250UM+_SPACING
PWR_750UM	PWR_SHAPE	250UM+_SPACING
PWR_SHAPE	GND	250UM+_SPACING
PWR_SHAPE	PWR_SHAPE	250UM+_SPACING

SYNC_MASTER=D52_AP_MASTER_0.169.0 SYNC_DATE=07/02/2019

PAGE TITLE

CONSTRAINTS: Power

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Diff Pair Constraints

Electrical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
E_DP_GENERIC	E	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET0	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y
E_DP_GENERIC	E	GENERIC_DP	DP:DP_VREG_S1_S6_SENSE	Y
E_DP_NTC	E	GENERIC_DP	DP:DP_NTC_*	Y

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_ETDAC_QET0	P	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET0	Y
DP_ETDAC_QET1	P	GENERIC_DP	DP:DP_SHIELD_ETDAC_QET1	Y
DP_GENERIC	P	GENERIC_DP	DP:DP_VREG_S1_S6_SENSE	Y
DP_NTC	P	GENERIC_DP	DP:DP_NTC_*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DP_GENERIC	S	DEFAULT	=	Y
DP_NTC	S	A_DIELECTRIC_1.5X	=	Y
DP_ETDAC_QET0	S	A_DIELECTRIC_1.5X	=	Y
DP_ETDAC_QET1	S	A_DIELECTRIC_1.5X	=	Y

RF-Shield

Physical

	CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
	CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
SuBus	RF_SHIELD_SUBUS_WIDE	P	PWR_SUBUS	*SUBUS_UAT*	Y
	RF_SHIELD_SUBUS_DEFAULT	P	DEFAULT	*SUBUS_LAT*	Y
RFFE	RF_SHIELD_RFFE	P	DEFAULT	RFFE_WLAN_TO_LAT*	Y
	RF_SHIELD_RFFE	P	DEFAULT	RFFE_WLAN_TO_UAT*	Y
	RF_SHIELD_RFFE	P	DEFAULT	RFFE0_XCVR_TO_LAT_LAA_VIO_R	Y
	RF_SHIELD_RFFE	P	DEFAULT	SHIELD_RFFE*	Y
Clocks	RF_SHIELD_CLK	P	DEFAULT	SHIELD*38P4M*CLK*	Y
	RF_SHIELD_CLK	P	DEFAULT	SHIELD*19P2M*CLK*	Y
	RF_SHIELD_CLK	P	DEFAULT	SHIELD*SLEEP*CLK*	Y
	RF_SHIELD_CLK	P	DEFAULT	SHIELD_*_CLK_32K	Y
Analog	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_ZQ	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_CAL	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_REXT	Y
	RF_SHIELD_ANALOG	P	DEFAULT	SHIELD_*_CAL_RES	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RF_SHIELD_RFFE	S	DEFAULT	=	Y
RF_SHIELD_SUBUS_WIDE	S	DEFAULT	=	Y
RF_SHIELD_SUBUS_DEFAULT	S	DEFAULT	=	Y
RF_SHIELD_CLK	S	A_DIELECTRIC_3X	=	Y
RF_SHIELD_ANALOG	S	A_DIELECTRIC_3X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
RF_SHIELD_RFFE	PWR_DEFAULT	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_50UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_80UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_100UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_200UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_300UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_500UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_750UM	A_DIELECTRIC_3X
RF_SHIELD_RFFE	PWR_SHAPE	A_DIELECTRIC_3X
RF_SHIELD_RFFE	GND	DEFAULT
RF_SHIELD_CLK	GND	DEFAULT
RF_SHIELD_ANALOG	GND	DEFAULT
DP_ETDAC_QET0	GND	DEFAULT
DP_ETDAC_QET1	GND	DEFAULT
DP_NTC	GND	DEFAULT

Grouping Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	P	DEFAULT	GPIO*, IO_*	Y
GRP_I2C	P	DEFAULT	I2C*	Y
GRP_I2S	P	DEFAULT	I2S*LRCLK*, I2S*BCLK*, I2S*DOUT*, I2S*DIN*	Y
GRP_SPI	P	DEFAULT	SPI*MOSI*, SPI*MISO*, SPI*CS*	Y
GRP_UART	P	DEFAULT	UART*	Y
GRP_SWD	P	DEFAULT	SWD*	Y
GRP_SPMI_DATA	P	DEFAULT	SPMI*DATA*	Y
GRP_PCIE_SIDE	P	DEFAULT	PCIE*CLKREQ*, PCIE*PERST*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GRP_GPIO	S	DEFAULT	=	Y
GRP_I2C	S	DEFAULT	=	Y
GRP_I2S	S	DEFAULT	=	Y
GRP_SPI	S	DEFAULT	=	Y
GRP_UART	S	DEFAULT	=	Y
GRP_SWD	S	DEFAULT	=	Y
GRP_SPMI_DATA	S	DEFAULT	=	Y
GRP_PCIE_SIDE	S	DEFAULT	=	Y

BB XO

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
XTAL_OSC	S	A_DIELECTRIC_3X	XO_GND	Y
XTAL_OSC	S	A_DIELECTRIC_3X	XO_THERM	Y
XTAL_OSC	S	A_DIELECTRIC_3X	THERMAL_GNSS_XO_THERM	Y

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
XTAL_OSC	XTAL_OSC	DEFAULT

Clocks

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	P	DEFAULT	CLK_*	Y
CLK	P	DEFAULT	SPMI*CLK*	Y
CLK	P	DEFAULT	SPI*SCLK*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLK	S	A_DIELECTRIC_1.5X	=	Y

Sensitive Analog

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG	P	DEFAULT	ANALOG*PDTS*	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	...	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
ANALOG	S	A_DIELECTRIC_1.5X	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
ANALOG	GND	DEFAULT
CLK	GND	DEFAULT

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50 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.059
ISL3	ISL2,ISL4	50	0.029
ISL5	ISL4,ISL6	50	0.041
ISL7	ISL6,BOTTOM	50	0.029

50 Wide

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
TOP	ISL3	50	0.166
ISL6	ISL4,BOTTOM	50	0.089

50 Wide, Surface Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_SURFACE_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.059
ISL6	ISL4,BOTTOM	50	0.089

50 Wide, L3 and Surface Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_SURFACE_L3_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.059
ISL3	ISL2,ISL4	50	0.029
ISL6	ISL4,BOTTOM	50	0.089

50 Wide, L3 Thin

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RF SPACING VALUES= ?			
RULE NAME= 50_WIDE_L3_THIN		ZONE NAME= PRIMARY	
TOP	ISL3	50	0.166
ISL3	ISL2,ISL4	50	0.029
ISL6	ISL4,BOTTOM	50	0.089

50-ohm (Wide) Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***	CONSTRAINT SET		
Cellular	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT2*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT4*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT4_MB_HB_WLAN24	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_ANT4_MB_HB_WLAN24_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HB_PAD_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LBDSM_*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_RX1_DRX_OUT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_RX1	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_TX	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LMB_HB_PORTB_TX_UAT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_HBDSM_*	Y
GNSS	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_L*_LNA_IN*	Y
WiFi	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_WLAN_G_BT_ANT3*	Y
UHB PAD	50_TRX_UHB_PAD	P	A_50_WIDE_SE	50_TRX_UHB_PAD_*	Y
Direct Net	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_WLAN_G_BT_ANT4*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_TPLX_ANT_LB_LMB_MB_HB_L1	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_G_BT_LAT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_LB_OUT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_LMB_ANT	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_MB_OUT_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_IN_LMB_PAD_2G_MB_OUT	Y
	50_TRX_PAUHBU	P	A_50_WIDE_SE	50_TRX_PAUHBU_N79_ANT1_TO_ANT4*	Y
	50_TRX_PAUHBU	P	A_50_WIDE_SE	50_TRX_PAUHBU_UHB_ANT1_TO_ANT4*	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_RX1_ANT2	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_TX	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_WLAN_G_BT_ANT4_NPLXR_M	Y
	50_TRX_WIDE	P	A_50_WIDE_SE	50_TRX_LB_PORTB_TX_M	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***	CONSTRAINT SET		
Everything	50_TRX_WIDE	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	Y
	50_TRX_UHB_PAD	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	Y
	50_TRX_PAUHBU	S	NA_DIELECTRIC_4XV_50_WIDE_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING			
CLASS NAME	CLASS NAME	CONSTRAINT SET	
GND	50_TRX_WIDE	GND	NA_DIELECTRIC_2X_50_WIDE_SE
	50_TRX_UHB_PAD	GND	NA_DIELECTRIC_2X_50_WIDE_SE
UHB PAD to Self	50_TRX_UHB_PAD	50_TRX_UHB_PAD	DIELECTRIC_4XV_50_WIDE_SE_UHB_PAD
	50_TRX_PAUHBU	GND	NA_DIELECTRIC_2X_50_WIDE_SE
PAUHBU to Self	50_TRX_PAUHBU	50_TRX_PAUHBU	DIELECTRIC_4XV_50_WIDE_SE_UHB_PAD

50-ohm (Hybrid) Constraints

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***	CONSTRAINT SET		
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_A_C1_TXRX_FEM_M	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_A_C1_TXRX_BPF	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_WLAN_A_C1_TXRX_BPF_R	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_IN_LMB_PAD_LMB_ANT_M	Y
50_TRX_HYBRID	P	A_50_WIDE_SURFACE_THIN_SE	50_TRX_CPLR_U_CPL2_ANT_LMB_MB_HB_M	Y
50_TRX_WIDE_SURFACE_L3_THIN	P	A_50_WIDE_SURFACE_L3_THIN_SE	50_TRX_PAUHBU_N79_ANT2_TO_ANT8*	Y
50_TRX_WIDE_SURFACE_L3_THIN	P	A_50_WIDE_SURFACE_L3_THIN_SE	50_WLAN_A_C1_TXRX	Y
50_TRX_WIDE_L3_THIN	P	A_50_WIDE_L3_THIN_SE	50_TRX_CPLR_U_CPL1_ANT_LB_LMB_MB_HB_L1	Y
50_TRX_WIDE_L3_THIN	P	A_50_WIDE_L3_THIN_SE	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***	CONSTRAINT SET		
50_TRX_HYBRID	S	NA_DIELECTRIC_4XV_50_WIDE_SURFACE_THIN_SE	=	Y
50_TRX_WIDE_SURFACE_L3_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_SURFACE_L3_THIN_SE	=	Y
50_TRX_WIDE_L3_THIN	S	NA_DIELECTRIC_4XV_50_WIDE_L3_THIN_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_TRX_HYBRID	GND	NA_DIELECTRIC_2X_50_WIDE_SURFACE_THIN_SE
50_TRX_WIDE_SURFACE_L3_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_SURFACE_L3_THIN_SE
50_TRX_WIDE_L3_THIN	GND	NA_DIELECTRIC_2X_50_WIDE_L3_THIN_SE

50-ohm (Thin) Constraints

Physical

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***	CONSTRAINT SET		
Wildcards	50_TX0_THIN	P	A_50_THIN_SE	50_TX_IN_*TX0_*	Y
	50_TX1_THIN	P	A_50_THIN_SE	50_TX_IN_*TX1_*	Y
	50_TX2_THIN	P	A_50_THIN_SE	50_TX_IN_*TX2_*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_HBDSM_RXOUT_DRX*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_XCVR_DRX*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_XCVR_PRX*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_HB_PAD_PRX_OUT*	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_MIMO*_RXOUT_DRX*	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_A_C0*	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_G_C0*	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_G_C1*	Y
Direct Net	50_RX_THIN	P	A_50_THIN_SE	50_LAA_RX_XCVR_DRX10	Y
	50_RX_THIN	P	A_50_THIN_SE	50_LAA_RX_XCVR_PRX12	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LBDSM_RXOUT1	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LBDSM_RXOUT2	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM_RX_OUT1	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM_N79_RX_OUT1	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM_RX_OUT2	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_UHB_DSM_N79_RX_OUT2	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LMB_PAD_LMB_PRX_OUT	Y
	50_RX_THIN	P	A_50_THIN_SE	50_RX_LMB_PAD_LMB_PRX_OUT_M	Y
	50_THIN	P	A_50_THIN_SE	50_RX_GNSS_L1	Y
	50_THIN	P	A_50_THIN_SE	50_RX_GNSS_L5	Y
	50_THIN	P	A_50_THIN_SE	50_RX_L5_LNA_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_L5_LNA_NOTCH2	Y
	50_THIN	P	A_50_THIN_SE	50_RX_L1_LNA_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_L1_LNA_NOTCH2	Y
	50_THIN	P	A_50_THIN_SE	50_TX_IN_XCVR_FBRX_1	Y
	50_THIN	P	A_50_THIN_SE	50_CPLR_L_CPL1_LAT_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_UHB_L_CPLR_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_CPLR_U_CPL1_UHB_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_CPLR_U_CPL1_UAT_OUT	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_G_LAT_TXRX_FEM	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_G_UAT_TXRX_FEM	Y
	50_THIN	P	A_50_THIN_SE	50_TANGIER_TP11	Y
	50_THIN	P	A_50_THIN_SE	50_WLAN_A_C1_TXRX_MODULE	Y
	50_THIN	P	A_50_THIN_SE	50_TRX_CPLR_U_CPL1_IN_LB_LMB_MB_HB_L1	Y
	50_THIN	P	A_50_THIN_SE	50_TRX_LB_PORTB_RX1_M	Y
	50_THIN	P	A_50_THIN_SE	50_TRX_ANT4_MB_HB_WLAN24_L	Y
	50_THIN	P	A_50_THIN_SE	50_TRX_ANT4_MB_HB_WLAN24_NOTCH	Y

Spacing

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	***	CONSTRAINT SET		
Everything	50_TX0_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
	50_TX1_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
	50_TX2_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
	50_RX_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y
	50_THIN	S	NA_DIELECTRIC_4XV_50_THIN_SE	=	Y

Class-Class Spacing

CLASS TO CLASS SPACING			
CLASS NAME	CLASS NAME	CONSTRAINT SET	
Same Class	50_TX0_THIN	50_TX0_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	50_TX1_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	50_TX2_THIN	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	50_RX_THIN	NA_DIELECTRIC_2X_50_THIN_SE
GND	50_TX0_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX1_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_TX2_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_RX_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE
	50_THIN	GND	NA_DIELECTRIC_2X_50_THIN_SE

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FEZ FIDUCIALS

FD0920 — 0P5MM_SM — 998-4642 — ROOM=ASSEMBLY
FD0922 — 0P5MM_SM — 998-4642 — ROOM=ASSEMBLY
FD0921 — 0P5MM_SM — 998-4642 — ROOM=ASSEMBLY
FD0923 — 0P5MM_SM — 998-4642 — ROOM=ASSEMBLY

SHIELDS

CRITICAL
SH0900 — SM — 806-23604
SHLD-TTS-SHORT-D52

CRITICAL
SH0901 — SM — 806-23497
SHLD-TTS-INTERNAL-NW-D54

CRITICAL
SH0902 — SM — 806-25905
SHLD-SOUTH-NARROW-D54

STIFFENER

CRITICAL
ST0900
STIFFENER-D54
SM — 806-24036

FIDUCIALS

FD0900 FID 0P5SQ-CROSS-NSP — 998-04808 — ROOM=ASSEMBLY
FD0910 FID 0P5SQ-SMP3SQ-NSP — 998-00557 — ROOM=ASSEMBLY
FD0901 FID 0P5SQ-CROSS-NSP — 998-04808 — ROOM=ASSEMBLY
FD0911 FID 0P5SQ-SMP3SQ-NSP — 998-00557 — ROOM=ASSEMBLY
FD0902 FID 0P5SQ-CROSS-NSP — 998-04808 — ROOM=ASSEMBLY
FD0912 FID 0P5SQ-SMP3SQ-NSP — 998-00557 — ROOM=ASSEMBLY
FD0903 FID 0P5SQ-CROSS-NSP — 998-04808 — ROOM=ASSEMBLY
FD0913 FID 0P5SQ-SMP3SQ-NSP — 998-00557 — ROOM=ASSEMBLY
FD0904 FID 0P5SQ-CROSS-NSP — 998-04808 — ROOM=ASSEMBLY
FD0914 FID 0P5SQ-SMP3SQ-NSP — 998-00557 — ROOM=ASSEMBLY
FD0905 FID 0P5SQ-CROSS-NSP — 998-04808 — ROOM=ASSEMBLY
FD0915 FID 0P5SQ-SMP3SQ-NSP — 998-00557 — ROOM=ASSEMBLY

UF: Always stuff

CKPLUS_WAIVE=TERMSHORTED
R0910 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0960 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0972 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0911 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0961 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0973 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0900 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0962 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0974 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0956 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0963 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0975 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0903 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0976 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0907 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0948 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0909 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0908 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0964 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0924 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0977 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0965 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0942 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0978 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0959 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0943 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0979 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0957 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0958 0.00 — 0R 1/32W MF 01005 — ROOM=DFM

UF: NOSTUFF with Kolkata

BOMOPTION=NO-KOLKATA
CKPLUS_WAIVE=TERMSHORTED
R0944 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0906 0.00 — 0R 1/32W MF 01005 — ROOM=DFM

UF: Stuff with Kolkata

BOMOPTION=RF_SKU:NAMM
CKPLUS_WAIVE=TERMSHORTED
R0912 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0920 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0929 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0937 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0953 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0913 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0921 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0930 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0938 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0901 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0914 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0922 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0931 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0939 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0904 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0915 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0923 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0932 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0940 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0905 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0916 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0925 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0933 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0941 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0966 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0917 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0926 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0934 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0945 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0967 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0918 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0927 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0935 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0950 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0968 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0919 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0928 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0936 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0952 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0969 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0949 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0902 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0971 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0970 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0951 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0946 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0954 0.00 — 0R 1/32W MF 01005 — ROOM=DFM
R0955 0.00 — 0R 1/32W MF 01005 — ROOM=DFM

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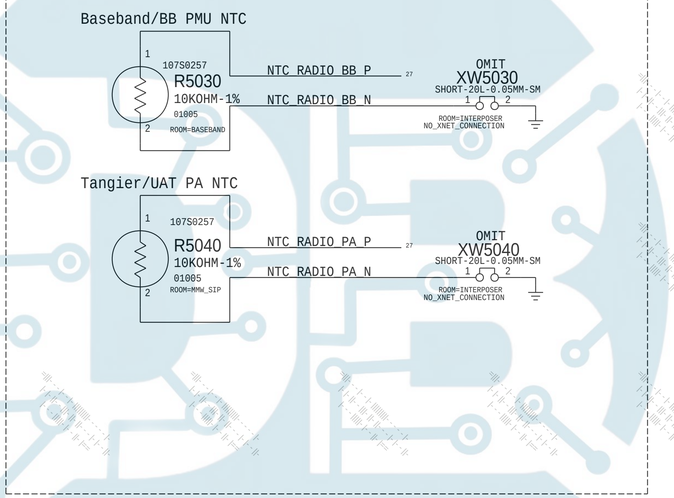
Bot NTCs

Place NTC XWs near PMU, route P/N differentially



PAGE TITLE: SYS PWR: NTCs (Bottom)

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LVCC

14 ANALOG_PP_GPU_LVCC — TP12660 1 A TP-P55 ROOM=TEST

14 ANALOG_PP_CPU_PCORE_LVCC — TP12661 1 A TP-P55 ROOM=TEST

REL Bias

14 IO_PMU_TO_SYSTEM_RESET_L — TP12681 1 A TP-P55 ROOM=TEST

DFU

14 IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU — TP12680 1 A TP-P55 ROOM=TEST

Power/GND

18 17 16 15 IN PP_VDD_MAIN

TP012600 1 A TP-P55 ROOM=TEST

TP012601 1 A TP-P55 ROOM=TEST

TP12602 1 A TP-P55 ROOM=TEST

TP12603 1 A TP-P55 ROOM=TEST

TP012610 1 A TP-P55 ROOM=TEST

TP012611 1 A TP-P55 ROOM=TEST

TP12612 1 A TP-P55 ROOM=TEST

TP12613 1 A TP-P55 ROOM=TEST

TP12614 1 A TP-P55 ROOM=TEST

TP12615 1 A TP-P55 ROOM=TEST

VBUS

15 PP_VBUS1_E75

TP12621 1 A TP-P55 ROOM=TEST

TP12622 1 A TP-P55 ROOM=TEST

AMUX

15 AMUX_PMU_AY — TP12685 1 A TP-P55 ROOM=TEST

15 AMUX_PMU_BY — TP12686 1 A TP-P55 ROOM=TEST

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TESTING: Test Points

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PAGE TITLE
TESTING: Probe Points

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13	GND	1	IO1	IO91	91	IO_BT_TO_R1_WAKE	13
13	GND	2	IO2	IO92	92	GPIO_R1_TO_BB_LAA_SW_CTRL	13
13	GND	3	IO3	IO93	93	GND	13
13	GPIO_CANARY_2C_TO_2D	4	IO4	IO94	94	GPIO_AP_FROM_WLAN_TIME_SYNC	13
13	NFC_P_ANT_NEG	5	IO5	IO95	95	GPIO_BB_TO_R1_COEX	13
13	GND	6	IO6	IO96	96	GND	13
13	NFC_P_ANT_NEG	7	IO7	IO97	97	GND	13
13	GND	8	IO8	IO98	98	IO_BT_TO_R1_TIME_SYNC	13
13	NFC_P_ANT_NEG	9	IO9	IO99	99	GPIO_R1_TO_WLAN_COEX	13
13	GND	10	IO10	IO100	100	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	13
13	NFC_P_ANT_NEG	11	IO11	IO101	101	GND	13
13	GPIO_NFC_F_NFC_P_SYNC2	12	IO12	IO102	102	SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA	13
13	GND	13	IO13	IO103	103	GPIO_WLAN_TO_R1_COEX	13
13	GND	14	IO14	IO104	104	GND	13
13	50_TRX_ANT4_MB_HB_WLAN24	15	IO15	IO105	105	GND	13
13	GND	16	IO16	IO106	106	NFC_P_ANT_POS	13
13	GND	17	IO17	IO107	107	GND	13
13	PCIE_GP1_AP_TO_WLAN_PERST_L	18	IO18	IO108	108	NFC_P_ANT_POS	13
13	GPIO_AP_TO_BB_PEAK_PWR_IND	19	IO19	IO109	109	GND	13
13	PCIE_GP1_AP_BI_WLAN_CLKREQ_L	20	IO20	IO110	110	NFC_P_ANT_POS	13
13	SWD_AP_BI_BB_SWDIO	21	IO21	IO111	111	GND	13
13	NTC_STOCKHOLM	22	IO22	IO112	112	NFC_P_ANT_POS	13
13	GPIO_R1_TO_BB_CH9_COEX	23	IO23	IO113	113	GND	13
13	GPIO_NFC_F_NFC_P_SYNC1	24	IO24	IO114	114	CLK_BBPMU_TO_DOTARA_38M4	13
13	GND	25	IO25	IO115	115	GND	13
13	GND	26	IO26	IO116	116	GND	13
13	PP1V2_S4	27	IO27	IO117	117	GND	13
13	GND	28	IO28	IO118	118	GND	13
13	I2C_R1_TO_NFC_SCL	29	IO29	IO119	119	50_WLAN_A_C0_TXRX_FEM_M	13
13	GND	30	IO30	IO120	120	GND	13
13	I2C_R1_TO_NFC_SDA	31	IO31	IO121	121	GND	13
13	GND	32	IO32	IO122	122	50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M	13
13	NFC_P_TEST_OUT	33	IO33	IO123	123	GND	13
13	GND	34	IO34	IO124	124	GND	13
13	GND	35	IO35	IO125	125	50_TRX_ANT2_LB_LMB_MB_HB_L1	13
13	GND	36	IO36	IO126	126	GND	13
13	GND	37	IO37	IO127	127	GND	13
13	GND	38	IO38	IO128	128	50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M	13
13	GND	39	IO39	IO129	129	GND	13
13	GND	40	IO40	IO130	130	GND	13
13	GND	41	IO41	IO131	131	50_LAA_RX_XCVR_DRX10	13
13	GND	42	IO42	IO132	132	GND	13
13	GND	43	IO43	IO133	133	GND	13
13	GND	44	IO44	IO134	134	GND	13
13	GND	45	IO45	IO135	135	IO_TOUCH_TO_MANY_SCAN_ACTIVE_U	13
13	GND	46	IO46	IO136	136	GPIO_CANARY_1C_TO_1D	13
13	GND	47	IO47	IO137	137	GND	13
13	GND	48	IO48	IO138	138	GND	13
13	GND	49	IO49	IO139	139	GPIO_CANARY_1C_TO_1D	13
13	GND	50	IO50	IO140	140	GND	13
13	GND	51	IO51	IO141	141	GND	13
13	GND	52	IO52	IO142	142	GND	13
13	GND	53	IO53	IO143	143	GND	13
13	GND	54	IO54	IO144	144	GND	13
13	GND	55	IO55	IO145	145	GND	13
13	GND	56	IO56	IO146	146	GND	13
13	GND	57	IO57				
13	GND	58	IO58				
13	GND	59	IO59	IO149	149	GND	13
13	GND	60	IO60	IO150	150	GND	13
13	GND	61	IO61	IO151	151	GND	13
13	GND	62	IO62	IO152	152	GND	13
13	GND	63	IO63	IO153	153	GND	13
13	GND	64	IO64	IO154	154	GND	13
13	GND	65	IO65	IO155	155	GND	13
13	GND	66	IO66	IO156	156	GND	13
13	GND	67	IO67	IO157	157	GND	13
13	GND	68	IO68	IO158	158	GND	13
13	GND	69	IO69	IO159	159	GND	13
13	GND	70	IO70	IO160	160	GND	13
13	GND	71	IO71	IO161	161	GND	13
13	GND	72	IO72	IO162	162	GND	13
13	GND	73	IO73	IO163	163	GND	13
13	GND	74	IO74	IO164	164	GND	13
13	GND	75	IO75	IO165	165	GND	13
13	GND	76	IO76	IO166	166	GND	13
13	GND	77	IO77	IO167	167	GND	13
13	GND	78	IO78	IO168	168	GND	13
13	GND	79	IO79	IO169	169	GND	13
13	GND	80	IO80	IO170	170	GND	13
13	GND	81	IO81	IO171	171	GND	13
13	GND	82	IO82	IO172	172	GPIO_CANARY_1A_TO_1B	13
13	GND	83	IO83	IO173	173	GND	13
13	GND	84	IO84	IO174	174	GND	13
13	GND	85	IO85	IO175	175	GND	13
13	GPIO_BB_TO_R1_CH9_REQ	86	IO86	IO176	176	SHIELD_RFFE5_SCLK_SDR	13
13	GND	87	IO87	IO177	177	GND	13
13	SWD_AP_TO_MANY_SWCLK	88	IO88	IO178	178	SHIELD_RFFE5_SDATA_SDR	13
13	GND	89	IO89	IO179	179	GND	13
13	UAT_TUNER_TO_R1_STATE	90	IO90	IO180	180	SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA	13

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14	GPIO_CANARY_1A_TO_1B	181	IO181	IO271	271	GPIO_S4_PMU_TO_WLAN_REG_ON	14
14	SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK	182	IO182	IO272	272	GND	14
14	GND	183	IO183	IO273	273	GND	14
14	CLK_BBPMU_TO_NFC_38M	184	IO184	IO274	274	GPIO_PMU_FROM_WLAN_HOST_WAKE	14
14	ANALOG_UAT_5G_FEM_TO_WLAN_PDTS	185	IO185	IO275	275	GND	14
14	GND	186	IO186	IO276	276	PP1V8_S4	14
14	GND	187	IO187	IO277	277	PP_1V8_LDO6	14
14	I2S2_AP_TO_BB_DOUT	188	IO188	IO278	278	GND	14
14	RFFE_WLAN_TO_UAT_5G_FEM_RST_L	189	IO189	IO279	279	PP_APT_L_PA	14
14	I2S2_AP_FROM_BB_DIN	190	IO190	IO280	280	GND	14
14	GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN	191	IO191	IO281	281	PP_APT_L_PA	14
14	I2S2_AP_FROM_BB_BCLK	192	IO192	IO282	282	IO_TOUCH_TO_MANY_SCAN_ACTIVE	14
14	GND	193	IO193	IO283	283	GND	14
14	I2S2_AP_FROM_BB_LRCLK	194	IO194	IO284	284	GND	14
14	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	195	IO195	IO285	285	SHIELD_ETDAC_QET1_N	14
14	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	196	IO196	IO286	286	GND	14
14	GPIO_NFC_TO_BBPMU_CLK_EN	197	IO197	IO287	287	SHIELD_ETDAC_QET1_P	14
14	GND	198	IO198	IO288	288	GND	14
14	GND	199	IO199	IO289	289	SUBUS_LAT_A	14
14	90_PCIE_GP1_AP_TO_WLAN_REFCLK_P	200	IO200	IO290	290	GND	14
14	GND	201	IO201	IO291	291	SHIELD_RFFE8_SCLK_SDR	14
14	90_PCIE_GP1_AP_TO_WLAN_REFCLK_N	202	IO202	IO292	292	GND	14
14	GND	203	IO203	IO293	293	SHIELD_RFFE8_SDATA_SDR	14
14	GND	204	IO204	IO294	294	GND	14
14	GND	205	IO205	IO295	295	GND	14
14	90_PCIE_GP2_AP_TO_BB_REFCLK_N	206	IO206	IO296	296	GND	14
14	GND	207	IO207	IO297	297	GND	14
14	90_PCIE_GP2_AP_TO_BB_REFCLK_P	208	IO208	IO298	298	GND	14
14	GND	209	IO209	IO299	299	GND	14
14	GND	210	IO210	IO300	300	GND	14
14	GND	211	IO211	IO301	301	GND	14
14	GND	212	IO212	IO302	302	GND	14
14	GND	213	IO213	IO303	303	GND	14
14	GND	214	IO214	IO304	304	GND	14
14	GND	215	IO215	IO305	305	GND	14
14	GND	216	IO216	IO306	306	50_RX_XCVR_PRX14_N79_RX_OUT1	14
14	GND	217	IO217	IO307	307	GND	14
14	GND	218	IO218	IO308	308	GND	14
14	GND	219	IO219	IO309	309	50_RX_XCVR_PRX16_UHB_RX_OUT1	14
14	GND	220	IO220	IO310	310	GND	14
14	GND	221	IO221	IO311	311	GND	14
14	GND	222	IO222	IO312	312	50_TRX_UHB_PAD_PORTB_TX_M	14
14	90_PCIE_GP1_AP_FROM_WLAN_RX_N	223	IO223	IO313	313	GND	14
14	GND	224	IO224	IO314	314	GND	14
14	90_PCIE_GP1_AP_FROM_WLAN_RX_P	225	IO225	IO315	315	50_TRX_UHB_PAD_N79_PORTB_TX_M	14
14	GND	226	IO226	IO316	316	GND	14
14	GND	227	IO227	IO317	317	GND	14
14	GND	228	IO228	IO318	318	50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1	14
14	90_PCIE_GP1_AP_TO_WLAN_TX_P	229	IO229	IO319	319	GND	14
14	GND	230	IO230	IO320	320	GND	14
14	90_PCIE_GP1_AP_TO_WLAN_TX_N	231	IO231	IO321	321	50_RX_XCVR_PRX15_N79_RX_OUT2	14
14	GND	232	IO232	IO322	322	GND	14
14	GND	233	IO233	IO323	323	GND	14
14	GND	234	IO234	IO324	324	50_TX_IN_XCVR_TX1_LB_JB	14
14	90_PCIE_GP2_AP_FROM_BB_RX_N	235	IO235	IO325	325	50_TX_IN_XCVR_TX0_LB	14
14	GND	236	IO236	IO326	326	GND	14
14	90_PCIE_GP2_AP_FROM_BB_RX_P	237	IO237	IO327	327	GND	14
14	GND	238	IO238	IO328	328	50_RX_XCVR_PRX6_LB_A_RX0	14
14	GND	239	IO239	IO329	329	50_RX_XCVR_PRX10_LB_PRX_OUT2	14
14	GND	240	IO240	IO330	330	GND	14
14	90_PCIE_GP2_AP_TO_BB_TX_P	241	IO241	IO331	331	GND	14
14	GND	242	IO242	IO332	332	50_TX_IN_TX2_UHB_PAD_TX_N79_IN	14
14	90_PCIE_GP2_AP_TO_BB_TX_N	243	IO243	IO333	333	GND	14
14	GND	244	IO244	IO334	334	GND	14
14	GND	245	IO245	IO335	335	50_RX_XCVR_PRX17_UHB_RX_OUT2	14
14	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	246	IO246	IO336	336	GND	14
14	GND	247	IO247	IO337	337	GND	14
14	GND	248	IO248	IO338	338	50_UHB_L_CPLR_OUT	14
14	GPIO_AOP_TO_WLAN_CONTEXT_A	249	IO249	IO339	339	GND	14
14	GPIO_AOP_TO_BB_FORCE_PWM	250	IO250	IO340	340	GND	14
14	GPIO_AOP_TO_WLAN_CONTEXT_B	251	IO251	IO341	341	GND	14
14	GND	252	IO252	IO342	342	GND	14
14	ANALOG_PP_GPU_LVCC	253	IO253	IO343	343	GND	14
14	IO_PMU_TO_SYSTEM_RESET_L	254	IO254	IO344	344	GND	14
14	GND	255	IO255	IO345	345	GND	14
14	GND	256	IO256	IO346	346	GND	14
14	SUBUS_UAT_B	257	IO257	IO347	347	GND	14
14	ANALOG_PP_CPU_PCORE_LVCC	258	IO258	IO348	348	GND	14
14	SUBUS_UAT_A	259	IO259	IO349	349	GND	14
14	IO_SOC_FROM_PMU_KRAKEN_FORCE_DFU	260	IO260	IO350	350	GND	14
14	ANALOG_LAT_5G_FEM_TO_WLAN_PDTS	261	IO261	IO351	351	GND	14
14	GND	262	IO262	IO352	352	GND	14
14	GND	263	IO263	IO353	353	GND	14
14	GND	264	IO264	IO354	354	GND	14
14	GND	265	IO265	IO355	355	GND	14
14	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	266	IO266	IO356	356	GND	14
14	GND	267	IO267	IO357	357	GND	14
14	GND	268	IO268	IO358	358	GND	14
14	GND	269	IO269	IO359	359	GND	14
14	PP1V2_S2	270	IO270	IO360	360	GND	14

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15	GND	361	IO361	451	SHIELD_RFFE3_SCLK_SDR	15
15	GND	362	IO362	452	GND	15
15	GND	363	IO363	453	SHIELD_RFFE3_SDATA_SDR	15
15	GND	364	IO364	454	GND	15
15	GND	365	IO365	455	SHIELD_RFFE2_SCLK_SDR	15
15	GND	366	IO366	456	GND	15
15	GND	367	IO367	457	SHIELD_RFFE2_SDATA_SDR	15
15	GND	368	IO368	458	GND	15
15	GND	369	IO369	459	GND	15
15	GND	370	IO370	460	GND	15
15	GND	371	IO371	461	GND	15
15	GND	372	IO372	462	PP_VBUS1_E75	15
15	GND	373	IO373	463	PP_VBUS1_E75	15
15	GND	374	IO374	464	GND	15
15	GND	375	IO375	465	PP_UIM1_LDO11	15
15	GND	376	IO376	466	IO_BB_FROM_SIM2_DETECT	15
15	GND	377	IO377	467	PP_UIM2_LDO13	15
15	GND	378	IO378	468	GND	15
15	GND	379	IO379	469	IO_BB_TO_SIM2_CLK	15
15	GND	380	IO380	470	IO_BB_TO_SIM2_RESET	15
15	GND	381	IO381	471	IO_BB_BI_SIM2_DATA	15
15	50_TRX_LB_PORTB_RX1_M	382	IO382	472	GND	15
15	GND	383	IO383	473	GND	15
15	GND	384	IO384	474	GND	15
15	50_TRX_LB_PORTB_TX_M	385	IO385	475	GND	15
15	GND	386	IO386	476	GND	15
15	GND	387	IO387	477	IO_BB_FROM_SIM1_DETECT	15
15	PP_VDD_RF_1V2	388	IO388	478	IO_BB_TO_SIM1_RESET	15
15	SUBUS_LAT_C	389	IO389	479	IO_BB_BI_SIM1_DATA	15
15	GND	390	IO390	480	GND	15
15	SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK	391	IO391	481	IO_BB_TO_SIM1_CLK	15
15	SUBUS_LAT_B	392	IO392	482	GPIO_SEQ_PMU_TO_NFC_EN	15
15	SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA	393	IO393	483	GND	15
15	GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN	394	IO394	484	GND	15
15	GND	395	IO395	485	AMUX_PMU_BY	15
15	GND	396	IO396	486	AMUX_PMU_AY	15
15	50_TRX_L5_LNA_IN	397	IO397	487	NTC_RADIO_BB_P	15
15	GND	398	IO398	488	GND	15
15	GND	399	IO399	489	NTC_RADIO_PA_P	15
15	GND	400	IO400	490	PP1V2_NFC_S2	15
15	50_TRX_WLAN_G_BT_ANT3_NPLXR	401	IO401	491	GND	15
15	GND	402	IO402	492	GND	15
15	GND	403	IO403	493	GND	15
15	50_TRX_IN_LMB_PAD_2G_LB_OUT_M	404	IO404	494	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	15
15	GND	405	IO405	495	GND	15
15	GND	406	IO406	496	GND	15
15	50_WLAN_A_C1_TXRX_FEM_M	407	IO407	497	GND	15
15	GND	408	IO408			
15	GND	409	IO409	499	GND	15
15	50_LAA_RX_XCVR_PRX12	410	IO410	500	GND	15
15	GND	411	IO411	501	GND	15
15	GND	412	IO412	502	GND	15
15	50_TRX_HB_PAD_ANT1	413	IO413	503	GND	15
15	RFFE_WLAN_TO_LAT_5G_FEM_RST_L	414	IO414	504	GND	15
15	GND	415	IO415	505	GND	15
15	GND	416	IO416	506	PP3V0_S2	15
15	SHIELD_RFFE1_SCLK_SDR	417	IO417	507	UART1_AOP_FROM_BB_RXD	15
15	GND	418	IO418	508	GND	15
15	SHIELD_RFFE1_SDATA_SDR	419	IO419	509	GND	15
15	GND	420	IO420	510	GPIO_NFC_TO_ARCAMP_RESET_L	15
15	GND	421	IO421	511	UART1_AOP_TO_BB_TXD	15
15	GND	422	IO422	512	GND	15
15	GND	423	IO423	513	GPIO_AP_TO_BB_TIME_MARK	15
15	GND	424	IO424	514	GPIO_NFC_TO_ARCAMP_TRIG	15
15	GND	425	IO425	515	GPIO_AP_FROM_BT_AUDIO_SYNC	15
15	GND	426	IO426	516	GND	15
15	GND	427	IO427	517	PP1V8_S2	15
15	GND	428	IO428	518	GPIO_AP_TO_BB_COREDUMP	15
15	PP_VDD_BOOST	429	IO429	519	GPIO_BT_TO_BOT_SPKR_TRIG	15
15	GND	430	IO430	520	GND	15
15	GND	431	IO431	521	GND	15
15	GND	432	IO432	522	GND	15
15	50_TRX_HB_PAD_ANT2_M	433	IO433	523	PP_VDD_MAIN	15
15	GND	434	IO434	524	GND	15
15	GND	435	IO435	525	PP_VDD_MAIN	15
15	GND	436	IO436	526	GND	15
15	GND	437	IO437	527	PP_VDD_MAIN	15
15	GND	438	IO438	528	GND	15
15	50_CPLR_L_CPL1_LAT_OUT	439	IO439	529	PP_VDD_MAIN	15
15	GND	440	IO440	530	GND	15
15	GND	441	IO441	531	PP_VDD_MAIN	15
15	GND	442	IO442	532	GND	15
15	GND	443	IO443	533	GND	15
15	GND	444	IO444	534	GND	15
15	GND	445	IO445	535	PP_VDD_MAIN	15
15	GND	446	IO446	536	GND	15
15	GND	447	IO447	537	PP_VDD_MAIN	15
15	GND	448	IO448	538	GND	15
15	GND	449	IO449	539	PP_VDD_MAIN	15
15	GND	450	IO450	540	GND	15

OMIT

J INT TOP
INTERPOSER-RF-TOP
SM
SYM 4 OF 4

998-22293

16	PP_VDD_MAIN	541	IO541	
16	GND	542	IO542	
16	PP_VDD_MAIN	543	IO543	
16	GPIO_CANARY_2A_TO_2B	544	IO544	
16	GND	545	IO545	
16	GND	546	IO546	
16	PP_VDD_MAIN	547	IO547	
16	GND	548	IO548	
16	GND	549	IO549	
16	GND	550	IO550	
16	GND	551	IO551	
16	GND	552	IO552	
16	GND	553	IO553	
16	GND	554	IO554	
16	GND	555	IO555	
16	GND	556	IO556	
16	GND	557	IO557	
16	GND	558	IO558	
16	GND	559	IO559	
16	GND	560	IO560	
16	GND	561	IO561	
16	GPIO_CANARY_2A_TO_2B	562	IO562	
16	GND	563	IO563	
16	GND	564	IO564	
16	GND	565	IO565	
16	GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG	566	IO566	
16	GND	567	IO567	
16	GPIO_AP_FROM_BB_RESET_DETECT_L	568	IO568	
16	GND	569	IO569	
16	PCIE_GP2_AP_TO_BB_PERST_L	570	IO570	
16	GND	571	IO571	
16	GND	572	IO572	
16	GND	573	IO573	
16	PCIE_GP2_AP_BT_BB_CLKREQ_L	574	IO574	
16	GND	575	IO575	
16	GND	576	IO576	
16	GND	577	IO577	
16	GPIO_CANARY_2C_TO_2D	578	IO578	
16	GND	579	IO579	
16	GND	580	IO580	
16	GND	581	IO581	
16	GND	582	IO582	
16	GND	583	IO583	
16	GND	584	IO584	
16	GND	585	IO585	
16	GND	586	IO586	
16	GND	587	IO587	
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16	GND	589	IO589	
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16	GND	608	IO608	
16	GND	609	IO609	
16	GND	610	IO610	
16	GND	611	IO611	
16	GND	612	IO612	
16	GND	613	IO613	
16	GND	614	IO614	
16	GND	615	IO615	
16	GND	616	IO616	

OMIT

SYNC_DATE=08/15/2019

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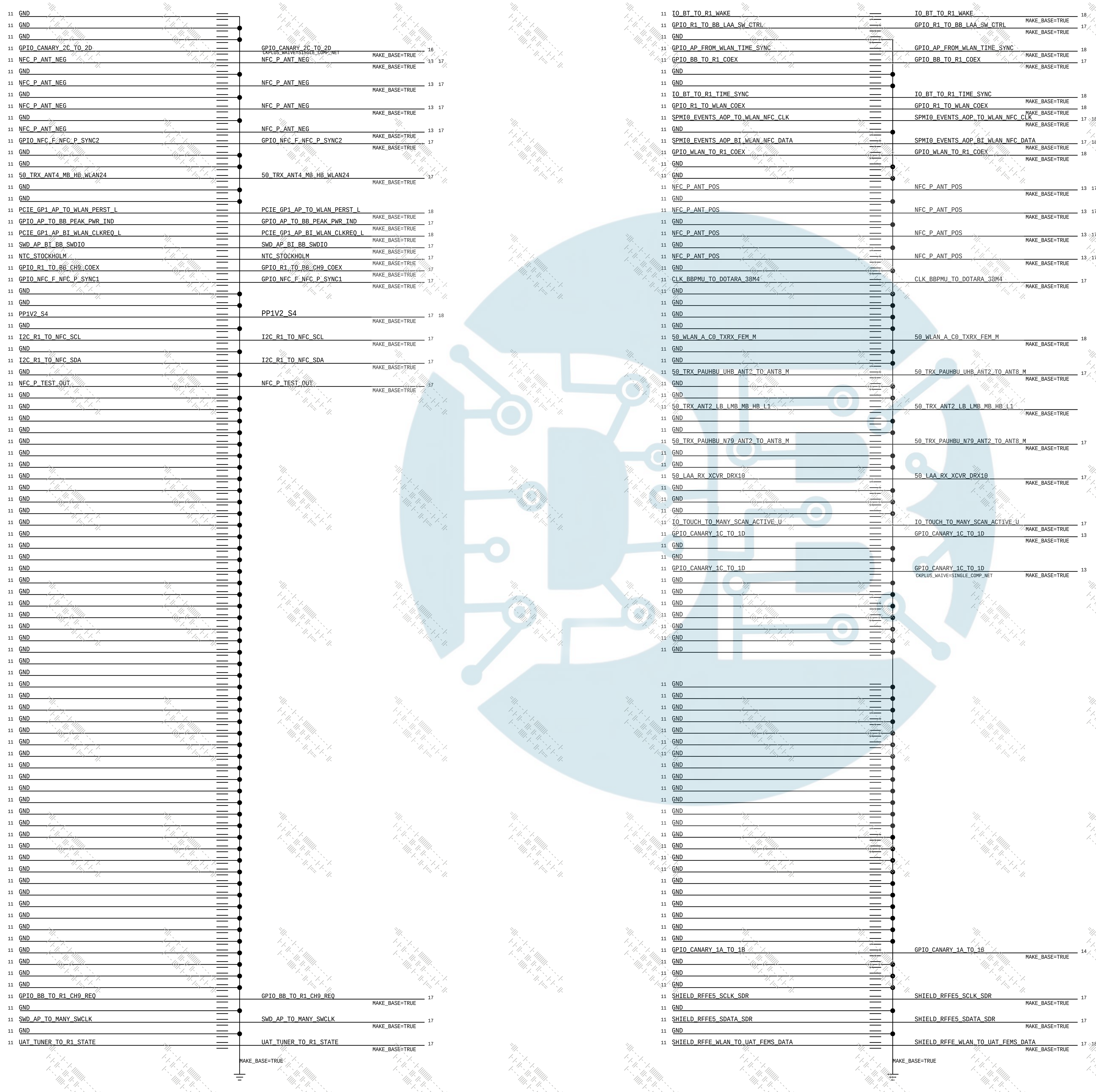
Interposer: Symbol 1 Aliases

LEFT SIDE

RIGHT SIDE



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INTERPOSER: Aliases (1/4)

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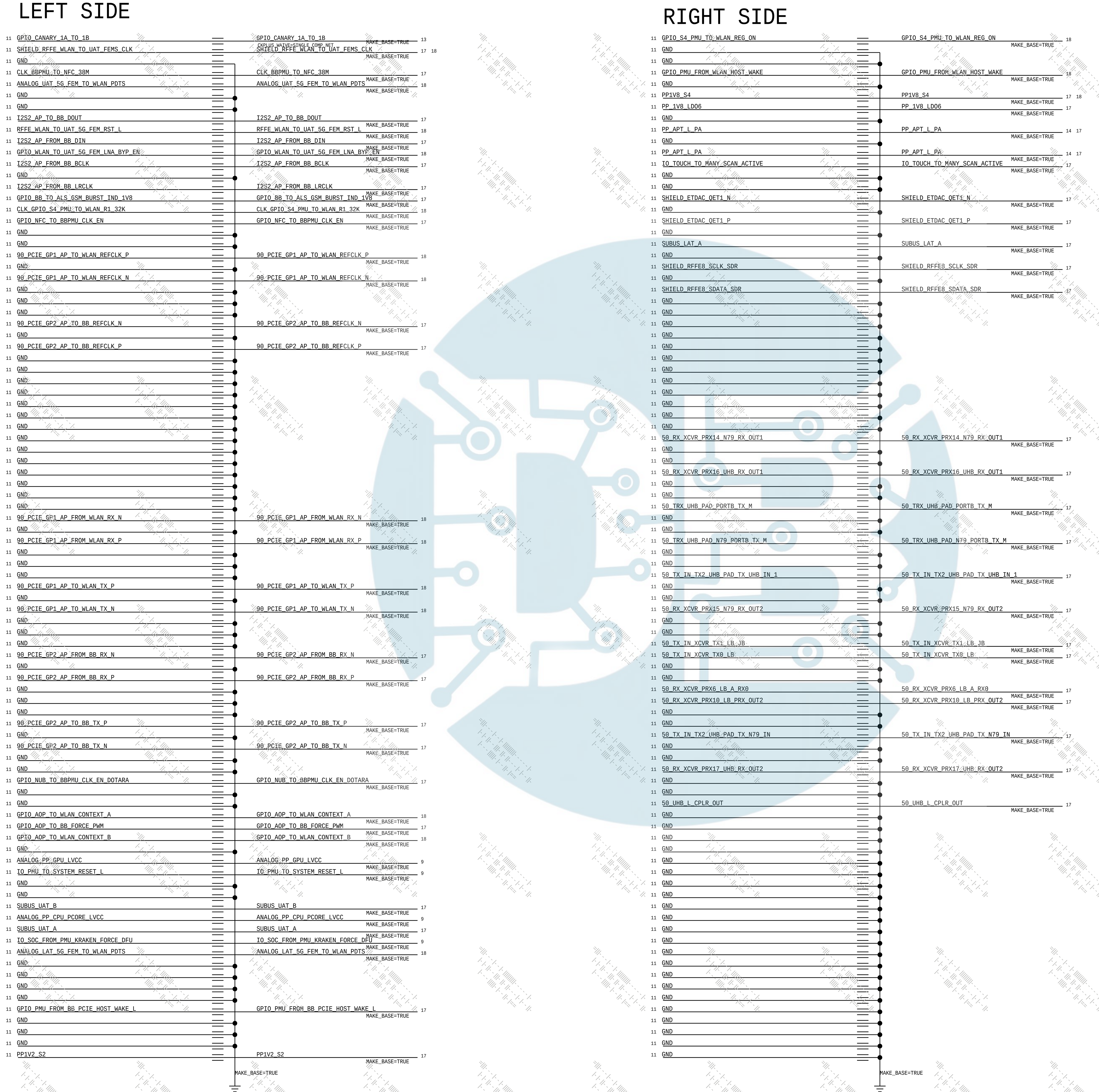
Interposer: Symbol 2 Aliases



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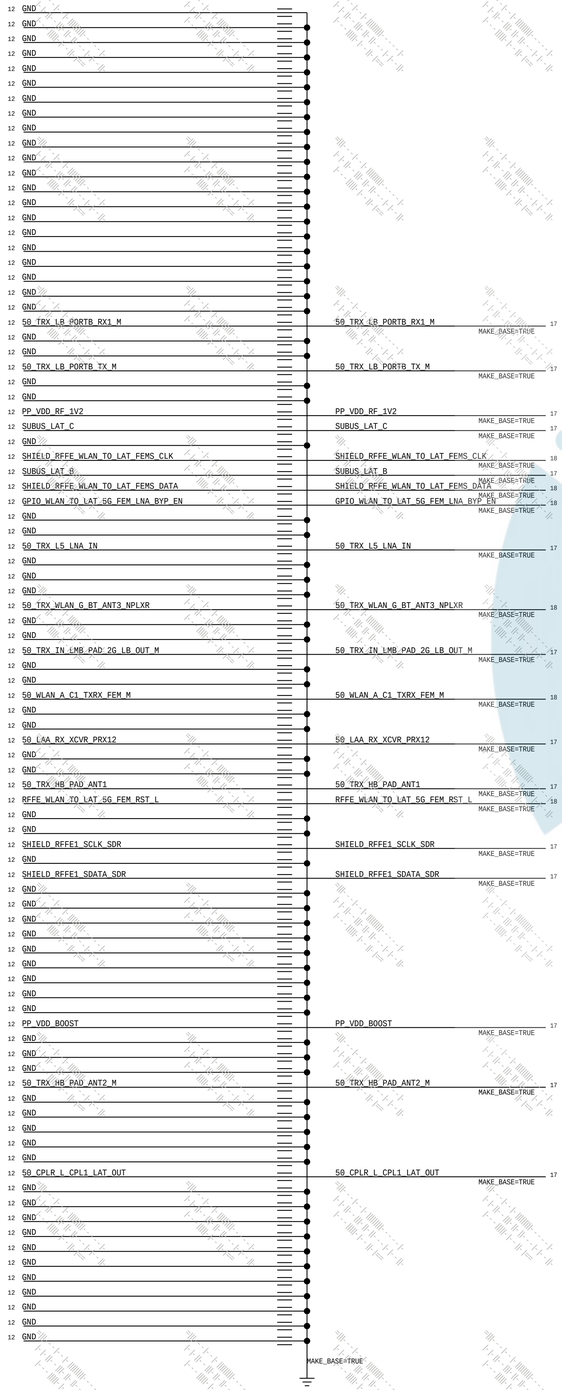
Interposer: Symbol 3 Aliases

LEFT SIDE



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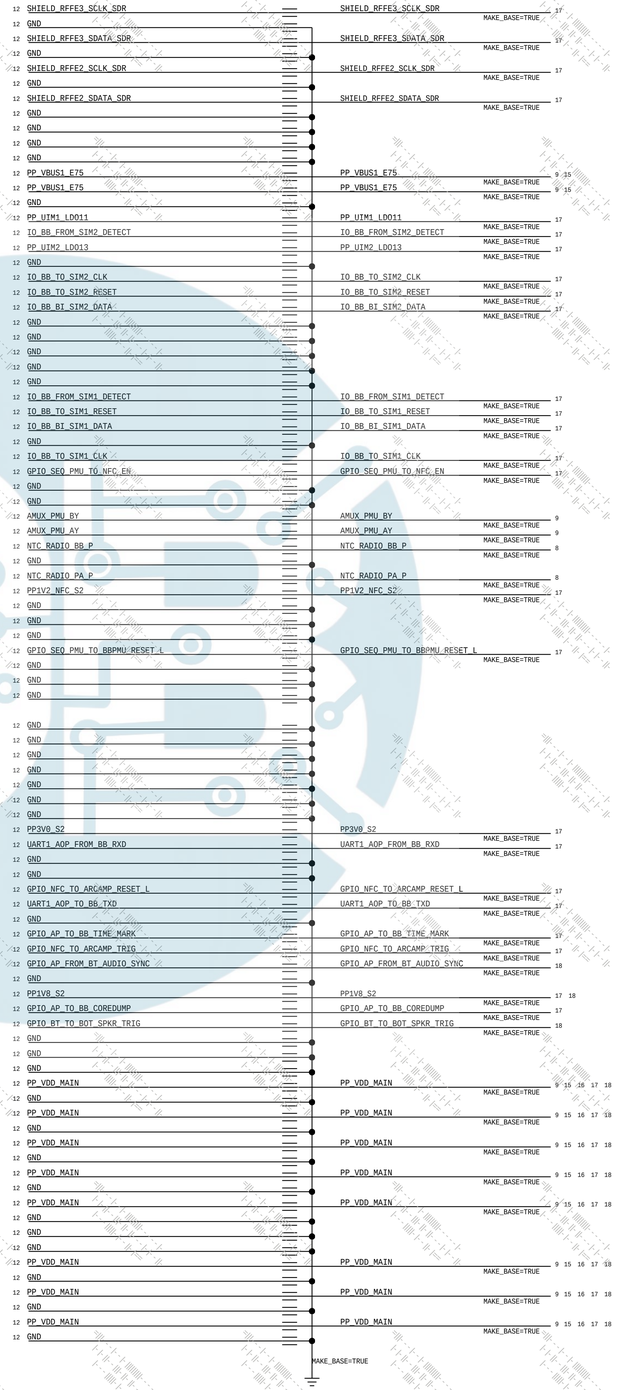

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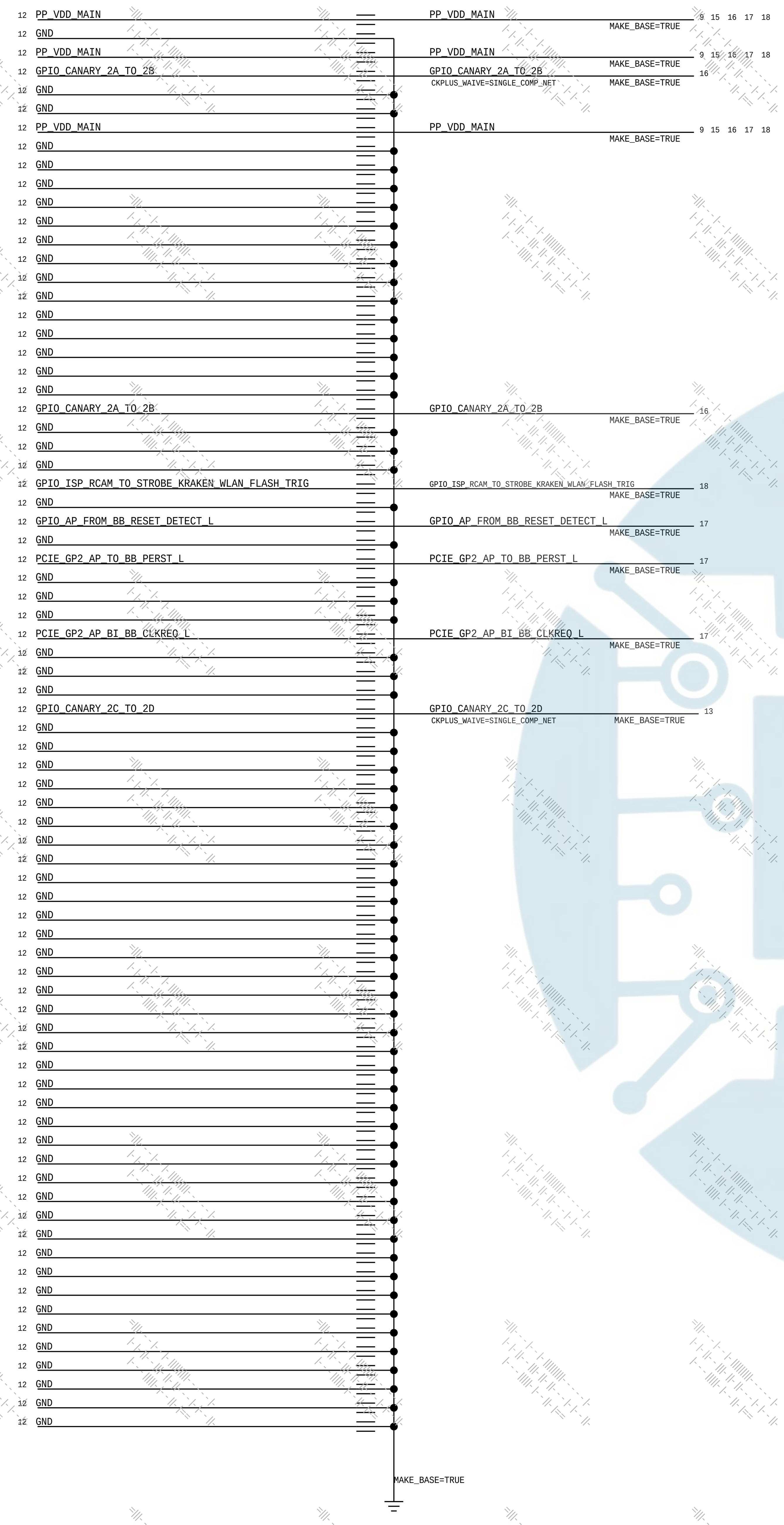
Interposer: Symbol 4 Aliases

LEFT SIDE



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HIERARCHIES

POWER

55 21 18 17 16 15 9 PP_VDD_MAIN
22 15 PP_VDD_BOOST
26 14 PP1V2_S2
55 47 18 17 13 PP1V2_S4
48 18 15 PP1V8_S2
55 47 18 17 14 PP1V8_S4
30 15 PP3V0_S2
22 15 PP_VDD_RF_1V2
31 14 PP_1V8_LDO6
22 15 PP_UIM1_LDO11
22 15 PP_UIM2_LDO13

PCIE

26 14 90_PCIE_GP2_AP_TO_BB_TX_N
26 14 90_PCIE_GP2_AP_TO_BB_TX_P
26 14 90_PCIE_GP2_AP_FROM_BB_RX_N
26 14 90_PCIE_GP2_AP_FROM_BB_RX_P
26 14 90_PCIE_GP2_AP_TO_BB_REFCLK_N
26 14 90_PCIE_GP2_AP_TO_BB_REFCLK_P
26 14 GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L
26 16 PCIE_GP2_AP_BI_BB_CLKREQ_L
26 16 PCIE_GP2_AP_TO_BB_PERST_L

90_PCIE_AP_TO_BB_TX_N
90_PCIE_AP_TO_BB_TX_P
90_PCIE_BB_TO_AP_RX_R_N
90_PCIE_BB_TO_AP_RX_R_P
90_PCIE_AP_TO_BB_REFCLK_N
90_PCIE_AP_TO_BB_REFCLK_P
PCIE_BB_TO_PMU_HOST_WAKE_1V2_L
PCIE_AP_BI_BB_CLKREQ_1V2_L
PCIE_AP_TO_BB_PERST_1V2_L

I2S

26 14 I2S2_AP_TO_BB_DOUT
26 14 I2S2_AP_FROM_BB_DIN
26 16 I2S2_AP_FROM_BB_BCLK
26 14 I2S2_AP_FROM_BB_LRCLK

I2S_AP_TO_BB_DOUT
I2S_BB_TO_AP_DIN
I2S_BB_TO_AP_BCLK
I2S_BB_TO_AP_WCLK

CONTROL

26 15 GPIO_AP_TO_BB_COREDUMP
23 15 GPIO_SEQ_PMU_TO_BBPMU_RESET_L
26 15 GPIO_AP_TO_BB_TIME_MARK
26 13 GPIO_AP_TO_BB_PEAK_PWR_IND
23 14 IO_TOUCH_TO_MANY_SCAN_ACTIVE
23 14 GPIO_AOP_TO_BB_FORCE_PWM
26 16 GPIO_BB_TO_ALS_GSM_BURST_IND_1V8
26 16 GPIO_AP_FROM_BB_RESET_DETECT_L

AP_TO_BB_COREDUMP_TRIG_1V2
APPMU_TO_BBPMU_RESET_L
AP_TO_BB_GPS_TIME_MARK_1V2
AP_TO_BB_PEAK_POWER_IND_1V2
BBPMU_QUIET_MODE_REQ1
BBPMU_QUIET_MODE_REQ2
BB_TO_AP_GSM_TXBURST_IND_1V8
BB_TO_AP_RESET_DET_1V2_L

R13810
33.2
1%
1/32W
MF
01005
ROOM=BBPMU

13 CLK_BBPMU_TO_DOTARA_38M4 1 2 CLK_BBPMU_TO_DOTARA_38M4_R 17 23

SWD

26 13 SWD_AP_TO_MANY_SWCLK
26 13 SWD_AP_BI_BB_SWDIO

BB_JTAG_TCK_SWD_CLK
BB_JTAG_TMS_SWD_IO

DOTARA

23 14 GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA
23 17 CLK_BBPMU_TO_DOTARA_38M4_R

DOTARA_TO_BBPMU_CLKREQ
SHIELD_DOTARA_38P4M_CLK

AOP UART

26 15 UART1_AOP_TO_BB_TXD
26 15 UART1_AOP_FROM_BB_RXD

UART_AOP_TO_BB_TXD
UART_BB_TO_AOP_RXD

WLAN UART/RFFE

26 18 UART_BB_TO_WLAN_RX
26 18 UART_BB_TO_WLAN_TX

UART_WLAN_TO_BB_COEX_RX_1V2
UART_BB_TO_WLAN_COEX_TX_1V2

47 18 14 SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
47 18 13 SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA

SHIELD_RFFE_SCLK_WLAN_SU
SHIELD_RFFE_SDATA_WLAN_SU

R1

26 13 GPIO_BB_TO_R1_CH9_REQ
26 13 GPIO_BB_TO_R1_COEX
26 13 GPIO_R1_TO_BB_CH9_COEX
26 13 GPIO_R1_TO_BB_LAA_SW_CTRL

BB_TO_R1_CH9_REQ
BB_TO_R1_LAA_REQ
R1_TO_BB_CH9_COEX
R1_TO_LAA_SW_CTRL

NFC

23 14 CLK_BBPMU_TO_NFC_38M
23 14 GPIO_NFC_TO_BBPMU_CLK_EN

SHIELD_STOCKHOLM_38P4M_CLK
STOCKHOLM_TO_BBPMU_CLKREQ

SIM

26 15 IO_BB_TO_SIM1_CLK
26 15 IO_BB_BI_SIM1_DATA
26 15 IO_BB_FROM_SIM1_DETECT
26 15 IO_BB_TO_SIM1_RESET
26 15 IO_BB_TO_SIM2_CLK
26 15 IO_BB_BI_SIM2_DATA
26 15 IO_BB_FROM_SIM2_DETECT
26 15 IO_BB_TO_SIM2_RESET

BB_SIM1_CLK
BB_SIM1_DATA
BB_SIM1_DETECT
BB_SIM1_RESET
BB_SIM2_CLK
BB_SIM2_DATA
BB_SIM2_DETECT
BB_SIM2_RESET

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ET/APT IC

PP_APT_L_PA 14 30
SHIELD_ETDAC_QET1_P 14 29
SHIELD_ETDAC_QET1_N 14 29

PP_VDD_MAIN
PP_VDD_BOOST
PP1V2_S2
PP1V2_S4
PP1V8_S2
PP1V8_S4
PP3V0_S2
PP_VDD_RF_1V2
PP_LDO6_VIO_1V8
PP_UIM1_LDO11
PP_UIM2_LDO13

RF RFFE

SHIELD_RFFE1_SCLK_SDR 15 30
SHIELD_RFFE1_SDATA_SDR 15 30
SHIELD_RFFE2_SCLK_SDR 15 30
SHIELD_RFFE2_SDATA_SDR 15 30
SHIELD_RFFE3_SCLK_SDR 15 30
SHIELD_RFFE3_SDATA_SDR 15 30
SHIELD_RFFE5_SCLK_SDR 13 30
SHIELD_RFFE5_SDATA_SDR 13 30
SHIELD_RFFE8_SCLK_SDR 14 30
SHIELD_RFFE8_SDATA_SDR 14 30

SHIELD_RFFE1_SCLK_SDR
SHIELD_RFFE1_SDATA_SDR
SHIELD_RFFE2_SCLK_SDR
SHIELD_RFFE2_SDATA_SDR
SHIELD_RFFE3_SCLK_SDR
SHIELD_RFFE3_SDATA_SDR
SHIELD_RFFE5_SCLK_SDR
SHIELD_RFFE5_SDATA_SDR
SHIELD_RFFE8_SCLK_SDR
SHIELD_RFFE8_SDATA_SDR

LB PAD

50_TX_IN_XCVR_TX1_LB_JB 14 30
50_TX_IN_XCVR_TX0_LB 14 30
50_RX_XCVR_PRX6_LB_A_RX0 14 30
50_RX_XCVR_PRX10_LB_PRX_OUT2 14 30
50_TRX_LB_PORTB_RX1_M 15 36
50_TRX_LB_PORTB_TX_M 15 36
50_TRX_IN_LMB_PAD_2G_LB_OUT_M 15 35

50_TX_IN_XCVR_TX1_LB_JB
50_TX_IN_XCVR_TX0_LB
50_RX_XCVR_PRX6_LB_A_RX0
50_RX_XCVR_PRX10_LB_PRX_OUT2
50_TRX_LB_PORTB_RX1_M
50_TRX_LB_PORTB_TX_M
50_TRX_IN_LMB_PAD_2G_LB_OUT_M

UHB PA

50_RX_XCVR_PRX14_N79_RX_OUT1 14 30
50_RX_XCVR_PRX15_N79_RX_OUT2 14 30
50_RX_XCVR_PRX16_UHB_RX_OUT1 14 30
50_RX_XCVR_PRX17_UHB_RX_OUT2 14 30
50_TX_IN_TX2_UHB_PAD_TX_N79_IN 14 30
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 14 30
50_UHB_L_CPLR_OUT 14 30

50_RX_XCVR_PRX14_N79_RX_OUT1
50_RX_XCVR_PRX15_N79_RX_OUT2
50_RX_XCVR_PRX16_UHB_RX_OUT1
50_RX_XCVR_PRX17_UHB_RX_OUT2
50_TX_IN_TX2_UHB_PAD_TX_N79_IN
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1
50_UHB_L_CPLR_OUT

LAA

50_TRX_WLAN_G_BT_ANT4_NPLXR 18 45
50_LAA_RX_XCVR_DRX10 13 30
50_LAA_RX_XCVR_PRX12 15 30

50_TRX_WLAN_G_BT_ANT4_NPLXR
50_LAA_RX_XCVR_DRX10
50_LAA_RX_XCVR_PRX12

LAT

LAT_SUBUS_A 14 48
LAT_SUBUS_B 15 48
LAT_SUBUS_C 15 48

SUBUS_LAT_A
SUBUS_LAT_B
SUBUS_LAT_C

50_CPLR_L_CPL1_LAT_OUT 15 30
50_TRX_HB_PAD_ANT1 15 34
50_TRX_HB_PAD_ANT2_M 15 34
50_TRX_L5_LNA_IN 15 43

50_CPLR_L_CPL1_LAT_OUT
50_TRX_HB_PAD_ANT1
50_TRX_HB_PAD_ANT2_M
50_TRX_L5_LNA_IN

UAT

UAT_SUBUS_A 14 47
UAT_SUBUS_B 14 47
UAT_TUNER_TO_R1_STATE 13 47
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M 13 44
50_TRX_ANT2_LB_LMB_MB_HB_L1
50_TRX_ANT4_MB_HB_WLAN24 13 45
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M 13 38
50_TRX_UHB_PAD_N79_PORTB_TX_M 14 38
50_TRX_UHB_PAD_PORTB_TX_M 14 39

SUBUS_UAT_A
SUBUS_UAT_B
UAT_TUNER_TO_R1_STATE
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M
50_TRX_ANT2_LB_LMB_MB_HB_L1
50_TRX_ANT4_MB_HB_WLAN24
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M
50_TRX_UHB_PAD_N79_PORTB_TX_M
50_TRX_UHB_PAD_PORTB_TX_M

POWER

55 21 18 17 16 15 9 PP_VDD_MAIN
55 47 18 17 14 PP1V8_S4
55 47 18 17 13 PP1V2_S4
55 15 PP1V2_NFC_S2

PP_VDD_MAIN
PP1V8_S4
PP1V2_S4
PP1V2_NFC_P_S2

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CONTROL

55 15 GPIO_SEQ_PMU_TO_NFC_EN

PMU_TO_NFC_P_EN

NFC I2C

55 13 I2C_R1_TO_NFC_SCL
55 13 I2C_R1_TO_NFC_SDA
55 18 I2C_BT_TO_NFC_SCL
55 18 I2C_BT_TO_NFC_SDA

I2C_R1_TO_SE_SCL
I2C_R1_TO_SE_SDA
I2C_BT_TO_NFC_P_SCL
I2C_BT_TO_NFC_P_SDA

NFC RF

56 13 NFC_P_ANT_POS
56 13 NFC_P_ANT_NEG

NFC_P_ANT_POS
NFC_P_ANT_NEG

NFC SPMI

55 19 13 SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
55 17 SPMI0_EVENTS_AOP_BI_NFC_P_DATA_R

SPMI_AOP_TO_RADIOS_CLK
SPMI_AOP_TO_RADIOS_DATA

MISC

55 18 GPIO_SE_TO_BT_PKT_RDY
55 13 NTC_STOCKHOLM
55 15 GPIO_NFC_TO_ARCAMP_RESET_L
55 15 GPIO_NFC_TO_ARCAMP_TRIG
55 13 NFC_P_TEST_OUT
55 13 GPIO_NFC_F_NFC_P_SYNC1
55 13 GPIO_NFC_F_NFC_P_SYNC2
55 13 IO_TOUCH_TO_MANY_SCAN_ACTIVE_U

IO_SE_TO_BT_PKT_READY
NFC_P_THERMISTOR_UAT2
NFC_P_THERMISTOR_UAT4
NC
NFC_P_TO_ARC_RESET_L
NFC_P_TO_ARC_TRIG
NFC_P_TEST_OUT
NFC_F_TO_NFC_P_COEX
NFC_P_TO_NFC_F_COEX
TOUCH_TO_NFC_SCAN_ACTIVE

ROOM=NFC
R13800
33.2
1%
1/32W
MF
01005

18 13 SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA 1 2 SPMI0_EVENTS_AOP_BI_NFC_P_DATA_R 17 55

PAGE TITLE
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HIERARCHIES

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POWER

- PP_VDD_MAIN_THELONIOUS
- PP_VDD_MAIN_2GFEMU
- PP_VDD_MAIN_2GFEML
- PP1V8_S4
- PP1V2_S4
- PP1V8_S2

PMU

- CLK_GPIO_PMU_TO_WLAN_R1_32K
- GPIO_PMU_TO_WLAN_REG_ON
- GPIO_PMU_FROM_WLAN_HOST_WAKE

PCIE

- 90_PCIE_WLAN_TO_AP_TX_P
- 90_PCIE_WLAN_TO_AP_TX_N
- 90_PCIE_AP_TO_WLAN_TX_P
- 90_PCIE_AP_TO_WLAN_TX_N
- 90_PCIE_AP_TO_WLAN_REFCLK_P
- 90_PCIE_AP_TO_WLAN_REFCLK_N
- PCIE_AP_TO_WLAN_PERST_1V2_L
- PCIE_AP_BI_WLAN_CLKREQ_L

SPMI

- SPMI_EVENTS_AOP_TO_WLAN_NFC_DATA
- SPMI_EVENTS_AOP_TO_WLAN_NFC_CLK

- WLAN_TO_AP_TIME_SYNC_1V2
- BT_TO_AP_AUDIO_SYNC
- BT_TO_ISP_STROBE_SYNC

CONTEXT

- GPIO_AOP_TO_WLAN_CONTEXT_B
- GPIO_AOP_TO_WLAN_CONTEXT_A

BOT_SPK

- BT_TO_BOT_SPK_TRIG

R1

- BT_TO_R1_TIME_SYNC
- BT_TO_R1_WAKE
- WLAN_TO_R1_COEX
- R1_TO_WLAN_COEX

SE

- I2C_BT_TO_SE_SCL
- I2C_BT_TO_SE_SDA
- IO_SE_TO_BT_PKT_READY

RFFE

- SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
- SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
- SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK
- SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA
- RFFE_WLAN_TO_UAT_5G_FEM_RST_L
- RFFE_WLAN_TO_LAT_5G_FEM_RST_L

- GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN
- GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN

RF UAT

- 50_WLAN_G_BT_ANT4_NPLXR
- 50_WLAN_A_C0_TXRX_FEM_M
- ANALOG_UAT_5G_FEM_TO_WLAN_PDTS

RF LAT

- 50_WLAN_A_C1_TXRX_FEM_M
- 50_WLAN_G_BT_ANT3_NPLXR
- ANALOG_LAT_5G_FEM_TO_WLAN_PDTS

COEX

- UART_BB_TO_WLAN_COEX_1V2
- UART_WLAN_TO_BB_COEX_1V2

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60 59 58 17 16 15 9 PP_VDD_MAIN

58 17 14 PP1V8_S4
58 17 13 PP1V2_S4
60 17 15 PP1V8_S2

58 14 CLK_GPIO_S4_PMU_TO_WLAN_R1_32K
58 18 14 GPIO_S4_PMU_TO_WLAN_REG_ON
58 14 GPIO_PMU_FROM_WLAN_HOST_WAKE

58 14 90_PCIE_GP1_AP_FROM_WLAN_RX_P
58 14 90_PCIE_GP1_AP_FROM_WLAN_RX_N
58 14 90_PCIE_GP1_AP_TO_WLAN_TX_P
58 14 90_PCIE_GP1_AP_TO_WLAN_TX_N
58 14 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P
58 14 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N
58 13 PCIE_GP1_AP_TO_WLAN_PERST_L
58 13 PCIE_GP1_AP_BI_WLAN_CLKREQ_L

58 18 SPMI0_EVENTS_AOP_BI_WLAN_DATA_R
58 17 13 SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK

58 13 GPIO_AP_FROM_WLAN_TIME_SYNC
58 15 GPIO_AP_FROM_BT_AUDIO_SYNC
58 16 GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG

58 14 GPIO_AOP_TO_WLAN_CONTEXT_B
58 14 GPIO_AOP_TO_WLAN_CONTEXT_A

58 15 GPIO_BT_TO_BOT_SPKR_TRIG

IO_BT_TO_R1_TIME_SYNC 13 58
IO_BT_TO_R1_WAKE 13 58
GPIO_WLAN_TO_R1_COEX 13 58
GPIO_R1_TO_WLAN_COEX 13 58

I2C_BT_TO_NFC_SCL 17 58
I2C_BT_TO_NFC_SDA 17 58
GPIO_SE_TO_BT_PKT_RDY 17 58

SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK 14 17 58
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA 13 17 58
SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK 15 58
SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA 15 58
RFFE_WLAN_TO_UAT_5G_FEM_RST_L 14 58
RFFE_WLAN_TO_LAT_5G_FEM_RST_L 15 58

GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN 14 58
GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN 15 58

50_TRX_WLAN_G_BT_ANT4_NPLXR 17 59
50_WLAN_A_C0_TXRX_FEM_M 13 58
ANALOG_UAT_5G_FEM_TO_WLAN_PDTS 14 58

50_WLAN_A_C1_TXRX_FEM_M 15 58
50_TRX_WLAN_G_BT_ANT3_NPLXR 15 60
ANALOG_LAT_5G_FEM_TO_WLAN_PDTS 14 58

UART_BB_TO_WLAN_TX 17 58
UART_BB_TO_WLAN_RX 17 58

58 18 14 GPIO_S4_PMU_TO_WLAN_REG_ON

R13900
200K
1%
1/32W
MF
01005
ROOM=WLAN

RADAR #: 58574355

17 13 SPMI0_EVENTS_AOP_BI_WLAN_NFC_DATA

R0947
33.2
1%
1/32W
MF
01005
ROOM=DFM

SPMI0_EVENTS_AOP_BI_WLAN_DATA_R 18 58

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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0024124377	ENGINEERING RELEASED	2020-07-01

MAV20 HIER_RADIO_MAV_BOT

LAST_MODIFICATION=Wed Jul 1 15:22:37 2020

X1804

POWER

PP_VDD_MAIN IN 3 5 13 14 15 31 32 34
PP_VDD_BOOST VOLTAGE=4.5 IN 4 16 17 19 20 23 31 32
PP1V2_S2 IN 8
PP1V2_S4 IN 29
PP1V8_S2 IN 30 32
PP1V8_S4 IN 29
PP3V0_S2 IN 12 31 32
PP_1V8_LDO6 OUT 4 13 14 15 16 17 18 19 20 21 22 23
PP_VDD_RF_1V2 OUT 4 16 17 18 19 20 21 22 24 25

PCIE

GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L OUT 8 31 32
PCIE_GP2_AP_TO_BB_PERST_L IN 8 31
PCIE_GP2_AP_BI_BB_CLKREQ_L IO 8 31 32
90_PCIE_GP2_AP_FROM_BB_RX_P OUT 8 31
90_PCIE_GP2_AP_FROM_BB_RX_N OUT 8 31
90_PCIE_GP2_AP_TO_BB_TX_P IN 8 31
90_PCIE_GP2_AP_TO_BB_TX_N IN 8 31
90_PCIE_GP2_AP_TO_BB_REFCLK_P OUT 8 31
90_PCIE_GP2_AP_TO_BB_REFCLK_N OUT 8 31

SIM

PP_UIM1_LDO11 OUT 4 6 28 31
IO_BB_TO_SIM1_RESET OUT 8 31
IO_BB_BI_SIM1_DATA IO 8 28 31
IO_BB_TO_SIM1_CLK OUT 8 31
IO_BB_FROM_SIM1_DETECT OUT 8 28 31

PP_UIM2_LDO13 OUT 4 6 28 31
IO_BB_TO_SIM2_RESET OUT 8
IO_BB_BI_SIM2_DATA IO 8 28
IO_BB_TO_SIM2_CLK OUT 8
IO_BB_FROM_SIM2_DETECT OUT 8 28

I2S

I2S2_AP_FROM_BB_DIN OUT 8 31
I2S2_AP_TO_BB_DOUT IN 8 31
I2S2_AP_FROM_BB_BCLK OUT 8 31
I2S2_AP_FROM_BB_LRCLK OUT 8 31

CONTROL

GPIO_AP_FROM_BB_RESET_DETECT_L OUT 8 31
GPIO_SEQ_PMU_TO_BBPMU_RESET_L IN 5 31 32
GPIO_AP_TO_BB_COREDUMP IN 8 31
GPIO_BB_TO_ALS_GSM_BURST_IND_1V8 OUT 8 31
IO_TOUCH_TO_MANY_SCAN_ACTIVE IN 5 31
GPIO_AOP_TO_BB_FORCE_PWM IN 5 31
GPIO_AP_TO_BB_TIME_MARK IN 8 31
GPIO_AP_TO_BB_PEAK_PWR_IND IN 8 31

SWD

SWD_AP_TO_MANY_SWCLK IN 8 31
SWD_AP_BI_BB_SWDIO IO 8 31

DOTARA

GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA IN 5 31
CLK_BBPMU_TO_DOTARA_38M4_R OUT 5 31

AOP UART

UART1_AOP_TO_BB_TXD IN 8 31
UART1_AOP_FROM_BB_RXD OUT 8 31

WLAN UART/RFFE

UART_BB_TO_WLAN_TX OUT 8 31
UART_BB_TO_WLAN_RX IN 8 31
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK IN 29
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA IO 29

R1

GPIO_BB_TO_R1_COEX OUT 8 31
GPIO_BB_TO_R1_CH9_REQ OUT 8 31
GPIO_R1_TO_BB_CH9_COEX IN 8 31
GPIO_R1_TO_BB_LAA_SW_CTRL IN 8 31

NFC

CLK_BBPMU_TO_NFC_38M OUT 5 31
GPIO_NFC_TO_BBPMU_CLK_EN IN 5 31

ET/APT IC

SHIELD_ETDAC_QET1_P OUT 11
SHIELD_ETDAC_QET1_N OUT 11
SHIELD_RFFE8_SDATA_SDR IO 1 12 31
SHIELD_RFFE8_SCLK_SDR OUT 1 12 31
PP_APT_L_PA VOLTAGE=5.5 OUT 15

RF RFFE

SHIELD_RFFE1_SCLK_SDR OUT 12 13 16 17 31
SHIELD_RFFE1_SDATA_SDR IO 12 13 16 17 31
SHIELD_RFFE2_SCLK_SDR OUT 12 15 31
SHIELD_RFFE2_SDATA_SDR IO 12 15 31
SHIELD_RFFE3_SCLK_SDR OUT 12 16 17 21 31
SHIELD_RFFE3_SDATA_SDR IO 12 16 17 21 31
SHIELD_RFFE5_SCLK_SDR OUT 12 18 19 20 22 31
SHIELD_RFFE5_SDATA_SDR IO 12 18 19 20 22 31
SHIELD_RFFE8_SDATA_SDR IO 1 12 31
SHIELD_RFFE8_SCLK_SDR OUT 1 12 31

LB PAD

50_TX_IN_XCVR_TX1_LB_JB OUT 12
50_TX_IN_XCVR_TX0_LB OUT 12
50_RX_XCVR_PRX6_LB_A_RX0 IN 12
50_RX_XCVR_PRX10_LB_PRX_OUT2 IN 12
50_TRX_LB_PORTB_RX1_M IN 18
50_TRX_LB_PORTB_TX_M IO 18
50_TRX_IN_LMB_PAD_2G_LB_OUT_M IO 17

UHB PA (LAT)

50_RX_XCVR_PRX14_N79_RX_OUT1 IN 12
50_RX_XCVR_PRX15_N79_RX_OUT2 IN 12
50_RX_XCVR_PRX16_UHB_RX_OUT1 IN 12
50_RX_XCVR_PRX17_UHB_RX_OUT2 IN 12
50_TX_IN_TX2_UHB_PAD_TX_N79_IN OUT 12
50_TX_IN_TX2_UHB_PAD_TX_UHB_IN_1 OUT 12
50_UHB_L_CPLR_OUT IN 12
50_TRX_UHB_PAD_PORTB_TX_M OUT 20
50_TRX_UHB_PAD_N79_PORTB_TX_M OUT 20

LAA

50_TRX_WLAN_G_BT_ANT4_NPLXR IO 27
50_LAA_RX_XCVR_DRX10 IN 12
50_LAA_RX_XCVR_PRX12 IN 12

LAT

SUBUS_LAT_A OUT 30
SUBUS_LAT_B OUT 30
SUBUS_LAT_C OUT 30

50_TRX_HB_PAD_ANT1 OUT 16
50_CPLR_L_CPL1_LAT_OUT IN 12
50_TRX_L5_LNA_IN IN 25
50_TRX_HB_PAD_ANT2_M OUT 16

UAT

SUBUS_UAT_A OUT 29
SUBUS_UAT_B OUT 29

UAT_TUNER_TO_R1_STATE OUT 29

50_TRX_ANT2_LB_LMB_MB_HB_L1 OUT 23
50_TRX_ANT4_MB_HB_WLAN24 OUT 27
50_TRX_PAUHBU_UHB_ANT2_TO_ANT8_M IO 26
50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M IO 20

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BOM TABLES AND CONSTRAINTS

ALT TABLES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00250	197S00249	?	Y601_E	TXC,38.4MHZ,8PF,1612

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01228	152S01120	?	L405_E	SEMCO,1.0UH,3.4A

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00013	335S0894	?	EEPROM_E	EEPROM,8KBIT,I2C

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339M00113	339S00112	?	U_TAN_E	MODULE,ES2.3,U,LGA388

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339M00115	339M00116	?	U_BG1_E	ANT,ES3.1,USI,LGA376

OMIT TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S00050	1	RES,MF,5.6K OHM,1%,1/32W,01005	R630_E	?	RF_SKU:WW+KOLKATA
118S0730	1	RES,MF,12K OHM,1%,1/32W,01005	R630_E	?	RF_SKU:NAJP
118S00088	1	RES,MF,19.1K OHM,1%,1/32W,01005	R630_E	?	RF_SKU:ROW
118S00122	1	RES,MF,27K OHM,1%,1/32W,01005	R630_E	?	RF_SKU:NAMM
353S02396	1	IC,LB DSM,WW,MCD,LMRXFNJB-K79,DSLGA20	DSM_LB_E	CRITICAL	RF_SKU:NAJP&RF_SKU:NAMM
353S02397	1	IC,LB DSM,ROW,MCD,LMRXFNJB-K83,DSLGA20	DSM_LB_E	CRITICAL	RF_SKU:ROW
353S02393	1	IC,2G-LMB PAD,SKYS8232,DSBGA79	PA_LMB_E	CRITICAL	RF_SKU:NAJP
353S02401	1	IC,2G-LMB PAD,ROW,SKYS8242,DSBGA79	PA_LMB_E	CRITICAL	RF_SKU:ROW&RF_SKU:NAMM
353S02391	1	IC,HB TX DSM,WW,HFQTWLQFA-580,DSLGA61	DSM_HB_E	CRITICAL	RF_SKU:NAJP
353S02392	1	IC,HB TX DSM,ROW,HFQTWLQFA-583,DSLGA61	DSM_HB_E	CRITICAL	RF_SKU:ROW&RF_SKU:NAMM
118S00122	1	RES,MF,27K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:PROTO2
118S00193	1	RES,MF,36.5K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:EVT
118S0868	1	RES,MF,47.5K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:
118S00136	1	RES,TK,60.4K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:DVT
118S0768	1	RES,MF,75K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:PVT
118S0688	1	RES,MF,143K OHM,1%,1/32W,01005	R631_E	?	BOARD_REV:EVT_DOE

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BB PMU: SMPS

SMPS INPUT CAPS

PP_VDD_MAIN
MAKE_BASE=TRUE
C401_E 15UF 20% 6.3V X5R 0402-0.1MM-1
C406_E 2.2UF 20% 6.3V X5R-CERM 0201
C402_E 2.2UF 20% 6.3V X5R-CERM 0201
C405_E 2.2UF 20% 6.3V X5R-CERM 0201
C412_E 2.2UF 20% 6.3V X5R-CERM 0201
C407_E 2.2UF 20% 6.3V X5R-CERM 0201
C427_E 15UF 20% 6.3V X5R 0402-0.1MM-1
C403_E 2.2UF 20% 6.3V X5R-CERM 0201
C404_E 2.2UF 20% 6.3V X5R-CERM 0201
GND
SHARE S7 INPUT POWER ROUTES WITH S5 CAP
C411_E 15UF 20% 6.3V X5R 0402-0.1MM-1

PMX_REF_BYP
C509_E 0.1UF 20% 6.3V X5R-CERM 01005
PMX_REF_BYP_GND
XW407_E SHORT-10L-0.1MM-SM

PART_NUMBER=338S00620
ROOM=BBPMU
UBBPMU_E
PMX55-0
FOWPSP
SYM 5 OF 6
VREG1
CRITICAL

REF_BYP 32
REF_GND 49

VDD_S1 137 138
VDD_S2 59 68
VDD_S3 144 145
VDD_S4 76 77 85
VDD_S5 1 10
VDD_S6 78 87
VDD_S7 3 11
VDD_S8 NC 61 NC 69

VSW_S1 120 129
VSW_S2 51 60
VSW_S3 128 136
VSW_S4 93 94 102
VSW_S5 18 19
VSW_S6 86 95
VSW_S7 4 12
VSW_S8 44 NC 52 NC

VFB_S1 70
VFB_S2 34
VFB_S3 126
VFB_S4 135
VFB_S5 45
VFB_S6 62
VFB_S7 20
VFB_S8 53 NC

S8 FOR BACKUP ONLY
NOT ENOUGH ROOM ON

VSW_SMPS1
REMOTE SENSE
CONNECT TO LOAD
VREG_S1_S6_SENSE_P
L401_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM
VOLTAGE=0.752V IPEAK: 7.8A
PP_0V75_SMPS1_6
VSW_SMPS2
L402_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM
VOLTAGE=1.224V IPEAK: 3.19A
PP_1V22_SMPS2
C429_E 20UF 20% 4V X5R 0402-0.1MM
PP_1V24_SMPS2_SNS
XW404_E SHORT-10L-0.1MM-SM
VSW_SMPS3
L403_E 152S01273 0.47UH-20%-4.8A-0.027OHM MCFE2016-SM-1
VOLTAGE=0.824V IPEAK: 3.59A
PP_0V82_SMPS3
C430_E 20UF 20% 4V X5R 0402-0.1MM
C434_E 20UF 20% 4V X5R 0402-0.1MM
PP_0V82_SMPS3_SNS
XW402_E SHORT-10L-0.1MM-SM
VSW_SMPS4
L404_E 152S01120 1.0UH-3.4A-0.053OHM PIJF2016FE-SM
VOLTAGE=1.88V IPEAK: 0.903A
PP_1V9_SMPS4
C431_E 20UF 20% 4V X5R 0402-0.1MM
C409_E 20UF 20% 4V X5R 0402-0.1MM
PP_1V9_SMPS4_SNS
XW403_E SHORT-10L-0.1MM-SM
VSW_SMPS5
L405_E 152S01120 1.0UH-3.4A-0.053OHM PIJF2016FE-SM
VOLTAGE=0.752V IPEAK: 2.39A
PP_0V75_SMPS5
C432_E 20UF 20% 4V X5R 0402-0.1MM
PP_0V75_SMPS5_SNS
XW405_E SHORT-10L-0.1MM-SM
VSW_SMPS6
L406_E 152S01227 0.47UH-20%-4.9A-0.025OHM CIGT2016-SM
PP_0V75_SMPS1_6
REMOTE SENSE
CONNECT TO LOAD
VREG_S1_S6_SENSE_P
VSW_SMPS7
L407_E 152S01273 0.47UH-20%-4.8A-0.027OHM MCFE2016-SM-1
VOLTAGE=0.752V IPEAK: 3.05A
PP_0V75_SMPS7
C433_E 20UF 20% 4V X5R 0402-0.1MM
C435_E 4UF 20% 6.3V CER-X5R 0201
PP_0V75_SMPS7_SNS
XW401_E SHORT-10L-0.1MM-SM

PART_NUMBER=338S00620
ROOM=BBPMU
UBBPMU_E
PMX55-0
FOWPSP
SYM 3 OF 6
CRITICAL

GND_S1 112 121
GND_S2 42 43
GND_S3 119 127
GND_S4 110 111
GND_S5 27 28
GND_S6 103 104
GND_S7 13 21
GND_S8 35 36
CMN_GND 47 56 64 65 73 81 82 90
RMT_GND_S1 96
RMT_GND_S6 88
RMT_GND_S8 79
VREG_S1_S6_SENSE_N

AVDD_BYP 108 AVDD_BYP_PMIC
DVDD_BYP 116 DVDD_BYP_PMIC
C408_E 1.0UF 20% 10V X5R-CERM 0201-1 DVDD_BYP_GND
XW408_E SHORT-10L-0.1MM-SM
C410_E 1.0UF 20% 10V X5R-CERM 0201-1 AVDD_BYP_GND
XW406_E SHORT-10L-0.1MM-SM

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BB PMU: LDOS

UBBPMU_E
PMX55-0
FOWPSP
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PART_NUMBER=338S00620
ROOM=BBPMU

VREG2
CRITICAL

PP_1V2_LDO15	33	VDD_AP_IO				
PP_1V22_SMPS2	17, 25	VDD_L1_L2	VREG_L1	9, 26	VOLTAGE: 1.2V IPEAK: 1.2A	PP_1V2_LDO1
			VREG_L2	8	VOLTAGE: 1.128V IPEAK: 0.324A	PP_1V1_LDO2
PP_0V82_SMPS3	124	VDD_L3_L9	VREG_L3	132	VOLTAGE: 0.8V IPEAK: 1.28A	PP_0V8_LDO3
			VREG_L9	115	VOLTAGE: 0.8V IPEAK: 0.283A	PP_0V8_LDO9
PP_1V22_SMPS2	15, 24	VDD_L4_L12	VREG_L4	16	VOLTAGE: 0.912V IPEAK: 1.85A	PP_0V875_LDO4
			VREG_L12	7	VOLTAGE: 1.2V IPEAK: 0.586A	PP_1V2_LDO12
PP_1V9_SMPS4	134	VDD_L5_L6	VREG_L5	143	VOLTAGE: 1.8V IPEAK: 0.178A	PP_1V8_LDO5
			VREG_L6	142	VOLTAGE: 1.8V IPEAK: 0.229A	PP_1V8_LDO6
PP_0V82_SMPS3	123, 131	VDD_L7_L8	VREG_L7	140	VOLTAGE: 0.744V IPEAK: 1.18A	PP_0V8_LDO7
			VREG_L8	139	VOLTAGE: 0.744V IPEAK: 0.825A	PP_0V8_LDO8
PP_VDD_BOOST	48	VDD_L10_L11_L13	VREG_L10	40	VOLTAGE: 3.088V IPEAK: 0.0082A	PP_3V1_LDO10
			VREG_L11	31	VOLTAGE: 2.848V IPEAK: 0.07A	PP_UIM1_LDO11
			VREG_L13	39	VOLTAGE: 2.848V IPEAK: 0.07A	PP_UIM2_LDO13
PP_0V75_SMPS7	14	VDD_L14	VREG_L14	5	VOLTAGE: 0.624V IPEAK: 0.369A	PP_0V6_LDO14
PP_1V22_SMPS2	23	VDD_L15	VREG_L15	6	VOLTAGE: 1.2V IPEAK: 0.03A	PP_1V2_LDO15
PP_1V9_SMPS4	133	VDD_L16	VREG_L16	141	VOLTAGE: 1.864V IPEAK: 0.418A	PP_1V7_LDO16
			VREG_L14_S	22	PP_0V6_LDO14_SNS	

ROOM=BBPMU
C528_E
2.2UF
20%
6.3V
X5R-CERM
0201

XW501_E
SHORT-10L-0.1MM-SM
ROOM=BBPMU

C511_E	4UF	20%	6.3V	CER-X5R	0201
C512_E	4UF	20%	6.3V	CER-X5R	0201
C513_E	4UF	20%	6.3V	CER-X5R	0201
C514_E	4UF	20%	6.3V	CER-X5R	0201
C515_E	4UF	20%	6.3V	CER-X5R	0201
C516_E	4UF	20%	6.3V	CER-X5R	0201
C517_E	4UF	20%	6.3V	CER-X5R	0201
C518_E	4UF	20%	6.3V	CER-X5R	0201
C501_E	0.47UF	20%	6.3V	X5R	01005
C502_E	0.47UF	20%	6.3V	X5R	01005
C503_E	0.47UF	20%	6.3V	X5R	01005
C522_E	4UF	20%	6.3V	CER-X5R	0201
C523_E	20UF	20%	6.3V	X5R	0402-0.1MM
C524_E	4UF	20%	6.3V	CER-X5R	0201
C525_E	4UF	20%	6.3V	CER-X5R	0201
C526_E	4UF	20%	6.3V	CER-X5R	0201

C511_E–C518_E: ROOM=BBPMU, 138S00071
C522_E: ROOM=BBPMU, 138S00071
C523_E: ROOM=BBPMU, 138S00279
C524_E–C526_E: ROOM=BBPMU, 138S00071
C523_E: PATH=I62
C525_E: PATH=I38

XW502_E
SHORT-8L-0.25MM-SM
PP_1V2_LDO1 — PP_VDD_RF_1V2

MAKE_BASE=TRUE
PP_1V8_LDO6 — PP_1V8_LDO6

PMX55 LDO CAPACITOR TABLE
N1200 (L1, L2, L3, L4, L7, L8, L9, L12, L14, L15) 4.7UF MIN, 22UF MAX N1200 (L14) 2X10UF OR 1X22UF MIN, 44UF MAX
MVP150 (L10, L11, L13) 0.47UF MIN, 5UF MAX
LVP600 (L5, L6, L16) 4.7UF MIN, 23.5UF MAX

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PMIC: LDOs

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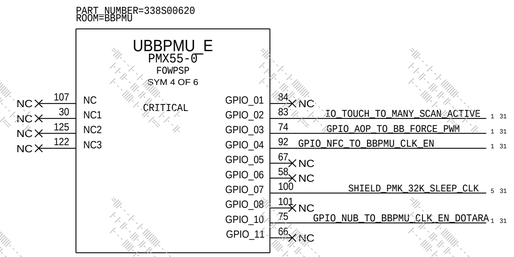
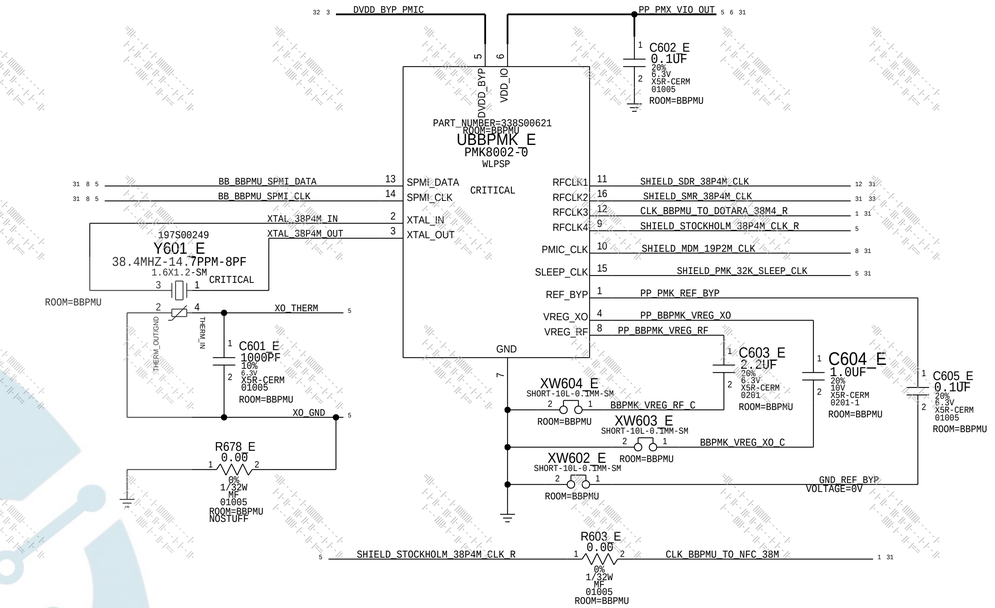
BB PMU: XTAL, CLK, ANALOG, IO

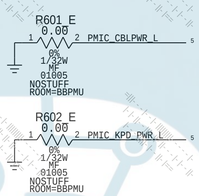
BOARD_ID	APN	R631_E	RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	PROTO0/DEV1	0X01
0.15V-0.25V	118S0730	12.0K	PROTO1/DEV2	0X02
0.25V-0.35V	118S00088	19.1K	PROTO1.5/DEV3	0X03
0.35V-0.45V	118S00122	27.0K	PROTO2/DEV4	0X04
0.45V-0.55V	118S00193	36.5K	EVT/DEV5	0X05
0.55V-0.65V	118S0868	47.5K	CARRIER/DEV6	0X06
0.65V-0.75V	118S0136	60.4K	DVT/DEV7	0X07
0.75V-0.85V	118S0768	75.0K	PVT	0X08
0.85V-0.95V	118S0626	100K	SPARE	0X09
0.95V-1.05V	118S0737	124K	SPARE	0X0A
1.05V-1.15V	118S0688	143K	EVT_DOE	0X0B
1.15V-1.25V	TBD	TBD	SPARE	SPARE

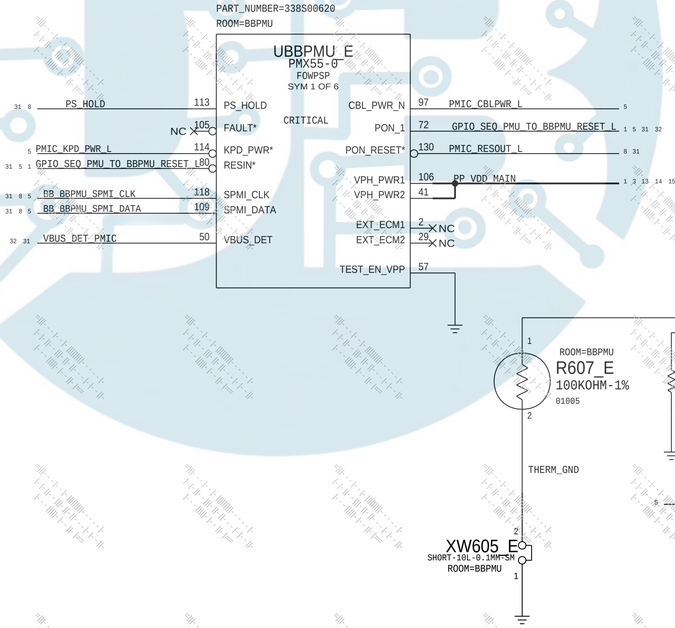
PLATFORM_ID	APN	R632_E	RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	RADIO_DEV	0X1
0.15V-0.25V	118S0730	12.0K	DARWIN_FX	0X2
0.25V-0.35V	118S00088	19.1K	DARWIN_PG	0X3
0.35V-0.45V	118S00122	27.0K	RESERVED	0X4
0.45V-0.55V	118S00193	36.5K	MAV20.1	0X5
0.55V-0.65V	118S0868	47.5K	MAV20.2	0X6
0.65V-0.75V	118S0136	60.4K	RESERVED	0X7
0.75V-0.85V	118S0768	75.0K	RESERVED	0X8
0.85V-0.95V	118S0626	100K	RESERVED	0X9
0.95V-1.05V	118S0737	124K	RESERVED	0XA
1.05V-1.15V	118S0688	143K	DEV_BEERPONG	0XB
1.15V-1.25V	TBD	TBD	SPARE	SPARE

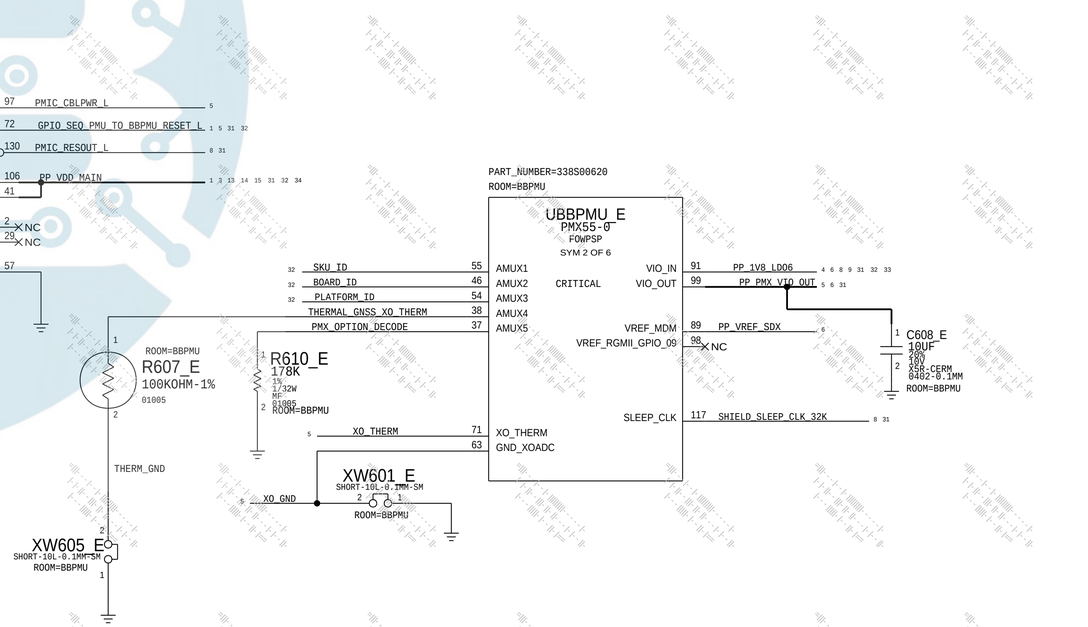
SKU_ID	APN	R630_E	RADIO_DEV	HEX
0.05V-0.15V	118S00050	5.6K	WW+KOLKATA	0X1
0.15V-0.25V	118S0730	12.0K	NAJP	0X2
0.25V-0.35V	118S00088	19.1K	ROW	0X3
0.35V-0.45V	118S00122	27.0K	NAMM	0X4
0.45V-0.55V	118S00193	36.5K	SPARE	0X5
0.55V-0.65V	118S0868	47.5K	SPARE	0X6
0.65V-0.75V	118S0136	60.4K	SPARE	0X7
0.75V-0.85V	118S0768	75.0K	SPARE	0X8
0.85V-0.95V	118S0626	100K	SPARE	0X9
0.95V-1.05V	118S0737	124K	SPARE	0XA
1.05V-1.15V	118S0688	143K	SPARE	0XB
1.15V-1.25V	TBD	TBD	SPARE	SPARE











SYNC_DATE=08/01/2019

PAGE TITLE

PMIC: CLOCKS & CONTROL

DRAWING NUMBER 051-05263 | SIZE D

REVISION 9.0.0

BRANCH 1

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SHEET 23 OF 60

BB: PDN

PART_NUMBER=337S00865 ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 5 OF 8
PWR
CRITICAL

31 6 3 PP_0V75_SMPS5
AA29 VDDCX
AB12 VDDCX
AB14 VDDCX
AB16 VDDCX
AC11 VDDCX
AC13 VDDCX
AC15 VDDCX
AC17 VDDCX
AC19 VDDCX
AC21 VDDCX
AC23 VDDCX
AC25 VDDCX
AC27 VDDCX
AC9 VDDCX
AD18 VDDCX
AD20 VDDCX
AD22 VDDCX
AD26 VDDCX
W29 VDDCX

31 6 4 3 PP_0V75_SMPS7
AB10 VDDMX
AB22 VDDMX
AB24 VDDMX
AB8 VDDMX
AD24 VDDMX
AE25 VDDMX
G23 VDDMX
G25 VDDMX
G27 VDDMX
H10 VDDMX
H8 VDDMX
K16 VDDMX
K18 VDDMX
L25 VDDMX
L27 VDDMX
M8 VDDMX
P28 VDDMX
P8 VDDMX
R19 VDDMX
R21 VDDMX
T14 VDDMX
T16 VDDMX
T28 VDDMX
T8 VDDMX
U21 VDDMX
U23 VDDMX
W13 VDDMX
W15 VDDMX
W19 VDDMX
W21 VDDMX

AA19 VDD_MODEM
AA27 VDD_MODEM
G21 VDD_MODEM
H12 VDD_MODEM
H14 VDD_MODEM
H16 VDD_MODEM
H18 VDD_MODEM
H20 VDD_MODEM
H22 VDD_MODEM
H24 VDD_MODEM
H26 VDD_MODEM
H28 VDD_MODEM
J11 VDD_MODEM
J9 VDD_MODEM
L11 VDD_MODEM
L13 VDD_MODEM
L15 VDD_MODEM
L17 VDD_MODEM
L19 VDD_MODEM
L21 VDD_MODEM
L23 VDD_MODEM
L9 VDD_MODEM
M10 VDD_MODEM
M12 VDD_MODEM
M14 VDD_MODEM
M16 VDD_MODEM
M18 VDD_MODEM
M20 VDD_MODEM
M22 VDD_MODEM
M24 VDD_MODEM
M26 VDD_MODEM
M28 VDD_MODEM
R11 VDD_MODEM
R13 VDD_MODEM
R15 VDD_MODEM
R17 VDD_MODEM
R23 VDD_MODEM
R25 VDD_MODEM
R27 VDD_MODEM
R9 VDD_MODEM
T10 VDD_MODEM
T12 VDD_MODEM
T18 VDD_MODEM
T20 VDD_MODEM
T22 VDD_MODEM
T24 VDD_MODEM
T26 VDD_MODEM
W11 VDD_MODEM
W17 VDD_MODEM
W23 VDD_MODEM
W25 VDD_MODEM
W27 VDD_MODEM
W5 VDD_MODEM
W9 VDD_MODEM
Y10 VDD_MODEM
Y12 VDD_MODEM
Y14 VDD_MODEM
Y16 VDD_MODEM
Y18 VDD_MODEM
Y20 VDD_MODEM
Y22 VDD_MODEM
Y24 VDD_MODEM
Y26 VDD_MODEM
Y28 VDD_MODEM
Y4 VDD_MODEM
Y6 VDD_MODEM
Y8 VDD_MODEM

3 PP_0V75_SMPS1_6
C761_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BASEBAND
C762_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BASEBAND
C763_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BASEBAND
C764_E 20UF 20% 4V X5R 0402-0.1MM 138S00279 ROOM=BASEBAND
NOSTUFF
XW701_E SHORT-10L-0.1MM-SM ROOM=BASEBAND
XW702_E SHORT-10L-0.1MM-SM ROOM=BASEBAND
3 VREG_S1_S6_SENSE_P
3 VREG_S1_S6_SENSE_N

33 32 31 9 8 6 5 4 PP_1V8_LDO6
31 4 PP_1V1_LDO2
C719_E C724_E C729_E 2.2UF C733_E 2.2UF C739_E C741_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
33 32 31 9 8 6 5 4 PP_1V8_LDO6
C720_E C725_E C730_E C734_E C737_E C740_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
31 5 PP_PMX_VIO_OUT
31 28 4 1 PP_UIM1_LDO11
31 28 4 1 PP_UIM2_LDO13
31 9 6 4 PP_1V2_LDO1
33 32 31 9 8 6 5 4 PP_1V8_LDO6
32 31 4 PP_1V2_LDO15
9 PP_VREF_SDX
C738_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
C789_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
C735_E 2.2UF C732_E 2.2UF C726_E 2.2UF C722_E 2.2UF C728_E 2.2UF C721_E 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=BASEBAND
C765_E 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=BASEBAND
31 8 6 4 PP_0V6_LDO14
31 4 3 PP_0V82_SMPS3
C767_E C723_E C727_E C731_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
132S00014 C736_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

AC37 VDD1
G37 VDD1
AA37 VDD2
C37 VDD2
K36 VDD2
L37 VDD2
R37 VDD2
U37 VDD2
AE37 VDDPX_3
AH2 VDDPX_3
AK22 VDDPX_3
AK34 VDDPX_3
B36 VDDPX_3
C1 VDDPX_3
R1 VDDPX_3
AG1 VDDPX_0
V2 VDDPX_4
W1 VDDPX_5
AF6 VDDPX_11
J1 VDDPX_12
AJ33 VDDPX_71
AG37 VDDPX_72
AJ21 VDDPX_73
AH4 VDDPX_74
V6 VDDPX_VBIAS_UIM
D36 VDDQ
F36 VDDQ
H36 VDDQ
M36 VDDQ
T36 VDDQ
V36 VDDQ
Y36 VDDQ
F32 VDD_ILDO_NAV
AE29 VDD_QFPROM
AF12 VDD_USB_HS_DVDD

33 32 31 9 8 6 5 4 PP_1V8_LDO6
33 31 9 6 4 PP_0V875_LDO4

PART_NUMBER=337S00865 ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
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PWR
CRITICAL

L29 VDDA_DDRSS
N29 VDDA_DDRSS
R29 VDDA_DDRSS
U29 VDDA_DDRSS
V30 VDDA_DDRSS_CC
P32 VDDA_DDRSS_HV
W31 VDDA_DDRSS_PLL_HV
AF10 VDDA_PCIE_0P9
AG11 VDDA_PCIE_0P9
AF8 VDDA_PCIE_1P2
G9 VDDA_QREF_0P9
AC7 VDDA_QREF_0P9
AE7 VDDA_QREF_1P8
AE13 VDDA_USB_HS_1P8
AG13 VDDA_USB_HS_3P3
AF14 VDDA_USB_SS_0P9
AE15 VDDA_USB_SS_1P2
G19 VDDA_QLINK0_HV
F20 VDDA_QLINK0_LV
G17 VDDA_QLINK0_LV
F18 VDDA_QLINK0_LV_CK
G13 VDDA_QLINK1_HV
G11 VDDA_QLINK1_LV
G15 VDDA_QLINK1_LV
F12 VDDA_QLINK1_LV_CK
F14 VDDA_QLINK1_LV_CK
J31 VDDIO_DDRSS
L31 VDDIO_DDRSS
N31 VDDIO_DDRSS
U31 VDDIO_DDRSS
R31 VDDIO_DDRSS_CK

PP_0V75_SMPS7
C749_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
C768_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND
C769_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND
PP_1V2_LDO1
PP_0V875_LDO4
PP_0V875_LDO4
PP_1V2_LDO1
PP_1V8_LDO5
C742_E C744_E C745_E 2.2UF C752_E 2.2UF C758_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
PP_1V8_LDO5
PP_3V1_LDO10
PP_0V875_LDO4
PP_1V2_LDO1
PP_1V2_LDO1
C759_E C755_E C766_E 0.22UF C746_E 2.2UF C750_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
PP_0V875_LDO4
C747_E 2.2UF C751_E 0.22UF C756_E 0.22UF C760_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND
PP_0V6_LDO14
C743_E C748_E 2.2UF C770_E C771_E C772_E 0.22UF C773_E 2.2UF C774_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

VDD_CX
31 6 3 PP_0V75_SMPS5
C701_E 2.2UF C704_E 2.2UF 132S00014 C706_E 0.22UF C709_E 0.22UF C712_E 0.22UF C715_E 0.22UF C754_E 0.22UF C757_E 0.22UF C775_E 0.22UF 132S00014 C776_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

VDD_MX
31 6 4 3 PP_0V75_SMPS7
C702_E 4UF 132S00014 C705_E 0.22UF 132S00014 C707_E 0.22UF 132S00014 C710_E 0.22UF C713_E 0.22UF C716_E 0.22UF C718_E 0.22UF C779_E 0.22UF C781_E 0.22UF C783_E 0.22UF 10% 6.3V CER-X5R 01005 ROOM=BASEBAND

VDD_MODEM
31 6 3 PP_0V75_SMPS1_6
138S00071 C777_E 4UF 138S00071 C787_E 4UF 138S00071 C788_E 4UF 20% 6.3V CER-X5R 0201 ROOM=BASEBAND
C708_E C711_E 0.47UF C714_E 0.47UF C717_E 0.47UF C778_E 0.47UF C780_E 0.47UF C782_E 0.47UF C784_E 0.47UF C785_E 0.47UF C786_E 0.47UF 20% 6.3V X5R 01005-1 138S00133 ROOM=BASEBAND

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PAGE TITLE
BB: POWER

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BRANCH 1
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BB: GND

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 7 OF 8

GND

CRITICAL

A1	GND	GND	AF24
A11	GND	GND	AF26
A15	GND	GND	AF28
A19	GND	GND	AG15
A23	GND	GND	AG5
A27	GND	GND	AG7
A3	GND	GND	AH10
A31	GND	GND	AH14
A35	GND	GND	AH18
A37	GND	GND	AH20
A7	GND	GND	AH8
AA11	GND	GND	AJ1
AA13	GND	GND	AJ17
AA15	GND	GND	AJ37
AA17	GND	GND	AK10
AA21	GND	GND	AK14
AA23	GND	GND	AK2
AA25	GND	GND	AK32
AA31	GND	GND	AK36
AA5	GND	GND	AK4
AA9	GND	GND	AK8
AB18	GND	GND	C3
AB20	GND	GND	C35
AB26	GND	GND	D10
AB28	GND	GND	D14
AB30	GND	GND	D18
AB36	GND	GND	D22
AB4	GND	GND	D26
AB6	GND	GND	D30
AD10	GND	GND	D34
AD12	GND	GND	D4
AD14	GND	GND	D6
AD16	GND	GND	E11
AD28	GND	GND	E13
AD30	GND	GND	E15
AD36	GND	GND	E17
AD8	GND	GND	E19
AE1	GND	GND	E21
AE11	GND	GND	E23
AE17	GND	GND	E25
AE19	GND	GND	E27
AE21	GND	GND	E29
AE23	GND	GND	E31
AE27	GND	GND	E33
AE5	GND	GND	E35
AE9	GND	GND	E37
AF16	GND	GND	E7
AF18	GND	GND	E9
AF20	GND	GND	F10
AF22	GND	GND	F16

PART_NUMBER=337S00865
ROOM=BASEBAND

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SDX-55M-0-PSP547-02-1
PSP
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GND

CRITICAL

F22	GND	GND	N23
F24	GND	GND	N25
F26	GND	GND	N27
F28	GND	GND	N33
F30	GND	GND	N35
F34	GND	GND	N9
F8	GND	GND	P10
G29	GND	GND	P12
G31	GND	GND	P14
G33	GND	GND	P16
G35	GND	GND	P18
H30	GND	GND	P20
H32	GND	GND	P22
H34	GND	GND	P24
J13	GND	GND	P26
J15	GND	GND	P30
J17	GND	GND	R33
J19	GND	GND	R35
J21	GND	GND	T30
J23	GND	GND	T32
J25	GND	GND	T34
J27	GND	GND	U1
J29	GND	GND	U11
J33	GND	GND	U13
J35	GND	GND	U15
J37	GND	GND	U17
K10	GND	GND	U19
K12	GND	GND	U25
K14	GND	GND	U27
K20	GND	GND	U33
K22	GND	GND	U35
K24	GND	GND	U9
K26	GND	GND	V10
K28	GND	GND	V12
K30	GND	GND	V14
K32	GND	GND	V16
K34	GND	GND	V18
K8	GND	GND	V20
L1	GND	GND	V22
L33	GND	GND	V24
L35	GND	GND	V26
M30	GND	GND	V28
M32	GND	GND	V32
M34	GND	GND	V34
N11	GND	GND	V8
N13	GND	GND	W33
N15	GND	GND	W35
N17	GND	GND	W37
N19	GND	GND	Y30
N21	GND		

SYNC_DATE=08/01/2019

PAGE TITLE
BB: GND

DRAWING NUMBER 051-05263
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BB:IO,MEM,SERDES,EEPROM

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 2 OF 8
QLINK
CRITICAL

31 11	85_SUB6_QLINK_L0_P	C29	QLINK0_L0_P	C11	85_MMW_QLINK_L0_P 31 33
31 11	85_SUB6_QLINK_L0_N	B28	QLINK0_L0_M	D12	85_MMW_QLINK_L0_N 31 33
11	85_SUB6_QLINK_L1_P	D32	QLINK0_L1_P	B14	85_MMW_QLINK_L1_P 33
11	85_SUB6_QLINK_L1_N	C31	QLINK0_L1_M	A13	85_MMW_QLINK_L1_N 33
11	85_SUB6_QLINK_L2_P	C33	QLINK0_L2_P	B18	85_MMW_QLINK_L2_P 33
11	85_SUB6_QLINK_L2_N	B32	QLINK0_L2_M	A17	85_MMW_QLINK_L2_N 33
11	85_SUB6_QLINK_L3_P	D24	QLINK0_L3_P	B8	85_MMW_QLINK_L3_P 33
11	85_SUB6_QLINK_L3_N	C23	QLINK0_L3_M	C9	85_MMW_QLINK_L3_N 33
11	85_SUB6_QLINK_L4_P	D28	QLINK0_L4_P	B6	85_MMW_QLINK_L4_P 33
11	85_SUB6_QLINK_L4_N	C27	QLINK0_L4_M	A5	85_MMW_QLINK_L4_N 33
11	85_SUB6_QLINK_L5_P	C25	QLINK0_L5_P	C17	85_MMW_QLINK_L5_P 33
11	85_SUB6_QLINK_L5_N	B24	QLINK0_L5_M	B16	85_MMW_QLINK_L5_N 33
11	85_SUB6_QLINK_L6_P	B26	QLINK0_L6_P	B20	85_MMW_QLINK_L6_P 33
11	85_SUB6_QLINK_L6_N	A25	QLINK0_L6_M	C21	85_MMW_QLINK_L6_N 33
11	85_SUB6_QLINK_L7_P	B34	QLINK0_L7_P	B12	85_MMW_QLINK_L7_P 33
11	85_SUB6_QLINK_L7_N	A33	QLINK0_L7_M	C13	85_MMW_QLINK_L7_N 33
11	85_SUB6_QLINK_CLK_P	A29	QLINK0_CLK_P	B10	85_MMW_QLINK_L8_P 33
11	85_SUB6_QLINK_CLK_N	B30	QLINK0_CLK_M	A9	85_MMW_QLINK_L8_N 33
			QLINK1_L9_P	D8	85_MMW_QLINK_L9_P 33
			QLINK1_L9_M	C7	85_MMW_QLINK_L9_N 33
			QLINK1_L10_P	B22	85_MMW_QLINK_L10_P 33
			QLINK1_L10_M	A21	85_MMW_QLINK_L10_N 33
			QLINK1_L11_P	C19	85_MMW_QLINK_L11_P 33
			QLINK1_L11_M	D20	85_MMW_QLINK_L11_N 33
			QLINK1_L12_P	B4	85_MMW_QLINK_L12_P 33
			QLINK1_L12_M	C5	85_MMW_QLINK_L12_N 33
			QLINK1_CLK_P	C15	85_MMW_QLINK_CLK_P 33
			QLINK1_CLK_M	D16	85_MMW_QLINK_CLK_N 33

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
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CONTROL
CRITICAL

31 5	SHIELD_SLEEP_CLK_32K	W3	SLEEP_CLK	P36	EBI_ZQ
	SHIELD_CXO_REXT	AJ3	QREFS_CXO_REXT	N37	EBI_CA_CAL
31 5	SHIELD_MDM_19P2M_CLK	AD6	CXO		
31	BB_JTAG_RST_L	P6	SRST*	T2	RESOUT*
31 5	PMIC_RESOUT_L	AC5	RESIN*	T4	PS_HOLD
NC		N3	MODE_0	AG19	DNC
NC		M4	MODE_1	M6	DNC
31 8	BB_JTAG_TCK_SWD_CLK_1V8_R	N1	TCK	N5	DNC
31	BB_JTAG_TRST_L	P2	TRST*	P34	DNC
31 8	BB_JTAG_TMS_SWD_IO_1V8_R	R3	TMS	AK20	REFGEN_REXT
31	BB_JTAG_TDI	R5	TDI	AF2	PMIC_SPMI_CLK
31	BB_JTAG_TDO	P4	TDO	AE3	PMIC_SPMI_DATA

SHIELD_BB_BDM_ZQ
SHIELD_BB_EBI1_CAL
PS_HOLD
SHIELD_PCIE_CAL_RES
BB_BBPMU_SPMI_CLK 5 31
BB_BBPMU_SPMI_DATA 5 31

R904_E 3.0K 1% 1/32W MF 01005 ROOM=BASEBAND
R902_E 240 1% 1/32W MF 01005 ROOM=BASEBAND
R903_E 240 1% 1/32W MF 01005 ROOM=BASEBAND
PP_0V6_LDO14 4 6 31
R901_E 100 1% 1/32W MF 01005 ROOM=BASEBAND
131S00353 C904_E 10PF 5% 16V NP0/C0G 01005 BASEBAND
131S00353 C905_E 10PF 5% 16V NP0/C0G 01005 BASEBAND

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 3 OF 8
GPIO
CRITICAL

28 1	IO_BB_BI_SIM2_DATA	AA3	GPIO_0	H2	NC
28 8 1	IO_BB_FROM_SIM2_DETECT	AA1	GPIO_1	H4	NC
1	IO_BB_TO_SIM2_RESET	AB2	GPIO_2	AK28	NC
1	IO_BB_TO_SIM2_CLK	Y2	GPIO_3	Y32	NC
NC		T6	GPIO_4	AJ23	UART_BB_TO_WLAN_TX 1 31
NC		U3	GPIO_5	AK24	UART_BB_TO_WLAN_RX 1 31
NC		V4	GPIO_6	AC33	NC
NC		U5	GPIO_7	AA35	GPIO_AP_FROM_BB_RESET_DETECT_L 1 31
31 1	UART1_AOP_FROM_BB_RXD	AK26	GPIO_8_BB_TX	AJ35	GPIO_AP_TO_BB_COREDUMP 1 31
31 1	UART1_AOP_TO_BB_TXD	AJ25	GPIO_9_BB_RX	AH36	NC
31 8	BB_EEPROM_I2C_SDA	AH26	GPIO_10	AG35	NC
31 8	BB_EEPROM_I2C_SCL	AG25	GPIO_11	AF36	NC
31 1	I2S2_AP_FROM_BB_LRCLK	AF30	GPIO_12	AC31	NC
31 1	I2S2_AP_TO_BB_DOUT	AF32	GPIO_13	AE33	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L 1 31 32
31 1	I2S2_AP_FROM_BB_DIN	AG31	GPIO_14	AE35	NC
31 1	I2S2_AP_FROM_BB_BCLK	AH30	GPIO_15	AD34	NC
NC		AK30	GPIO_16	AF34	PCIE_GP2_AP_BI_BB_CLKREQ_L 1 31 32
NC		AG33	GPIO_17	AE31	PCIE_GP2_AP_TO_BB_PERST_L 1 31
NC		AH32	GPIO_18	AB34	BOOT_CFG1 31 32
NC		AJ31	GPIO_19	AC35	NC
31 1	GPIO_R1_TO_BB_CH9_COEX	AJ27	GPIO_20	AB37	NC
31	GPIO_R1_TO_BB_LAA_SW_CTRL	AG27	GPIO_21	AD32	GPIO_AP_TO_BB_PEAK_PWR_IND 1 31
NC		AJ29	GPIO_22	AG29	NC
NC		AD28	GPIO_23	K6	NC
32 31	BOOT_CFG2	AA33	GPIO_24	L3	NC
NC		Y34	GPIO_25	L5	NC
NC		K2	GPIO_26	M4	NC
NC		K4	GPIO_27	AD2	IO_BB_BI_SIM1_DATA 1 26 31
31 11	BB_TO_SDR_WMSS_RESET_L	E1	GPIO_28	AC1	IO_BB_FROM_SIM1_DETECT 1 8 28 31
33 31 12	SHIELD_RFFE4_SCLK_BB	G3	GPIO_29	AD4	IO_BB_TO_SIM1_RESET 1 31
33 31 12	SHIELD_RFFE4_SDATA_BB	F4	GPIO_30	AC3	IO_BB_TO_SIM1_CLK 1 31
NC		AA23	GPIO_31	AH34	NC
31 1	GPIO_AP_TO_BB_TIME_MARK	AH24	GPIO_32	E3	NC
31 1	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	G1	GPIO_33	D2	QLINK_REQ_SMR_TO_BB 31 33
31 11	QLINK_EN_BB_TO_SDR	F2	GPIO_34	B2	BB_TO_SMR_WMSS_RESET_L 31 33
	QLINK_REQ_SDR_TO_BB	E5	GPIO_35	AH22	GPIO_BB_TO_R1_COEX 1 31
31 30	SHIELD_RFFE0_SDATA_BB	J5	GPIO_36	AG21	GPIO_BB_TO_R1_CH9_REQ 1 31
31 30	SHIELD_RFFE0_SCLK_BB	J3	GPIO_37	F6	NC
31 29	SHIELD_RFFE1_SDATA_BB	G5	GPIO_38	AF4	NC
31 29	SHIELD_RFFE1_SCLK_BB	H6	GPIO_39	AG1	NC

BB_TO_DOTARA_COEX_1V2:NOT USED

C906_E 33PF 5% 16V NP0-C0G 01005-1 ROOM=BASEBAND
NOSTUFF
131S00292

NOTE:
ENSURE THAT THERE ARE NO UNINTENTIONAL EXTERNAL PULL-UPS ON THE FOLLOWING GPIOS AND THESE GPIOS ARE NOT LOGIC HIGH UNINTENTIONALLY BEFORE SDX55M COMES OUT OF RESET

(I.E. BEFORE SDX_RESOUT_N DE-ASSERTS TO LOGIC HIGH): GPIO_24, 54, 58, 59, AND 75.
SEE BOOT CONFIGURATION GPIOS PAGE OF SDX55M DESIGN GUIDELINES (80-PK565-5BM) FOR DETAILS.

NOTE: TYPO IN SPEC

AP_TO_BB_DEV_WAKE : NOT USED
WAKE O/P WHEN BB IS END POINT

BB EEPROM

33 32 31 9 8 6 5 4 PP_1V8_LDO6

R908_E 10K 5% 1/32W MF 01005 ROOM=BASEBAND
C901_E 1.0UF 20% 10V X5R-CERM 0201-1 ROOM=BASEBAND
R909_E 10K 5% 1/32W MF 01005 ROOM=BASEBAND

EEPROM_E
CAT24C08C4A
WLCSP
ROOM=BASEBAND
CRITICAL

A1 VCC
B1 SCL
SDA B2
A2 VSS

31 8 BB_EEPROM_I2C_SCL
BB_EEPROM_I2C_SDA 8 31

DUAL-VOLTAGE IO PADS
VDD_PX71: GPIO8,9,12-23
VDD_PX72: GPIO46-57,59-61,71
VDD_PX73: GPIO31-32,44-45, 75-76
VDD_PX74: GPIO78-79

DUAL PSIM: SHORT SIM1_DET WITH SIM2_DET
PSIM AND ESIM: SIM2_DET STUFF PU

33 32 31 9 8 6 5 4 PP_1V8_LDO6

R905_E 100K 5% 1/32W MF 01005 ROOM=BASEBAND
R907_E 100K 5% 1/32W MF 01005 ROOM=BASEBAND
31 28 8 1 IO_BB_FROM_SIM1_DETECT
28 8 1 IO_BB_FROM_SIM2_DETECT
NOSTUFF
R906_E 100K 5% 1/32W MF 01005 ROOM=BASEBAND

PART_NUMBER=337S00865
ROOM=BASEBAND

U_BB_E
SDX-55M-0-PSP547-02-1
PSP
SYM 4 OF 8
USB_PCIE
CRITICAL

			PCIE_REFCLK_P	AJ9	90_PCIE_GP2_AP_TO_BB_REFCLK_P 1 31
			PCIE_REFCLK_M	AG9	90_PCIE_GP2_AP_TO_BB_REFCLK_N 1 31
32 31	90_USB_BB_P	AJ15	USB_HS_DP		
32 31	90_USB_BB_N	AK16	USB_HS_DM		
			PCIE_TX0_P	AJ13	90_PCIE_BB_TO_AP_RX_SDX_P
			PCIE_TX0_M	AH12	90_PCIE_BB_TO_AP_RX_SDX_N
NC		AG17	USB_SS_TX_P		PCIE_TX1_P AJ11 NC
NC		AJ16	USB_SS_TX_M		PCIE_TX1_M AK11 NC
NC		AK18	USB_SS_RX_P	AJ5	90_PCIE_GP2_AP_TO_BB_TX_P 1 31
NC		AJ19	USB_SS_RX_M	AK6	90_PCIE_GP2_AP_TO_BB_TX_N 1 31
			PCIE_RX1_P	AH6	NC
			PCIE_RX1_M	AJ7	NC

132S00014 ROOM=BASEBAND
C903_E 0.22UF 10% 6.3V CER-X5R 01005
90_PCIE_GP2_AP_FROM_BB_RX_P 1 31
C902_E 0.22UF 10% 6.3V CER-X5R 01005
90_PCIE_GP2_AP_FROM_BB_RX_N 1 31
ROOM=BASEBAND
132S00014

PP1V2_S2
C907_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=BASEBAND
R910_E 10K 5% 1/32W MF 01005 ROOM=BASEBAND
R911_E 10K 5% 1/32W MF 01005 ROOM=BASEBAND NOSTUFF
SWD_E NVT0202JK X2SON CRITICAL
VCCA VCCB ROOM=BASEBAND
GND
SWD_OE 6 OE
SWD_AP_TO_MANY_SWCLK 5 A1
BB_JTAG_TMS_SWD_IO_R 4 A2
B1 8 BB_JTAG_TCK_SWD_CLK_1V8
B2 1 BB_JTAG_TMS_SWD_IO_1V8
C908_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=BASEBAND
PP_1V8_LDO6 4 5 6 8 9 31 32 33

XW912_E SHORT-01005-SP 998-23033 BASEBAND
31 1 SWD_AP_BI_BB_SWDIO
XW914_E SHORT-01005-SP 998-23033 BASEBAND
BB_JTAG_TCK_SWD_CLK_1V8_R 8 31
XW913_E SHORT-01005-SP 998-23033 BASEBAND
BB_JTAG_TMS_SWD_IO_1V8_R 8 31

SYNC_DATE=08/01/2019

PAGE TITLE
BB: GPIOS & QLINK

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TRANSCEIVER: PDN

NOTE: 4UF BULK COULD BE FURTHER AWAY AND MAKE SURE THE STAR ROUTING IS FROM 4UF.
NOTE: 1UF SHOULD BE AS CLOSE AS POSSIBLE TO CORRESPONDING PIN ON SDR

PP_1V2_LDO1 → C1135_E 4UF, C1136_E 4UF (ROOM=SUB6_XCVR) — STAR ROUTE

U_SDR_E SDR865-0 PSP SYM 6 OF 8 CRITICAL
PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

A24	VDDAM_TP0	VDDAH_TP0	B25
AG26	VDDAM_TP1	VDDAH_TP1	AF25
B29	VDDAM_TX0	VDDAH_TX0	A30
AF29	VDDAM_TX1	VDDAH_TX1	AF31
AF23	VDDAM_TX2	VDDAH_TX2	AG22
E2	VDDAM_RP0	VDDAH_RP0	C2
F1	VDDAM_RP1	VDDAH_RP1	G2
P1	VDDAM_RP2	VDDAH_RP2	M1
V1	VDDAM_RP3	VDDAH_RP3	Y1
AB1	VDDAM_RP4	VDDAH_RP4	AG4
AF15	VDDAM_RP5	VDDAH_RP5_2	AF13
A16	VDDAM_RX0	VDDAH_RX0	A18
AG10	VDDAM_RX5		
D21	VDDAM_BBRX_TOP	VDDAH_TXDAC0	J32
AA22	VDDAM_BBRX_BOT	VDDAH_TXDAC1	W30
V35	VDD_CX	VDDAH_LVDS	T21
W36	VDD_CX		
L36	VDD_CX		
J34	VDD_MX0		
V33	VDD_MX1		
L34	VDD_PHY		
K35	VDD_PX		
K33	VDD_PXM		

PP_1V7_LDO16 → C1140_E 4UF, C1141_E 4UF (ROOM=SUB6_XCVR) — STAR ROUTE

CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN. FOR REFERENCE ONLY - NOT A CHANGE REQUEST

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BRANCH	1
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TRANSCEIVER: PDN

NOTE: 4UF BULK COULD BE FURTHER AWAY AND MAKE SURE THE STAR ROUTING IS FROM 4UF.
NOTE: 1UF SHOULD BE AS CLOSE AS POSSIBLE TO CORRESPONDING PIN ON SDR

PP_0V8_LDO3 (4 10 31)

C1226_E 4UF 20% 6.3V CER-X5R 0805 ROOM=SUB6_XCVR
C1227_E 4UF 20% 6.3V CER-X5R 0805 ROOM=SUB6_XCVR

XW1202_E XW1203_E XW1204_E XW1205_E XW1206_E XW1207_E XW1208_E XW1209_E XW1210_E XW1211_E XW1212_E XW1213_E XW1214_E XW1215_E XW1216_E XW1217_E XW1218_E XW1201_E XW1237_E XW1238_E XW1239_E XW1240_E
SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR

PP_LDO3_SDR_VDDAL_RP0 57
PP_LDO3_SDR_VDDAL_RP1 57
PP_LDO3_SDR_VDDAL_RP2 57
PP_LDO3_SDR_VDDAL_RP3 57
PP_LDO3_SDR_VDDAL_RP4 57
PP_LDO3_SDR_VDDAL_RP5 57
PP_LDO3_SDR_VDDAL_RX0 67
PP_LDO3_SDR_VDDAL_RX1 22
PP_LDO3_SDR_VDDAL_RX2 22
PP_LDO3_SDR_VDDAL_RX3 22
PP_LDO3_SDR_VDDAL_RX4 22
PP_LDO3_SDR_VDDAL_RX5 22
PP_LDO3_SDR_VDDAL_RX6 90
PP_LDO3_SDR_VDDAL_RXLO0 27
PP_LDO3_SDR_VDDAL_RXLO4 27
PP_LDO3_SDR_VDDAL_RXLO5 27
PP_LDO3_SDR_VDDAL_RXLO7 27
PP_LDO3_SDR_VDDAL_TP0 30
PP_LDO3_SDR_VDDAL_TP1 30
PP_LDO3_SDR_VDDAL_TX0 20
PP_LDO3_SDR_VDDAL_TX1 20
PP_LDO3_SDR_VDDAL_TX2 20

C1217_E C1215_E C1212_E C1209_E C1205_E C1201_E C1202_E C1233_E C1206_E C1234_E C1235_E C1210_E C1213_E C1203_E C1236_E C1237_E C1207_E C1204_E C1208_E C1216_E C1214_E C1211_E
0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

PART_NUMBER=338S00647
SHIELD=TTS
ROOM=SUB6_XCVR

U_SDR_E
SDR865-0
PSP
SYM 5 OF 8
CRITICAL

D1	VDDAL_RP0	VDDAL_DIG_RP0	A4
F3	VDDAL_RP1	VDDAL_DIG_RP1	K1
N2	VDDAL_RP2	VDDAL_DIG_RP2	L2
W2	VDDAL_RP3	VDDAL_DIG_RP3	AA2
AC2	VDDAL_RP4	VDDAL_DIG_RP4	AE2
AG16	VDDAL_RP5	VDDAL_DIG_RP5	AG14
B13	VDDAL_RX0	VDDAL_DIG_TP0	G24
C6	VDDAL_RX1	VDDAL_DIG_TP1	AA24
J6	VDDAL_RX2	VDDAL_DIG1	B21
L6	VDDAL_RX3	VDDAL_DIG2	Y23
W6	VDDAL_RX4	VDDAL_FBRX	H21
AC6	VDDAL_RX5	VDDAL_GNSS	B17
AG12	VDDAL_RX6	VDDAL_ICON6	A20
E12	VDDAL_RXLO0	VDDAL_ICON32	T19
N12	VDDAL_RXLO4	VDDAL_XO	T1
R12	VDDAL_RXLO5		
W12	VDDAL_RXLO7		
A26	VDDAL_TP0		
AF27	VDDAL_TP1		
A28	VDDAL_TX0		
AG30	VDDAL_TX1		
AE22	VDDAL_TX2		

PP_LDO3_SDR_VDDAL_DIG_RP0 6
PP_LDO3_SDR_VDDAL_DIG_RP1 6
PP_LDO3_SDR_VDDAL_DIG_RP2 6
PP_LDO3_SDR_VDDAL_DIG_RP3 6
PP_LDO3_SDR_VDDAL_DIG_RP4 6
PP_LDO3_SDR_VDDAL_DIG_RP5 6
PP_LDO3_SDR_VDDAL_DIG_TP0 10
PP_LDO3_SDR_VDDAL_DIG_TP1 10
PP_LDO3_SDR_VDDAL_DIG1 171
PP_LDO3_SDR_VDDAL_DIG2 124
PP_LDO3_SDR_VDDAL_FBRX 20
PP_LDO3_SDR_VDDAL_GNSS 40
PP_LDO3_SDR_VDDAL_ICON6 5
PP_LDO3_SDR_VDDAL_ICON32 25
PP_LDO3_SDR_VDDAL_XO 18

C1218_E C1219_E C1220_E C1222_E C1223_E C1225_E C1221_E C1224_E C1231_E C1232_E C1238_E C1230_E C1239_E C1229_E C1228_E
0.1UF 20% 6.3V X5R-CERM 0100S ROOM=SUB6_XCVR

XW1223_E XW1224_E XW1225_E XW1226_E XW1227_E XW1228_E XW1229_E XW1232_E XW1230_E XW1231_E XW1287_E XW1233_E XW1291_E XW1235_E XW1236_E
SHORT-8L-0.1MM-SM ROOM=SUB6_XCVR
XW1230_E XW1231_E: SHORT-8L-0.25MM-SM
XW1235_E: ROOM=SUB6_XCVR
XW1236_E: PATH=I106

PP_0V8_LDO3 (4 10 31)

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XCVR POWER_2

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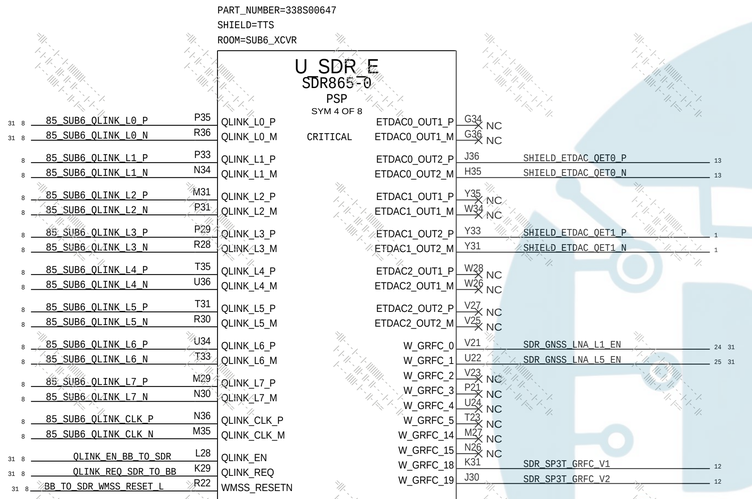
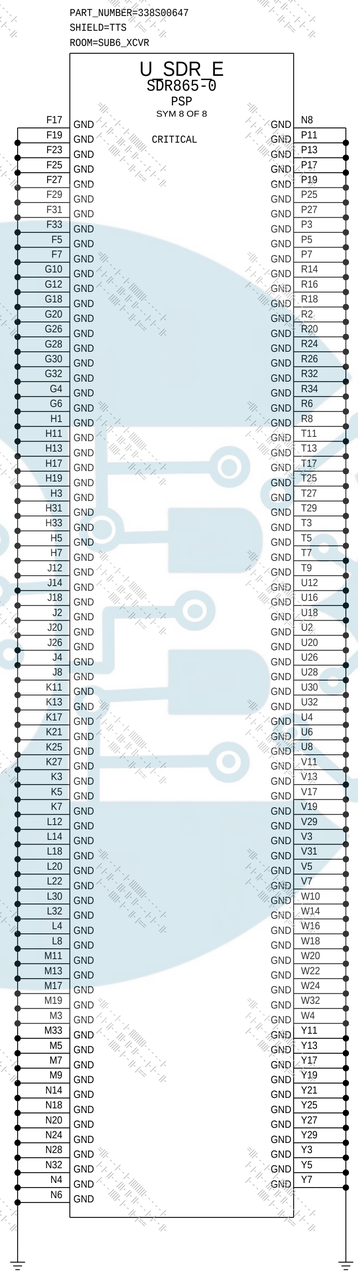
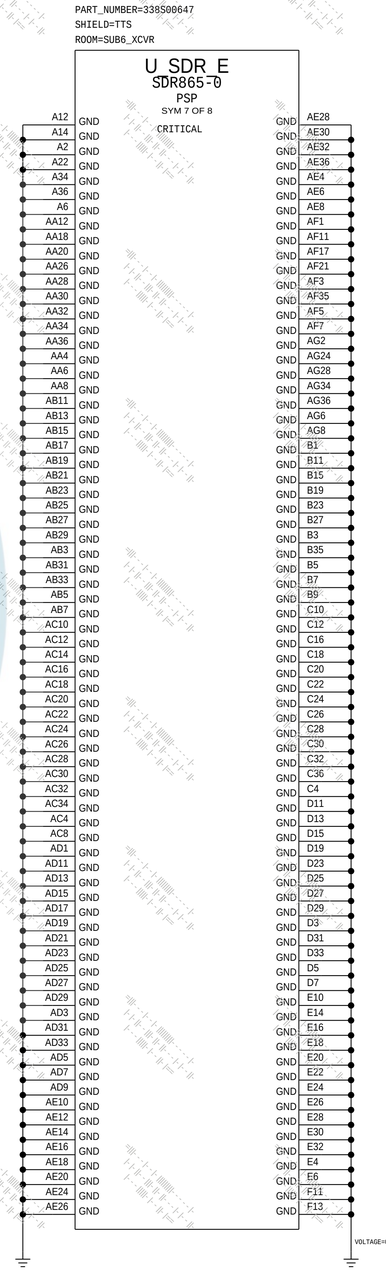
TRANSCEIVER: DIGITAL & GND







SYNC_DATE=08/01/2019

PAGE TITLE

XCVR DIGITAL & GND

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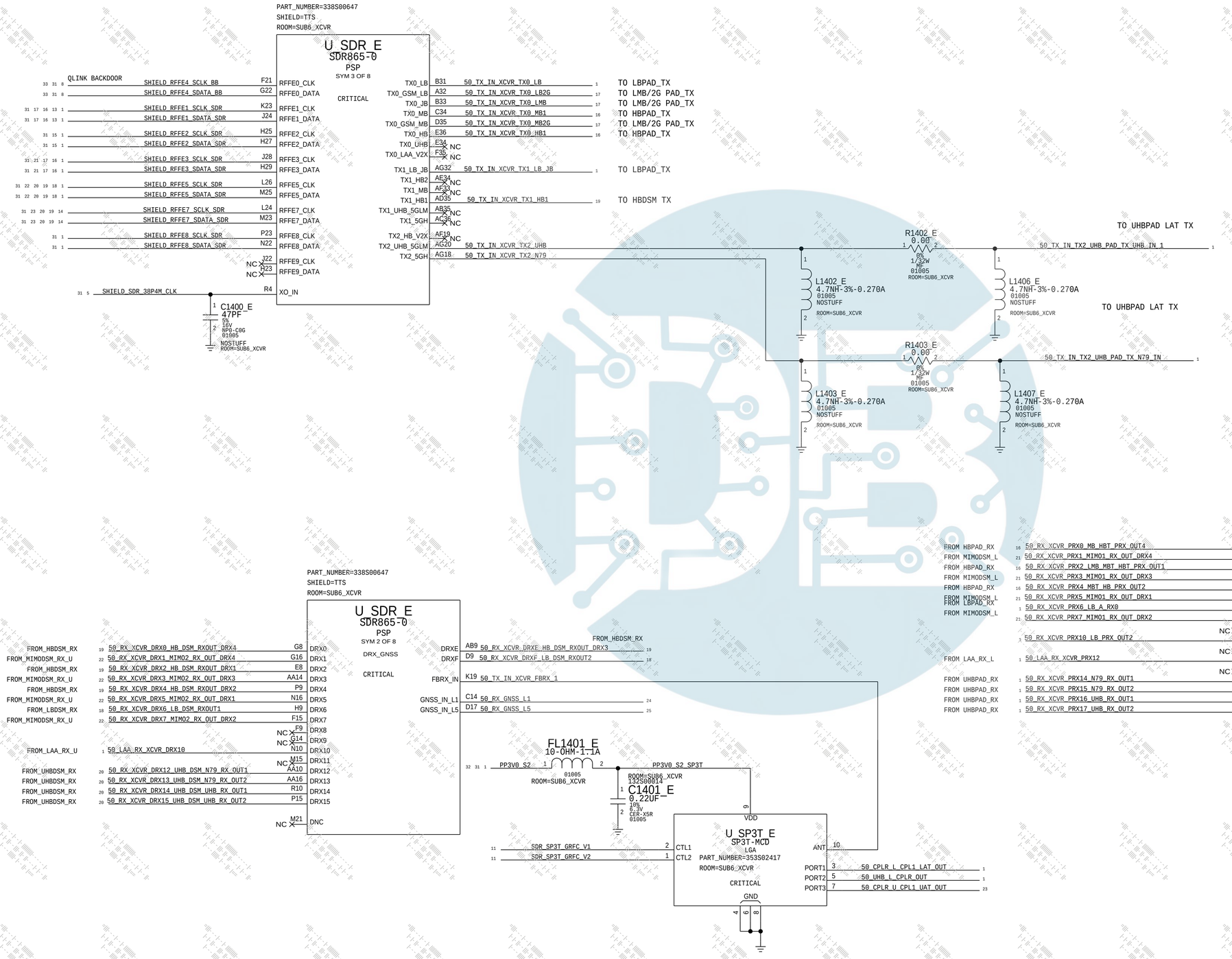
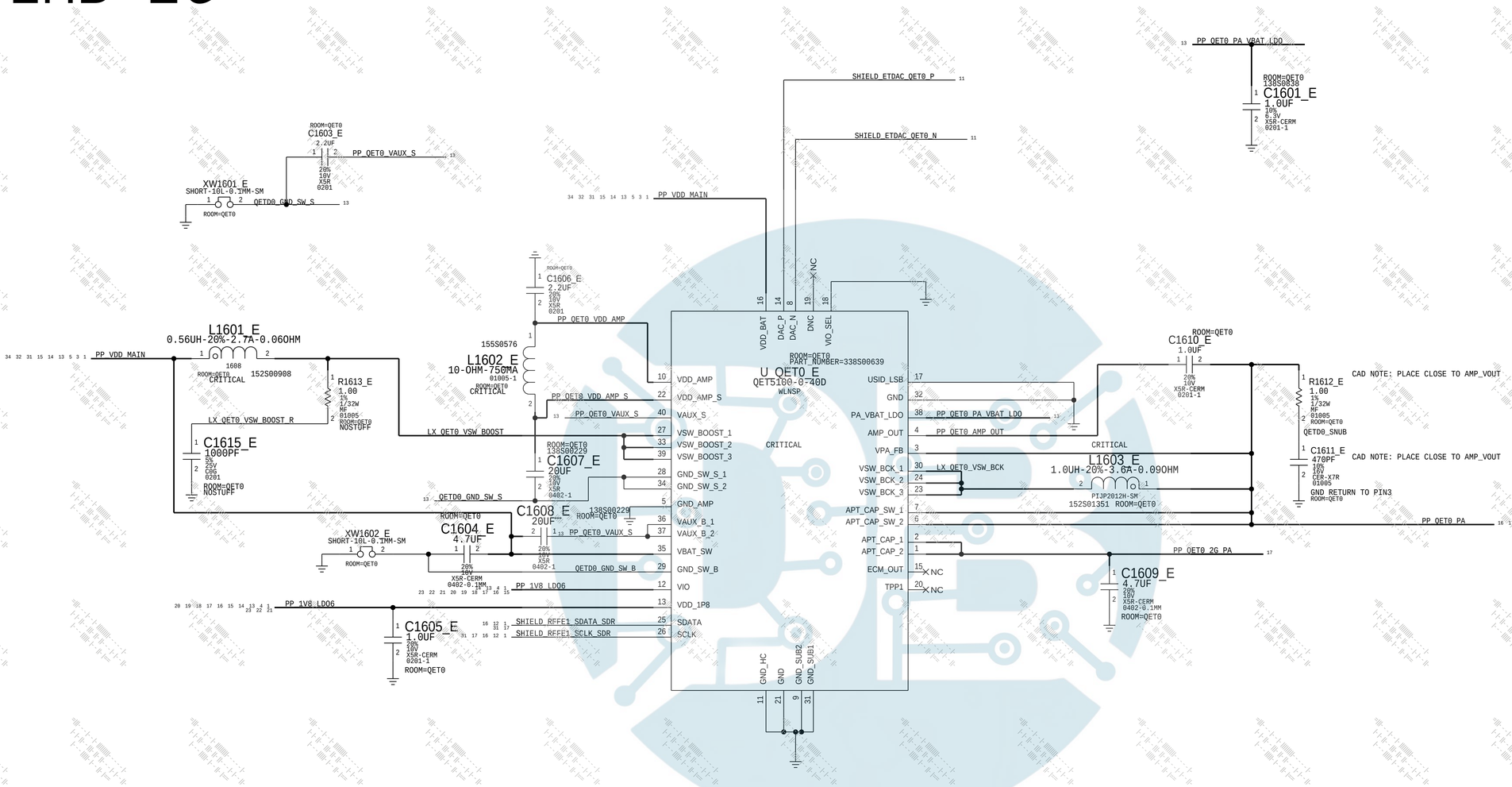
TRANSCEIVER: TX & RX



DISCRETE QET5100 0
HB/LMB-2G



USID = 0X4 WHEN USID PIN IS GND
USID = 0X5 WHEN USID PIN IS HIGH

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PAGE TITLE	QET_DISCRETE_0
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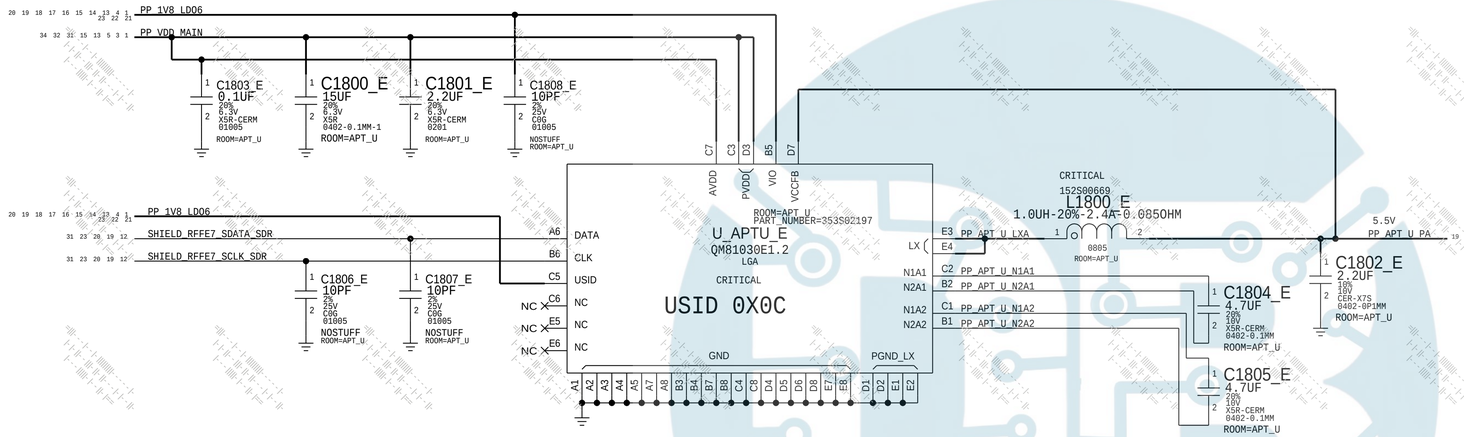
APT DCDC 2



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PAGE TITLE

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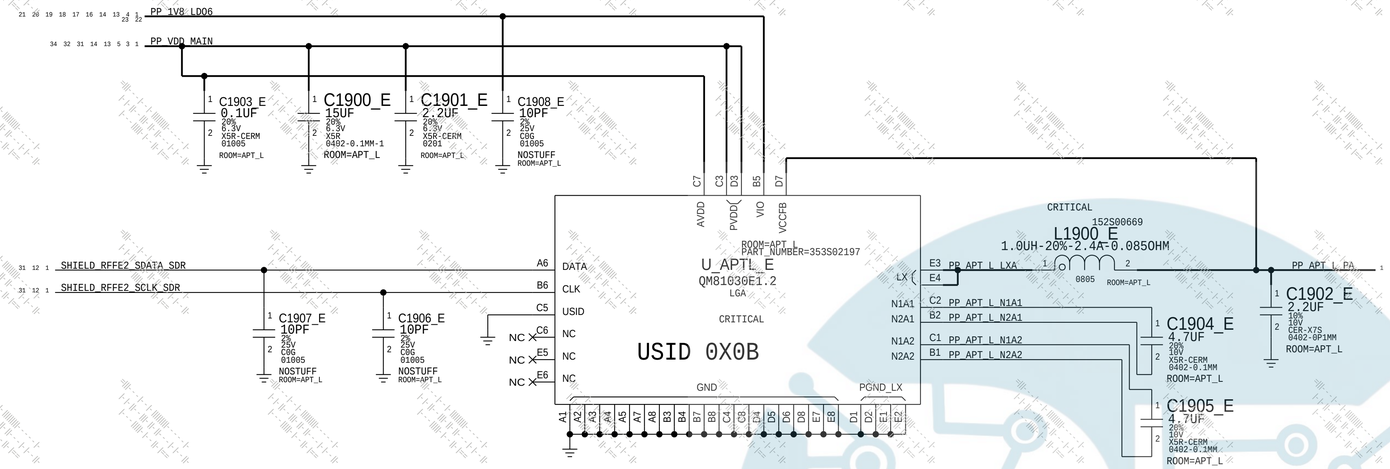
APT DCDC 1



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PAGE TITLE

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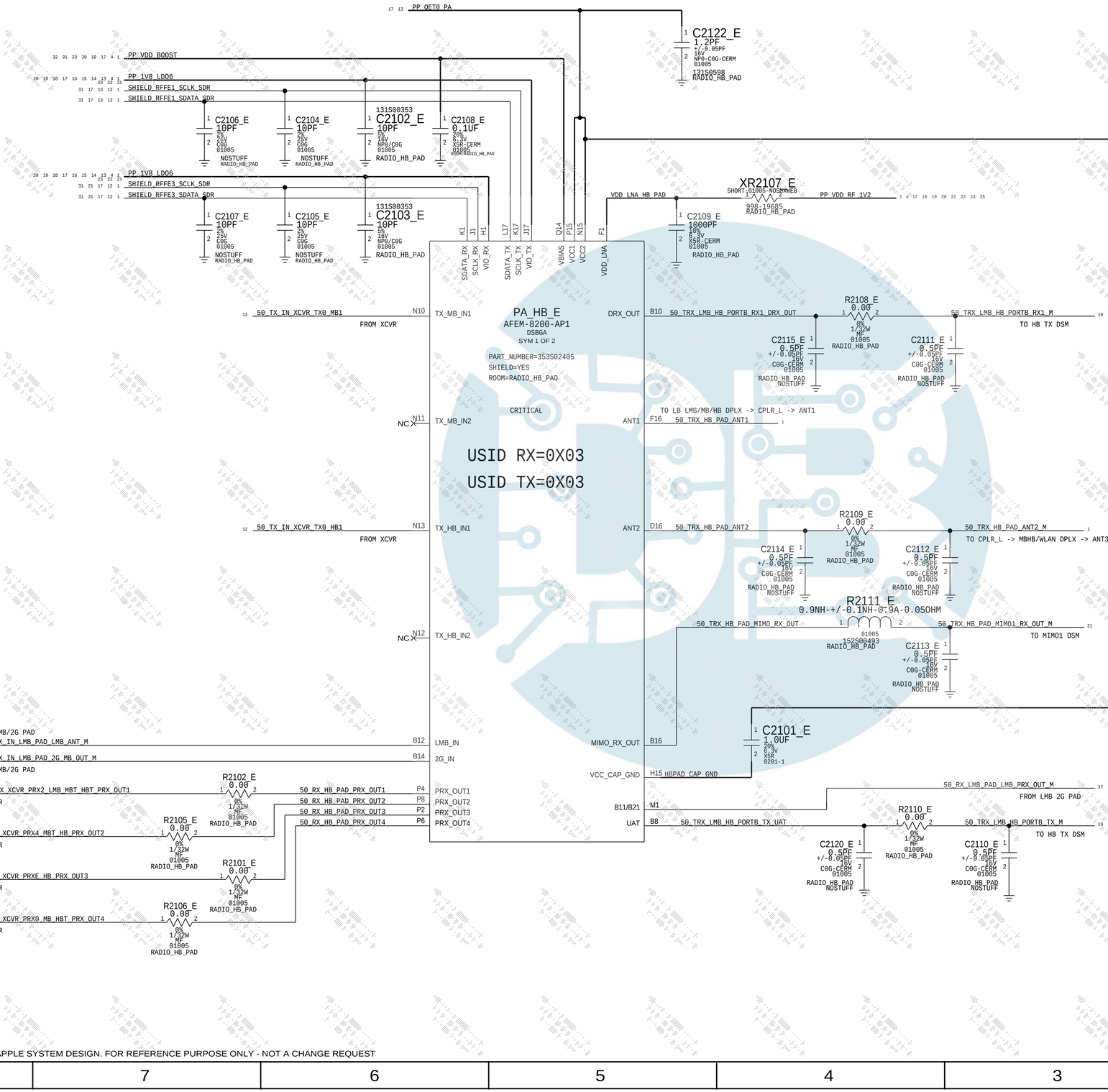
HB PAD



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PAGE TITLE

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BRANCH 1

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LMB_2G_PAD

PP_QET0_2G_PA
C2305_E 100PF 5% 16V NP0-C0G 01005-1 LMB_2GPAD (131S00303)
C2304_E 2.2UF 20% 10V X5R 0201 LMB_2GPAD
PP_VDD_BOOST
C2306_E 1.0UF 20% 10V X5R-CERM 0201-1 LMB_2GPAD

PP_1V8_LDO6
SHIELD_RFFE1_SCLK_SDR
SHIELD_RFFE1_SDATA_SDR
C2311_E 18PF 5% 16V NP0/C0G 01005 LMB_2GPAD
C2313_E 18PF 5% 16V NP0/C0G 01005 NOSTUFF LMB_2GPAD
C2302_E 10PF 5% 25V C0G 01005 NOSTUFF LMB_2GPAD

PP_1V8_LDO6
SHIELD_RFFE3_SCLK_SDR
SHIELD_RFFE3_SDATA_SDR
C2312_E 18PF 5% 16V NP0/C0G 01005 LMB_2GPAD
C2301_E 18PF 5% 16V NP0/C0G 01005 NOSTUFF LMB_2GPAD
C2303_E 10PF 5% 25V C0G 01005 NOSTUFF LMB_2GPAD

PP_QET0_PA
C2314_E 18PF 5% 16V NP0/C0G 01005 NOSTUFF LMB_2GPAD

VFE_LO_1V14_LMB_PAD
XR2304_E SHORT-01005-NOSMMEB 998-19685 LMB_2GPAD
PP_VDD_RF_1V2
C2315_E 1000PF 10% 6.3V X5R-CERM 01005 LMB_2GPAD

R2301_E 0.00 0% 1/32W MF 01005 LMB_2GPAD
50_TX_IN_XCVR_TX0_LB2G — FROM XCVR
50_TX_IN_XCVR_TX0_LB2_2G_LB_IN — C1 2G_LB_IN

R2302_E 0.00 0% 1/32W MF 01005 LMB_2GPAD
50_TX_IN_XCVR_TX0_MB2G — FROM XCVR
50_TX_IN_XCVR_TX0_MB2G_2G_MB_IN — D1 2G_MB_IN

NC — E1 NC

R2303_E 0.00 0% 1/32W MF 01005 LMB_2GPAD
50_TX_IN_XCVR_TX0_LMB — FROM XCVR
50_TX_IN_XCVR_TX0_LMB_TX_LMB_IN_2 — F1 TX_LMB_IN

PA_LMB_E
SKY58232
DSBGA
SYM 1 OF 2
PART_NUMBER=353S02393
BOMOPTION=OMIT_TABLE
SHIELD=YES
ROOM=LMB_2GPAD

SDATA_RX A7
CLK_RX A6
VIO_RX A5
SDATA_TX J4
SCLK_TX J3
VIO_TX J2
VAPT_1 F6
VAPT_2 F7
VBIAS H1
VCC1 J6
VCC2 J7
VDD_LNA A9
2G_LB_OUT B11
2G_MB_OUT D11
LMB_ANT G11
LMB_PRX_OUT C4

USID_RX=0X05
USID_TX=0X05

LMB_2GPAD 152S00493
R2305_E 0.9NH-+/-0.1NH-0.9A-0.05OHM 01005
50_TRX_IN_LMB_PAD_2G_LB_OUT — 50_TRX_IN_LMB_PAD_2G_LB_OUT_M — TO LB PAD
C2307_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

R2306_E 0.00 0% 1/32W MF 01005 LMB_2GPAD
50_TRX_IN_LMB_PAD_2G_MB_OUT — 50_TRX_IN_LMB_PAD_2G_MB_OUT_M — TO HB PAD
C2308_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

R2307_E 0.00 0% 1/32W MF 01005 LMB_2GPAD
50_TRX_IN_LMB_PAD_LMB_ANT — 50_TRX_IN_LMB_PAD_LMB_ANT_M — TO HB PAD
C2309_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

R2308_E 0.00 0% 1/32W MF 01005 LMB_2GPAD
50_RX_LMB_PAD_LMB_PRX_OUT — 50_RX_LMB_PAD_LMB_PRX_OUT_M — TO HB PAD
C2310_E 0.5PF +/-0.05PF 16V C0G-CERM 01005 LMB_2GPAD NOSTUFF

PA_LMB_E
SKY58232
DSBGA
SYM 2 OF 2
PART_NUMBER=353S02393
BOMOPTION=OMIT_TABLE
SHIELD=YES
ROOM=LMB_2GPAD

A1, A2, B3, B4, B9, B10, B12, C2, C3, C9, C10, C11, A3, C12, D2, D3, D4, D12, E2, E3, E4, E11, E12, A4, F2, F3, F4, F5, F11 GND, F12, G1, G2, G3, G4, A8, G5, G6, G7, G12, H2, H3, H4, H5, H6, H7, A10, H11, H12, J1, J5, J8, J9, J10, J11, J12, A11, A12, B1, B2

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PAGE TITLE	LMB_2G_PAD
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BRANCH	1
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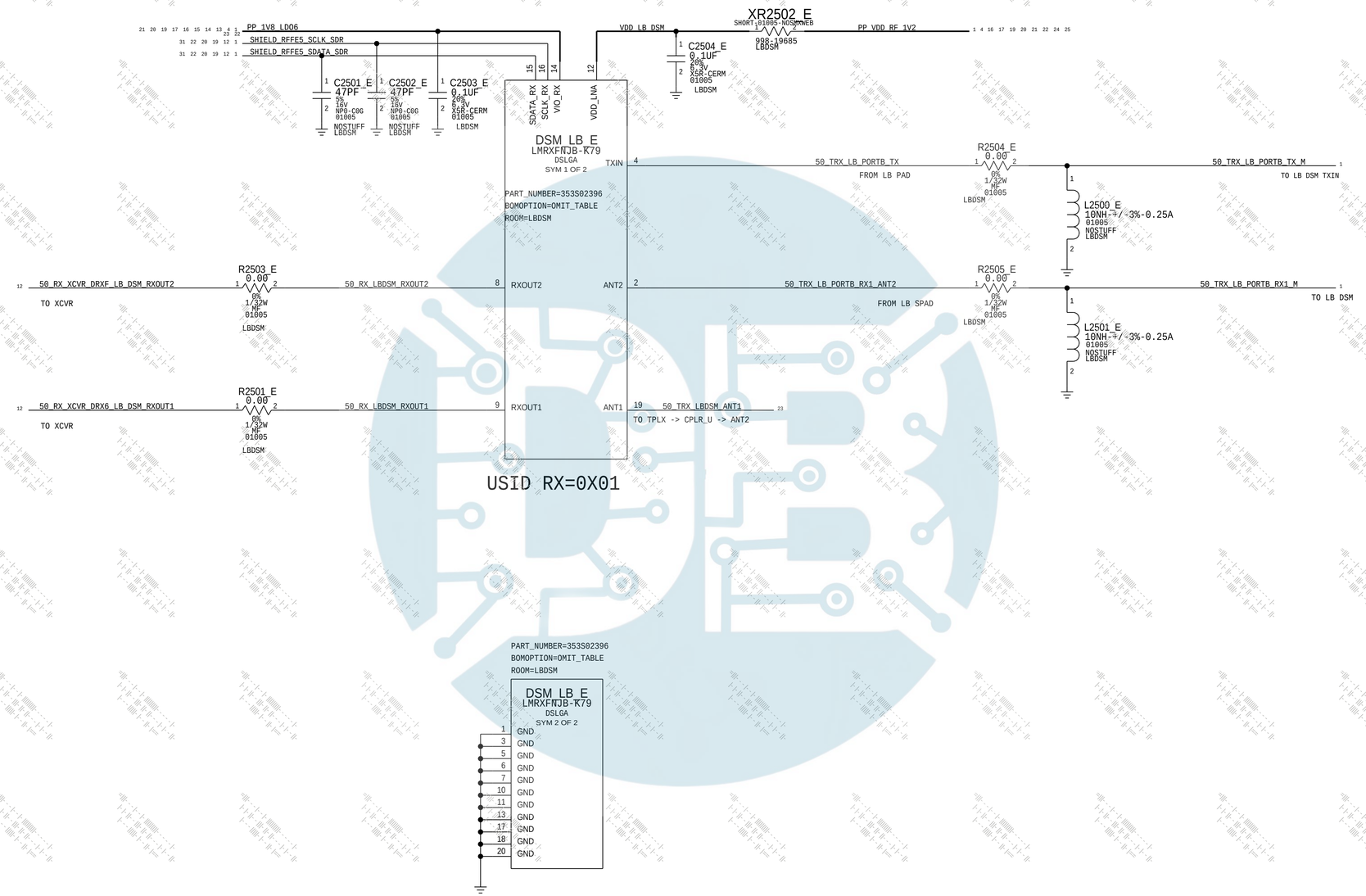
LB DIVERSITY MODULE



SYNC_DATE=08/01/2019

PAGE TITLE: LB DSM

DRAWING NUMBER: 051-05263 | SIZE: D

REVISION: 9.0.0

BRANCH: 1

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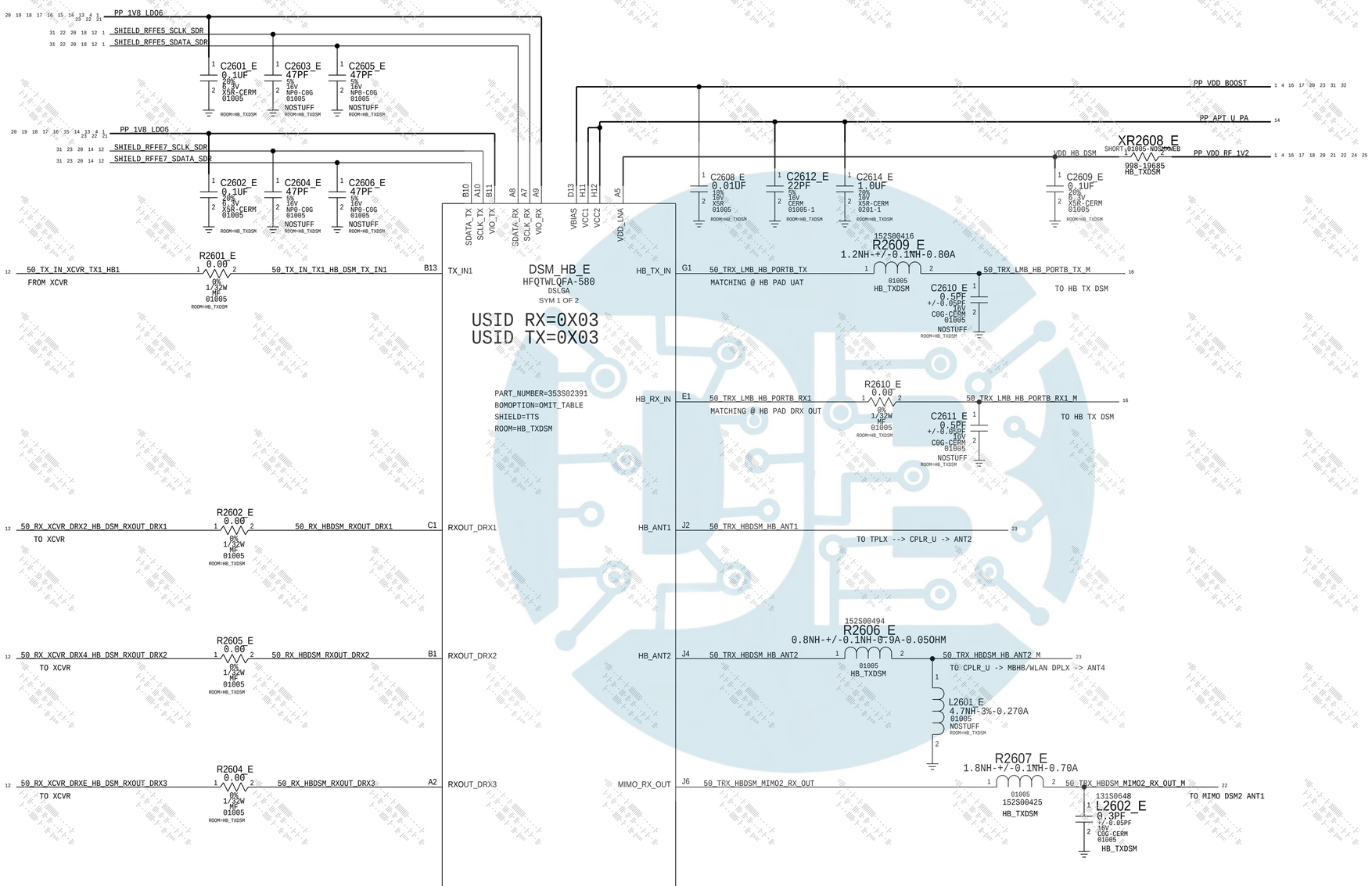
HB RECEIVE DIVERSITY & TX MODULE



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PAGE TITLE

HB TXDSM

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UHB DIVERSITY MODULE

PP_1V8_LDO6
SHIELD_RFFE5_SCLK_SDR
SHIELD_RFFE5_SDATA_SDR
SHIELD_RFFE7_SCLK_SDR
SHIELD_RFFE7_SDATA_SDR

C2701_E 47PF 5% 16V NP0-C0G 01005 UHB_UAT NOSTUFF
C2702_E 47PF 5% 16V NP0-C0G 01005 UHB_UAT NOSTUFF
C2703_E 0.1UF 20% 6.3V X5R-CERM 01005 UHB_UAT
C2721_E 47PF 5% 16V NP0-C0G 01005 UHB_UAT NOSTUFF
C2722_E 47PF 5% 16V NP0-C0G 01005 UHB_UAT NOSTUFF
C2723_E 0.1UF 20% 6.3V X5R-CERM 01005 UHB_UAT

DSMUHB_E
SKY53807
DSBGA
SYM 1 OF 2
PART_NUMBER=353S02390
SHIELD=TTS
ROOM=UHB_UAT
CRITICAL

USID RX=0X06
USID RX=0X06

SDATA_RX D4
SCLK_RX E4
VIO_RX C4
SDATA_TX D9
SCLK_TX E9
VIO_TX C9
VBIAS C6
NC F7
NC G7
VDD_LNA C7
NC B1
NC B12
FBRX1 E12

XR2705_E SHORT_01005-NOSTUFF_WEB 999-19685 UHB_UAT
VDD_UHB_DSM
PP_VDD_RF_1V2
C2704_E 0.1UF 20% 6.3V X5R-CERM 01005 UHB_UAT
PP_VDD_BOOST
C2706_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=UHB_UAT

UHB_ANT1 M2 50_TRX_PAUHBU_UHB_ANT1_TO_ANT4 27
TO UHB/N79 QPLX -> ANT4
UHB_ANT2 M3 50_TRX_PAUHBU_UHB_ANT2_TO_ANT8 26
TO UHB/N79 DPLX -> ANT8
N79_ANT1 M7 50_TRX_PAUHBU_N79_ANT1_TO_ANT4 27
TO UHB/N79 QPLX -> ANT4
N79_ANT2 M8 50_TRX_PAUHBU_N79_ANT2_TO_ANT8_M 1
TO UHB/N79 DPLX -> ANT8

UHB_ANT4 M5 50_TRX_UHB_PAD_PORTB_TX_UHB_ANT4
TO UHB UAT PAD UHB ANT 4
152S00497 R2708_E 0.5NH-+/-0.1NH-I.0A-0.040HM 01005 UHB_UAT
50_TRX_UHB_PAD_PORTB_TX_M 1
131S0037O C2708_E 0.6PF +/-0.1PF 16V NP0-C0G 01005 UHB_UAT

N79_ANT4 M10 50_TRX_UHB_PAD_N79_PORTB_TX_N79_ANT4
TO UHB UAT PAD N79 ANT4
R2709_E 0.00 1/32W MF 01005 UHB_UAT
50_TRX_UHB_PAD_N79_PORTB_TX_M 1
131S0030 C2709_E 0.4PF +/-0.05PF 16V C0G 01005 UHB_UAT

12 50_RX_XCVR_DRX14_UHB_DSM_UHB_RX_OUT1
TO XCVR
R2701_E 0.00 1/32W MF 01005 UHB_UAT
50_RX_UHB_DSM_RX_OUT1 A3 RX_OUT1

12 50_RX_XCVR_DRX12_UHB_DSM_N79_RX_OUT1
TO XCVR
R2703_E 0.00 1/32W MF 01005 UHB_UAT
50_RX_UHB_DSM_N79_RX_OUT1 A4 RX_OUT2

12 50_RX_XCVR_DRX15_UHB_DSM_UHB_RX_OUT2
TO XCVR
R2702_E 0.00 1/32W MF 01005 UHB_UAT
50_RX_UHB_DSM_RX_OUT2 A8 RX_OUT3

12 50_RX_XCVR_DRX13_UHB_DSM_N79_RX_OUT2
TO XCVR
R2704_E 0.00 1/32W MF 01005 UHB_UAT
50_RX_UHB_DSM_N79_RX_OUT2 A9 RX_OUT4

EXT_CPL1 NC
L12 L12
NC NC

DSMUHB_E
SKY53807
DSBGA
SYM 2 OF 2
PART_NUMBER=353S02390
SHIELD=TTS
ROOM=UHB_UAT
CRITICAL

GND A1 A2 A5 A6 A7 A10 A11 A12 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 C1 C2 C3 C5 C8 C10 C11 C12 D1 D2 D3 D5 D6 D7 D8 D10 D11 D12 E1 E2 E3 E5
GND E6 E7 E8 E10 E11 F1 F2 F3 F4 F5 F6 F8 F9 F10 F11 F12 G1 G2 G3 G4 G5 G6 G8 G9 G10 G11 G12 H1 H12 J1 K1 K12 L1 M1 M4 M6 M9 M11 M12

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PAGE TITLE
UHB DSM

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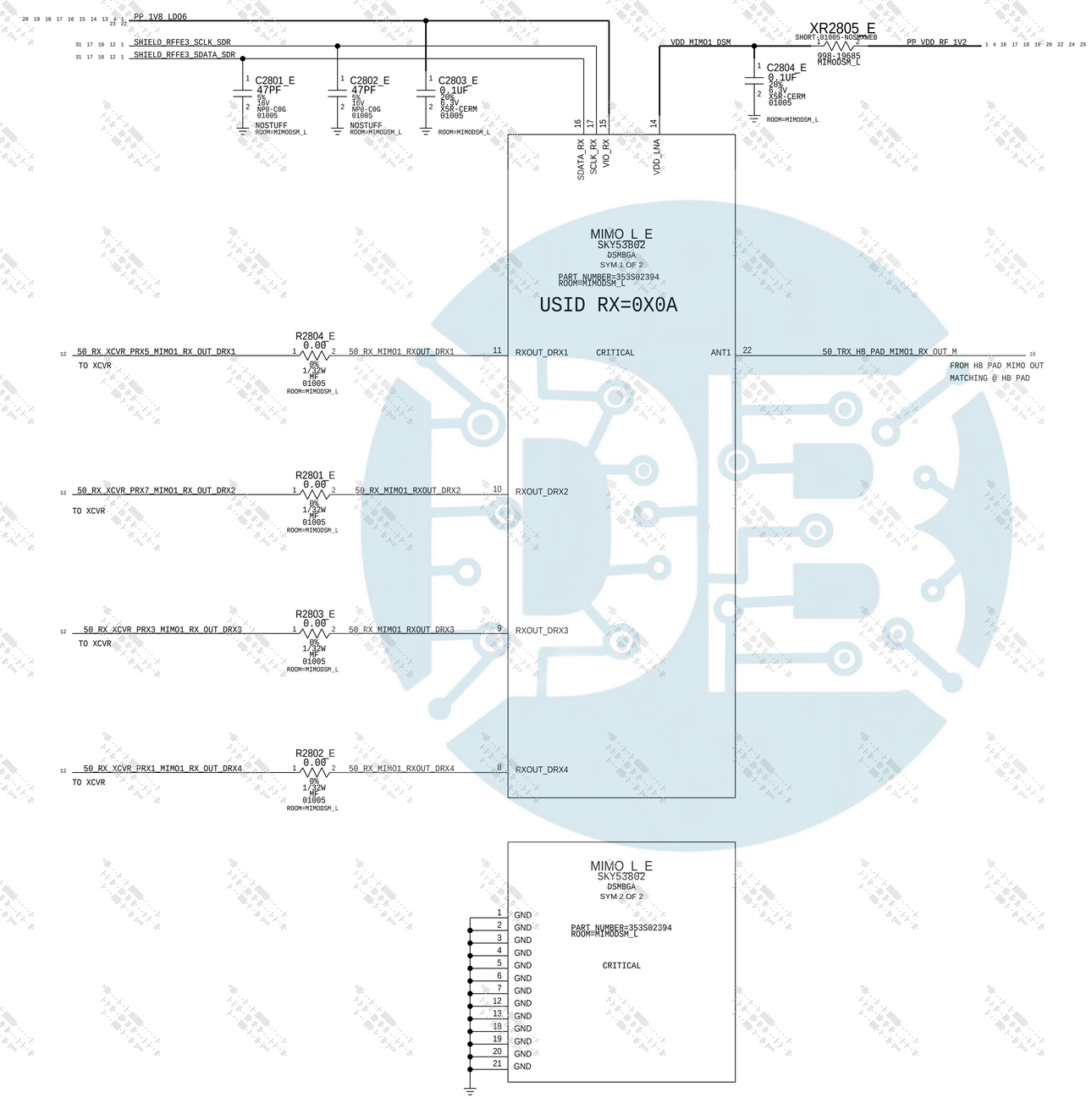
LOWER MIMO DIVERSITY MODULE



SYNC_DATE=08/01/2019

PAGE TITLE

MIMO DSM LOWER

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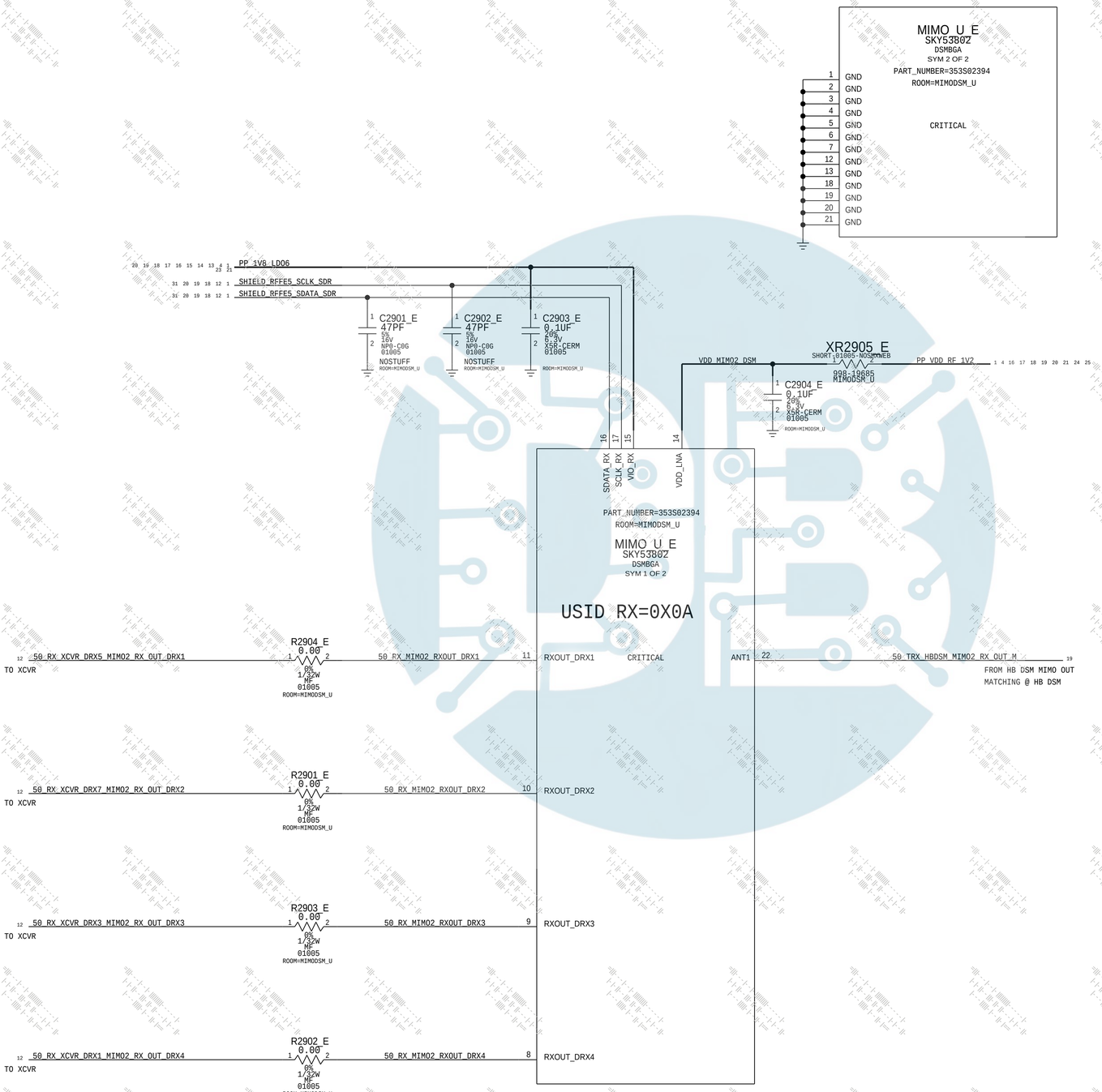
UPPER MIMO DIVERSITY MODULE



SYNC_DATE=08/01/2019

PAGE TITLE

MIMO DSM UPPER

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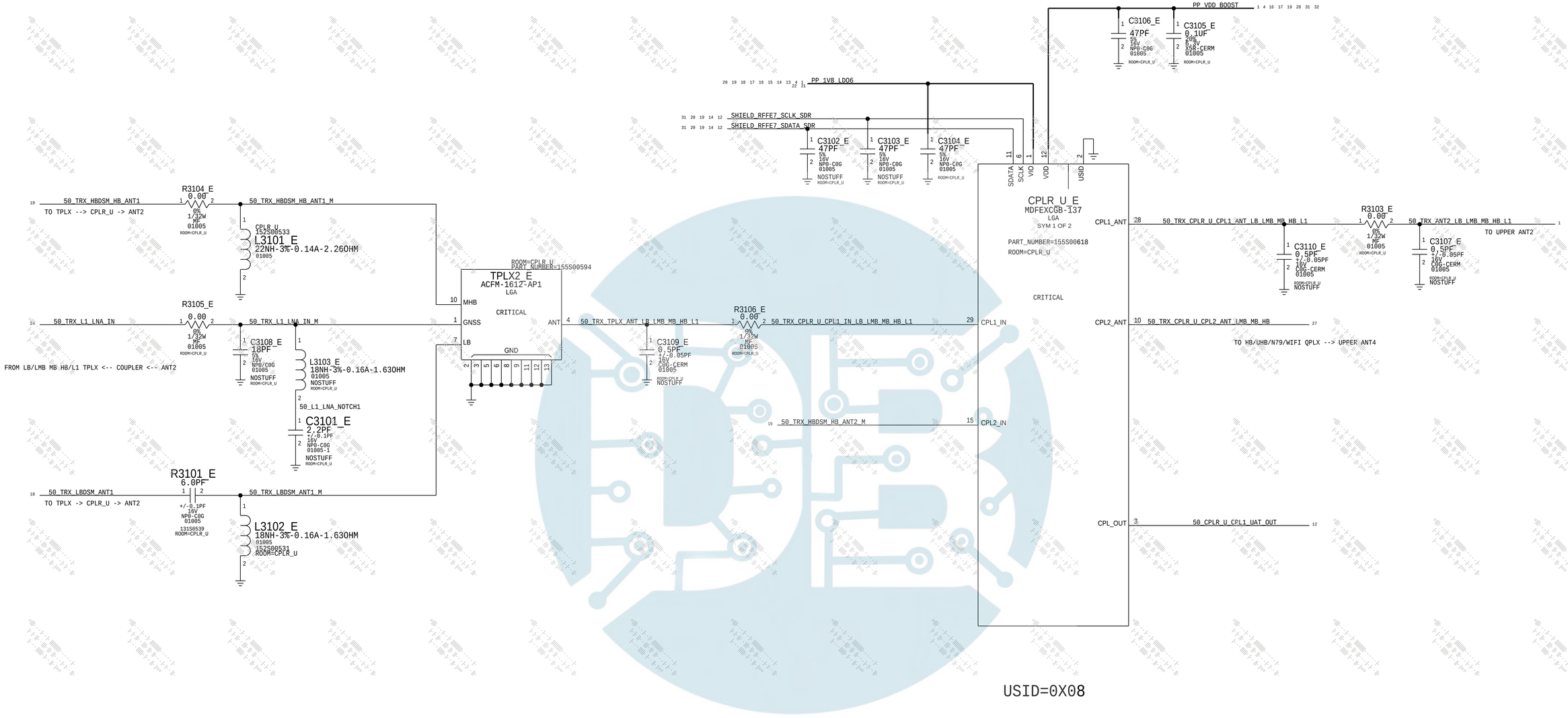
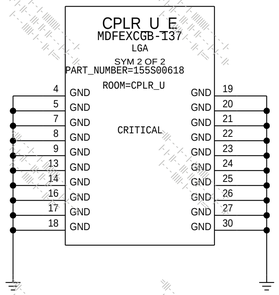
UPPER COUPLER





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PAGE TITLE
COUPLER UPPER

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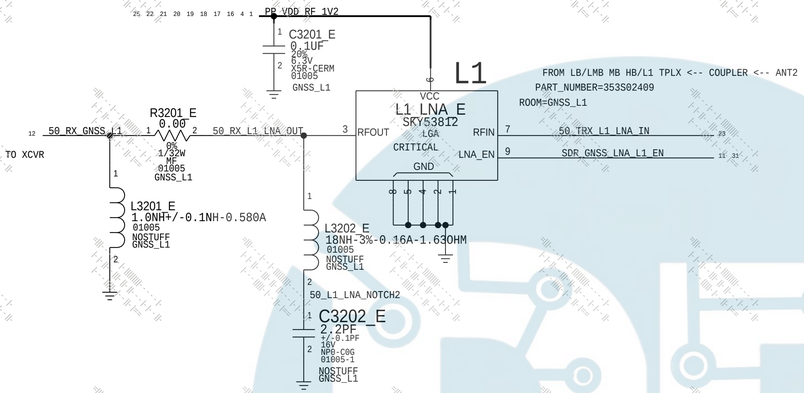
GNSS_L1



SYNC_DATE=08/01/2019

PAGE TITLE
GNSS_L1

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REVISION 9.0.0
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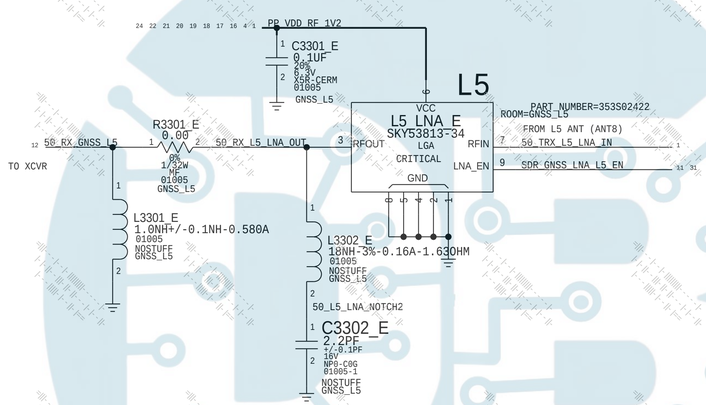
GNSS_L5



SYNC_DATE=08/01/2019

PAGE TITLE
GNSS_L5

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BRANCH 1
PAGE 33 OF 60
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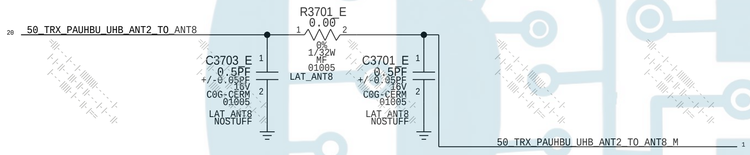
LOWER ANTENNA FEEDS: ANT8

UAT ANTENNAS

ANT2	ANT4	ANT6	ANT8
LB	MB/HB	SAM	UHB
LMB/MB/HB	2.4GHZ	5GHZ	N79
L1 GNSS	UHB		
	N79		

LAT ANTENNAS

ANT1	ANT3	ANT5	ANT7	ANT9
LB	MB/HB	5GHZ	UHB	UHB
LMB/MB/HB	2.4GHZ		N79	N79
	L5 GNSS			



ANT8

5GHZ WLAN BPF IS ON LAA SCHEMATIC (ANT5)

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PAGE TITLE
LOWER ANTENNA FEEDS_ANT8

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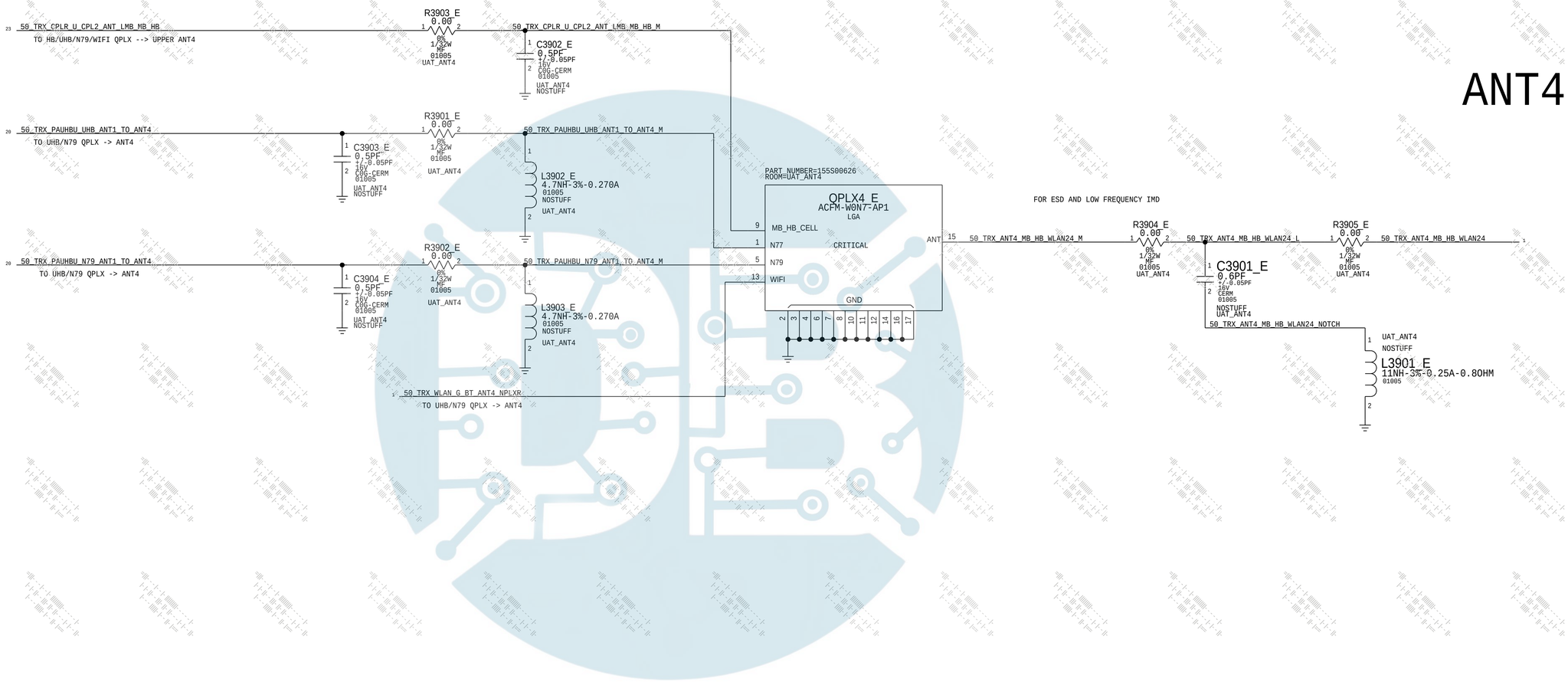
UPPER ANTENNA FEEDS

ANT4



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PAGE TITLE
UPPER ANTENNA FEEDS_ANT4

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PHYSICAL SIM
PSIM AND ESIM ARE ON FLEX FOR BOTH D53 AND D54
D53 J_SIM (PLUG.APN:516S00659) ON BOT_MAV
D54 J_SIM (PLUG.APN:516S00635) ON TOP

SIM1 IO Filters

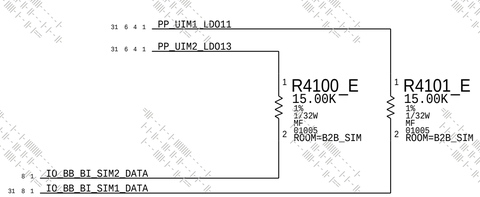
MOVE TO TOP

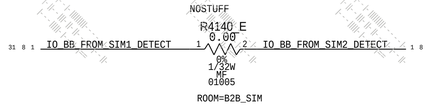
SIM2 IO Filters

MOVE TO TOP

Power Filters & Pull-ups

MOVE TWO 220PF DESENSE CAPS TO TOP





SYNC_DATE=08/01/2019

PAGE TITLE
PSIM

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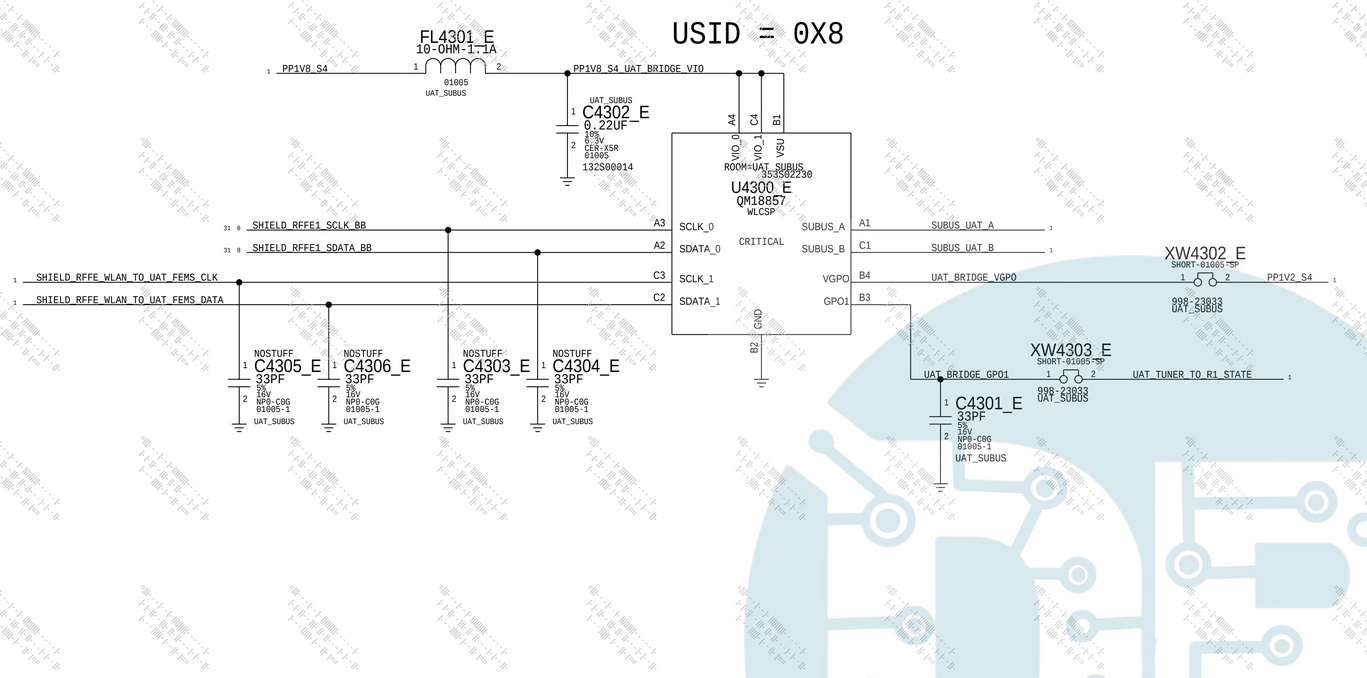
ANTENNA SYSTEM UAT



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BRANCH	1
PAGE	43 OF 60
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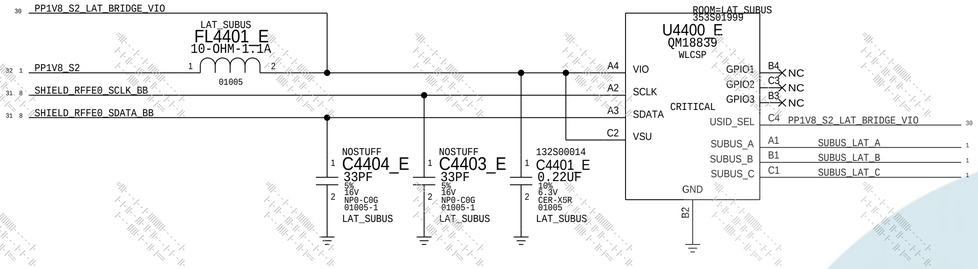
ANTENNA SYSTEM LAT

USID = 0X8 (SEL=VIO)
USID = 0XF (SEL=GND)



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PAGE TITLE

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DEBUG & BB PROBE POINTS

NOSTUFF
ROOM=DEBUG
PART_NUMBER=516S00280

JDEBUG_E
BM29P-24DP-2-0.35V
M-ST-SM

34 32 31 15 14 13 5 3 1	PP_VDD_MAIN	2	1	PP_VDD_MAIN	1 3 5 13 14 15 31 32 34
32 5 1	GPIO_SEQ_PMU_TO_BBPMU_RESET_L	4	3	PP3V0_DEBUG	32
		6	5	BB_JTAG_TDI	8
32 8	90_USB_BB_N	8	7	BB_JTAG_TDO	8
32 8	90_USB_BB_P	10	9	BB_JTAG_TRST_L	8
		12	11	BB_JTAG_RST_L	8
32 5	VBUS_DET_PMIC	14	13	UART_BB_TO_WLAN_TX	1 8
8	BB_JTAG_TCK_SWD_CLK_1V8_R	16	15	UART_BB_TO_WLAN_RX	1 8
8	BB_JTAG_TMS_SWD_IO_1V8_R	18	17	UART1_AOP_TO_BB_TXD	1 8
8 1	IO_BB_TO_SIM1_RESET	20	19	UART1_AOP_FROM_BB_RXD	1 8
28 8 1	IO_BB_FROM_SIM1_DETECT	22	21	IO_BB_TO_SIM1_CLK	1 8
31 28 6 4 1	PP_UIM1_LDO11	24	23	IO_BB_BI_SIM1_DATA	1 8 28
		26	25		
		28	27		

SDR RFFE

PP4620_E	SHIELD_RFFE1_SDATA_SDR	1 12 13 16 17
PP4621_E	SHIELD_RFFE1_SCLK_SDR	1 12 13 16 17
PP4622_E	SHIELD_RFFE2_SDATA_SDR	1 12 15
PP4623_E	SHIELD_RFFE2_SCLK_SDR	1 12 15
PP4624_E	SHIELD_RFFE3_SDATA_SDR	1 12 16 17 21
PP4625_E	SHIELD_RFFE3_SCLK_SDR	1 12 16 17 21
PP4626_E	SHIELD_RFFE5_SDATA_SDR	1 12 18 19 20 22
PP4627_E	SHIELD_RFFE5_SCLK_SDR	1 12 18 19 20 22
PP4628_E	SHIELD_RFFE7_SDATA_SDR	12 14 19 20 23
PP4629_E	SHIELD_RFFE7_SCLK_SDR	12 14 19 20 23
PP4642_E	SHIELD_RFFE8_SDATA_SDR	1 12
PP4643_E	SHIELD_RFFE8_SCLK_SDR	1 12

BB RFFE

PP4712_E	SHIELD_RFFE0_SDATA_BB	8 30
PP4714_E	SHIELD_RFFE0_SCLK_BB	8 30
PP4716_E	SHIELD_RFFE1_SDATA_BB	8 29
PP4718_E	SHIELD_RFFE1_SCLK_BB	8 29

QLINK RFFE

PP4640_E	SHIELD_RFFE4_SDATA_BB	8 12 33
PP4641_E	SHIELD_RFFE4_SCLK_BB	8 12 33

AP POWER

PP4720_E	PP_VDD_MAIN	1 3 5 13 14 15 31 32 34
PP4679_E	PP_VDD_BOOST	1 4 16 17 19 20 23 32
PP4698_E	PP3V0_S2	1 12 32

BB POWER

PP4721_E	PP_0V75_SMPS1_6	3 6
PP4722_E	PP_1V22_SMPS2	3 4
PP4723_E	PP_0V82_SMPS3	3 4 6
PP4724_E	PP_1V9_SMPS4	3 4 34
PP4725_E	PP_0V75_SMPS5	3 6
PP4726_E	PP_0V75_SMPS7	3 4 6
PP4727_E	PP_1V2_LDO1	4 6 9
PP4728_E	PP_1V1_LDO2	4 6
PP4729_E	PP_0V8_LDO3	4 10
PP4730_E	PP_0V875_LDO4	4 6 9 33
PP4731_E	PP_1V8_LDO5	4 6 33
PP4647_E	PP_1V8_LDO6	4 5 6 8 9 32 33
PP4733_E	PP_0V8_LDO7	4 33
PP4734_E	PP_0V8_LDO8	4 9
PP4735_E	PP_0V8_LDO9	4 33
PP4736_E	PP_3V1_LDO10	4 6
PP4737_E	PP_UIM1_LDO11	1 4 6 28 31
PP4738_E	PP_1V2_LDO12	4 33
PP4739_E	PP_UIM2_LDO13	1 4 6 28
PP4740_E	PP_0V6_LDO14	4 6 8
PP4741_E	PP_1V2_LDO15	4 6 32
PP4742_E	PP_1V7_LDO16	4 9

PCIE

PP4634_E	90_PCIE_GP2_AP_TO_BB_TX_P	1 8
PP4635_E	90_PCIE_GP2_AP_TO_BB_TX_N	1 8
PP4636_E	90_PCIE_GP2_AP_FROM_BB_RX_P	1 8
PP4637_E	90_PCIE_GP2_AP_FROM_BB_RX_N	1 8
PP4638_E	90_PCIE_GP2_AP_TO_BB_REFCLK_P	1 8
PP4639_E	90_PCIE_GP2_AP_TO_BB_REFCLK_N	1 8
PP4684_E	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_L	1 8 32
PP4685_E	PCIE_GP2_AP_TO_BB_PERST_L	1 8
PP4686_E	PCIE_GP2_AP_BI_BB_CLKREQ_L	1 8 32

CLOCKS

PP4651_E	SHIELD_MDM_19P2M_CLK	5 8
PP4690_E	SHIELD_SDR_38P4M_CLK	5 12
PP4608_E	SHIELD_SMR_38P4M_CLK	5 33
PP4609_E	CLK_BBPMU_TO_DOTARA_38M4_R	1 5
PP4610_E	CLK_BBPMU_TO_NFC_38M	1 5
PP4611_E	SHIELD_PMK_32K_SLEEP_CLK	5
PP4612_E	SHIELD_SLEEP_CLK_32K	5 8

DOTARA

PP4632_E	GPIO_NUB_TO_BBPMU_CLK_EN_DOTARA	5

I2S

PP4693_E	I2S2_AP_TO_BB_DOUT	1 8
PP4694_E	I2S2_AP_FROM_BB_BCLK	1 8
PP4695_E	I2S2_AP_FROM_BB_DIN	1 8
PP4696_E	I2S2_AP_FROM_BB_LRCLK	1 8

BASEBAND

PP4652_E	GPIO_AP_TO_BB_COREDUMP	1 8
PP4658_E	GPIO_AP_TO_BB_TIME_MARK	1 8
PP4655_E	BB_BBPMU_SPMI_CLK	5 8
PP4656_E	BB_BBPMU_SPMI_DATA	5 8
PP4671_E	BB_EEPROM_I2C_SCL	8
PP4672_E	BB_EEPROM_I2C_SDA	8
PP4653_E	IO_TOUCH_TO_MANY_SCAN_ACTIVE	1 5
PP4654_E	GPIO_AOP_TO_BB_FORCE_PWM	1 5
PP4687_E	GPIO_AP_FROM_BB_RESET_DETECT_L	1 8
PP4688_E	PMIC_RESOUT_L	5 8
PP4689_E	GPIO_BB_TO_ALS_GSM_BURST_IND_1V8	1 8
PP4600_E	GPIO_AP_TO_BB_PEAK_PWR_IND	1 8
PP4660_E	PS_HOLD	5 8
PP4644_E	PP_PMX_VIO_OUT	5 6
PP4743_E	BOOT_CFG1	8 32
PP4744_E	BOOT_CFG2	8 32
PP4732_E	BB_TO_SDR_WMSS_RESET_L	8 11
PP4745_E	BB_TO_SMR_WMSS_RESET_L	8 33

SWD

PP4691_E	SWD_AP_TO_MANY_SWCLK	1 8
PP4692_E	SWD_AP_BI_BB_SWDIO	1 8

QLINK

PP4681_E	QLINK_REQ_SDR_TO_BB	8 11
PP4682_E	QLINK_EN_BB_TO_SDR	8 11
PP4683_E	QLINK_REQ_SMR_TO_BB	8 33
PP4605_E	QLINK_EN_BB_TO_SMR	8 33
PP4601_E	85_SUB6_QLINK_L0_P	8 11
PP4602_E	85_SUB6_QLINK_L0_N	8 11
PP4603_E	85_MMW_QLINK_L0_P	8 33
PP4604_E	85_MMW_QLINK_L0_N	8 33

R1

PP4661_E	GPIO_BB_TO_R1_COEX	1 8
PP4662_E	GPIO_BB_TO_R1_CH9_REQ	1 8
PP4668_E	GPIO_R1_TO_BB_CH9_COEX	1 8
PP4669_E	GPIO_R1_TO_BB_LAA_SW_CTRL	8

STOCKHOLM

PP4670_E	GPIO_NFC_TO_BBPMU_CLK_EN	1 5

GNSS

PP4645_E	SDR_GNSS_LNA_L1_EN	11 24
PP4646_E	SDR_GNSS_LNA_L5_EN	11 25

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DEBUG & TEST POINTS

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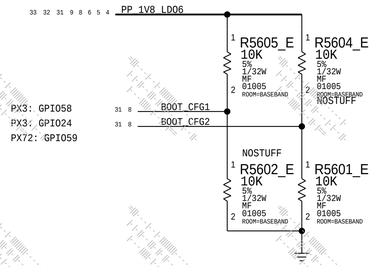
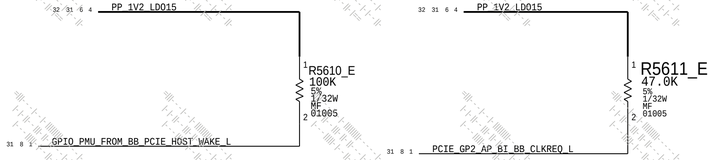
ADJUSTABLES



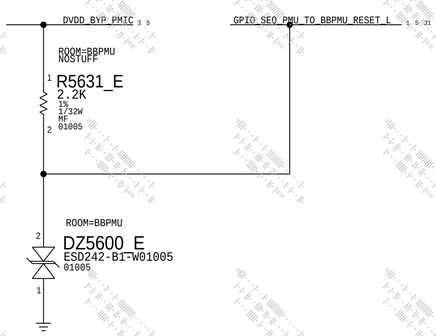
BOOT SEQ	BOOT_CFG3	BOOT_CFG2	BOOT_CFG1	CONFIG
NAND>HSUSB	0	0	0	
PCIE	0	0	1	POR
USB	0	1	0	EUREKA
EMMC>USB	0	1	1	

POR PCIE BOOT:
BOOT_CFG2 PD, BOOT_CFG1 PU

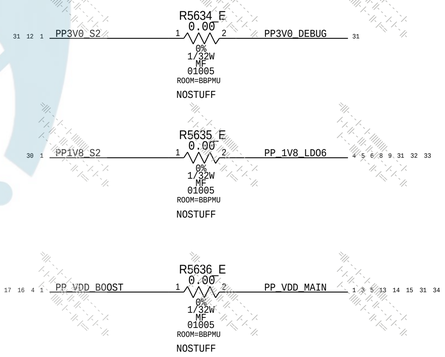
EUREKA CONFIG USB BOOT:
BOOT_CFG2 PU, BOOT_CFG1 PD

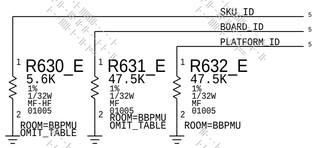


AUTO POWER ON FOR EUREKA CONFIG
+ BB PMU ESD DIODE PROTECTION

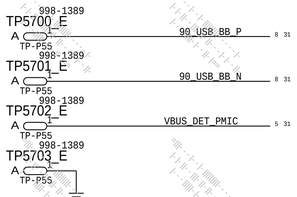


STUFF ONLY FOR VENDOR CONFIG





USB TP FOR TEXT FIXTURE



SYNC_DATE=08/01/2019

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ADJUSTABLES

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MMW IF TRANSCEIVER IC

1.2A VDD_CX MAX CURRENT

PP_0V8_LDO7

C5801_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC

BOMOPTION=RF_SKU:NAMM

C5804_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5807_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5809_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5830_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

PP_1V8_LDO6

XW5801_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

C5802_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

PP_LDO6_SMR_VDD_PX_20

C5805_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC RF_SKU:NAMM

PP_0V875_LDO4

XW5824_E SHORT-8L-0.25MM-SM ROOM=MMW_IFIC

PP_LDO4_SMR_MX_115

C5803_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

XW5825_E SHORT-8L-0.25MM-SM ROOM=MMW_IFIC

PP_LDO4_SMR_PHY_152

C5806_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5808_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

PART_NUMBER=338S00651
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 2 OF 3
CRITICAL

B12	VDD_CX	VDDAH_1	A7
F12	VDD_CX	VDDAH_2	H4
M14	VDD_CX	VDDAH_3	P2
R7	VDD_CX	VDDAH_4	H8
P10	VDD_PX	VDDAL_1	C5
P12	VDD_MX	VDDAL_2	B4
H18	VDDA_PHY	VDDAL_3	F4
		VDDAL_4	R5
		VDDAL_5	B10
		VDDAL_6	E11
		VDDAL_7	R9
		VDDAM_1	B6
		VDDAM_2	G5
		VDDAM_3	P4
		VDDAM_4	A9
		VDDAM_5	P8

PP_LDO5_SMR_VDDAH_1_10 — XW5802_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC — PP_1V8_LDO5

PP_LDO5_SMR_VDDAH_2_140 — XW5803_E SHORT-8L-0.25MM-SM ROOM=MMW_IFIC

C5823_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

PP_LDO5_SMR_VDDAH_3_10 — XW5804_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

PP_LDO5_SMR_VDDAH_4_40 — XW5805_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

C5812_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5814_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5818_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5820_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

PP_LDO9_SMR_VDDAL_1_50 — XW5806_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC — PP_0V8_LDO9

PP_LDO9_SMR_VDDAL_2_10 — XW5807_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

C5828_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

PP_LDO9_SMR_VDDAL_3_140 — XW5808_E SHORT-8L-0.25MM-SM ROOM=MMW_IFIC

PP_LDO9_SMR_VDDAL_4_90 — XW5809_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

PP_LDO9_SMR_VDDAL_5_10 — XW5810_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

PP_LDO9_SMR_VDDAL_6_10 — XW5811_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

PP_LDO9_SMR_VDDAL_7_10 — XW5812_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

C5810_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5813_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5816_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5819_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5822_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5825_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5826_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

PLACE C5813 CLOSE TO PIN B4

XW5813_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

PP_LDO12_SMR_VDDAM_1_70 — XW5814_E SHORT-8L-0.25MM-SM ROOM=MMW_IFIC — PP_1V2_LDO12

VDD_AM MAX CURRENT 740 MA

PP_LDO12_SMR_VDDAM_2_120 — XW5815_E SHORT-8L-0.1MM-SM ROOM=MMW_IFIC

C5827_E 4UF 20% 6.3V CER-X5R 0201 ROOM=MMW_IFIC BOMOPTION=RF_SKU:NAMM

PP_LDO12_SMR_VDDAM_3_70

VDDAM_4:0.24A

VDDAM_5:0.24A

C5811_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5815_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5817_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5821_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

C5824_E 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=MMW_IFIC — RF_SKU:NAMM

PART_NUMBER=338S00651
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 1 OF 3
CRITICAL

SHIELD_SMR_38P4M_CLK	A3	XO_IN	XO
	G9	XO_SEL	XO
	J1	IFH1	IF
50_MMW_SMR526_IFH2	K2	IFH2	IF
50_MMW_SMR526_IFH3	L1	IFH3	IF
	M2	IFH4	IF
	F2	IFV1	IF
50_MMW_SMR526_IFV2	E1	IFV2	IF
50_MMW_SMR526_IFV3	D2	IFV3	IF
	C1	IFV4	IF
SMR_TO_FEZ_PON	P6	GRFC_1_QTM3_PON	GRFC
	G7	GRFC_2_QTM0_PON	GRFC
	K10	GRFC_3	GRFC
	J7	GRFC_4_QTM1_PON	GRFC
SMR_TO_TANGIER_PON	N5	GRFC_5_QTM2_PON	GRFC
	D12	GRFC_6	GRFC
	M12	GRFC_7	GRFC
	N11	GRFC_8	GRFC
	H12	GRFC_9	GRFC
	J11	GRFC_10	GRFC
SHIELD_RFFE4_SDATA_BB	K12	RFFE0_DATA	RFFE
SHIELD_RFFE4_SCLK_BB	L11	RFFE0_CLK	RFFE
	C11	DNC	DNC
QLINK_REQ_SMR_TO_BB	D14	QLINK_REQ	QLINK PHY
QLINK_EN_BB_TO_SMR	G13	QLINK_EN	QLINK PHY
BB_TO_SMR_WMSS_RESET_L	J13	WMSS_RESET*	QLINK PHY

QLINK_L0_P	K14	85_MMW_QLINK_L0_P	8
QLINK_L0_M	J15	85_MMW_QLINK_L0_N	8
QLINK_L1_P	G15	85_MMW_QLINK_L1_P	8
QLINK_L1_M	F14	85_MMW_QLINK_L1_N	8
QLINK_L2_P	E15	85_MMW_QLINK_L2_P	8
QLINK_L2_M	D16	85_MMW_QLINK_L2_N	8
QLINK_L3_P	L15	85_MMW_QLINK_L3_P	8
QLINK_L3_M	M16	85_MMW_QLINK_L3_N	8
QLINK_L4_P	P16	85_MMW_QLINK_L4_P	8
QLINK_L4_M	R15	85_MMW_QLINK_L4_N	8
QLINK_L5_P	D18	85_MMW_QLINK_L5_P	8
QLINK_L5_M	E17	85_MMW_QLINK_L5_N	8
QLINK_L6_P	B16	85_MMW_QLINK_L6_P	8
QLINK_L6_M	A15	85_MMW_QLINK_L6_N	8
QLINK_L7_P	K18	85_MMW_QLINK_L7_P	8
QLINK_L7_M	J17	85_MMW_QLINK_L7_N	8
QLINK_L8_P	L17	85_MMW_QLINK_L8_P	8
QLINK_L8_M	M18	85_MMW_QLINK_L8_N	8
QLINK_L9_P	P18	85_MMW_QLINK_L9_P	8
QLINK_L9_M	R17	85_MMW_QLINK_L9_N	8
QLINK_L10_P	A13	85_MMW_QLINK_L10_P	8
QLINK_L10_M	B14	85_MMW_QLINK_L10_N	8
QLINK_L11_P	B18	85_MMW_QLINK_L11_P	8
QLINK_L11_M	A17	85_MMW_QLINK_L11_N	8
QLINK_L12_P	R13	85_MMW_QLINK_L12_P	8
QLINK_L12_M	P14	85_MMW_QLINK_L12_N	8
QLINK_CLK_P	G17	85_MMW_QLINK_CLK_P	8
QLINK_CLK_M	F18	85_MMW_QLINK_CLK_N	8

PART_NUMBER=338S00651
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_IFIC

U_SMR_E
SMR526-0
PSP
SYM 3 OF 3
CRITICAL

A1	GND	GND	H10
A5	GND	GND	H14
A11	GND	GND	H16
B2	GND	GND	J3
B8	GND	GND	J5
C3	GND	GND	J9
C7	GND	GND	K4
C9	GND	GND	K6
C13	GND	GND	K8
C15	GND	GND	K16
C17	GND	GND	L3
D4	GND	GND	L5
D6	GND	GND	L7
D8	GND	GND	L9
D10	GND	GND	L13
E3	GND	GND	M4
E5	GND	GND	M6
E7	GND	GND	M8
E9	GND	GND	M10
E13	GND	GND	N1
F6	GND	GND	N3
F8	GND	GND	N7
F10	GND	GND	N9
F16	GND	GND	N13
G1	GND	GND	N15
G3	GND	GND	N17
G11	GND	GND	R1
H2	GND	GND	R3
H6	GND	GND	R11

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TANGIER SIP

PART_NUMBER=339M00112
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

U_TAN_E
LBKA0QE1XR-481
SIP-1
SYM 1 OF 4

SMR_TO_TANGIER_PON — R5932_E 100K 5% 1/32W MF 01005 — ROOM=MMW_SIP — BOMOPTION=RF_SKU:NAMM

PP5901_E	TANGIER_TP1	386	TP1
PP5902_E	TANGIER_TP2	379	TP2
PP5903_E	TANGIER_TP3	380	TP3
PP5904_E	TANGIER_TP4	319	TP4
PP5905_E	TANGIER_TP5	378	TP5
PP5906_E	TANGIER_TP6	375	TP6
PP5907_E	TANGIER_TP7	376	TP7
PP5908_E	TANGIER_RFFE_CLK	358	RFFE_CLK
PP5909_E	TANGIER_RFFE_DATA	377	RFFE_DATA
PP5910_E	50_TANGIER_TP11	298	TP11

50_MMW_SMR526_IFH2 — 373 — 50_IF1_H
50_MMW_SMR526_IFV3 — 382 — 50_IF2_V

PP_VDD_MAIN — C5901_E 131S00303 100PF 5% 16V NP0-C0G 01005-1 — ROOM=MMW_SIP — 68 VBATT, 69 VBATT, 90 VBATT, 91 VBATT, 92 VBATT

PP_1V8_SMPS4 (MAKE_BASE=TRUE) — PP_1V8_SMPS4 — C5902_E 131S00303 100PF 5% 16V NP0-C0G 01005-1 — ROOM=MMW_SIP — 42 VDD_IO_1V85

BOMOPTION=RF_SKU:NAMM

V_ON — CRITICAL

50_RFH_Q1_39G_S1	209	50_MMW_SMR525_S1H_HPOL	35
50_RFH_Q1_28G_S1	208	50_MMW_SMR525_S1L_HPOL	35
50_RFH_Q1_39G_S2	210	50_MMW_SMR525_S2H_HPOL	35
50_RFH_Q1_28G_S2	211	50_MMW_SMR525_S2L_HPOL	35
50_RFH_Q1_39G_S3	335		
50_RFH_Q1_28G_S3	334		
50_RFH_Q1_39G_S4	336		
50_RFH_Q1_28G_S4	337		
50_RFH_Q2_39G_S5	206	50_MMW_SMR525_S5H_HPOL	35
50_RFH_Q2_28G_S5	207	50_MMW_SMR525_S5L_HPOL	35
50_RFH_Q2_39G_S6	205	50_MMW_SMR525_S6H_HPOL	35
50_RFH_Q2_28G_S6	204	50_MMW_SMR525_S6L_HPOL	35
50_RFH_Q2_39G_S7	332	50_MMW_SMR525_S7H_HPOL	34
50_RFH_Q2_28G_S7	333	50_MMW_SMR525_S7L_HPOL	34
50_RFH_Q2_39G_S8	331	50_MMW_SMR525_S8H_HPOL	34
50_RFH_Q2_28G_S8	330	50_MMW_SMR525_S8L_HPOL	34
50_RFV_Q3_39G_S9	216	50_MMW_SMR525_S9H_VPOL	35
50_RFV_Q3_28G_S9	217	50_MMW_SMR525_S9L_VPOL	35
50_RFV_Q3_39G_S10	215	50_MMW_SMR525_S10H_VPOL	35
50_RFV_Q3_28G_S10	214	50_MMW_SMR525_S10L_VPOL	35
50_RFV_Q3_39G_S11	342	50_MMW_SMR525_S11H_VPOL	34
50_RFV_Q3_28G_S11	343	50_MMW_SMR525_S11L_VPOL	34
50_RFV_Q3_39G_S12	341	50_MMW_SMR525_S12H_VPOL	34
50_RFV_Q3_28G_S12	340	50_MMW_SMR525_S12L_VPOL	34
50_RFV_Q4_39G_S13	219	50_MMW_SMR525_S13H_VPOL	35
50_RFV_Q4_28G_S13	218	50_MMW_SMR525_S13L_VPOL	35
50_RFV_Q4_39G_S14	220	50_MMW_SMR525_S14H_VPOL	35
50_RFV_Q4_28G_S14	221	50_MMW_SMR525_S14L_VPOL	35
50_RFV_Q4_39G_S15	345		
50_RFV_Q4_28G_S15	344		
50_RFV_Q4_39G_S16	346		
50_RFV_Q4_28G_S16	347		

SMYRNA

PART_NUMBER=518S00234
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

J_SMYR_E
MM3631-2703A16
F-ST-SM

50_MMW_SMR525_S11L_VPOL	34	9	50_MMW_SMR525_S11H_VPOL 34
50_MMW_SMR525_S7L_HPOL	34	11	50_MMW_SMR525_S7H_HPOL 34
50_MMW_SMR525_S12H_VPOL	34	13	50_MMW_SMR525_S8L_HPOL 34
50_MMW_SMR525_S8H_HPOL	34	15	50_MMW_SMR525_S12L_VPOL 34

PART_NUMBER=339M00112
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

U_TAN_E
LBKA0QE1XR-481
SIP-1
SYM 2 OF 4

CRITICAL

1	GND	GND	66	136	GND	GND	200
2	GND	GND	67	137	GND	GND	201
3	GND	GND	70	138	GND	GND	202
4	GND	GND	71	139	GND	GND	203
5	GND	GND	72	140	GND	GND	212
6	GND	GND	73	141	GND	GND	213
7	GND	GND	74	142	GND	GND	222
8	GND	GND	75	143	GND	GND	223
9	GND	GND	76	144	GND	GND	224
10	GND	GND	77	145	GND	GND	225
11	GND	GND	78	146	GND	GND	226
12	GND	GND	80	147	GND	GND	227
13	GND	GND	81	148	GND	GND	228
14	GND	GND	82	149	GND	GND	229
15	GND	GND	83	150	GND	GND	230
16	GND	GND	84	151	GND	GND	231
17	GND	GND	85	152	GND	GND	232
18	GND	GND	86	153	GND	GND	233
19	GND	GND	87	154	GND	GND	234
20	GND	GND	88	155	GND	GND	235
21	GND	GND	89	156	GND	GND	236
22	GND	GND	93	157	GND	GND	237
23	GND	GND	94	158	GND	GND	238
24	GND	GND	95	159	GND	GND	239
25	GND	GND	96	160	GND	GND	240
26	GND	GND	97	161	GND	GND	241
27	GND	GND	98	162	GND	GND	242
28	GND	GND	99	163	GND	GND	243
29	GND	GND	100	164	GND	GND	244
30	GND	GND	101	165	GND	GND	245
31	GND	GND	102	166	GND	GND	246
32	GND	GND	103	167	GND	GND	247
33	GND	GND	104	168	GND	GND	248
34	GND	GND	105	169	GND	GND	249
35	GND	GND	106	170	GND	GND	250
36	GND	GND	107	171	GND	GND	251
37	GND	GND	108	172	GND	GND	252
38	GND	GND	109	173	GND	GND	253
39	GND	GND	110	174	GND	GND	254
40	GND	GND	111	175	GND	GND	255
41	GND	GND	112	176	GND	GND	256
43	GND	GND	113	177	GND	GND	257
44	GND	GND	114	178	GND	GND	258
45	GND	GND	115	179	GND	GND	259
46	GND	GND	116	180	GND	GND	260
47	GND	GND	117	181	GND	GND	261
48	GND	GND	118	182	GND	GND	262
49	GND	GND	119	183	GND	GND	263
50	GND	GND	120	184	GND	GND	264
51	GND	GND	121	185	GND	GND	265
52	GND	GND	122	186	GND	GND	266
53	GND	GND	123	187	GND	GND	267
54	GND	GND	124	188	GND	GND	268
55	GND	GND	125	189	GND	GND	269
56	GND	GND	126	190	GND	GND	270
57	GND	GND	127	191	GND	GND	271
58	GND	GND	128	192	GND	GND	272
59	GND	GND	129	193	GND	GND	273
60	GND	GND	130	194	GND	GND	274
61	GND	GND	131	195	GND	GND	275
62	GND	GND	132	196	GND	GND	276
63	GND	GND	133	197	GND	GND	277
64	GND	GND	134	198	GND	GND	278
65	GND	GND	135	199	GND	GND	279

PART_NUMBER=339M00112
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

U_TAN_E
LBKA0QE1XR-481
SIP-1
SYM 3 OF 4

CRITICAL

1	GND	GND	66	136	GND	GND	200
2	GND	GND	67	137	GND	GND	201
3	GND	GND	70	138	GND	GND	202
4	GND	GND	71	139	GND	GND	203
5	GND	GND	72	140	GND	GND	212
6	GND	GND	73	141	GND	GND	213
7	GND	GND	74	142	GND	GND	222
8	GND	GND	75	143	GND	GND	223
9	GND	GND	76	144	GND	GND	224
10	GND	GND	77	145	GND	GND	225
11	GND	GND	78	146	GND	GND	226
12	GND	GND	80	147	GND	GND	227
13	GND	GND	81	148	GND	GND	228
14	GND	GND	82	149	GND	GND	229
15	GND	GND	83	150	GND	GND	230
16	GND	GND	84	151	GND	GND	231
17	GND	GND	85	152	GND	GND	232
18	GND	GND	86	153	GND	GND	233
19	GND	GND	87	154	GND	GND	234
20	GND	GND	88	155	GND	GND	235
21	GND	GND	89	156	GND	GND	236
22	GND	GND	93	157	GND	GND	237
23	GND	GND	94	158	GND	GND	238
24	GND	GND	95	159	GND	GND	239
25	GND	GND	96	160	GND	GND	240
26	GND	GND	97	161	GND	GND	241
27	GND	GND	98	162	GND	GND	242
28	GND	GND	99	163	GND	GND	243
29	GND	GND	100	164	GND	GND	244
30	GND	GND	101	165	GND	GND	245
31	GND	GND	102	166	GND	GND	246
32	GND	GND	103	167	GND	GND	247
33	GND	GND	104	168	GND	GND	248
34	GND	GND	105	169	GND	GND	249
35	GND	GND	106	170	GND	GND	250
36	GND	GND	107	171	GND	GND	251
37	GND	GND	108	172	GND	GND	252
38	GND	GND	109	173	GND	GND	253
39	GND	GND	110	174	GND	GND	254
40	GND	GND	111	175	GND	GND	255
41	GND	GND	112	176	GND	GND	256
43	GND	GND	113	177	GND	GND	257
44	GND	GND	114	178	GND	GND	258
45	GND	GND	115	179	GND	GND	259
46	GND	GND	116	180	GND	GND	260
47	GND	GND	117	181	GND	GND	261
48	GND	GND	118	182	GND	GND	262
49	GND	GND	119	183	GND	GND	263
50	GND	GND	120	184	GND	GND	264
51	GND	GND	121	185	GND	GND	265
52	GND	GND	122	186	GND	GND	266
53	GND	GND	123	187	GND	GND	267
54	GND	GND	124	188	GND	GND	268
55	GND	GND	125	189	GND	GND	269
56	GND	GND	126	190	GND	GND	270
57	GND	GND	127	191	GND	GND	271
58	GND	GND	128	192	GND	GND	272
59	GND	GND	129	193	GND	GND	273
60	GND	GND	130	194	GND	GND	274
61	GND	GND	131	195	GND	GND	275
62	GND	GND	132	196	GND	GND	276
63	GND	GND	133	197	GND	GND	277
64	GND	GND	134	198	GND	GND	278
65	GND	GND	135	199	GND	GND	279

PART_NUMBER=339M00112
BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

U_TAN_E
LBKA0QE1XR-481
SIP-1
SYM 4 OF 4

CRITICAL

280	GND	GND	323				
281	GND	GND	324				
282	GND	GND	325				
283	GND	GND	326				
284	GND	GND	327				
285	GND	GND	328				
286	GND	GND	329				
287	GND	GND	338				
288	GND	GND	339				
289	GND	GND	348				
290	GND	GND	349				
291	GND	GND	350				
292	GND	GND	351				
293	GND	GND	352				
294	GND	GND	353				
295	GND	GND	354				
296	GND	GND	355				
297	GND	GND	356				
299	GND	GND	357				
300	GND	GND	359				
301	GND	GND	360				
302	GND	GND	361				
303	GND	GND	362				
304	GND	GND	363				
305	GND	GND	364				
306	GND	GND	365				
307	GND	GND	366				
308	GND	GND	367				
309	GND	GND	368				
310	GND	GND	369				
311	GND	GND	370				
312	GND	GND	371				
313	GND	GND	372				
314	GND	GND	374				
315	GND	GND	381				
316	GND	GND	383				
317	GND	GND	384				
318	GND	GND	385				
320	GND	GND	387				
321	GND	GND	388				
322	GND						

SIDE FIRE

PP_VDD_MAIN — FL5911_E 155S00373 FERR-33-OHM-25%-3.5A 0402 — PP_VBAT_FEZ

C5911_E 131S00303 100PF 5% 16V NP0-C0G 01005-1 — ROOM=MMW_SIP — BOMOPTION=RF_SKU:NAMM

C5912_E 220PF 5% 25V C0G 01005 — ROOM=MMW_SIP — NOSTUFF

BOMOPTION=RF_SKU:NAMM
ROOM=MMW_SIP

J_FEZ_E
SMT-FLEX-FEZ-3L-X1804
SMT-PAD

1	GND0	13	VBAT0
2	GND1	14	GND8
3	GND2	15	GND9
4	PON	16	GND10
5	GND3	17	VBAT1
6	IFV	18	GND11
7	GND4	19	IFH
8	1P85V	20	GND12
9	GND5	21	VBAT2
10	GND6	22	GND13
11	GND7	23	GND14
12	VBAT0	24	GND15

0R HOLDERS

50_MMW_SMR526_IFV2
50_MMW_SMR526_IFH3

PP_1V8_SMPS4 — FL5921_E 155S00402 FERR-330HM-25%-1.5A 0201 — 1.85V PP_1V85_FEZ

C5921_E 131S00385 68PF 5% 16V NP0/C0G 01005 — ROOM=MMW_SIP — BOMOPTION=RF_SKU:NAMM

C5922_E 220PF 5% 25V C0G 01005 — ROOM=MMW_SIP — NOSTUFF

SMR_TO_FEZ_PON — FL5931_E 0.00 1/32W 01005 — V_PON_FEZ — BOMOPTION=RF_SKU:NAMM

R5931_E 117S0158 100K 5% 1/32W MF 01005 — BOMOPTION=RF_SKU:NAMM — ROOM=MMW_SIP

50_MMW_SMR526_IFH3 NET CONNECTS TO 50_IF1_H AND
50_MMW_SMR526_IFV2 NET CONNECTS TO 50_IF2_V IN FEZ FLEX

SAISS FLEX SHOULD BE ASSEMBLED WITH APN:632-03619

SYNC_DATE=08/01/2019

PAGE TITLE: TANGIER SIP

DRAWING NUMBER: 051-05263
SIZE: D
REVISION: 9.0.0
BRANCH: 1
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BG1 ARRAY

PART_NUMBER=339M00116
BOMOPTION=RF_SKU:NAMM
ROOM=BG1

U_BG1_E
MWNP01SEMA01
LGA
SYM 1 OF 3
CRITICAL

34	50_MMW_SMR525_S6L_HPOL	244	50_LB1_H	50_HB1_H	235	50_MMW_SMR525_S6H_HPOL	34
34	50_MMW_SMR525_S14L_VPOL	236	50_LB1_V	50_HB1_V	243	50_MMW_SMR525_S14H_VPOL	34
34	50_MMW_SMR525_S1L_HPOL	309	50_LB2_H	50_HB2_H	298	50_MMW_SMR525_S1H_HPOL	34
34	50_MMW_SMR525_S9L_VPOL	299	50_LB2_V	50_HB2_V	307	50_MMW_SMR525_S9H_VPOL	34
34	50_MMW_SMR525_S5L_HPOL	278	50_LB3_H	50_HB3_H	266	50_MMW_SMR525_S5H_HPOL	34
34	50_MMW_SMR525_S13L_VPOL	267	50_LB3_V	50_HB3_V	277	50_MMW_SMR525_S13H_VPOL	34
34	50_MMW_SMR525_S2L_HPOL	338	50_LB4_H	50_HB4_H	328	50_MMW_SMR525_S2H_HPOL	34
34	50_MMW_SMR525_S10L_VPOL	300	50_LB4_V	50_HB4_V	308	50_MMW_SMR525_S10H_VPOL	34

PART_NUMBER=339M00116
BOMOPTION=RF_SKU:NAMM
ROOM=BG1

U_BG1_E
MWNP01SEMA01
LGA
SYM 2 OF 3
CRITICAL

1	GND	GND	97
2	GND	GND	98
3	GND	GND	99
4	GND	GND	100
5	GND	GND	101
6	GND	GND	102
7	GND	GND	103
8	GND	GND	104
9	GND	GND	105
10	GND	GND	106
11	GND	GND	107
12	GND	GND	108
13	GND	GND	109
14	GND	GND	110
15	GND	GND	111
16	GND	GND	112
17	GND	GND	113
18	GND	GND	114
19	GND	GND	115
20	GND	GND	116
21	GND	GND	117
22	GND	GND	118
23	GND	GND	119
24	GND	GND	120
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26	GND	GND	122
27	GND	GND	123
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33	GND	GND	129
34	GND	GND	130
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36	GND	GND	132
37	GND	GND	133
38	GND	GND	134
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44	GND	GND	140
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46	GND	GND	142
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52	GND	GND	148
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54	GND	GND	150
55	GND	GND	151
56	GND	GND	152
57	GND	GND	153
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63	GND	GND	159
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66	GND	GND	162
67	GND	GND	163
68	GND	GND	164
69	GND	GND	165
70	GND	GND	166
71	GND	GND	167
72	GND	GND	168
73	GND	GND	169
74	GND	GND	170
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81	GND	GND	177
82	GND	GND	178
83	GND	GND	179
84	GND	GND	180
85	GND	GND	181
86	GND	GND	182
87	GND	GND	183
88	GND	GND	184
89	GND	GND	185
90	GND	GND	186
91	GND	GND	187
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96	GND	GND	192

PART_NUMBER=339M00116
BOMOPTION=RF_SKU:NAMM
ROOM=BG1

U_BG1_E
MWNP01SEMA01
LGA
SYM 3 OF 3
CRITICAL

193	GND	GND	293
194	GND	GND	294
195	GND	GND	295
196	GND	GND	296
197	GND	GND	297
198	GND	GND	301
199	GND	GND	302
200	GND	GND	303
201	GND	GND	304
202	GND	GND	305
203	GND	GND	306
204	GND	GND	310
205	GND	GND	311
206	GND	GND	312
207	GND	GND	313
208	GND	GND	314
209	GND	GND	315
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211	GND	GND	317
212	GND	GND	318
213	GND	GND	319
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217	GND	GND	323
218	GND	GND	324
219	GND	GND	325
220	GND	GND	326
221	GND	GND	327
222	GND	GND	329
223	GND	GND	330
224	GND	GND	331
225	GND	GND	332
226	GND	GND	333
227	GND	GND	334
228	GND	GND	335
229	GND	GND	336
230	GND	GND	337
231	GND	GND	339
232	GND	GND	340
233	GND	GND	341
234	GND	GND	342
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264	GND	GND	368
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268	GND	GND	370
269	GND	GND	371
270	GND	GND	372
271	GND	GND	373
272	GND	GND	374
273	GND	GND	375
274	GND	GND	376
275	GND		
276	GND		
279	GND		
280	GND		
281	GND		
282	GND		
283	GND		
284	GND		
285	GND		
286	GND		
287	GND		
288	GND		
289	GND		
290	GND		
291	GND		
292	GND		

SYNC_DATE=08/01/2019
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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0024124377	ENGINEERING RELEASED	2020-07-01

HIER_NFC

LAST_MODIFICATION=Wed Jul 1 15:22:42 2020

PRIMARY CHIP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00629	338S00630	?	NFC_P	SN210V PROD VS DEV

D54 PRIMARY MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00026	2	CAP,CER,C0G,820PF,2%25V,0201	C7510_S,C7513_S	?
131S00016	2	CAP,CER,C0G,470PF,2%25V,0201	C7550_S,C7551_S	?
152S01116	2	IND,82NH,2.5%,0.55A,0402	L7500_S,L7501_S	?
131S00025	2	CAP,CER,C0G,1000PF,2%,25V,0201	C7514_S,C7542_S	?
131S0825	2	CAP,CER,C0G,560PF,2%,25V,0201	C7512_S,C7541_S	?
131S00025	1	CAP,CER,C0G,1000PF,2%,50V,0201	C7546_S	?
131S00209	1	CAP,CER,C0G,68PF,2%,25V,0201	C7547_S	?
131S00016	1	CAP,CER,C0G,470PF,2%,50V,0201	C7548_S	?
131S0731	1	CAP,CER,C0G,100PF,2%,25V,0201	C7558_S	NOSTUFF

XTAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00077	197S00206	?	Y7500_S	XTAL,27P12 MHZ
197S00076	197S00206	?	Y7500_S	XTAL,27P12 MHZ

2 IN PP_VDD_MAIN VOLTAGE=3.8
2 IN PP1V2_NFC_S2 VOLTAGE=1.2
2 IN PP1V8_S4 VOLTAGE=1.8V
2 IN PP1V2_S4 VOLTAGE=1.2

2 IO I2C_R1_TO_NFC_SCL
2 IO I2C_R1_TO_NFC_SDA
2 IO I2C_BT_TO_NFC_SCL
2 IO I2C_BT_TO_NFC_SDA

2 IO SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
2 IO SPMI0_EVENTS_AOP_BI_NFC_P_DATA_R

2 IN GPIO_SEQ_PMU_TO_NFC_EN

2 IN NFC_P_THERMISTOR_UAT4
2 IN NTC_STOCKHOLM

2 OUT GPIO_SE_TO_BT_PKT_RDY
2 OUT GPIO_NFC_TO_ARCAMP_RESET_L
2 OUT GPIO_NFC_TO_ARCAMP_TRIG
2 IO NFC_P_ANT_POS
2 IO NFC_P_ANT_NEG
IO 2 NFC_P_TEST_OUT

2 IN GPIO_NFC_F_NFC_P_SYNC2
2 IN GPIO_NFC_F_NFC_P_SYNC1

2 IN IO_TOUCH_TO_MANY_SCAN_ACTIVE_U

NFC: TABLE OF CONTENTS

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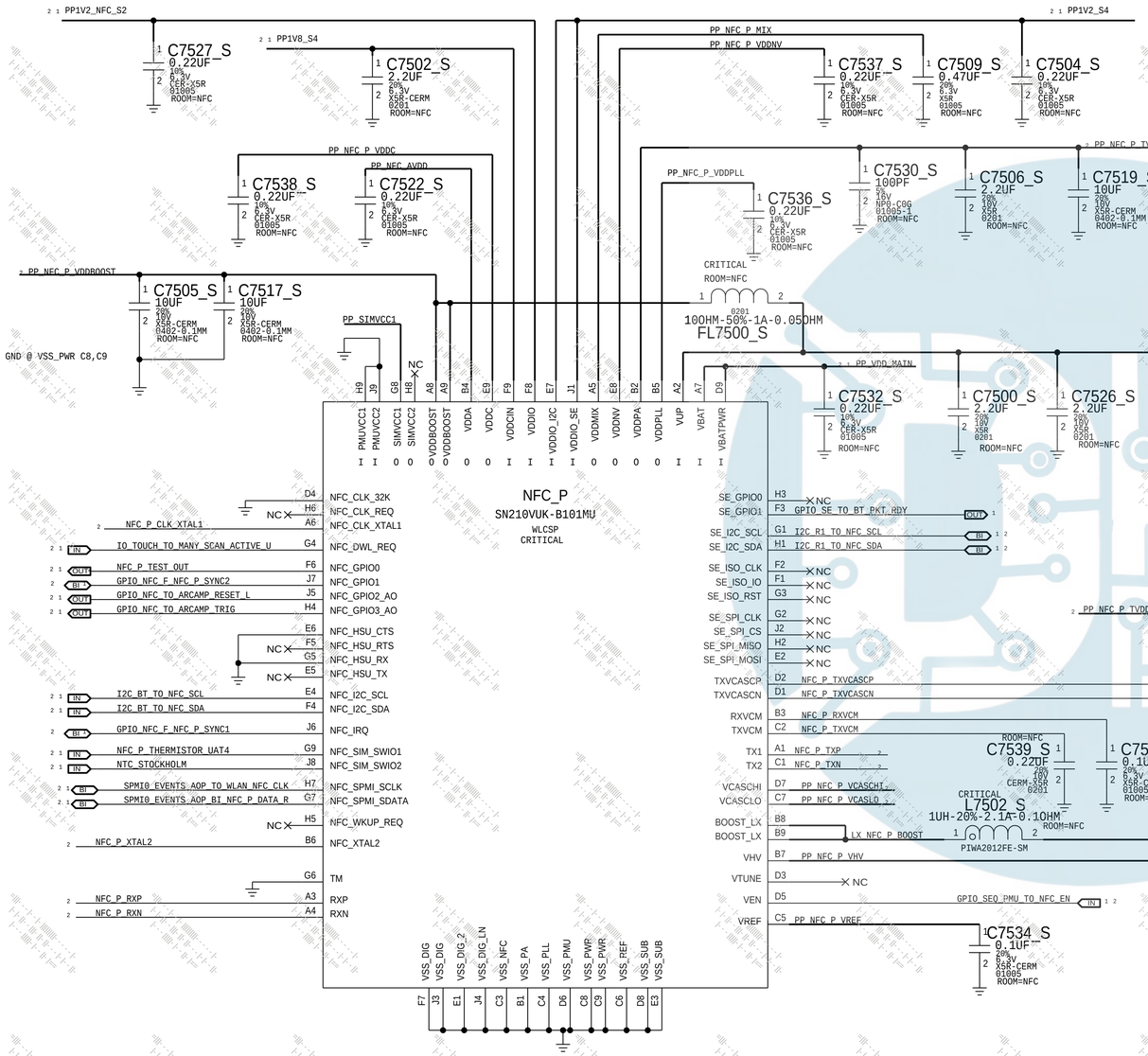
STOCKHOLM

PRIMARY NFC CONTROLLER



PAGE TITLE	NFC_P
DRAWING NUMBER	051-05263
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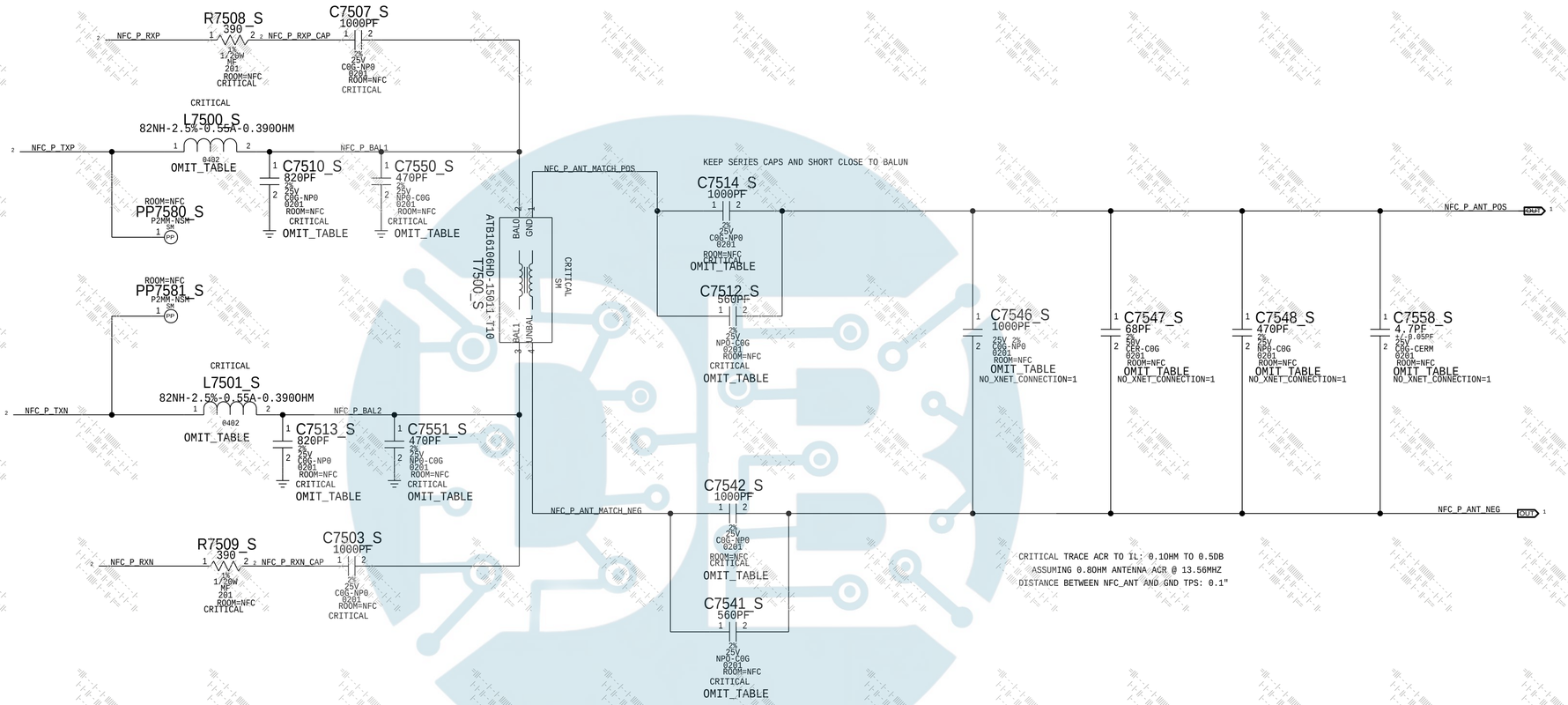
PRIMARY NFC FRONT END



PAGE TITLE
NFC_P_FE

DRAWING NUMBER 051-05263
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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	0024124377	ENGINEERING RELEASED	2020-07-01

D54 HIER_WIFI_BOT

LAST_MODIFICATION=Wed Jul 1 15:22:37 2020

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
D52	WIFI_MASTER	2	0.21.0	S	2019_12_09_16:30:41

SYMBOL IO PORTS

POWER

MAKE_BASE=TRUE

- PP_VDD_MAIN — VOLTAGE=3.8 — PP_VDD_MAIN
- PP_VDD_MAIN — VOLTAGE=3.8
- PP_VDD_MAIN — VOLTAGE=3.8
- PP1V8_S2 — VOLTAGE=1.8V
- PP1V8_S4 — VOLTAGE=1.8V
- PP1V2_S4 — VOLTAGE=1.2

ANTENNA

- 50_TRX_WLAN_G_BT_ANT4_NPLXR
- 50_TRX_WLAN_G_BT_ANT3_NPLXR

RFEM CONNECTIONS

RF
- 50_WLAN_A_C0_TXRX_FEM_M
- 50_WLAN_A_C1_TXRX_FEM_M

ANALOG
- ANALOG_UAT_5G_FEM_TO_WLAN_PDTS
- ANALOG_LAT_5G_FEM_TO_WLAN_PDTS

GPIO
- GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN
- GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN

RFFE
- RFFE_WLAN_TO_UAT_5G_FEM_RST_L
- RFFE_WLAN_TO_LAT_5G_FEM_RST_L
- SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK
- SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA
- SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK
- SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA

CELLULAR CONNECTIONS

- UART_BB_TO_WLAN_TX
- UART_BB_TO_WLAN_RX

AP CONNECTIONS

- GPIO_AP_FROM_WLAN_TIME_SYNC
- GPIO_ISP_RCAM_TO_STROBE_KRAKEN_WLAN_FLASH_TRIG
- GPIO_AP_FROM_BT_AUDIO_SYNC

PCIE
- PCIE_GP1_AP_TO_WLAN_PERST_L
- PCIE_GP1_AP_BI_WLAN_CLKREQ_L
- 90_PCIE_GP1_AP_TO_WLAN_TX_P
- 90_PCIE_GP1_AP_TO_WLAN_TX_N
- 90_PCIE_GP1_AP_FROM_WLAN_RX_P
- 90_PCIE_GP1_AP_FROM_WLAN_RX_N
- 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P
- 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N

AOP CONNECTIONS

- SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK
- SPMI0_EVENTS_AOP_BI_WLAN_DATA_R
- GPIO_AOP_TO_WLAN_CONTEXT_A
- GPIO_AOP_TO_WLAN_CONTEXT_B

PMU CONNECTIONS

- GPIO_S4_PMU_TO_WLAN_REG_ON
- GPIO_PMU_FROM_WLAN_HOST_WAKE
- CLK_GPIO_S4_PMU_TO_WLAN_R1_32K

SE CONNECTIONS

- I2C_BT_TO_NFC_SCL
- I2C_BT_TO_NFC_SDA
- GPIO_SE_TO_BT_PKT_RDY

R1 CONNECTIONS

- GPIO_R1_TO_WLAN_COEX
- GPIO_WLAN_TO_R1_COEX
- IO_BT_TO_R1_TIME_SYNC
- IO_BT_TO_R1_WAKE

SPKR CONNECTIONS

- GPIO_BT_TO_BOT_SPKR_TRIG

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WIFI/BT THELONIOUS

5G INTERSTATE BPFS

R201_W 0.8NH-+/-0.05NH-0.9A — 50_WLAN_A_C0_TXRX_FEM_M — 01005 — 50_WLAN_A_C0_TXRX_BPF
C203_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN
C204_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN
FL_ISG_U_W ACPF-7350-AP1 LGA CRITICAL — TX/RX, ANT, GND — ROOM=WLAN
50_WLAN_A_C0_TXRX_BPF_R — R233_W 0.0D 5% 1/32W MF 01005 ROOM=WLAN — 50_WLAN_A_C0_TXRX
C201_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN
C202_W 0.2PF +/-0.05PF 16V CERM 01005

R202_W 0.6NH-+/-0.05NH-0.95A — 50_WLAN_A_C1_TXRX_FEM_M — 01005 — 50_WLAN_A_C1_TXRX_BPF
C205_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN
C206_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN
FL_ISG_L_W ACPF-7350-AP1 LGA CRITICAL — TX/RX, ANT, GND — ROOM=WLAN
50_WLAN_A_C1_TXRX_BPF_R — R235_W 0.6NH-+/-0.05NH-0.95A 01005 — 50_WLAN_A_C1_TXRX
C228_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN
C241_W 0.2PF +/-0.05PF 16V CERM 01005

50_WLAN_G_C0_TXRX_FEM_M — R237_W 0.0D 5% 1/32W MF 01005 ROOM=WLAN — 50_WLAN_G_C0_TXRX_R
C230_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN
C243_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN

50_WLAN_G_C1_TXRX_FEM_M — R238_W 0.0D 5% 1/32W MF 01005 ROOM=WLAN — 50_WLAN_G_C1_TXRX_R
C231_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN
C244_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF ROOM=WLAN

PP1V2_S4 — VOLTAGE=1.2
C250_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN
PP1V8_S4
C252_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN
C257_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN
PP_VDD_MAIN — VOLTAGE=3.8
C232_W 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=WLAN
C233_W 4.7PF +/-0.1PF 16V NP0_C0G 01005 ROOM=WLAN
PP_VDD_MAIN
C245_W 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=WLAN
C247_W 2.2UF 20% 6.3V X5R-CERM 0201
C246_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN

L253_W 2.2UH-20%-1.1A-0.293OHM 0603 ROOM=WLAN — PP1V02_ABUCK_L — VOLTAGE=1.02
C254_W 7.5UF 20% 4V CERM 0402 ROOM=WLAN
PP1V02_ABUCK — VOLTAGE=1.02
L255_W 2.2UH-20%-1.1A-0.293OHM 0603 ROOM=WLAN — CSR_VLX — PP0V72_CBUCK_L — VOLTAGE=0.72
C256_W 7.5UF 20% 4V CERM 0402 ROOM=WLAN
PP0V72_CBUCK — VOLTAGE=0.72
PP3V3_BTLDO — VOLTAGE=3.3
C270_W 27PF 5% 16V NP0_C0G 01005-1 ROOM=WLAN

ROOM=WLAN

VBAT	169		
VBAT	183		
VBAT_RF	205		
VDDIO_RF	5		
VDDIO1P2	204		
VDDIO1P8	6		
ASR_VLX	186		
ASR_VLX	200		
ABUCK_1P02	202		
ABUCK_WL2G_BT_1P02	206		
ABUCK_WL2G_BT_1P02	207		
ABUCK_WL5G_1P02	179		
ABUCK_WL5G_1P02	165		
CSR_VLX	194		
CSR_VLX	198		
CBUCK_0P72	3		
CBUCK_0P72	17		
CBUCK_0P72	141		
CBUCK_0P72	194		
BTLDO3V3			

ANALOG_UAT_5G_FEM_TO_WLAN_PDTS — 28 5G_C0_ANT — 56 5GTSSI_C0 — 12 5G_C1_ANT — 10 5GTSSI_C1
ANALOG_UAT_2G_FEM_TO_WLAN_PDTS — 196 2G_C0_ANT — 168 2GTSSI_C0 — 112 2G_C1_ANT — 140 2GTSSI_C1
ANALOG_LAT_2G_FEM_TO_WLAN_PDTS

GPIO_WLAN_TO_UAT_5G_FEM_LNA_BYP_EN — 61 LNA_EN_5GC0
GPIO_WLAN_TO_LAT_5G_FEM_LNA_BYP_EN — 46 LNA_EN_5GC1
GPIO_WLAN_TO_UAT_2G_FEM_LNA_BYP_EN — 62 LNA_EN_2GC0
GPIO_WLAN_TO_LAT_2G_FEM_LNA_BYP_EN — 20 LNA_EN_2GC1

RFFE_WLAN_TO_UAT_5G_FEM_RST_L — 48 5G_C0_RESET
RFFE_WLAN_TO_UAT_2G_FEM_RST_L — 33 2G_C0_RESET
SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK — 50 C0_MIPI_CLK
SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA — 49 C0_MIPI_DATA
RFFE_WLAN_TO_LAT_5G_FEM_RST_L — 19 5G_C1_RESET
RFFE_WLAN_TO_LAT_2G_FEM_RST_L — 34 2G_C1_RESET
SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK — 36 C1_MIPI_CLK
SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA — 35 C1_MIPI_DATA

NC — 63 WL_GPIO_7/DAP_SEL

PLACE_SIDE=BOTTOM
SM PP207_W P2MM-NSM ROOM=WLAN OMIT — WL_GPIO_18 — 120 WL_GPIO_18
UART_BB_TO_WLAN_TX — 105 WLBT_SECI_IN
UART_BB_TO_WLAN_RX — 119 WLBT_SECI_OUT
SM PP242_W P2MM-NSM ROOM=WLAN OMIT — GPIO_AP_FROM_WLAN_TIME_SYNC — 147 WLAN_TIME_SYNC
NC — 130 LHL_GPIO2
NC — 157 SPMI_IDC_CLK
NC — 144 SPMI_IDC_DAT

PCIE_GP1_AP_TO_WLAN_PERST_L — 44 WLBT_WL_PCIE_PERST_L
C226_W 100PF 1% 16V NP0-C0G 01005-1 ROOM=WLAN NOSTUFF
PCIE_GP1_AP_BI_WLAN_CLKREQ_L — 86 WLBT_WL_PCIE_CLKREQ_L
90_PCIE_GP1_AP_TO_WLAN_TX_P — 29 90_WLBT_WL_PCIE_RD_P
90_PCIE_GP1_AP_TO_WLAN_TX_N — 15 90_WLBT_WL_PCIE_RD_N
90_PCIE_GP1_AP_FROM_WLAN_RX_P — 71 90_WLBT_WL_PCIE_TD_P
90_PCIE_GP1_AP_FROM_WLAN_RX_N — 57 90_WLBT_WL_PCIE_TD_N
90_PCIE_GP1_AP_TO_WLAN_REFCLK_P — 113 90_WLBT_WL_PCIE_REFCLK_P
90_PCIE_GP1_AP_TO_WLAN_REFCLK_N — 99 90_WLBT_WL_PCIE_REFCLK_N

SM PP243_W P2MM-NSM ROOM=WLAN OMIT — RF_SW_CTRL_3 — 47 RF_SW_CTRL_3

NC — 172 CLK_REQ

U_WLAN_W
THELONIOUS-U-ES4.3
LGA
2103-601901-80
SYM 1 OF 2
CRITICAL

WLBT_WL_FAST_UART_RX	104	NC	
WLBT_WL_FAST_UART_RTS_OUT	75	NC	
WLBT_WL_FAST_UART_CTS_IN	89	NC	
WLBT_WL_FAST_UART_TX	90	NC	
WLBT_WL_HOST_WAKE	91	GPIO_PMU_FROM_WLAN_HOST_WAKE	PP244_W SM P2MM-NSM OMIT ROOM=WLAN
WLBT_WL_REG_ON	174	GPIO_S4_PMU_TO_WLAN_REG_ON	PP206_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_TDI/CXT_A	74	GPIO_AOP_TO_WLAN_CONTEXT_A	PP201_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_TDO/CXT_B	60	GPIO_AOP_TO_WLAN_CONTEXT_B	PP202_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_TRST_L	64	JTAG_WLAN_TRST_L	PP203_W SM P2MM-NSM OMIT ROOM=WLAN
JTAG_SEL	171	JTAG_WLAN_SEL	PP232_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_SCT/SWD_CLK	103	JTAG_WLAN_TCK	PP204_W SM P2MM-NSM OMIT ROOM=WLAN
WLAN_TMS/SWD_DAT	78	JTAG_WLAN_TMS	PP205_W SM P2MM-NSM OMIT ROOM=WLAN
WL_GPIO_21/BT_OVER_UART	146	NC	
WLBT_BT_UART_RXD	177	NC	
WLBT_BT_UART_RTS_L	178	NC	
WLBT_BT_UART_CTS_L	176	NC	
WLBT_BT_UART_TXD	175	NC	
WLBT_BT_DEV_WAKE	189	GPIO_BT_TO_BOT_SPKR_TRIG	PP210_W SM P2MM-NSM OMIT ROOM=WLAN
WLBT_BT_REG_ON	173	NC	
1V2_WIFI_TO_SENSORA_COEX	116	NC	
1V2_BT_TO_SENSORA_COEX	134	NC	
1V8_WIFI_TO_SENSORA_COEX	77	NC	
1V8_BT_TO_SENSORA_COEX	76	NC	
GPIO_SENSORB_TO_BT_SYNC	161	GPIO_SE_TO_BT_PKT_RDY	PP211_W SM P2MM-NSM OMIT ROOM=WLAN
SENSORC_TO_WIFI_COEX	118	GPIO_R1_TO_WLAN_COEX	PP233_W SM P2MM-NSM OMIT ROOM=WLAN
WIFI_TO_SENSORC_COEX	117	GPIO_WLAN_TO_R1_COEX	PP234_W SM P2MM-NSM OMIT ROOM=WLAN
BT_TO_SENSORC_TIME_SYNC	160	TO_BT_TO_R1_TIME_SYNC	PP235_W SM P2MM-NSM OMIT ROOM=WLAN
BT_TO_SENSORC_WAKE	133	IO_BT_TO_R1_WAKE	PP212_W SM P2MM-NSM OMIT ROOM=WLAN
SOC_TO_BT_TIME_SYNC	162	GPIO_ISP_RCAM_TO_STROBE_KRAKEN	PP213_W SM P2MM-NSM OMIT ROOM=WLAN
BT_TO_AP_TIME_SYNC	191	GPIO_AP_FROM_BT_AUDIO_SYNC	PP236_W SM P2MM-NSM OMIT ROOM=WLAN
SE_I2C_CLK	158	I2C_BT_TO_NFC_SCL (CKPLUS_WAIVE=I2C_PULLUP)	
SE_I2C_DAT	159	I2C_BT_TO_NFC_SDA (CKPLUS_WAIVE=I2C_PULLUP)	
SPMI_HEB_CLK	132	SPMI0_EVENTS_AOP_TO_WLAN_NFC_CLK	PP214_W SM P2MM-NSM OMIT ROOM=WLAN
SPMI_HEB_DAT	131	SPMI0_EVENTS_AOP_BI_WLAN_DATA_R	PP215_W SM P2MM-NSM OMIT ROOM=WLAN
WLBT_CLK_32K	145	CLK_GPIO_S4_PMU_TO_WLAN_R1_32K	PP239_W SM P2MM-NSM OMIT ROOM=WLAN
TCXO_IN	8	NC	

U_WLAN_W
THELONIOUS-U-ES4.3
LGA
2103-601901-80
SYM 2 OF 2
CRITICAL

1	GND	GND	98
2	GND	GND	100
4	GND	GND	101
7	GND	GND	102
9	GND	GND	106
11	GND	GND	107
13	GND	GND	108
14	GND	GND	109
16	GND	GND	110
18	GND	GND	111
21	GND	GND	114
22	GND	GND	115
23	GND	GND	121
24	GND	GND	122
25	GND	GND	123
26	GND	GND	124
27	GND	GND	125
30	GND	GND	126
31	GND	GND	127
32	GND	GND	128
37	GND	GND	129
38	GND	GND	135
39	GND	GND	136
40	GND	GND	137
41	GND	GND	138
42	GND	GND	139
43	GND	GND	142
45	GND	GND	143
51	GND	GND	148
52	GND	GND	149
53	GND	GND	150
54	GND	GND	151
55	GND	GND	152
58	GND	GND	153
59	GND	GND	154
65	GND	GND	155
66	GND	GND	156
67	GND	GND	163
68	GND	GND	164
69	GND	GND	166
70	GND	GND	167
72	GND	GND	170
73	GND	GND	192
79	GND	GND	193
80	GND	GND	180
81	GND	GND	181
82	GND	GND	182
83	GND	GND	185
84	GND	GND	187
85	GND	GND	188
87	GND	GND	190
88	GND	GND	195
92	GND	GND	197
93	GND	GND	199
94	GND	GND	201
95	GND	GND	203
96	GND	GND	208
97	GND	GND	209
		GND	210

OMIT SM PP222_W P2MM-NSM ROOM=WLAN — PCIE_GP1_AP_TO_WLAN_PERST_L
OMIT SM PP223_W P2MM-NSM ROOM=WLAN — PCIE_GP1_AP_BI_WLAN_CLKREQ_L
OMIT SM PP224_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_TO_WLAN_TX_P
OMIT SM PP225_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_TO_WLAN_TX_N
OMIT SM PP226_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_FROM_WLAN_RX_P
OMIT SM PP227_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_FROM_WLAN_RX_N
OMIT SM PP228_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_TO_WLAN_REFCLK_P
OMIT SM PP229_W P2MM-NSM ROOM=WLAN — 90_PCIE_GP1_AP_TO_WLAN_REFCLK_N

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00773	339S00761	?	U_WLAN_W	BOMOPTION FOR STATS

SENSOR A = DOTARA
SENSOR B = SE
SENSOR C = R1

GPIO_PMU_FROM_WLAN_HOST_WAKE — R259_W 100K 5% 1/32W MF 01005 ROOM=WLAN
PP1V2_S4 — R257_W 10K 5% 1/32W MF 01005 ROOM=WLAN NOSTUFF
JTAG_WLAN_SEL
NOSTUFF= JTAG DISABLED

PAGE TITLE: THELONIOUS

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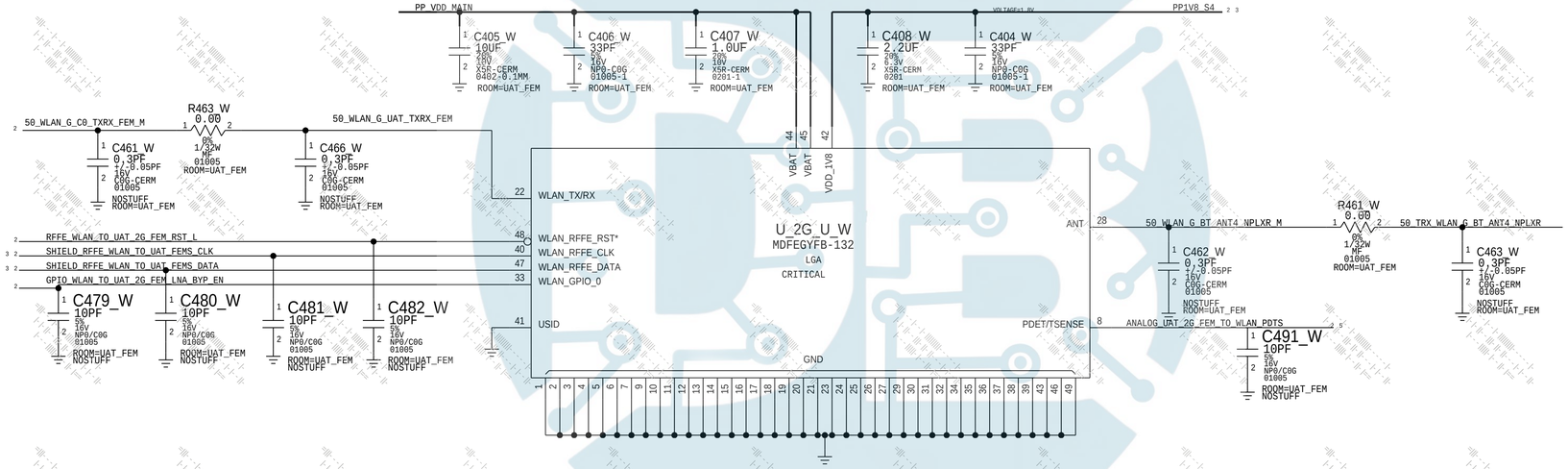
UAT 2.4 GHZ RFEM



OMIT_SM PP216_W P2MM-NSN ROOM=WLAN — PP — 1 — ANALOG_UAT_2G_FEM_TO_WLAN_PDTS

OMIT_SM PP250_W P2MM-NSN ROOM=UAT_FEM — PP — 1 — SHIELD_RFFE_WLAN_TO_UAT_FEMS_CLK

OMIT_SM PP251_W P2MM-NSN ROOM=UAT_FEM — PP — 1 — SHIELD_RFFE_WLAN_TO_UAT_FEMS_DATA

PAGE TITLE
2G4 rFEM (UAT)

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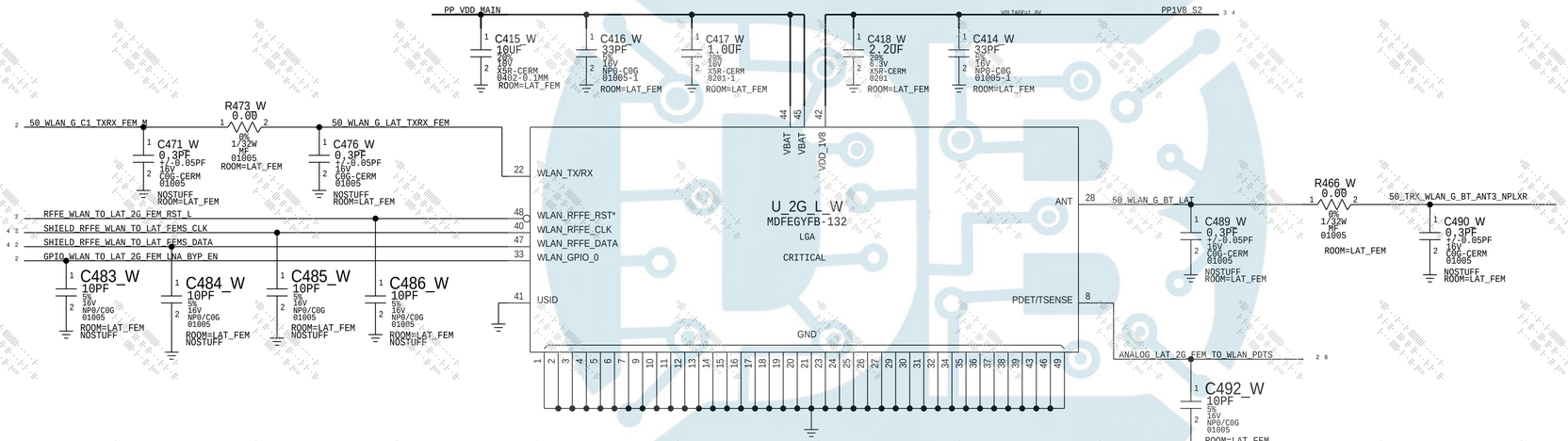
LAT 2.4 GHZ RFEM



OMIT_SM PP217_W P2MM-NSM ROOM=WLAN — ANALOG_LAT_2G_FEM_TO_WLAN_PDTS

OMIT_SM PP252_W P2MM-NSM ROOM=LAT_FEM — SHIELD_RFFE_WLAN_TO_LAT_FEMS_CLK

OMIT_SM PP253_W P2MM-NSM ROOM=LAT_FEM — SHIELD_RFFE_WLAN_TO_LAT_FEMS_DATA

PAGE TITLE	2G4 rFEM (LAT)
DRAWING NUMBER	051-05263
SIZE	D
REVISION	9.0.0
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