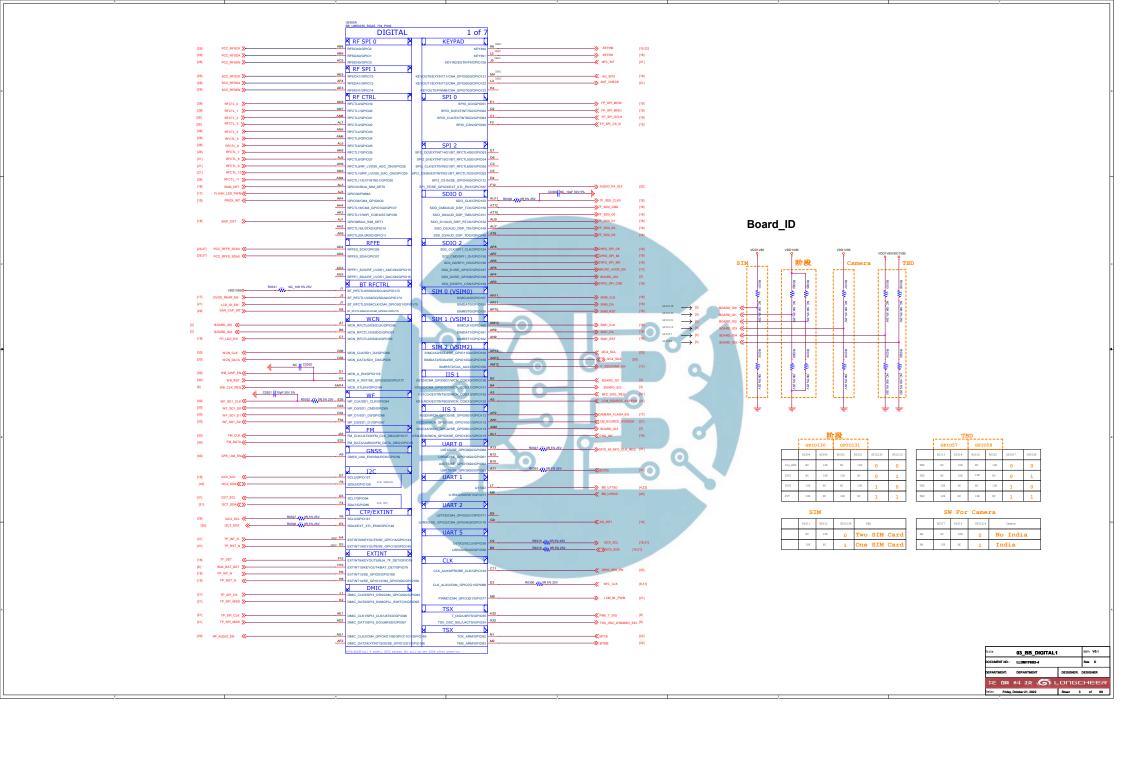
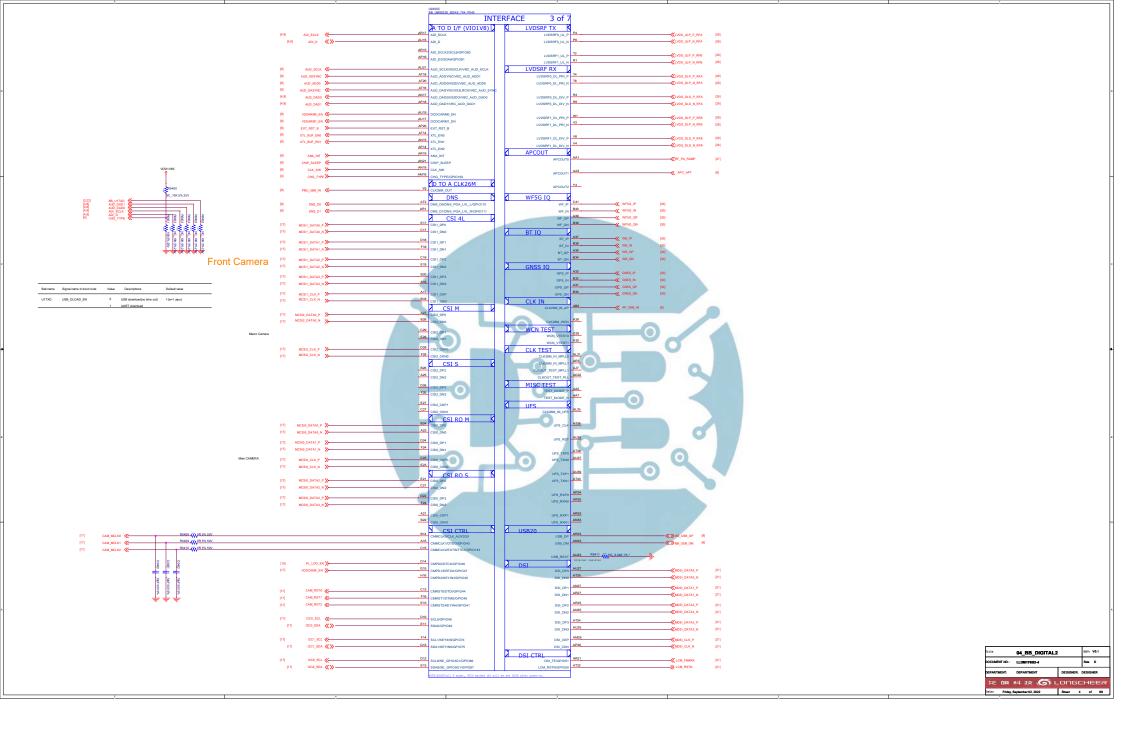
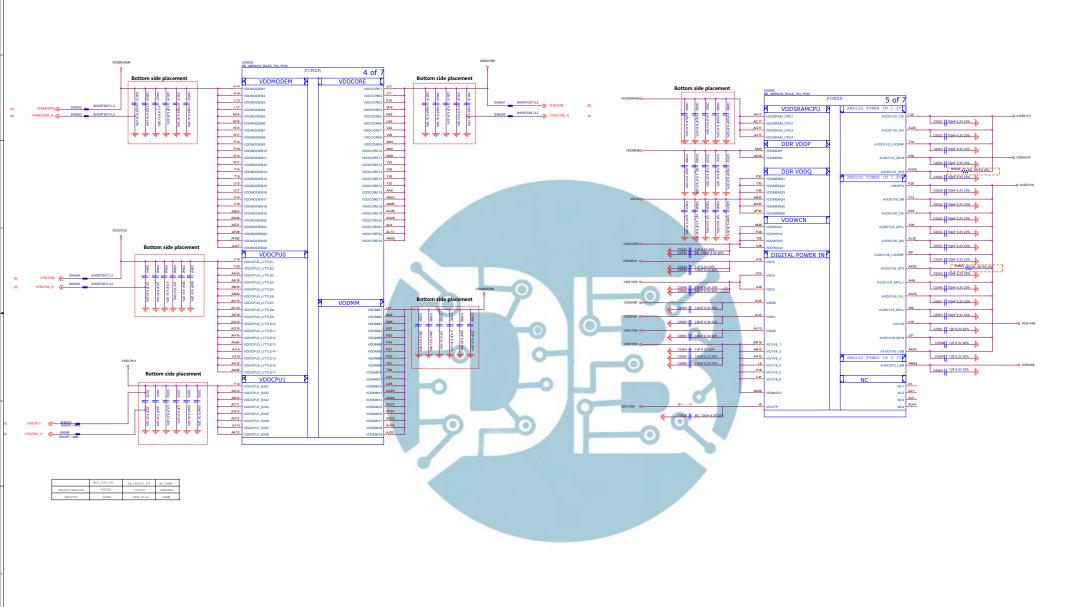


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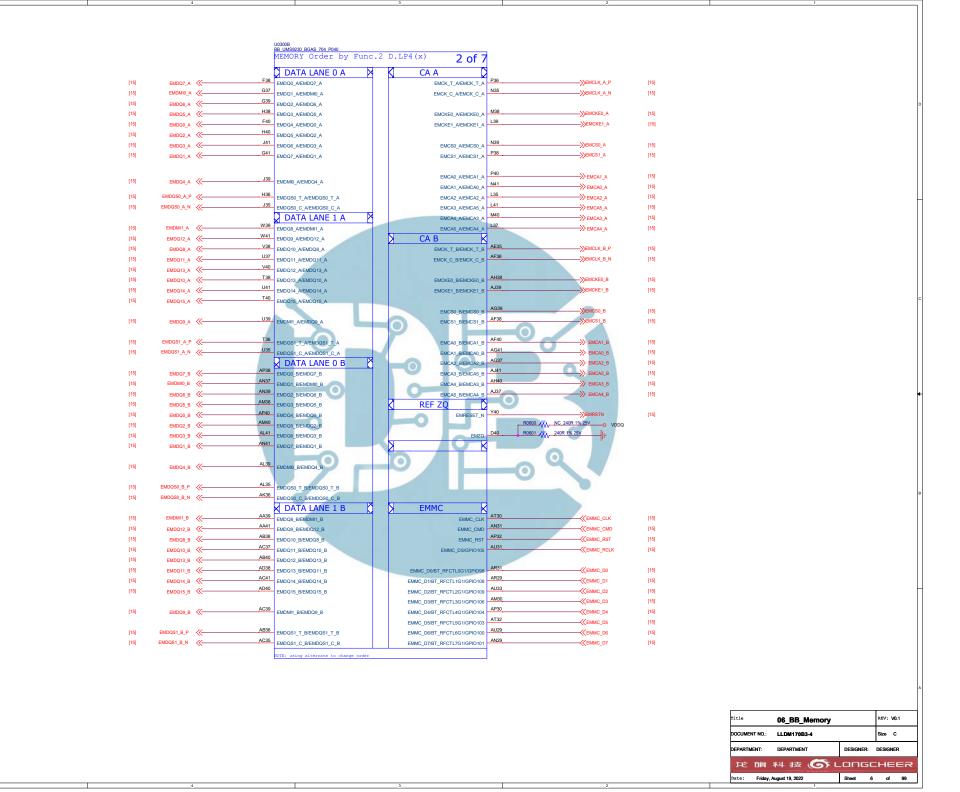
Date: Friday, August 19, 2022 Sheet 2 of 99

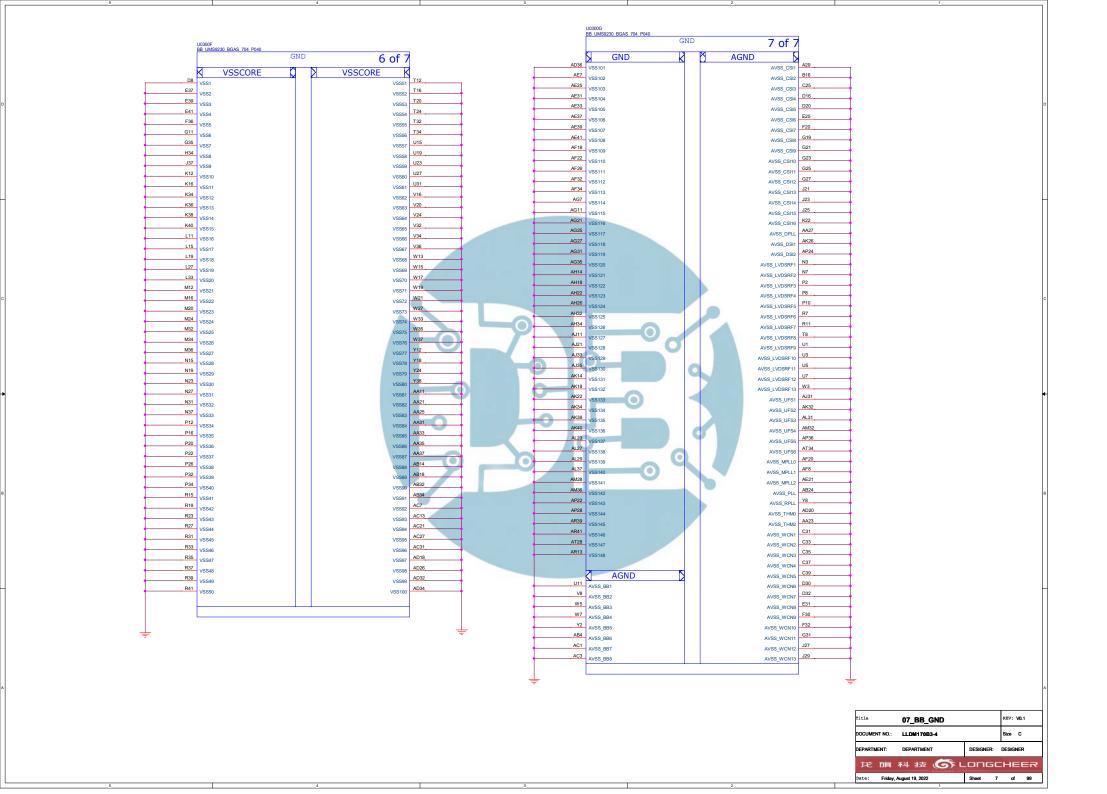






litle	05_BB_POWER		22V: V0.1
DOCUMENT NO.:	LLDM170B3-4		Size D
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Date: Friday	August 19, 2022	Sheet 5	of 99





## PMU ANALOG TSX (PMU) Only 1 ANALOG PMU CLK IN ( C PMI TREN IN AUDIO A TO D INTERFACE —≪≫ ADI D MAIN\_MC\_N >> C0820 100nF 6.3V 20% R0837 W 1K5% 25V K7 MIC1\_N AUD\_SCLK A11 ≪ AUD\_SCLK ALCONC\_P >> C5051 F00FF8.3V20% R0838 W TK35/25V H2 MIC2\_P ALDOMC\_N >> C0815 190+F 6.3V 20% R0839 W 1K 5% 25V G2 MIC2\_N AUD\_DADO B8 ✓ AUD DAD0 HEADMIC P J5 HEADMIC\_N HEADMIC\_N >> (20) HEADMIC\_IN\_DET >> R0802\_W\_1K.5%.25V J4 HEADMIC\_IN\_DET ANA INT R0835 Memory →>> ANA INT IN BOARD ID ADC1 ≪ HP\_DET >> CHIP\_SLEEP C11 PICC输入、CPI输出、高有效 H5 GND\_DET →>>> CLK\_32K 47K+/-1% L900R4x sHC9 DCDC\_CPU\_EN B10 ✓ VDDARMO EN HP R ≪ PTESTO E11 R0807 NC →>> DNS\_D0 M4 RCV N [20] A TO D INTERFACE CLK26M D3 SPK\_N DCXO LOWCUR **Board ID** DCXO\_LOWCUR U5 CLK C0805 2.2UF 6.3V 20% REF\_OUT0 U2 REF\_OUT1 V1 SHORTDOT-L4 R0814 W NC 0R 5% 29 CLASS G RTC C0808 470+F 6 3V 20% C0807 10UF 6.3V 20% VDORTO Wee 系统的32KHz 时钟,默认由26MHz 时钟在PMIC 内部分频产生 C0810 2 2UF 6.3V 20% L4 VDD\_CP C0812 | 4 7UF 8:3V 20% M1 | R0824 | C0813 | NC 4.7UF 8:3V 20% P1 | ADCIA T14 BOARD ID ADC1 C0814 2 2UF 6 3V 20% K1 CP\_CAP\_P —≪≫ usso\_hs\_DP [16.2 —≪≫ usso\_hs\_DM [16.2 Item Scenario Option1 Option2 RGB LED Qogir L6+UMP510G 0 0 SYSTEM Qogir L6+UMP510G+DCDC 0 1 T11 RGB\_IB1 SINK27mA T12 RGB\_IB2 SINK27mA 2 3 TSX Scenario Option3(264/524) Option4(TCXO\_MODE)Option5(TSX\_MODE) Option6(RTC\_MODE) 26M TCXO+32K Crystal C0818 100pF 50V 5%/10% 26M TSX+32K Crystal 26M TSX+32K-less from PMIC internal 0 0 1 1 R0831 W 0R 5% 25V B2 T\_DIG EXT XTL EN 1 A2 →>> BUA\_BAT\_DET 26M DCXO+32K-less from PMIC internal EXT\_XTL\_EN\_2 B1 ≪ XTL\_BUF\_EN1 26M DCXO+32K Crystal OPTION 2 VSS TSX A 1 V88\_T8X\_A\_1 V88\_T8X\_A\_2 V88\_T8X\_A\_3 V88\_T8X\_A\_4 Option1 Option2 OPTION\_4 R5 The DCDCGPU controlled by UMP510G ADI interface signal DCDC\_GPU\_EN. The typical application of DCDCGPU is Unisoc BB chip 0 OPTION\_6 U7 OPTION RTC MODE (8) T1 VSS\_TSX\_B The DCDCGPU default on and uncontrollable by UMP510G ADI interface signal DCDC\_GPU\_EN 1 The DCDCMEMQ controlled by UMP510G ADI interface signal DCDC\_GPU\_EN. The typical application of DCDCMEMQ is Unisoc BB chip

***** 08_UMP510G_Digital		REV: V0.1	
DOCUMENT NO: LLD	M170B3-4		Size D
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Date: Friday, August	19, 2022	Sheet 8	of 99

dual rail SRAM power supply.

## shipping mode [14] CHO | | 10 4 2 7 2 7 1 DCDCCGPU 0.8-14 2000mA 8.8 DN Remote DCDCCGPU 0.8-14 4000mA 0.8 DN Remote Supply power for digital CORE Supply power for GPU DCDCCPU 9.5-1.4 4000mA 0.8 DN Remote DCDCMDDEM 0.8-1.4 4000mA 0.8 DN Remote Supply power for CPU BAT DET Supply power for MODEM DGDCMEM 0.6-1.4 2000mA 1.15 DN Local Supply power for external DDR DCDCMEMO 0.4-1.4 1000mA 0.5 DN Level Supply power for external DDR & D die 10 1.2-2.2 1500mA 1.875 ON Local 0.6-1.95 1000mA 1.95 ON Local 0.6-1.4 2000mA 0.8 DN Local care. He are a respect DCDOWPA 0.4-3:6 1500mA NA OFF Local VEST\_PA 5.0-6.0 1000mA NA OFF Local CHIL THE 19 63V 201 CONT. BLAZE S NO. OF LAND UMP510G5 DCDC output Input Power Power Name Output Voltage (V) Output Current (mA) Default Voltage (V) DCDC CORE 0.3-1.3 ON 2000 8.0 DCDC GPU 0.3-1.3 4000 8.0 ON DCDC CPU 0.3-1.3 4000 8.0 ON

	DCDC SRAM	0.3-1.3		
	DCDC WPA	0.6-3.3		
UMP510G5 LDO output				

DCDC MODEM

DCDC MEM

DCDC MEMQ

DCDC GEN0

DCDC GEN1

0.3-1.3

0.25-1.25

0.25-1.25

1.8-2.5

0.6-1.5

0.3-1.3

4000

2000

1000

1500

1000

2000

1500

0.8

1.15

0.6

1.85

1.3

8.0

ON

ON

ON

ON

ON

ON

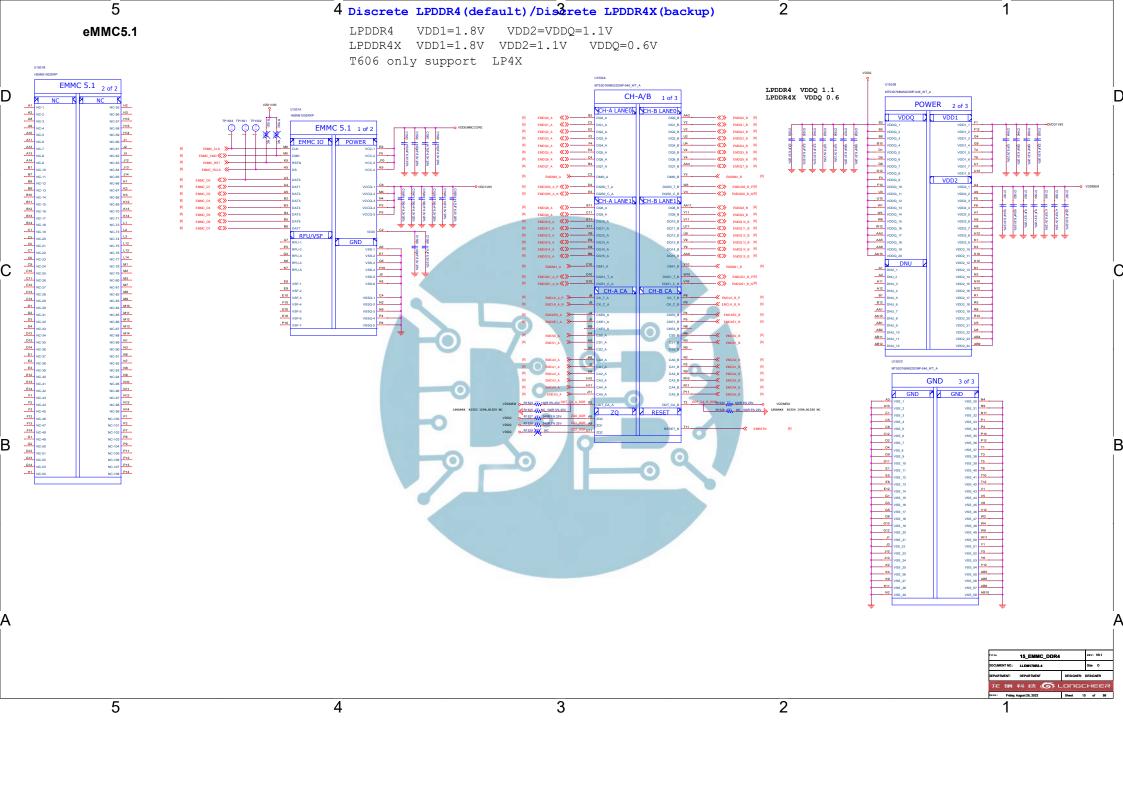
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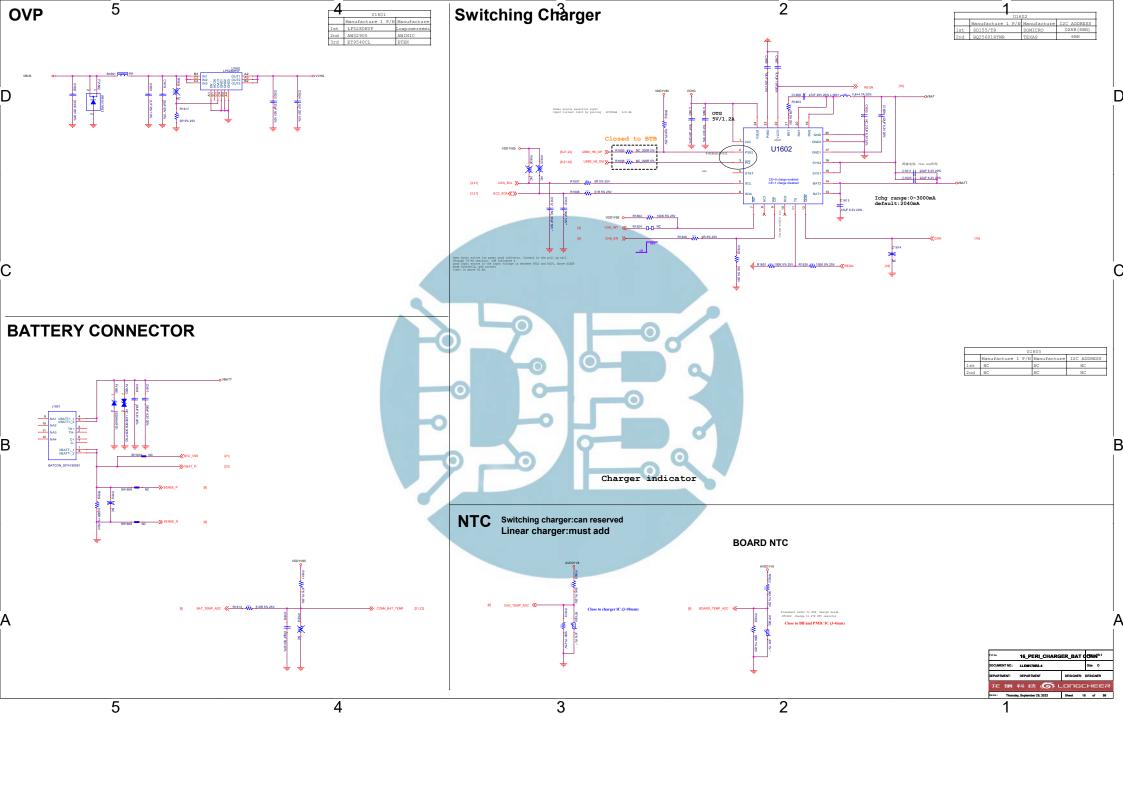
Input Power	Power Name	Output Voltage (V)	Output Current (mA)	Default Voltage (V)	Defaul
	VDD28	1.8-3.3	200	2.8	ON
	VDDCAMA0	1.8-3.3	200	2.8	OFF
	VDDCAMA1	1.8-3.3	200	2.8	OFF
	VDDCAMMOT	1.8-3.3	400	3	OFF
	VDD18_DCXO	1.8-3.3	50	1.8	ON
	VDDEMMCCORE	1.8-3.3	600	3	ON
	VDDSDCORE	1.8-3.3	800	3	ON
VBAT	VDDSDIO	1.8-3.3	200	3	ON
	VDDSIM0	1.8-3.3	60	3	OFF
	VDDSIM1	1.8-3.3	60	3	OFF
	VDDSIM2	1.8-3.3	60	3	OFF
	VDDUSB33	1.8-3.3	100	3.3	ON
	VDDWIFIPA	1.8-3.3	500	3.3	OFF
	VDDLDO0	1.8-3.3	50	2.8	OFF
	VDDLDO1	1.8-3.3	100	3.3	OFF
	VDDLDO2	1.8-3.3	200	3.3	OFF
	VDDCAMD0	1.0-1.25	400	1.1	OFF
GEN1	VDDCAMD1	1.0-1.25	200	1.1	OFF
GENT	VDDRF1V25	1.0-1.25	300	1.25	OFF
	AVDD12	1.0-1.25	150	1.2	ON
	AVDD18	1.2-1.8	200	1.8	ON
GEN0	VDDRF18	1.2-1.8	300	1.8	ON
	VDDCAMIO	1.2-1.8	100	1.8	OFF
GEN1	WCN	1.0-1.6	200	1	OFF

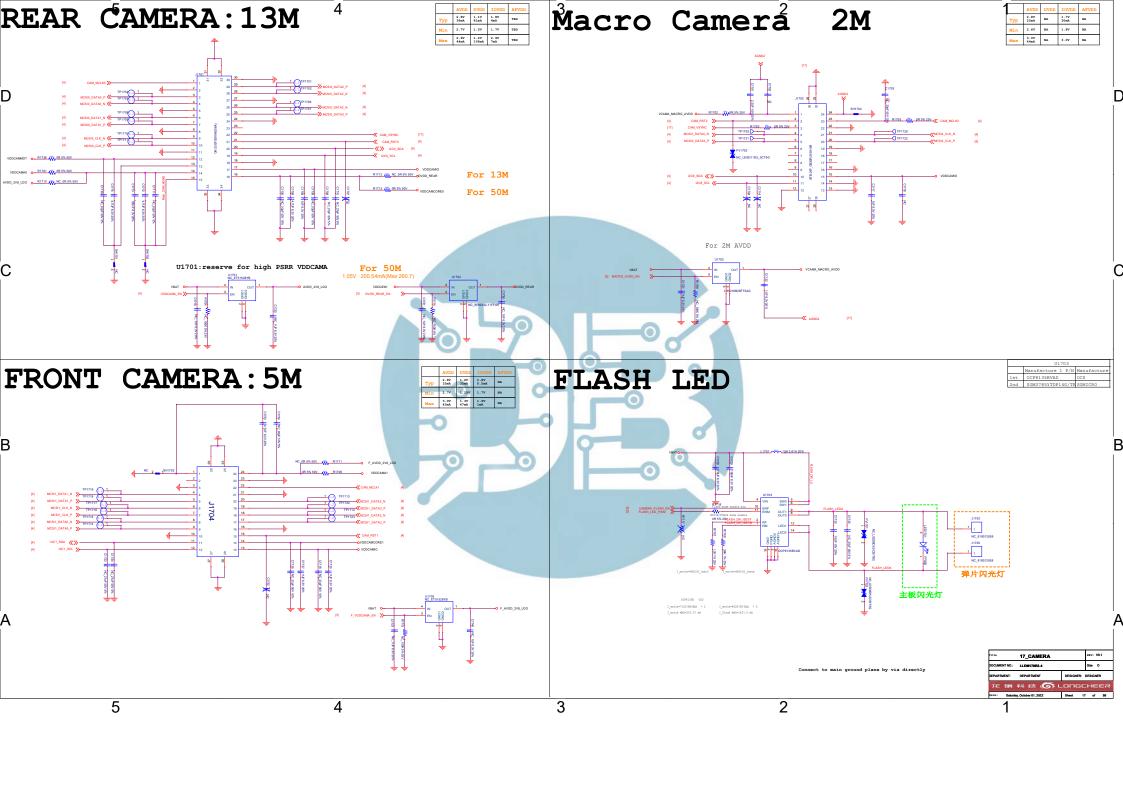
isla	09_UMP510G_P	OWER NO.1
DOCUMENT NO.	LLC0017003-4	No. 1
DEPARTMENT DEPARTMENT		DESCRIPTION DESIGNATE
212 DR	80 aw 65	LONGCHEER

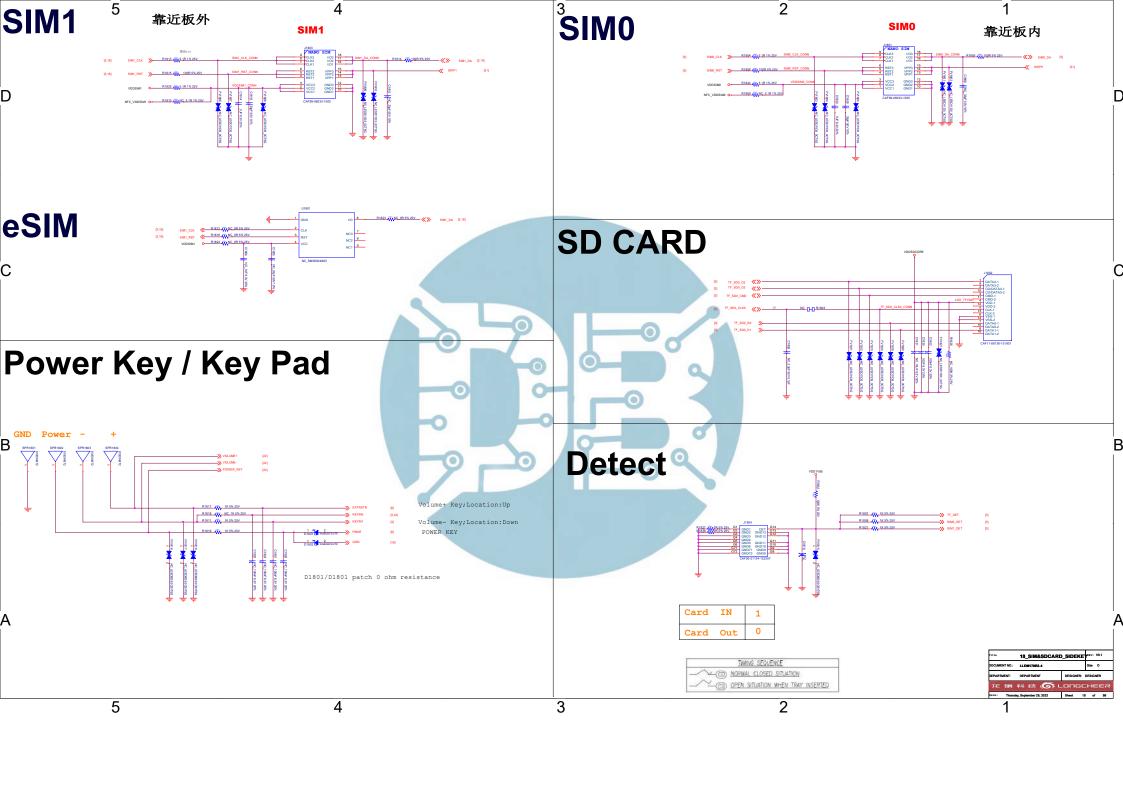
UMS9230	T606	不需要外部DCDC供电
UMS9230H	T612	VDD_CPU1使用PMIC DCDC_GPU供
UMS9230T	T616	需要外部DCDC供电

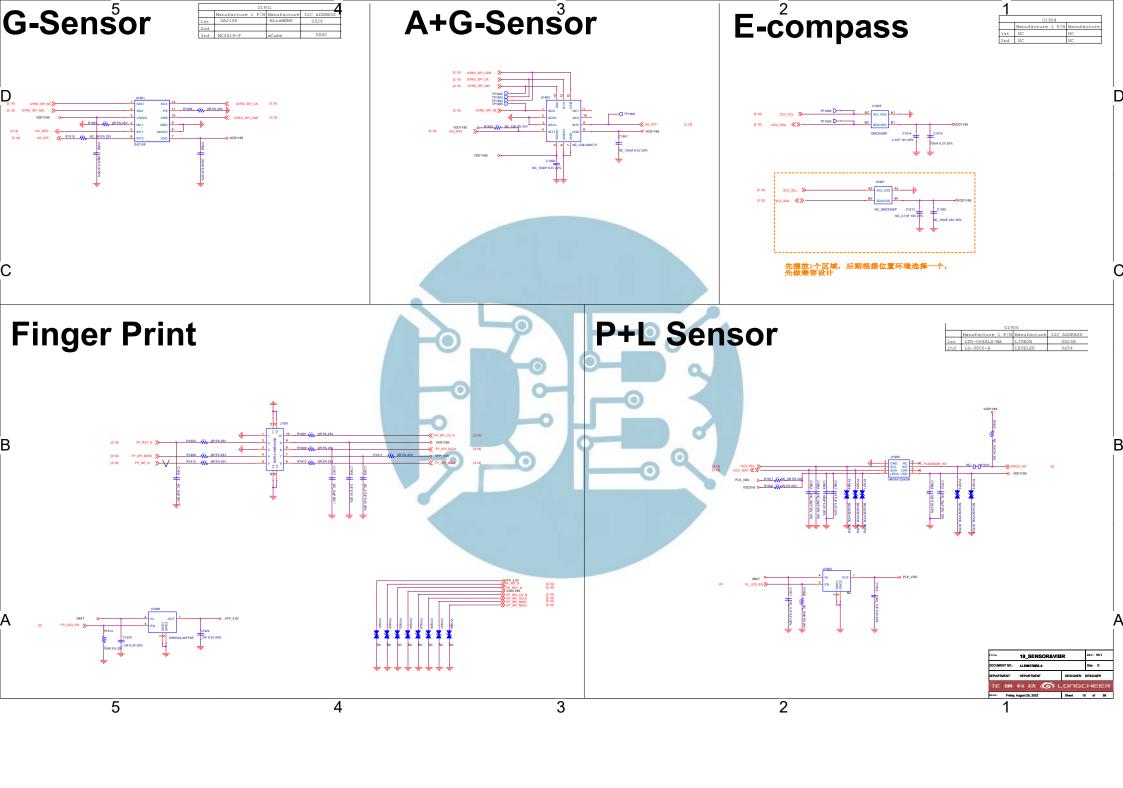
COOR | Day of July |

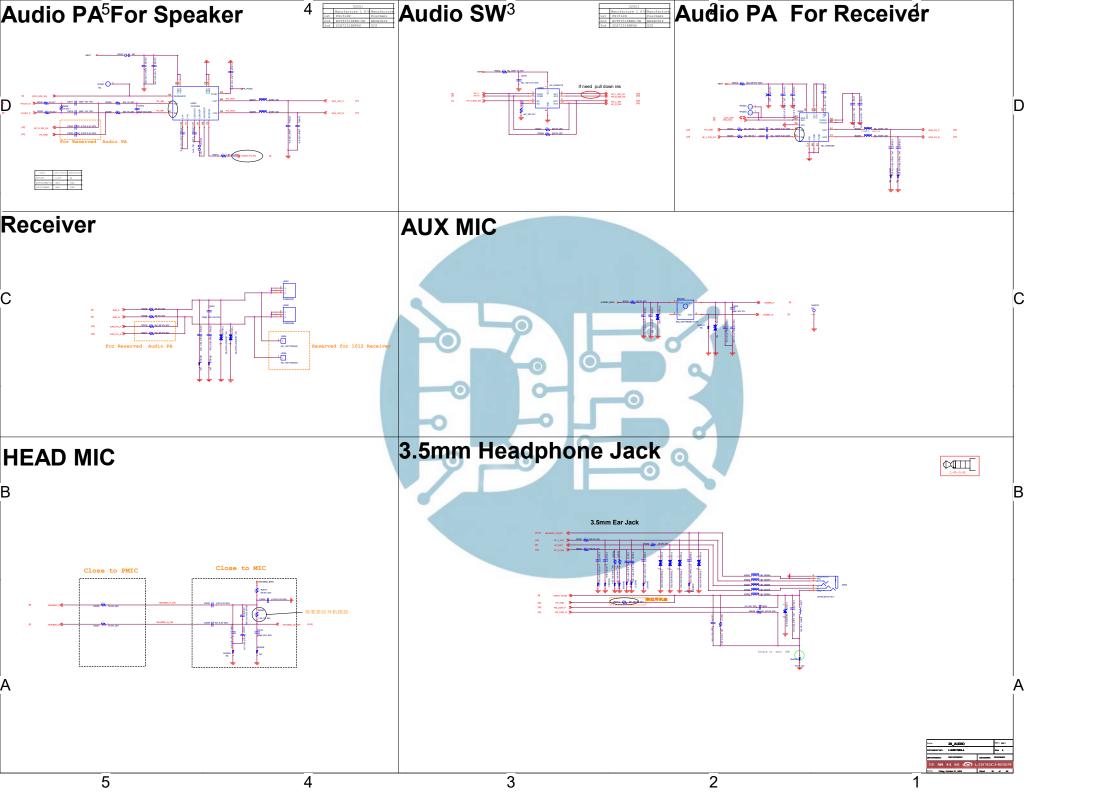


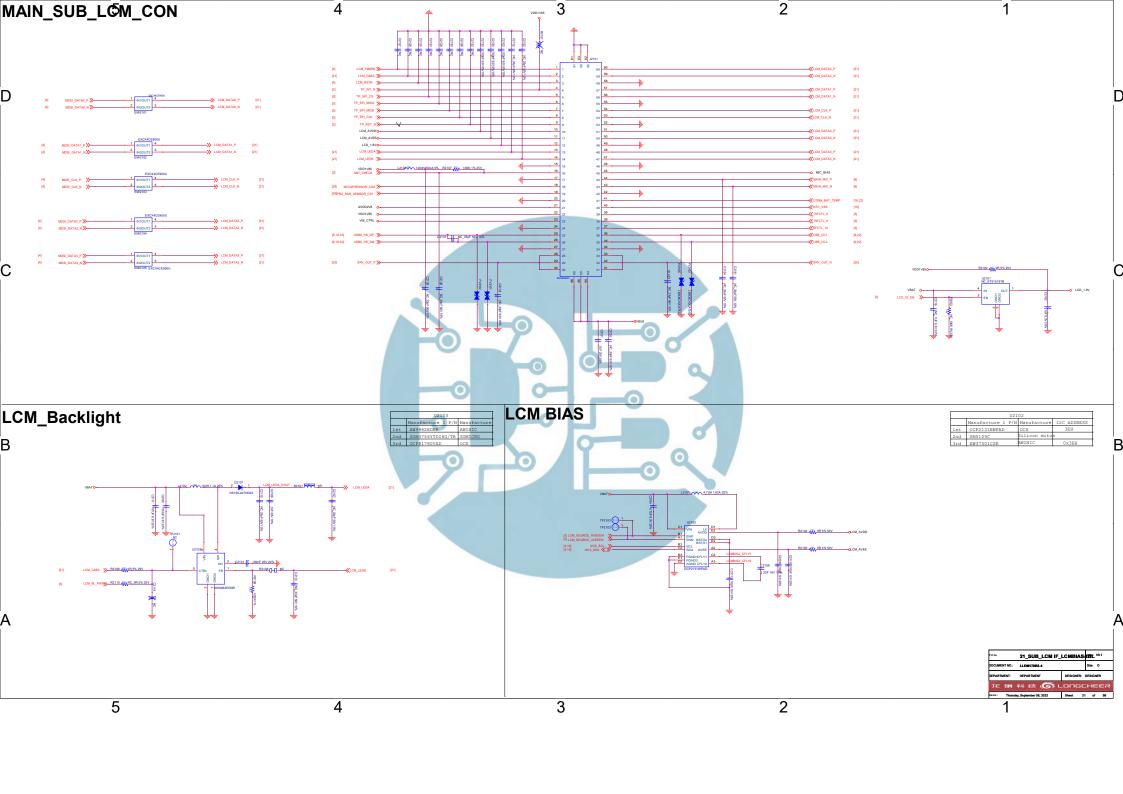


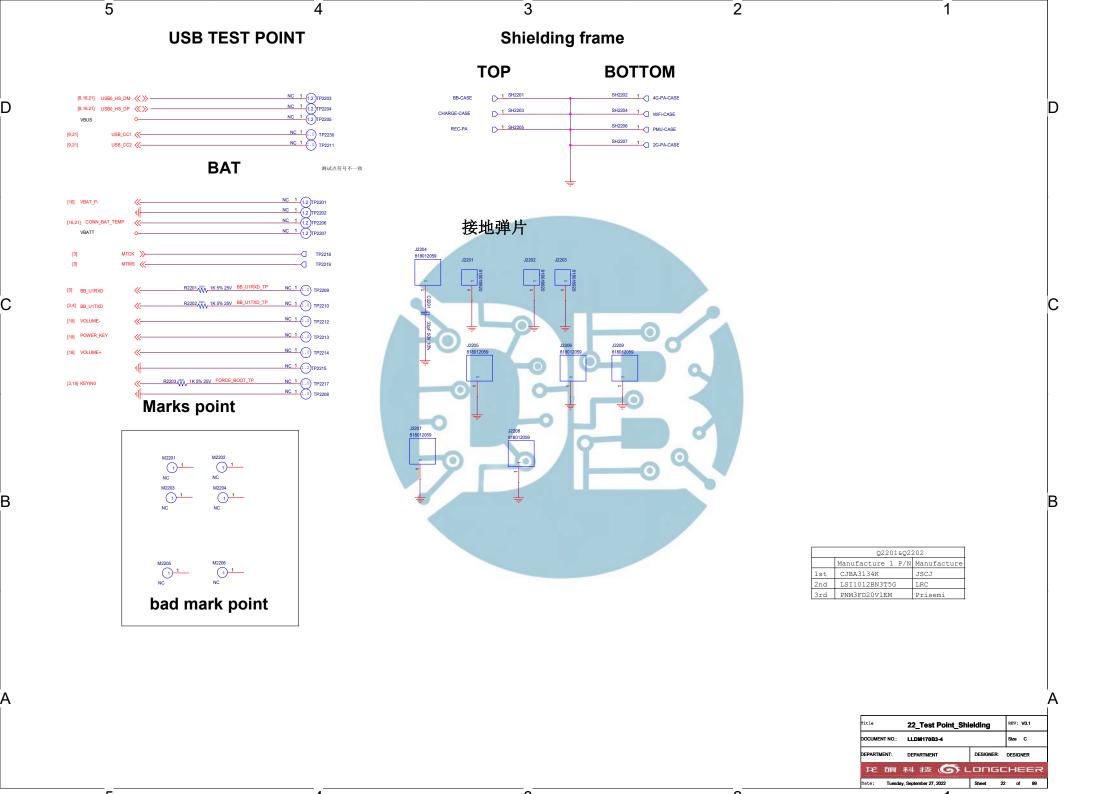












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Modify List:
1:SAR Sense I2C Port change:I2C5--->I2C3.Reference Design remand
2:TXM TRX Port change:TRX4/6, TRX8/9

В

3:NFC Transciver change from NXP PN557 to SAMS S3NRN4V
4: LTE MB Tx PA out port adjust 1/3/66 for good routing

8:RFCTL0/1/2原本连接到TUNNERU2901变更为连接到U2818/U2819/U2802

7:去除R3001,GPS LNA R3018供电由VDD2.8换VDD SIM2

9:网络名RFCTL17/18名字更换为RFCTL19/20连接到U2901 10:U2607/U2818/U2819/U2802的供电从VDD2V8换成VDDLD01

11:U2804/U2817供电由VDDSIM2换成AVDD2V8

17:调换C3109、C3119至NFC芯片端的网络

14:U2818控制网络改成RFCTL\_16

16:删除物料R1801、R1802

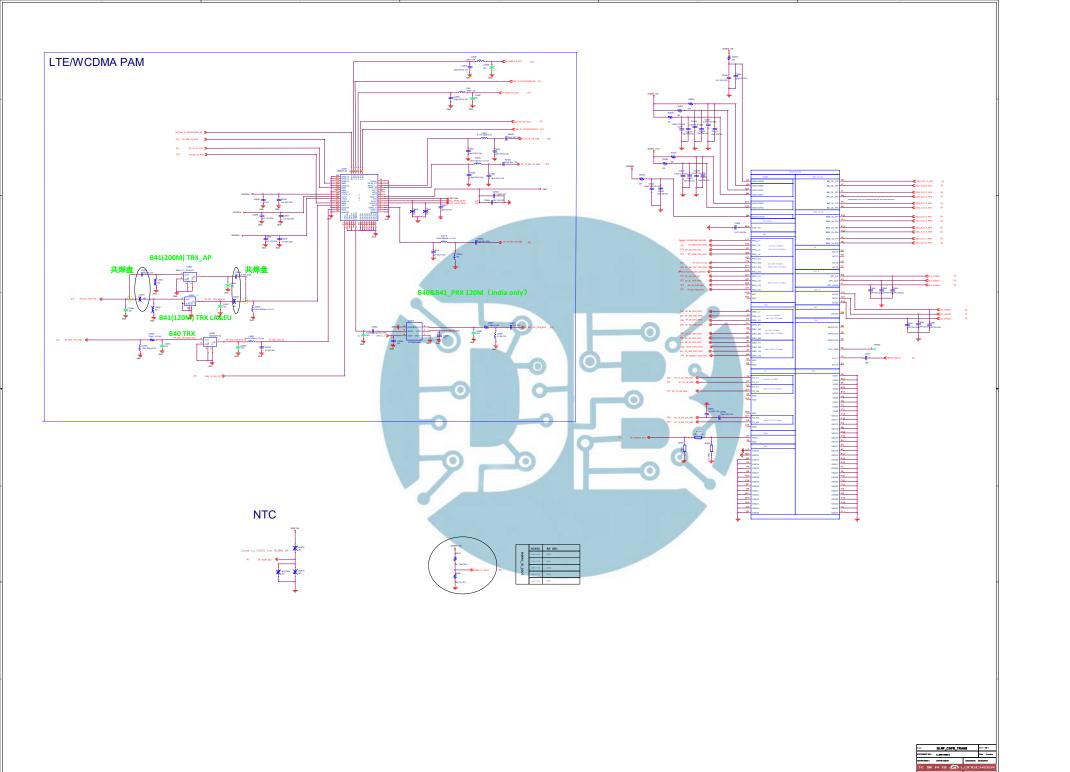
13:RF\_B1\_TRX\_TXM RF\_B66\_TRX\_TXM端口调换

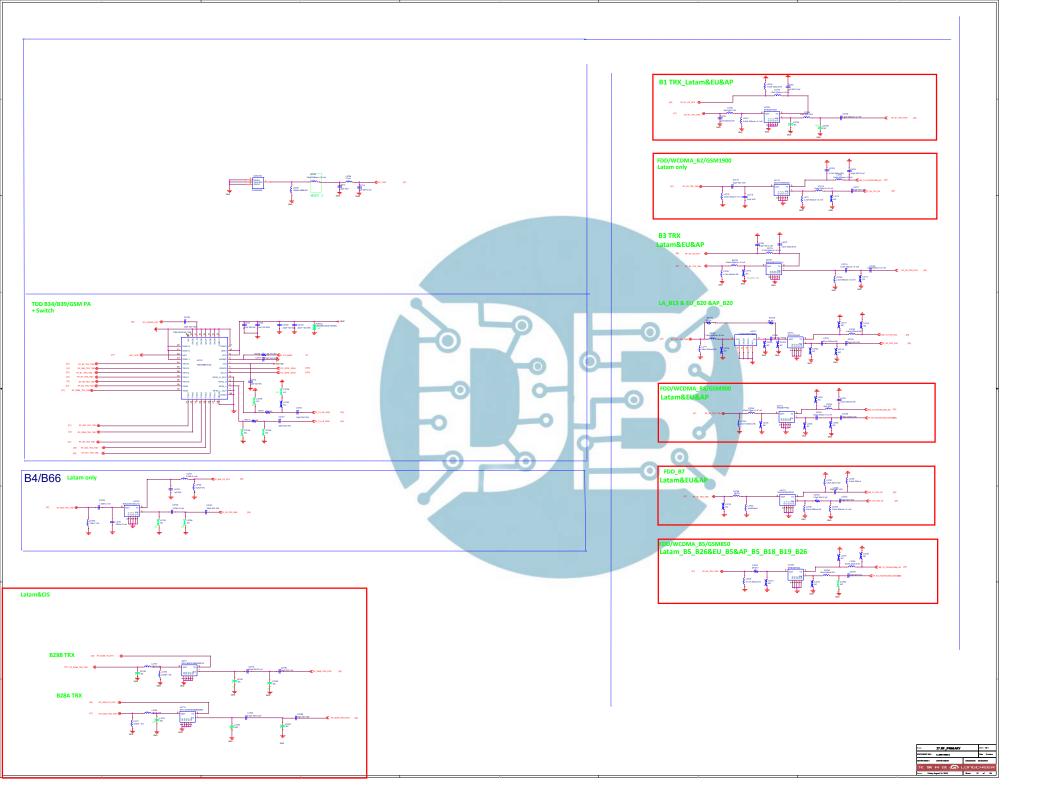
5:去除2908/2907 6:WCN VDDFU接地

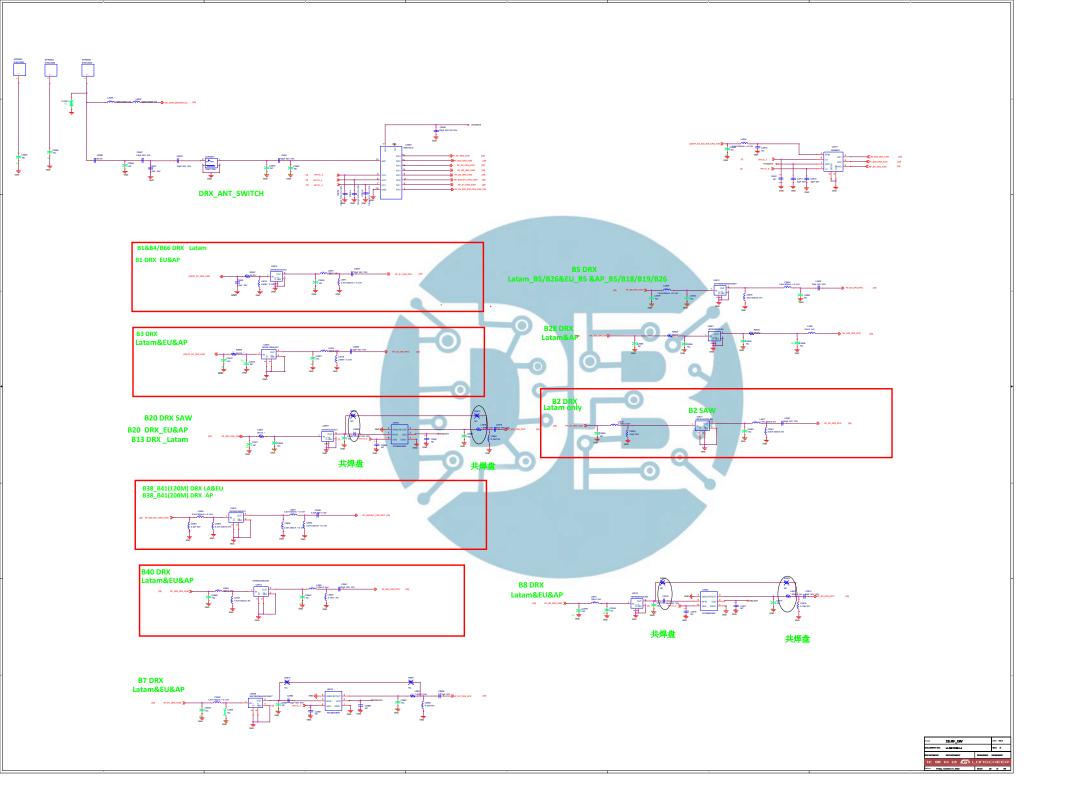
12:新增C3052

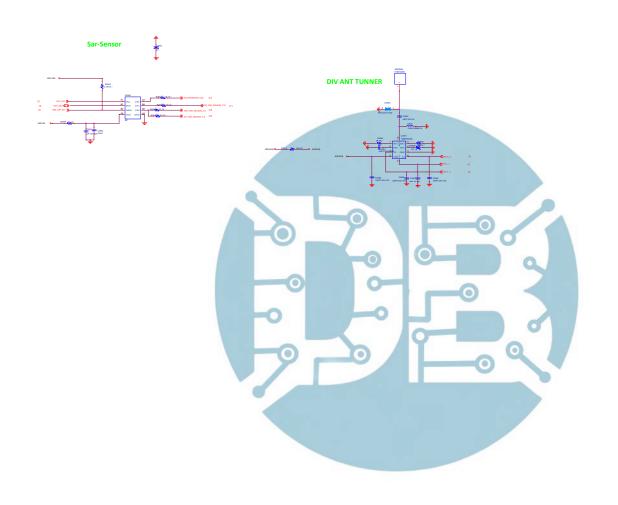
15:+C3053

5 3 2

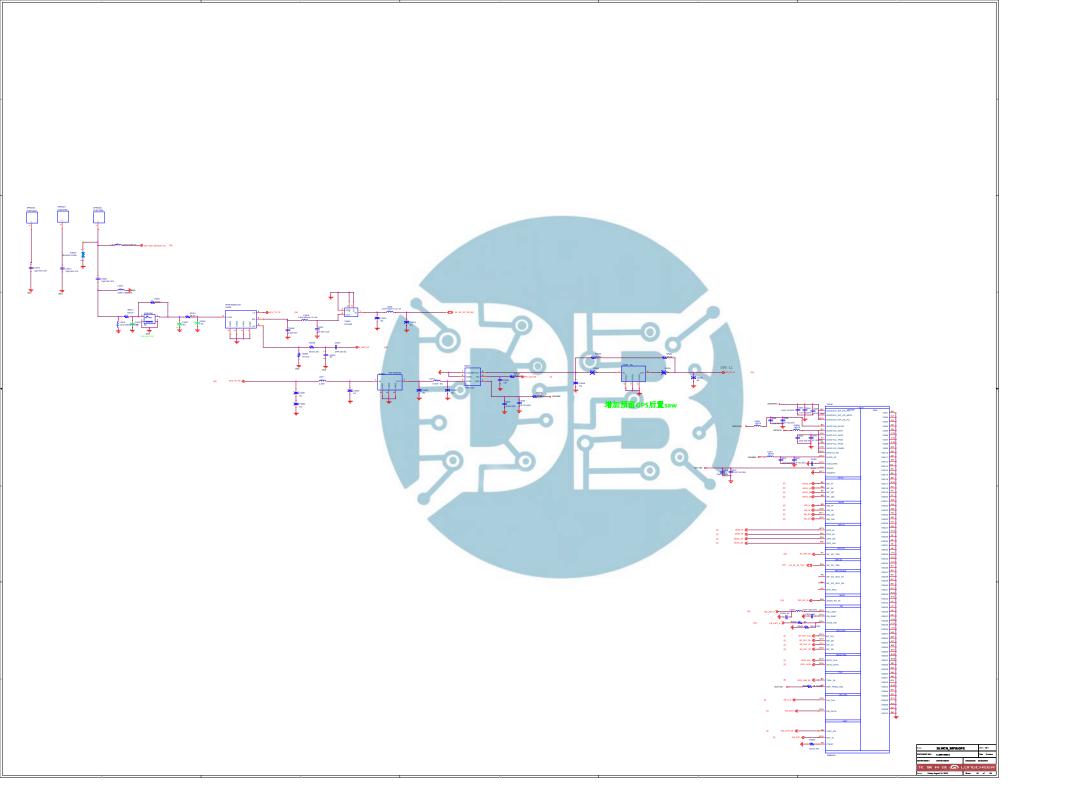


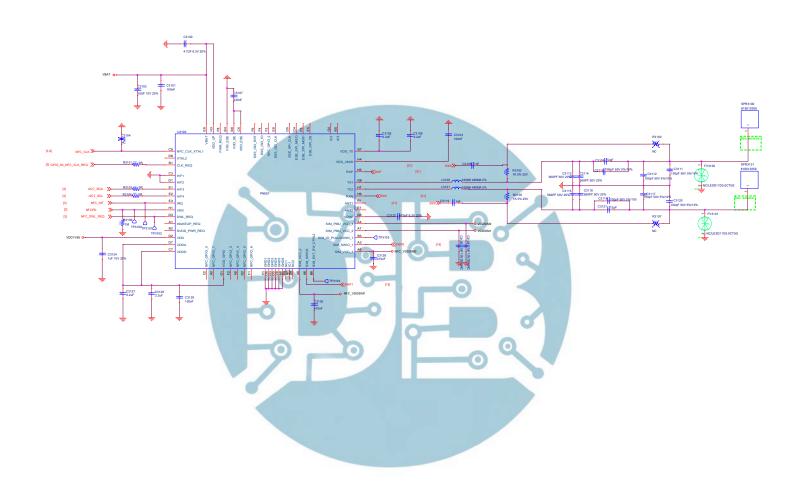












Title	31.NFC		25V: V0.1
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