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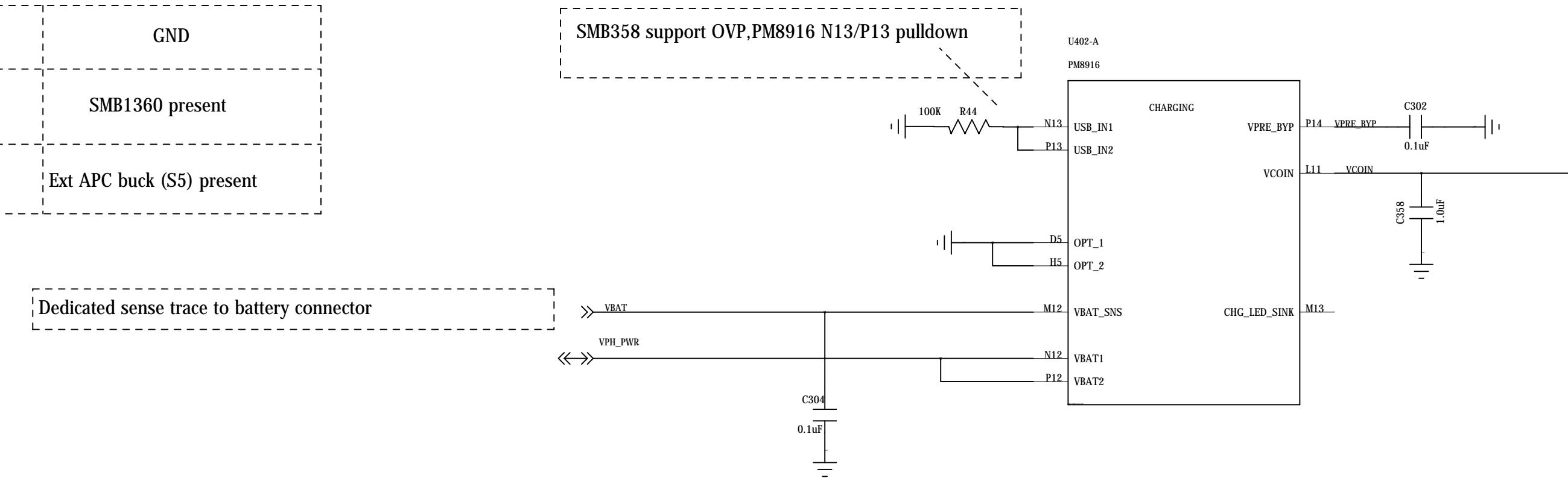
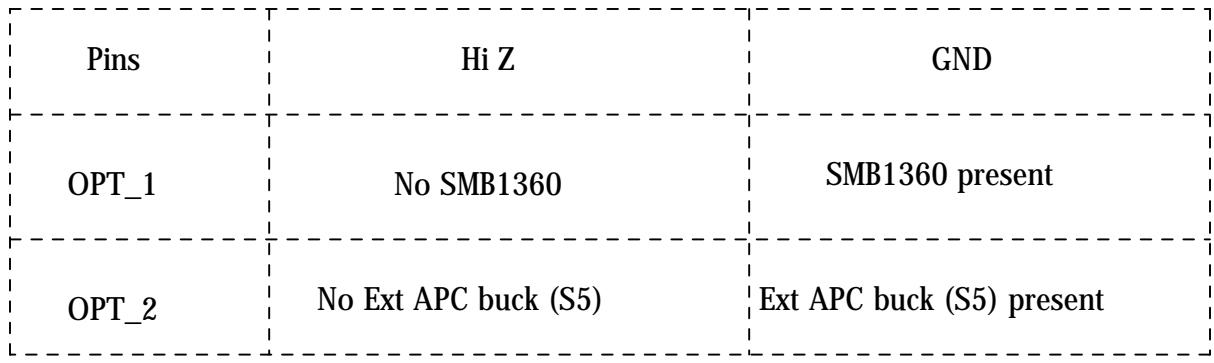
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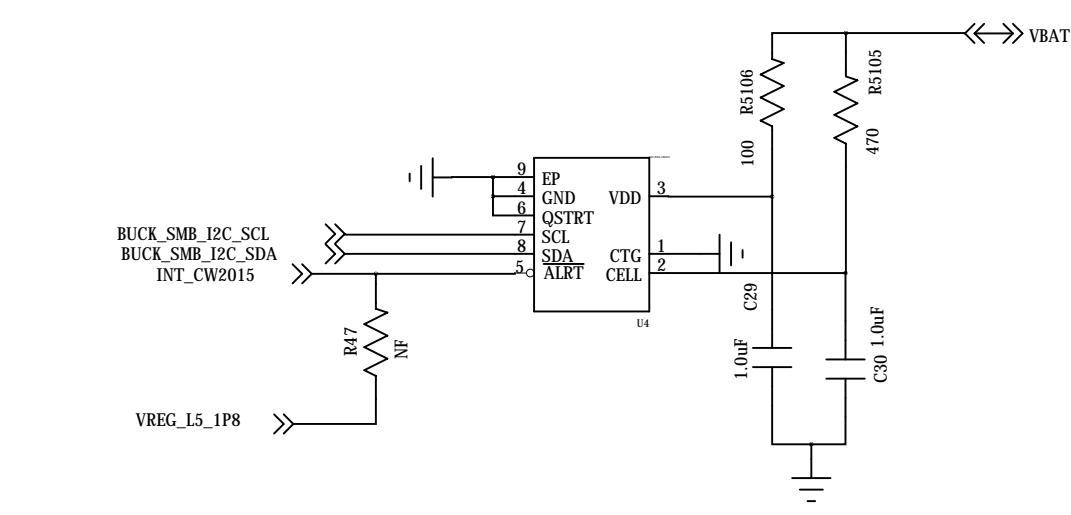
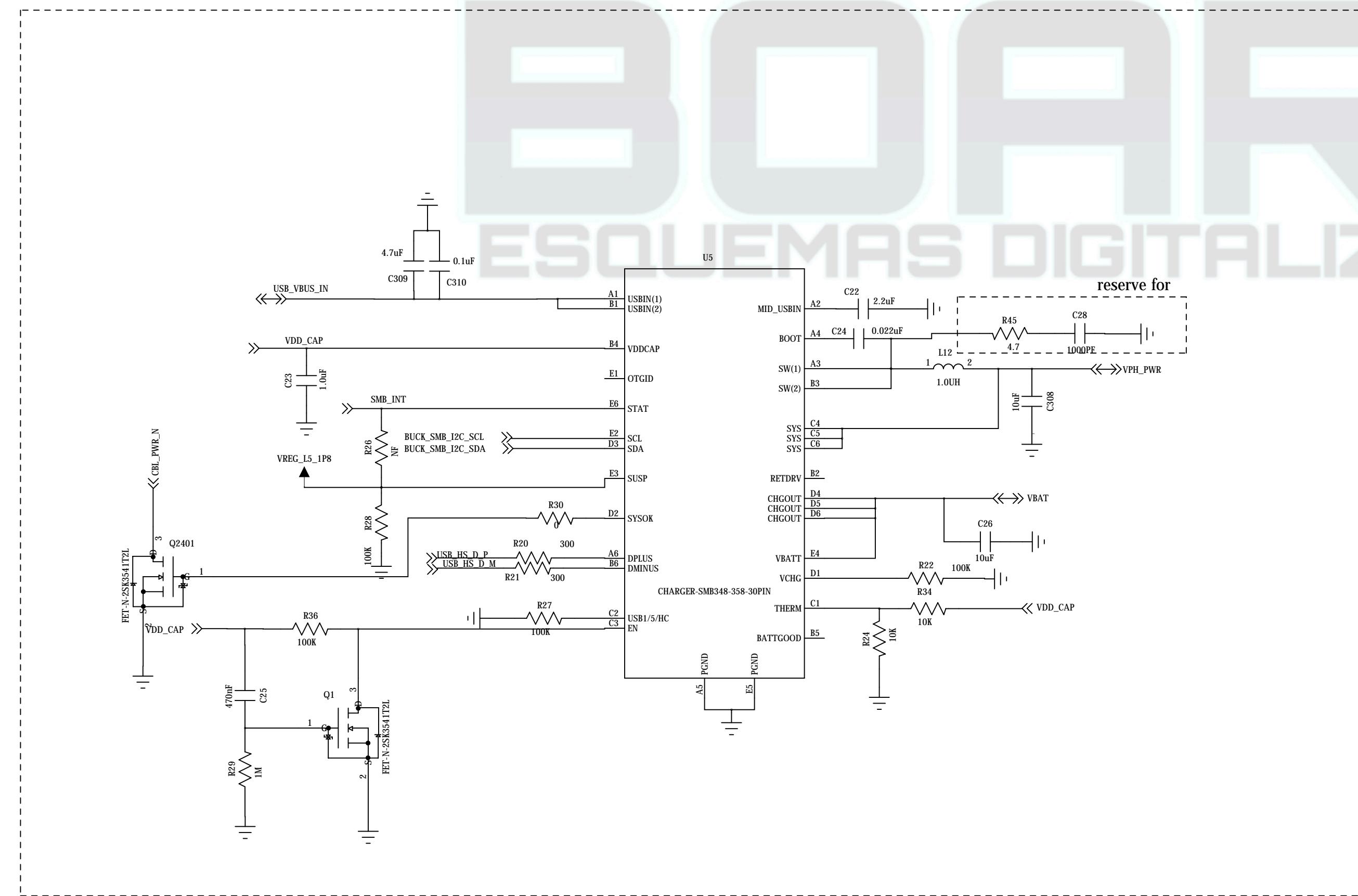
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Size	Sheet Name	Rev
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-----  
Already have 47K resistor in subboard



# BATTERY CONNECTOR

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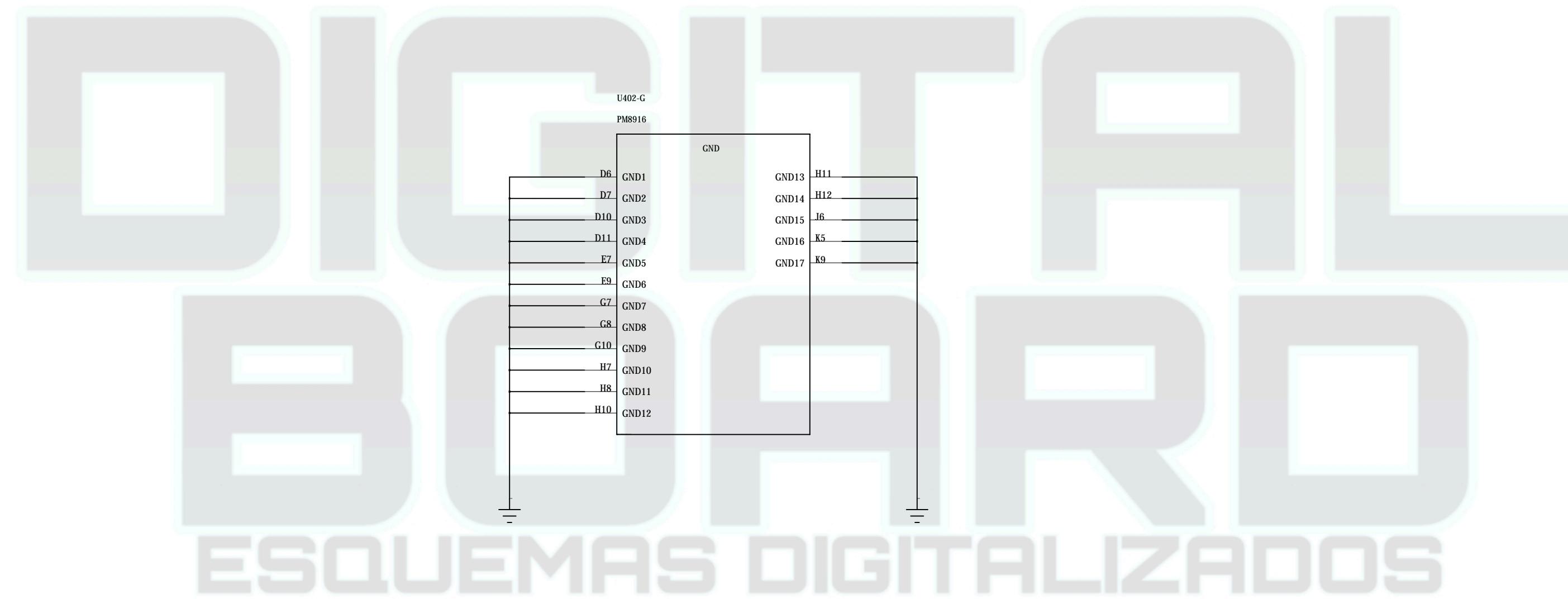
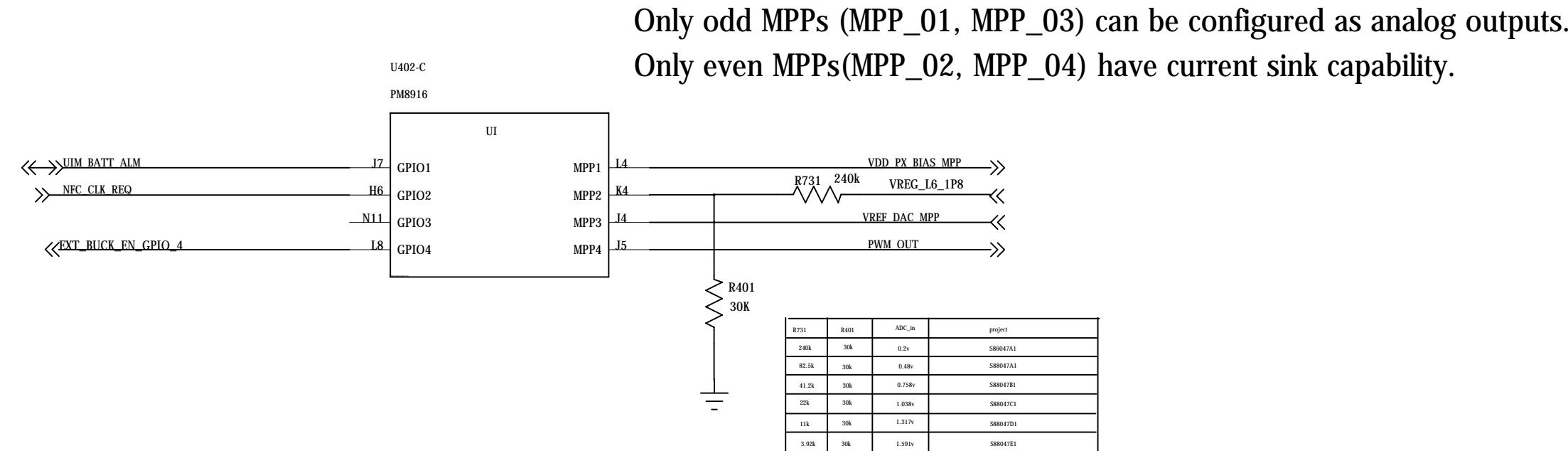
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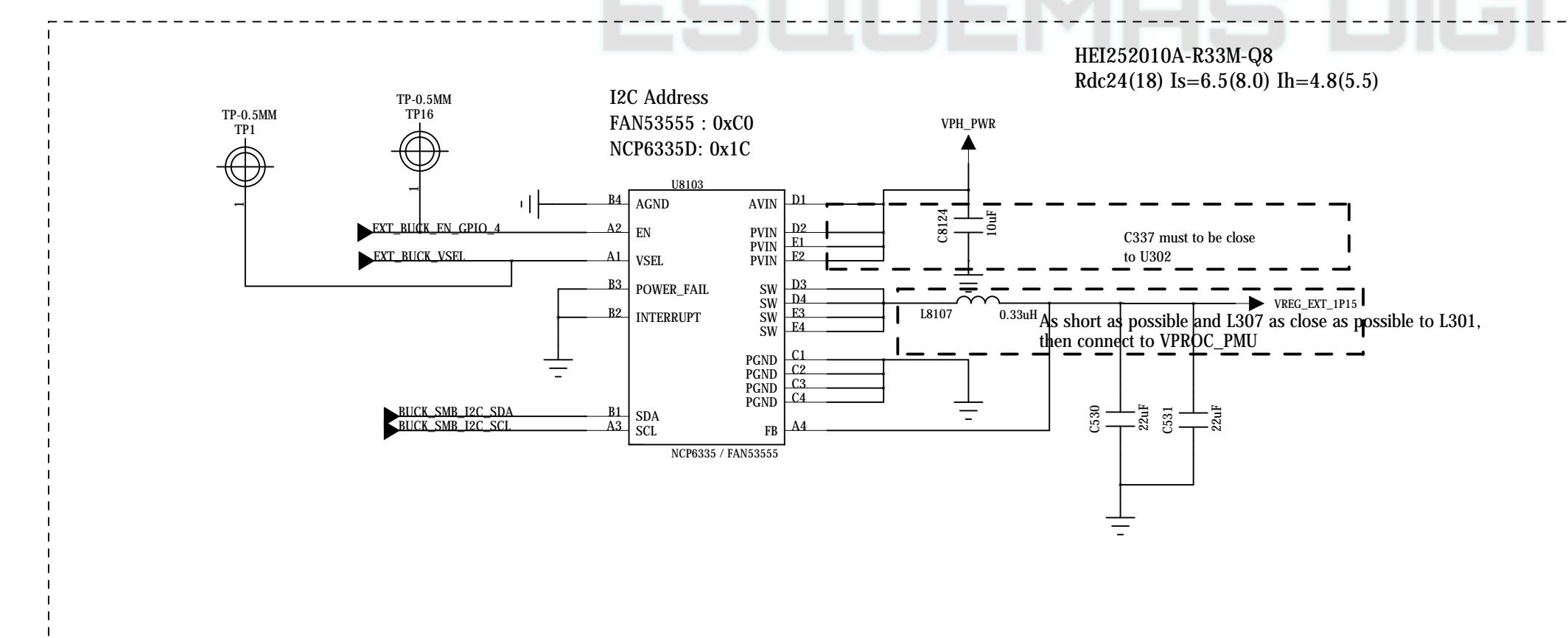
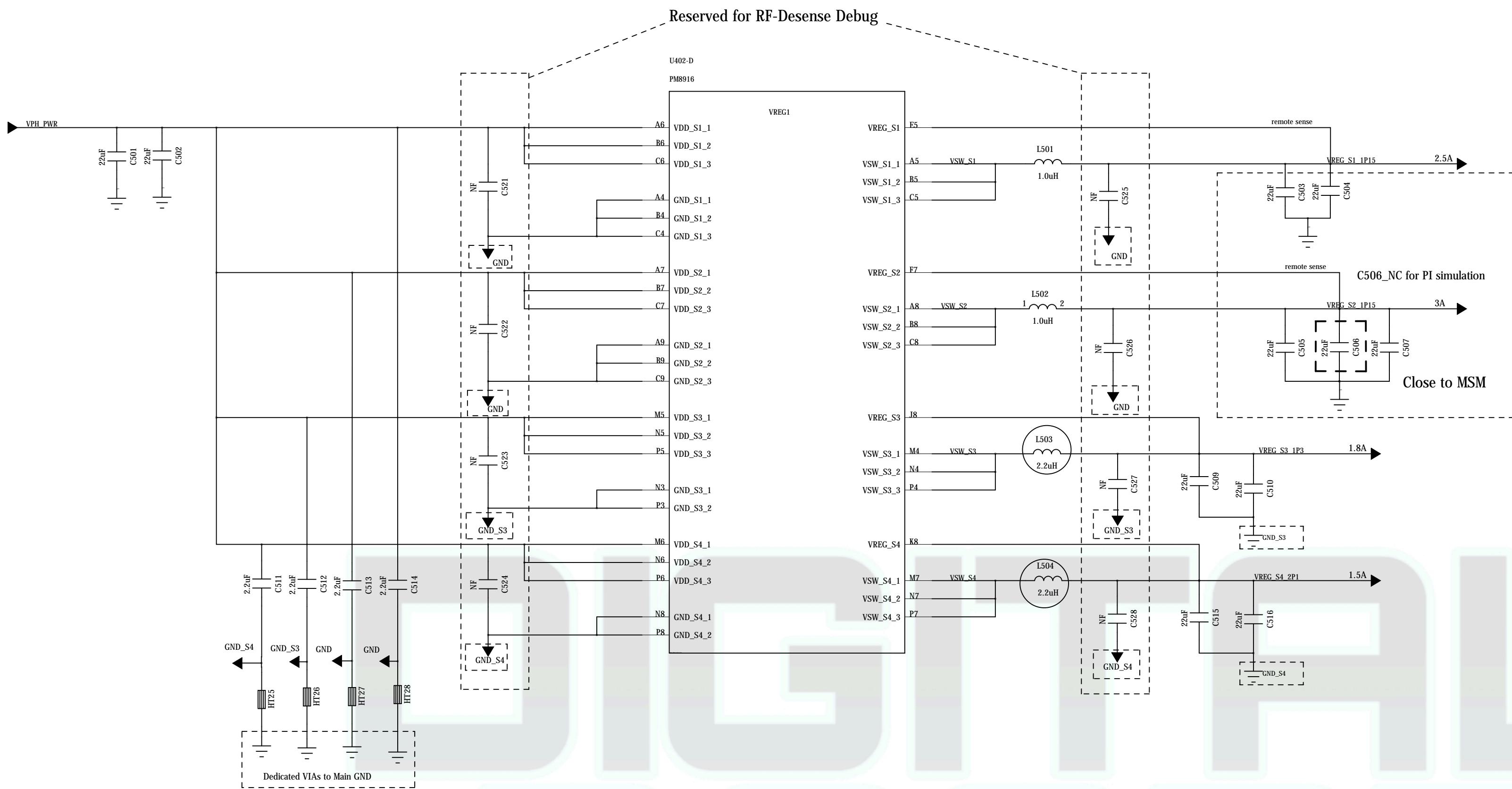
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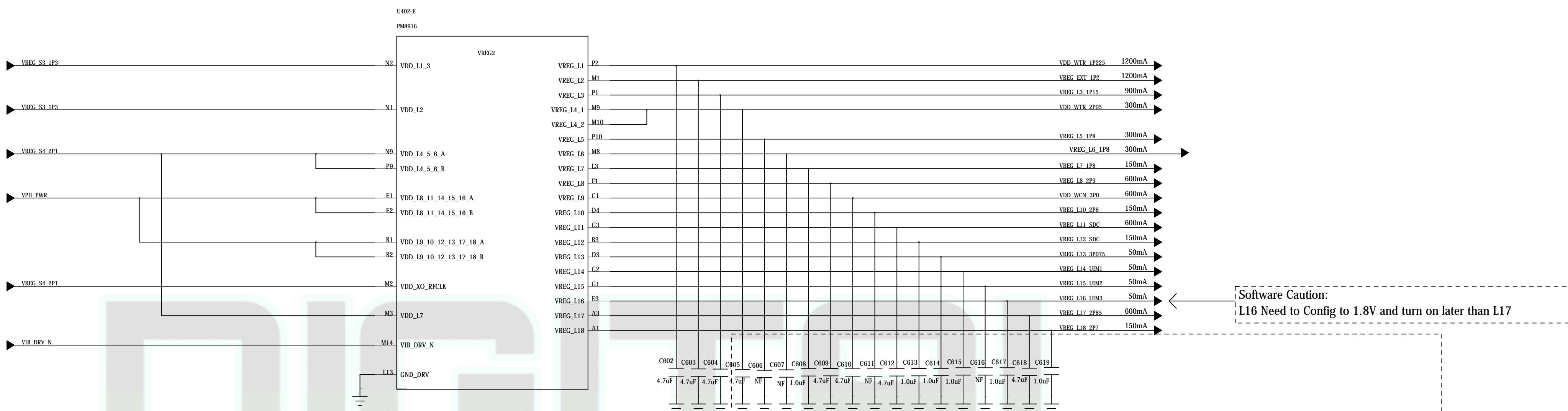
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Size	Sheet Name	Rev
Date:	Sheet	of



PSEUDO CAPLESS LDOs  
I4, I5, L6, L7, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18

Local output capacitor can NC/Remove depends on remote load capacitors and PCB layout  
LDOs I8, I9, L11, L17 each shall have total effective output capacitance of 4.7uF.  
Please refer to PM8916 training slides(80-NK808-21) for limits on LDO output trace resistance and inductance  
Rest of the LDOs shall each have total effective output capacitance of 1.0uF.

The Pseudo capless LDOs must comply to following tolerable routing requirement:  
P50: R<400mOhms, L<45nH  
P150: R<200mOhms, L<20nH  
P300: R<150mOhms, L<18nH  
P600: R<150mOhms, L<18nH

Please ensure when you DNI the output capacitor of Pseudo capless LDOs  
the effective total capacitance at load side shall match above requirement

NC first

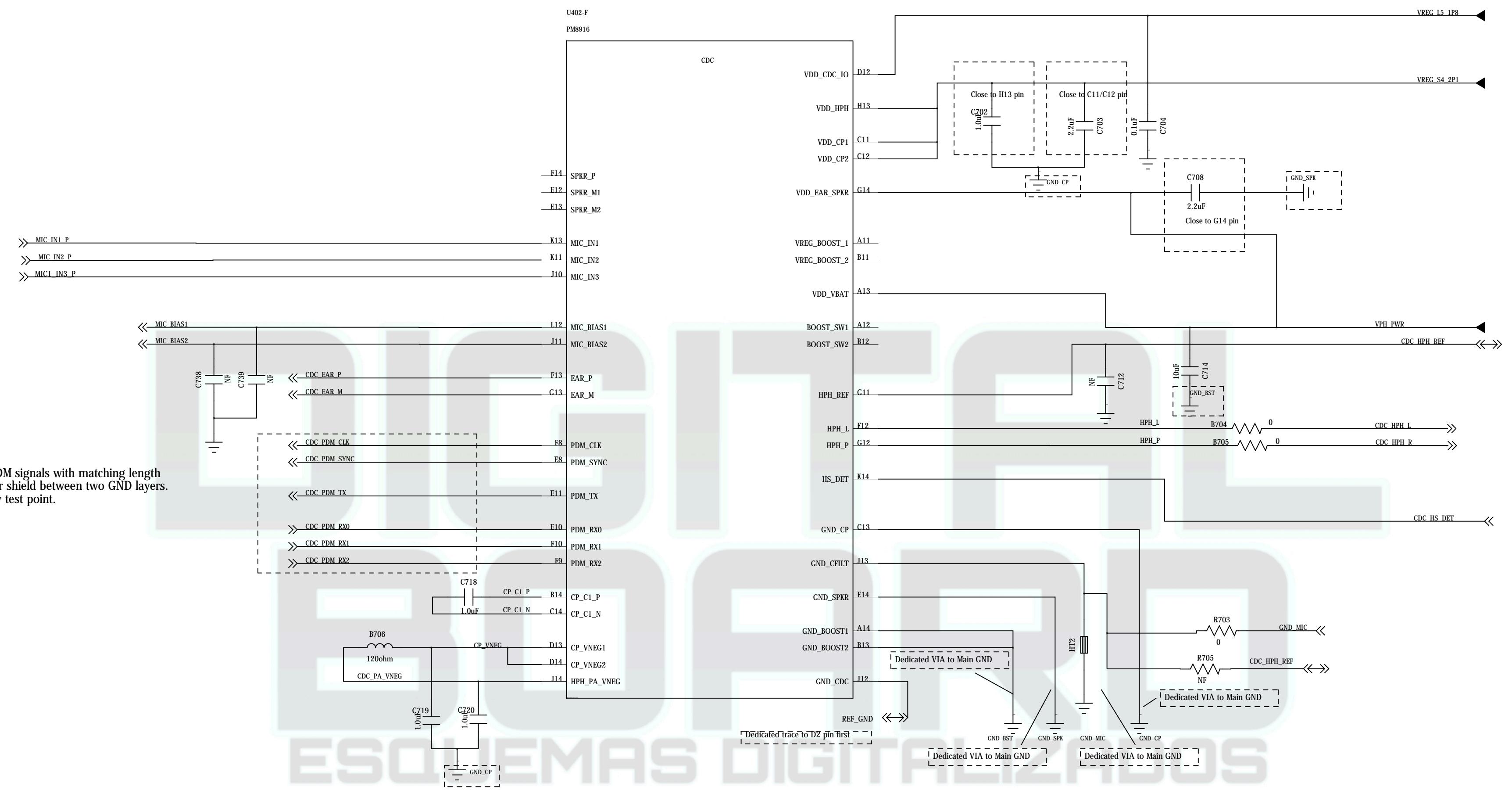
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Date	Sheet	of



Route codec PDM signals with matching length on a inner layer shield between two GND layers. Do not add any test point.

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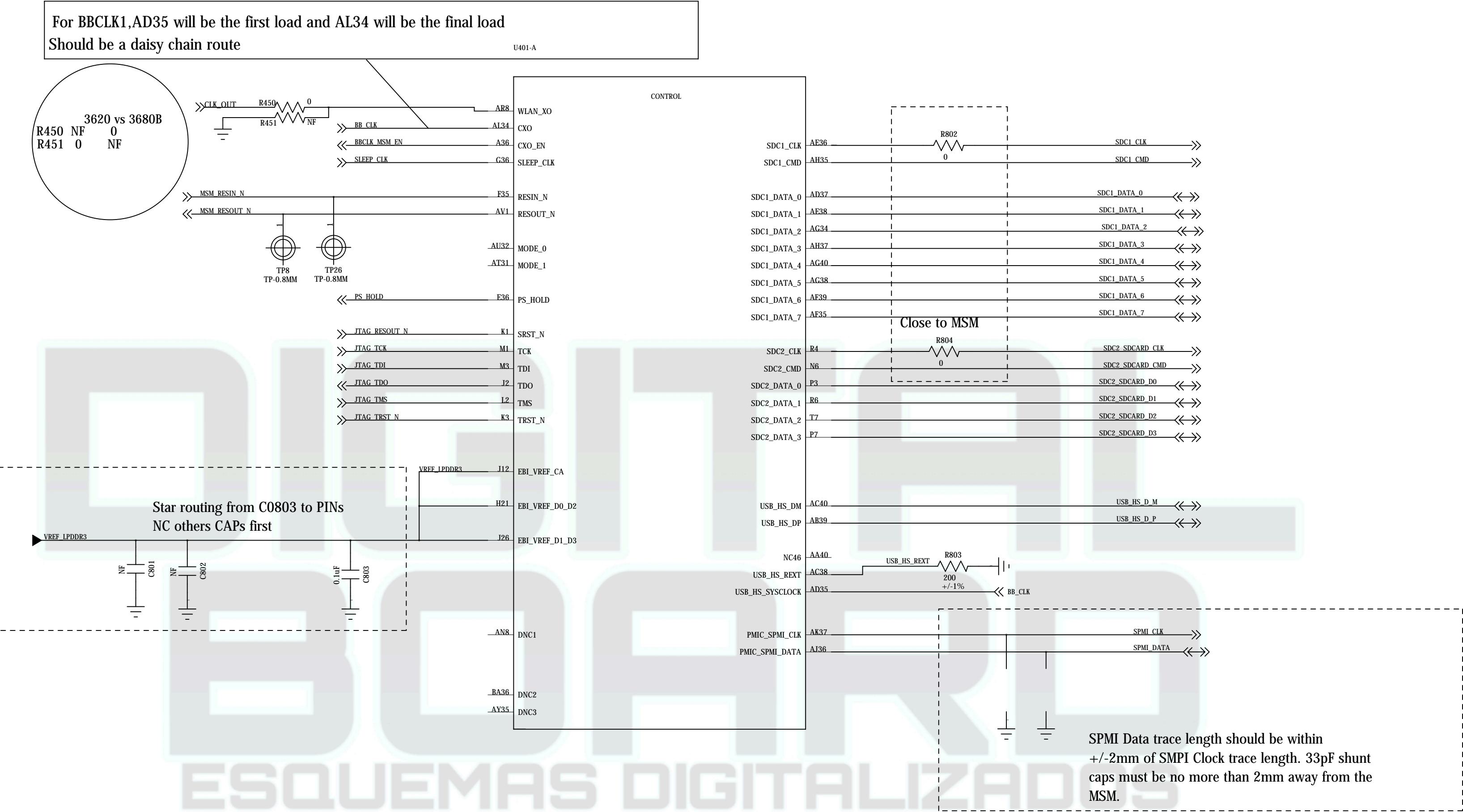
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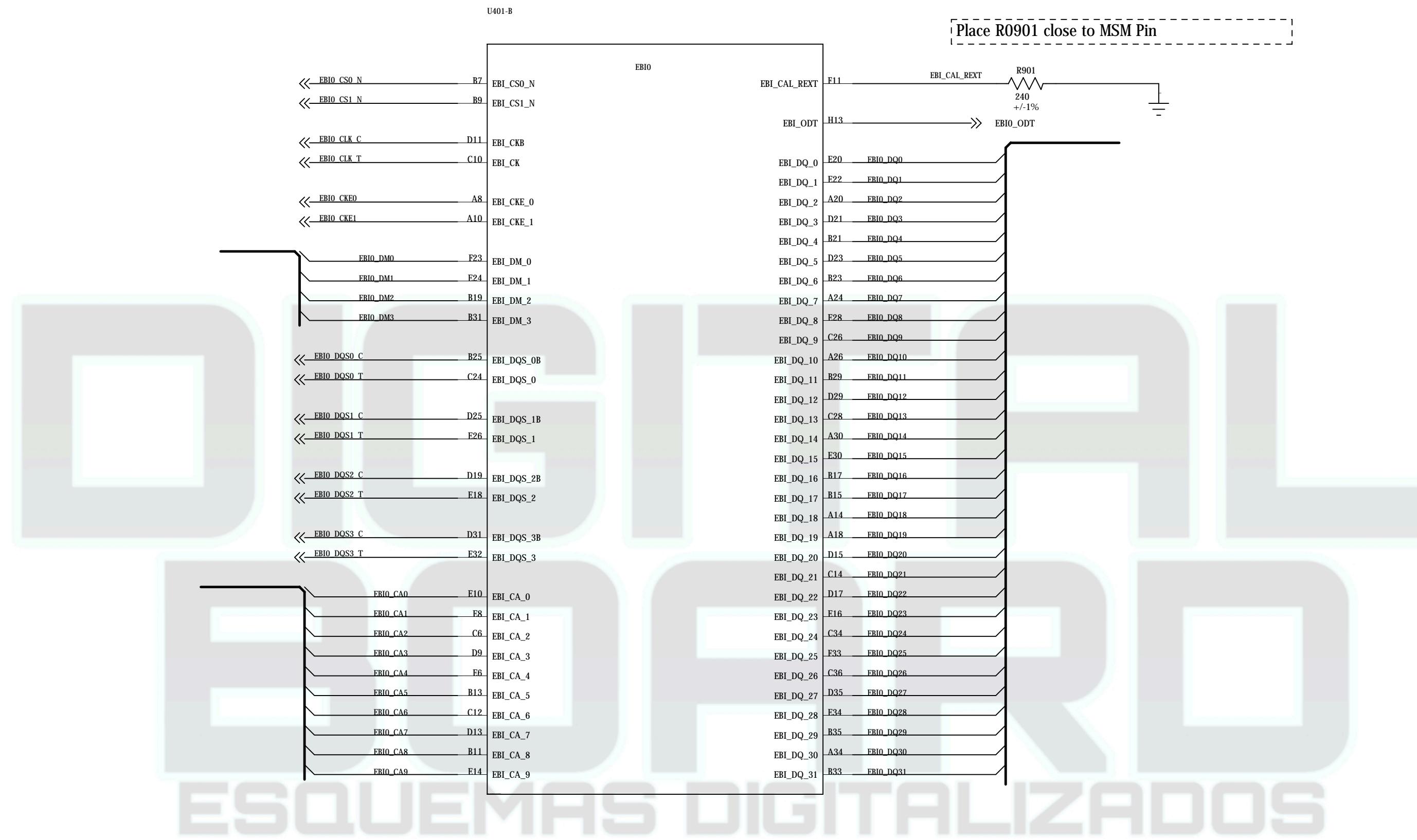
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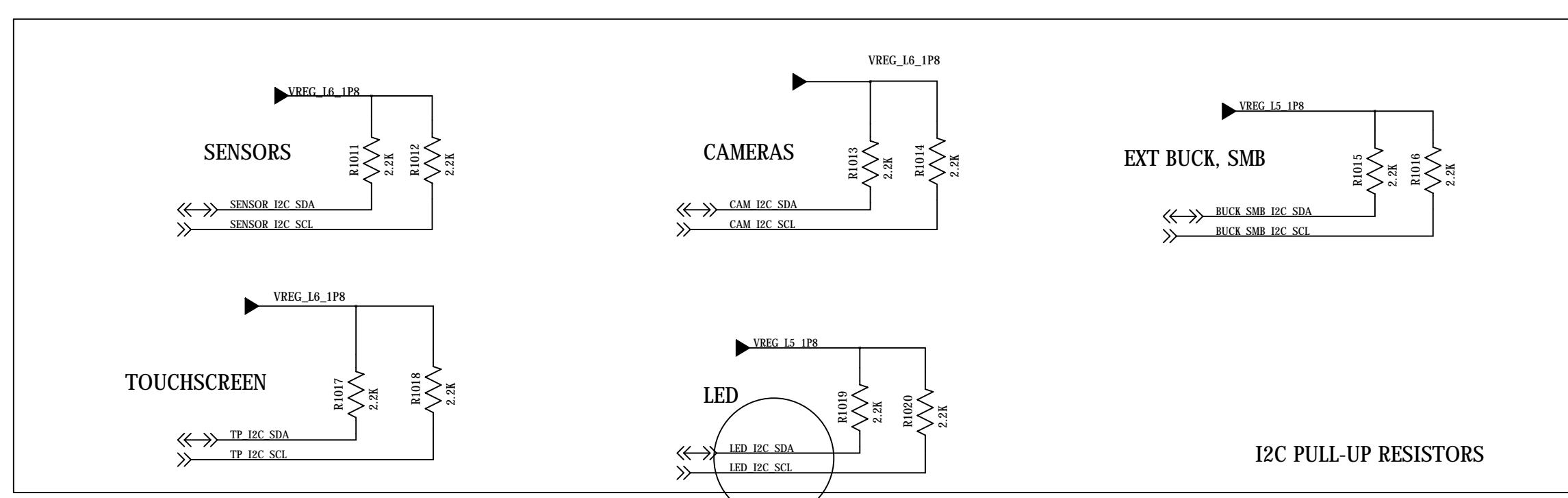
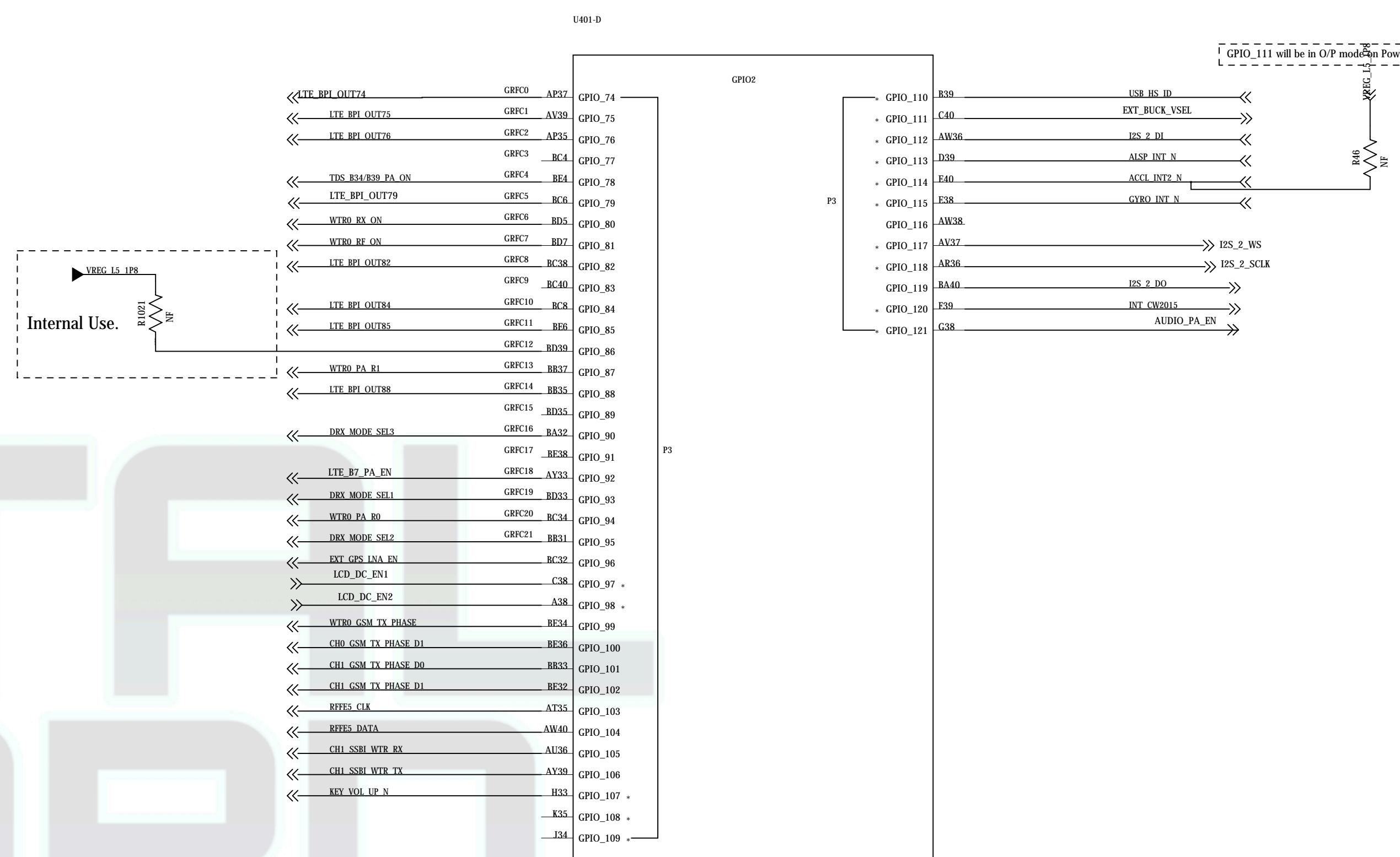
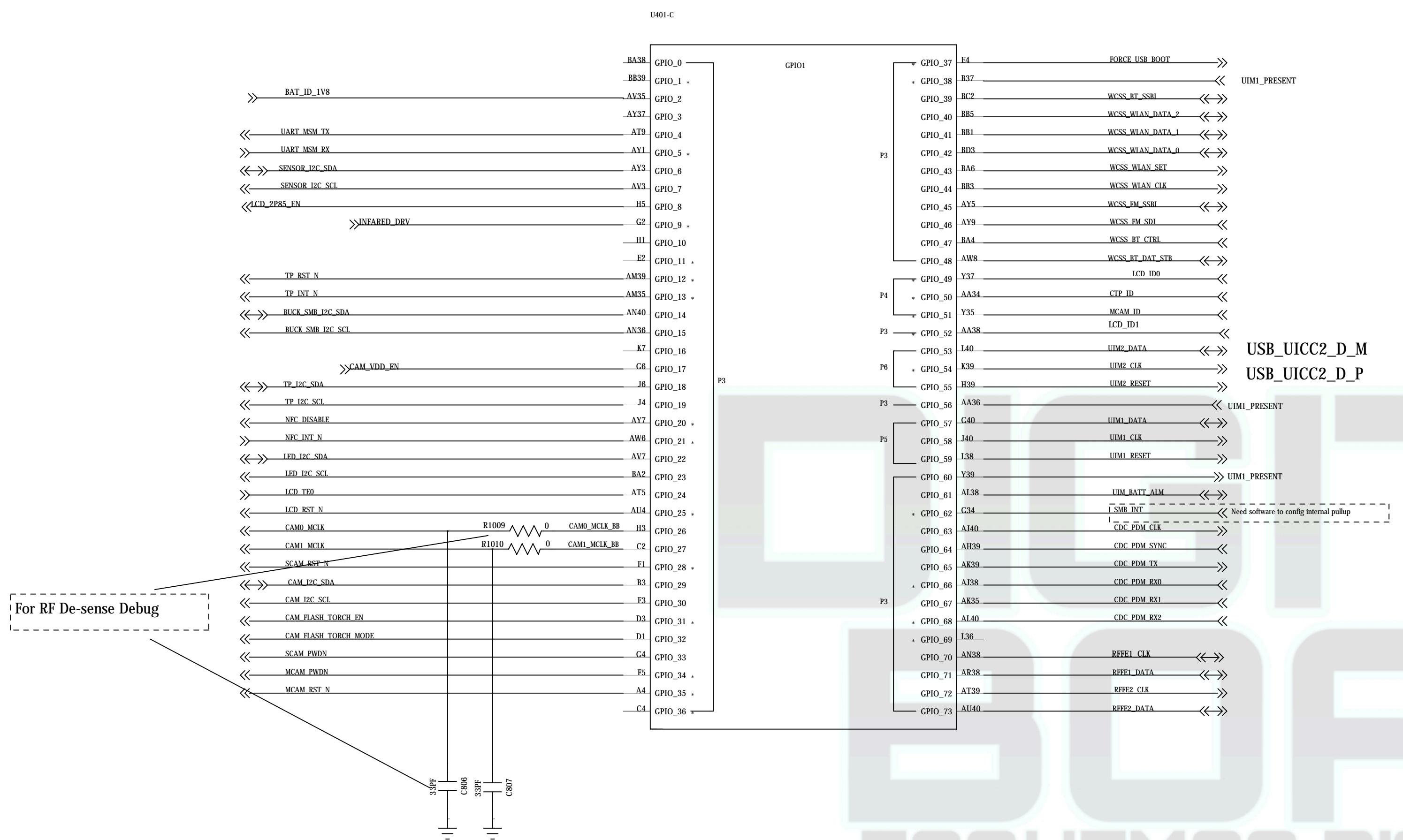
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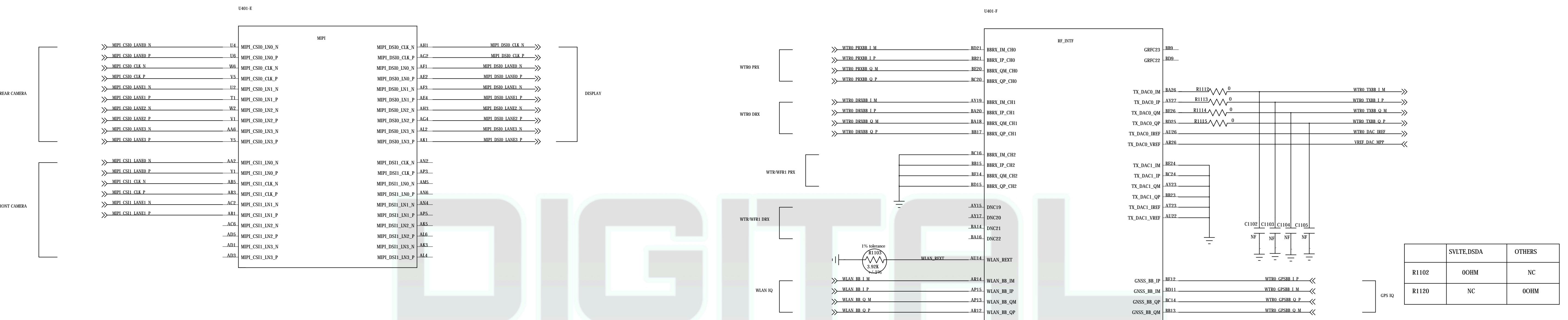
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Date:		Sheet of



These NC resistor is for SVLTE or DSDA. Change them to 0ohm on other modes.

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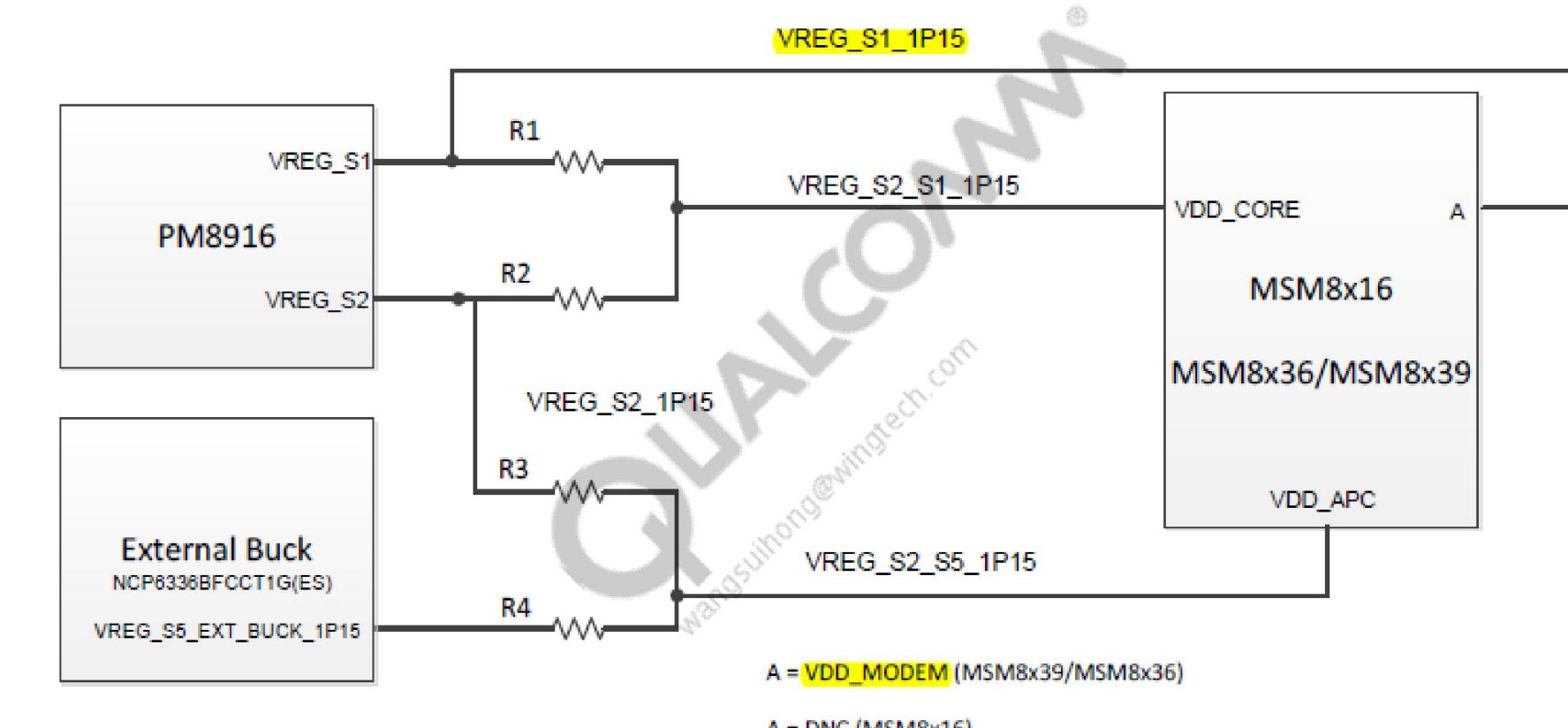
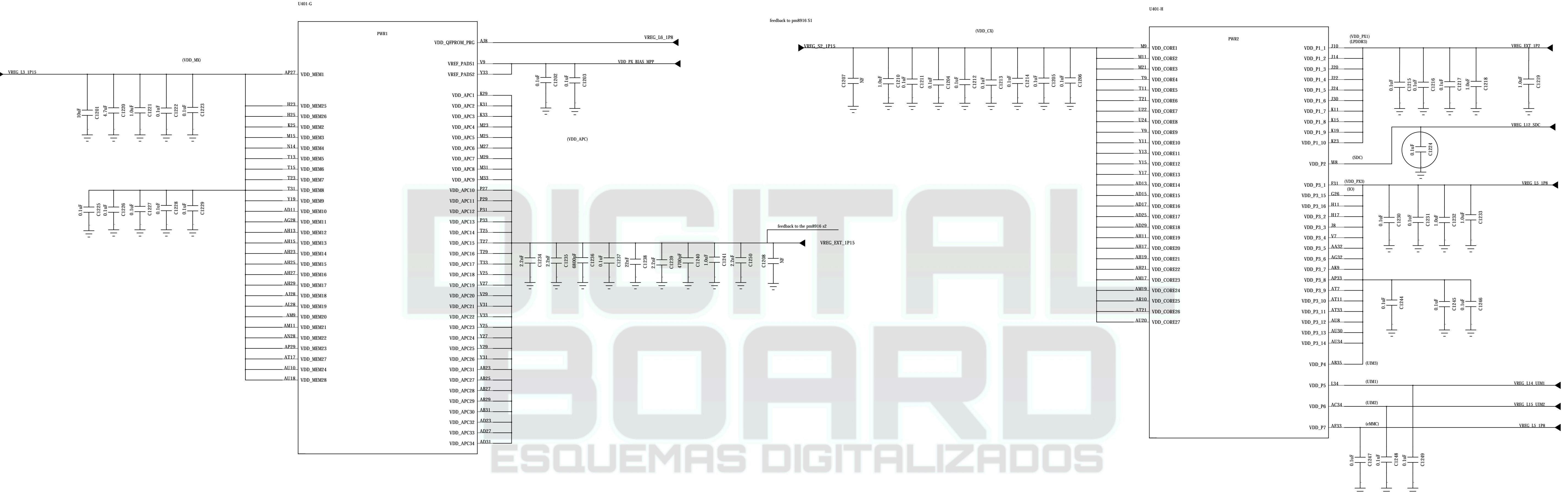
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# IC BOARD

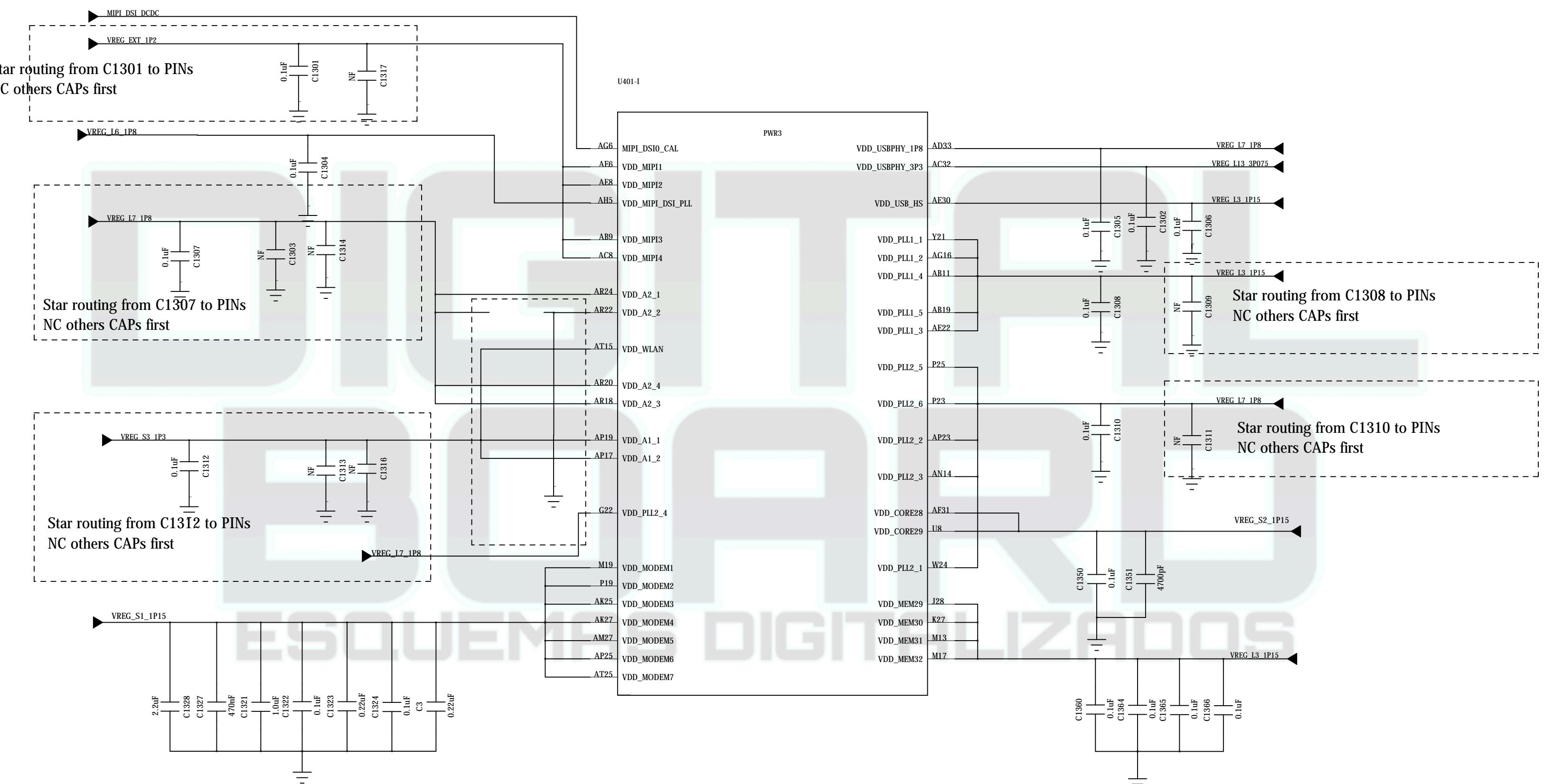
## ESQUEMAS DIGITALIZADOS



SoC	Jumper on	Jumper off
MSM8x16	R1, R3	R2, R4
MSM8x36/MSM8x39	R2, R4	R1, R3

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Sheet _____	of _____



	SVLTE,DSDA	OTHERS
R1301	0OHM	NC
R1302	NC	0OHM

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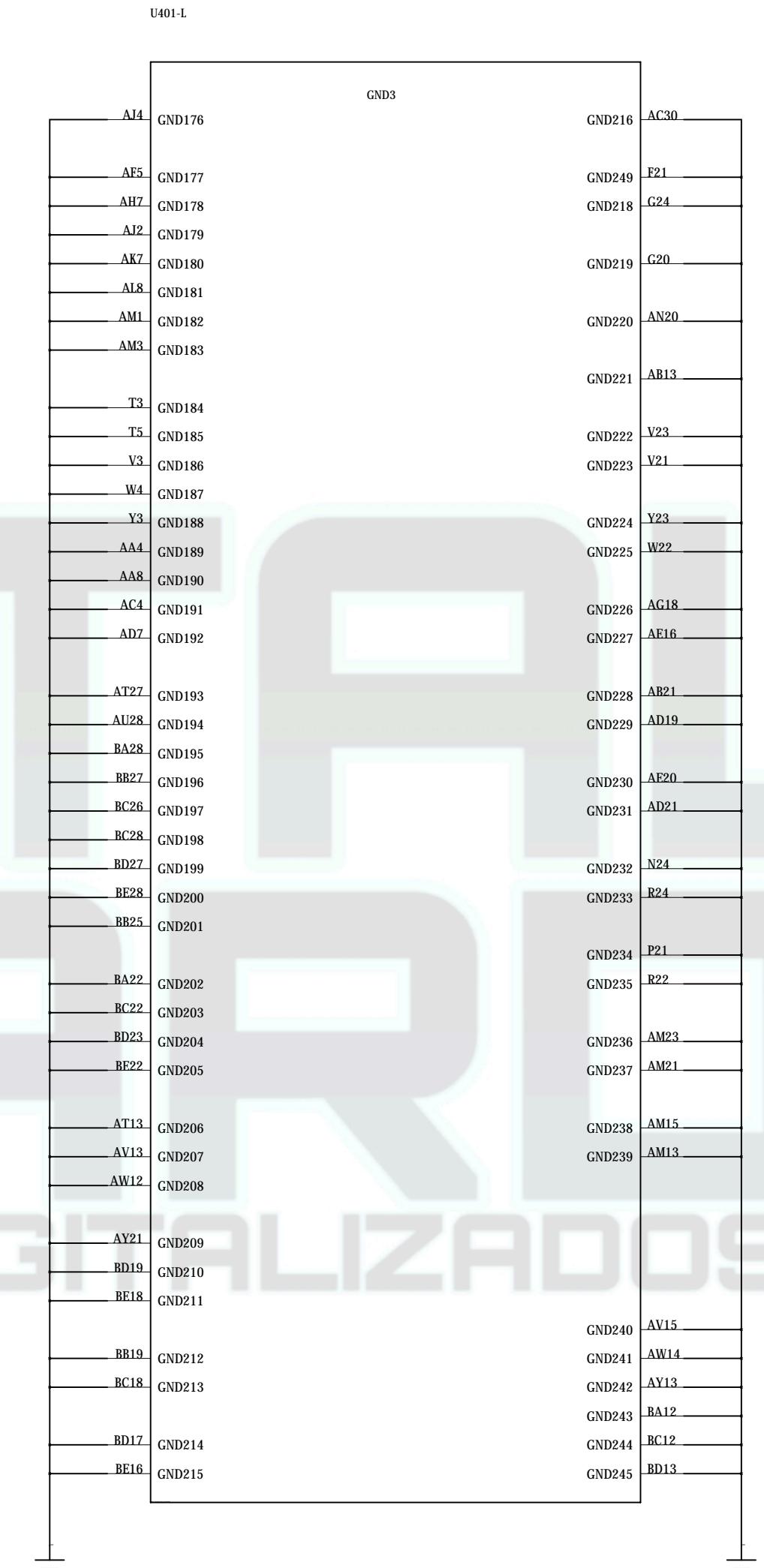
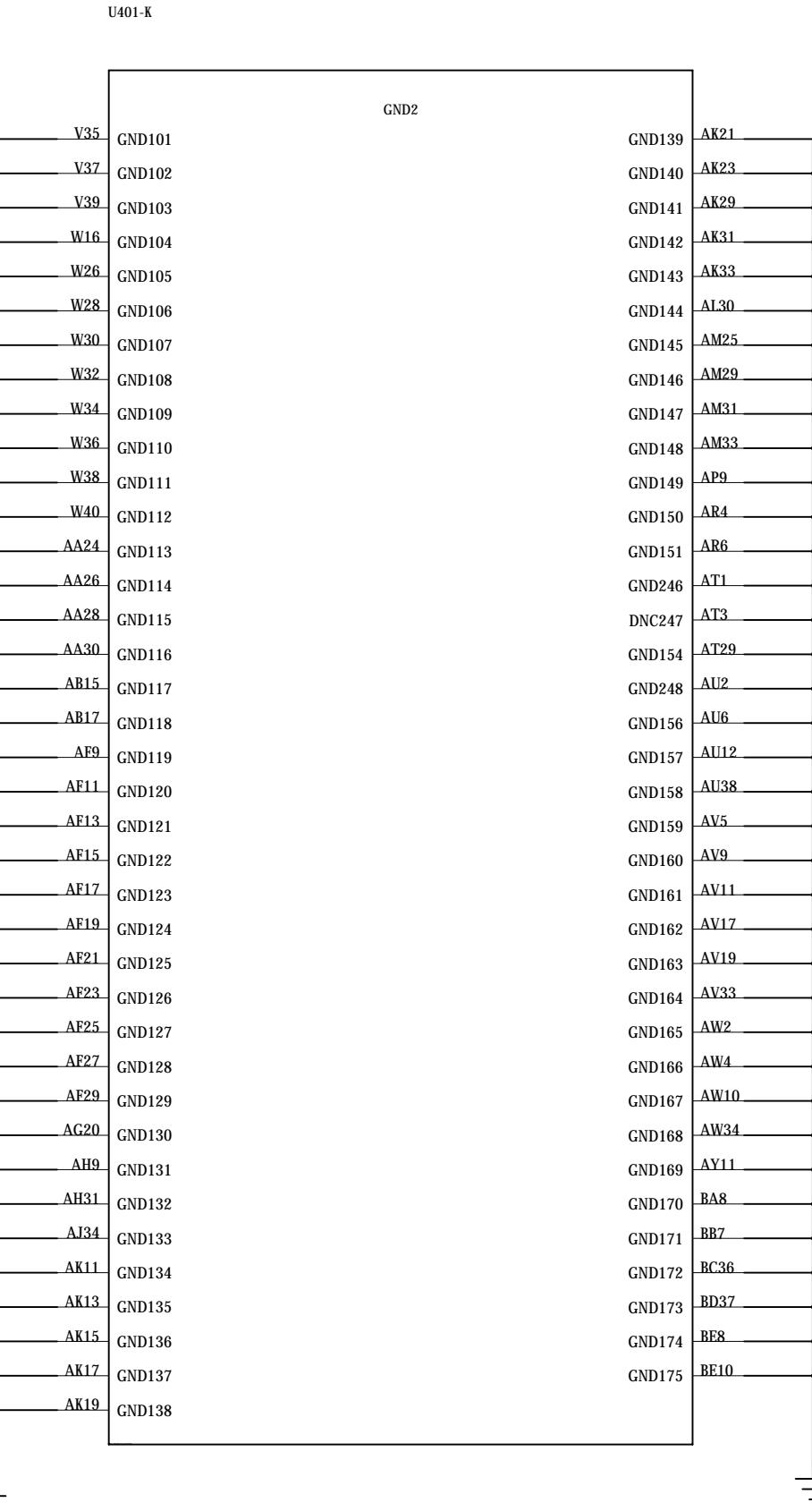
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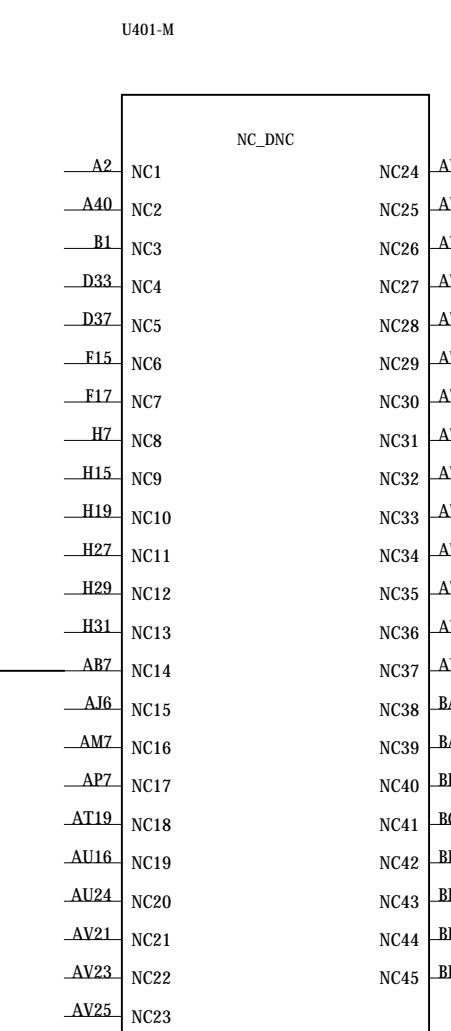
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ize	Sheet Name	Rev
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MIPI\_DSI\_LDO is configured to be LDO mode defaultly.  
if using DC/DC mode,  
L1401 need to be replaced with 2.2uH inductor

CAD NOTE: Loop to be shorted with MSM AB7 pin



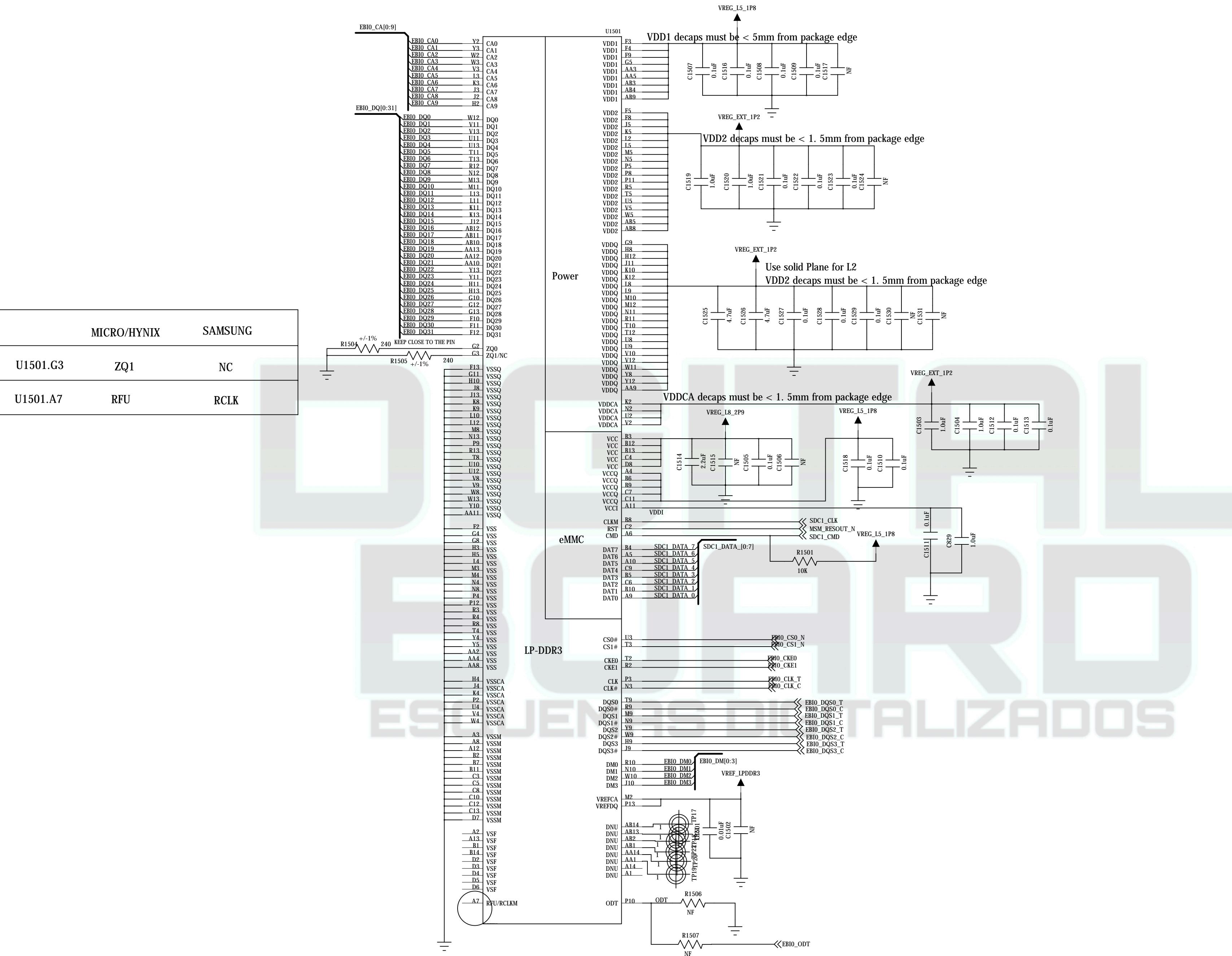
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Note: Pull-up resistors on SDC1\_DATA are PCB and eMMC vendor dependent

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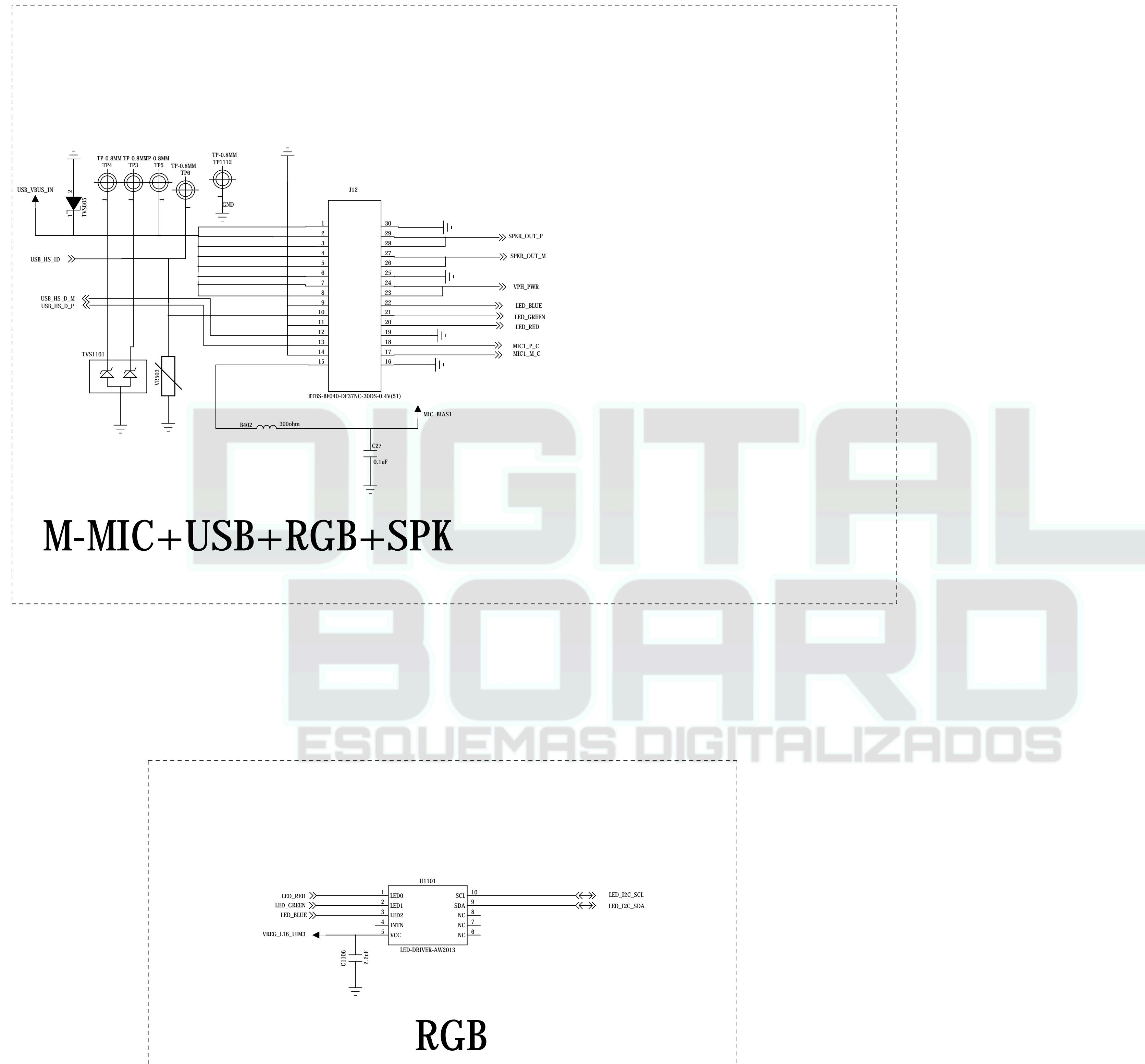
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ize	Sheet Name	Rev
te:	Sheet	of



Power on sequence: can be applied in any order

I2C Address	
Write	8B0x8A
Read	8B0x8B

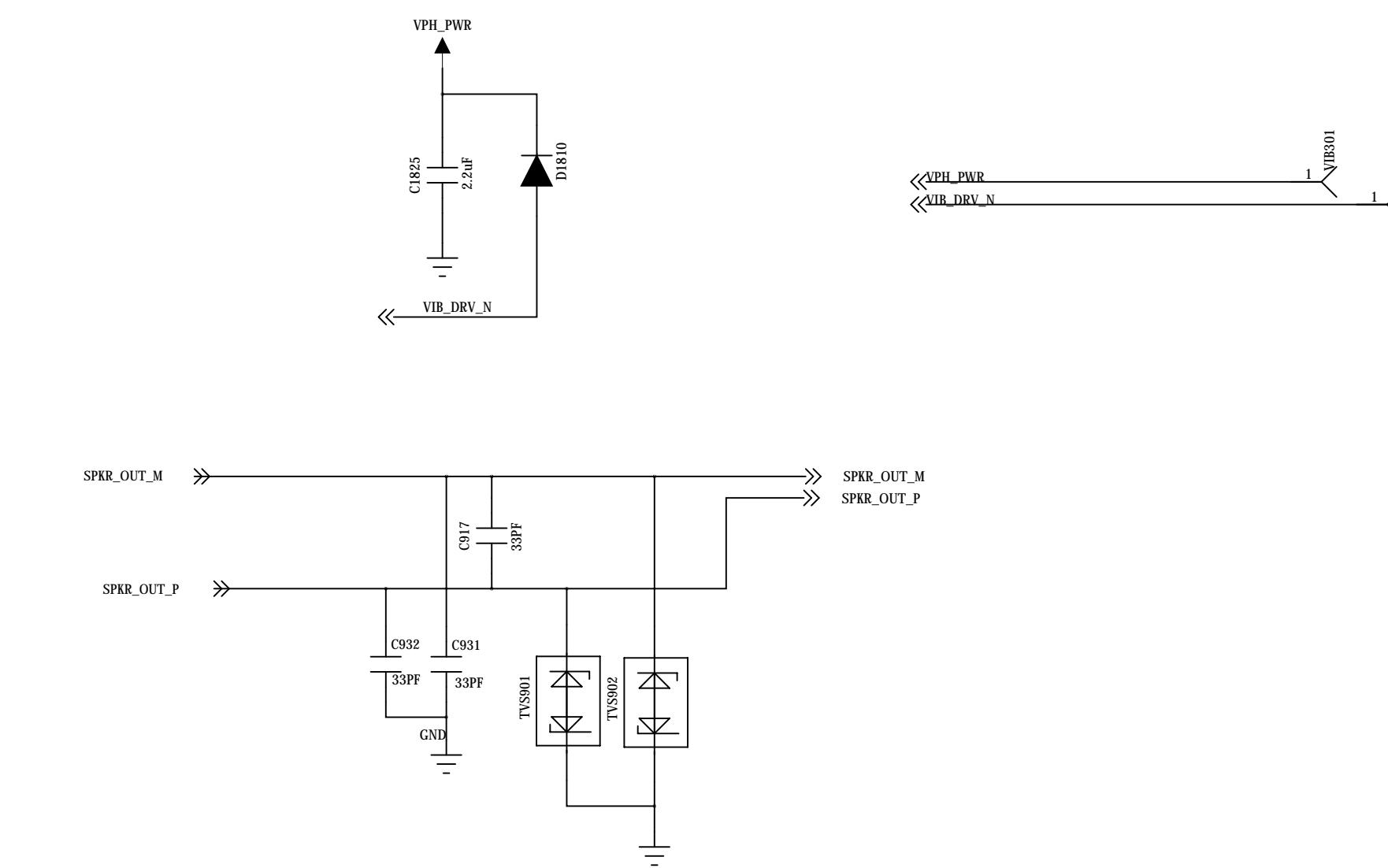
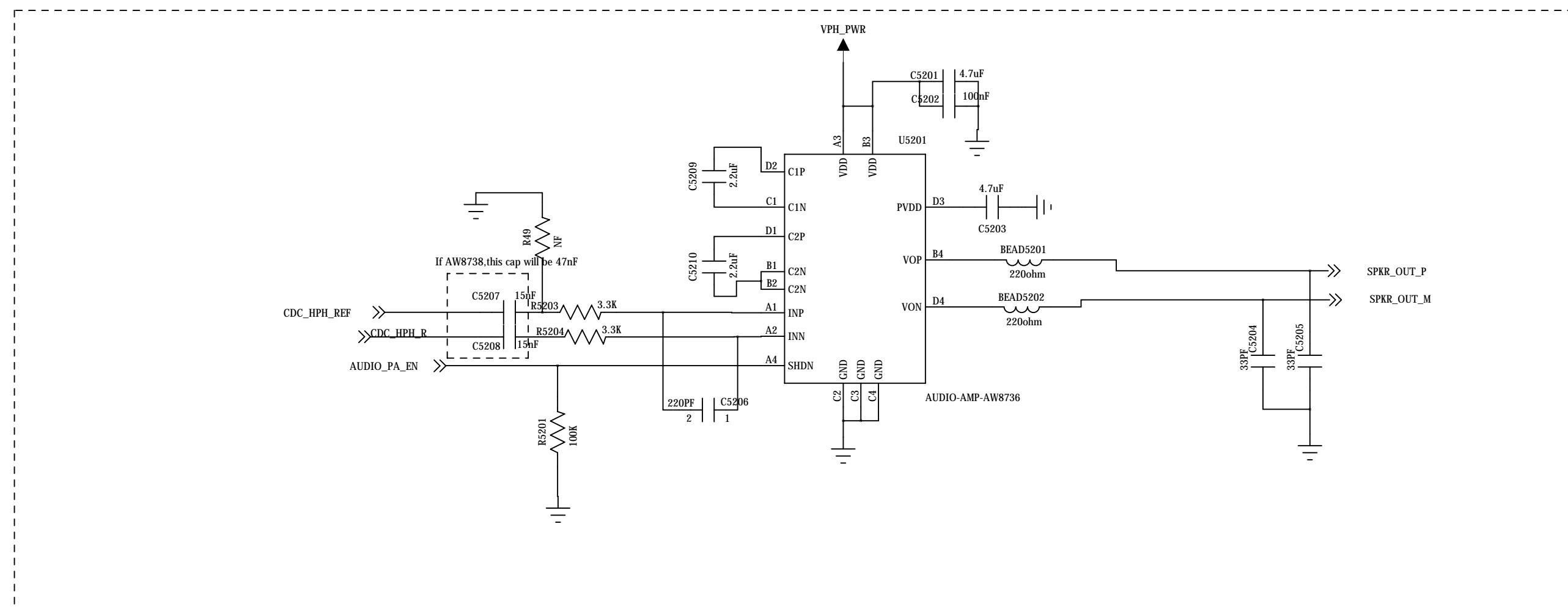
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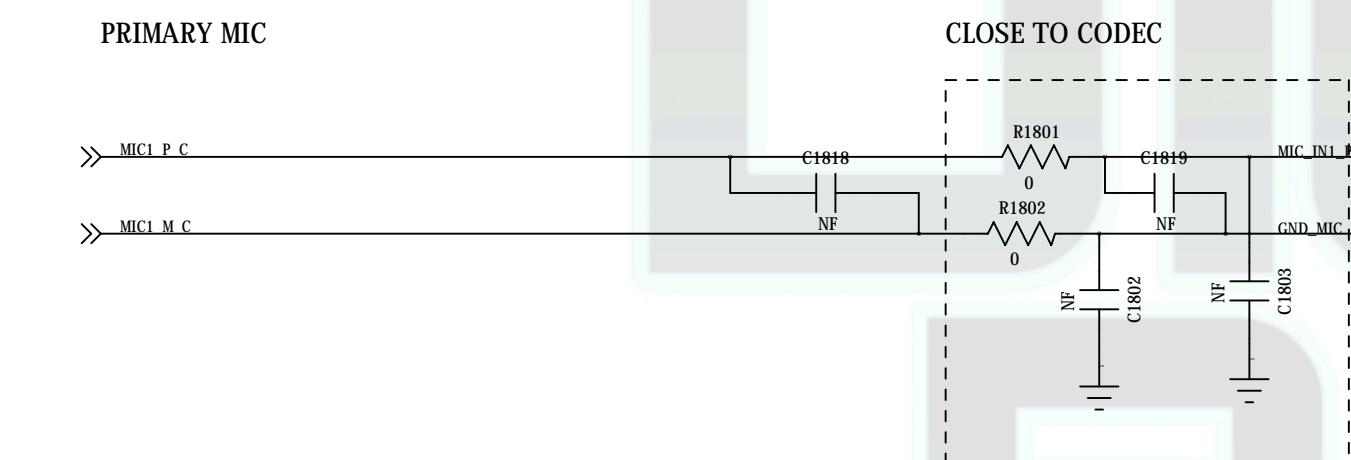
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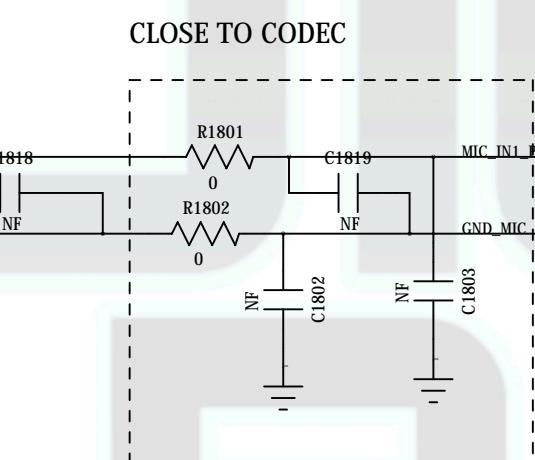
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Date		
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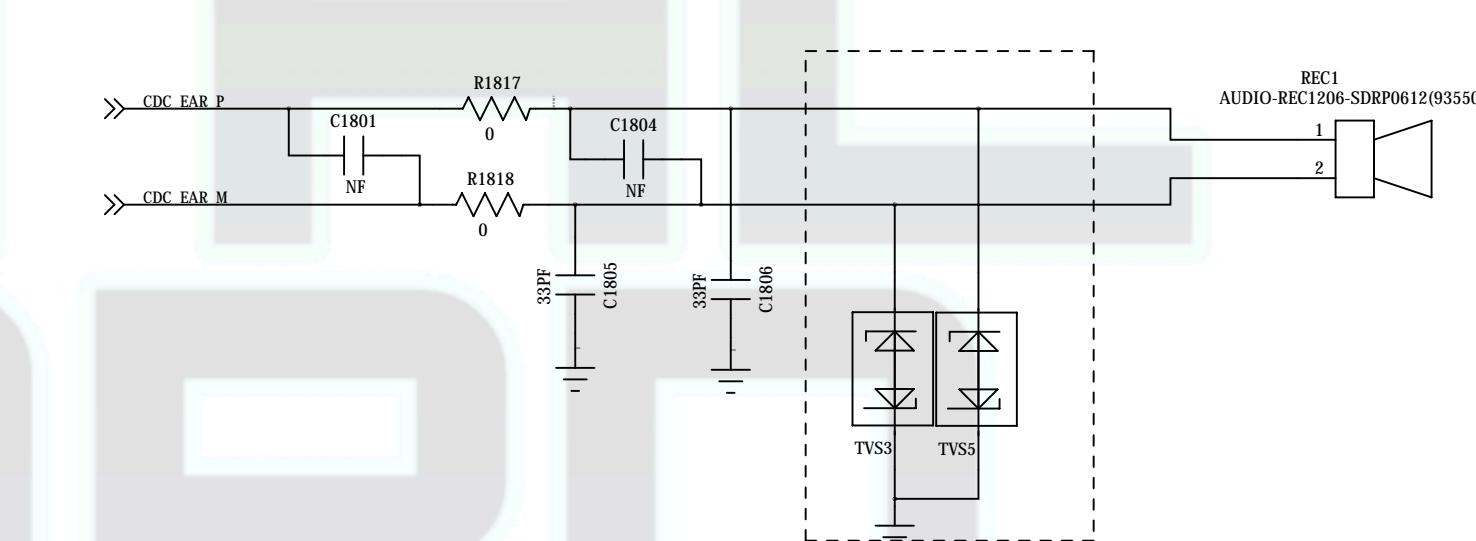
PRIMARY MIC



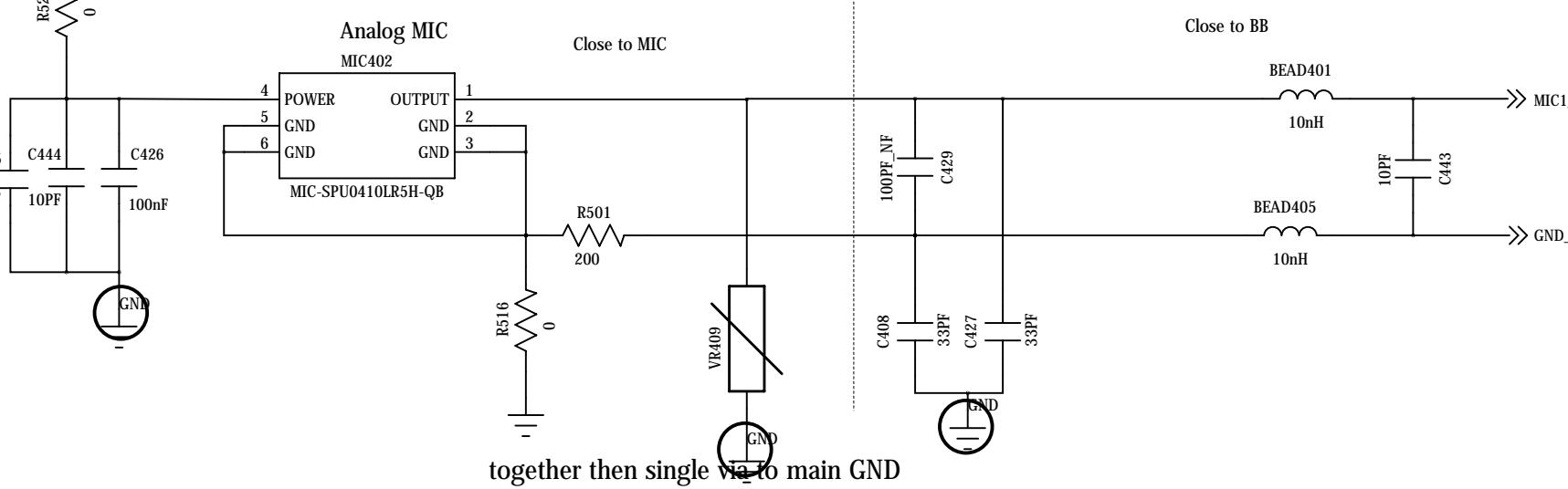
CLOSE TO CODEC



RECEIVER



auxMIC



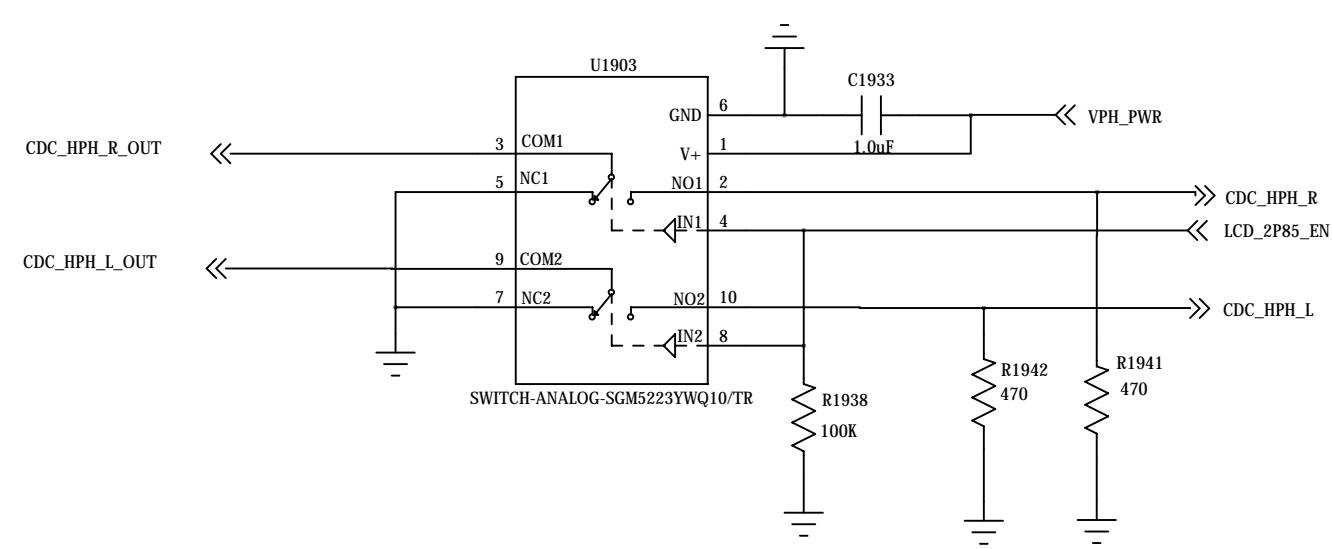
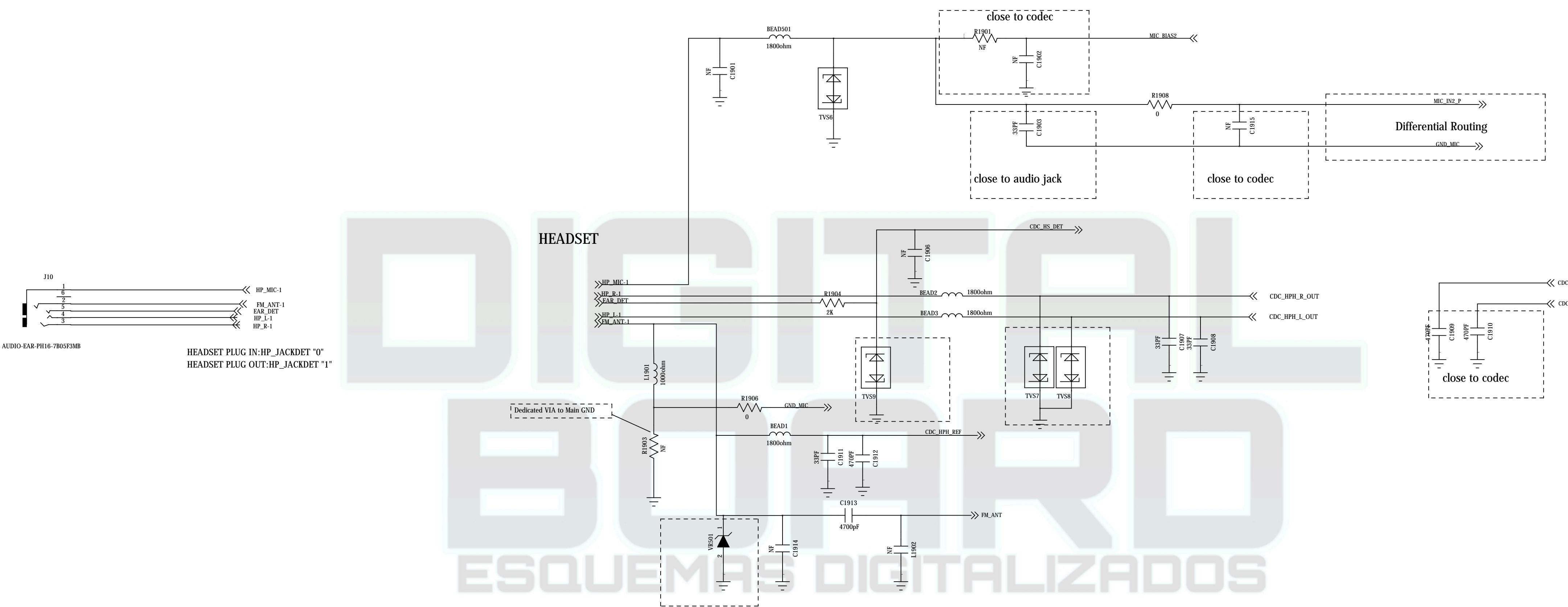
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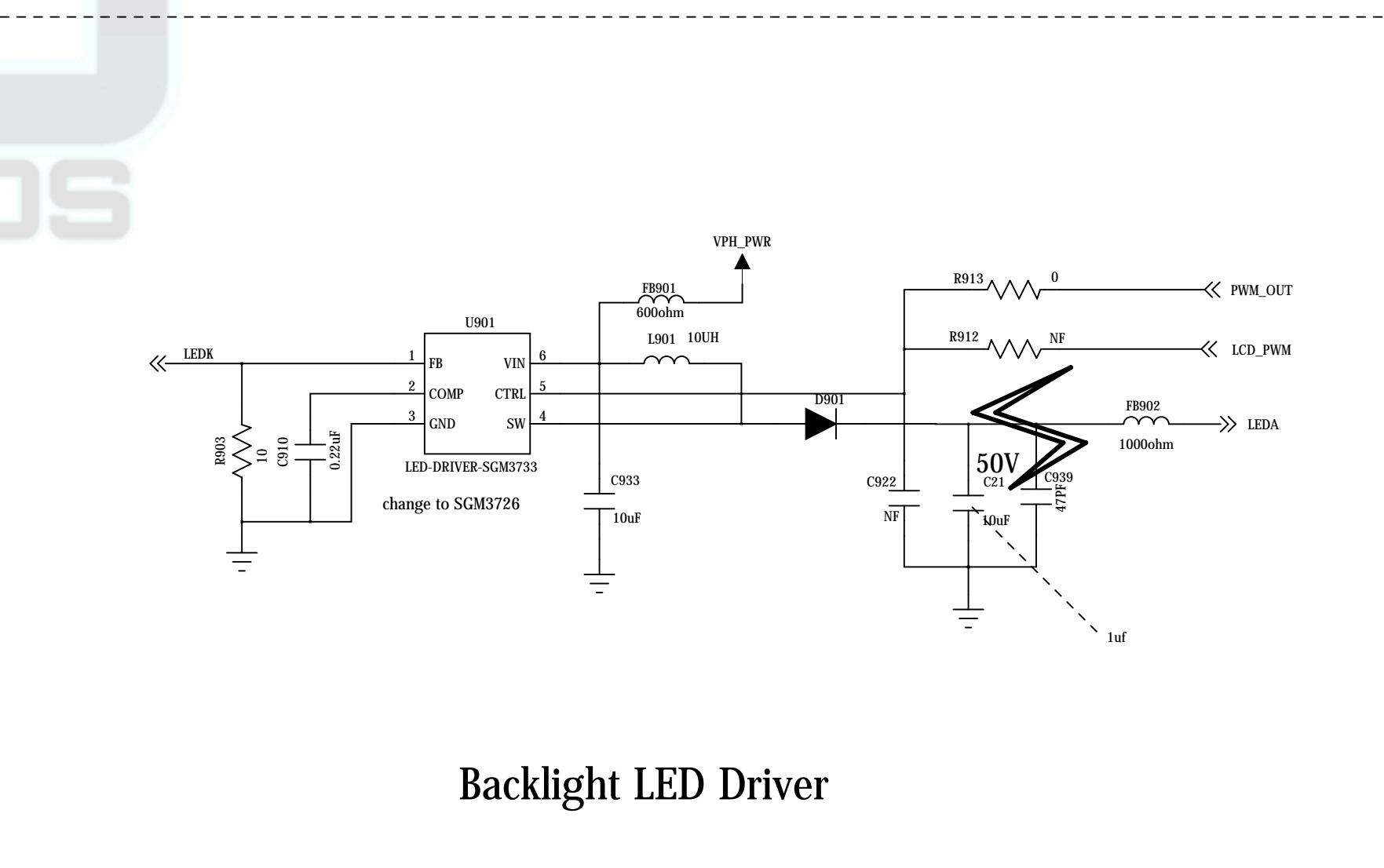
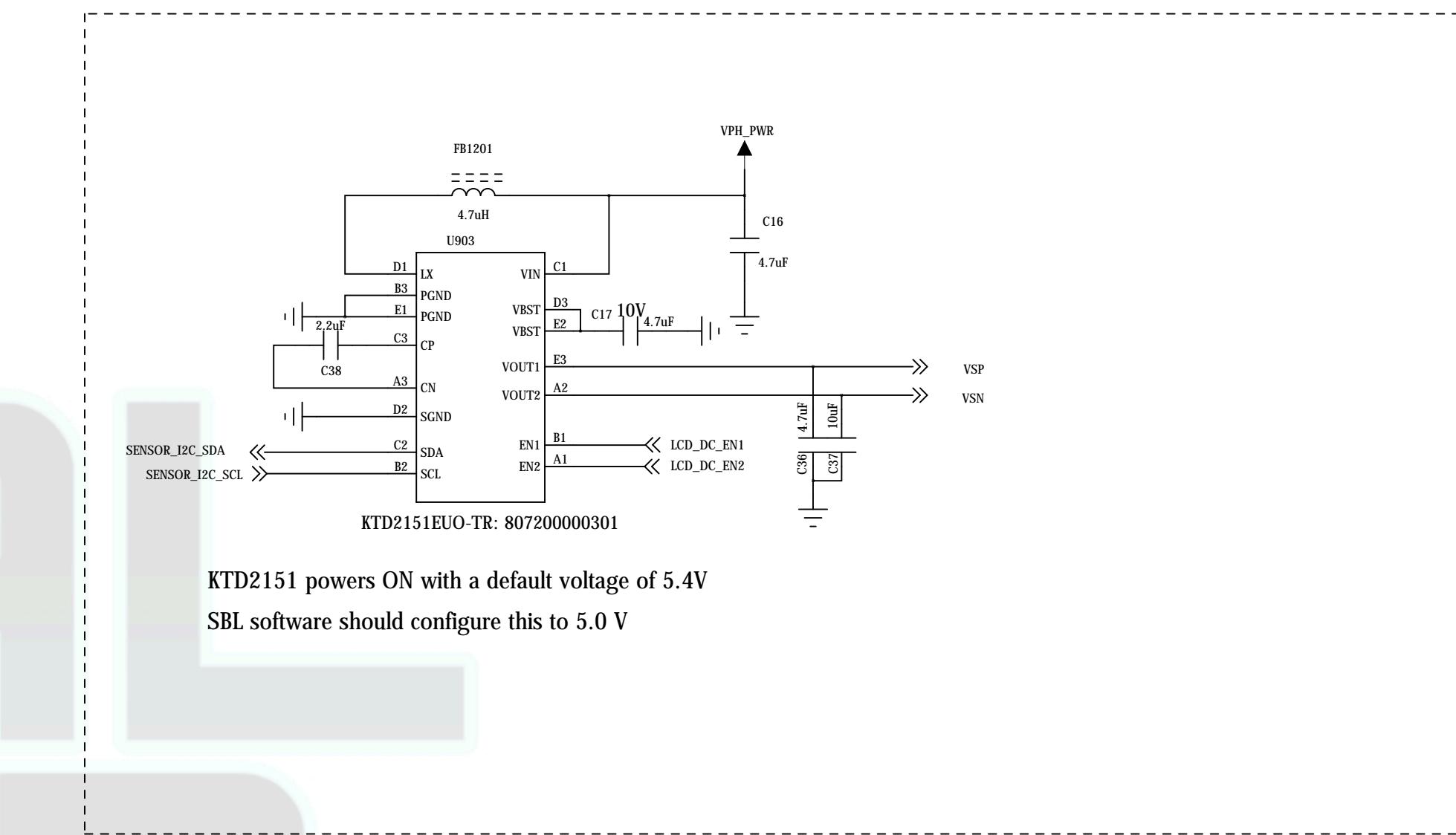
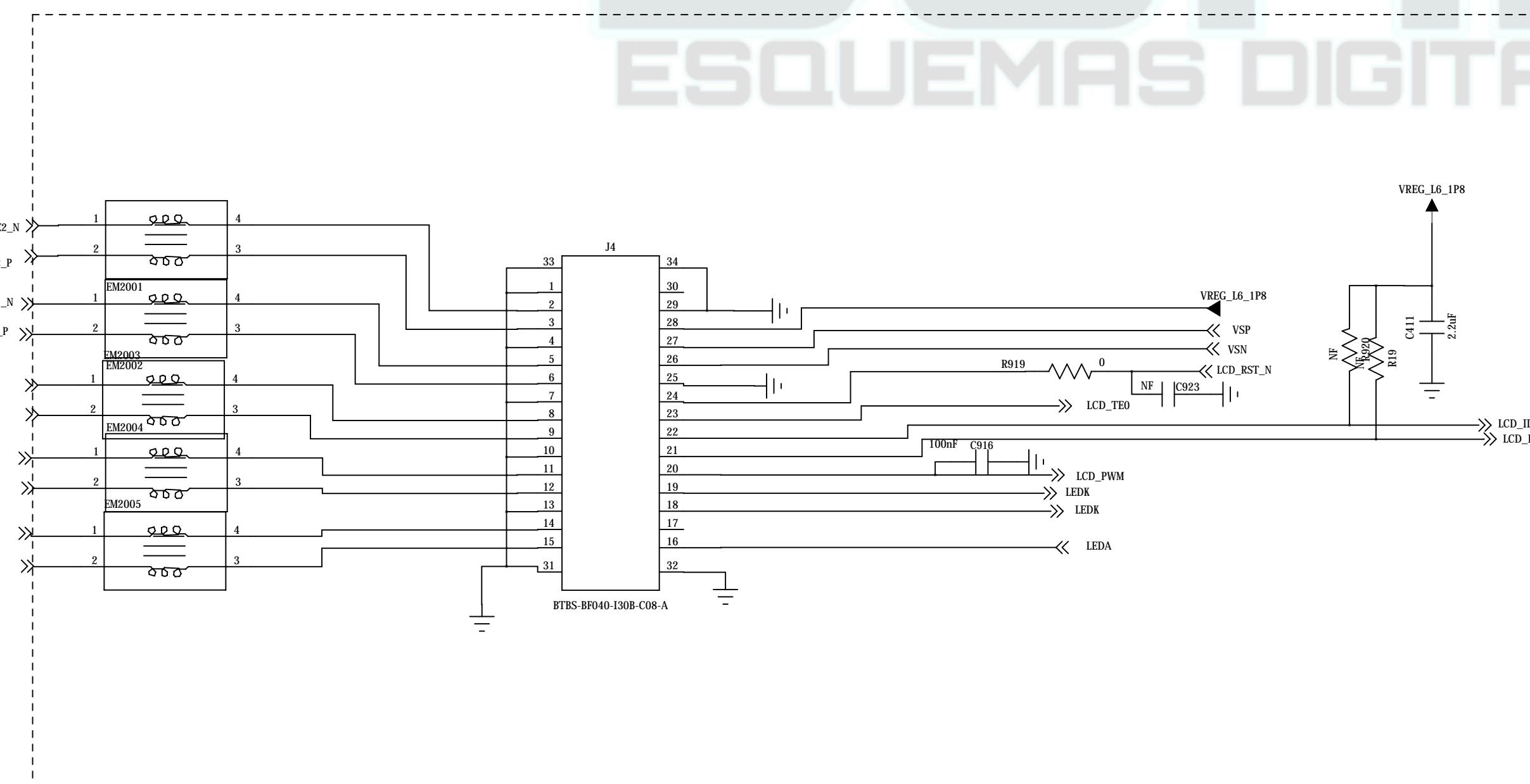
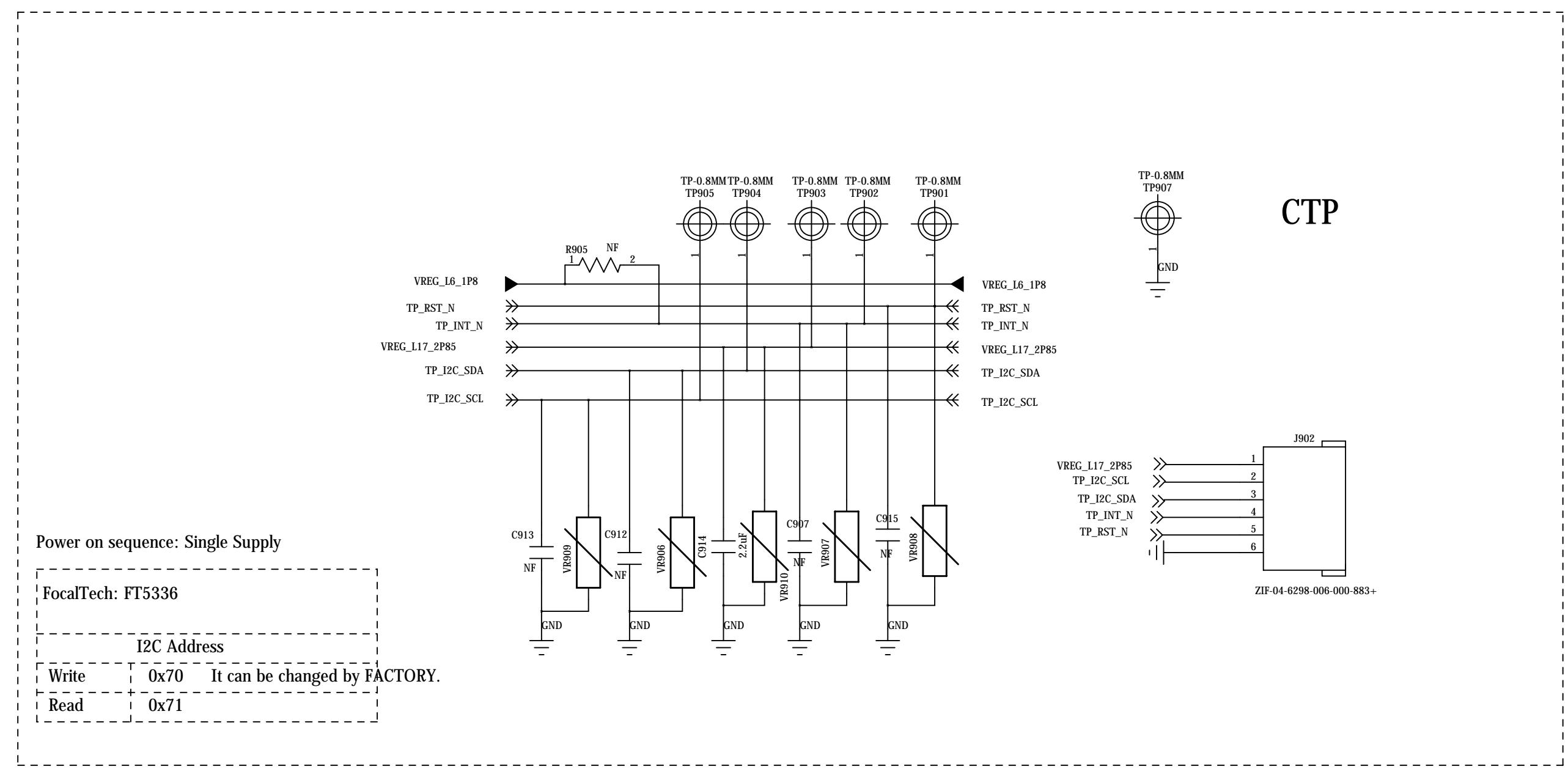
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Date:		
Page	Sheet	of



IN=0, COM Connected to NC;  
IN=1, COM Connected to NO;

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Date _____	Sheet _____ of _____



# Backlight LED Driver

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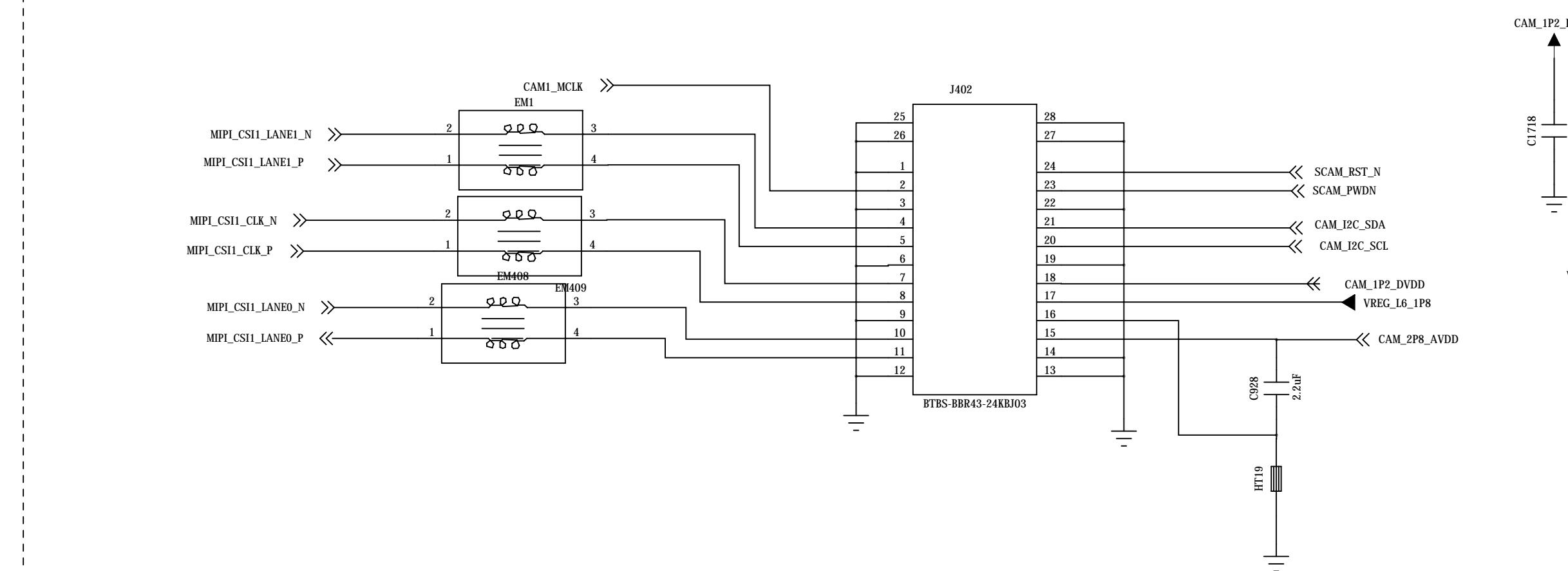
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PIN		
1	GND	
2	MCLK	
3	GND	
4	MDN1	
5	MDP1	
6	GND	
7	MCN	
8	MCP	
9	GND	
10	MDNO	
11	MDPO	
12	GND	
13	GND	
14	GND	
15	AVDD	2.8V
16	GND	
17	DVDD	1.8V
18	DVDD	1.2V
19	GND	
20	SCL	
21	SDA	
22	GND	
23	PWDN	
24	RESET	

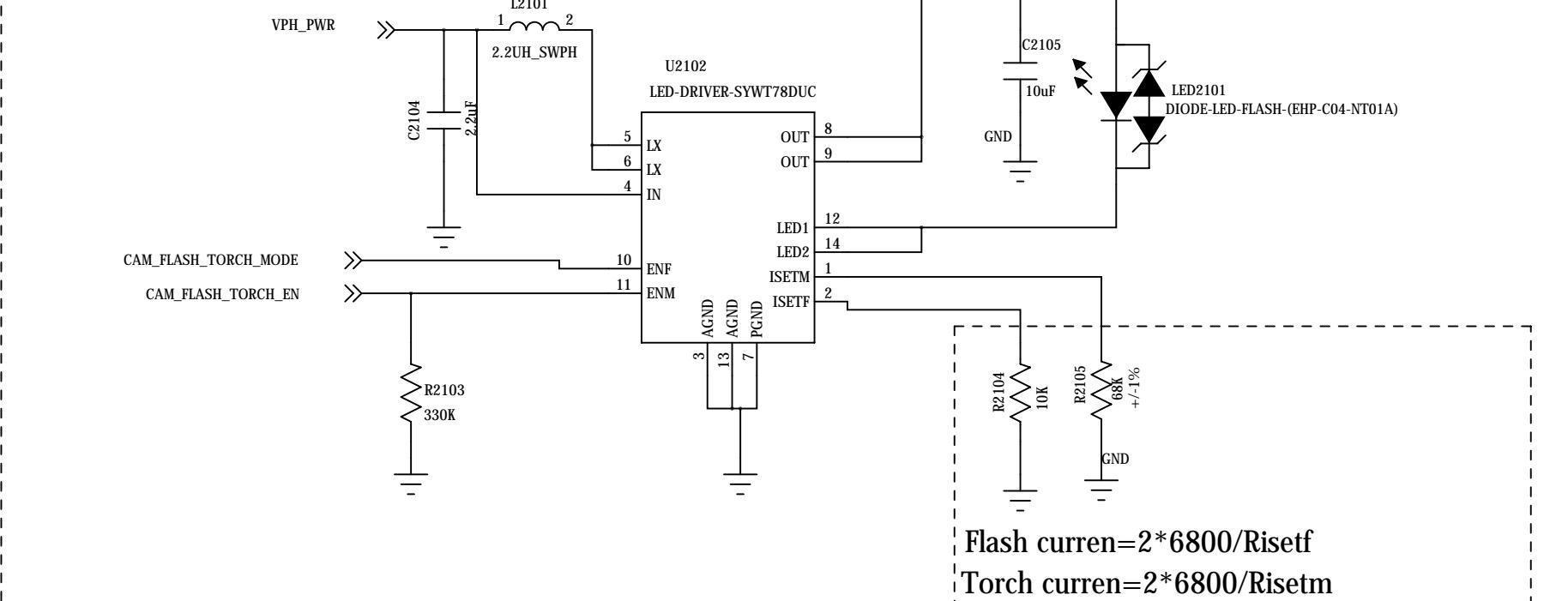
## Sub Camera



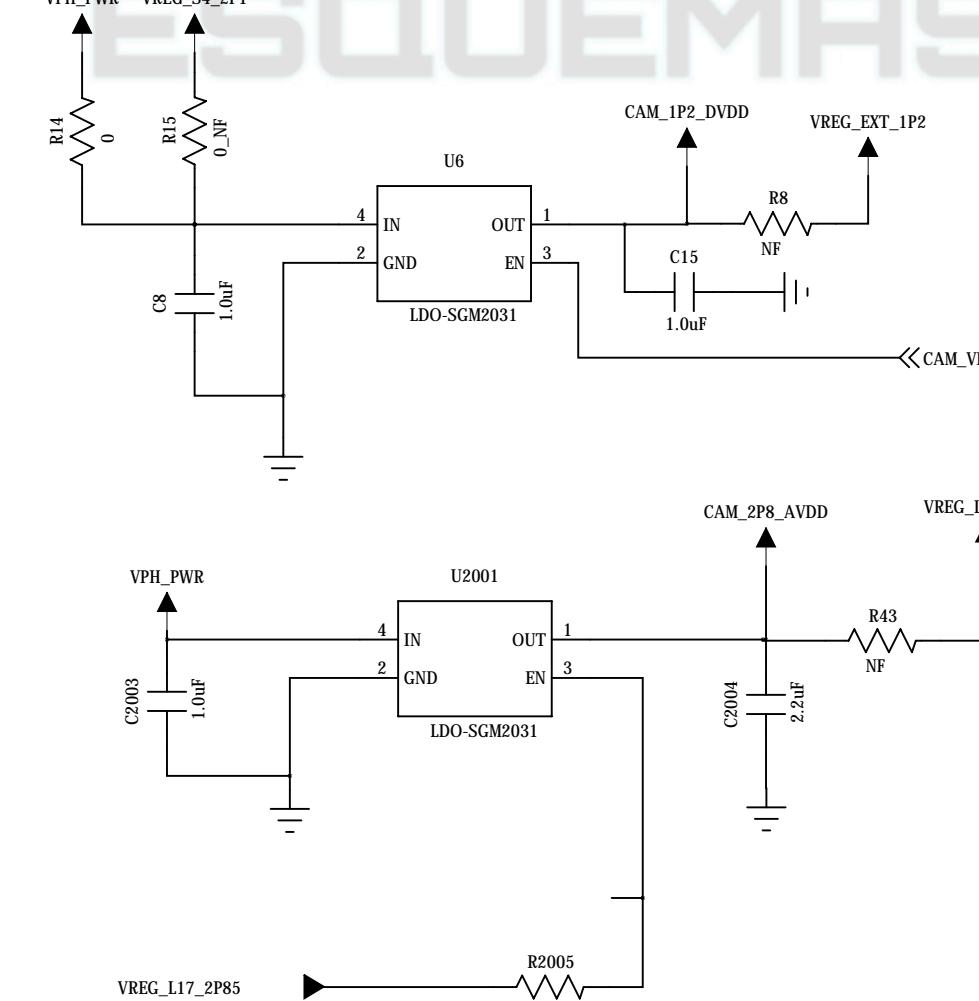
# FRONT\\_camera

Main Camera / Sub Camera share power domain design  
should double check the voltage level is compatible

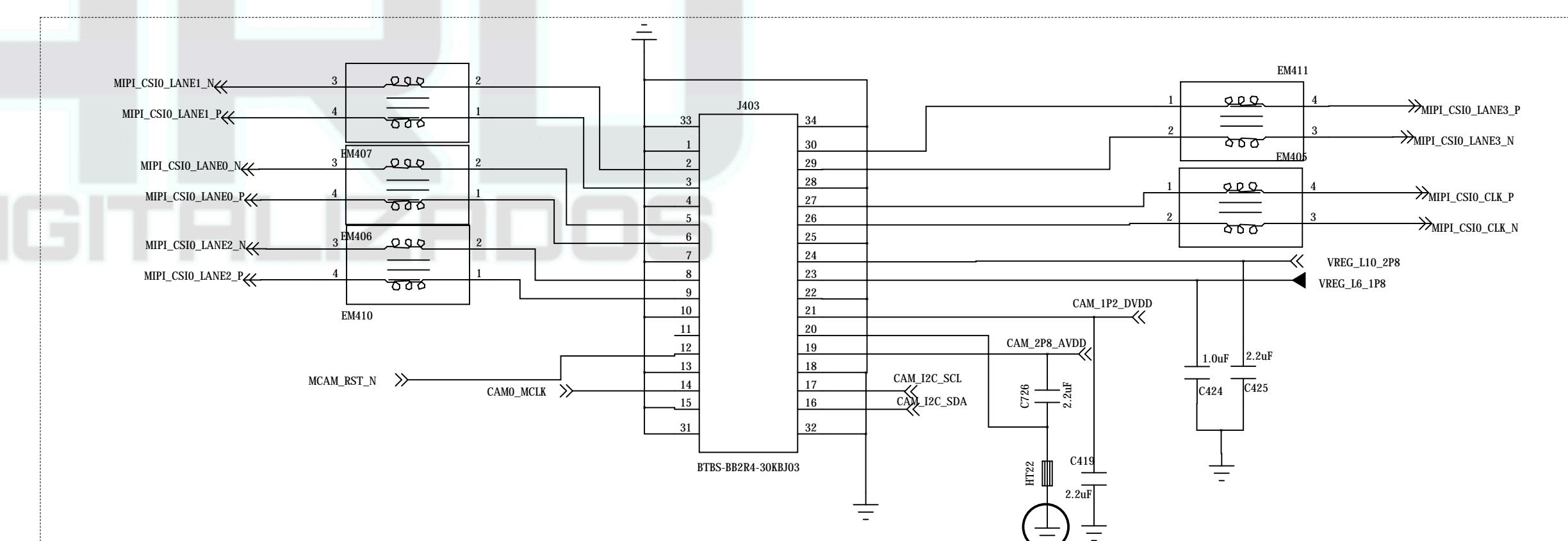
# FLASH LED DRIVER



Flash curren=2\*6800/Risetf  
Torch curren=2\*6800/Risetz



Main Camera / Sub Camera share power domain design  
should double check the voltage level is compatible



# Main Camera

Rear Camera: 8Mp	I2C Address
Module:	Write             0x6C
Sensor: OV8865	Read             0x6D
Power on sequence: L6(DOVDD) must before L17(AVDD)	

Power on sequence: L6(DOVDD) must before L17(AVDD)

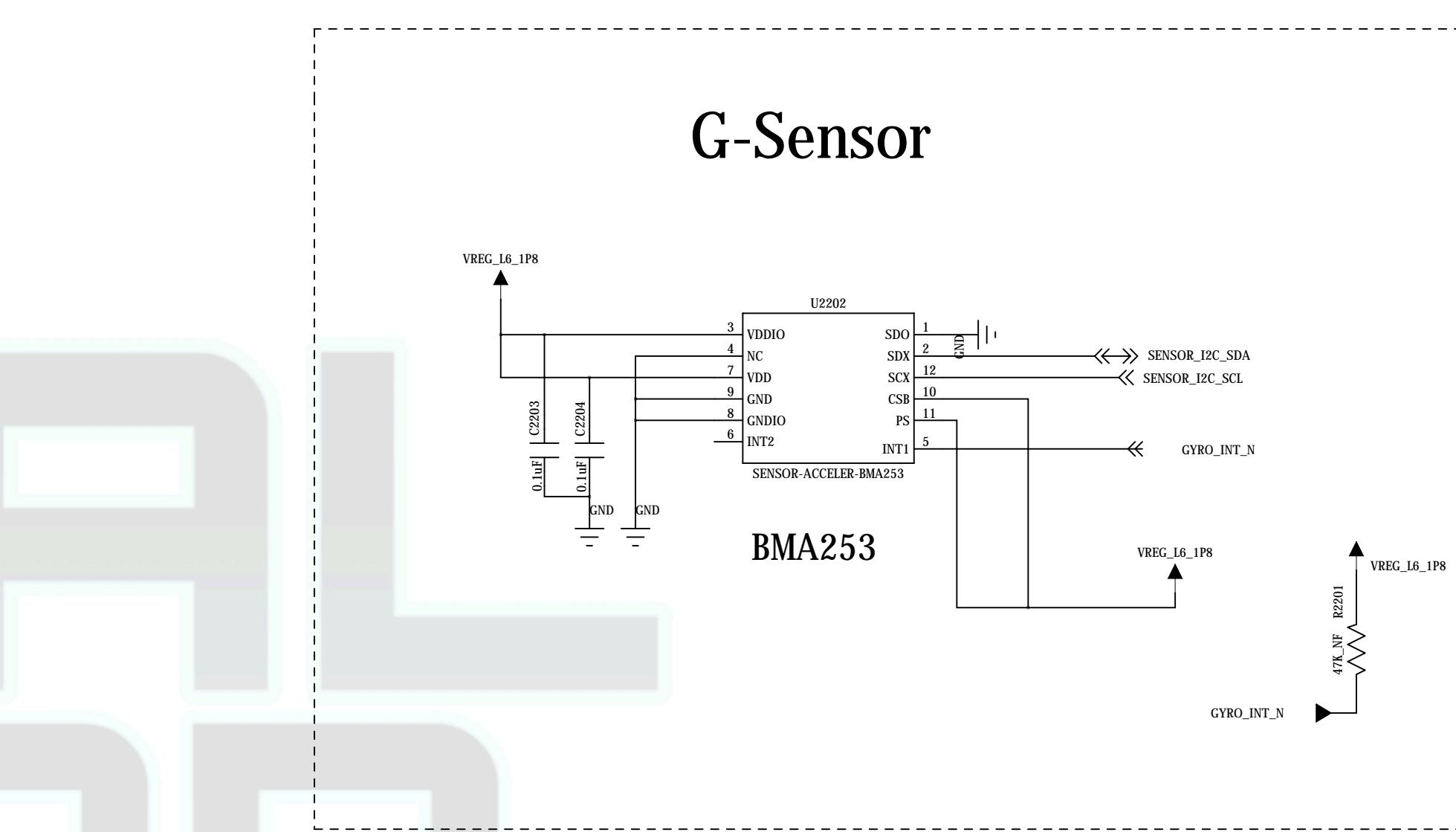
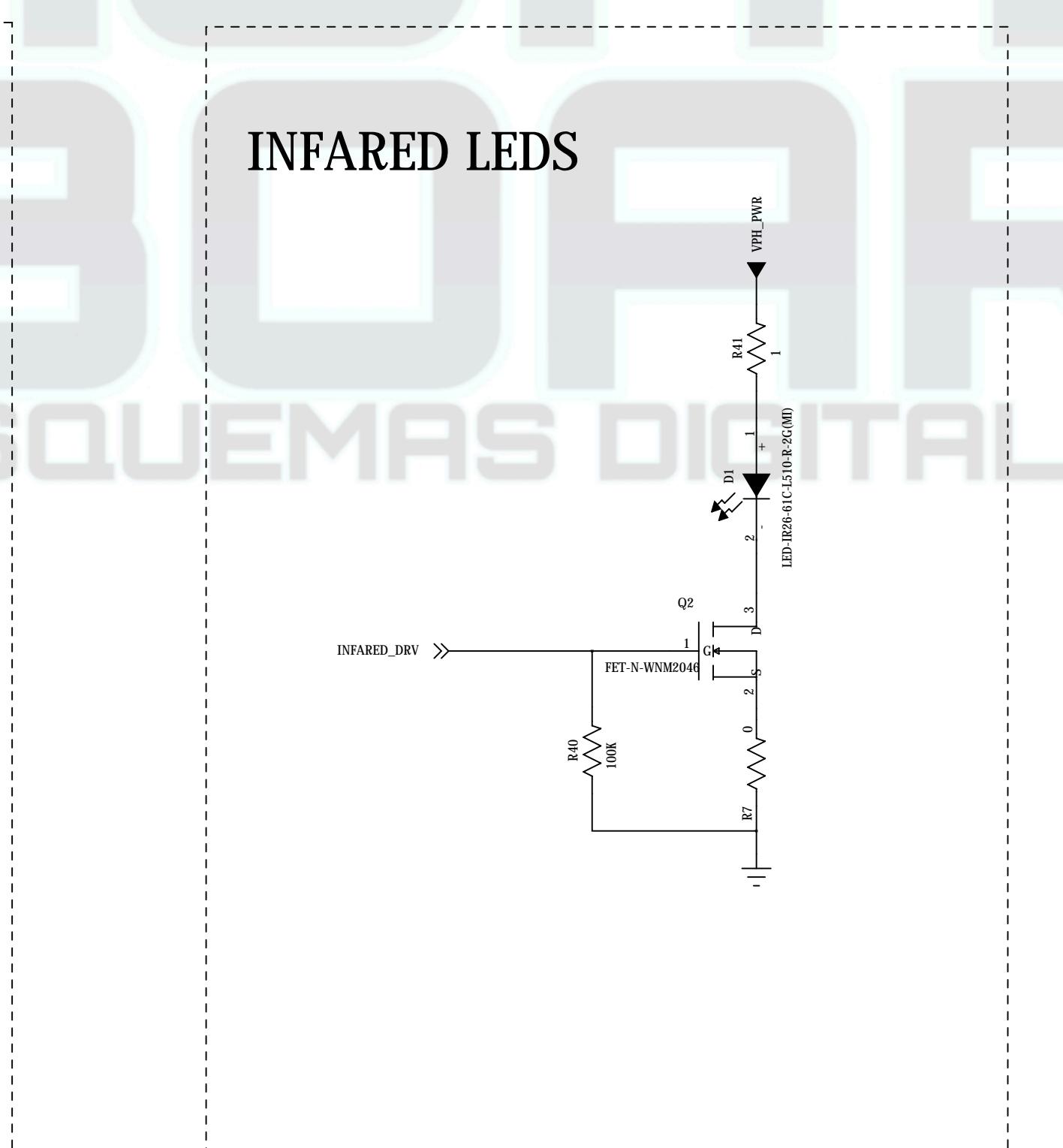
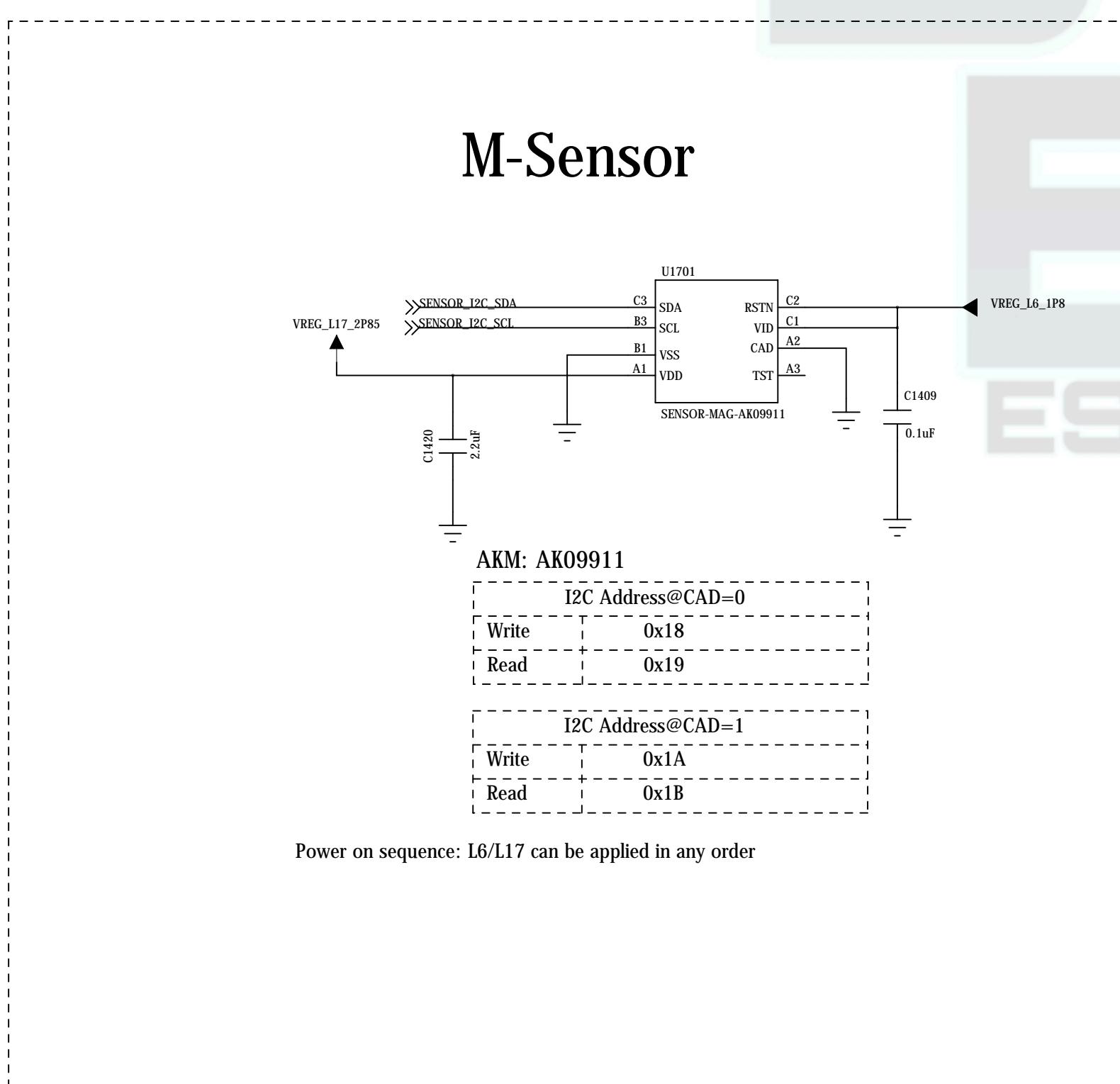
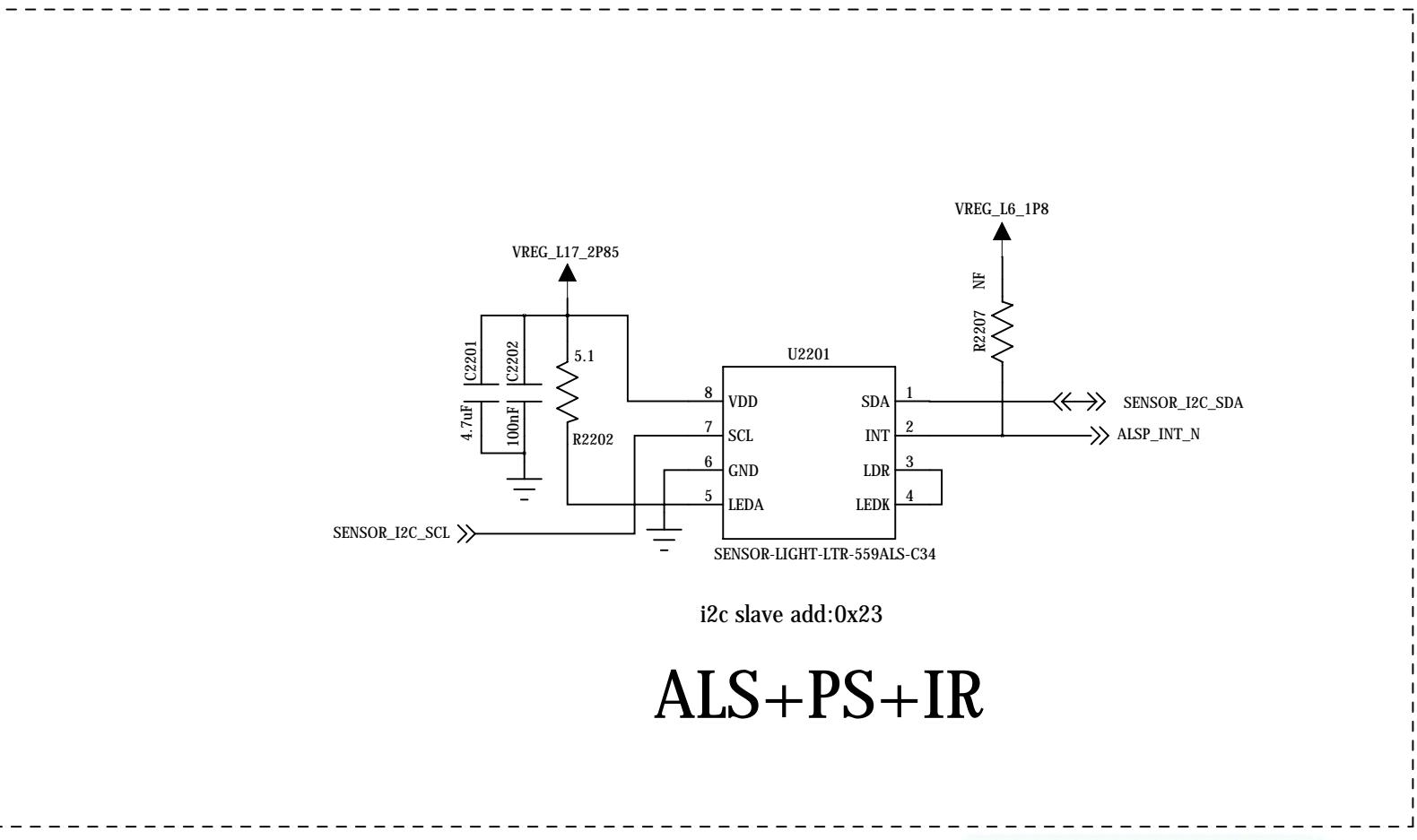
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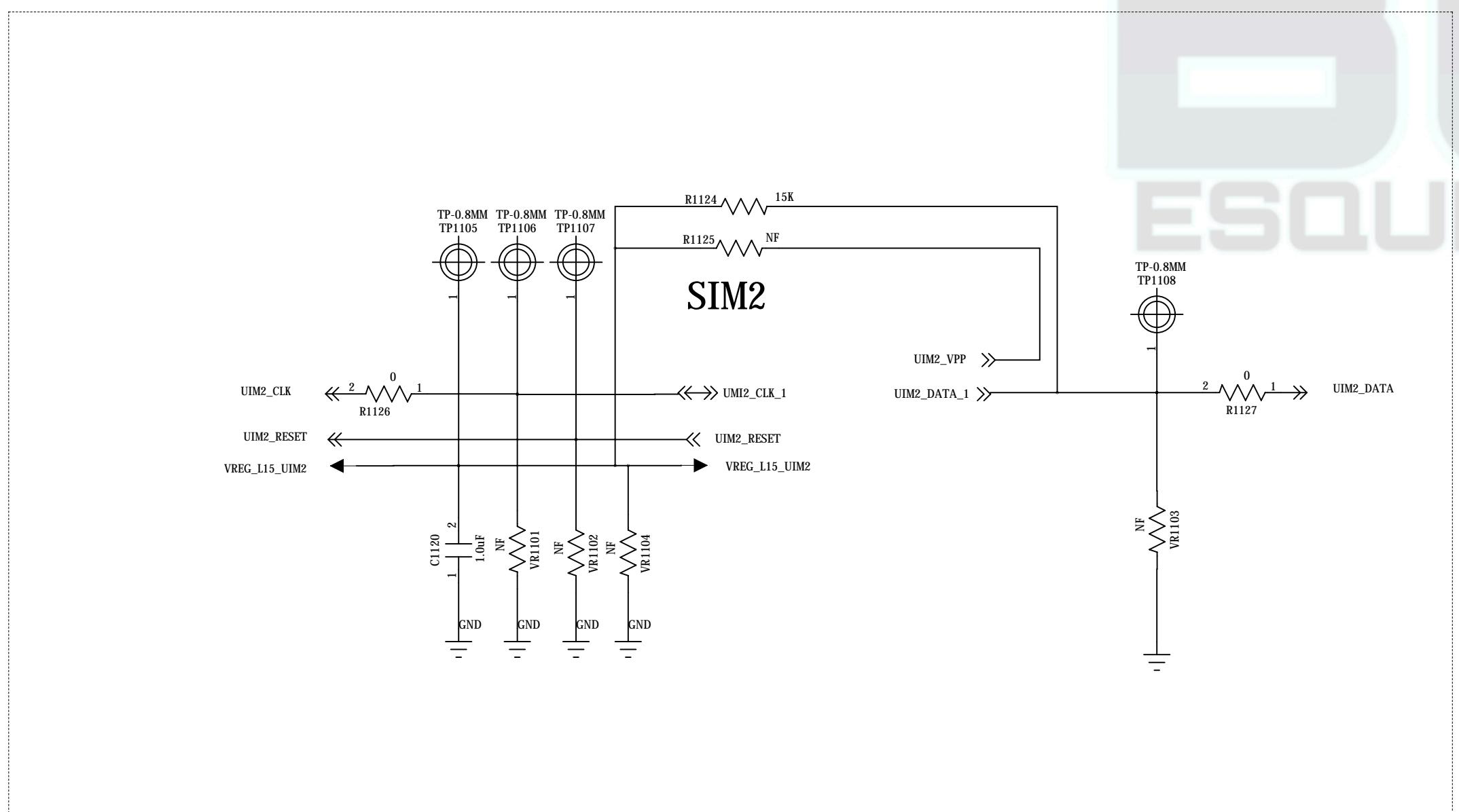
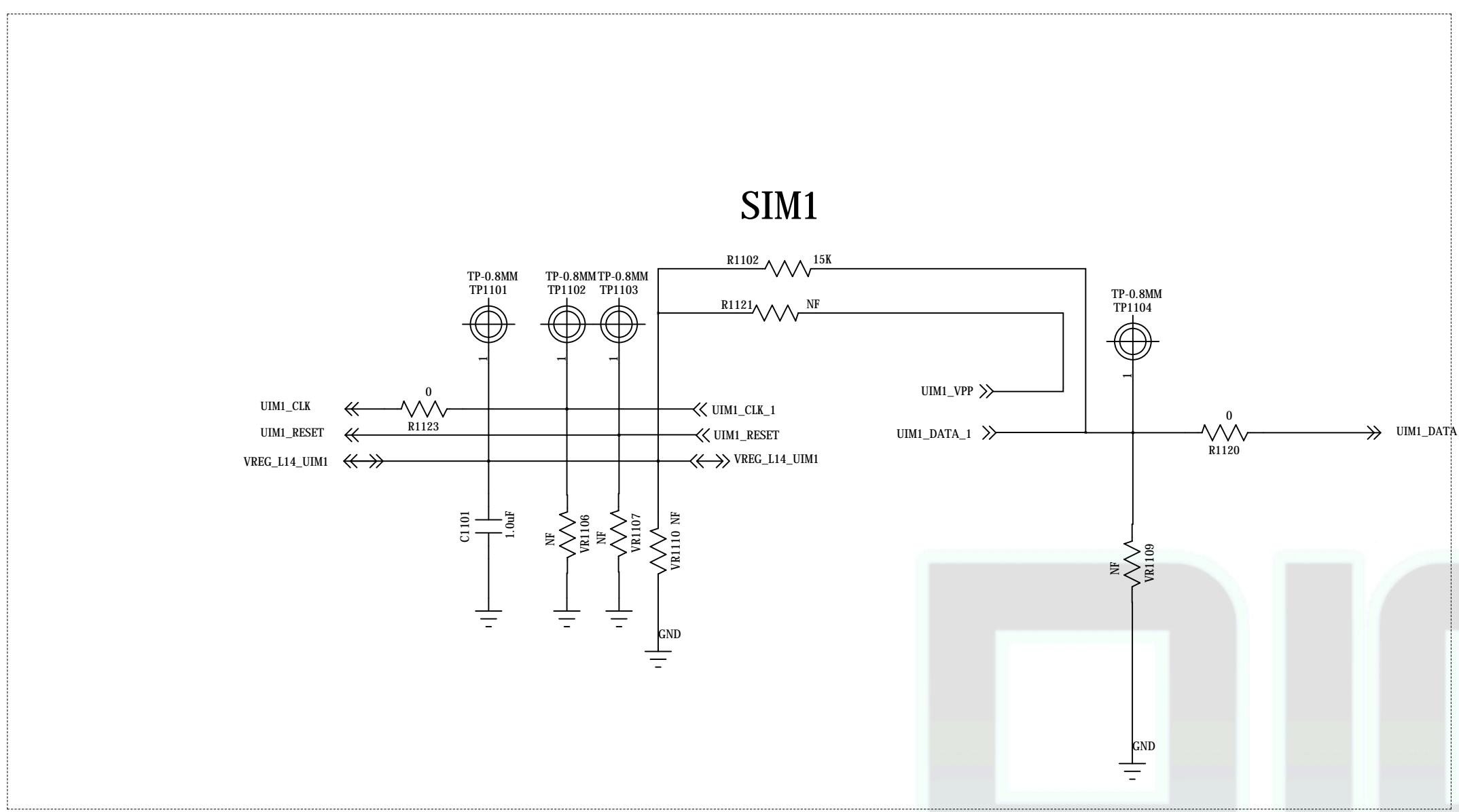
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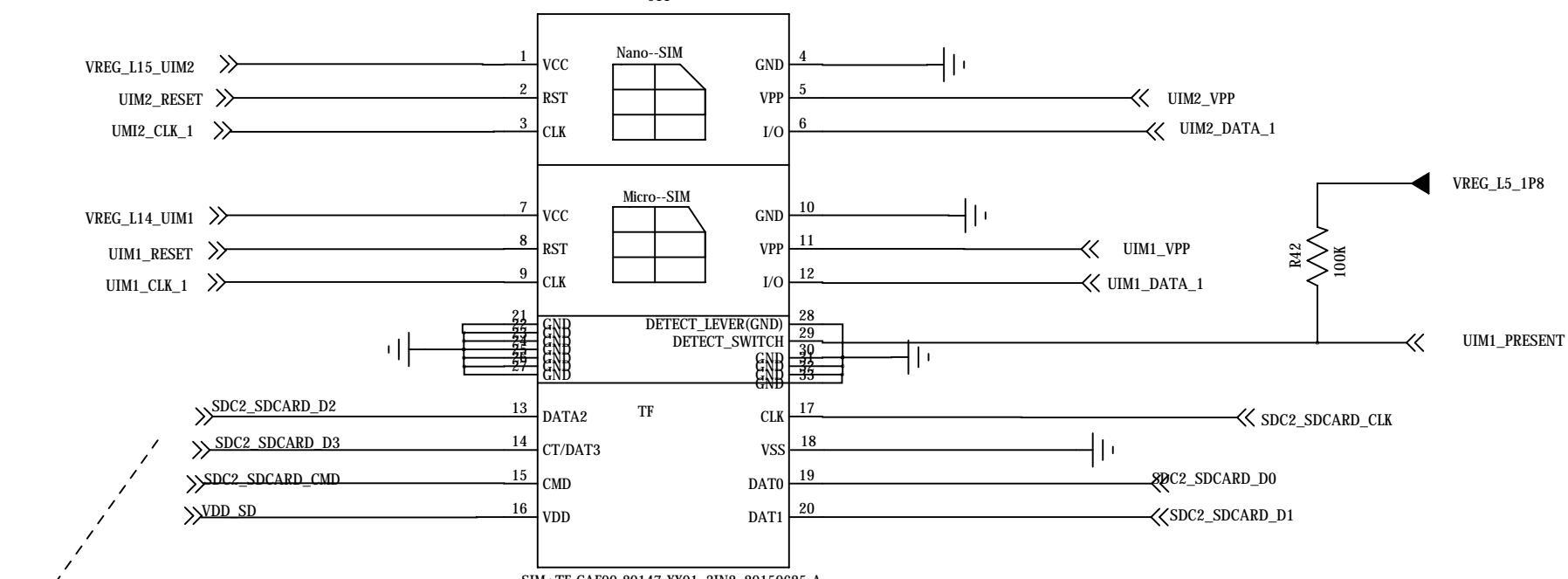
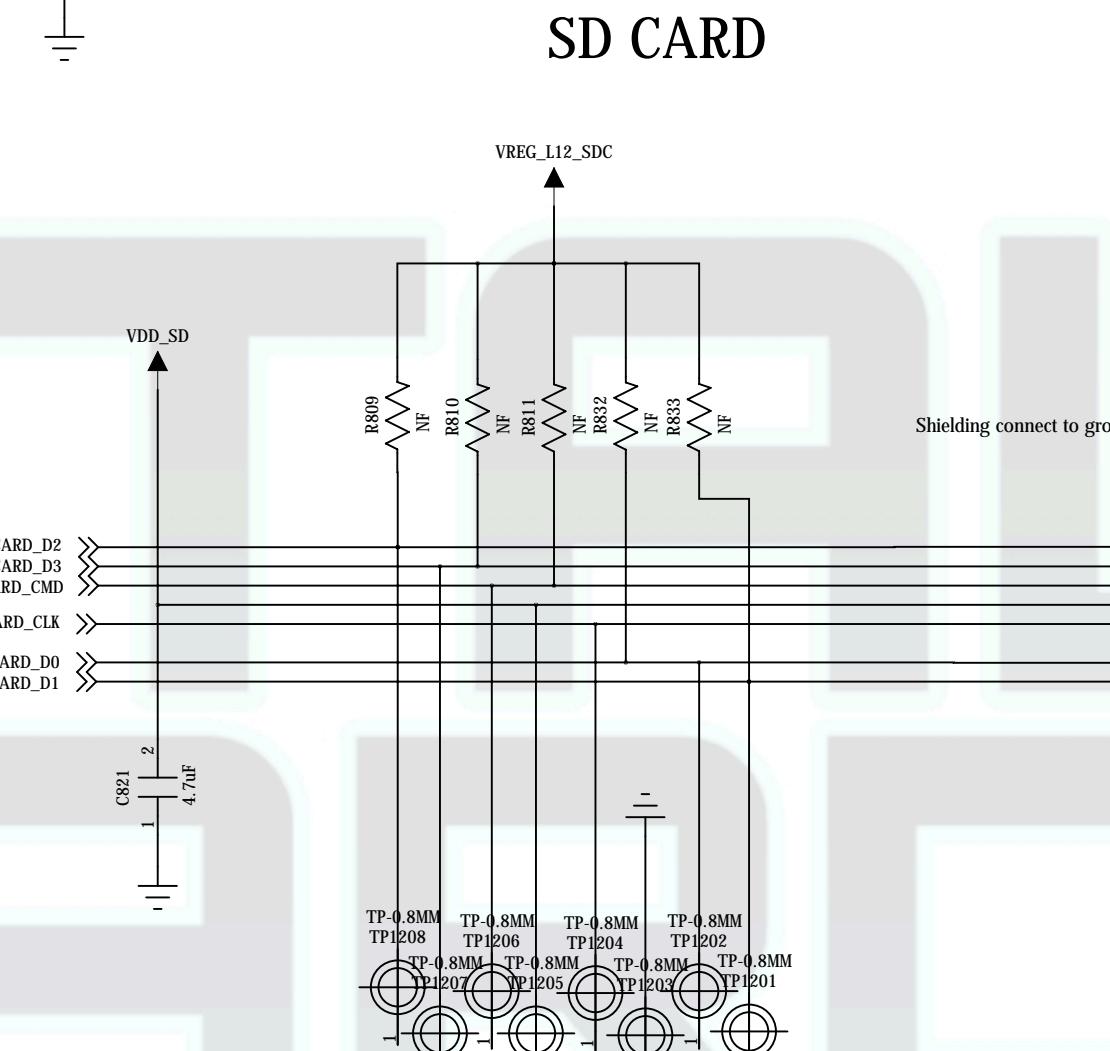
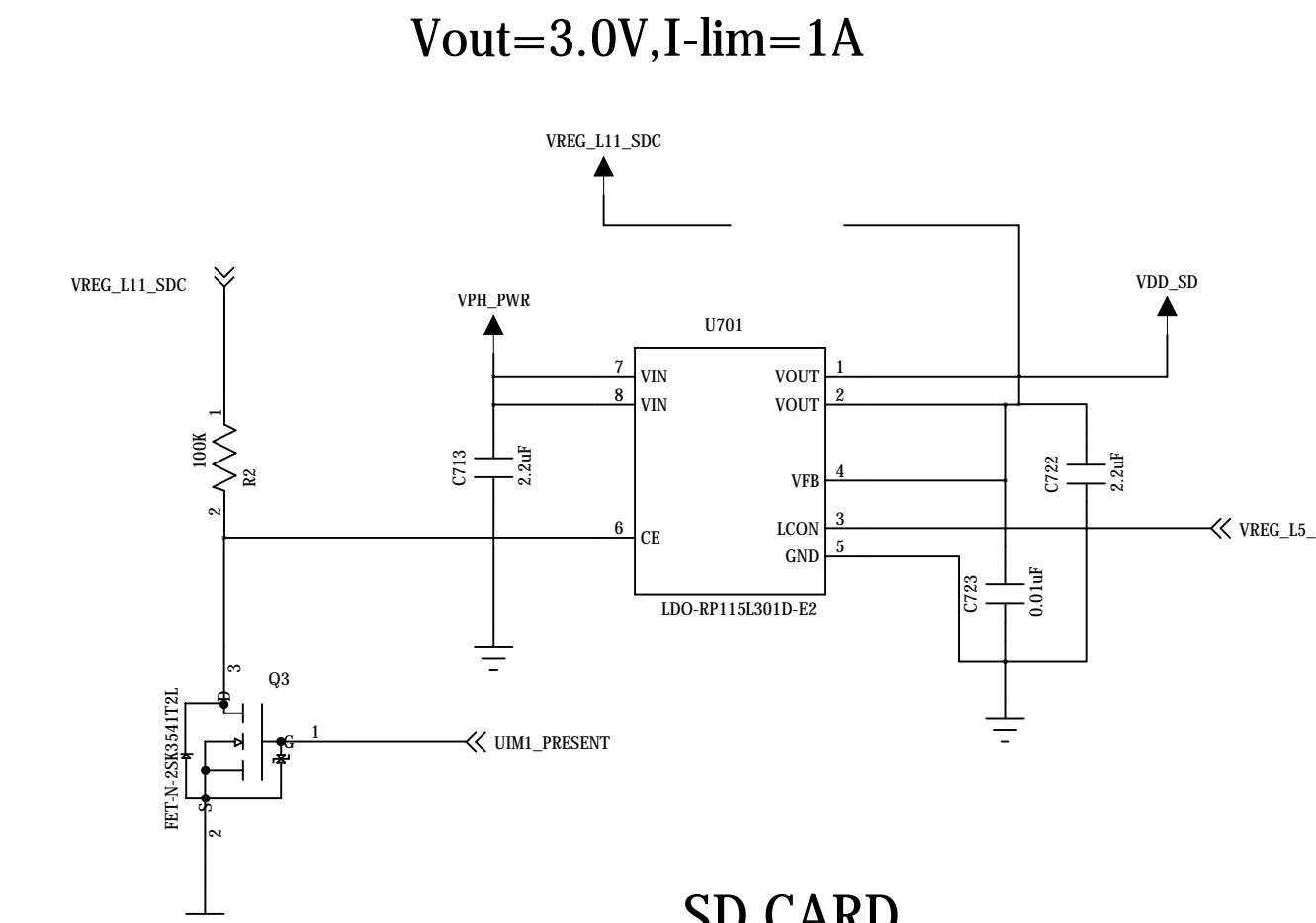


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This int should give to GPIO38/GPIO56/GPIO60



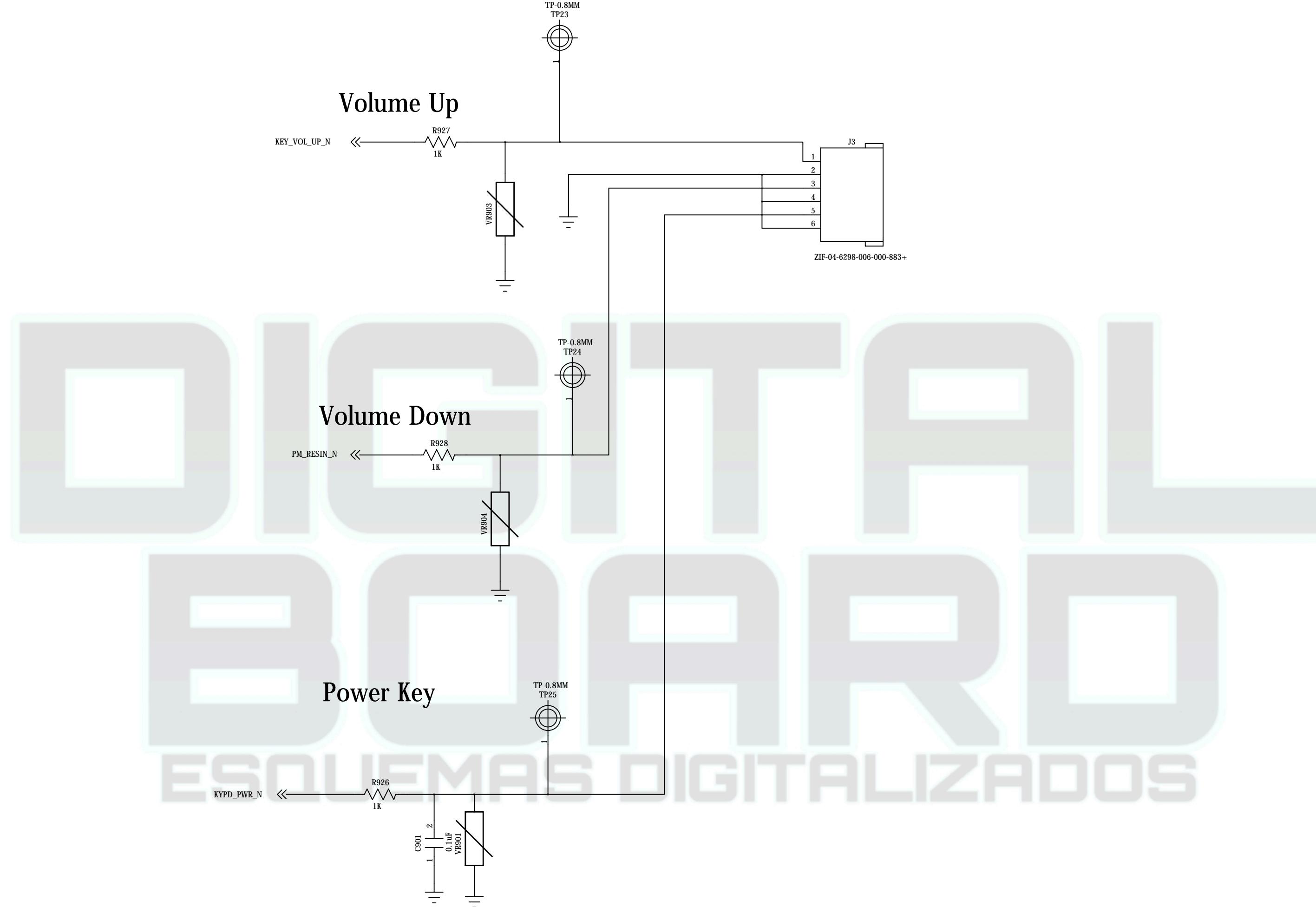
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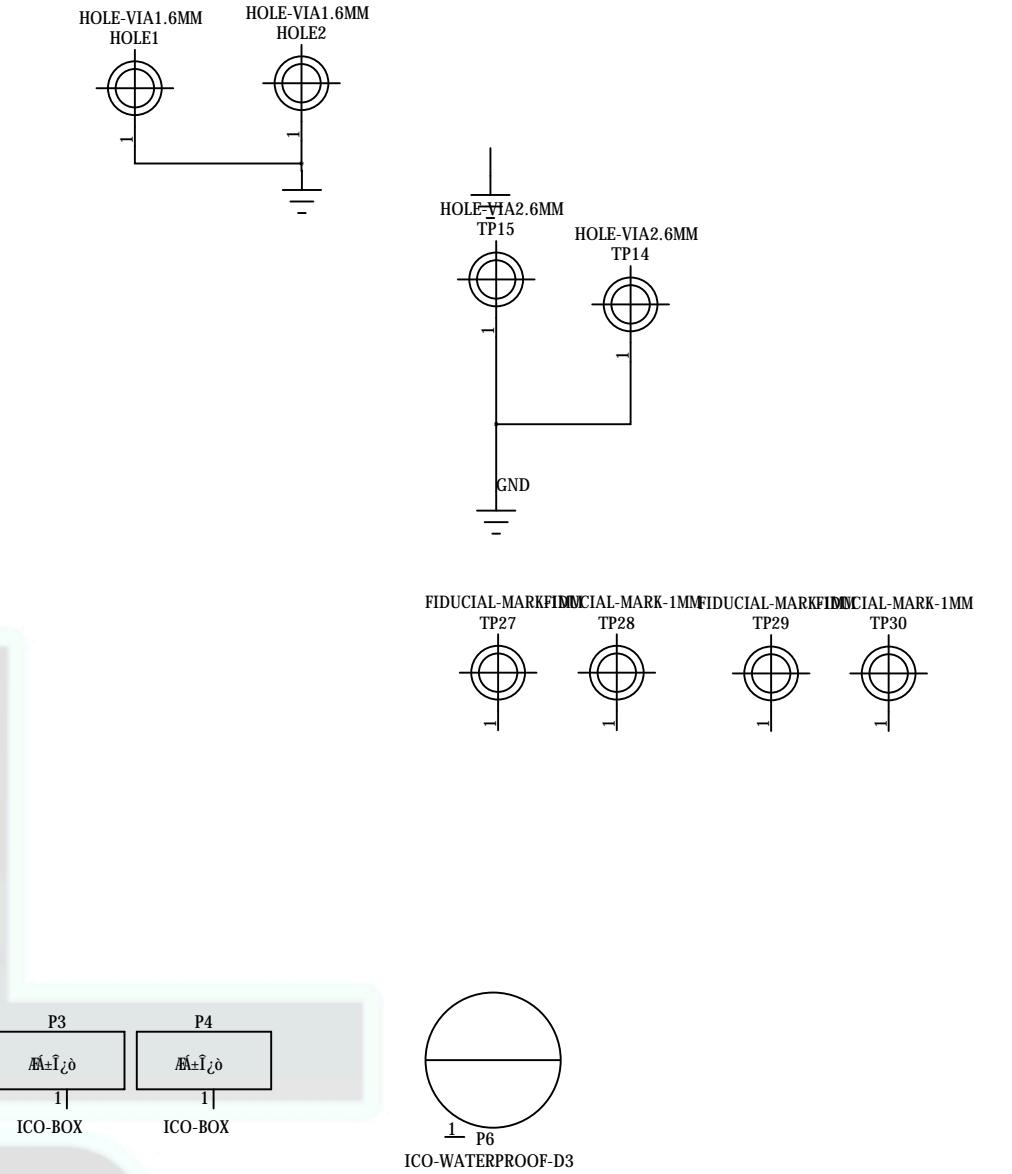
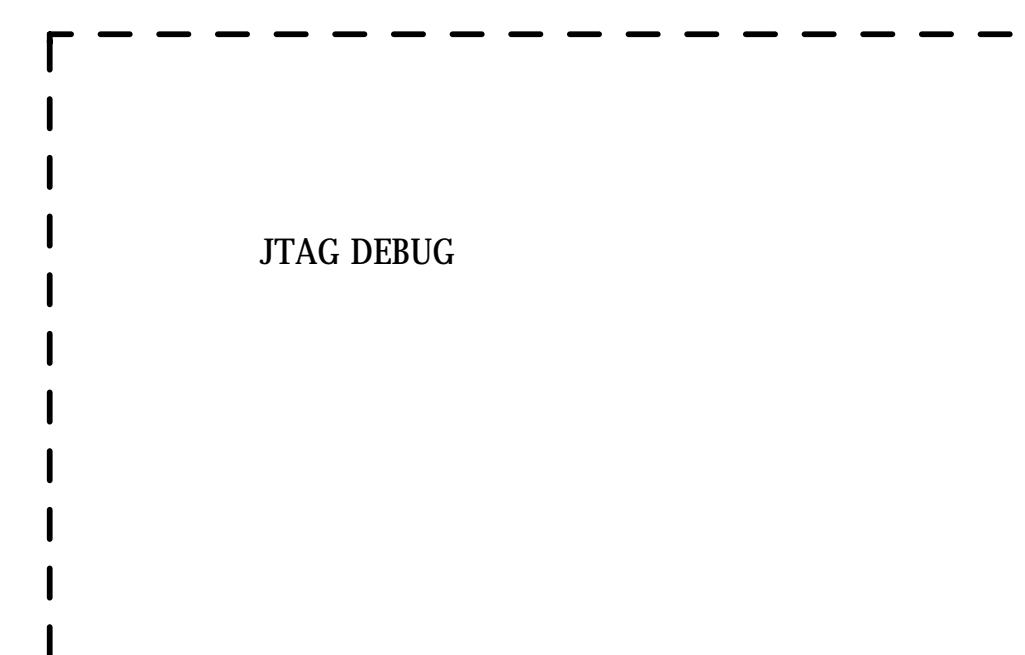
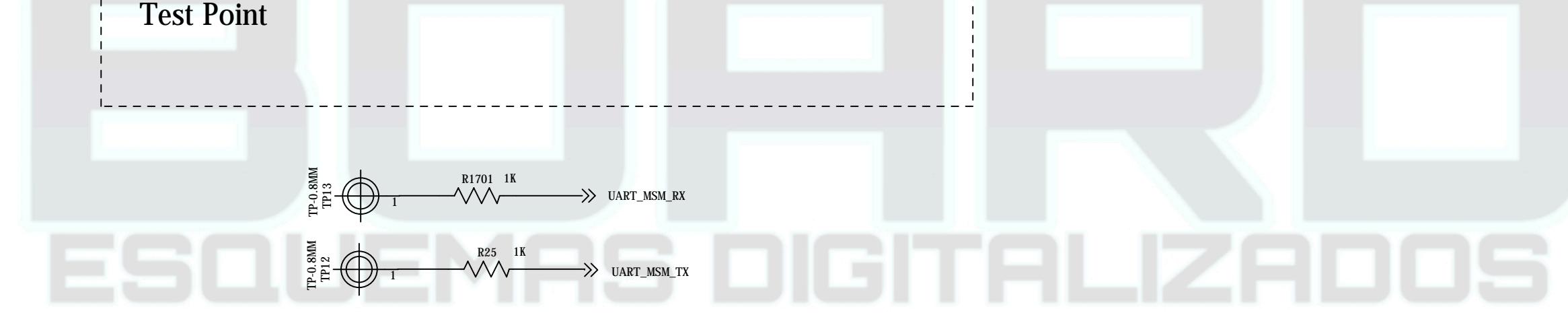
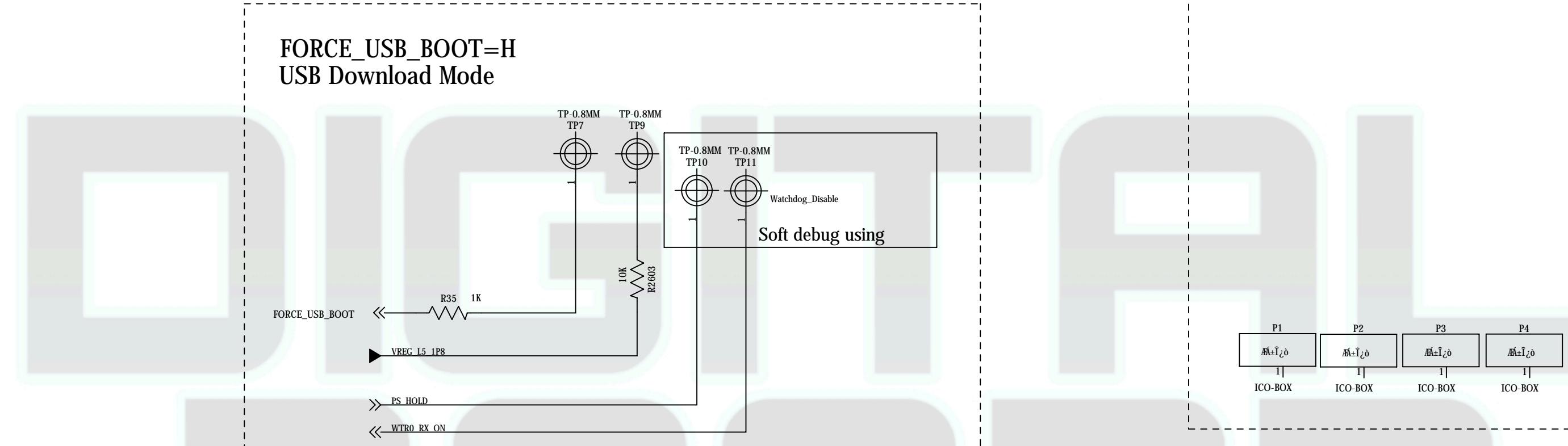
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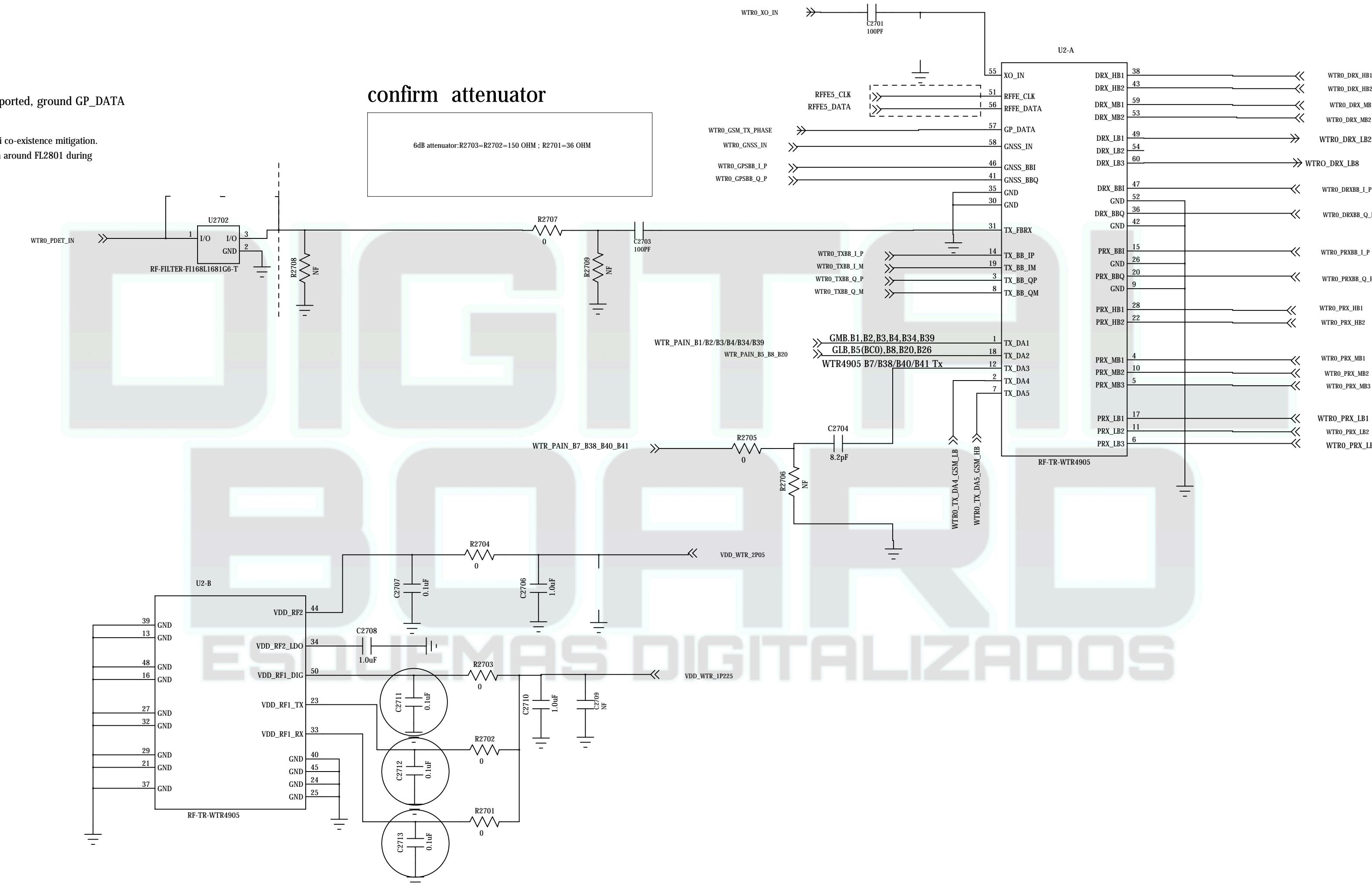
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Size	Sheet Name	Rev
Date:	Sheet	of

WTR4905 CONTROL, PWR & GN

If GSM is not supported, ground GP\_DATA

Note: FL2801 is a 5GHz LPF for Wi-Fi co-existence mitigation.  
Recommend a bypass option around FL2801 during evaluation until proven.



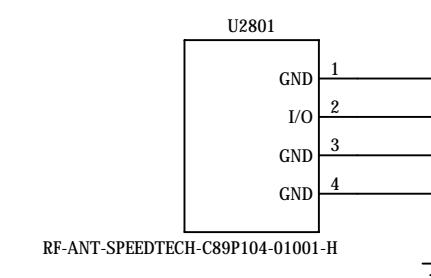
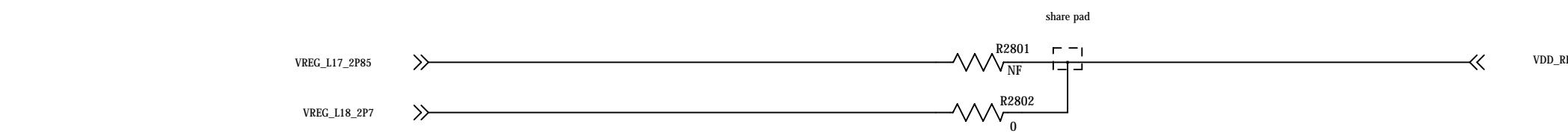
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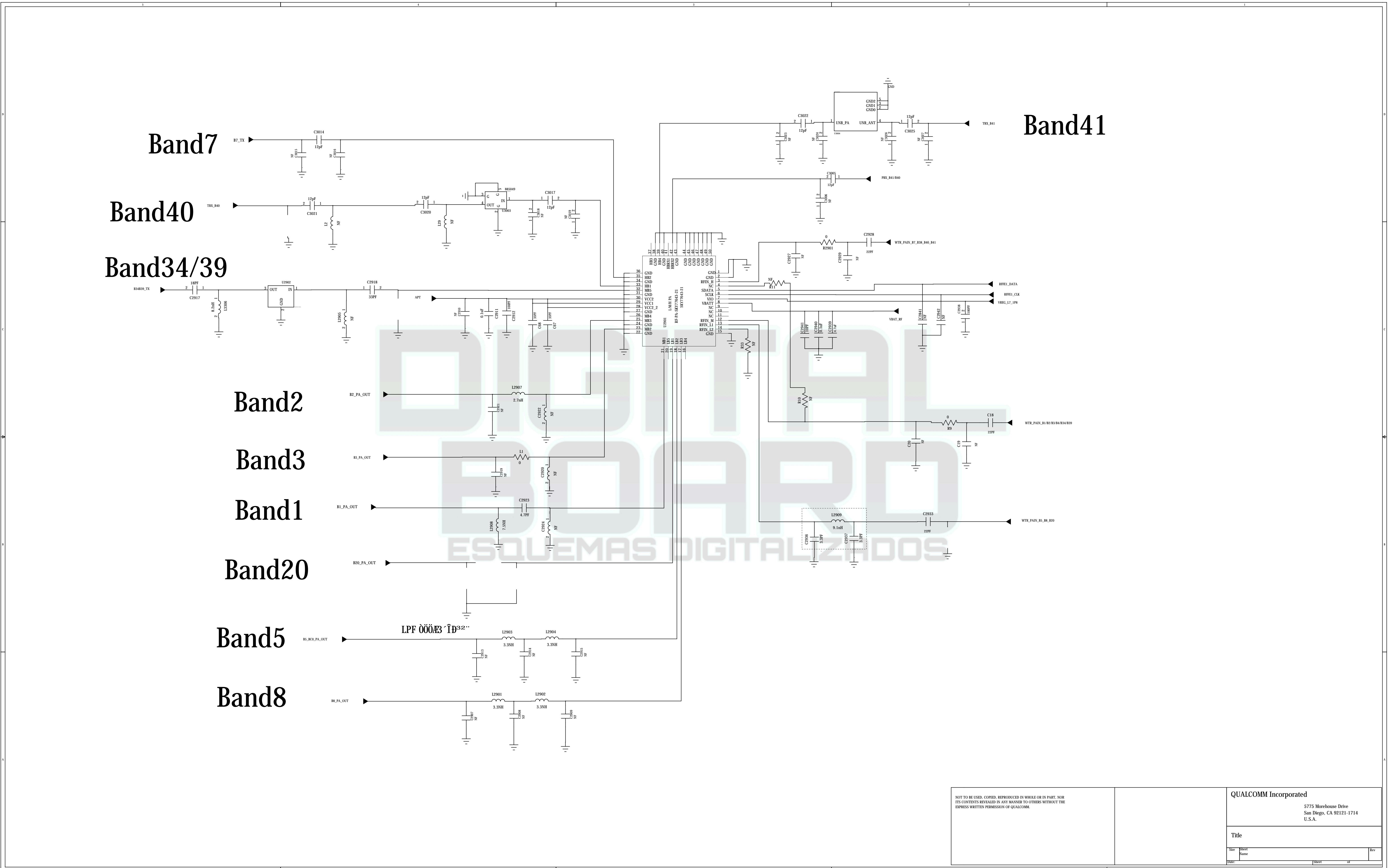


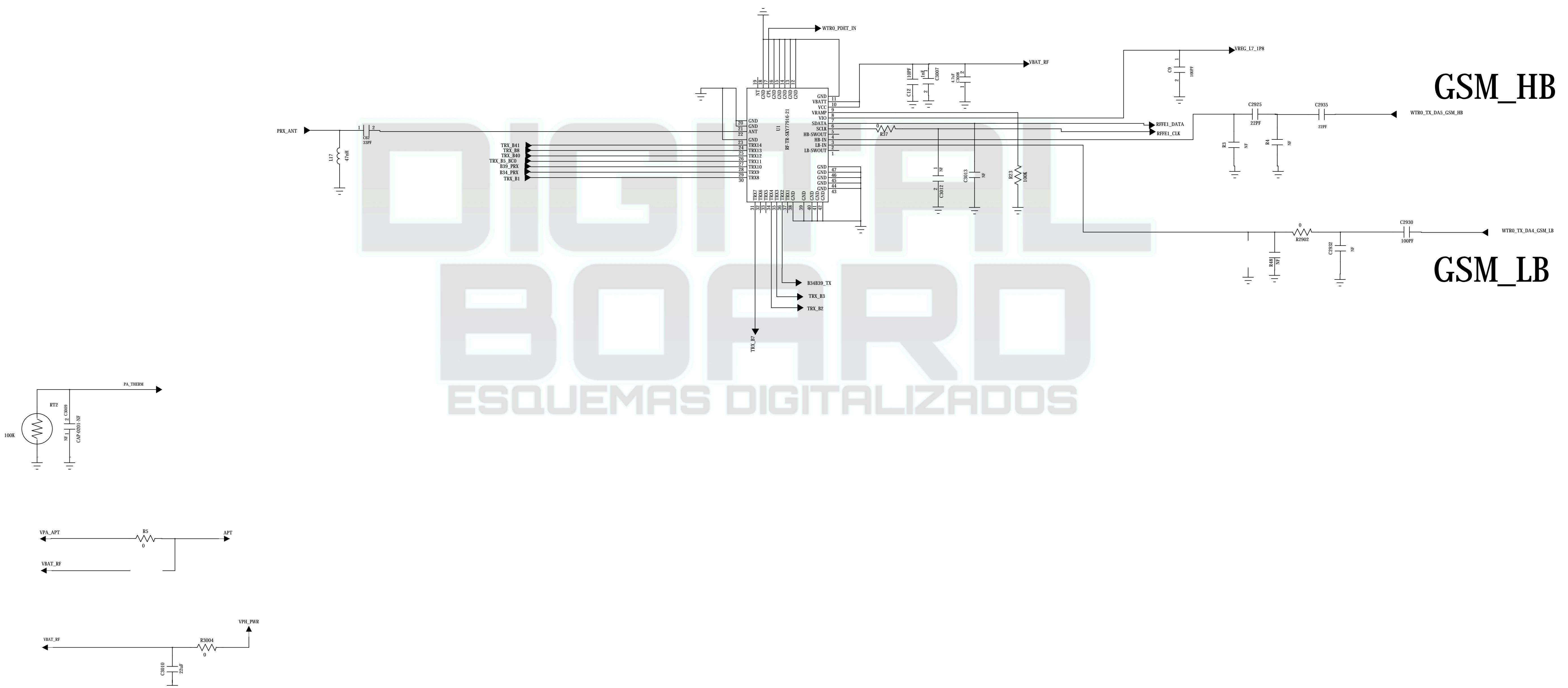
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TRX_B40		
QFE2320_ANT		
TRX_B38_41		

	ANT_SWITCH_CTL0	ANT_SWITCH_CTL1
TRX_B7		
TRX_B40		
QFE2320_ANT		
TRX_B38_41		

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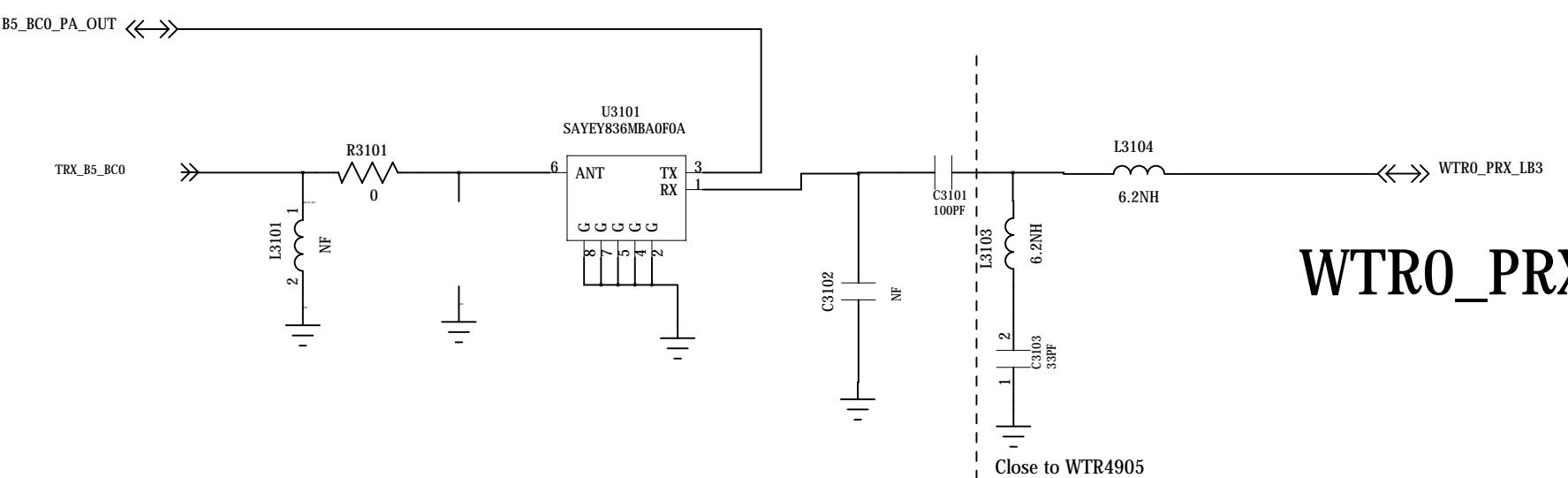
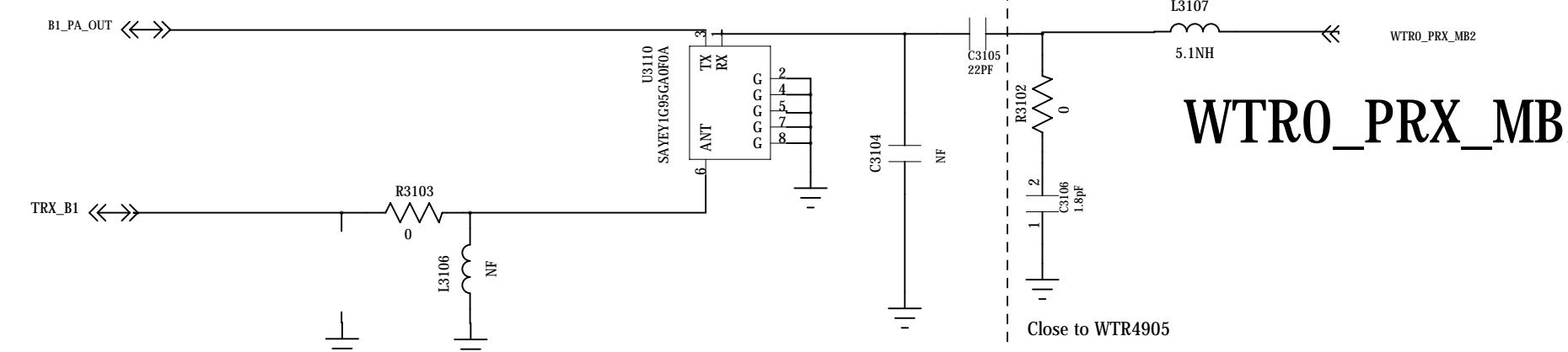
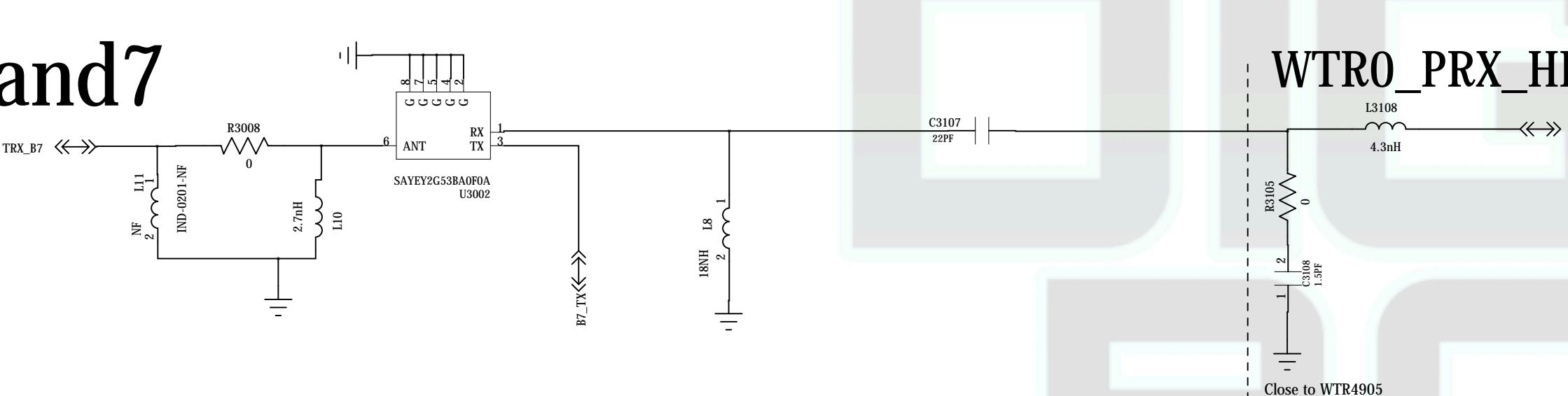
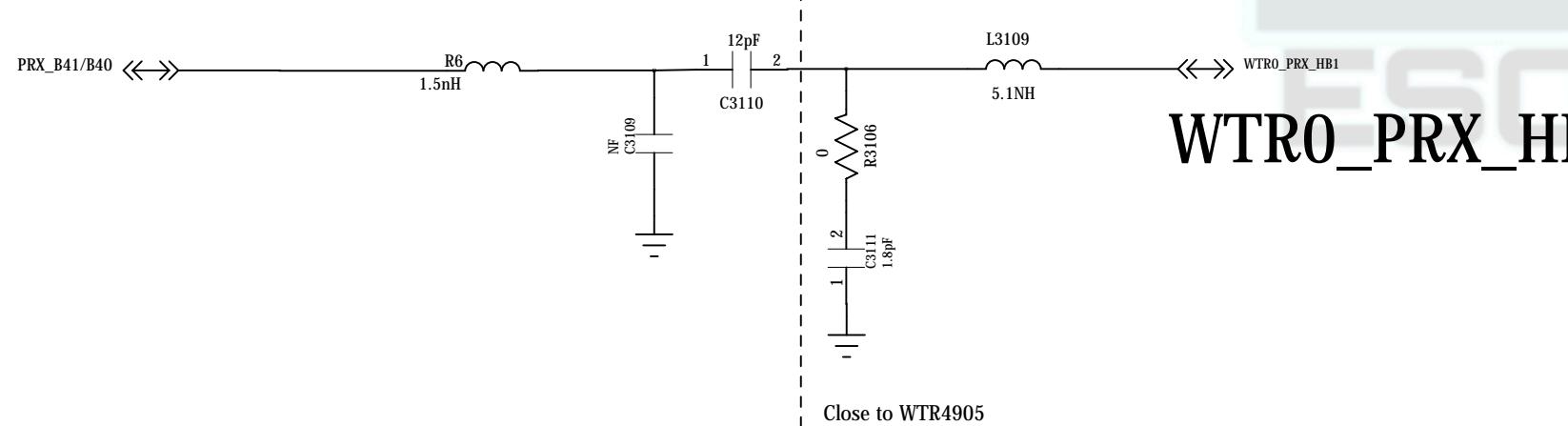
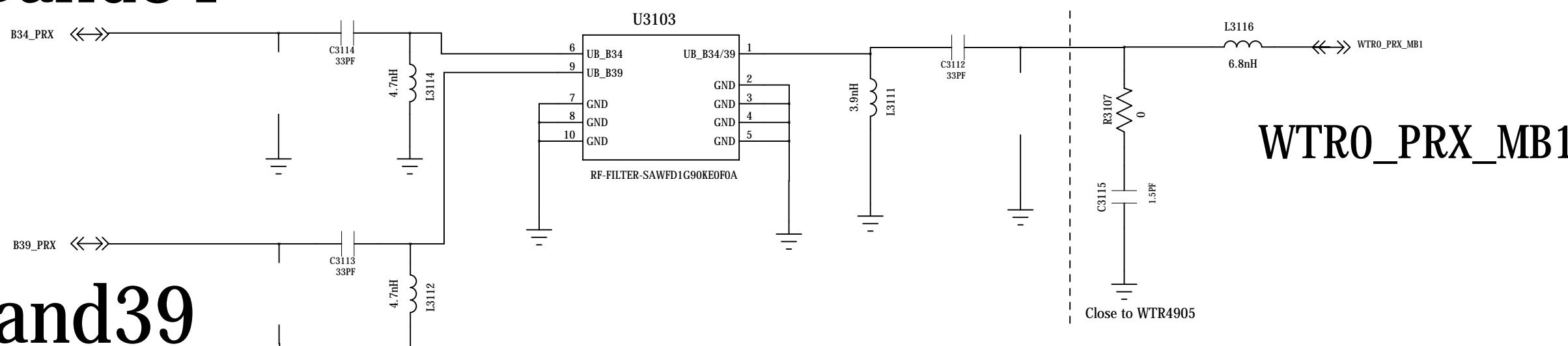
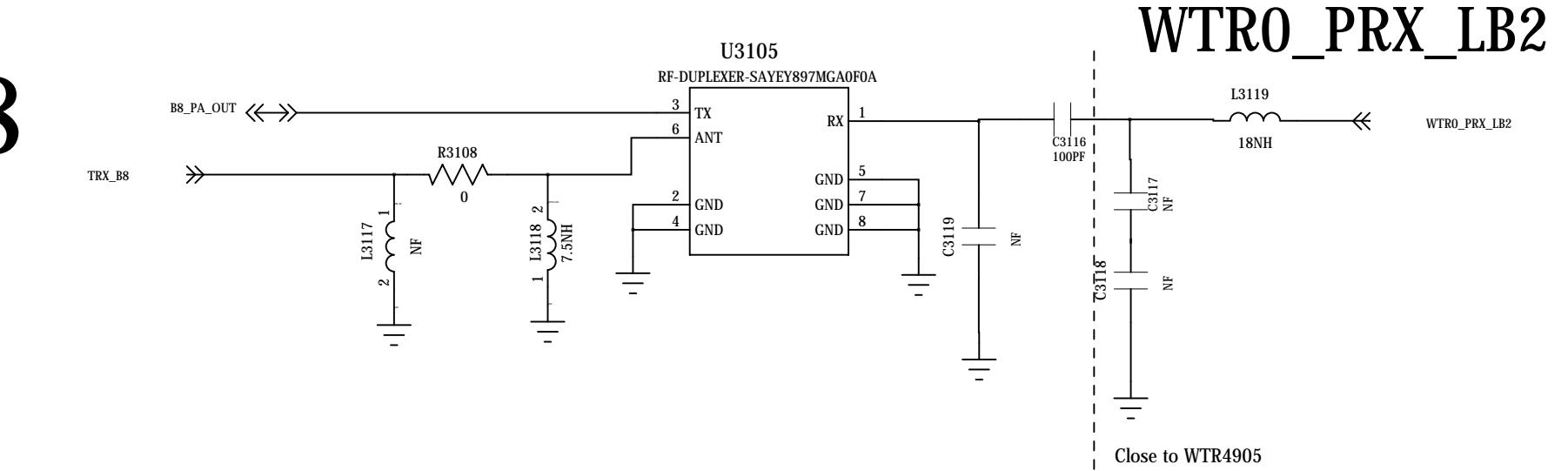
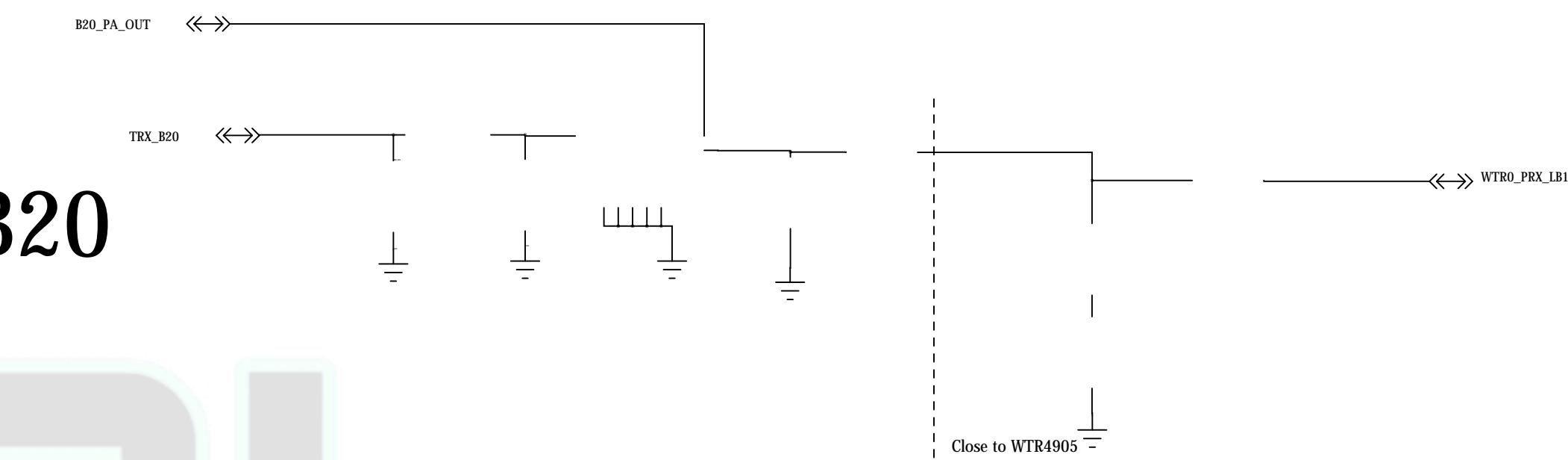
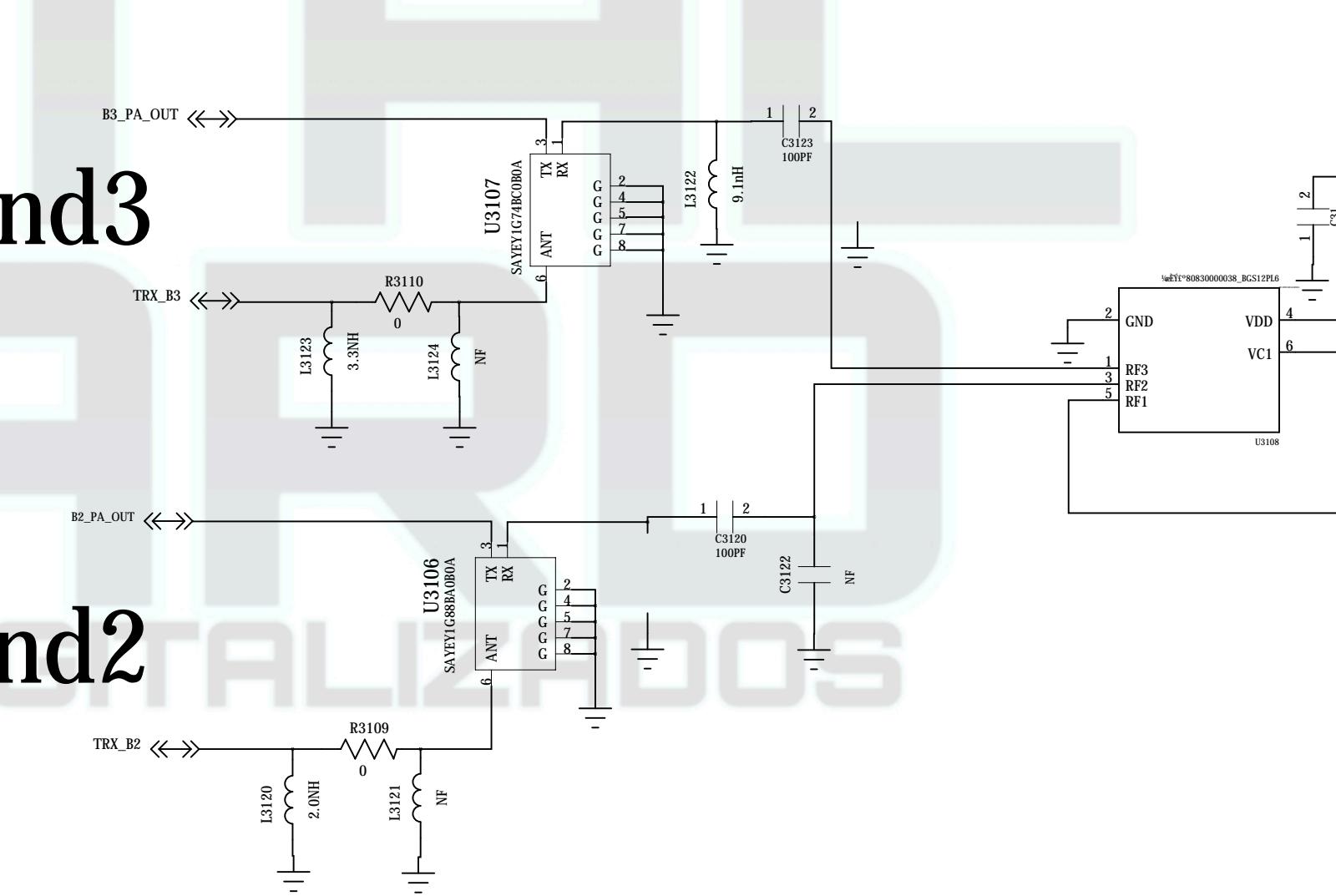
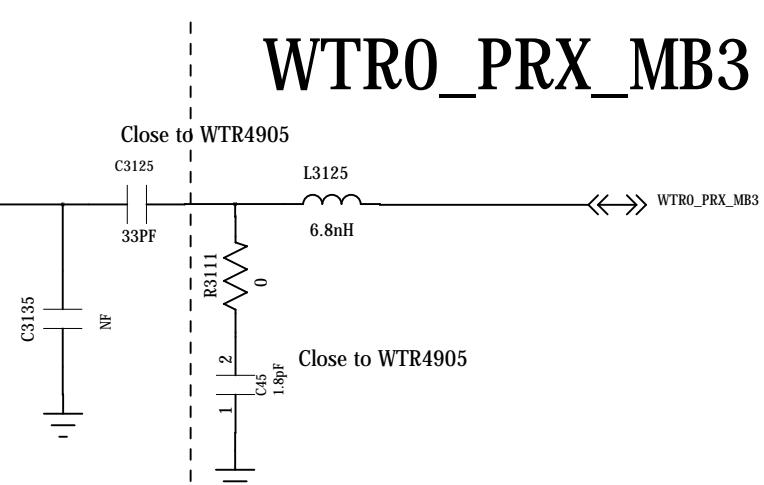
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Title	
Size	Sheet Name
Date:	Rev:
1	1
Sheet	of

**Band5****WTR0\_PRX\_LB3****Band1****WTR0\_PRX\_MB2****Band7****WTR0\_PRX\_HB2****Band40/41****WTR0\_PRX\_HB1****Band34****WTR0\_PRX\_MB1****Band39****Band8****WTR0\_PRX\_LB2****BandB20****Band3****Band2****WTR0\_PRX\_MB3**

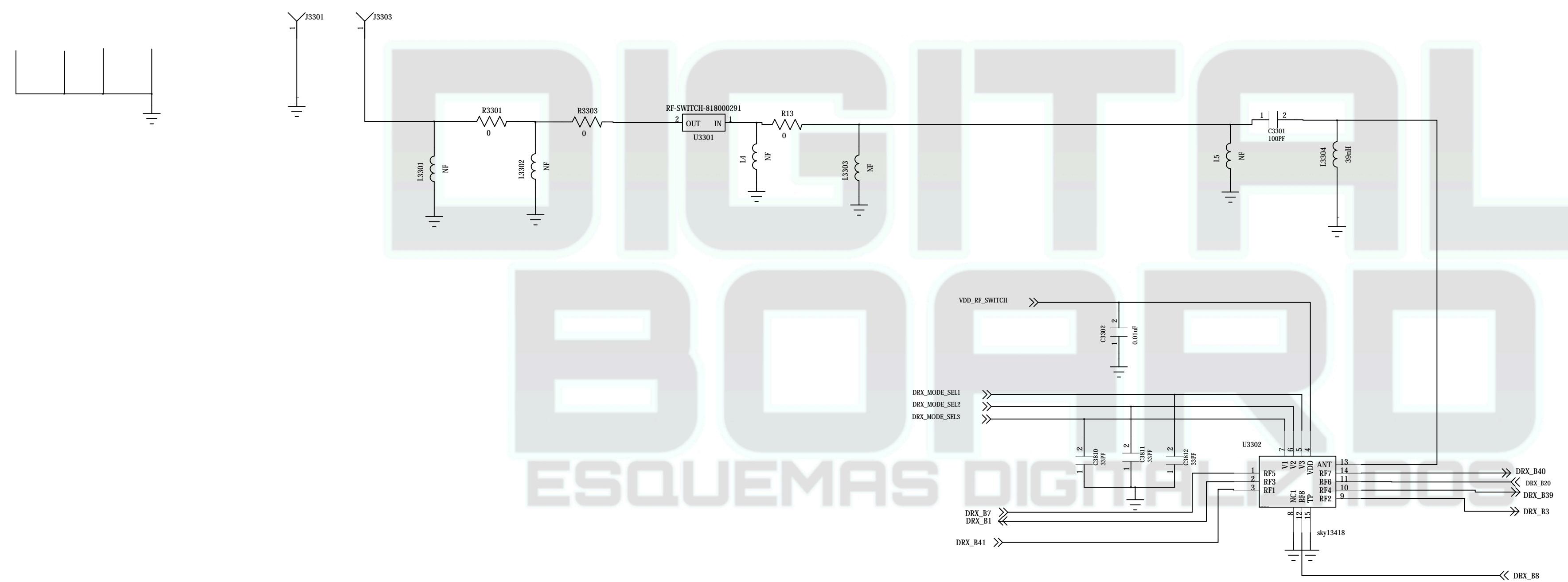
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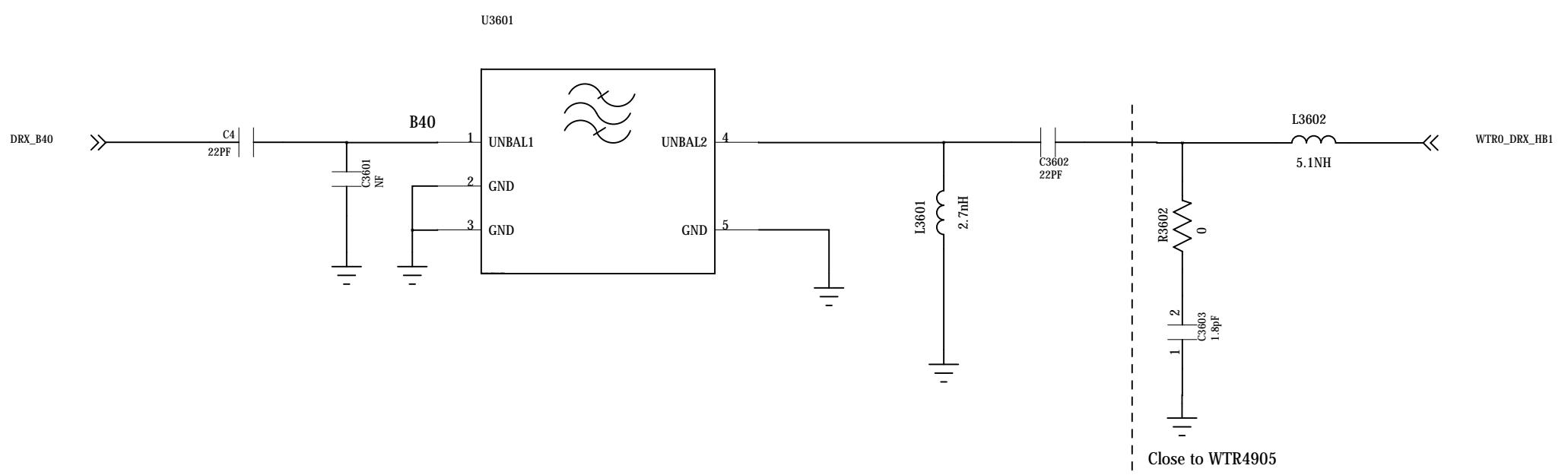
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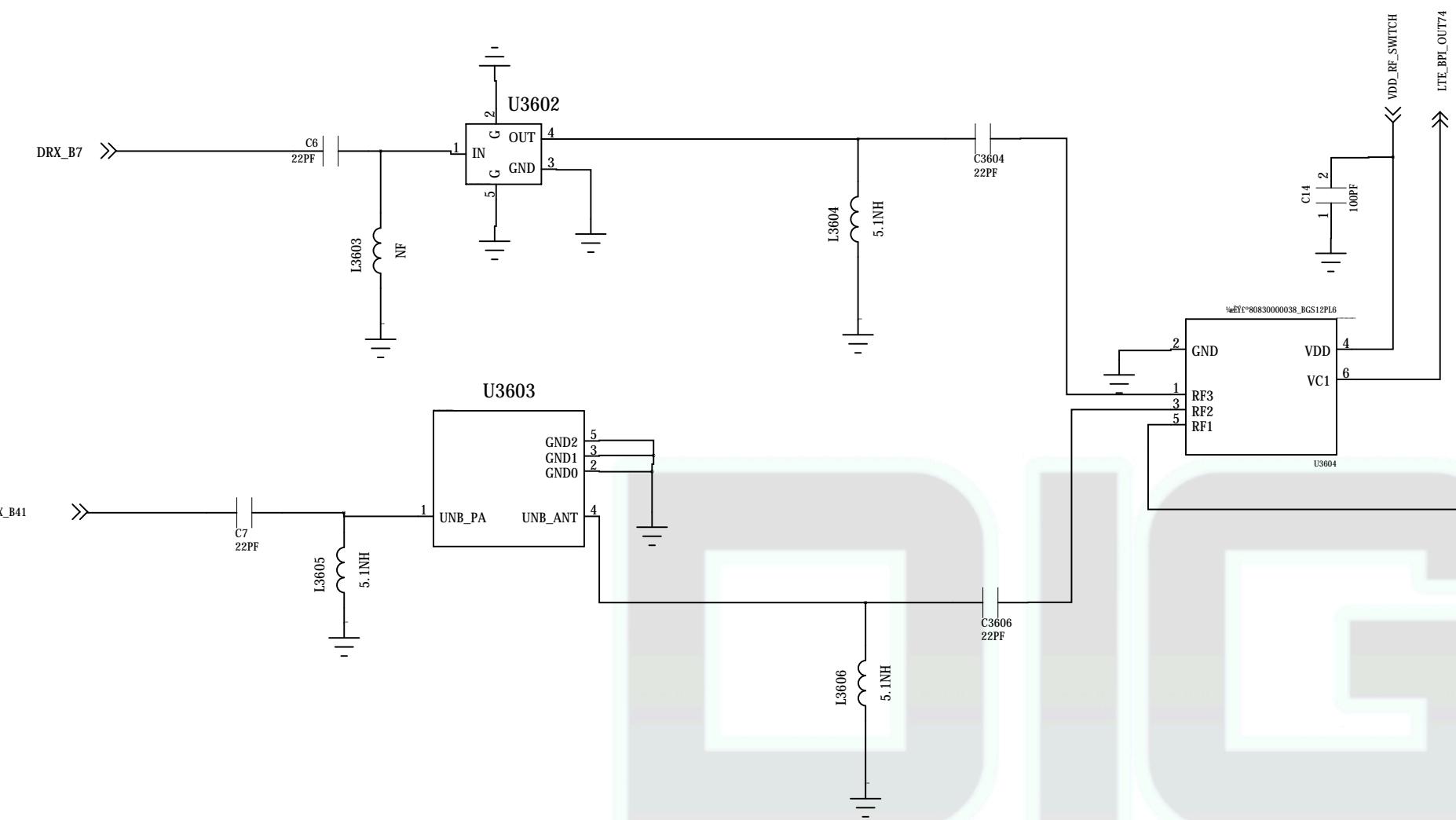


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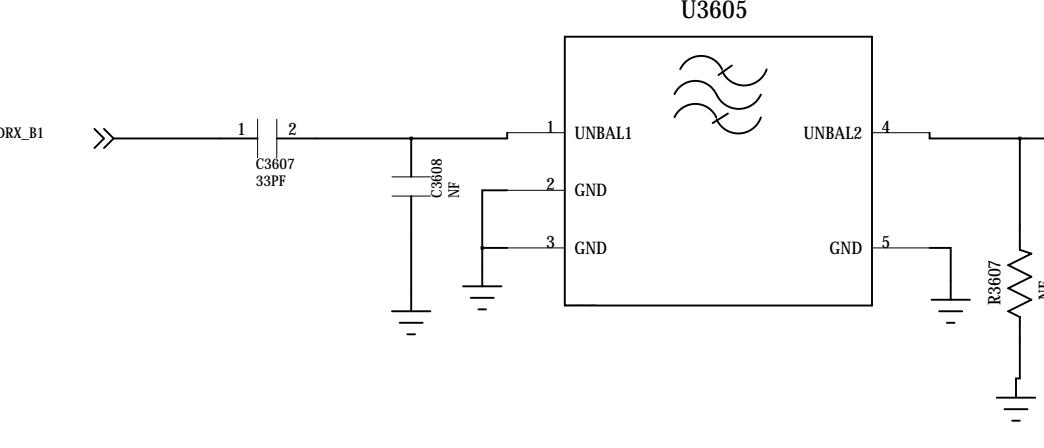


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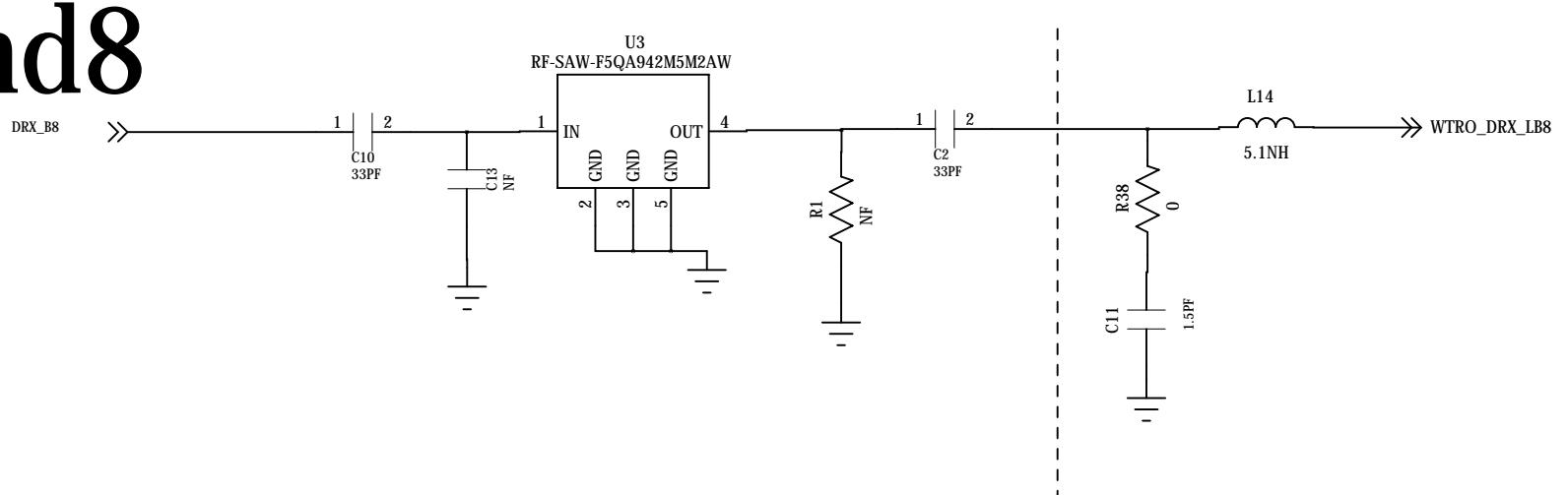


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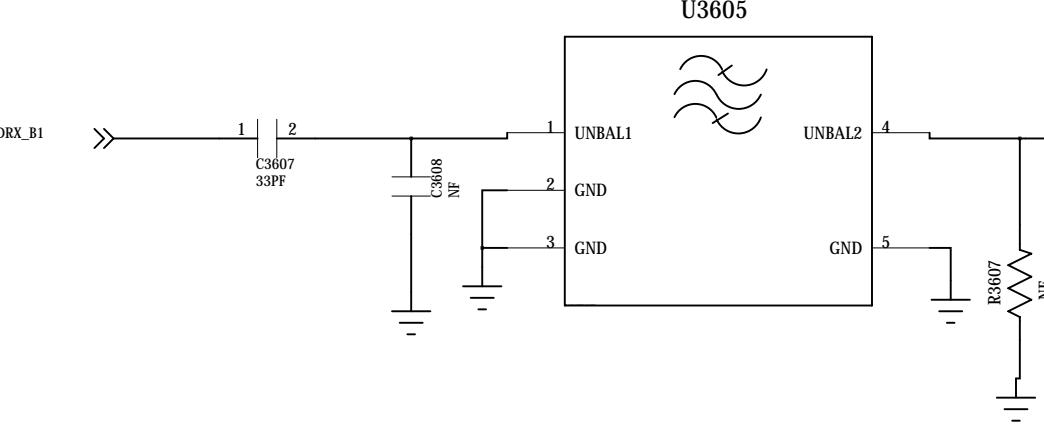


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Band8



Band1\_4

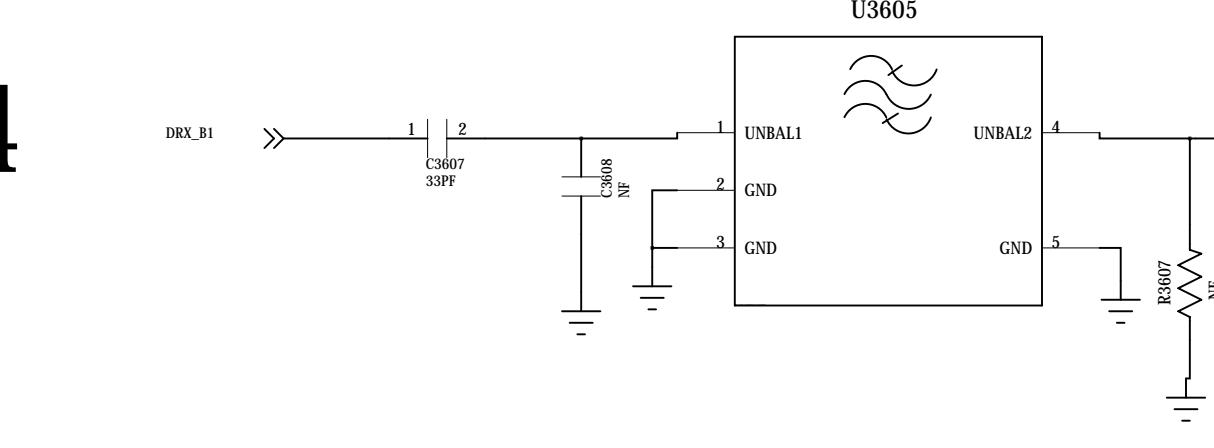


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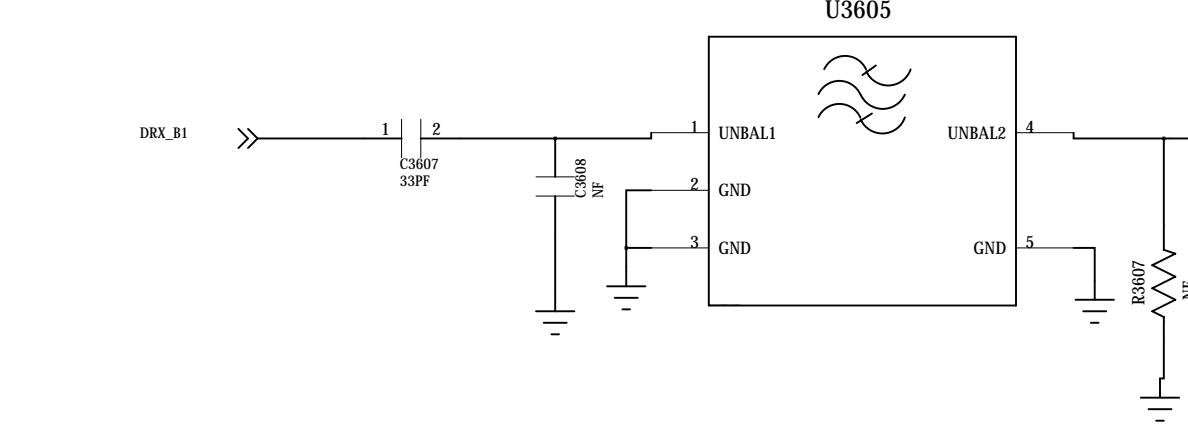


Band39



WTR0\_DRX\_MB2

Band3



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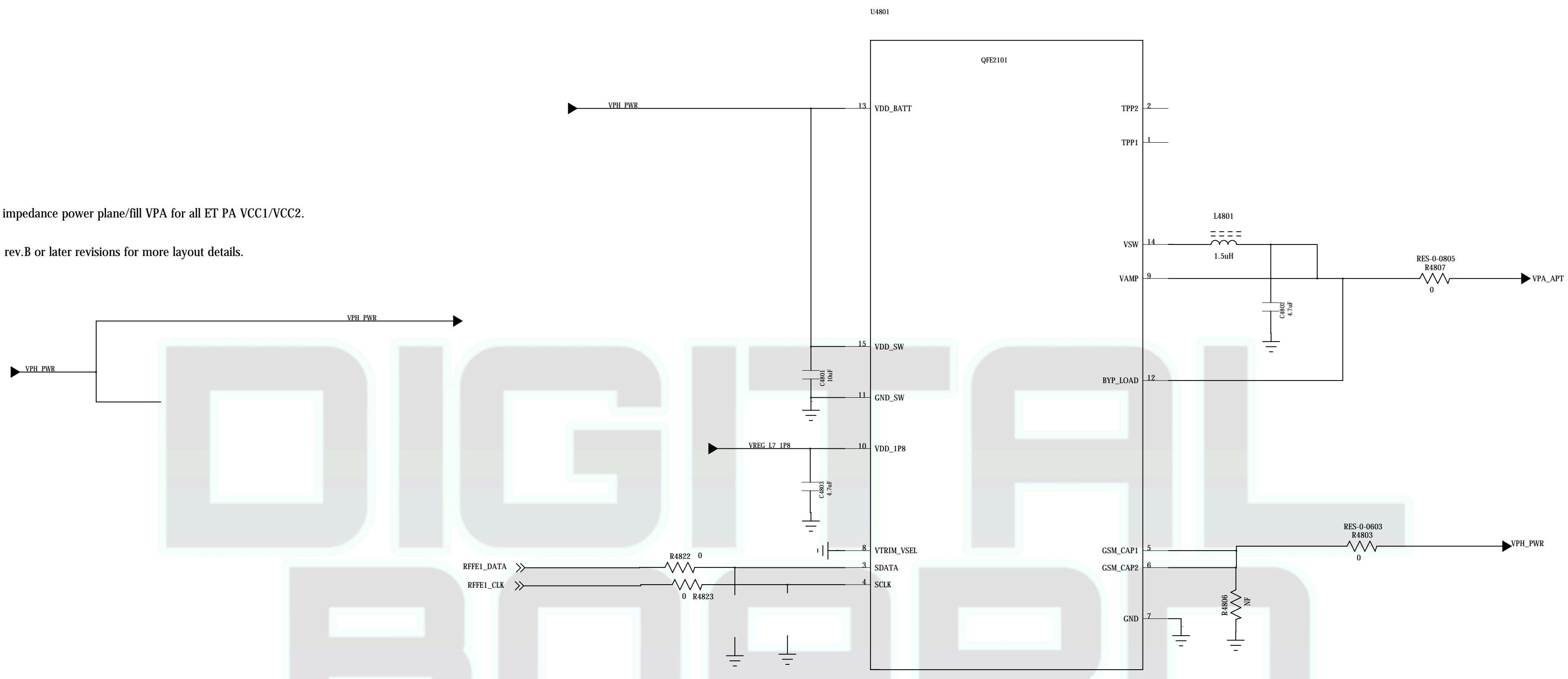
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Date:	Sheet	of

Note: Use a single low impedance power plane/fill VPA for all ET PA VCC1/VCC2.

Refer to 80-NA681-91 rev.B or later revisions for more layout details.



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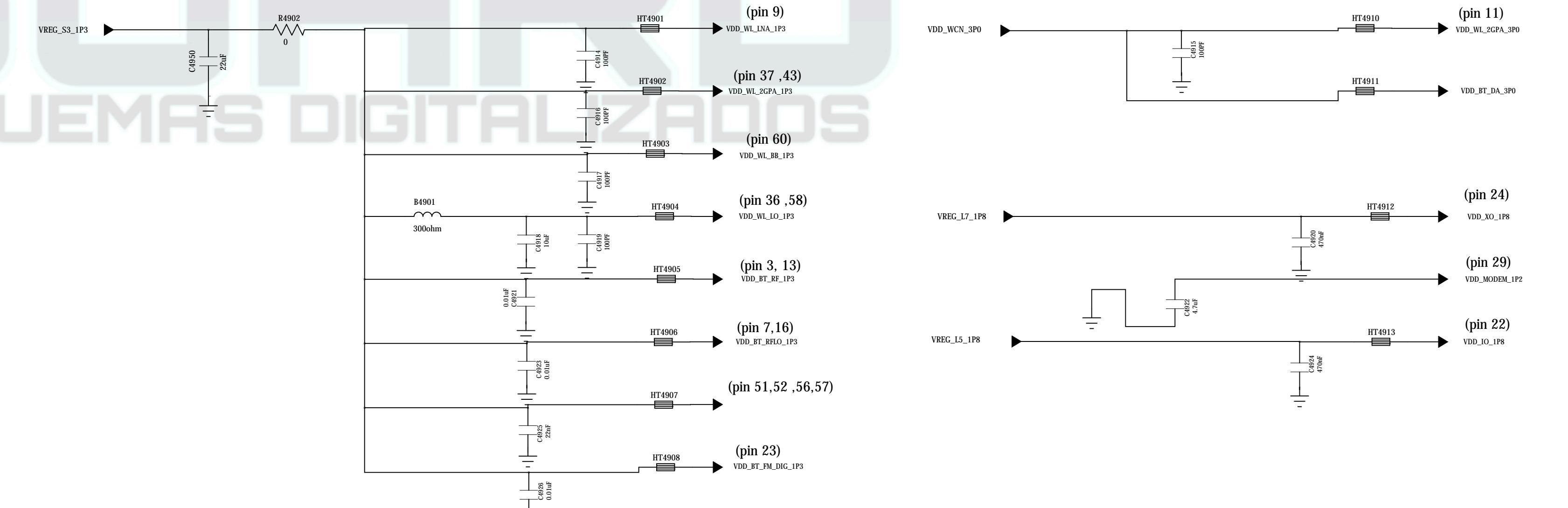
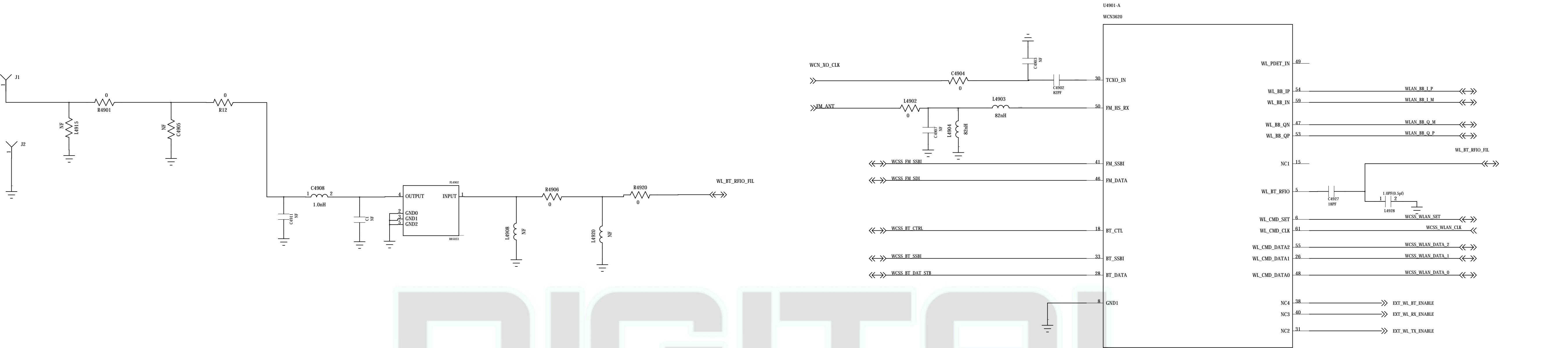
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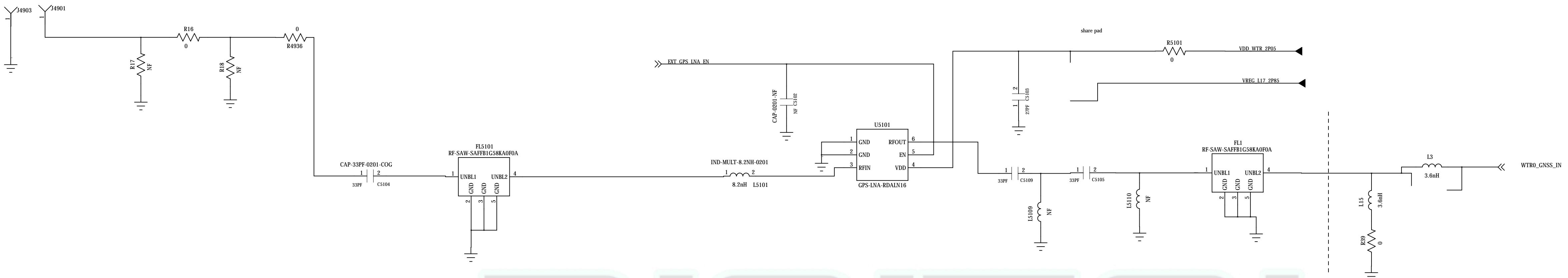
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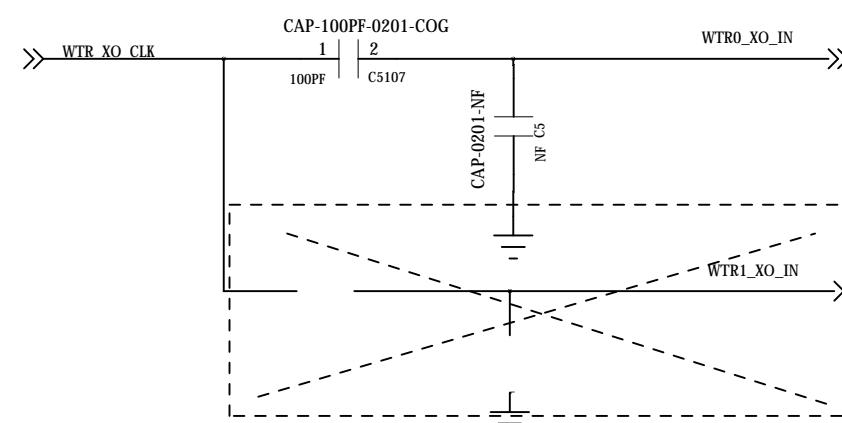
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