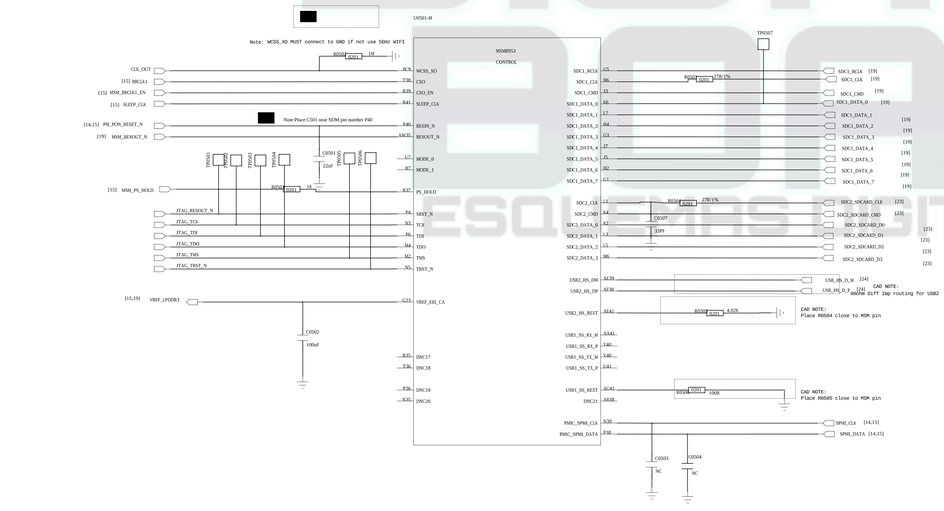

MSM8953 Control

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U0501-8

MSM8953
CONTROL

NOTE:
Place R0601 close to MSM Pin
10,11,16,17,19,22

R0601 240R/1% VREF_SS_EBI225 [10,11,16,17,19]

[19] EB0_CS0_N	A21	EB0_CS_N_0	EB0_CA0	E23			
[19] EB0_CS1_N	B18	EB0_CS_N_1					
[19] EB0_CLK_C	B22	EB0_CK0					
[19] EB0_CLK_T	A23	EB0_CK	EB0_DQ_0	E33	EB0_DQ0		
			EB0_DQ_1	E31	EB0_DQ1		
[19] EB0_CKE0	A19	EB0_CKE_0	EB0_DQ_2	C33	EB0_DQ2		
[19] EB0_CKE1	A17	EB0_CKE_1	EB0_DQ_3	E29	EB0_DQ3		
			EB0_DQ_4	C31	EB0_DQ4		
EB0_DM0	E21	EB0_DM_0	EB0_DQ_5	E27	EB0_DQ5		
EB0_DM1	C19	EB0_DM_1	EB0_DQ_6	C29	EB0_DQ6		
EB0_DM2	A33	EB0_DM_2	EB0_DQ_7	C27	EB0_DQ7		
EB0_DM3	B8	EB0_DM_3	EB0_DQ_8	E15	EB0_DQ8		
			EB0_DQ_9	E13	EB0_DQ9		
[19] EB0_DQS0_C	C25	EB0_DQS0_0	EB0_DQ_10	C15	EB0_DQ10		
[19] EB0_DQS0_T	E25	EB0_DQS_0	EB0_DQ_11	E11	EB0_DQ11		
			EB0_DQ_12	C13	EB0_DQ12		
[19] EB0_DQS1_C	E17	EB0_DQS0_1	EB0_DQ_13	C11	EB0_DQ13		
[19] EB0_DQS1_T	C17	EB0_DQS_1	EB0_DQ_14	E9	EB0_DQ14		
			EB0_DQ_15	C9	EB0_DQ15		
[19] EB0_DQS2_C	B34	EB0_DQS0_2	EB0_DQ_16	A39	EB0_DQ16		
[19] EB0_DQS2_T	A35	EB0_DQS_2	EB0_DQ_17	C37	EB0_DQ17		
			EB0_DQ_18	A37	EB0_DQ18		
[19] EB0_DQS3_C	A7	EB0_DQS0_3	EB0_DQ_19	C39	EB0_DQ19		
[19] EB0_DQS3_T	C7	EB0_DQS_3	EB0_DQ_20	E37	EB0_DQ20		
			EB0_DQ_21	B36	EB0_DQ21		
EB0_CA0	B30	EB0_CA_0	EB0_DQ_22	E39	EB0_DQ22		
EB0_CA1	A29	EB0_CA_1	EB0_DQ_23	E35	EB0_DQ23		
EB0_CA2	A27	EB0_CA_2	EB0_DQ_24	C3	EB0_DQ24		
EB0_CA3	B26	EB0_CA_3	EB0_DQ_25	A3	EB0_DQ25		
EB0_CA4	A25	EB0_CA_4	EB0_DQ_26	C5	EB0_DQ26		
EB0_CA5	A15	EB0_CA_5	EB0_DQ_27	C1	EB0_DQ27		
EB0_CA6	B14	EB0_CA_6	EB0_DQ_28	A5	EB0_DQ28		
EB0_CA7	A13	EB0_CA_7	EB0_DQ_29	E5	EB0_DQ29		
EB0_CA8	A11	EB0_CA_8	EB0_DQ_30	E3	EB0_DQ30		
EB0_CA9	B10	EB0_CA_9	EB0_DQ_31	E1	EB0_DQ31		

MSM8953 EBI

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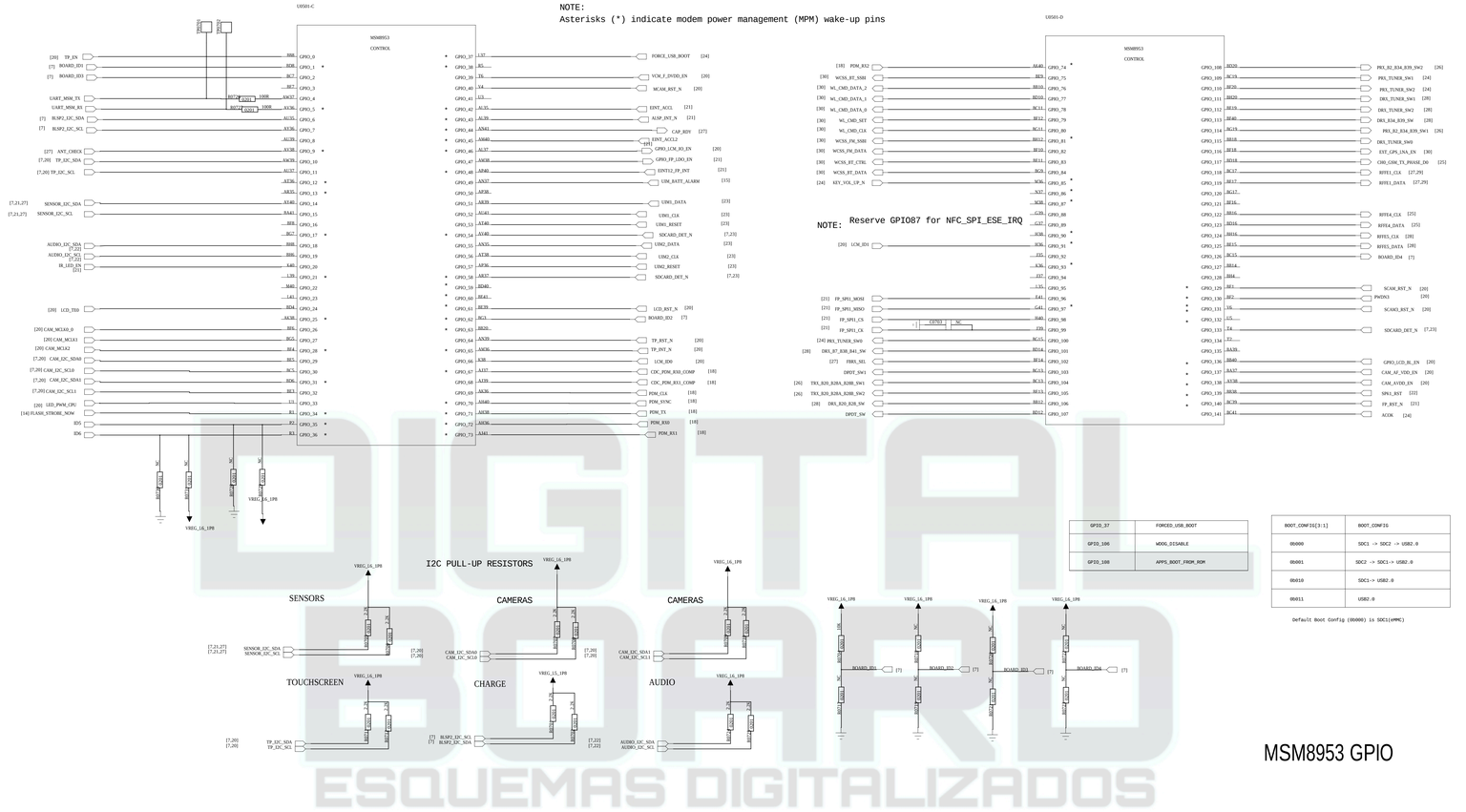


NOTE:
Asterisks (*) indicate modem power management (MPM) wake-up pins

NOTE: Reserve GPIO87 for NFC_SPI_ESE_IRQ

GPIO_37	FORCED_USB_BOOT
GPIO_106	WDOG_DISABLE
GPIO_108	APPS_BOOT_FROM_ROM

BOOT_CONFIG[3:1]	BOOT_CONFIG
0b000	SDC1 -> SDC2 -> USB2.0
0b001	SDC2 -> SDC1-> USB2.0
0b010	SDC1-> USB2.0
0b011	USB2.0

Default Boot Config (0b000) is SDC1(eMMC)

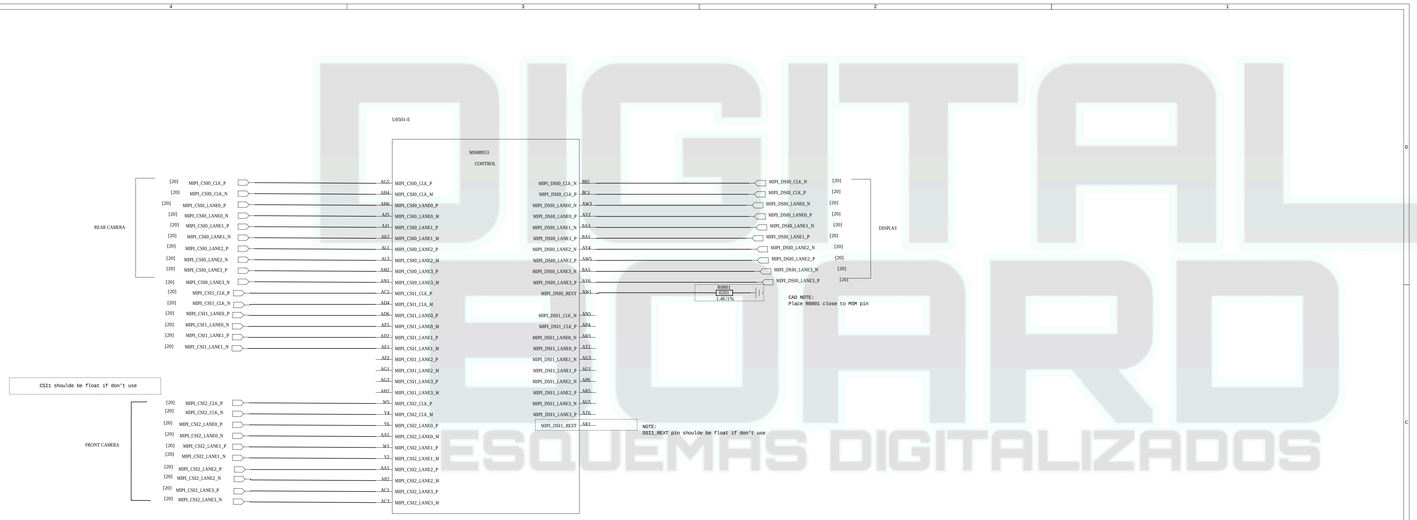
NOTE:
Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to,inout pull down when the peripherals are powered off to eliminate leakage.

MSM8953 GPIO

<Company Name>

DRAWING NO: <Drawing Number>

REV: <Revision>



CSI Pin Name	CSI DPHY 4-lane	CSI DPHY 2+1 Mode	CSI CPHY 3Phase Mode
CSI0_3PHASE_PIN0	CSI0_CLKP	CSI0_2LANE_CLKP	NC
CSI0_3PHASE_PIN1	CSI0_CLKN	CSI0_2LANE_CLKN	CSI0_TRI0_A
CSI0_3PHASE_PIN2	CSI0_DP0	CSI0_2LANE_DP0	CSI0_TRI0_B
CSI0_3PHASE_PIN3	CSI0_DN0	CSI0_2LANE_DN0	CSI0_TRI0_C
CSI0_3PHASE_PIN4	CSI0_DP1	CSI0_2LANE_DP1	CSI0_TRI1_A
CSI0_3PHASE_PIN5	CSI0_DN1	CSI0_2LANE_DN1	CSI0_TRI1_B
CSI0_3PHASE_PIN6	CSI0_DP2	CSI0_1LANE_DP0	CSI0_TRI1_C
CSI0_3PHASE_PIN7	CSI0_DN2	CSI0_1LANE_DN0	CSI0_TRI2_A
CSI0_3PHASE_PIN8	CSI0_DP3	CSI0_1LANE_CLKP	CSI0_TRI2_B
CSI0_3PHASE_PIN9	CSI0_DN3	CSI0_1LANE_CLKN	CSI0_TRI2_C
CSI1_3PHASE_PIN0	CSI1_CLKP	CSI1_2LANE_CLKP	NC
CSI1_3PHASE_PIN1	CSI1_CLKN	CSI1_2LANE_CLKN	CSI1_TRI0_A
CSI1_3PHASE_PIN2	CSI1_DP0	CSI1_2LANE_DP0	CSI1_TRI0_B
CSI1_3PHASE_PIN3	CSI1_DN0	CSI1_2LANE_DN0	CSI1_TRI0_C
CSI1_3PHASE_PIN4	CSI1_DP1	CSI1_2LANE_DP1	CSI1_TRI1_A
CSI1_3PHASE_PIN5	CSI1_DN1	CSI1_2LANE_DN1	CSI1_TRI1_B
CSI1_3PHASE_PIN6	CSI1_DP2	CSI1_1LANE_DP0	CSI1_TRI1_C
CSI1_3PHASE_PIN7	CSI1_DN2	CSI1_1LANE_DN0	CSI1_TRI2_A
CSI1_3PHASE_PIN8	CSI1_DP3	CSI1_1LANE_CLKP	CSI1_TRI2_B
CSI1_3PHASE_PIN9	CSI1_DN3	CSI1_1LANE_CLKN	CSI1_TRI2_C
CSI2_3PHASE_PIN0	CSI2_CLKP	CSI2_2LANE_CLKP	NC
CSI2_3PHASE_PIN1	CSI2_CLKN	CSI2_2LANE_CLKN	CSI2_TRI0_A
CSI2_3PHASE_PIN2	CSI2_DP0	CSI2_2LANE_DP0	CSI2_TRI0_B
CSI2_3PHASE_PIN3	CSI2_DN0	CSI2_2LANE_DN0	CSI2_TRI0_C
CSI2_3PHASE_PIN4	CSI2_DP1	CSI2_2LANE_DP1	CSI2_TRI1_A
CSI2_3PHASE_PIN5	CSI2_DN1	CSI2_2LANE_DN1	CSI2_TRI1_B
CSI2_3PHASE_PIN6	CSI2_DP2	CSI2_1LANE_DP0	CSI2_TRI1_C
CSI2_3PHASE_PIN7	CSI2_DN2	CSI2_1LANE_DN0	CSI2_TRI2_A
CSI2_3PHASE_PIN8	CSI2_DP3	CSI2_1LANE_CLKP	CSI2_TRI2_B
CSI2_3PHASE_PIN9	CSI2_DN3	CSI2_1LANE_CLKN	CSI2_TRI2_C

MSM8953 MIPI

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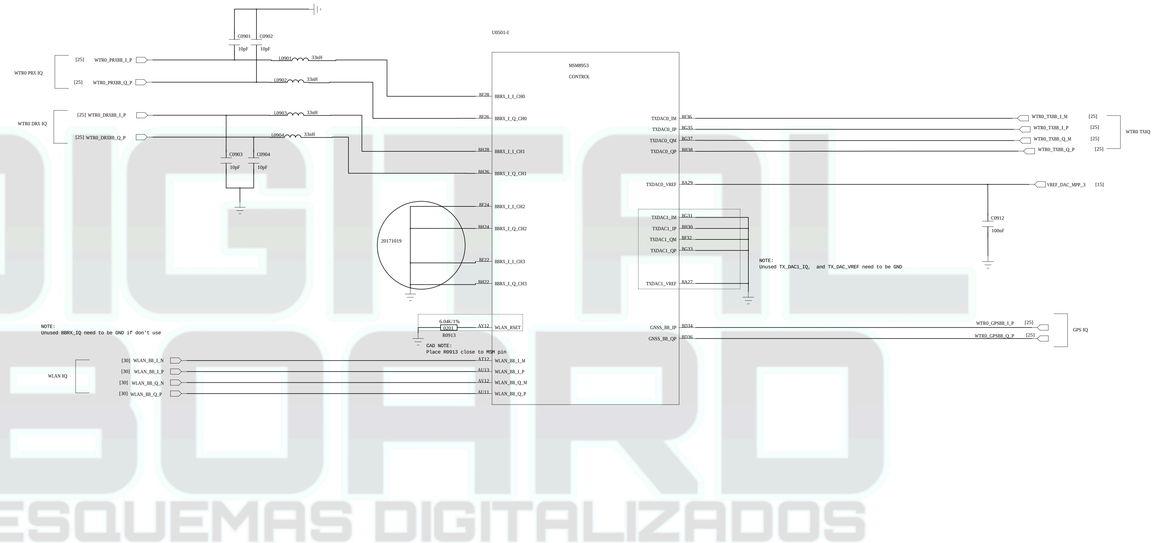
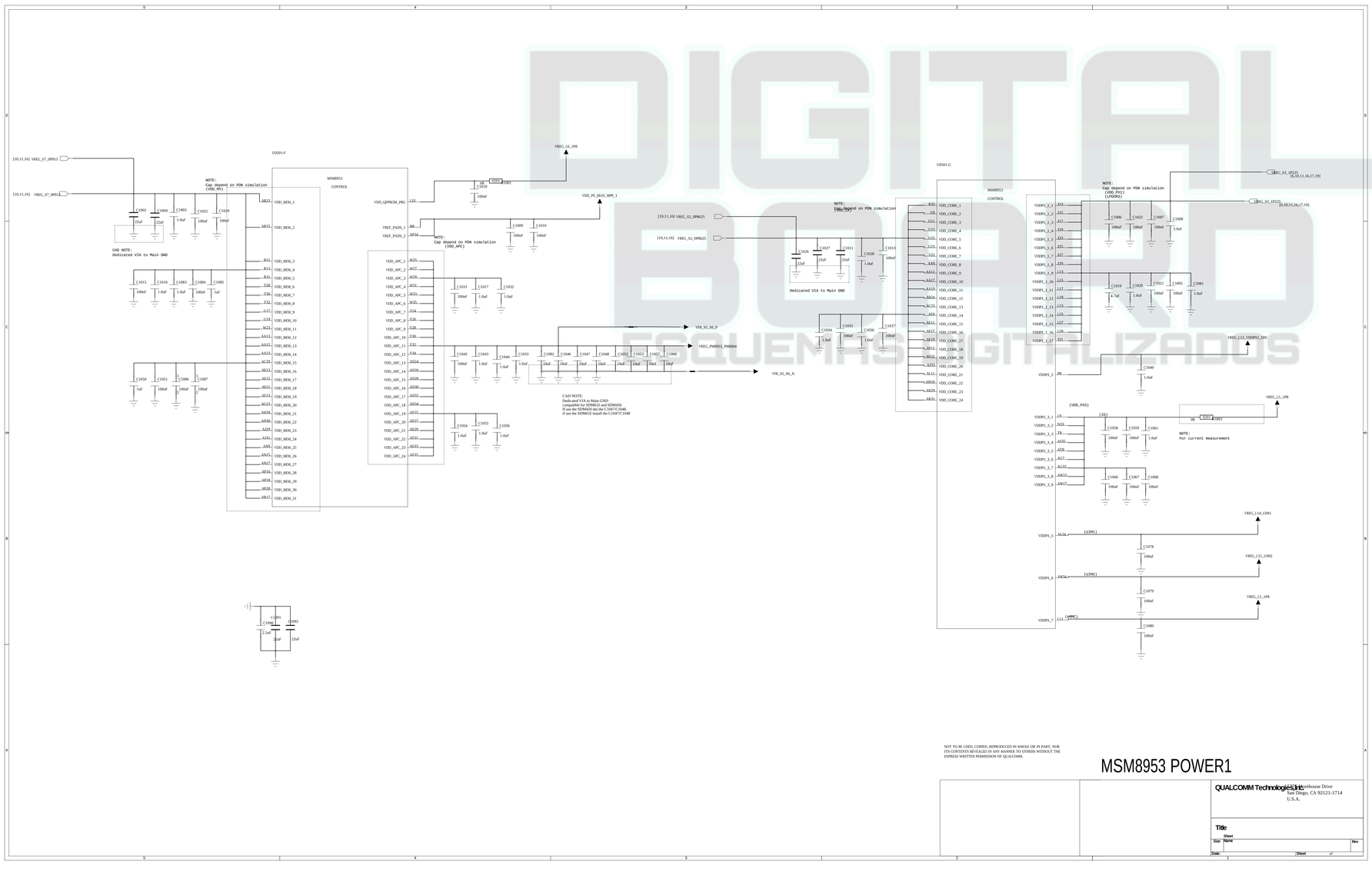


DRAWN: LiuMengya	DATED: <Drawn Date>	<Company Name>		
		21_LTE_B7		
		CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number> REV: <Revision>



MSM8953 POWER1

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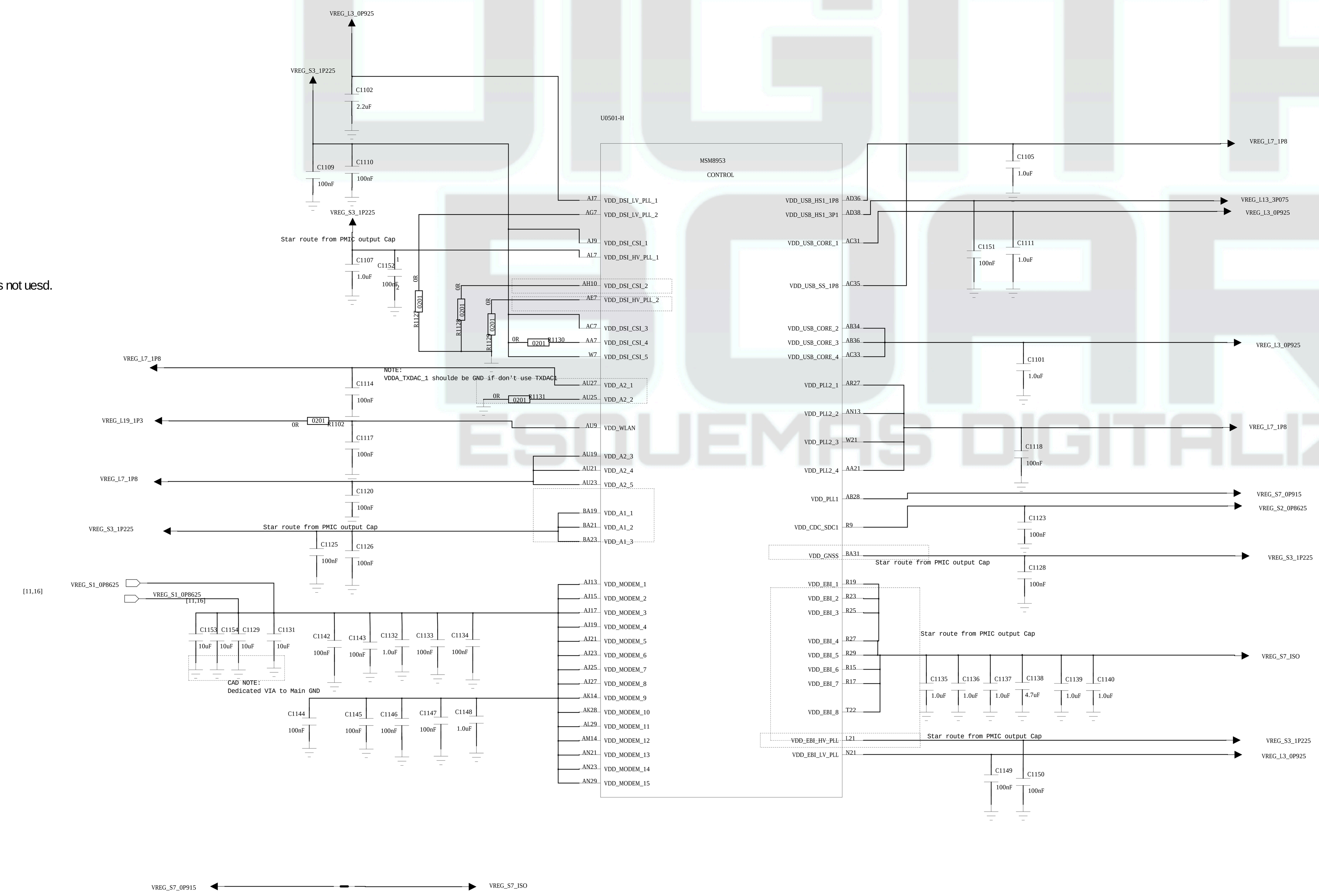
CAD NOTE:
About star route from PMIC output Cap:

Note: Connect SDM pins(AG7,AH10 and AE7) to GND if DSI1 is not uesd.

Note: Respective Camera pins can be left open if not used.
Float AC7 pin if CAM0 not used
Float AA7 pin if CAM1 not used
Float W7 pin if CAM2 not used



MSM8953 POWER2

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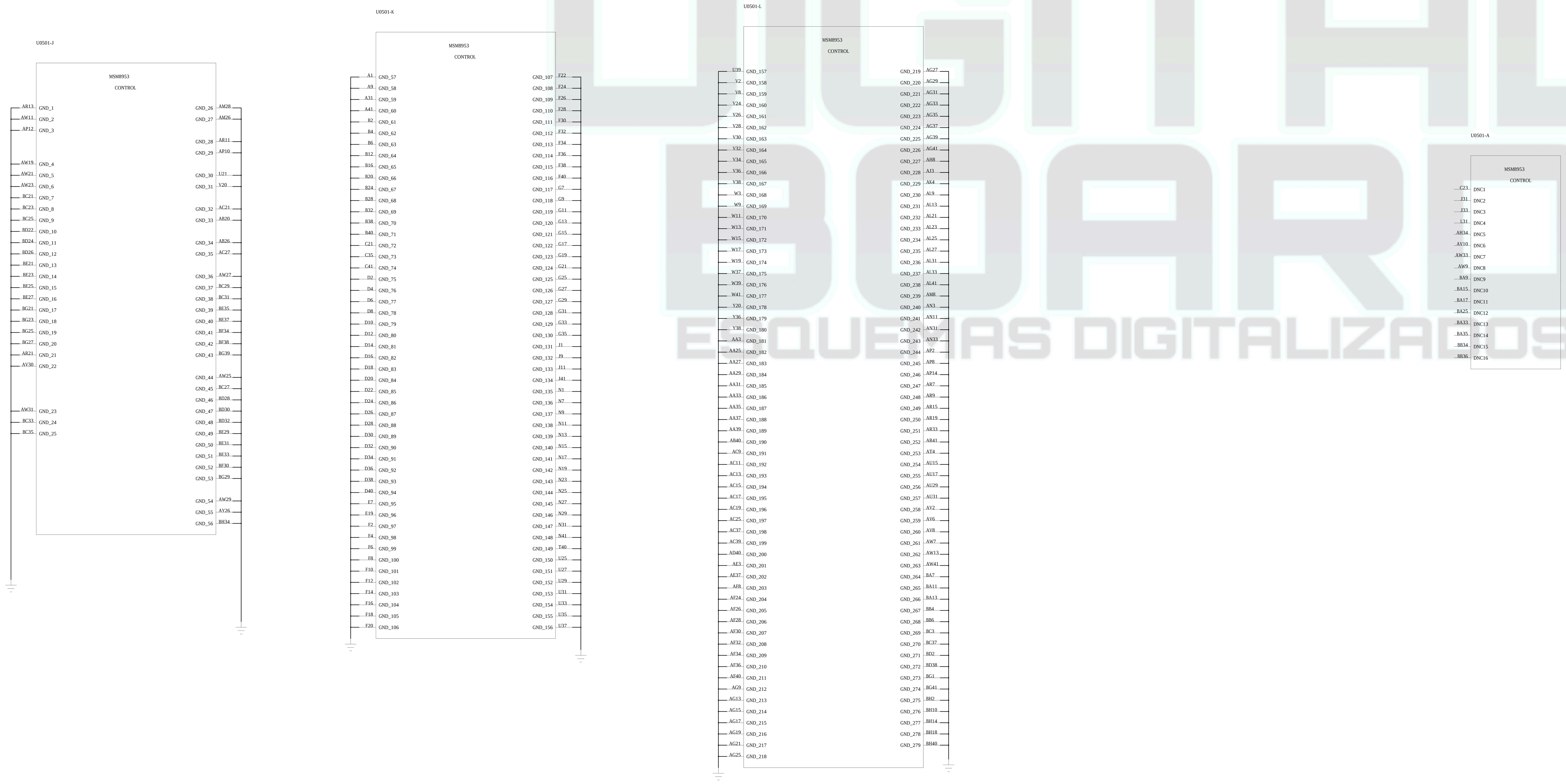

MSM8953 GND

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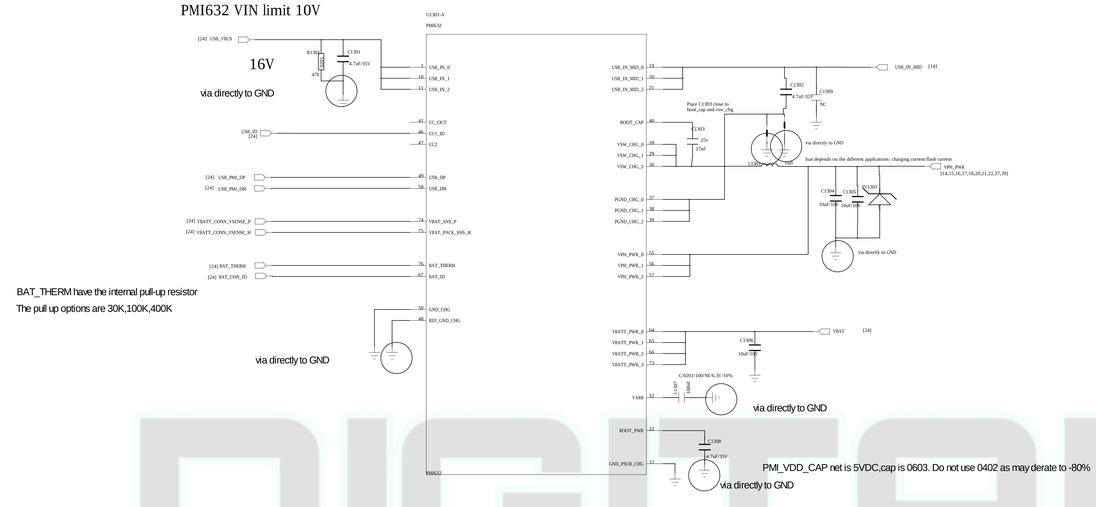
Use C1301= 4.7uF for Single Charging Config

Use C1301 = 2.2uF for Parallel Charging Config

PMI632 VIN limit 10V



PMI_VDD_CAP net is 5VDC,cap is 0603. Do not use 0402 as may derate to -80%

BAT_THERM have the internal pull-up resistor

The pull up options are 30K,100K,400K

PMI8952 Charger

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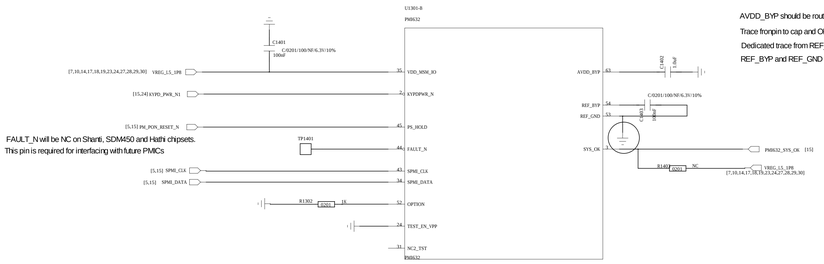
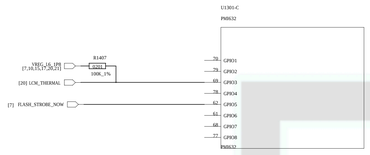
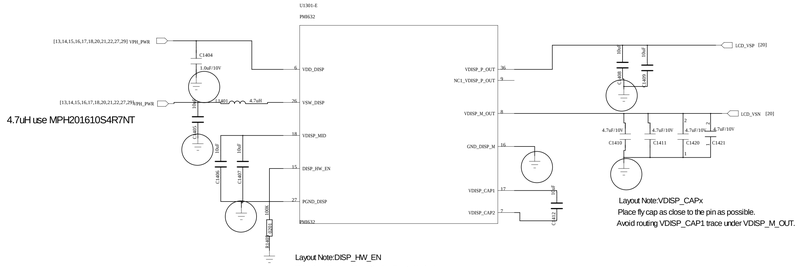


FAULT_N will be NC on Shanti, SDM450 and Hathi chipsets.
This pin is required for interfacing with future PMICs

AVDD_BYP should be routed away from noisy traces
Trace fronpin to cap and ONE dedicated via fron cap to main groung plane.
Dedicated trace from REF_BYP REF_GND to cap
REF_BYP and REF_GND should be routed away from noisy trace

OPTION	PON Configuration	PD Resistance
1	SPMI,uUSB	1K
2	I2C,uUSB	22K
7	I2C,TypeC	510K
	SPMI,TypeC	1M



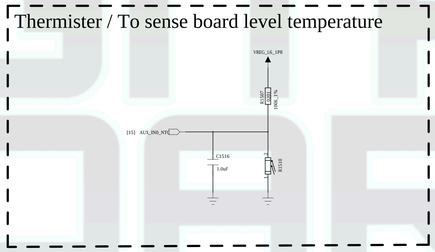


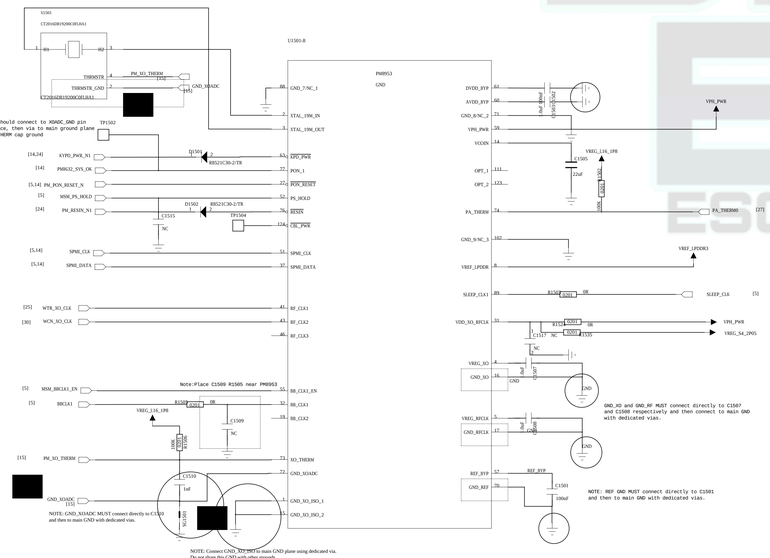
4.7uH use MPH201610S4R7NT

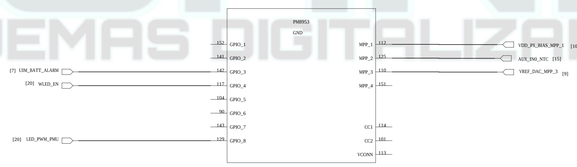
Layout Note:DISP_HW_EN
This signal is used for "Display Tap to Wake"
If unused in HW, this pin should be connected to GND
Bench DC - Connect to a DIO for testability

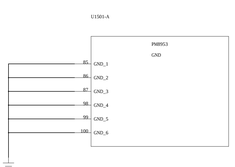
Layout Note:VDISP_CAPx
Place fly cap as close to the pin as possible.
Avoid routing VDISP_CAP1 trace under VDISP_M_OUT.

PVDD is supply for RGB only
VDD_DISP is supply for VIB_DRV_LDO_P also along with LCDB









PM8953 Control/Interface

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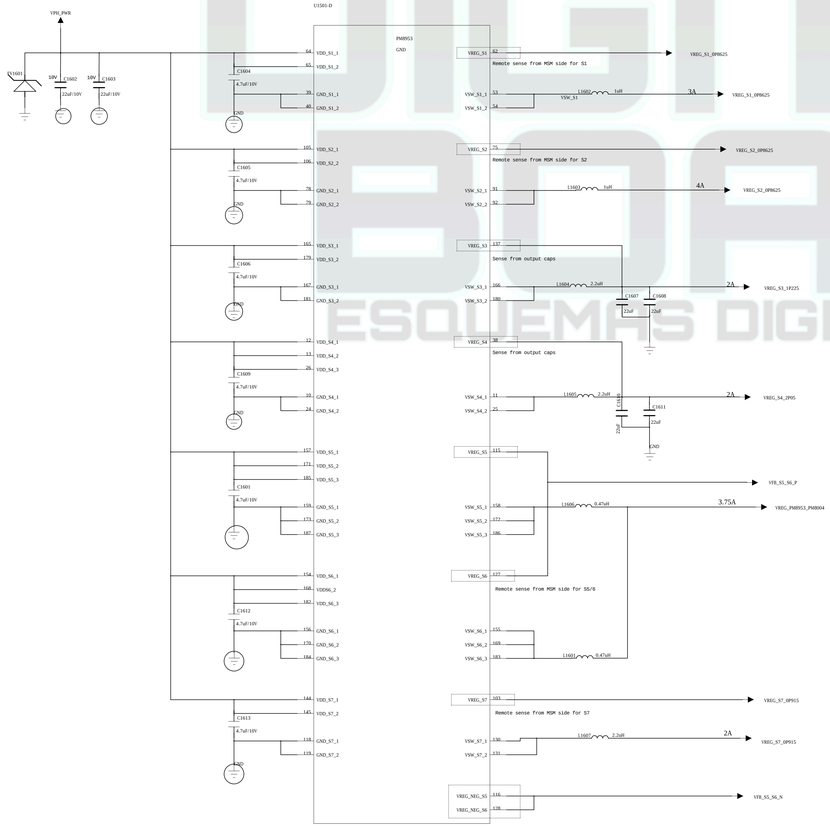

PM8953 SMPS

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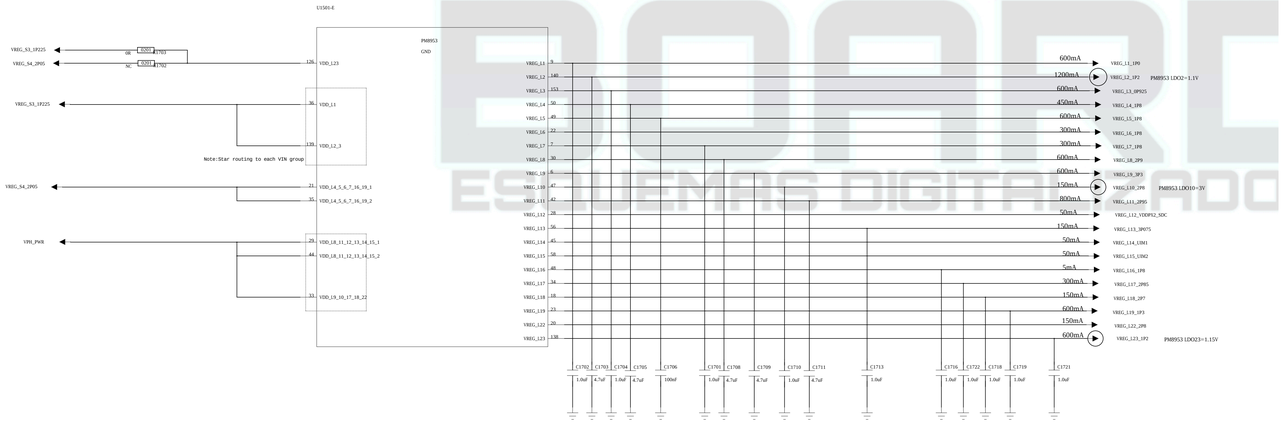

Table 3-7 PM8953 regulators and their intended uses

Function	Circuit type	Default voltage (V) [1]	Specified range (V) [2] (MSM8953/SDM450)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8953/SDM450)
S1	SMPS	0.87	0.4–1.14	0.32–2.04	3000	N	MSM modem
S2	SMPS	0.87	0.4–1.14	0.32–2.04	4000	Y	MSM core and graphics
S3	SMPS	1.225	1.2–1.25	0.32–2.04	2000	Y	LPDDR2 and LPDDR3, MIPI CSI, and DSI. Low-voltage LDOs (1, 2, 3, and 23)
S4	SMPS	2.04	1.8–2.04	0.32–2.04	2000	Y	High-voltage LDOs (4, 5, 6, 7, 16, 19 RFCLK, and XO)
S5	SMPS	0.87	0.4–1.14	0.350–1.355	3750	Y	MSM applications processor
S6	SMPS	0.87	0.4–1.14	0.350–1.355	3750	Y	MSM applications processor
S7	SMPS	0.915	0.4–1.14	0.32–2.04	2000	Y	MSM VDD memory rail (VDDMX)
L1	NMOS LDO	1.0 [3]	1.0 [3]	0.375–1.5375	600	N	RFICs
L2	NMOS LDO	1.100	1.100	0.375–1.5375	1200	N	Camera: digital
L3	NMOS LDO	0.925	0.925	0.375–1.5375	600	Y	MSM DSI PLL and USB
L4	PMOS LDO	1.800	1.800	1.750–3.3375	450	N	RFICs and GPS eLNA
L5 [4]	PMOS LDO	1.800	1.800	1.750–3.3375	600	Y	Most digital I/Os, MSM pad groups 3 and 7, LPDDR, and eMMC
L6	PMOS LDO	1.800	1.800	1.750–3.3375	300	N	MSM QFPROM, camera, touchscreen, display, and sensors
L7	PMOS LDO	1.800	1.800	1.750–3.3375	300	Y	MSM analog, USB and PLLs, WCN XO, and PM baseband clock driver
L8	PMOS LDO	2.900	2.900	1.750–3.3375	600	Y	eMMC
L9	PMOS LDO	V_{out} = 3.3 V for VBAT > 3.575 V; V_{out} = 3 V for VBAT < 3.575 V	3.000–3.300	1.750–3.3375	600	N	WCN
L10	PMOS LDO	3.0	3.0	1.750–3.3375	150	N	Sensors and touchscreen
L11 [5]	PMOS LDO	2.950	2.950	1.750–3.3375	800	Y	Micro SD

Table 3-7 PM8953 regulators and their intended uses (cont.)

Function	Circuit type	Default voltage (V) [1]	Specified range (V) [2] (MSM8953/SDM450)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8953/SDM450)
L12 [4]	PMOS LDO	2.950	1.800/2.950	1.750–3.3375	50	Y	MSM pad group 2
L13	PMOS LDO	3.125	3.125	1.750–3.3375	150	Y	MSM USB and PMIC and external codec audio
L14 [5]	PMOS LDO	1.800	1.800/3	1.750–3.3375	50	N	MSM pad group 5, dual-voltage UIM1, and NFC
L15 [5]	PMOS LDO	1.800	1.800/3	1.750–3.3375	50	N	MSM pad group 6 and dual-voltage UIM2
L16	PMOS LDO	1.800	1.800	1.750–3.3375	5	N	PMIC HKADC
L17	PMOS LDO	2.850	2.850	1.750–3.3375	300	N	Camera and display
L18	PMOS LDO	2.700	2.700	1.750–3.3375	150	N	QTI RF front-end
L19	NMOS LDO	1.350	1.350	0.375–1.5375	600	N	MSM analog, WCN, and WGR
L20	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC XO circuits
L21	Low-noise LDO	1.74	1.74	1.74–3.3375	5	Y	PMIC RF clock buffers
L22	PMOS LDO	2.800	2.800	1.750–3.3375	150	N	Camera: analog
L23	NMOS LDO	1.15	1.15	0.375–1.5375	600	N	Camera: digital

1. All regulators have default voltage settings, whether or not they default on; the voltage and state depends upon the programmable boot processor (PBS) configuration

PM8953 LDO

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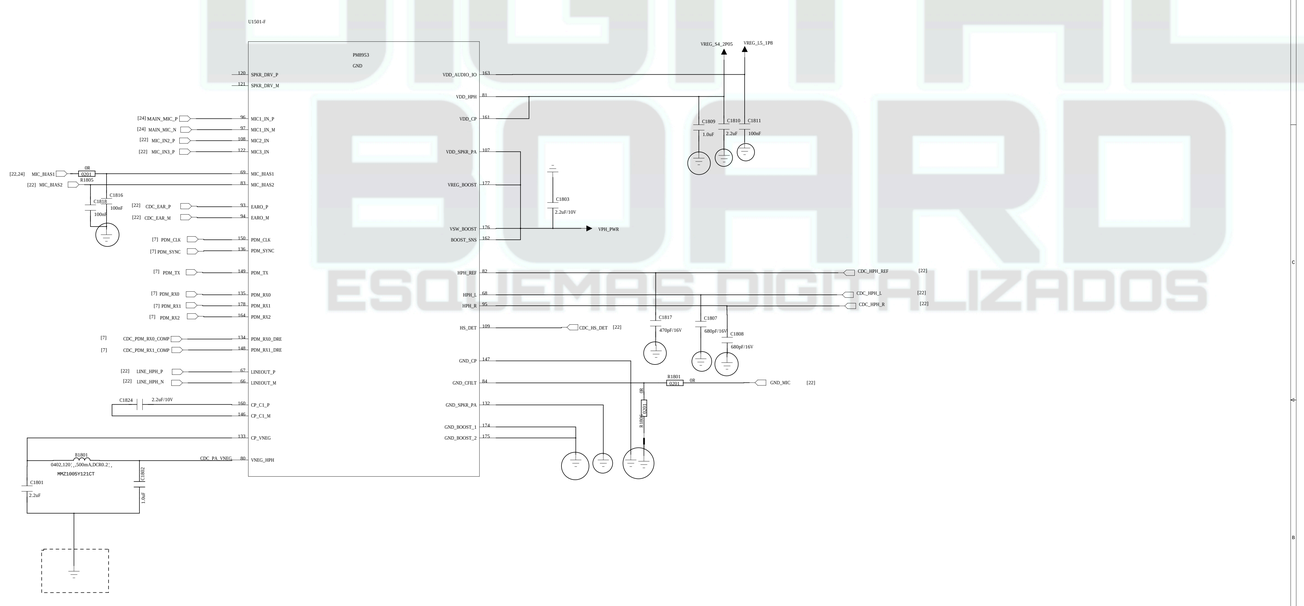

PM8953 CODEC/Audio PA

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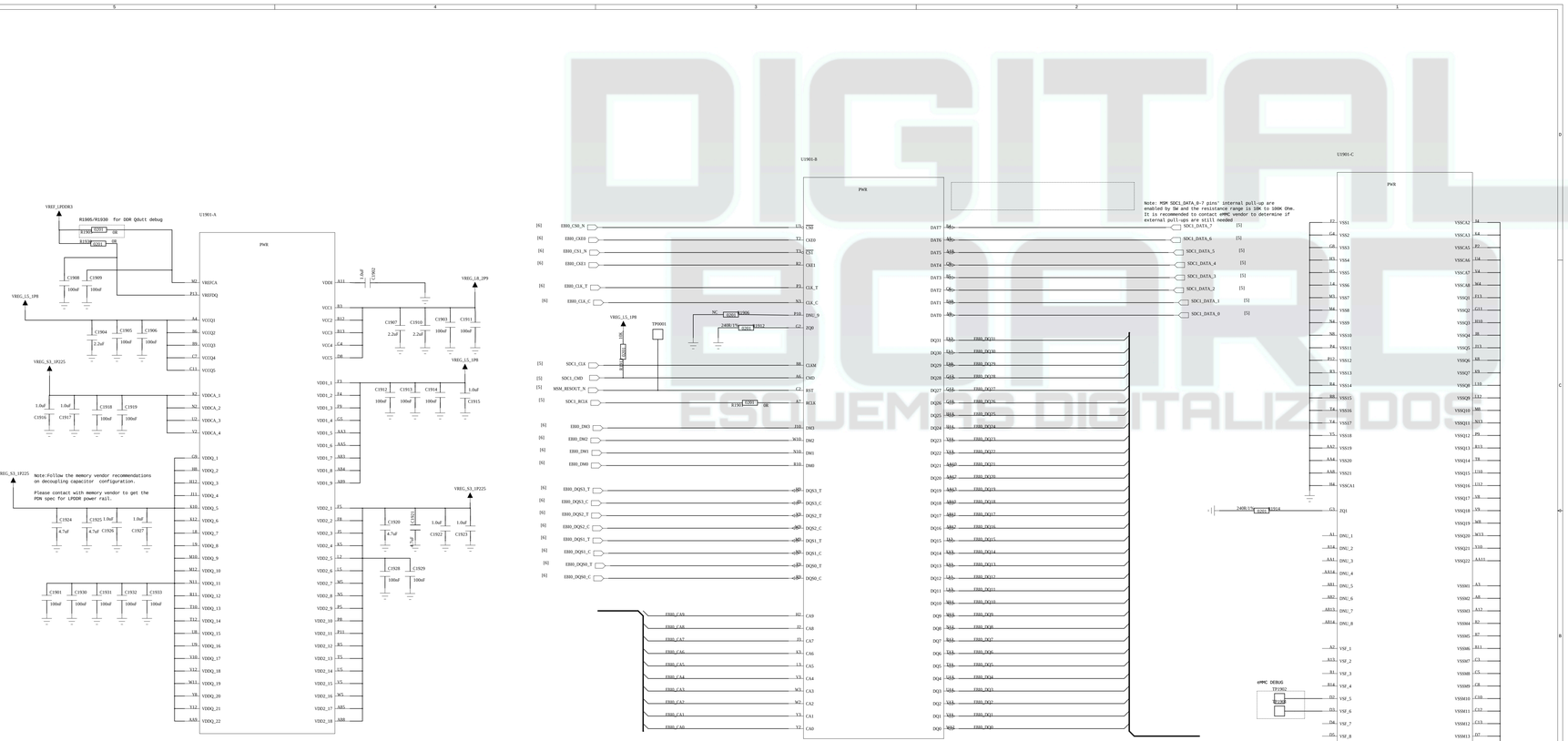

MEMORY(LPDDR3+EMMC V5.1)

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REVISION RECORD			
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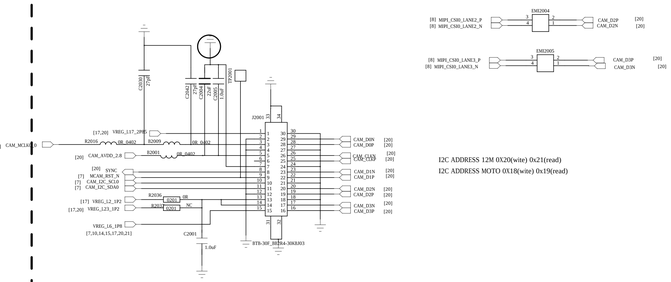
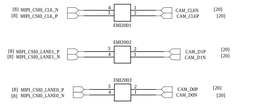
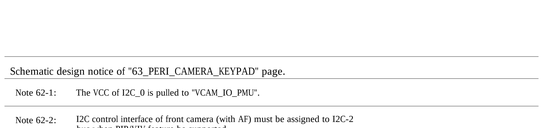
Main Camera A



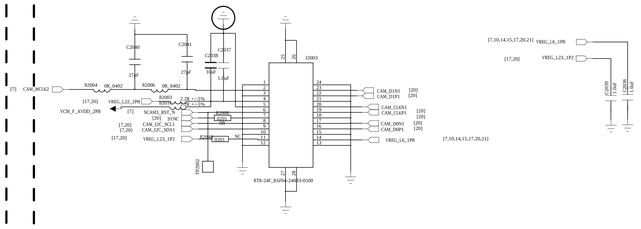


I2C ADDRESS 12M 0X20(wite) 0x21(read)
I2C ADDRESS MOTO 0X18(wite) 0x19(read)

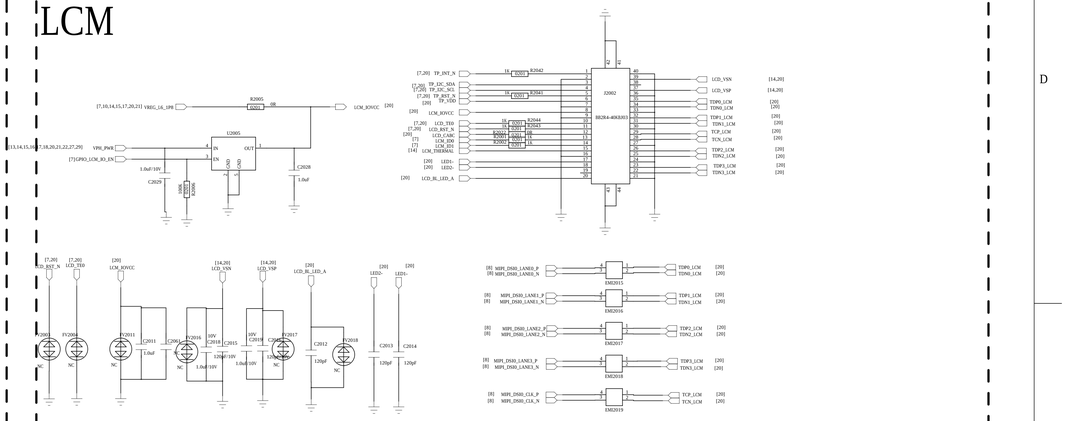


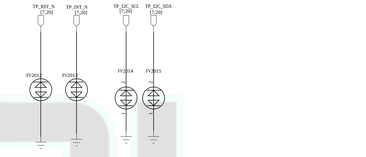
Main Camera B

I2C ADDRESS 5M 0X20(wite) 0x21(read)

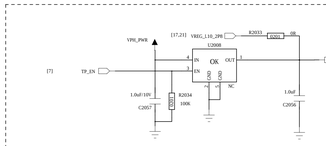


LCM

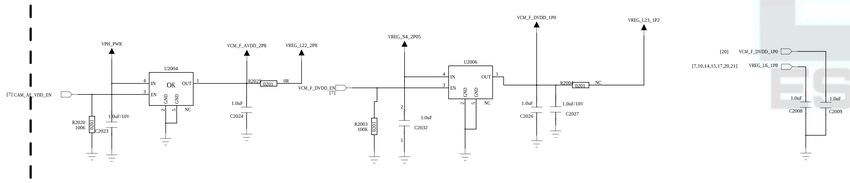


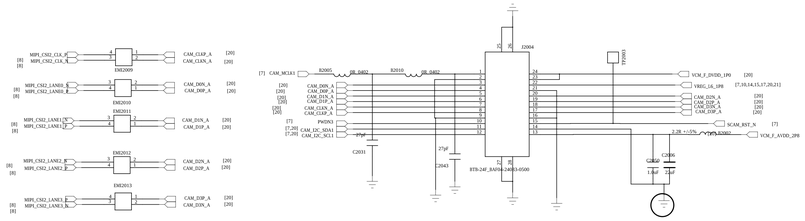


LDO



Front Camera



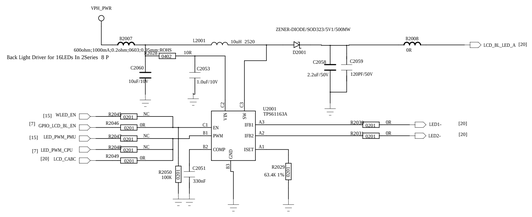


I2C ADDRESS 2M 0X7a(wite) 0x7b(read)

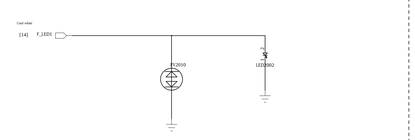
Schematic design notice of "63_PERI_CAMERA_KEYPAD" page.

Note 62-1:	The VCC of I2C_0 is pulled to "VCAM_IO_PMU".
Note 62-2:	I2C control interface of front camera (with AF) must be assigned to I2C-2 bus when PIP/VIV feature be supported.
Note 62-3:	Reserve a capacitor (27pF) on camera's MCLK and shunt it to GND to prevent GPS de-sense.

LCM Black Light



Main FLASHLIGHT



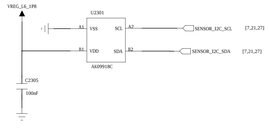
COMPANY:	<Company Name>		
TITLE:	<Title>		
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 30 31

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

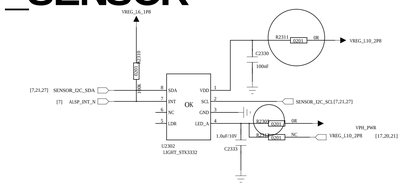
L-SENSOR

M-Sensor

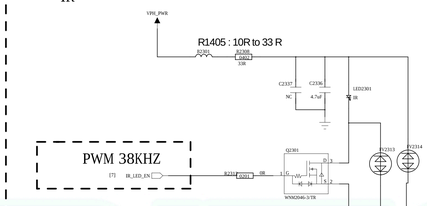
M-Sensor I2C Address: 0x0C

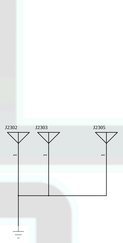


P_SENSOR

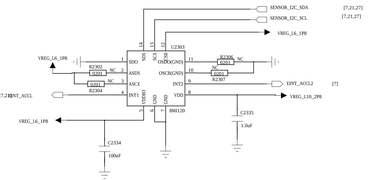


IR



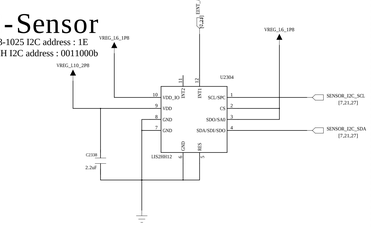


ACC-Sensor

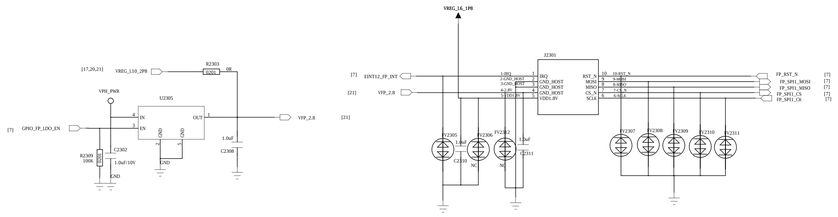


ACC-Sensor

KX023-1025 I2C address : 1E
LIS3DH I2C address : 0011000b



FingerPrint-Sensor

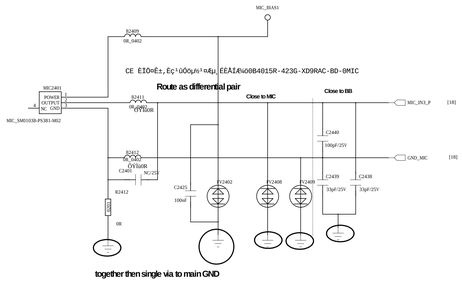


MARK POINT

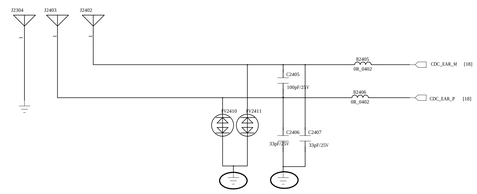
COMPANY: <Company Name>			
TITLE: <Title>			
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		
CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
SCALE: <Scale>		SHEET: 21 31	

REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE:

Sub MIC

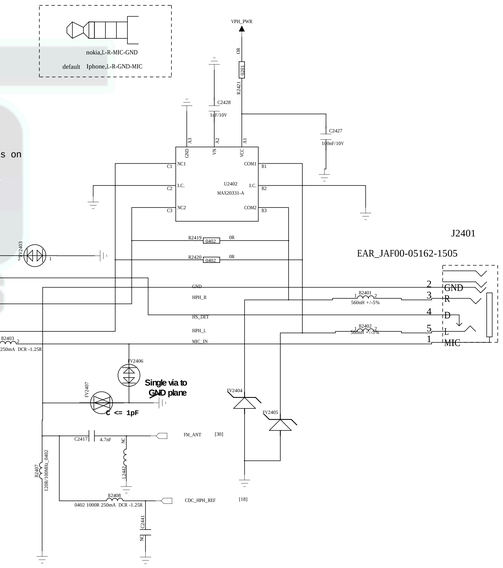


REC



Audio PA

Earphone Audio



Note: Ferrite beads and their corresponding bypass capacitors on on CDC_HPH_L_P, CDC_HPH_L_M and CDC_HPH_REF are needed to reduce noise generated by audio/FM concurrency

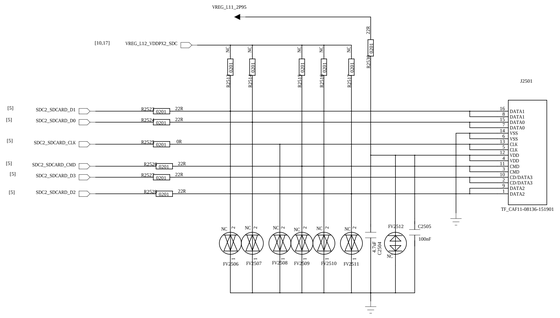
Note: Place B202,B203,C216,C217 close to headset jack connector

Note: For Cable detection

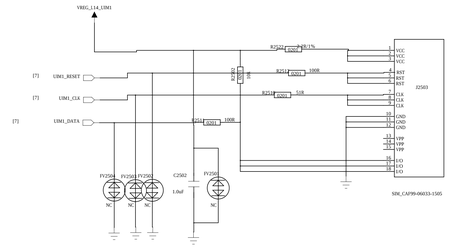
DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
		SCALE: <Scale>	SHEET: 31

LTR	ECO NO:	APPROVED:	DATE:

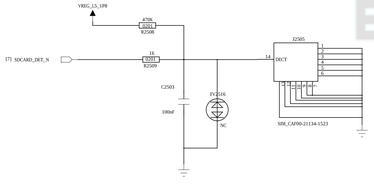
T-Card



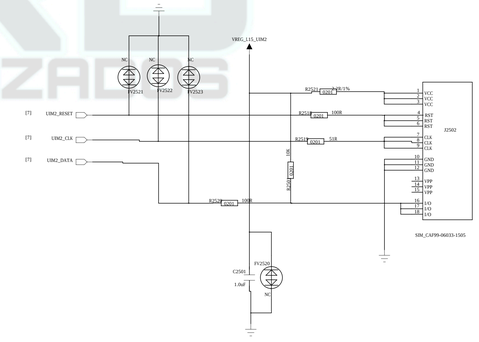
SIM1



INT

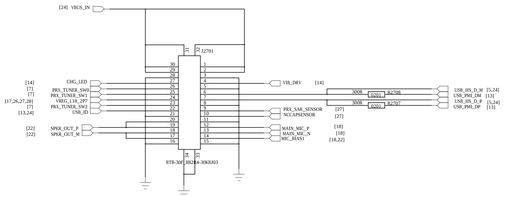


SIM2

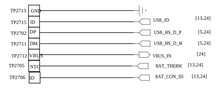


DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
		SCALE: <Scale>	SHEET: 28 31

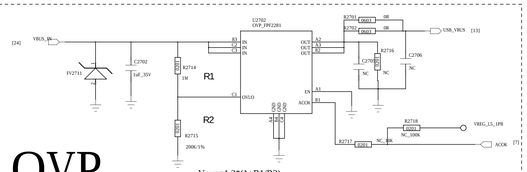
SUB_FPC



Test point



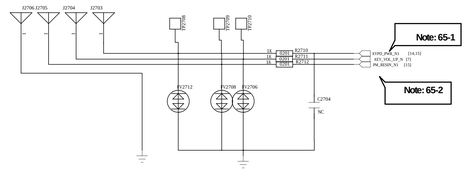
OVP



Vovp=1.2*(1+R1/R2)

R1 Min 1M

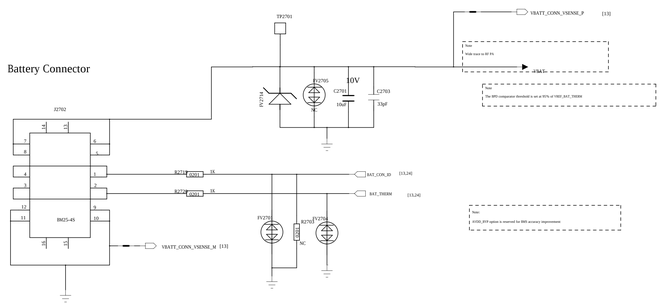
Power Key



Schematic design notice of "65_PERI_Dual_SIM_ICUSB_KEYPAD" page.

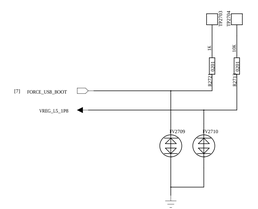
Note 65-1:	DO NOT put pull-up resistor on PWRKEY
Note 65-2:	Volume Up : HOME Key / GND Volume Down : (KPROW0/KPCOL0) or KPCOL0 / GND

BAT

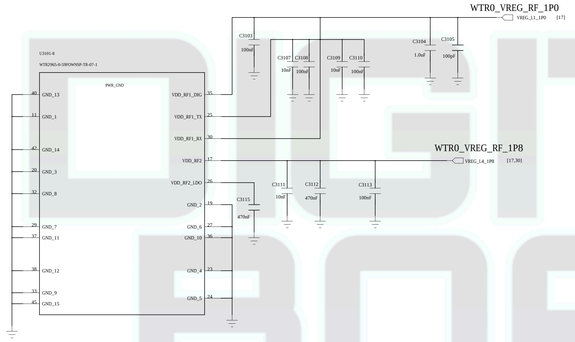


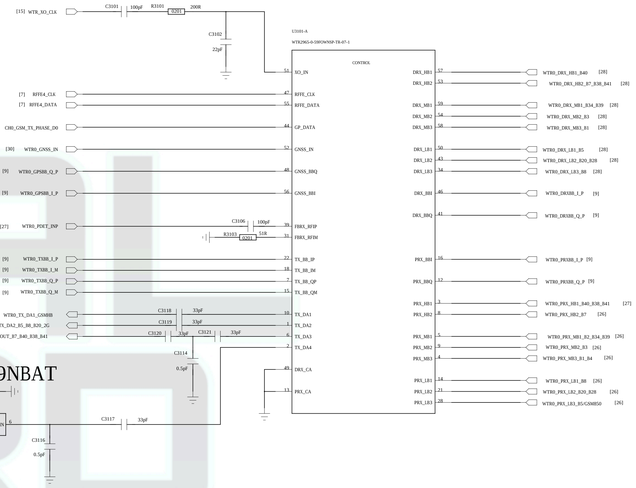
Note:
Battery ID resistor value require 20K~150K,
Add 100K to ground If battery package ID not meet requirement

Force USB boot



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

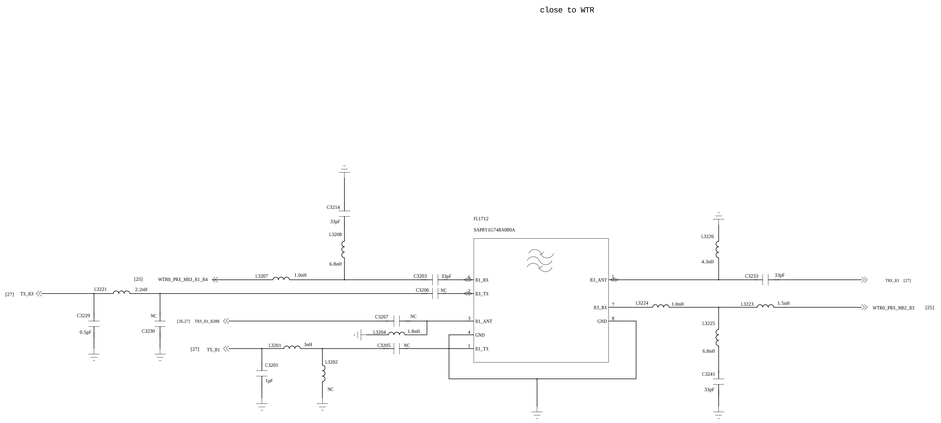




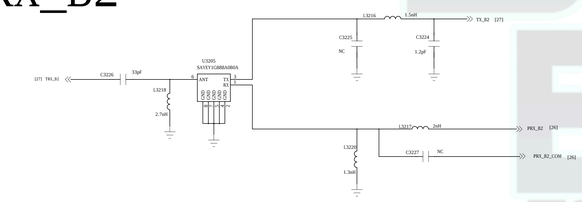
Note:RX ports have DC at the pin, so it need DC block,
please make sure there is no DC short to other voltages and GND

COMPANY: <Company Name>			
TITLE: <Title>			
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>	SHEET: 25 31

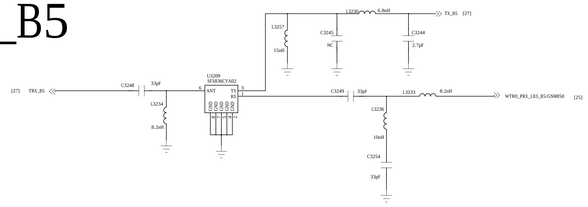
TRX_B1 TRX_B3



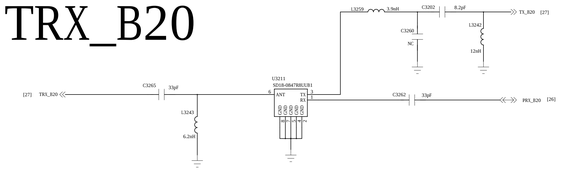
TRX_B2



TRX_B5

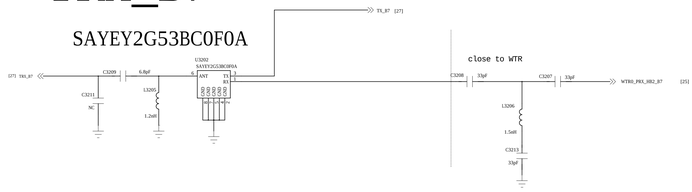


TRX_B20



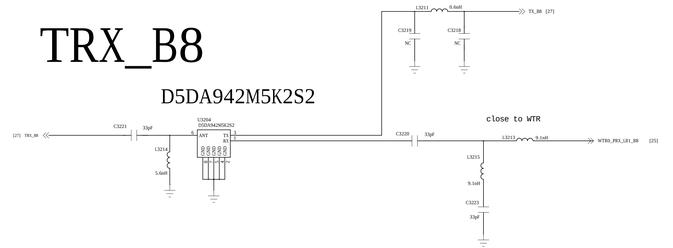
TRX_B7

SAYEY2G53BC0F0A

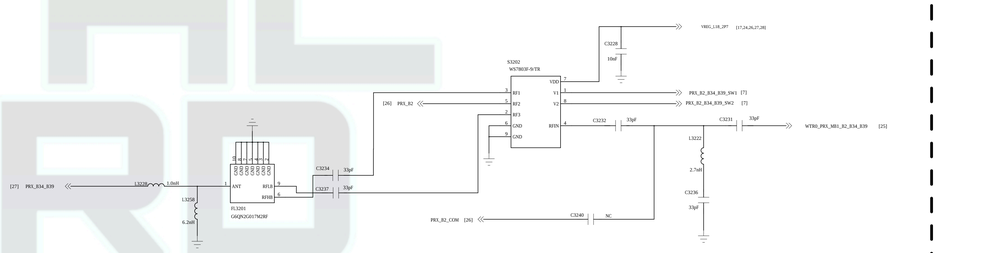


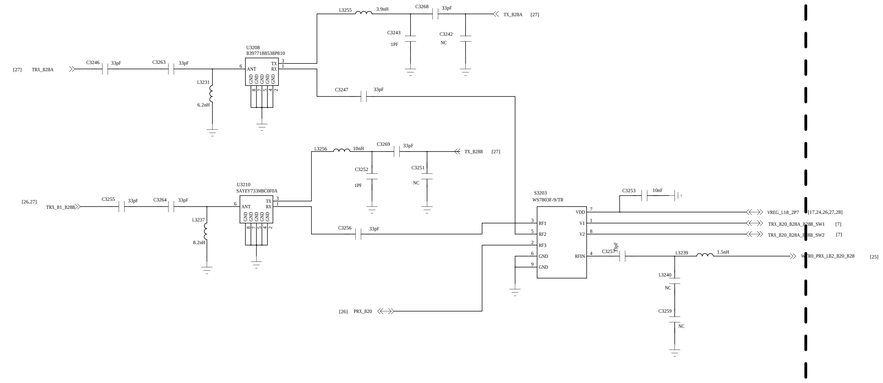
TRX_B8

D5DA942M5K2S2



TRX_TDS_B34_B39





COMPANY:	<Company Name>		
TITLE:	20_LTE_DUPLEXER		
CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
DRAWN: LiuMengya	DATED: <Drawn Date>		
CHECKED: LiLi	DATED: <Checked Date>	SCALE: <Scale>	SHEET: 26 of 81

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

TXM

X.FL-R-SMT-1(80)

MM8030-2610B

SKY77912-61C

SAR Sensor

S3S325

MMPA

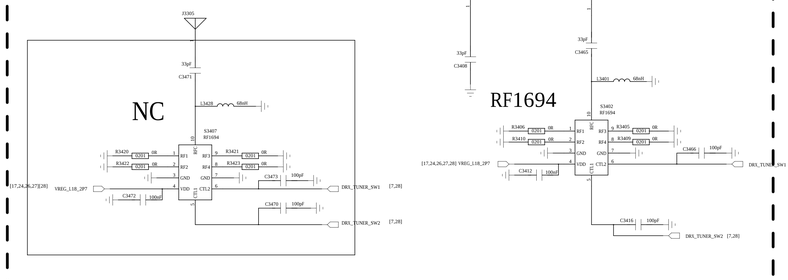
B39262B8870L210

ACX BF1608-L1R9NDB

Near to PA

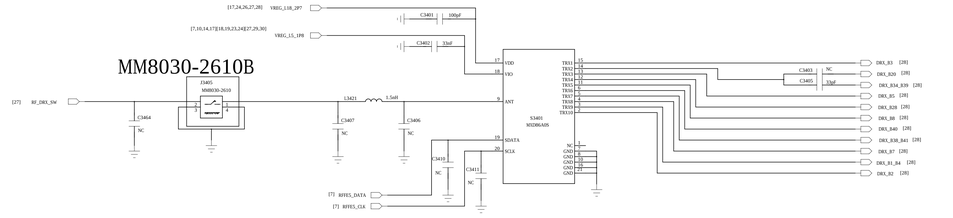
DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number>×<Revision>	REV:
		SCALE: <Scale>	SHEET: 30 31

ANT Switch

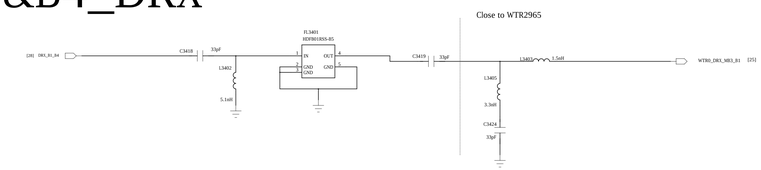


DRX

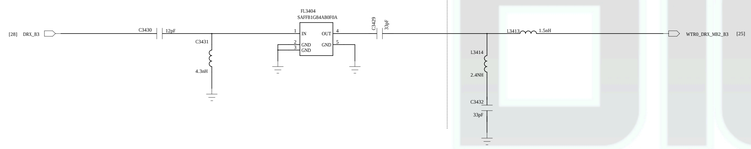
MM8030-2610B



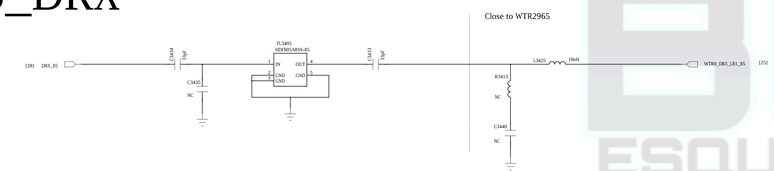
B1&B4_DRX



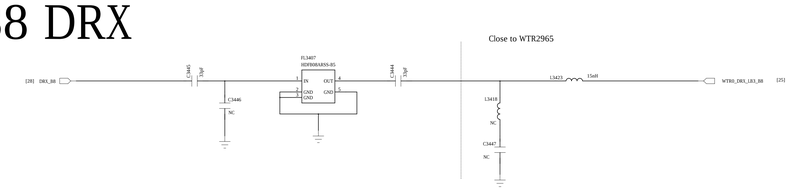
B3_DRX



B5_DRX

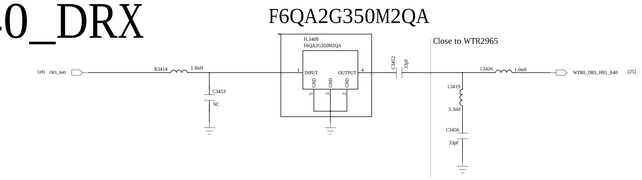


B8 DRX



B40_DRX

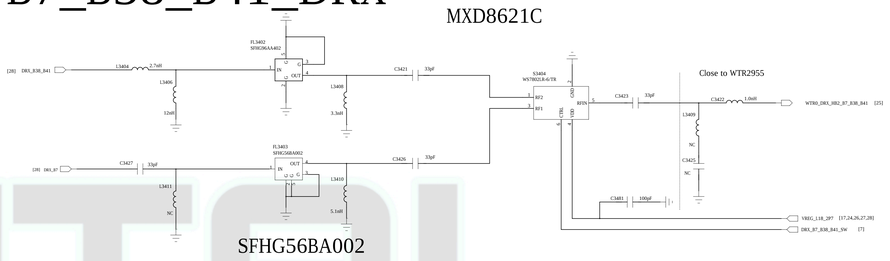
F6QA2G350M2QA



B7_B38_B41_DRX

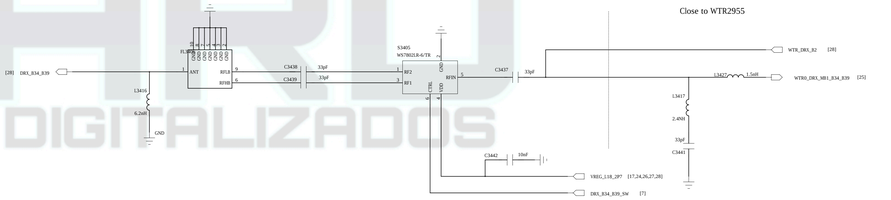
MXD8621C

SFHG56BA002

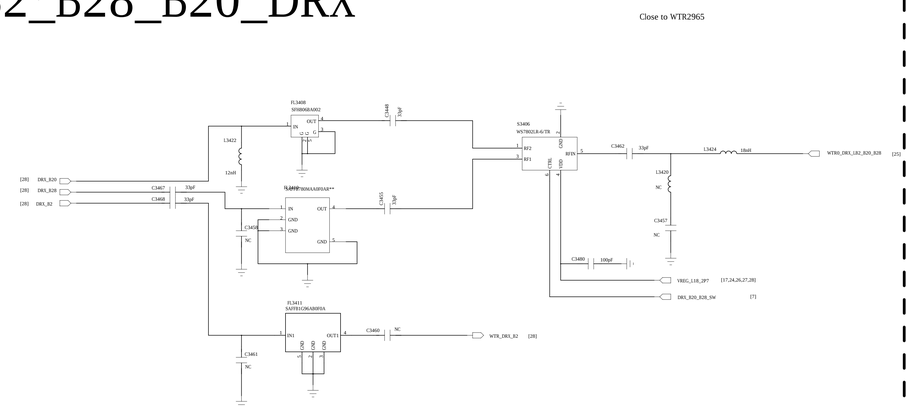


B34_B39_DRX

MXD8621C

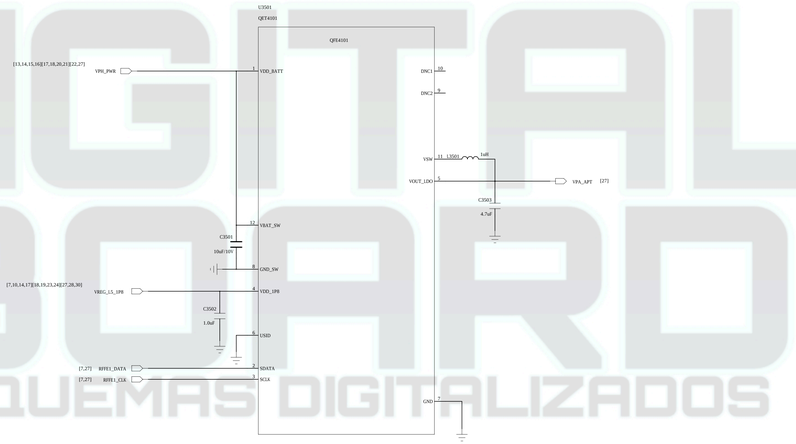


B2_B28_B20_DRX



COMPANY:	<Company Name>
TITLE:	21_LTE_B7
CODE: <Code>	SIZE: A0
DRAWING NO: <Drawing Number>	REV: <Revision>
DRAWN: LiuMengya	DATED: <Drawn Date>

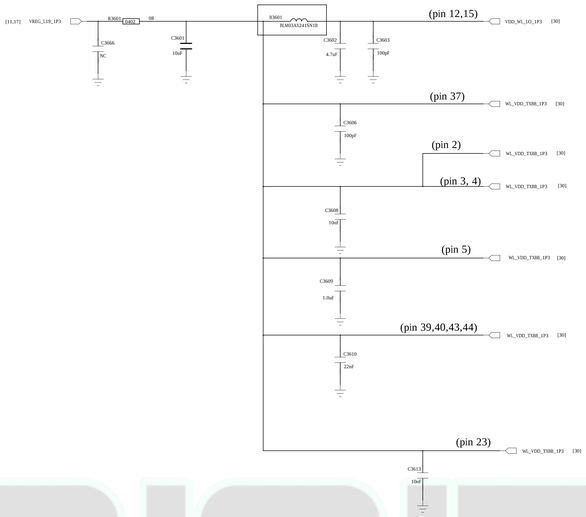
APT



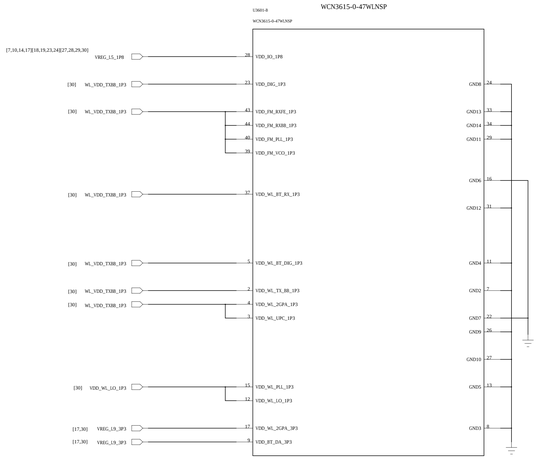
DRAWN: LiuMengya	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: LiLi	DATED: <Checked Date>	TITLE: 22_DRX	
		CODE: <Code>	SIZE: A0
		DRAWING NO: <Drawing Number>	REV: <Revision>
		SCALE: <Scale>	SHEET: 29 OF 31

WCN

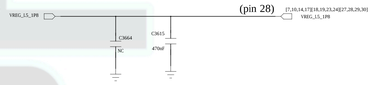
BLM03AX241SN1B



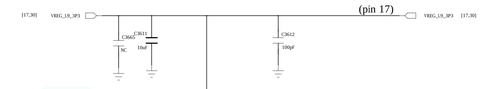
WCN3615-0-47WLNSP



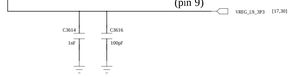
(pin 28)



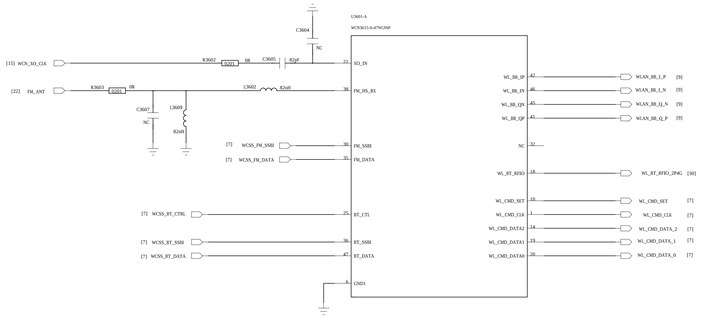
(pin 17)



(pin 9)



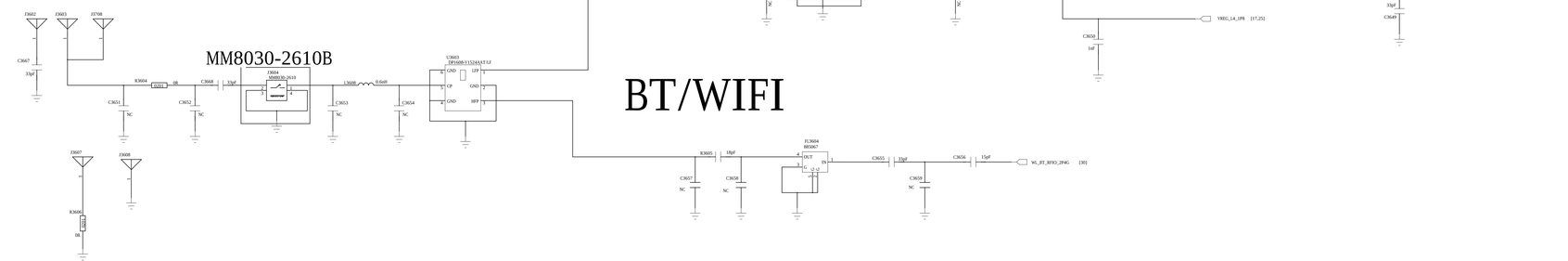
U3601-A WCN3615-0-47WLNSP



GNSS

BT/WIFI

MM8030-2610B



COMPANY:	<Company Name>		
TITLE:	24_WCN3680B		
CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
DRAWN: LiuMengya	DATED: <Drawn Date>		
CHECKED: LiLi	DATED: <Checked Date>	SCALE: <Scale>	SHEET: 30 OF 31