

REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE:

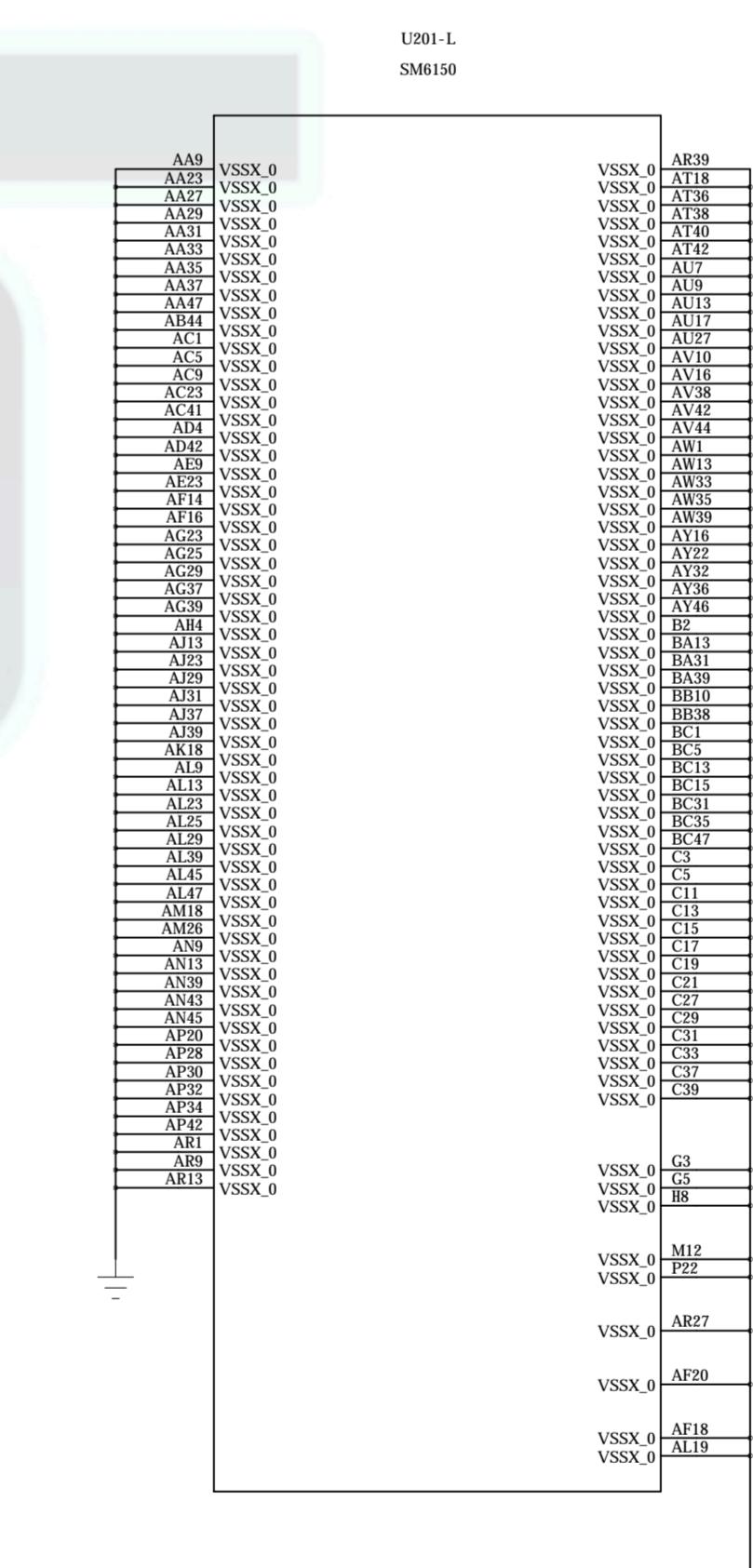
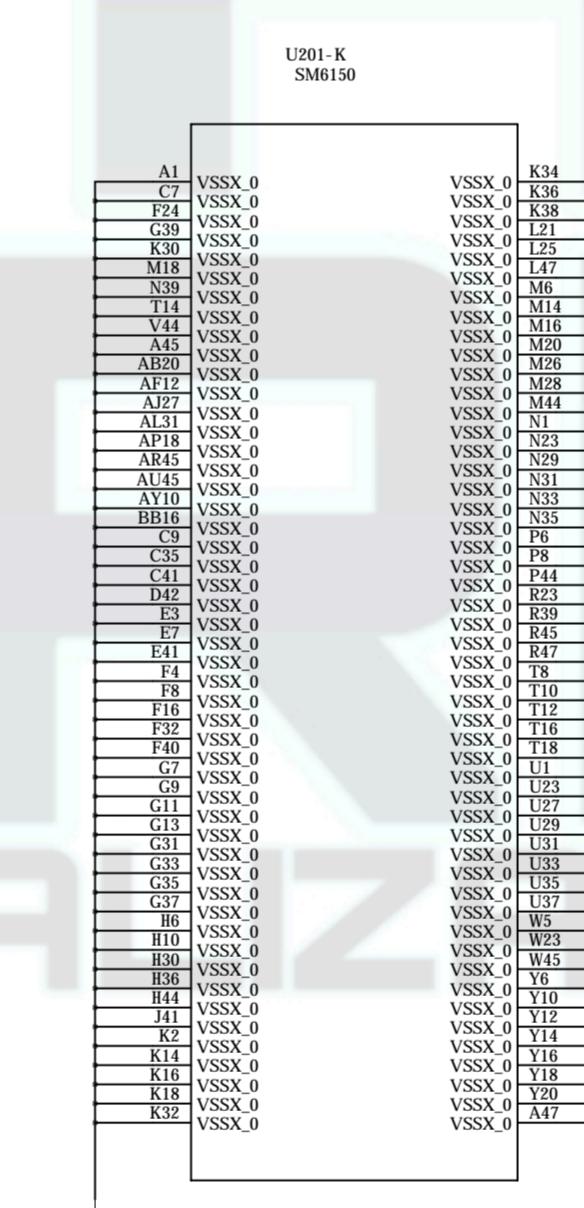
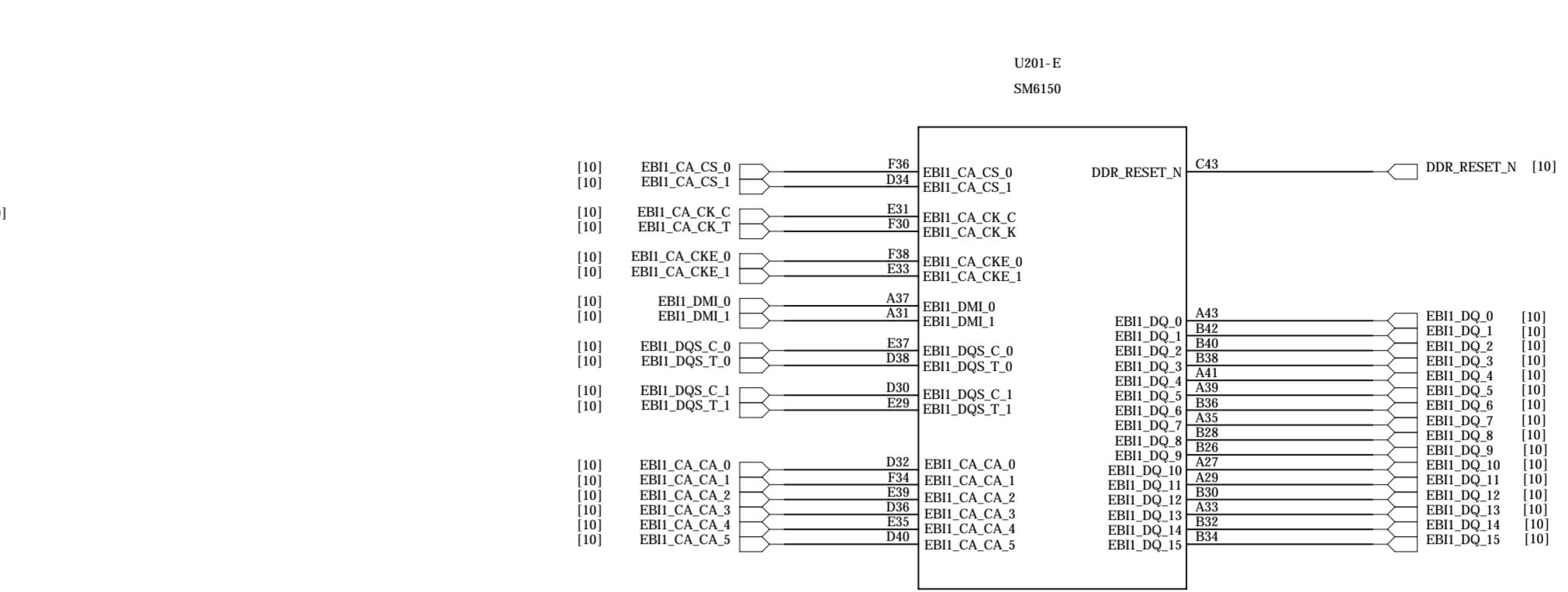
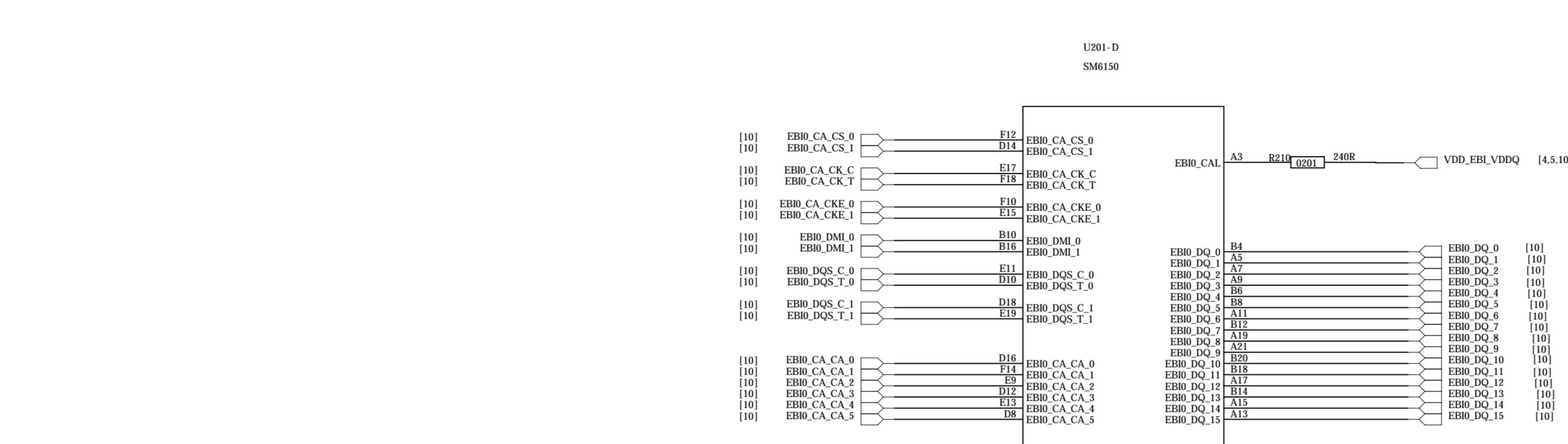
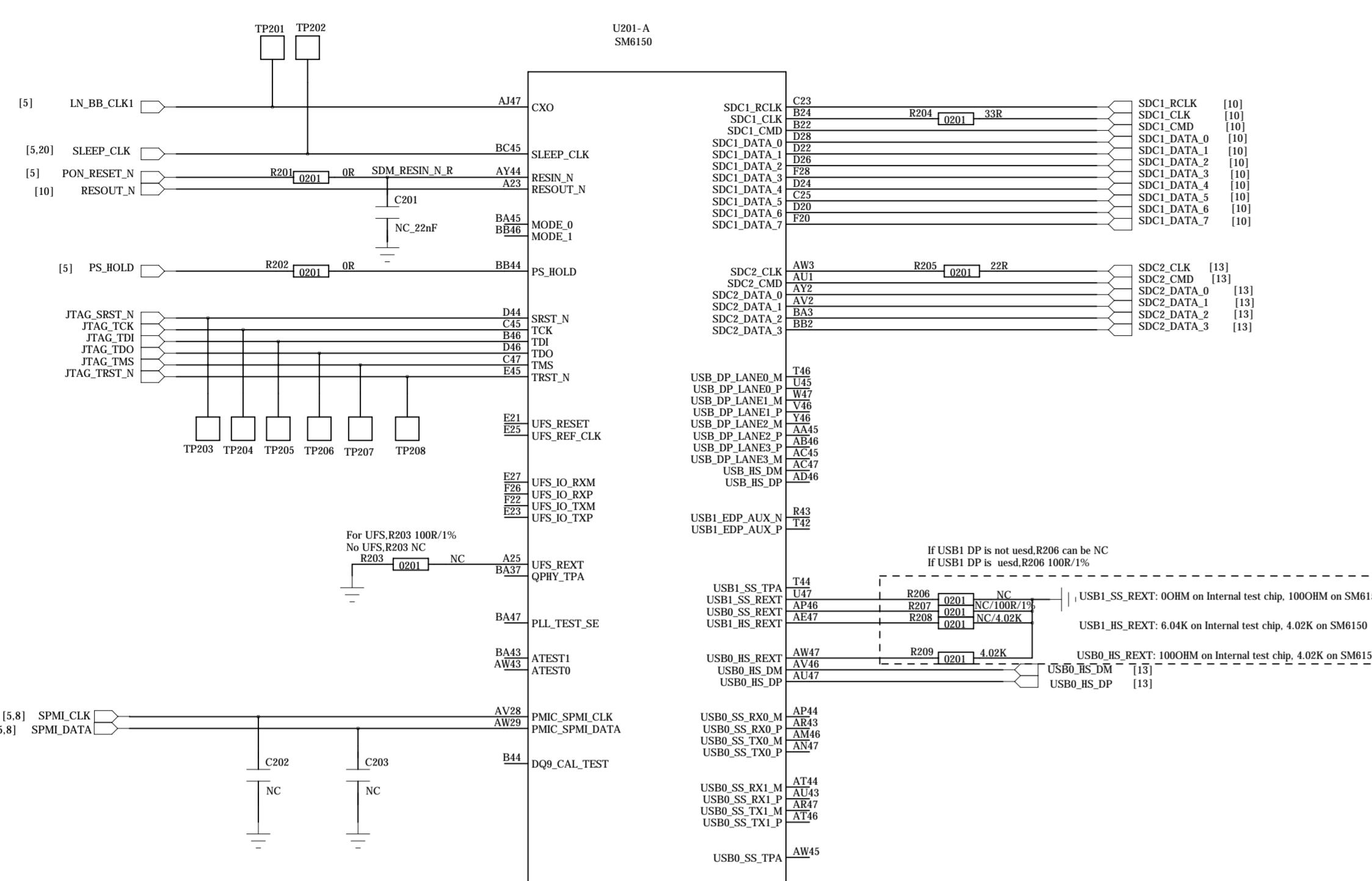
SDM636 GPIO Configuration For Starlord					
GPIO_0	FP_SPI_MISO	GPIO_50	NFC_CLKREQ	GPIO_100	NC
GPIO_1	FP_SPI_MOSI	GPIO_51	QLINK_REQUEST	GPIO_101	FP_RESET_N
GPIO_2	FP_SPI_SLCK	GPIO_52	QLINK_ENABLE	GPIO_102	WLAN_SW_CTRL
GPIO_3	I2C_TP_CS_N	GPIO_53	NC	GPIO_103	LCD_ID
GPIO_4	TS_I2C_SDA	GPIO_54	NC	GPIO_104	USB_PHY_PS
GPIO_5	TS_I2C_SCL	GPIO_55	NC	GPIO_105	WMSS_RESET
GPIO_6	ESE_SPI_MISO	GPIO_56	NC	GPIO_106	MSS_LTE_COXM_TXD
GPIO_7	ESE_SPI_MOSI	GPIO_57	NC	GPIO_107	MSS_LTE_COXM_RXD
GPIO_8	ESE_SPI_SLCK	GPIO_58	NC	GPIO_108	WSA_SPKR_SD_N_1
GPIO_9	ESE_SPI_CS_N	GPIO_59	NC	GPIO_109	NC
GPIO_10	BT_UART_CTS_N	GPIO_60	NC	GPIO_110	WSA_DATA
GPIO_11	BT_UART_RFR_N	GPIO_61	RFFE1_DATA	GPIO_111	WSA_CLK
GPIO_12	BT_UART_TX_N	GPIO_62	RFFE1_CLK	GPIO_112	RCM_MARKER2
GPIO_13	BT_UART_RX_N	GPIO_63	RFFE2_DATA	GPIO_113	NC
GPIO_14	NFC_I2C_SDA	GPIO_64	RFFE2_CLK	GPIO_114	NC
GPIO_15	NFC_I2C_SCL	GPIO_65	RFFE3_DATA	GPIO_115	NC
GPIO_16	DEBUG_UART_TX	GPIO_66	RFFE3_CLK	GPIO_116	NC
GPIO_17	DEBUG_UART_RX	GPIO_67	RFFE4_DATA	GPIO_117	NC
GPIO_18	SHARED_I2C_SDA	GPIO_68	RFFE4_CLK	GPIO_118	NC
GPIO_19	SHARED_I2C_SCL	GPIO_69	RFFE5_DATA	GPIO_119	NC
GPIO_20	NC	GPIO_70	RFFE5_CLK	GPIO_120	NC
GPIO_21	NC	GPIO_71	RFFE6_CLK	GPIO_121	NC
GPIO_22	NC	GPIO_72	RFFE6_DATA	GPIO_122	NC
GPIO_23	NC	GPIO_73	UIM2_DATA		
GPIO_24	NC	GPIO_74	UIM2_CLK	LPI_0	SSC_I2C_1_SDA
GPIO_25	NC	GPIO_75	UIM2_RESET	LPI_1	SSC_I2C_1_SCL
GPIO_26	NC	GPIO_76	UIM1_PRESENT	LPI_2	SSC_SPI1_MISO
GPIO_27	NC	GPIO_77	UIM1_DATA	LPI_3	SSC_SPI1_MOSI
GPIO_28	CAM_MCLK0	GPIO_78	UIM1_CLK	LPI_4	SSC_SPI1_SCLK
GPIO_29	CAM_MCLK1	GPIO_79	UIM1_RESET	LPI_5	SSC_SPI1_CS0_N
GPIO_30	CAM_MCLK2	GPIO_80	UIM1_PRESENT	LPI_6	NC
GPIO_31	CAM_MCLK3	GPIO_81	ACCEL_INT	LPI_7	NC
GPIO_32	CCI_I2C_SDA0	GPIO_82	GYRO_INT	LPI_8	TS_SPI_MISO
GPIO_33	CCI_I2C_SCL0	GPIO_83	MAG_RDY_INT	LPI_9	TS_SPI_MOSI
GPIO_34	CCI_I2C_SDA1	GPIO_84	NFC_ENABLE	LPI_10	TS_SPI_SCLK
GPIO_35	CCI_I2C_SCL1	GPIO_85	NFC_DWL_REQ	LPI_11	TS_SPI_CS_N
GPIO_36	NC	GPIO_86	NFC_IRQ	LPI_12	LPI_UART1_TX
GPIO_37	CAM2_RST_N	GPIO_87	NC	LPI_13	LPI_UART1_RX
GPIO_38	NC	GPIO_88	TS_TESET_M	LPI_14	LPI_UART2_TX
GPIO_39	FL_STROBE_TRIG	GPIO_89	TS_INT_N	LPI_15	LPI_UART2_RX
GPIO_40	NC	GPIO_90	MDP_VSYNC_P	LPI_16	NC
GPIO_41	NC	GPIO_91	LCD0_RESET_N	LPI_17	NC
GPIO_42	NC	GPIO_92	ALSPG_INT_N	LPI_18	SWR_RX_CLK
GPIO_43	FROCED_USB_BOOT_POLARITY	GPIO_93	FP_INT_N1	LPI_19	SWR_RX_DATA1
GPIO_44	NC	GPIO_94	FP_INT_N2	LPI_20	SWR_RX_DATA2
GPIO_45	CAM1_RST_N	GPIO_95	NC	LPI_21	SWR_RX_CLK
GPIO_46	DVDD1_P2_EN	GPIO_96	NC	LPI_22	SWR_RX_DATA1
GPIO_47	CAM0_RST_N	GPIO_97	RCM_MARKER1	LPI_23	SWR_RX_DATA2
GPIO_48	WCSS_PWR_REQ	GPIO_98	NC	LPI_24	CODEC_RST_N
GPIO_49	NC	GPIO_99	SD_CARD_DET_N	LPI_25	NC

PM6150	
GPIO_01	NC
GPIO_02	NC
GPIO_03	SMB_STAT
GPIO_04	NC
GPIO_05	SLB
GPIO_06	SD_CARD_DET_N
GPIO_07	NFC_SLEEP_CLK
GPIO_08	NC
GPIO_09	FMB1
GPIO_10	FMB2
AMUX_THERM1	Option_1
AMUX_THERM2	MSM_THERM
AMUX_THERM3	SMB_THERM
AMUX_THERM4	CONN_THERM

PM6150L	
GPIO_01	AOSS_SLEEP_INDICATOR
GPIO_02	KYPD_VOLP_N
GPIO_03	DVDD1_P2_EN
GPIO_04	AVDD1_P2B_EN
GPIO_05	CAM_FLASH_THERM
GPIO_06	NC
GPIO_07	SLB
GPIO_08	NC
GPIO_09	AVDD0_2P8_EN
GPIO_10	QUIET_THERM
GPIO_11	NC
GPIO_12	NC
AMUX_THERM1	EMMC_THERM
AMUX_THERM2	PA_THERMO
AMUX_THERM3	NC

COMPANY: <Company Name>	
TITLE: <Title>	
DRAWN: <Drawn By>	DATED: <Drawn Date>
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SCALE: <Scale>	REV: <Rev>
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REVISION RECORD			
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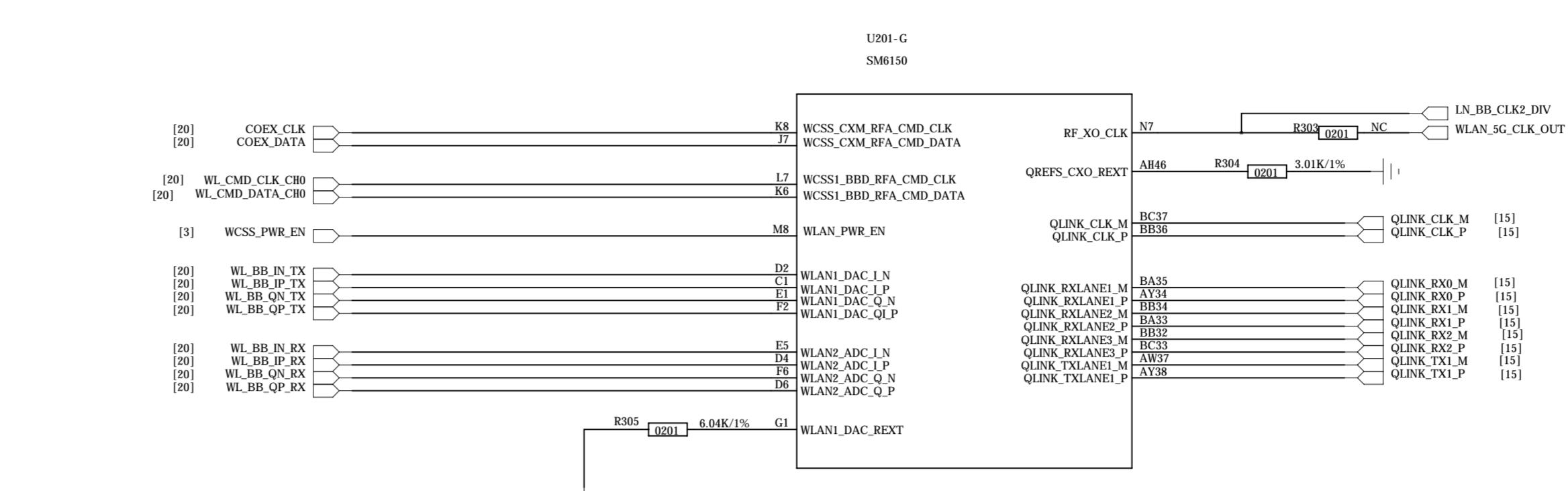
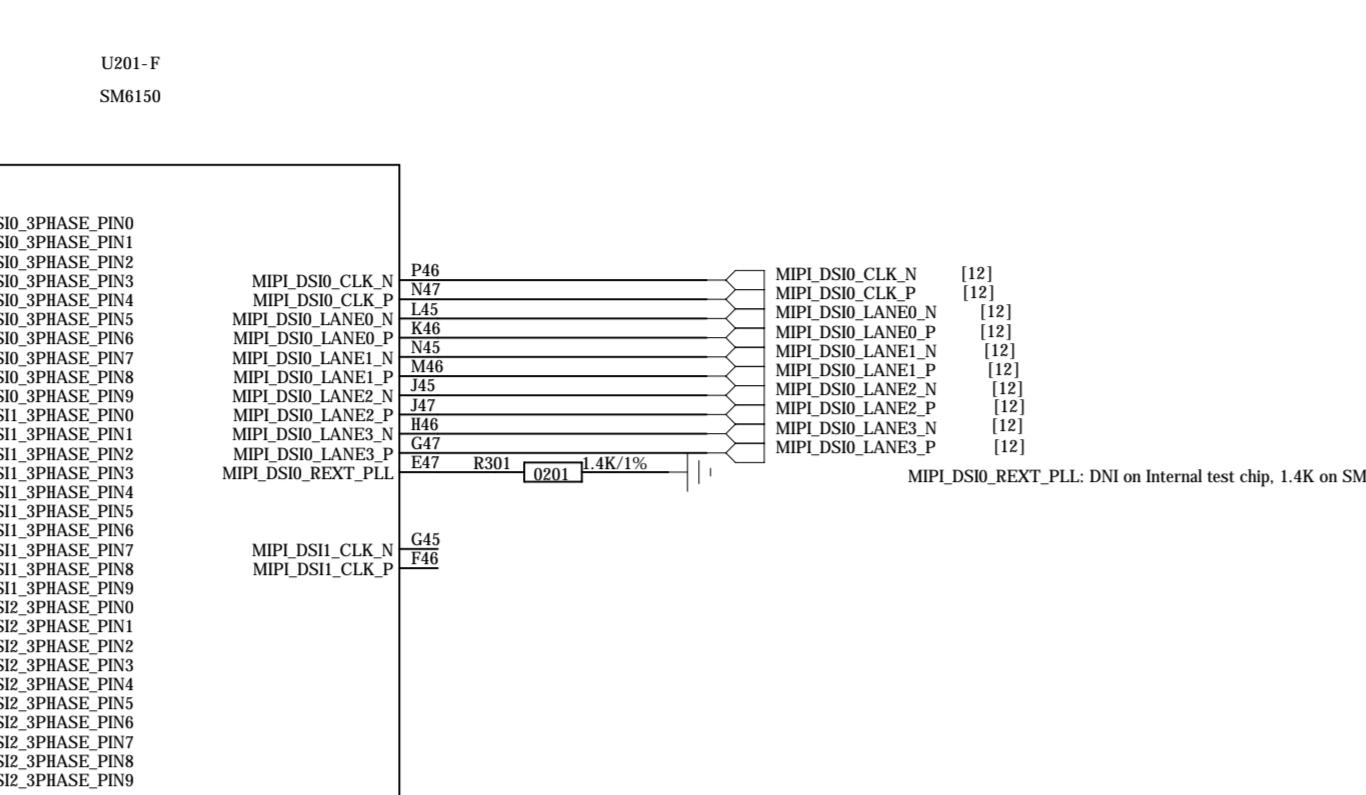
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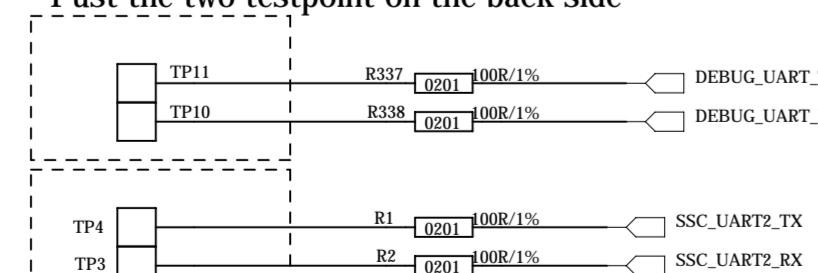
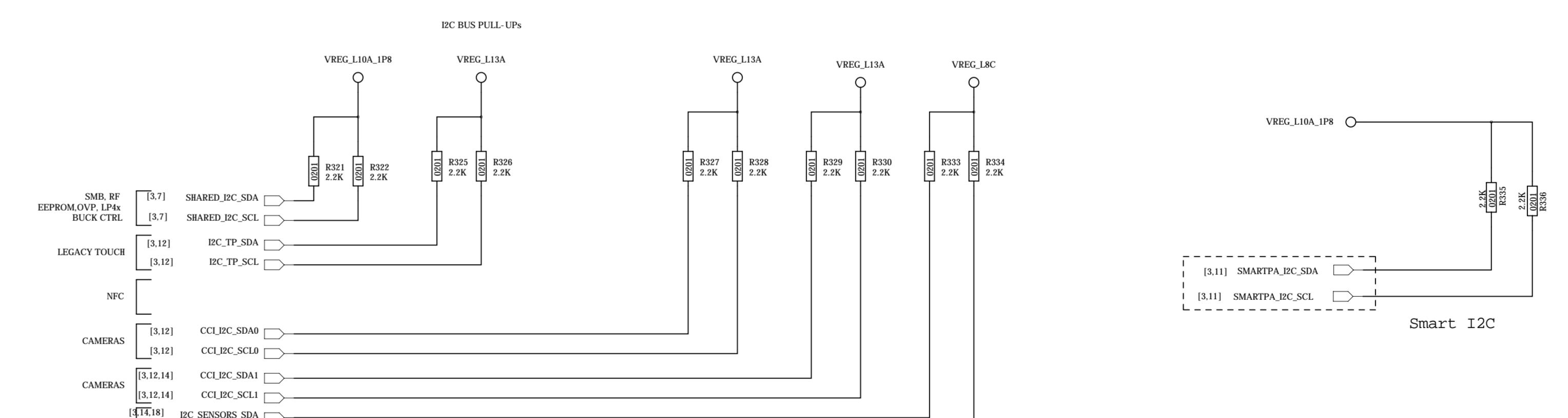
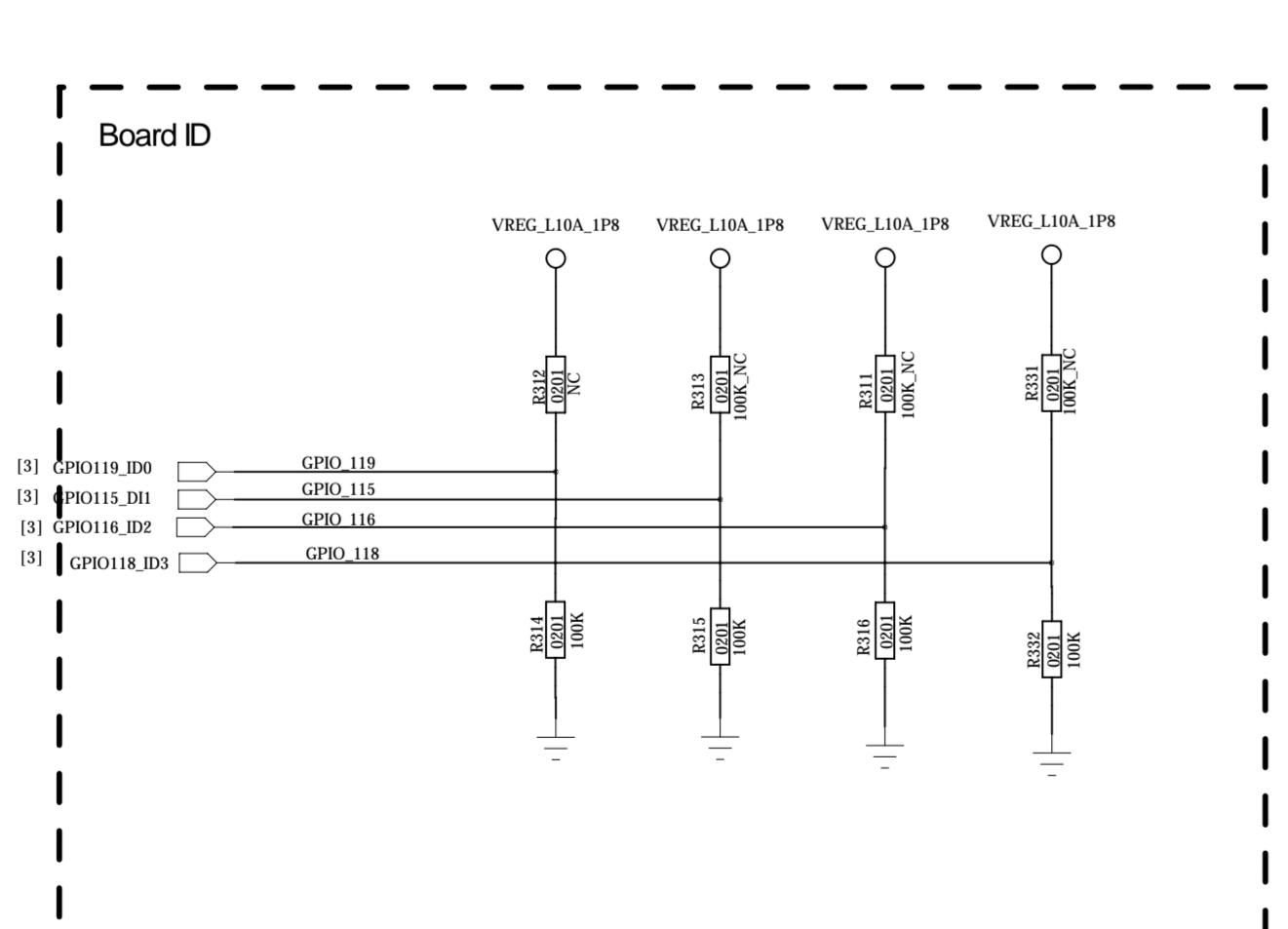
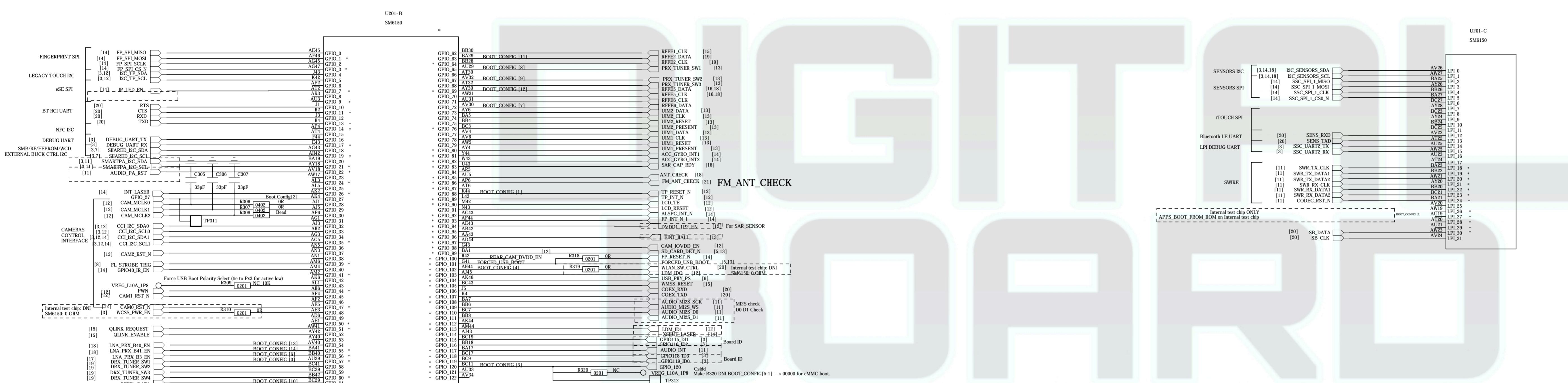
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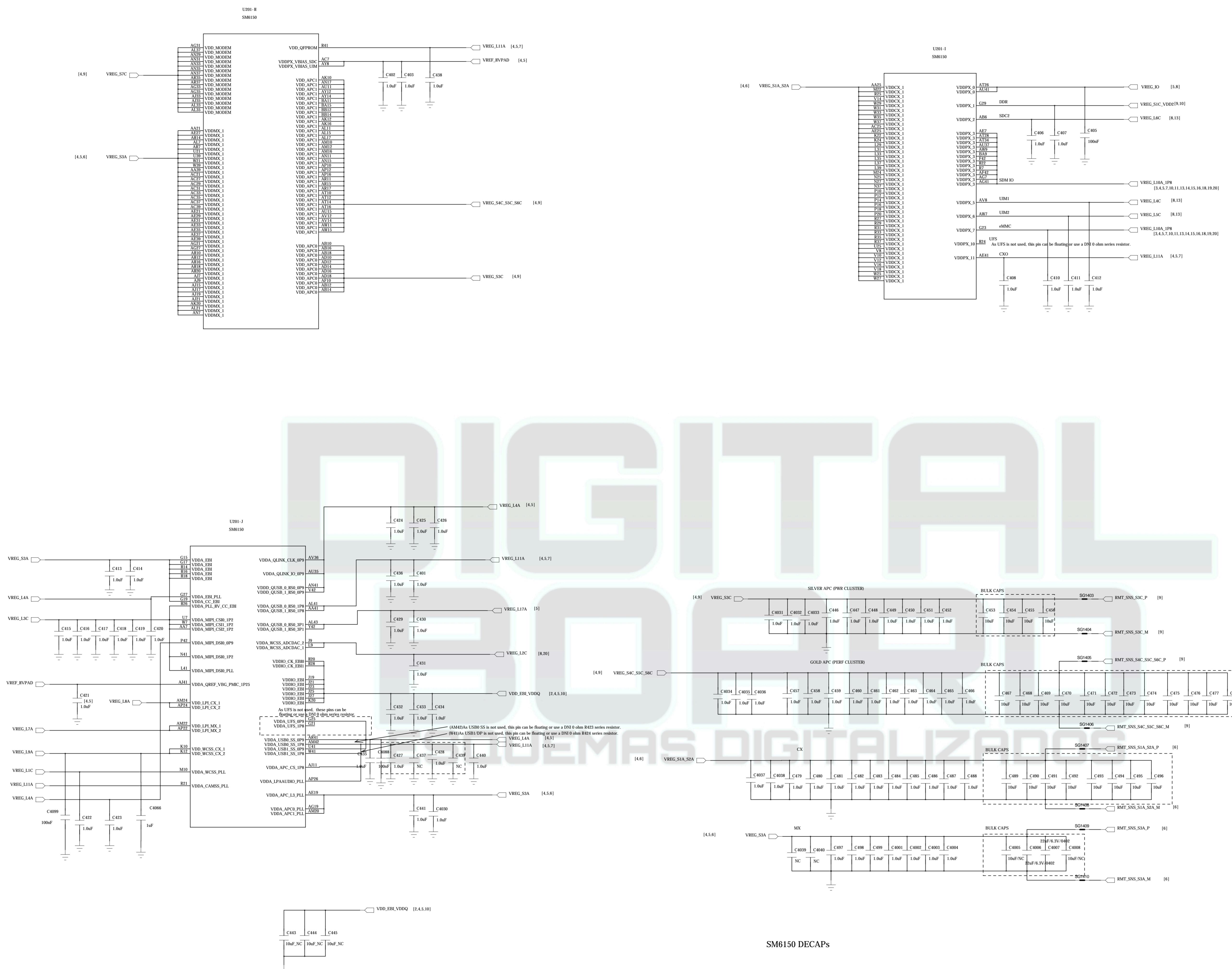
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Add C1001,C1002,C1003,C1004 place holders for CLK desense to improve Rx sensitivity.



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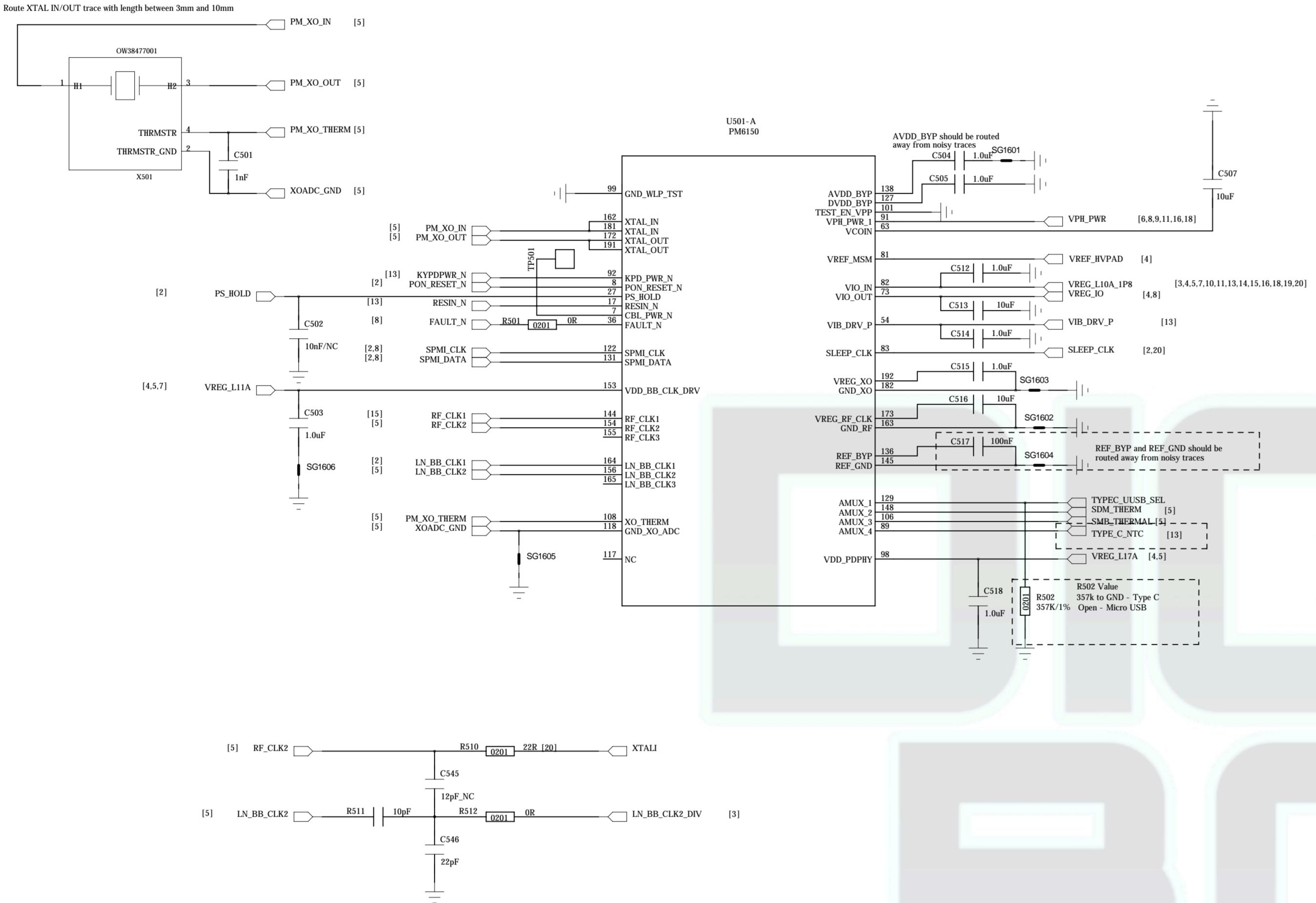
COMPANY: <b>&lt;Company Name&gt;</b>			
TITLE: <b>&lt;Title&gt;</b>			
CODE: <b>&lt;Code&gt;</b>	SIZE: <b>A0</b>	DRAWING NO: <b>&lt;Drawing Number&gt;×Revision</b>	REV:
CALE: <b>&lt;Scale&gt;</b>		SHEET: <b>4E</b>	<b>22</b>

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## Layout Note:

No trace shall be present in at-least two immediate layers below XTAL.  
Route XTAL IN/OUT trace with length between 3mm and 10mm.

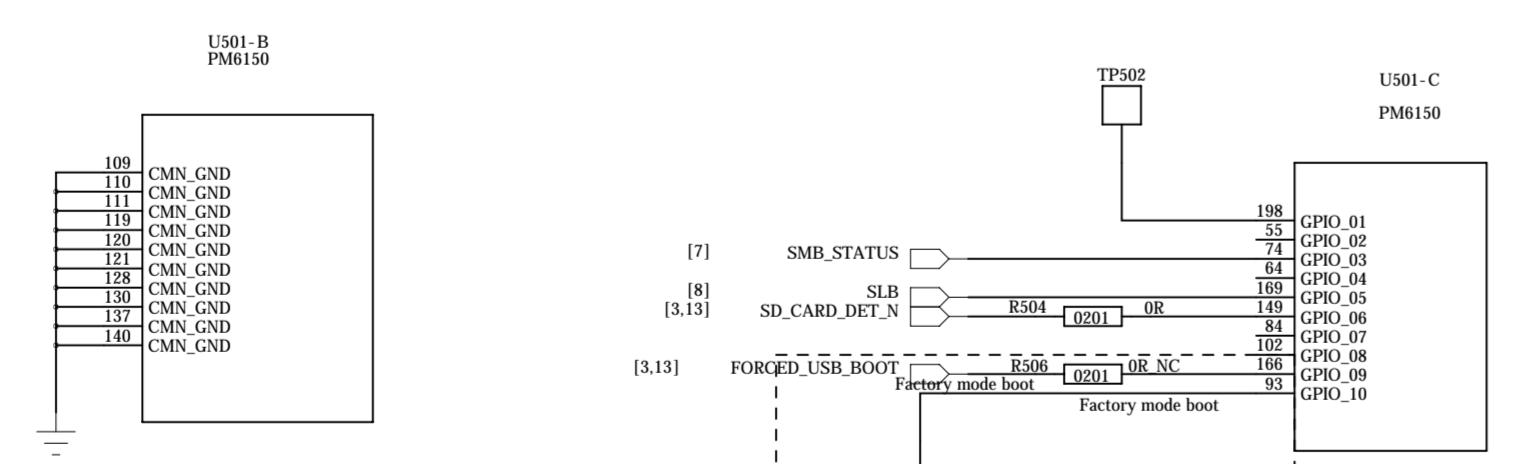
Route XTAL IN/OUT trace with length between 3mm and 10mm



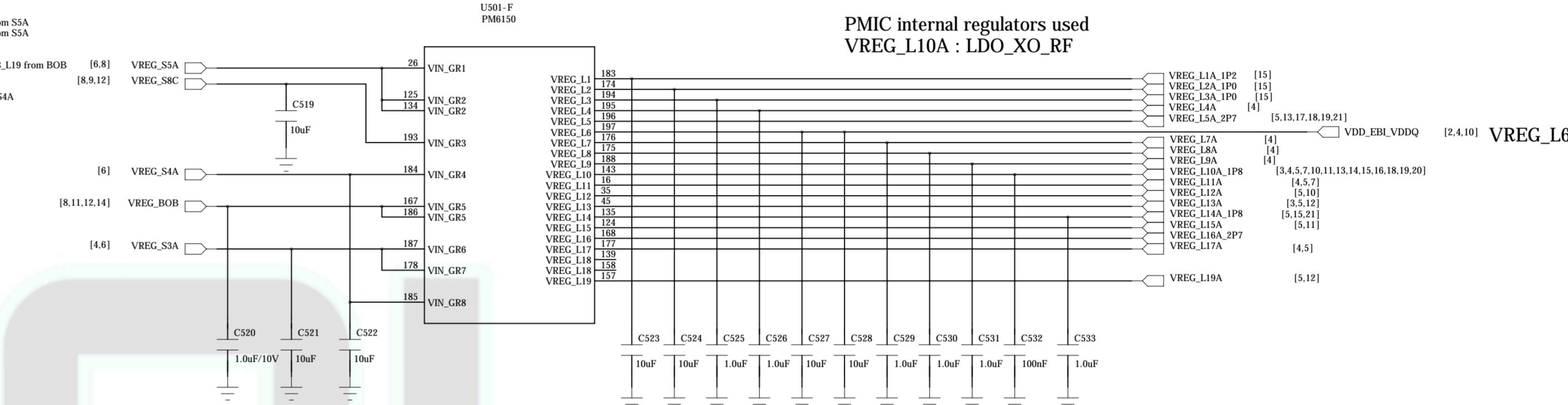
Three compatible designs are provided for SDM\_RF\_XO\_CLK.

- Three compatible designs are provided for SDM\_RI\_XO\_CLK.

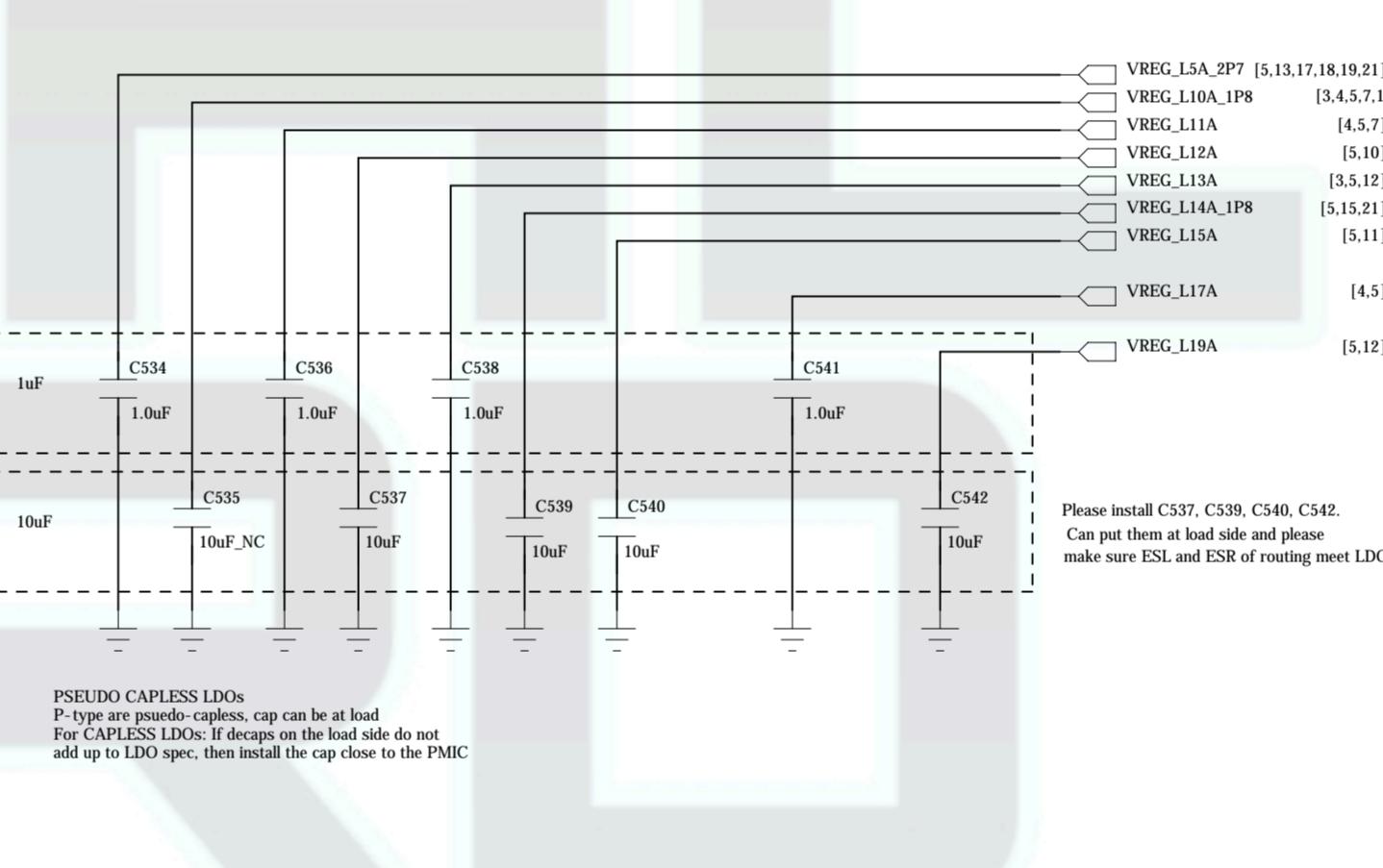
  1. WLAN\_5G\_CLK\_OUT:  
R511/C545/C546/R512/R302 are DNI
  2. Divided CLK of RFCLK2(LN\_BB\_CLK2\_DIV):  
R511/R303/C2027/C2005/C2006 are DNI and SW needs to ban WLAN\_5G\_CLK\_OUT
  3. LN\_BB\_CLK2 (Default)  
C545/R303/C2027/C2005/C2006 are DNI and SW needs to ban WLAN\_5G\_CLK\_OUT  
R511 and C546 as a divider is following IDP design.



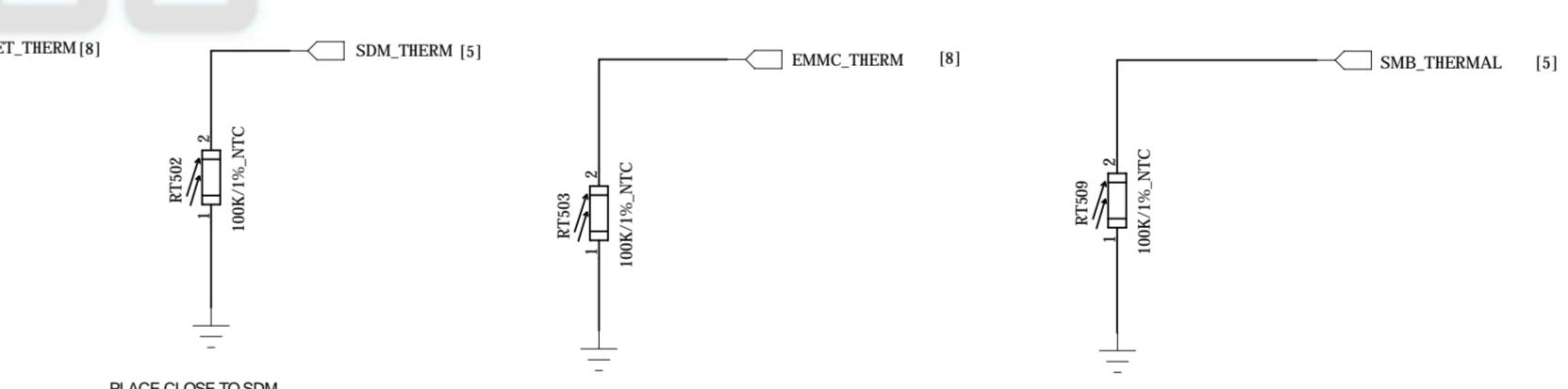
VIN\_GR1: VIN\_L11\_L12\_L13  
VIN\_GR2: VIN\_L10\_L14\_L15  
VIN\_GR3: VIN\_L1 from S8C  
VIN\_GR4: VIN\_L2\_L3 from S8C  
VIN\_GR5: VIN\_L5\_L16\_L17\_L18  
VIN\_GR6: VIN\_L6 from S3A  
VIN\_GR7: VIN\_9 from S3A  
VIN\_GR8: VIN\_L4\_L7\_L9\_L10\_L11



PMIC internal regulators used  
VREG\_L10A : LDO\_XO\_RF

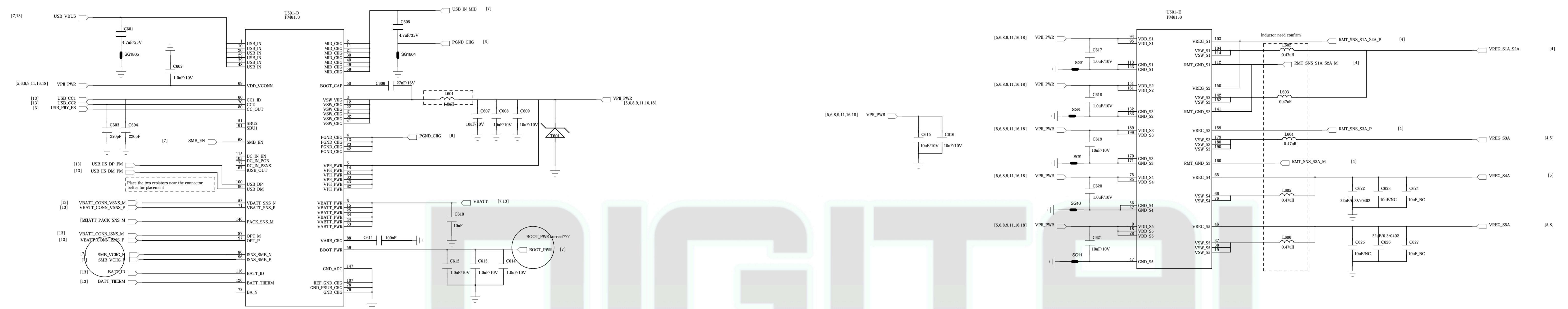


PSEUDO CAPLESS LDOs  
P-type are pseudo-capless, cap can be at load  
For CAPLESS LDOs: If decaps on the load side do not



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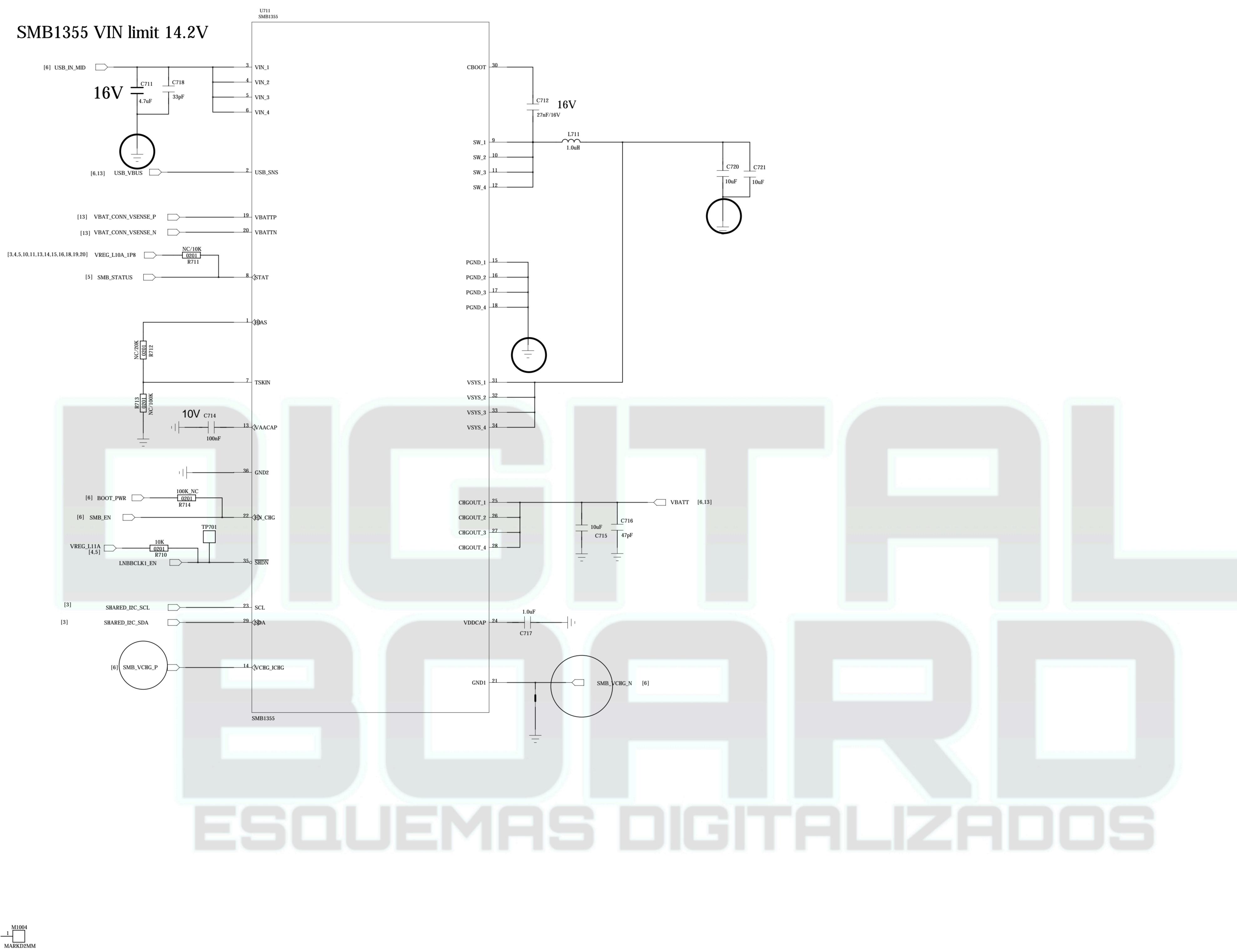
REVISION RECORD			
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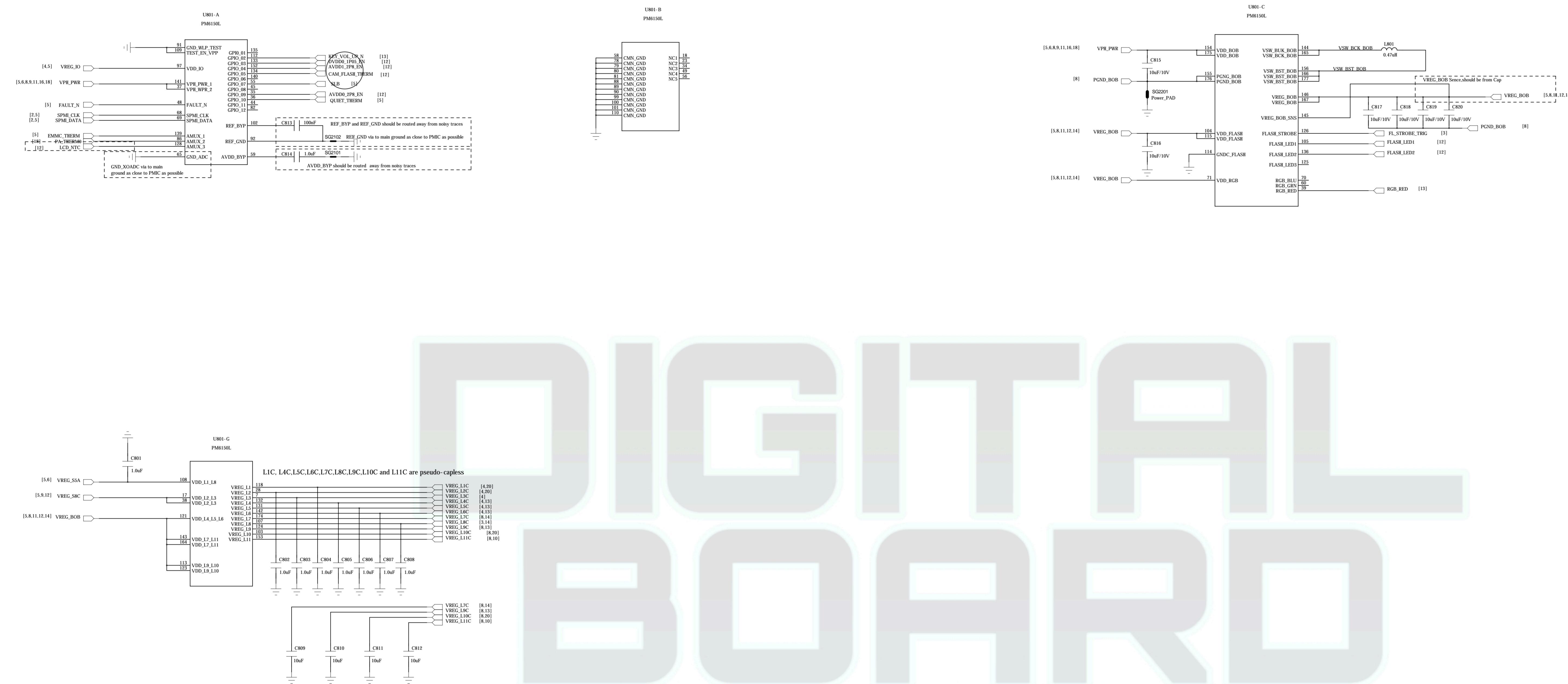
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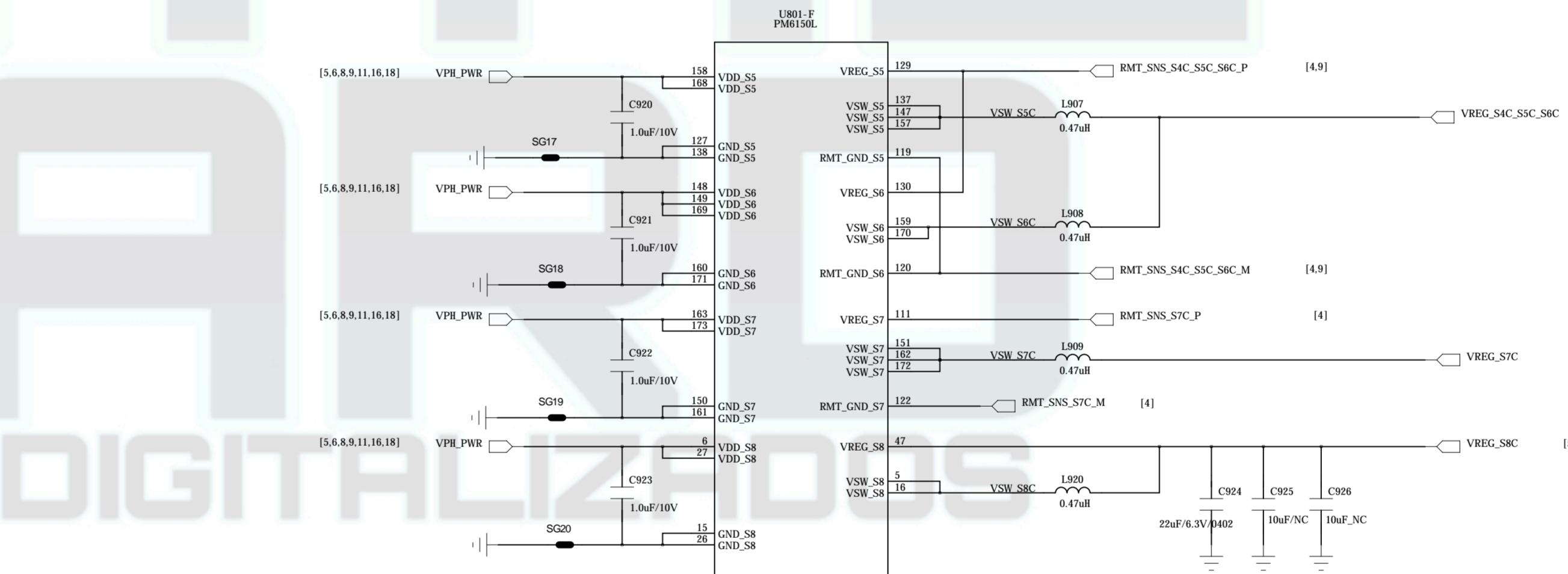
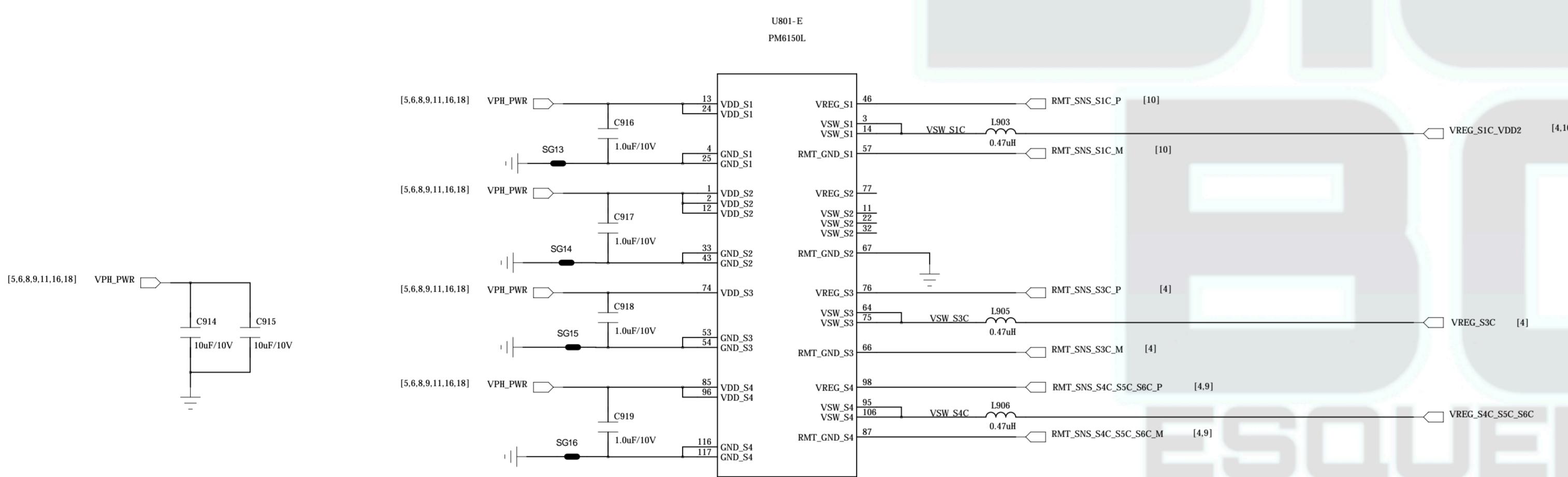
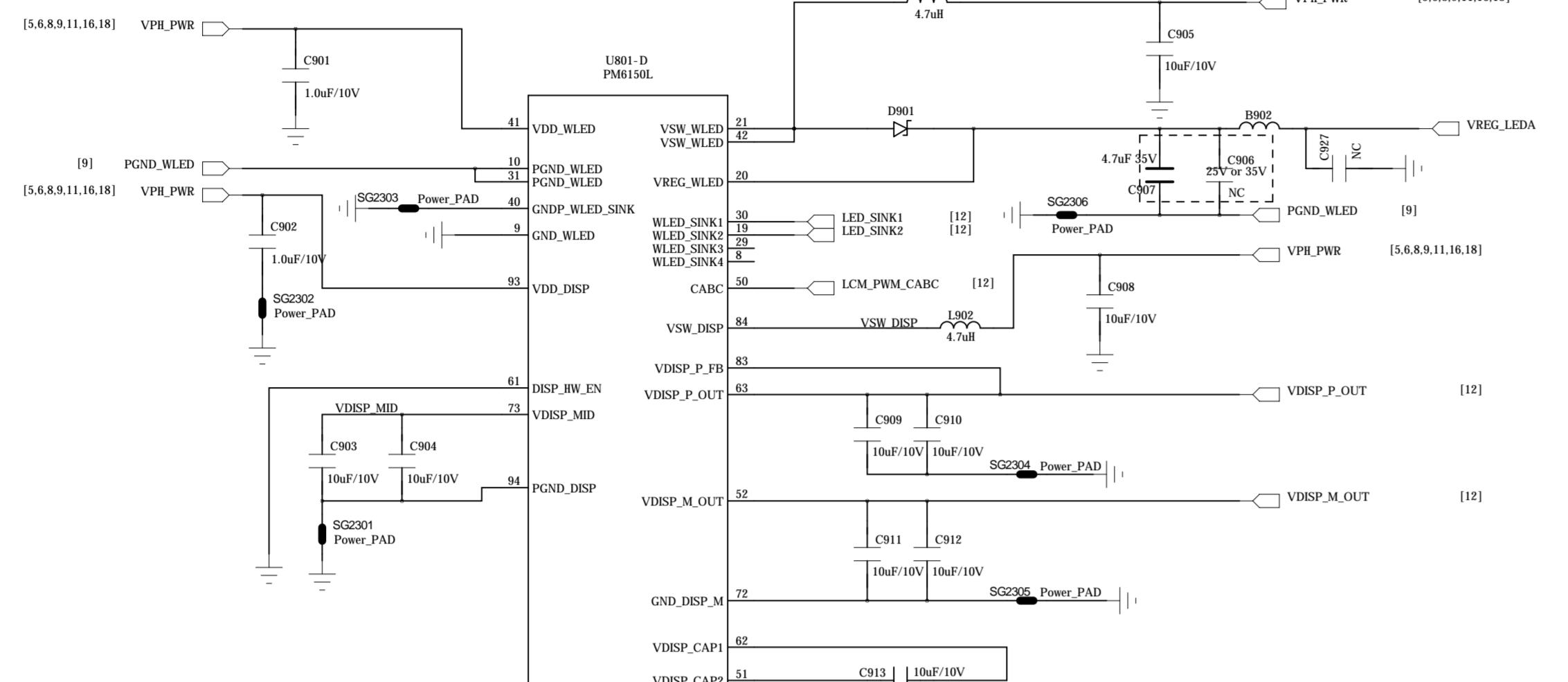
COMPANY: <Company Name>	
TITLE: <Title>	
DRAWN: <Drawn By>	DATED: <Drawn Date>
CHCKED: <Checked By>	DATED: <Checked Date>
QUALITY CON: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>
CODE: A0 <Drawing Number> × REVISION: <Code>	
SCALE: <Scale>	SIZE: <Size>
DRAWING NO: <Drawing Number>	
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COMPANY:	<Company Name>		
TITLE:	<Title>		
DRAWN:	<Drawn By>	DATED:	<Drawn Date>
CHECKED:	<Checked By>	DATED:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>
RELEASED:	<Released By>	DATED:	<Release Date>
CODE:	SIZE:	DRAWING NO.:	REV:
<Code>		A0	<Drawing Number><Revision>
SCALE:	<Scale>	SHEET:	8e 22

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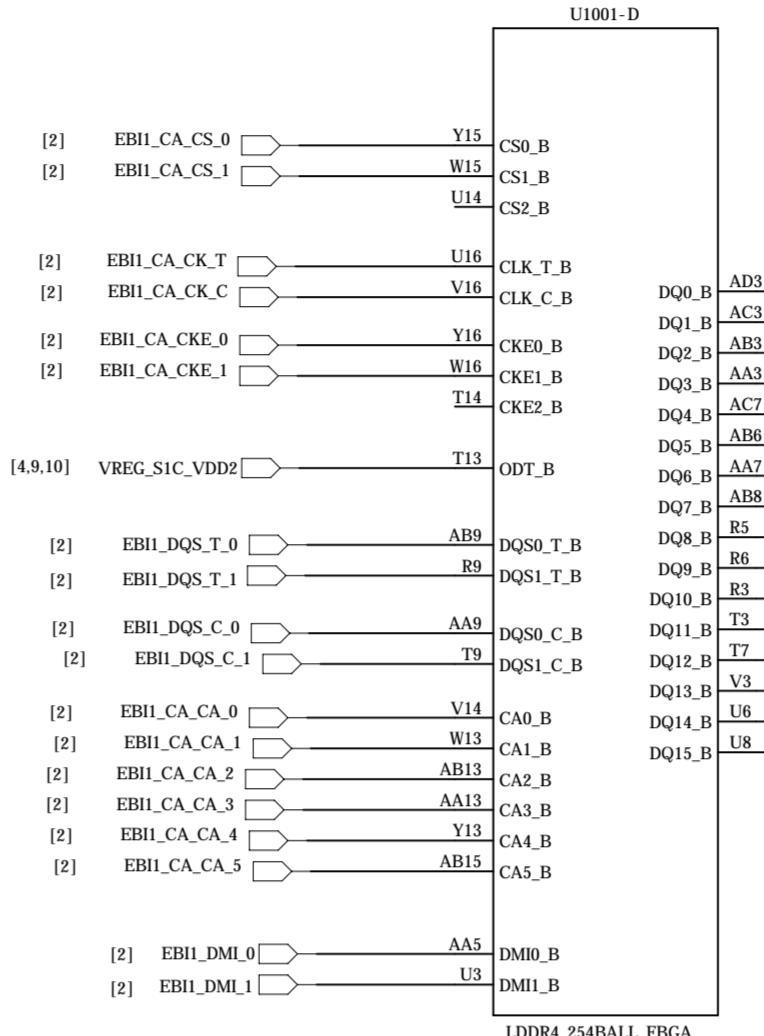
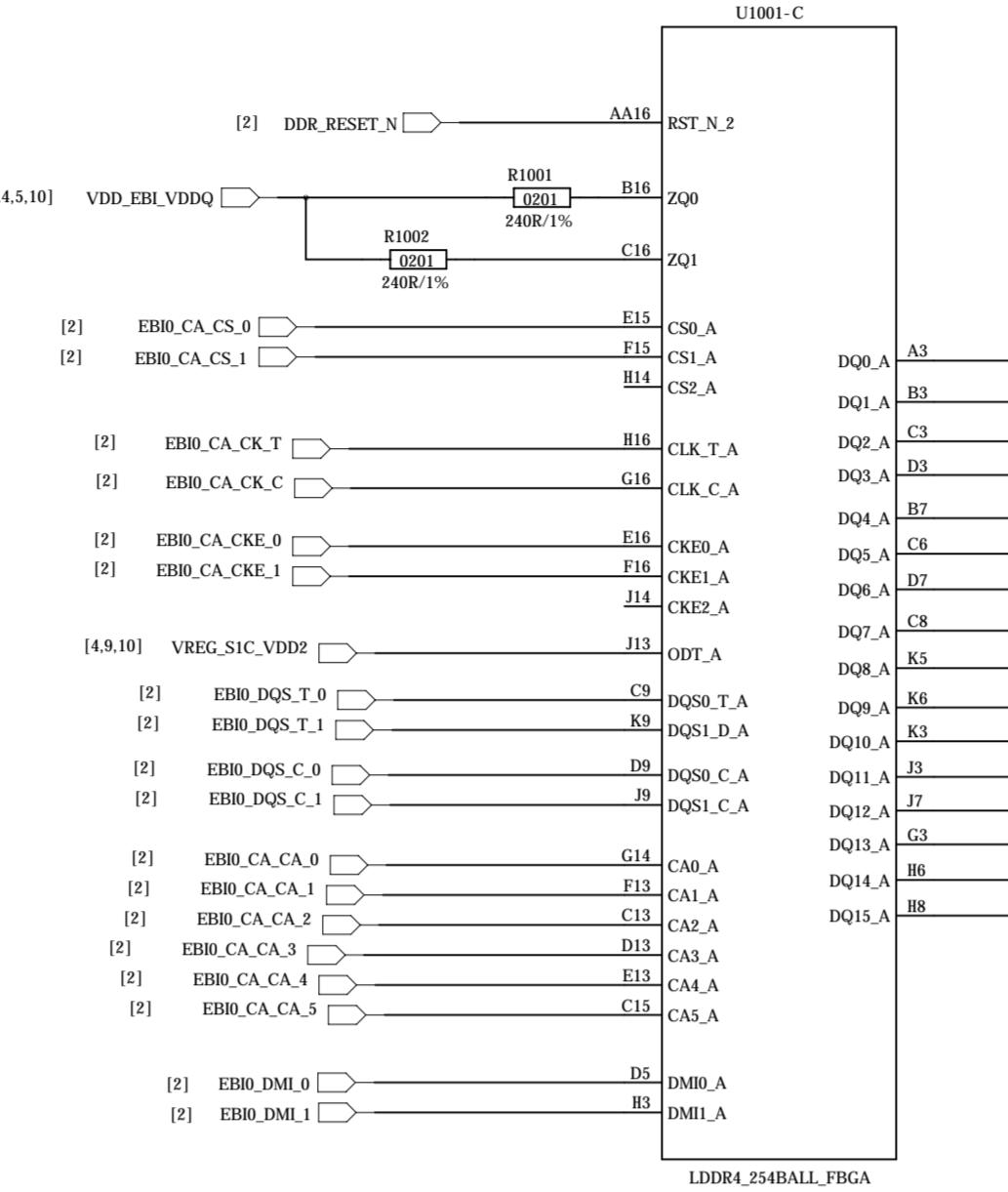
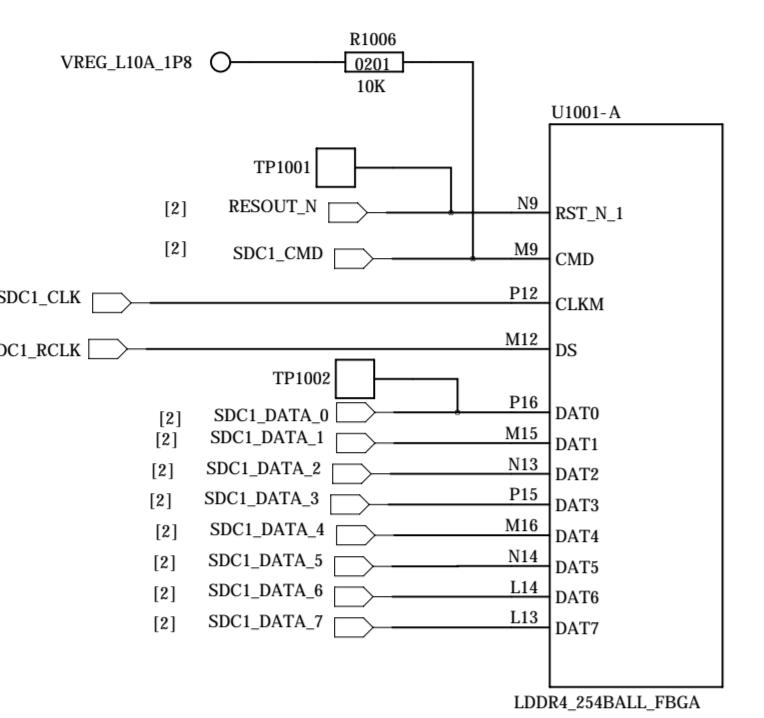
COMPANY:	<Company Name>		
TITLE:	<Title>		
DRAWN:	<Drawn By>	DATED:	<Drawn Date>
CHECKED:	<Checked By>	DATED:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>
RELEASED:	<Released By>	DATED:	<Release Date>
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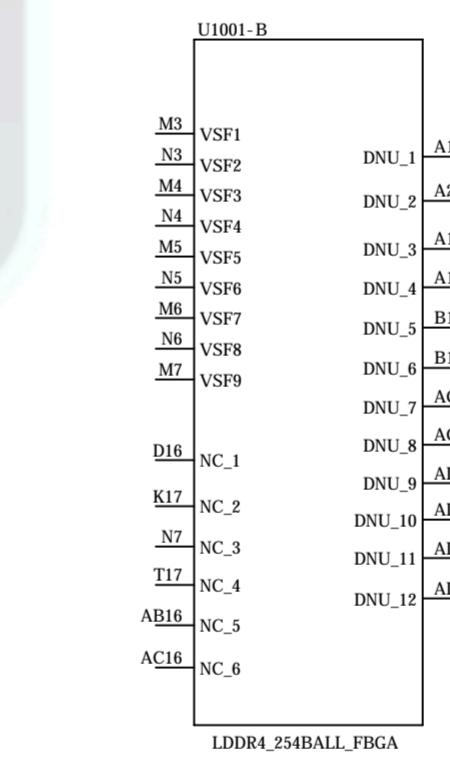
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CMD/DATA0/RST need TEST POINT



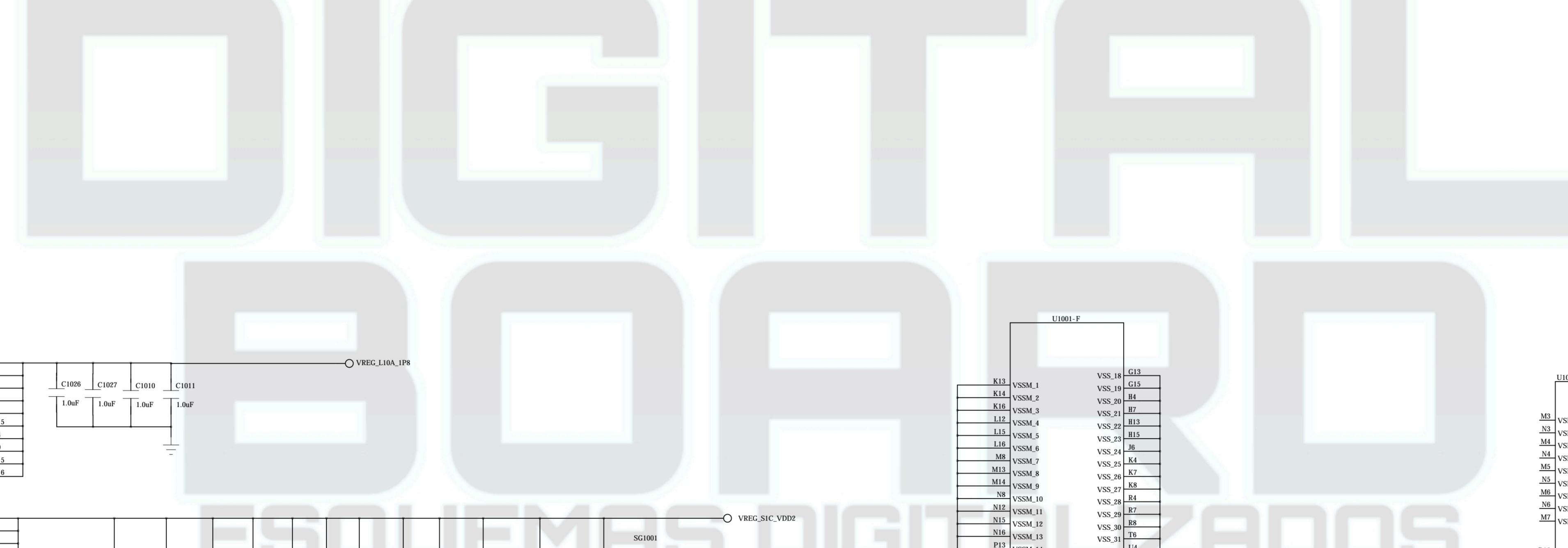
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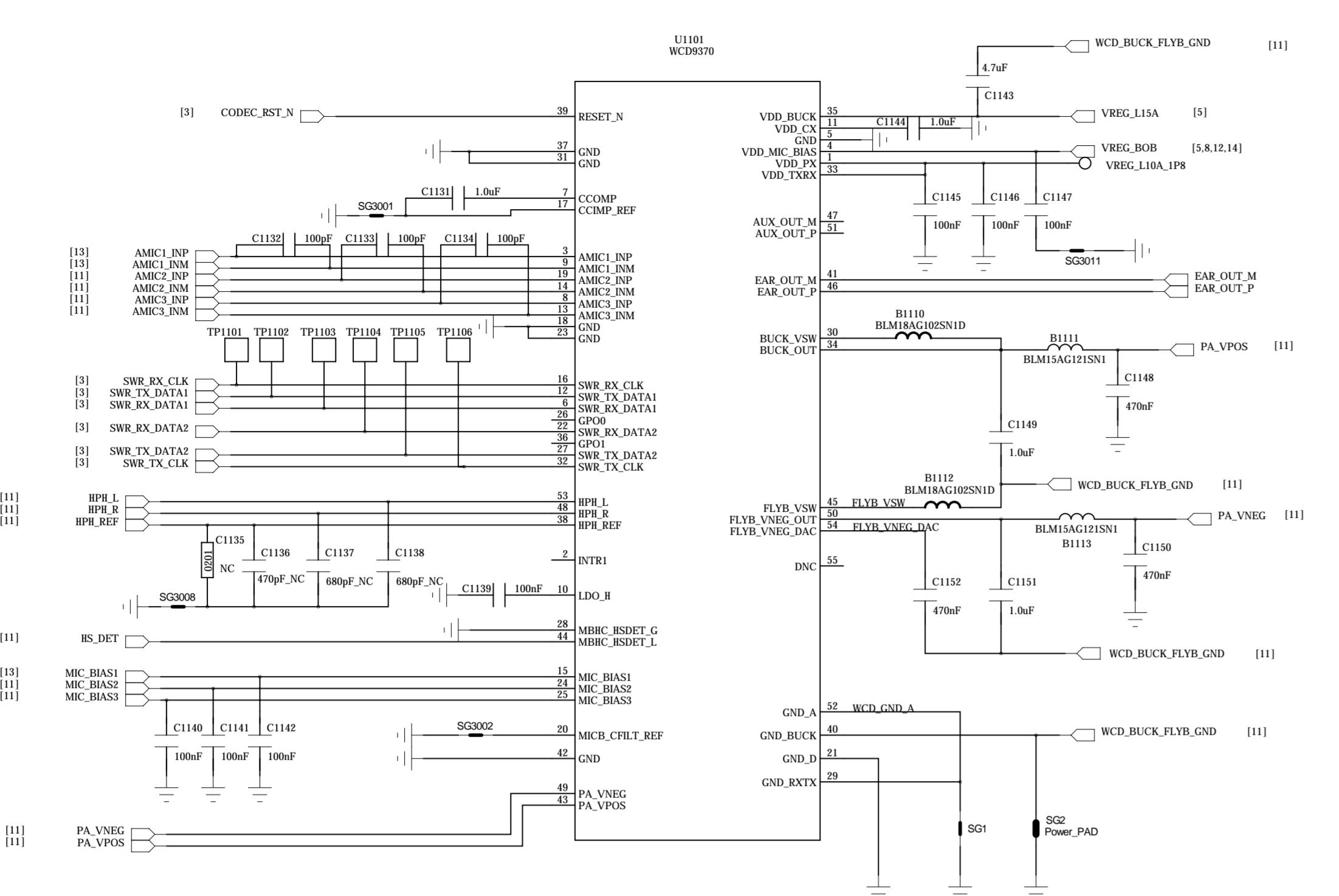


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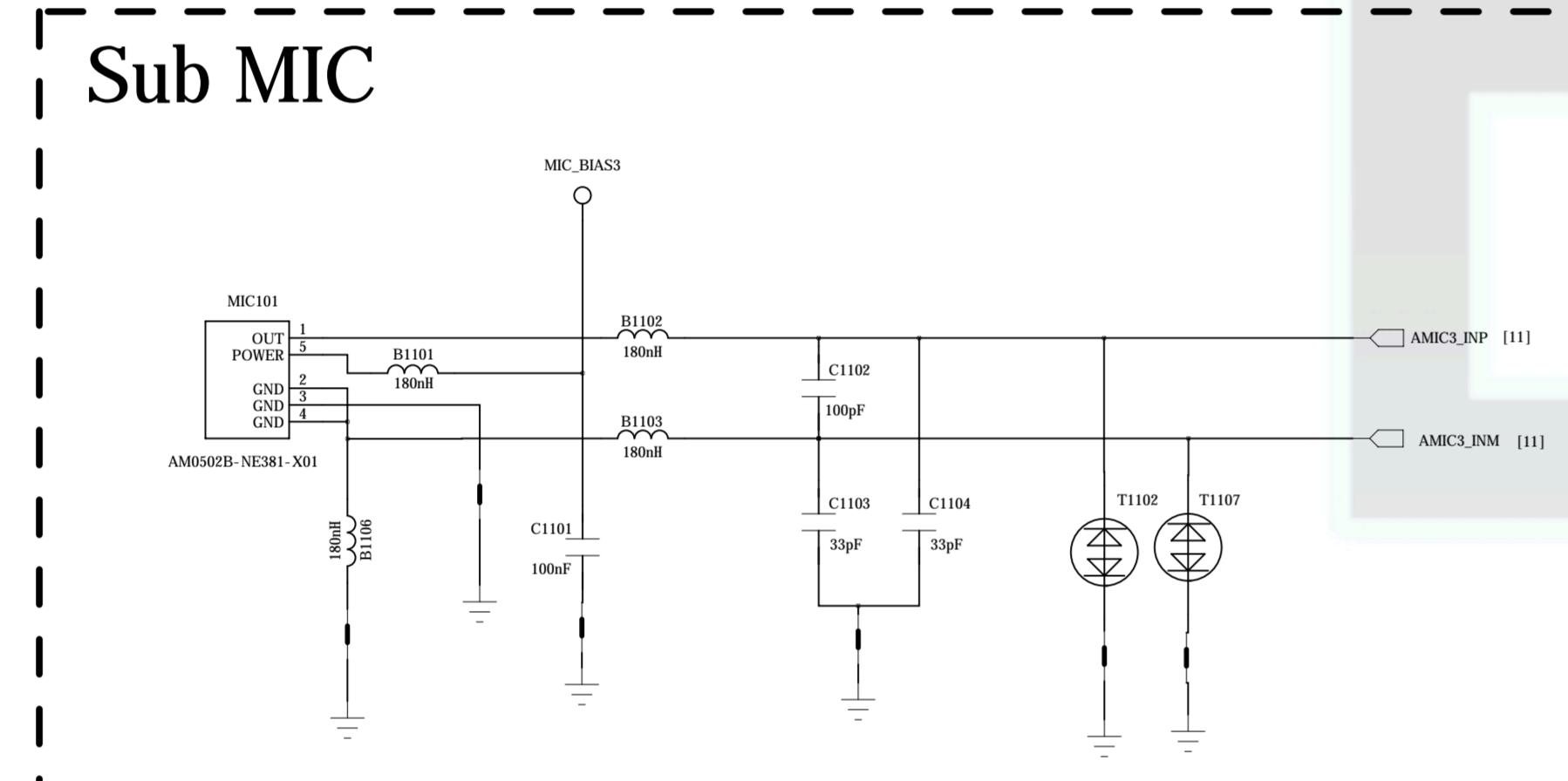
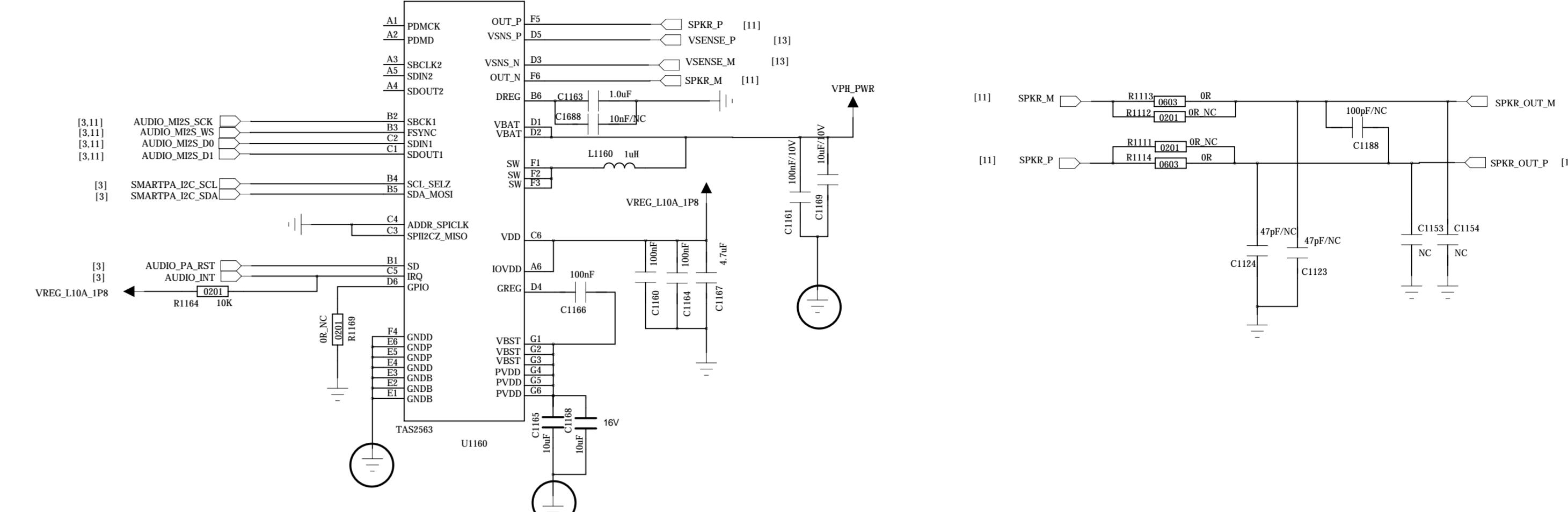
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TITLE:	<Title>		
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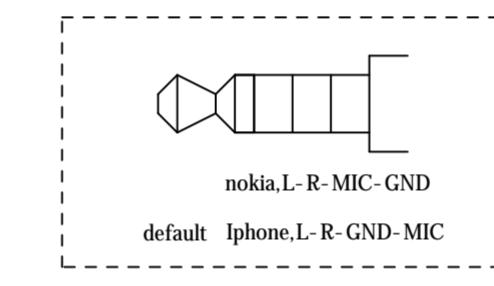
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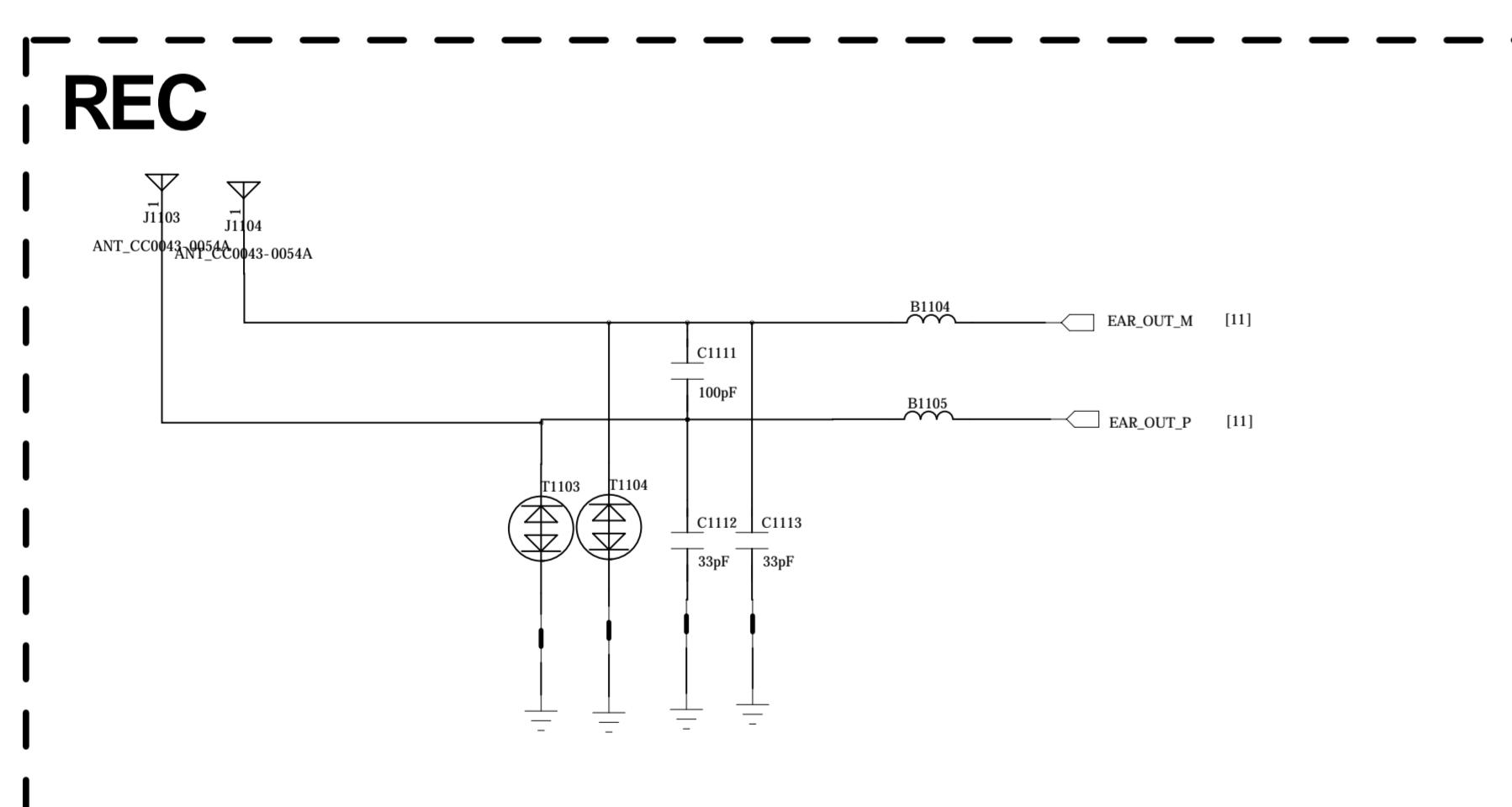
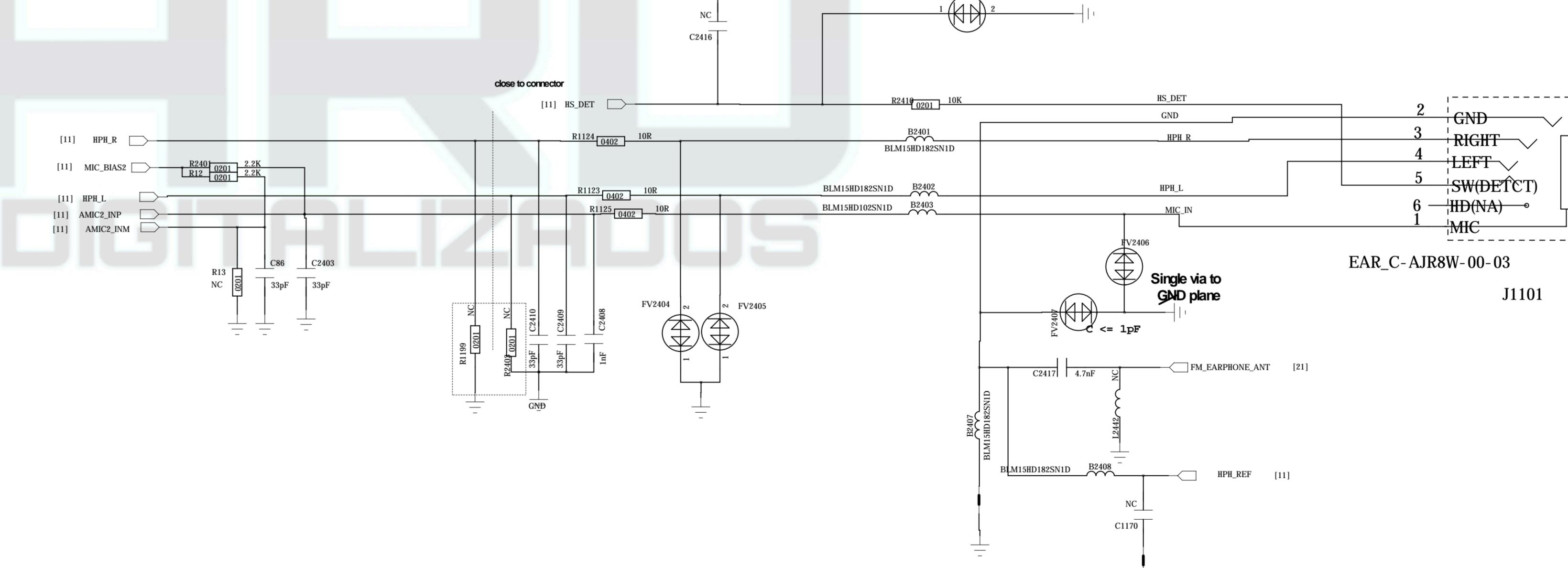
# Smart PA



# Earphone Audio

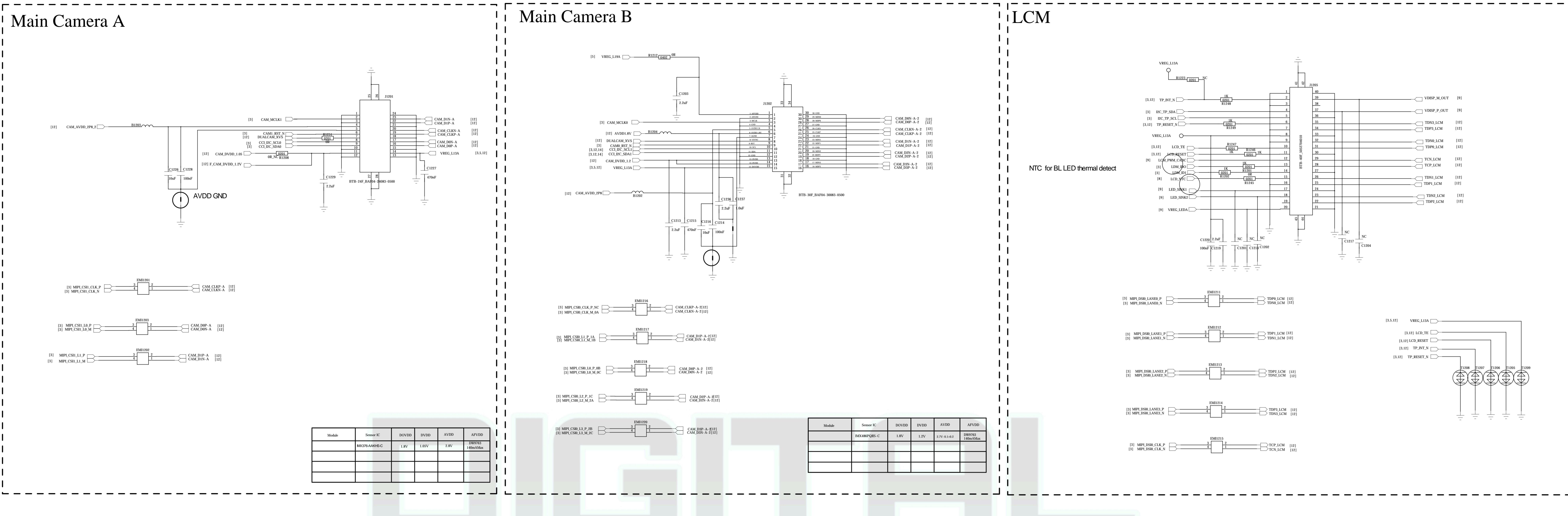


Note: Ferrite beads and their corresponding bypass capacitors are needed to reduce noise generated by audio/FM concurrency on CDC\_HPH\_L\_P, CDC\_HPH\_L\_M and CDC\_HPH\_REF

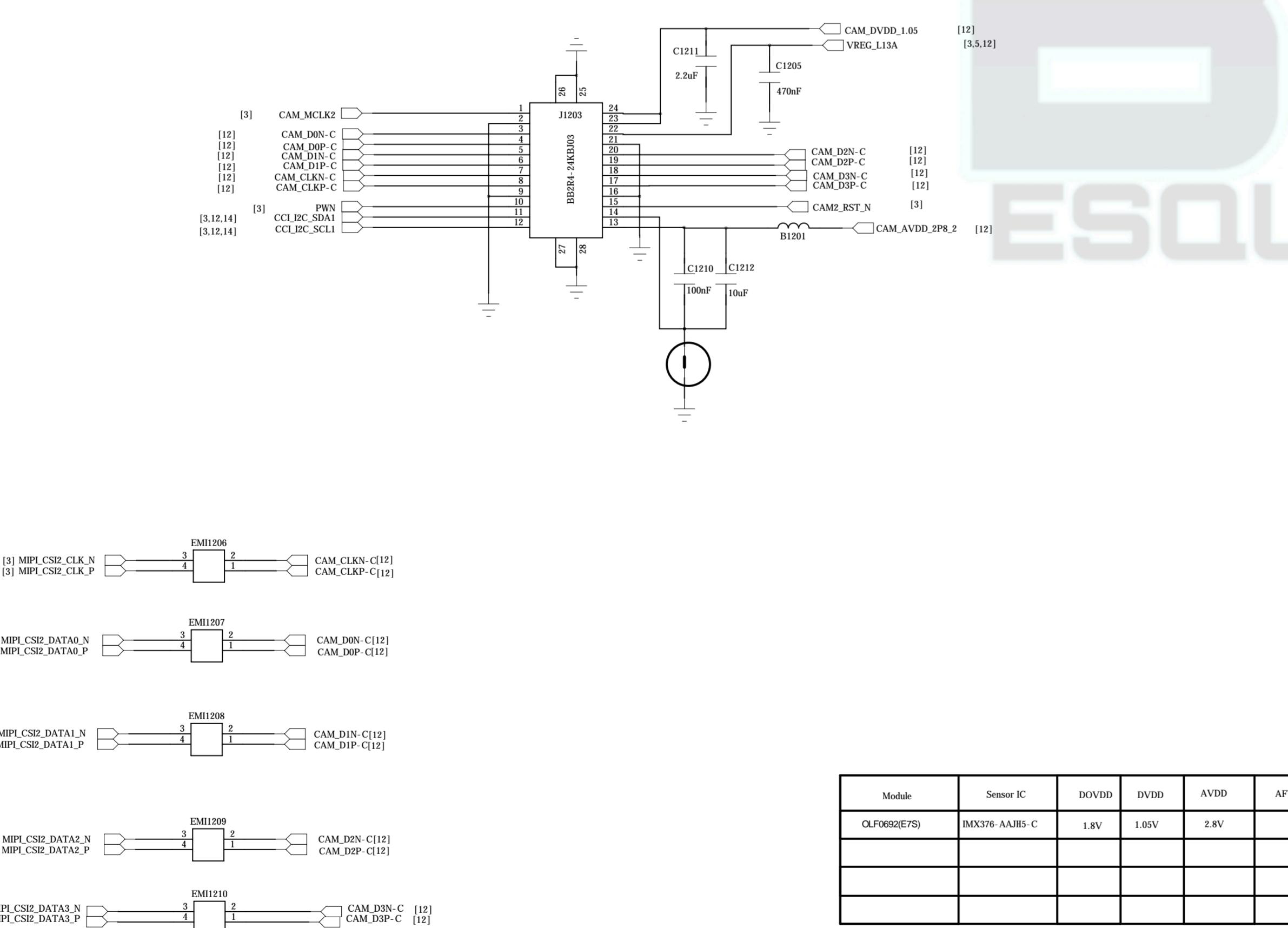


Note: Place B202,B203,C216,C217 close to headset jack connector  
Note: For Cable detection

COMPANY:	<Company Name>		
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# Front Camera



Schematic design notice of "63\_PERI\_CAMERA\_KEYPAD" page.

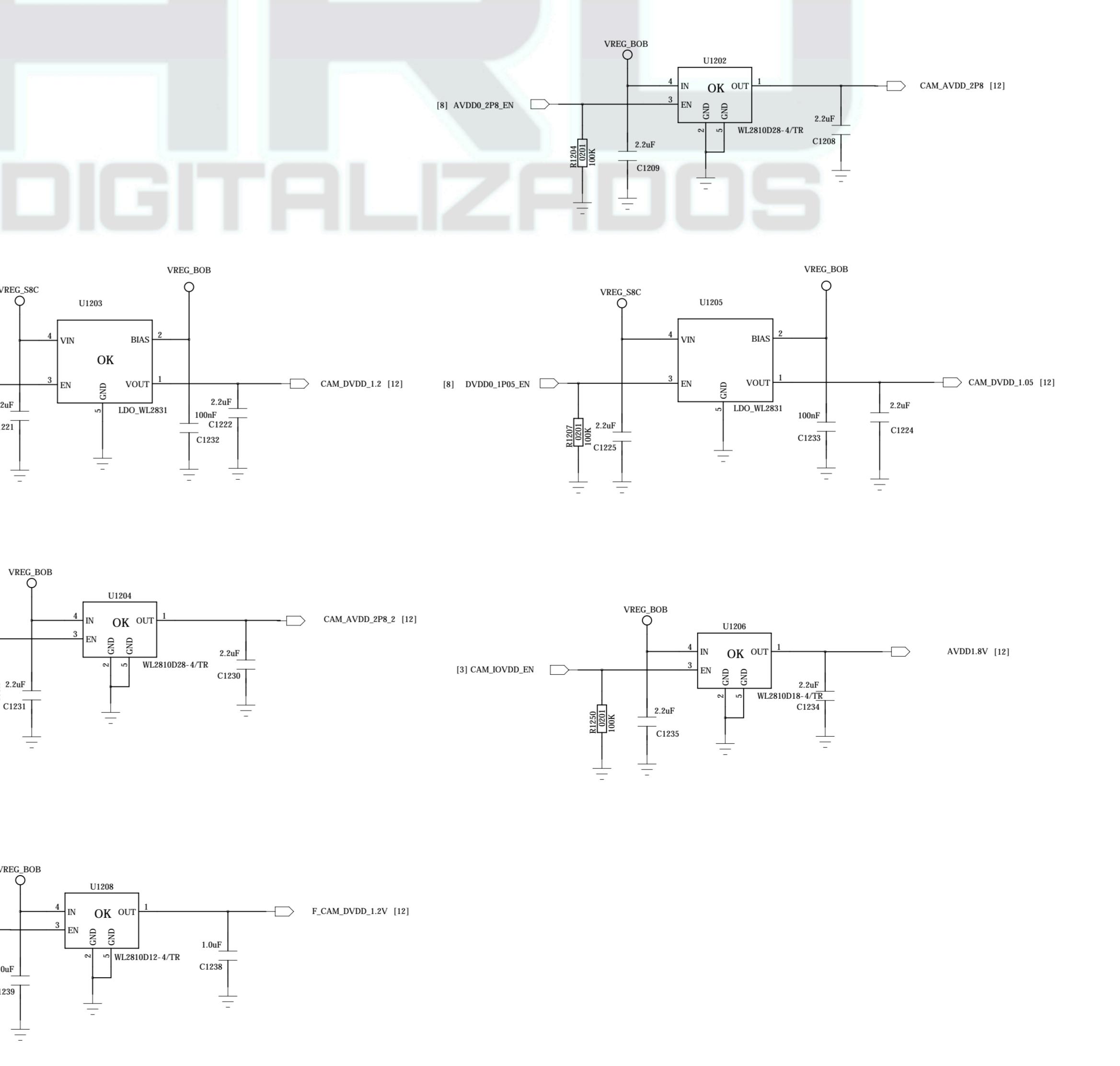
Note 62-1: The VCC of I2C\_0 is pulled to "VCAM\_IO\_PMU

Note 62-2: I2C control interface of front camera (with AF) must be assigned to I2C-2 bus when PIP/VIV feature be supported.

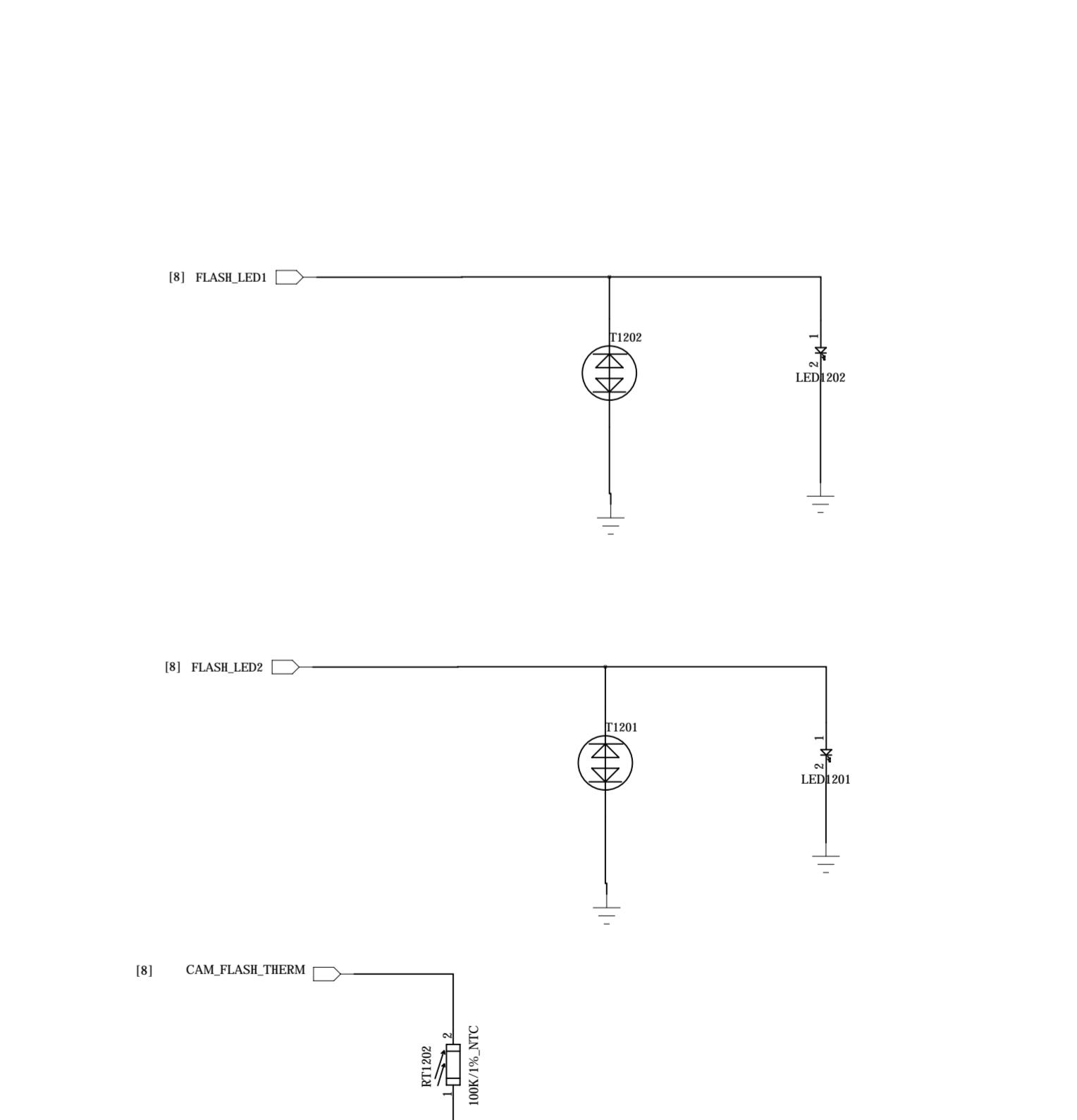
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Note 62-3: Reserve a capacitor (27pF) on camera's MCLK and shunt it to GND to prevent CPS de-sense

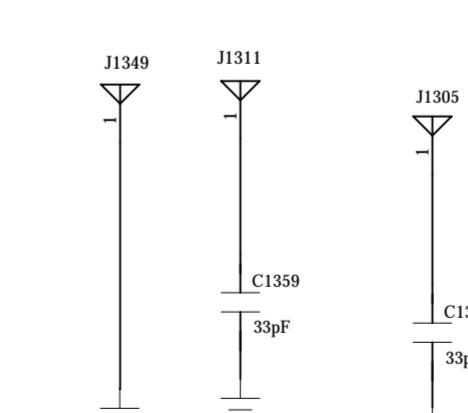
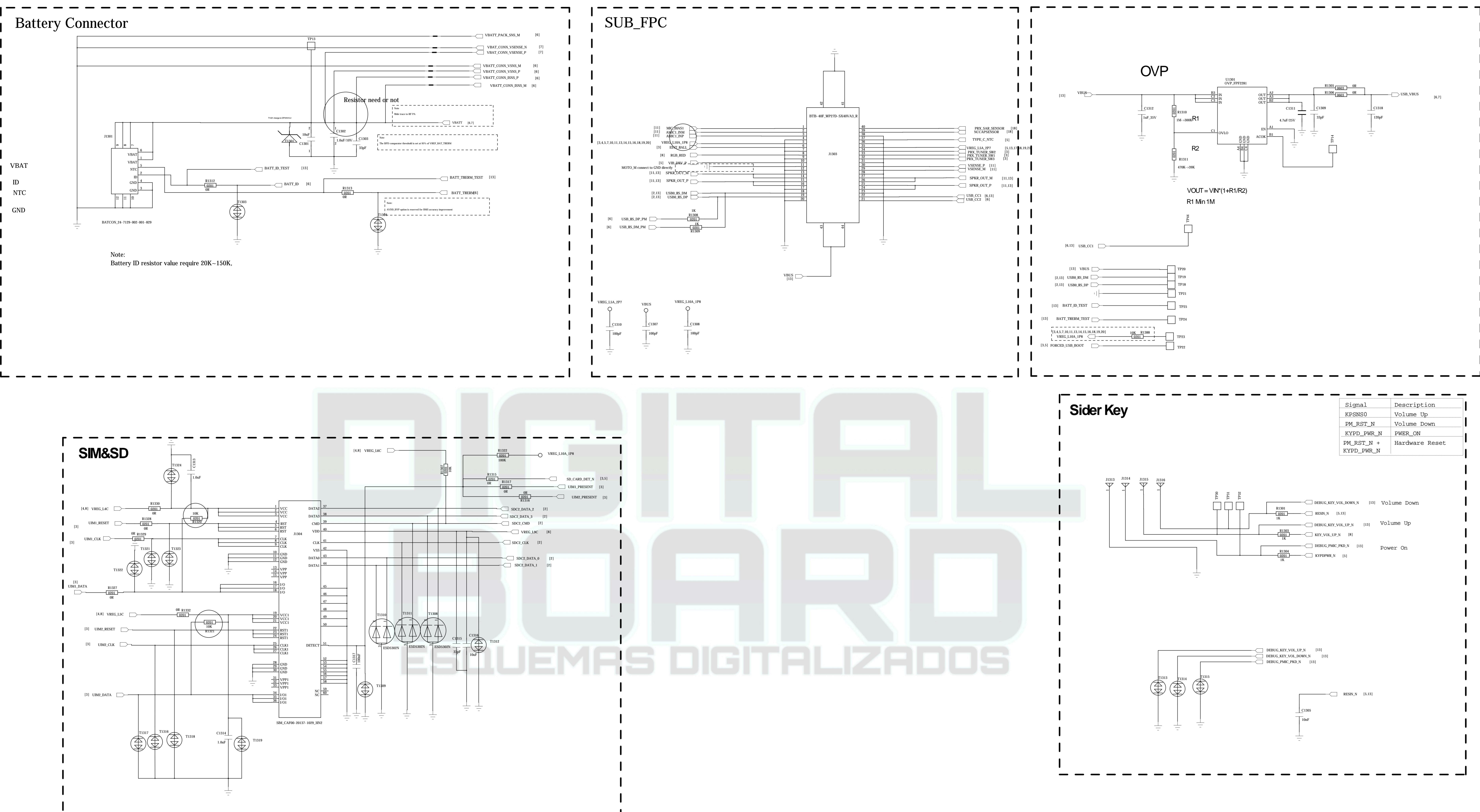
# Camera Power



# Flash Light

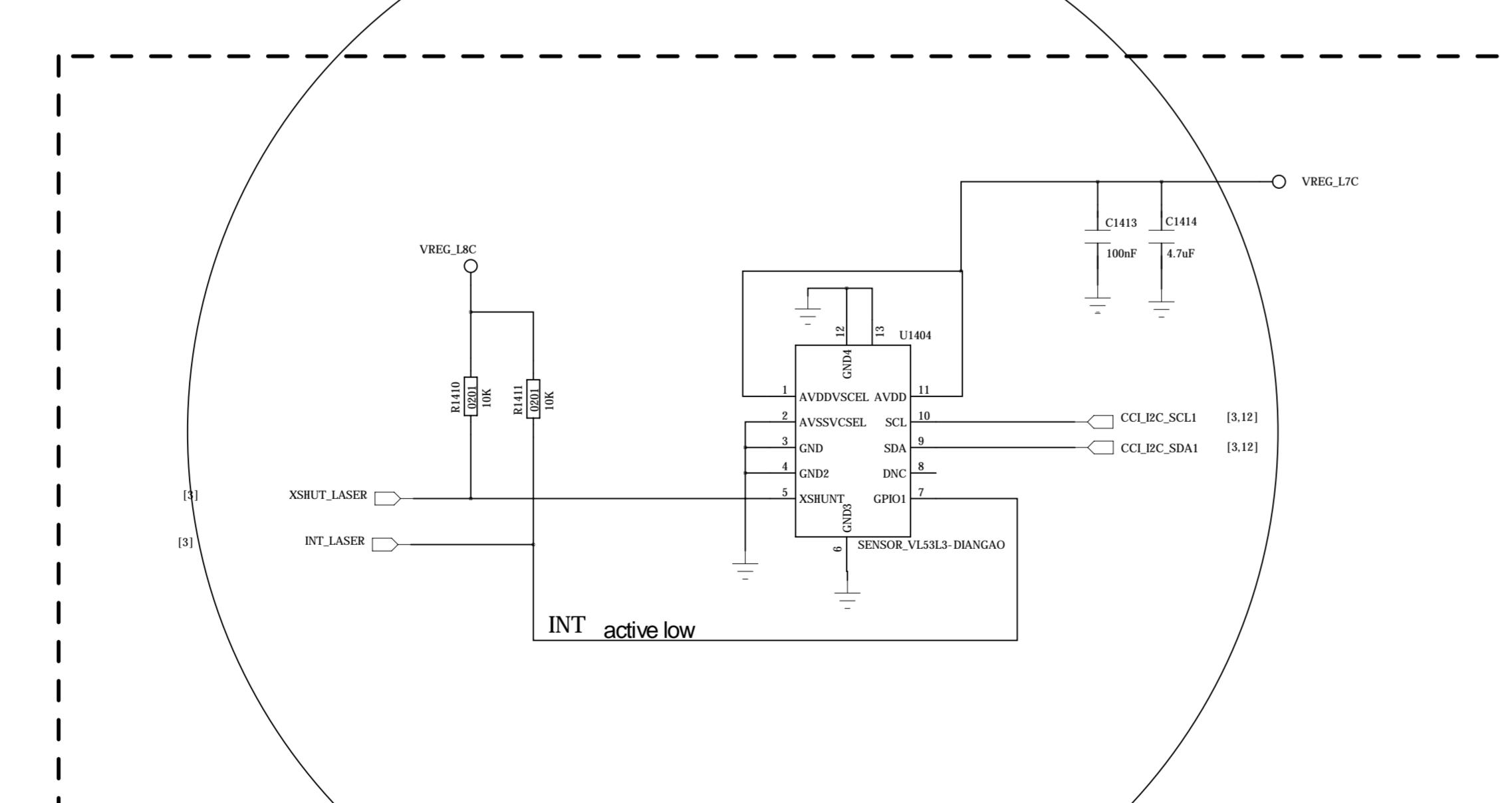
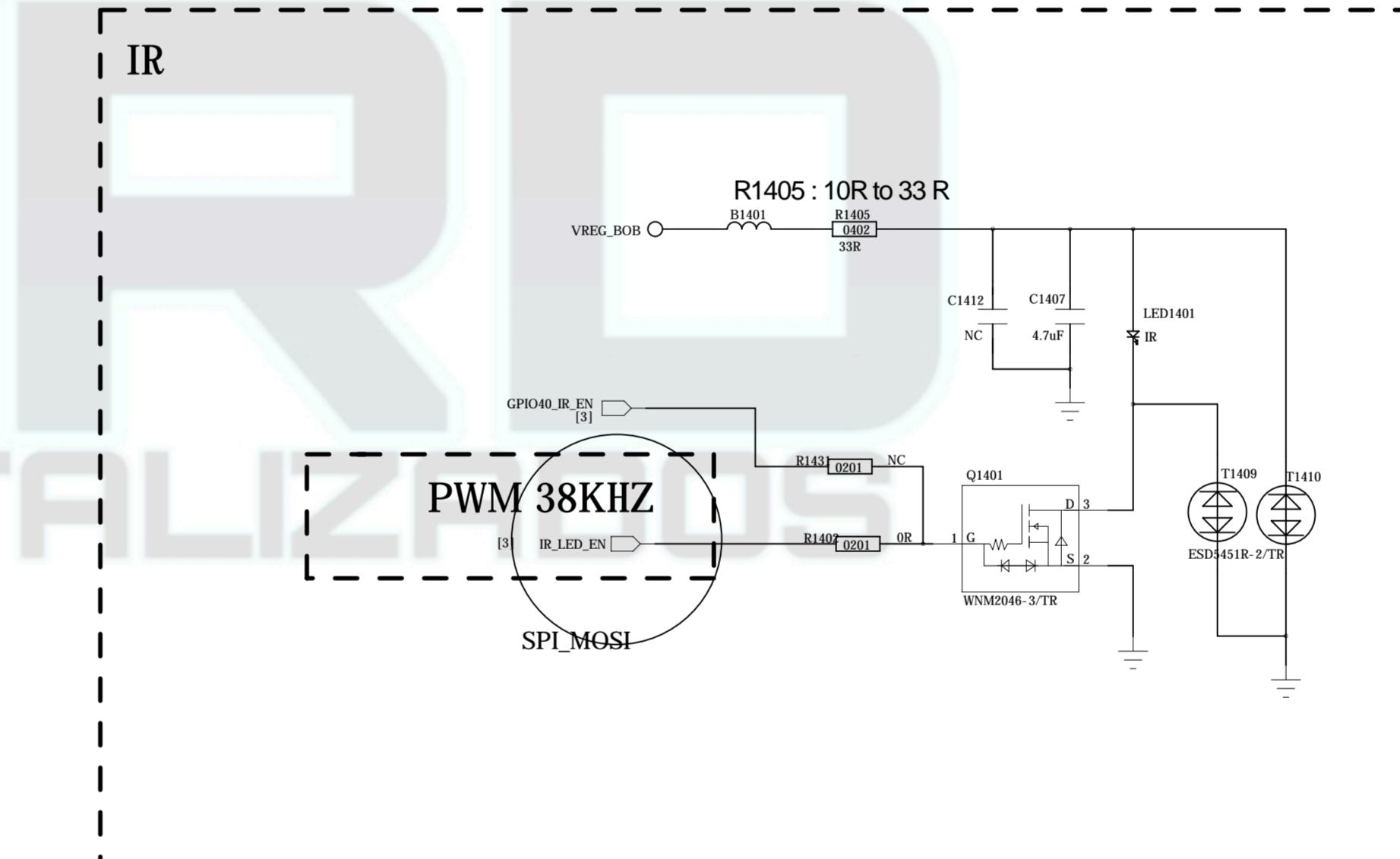
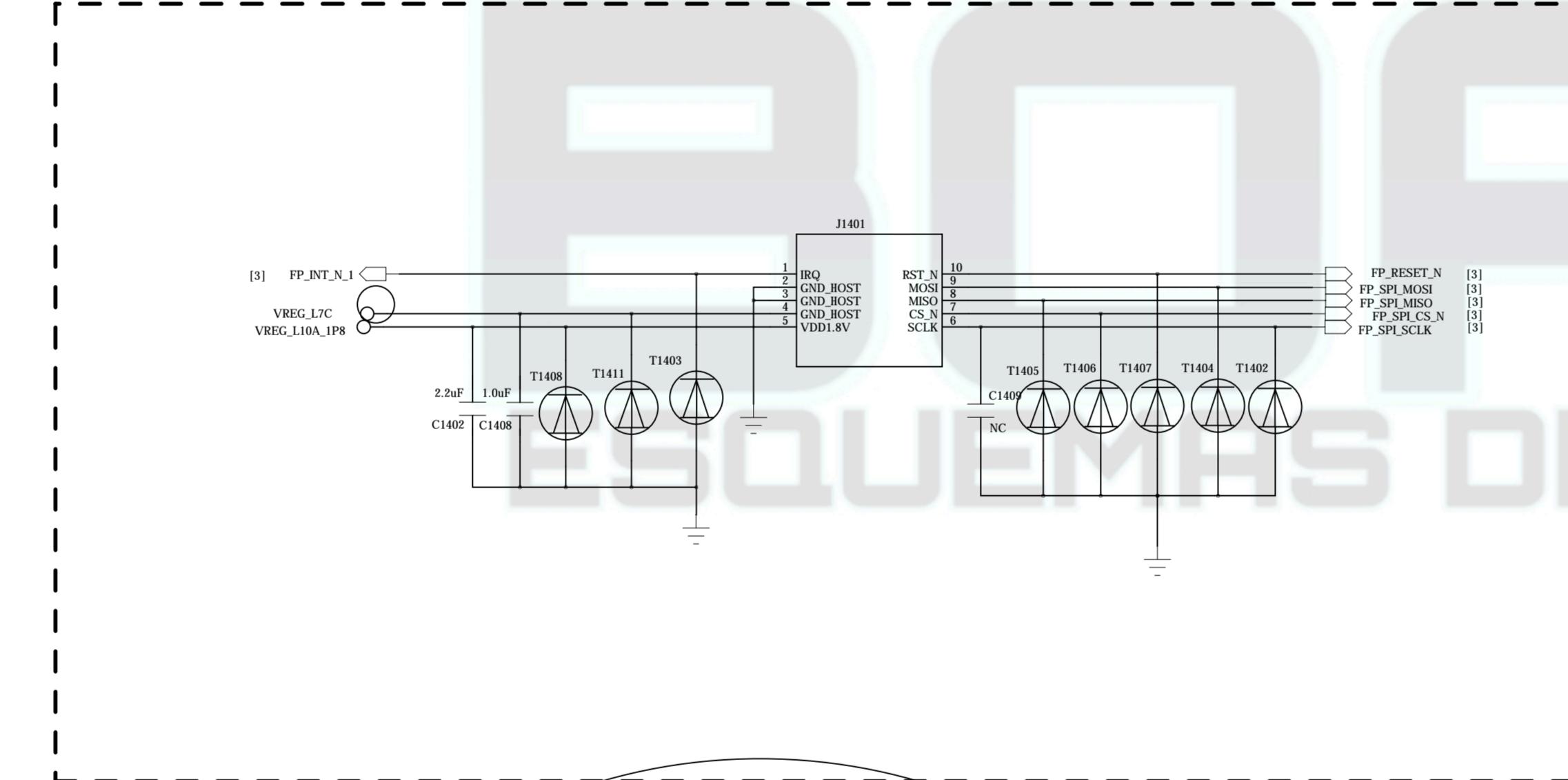
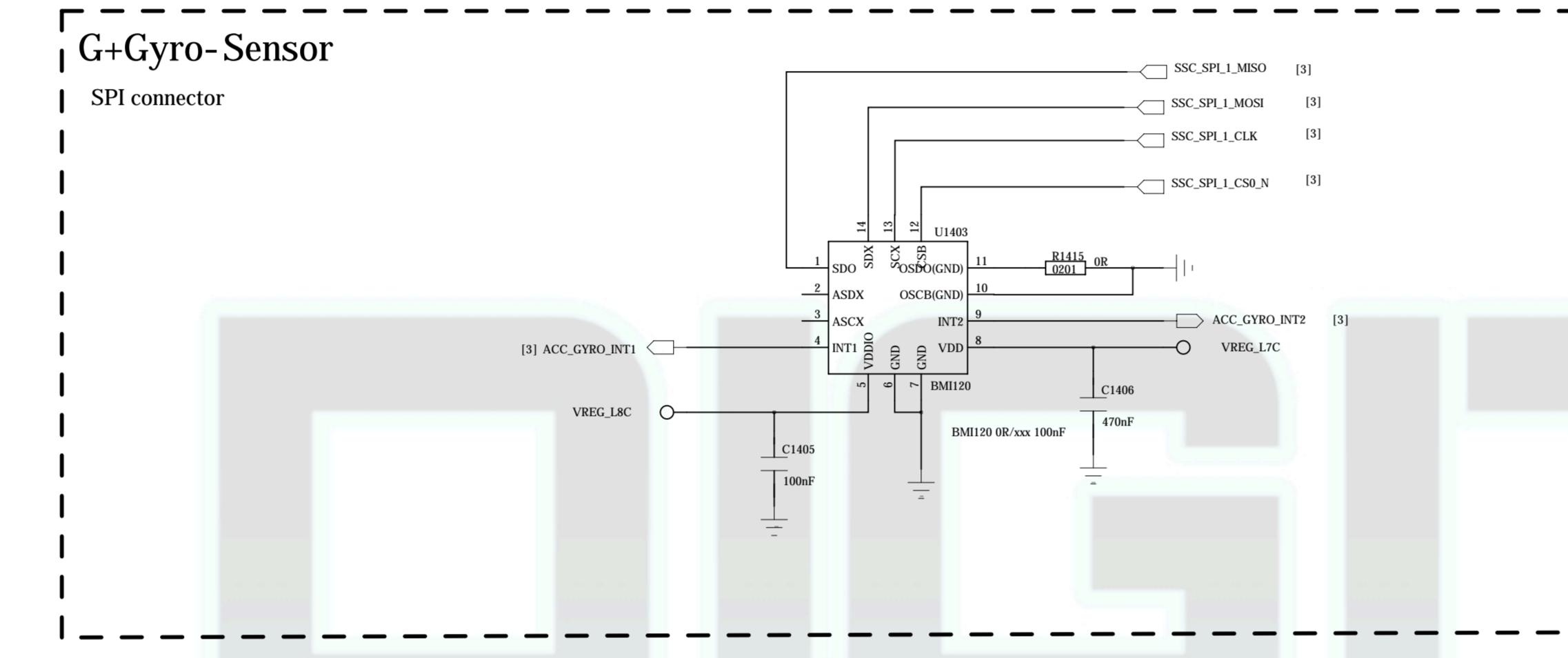
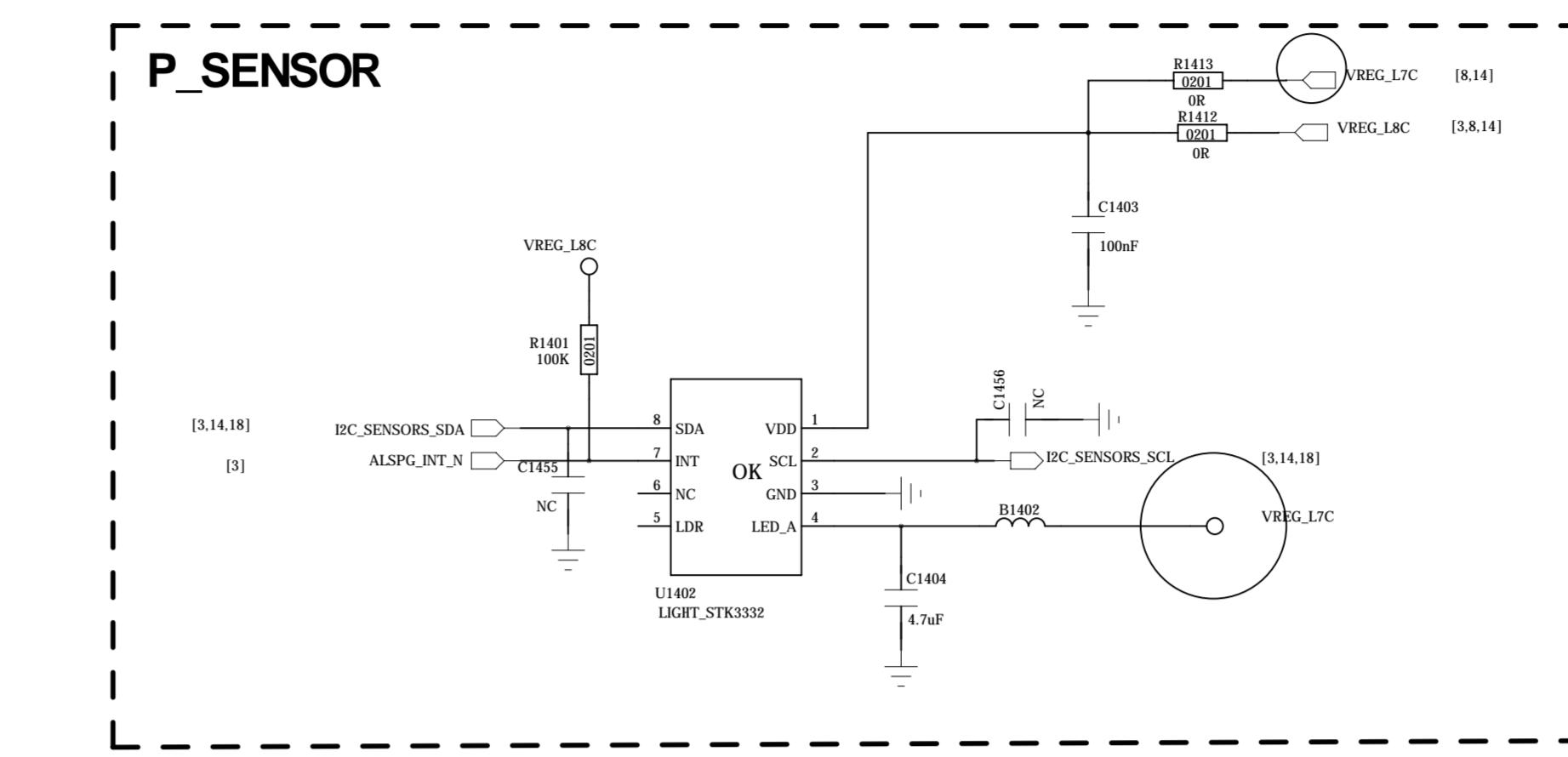
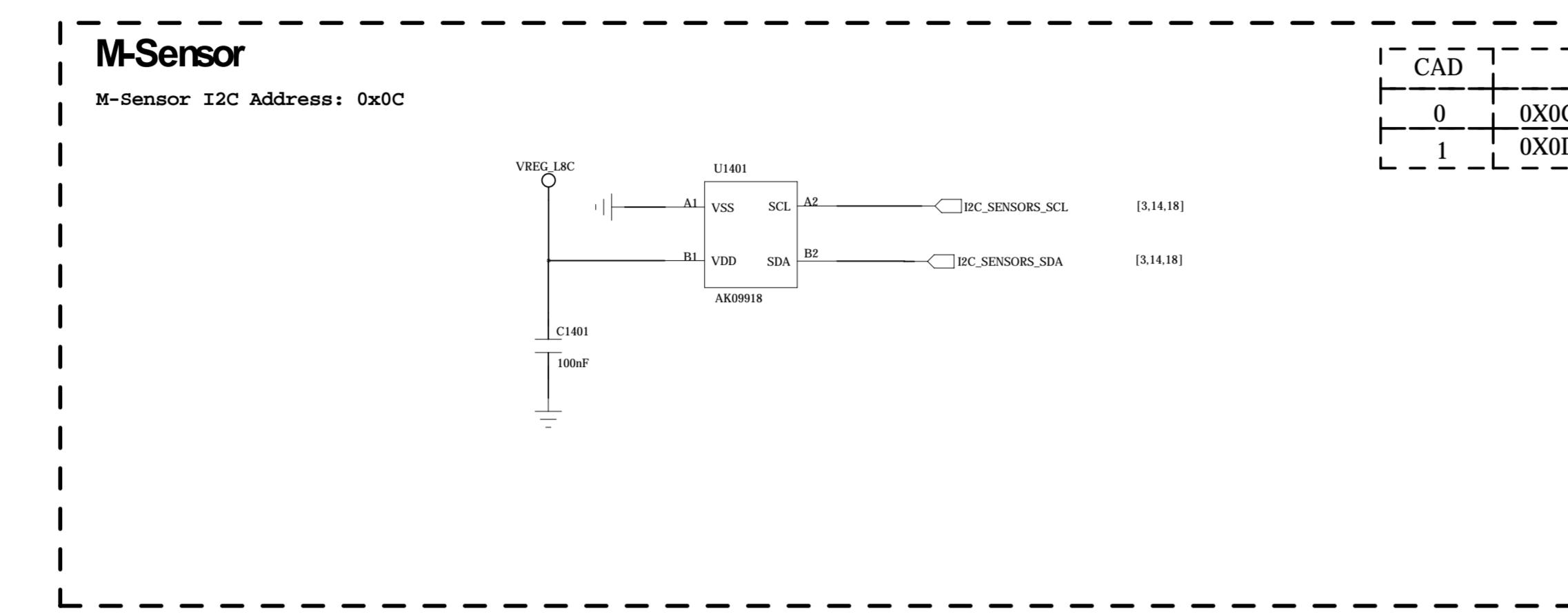


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REVISION RECORD			
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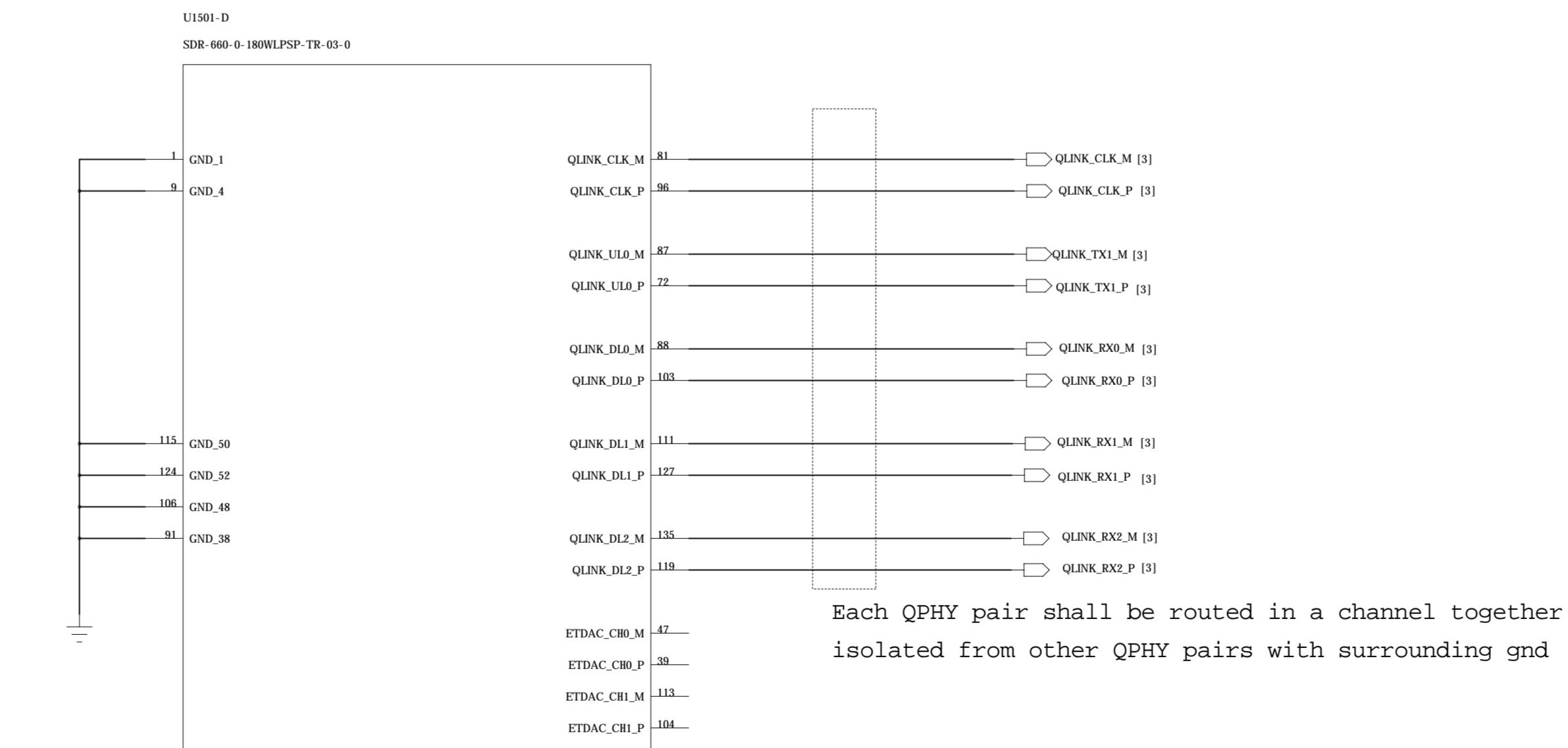
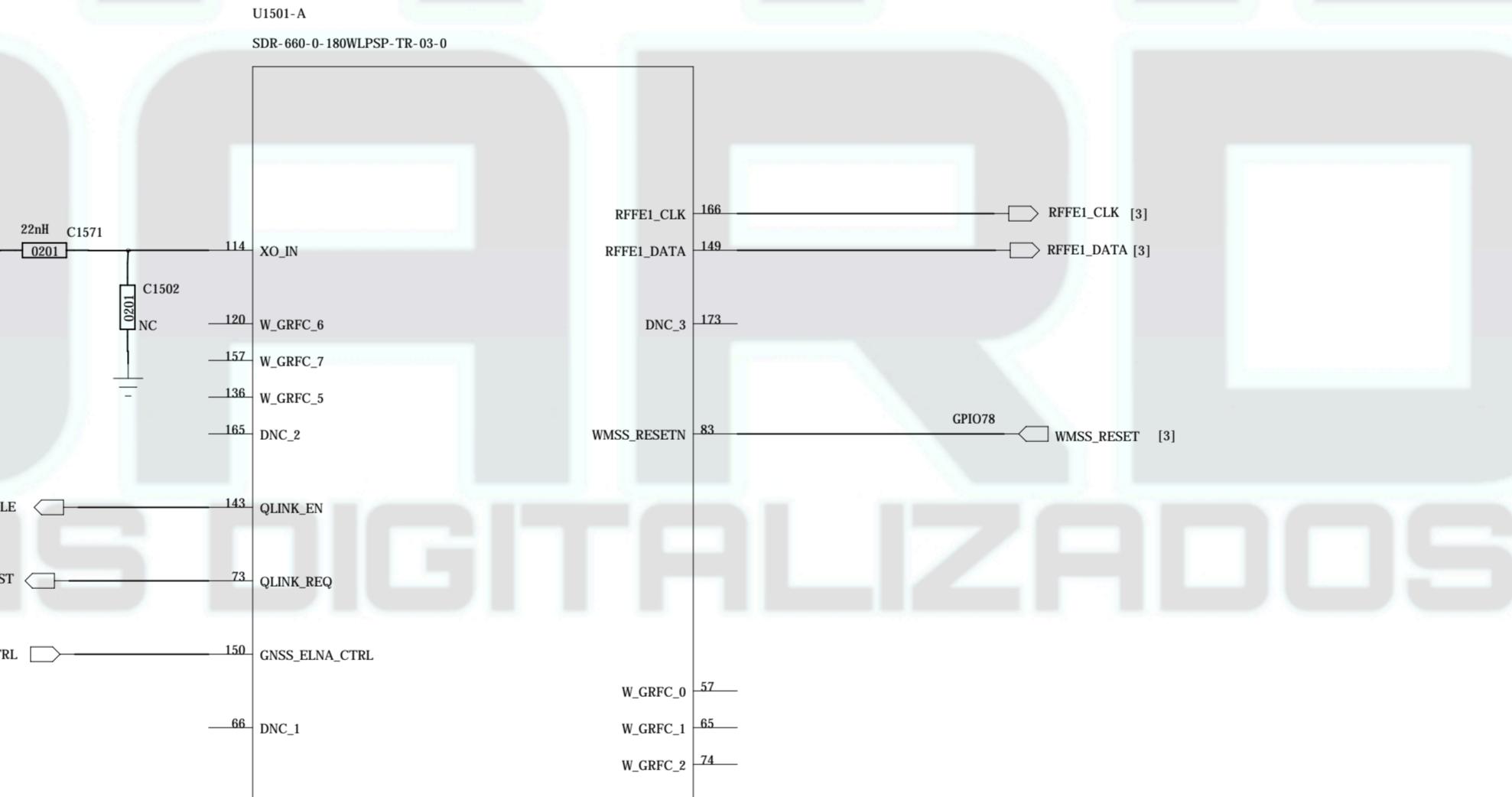
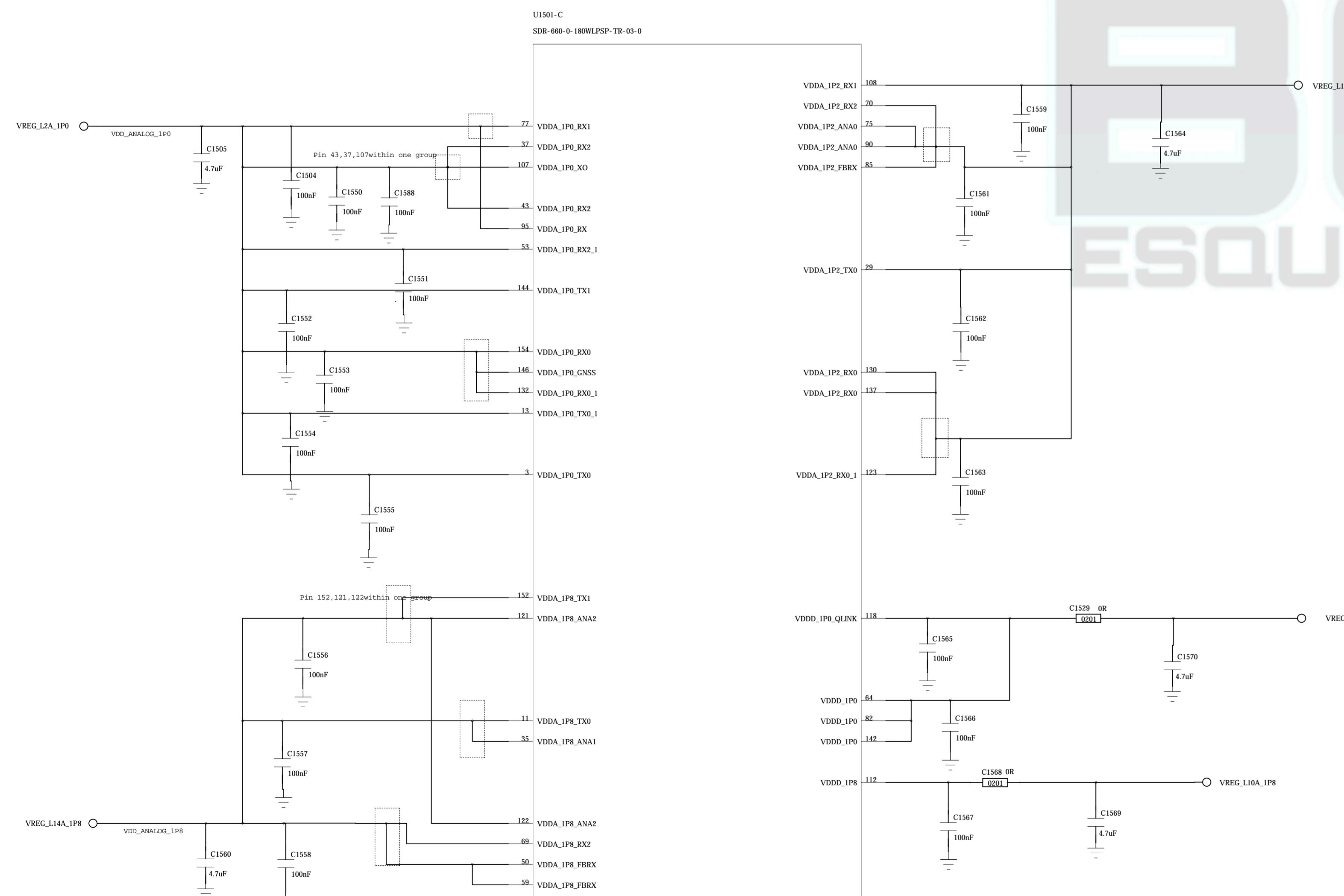
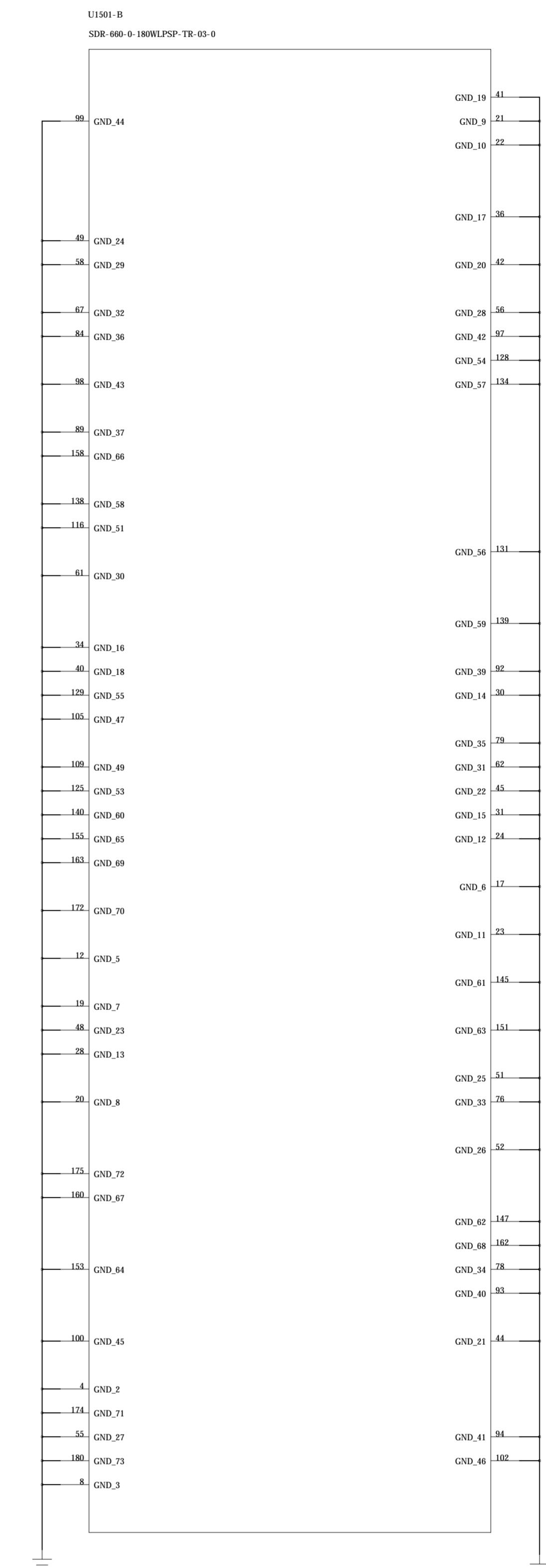
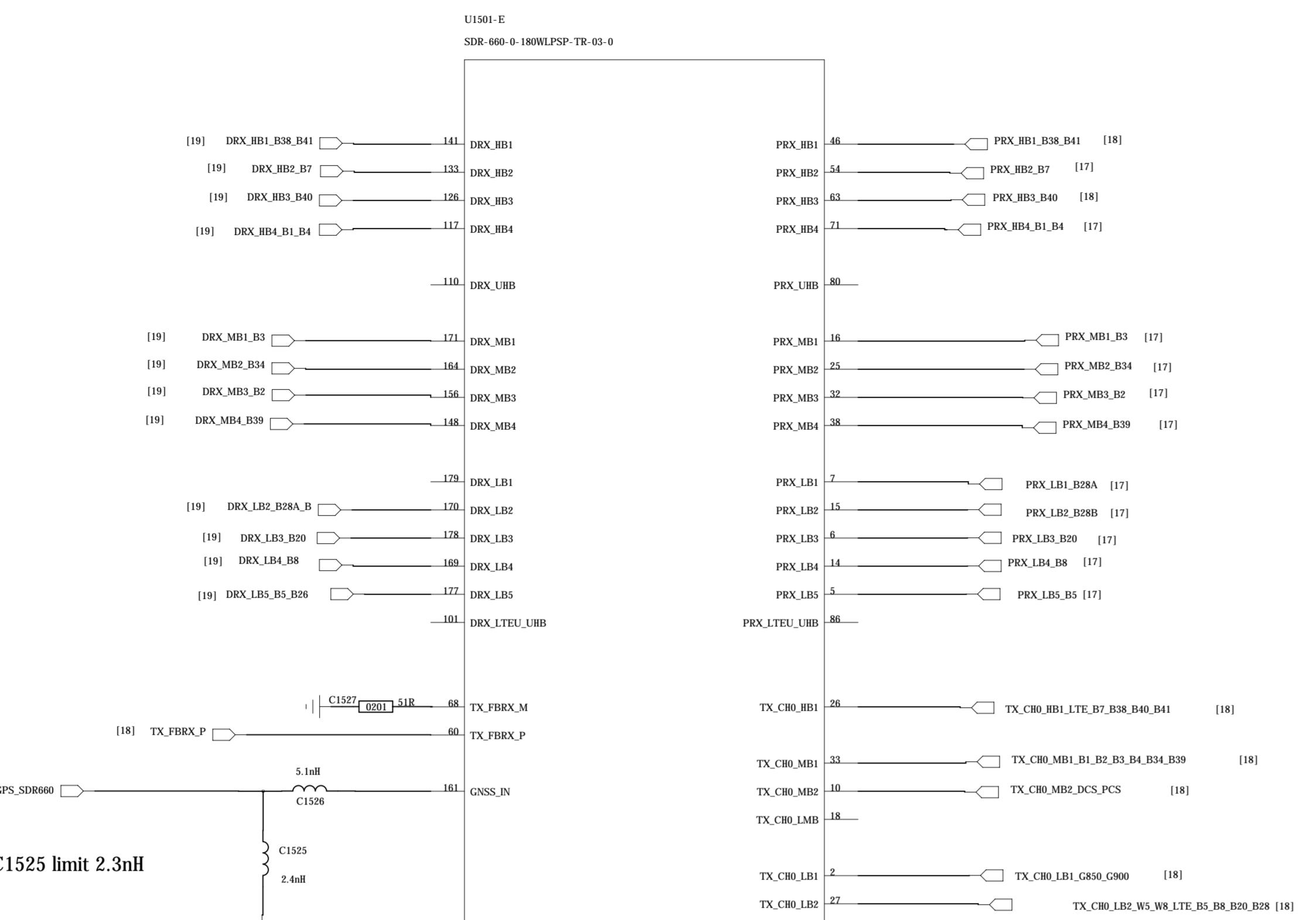


		COMPANY:  <b>&lt;Company Name&gt;</b>			
		TITLE:  <b>&lt;Title&gt;</b>			
DATED:  <b>&lt;Drawn Date&gt;</b>					
DATED:  <b>&lt;Checked Date&gt;</b>	CODE:	SIZE:	DRAWING NO:		REV:
DATED:  <b>&lt;QC Date&gt;</b>	<b>&lt;Code&gt; A0 &lt;Drawing Number&gt;&lt;Revision&gt;</b>				
DATED:  <b>&lt;Release Date&gt;</b>	SCALE: <b>&lt;Scale&gt;</b>			SHEET: <b>b4 22</b>	

REVISION RECORD			
UTR	ECO NO.	APPROVED	DATE

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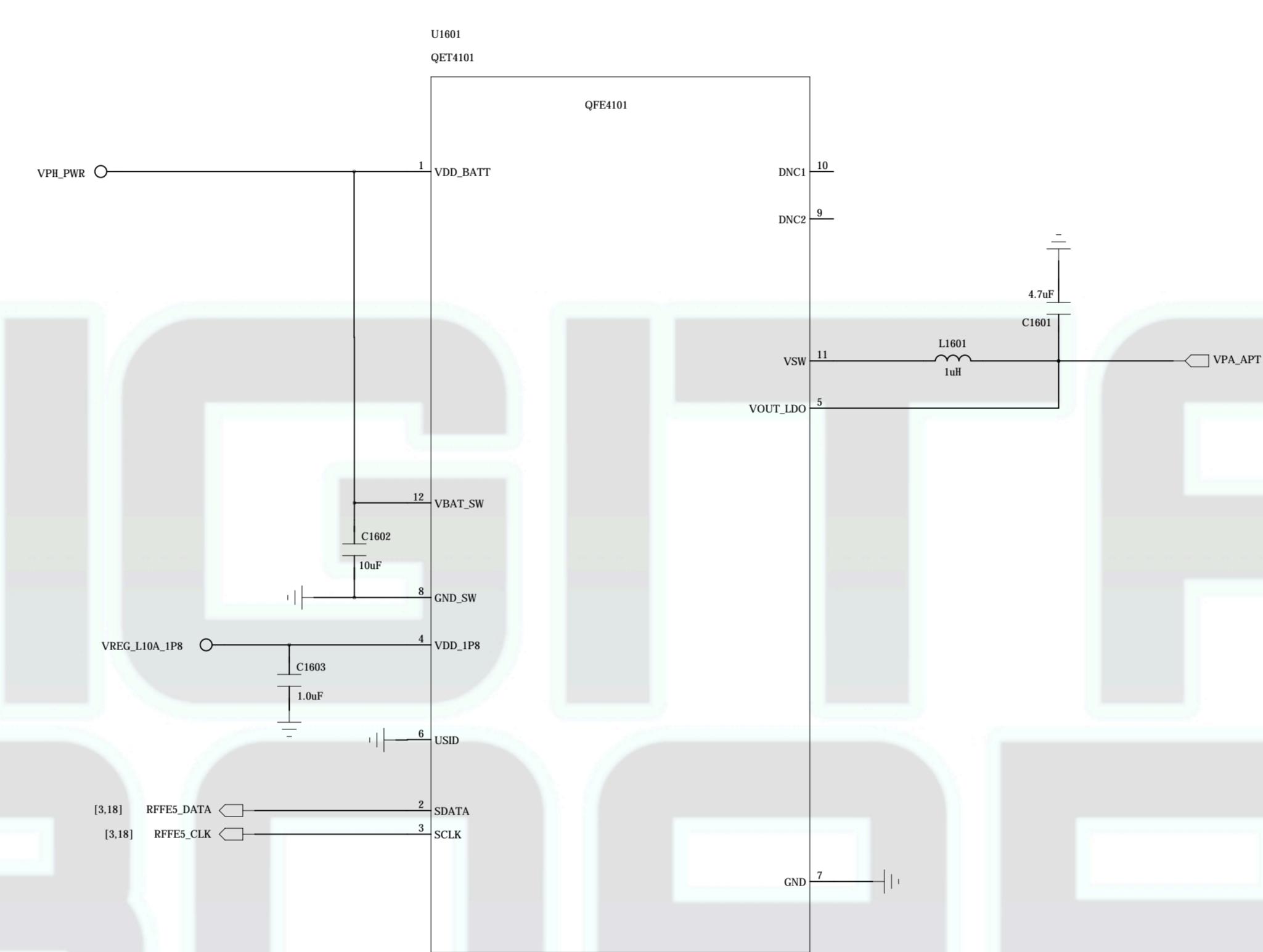
D



### QPHY\_ETDAC\_TEST

COMPANY:	<Company Name>		
TITLE:	<Title>		
DRAWN:	<Drawn By>	DATED:	<Drawn Date>
CHECKED:	<Checked By>	DATED:	<Checked Date>
QUALITY CONTROL:	<QC Date>		
RELEASED:	<Released By>	DATED:	<Release Date>
SCALE:	<Scale>	SIZE:	<Drawing Number><Revision>
REV:			

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



The schematic diagram illustrates a power supply and digital interface circuit. It includes a VREG\_L10A\_1P8 regulator connected to VDD\_1P8 through a capacitor C1603 and a 1.0uF bypass capacitor. The VDD\_1P8 line also connects to GND\_SW and a node labeled 12, which is connected to VBAT\_SW. A 10uF capacitor is connected between node 12 and GND\_SW. The VBAT\_SW line is connected to node 12 and to a VSW terminal. The VOUT\_LDO terminal is connected to node 11, which is connected to L1601 (1uH) and C1601 (4.7uF). The output of the filter is connected to VPA\_APT [18]. The USID signal is connected to node 6. The RFFE5\_DATA and RFFE5\_CLK signals are multiplexed onto the SDATA and SCLK lines, respectively. The GND line is connected to node 7.

VREG\_L10A\_1P8 → VDD\_1P8 (4) → C1603 → GND\_SW → 12 → VBAT\_SW

VBAT\_SW → 12 → 10uF → GND\_SW

VDD\_1P8 → 12 → VSW

VOUT\_LDO → 11 → L1601 (1uH) → C1601 (4.7uF) → VPA\_APT [18]

USID → 6

[3,18] RFFE5\_DATA → 2 → SDATA

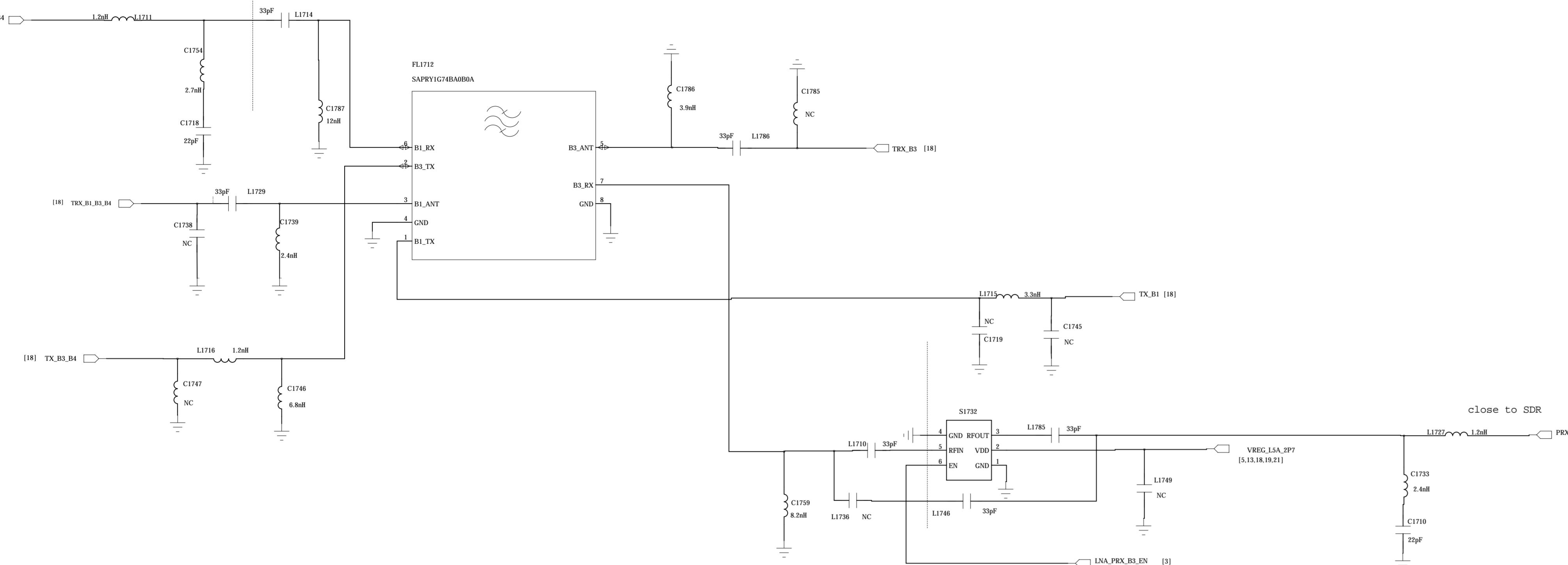
[3,18] RFFE5\_CLK → 3 → SCLK

GND → 7

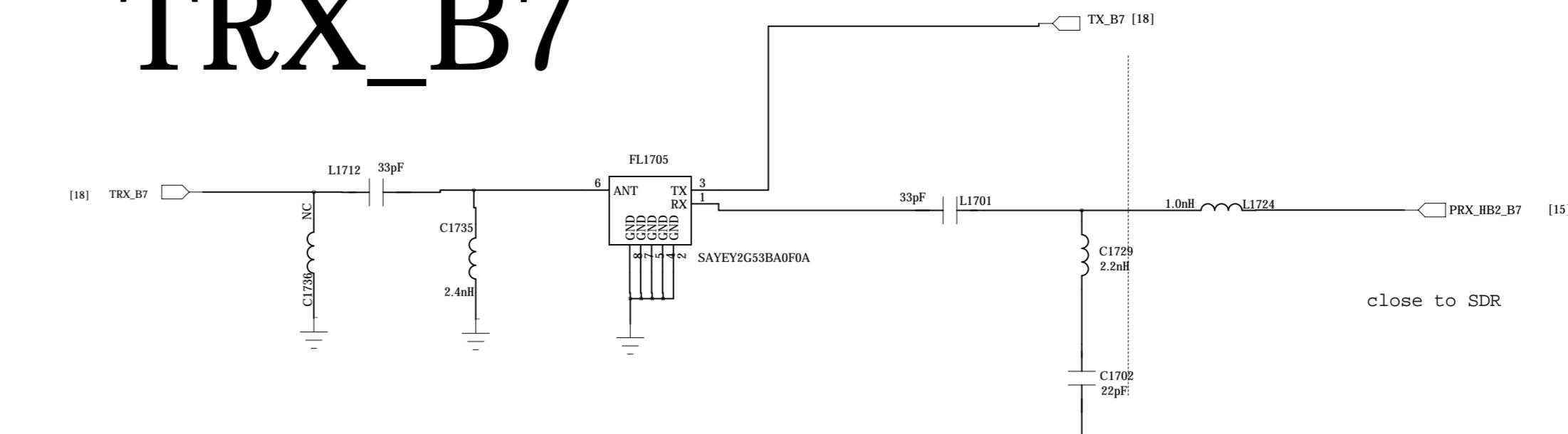
COMPANY:	<Company Name>		
TITLE:	<Title>		
Date>	CODE:	SIZE:	DRAWING NO:
Date>	<Code>	A0	<Drawing Number><Revision>
Date>	SCALE: <Scale>		SHEET: 16 22

REVISION RECORD			
LTN	ECO NO.	APPROVED:	DATE:

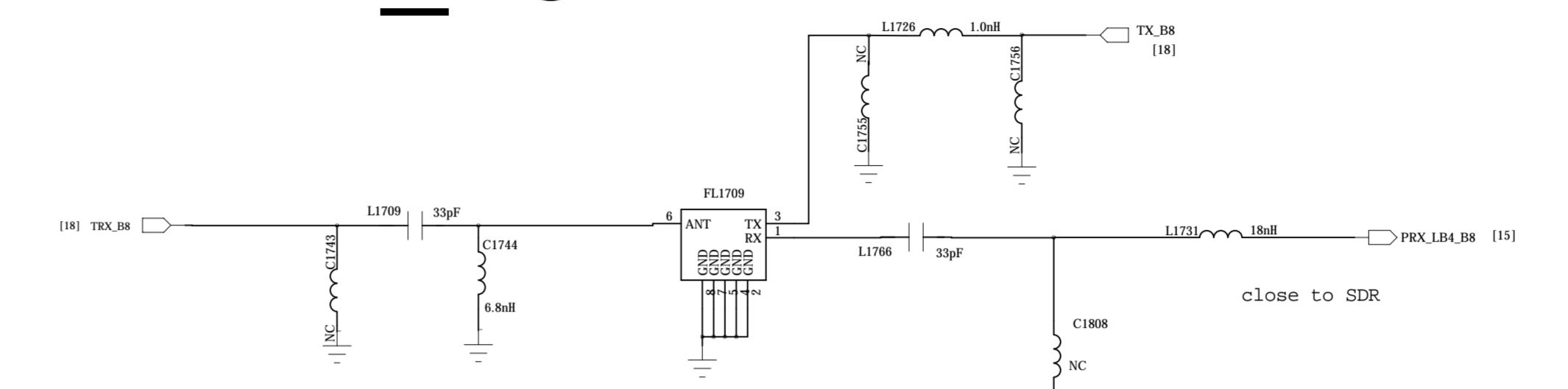
**TRX\_B1\_B3\_B4**



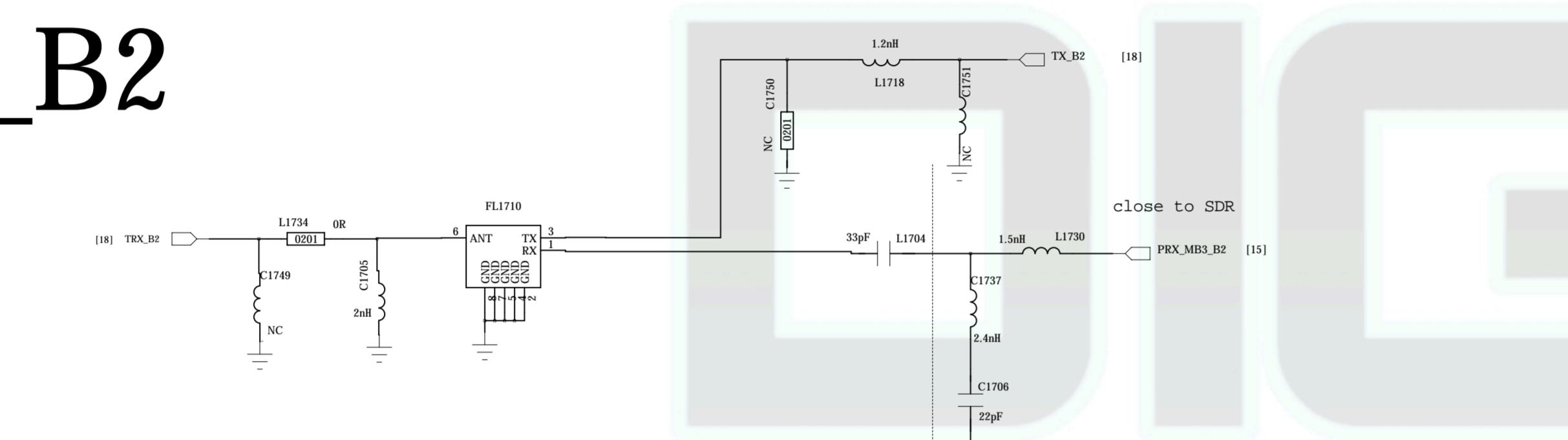
**TRX\_B7**



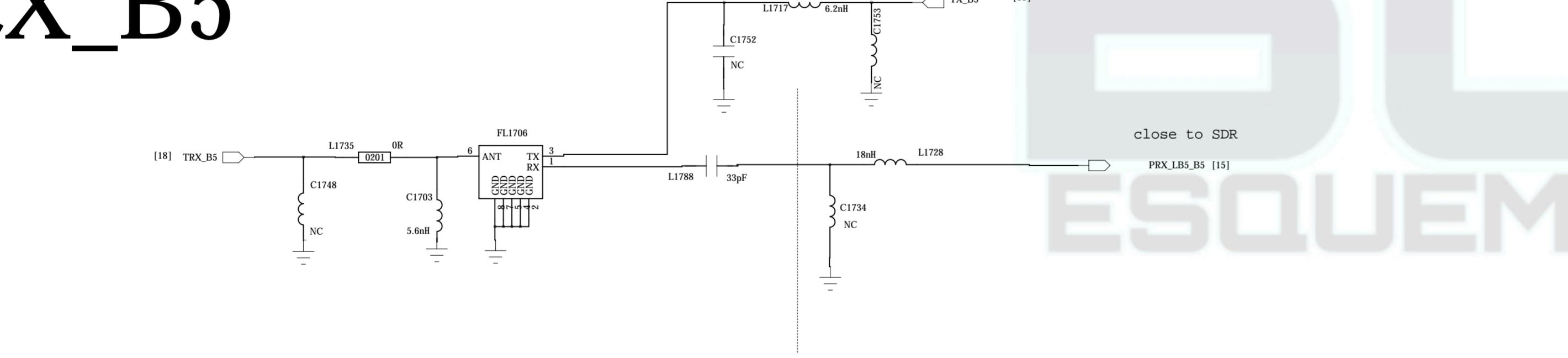
**TRX\_B8**



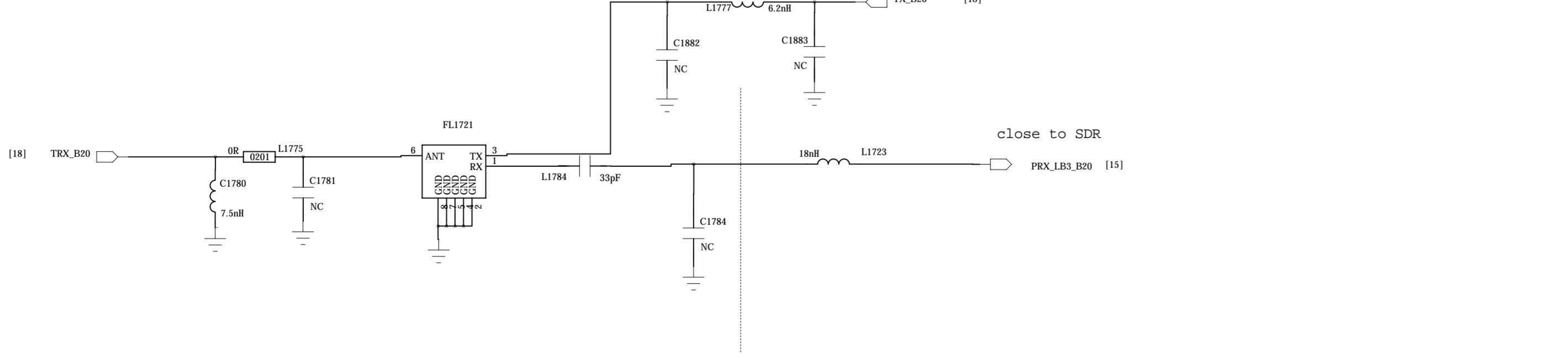
**TRX\_B2**



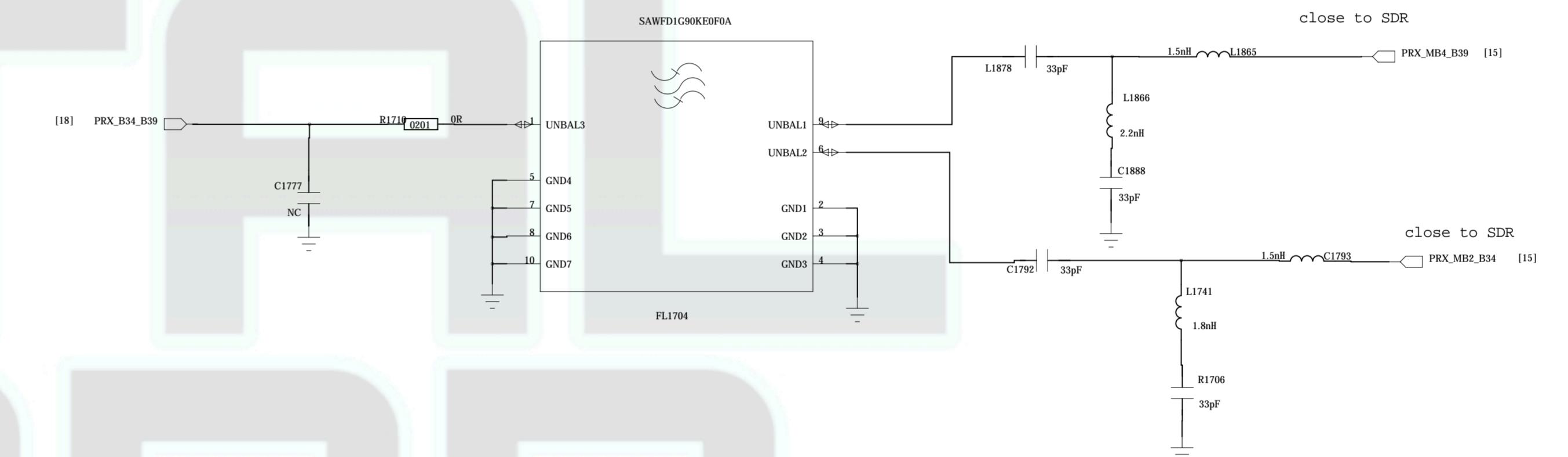
**TRX\_B5**



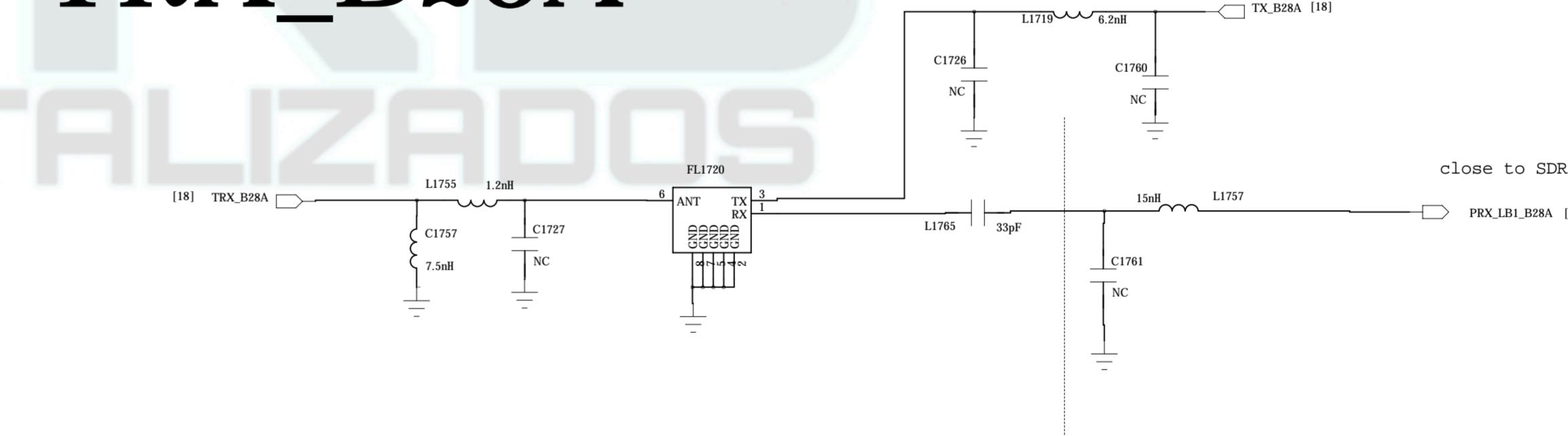
**TRX\_B20**



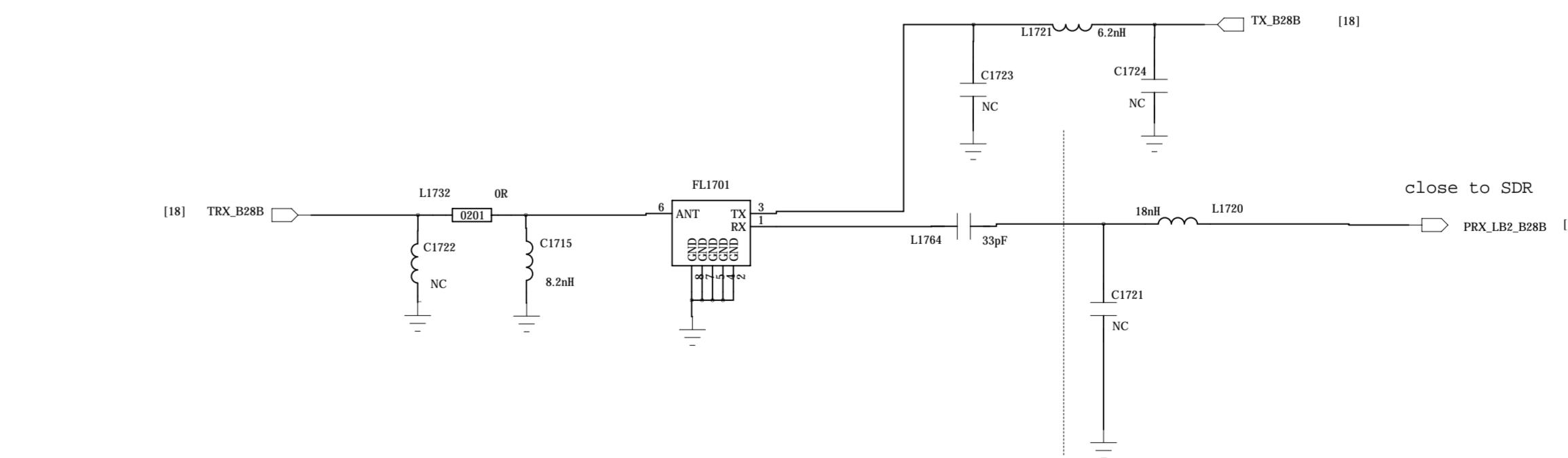
**PRX\_B34\_B39**



**TRX\_B28A**



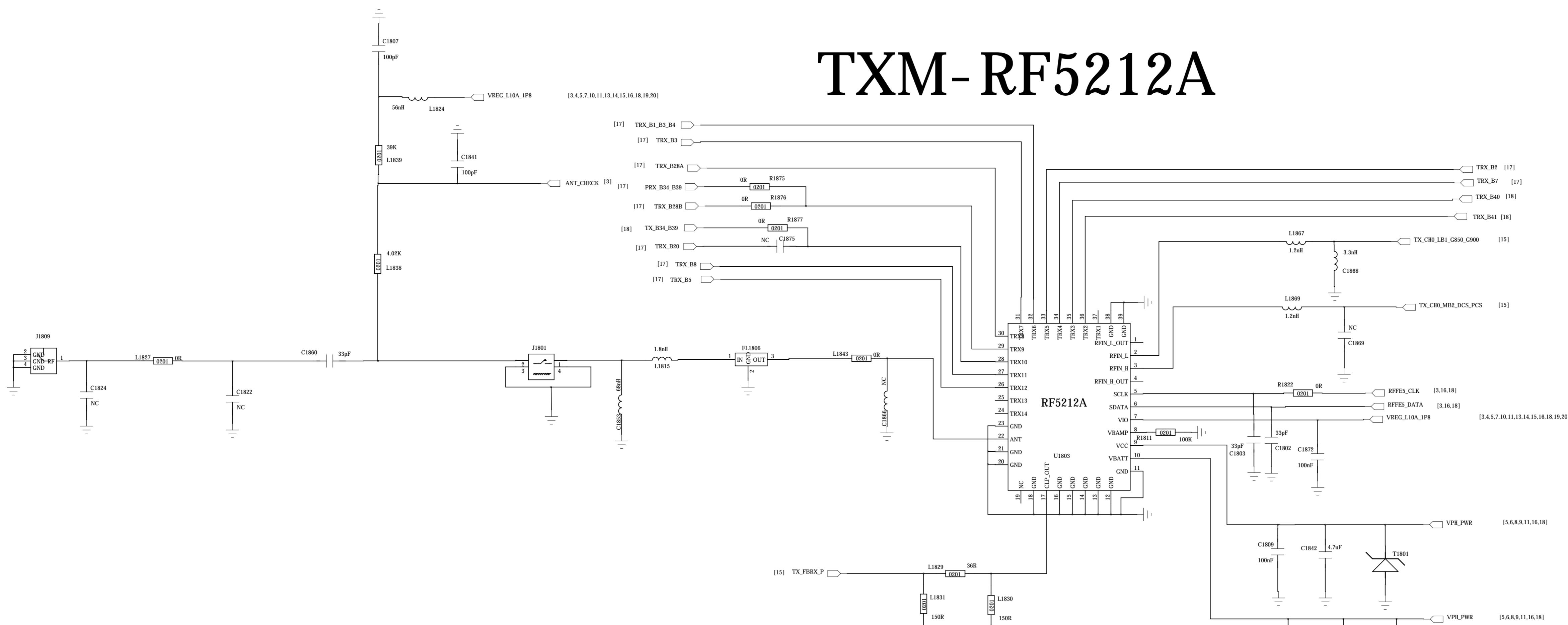
**TRX\_B28B**



COMPANY: <Company Name>
TITLE: <Title>
DRAWN: <Drawn By> DATED: <Drawn Date>
CHECKED: <Checked By> DATED: <Checked Date>
QUALITY CONTROLLED: <QC Controlled By> DATED: <QC Date>
RELEASED: <Released By> DATED: <Release Date>
SCALE: <Scale> SHEET: 1F 22

REVISION RECORD			
REV	ECO NO.	APPROVED:	DATE:

# TXM-RF5212A



MMMB\_PA

PRX\_B41

PRX\_B40

PA\_THERMO

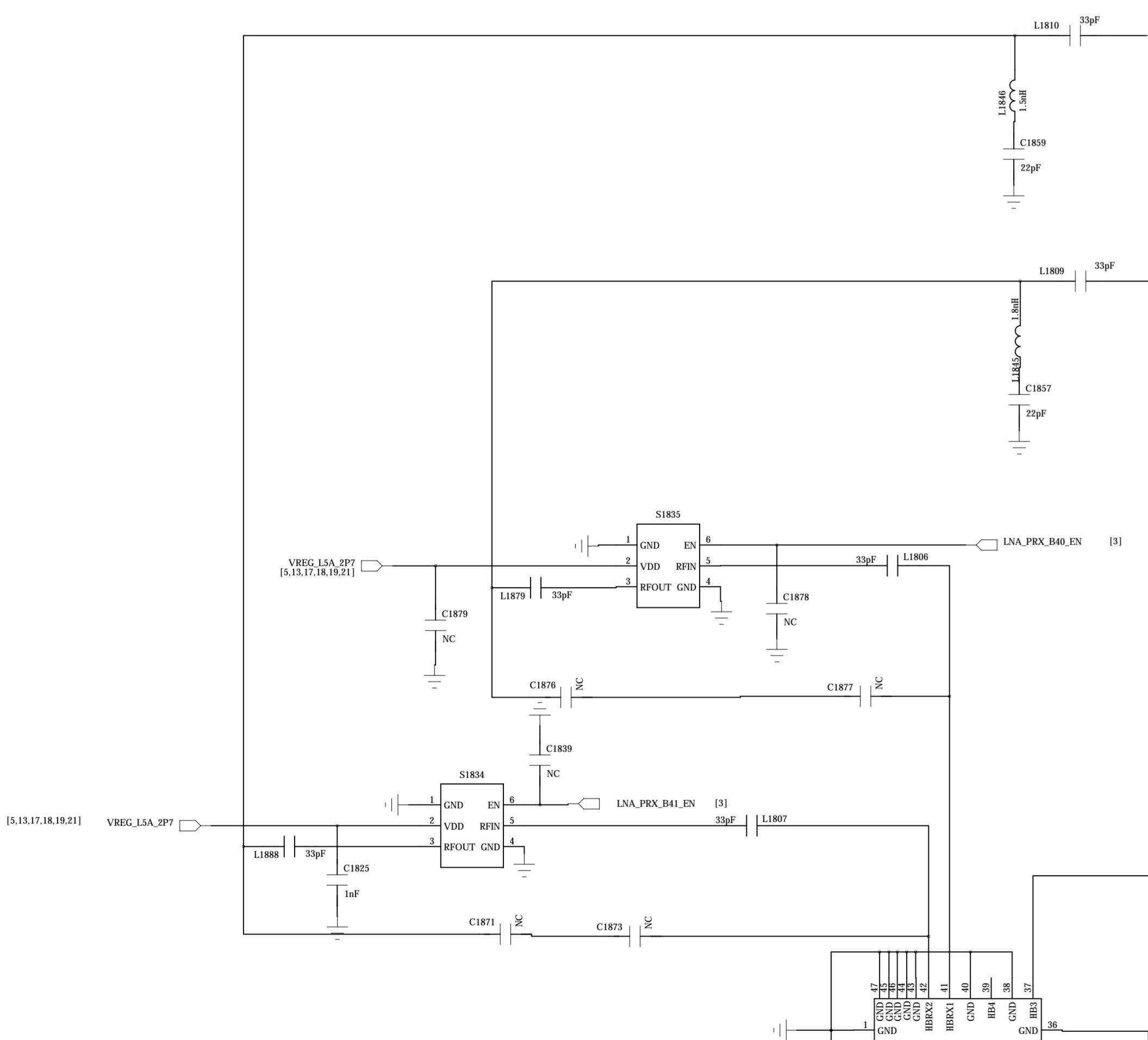
TX\_B7

TRX\_B40

SAR\_SENSOR

TRX\_B41

TX\_B34\_B39

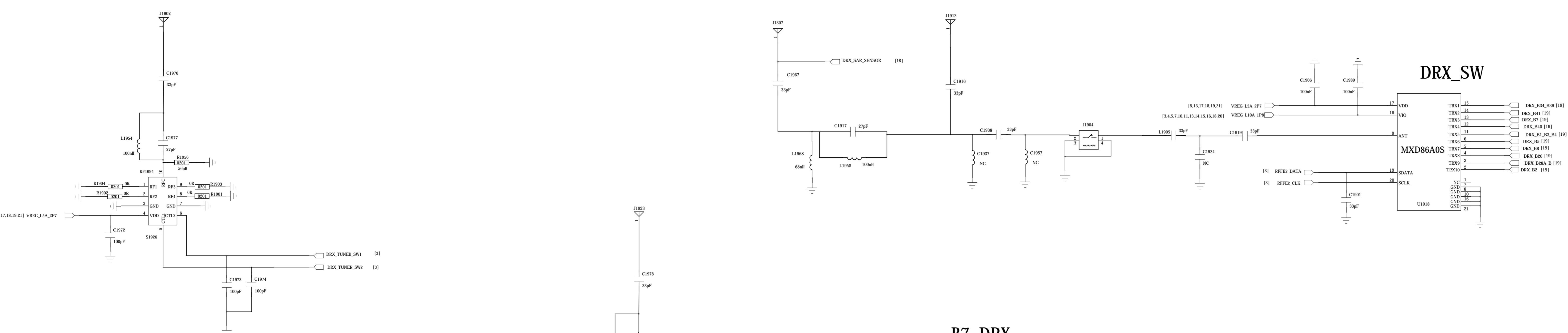


A

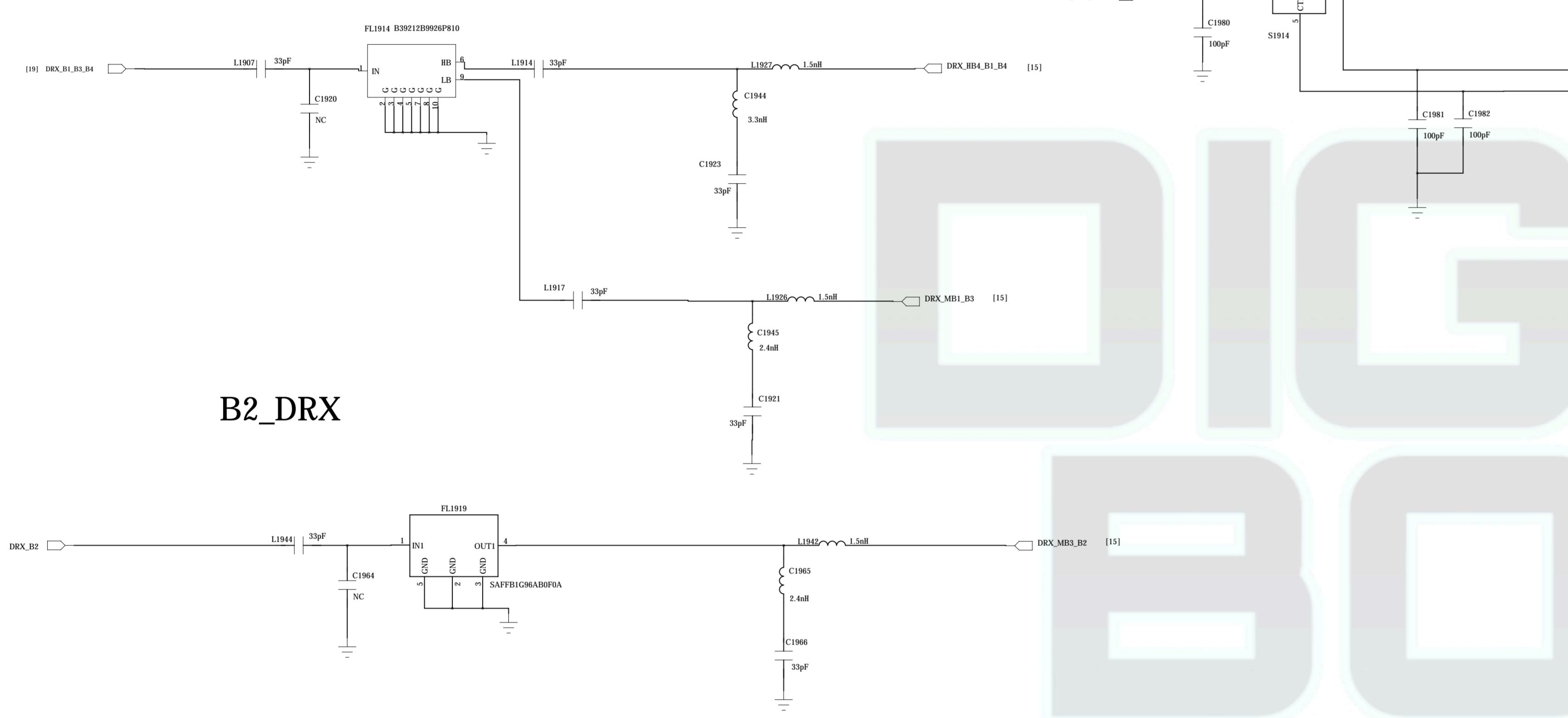
COMPANY:	<Company Name>		
TITLE:	<Title>		
DRAWN:	<Drawn By>		
CHECKED:	<Checked Date>		
QUALITY CONTROL:	<QC By>		
RELEASED:	<Released By>		
CODE:	SIZE:	DRAWING NO.:	REV.:

<Code> A0 <Drawing Number><Revision>

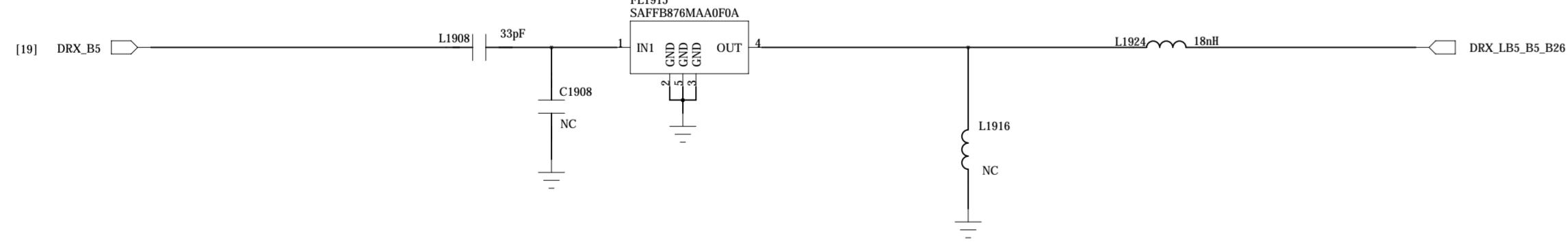
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



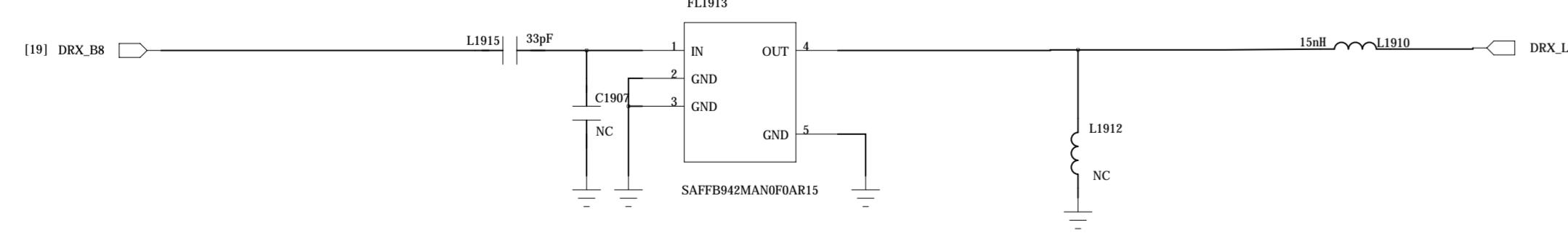
B1\_B3\_B4\_DRX



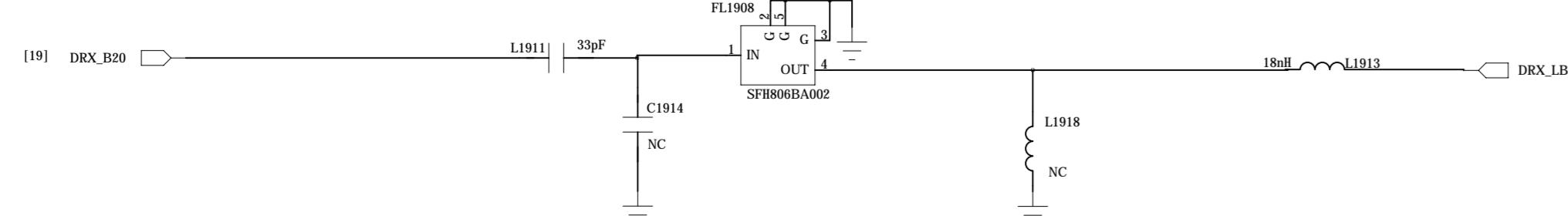
B5\_DRX



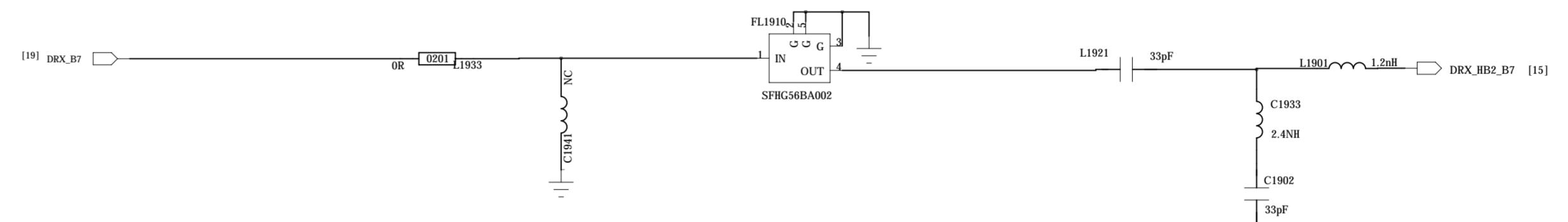
B8 DRX



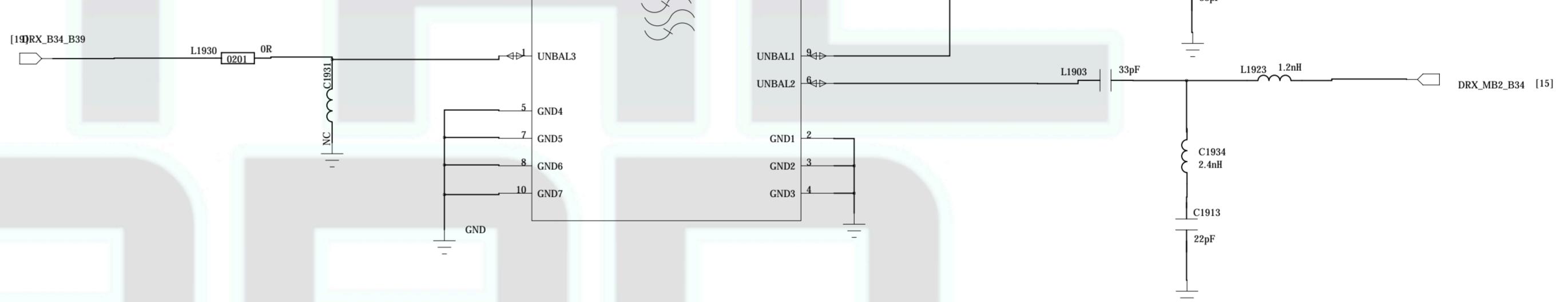
B20 DRX



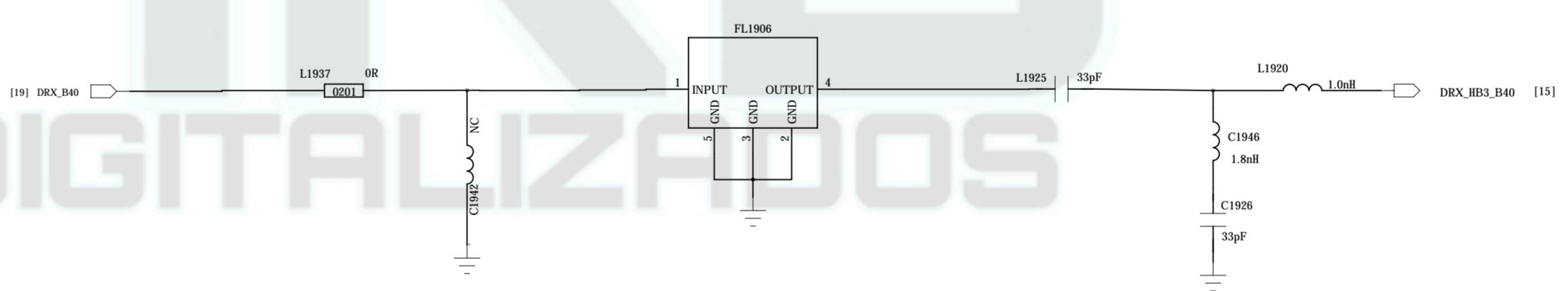
B7\_DRX



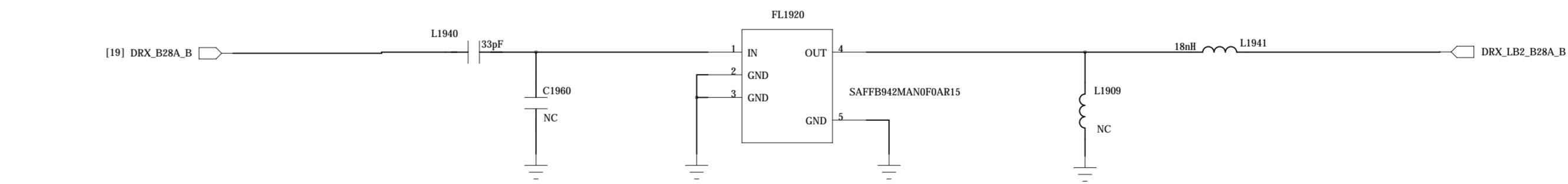
DRX\_B34\_B39



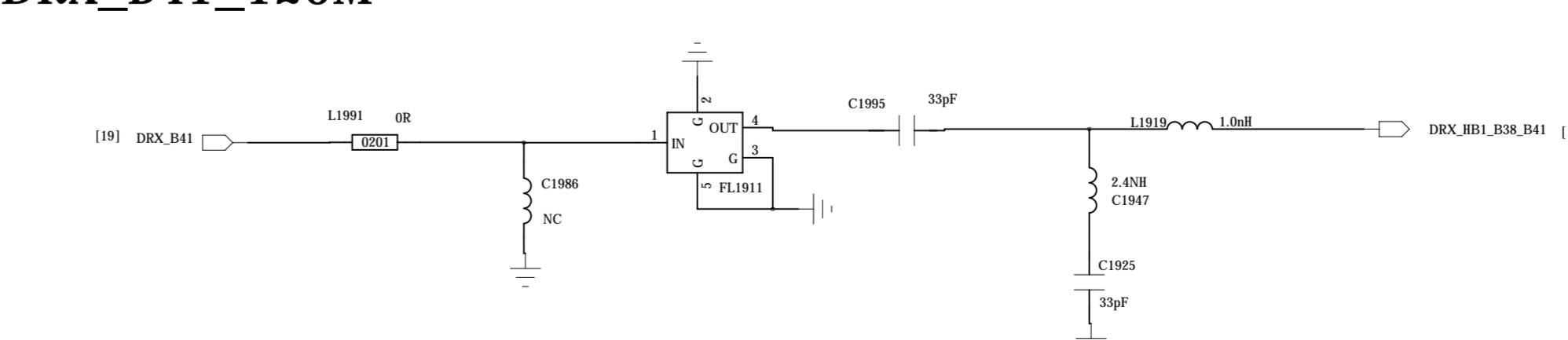
B40\_DRX



B28 A+B DRX

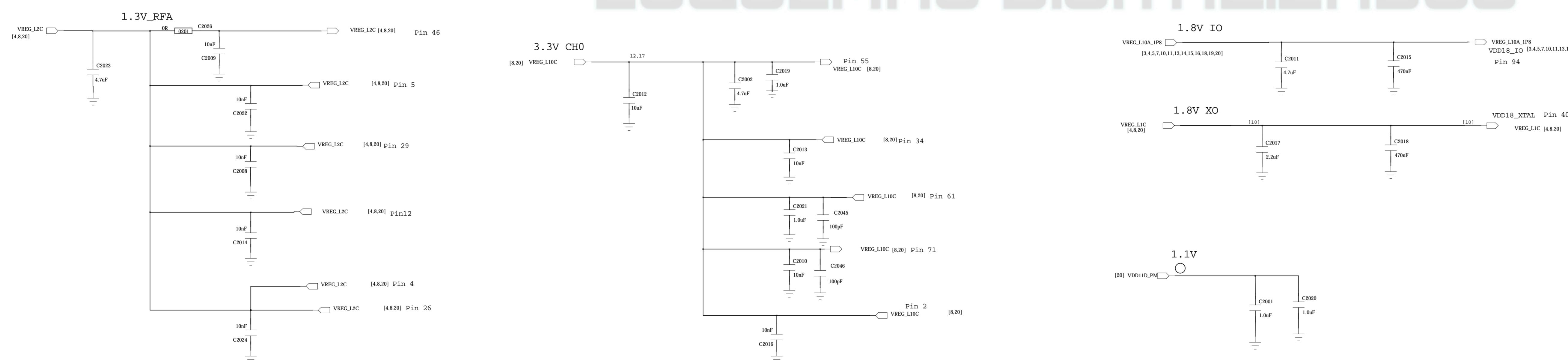
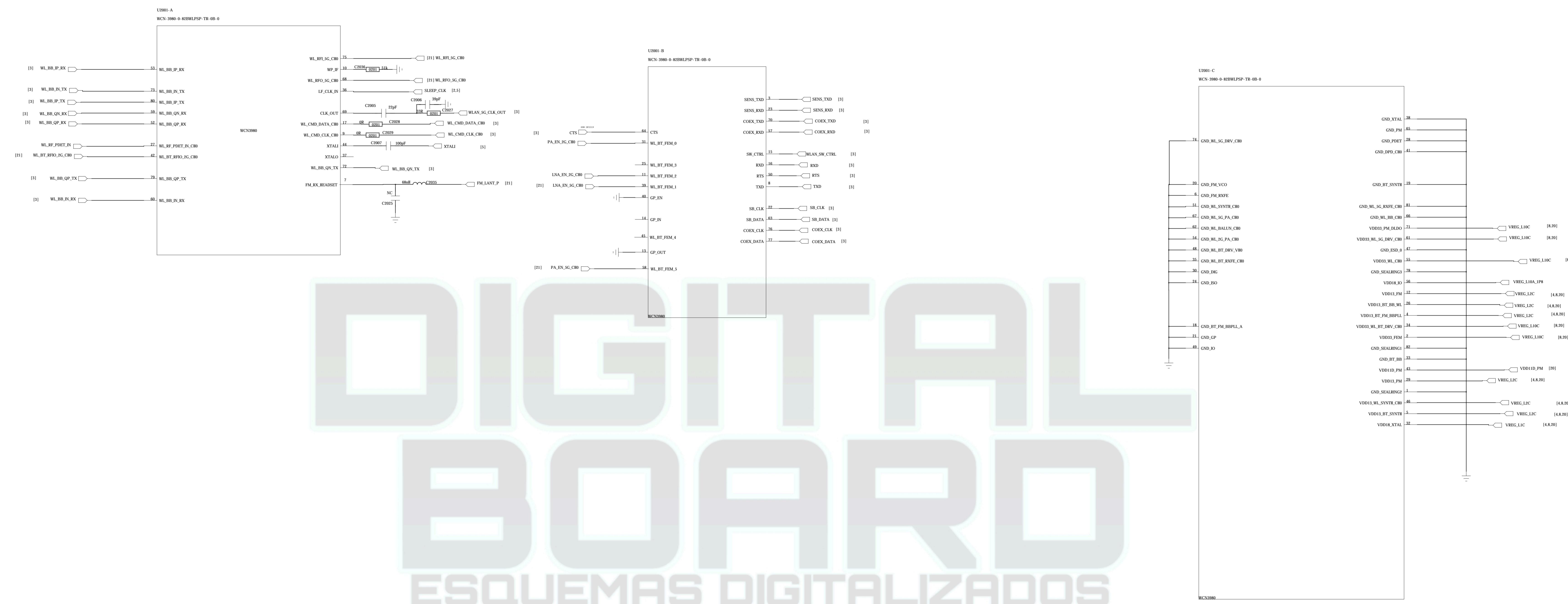


DRX B41 120M



COMPANY:  <b>&lt;Company Name&gt;</b>			
TITLE:  <b>&lt;Title&gt;</b>			
DATED:  <b>&lt;Drawn Date&gt;</b>	CODE:      SIZE:      DRAWING NO:      REV:		
DATED:  <b>&lt;Checked Date&gt;</b>	<b>&lt;Code&gt; A0 &lt;Drawing Number&gt;&lt;Revision&gt;</b>		
DATED:  <b>&lt;QC Date&gt;</b>			
DATED:  <b>&lt;Release Date&gt;</b>	SCALE: <b>&lt;Scale&gt;</b>		SHEET: <b>10 22</b>

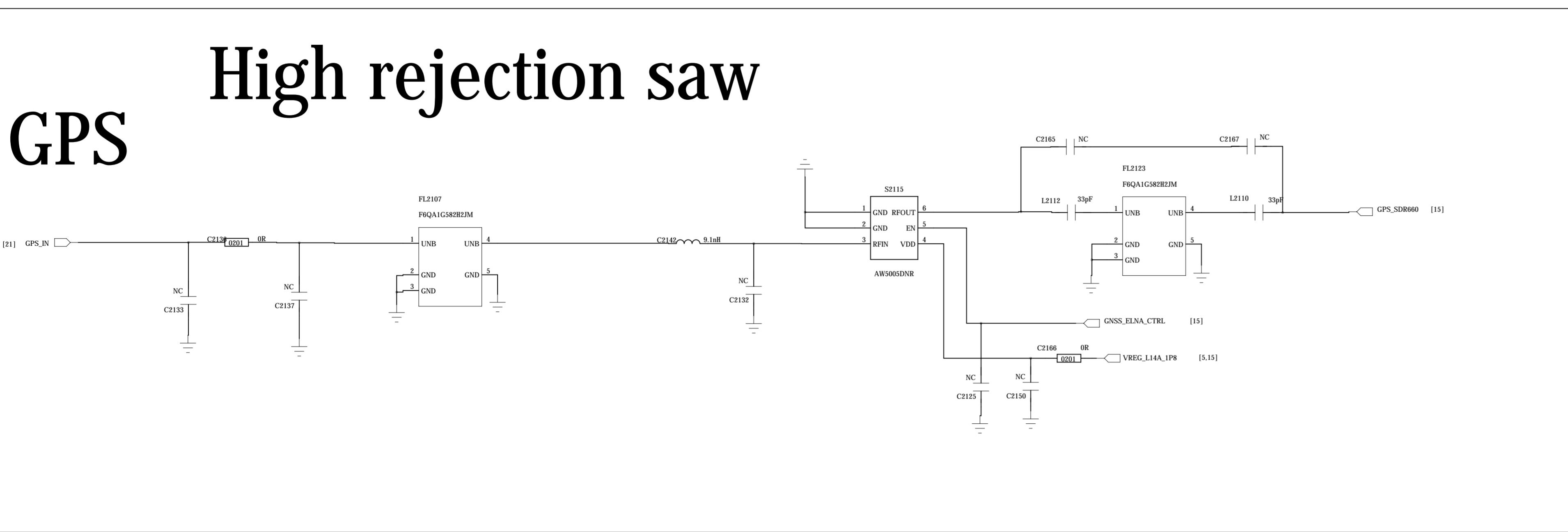
REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE:



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

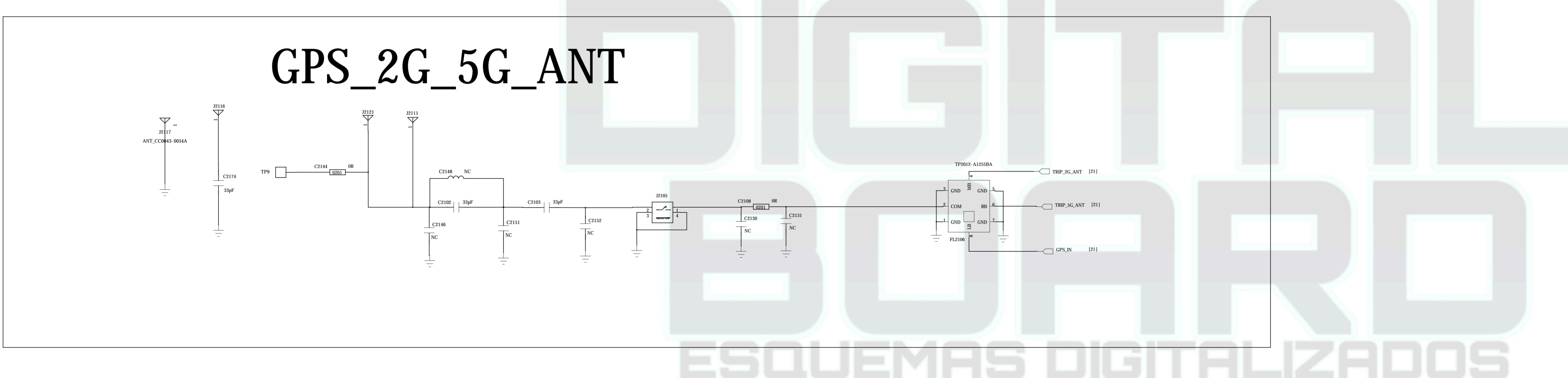
# GPS

# High rejection saw

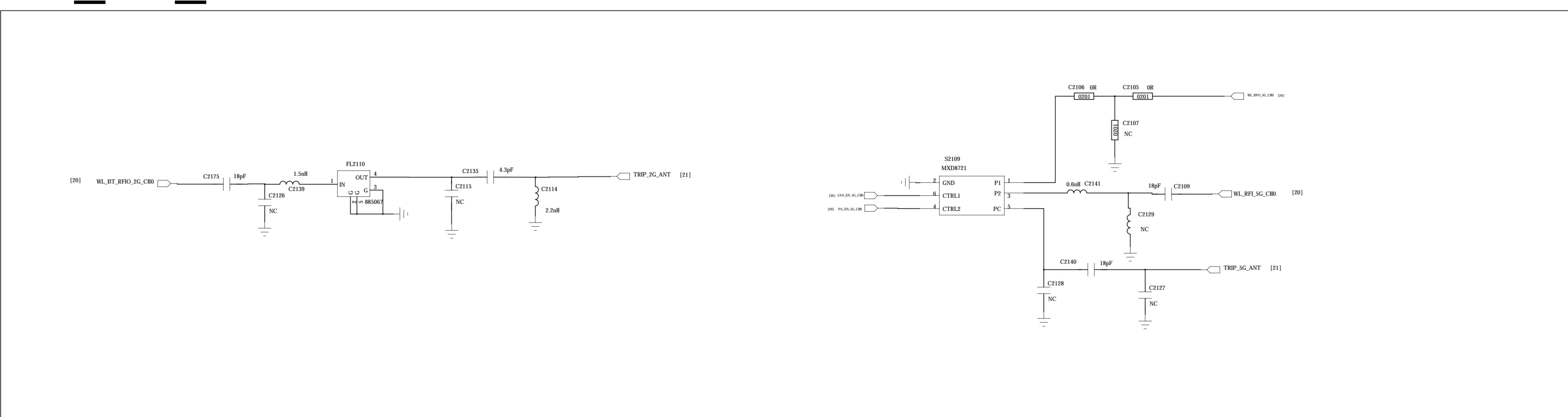


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# GPS\_2G\_5G\_ANT



# **2G\_5G\_WLAN**



COMPANY:	<Company Name>		
TITLE:	<Title>		
Date>	CODE:	SIZE:	DRAWING NO:
ed Date>	<Code>	A0	<Drawing Number×Revision>
te>	SCALE: <Scale>		SHEET: 2F 22
e Date>			

REVISION RECORD			
ltr	ECO NO.	APPROVED:	DATE:

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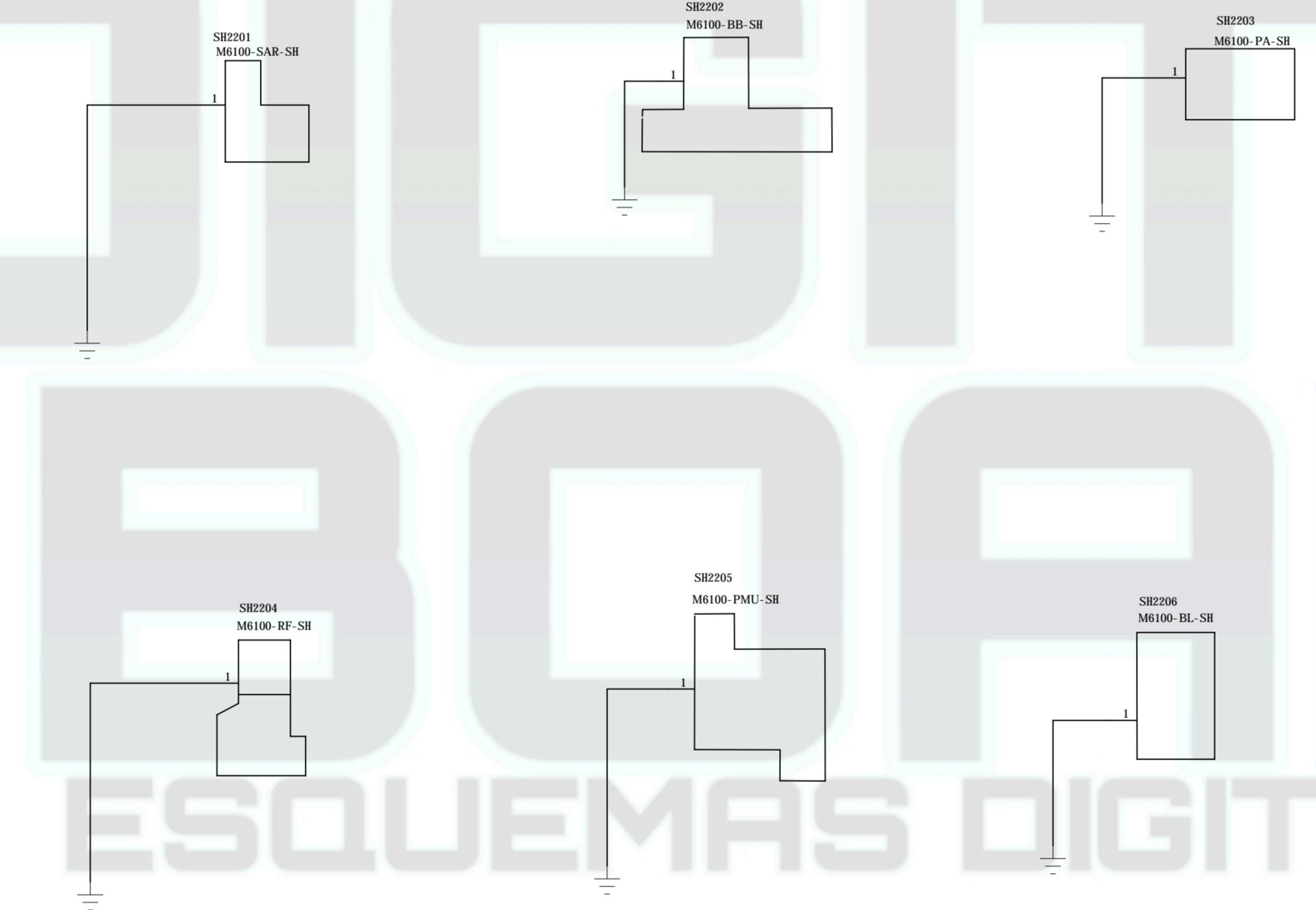
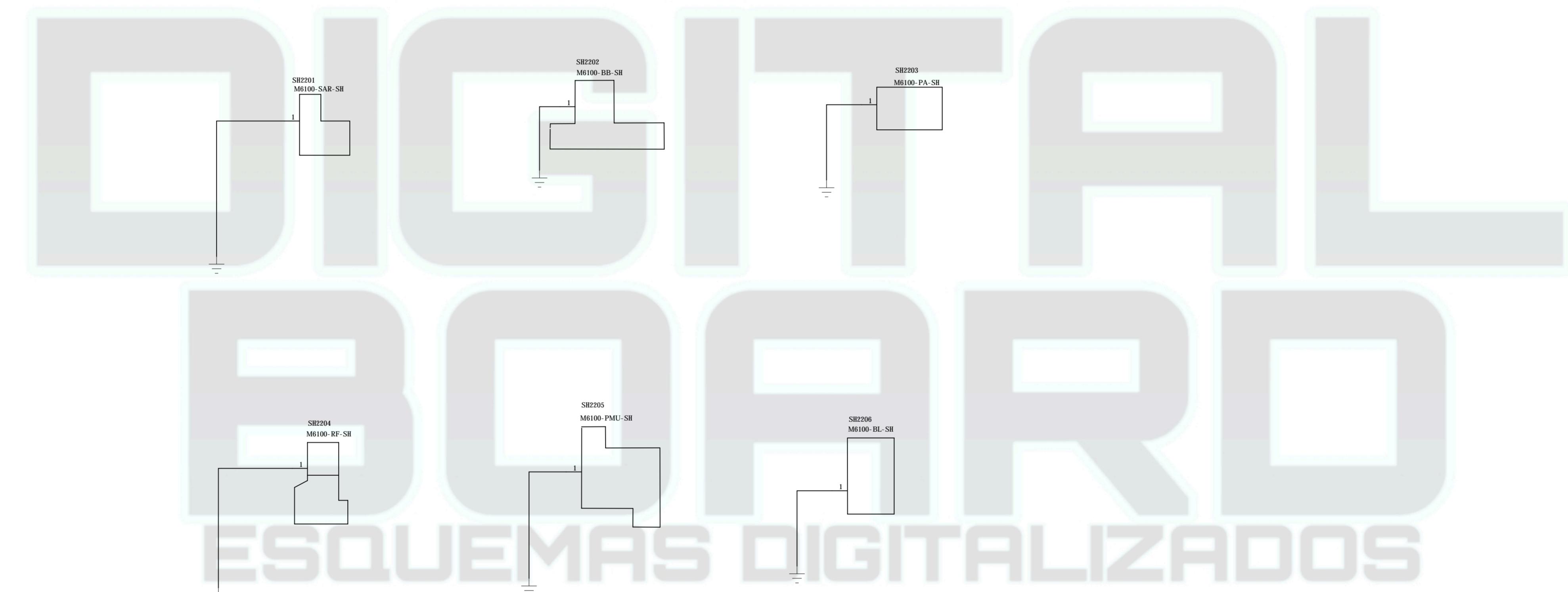
C

B

B

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A



COMPANY		<Company Name>	
TITLE			
DRAWN		<Drawn By>	
CHECKED		<Checked By>	
QUALITY CONTROL		<QC Date>	
RELEASED		<Release Date>	
CODE	SIZE	DRAWING NO. REV.	
<Code>	A0	<Drawing Number><Revision>	
SCALE	<Scale>	SHEET 22 22	