

REVISION RECORD			
ltr	ECD NO.	APPROVED:	DATE:

SDM660 GPIO Configuration For Starlord					
GPIO_0	BLSP_SPI_MOSI_1	GPIO_42	NC	GPIO_84	UIM2_CLK
GPIO_1	BLSP_SPI_MISO_1	GPIO_43	NC	GPIO_85	UIM2_RESET
GPIO_2	BLSP_SPI_CS1_N_1	GPIO_44	NC	GPIO_86	UIM2_PRESENT
GPIO_3	BLSP_SPI_CLK_1	GPIO_45	NC	GPIO_87	UIM1_DATA
GPIO_4	BLSP_UART_TX_2	GPIO_46	CAM0_RST_N	GPIO_88	UIM1_CLK
GPIO_5	BLSP_UART_RX_2	GPIO_47	CAM1_RST_N	GPIO_89	UIM1_RESET
GPIO_6	BLSP_I2C_SDA_2	GPIO_48	CAM2_RST_N	GPIO_90	UIM1_PRESENT
GPIO_7	BLSP_I2C_SCL_2	GPIO_49	NC	GPIO_91	UIM_BATT_ALARM
GPIO_8	BLSP_SPI_MOSI_3	GPIO_50	CAM_AVDD_EN	GPIO_92	GRFC_0
GPIO_9	BLSP_SPI_MISO_3	GPIO_51	CAM_AVDD_EN	GPIO_93	NC
GPIO_10	BLSP_SPI_CS_N_3	GPIO_52	NC	GPIO_94	NC
GPIO_11	BLSP_SPI_CLK_3	GPIO_53	LCD0_RESET_N	GPIO_95	NC
GPIO_12	NC	GPIO_54	SD_CARD_DET_N	GPIO_96	WDOD_DISABLE
GPIO_13	NC	GPIO_55	DP_EN_N	GPIO_97	NC
GPIO_14	BLSP_I2C_SDA_4	GPIO_56	USBC_ORIENTATION	GPIO_98	NC
GPIO_15	BLSP_I2C_SCL_4	GPIO_57	FORCED_USB_BOOT	GPIO_99	QLINK_REQUEST
GPIO_16	BLSP_UART_TX_5	GPIO_58	USB_PHY_PS	GPIO_100	QLINK_ENABLE
GPIO_17	BLSP_UART_RX_5	GPIO_59	MDP_VSYNC_P	GPIO_101	RFFE1_DATA - WTR6955 debug
GPIO_18	BLSP_UART_CTS_N_5	GPIO_60	NC	GPIO_102	RFFE1_CLK - WTR6955 debug
GPIO_19	BLSP_UART_RFR_N_5	GPIO_61	NC	GPIO_103	RFFE2_DATA - (42)QFE2101 ch0, (43)QFE4360
GPIO_20	FP_SUB_RESET	GPIO_62	NC	GPIO_104	RFFE2_CLK - (42)QFE2101 ch0, (43)QFE4360
GPIO_21	SMB_STAT	GPIO_63	NC	GPIO_105	NC
GPIO_22	BLSP_I2C_SDA_6	GPIO_64	NC	GPIO_106	NC
GPIO_23	BLSP_I2C_SCL_6	GPIO_65	NC	GPIO_107	RFFE4_DATA - (53)QAT3514, (53)QAT3550
GPIO_24	NC	GPIO_66	TS_RESET_N	GPIO_108	RFFE4_CLK - (53)QAT3514, (53)QAT3550
GPIO_25	NC	GPIO_67	TS_INT_N	GPIO_109	RFFE5_DATA
GPIO_26	WSA_SPKR_SD_N_1	GPIO_68	ACC_GYRO_DATA_AVA_INT_N	GPIO_110	RFFE6_CLK
GPIO_27	WSA_SPKR_SD_N_2	GPIO_69	ACC_GYRO_MOT_INT_N	GPIO_111	RFFE6_DATA
GPIO_28	NFC_IRQ	GPIO_70	MAG_INT_N	GPIO_112	RFFE6_CLK
GPIO_29	NFC_EN	GPIO_71	ALSP_INT_N	GPIO_113	NC
GPIO_30	NFC_DWL_REQ	GPIO_72	FP_INT_N_1	SSC_0	LPI_SPI_1_CS1_N
GPIO_31	NFC_ESE_PWR_REQ	GPIO_73	NC	SSC_1	LPI_PWR_EN
GPIO_32	CAM_MCLK0	GPIO_74	NC	SSC_2	LPI_I2C_3_SDA
GPIO_33	CAM_MCLK1	GPIO_75	NC	SSC_3	LPI_I2C_3_SCL
GPIO_34	CAM_MCLK2	GPIO_76	NC	SSC_4	LPI_SPI_2_CS_N
GPIO_35	GPIO_77	AUDIO_USBC_EN2_N	SSC_5	LPI_SPI_2_CLK	
GPIO_36	CCI_I2C_SDA0	GPIO_78	WMSS_RESETN	SSC_6	LPI_SPI_2_MOSI
GPIO_37	CCI_I2C_SCL0	GPIO_79	PWM_CNTRL	SSC_7	LPI_SPI_2_MISO
GPIO_38	CCI_I2C_SDA1	GPIO_80	AUDIO_USBC_EN1	SSC_8	LPI_SPI_1_CS_N
GPIO_39	CCI_I2C_SCL1	GPIO_81	MSS_LTE_COXM_TXD	SSC_9	LPI_SPI_1_CS_N
GPIO_40	NC	GPIO_82	MSS_LTE_COXM_RXD	SSC_10	LPI_SPI_1_MOSI
GPIO_41	FL_STROBE_TRIG	GPIO_83	UIM2_DATA	SSC_11	LPI_SPI_1_MISO

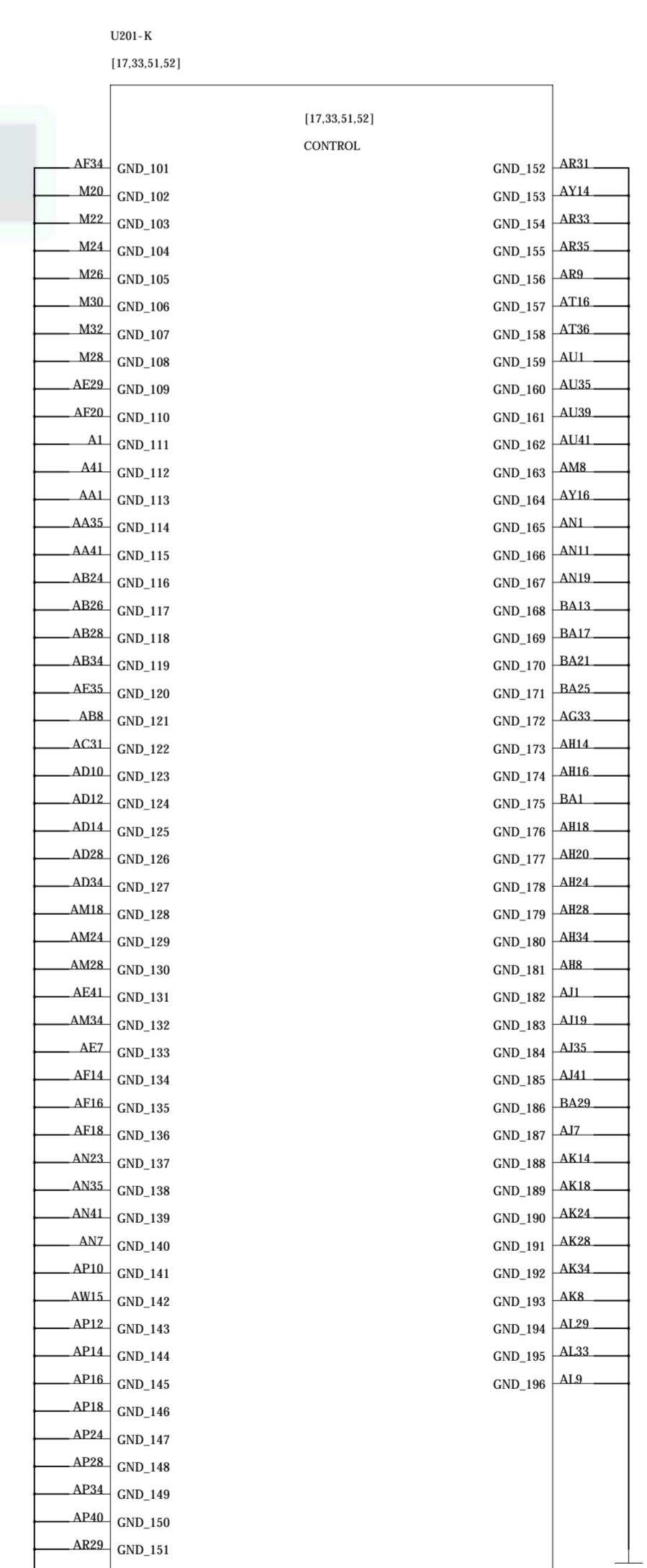
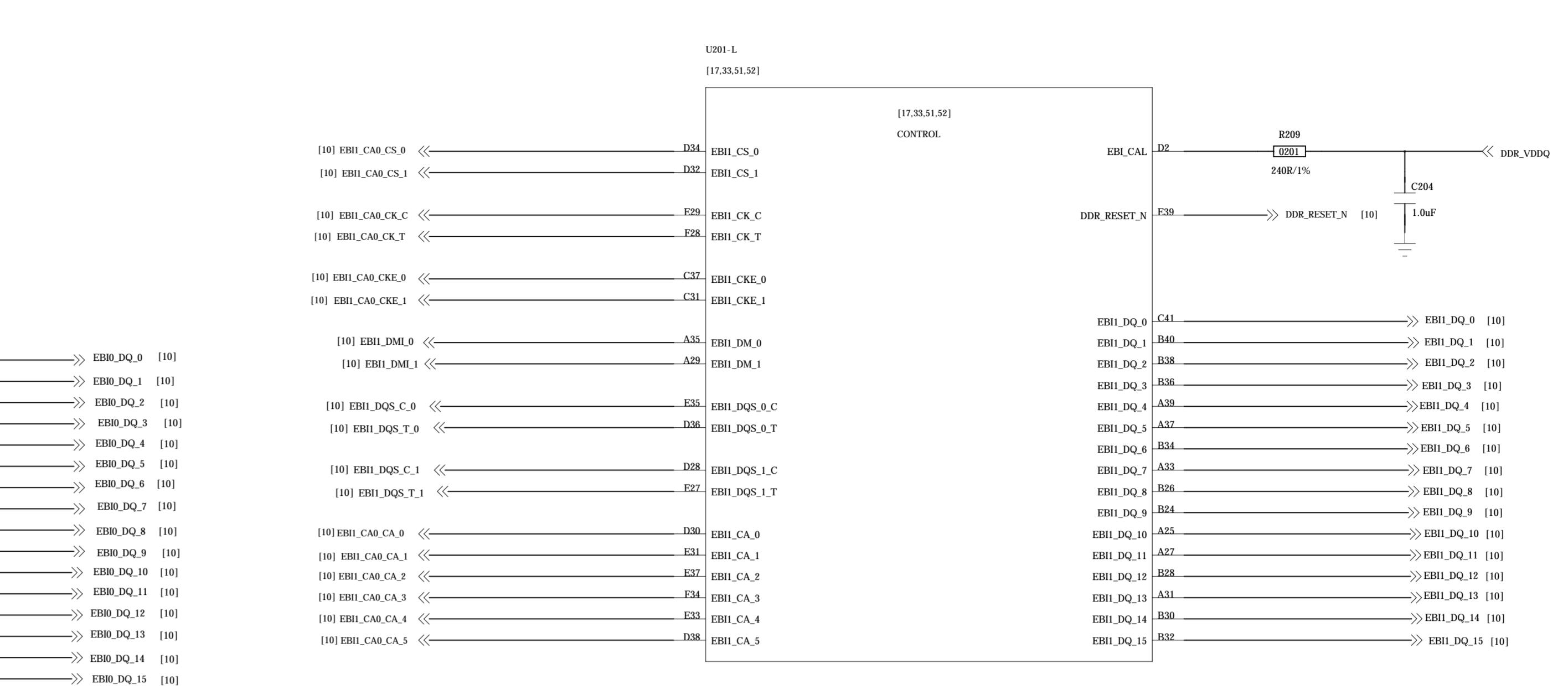
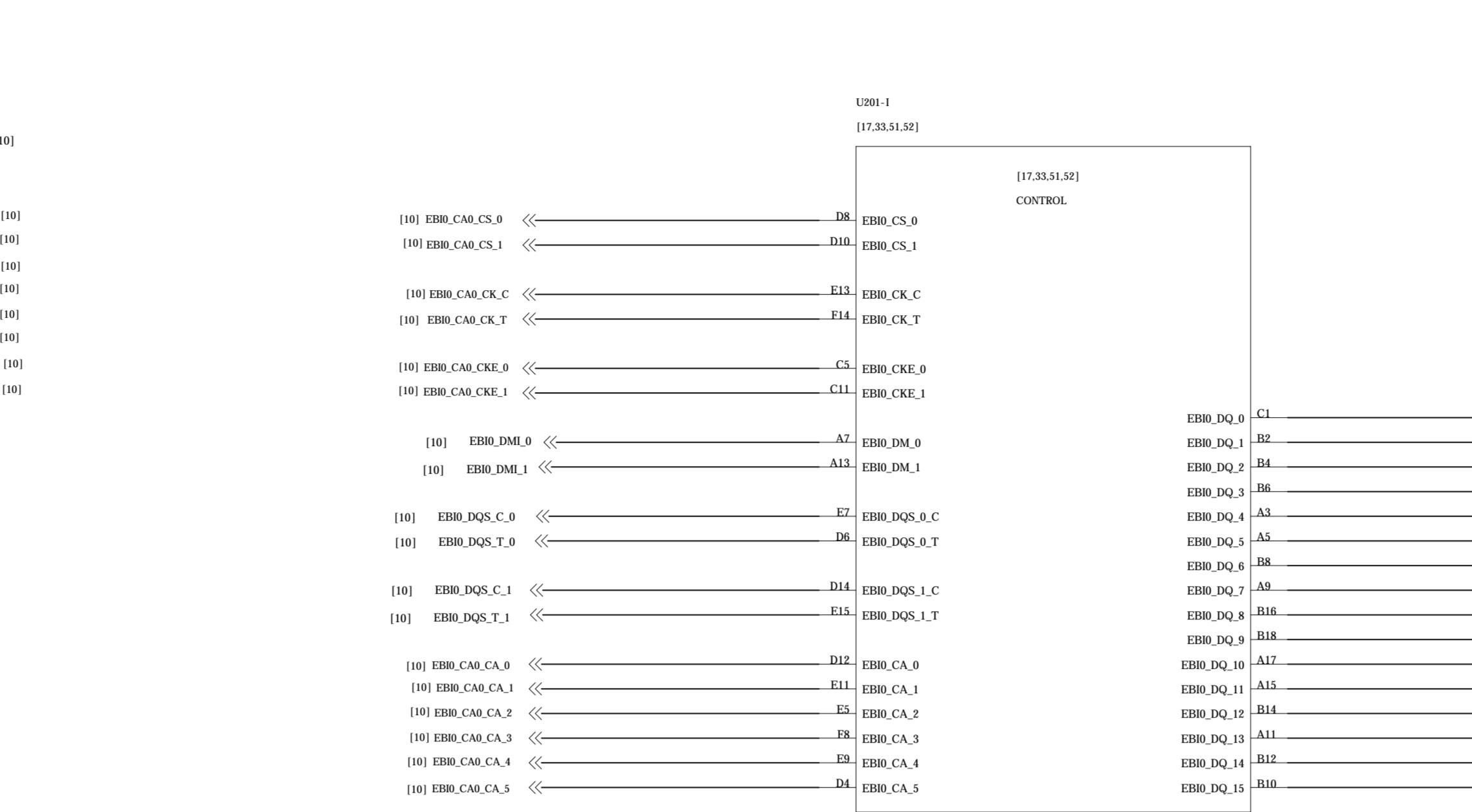
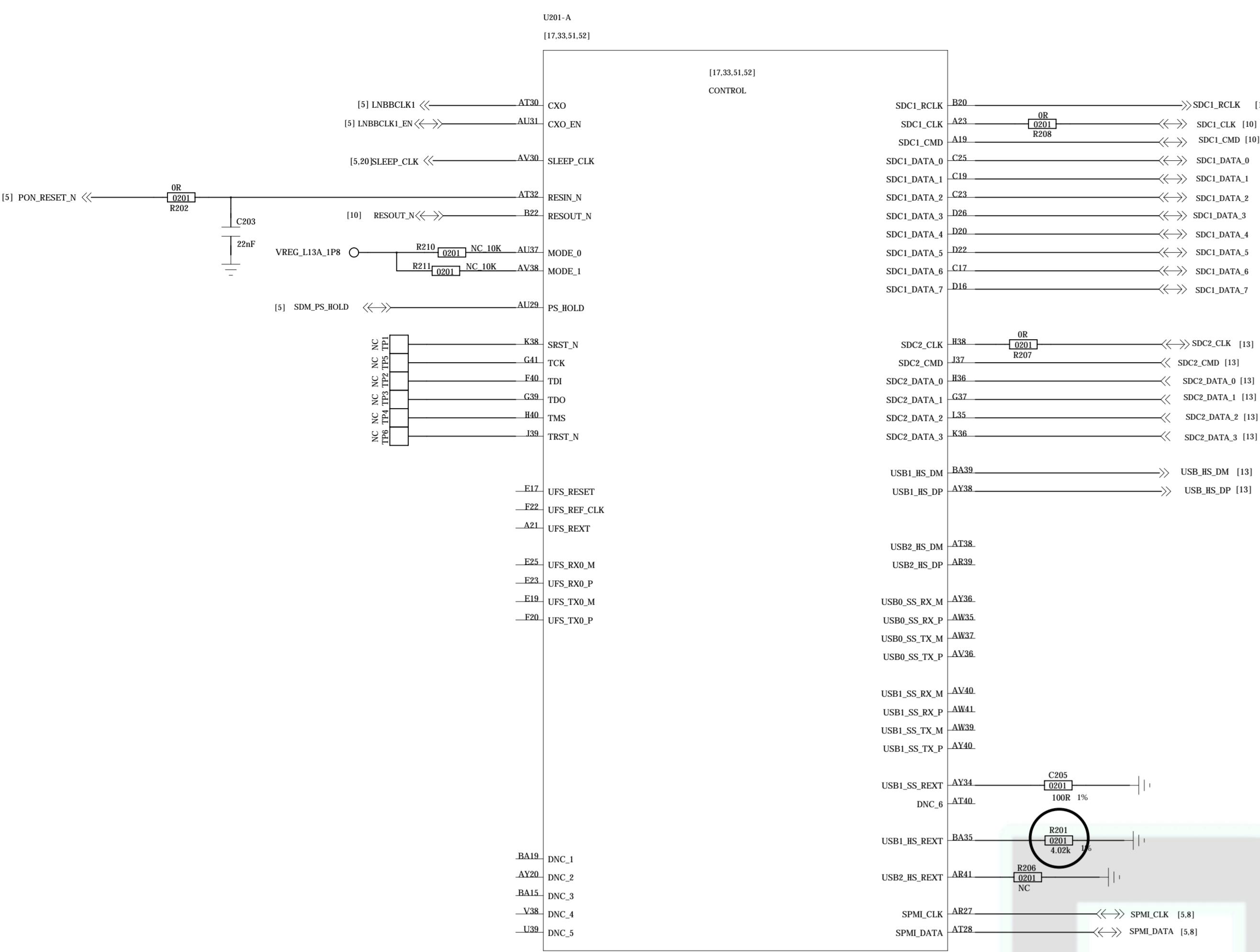
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SSC_13	LPI_UART_1_RX
SSC_14	NC
SSC_15	NC
SSC_16	NC
SSC_17	NC
SSC_18	WCD_SDM_MCLK
SSC_19	LPI_AUD_SB_CLK
SSC_20	LPI_AUD_SB_DATA0
SSC_21	LPI_AUD_SB_DATA1
SSC_22	LPI_AUD_CDC_INT1
SSC_23	LPI_AUD_CDC_INT2
SSC_24	LPI_AUD_CDC_RSTN
SSC_25	NC
SSC_26	NC
SSC_27	NC
SSC_29	NC
SSC_30	LPI_QCA_SB_CLK
SSC_31	LPI_QCA_SB_DATA0

GROOT GPIO Configuration For Starlord			
GPIO_1	OPTION1	GPIO_8	SLB
GPIO_2	DIV_CLK2	GPIO_9	uUSB_TYPEC
GPIO_3	DIV_CLK1	GPIO_10	WCSS_VCTRL
GPIO_4	NFC_CLK_REQ	GPIO_11	HOMEKEY_FP_PM_INT
GPIO_5	WLAN_SW_CTRL	GPIO_12	WIPWR_MODE
GPIO_6	SLP_CLK	GPIO_13	PM_A_GPIO_13
GPIO_7	UIM_BATT_ALARM		

DRAX GPIO Configuration For Starlord			
GPIO_1	OPTION2	GPIO_8	SD_CARD_DET_N
GPIO_2	LPI_PWR_EN	GPIO_9	WCSS_VCTRL
GPIO_3	FRONT_CAM_DVDD_EN	GPIO_10	SLB
GPIO_4	REAR_CAM_DVDD_EN	GPIO_11	LP4x_CTRL
GPIO_5	NC	GPIO_12	LP4x_MODE
GPIO_6	FP_VDD_EN		
GPIO_7	KEY_VOL_UP_N		

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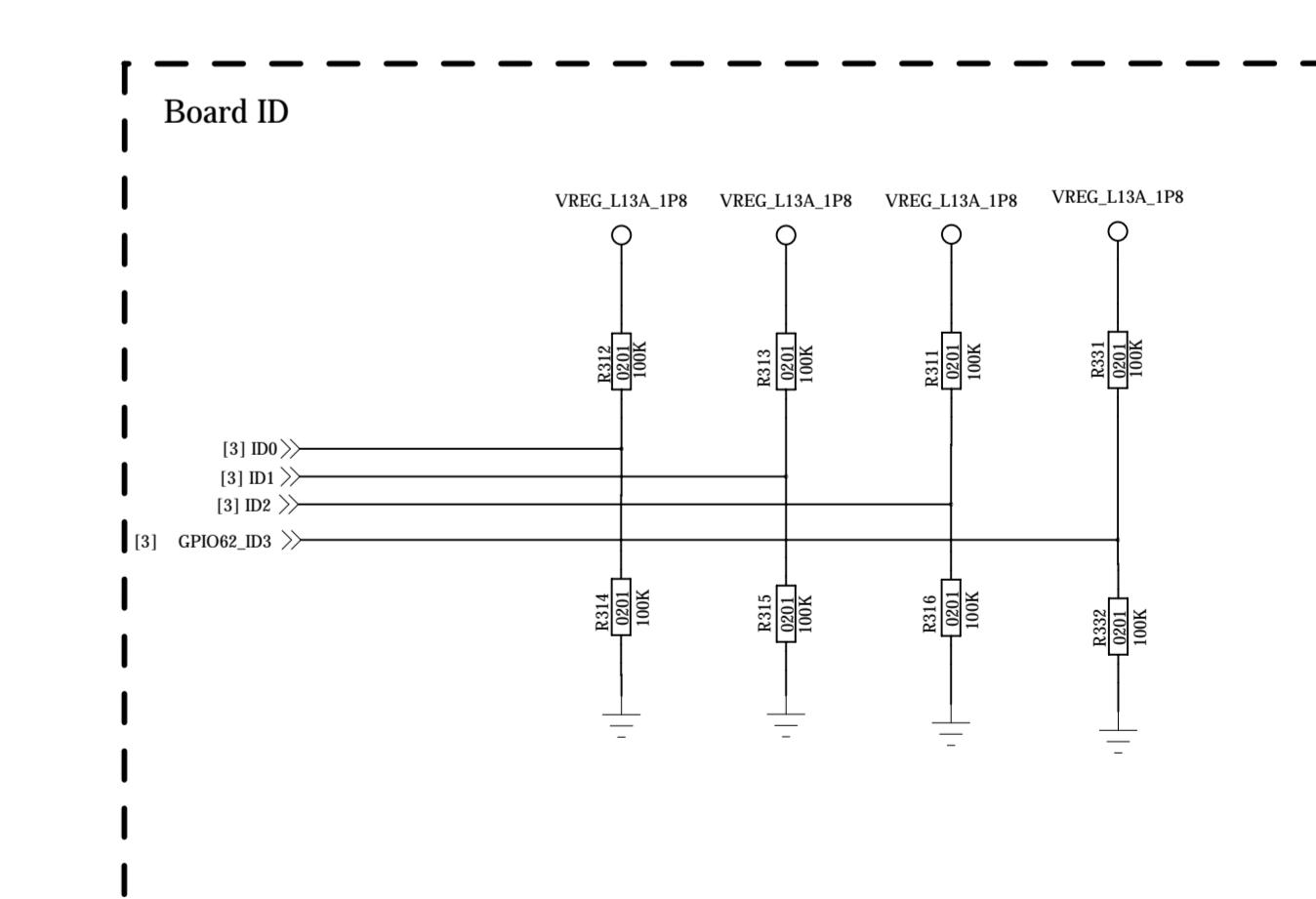
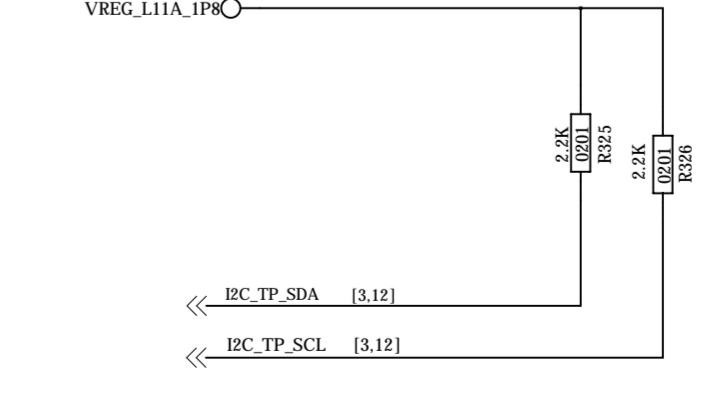
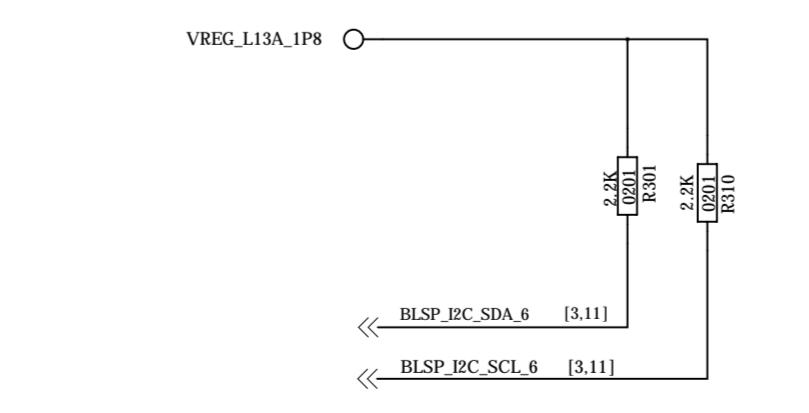
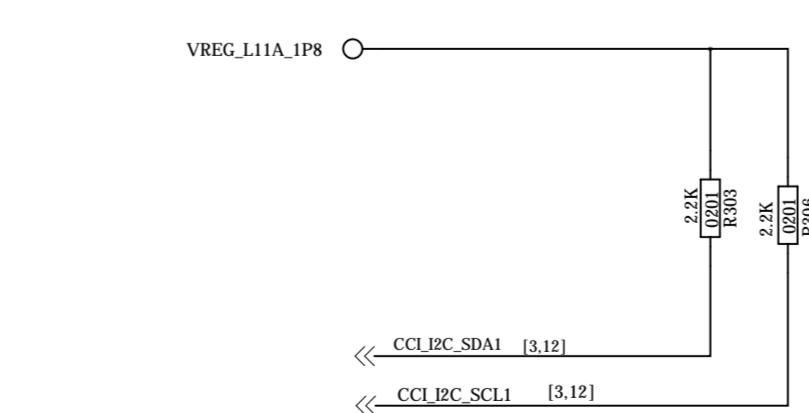
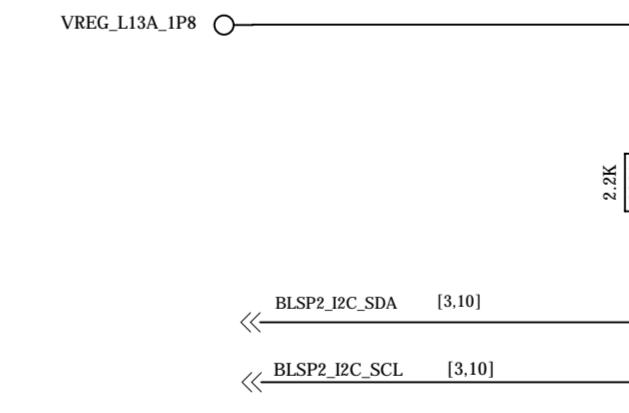
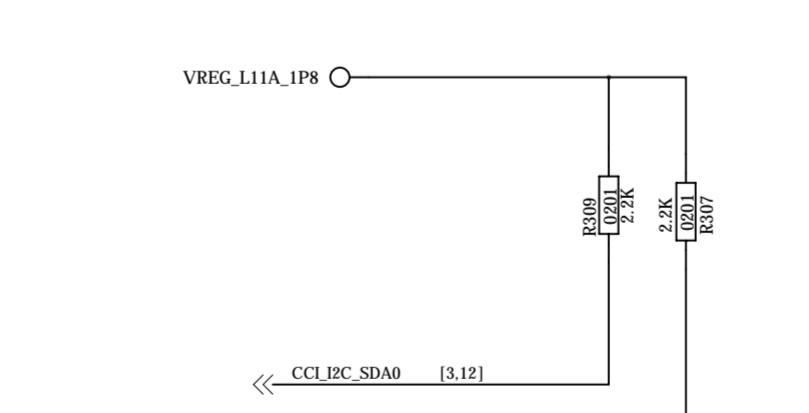
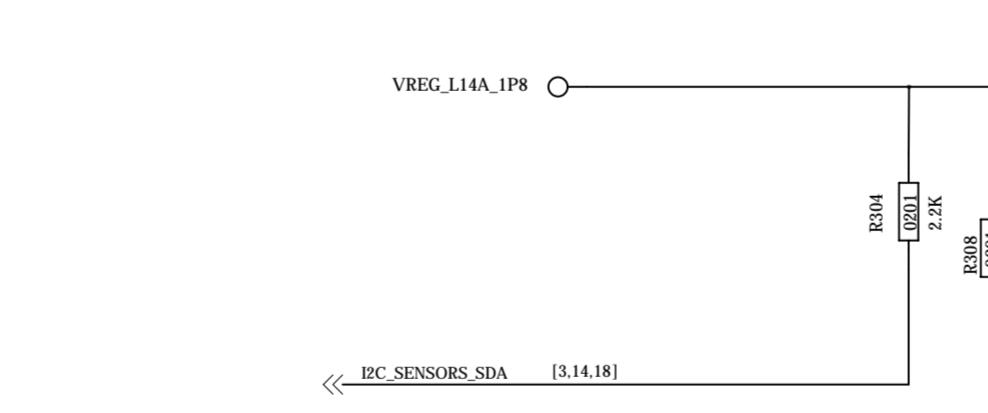
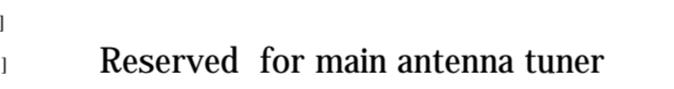
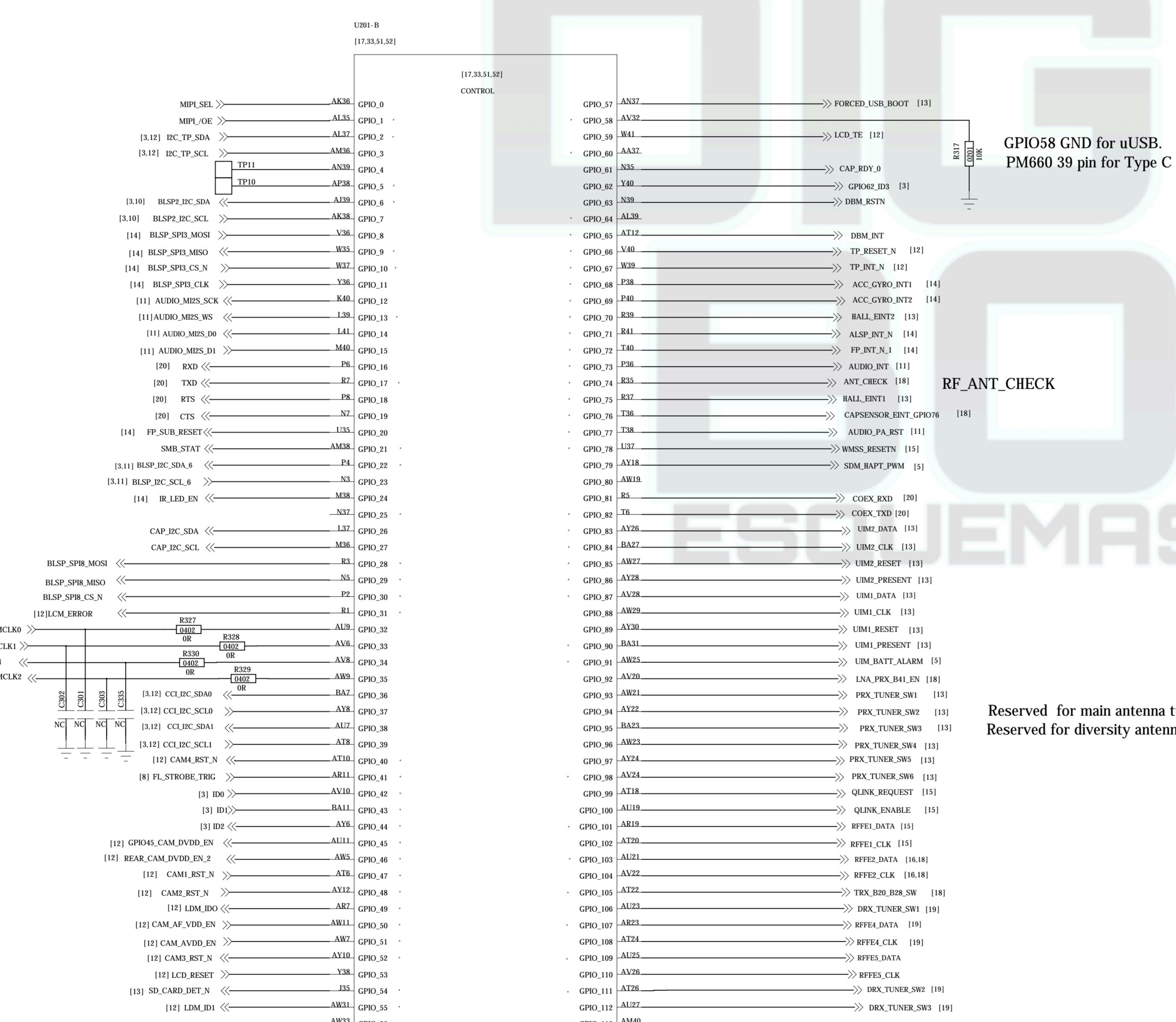
The diagram shows a U201-J integrated circuit (IC) package with 24 pins. The pins are labeled as follows:

Pin	Label
AE1	GND_1
BA33	GND_2
AM14	GND_3
F10	GND_4
F12	GND_5
F16	GND_6
F18	GND_7
Y28	GND_8
Y34	GND_9
M6	GND_10
M8	GND_11
U9	GND_12
BA37	GND_13
L5	GND_14
H8	GND_15
F36	GND_16
F38	GND_17
F4	GND_18
F6	GND_19
C21	GND_20
C27	GND_21
C29	GND_22
C3	GND_23
BA41	GND_24

Below the IC package, there is a vertical column of labels representing the connections to the pins:

- [17,33,51,52] CONTROL
- GND_51 U1
- GND_52 U41
- GND_53 U7
- GND_54 V12
- GND_55 V14
- GND_56 V18
- GND_57 C13
- GND_58 V20
- GND_59 V22
- GND_60 V24
- GND_61 V26
- GND_62 V28
- GND_63 V30
- GND_64 V32
- GND_65 V8
- GND_66 W9
- GND_67 Y14
- GND_68 C15
- GND_69 Y20
- GND_70 Y22
- GND_71 Y24
- GND_72 Y26
- GND_73 P14
- GND_74 P16

At the top left of the image, there are two small text labels: "CLK [5,8]" and "DATA [5,8]".

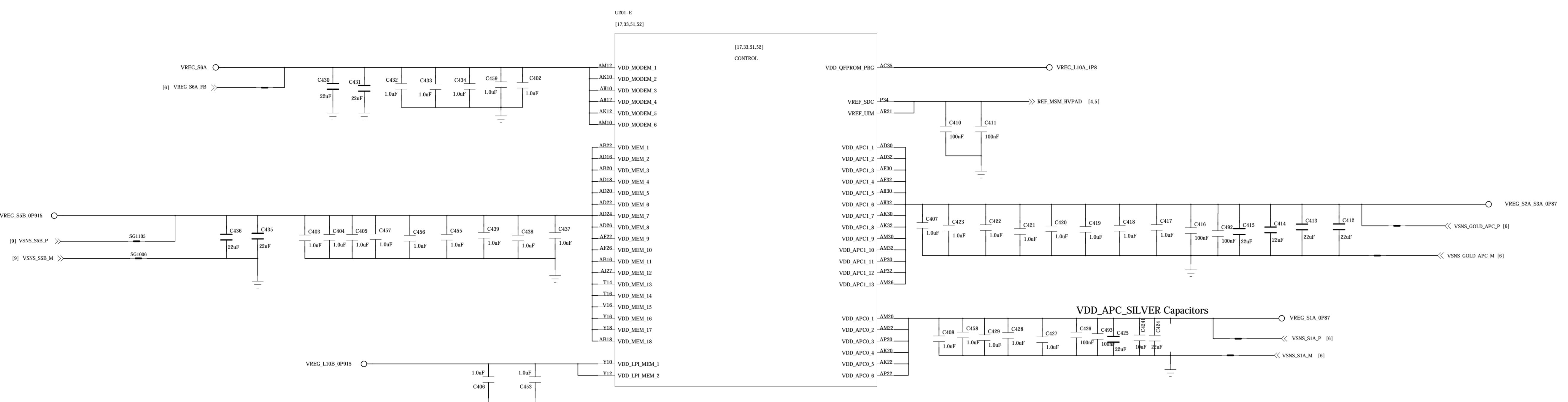


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The diagram illustrates a power supply network for a digital signal processing chip, showing various voltage rails and their connections to regulators and capacitors.

Voltage Rails:

- VDD_P1:** Connected to H24 and VREG_S1B_1P125.
- VDD_P2:** Connected to K34 and VREG_L2B_SDC2. It also connects to C478 and C479, which are connected to ground.
- VDD_P3_1:** Connected to AD8 and VREG_L13A_1P8. It connects to C475, C476, C477, C474, C481, C482, and C483, which are connected to ground.
- VDD_P3_10:** Connected to K32.
- VDD_P3_2:** Connected to AF8.
- VDD_P3_3:** Connected to AP8.
- VDD_P3_4:** Connected to AP36.
- VDD_P3_5:** Connected to V34.
- VDD_P3_6:** Connected to AR13.
- VDD_P3_7:** Connected to AR37.
- VDD_P3_8:** Connected to Y8.
- VDD_P3_9:** Connected to H32.

Regulators:

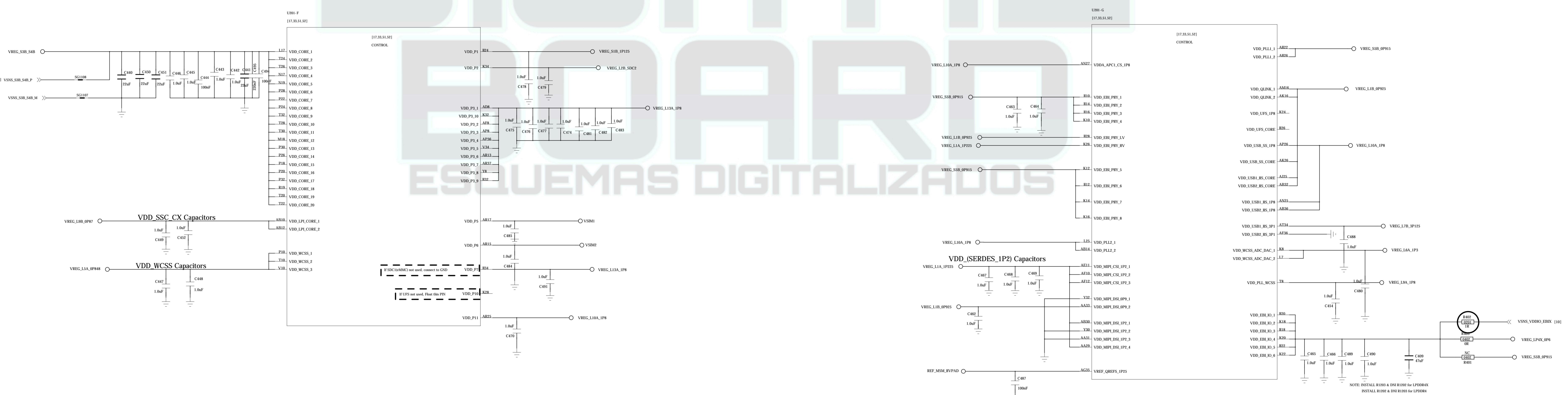
- VREG_S1B_1P125**: Regulates the VDD_P1 rail.
- VREG_L2B_SDC2**: Regulates the VDD_P2 rail.
- VREG_L13A_1P8**: Regulates the VDD_P3_1 rail.
- VREG_L10A_1P8**: Regulates the VREG_L10A_1P8 rail.
- VREG_S5B_0P915**: Regulates the VREG_S5B_0P915 rail.
- VREG_L1B_0P925**: Regulates the VREG_L1B_0P925 rail.
- VREG_L1A_1P225**: Regulates the VREG_L1A_1P225 rail.
- VREG_S5B_0P915**: Regulates the second VREG_S5B_0P915 rail.

Capacitors:

- Decoupling capacitors (1.0uF) are placed between the VDD_P2 and VDD_P3_1 rails and their respective regulators.
- Decoupling capacitors (1.0uF) are placed between the VDD_P3_1 rail and its regulator.
- Decoupling capacitors (1.0uF) are placed between the VREG_S5B_0P915 rail and its regulators.

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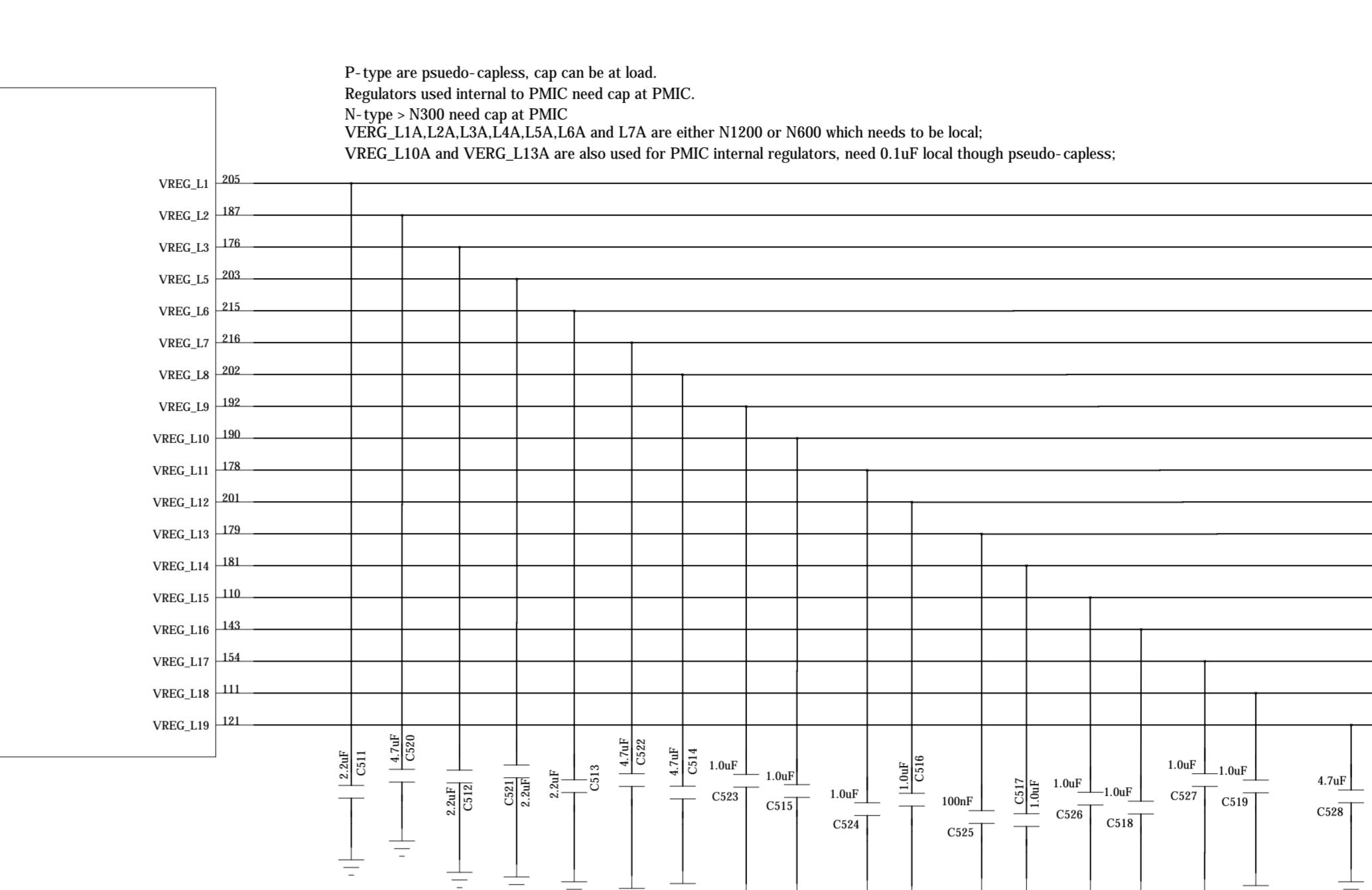
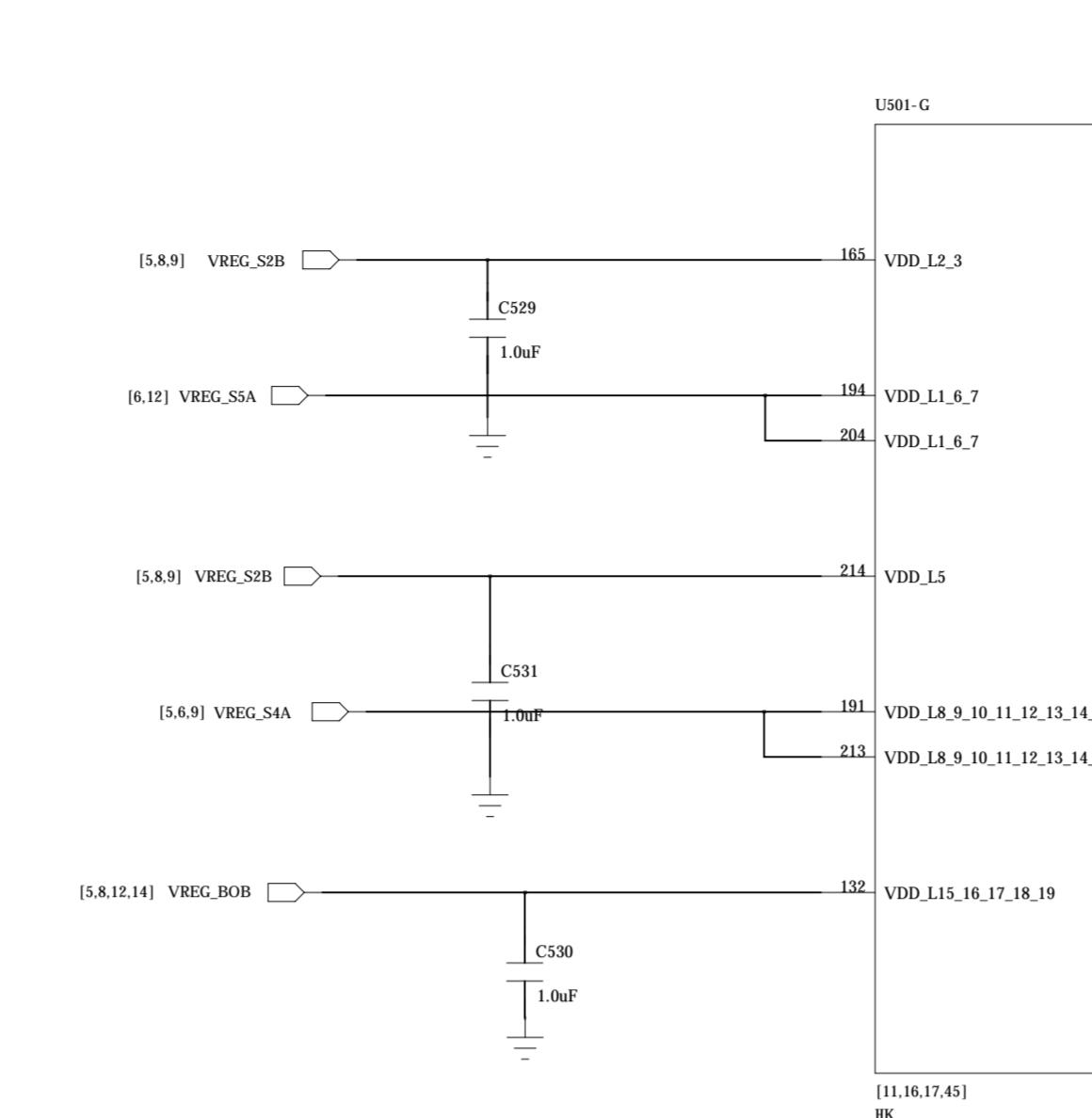
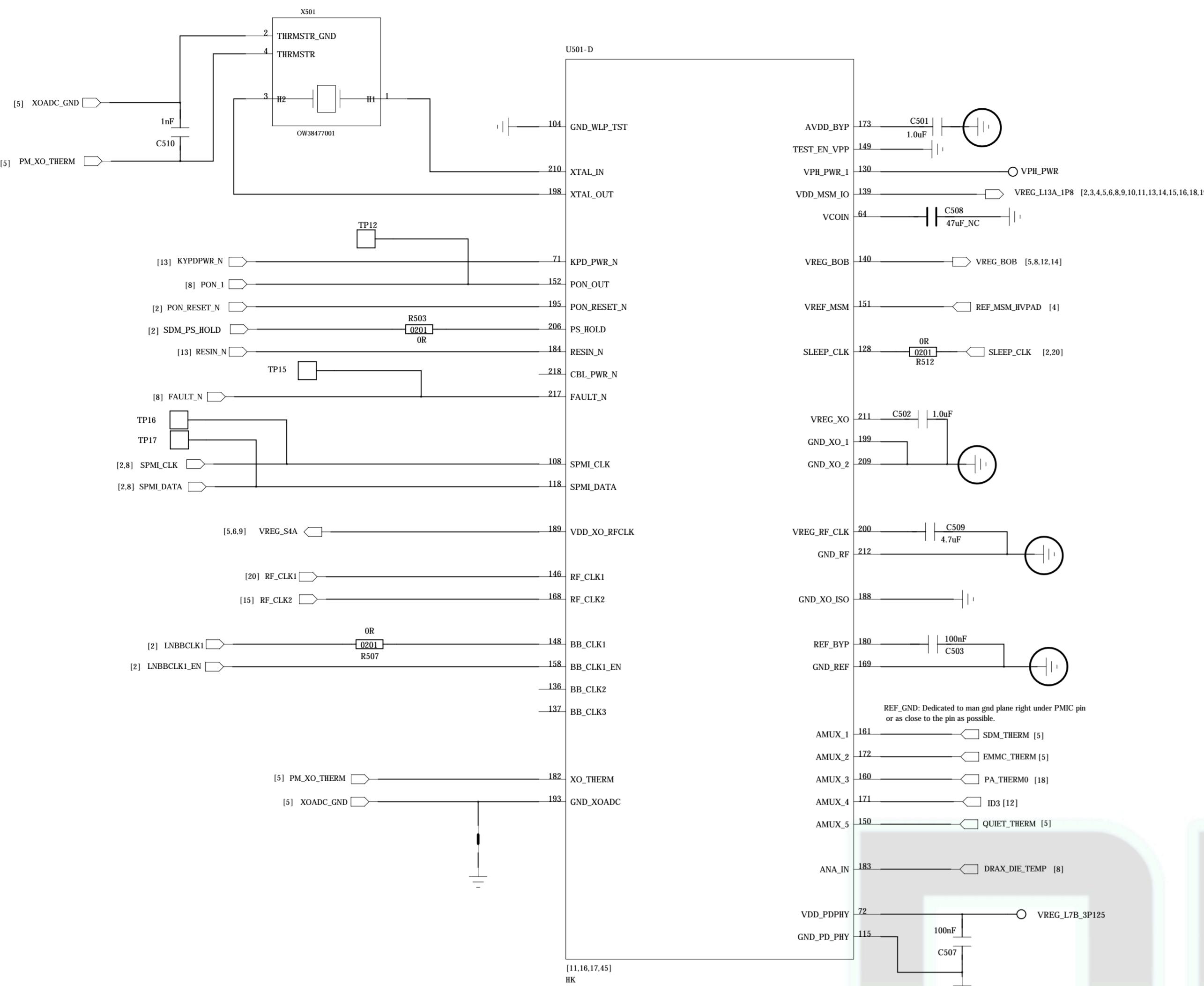
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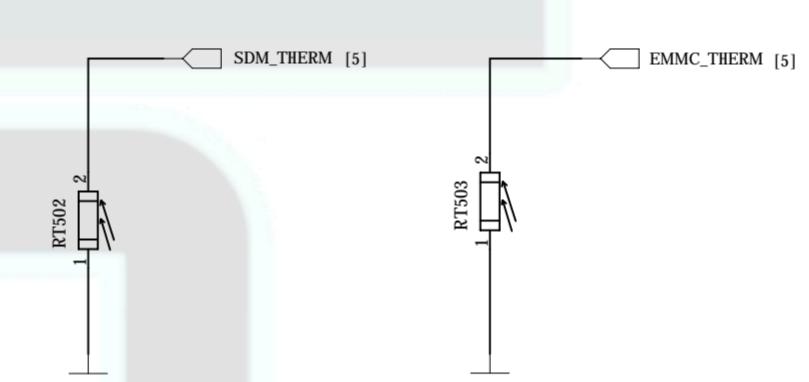
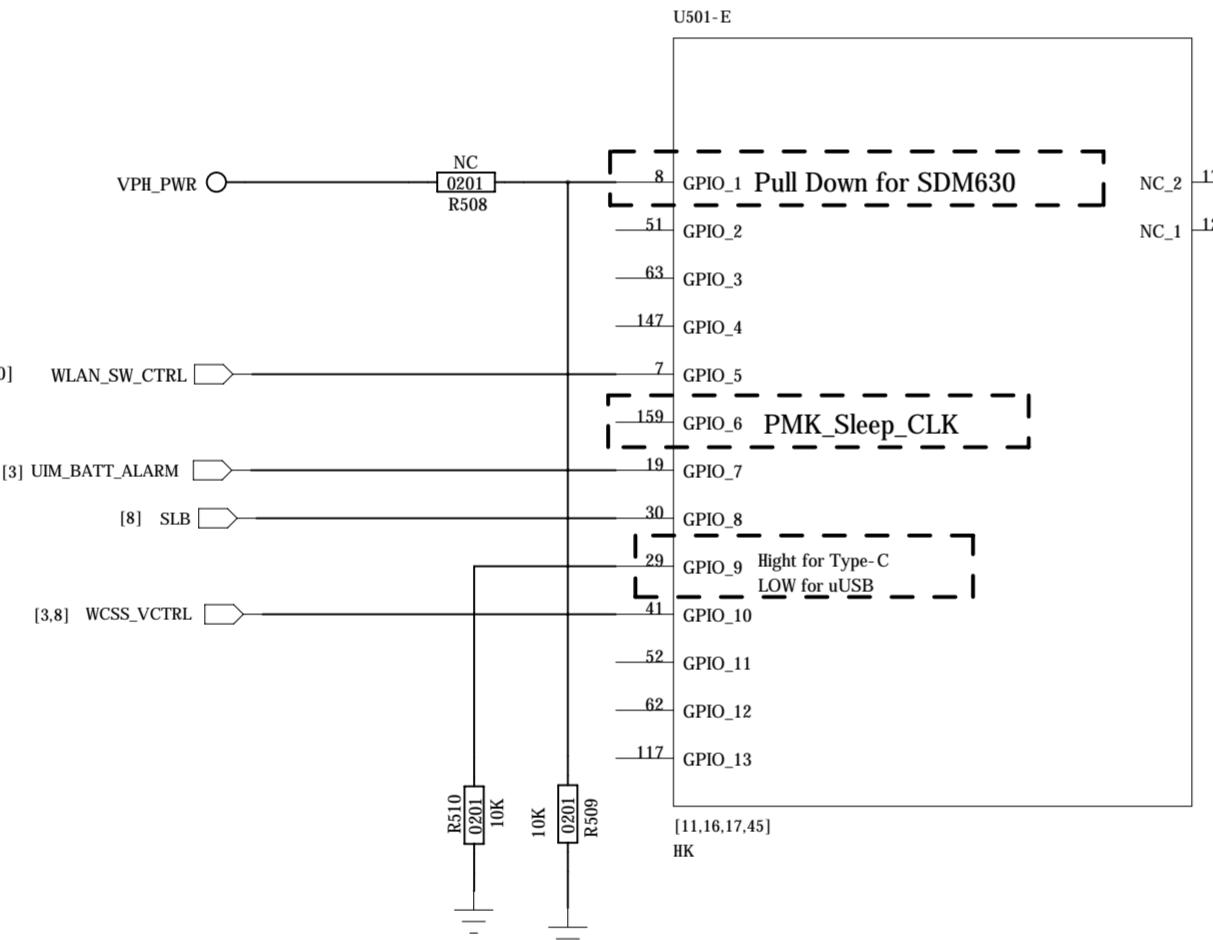
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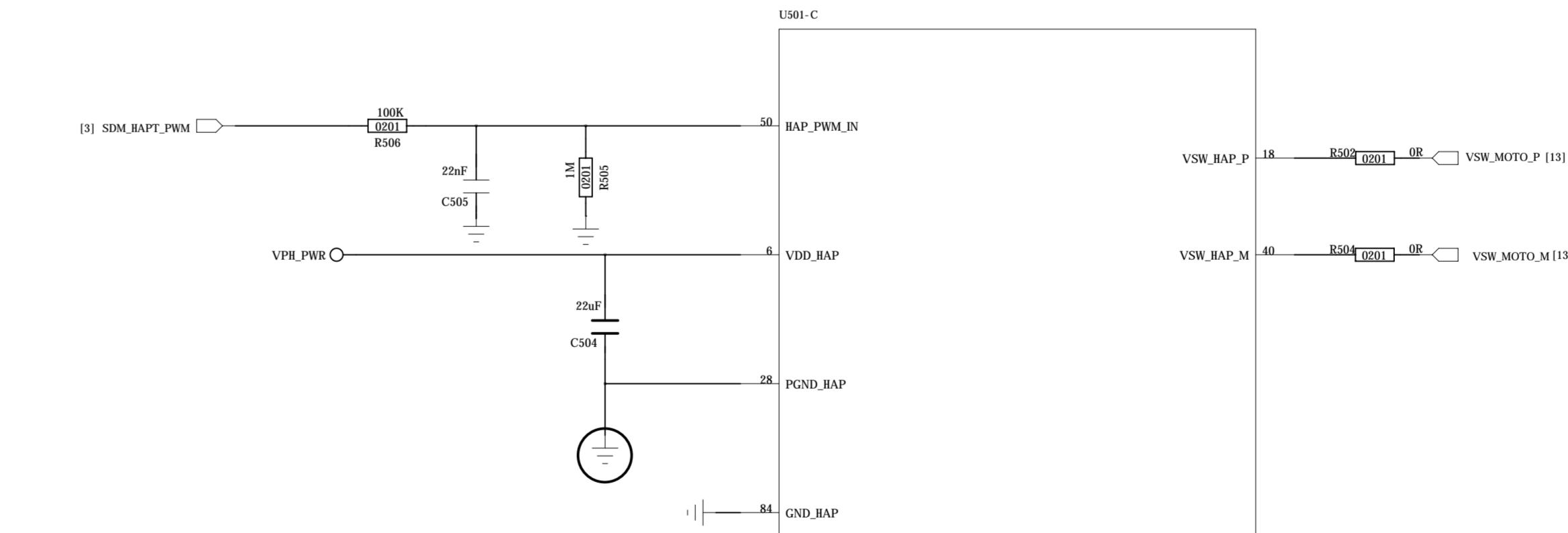
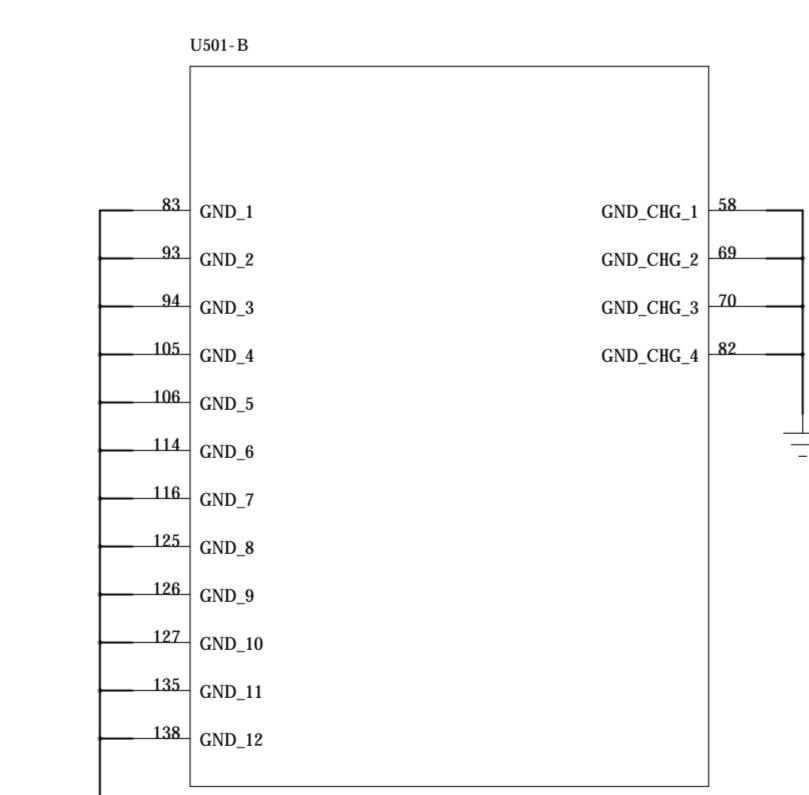
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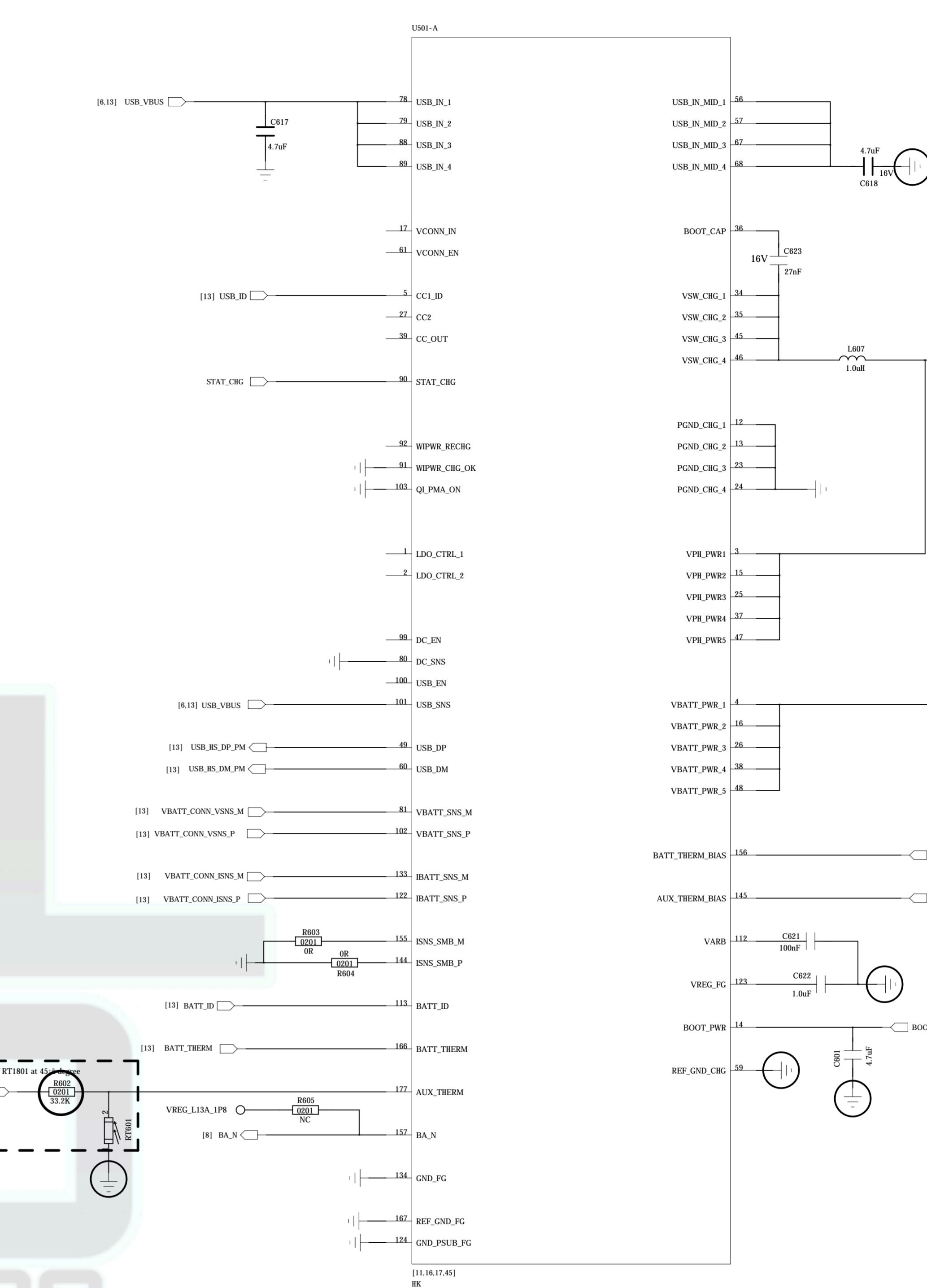
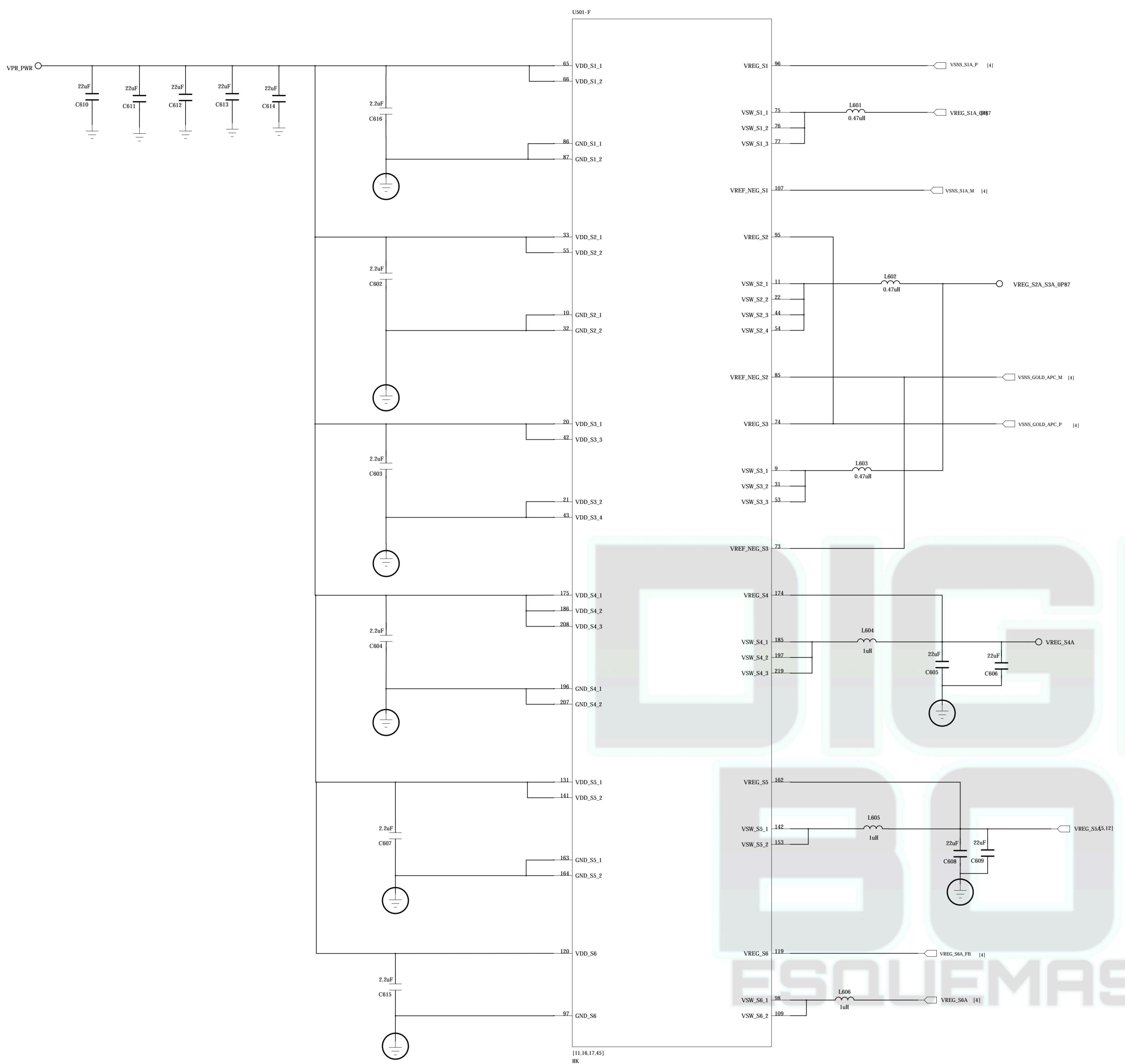


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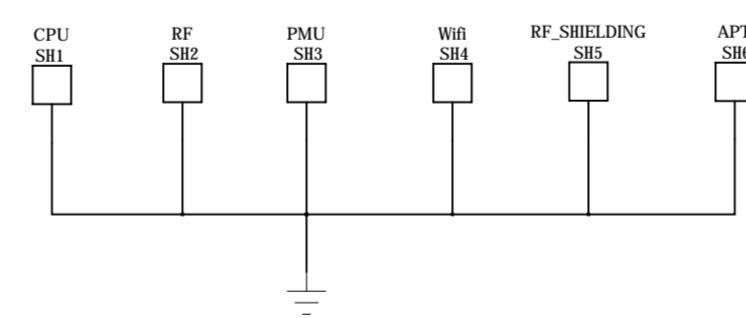
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DIGITAL BOARD

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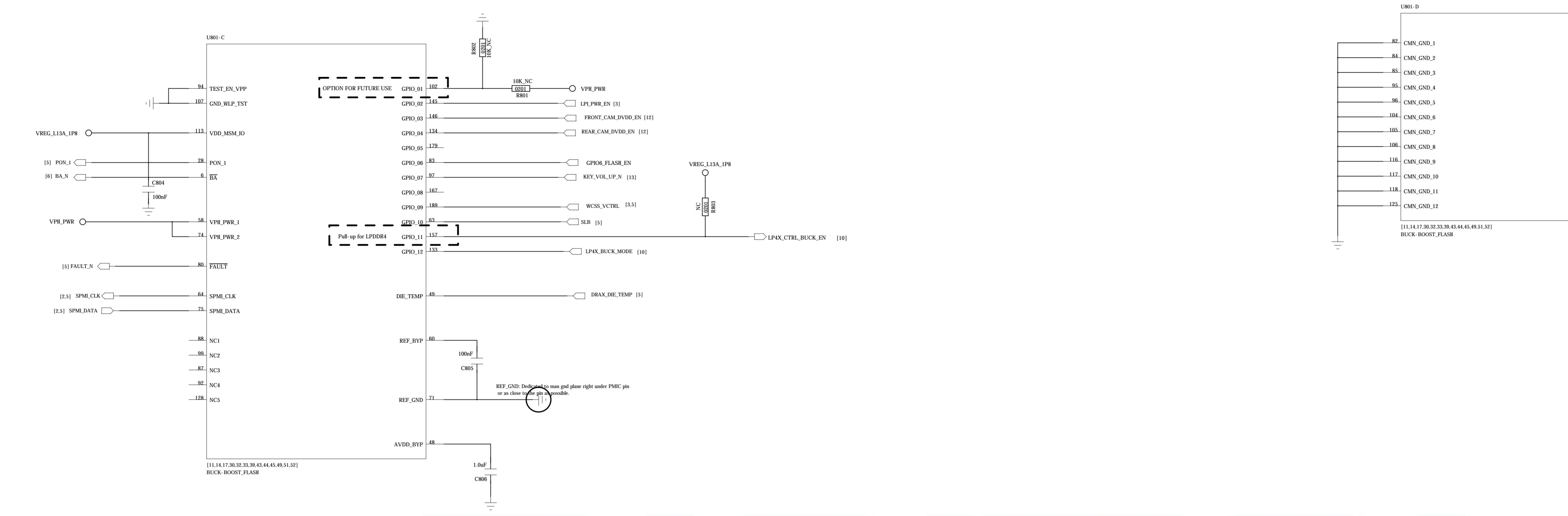
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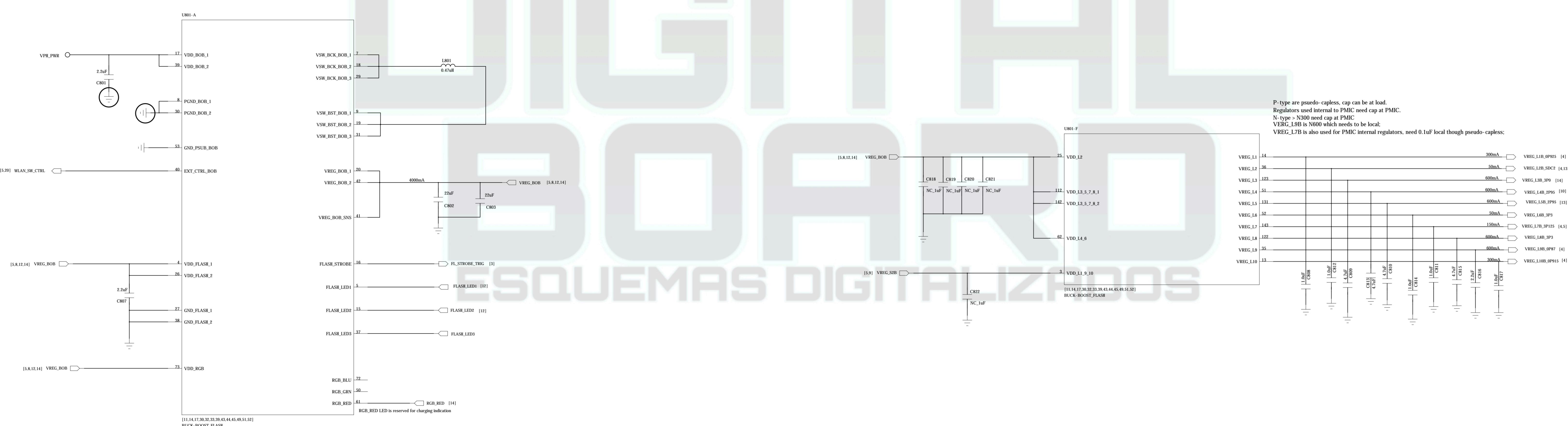
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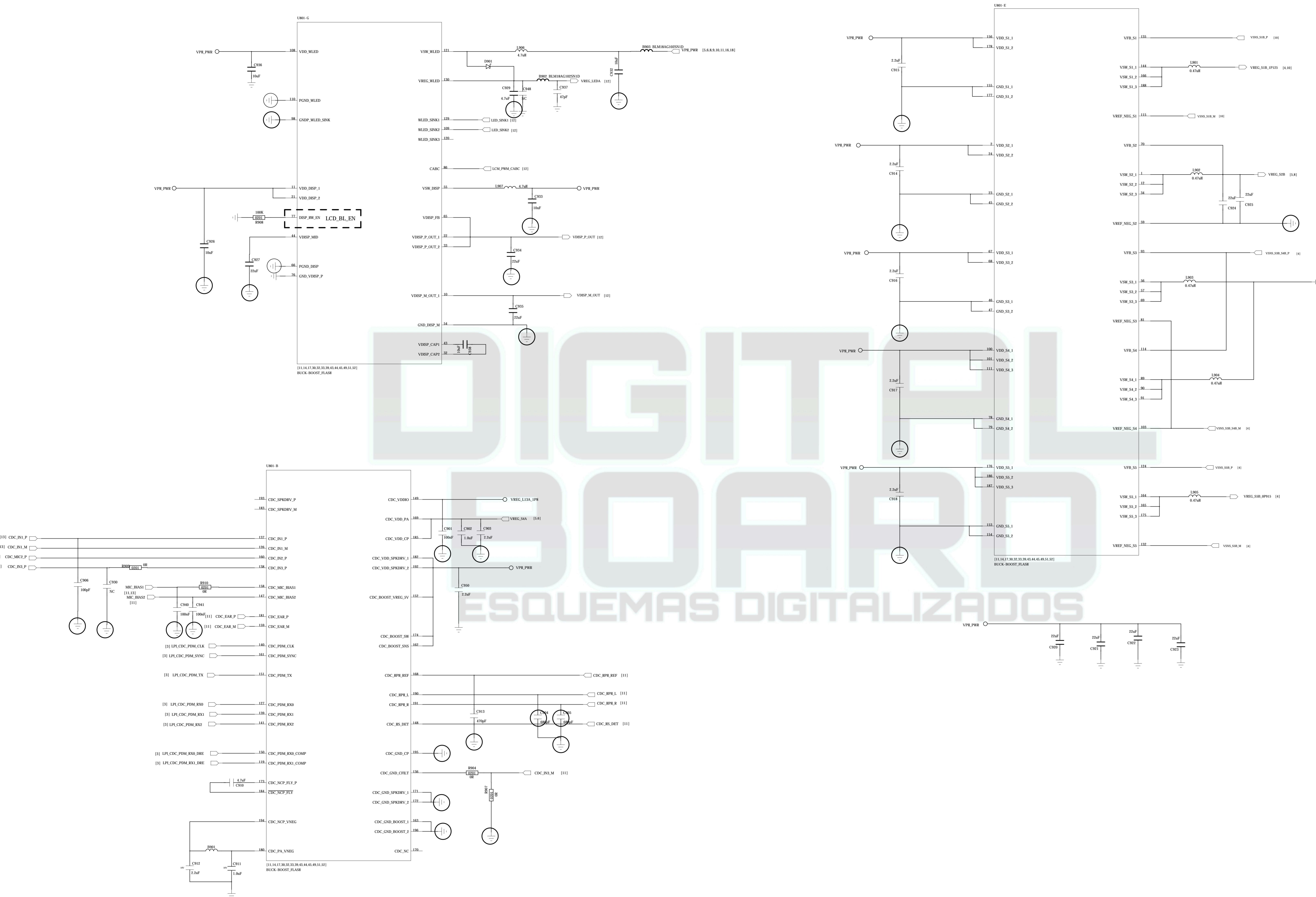
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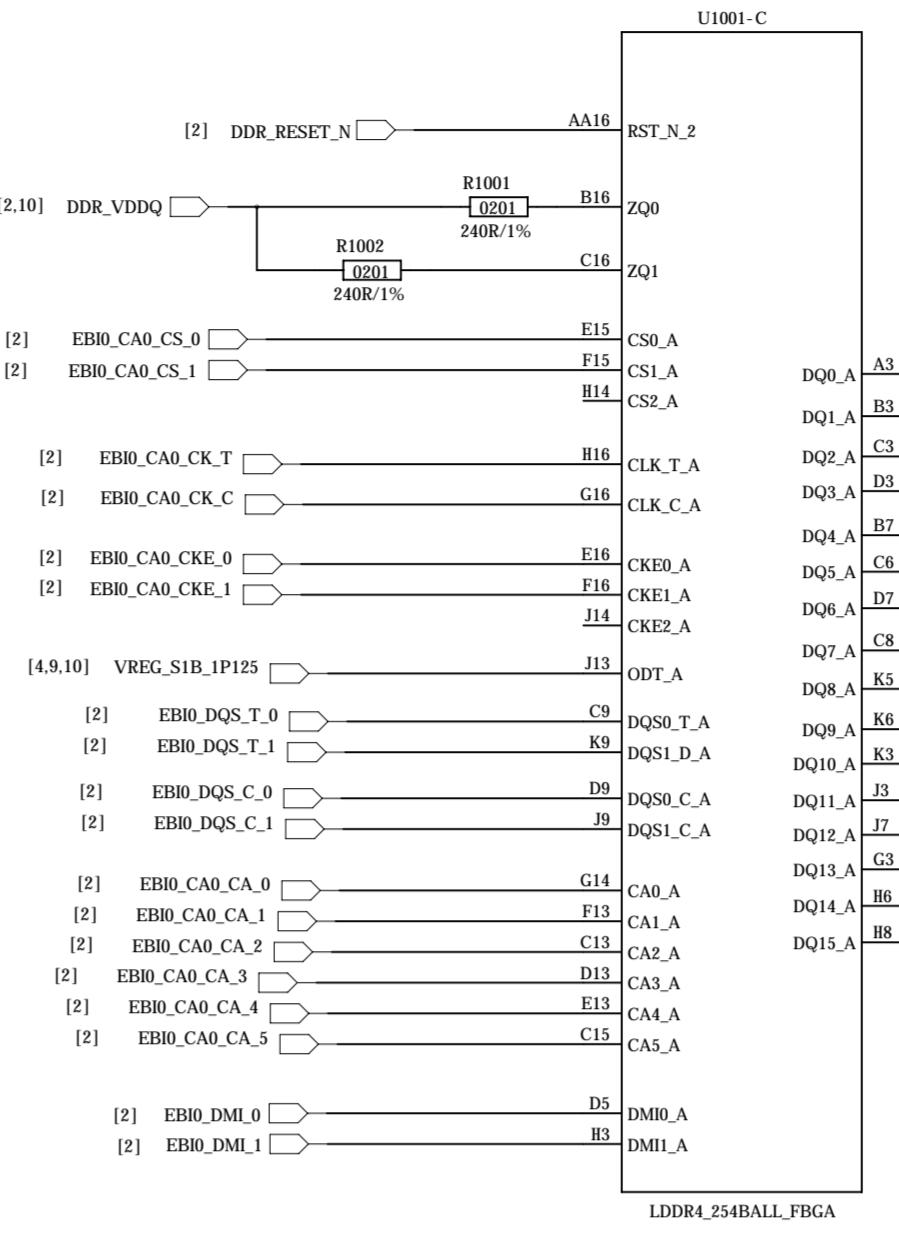
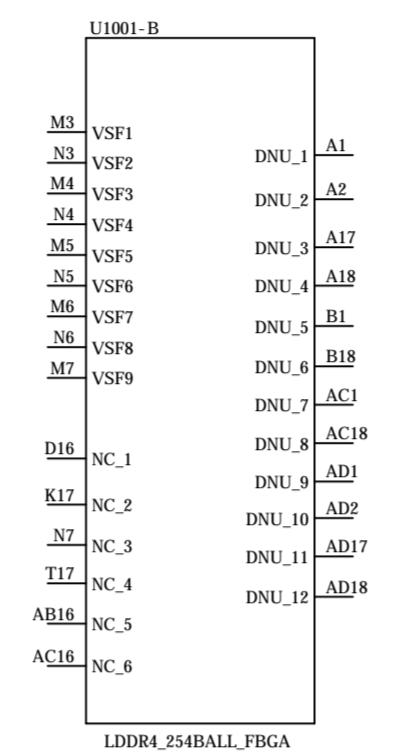
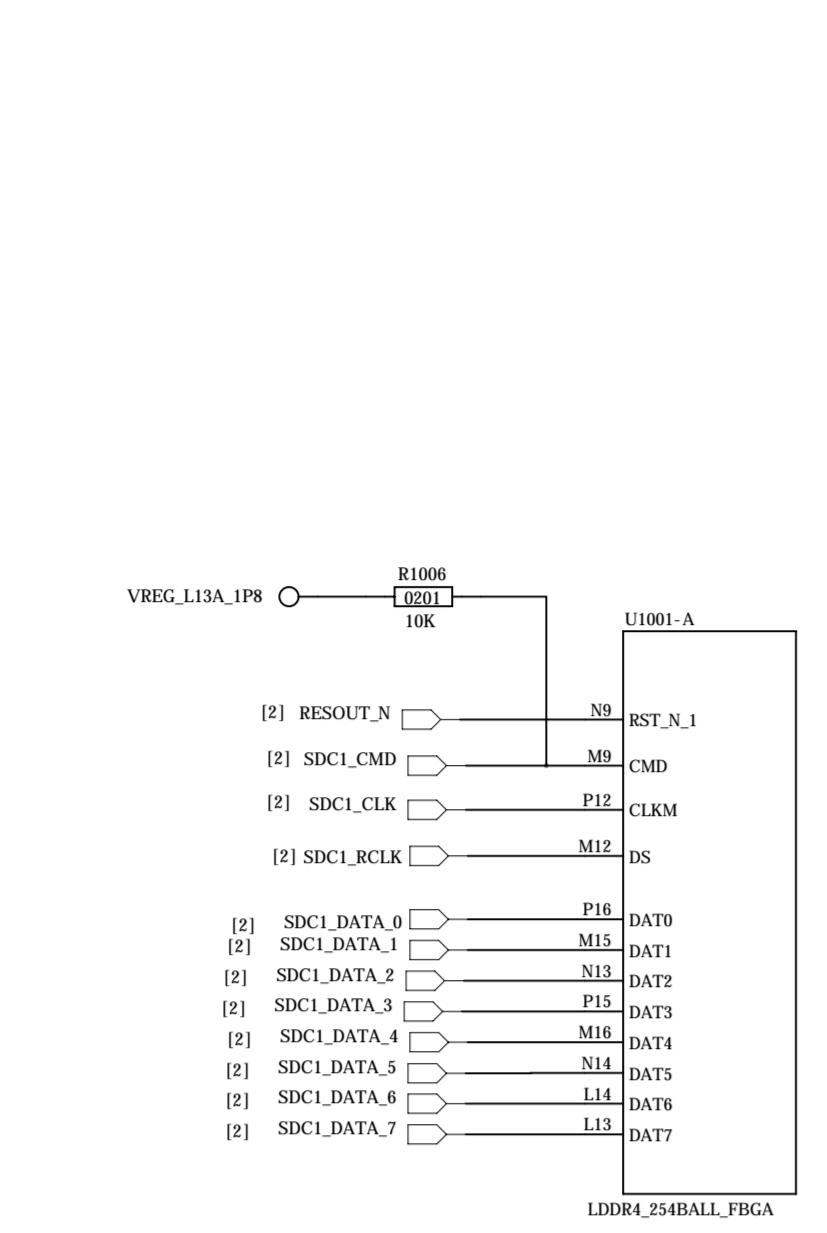


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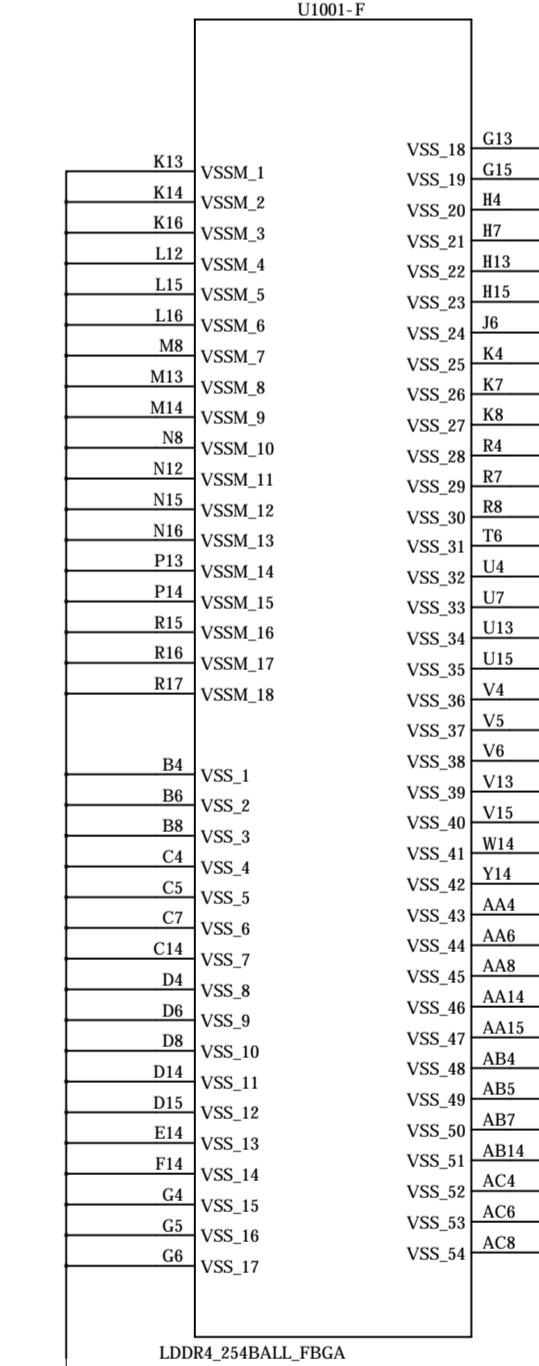
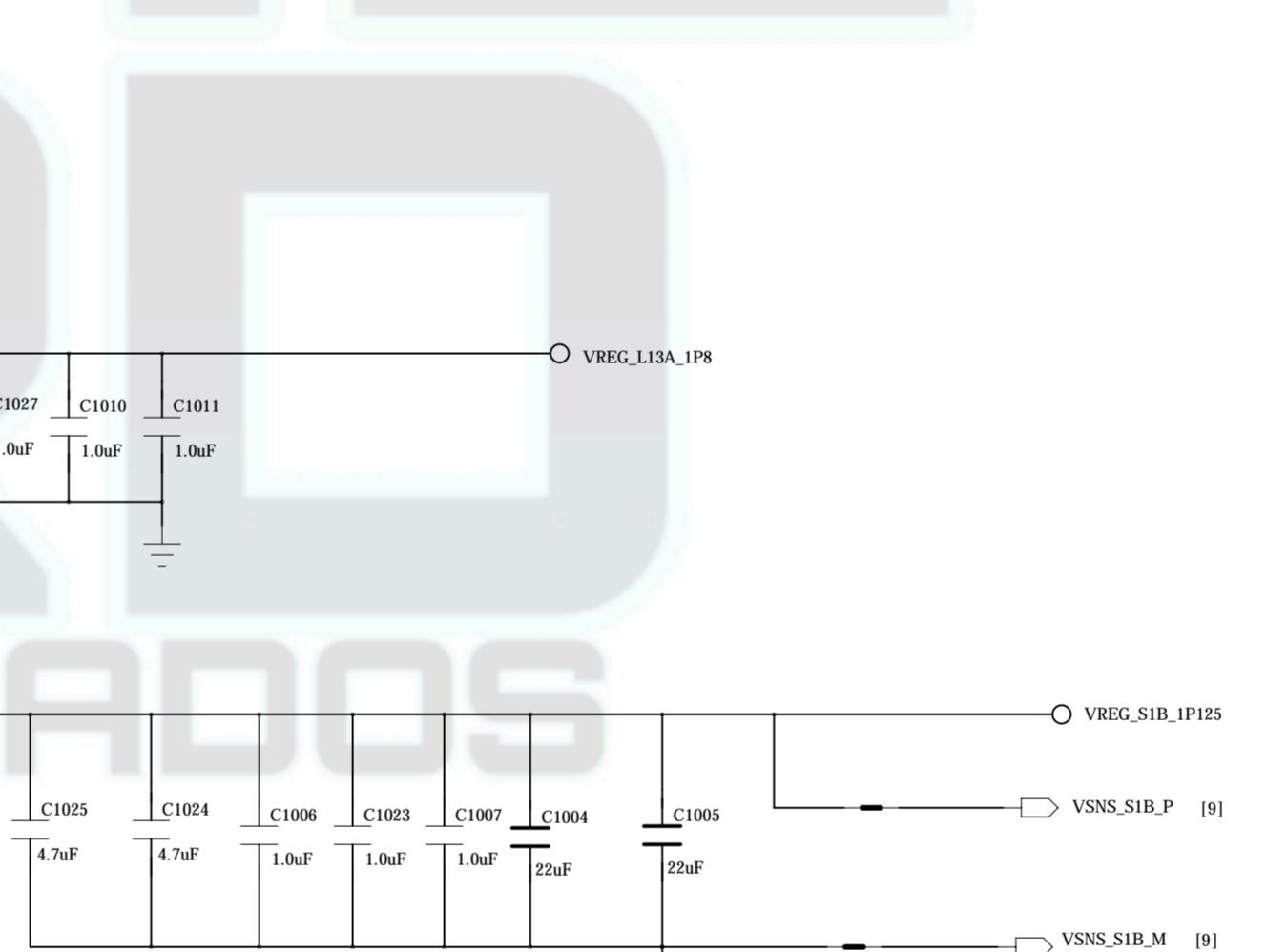
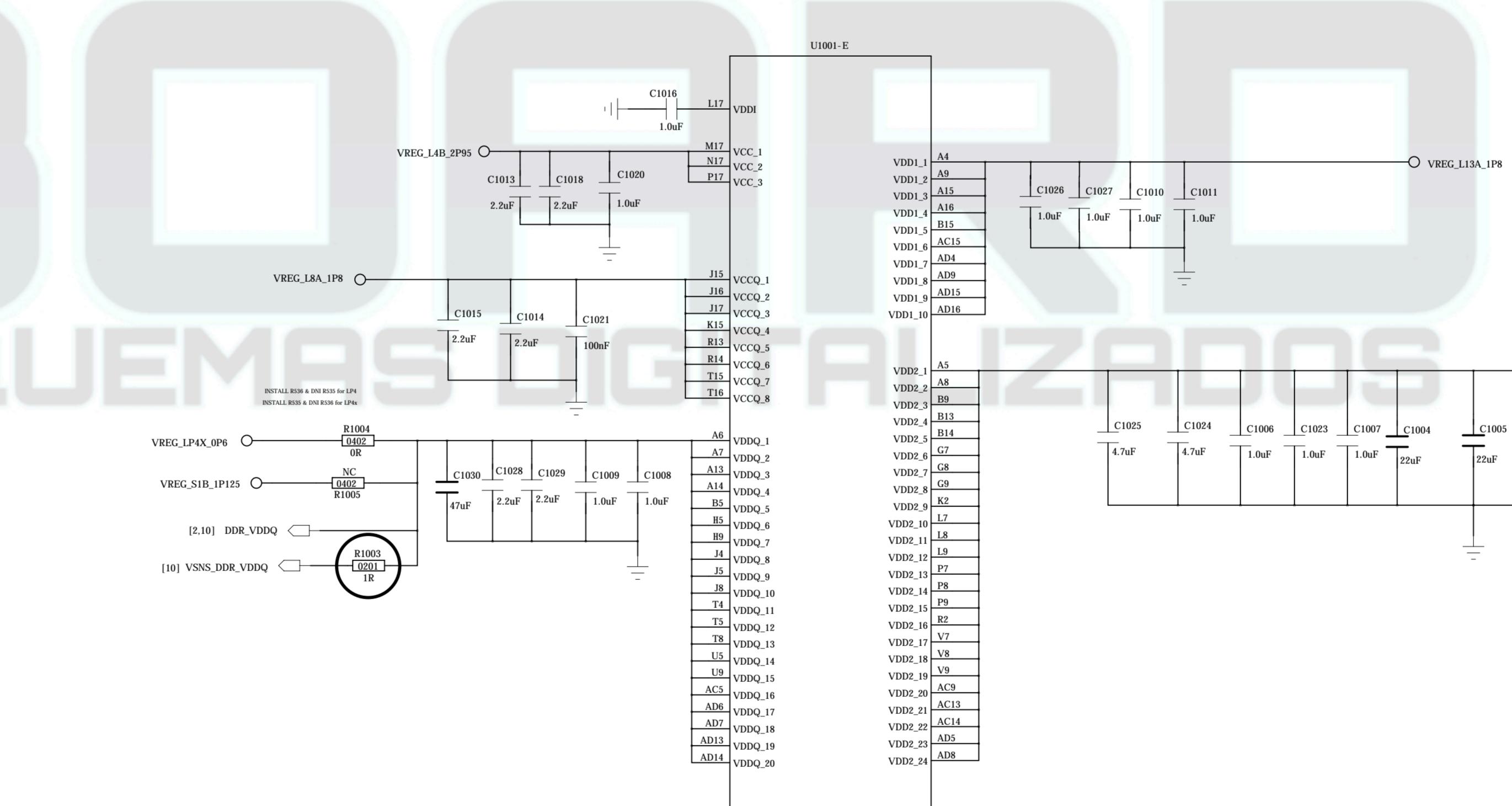
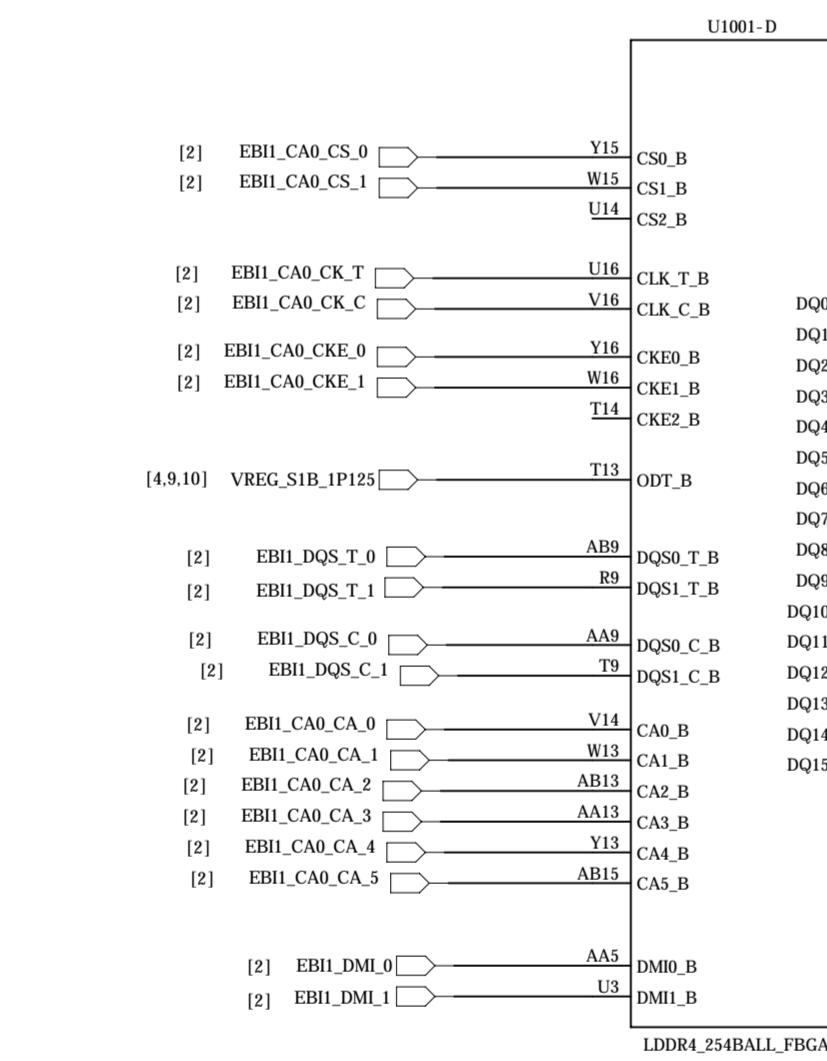
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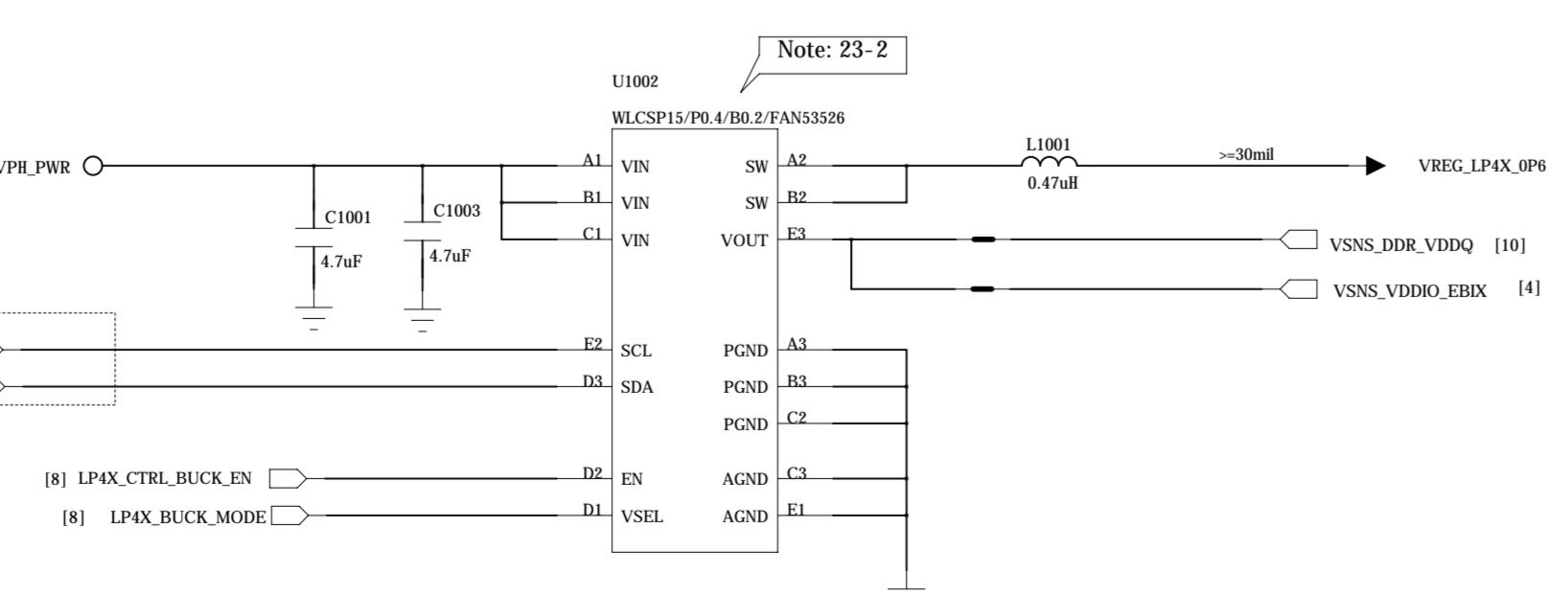


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Buck for VDRAM

FAN53526 / Buck I2C address: 0X60 (Write:0xC0, Read:0xC1)



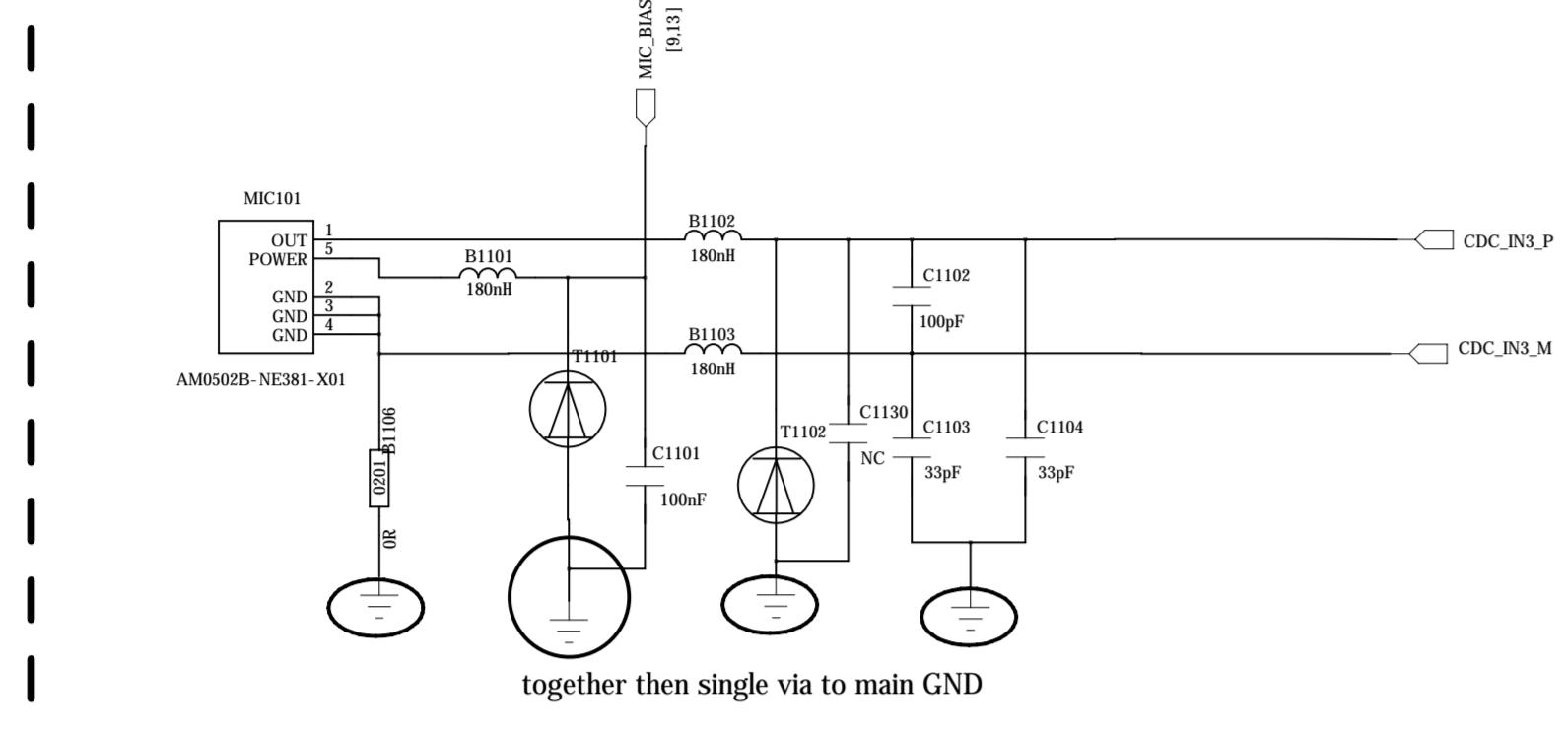
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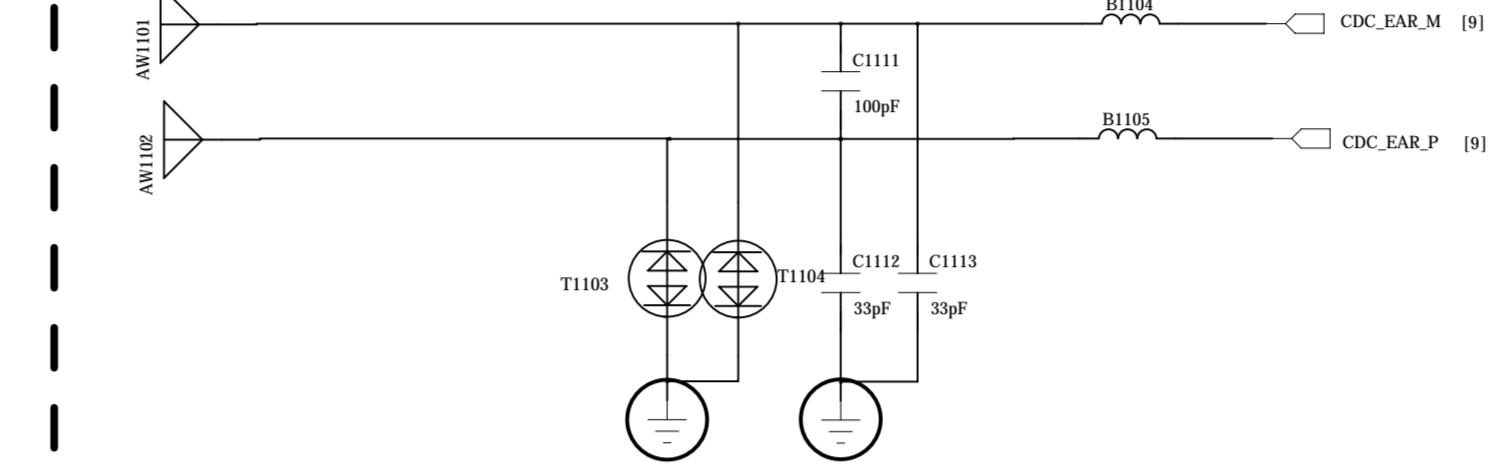
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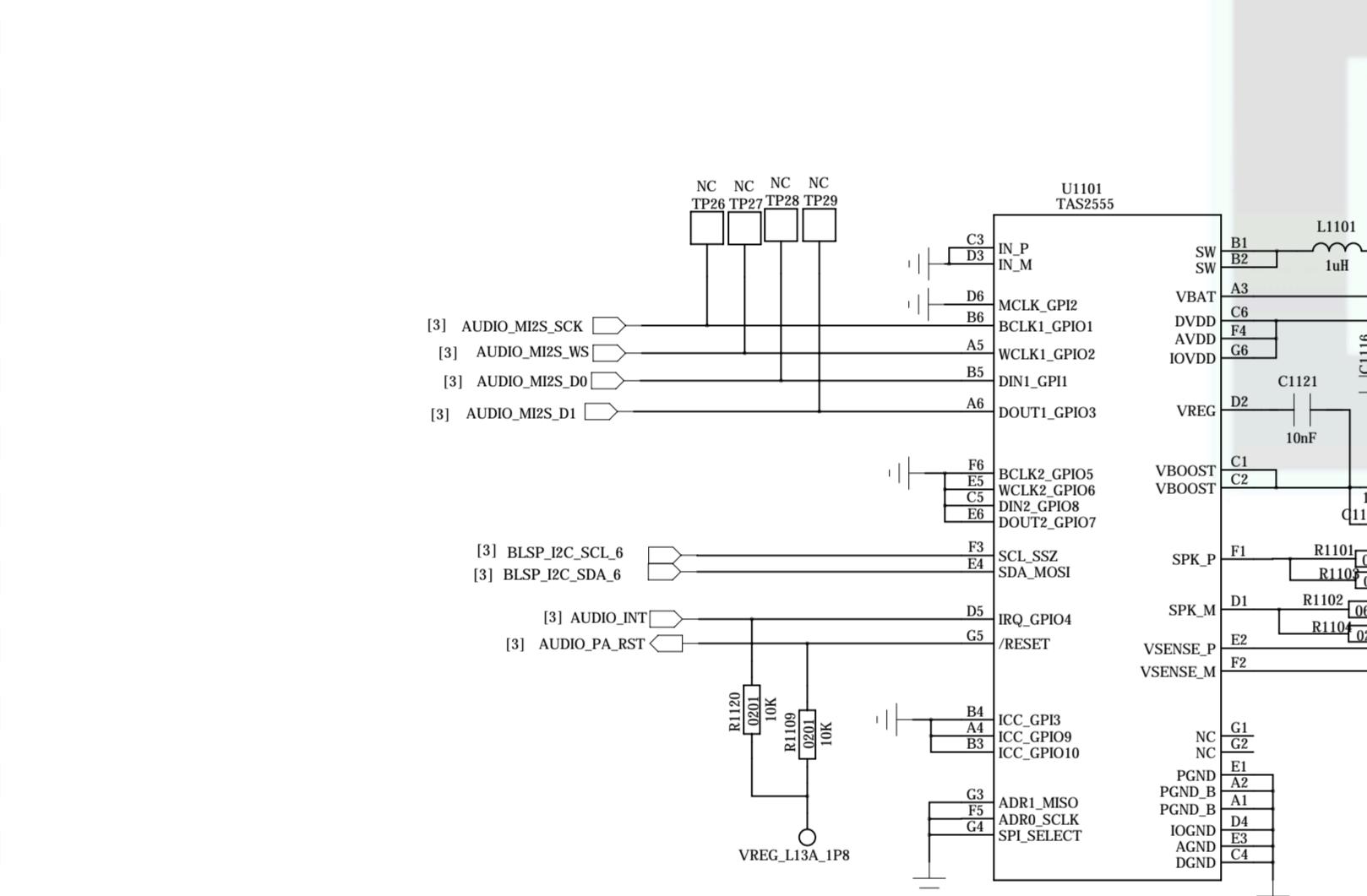
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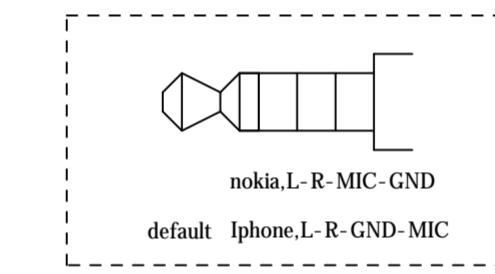
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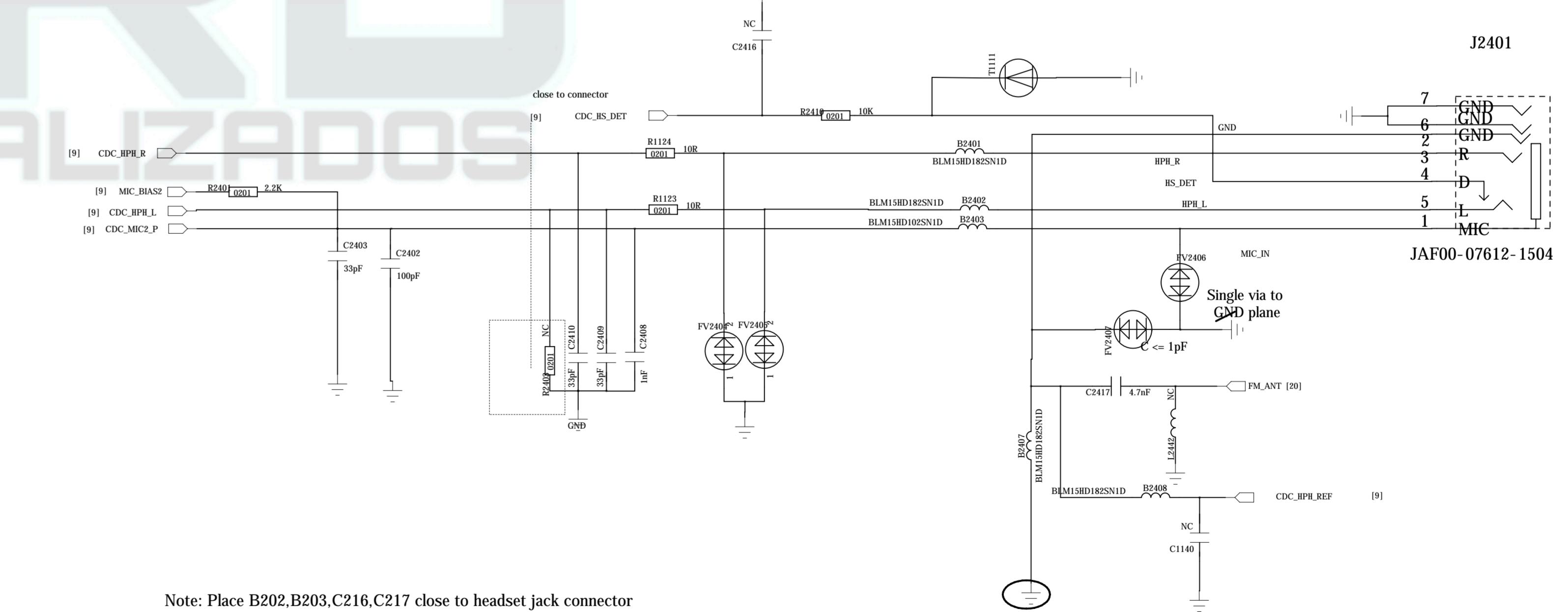
Smart PA



Earphone Audio



Note: Ferrite beads and their corresponding bypass capacitors on
on CDC_HPH_L_P, CDC_HPH_L_M and CDC_HPH_REF
are needed to reduce noise generated by audio/FM concurrency

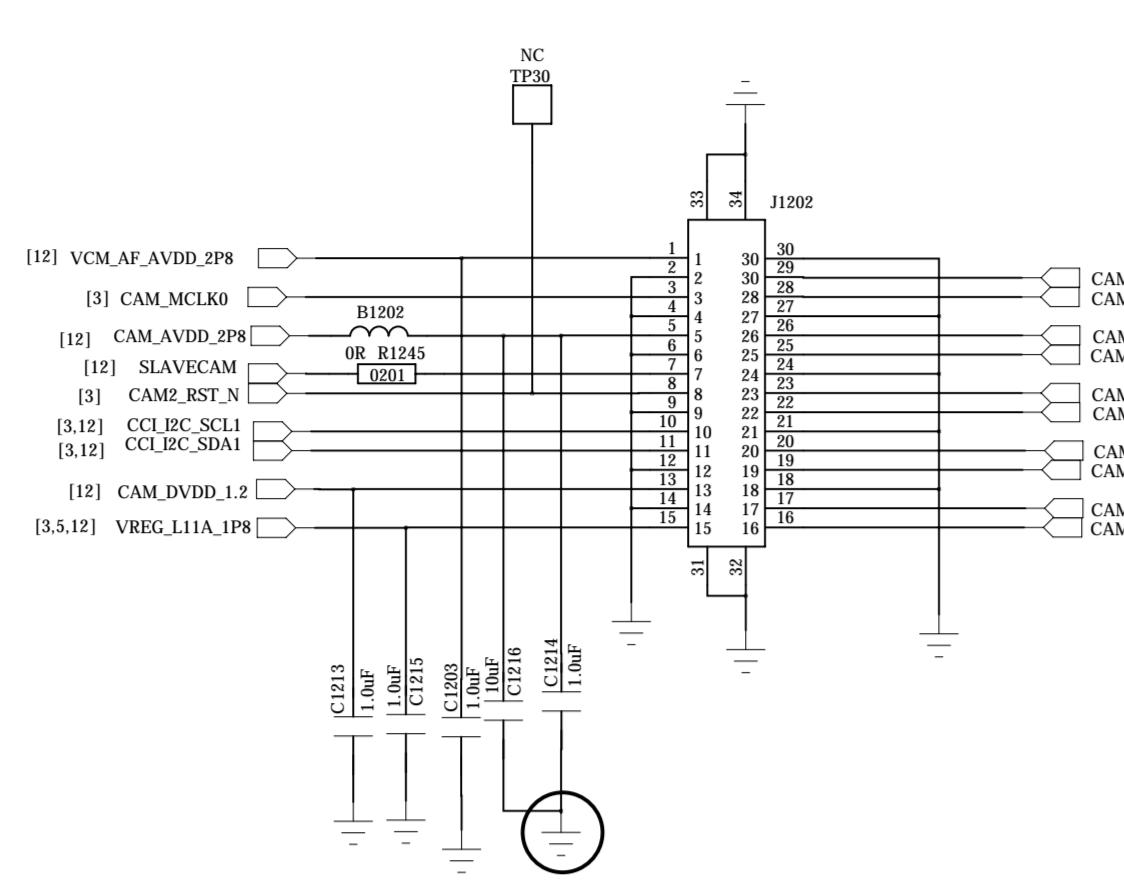


Note: Place B202,B203,C216,C217 close to headset jack connection
Note: For Cable detection

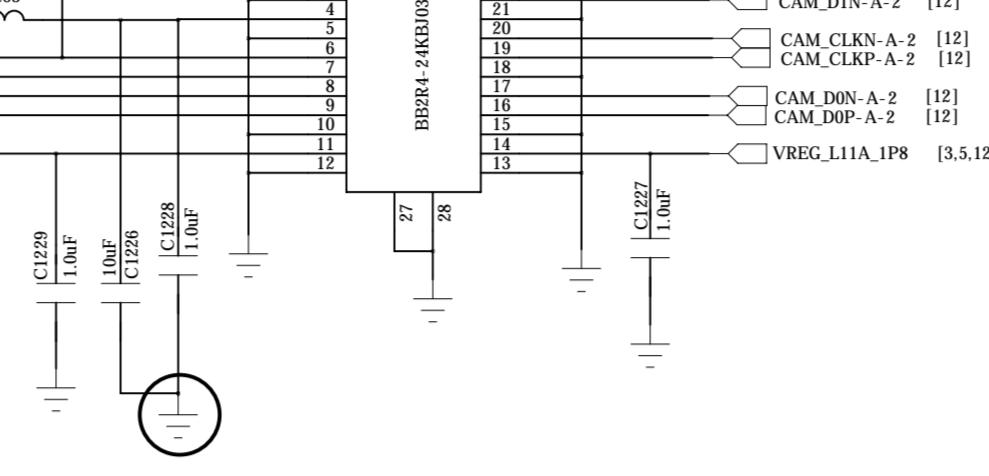
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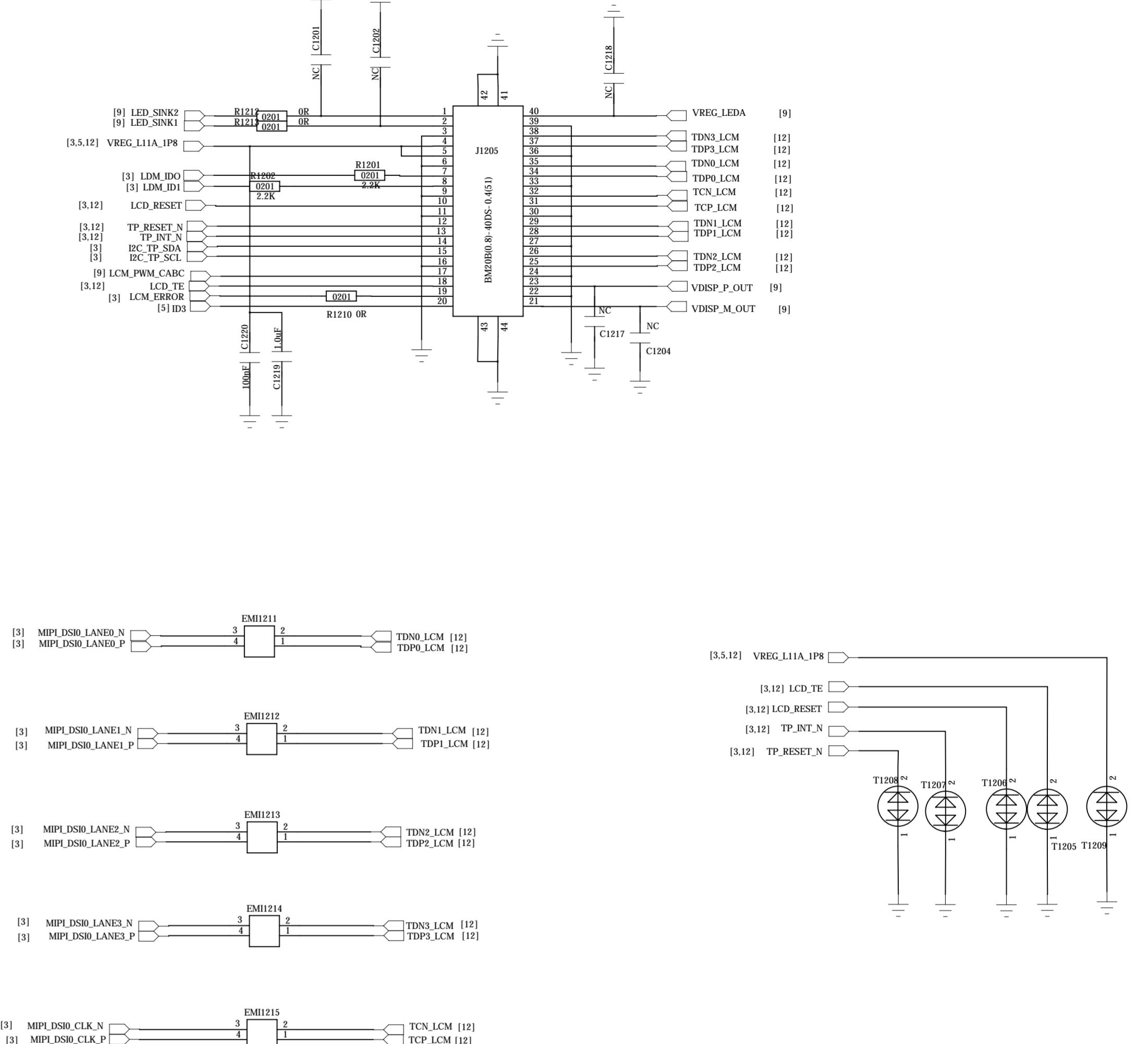
Main Camera A



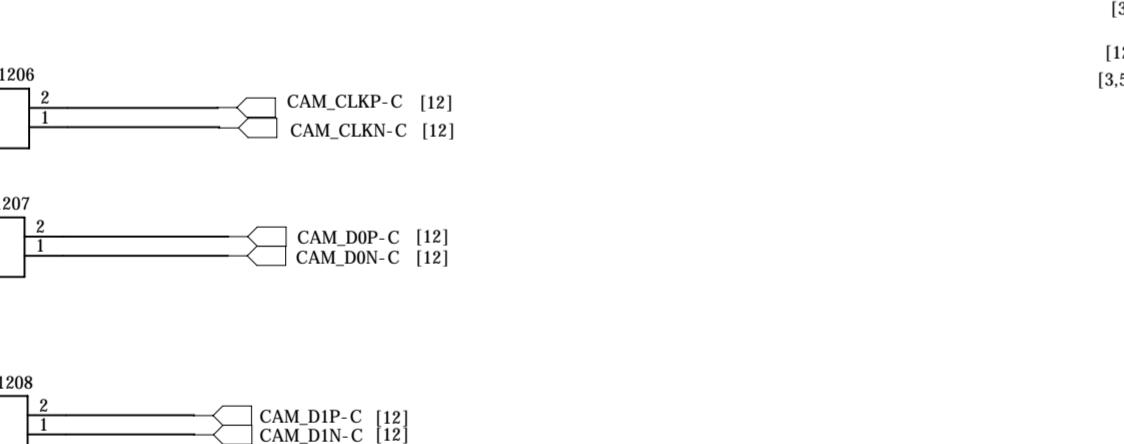
Main Camera B



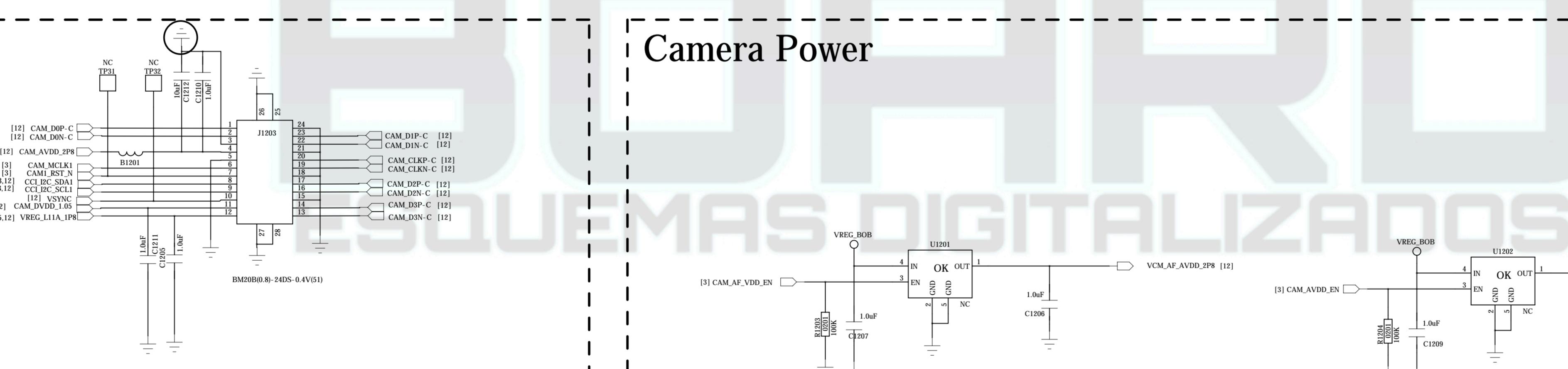
LCM



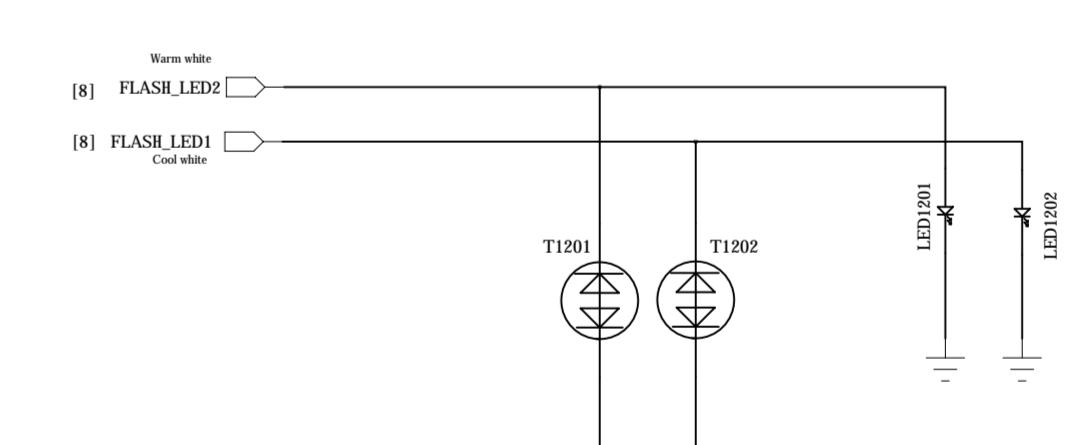
Front Camera_A



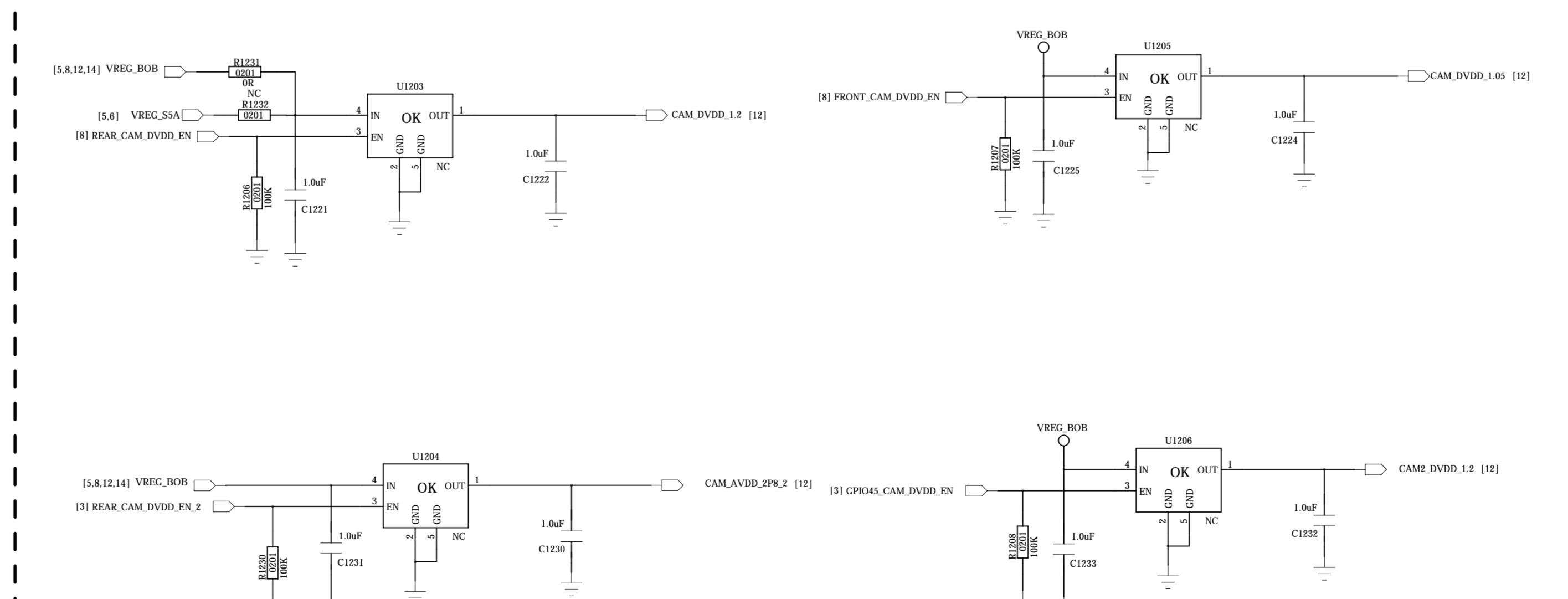
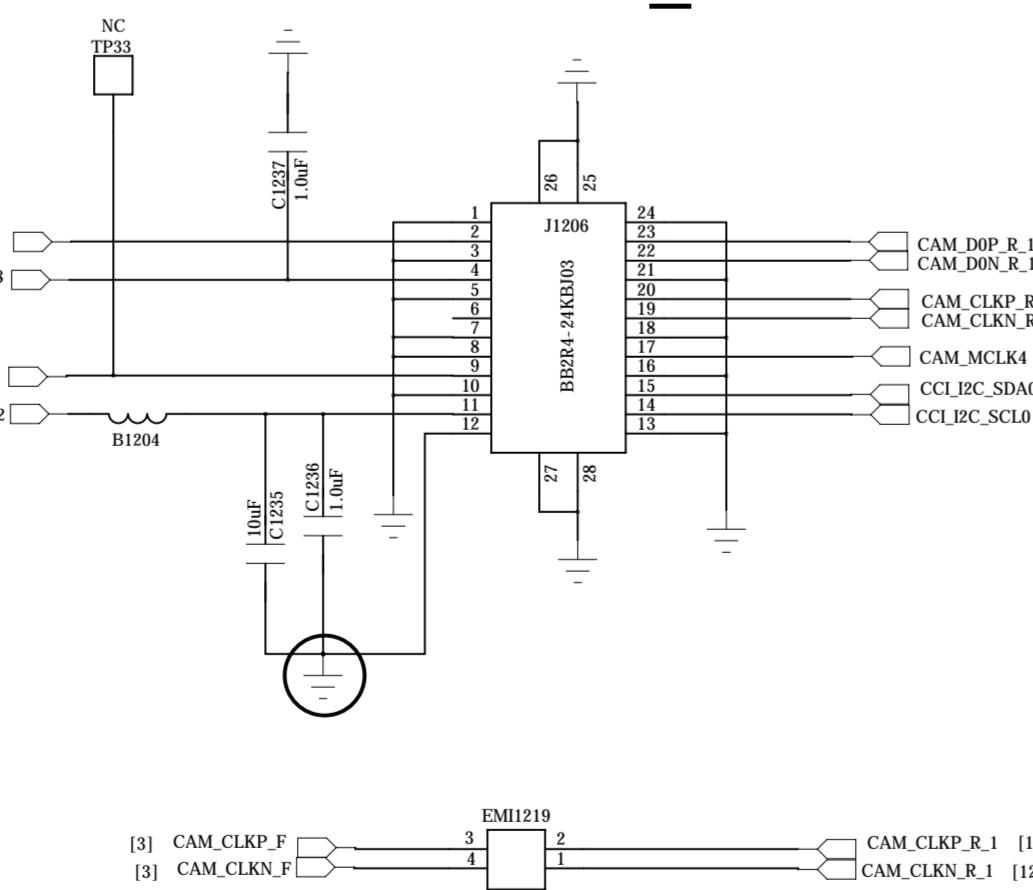
Camera Power



Flash Light



Front Camera_B



Schematic design notice of "63_PERI_CAMERA_KEYPAD" page.

Note 62-1: The VCC of I2C_0 is pulled to "VCAM_IO_PMU"

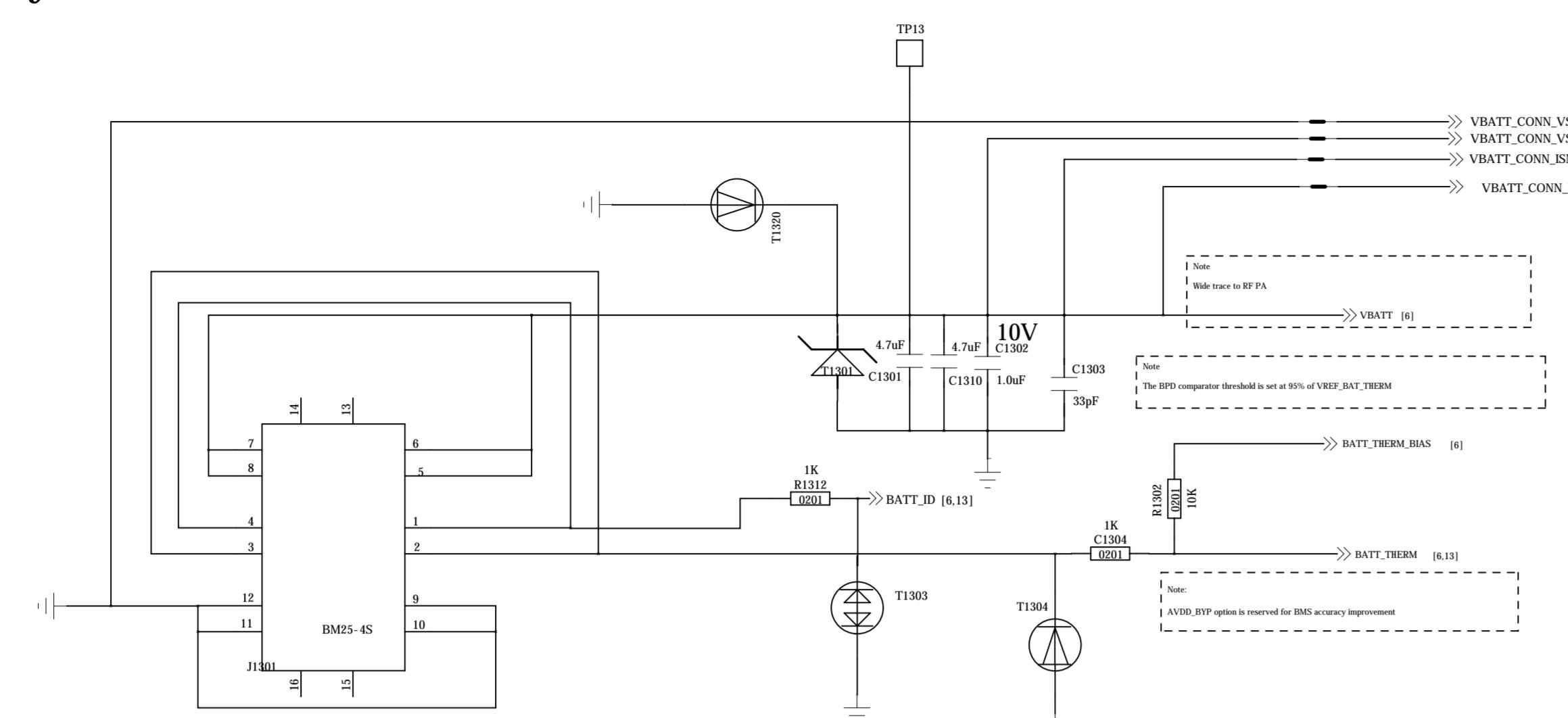
Note 62-2: I2C control interface of front camera (with AF) must be assigned to I2C-2 bus when PIP/VIV feature be supported.

Note 62-3: Reserve a capacitor (27pF) on camera's MCLK and shunt it to GND to prevent GPS de-sense.

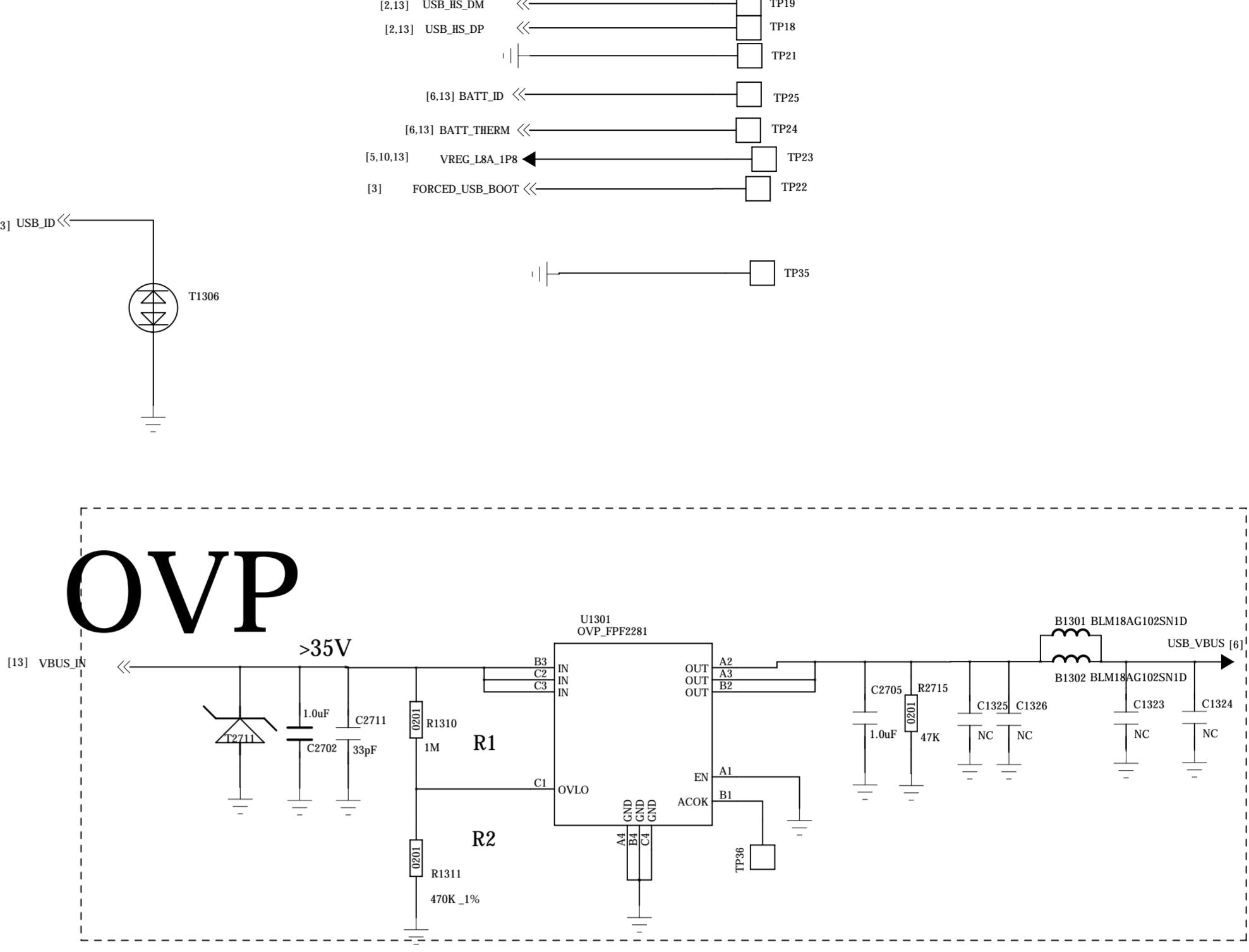
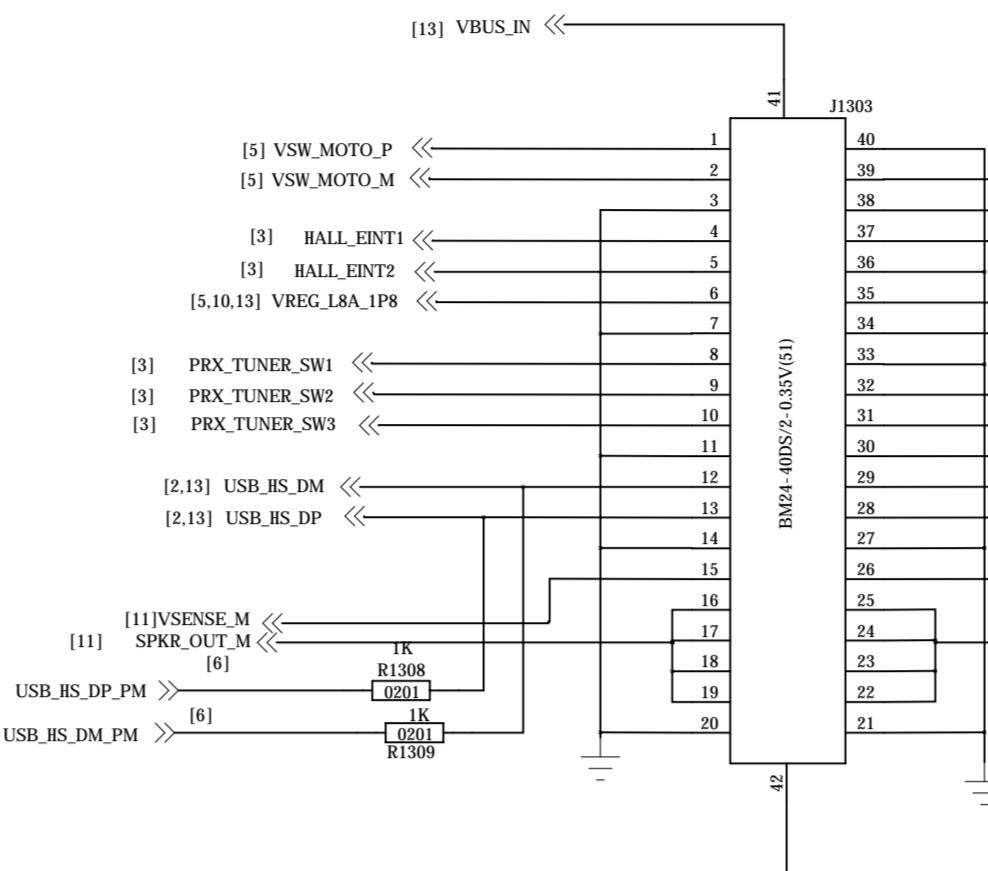
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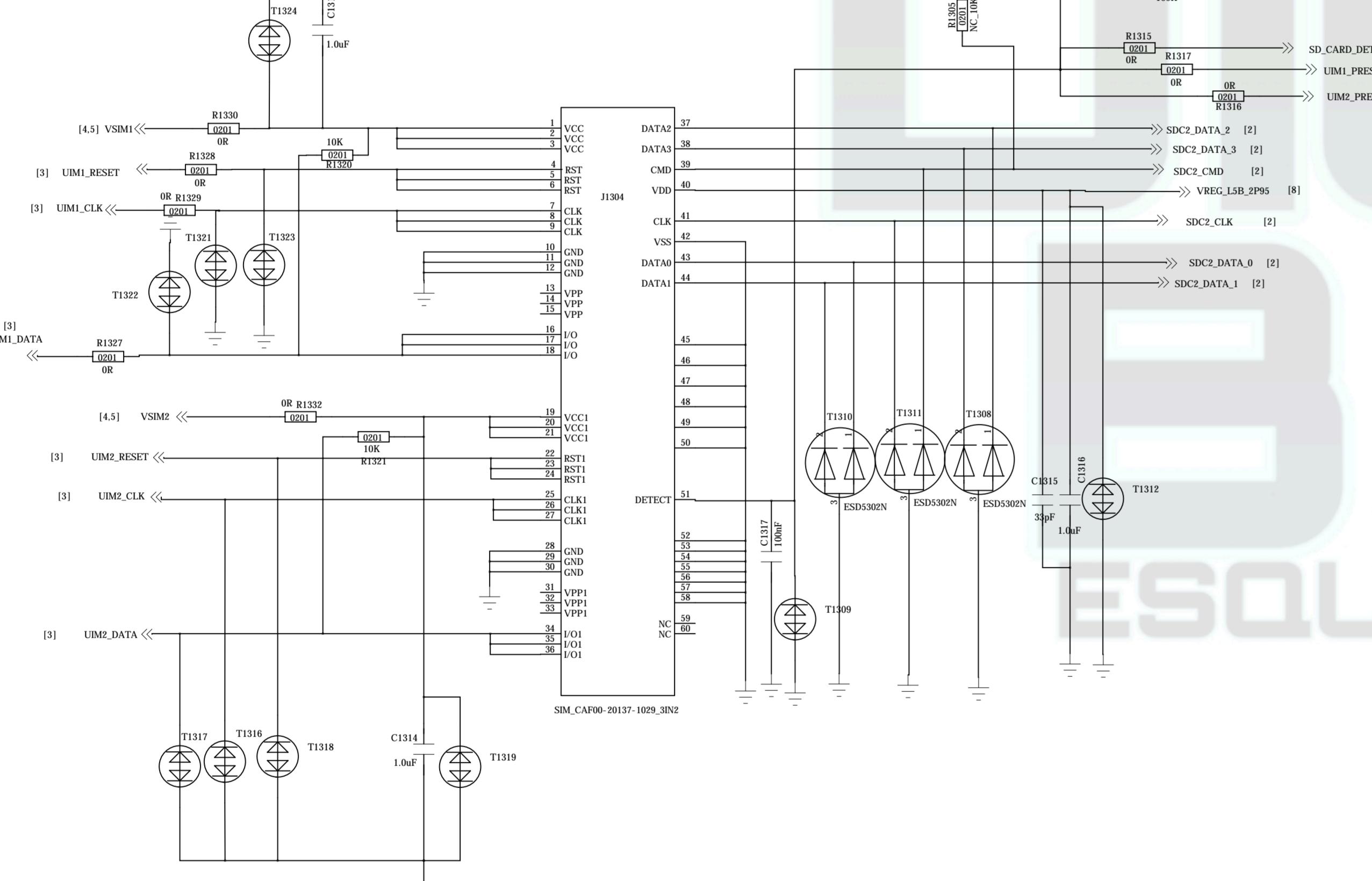
Battery Connector



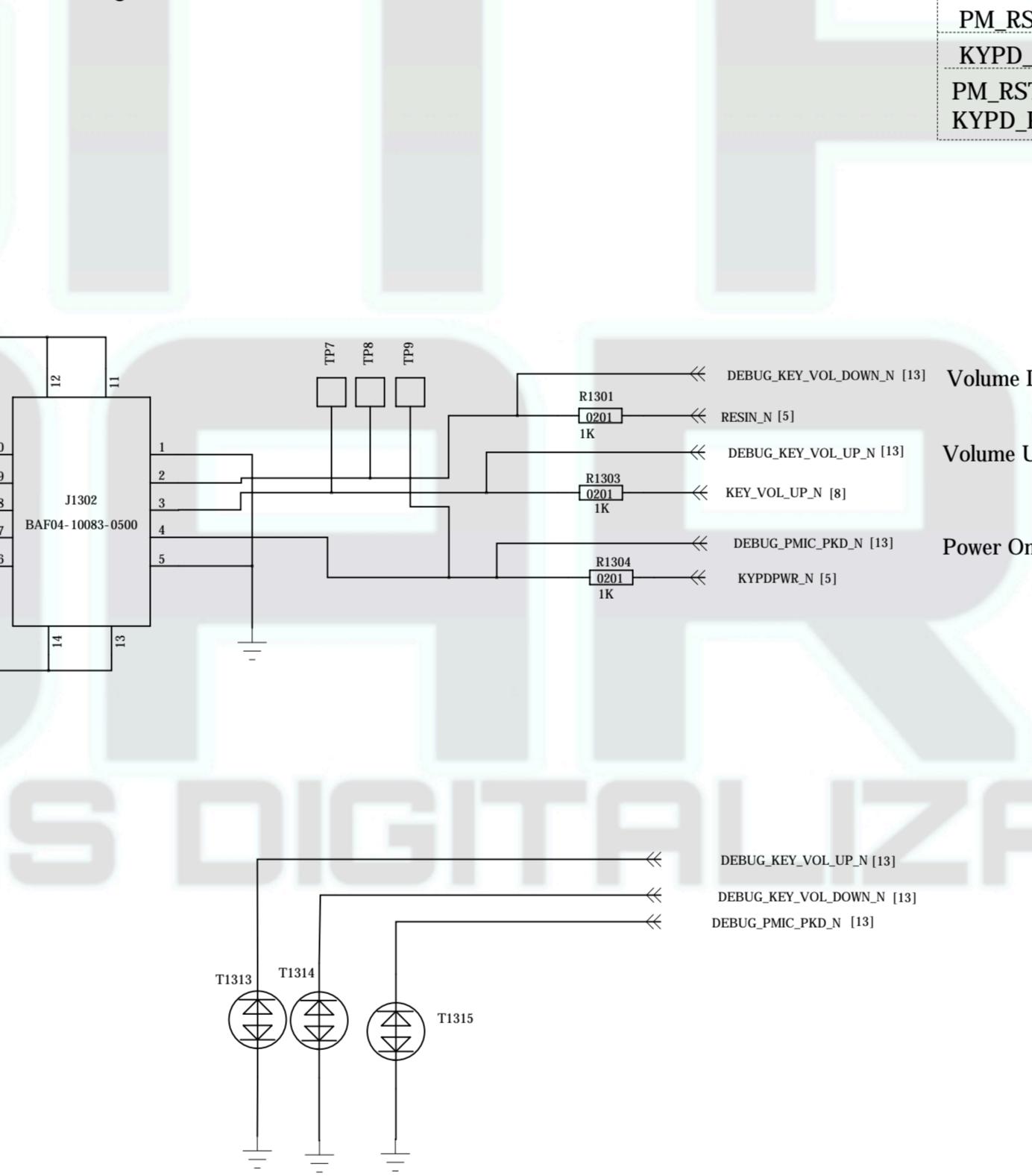
SUB_FPC



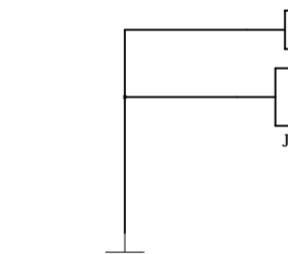
SIM&SD



Sider Key



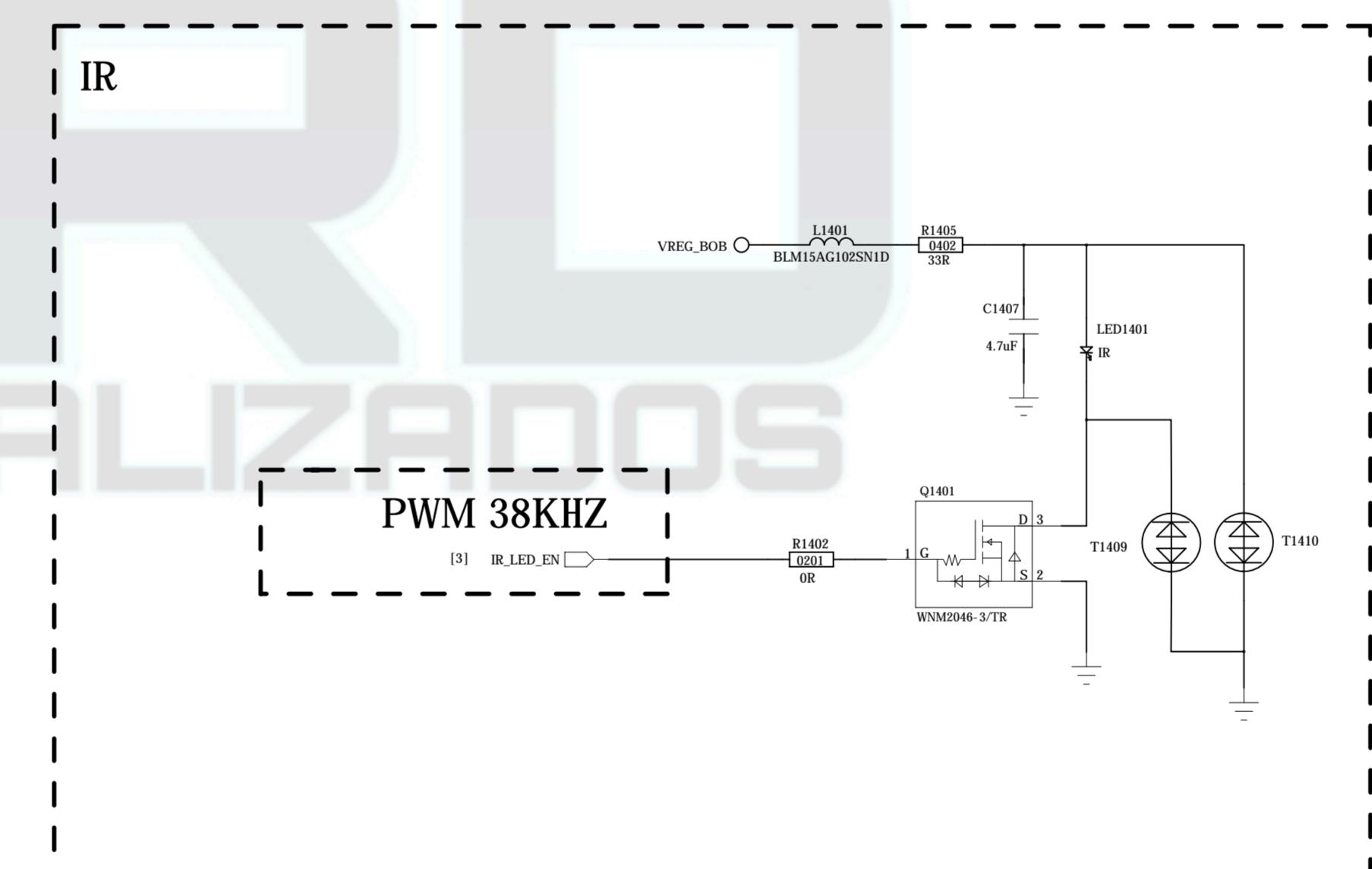
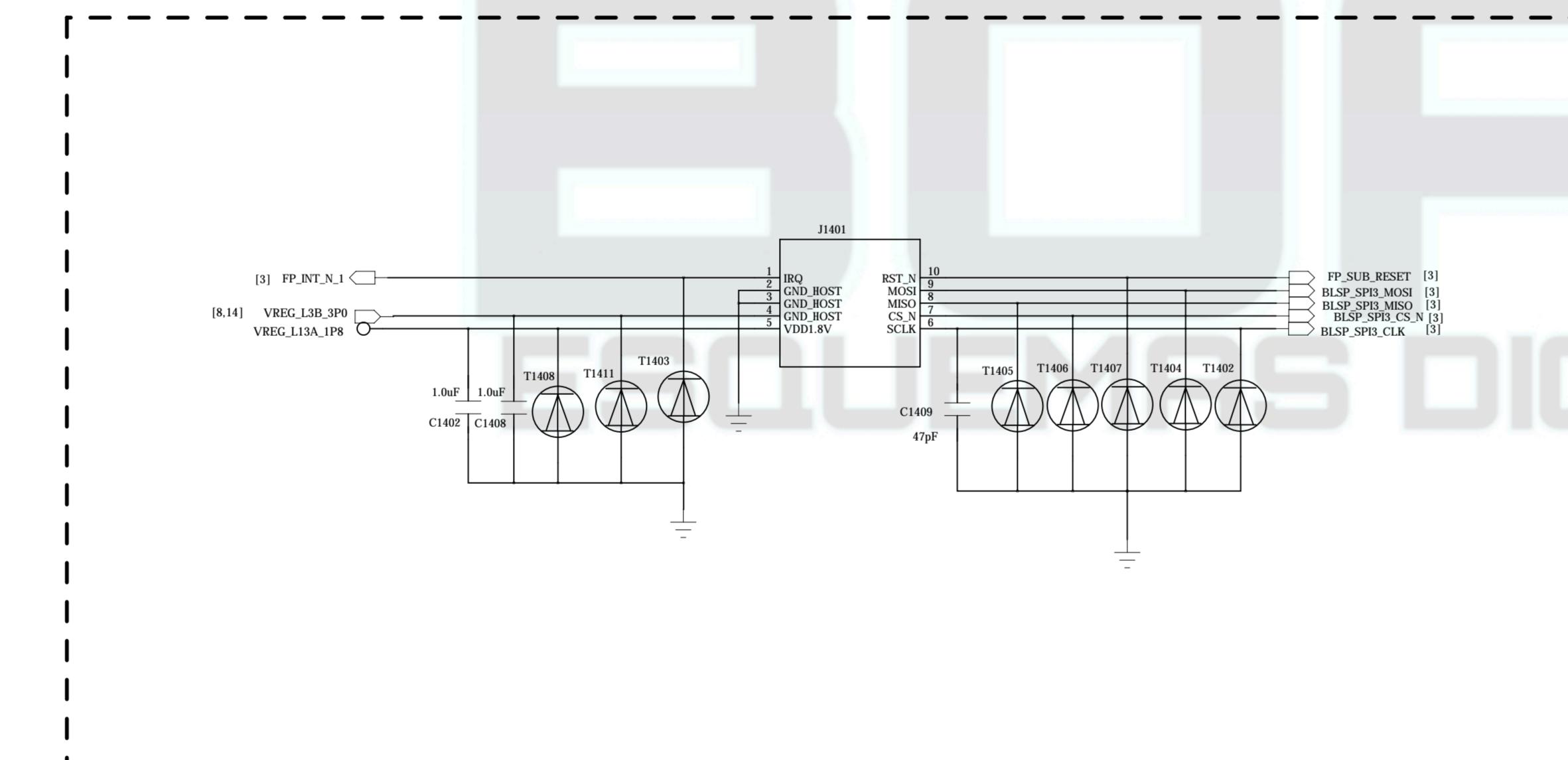
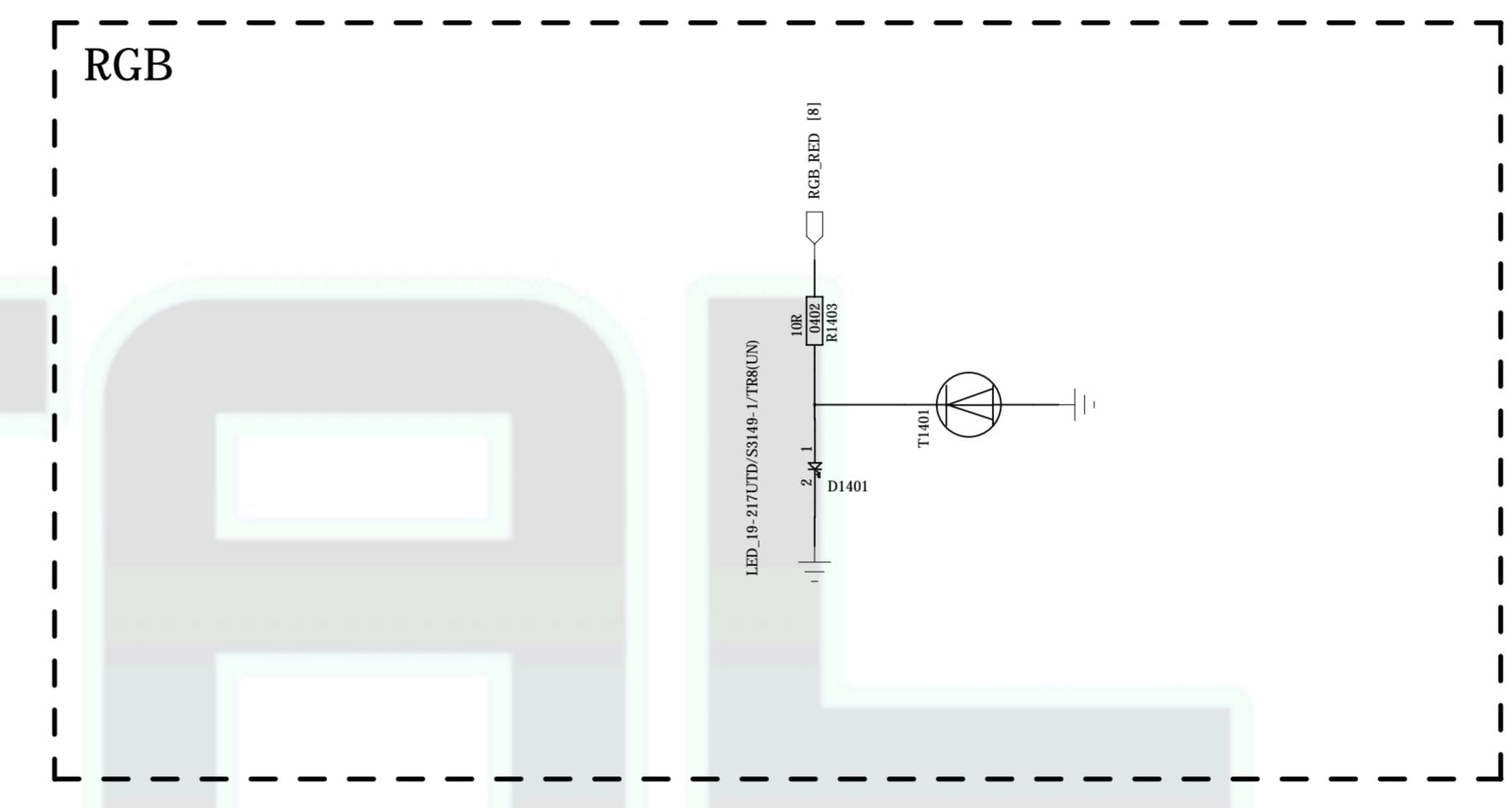
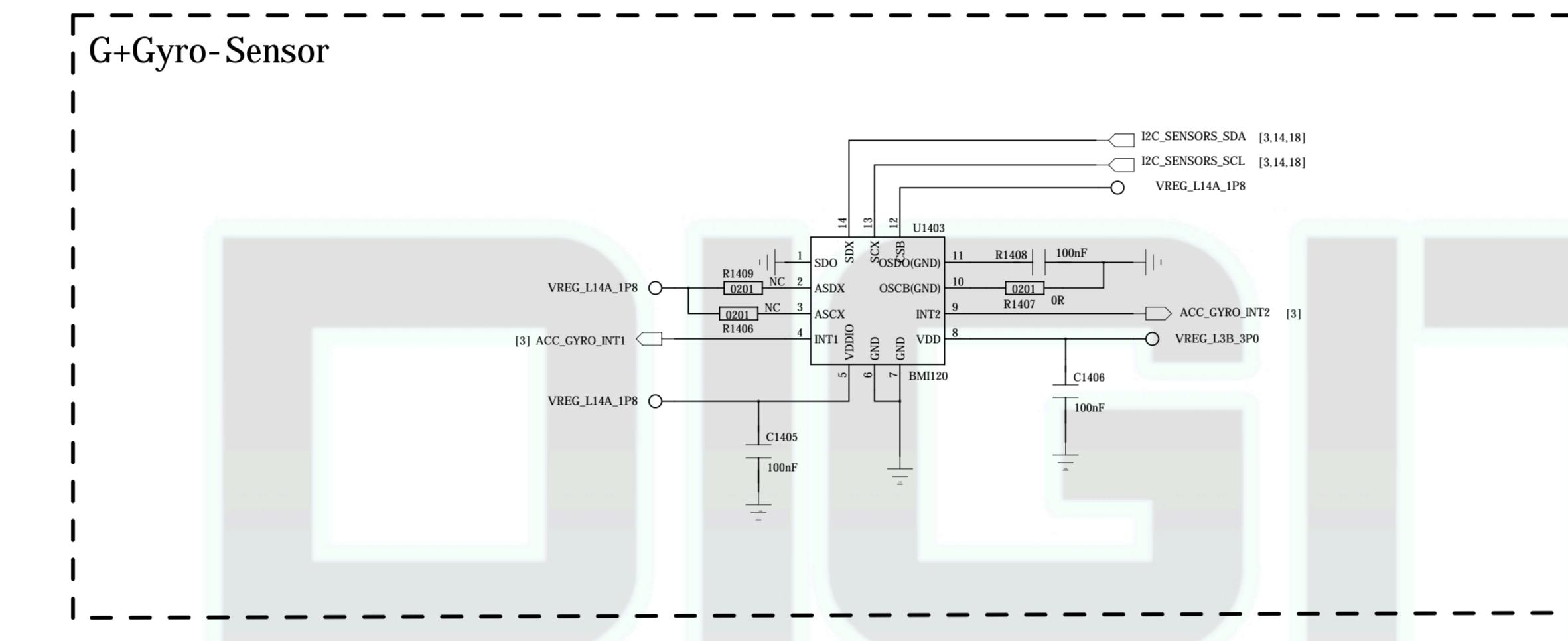
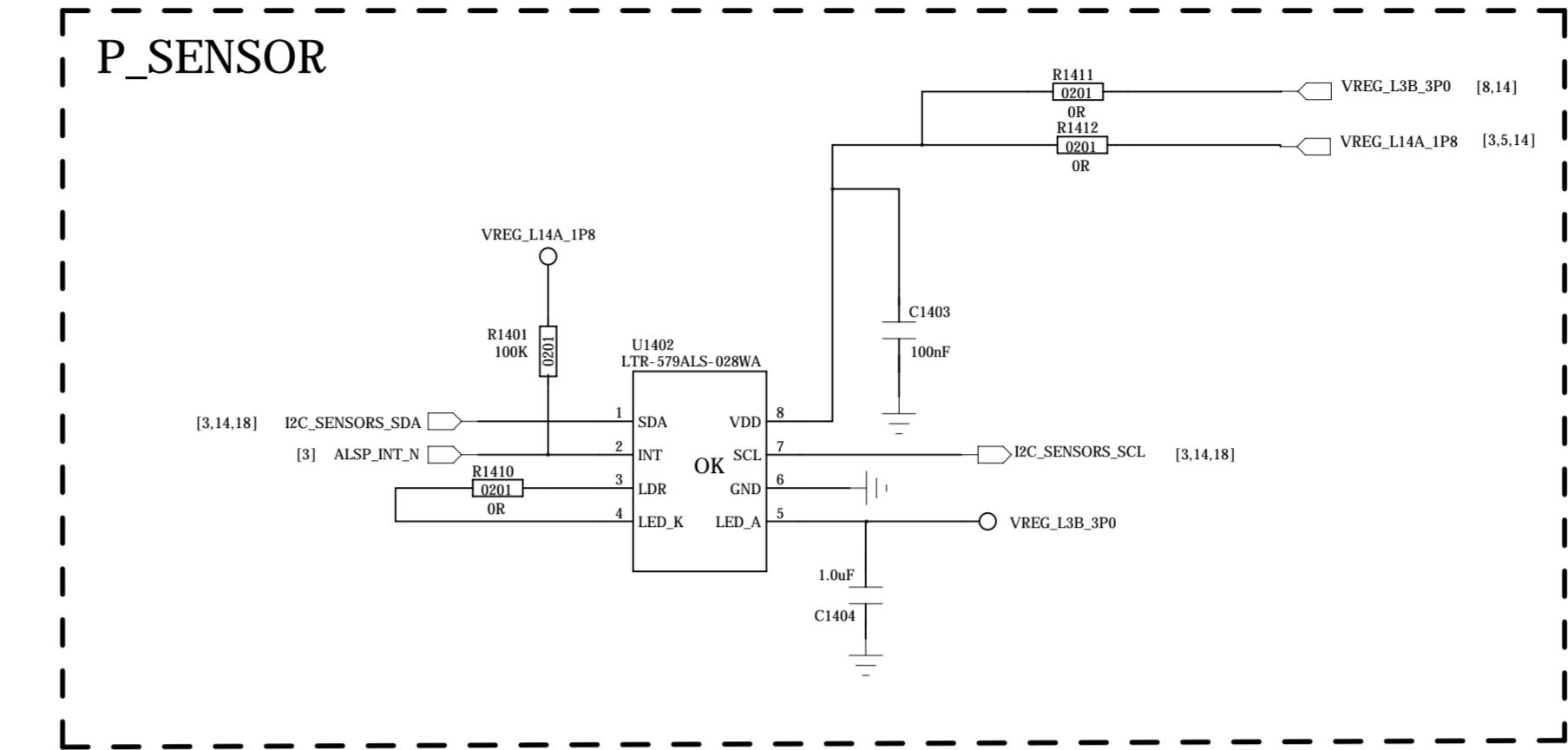
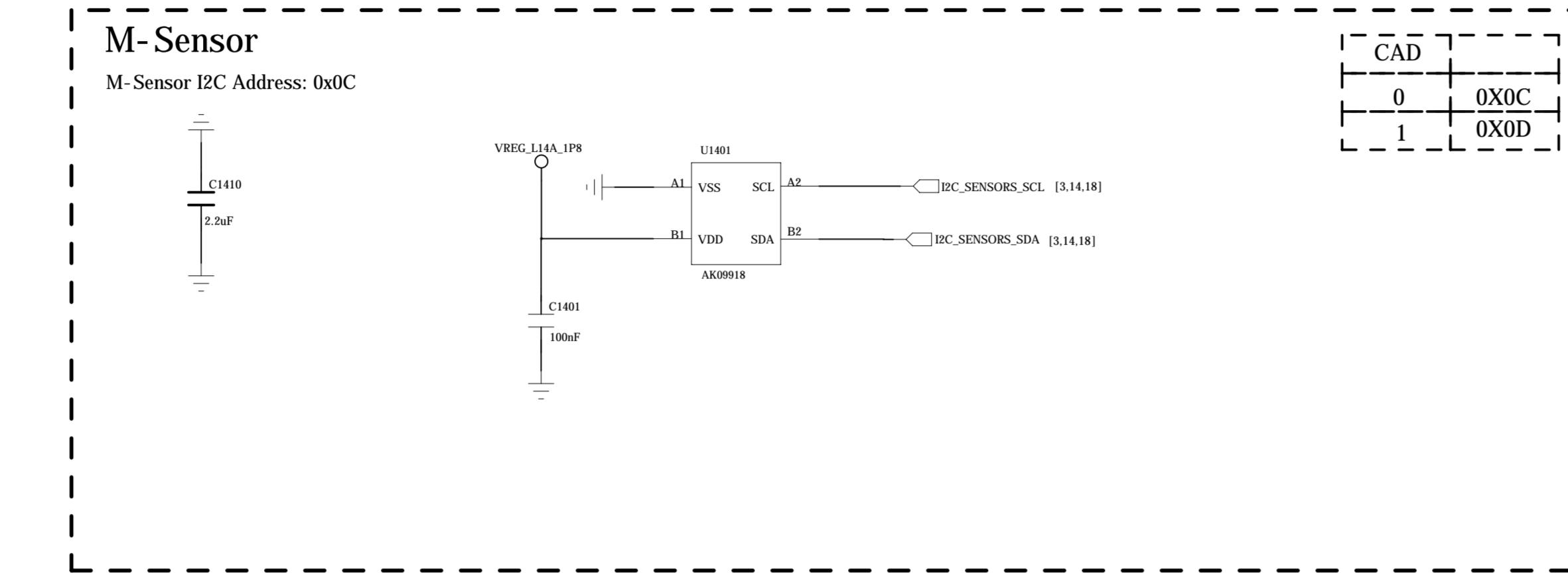
SUB_LED



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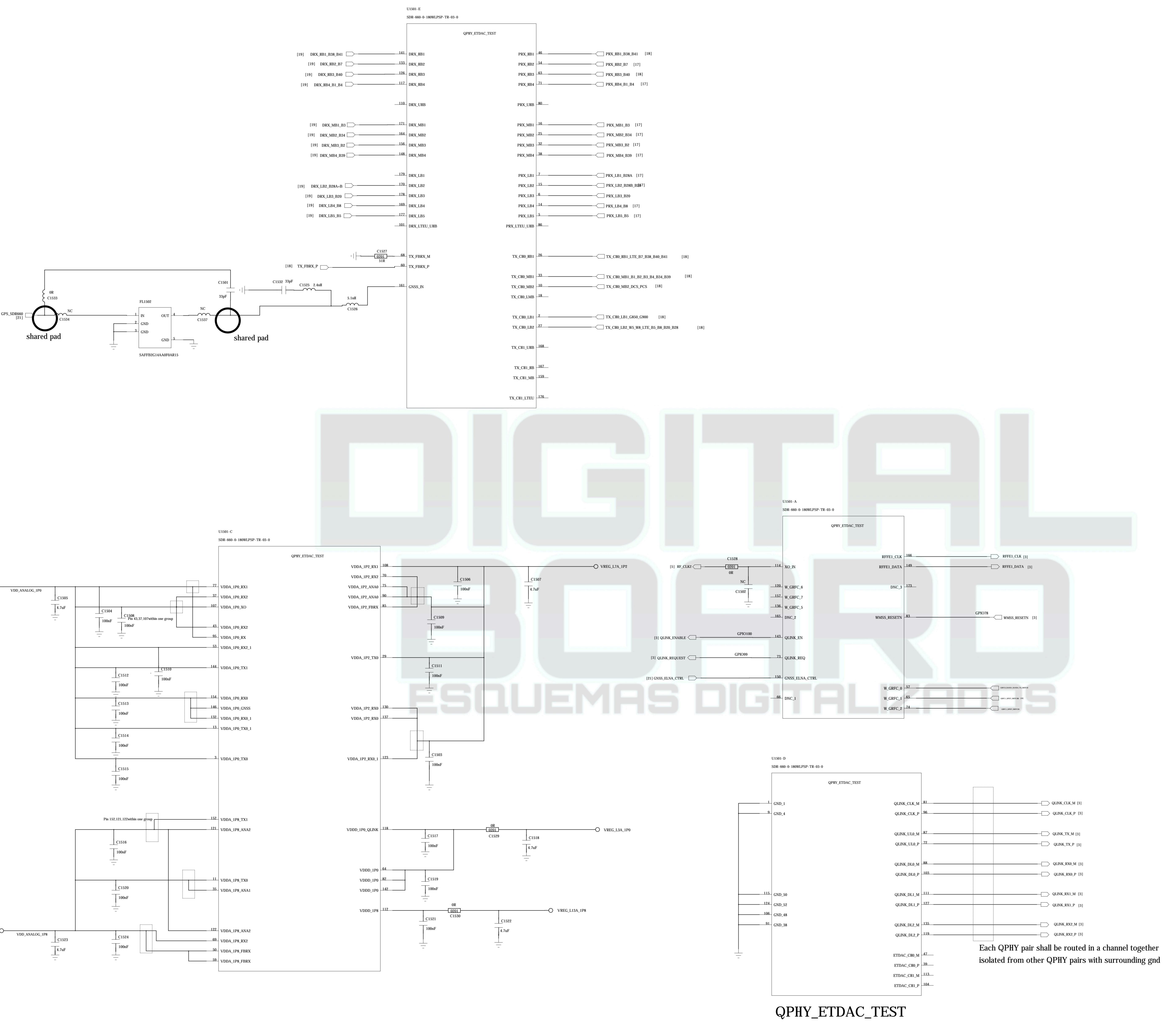
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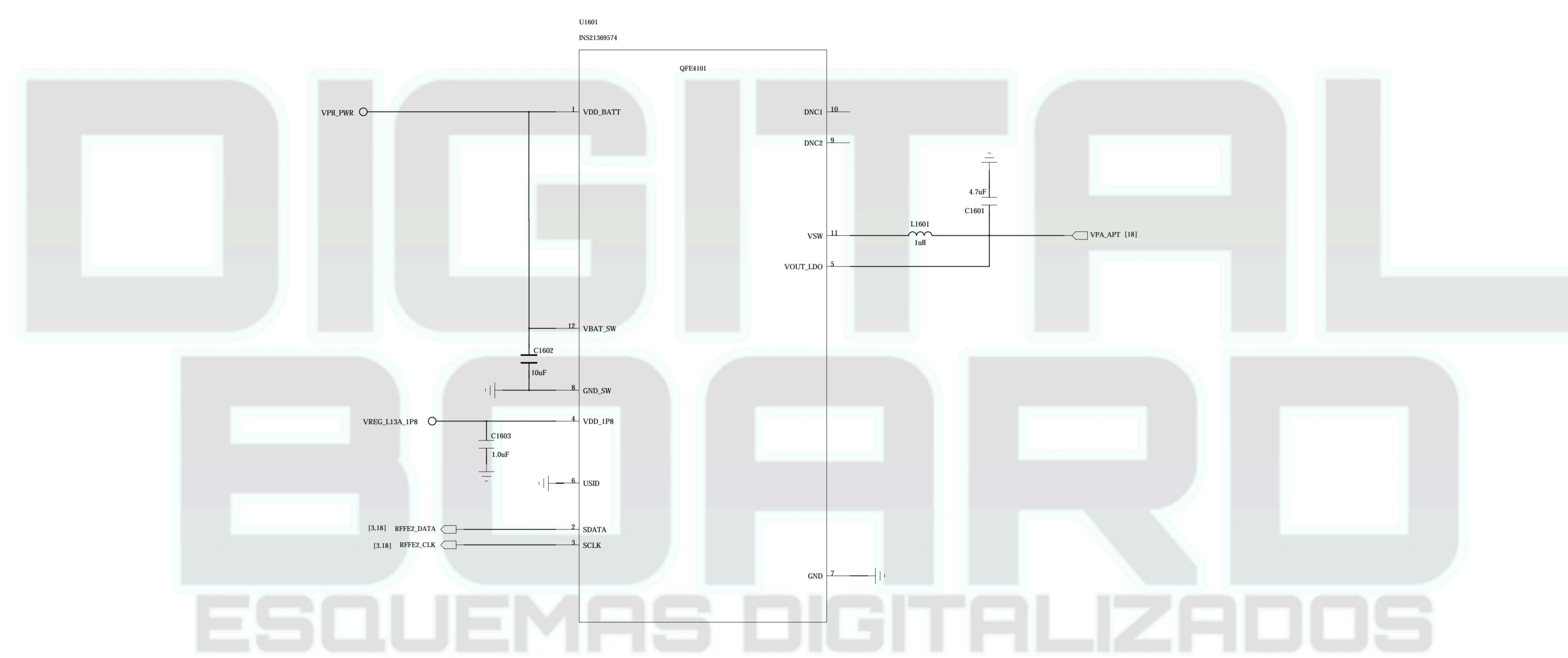
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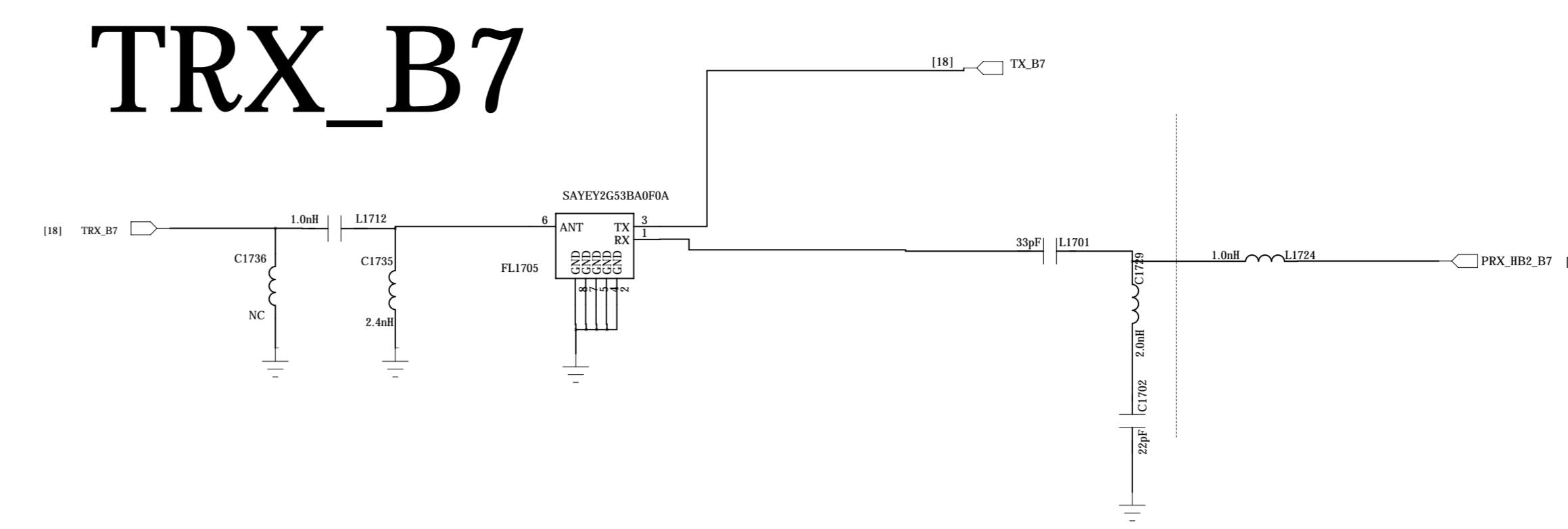


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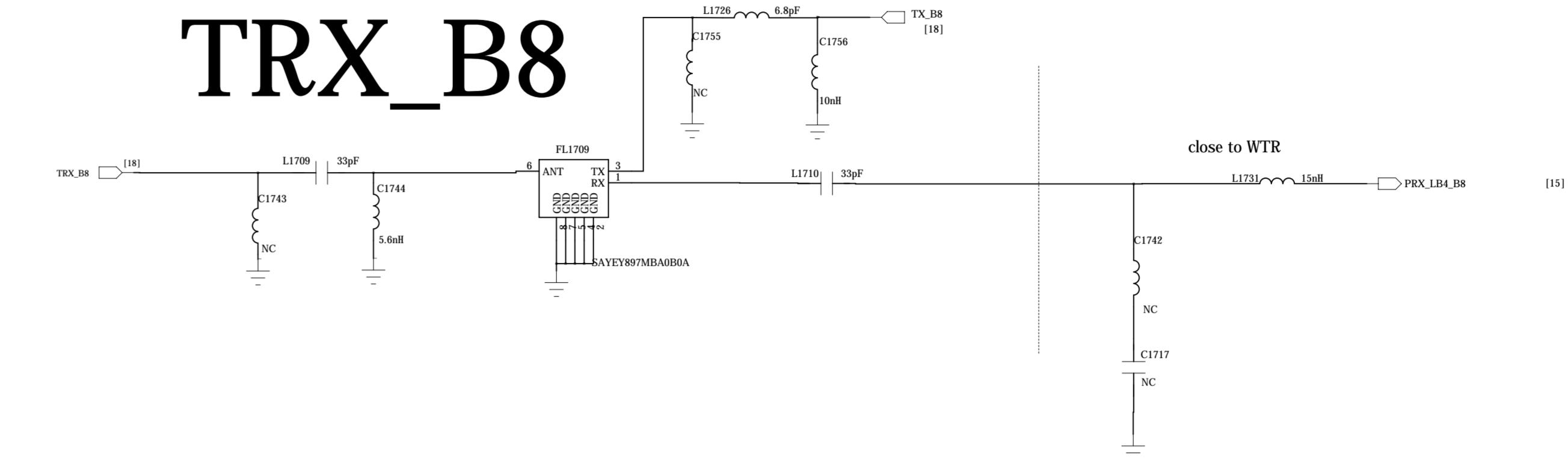
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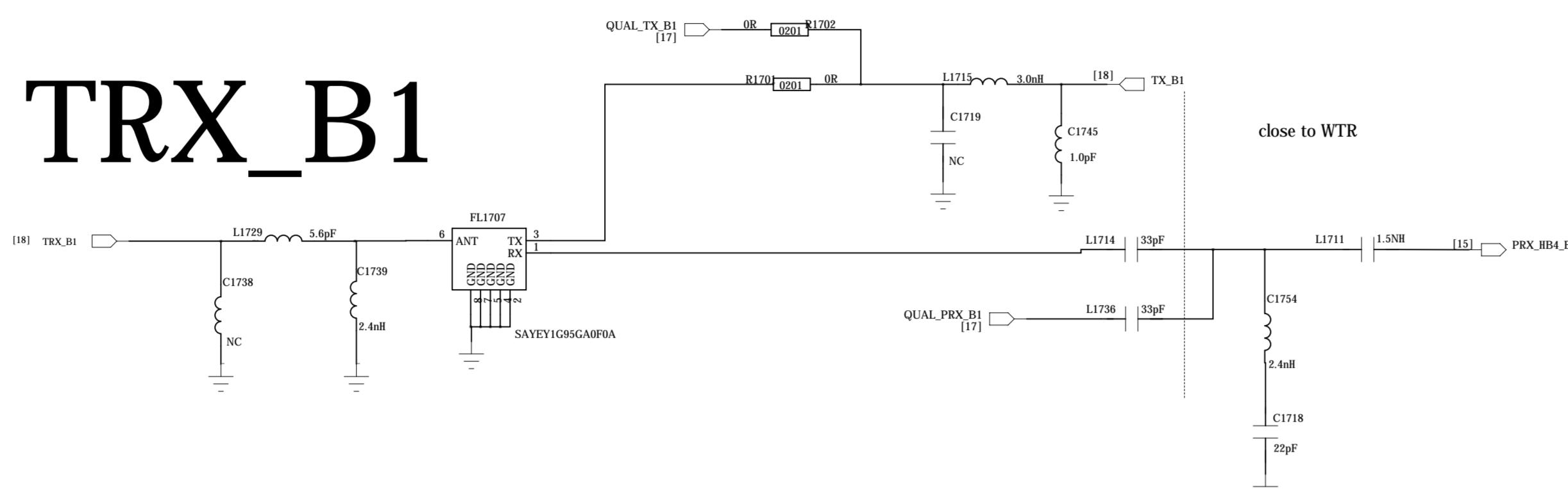
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TRX_B8



TRX B1



TRX_B1_B3_B4

RF1630	
MODE	VC1
RFIN--RF1	0
RFIN--RF2	1

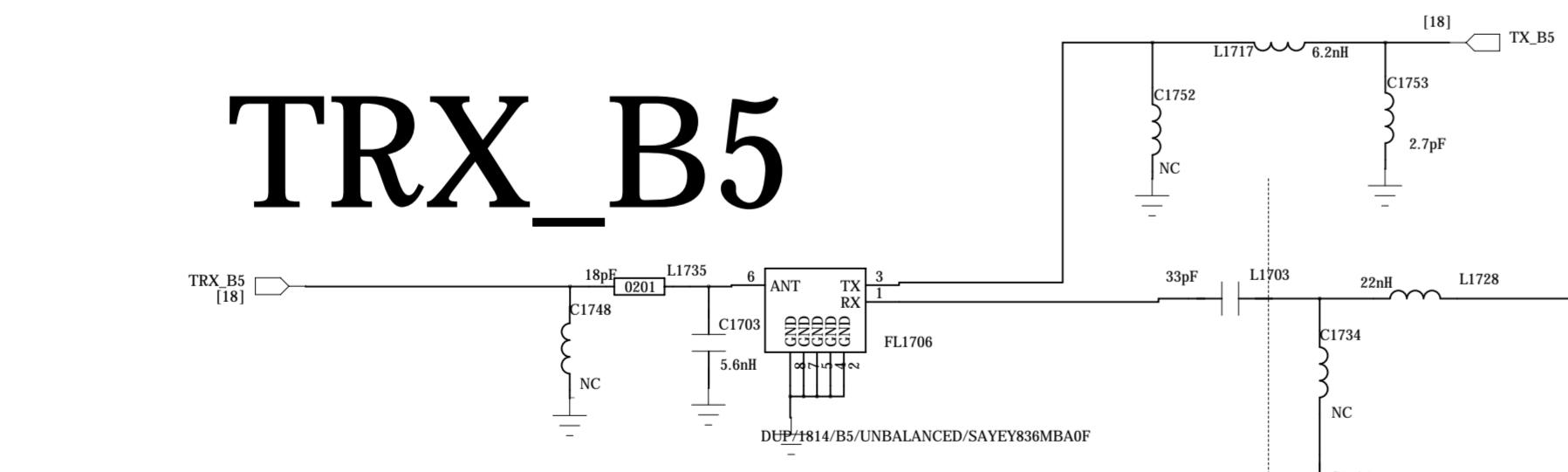
TRX_B2



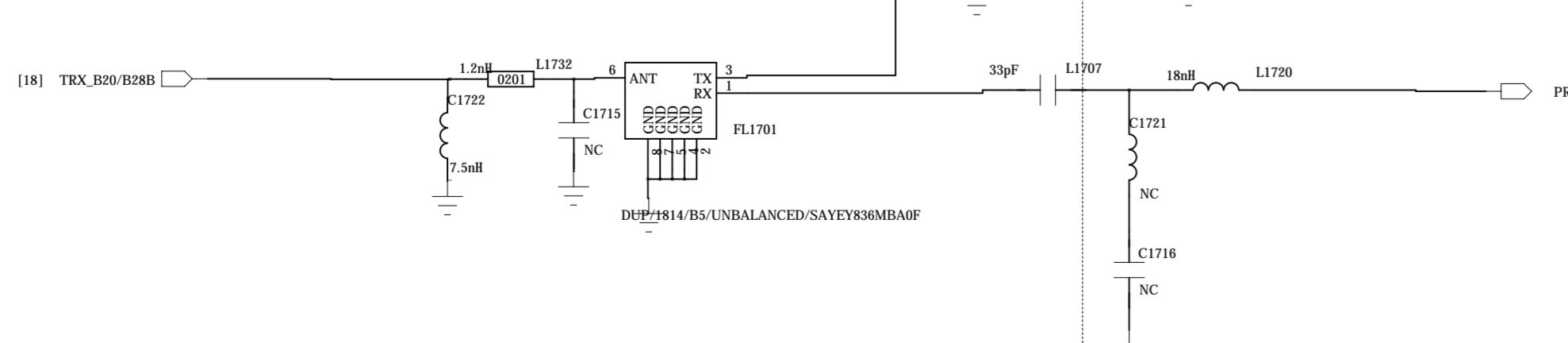
TRX_B3



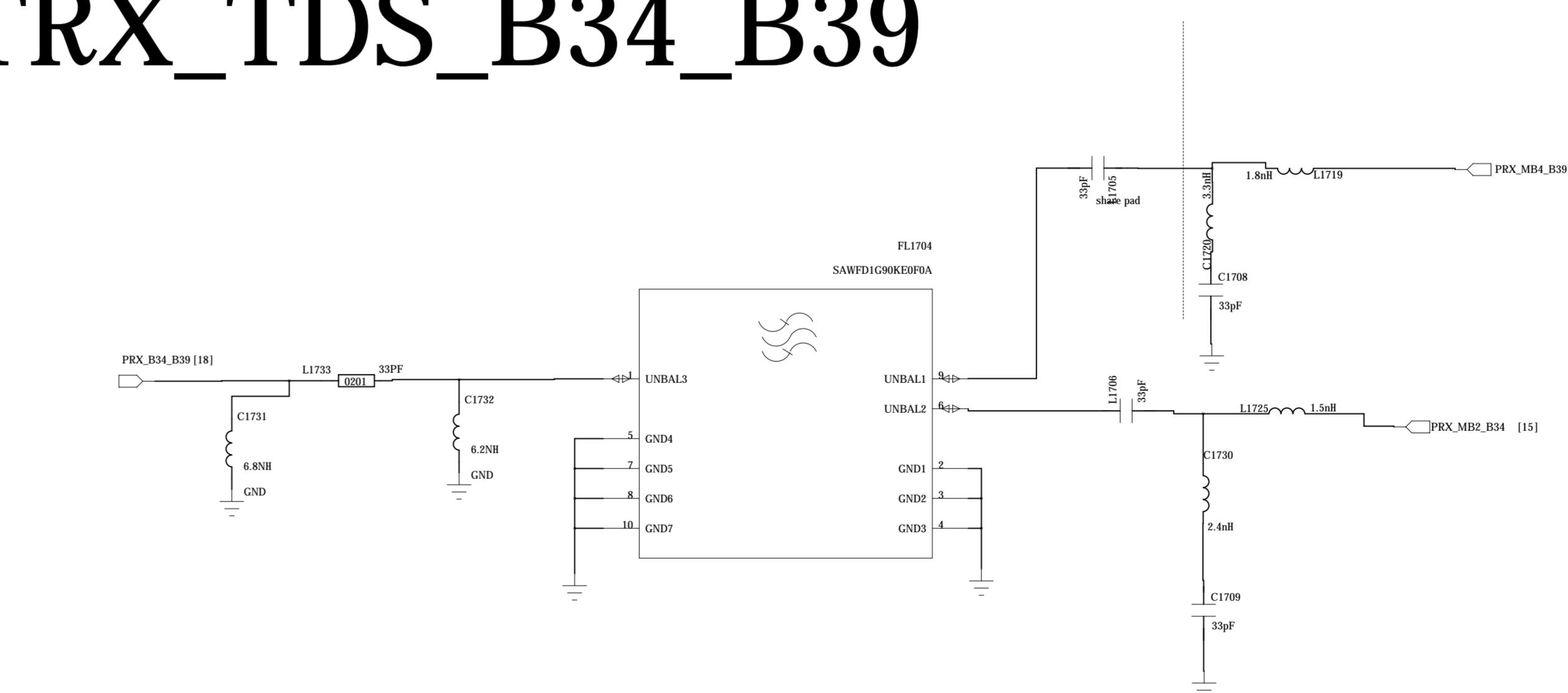
TRX B5



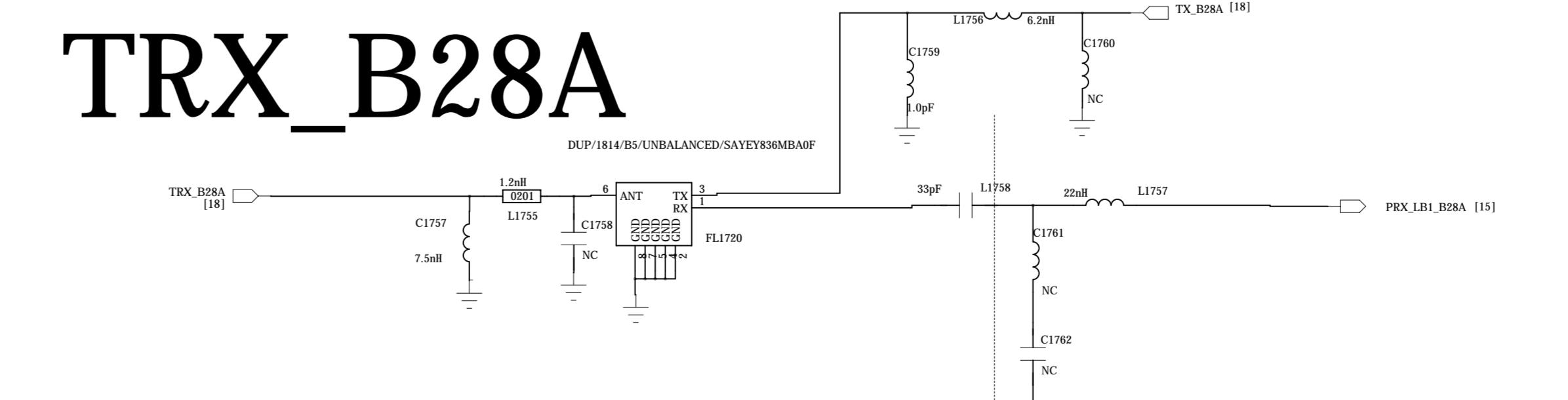
TRX_B20/B28B Shared with B34_39_RX



TRX_TDS_B34_B39



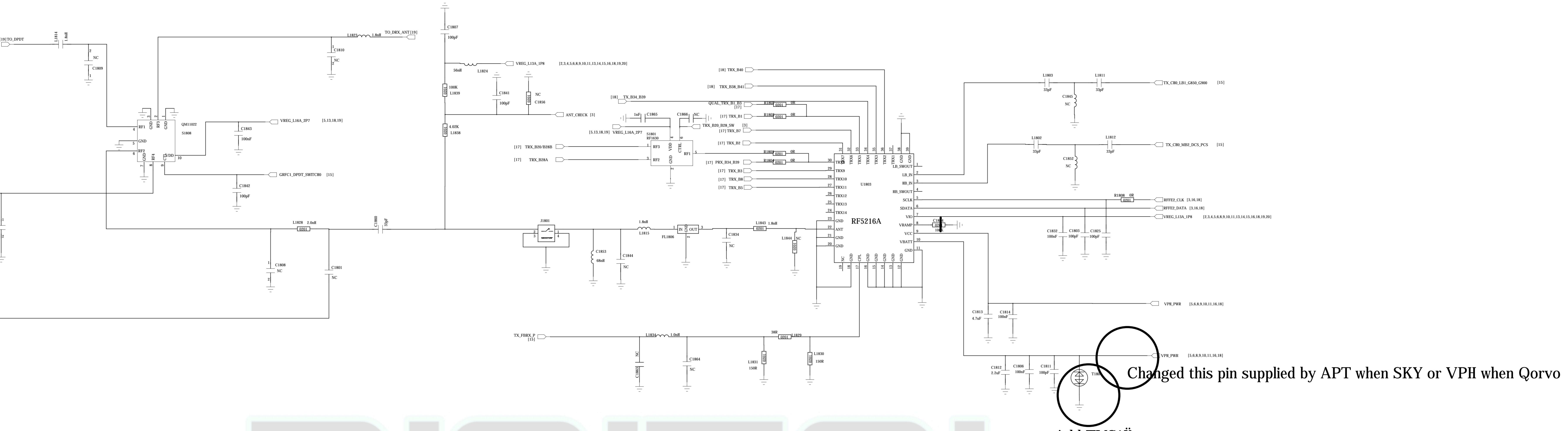
TRX_B28A



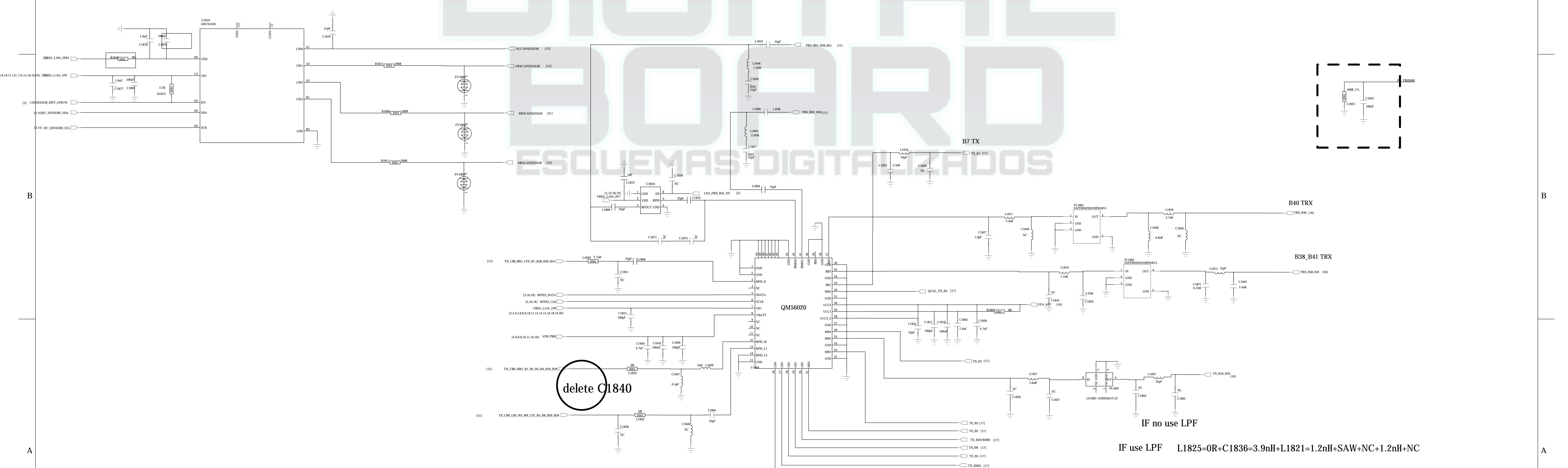
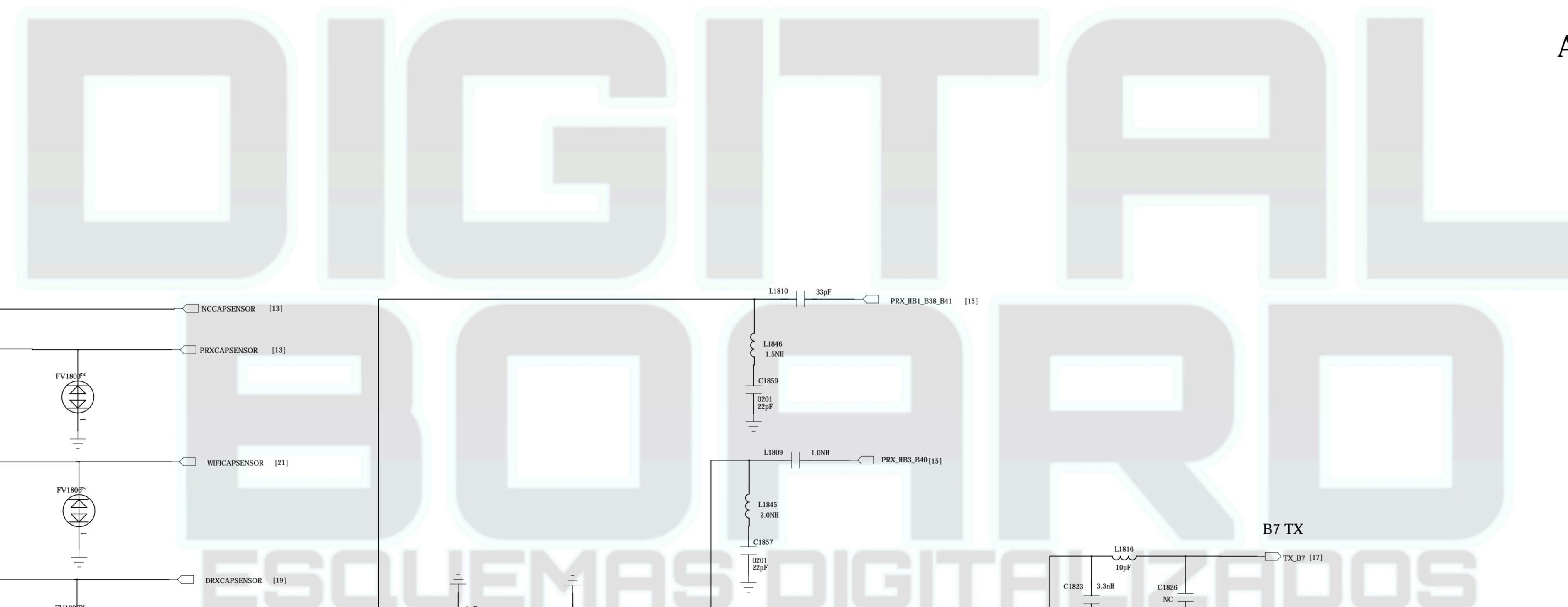
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DATED:			

If walsin,R61,R62 should be NC



SAR Sensor




(delete C18)

If no use LF

IF use LPF L1825=0R+C1836=3.9nH+L1821=1.2nH+SAW+NC+1.2nH+NC

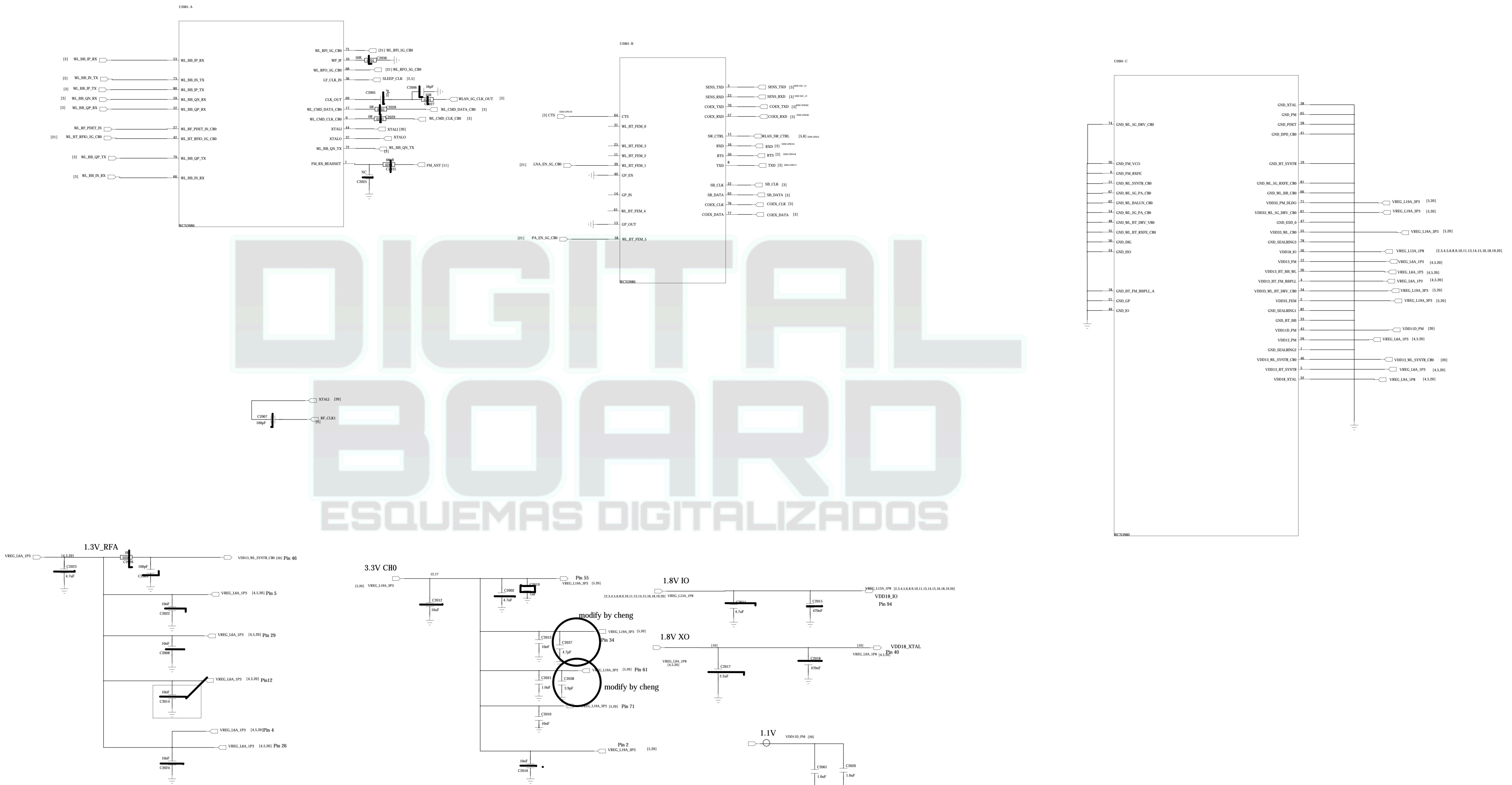
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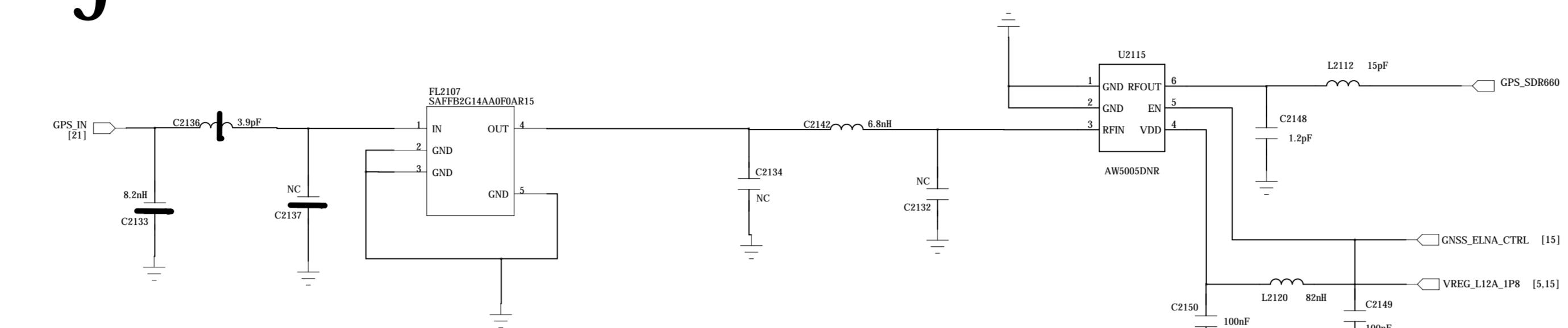


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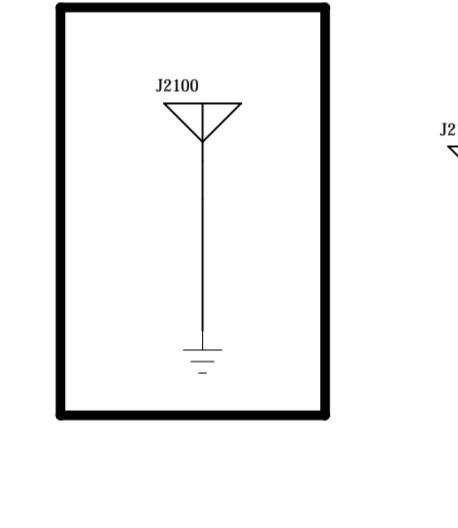
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GPS

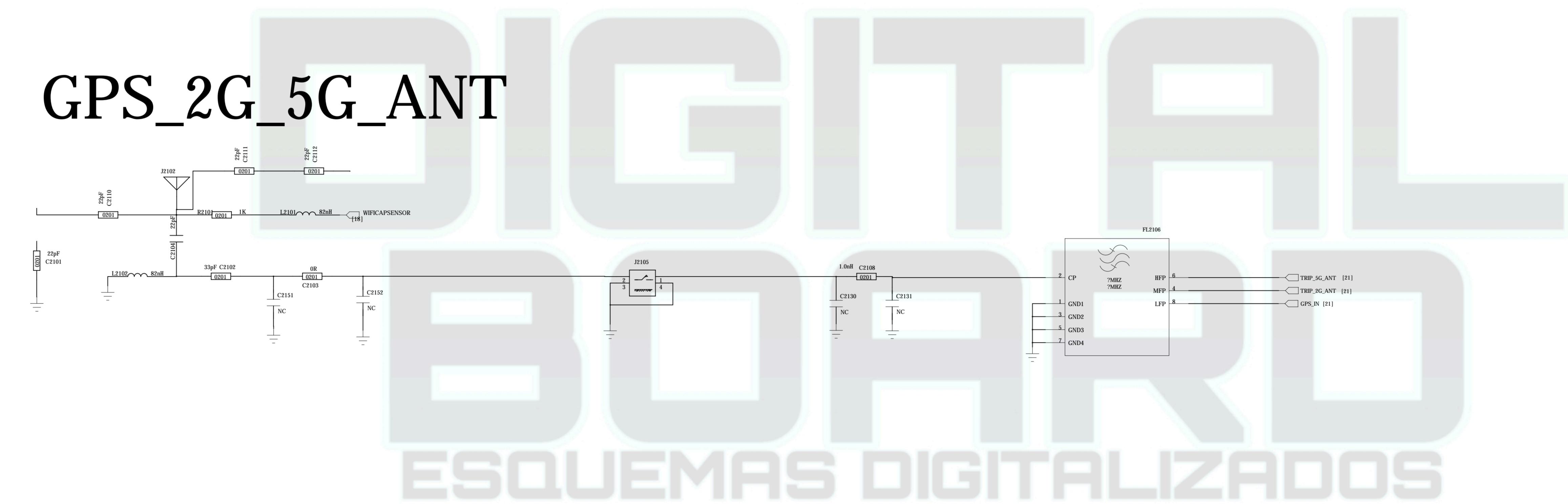
High rejection saw



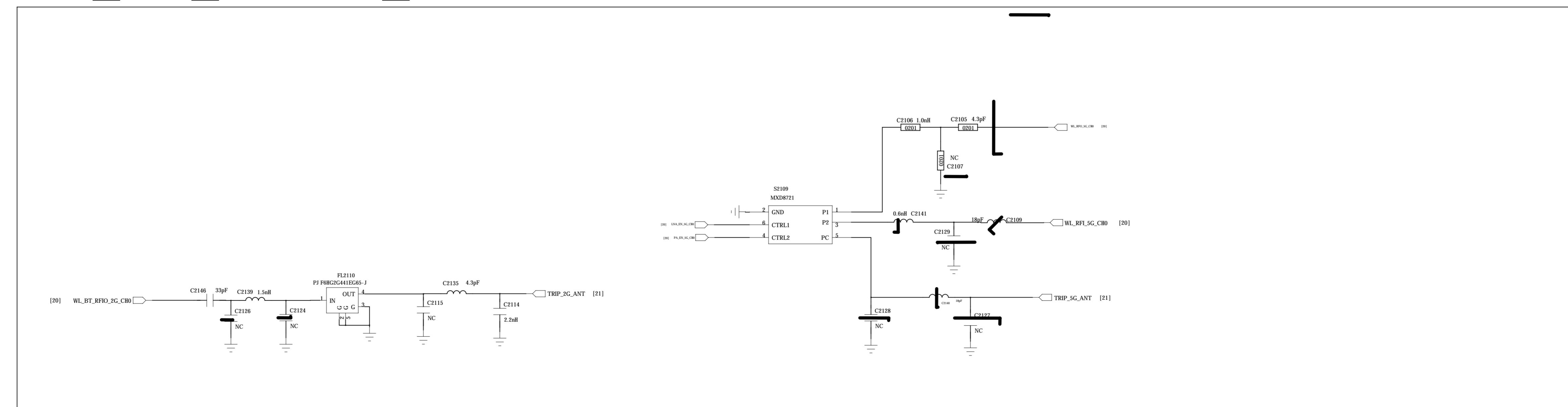
used for connect to ground



GPS_2G_5G_ANT



2G_5G_WLAN_FEM



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