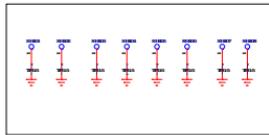
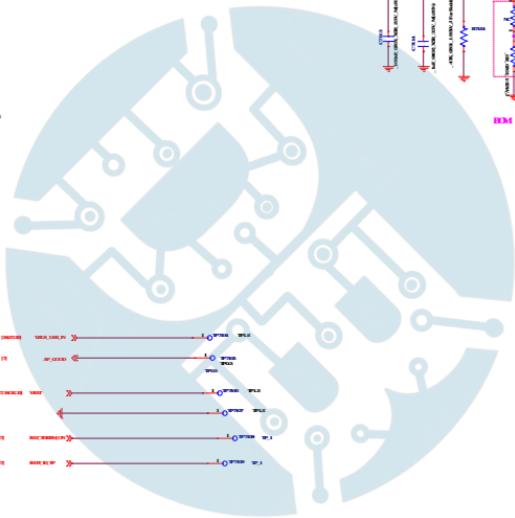
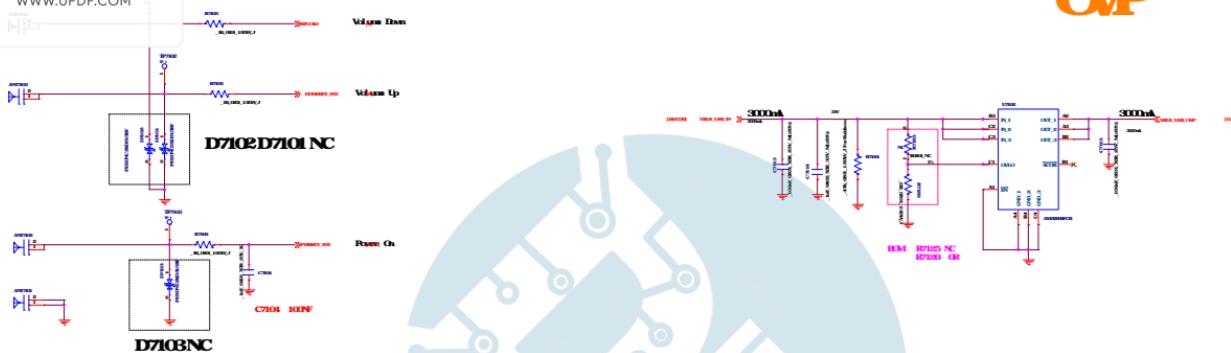
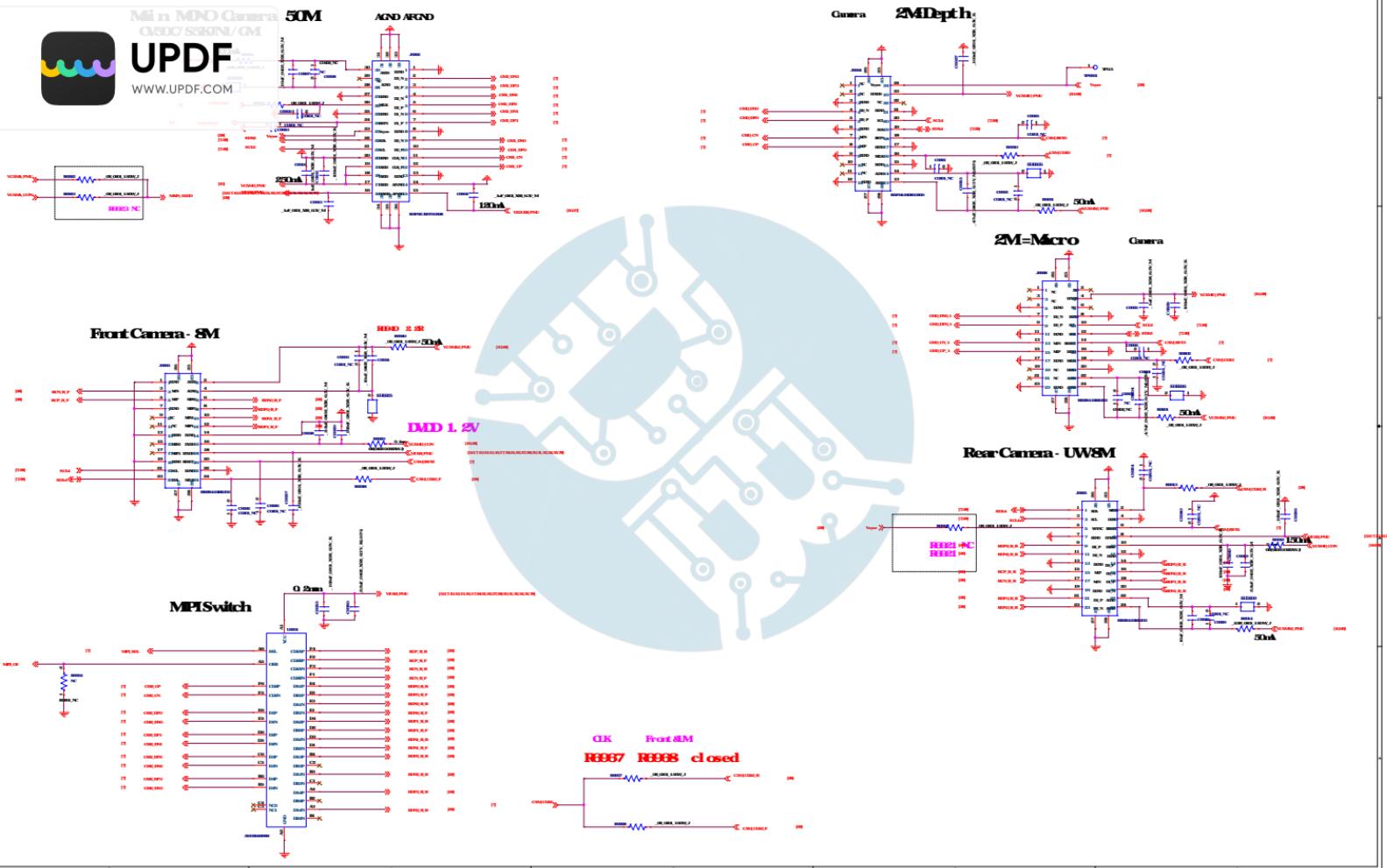




OP





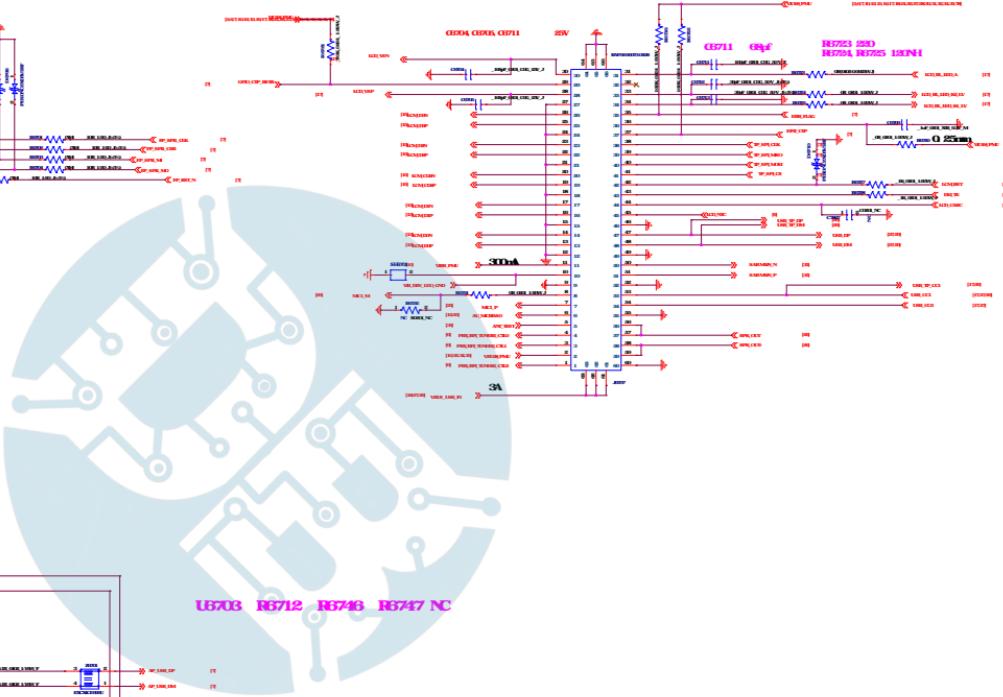
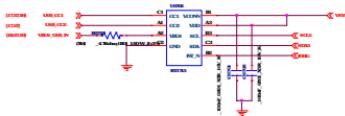


EngerPoint

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HD

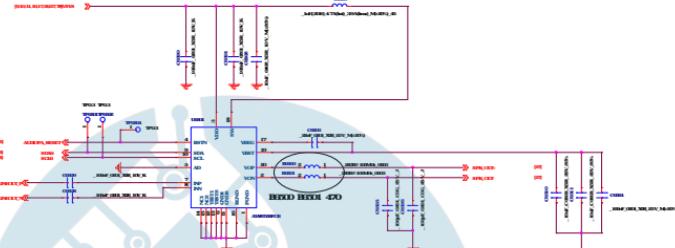




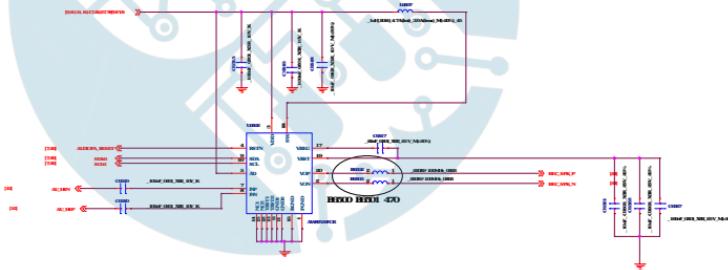
# SPEAKER

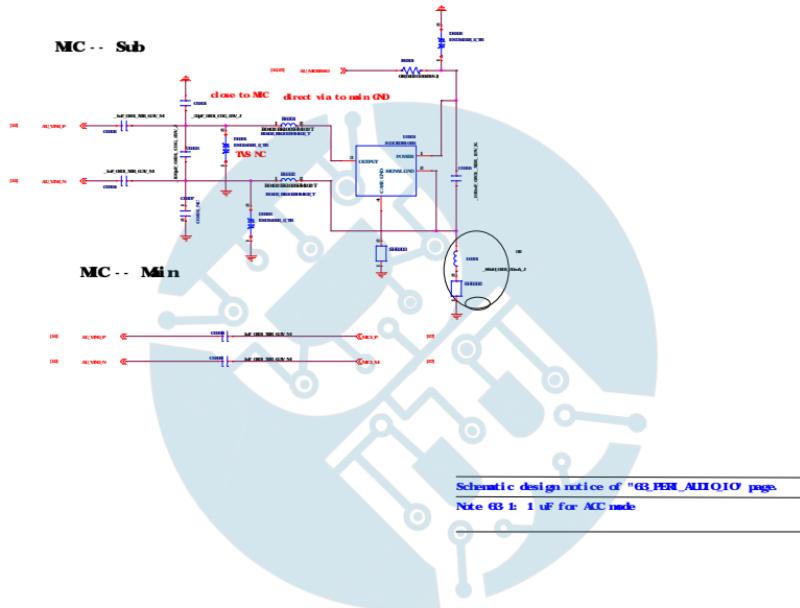
	ICL2866
ADDRESS	00001111

# Allopa



# REC&SPEAKER





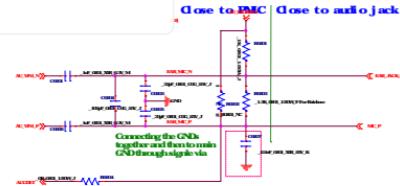


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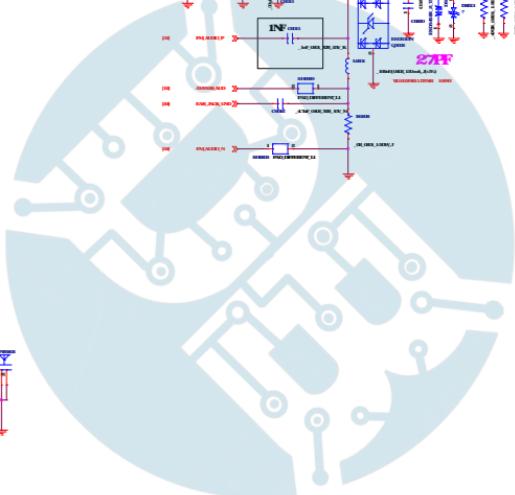
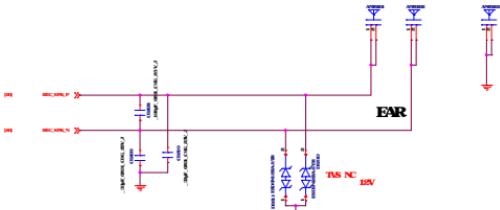
000108 DB212 DB214 DB213 DB215  
000208 DB205 DB204 DB202 DB207

Close to BMC Close to audio jack



Connecting the GNDs together and then connect GND through bridge

## Receiver



Schematic design notice of "08\_BRR\_AUDIO10" page.

Note 08\_1: Part # of BEN0008, BEN0003, BEN0004 and BEN0005 needs changed to "BLM000005N" for high TD performance (-0.03B) but this BMchange will results in PM RSSI 10B degraded .

Note 08\_2: Reserved Cap for CS/BS test, please double check multi-key function when used

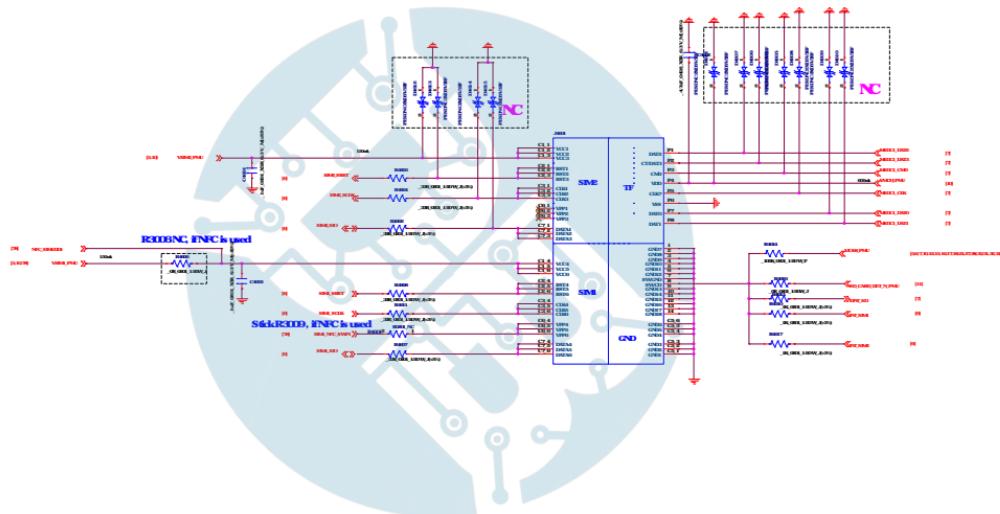
Note 08\_3:

Preferred Jack	Alt Jack
MINI	MINI



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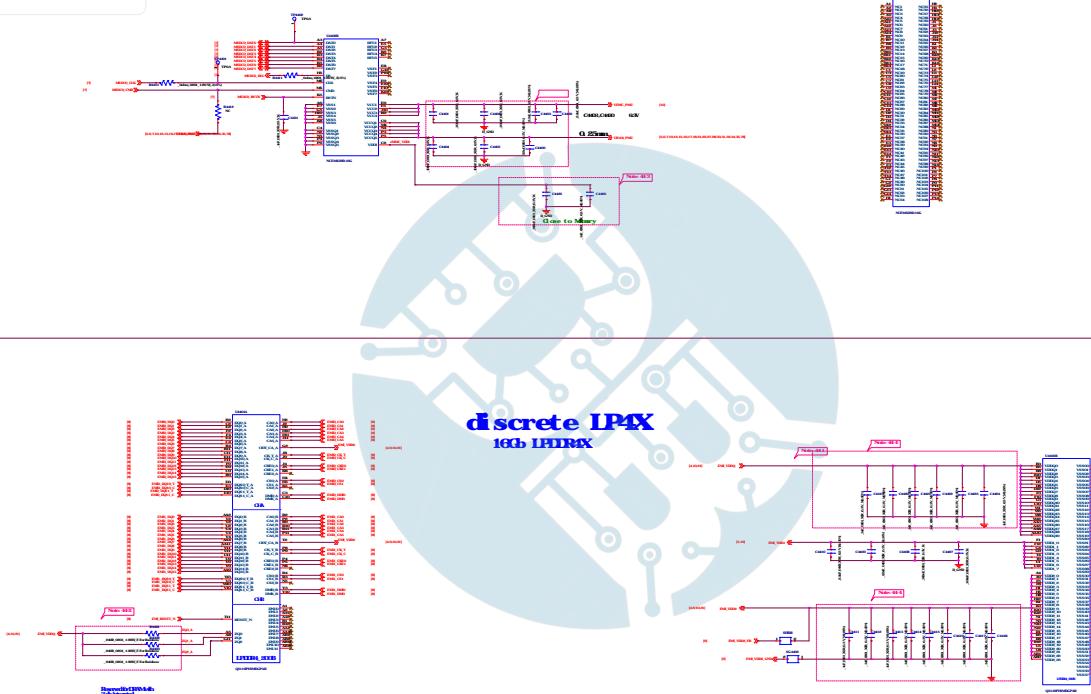


Note 431

Schematic design notice of "4G\_MEMORY\_SD Card" page

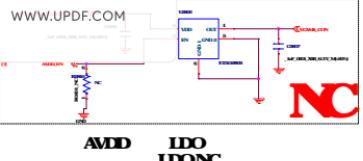
**For better ESD performance, please select suitable components for system protection**

### DISCRETE EMMC 16GB 100PIN

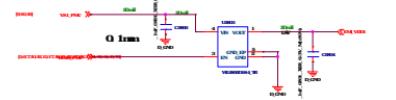




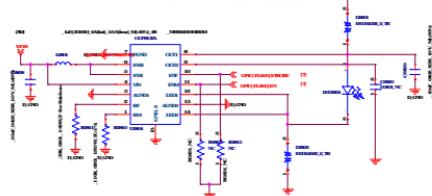
# UPDF Dual Camera (VCAMA\_EXT)



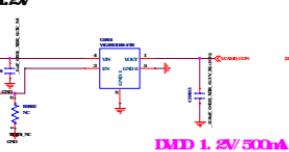
## Ext EM VDD1 for LPDDR4XVDD1



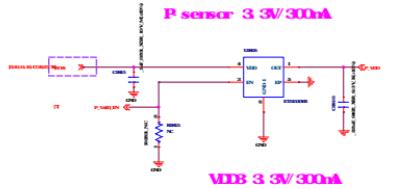
## FlashLED 5V/Boost



## IDO for Front Camera & LMS (VCAMD\_EXT) 1.2V



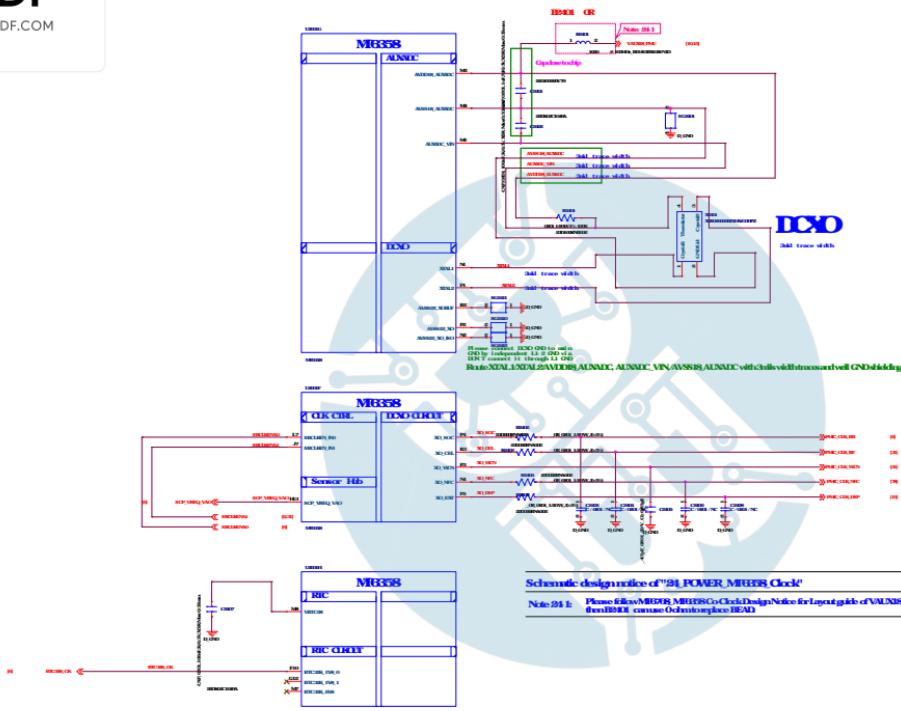
## P sensor 3.3V/300mA





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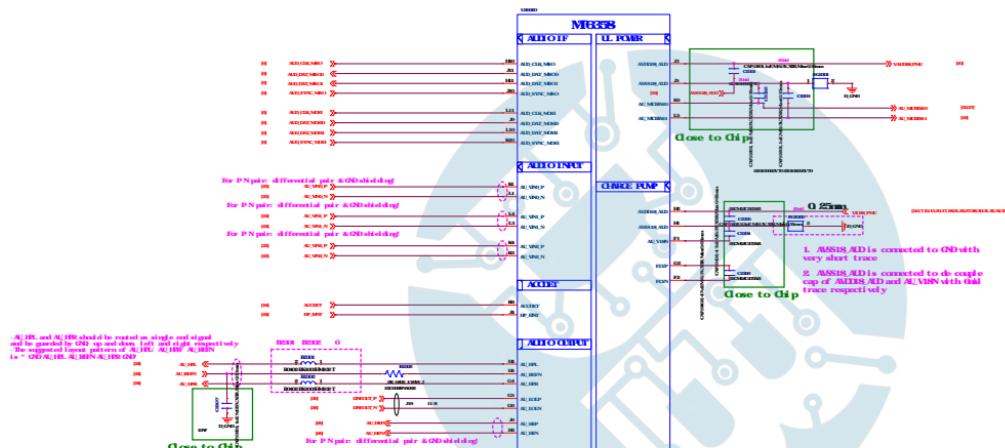
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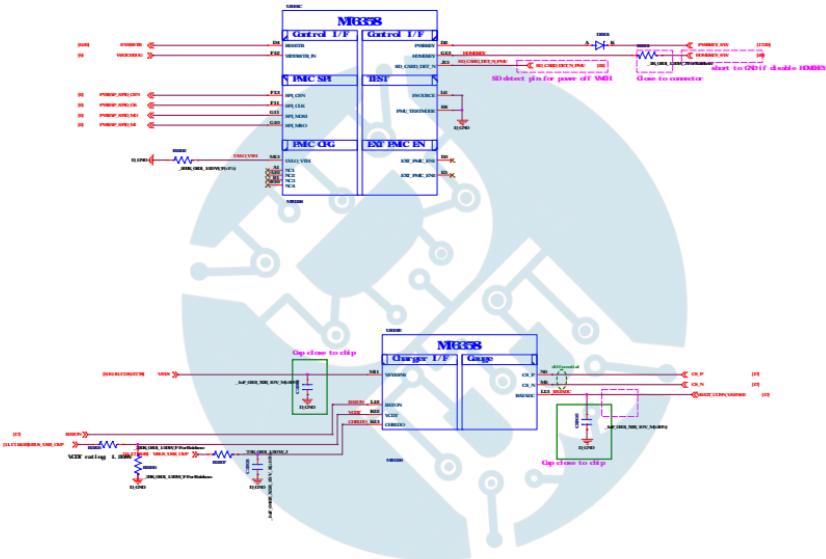
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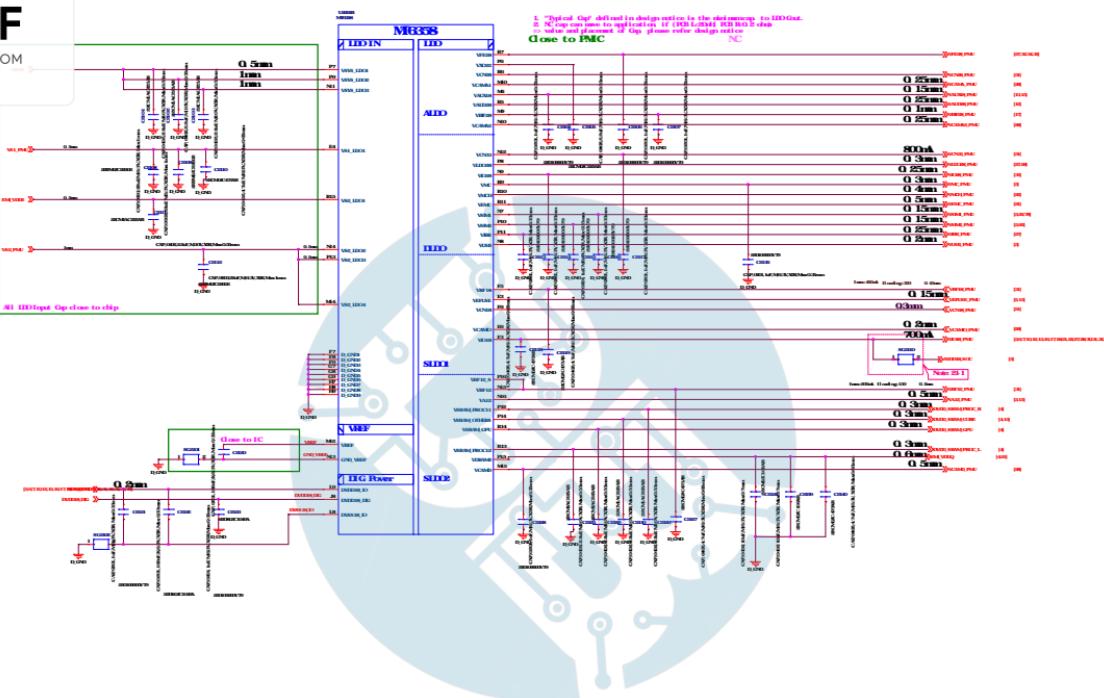
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Schematic design notice of "21\_POWER\_M16358LDO" page

Note 21-1: Please set SG2110 close to C211S making star connection between VIOIS PMU and AVIDIS SOC near to I2O can C211S

Please also contact MIEERS design unit for further detail design information.

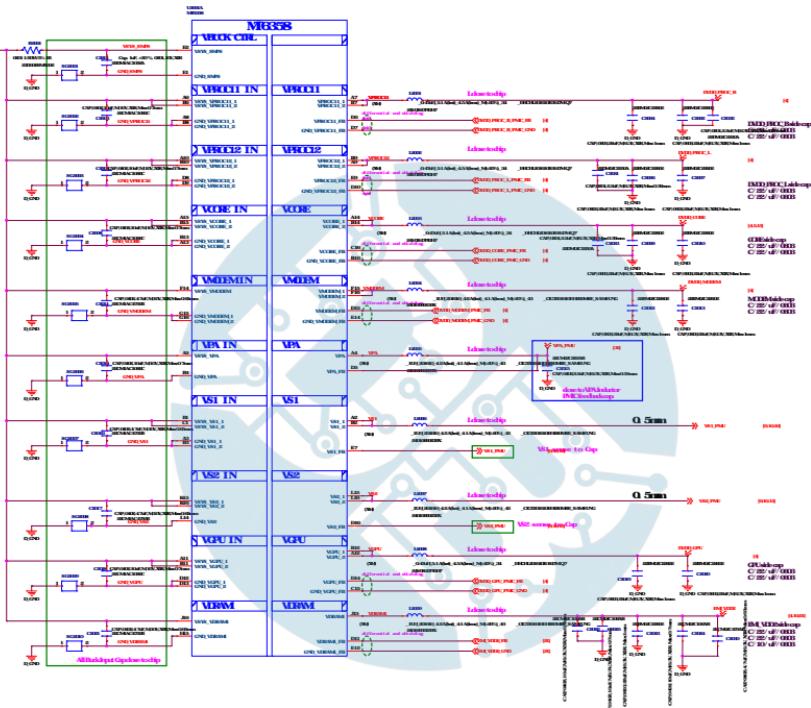
**Note 21-2** These poverince cannot IIO layout constraint, these CAP can be NC or mixed

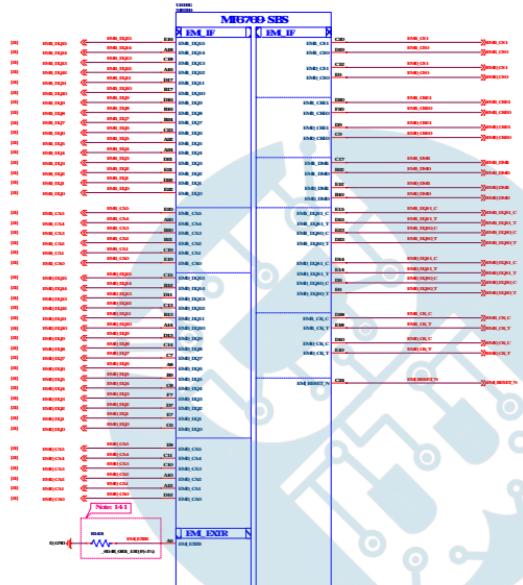
第10章



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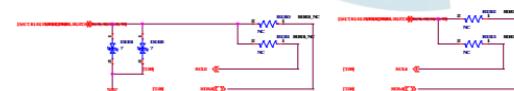
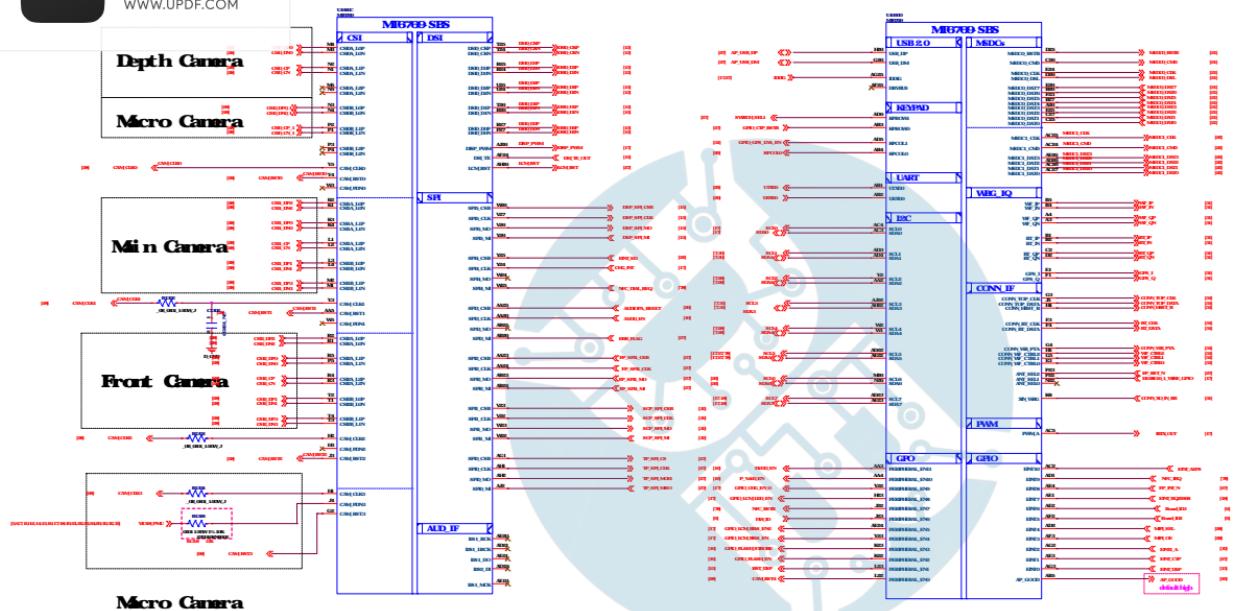
Schematic design notice of "14.BR.3" page

Note 14.1: R14.1 please select 0.47m(1%) resistor



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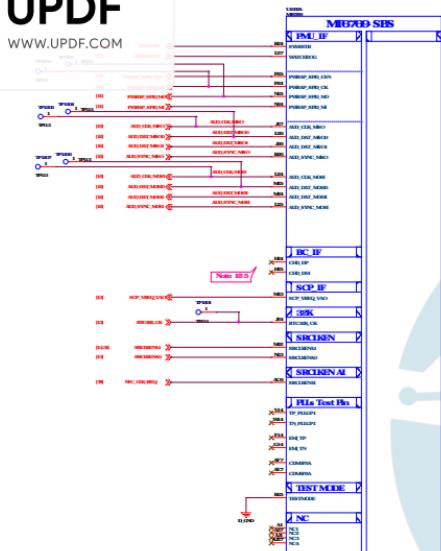
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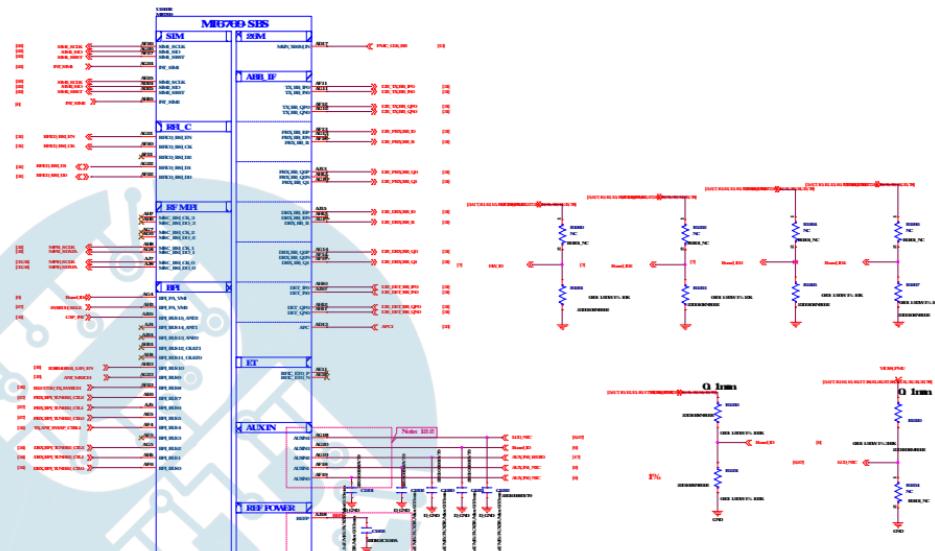
### Schematic design notice of "12 BB-1" user

Note 12-1: PWRAP, SPD, CSN, and "AUD DAT MOSI/D" are bootstrap pins to select which interface will be the JTAG pin out.

PWR/PD CSN	ALD DUE MOSID	JTAG Function	
default-PU	default-PD	AP_JTAG	MD_JTAG
H	IO	NA	NA
H	IO	SPD+ENB	SPZ+SP3
IO	IO	SPD+ENB	NA
		SPZ	NA

**Note 13.2** Toshanta 1uF capacitor in the AUNN ADC input to prevent noise coupling. It should be placed

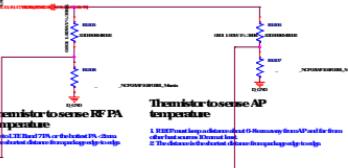
卷之三十一

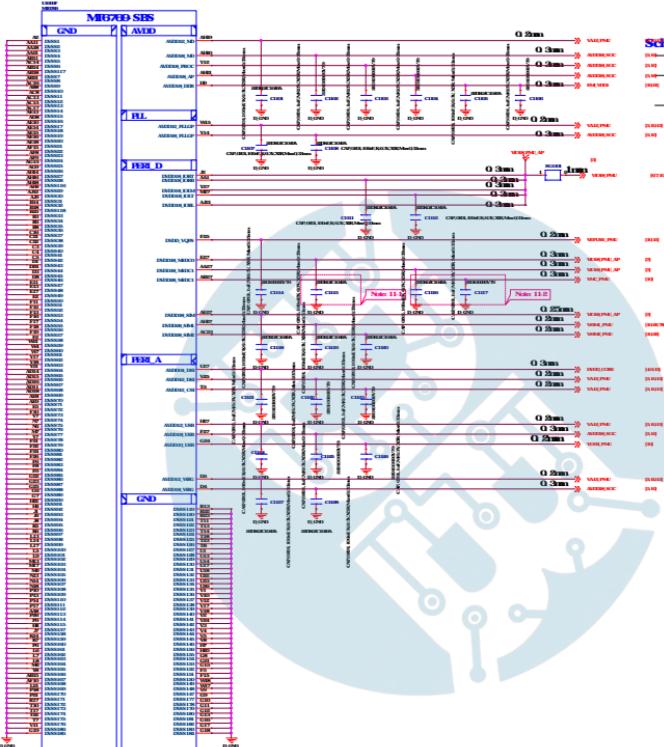


Note 134 HW info for DLR type fixtures in hot step (refer to EER HW design Notice)

ADD SYNC MSO	ADD CLK MSO	CAMPONI	PMC GDBvoltage	DDR Type
default-PD	default-PD	default-PD	VEMR / VEMAVE	DDR
No test pull	No test pull	No test pull	1.8V / 0.0V	IPaKcMP
No test pull	B1KpULLtoVIOHS	No test pull	0.7V / 1.8V	Reserved
B1KpULLtoVIOHS	No test pull	No test pull	1.8V / 0.7V	IP3dMDP
B1KpULLtoVIOHS	B1KpULLtoVIOHS	No test pull	1.8V / 1.8V	Reserved

**Note 13.5 Charger must have D/D pins for charging type USB detection**  
Charger must have at least 50mA USB current for All chargertype





Schematic designation of "11\_BB\_POWER\_IO" page:

Note 11-1: C1115 closed DMD88 MDCC 15mA

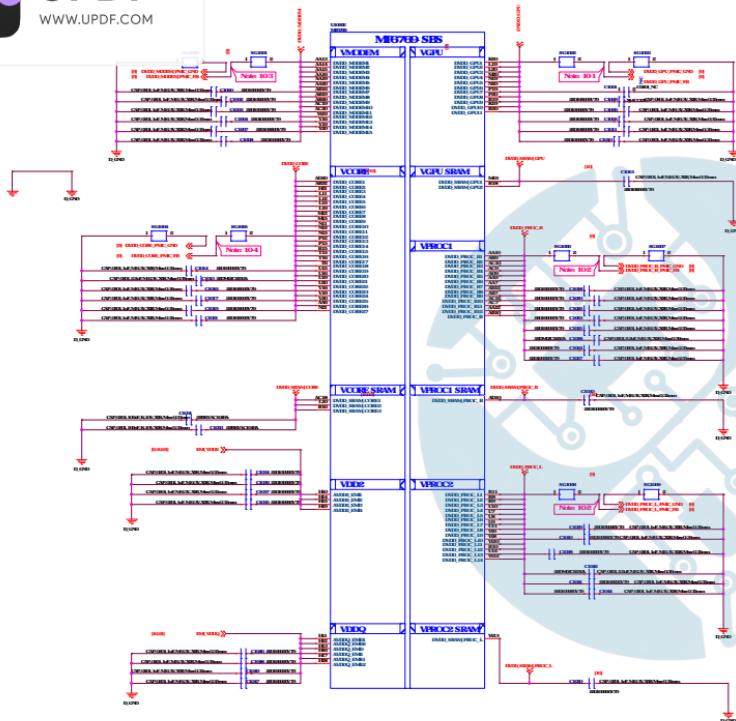
Note 11-2: C1116 closed DMD88 MDCC 15mA

C1117 closed DMD88 MDCC 15mA

A1022 : 5mA, 10mA, 20mA

VACUUM/AR 40mA

A1023 SOI 30mA



## Schematic design notice of "IO\_BB\_POWER\_PDN" page

- Note 101:** Differential pair of DQDQ GPU memory sense must be close to HPC ball. Bounce sense trace will GND shielding to PMC (Differential)
- Note 102:** Differential pair of DQDQ MCCM memory sense must be close to HPC ball. Bounce sense trace will GND shielding to PMC (Differential)
- Note 103:** Differential pair of DQDQ MCCM memory sense must be close to HPC ball. Bounce sense trace will GND shielding to PMC (Differential)
- Note 104:** Differential pair of DQDQ COMC memory sense must be close to HPC ball. Bounce sense trace will GND shielding to PMC (Differential)



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<b>Category</b>	<b>Item</b>
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**Page 04**

**V0 1 Release**

**(V0 1)**

**2019.01.11**

**(V0 2)**

**Page 12**

**Page 13**

**Page 69**

**Add CAMHDN3(GH010) Hwin for Note 12 4 Hwin for IIR type feature in bootstrap  
Delete R1007 and R1012 ext. pull for IP4X eMP**



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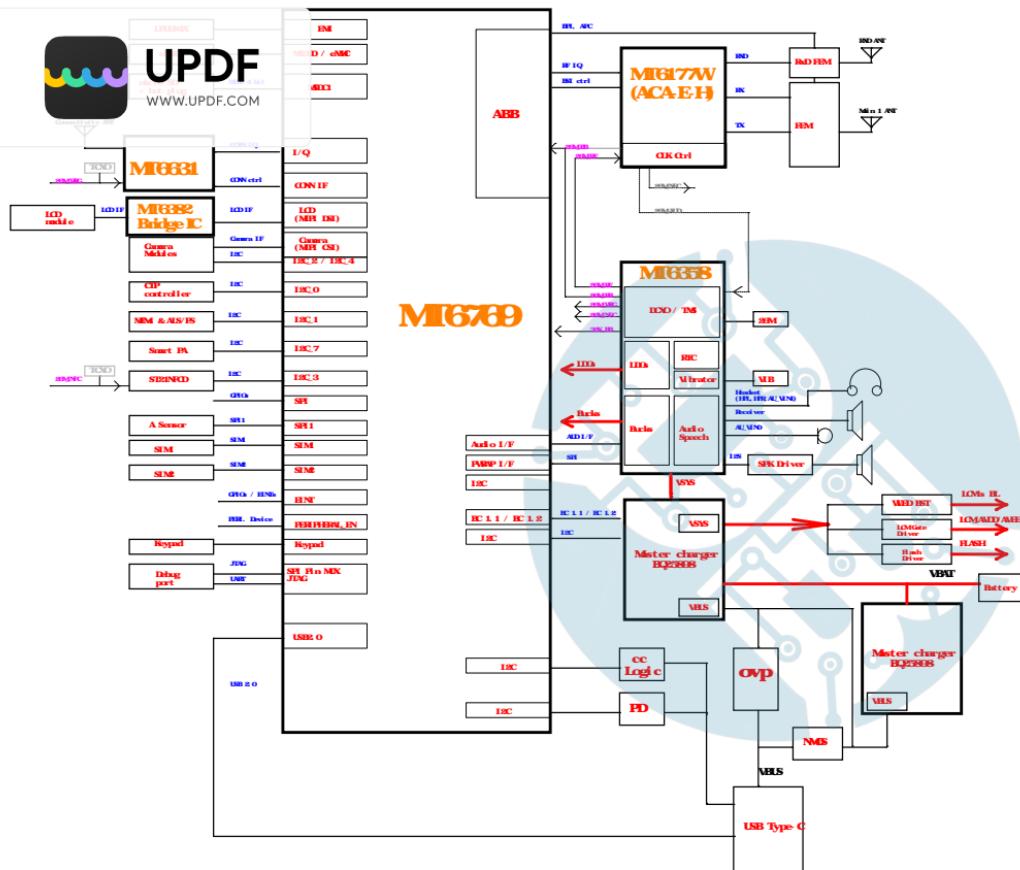
		Part Number	IC Spec	Support Doing	IC Slave Address / Write / Read (7bit mode)
EC 1 (EC) Microphone	AP	Microphone	IR	400Kps	Yes. 0x01 Value0xC / Read0xD
		Microphone	IR	400Kps	Yes. 0x02 Value0xC / Read0xD
		Microphone	IR	400Kps	Yes. 0x03 Value0xC / Read0xD
		Microphone	IR	400Kps	Yes. 0x04 Value0xC / Read0xD
		Audible Light Sensor	IR(IR2153)	400Kps	Yes. 0x01 Value0xC2 / Read0x23
EC 2 (EC)	AP	Rear Camera	CMOSIM	400Kps	Value0xD / Read0x09
		Rear Camera	CMOSIM	400Kps	Value0xD / Read0x0A
		Rear Camera	CMOSIM	400Kps	Value0xD / Read0x0B
		Rear Camera	CMOSIM	400Kps	Value0xD / Read0x0C
EC 3	AP	SAR			
		Front Camera	CMOSIM	400Kps	Value0xD / Read0x09
		Front Camera	CMOSIM	400Kps	Value0xD / Read0x0A
		Front Camera	CMOSIM	400Kps	Value0xD / Read0x0B
EC 4 (EC)	AP	IRUW	IR	400Kps	Value0xC / Read0xD
		IRUW	IR	400Kps	Value0xC / Read0xA
		IRUW	IR	400Kps	Value0xC / Read0xB
		IRUW	IR	400Kps	Value0xC / Read0xC
EC 5	AP	PD	RT720ASC	400Kps	Yes. 0x01 Value0xC / Read0xD
		CC Detect	FUSIONIMK	400Kps	Yes. 0x01 Value0xD / Read0x0E
		NFC			
EC 6	AP SSIM	AudioSmart PA	AM2510CH	400Kps	Yes. 0x01 Value0xC / Read0xD
		AudioSmart PA	AM2510	400Kps	Yes. 0x01 Value0xD / Read0xB
EC 7	AP	Master Charger	IQ2000D	400Kps	Yes. 0x01 Value0xD / Read0xD
		Slave Charger	IQ2000B	400Kps	Yes. 0x01 Value0xD / Read0xE

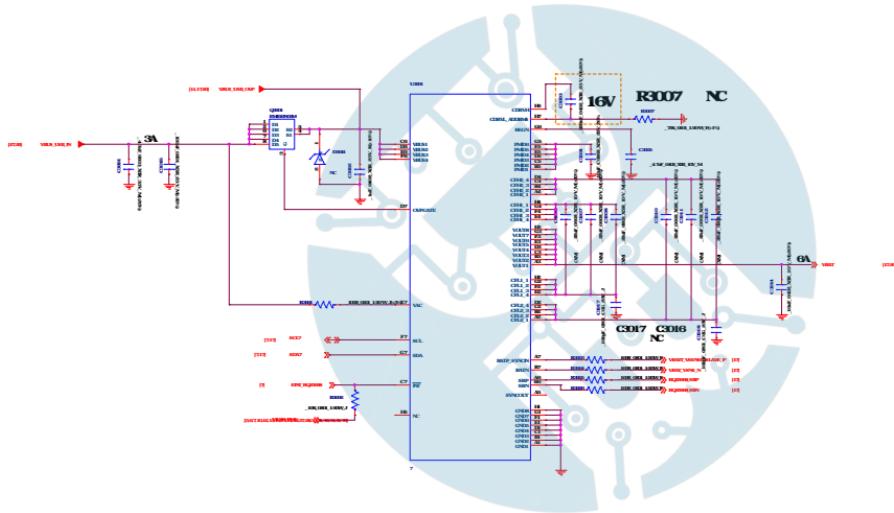
Note: IC Spec : Standard mode (100Kps) and Fast mode (400Kps), Fast mode Plus (1Mps) and High speed mode (3.4Mps)



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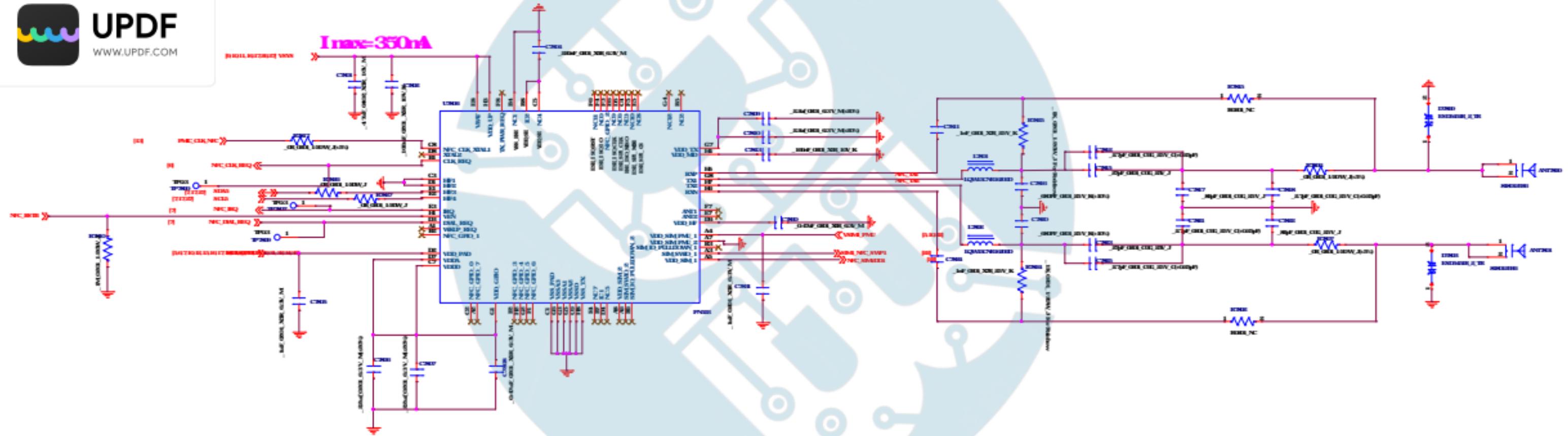


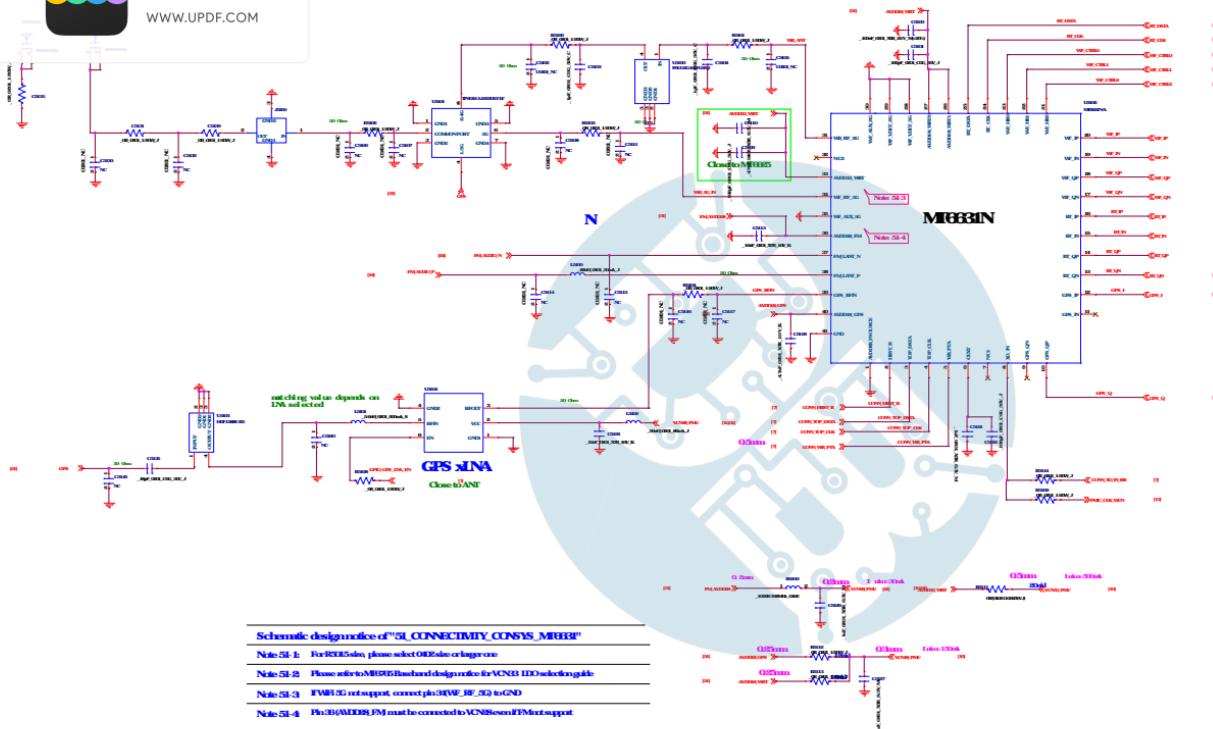


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Imax=350mA





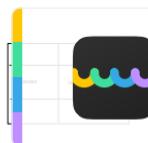
**Schematic design notice of "SL\_CONNECTIVITY\_CONVS\_MI63IN"**

Note SL-1: For RDO301s, please select ODE016 or ope016

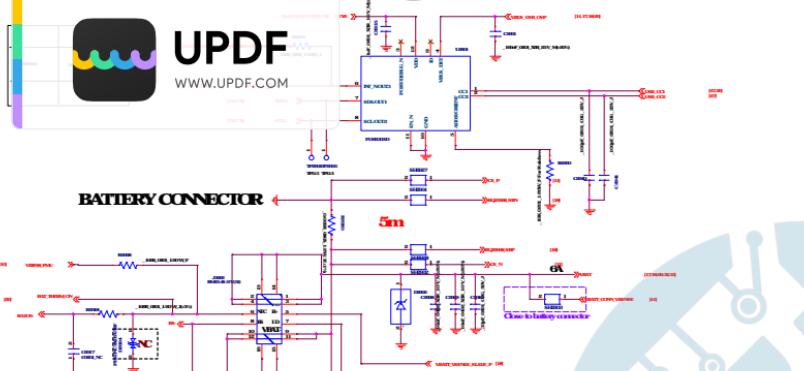
Note SL-2: Please refer to MI63IN board level design note for VCN1100 selection guide

Note SL-3: FVB10G not support connect pin(MWF\_RF\_02) to GND

Note SL-4: Pin(30)(ADDR0M) must be connected to VCN1100 pin(31) not support

**BATTERY CONNECTOR**

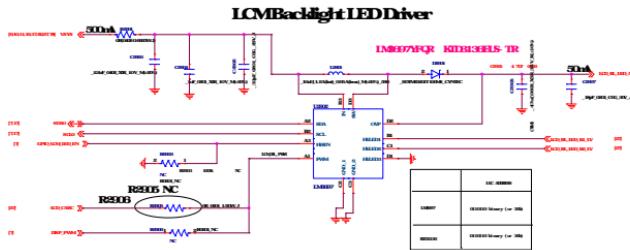
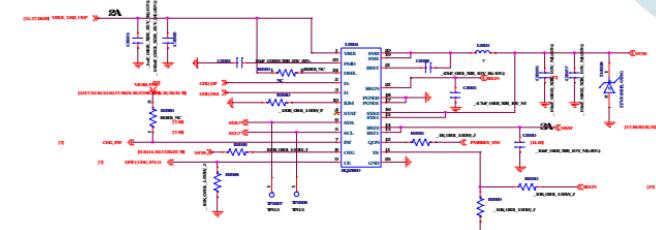
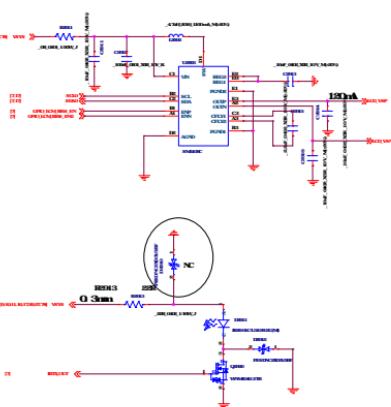
5m



	LC Address
x	0x00

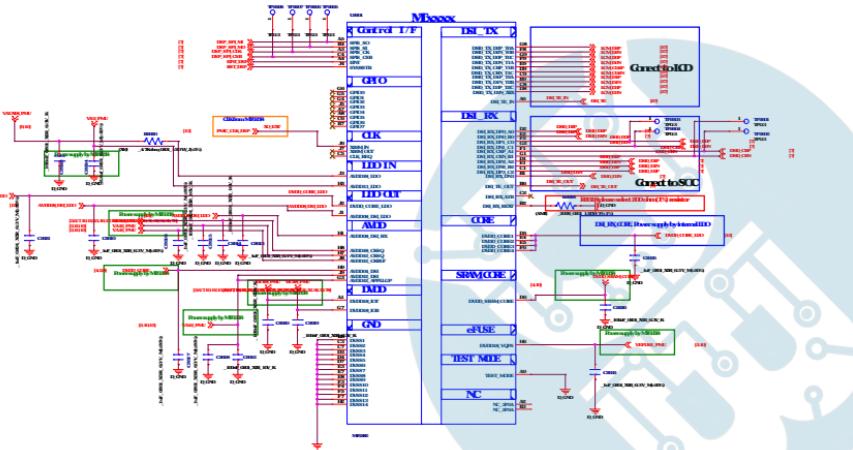
**Schematic design notice of "2) EXL\_VLED\_DB-FL-CHG-PD" page**

Note 10: For better ESD usage performance we used close suitable diodes for protection. Please refer to Stage device selecting guide V2Q provided by MKS.

**SWCharger****LCM as****SM300C**



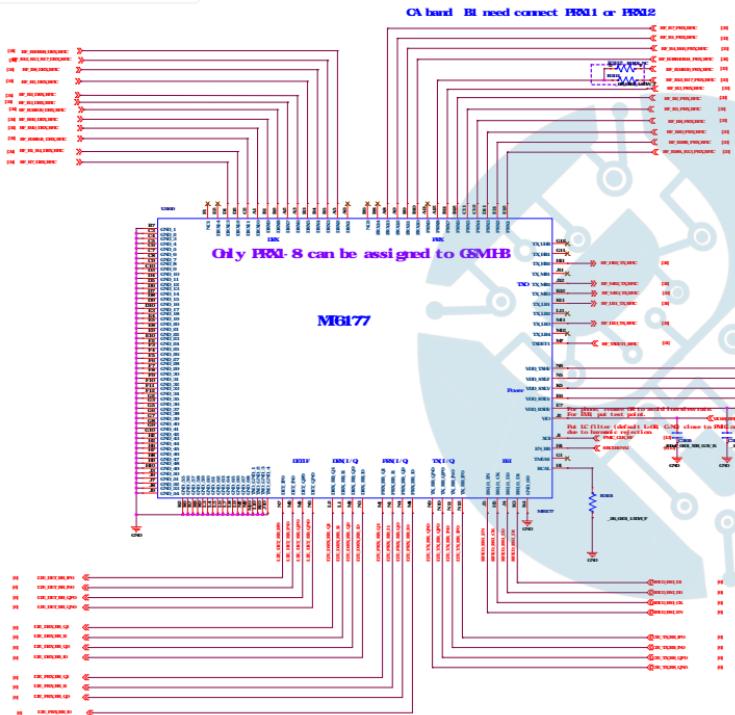
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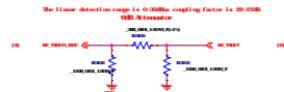
MT2522 Power Rail	Pinout
AVID08_08_LDO (LDO output)	AVDD08_08
DVID_CORE_LDO (LDO output)	Supply_DVID_CORE
DVID_CORE	By internal LDO
AVID08_VDD_08	By internal LDO
DS1S_HVDD_08	DS1S_HVDD_08
DS1S18_VDD	VDD18
DS1S18_IOD	
AVDD18_A24D	
AVDD18_A12D	
AVDD12_VDD	VDD12
AVDD12_APPLUG	
AVDD12_VREF	VREF12
AVDD12_VDD	VDD12
AVDD12_GND	GND12
AVDD08_VDD	VDD08
DS2M_IN	IO2_IOP
DS2M_OUT	X



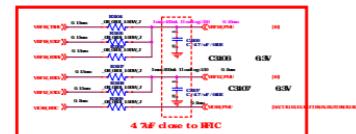
## Transceiver



## Attenuator for Detector



## Power For M6177

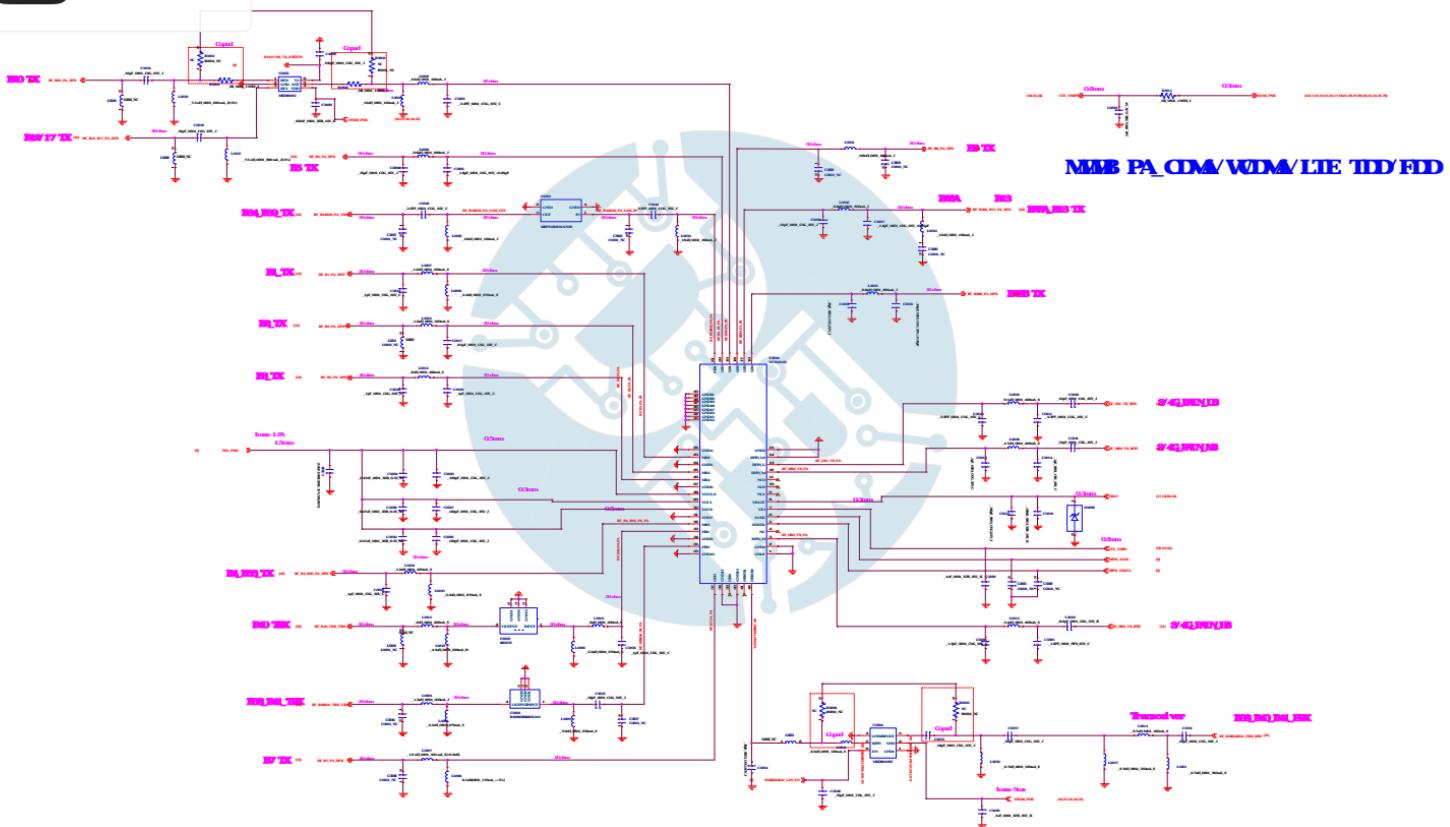


GND



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MIN ANT

TDM\_GSM

TRX LB

B5 TRX

B8 TRX

B9 TRX

B12 B17 TRX

CO PAD LPF

B28A B33 TRX

BOM B13/B28A LPF

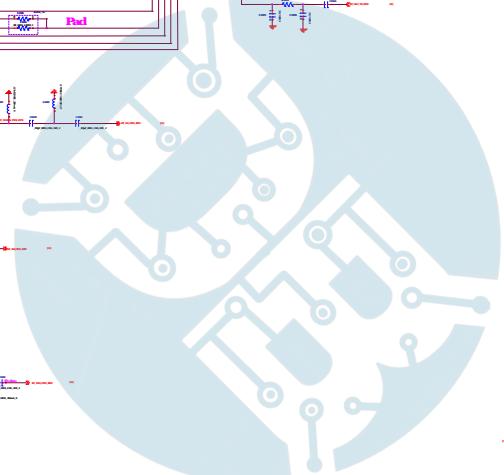
TRX MB

B1 B3 TRX

B2 TRX

B4 B6 B7 TRX

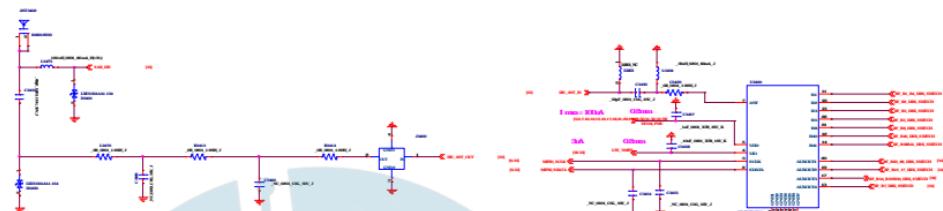
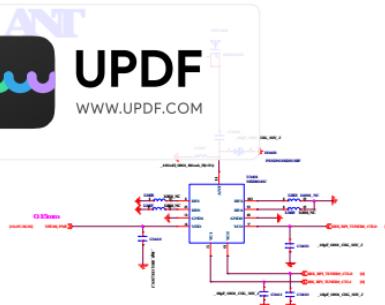
B34 B39 TRX





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DIV\_LB

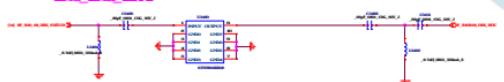
B5\_DRX



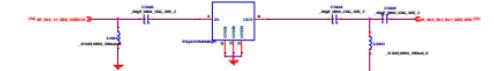
B8\_DRX



B30\_B28\_DRX

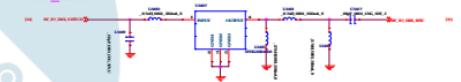


B12\_17\_DRX



DIV\_HB

B7\_DRX



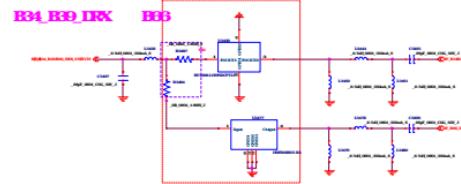
B10\_DRX



B88/B41\_DRX



B34\_B39\_DRX



B6

