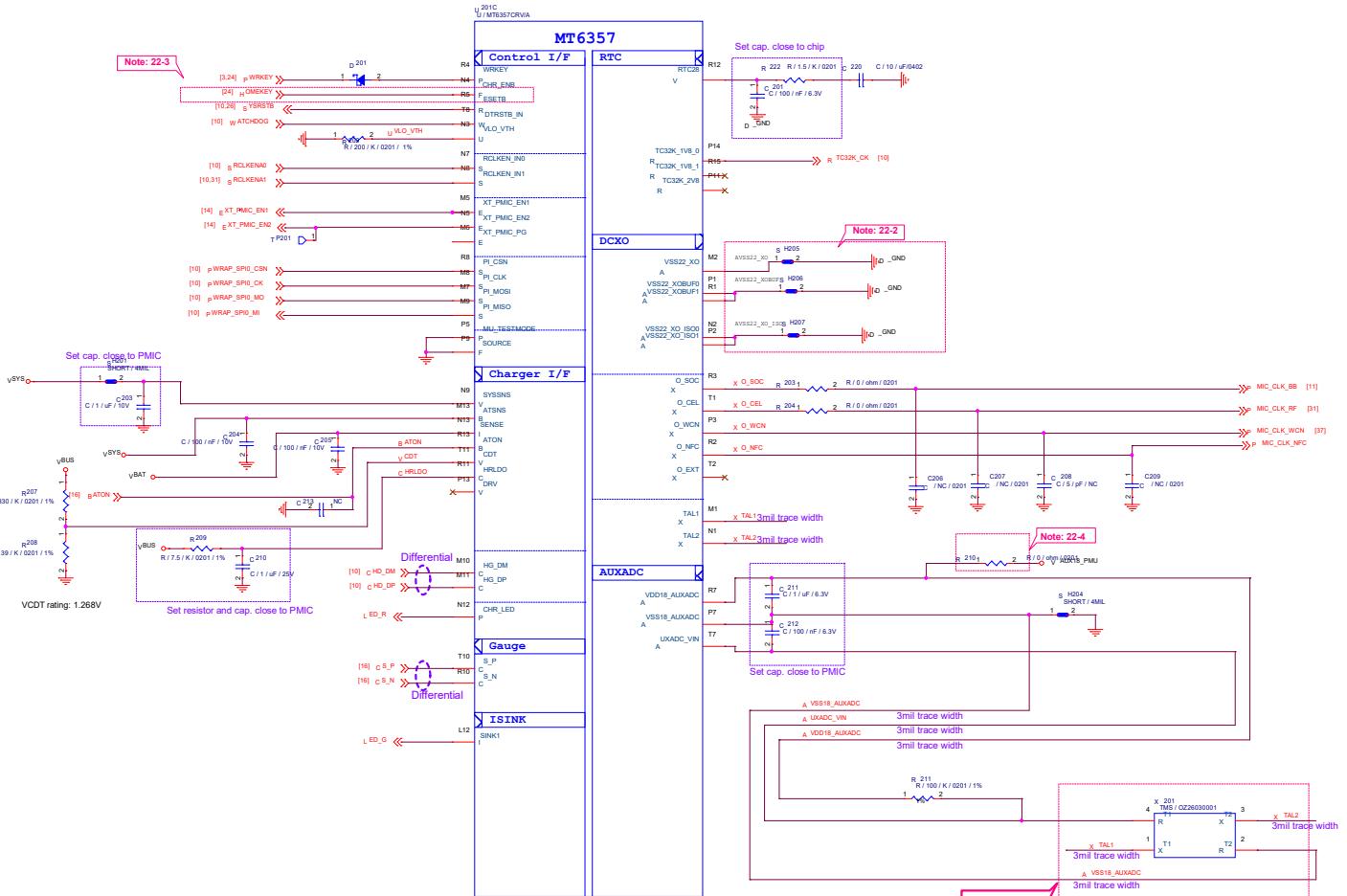


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Note 22-1: Please refer to MT6765_MT6357 Co-Clock Design Notice for co-layout guide

Note 22-2:

1. Please Connect P1 and R1 ball first and then to GND
2. Please Connect P2 and N2 ball first and then to GND
3. Please connect DCXO GND to main GND by independent L1-2 GND via.; DO NOT connect it through L1 GND

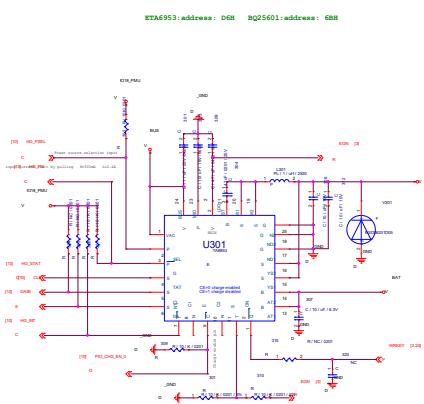
Note 22-3: Let floating if disable HOMEKEY function

Note 22-4: Please follow MT6765_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R210 can use 0 ohm to replace BEAD.

Note: 22-1 Route AVDD18_AUXADC, AUXADC_VIN, and AVSS18_AUXADC with 3mils width traces and well GND shielding

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Switching Charger Power Path

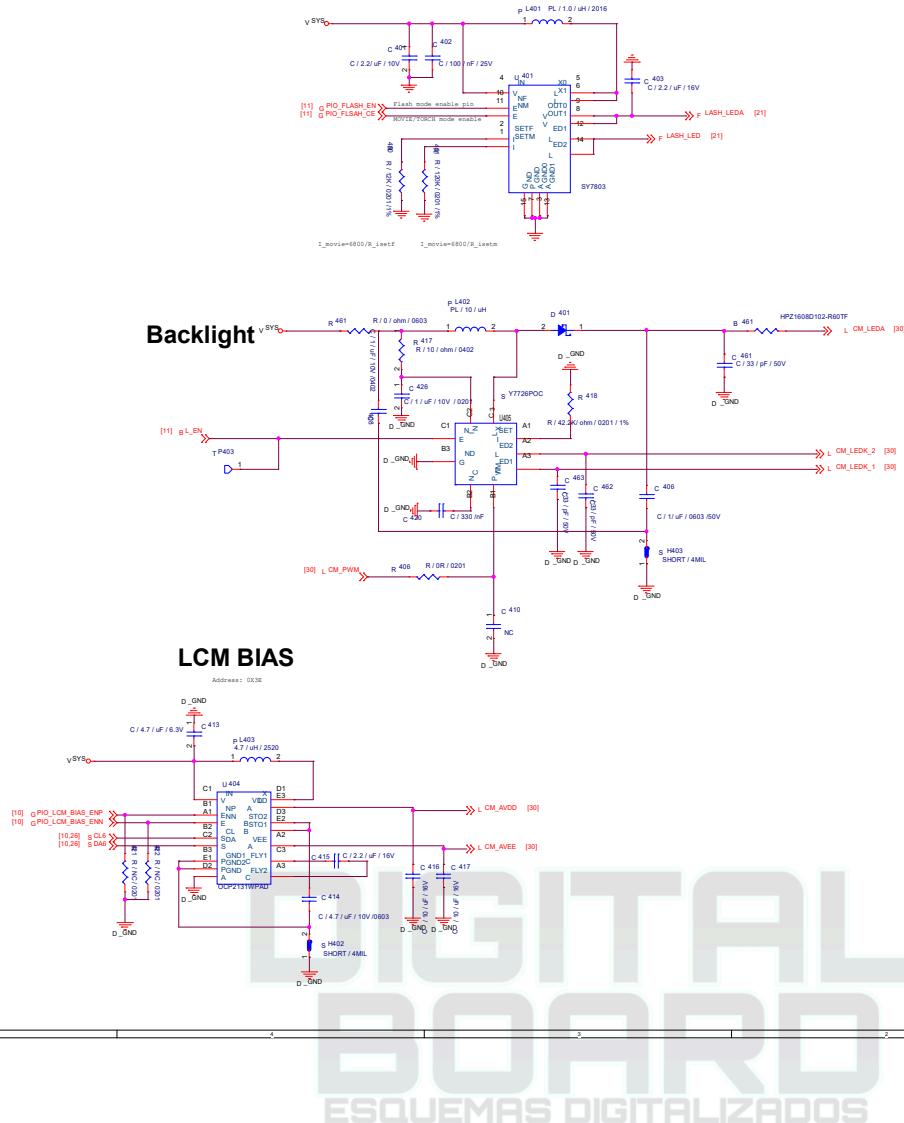


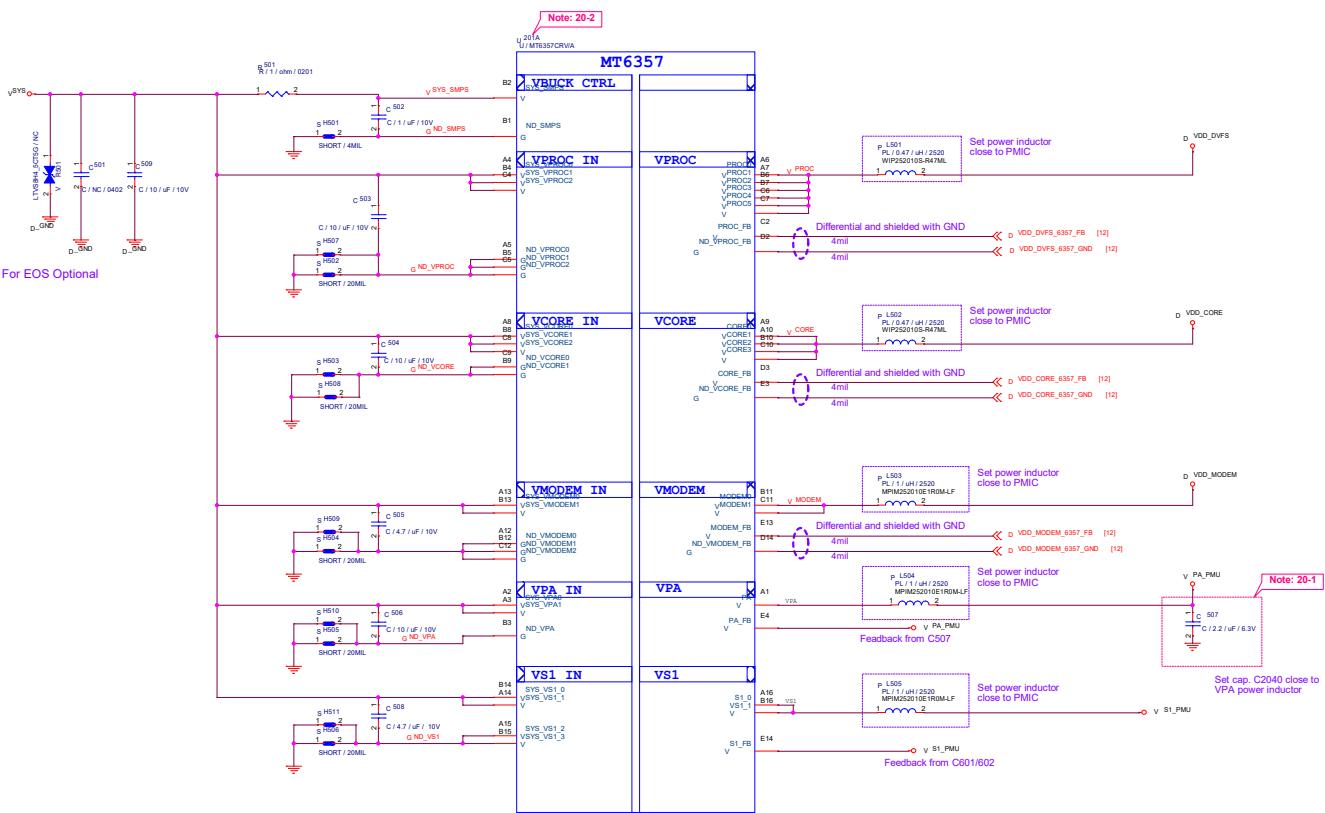
Page	Document Number	Document Location	Printed Date
1	1-POWER_Sub-MTC-General	1	Wednesday, April 21, 2010

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File Name: 1-POWER_Sub-MTC-General
Version: MTK Confidential

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Flash LED Driver





Note 20-1: C507, please choose 0402 size

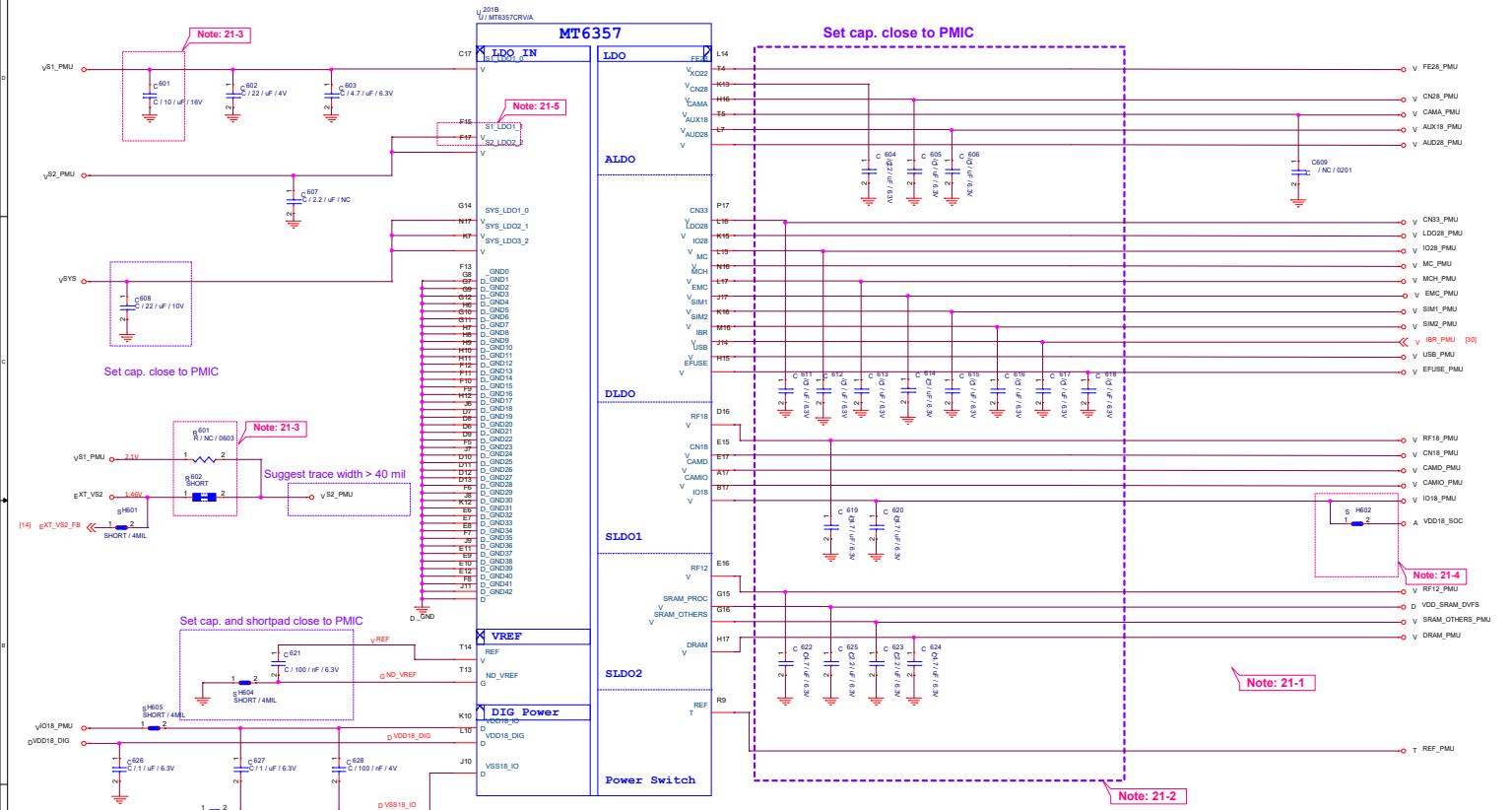
Note 20-2: PMIC Part number notice for MT6765/62/61 platform

MTK Platform	PMIC
MT6765 / 62	MT6357 CRV
MT6761	MT6357 MRV

REV	V1.0
DATE	Wednesday April 01 2020
DOCUMENT NUMBER	POWER_MT6357_Buck

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1. "Typical Cap" defined in design notice is the minimum cap, to LDO Cout. 2.
 NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm)
 => value and placement of Cap, please refer design notice



Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed.
 Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

Note 21-3: Ext Buck BOM option

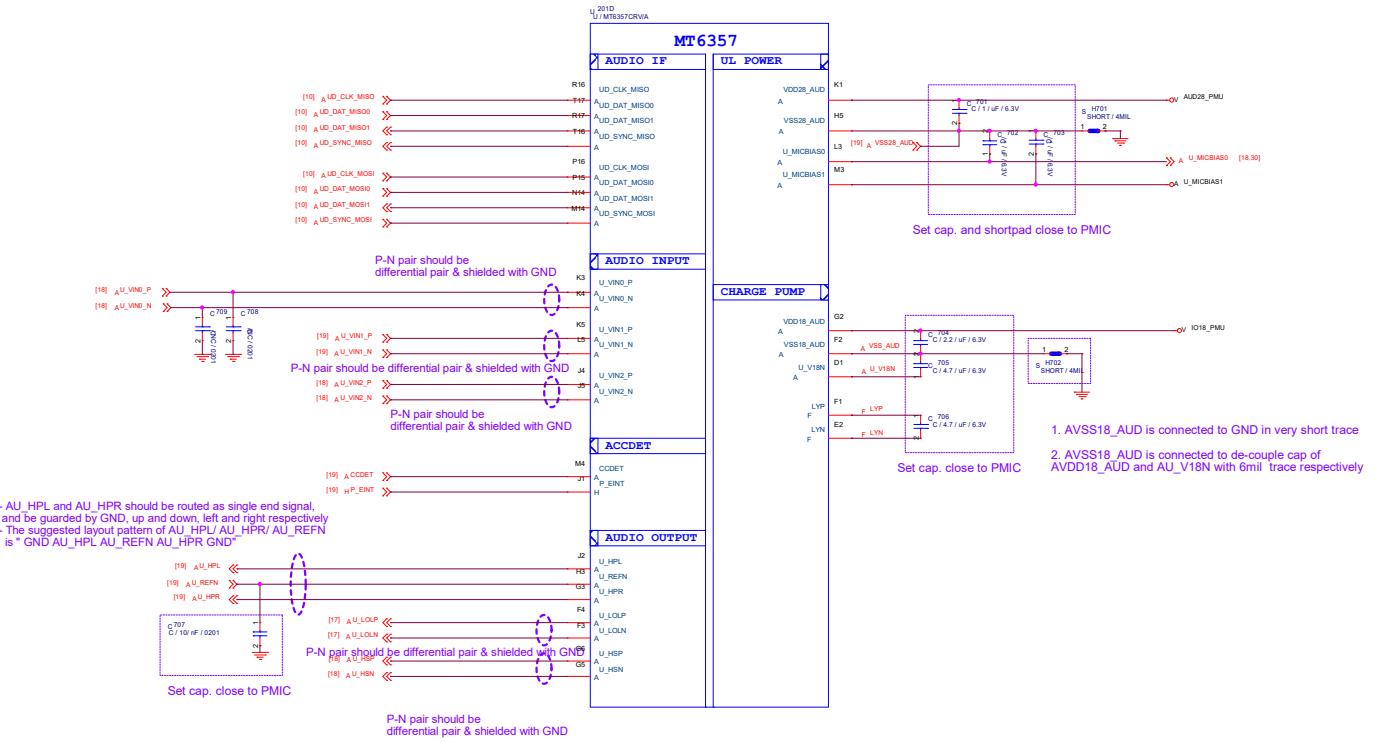
	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C601	10uF	22uF, 0603
R602	0-ohm, 0603	NC
R601	NC	0-ohm, 0603

Note 21-4: Please set SH602 and SH603 close to C620, making star connection among VIO18_PMU, AVDD18_SOC, and EMI_VDD1 near to LDO cap. C620
 Please also refer to MT6357 design notice for further detail design information

Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V

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C		Wednesday, April 17, 2024	POWER_MT6357_LDO	1/28

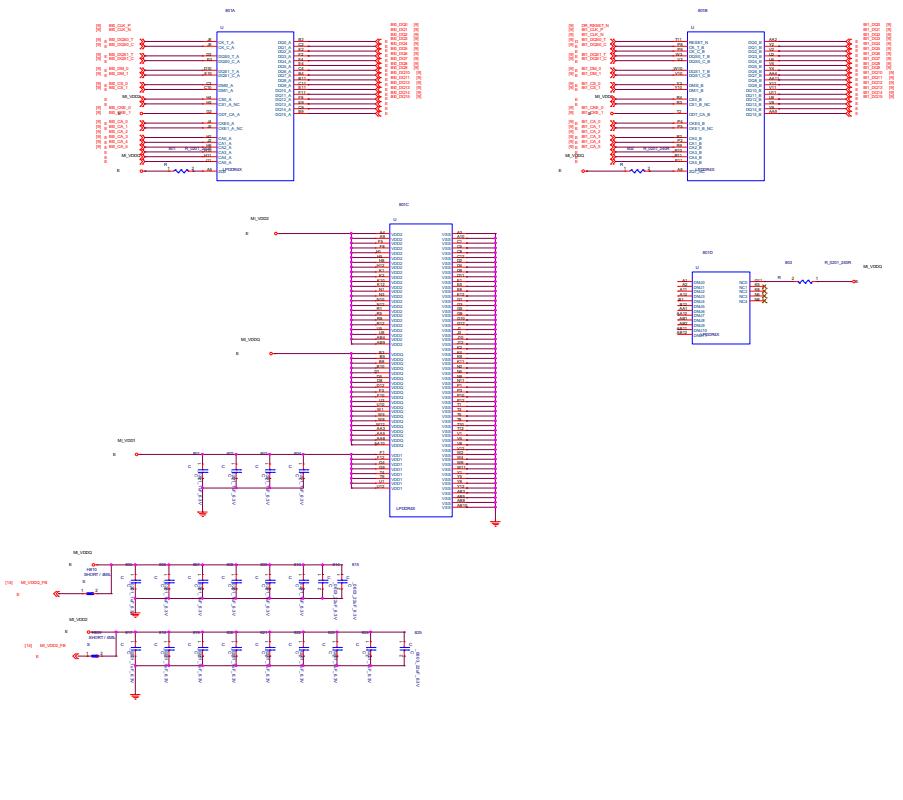
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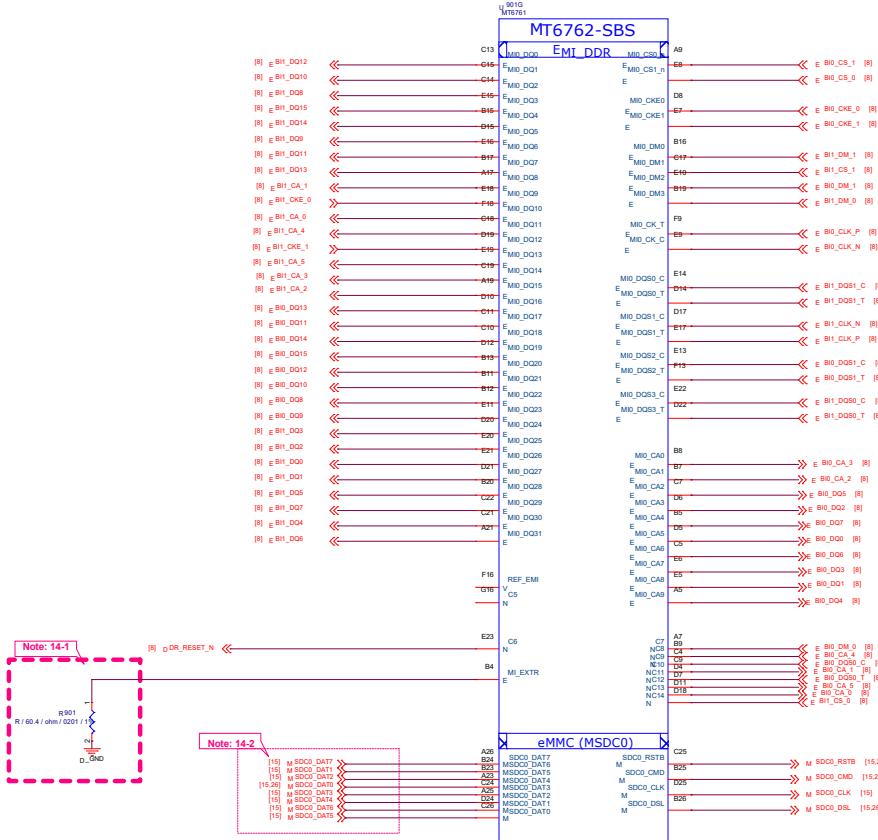
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Last	Wednesday, April 01, 2020	Sheet	1 / 1



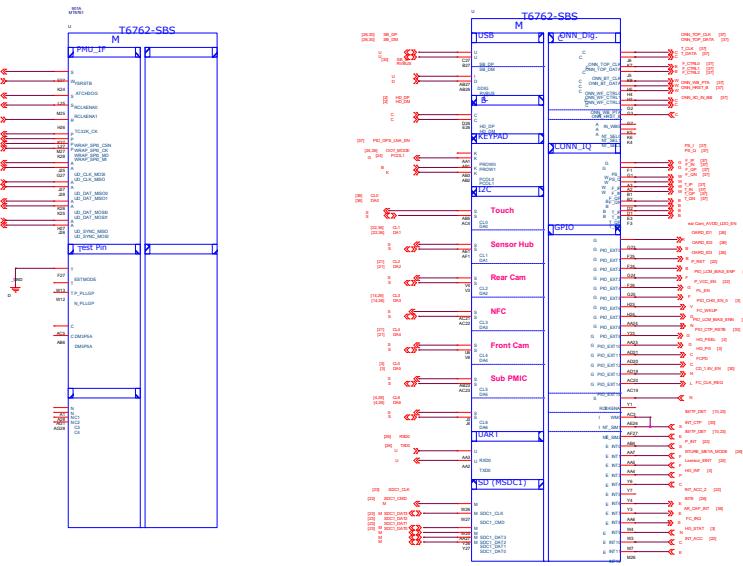
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Tech Annex	
Rev C	Document Revision MT6761_EB1

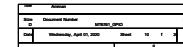
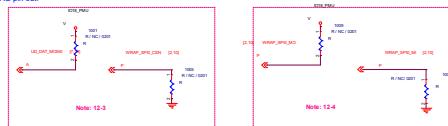


Note 12-3: "PWRAP SPI0 CSN" and "AUDI DAT MOS#0" are bootstrap pin to select which interface will be the JTAG pin out.

PWRAP SPI0 CSN		AUDI DAT MOS#0	JTAG Function
defaultPU	defaultPO	N/A	NO JTAG
HI	LO	SPDIF_HBTB	SPI1-SPI3
LO	HI	SPDIF_HBTB	N/A
LO	HI	SPDIF_CTI	N/A

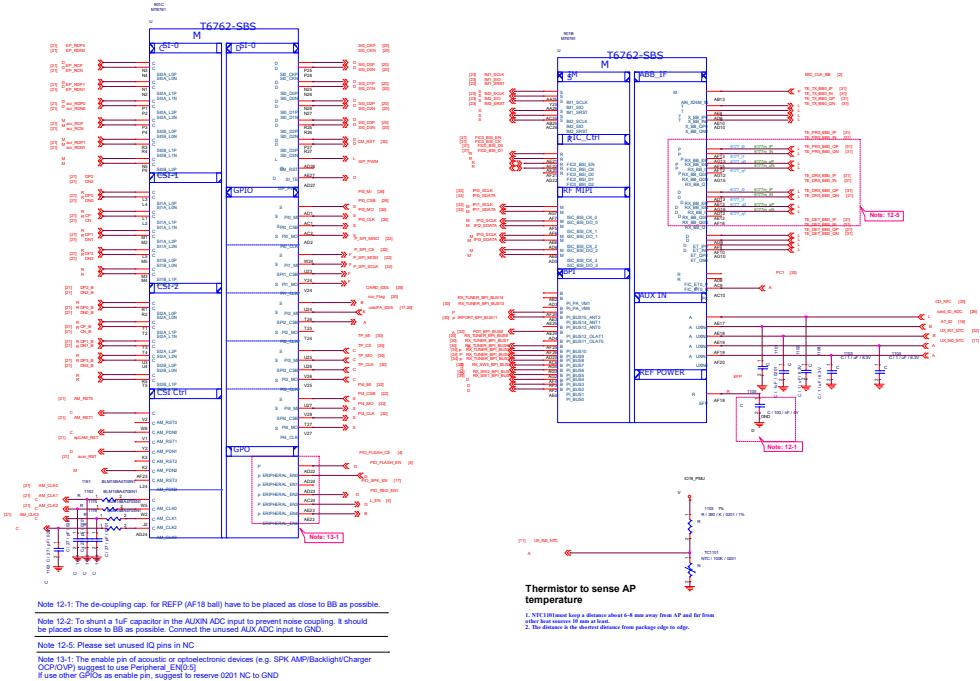
Note 12-4: PWRAP SPI0 MI is DDR type feature in bootstrap

PWRAP SPI0 MI		PWRAP SPI0 MO	Bootstrapping interface
defaultPU	defaultPO	DDR	MSDC0 p/m mux
HI	LO	LPDDR3	follow LP3 Ref SCH
LO	HI	LPDDR4X	follow LP4X Ref SCH

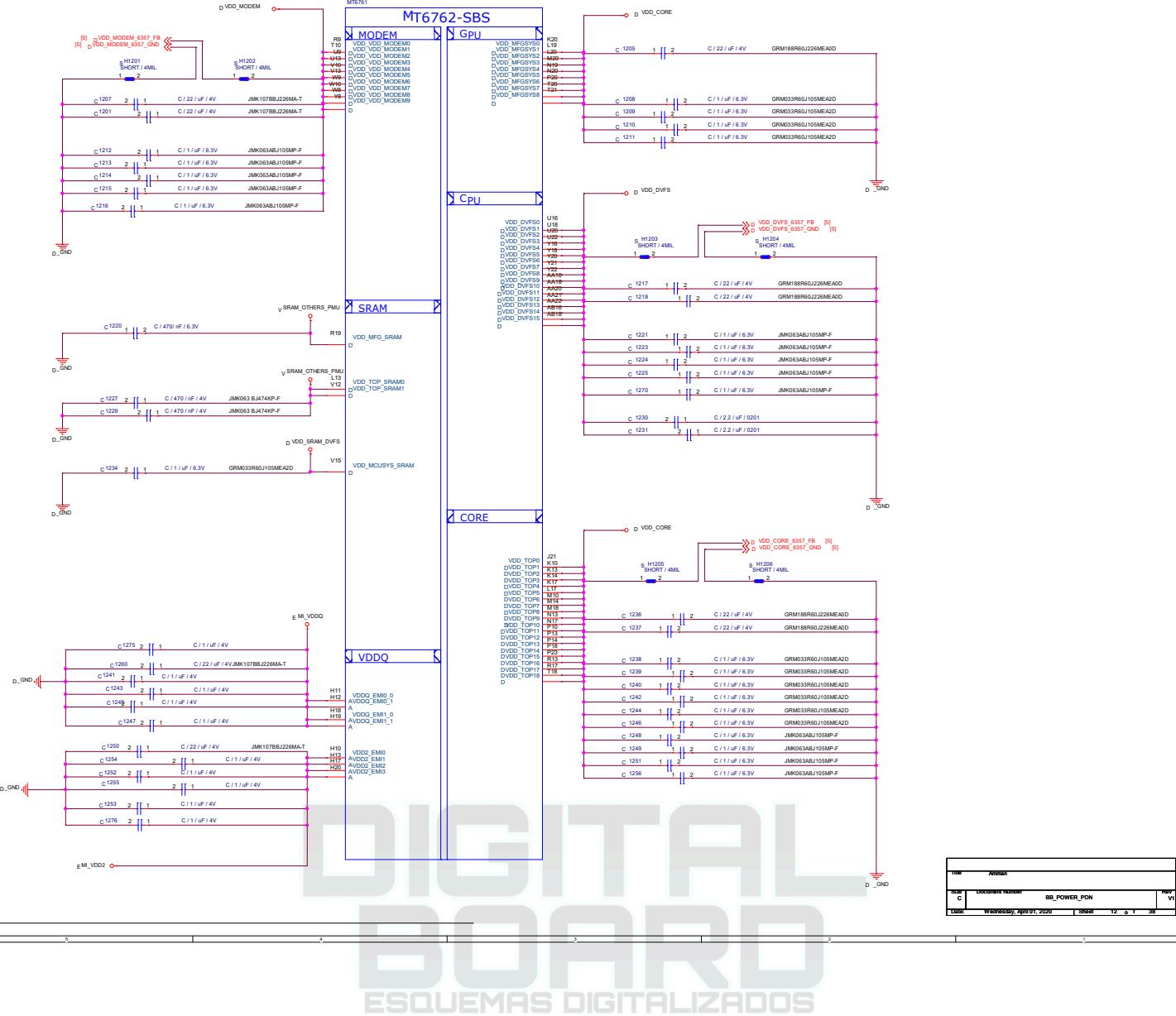


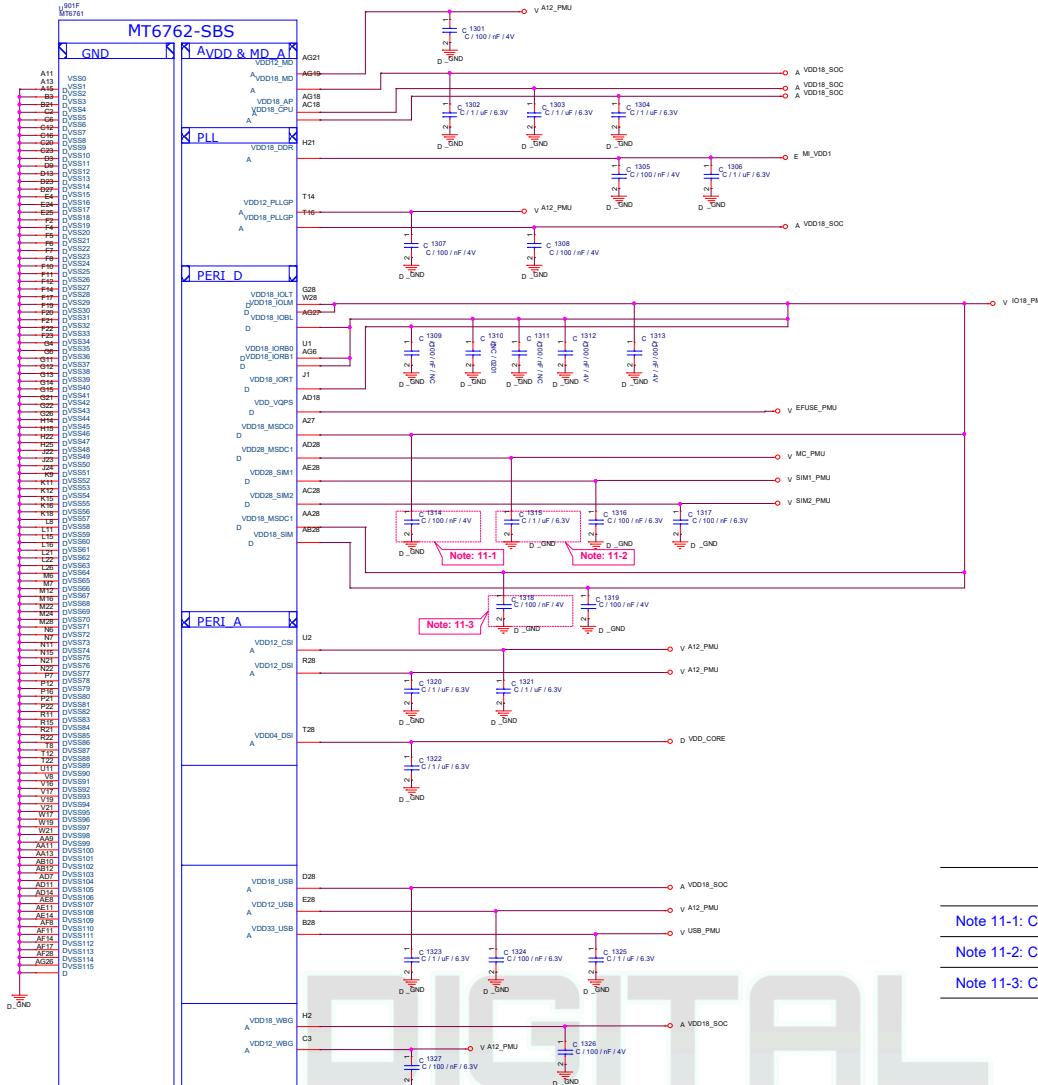
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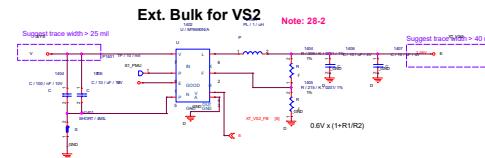
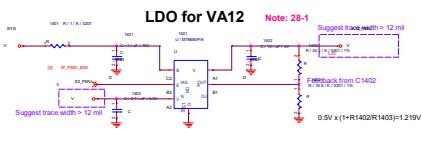


Note 11-1: C1314 closed DVDD18 MSDC0 150mil

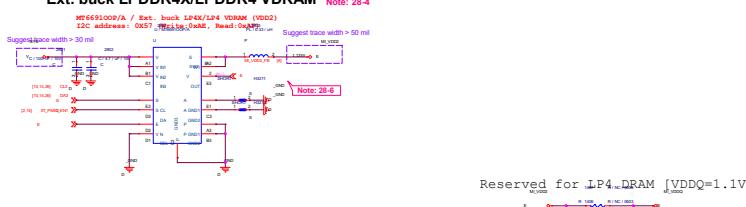
Note 11-2: C1315 closed DVDD28 MSDC1 150mil

Note 11-3: C1318 closed DVDD18_MSDC1 150mil

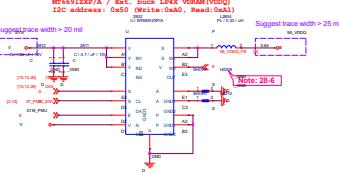
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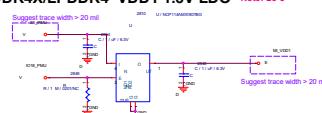
Ext. buck LPDDR4X/LPDDR4 VDRAM Note: 28-4



Ext. buck LPDDR4X VDDQ Note: 28-4



LPDDR4X/LPDDR4 VDD1 1.8V LDO Note: 28-5

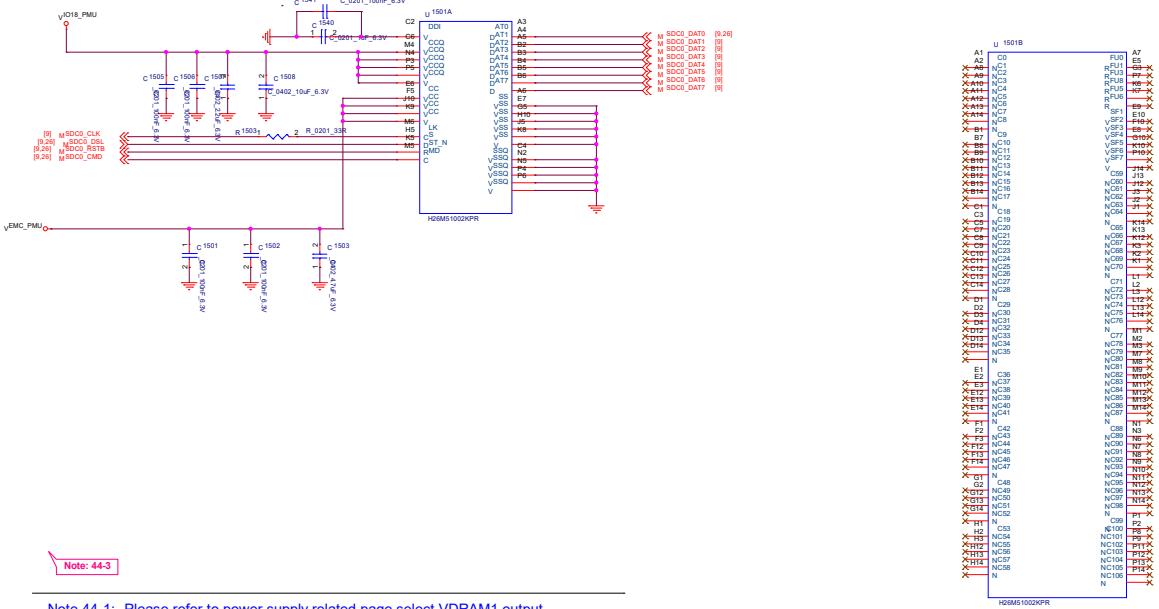


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Note 28-1: VA12 Layout placement please close to AP

Note 28-2: VS2 Buck Layout placement please close to PMC: MT6357, only used for MT6762, NC for MT6761



Note: 44-3

Note 44-1: Please refer to power supply related page select VDRAM1 output voltage properly for LPDDR3

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to GND

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4: VDD2 VDDQ VDDCA decoupling cap: closed to DRAM ball.
For other cap for PMIC [-10uF, at PMIC page];
please also refer to MMD and layout guide for placement.

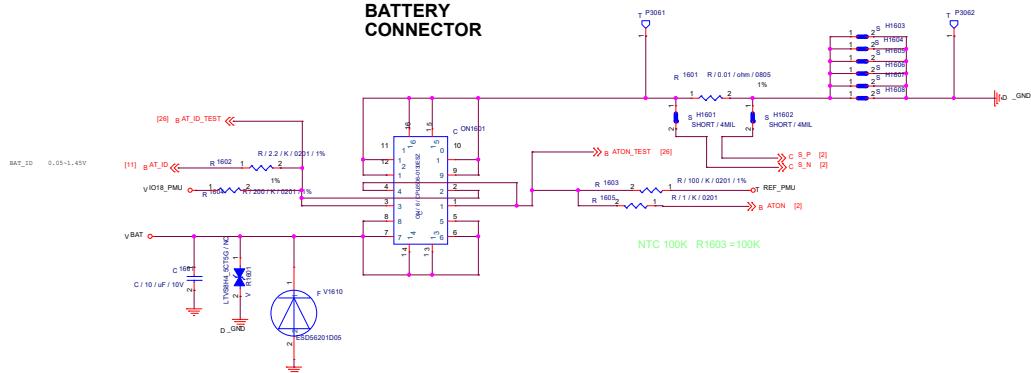
Note 44-5: Please check MT6765, MT6762 and MT6761's capacitor value.

Project	C1517	C1418
MT6765	2.2uF	1uF
MT6762	2.2uF	1uF
MT6761	0.1uF	0.1uF

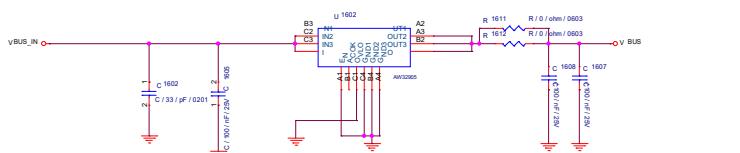
Task	Annex
Sub	Document Number
C	Memory_eMMC_LPDDR3
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BATTERY CONNECTOR



OVP

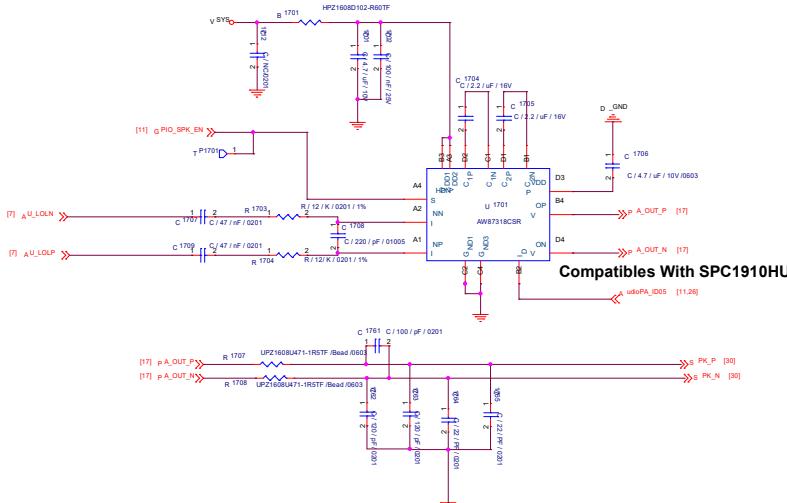


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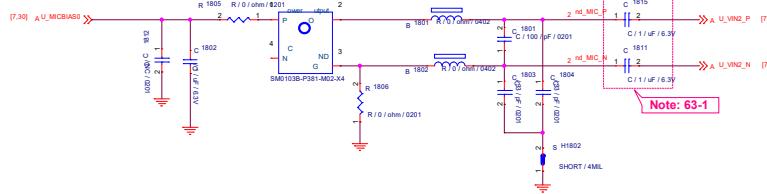


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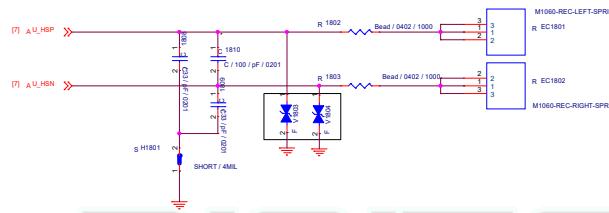
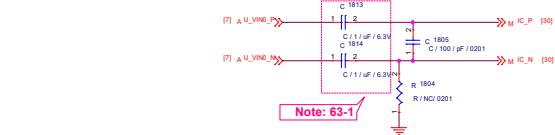
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MIC2



MIC1

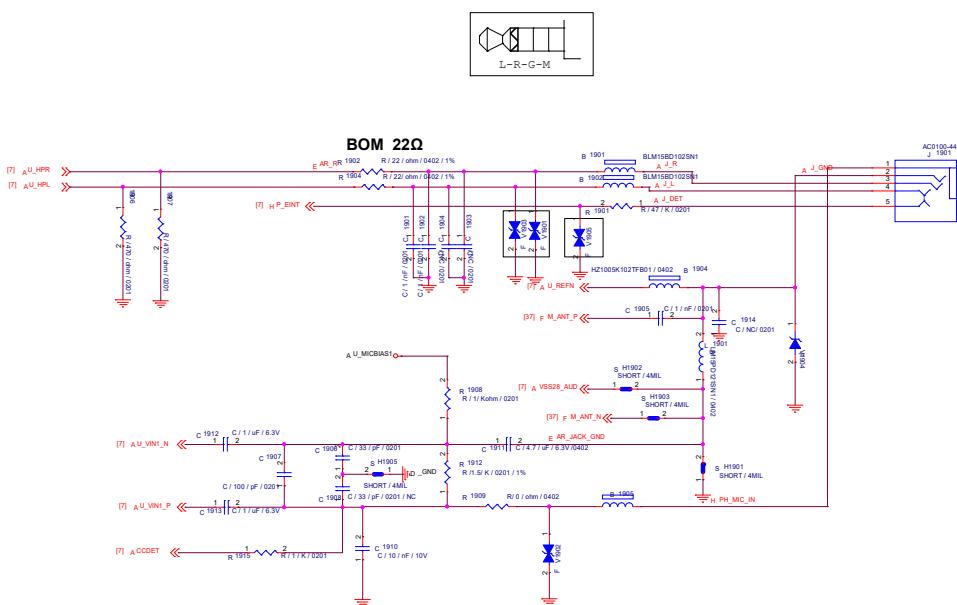


Schematic design notice of "63_PERI_AUDIO_IO" page.

Note 63-1: 1 uF for ACC mode
0 ohm for DCC mode

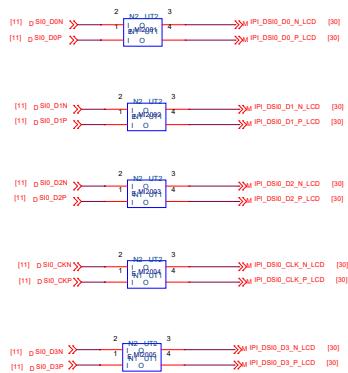
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3.5mm Headphone Jack



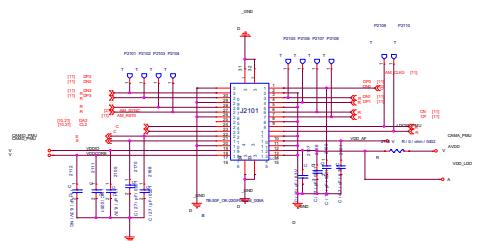
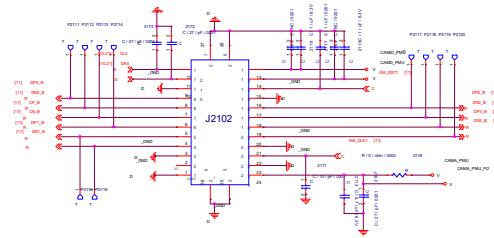
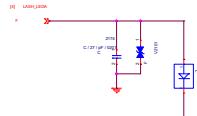
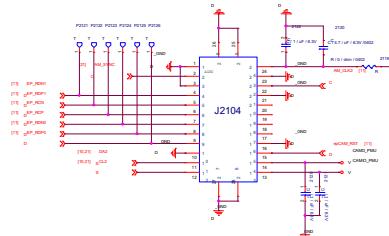
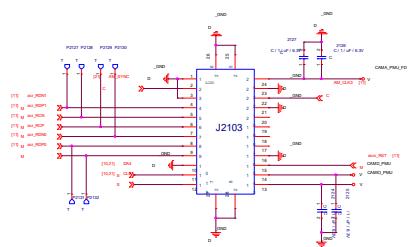
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Main LCM



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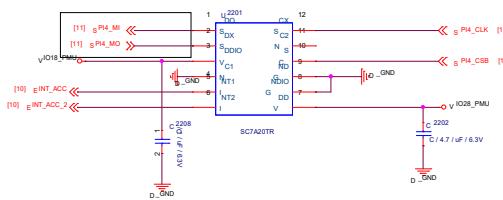
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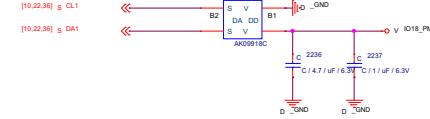
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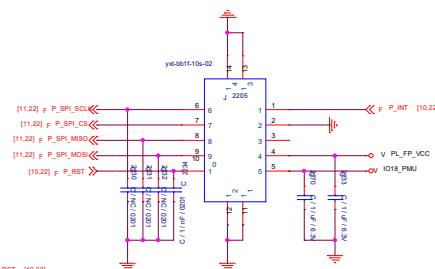
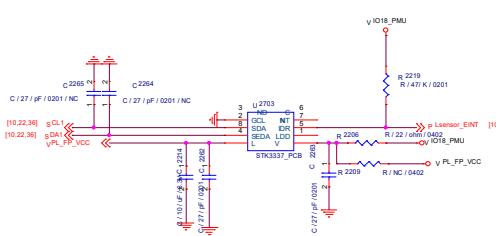
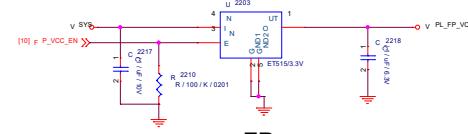
G-Sensor



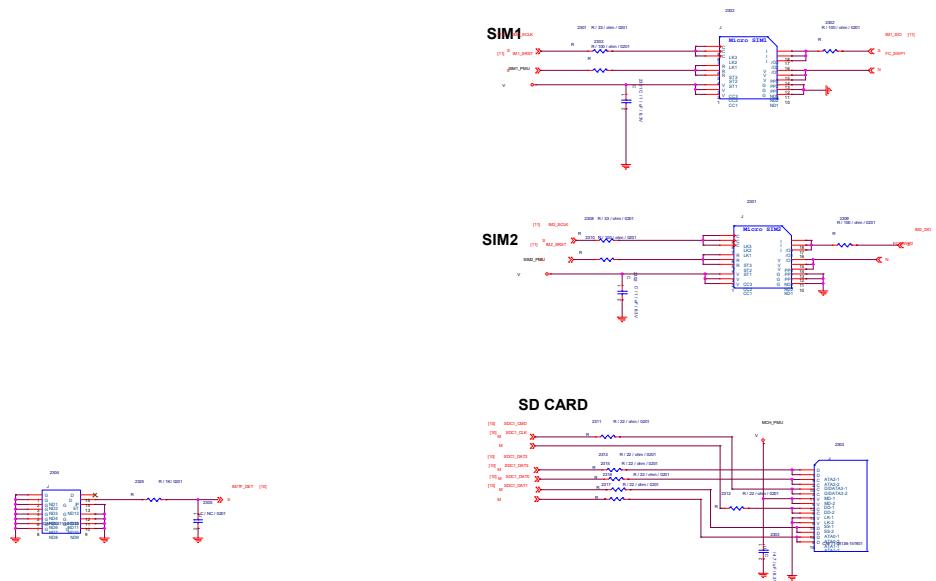
M SENSOR



FP



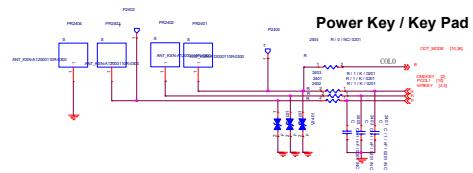
The diagram illustrates a digital logic circuit. It features a 4-to-16 decoder (74138) with four enable inputs labeled A, B, C, and D. The outputs of the decoder are labeled S₀ through S₁₅. Below the decoder is a 4-bit counter (74161) with its clock input (CLK) connected to ground. The counter's outputs are labeled Q₀ through Q₃. The circuit also includes a 4-to-16 decoder (74138) with four enable inputs labeled E, F, G, and H. Its outputs are labeled S₀' through S₁₅'. The outputs S₀ and S₁ from the first decoder are connected to the enable inputs E and F of the second decoder, respectively. The outputs S₂ and S₃ from the first decoder are connected to the enable inputs G and H of the second decoder, respectively. The outputs S₀' and S₁' from the second decoder are connected to the enable inputs A and B of the first decoder, respectively. The outputs S₂' and S₃' from the second decoder are connected to the enable inputs C and D of the first decoder, respectively.



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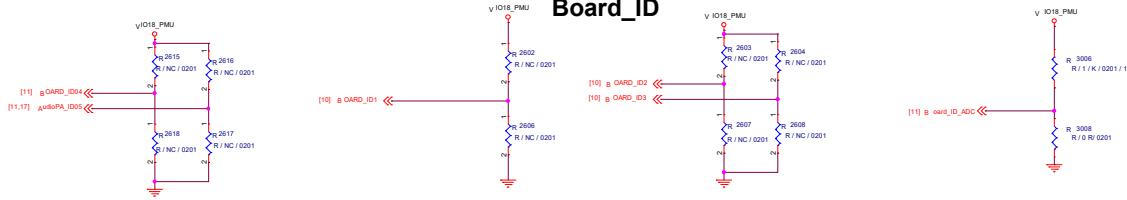
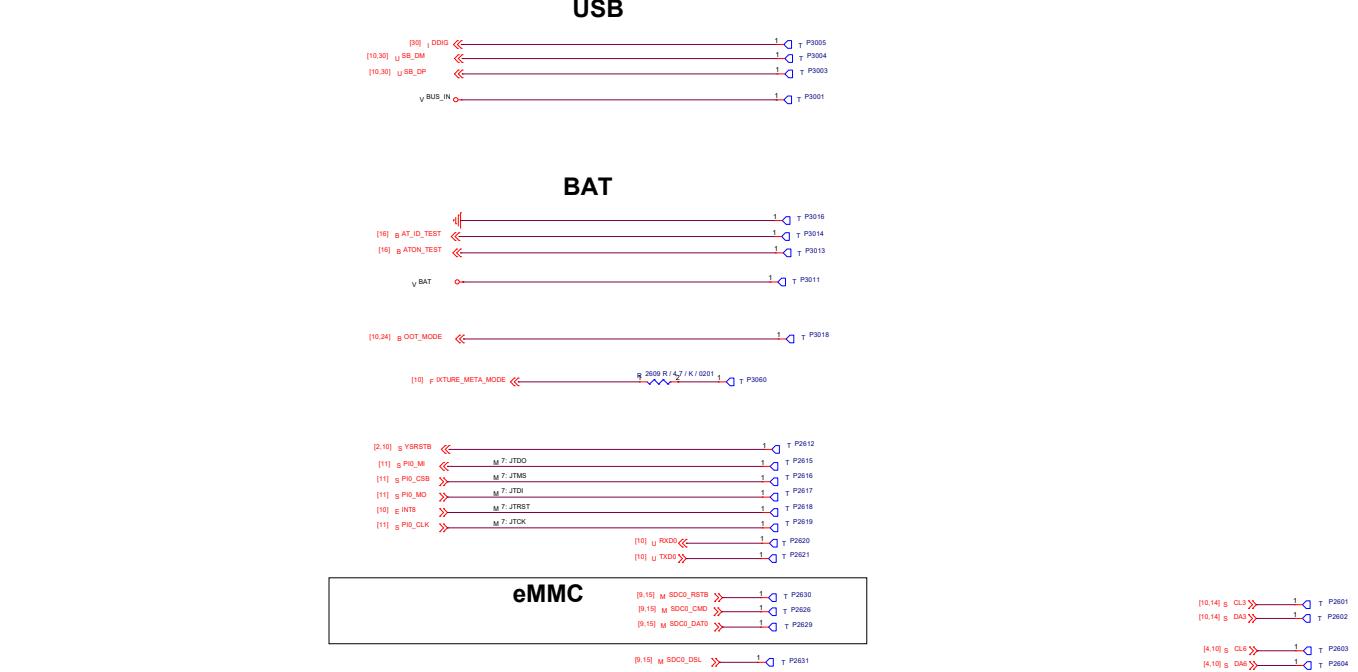
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Note 52-1: NFC host I/F and power info are listed in the above connector, NFC COB reference schematic is in the file named "MTK ST NFC Reference Schematic_20170809"

Note 52-2: When NFC is applied, please keep
1. 0ohm NC between VSIM1_PMU and SIM1_VCC
2. 0ohm NC between VSIM2_PMU and SIM2_VCC

Note 52-3: When NFC is applied, please follow NFC COB reference schematic to draw NFC COB schematic

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Shielding frame

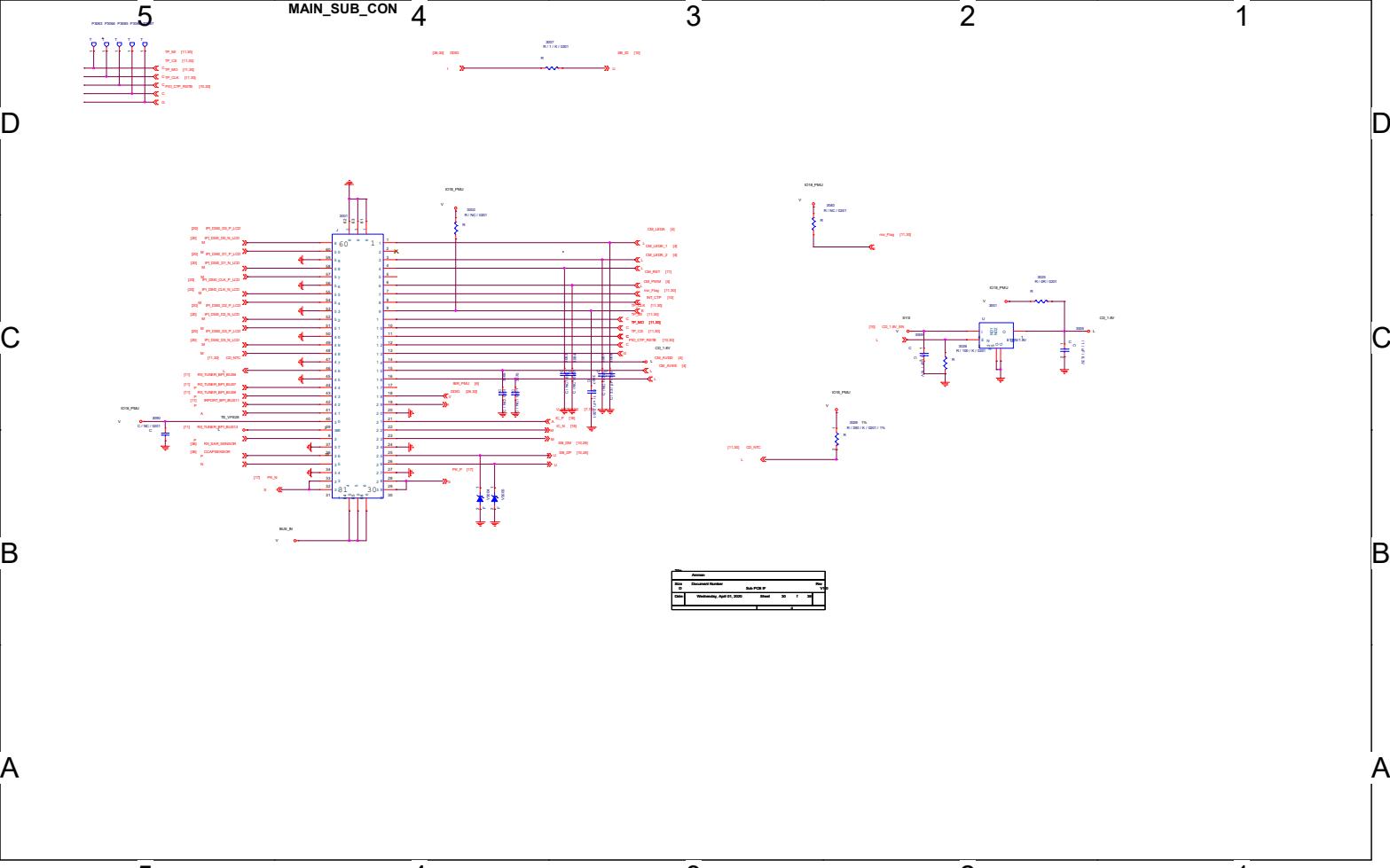
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S H2902
S H2901
S H2907
S H2906
S H2905
S H2904

M 2901 1
Mark
M 2903 1
Mark
M 2902 1
Mark
M 2904 1
Mark

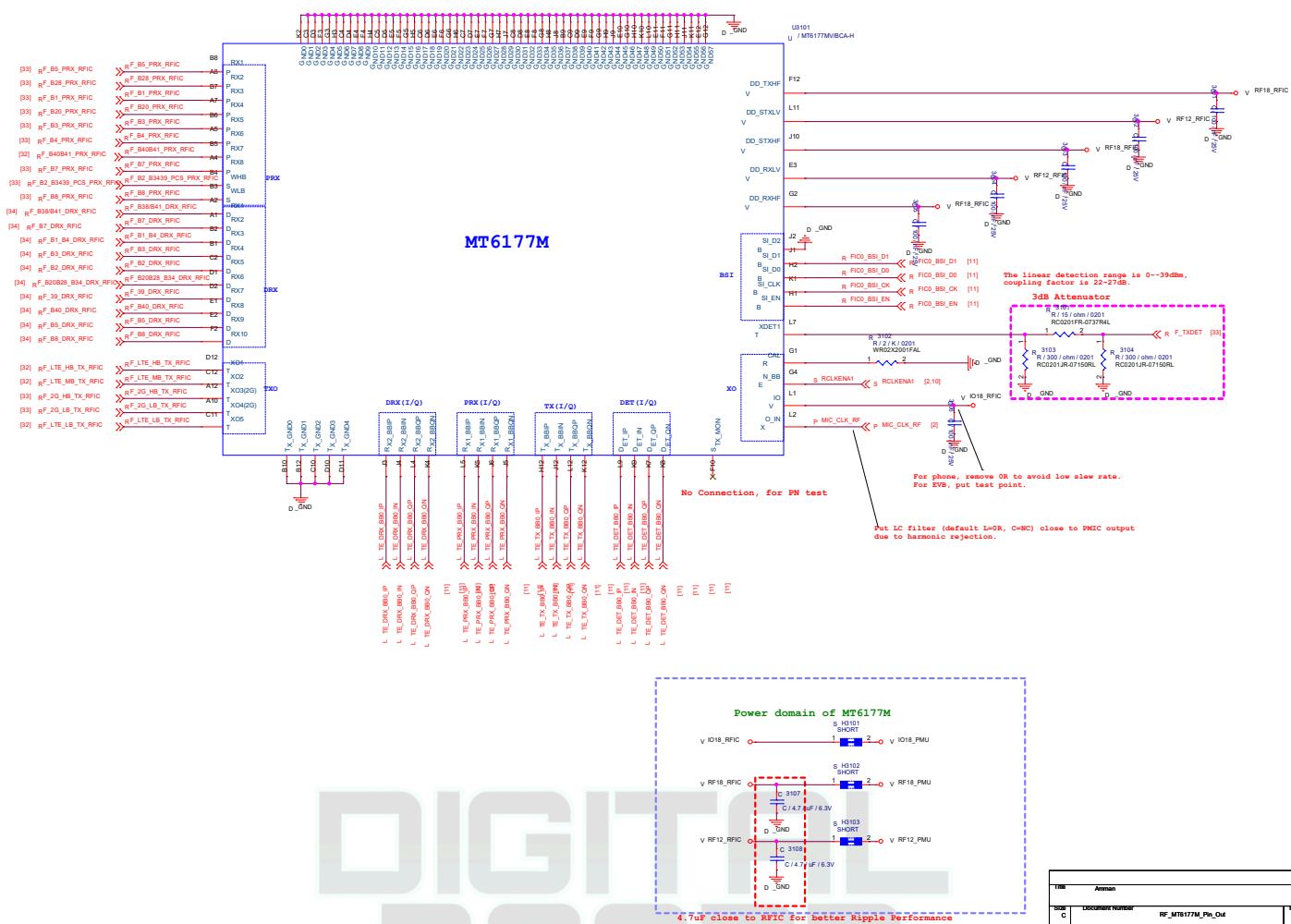
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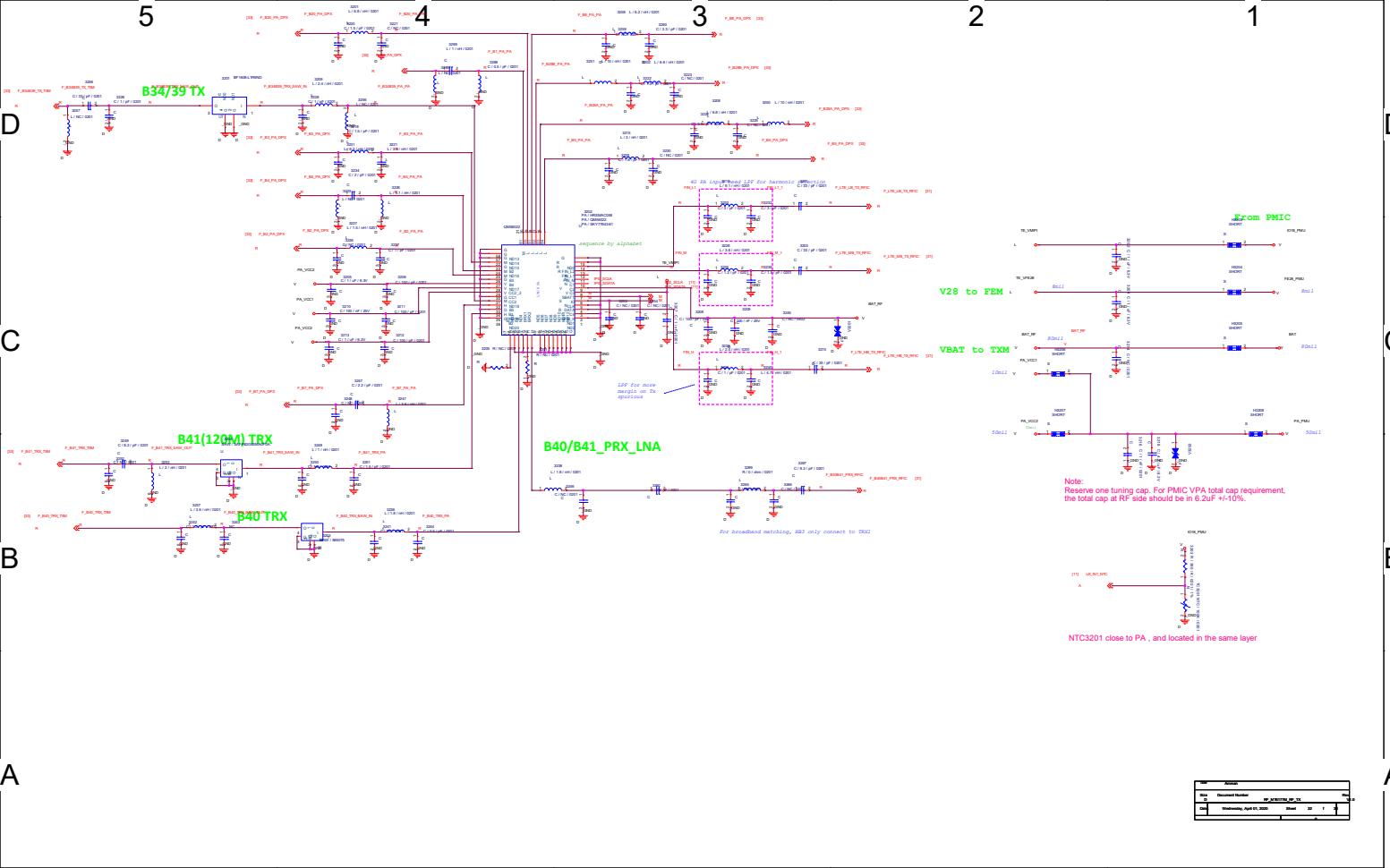
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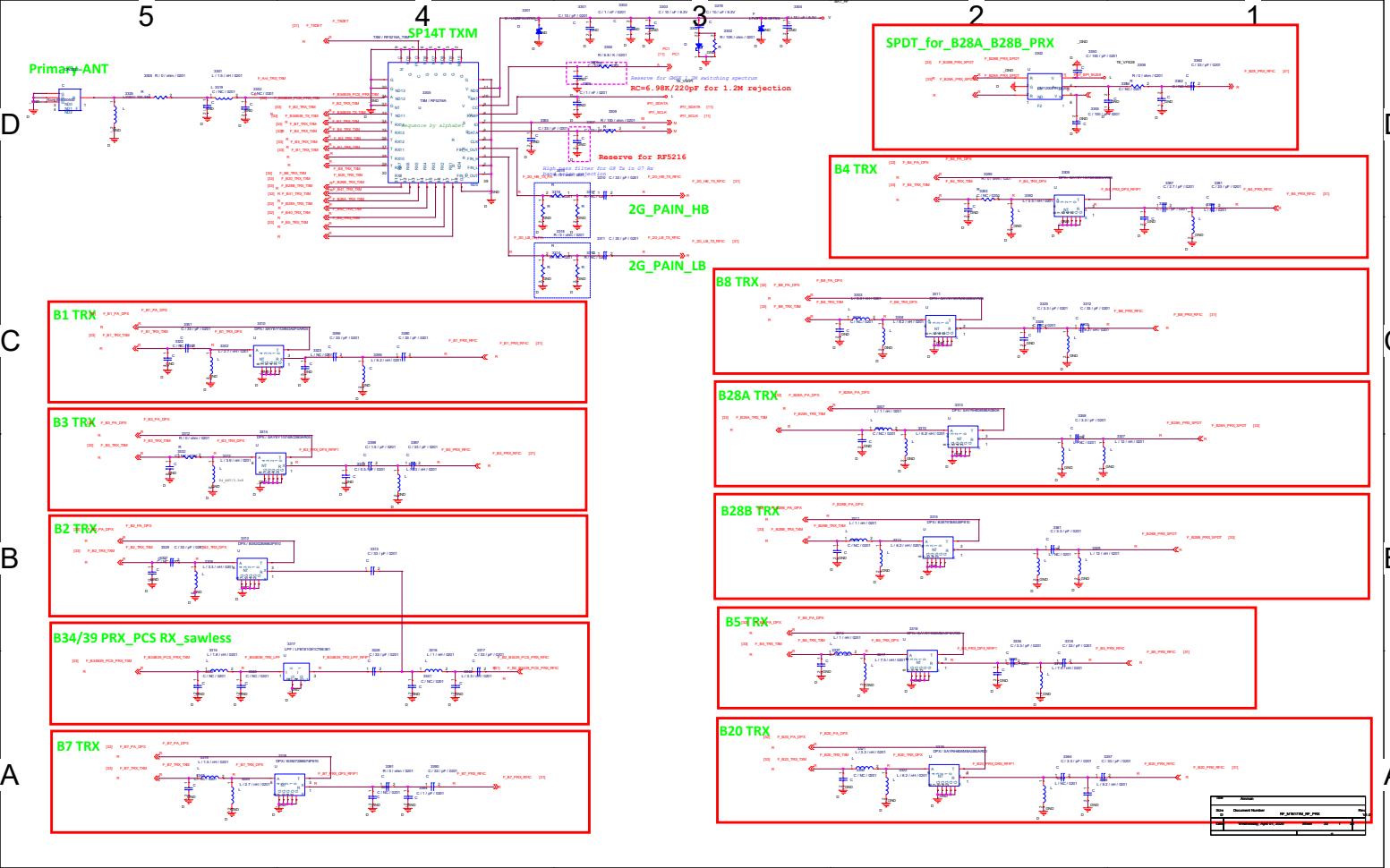


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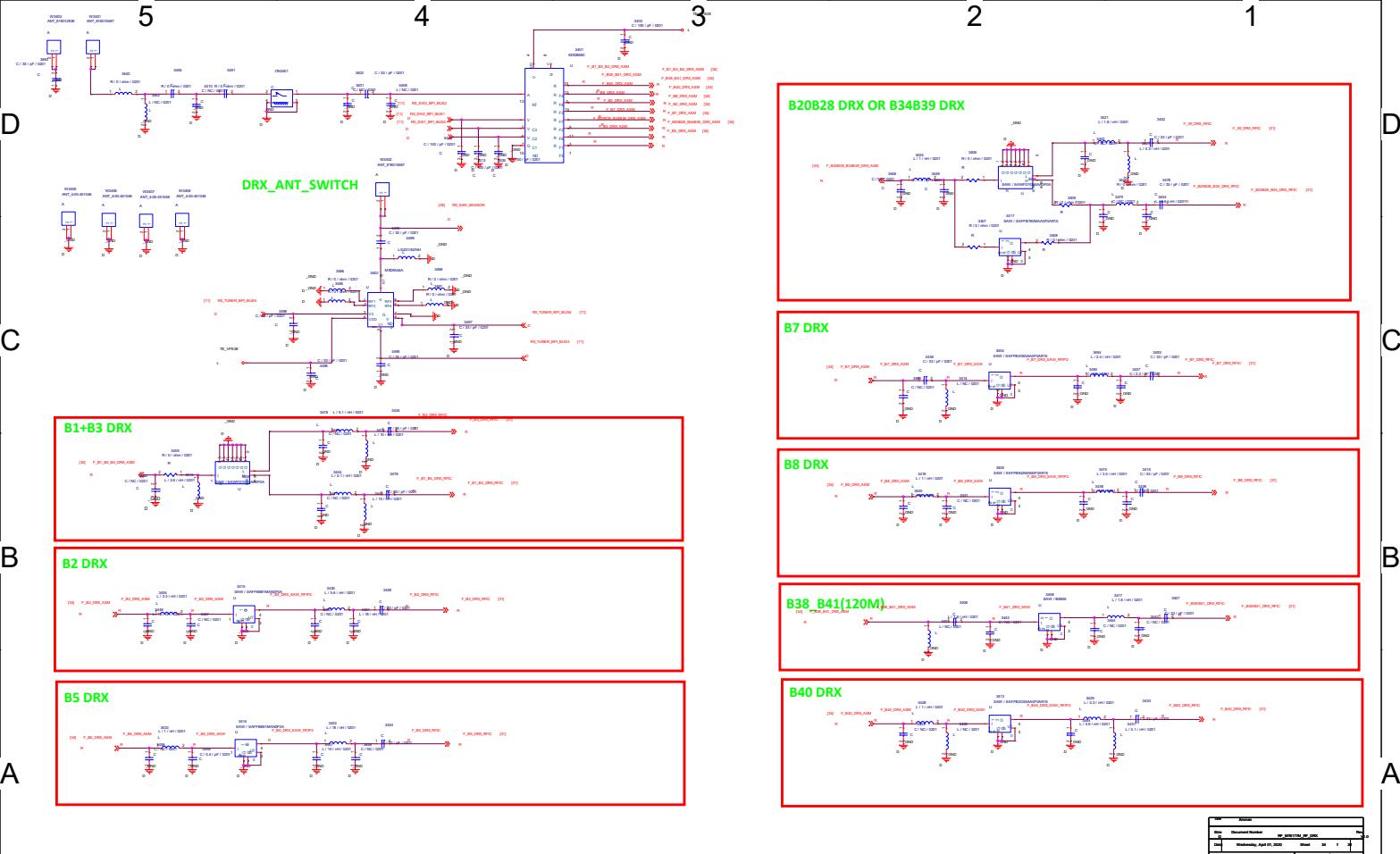


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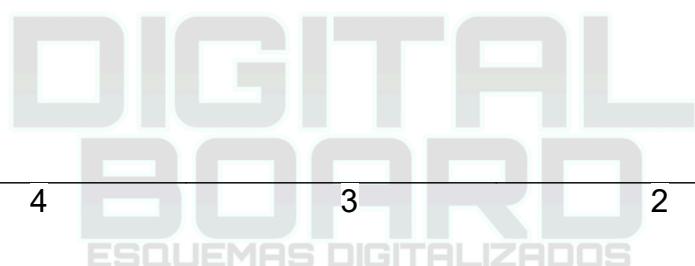
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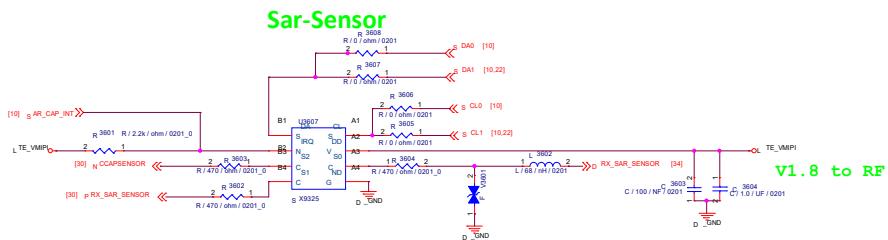
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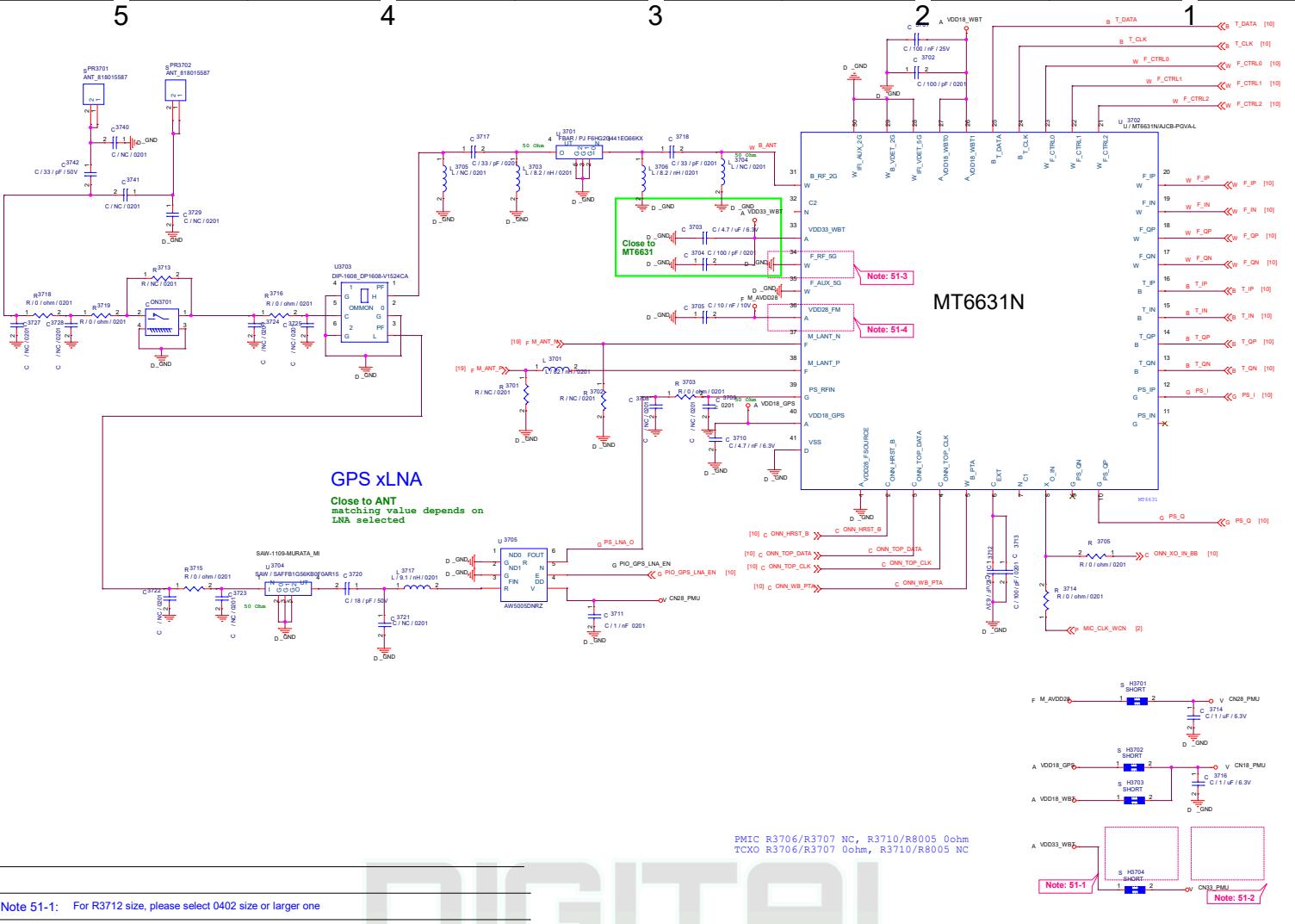
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Note 51-1: For R3712 size, please select 0402 size or larger one

Note 51-2: Please refer to MT6765 Baseband design notice for VCN33 LDO selection guide

Note 51-3: If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND

Note 51-4: Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support

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