1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,D1

8/8/12

Page (.csa)		Contents	Sync	Date
1	1	Table of Contents	MASTER	MASTER
2	2	System Block Diagram	MASTER	02/15/2011
3	3	Power Block Diagram	K17_REF	06/30/2009
4	4	Revision History	MASTER	MASTER
5	5	BOM Configuration	MASTER	MASTER
6	6	BOM Configuration	MASTER	MASTER
7	7	Functional / ICT Test	MASTER	MASTER
8	8	Power Aliases	MASTER	MASTER
9	9	Signal Aliases	D1_MLB_TEST	01/27/2012
10	10	CPU DMI/PEG/FDI/RSVD	J30_MLB	07/14/2011
11	11	CPU CLOCK/MISC/JTAG	J30_MLB	07/14/2011
12	12	CPU DDR3 INTERFACES	J30_MLB	07/14/2011
13	13	CPU POWER	J30_MLB	07/14/2011
14	14	CPU GROUNDS	J30_MLB	07/14/2011
15	16	CPU DECOUPLING-I	MASTER	MASTER
16	17	CPU DECOUPLING-II	MASTER	MASTER
17	18	PCH SATA/PCIe/CLK/LPC/SPI	J13_MLB	09/15/2011
18	19	PCH DMI/FDI/PM/Graphics	J13_MLB	09/15/2011
19	20	PCH PCI/USB/TP/RSVD	J13_MLB	09/15/2011
20	21	PCH GPIO/MISC/NCTF	J13_MLB	09/15/2011
21	22	PCH POWER	J13_MLB	09/15/2011
22	23	PCH GROUNDS	J13_MLB	09/15/2011
23	24	PCH DECOUPLING	J13_MLB	09/15/2011
24	25	CPU & PCH XDP	J30_MLB	07/14/2011
25	26	Chipset Support	MASTER	MASTER
26	27	USB HUB & MUX	J5_AMD	08/17/2011
27	28	CPU Memory S3 Support	J5_MLB	07/29/2011
28	29	DDR3 SDRAM Bank A (Rank 0)	J5_MLB	07/14/2011
29	31	DDR3 SDRAM Bank B (Rank 0)	J5_MLB	07/14/2011
30	33	DDR3 Termination	MASTER	MASTER
31	34	DDR3/FRAMEBUF VREF MARGINING	J5_MLB	07/29/2011
32	35	ALS/CAMERA CONNECTOR	MASTER	MASTER
33	36	Thunderbolt Host (1 of 2)	J5_MLB_KEPLER	11/14/2011
34	37	Thunderbolt Host (2 of 2)	J5_MLB_KEPLER	11/14/2011
35	38	Thunderbolt Power Support	J5_MLB_KEPLER	11/14/2011
36	44	RIO CONNECTORS	MASTER	MASTER
37	45	SSD/HDD Connectors	MASTER	MASTER
38	46	USB 3.0 CONNECTORS	J5_AMD	08/24/2011
39	49	SMC	D1_SENSORS	02/20/2012
40	50	SMC Support	D1_SENSORS	02/20/2012
41	51	LPC+SPI Debug Connector	D1_SENSORS	02/20/2012
42	52	SMBus Connections	MASTER	MASTER
43	53	Power Sensor: Load Side	D1_SENSORS	02/20/2012
44	54	Power Sensor: High Side	D1_SENSORS	02/20/2012
45	55	Thermal Sensors	D1_SENSORS	02/20/2012
46	56	Fan Connectors	J5_MLB	07/29/2011
47	57	KEYBOARD/TRACKPAD (1 OF 2)	D2_MLB_KEPLER	12/08/2011
48	58	KEYBOARD/TRACKPAD (2 OF 2)	D2_MLB_KEPLER	12/08/2011
49	59	DIGITAL ACCELEROMETER & GYRO	J5_MLB	07/29/2011
50	61	SPI ROM	J13_MLB	01/20/2012
51	62	AUDIO: CODEC/REGULATOR	D1_AUDIO	06/06/2012
52	63	AUDIO: HEADPHONE FILTER	D1_AUDIO	06/06/2012
53	66	AUDIO: SPEAKER AMP	D1_AUDIO	06/06/2012
54	67	AUDIO: JACK	D1_AUDIO	06/06/2012
55	68	AUDIO: JACK TRANSLATORS	D1_AUDIO	06/06/2012
56	69	DC-In & Battery Connectors	MASTER	MASTER
57	70	PBus Supply & Battery Charger	MASTER	MASTER
58	71	System Agent Supply	MASTER	MASTER
59	72	5V / 3.3V Power Supply	MASTER	MASTER
60	73	1.5V DDR3 Supply	MASTER	MASTER
61	74	CPU IMVP7 & AXG VCore Regulator	MASTER	MASTER
62	75	CPU IMVP7 & AXG VCore Output	MASTER	MASTER
63	76	CPUVCCIO (1.05V) Power Supply	MASTER	MASTER
64	77	Misc Power Supplies	MASTER	MASTER
65	78	Power FETs	MASTER	MASTER
66	79	Power Control 1/ENABLE	MASTER	MASTER
67	90	eDP Display Connector	D1_SENSORS	07/11/2012
68	92	DDC Crossbar	MASTER	MASTER
69	94	Thunderbolt Connector A	J5_MLB_KEPLER	11/14/2011
70	96	Thunderbolt Connector B	J5_MLB_KEPLER	11/14/2011
71	97	LCD Backlight Driver (LP8545)	J5_MLB_KEPLER	09/21/2011
72	100	CPU Constraints	J5_MLB	09/13/2011
73	101	Memory Constraints	J5_MLB	09/13/2011
74	102	PCH Constraints 1	J5_MLB_KEPLER	09/21/2011
75	103	PCH Constraints 2	J5_MLB	07/29/2011
76	105	Thunderbolt Constraints	T29_CR	08/31/2011
77	106	SMC Constraints	J5_MLB	07/29/2011
78	108	Project Specific Constraints	J5_MLB	07/29/2011
79	109	PCB Rule Definitions	J5_MLB	07/29/2011
80	132	Power Sensors: Extended	D1_SENSORS	07/11/2012

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9216	1	SCHEM,MLB,D1	SCH	CRITICAL	
820-3462	1	PCBF,MLB(NEW),D1	PCB	CRITICAL	

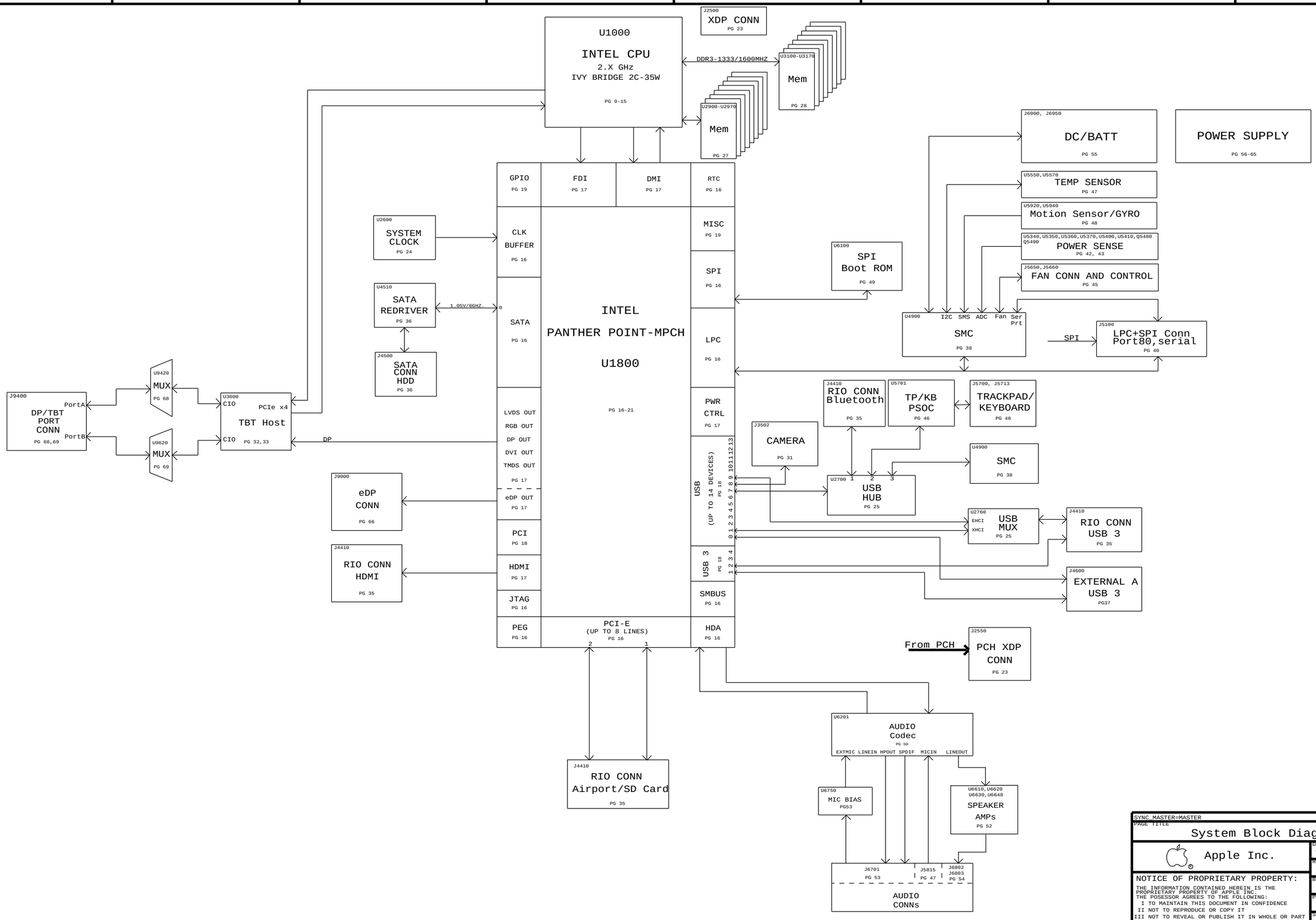
DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Thu Aug 9 12:34:09 2012

DRAWING TITLE: SCHEM,MLB,D1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 132
SHEET: 1 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=MASTER SYNC DATE=02/15/2013

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

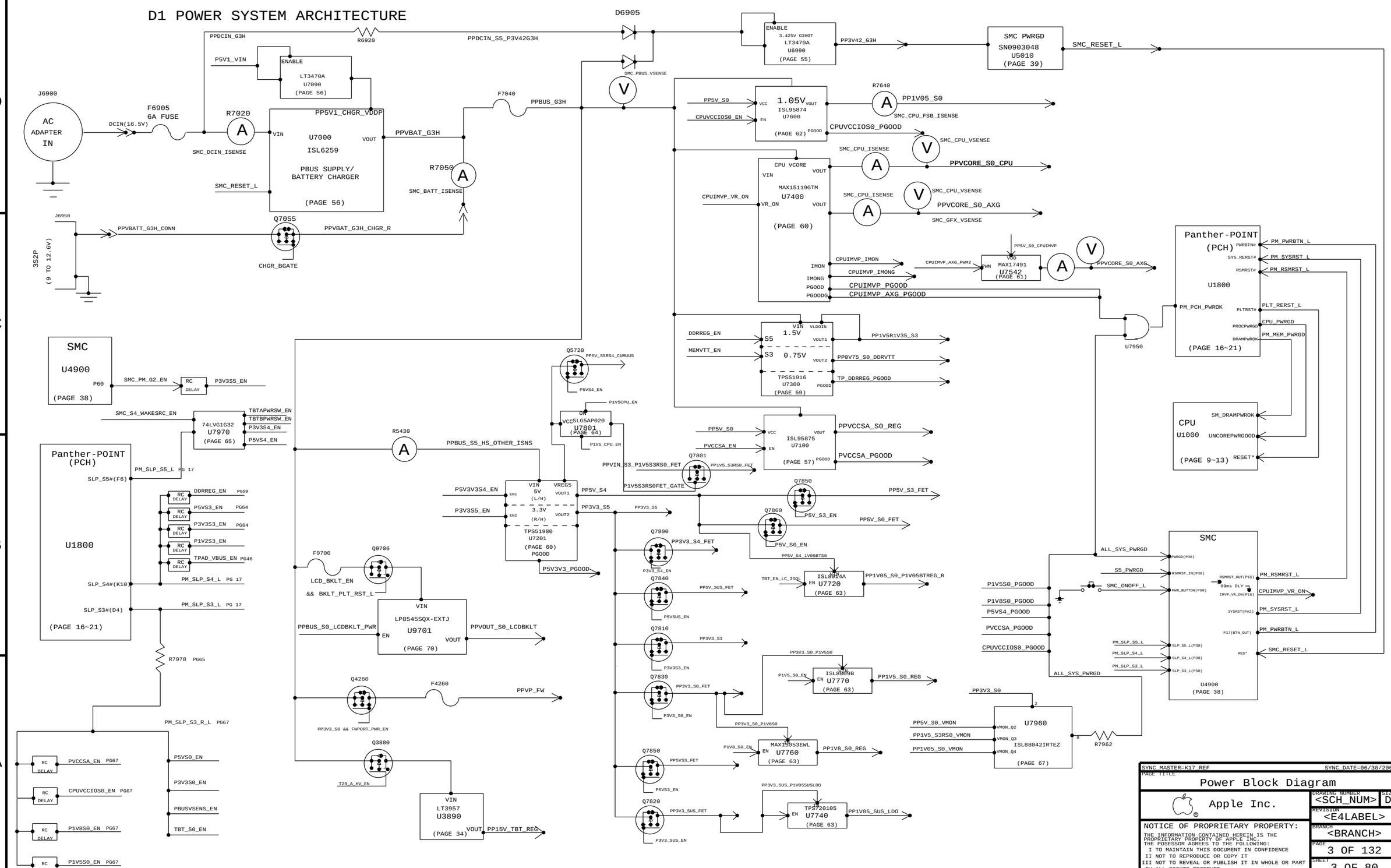
PAGE 2 OF 132

SHEET 2 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

D1 POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE

Power Block Diagram

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 3 OF 132

SHEET 3 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Revision History

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 4 OF 132

SHEET 4 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-4094	DEV BOM,MLB,D1	D1_DEVEL:PVB
607-9189	CMN PTS,PCBA,MLB,D1	D1_COMMON
639-3288	PCBA,2.5G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:DWP2,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3289	PCBA,2.9G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:DWNY,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3290	PCBA,2.5G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:DWP0,RAM_6G_HYNIX_CH0_1600_S
639-3291	PCBA,2.9G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:DWNW,RAM_6G_HYNIX_CH0_1600_S
639-3694	PCBA,2.5G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F16P,RAM_4G_SAMSUNG_35NM_1600_S
639-3695	PCBA,2.9G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F16M,RAM_4G_SAMSUNG_35NM_1600_S
639-3696	PCBA,2.9G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F16N,RAM_4G_HYNIX_1600_S
639-3697	PCBA,2.5G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F16V,RAM_4G_HYNIX_1600_S
639-3773	PCBA,2.5G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F26M,RAM_6G_ELPIDA_CH0_1600_S
639-3772	PCBA,2.9G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F26J,RAM_6G_ELPIDA_CH0_1600_S
639-3770	PCBA,2.5G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F26L,RAM_4G_ELPIDA_1600_S
639-3771	PCBA,2.9G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F26H,RAM_4G_ELPIDA_1600_S
639-3849	PCBA,2.5G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F2WT,RAM_6G_MICRON_CH0_1600_S
639-3848	PCBA,2.9G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F2WR,RAM_6G_MICRON_CH0_1600_S
639-3873	PCBA,2.6G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33H,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3874	PCBA,2.8G,SS 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33P,RAM_6G_SAMSUNG_35NM_CH0_1600_S
639-3875	PCBA,2.6G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33L,RAM_6G_HYNIX_CH0_1600_S
639-3876	PCBA,2.8G,HYNIX 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F339,RAM_6G_HYNIX_CH0_1600_S
639-3881	PCBA,2.6G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33G,RAM_4G_SAMSUNG_35NM_1600_S
639-3882	PCBA,2.8G,SS 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33C,RAM_4G_SAMSUNG_35NM_1600_S
639-3884	PCBA,2.8G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F337,RAM_4G_HYNIX_1600_S
639-3883	PCBA,2.6G,HYNIX 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33D,RAM_4G_HYNIX_1600_S
639-3877	PCBA,2.6G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33Q,RAM_6G_ELPIDA_CH0_1600_S
639-3878	PCBA,2.8G,ELPIDA 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F338,RAM_6G_ELPIDA_CH0_1600_S
639-3885	PCBA,2.6G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33J,RAM_4G_ELPIDA_1600_S
639-3886	PCBA,2.8G,ELPIDA 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33N,RAM_4G_ELPIDA_1600_S
639-3879	PCBA,2.6G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33M,RAM_6G_MICRON_CH0_1600_S
639-3880	PCBA,2.8G,MICRON 6GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F336,RAM_6G_MICRON_CH0_1600_S
639-3846	PCBA,2.5G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.5G,PCH_C1,EEEE:F2WV,RAM_4G_MICRON_1600_S
639-3847	PCBA,2.9G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.9G,PCH_C1,EEEE:F2WQ,RAM_4G_MICRON_1600_S
639-3887	PCBA,2.6G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.6G,PCH_C1,EEEE:F33K,RAM_4G_MICRON_1600_S
639-3888	PCBA,2.8G,MICRON 8GB,MLB,D1	DEVEL_BOM,BASE_BOM,CPU_IVB_2C_2.8G,PCH_C1,EEEE:F33F,RAM_4G_MICRON_1600_S

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DV7Q]	CRITICAL	EEEE:DV7Q
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWNY]	CRITICAL	EEEE:DWNY
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWNW]	CRITICAL	EEEE:DWNW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWP0]	CRITICAL	EEEE:DWP0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DWP2]	CRITICAL	EEEE:DWP2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16M]	CRITICAL	EEEE:F16M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16N]	CRITICAL	EEEE:F16N
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16P]	CRITICAL	EEEE:F16P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F16V]	CRITICAL	EEEE:F16V
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26H]	CRITICAL	EEEE:F26H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26J]	CRITICAL	EEEE:F26J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26L]	CRITICAL	EEEE:F26L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F26M]	CRITICAL	EEEE:F26M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WQ]	CRITICAL	EEEE:F2WQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WR]	CRITICAL	EEEE:F2WR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WT]	CRITICAL	EEEE:F2WT
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F2WV]	CRITICAL	EEEE:F2WV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F336]	CRITICAL	EEEE:F336
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F337]	CRITICAL	EEEE:F337
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F338]	CRITICAL	EEEE:F338
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F339]	CRITICAL	EEEE:F339
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33C]	CRITICAL	EEEE:F33C
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33D]	CRITICAL	EEEE:F33D
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33F]	CRITICAL	EEEE:F33F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33G]	CRITICAL	EEEE:F33G
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33H]	CRITICAL	EEEE:F33H
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33J]	CRITICAL	EEEE:F33J
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33K]	CRITICAL	EEEE:F33K
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33L]	CRITICAL	EEEE:F33L
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33M]	CRITICAL	EEEE:F33M
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33N]	CRITICAL	EEEE:F33N
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33P]	CRITICAL	EEEE:F33P
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F33Q]	CRITICAL	EEEE:F33Q

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0364	128S0264		ALL	Kemet alt to Sanyo
128S0303	128S0353		ALL	Panasonic alt to Sanyo
376S0953	376S0958		ALL	RENESAS ALT TO FAIRCHILD
128S0311	128S0329		ALL	NEC ALT TO SANYO
353S3237	353S2192		ALL	TI ALT TO INTERSIL
376S0977	376S0859		ALL	Diodes alt to Toshiba
138S0722	138S0691		ALL	Multi alt to Samsung
197S0487	197S0485		ALL	Epson alt to TXC
197S0484	197S0485		ALL	NDK alt to TXC
197S0479	197S0486		ALL	Epson alt to TXC
197S0478	197S0486		ALL	NDK alt to TXC
197S0481	197S0480		ALL	Epson alt to NDK
376S0972	376S0612		ALL	ROHM alt to Toshiba
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S1017	376S0612		ALL	ROHM alt to Toshiba
138S0624	138S0677		ALL	Murata alt to Taiyo Yuden
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung
152S1703	152S1701		ALL	Sumida alt to Cyntec
371S0730	371S0490		ALL	Diodes alt to NXP
138S0725	138S0724		ALL	Samsung alt to Murata
138S0727	138S0709		ALL	Samsung alt to Murata
376S1080	376S0820		ALL	Diodes alt to ON Semi
372S0186	372S0185		ALL	NXP alt to Diodes
128S0363	128S0296		ALL	NEC alt to Sanyo
376S0903	376S0796		ALL	Fairchild alt to Siliconix
740S0144	740S0118		ALL	Littlefuse alt to Polytronic
152S1539	152S1598		ALL	Cyntec alt to Toko
152S1645	152S0461		ALL	Cyntec alt to Vishay
155S0667	155S0583		ALL	MAG LAYERS ALT TO MURATA
103S0305	103S0266		ALL	Yageo alt to Cyntec
112S0274	112S0254		ALL	Yageo alt to Cyntec
376S1113	376S1110		ALL	Diodes to AOS
155S0588	155S0367		ALL	murata ALT TO MURATA

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4181	1	IVB,QBP0,ES2,K0,2.3,35W,2+2,1.0,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.3G_ES2
337S4182	1	IVB,QBP0,ES2,K0,2.6,35W,2+2,1.05,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G_ES2
337S4292	1	IVB,Q4C7,Q5,L1,2.5,35W,2+2,1.1,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.5G_Q5
337S4300	1	IVB,QC30,Q5,L1,2.6,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G_Q5
337S4302	1	IVB,QC84,Q5,L1,2.8,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.8G_Q5
337S4294	1	IVB,QC4M,Q5,L1,2.9,35W,2+2,1.25,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.9G_Q5
337S4264	1	IVB,S R0N0,PRQ,L1,2.5,35W,2+2,1.1,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.5G
337S4338	1	IVB,S R0MY,PRQ,L1,2.6,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.6G
337S4339	1	IVB,S R0MU,PRQ,L1,2.8,35W,2+2,1.2,3M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.8G
337S4265	1	IVB,S R0MU,PRQ,L1,2.9,35W,2+2,1.25,4M,BGA	U1000	CRITICAL	CPU_IVB_2C_2.9G
337S4180	1	IC,PCH,PPT-MB SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB SFF,P-Q5,C0	U1800	CRITICAL	PCH_C0
337S4283	1	IC,PCH,PPT-MB SFF,PRQ,C1	U1800	CRITICAL	PCH_C1
338S1113	1	IC,TBT,CR-4C,B1,PRQ,288FCBGA,12x12MM	U3600	CRITICAL	TBTRTR:B1
333S0623	16	IC,SDRAM,2GB2T,256MX8,DDR3-1600,78FBGA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_SAMSUNG_35NM_1600_S
333S0622	16	IC,SDRAM,2GB1T,256MX8,DDR3-1600,78FBGA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_HYNIX_1600_S
333S0628	16	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_ELPIDA_1600_S
333S0649	16	IC,SDRAM,DDR3-1600,256MX8,78FBGA,MICRON	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	2G_MICRON_1600_S
333S0625	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_HYNIX_1600_S
333S0629	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,B-DIE,ELPIDA	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_ELPIDA_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,D35,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_SAMSUNG_35NM_1600_S
333S0623	8	IC,SDRAM,2GB2T,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_SAMSUNG_35NM_CH0_1600_S
333S0624	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,D35,SAMSUNG	U2200,U2210,U2220,U2230,U2240,U2250,U2260,U2270	CRITICAL	6G_SAMSUNG_35NM_CH0_1600_S
333S0622	8	IC,SDRAM,2GB1T,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_HYNIX_CH0_1600_S
333S0625	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,HYNIX	U2200,U2210,U2220,U2230,U2240,U2250,U2260,U2270	CRITICAL	6G_HYNIX_CH0_1600_S
333S0628	8	IC,SDRAM,DDR3-1600,256MX8,78FBGA,D-DIE,ELPIDA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_ELPIDA_CH0_1600_S
333S0629	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,B-DIE,ELPIDA	U2200,U2210,U2220,U2230,U2240,U2250,U2260,U2270	CRITICAL	6G_ELPIDA_CH0_1600_S
333S0660	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,MICRON	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_MICRON_1600_S
333S0649	8	IC,SDRAM,DDR3-1600,256MX8,78FBGA,MICRON	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_MICRON_CH0_1600_S
333S0660	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,MICRON	U2200,U2210,U2220,U2230,U2240,U2250,U2260,U2270	CRITICAL	6G_MICRON_CH0_1600_S

D1 BOM GROUPS

BOM GROUP	BOM OPTIONS
D1_COMMON	ALTERNATE,COMMON,D1_COMMON1,D1_COMMON2,D1_PROGPARTS,D1_PVB
D1_COMMON1	CPUMEM:S0,SMC_DEBUG_YES,TBTBST:Y,TBTRTR:B1,TBTHV:P15V,HUB_2NONREM,USBHUB:2512B,AXG_PHASE2,TBTISNS:YES
D1_COMMON2	EDP:YES,PPDDR:1V35,LPCPLUS_CONN:YES,LPCPLUS_R:YES,CAPS:INT,BTPWR:S4,SKIP_5V3V3:AUDIBLE,TPAD_5V_LDO:S5,SMS
D1_PVB	LOADISNS:NO,LCDBKLT:PROD,KBDBKLT:PROD
D1_PROGPARTS	SMC_PROG:PVB,TBTROM:PROG,BOOTROM_PROG:PVB,TPAD_PSOC:PROG
D1_BLANK	
D1_DEVEL:ENG	ALTERNATE,IVB_PPT_XDP,LOADISNS:YES,S0PGOOD_ISL,DDRVREF_DAC,VREFDQ:M1_M3,VREFCA:LDO_DAC
D1_DEVEL:PVB	ALTERNATE,IVB_PPT_XDP,VREFDQ:M1_M3,VREFCA:LDO
IVB_PPT_XDP	XDP,XDP_CONN,XDP_CPU:BPM,XDP_PCH

DDR3 SPD STRAPPINGS

BOM GROUP	BOM OPTIONS
RAM_4G_HYNIX_1600_S	4G_HYNIX_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_2G_ELPIDA_1600_S	2G_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM_4G_SAMSUNG_28NM_1600_S	4G_SAMSUNG_28NM_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_2G_MICRON_1600_S	2G_MICRON_1600_S,RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_4G_ELPIDA_1600_S	4G_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_4G_SAMSUNG_35NM_1600_S	4G_SAMSUNG_35NM_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_6G_SAMSUNG_35NM_CH0_1600_S	6G_SAMSUNG_35NM_CH0_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM_4G_MICRON_1600_S	4G_MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM_6G_MICRON_CH0_1600_S	6G_MICRON_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM_6G_ELPIDA_CH0_1600_S	6G_ELPIDA_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM_6G_SAMSUNG_28NM_CH0_1600_S	6G_SAMSUNG_28NM_CH0_1600_S,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM_6G_HYNIX_CH0_1600_S	6G_HYNIX_CH0_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM_2G_SAMSUNG_1600_S	2G_SAMSUNG_35NM_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM_2G_HYNIX_1600_S	2G_HYNIX_1600_S,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0642	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	U2000,U2010,U2020,U2030,U2040,U2050,U2060,U2070,U2080,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	4G_SAMSUNG_28NM_1600_S
333S0623	8	IC,SDRAM,2GB2T,256MX8,DDR3-1600,78FBGA	U2100,U2110,U2120,U2130,U2140,U2150,U2160,U2170	CRITICAL	6G_SAMSUNG_28NM_CH0_1600_S
333S0642	8	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	U2200,U2210,U2220,U2230,U2240,U2250,U2260,U2270	CRITICAL	6G_SAMSUNG_28NM_CH0_1600_S

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 5 OF 132

SHEET 5 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PD Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-1533	1	STDOFF,BMU,TOPSIDE,D1,SM	J6950_63	CRITICAL	
860-1530	1	STDOFF-1.9D2.93H-TH-0.85-1.2	J6950_64	CRITICAL	
860-1529	1	STDOFF-1.80D1.53H-SM	J6950_65	CRITICAL	
825-7841	1	LBL,PART CONFIG,BOARDS,D2	CONFIG_LABEL	CRITICAL	
946-4350	1	D1 MLB LOCTITE UV GLUE 190024/S 0.24G	EDGE_BOND	CRITICAL	

DEVELOPMENT/BASE BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-4094	1	D1 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
607-9189	1	D1 MLB BASE BOM	BASE	CRITICAL	BASE_BOM

SMC

341S3528	1	IC,SMC12,PROTO1,D1	U4900	CRITICAL	SMC_PROG:PROTO
341S3404	1	IC,SMC,DEVELOPMENT-PIB,D1	U4900	CRITICAL	SMC_PROG:PIB
341S3405	1	IC,SMC,DEVELOPMENT-FSB,D1	U4900	CRITICAL	SMC_PROG:FSB
341S3406	1	IC,SMC,DEVELOPMENT-PVB,D1	U4900	CRITICAL	SMC_PROG:PVB

EFI ROM

341S3571	1	IC,EF,ROM,PROTO1,D1	U6100	CRITICAL	BOOTROM_PROG:PROTO
341S3603	1	IC,EFI,ROM,PIB, D1	U6100	CRITICAL	BOOTROM_PROG:PIB
341S3636	1	IC,EFI,ROM,PIB2, D1	U6100	CRITICAL	BOOTROM_PROG:PIB2
341S3650	1	IC,EFI,ROM,FSB, D1	U6100	CRITICAL	BOOTROM_PROG:FSB
341SXXXX	1	IC,EFI,ROM,FSB2, D1	U6100	CRITICAL	BOOTROM_PROG:FSB2
341S3667	1	IC,EFI,ROM,PVB, D1	U6100	CRITICAL	BOOTROM_PROG:PVB

Programmables - All builds

335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Macronix	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,Numonyx	U6100	CRITICAL	BOOTROM_BLANK
341S3670	1	IC,TP PSOC,V224,PVB,D1	U5701	CRITICAL	TPAD_PSOC:PROG
337S2983	1	IC,TP PSOC,QFN,BLANK	U5701	CRITICAL	TPAD_PSOC:BLANK
341S3668	1	IC,EEPROM,CR,V14.1,D1 PVB	U3690	CRITICAL	TBTROM:PROG
335S0865	1	IC,EEPROM,SERIAL,8KB,SOIC	U3690	CRITICAL	TBTROM:BLANK
338S1098	1	IC,SMC12-A3,LX4FS1AH58BCI6A3	U4900	CRITICAL	SMC_BLANK
998-3919	1	SOCKET, SMC12	J4900	CRITICAL	SMC_SOCKET

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 6 OF 132

SHEET 6 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Functional Test Points

J5650 (LEFT FAN CONN)

FUNC_TEST
PP5V_S0 — 3 TPs per Fan
FAN_LT_PWM
FAN_LT_TACH

J5660 (RIGHT FAN CONN)

FAN_RT_PWM
FAN_RT_TACH
GND — 5 TPs per Fan

J3502 (ALS/CAMERA CONN)

SMBUS_SMC_2_S3_SDA
SMBUS_SMC_2_S3_SCL
PP5V_S3_ALSCAMERA_F

J4400 (RIO CABLE CONN)

PP3V3_S4
PP3V3_S3
PP3V3_WLAN_F
PP5V_S4
PP1V5_S0

J4410 (RIO FLEX CONN)

USB_EXTB_OC_L
HDMI_IG_DDC_CLK
HDMI_IG_DDC_DATA
HDMI_HPD_L
PM_SLP_S3_L
PM_SLP_S4_L
AP_CLKREQ_Q_L
ENET_RESET_L
ENET_CLKREQ_L
SD_PWR_EN
SDCONN_STATE_CHANGE_SMC
PCIE_WAKE_L
AP_CLKREQ_Q_L
AP_RESET_CONN_L
WIFI_EVENT_L
USB_EXTB_P
USB_EXTB_N
USB_BT_CONN_P
USB_BT_CONN_N

AP_RESET_CONN_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA

SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA

J5815 (KBD BACKLIGHT CONN)

PP_KBD_BOOST_VOUT
KBDLED_CATHODE1
KBDLED_CATHODE2
SMC_KBDLED_PRESENT_L

J6950 (MAIN BATT CONN)

PPVBAT_G3H_CONN
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
SYS_DETECT_L_R

SYSDET1
SYSDET_3_4

J6801 (2 MIC CONN)

CON_DMIC_PWR
CON_DMIC_SDA1
CON_DMIC_CLK

PCH_VSS_NCTF<19>
PCH_VSS_NCTF<19>

J4600 (LEFT USB CONN)

PP5V_S3_LTUSB_A_F
USB_LT1_N
USB_LT1_P

FUNC_TEST
GND
GND
GND
6 TPs

U1000 CHARZ TPS

PCIE_TBT_D2R_P<0> — PP0700
PCIE_TBT_D2R_N<0> — PP0701
DMI_S2N_P<0> — PP0702
DMI_S2N_N<0> — PP0703
DMI_CLK100M_CPU_P — PP0721
DMI_CLK100M_CPU_N — PP0722

U1800 CHARZ TPS

DMI_N2S_P<0> — PP0704
DMI_N2S_N<0> — PP0705
FDI_DATA_P<0> — PP0706
FDI_DATA_N<0> — PP0707
FDI_DATA_P<4> — PP0708
FDI_DATA_N<4> — PP0709
PCIE_AP_D2R_P — PP0710
PCIE_AP_D2R_N — PP0711
PCIE_ENET_D2R_P — PP0712
PCIE_ENET_D2R_N — PP0713
PCIE_CLK100M_TBT_P — PP0723
PCIE_CLK100M_TBT_N — PP0724

U4900 CHARZ TPS

LPC_AD<0> — PP0714
LPC_AD<1> — PP0715
LPC_AD<2> — PP0716
LPC_AD<3> — PP0717
LPC_FRAME_L — PP0718
LPC_CLK33M_SMC — PP0719

AUD_DMIC_SDA1 — PP0720

J6701 (AUDIO JACK CONN)

AUD_CONN_SLEEVE
AUD_CONN_MIC_XW
AUD_CONN_SLEEVE_XW
AUD_CONN_HP_LEFT
AUD_CONN_TIPDET_INV
PP3V3_S0
AUD_SPDIF_OUT_JACK
AUD_CONN_HP_RIGHT
AUD_CONN_TYPEDET
AUD_CONN_MIC

J6802 (AUDIO LEFT SPEAKER CONN)

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6803 (AUDIO RIGHT SPEAKER CONN)

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N
GND

J9000 (EDP CONN)

PP5VR3V3_SW_LCD

PPVOUT_S0_LCDBKLT — 2 TP needed

LED_RETURN_6
LED_RETURN_5
LED_RETURN_4
LED_RETURN_3
LED_RETURN_2
LED_RETURN_1
LCD_HPD_CONN

DP_INT_AUX_P
DP_INT_AUX_N

J3401 & J3402 (AIRPORT/BT/CAMERA CONN)

PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
AP_CLKREQ_Q_L
PCIE_WAKE_L
AP_RESET_CONN_L
PP3V3_WLAN_F
PP5V_S3_ALSCAMERA_F
SMBUS_SMC_2_S3_SDA
SMBUS_SMC_2_S3_SCL
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N

J5713 (KEY BOARD CONN)

PP3V3_S4
PP3V42_G3H
WS_KBD1
WS_KBD2
WS_KBD3
WS_KBD4
WS_KBD5
WS_KBD6
WS_KBD7
WS_KBD8
WS_KBD9
WS_KBD10
WS_KBD11
WS_KBD12
WS_KBD13
WS_KBD14
WS_KBD15_CAP
WS_KBD16_NUM
WS_KBD17
WS_KBD18
WS_KBD19
WS_KBD20
WS_KBD21
WS_KBD22
WS_KBD23
WS_KBD_ONOFF_L
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD

J5700 (IPD FLEX CONN)

PP3V3_S4
Z2_CS_L
Z2_MOSI
Z2_MISO
Z2_SCLK
Z2_HOST_INTN
PP5V_S4_CUMULUS
Z2_CLKIN
SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
PSOC_SCLK
PSOC_MOSI
PSOC_MISO
PICKB_L
PSOC_F_CS_L
Z2_KEY_ACT_L

J6900 (DC POWER CONN)

TDM_ONEWIRE_MPM
ADAPTER_SENSE
PP18V5_DCIN_FUSE

GND

J4500 (SSD/HDD FLEX CONN)

PP3V3_S0_SSD_FLT
SMC_OOB1_TX_L
SMC_OOB1_RX_L
PP5V_S0_HDD_FLT

GND

FUNC_TEST
BKLT_EN
LCD_BKLT_PWM
PM_CLKRUN_L
PM_SYSRST_L

SMC_ONOFF_L

J5100 (LPC + SPI CONN)

PP3V42_G3H
PP5V_S0
LPC_CLK33M_LPCPLUS
LPC_AD<0>
LPC_AD<2>
LPC_AD<1>
LPC_AD<3>
SPI_ALT_MOSI
LPCPLUS_GPIO
LPCPLUS_RESET_L
SMC_TDO
TP_SMC_TRST_L
TP_SMC_MD1
SMC_TX_L
SPI_ALT_MISO
LPC_FRAME_L
SPIROM_USE_MLB
PM_CLKRUN_L
SPI_ALT_CLK
SPI_ALT_CS_L
LPC_SERIRQ
LPC_PWRDWN_L
SMC_TDI
SMC_TCK
SMC_RESET_L
SMC_ROMBOOT
SMC_RX_L
SMC_TMS

POWER RAILS

FUNC_TEST
PM_SLP_S3_L
PP0V75_S0_DDRVTT
PP1V05_S0

LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
GND — 4 TPs

PP3V3_S0
PP3V3_S3
PP3V3_S5
PP3V3_S5_AVREF_SMC
PP3V42_G3H
PP5V_S0
PP5V_S3
PP5V_S5
PPBUS_G3H
PPDCIN_G3H

PPVCORE_S0_CPU

PPVTTDDR_S3

DMI_S2N_P<3..1>
DMI_S2N_N<3..1>
DMI_N2S_P<3..1>
DMI_N2S_N<3..1>

TBTBPWRSW_ISET_V3P3

TBTBPWRSW_ISET_S0_R
TBTBPWRSW_ISET_S3

TBTAPWRSW_ISET_V3P3

TBTAPWRSW_ISET_S0

TBTAPWRSW_ISET_S3
TBTAPWRSW_ISET_S3_R

TBT_A_R2D_C_P<1..0>
TBT_A_R2D_C_N<1..0>
TBT_A_R2D_P<1..0>
TBT_A_R2D_N<1..0>

TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>

TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>

TBT_B_R2D_C_P<1..0>
TBT_B_R2D_C_N<1..0>
TBT_B_R2D_P<1..0>
TBT_B_R2D_N<1..0>

TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
TBT_B_D2R_C_P<1>
TBT_B_D2R_C_N<1>

TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>

PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_AP_R2D_P
PCIE_AP_R2D_N

ICT Test Points

CPU NO_TESTs

TP_TBT_MONDC0 — NC_TBT_MONDC0
TP_TBT_MONDC1 — NC_TBT_MONDC1
TP_TBT_PCIE_RESET0_L — NC_TBT_PCIE_RESET0_L
TP_TBT_PCIE_RESET1_L — NC_TBT_PCIE_RESET1_L
TP_TBT_PCIE_RESET2_L — NC_TBT_PCIE_RESET2_L
TP_TBT_PCIE_RESET3_L — NC_TBT_PCIE_RESET3_L
TP_TBT_XTAL25OUT — NC_TBT_XTAL25OUT

TP_DP_TBTSRC_ML_CP<3> — NC_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3> — NC_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2> — NC_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2> — NC_DP_TBTSRC_ML_CN<2>
TP_DP_TBTSRC_ML_CP<1> — NC_DP_TBTSRC_ML_CP<1>
TP_DP_TBTSRC_ML_CN<1> — NC_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0> — NC_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0> — NC_DP_TBTSRC_ML_CN<0>
TP_DP_TBTSRC_AUXCH_CP — NC_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_AUXCH_CN — NC_DP_TBTSRC_AUXCH_CN

TP_SPI_CS1_L — NC_SPI_CS1_L
TP_PCH_GPIO8 — NC_PCH_GPIO8
TP_PCH_STRP_BBS1 — NC_PCH_STRP_BBS1
TP_PCH_STRP_ESI_L — NC_PCH_STRP_ESI_L
TP_PCH_TP23 — NC_PCH_TP23
TP_PCI_CLK33M_OUT2 — NC_PCI_CLK33M_OUT2
TP_PCIE_CLK100M_PEGAN — NC_PCIE_CLK100M_PEGAN
TP_PCIE_CLK100M_PEGAP — NC_PCIE_CLK100M_PEGAP
TP_PM_SLP_A_L — NC_PM_SLP_A_L
TP_PPVOUT_PCH_DCPSUSBYP — NC_PPVOUT_PCH_DCPSUSBYP
TP_SMC_MPM5_LED_PWR — NC_SMC_MPM5_LED_PWR
TP_SMC_MPM5_LED_CHG — NC_SMC_MPM5_LED_CHG
TP_SMS_INT2 — NC_SMS_INT2

PCIE_TBT_R2D_C_P<3..0>
PCIE_TBT_R2D_C_N<3..0>
PCIE_TBT_R2D_P<3..0>
PCIE_TBT_R2D_N<3..0>
PCIE_TBT_D2R_P<3..1>
PCIE_TBT_D2R_N<3..1>
PCIE_TBT_D2R_C_P<3..1>
PCIE_TBT_D2R_C_N<3..1>

MEM_A_DQ<0>
MEM_A_DQ<12..2>
MEM_A_DQ<19..14>
MEM_A_DQ<24..21>
MEM_A_DQ<32..26>
MEM_A_DQ<42..34>
MEM_A_DQ<54..44>
MEM_A_DQ<56>
MEM_A_DQ<63..58>

MEM_B_DQ<2..0>
MEM_B_DQ<13..4>
MEM_B_DQ<19..15>
MEM_B_DQ<25..21>
MEM_B_DQ<35..27>
MEM_B_DQ<40..37>
MEM_B_DQ<47..42>
MEM_B_DQ<57..49>
MEM_B_DQ<63..59>

NC_MEM_EVENT_L

HDMI_IG_CLK_C_P
HDMI_IG_CLK_C_N
HDMI_IG_DATA_C_P<2..0>
HDMI_IG_DATA_C_N<2..0>

PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
USB3_EXTB_TX_C_P
USB3_EXTB_TX_C_N

S2 CAMERA PCIE SIGNALS

NC_PCIE_CAMERA_D2RP — PCIE_EXCARD_D2R_N
NC_PCIE_CAMERA_D2RN — PCIE_EXCARD_D2R_P
NC_PCIE_CAMERA_R2D_CN — PCIE_EXCARD_R2D_C_N
NC_PCIE_CAMERA_R2D_CP — PCIE_EXCARD_R2D_C_P

NC_PCIE_CLK100M_CAMERAN — PCIE_CLK100M_EXCARD_N
NC_PCIE_CLK100M_CAMERAP — PCIE_CLK100M_EXCARD_P

NO_TEST NC NO_TESTs

NC_PCIE_5_D2RN
NC_PCIE_5_D2RP
NC_PCIE_5_R2D_CN
NC_PCIE_5_R2D_CP
NC_PCIE_6_D2RN
NC_PCIE_6_D2RP
NC_PCIE_6_R2D_CN
NC_PCIE_6_R2D_CP
NC_PCIE_7_D2RN
NC_PCIE_7_D2RP
NC_PCIE_7_R2D_CN
NC_PCIE_7_R2D_CP
NC_PCIE_8_D2RN
NC_PCIE_8_D2RP
NC_PCIE_8_R2D_CN
NC_PCIE_8_R2D_CP

TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4P
TP_PCIE_CLK100M_PEBN — NC_PCIE_CLK100M_PEBN
TP_PCIE_CLK100M_PEBP — NC_PCIE_CLK100M_PEBP

TP_SATA_C_D2RN — NC_SATA_C_D2RN
TP_SATA_C_D2RP — NC_SATA_C_D2RP
TP_SATA_C_R2D_CN — NC_SATA_C_R2D_CN
TP_SATA_C_R2D_CP — NC_SATA_C_R2D_CP
TP_SATA_D_D2RN — NC_SATA_D_D2RN
TP_SATA_D_D2RP — NC_SATA_D_D2RP
TP_SATA_D_R2D_CN — NC_SATA_D_R2D_CN
TP_SATA_D_R2D_CP — NC_SATA_D_R2D_CP
TP_SATA_E_D2RN — NC_SATA_E_D2RN
TP_SATA_E_D2RP — NC_SATA_E_D2RP
TP_SATA_E_R2D_CN — NC_SATA_E_R2D_CN
TP_SATA_E_R2D_CP — NC_SATA_E_R2D_CP
TP_SATA_F_D2RN — NC_SATA_F_D2RN
TP_SATA_F_D2RP — NC_SATA_F_D2RP
TP_SATA_F_R2D_CN — NC_SATA_F_R2D_CN
TP_SATA_F_R2D_CP — NC_SATA_F_R2D_CP

TP_CRT_IG_BLUE — NC_CRT_IG_BLUE
TP_CRT_IG_GREEN — NC_CRT_IG_GREEN
TP_CRT_IG_RED — NC_CRT_IG_RED

TP_CRT_IG_DDC_CLK — NC_CRT_IG_DDC_CLK
TP_CRT_IG_DDC_DATA — NC_CRT_IG_DDC_DATA

TP_CRT_IG_HSYNC — NC_CRT_IG_HSYNC
TP_CRT_IG_VSYNC — NC_CRT_IG_VSYNC

TP_HDA_SDIN1 — NC_HDA_SDIN1
TP_HDA_SDIN2 — NC_HDA_SDIN2
TP_HDA_SDIN3 — NC_HDA_SDIN3

TP_SDVO_TVCLKINN — NC_SDVO_TVCLKINN
TP_SDVO_TVCLKINP — NC_SDVO_TVCLKINP
TP_SDVO_STALLN — NC_SDVO_STALLN
TP_SDVO_STALLP — NC_SDVO_STALLP
TP_SDVO_INTN — NC_SDVO_INTN
TP_SDVO_INTP — NC_SDVO_INTP

TP_PCI_PME_L — NC_PCI_PME_L
TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3

NC_ISNS_LCDBKLTN
NC_ISNS_LCDBKLTP
NC_ISNS_WLANN
NC_ISNS_WLANP

NC_ISNS_LCD_PANELN
NC_ISNS_LCD_PANELP

PCH ALIASES

NC_LPC_DREQ0_L — TP_LPC_DREQ0_L
NC_LPC_DREQ1_L — TP_LPC_DREQ1_L
TP_CLINK_CLK — NC_CLINK_CLK
TP_CLINK_DATA — NC_CLINK_DATA
TP_CLINK_RESET_L — NC_CLINK_RESET_L

TP_XDP_PCH_HOOK4 — NC_XDP_PCH_HOOK4
TP_XDP_PCH_HOOK5 — NC_XDP_PCH_HOOK5
TP_XDP_PCH_OBSFN_B<0> — NC_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1> — NC_XDP_PCH_OBSFN_B<1>
TP_XDP_PCH_OBSFN_A<0> — NC_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1> — NC_XDP_PCH_OBSFN_A<1>
TP_XDP_PCH_OBSFN_D<0> — NC_XDP_PCH_OBSFN_D<0>
TP_XDP_PCH_OBSFN_D<1> — NC_XDP_PCH_OBSFN_D<1>
TP_XDP_PCH_TRST_L — NC_XDP_PCH_TRST_L

TP_1V05_S0_PCH_VCCAPLLEXP — NC_1V05_S0_PCH_VCCAPLLEXP
TP_AUD_CODEC_MICBIAS — NC_AUD_CODEC_MICBIAS
TP_AUD_MIC_INRP — NC_AUD_MIC_INRP
TP_AUD_MIC_INRN — NC_AUD_MIC_INRN
AUD_SPDIF_IN — AUD_SPDIF_IN
TP_BKL_FAULT — NC_BKL_FAULT
TP_LPC_DREQ0_L — NC_LPC_DREQ0_L

PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N

PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
PCIE_AP_D2R_P
PCIE_AP_D2R_N

PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N
PCIE_AP_R2D_PI_P
PCIE_AP_R2D_PI_N

PCIE_CLK100M_PCH_P
PCIE_CLK100M_PCH_N
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N

PCH_CLK100M_SATA_P

PCH_CLK33M_PCIIN

PCIE_CLK100M_SSD_P
PCIE_CLK100M_SSD_N
PEG_CLK100M_P
PEG_CLK100M_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N
PCIE_CLK100M_EXCARD_P
PCIE_CLK100M_EXCARD_N

SATA_HDD_R2D_RDRIN_P
SATA_HDD_R2D_RDRIN_N
SATA_HDD_D2R_RDROUT_P
SATA_HDD_D2R_RDROUT_N
SATA_HDD_D2R_RDRIN_P
SATA_HDD_D2R_RDRIN_N
SATA_HDD_R2D_RDROUT_P
SATA_HDD_R2D_RDROUT_N
SATA_HDD_D2R_RC_P
SATA_HDD_D2R_RC_N
SATA_HDD_R2D_RC_P

SATA_HDD_R2D_C_P
SATA_HDD_R2D_C_N
SATA_HDD_D2R_P
SATA_HDD_D2R_N

SATA_SSDRHDD_D2R_P
SATA_SSDRHDD_D2R_N
SATA_SSDRHDD_R2D_P
SATA_SSDRHDD_R2D_N

USB3_EXTA_RX_F_P
USB3_EXTA_RX_F_N
USB3_EXTA_RX_P
USB3_EXTA_RX_N

USB3_EXTA_TX_C_P
USB3_EXTA_TX_C_N
USB3_EXTA_TX_N
USB3_EXTA_RX_N

USB3_EXTB_RX_RC_P
USB3_EXTB_RX_RC_N
USB3_EXTB_RX_P
USB3_EXTB_RX_N

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Functional / ICT Test

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 7 OF 132
SHEET 7 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

G3H Rails

=PPBUS_G3H — PPBUS_G3H (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V, MAKE_BASE=TRUE)
- =PPBUS_S0_LCDBKLT
- =PPVIN_S5_HS_OTHER_ISNS_R
- =PPVIN_S5_HS_COMPUTING_ISNS_R
- =PPVIN_SW_TBTBST
- =PPBUS_S0_VSENSE
- =PPBUS_G3H_T25_R

=PPVIN_S5_HS_COMPUTING_ISNS — PPVIN_S5_HS_COMPUTING_ISNS (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.6V, MAKE_BASE=TRUE)
- =PPVIN_S0_CPUIMVP
- =PPVIN_S3_DDRREG
- =PPVIN_S0_CPUVCCIOS0
- =PPVIN_S0_CPUAXG
- =PPVIN_S0_VCCSAS0

=PPVIN_S5_HS_OTHER_ISNS — PPVIN_S5_HS_OTHER_ISNS (MIN_LINE_WIDTH=0.6 mm, VOLTAGE=12.6V, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE)
- =PPVIN_S5_P5VP3V3

=PP18V5_DCIN_CONN — PPDCIN_G3H (MIN_LINE_WIDTH=0.6 mm, VOLTAGE=18.5V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PPDCIN_S5_CHGR

=PP3V42_G3H_REG — PP3V42_G3H (MIN_LINE_WIDTH=0.3 mm, VOLTAGE=3.42V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PP3V3_S5_LPCPLUS
- =PP3V3_S5_SMC
- =PP3V42_G3H_CHGR
- =PP3V42_G3H_ONEWIREPROT
- =PP3V42_G3H_PWRCTL
- =PP3V42_G3H_SMBUS_SMC_5
- =PP3V42_G3H_SMCUSBMUX
- =PP3V42_G3H_TPAD
- =PPVIN_S5_SMCVREF
- =PPVBAT_G3_SYSCLK

=PP3V42_G3H_BMU
=PP3V42_G3H_AUDIO
=PP3V42_G3H_TDM
=PP3V42_S3_HALL

For PCH RTC Power

=PPVRTC_G3_OUT — PPVRTC_G3H (MIN_LINE_WIDTH=0.3 mm, VOLTAGE=3.42V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PPVRTC_G3_PCH

5V Rails

=PP5V_S5_LDO — PP5V_S5 (MIN_LINE_WIDTH=0.5 mm, VOLTAGE=5V, MIN_NECK_WIDTH=0.1 mm, MAKE_BASE=TRUE)
- =PP5V_S5_P1V5S3RS0FET
- =PP5V_S5_P5VSUSFET
- =PP5V_S5_TPAD

=PP5V_SUS_FET — PP5V_SUS (MIN_LINE_WIDTH=0.6 mm, VOLTAGE=5V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PP5V_SUS_PCH

=PP5V_S4_REG — PP5V_S4 (MIN_LINE_WIDTH=0.5 mm, VOLTAGE=5V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PP5V_S0_LCD
- =PP5V_S3_LTUSB
- =PP5V_S4_P5VS0FET
- =PP5V_S4_P5VS3FET
- =PP5V_S4_AUDIO
- =PP5V_S4_RIO
- =PP5V_S4_P1V05TBTS0
- =PP5V_S4_TPAD

=PP5V_S3_FET — PP5V_S3 (MIN_LINE_WIDTH=0.5 mm, VOLTAGE=5V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PP5V_S3_ISNS
- =PP5V_S3_ALSCAMERA
- =PP5V_S3_DDRREG
- =PP5V_S3_DEBUG_ADC_AVDD
- =PP5V_S3_DEBUG_ADC_DVDD
- =PP5V_S3_DEBUG_ISNS
- =PP5V_S3_MEMRESET

=PP5V_S0_FET — PP5V_S0 (MIN_LINE_WIDTH=0.4 mm, VOLTAGE=5V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PP5V_S0_AUDIO_XW
- =PP5V_S0_AUDIO
- =PP5V_S0_BKL
- =PP5V_S0_CPUIMVP
- =PP5V_S0_CPUVCCIOS0
- =PP5V_S0_FAN_LT
- =PP5V_S0_FAN_RT
- =PP5V_S0_KBDLED
- =PP5V_S0_LPCPLUS
- =PP5V_S0_PCH
- =PP5V_S0_HDD
- =PP5V_S0_RMC
- =PP5V_S0_VCCSAS0
- =PP5V_S0_VMON

3.3V Rails

=PP3V3_S4_FET — PP3V3_S4 (MIN_LINE_WIDTH=0.6 mm, VOLTAGE=3.3V, MIN_NECK_WIDTH=0.1 mm, MAKE_BASE=TRUE)
- =PP3V3_S4_TPAD
- =PP3V3_S4_SMC
- =PP3V3_S4_BT

=PP3V3_S4_TBT
=PP3V3_S4_RIO

=PP3V3_SUS_FET — PP3V3_SUS (MIN_LINE_WIDTH=0.6 mm, VOLTAGE=3.3V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PP3V3_SUS_P1V05SUSLDO
- =PP3V3_SUS_PCH_VCCSUS
- =PP3V3_SUS_PCH_VCCSUS_GPIO
- =PP3V3_SUS_PCH_GPIO
- =PP3V3_SUS_PCH_VCCSUS_USB
- =PP3V3_SUS_CNTRL
- =PP3V3_SUS_SMC

=PP3V3_SUS_PCH
=PP3V3_SUS_ROM
=PP3V3_SUS_PCH_VCC_SPI

=PP3V3_S5_REG — PP3V3_S5 (MIN_LINE_WIDTH=0.6 MM, VOLTAGE=3.3V, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE)
- =PP3V3_S0_P3V3S0FET
- =PP3V3_S3_P3V3S3FET
- =PP3V3_S4_TBTAPWRSW
- =PP3V3_S4_TBTBPWRSW
- =PP3V3_S4_P3V3S4FET
- =PP3V3_S5_CPU_VCCDDR
- =PP3V3_S5_P3V3SUSFET
- =PP3V3_S5_PCH
- =PP3V3_S5_PCHPWRGD
- =PP3V3_S5_PCH_GPIO
- =PP3V3_S5_PCH_VCCDSW
- =PP3V3_S5_PWRCTL
- =PP3V3_S5_SMCBATLOW
- =PP3V3_S5_SYSCLK
- =PP3V3_S5_VMON
- =PP3V3_S5_XDP
- =PP3V3_S5_P1V5S0

=PP3V3_S3_FET — PP3V3_S3 (MIN_LINE_WIDTH=0.58MM, VOLTAGE=3.3V, MIN_NECK_WIDTH=0.28MM, MAKE_BASE=TRUE)
- =PP3V3_S3_ISNS
- =PP3V3_S3_MEMRESET
- =PP3V3_S3_PCH_GPIO
- =PP3V3_S3_RIO
- =PP3V3_S3_SMBUS_SMC_2_S3
- =PP3V3_S3_SMBUS_SMC_3
- =PP3V3_S3_USBMUX
- =PP3V3_S3_USB_HUB
- =PP3V3_S3_USB_RESET
- =PP3V3_S3_VREFMRGN
- =PP3V3_S3_WLAN
- =PP3V3_S3_GYRO
- =PP3V3_S3_SMS
- =PP3V3_S3_SDBUF
- =PP3V3_S3_CAMERA
- =PP3V3_S3_P1V2S3
- =PP3V3_S3_P1V8S3
- =PP3V3_S3_BT

=PP3V3_S0_FET — PP3V3_S0 (MIN_LINE_WIDTH=0.5 MM, VOLTAGE=3.3V, MIN_NECK_WIDTH=0.075 mm, MAKE_BASE=TRUE)
- =PP3V3_S0_AUDIO
- =PP3V3_S0_AUDIO_DIG
- =PP3V3_S0_BKL_VDDIO
- =PP3V3_S0_CPUTHMSNS
- =PP3V3_S0_P1V5S0
- =PP3V3_S0_P1V8S0
- =PP3V3_S0_BKLI2C
- =PP3V3_S0_DDCMUX
- =PP3V3_S0_FAN_LT
- =PP3V3_S0_FAN_RT
- =PP3V3_S0_GPUTHMSNS
- =PP3V3_S0_HS_ISNS
- =PP3V3_S0_IMVPISNS
- =PP3V3_S0_ISNS
- =PP3V3_S0_CPU_VCCIO_SEL
- =PP3V3_S0_LCD
- =PP3V3_S0_P3V3TBTFET
- =PP3V3_S0_PCH
- =PP3V3_S0_PCH_GPIO
- =PP3V3_S0_PCH_VCC3_3_CLK
- =PP3V3_S0_PCH_VCC3_3_GPIO
- =PP3V3_S0_PCH_VCC3_3_HVCMOS
- =PP3V3_S0_PCH_VCC3_3_PCI
- =PP3V3_S0_PCH_VCC3_3_SATA
- =PP3V3_S0_PCH_VCCADAC
- =PP3V3_S0_PCH_VCC3_3
- =PP3V3_S0_PWRCTL
- =PP3V3_S0_RSTBUF
- =PP3V3_S0_SATAMUX
- =PP3V3_S0_SB_PM
- =PP3V3_S0_SMBUS_PCH
- =PP3V3_S0_SMBUS_SMC_0_S0
- =PP3V3_S0_SMBUS_SMC_1_S0
- =PP3V3_S0_SSD
- =PP3V3_S0_SYSCLK
- =PP3V3_S0_TBTI2C
- =PP3V3_S0_TBTPWRCTL
- =PP3V3_S0_HDMI
- =PP3V3_S0_TPAD
- =PP3V3_S0_VMON
- =PP3V3_S0_XDP
- =PP3V3_S0_DDR3THMSNS
- =PP3V3_S0_SPKRTHMSNS
- =PP3V3_S0_HS_COMPUTING_ISNS
- =PP3V3_S0_HS_OTHER_ISNS
- =PP3V3_S0_PCH_STRAPS

1.8V/1.5V/1.2V/1.05V Rails

=PP1V8_S0_REG — PP1V8_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.8V, MAKE_BASE=TRUE)
2A max supply
- =PP1V8R1V5_S0_PCH_VCCVRM
- =PP1V8_S0_AUDIO
- =PP1V8_S0_CPU_VCCPLL
- =PP1V8_S0_PCH_VCC_DFTERM
- =PPVDDIO_S0_SBCLK

=PP1V8_S0_CPU_VCCPLL_R — PP1V8_S0_CPU_VCCPLL_R (MIN_LINE_WIDTH=0.5 MM, VOLTAGE=1.8V, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE)

=PPDDR_S3_REG — PP1V5R1V35_S3 (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.17 mm, VOLTAGE=1.35V, MAKE_BASE=TRUE)
- =PPDDR_S3_MEMVREF
- =PPVIN_S3_P1V5S3RS0_FET
- =PPVIN_S0_DDRREG_LDO
- =PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS — PP1V5R1V35_MEM (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.17 mm, VOLTAGE=1.35V, MAKE_BASE=TRUE)
- =PP1V5R1V35_S3_MEM_A
- =PP1V5R1V35_S3_MEM_B
- =PP1V5_S3_MEMRESET

=PP1V5_S3RS0_FET — PP1V5_S3RS0_CPUDDR (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V5_S3RS0_VMON
- =PP1V5R1V35_S3_CPU_VCCDDR

=PP1V5_S0_REG — PP1V5_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.15 MM, VOLTAGE=1.5V, MAKE_BASE=TRUE)
- =PP1V5_S0_AUDIO
- =PP3V3R1V5_S0_PCH_VCCSUSHDA
- =PP1V5_S0_RDRVR

=PPVTT_S3_DDR_BUF — PPVTTDDR_S3 (MIN_LINE_WIDTH=0.3 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=0.675V, MAKE_BASE=TRUE)

=PPVTT_S0_DDR_LDO — PP0V75_S0_DDRVTT (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.17 mm, VOLTAGE=0.675V, MAKE_BASE=TRUE)
- =PP0V75_S0_MEM_VTT_A
- =PP0V75_S0_MEM_VTT_B
- =PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO — PP1V05_SUS (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_SUS_PCH_JTAG

=PPCPUVCCIO_S0_REG — PP1V05_S0 (MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.15 MM, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_S0_CPU_VCCIO
- =PPVCCIO_S0_XDP
- =PPVCCIO_S0_CPUIMVP
- =PPVCCIO_S0_SMC
- =PP1V05_S0_VMON
- =PP1V05_S0_RMC
- =PP1V05_S0_PCH_VCCIO_PLLPCIE
- =PP1V05_S0_PCH_VCCADPLL
- =PP1V05_S0_PCH_VCCIO
- =PP1V05_S0_PCH_VCCIO_PCIE
- =PP1V05_S0_PCH_VCCIO_SATA
- =PP1V05_S0_PCH_VCCIO_CLK
- =PP1V05_S0_PCH_VCCIO_USB
- =PP1V05_S0_PCH_VCC_CORE
- =PP1V05_S0_PCH_VCCASW
- =PP1V05_S0_PCH_VCCIO_CLK
- =PP1V05_S0_PCH_VCCDIFFCLK
- =PP1V05_S0_PCH
- =PP1V05_S0_PCH_VCCSSC
- =PP1V05_S0_PCH_V_PROC_IO
- =PP1V05_S0_PCH_VCCIO_PLLUSB
- =PP1V05_S0_PCH_VCC_DMI
- =PP1V05_S0_PCH_VCCIO_PLLFDI
- =PP1V05_S0_PCH_VCCDMI_FDI

=PPBUS_G3H_T25 — PPBUS_G3H_T25_PWR (MIN_LINE_WIDTH=0.6 MM, MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=12.8V)

Backlight Rails

=PPBUS_SW_BKL — PPBUS_SW_BKL (MIN_LINE_WIDTH=0.6 MM, MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=12.6V)
- PPBUS_S0_LCDBKLT_PWR

=PP18V5_DCIN_ISOL — PPDCIN_G3H_ISOL (MIN_LINE_WIDTH=0.3 MM, VOLTAGE=18.5V, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE)
- =PPDCIN_S5_CHGR_ISOL
- =PPDCIN_S5_VSENSE

TBT Rails (off when no cable)

PPVIN_SW_TBTBST (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=12.8V)

=PP15V_TBT_REG — PP15V_TBT (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE)
- =PPHV_SW_TBTAPWRSW
- =PPHV_SW_TBTBPWRSW

=PP3V3_TBTLC_FET — PP3V3_TBTLC (MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE)
- =PP3V3_TBT_PCH_GPIO
- =PP3V3_TBTLC_RTR
- =PPVDDIO_TBT_CLK
- =PP3V3_TBT_PCH_GPIO

=PP1V05_S0_P1V05TBTREG_R — PP1V05_S0_P1V05TBTREG_R (MIN_LINE_WIDTH=0.4 MM, VOLTAGE=1.05V, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE)

=PP1V05_S0_P1V05TBTREG — PP1V05_S0_P1V05TBTREG (MIN_LINE_WIDTH=0.4 MM, VOLTAGE=1.05V, MIN_NECK_WIDTH=0.2 MM, MAKE_BASE=TRUE)
- =PP1V05_TBTLC_RTR
- =PP1V05_TBTLC

=PP1V05_TBTCIO_FET — PP1V05_TBTCIO (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V, MAKE_BASE=TRUE)
- =PP1V05_TBTCIO_RTR

Chipset "VCore" Rails

=PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU (MIN_LINE_WIDTH=0.6 mm, MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.25V)
- =PPVCORE_S0_CPU

=PPVCORE_S0_AXG_REG — PPVCORE_S0_AXG (MIN_LINE_WIDTH=0.6 mm, MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.05V)
- =PPVCORE_S0_CPU_VCCAXG

=PP1V5_S3_CPU_VCCDQ — PP1V5_S3_CPU_VCCDQ (MIN_LINE_WIDTH=0.6 mm, MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.5V)

=PP1V05_S0_CPU_VCCPQE — PP1V05_S0_CPU_VCCPQE (MIN_LINE_WIDTH=0.6 mm, VOLTAGE=1.05V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)

=PPVCCSA_S0_REG — PPVCCSA_S0_REG (MIN_LINE_WIDTH=0.6 mm, VOLTAGE=0.9V, MIN_NECK_WIDTH=0.2 mm, MAKE_BASE=TRUE)
- =PPVCCSA_S0_CPU

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Power Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 8 OF 132

SHEET: 8 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Frame Holes

ZT0940 4P5R2P3-3P5B
ZT0960 4P5R2P3-3P5B

Bosses for limiting deflection

SH0910 2.8OD1.2ID-2.25H-SM-D1 APN:860-1557
SH0911 2.8OD1.2ID-2.25H-SM-D1
SH0912 2.8OD1.2ID-2.25H-SM-D1
SH0913 2.8OD1.2ID-2.25H-SM-D1

SH0950 SM SHLD-D1-USB
SH0951 SM SHLD-D1-MLB-T29

D1 THERMAL MODULE STANDOFF (860-1439)

SH0920 STDOFF-4.5OD2.15H-SM
SH0921 STDOFF-4.5OD2.15H-SM
SH0926 STDOFF-4.5OD2.15H-SM
SH0927 STDOFF-4.5OD2.15H-SM

D1 BMU MODULE STANDOFFS

SH0928 STDOFF-4.5OD1.73H-SM
SH0963 STDOFF-4.5OD2.33H-SM
APN: 860-1490

SH0963 is BMU standoff with flange. 860-1534

TH0900 for upper TBT can gnd slot

TH0903 for lower TBT can gnd slot

TH0904,5 for USB can gnd slot

FAN BOSSES (4X 860-1327)

SH0922 STDOFF-4.5OD1.8H-SM
SH0923 STDOFF-4.5OD1.8H-SM
SH0924 STDOFF-4.5OD1.8H-SM
SH0925 STDOFF-4.5OD1.8H-SM

D1 POGO PINS (870-2451)

SH0932 POGO-2.3OD-5.5H-SM-LOW-FORCE
SH0933 POGO-2.3OD-4.1H-SM-LOW-FORCE
SH0934 POGO-2.3OD-5.5H-SM-LOW-FORCE
SH0935 POGO-2.3OD-5.5H-SM-LOW-FORCE
SH0936 POGO-2.3OD-5.5H-SM-LOW-FORCE
SH0937 POGO-2.3OD-5.5H-SM-LOW-FORCE

D1 ELIPTICAL SLOT HOLES

ZT0930 SL-13.9X2.3-4.2x2.6
ZT0920 SL-12.8X1.8-3.1x2.1
ZT0931 SL-13.9X2.3-4.2x2.6

TH0900 SL-1.1X0.5-1.4x0.8
TH0903 APN:862-0118 SL-1.1X0.5-1.4x0.8
TH0904 APN:998-3975 SL-1.1X0.45-1.4x0.75
TH0905 SL-1.1X0.45-1.4x0.75

eDP signals

79 67 DP_INT_AUX_C_P (MAKE_BASE=TRUE)	—	TP_EDP_AUX_P 10
79 67 DP_INT_AUX_C_N (MAKE_BASE=TRUE)	—	TP_EDP_AUX_N 10
79 67 DP_INT_ML_C_P<3..0> (MAKE_BASE=TRUE)	—	TP_EDP_TX_P<3..0> 10
79 67 DP_INT_ML_C_N<3..0> (MAKE_BASE=TRUE)	—	TP_EDP_TX_N<3..0> 10

71 7 LCD_BKLT_PWM (MAKE_BASE=TRUE)	—	LVDS_IG_BKL_PWM 18
71 LCD_BKLT_EN (MAKE_BASE=TRUE)	—	LVDS_IG_BKL_ON 18
67 LCD_PWR_EN (MAKE_BASE=TRUE)	—	LVDS_IG_PANEL_PWR 18

CR SFF DG v1p0 Table 3-56 mapping for HDMI

78 36 7 HDMI_IG_CLK_C_P (MAKE_BASE=TRUE)	—	TP_DP_IG_B_MLP<3> 18
78 36 7 HDMI_IG_CLK_C_N (MAKE_BASE=TRUE)	—	TP_DP_IG_B_MLN<3> 18
78 36 7 HDMI_IG_DATA_C_P<2..0> (MAKE_BASE=TRUE)	—	TP_DP_IG_B_MLP<0..2> 18
78 36 7 HDMI_IG_DATA_C_N<2..0> (MAKE_BASE=TRUE)	—	TP_DP_IG_B_MLN<0..2> 18
36 7 HDMI_IG_DDC_CLK (MAKE_BASE=TRUE)	—	DPA_IG_DDC_CLK 18
HDMI_IG_DDC_DATA (MAKE_BASE=TRUE)	—	DPA_IG_DDC_DATA 18
36 HDMI_HPD (MAKE_BASE=TRUE)	—	DPA_IG_HPD 18

79 33 DP_TBTSNK0_AUXCH_C_P (MAKE_BASE=TRUE)	—	DPB_IG_AUX_CH_P 18
79 33 DP_TBTSNK0_AUXCH_C_N (MAKE_BASE=TRUE)	—	DPB_IG_AUX_CH_N 18
79 33 DP_TBTSNK0_ML_C_P<3..0> (MAKE_BASE=TRUE)	—	TP_DP_IG_C_MLP<3..0> 18
79 33 DP_TBTSNK0_ML_C_N<3..0> (MAKE_BASE=TRUE)	—	TP_DP_IG_C_MLN<3..0> 18
68 DP_TBTSNK0_DDC_CLK (MAKE_BASE=TRUE)	—	DPB_IG_DDC_CLK 18
68 DP_TBTSNK0_DDC_DATA (MAKE_BASE=TRUE)	—	DPB_IG_DDC_DATA 18
33 DP_TBTSNK0_HPD (MAKE_BASE=TRUE)	—	DPB_IG_HPD 18
79 33 DP_TBTSNK1_AUXCH_C_P (MAKE_BASE=TRUE)	—	TP_DP_IG_D_AUXP 18
79 33 DP_TBTSNK1_AUXCH_C_N (MAKE_BASE=TRUE)	—	TP_DP_IG_D_AUXN 18
79 33 DP_TBTSNK1_ML_C_P<3..0> (MAKE_BASE=TRUE)	—	TP_DP_IG_D_MLP<3..0> 18
79 33 DP_TBTSNK1_ML_C_N<3..0> (MAKE_BASE=TRUE)	—	TP_DP_IG_D_MLN<3..0> 18
68 DP_TBTSNK1_DDC_CLK (MAKE_BASE=TRUE)	—	TP_DP_IG_D_CTRL_CLK 18
68 DP_TBTSNK1_DDC_DATA (MAKE_BASE=TRUE)	—	TP_DP_IG_D_CTRL_DATA 18
33 DP_TBTSNK1_HPD (MAKE_BASE=TRUE)	—	TP_DP_IG_D_HPD 18

NC_PCH_GPIO64_CLKOUTFLEX0 (MAKE_BASE=TRUE)	—	TP_PCH_GPIO64_CLKOUTFLEX0 17
NC_PCH_GPIO65_CLKOUTFLEX1 (MAKE_BASE=TRUE)	—	TP_PCH_GPIO65_CLKOUTFLEX1 17
NC_PCH_GPIO66_CLKOUTFLEX2 (MAKE_BASE=TRUE)	—	TP_PCH_GPIO66_CLKOUTFLEX2 17
NC_PCH_GPIO67_CLKOUTFLEX3 (MAKE_BASE=TRUE)	—	TP_PCH_GPIO67_CLKOUTFLEX3 17

MLB_RAMCFG3 20
MLB_RAMCFG2 20
MLB_RAMCFG1 20
MLB_RAMCFG0 20

RAMCFG0:L R0910[1] 1K 5% 1/20W MF 0201[2]
RAMCFG1:L R0911[1] 1K 5% 1/20W MF 0201[2]
RAMCFG2:L R0912[1] 1K 5% 1/20W MF 0201[2]
RAMCFG3:L R0913[1] 1K 5% 1/20W MF 0201[2]

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

Digital Ground

8 =PP5V_S0_AUDIO_XW

XW0902 SM 1 2 PP5V_S0_AUDIO_AMP_L 53
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XW0903 SM 1 2 PP5V_S0_AUDIO_AMP_R 53
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

CPU signals

27 MEMVTT_EN (MAKE_BASE=TRUE)	—	=DDRVTT_EN 27 60

T29 Signals Through PEG

75 33 7 PCIE_TBT_D2R_P<3..0> (MAKE_BASE=TRUE)	—	=PEG_D2R_P<11..8> 10
75 33 7 PCIE_TBT_D2R_N<3..0> (MAKE_BASE=TRUE)	—	=PEG_D2R_N<11..8> 10
75 33 7 PCIE_TBT_R2D_C_P<3..0> (MAKE_BASE=TRUE)	—	=PEG_R2D_C_P<11..8> 10
75 33 7 PCIE_TBT_R2D_C_N<3..0> (MAKE_BASE=TRUE)	—	=PEG_R2D_C_N<11..8> 10

SD_PWR_EN_PCH (MAKE_BASE=TRUE)	—	ENET_LOW_PWR_PCH 20 24 25
36 7 SD_PWR_EN (MAKE_BASE=TRUE)	—	ENET_LOW_PWR 25
TP_FW_PWR_EN (MAKE_BASE=TRUE)	—	FW_PWR_EN 25

NC_CPU_THERMDN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	CPU_THERMD_N 10 78
NC_CPU_THERMDP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	CPU_THERMD_P 10 78
NC_LCD_FSS (MAKE_BASE=TRUE NO_TEST=TRUE)	—	LCD_FSS 67

NC_PCIE_CLK100M_SSDN (MAKE_BASE=TRUE TRUE)	—	PCIE_CLK100M_SSD_N 7 17 75
NC_PCIE_CLK100M_SSDP (MAKE_BASE=TRUE TRUE)	—	PCIE_CLK100M_SSD_P 7 17 75
NC_PCIE_CLK100M_FWN (MAKE_BASE=TRUE TRUE)	—	PCIE_CLK100M_FW_N 7 17 75
NC_PCIE_CLK100M_FWP (MAKE_BASE=TRUE TRUE)	—	PCIE_CLK100M_FW_P 7 17 75

Unused PEG signals

NC_PEG_D2RP<15..12> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	=PEG_D2R_P<15..12> 10
NC_PEG_D2RN<15..12> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	=PEG_D2R_N<15..12> 10
NC_PEG_R2D_CP<15..12> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	=PEG_R2D_C_P<15..12> 10
NC_PEG_R2D_CN<15..12> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	=PEG_R2D_C_N<15..12> 10

NC_PCIE_FW_D2RN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	PCIE_FW_D2R_N 17
NC_PCIE_FW_D2RP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	PCIE_FW_D2R_P 17
NC_PCIE_FW_R2D_CN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	PCIE_FW_R2D_C_N 17
NC_PCIE_FW_R2D_CP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	PCIE_FW_R2D_C_P 17

Unused GPU signals

NC_PEG_D2RP<7..0> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	=PEG_D2R_P<7..0> 10
NC_PEG_D2RN<7..0> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	=PEG_D2R_N<7..0> 10
NC_PEG_R2D_CP<7..0> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	=PEG_R2D_C_P<7..0> 10
NC_PEG_R2D_CN<7..0> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	=PEG_R2D_C_N<7..0> 10

NC_DPA_IG_AUX_CHP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	DPA_IG_AUX_CH_P 18
NC_DPA_IG_AUX_CHN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	DPA_IG_AUX_CH_N 18

NC_PEG_CLK100MN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	PEG_CLK100M_N 7 17 75
NC_PEG_CLK100MP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	PEG_CLK100M_P 7 17 75

UNUSED USB SIGNALS

NC_USB3_EXTC_TXP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB3_EXTC_TX_P 19
NC_USB3_EXTC_TXN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB3_EXTC_TX_N 19
NC_USB3_EXTC_RXP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB3_EXTC_RX_P 19
NC_USB3_EXTC_RXN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB3_EXTC_RX_N 19
NC_USB_EXTCP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB_EXTC_P 19
NC_USB_EXTCN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB_EXTC_N 19
NC_USB3_EXTD_TXP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB3_EXTD_TX_P 19
NC_USB3_EXTD_TXN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB3_EXTD_TX_N 19
NC_USB3_EXTD_RXP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB3_EXTD_RX_P 19
NC_USB3_EXTD_RXN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB3_EXTD_RX_N 19
NC_USB_EXTD_EHCIP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB_EXTD_EHCI_P 19
NC_USB_EXTD_EHCIN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	USB_EXTD_EHCI_N 19
NC_USB_4N (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_4N 19
NC_USB_4P (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_4P 19
NC_USB_SDN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_SDN 19
NC_USB_SDP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_SDP 19
NC_USB_WLANN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_WLANN 19
NC_USB_WLANP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_WLANP 19
NC_USB_BT_HSN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_BT_HSN 19
NC_USB_BT_HSP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_BT_HSP 19
NC_USB_12N (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_12N 19
NC_USB_12P (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_12P 19
NC_USB_13N (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_13N 19
NC_USB_13P (MAKE_BASE=TRUE NO_TEST=TRUE)	—	TP_USB_13P 19

Unused SATA ODD Signals

NC_SATA_ODD_D2RN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	SATA_ODD_D2R_N 17
NC_SATA_ODD_D2RP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	SATA_ODD_D2R_P 17
NC_SATA_ODD_R2D_CN (MAKE_BASE=TRUE NO_TEST=TRUE)	—	SATA_ODD_R2D_C_N 17
NC_SATA_ODD_R2D_CP (MAKE_BASE=TRUE NO_TEST=TRUE)	—	SATA_ODD_R2D_C_P 17

Unused Memory Signals

NC_MEM_A_CLKP<1> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	MEM_A_CLK_P<1> 12
NC_MEM_A_CLKN<1> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	MEM_A_CLK_N<1> 12
NC_MEM_B_CLKP<1> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	MEM_B_CLK_P<1> 12
NC_MEM_B_CLKN<1> (MAKE_BASE=TRUE NO_TEST=TRUE)	—	MEM_B_CLK_N<1> 12

66 8 =PP3V3_S0_PWRCTL

R0991[1] 10K 5% 1/20W MF 0201[2]

Unused PGOOD signal

CPUIMVP_AXG_PGOOD 61

TP_P1V5S3RS0_RAMP_DONE (MAKE_BASE=TRUE)	—	P1V5S3RS0_RAMP_DONE 65
TP_DDRREG_PGOOD (MAKE_BASE=TRUE)	—	DDRREG_PGOOD 60

USB SIGNALS

74 36 7 USB_BT_P (MAKE_BASE=TRUE)	—	USBHUB_DN1_P 26
74 36 7 USB_BT_N (MAKE_BASE=TRUE)	—	USBHUB_DN1_N 26
74 47 USB_TPAD_P (MAKE_BASE=TRUE)	—	USBHUB_DN2_P 26
74 47 USB_TPAD_N (MAKE_BASE=TRUE)	—	USBHUB_DN2_N 26
74 39 USB_SMC_P (MAKE_BASE=TRUE)	—	USBHUB_DN3_P 26
74 39 USB_SMC_N (MAKE_BASE=TRUE)	—	USBHUB_DN3_N 26
78 PU_USBHUB_DN4_P (MAKE_BASE=TRUE)	—	USBHUB_DN4_P 26
78 PU_USBHUB_DN4_N (MAKE_BASE=TRUE)	—	USBHUB_DN4_N 26

SYNC_MASTER=D1_MLB_TEST SYNC_DATE=01/27/2012

PAGE TITLE

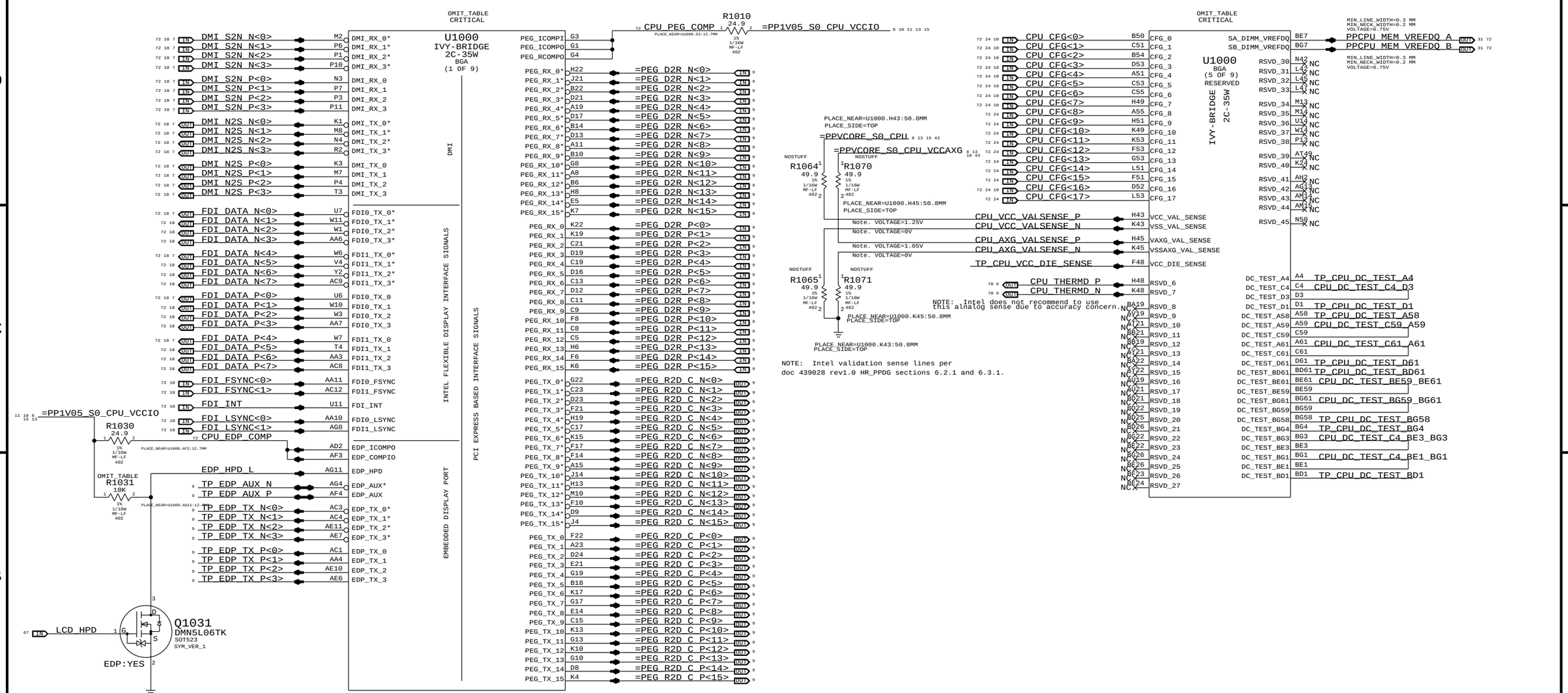
Signal Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 9 OF 132
SHEET 9 OF 80

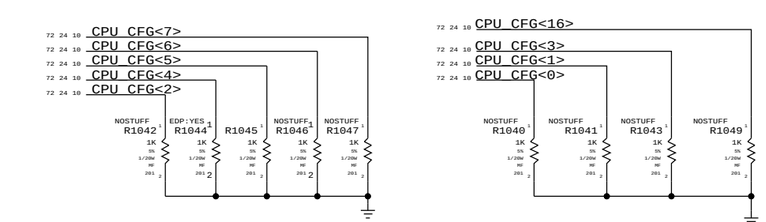
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.



NOTE: Intel does not recommend to use this alnalog sense due to accuracy concern.

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.



These can be Placed close to J2500 and Only for debug access

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8	01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0066	1	RES,MTL FILM,1/16W,1K,0402,SMD,LF	R1031		EDP:YES
116S0090	1	RES,MTL FILM,1/16W,10K,0402,SMD,LF	R1031		EDP:NO

Intel Doc 460452 ChiefRiver Platform design guild rev1.0 section 2.2.12 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if Internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

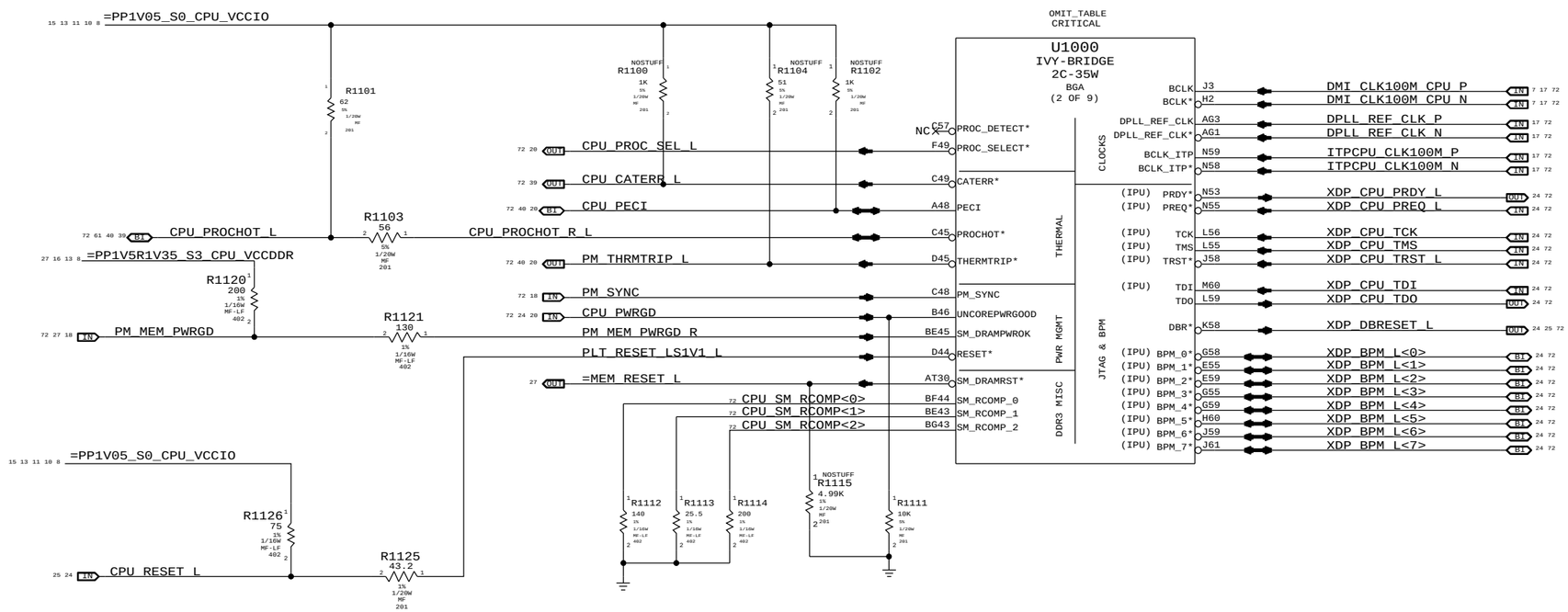
SYNC MASTER=J30_MLB SYNC_DATE=07/14/2013

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 10 OF 132
SHEET 10 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2013

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

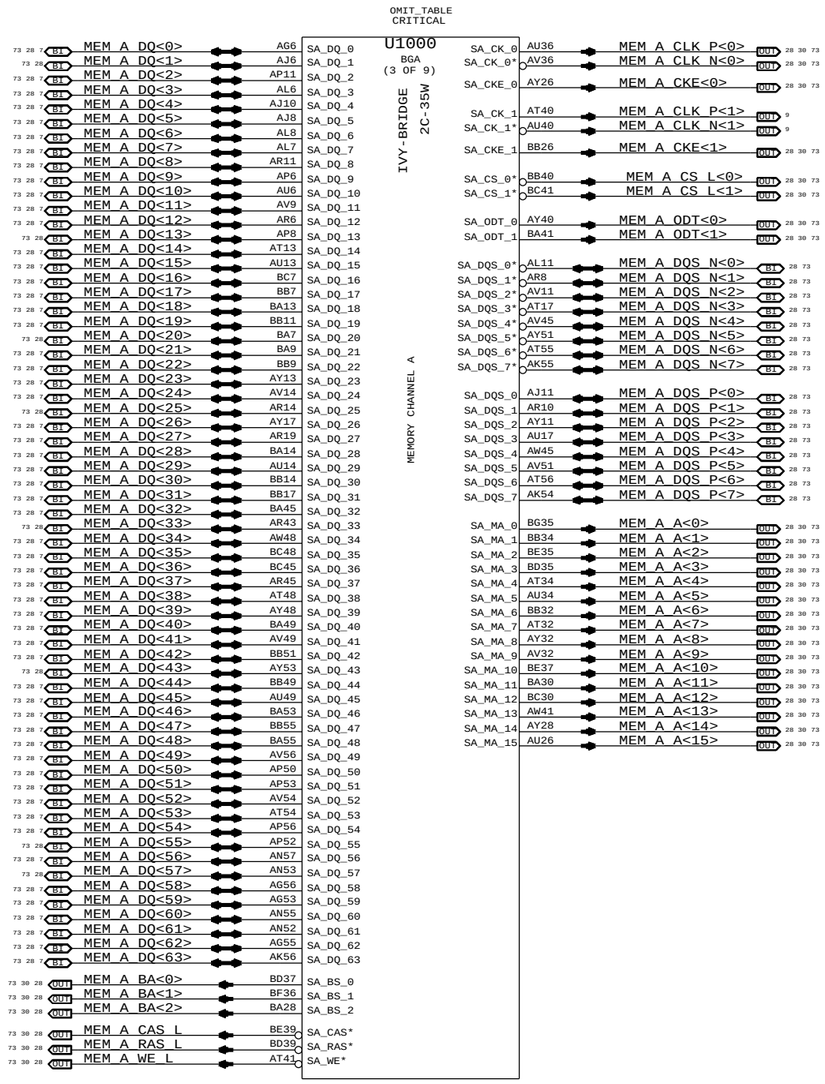
REVISION <E4LABEL>

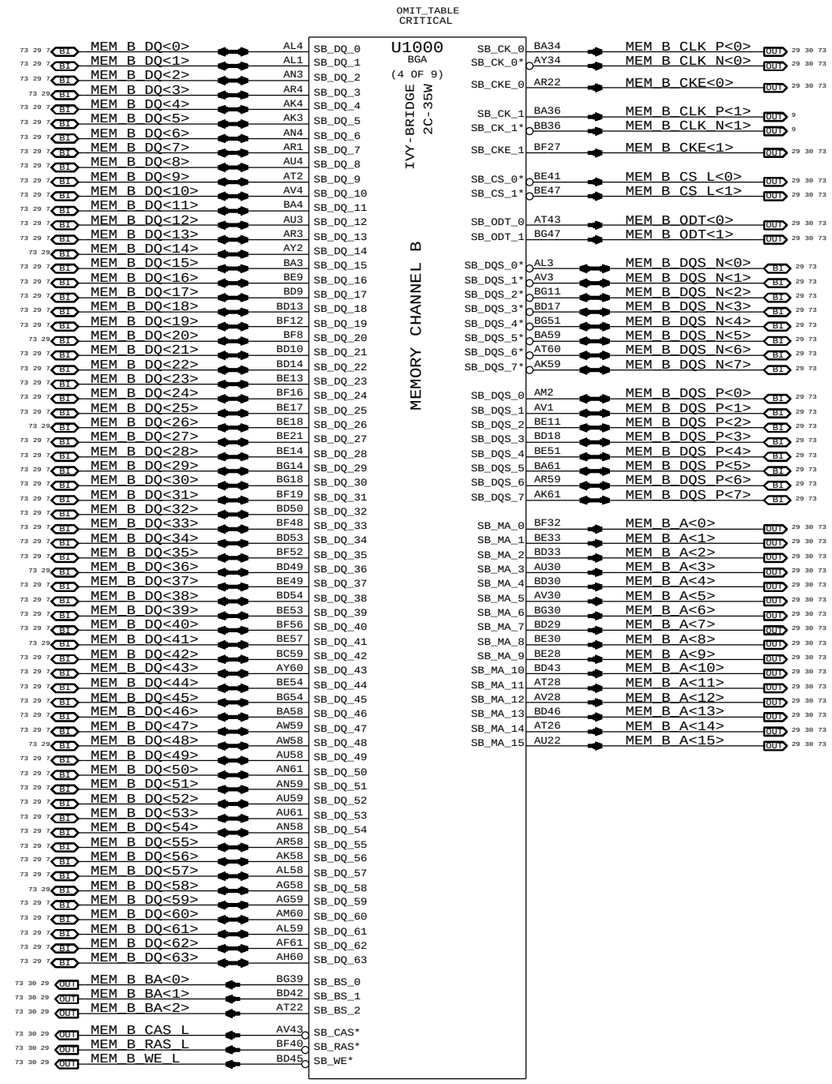
BRANCH <BRANCH>

PAGE 11 OF 132

SHEET 11 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





SYNC_MASTER=J30_MLB SYNC_DATE=07/14/2011

PAGE TITLE

CPU DDR3 INTERFACES

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

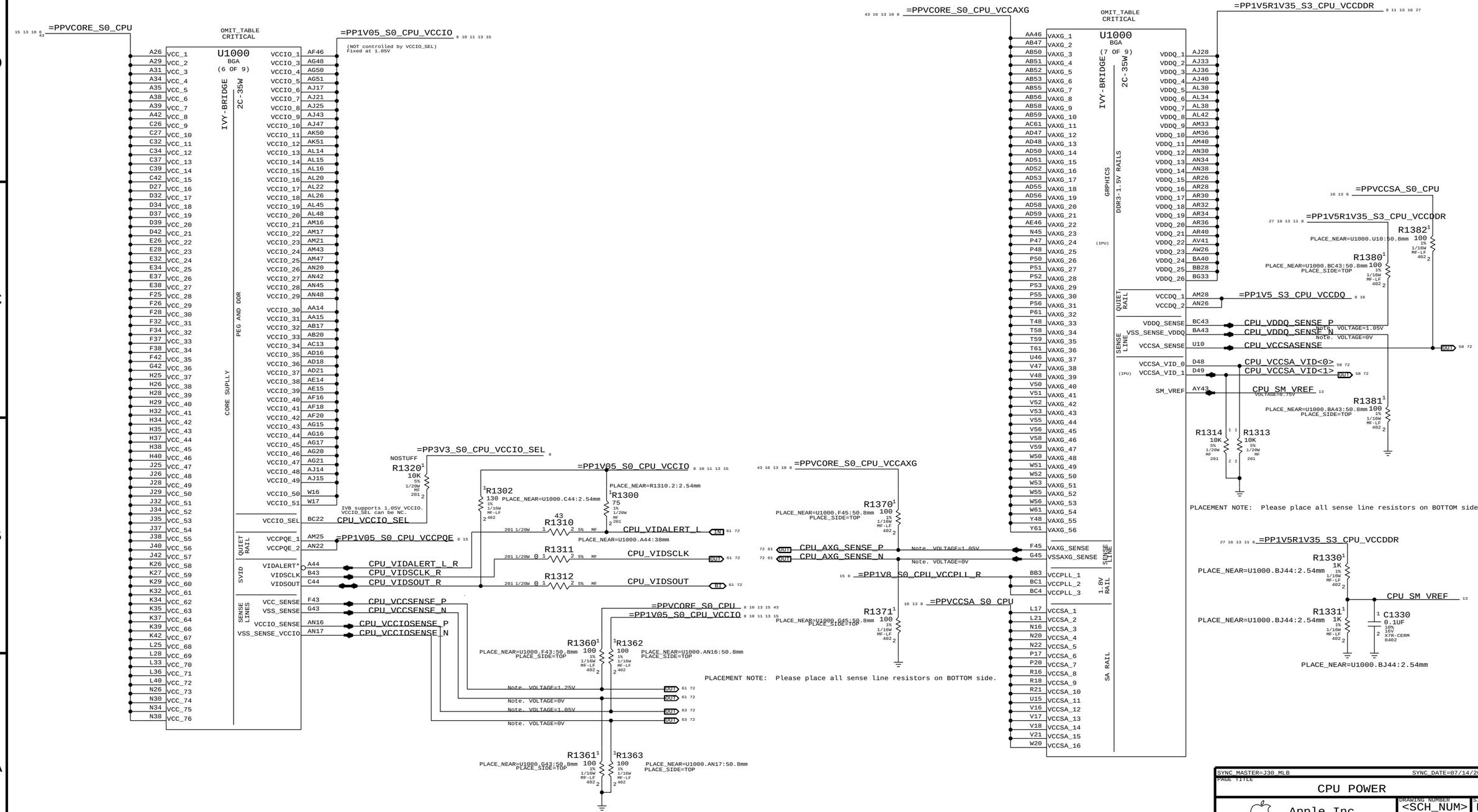
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 12 OF 132

SHEET 12 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=J30_MLB SYNC_DATE=07/14/2013

PAGE TITLE

CPU POWER

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 13 OF 132

SHEET: 13 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE
CRITICAL

U1000
BGA
(9 OF 9)
IVY-BRIDGE
2C-35W

BG13	VSS	VSS	M11
BG17	VSS	VSS	M15
BG21	VSS	VSS	M58
BG24	VSS	VSS	N1
BG28	VSS	VSS	N17
BG37	VSS	VSS	N21
BG41	VSS	VSS	N25
BG45	VSS	VSS	N28
BG49	VSS	VSS	N33
BG53	VSS	VSS	N36
C29	VSS	VSS	N40
C35	VSS	VSS	N43
C40	VSS	VSS	N47
D4	VSS	VSS	N48
D6	VSS	VSS	N51
D10	VSS	VSS	N52
D14	VSS	VSS	N56
D18	VSS	VSS	N61
D22	VSS	VSS	P9
D26	VSS	VSS	P14
D29	VSS	VSS	P16
D35	VSS	VSS	P18
D40	VSS	VSS	P21
D43	VSS	VSS	P58
D46	VSS	VSS	P59
D50	VSS	VSS	R4
D54	VSS	VSS	R17
D58	VSS	VSS	R20
E3	VSS	VSS	R46
E25	VSS	VSS	T1
E29	VSS	VSS	T47
E35	VSS	VSS	T50
E40	VSS	VSS	T51
F13	VSS	VSS	T52
F15	VSS	VSS	T53
F19	VSS	VSS	T55
F29	VSS	VSS	T56
F35	VSS	VSS	U8
F40	VSS	VSS	U13
F55	VSS	VSS	V20
G6	VSS	VSS	V61
G48	VSS	VSS	W8
G51	VSS	VSS	W13
G61	VSS	VSS	W15
H4	VSS	VSS	W18
H10	VSS	VSS	W21
H14	VSS	VSS	W46
H17	VSS	VSS	Y4
H21	VSS	VSS	Y47
H53	VSS	VSS	Y58
H58	VSS	VSS	Y59
J1	VSS		
J49	VSS		
J55	VSS		
K8	VSS		
K11	VSS		
K21	VSS	VSS_NCTF	A5
K51	VSS	VSS_NCTF	A57
L16	VSS	VSS_NCTF	BC61
L20	VSS	VSS_NCTF	BD3
L22	VSS	VSS_NCTF	BD59
L26	VSS	VSS_NCTF	BE4
L30	VSS	VSS_NCTF	BE58
L34	VSS	VSS_NCTF	BG5
L38	VSS	VSS_NCTF	BG57
L43	VSS	VSS_NCTF	C3
L48	VSS	VSS_NCTF	C58
L61	VSS	VSS_NCTF	D59
M4	VSS	VSS_NCTF	E1
M6	VSS	VSS_NCTF	E61

OMIT_TABLE
CRITICAL

U1000
BGA
(8 OF 9)
IVY-BRIDGE
2C-35W

A9	VSS	VSS	AM34
A13	VSS	VSS	AM38
A17	VSS	VSS	AM42
A21	VSS	VSS	AM45
A25	VSS	VSS	AM48
A28	VSS	VSS	AM58
A33	VSS	VSS	AN1
A37	VSS	VSS	AN21
A40	VSS	VSS	AN25
A45	VSS	VSS	AN28
A49	VSS	VSS	AN33
A53	VSS	VSS	AN36
AA1	VSS	VSS	AN40
AA8	VSS	VSS	AN43
AA13	VSS	VSS	AN47
AA50	VSS	VSS	AN50
AA51	VSS	VSS	AN54
AA52	VSS	VSS	AP7
AA53	VSS	VSS	AP10
AA55	VSS	VSS	AP51
AA56	VSS	VSS	AP55
AB16	VSS	VSS	AR7
AB18	VSS	VSS	AR13
AB21	VSS	VSS	AR17
AB48	VSS	VSS	AR21
AB61	VSS	VSS	AR41
AC6	VSS	VSS	AR48
AC10	VSS	VSS	AR61
AC14	VSS	VSS	AT4
AC46	VSS	VSS	AT14
AD4	VSS	VSS	AT19
AD17	VSS	VSS	AT36
AD20	VSS	VSS	AT45
AD61	VSS	VSS	AT52
AE8	VSS	VSS	AT58
AE13	VSS	VSS	AU1
AF1	VSS	VSS	AU7
AF17	VSS	VSS	AU11
AF21	VSS	VSS	AU28
AF47	VSS	VSS	AU32
AF48	VSS	VSS	AU51
AF50	VSS	VSS	AV17
AF51	VSS	VSS	AV21
AF52	VSS	VSS	AV22
AF53	VSS	VSS	AV34
AF55	VSS	VSS	AV40
AF56	VSS	VSS	AV48
AF58	VSS	VSS	AV55
AF59	VSS	VSS	AW7
AG7	VSS	VSS	AW13
AG10	VSS	VSS	AW43
AG14	VSS	VSS	AW61
AG18	VSS	VSS	AY4
AG47	VSS	VSS	AY9
AG52	VSS	VSS	AY14
AG61	VSS	VSS	AY19
AH4	VSS	VSS	AY30
AH58	VSS	VSS	AY36
AJ7	VSS	VSS	AY41
AJ13	VSS	VSS	AY45
AJ16	VSS	VSS	AY49
AJ20	VSS	VSS	AY55
AJ22	VSS	VSS	AY58
AJ26	VSS	VSS	BA1
AJ30	VSS	VSS	BA11
AJ34	VSS	VSS	BA17
AJ38	VSS	VSS	BA21
AJ42	VSS	VSS	BA26
AJ45	VSS	VSS	BA32
AJ48	VSS	VSS	BA48
AK1	VSS	VSS	BA51
AK52	VSS	VSS	BB53
AL10	VSS	VSS	BC5
AL13	VSS	VSS	BC13
AL17	VSS	VSS	BC57
AL21	VSS	VSS	BD8
AL25	VSS	VSS	BD12
AL28	VSS	VSS	BD16
AL33	VSS	VSS	BD19
AL36	VSS	VSS	BD23
AL40	VSS	VSS	BD27
AL43	VSS	VSS	BD32
AL47	VSS	VSS	BD36
AL61	VSS	VSS	BD40
AM4	VSS	VSS	BD44
AM13	VSS	VSS	BD48
AM20	VSS	VSS	BD52
AM22	VSS	VSS	BD56
AM26	VSS	VSS	BE5
AM30	VSS	VSS	BG9

SYNC MASTER=J30_MLB SYNC DATE=07/14/2013

PAGE TITLE
CPU GROUNDS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 14 OF 132
SHEET 14 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

All INTEL recommendations from Intel doc #458544 Chief River Platform Power Design Guide v0p9

CPU VCORE DECOUPLING

Intel recommendation (Table 7-2): Option 2: 35x 2.2uF, 12x 22uF, 4x 470uF, or Option 3: 35x 2.2uF, 6x 22uF, 6x 330 uF

43 13 10 8 =PPVCORE_S0_CPU

CRITICAL C1600 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1604 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1606 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1607 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1608 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1609 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1610 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1612 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1613 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1615 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1617 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1623 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1624 2.2UF 20% 6.3V CERM 402-2

CRITICAL C1625 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1627 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1628 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1631 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1632 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1635 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1637 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1638 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1639 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1640 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1641 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1642 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1643 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1644 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1645 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1647 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1648 2.2UF 20% 6.3V CERM 402-2

CRITICAL C1650 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1651 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1652 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1653 2.2UF 20% 6.3V CERM 402-2
CRITICAL C1654 2.2UF 20% 6.3V CERM 402-2

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

CRITICAL C1646 20UF 20% 2V X6T-CERM 0402
CRITICAL C168F 20UF 20% 2V X6T-CERM 0402
NO STUFF C16A0 20UF 20% 2V X6T-CERM 0402

CRITICAL C1655 20UF 20% 2V X6T-CERM 0402
NO STUFF C1656 20UF 20% 2V X6T-CERM 0402
CRITICAL C1657 20UF 20% 2V X6T-CERM 0402
CRITICAL C1658 20UF 20% 2V X6T-CERM 0402
NO STUFF C1659 20UF 20% 2V X6T-CERM 0402
NO STUFF C1660 20UF 20% 2V X6T-CERM 0402
CRITICAL C1661 20UF 20% 2V X6T-CERM 0402
NO STUFF C1662 20UF 20% 2V X6T-CERM 0402
NO STUFF C1663 20UF 20% 2V X6T-CERM 0402
NO STUFF C1664 20UF 20% 2V X6T-CERM 0402
NO STUFF C1665 20UF 20% 2V X6T-CERM 0402
NO STUFF C1666 20UF 20% 2V X6T-CERM 0402
CRITICAL C166A 20UF 20% 2V X6T-CERM 0402
NO STUFF C166B 20UF 20% 2V X6T-CERM 0402
CRITICAL C166C 20UF 20% 2V X6T-CERM 0402
NO STUFF C166D 20UF 20% 2V X6T-CERM 0402
NO STUFF C166E 20UF 20% 2V X6T-CERM 0402
CRITICAL C166F 20UF 20% 2V X6T-CERM 0402
CRITICAL C165A 20UF 20% 2V X6T-CERM 0402
NO STUFF C165B 20UF 20% 2V X6T-CERM 0402
NO STUFF C167 20UF 20% 2V X6T-CERM 0402
CRITICAL C1674 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

CRITICAL C16A1 20UF 20% 2V X6T-CERM 0402
NO STUFF C16A2 20UF 20% 2V X6T-CERM 0402
CRITICAL C16A3 20UF 20% 2V X6T-CERM 0402

NO STUFF C1675 20UF 20% 2V X6T-CERM 0402
NO STUFF C1668 20UF 20% 2V X6T-CERM 0402
CRITICAL C1669 20UF 20% 2V X6T-CERM 0402
NO STUFF C1670 20UF 20% 2V X6T-CERM 0402
CRITICAL C1671 20UF 20% 2V X6T-CERM 0402
NO STUFF C1672 20UF 20% 2V X6T-CERM 0402
NO STUFF C1673 20UF 20% 2V X6T-CERM 0402
NO STUFF C1649 20UF 20% 2V X6T-CERM 0402
NO STUFF C164A 20UF 20% 2V X6T-CERM 0402
NO STUFF C1676 20UF 20% 2V X6T-CERM 0402
CRITICAL C1677 20UF 20% 2V X6T-CERM 0402
NO STUFF C1678 20UF 20% 2V X6T-CERM 0402
CRITICAL C1679 20UF 20% 2V X6T-CERM 0402
CRITICAL C165C 20UF 20% 2V X6T-CERM 0402
NO STUFF C165D 20UF 20% 2V X6T-CERM 0402
CRITICAL C165E 20UF 20% 2V X6T-CERM 0402
NO STUFF C165F 20UF 20% 2V X6T-CERM 0402
NO STUFF C164E 20UF 20% 2V X6T-CERM 0402
NO STUFF C164B 20UF 20% 2V X6T-CERM 0402
NO STUFF C164C 20UF 20% 2V X6T-CERM 0402
CRITICAL C164D 20UF 20% 2V X6T-CERM 0402
CRITICAL C164F 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1681 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1682 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1683 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C168D 270UF 20% 2V TANT CASE-B2-SM
C168E 270UF 20% 2V TANT CASE-B2-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Table 7-7): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

13 11 10 8 =PP1V05_S0_CPU_VCCIO

C1684 1UF 10% 10V X5R-CERM 0402
C1685 1UF 10% 10V X5R-CERM 0402
C1686 1UF 10% 10V X5R-CERM 0402
C1687 1UF 10% 10V X5R-CERM 0402
C1688 1UF 10% 10V X5R-CERM 0402
C1689 1UF 10% 10V X5R-CERM 0402
C1690 1UF 10% 10V X5R-CERM 0402
C1691 1UF 10% 10V X5R-CERM 0402
C1692 1UF 10% 10V X5R-CERM 0402
C1693 1UF 10% 10V X5R-CERM 0402
C1694 1UF 10% 10V X5R-CERM 0402
C1695 1UF 10% 10V X5R-CERM 0402
C1696 1UF 10% 10V X5R-CERM 0402

C1697 1UF 10% 10V X5R-CERM 0402
C1698 1UF 10% 10V X5R-CERM 0402
C1699 1UF 10% 10V X5R-CERM 0402
C169A 1UF 10% 10V X5R-CERM 0402
C169B 1UF 10% 10V X5R-CERM 0402
C169C 1UF 10% 10V X5R-CERM 0402
C169D 1UF 10% 10V X5R-CERM 0402
C169E 1UF 10% 10V X5R-CERM 0402
C169F 1UF 10% 10V X5R-CERM 0402
C161A 1UF 10% 10V X5R-CERM 0402
C161B 1UF 10% 10V X5R-CERM 0402
C161C 1UF 10% 10V X5R-CERM 0402
C161D 1UF 10% 10V X5R-CERM 0402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E 10UF 20% 6.3V CERM-X5R 0402-1
C161F 10UF 20% 6.3V CERM-X5R 0402-1
C162A 10UF 20% 6.3V CERM-X5R 0402-1
C162B 10UF 20% 6.3V CERM-X5R 0402-1
C162C 10UF 20% 6.3V CERM-X5R 0402-1
C162D 10UF 20% 6.3V CERM-X5R 0402-1
C162E 10UF 20% 6.3V CERM-X5R 0402-1
C167A 10UF 20% 6.3V CERM-X5R 0402-1
C167B 10UF 20% 6.3V CERM-X5R 0402-1
C167C 10UF 20% 6.3V CERM-X5R 0402-1

C167D 270UF 20% 2V TANT CASE-B2-SM
C167E 270UF 20% 2V TANT CASE-B2-SM
C168A 270UF 20% 2V TANT CASE-B2-SM
C168B 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603 =PP1V05_S0_CPU_VCCPQE 8 13

C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (table 7-5): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):

8 =PP1V8_S0_CPU_VCCPLL

R1600 0 5% 1/16W MF-LF 402

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402

PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

=PP1V8_S0_CPU_VCCPLL_R 8 13

PLACE_NEAR=U1000.AK61:5mm

C160Z 270UF 20% 2V TANT CASE-B2-SM

PLACE_NEAR=U1000.AK61:5mm

C168C 270UF 20% 2V TANT CASE-B2-SM

CPU VCCPLL Low pass filter

SYNC MASTER=MASTER	SYNC DATE=MASTER
PAGE TITLE	CPU DECOUPLING-I
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 16 OF 132
	SHEET 15 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

VAXG DECOUPLING

Intel recommendation (Table 7-4) for GT2 3.9mOhm LL: 11x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

43 13 10 8 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R-CERM 0402
CRITICAL C1701 1UF 10% 10V X5R-CERM 0402
CRITICAL C1702 1UF 10% 10V X5R-CERM 0402
CRITICAL C1703 1UF 10% 10V X5R-CERM 0402
CRITICAL C1704 1UF 10% 10V X5R-CERM 0402
CRITICAL C1705 1UF 10% 10V X5R-CERM 0402
CRITICAL C1706 1UF 10% 10V X5R-CERM 0402
CRITICAL C1707 1UF 10% 10V X5R-CERM 0402
CRITICAL C1708 1UF 10% 10V X5R-CERM 0402
CRITICAL C1709 1UF 10% 10V X5R-CERM 0402
CRITICAL C1710 1UF 10% 10V X5R-CERM 0402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL C1717 20UF 20% 2V X6T-CERM 0402
CRITICAL C1718 20UF 20% 2V X6T-CERM 0402
CRITICAL C1719 20UF 20% 2V X6T-CERM 0402
CRITICAL C1720 20UF 20% 2V X6T-CERM 0402
CRITICAL C1721 20UF 20% 2V X6T-CERM 0402
CRITICAL C1722 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1725 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1726 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1727 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1728 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C1729 20UF 20% 2V X6T-CERM 0402
CRITICAL NO STUFF C172A 20UF 20% 2V X6T-CERM 0402

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1724 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Table 7-11): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

27 13 11 8 =PP1V5R1V35_S3_CPU_VCCDDR

Place on bottom side of U1000

C1738 1UF 10% 10V X5R-CERM 0402
C1739 1UF 10% 10V X5R-CERM 0402
C1740 1UF 10% 10V X5R-CERM 0402
C1741 1UF 10% 10V X5R-CERM 0402
C1742 1UF 10% 10V X5R-CERM 0402
C1743 1UF 10% 10V X5R-CERM 0402
C1744 1UF 10% 10V X5R-CERM 0402
C1745 1UF 10% 10V X5R-CERM 0402
C1746 1UF 10% 10V X5R-CERM 0402
C1747 1UF 10% 10V X5R-CERM 0402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V CERM-X5R 0402-1
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V CERM-X5R 0402-1
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 270UF 20% 2V TANT CASE-B2-SM
C1770 270UF 20% 2V TANT CASE-B2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 8 13

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Table 7-9): 5x 1uf, 5x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

13 8 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R-CERM 0402
C1759 1UF 10% 10V X5R-CERM 0402
C1760 1UF 10% 10V X5R-CERM 0402
C1761 1UF 10% 10V X5R-CERM 0402
C1762 1UF 10% 10V X5R-CERM 0402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 270UF 20% 2V TANT CASE-B2-SM
C1769 270UF 20% 2V TANT CASE-B2-SM

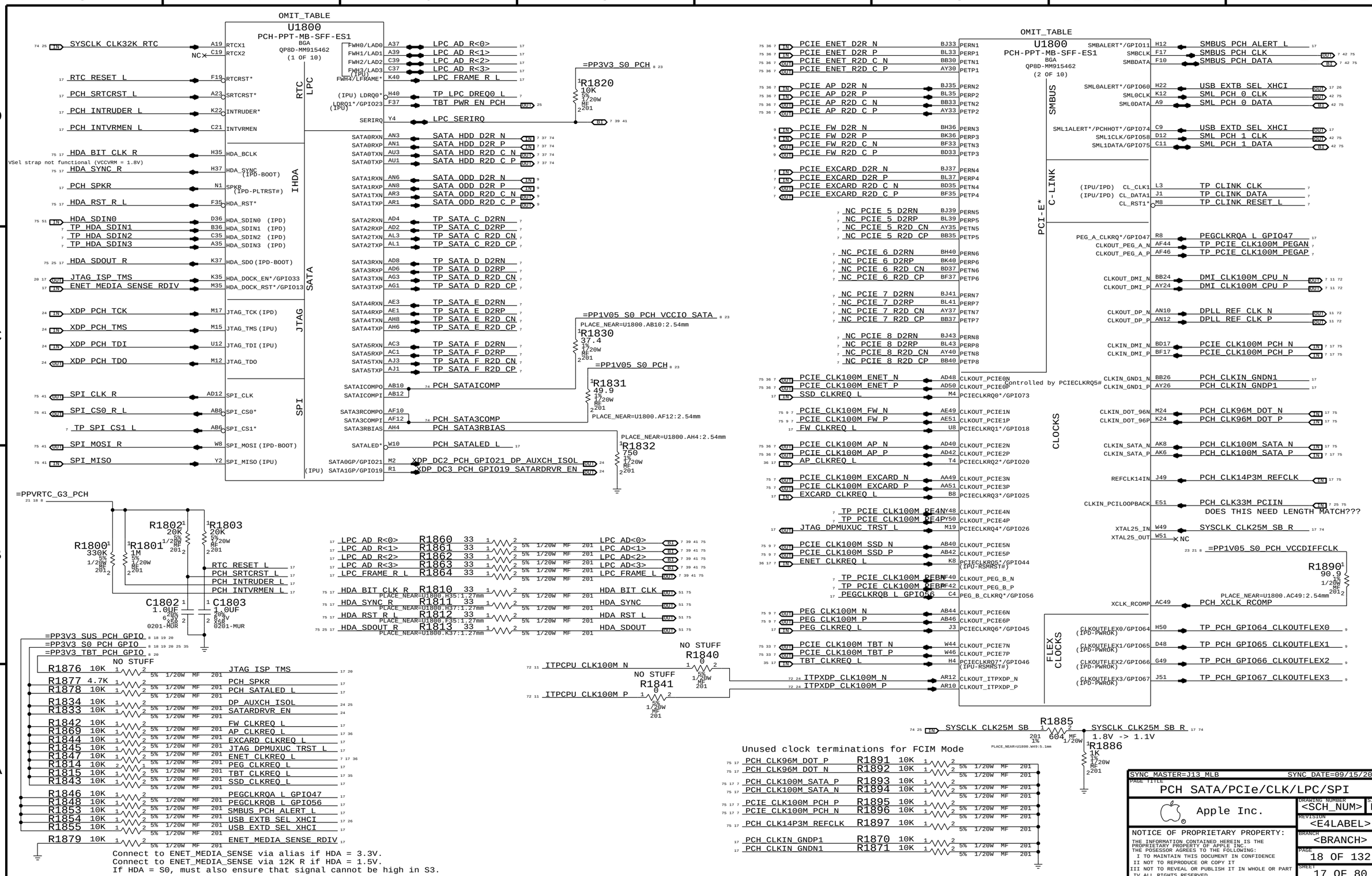
SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 17 OF 132
SHEET 16 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



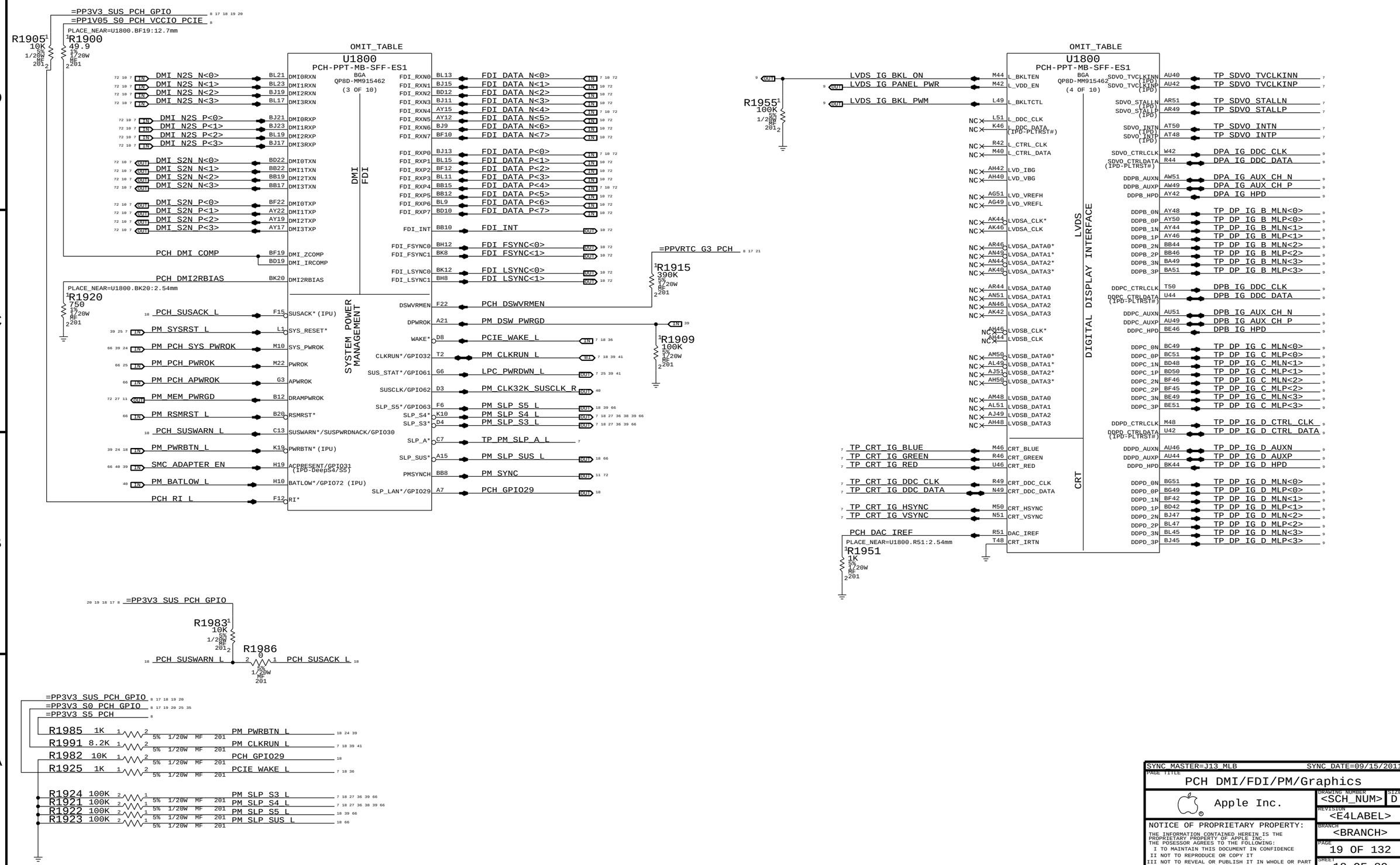
SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE
PCH SATA/PCIe/CLK/LPC/SPI

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 18 OF 132
SHEET 17 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE
PCH DMI/FDI/PM/Graphics

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

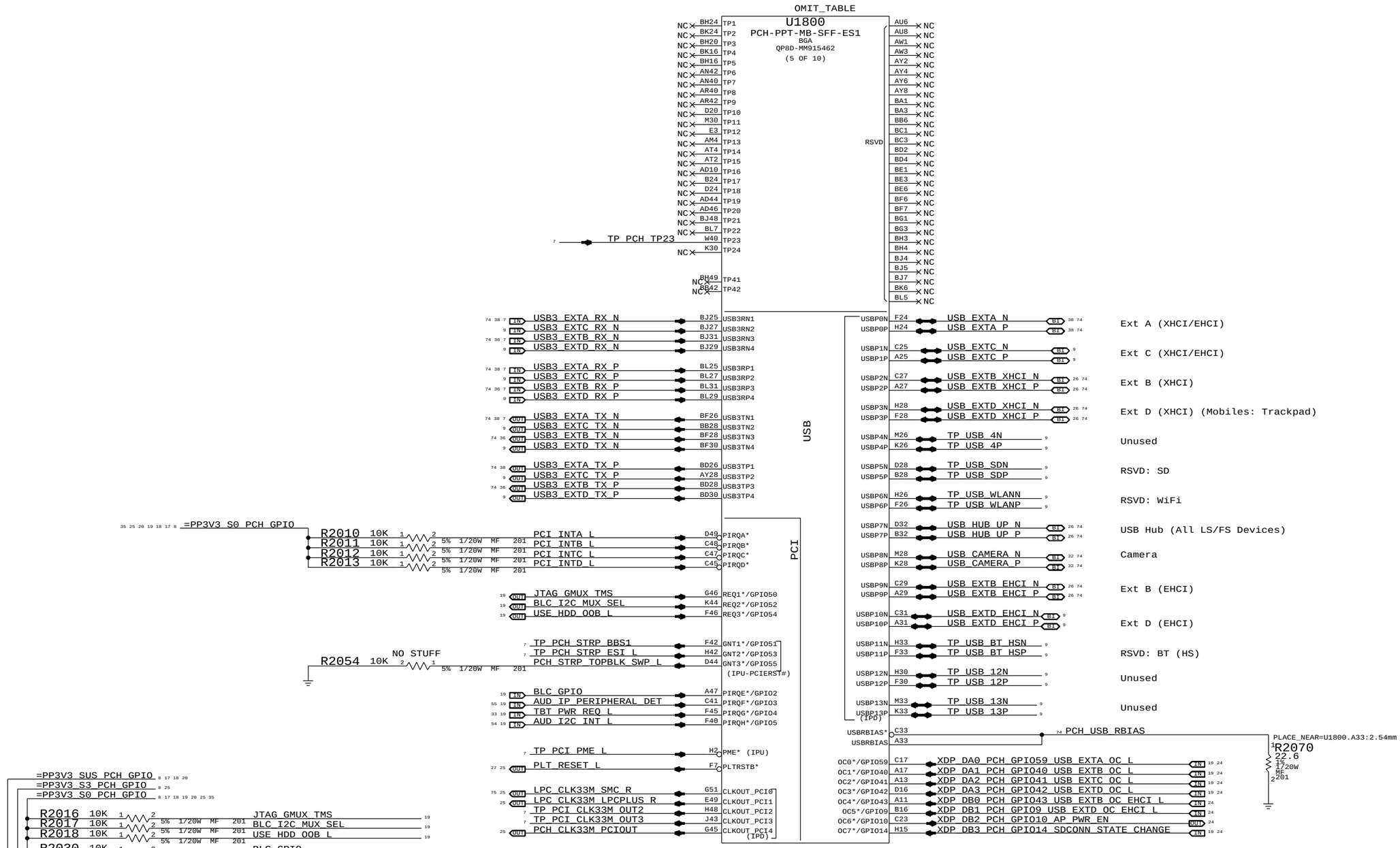
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 19 OF 132

SHEET 18 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE

PCH PCI/USB/TP/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 20 OF 132

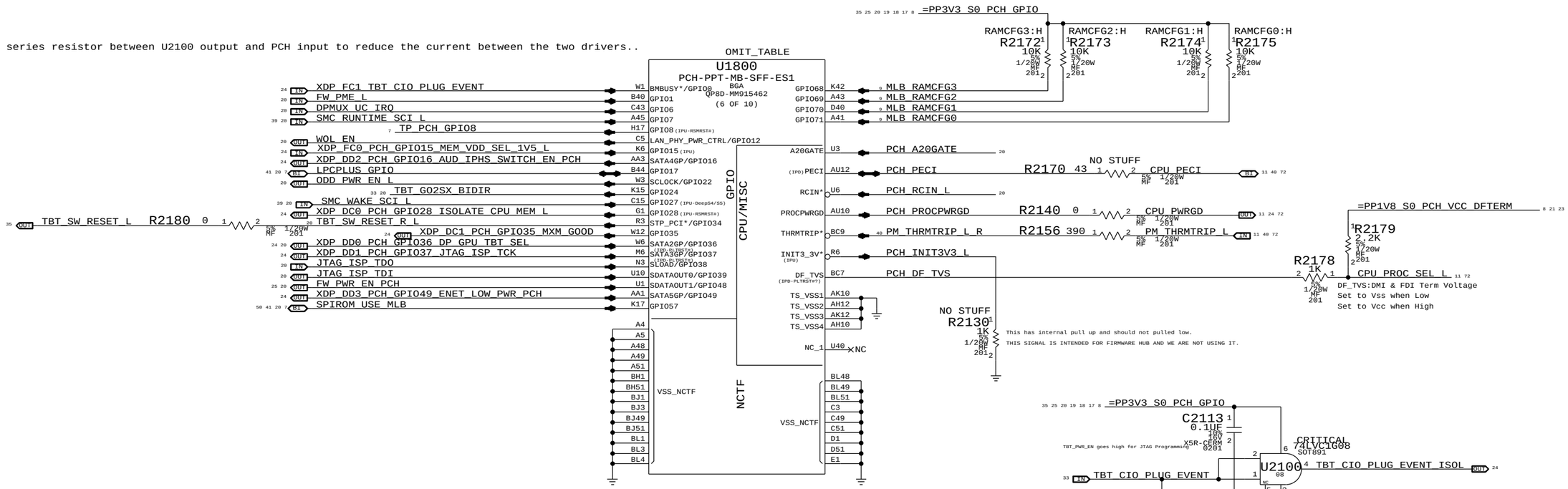
SHEET 19 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

R2574 is 1K series resistor between U2100 output and PCH input to reduce the current between the two drivers..



SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE
PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

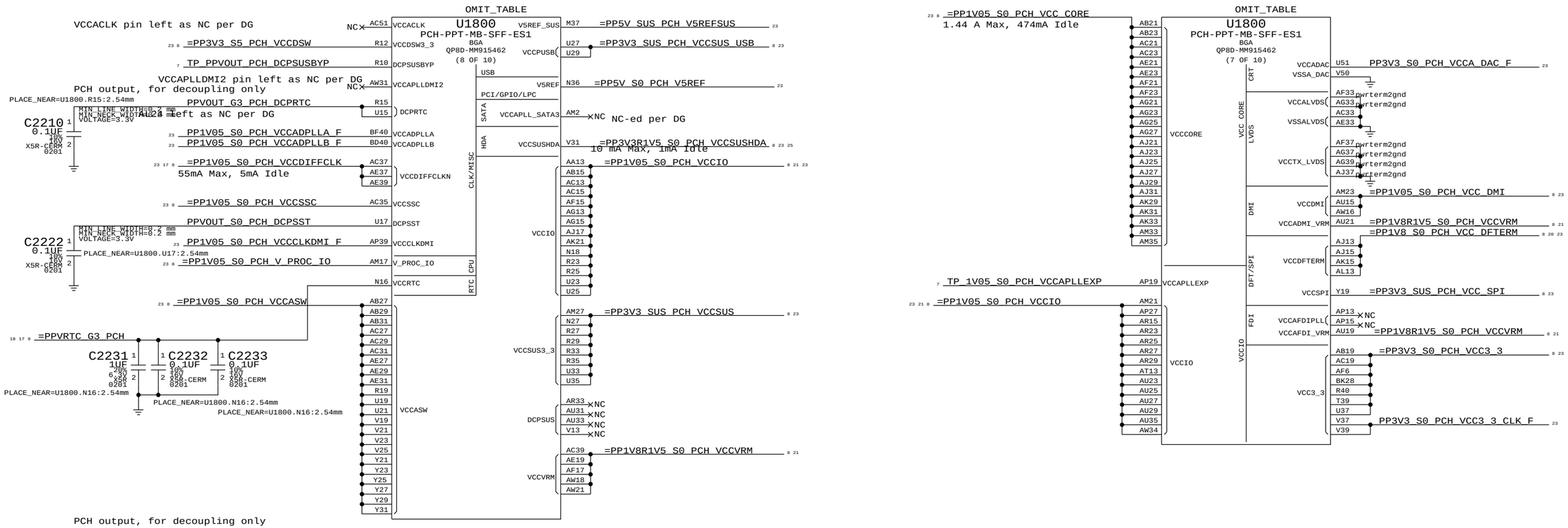
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 21 OF 132

SHEET 20 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE

PCH POWER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 22 OF 132

SHEET 21 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(9 OF 10)

AA7		AP2
AA9		AP4
AA11		AP7
AA39		AP9
AA41		AP11
AA43		AP17
AA45		AP21
AB2		AP23
AB4		AP25
AB17		AP29
AB25		AP31
AB33		AP33
AB35		AP35
AB37		AP37
AB48		AP41
AB50		AP43
AC7		AP45
AC9		AP48
AC11		AP50
AC17		AR6
AC25		AR8
AC41		AR17
AC43		AR19
AC45		AR21
AE7		AR31
AE9		AR35
AE11		AR37
AE13		AT7
AE15		AT9
AE17		AT11
AE25		AT39
AE35		AT41
AE41		AT43
AE43		AT45
AE45		AU17
AF2		AU37
AF4		AV2
AF8		AV4
AF19		AV48
AF25		AV50
AF27		AW7
AF29	VSS	AW9
AF31		AW11
AF35		AW13
AF48		AW23
AF50		AW25
AG7		AW27
AG9		AW29
AG11		AW36
AG17		AW39
AG19		AW41
AG29		AW43
AG31		AW45
AG35		AY10
AG41		B6
AG43		B10
AG45		B14
AH2		B18
AJ7		B22
AJ9		B26
AJ11		B30
AJ19		B34
AJ33		B38
AJ35		B42
AJ39		B46
AJ41		BA7
AJ43		BA9
AJ45		BA11
AK2		BA13
AK4		BA16
AK17		BA18
AK19		BA21
AK23		BA23
AK25		BA25
AK27		BA27
AK35		BA29
AK37		BA31
AK48		BA34
AK50		BA36
AL7		BA39
AL9		BA41
AL11		BA43
AL39		BA45
AL41		BB2
AL43		BB4
AL45		BB48
AM15		BB50
AM19		BC11
AM25		BC13
AM29		BC16
AM31		BC18
AM37		BC21

OMIT_TABLE

U1800
PCH-PPT-MB-SFF-ES1
BGA
QP8D-MM915462
(10 OF 10)

BC23		G39
BC25		G41
BC27		G43
BC29		J7
BC31		J9
BC34		J11
BC36		J13
BC39		J16
BC41		J18
BC43		J21
BC45		J23
BD15		J25
BD24		J27
BE7		J29
BE9		J31
BE11		J34
BE13		J36
BE16		J39
BE18		J41
BE21		J45
BE23		K2
BE25		K4
BE27		K48
BE29		K50
BE31		L7
BE34		L9
BE36		L11
BE39		L13
BE41		L16
BE43		L18
BE45		L21
BF2		L23
BF4		L25
BF15		L27
BF24		L29
BF48		L31
BF50		L34
BH6		L36
BH10		L39
BH14	VSS	L41
BH18		L43
BH22		L45
BH26		N7
BH28		N9
BH30		N11
BH32		N13
BH34		N21
BH38		N23
BH42		N25
BH44		N29
BH46		N31
BH48		N34
BK10		N39
BK14		N41
BK18		N43
BK22		N45
BK26		P2
BK30		P4
BK32		P48
BK34		P50
BK38		R17
BK42		R21
BK46		R31
D6		R37
D10		T7
D14		T9
D18		T11
D22		T13
D26		T41
D30		T43
D34		T45
D38		U31
D42		U49
D46		V2
F2		V4
F4		V7
F48		V9
F50		V11
G7		V15
G9		V17
G11		V27
G13		V29
G16		V33
G18		V35
G21		V41
G23		V43
G25		V45
G27		V48
G29		Y15
G31		Y17
G34		Y33
G36		Y35
		Y37

SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2011

PAGE TITLE
PCH GROUNDS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

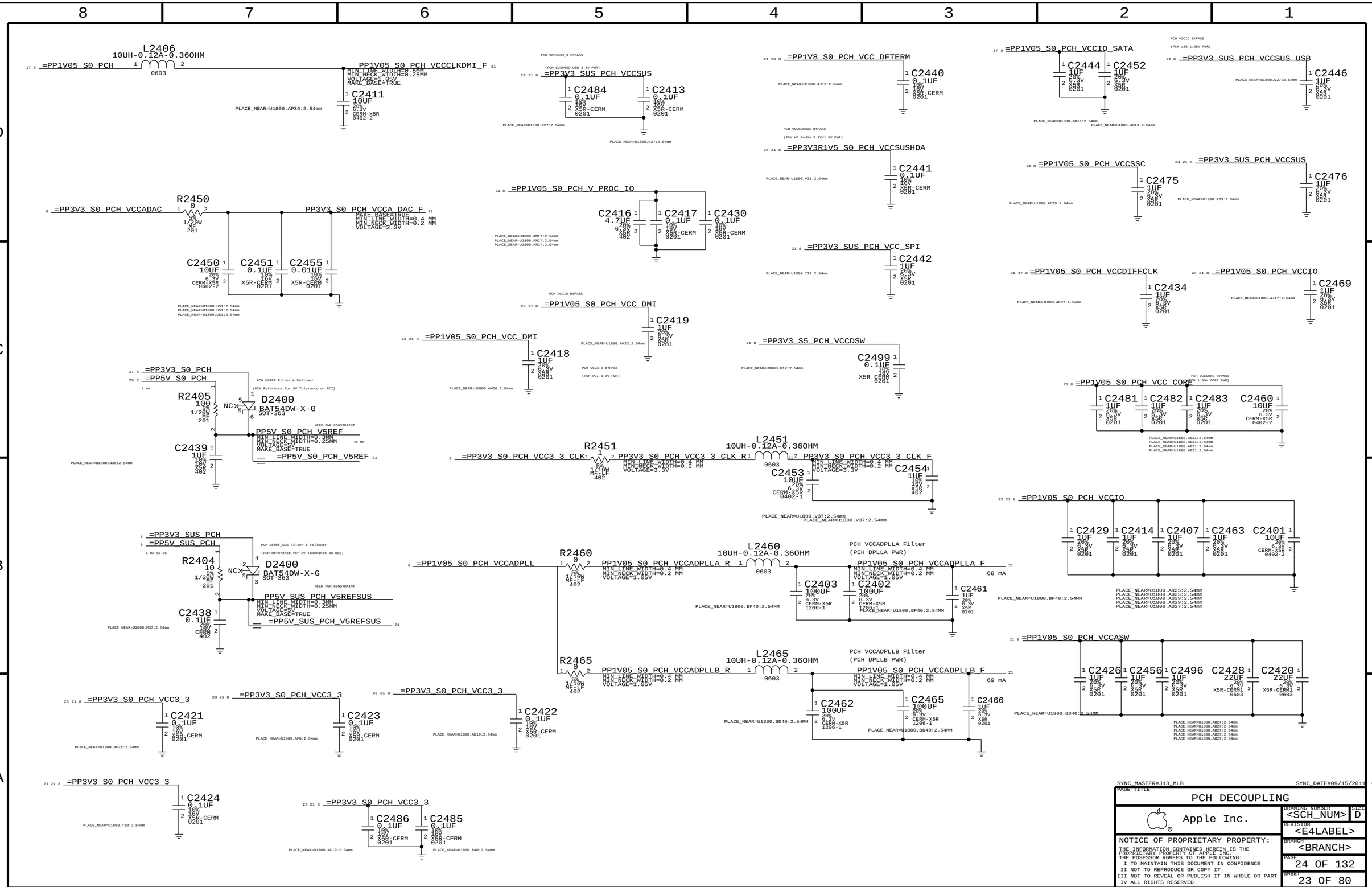
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 23 OF 132

SHEET 22 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J13_MLB SYNC_DATE=09/15/2013

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

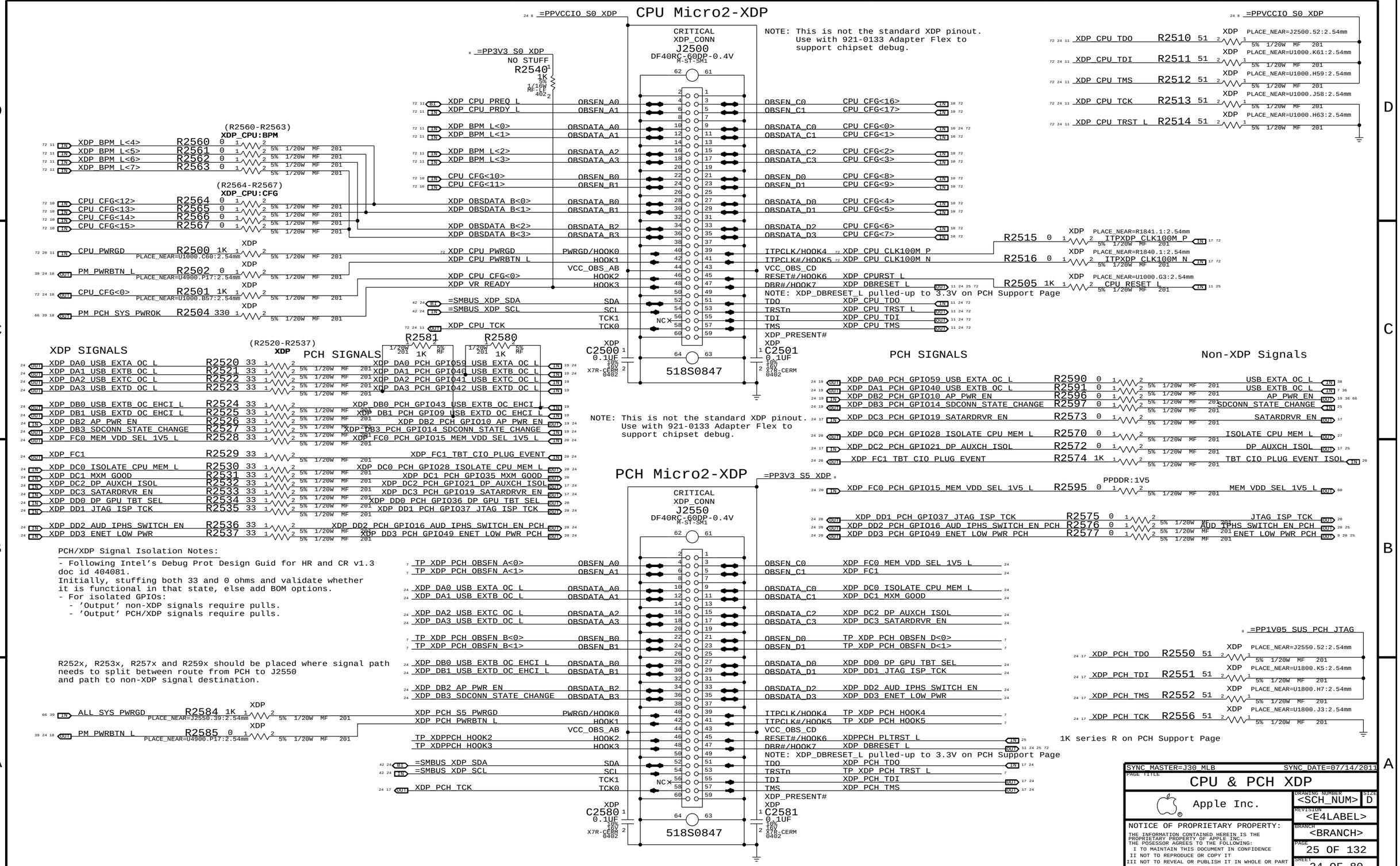
BRANCH <BRANCH>

PAGE 24 OF 132

SHEET 23 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU Micro2-XDP



PCH/XDP Signal Isolation Notes:

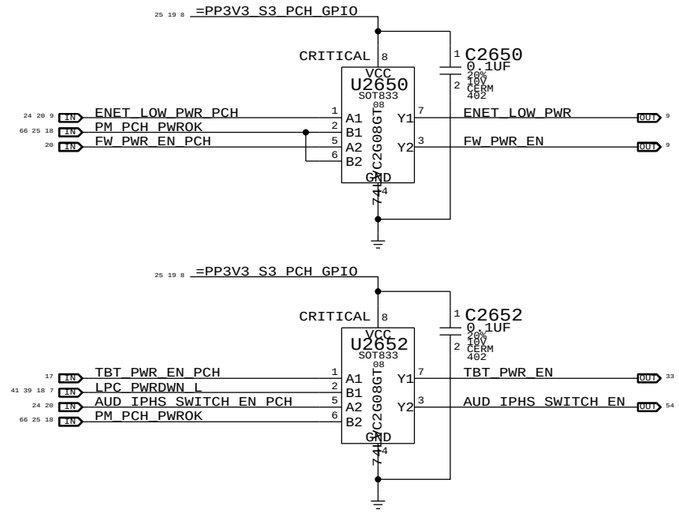
- Following Intel's Debug Prot Design Guid for HR and CR v1.3 doc id 404081.
  Initially, stuffing both 33 and 0 ohms and validate whether it is functional in that state, else add BOM options.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

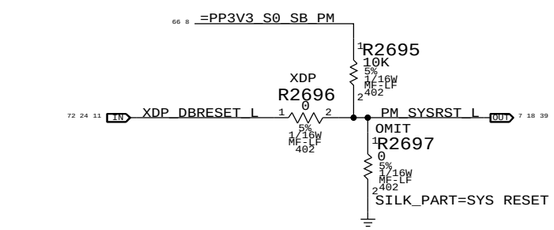
SYNC_MASTER=J30_MLB	SYNC_DATE=07/14/2011
PAGE TITLE	CPU & PCH XDP
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 25 OF 132
	SHEET 24 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

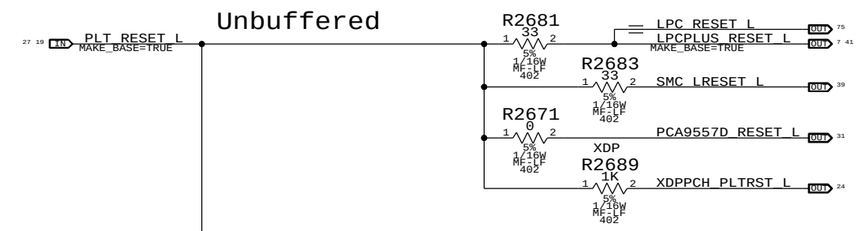
GPIO Glitch Prevention

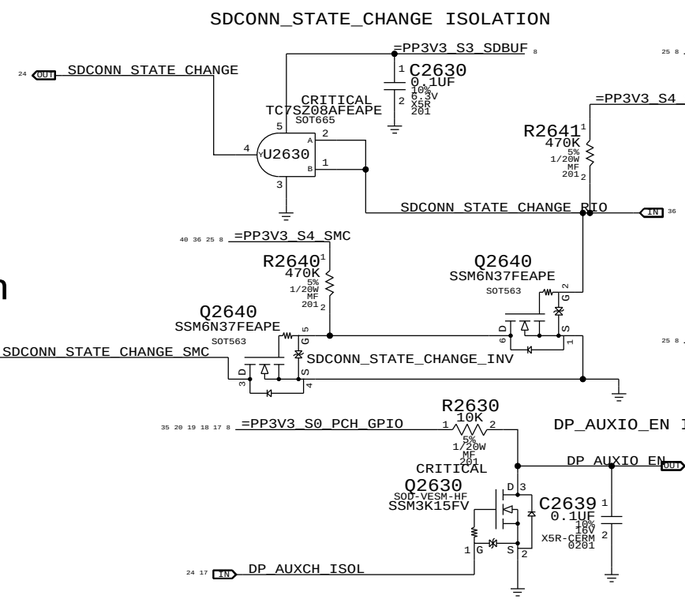


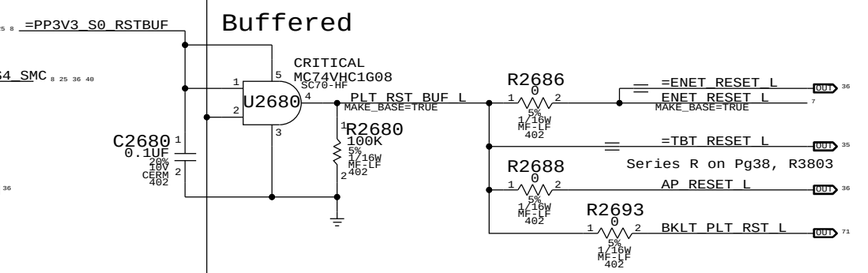
PCH Reset Button



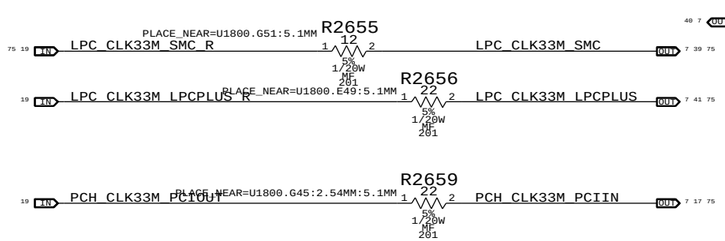
Platform Reset Connections

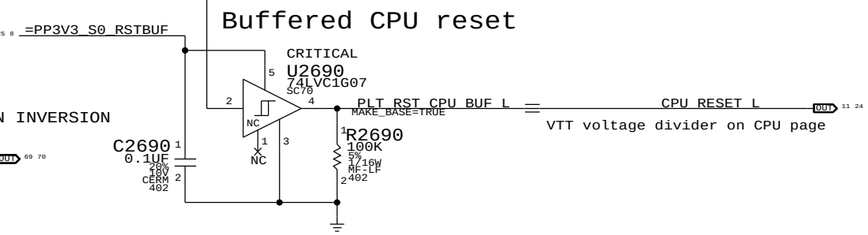






33 MHz Clock Series Termination

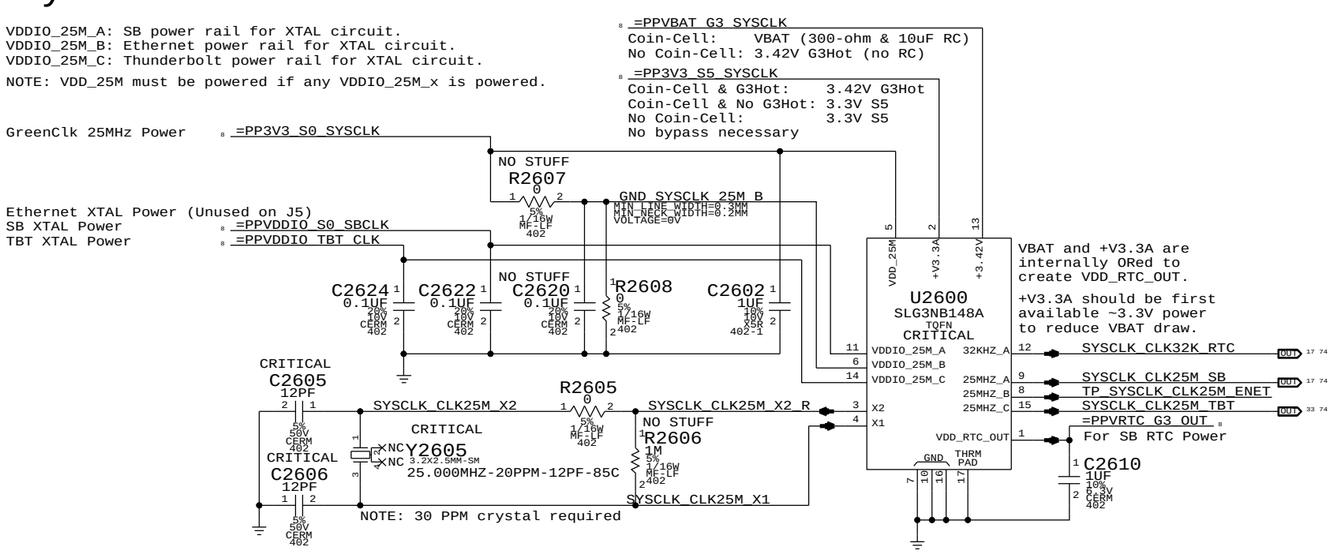




System RTC Power Source & 32kHz / 25MHz Clock Generator

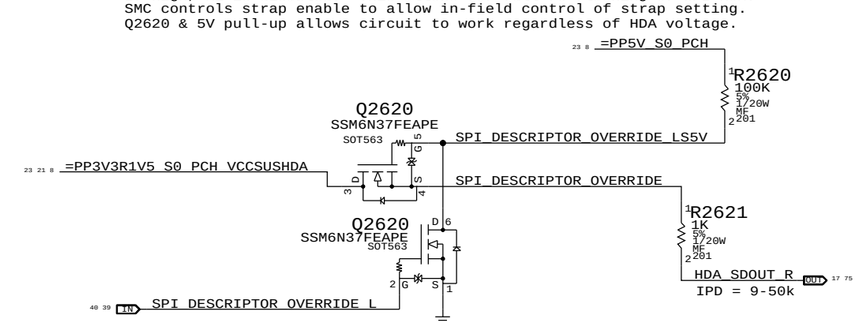
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 26 OF 132
SHEET 25 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

USB MUX FOR LS/FS INTERNAL DEVICES

NON_REM 1 :	NON_REM 0	STRAP PIN CFG
0	0	ALL PORTS ARE REMOVABLE
0	1	PORT 1 IS NON REMOVABLE
1	0	PORT 1&2 ARE NON REMOVABLE
1	1	PORT 1&2&3 ARE NON REMOVABLE

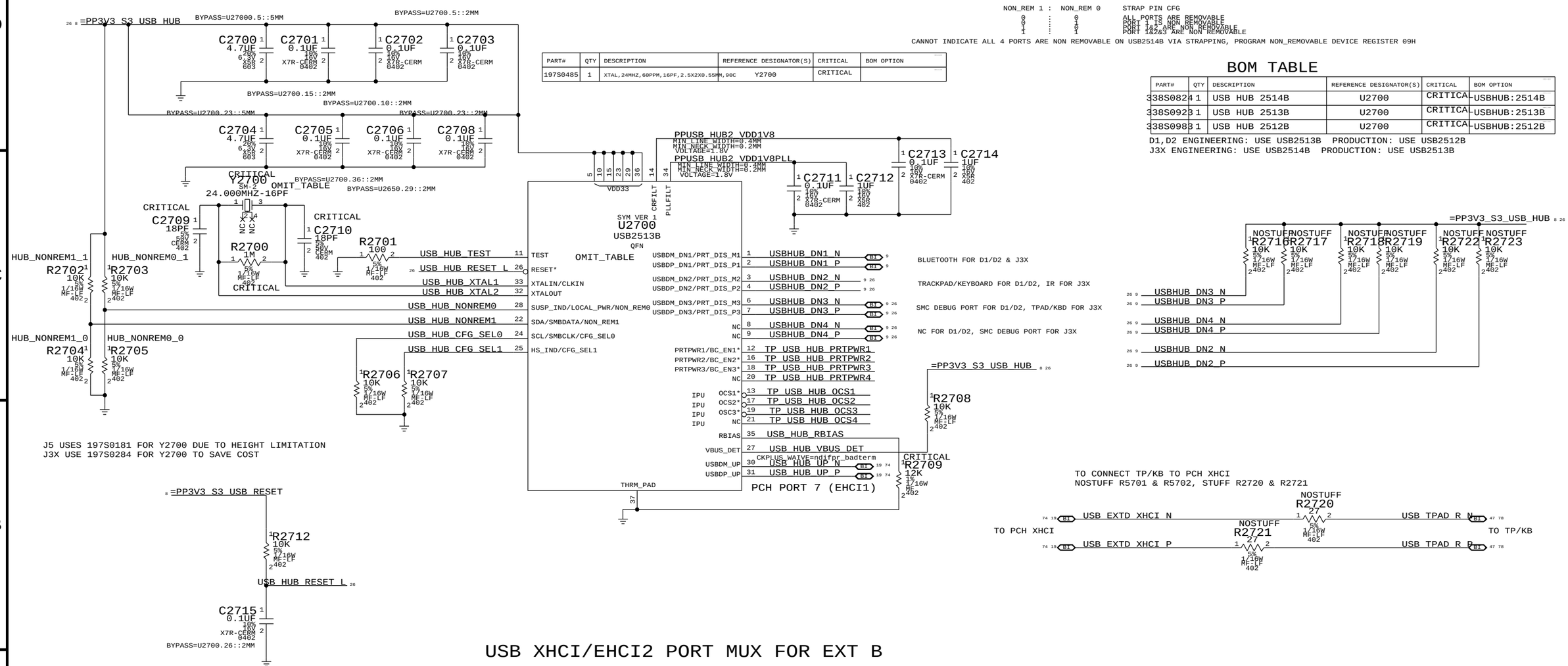
CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STRAPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0485	1	XTAL,24MHZ,60PPM,16PF,2.5X2X0.55MM,90C	Y2700	CRITICAL	

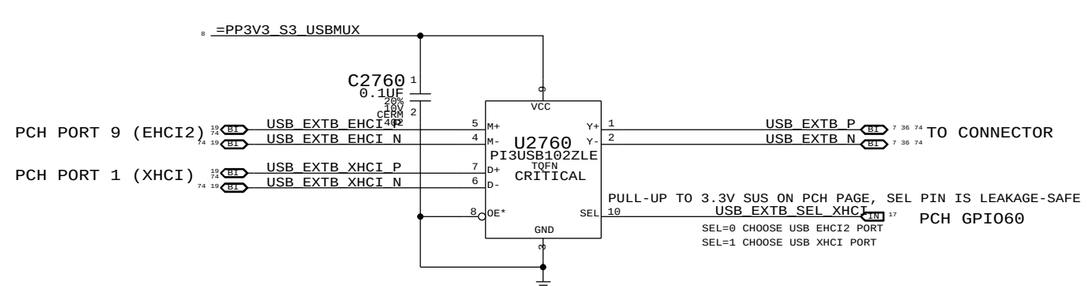
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB:2514B
338S0923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB:2513B
338S0983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB:2512B

D1,D2 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



USB XHCI/EHCI2 PORT MUX FOR EXT B



SYNC_MASTER=J5_AMD SYNC_DATE=08/17/2011

PAGE TITLE
USB HUB & MUX

Apple Inc.

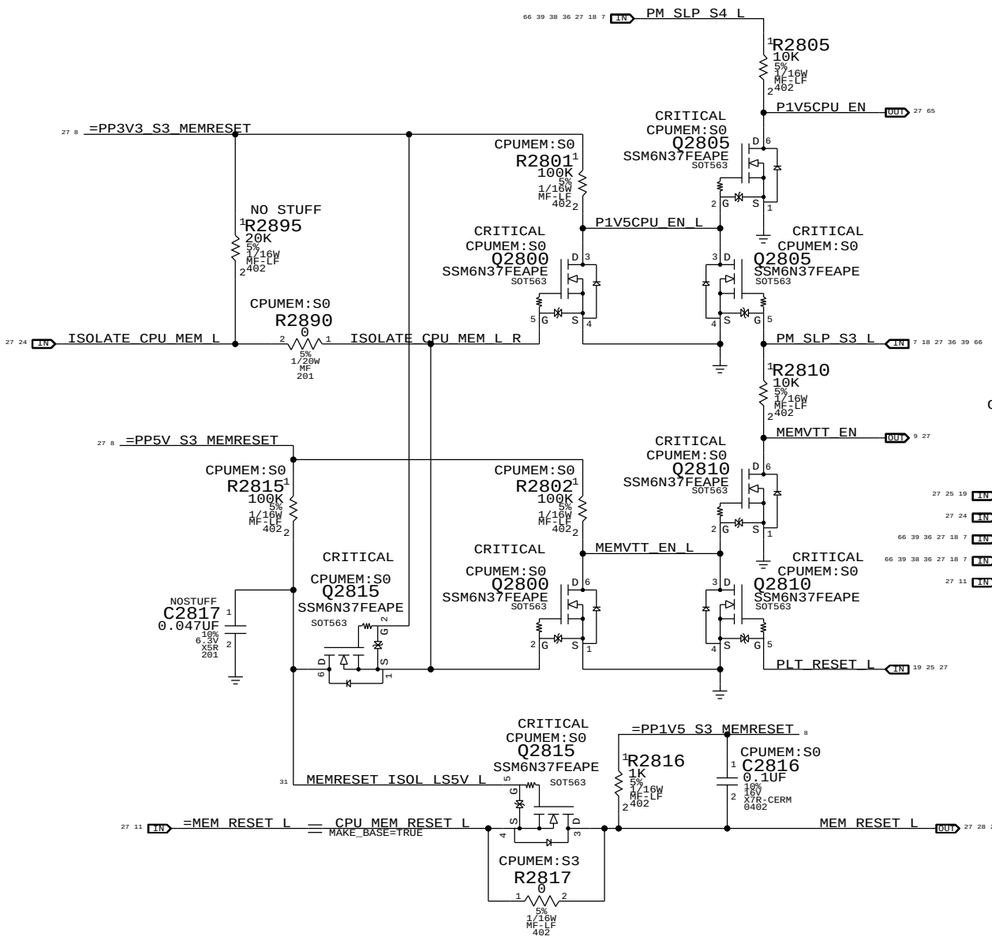
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 27 OF 132
SHEET 26 OF 80

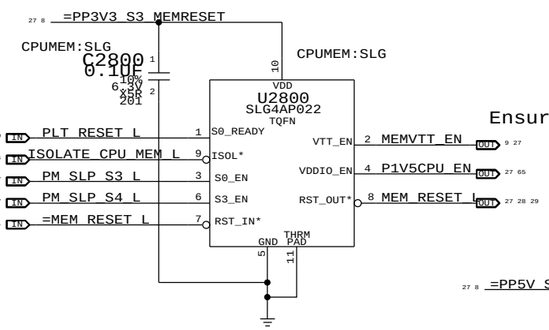
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

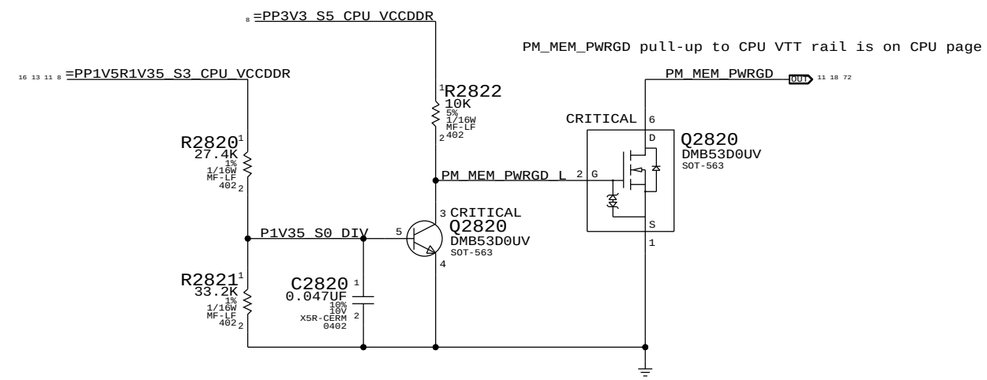
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



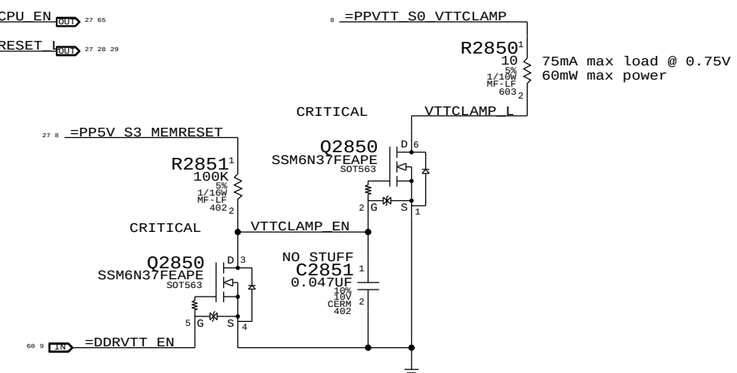


1V35 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

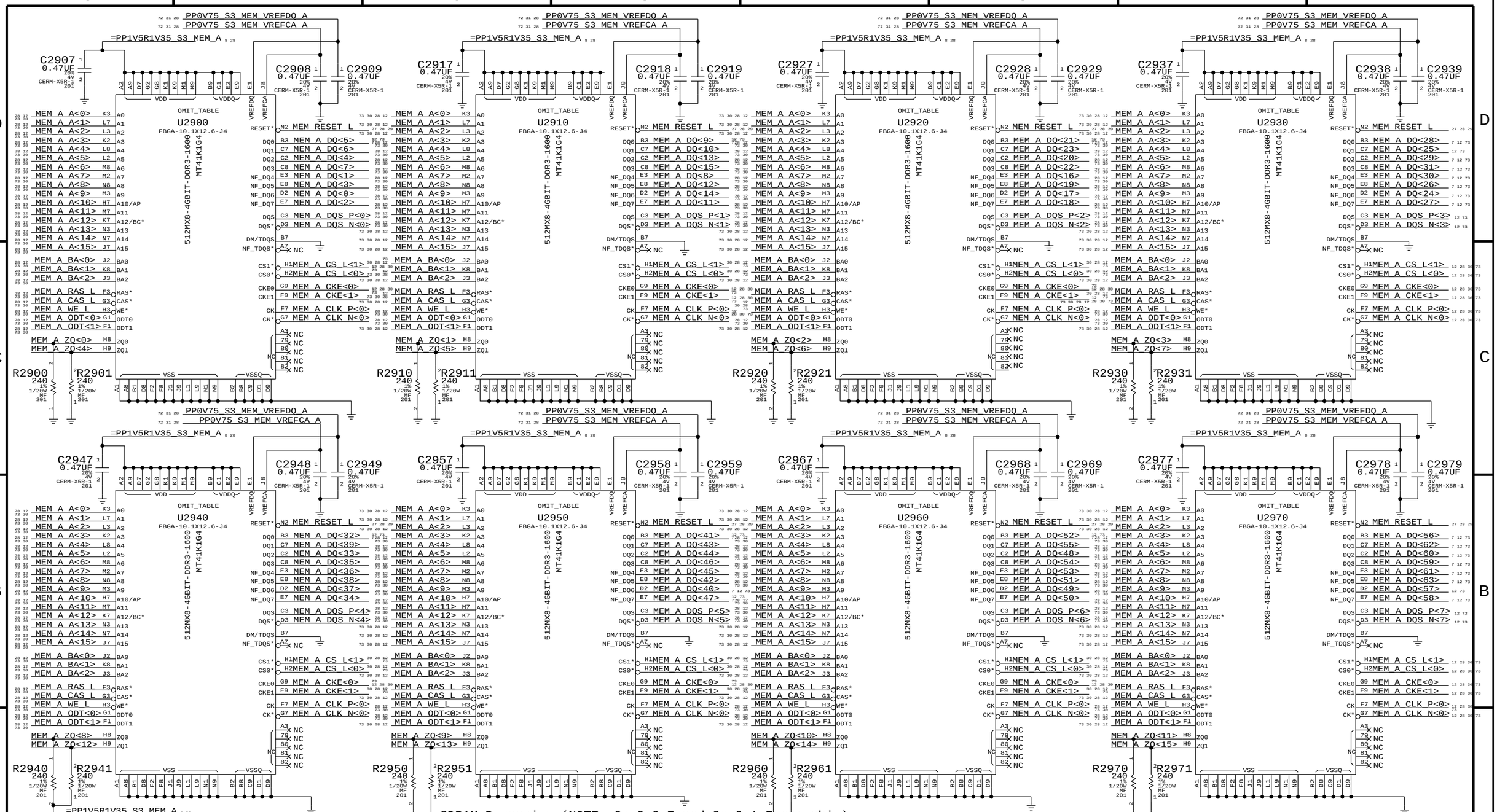
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 28 OF 132

SHEET: 27 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J5_MLB SYNC_DATE=07/14/2011

PAGE TITLE

DDR3 SDRAM Bank A (Rank 0)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

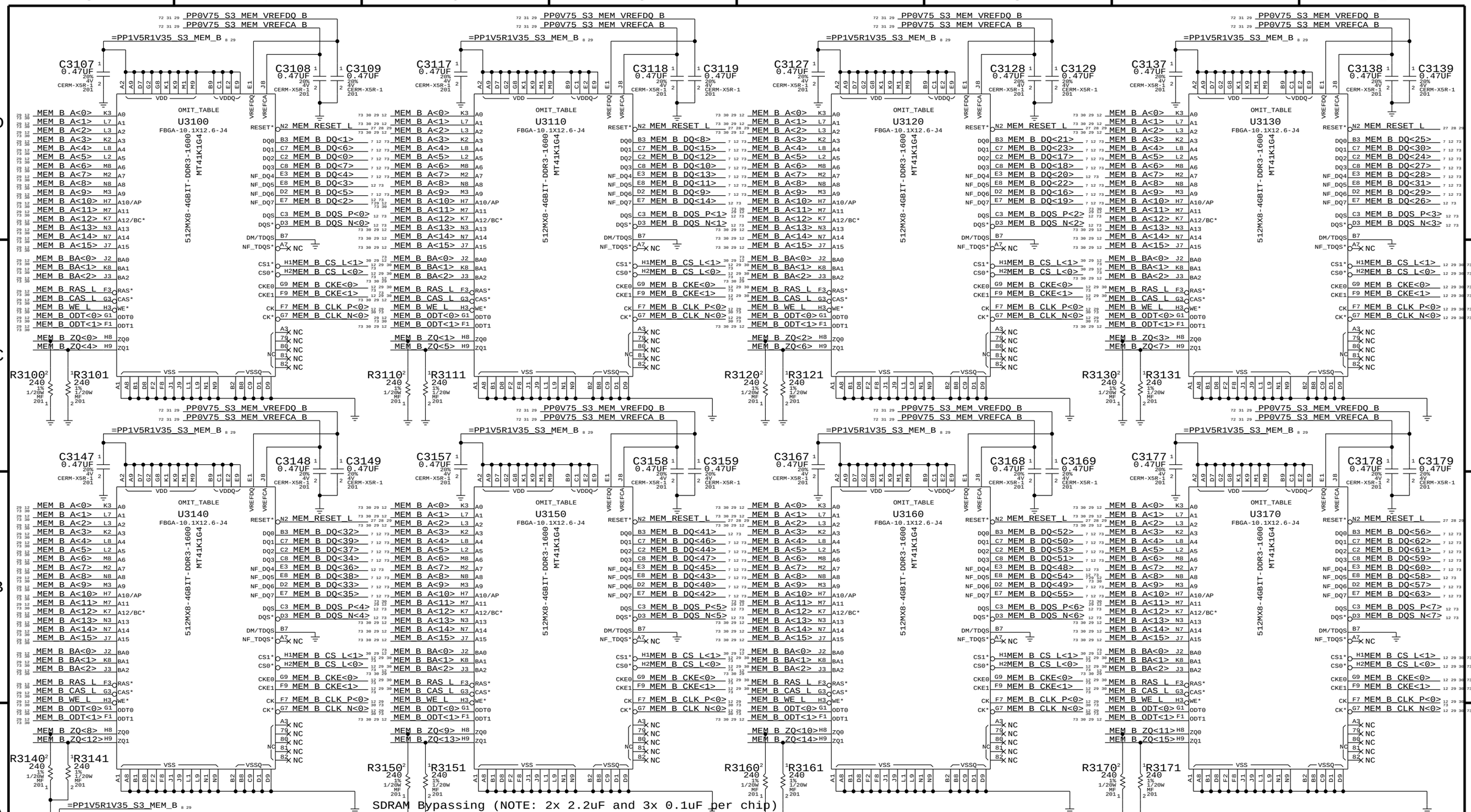
BRANCH <BRANCH>

PAGE 29 OF 132

SHEET 28 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC MASTER=J5_MLB SYNC DATE=07/14/2011

PAGE TITLE

DDR3 SDRAM Bank B (Rank 0)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

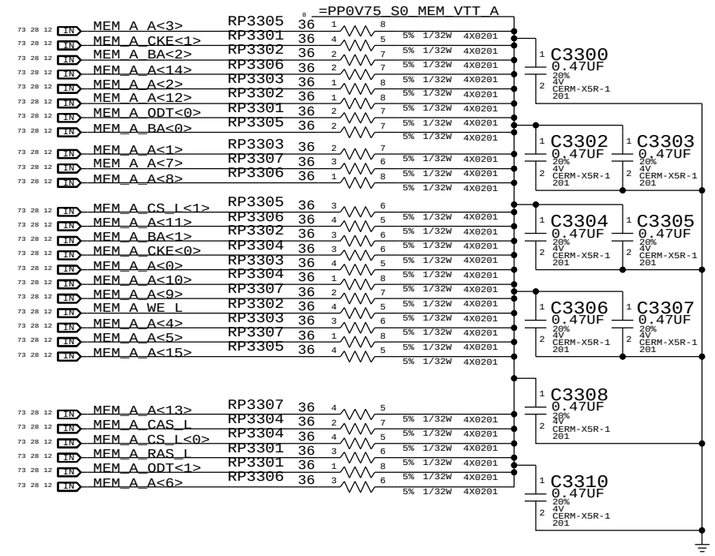
BRANCH <BRANCH>

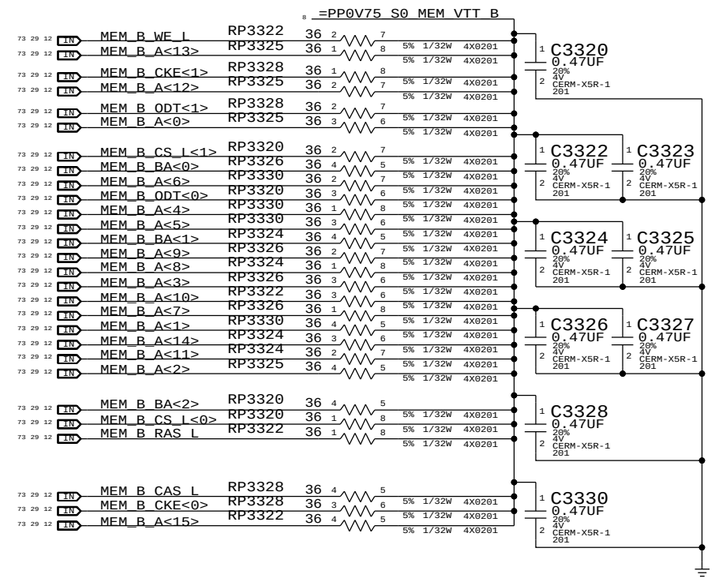
PAGE 31 OF 132

SHEET 29 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

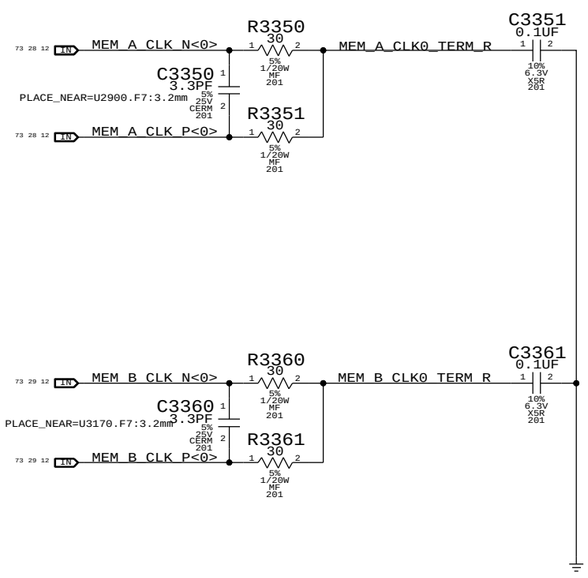
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=MASTER SYNC_DATE=MASTER

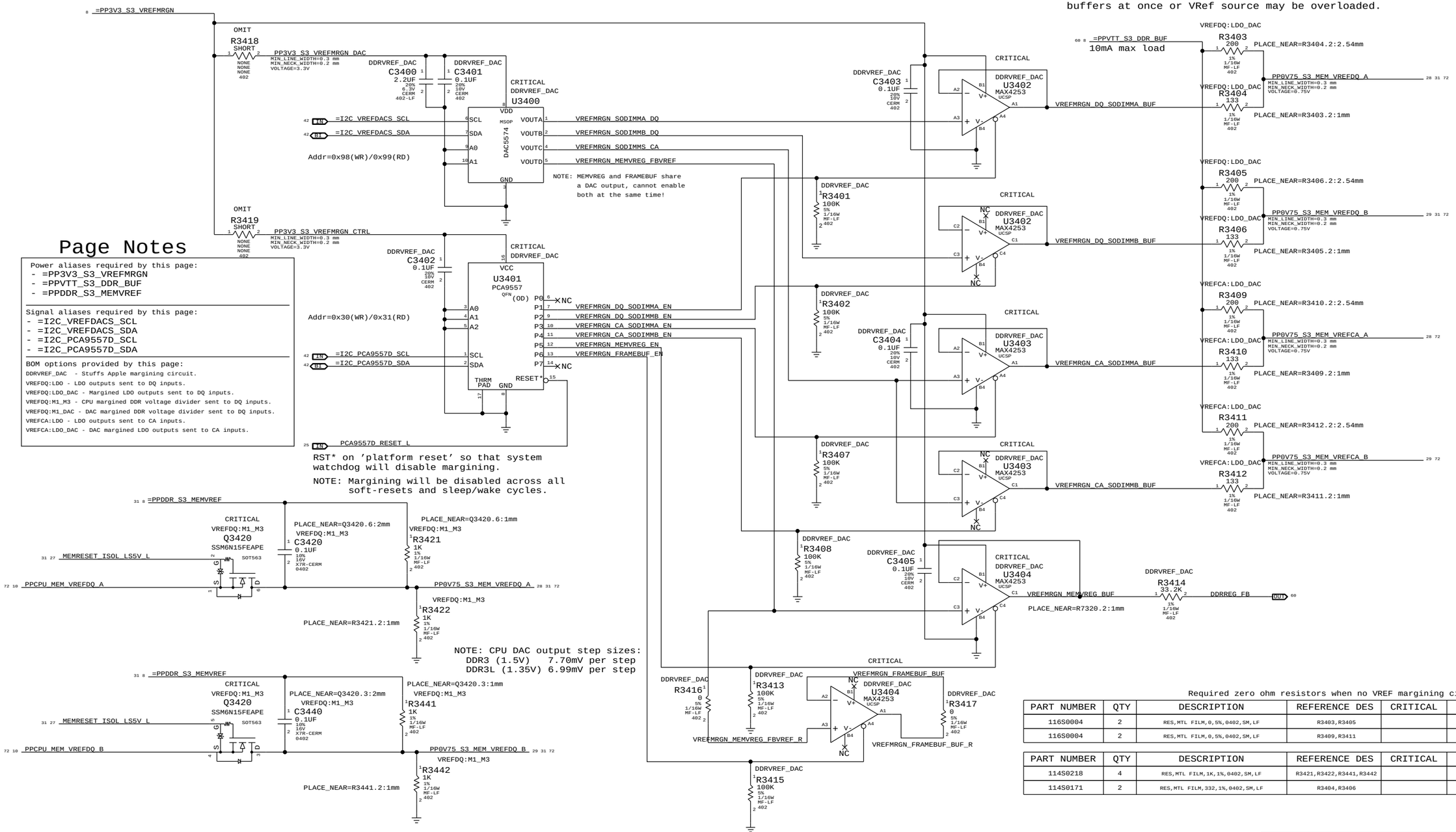
PAGE TITLE
DDR3 Termination

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 33 OF 132
SHEET 30 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J5_MLB SYNC DATE=07/29/2011

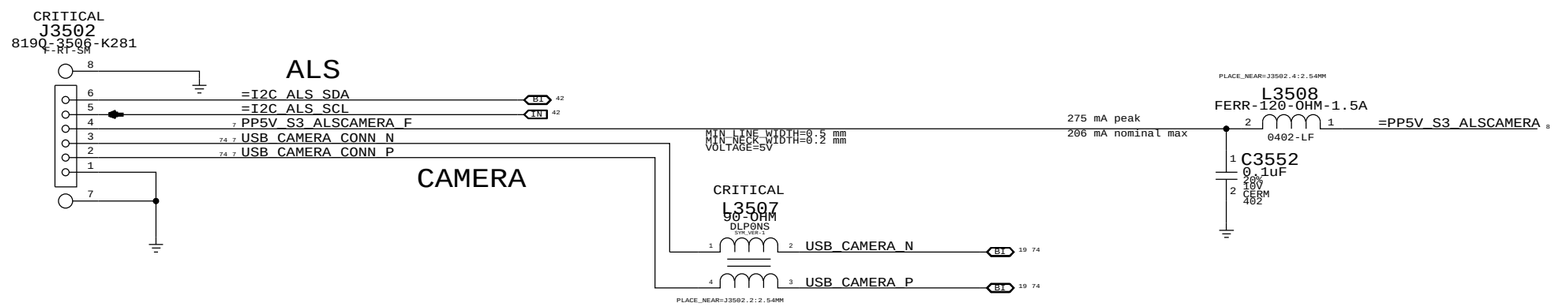
PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 34 OF 132
SHEET 31 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

518S0767



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
ALS/CAMERA CONNECTOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

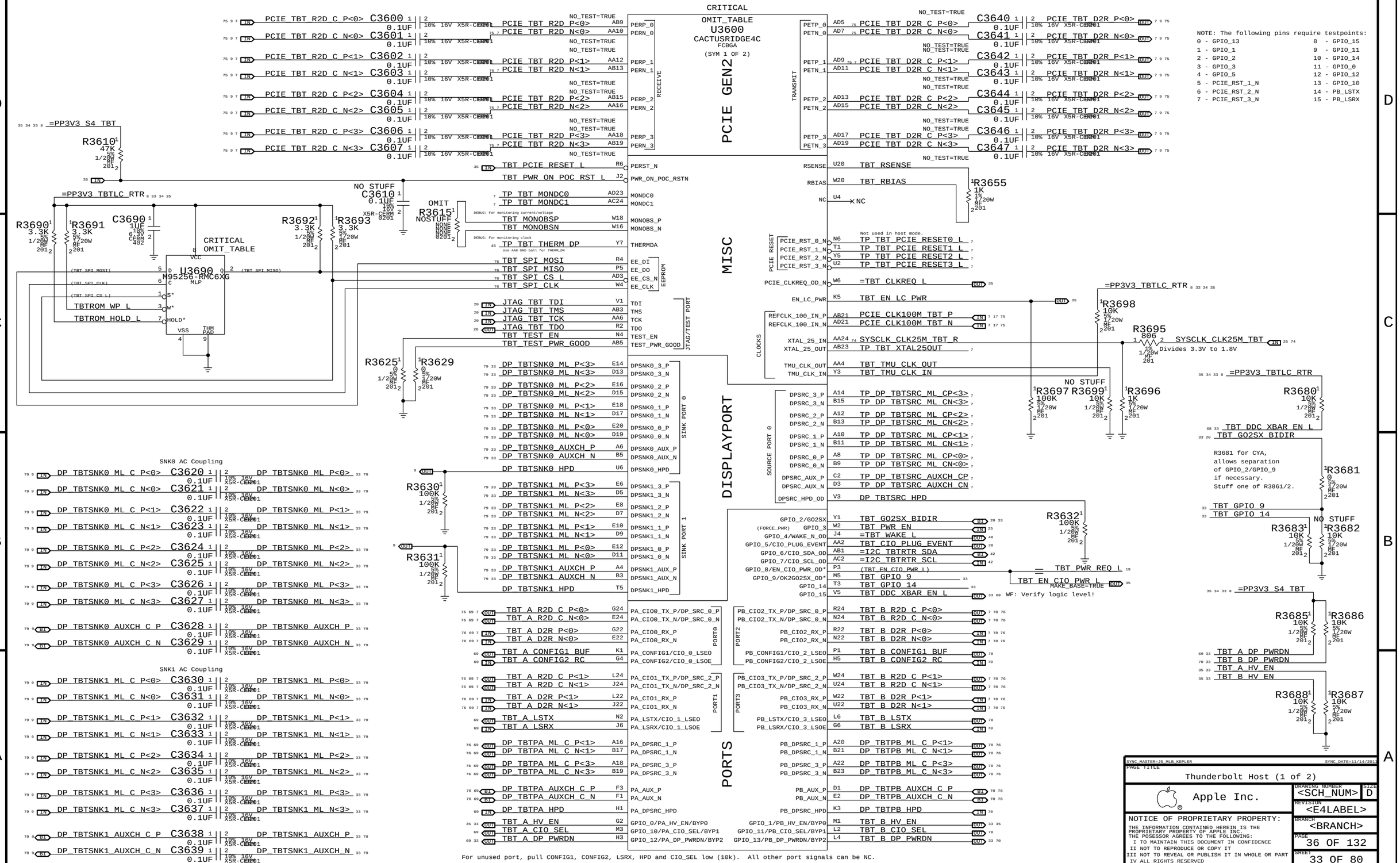
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 35 OF 132

SHEET 32 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE

Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

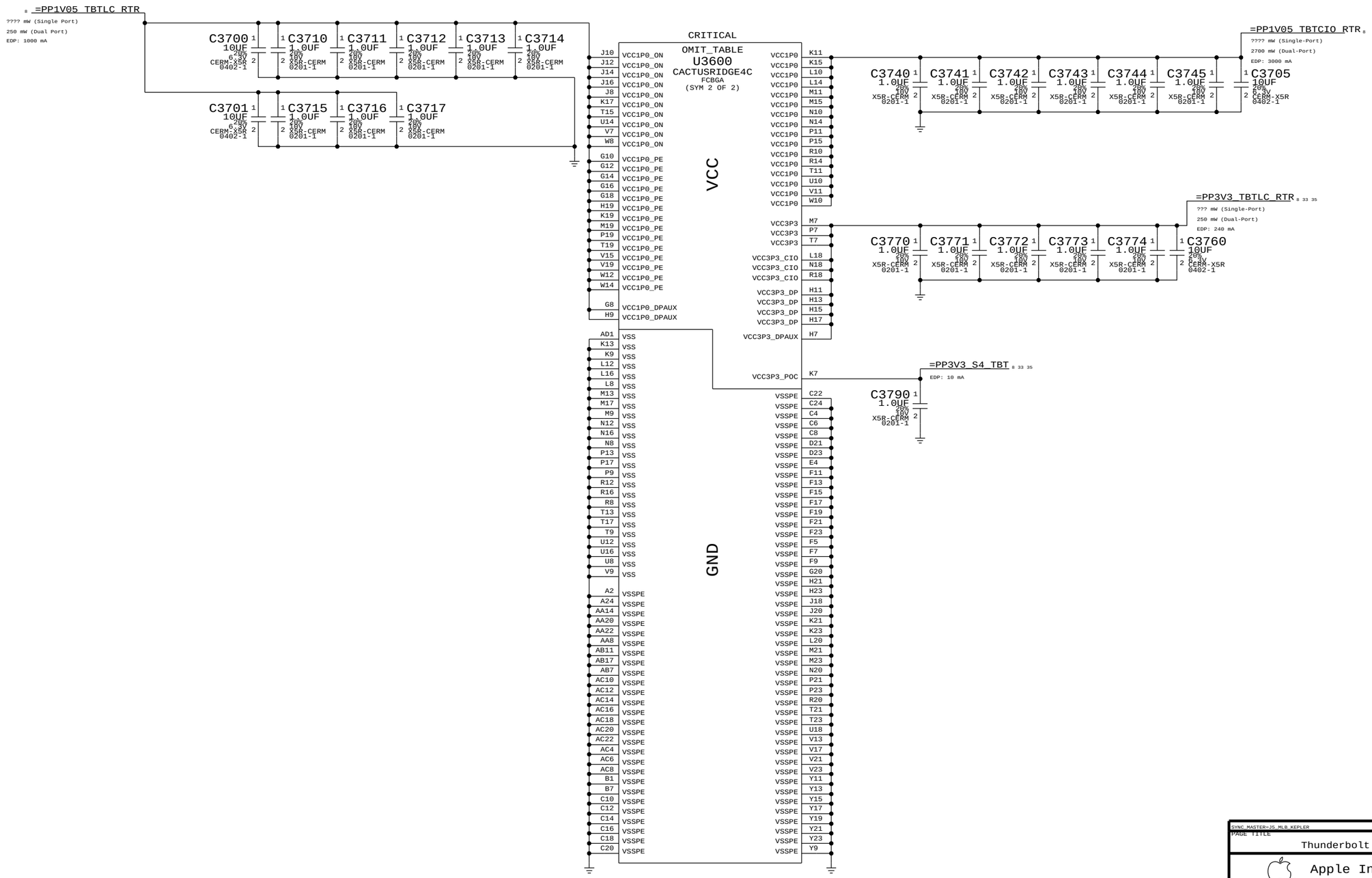
BRANCH <BRANCH>

PAGE 36 OF 132

SHEET 33 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 37 OF 132

SHEET 34 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Thunderbolt 15V Boost Regulator

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBTLC_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBTLC_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

=PPVIN_SW_TBTBST
8-13V Input
Changes required
for 2S.

CRITICAL
TBTBST:Y
Q3880
SI8409DB
BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here,
add property on another page.

CRITICAL
TBTBST:Y
L3895
3.3UH-6.5A
IHLP

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

TBTBST:Y R3880 470K 5% 1/16W MF-LF 402
TBTBST:Y C3880 0.1UF 10% 16V X5R-CERM 402
TBTBST_PWREN_DIV_L
TBTBST:Y R3881 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L
TBTBST:Y R3891 200K 1% 1/16W MF-LF 402 <R1>
TBTBST:Y C3860 10UF 20% 25V X5R-CERM 0603
TBTBST:Y C3861 10UF 20% 25V X5R-CERM 0603

CRITICAL
TBTBST:Y
U3890
LT3957
QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

TBTBST:Y Q3805 SSM6N37FEAPE SOT563
TBTBST:Y Q3805 SSM6N37FEAPE SOT563
TBT_A_HV_EN
TBT_B_HV_EN

TBTBST:Y C3890 2.2UF 20% 16V X5R-CERM 402
TBTBST:Y C3891 2.2UF 20% 16V X5R-CERM 402
TBTBST:Y C3892 2.2UF 20% 16V X5R-CERM 402
TBTBST:Y C3887 68PF 5% 50V C0G CERM 402-1
TBTBST:Y R3893 49.9K 1% 1/16W MF-LF 402
TBTBST:Y R3892 73.2K 1% 1/16W MF-LF 402 <R2>
TBTBST:Y C3893 0.0033UF 10% 50V CERM 402
TBTBST:Y R3894 26.7K 1% 1/16W MF-LF 402
TBTBST:Y C3894 0.33UF 10% 6.3V CERM-X5R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

TBTBST_SNS1
TBTBST:Y R3889 0 5% 1/20W MF 201
CRITICAL
TBTBST:Y
D3895
PDS540XF
PWRDI5
TBTBST_SNS2
XW3895
SM
PLACE_NEAR=C3895.1:2 mm
TBTBST_VSNS
TBTBST:Y C3888 10PF 5% 50V CERM 402
TBTBST:Y R3895 137K 1% 1/10W MF-LF 402 <Ra>
NO STUFF C3889 100PF 5% 50V CERM 402
TBTBST:Y R3896 15.8K 1% 1/10W MF-LF 402 <Rb>
TBTBST_FBX

=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
Freq = 500KHz

OMIT_TABLE C3895 4.7UF 20% 6.3V X6S-CERM 0603
OMIT_TABLE C3897 4.7UF 20% 6.3V X6S-CERM 0603
OMIT_TABLE C3898 4.7UF 20% 6.3V X6S-CERM 0603
OMIT_TABLE C389A 4.7UF 20% 6.3V X6S-CERM 0603
TBTBST:Y C3896 33UF-0.06OHM 20% 25V POLY-TANT CASE-D3L
TBTBST:Y C3899 0.001UF 10% 50V X7R 402

SGND shorted to
GND inside package,
no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

Supervisor & CLKREQ# Isolation

=PP3V3_S0_TBTPWRCTL
C3800 0.1UF 10% 16V X5R-CERM 0201
Q3840 SSM3K15FV SOD-VESM-HF
R3840 10K 5% 1/20W MF 201
TBT_EN_LC_PWR
TBT_EN_LC_ISOL
=TBT_RESET_L
Platform (PCIe) Reset
TBT_CLKREQ_L
Pull-ups provided by SB page.

CRITICAL
U3800
SLG4AP016V
TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
GND
THRM PAD

=PP3V3_TBTLC_RTR
R3807 100K 5% 1/20W MF 201
=PP1V05_TBTLC
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
=TBT_CLKREQ_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

NO STUFF R3816 0 5% 1/20W MF 201

TBTBST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
TBTBST:Y R3888 330K 5% 1/10W MF-LF 402
TBTBST_SHDN_DIV
TBTBST:Y R3887 330K 5% 1/10W MF-LF 402
TBTBST:Y Q3888 SSM6N37FEAPE SOT563
SMC_DELAYED_PWRGD

TBT_A_HV_EN
R3850 0 5% 1/20W MF 201
NO STUFF D3850 1N4448HLP-7 DFN1006
TBT_A_HV_EN_RC
C3850 1.0UF 10% 6.3V X5R-CERM 0201 NO STUFF

TBT_B_HV_EN
R3860 0 5% 1/20W MF 201
NO STUFF D3860 1N4448HLP-7 DFN1006
TBT_B_HV_EN_RC
C3865 1.0UF 10% 6.3V X5R-CERM 0201 NO STUFF

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

=PP3V3_S4_TBT
CRITICAL
U3830
TPS3808
QFN
VDD
SENSE
CT
RESET*
MR*
GND
THRM PAD
Pull-up: R3610
TBT_PWR_ON_POC_RST_L
TBTPOCRST_CT
TBTPOCRST_MR_L
C3831 0.0047UF 10% 16V CERM 402
C3830 0.1UF 10% 16V X5R 402
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms

Q3825 SSM6N37FEAPE SOT563
C3825 330PF 10% 16V X7R-CERM 0201
=PP3V3_S0_PCH_GPIO
R3830 100K 5% 1/20W MF 201
TBT_SW_RESET_L

3.3V TBT "LC" Switch

=PP3V3_S0_P3V3TBTFET
U3810
TPS22924
CSP
VIN
VOUT
ON
GND
CRITICAL
=PP3V3_TBTLC_FET
Max Current = 2A (85C)
R3811 0 5% 1/20W MF 201
C3810 1UF 20% 6.3V X5R 0201
C3811 1UF 20% 6.3V X5R 0201
NO STUFF
R3810 10K 5% 1/20W MF 201
TBT_EN_LC_ISOL_R

U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

R3812 0 5% 1/20W MF 201
TBT_EN_LC_RC
P1V05TBTS0_PGOOD

1.05V TBT "CIO" Switch

=PP1V05_S0_P1V05TBTREG
=PP3V3_TBTLC_RTR
R3820 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
U3820
TPS22920
CSP
VIN
VOUT
ON
GND
CRITICAL
=PP1V05_TBTCIO_FET
Max Current = 4A (85C)
C3820 1UF 20% 6.3V X5R 0201
Q3825 SSM6N37FEAPE SOT563
TBT_EN_CIO_PWR_L

U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP,CER,4.7UF,10%,25V,X6S,0603	C3895,C3897,C3898,C389A	CRITICAL	TBTBST:Y

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2012

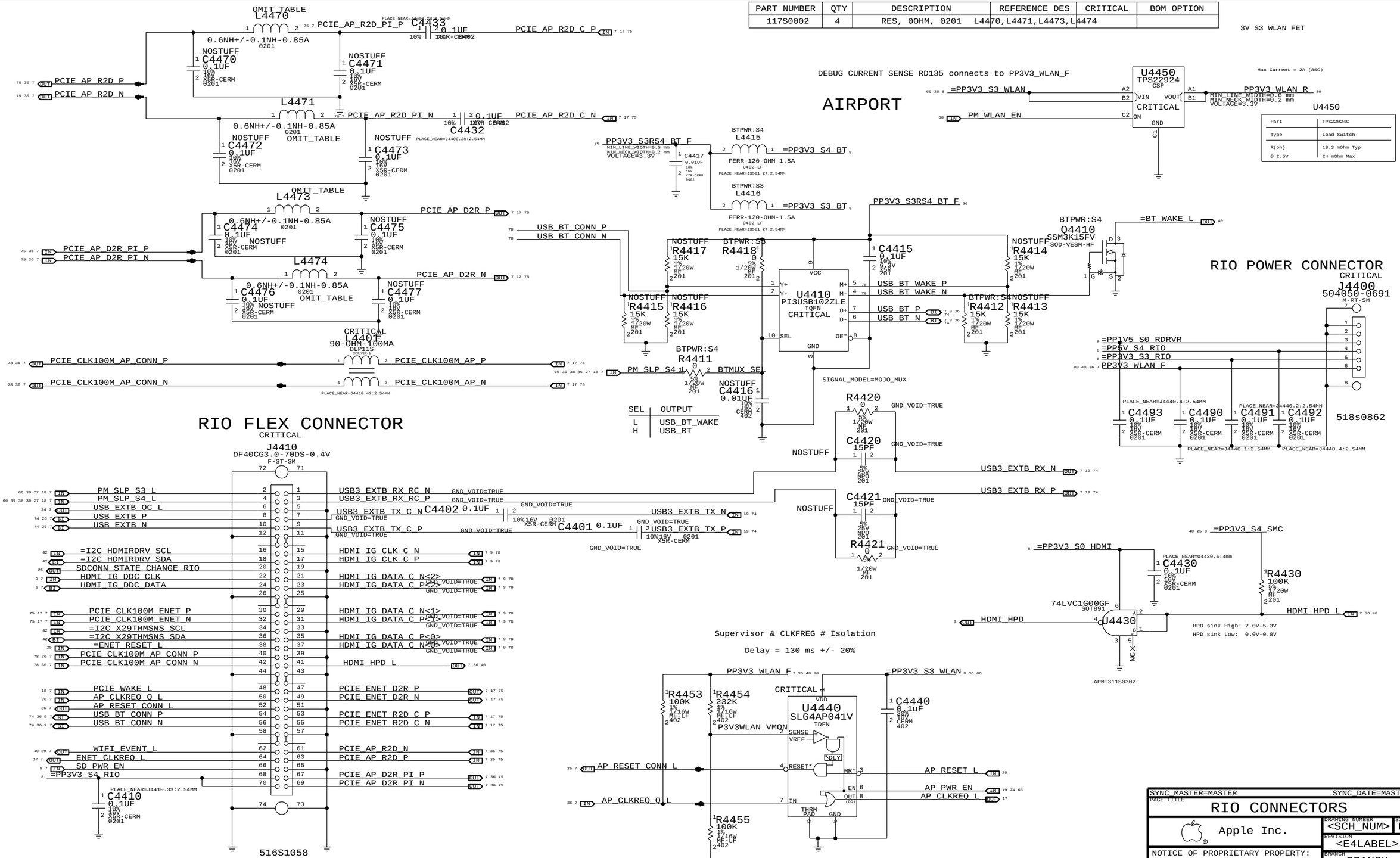
PAGE TITLE
Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 38 OF 132
SHEET 35 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0OHM, 0201	L4470,L4471,L4473,L4474		



SEL	OUTPUT
L	USB_BT_WAKE
H	USB_BT

Part	TPS22924C
Type	Load Switch
R(on)	18.3 mOhm Typ
@ 2.5V	24 mOhm Max

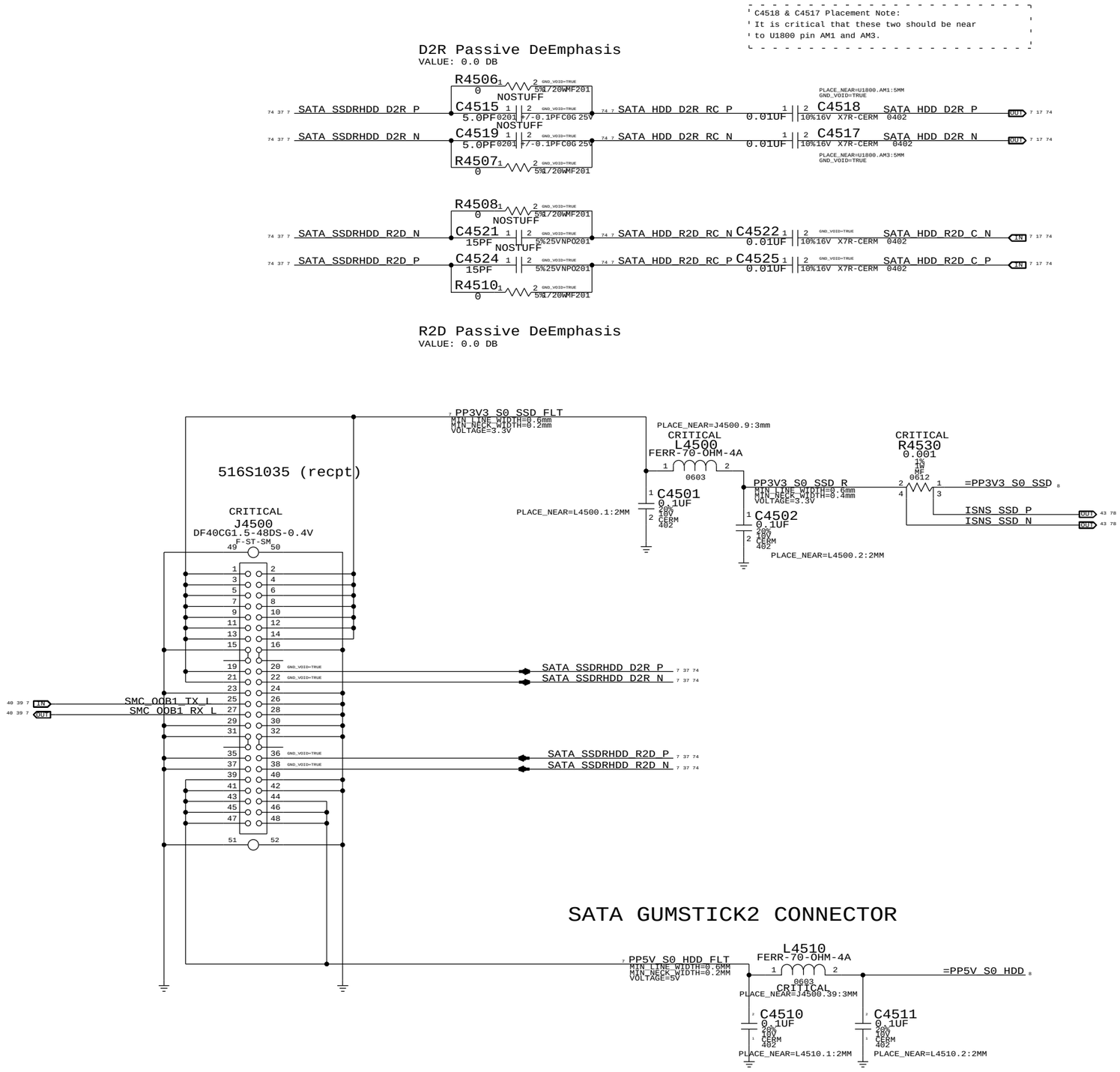
SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE
RIO CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 44 OF 132
SHEET 36 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

SSD/HDD Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

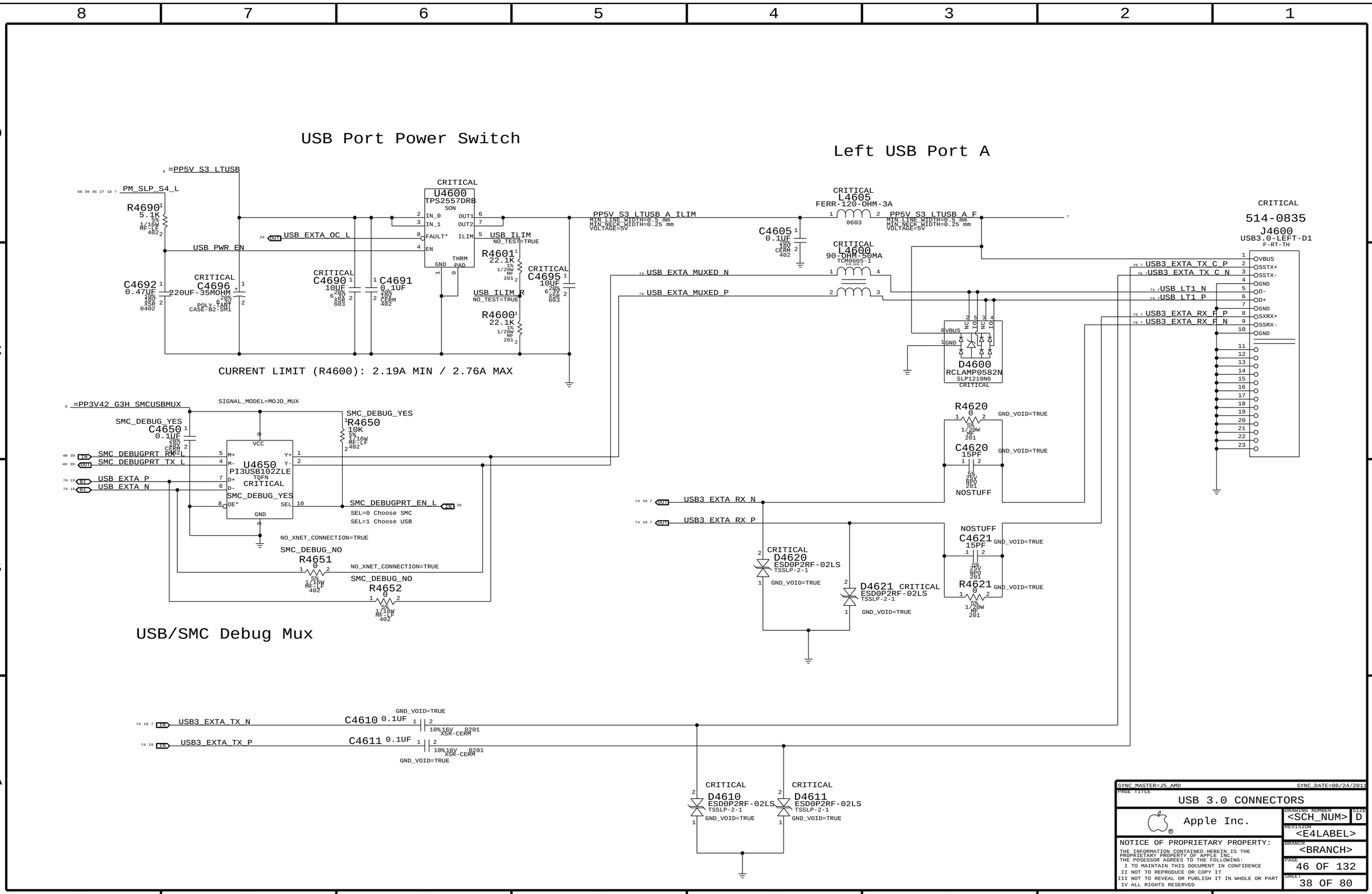
REVISION <E4LABEL>

BRANCH <BRANCH>

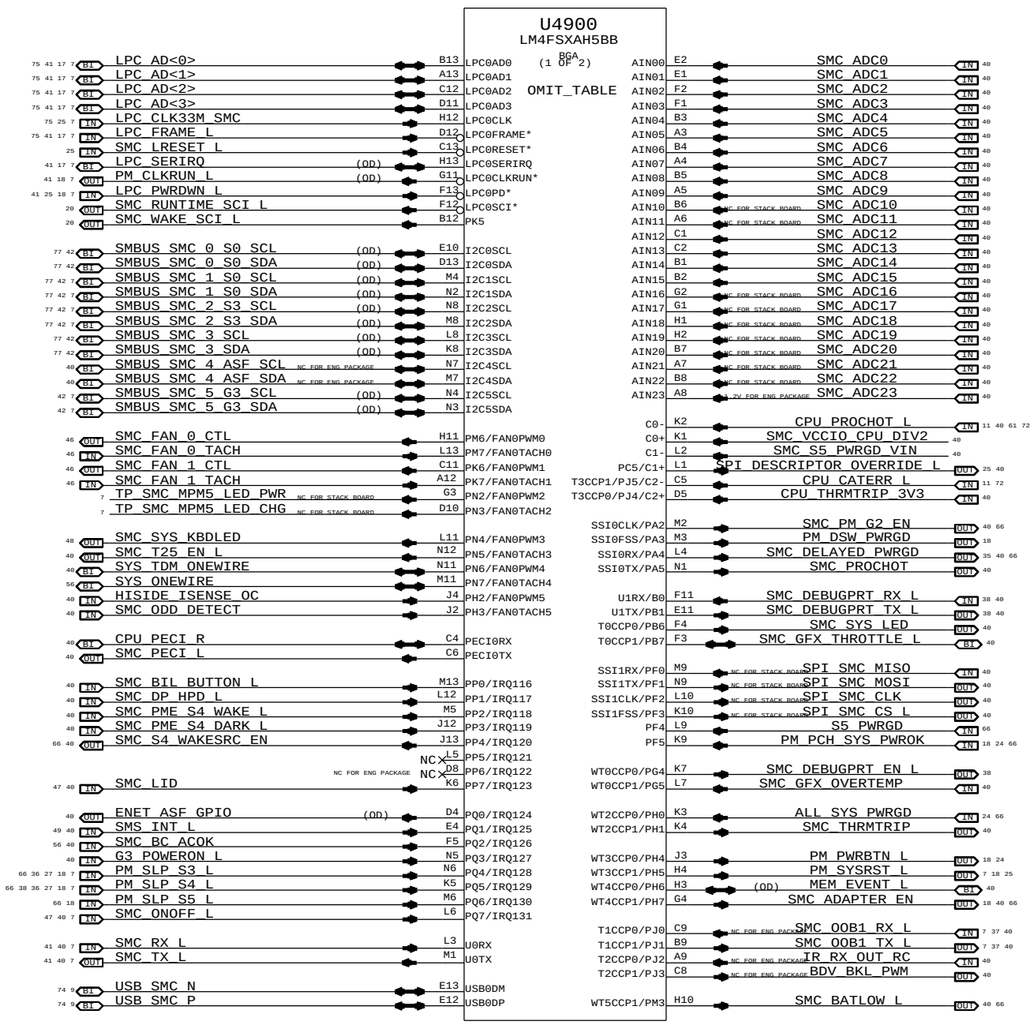
PAGE 45 OF 132

SHEET 37 OF 80

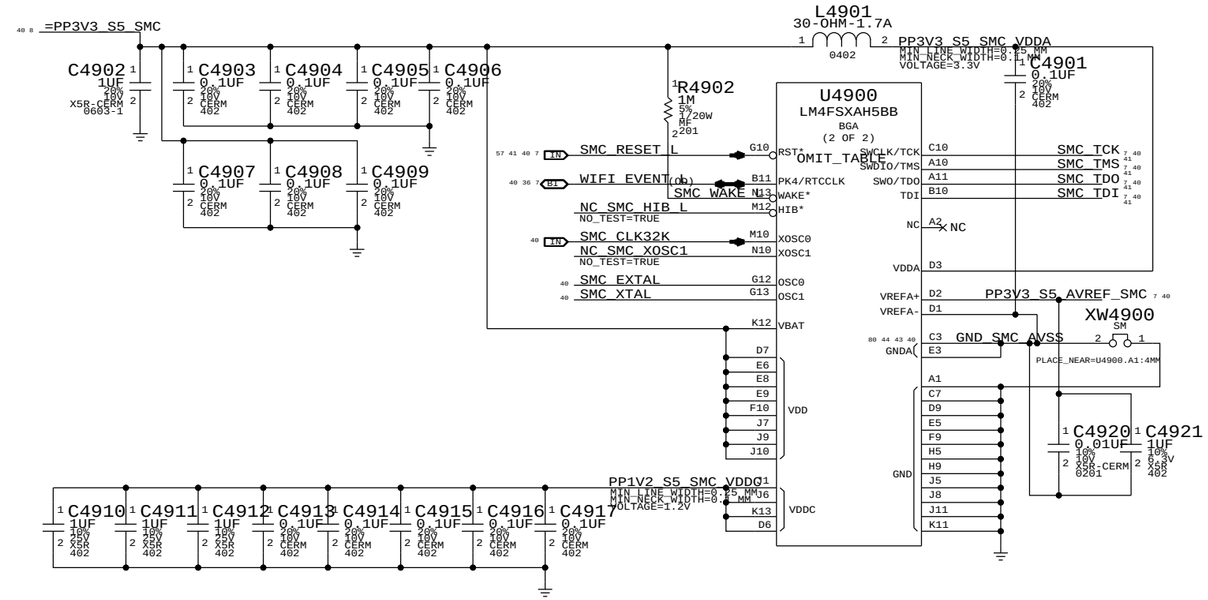
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


USB Port Power Switch
Left USB Port A
=PP5V_S3_LTUSB
PM_SLP_S4_L
R4690 5.1K
USB_EXTA_OC_L
USB_PWR_EN
C4692 0.47UF
CRITICAL C4696 220UF-35MOHM
CRITICAL C4690 10UF
C4691 0.1UF
CRITICAL U4600 TPS2557DRB
IN_0 IN_1 FAULT* EN OUT1 OUT2 ILIM THRM PAD GND
R4601 22.1K
USB_ILIM_R
R4600 22.1K
CRITICAL C4695 10UF
PP5V_S3_LTUSB_A_ILIM
CRITICAL L4605 FERR-120-OHM-3A
PP5V_S3_LTUSB_A_F
C4605 0.1UF
CRITICAL L4600 90-OHM-50MA
USB_EXTA_MUXED_N
USB_EXTA_MUXED_P
D4600 RCLAMP0582N
CRITICAL 514-0835 J4600 USB3.0-LEFT-D1
USB3_EXTA_TX_C_P
USB3_EXTA_TX_C_N
USB_LT1_N
USB_LT1_P
USB3_EXTA_RX_F_P
USB3_EXTA_RX_F_N
CURRENT LIMIT (R4600): 2.19A MIN / 2.76A MAX
=PP3V42_G3H_SMCUSBMUX
SIGNAL_MODEL=MOJO_MUX
SMC_DEBUG_YES
C4650 0.1UF
R4650 10K
SMC_DEBUGPRT_RX_L
SMC_DEBUGPRT_TX_L
U4650 PI3USB102ZLE TQFN CRITICAL
USB_EXTA_P
USB_EXTA_N
SMC_DEBUGPRT_EN_L
SEL=0 Choose SMC
SEL=1 Choose USB
NO_XNET_CONNECTION=TRUE
SMC_DEBUG_NO
R4651 0
R4652 0
USB/SMC Debug Mux
R4620 0
C4620 15PF
NOSTUFF
C4621 15PF
R4621 0
USB3_EXTA_RX_N
USB3_EXTA_RX_P
CRITICAL D4620 ESD0P2RF-02LS
D4621 CRITICAL ESD0P2RF-02LS
GND_VOID=TRUE
USB3_EXTA_TX_N
USB3_EXTA_TX_P
C4610 0.1UF
C4611 0.1UF
CRITICAL D4610 ESD0P2RF-02LS
CRITICAL D4611 ESD0P2RF-02LS
SYNC_MASTER=J5_AMD
SYNC_DATE=08/24/2011
PAGE TITLE
USB 3.0 CONNECTORS
Apple Inc.
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 46 OF 132
SHEET 38 OF 80
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

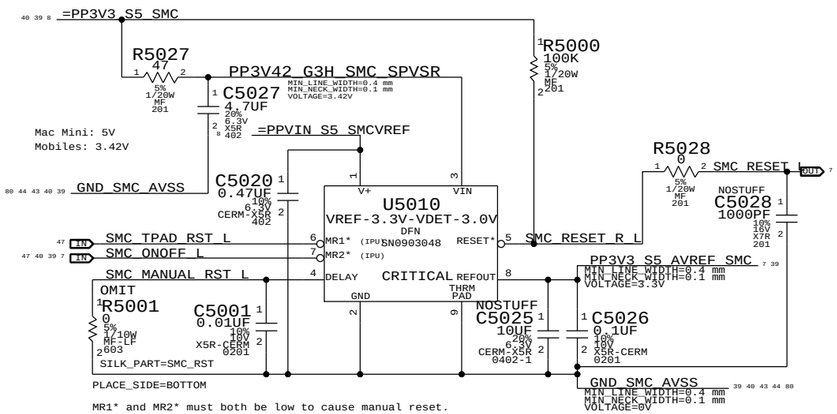
BRANCH: <BRANCH>

PAGE: 49 OF 132

SHEET: 39 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

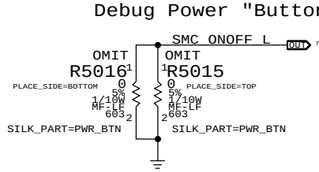
SMC Reset "Button", Supervisor & AVREF Supply

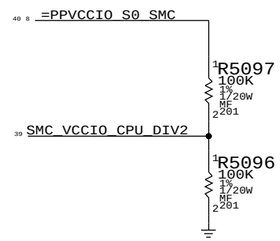


MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

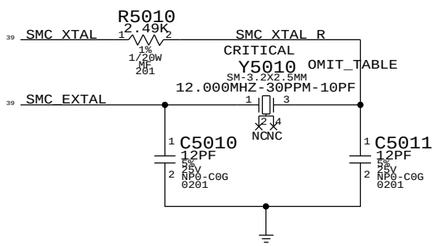
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"





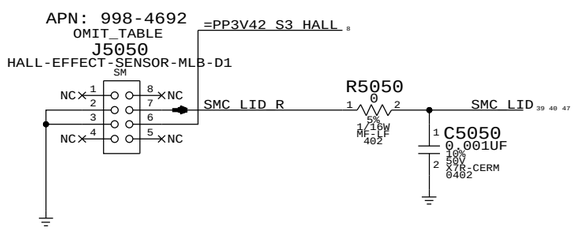
SMC Crystal Circuit



SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

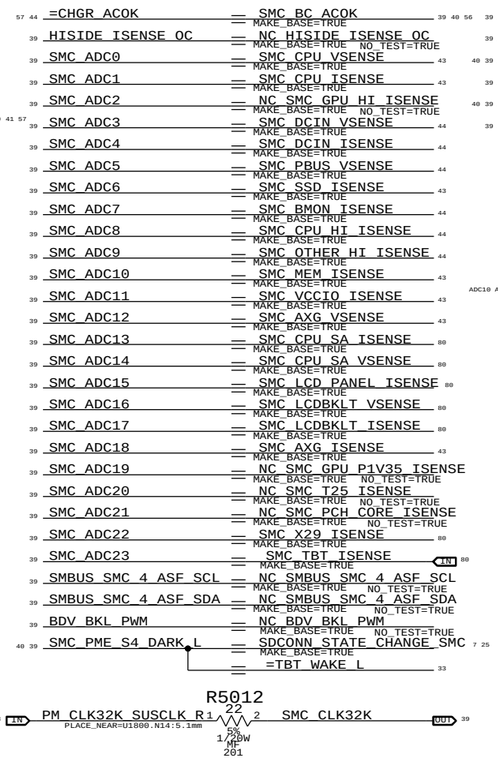
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0486	1	XTAL,12MHZ,30PPM,10PF,3.2X2.5X0.7MM,90C	Y5010	CRITICAL	

Hall Effect pads

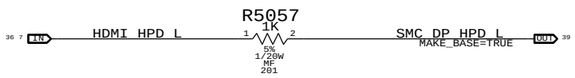


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-9320	1	SUBASSY,PCBA HALL EFFECT,J4	J5050	CRITICAL	

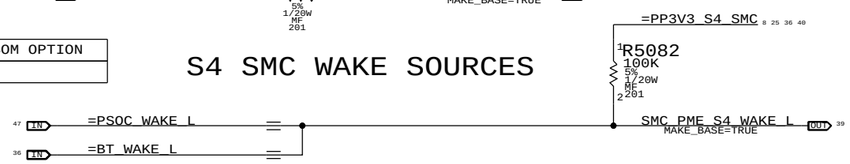
639-3261 (J4 Hall effect board) reports to 607-9320



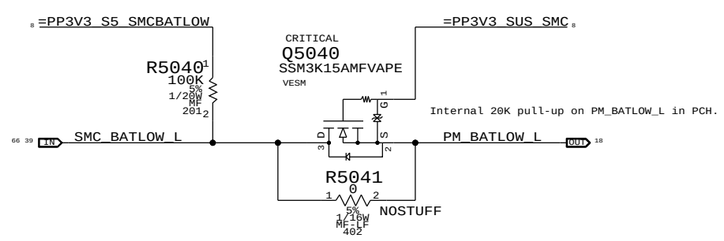
HDMI HPD ESD PROTECTION

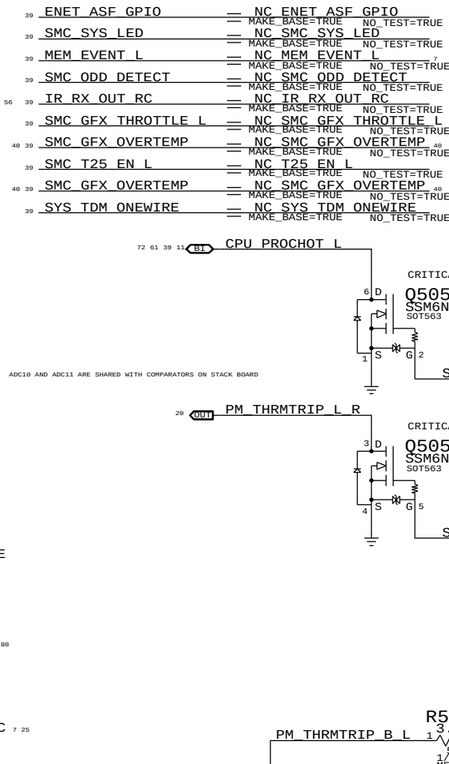


S4 SMC WAKE SOURCES

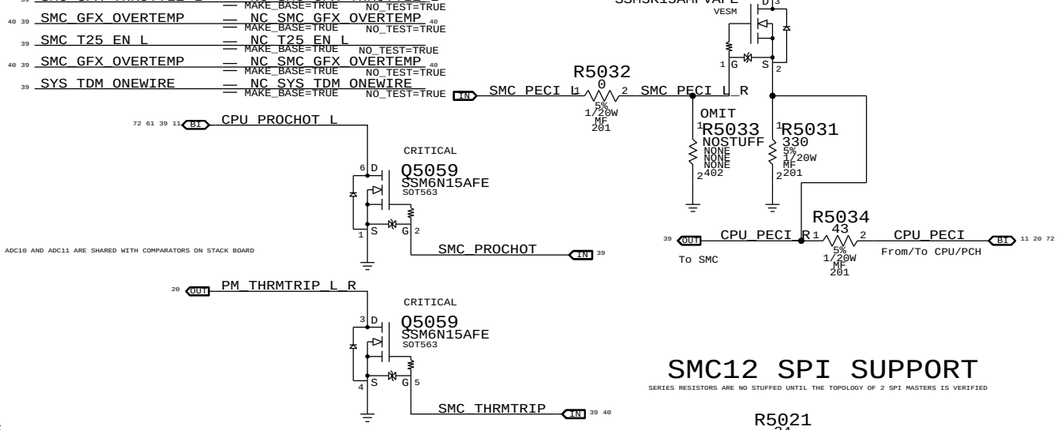


BATLOW# ISOLATION



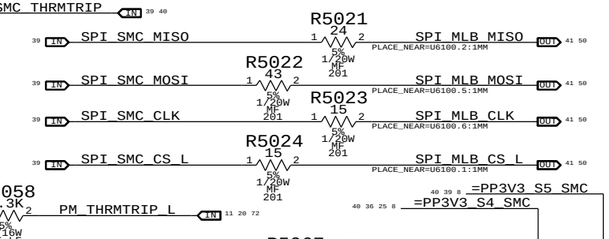


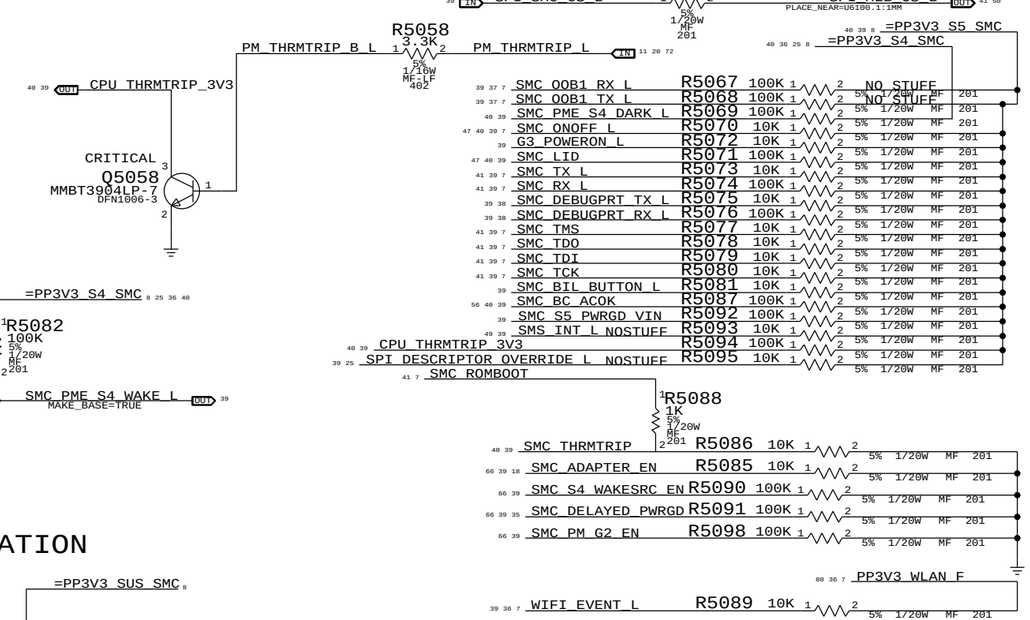
SMC12 PECI SUPPORT



SMC12 SPI SUPPORT

SERIES RESISTORS ARE NO STUFFED UNTIL THE TOPOLOGY OF 2 SPI MASTERS IS VERIFIED





SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

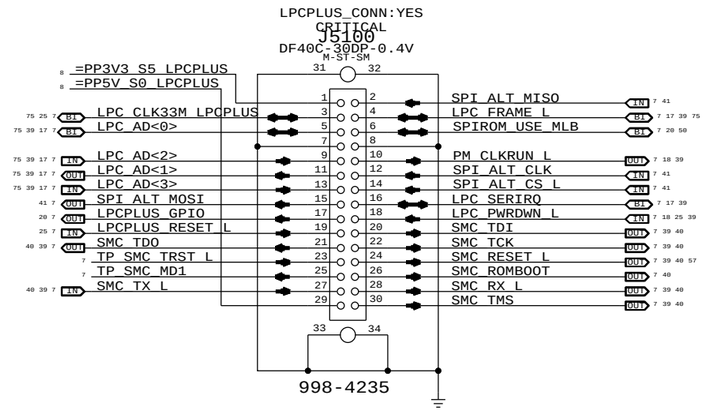
BRANCH: <BRANCH>

PAGE: 50 OF 132

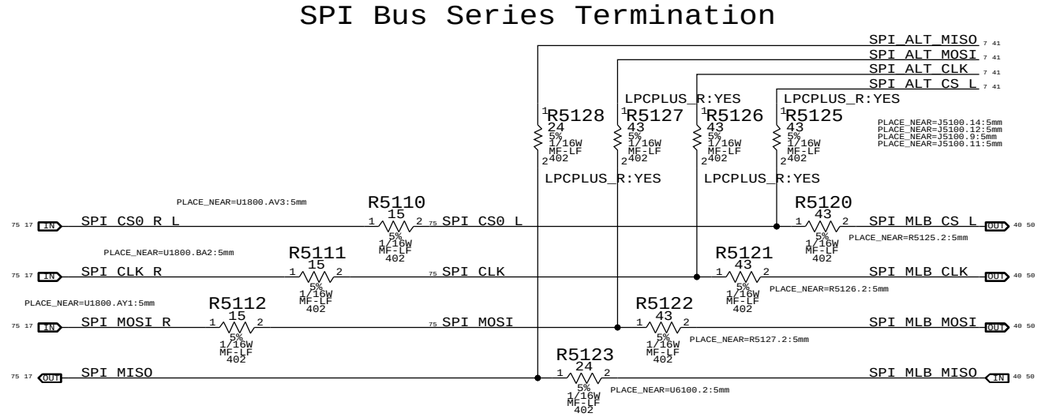
SHEET: 40 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2013

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 51 OF 132

SHEET 41 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

R5200 1K 5% 1/20W MF 201 2 — R5201 1K 5% 1/20W MF 201 2

Panther Point
U1800
(MASTER)
- SMBUS_PCH_CLK (MAKE_BASE=TRUE)
- SMBUS_PCH_DATA (MAKE_BASE=TRUE)

TBT
U3600
(WRITE: 0XXX READ: 0XXX)
- =I2C_TBTRTR_SCL
- =I2C_TBTRTR_SDA

VRef DACs
U3300
(Write: 0x98 Read: 0x99)
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA

AUDIO
U6411
(WRITE: 0X34 READ: 0X35)

Margin Control
U3301
(Write: 0x30 Read: 0x31)
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

AUDIO
U6410
(WRITE: 0X32 READ: 0X33)

MIKEY
U6751
(WRITE: 0X72 READ: 0X73)
- =I2C_MIKEY_SCL
- =I2C_MIKEY_SDA

AUDIO
U6400
(WRITE: 0XE0 READ: 0XE1)

XDP Connectors
J2500 & J2550
(MASTER)
- =SMBUS_XDP_SCL
- =SMBUS_XDP_SDA

AUDIO
U6750
(WRITE: 0X76 READ: 0X77)

HDMI Redriver (on RIO)
J4410
(WRITE: 0xCC READ: 0xCD)
- =I2C_HDMIRDRV_SCL
- =I2C_HDMIRDRV_SDA

LED BACKLIGHT
U9700
(WRITE: 0X58 READ: 0X59)
- =I2C_BKL_1_SCL
- =I2C_BKL_1_SDA

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

R5250 4.7K 5% 1/20W MF 201 2 — R5251 4.7K 5% 1/20W MF 201 2

SMC
U4900
(MASTER)
- SMB_0_S0_CLK — SMBUS_SMC_0_S0_SCL (MAKE_BASE=TRUE)
- SMB_0_S0_DATA — SMBUS_SMC_0_S0_SDA (MAKE_BASE=TRUE)

GPU Temp (Ext)
EMC1414-A: U5550
(Write: 0x98 Read: 0x99)
- =SMBUS_GPUTHMSNS_SCL
- =SMBUS_GPUTHMSNS_SDA

SMC "5" SMBUS CONNECTIONS

=PP3V42_G3H_SMBUS_SMC_5

R5280 2.0K 5% 1/20W MF 201 2 — R5281 2.0K 5% 1/20W MF 201 2

SMC
U4900
(MASTER)
- SMB_5_CLK — SMBUS_SMC_5_G3_SCL (MAKE_BASE=TRUE)
- SMB_5_DATA — SMBUS_SMC_5_G3_SDA (MAKE_BASE=TRUE)

Battery Charger
ISL6258 - U7000
(Write: 0x12 Read: 0x13)
- =SMBUS_CHGR_SCL
- =SMBUS_CHGR_SDA

Battery
Battery Manager - (Write: 0x16 Read: 0x17)

Battery
J6955
(See Table)
- =SMBUS_BATT_SCL
- =SMBUS_BATT_SDA

SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

R5270 1K 5% 1/20W MF 201 2 — R5271 1K 5% 1/20W MF 201 2

SMC
U4900
(MASTER)
- SMB_2_S3_CLK — SMBUS_SMC_2_S3_SCL (MAKE_BASE=TRUE)
- SMB_2_S3_DATA — SMBUS_SMC_2_S3_SDA (MAKE_BASE=TRUE)

Trackpad
J5800
(Write: 0x90 Read: 0x91)
- =I2C_TPAD_SCL
- =I2C_TPAD_SDA

ALS
J3502
(Write: 0x72 Read: 0x73)
- =I2C_ALS_SCL
- =I2C_ALS_SDA

SMS
U5920
(WRITE: 0X30/31 READ: 0X32/33)
- =I2C_SMC_SMS_SCL
- =I2C_SMC_SMS_SDA

GYRO
U5940
(WRITE: 0XD0 READ: 0XD1)
- =I2C_SMC_GYRO_SCL
- =I2C_SMC_GYRO_SDA

SMC "3" SMBUS CONNECTIONS

=PP3V3_S3_SMBUS_SMC_3

R5290 4.7K 5% 1/20W MF 201 2 (DEBUG_ADC) — R5291 4.7K 5% 1/20W MF 201 2 (DEBUG_ADC)

SMC
U4900
(MASTER)
- SMB_3_CLK — SMBUS_SMC_3_SCL (MAKE_BASE=TRUE)
- SMB_3_DATA — SMBUS_SMC_3_SDA (MAKE_BASE=TRUE)

DEBUG SENSOR ADC A
UD000
(Write: 0x10 Read: 0x11)
- =I2C_SMC_ADCS_SCL
- =I2C_SMC_ADCS_SDA

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

R5210 8.2K 5% 1/20W MF 201 2 — R5211 8.2K 5% 1/20W MF 201 2

Panther Point
U1800
(MASTER)
- SML_PCH_0_CLK (MAKE_BASE=TRUE)
- SML_PCH_0_DATA (MAKE_BASE=TRUE)

SMC "1" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_1_S0

R5260 1K 5% 1/20W MF 201 2 — R5261 1K 5% 1/20W MF 201 2

SMC
U4900
(MASTER)
- SMB_1_S0_CLK — SMBUS_SMC_1_S0_SCL (MAKE_BASE=TRUE)
- SMB_1_S0_DATA — SMBUS_SMC_1_S0_SDA (MAKE_BASE=TRUE)

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5570
(Write: 0x98 Read: 0x99)
- =I2C_CPUTHMSNS_SCL
- =I2C_CPUTHMSNS_SDA

PCH "SMLink 1" Connections

Panther Point
U1800
(Write: 0x88 Read: 0x89)
- SML_PCH_1_CLK
- SML_PCH_1_DATA

SMLink 1 is slave port to access PCH & CPU via PECI.

X29 TEMP
TMP105: U5523
(WRITE: 0X92 READ: 0X93)
- =I2C_X29THMSNS_SCL
- =I2C_X29THMSNS_SDA

SPKR TEMP
U6420
(WRITE: 0XD8 READ: 0XD9)
U6421
(WRITE: 0X38 READ: 0X39)
- =I2C_SPKRTHMSNS_SCL
- =I2C_SPKRTHMSNS_SDA

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

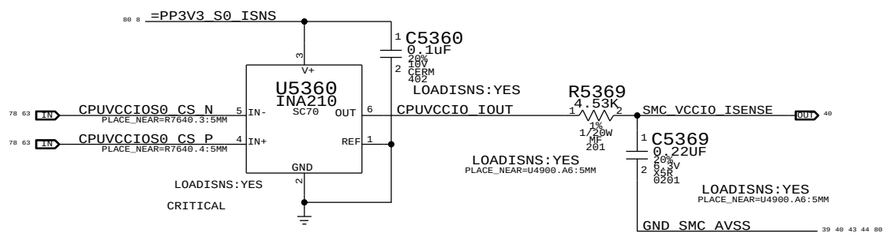
PAGE: 52 OF 132

SHEET: 42 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

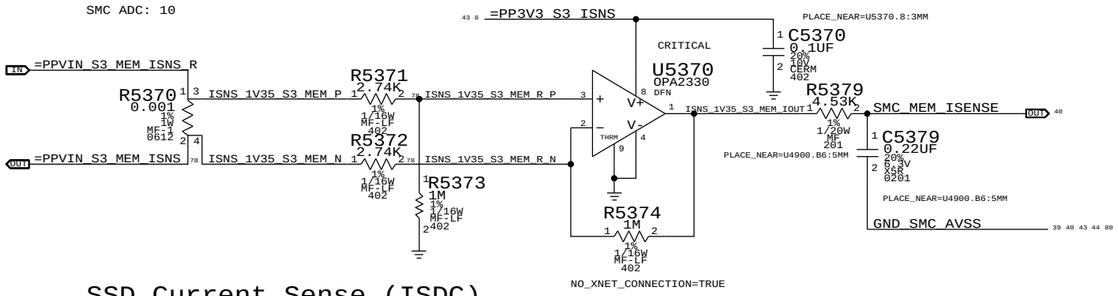
CPU/PCH VCCIO & TBT 1.05V Load Side Current Sense (IC1C)

Gain: 200x, EDP: 20 A
Rsense: 0.001 (R7640)
V across Rsense: 15 mV
SMC ADC: 11



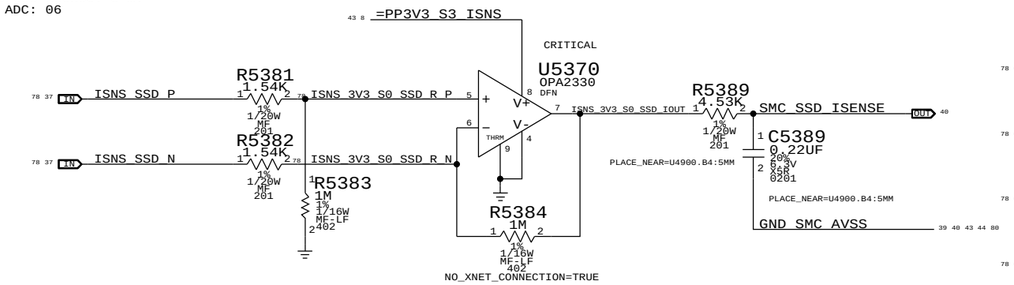
DDR 1.35V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
SMC ADC: 10



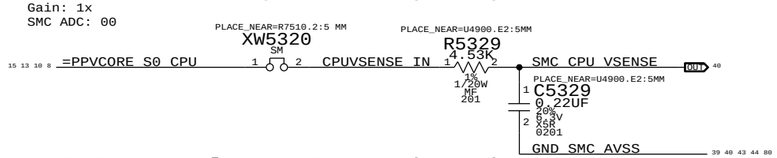
SSD Current Sense (ISDC)

Gain: 649.35x, EDP: 5 A (16.5 W)
Rsense: 0.001 (R5370)
V across Rsense: 5 mV
SMC ADC: 06



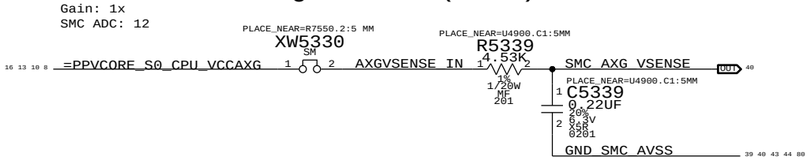
CPU Core Voltage Sense (VC0C)

Gain: 1x
SMC ADC: 00



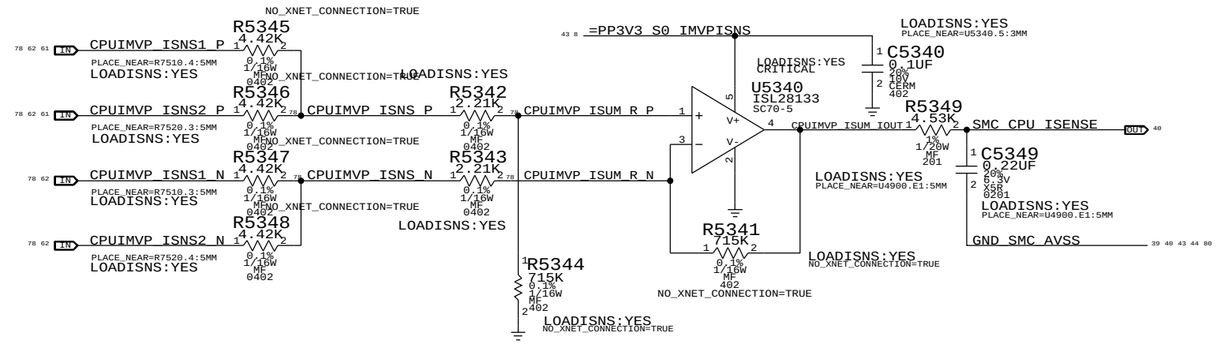
AXG Core Voltage Sense (VN0C)

Gain: 1x
SMC ADC: 12



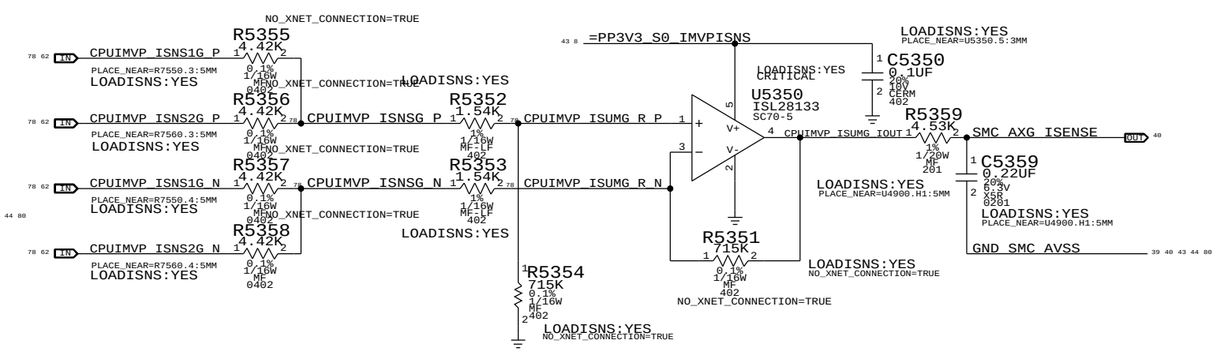
CPU Core Load Side Current Sense (IC0C)

Gain: 161.7x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
SMC ADC: 01



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
SMC ADC: 18



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC MASTER=D1 SENSORS SYNC DATE=02/20/2012

PAGE TITLE
Power Sensor: Load Side

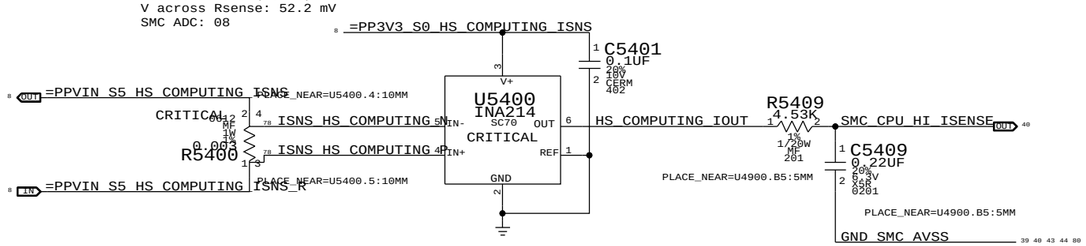
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 53 OF 132
SHEET 43 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

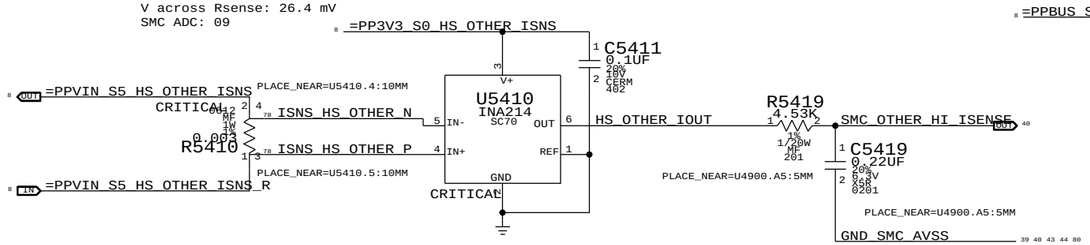
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
SMC ADC: 08



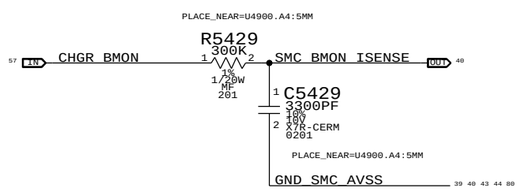
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
SMC ADC: 09



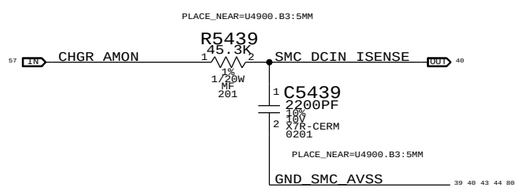
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x, EDP: 6.6 A
Rsense: 0.010 (R7050)
SMC ADC: 07



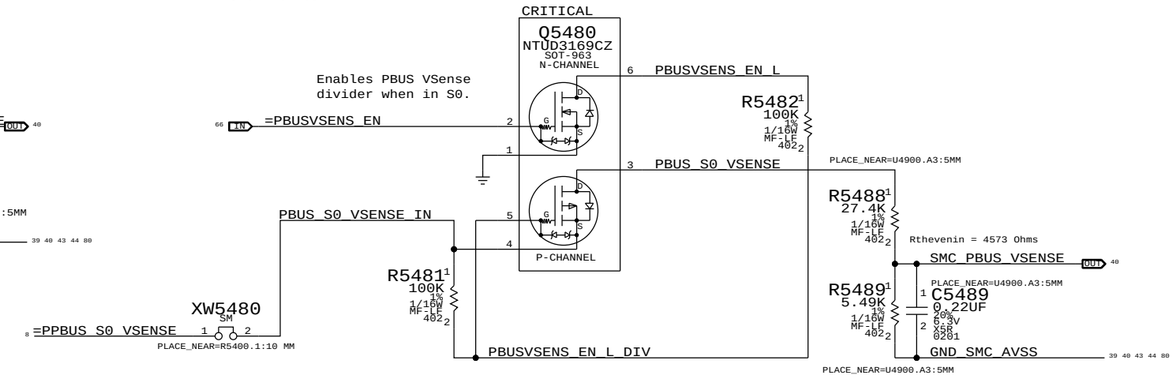
DC-In (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 04



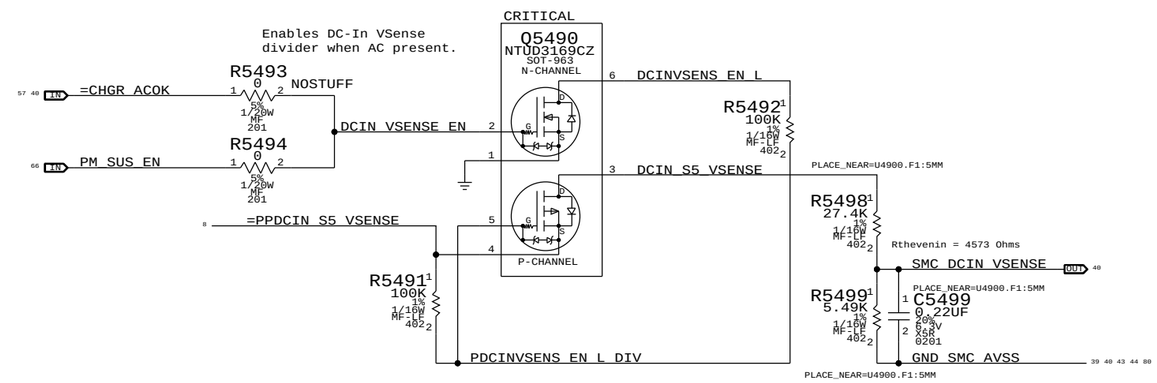
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
SMC ADC: 05



DC In Voltage Sense & Enable (VD0R)

Gain: 0.167x
SMC ADC: 03



SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE
Power Sensor: High Side

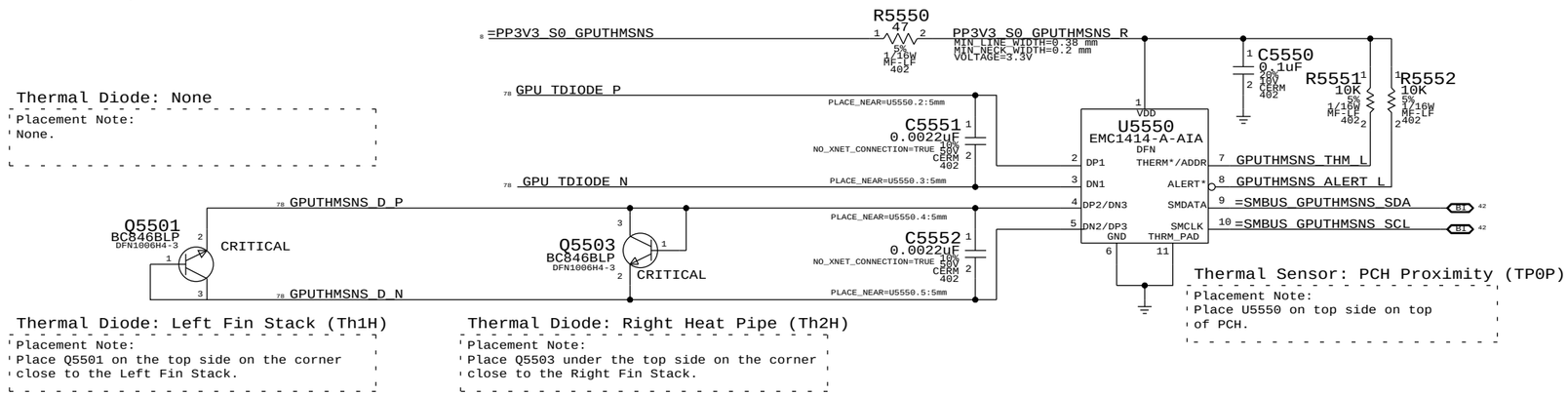
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 54 OF 132
SHEET 44 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

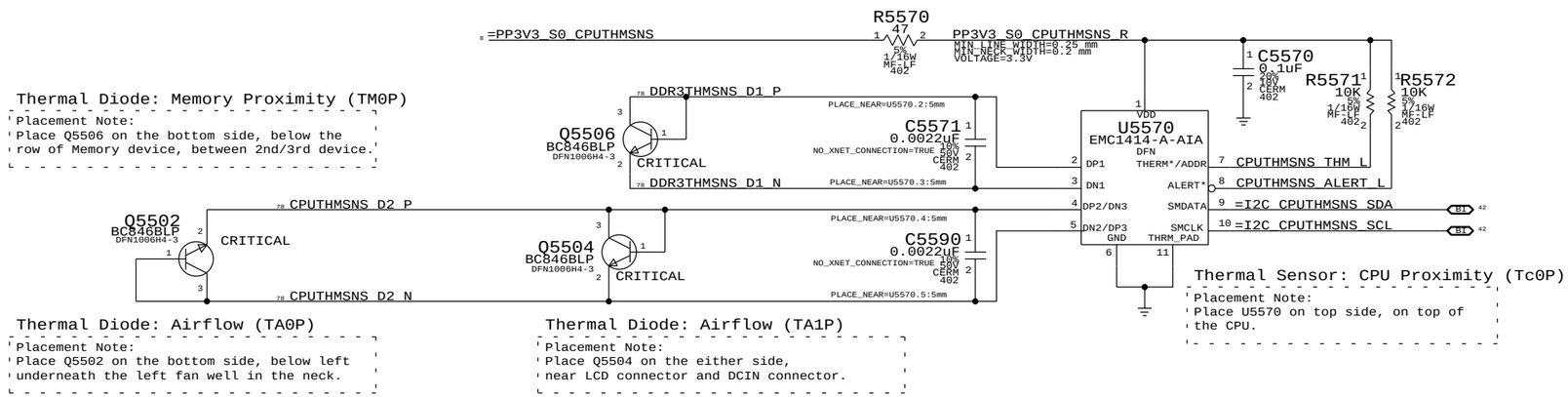
Thermal Sensor A:
PCH Proximity, Left Fin Pipe, Right Fin Stack

I2C Write: 0x98, I2C Read: 0x99

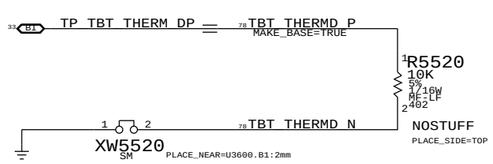


Thermal Sensor B:
CPU Proximity, Memory Proximity, Airflow

I2C Write: 0x98, I2C Read: 0x99



Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

SYNC_MASTER=D1_SENSORS SYNC_DATE=02/20/2012

PAGE TITLE

Thermal Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

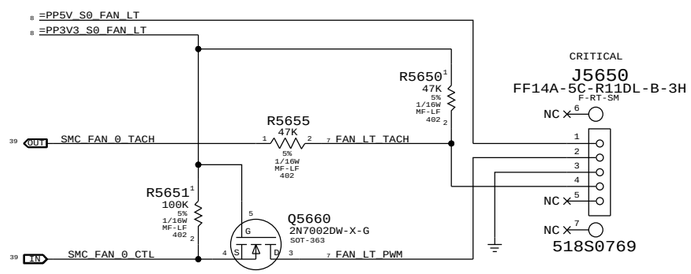
BRANCH <BRANCH>

PAGE 55 OF 132

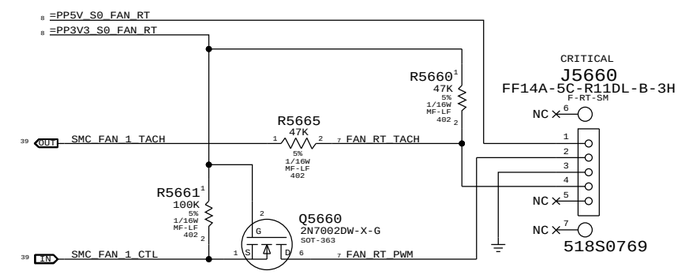
SHEET 45 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Left Fan



Right Fan



SYNC MASTER=J5_MLB SYNC DATE=07/29/2013

PAGE TITLE

Fan Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

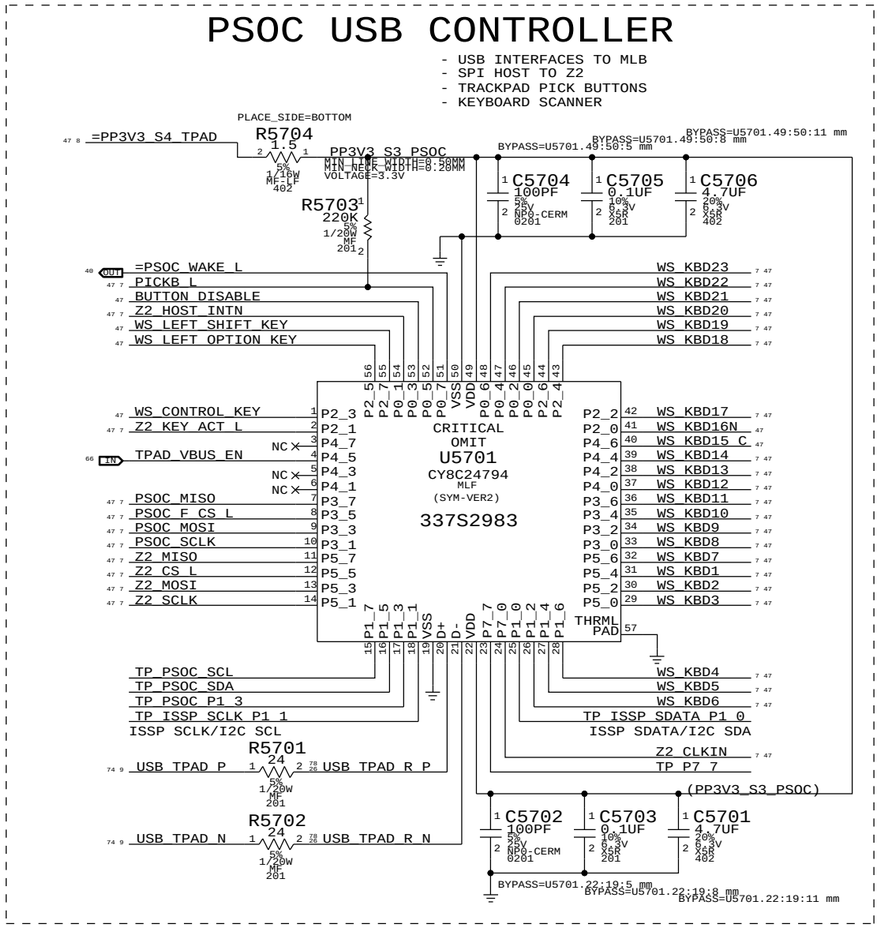
PAGE 56 OF 132

SHEET 46 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

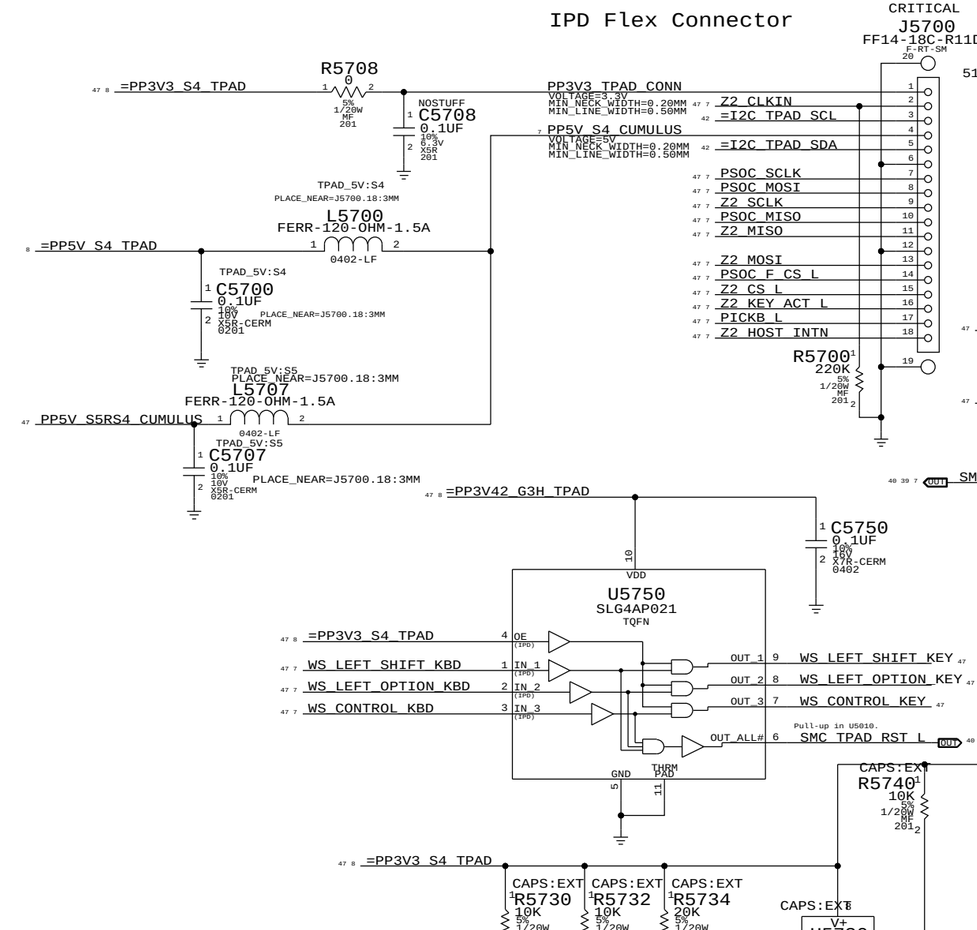
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER

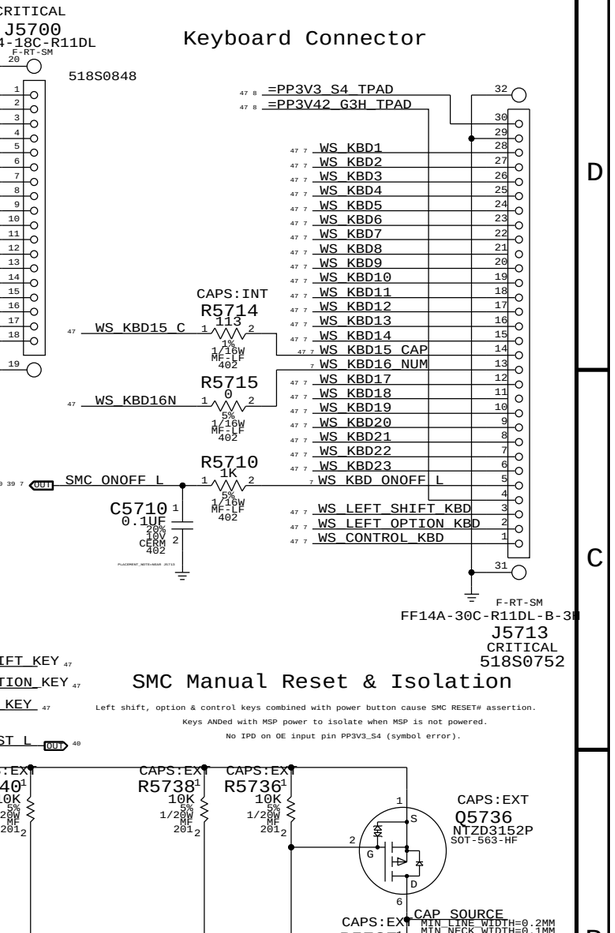


IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA (MAX) 60MA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

IPD Flex Connector



Keyboard Connector



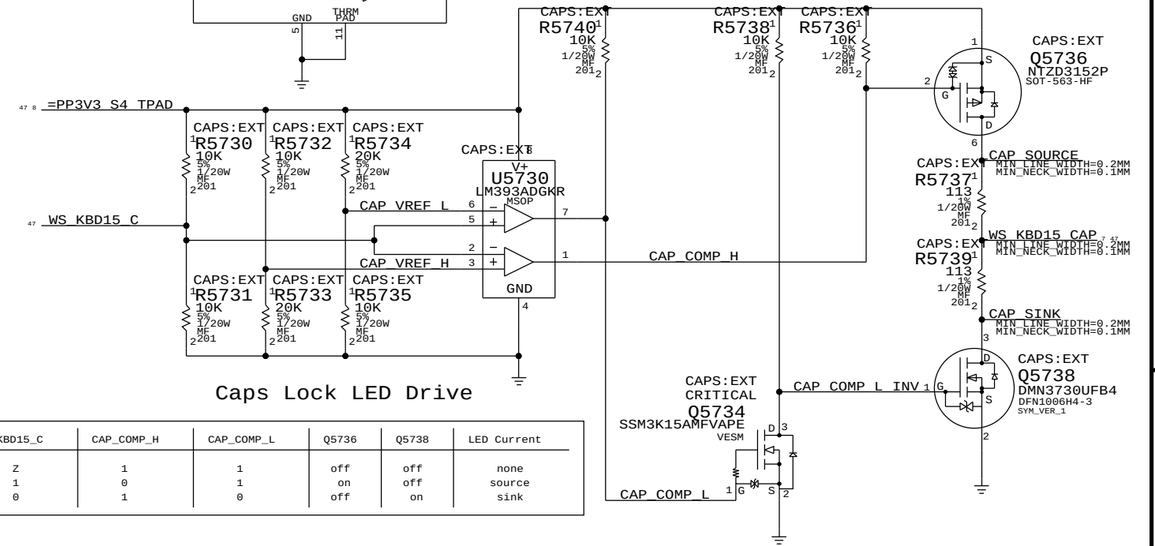
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC_RESET# assertion.

Keys ANDed with MSP power to isolate when MSP is not powered.

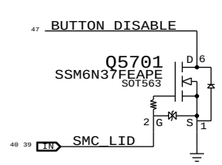
No IPD on OE input pin PP3V3_S4 (symbol error).

Caps Lock LED Drive



WS_KBD15_C	CAP_COMP_H	CAP_COMP_L	Q5736	Q5738	LED Current
Z	1	1	off	off	none
1	0	1	on	off	source
0	1	0	off	on	sink

TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800

THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

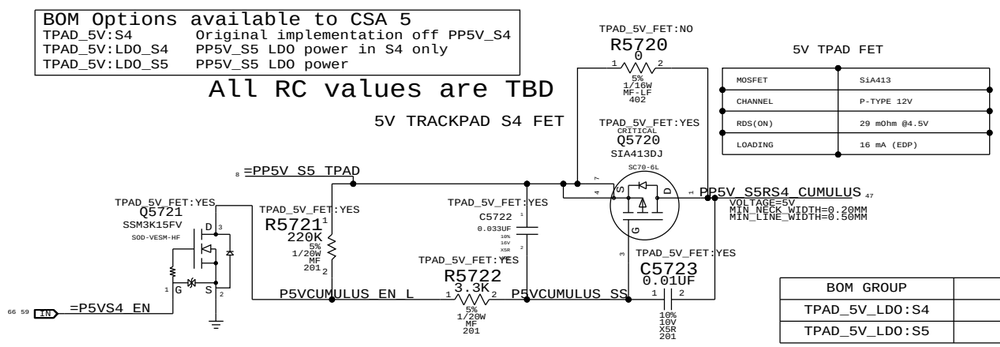
THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

BOM Options available to CSA 5

TPAD_5V:S4	Original implementation off PP5V_S4
TPAD_5V:LDO_S4	PP5V_S5 LDO power in S4 only
TPAD_5V:LDO_S5	PP5V_S5 LDO power

All RC values are TBD

5V TRACKPAD S4 FET



5V TPAD FET

MOSFET	SiA413
CHANNEL	P-TYPE 12V
RDS(ON)	29 mOhm @4.5V
LOADING	16 mA (EDP)

BOM GROUP	BOM OPTIONS
TPAD_5V_LDO:S4	TPAD_5V_FET:YES,TPAD_5V:S5
TPAD_5V_LDO:S5	TPAD_5V_FET:NO,TPAD_5V:S5

SYNC_MASTER=D2_MLB_KEPLER SYNC_DATE=12/08/2011

PAGE TITLE

KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

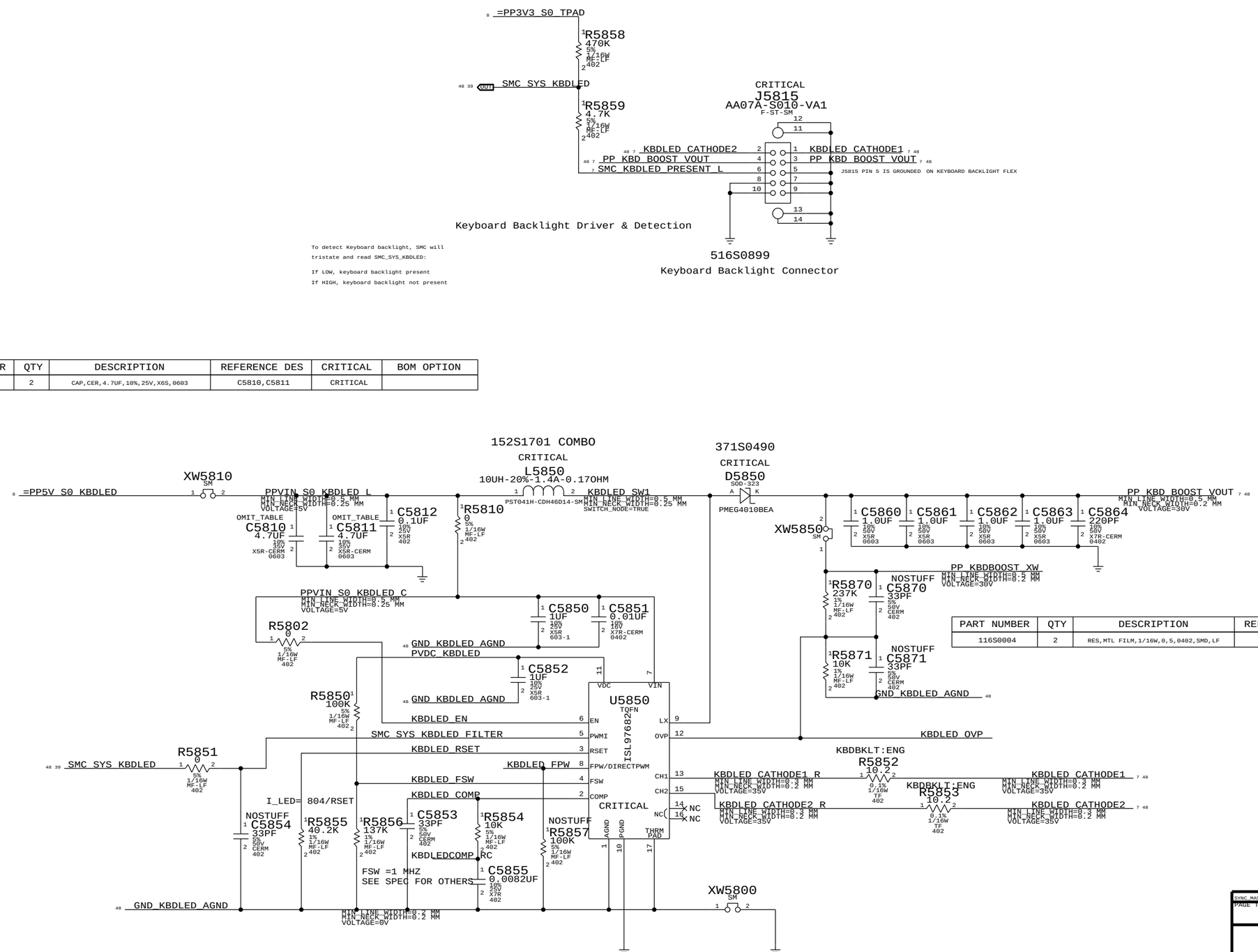
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 57 OF 132

SHEET 47 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	2	CAP,CER,4.7UF,10%,25V,X6S,0603	C5810,C5811	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,1/16W,0,5,0402,SMD,LF	R5852,R5853	CRITICAL	KBDBKLT:PROD

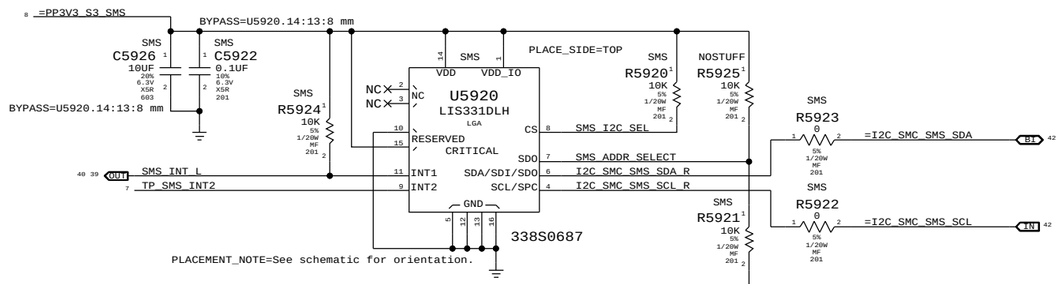
SYNC_MASTER=D2_MLB_KEPLER SYNC_DATE=12/08/2011

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 58 OF 132
SHEET 48 OF 80

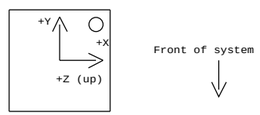
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



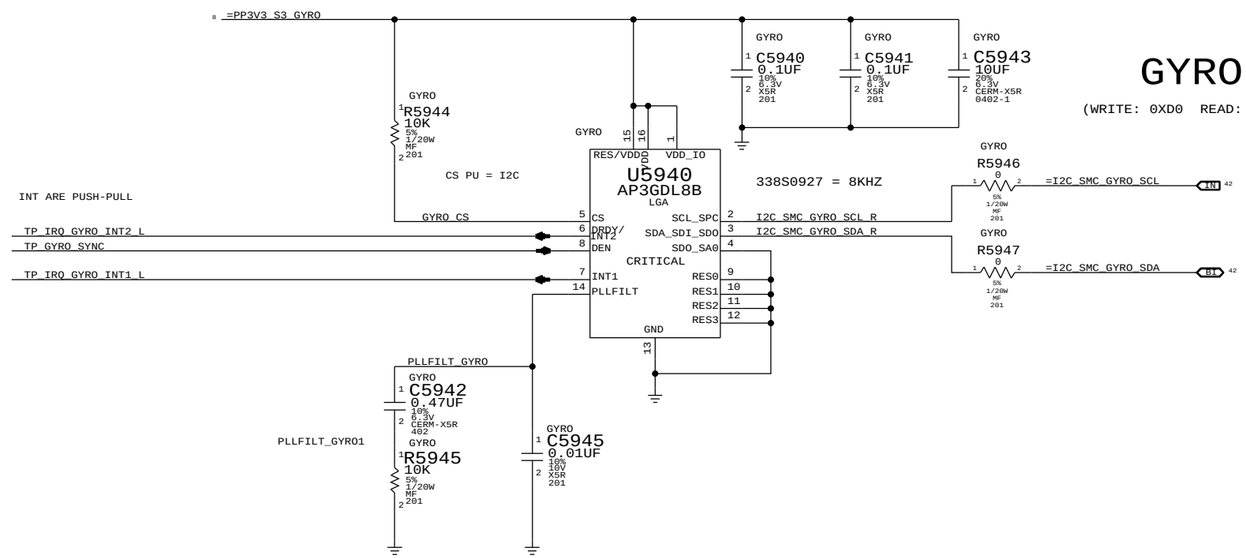
SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when placed on top-side (view top):



Circle indicates pin 1 location when placed in correct orientation



GYRO

(WRITE: 0XD0 READ: 0XD1)

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE
DIGITAL ACCELEROMETER & GYRO

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

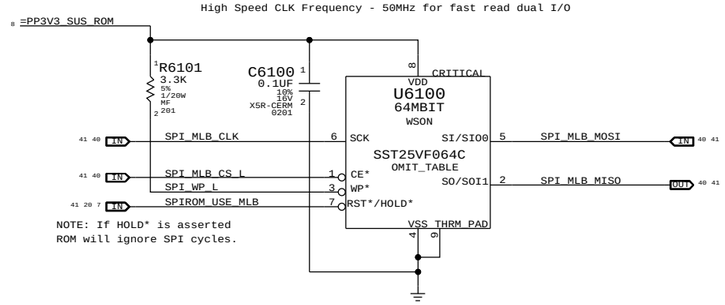
BRANCH <BRANCH>

PAGE 59 OF 132

SHEET 49 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DUAL I/O MODE (MODE 0 & 3) SUPPORTED
High Speed CLK Frequency - 50MHz for fast read dual I/O



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles.

SYNC MASTER=J13 MLB SYNC DATE=01/20/2012

PAGE TITLE
SPI ROM

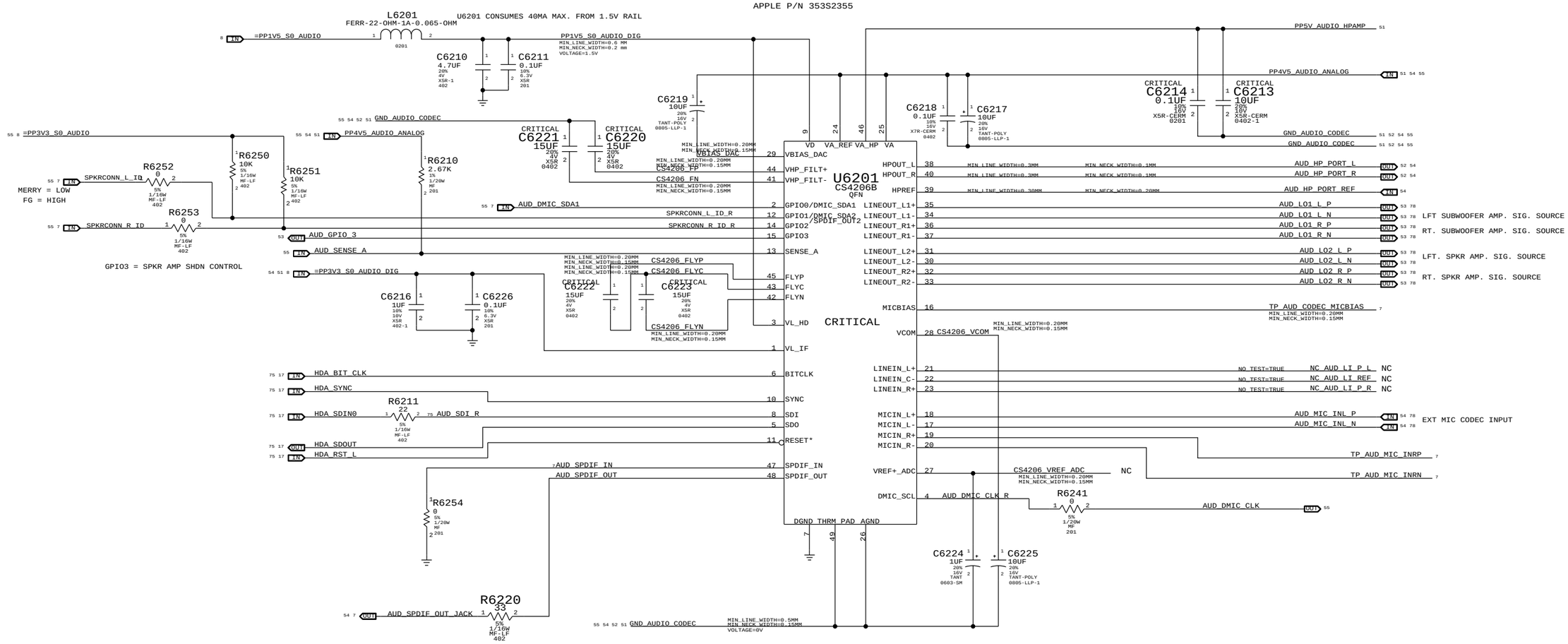
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 61 OF 132
SHEET 50 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

AUDIO CODEC

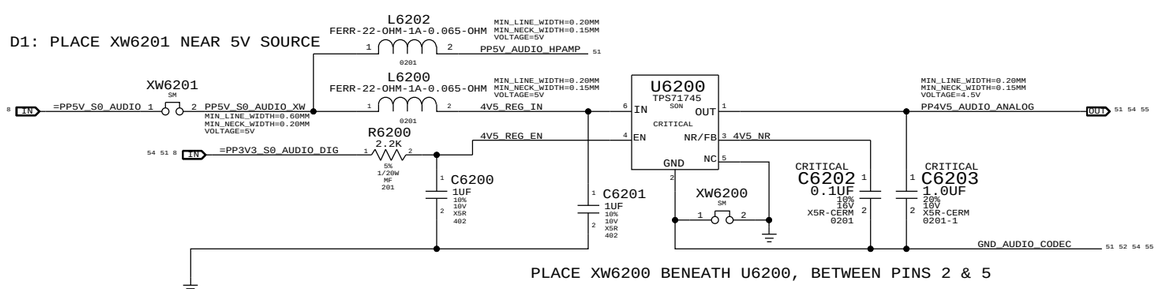
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

D1: PLACE XW6201 NEAR 5V SOURCE



PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC MASTER=D1_AUDIO SYNC DATE=06/06/2012

PAGE TITLE

AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

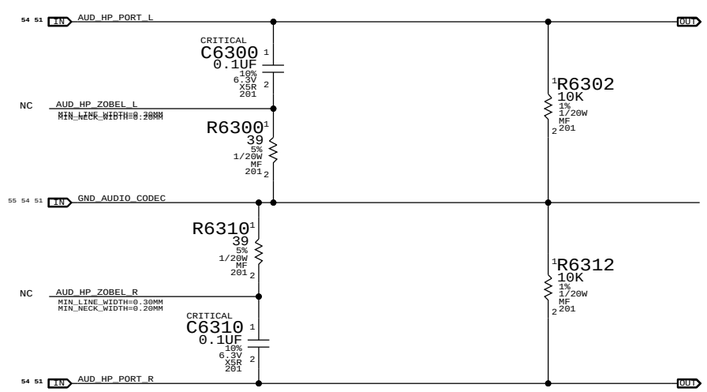
BRANCH <BRANCH>

PAGE 62 OF 132

SHEET 51 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

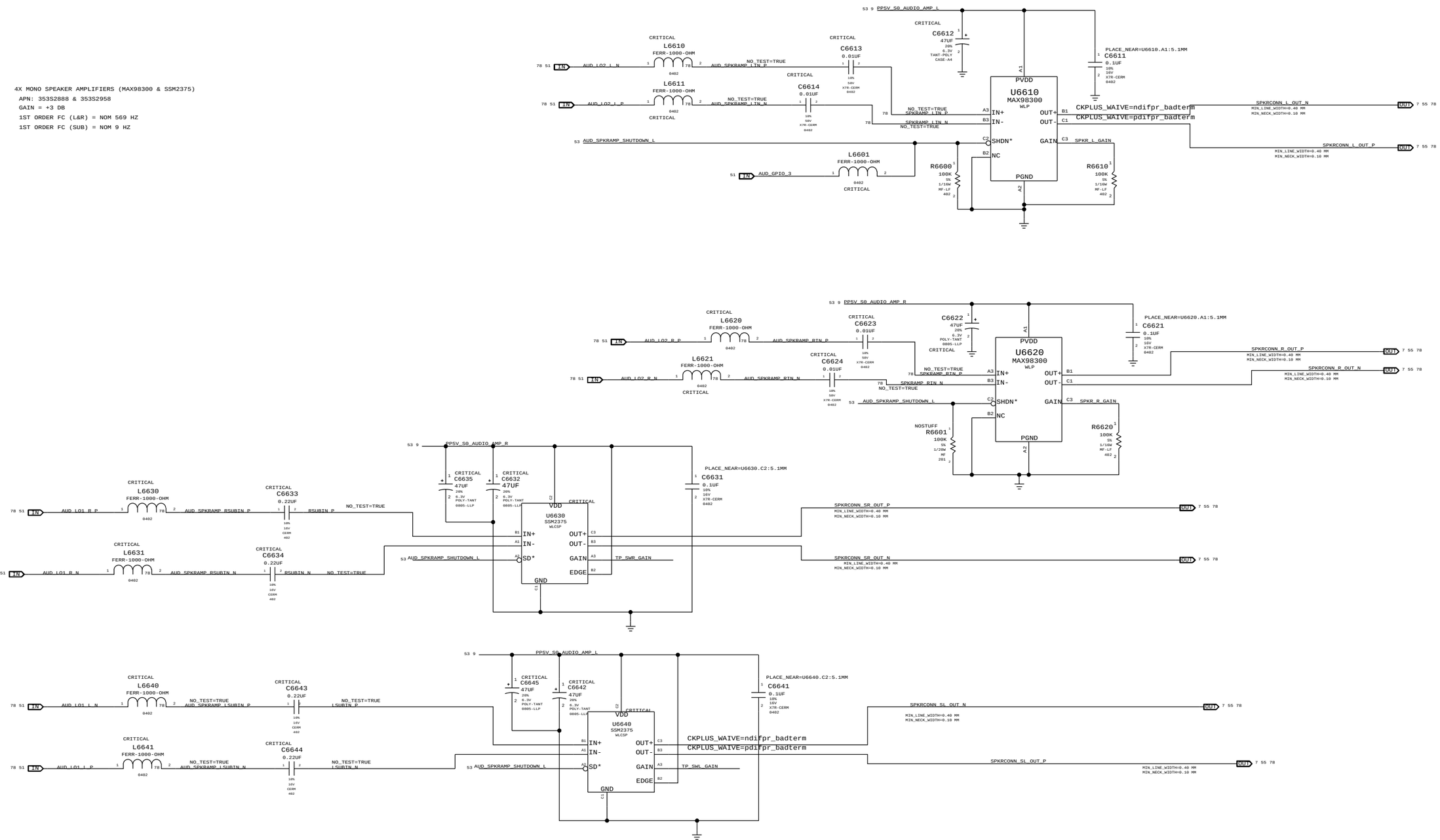
BRANCH <BRANCH>

PAGE 63 OF 132

SHEET 52 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ



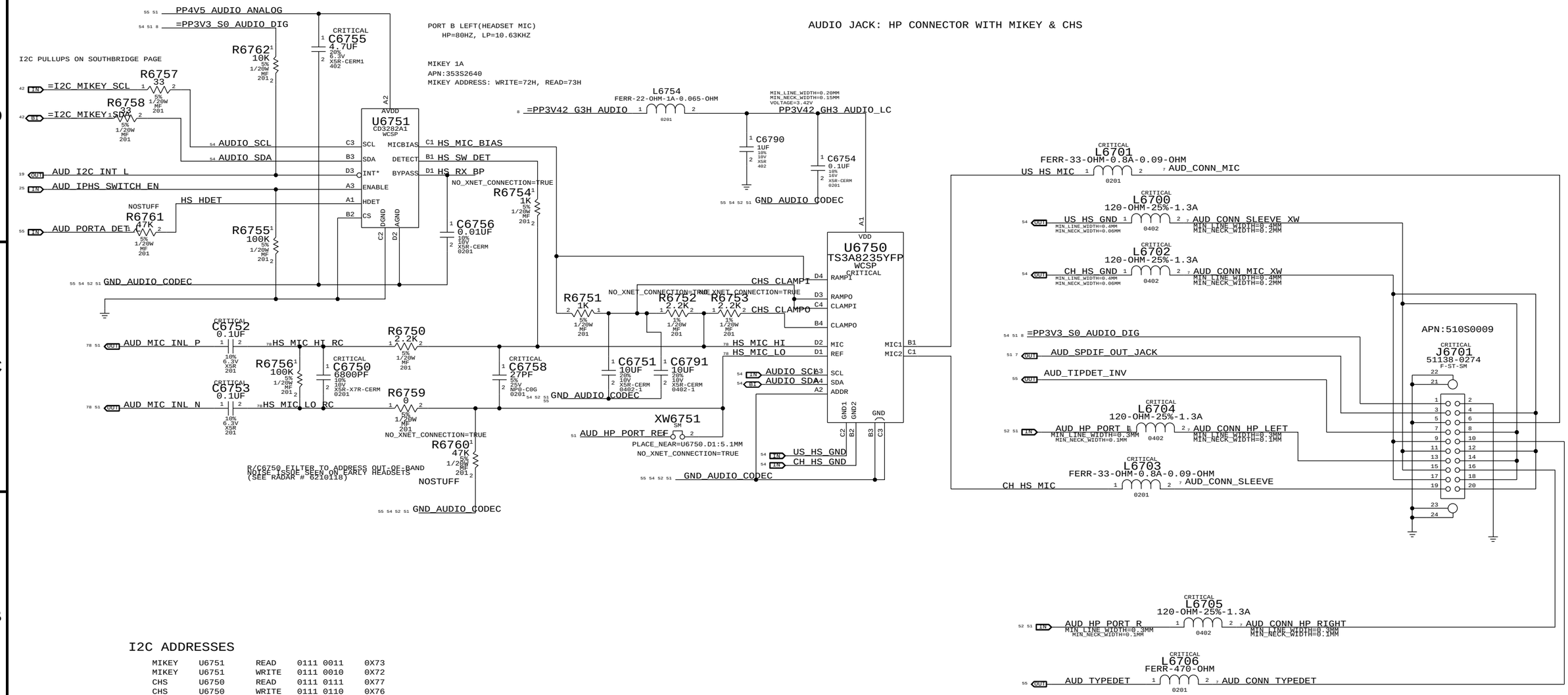
SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 66 OF 132
SHEET 53 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



I2C ADDRESSES

MIKEY	U6751	READ	0111 0011	0X73
MIKEY	U6751	WRITE	0111 0010	0X72
CHS	U6750	READ	0111 0111	0X77
CHS	U6750	WRITE	0111 0110	0X76

SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2013

PAGE TITLE

AUDIO: JACK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 67 OF 132

SHEET 54 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (B)
TWEETERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (A)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
DMIC 1	0X06 (6)	0X0E (0,E)	3V3	N/A
DMIC2	0X05 (5)	0X12 (12,C)	3V3	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,8,LEFT)	MIKEY	MIKEY

SYSTEM INT AND GPIO LINES

FUNCTION	INT	GPIO
MIKEY ENABLE		SATA4GP/GPIO 16
MIKEY INTERRUPT	PIRQ H	GPIO 5
PERIPHERAL DETECT	PIRQ F	GPIO 3

2-MIC CONNECTOR

MIN_LINE_WIDTH=0.40MM
MIN_NECK_WIDTH=0.15MM
VOLTAGE=3.3V

55 51 8 =PP3V3_S0_AUDIO — R6885 0 5% 1/16W MF-LF 402 — 7 CON_DMIC_PWR
51 7 OUT AUD_DMIC_SDA1 — R6884 0 5% 1/16W MF-LF 402 — 7 CON_DMIC_SDA1
51 OUT AUD_DMIC_CLK — R6883 0 5% 1/16W MF-LF 402 — 7 CON_DMIC_CLK

CRITICAL
J6801
FF14A-6C-R11DL-B-3H
F-RT-SM
NC 7
NC 8

SPEAKER CONNECTOR

HP=80HZ

APN: 518S0627

CRITICAL
J6802
78171-6006
M-RT-SM

78 53 7 IN SPKRCONN_L_OUT_P
78 53 7 IN SPKRCONN_L_OUT_N
55 51 7 OUT SPKRCONN_L_ID
78 53 7 IN SPKRCONN_SL_OUT_P
78 53 7 IN SPKRCONN_SL_OUT_N

CRITICAL
J6803
78171-6006
M-RT-SM

78 53 7 IN SPKRCONN_R_OUT_P
78 53 7 IN SPKRCONN_R_OUT_N
55 51 7 OUT SPKRCONN_R_ID
78 53 7 IN SPKRCONN_SR_OUT_P
78 53 7 IN SPKRCONN_SR_OUT_N

PORT B DETECT(SPDIF DELEGATE)

PORT A DETECT (HEADPHONES)

55 51 OUT AUD_SENSE_A

R6896 20.0K 1% 1/16W MF-LF 402 — AUD_PORTA_DET_L 54
R6895 39.2K 1% 1/16W MF-LF 402 — AUD_PORTB_DET_L NC

Q6897 SSM6N15AFE SOT563
Q6897 SSM6N15AFE SOT563

55 IN AUD_OUTJACK_INSERT_L

AUD_TYPEDET_OD OUT 55

55 54 52 51 GND_AUDIO_CODEC — R6802 100K 5% 1/20W MF 201

PP4V5_AUDIO_ANALOG
R6801 150K 1% 1/20W MF 201
AUD_TYPEDET IN 54

Q6800 DMC2400UV SOT563 P-CHN

55 54 51 PP4V5_AUDIO_ANALOG — R6803 100K 5% 1/20W MF 201 — AUD_TYPEDET_OD_INV

PP4V5_AUDIO_ANALOG 51 54 55

C6800 0.1UF 10% 6.3V X5R 201 — PLACE_NEAR=Q6800.4:5.1MM

Q6800 DMC2400UV SOT563 — AUD_TYPEDET_OD IN 55

GND_AUDIO_CODEC 51 52 54 55

55 8 =PP5V_S4_AUDIO

SPEAKERID R6810 100K 1% 1/16W MF-LF 402
SPEAKERID R6811 100K 1% 1/16W MF-LF 402

55 51 7 IN SPKRCONN_L_ID
SPKRCONN_R_ID IN 7 51 55

SPEAKERID R6812 100K 1% 1/16W MF-LF 402
SPEAKERID R6813 100K 1% 1/16W MF-LF 402

SPEAKERID R6816 100K 1% 1/16W MF-LF 402

55 8 =PP5V_S4_AUDIO

SPEAKERID C6810 0.1UF 10% 6.3V X5R 201

SPEAKERID CRITICAL U6800 MCP6541T SC70-5

MCP6514_POS 3
MCP6514_NEG 4
MCP6514_OUT 1

SPEAKERID L6802 FERR-1000-OHM 0402

SPKR_MATCH_DRV_R — SPEAKERID R6820 33 5% 1/10W MF-LF 402 — SPKR_MATCH_DRV

PORT C DETECT(SPEAKER MISMATCH)

55 51 OUT AUD_SENSE_A

SPEAKERID R6894 10K 1% 1/16W MF-LF 402

NC AUD_PORTC_DET_L

SPEAKERID Q6896 SSM6N15AFE SOT563

55 54 52 51 GND_AUDIO_CODEC

55 51 8 =PP3V3_S0_AUDIO

R6867 0 5% 1/10W MF-LF 402 — AUD_IP_PERIPHERAL_DET OUT 19

EXTRACTION NOTIFICATION

R6865 47K 5% 1/20W MF 201

R6866 475K 1% 1/20W MF 201

AUD_TIPDET_FET1

AUD_OUTJACK_INSERT_L OUT 55

APN:376S0613

Q6803 SSM6N15AFE SOT563

Q6803 SSM6N15AFE SOT563

54 IN AUD_TIPDET_INV — R6892 1.5K 1% 1/16W MF-LF 402 — AUD_TIPDET_INV_R

C6860 1UF 10% 25V X5R 402

CRITICAL
L6801
FERR-33-OHM-0.8A-0.09-OHM
0201

AUD_TIPDET_FET2

C6891 1UF 10% 25V X5R 402

55 54 52 51 GND_AUDIO_CODEC

55 8 =PP5V_S4_AUDIO

SPEAKERID R6814 274K 1% 1/10W MF-LF 402
SPEAKERID R6815 90.9K 1% 1/10W MF-LF 402

SPEAKERID C6811 4.7UF 10% 10V X5R-CERM 0402

SPEAKERID R6817 45.3K 1% 1/10W MF-LF 402

AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_J1_TYPEDET_R	1	1	0
AUD_J1_TIPDET_R	0	1	1
AUD_OUTJACK_INSERT_L	1	0	0
AUD_SENSE_A	1	20K/2.67K RDIV	39.2K/2.67K RDIV

NOM R6892-C6860 FC = 106Hz
SSM6N15FE Vth = 0.8V to 1.5V
SSM6N15FE IGSS = +/-1uA
FLEX-SIDE RPULLDOWN = 100k (TB 49.9k in REV 3)

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S3452	353S1286		U6800	MAXIM ALT TO MICROCHIP
376S0975	376S1081		Q6800	TOSHIBA ALT TO DIODES

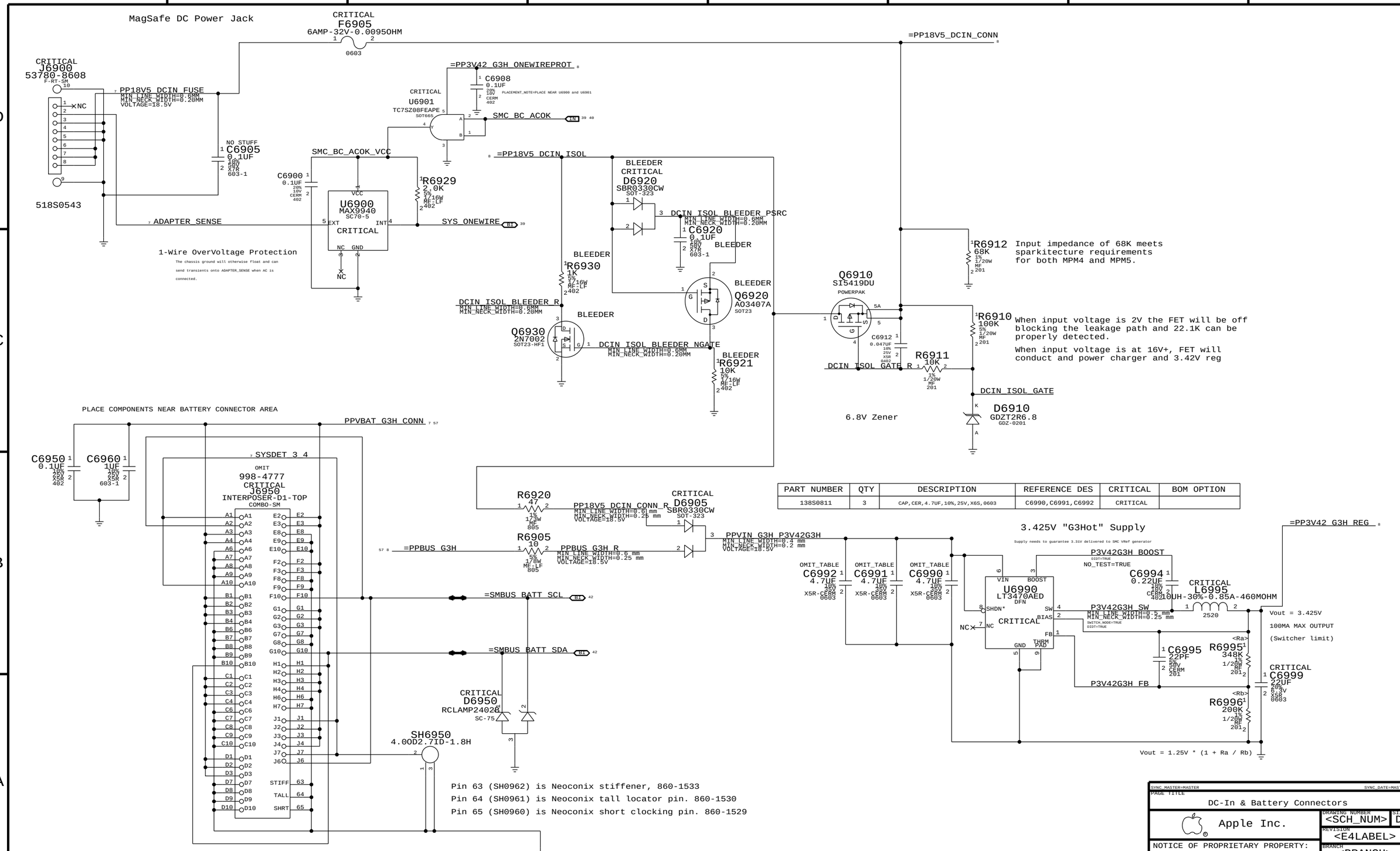
SYNC_MASTER=D1_AUDIO SYNC_DATE=06/06/2012

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 68 OF 132
SHEET 55 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	3	CAP,CER,4.7UF,10%,25V,X6S,0603	C6990,C6991,C6992	CRITICAL	

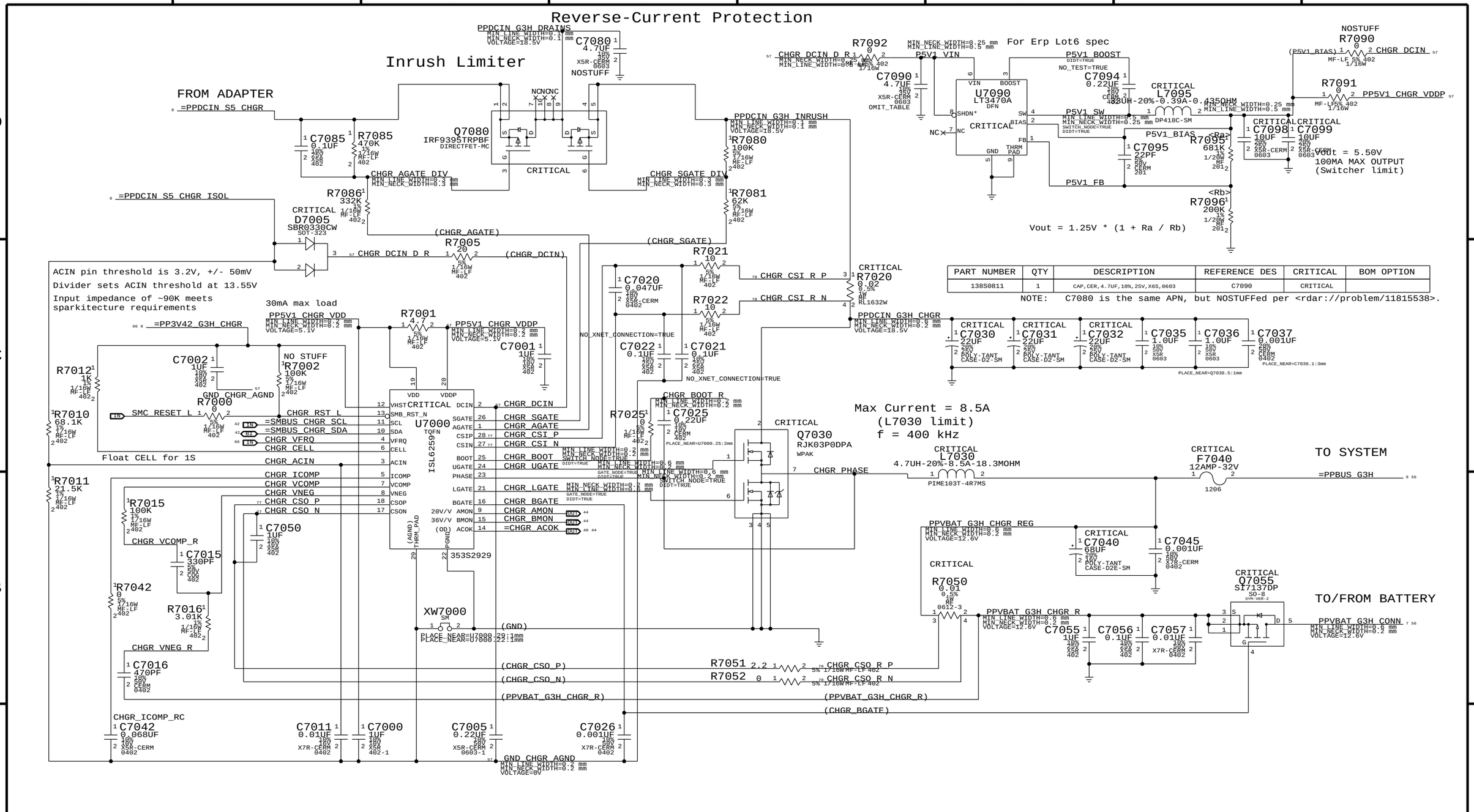
SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 69 OF 132
SHEET 56 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X6S,0603	C7090	CRITICAL	

NOTE: C7080 is the same APN, but NOSTUFFed per <rdar://problem/11815538>.

SYNC MASTER=MASTER SYNC DATE=MASTER

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

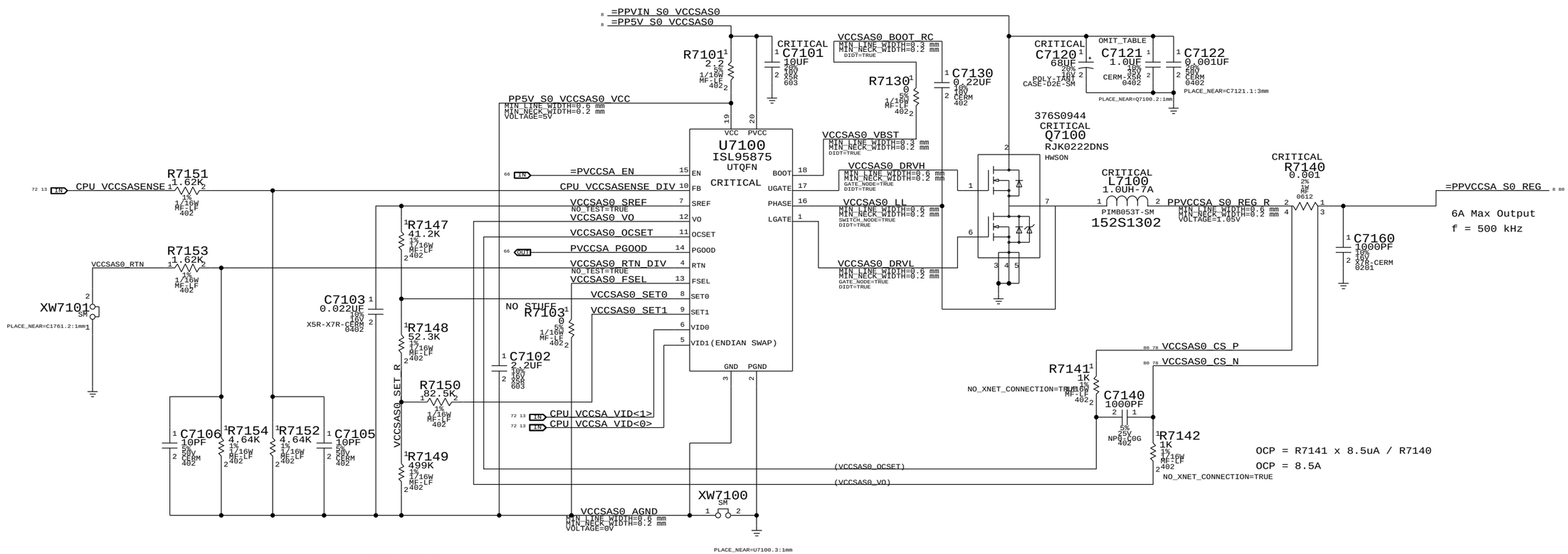
PAGE: 70 OF 132

SHEET: 57 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

System Agent Power Supply

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7121	CRITICAL	



INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

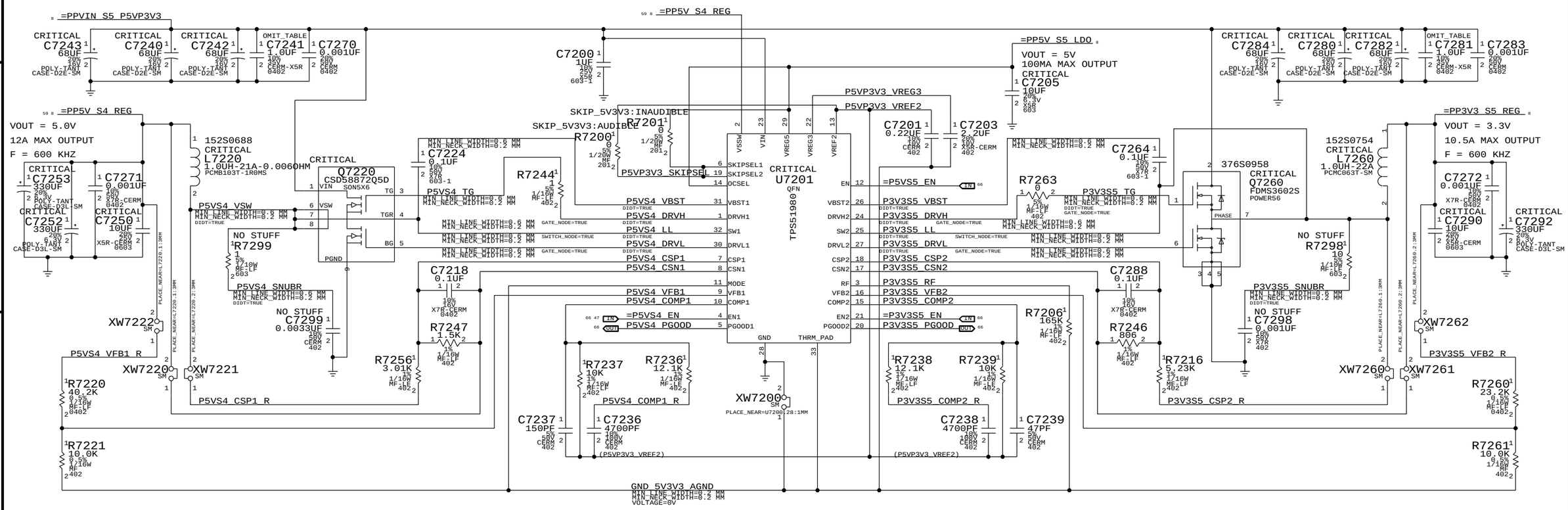
BRANCH: <BRANCH>

PAGE: 71 OF 132

SHEET: 58 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7241,C7281	CRITICAL	



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

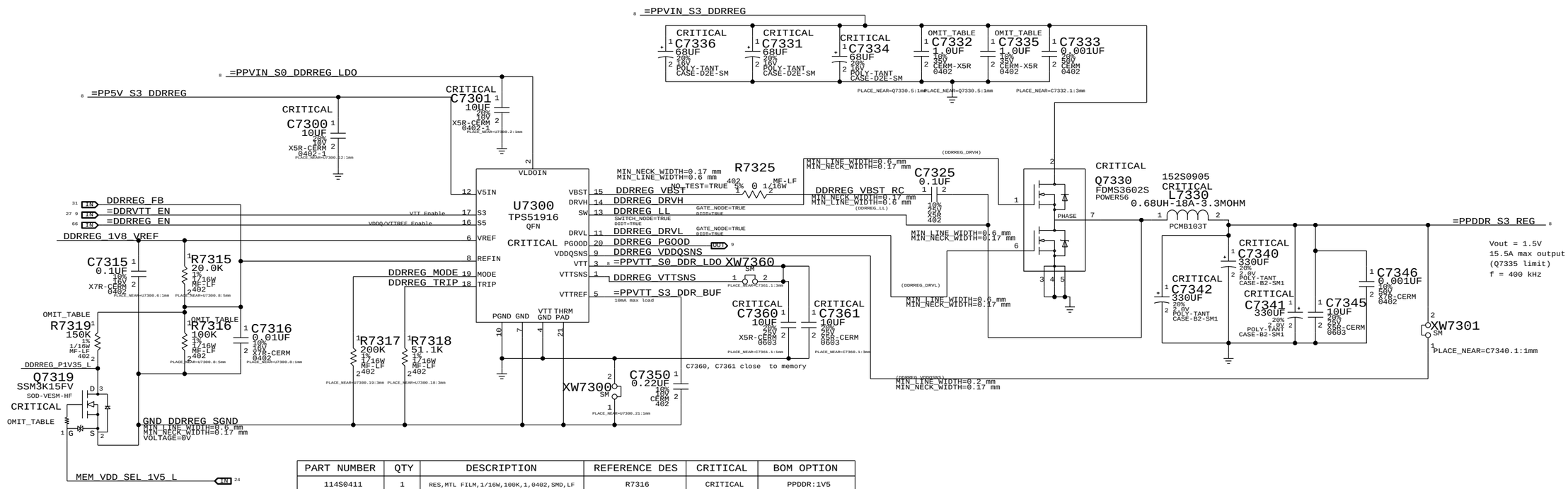
PAGE 72 OF 132

SHEET 59 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	2	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7332,C7335	CRITICAL	

DDR3 (1V5R1V35 S3) REGULATOR



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V5
114S0391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7316	CRITICAL	PPDDR:1V35
376S0612	1	MOSFET,N-CH,30V,100MA,7.0OHM,SOT-723,HF	Q7319	CRITICAL	PPDDR:1V5
114S0428	1	RES, MTL FILM,1/16W,150k,0402,SMD,LF	R7319	CRITICAL	PPDDR:1V5

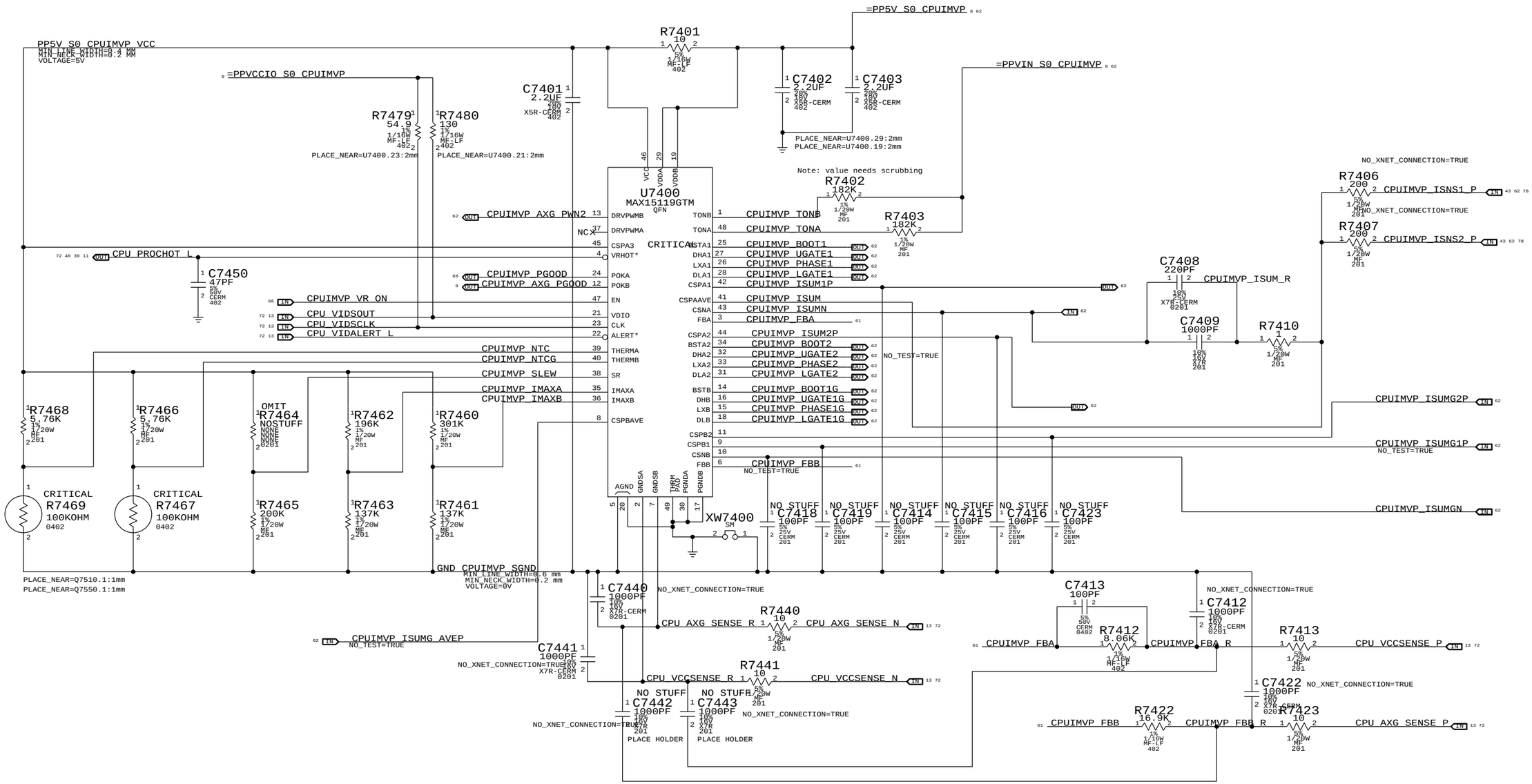
SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 73 OF 132
SHEET 60 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

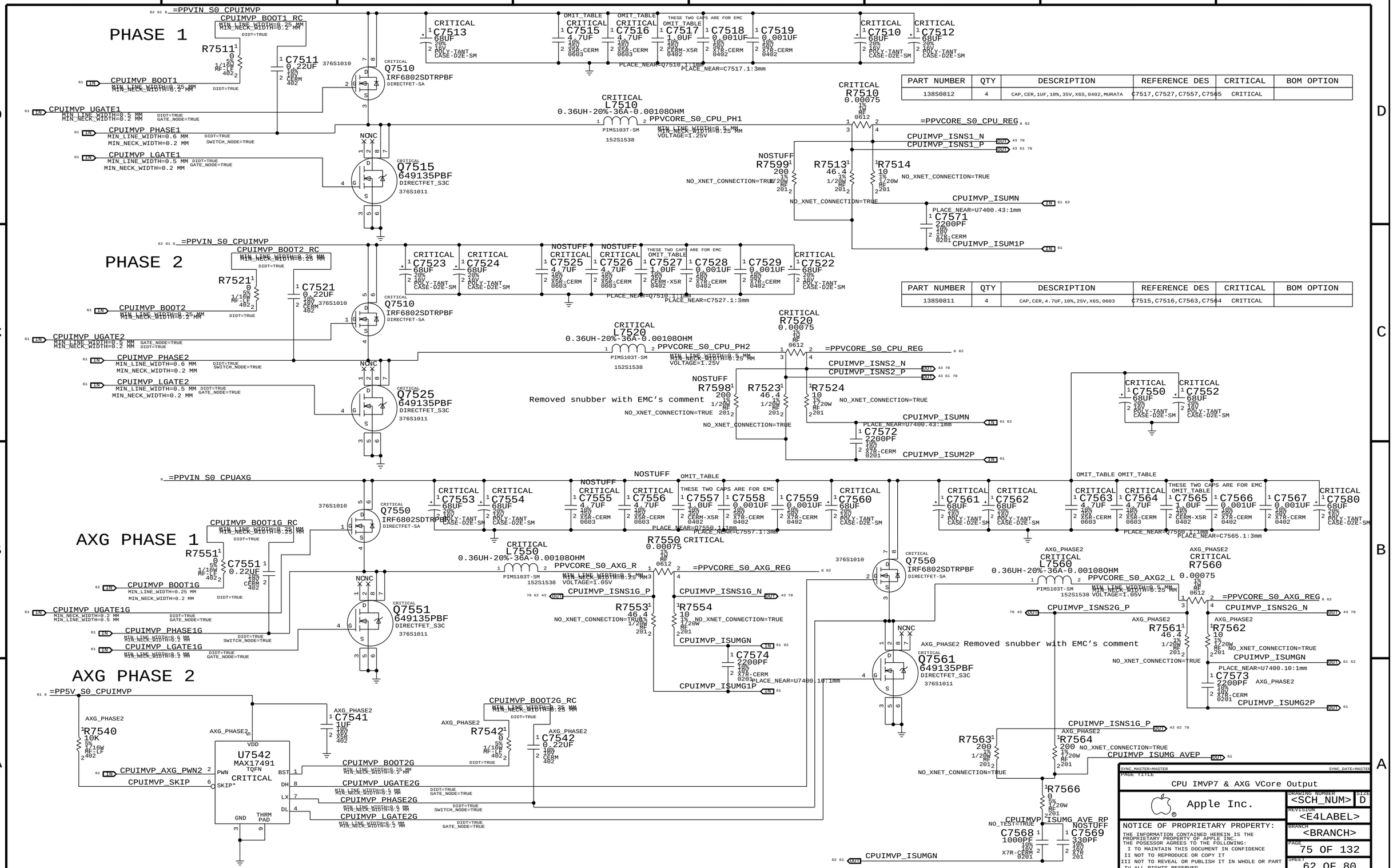
BRANCH <BRANCH>

PAGE 74 OF 132

SHEET 61 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

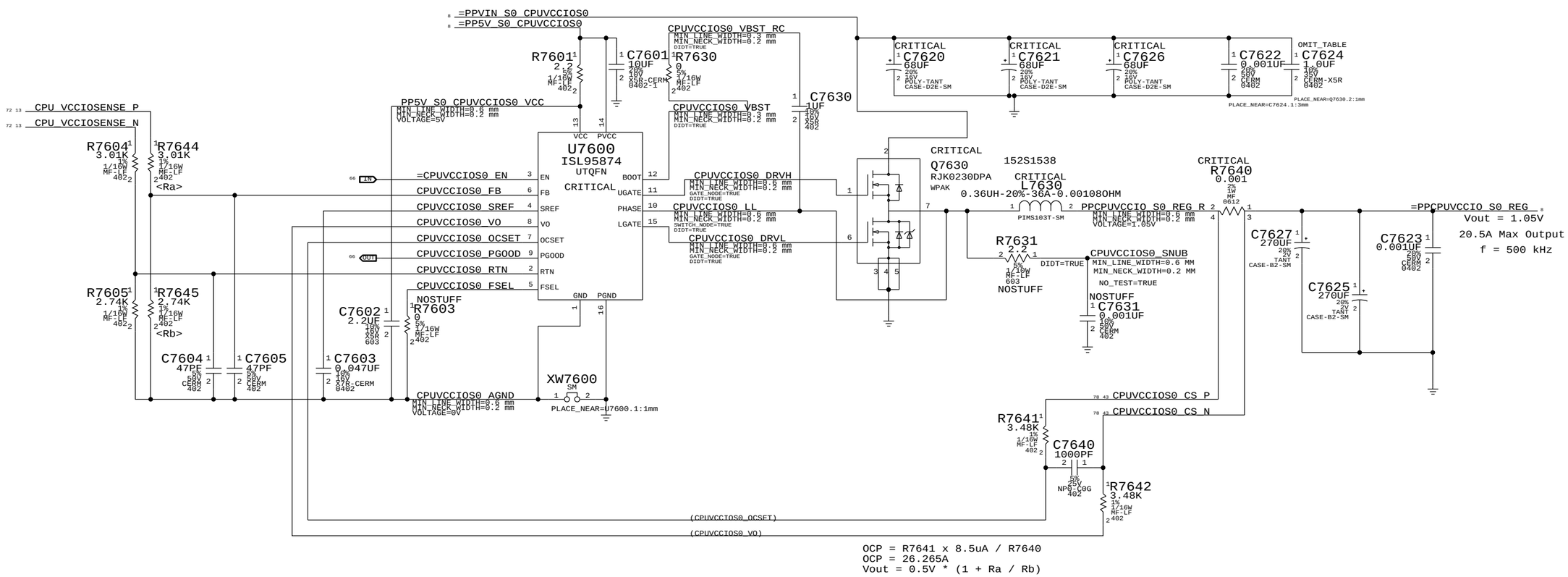


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	4	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7517,C7527,C7557,C7565	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	4	CAP,CER,4.7UF,10%,25V,X6S,0603	C7515,C7516,C7563,C7564	CRITICAL	

CPU VCCIO (1.05V S0) Regulator

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0812	1	CAP,CER,1UF,10%,35V,X6S,0402,MURATA	C7624	CRITICAL	



OCP = R7641 x 8.5uA / R7640
OCP = 26.265A
Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=MASTER SYNC_DATE=MASTER

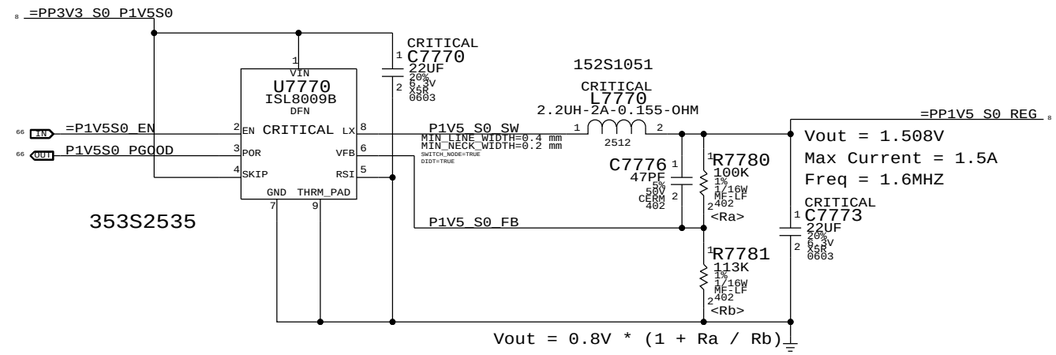
PAGE TITLE
CPUVCCIO (1.05V) Power Supply

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 76 OF 132
SHEET 63 OF 80

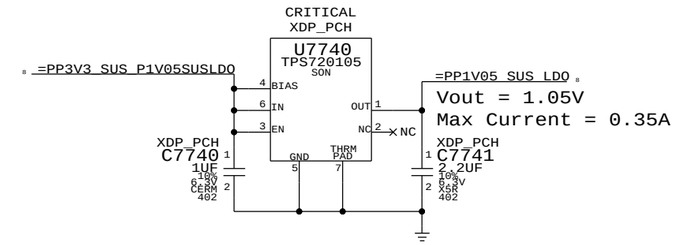
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

1.5V S0 Switcher



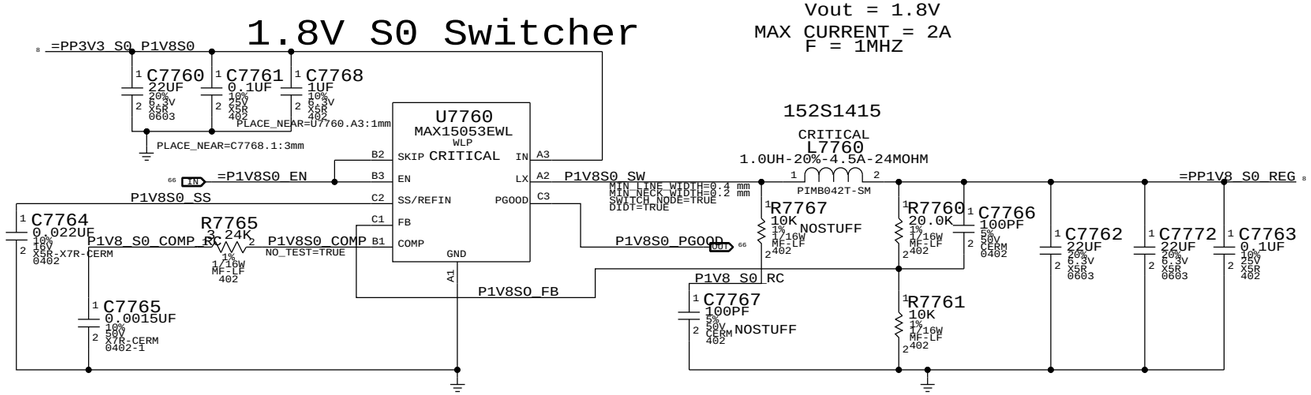
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

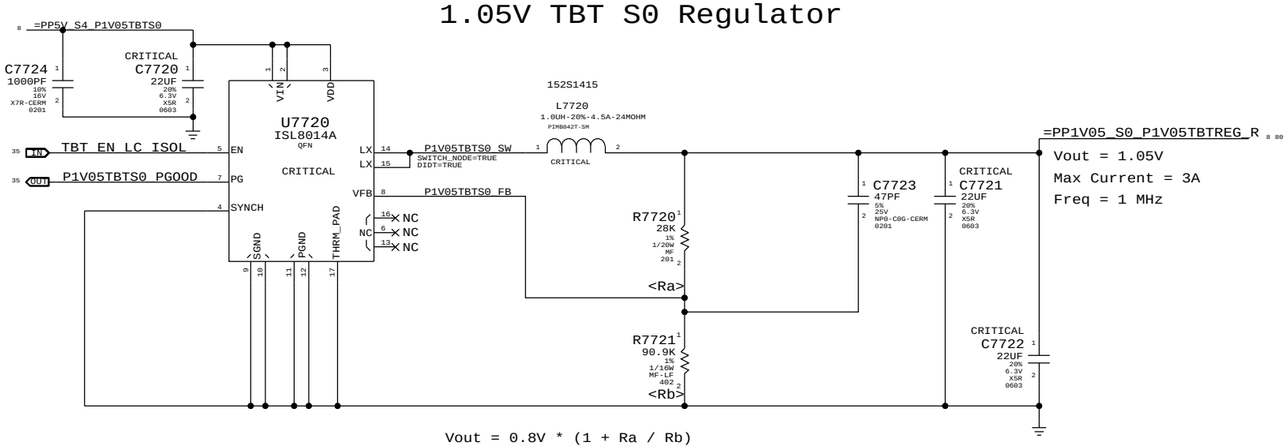


1.8V S0 Switcher

Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.05V TBT S0 Regulator



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Misc Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

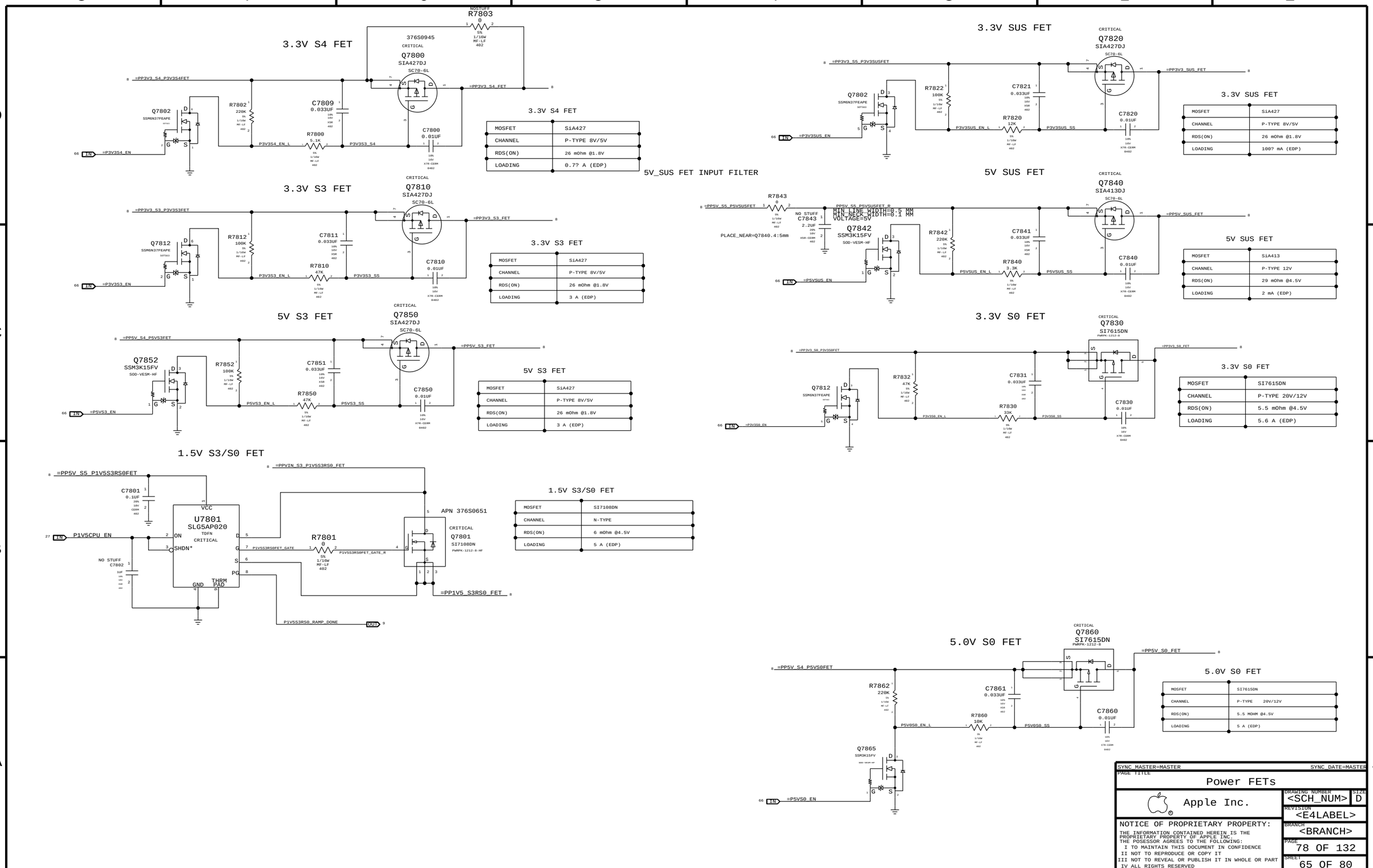
REVISION <E4LABEL>

BRANCH <BRANCH>

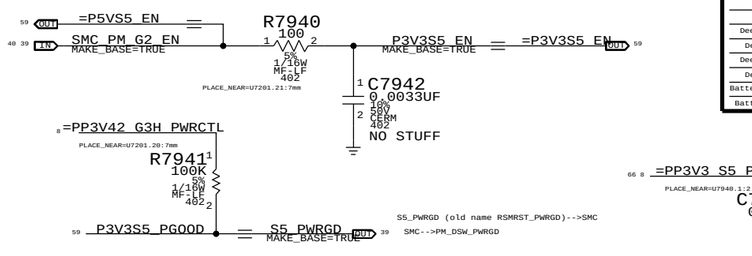
PAGE 77 OF 132

SHEET 64 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


3.3V S4 FET
3.3V S3 FET
5V S3 FET
1.5V S3/S0 FET
3.3V SUS FET
5V SUS FET
3.3V S0 FET
5.0V S0 FET
5V_SUS FET INPUT FILTER
Q7800 SIA427DJ
Q7810 SIA427DJ
Q7850 SIA427DJ
Q7820 SIA427DJ
Q7840 SIA413DJ
Q7830 SI7615DN
Q7860 SI7615DN
U7801 SLG5AP020
Q7801 SI7108DN
APN 376S0651
R7803 0
R7801 0
=PP3V3_S4_P3V3S4FET
=PP3V3_S4_FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S3_FET
=PPV5_S4_P5V5S3FET
=PPV5_S3_FET
=PP3V3_S5_P3V3SUSFET
=PP3V3_SUS_FET
=PP3V3_S0_P3V3S0FET
=PP3V3_S0_FET
=PP5V_S4_P5VS0FET
=PP5V_S0_FET
=PP5V_S5_P5VSUSFET
=PP5V_SUS_FET
=PP5V_S5_P1V5S3RS0FET
=PPVIN_S3_P1V5S3RS0_FET
=PP1V5_S3RS0_FET
P1V5CPU_EN
P1V5S3RS0_RAMP_DONE
PP5V_S5_P5VSUSFET_R
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=5V
PLACE_NEAR=Q7840.4:5mm
NO STUFF
CRITICAL
MOSFET
CHANNEL
RDS(ON)
LOADING
SiA427
P-TYPE 8V/5V
26 mOhm @1.8V
0.7? A (EDP)
3 A (EDP)
SiA413
P-TYPE 12V
29 mOhm @4.5V
2 mA (EDP)
SI7615DN
P-TYPE 20V/12V
5.5 mOhm @4.5V
5.6 A (EDP)
N-TYPE
6 mOhm @4.5V
5 A (EDP)
100? mA (EDP)
5.5 MOHM @4.5V
Apple Inc.
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED
SYNC_MASTER=MASTER
SYNC_DATE=MASTER
PAGE TITLE
Power FETs
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
78 OF 132
SHEET
65 OF 80

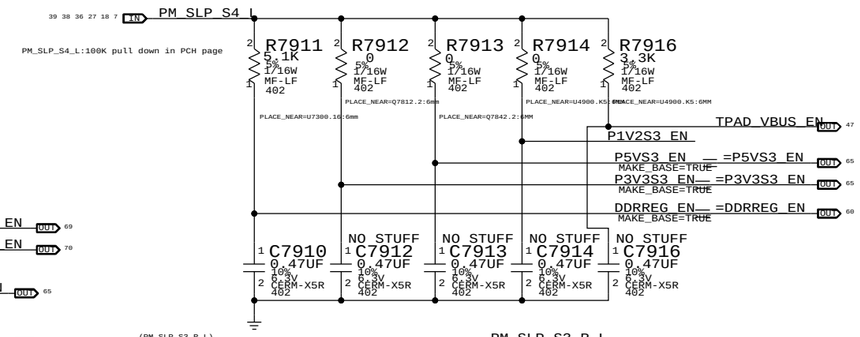
S5 Rail Enables & PGOOD



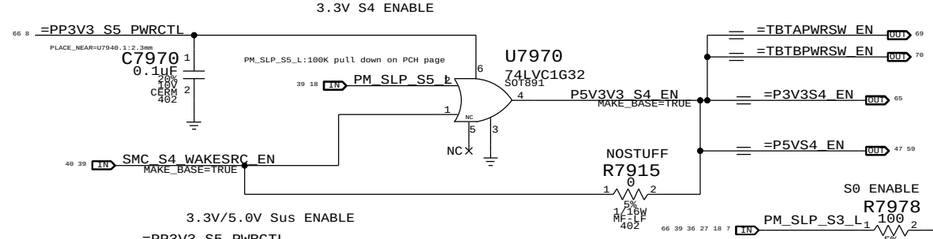
Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

1.2V, 5V, 3.3V, DDR S3 ENABLE

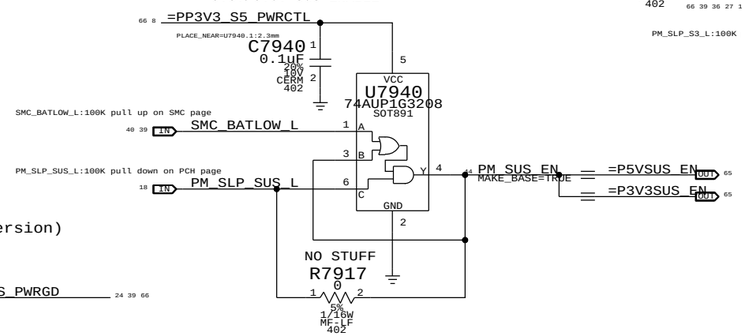


3.3V S4 ENABLE

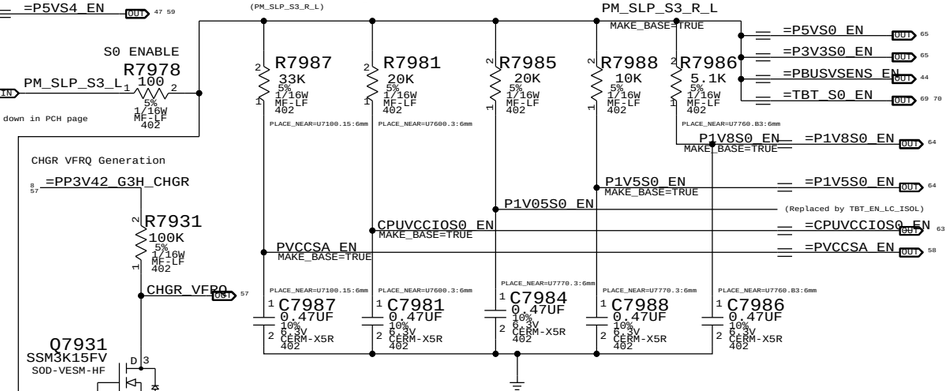


CPUVCORE ENABLE

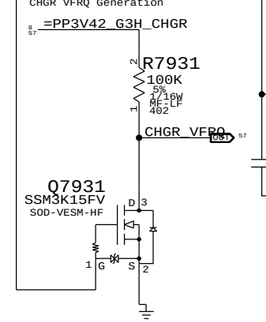
3.3V/5.0V Sus ENABLE



S0 ENABLE

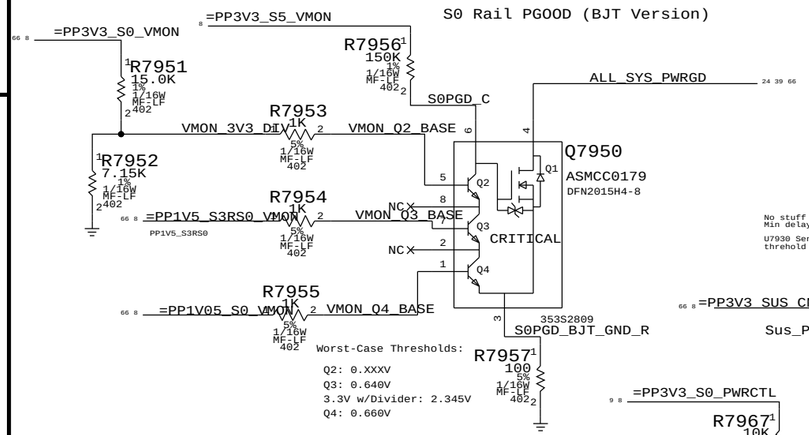


CHGR VFRQ Generation

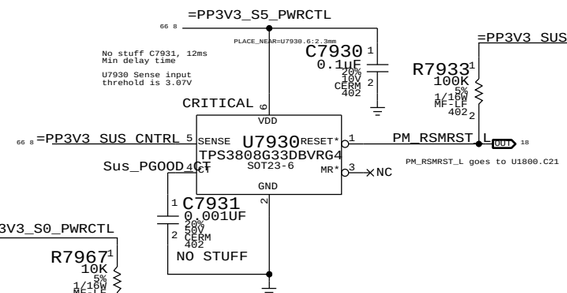


VFRQ Low: Fix Frequency
VFRQ High: Variable Frequency

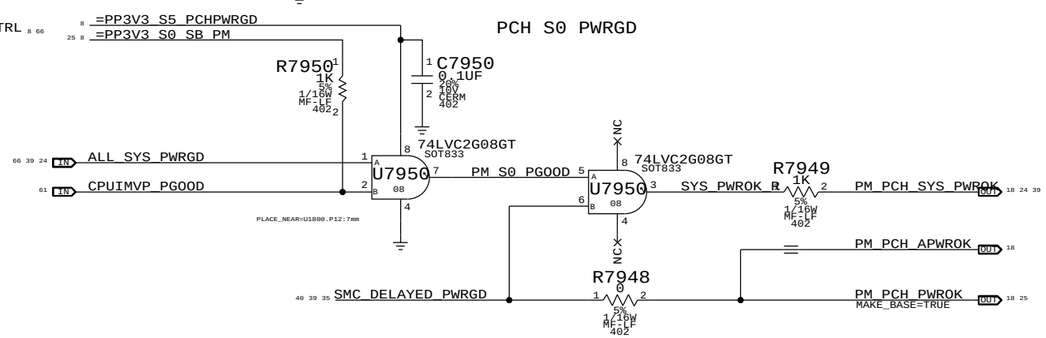
S0 Rail PGOOD (BJT Version)



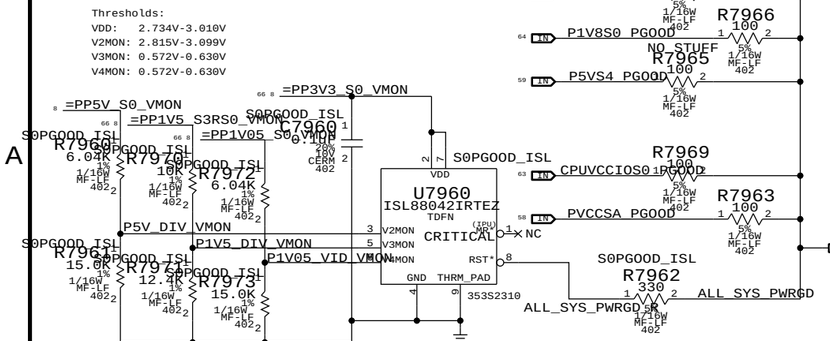
3.3V SUS Detect



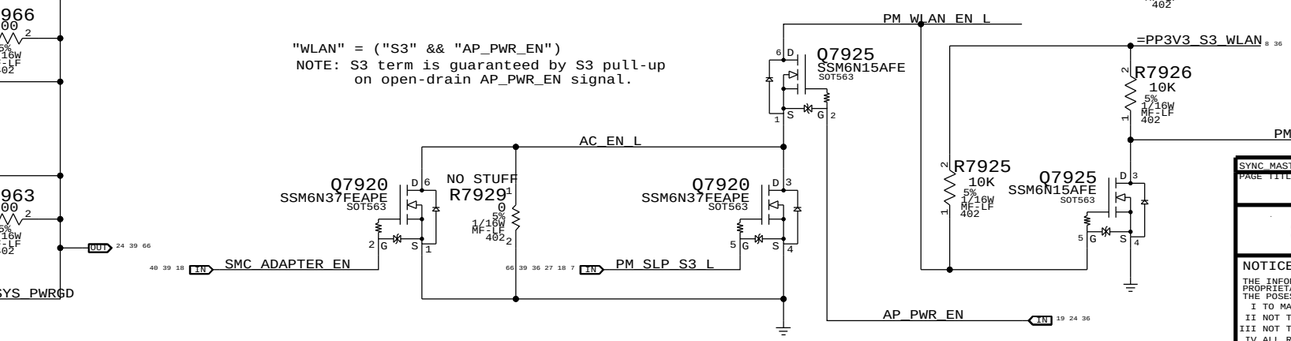
PCH S0 PWRGD



S0 Rail PGOOD Circuitry
(ISL Version in development)



"WLAN" = ("S3" && "AP_PWR_EN")
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



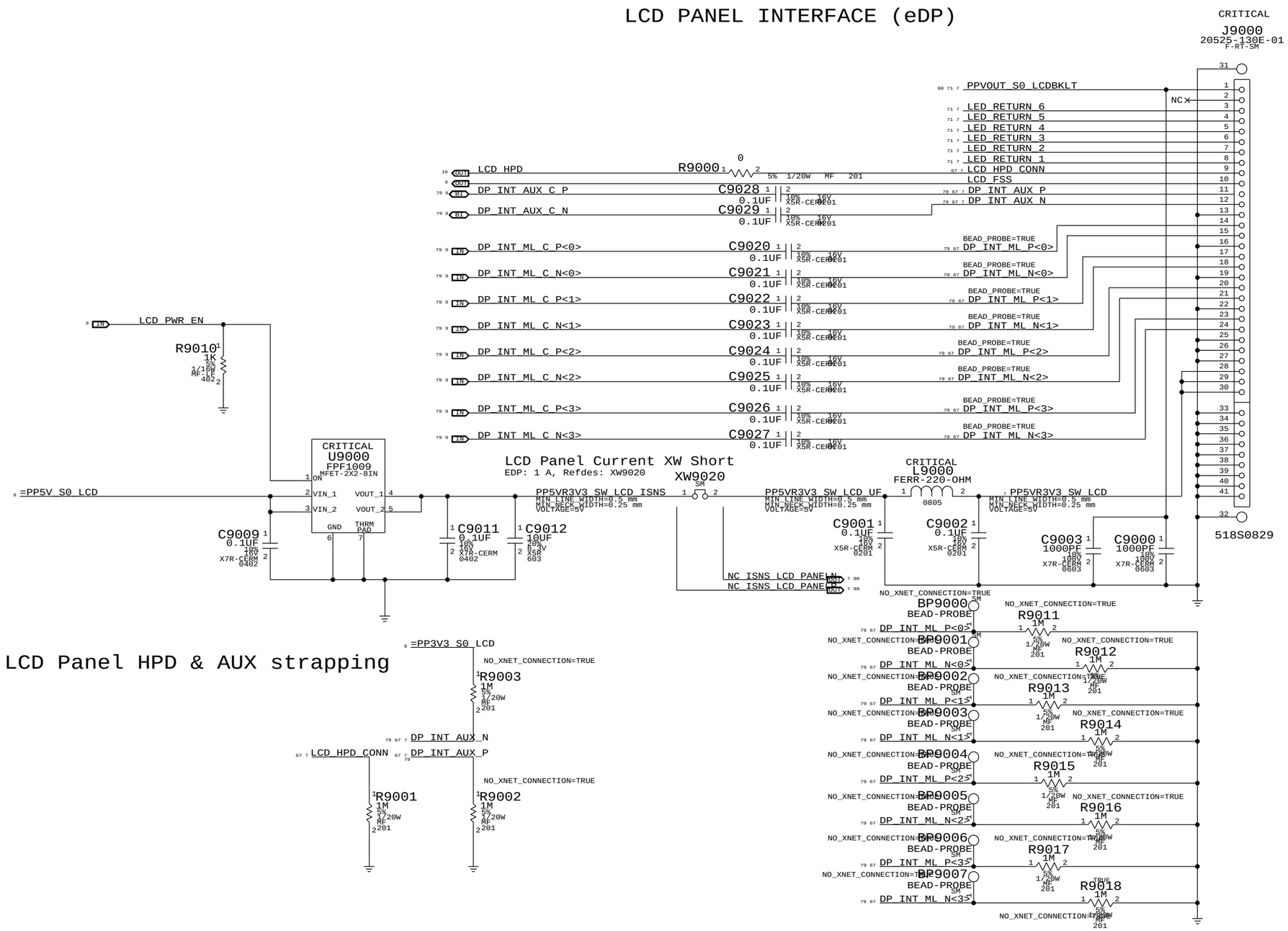
SYNC MASTER=MASTER SYNC DATE=MASTER
PAGE TITLE
Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 79 OF 132
SHEET 66 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LCD PANEL INTERFACE (eDP)



SYNC_MASTER=D1_SENSORS SYNC_DATE=07/11/2012

PAGE TITLE

eDP Display Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

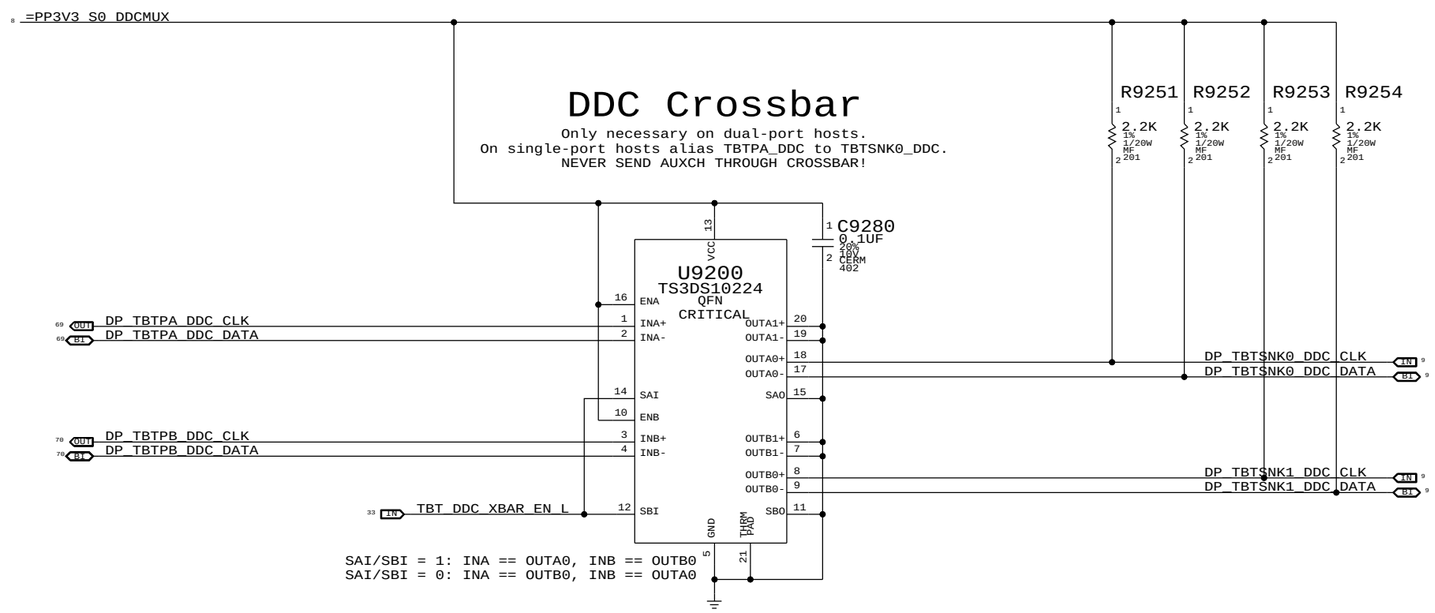
BRANCH <BRANCH>

PAGE 90 OF 132

SHEET 67 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
DDC Crossbar

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 92 OF 132

SHEET 68 OF 80

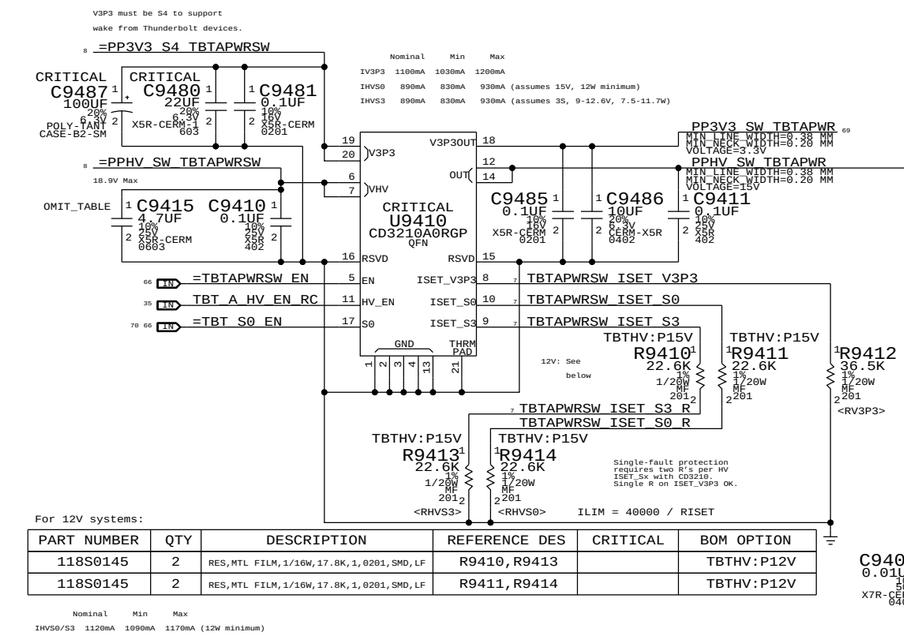
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9415	CRITICAL	

3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

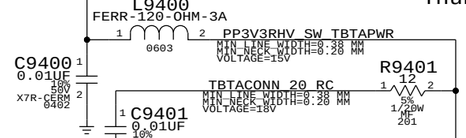
	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 35, 9-12.6V, 7.5-11.7W)

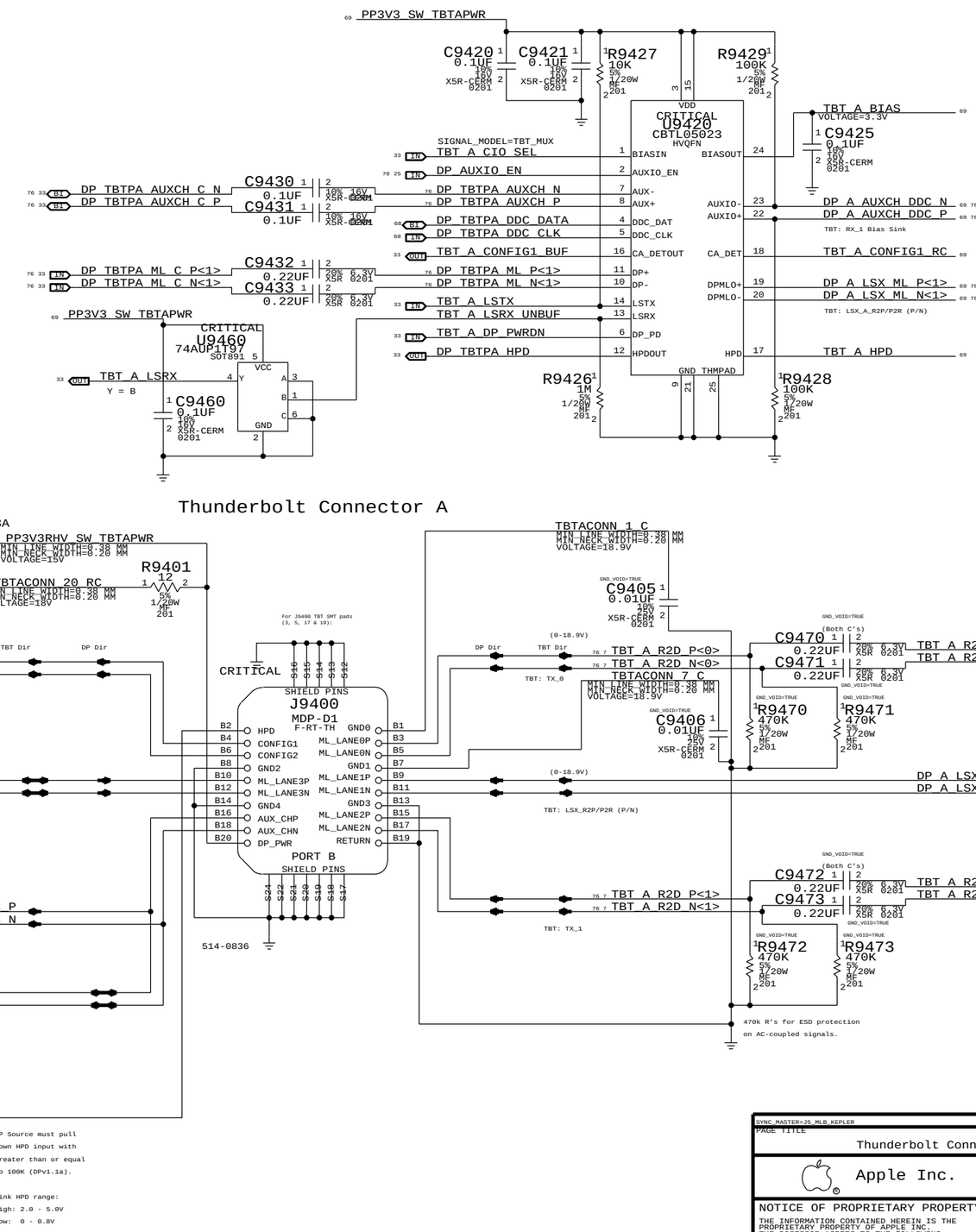


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9410,R9413		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)





SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2013

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 94 OF 132

SHEET: 69 OF 80

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0811	1	CAP,CER,4.7UF,10%,25V,X5R,0603,MURATA	C9615	CRITICAL	

3.3V/HV Power MUX

V3P3 must be S4 to support wake from Thunderbolt devices.

=PP3V3_S4_TBTBPWRSW

CRITICAL C9687 100UF 20% 6.3V POLY-TANT CASE-B2-SM; CRITICAL C9680 22UF 20% 6.3V X5R-CERM-1 603; C9681 0.1UF 10% 16V X5R-CERM 0201

=PPHV_SW_TBTBPWRSW

18V Max

OMIT_TABLE

C9615 4.7UF 10% 16V X5R-CERM 0603; C9610 0.1UF 10% 16V X5R-CERM 402

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 35, 9-12.6V, 7.5-11.7W)

CRITICAL U9610 CD3210A0RGP QFN

V3P3 — V3P3OUT; VHV — OUT; RSVD; EN; HV_EN; S0; ISET_V3P3; ISET_S0; ISET_S3; GND; THRM PAD

C9685 0.1UF 10% 16V X5R-CERM 0201; C9686 10UF 20% 6.3V CERM-X5R 0402; C9611 0.1UF 10% 25V X5R 402

PP3V3_SW_TBTBPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=3.3V

PPHV_SW_TBTBPWR — MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

=TBTBPWRSW_EN; TBT_B_HV_EN_RC; =TBT_S0_EN

TBTBPWRSW_ISET_V3P3; TBTBPWRSW_ISET_S0; TBTBPWRSW_ISET_S3; TBTBPWRSW_ISET_S3_R; TBTBPWRSW_ISET_S0_R

12V: See below

R9610 22.6K 1% 1/20W MF 201 — TBTHV:P15V; R9611 22.6K 1% 1/20W MF 201 — TBTHV:P15V; R9612 36.5K 1% 1/20W MF 201 <RV3P3>

R9613 22.6K 1% 1/20W MF 201 <RHVS3> — TBTHV:P15V; R9614 22.6K 1% 1/20W MF 201 <RHVS0> — TBTHV:P15V

Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9610,R9613		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/16W,17.8K,1,0201,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

PP3V3_SW_TBTBPWR

C9620 0.1UF 10% 16V X5R-CERM 0201; C9621 0.1UF 10% 16V X5R-CERM 0201; R9627 10K 5% 1/20W MF 201; R9629 100K 5% 1/20W MF 201

CRITICAL U9620 CBTL05023 HVQFN

SIGNAL_MODEL=TBT_MUX

TBT_B_CIO_SEL; DP_AUXIO_EN; DP_TBTPB_AUXCH_N; DP_TBTPB_AUXCH_P; DP_TBTPB_DDC_DATA; DP_TBTPB_DDC_CLK; TBT_B_CONFIG1_BUF; DP_TBTPB_ML_P<1>; DP_TBTPB_ML_N<1>; TBT_B_LSTX; TBT_B_LSRX_UNBUF; TBT_B_DP_PWRDN; DP_TBTPB_HPD

BIASIN; AUXIO_EN; AUX-; AUX+; DDC_DAT; DDC_CLK; CA_DETOUT; DP+; DP-; LSTX; LSRX; DP_PD; HPDOUT; BIASOUT; AUXIO-; AUXIO+; CA_DET; DPML0+; DPML0-; HPD; VDD; GND; THMPAD

TBT_B_BIAS VOLTAGE=3.3V — C9625 0.1UF 10% 16V X5R-CERM 0201

DP_B_AUXCH_DDC_N; DP_B_AUXCH_DDC_P — TBT: RX_1 Bias Sink

TBT_B_CONFIG1_RC; DP_B_LSX_ML_P<1>; DP_B_LSX_ML_N<1> — TBT: LSX_A_R2P/P2R (P/N)

TBT_B_HPD

C9630 0.1UF 10% 16V X5R-CERM 0201; C9631 0.1UF 10% 16V X5R-CERM 0201

C9632 0.22UF 20% 6.3V X5R 0201; C9633 0.22UF 20% 6.3V X5R 0201

R9626 1M 5% 1/20W MF 201; R9628 100K 5% 1/20W MF 201

PP3V3_SW_TBTBPWR

CRITICAL U9660 74AUP1T97 SOT891

TBT_B_LSRX Y = B

C9660 0.1UF 10% 16V X5R-CERM 0201

L9600 FERR-120-OHM-3A 0603 — PP3V3RHV_SW_TBTBPWR MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=15V

C9600 0.01UF 10% 50V X7R-CERM 0402

TBTBCONN_20_RC MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18V

C9601 0.01UF 10% 50V X7R-CERM 0402

R9601 12 5% 1/20W MF 201

TBT Dir; DP Dir

For J9600 TBT SMT pads (3, 5, 17 & 19):

CRITICAL J9400 MDP-D1 F-RT-TH

SHIELD PINS: S5 S4 S3 S2 S1

HPD; CONFIG1; CONFIG2; GND2; ML_LANE3P; ML_LANE3N; GND4; AUX_CHP; AUX_CHN; DP_PWR

GND0; ML_LANE0P; ML_LANE0N; GND1; ML_LANE1P; ML_LANE1N; GND3; ML_LANE2P; ML_LANE2N; RETURN

PORT A

SHIELD PINS: S23 S11 S10 S9 S8 S7 S6

514-0836

TBTBCONN_1_C MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V

C9605 0.01UF 10% 16V X5R-CERM 0201

(0-18.9V) DP Dir; TBT Dir

TBT: TX_0

TBTBCONN_7_C MIN_LINE_WIDTH=0.38 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=18.9V

C9606 0.01UF 10% 16V X5R-CERM 0201

TBT_B_R2D_C_P<0>; TBT_B_R2D_N<0>

C9670 0.22UF 20% 6.3V X5R 0201; C9671 0.22UF 20% 6.3V X5R 0201

R9670 470K 5% 1/20W MF 201; R9671 470K 5% 1/20W MF 201

(0-18.9V)

DP_B_LSX_ML_P<1>; DP_B_LSX_ML_N<1>

TBT: LSX_R2P/P2R (P/N)

TBT_B_R2D_P<1>; TBT_B_R2D_N<1>

TBT: TX_1

C9672 0.22UF 20% 6.3V X5R 0201; C9673 0.22UF 20% 6.3V X5R 0201

R9672 470K 5% 1/20W MF 201; R9673 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

TBT_B_D2R_P<0>; TBT_B_D2R_N<0>

C9674 0.47UF 20% 4V CERM-X5R-201; C9675 0.47UF 20% 4V CERM-X5R-201

TBT_B_D2R_C_P<0>; TBT_B_D2R_C_N<0>

R9694 1K 5% 1/20W MF 201; R9695 1K 5% 1/20W MF 201

DP_TBTPB_ML_C_P<3>; DP_TBTPB_ML_C_N<3>

C9678 0.22UF 20% 6.3V X5R 0201; C9679 0.22UF 20% 6.3V X5R 0201

DP_TBTPB_ML_P<3>; DP_TBTPB_ML_N<3> — TBT: Unused

R9678 470K 5% MF 1/20W 201; R9679 470K 5% MF 1/20W 201

TBT_B_BIAS

R9698 2.2K 5% 1/20W MF 201; R9699 2.2K 5% 1/20W MF 201

TBT_B_D2R_P<1>; TBT_B_D2R_N<1>

C9676 0.47UF 20% 4V CERM-X5R-201; C9677 0.47UF 20% 4V CERM-X5R-201

TBT_B_D2R_C_P<1>; TBT_B_D2R_C_N<1>

CRITICAL SIGNAL_MODEL=TBTPIN

D9698 BAR90-02LRH; D9699 BAR90-02LRH — TSLP-2-7 (Both D's)

TBT_B_D2R1_AUXDDC_P; TBT_B_D2R1_AUXDDC_N

CRITICAL L9698 650NH-5%-0.430MA-0.52OHM 0603

DP_B_AUXCH_DDC_P; DP_B_AUXCH_DDC_N

C9698 30PF 5% 25V C0G-CERM 0201; C9699 30PF 5% 25V C0G-CERM 0201

CRITICAL L9699 650NH-5%-0.430MA-0.52OHM 0603

TBT_B_HPD; TBT_B_CONFIG1_RC; TBT_B_CONFIG2_RC

R9652 1M 5% 1/20W MF 201; R9651 1M 5% 1/20W MF 201

C9694 330PF 10% 16V X7R-CERM 0201; C9695 330PF 10% 16V X7R-CERM 0201

R9641 100K 5% 1/20W MF 201

C9602 0.01UF 10% 16V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=11/14/2011

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

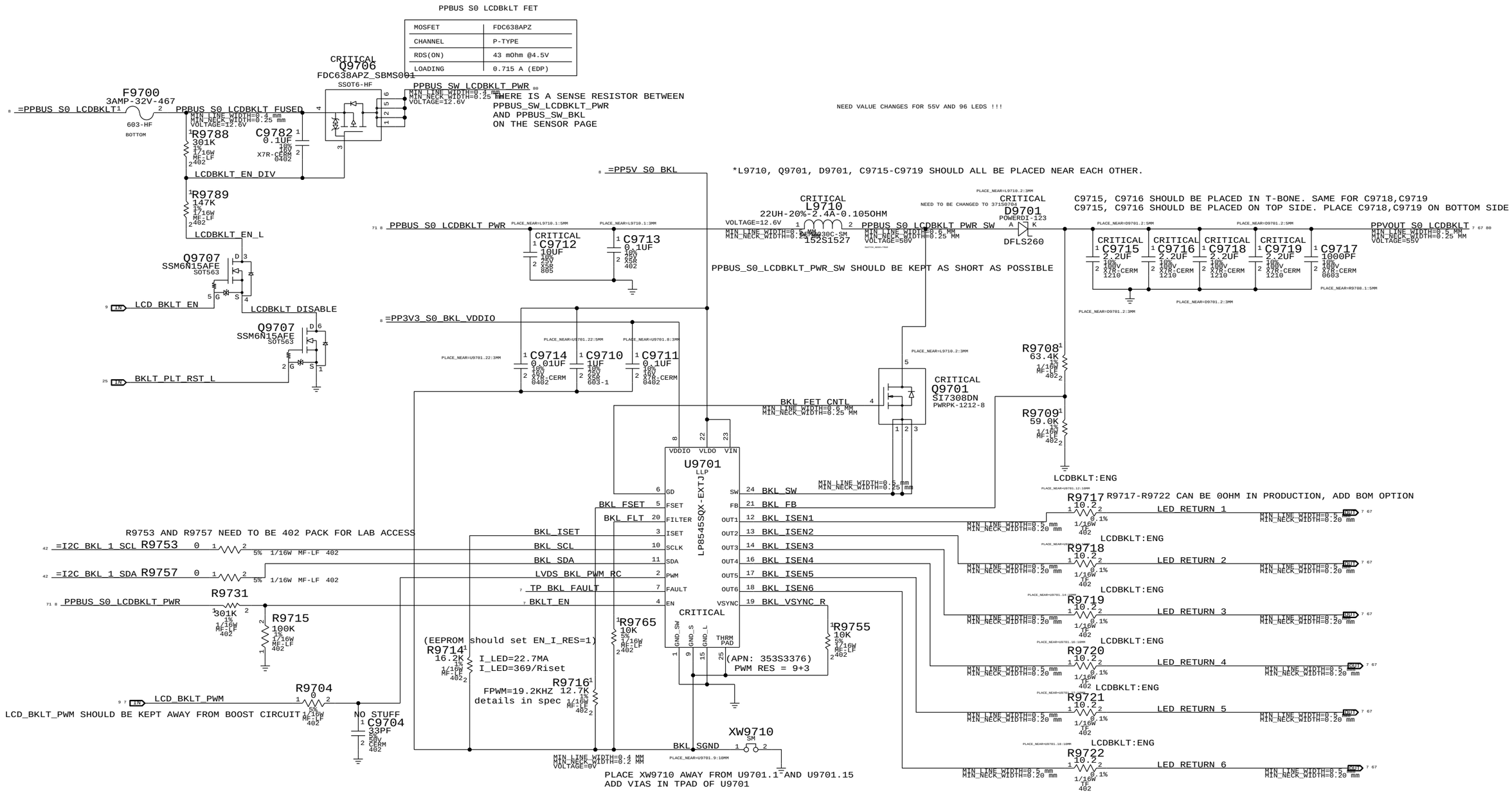
REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 96 OF 132

SHEET: 70 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	6	RES,MTL FILM,1/16W,0,5,0402,SMD,LF	R9717,R9718,R9719,R9720,R9721,R9722	CRITICAL	LCDBKLT:PROD

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=09/21/2011

PAGE TITLE

LCD Backlight Driver (LP8545)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 97 OF 132

SHEET 71 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.1MM	0.1MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	=4X_DIELECTRIC	?
CPU_ITP	*	=4x_DIELECTRIC	?
CPU_VCCSENSE	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=6X_DIELECTRIC	?
CLK_PCIE	*	=5X_DIELECTRIC	?

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	7 10 18
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	7 10 18
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	7 10 18
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	7 10 18
FDI_FSYNC	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	10 18
FDI_LSYNC	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	10 18
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	10 18
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	7 11 17
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	7 11 17
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_COMP	10
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	10
CPU_CFG	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 24
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	11 17
XDP_CLK_CPU	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	11 17
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	17 24
XDP_CLK_PCH	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	17 24
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_P	11 17
DPLL_REF_CLK120M	CLK_PCIE_90D	CLK_PCIE	DPLL_REF_CLK_N	11 17
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	11 24
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	11 24
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	11 24
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	11 24
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	11 24
XDP_BPM	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	11 24
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<7..4>	11 24
XDP_DBRESET_L	CPU_50S	CPU_ITP	XDP_DBRESET_L	11 24 25
XDP_PRDY_L	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	11 24
XDP_PREQ_L	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	11 24
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	11 39
CPU_PROC_SEL_L	CPU_50S	CPU_AGTL	CPU_PROC_SEL_L	11 20
CPU_PECI	CPU_50S	CPU_VID	CPU_PECI	11 20 40
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	11 39 40 61
XDP_CPU_PWRGD	CPU_50S	CPU_ITP	XDP_CPU_PWRGD	24
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	11 20 40
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	11 18
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	11 18 27
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	11 20 24
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	11
	CPU_50S	CPU_VID	CPU_VIDSOUT	13 61
	CPU_50S	CPU_VID	CPU_VIDSCLK	13 61
	CPU_50S	CPU_VID	CPU_VIDALERT_L	13 61
	CPU_55S	CPU_VID	CPU_VCCSA_VID<1..0>	13 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	13 63
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	13 61
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	10
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	10
CPU_VCCSASENSE	CPU_50S	CPU_AGTL	CPU_VCCSASENSE	13 58
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_A	10 31
CPU_MEM_VREF		CPU_VREF	PPCPU_MEM_VREFDQ_B	10 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	29 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_A	28 31
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFCA_B	29 31
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	24
XDP_CLK_ITP	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	24

SYNC_MASTER=J5_MLB SYNC_DATE=09/13/2012

PAGE TITLE

CPU Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 100 OF 132

SHEET 72 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4X_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3X_DIELECTRIC	?
MEM_CTRL2MEM	*	=3X_DIELECTRIC	?
MEM_CMD2CMD	*	=2X_DIELECTRIC	?
MEM_CMD2MEM	*	=3X_DIELECTRIC	?
MEM_DATA2DATA	*	=2X_DIELECTRIC	?
MEM_DATA2MEM	*	=3X_DIELECTRIC	?
MEM_DQS2MEM	*	=4X_DIELECTRIC	?
MEM_2OTHER	*	=6X_DIELECTRIC	?
MEM_DQBL2BL	*	=4X_DIELECTRIC	?
MEM_DQCH2CH	*	=6X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_*	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_*	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_*	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_*	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQ_BYTE*	MEM_*	*	MEM_DATA2MEM
MEM_*_DQ_BYTE*	=SAME	*	MEM_DATA2DATA
MEM_A_DQ_BYTE*	MEM_A_DQ_BYTE*	*	MEM_DQBL2BL
MEM_B_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQBL2BL
MEM_A_DQ_BYTE*	MEM_B_DQ_BYTE*	*	MEM_DQCH2CH

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	12 28 30
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	12 28 30
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<1..0>	12 28 30
1181 MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<1>	12 28 30
1182 MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<0>	12 28 30
1183 MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<1>	12 28 30
1184 MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	12 28 30
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	12 28 30
MEM_A_DQ_BYTE0	MEM_50S	MEM_A_DQ_BYTE0	MEM_A_DQ<7..0>	7 12 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_A_DQ_BYTE1	MEM_A_DQ<15..8>	7 12 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_A_DQ_BYTE2	MEM_A_DQ<23..16>	7 12 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_A_DQ_BYTE3	MEM_A_DQ<31..24>	7 12 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_A_DQ_BYTE4	MEM_A_DQ<39..32>	7 12 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_A_DQ_BYTE5	MEM_A_DQ<47..40>	7 12 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_A_DQ_BYTE6	MEM_A_DQ<55..48>	7 12 28
1185 MEM_A_DQ_BYTE7	MEM_50S	MEM_A_DQ_BYTE7	MEM_A_DQ<63..56>	7 12 28
1186 MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	12 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	12 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	12 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	12 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	12 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	12 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	12 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	12 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	12 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	12 29 30
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	12 29 30
1110 MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<1>	12 29 30
1111 MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<0>	12 29 30
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	12 29 30
1109 MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<1..0>	12 29 30
1108 MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	12 29 30
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	12 29 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_B_DQ_BYTE0	MEM_B_DQ<7..0>	7 12 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_B_DQ_BYTE1	MEM_B_DQ<15..8>	7 12 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_B_DQ_BYTE2	MEM_B_DQ<23..16>	7 12 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_B_DQ_BYTE3	MEM_B_DQ<31..24>	7 12 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_B_DQ_BYTE4	MEM_B_DQ<39..32>	7 12 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_B_DQ_BYTE5	MEM_B_DQ<47..40>	7 12 29
MEM_B_DQ_BYTE6	MEM_50S	MEM_B_DQ_BYTE6	MEM_B_DQ<55..48>	7 12 29
MEM_B_DQ_BYTE7	MEM_50S	MEM_B_DQ_BYTE7	MEM_B_DQ<63..56>	7 12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	12 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	12 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	12 29
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	12 29
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	12 29
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	12 29
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	12 29
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	12 29
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	12 29

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Chief River SFF Platform DG, Rev 0.7 (#460452), Section 2.6.3

SYNC_MASTER=J5_MLB SYNC_DATE=09/13/2013

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 101 OF 132

SHEET: 73 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Digital Video Signal Constraints

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5:1_SPACING	?
SATA_ICOMP	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4:1_SPACING	?
USB_RBIAS	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4:1_SPACING	?

SOURCE: HR PLATFORM DESIGN GUIDE, TABLES 191,193

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	*	=5:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	=5:1_SPACING	?

SOURCE: CR SFF PLATFORM DESIGN GUIDE V0.7, TABLE 4-211, 1X1+

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T25 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_P	7
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDRIN_N	7
T25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_P	7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDROUT_N	7
T25 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_P	7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RDRIN_N	7
T25 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_N	7
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RDROUT_P	7
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_P	7 37
T26 SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_RC_N	7 37
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_N	7 37
T26 SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_RC_P	7 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	7 17 37
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_N	7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	7 17 37
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	7 17 37
T232 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_P	7 37
T233 SATA_HDD_D2R	SATA_90D	SATA	SATA_SSDRHDD_D2R_N	7 37
T234 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_P	7 37
T235 SATA_HDD_R2D	SATA_90D	SATA	SATA_SSDRHDD_R2D_N	7 37
T33 PCH_SATA3_ICOMP	SATA_50SE	SATA_ICOMP	PCH_SATA3COMP	17
PCH_SATA_ICOMP	SATA_37SE	SATA_ICOMP	PCH_SATAICOMP	17
T236 USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_P	19 26
T237 USB_EXTB	USB_85D	USB	USB_EXTB_XHCI_N	19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_P	19 26
USB_EXTB	USB_85D	USB	USB_EXTB_EHCI_N	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_P	19 26
USB_HUB2_UP	USB_85D	USB	USB_HUB_UP_N	19 26
USB_EXTA	USB_85D	USB	USB_EXTA_P	19 38
USB_EXTA	USB_85D	USB	USB_EXTA_N	19 38
USB_EXTB	USB_85D	USB	USB_EXTB_P	7 26 36
USB_EXTB	USB_85D	USB	USB_EXTB_N	7 26 36
USB_EXTC	USB_85D	USB	USB_EXTD_P	
USB_EXTC	USB_85D	USB	USB_EXTD_N	
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	7 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_N	7 32
USB_BT	USB_85D	USB	USB_BT_P	7 9 36
USB_BT	USB_85D	USB	USB_BT_N	7 9 36
USB_TPAD	USB_85D	USB	USB_TPAD_P	9 47
USB_TPAD	USB_85D	USB	USB_TPAD_N	9 47
USB_SMC	USB_85D	USB	USB_SMC_P	9 39
USB_SMC	USB_85D	USB	USB_SMC_N	9 39
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	19
T238 USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_P	19 26
T239 USB_EXTD	USB_85D	USB	USB_EXTD_XHCI_N	19 26
T245 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	38
T244 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	38
T247 USB_CAMERA	USB_85D	USB	USB_CAMERA_P	19 32
T246 USB_CAMERA	USB_85D	USB	USB_CAMERA_N	19 32
T248 USB_EXTA	USB_85D	USB	USB_LT1_P	7 38
T249 USB_EXTA	USB_85D	USB	USB_LT1_N	7 38
T220 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_P	19 36
T221 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_N	19 36
T222 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_P	7 19 36
T223 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_N	7 19 36
T230 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_P	19 38
T229 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_N	7 19 38
T228 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_P	7 19 38
T231 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_N	7 19 38

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T256 SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	17 25
T255 SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	17 25
T254	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	17
T253 SYSCLK_CLK25M_ENET	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	
T252	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
T251 SYSCLK_CLK25M_TBT	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT	25 33
T250	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_TBT_R	33

SYNC_MASTER=J5_MLB_KEPLER SYNC_DATE=09/21/2012

PAGE TITLE

PCH Constraints 1

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 102 OF 132

SHEET 74 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LPC_AD	LPC_50S	LPC	LPC AD<3..0>	7 17 39 41
	LPC_FRAME_L	LPC_50S	LPC	LPC FRAME L	7 17 39 41
	LPC_RESET_L	LPC_50S	LPC	LPC RESET L	25
	PCH_LPC_CLK0	CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC R	19 25
		CLK_LPC_50S	CLK_LPC	LPC CLK33M SMC	7 25 39
		CLK_LPC_50S	CLK_LPC	LPC CLK33M LPCPLUS	7 25 41
	SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS PCH CLK	7 17 42
	SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS PCH DATA	7 17 42
	SMBUS_PCH_0_CLK	SMB_50S	SMB	SML PCH 0 CLK	17 42
	SMBUS_PCH_0_DATA	SMB_50S	SMB	SML PCH 0 DATA	17 42
	SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SML PCH 1 CLK	17 42
	SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SML PCH 1 DATA	17 42
	HDA_BIT_CLK	HDA_50S	HDA	HDA BIT CLK	17 51
		HDA_50S	HDA	HDA BIT CLK R	17
	HDA_SYNC	HDA_50S	HDA	HDA SYNC	17 51
		HDA_50S	HDA	HDA SYNC R	17
	HDA_RST_L	HDA_50S	HDA	HDA RST R L	17
		HDA_50S	HDA	HDA RST L	17 51
	HDA_SDIN0	HDA_50S	HDA	HDA SDIN0	17 51
		HDA_50S	HDA	AUD SDI R	51
	HDA_SDOUT	HDA_50S	HDA	HDA SDOUT	17 51
		HDA_50S	HDA	HDA SDOUT R	17 25
	SPI_CLK	SPI_55S	SPI	SPI CLK R	17 41
		SPI_55S	SPI	SPI CLK	41
	SPI_MOSI	SPI_55S	SPI	SPI MOSI R	17 41
		SPI_55S	SPI	SPI MOSI	41
	SPI_MISO	SPI_55S	SPI	SPI MISO	17 41
	SPI_CS0	SPI_55S	SPI	SPI CS0 R L	17 41
		SPI_55S	SPI	SPI CS0 L	41
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C P	7 17 36
	PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE ENET R2D C N	7 17 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R P	7 17 36
	PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE ENET D2R N	7 17 36
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D P	7 36
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D N	7 36
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C P	7 17 36
	PCIE_AP_R2D	PCIE_85D	PCIE	PCIE AP R2D C N	7 17 36
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R P	7 17 36
	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R N	7 17 36
1276	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R PI P	7 36
1275	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP D2R PI N	7 36
1277	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP R2D PI P	7 36
1277	PCIE_AP_D2R	PCIE_85D	PCIE	PCIE AP R2D PI N	7 36
1263	PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH P	7 17
1264	PCIE_CLK100M_PCH	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M PCH N	7 17
1262	PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M TBT P	7 17 33
1261	PCIE_CLK100M_TBT	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M TBT N	7 17 33
1267	PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT P	17
1266	PCH_CLK96M	CLK_PCIE_90D	CLK_PCIE	PCH CLK96M DOT N	17
1269	PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA P	7 17
1268	PCH_CLK100M_SATA	CLK_PCIE_90D	CLK_PCIE	PCH CLK100M SATA N	17
1256		CPU_50S	CLK_PCIE	PCH CLK14P3M REFCLK	17
1246		CPU_50S	CLK_PCIE	PCH CLK33M PCIIN	7 17 25
1270	PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M SSD P	7 9 17
1271	PCIE_CLK100M_SSD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M SSD N	7 9 17
	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M P	7 9 17
	PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PEG CLK100M N	7 9 17
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET P	7 17 36
	PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M ENET N	7 17 36
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP P	7 17 36
	PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M AP N	7 17 36
	PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW P	7 9 17
	PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M FW N	7 9 17
	PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD P	7 17
	PCIE_CLK100M_EXCARD	CLK_PCIE_90D	CLK_PCIE	PCIE CLK100M EXCARD N	7 17
1243	PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE TBT R2D C P<3..0>	7 9 33
1244	PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE TBT R2D C N<3..0>	7 9 33
1245	PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE TBT R2D P<3..0>	7 33
1247	PCIE_TBT_R2D	PCIE_85D	PCIE	PCIE TBT R2D N<3..0>	7 33
1250	PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE TBT D2R P<3..0>	7 9 33
1248	PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE TBT D2R N<3..0>	7 9 33
1276	PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE TBT D2R C P<3..0>	7 33
1260	PCIE_TBT_D2R	PCIE_85D	PCIE	PCIE TBT D2R C N<3..0>	7 33

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2013

PAGE TITLE
PCH Constraints 2

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 103 OF 132
SHEET 75 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?

NOTE: Thunderbolt high-speed nets are NOT directly assigned to TBTDP_*D physical rules.
TABLE_PHYSICAL_ASSIGNMENT symbols must be used to create the assignments.
Proper differential impedance depends on mDP connector used.
For 514-0637: R2D nets (SMT pins) = 80D, D2R nets (TH pins) = 100D

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
HDMI	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMI	TOP,BOTTOM	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_P<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_C_N<1..0>	7 33 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_P<1..0>	7 69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_A_R2D_N<1..0>	7 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3..1:2>	33 69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3..1:2>	69
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3..1:2>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	69
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<1>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<1>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_C_P<0>	7 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_C_N<0>	7 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_P<1>	7 33 69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R_N<1>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_P<0>	7 33 69
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_A_D2R_N<0>	7 33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	33 69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	69
TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	69
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	69
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_P	69
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_A_D2R1_AUXDDC_N	69
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_P<1..0>	7 33 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_C_N<1..0>	7 33 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_P<1..0>	7 70
TBT_A_R2D	TBTDP_85D	TBTDP	TBT_B_R2D_N<1..0>	7 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3..1:2>	33 70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3..1:2>	70
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3..1:2>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	70
DP_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<0>	7 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<0>	7 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_C_P<1>	7 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_C_N<1>	7 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_P<0>	7 33 70
TBT_A_D2R0	TBTDP_85D	TBTDP	TBT_B_D2R_N<0>	7 33 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_P<1>	7 33 70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R_N<1>	7 33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	33 70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	70
TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	70
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	70
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_P	70
TBT_A_D2R1	TBTDP_85D	TBTDP	TBT_B_D2R1_AUXDDC_N	70

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	33
TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	33
TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	33
TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	33

Only used on hosts supporting Thunderbolt video-in

SYNC MASTER=T29_CR SYNC_DATE=08/31/2013

PAGE TITLE
Thunderbolt Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 105 OF 132

SHEET 76 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_2_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	7 39 42
SMBUS_SMC_2_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	7 39 42
SMBUS_SMC_1_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	7 39 42
SMBUS_SMC_1_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	7 39 42
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	39 42
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	39 42
SMBUS_SMC_5_SCL	SMB_50S	SMB	SMBUS_SMC_5_SCL	
SMBUS_SMC_5_SDA	SMB_50S	SMB	SMBUS_SMC_5_SDA	
SMBUS_SMC_3_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	39 42
SMBUS_SMC_3_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	39 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	57
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_N	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	57
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_N	57

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE
SMC Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 106 OF 132

SHEET 77 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_CLK	*	GND_P2MM
GND	MEM_CMD	*	GND_P2MM
GND	MEM_CTRL	*	GND_P2MM
GND	MEM_*_DQ_BYTE*	*	GND_P2MM
GND	MEM_DQS	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB3	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB3	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations
Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_37S	BGA_MEM	MEM_50S
MEM_40S	BGA_MEM	MEM_50S
MEM_72D	BGA_MEM	MEM_85D

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
1TO1_DIFFPAIR	*	1:1_DIFFPAIR
SENSE_1TO1_55S	*	SENSE_1TO1_55S
THERM_1TO1_55S	*	THERM_1TO1_55S
DIFFPAIR	*	DIFFPAIR

Graphics, SATA Constraint Relaxations
Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	100_DIFF_BGA
SATA_90D	BGA	100_DIFF_BGA
CLK_PCIE_90D	BGA	100_DIFF_BGA

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 10
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	TBT_THERMD_N	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_P	45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	DDR3THMSNS_D1_N	45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	43 63
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_P	13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_VDDQ_SENSE_N	13
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCD_PANEL_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_P	37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_SSD_N	37 43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_3V3_S0_SSD_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_WLAN_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_P	80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_TBT_N	80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V35_S3_MEM_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	58 80
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	58 80
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_P	7 9 36
HDMI_CLK	HDMI_90D	HDMI	HDMI_IG_CLK_C_N	7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_P<2..0>	7 9 36
HDMI_DATA	HDMI_90D	HDMI	HDMI_IG_DATA_C_N<2..0>	7 9 36

D1 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	7 36
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	7 36
	1TO1_DIFFPAIR		CHGR_CSI_R_P	57
	1TO1_DIFFPAIR		CHGR_CSI_R_N	57
	1TO1_DIFFPAIR		CHGR_CSO_R_P	57
	1TO1_DIFFPAIR		CHGR_CSO_R_N	57
USB_BT	USB_85D	USB	USB_BT_CONN_P	36
USB_BT	USB_85D	USB	USB_BT_CONN_N	36
USB_BT	USB_85D	USB	USB_BT_WAKE_P	36
USB_BT	USB_85D	USB	USB_BT_WAKE_N	36
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	7 53 55
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	7 53 55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	43 61 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	43 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	43
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	43
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	51 54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	RSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI_RC	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO_RC	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_HI	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_LO	54
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_L_OUT_N	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_P	7 53 55 78
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	SPKRCONN_R_OUT_N	7 53 55 78
USB_TPAD	USB_85D	USB	USB_TPAD_R_P	26 47
USB_TPAD	USB_85D	USB	USB_TPAD_R_N	26 47
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_P	9
USB_HUB	USB_85D	USB	PU_USBHUB_DN4_N	9
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8
		SB_POWER	PP1V5_S3RS0_CPUDDR	8
		GND	GND	

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE
Project Specific Constraints

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 108 OF 132
SHEET 78 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

D1 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_MEM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
50_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.105 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.120 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.190 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.124 MM	0.124 MM		0.200 MM	0.200 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.180 MM	0.180 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.110 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.090 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.065 MM	0.065 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.079 MM	0.079 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE

Stackup-Defined Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	TOP,BOTTOM	0.1 MM	?
1:1_SPACING	ISL3,ISL4,ISL9,ISL10	0.1 MM	?
1:1_SPACING	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

J4 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
166 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	9 33
167 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	9 33
165 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	9 33
167 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	9 33
168 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	9 33
169 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	9 33
168 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	9 33
170 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	9 33
172 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	33
173 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	33
174 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	33
175 DP_TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	33
176 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	33
177 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	33
178 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	33
179 DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	33
162 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	9 67
161 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	9 67
159 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_P	9 67
160 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_C_N	9 67
157 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	7 67
158 DP_INT_AUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	7 67
156 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67
155 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67
154 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	
153 DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	
141 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_P	7 36
142 USB3_EXTB_RX	USB3_85D	USB3	USB3_EXTB_RX_RC_N	7 36
143 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_P	7 38
144 USB3_EXTA_RX	USB3_85D	USB3	USB3_EXTA_RX_F_N	7 38
145 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_P	7 38
146 USB3_EXTA_TX	USB3_85D	USB3	USB3_EXTA_TX_C_N	7 38
147 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_P	7 36
148 USB3_EXTB_TX	USB3_85D	USB3	USB3_EXTB_TX_C_N	7 36

SYNC_MASTER=J5_MLB SYNC_DATE=07/29/2011

PAGE TITLE
PCB Rule Definitions

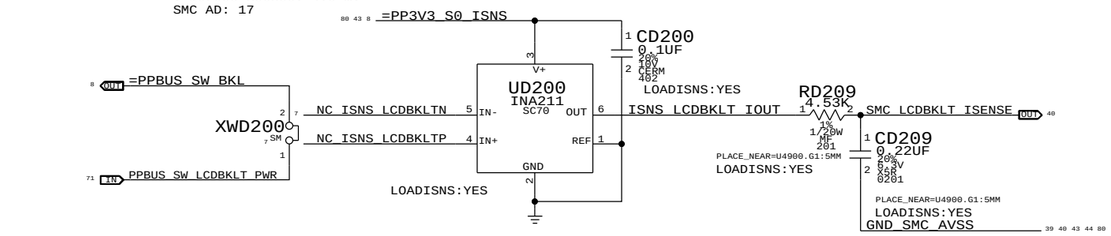
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 109 OF 132
SHEET 79 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

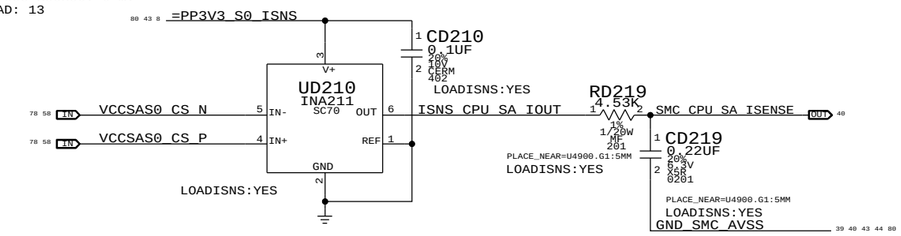
LCD Backlight Current Sense (IBLC)

Gain: 500x. EDP: 0.9 A
Rsense: 0.005 (RD200 / XWD200)
V across Rsense: 4.5 mV
SMC AD: 17



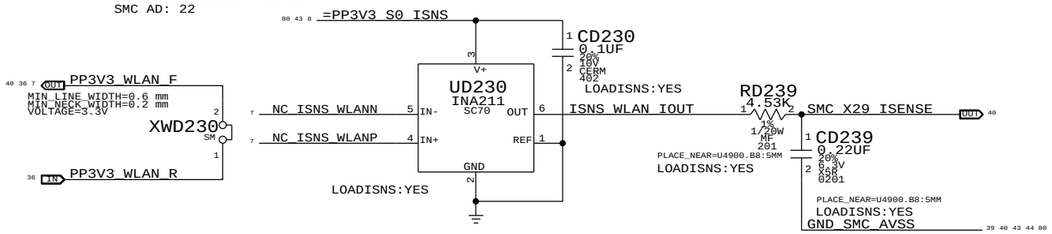
CPU SA Current Sense (IC2C)

Gain: 500x. EDP: 6 A
Rsense: 0.001 (R7140)
V across Rsense: 6 mV
SMC AD: 13



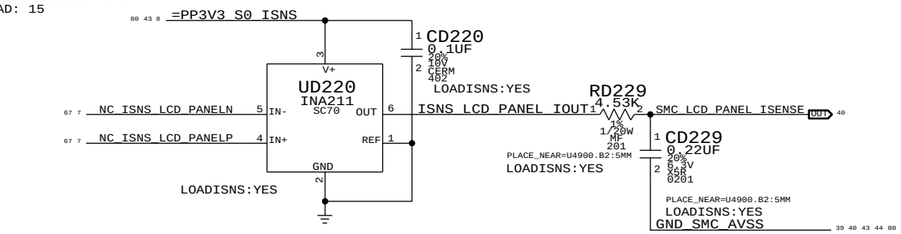
Airport X29 Current Sense (IAPC)

Gain: 500x. EDP: 1.06 A
Rsense: 0.005 (RD230 / XWD230)
V across Rsense: 5.3 mV
SMC AD: 22



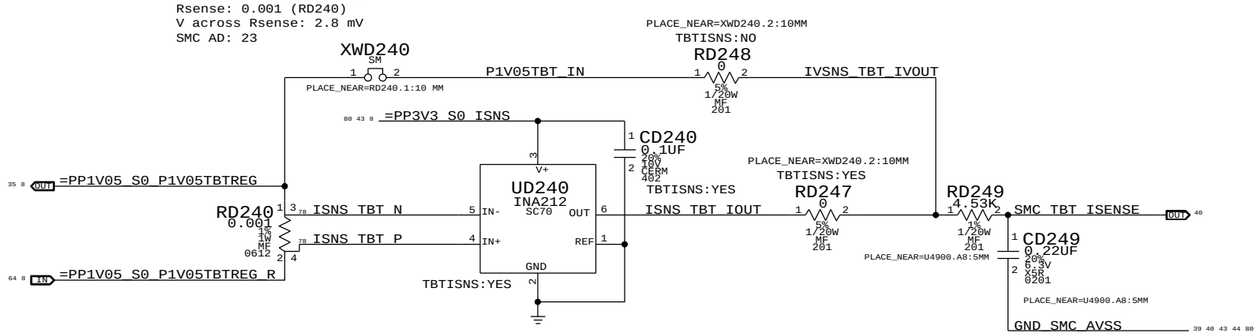
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
Rsense: 0.005 (R9020, XW9020)
V across Rsense: 5 mV
SMC AD: 15



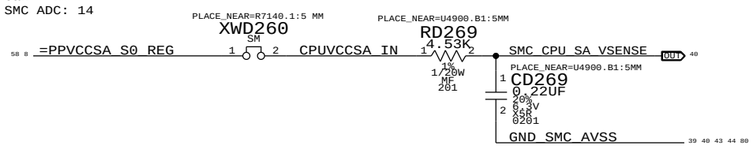
Thunderbolt TBT Current/Voltage Sense (IHSP/VHSP)

Gain: 1000x. EDP: 2.8 A
Rsense: 0.001 (RD240)
V across Rsense: 2.8 mV
SMC AD: 23



CPU SA Voltage Sense (VC2C)

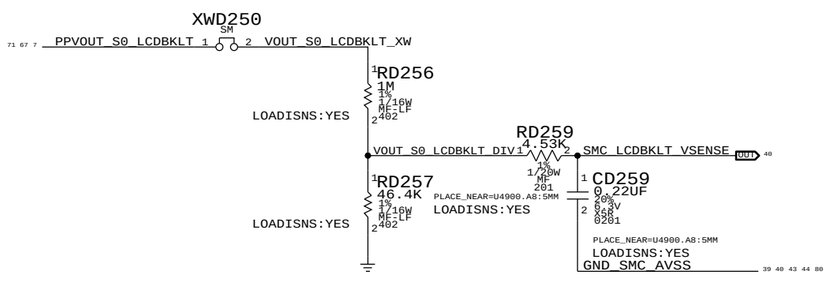
Gain: 1x
SMC ADC: 14



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD209,CD219,CD229		LOADISNS:NO
117S0008	3	RES,MTL FILM,100K,1/16W,0201,SMD,LF	CD239,CD259		LOADISNS:NO

LCD Backlight Voltage Sense (VBLC)

Gain: 0.04434



SYNC_MASTER=D1_SENSORS SYNC_DATE=07/11/2012

PAGE TITLE
Power Sensors: Extended

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 132 OF 132
SHEET 80 OF 80

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED