1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J17 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0002056619	PRODUCTION RELEASED	2013-05-30

LAST_MODIFIED=Fri May 31 13:43:58 2013

Page (.csa)		Contents	Sync Date
1	1	Table of Contents	MASTER N/A
2	2	BOM Configuration	J17_DINI 02/06/2013
3	3	DEBUG LEDS	J17_ULTIMATE 05/16/2013
4	4	Holes/PD parts	J17_ULTIMATE 05/16/2013
5	5	CPU DMI/PEG/FDI/RSVD	J17_ULTIMATE 05/16/2013
6	6	CPU Clock/Misc/JTAG/CFG	J17_ULTIMATE 05/16/2013
7	7	CPU DDR3 Interfaces	J17_ULTIMATE 05/16/2013
8	8	CPU Power	J17_ULTIMATE 05/16/2013
9	9	CPU Ground	J17_ULTIMATE 05/16/2013
10	10	CPU DECOUPLING	J17_ULTIMATE 05/16/2013
11	11	PCH RTC/HDA/JTAG/SATA/CLK	J17_ULTIMATE 05/16/2013
12	12	PCH DMI/FDI/PM/GFX/PCI	J17_ULTIMATE 05/16/2013
13	13	PCH PCI-E/USB	J17_ULTIMATE 05/16/2013
14	14	PCH GPIO/MISC/NCTF	J17_ULTIMATE 05/16/2013
15	15	PCH Power	J17_ULTIMATE 05/16/2013
16	16	PCH Grounds	J17_ULTIMATE 05/16/2013
17	17	PCH DECOUPLING	J17_ULTIMATE 05/16/2013
18	18	CPU & PCH XDP	J17_ULTIMATE 05/16/2013
19	19	Chipset Support	J17_ULTIMATE 05/16/2013
20	20	Project Chipset Support	J17_ULTIMATE 05/16/2013
21	21	CPU Memory S3 Support	J17_ULTIMATE 05/16/2013
22	22	DDR3 VREF MARGINING	J17_ULTIMATE 05/16/2013
23	23	DDR3 SO-DIMM Connector A Slot0	J17_ULTIMATE 05/16/2013
24	24	DDR3 SO-DIMM Connector A Slot1	J17_ULTIMATE 05/16/2013
25	25	DDR3 SO-DIMM CONNECTOR B SLOT0	J17_ULTIMATE 05/16/2013
26	26	DDR3 SO-DIMM CONNECTOR B SLOT1	J17_ULTIMATE 05/16/2013
27	27	DDR3 ALIASES AND BITSWAPS	J17_ULTIMATE 05/16/2013
28	28	Thunderbolt Host (1 of 2)	J17_ULTIMATE 05/16/2013
29	29	Thunderbolt Host (2 of 2)	J17_ULTIMATE 05/16/2013
30	30	Thunderbolt Power Support	J17_ULTIMATE 05/16/2013
31	32	Thunderbolt Connector A	J17_ULTIMATE 05/16/2013
32	33	Thunderbolt Connector B	J17_ULTIMATE 05/16/2013
33	34	TBT DDC Crossbar	J17_ULTIMATE 05/16/2013
34	35	AIRPORT/BT	J17_ULTIMATE 05/16/2013
35	37	SATA/SSD Connectors	J17_ULTIMATE 05/16/2013
36	38	HDD/SSD Temp Sense	J17_ULTIMATE 05/16/2013
37	39	ETHERNET PHY (CAESAR IV)	J17_ULTIMATE 05/16/2013
38	40	Ethernet Support & Connector	J17_ULTIMATE 05/16/2013
39	41	SD READER CONNECTOR	J17_ULTIMATE 05/16/2013
40	42	Camera Controller	J17_ULTIMATE 05/16/2013
41	43	Camera Controller Support	J17_ULTIMATE 05/16/2013
42	44	Internal DP Support	J17_ULTIMATE 05/16/2013
43	45	Internal DP MUXing	J17_ULTIMATE 05/16/2013
44	46	EXTERNAL USB PORTS A & B	J17_ULTIMATE 05/16/2013
45	47	EXTERNAL USB PORTS C & D	J17_ULTIMATE 05/16/2013
46	50	SMC	J17_ULTIMATE 05/16/2013
47	51	SMC Support	J17_ULTIMATE 05/16/2013
48	52	SPI and Debug Connector	J17_ULTIMATE 05/16/2013
49	53	SMBus Connections	J17_ULTIMATE 05/16/2013
50	54	I and V Sense	J17_ULTIMATE 05/16/2013
51	55	I and V Sense(Continued)	J17_ULTIMATE 05/16/2013
52	56	Temperature Sensors	J17_ULTIMATE 05/16/2013
53	60	System Fan	J17_ULTIMATE 05/16/2013
54	61	AUDIO: CODEC/REGULATORS	J17_ULTIMATE 05/16/2013
55	62	AUDIO: HEADPHONE AMP	J17_ULTIMATE 05/16/2013
56	63	AUDIO: LEFT SPKR AMP	J17_ULTIMATE 05/16/2013
57	64	AUDIO: RIGHT SPKR AMP	J17_ULTIMATE 05/16/2013
58	65	AUDIO: Jack, Mikey, CHS Switch	J17_ULTIMATE 05/16/2013
59	66	Audio: Spkr/Mic Conn.	J17_ULTIMATE 05/16/2013
60	67	AUDIO: Detects/Grounding	J17_ULTIMATE 05/16/2013
61	68	AUDIO: Speaker ID	J17_ULTIMATE 05/16/2013
62	69	Power Connectors / VReg G3Hot	J17_ULTIMATE 05/16/2013
63	70	VReg CPU VCC Cntl	J17_ULTIMATE 05/16/2013
64	71	VReg CPU VCC Phases	J17_ULTIMATE 05/16/2013
65	72	VReg CPU VCC Phase 4	J17_ULTIMATE 05/16/2013
66	73	VReg VDDQ S3	J17_ULTIMATE 05/16/2013
67	76	VReg 3.3V S5/5V S4	J17_ULTIMATE 05/16/2013
68	77	GPU VDDQ AND 1V05 GPU/PCH/TBT VREGS	J17_ULTIMATE 05/16/2013
69	78	VReg GPU Core Phases	J17_ULTIMATE 05/16/2013
70	79	VReg GPU Core Phases	J17_ULTIMATE 05/16/2013
71	80	VREG GPU CORE PHASE 4	J17_ULTIMATE 05/16/2013
72	81	BACKLIGHT LED DRIVER	J17_ULTIMATE 05/16/2013
73	82	Backlight LED Driver	J17_ULTIMATE 05/16/2013
74	83	Backlight Controller	J17_ULTIMATE 05/16/2013
75	84	FET-Controlled S0 and S4	J17_ULTIMATE 05/16/2013
76	85	PM Regulator Enables	J17_ULTIMATE 05/16/2013
77	86	PM Power Good	J17_ULTIMATE 05/16/2013
78	87	KEPLER PCI-E	J17_PETE 01/21/2013
79	88	KEPLER CORE/FB POWER	J17_PETE 01/21/2013
80	90	KEPLER FRAME BUFFER I/F	J17_PETE 11/02/2012
81	92	GDDR5 Frame Buffer A	J17_PETE 11/02/2012
82	93	GDDR5 Frame Buffer B	J17_PETE 11/02/2012
83	96	KEPLER EDP/DP/GPIO	J17_PETE 11/02/2012
84	97	KEPLER GPIOS,CLK & STRAPS	J17_PETE 11/02/2012
85	98	GPU SIGNAL & POWER ALIASES	J17_PETE 01/21/2013
86	99	KEPLER PEX PWR/GNDS	J17_PETE 01/21/2013
87	100	Power Connectors/Aliases	J17_ULTIMATE 05/16/2013
88	102	Signal Aliases	J17_ULTIMATE 05/16/2013
89	104	Unused Signal Aliases	J17_ULTIMATE 05/16/2013
90	105	Functional / ICT Test	J17_ULTIMATE 05/16/2013
91	110	J17 RULE DEFINITIONS	J17_ULTIMATE 05/16/2013
92	111	DDR3 Constraints	J17_ULTIMATE 05/16/2013
93	112	CPU PCIe Constraints	J17_NICK 12/14/2012
94	113	PCH PCIe/DMI Constaints	J17_ULTIMATE 05/16/2013
95	114	SATA/FDI/XDP Constraints	J17_ULTIMATE 05/16/2013
96	115	PCH and BR Constraints	J17_ULTIMATE 05/16/2013
97	116	USB/Ethernet/SD Constraints	J17_ULTIMATE 05/16/2013
98	117	SMBus/Sensor Constraints	J17_ULTIMATE 05/16/2013
99	118	VReg Constraints	J17_ULTIMATE 05/16/2013
100	119	CPU VReg Constraints	J17_ULTIMATE 05/16/2013
101	120	Platform VReg Constraints	J17_ULTIMATE 05/16/2013
102	121	TBT/DP Constraints	J17_ULTIMATE 05/16/2013
103	122	GDDR5/GPU Constraints	D8_AARON 03/13/2012
104	124	BLC Constraints	J17_ULTIMATE 05/16/2013
105	125	GPU VREG CONSTRAINTS	J17_ULTIMATE 05/16/2013
106	127	MISC-CONSTRAINTS 1	J17_ULTIMATE 05/16/2013

DRAWING
TITLE=J17
ABBREV=DRAWING
LAST_MODIFIED=Fri May 31 13:43:58 2013

DRAWING TITLE
SCHEM,MLB,J17

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DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
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PAGE 1 OF 127
SHEET 1 OF 106

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BOM VARIANTS

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4206	PCBA,MLB,GOOD,HYNIX,J17	J17_COMMON,J17,CPU:GOOD,GPU:GK107EGX,FB:2G_HYNIX,FBA,FBB,SSD:Y,EEEE:F8YL
639-4418	PCBA,MLB,GOOD,ELPIDA,J17	J17_COMMON,J17,CPU:GOOD,GPU:GK107EGX,FB:2G_ELPIDA,FBA,FBB,SSD:Y,EEEE:FCTC
985-0047	PCBA,MLB,DEV,J17	DEVELOPMENT,J17_DEVEL

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4532	1	HSW,SR14E,PRQ,C0,3.2G,84W,4+2,1.15,6M,LGA	CPU	CRITICAL	CPU:GOOD
337S4505	1	HSW,QE70,QS,C0,3.2G,84W,4+2,1.15,6M,LGA	CPU	CRITICAL	CPU:GOOD_TDP

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0080	1	SOCKET,MOLEX,LGA1150,CPU-HF	U0500	CRITICAL	

BOM Groups

BOM GROUP	BOM OPTIONS
J17_COMMON	COMMON,ALTERNATE,J17_COMMON1,J17_PROGPARTS
J17_COMMON1	XDP,SPEAKERID,TBTHV:P12V,CPUVCC:4PHASE,EXT_GPU:YES,VDDQ:P1V5
J17_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG,BLCMCU:PROG
J17_DEVEL	XDP_CONN,LPCPLUS,DDRVREF_DAC
DEVEL_SENSORS	TEMPSNSDEV,AP_ISNS:Y
J17_PRODUCTION	AP_ISNS:N

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4541	1	IC,SR198,Z87,LPT-D,C2,PRQ,23X23MM,FCBGA708	U1100	CRITICAL	
337S4562	1	IC,QEWL,LPT-D,C2,SQS,23X22MM,FCBGA708	U1100	CRITICAL	PCH_TDP
338S1113	1	IC,TBT,CR-4C,B1,PRQ,288 FCBGA,12X12MM	U2800	CRITICAL	
343S0616	1	IC,BCM57766A1,ENET&SD,8X8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S3880	1	IC,PROGRMD,EFI ROM,V0095,J17	U5210	CRITICAL	BOOTROM:PROG
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM:BLANK
341S3874	1	IC,PROG,SMC-A3,V2.14F9,PVT,J17	U5000	CRITICAL	SMC:PROG
338S1159	1	IC,SMC,LM4FS1BH5BBCIGR,SCPL	U5000	CRITICAL	SMC:BLANK
341S3860	1	IC,EEPROM,CR,V23.10,J17	U2890	CRITICAL	TBTROM:PROG
335S0865	1	IC,EEPROM,SERIAL,8KB,MLP8	U2890	CRITICAL	TBTROM:BLANK
341S3735	1	IC,ENET 1MBIT, SPI,ROM, V1.13 J17	U3990	CRITICAL	CIVROM:PROG
335S0862	1	IC,SERIAL FLASH,2MBIT, 2.7V, REF F	U3990	CRITICAL	CIVROM:BLANK
341S3778	1	IC,CAMERA FLASH,V7230,J16/17	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S3674	1	IC,BLC,MCU, PRPOGRAMMED, V0204, D8	U8100	CRITICAL	BLCMCU:PROG
337S3978	1	IC,BLC MCU LPC2132FBD64/01, LQFP64	U8100	CRITICAL	BLCMCU:BLANK

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_F8YL	CRITICAL	EEEE:F8YL
825-7896	1	LABEL,MLB,2D	EEEE_FCTC	CRITICAL	EEEE:FCTC

J17 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9884	1	SCH,MLB,J17	SCH1	CRITICAL	J17
820-3478	1	PCBF,MLB,J17	PCB1	CRITICAL	J17

J17 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB Diodes Array
377S0155	377S0104		ALL	USB Diode
157S0084	157S0058		ALL	Enet Magnetics
376S0975	376S1081		ALL	P/NCH DUAL FET
128S0365	128S0368		ALL	150UF CAPS BLK
138S0803	138S0804		ALL	2.2UF CAPS SOFT
126-0161	126-0160		ALL	56UF CAPS 10X12 THD
197S0481	197S0480		Y1950	25MHz PCH Xtal
197S0479	197S0478		ALL	12MHz Cam Xtal Y4200 and Y8105
372S0186	372S0185		ALL	Alt temp diode
107S0251	107S0249		R5520	Alt 2mOhm sense
107S0254	107S0241		R5450,R5480	Alt 5mOhm sense
107S0255	107S0240		R5450,R5480	Alt 1mOhm sense
341S3747	341S3735		U3990	ENET ROM,ATMEL,V1.13
138S0681	138S0638		ALL	10uF Caps
376S1106	376S0969		ALL	N-Ch FET
138S0860	138S0775		ALL	Single-source 1uF
138S0859	138S0788		ALL	Single-source 10uF

GPU and VRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4430	1	IC,GPU,NV,GK107-EGX,PS-A2	U8700	CRITICAL	GPU:GK107EGX
333S0630	4	IC,GDDR5,2GBIT,64MX32,GEMMA-DIE,170B FBGA	U9200,U9250,U9300,U9350	CRITICAL	FB:2G_HYNIX
333S0695	4	IC,GDDR5,2GBIT,64MX32,B-DIE,170B FBGA	U9200,U9250,U9300,U9350	CRITICAL	FB:2G_ELPIDA

SYNC_MASTER=J17_DINI SYNC_DATE=02/06/2013

PAGE TITLE
BOM Configuration

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REVISION A.0.0

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PAGE 2 OF 127

SHEET 2 OF 106

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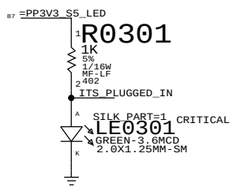
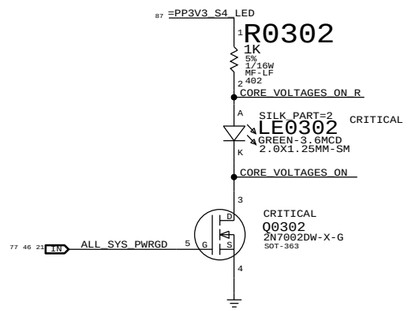
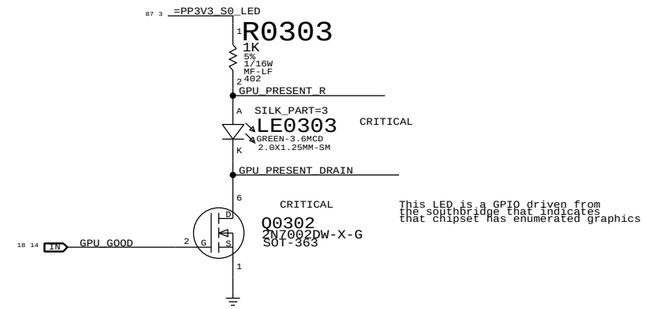
S5 Led



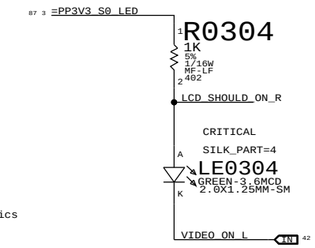
ALL_SYS_PWRGD Led



GPU GOOD Led



VIDEO ON Led



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
DEBUG LEDS

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

PAGE 3 OF 127

SHEET 3 OF 106

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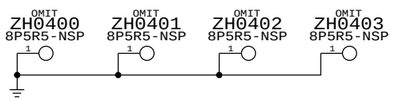
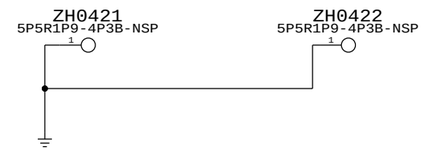
CPU Heatsink

4MM PLATED HOLES (998-4158)



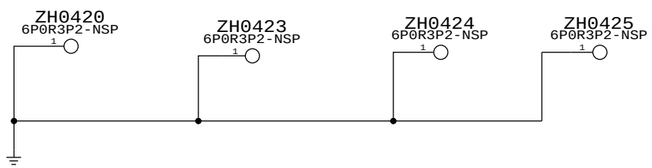
WIRELESS CARD MTG HOLES

998-4938 (PLATED HOLES, 1.9MM INNER DIAMETER, 4.3MM PAD)



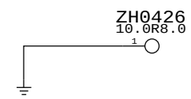
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



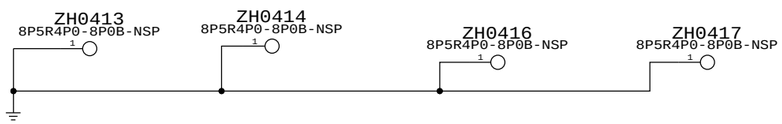
HEATPIPE MTG HOLES

998-4640 (PLATED HOLES, 10MM DIA, 12MM PAD)



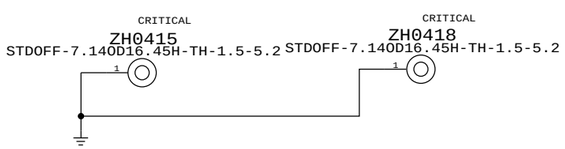
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



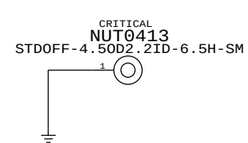
Rear Cover

860-1487 (PCB STANDOFF)



SSD STANDOFF

APN: 860-1624



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: Holes/PD parts

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DRAWING NUMBER: 051-9884 SIZE: D

REVISION: A.0.0

BRANCH

PAGE: 4 OF 127

SHEET: 4 OF 106

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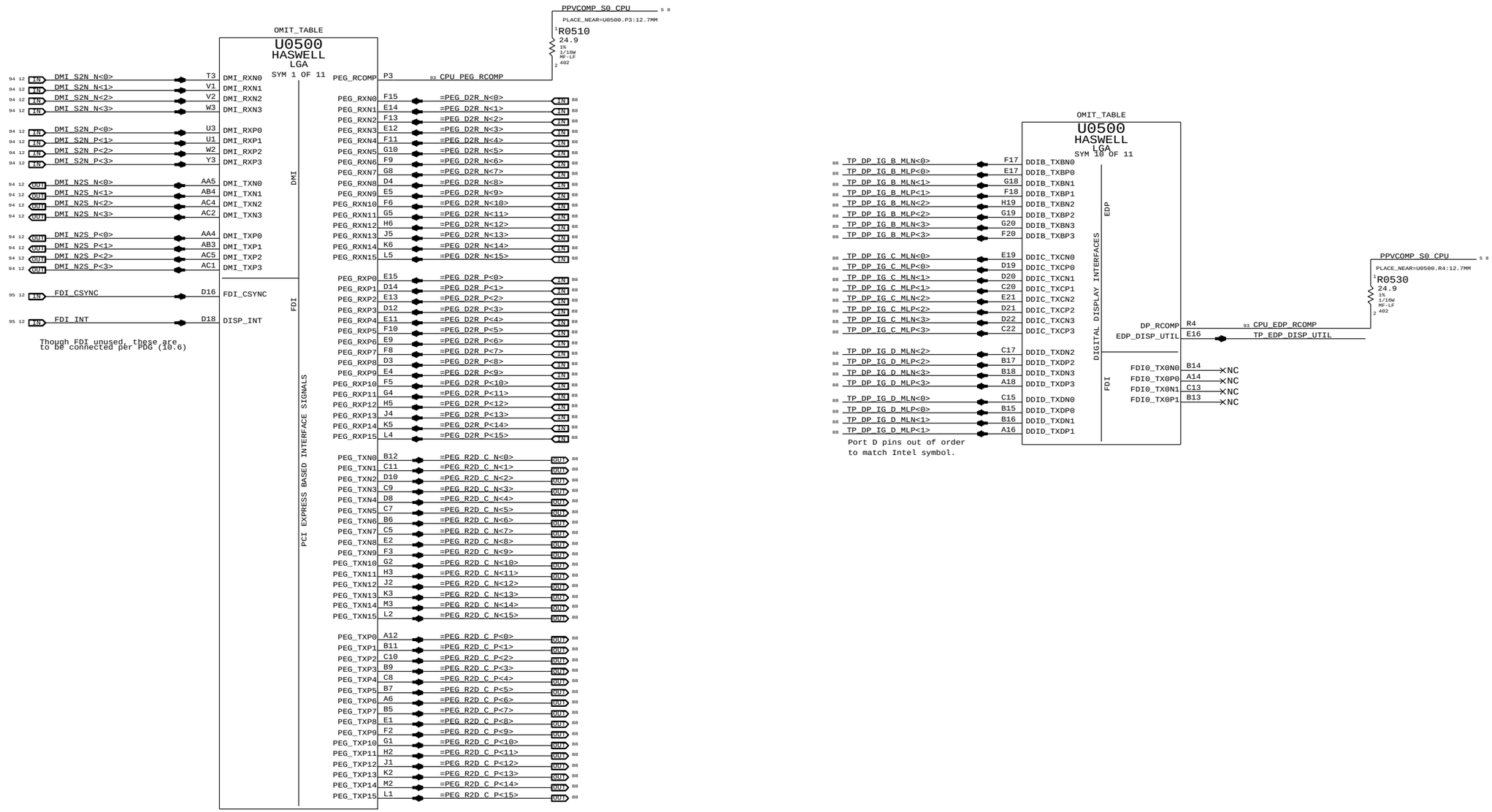

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE

CPU DMI/PEG/FDI/RSVD

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DRAWING NUMBER 051-9884

SIZE D

REVISION A.0.0

BRANCH

PAGE 5 OF 127

SHEET 5 OF 106

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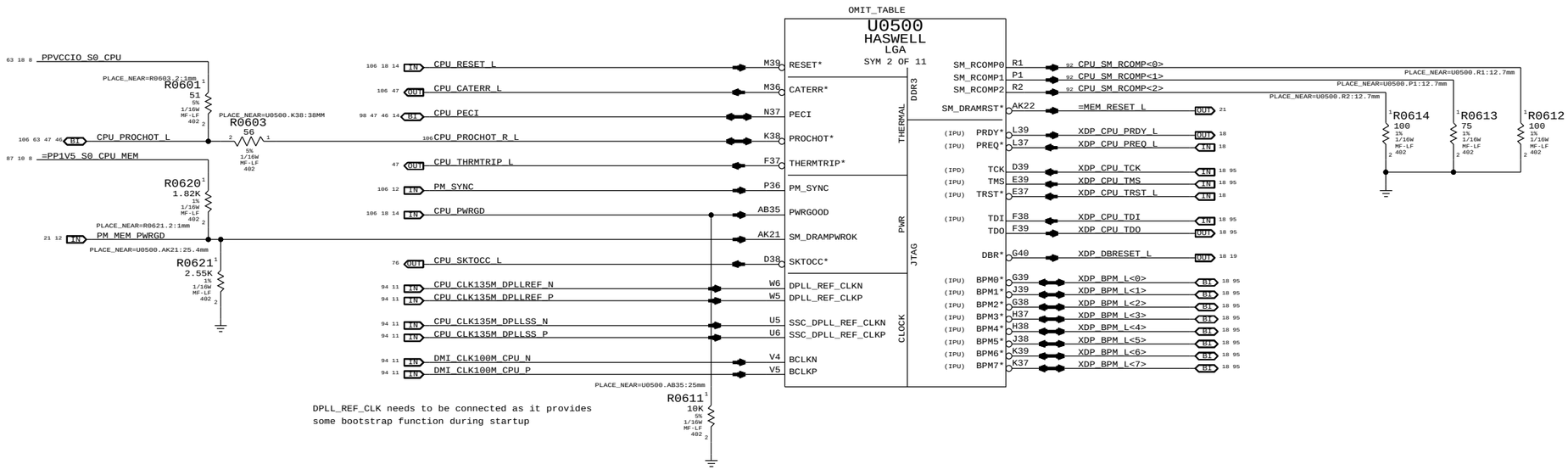

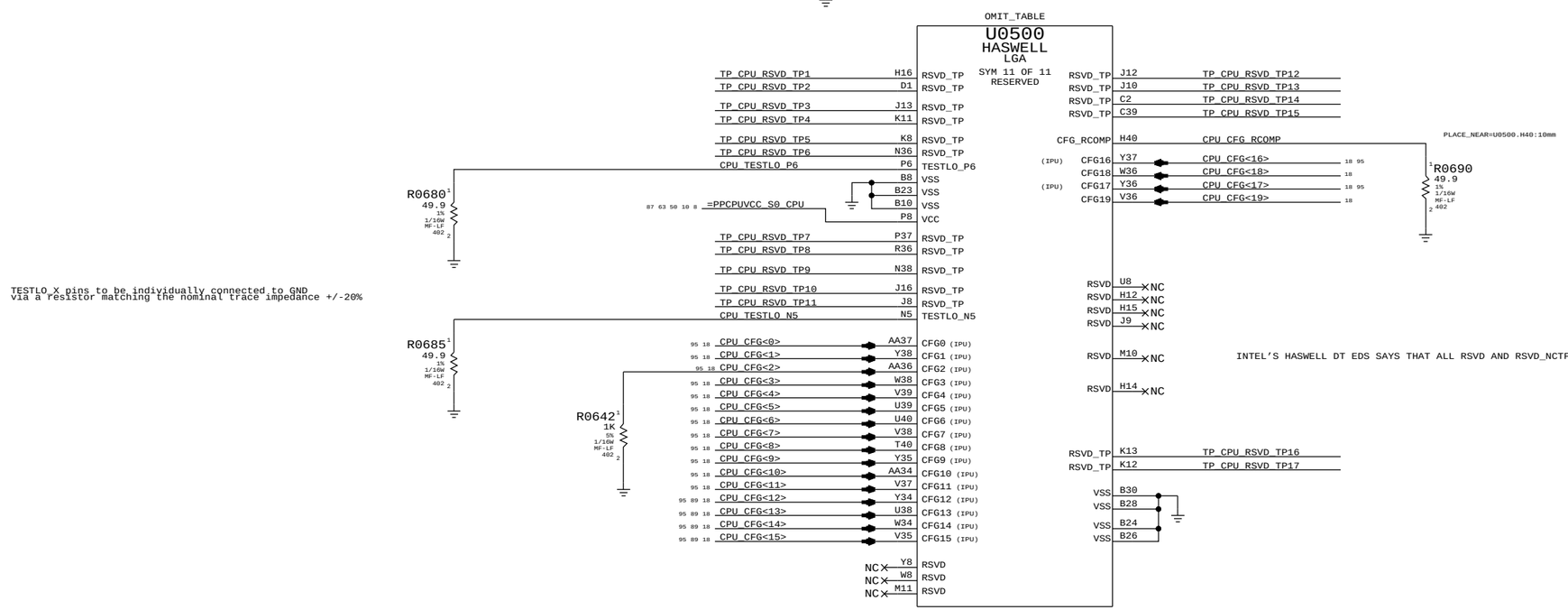

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (default) 10 = 2 X8	01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED(default)	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION(default)	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION(default)	0 = LANES REVERSED

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
CPU Clock/Misc/JTAG/CFG

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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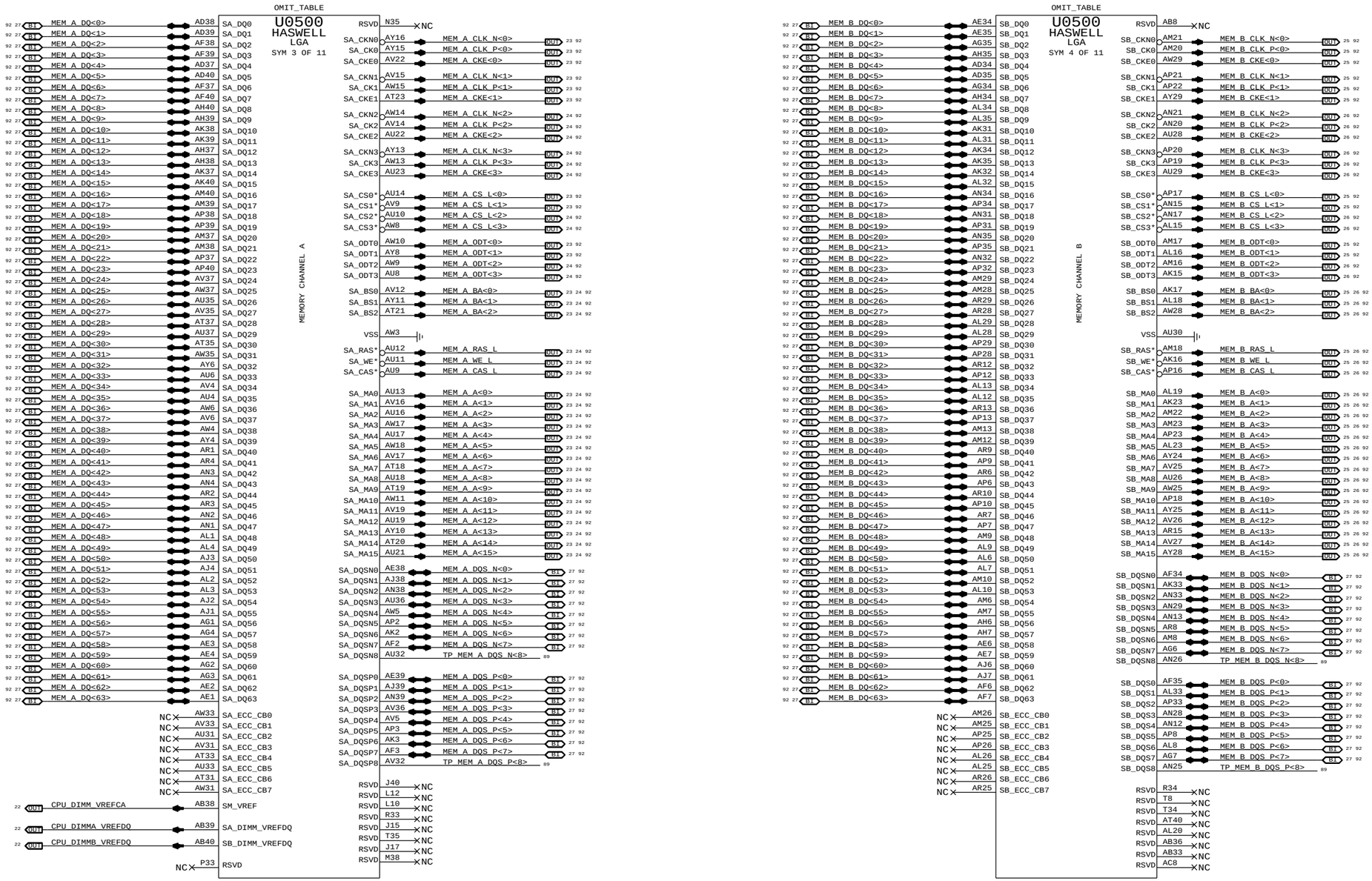

INTEL'S HASWELL DT EDS SAYS THAT ALL RSVD AND RSVD_NCTF SHOULD BE NC'D

SYNC MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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PAGE 7 OF 127

SHEET 7 OF 106

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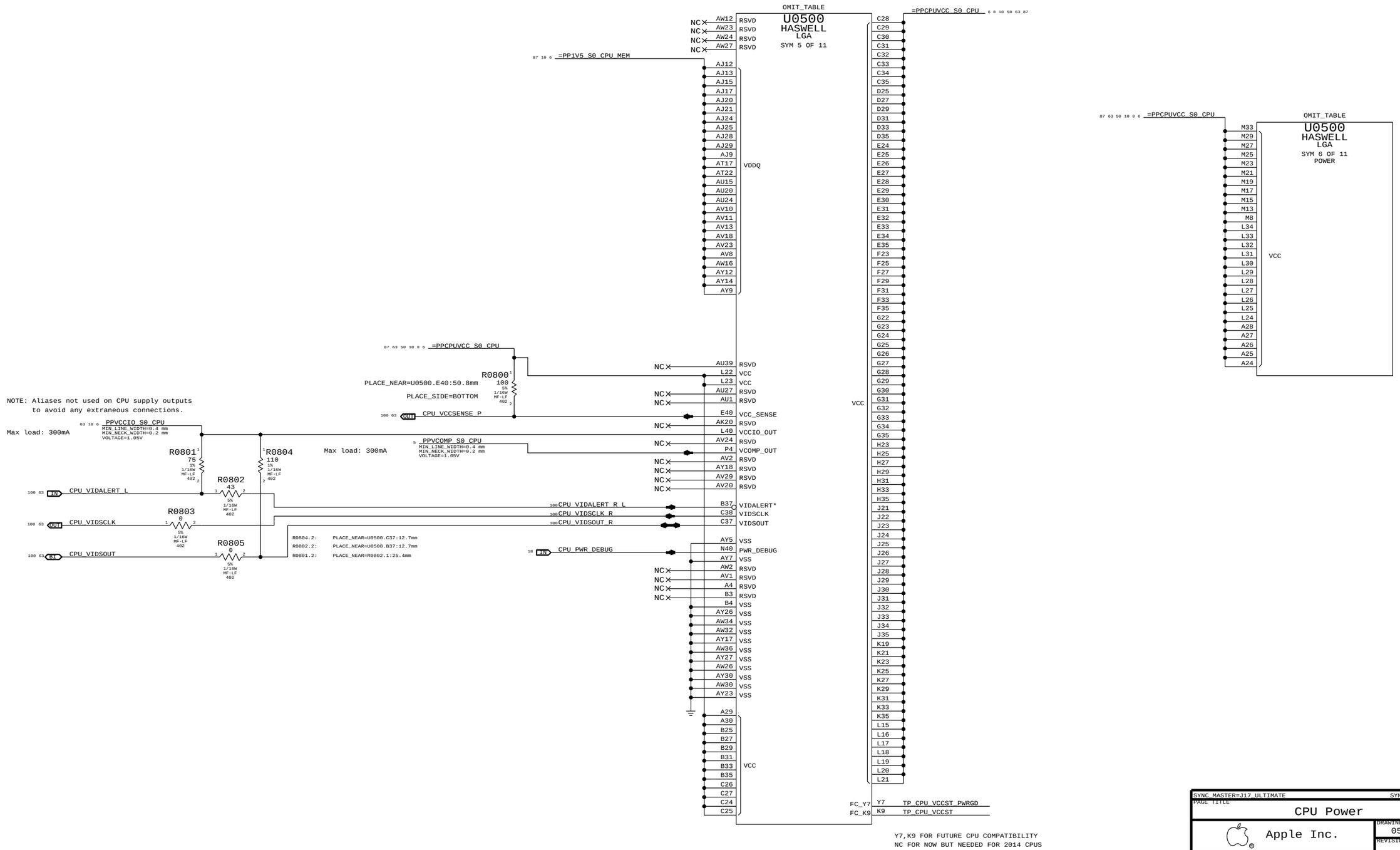

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

CPU Power

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

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PAGE 8 OF 127

SHEET 8 OF 106

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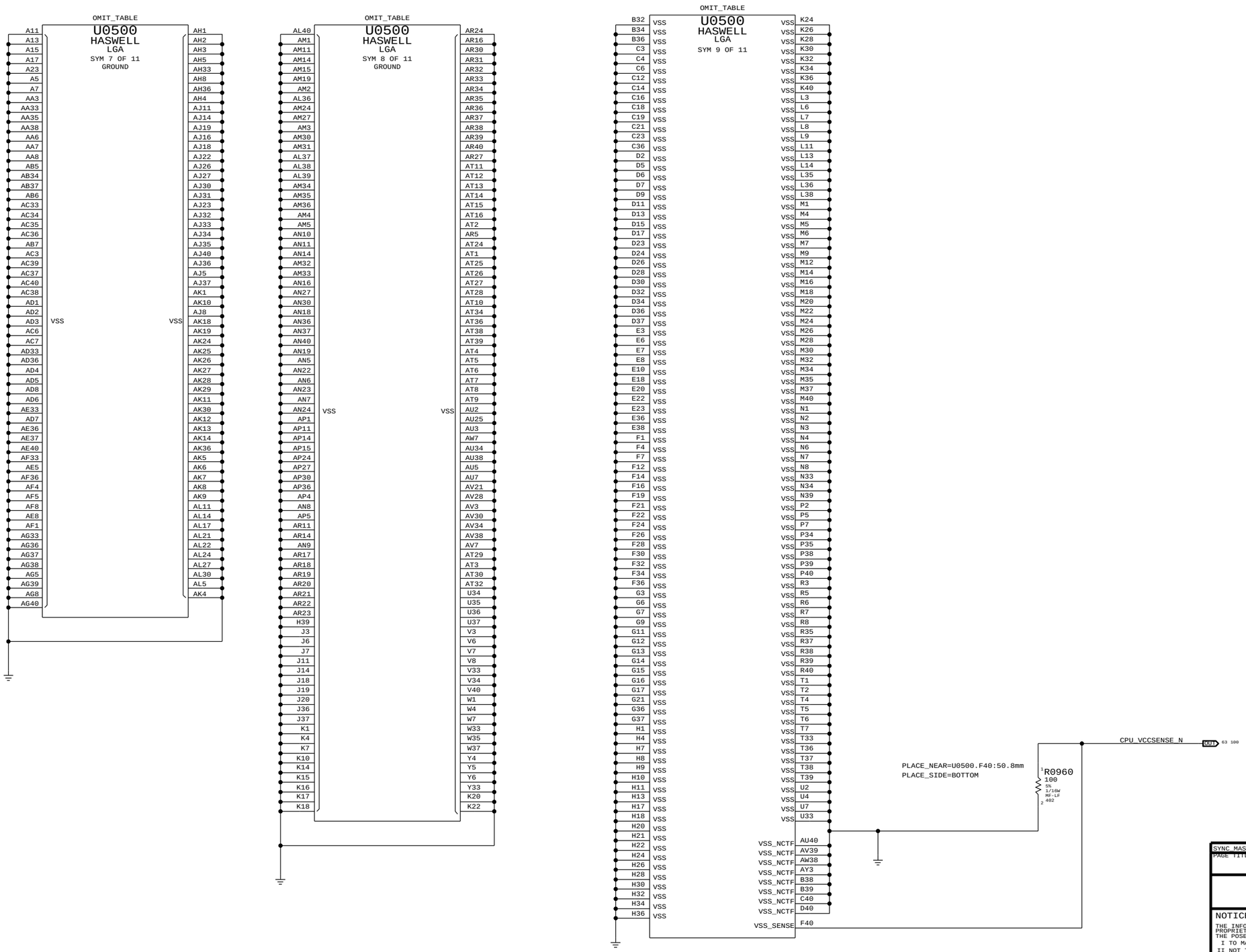

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PAGE TITLE

CPU Ground

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DRAWING NUMBER 051-9884

SIZE D

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PAGE 9 OF 127

SHEET 9 OF 106

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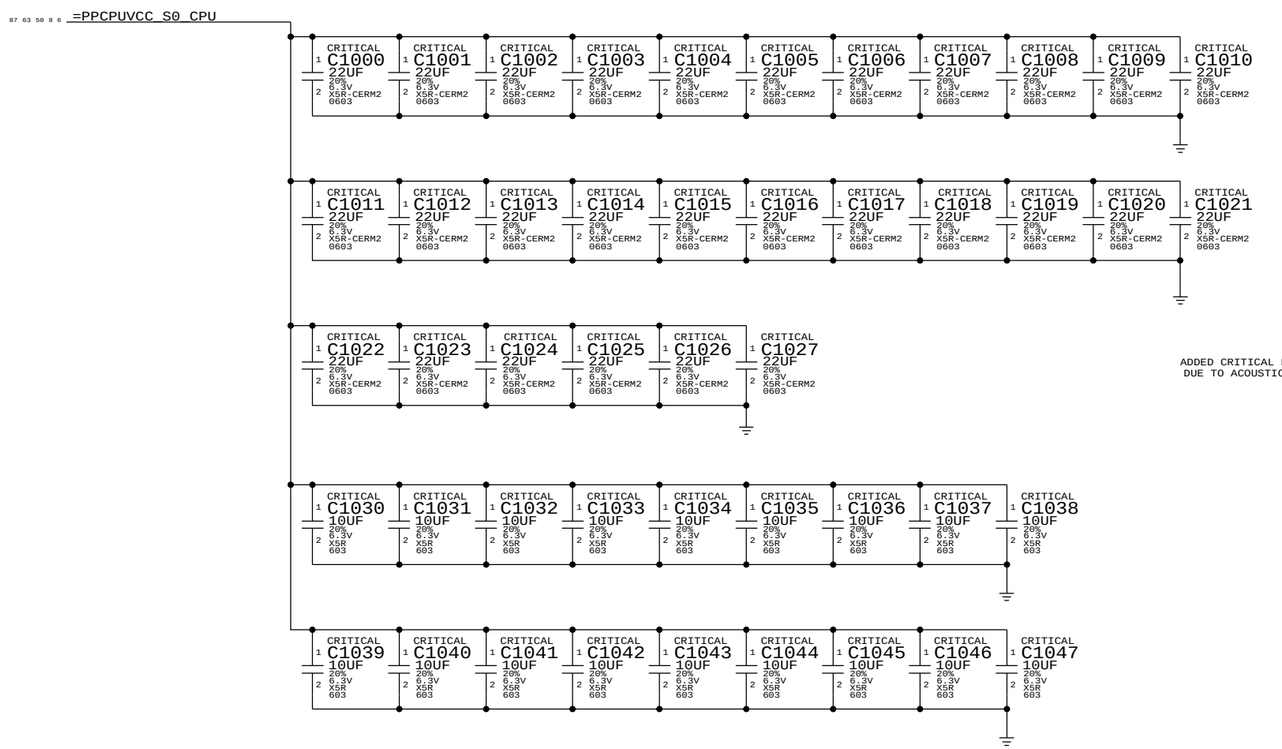
CPU VCORE DECOUPLING

Intel Recommendation:22x 22UF 0805,topside (18 inside cavity, 4 north of processor),8x 470uF bulk caps(5 stuffed,3 no-stuffed)
Apple Implementation:28x 22UF 0603 per Harold
18x 10UF 0603 placed inside socket cavity

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71

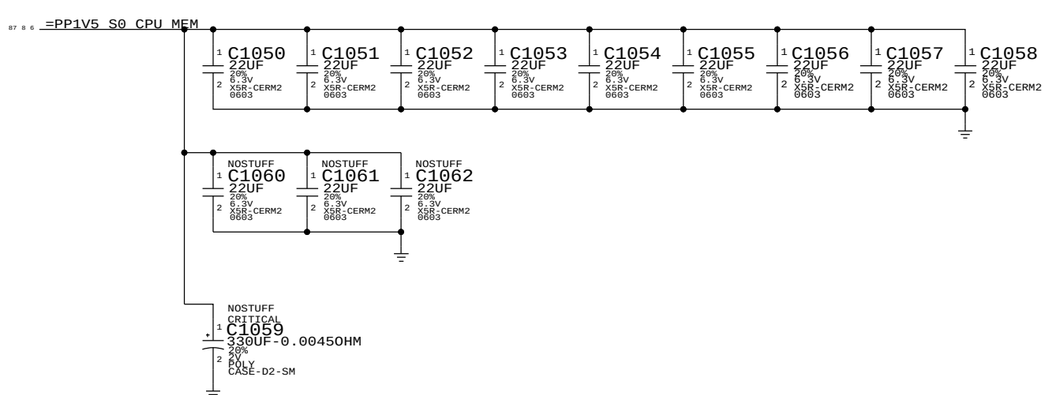


ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

Memory (CPU VCCDDR) DECOUPLING

Intel Recommendation:9x 22UF 0805 near CPU power pins
Apple Implementation:9x 22UF 0603 per Harold

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
CPU DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 10 OF 127
SHEET 10 OF 106

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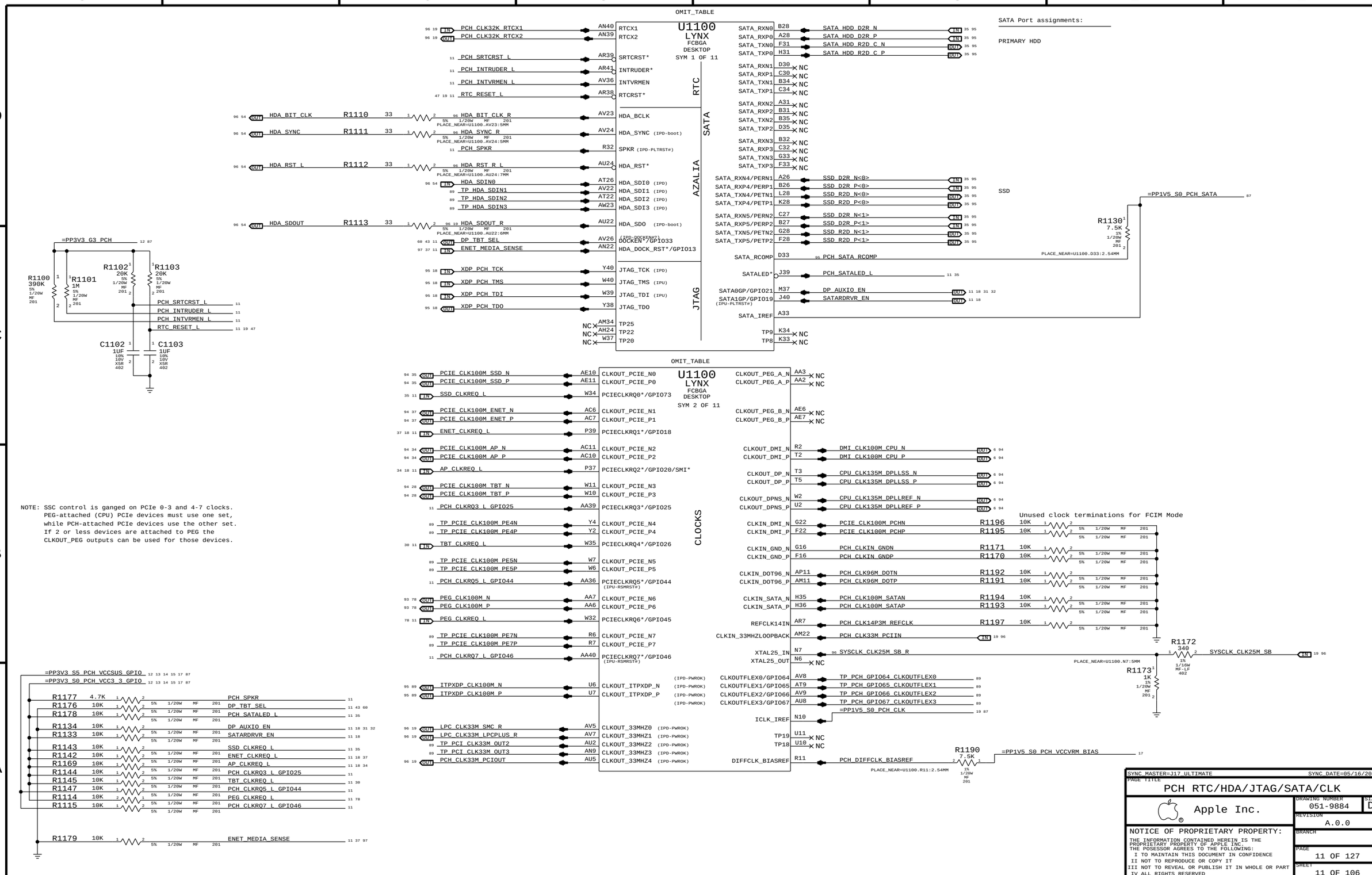
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 1 OF 11
RTC
SATA
AZALIA
JTAG
PCH_CLK32K_RTCX1
PCH_CLK32K_RTCX2
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
HDA_SDOUT
R1110 33
R1111 33
R1112 33
R1113 33
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
PLACE_NEAR=U1100.AV23:5MM
PLACE_NEAR=U1100.AV24:5MM
PLACE_NEAR=U1100.AU24:7MM
PLACE_NEAR=U1100.AU22:6MM
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
DP_TBT_SEL
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
SATA_RXN3
SATA_RXP3
SATA_TXN3
SATA_TXP3
SATA_RXN4/PERN1
SATA_RXP4/PERP1
SATA_TXN4/PETN1
SATA_TXP4/PETP1
SATA_RXN5/PERN2
SATA_RXP5/PERP2
SATA_TXN5/PETN2
SATA_TXP5/PETP2
SATA_RCOMP
SATALED*
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA_IREF
TP9
TP8
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SSD_D2R_N<0>
SSD_D2R_P<0>
SSD_R2D_N<0>
SSD_R2D_P<0>
SSD_D2R_N<1>
SSD_D2R_P<1>
SSD_R2D_N<1>
SSD_R2D_P<1>
PCH_SATA_RCOMP
PCH_SATALED_L
DP_AUXIO_EN
SATARDRVR_EN
SATA Port assignments:
PRIMARY HDD
SSD
=PP1V5_S0_PCH_SATA
R1130 7.5K
PLACE_NEAR=U1100.D33:2.54MM
=PP3V3_G3_PCH
R1100 390K
R1101 1M
R1102 20K
R1103 20K
C1102 1UF
C1103 1UF
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 2 OF 11
CLOCKS
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
SSD_CLKREQ_L
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
ENET_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
AP_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PCH_CLKRQ3_L_GPIO25
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
TBT_CLKREQ_L
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCH_CLKRQ5_L_GPIO44
PEG_CLK100M_N
PEG_CLK100M_P
PEG_CLKREQ_L
TP_PCIE_CLK100M_PE7N
TP_PCIE_CLK100M_PE7P
PCH_CLKRQ7_L_GPIO46
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
LPC_CLK33M_SMC_R
LPC_CLK33M_LPCPLUS_R
TP_PCI_CLK33M_OUT2
TP_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
PCIE_CLK100M_PCHN
PCIE_CLK100M_PCHP
PCH_CLKIN_GNDN
PCH_CLKIN_GNDP
PCH_CLK96M_DOTN
PCH_CLK96M_DOTP
PCH_CLK100M_SATAN
PCH_CLK100M_SATAP
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB_R
SYSCLK_CLK25M_SB
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
=PP1V5_S0_PCH_CLK
PCH_DIFFCLK_BIASREF
R1190 7.5K
=PP1V5_S0_PCH_VCCVRM_BIAS
Unused clock terminations for FCIM Mode
R1196 10K
R1195 10K
R1171 10K
R1170 10K
R1192 10K
R1191 10K
R1194 10K
R1193 10K
R1197 10K
R1172 340
R1173 1K
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.
=PP3V3_S5_PCH_VCCSUS_GPIO
=PP3V3_S0_PCH_VCC3_3_GPIO
R1177 4.7K PCH_SPKR
R1176 10K DP_TBT_SEL
R1178 10K PCH_SATALED_L
R1134 10K DP_AUXIO_EN
R1133 10K SATARDRVR_EN
R1143 10K SSD_CLKREQ_L
R1142 10K ENET_CLKREQ_L
R1169 10K AP_CLKREQ_L
R1144 10K PCH_CLKRQ3_L_GPIO25
R1145 10K TBT_CLKREQ_L
R1147 10K PCH_CLKRQ5_L_GPIO44
R1114 10K PEG_CLKREQ_L
R1115 10K PCH_CLKRQ7_L_GPIO46
R1179 10K ENET_MEDIA_SENSE
SYNC_MASTER=J17_ULTIMATE
SYNC_DATE=05/16/2013
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER 051-9884
SIZE D
REVISION A.0.0
BRANCH
PAGE 11 OF 127
SHEET 11 OF 106
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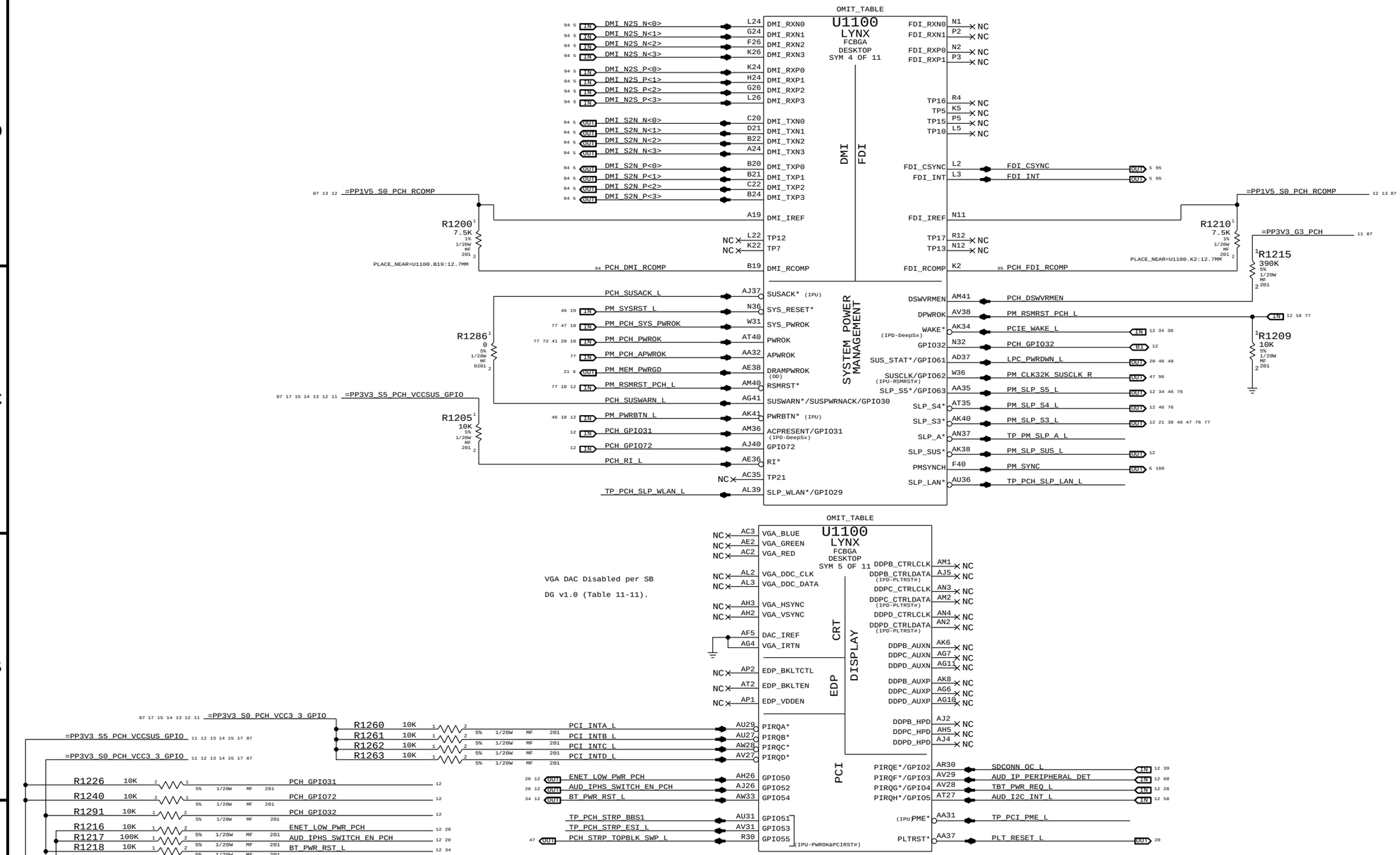

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PAGE TITLE

PCH DMI/FDI/PM/GFX/PCI

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DRAWING NUMBER 051-9884 SIZE D

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PAGE 12 OF 127

SHEET 12 OF 106

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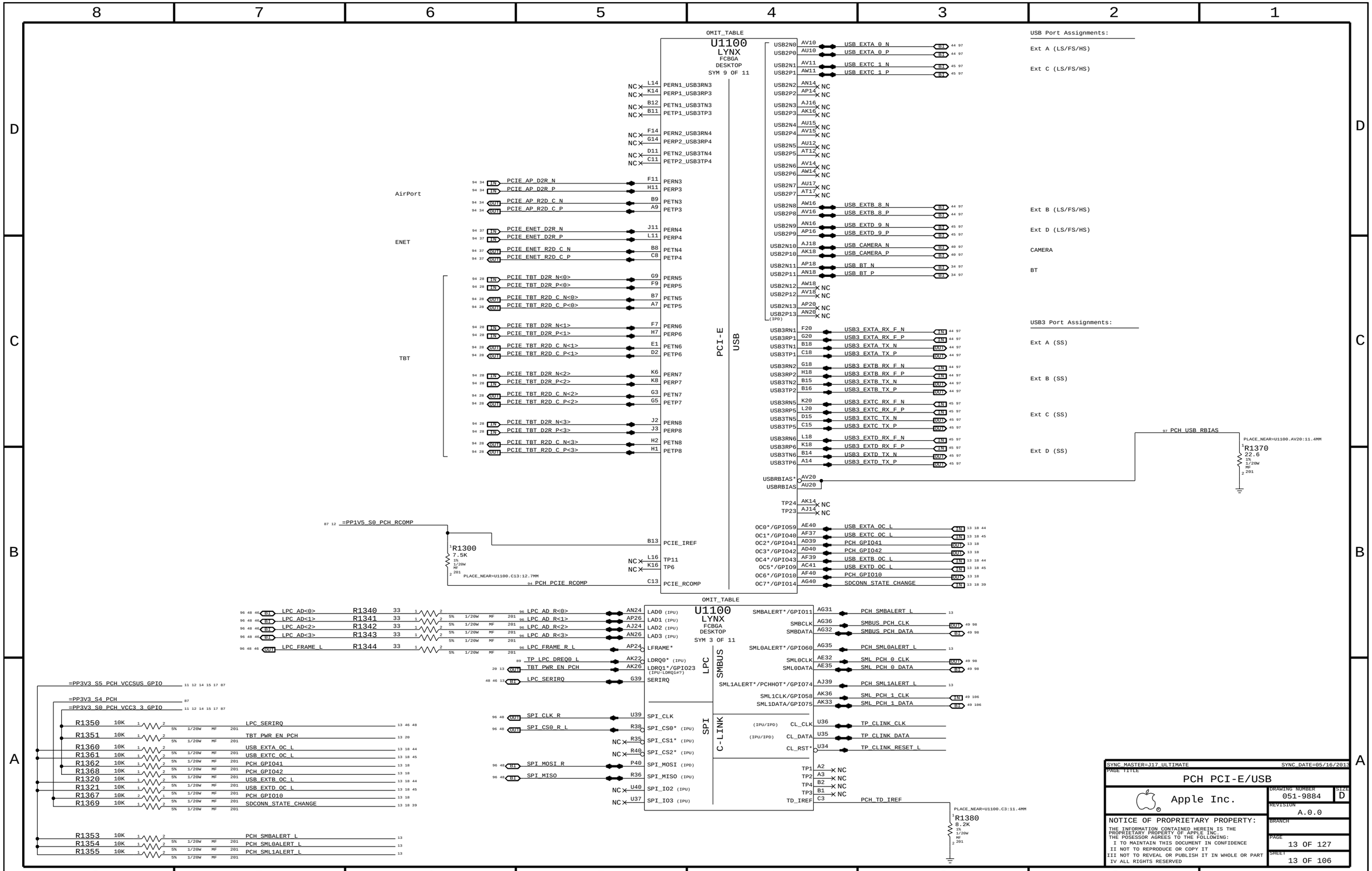
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 9 OF 11
PCI-E
USB
AirPort
ENET
TBT
PERN1_USB3RN3
PERP1_USB3RP3
PETN1_USB3TN3
PETP1_USB3TP3
PERN2_USB3RN4
PERP2_USB3RP4
PETN2_USB3TN4
PETP2_USB3TP4
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PERN3
PERP3
PETN3
PETP3
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PERN4
PERP4
PETN4
PETP4
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<0>
PERN5
PERP5
PETN5
PETP5
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<1>
PERN6
PERP6
PETN6
PETP6
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<2>
PERN7
PERP7
PETN7
PETP7
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
PERN8
PERP8
PETN8
PETP8
=PP1V5_S0_PCH_RCOMP
R1300
7.5K
PLACE_NEAR=U1100.C13:12.7MM
PCH_PCIE_RCOMP
PCIE_IREF
TP11
TP6
PCIE_RCOMP
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
CAMERA
BT
USB_EXTA_0_N
USB_EXTA_0_P
USB_EXTC_1_N
USB_EXTC_1_P
USB_EXTB_8_N
USB_EXTB_8_P
USB_EXTD_9_N
USB_EXTD_9_P
USB_CAMERA_N
USB_CAMERA_P
USB_BT_N
USB_BT_P
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
USB3_EXTA_RX_F_N
USB3_EXTA_RX_F_P
USB3_EXTA_TX_N
USB3_EXTA_TX_P
USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P
USB3_EXTB_TX_N
USB3_EXTB_TX_P
USB3_EXTC_RX_F_N
USB3_EXTC_RX_F_P
USB3_EXTC_TX_N
USB3_EXTC_TX_P
USB3_EXTD_RX_F_N
USB3_EXTD_RX_F_P
USB3_EXTD_TX_N
USB3_EXTD_TX_P
PCH_USB_RBIAS
PLACE_NEAR=U1100.AV20:11.4MM
R1370
22.6
USBRBIAS*
USBRBIAS
OC0*/GPIO59
OC1*/GPIO40
OC2*/GPIO41
OC3*/GPIO42
OC4*/GPIO43
OC5*/GPIO9
OC6*/GPIO10
OC7*/GPIO14
USB_EXTA_OC_L
USB_EXTC_OC_L
PCH_GPIO41
PCH_GPIO42
USB_EXTB_OC_L
USB_EXTD_OC_L
PCH_GPIO10
SDCONN_STATE_CHANGE
OMIT_TABLE
U1100
LYNX
FCBGA
DESKTOP
SYM 3 OF 11
LPC
SMBUS
SPI
C-LINK
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
R1340
R1341
R1342
R1343
R1344
LAD0 (IPU)
LAD1 (IPU)
LAD2 (IPU)
LAD3 (IPU)
LFRAME*
LDRQ0* (IPU)
LDRQ1*/GPIO23 (IPU-LDRQ1#?)
SERIRQ
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
SPI_CLK_R
SPI_CS0_R_L
SPI_MOSI_R
SPI_MISO
SPI_CLK
SPI_CS0* (IPU)
SPI_CS1* (IPU)
SPI_CS2* (IPU)
SPI_MOSI (IPD)
SPI_MISO (IPU)
SPI_IO2 (IPU)
SPI_IO3 (IPU)
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CL_CLK
CL_DATA
CL_RST*
TP1
TP2
TP3
TP4
TD_IREF
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
PCH_SML0ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
PCH_SML1ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
TP_CLINK_CLK
TP_CLINK_DATA
TP_CLINK_RESET_L
PCH_TD_IREF
PLACE_NEAR=U1100.C3:11.4MM
R1380
8.2K
=PP3V3_S5_PCH_VCCSUS_GPIO
=PP3V3_S4_PCH
=PP3V3_S0_PCH_VCC3_3_GPIO
R1350
R1351
R1360
R1361
R1362
R1368
R1320
R1321
R1367
R1369
R1353
R1354
R1355
LPC_SERIRQ
TBT_PWR_EN_PCH
USB_EXTA_OC_L
USB_EXTC_OC_L
PCH_GPIO41
PCH_GPIO42
USB_EXTB_OC_L
USB_EXTD_OC_L
PCH_GPIO10
SDCONN_STATE_CHANGE
PCH_SMBALERT_L
PCH_SML0ALERT_L
PCH_SML1ALERT_L
SYNC_MASTER=J17_ULTIMATE
SYNC_DATE=05/16/2013
PAGE TITLE
PCH PCI-E/USB
Apple Inc.
DRAWING NUMBER
051-9884
SIZE
D
REVISION
A.0.0
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PAGE
13 OF 127
SHEET
13 OF 106
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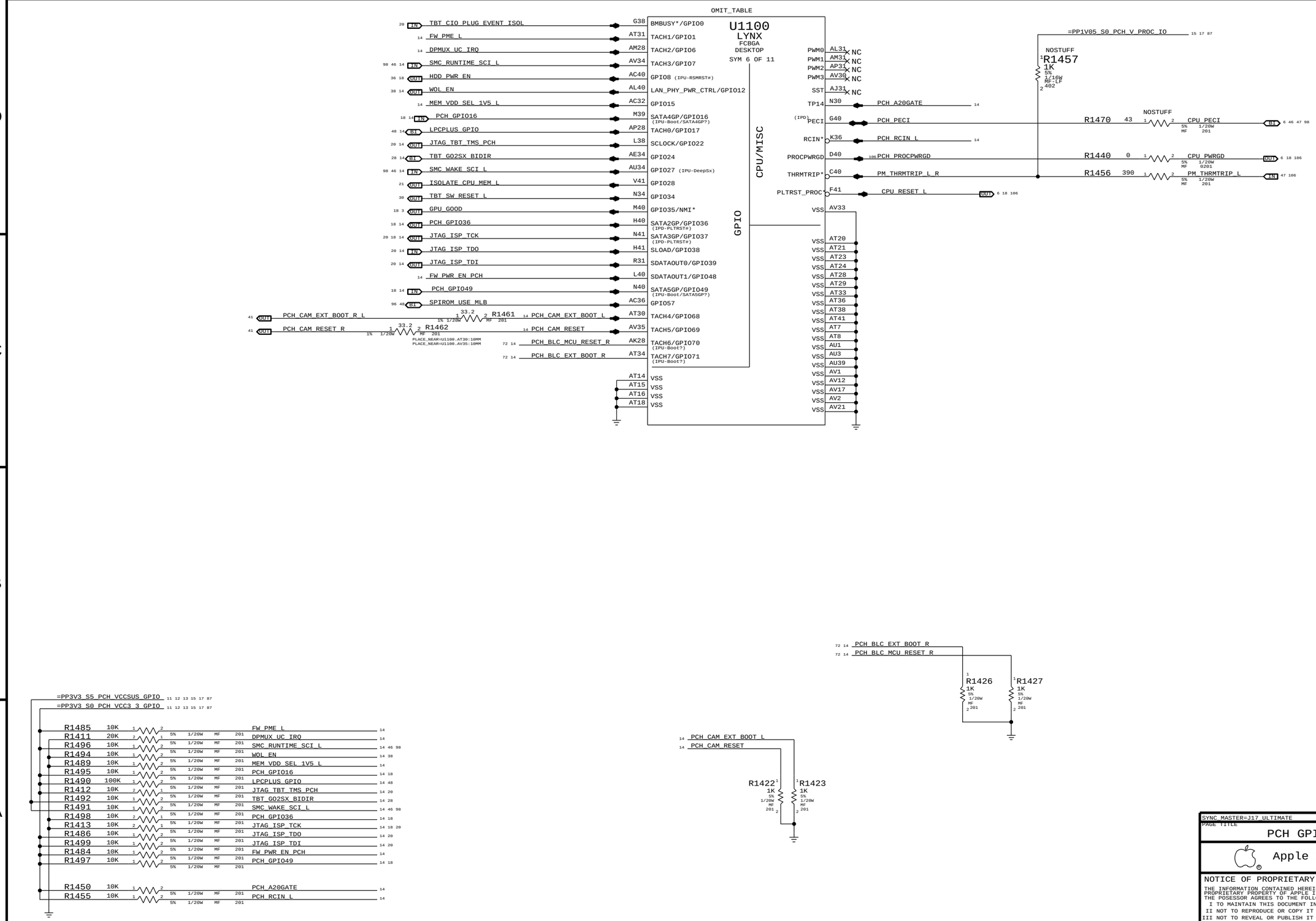

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PAGE TITLE

PCH GPIO/MISC/NCTF

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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PAGE 14 OF 127

SHEET 14 OF 106

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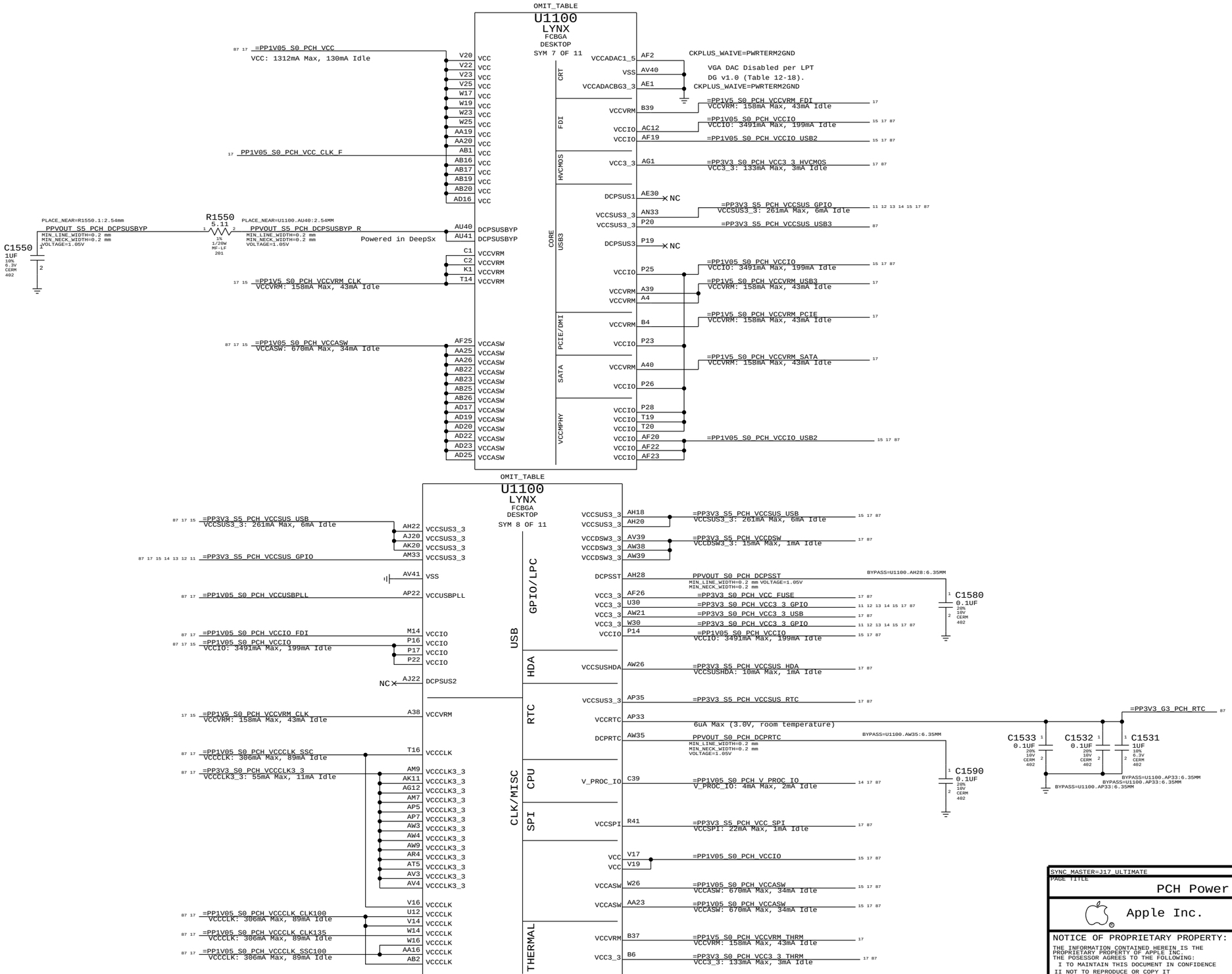

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PCH Power

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DRAWING NUMBER 051-9884

SIZE D

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BRANCH

PAGE 15 OF 127

SHEET 15 OF 106

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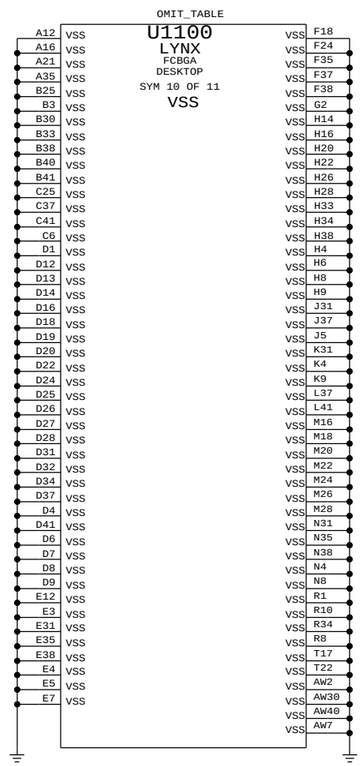

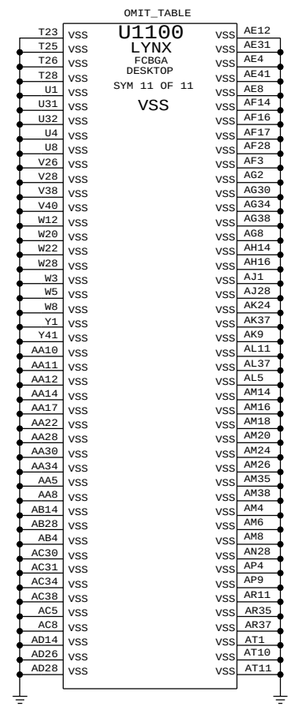

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

PCH Grounds

Apple Inc.

DRAWING NUMBER 051-9884

SIZE D

REVISION A.0.0

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PAGE 16 OF 127

SHEET 16 OF 106

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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR) INTEL:1X 0.1UF(402)
=PP3V3_S5_PCH_VCCDSW
15mA Max, 1mA Idle
C1700 0.1UF 20% 10V CERM 402
BYPASS=U1100.AW39:6.35MM

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR) INTEL:1X 1UF(402)
=PP3V3_S5_PCH_VCC_SPI
22mA Max, 1mA Idle
C1702 1UF 10% 6.3V CERM 402
BYPASS=U1100.R41:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR) INTEL:1X 0.1UF(402)
=PP3V3_S5_PCH_VCCSUS_GPIO
261mA Max, 6mA Idle
C1704 0.1UF 20% 10V CERM 402
BYPASS=U1100.AN33:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR) INTEL:1X 0.1UF(402)
=PP3V3_S5_PCH_VCCSUS_USB
261mA Max, 6mA Idle
C1706 0.1UF 20% 10V CERM 402
BYPASS=U1100.AK20:6.35MM

PCH VCCSUS3_3 BYPASS
(PCH 3.3V DSW RTC PWR) INTEL:1X 1UF(402)
=PP3V3_S5_PCH_VCCSUS_RTC
C1708 1UF 10% 6.3V CERM 402
BYPASS=U1100.AP35:6.35MM

PCH VCCSUSHDA BYPASS
(PCH 3.3V HDA PWR) INTEL:1X 0.1UF(402)
=PP3V3_S5_PCH_VCCSUS_HDA
10mA Max, 1mA Idle
C1710 0.1UF 20% 10V CERM 402
BYPASS=U1100.AW26:6.35MM

PCH VCCCLK3_3 BYPASS 55mA Max, 11mA Idle
(PCH 3.3V CLK PWR) INTEL:4X 1UF(402)
=PP3V3_S0_PCH_VCCCLK3_3
C1720 1UF 10% 6.3V CERM 402
C1721 1UF 10% 6.3V CERM 402
C1722 1UF 10% 6.3V CERM 402
C1723 1UF 10% 6.3V CERM 402
BYPASS=U1100.AP5:6.35MM
BYPASS=U1100.AV4:6.35MM
BYPASS=U1100.AR4:6.35MM
BYPASS=U1100.AT5:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR) INTEL:1X 0.1UF(402)
=PP3V3_S0_PCH_VCC3_3_HVCMOS
133mA Max, 3mA Idle
C1726 0.1UF 20% 10V CERM 402
BYPASS=U1100.AG1:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR) INTEL:1X 0.1UF(402)
=PP3V3_S0_PCH_VCC3_3_GPIO
133mA Max, 3mA Idle
C1728 0.1UF 20% 10V CERM 402
BYPASS=U1100.W30:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR) INTEL:1X 1UF(402)
=PP3V3_S0_PCH_VCC3_3_USB
133mA Max, 3mA Idle
C1730 1UF 10% 6.3V CERM 402
BYPASS=U1100.AW21:6.35MM

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR) INTEL:1X 0.1UF(402)
=PP3V3_S0_PCH_VCC3_3_THRM
133mA Max, 3mA Idle
C1732 0.1UF 20% 10V CERM 402
BYPASS=U1100.B6:6.35MM

PCH VCC BYPASS
(PCH 3.3V FUSE PWR) INTEL:1X 1UF(402)
=PP3V3_S0_PCH_VCC_FUSE
133mA Max, 3mA Idle
C1734 1UF 10% 6.3V CERM 402
BYPASS=U1100.AF26:6.35MM

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR) INTEL:1X 0.1UF(402)
=PP1V5_S0_PCH_VCCVRM
158mA Max, 43mA Idle
=PP1V5_S0_PCH_VCCVRM_BIAS
=PP1V5_S0_PCH_VCCVRM_FDI
=PP1V5_S0_PCH_VCCVRM_USB3
=PP1V5_S0_PCH_VCCVRM_PCIE
=PP1V5_S0_PCH_VCCVRM_SATA
=PP1V5_S0_PCH_VCCVRM_CLK
=PP1V5_S0_PCH_VCCVRM_THRM
C1740 0.1UF 20% 16V CERM 603
BYPASS=U1100.T14:12.7MM

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR) INTEL:1X10UF(805), 1X1UF(402)
=PP1V05_S0_PCH_VCCASW
670mA Max, 34mA Idle
C1750 10UF 20% 6.3V XSR 603
C1751 1UF 10% 6.3V CERM 402
C1752 1UF 10% 6.3V CERM 402
place_near=U1100.AD17:2.54MM
place_near=U1100.AD17:2.54MM
place_near=U1100.AD19:2.54MM

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
=PP1V05_S0_PCH_VCC
1312mA Max, 130mA Idle
THESE 4X1UF ARE EXTRA BYPASS
C1761 1UF 10% 6.3V CERM 402
C1756 1UF 10% 6.3V CERM 402
C1757 1UF 10% 6.3V CERM 402
C1758 1UF 10% 6.3V CERM 402
BYPASS=U1100.P14:6.35MM
BYPASS=U1100.V22:6.35MM
BYPASS=U1100.V25:6.35MM
BYPASS=U1100.AA19:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR) INTEL:2X10UF(805), 3X1UF(402)
=PP1V05_S0_PCH_VCCIO
3491mA Max, 114mA Idle
C1760 10UF 20% 6.3V XSR 603
C1755 10UF 20% 6.3V XSR 603
C1762 1UF 10% 6.3V CERM 402
C1763 1UF 10% 6.3V CERM 402
C1764 1UF 10% 6.3V CERM 402
BYPASS=U1100.P14:12.7MM
BYPASS=U1100.P28:12.7MM
BYPASS=U1100.P16:6.35MM
BYPASS=U1100.P17:6.35MM
BYPASS=U1100.P26:6.35MM

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR) INTEL:1X 1UF(402)
=PP1V05_S0_PCH_VCCUSBPLL
C1770 1UF 10% 6.3V CERM 402
BYPASS=U1100.AP22:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR) INTEL:1X 1UF(402)
=PP1V05_S0_PCH_VCCIO_FDI
3491mA Max, 114mA Idle
C1772 1UF 10% 6.3V CERM 402
BYPASS=U1100.M14:6.35MM

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR) INTEL:1X 1UF(402)
=PP1V05_S0_PCH_VCCIO_USB2
3491mA Max, 114mA Idle
C1774 1UF 10% 6.3V CERM 402
BYPASS=U1100.AF19:6.35MM

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR) INTEL:1X1UF(603), 2X0.1UF(402)
=PP1V05_S0_PCH_V_PROC_IO
4mA Max, 2mA Idle
C1785 1UF 10% 6.3V CERM 402
C1786 0.1UF 20% 10V CERM 402
C1787 0.1UF 20% 10V CERM 402
BYPASS=U1100.C39:12.7MM
BYPASS=U1100.C39:6.35MM
BYPASS=U1100.C39:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR) INTEL:2X 1UF(402)
=PP1V05_S0_PCH_VCCCLK_SSC100
306mA Max, 89mA Idle
C1776 1UF 10% 6.3V CERM 402
C1777 1UF 10% 6.3V CERM 402
BYPASS=U1100.AA16:6.35MM
BYPASS=U1100.W16:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR) INTEL:2X 1UF(402)
=PP1V05_S0_PCH_VCCCLK_CLK100
306mA Max, 89mA Idle
C1778 1UF 10% 6.3V CERM 402
C1783 1UF 10% 6.3V CERM 402
BYPASS=U1100.U12:6.35MM
BYPASS=U1100.AB2:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR) INTEL:1X 1UF(402)
=PP1V05_S0_PCH_VCCCLK_CLK135
306mA Max, 89mA Idle
C1780 1UF 10% 6.3V CERM 402
BYPASS=U1100.W14:6.35MM

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR) INTEL:1X 1UF(402)
=PP1V05_S0_PCH_VCCCLK_SSC
306mA Max, 89mA Idle
C1782 1UF 10% 6.3V CERM 402
BYPASS=U1100.V16:6.35MM

PCH CLK VCC BYPASS INTEL:1X10UF(603), 1X1UF(402)
(PCH 1.05V CLK PLL PWR. NOSTUFF 10UF IF IDG NO USED)
=PP1V05_S0_PCH_VCC_CLK
306mA Max, 89mA Idle
L1790 0 5% 1/10W MF-LF 603
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
C1790 10UF 20% 6.3V XSR 603 NOSTUFF
C1791 1UF 10% 10V XSR 402
BYPASS=U1100.AB1:12.7mm
BYPASS=U1100.AB1:6.35mm

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013
PAGE TITLE
PCH DECOUPLING
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DRAWING NUMBER 051-9884
SIZE D
REVISION A.0.0
BRANCH
PAGE 17 OF 127
SHEET 17 OF 106

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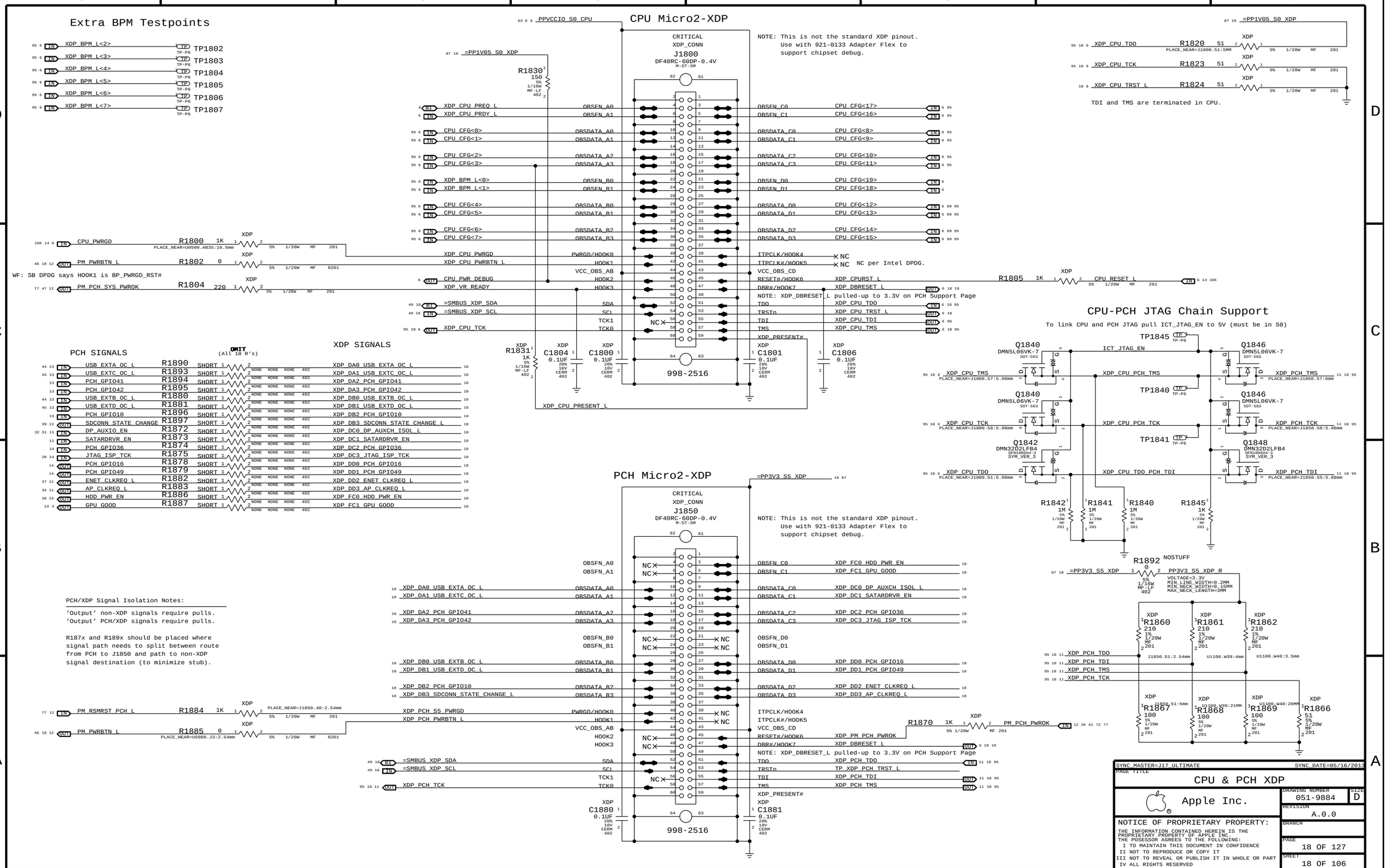
Extra BPM Testpoints
XDP_BPM_L<2> TP1802
XDP_BPM_L<3> TP1803
XDP_BPM_L<4> TP1804
XDP_BPM_L<5> TP1805
XDP_BPM_L<6> TP1806
XDP_BPM_L<7> TP1807
CPU Micro2-XDP
CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
998-2516
NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.
=PP1V05_S0_XDP
R1830 150
PPVCCIO_S0_CPU
XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
XDP_BPM_L<0>
XDP_BPM_L<1>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
CPU_PWR_DEBUG
XDP_VR_READY
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_CPU_TCK
XDP_CPU_PRESENT_L
R1831 1K
C1804 0.1UF
C1800 0.1UF
C1801 0.1UF
C1806 0.1UF
R1820 51 XDP_CPU_TDO
R1823 51 XDP_CPU_TCK
R1824 51 XDP_CPU_TRST_L
TDI and TMS are terminated in CPU.
CPU_PWRGD R1800 1K
PM_PWRBTN_L R1802 0
WF: SB DPDG says HOOK1 is BP_PWRGD_RST#
PM_PCH_SYS_PWROK R1804 220
R1805 1K CPU_RESET_L
NC per Intel DPDG.
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page
CPU-PCH JTAG Chain Support
To link CPU and PCH JTAG pull ICT_JTAG_EN to 5V (must be in S0)
TP1845
TP1840
TP1841
ICT_JTAG_EN
XDP_CPU_TMS
XDP_CPU_TCK
XDP_CPU_TDO
XDP_PCH_TMS
XDP_PCH_TCK
XDP_PCH_TDI
XDP_CPU_TDO_PCH_TDI
Q1840 DMN5L06VK-7
Q1842 DMN32D2LFB4
Q1846 DMN5L06VK-7
Q1848 DMN32D2LFB4
R1842 1M
R1841 1M
R1840 1M
R1845 1K
PCH SIGNALS
OMIT (All 18 R's)
XDP SIGNALS
USB_EXTA_OC_L R1890 XDP_DA0_USB_EXTA_OC_L
USB_EXTC_OC_L R1893 XDP_DA1_USB_EXTC_OC_L
PCH_GPIO41 R1894 XDP_DA2_PCH_GPIO41
PCH_GPIO42 R1895 XDP_DA3_PCH_GPIO42
USB_EXTB_OC_L R1880 XDP_DB0_USB_EXTB_OC_L
USB_EXTD_OC_L R1881 XDP_DB1_USB_EXTD_OC_L
PCH_GPIO10 R1896 XDP_DB2_PCH_GPIO10
SDCONN_STATE_CHANGE R1897 XDP_DB3_SDCONN_STATE_CHANGE_L
DP_AUXIO_EN R1872 XDP_DC0_DP_AUXCH_ISOL_L
SATARDRVR_EN R1873 XDP_DC1_SATARDRVR_EN
PCH_GPIO36 R1874 XDP_DC2_PCH_GPIO36
JTAG_ISP_TCK R1875 XDP_DC3_JTAG_ISP_TCK
PCH_GPIO16 R1878 XDP_DD0_PCH_GPIO16
PCH_GPIO49 R1879 XDP_DD1_PCH_GPIO49
ENET_CLKREQ_L R1882 XDP_DD2_ENET_CLKREQ_L
AP_CLKREQ_L R1883 XDP_DD3_AP_CLKREQ_L
HDD_PWR_EN R1886 XDP_FC0_HDD_PWR_EN
GPU_GOOD R1887 XDP_FC1_GPU_GOOD
PCH Micro2-XDP
CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
998-2516
NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.
=PP3V3_S5_XDP
R1892 0 NOSTUFF
PP3V3_S5_XDP_R
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM
MAX_NECK_LENGTH=3MM
R1860 210
R1861 210
R1862 210
R1867 100
R1868 100
R1869 100
R1866 51
XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_PCH_TCK
PM_RSMRST_PCH_L R1884 1K
PM_PWRBTN_L R1885 0
R1870 1K PM_PCH_PWROK
PCH/XDP Signal Isolation Notes:
'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.
R187x and R189x should be placed where
signal path needs to split between route
from PCH to J1850 and path to non-XDP
signal destination (to minimize stub).
SYNC_MASTER=J17_ULTIMATE
SYNC_DATE=05/16/2013
PAGE TITLE
CPU & PCH XDP
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DRAWING NUMBER 051-9884
SIZE D
REVISION A.0.0
BRANCH
PAGE 18 OF 127
SHEET 18 OF 106
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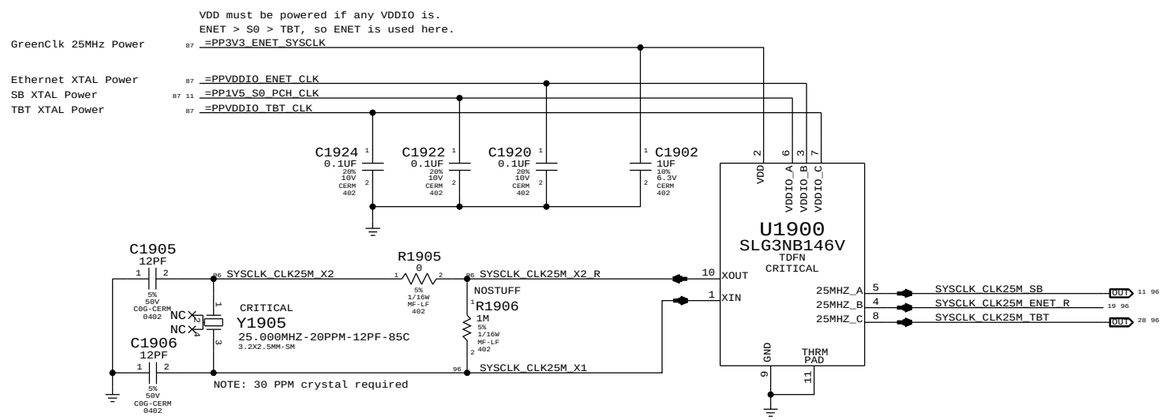
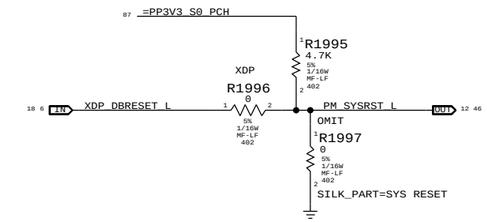
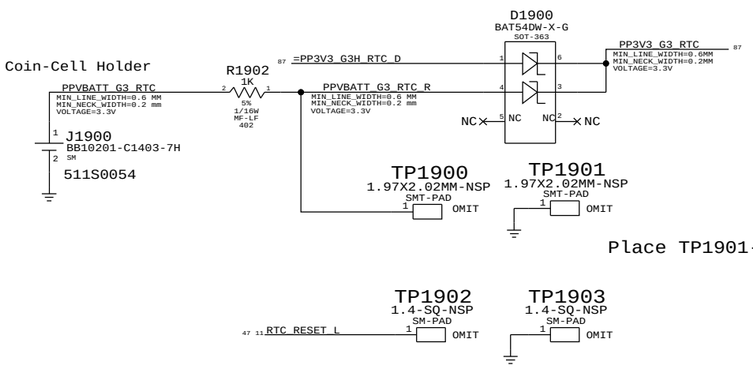
System 25MHz Clock Generator



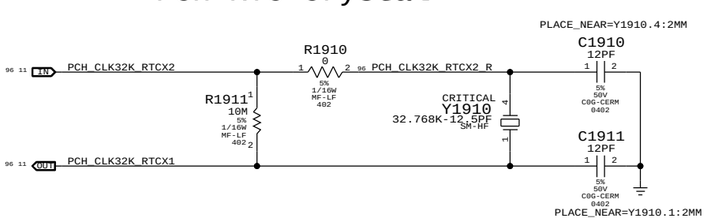
PCH Reset Button



RTC Power Sources

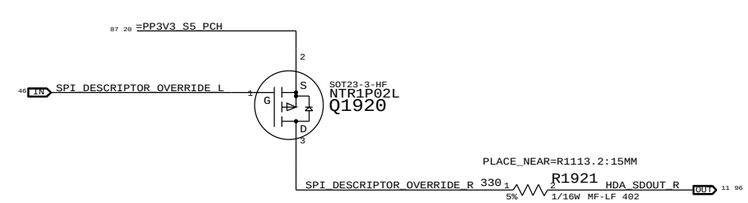


PCH RTC Crystal

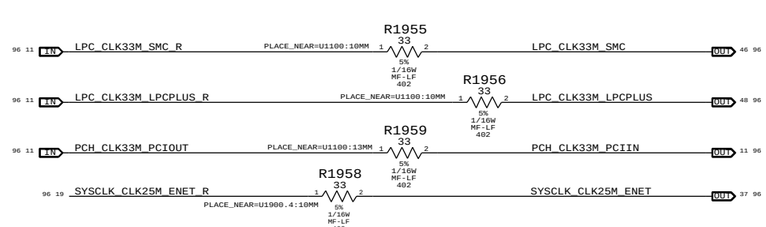


PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



Clock series termination



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PAGE TITLE: Chipset Support

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DRAWING NUMBER: 051-9884 SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 19 OF 127

SHEET: 19 OF 106

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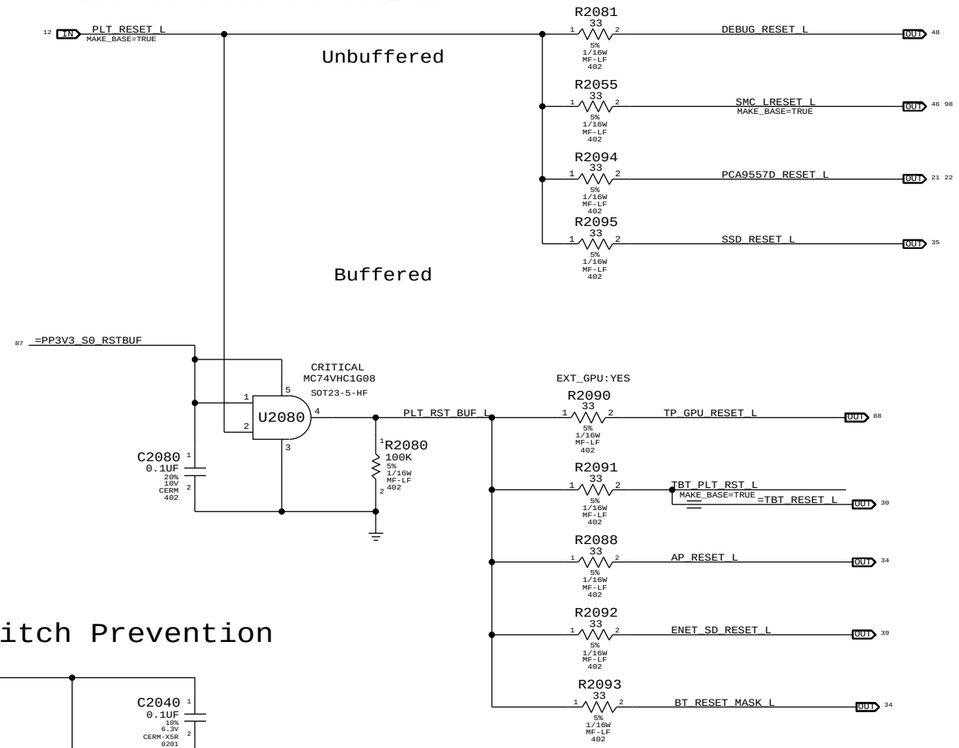
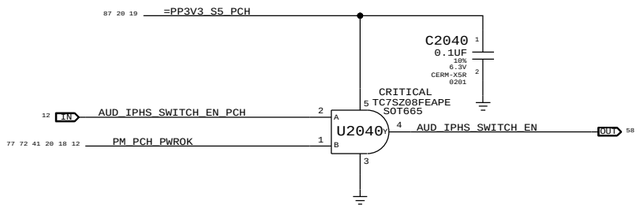
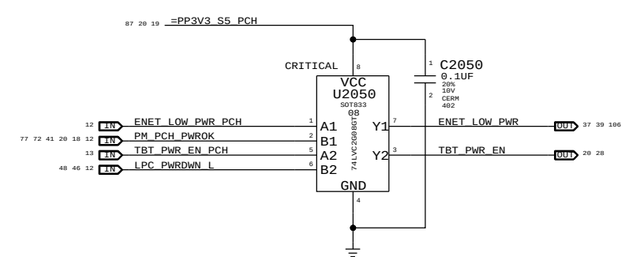
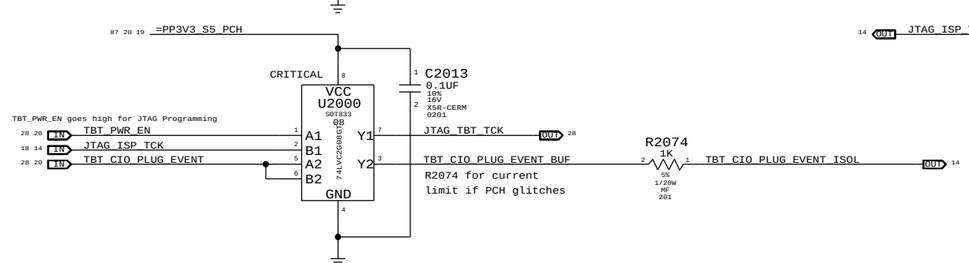
Platform Reset Connections

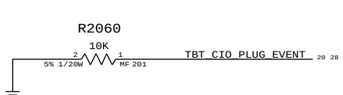


GPIO Glitch Prevention



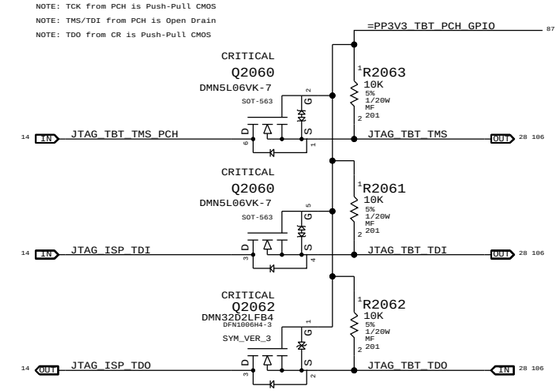






JTAG GPIO Isolation due to glitch in and out of sleep

NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TMS/TDI from PCH is Open Drain
NOTE: TDO from CR is Push-Pull CMOS



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

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Project Chipset Support

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DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 20 OF 127
SHEET 20 OF 106

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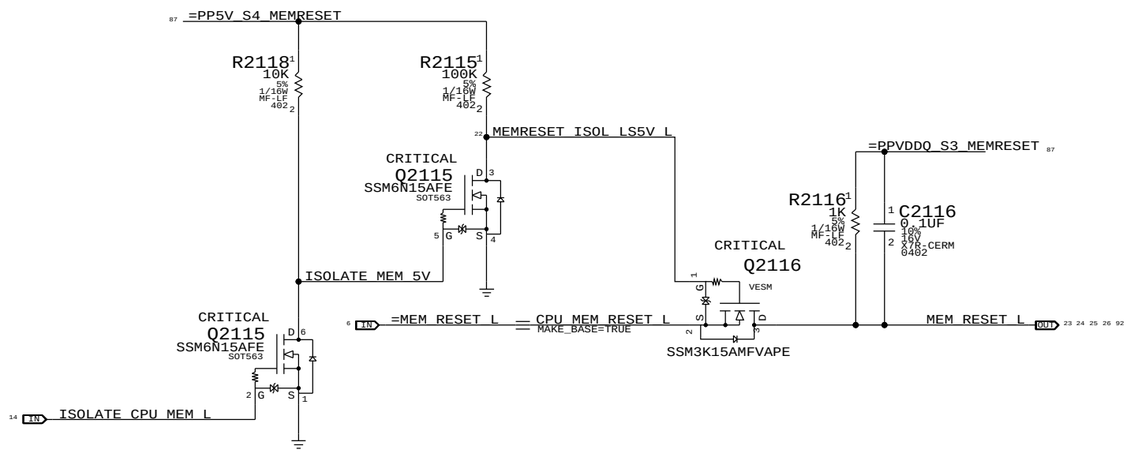
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

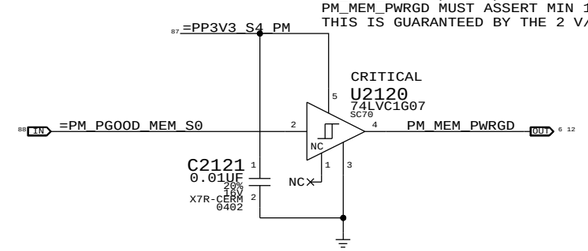
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

MEMVTT_EN = PLT_RESET_L * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



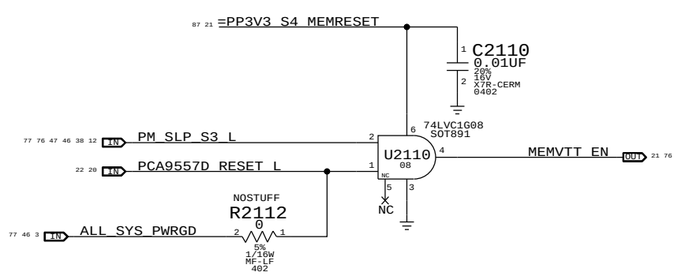
MEM S0 "PGOOD" FOR CPU

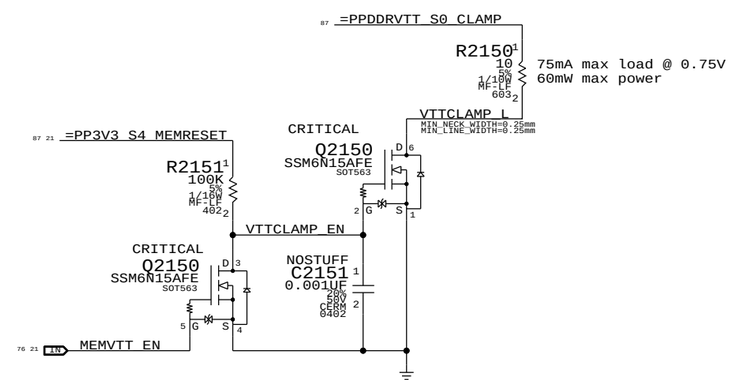
PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page
PM_MEM_PWRGD MUST ASSERT MIN 100 NS AFTER MEM_VDDQ RAMPS 80%
THIS IS GUARANTEED BY THE 2 V/MS RAMP RATE OF THE FET



MEMVTT Clamp

Ensures CKE signals are held low in S3





	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1
to	1	0	1	1	1	1	1
S3	2	0	0	1	1	1	0
	3	0	0	0	X	1	0
to	4	0	0	1	X	1	0
S0	5	0	1	1	0 (*)	1	1
	6	0	1	1	1	1	1
	7	1	1	1	1	CPU_MEM_RESET_L	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
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PAGE 21 OF 127
SHEET 21 OF 106

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Page Notes

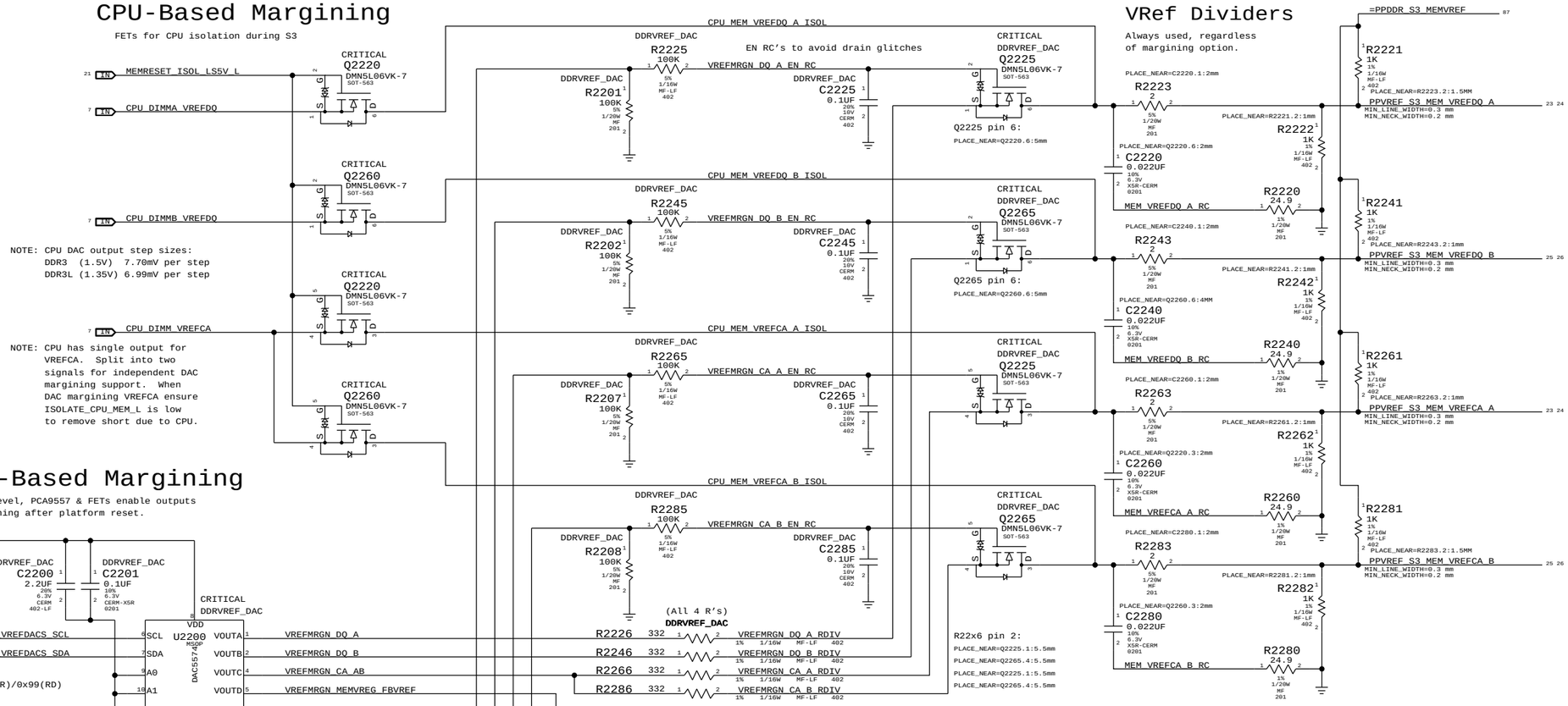
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during S3



NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step

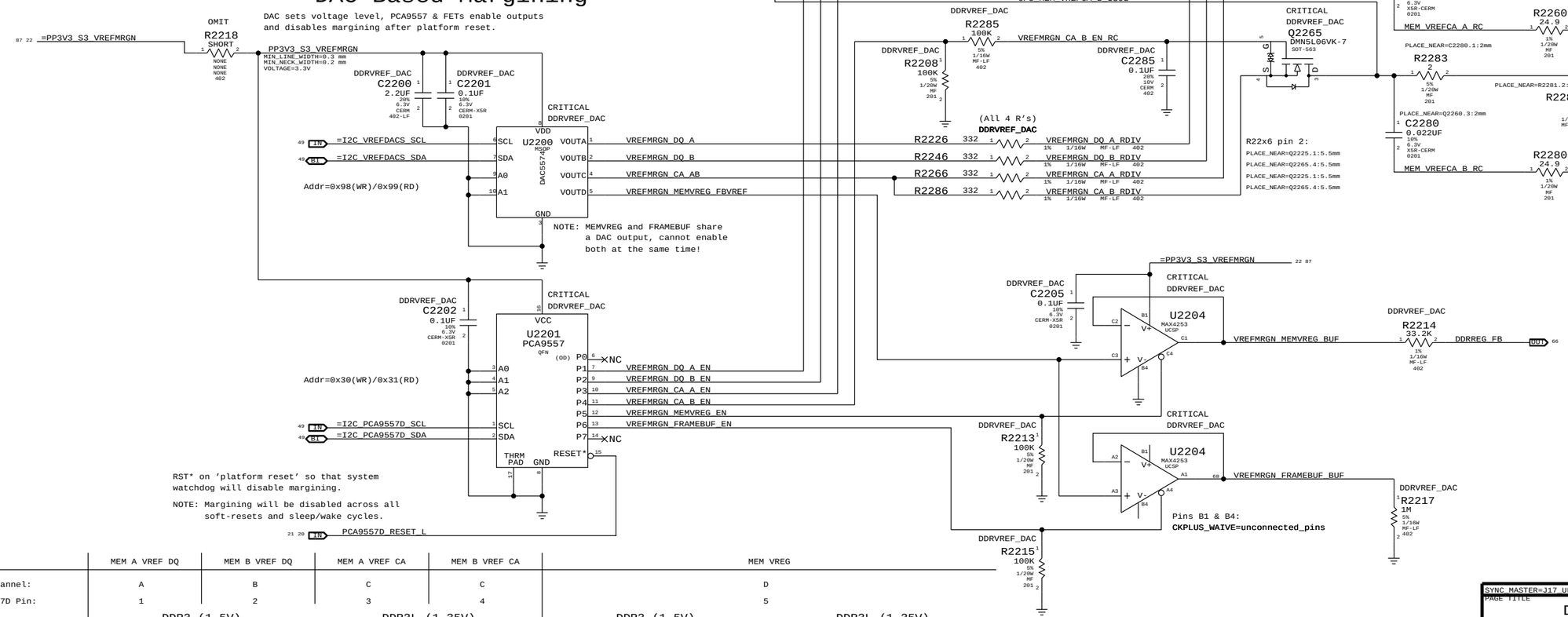
NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure ISOLATE_CPU_MEM_L is low to remove short due to CPU.

VRef Dividers

Always used, regardless of margining option.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER: 051-9884 SIZE: D

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PAGE: 22 OF 127

SHEET: 22 OF 106

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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

24 22 PPVREF_S3_MEM_VREFDQ_A
VOLTAGE=0.75V

C2330 2.2UF 20% 6.3V CERM 402-LF
C2331 0.1UF 20% 10V CERM 402

J2300 CRITICAL
F-ANG-SM-1
SODIMM-P0.60-D8
SYM 1 OF 2

P/N: 516S1019

J2300
SODIMM-P0.60-D8
F-ANG-SM-1
SYM 2 OF 2
MTG HOLE

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

87 24 23 =PPVDDQ_S3_MEM_A

C2310 0.1UF 20% 10V CERM 402
C2311 0.1UF 20% 10V CERM 402
C2312 0.1UF 20% 10V CERM 402
C2313 0.1UF 20% 10V CERM 402
C2314 0.1UF 20% 10V CERM 402
C2315 0.1UF 20% 10V CERM 402
C2316 0.1UF 20% 10V CERM 402
C2317 0.1UF 20% 10V CERM 402

C2300 10UF 20% 6.3V X5R 603
C2301 10UF 20% 6.3V X5R 603
C2318 0.1UF 20% 10V CERM 402
C2319 0.1UF 20% 10V CERM 402
C2320 0.1UF 20% 10V CERM 402
C2321 0.1UF 20% 10V CERM 402
C2322 0.1UF 20% 10V CERM 402
C2323 0.1UF 20% 10V CERM 402

23 MEM_DIMM0_SA<1>
23 MEM_DIMM0_SA<0>
87 24 23 =PP3V3_S0_MEM_A_SPD

C2340 2.2UF 20% 6.3V CERM 402-LF
R2340 10K 5% 1/16W MF-LF 402
R2341 10K 5% 1/16W MF-LF 402

87 24 23 =PPDDRVTT_S0_MEM_A

Pin	Signal	Pin	Signal
1	VREFDQ	2	VSS_0
3	VSS_1	4	DQ4
5	DQ0	6	DQ5
7	DQ1	8	VSS_2
9	VSS_3	10	DQS0*
11	DM0	12	DQS0
13	VSS_4	14	VSS_5
15	DQ2	16	DQ6
17	DQ3	18	DQ7
19	VSS_6	20	VSS_7
21	DQ8	22	DQ12
23	DQ9	24	DQ13
25	VSS_8	26	VSS_9
27	DQS1*	28	DM1
29	DQS1	30	RESET*
31	VSS_10	32	VSS_11
33	DQ10	34	DQ14
35	DQ11	36	DQ15
37	VSS_12	38	VSS_13
39	DQ16	40	DQ20
41	DQ17	42	DQ21
43	VSS_14	44	VSS_15
45	DQS2*	46	DM2
47	DQS2	48	VSS_16
49	VSS_17	50	DQ22
51	DQ18	52	DQ23
53	DQ19	54	VSS_18
55	VSS_19	56	DQ28
57	DQ24	58	DQ29
59	DQ25	60	VSS_20
61	VSS_21	62	DQS3*
63	DM3	64	DQS3
65	VSS_22	66	VSS_23
67	DQ26	68	DQ30
69	DQ27	70	DQ31
71	VSS_24	72	VSS_25
73	CKE0	74	CKE1
75	VDD_0	76	VDD_1
77	NC_0	78	A15
79	BA2	80	A14
81	VDD_2	82	VDD_3
83	A12/BC*	84	A11
85	A9	86	A7
87	VDD_4	88	VDD_5
89	A8	90	A6
91	A5	92	A4
93	VDD_6	94	VDD_7
95	A3	96	A2
97	A1	98	A0
99	VDD_8	100	VDD_9
101	CK0	102	CK1
103	CK0*	104	CK1*
105	VDD_10	106	VDD_11
107	A10_AP	108	BA1
109	BA0	110	RAS*
111	VDD_12	112	VDD_13
113	WE*	114	S0*
115	CAS*	116	ODT0
117	VDD_14	118	VDD_15
119	A13	120	ODT1
121	S1*	122	NC_1
123	VDD_16	124	VDD_17
125	TEST	126	VREFCA
127	VSS_26	128	VSS_27
129	DQ32	130	DQ36
131	DQ33	132	DQ37
133	VSS_28	134	VSS_29
135	DQS4*	136	DM4
137	DQS4	138	VSS_30
139	VSS_31	140	DQ38
141	DQ34	142	DQ39
143	DQ35	144	VSS_32
145	VSS_33	146	DQ44
147	DQ40	148	DQ45
149	DQ41	150	VSS_34
151	VSS_35	152	DQS5*
153	DM5	154	DQS5
155	VSS_36	156	VSS_37
157	DQ42	158	DQ46
159	DQ43	160	DQ47
161	VSS_38	162	VSS_39
163	DQ48	164	DQ52
165	DQ49	166	DQ53
167	VSS_40	168	VSS_41
169	DQS6*	170	DM6
171	DQS6	172	VSS_42
173	VSS_43	174	DQ54
175	DQ50	176	DQ55
177	DQ51	178	VSS_44
179	VSS_45	180	DQ60
181	DQ56	182	DQ61
183	DQ57	184	VSS_46
185	VSS_47	186	DQS7*
187	DM7	188	DQS7
189	VSS_48	190	VSS_49
191	DQ58	192	DQ62
193	DQ59	194	DQ63
195	VSS_50	196	VSS_51
197	SA0	198	EVENT*
199	VDDSPD	200	SDA
201	SA1	202	SCL
203	VTT_0	204	VTT_1
205		206	
207		208	
209			

Signal	Pin
=MEM_A_DQ<0>	3
=MEM_A_DQ<1>	5
=MEM_A_DQ<2>	13
=MEM_A_DQ<3>	15
=MEM_A_DQ<8>	19
=MEM_A_DQ<9>	21
=MEM_A_DQS_N<1>	25
=MEM_A_DQS_P<1>	27
=MEM_A_DQ<10>	31
=MEM_A_DQ<11>	33
=MEM_A_DQ<16>	37
=MEM_A_DQ<17>	39
=MEM_A_DQS_N<2>	43
=MEM_A_DQS_P<2>	45
=MEM_A_DQ<18>	49
=MEM_A_DQ<19>	51
=MEM_A_DQ<24>	55
=MEM_A_DQ<25>	57
=MEM_A_DQ<26>	65
=MEM_A_DQ<27>	67
MEM_A_CKE<0>	71
MEM_A_BA<2>	77
MEM_A_A<12>	81
MEM_A_A<9>	83
MEM_A_A<8>	87
MEM_A_A<5>	89
MEM_A_A<3>	93
MEM_A_A<1>	95
MEM_A_CLK_P<0>	99
MEM_A_CLK_N<0>	101
MEM_A_A<10>	105
MEM_A_BA<0>	107
MEM_A_WE_L	111
MEM_A_CAS_L	113
MEM_A_A<13>	117
MEM_A_CS_L<1>	119
=MEM_A_DQ<32>	127
=MEM_A_DQ<33>	129
=MEM_A_DQS_N<4>	133
=MEM_A_DQS_P<4>	135
=MEM_A_DQ<34>	139
=MEM_A_DQ<35>	141
=MEM_A_DQ<40>	145
=MEM_A_DQ<41>	147
=MEM_A_DQ<42>	155
=MEM_A_DQ<43>	157
=MEM_A_DQ<48>	161
=MEM_A_DQ<49>	163
=MEM_A_DQS_N<6>	167
=MEM_A_DQS_P<6>	169
=MEM_A_DQ<50>	173
=MEM_A_DQ<51>	175
=MEM_A_DQ<56>	179
=MEM_A_DQ<57>	181
=MEM_A_DQ<58>	185
=MEM_A_DQ<59>	187
MEM_DIMM0_SA<0>	191
=PP3V3_S0_MEM_A_SPD	193
MEM_DIMM0_SA<1>	197
=MEM_A_DQ<4>	3
=MEM_A_DQ<5>	5
=MEM_A_DQS_N<0>	9
=MEM_A_DQS_P<0>	11
=MEM_A_DQ<6>	15
=MEM_A_DQ<7>	17
=MEM_A_DQ<12>	21
=MEM_A_DQ<13>	23
MEM_RESET_L	29
=MEM_A_DQ<14>	33
=MEM_A_DQ<15>	35
=MEM_A_DQ<20>	39
=MEM_A_DQ<21>	41
=MEM_A_DQ<22>	49
=MEM_A_DQ<23>	51
=MEM_A_DQ<28>	55
=MEM_A_DQ<29>	57
=MEM_A_DQS_N<3>	61
=MEM_A_DQS_P<3>	63
=MEM_A_DQ<30>	67
=MEM_A_DQ<31>	69
MEM_A_CKE<1>	73
MEM_A_A<15>	77
MEM_A_A<14>	79
MEM_A_A<11>	83
MEM_A_A<7>	85
MEM_A_A<6>	89
MEM_A_A<4>	91
MEM_A_A<2>	95
MEM_A_A<0>	97
MEM_A_CLK_P<1>	101
MEM_A_CLK_N<1>	103
MEM_A_BA<1>	107
MEM_A_RAS_L	109
MEM_A_CS_L<0>	113
MEM_A_ODT<0>	115
MEM_A_ODT<1>	119
MEM_A_DQ<36>	129
MEM_A_DQ<37>	131
MEM_A_DQ<38>	139
MEM_A_DQ<39>	141
MEM_A_DQ<44>	145
MEM_A_DQ<45>	147
MEM_A_DQS_N<5>	151
MEM_A_DQS_P<5>	153
MEM_A_DQ<46>	157
MEM_A_DQ<47>	159
MEM_A_DQ<52>	163
MEM_A_DQ<53>	165
MEM_A_DQ<54>	173
MEM_A_DQ<55>	175
MEM_A_DQ<60>	179
MEM_A_DQ<61>	181
MEM_A_DQS_N<7>	185
MEM_A_DQS_P<7>	187
MEM_A_DQ<62>	191
MEM_A_DQ<63>	193
MEM_EVENT_L	197
=I2C_SODIMMA_SDA	199
=I2C_SODIMMA_SCL	201

=PPVDDQ_S3_MEM_A 23 24 87

PPVREF_S3_MEM_VREFCA_A 22 24
VOLTAGE=0.75V

C2335 2.2UF 20% 6.3V CERM 402-LF
C2336 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A 23 24 87

C2350 1UF 10% 10V X5R 402
C2351 1UF 10% 10V X5R 402
C2352 1UF 10% 10V X5R 402
C2353 1UF 10% 10V X5R 402

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
DDR3 SO-DIMM Connector A Slot0

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DRAWING NUMBER 051-9884 SIZE D
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PAGE 23 OF 127
SHEET 23 OF 106

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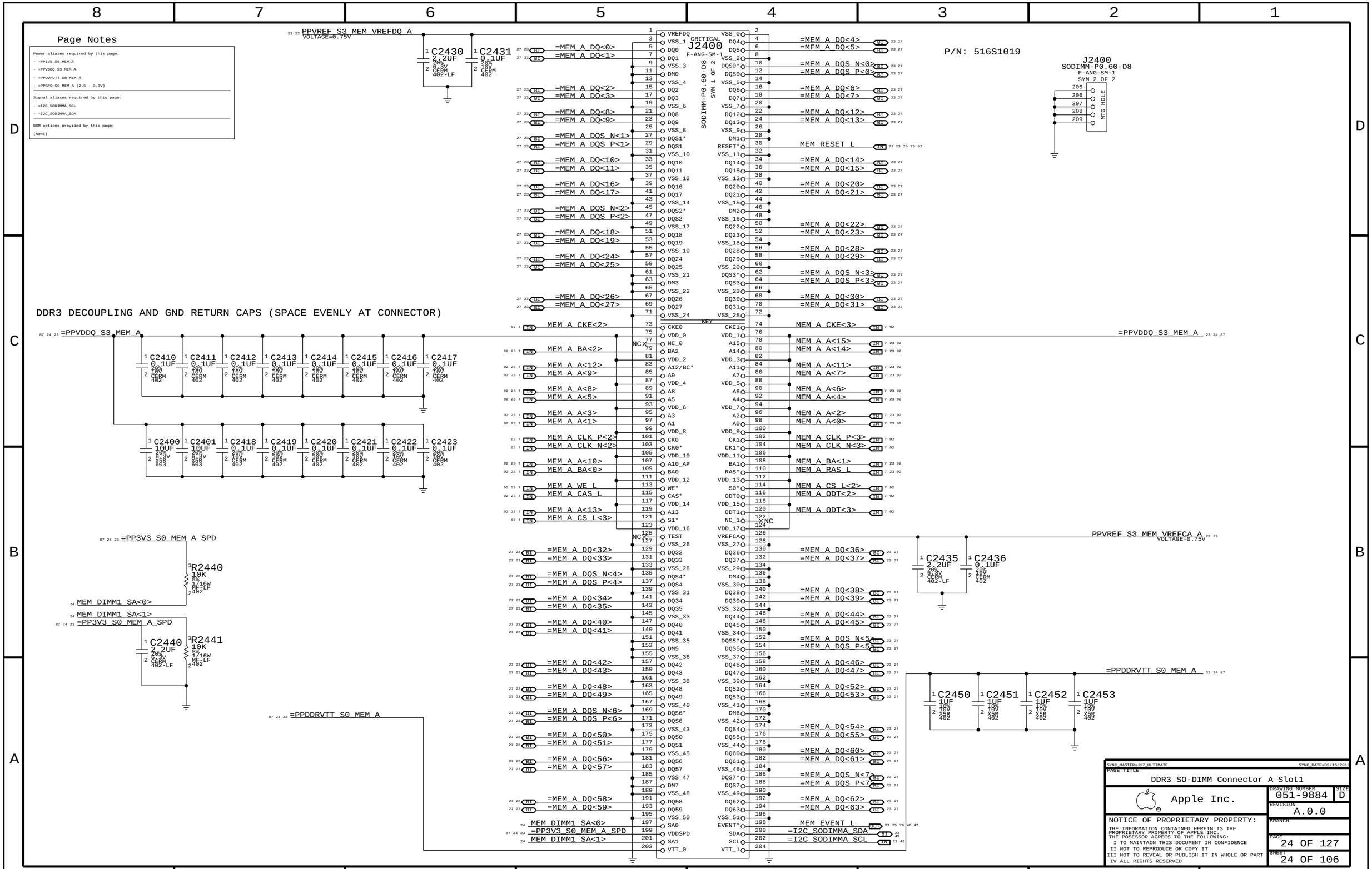
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)



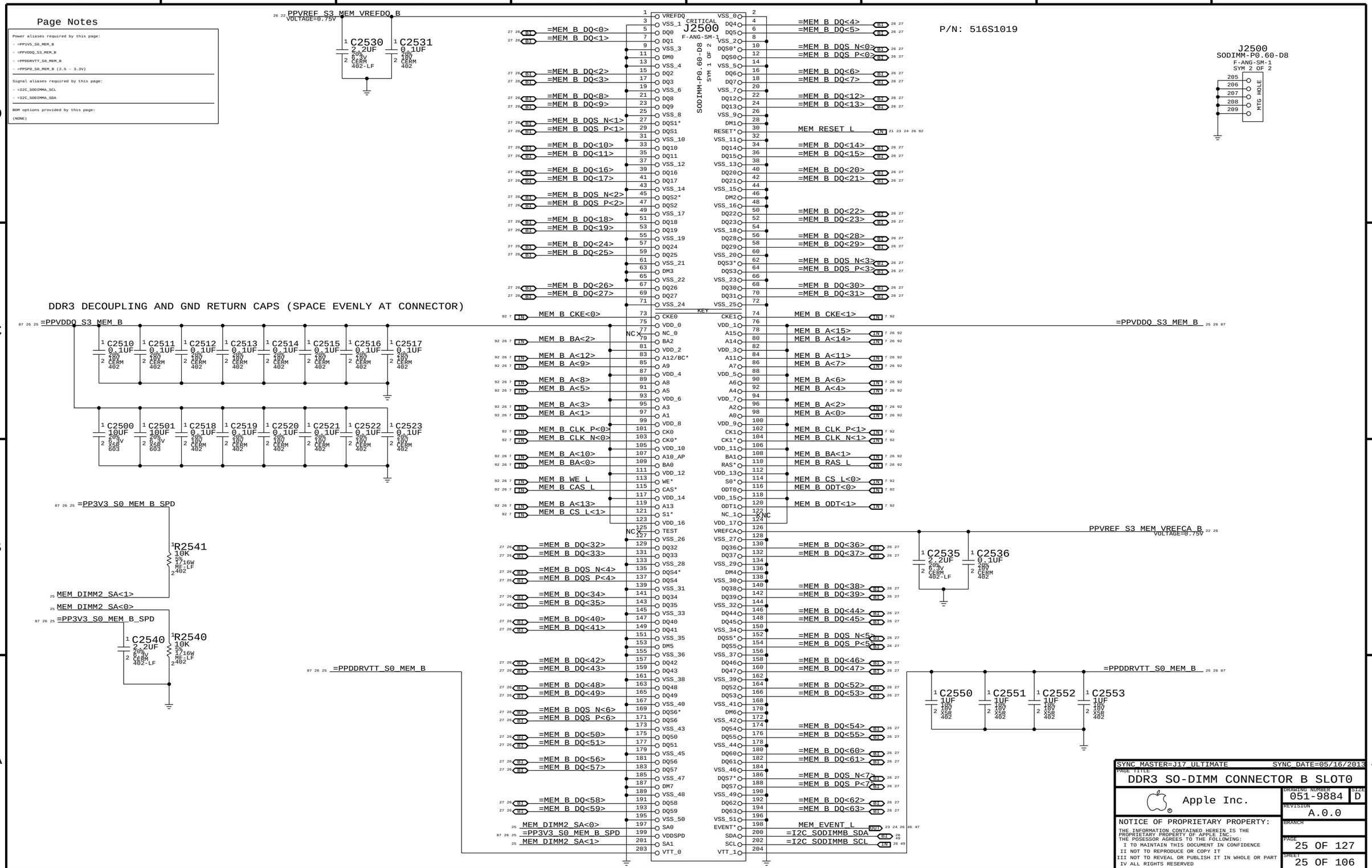
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B SLOT0

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DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
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PAGE 25 OF 127
SHEET 25 OF 106

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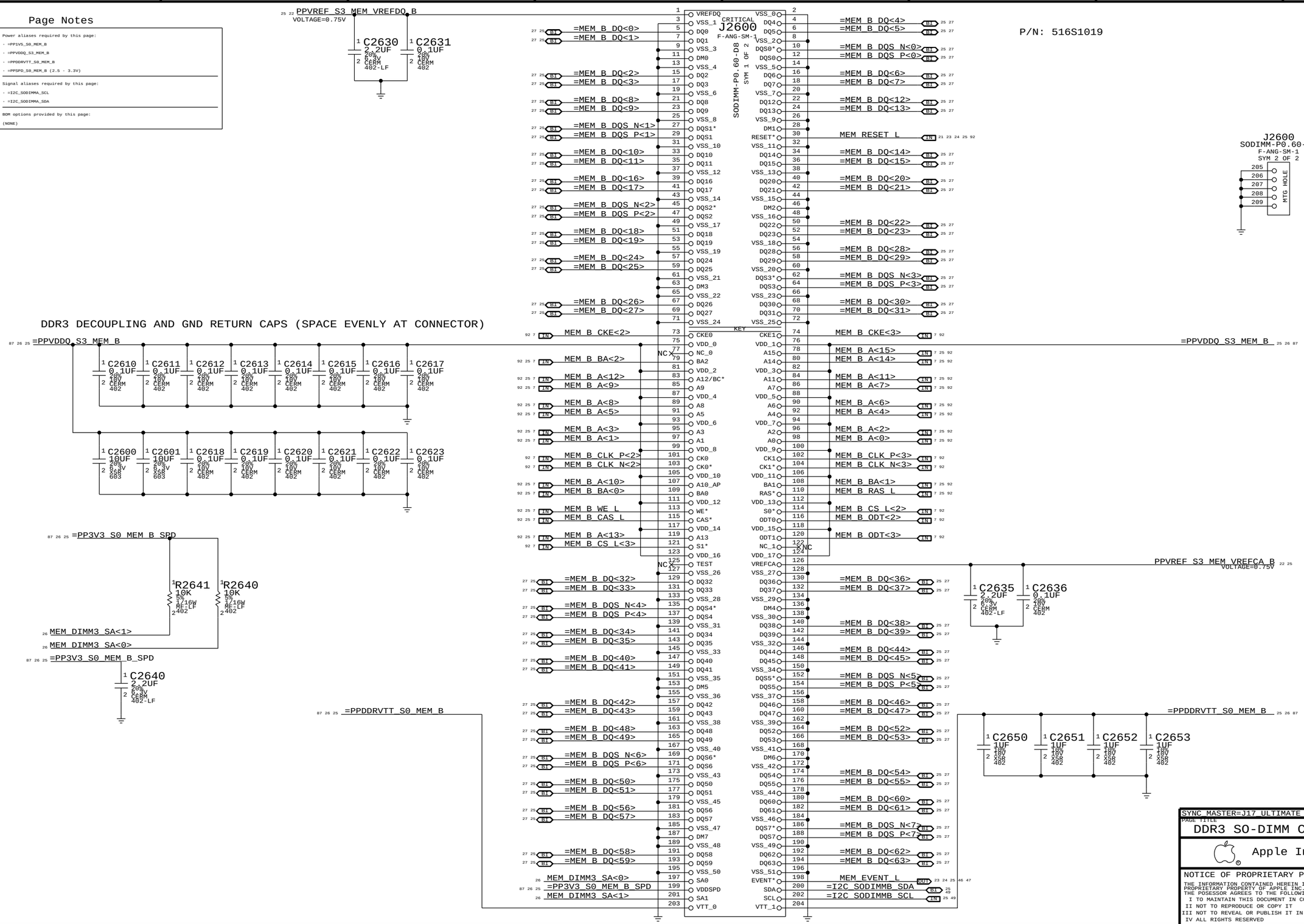
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B SLOT1

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BRANCH
PAGE 26 OF 127
SHEET 26 OF 106

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THERE ARE NO PIN SWAPS

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	MEM_B_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	MEM_B_DQS_P<0>
	MAKE_BASE=TRUE		
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	MEM_B_DQ<7>
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	MEM_B_DQ<6>
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	MEM_B_DQ<5>
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	MEM_B_DQ<4>
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	MEM_B_DQ<3>
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	MEM_B_DQ<2>
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	MEM_B_DQ<1>
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	MEM_B_DQ<0>
	MAKE_BASE=TRUE		
MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	MEM_B_DQS_N<1>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	MEM_B_DQS_P<1>
	MAKE_BASE=TRUE		
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	MEM_B_DQ<15>
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	MEM_B_DQ<14>
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	MEM_B_DQ<13>
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	MEM_B_DQ<12>
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	MEM_B_DQ<11>
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	MEM_B_DQ<10>
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	MEM_B_DQ<9>
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	MEM_B_DQ<8>
	MAKE_BASE=TRUE		
MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	MEM_B_DQS_N<2>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	MEM_B_DQS_P<2>
	MAKE_BASE=TRUE		
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	MEM_B_DQ<23>
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	MEM_B_DQ<22>
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	MEM_B_DQ<21>
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	MEM_B_DQ<20>
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	MEM_B_DQ<19>
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	MEM_B_DQ<18>
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	MEM_B_DQ<17>
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	MEM_B_DQ<16>
	MAKE_BASE=TRUE		
MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	MEM_B_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	MEM_B_DQS_P<3>
	MAKE_BASE=TRUE		
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	MEM_B_DQ<31>
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	MEM_B_DQ<30>
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	MEM_B_DQ<29>
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	MEM_B_DQ<28>
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	MEM_B_DQ<27>
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	MEM_B_DQ<26>
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	MEM_B_DQ<25>
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	MEM_B_DQ<24>
	MAKE_BASE=TRUE		
MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	MEM_B_DQS_N<4>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	MEM_B_DQS_P<4>
	MAKE_BASE=TRUE		
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	MEM_B_DQ<39>
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	MEM_B_DQ<38>
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	MEM_B_DQ<37>
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	MEM_B_DQ<36>
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	MEM_B_DQ<35>
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	MEM_B_DQ<34>
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	MEM_B_DQ<33>
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	MEM_B_DQ<32>
	MAKE_BASE=TRUE		
MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	MEM_B_DQS_N<5>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	MEM_B_DQS_P<5>
	MAKE_BASE=TRUE		
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	MEM_B_DQ<47>
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	MEM_B_DQ<46>
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	MEM_B_DQ<45>
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	MEM_B_DQ<44>
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	MEM_B_DQ<43>
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	MEM_B_DQ<42>
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	MEM_B_DQ<41>
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	MEM_B_DQ<40>
	MAKE_BASE=TRUE		
MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	MEM_B_DQS_N<6>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	MEM_B_DQS_P<6>
	MAKE_BASE=TRUE		
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	MEM_B_DQ<55>
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	MEM_B_DQ<54>
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	MEM_B_DQ<53>
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	MEM_B_DQ<52>
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	MEM_B_DQ<51>
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	MEM_B_DQ<50>
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	MEM_B_DQ<49>
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	MEM_B_DQ<48>
	MAKE_BASE=TRUE		
MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	MEM_B_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	MEM_B_DQS_P<7>
	MAKE_BASE=TRUE		
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	MEM_B_DQ<63>
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	MEM_B_DQ<62>
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	MEM_B_DQ<61>
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	MEM_B_DQ<60>
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	MEM_B_DQ<59>
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	MEM_B_DQ<58>
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	MEM_B_DQ<57>
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	MEM_B_DQ<56>

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
DDR3 ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

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PAGE 27 OF 127

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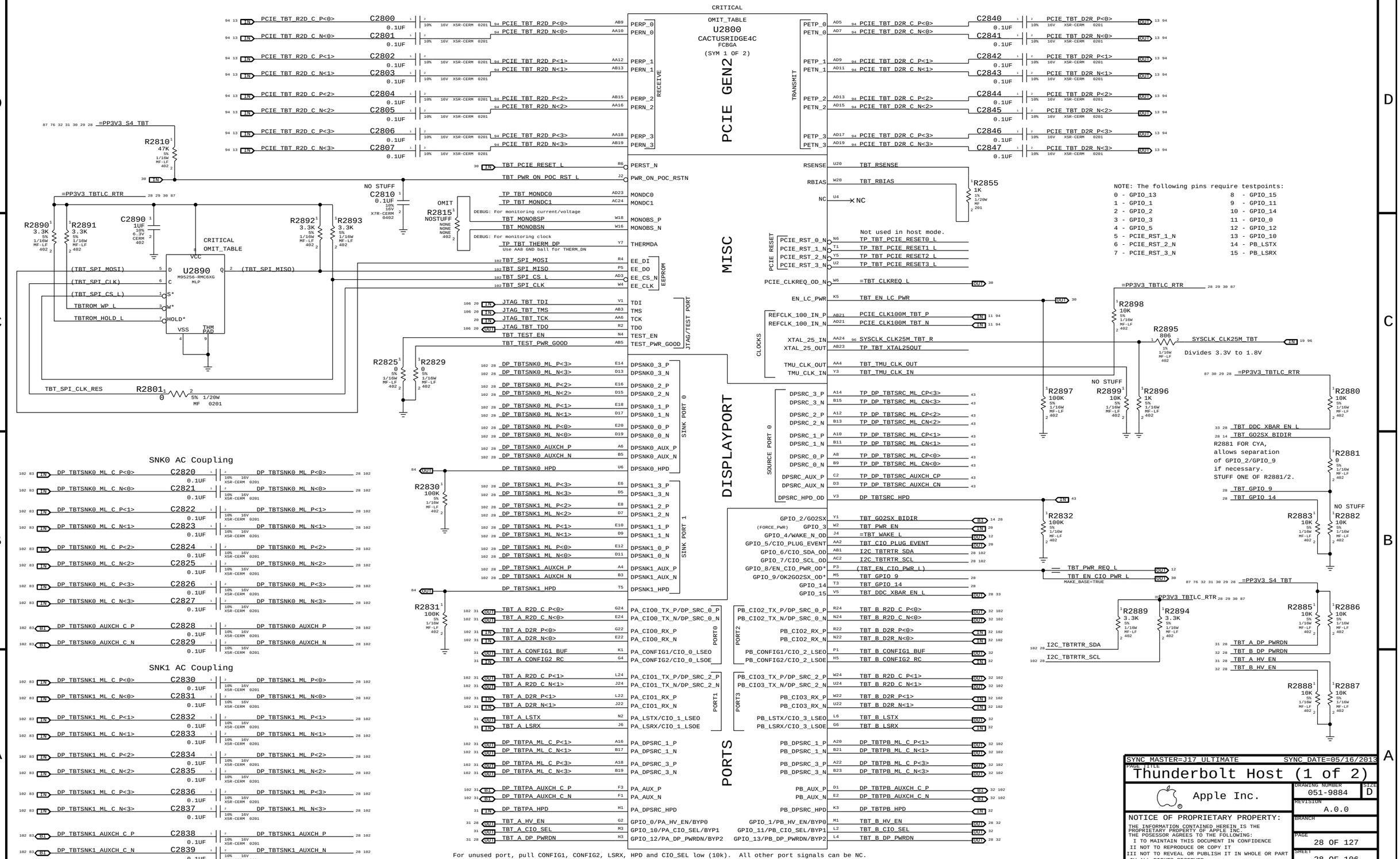

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PAGE TITLE
Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

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PAGE 28 OF 127

SHEET 28 OF 106

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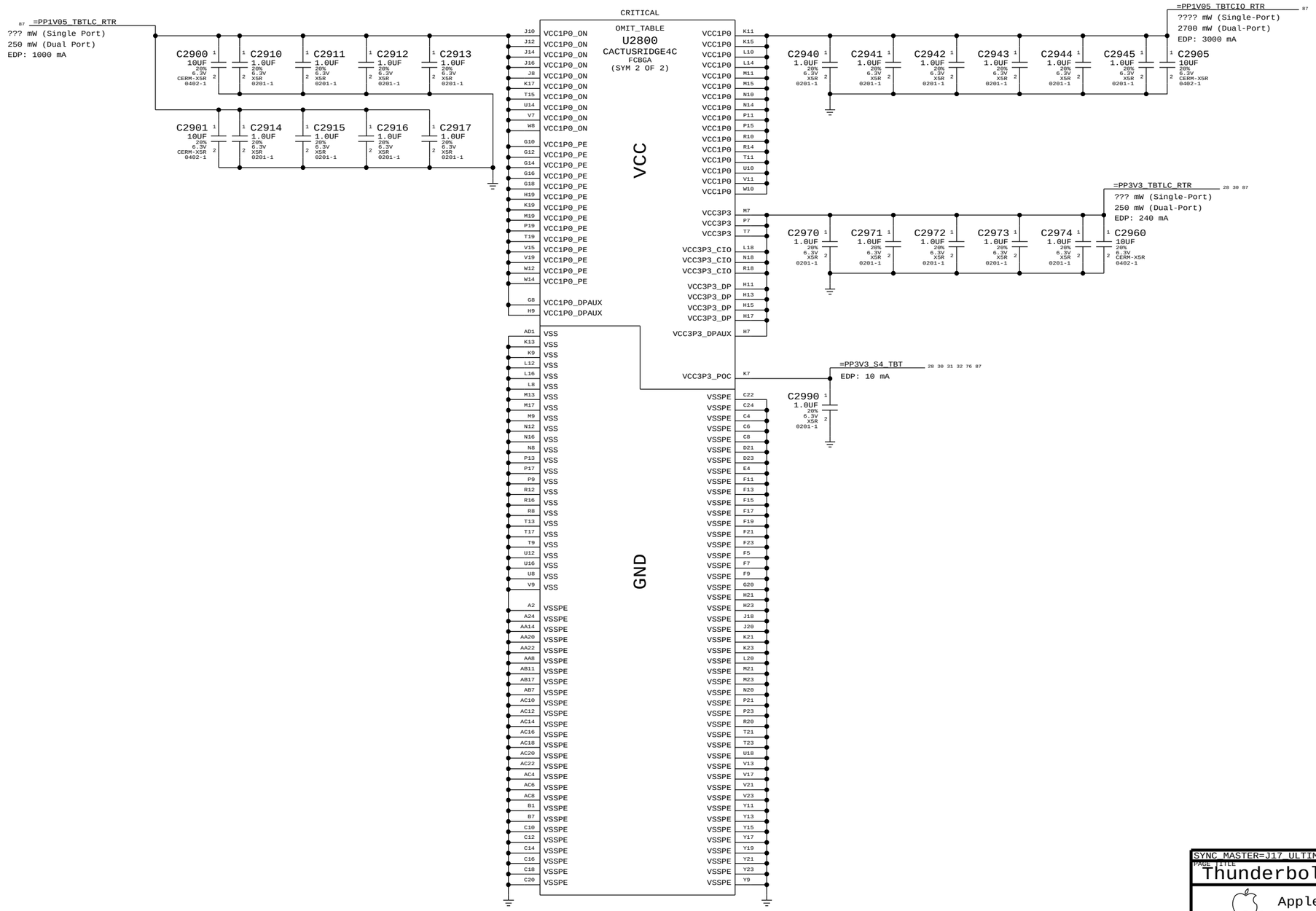

EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

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PAGE TITLE
Thunderbolt Host (2 of 2)

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PAGE 29 OF 127

SHEET 29 OF 106

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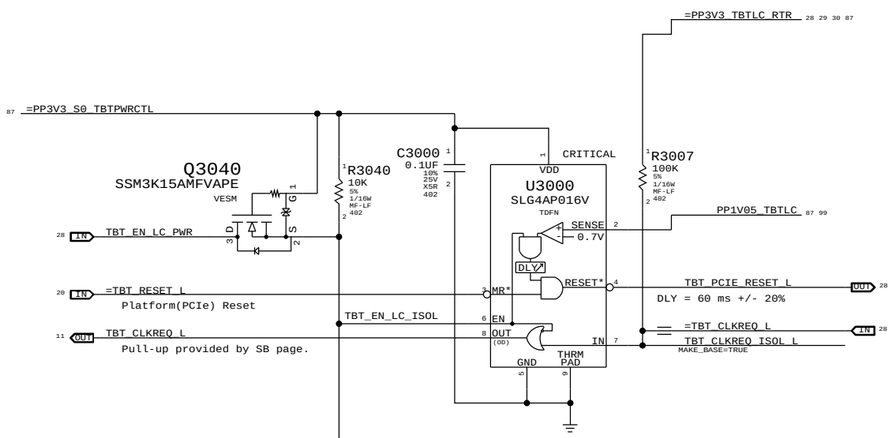
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

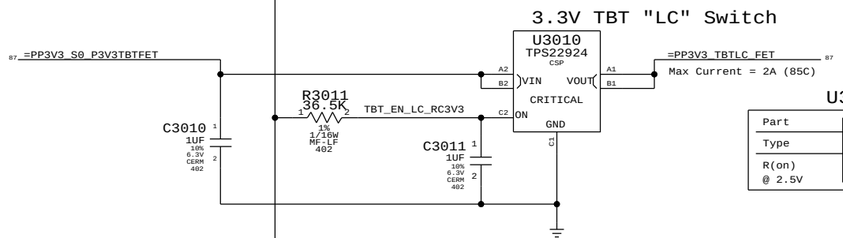
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation



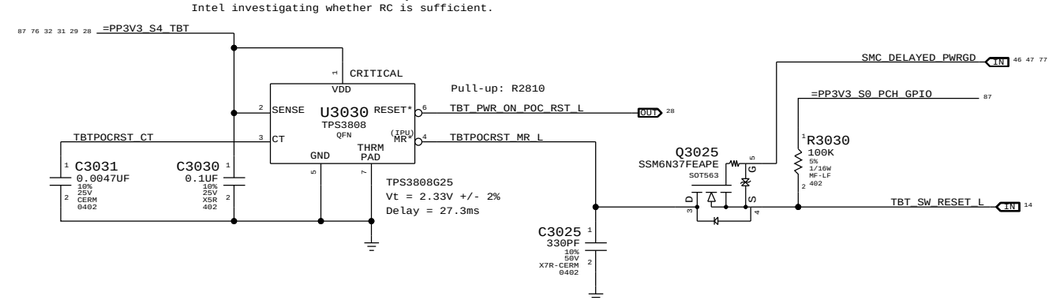
3.3V TBT "LC" Switch



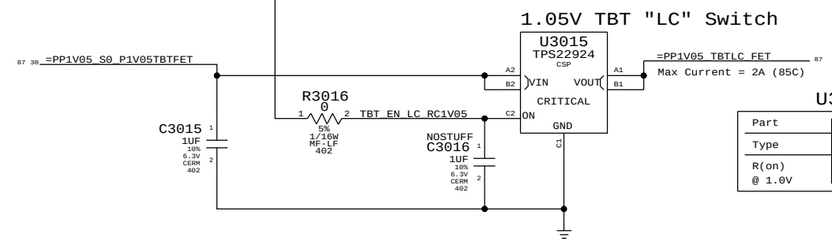
U3010	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

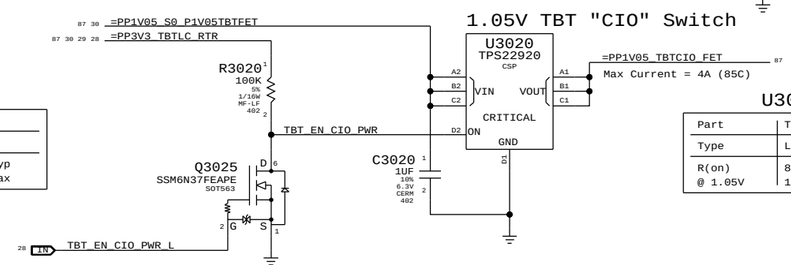


1.05V TBT "LC" Switch



U3015	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

1.05V TBT "CIO" Switch



U3020	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: Thunderbolt Power Support

Apple Inc.

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PAGE: 30 OF 127

SHEET: 30 OF 106

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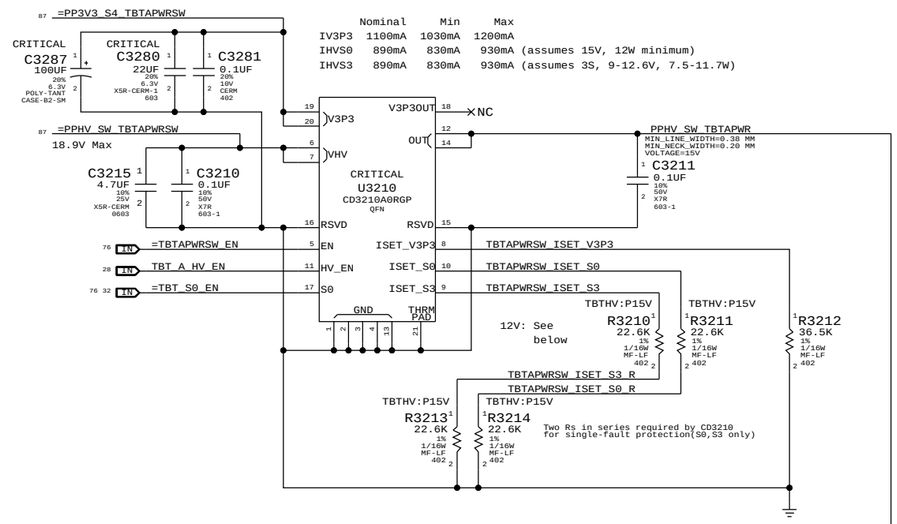
3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

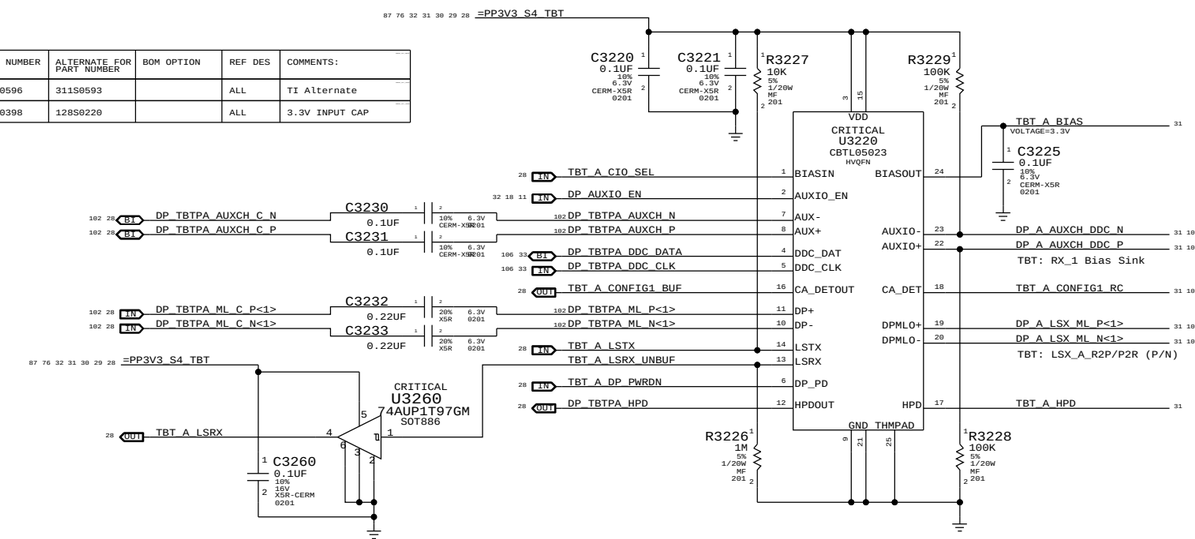


For 12V systems:

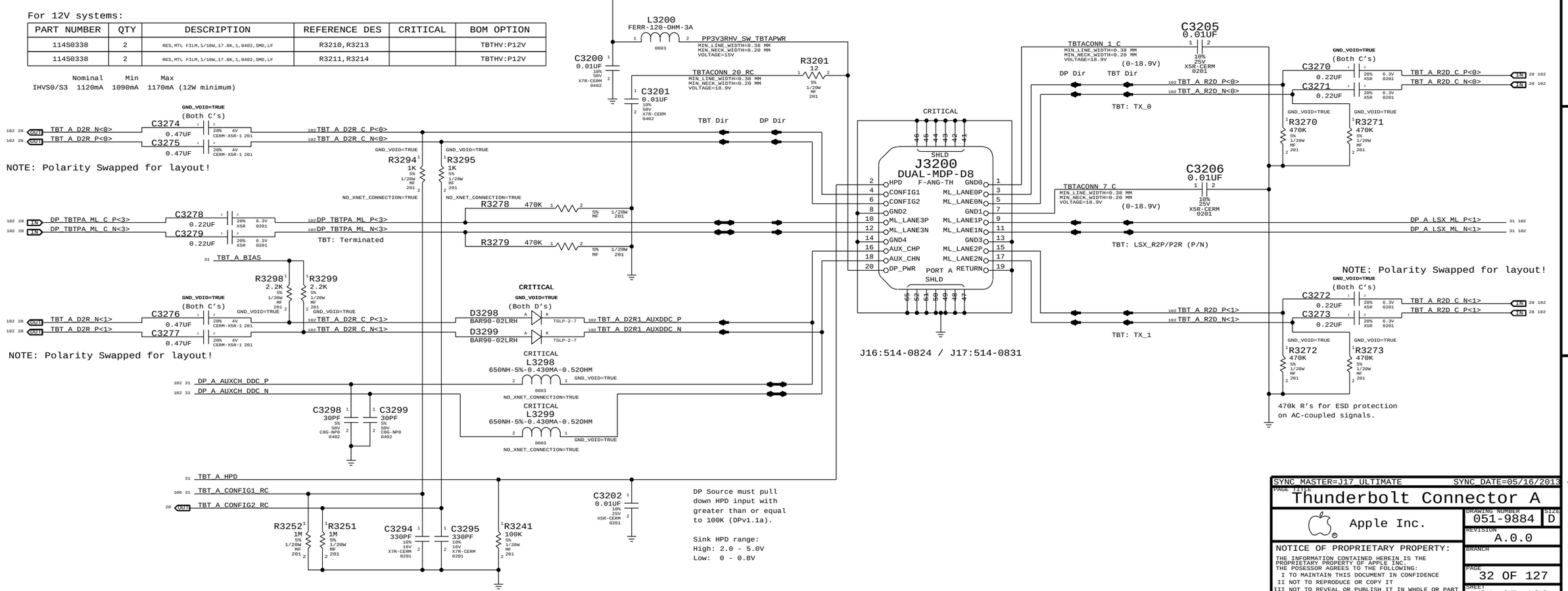
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3210,R3213		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0596	311S0593		ALL	TI Alternate
128S0398	128S0220		ALL	3.3V INPUT CAP



Thunderbolt Connector A



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PAGE TITLE: Thunderbolt Connector A

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PAGE: 32 OF 127

SHEET: 31 OF 106

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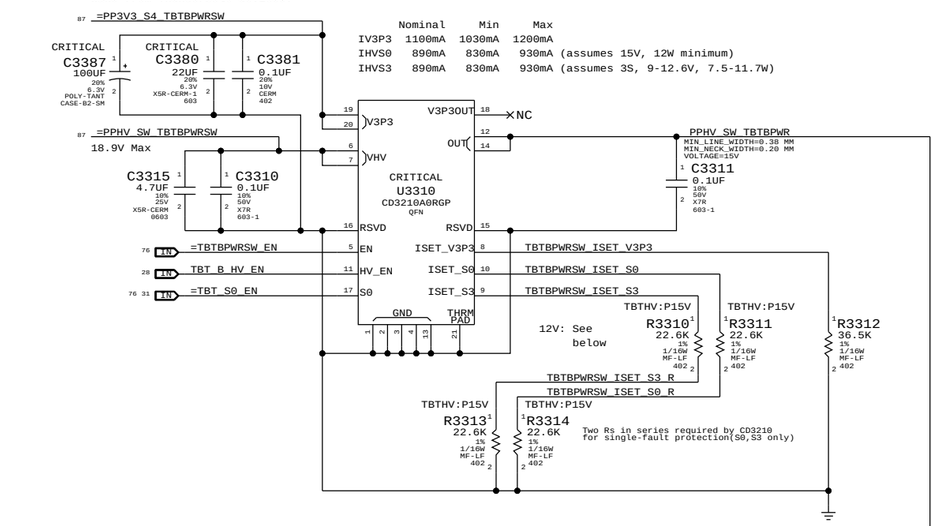
3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

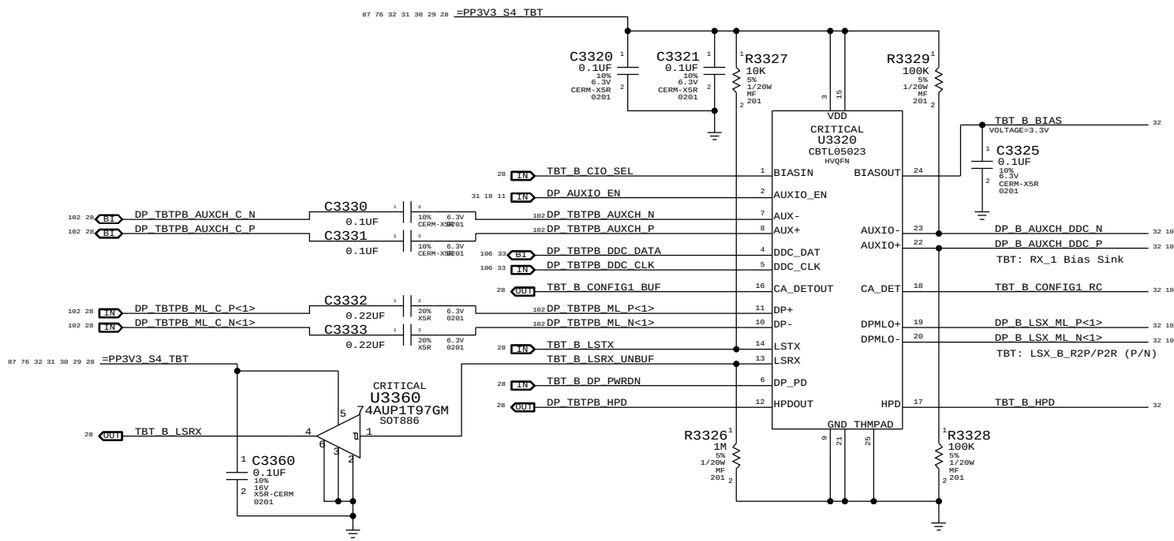


For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3310,R3313		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

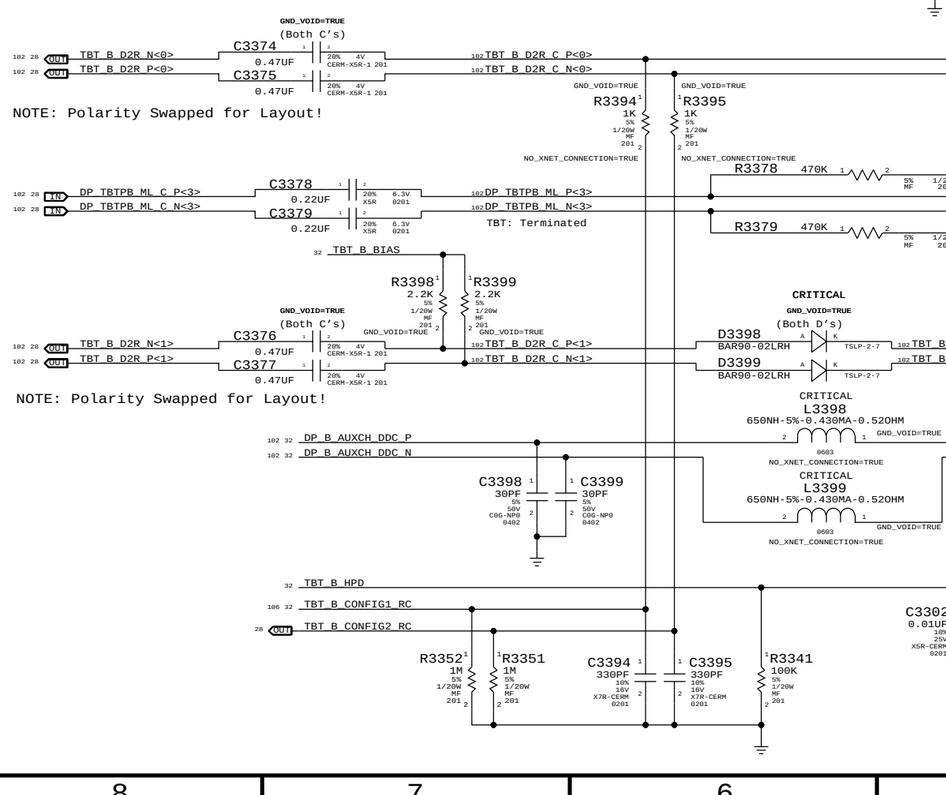
Thunderbolt Connector B



For 12V systems:

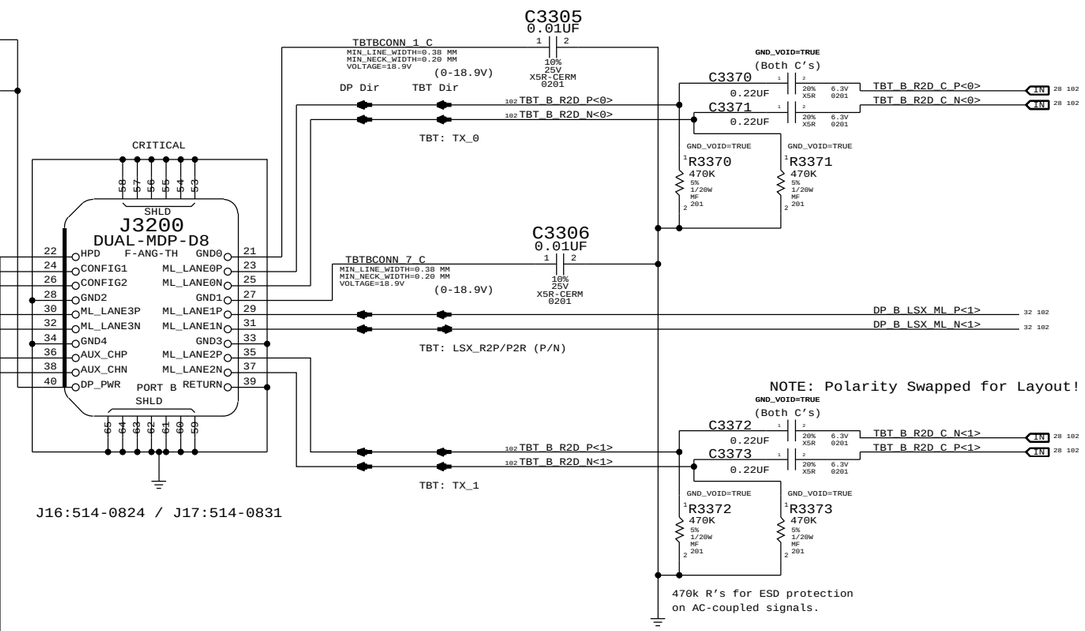
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3310,R3313		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)



DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V



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Thunderbolt Connector B

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PAGE 33 OF 127

SHEET 32 OF 106

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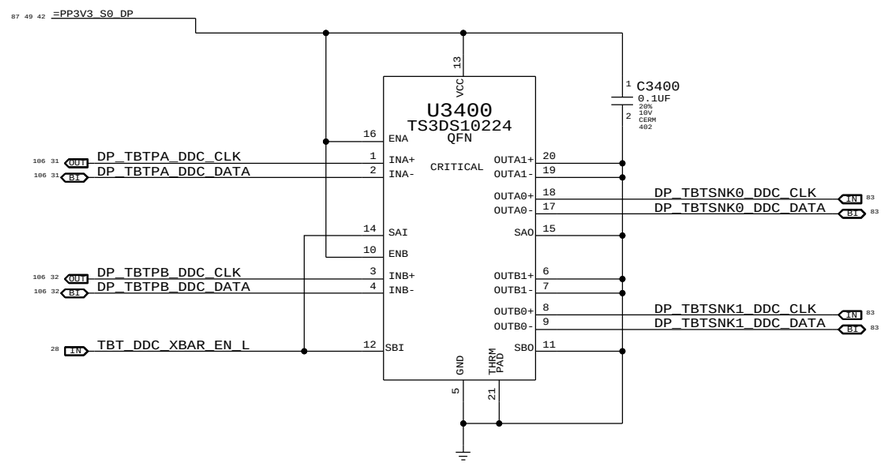
Dual-Port Host DDC Crossbar



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TBT DDC Crossbar

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PAGE 34 OF 127

SHEET 33 OF 106

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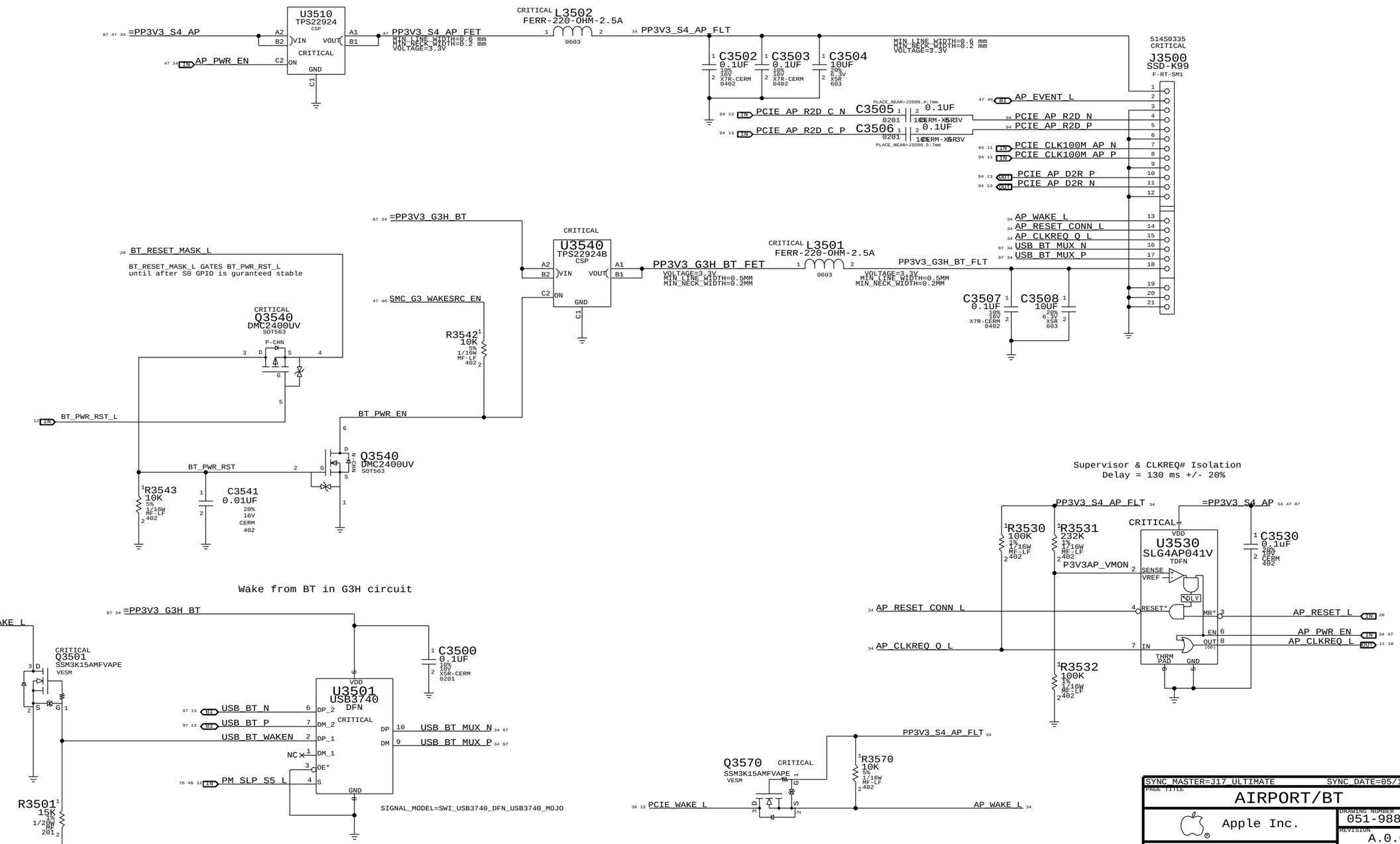
AIRPORT BLUETOOTH

AP & BT Load Switch

SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)



SYNC_MASTER=J17_ULTIMATE	SYNC_DATE=05/16/2013
PAGE TITLE	AIRPORT/BT
Apple Inc.	DRAWING NUMBER 051-9884 SIZE D
	REVISION A.0.0
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	PAGE 35 OF 127
	SHEET 34 OF 106

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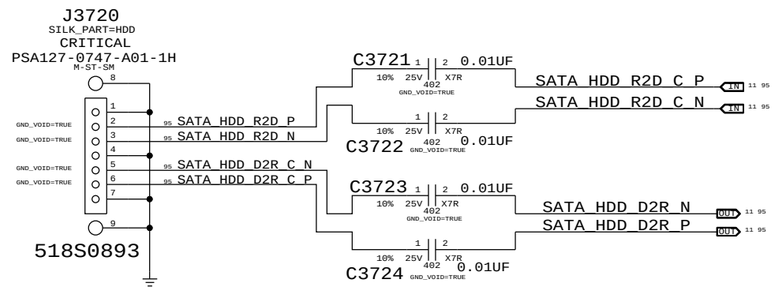
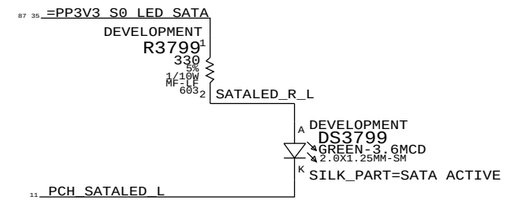
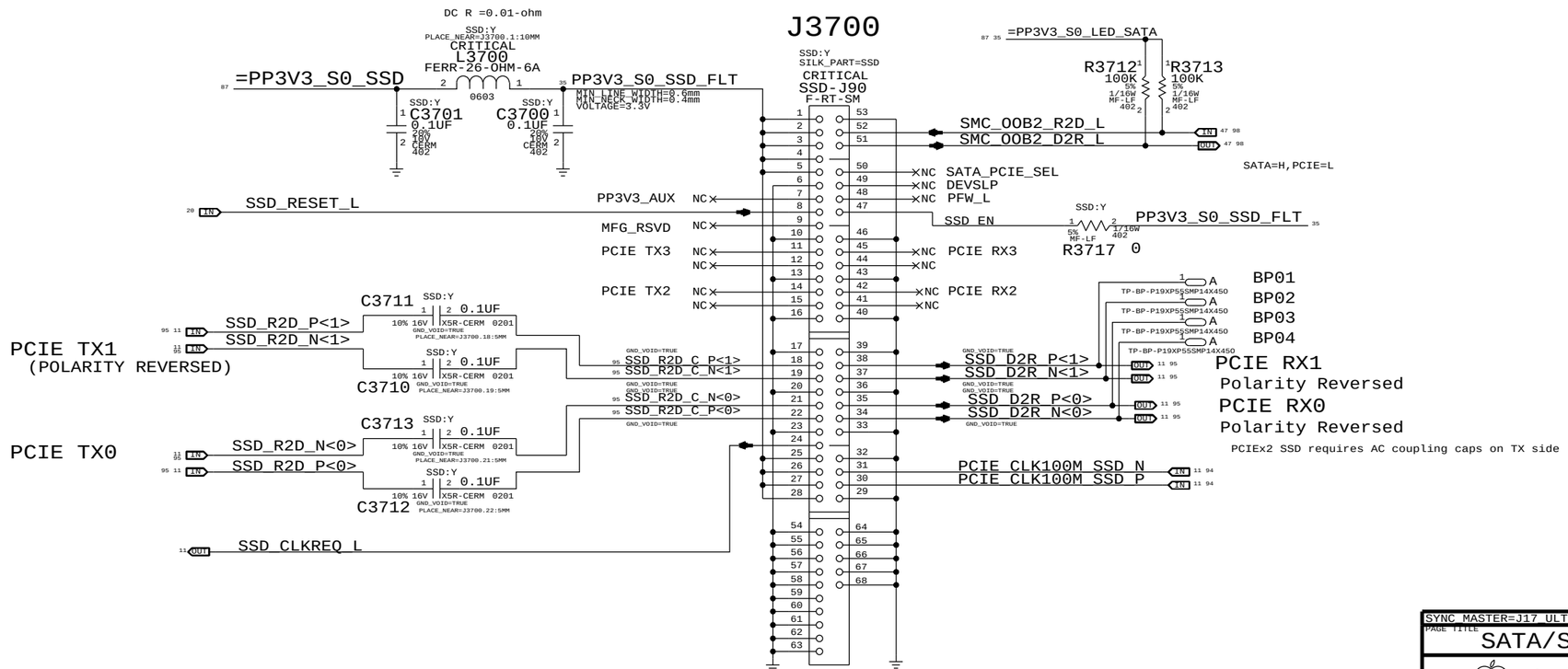
HDD SIGNAL CONNECTOR



SATA Activity LED



GS3 SSD



SYNC_MASTER=J17_ULTIMATE	SYNC_DATE=05/16/2013
PAGE TITLE: SATA/SSD Connectors	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
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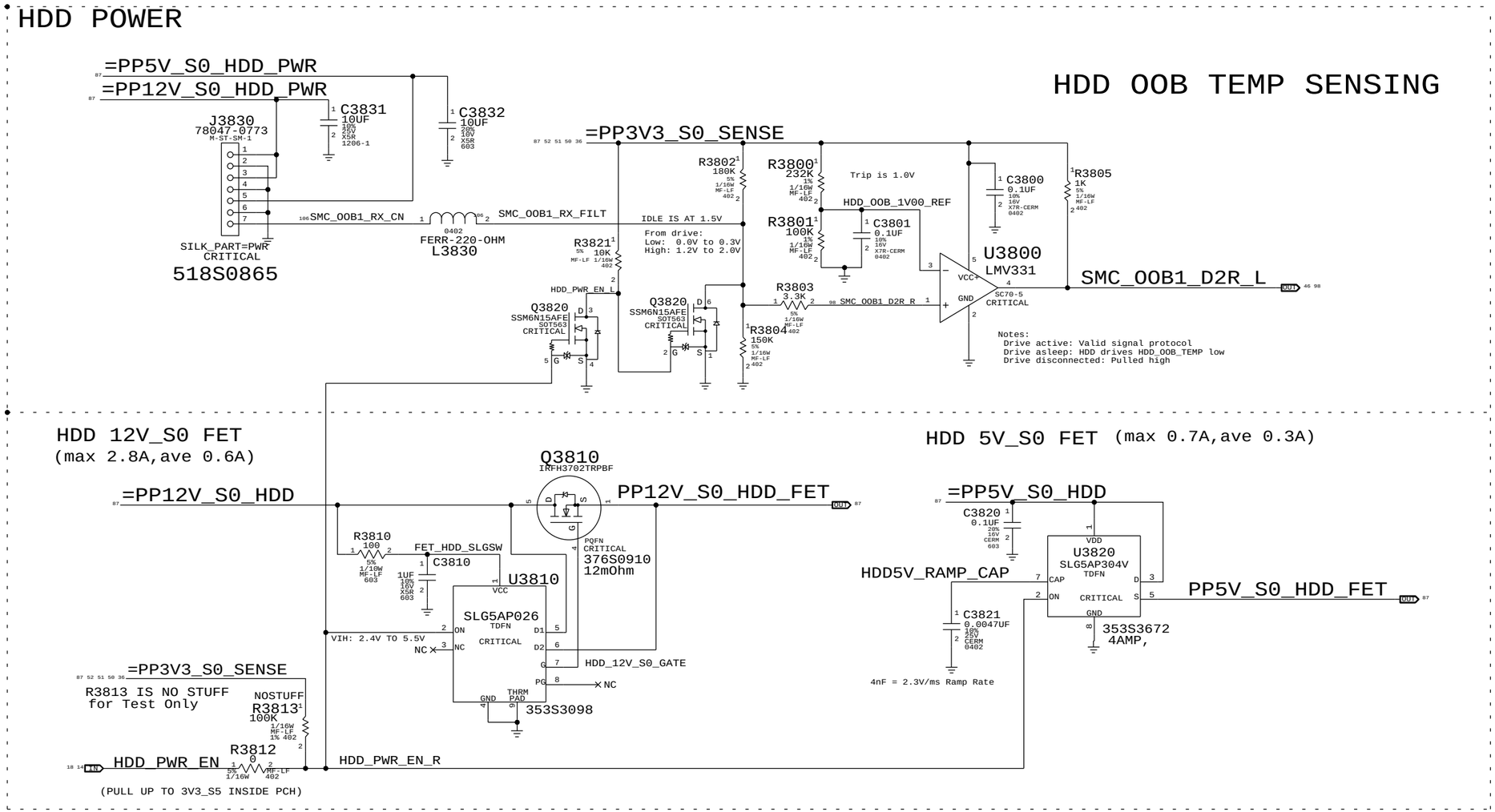
	SHEET: 35 OF 106



REMOVE R3813 AND SHORT R3812 AFTER HDD_PWR_EN WORKS

SYNC MASTER=J17_ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
HDD/SSD Temp Sense

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PAGE 38 OF 127

SHEET 36 OF 106

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)

VDD for Card Reader I/O
=PP3V3R1V8_CR_VDDIO

ENET_SR_LX
=ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_BIASVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_AVDDH MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201

=PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
=ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8

AVDDH, BIASVDDH, XTALVDDH, VDDO, SR_VDD, SR_VDDP, SR_LX, SR_VFB, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC

ENET_VMAIN_PRSNT — VMAIN_PRSNT (IPD-ENET)
PCIE_ENET_D2R_C_N — PCIE_TXD_N
PCIE_ENET_D2R_C_P — PCIE_TXD_P
PCIE_ENET_R2D_P — PCIE_RXD_P
PCIE_ENET_R2D_N — PCIE_RXD_N
PCIE_CLK100M_ENET_P — PCIE_REFCLK_P
PCIE_CLK100M_ENET_N — PCIE_REFCLK_N
ENET_RESET_L — PERST* (IPD)
ENET_CLKREQ_L — CLKREQ* (OD)
WAKE* (OD)
ENET_LOW_PWR — LOW_PWR (IPD)
SMB_ENET_SCL — SMB_CLK
SMB_ENET_SDA — SMB_DATA (IPD-ENETM)
ENET_SCLK — SCLK_SPD1000LED*
ENET_MISO — SI/EEDATA
ENET_MOSI — SO_LINKLED*
ENET_CS_L — CS*/EECLK
(IPU)
NC — SPD100LED*/SERIAL_DO (OD)
ENET_TRAFFICLED_L — TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET — XTALI
NC — XTALO
ENET_RDAC — RDAC
THRM_PAD

NOTE: "IPx" == Programmable pull-up/down
(IPx-ENET) SD_DETECT can only be used active low due to errata.

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_AVDDL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_GPHYPLL MIN_LINE_WIDTH=0.4 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

ENETCONN_MDI_P<0> — TRD0_P
ENETCONN_MDI_N<0> — TRD0_N
ENETCONN_MDI_P<1> — TRD1_P
ENETCONN_MDI_N<1> — TRD1_N
ENETCONN_MDI_P<2> — TRD2_P
ENETCONN_MDI_N<2> — TRD2_N
ENETCONN_MDI_P<3> — TRD3_P
ENETCONN_MDI_N<3> — TRD3_N

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.15 mm VOLTAGE=3.3V

(IPD) GPIO_0/CR_ACT_LED* — NC
GPIO_1/LR_OUT
GPIO_2/MEDIA_SENSE — ENET_MEDIA_SENSE

ENET_SD_DETECT_L

ENET_SD_CMD — R3961 33 5% 1/20W MF 201 — SDCONN_CMD
ENET_SD_CLK — R3979 33 5% 1/20W MF 201 — SDCONN_CLK
ENET_CR_DATA<0> — R3971 33 5% 1/20W MF 201 — SDCONN_DATA<0>
ENET_CR_DATA<1> — R3972 33 5% 1/20W MF 201 — SDCONN_DATA<1>
ENET_CR_DATA<2> — R3973 33 5% 1/20W MF 201 — SDCONN_DATA<2>
ENET_CR_DATA<3> — R3974 33 5% 1/20W MF 201 — SDCONN_DATA<3>
ENET_CR_DATA<4> — R3975 33 5% 1/20W MF 201 — SDCONN_DATA<4>
ENET_CR_DATA<5> — R3976 33 5% 1/20W MF 201 — SDCONN_DATA<5>
ENET_CR_DATA<6> — R3977 33 5% 1/20W MF 201 — SDCONN_DATA<6>
ENET_CR_DATA<7> — R3978 33 5% 1/20W MF 201 — SDCONN_DATA<7>
(IPU-ENET)

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

MS_INS* — NC
(IPU-ENET) CR_LED*/CR_BUS_PWR — ENET_CR_PWREN
(IPU-ENET) CR_WP* — SDCONN_WP
(NO IPU OR IPD-ENET) SR_DISABLE — ENET_SR_DISABLE — R3981 1K 5% 1/16W MF-LF 402
(See note)

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

R3965 1.24K 1% 1/16W MF-LF 402

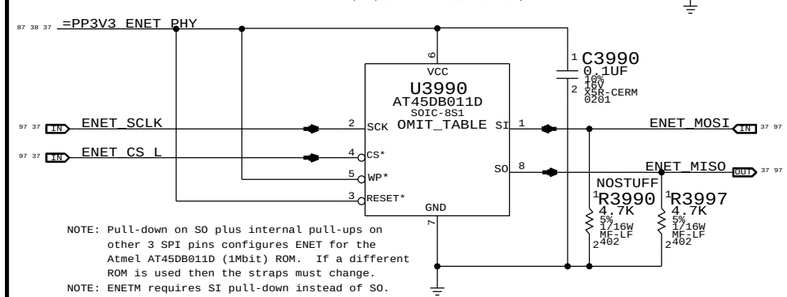
ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
If ENET switching regulator is used, this pin should have a 1K pull-down to GND

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)



NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

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PAGE TITLE
ETHERNET PHY (CAESAR IV)

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PAGE 39 OF 127
SHEET 37 OF 106

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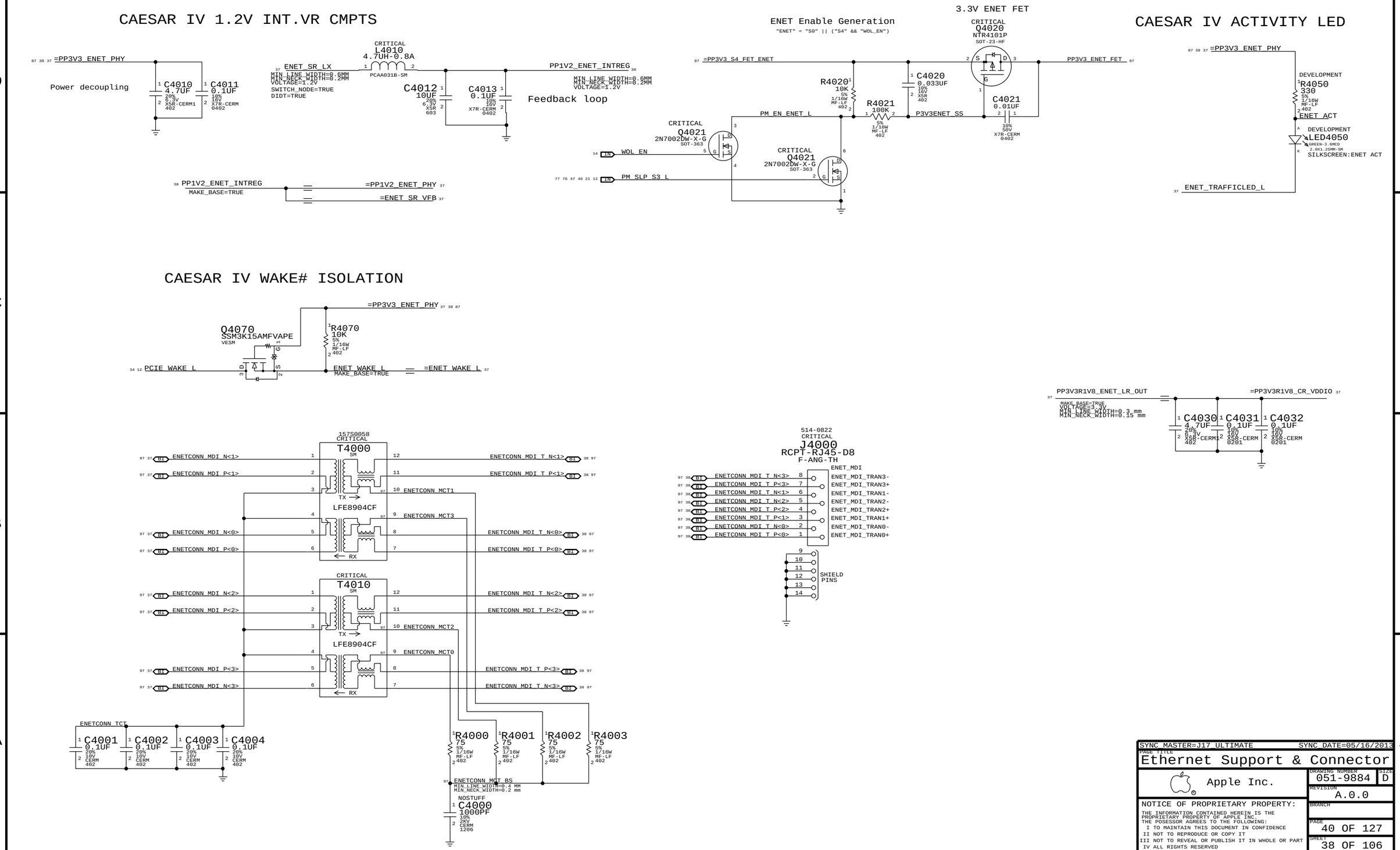

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: Ethernet Support & Connector

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DRAWING NUMBER: 051-9884 SIZE: D

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PAGE: 40 OF 127

SHEET: 38 OF 106

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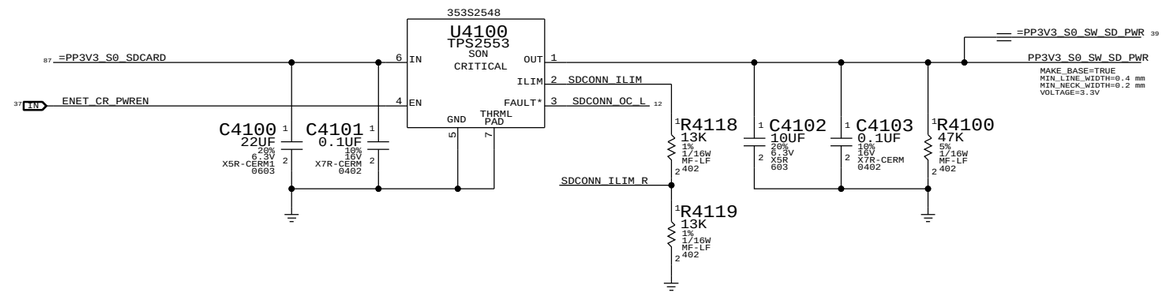
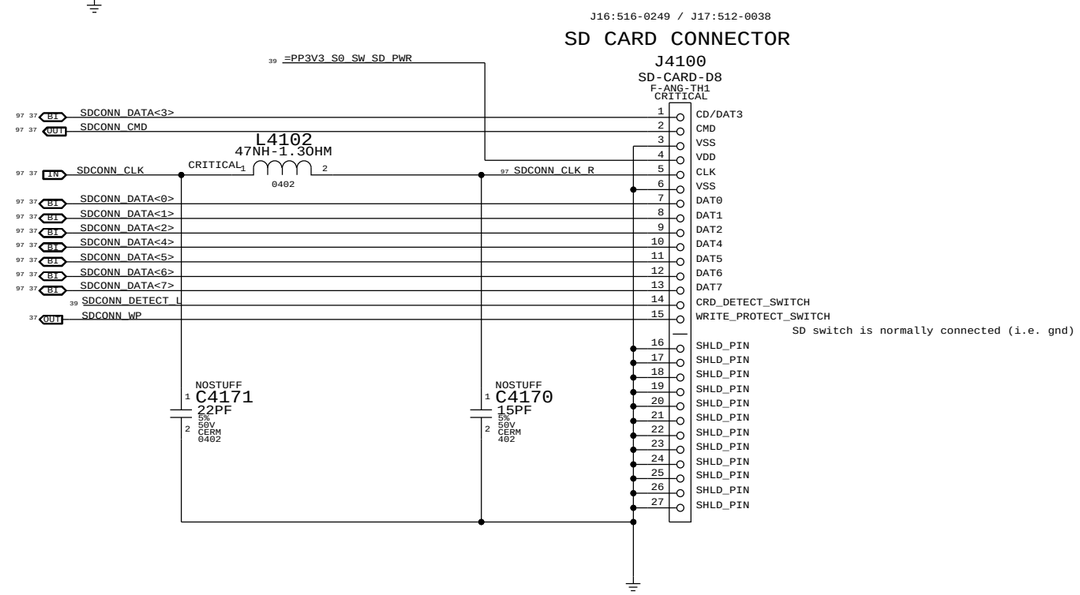
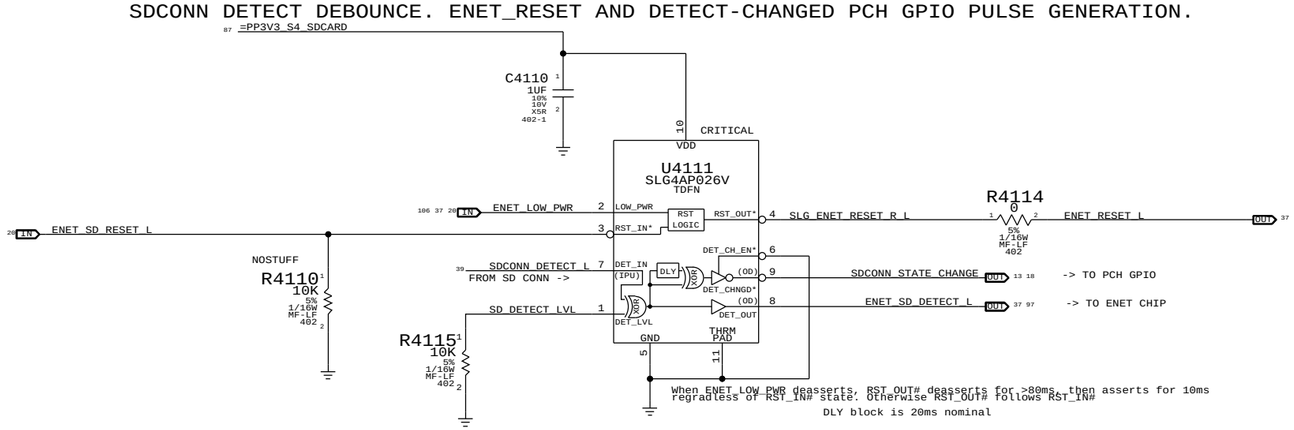
SD CARD 3.3V OVERCURRENT PROTECTION CHIP



SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
SD READER CONNECTOR

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PAGE 41 OF 127

SHEET 39 OF 106

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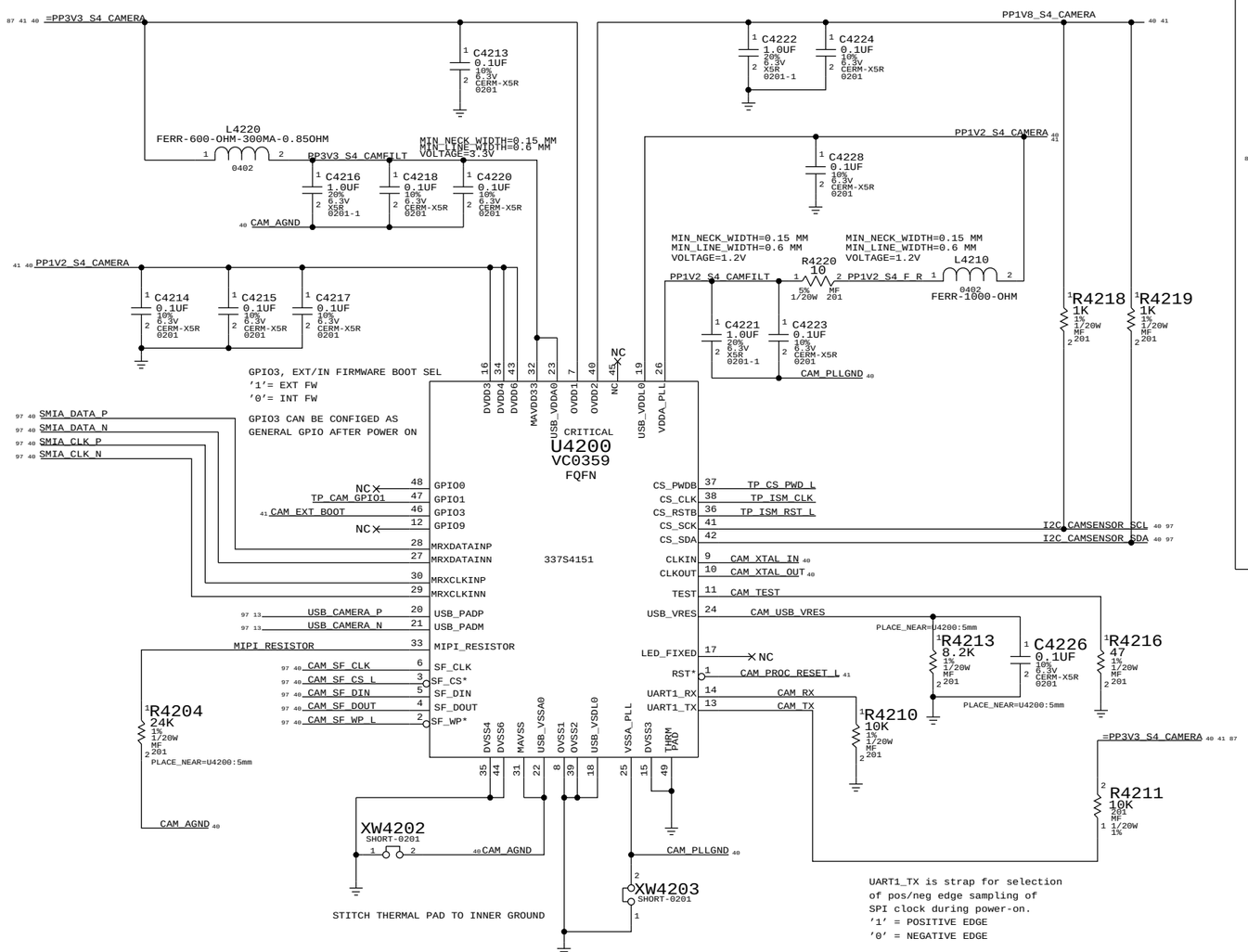
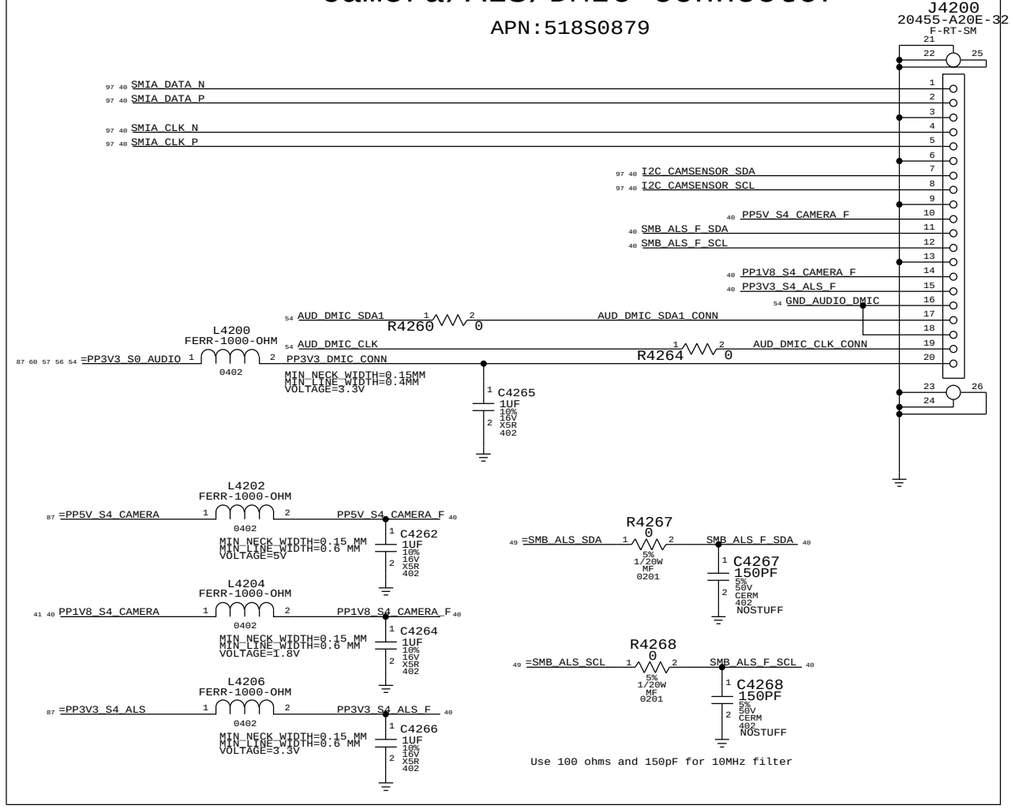
USB CAMERA CONTROLLER

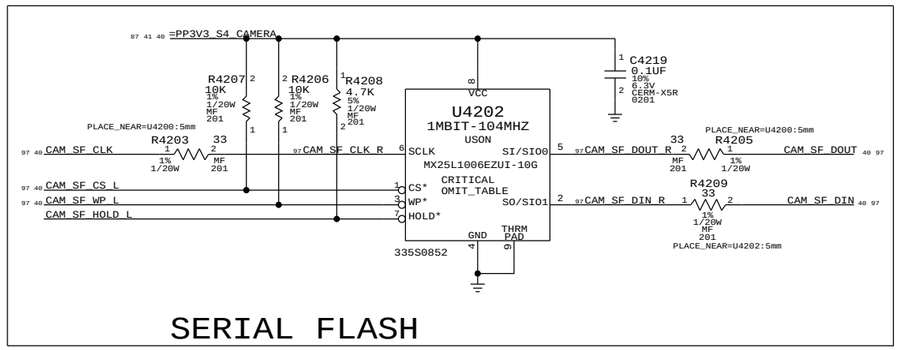


Camera/ALS/DMIC connector

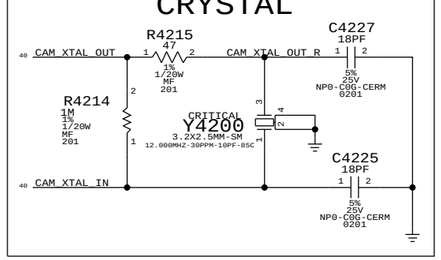
APN:518S0879



SERIAL FLASH



CRYSTAL



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: Camera Controller

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DRAWING NUMBER: 051-9884 SIZE: D

REVISION: A.0.0

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PAGE: 42 OF 127

SHEET: 40 OF 106

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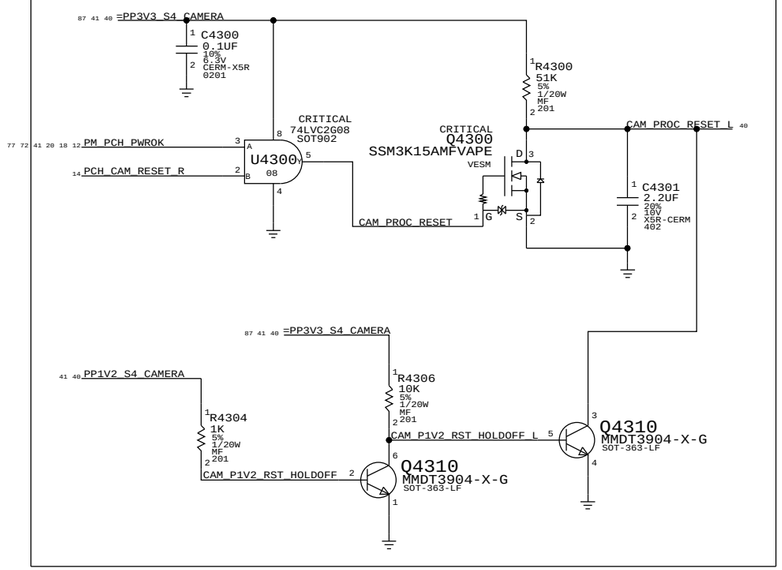
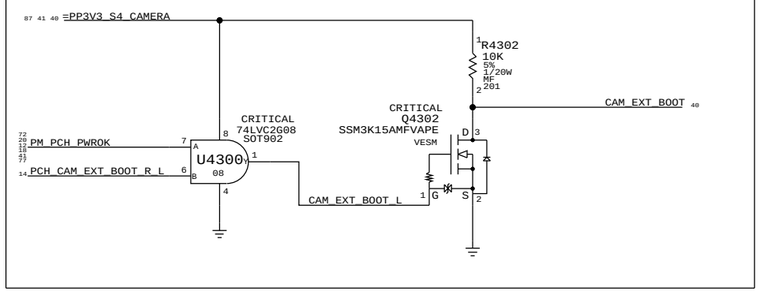
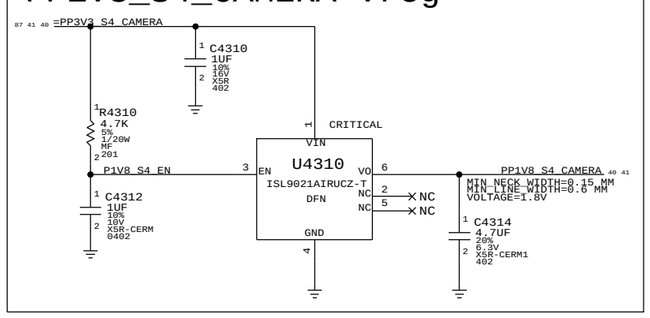
Camera Processor Reset



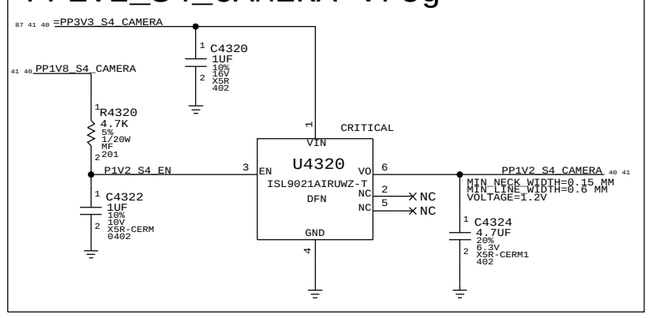
Camera Processor ExtBoot Cntl



PP1V8_S4_CAMERA Vreg



PP1V2_S4_CAMERA Vreg



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PAGE TITLE
Camera Controller Support

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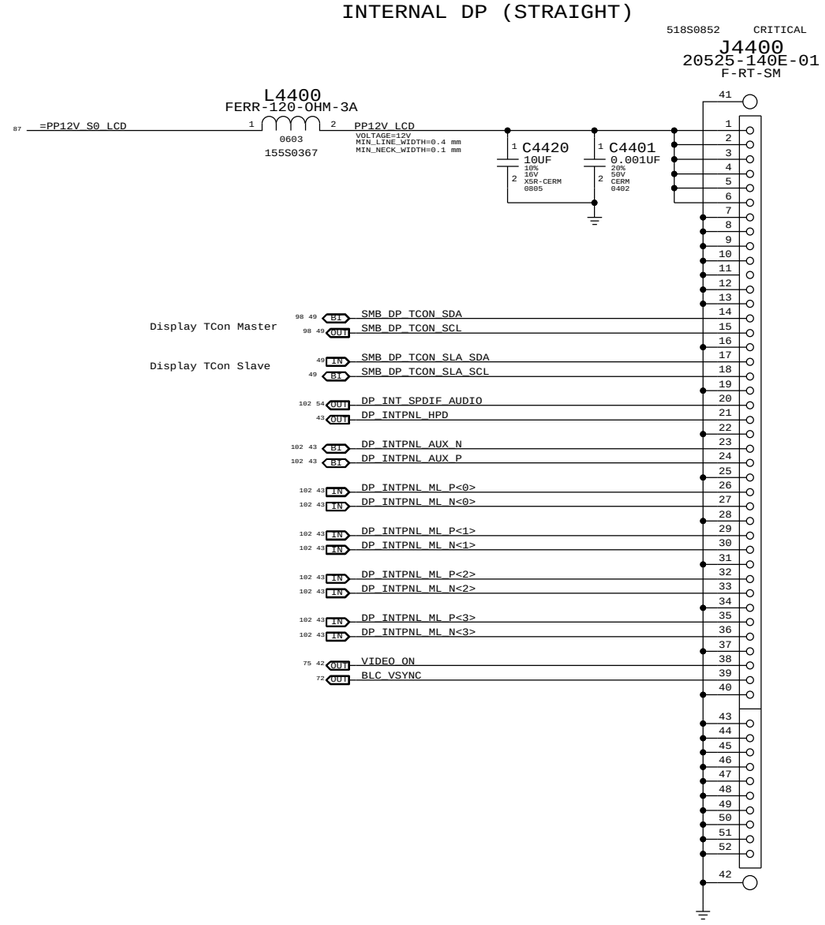
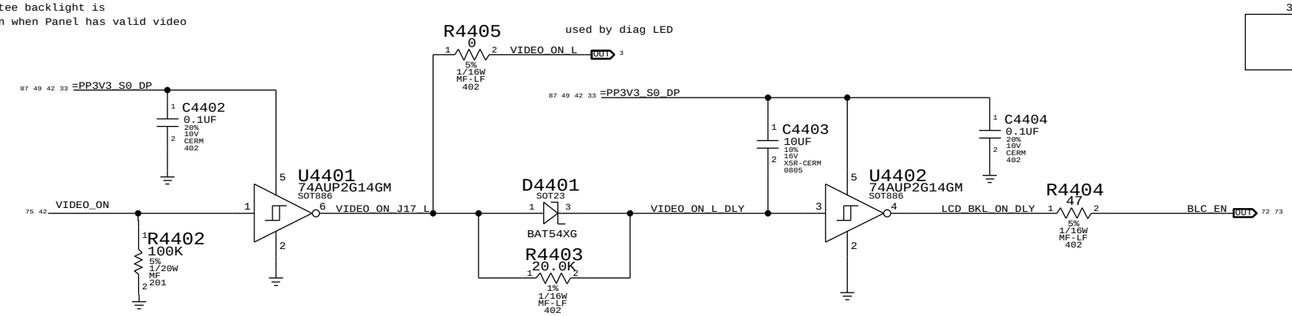
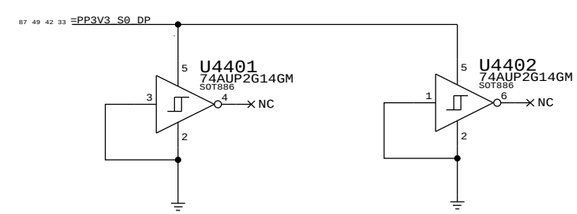
INTERNAL DP (STRAIGHT)



BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video





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PAGE TITLE
Internal DP Support

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PAGE 44 OF 127

SHEET 42 OF 106

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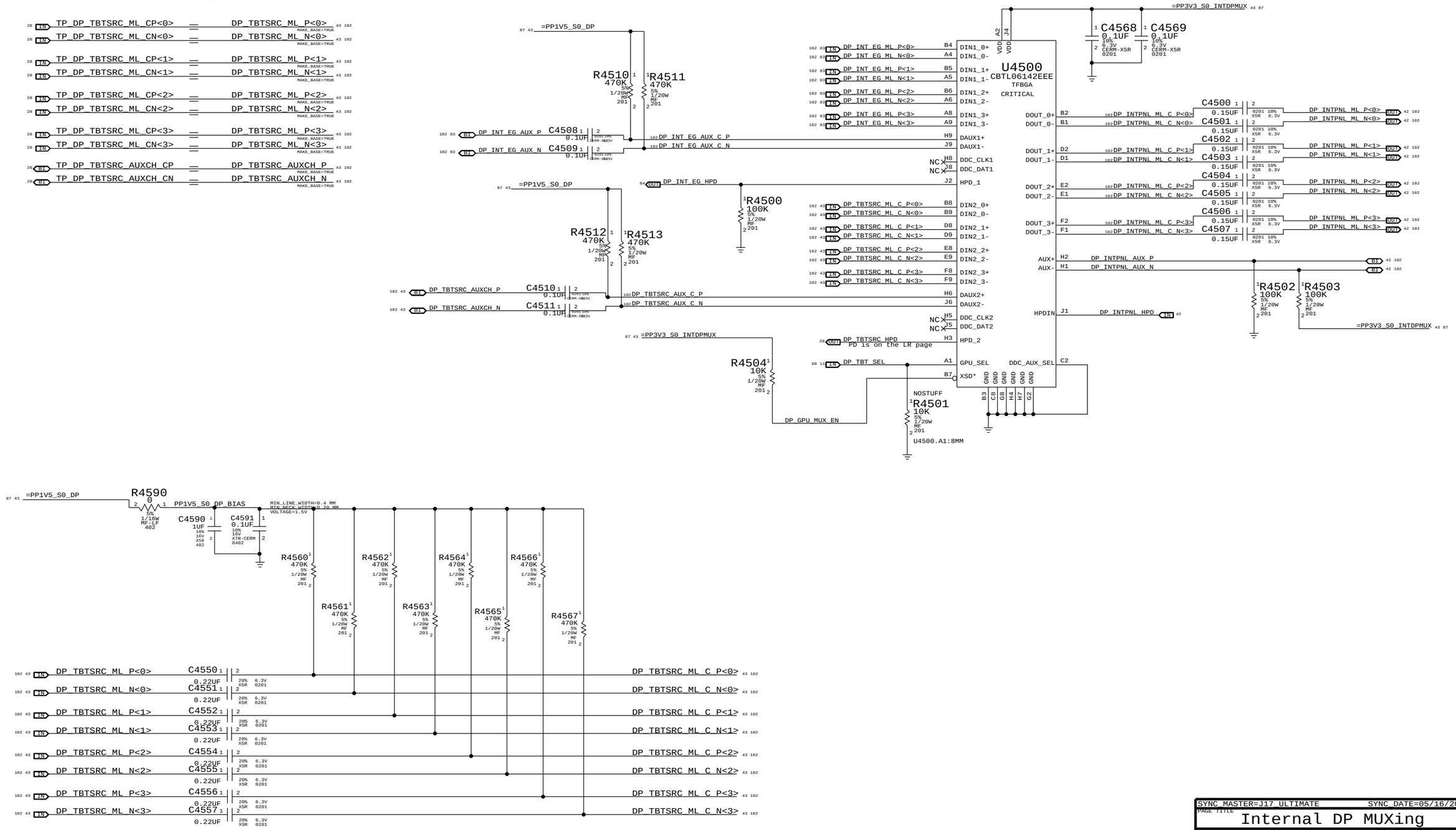
TP to DP aliases

TP_DP_TBTSRC_ML_CP<0>	=	DP_TBTSRC_ML_P<0>
TP_DP_TBTSRC_ML_CN<0>	=	DP_TBTSRC_ML_N<0>
TP_DP_TBTSRC_ML_CP<1>	=	DP_TBTSRC_ML_P<1>
TP_DP_TBTSRC_ML_CN<1>	=	DP_TBTSRC_ML_N<1>
TP_DP_TBTSRC_ML_CP<2>	=	DP_TBTSRC_ML_P<2>
TP_DP_TBTSRC_ML_CN<2>	=	DP_TBTSRC_ML_N<2>
TP_DP_TBTSRC_ML_CP<3>	=	DP_TBTSRC_ML_P<3>
TP_DP_TBTSRC_ML_CN<3>	=	DP_TBTSRC_ML_N<3>
TP_DP_TBTSRC_AUXCH_CP	=	DP_TBTSRC_AUXCH_P
TP_DP_TBTSRC_AUXCH_CN	=	DP_TBTSRC_AUXCH_N



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: Internal DP MUXing

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DRAWING NUMBER: 051-9884 SIZE: D

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PAGE: 45 OF 127

SHEET: 43 OF 106

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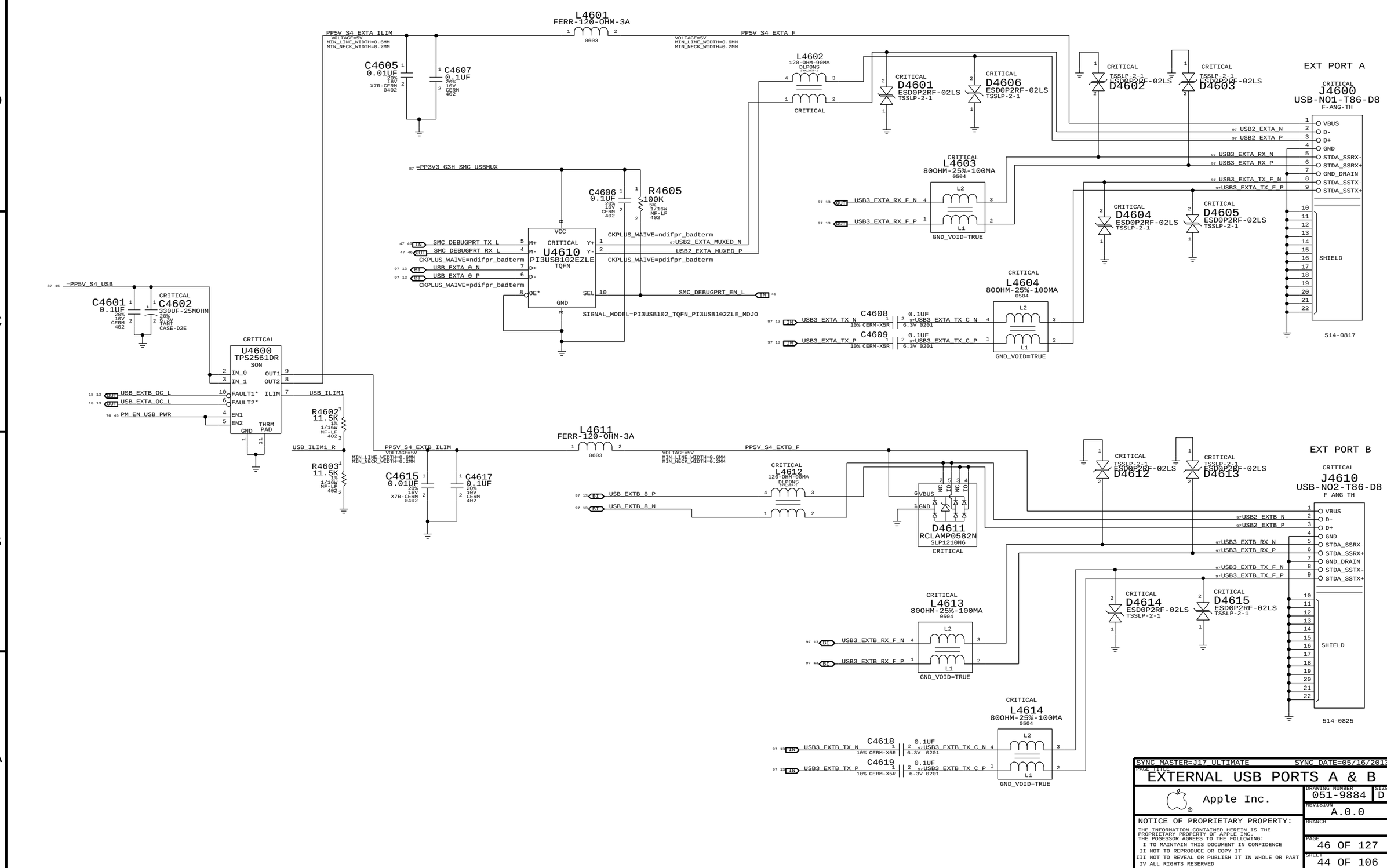

SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE
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PAGE 46 OF 127

SHEET 44 OF 106

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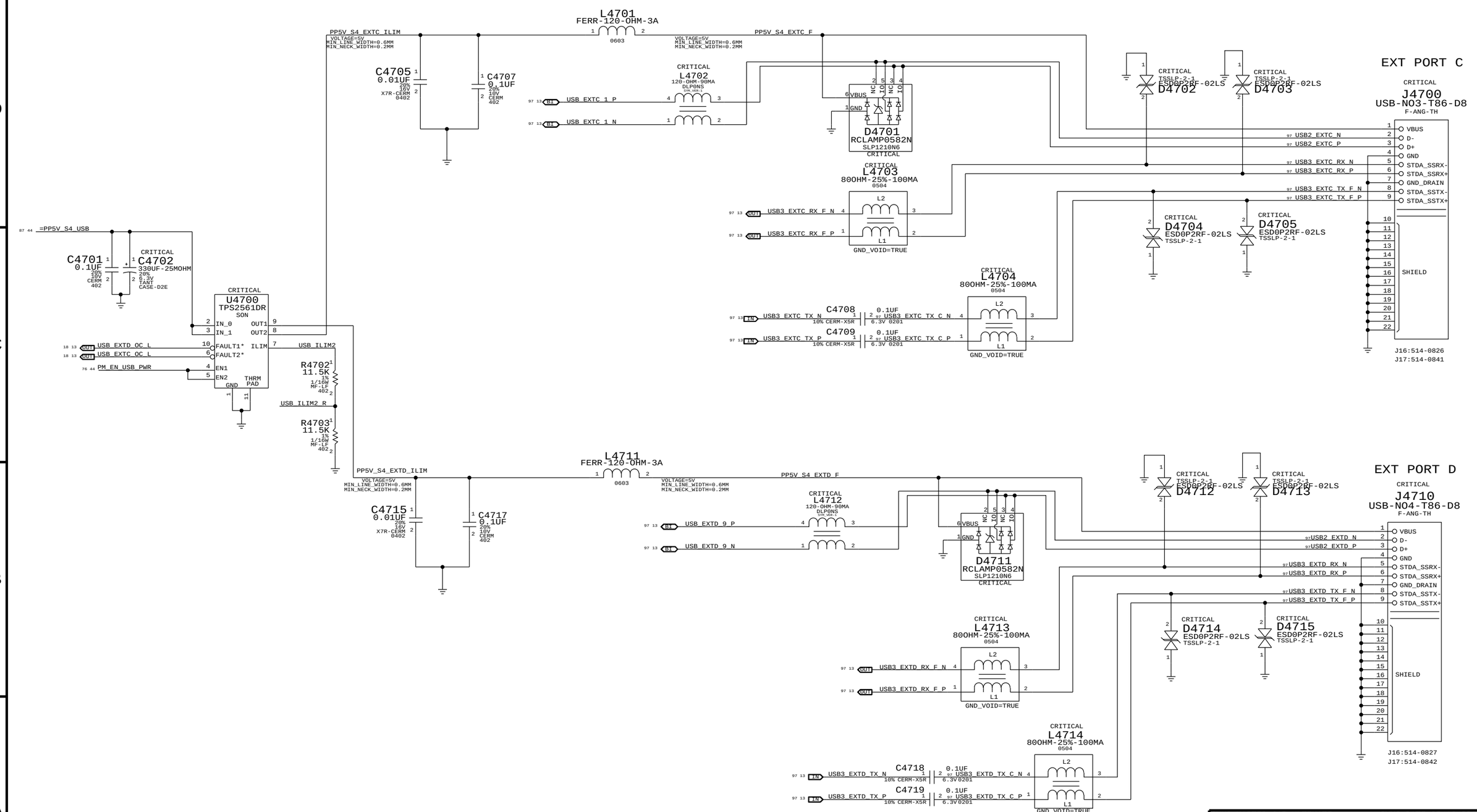

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PAGE TITLE
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PAGE 47 OF 127

SHEET 45 OF 106

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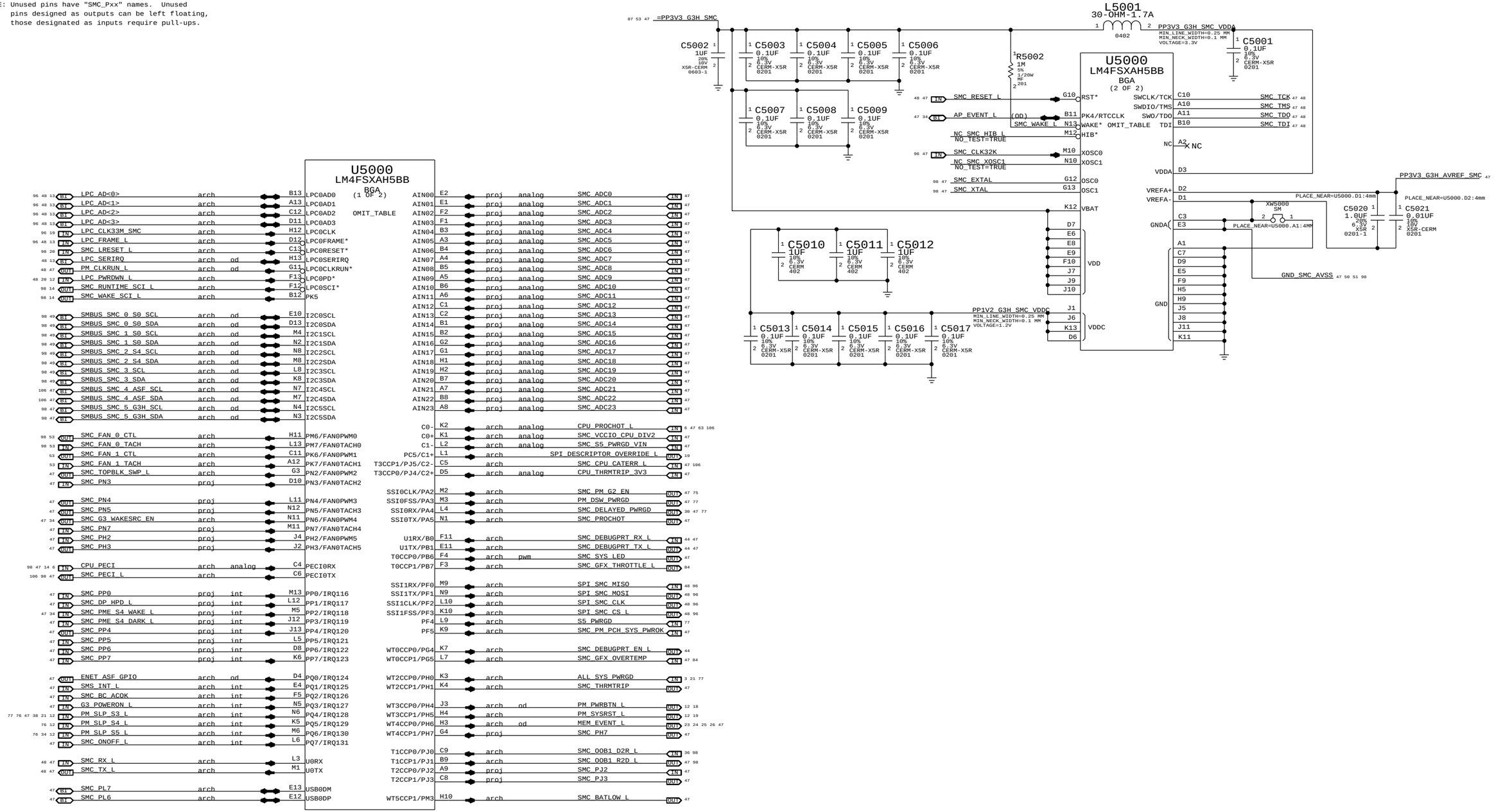
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



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PAGE TITLE
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PAGE 50 OF 127

SHEET 46 OF 106

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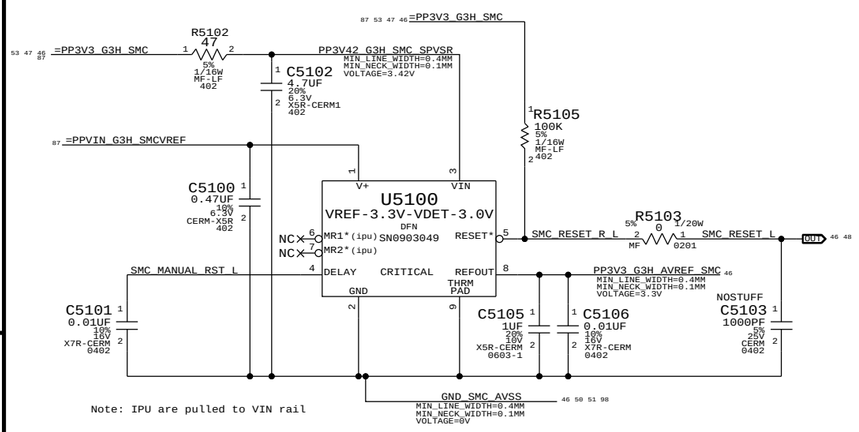
SMC Supervisor and AVREF Supply



Note: IPU are pulled to VIN rail

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE	
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE	
SMC_ADC2	VSNS_P12VS0_GPUCORE	MAKE_BASE=TRUE	
SMC_ADC3	ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE	
SMC_ADC4	VSNS_P1V5S0	MAKE_BASE=TRUE	
SMC_ADC5	ISNS_P1V5S0	MAKE_BASE=TRUE	
SMC_ADC6	VSNS_VDDQS3_DDR	MAKE_BASE=TRUE	
SMC_ADC7	ISNS_VDDQS3_DDR	MAKE_BASE=TRUE	
SMC_ADC9	ISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	
SMC_ADC10	VSNS_CPUVCC	MAKE_BASE=TRUE	
SMC_ADC11	ISNS_CPUVCC	MAKE_BASE=TRUE	
SMC_ADC12	VSNS_GPUCORE_ALT	MAKE_BASE=TRUE	
SMC_ADC13	ISNS_GPUCORE_ALT	MAKE_BASE=TRUE	
SMC_ADC14	VSNS_HDDS0	MAKE_BASE=TRUE	
SMC_ADC15	ISNS_HDDS0	MAKE_BASE=TRUE	
SMC_ADC17	VSNS_P1V05S0_PCH	MAKE_BASE=TRUE	
SMC_ADC18	ISNS_P12VS0_HDD	MAKE_BASE=TRUE	
SMC_ADC19	ISNS_P3V3S4_AP	MAKE_BASE=TRUE	
SMC_ADC20	ISNS_SSDS0	MAKE_BASE=TRUE	
SMC_ADC21	VSNS_P3V3S5	MAKE_BASE=TRUE	
SMC_ADC8	VSNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	

Unused ADC Channels

SMC_PH3	NC_SMC_PH3	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_ADC16	NC_SMC_ADC16	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_ADC22	NC_SMC_ADC22	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_ADC23	NC_SMC_ADC23	MAKE_BASE=TRUE	NO_TEST=TRUE

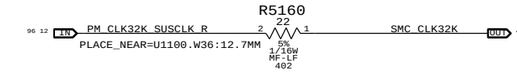
Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE	
SMC_PJ3	SMC_OOB2_R2D_L	MAKE_BASE=TRUE	
SMC_PJ2	SMC_OOB2_D2R_L	MAKE_BASE=TRUE	
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE	
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE	
SMC_PL6	SMC_WIFI_PWR_EN	MAKE_BASE=TRUE	

Unused Project-specific

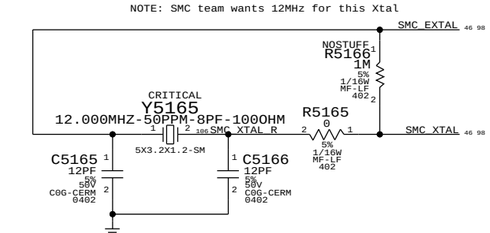
SMC_PL7	NC_SMC_PL7	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PN4	NC_SMC_PN4	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE	NO_TEST=TRUE
TP for access if ZPB re-intstated			
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE	NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE	NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE	NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_S5_PWRGD_VIN	NC_SMC_S5_PWRGD_VIN	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_OOB1_R2D_L	NC_SMC_OOB1_R2D_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_BATLOW_L	NC_SMC_SMC_BATLOW_L	MAKE_BASE=TRUE	NO_TEST=TRUE

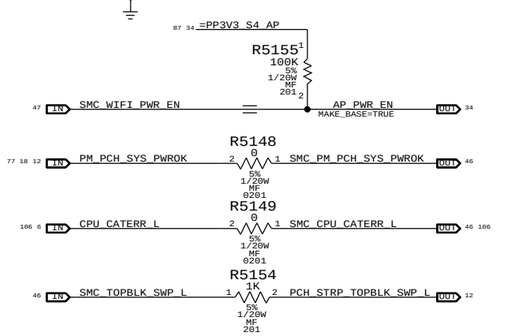
SMC 32KHz Clock



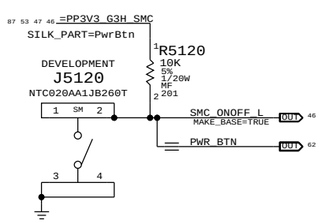
SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal



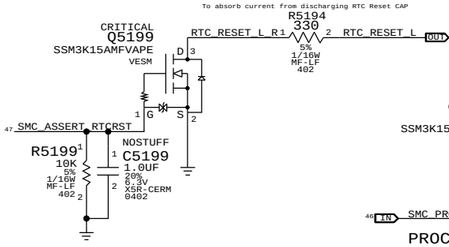


Power Button



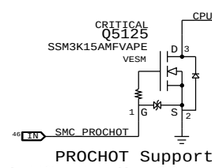
SMC Controlled RTC Reset

To absorb current from discharging RTC Reset CAP



PROCHOT Support

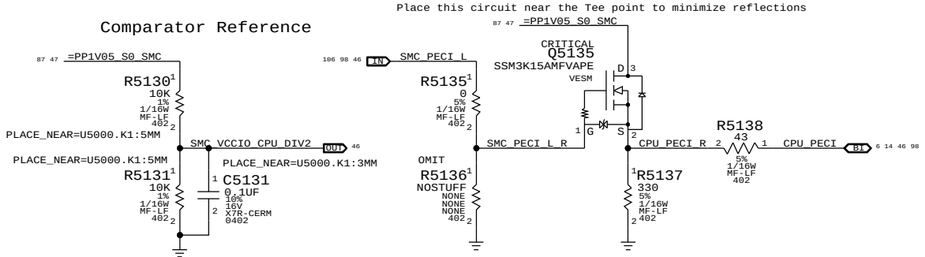
Level-shifter that allows SMC to drive PROCHOT



PECI Support

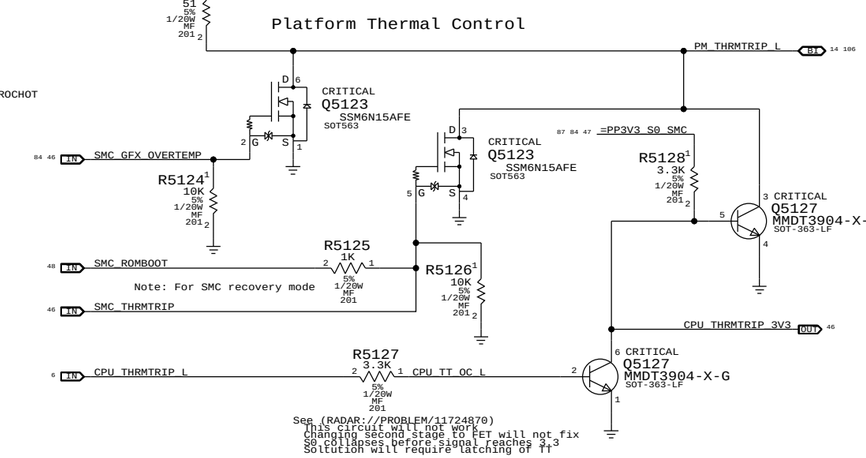
Level-shifter that allows SMC to drive PECI

Place this circuit near the Tee point to minimize reflections



Comparator Reference

Platform Thermal Control



See (RADAR://PROBLEM/11724870)
This circuit will not work
Changing second stage to FET will not fix
So collapses before signal reaches 2.3
Solution will require latching of TT

Arch Pull Up/Down

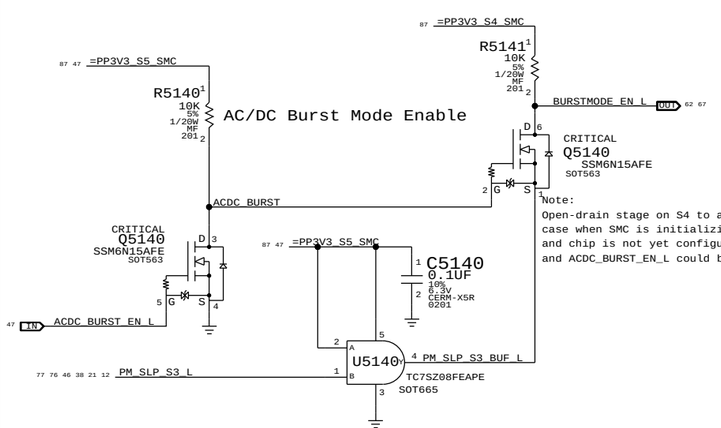
MEM_EVENT_L	R5170	10K	1/20W MF 201	=PP3V3_S0_SMC	87 84 47
PM_CLKRUN_L	R5171	10K	1/20W MF 201		
ENET_ASF_GPIO	R5175	10K	1/20W MF 201	=PP3V3_G3H_SMC	87 53 47 46
G3_POWERON_L	R5176	10K	1/20W MF 201		
SMC_BC_ACOK	R5178	100K	1/20W MF 201		
SMC_SYS_LED	R5179	100K	1/20W MF 201		
SMS_INT_L	R5180	10K	1/20W MF 201		
SMC_PME_S4_WAKE_L	R5181	10K	1/20W MF 201		
AP_EVENT_L	R5185	10K	1/20W MF 201	PP3V3_S4_AP_FET	34
SMC_G3_WAKESRC_EN	R5118	100K	1/20W MF 201		
SMC_DELAYED_PWRGD	R5186	100K	1/16W MF-LF 402		
PM_DSW_PWRGD	R5184	100K	1/16W MF-LF 402		
SMC_PM_G2_EN	R5187	100K	1/20W MF 201		

Note:

Serial/JTAG Interface Pull-ups

SMC_TX_L	R5190	10K	1/20W MF 201	=PP3V3_G3H_SMC	87 53 47 46
SMC_RX_L	R5191	100K	1/20W MF 201		
SMC_TCK	R5195	10K	1/20W MF 201		
SMC_TDI	R5196	10K	1/20W MF 201		
SMC_TDO	R5197	10K	1/20W MF 201		
SMC_TMS	R5198	10K	1/20W MF 201		
SMC_DEBUGPRT_TX_L	R5192	20K	1/20W MF 201		
SMC_DEBUGPRT_RX_L	R5193	20K	1/20W MF 201		

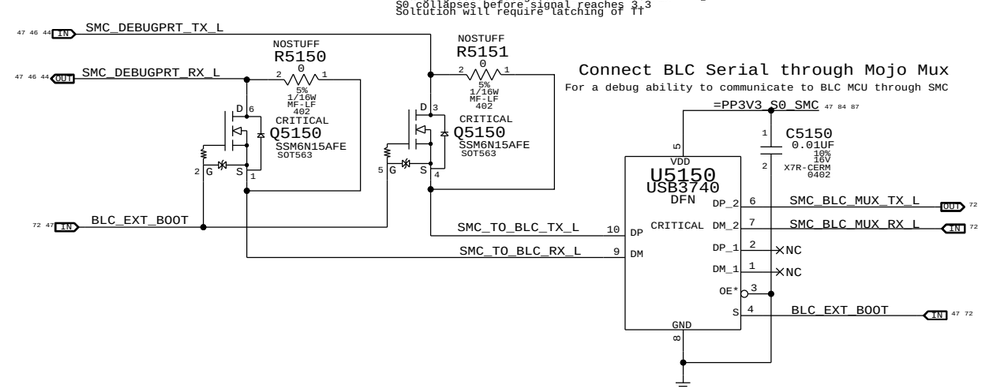
AC/DC Burst Mode Enable



Note:
Open-drain stage on S4 to account case when SMC is initializing in S5, and chip is not yet configured. and ACDC_BURST_EN_L could be floating.

Connect BLC Serial through Mojo Mux

For a debug ability to communicate to BLC MCU through SMC



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SMC Support

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PAGE 51 OF 127

SHEET 47 OF 106

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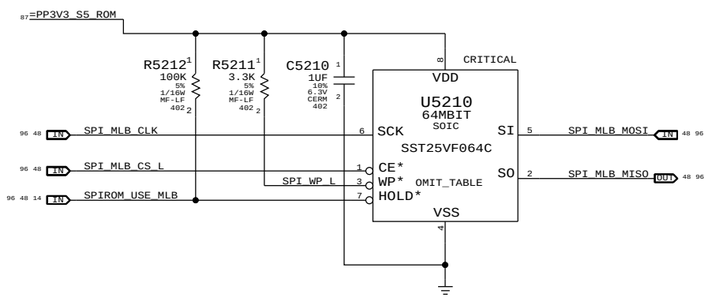
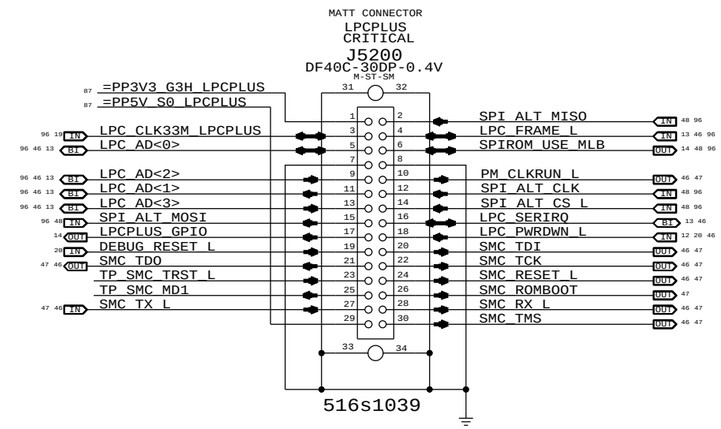
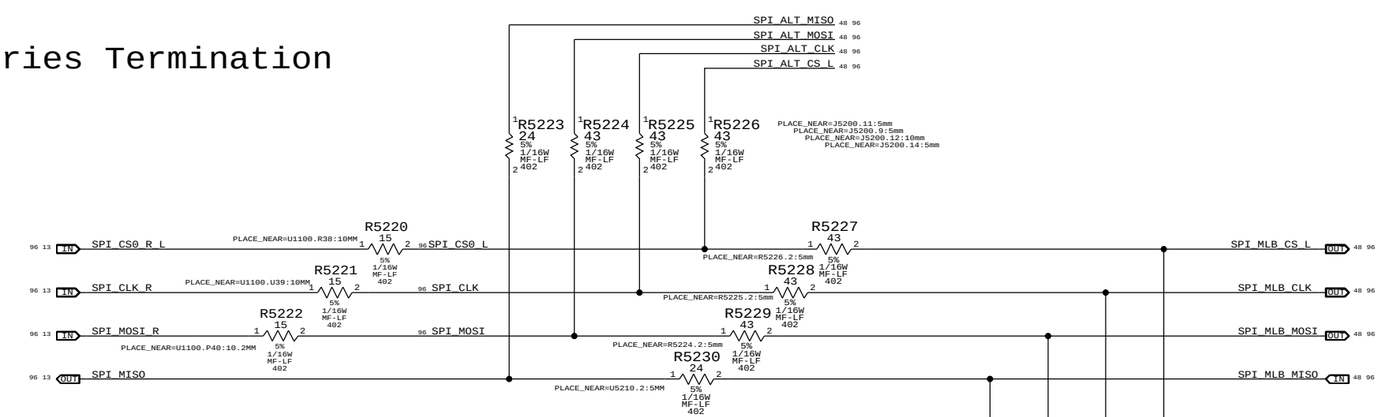
SPI BootROM



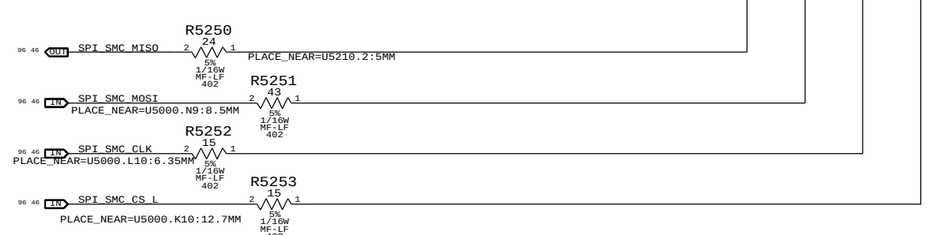
LPC+SPI Connector



SPI Series Termination



SMC SPI Support



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PAGE TITLE
SPI and Debug Connector

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SHEET 48 OF 106

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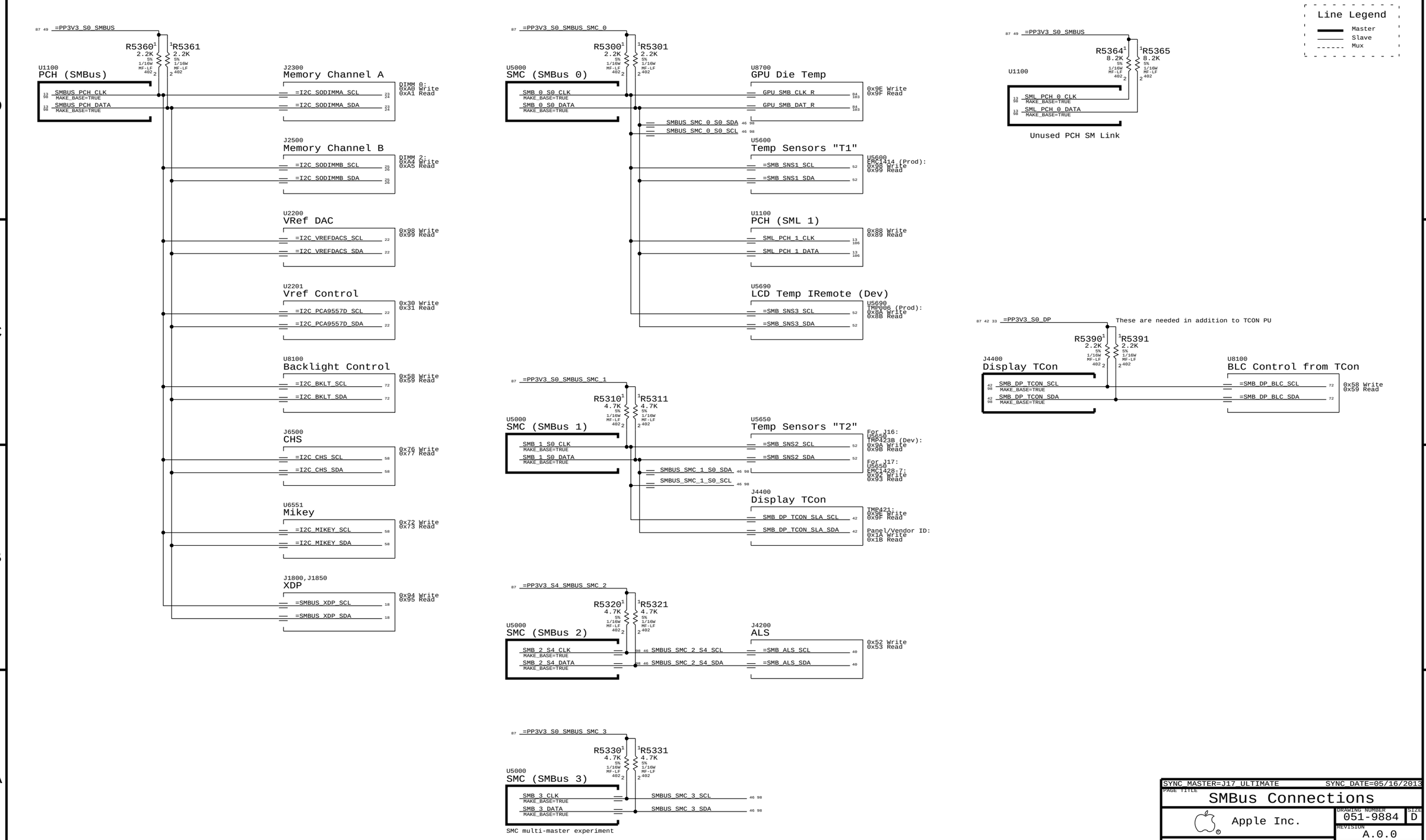

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SMBus Connections

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PAGE 53 OF 127

SHEET 49 OF 106

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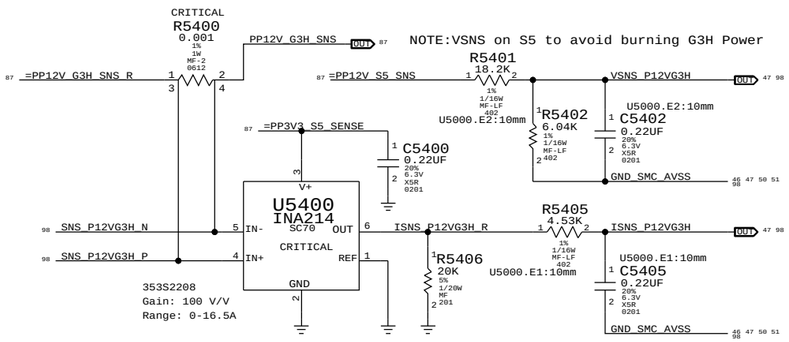
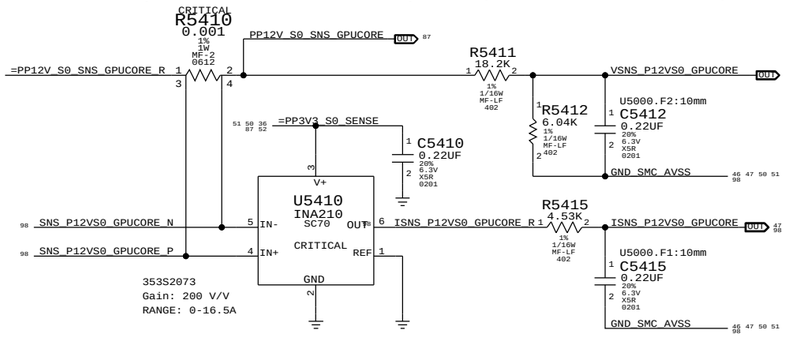
12V G3H (VD2R:ADC0/ID2R:ADC1) AC/DC lowside sense (System total)

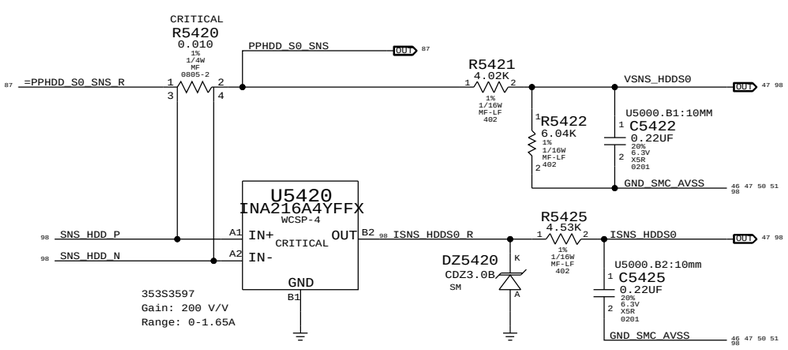


GPU Core (VG1C:ADC2/IG1C:ADC3) GPU highside sense for GPU Core Regulator

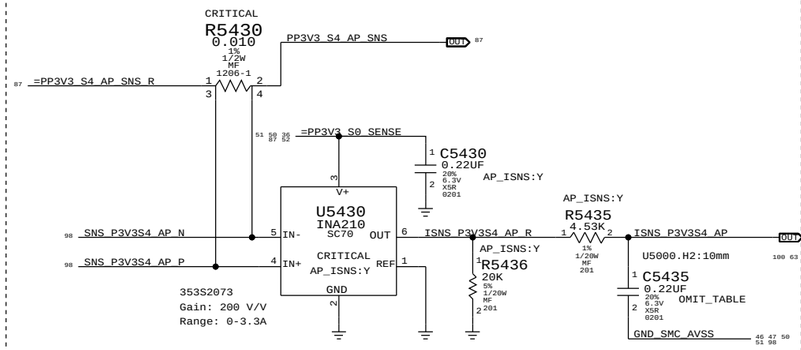


HDD S0 (VH05:ADC14/IH05:ADC15)

I/V-sense for HDD (Development, but need R5420)



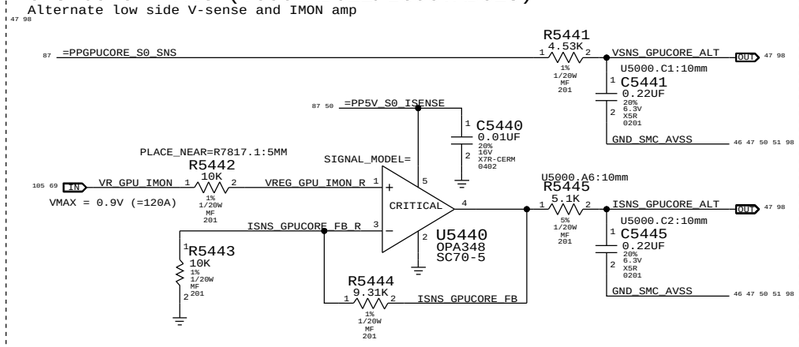
PP3V3_S4_AP (IW0R:ADC19) Airport supply current sense



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	1	CAP,0.22UF,201	C5435	AP_ISNS:Y
117S0201	1	RES,0 OHM,201	C5435	AP_ISNS:N

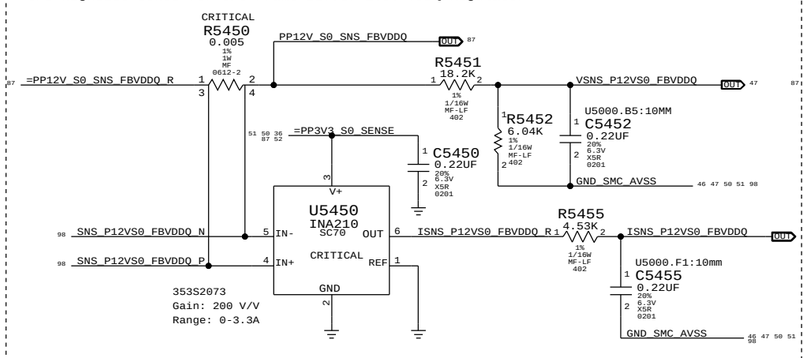
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)

Alternate low side V-sense and IMON amp



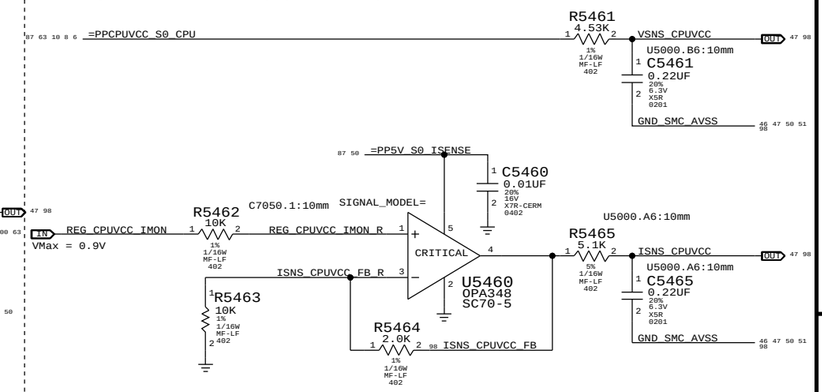
GPU FB (VG0F:ADC8/IG0F:ADC9)

GPU highside sense for GPU Frame Buffer 1.5V VDDQ Regulator



CPU Core (VC0C:ADC10/IC0C:ADC11)

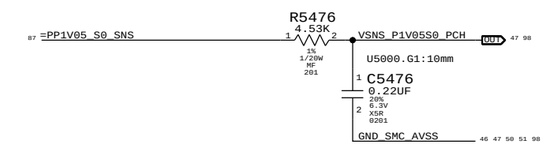
Voltage sense and IMON amp (VC0C, IC0C)



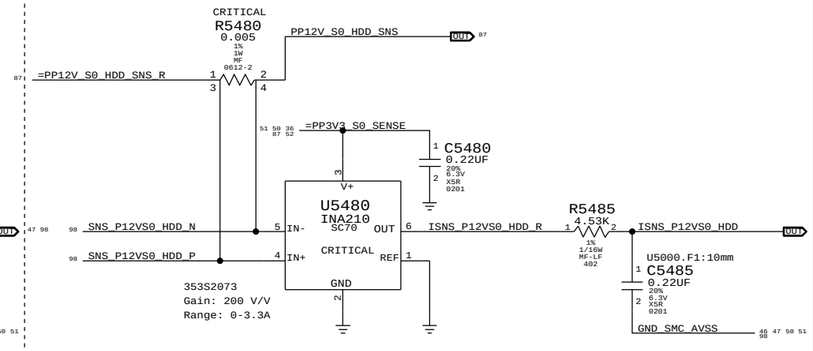
PP1V05_S0_PCH (VR1R:ADC17)

I/V-sense for PP1V05_S0_PCH

Since PP1V05 Vreg feedback is coming
from near GPU, place this sensor near PCH.



PP12V_S0_HDD (IH02:ADC18) HDD 12V CURRENT SENSE



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PAGE TITLE
I and V Sense

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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PAGE 54 OF 127

SHEET 50 OF 106

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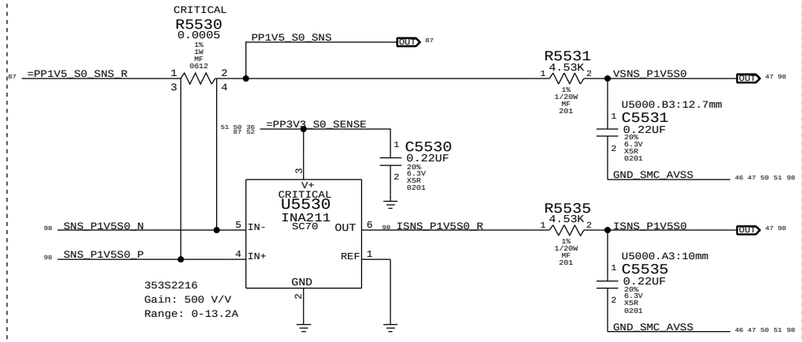
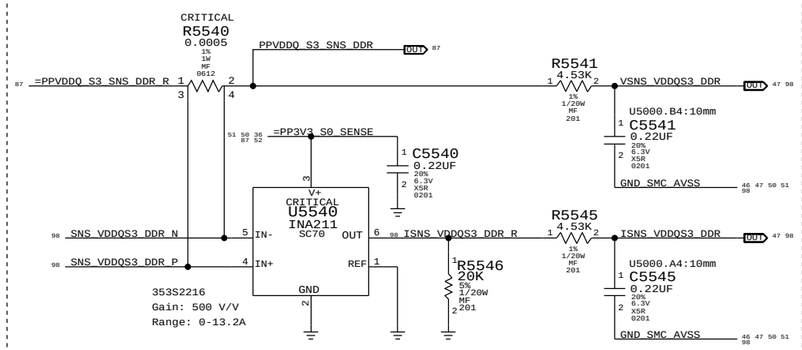
PP1V5_S0 (VC0M:ADC4/IC0M:ADC5)

lowside sense for VCCVRM,PCH,CPU mem, audio



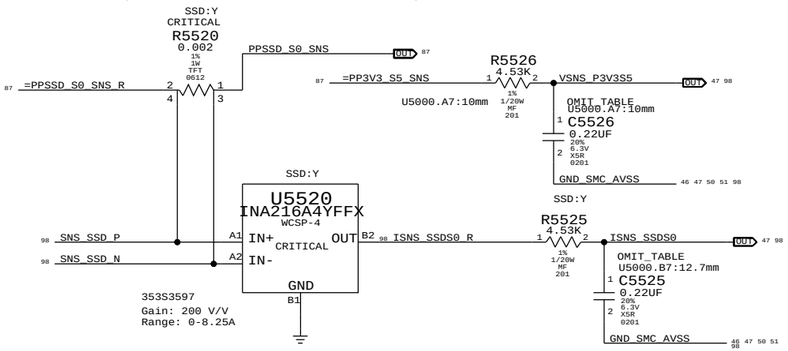
VDDQ S3 (VM0R:ADC6/IM0R:ADC7)

VDDQ lowside sense for SO-DIMM modules



SSD S0 (IH1R:ADC20/VR3R:ADC21)

I-sense for SSD / V-sense for PP3V3_S5)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5525,C5526	SSD:Y
117S0201	2	RES,0 OHM,201	C5525,C5526	SSD:N

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

I and V Sense(Continued)

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DRAWING NUMBER 051-9884 SIZE D

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PAGE 55 OF 127

SHEET 51 OF 106

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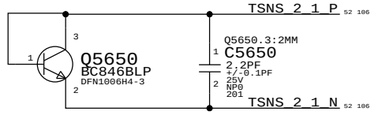
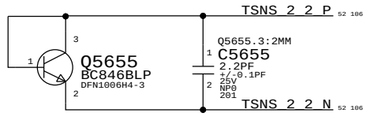
Temperature Sensor T2 EMC1428: Near GPU VR

GPU Proximity



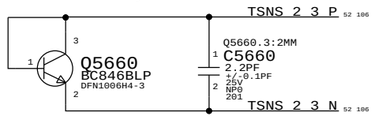
PLACEMENT_NOTE=Place Q5550 near GPU and GDDR5

Ambient



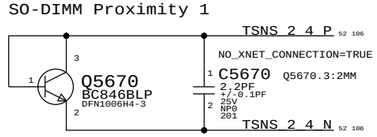
PLACEMENT_NOTE=Place Q5555 near bottom of board

BLC Proximity



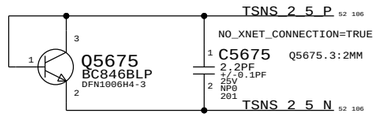
PLACEMENT_NOTE=Place Q5560 near BLC VR

SO-DIMM Proximity 1



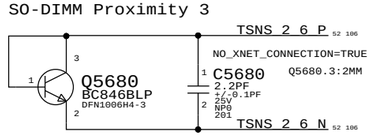
PLACEMENT_NOTE=Place Q5570 near SO-DIMM connectors (top left)

SO-DIMM Proximity 2



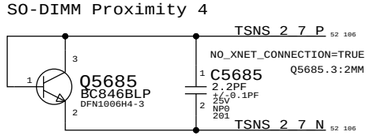
PLACEMENT_NOTE=Place Q5575 near SO-DIMM connectors (top right)

SO-DIMM Proximity 3



PLACEMENT_NOTE=Place Q5580 near SO-DIMM connectors (bottom left)

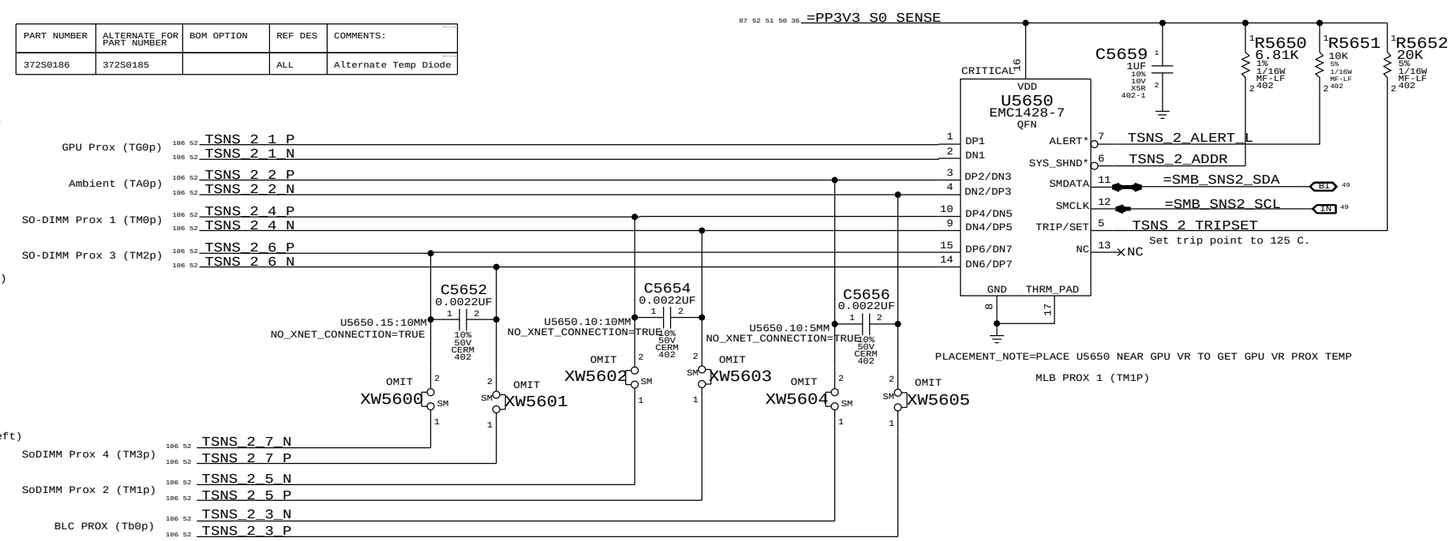
SO-DIMM Proximity 4



PLACEMENT_NOTE=Place Q5585 near SO-DIMM connectors (bottom right)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

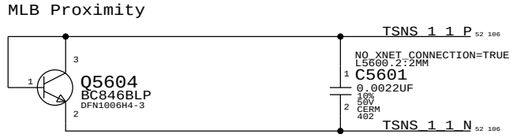
SNS T2: TEMP SENSOR IC



EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

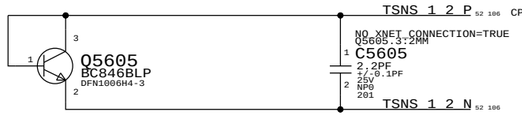
Temperature Sensor T1 EMC1414: Near PSU Conn

MLB Proximity



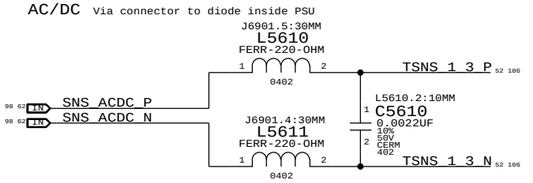
PLACEMENT_NOTE=PLACE Q5504 UNDER CPU

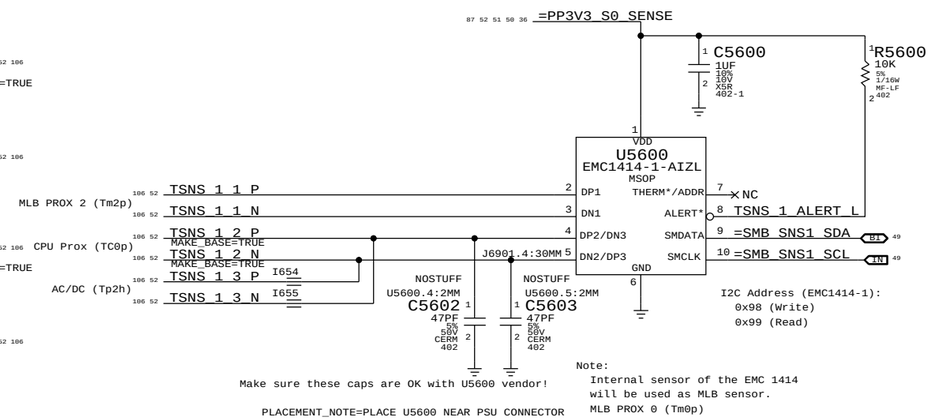
CPU Proximity



PLACEMENT_NOTE=PLACE Q5505 NEAR CPU

AC/DC Via connector to diode inside PSU



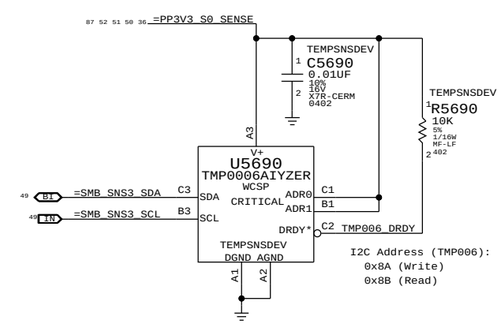


Make sure these caps are OK with U5600 vendor!

PLACEMENT_NOTE=PLACE U5600 NEAR PSU CONNECTOR

Note:
Internal sensor of the EMC 1414
will be used as MLB sensor.
MLB PROX 0 (Tm0p)

Temperature Sensor T3: LCD Remote Sensor(Dev Only)



NOTE - Follow TI layout guide (SBOU108.pdf) for this part!!!

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PAGE TITLE
Temperature Sensors

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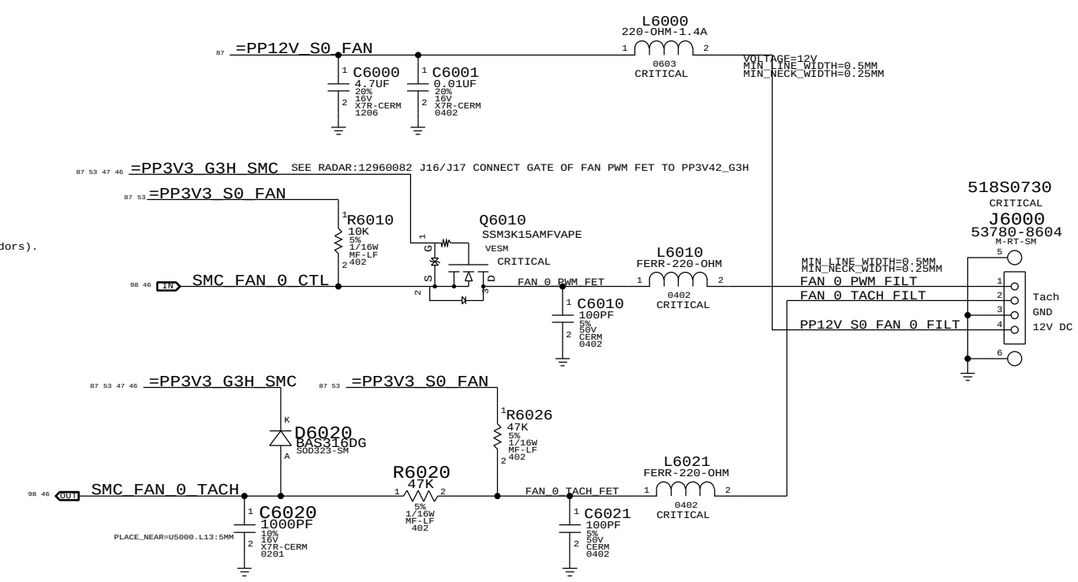
Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).

SMC Fan 0 (System)



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

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PAGE TITLE
System Fan

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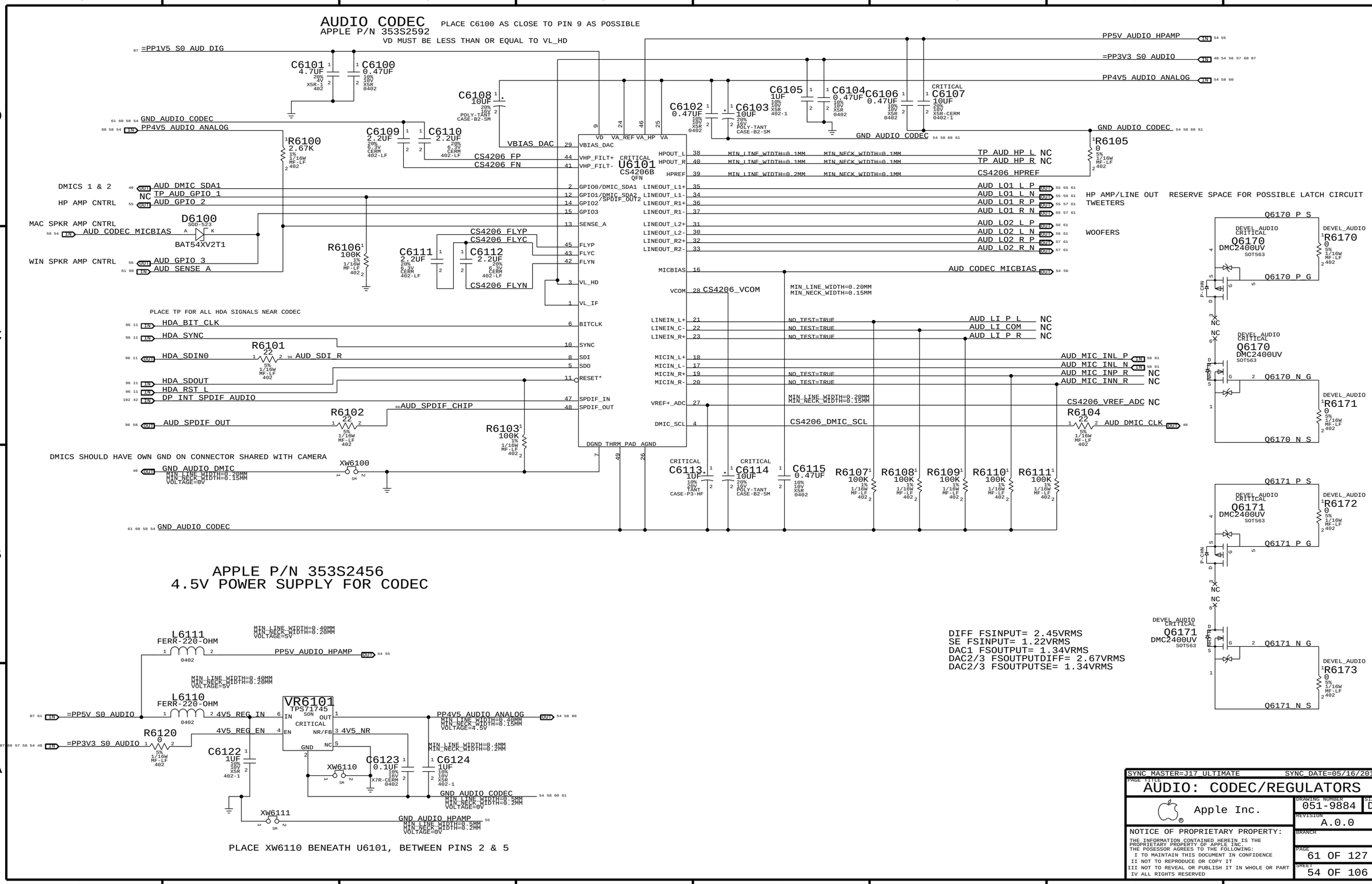
AUDIO CODEC
APPLE P/N 353S2592
PLACE C6100 AS CLOSE TO PIN 9 AS POSSIBLE
VD MUST BE LESS THAN OR EQUAL TO VL_HD
=PP1V5_S0_AUD_DIG
C6101 4.7UF
C6100 0.47UF
C6108 10UF
C6109 2.2UF
C6110 2.2UF
R6100 2.67K
GND_AUDIO_CODEC
PP4V5_AUDIO_ANALOG
VBIAS_DAC
CS4206_FP
CS4206_FN
U6101
CS4206B
QFN
DMICS 1 & 2
HP AMP CNTRL
MAC SPKR AMP CNTRL
WIN SPKR AMP CNTRL
AUD_DMIC_SDA1
TP_AUD_GPIO_1
AUD_GPIO_2
D6100
BAT54XV2T1
AUD_CODEC_MICBIAS
AUD_GPIO_3
AUD_SENSE_A
R6106 100K
C6111 2.2UF
C6112 2.2UF
CS4206_FLYP
CS4206_FLYC
CS4206_FLYN
PLACE TP FOR ALL HDA SIGNALS NEAR CODEC
HDA_BIT_CLK
HDA_SYNC
HDA_SDIN0
HDA_SDOUT
HDA_RST_L
DP_INT_SPDIF_AUDIO
AUD_SPDIF_OUT
R6101 22
AUD_SDI_R
R6102 22
AUD_SPDIF_CHIP
R6103 100K
DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA
GND_AUDIO_DMIC
XW6100
PP5V_AUDIO_HPAMP
=PP3V3_S0_AUDIO
PP4V5_AUDIO_ANALOG
C6105 1UF
C6104 0.47UF
C6106 0.47UF
C6107 10UF
C6102 0.47UF
C6103 10UF
GND_AUDIO_CODEC
R6105 0
HPOUT_L
HPOUT_R
HPREF
TP_AUD_HP_L
TP_AUD_HP_R
CS4206_HPREF
LINEOUT_L1+
LINEOUT_L1-
LINEOUT_R1+
LINEOUT_R1-
LINEOUT_L2+
LINEOUT_L2-
LINEOUT_R2+
LINEOUT_R2-
AUD_LO1_L_P
AUD_LO1_L_N
AUD_LO1_R_P
AUD_LO1_R_N
AUD_LO2_L_P
AUD_LO2_L_N
AUD_LO2_R_P
AUD_LO2_R_N
HP AMP/LINE OUT
TWEETERS
RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT
WOOFERS
MICBIAS
VCOM
CS4206_VCOM
LINEIN_L+
LINEIN_C-
LINEIN_R+
AUD_LI_P_L
AUD_LI_COM
AUD_LI_P_R
MICIN_L+
MICIN_L-
MICIN_R+
MICIN_R-
AUD_MIC_INL_P
AUD_MIC_INL_N
AUD_MIC_INP_R
AUD_MIC_INN_R
VREF+_ADC
CS4206_VREF_ADC
DMIC_SCL
CS4206_DMIC_SCL
R6104 22
AUD_DMIC_CLK
DGND THRM PAD AGND
C6113 1UF
C6114 10UF
C6115 0.47UF
R6107 100K
R6108 100K
R6109 100K
R6110 100K
R6111 100K
Q6170 P S
Q6170 P G
Q6170 N G
Q6170 N S
Q6170
DMC2400UV
R6170 0
R6171 0
Q6171 P S
Q6171 P G
Q6171 N G
Q6171 N S
Q6171
R6172 0
R6173 0
DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS
APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC
L6111 FERR-220-OHM
PP5V_AUDIO_HPAMP
L6110 FERR-220-OHM
=PP5V_S0_AUDIO
=PP3V3_S0_AUDIO
R6120 0
VR6101
TPS71745
4V5_REG_IN
4V5_REG_EN
4V5_NR
C6122 1UF
C6123 0.1UF
C6124 1UF
XW6110
XW6111
PP4V5_AUDIO_ANALOG
GND_AUDIO_CODEC
GND_AUDIO_HPAMP
PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5
SYNC MASTER=J17 ULTIMATE
SYNC DATE=05/16/2013
PAGE TITLE
AUDIO: CODEC/REGULATORS
Apple Inc.
DRAWING NUMBER 051-9884
SIZE D
REVISION A.0.0
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PAGE 61 OF 127
SHEET 54 OF 106
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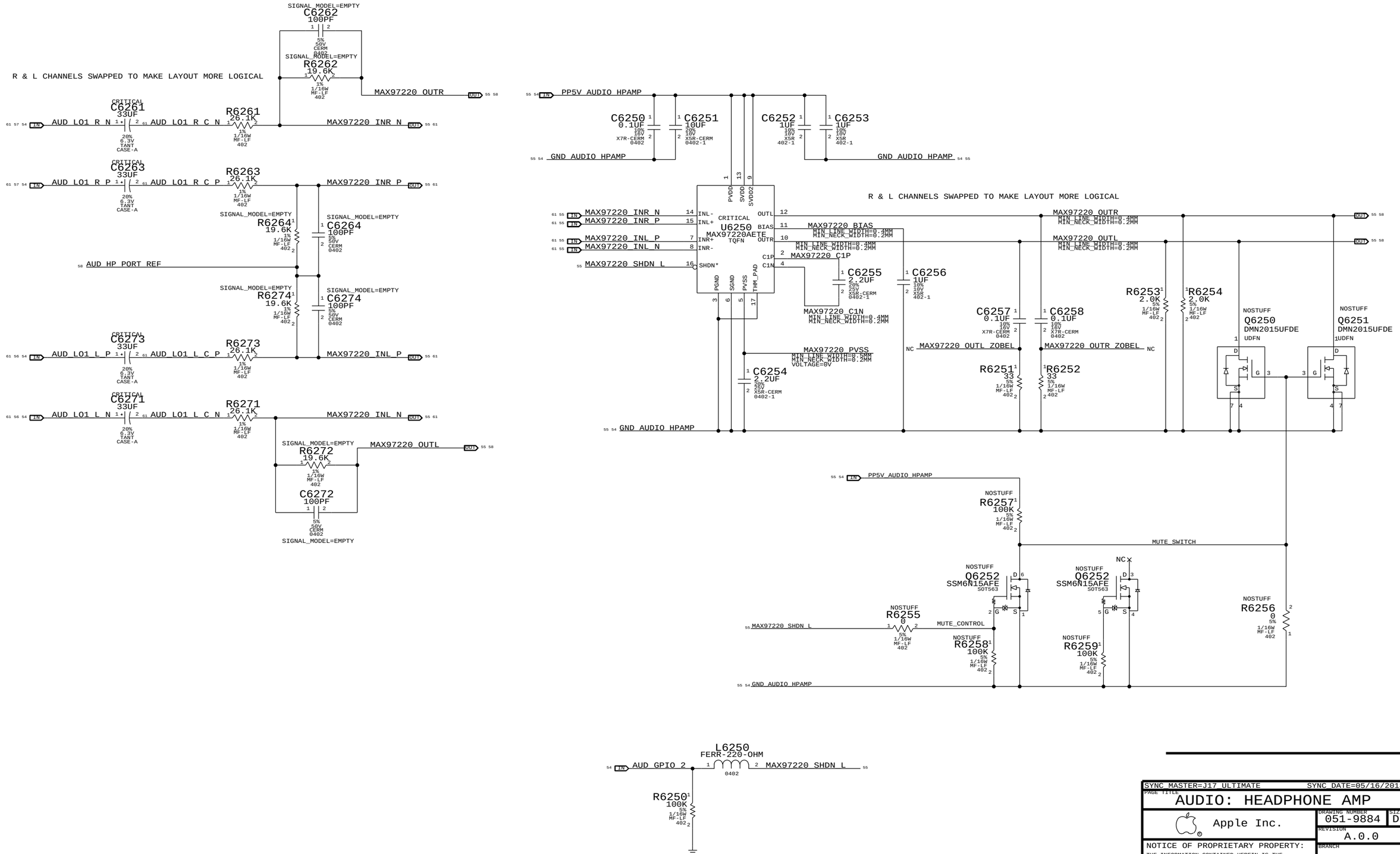

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PAGE TITLE
AUDIO: HEADPHONE AMP

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DRAWING NUMBER 051-9884 SIZE D

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PAGE 62 OF 127

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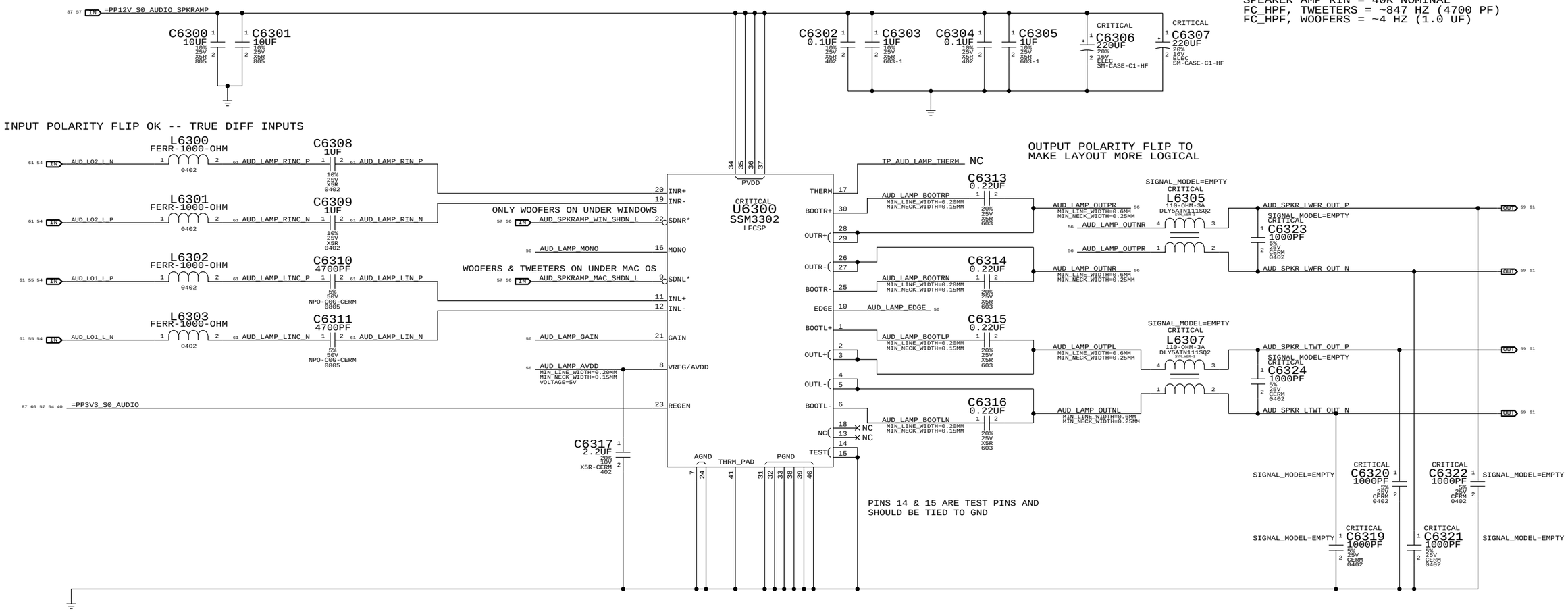
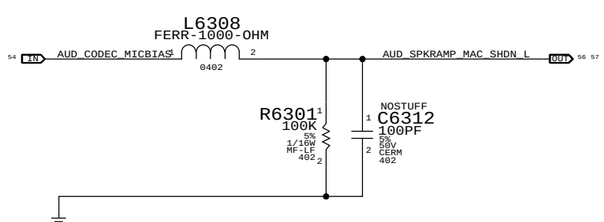
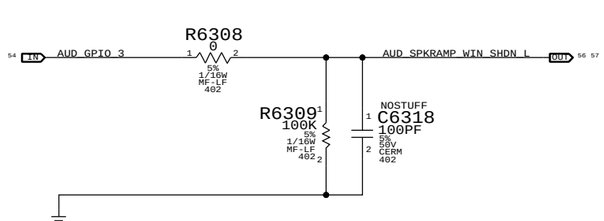
LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)





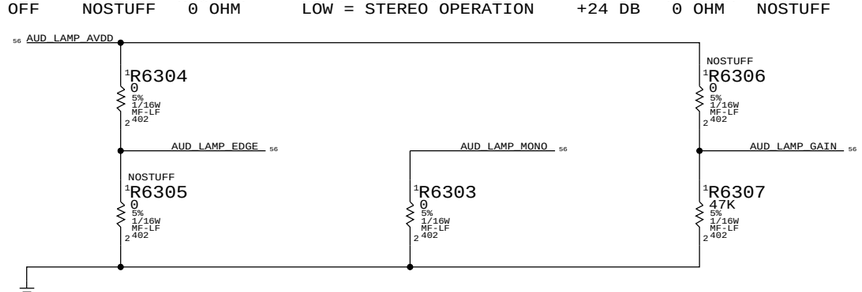


EDGE RATE CONTROL

ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: AUDIO: LEFT SPKR AMP

Apple Inc.

DRAWING NUMBER: 051-9884 SIZE: D

REVISION: A.0.0

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PAGE: 63 OF 127

SHEET: 56 OF 106

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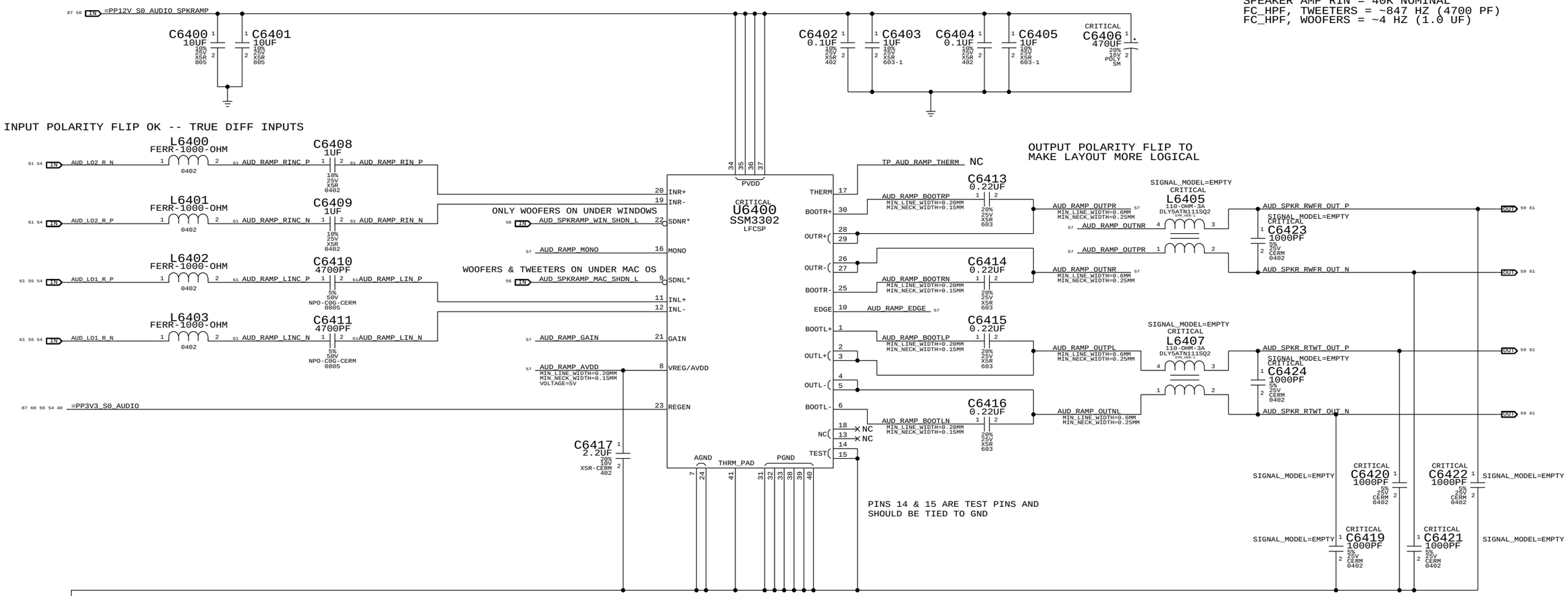
RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

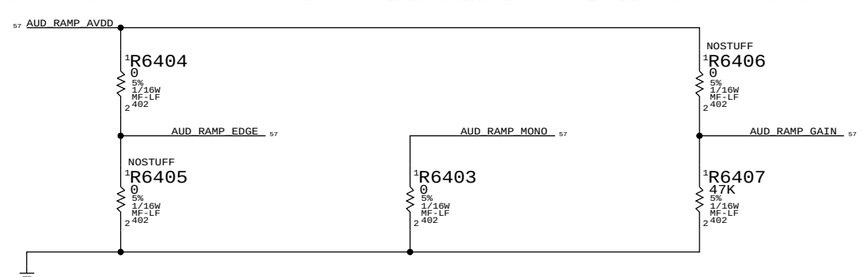
SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)



EDGE RATE CONTROL	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
AUDIO: RIGHT SPKR AMP

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DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 64 OF 127
SHEET 57 OF 106

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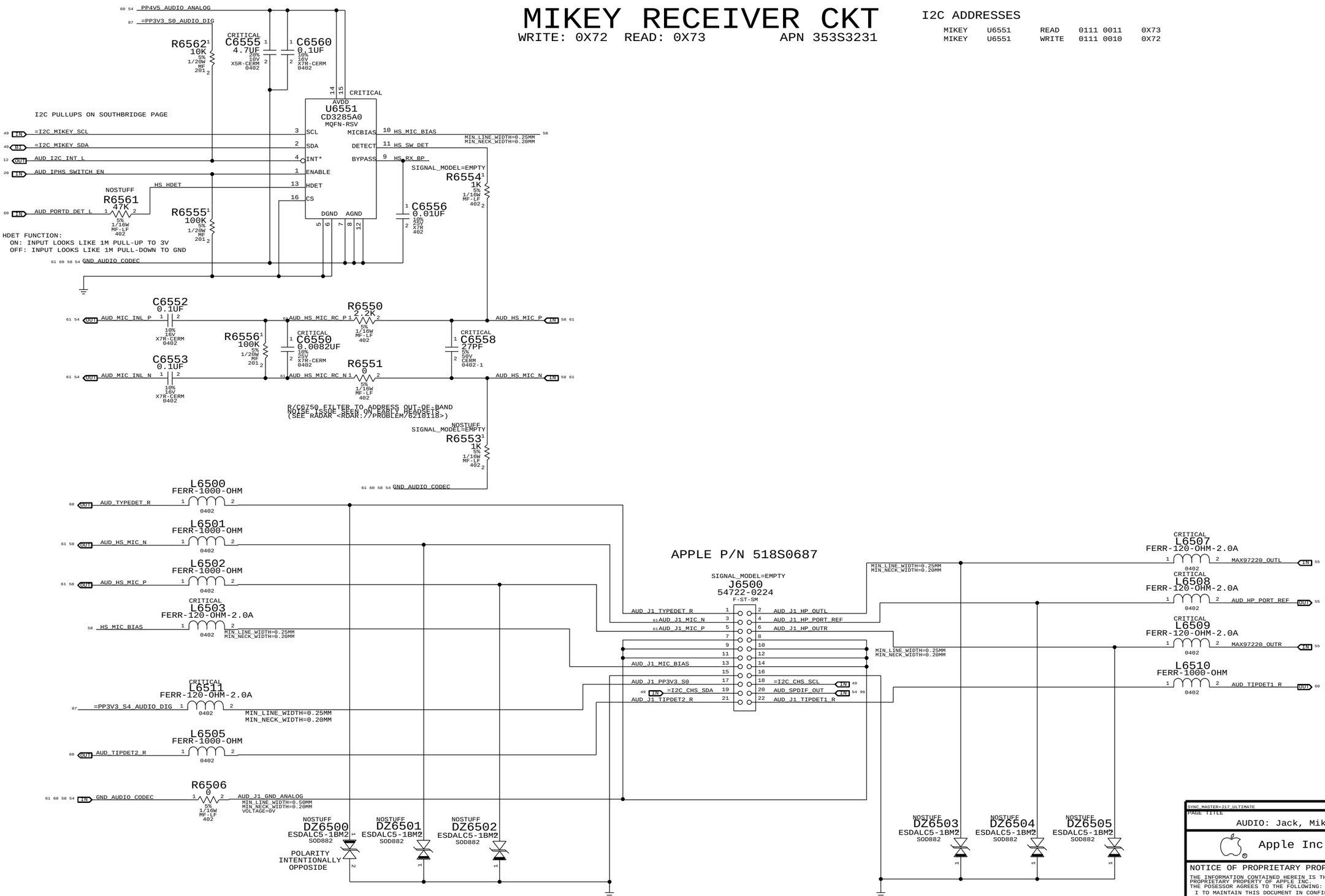
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

MIKEY	U6551	READ	0111 0011	0X73
MIKEY	U6551	WRITE	0111 0010	0X72



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

AUDIO: Jack, Mikey, CHS Switch

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DRAWING NUMBER 051-9884 SIZE D

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PAGE 65 OF 127

SHEET 58 OF 106

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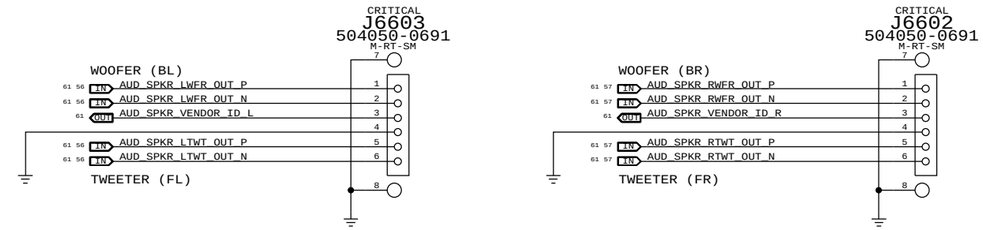
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
Audio: Spkr/Mic Conn.

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BRANCH

PAGE 66 OF 127

SHEET 59 OF 106

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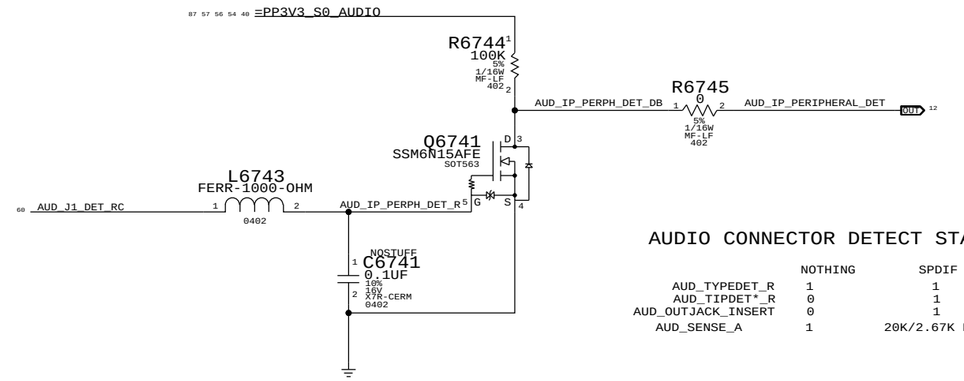
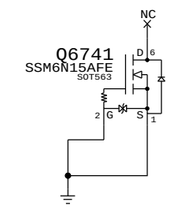
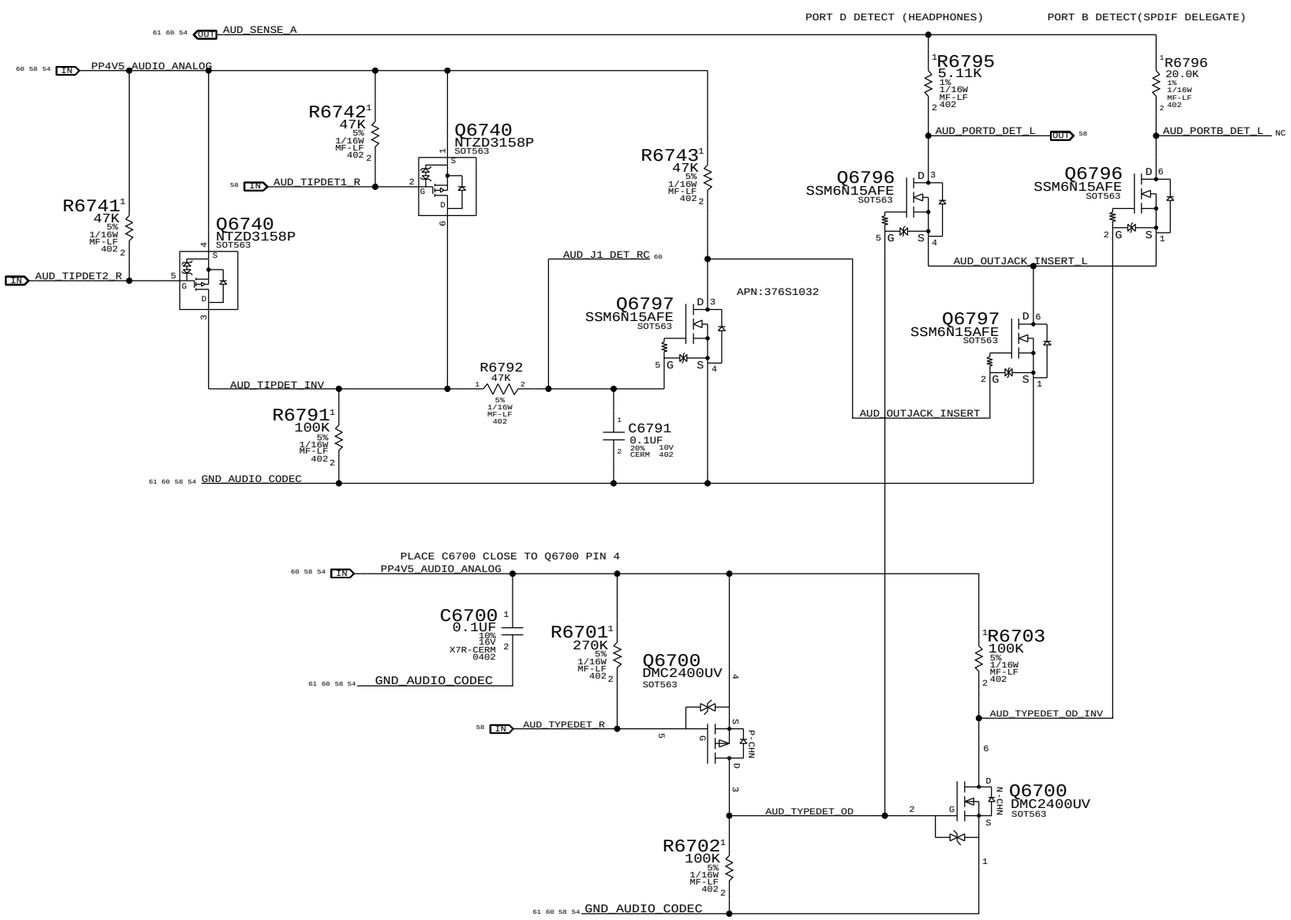
IPHS HS Detect Debounce CKT



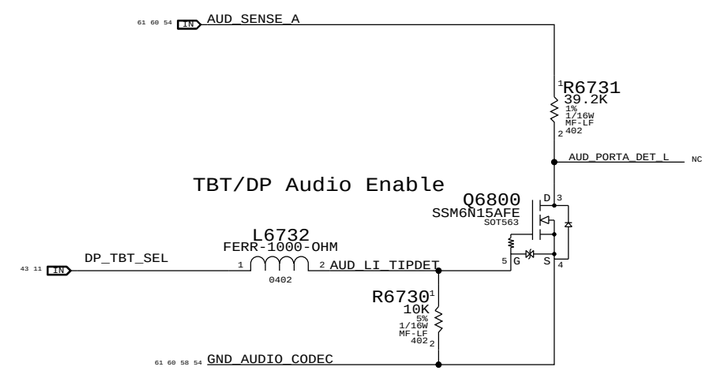
AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV





Target Display Mode Detect



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PAGE TITLE
AUDIO: Detects/Grounding

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PAGE 67 OF 127

SHEET 60 OF 106

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0x12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

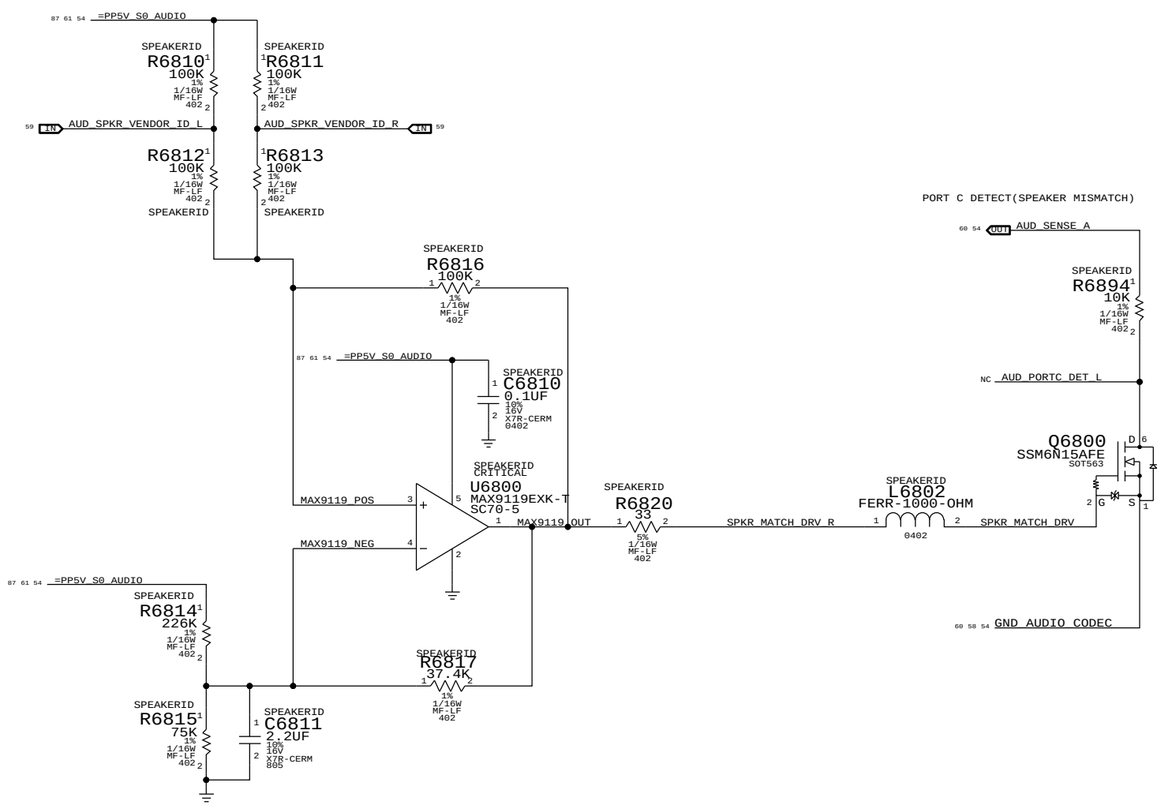
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	54 55 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	54 55 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	54 55 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	54 55 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	54 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	54 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	54 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	54 57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	55
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	55
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	57 59
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	57 59
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	57 59
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	57 59
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	56 59
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	56 59
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	56 59
SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	56 59
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	54 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	54 58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	58
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	58

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
AUDIO: Speaker ID

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REVISION A.0.0

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PAGE 68 OF 127

SHEET 61 OF 106

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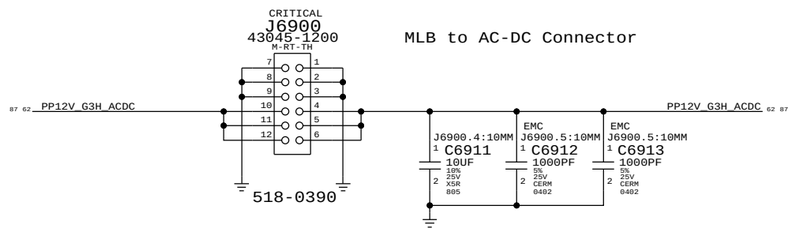
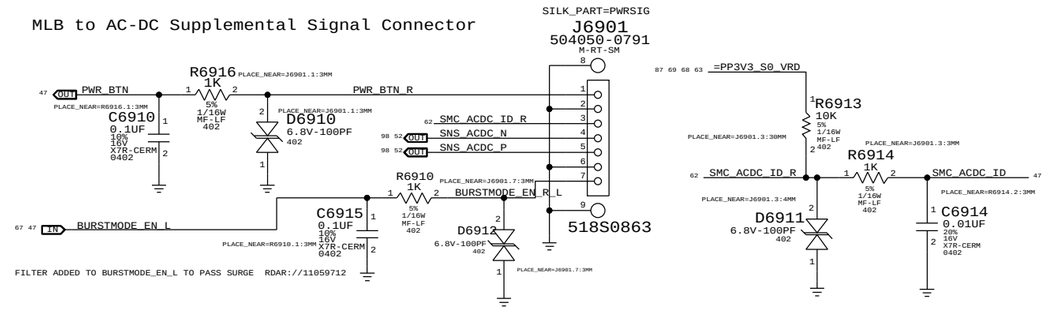
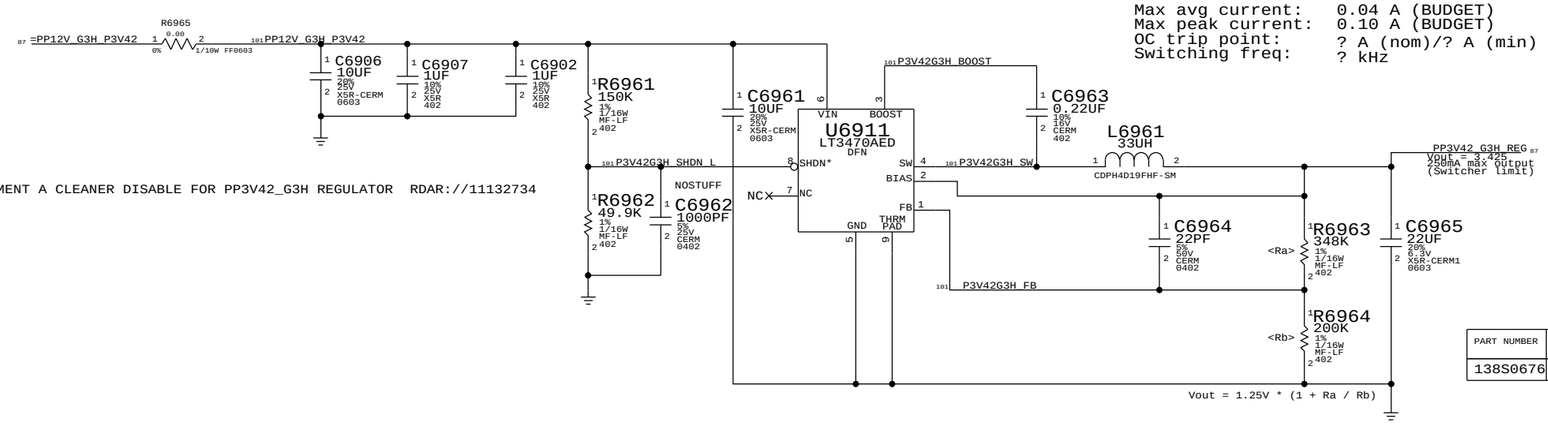




D8:CONTROLLER CHANGE FOR 3.42V SMC SUPPLY RDAR://11003901

3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42_G3H REGULATOR RDAR://11132734

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0676	138S0691		C6965	

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
Power Connectors / VReg G3Hot

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DRAWING NUMBER 051-9884 SIZE D

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PAGE 69 OF 127

SHEET 62 OF 106

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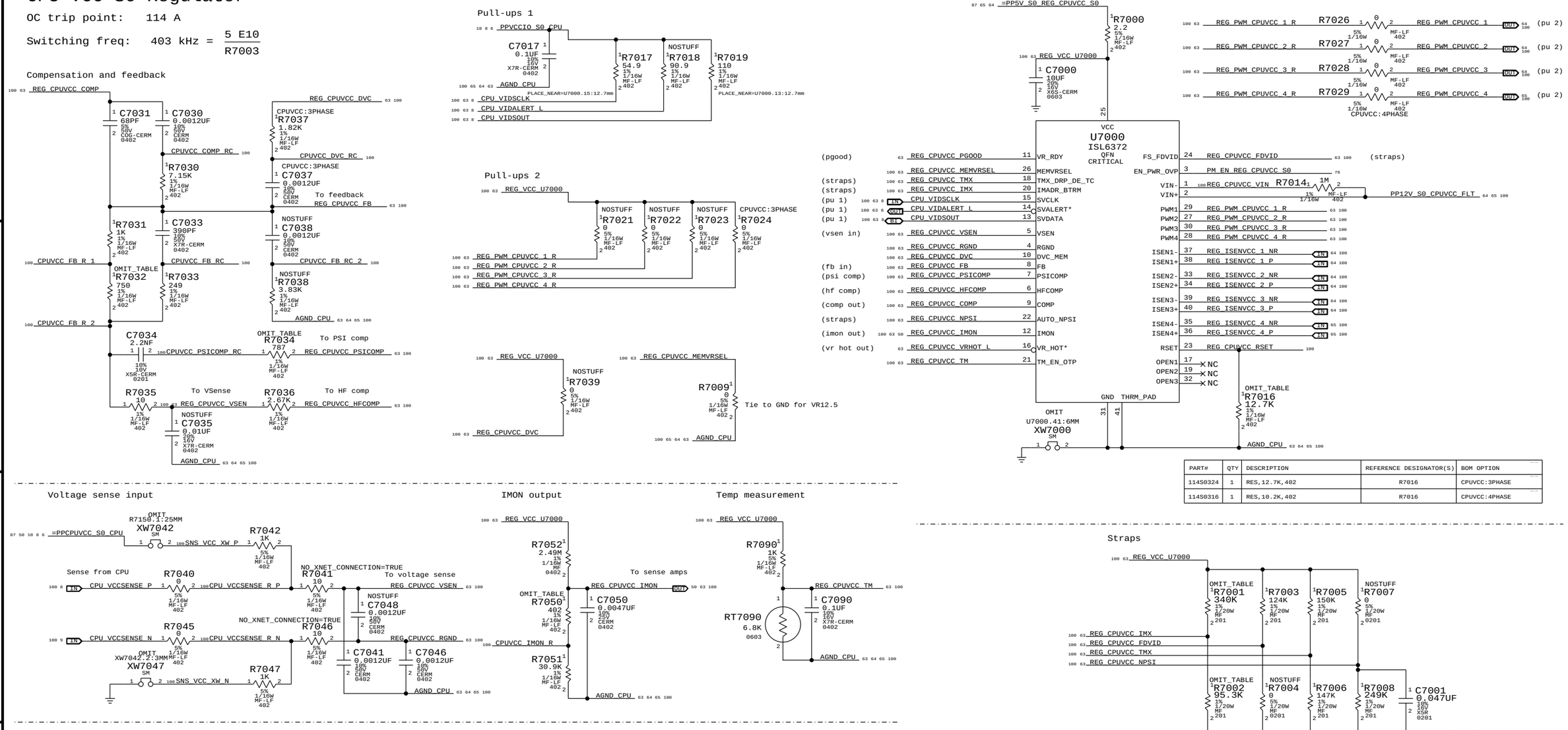
CPU VCC S0 Regulator

OC trip point: 114 A

Switching freq: 403 kHz = $\frac{5\ E10}{R7003}$



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0324	1	RES,12.7K,402	R7016	CPUVCC:3PHASE
114S0316	1	RES,10.2K,402	R7016	CPUVCC:4PHASE

J16: 3PHASE
J17: 4PHASE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0311	1	RES,340K,201	R7001	CPUVCC:3PHASE
118S0116	1	RES,158K,201	R7001	CPUVCC:4PHASE
118S0575	1	RES,95.3K,201	R7002	CPUVCC:3PHASE
118S0380	1	RES,44.2K,201	R7002	CPUVCC:4PHASE
114S0206	1	RES,750 OHM,402	R7032	CPUVCC:3PHASE
114S0210	1	RES,825 OHM,402	R7032	CPUVCC:4PHASE
114S0208	1	RES,787 OHM,402	R7034	CPUVCC:3PHASE
114S0189	1	RES,499 OHM,402	R7034	CPUVCC:4PHASE
114S0179	1	RES,402 OHM,402	R7050	CPUVCC:3PHASE
114S0184	1	RES,453 OHM,402	R7050	CPUVCC:4PHASE

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
VReg CPU VCC Cntl

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PAGE 70 OF 127

SHEET 63 OF 106

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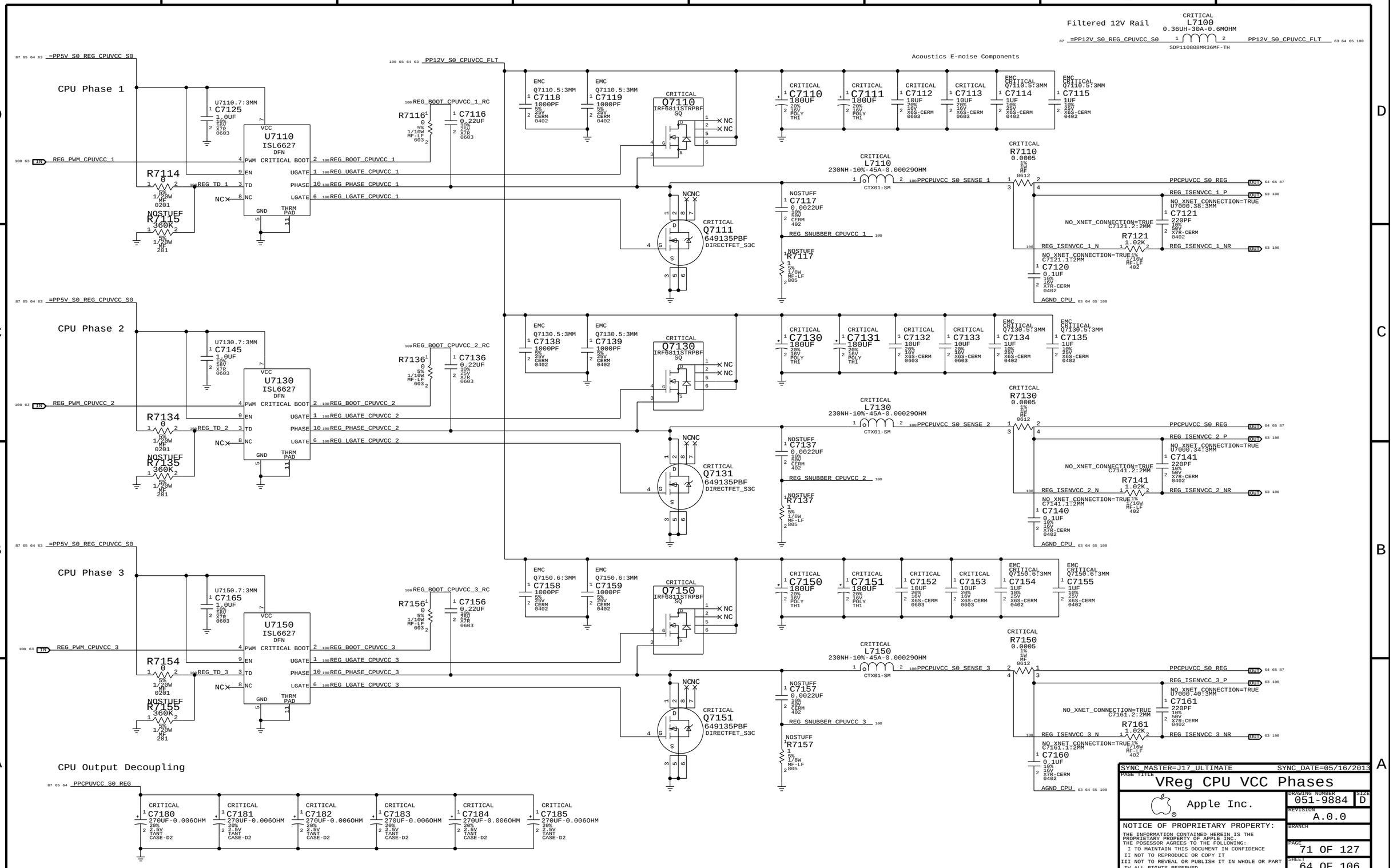

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: VReg CPU VCC Phases

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REVISION: A.0.0

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PAGE: 71 OF 127

SHEET: 64 OF 106

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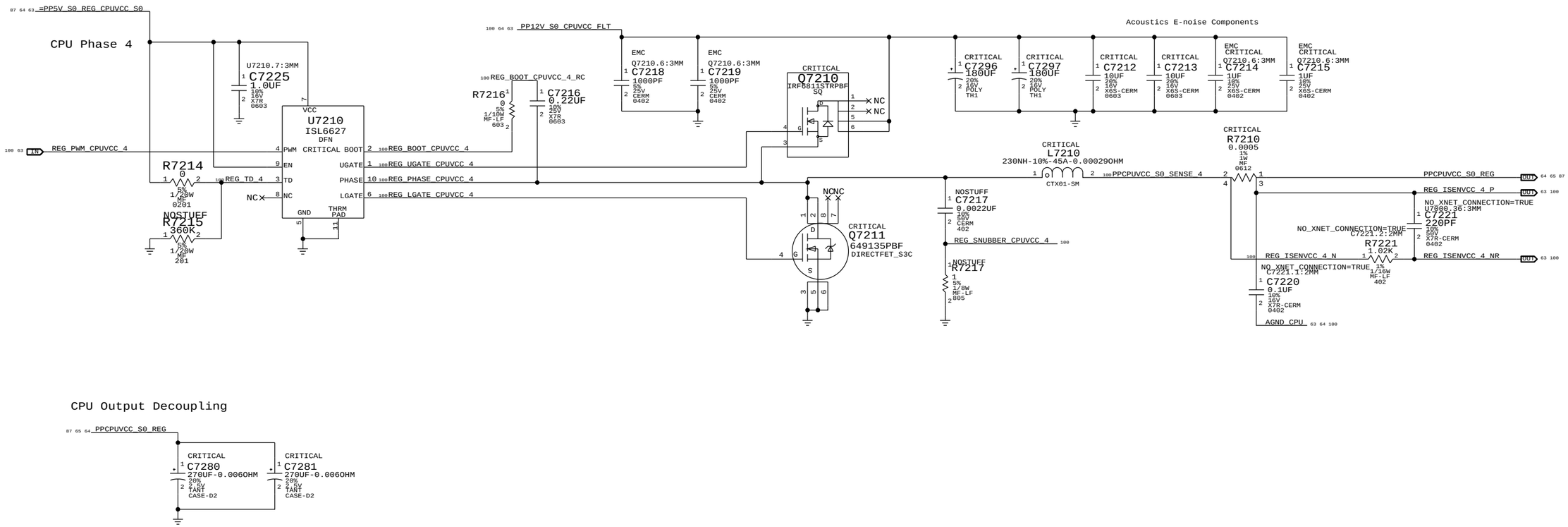

CPU Output Decoupling

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
VReg CPU VCC Phase 4

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PAGE 72 OF 127

SHEET 65 OF 106

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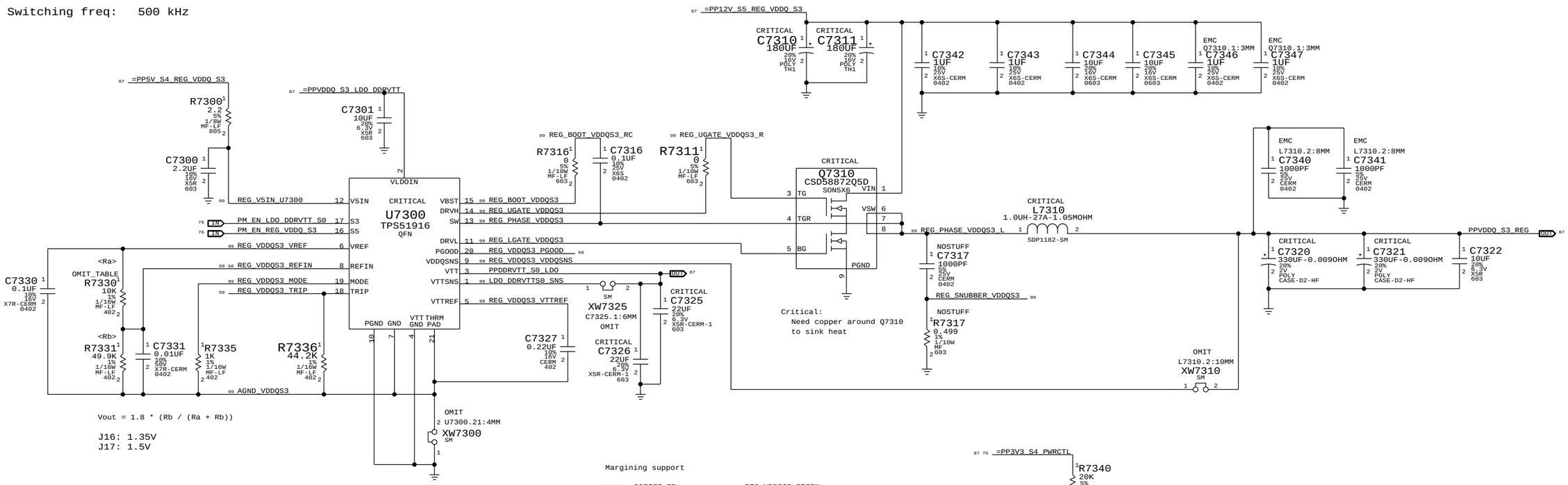
VDDQ (1.5V / 1.35V) S3 Regulator

OC trip point: 30.4 A VDDQ = $\frac{R7336}{8\ E5 * Rds(Q7310)} + \frac{0.65625}{L7310 * f(switch)}$

3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz



Vout = 1.8 * (Rb / (Ra + Rb))

J16: 1.35V
J17: 1.5V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0335	1	RES,16.5K,402	R7330	VDDQ:P1V35
114S0315	1	RES,10K,402	R7330	VDDQ:P1V5

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
VReg VDDQ S3

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PAGE 73 OF 127

SHEET 66 OF 106

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3.3V S5 Regulator

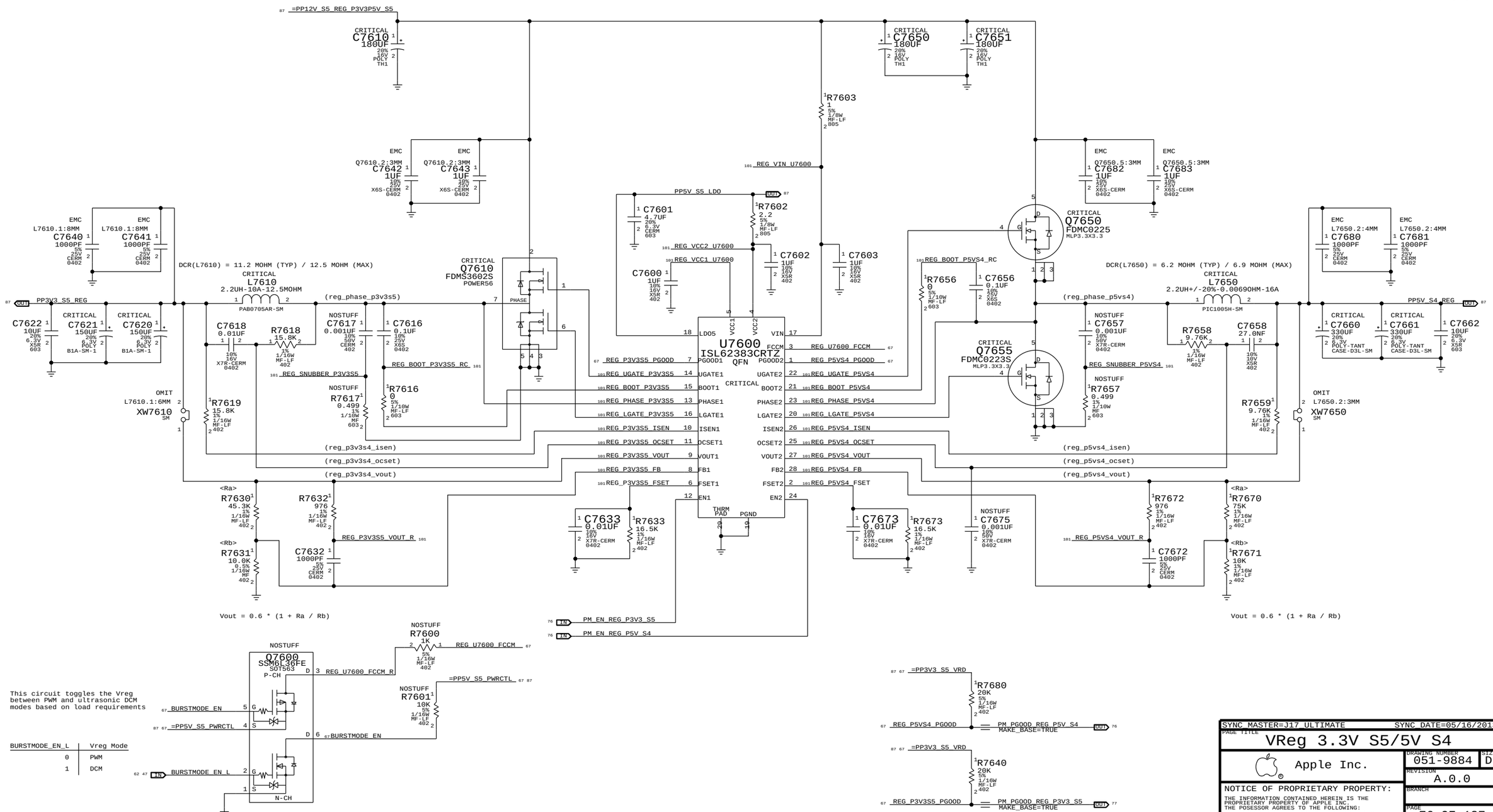
OC trip point: 12.5 A = R7618 * 10 E-6 / DCR(L7610)

Switching freq: 356 kHz = 1 / (170 E-12 * R7633)

5V S4 Regulator

OC trip point: 14.1 A = R7658 * 10 E-6 / DCR(L7650)

Switching freq: 356 kHz = 1 / (170 E-12 * R7673)



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE: VReg 3.3V S5/5V S4

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PAGE: 76 OF 127

SHEET: 67 OF 106

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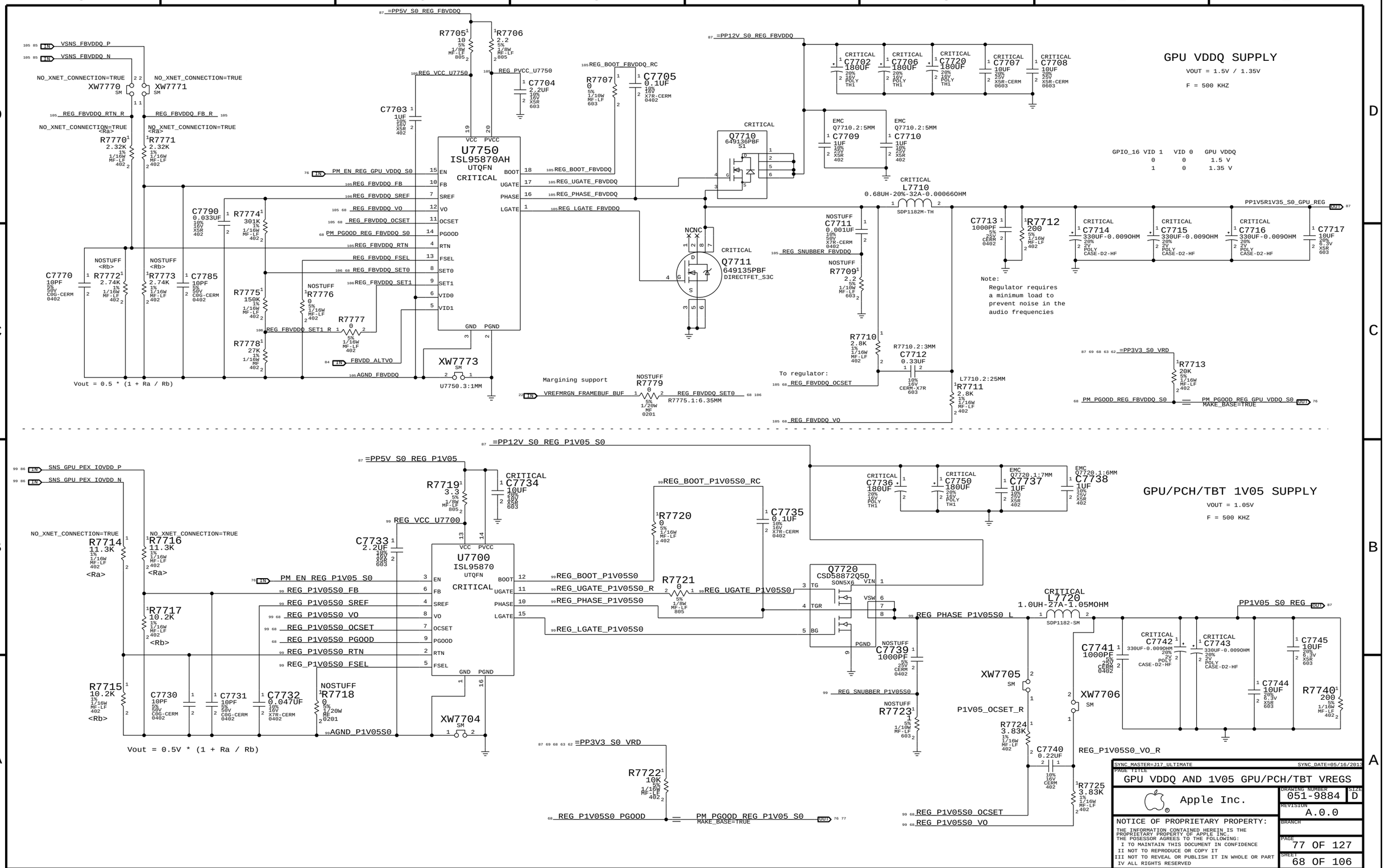
GPU VDDQ SUPPLY
VOUT = 1.5V / 1.35V
F = 500 KHZ
GPIO_16 VID 1 VID 0 GPU VDDQ
0 0 1.5 V
1 0 1.35 V
U7750
ISL95870AH
UTQFN
CRITICAL
Q7710
649136PBF
Q7711
649135PBF
DIRECTFET_S3C
L7710
0.68UH-20%-32A-0.000660HM
SDP1182M-TH
PP1V5R1V35_S0_GPU_REG
Note:
Regulator requires
a minimum load to
prevent noise in the
audio frequencies
Vout = 0.5 * (1 + Ra / Rb)
GPU/PCH/TBT 1V05 SUPPLY
VOUT = 1.05V
F = 500 KHZ
U7700
ISL95870
UTQFN
CRITICAL
Q7720
CSD58872Q5D
L7720
1.0UH-27A-1.05MOHM
SDP1182-SM
PP1V05_S0_REG
Vout = 0.5V * (1 + Ra / Rb)
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GPU VDDQ AND 1V05 GPU/PCH/TBT VREGS
051-9884
D
A.0.0
77 OF 127
68 OF 106
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GPU CORE REG 1.1V/???A O/P= PPGPUCORE_S0_REG

GPU VCORE
VOUT = VCORE
PEAK = ???A
AVG = ???A

=PP5V_S0_VRD — R7818 2.2 5% 1/8W MF-LF 805 (MAX NECK LENGTH=3MM, MIN NECK WIDTH=0.2MM, MIN LINE WIDTH=0.6MM, VOLTAGE=5V)

PP5V_S0_GPU_VCORE_VCC — R7847, R7848, R7844, R7855 (NOSTUFF) 0 5% 1/16W MF-LF 402

VR_GPU_PWM1_R, VR_GPU_PWM2_R, VR_GPU_PWM3_R, VR_GPU_PWM4_R

VSNS_GPU_VDD — XW7820 (SM, OMIT) — VR_GPU_VSEN (VOLTAGE=1.1V, NET_PHYSICAL_TYPE=SNS_DIFF_PWR, SIGNAL_MODEL=EMPTY)

VSNS_GPU_VSS — XW7830 (SM, OMIT) — VR_GPU_RGND (VOLTAGE=0V, NET_PHYSICAL_TYPE=SNS_DIFF_PWR)

1.25 mOhm loadline

C7801 0.0022UF 10% 50V CERM 402 (NOSTUFF)

C7802 0.0022UF 10% 50V CERM 402 — C7803 0.0022UF 10% 50V CERM 402 — AGND_GPU

C7804 47PF 5% 50V CERM 402 (VR_GPU_FB_R, VR_GPU_COMP_R)

R7801 8.06K 1% 1/16W MF-LF 402 — VR_GPU_COMP_RC — C7805 0.0047UF 10% 25V CERM 0402

R7879 0 5% 1/16W MF-LF 402

R7802 1K 1% 1/16W MF-LF 402 — VR_VDF_R1 — R7803 287 1% 1/16W MF-LF 402

C7806 0.001UF 10% 50V X7R-CERM 0402 — VR_VDF_R2 — R7849 47.5 1% 1/16W MF-LF 402

R7846 1M 5% 1/16W MF-LF 402 (NOSTUFF) — R7804 0 5% 1/16W MF-LF 402

LOCAL 5V — C7807 1UF 10% 10V X6S-CERM 0402 — AGND_GPU

PP5V_S0_GPU_VCORE_VCC

R7800 1.02K 1% 1/16W MF-LF 402 — R7805 20.0K 1% 1/16W MF-LF 402 (NOSTUFF) — R7898 0 5% 1/16W MF-LF 402 (NOSTUFF) — R7877 100K 1% 1/16W MF-LF 402

VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.

LAYOUT: PLACE RT7801 NEAR HOT SPOT

RT7801 6.8K 0603 — C7880 0.1UF 10% 10V CERM 402

R7806 0 5% 1/16W MF-LF 402 — R7807 21K 1% 1/16W MF-LF 402 (NOSTUFF) — R7808 75K 1% 1/16W MF-LF 402 — R7809 100K 1% 1/16W MF-LF 402 (NOSTUFF)

C7810 0.0033UF 10% 50V X7R-CERM 0402 — R7810 2.15K 1% 1/16W MF-LF 402 — AGND_GPU

=PP5V_S0_VRD — R7811 10K 0.1% 1/16W MF-LF 0402

PP5V_S0_GPU_VCORE_VCC

=PP3V3_S0_VRD

=PP3V3_S0_GPU — R7812 2.0K 5% 1/16W MF-LF 402

R7899 10K 0.1% 1/16W MF-LF 0402

PM_PGOOD_REG_GPUCORE_S0

GPU_PSI_L

VR_GPU_IMON

R7814 49.9K 1% 1/16W MF-LF 402 — R7815 49.9K 1% 1/16W MF-LF 402

R7845 0 5% 1/16W MF-LF 402

R7817 10K 1% 1/16W MF-LF 402 — C7812 0.022UF 10% 16V X5R-X7R-CERM 0402 — R7816 0 5% 1/16W MF-LF 402 (VR_GPU_IOUT_PD)

DEFAULT: 0.9000V STEP: 12.5MV

=PP3V3_S0_GPU — R7878, R7870, R7871, R7872, R7873, R7874, R7875, R7876 1K 1% 1/16W MF-LF 402 (NOSTUFF)

REG_GPUCORE_VID7, REG_GPUCORE_VID6, REG_GPUCORE_VID5, REG_GPUCORE_VID4, REG_GPUCORE_VID3, REG_GPUCORE_VID2, REG_GPUCORE_VID1, REG_GPUCORE_VID0

R7895, R7896, R7897, R7880, R7881, R7882, R7885, R7883 1K 1% 1/16W MF-LF 402 (NOSTUFF)

U7800 ISL6334D QFN — VCC CRITICAL SYM_VER_2

Pin	Signal
13	COMP
14	FB
15	VDIFF
17	VSEN
16	RGND
18	TCOMP
9	OFS
34	FS
35	SS
11	DAC
12	REF
39	TM
33	EN_VTT
36	VR_RDY
7	VID0
6	VID1
5	VID2
4	VID3
3	VID4
2	VID5
1	VID6
40	VID7
8	PSI*
10	IMON
37	VR_FAN
38	VR_HOT
32	EN_PWR
26	PWM1
28	ISEN1+
27	ISEN1-
20	PWM2
22	ISEN2+
21	ISEN2-
31	PWM3
29	ISEN3+
30	ISEN3-
25	PWM4
23	ISEN4+
24	ISEN4-
19	THRM PAD

VR_GPU_VDIFF, VR_GPU_TCOMP, VR_GPU_OFS, VR_GPU_FS, VR_GPU_SS, VR_GPU_DAC, VR_GPU_REF, VR_GPU_TM, VR_GPU_EN_VTT, VR_GPU_IMON_R, VR_GPU_FAN, VR_GPU_VRDHOT

XW7801 (SM, OMIT) — AGND_GPU (MAX NECK LENGTH=5MM, MIN NECK WIDTH=0.3MM, MIN LINE WIDTH=0.6MM, VOLTAGE=0V)

R7884 0 5% 1/16W MF-LF 402 — PM_EN_REG_GPUCORE_S0 — PM_EN_REG_GPUCORE_S0_R — C7809 0.01UF 10% 16V X7R-CERM 0402 (NOSTUFF)

R7834 0 5% 1/16W MF-LF 402 — REG_PWM_GPUCORE_1

R7831 178 1% 1/16W MF-LF 402 — VR_GPU_ISNS1_RR_2 — R7832 0 5% 1/16W MF-LF 402

C7830 15PF 1% 50V C0G 402 (NOSTUFF) — C7831 150PF 5% 50V CERM 402 — C7832 0.1UF 10% 16V X7R-CERM 0402 — C7833 220PF 5% 25V C0G-CERM 0402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_1
REG_ISEN_GCORE_1_P, REG_ISEN_GCORE_1_N

R7833 1.02K 1% 1/16W MF-LF 402

R7840 0 5% 1/16W MF-LF 402 — REG_PWM_GPUCORE_2

R7841 178 1% 1/16W MF-LF 402 — VR_GPU_ISNS2_RR_2 — R7842 0 5% 1/16W MF-LF 402

C7840 15PF 1% 50V C0G 402 (NOSTUFF) — C7841 150PF 5% 50V CERM 402 — C7842 0.1UF 10% 16V X7R-CERM 0402 — C7843 220PF 5% 25V C0G-CERM 0402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_2
REG_ISEN_GCORE_2_P, REG_ISEN_GCORE_2_N

R7843 1.02K 1% 1/16W MF-LF 402

R7850 0 5% 1/16W MF-LF 402 — REG_PWM_GPUCORE_3

R7851 178 1% 1/16W MF-LF 402 — VR_GPU_ISNS3_RR_2 — R7852 0 5% 1/16W MF-LF 402

C7850 15PF 1% 50V C0G 402 (NOSTUFF) — C7851 150PF 5% 50V CERM 402 — C7852 0.1UF 10% 16V X7R-CERM 0402 — C7853 220PF 5% 25V C0G-CERM 0402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_3
REG_ISEN_GCORE_3_P, REG_ISEN_GCORE_3_N

R7853 1.02K 1% 1/16W MF-LF 402

R7838 0 5% 1/16W MF-LF 402 — REG_PWM_GPUCORE_4

R7839 178 1% 1/16W MF-LF 402 — VR_GPU_ISNS4_RR_2 — R7820 0 5% 1/16W MF-LF 402

C7860 15PF 1% 50V C0G 402 (NOSTUFF) — C7861 150PF 5% 50V CERM 402 — C7862 0.1UF 10% 16V X7R-CERM 0402 — C7863 220PF 5% 25V C0G-CERM 0402

DIFFERENTIAL_PAIR=REG_ISEN_GCORE_4
REG_ISEN_GCORE_4_P, REG_ISEN_GCORE_4_N

R7821 1.02K 1% 1/16W MF-LF 402

AGND_GPU

NEED TO FIGURE OUT SEQUENCING FOR ENABLE

=PP12V_S0_REG_GPUCORE — IMAX = 10.5A — L7800 (CRITICAL) 0.36UH-30A-0.6MOHM SDP110808MR36MF-TH 152-0110 — PP12V_S0_GPUCORE_FLT

GPU CORE INPUT Filtering

SYNC MASTER=J17_ULTIMATE	SYNC DATE=05/16/2013
PAGE TITLE	VReg GPU Core Phases
Apple Inc.	DRAWING NUMBER 051-9884 — SIZE D
	REVISION A.0.0
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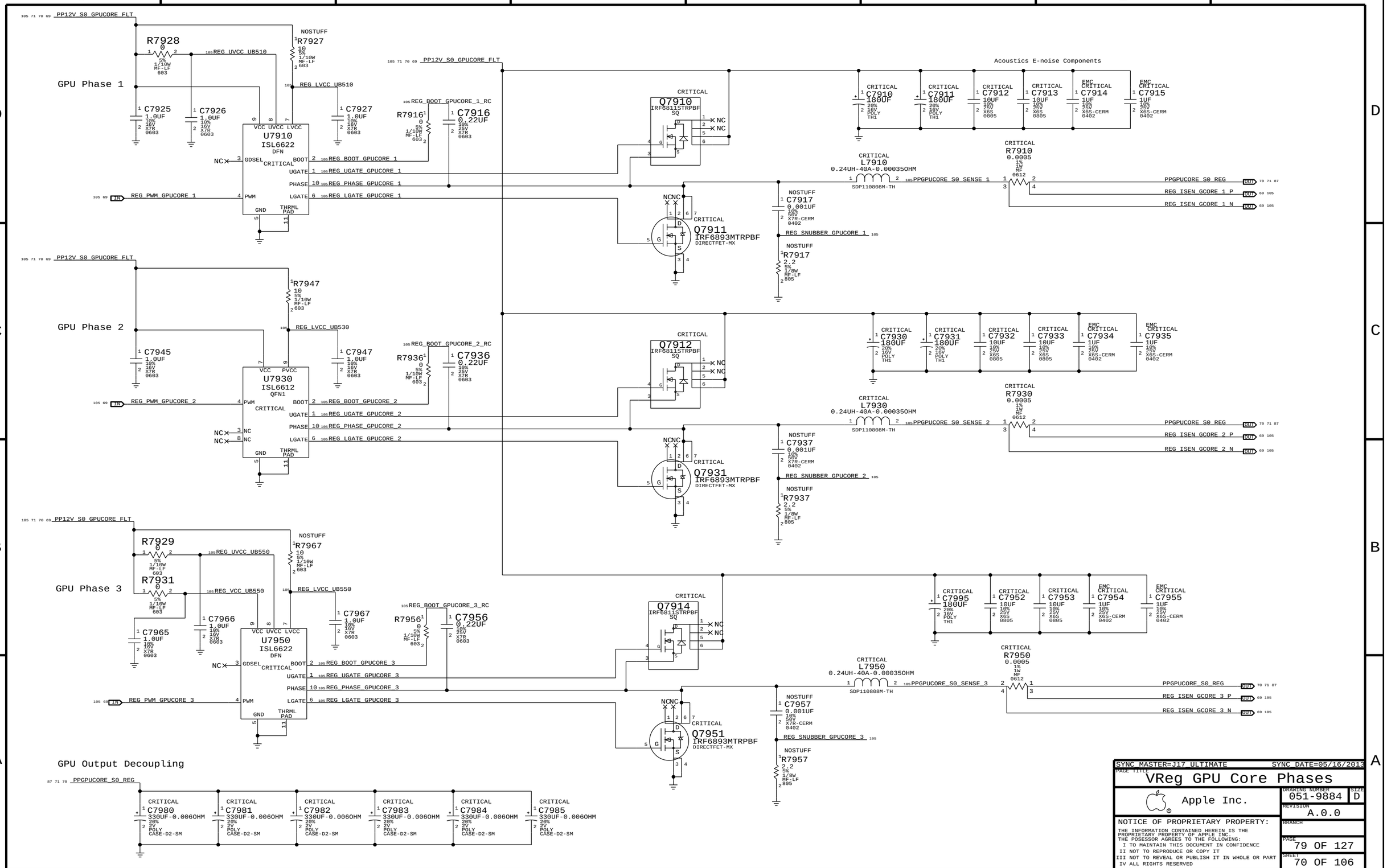
	PAGE 78 OF 127
	SHEET 69 OF 106



SYNC MASTER=J17 ULTIMATE SYNC DATE=05/16/2013

PAGE TITLE: VReg GPU Core Phases

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DRAWING NUMBER: 051-9884 SIZE: D

REVISION: A.0.0

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PAGE: 79 OF 127

SHEET: 70 OF 106

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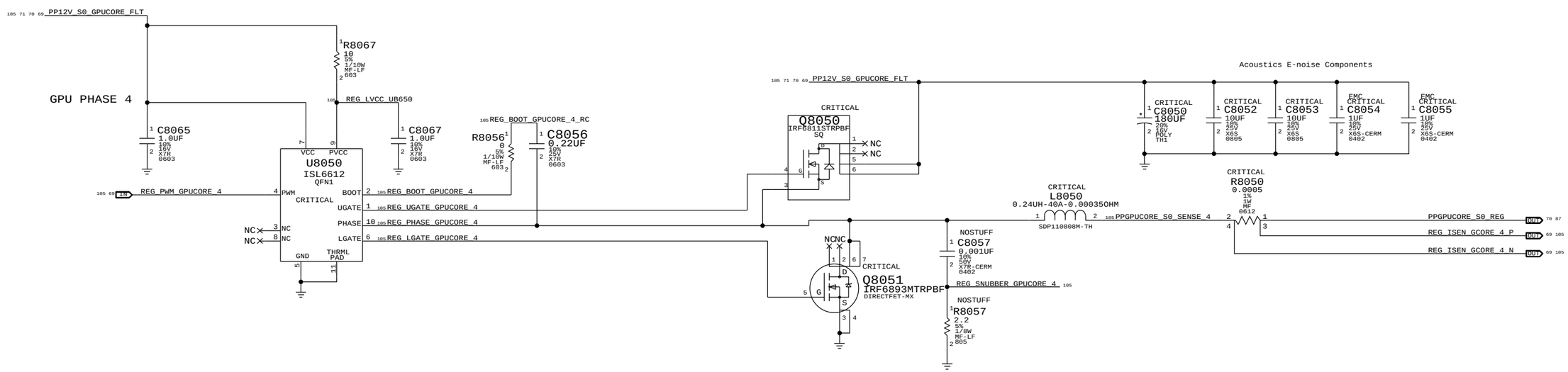

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PAGE TITLE

VREG GPU CORE PHASE 4

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PAGE 80 OF 127

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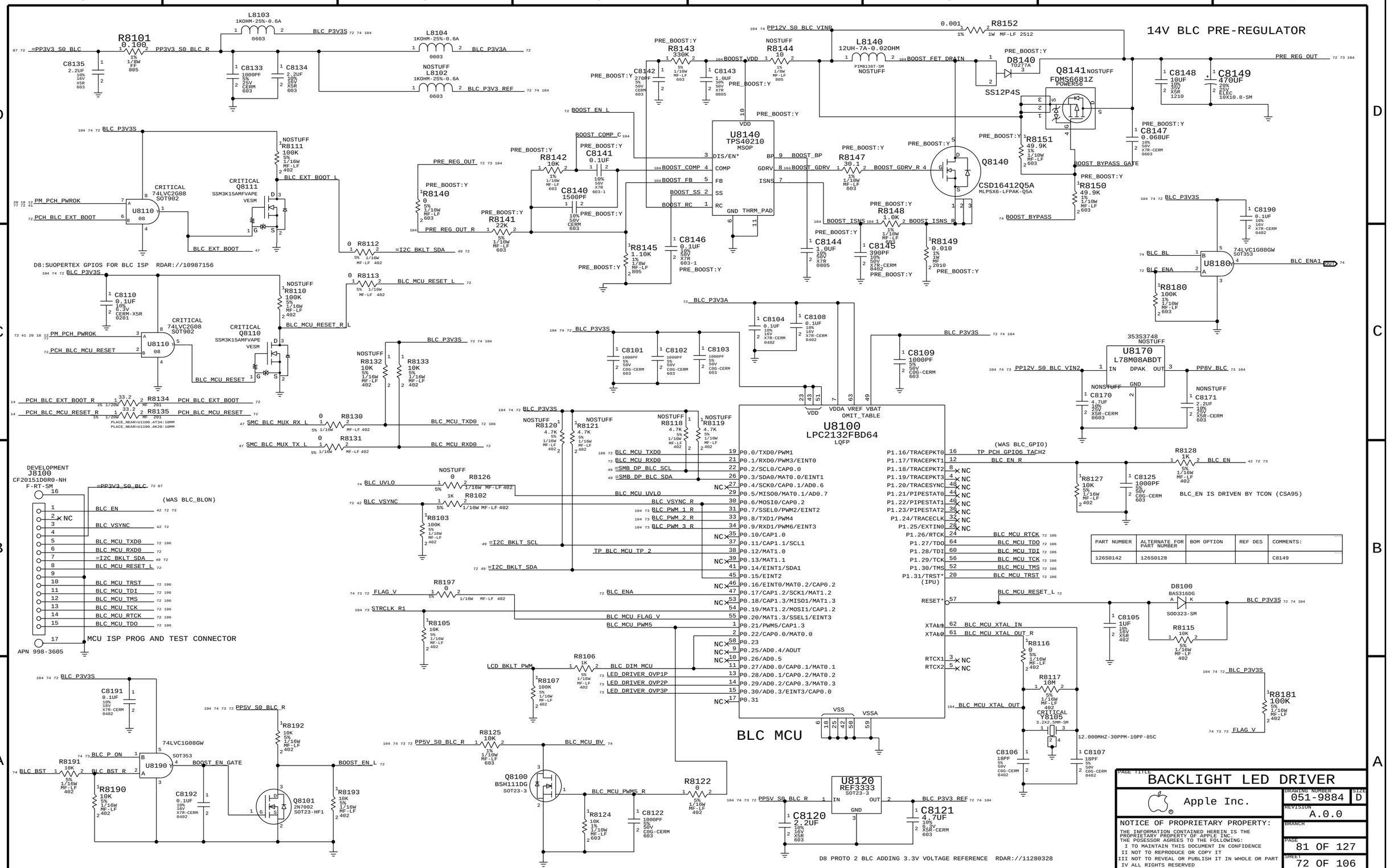

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0142	126S0128			C8149

PAGE TITLE
BACKLIGHT LED DRIVER

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DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 81 OF 127
SHEET 72 OF 106

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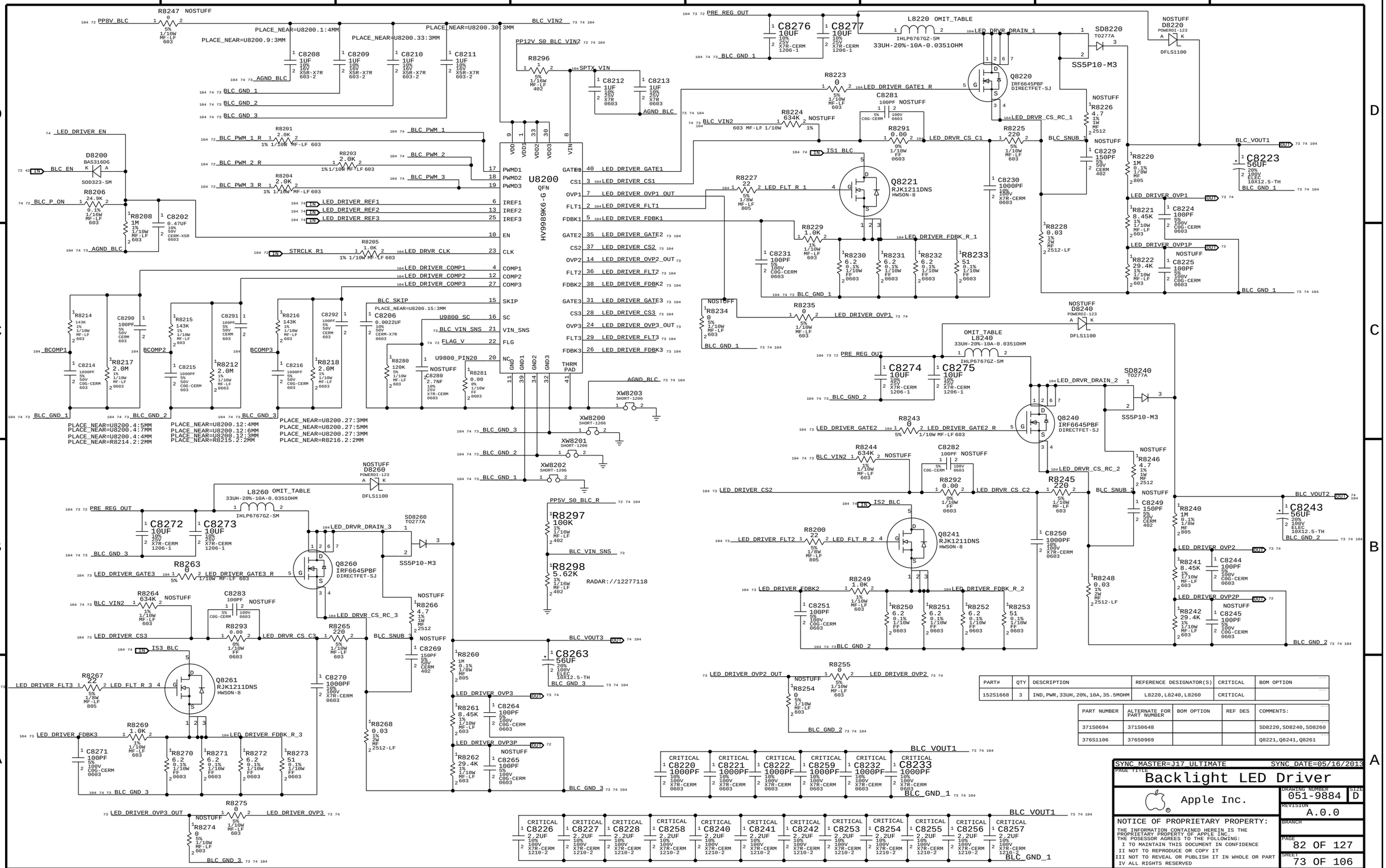

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	3	IND,PWR,33UH,20%,10A,35.5MOHM	L8220,L8240,L8260	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0694	371S0648			SD8220,SD8240,SD8260
376S1106	376S0969			Q8221,Q8241,Q8261

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PAGE TITLE
Backlight LED Driver

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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PAGE 82 OF 127

SHEET 73 OF 106

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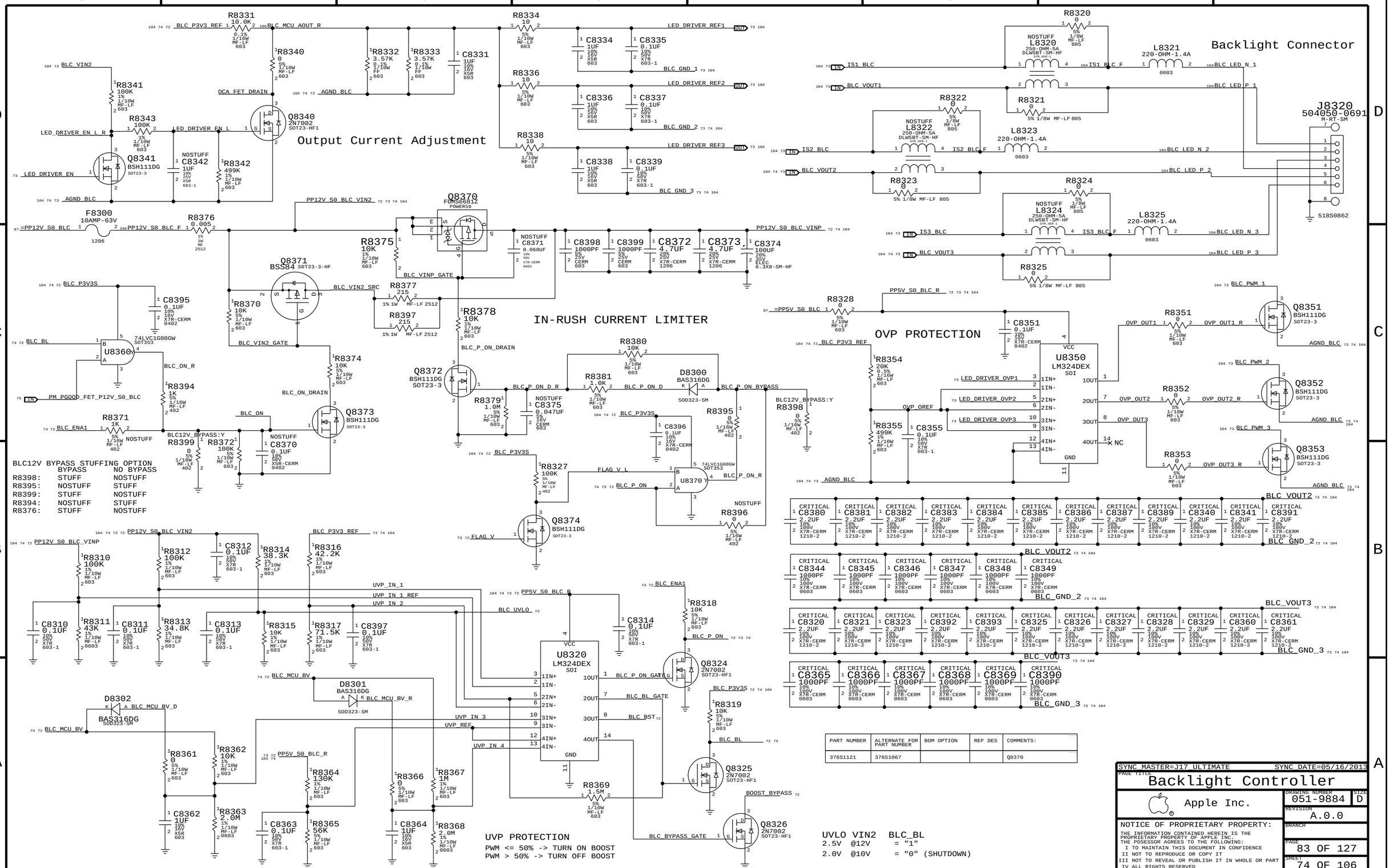
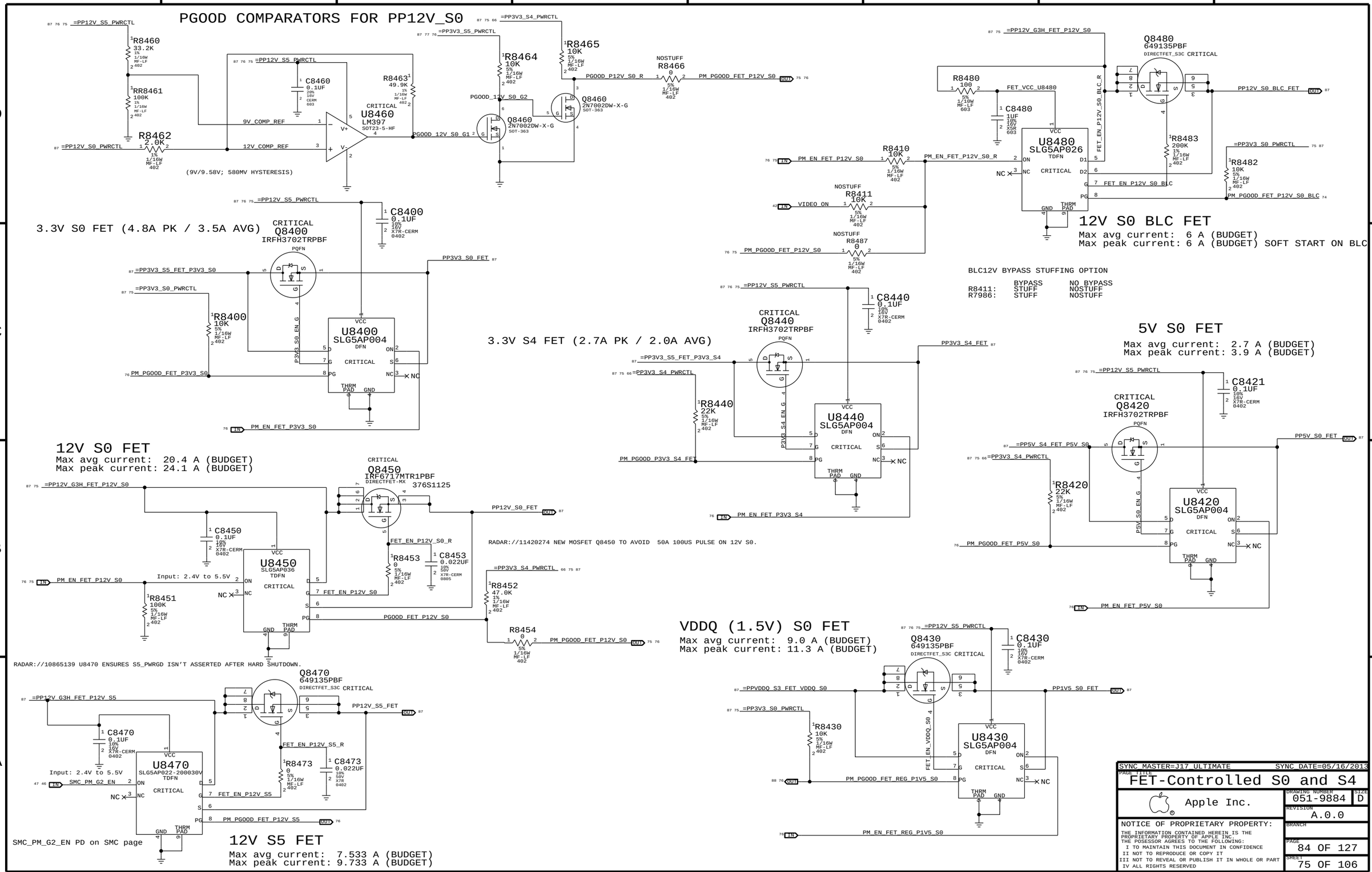


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1067			Q8370

PGOOD COMPARATORS FOR PP12V_S0



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE: FET-Controlled S0 and S4

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DRAWING NUMBER: 051-9884 SIZE: D

REVISION: A.0.0

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PAGE: 84 OF 127

SHEET: 75 OF 106

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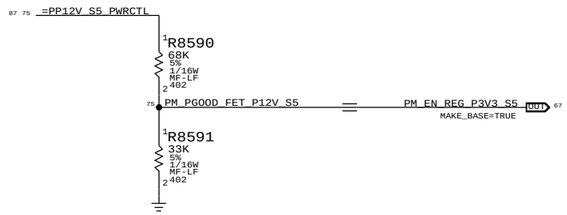
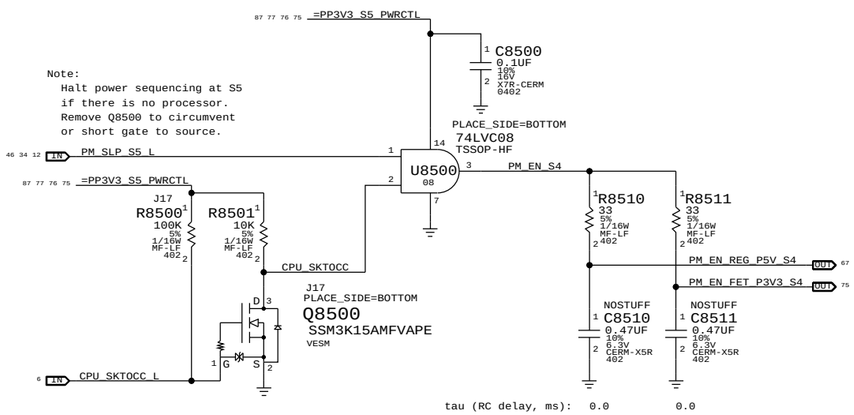
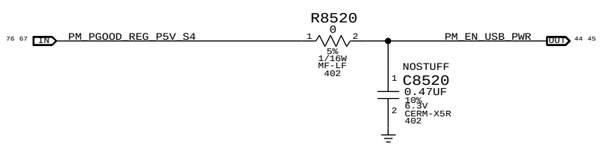
S5 Enable



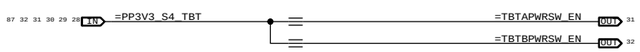
S4 Enables



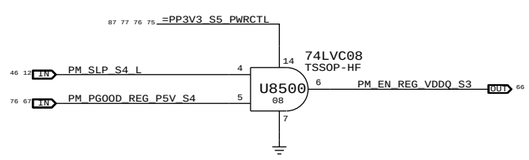
S4 USB Enable



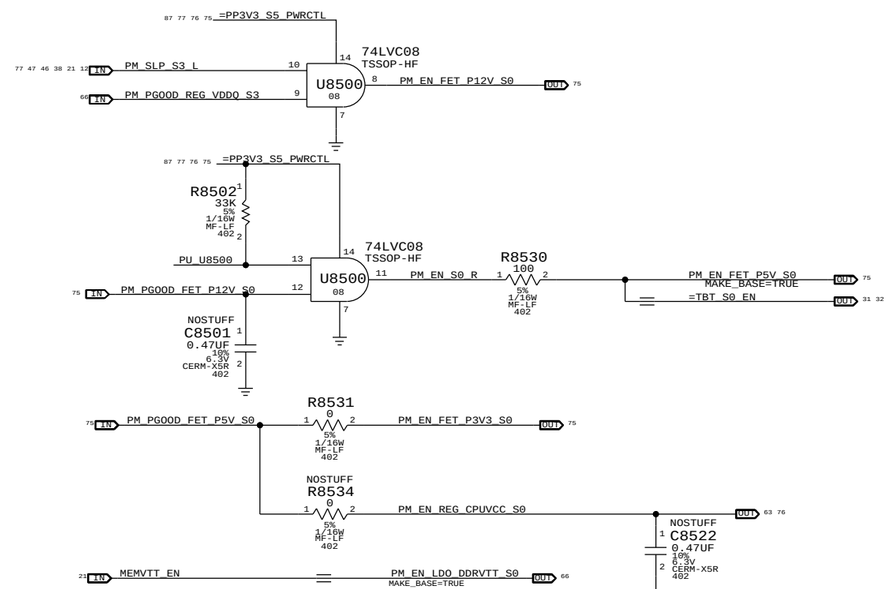
S4 TBT S4 Port Enable



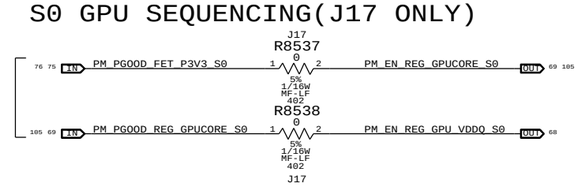
S3 VDDQ Enable



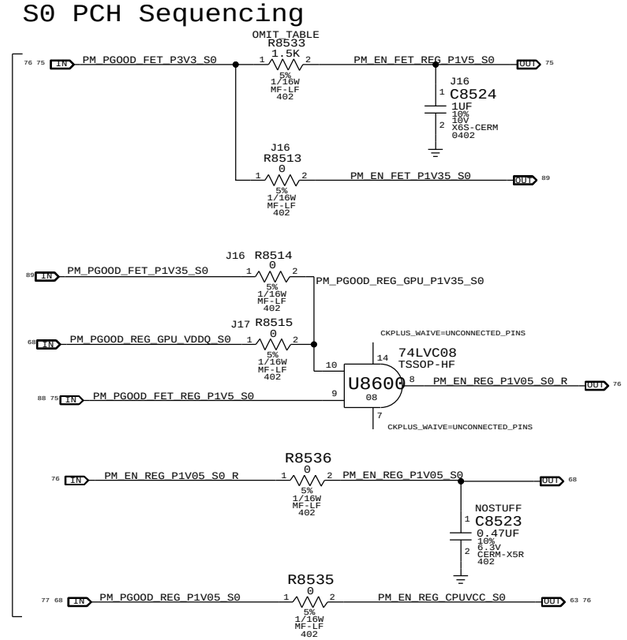
S0 Enables



S0 GPU SEQUENCING(J17 ONLY)



S0 PCH Sequencing



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0070	1	RES,1.5K,0402,5%	R8533	J16
116S0004	1	RES,0OHM,0402,5%	R8533	J17

Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.5 V, 1.05V for PCH/TBT/GPU)
Uncore: VDDQ

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

NVIDIA:
1. 3V3_S0 must ramp first
4. VDDQ MUST RAMP AFTER GPU_CORE
5. PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ
6. All rails must reach their target voltages in more than 40 uS

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PAGE TITLE
PM Regulator Enables

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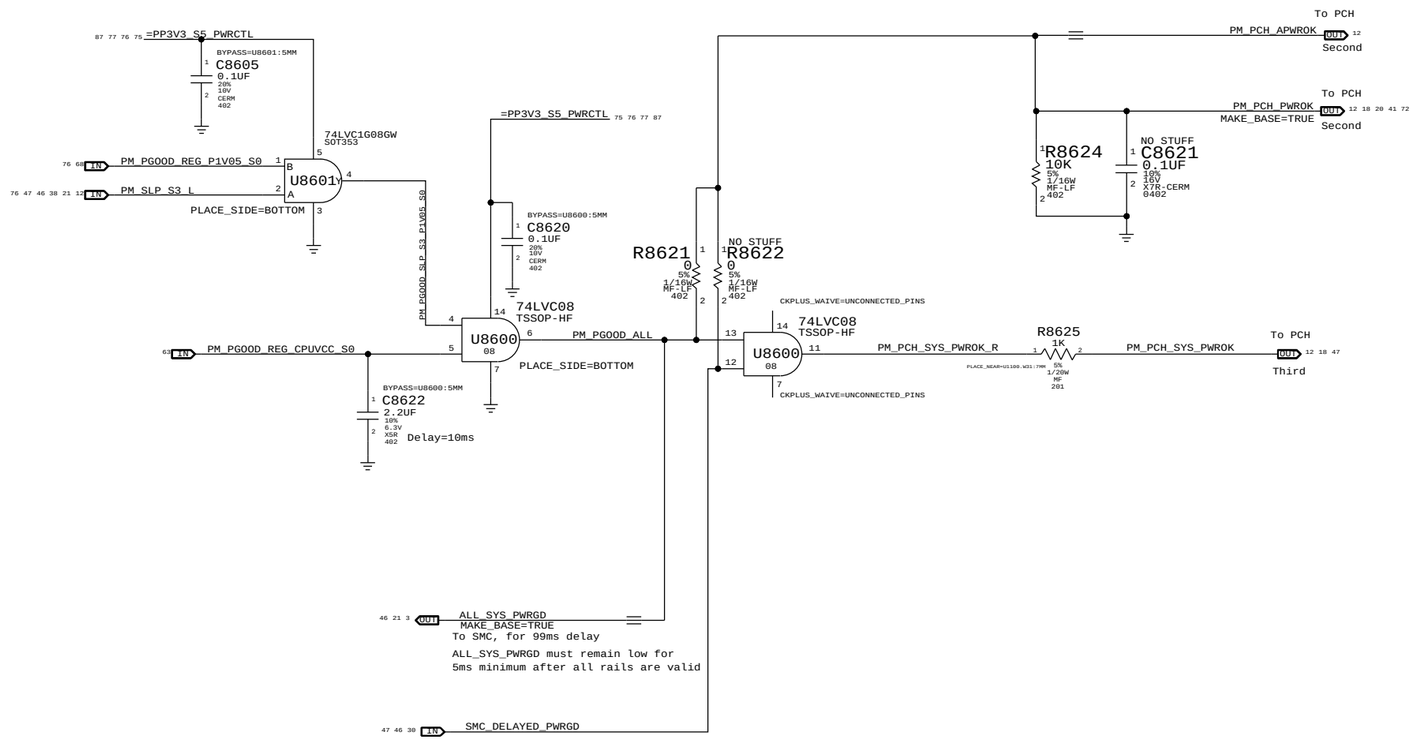
DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 85 OF 127
SHEET 76 OF 106

ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods



Resume Reset

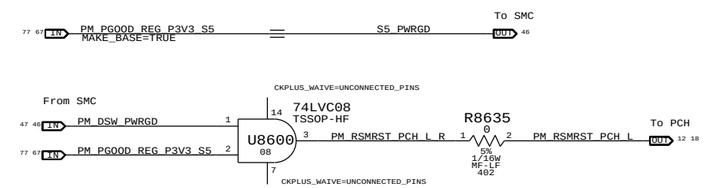
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J16/J17 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
PM Power Good

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DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 86 OF 127
SHEET 77 OF 106

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Page Notes

Power aliases required by this page:

- +PP3V3_GPU_VDD33

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

ALL LANES ARE REVERSED (SEE ALIASES ON CSA 102),SEE DIFF PAIRS FOR POLARITY SWAPPED

93 78 PEG_R2D_N<0>	C8720	0.22UF	1	2	PEG_R2D_C_P<0> 88 93
POLARITY SWAPPED!		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_P<0>	C8721	0.22UF	1	2	PEG_R2D_C_N<0> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<1>	C8722	0.22UF	1	2	PEG_R2D_C_P<1> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 78 PEG_R2D_P<1>	C8723	0.22UF	1	2	PEG_R2D_C_N<1> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_P<2>	C8724	0.22UF	1	2	PEG_R2D_C_P<2> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<2>	C8725	0.22UF	1	2	PEG_R2D_C_N<2> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_P<3>	C8726	0.22UF	1	2	PEG_R2D_C_P<3> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<3>	C8727	0.22UF	1	2	PEG_R2D_C_N<3> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_P<4>	C8728	0.22UF	1	2	PEG_R2D_C_P<4> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<4>	C8729	0.22UF	1	2	PEG_R2D_C_N<4> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<5>	C8730	0.22UF	1	2	PEG_R2D_C_P<5> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 78 PEG_R2D_P<5>	C8731	0.22UF	1	2	PEG_R2D_C_N<5> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
	C8732	0.22UF	1	2	
93 78 PEG_R2D_P<6>		GND_VOID=TRUE		20% 6.3V X5R 0201	PEG_R2D_C_P<6> 88 93
	C8733	0.22UF	1	2	
93 78 PEG_R2D_N<6>		GND_VOID=TRUE		20% 6.3V X5R 0201	PEG_R2D_C_N<6> 88 93
	C8734	0.22UF	1	2	
93 78 PEG_R2D_P<7>		GND_VOID=TRUE		20% 6.3V X5R 0201	PEG_R2D_C_P<7> 88 93
	C8735	0.22UF	1	2	
93 78 PEG_R2D_N<7>		GND_VOID=TRUE		20% 6.3V X5R 0201	PEG_R2D_C_N<7> 88 93

93 78 PEG_R2D_N<8>	C8736	0.22UF	1	2	PEG_R2D_C_P<8> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 78 PEG_R2D_P<8>	C8737	0.22UF	1	2	PEG_R2D_C_N<8> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<9>	C8738	0.22UF	1	2	PEG_R2D_C_P<9> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 78 PEG_R2D_P<9>	C8739	0.22UF	1	2	PEG_R2D_C_N<9> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<10>	C8740	0.22UF	1	2	PEG_R2D_C_P<10> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 78 PEG_R2D_P<10>	C8741	0.22UF	1	2	PEG_R2D_C_N<10> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_P<11>	C8742	0.22UF	1	2	PEG_R2D_C_P<11> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<11>	C8743	0.22UF	1	2	PEG_R2D_C_N<11> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<12>	C8744	0.22UF	1	2	PEG_R2D_C_P<12> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 78 PEG_R2D_P<12>	C8745	0.22UF	1	2	PEG_R2D_C_N<12> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 78 PEG_R2D_N<13>	C8746	0.22UF	1	2	PEG_R2D_C_P<13> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 78 PEG_R2D_P<13>	C8747	0.22UF	1	2	PEG_R2D_C_N<13> 88 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
	C8748	0.22UF	1	2	
93 78 PEG_R2D_N<14>		GND_VOID=TRUE		20% 6.3V X5R 0201	PEG_R2D_C_P<14> 88 93
POLARITY SWAPPED!	C8749	0.22UF	1	2	
93 78 PEG_R2D_P<14>		GND_VOID=TRUE		20% 6.3V X5R 0201	PEG_R2D_C_N<14> 88 93
	C8750	0.22UF	1	2	
93 78 PEG_R2D_P<15>		GND_VOID=TRUE		20% 6.3V X5R 0201	PEG_R2D_C_P<15> 88 93
	C8751	0.22UF	1	2	
93 78 PEG_R2D_N<15>		GND_VOID=TRUE		20% 6.3V X5R 0201	PEG_R2D_C_N<15> 88 93

ALL LANES ARE REVERSED (SEE ALIASES ON CSA 102),SEE DIFF PAIRS FOR POLARITY SWAPPED

93 88 PEG_D2R_P<0>	C8755	0.22UF	1	2	PEG_D2R_C_P<0> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<0>	C8756	0.22UF	1	2	PEG_D2R_C_N<0> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<1>	C8757	0.22UF	1	2	PEG_D2R_C_P<1> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<1>	C8758	0.22UF	1	2	PEG_D2R_C_N<1> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<2>	C8759	0.22UF	1	2	PEG_D2R_C_P<2> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 88 PEG_D2R_P<2>	C8760	0.22UF	1	2	PEG_D2R_C_N<2> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<3>	C8761	0.22UF	1	2	PEG_D2R_C_P<3> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<3>	C8762	0.22UF	1	2	PEG_D2R_C_N<3> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<4>	C8763	0.22UF	1	2	PEG_D2R_C_P<4> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<4>	C8764	0.22UF	1	2	PEG_D2R_C_N<4> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<5>	C8765	0.22UF	1	2	PEG_D2R_C_P<5> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<5>	C8766	0.22UF	1	2	PEG_D2R_C_N<5> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<6>	C8767	0.22UF	1	2	PEG_D2R_C_P<6> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<6>	C8768	0.22UF	1	2	PEG_D2R_C_N<6> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<7>	C8769	0.22UF	1	2	PEG_D2R_C_P<7> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 88 PEG_D2R_P<7>	C8770	0.22UF	1	2	PEG_D2R_C_N<7> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	

93 88 PEG_D2R_P<8>	C8771	0.22UF	1	2	PEG_D2R_C_P<8> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<8>	C8772	0.22UF	1	2	PEG_D2R_C_N<8> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<9>	C8773	0.22UF	1	2	PEG_D2R_C_P<9> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<9>	C8774	0.22UF	1	2	PEG_D2R_C_N<9> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<10>	C8775	0.22UF	1	2	PEG_D2R_C_P<10> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 88 PEG_D2R_P<10>	C8776	0.22UF	1	2	PEG_D2R_C_N<10> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<11>	C8777	0.22UF	1	2	PEG_D2R_C_P<11> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<11>	C8778	0.22UF	1	2	PEG_D2R_C_N<11> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<12>	C8779	0.22UF	1	2	PEG_D2R_C_P<12> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 88 PEG_D2R_P<12>	C8780	0.22UF	1	2	PEG_D2R_C_N<12> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<13>	C8781	0.22UF	1	2	PEG_D2R_C_P<13> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<13>	C8782	0.22UF	1	2	PEG_D2R_C_N<13> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_P<14>	C8783	0.22UF	1	2	PEG_D2R_C_P<14> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<14>	C8784	0.22UF	1	2	PEG_D2R_C_N<14> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
93 88 PEG_D2R_N<15>	C8785	0.22UF	1	2	PEG_D2R_C_P<15> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	
POLARITY SWAPPED!					
93 88 PEG_D2R_P<15>	C8786	0.22UF	1	2	PEG_D2R_C_N<15> 78 93
		GND_VOID=TRUE		20% 6.3V X5R 0201	

OMIT_TABLE

U8700
NV-GK107
BGA
(1 OF 10)

93 78 PEG_R2D_P<0>	AN12	PEX_RX0	PEX_TX0	AK14	PEG_D2R_C_P<0> 78 93
93 78 PEG_R2D_N<0>	AM12	PEX_RX0*	PEX_TX0*	AJ14	PEG_D2R_C_N<0> 78 93
93 78 PEG_R2D_P<1>	AN14	PEX_RX1	PEX_TX1	AH14	PEG_D2R_C_P<1> 78 93
93 78 PEG_R2D_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_C_N<1> 78 93
93 78 PEG_R2D_P<2>	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_C_P<2> 78 93
93 78 PEG_R2D_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_C_N<2> 78 93
93 78 PEG_R2D_P<3>	AN15	PEX_RX3	PEX_TX3	AL16	PEG_D2R_C_P<3> 78 93
93 78 PEG_R2D_N<3>	AM15	PEX_RX3*	PEX_TX3*	AK16	PEG_D2R_C_N<3> 78 93
93 78 PEG_R2D_P<4>	AN17	PEX_RX4	PEX_TX4	AK17	PEG_D2R_C_P<4> 78 93
93 78 PEG_R2D_N<4>	AM17	PEX_RX4*	PEX_TX4*	AJ17	PEG_D2R_C_N<4> 78 93
93 78 PEG_R2D_P<5>	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_C_P<5> 78 93
93 78 PEG_R2D_N<5>	AP18	PEX_RX5*	PEX_TX5*	AG17	PEG_D2R_C_N<5> 78 93
93 78 PEG_R2D_P<6>	AN18	PEX_RX6	PEX_TX6	AK18	PEG_D2R_C_P<6> 78 93
93 78 PEG_R2D_N<6>	AM18	PEX_RX6*	PEX_TX6*	AJ18	PEG_D2R_C_N<6> 78 93
93 78 PEG_R2D_P<7>	AN20	PEX_RX7	PEX_TX7	AL19	PEG_D2R_C_P<7> 78 93
93 78 PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7> 78 93
93 78 PEG_R2D_P<8>	AP20	PEX_RX8	PEX_TX8	AK20	PEG_D2R_C_P<8> 78 93
93 78 PEG_R2D_N<8>	AP21	PEX_RX8*	PEX_TX8*	AJ20	PEG_D2R_C_N<8> 78 93
93 78 PEG_R2D_P<9>	AN21	PEX_RX9	PEX_TX9	AH20	PEG_D2R_C_P<9> 78 93
93 78 PEG_R2D_N<9>	AM21	PEX_RX9*	PEX_TX9*	AG20	PEG_D2R_C_N<9> 78 93
93 78 PEG_R2D_P<10>	AN23	PEX_RX10	PEX_TX10	AK21	PEG_D2R_C_P<10> 78 93
93 78 PEG_R2D_N<10>	AM23	PEX_RX10*	PEX_TX10*	AJ21	PEG_D2R_C_N<10> 78 93
93 78 PEG_R2D_P<11>	AP23	PEX_RX11	PEX_TX11	AL22	PEG_D2R_C_P<11> 78 93
93 78 PEG_R2D_N<11>	AP24	PEX_RX11*	PEX_TX11*	AK22	PEG_D2R_C_N<11> 78 93
93 78 PEG_R2D_P<12>	AN24	PEX_RX12	PEX_TX12	AK23	PEG_D2R_C_P<12> 78 93
93 78 PEG_R2D_N<12>	AM24	PEX_RX12*	PEX_TX12*	AJ23	PEG_D2R_C_N<12> 78 93
93 78 PEG_R2D_P<13>	AN26	PEX_RX13	PEX_TX13	AH23	PEG_D2R_C_P<13> 78 93
93 78 PEG_R2D_N<13>	AM26	PEX_RX13*	PEX_TX13*	AG23	PEG_D2R_C_N<13> 78 93
93 78 PEG_R2D_P<14>	AP26	PEX_RX14	PEX_TX14	AK24	PEG_D2R_C_P<14> 78 93
93 78 PEG_R2D_N<14>	AP27	PEX_RX14*	PEX_TX14*	AJ24	PEG_D2R_C_N<14> 78 93
93 78 PEG_R2D_P<15>	AN27	PEX_RX15	PEX_TX15	AL25	PEG_D2R_C_P<15> 78 93
93 78 PEG_R2D_N<15>	AM27	PEX_RX15*	PEX_TX15*	AK25	PEG_D2R_C_N<15> 78 93
93 11 IN PEG_CLK100M_P	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26	103 PEX_TSTCLK_O_PL
93 11 IN PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	103 PEX_TSTCLK_O_NG
88 84 IN GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29	103 GPU_PEX_TERMP
11 OUT PEG_CLKREQ_L	AK12	PEX_CLKREQ*			
NC	AJ11	PEX_WAKE*	PEX_SVDD_3V3	AG12	=PP3V3_GPU_VDD33 83 84 85 86

R8700 0 GPU_RESET_R_L 1 2 MF 5% 1/20W 0201

R8702 200 1 2 1% 1/20W MF 201 NOSTUFF PLACE_NEAR=U8700.AJ26:8MM

R8705 2.49K 1 2 1% 1/20W MF 201 PLACE_NEAR=U8700.AP29:8MM

SYNC MASTER=J17 PETE	SYNC DATE=01/21/2013
PAGE TITLE: KEPLER PCI-E	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
	REVISION: A.0.0
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	PAGE: 87 OF 127
	SHEET: 78 OF 106

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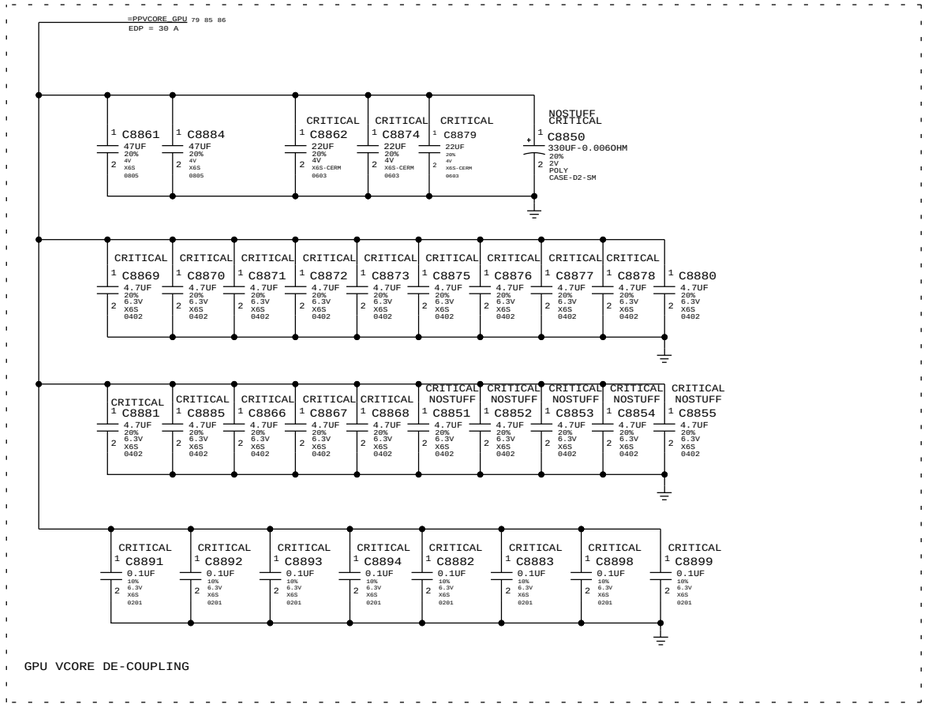

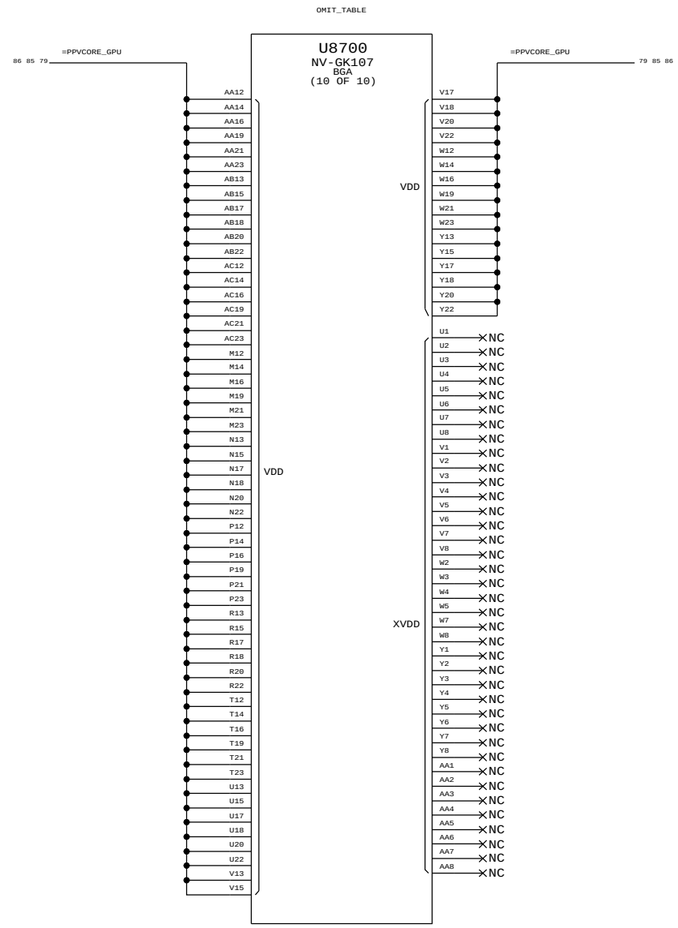

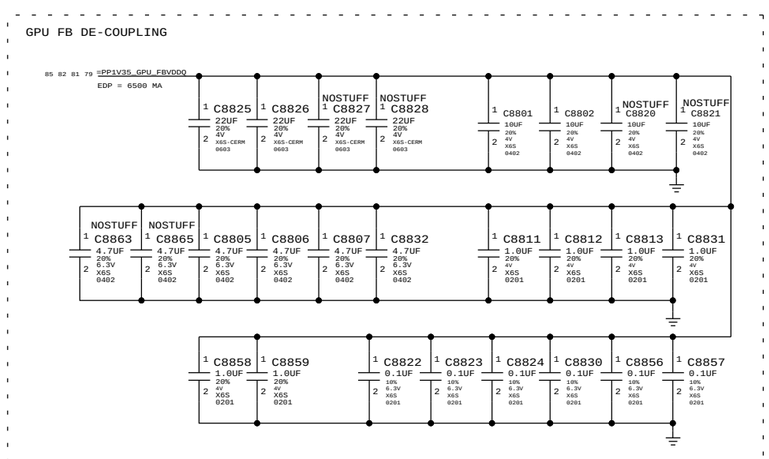

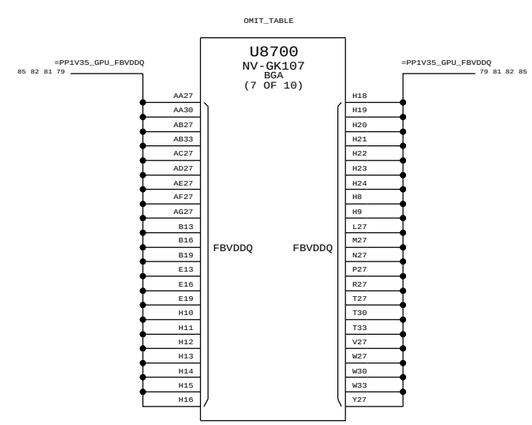

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PPSVSS_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC MASTER=J17 PETE	SYNC DATE=01/21/2013
PAGE TITLE: KEPLER CORE/FB POWER	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
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	PAGE: 88 OF 127
	SHEET: 79 OF 106

NOTE:GDDR5 MODE H MAPPING

OMIT_TABLE

U8700
NV-GK107
BGA
(3 OF 10)
MEM INTERFACE A

FBA_D0	L28	FBA_CMD0	U30
FBA_D1	M29	FBA_CMD1	T31
FBA_D2	L29	FBA_CMD2	U29
FBA_D3	M28	FBA_CMD3	R34
FBA_D4	N31	FBA_CMD4	R33
FBA_D5	P29	FBA_CMD5	U32
FBA_D6	R29	FBA_CMD6	U33
FBA_D7	P28	FBA_CMD7	U28
FBA_D8	J28	FBA_CMD8	V28
FBA_D9	H29	FBA_CMD9	V29
FBA_D10	J29	FBA_CMD10	V30
FBA_D11	H28	FBA_CMD11	U34
FBA_D12	G29	FBA_CMD12	U31
FBA_D13	E31	FBA_CMD13	V34
FBA_D14	E32	FBA_CMD14	V33
FBA_D15	F30	FBA_CMD15	Y32
FBA_D16	C34	FBA_CMD16	AA31
FBA_D17	D32	FBA_CMD17	AA29
FBA_D18	B33	FBA_CMD18	AA28
FBA_D19	C33	FBA_CMD19	AC34
FBA_D20	F33	FBA_CMD20	AC33
FBA_D21	F32	FBA_CMD21	AA32
FBA_D22	H33	FBA_CMD22	AA33
FBA_D23	H32	FBA_CMD23	Y28
FBA_D24	P34	FBA_CMD24	Y29
FBA_D25	P32	FBA_CMD25	W31
FBA_D26	P31	FBA_CMD26	Y30
FBA_D27	P33	FBA_CMD27	AA34
FBA_D28	L31	FBA_CMD28	Y31
FBA_D29	L34	FBA_CMD29	Y34
FBA_D30	L32	FBA_CMD30	Y33
FBA_D31	L33	FBA_CMD31	V31
FBA_D32	AG28		
FBA_D33	AF29	FBA_CLK0	R30
FBA_D34	AG29	FBA_CLK0*	R31
FBA_D35	AF28	FBA_CLK1	AB31
FBA_D36	AD30	FBA_CLK1*	AC31
FBA_D37	AD29		
FBA_D38	AC29	FBA_DQM0	P30
FBA_D39	AD28	FBA_DQM1	F31
FBA_D40	AJ29	FBA_DQM2	F34
FBA_D41	AK29	FBA_DQM3	M32
FBA_D42	AJ30	FBA_DQM4	AD31
FBA_D43	AK28	FBA_DQM5	AL29
FBA_D44	AM29	FBA_DQM6	AM32
FBA_D45	AM31	FBA_DQM7	AF34
FBA_D46	AN29		
FBA_D47	AM30	FBA_DQS_RN0	M30
FBA_D48	AN31	FBA_DQS_RN1	H30
FBA_D49	AN32	FBA_DQS_RN2	E34
FBA_D50	AP30	FBA_DQS_RN3	M34
FBA_D51	AP32	FBA_DQS_RN4	AF30
FBA_D52	AM33	FBA_DQS_RN5	AK31
FBA_D53	AL31	FBA_DQS_RN6	AM34
FBA_D54	AK33	FBA_DQS_RN7	AF32
FBA_D55	AK32		
FBA_D56	AD34	FBA_DQS_WP0	M31
FBA_D57	AD32	FBA_DQS_WP1	G31
FBA_D58	AC30	FBA_DQS_WP2	E33
FBA_D59	AD33	FBA_DQS_WP3	M33
FBA_D60	AF31	FBA_DQS_WP4	AE31
FBA_D61	AG34	FBA_DQS_WP5	AK30
FBA_D62	AG32	FBA_DQS_WP6	AN33
FBA_D63	AG33	FBA_DQS_WP7	AF33
		FBA_DLL_AVDD	K27
FBA_WCK01	K31	FBA_PLL_AVDD	U27
FBA_WCK01*	L30		
FBA_WCK23	H34	FBA_DEBUG	R28
FBA_WCK23*	J34	FBA_DEBUG	AC28
FBA_WCK45	AG30		
FBA_WCK45*	AG31	FB_CAL_PD_VDDQ	J27
FBA_WCK67	AJ34	FB_CAL_PU_GND	H27
FBA_WCK67*	AK34	FB_CAL_TERM_GND	H25
		FB_CLAMP	E1
NC	J30	FBA_CMD_RFU	R32
NC	J31	FBA_CMD_RFU	AC32
FBA_WCKB01			
FBA_WCKB01*		FB_VDDQ_SENSE	F1
NC	J32		
NC	J33	FB_GND_SENSE	F2
FBA_WCKB23			
FBA_WCKB23*			
NC	AH31		
NC	AJ31		
FBA_WCKB45			
FBA_WCKB45*			
NC	AJ32		
NC	AJ33		
FBA_WCKB67			
FBA_WCKB67*			

103 81 80 FB_A0_RESET_L — R9050 10K 1% 1/20W MF 201
103 81 80 FB_A1_RESET_L — R9051 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 80 85
R9052 10K 1% 1/20W MF 201 — 103 81 80 FB_A0_CKE_L
R9053 10K 1% 1/20W MF 201 — 103 81 80 FB_A1_CKE_L

=PP1V35_GPU_S0_FB 80 85
NOSTUFF R9058 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8700.H26:5.0MM
FB_VREF 80
NOSTUFF R9059 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8700.H26:8.4MM
NOSTUFF C9060 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=U8700.H26:8.4MM

FB VREF GEN (TEST ONLY)

=PP1V35_GPU_S0_FB 80 85
NOSTUFF R9003 60.4 1% 1/20W MF 201
NOSTUFF R9002 60.4 1% 1/20W MF 201
NOSTUFF R9070 100 5% 1/20W MF 201
R9001 1.0K 1% 1/20W MF 201 — PLACE_NEAR=U8700.H25:8.4MM
R9061 10K 1% 1/20W MF 201
NOSTUFF R9071 100 5% 1/20W MF 201

PLACE CLOSE TO BGA
103 80 FB_CAL_PU_GND — PLACE_NEAR=U8700.H27:8.4MM — R9004 40.2 1% 1/20W MF 201
=PP1V35_GPU_S0_FB 80 85 — PLACE_NEAR=U8700.J27:8.4MM — R9005 40.2 1% 1/20W MF 201 — FB_CAL_PD_VDDQ 80 103

OMIT_TABLE

U8700
NV-GK107
BGA
(4 OF 10)
MEM INTRERFACE B

FBB_D0	G9	FBB_CMD0	D13
FBB_D1	E9	FBB_CMD1	E14
FBB_D2	G8	FBB_CMD2	F14
FBB_D3	F9	FBB_CMD3	A12
FBB_D4	F11	FBB_CMD4	B12
FBB_D5	G11	FBB_CMD5	C14
FBB_D6	F12	FBB_CMD6	B14
FBB_D7	G12	FBB_CMD7	G15
FBB_D8	G6	FBB_CMD8	F15
FBB_D9	F5	FBB_CMD9	E15
FBB_D10	E6	FBB_CMD10	D15
FBB_D11	F6	FBB_CMD11	A14
FBB_D12	F4	FBB_CMD12	D14
FBB_D13	G4	FBB_CMD13	A15
FBB_D14	E2	FBB_CMD14	B15
FBB_D15	F3	FBB_CMD15	C17
FBB_D16	C2	FBB_CMD16	D18
FBB_D17	D4	FBB_CMD17	E18
FBB_D18	D3	FBB_CMD18	F18
FBB_D19	C1	FBB_CMD19	A20
FBB_D20	B3	FBB_CMD20	B20
FBB_D21	C4	FBB_CMD21	C18
FBB_D22	B5	FBB_CMD22	B18
FBB_D23	C5	FBB_CMD23	G18
FBB_D24	A11	FBB_CMD24	G17
FBB_D25	C11	FBB_CMD25	F17
FBB_D26	D11	FBB_CMD26	D16
FBB_D27	B11	FBB_CMD27	A18
FBB_D28	D8	FBB_CMD28	D17
FBB_D29	A8	FBB_CMD29	A17
FBB_D30	C8	FBB_CMD30	B17
FBB_D31	B8	FBB_CMD31	E17
FBB_D32	F24		
FBB_D33	G23	FBB_CLK0	D12
FBB_D34	E24	FBB_CLK0*	E12
FBB_D35	G24	FBB_CLK1	E20
FBB_D36	D21	FBB_CLK1*	F20
FBB_D37	E21		
FBB_D38	G21	FBB_DQM0	E11
FBB_D39	F21	FBB_DQM1	E3
FBB_D40	G27	FBB_DQM2	A3
FBB_D41	D27	FBB_DQM3	C9
FBB_D42	G26	FBB_DQM4	F23
FBB_D43	E27	FBB_DQM5	F27
FBB_D44	E29	FBB_DQM6	C30
FBB_D45	F29	FBB_DQM7	A24
FBB_D46	E30		
FBB_D47	D30	FBB_DQS_RN0	D9
FBB_D48	A32	FBB_DQS_RN1	E4
FBB_D49	C31	FBB_DQS_RN2	B2
FBB_D50	C32	FBB_DQS_RN3	A9
FBB_D51	B32	FBB_DQS_RN4	D22
FBB_D52	D29	FBB_DQS_RN5	D28
FBB_D53	A29	FBB_DQS_RN6	A30
FBB_D54	C29	FBB_DQS_RN7	B23
FBB_D55	B29		
FBB_D56	B21	FBB_DQS_WP0	D10
FBB_D57	C23	FBB_DQS_WP1	D5
FBB_D58	A21	FBB_DQS_WP2	C3
FBB_D59	C21	FBB_DQS_WP3	B9
FBB_D60	B24	FBB_DQS_WP4	E23
FBB_D61	C24	FBB_DQS_WP5	E28
FBB_D62	B26	FBB_DQS_WP6	B30
FBB_D63	C26	FBB_DQS_WP7	A23
FBB_WCK01	F8	FBB_PLL_AVDD	H17
FBB_WCK01*	E8	FBB_DEBUG0	G14
FBB_WCK23	A5	FBB_DEBUG1	G20
FBB_WCK23*	A6	FB_VREF	H26
FBB_WCK45	D24		
FBB_WCK45*	D25	FBB_CMD_RFU0	C12
FBB_WCK67	B27	FBB_CMD_RFU1	C20
FBB_WCK67*	C27		
NC	D6		
FBB_WCKB01			
FBB_WCKB01*	D7		
NC	C6		
FBB_WCKB23			
FBB_WCKB23*	B6		
NC	F26		
FBB_WCKB45			
FBB_WCKB45*	E26		
NC	A26		
FBB_WCKB67			
FBB_WCKB67*	A27		

=PP1V35_GPU_S0_FB 80 85
NOSTUFF R9006 60.4 1% 1/20W MF 201 — 80 GPU_FBB_DEBUG0
NOSTUFF R9007 60.4 1% 1/20W MF 201 — 80 GPU_FBB_DEBUG1

=PP1V05_GPU_PEX_IOVDD — L9001 30-OHM-25%-5A-0.01-OHM 0603 CRITICAL ESR = 0.050OHM — PP1V05_GPU_FB_PLL_AVDD 80
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
C9001 20UF 20% 4V X5R-CERM 0402; C9002 1.0UF 20% 4V X6S 0201; C9003 0.1UF 10% 6.3V X6S 0201; C9004 0.1UF 10% 6.3V X6S 0201

RDAR://11427653 D8: NV GUIDELINE USES 22UF. APPLE USES 20UF

=PP1V05_GPU_PEX_IOVDD — L9002 30-OHM-25%-5A-0.01-OHM 0603 CRITICAL ESR = 0.050OHM — PP1V05_GPU_FB_DLL_AVDD 80
MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
C9008 20UF 20% 4V X5R-CERM 0402; C9009 1.0UF 20% 4V X6S 0201; C9005 0.1UF 10% 6.3V X6S 0201

FB PLL & DLL VDD

103 82 80 FB_B0_RESET_L — R9054 10K 1% 1/20W MF 201
103 82 80 FB_B1_RESET_L — R9055 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 80 85
R9056 10K 1% 1/20W MF 201 — 103 82 80 FB_B0_CKE_L
R9057 10K 1% 1/20W MF 201 — 103 82 80 FB_B1_CKE_L

MEM VREFC & VREFD SWITCH

82 81 FB_SW_LEG
Q9065 SSM3K15AMFVAPE VESM (CRITICAL)
GPU_ALT_VREF — 84
R9060 10K 5% 1/20W MF 201

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC MASTER=J17 PETE	SYNC DATE=11/02/2012
PAGE TITLE: KEPLER FRAME BUFFER I/F	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
	REVISION: A.0.0
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	PAGE: 90 OF 127
	SHEET: 80 OF 106

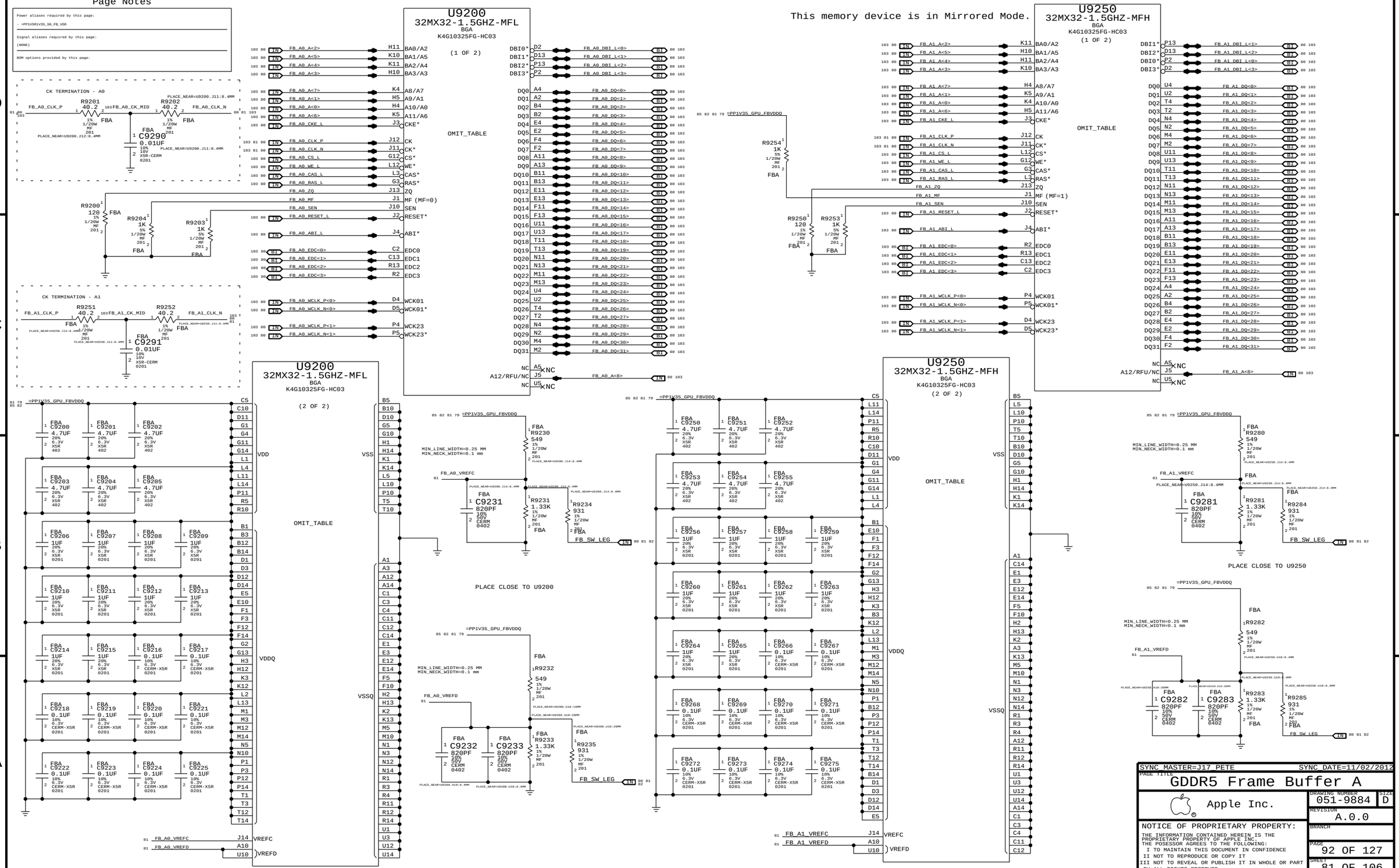
Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

This memory device is in Mirrored Mode.



SYNC MASTER=J17 PETE SYNC DATE=11/02/2012

PAGE TITLE
GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

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PAGE 92 OF 127

SHEET 81 OF 106

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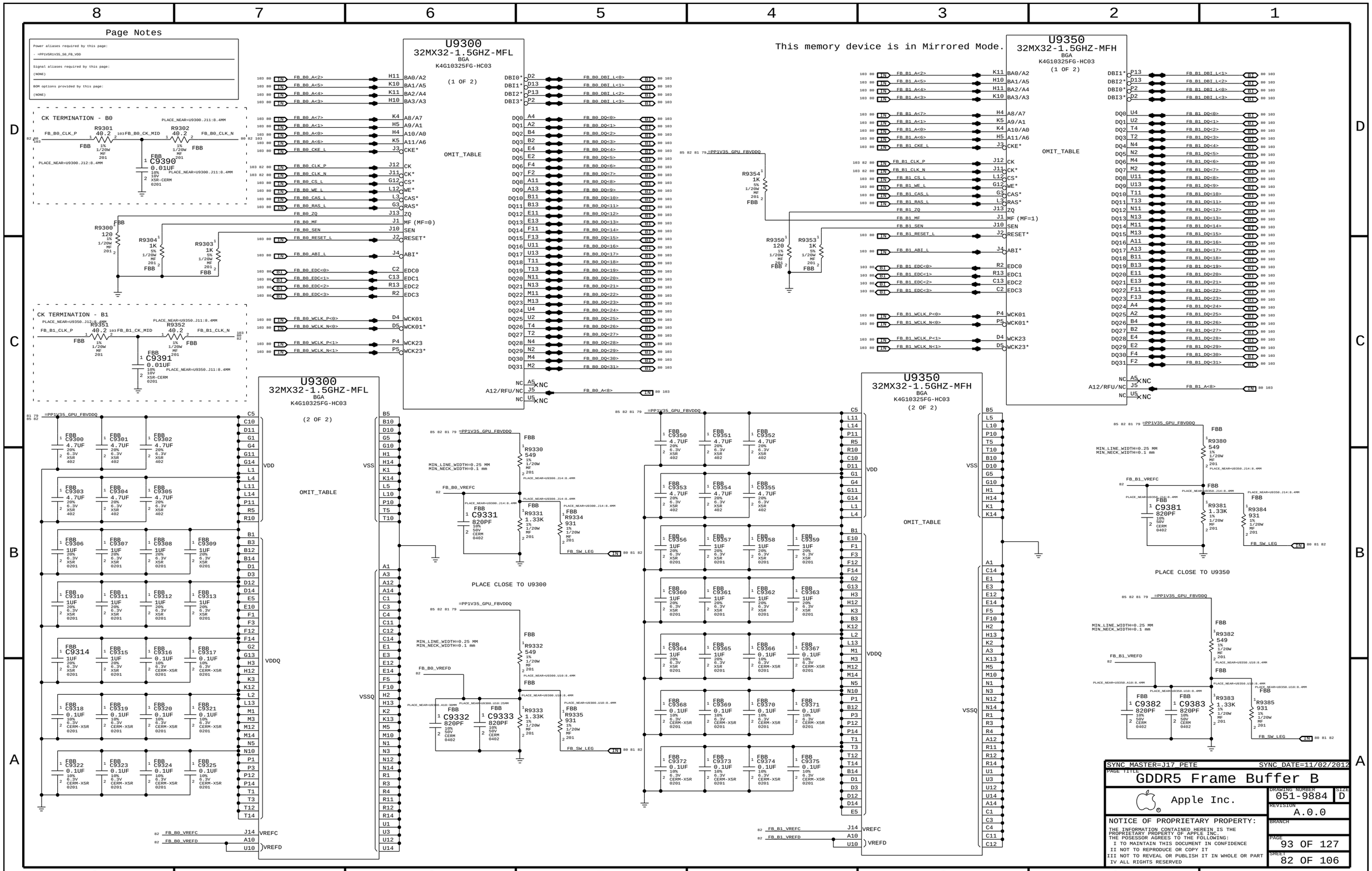
Page Notes
Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
This memory device is in Mirrored Mode.
U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
U9300
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
U9350
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
CK TERMINATION - B0
CK TERMINATION - B1
PLACE CLOSE TO U9300
PLACE CLOSE TO U9350
VDD
VSS
VDDQ
VSSQ
VREFC
VREFD
SYNC MASTER=J17 PETE
SYNC DATE=11/02/2012
PAGE TITLE
GDDR5 Frame Buffer B
Apple Inc.
DRAWING NUMBER
051-9884
SIZE
D
REVISION
A.0.0
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PAGE
93 OF 127
SHEET
82 OF 106
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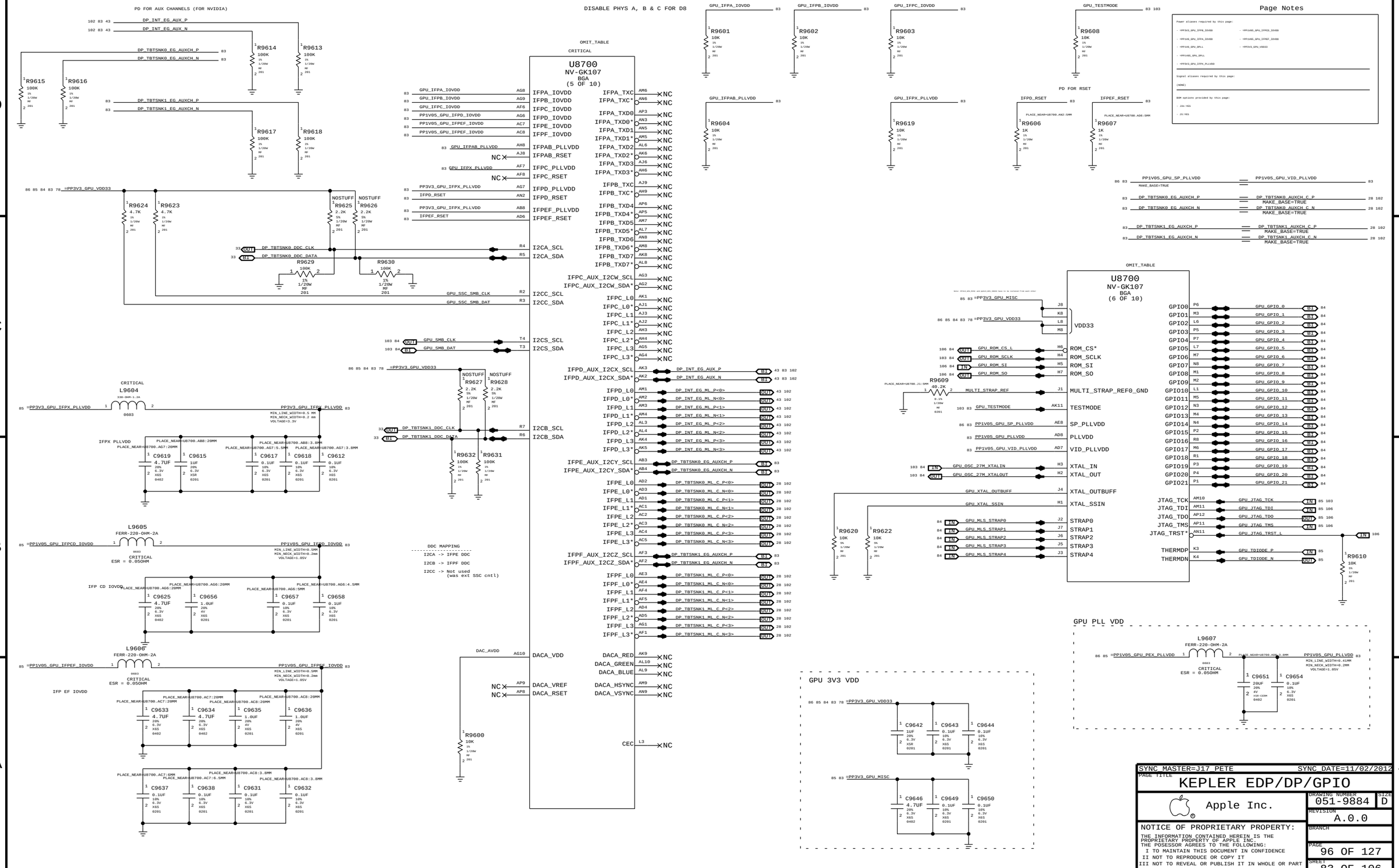
PD FOR AUX CHANNELS (FOR NVIDIA)
DISABLE PHYS A, B & C FOR D8
OMIT_TABLE
U8700
NV-GK107
BGA
(5 OF 10)
U8700
NV-GK107
BGA
(6 OF 10)
Page Notes
PD FOR RSET
DDC MAPPING
I2CA -> IFPE DDC
I2CB -> IFPF DDC
I2CC -> Not used
(was ext SSC cntl)
GPU PLL VDD
GPU 3V3 VDD
SYNC_MASTER=J17_PETE
SYNC_DATE=11/02/2012
PAGE TITLE
KEPLER EDP/DP/GPIO
Apple Inc.
DRAWING NUMBER
051-9884
SIZE
D
REVISION
A.0.0
BRANCH
PAGE
96 OF 127
SHEET
83 OF 106
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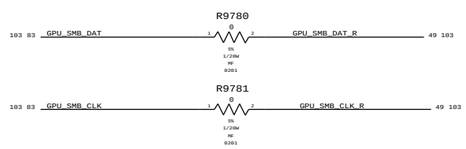
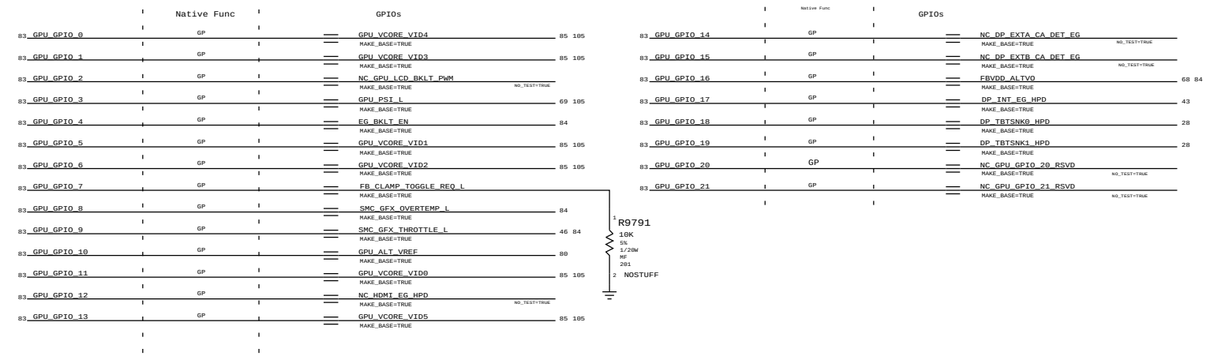
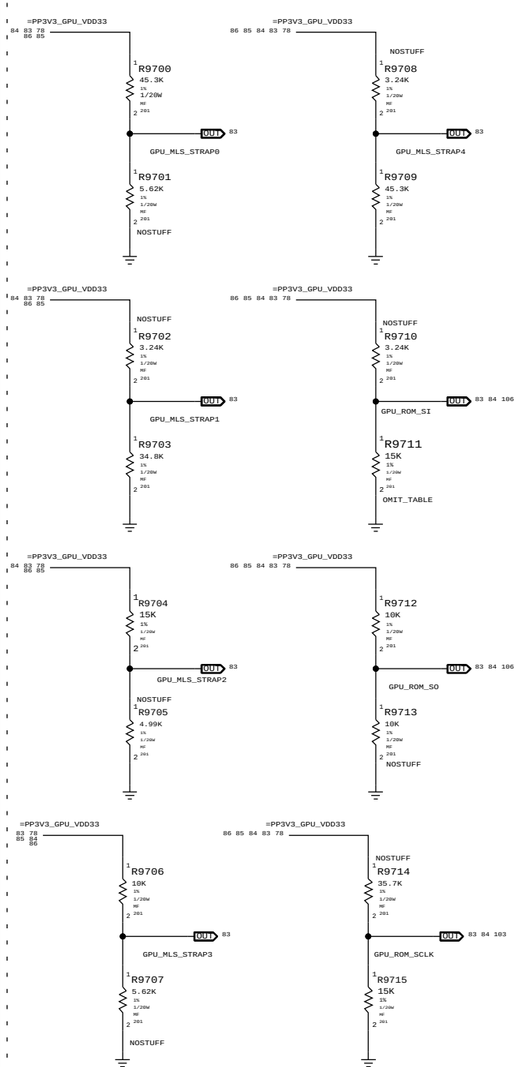
ISOLATION R's for GPU Int Temp Sense



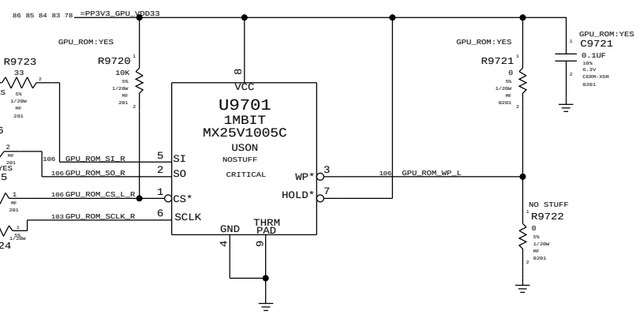
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0280	1	RES,MF,30.1K ,1,1/20W,0201	R9711		FB:2G_ELPIDA
118S0230	1	RES,MF,24.9K ,1,1/20W,0201	R9711		FB:2G_HYNIX



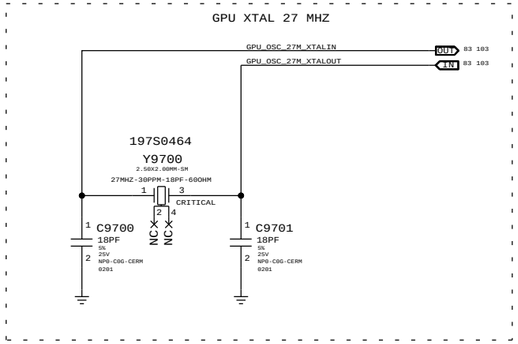
CONFIG STRAPS - MLPS USE 1% FOR ACCURACY



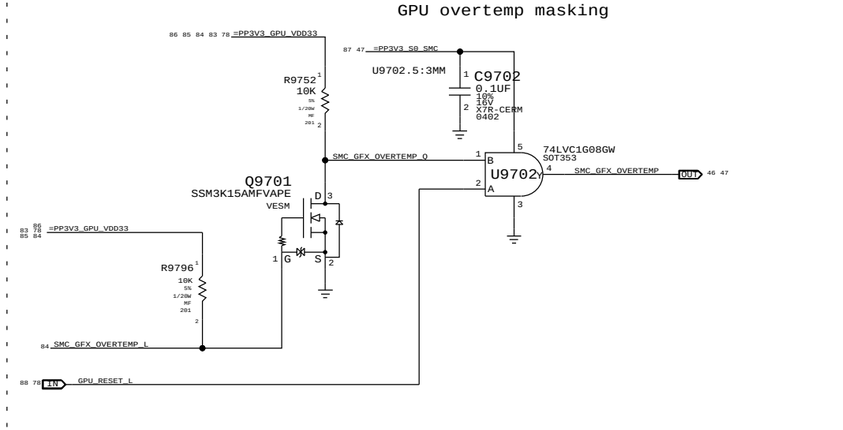
GPU VBIOS ROM

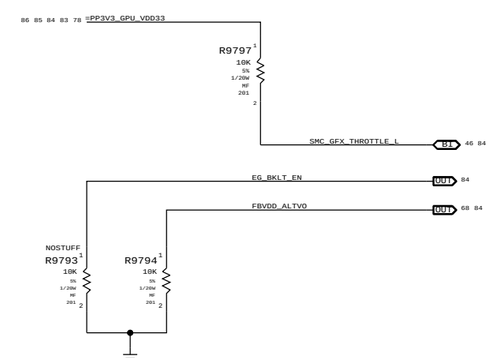


GPU XTAL 27 MHZ



GPU overtemp masking





SYNC_MASTER=J17_PETE SYNC_DATE=11/02/2012

PAGE TITLE
KEPLER GPIOS,CLK & STRAPS

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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PAGE 97 OF 127

SHEET 84 OF 106

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GPU POWER ALIAS

82 81 79	=PP1V35_GPU_FBVDDQ	=PP1V35_S0_GPU_FBVDDQ	87
80	=PP1V35_GPU_S0_FB		
86 79	=PPVCORE_GPU	=PPVCORE_S0_GPU	87
86 80	=PP1V05_GPU_PEX_IOVDD	=PP1V05_S0_GPU_PEX_IOVDD	87
86 84 83 78	=PP3V3_GPU_VDD33	=PP3V3_S0_GPU_VDD33	87
83	=PP3V3_GPU_MISC	=PP3V3_S0_GPU_MISC	87
86 83	=PP1V05_GPU_PEX_PLLVDD	=PP1V05_S0_GPU_PEX_PLLVDD	87
83	=PP1V05_GPU_IFPCD_IOVDD	=PP1V05_S0_GPU_IFPCD_IOVDD	87
83	=PP1V05_GPU_IFPEF_IOVDD	=PP1V05_S0_GPU_IFPEF_IOVDD	87
83	=PP3V3_GPU_IFPX_PLLVDD	=PP3V3_S0_GPU_IFPX_PLLVDD	87

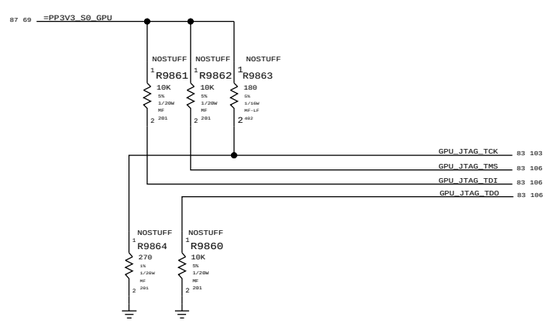
GPU SIGNAL & SENSE ALIAS

86	GPU_VDD_SENSE	VSNS_GPU_VDD MAKE_BASE=TRUE		69 105
86	GPU_GND_SENSE	VSNS_GPU_VSS MAKE_BASE=TRUE		69 105
80	SNS_GPUVDDQ_P	VSNS_FBVDDQ_P MAKE_BASE=TRUE		68 105
80	SNS_GPUVDDQ_N	VSNS_FBVDDQ_N MAKE_BASE=TRUE		68 105
83	GPU_TDIODE_P	NC_GPU_TDIODEP MAKE_BASE=TRUE	NO_TEST=TRUE	
83	GPU_TDIODE_N	NC_GPU_TDIODEN MAKE_BASE=TRUE	NO_TEST=TRUE	

GPU VIDS ALIAS (VR VID0 IS TIED LOW)

105 84	GPU_VCORE_VID0	R9850 0 5% 1/20W MF 0201	REG_GPUCORE_VID1	69 105
105 84	GPU_VCORE_VID1	R9851 0 5% 1/20W MF 0201	REG_GPUCORE_VID2	69 105
105 84	GPU_VCORE_VID2	R9852 0 5% 1/20W MF 0201	REG_GPUCORE_VID3	69 105
105 84	GPU_VCORE_VID3	R9853 0 5% 1/20W MF 0201	REG_GPUCORE_VID4	69 105
105 84	GPU_VCORE_VID4	R9854 0 5% 1/20W MF 0201	REG_GPUCORE_VID5	69 105
105 84	GPU_VCORE_VID5	R9855 0 5% 1/20W MF 0201	REG_GPUCORE_VID6	69 105

PU/PD IS BASED ON RECOMMENDATION FROM NVDIA FOR THEIR GPU JTAG DEBUGGER



SYNC_MASTER=J17_PETE SYNC_DATE=01/21/2013

PAGE TITLE
GPU SIGNAL & POWER ALIASES

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

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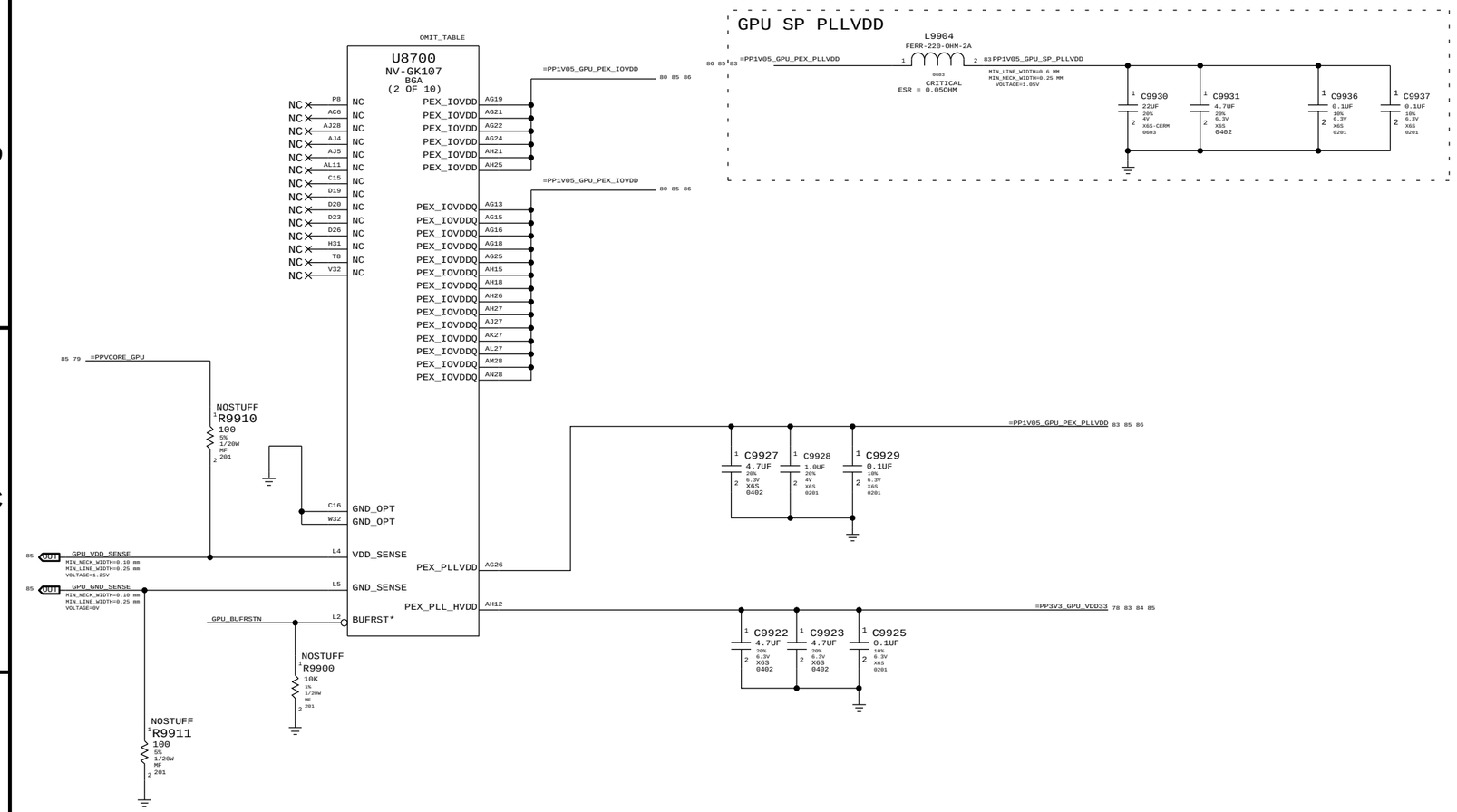
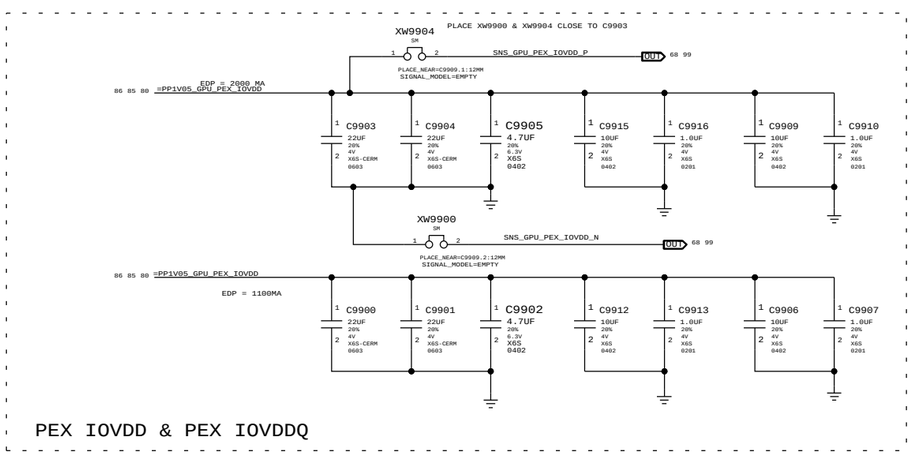
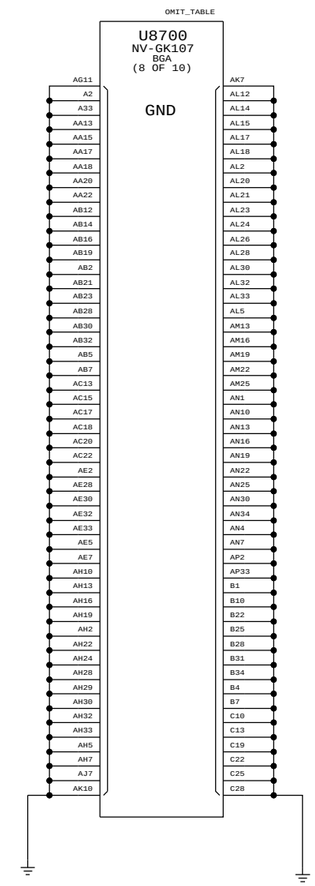
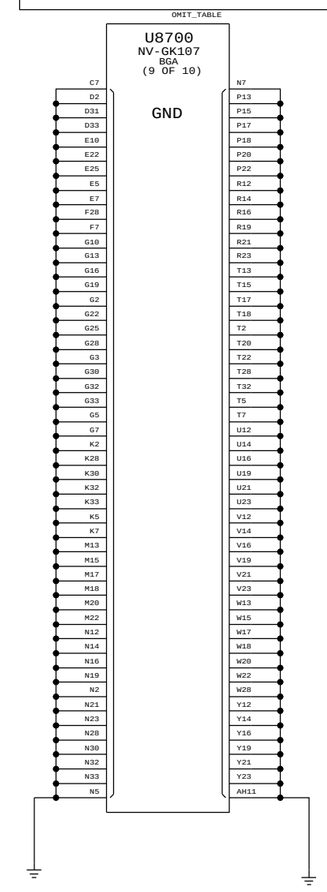




PEX IOVDD & PEX IOVDDQ





Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC_MASTER=J17_PETE	SYNC_DATE=01/21/2013
PAGE TITLE: KEPLER PEX PWR/GNDS	
Apple Inc.	DRAWING NUMBER: 051-9884 SIZE: D
	REVISION: A.0.0
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	PAGE: 99 OF 127
	SHEET: 86 OF 106

G3 Rails
Always on: Keeps the PCH RTC alive

101 PP3V3_G3 (MAKE_BASE=TRUE)	PP3V3_G3_RTC	19
	=PP3V3_G3_PCH_RTC	15
	=PP3V3_G3_PCH	11 12

G3H Rails
On with AC/DC plugged in

101 PP12V_ACDC (MAKE_BASE=TRUE)	PP12V_G3H_ACDC	62
	=PP12V_G3H_SNS_R	50
101 PP12V_G3H (MAKE_BASE=TRUE)	PP12V_G3H_SNS	50
	=PP12V_G3H_P3V42	62
	=PP12V_G3H_FET_P12V_S0	75
	=PP12V_G3H_FET_P12V_S5	75
101 PP3V42_G3H (MAKE_BASE=TRUE)	PP3V42_G3H_REG	62
	=PP3V3_G3H_BT	34
	=PP3V3_G3H_RTC_D	19
	=PP3V3_G3H_SMC	46 47 53
	=PP3V3_G3H_SMC_USBMUX	44
	=PPVIN_G3H_SMCVREF	47
	=PP3V3_G3H_LPCPLUS	48

Ground/Common

GND (MAKE_BASE=TRUE)

S5 Rails
On when in S5

101 PP12V_S5 (MAKE_BASE=TRUE)	PP12V_S5_FET	75
	=PP12V_S5_REG_P3V3P5V_S5	67
	=PP12V_S5_REG_VDDQ_S3	66
	=PP12V_S5_PWRCTL	75 76
	=PPHV_SW_TBTAPWRSW	31
	=PPHV_SW_TBTBPWRSW	32
	=PP12V_S5_SNS	50
101 PP5V_S5 (MAKE_BASE=TRUE)	PP5V_S5_LDO	67
	=PP5V_S5_PWRCTL	67
101 PP3V3_S5 (MAKE_BASE=TRUE)	PP3V3_S5_REG	67
	=PP3V3_S5_FET_P3V3_S0	75
	=PP3V3_S5_FET_P3V3_S4	75
	=PP3V3_S5_SMC	47
	=PP3V3_S5_LED	3
	=PP3V3_S5_PCH_VCCSUS_GPIO	11 12 13 14 15 17
	=PP3V3_S5_PCH_VCCDSW	15 17
	=PP3V3_S5_PCH_VCC_SPI	15 17
	=PP3V3_S5_PCH_VCCSUS_HDA	15 17
	=PP3V3_S5_PCH_VCCSUS_USB	15 17
	=PP3V3_S5_PCH_VCCSUS_RTC	15 17
	=PP3V3_S5_PCH_VCCSUS_USB3	15
	=PP3V3_S5_PCH	19 20
	=PP3V3_S5_PWRCTL	75 76 77
	=PP3V3_S5_ROM	48
	=PP3V3_S5_VRD	67
	=PP3V3_S5_XDP	18
	=PP3V3_S5_SENSE	50
	=PP3V3_S5_SNS	51

S4 Rails
Enabled when system has AC and is in run or sleep

101 PP5V_S4 (MAKE_BASE=TRUE)	PP5V_S4_REG	67
	=PP5V_S4_REG_VDDQ_S3	66
	=PP5V_S4_FET_P5V_S0	75
	=PP5V_S4_MEMRESET	21
	=PP5V_S4_USB	44 45
	=PP5V_S4_CAMERA	40
101 PP3V3_S4 (MAKE_BASE=TRUE)	PP3V3_S4_FET	75
	=PP3V3_S4_FET_ENET	38
	=PP3V3_S4_PWRCTL	66 75
	=PP3V3_S4_ALS	40
	=PP3V3_S4_LED	3
	=PP3V3_S4_MEMRESET	21
	=PP3V3_S4_PCH	13
	=PP3V3_S4_PM	21
	=PP3V3_S4_SDCARD	39
	=PP3V3_S4_SMC	47
	=PP3V3_S4_SMBUS_SMC_2	49
	=PP3V3_S4_TBT	28 29 30 31 32 76
	=PP3V3_S4_CAMERA	40 41
	=PP3V3_S4_AUDIO_DIG	58
	=PP3V3_S4_AP_SNS_R	50
	=PP3V3_S3_VREFMRGN	22
	=PP3V3_S4_TBTAPWRSW	31
	=PP3V3_S4_TBTBPWRSW	32
101 PP3V3_S4_AP (MAKE_BASE=TRUE)	PP3V3_S4_AP_SNS	50
	=PP3V3_S4_AP	34 47

S3 Rails
Enabled when system is in run or sleep

101 PP3V3_ENET (MAKE_BASE=TRUE)	PP3V3_ENET_FET	38
	=PP3V3_ENET_PHY	37 38
	=PP3V3_ENET_SYSCLK	19
	=PPVDDIO_ENET_CLK	19
99 PPVDDQ_S3 (MAKE_BASE=TRUE)	PPVDDQ_S3_REG	66
	=PPVDDQ_S3_SNS_DDR_R	51
THIS IS 1.5V RAIL	=PPVDDQ_S3_FET_VDDQ_S0	75
99 PPVDDQ_S3_DDR (MAKE_BASE=TRUE)	PPVDDQ_S3_SNS_DDR	51
	=PPDDR_S3_MEMVREF	22
THIS IS 1.5V RAIL	=PPVDDQ_S3_MEM_A	23 24
	=PPVDDQ_S3_MEM_B	25 26
	=PPVDDQ_S3_MEMRESET	21
	=PPVDDQ_S3_LDO_DDRVTT	66

S0 Rails
Enabled when system is in run

101 PP12V_S0 (MAKE_BASE=TRUE)	PP12V_S0_FET	75
	=PP12V_S0_AUDIO_SPKRAMP	56 57
	=PP12V_S0_FAN	53
	=PP12V_S0_SNS_GPUCORE_R	50
	=PP12V_S0_LCD	42
	=PP12V_S0_REG_CPUVCC_S0	64
	=PP12V_S0_REG_P1V05_S0	68
	=PP12V_S0_PWRCTL	75
	=PP12V_S0_SNS_FBVDDQ_R	50
	=PP12V_S0_HDD	36
101 PP12V_S0_GPUCORE (MAKE_BASE=TRUE)	PP12V_S0_SNS_GPUCORE	50
	=PP12V_S0_REG_GPUCORE	69
101 PPHDD12_S0 (MAKE_BASE=TRUE)	PP12V_S0_HDD_FET	36
	=PP12V_S0_HDD_SNS_R	50
101 PP12V_S0_HDD (MAKE_BASE=TRUE)	PP12V_S0_HDD_SNS	50
	=PP12V_S0_HDD_PWR	36
101 PP12V_S0_BLC (MAKE_BASE=TRUE)	PP12V_S0_BLC_FET	75
	=PP12V_S0_BLC	74
101 PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)	PP12V_S0_SNS_FBVDDQ	50
	=PP12V_S0_REG_FBVDDQ	68
101 PP5V_S0 (MAKE_BASE=TRUE)	PP5V_S0_FET	75
	=PP5V_S0_AUDIO	54 61
	=PP5V_S0_BLC	74
	=PP5V_S0_ISENSE	50
	=PP5V_S0_LPCPLUS	48
	=PP5V_S0_REG_CPUVCC_S0	63 64 65
	=PP5V_S0_REG_FBVDDQ	68
	=PP5V_S0_REG_P1V05	68
	=PP5V_S0_HDD	36
	=PP5V_S0_VRD	69
101 PPHDD_S0 (MAKE_BASE=TRUE)	PP5V_S0_HDD_FET	36
	=PPHDD_S0_SNS_R	50
101 PP5V_S0_HDD (MAKE_BASE=TRUE)	PPHDD_S0_SNS	50
	=PP5V_S0_HDD_PWR	36
101 PP3V3_S0 (MAKE_BASE=TRUE)	PP3V3_S0_FET	75
	=PP3V3_S0_GPU_IFPX_PLLVDD	85
	=PP3V3_S0_GPU_MISC	85
	=PP3V3_S0_GPU_VDD33	85
	=PP3V3_S0_AUDIO	40 54 56 57 60
	=PP3V3_S0_AUDIO_DIG	58
	=PP3V3_S0_BLC	72
	=PP3V3_S0_DP	33 42 49
	=PP3V3_S0_ENET	37
	=PP3V3_S0_FAN	53
	=PP3V3_S0_GPU	69 85
	=PP3V3_S0_INTDPMUX	43
	=PP3V3_S0_LED	3
	=PP3V3_S0_LED_SATA	35
	=PP3V3_S0_MEM_A_SPD	23 24
	=PP3V3_S0_MEM_B_SPD	25 26
	=PP3V3_S0_P3V3TBTFET	30
	=PP3V3_S0_PCH	19
	=PP3V3_S0_PCH_VCC3_3_GPIO	11 12 13 14 15 17
	=PP3V3_S0_PCH_VCC3_3_THRM	15 17
	=PP3V3_S0_PCH_VCCCLK3_3	15 17
	=PP3V3_S0_PCH_VCC3_3_HVCMOS	15 17
	=PP3V3_S0_PCH_VCC_FUSE	15 17
	=PP3V3_S0_PWRCTL	75
	=PP3V3_S0_RSTBUF	20
	=PP3V3_S0_SDCARD	39
	=PP3V3_S0_SENSE	36 50 51 52
	=PP3V3_S0_SMBUS	49
	=PP3V3_S0_SMBUS_SMC_0	49
	=PP3V3_S0_SMBUS_SMC_1	49
	=PP3V3_S0_SMBUS_SMC_3	49
	=PP3V3_S0_SMC	47 84
	=PP3V3_S0_TBTPWRCTL	30
	=PP3V3_S0_VRD	62 63 68 69
	=PP3V3_S0_PCH_GPIO	30
	=PP3V3_S0_PCH_VCC3_3_USB	15 17
	=PPSSD_S0_SNS_R	51
101 PPSSD_S0 (MAKE_BASE=TRUE)	PPSSD_S0_SNS	51
	=PP3V3_S0_SSD	35
99 PP1V5_S0 (MAKE_BASE=TRUE)	PP1V5_S0_FET	75
	=PP1V5_S0_SNS_R	51
99 PP1V5_S0_PCH (MAKE_BASE=TRUE)	PP1V5_S0_SNS	51
	=PP1V5_S0_CPU_MEM	6 8 10
	=PP1V5_S0_AUD_DIG	54
	=PP1V5_S0_PCH_VCCVRM	17
	=PP1V5_S0_PCH_RCOMP	12 13
	=PP1V5_S0_PCH_SATA	11
	=PP1V5_S0_PCH_CLK	11 19
	=PP1V5_S0_DP	43
99 PPDDRVTT_S0 (MAKE_BASE=TRUE)	PPDDRVTT_S0_LDO	66
	=PPDDRVTT_S0_CLAMP	21
	=PPDDRVTT_S0_MEM_A	23 24
	=PPDDRVTT_S0_MEM_B	25 26
100 PPCPUVCC_S0_CPU (MAKE_BASE=TRUE)	PPCPUVCC_S0_REG	64 65
	=PPCPUVCC_S0_CPU	6 8 10 50 63

GPU Rails (S0)
Enabled when system is in run

105 PPVCORE_S0_GPU (MAKE_BASE=TRUE)	PPGPUCORE_S0_REG	70 71
	=PPVCORE_S0_GPU	85
	=PPGPUCORE_S0_SNS	50
105 PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)	PP1V5R1V35_S0_GPU_REG	68
	=PP1V35_S0_GPU_FBVDDQ	85
99 PP1V05_S0 (MAKE_BASE=TRUE)	PP1V05_S0_REG	68
	=PP1V05_S0_P1V05TBTFET	30
	=PP1V05_S0_PCH_VCC	15 17
	=PP1V05_S0_PCH_VCCCLK_CLK100	15 17
	=PP1V05_S0_PCH_VCCASW	15 17
	=PP1V05_S0_PCH_VCC_CLK	17
	=PP1V05_S0_PCH_VCCIO_FDI	15 17
	=PP1V05_S0_PCH_VCCCLK_SSC	15 17
	=PP1V05_S0_PCH_VCCUSBPLL	15 17
	=PP1V05_S0_PCH_VCCIO	15 17
	=PP1V05_S0_PCH_VCCCLK_SSC100	15 17
	=PP1V05_S0_PCH_VCCCLK_CLK135	15 17
	=PP1V05_S0_PCH_VCCIO_USB2	15 17
	=PP1V05_S0_PCH_V_PROC_IO	14 15 17
	=PP1V05_S0_SNS	50
	=PP1V05_S0_SMC	47
	=PP1V05_S0_XDP	18
	=PP1V05_S0_GPU_IFPCD_IOVDD	85
	=PP1V05_S0_GPU_IFPEF_IOVDD	85
	=PP1V05_S0_GPU_PEX_IOVDD	85
	=PP1V05_S0_GPU_PEX_PLLVDD	85

Thunderbolt Rails (S0)
Enabled when Thunderbolt cable is plugged in

101 PP3V3_TBTLC (MAKE_BASE=TRUE)	=PP3V3_TBTLC_FET	30
	=PP3V3_TBT_PCH_GPIO	20
	=PP3V3_TBTLC_RTR	28 29 30
	=PPVDDIO_TBT_CLK	19
99 30 PP1V05_TBTLC (MAKE_BASE=TRUE)	=PP1V05_TBTLC_FET	30
	=PP1V05_TBTLC_RTR	29
99 PP1V05_TBTCIO (MAKE_BASE=TRUE)	=PP1V05_TBTCIO_FET	30
	=PP1V05_TBTCIO_RTR	29

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
Power Connectors/Aliases

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 100 OF 127
SHEET 87 OF 106

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PEG aliases

93 78 PEG_D2R_N<0..15> —— =PEG_D2R_N<15..0> 5
MAKE_BASE=TRUE
93 78 PEG_D2R_P<0..15> —— =PEG_D2R_P<15..0> 5
MAKE_BASE=TRUE
93 78 PEG_R2D_C_N<0..15> —— =PEG_R2D_C_N<15..0> 5
MAKE_BASE=TRUE
93 78 PEG_R2D_C_P<0..15> —— =PEG_R2D_C_P<15..0> 5
MAKE_BASE=TRUE

DDI/FDI ALIASES

I64
5 TP_DP_IG_B_MLN<0..3> —— NC_DP_IG_B_MLN<0..3>
MAKE_BASE=TRUE
5 TP_DP_IG_B_MLP<0..3> —— NC_DP_IG_B_MLP<0..3>
MAKE_BASE=TRUE
5 TP_DP_IG_C_MLN<0..3> —— NC_DP_IG_C_MLN<0..3>
MAKE_BASE=TRUE
5 TP_DP_IG_C_MLP<0..3> —— NC_DP_IG_C_MLP<0..3>
MAKE_BASE=TRUE
5 TP_DP_IG_D_MLN<0..3> —— NC_DP_IG_D_MLN<0..3>
MAKE_BASE=TRUE
5 TP_DP_IG_D_MLP<0..3> —— NC_DP_IG_D_MLP<0..3>
MAKE_BASE=TRUE

GPU ALIASES

84 78 GPU_RESET_L —— TP_GPU_RESET_L 20
MAKE_BASE=TRUE

MEMORY PGOOD

21 =PM_PGOOD_MEM_S0 —— PM_PGOOD_FET_REG_P1V5_S0 75 76
MAKE_BASE=TRUE

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
Signal Aliases

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DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 102 OF 127
SHEET 88 OF 106

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CPU Reserved

95 18 6 CPU_CFG<15..12> — TP_CPU_CFG<15..12>
MAKE_BASE=TRUE

CPU Memory

7 TP_MEM_A_DQS_N<8> — NC_MEM_A_DQSNX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_A_DQS_P<8> — NC_MEM_A_DQSPX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_B_DQS_N<8> — NC_MEM_B_DQSNX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

7 TP_MEM_B_DQS_P<8> — NC_MEM_B_DQSPX<8>
MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCIe

11 TP_PCIE_CLK100M_PE4N — NC_PCIE_CLK100M_PE4NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE4P — NC_PCIE_CLK100M_PE4PX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE5N — NC_PCIE_CLK100M_PE5NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE5P — NC_PCIE_CLK100M_PE5PX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE7N — NC_PCIE_CLK100M_PE7NX
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCIE_CLK100M_PE7P — NC_PCIE_CLK100M_PE7PX
MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

11 TP_PCH_GPIO64_CLKOUTFLEX0 — NC_PCH_GPIO64_CLKOUTFLEX0
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO65_CLKOUTFLEX1 — NC_PCH_GPIO65_CLKOUTFLEX1
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO66_CLKOUTFLEX2 — NC_PCH_GPIO66_CLKOUTFLEX2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCH_GPIO67_CLKOUTFLEX3 — NC_PCH_GPIO67_CLKOUTFLEX3
MAKE_BASE=TRUE NO_TEST=TRUE

TP_ITPXDP_CLK100MP — ITPXDP_CLK100M_P 11 95
MAKE_BASE=TRUE NO_TEST=TRUE

TP_ITPXDP_CLK100MN — ITPXDP_CLK100M_N 11 95
MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

13 TP_LPC_DREQ0_L — NC_LPC_DREQ0_L
MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

11 TP_HDA_SDIN1 — NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_HDA_SDIN2 — NC_HDA_SDIN2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_HDA_SDIN3 — NC_HDA_SDIN3
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCI_CLK33M_OUT2 — NC_PCI_CLK33M_OUT2
MAKE_BASE=TRUE NO_TEST=TRUE

11 TP_PCI_CLK33M_OUT3 — NC_PCI_CLK33M_OUT3
MAKE_BASE=TRUE NO_TEST=TRUE

POWER SEQUENCING

76 PM_EN_FET_P1V35_S0 — NC_PM_EN_FET_P1V35_S0
MAKE_BASE=TRUE NO_TEST=TRUE

76 PM_PGOOD_FET_P1V35_S0 — NC_PGOOD_FET_P1V35_S0
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
Unused Signal Aliases

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DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 104 OF 127
SHEET 89 OF 106

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SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE

Functional / ICT Test

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

PAGE 105 OF 127

SHEET 90 OF 106

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J17 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

Top	Signal	0.5 oz (Cu plated)
	Prepreg	0.071 MM
2	Plane	1 oz
	Core	0.101 MM
3	Signal	0.5 oz
	Prepreg	0.115 MM
4	Plane	1 oz
	Core	0.076 MM
5	Signal	0.5 oz
	Prepreg	0.380 MM
6	Plane	1 oz
	Core	0.076 MM
7	Plane	1 oz
	Prepreg	0.380 MM
8	Signal	0.5 oz
	Core	0.076 MM
9	Plane	1 oz
	Prepreg	0.115 MM
10	Signal	0.5 oz
	Core	0.101 MM
11	Plane	1 oz
	Prepreg	0.071 MM
Btm	Signal	0.5 oz (Cu plated)

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
J17 RULE DEFINITIONS

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF
DDR_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D
DDR_COMP_PHY	*	DDR_COMP

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2.5:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?
DDR_COMP_ISO	*	0.381 MM	?

Main Segment Min Spacing Rules (mils) (Shark Bay PDG, Intel Doc# 486712)

Table	Trace	Design (diff)	Iso	Design	Comments
4-2	4		15	19.69	CLK trace spacing controlled by =68_OHM_DIFF
4-3	8	9.84	12	13.78	
4-4	6	7.87	12	13.78	
4-5	8.5	7.87	12	11.81	DQ or DQS to other signals not in the same bytelane (but not ch)
					DQ to DQ in the same bytelane of the same channel
			10	11.81	DQ to DQS in the same bytelane of the same channel
			12	11.81	DQ or DQS in different bytelanes of the same channel
			25	25.59	DQ or DQS in different channels
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_COMP	*	*	DDR_COMP_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
I17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	7 23
I17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	7 23
I25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	7 24
I25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	7 24
I18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	7 23
I18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	7 23
I18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	7 23
I24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	7 24
I24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	7 24
I24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	7 24
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	7 23 24
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	7 23 24
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	7 23 24
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	7 23 24
I18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	7 23 24
I18 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	7 27
I18 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	7 27
I19 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	7 27
I19 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	7 27
I19 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	7 27
I19 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	7 27
I19 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	7 27
I19 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	7 27
I19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	7 27
I19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	7 27
I19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	7 27
I19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	7 27
I20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	7 27
I20 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	7 27
I20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	7 27
I20 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	7 27
I20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	7 27
I20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	7 27
I20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	7 27
I20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	7 27
I20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	7 27
I20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	7 27
I21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	7 27
I21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	7 27
Channel B				
I21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	7 25
I21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	7 25
I25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	7 26
I25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	7 26
I21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	7 25
I21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	7 25
I21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	7 25
I25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	7 26
I25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	7 26
I25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	7 26
I21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	7 25 26
I21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	7 25 26
I21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	7 25 26
I22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	7 25 26
I22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	7 25 26
I22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	7 27
I22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	7 27
I22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	7 27
I22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	7 27
I22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	7 27
I22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	7 27
I22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	7 27
I22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	7 27
I23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	7 27
I23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	7 27
I23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	7 27
I23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	7 27
I23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	7 27
I23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	7 27
I23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	7 27
I23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	7 27
I23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	7 27
I23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	7 27
I24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	7 27
I24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	7 27
I24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	7 27
I24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	7 27
I24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	7 27
I24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	7 27
Reset				
I24	DDR_50S		MEM_RESET_L	21 23 24 25 26
SM COMP				
I28	DDR_COMP_PHY	DDR_COMP	CPU_SM_RCOMP<0..2>	6

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
DDR3 Constraints

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PAGE 111 OF 127
SHEET 92 OF 106

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PCI Express/DMI

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE3_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
PEG_R2D	PEG_R2D	*	PEG_SAME_DIR
PEG_D2R	PEG_D2R	*	PEG_SAME_DIR
PEG_D2R	PEG_R2D	*	PEG_ALT_DIR
PEG_D2R	*	*	PEG_ISO
PEG_R2D	*	*	PEG_ISO

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PEG_SAME_DIR	*	=3.5X_DIELECTRIC	?
PEG_ALT_DIR	*	=7X_DIELECTRIC	?
PEG_ISO	*	=4:1_SPACING	?

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
1440 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<15>	78
1441 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<15>	78
1442	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<15>	78 88
1443	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<15>	78 88
1444 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<15>	78 88
1445 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<15>	78 88
1446	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<15>	78
1447	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<15>	78
1448 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<14>	78
1449 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<14>	78
1450	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<14>	78 88
1451	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<14>	78 88
1452 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<14>	78 88
1453 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<14>	78 88
1454	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<14>	78
1455	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<14>	78
1456 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<13>	78
1457 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<13>	78
1458	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<13>	78 88
1459	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<13>	78 88
1460 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<13>	78 88
1461 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<13>	78 88
1462	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<13>	78
1463	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<13>	78
1464 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<12>	78
1465 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<12>	78
1466	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<12>	78 88
1467	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<12>	78 88
1468 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<12>	78 88
1469 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<12>	78 88
1470	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<12>	78
1471	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<12>	78
1472 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<11>	78
1473 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<11>	78
1474	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<11>	78 88
1475	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<11>	78 88
1476 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<11>	78 88
1477 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<11>	78 88
1478	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<11>	78
1479	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<11>	78
1480 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<10>	78
1481 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<10>	78
1482	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<10>	78 88
1483	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<10>	78 88
1484 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<10>	78 88
1485 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<10>	78 88
1486	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<10>	78
1487	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<10>	78
1488 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<9>	78
1489 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<9>	78
1490	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<9>	78 88
1491	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<9>	78 88
1492 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<9>	78 88
1493 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<9>	78 88
1494	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<9>	78
1495	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<9>	78
1496 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<8>	78
1497 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<8>	78
1498	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<8>	78 88
1499	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<8>	78 88
1500 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<8>	78 88
1501 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<8>	78 88
1502	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<8>	78
1503	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<8>	78

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
1504 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<7>	78
1505 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<7>	78
1506	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<7>	78 88
1507	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<7>	78 88
1508 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<7>	78 88
1509 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<7>	78 88
1510	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<7>	78
1511	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<7>	78
1512 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<6>	78
1513 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<6>	78
1514	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<6>	78 88
1515	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<6>	78 88
1516 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<6>	78 88
1517 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<6>	78 88
1518	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<6>	78
1519	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<6>	78
1520 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<5>	78
1521 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<5>	78
1522	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<5>	78 88
1523	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<5>	78 88
1524 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<5>	78 88
1525 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<5>	78 88
1526	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<5>	78
1527	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<5>	78
1528 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<4>	78
1529 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<4>	78
1530	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<4>	78 88
1531	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<4>	78 88
1532 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<4>	78 88
1533 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<4>	78 88
1534	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<4>	78
1535	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<4>	78
1536 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<3>	78
1537 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<3>	78
1538	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<3>	78 88
1539	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<3>	78 88
1540 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<3>	78 88
1541 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<3>	78 88
1542	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<3>	78
1543	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<3>	78
1544 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_P<2>	78
1545 PCIE_GEN3_R2D	PCIE3_PHY	PEG_R2D	PEG_R2D_N<2>	78
1546	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<2>	78 88
1547	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<2>	78 88
1548 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_P<2>	78 88
1549 PCIE_GEN3_D2R_RVSD	PCIE3_PHY	PEG_D2R	PEG_D2R_N<2>	78 88
1550	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<2>	78
1551	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<2>	78
1552 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<1>	78
1553 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<1>	78
1554	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<1>	78 88
1555	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<1>	78 88
1556 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<1>	78 88
1557 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<1>	78 88
1558	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<1>	78
1559	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<1>	78
1560 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_P<0>	78
1561 PCIE_GEN3_R2D_RVSD	PCIE3_PHY	PEG_R2D	PEG_R2D_N<0>	78
1562	PCIE3_PHY	PEG_R2D	PEG_R2D_C_P<0>	78 88
1563	PCIE3_PHY	PEG_R2D	PEG_R2D_C_N<0>	78 88
1564 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_P<0>	78 88
1565 PCIE_GEN3_D2R	PCIE3_PHY	PEG_D2R	PEG_D2R_N<0>	78 88
1566	PCIE3_PHY	PEG_D2R	PEG_D2R_C_P<0>	78
1567	PCIE3_PHY	PEG_D2R	PEG_D2R_C_N<0>	78

CPU PCIe Clocks

1568 PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P	11 78
1569 PEG_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N	11 78

CPU PCIe Compensation

1570	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_RCOMP	5

CPU eDP Compensation

1571	COMP_PCIE_PHY	COMP_PCIE	CPU_EDP_RCOMP	5

SYNC_MASTER=J17_NICK SYNC_DATE=12/14/2012

PAGE TITLE
CPU PCIe Constraints

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 112 OF 127
SHEET 93 OF 106

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D
COMP_DMI_PHY	*	DMI_COMP

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=7X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

DMI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
DMI_SAME_DIR	*	=4X_DIELECTRIC	?
DMI_ALT_DIR	*	=5X_DIELECTRIC	?
DMI_ISO	*	=4X_DIELECTRIC	?

DMI x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_N2S	DMI_N2S	*	DMI_SAME_DIR
DMI_S2N	DMI_S2N	*	DMI_SAME_DIR
DMI_N2S	DMI_S2N	*	DMI_ALT_DIR
DMI_N2S	*	*	DMI_ISO
DMI_S2N	*	*	DMI_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_COMP	*	Y	0.2032 MM	0.2032 MM	3 MM	=STANDARD	=STANDARD

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
1832 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3..0>	28
1833 PCIE_GEN2_R2D	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3..0>	28
1834	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3..0>	13 28
1835	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3..0>	13 28
1836 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3..0>	13 28
1837 PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3..0>	13 28
1838	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3..0>	28
1839	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3..0>	28
1840 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
1841 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
x1 AirPort				
1842 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	34
1843 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	34
1844	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	13 34
1845	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	13 34
1846 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	13 34
1847 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	13 34
1848 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	11 34
1849 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	11 34
x1 Caesar IV				
1850 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	37
1851 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	37
1852	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	13 37
1853	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	13 37
1854 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	13 37
1855 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	13 37
1856	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	37
1857	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	37
1858 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	11 37
1859 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	11 37
x2 SSD				
1860 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	11 35
1861 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	11 35
PCH PCIE Compensation				
1862	COMP_DMI_PHY	COMP_PCIE	PCH_PCIE_RCOMP	13

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
1863 DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_P<3..0>	5 12
1864 DMI_N2S	PCIE_PHY	DMI_N2S	DMI_N2S_N<3..0>	5 12
1865 DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_P<3..0>	5 12
1866 DMI_S2N	PCIE_PHY	DMI_S2N	DMI_S2N_N<3..0>	5 12
1867 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	6 11
1868 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	6 11
DMI Compensation				
1869	COMP_DMI_PHY	COMP_PCIE	PCH_DMI_RCOMP	12

CPU DP REF CLK

Electrical Contraint Set	Physical	Spacing		
CPU DP REF CLK				
1870 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
1871 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
1872 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
1873 CPU_CLK135_PLL	PCIE_PHY	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11

SYNC_MASTER=J17 ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
PCH PCIe/DMI Constaints

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

PAGE 113 OF 127

SHEET 94 OF 106

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_85D
COMP_SATA_PHY	*	SATA_50S
SATA_PHY_90	*	SATA_90D

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

FDI

FDI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FDI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI	*	Y	0.25 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FDI_SE_PHY	*	FDI_50S
COMP_FDI_PHY	*	COMP_FDI

FDI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FDI_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FDI	*	*	FDI_ISO
COMP_FDI	*	*	COMP_FDI_ISO

FDI Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Imp	Design	Iso	Design	Comments
6-1/6-2	85	85	12	11.81	FDI main length

FDI Compensation Rules (mils)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

SATA

Electrical Contraint Set		Physical	Spacing		
PCH SATA Port 0 (HDD)					
180	SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_P	35
182	SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_N	35
188		SATA_PHY_90	SATA	SATA_HDD_R2D_C_P	11 35
189		SATA_PHY_90	SATA	SATA_HDD_R2D_C_N	11 35
184	SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_P	11 35
185	SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_N	11 35
191		SATA_PHY_90	SATA	SATA_HDD_D2R_C_P	35
193		SATA_PHY_90	SATA	SATA_HDD_D2R_C_N	35
PCH SATA Port 1 (SSD)					
186	SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_P<0..1>	11 35
198	SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_N<0..1>	11 35
1414	SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_P<0..1>	35
1416	SATA_SSD_R2D	SATA_PHY	SATA	SSD_R2D_C_N<0..1>	35
1418	SATA_SSD_D2R	SATA_PHY	SATA	SSD_D2R_P<0..1>	11 35
1420	SATA_SSD_D2R	SATA_PHY	SATA	SSD_D2R_N<0..1>	11 35
PCH SATA Compensation					
1424		COMP_SATA_PHY	COMP_SATA	PCH_SATA_RCOMP	11

FDI

Electrical Contraint Set		Physical	Spacing		
FDI					
1412		FDI_SE_PHY	FDI	FDI_CSYNC	5 12
1414		FDI_SE_PHY	FDI	FDI_INT	5 12
FDI Compensation					
1416		COMP_FDI_PHY	COMP_FDI	PCH_FDI_RCOMP	12

XDP

Electrical Contraint Set		Physical	Spacing		
CPU XDP					
137		XDP_PHY	XDP	XDP_BPM_L<7..0>	6 18
138		XDP_PHY	XDP	CPU_CFG<17..0>	6 18 89
168	ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	
140	ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	
141		CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	11 89
143		CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	11 89
142		CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	
144		CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	
145		XDP_PHY	CLK_JTAG	XDP_CPU_TCK	6 18
146		XDP_PHY	XDP	XDP_CPU_TMS	6 18
147		XDP_PHY	XDP	XDP_CPU_TDI	6 18
148		XDP_PHY	XDP	XDP_CPU_TDO	6 18
PCH XDP					
149		XDP_PHY	CLK_JTAG	XDP_PCH_TCK	11 18
150		XDP_PHY	XDP	XDP_PCH_TMS	11 18
151		XDP_PHY	XDP	XDP_PCH_TDI	11 18
152		XDP_PHY	XDP	XDP_PCH_TDO	11 18

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
SATA/FDI/XDP Constraints

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

PAGE 114 OF 127

SHEET 95 OF 106

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	=2:1_SPACING	?

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI	*	=2:1_SPACING	?

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=1.5:1_SPACING	?
CLK_LPC	*	=2:1_SPACING	?

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=2:1_SPACING	?

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
1833	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	11 19
1832	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	11 19

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
1838	LPC_55S	LPC	LPC_AD<3..0>	13 46 48
1839	LPC_55S	LPC	LPC_AD_R<3..0>	13
1836	LPC_55S	LPC	LPC_FRAME_L	13 46 48
1837	LPC_55S	LPC	LPC_FRAME_R_L	13
LPC Clocks				
1835	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 48
1840	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
1841	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	19 46
1842	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	11 19

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
1488	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB	11 19
1489	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_SB_R	11
PCH RTC 32K				
1844	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	11 19
1845	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	11 19
1852	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	19
SMC 32K				
1846	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	12 47
1958	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	46 47

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
1479	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	19
1480	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	19
1481	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	19
25M Reference Clocks				
1482	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET	19 37
1483	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_ENET_R	19
1486	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT	19 28
1487	CLK_PCH_55S	CLK_PCH	SYSCLK_CLK25M_TBT_R	28

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
1850	HDA_55S	HDA	HDA_BIT_CLK	11 54
1851	HDA_55S	HDA	HDA_BIT_CLK_R	11
1860	HDA_55S	HDA	HDA_RST_L	11 54
1859	HDA_55S	HDA	HDA_RST_R_L	11
1865	HDA_55S	HDA	HDA_SDOUT	11 54
1867	HDA_55S	HDA	HDA_SDOUT_R	11 19
1866	HDA_55S	HDA	HDA_SYNC	11 54
1868	HDA_55S	HDA	HDA_SYNC_R	11
1869	HDA_55S	HDA	HDA_SDIN0	11 54
1860	HDA_55S	HDA	AUD_SDI_R	54
SPDIF				
1872		HDA	AUD_SPDIF_CHIP	54
1873		HDA	AUD_SPDIF_OUT	54 58

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
1891	SPI_50S	SPI	SPI_CLK_R	13 48
1892	SPI_50S	SPI	SPI_CLK	48
1893	SPI_50S	SPI	SPI_ALT_CLK	48
1640	SPI_50S	SPI	SPI_SMC_CLK	46 48
1639	SPI_50S	SPI	SPI_MLB_CLK	48
1894	SPI_50S	SPI	SPI_CS0_R_L	13 48
1895	SPI_50S	SPI	SPI_CS0_L	48
1896	SPI_50S	SPI	SPI_ALT_CS_L	48
1642	SPI_50S	SPI	SPI_SMC_CS_L	46 48
1897	SPI_50S	SPI	SPI_MLB_CS_L	48
1898	SPI_50S	SPI	SPI_MOSI_R	13 48
1860	SPI_50S	SPI	SPI_MOSI	48
1861	SPI_50S	SPI	SPI_ALT_MOSI	48
1641	SPI_50S	SPI	SPI_SMC_MOSI	46 48
1638	SPI_50S	SPI	SPI_MLB_MOSI	48
1862	SPI_50S	SPI	SPI_MISO	13 48
1863	SPI_50S	SPI	SPI_ALT_MISO	48
1643	SPI_50S	SPI	SPI_SMC_MISO	46 48
1644	SPI_50S	SPI	SPI_MLB_MISO	48
1899	SPI_50S	SPI	SPIROM_USE_MLB	14 48

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
PCH and BR Constraints

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

PAGE 115 OF 127

SHEET 96 OF 106

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions

Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints

Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor's SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor's SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set		Physical	Spacing		
External Port A (J4600)					
1820	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P	44
1822	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N	44
1893		USB3_PHY	USB3	USB3_EXTA_RX_F_P	13 44
1892		USB3_PHY	USB3	USB3_EXTA_RX_F_N	13 44
1811	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P	13 44
1814	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N	13 44
1816		USB3_PHY	USB3	USB3_EXTA_TX_F_P	44
1816		USB3_PHY	USB3	USB3_EXTA_TX_F_N	44
1819		USB3_PHY	USB3	USB3_EXTA_TX_C_P	44
1819		USB3_PHY	USB3	USB3_EXTA_TX_C_N	44
1817	USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_P	13 44
1818	USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_0_N	13 44
1816		USB2_PHY	USB2	USB2_EXTA_MUXED_P	44
1812		USB2_PHY	USB2	USB2_EXTA_MUXED_N	44
1893		USB2_PHY	USB2	USB2_EXTA_P	44
1894		USB2_PHY	USB2	USB2_EXTA_N	44
External Port B (J4610)					
1821	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P	44
1823	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N	44
1823		USB3_PHY	USB3	USB3_EXTB_RX_F_P	13 44
1824		USB3_PHY	USB3	USB3_EXTB_RX_F_N	13 44
1826	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P	13 44
1822	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N	13 44
1826		USB3_PHY	USB3	USB3_EXTB_TX_F_P	44
1826		USB3_PHY	USB3	USB3_EXTB_TX_F_N	44
1849		USB3_PHY	USB3	USB3_EXTB_TX_C_P	44
1849		USB3_PHY	USB3	USB3_EXTB_TX_C_N	44
1829	USB2_CONN	USB2_PHY	USB2	USB_EXTB_8_P	13 44
1830	USB2_CONN	USB2_PHY	USB2	USB_EXTB_8_N	13 44
1825		USB2_PHY	USB2	USB2_EXTB_P	44
1835		USB2_PHY	USB2	USB2_EXTB_N	44
External Port C (J4700)					
1837	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P	45
1839	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N	45
1838		USB3_PHY	USB3	USB3_EXTC_RX_F_P	13 45
1844		USB3_PHY	USB3	USB3_EXTC_RX_F_N	13 45
1841	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P	13 45
1842	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N	13 45
1844		USB3_PHY	USB3	USB3_EXTC_TX_F_P	45
1844		USB3_PHY	USB3	USB3_EXTC_TX_F_N	45
1850		USB3_PHY	USB3	USB3_EXTC_TX_C_P	45
1850		USB3_PHY	USB3	USB3_EXTC_TX_C_N	45
1843	USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_P	13 45
1845	USB2_CONN	USB2_PHY	USB2	USB_EXTC_1_N	13 45
1850		USB2_PHY	USB2	USB2_EXTC_P	45
1852		USB2_PHY	USB2	USB2_EXTC_N	45
External Port D (J4710)					
1855	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P	45
1856	USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N	45
1856		USB3_PHY	USB3	USB3_EXTD_RX_F_P	13 45
1856		USB3_PHY	USB3	USB3_EXTD_RX_F_N	13 45
1857	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P	13 45
1858	USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N	13 45
1860		USB3_PHY	USB3	USB3_EXTD_TX_F_P	45
1860		USB3_PHY	USB3	USB3_EXTD_TX_F_N	45
1859		USB3_PHY	USB3	USB3_EXTD_TX_C_P	45
1860		USB3_PHY	USB3	USB3_EXTD_TX_C_N	45
1862	USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_P	13 45
1861	USB2_CONN	USB2_PHY	USB2	USB_EXTD_9_N	13 45
1860		USB2_PHY	USB2	USB2_EXTD_P	45
1860		USB2_PHY	USB2	USB2_EXTD_N	45
Camera (J3510)					
1874	USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_P	13 40
1876	USB2_CONN_TNT	USB2_PHY	USB2	USB_CAMERA_N	13 40
PCH USB Compensation					
1882		PCH_55S	COMP_PCH	PCH_USB_RBIAS	13

RMH Love

Electrical Contraint Set		Physical	Spacing		
1408	USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_P	13 34
1410	USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_N	13 34
1506	USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_P	34
1506	USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_N	34

Et tu Brute?

Electrical Contraint Set		Physical	Spacing		
Ethernet					
1476	ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>	37 38
1475	ENET_MDI	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>	37 38
1476		ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>	38
1477		ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>	38
1519			ENET_TRANS	ENETCONN_MCT0	38
1520			ENET_TRANS	ENETCONN_MCT1	38
1524			ENET_TRANS	ENETCONN_MCT2	38
1522			ENET_TRANS	ENETCONN_MCT3	38
1523			ENET_TRANS	ENETCONN_MCT_BS	38
1475		ENET_COMP_PHY	COMP_ENET	ENET_RDAC	37
SD					
1479	SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0>	37
1480		SD_PHY	SD	SDCONN_DATA<7..0>	37 39
1515		SD_PHY	SD	SDCONN_DATA_R <7..0>	
1481	SD_CMD	SD_PHY	SD	ENET_SD_CMD	37
1482		SD_PHY	SD	SDCONN_CMD	37 39
1516		SD_PHY	SD	SDCONN_CMD_R	
1483	SD_CLK	SD_PHY	SD	ENET_SD_CLK	37
1484		SD_PHY	SD	SDCONN_CLK	37 39
1485		SD_PHY	SD	SDCONN_CLK_R	39
1486		SD_PHY	SD	ENET_MEDIA_SENSE	11 37
1488		SD_PHY	SD	ENET_SD_DETECT_L	37 39
CIV SPI					
1489		CIV_SPI	SPI	ENET_SCLK	37
1488		CIV_SPI	SPI	ENET_MISO	37
1492		CIV_SPI	SPI	ENET_MOSI	37
1491		CIV_SPI	SPI	ENET_CS_L	37

Camera Processor-Camera Sensor I/F

Electrical Contraint Set		Physical	Spacing		
1589	SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	40
1590	SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	40
1594	SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	40
1595	SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	40
1597		SPI_50S	SPI	CAM_SF_CLK	40
1598		SPI_50S	SPI	CAM_SF_CLK_R	40
1599		SPI_50S	SPI	CAM_SF_DIN	40
1516		SPI_50S	SPI	CAM_SF_DIN_R	40
1511		SPI_50S	SPI	CAM_SF_CS_L	40
1513		SPI_50S	SPI	CAM_SF_WP_L	40
1512		SPI_50S	SPI	CAM_SF_DOUT	40
1514		SPI_50S	SPI	CAM_SF_DOUT_R	40
1517		SMB_PHY	SMB	I2C_CAMSENSOR_SDA	40
1518		SMB_PHY	SMB	I2C_CAMSENSOR_SCL	40

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
USB/Ethernet/SD Constraints

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 116 OF 127
SHEET 97 OF 106

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=1.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMC Generic Control Line Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMC_ISO	*	=1:1_SPACING	?
SMC_3xISO	*	=3:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMC_CTRL	*	*	SMC_ISO
SMC_3XCTRL	*	*	SMC_3xISO

SMC Generic Control Line Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMC_GEN	*	SMC_50S

Current/Voltage Sense

Electrical Contraint Set		Physical	Spacing		
Common					
I3			SENSE	GND_SMC_AVSS	46 47 50 51
12V S5 (System Total)					
I4	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	50
I5	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	50
I6			SENSE	ISNS_P12VG3H_R	50 106
I7			SENSE	ISNS_P12VG3H	47 50
I8			SENSE	VSNS_P12VG3H	47 50
12V S0 (GPU Core)					
I22	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_P	50
I23	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_GPUCORE_N	50
I24			SENSE	ISNS_P12VS0_GPUCORE_R	50
I25			SENSE	ISNS_P12VS0_GPUCORE	47 50
I26			SENSE	VSNS_P12VS0_GPUCORE	47 50
HDD					
I80	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_P	50
I82	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_HDD_N	50
I81			SENSE	ISNS_HDDS0_R	50
I83			SENSE	ISNS_HDDS0	47 50
I84			SENSE	VSNS_HDDS0	47 50
I125	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_HDD_P	50
I126	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_HDD_N	50
I127			SENSE	ISNS_P12VS0_HDD_R	50 106
I128			SENSE	ISNS_P12VS0_HDD	47 50
SSD					
I85	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	51
I87	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	51
I86			SENSE	ISNS_SSDS0_R	51
I88			SENSE	ISNS_SSDS0	47 51
I89			SENSE	VSNS_P3V3S5	47 51
GPU Core (alternate low side sense)					
I119	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_GPUCORE_P	
I120	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_GPUCORE_N	
I118			SENSE	ISNS_GPUCORE_ALT	47 50
I129			SENSE	ISNS_GPUCORE_FB	50 106
I122			SENSE	VSNS_GPUCORE_ALT	47 50
VDDQ S3 (DDR)					
I83	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_P	51
I82	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_VDDQS3_DDR_N	51
I85			SENSE	ISNS_VDDQS3_DDR_R	51
I84			SENSE	ISNS_VDDQS3_DDR	47 51
I86			SENSE	VSNS_VDDQS3_DDR	47 51
VDDQ S0 (GPU FBVDDQ)					
I87	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_FBVDDQ_P	50
I88	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VS0_FBVDDQ_N	50
I89			SENSE	ISNS_P12VS0_FBVDDQ_R	50 106
I90			SENSE	ISNS_P12VS0_FBVDDQ	47 50
CPU Core					
I42	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUVCC_P	
I43	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNS_CPUVCC_N	
I44			SENSE	ISNS_CPUVCC_FB	50
I45			SENSE	ISNS_CPUVCC	47 50
I46			SENSE	VSNS_CPUVCC	47 50
PP1V05_S0_PCH					
I510			SENSE	VSNS_P1V05S0_PCH	47 50
PP1V5_S0					
I511	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V5S0_P	51
I513	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V5S0_N	51
I512			SENSE	ISNS_P1V5S0_R	51
I514			SENSE	ISNS_P1V5S0	47 51
I515			SENSE	VSNS_P1V5S0	47 51
Airport					
I102	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P3V3S4_AP_P	50
I103	SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P3V3S4_AP_N	50
I104			SENSE	ISNS_P3V3S4_AP_R	50 106
I105			SENSE	ISNS_P3V3S4_AP	47 50

SMC

Electrical Contraint Set		Physical	Spacing		
SMC					
H1		CLK_XTAL	XTAL	SMC_XTAL	46 47
H2		CLK_XTAL	XTAL	SMC_EXTAL	46 47
H91		SMC_GEN	SMC_CTRL	SMC_LRESET_L	20 46
H90		SMC_GEN	SMC_CTRL	SMC_RUNTIME_SCI_L	14 46
H92		SMC_GEN	SMC_CTRL	SMC_WAKE_SCI_L	14 46
H93		SMC_GEN	SMC_CTRL	SMC_FAN_0_CTL	46 53
H94		SMC_GEN	SMC_CTRL	SMC_FAN_0_TACH	46 53
H95		CPU_ASYNC_PHY	CPU_ASYNC	SMC_PECI_L	46 47 106
H96		SMC_GEN	SMC_3XCTRL	CPU_PECI	6 14 46 47

SMBus

Electrical Contraint Set		Physical	Spacing		
SMC					
H10		SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	46 49
H9		SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	46 49
H11		SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	46 49
H12		SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	46 49
H13		SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	46 49
H14		SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	46 49
H15		SMB_PHY	SMB	SMBUS_SMC_3_SCL	46 49
H16		SMB_PHY	SMB	SMBUS_SMC_3_SDA	46 49
H19		SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	46 47
H20		SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	46 47
PCH					
H51		SMB_PHY	SMB	SMBUS_PCH_CLK	13 49
H52		SMB_PHY	SMB	SMBUS_PCH_DATA	13 49
H53		SMB_PHY	SMB	SML_PCH_0_CLK	13 49
H54		SMB_PHY	SMB	SML_PCH_0_DATA	13 49
Display TCon					
H55		SMB_PHY	SMB	SMB_DP_TCON_SCL	42 49
H56		SMB_PHY	SMB	SMB_DP_TCON_SDA	42 49

Temperature Sense

Electrical Contraint Set		Physical	Spacing		
EMC1414-1 (Production)					
H67	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P	
H68	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N	
H69	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_P	
H60	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_2_N	
H65	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	52 62
H66	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	52 62
H124		SNS_DIFF_PHY	SENSE	SNS_T1_3_P	
H124		SNS_DIFF_PHY	SENSE	SNS_T1_3_N	
TMP423 (Development)					
H67	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P	
H68	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N	
H69	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P	
H70	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N	
H61	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_P	
H62	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_SKIN_N	
H71	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P	
H72	SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N	
HDD Out-of-Band					
H117			SENSE	SMC_OOB1_D2R_L	36 46
H76			SENSE	SMC_OOB1_R2D_L	46 47
H110			SENSE	SMC_OOB1_D2R_R	36
SSD Out-of-Band					
H77			SENSE	SMC_OOB2_R2D_L	35 47
H78			SENSE	SMC_OOB2_D2R_L	35 47

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
SMBus/Sensor Constraints

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

PAGE 117 OF 127

SHEET 98 OF 106

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

PCH/GPU/TBT 1.05V S0

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
	Input Bus							
I1		POWER	POWER	5V			REG_VCC_U7700	68
	Local Ground							
I3		GND	GND	0V			AGND_P1V05S0	68
	1.05V S0							
I5		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	68
I4		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	68
I7		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	68
I6		VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC	68
I8		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	68
I9		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	68
I10		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0	68
I12		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0	68
I11		VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	68
I14		VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	68
I16	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE				SNS_GPU_PEX_IOVDD_P	68 86
I17	VSNS_GPU_P1V05	SNS_DIFF_PHY	SENSE				SNS_GPU_PEX_IOVDD_N	68 86
I15			SENSE				REG_P1V05S0_FB	68
I18			SENSE				REG_P1V05S0_RTN	68
I21		VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	68
I20		VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	68
	Output Bus							
I22		POWER	POWER	1.05V			PP1V05_S0	87
	FET Switched							
I23		POWER	POWER	1.05V			PP1V05_TBTLC	30 87
I66		POWER	POWER	1.05V			PP1V05_TBTCIO	87

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
	Input Bus						
I44	POWER	POWER	5V			REG_V5IN_U7300	66
	Local Ground						
I45	GND	GND	0V			AGND_VDDQS3	66
	VDDQ S3						
I46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3	66
I47	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L	66
I48	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3	66
I49	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC	66
I50	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3	66
I52	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R	66
I51	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_VDDQS3	66
I53	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3	66
I58	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS	66
I55	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF	66
I56	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN	66
I57	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE	66
I59	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP	66
I62	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	66
I61	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VTTREF	66
	Output Bus						
I65	POWER	POWER	1.5V			PPVDDQ_S3	87
I64	POWER_DDR	POWER_DDR	0.75V			PPDDRVTT_S0	87
	FET Switched						
I63	POWER	POWER	1.5V			PP1V5_S0	87
	Sensed						
I63	POWER	POWER	1.5V			PPVDDQ_S3_DDR	87
I67	POWER	POWER	1.5V			PP1V5_S0_PCH	87

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
VReg Constraints

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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PAGE 118 OF 127

SHEET 99 OF 106

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CPU VCC Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
	POWER	POWER	12V			PP12V_S0_CPUVCC_FLT	63 64 65
	POWER	POWER	5V			REG_VCC_U7000	63
Local Ground							
	GND	GND	0V			AGND_CPU	63 64 65
Phase 1							
	VR_CTL_PHY	VR_CTL				REG_TD_1	64
	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1	63 64
	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1_R	63
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_1	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_1_RC	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_1	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_1	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_1	64
	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_1	64
ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_1_P	63 64
ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_1_N	64
		SENSE				REG_ISENVCC_1_NR	63 64
Phase 2							
	VR_CTL_PHY	VR_CTL				REG_TD_2	64
	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2	63 64
	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2_R	63
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_2	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_2_RC	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_2	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_2	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_2	64
	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_2	64
ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_2_P	63 64
ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_2_N	64
		SENSE				REG_ISENVCC_2_NR	63 64
Phase 3							
	VR_CTL_PHY	VR_CTL				REG_TD_3	64
	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3	63 64
	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_3_R	63
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_3	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_3	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_3_RC	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_3	64
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_3	64
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_3	64
	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_3	64
ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_3_P	63 64
ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_3_N	64
		SENSE				REG_ISENVCC_3_NR	63 64
Phase 4							
	VR_CTL_PHY	VR_CTL				REG_TD_4	65
	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_4	63 65
	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_4_R	63
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_4	65
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_4	65
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUVCC_4_RC	65
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_4	65
	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_4	65
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_4	65
	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_4	65
ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_4_P	63 65
ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENVCC_4_N	65
		SENSE				REG_ISENVCC_4_NR	63 65

CPU VCC Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
ISL6372							
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_DVC	63
	VR_CTL_PHY	VR_CTL				CPUVCC_DVC_RC	63
	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC_2	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP	63
	VR_CTL_PHY	VR_CTL				CPUVCC_COMP_RC	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB	63
	VR_CTL_PHY	VR_CTL				CPUVCC_FB_RC	63
	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_1	63
	VR_CTL_PHY	VR_CTL				CPUVCC_FB_R_2	63
	VR_CTL_PHY	VR_CTL				CPUVCC_PSICOMP_RC	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PSICOMP	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_HFCOMP	63
VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_P	8 63
VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_N	9 63
	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_R_P	63
	SNS_DIFF_PHY	SENSE				CPU_VCCSENSE_R_N	63
	SNS_DIFF_PHY	SENSE	1.8V			SNS_VCC_XW_P	63
	SNS_DIFF_PHY	SENSE	0V			SNS_VCC_XW_N	63
		SENSE				REG_CPUVCC_VSEN	63
		SENSE				REG_CPUVCC_RGND	63
		SENSE				REG_CPUVCC_VIN	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMON	50 63
	VR_CTL_PHY	VR_CTL				CPUVCC_IMON_R	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TM	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_IMX	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NPSI	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FDVID	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_TMX	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_MEMVRSEL	63
	VR_CTL_PHY	VR_CTL				REG_CPUVCC_RSET	63
CPU_VIDSCLK	VR_VID_PHY	VR_VID				CPU_VIDSCLK	8 63
	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R	8
CPU_VIDALERT_L	VR_VID_PHY	VR_VID				CPU_VIDALERT_L	8 63
	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L	8
CPU_VIDSOUT	VR_VID_PHY	VR_VID				CPU_VIDSOUT	8 63
	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R	8
Output Bus							
	POWER	POWER	1.8V			PPCPUVCC_S0_CPU	87

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
CPU VReg Constraints

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
1843	POWER	POWER	12V			REG_VIN_U7600	67
1822	POWER	POWER	5V			REG_VCC1_U7600	67
1822	POWER	POWER	5V			REG_VCC2_U7600	67
3.3V S5							
1849	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5	67
1847	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5	67
1851	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC	67
1848	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5	67
1850	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5	67
1852	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5	67
1107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN	67
1107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET	67
1115	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET	67
1108	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT	67
1107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R	67
1107	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB	67
5V S3							
1113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4	67
1113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4	67
1113	VR_DIDT_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC	67
1114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4	67
1114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4	67
1114	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4	67
1114	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN	67
1114	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET	67
1115	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET	67
1114	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT	67
1114	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R	67
1114	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB	67
Output Bus							
1115	POWER	POWER	5V			PP5V_S5	87
1115	POWER	POWER	5V			PP5V_S4	87
1115	POWER	POWER	3.3V			PP3V3_S5	87
FET Switched							
1122	POWER	POWER	5V			PP5V_S0	87
1123	POWER	POWER	3.3V			PP3V3_S4	87
1125	POWER	POWER	3.3V			PP3V3_S0	87
1145	POWER	POWER	3.3V			PP3V3_S0_SSD	
1124	POWER	POWER	3.3V			PP3V3_ENET	87
1138	POWER	POWER	3.3V			PP3V3_TBTLC	87
Sensed							
1145	POWER	POWER	3.3V			PPSSD_S0	87
1147	POWER	POWER	3.3V			PP3V3_S4_AP	87

3.42V G3H

	Physical	Spacing	Voltage	DIDT	NO_TEST		
3.42V G3H							
1146	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_BOOST	62
1146	POWER	VR_SWITCH	12V	TRUE		P3V42G3H_SW	62
1146	VR_CTL_PHY	VR_CTL				P3V42G3H_FB	62
1146	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L	62
Output Bus							
1146	POWER	POWER	3.425V			PP3V42_G3H	87

3.3V G3

	Physical	Spacing	Voltage	DIDT	NO_TEST		
1147	POWER	POWER	3.3V			PP3V3_G3	87

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
FET Switched							
1150	POWER	POWER	5V			PPHDD_S0	87
Sensed							
1150	POWER	POWER	5V			PP5V_S0_HDD	87

12V

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
1145	POWER	POWER	12V			PP12V_ACDC	87
FET Switched							
1145	POWER	POWER	12V			PP12V_S5	87
1145	POWER	POWER	12V			PP12V_S0	87
1147	POWER	POWER	12V			PP12V_S0_BLC	87
1145	POWER	POWER	12V			PPHDD12_S0	87
Sensed							
1145	POWER	POWER	12V			PP12V_G3H	87
1147	POWER	POWER	12V			PP12V_G3H_P3V42	62
1145	POWER	POWER	12V			PP12V_S0_GPUCORE	87
1145	POWER	POWER	12V			PP12V_S0_FBVDDQ	87
1147	POWER	POWER	12V			PP12V_S0_HDD	87

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Common							
1130	GND	GND	0V			GND	

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
Platform VReg Constraints

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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PAGE 120 OF 127

SHEET 101 OF 106

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C	*	=2x_DIELECTRIC	?
TBT_SPI	*	=2x_DIELECTRIC	?
TBTDP	*	=5x_DIELECTRIC	?
TBTDP	TOP,BOTTOM	=7x_DIELECTRIC	?
BGA_TBT_AREA	*	0.075MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_TBT	BGA_TBT_AREA

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
1G11	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 83
1G12	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 83
1G13 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28
1G14 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28
1G16	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	28 83
1G15	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	28 83
1G17 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	28
1G18 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	28
1G19	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 83
1G21	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 83
1G20 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28
1G22 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28
1G23	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	28 83
1G24	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	28 83
1G26 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	28
1G25 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	28
1G60 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	43
1G62 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	43
1G61 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	43
1G63 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	43
1G70 DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	43
1G71 DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	43
1G69	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	43
1G68	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	43
1G32	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SCL	28
1G31	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SDA	28
1G33 TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	28
1G34 TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	28
1G35 TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	28
1G36 TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	28

*: Only used on hosts supporting T29 video-in

DisplayPort

Electrical Contraint Set	Physical	Spacing		
Graphics Source				
1G42 DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	43 83
1G41 DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	43 83
1G44 DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	43 83
1G45 DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	43 83
1G46	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	43
1G47	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	43
Internal Panel				
1G80	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	43
1G90	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	43
1G87 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	42 43
1G88 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	42 43
1G89 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	42 43
1G91 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	42 43
Internal DP SPDIF				
1G31		HDA	DP_INT_SPDIF_AUDIO	42 54

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
1G41 TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	28 31
1G42 TBT_A_R2D1	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	28 31
1G60 TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	28 31
1G59 TBT_A_R2D0	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	28 31
1G43	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	31
1G44	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	31
1G50 DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	28 31
1G52 DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	28 31
1G51 DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	28 31
1G53 DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	28 31
1G45	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	31
1G47	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	31
1G74	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	31
1G76	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	31
1G40 DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	31
1G39 DP_A_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	31
1G48	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	31
1G50	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	31
1G54 TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	28 31
1G56 TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	28 31
1G73 TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	28 31
1G74 TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	28 31
1G57 TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	28 31
1G58 TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	28 31
1G65	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	31
1G66	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	31
1G67 DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	31
1G68 DP_A_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	31
1G69	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	31
1G61	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	31
Port B				
1G52 TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1>	28 32
1G53 TBT_B_R2D1	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1>	28 32
1G60 TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<0>	28 32
1G61 TBT_B_R2D0	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<0>	28 32
1G55	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	32
1G54	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	32
1G57 DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	28 32
1G59 DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	28 32
1G58 DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	28 32
1G62 DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	28 32
1G63	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	32
1G62	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	32
1G64	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	32
1G66	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	32
1G67 DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32
1G68 DP_B_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32
1G69	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	32
1G70	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	32
1G66 TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	28 32
1G64 TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	28 32
1G76 TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	28 32
1G77 TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	28 32
1G65 TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	28 32
1G67 TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	28 32
1G63	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	32
1G72	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	32
1G68 DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	32
1G72 DP_B_AUXCH_DDC	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	32
1G74	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	32
1G75	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	32

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PAGE TITLE
TBT/DP Constraints

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D
REVISION A.0.0
BRANCH
PAGE 121 OF 127
SHEET 102 OF 106

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=3X_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR_MA2MA	*	=2x_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CLK2CLK	*	=3X_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3x_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_EDC_ISO	*	=3X_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_EDC2EDC	*	=3X_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_DBI2DBI	*	=3x_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_WCK2WCK	*	=3X_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5x_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GPU

GPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_GPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

GPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_GPU_ISO	*	=4:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_GPU	*	*	CLK_GPU_ISO

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing				
Memory Address						
1642 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	NO_TEST=TRUE	80	81
1643 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	NO_TEST=TRUE	80	81
Address Dynamic Bus Inv						
1644 GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	NO_TEST=TRUE	80	81
1645 GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	NO_TEST=TRUE	80	81
Control						
1647 GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	NO_TEST=TRUE	80	81
1648 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	NO_TEST=TRUE	80	81
1649 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	NO_TEST=TRUE	80	81
1650 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	NO_TEST=TRUE	80	81
1651 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	NO_TEST=TRUE	80	81
1652 GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	NO_TEST=TRUE	80	81
1653 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	NO_TEST=TRUE	80	81
1654 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	NO_TEST=TRUE	80	81
1655 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	NO_TEST=TRUE	80	81
1656 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	NO_TEST=TRUE	80	81
Clock						
1657 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	NO_TEST=TRUE	80	81
1658 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	NO_TEST=TRUE	80	81
1659 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	NO_TEST=TRUE	80	81
1660 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	NO_TEST=TRUE	80	81
Data						
1661 GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	NO_TEST=TRUE	80	81
1662 GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	NO_TEST=TRUE	80	81
1663 GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	NO_TEST=TRUE	80	81
1664 GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	NO_TEST=TRUE	80	81
1665 GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	NO_TEST=TRUE	80	81
1666 GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	NO_TEST=TRUE	80	81
1667 GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	NO_TEST=TRUE	80	81
1668 GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	NO_TEST=TRUE	80	81
Error Detection						
1670 GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	NO_TEST=TRUE	80	81
1669 GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	NO_TEST=TRUE	80	81
1671 GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	NO_TEST=TRUE	80	81
1672 GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	NO_TEST=TRUE	80	81
1673 GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	NO_TEST=TRUE	80	81
1674 GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	NO_TEST=TRUE	80	81
1675 GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	NO_TEST=TRUE	80	81
1676 GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	NO_TEST=TRUE	80	81
Data Dynamic Bus Inv						
1677 GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	NO_TEST=TRUE	80	81
1678 GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	NO_TEST=TRUE	80	81
1679 GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	NO_TEST=TRUE	80	81
1680 GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	NO_TEST=TRUE	80	81
1681 GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	NO_TEST=TRUE	80	81
1682 GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	NO_TEST=TRUE	80	81
1683 GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	NO_TEST=TRUE	80	81
1684 GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	NO_TEST=TRUE	80	81
Forwarded Clock						
1685 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	NO_TEST=TRUE	80	81
1686 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	NO_TEST=TRUE	80	81
1687 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	NO_TEST=TRUE	80	81
1688 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	NO_TEST=TRUE	80	81
1689 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	NO_TEST=TRUE	80	81
1690 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	NO_TEST=TRUE	80	81
1691 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	NO_TEST=TRUE	80	81
1692 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	NO_TEST=TRUE	80	81

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing				
Memory Address						
1698 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	NO_TEST=TRUE	80	82
1699 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	NO_TEST=TRUE	80	82
Address Dynamic Bus Inv						
1696 GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	NO_TEST=TRUE	80	82
1697 GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	NO_TEST=TRUE	80	82
Control						
1695 GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	NO_TEST=TRUE	80	82
1701 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	NO_TEST=TRUE	80	82
1702 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	NO_TEST=TRUE	80	82
1703 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	NO_TEST=TRUE	80	82
1704 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	NO_TEST=TRUE	80	82
1706 GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	NO_TEST=TRUE	80	82
1707 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	NO_TEST=TRUE	80	82
1708 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	NO_TEST=TRUE	80	82
1709 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	NO_TEST=TRUE	80	82
1710 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	NO_TEST=TRUE	80	82
Clock						
1693 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	NO_TEST=TRUE	80	82
1694 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	NO_TEST=TRUE	80	82
1711 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	NO_TEST=TRUE	80	82
1712 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	NO_TEST=TRUE	80	82
Data						
1713 GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	NO_TEST=TRUE	80	82
1714 GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	NO_TEST=TRUE	80	82
1715 GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	NO_TEST=TRUE	80	82
1716 GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	NO_TEST=TRUE	80	82
1717 GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	NO_TEST=TRUE	80	82
1718 GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	NO_TEST=TRUE	80	82
1719 GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	NO_TEST=TRUE	80	82
1720 GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	NO_TEST=TRUE	80	82
Error Detection						
1722 GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	NO_TEST=TRUE	80	82
1721 GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	NO_TEST=TRUE	80	82
1723 GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	NO_TEST=TRUE	80	82
1724 GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	NO_TEST=TRUE	80	82
1725 GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	NO_TEST=TRUE	80	82
1726 GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	NO_TEST=TRUE	80	82
1728 GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	NO_TEST=TRUE	80	82
1727 GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	NO_TEST=TRUE	80	82
Data Dynamic Bus Inv						
1729 GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	NO_TEST=TRUE	80	82
1730 GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	NO_TEST=TRUE	80	82
1731 GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	NO_TEST=TRUE	80	82
1732 GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	NO_TEST=TRUE	80	82
1733 GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	NO_TEST=TRUE	80	82
1734 GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	NO_TEST=TRUE	80	82
1735 GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	NO_TEST=TRUE	80	82
1736 GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	NO_TEST=TRUE	80	82
Forwarded Clock						
1737 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	NO_TEST=TRUE	80	82
1738 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	NO_TEST=TRUE	80	82
1739 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	NO_TEST=TRUE	80	82
1740 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	NO_TEST=TRUE	80	82
1741 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	NO_TEST=TRUE	80	82
1742 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	NO_TEST=TRUE	80	82
1743 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	NO_TEST=TRUE	80	82
1744 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	NO_TEST=TRUE	80	82

GPU

Electrical Contraint Set	Physical	Spacing			
Clocks					
1747	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_PL		78
1748	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_NG		78
1749	CLK_PCIE_PHY	CLK_PCIE	GPU_TESTMODE		83
1750	CLK_PCIE_PHY	CLK_PCIE	GPU_PEX_TERMP		78
1751	CLK_GPU_55S	CLK_GPU	FB_A0_CK_MID	NO_TEST=TRUE	81
1752	CLK_GPU_55S	CLK_GPU	FB_A1_CK_MID	NO_TEST=TRUE	81
1753	CLK_GPU_55S	CLK_GPU	FB_B0_CK_MID	NO_TEST=TRUE	82
1754	CLK_GPU_55S	CLK_GPU	FB_B1_CK_MID	NO_TEST=TRUE	82
1755	CLK_GPU_55S	CLK_GPU	FB_C0_CK_MID	NO_TEST=TRUE	
1756	CLK_GPU_55S	CLK_GPU	FB_C1_CK_MID	NO_TEST=TRUE	ULTIMATE
1757	CLK_GPU_55S	CLK_GPU	FB_D0_CK_MID	NO_TEST=TRUE	ONLY
1758	CLK_GPU_55S	CLK_GPU	FB_D1_CK_MID	NO_TEST=TRUE	
1771	CLK_GPU_55S	CLK_GPU	GPU_JTAG_TCK		83 85
1772	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK		83 84
1773	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK_R		84
1774	CLK_GPU_55S	CLK_GPU	GPU_XTALOUT		
1775	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTALOUT		83 84
1776	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTALIN		83 84
SMB					
1754	SMB_PHY	SMB	GPU_SMB_CLK		83 84
1755	SMB_PHY	SMB	GPU_SMB_DAT		83 84
1753	SMB_PHY	SMB	GPU_SMB_CLK_R		49 84
1752	SMB_PHY	SMB	GPU_SMB_DAT_R		49 84
PCIe Compensation					
1761	PCIE_50S	COMP_PCIE	FB_CAL_PD_VDDQ		80
1760	PCIE_50S	COMP_PCIE	FB_CAL_PU_GND		80
1762	PCIE_50S	COMP_PCIE	FB_CAL_TERM_GND		80

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing		
Reset				
1764 GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L	80 81
1765 GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L	80 81
1766 GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L	80 82
1767 GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L	80 82
1768 GDDR_C0_RESET	GDDR_50S	GDDR_CTRL	FB_C0_RESET_L	
1769 GDDR_C1_RESET	GDDR_50S	GDDR_CTRL	FB_C1_RESET_L	ULTIMATE
1770 GDDR_D0_RESET	GDDR_50S	GDDR_CTRL	FB_D0_RESET_L	ONLY
1763 GDDR_D1_RESET	GDDR_50S	GDDR_CTRL	FB_D1_RESET_L	

SYNC_MASTER=D8_AARON SYNC_DATE=03/13/2012

PAGE TITLE
GDDR5/GPU Constraints

Apple Inc.

DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

BRANCH

PAGE 122 OF 127

SHEET 103 OF 106

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	1.00MM	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

BKLT MISCELLANEOUS

Electrical Contraint Set	Physical	Spacing		
SPI				
1556	SMB_PHY	SMB	SMB_PCH_BLC_SCL	
1557	SMB_PHY	SMB	SMB_PCH_BLC_SDA	
1812	SMB_PHY	SMB	SMB_TCON_BLC_SCL	
1811	SMB_PHY	SMB	SMB_TCON_BLC_SDA	
12M REFERENCE CRYSTAL				
1844	CLK_XTAL	XTAL	BLC_MCU_XTAL_IN	72
1843	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT	72
1845	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT_R	72
250K REFERENCE CLOCKS				
1848	CPU_50S	CLK_PCH	STRCLK_R1	72 73
1849	CPU_50S	CLK_PCH	LED_DRVR_CLK	73

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
1766	POWER	POWER	12V			PP12V_S0_BLC_VIN2	72 73 74
1772	POWER	POWER	12V			PP12V_S0_BLC_VINP	72 74
1860	POWER	POWER	14V			PRE_REG_OUT	72 73
1837	POWER	POWER	3.3V			BLC_P3V3S	72 74
1857	POWER	POWER	3.3V			BLC_P3V3_REF	72 74
1838	POWER	POWER	3.3V			BLC_P3V3	
1842	POWER	POWER	3.3V			PP3V3_S0_BLC_R	72
1841	POWER	POWER	8V			SPTX_VIN	73
1840	POWER	POWER	8V			PP8V_BLC	72 73
1847	POWER	POWER	8V			BLC_VIN2	73 74
1862	POWER	POWER	14V			BOOST_FET_DRAIN	72
1863	POWER	POWER	12V			BOOST_VDD	72
1865	POWER	POWER	5V			PP5V_S0_BLC_R	72 73 74
1866	POWER	POWER	12V			PP12V_S0_BLC_F	74
Local Ground							
1764	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_1	73 74
1804	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_2	73 74
1805	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_3	73 74
1810	GND	GND	0V			AGND_BLC	73 74
Backlight							
1765	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1	73
1766	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1_R	73
1796	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2	73
1797	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2_R	73
1798	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3	73
1799	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3_R	73
1795	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_1	73
1793	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_2	73
1794	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_3	73
1801	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS1	73
1800	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS2	73
1802	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS3	73
1876	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C1	73
1877	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C2	73
1878	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C3	73
1813	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_1	73
1832	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_2	73
1841	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_3	73
1836	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK1	73
1834	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK2	73
1835	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK3	73
1852	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1_R	72 73
1850	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2_R	72 73
1847	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3_R	72 73
1840	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1	73 74
1850	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2	73 74
1836	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3	73 74
1816	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF1	73 74
1818	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF2	73 74
1817	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF3	73 74
1795	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP1	73
1800	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP2	73
1801	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP3	73
1822	BLC_CTL_PHY	BLC_CTL				BCOMP1	73
1823	BLC_CTL_PHY	BLC_CTL				BCOMP2	73
1820	BLC_CTL_PHY	BLC_CTL				BCOMP3	73
1839	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT1	73
1838	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT2	73
1837	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT3	73
1853	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_1	73
1855	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_2	73
1856	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_3	73
1858	BLC_CTL_PHY	BLC_CTL				PRE_REG_OUT_R	72
1855	BLC_CTL_PHY	BLC_CTL				BOOST_FB	72
1854	BLC_CTL_PHY	BLC_CTL				BOOST_COMP	72
1857	BLC_CTL_PHY	BLC_CTL				BOOST_COMP_C	72
1870	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV	72
1871	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV_R	72
1869	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS	72
1868	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS_R	72
1750	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_1	73
1753	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_2	73
1754	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_3	73
OUTPUT BUS							
1749	POWER_BLC_RET	BLC_HV	80V			IS1_BLC_F	74
1748	POWER_BLC_RET	BLC_HV	80V			IS2_BLC_F	74
1750	POWER_BLC_RET	BLC_HV	80V			IS3_BLC_F	74
1751	POWER_BLC_RET	BLC_HV	80V			IS1_BLC	73 74
1752	POWER_BLC_RET	BLC_HV	80V			IS2_BLC	73 74
1753	POWER_BLC_RET	BLC_HV	80V			IS3_BLC	73 74
1783	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_1	74
1782	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_1	74
1784	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_2	74
1785	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_2	74
1786	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_3	74
1787	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_3	74
1825	POWER_BLC	BLC_HV	80V			BLC_VOUT1	73 74
1824	POWER_BLC	BLC_HV	80V			BLC_VOUT2	73 74
1826	POWER_BLC	BLC_HV	80V			BLC_VOUT3	73 74

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
BLC Constraints

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DRAWING NUMBER 051-9884 SIZE D

REVISION A.0.0

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PAGE 124 OF 127

SHEET 104 OF 106

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GPU CORE PHASES

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
	POWER	POWER	12V			PP12V_S0_GPUCORE_FLT	69 70 71
	POWER	POWER	5V			PP5V_S0_GPU_VCORE_VCC	69
Local Ground							
	GND	GND	0V			AGND_GPU	69
Phase 1							
	POWER	POWER	12V			REG_LVCC_UB510	70
	POWER	POWER	12V			REG_UVCC_UB510	70
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_1	69 70
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM1_R	69
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_1	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_1	70
	POWER	POWER	0.9V			PPGPUCORE_S0_SENSE_1	70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_P	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_N	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_P	69
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_N	69
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS1_RR_2	69
Phase 2							
	POWER	POWER	12V			REG_LVCC_UB530	70
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_2	69 70
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM2_R	69
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_2	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_2	70
	POWER	POWER	0.9V			PPGPUCORE_S0_SENSE_2	70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_P	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_N	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_P	69
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_N	69
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS2_RR_2	69
Phase 3							
	POWER	POWER	12V			REG_VCC_UB550	70
	POWER	POWER	12V			REG_UVCC_UB550	70
	POWER	POWER	12V			REG_LVCC_UB550	70
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_3	69 70
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM3_R	69
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_3	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_3	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_3_RC	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_3	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_3	70
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_3	70
	POWER	POWER	0.9V			PPGPUCORE_S0_SENSE_3	70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_P	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_N	69 70
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_P	69
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_N	69
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS3_RR_2	69
Phase 4							
	POWER	POWER	12V			REG_LVCC_UB650	71
	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_4	69 71
	VR_CTL_PHY	VR_CTL				VR_GPU_PWM4_R	69
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_4	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_4	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_4_RC	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_4	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_GPUCORE_4	71
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_4	71
	POWER	POWER	0.9V			PPGPUCORE_S0_SENSE_4	71
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_P	69 71
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_N	69 71
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_P	69
ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_N	69
ISNS_GPU_CORE		SENSE				VR_GPU_ISNS4_RR_2	69

GPU CORE CONTROLLER

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
ISL6334							
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP	69
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_R	69
	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_RC	69
	VR_CTL_PHY	VR_CTL				VR_GPU_FB	69
	VR_CTL_PHY	VR_CTL				VR_GPU_FB_R	69
	VR_CTL_PHY	VR_CTL				VR_GPU_VDIFF	69
	VR_CTL_PHY	VR_CTL				VR_VDF_R1	69
	VR_CTL_PHY	VR_CTL				VR_VDF_R2	69
	VR_CTL_PHY	VR_CTL				VR_GPU_TCOMP	69
	VR_CTL_PHY	VR_CTL				VR_GPU_OFS	69
	VR_CTL_PHY	VR_CTL				VR_GPU_FS	69
		VR_CTL				VR_GPU_EN_VTT	69
		VR_CTL				PM_EN_REG_GPUCORE_S0	69 76
		VR_CTL				PM_PGOOD_REG_GPUCORE_S0	69 76
		VR_CTL				GPU_PSI_L	69 84
	VR_CTL_PHY	VR_CTL				VR_GPU_IOUT	
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON	50 69 105
	VR_CTL_PHY	VR_CTL				VR_GPU_FAN	69 105
		VR_CTL				VR_GPU_VRDHOT	69
		VR_CTL				VR_GPU_EN_PWR	
	VR_CTL_PHY	VR_CTL				VR_GPU_SS	69
	VR_CTL_PHY	VR_CTL				VR_GPU_DAC	69
	VR_CTL_PHY	VR_CTL				VR_GPU_REF	69
	VR_CTL_PHY	VR_CTL				VR_GPU_TM	69
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON	50 69 105
	VR_CTL_PHY	VR_CTL				VR_GPU_FAN	69 105
	VR_CTL_PHY	VR_CTL				VR_GPU_VRHOT	
		VR_CTL				GPU_PSI_R	
		VR_CTL				GPU_PSI_L_R	
	VR_CTL_PHY	VR_CTL				VR_GPU_IMON_R	69
VSNS_GPU_VDD	SNS_DIFF_PHY	SENSE				VSNS_GPU_VDD	69 85
VSNS_GPU_VSS	SNS_DIFF_PHY	SENSE				VSNS_GPU_VSS	69 85
	SNS_DIFF_PHY	SENSE				VR_GPU_VSEN	69
	SNS_DIFF_PHY	SENSE				VR_GPU_RGND	69
GPU VIDS							
		VR_VID				REG_GPUCORE_VID7	69
		VR_VID				REG_GPUCORE_VID6	69 85
		VR_VID				REG_GPUCORE_VID5	69 85
		VR_VID				REG_GPUCORE_VID4	69 85
		VR_VID				REG_GPUCORE_VID3	69 85
		VR_VID				REG_GPUCORE_VID2	69 85
		VR_VID				REG_GPUCORE_VID1	69 85
		VR_VID				REG_GPUCORE_VID0	69
		VR_VID				GPU_VCORE_VID6	
		VR_VID				GPU_VCORE_VID5	84 85
		VR_VID				GPU_VCORE_VID4	84 85
		VR_VID				GPU_VCORE_VID3	84 85
		VR_VID				GPU_VCORE_VID2	84 85
		VR_VID				GPU_VCORE_VID1	84 85
		VR_VID				GPU_VCORE_VID0	84 85
Output Bus							
	POWER	POWER	0.9V			PPVCORE_S0_GPU	87

GPU FBVDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
	POWER	POWER	5V			REG_VCC_U7750	68
	POWER	POWER	5V			REG_PVCC_U7750	68
Local Ground							
	GND	GND	0V			AGND_FBVDDQ	68
FBVDDQ							
	POWER	VR_SWITCH	12V	TRUE		REG_PHASE_FBVDDQ	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_FBVDDQ	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_FBVDDQ_RC	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ_R	
	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_FBVDDQ	68
	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_FBVDDQ	68
		SENSE				VSNS_FBVDDQ	
VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_P	68 85
VSNS_GPU_VDDQ	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_N	68 85
		SENSE				FBVDDQ_SENSE_R	
	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_OCSET	68
	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_VO	68
		SENSE				REG_FBVDDQ_FB	
		SENSE				REG_FBVDDQ_RTN	
		SENSE				REG_FBVDDQ_FB_R	68
		SENSE				REG_FBVDDQ_RTN_R	68
Output Bus							
	POWER	POWER	1.5V			PPFBVDDQ_S0_GPU	87

SYNC_MASTER=J17_ULTIMATE SYNC_DATE=05/16/2013

PAGE TITLE
GPU VREG CONSTRAINTS

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DRAWING NUMBER 051-9884 SIZE D

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PAGE 125 OF 127

SHEET 105 OF 106

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4V5_*

Physical	Spacing	Netname	
POWER	POWER	4V5_REG_IN	54

ENET_*

Physical	Spacing	Netname	
XDP_PHY	XDP	ENET_LOW_PWR	20 37 39

GPU_*

Physical	Spacing	Netname	
SPI_50S	SPI	GPU_ROM_CS_L	83 84
SPI_50S	SPI	GPU_ROM_CS_L_R	84
SPI_50S	SPI	GPU_ROM_SI	83 84
SPI_50S	SPI	GPU_ROM_SI_R	84
SPI_50S	SPI	GPU_ROM_SO	83 84
SPI_50S	SPI	GPU_ROM_SO_R	84
SPI_50S	SPI	GPU_ROM_WP_L	84

GPU_*

Physical	Spacing	Netname	
XDP_PHY	XDP	GPU_JTAG_TDI	83 85
XDP_PHY	XDP	GPU_JTAG_TDO	83 85
XDP_PHY	XDP	GPU_JTAG_TMS	83 85
XDP_PHY	XDP	GPU_JTAG_TRST_L	83

JTAG_*

Physical	Spacing	Netname	
XDP_PHY	XDP	JTAG_TBT_TDI	20 28
XDP_PHY	XDP	JTAG_TBT_TDO	20 28
XDP_PHY	XDP	JTAG_TBT_TMS	20 28

ISNS_*

Physical	Spacing	Netname	
SMC_50S	SENSE	ISNS_GPUCORE_FB	50 98
SMC_50S	SENSE	ISNS_P12VG3H_R	50 98
SMC_50S	SENSE	ISNS_P12VS0_FBVDDQ_R	50 98
SMC_50S	SENSE	ISNS_P12VS0_HDD_R	50 98
SMC_50S	SENSE	ISNS_P3V3S4_AP_R	50 98

SMC_*

Physical	Spacing	Netname	
CLK_XTAL	XTAL	SMC_XTAL_R	47

REG_*

Physical	Spacing	Netname	
VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET0	68
VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1	68
VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1_R	68
VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SREF	68

SMBUS_*

Physical	Spacing	Netname	
SMB_PHY	SMB	SMBUS_SMC_4_ASF_SCL	46 47
SMB_PHY	SMB	SMBUS_SMC_4_ASF_SDA	46 47

SMC_*

Physical	Spacing	Netname	
	SENSE	SMC_OOB1_RX_CN	36
	SENSE	SMC_OOB1_RX_FILT	36

TSNS_*

Electrical	Physical	Spacing	Netname	
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_N	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_P	52
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_N	
SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_P	

BLC_*

Physical	Spacing	Voltage	Netname	
BLC_CTL_PHY	BLC_CTL	5V	BLC_MCU_AOUT_R	74
SMB_PHY	SMB		BLC_MCU_B_SDA_CONN	
XDP_PHY	CLK_JTAG		BLC_MCU_RTCK	72
XDP_PHY	XDP		BLC_MCU_TCK	72
XDP_PHY	XDP		BLC_MCU_TDI	72
XDP_PHY	XDP		BLC_MCU_TDO	72
XDP_PHY	XDP		BLC_MCU_TMS	72
XDP_PHY	XDP		BLC_MCU_TRST	72
XDP_PHY	XDP		BLC_MCU_TXD0	72

TBT_*

Physical	Spacing	Voltage	Netname	
TBT_I2C_55S	TBT_I2C		TBT_A_CONFIG1_RC	31
TBT_I2C_55S	TBT_I2C		TBT_B_CONFIG1_RC	32

DP_*

Physical	Spacing	Netname	
TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_CLK	31 33
TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_DATA	31 33
TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_CLK	32 33
TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_DATA	32 33

SML_*

Physical	Spacing	Netname	
SMB_PHY	SMB	SML_PCH_1_CLK	13 49
SMB_PHY	SMB	SML_PCH_1_DATA	13 49

AYNCHRONOUS

Electrical	Physical	Spacing	Netname	
	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_L	6 46 47 63
	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_R_L	6
	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PECI_L	
	CPU_ASYNC_PHY	CPU_ASYNC	SMC_PECI_L	46 47 98
	CPU_ASYNC_PHY	CPU_ASYNC	CPU_CATERR_L	6 47
	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PWRGD	6 14 18
	CPU_ASYNC_PHY	CPU_ASYNC	PM_SYNC	6 12
	CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L	14 47
	CPU_ASYNC_PHY	CPU_ASYNC	CPU_RESET_L	6 14 18
	CPU_ASYNC_PHY	CPU_ASYNC	SMC_CPU_CATERR_L	46 47
	CPU_ASYNC_PHY	CPU_ASYNC	PCH_PROCPWRGD	14

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ASYNC_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ASYNC	*	*	CPU_ASYNC_ISO

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_ASYNC_PHY	*	CPU_50S

PAGE TITLE
MISC-CONSTRAINTS 1

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REVISION A.0.0

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PAGE 127 OF 127

SHEET 106 OF 106

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