1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

# D8 MLB ULTIMATE

LAST_MODIFIED=Tue Jul 3 15:14:05 2012

| REV | ECN | DESCRIPTION OF REVISION | CK APPD / DATE |
|---|---|---|---|
| | | | 2012-07-03 |


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DRAWING

TITLE=K72
ABBREV=DRAWING
LAST_MODIFIED=Tue Jul 3 15:14:05 2012

DRAWING TITLE: SCH,D8,MLB ULTIMATE

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DRAWING NUMBER: 051-9505 SIZE: D
REVISION: 6.1.0
BRANCH:
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DRAWING

System Block diagram can be found on Kismet

PATH: KISMET > K70/72 > BLOCK DIAGRAMS > K72 BLOCK DIAGRAM

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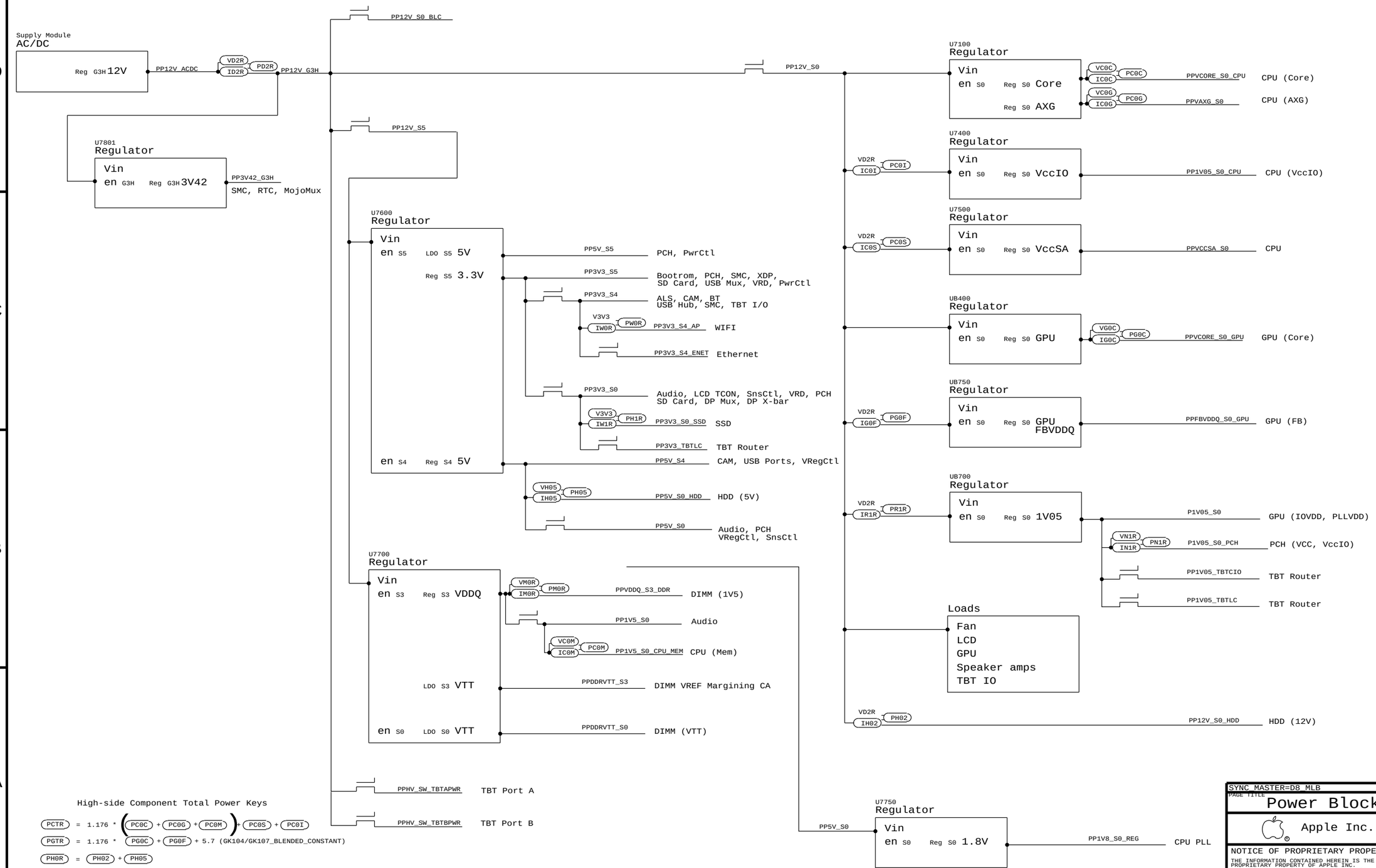


High-side Component Total Power Keys

PCTR = 1.176 * (PC0C + PC0G + PC0M) + PC0S + PC0I

PGTR = 1.176 * PG0C + PG0F + 5.7 (GK104/GK107_BLENDED_CONSTANT)

PH0R = PH02 + PH05

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# Power Block Diagram

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## BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|---|---|---|
| 639-3662 | PCBA,MLB,ULTIMATE,3.4G,GTX,SAM,2GB,D8 | D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GTX,FB:2G_SAMSUNG,EEEE:F0V5 |
| 639-3950 | PCBA,MLB,ULTIMATE,3.2G,GTX,SAM,2GB,D8 | D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GTX,FB:2G_SAMSUNG,EEEE:F49R |
| 639-3560 | PCBA,MLB,ULTIMATE,3.4G,GT,SAM,1GB,D8 | D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GT,FB:1G_SAMSUNG,EEEE:DYW3 |
| 639-3949 | PCBA,MLB,ULTIMATE,3.2G,GT,SAM,1GB,D8 | D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GT,FB:1G_SAMSUNG,EEEE:F49P |
| 639-4087 | PCBA,MLB,ULTIMATE,3.4G,GTX,HYN,2GB,D8 | D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GTX,FB:2G_HYNIX,EEEE:F64W |
| 639-4091 | PCBA,MLB,ULTIMATE,3.2G,GTX,HYN,2GB,D8 | D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GTX,FB:2G_HYNIX,EEEE:F652 |
| 639-4086 | PCBA,MLB,ULTIMATE,3.4G,GT,HYN,1GB,D8 | D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GT,FB:1G_HYNIX,EEEE:F64V |
| 639-4090 | PCBA,MLB,ULTIMATE,3.2G,GT,HYN,1GB,D8 | D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GT,FB:1G_HYNIX,EEEE:F651 |
| 085-4435 | PCBA,MLB,DEV,D8.ULTIMATE | DEVELOPMENT,D8_DEVEL |

## Bar Code Labels / EEEE #'s

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_DYW3 | CRITICAL | EEEE:DYW3 |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F0V5 | CRITICAL | EEEE:F0V5 |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F49P | CRITICAL | EEEE:F49P |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F49R | CRITICAL | EEEE:F49R |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F4MW | CRITICAL | EEEE:F4MW |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F4TY | CRITICAL | EEEE:F4TY |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F64W | CRITICAL | EEEE:F64W |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F652 | CRITICAL | EEEE:F652 |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F64V | CRITICAL | EEEE:F64V |
| 825-7122 | 1 | MLB LABEL,48.0X4.8 | EEEE_F651 | CRITICAL | EEEE:F651 |

## BOM Groups

| BOM GROUP | BOM OPTIONS |
|---|---|
| D8_COMMON | COMMON,ALTERNATE,D8_COMMON1,D8_PROGPARTS |
| D8_COMMON1 | XDP,RSMRST:GATE,SPEAKERID,VREF:CPU,TBTHV:P12V,PRE_BOOST:Y |
| D8_PROGPARTS | SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG,BLCMCU:PROG |
| D8_DEVEL | XDP_CONN,LPCPLUS,VREFMRGN:EXT,BKLT_PWM,DEVEL_AUDIO,TEMPSNSDEV |

## CPUs

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S4356 | 1 | IVB,SR0T8,PRQ,N1,3.2,77W,4+1,1.1,6M,LGA | CPU | CRITICAL | CPU:4C_3P2GHZ |
| 337S4247 | 1 | IVB,SR0PK,PRQ,E1,3.4,77W,4+2,1.15,8M,LG | CPU | CRITICAL | CPU:4C_3P4GHZ |

## ASICs

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 337S4277 | 1 | IC,PANTHER POINT,C1,SLJC7,PRQ,BD82Z77 | U1800 | CRITICAL | |
| 338S1113 | 1 | IC,TBT,CR-4C,B1,PRQ,288 FCBGA,12X12MM | U3600 | CRITICAL | |
| 343S0616 | 1 | IC,BCM57766A1,ENET&SD,8X8 | U3900 | CRITICAL | |
| 337S4333 | 1 | IC, GPU, NV GK104 7-4-PS-A2 | UA000 | CRITICAL | GPU:104GT |
| 337S4333 | 1 | IC, GPU, NV GK104 7-4-PS-A2 | UA000 | CRITICAL | GPU:104GT2 |
| 337S4332 | 1 | IC, GPU, NV GK104 8-4-PS-A2, | UA000 | CRITICAL | GPU:104GTX |

## Programmable Parts

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION | |
|---|---|---|---|---|---|---|
| 341S3640 | 1 | IC,EEPROM,CR,V11.1 (B1),D8 | U3690 | CRITICAL | TBTROM:PROG | |
| 335S0865 | 1 | IC,EEPROM,SERIAL,8KB,MLP8 | U3690 | CRITICAL | TBTROM:BLANK | |
| 341S3641 | 1 | IC,PROGRMD,EFI ROM,PIB,D7/D8 | U5110 | CRITICAL | BOOTROM:PROG | ALTERNATE:335S0812 |
| 335S0807 | 1 | IC,64 MBIT SPI SERIAL FLASH | U5110 | CRITICAL | BOOTROM:BLANK | |
| 341S3394 | 1 | IC,PROGRMD,SMC,A3,V2.2A32,D8 | U4900 | CRITICAL | SMC:PROG | |
| 338S1098 | 1 | IC,SMC,LX4FS1AH5BBCIGA3 | U4900 | CRITICAL | SMC:BLANK | |
| 341S3646 | 1 | IC,CAMERA FLASH,V7226,D7/D8 | U4202 | CRITICAL | CAMROM:PROG | |
| 335S0852 | 1 | IC,FLASH,SPI,1MBIT,3V3 | U4202 | CRITICAL | CAMROM:BLANK | |
| 341S3645 | 1 | IC,ENET 1MBIT, SPI,ROM, V1.13 D8 | U3990 | CRITICAL | CIVROM:PROG | ALTERNATE:335S0854 |
| 335S0862 | 1 | IC,SERIAL FLASH,2MBIT, 2.7V, REF F | U3990 | CRITICAL | CIVROM:BLANK | |
| 341S3627 | 1 | IC,BLC,MCU, PRPOGRAMMED, V0203, D8 | U9700 | CRITICAL | BLCMCU:PROG | |
| 337S3978 | 1 | IC,BLC MCU LPC2132FBD64/01, LQFP64 | U9700 | CRITICAL | BLCMCU:BLANK | |

## CPU SOCKET

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 511S0073 | 1 | SOCKET.MOLEX,LGA1155,CPU-LF | U1000 | CRITICAL | |

## CPU SOCKET ALTERNATES

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 511S0071 | 511S0073 | | ALL | TYCO SOCKET |
| 511S0072 | 511S0073 | | ALL | FOXCONN SOCKET |

## D8 SCHEMATIC / PCB #'S

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 051-9505 | 1 | SCH,MLB,D8,ULTIMATE | SCH1 | CRITICAL | D8 |
| 820-3299 | 1 | PCBF,MLB,D8,ULTIMATE | PCB1 | CRITICAL | D8 |

## D8 ALTERNATES

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 377S0147 | 377S0126 | | ALL | USB diodes |
| 157S0084 | 157S0058 | | ALL | Enet Magnetics |
| 341S3644 | 341S3645 | | U3990 | CIVROM |
| 376S0975 | 376S1081 | | ALL | P/NCH DUAL FET |
| 152S1668 | 152S1591 | | ALL | 33UH BLC INDUCTOR |
| 128S0365 | 128S0368 | | ALL | 150UF CAPS BLK |

## VRAM Module Parts

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 333S0619 | 4 | IC,SGRAM,GDDR5,32MX32,1.5GHZ,G-DIE,HF | UA300,UA350,UA400,UA450 | CRITICAL | FB:1G_SAMSUNG |
| 333S0619 | 4 | IC,SGRAM,GDDR5,32MX32,1.5GHZ,G-DIE,HF | UA500,UA550,UA600,UA650 | CRITICAL | FB:1G_SAMSUNG |
| 333S0620 | 4 | IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE | UA300,UA350,UA400,UA450 | CRITICAL | FB:1G_HYNIX |
| 333S0620 | 4 | IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE | UA500,UA550,UA600,UA650 | CRITICAL | FB:1G_HYNIX |
| 333S0631 | 4 | IC,SGRAM,GDDR5,64MX32,D-DIE | UA300,UA350,UA400,UA450 | CRITICAL | FB:2G_SAMSUNG |
| 333S0631 | 4 | IC,SGRAM,GDDR5,64MX32,D-DIE | UA500,UA550,UA600,UA650 | CRITICAL | FB:2G_SAMSUNG |
| 333S0630 | 4 | IC,GDDR5,64MX32,A-DIE | UA300,UA350,UA400,UA450 | CRITICAL | FB:2G_HYNIX |
| 333S0630 | 4 | IC,GDDR5,64MX32,A-DIE | UA500,UA550,UA600,UA650 | CRITICAL | FB:2G_HYNIX |

SYNC MASTER=D8_MLB_ULTIMATE SYNC DATE=06/15/2012

PAGE TITLE
# BOM Configuration

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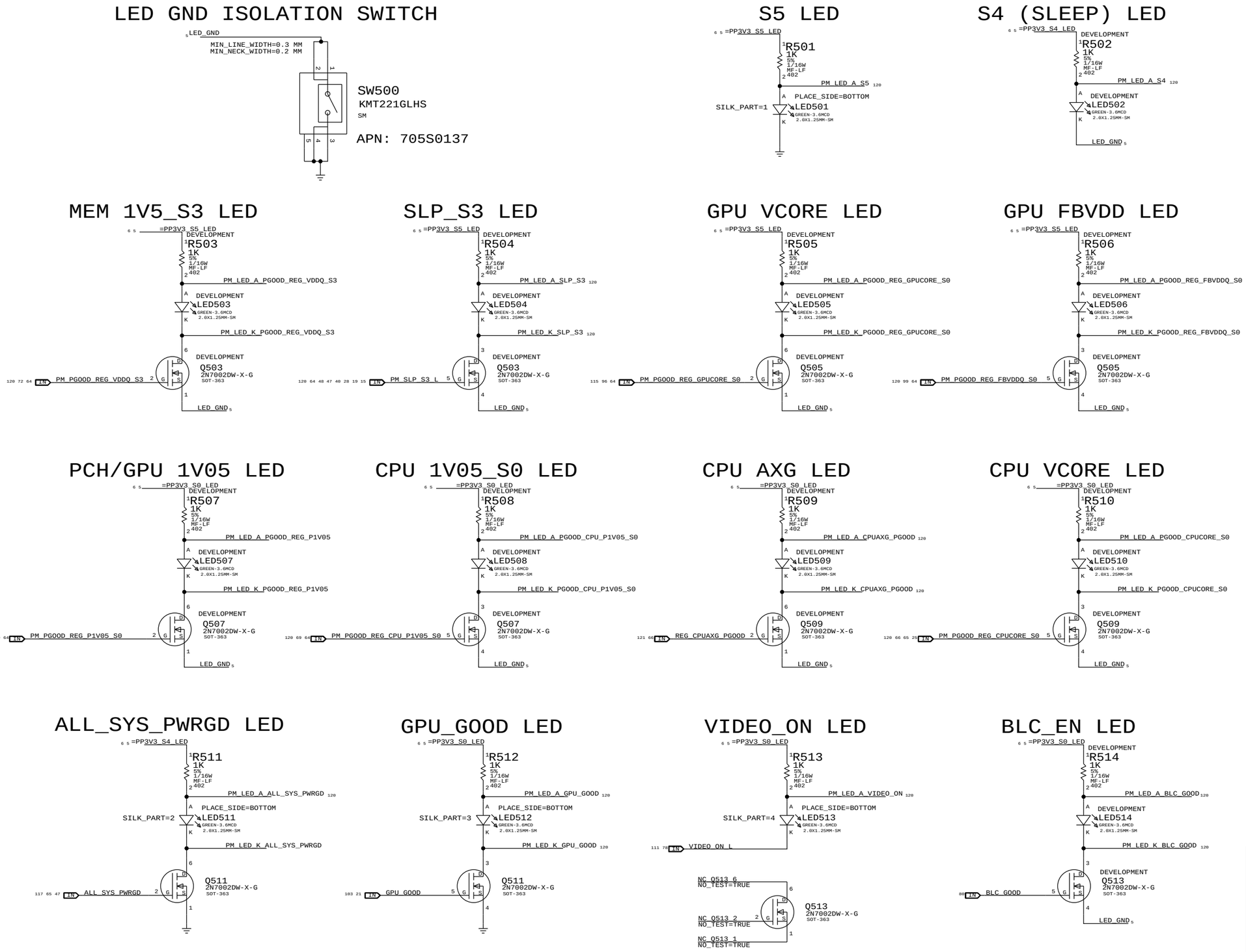


SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
DEBUG LEDS

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## MLB to AC-DC Supplemental Signal Connector

SILK_PART=PWRSIG
J601
504050-0791
M-RT-SM
518S0863

121 48 OUT PWR_BTN — PLACE_NEAR=R606.1:3MM
R606 1K 5% 1/10W MF-LF 402 — PLACE_NEAR=J601.1:3MM
121 PWR_BTN_R — PLACE_NEAR=J601.1:3MM
C600 0.1UF 10% 16V X5R 402
D600 6.8V-100PF 402
122 6 SMC_ACDC_ID_R
122 53 OUT TSNS_ACDC_N
122 53 OUT TSNS_ACDC_P
71,48 117 IN BURSTMODE_EN_L — PLACE_NEAR=R600.1:3MM
C605 0.1UF 10% 16V X5R 402
R600 1K 5% 1/10W MF-LF 402 — PLACE_NEAR=J601.7:3MM
BURSTMODE_EN_R_L
D602 6.8V-100PF 402 — PLACE_NEAR=J601.7:3MM

FILTER ADDED TO BURSTMODE_EN_L TO PASS SURGE RDAR://11059712

99 96 72 70 69 66 6 =PP3V3_S0_VRD
R603 10K 5% 1/16W MF-LF 402 — PLACE_NEAR=J601.3:30MM
122 6 SMC_ACDC_ID_R
R604 1K 5% 1/16W MF-LF 402 — PLACE_NEAR=J601.3:3MM
SMC_ACDC_ID 48 122
D601 6.8V-100PF 402 — PLACE_NEAR=J601.1:4MM
C604 0.01UF 20% 16V X7R-CERM 0402 — PLACE_NEAR=R604.2:3MM

## MLB to AC-DC Connector

CRITICAL
J600
43045-1201
M-RT-TH-1
518-0389

6 PP12V_G3H_ACDC
J600.4:10MM C601 10UF 10% 25V X5R 805
EMC J600.5:10MM C602 1000PF 5% 25V NP0-C0G 402
EMC J600.5:10MM C603 1000PF 5% 25V NP0-C0G 402
PP12V_G3H_ACDC 6

## G3 Rails

Always on: Keeps the PCH RTC alive

110 PP3V3_G3 MAKE_BASE=TRUE
- PP3V3_G3_RTC 26 121
- =PP3V3_G3_PCH_RTC 22
- =PP3V3_G3_PCH 18 19

## G3H Rails

On with AC/DC plugged in

110 PP12V_ACDC MAKE_BASE=TRUE
- PP12V_G3H_ACDC 6
- =PP12V_G3H_PWR 51

110 PP12V_G3H MAKE_BASE=TRUE
- PP12V_G3H_SNS 51
- =PP12V_G3H_P3V42 73
- =PP12V_G3H_FET_P12V_S0 74
- =PP12V_G3H_FET_P12V_S5 74

110 PP3V42_G3H MAKE_BASE=TRUE
- PP3V42_G3H_REG 73
- =PP3V3_G3H_BT 35
- =PP3V3_G3H_RTC_D 26
- =PP3V3_G3H_SMC 47 48 50
- =PP3V3_G3H_SMC_USBMUX 45
- =PPVIN_G3H_SMCVREF 48
- =PP3V3_G3H_LPCPLUS 49

## S5 Rails

On when in S5

110 PP12V_S5 MAKE_BASE=TRUE
- PP12V_S5_FET 74
- =PP12V_S5_REG_P3V3P5V_S5 71
- =PP12V_S5_REG_VDDQ_S3 72
- =PP12V_S5_PWRCTL 64 65 74
- =PPHV_SW_TBTAPWRSW 77
- =PPHV_SW_TBTBPWRSW 79
- =PP12V_S5_SNS 51

110 PP5V_S5 MAKE_BASE=TRUE
- PP5V_S5_LDO 71
- =PP5V_S5_PWRCTL 71
- =PP5V_S5_PCH 24

110 PP3V3_S5 MAKE_BASE=TRUE
- PP3V3_S5_REG 71
- =PP3V3_S5_FET_P3V3_S0 74
- =PP3V3_S5_FET_P3V3_S4 74
- =PP3V3_S5_SMC 48
- =PP3V3_S5_LED 5
- =PP3V3_S5_PCH 19 24 26
- =PP3V3_S5_PCH_STRAPS 15
- =PP3V3_S5_PCH_VCCSUS_HDA 22 24
- =PP3V3_S5_PCH_VCCSUS_USB 22 24
- =PP3V3_S5_PCH_VCC_DSW 22 24
- =PP3V3_S5_PCH_VCC_SPI 22 24
- =PP3V3_S5_PWRCTL 64 65
- =PP3V3_S5_ROM 49
- =PP3V3_S5_VRD 71
- =PP3V3_S5_XDP 25
- =PP3V3_S5_SMC_USBMUX 45 46
- =PP3V3_S5_SENSE 51
- =PP3V3_S5_SDCARD 41

## S4 Rails

Enabled when system has AC and is in run or sleep

110 PP5V_S4 MAKE_BASE=TRUE
- PP5V_S4_REG 71
- =PP5V_S4_REG_VDDQ_S3 72
- =PP5V_S4_FET_P5V_S0 74
- =PP5V_S4_MEMRESET 28
- =PP5V_S4_USB 45 46
- =PP5V_S4_CAMERA 42

110 60 PP3V3_S4 MAKE_BASE=TRUE
- PP3V3_S4_FET 74
- =PP3V3_S4_ALS 42
- =PP3V3_S4_AP_PWR 55
- =PP3V3_S4_CAMERA 42 43
- =PP3V3_S4_ENET 40
- =PP3V3_S4_LED 5
- =PP3V3_S4_MEMRESET 28
- =PP3V3_S4_PM 28
- =PP3V3_S4_PWRCTL 65 72 74
- =PP3V3_S4_SENSE 51
- =PP3V3_S4_SMBUS 50
- =PP3V3_S4_SMBUS_SMC 50
- =PP3V3_S4_SMC 48
- =PP3V3_S4_TBT 36 37 38 77 79
- =PP3V3_S4_TBTAPWRSW 48 77
- =PP3V3_S4_TBTBPWRSW 48 79
- =PP3V3_S4_USB_HUB 27
- =PP3V3_S4_VREFMRGN 34

110 PP3V3_S4_AP MAKE_BASE=TRUE
- PP3V3_S4_AP_SNS 55
- =PP3V3_S4_AP 15 35

110 PP3V3_S4_ENET MAKE_BASE=TRUE
- PP3V3_S4_ENET_FET 40
- =PP3V3_S4_ENET_FET 39 40
- =PP3V3_S4_ENET_SYSCLK 26
- =PP3V3_S4_ENET_CLK 26

## S3 Rails

Enabled when system is in run or sleep

110 PPVDDQ_S3 MAKE_BASE=TRUE
- PPVDDQ_S3_REG 72
- =PPVDDQ_S3_DDR_PWR 51
- =PPVDDQ_S3_FET_VDDQ_S0 74
- =PPVDDQ_S3_LDO_DDRVTT 72

THIS IS 1.5V RAIL

110 PPVDDQ_S3_DDR MAKE_BASE=TRUE
- PPVDDQ_S3_DDR_SNS 51
- =PPVDDQ_S3_DDR_VREF 34
- =PPVDDQ_S3_MEM_A 29 30
- =PPVDDQ_S3_MEM_B 31 32
- =PPVDDQ_S3_MEMRESET 28

THIS IS 1.5V RAIL

110 PPDDRVTT_S3 MAKE_BASE=TRUE
- PPDDRVTT_S3_LDO 72
- =PPDDRVTT_S3_VREFCA 34

THIS IS 1.5V RAIL

## S0 Rails

Enabled when system is in run

110 PP12V_S0 MAKE_BASE=TRUE
- PP12V_S0_FET 74
- =PP12V_S0_AUDIO_SPKRAMP 58 59
- =PP12V_S0_FAN 54
- =PP12V_S0_FBVDDQ_PWR 51
- =PP12V_S0_REG_GPUCORE 96
- =PP12V_S0_HDD_PWR 51
- =PP12V_S0_LCD 78
- =PP12V_S0_REG_CPUCORE 67
- =PP12V_S0_REG_CPU_P1V05_PWR 55
- =PP12V_S0_REG_CPU_VCCSA_PWR 55
- =PP12V_S0_REG_P1V05_PWR 55
- =PP12V_S0_PWRCTL 65

110 PP12V_S0_HDD MAKE_BASE=TRUE
- PP12V_S0_HDD_SNS 51
- =PP12V_S0_HDD 52

110 PP12V_S0_BLC MAKE_BASE=TRUE
- PP12V_S0_BLC_FET 74
- =PP12V_S0_BLC 82

110 PP12V_S0_FBVDDQ MAKE_BASE=TRUE
- PP12V_S0_FBVDDQ_SNS 51
- =PP12V_S0_REG_FBVDDQ 99

110 PP12V_S0_CPU_P1V05 MAKE_BASE=TRUE
- PP12V_S0_REG_CPU_P1V05_SNS 55
- =PP12V_S0_REG_CPU_P1V05 69

110 PP12V_S0_VCCSA MAKE_BASE=TRUE
- PP12V_S0_REG_CPU_VCCSA_SNS 55
- =PP12V_S0_REG_VCCSA 70

110 PP12V_S0_P1V05 MAKE_BASE=TRUE
- PP12V_S0_REG_P1V05_SNS 55
- =PP12V_S0_REG_P1V05 99

110 PP5V_S0 MAKE_BASE=TRUE
- PP5V_S0_FET 74
- =PP5V_S0_AUDIO 56 63
- =PP5V_S0_BLC 82
- =PP5V_S0_HDD_PWR 51
- =PP5V_S0_ISENSE 51
- =PP5V_S0_LPCPLUS 49
- =PP5V_S0_PCH 24
- =PP5V_S0_REG_CPUCORE 66
- =PP5V_S0_REG_CPU_P1V05 69
- =PP5V_S0_REG_FBVDDQ 99
- =PP5V_S0_REG_P1V05 99
- =PP5V_S0_REG_P1V8 72
- =PP5V_S0_REG_VCCSA 70
- =PP5V_S0_VRD 72 96

110 PP5V_S0_HDD MAKE_BASE=TRUE
- PP5V_S0_HDD_SNS 51
- =PP5V_S0_HDD 52

110 PP3V3_S0 MAKE_BASE=TRUE
- PP3V3_S0_FET 74
- =PP3V3_S0_GPU_IFPX_PLLVDD 90
- =PP3V3_S0_GPU_MISC 92
- =PP3V3_S0_GPU_VDD33 91
- =PP3V3_S0_AUDIO 42 56 58 59 62
- =PP3V3_S0_AUDIO_DIG 60
- =PP3V3_S0_BLC 80
- =PP3V3_S0_DP 76 78
- =PP3V3_S0_ENET 39
- =PP3V3_S0_FAN 54
- =PP3V3_S0_GPU 83 91 92 95 96
- =PP3V3_S0_INTDPMUX 75
- =PP3V3_S0_LED 5
- =PP3V3_S0_LED_SATA 15 44
- =PP3V3_S0_MEM_A_SPD 29 30
- =PP3V3_S0_MEM_B_SPD 31 32
- =PP3V3_S0_P3V3TBTFET 38
- =PP3V3_S0_PCH 18 21 24
- =PP3V3_S0_PCH_GPIO 15 19 20 38
- =PP3V3_S0_PCH_PM 26
- =PP3V3_S0_PCH_STRAPS 15
- =PP3V3_S0_PCH_VCC 22 24
- =PP3V3_S0_PCH_VCC_ADAC 17
- =PP3V3_S0_PCH_VCC_GPIO 22 24
- =PP3V3_S0_PCH_VCC_HVCMOS 22 24
- =PP3V3_S0_PCH_VCC_PCI 22 24
- =PP3V3_S0_PWRCTL 28 74
- =PP3V3_S0_RSTBUF 26
- =PP3V3_S0_SDCARD 41
- =PP3V3_S0_SENSE 51 52 53 55
- =PP3V3_S0_SMBUS 50
- =PP3V3_S0_SMBUS_SMC 50
- =PP3V3_S0_SMBUS_TCON 50
- =PP3V3_S0_SMC 48 51 91
- =PP3V3_S0_TBTPWRCTL 38
- =PP3V3_S0_VRD 6 66 69 70 72 96 99
- =PP3V3_S0_SSD_PWR 51

110 PP3V3_S0_SSD MAKE_BASE=TRUE
- PP3V3_S0_SSD_SNS 51
- =PP3V3_S0_SSD 44

110 PP1V8_S0 MAKE_BASE=TRUE
- PP1V8_S0_REG 72
- =PP1V8_S0_CPU_PLL 13 16
- =PP1V8_S0_PCH 19
- =PP1V8_S0_PCH_VCC_DFTERM 22 24
- =PP1V8_S0_PCH_VCC_VRM 24
- =PP1V8_S0_PCH_CLK 26

110 PP1V5_S0 MAKE_BASE=TRUE
- PP1V5_S0_FET 74
- =PP1V5_S0_AUD_DIG 56
- =PP1V5_S0_CPU_MEM_PWR 51
- =PP1V5_S0_DP 75

110 PP1V5_S0_CPU_MEM MAKE_BASE=TRUE
- PP1V5_S0_CPU_MEM_SNS 51
- =PP1V5_S0_CPU_MEM 11 13 16

110 PPDDRVTT_S0 MAKE_BASE=TRUE
- PPDDRVTT_S0_LDO 72
- =PPDDRVTT_S0_CLAMP 28
- =PPDDRVTT_S0_MEM_A 29 30
- =PPDDRVTT_S0_MEM_B 31 32

110 PPDDRVREF_DQ_MEM_A_S3 MAKE_BASE=TRUE
- PPDDRVREF_DQ_MEM_A 34
- =PPDDRVREF_DQ_MEM_A 29 30

110 PPDDRVREF_CA_MEM_A_S3 MAKE_BASE=TRUE
- PPDDRVREF_CA_MEM_A 34
- =PPDDRVREF_CA_MEM_A 29 30

110 PPDDRVREF_DQ_MEM_B_S3 MAKE_BASE=TRUE
- PPDDRVREF_DQ_MEM_B 34
- =PPDDRVREF_DQ_MEM_B 31 32

110 PPDDRVREF_CA_MEM_B_S3 MAKE_BASE=TRUE
- PPDDRVREF_CA_MEM_B 34
- =PPDDRVREF_CA_MEM_B 31 32

100 PP1V05_S0_CPU MAKE_BASE=TRUE
- PP1V05_S0_CPU_REG 69
- =PPVCCIO_S0_CPU 10 11 13 16 28 66
- =PPVCCIO_S0_SMC 48
- =PPVCCIO_S0_XDP 25

100 PP1V05_S0 MAKE_BASE=TRUE
- PP1V05_S0_REG 99
- =PP1V05_S0_PCH_PWR 51
- =PP1V05_S0_P1V05TBTFET 38
- =PP1V05_S0_GPU_IFPCD_IOVDD 90
- =PP1V05_S0_GPU_IFPEF_IOVDD 90
- =PP1V05_S0_GPU_PEX_PLLVDD 83 95
- =PP1V05_S0_GPU_PEX_IOVDD 83

109 PPVCORE_S0_CPU MAKE_BASE=TRUE
- PPCPUCORE_S0_REG 67 68
- =PPVCORE_S0_CPU 13 16 51 66

109 PPVAXG_S0 MAKE_BASE=TRUE
- PPCPUAXG_S0_REG 17 68
- =PPVAXG_S0_CPU 13 17 51 66

108 PPVCCSA_S0 MAKE_BASE=TRUE
- PPVCCSA_S0_REG 70
- =PPVCCSA_S0_CPU 13 16

## Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

110 PP3V3_TBTLC MAKE_BASE=TRUE
- =PP3V3_TBTLC_FET 38
- =PP3V3_TBT_PCH_GPIO 15
- =PP3V3_TBTLC_RTR 15 36 37 38 50
- =PP3V3_TBT_CLK 26

100 38 PP1V05_TBTLC MAKE_BASE=TRUE
- =PP1V05_TBTLC_FET 38
- =PP1V05_TBTLC_RTR 37

100 PP1V05_TBTCIO MAKE_BASE=TRUE
- =PP1V05_TBTCIO_FET 38
- =PP1V05_TBTCIO_RTR 37

## Ground/Common

GND MAKE_BASE=TRUE

## GPU Rails (S0)

Enabled when system is in run

110 PPVCORE_S0_GPU MAKE_BASE=TRUE
- PPGPUCORE_S0_REG 97 98
- =PPVCORE_S0_GPU 51 93

110 PPFBVDDQ_S0_GPU MAKE_BASE=TRUE
- PP1V5R1V35_S0_GPU_REG 99 115
- =PP1V35_S0_GPU_FBVDDQ 94 84 85 86 87 88 89

100 PP1V05_S0_PCH MAKE_BASE=TRUE
- PP1V05_S0_PCH_SNS 51
- =PP1V05_S0_PCH 18
- =PP1V05_S0_PCH_VCCCLKDMI 22 24
- =PP1V05_S0_PCH_VCCIO_DMI 22 24
- =PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
- =PP1V05_S0_PCH_VCCIO_SATA 18 22 24
- =PP1V05_S0_PCH_VCCIO_USB 22 24
- =PP1V05_S0_PCH_VCC_ADPLL 17
- =PP1V05_S0_PCH_VCC_ASW 22 24
- =PP1V05_S0_PCH_VCC_CORE 22 24
- =PP1V05_S0_PCH_VCC_DIFFCLK 22 24
- =PP1V05_S0_PCH_VCC_DMI 22 24
- =PP1V05_S0_PCH_VCC_SSC 22 24
- =PP1V05_S0_PCH_V_PROC_IO 22 24

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# Power Connectors/Aliases

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D
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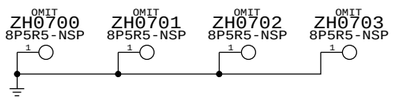
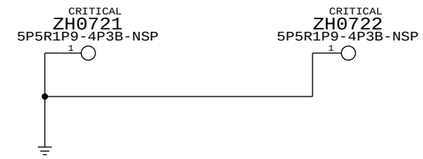
## CPU Heatsink

4MM PLATED HOLES (998-4158)



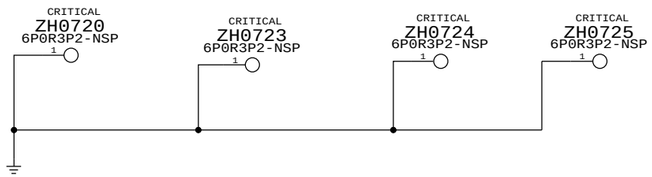

## WIRELESS CARD MTG HOLES

998-4938 (PLATED HOLES, 1.9MM INNER DIAMETER, 4.3MM PAD)



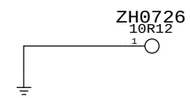

## GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



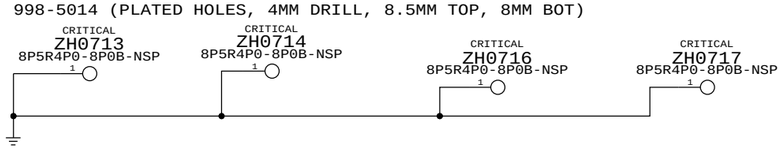

## HEATPIPE MTG HOLES

998-4640 (PLATED HOLES, 10MM DIA, 12MM PAD)



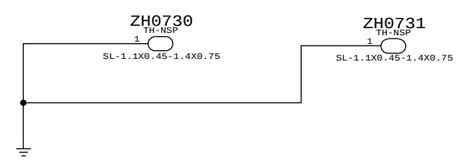

## Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



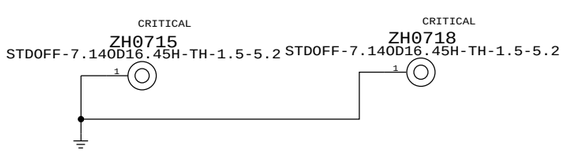

## USB CAN MTG HOLES

998-3975 (PLATED HOLES, 1.10MM X 0.45MM PAD)



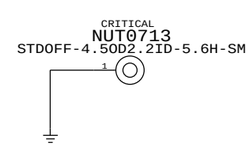

## Rear Cover

860-1487 (PCB STANDOFF)




## SSD STANDOFF

APN: 860-1461




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

REVISION: 6.1.0

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## CPU Reserved

| | | | |
|---|---|---|---|
| 10 | TP_CPU_RSVD<16..1> | NC_CPU_RSVD<16..1> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_CPU_RSVD<46..19> | NC_CPU_RSVD<46..19> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | CPU_CFG<15..12> | TP_CPU_CFG<15..12> | MAKE_BASE=TRUE |

## CPU Memory

| | | | |
|---|---|---|---|
| 12 | TP_MEM_A_DQ_CB<7..0> | NC_MEM_A_DQ_CB<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_A_DQS_N<8> | NC_MEM_A_DQSNX<8> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_A_DQS_P<8> | NC_MEM_A_DQSPX<8> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_B_DQ_CB<7..0> | NC_MEM_B_DQ_CB<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_B_DQS_N<8> | NC_MEM_B_DQSNX<8> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 12 | TP_MEM_B_DQS_P<8> | NC_MEM_B_DQSPX<8> | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH PCIe

| | | | |
|---|---|---|---|
| 18 | TP_PCIE1_D2RN | NC_PCIE1_D2RNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE1_D2RP | NC_PCIE1_D2RPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE1_R2D_CN | NC_PCIE1_R2D_CNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE1_R2D_CP | NC_PCIE1_R2D_CPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE2_D2RN | NC_PCIE2_D2RNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE2_D2RP | NC_PCIE2_D2RPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE2_R2D_CN | NC_PCIE2_R2D_CNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE2_R2D_CP | NC_PCIE2_R2D_PNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | DMI_MIDBUS_CLK100M_N | NC_DMI_MIDBUS_CLK100NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | DMI_MIDBUS_CLK100M_P | NC_DMI_MIDBUS_CLK100PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE0N | NC_PCIE_CLK100M_PE0NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE0P | NC_PCIE_CLK100M_PE0PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE4N | NC_PCIE_CLK100M_PE4NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE4P | NC_PCIE_CLK100M_PE4PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE5N | NC_PCIE_CLK100M_PE5NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCIE_CLK100M_PE5P | NC_PCIE_CLK100M_PE5PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCIE_CLK100M_PE6N | NC_PCIE_CLK100M_PE6NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCIE_CLK100M_PE6P | NC_PCIE_CLK100M_PE6PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCIE_CLK100M_PE7N | NC_PCIE_CLK100M_PE7NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCIE_CLK100M_PE7P | NC_PCIE_CLK100M_PE7PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_PE_TX_N<3..0> | NC_PE_TNX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_PE_TX_P<3..0> | NC_PE_TPX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_PE_RX_N<3..0> | NC_PE_RNX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_PE_RX_P<3..0> | NC_PE_RPX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH USB

| | | | |
|---|---|---|---|
| 20 | USB_PCH_4_N | NC_USB_PCH_4NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_4_P | NC_USB_PCH_4PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_5_N | NC_USB_PCH_5NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_5_P | NC_USB_PCH_5PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_6_N | NC_USB_PCH_6NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_6_P | NC_USB_PCH_6PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_11_N | NC_USB_PCH_11NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_11_P | NC_USB_PCH_11PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_12_N | NC_USB_PCH_12NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_12_P | NC_USB_PCH_12PX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_13_N | NC_USB_PCH_13NX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | USB_PCH_13_P | NC_USB_PCH_13PX | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH Clocks

| | | | |
|---|---|---|---|
| 18 | TP_PCH_CLKOUT_DPN | NC_PCH_CLKOUT_DPNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CLKOUT_DPP | NC_PCH_CLKOUT_DPPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | PCH_CLK25M_XTALOUT | NC_PCH_CLK25M_XTALOUT | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_GPIO64_CLKOUTFLEX0 | NC_PCH_GPIO64_CLKOUTFLEX0 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_GPIO65_CLKOUTFLEX1 | NC_PCH_GPIO65_CLKOUTFLEX1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_GPIO66_CLKOUTFLEX2 | NC_PCH_GPIO66_CLKOUTFLEX2 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_GPIO67_CLKOUTFLEX3 | NC_PCH_GPIO67_CLKOUTFLEX3 | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH Unused Display

| | | | |
|---|---|---|---|
| 19 | TP_CRT_IG_RED | NC_CRT_IG_RED | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_GREEN | NC_CRT_IG_GREEN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_BLUE | NC_CRT_IG_BLUE | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_HSYNC | NC_CRT_IG_HSYNC | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_VSYNC | NC_CRT_IG_VSYNC | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_DDC_CLK | NC_CRT_IG_DDC_CLK | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_CRT_IG_DDC_DATA | NC_CRT_IG_DDC_DATA | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_B_MLN<3..0> | NC_DP_IG_B_MLNX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_B_MLP<3..0> | NC_DP_IG_B_MLPX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_B_AUX_N | NC_DP_IG_B_AUXNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_B_AUX_P | NC_DP_IG_B_AUXPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_B_HPD | NC_DP_IG_B_HPD | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_B_DDC_CLK | NC_DP_IG_B_CTRL_CLK | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_B_DDC_DATA | NC_DP_IG_B_CTRL_DATA | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_C_MLN<3..0> | NC_DP_IG_C_MLNX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_C_MLP<3..0> | NC_DP_IG_C_MLPX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_C_AUX_N | NC_DP_IG_C_AUXNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_C_AUX_P | NC_DP_IG_C_AUXPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_C_HPD | NC_DP_IG_C_HPD | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_C_CTRL_CLK | NC_DP_IG_C_CTRL_CLK | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_C_CTRL_DATA | NC_DP_IG_C_CTRL_DATA | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_D_MLN<3..0> | NC_DP_IG_D_MLNX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_D_MLP<3..0> | NC_DP_IG_D_MLPX<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_D_AUXN | NC_DP_IG_D_AUXNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_D_AUXP | NC_DP_IG_D_AUXPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_D_HPD | NC_DP_IG_D_HPD | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_D_CTRL_CLK | NC_DP_IG_D_CTRL_CLK | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | DP_IG_D_CTRL_DATA | NC_DP_IG_D_CTRL_DATA | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_TVCLKINN | NC_SDVO_TVCLKINNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_TVCLKINP | NC_SDVO_TVCLKINPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_STALLN | NC_SDVO_STALLNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_STALLP | NC_SDVO_STALLPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_INTN | NC_SDVO_INTNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_SDVO_INTP | NC_SDVO_INTPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_L_BKLTCTL | NC_PCH_L_BKLTCTL | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_L_BKLTEN | NC_PCH_L_BKLTEN | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_L_VDD_EN | NC_PCH_L_VDD_EN | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH SATA

| | | | |
|---|---|---|---|
| 18 | TP_SATA_C_R2D_CN | NC_SATA_C_R2D_CNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_C_R2D_CP | NC_SATA_C_R2D_CPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_C_D2RN | NC_SATA_C_D2RNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_C_D2RP | NC_SATA_C_D2RPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_D_R2D_CN | NC_SATA_D_R2D_CNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_D_R2D_CP | NC_SATA_D_R2D_CPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_D_D2RN | NC_SATA_D_D2RNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_D_D2RP | NC_SATA_D_D2RPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_E_R2D_CN | NC_SATA_E_R2D_CNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_E_R2D_CP | NC_SATA_E_R2D_CPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_E_D2RN | NC_SATA_E_D2RNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_E_D2RP | NC_SATA_E_D2RPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_F_R2D_CN | NC_SATA_F_R2D_CNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_F_R2D_CP | NC_SATA_F_R2D_CPX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_F_D2RN | NC_SATA_F_D2RNX | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_SATA_F_D2RP | NC_SATA_F_D2RPX | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH Reserved

| | | | |
|---|---|---|---|
| 19 | TP_PCH_RESERVE_0 | NC_PCH_RESERVE_0 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_1 | NC_PCH_RESERVE_1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_2 | NC_PCH_RESERVE_2 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_3 | NC_PCH_RESERVE_3 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_4 | NC_PCH_RESERVE_4 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_5 | NC_PCH_RESERVE_5 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_6 | NC_PCH_RESERVE_6 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_7 | NC_PCH_RESERVE_7 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_8 | NC_PCH_RESERVE_8 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_9 | NC_PCH_RESERVE_9 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_10 | NC_PCH_RESERVE_10 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_11 | NC_PCH_RESERVE_11 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_12 | NC_PCH_RESERVE_12 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_13 | NC_PCH_RESERVE_13 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_14 | NC_PCH_RESERVE_14 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_15 | NC_PCH_RESERVE_15 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_16 | NC_PCH_RESERVE_16 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_17 | NC_PCH_RESERVE_17 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_18 | NC_PCH_RESERVE_18 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_19 | NC_PCH_RESERVE_19 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_20 | NC_PCH_RESERVE_20 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_21 | NC_PCH_RESERVE_21 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_22 | NC_PCH_RESERVE_22 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_23 | NC_PCH_RESERVE_23 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_24 | NC_PCH_RESERVE_24 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_25 | NC_PCH_RESERVE_25 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_26 | NC_PCH_RESERVE_26 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_27 | NC_PCH_RESERVE_27 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_RESERVE_28 | NC_PCH_RESERVE_28 | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH and CPU FDI

| | | | |
|---|---|---|---|
| 10 | TP_CPU_FDI_TX_N<7..0> | NC_CPU_FDI_TNX<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_CPU_FDI_TX_P<7..0> | NC_CPU_FDI_TPX<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | PCH_FDI_RX_N<7..0> | NC_PCH_FDI_RNX<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | PCH_FDI_RX_P<7..0> | NC_PCH_FDI_RPX<7..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_CPU_FDI_FSYNC<1..0> | NC_CPU_FDI_FSYNC<1..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_CPU_FDI_LSYNC<1..0> | NC_CPU_FDI_LSYNC<1..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 10 | TP_CPU_FDI_INT | NC_CPU_FDI_INT | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | PCH_FDI_FSYNC<1..0> | NC_PCH_FDI_FSYNC<1..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | PCH_FDI_LSYNC<1..0> | NC_PCH_FDI_LSYNC<1..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | PCH_FDI_INT | NC_PCH_FDI_INT | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH Test Points

| | | | |
|---|---|---|---|
| 21 | TP_PCH_TP1 | NC_PCH_TP1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP2 | NC_PCH_TP2 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP3 | NC_PCH_TP3 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP4 | NC_PCH_TP4 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP5 | NC_PCH_TP5 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP6 | NC_PCH_TP6 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP7 | NC_PCH_TP7 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP8 | NC_PCH_TP8 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP9 | NC_PCH_TP9 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP10 | NC_PCH_TP10 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP11 | NC_PCH_TP11 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP12 | NC_PCH_TP12 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP13 | NC_PCH_TP13 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP14 | NC_PCH_TP14 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP15 | NC_PCH_TP15 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP16 | NC_PCH_TP16 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP17 | NC_PCH_TP17 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP18 | NC_PCH_TP18 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP19 | NC_PCH_TP19 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_TP20 | NC_PCH_TP20 | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH PCI

| | | | |
|---|---|---|---|
| 20 | TP_PCI_AD<31..0> | NC_PCI_AD<31..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCI_C_BE_L<3..0> | NC_PCI_C_BE_L<3..0> | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCI_PAR | NC_PCI_PAR | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCI_RESET_L | NC_PCI_RESET_L | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCH_PCI_GNT0_L | NC_PCI_GNT0_L | MAKE_BASE=TRUE NO_TEST=TRUE |
| 19 | TP_PCH_INIT3V3_L | NC_PCH_INIT3V3_L | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_LPC_DREQ0_L | NC_LPC_DREQ0_L | MAKE_BASE=TRUE NO_TEST=TRUE |

## PCH Miscellaneous

| | | | |
|---|---|---|---|
| 18 | TP_HDA_SDIN1 | NC_HDA_SDIN1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_HDA_SDIN2 | NC_HDA_SDIN2 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_HDA_SDIN3 | NC_HDA_SDIN3 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_PWM0 | NC_PCH_PWM0 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_PWM1 | NC_PCH_PWM1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_PWM2 | NC_PCH_PWM2 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_PWM3 | NC_PCH_PWM3 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 21 | TP_PCH_SST | NC_PCH_SST | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CL_CLK1 | NC_PCH_CL_CLK1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CL_DATA1 | NC_PCH_CL_DATA1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 18 | TP_PCH_CL_RST1 | NC_PCH_CL_RST1 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCI_CLK33M_OUT2 | NC_PCI_CLK33M_OUT2 | MAKE_BASE=TRUE NO_TEST=TRUE |
| 20 | TP_PCI_CLK33M_OUT3 | NC_PCI_CLK33M_OUT3 | MAKE_BASE=TRUE NO_TEST=TRUE |

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PAGE TITLE
# Unused Signal Aliases

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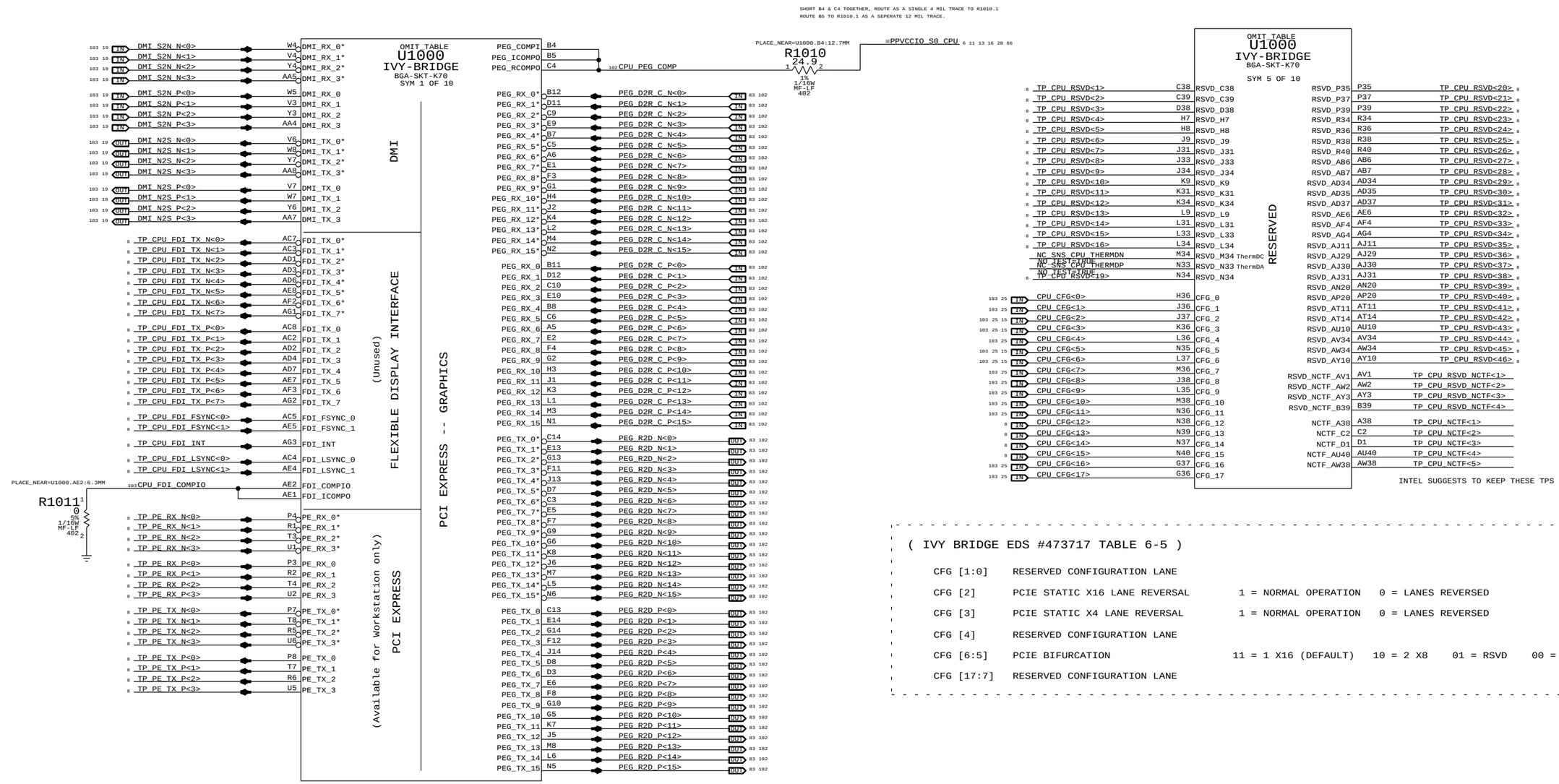


( IVY BRIDGE EDS #473717 TABLE 6-5 )

| | | | | | |
|---|---|---|---|---|---|
| CFG [1:0] | RESERVED CONFIGURATION LANE | | | | |
| CFG [2] | PCIE STATIC X16 LANE REVERSAL | 1 = NORMAL OPERATION | 0 = LANES REVERSED | | |
| CFG [3] | PCIE STATIC X4 LANE REVERSAL | 1 = NORMAL OPERATION | 0 = LANES REVERSED | | |
| CFG [4] | RESERVED CONFIGURATION LANE | | | | |
| CFG [6:5] | PCIE BIFURCATION | 11 = 1 X16 (DEFAULT) | 10 = 2 X8 | 01 = RSVD | 00 = 1 X8, 2 X4 |
| CFG [17:7] | RESERVED CONFIGURATION LANE | | | | |

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# CPU DMI/PEG/FDI/RSVD

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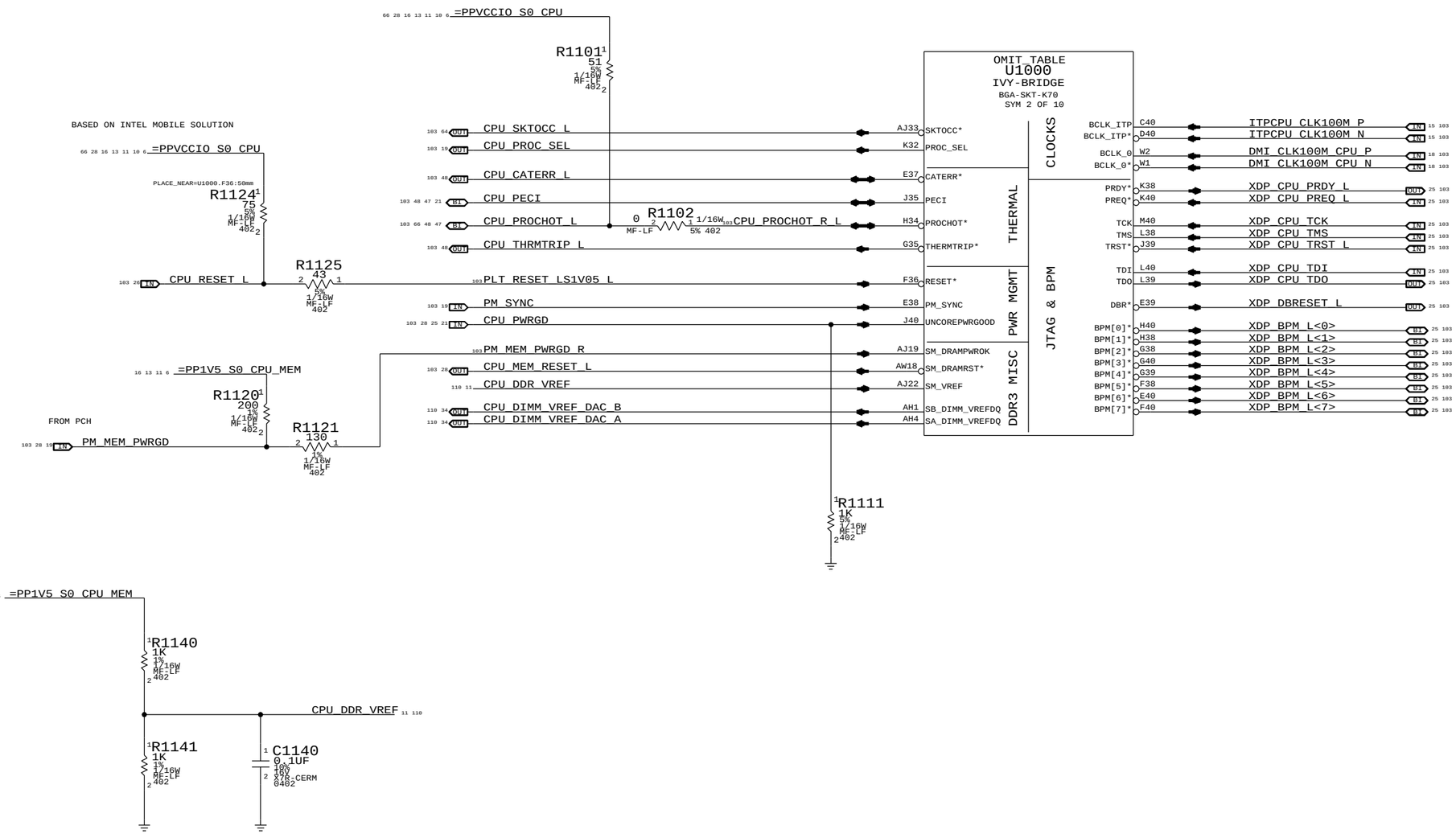


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# CPU CLOCK/MISC/JTAG

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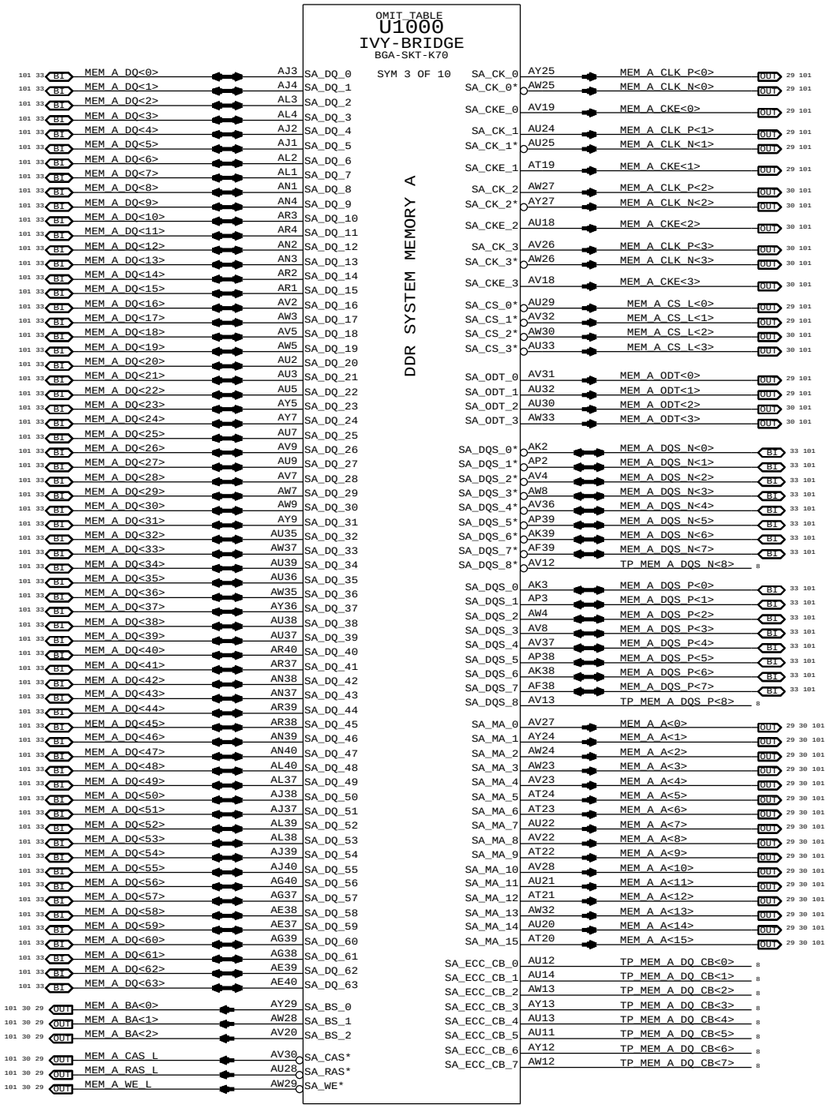


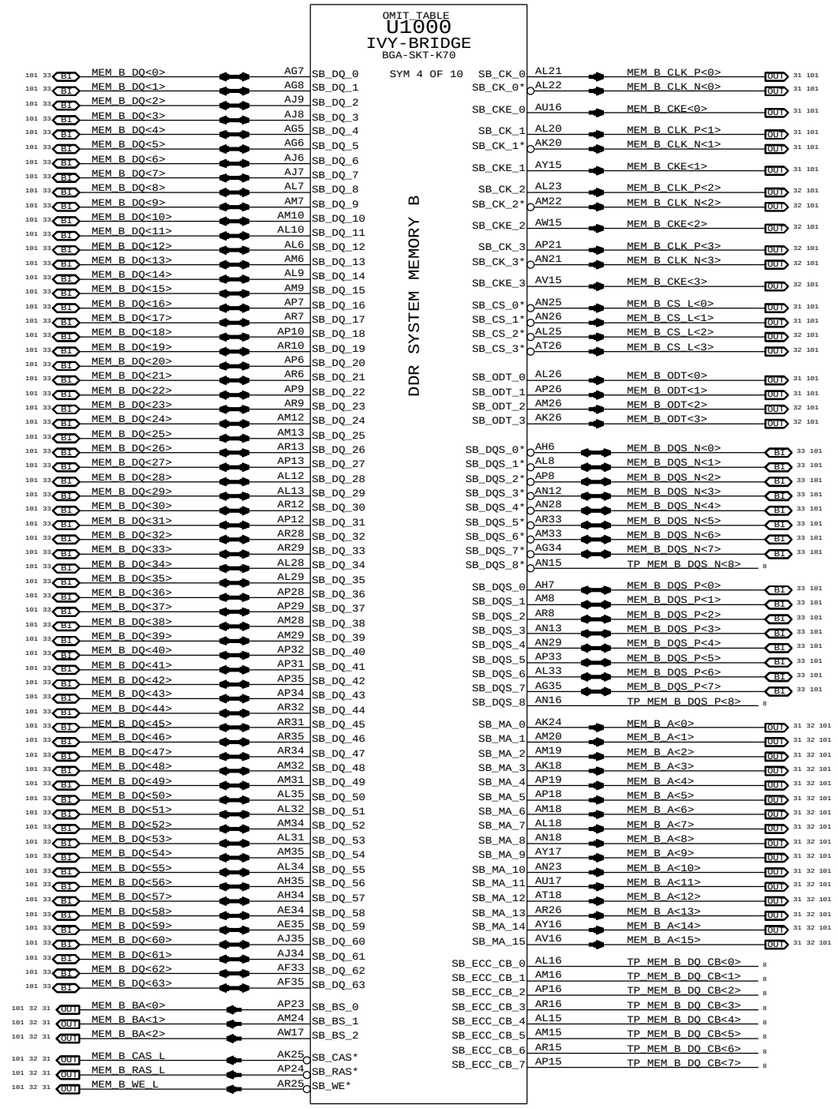


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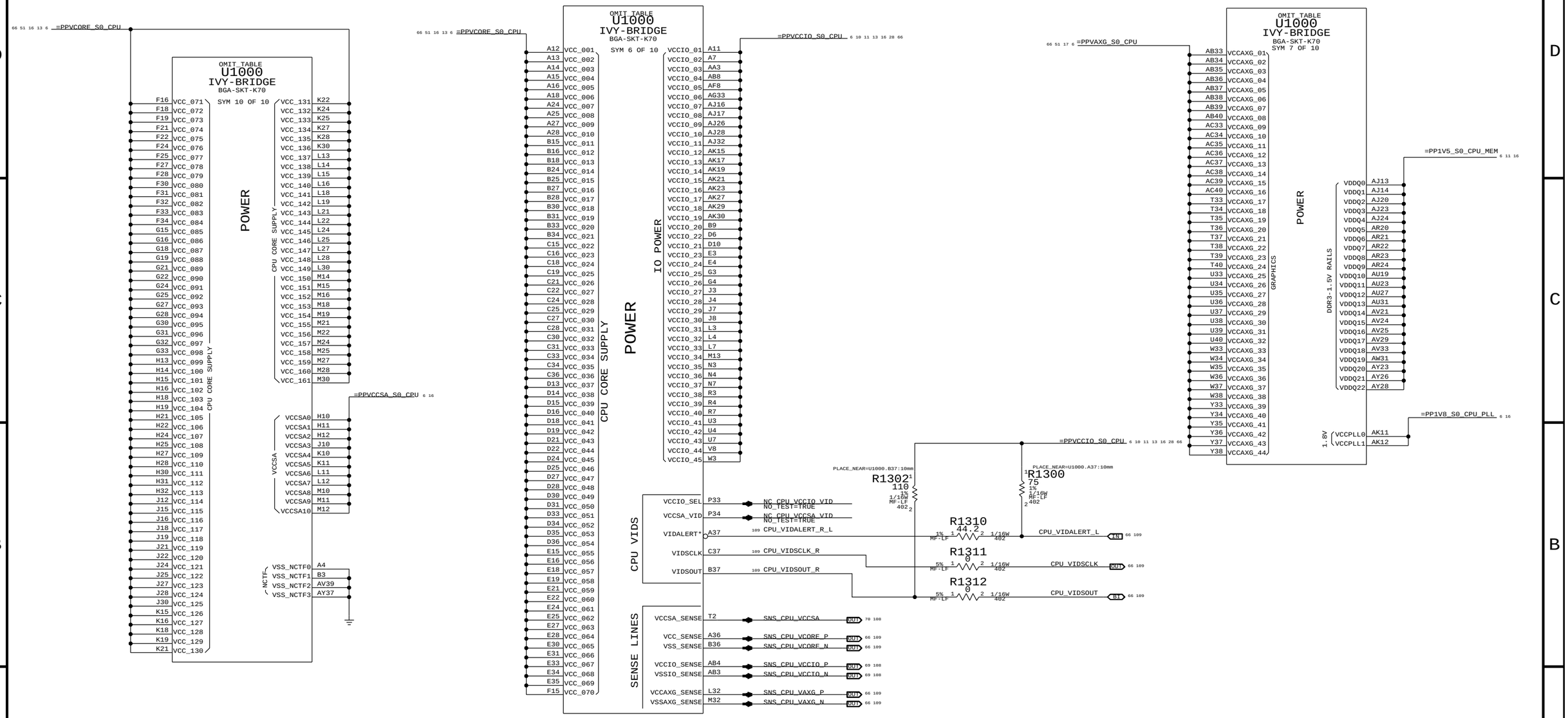


| | |
|---|---|
| SYNC_MASTER=D8_MLB | SYNC_DATE=07/03/2012 |
| PAGE TITLE | CPU POWER |
| Apple Inc. | DRAWING NUMBER 051-9505 SIZE D |
| | REVISION 6.1.0 |
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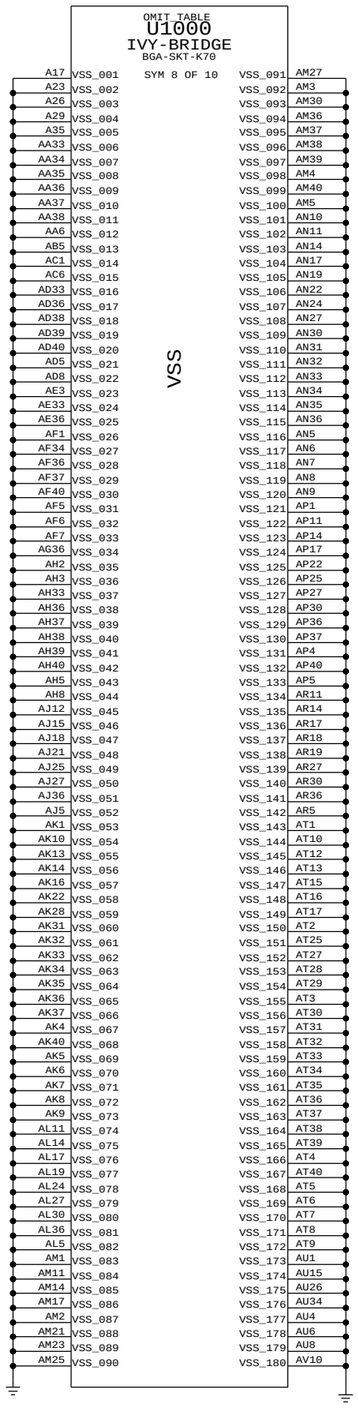


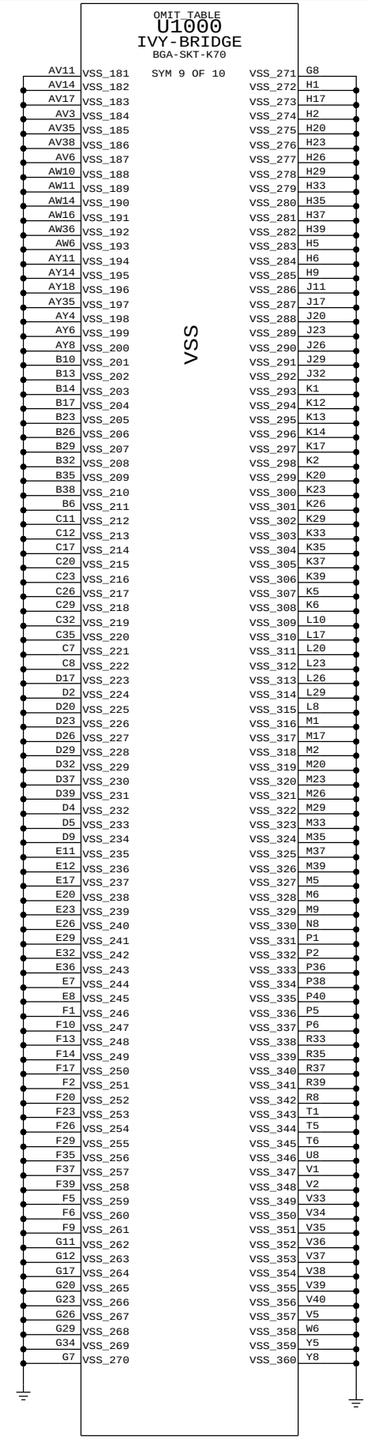


SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE

# CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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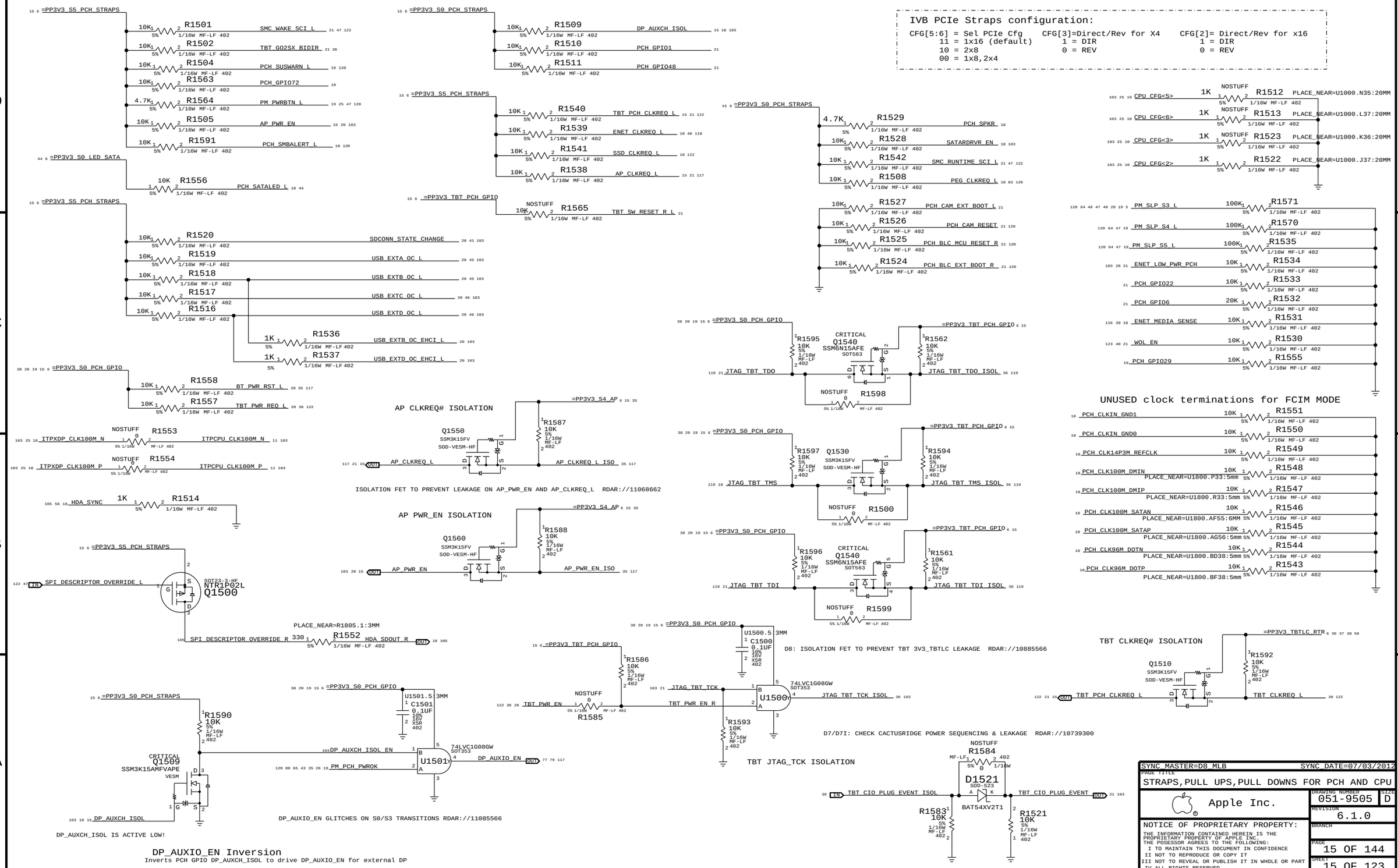
IVB PCIe Straps configuration:
CFG[5:6] = Sel PCIe Cfg
11 = 1x16 (default)
10 = 2x8
00 = 1x8,2x4
CFG[3]=Direct/Rev for X4
1 = DIR
0 = REV
CFG[2]= Direct/Rev for x16
1 = DIR
0 = REV
=PP3V3_S5_PCH_STRAPS
R1501 10K SMC_WAKE_SCI_L
R1502 10K TBT_GO2SX_BIDIR
R1504 10K PCH_SUSWARN_L
R1563 10K PCH_GPIO72
R1564 4.7K PM_PWRBTN_L
R1505 10K AP_PWR_EN
R1591 10K PCH_SMBALERT_L
=PP3V3_S0_PCH_STRAPS
R1509 10K DP_AUXCH_ISOL
R1510 10K PCH_GPIO1
R1511 10K PCH_GPIO48
=PP3V3_S5_PCH_STRAPS
R1540 10K TBT_PCH_CLKREQ_L
R1539 10K ENET_CLKREQ_L
R1541 10K SSD_CLKREQ_L
R1538 10K AP_CLKREQ_L
=PP3V3_TBT_PCH_GPIO
R1565 NOSTUFF 10K TBT_SW_RESET_R_L
=PP3V3_S0_PCH_STRAPS
R1529 4.7K PCH_SPKR
R1528 10K SATARDRVR_EN
R1542 10K SMC_RUNTIME_SCI_L
R1508 10K PEG_CLKREQ_L
R1527 10K PCH_CAM_EXT_BOOT_L
R1526 10K PCH_CAM_RESET
R1525 10K PCH_BLC_MCU_RESET_R
R1524 10K PCH_BLC_EXT_BOOT_R
R1512 NOSTUFF 1K CPU_CFG<5> PLACE_NEAR=U1000.N35:20MM
R1513 NOSTUFF 1K CPU_CFG<6> PLACE_NEAR=U1000.L37:20MM
R1523 NOSTUFF 1K CPU_CFG<3> PLACE_NEAR=U1000.K36:20MM
R1522 1K CPU_CFG<2> PLACE_NEAR=U1000.J37:20MM
=PP3V3_S0_LED_SATA
R1556 10K PCH_SATALED_L
=PP3V3_S5_PCH_STRAPS
R1520 10K SDCONN_STATE_CHANGE
R1519 10K USB_EXTA_OC_L
R1518 10K USB_EXTB_OC_L
R1517 10K USB_EXTC_OC_L
R1516 10K USB_EXTD_OC_L
R1536 1K USB_EXTB_OC_EHCI_L
R1537 1K USB_EXTD_OC_EHCI_L
R1571 100K PM_SLP_S3_L
R1570 100K PM_SLP_S4_L
R1535 100K PM_SLP_S5_L
R1534 10K ENET_LOW_PWR_PCH
R1533 10K PCH_GPIO22
R1532 20K PCH_GPIO6
R1531 10K ENET_MEDIA_SENSE
R1530 10K WOL_EN
R1555 10K PCH_GPIO29
=PP3V3_S0_PCH_GPIO
R1558 10K BT_PWR_RST_L
R1557 10K TBT_PWR_REQ_L
R1553 NOSTUFF 0 ITPXDP_CLK100M_N ITPCPU_CLK100M_N
R1554 NOSTUFF 0 ITPXDP_CLK100M_P ITPCPU_CLK100M_P
HDA_SYNC 1K R1514
AP CLKREQ# ISOLATION
Q1550 SSM3K15FV SOD-VESM-HF
R1587 10K =PP3V3_S4_AP
AP_CLKREQ_L AP_CLKREQ_L_ISO
ISOLATION FET TO PREVENT LEAKAGE ON AP_PWR_EN AND AP_CLKREQ_L RDAR://11068662
AP PWR_EN ISOLATION
Q1560 SSM3K15FV SOD-VESM-HF
R1588 10K =PP3V3_S4_AP
AP_PWR_EN AP_PWR_EN_ISO
R1595 10K JTAG_TBT_TDO
CRITICAL Q1540 SSM6N15AFE SOT563
R1598 NOSTUFF 0
R1562 10K =PP3V3_TBT_PCH_GPIO JTAG_TBT_TDO_ISOL
R1597 10K JTAG_TBT_TMS
Q1530 SSM3K15FV SOD-VESM-HF
R1500 NOSTUFF 0
R1594 10K =PP3V3_TBT_PCH_GPIO JTAG_TBT_TMS_ISOL
R1596 10K JTAG_TBT_TDI
CRITICAL Q1540 SSM6N15AFE SOT563
R1599 NOSTUFF 0
R1561 10K =PP3V3_TBT_PCH_GPIO JTAG_TBT_TDI_ISOL
UNUSED clock terminations for FCIM MODE
R1551 10K PCH_CLKIN_GND1
R1550 10K PCH_CLKIN_GND0
R1549 10K PCH_CLK14P3M_REFCLK
R1548 10K PCH_CLK100M_DMIN PLACE_NEAR=U1800.P33:5mm
R1547 10K PCH_CLK100M_DMIP PLACE_NEAR=U1800.R33:5mm
R1546 10K PCH_CLK100M_SATAN PLACE_NEAR=U1800.AF55:6MM
R1545 10K PCH_CLK100M_SATAP PLACE_NEAR=U1800.AG56:5mm
R1544 10K PCH_CLK96M_DOTN PLACE_NEAR=U1800.BD38:5mm
R1543 10K PCH_CLK96M_DOTP PLACE_NEAR=U1800.BF38:5mm
=PP3V3_S5_PCH_STRAPS
Q1500 NTR1P02L SOT23-3-HF
SPI_DESCRIPTOR_OVERRIDE_L
PLACE_NEAR=R1805.1:3MM
R1552 330 SPI_DESCRIPTOR_OVERRIDE_R HDA_SDOUT_R
D8: ISOLATION FET TO PREVENT TBT 3V3_TBTLC LEAKAGE RDAR://10885566
U1500.5 3MM C1500 0.1UF
=PP3V3_S0_PCH_GPIO
=PP3V3_TBT_PCH_GPIO
R1586 10K
NOSTUFF R1585 TBT_PWR_EN
JTAG_TBT_TCK
TBT_PWR_EN_R
U1500 74LVC1G08GW SOT353
JTAG_TBT_TCK_ISOL
R1593 10K
TBT JTAG_TCK ISOLATION
TBT CLKREQ# ISOLATION
Q1510 SSM3K15FV SOD-VESM-HF
R1592 10K =PP3V3_TBTLC_RTR
TBT_PCH_CLKREQ_L TBT_CLKREQ_L
=PP3V3_S0_PCH_STRAPS
R1590 10K
CRITICAL Q1509 SSM3K15AMFVAPE VESM
DP_AUXCH_ISOL
DP_AUXCH_ISOL IS ACTIVE LOW!
U1501.5 3MM C1501 0.1UF
DP_AUXCH_ISOL_EN
PM_PCH_PWROK
U1501 74LVC1G08GW SOT353
DP_AUXIO_EN
DP_AUXIO_EN GLITCHES ON S0/S3 TRANSITIONS RDAR://11085566
DP_AUXIO_EN Inversion
Inverts PCH GPIO DP_AUXCH_ISOL to drive DP_AUXIO_EN for external DP
D7/D7I: CHECK CACTUSRIDGE POWER SEQUENCING & LEAKAGE RDAR://10739300
R1584 NOSTUFF
D1521 SOD-523 BAT54XV2T1
TBT_CIO_PLUG_EVENT_ISOL TBT_CIO_PLUG_EVENT
R1583 10K
R1521 10K
SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012
PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU
Apple Inc.
DRAWING NUMBER 051-9505
SIZE D
REVISION 6.1.0
BRANCH
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## CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613):

REPLACED WITH 603 PER RDAR://10700439

16 13 6 66 51 =PPVCORE_S0_CPU

C1600 22UF 20% 6.3V X5R-CERM2 0603
C1601 22UF 20% 6.3V X5R-CERM2 0603
C1602 22UF 20% 6.3V X5R-CERM2 0603
C1603 22UF 20% 6.3V X5R-CERM2 0603
C1604 22UF 20% 6.3V X5R-CERM2 0603
C1605 22UF 20% 6.3V X5R-CERM2 0603
C1606 22UF 20% 6.3V X5R-CERM2 0603
C1607 22UF 20% 6.3V X5R-CERM2 0603
C1608 22UF 20% 6.3V X5R-CERM2 0603
C1609 22UF 20% 6.3V X5R-CERM2 0603

C1610 22UF 20% 6.3V X5R-CERM2 0603
C1611 22UF 20% 6.3V X5R-CERM2 0603
C1612 22UF 20% 6.3V X5R-CERM2 0603
C1613 22UF 20% 6.3V X5R-CERM2 0603

BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS

66 51 16 13 6 =PPVCORE_S0_CPU

**Place inside socket cavity**

C1620 10UF 20% 16V X5R 603
C1621 10UF 20% 16V X5R 603
C1622 10UF 20% 16V X5R 603
C1623 10UF 20% 16V X5R 603
C1624 10UF 20% 16V X5R 603
C1625 10UF 20% 16V X5R 603
C1626 10UF 20% 16V X5R 603
C1627 10UF 20% 16V X5R 603
C1628 10UF 20% 16V X5R 603
C1629 10UF 20% 16V X5R 603

C1630 1UF 10% 16V X5R 402
C1631 1UF 10% 16V X5R 402
C1632 1UF 10% 16V X5R 402
C1633 1UF 10% 16V X5R 402
C1634 1UF 10% 16V X5R 402
C1635 1UF 10% 16V X5R 402
C1636 1UF 10% 16V X5R 402
C1637 1UF 10% 16V X5R 402
C1638 1UF 10% 16V X5R 402
C1639 1UF 10% 16V X5R 402

## CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 66 28 =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

C1650 22UF 20% 6.3V X5R-CERM2 0603
C1651 22UF 20% 6.3V X5R-CERM2 0603
C1652 22UF 20% 6.3V X5R-CERM2 0603
C1653 22UF 20% 6.3V X5R-CERM2 0603
C1654 22UF 20% 6.3V X5R-CERM2 0603
C1655 22UF 20% 6.3V X5R-CERM2 0603
C1656 22UF 20% 6.3V X5R-CERM2 0603
C1657 22UF 20% 6.3V X5R-CERM2 0603

PLACEMENT_NOTE (C1660-C1665):

**Place at edge of socket.**

C1660 10UF 20% 6.3V X5R 603
C1661 10UF 20% 6.3V X5R 603
C1662 10UF 20% 6.3V X5R 603
C1663 10UF 20% 6.3V X5R 603
C1664 10UF 20% 6.3V X5R 603
C1665 10UF 20% 6.3V X5R 603

BULK CAPS ON CPU VREG PAGE 74

CRITICAL
C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

## CPU VCCSA DECOUPLING

2x 10uF 0603. INTEL RECOMMENDATION 2X 10uF 0805

13 6 =PPVCCSA_S0_CPU

C1666 10UF 20% 6.3V X5R 603
C1667 10UF 20% 6.3V X5R 603

Bulk decoupling is on VCCSA reg page 75

## Memory (CPU VCCDDR) DECOUPLING

13 11 6 =PP1V5_S0_CPU_MEM

C1676 22UF 20% 6.3V X5R-CERM2 0603
C1677 22UF 20% 6.3V X5R-CERM2 0603
C1678 22UF 20% 6.3V X5R-CERM2 0603
C1679 22UF 20% 6.3V X5R-CERM2 0603
C1680 22UF 20% 6.3V X5R-CERM2 0603
C1681 22UF 20% 6.3V X5R-CERM2 0603
C1682 1UF 10% 6.3V X5R 0201
C1683 1UF 20% 6.3V X5R 0201
C1684 1UF 20% 6.3V X5R 0201
C1685 1UF 20% 6.3V X5R 0201
C1686 1UF 20% 6.3V X5R 0201

CRITICAL
NOSTUFF
C1687 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

## PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 1x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1692 2.2UF 10% 6.3V X5R 402
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1695 10UF 20% 6.3V X5R 603
C1690 22UF 20% 6.3V X5R-CERM2 0603
C1696 47UF 20% 6.3V X5R 0805
C1697 47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 77

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D
REVISION 6.1.0
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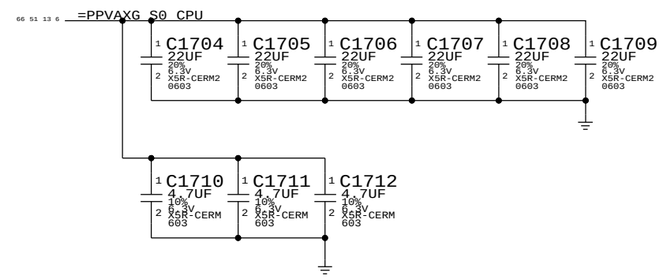
# VAXG DECOUPLING

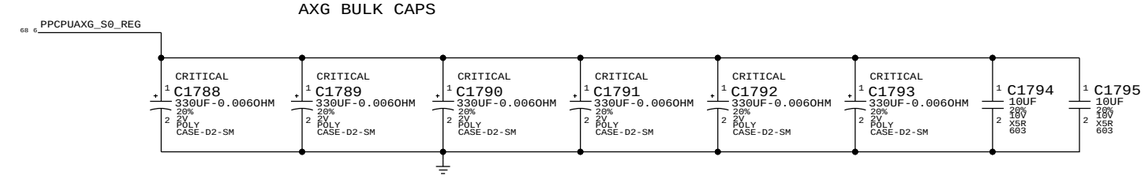
INTEL RECOMMENDATION 4X22UF 0805,3X 4.7UF

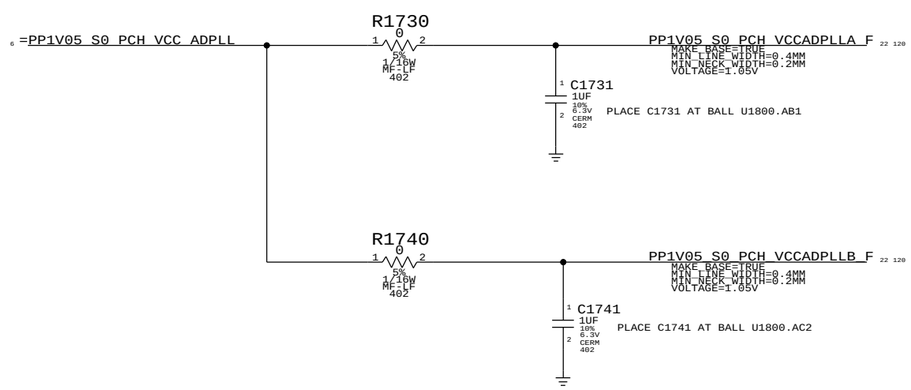
PLACEMENT_NOTE (C1704-C1709):

**Place inside socket cavity**




AXG BULK CAPS






SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
GFX DECOUPLING & PCH PWR ALIAS

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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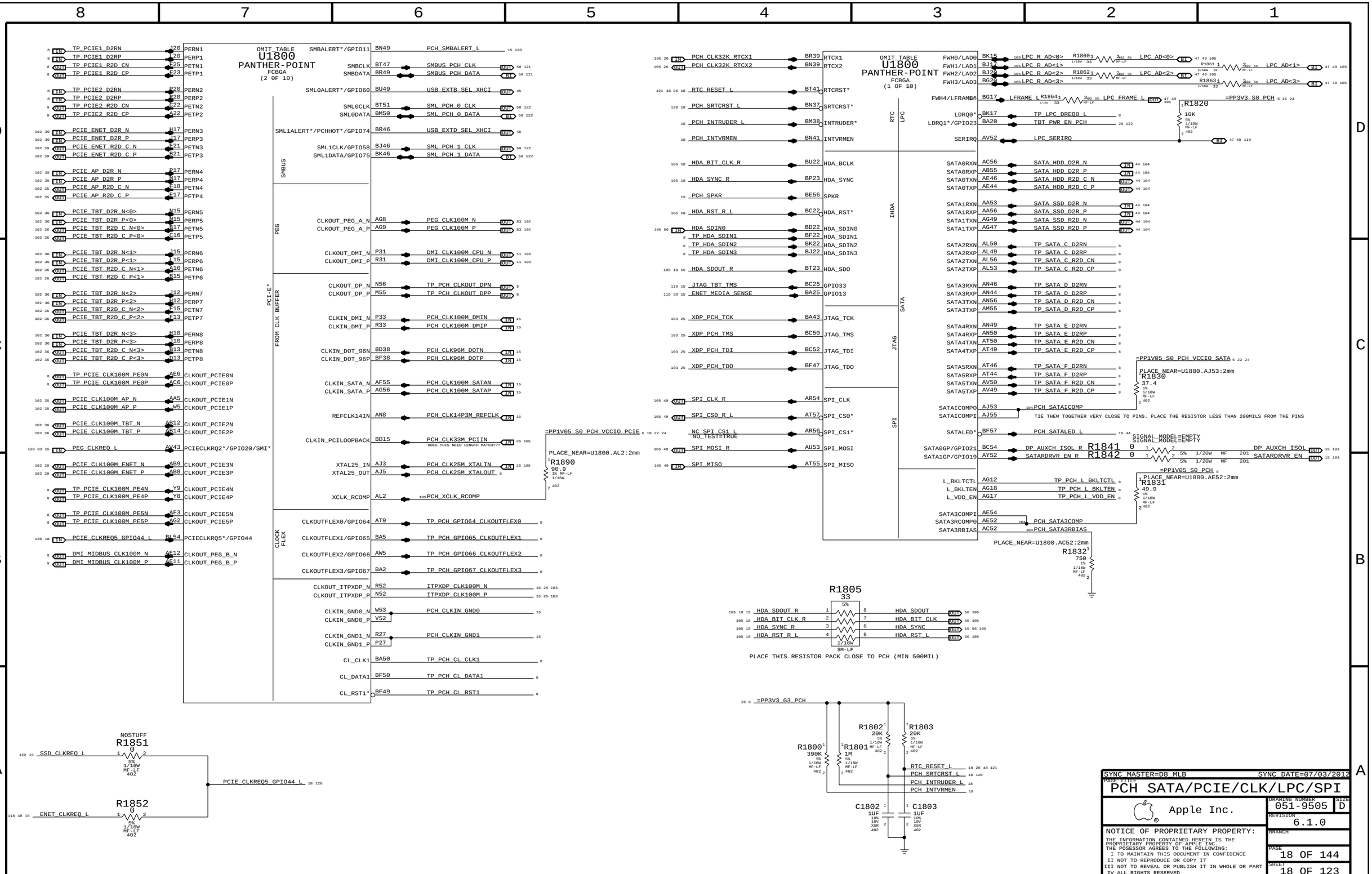
OMIT TABLE
U1800
PANTHER-POINT
FCBGA
(2 OF 10)
OMIT TABLE
U1800
PANTHER-POINT
FCBGA
(1 OF 10)
PCI-E*
FROM CLK BUFFER
SMBUS
PEG
CLOCK FLEX
RTC
LPC
IHDA
SATA
JTAG
SPI
TP_PCIE1_D2RN
TP_PCIE1_D2RP
TP_PCIE1_R2D_CN
TP_PCIE1_R2D_CP
TP_PCIE2_D2RN
TP_PCIE2_D2RP
TP_PCIE2_R2D_CN
TP_PCIE2_R2D_CP
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<0>
PCIE_TBT_R2D_C_N<0>
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PCIE_TBT_D2R_P<1>
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PCIE_TBT_D2R_P<2>
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PCIE_TBT_R2D_C_P<2>
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
TP_PCIE_CLK100M_PE0N
TP_PCIE_CLK100M_PE0P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PEG_CLKREQ_L
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCIE_CLKREQ5_GPIO44_L
DMI_MIDBUS_CLK100M_N
DMI_MIDBUS_CLK100M_P
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20/SMI*
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKIN_GND0_N
CLKIN_GND0_P
CLKIN_GND1_N
CLKIN_GND1_P
CL_CLK1
CL_DATA1
CL_RST1*
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
PEG_CLK100M_N
PEG_CLK100M_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCH_CLK100M_DMIN
PCH_CLK100M_DMIP
PCH_CLK96M_DOTN
PCH_CLK96M_DOTP
PCH_CLK100M_SATAN
PCH_CLK100M_SATAP
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
DOES THIS NEED LENGTH MATCH???
PCH_CLK25M_XTALIN
PCH_CLK25M_XTALOUT
PCH_XCLK_RCOMP
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
PCH_CLKIN_GND0
PCH_CLKIN_GND1
TP_PCH_CL_CLK1
TP_PCH_CL_DATA1
TP_PCH_CL_RST1
=PP1V05_S0_PCH_VCCIO_PCIE
PLACE_NEAR=U1800.AL2:2mm
R1890
90.9
1% MF-LF
1/16W
402
PCH_CLK32K_RTCX1
PCH_CLK32K_RTCX2
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_TBT_TMS
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
NC_SPI_CS1_L
NO_TEST=TRUE
SPI_MOSI_R
SPI_MISO
RTCX1
RTCX2
RTCRST*
SRTCRST*
INTRUDER*
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST*
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
GPIO33
GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI_CLK
SPI_CS0*
SPI_CS1*
SPI_MOSI
SPI_MISO
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME*
LDRQ0*
LDRQ1*/GPIO23
SERIRQ
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED*
SATA0GP/GPIO21
SATA1GP/GPIO19
L_BKLTCTL
L_BKLTEN
L_VDD_EN
SATA3COMPI
SATA3RCOMP0
SATA3RBIAS
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
R1860
R1861
R1862
R1863
LFRAME_L
R1864
LPC_FRAME_L
=PP3V3_S0_PCH
R1820
10K
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_SSD_D2R_N
SATA_SSD_D2R_P
SATA_SSD_R2D_N
SATA_SSD_R2D_P
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.AJ53:2mm
R1830
37.4
PCH_SATAICOMP
TIE THEM TOGETHER VERY CLOSE TO PINS. PLACE THE RESISTOR LESS THAN 200MILS FROM THE PINS
PCH_SATALED_L
SIGNAL_MODEL=EMPTY
DP_AUXCH_ISOL_R
SATARDRVR_EN_R
R1841
R1842
DP_AUXCH_ISOL
SATARDRVR_EN
=PP1V05_S0_PCH
PLACE_NEAR=U1800.AE52:2mm
R1831
49.9
TP_PCH_L_BKLTCTL
TP_PCH_L_BKLTEN
TP_PCH_L_VDD_EN
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AC52:2mm
R1832
750
R1805
33
5%
HDA_SDOUT_R
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
HDA_SDOUT
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
1/16W
SM-LF
PLACE THIS RESISTOR PACK CLOSE TO PCH (MIN 500MIL)
=PP3V3_G3_PCH
R1800
390K
R1801
1M
R1802
20K
R1803
20K
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN
C1802
1UF
C1803
1UF
NOSTUFF
R1851
0
SSD_CLKREQ_L
R1852
0
ENET_CLKREQ_L
PCIE_CLKREQ5_GPIO44_L
SYNC_MASTER=D8_MLB
SYNC_DATE=07/03/2012
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
D
REVISION
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18 OF 123
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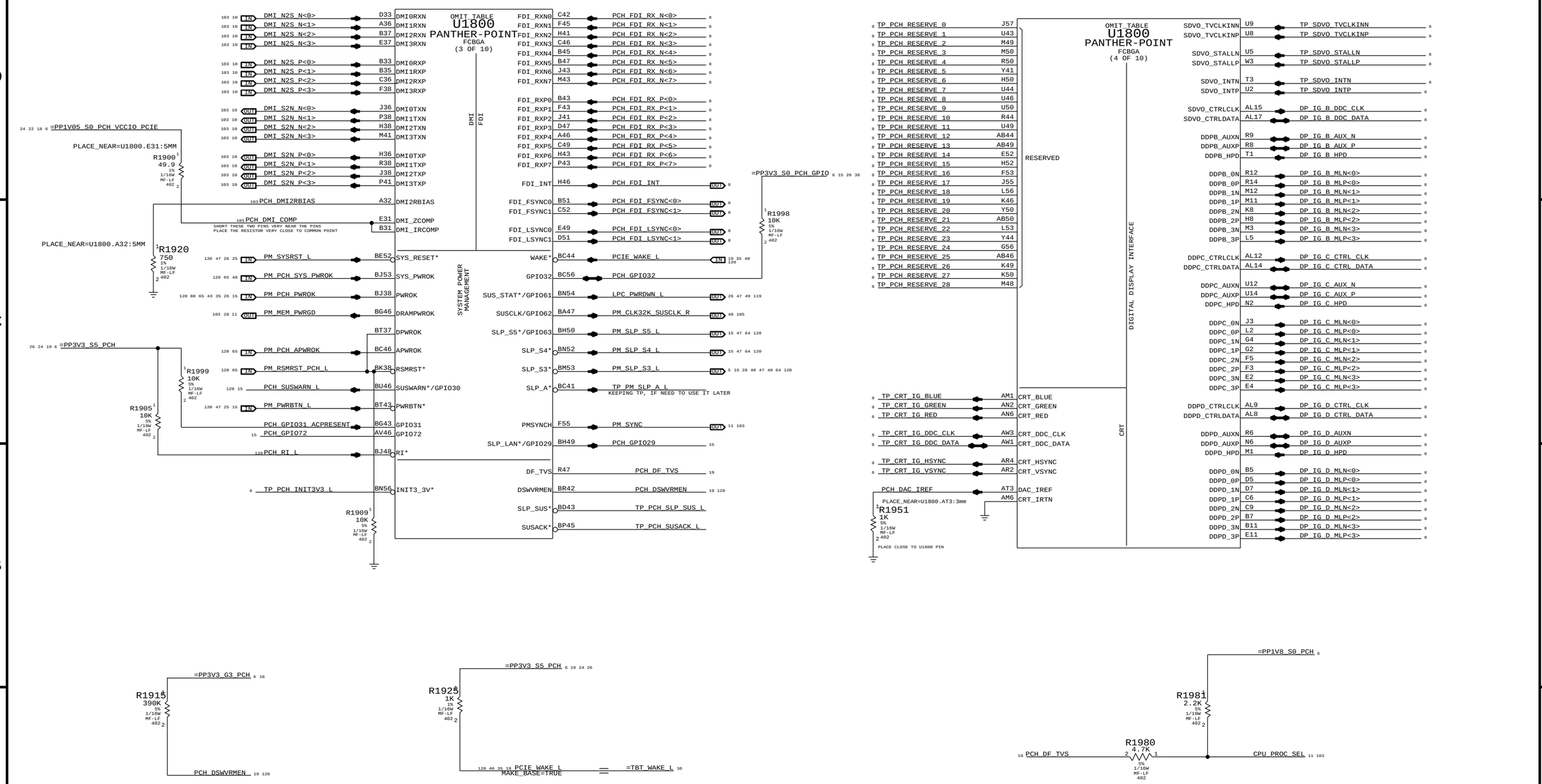


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PAGE TITLE
# PCH DMI/FDI/GRAPHICS

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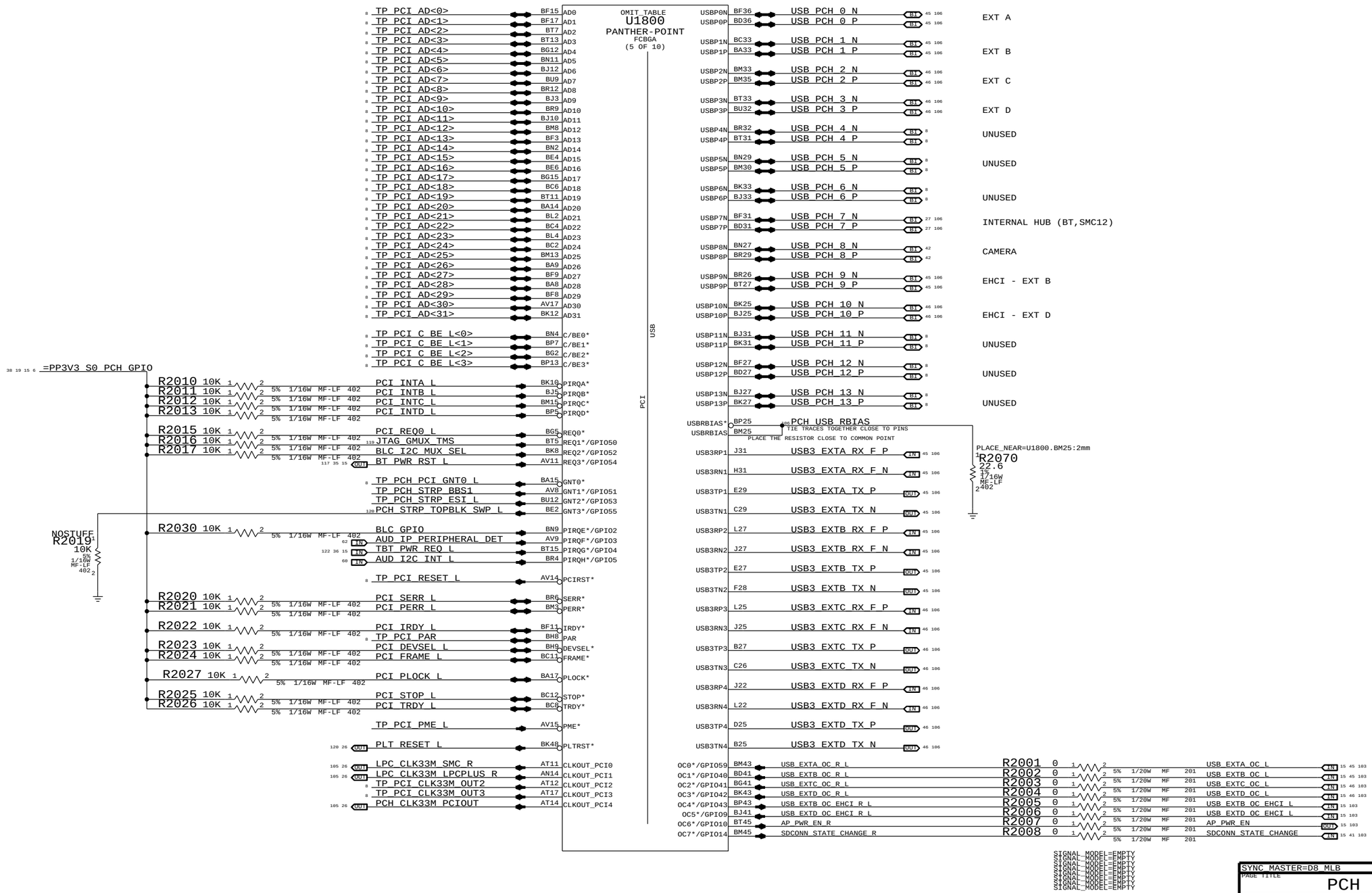


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# PCH PCI/USB

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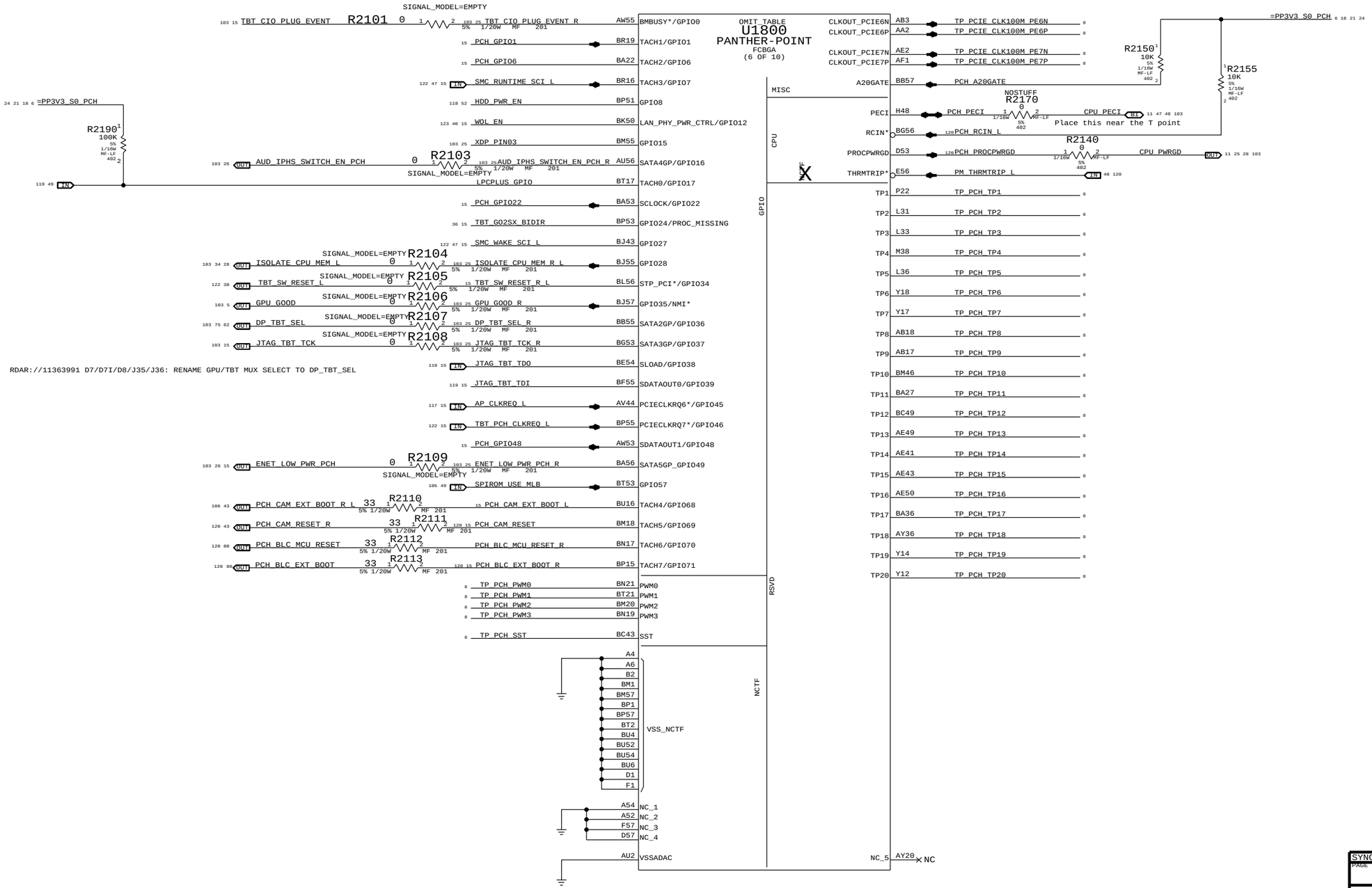


RDAR://11363991 D7/D7I/D8/J35/J36: RENAME GPU/TBT MUX SELECT TO DP_TBT_SEL

| | |
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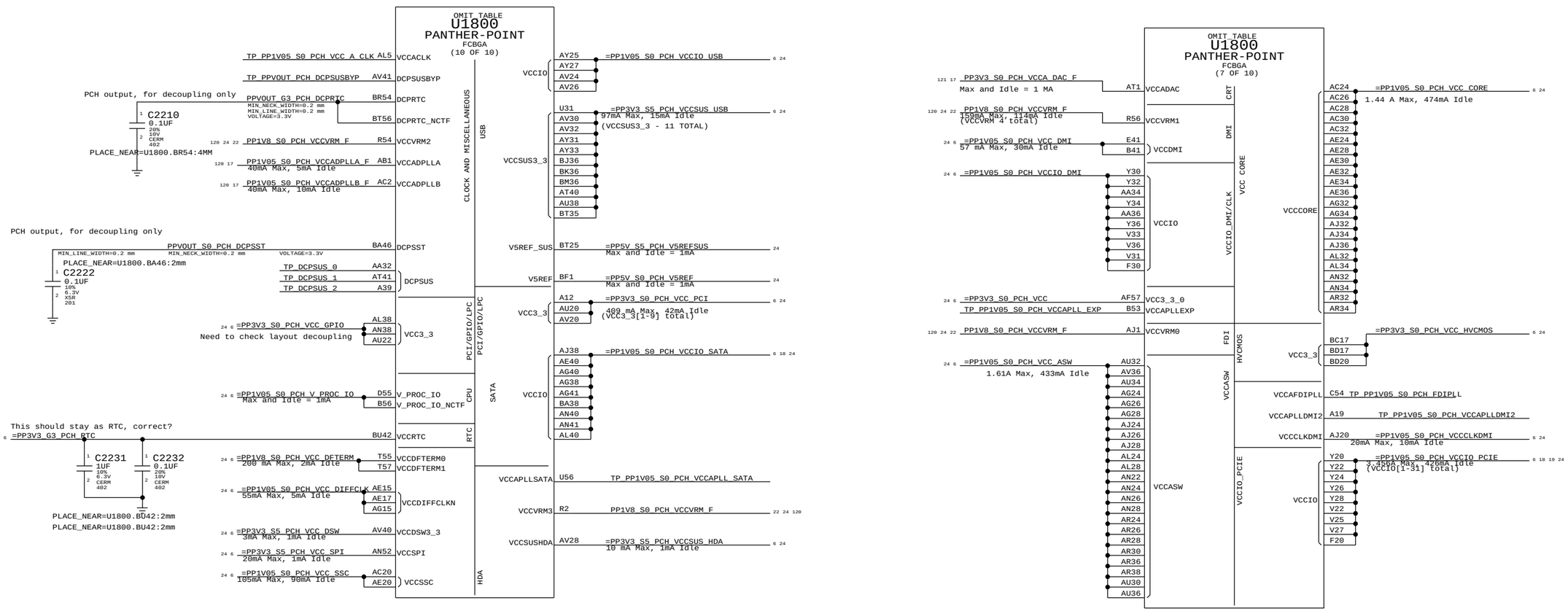





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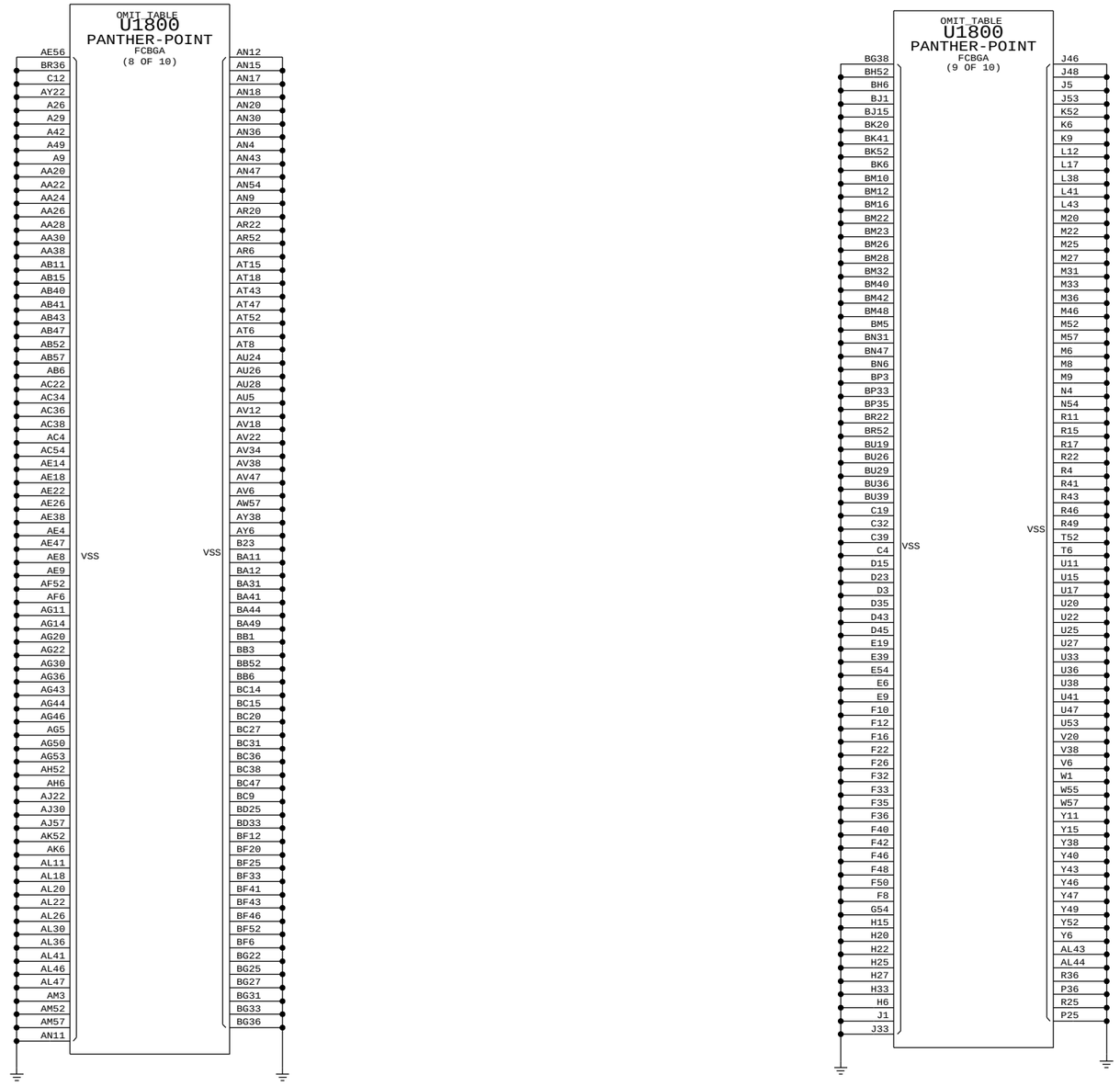


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# PCH GROUNDS

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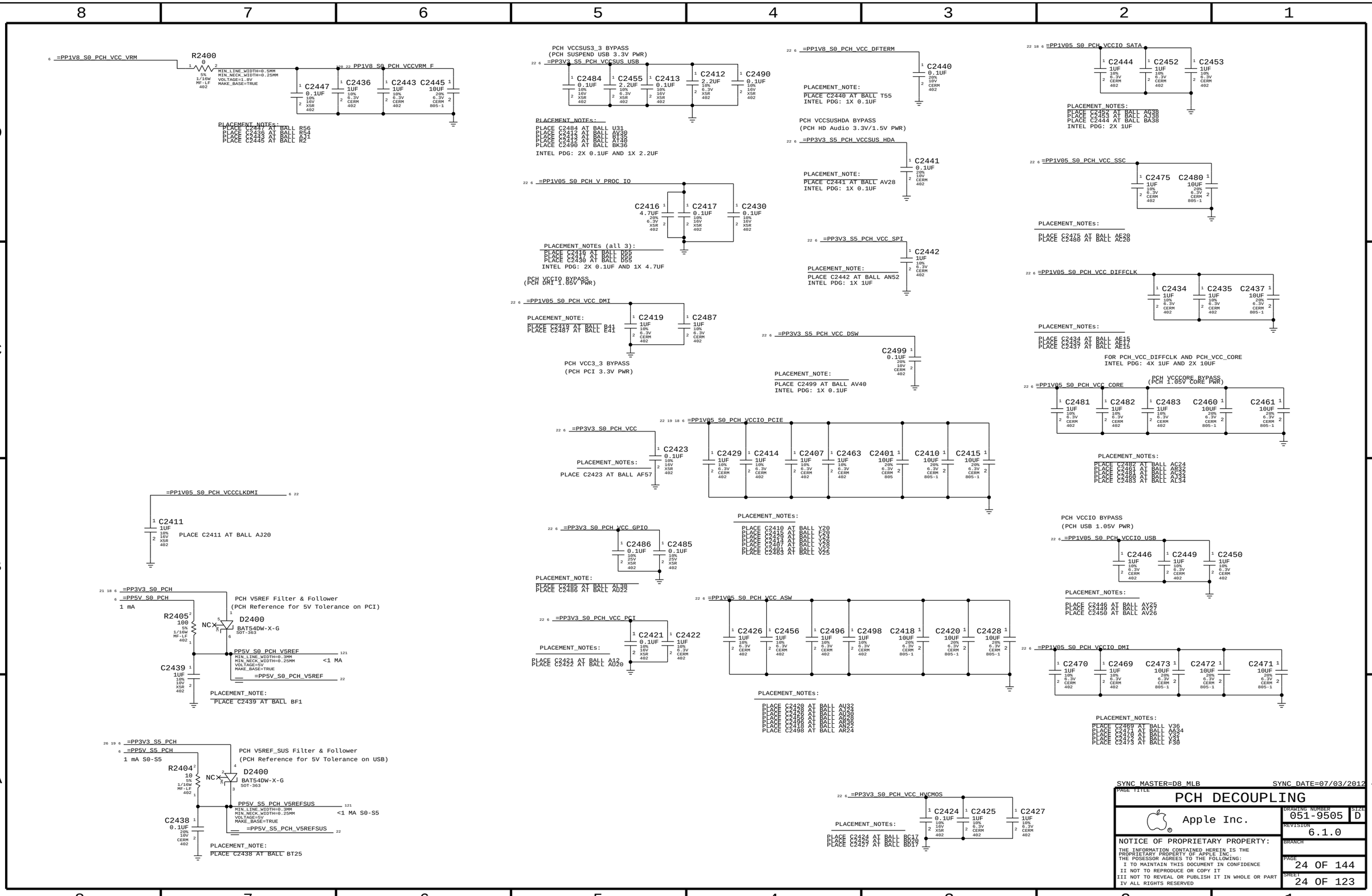


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PAGE TITLE
# PCH DECOUPLING

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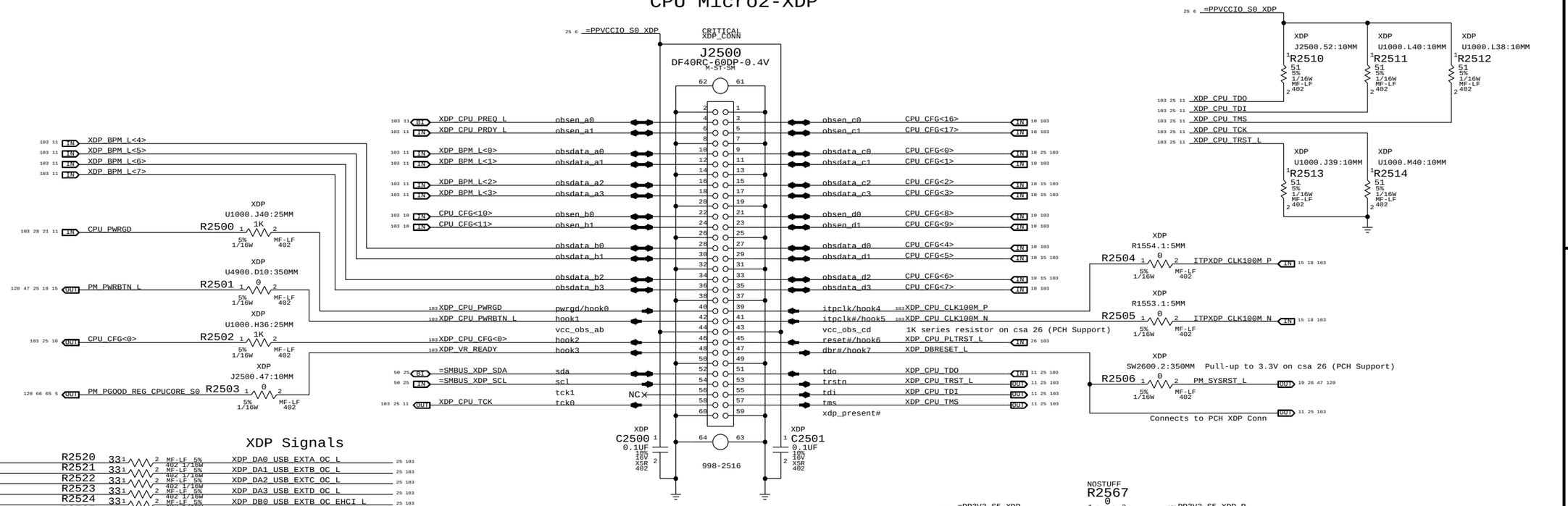
# CPU Micro2-XDP

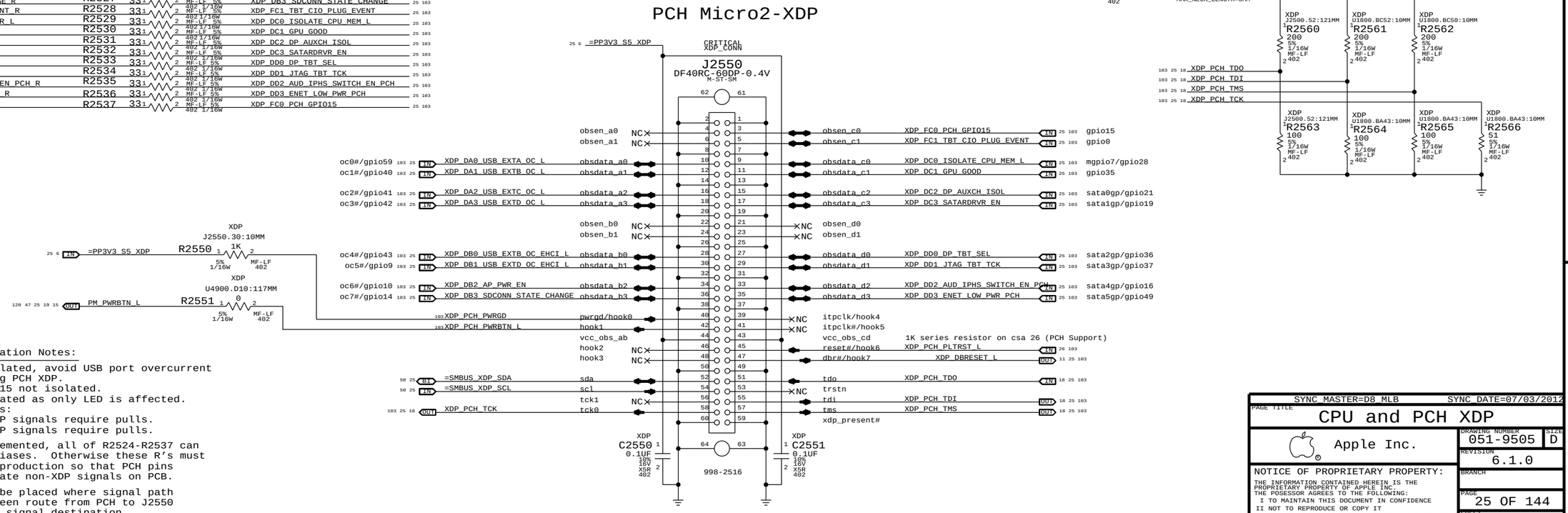



## PCH Signals

| | | | |
|---|---|---|---|
| USB_EXTA_OC_R_L | R2520 | 33 | XDP_DA0_USB_EXTA_OC_L |
| USB_EXTB_OC_R_L | R2521 | 33 | XDP_DA1_USB_EXTB_OC_L |
| USB_EXTC_OC_R_L | R2522 | 33 | XDP_DA2_USB_EXTC_OC_L |
| USB_EXTD_OC_R_L | R2523 | 33 | XDP_DA3_USB_EXTD_OC_L |
| USB_EXTB_OC_EHCI_R_L | R2524 | 33 | XDP_DB0_USB_EXTB_OC_EHCI_L |
| USB_EXTD_OC_EHCI_R_L | R2525 | 33 | XDP_DB1_USB_EXTD_OC_EHCI_L |
| AP_PWR_EN_R | R2526 | 33 | XDP_DB2_AP_PWR_EN |
| SDCONN_STATE_CHANGE_R | R2527 | 33 | XDP_DB3_SDCONN_STATE_CHANGE |
| TBT_CIO_PLUG_EVENT_R | R2528 | 33 | XDP_FC1_TBT_CIO_PLUG_EVENT |
| ISOLATE_CPU_MEM_R_L | R2529 | 33 | XDP_DC0_ISOLATE_CPU_MEM_L |
| GPU_GOOD_R | R2530 | 33 | XDP_DC1_GPU_GOOD |
| DP_AUXCH_ISOL_R | R2531 | 33 | XDP_DC2_DP_AUXCH_ISOL |
| SATARDRVR_EN_R | R2532 | 33 | XDP_DC3_SATARDRVR_EN |
| DP_TBT_SEL_R | R2533 | 33 | XDP_DD0_DP_TBT_SEL |
| JTAG_TBT_TCK_R | R2534 | 33 | XDP_DD1_JTAG_TBT_TCK |
| AUD_IPHS_SWITCH_EN_PCH_R | R2535 | 33 | XDP_DD2_AUD_IPHS_SWITCH_EN_PCH |
| ENET_LOW_PWR_PCH_R | R2536 | 33 | XDP_DD3_ENET_LOW_PWR_PCH |
| XDP_PIN03 | R2537 | 33 | XDP_FC0_PCH_GPIO15 |

## XDP Signals

# PCH Micro2-XDP




PCH/XDP Signal Isolation Notes:

- USB OC#'s not isolated, avoid USB port overcurrent events while using PCH XDP.
- Unused GPIOs 0 & 15 not isolated.
- MXM_GOOD not isolated as only LED is affected.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

If PCH XDP not implemented, all of R2524-R2537 can be replaced with aliases. Otherwise these R's must be stuffed even in production so that PCH pins connect to appropriate non-XDP signals on PCB.

R2524-R2537 should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

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PAGE TITLE: CPU and PCH XDP

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# System 25MHz Clock Generator

VDD must be powered if any VDDIO is.
ENET > S0 > TBT, so ENET is used here.

GreenClk 25MHz Power — =PP3V3_S4_ENET_SYSCLK
Ethernet XTAL Power — =PP3V3_S4_ENET_CLK
SB XTAL Power — =PP1V8_S0_PCH_CLK
TBT XTAL Power — =PP3V3_TBT_CLK

C2624 0.1UF 20% 10V CERM 402
C2622 0.1UF 20% 10V CERM 402
C2620 0.1UF 20% 10V CERM 402
C2602 1UF 10% 6.3V CERM 402

U2600
SLG3NB146V
TDFN
CRITICAL

VDD, VDDIO_A, VDDIO_B, VDDIO_C, XOUT, XIN, GND, THRM PAD
25MHZ_A — SYSCLK_CLK25M_SB
25MHZ_B — SYSCLK_CLK25M_ENET_R
25MHZ_C — SYSCLK_CLK25M_TBT

C2605 12PF 5% 50V C0G-CERM 0402
C2606 12PF 5% 50V C0G-CERM 0402
CRITICAL
Y2605
25.000MHZ-20PPM-12PF-85C
3.2X2.5MM-SM
NC NC
R2605 0 5% 1/16W MF-LF 402
NO STUFF
R2606 1M 5% 1/16W MF-LF 402
SYSCLK_CLK25M_X2
SYSCLK_CLK25M_X2_R
SYSCLK_CLK25M_X1
NOTE: 30 PPM crystal required

# RTC Power Sources

Coin-Cell Holder
J2600
BB10201-C1403-7H
511-0054
PPVBATT_G3_RTC
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R2602 1K 5% 1/16W MF-LF 402
=PP3V3_G3H_RTC_D
PPVBATT_G3_RTC_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

D2600
BAT54DW-X-G
SOT-363
NC NC NC NC
PP3V3_G3_RTC
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V

TP2600 1.97X2.02MM-NSP SMT-PAD OMIT
TP2601 1.97X2.02MM-NSP SMT-PAD OMIT

RDAR://11218892 TESTPOINT TO RESET RTC FOR APPLE CARE

TP2602 1.4-SQ-NSP SM-PAD OMIT
TP2603 1.4-SQ-NSP SM-PAD OMIT
RTC_RESET_L

# PCH 25MHZ CLOCK

SYSCLK_CLK25M_SB From GreenClk @ 1.8V
R2671 40.2 1% 1/16W MF-LF 402
PCH_CLK25M_XTALIN To PCH @ 1.1V
R2672 140 1% 1/16W MF-LF 402

# PCH RTC Crystal

PCH_CLK32K_RTCX2
R2610 0 5% 1/16W MF-LF 402
PCH_CLK32K_RTCX2_R
R2611 10M 5% 1/16W MF-LF 402
CRITICAL
Y2610
32.768K-12.5PF
SM-MF
PLACE_NEAR=Y2610.3:7MM
C2610 12PF 5% 50V C0G-CERM 0402
C2611 12PF 5% 50V C0G-CERM 0402
PLACE_NEAR=Y2610.1:2MM
PCH_CLK32K_RTCX1

# Clock series termination

LPC_CLK33M_SMC_R — PLACE_NEAR=U1800.AT11:10mm — R2625 33 — LPC_CLK33M_SMC
LPC_CLK33M_LPCPLUS_R — PLACE_NEAR=U1800.AN14:10mm — R2626 33 — LPC_CLK33M_LPCPLUS
PCH_CLK33M_PCIOUT — PLACE_NEAR=U1800.AT14:10mm — R2627 33 — PCH_CLK33M_PCIIN
SYSCLK_CLK25M_ENET_R — PLACE_NEAR=U2600.4:10MM — R2628 33 — SYSCLK_CLK25M_ENET

# GPIO Isolation to prevent glitches on critical core well GPIOs

=PP3V3_S5_PCH
PLACE_NEAR=U2650.8:2MM
C2650 0.1UF 20% 10V CERM 402
CRITICAL
74LVC2G08GT SOT833
U2650
TBT_PWR_EN_PCH
LPC_PWRDWN_L
TBT_PWR_EN

=PP3V3_S5_PCH
CRITICAL
74LVC2G08GT SOT833
U2650
ENET_LOW_PWR_PCH
PM_PCH_PWROK
ENET_LOW_PWR

=PP3V3_S5_PCH
PLACE_NEAR=U2660.5:2MM
C2660 0.1UF 20% 10V CERM 402
MC74VHC1G08 SOT23-5-HF
U2660
AUD_IPHS_SWITCH_EN_PCH
PM_PCH_PWROK
AUD_IPHS_SWITCH_EN

# Platform Reset Connections

PLT_RESET_L MAKE_BASE=TRUE

## Unbuffered

R2681 33 5% 1/16W MF-LF 402 — DEBUG_RESET_L
R2655 33 5% 1/16W MF-LF 402 — SMC_LRESET_L MAKE_BASE=TRUE
XDP R2699 1K 5% 1/16W MF-LF 402 — XDP_PCH_PLTRST_L
XDP R2698 1K 5% 1/16W MF-LF 402 — XDP_CPU_PLTRST_L
MAY NEED TO MOVE LONGER TRACE ONES TO BUFFERED
R2694 33 5% 1/16W MF-LF 402 — PCA9557D_RESET_L

## Buffered

=PP3V3_S0_RSTBUF
MC74VHC1G08 SOT23-5-HF
U2680
C2680 0.1UF 20% 10V CERM 402
PLT_RST_BUF_L
R2680 100K 5% 1/16W MF-LF 402

R2690 33 5% 1/16W MF-LF 402 — GPU_RESET_L
R2691 33 5% 1/16W MF-LF 402 — TBT_PLT_RST_L MAKE_BASE=TRUE — =TBT_RESET_L
R2688 33 5% 1/16W MF-LF 402 — AP_RESET_L
R2692 33 5% 1/16W MF-LF 402 — ENET_SD_RESET_L

=PP3V3_S0_RSTBUF
OPEN-DRAIN BUFFER
U2690
74LVC1G07
SC70
NC NC
C2690 0.1UF 20% 10V CERM 402
VTT VOLTAGE DIVIDER AND PU ON CPU PAGE
CPU_RESET_L

# Reset Button

=PP3V3_S0_PCH_PM
R2697 4.7K 5% 1/16W MF-LF 402
DEVELOPMENT
SW2600
NTC020AA1JB260T
SILK_PART=SYS RESET
PM_SYSRST_L
NOSTUFF
R2696 0 5% 1/16W MF-LF 402
SILK_PART=SYS RESET

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PAGE TITLE
CHIPSET SUPPORT

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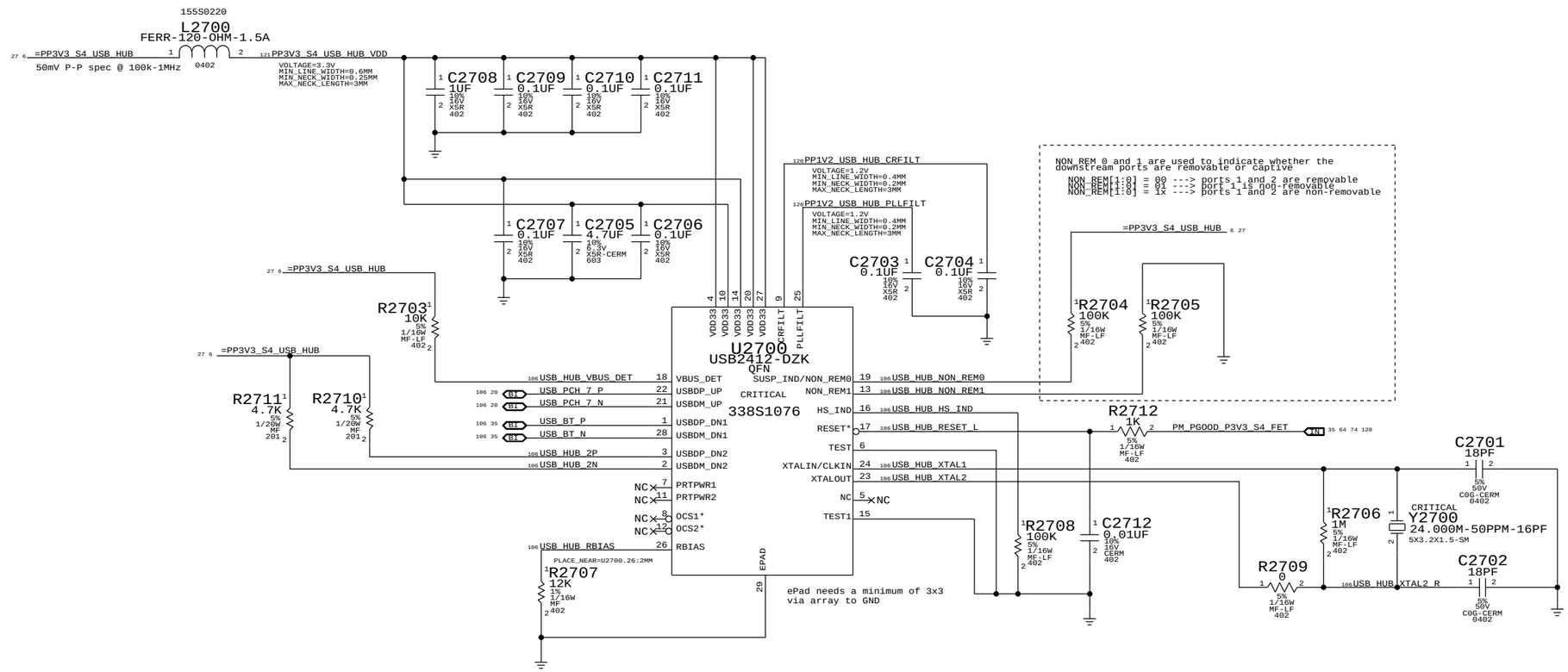


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# USB 2.0 HUB (BT/SMC)

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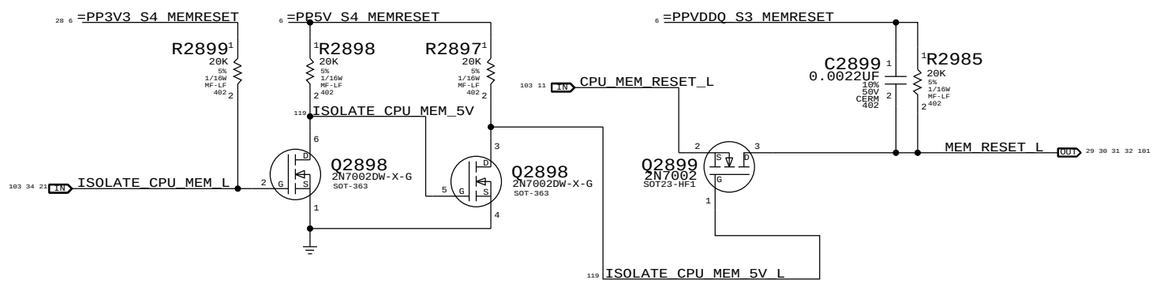
# MEM_RESET_L Generator

The circuits below handle MEMVTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

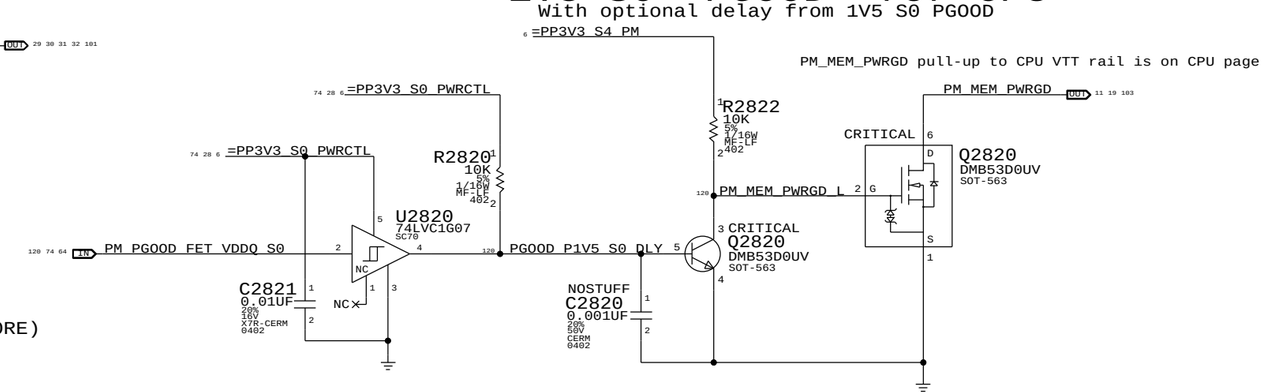
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behaviour of signals.
WHEN HIGH: MEM_RESET_L NOT ISOLATED.
WHEN LOW: MEM_RESET_L IS ISOLATED.
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L (Block CPU from driving MEM_RESET_L in S3)




# 1V5 S0 "PGOOD" for CPU

With optional delay from 1V5 S0 PGOOD

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



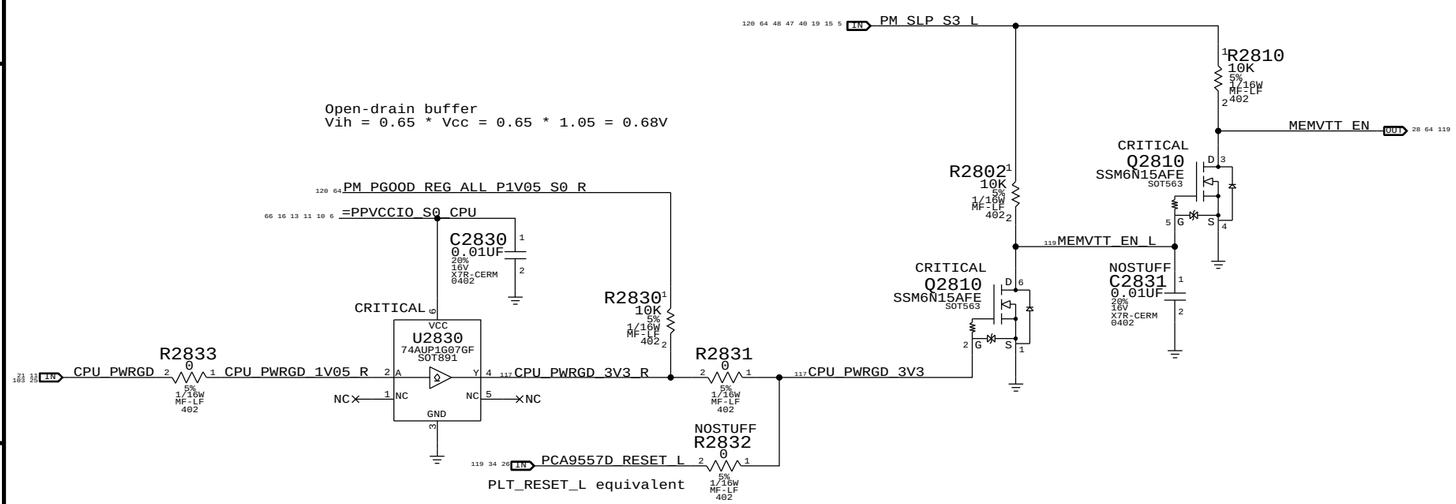

# MEMVTT_EN Generator

rdar://11117167

Enables MEMVTT when PCH drives CPU PWRGD.

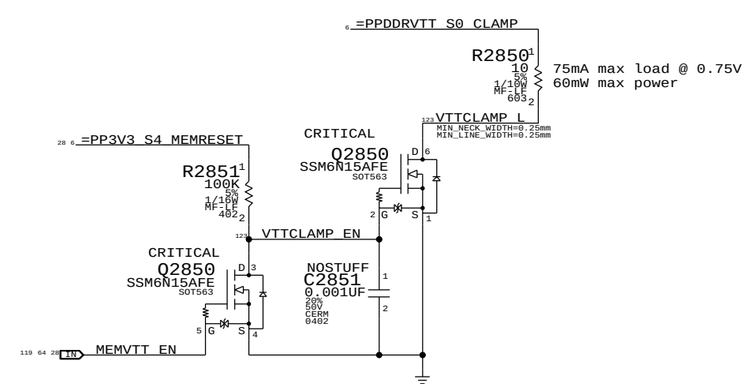
CPU does not drive MEM_CKE until VCCORE activated but CPU 1V5 (VDDQ) leaks into it.
Clamping MEMVTT will keep the MEM_CKE low until CPU actively controls it.
MEMVTT Clamp actively holds MEMVTT rail low until MEMVTT is enabled.
MEMVTT_EN = CPU_PWRGD * PM_SLP_S3_L (VTT is enabled when PCH tells CPU to enable VCCORE)

Open-drain buffer
Vih = 0.65 * Vcc = 0.65 * 1.05 = 0.68V




# MEMVTT Clamp

Ensures CKE signals are held low in S3 and in S0 before CPU PWRGD




| | Step | ISOLATE_CPU_MEM_L | PM_SLP_S3_L | CPU_PWRGD | CPU_MEM_RESET_L | MEM_RESET_L | MEMVTT_EN |
|---|---|---|---|---|---|---|---|
| S0 | 0 | 1 | 1 | 1 | CPU_MEM_RESET_L | 1 | 1 |
| to | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| S3 | 2 | 0 | 1 | 1 | 1 | 1 | 1 |
| to | 3 | 0 | 0 | 0 | X | 1 | 0 |
| S0 | 4 | 0 | 0 | 0 | X | 1 | 0 |
| | 5 | 0 | 1 | 1 | 0 (*) | 1 | 1 |
| | 6 | 0 | 1 | 1 | 1 | 1 | 1 |
| | 7 | 1 | 1 | 1 | CPU_MEM_RESET_L | 1 | 1 |

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: On a S5->S0 transition, ISOLATE_CPU_MEM_L will default low.
Rails will power-up as if from S3, but MEM_RESET_L now needs to be asserted in S0. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

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CPU Memory S3 Support

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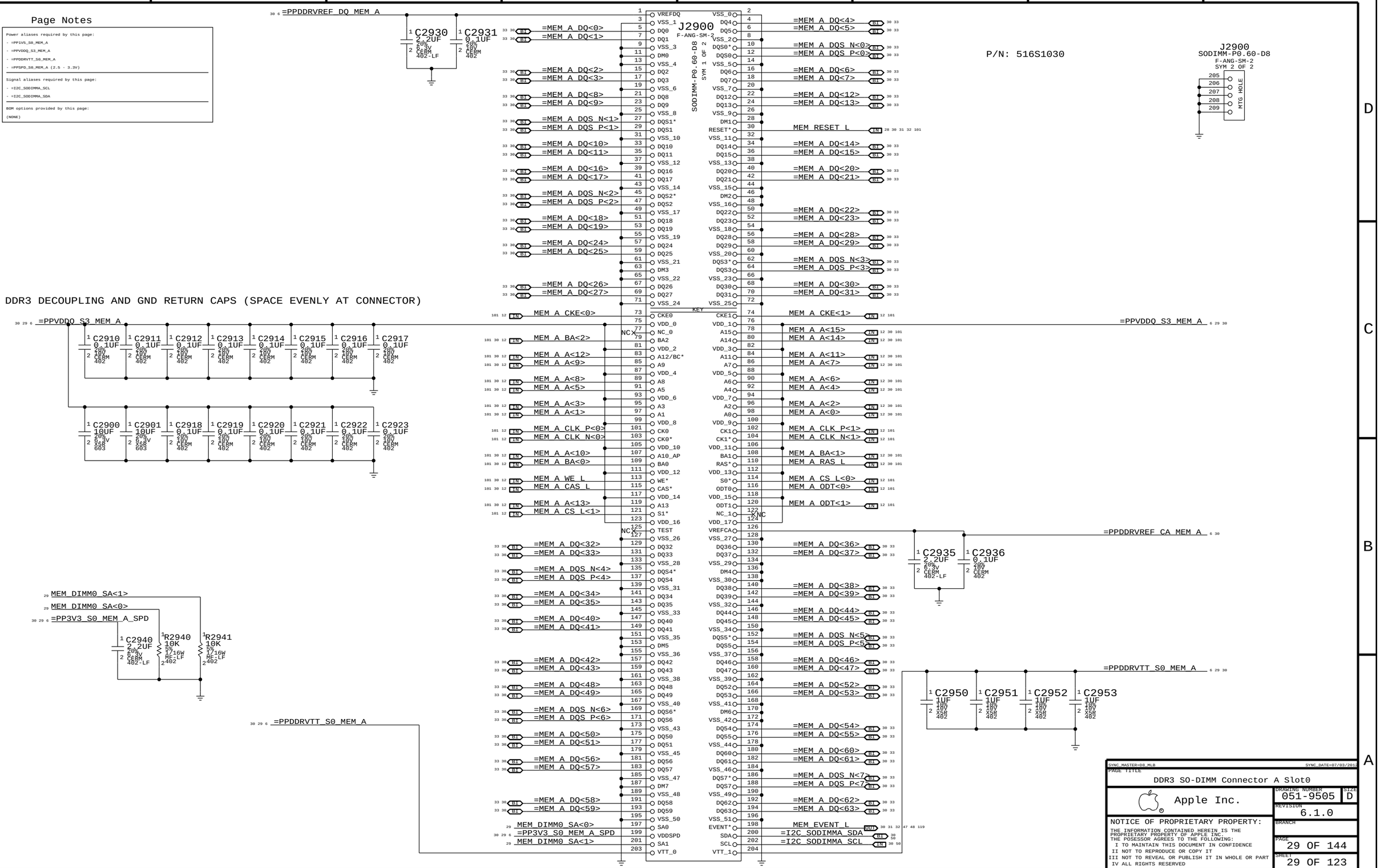
## Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

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PAGE TITLE
DDR3 SO-DIMM Connector A Slot0

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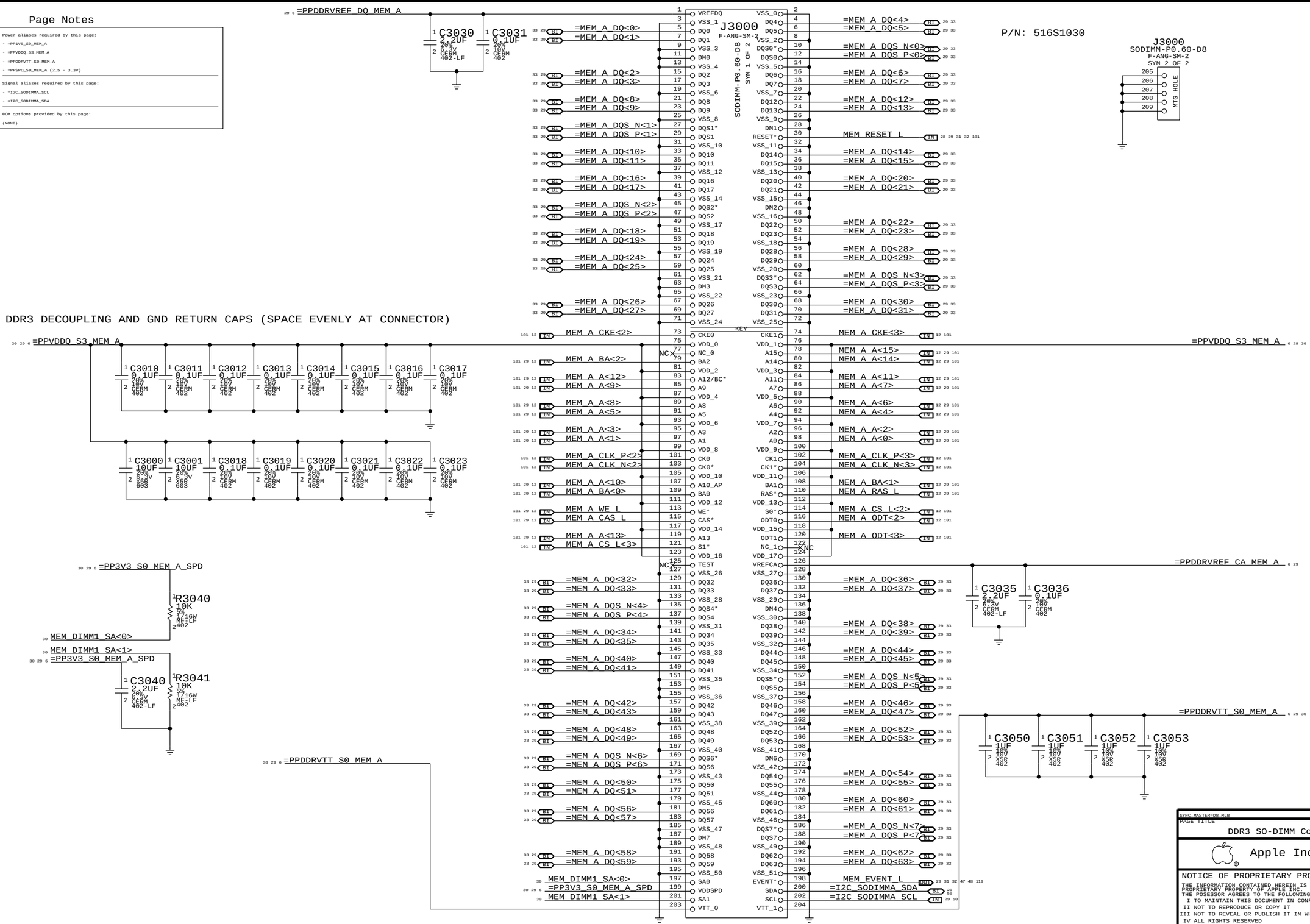
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

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PAGE TITLE
DDR3 SO-DIMM Connector A Slot1

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## Page Notes

Power aliases required by this page:
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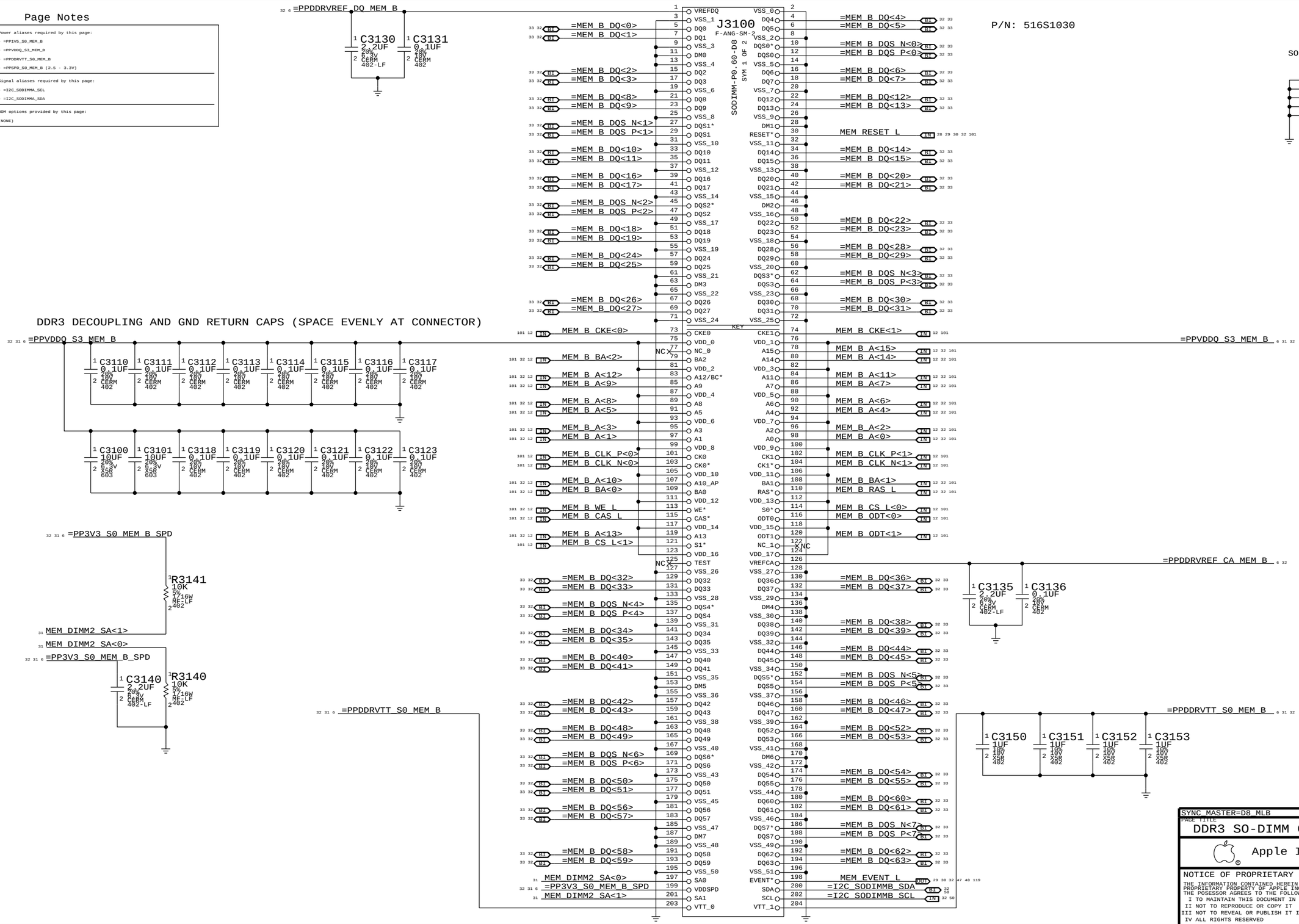
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

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PAGE TITLE
DDR3 SO-DIMM CONNECTOR B SLOT0

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- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

=PPDDRVREF_DQ_MEM_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 1 OF 2

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | VREFDQ | 2 | VSS_0 |
| 3 | VSS_1 | 4 | DQ4 |
| 5 | DQ0 | 6 | DQ5 |
| 7 | DQ1 | 8 | VSS_2 |
| 9 | VSS_3 | 10 | DQS0* |
| 11 | DM0 | 12 | DQS0 |
| 13 | VSS_4 | 14 | VSS_5 |
| 15 | DQ2 | 16 | DQ6 |
| 17 | DQ3 | 18 | DQ7 |
| 19 | VSS_6 | 20 | VSS_7 |
| 21 | DQ8 | 22 | DQ12 |
| 23 | DQ9 | 24 | DQ13 |
| 25 | VSS_8 | 26 | VSS_9 |
| 27 | DQS1* | 28 | DM1 |
| 29 | DQS1 | 30 | RESET* |
| 31 | VSS_10 | 32 | VSS_11 |
| 33 | DQ10 | 34 | DQ14 |
| 35 | DQ11 | 36 | DQ15 |
| 37 | VSS_12 | 38 | VSS_13 |
| 39 | DQ16 | 40 | DQ20 |
| 41 | DQ17 | 42 | DQ21 |
| 43 | VSS_14 | 44 | VSS_15 |
| 45 | DQS2* | 46 | DM2 |
| 47 | DQS2 | 48 | VSS_16 |
| 49 | VSS_17 | 50 | DQ22 |
| 51 | DQ18 | 52 | DQ23 |
| 53 | DQ19 | 54 | VSS_18 |
| 55 | VSS_19 | 56 | DQ28 |
| 57 | DQ24 | 58 | DQ29 |
| 59 | DQ25 | 60 | VSS_20 |
| 61 | VSS_21 | 62 | DQS3* |
| 63 | DM3 | 64 | DQS3 |
| 65 | VSS_22 | 66 | VSS_23 |
| 67 | DQ26 | 68 | DQ30 |
| 69 | DQ27 | 70 | DQ31 |
| 71 | VSS_24 | 72 | VSS_25 |
| 73 | CKE0 | 74 | CKE1 |
| 75 | VDD_0 | 76 | VDD_1 |
| 77 | NC_0 | 78 | A15 |
| 79 | BA2 | 80 | A14 |
| 81 | VDD_2 | 82 | VDD_3 |
| 83 | A12/BC* | 84 | A11 |
| 85 | A9 | 86 | A7 |
| 87 | VDD_4 | 88 | VDD_5 |
| 89 | A8 | 90 | A6 |
| 91 | A5 | 92 | A4 |
| 93 | VDD_6 | 94 | VDD_7 |
| 95 | A3 | 96 | A2 |
| 97 | A1 | 98 | A0 |
| 99 | VDD_8 | 100 | VDD_9 |
| 101 | CK0 | 102 | CK1 |
| 103 | CK0* | 104 | CK1* |
| 105 | VDD_10 | 106 | VDD_11 |
| 107 | A10_AP | 108 | BA1 |
| 109 | BA0 | 110 | RAS* |
| 111 | VDD_12 | 112 | VDD_13 |
| 113 | WE* | 114 | S0* |
| 115 | CAS* | 116 | ODT0 |
| 117 | VDD_14 | 118 | VDD_15 |
| 119 | A13 | 120 | ODT1 |
| 121 | S1* | 122 | NC_1 |
| 123 | VDD_16 | 124 | VDD_17 |
| 125 | TEST | 126 | VREFCA |
| 127 | VSS_26 | 128 | VSS_27 |
| 129 | DQ32 | 130 | DQ36 |
| 131 | DQ33 | 132 | DQ37 |
| 133 | VSS_28 | 134 | VSS_29 |
| 135 | DQS4* | 136 | DM4 |
| 137 | DQS4 | 138 | VSS_30 |
| 139 | VSS_31 | 140 | DQ38 |
| 141 | DQ34 | 142 | DQ39 |
| 143 | DQ35 | 144 | VSS_32 |
| 145 | VSS_33 | 146 | DQ44 |
| 147 | DQ40 | 148 | DQ45 |
| 149 | DQ41 | 150 | VSS_34 |
| 151 | VSS_35 | 152 | DQS5* |
| 153 | DM5 | 154 | DQS5 |
| 155 | VSS_36 | 156 | VSS_37 |
| 157 | DQ42 | 158 | DQ46 |
| 159 | DQ43 | 160 | DQ47 |
| 161 | VSS_38 | 162 | VSS_39 |
| 163 | DQ48 | 164 | DQ52 |
| 165 | DQ49 | 166 | DQ53 |
| 167 | VSS_40 | 168 | VSS_41 |
| 169 | DQS6* | 170 | DM6 |
| 171 | DQS6 | 172 | VSS_42 |
| 173 | VSS_43 | 174 | DQ54 |
| 175 | DQ50 | 176 | DQ55 |
| 177 | DQ51 | 178 | VSS_44 |
| 179 | VSS_45 | 180 | DQ60 |
| 181 | DQ56 | 182 | DQ61 |
| 183 | DQ57 | 184 | VSS_46 |
| 185 | VSS_47 | 186 | DQS7* |
| 187 | DM7 | 188 | DQS7 |
| 189 | VSS_48 | 190 | VSS_49 |
| 191 | DQ58 | 192 | DQ62 |
| 193 | DQ59 | 194 | DQ63 |
| 195 | VSS_50 | 196 | VSS_51 |
| 197 | SA0 | 198 | EVENT* |
| 199 | VDDSPD | 200 | SDA |
| 201 | SA1 | 202 | SCL |
| 203 | VTT_0 | 204 | VTT_1 |

SODIMM-P0.60-D8 SYM 1 OF 2

KEY

| Net | Pin |
|---|---|
| =MEM_B_DQ<0> | 5 |
| =MEM_B_DQ<1> | 7 |
| =MEM_B_DQ<2> | 15 |
| =MEM_B_DQ<3> | 17 |
| =MEM_B_DQ<8> | 21 |
| =MEM_B_DQ<9> | 23 |
| =MEM_B_DQS_N<1> | 27 |
| =MEM_B_DQS_P<1> | 29 |
| =MEM_B_DQ<10> | 33 |
| =MEM_B_DQ<11> | 35 |
| =MEM_B_DQ<16> | 39 |
| =MEM_B_DQ<17> | 41 |
| =MEM_B_DQS_N<2> | 45 |
| =MEM_B_DQS_P<2> | 47 |
| =MEM_B_DQ<18> | 51 |
| =MEM_B_DQ<19> | 53 |
| =MEM_B_DQ<24> | 57 |
| =MEM_B_DQ<25> | 59 |
| =MEM_B_DQ<26> | 67 |
| =MEM_B_DQ<27> | 69 |
| MEM_B_CKE<2> | 73 |
| MEM_B_BA<2> | 79 |
| MEM_B_A<12> | 83 |
| MEM_B_A<9> | 85 |
| MEM_B_A<8> | 89 |
| MEM_B_A<5> | 91 |
| MEM_B_A<3> | 95 |
| MEM_B_A<1> | 97 |
| MEM_B_CLK_P<2> | 101 |
| MEM_B_CLK_N<2> | 103 |
| MEM_B_A<10> | 107 |
| MEM_B_BA<0> | 109 |
| MEM_B_WE_L | 113 |
| MEM_B_CAS_L | 115 |
| MEM_B_A<13> | 119 |
| MEM_B_CS_L<3> | 121 |
| =MEM_B_DQ<32> | 129 |
| =MEM_B_DQ<33> | 131 |
| =MEM_B_DQS_N<4> | 135 |
| =MEM_B_DQS_P<4> | 137 |
| =MEM_B_DQ<34> | 141 |
| =MEM_B_DQ<35> | 143 |
| =MEM_B_DQ<40> | 147 |
| =MEM_B_DQ<41> | 149 |
| =MEM_B_DQ<42> | 157 |
| =MEM_B_DQ<43> | 159 |
| =MEM_B_DQ<48> | 163 |
| =MEM_B_DQ<49> | 165 |
| =MEM_B_DQS_N<6> | 169 |
| =MEM_B_DQS_P<6> | 171 |
| =MEM_B_DQ<50> | 175 |
| =MEM_B_DQ<51> | 177 |
| =MEM_B_DQ<56> | 181 |
| =MEM_B_DQ<57> | 183 |
| =MEM_B_DQ<58> | 191 |
| =MEM_B_DQ<59> | 193 |
| MEM_DIMM3_SA<0> | 197 |
| =PP3V3_S0_MEM_B_SPD | 199 |
| MEM_DIMM3_SA<1> | 201 |

| Net | Pin |
|---|---|
| =MEM_B_DQ<4> | 6 |
| =MEM_B_DQ<5> | 8 |
| =MEM_B_DQS_N<0> | 10 |
| =MEM_B_DQS_P<0> | 12 |
| =MEM_B_DQ<6> | 16 |
| =MEM_B_DQ<7> | 18 |
| =MEM_B_DQ<12> | 22 |
| =MEM_B_DQ<13> | 24 |
| MEM_RESET_L | 30 |
| =MEM_B_DQ<14> | 34 |
| =MEM_B_DQ<15> | 36 |
| =MEM_B_DQ<20> | 40 |
| =MEM_B_DQ<21> | 42 |
| =MEM_B_DQ<22> | 50 |
| =MEM_B_DQ<23> | 52 |
| =MEM_B_DQ<28> | 56 |
| =MEM_B_DQ<29> | 58 |
| =MEM_B_DQS_N<3> | 62 |
| =MEM_B_DQS_P<3> | 64 |
| =MEM_B_DQ<30> | 68 |
| =MEM_B_DQ<31> | 70 |
| MEM_B_CKE<3> | 74 |
| MEM_B_A<15> | 78 |
| MEM_B_A<14> | 80 |
| MEM_B_A<11> | 84 |
| MEM_B_A<7> | 86 |
| MEM_B_A<6> | 90 |
| MEM_B_A<4> | 92 |
| MEM_B_A<2> | 96 |
| MEM_B_A<0> | 98 |
| MEM_B_CLK_P<3> | 102 |
| MEM_B_CLK_N<3> | 104 |
| MEM_B_BA<1> | 108 |
| MEM_B_RAS_L | 110 |
| MEM_B_CS_L<2> | 114 |
| MEM_B_ODT<2> | 116 |
| MEM_B_ODT<3> | 120 |
| =MEM_B_DQ<36> | 130 |
| =MEM_B_DQ<37> | 132 |
| =MEM_B_DQ<38> | 140 |
| =MEM_B_DQ<39> | 142 |
| =MEM_B_DQ<44> | 146 |
| =MEM_B_DQ<45> | 148 |
| =MEM_B_DQS_N<5> | 152 |
| =MEM_B_DQS_P<5> | 154 |
| =MEM_B_DQ<46> | 158 |
| =MEM_B_DQ<47> | 160 |
| =MEM_B_DQ<52> | 164 |
| =MEM_B_DQ<53> | 166 |
| =MEM_B_DQ<54> | 174 |
| =MEM_B_DQ<55> | 176 |
| =MEM_B_DQ<60> | 180 |
| =MEM_B_DQ<61> | 182 |
| =MEM_B_DQS_N<7> | 186 |
| =MEM_B_DQS_P<7> | 188 |
| =MEM_B_DQ<62> | 192 |
| =MEM_B_DQ<63> | 194 |
| MEM_EVENT_L | 198 |
| =I2C_SODIMMB_SDA | 200 |
| =I2C_SODIMMB_SCL | 202 |

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SODIMM-P0.60-D8
F-ANG-SM-2
SYM 2 OF 2

| Pin | Signal |
|---|---|
| 205 | MTG HOLE |
| 206 | |
| 207 | |
| 208 | |
| 209 | |

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X6S 603
C3201 10UF 20% 6.3V X6S 603
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD

R3241 10K 5% 1/16W 0402-LF 402
R3240 10K 5% 1/16W 0402-LF 402

MEM_DIMM3_SA<1>
MEM_DIMM3_SA<0>
=PP3V3_S0_MEM_B_SPD

C3240 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVREF_CA_MEM_B

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_B

C3250 1UF 10% 10V X5R 402
C3251 1UF 10% 10V X5R 402
C3252 1UF 10% 10V X5R 402
C3253 1UF 10% 10V X5R 402

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B SLOT1

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| | | | |
|---|---|---|---|
| MEM_A_DQS_N<0> | MAKE_BASE=TRUE | =MEM_A_DQS_N<0> | MEM_B_DQS_N<0> |
| MEM_A_DQS_P<0> | MAKE_BASE=TRUE | =MEM_A_DQS_P<0> | MEM_B_DQS_P<0> |
| MEM_A_DQ<7> | MAKE_BASE=TRUE | =MEM_A_DQ<7> | MEM_B_DQ<7> |
| MEM_A_DQ<6> | MAKE_BASE=TRUE | =MEM_A_DQ<6> | MEM_B_DQ<6> |
| MEM_A_DQ<5> | MAKE_BASE=TRUE | =MEM_A_DQ<4> | MEM_B_DQ<5> |
| MEM_A_DQ<4> | MAKE_BASE=TRUE | =MEM_A_DQ<1> | MEM_B_DQ<4> |
| MEM_A_DQ<3> | MAKE_BASE=TRUE | =MEM_A_DQ<3> | MEM_B_DQ<3> |
| MEM_A_DQ<2> | MAKE_BASE=TRUE | =MEM_A_DQ<2> | MEM_B_DQ<2> |
| MEM_A_DQ<1> | MAKE_BASE=TRUE | =MEM_A_DQ<5> | MEM_B_DQ<1> |
| MEM_A_DQ<0> | MAKE_BASE=TRUE | =MEM_A_DQ<0> | MEM_B_DQ<0> |
| MEM_A_DQS_N<1> | MAKE_BASE=TRUE | =MEM_A_DQS_N<1> | MEM_B_DQS_N<1> |
| MEM_A_DQS_P<1> | MAKE_BASE=TRUE | =MEM_A_DQS_P<1> | MEM_B_DQS_P<1> |
| MEM_A_DQ<15> | MAKE_BASE=TRUE | =MEM_A_DQ<15> | MEM_B_DQ<15> |
| MEM_A_DQ<14> | MAKE_BASE=TRUE | =MEM_A_DQ<14> | MEM_B_DQ<14> |
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SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# DDR3 ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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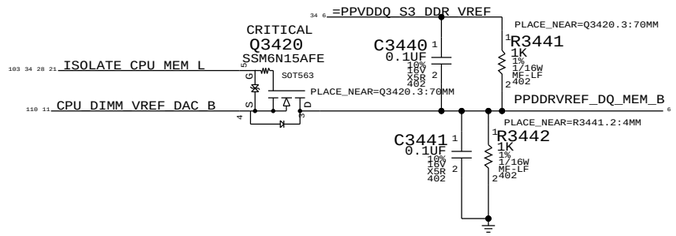
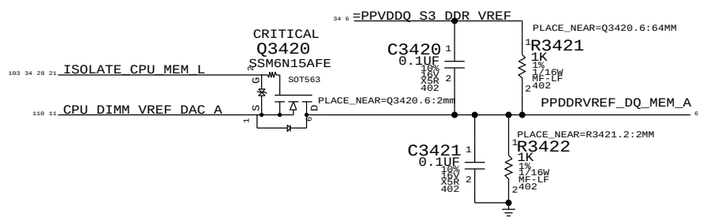
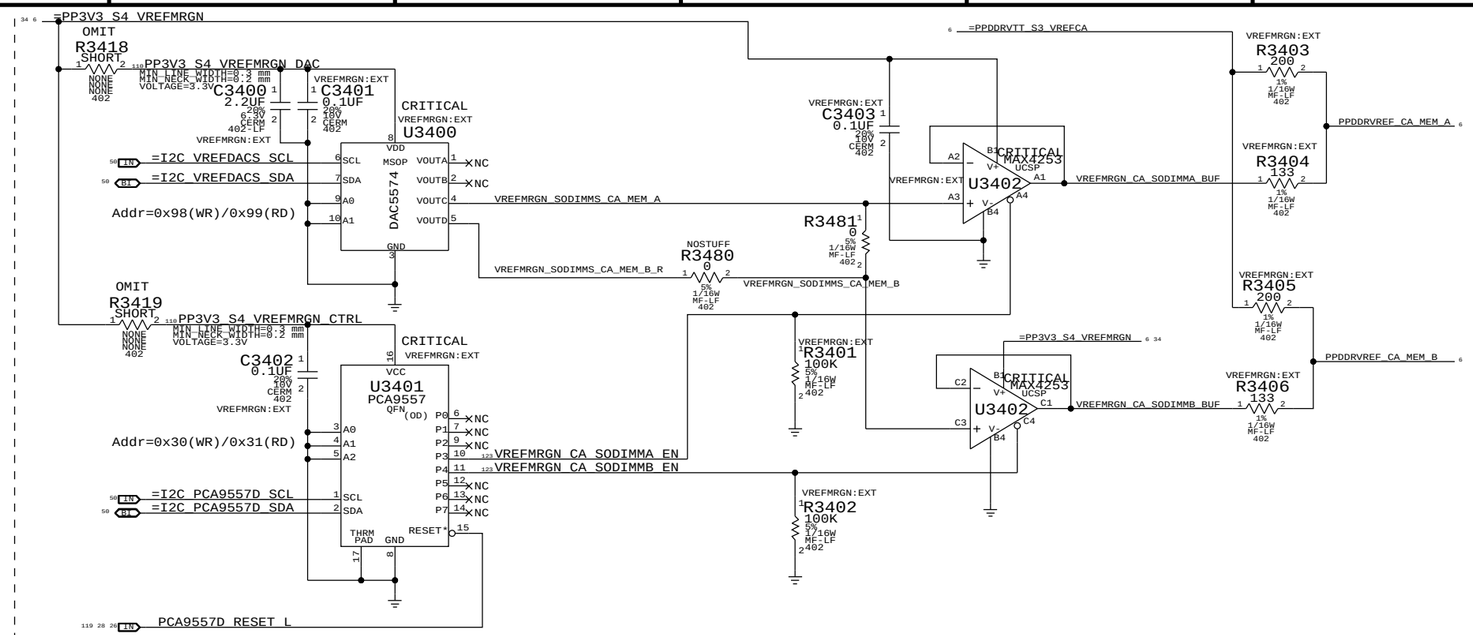
# VRef DQ

Driven by CPU

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step




RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 116S0004 | 2 | RES,MTL FLM,0,5%,402,SM,LF | R3403,R3405 | | VREFMRGN:N |

| | MEM A VREF CA | MEM B VREF CA | MEM VREG | GPU Frame Buffer (1.8V, 70% VRef) |
|---|---|---|---|---|
| DAC Channel: | C | C | D | D |
| PCA9557D Pin: | 3 | 4 | 5 | 6 |
| Nominal value | 0.75V (DAC: 0x3A) | | 1.5V (DAC: 0x3A) | 1.267V (DAC: 0x8B) |
| Margined target: | 0.300V - 1.200V (+/- 450mV) | | 1.000V - 2.000V (+/- 500mV) | 1.056V - 1.442V (+/- 180mV) |
| DAC range: | 0.000V - 1.501V (0x00 - 0x74) | | 0.000V - 3.000V (0x00 - 0x74) | 0.000V - 3.300V (0x00 - 0xFF) |
| VRef current: | +3.4mA - -3.4mA (- = sourced) | | +61uA - -61uA (- = sourced) | +6.0mA - -5.0mA (- = sourced) |
| DAC step size: | 7.69mV / step @ output | | 8.59mV / step @ output | 1.51mV / step @ output |

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PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

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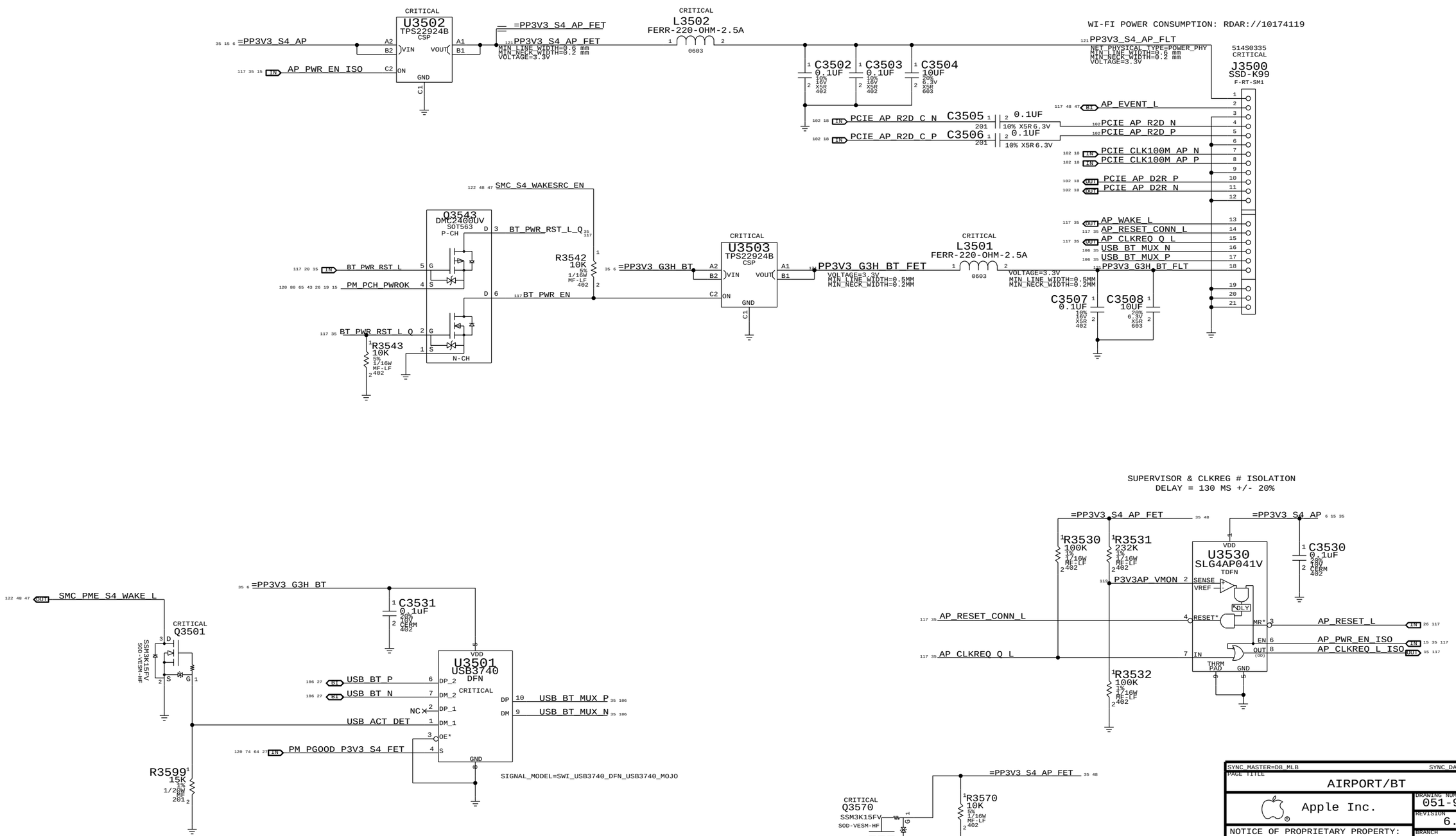
# AIRPORT BLUETOOTH

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PAGE TITLE: AIRPORT/BT

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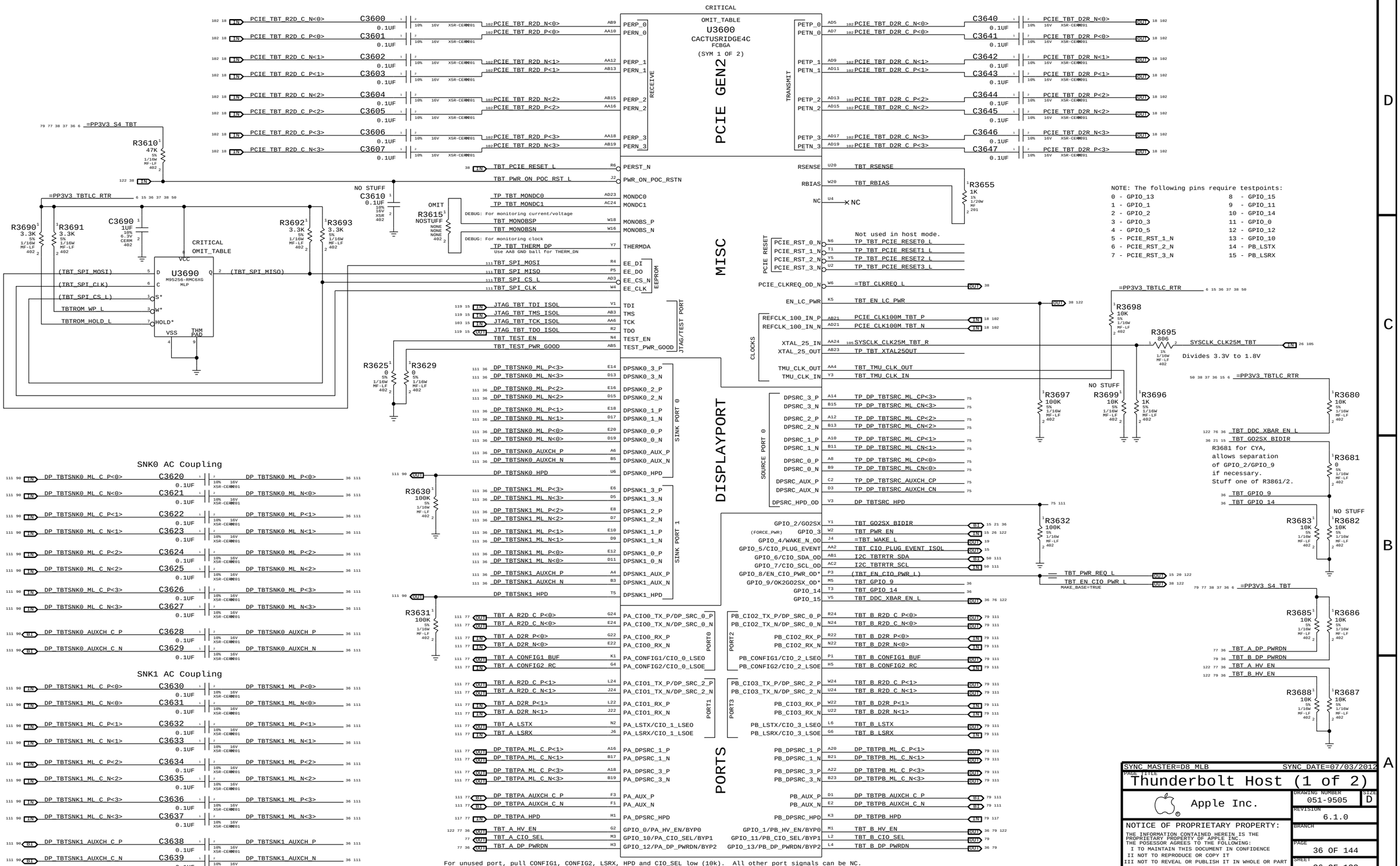


SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# Thunderbolt Host (1 of 2)

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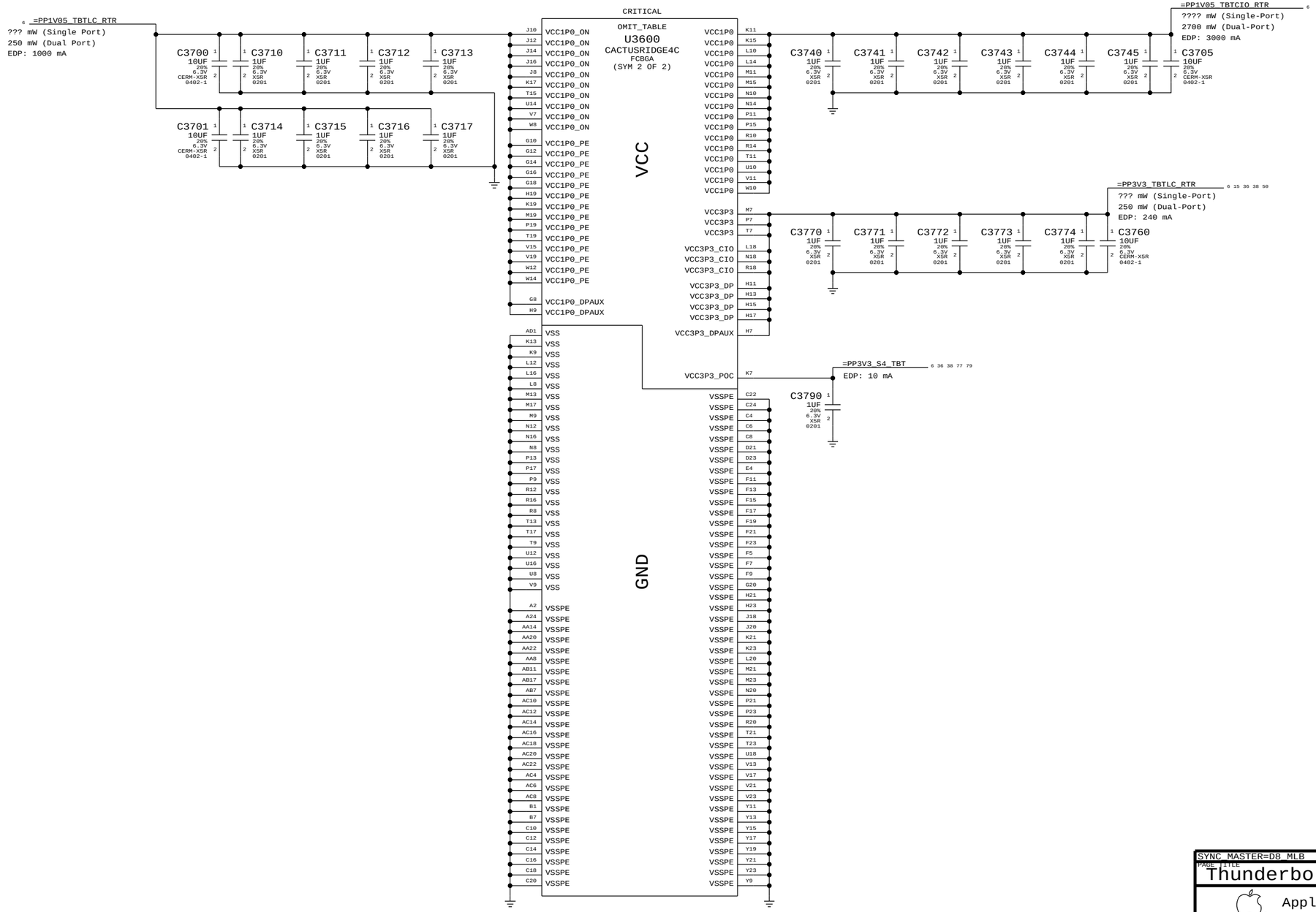


EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# Thunderbolt Host (2 of 2)

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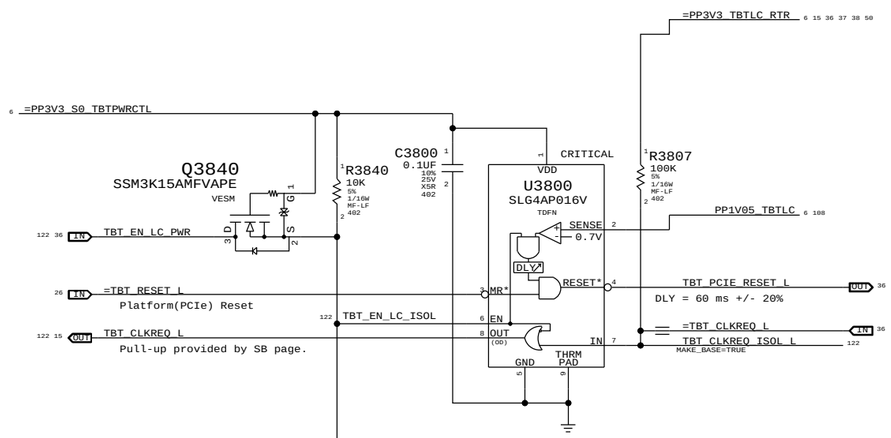
# Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

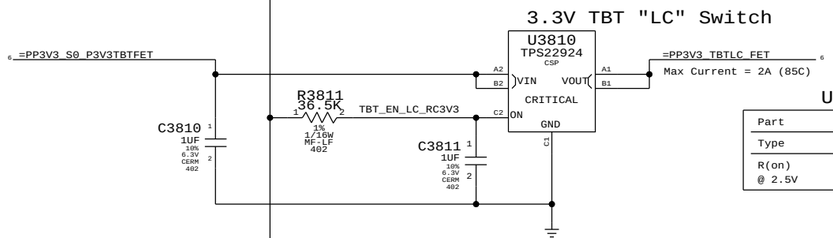
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

## Supervisor & CLKREQ# Isolation




## 3.3V TBT "LC" Switch

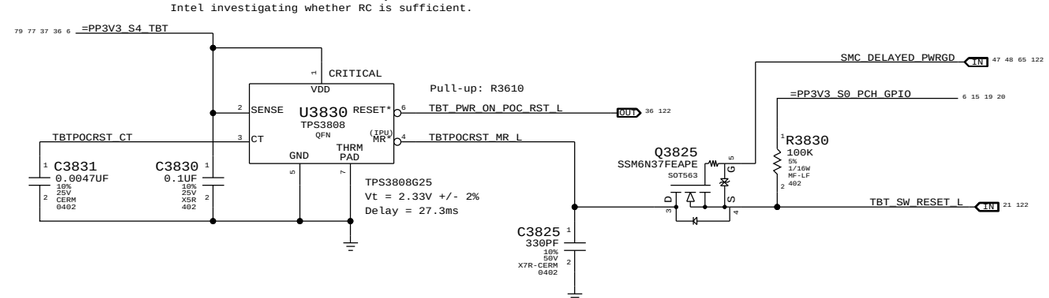



### U3810

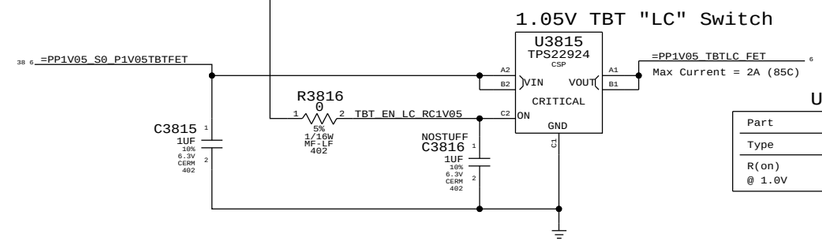
| Part | TPS22924C |
|---|---|
| Type | Load Switch |
| R(on) @ 2.5V | 18.5 mOhm Typ<br>25.8 mOhm Max |

## TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



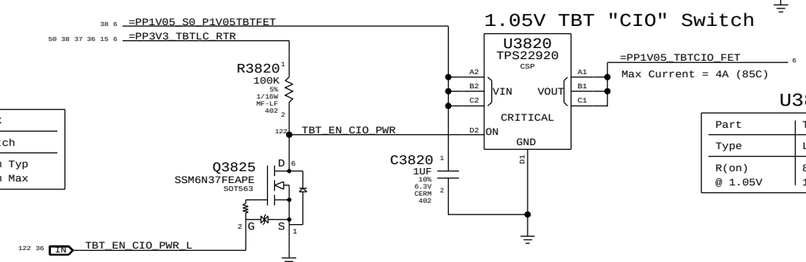

## 1.05V TBT "LC" Switch




### U3815

| Part | TPS22924C |
|---|---|
| Type | Load Switch |
| R(on) @ 1.0V | 20.3 mOhm Typ<br>28.6 mOhm Max |

## 1.05V TBT "CIO" Switch




### U3820

| Part | TPS22920 |
|---|---|
| Type | Load Switch |
| R(on) @ 1.05V | 8 mOhm Typ<br>11.5 mOhm Max |

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_S4_ENET_FET
281mA (1000base-T max power, Caesar IV)

R3901 0 5% 1/16W MF-LF 402

C3979 4.7UF 20% 6.3V X5R-CERM1 402

PP3V3_S4_ENET_FET_SRVDD — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

C3996 0.1UF 10% 16V X5R-CERM 0201

C3997 0.1UF 10% 16V X5R-CERM 0201

=PP3V3R1V8_CR_IOPWR_OUT
VDD for Card Reader I/O

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402

PP3V3_S4_ENET_FET_XTALVDDH — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

C3900 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402

PP3V3_S4_ENET_FET_BIASVDDH — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402

PP3V3_S4_ENET_FET_AVDDH — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402

C3910 0.1UF 10% 16V X5R-CERM 0201

C3911 0.1UF 10% 16V X5R-CERM 0201

C3912 1.0UF 10% 6.3V X5R-CERM 0201

C3915 4.7UF 20% 6.3V X5R-CERM 402

C3999 0.1UF 10% 16V X5R-CERM 0201

C3998 0.1UF 10% 16V X5R-CERM 0201

C3916 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/16W MF-LF 402

R3941 4.7K 5% 1/16W MF-LF 402

=PP3V3_S0_ENET

Current Limiting Resistor R3942 1K 5% 1/16W MF-LF 402

C3950 0.1UF 10% 16V X5R-CERM 0201

C3951 0.1UF 10% 16V X5R-CERM 0201

C3955 0.1UF 10% 16V X5R-CERM 0201

C3956 0.1UF 10% 16V X5R-CERM 0201

=ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_SR_LX
ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_S4_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402

PP1V2_S4_ENET_PHY_AVDDL — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V

C3921 0.1UF 10% 16V X5R-CERM 0201

C3920 4.7UF 20% 6.3V X5R-CERM1 402

C3913 1.0UF 10% 6.3V X5R-CERM 0201

CRITICAL L3925 FERR-600-OHM-0.5A SM

PP1V2_S4_ENET_PHY_PCIEPLL — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V

C3926 0.1UF 10% 16V X5R-CERM 0201

C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402

PP1V2_S4_ENET_PHY_GPHYPLL — MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=1.2V

C3931 0.1UF 10% 16V X5R-CERM 0201

C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201

C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

OMIT_TABLE
U3900
BCM57765
QFN-8X8

| Pin | Signal | Net |
|---|---|---|
| 42, 48 | AVDDH | |
| 37 | BIASVDDH | |
| 17 | XTALVDDH | |
| 7, 20, 56, 62 | VDDO | |
| 14 | SR_VDD | |
| 15 | SR_VDDP | |
| 16 | SR_LX | ENET_SR_LX |
| 13 | SR_VFB | ENET_SR_VFB |
| 39, 45, 51 | AVDDL | |
| 29, 32 | PCIE_PLLVDDL | |
| 36 | GPHY_PLLVDDL | |
| 35, 61 | VDDC | |
| 58 | VMAIN_PRSNT (IPD-ENET) | ENET_VMAIN_PRSNT |
| 27 | PCIE_TXD_N | PCIE_ENET_D2R_C_N |
| 28 | PCIE_TXD_P | PCIE_ENET_D2R_C_P |
| 33 | PCIE_RXD_P | PCIE_ENET_R2D_P |
| 34 | PCIE_RXD_N | PCIE_ENET_R2D_N |
| 31 | PCIE_REFCLK_P | PCIE_CLK100M_ENET_P |
| 30 | PCIE_REFCLK_N | PCIE_CLK100M_ENET_N |
| 11 | PERST* (IPD) | ENET_RESET_L |
| 12 | CLKREQ* (OD) | ENET_CLKREQ_L_Q |
| 3 | WAKE* (OD) | |
| 4 | LOW_PWR (IPD) | ENET_LOW_PWR |
| 6 | SMB_CLK | SMB_ENET_SCL |
| 10 | SMD_DATA (IPD-ENETM) | SMB_ENET_SDA |
| 66 | SCLK | ENET_SCLK |
| 64 | SI/LINKLED* | ENET_MISO |
| 65 | SO | ENET_MOSI |
| 63 | CS* | ENET_CS_L |
| 2 | SPD100LED*/SERIAL_DO (OD) | TP_ENET_CR_3V3_EN_L |
| 67 | TRAFFICLED*/SERIAL_DI (OD) | ENET_TRAFFICLED_L |
| 18 | XTALI | SYSCLK_CLK25M_ENET |
| 19 | XTALO | NC |
| 38 | RDAC | ENET_RDAC |
| 69 | THRM_PAD (NO IPU OR IPD-ENET) | |

NOTE: "IPx" == Programmable pull-up/down

| Pin | Signal | Net |
|---|---|---|
| 40 | TRD0_P | ENETCONN_MDI_P<0> |
| 41 | TRD0_N | ENETCONN_MDI_N<0> |
| 44 | TRD1_P | ENETCONN_MDI_P<1> |
| 43 | TRD1_N | ENETCONN_MDI_N<1> |
| 46 | TRD2_P | ENETCONN_MDI_P<2> |
| 47 | TRD2_N | ENETCONN_MDI_N<2> |
| 50 | TRD3_P | ENETCONN_MDI_P<3> |
| 49 | TRD3_N | ENETCONN_MDI_N<3> |
| 5 | GPIO_0 (IPD) | TP_ENET_CR_1V8_EN |
| 8 | GPIO_1/CR_BUS_PWR (IPD) | PP3V3R1V8_ENET_LR_OUT_REG |
| 9 | RE*/GPIO_2 (IPD) | ENET_MEDIA_SENSE |
| 1 | SD_DETECT/WE* (IPx-ENETM) | ENET_SD_DETECT_L |
| 26 | CR_CMD/CLE (IPU-ENET) | ENET_SD_CMD |
| 21 | CR_CLK/RY_BY* | ENET_SD_CLK |
| 25 | CR_DATA0 (IPU-ENET) | ENET_CR_DATA<0> |
| 24 | CR_DATA1 | ENET_CR_DATA<1> |
| 23 | CR_DATA2 | ENET_CR_DATA<2> |
| 22 | CR_DATA3 | ENET_CR_DATA<3> |
| 52 | CR_DATA4 | ENET_CR_DATA<4> |
| 53 | CR_DATA5 | ENET_CR_DATA<5> |
| 54 | CR_DATA6 | ENET_CR_DATA<6> |
| 55 | CR_DATA7 | ENET_CR_DATA<7> |
| 59 | CE*/MS_INS* (IPU-ENET) | NC_ENET_CE_L_MS_INS_L |
| 60 | CR_LED/ALE (IPU-ENET) | ENET_CR_PWREN |
| 57 | CR_WP*/XD_WP* (IPU-ENET) | |
| 68 | XD_DETECT (IPU-ENET) | ENET_SR_DISABLE |

SD_DETECT can only be used active low due to errata.

MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.3V, MAKE_BASE=TRUE — =PP3V3R1V8_CR_IOPWR_OUT

R3961 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.26:5MM — SDCONN_CMD
R3979 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.21:5MM — SDCONN_CLK
R3971 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.25:5MM — SDCONN_DATA<0>
R3972 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.24:5MM — SDCONN_DATA<1>
R3973 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.23:5MM — SDCONN_DATA<2>
R3974 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.22:5MM — SDCONN_DATA<3>
R3975 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.52:5MM — SDCONN_DATA<4>
R3976 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.53:5MM — SDCONN_DATA<5>
R3977 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.54:5MM — SDCONN_DATA<6>
R3978 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.55:5MM — SDCONN_DATA<7>

NO_TEST=TRUE
No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3981 1K 5% 1/16W MF-LF 402

SDCONN_WP

ENET supports both active-levels for WP.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
IF ENET SWITCHING REGULATOR IS USED, THIS PIN SHOULD HAVE A 1K PD TO GND

R3965 1.24K 1% 1/16W MF-LF 402

## PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_S4_ENET_FET

C3990 0.1UF 10% 16V X5R-CERM 0201

U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE

| Pin | Signal | Net |
|---|---|---|
| 8 | VCC | |
| 2 | SCK | ENET_SCLK |
| 4 | CS* | ENET_CS_L |
| 5 | WP* | |
| 3 | RESET* | |
| 1 | SI | ENET_MOSI |
| 8 | SO | ENET_MISO |
| 7 | GND | |

NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402

R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
ETHERNET PHY (CAESAR IV+)

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D
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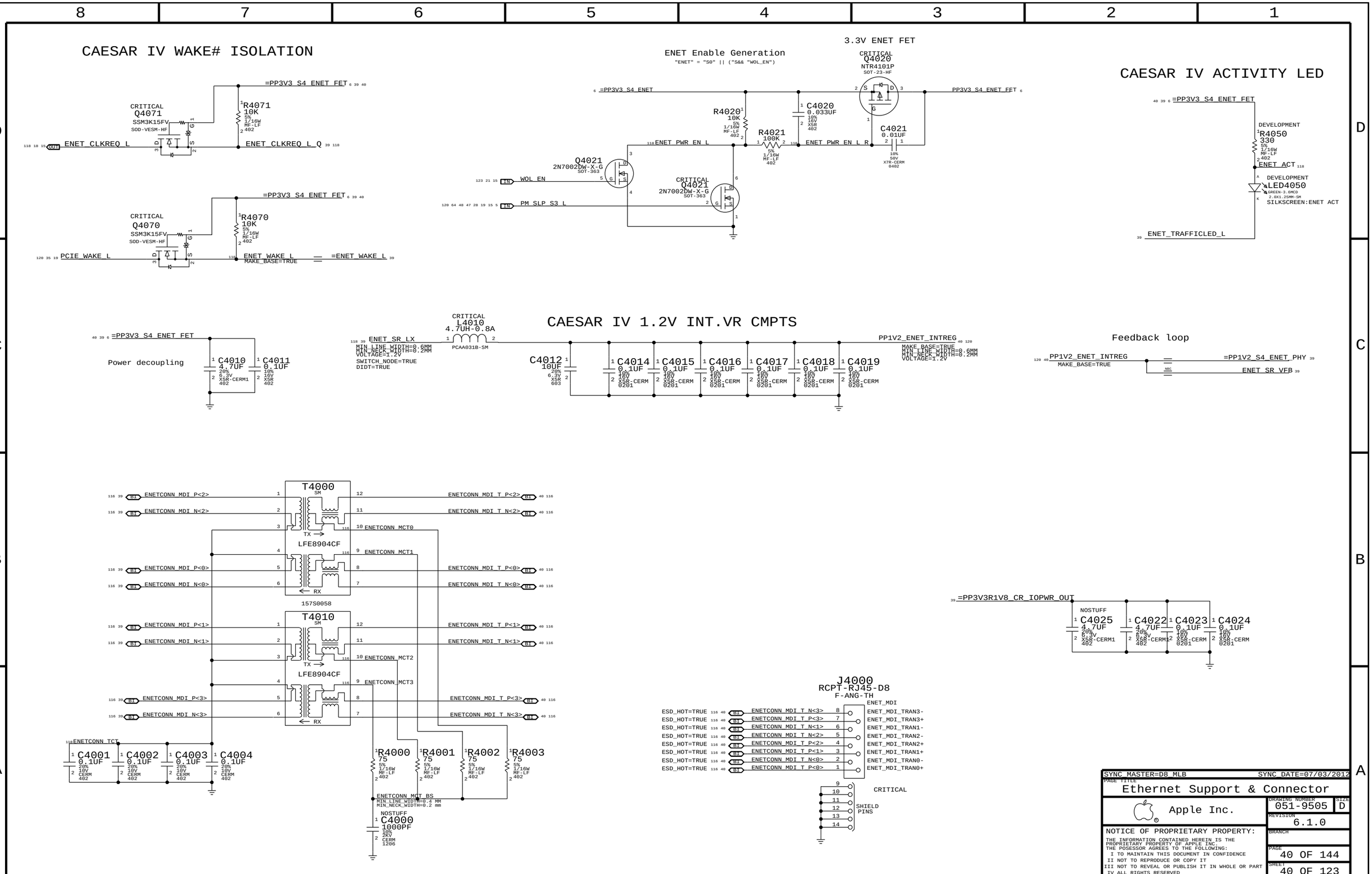
CAESAR IV WAKE# ISOLATION
CRITICAL
Q4071
SSM3K15FV
SOD-VESM-HF
R4071
10K
5%
1/16W
MF-LF
402
=PP3V3_S4_ENET_FET
ENET_CLKREQ_L
ENET_CLKREQ_L_Q
CRITICAL
Q4070
SSM3K15FV
SOD-VESM-HF
R4070
10K
5%
1/16W
MF-LF
402
=PP3V3_S4_ENET_FET
PCIE_WAKE_L
ENET_WAKE_L
MAKE_BASE=TRUE
=ENET_WAKE_L
3.3V ENET FET
ENET Enable Generation
"ENET" = "S0" || ("S&& "WOL_EN")
CRITICAL
Q4020
NTR4101P
SOT-23-HF
=PP3V3_S4_ENET
PP3V3_S4_ENET_FET
R4020
10K
5%
1/16W
MF-LF
402
C4020
0.033UF
10%
16V
X5R
402
R4021
100K
5%
1/16W
MF-LF
402
C4021
0.01UF
10%
50V
X7R-CERM
0402
ENET_PWR_EN_L
ENET_PWR_EN_L_R
Q4021
2N7002DW-X-G
SOT-363
WOL_EN
CRITICAL
Q4021
2N7002DW-X-G
SOT-363
PM_SLP_S3_L
CAESAR IV ACTIVITY LED
=PP3V3_S4_ENET_FET
DEVELOPMENT
R4050
330
5%
1/16W
MF-LF
402
ENET_ACT
DEVELOPMENT
LED4050
GREEN-3.6MCD
2.0X1.25MM-SM
SILKSCREEN:ENET ACT
ENET_TRAFFICLED_L
=PP3V3_S4_ENET_FET
Power decoupling
C4010
4.7UF
20%
6.3V
X5R-CERM1
402
C4011
0.1UF
10%
16V
X5R
402
CRITICAL
L4010
4.7UH-0.8A
PCAA031B-SM
ENET_SR_LX
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE
CAESAR IV 1.2V INT.VR CMPTS
C4012
10UF
20%
6.3V
X5R
603
C4014
C4015
C4016
C4017
C4018
C4019
0.1UF
10%
16V
X5R-CERM
0201
PP1V2_ENET_INTREG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
Feedback loop
PP1V2_ENET_INTREG
MAKE_BASE=TRUE
=PP1V2_S4_ENET_PHY
ENET_SR_VFB
T4000
SM
LFE8904CF
157S0058
T4010
SM
LFE8904CF
TX
RX
ENETCONN_MDI_P<2>
ENETCONN_MDI_N<2>
ENETCONN_MDI_P<0>
ENETCONN_MDI_N<0>
ENETCONN_MDI_P<1>
ENETCONN_MDI_N<1>
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>
ENETCONN_MDI_T_P<2>
ENETCONN_MDI_T_N<2>
ENETCONN_MDI_T_P<0>
ENETCONN_MDI_T_N<0>
ENETCONN_MDI_T_P<1>
ENETCONN_MDI_T_N<1>
ENETCONN_MDI_T_P<3>
ENETCONN_MDI_T_N<3>
ENETCONN_MCT0
ENETCONN_MCT1
ENETCONN_MCT2
ENETCONN_MCT3
ENETCONN_TCT
C4001
C4002
C4003
C4004
0.1UF
20%
10V
CERM
402
R4000
R4001
R4002
R4003
75
5%
1/16W
MF-LF
402
ENETCONN_MCT_BS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NOSTUFF
C4000
1000PF
10%
2KV
CERM
1206
=PP3V3R1V8_CR_IOPWR_OUT
NOSTUFF
C4025
C4022
C4023
C4024
4.7UF
20%
6.3V
X5R-CERM1
402
0.1UF
10%
16V
X5R-CERM
0201
J4000
RCPT-RJ45-D8
F-ANG-TH
ENET_MDI
ESD_HOT=TRUE
ENETCONN_MDI_T_N<3>
ENETCONN_MDI_T_P<3>
ENETCONN_MDI_T_N<1>
ENETCONN_MDI_T_N<2>
ENETCONN_MDI_T_P<2>
ENETCONN_MDI_T_P<1>
ENETCONN_MDI_T_N<0>
ENETCONN_MDI_T_P<0>
ENET_MDI_TRAN3-
ENET_MDI_TRAN3+
ENET_MDI_TRAN1-
ENET_MDI_TRAN2-
ENET_MDI_TRAN2+
ENET_MDI_TRAN1+
ENET_MDI_TRAN0-
ENET_MDI_TRAN0+
CRITICAL
SHIELD PINS
SYNC_MASTER=D8_MLB
SYNC_DATE=07/03/2012
PAGE TITLE
Ethernet Support & Connector
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
D
REVISION
6.1.0
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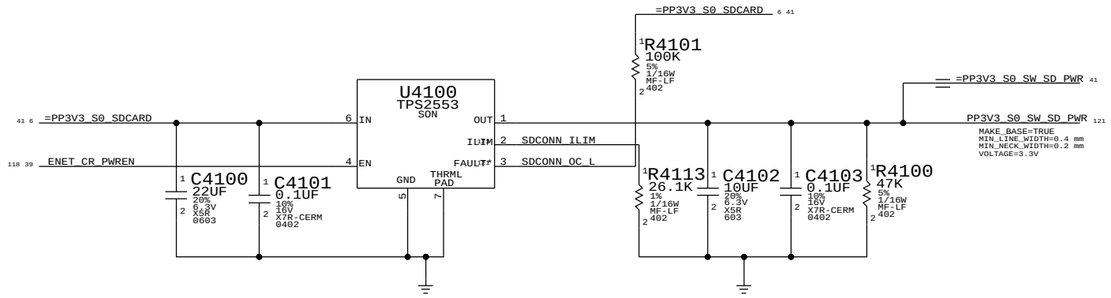
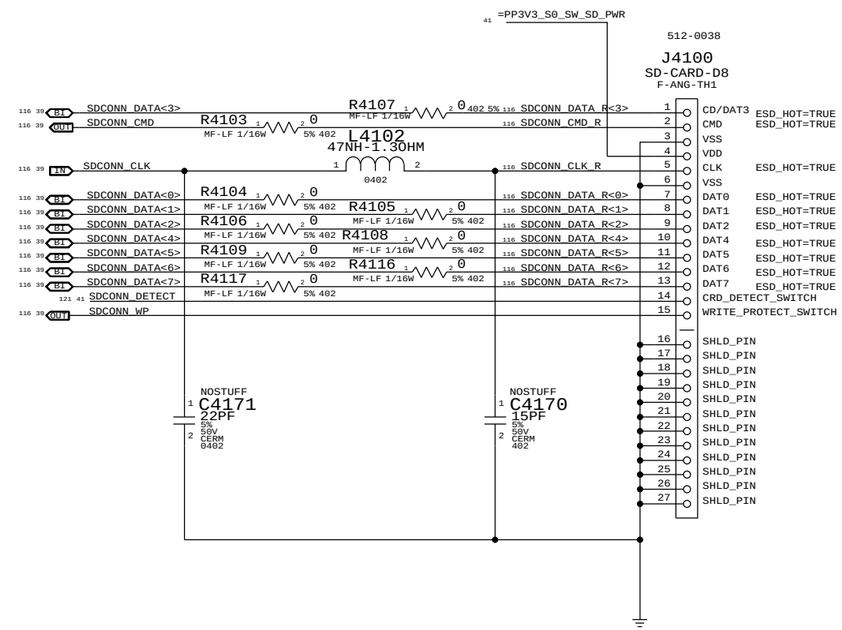
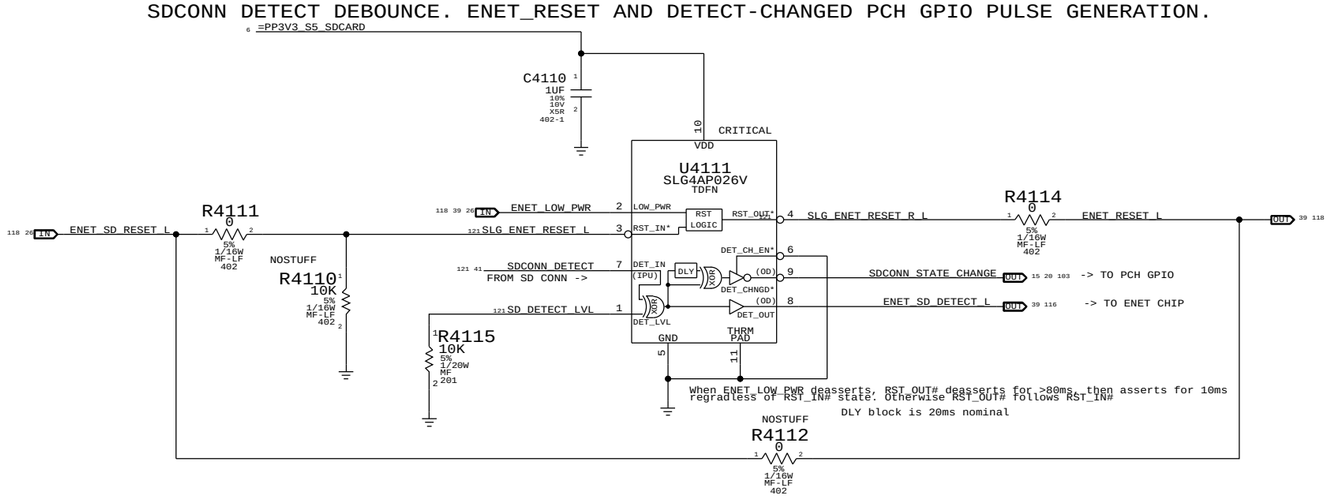
## SD CARD 3.3V OVERCURRENT PROTECTION




## SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.

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PAGE TITLE
# SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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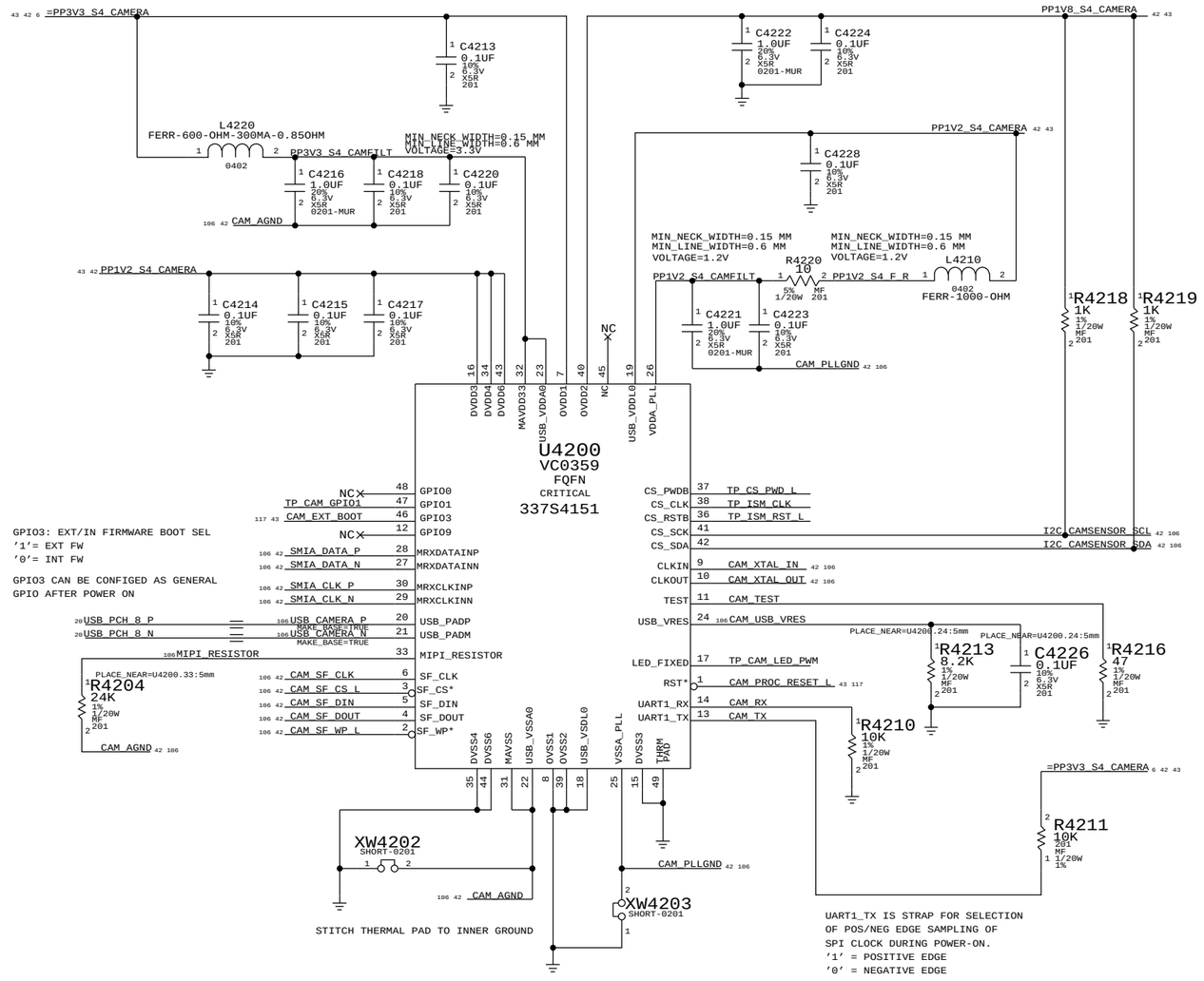
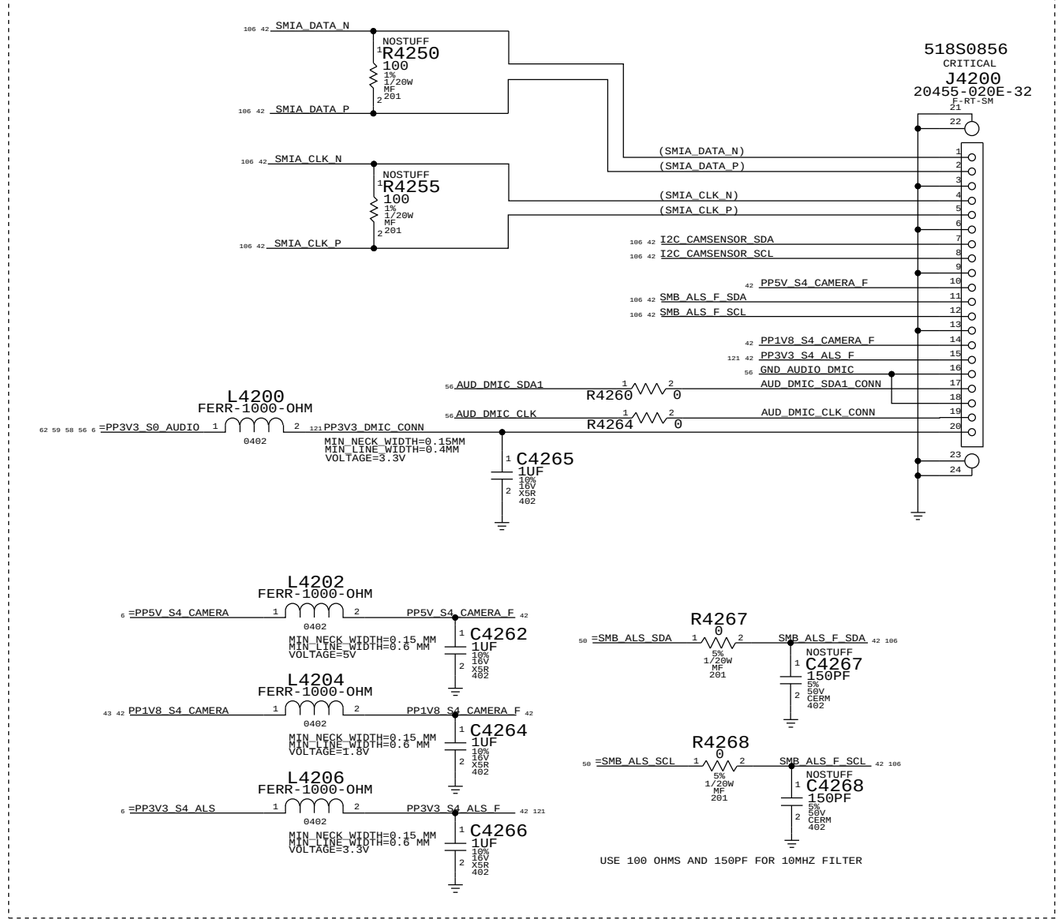
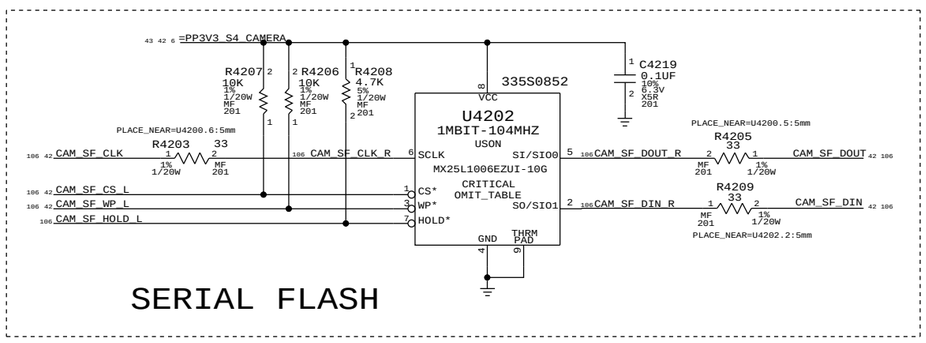
# USB CAMERA CONTROLLER

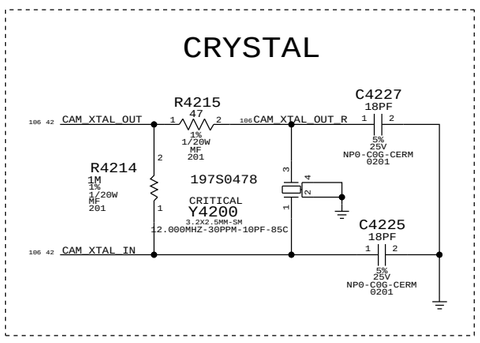



## CAMERA/ALS/DMIC CONNECTOR




SERIAL FLASH

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PAGE TITLE: Camera Controller

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

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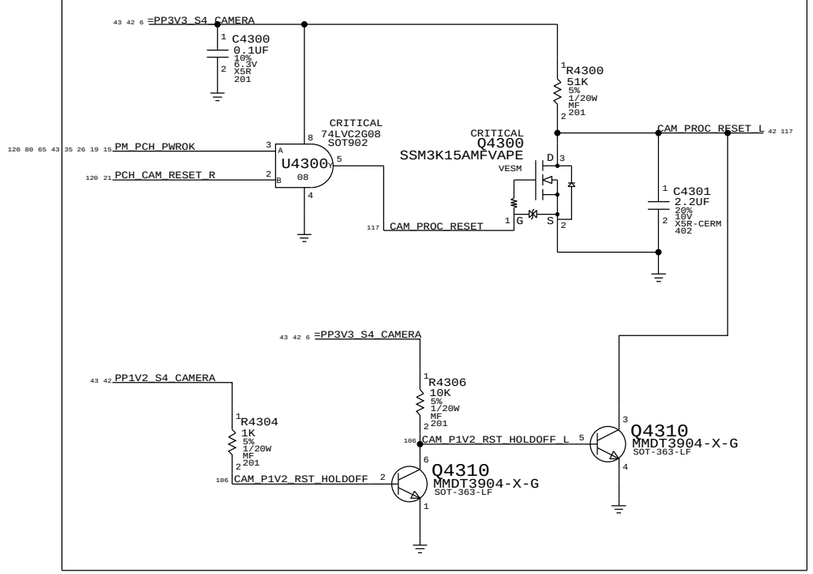
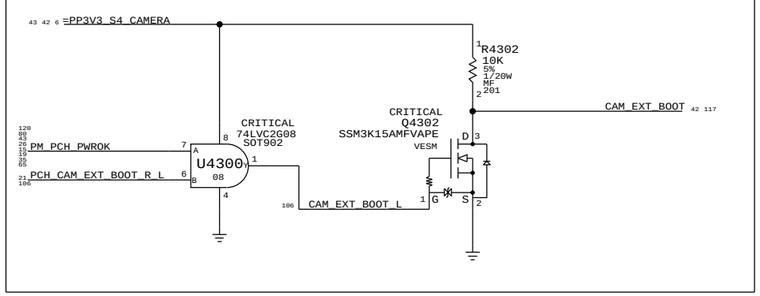
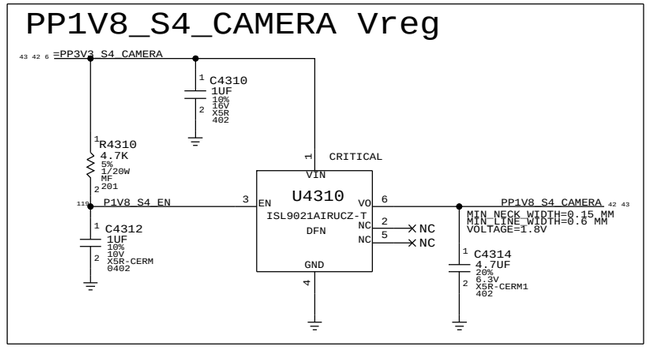
## Camera Processor Reset



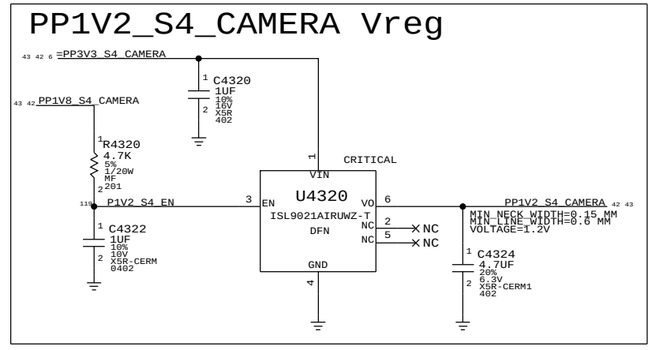

## Camera Processor ExtBoot Cntl




## PP1V8_S4_CAMERA Vreg




## PP1V2_S4_CAMERA Vreg

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PAGE TITLE
# Camera Controller Support

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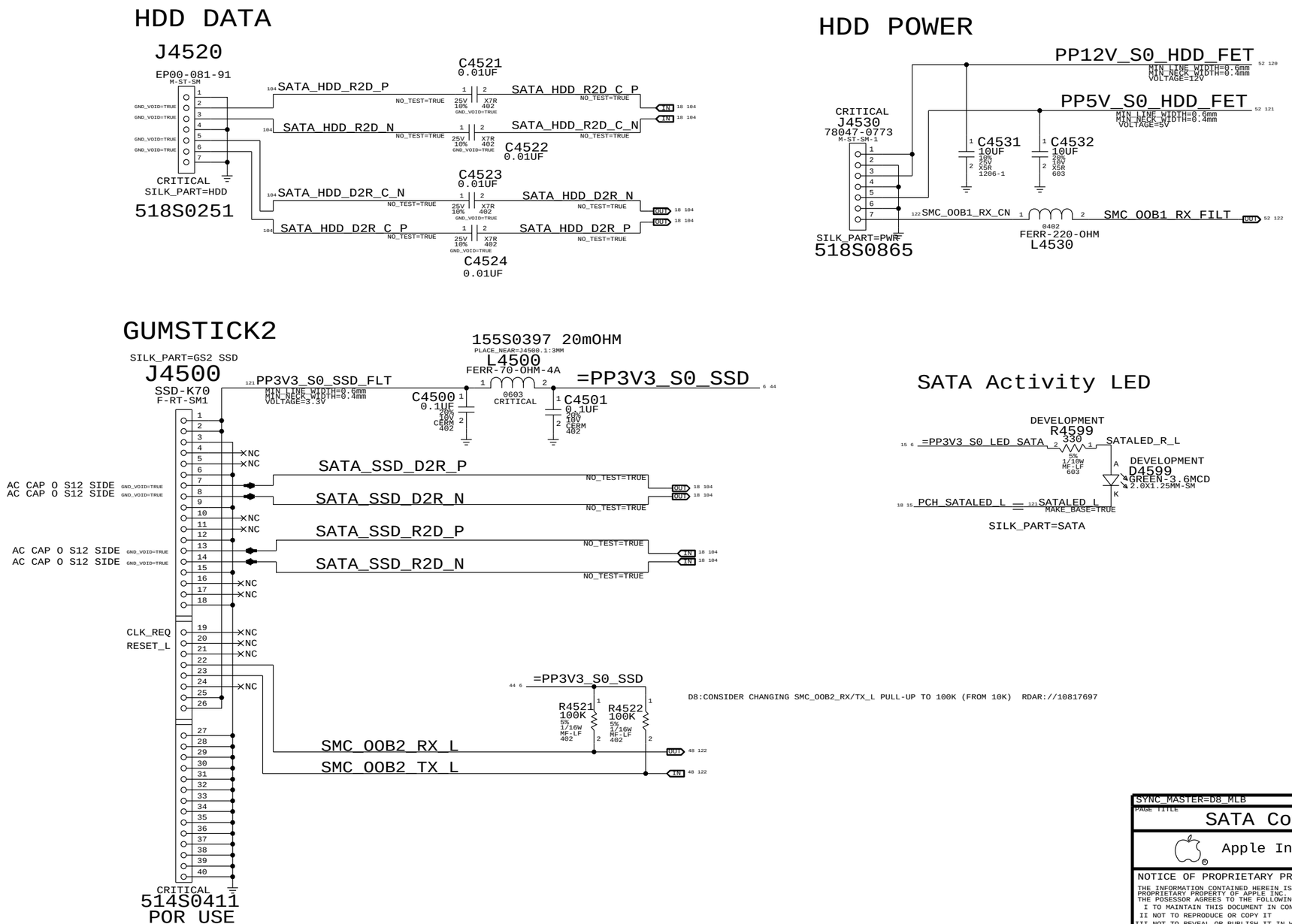


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PAGE TITLE
SATA Connectors

Apple Inc.

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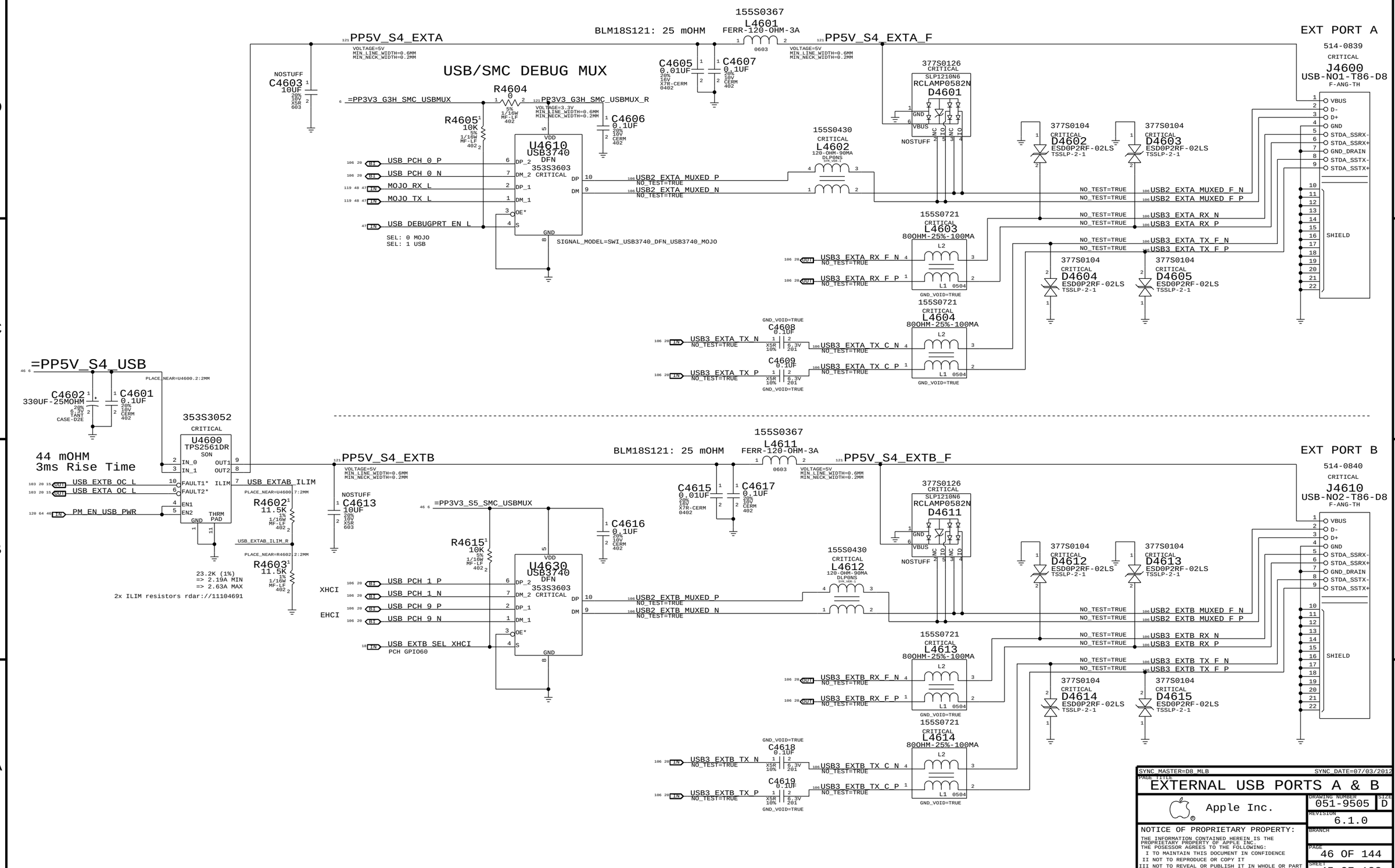
USB/SMC DEBUG MUX
PP5V_S4_EXTA
PP5V_S4_EXTA_F
EXT PORT A
514-0839
J4600
USB-NO1-T86-D8
PP5V_S4_EXTB
PP5V_S4_EXTB_F
EXT PORT B
514-0840
J4610
USB-NO2-T86-D8
=PP5V_S4_USB
44 mOHM
3ms Rise Time
U4600
TPS2561DR
U4610
USB3740
U4630
USB3740
=PP3V3_S5_SMC_USBMUX
XHCI
EHCI
USB_EXTB_SEL_XHCI
PCH GPIO60
SHIELD
EXTERNAL USB PORTS A & B
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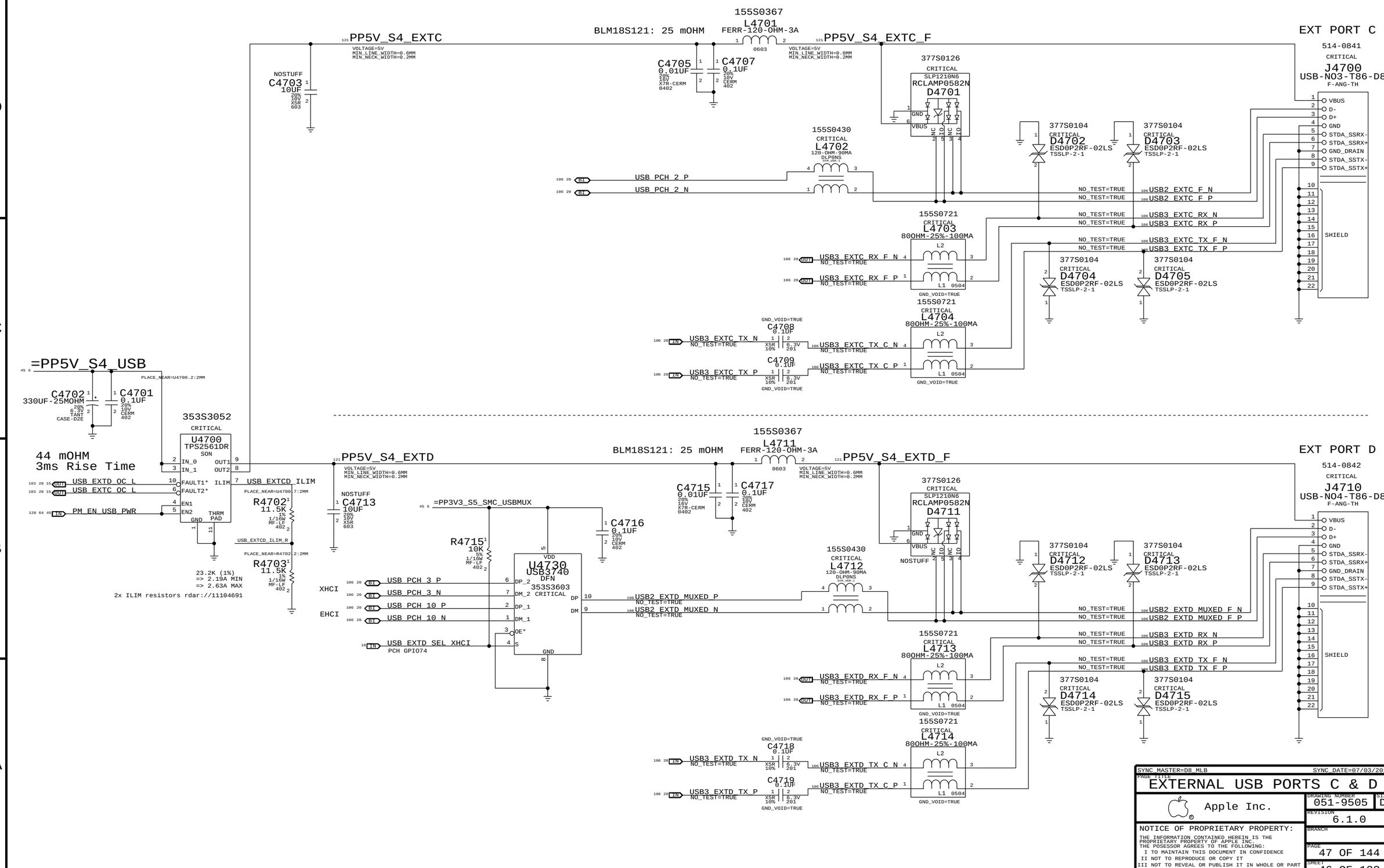


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PAGE TITLE
# EXTERNAL USB PORTS C & D

Apple Inc.

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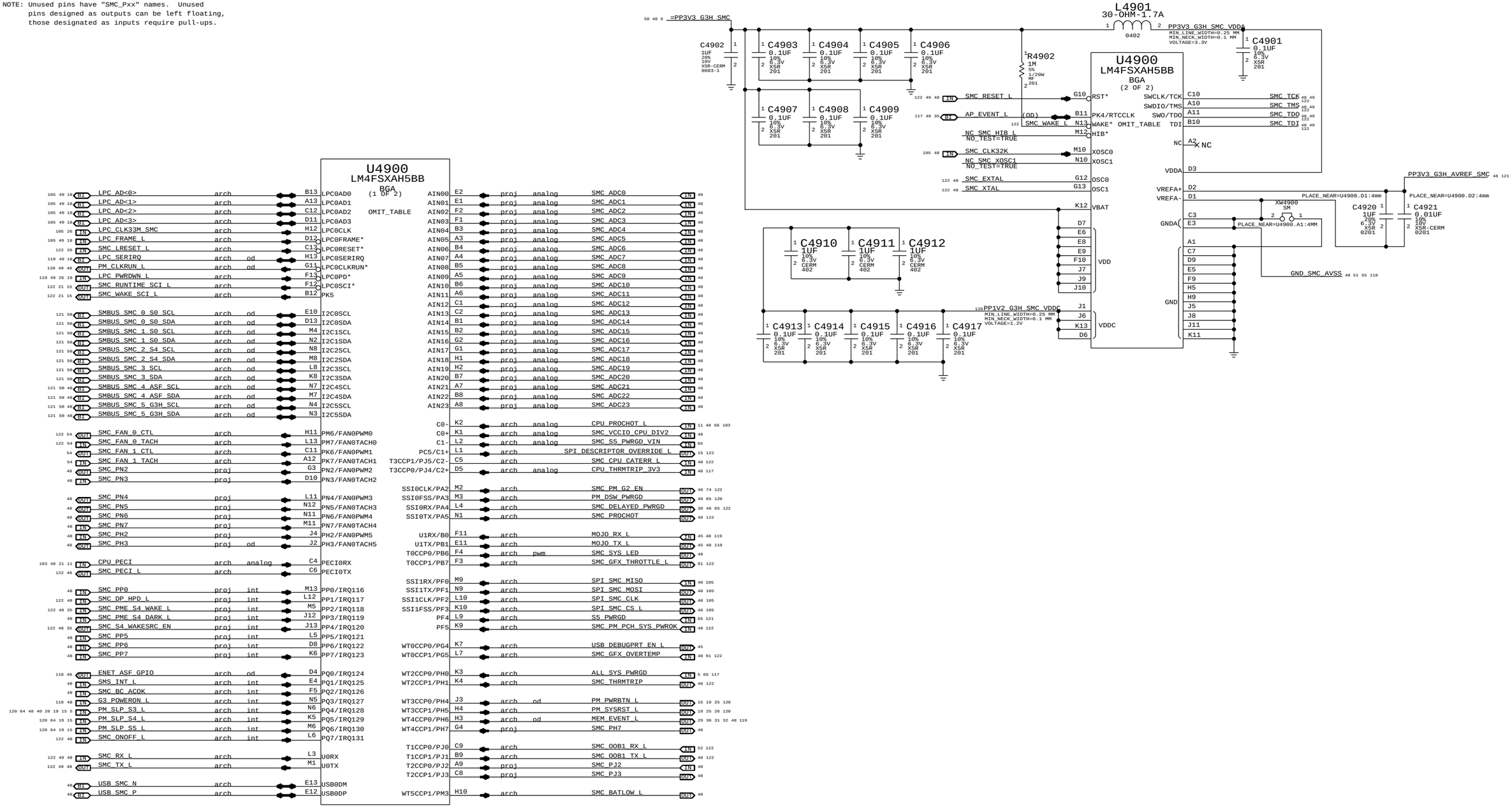
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# SMC

Apple Inc.

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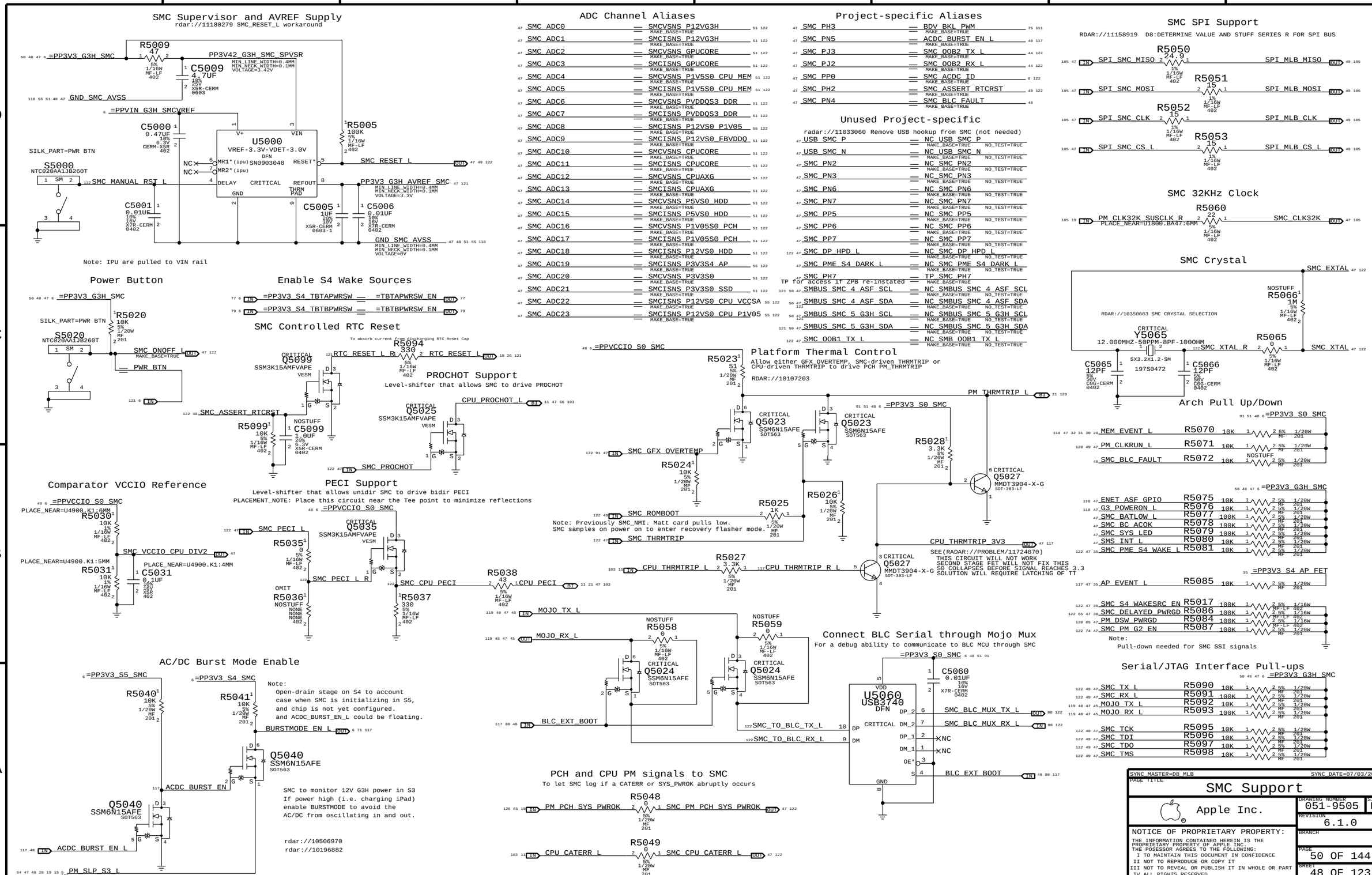
SMC Supervisor and AVREF Supply
rdar://11180279 SMC_RESET_L workaround
R5009 47
=PP3V3_G3H_SMC
PP3V42_G3H_SMC_SPVSR
C5009 4.7UF
GND_SMC_AVSS
=PPVIN_G3H_SMCVREF
C5000 0.47UF
U5000
VREF-3.3V-VDET-3.0V
DFN
SN0903048
R5005 100K
SILK_PART=PWR BTN
S5000
NTC020AA1JB260T
SMC_MANUAL_RST_L
SMC_RESET_L
PP3V3_G3H_AVREF_SMC
C5001 0.01UF
C5005 1UF
C5006 0.01UF
GND_SMC_AVSS
Note: IPU are pulled to VIN rail
Power Button
=PP3V3_G3H_SMC
R5020 10K
S5020
NTC020AA1JB260T
SMC_ONOFF_L
PWR_BTN
Enable S4 Wake Sources
=PP3V3_S4_TBTAPWRSW
=TBTAPWRSW_EN
=PP3V3_S4_TBTBPWRSW
=TBTBPWRSW_EN
SMC Controlled RTC Reset
To absorb current from discharging RTC Reset Cap
R5094 330
RTC_RESET_L
Q5099
SSM3K15AMFVAPE
R5099 10K
C5099 1.0UF
SMC_ASSERT_RTCRST
PROCHOT Support
Level-shifter that allows SMC to drive PROCHOT
CPU_PROCHOT_L
Q5025
SSM3K15AMFVAPE
SMC_PROCHOT
Comparator VCCIO Reference
=PPVCCIO_S0_SMC
PLACE_NEAR=U4900.K1:6MM
R5030 10K
SMC_VCCIO_CPU_DIV2
PLACE_NEAR=U4900.K1:5MM
R5031 10K
C5031 0.1UF
PLACE_NEAR=U4900.K1:4MM
PECI Support
Level-shifter that allows unidir SMC to drive bidir PECI
PLACEMENT_NOTE: Place this circuit near the Tee point to minimize reflections
SMC_PECI_L
R5035 0
Q5035
SSM3K15AMFVAPE
SMC_PECI_L_R
R5036 0
SMC_CPU_PECI
R5037 330
R5038 43
CPU_PECI
AC/DC Burst Mode Enable
=PP3V3_S5_SMC
=PP3V3_S4_SMC
R5040 10K
R5041 10K
BURSTMODE_EN_L
Q5040
SSM6N15AFE
ACDC_BURST_EN
Q5040
SSM6N15AFE
ACDC_BURST_EN_L
PM_SLP_S3_L
Note:
Open-drain stage on S4 to account
case when SMC is initializing in S5,
and chip is not yet configured.
and ACDC_BURST_EN_L could be floating.
SMC to monitor 12V G3H power in S3
If power high (i.e. charging iPad)
enable BURSTMODE to avoid the
AC/DC from oscillating in and out.
rdar://10506970
rdar://10196882
ADC Channel Aliases
SMC_ADC0 — SMCVSNS_P12VG3H
SMC_ADC1 — SMCISNS_P12VG3H
SMC_ADC2 — SMCVSNS_GPUCORE
SMC_ADC3 — SMCISNS_GPUCORE
SMC_ADC4 — SMCVSNS_P1V5S0_CPU_MEM
SMC_ADC5 — SMCISNS_P1V5S0_CPU_MEM
SMC_ADC6 — SMCVSNS_PVDDQS3_DDR
SMC_ADC7 — SMCISNS_PVDDQS3_DDR
SMC_ADC8 — SMCISNS_P12VS0_P1V05
SMC_ADC9 — SMCISNS_P12VS0_FBVDDQ
SMC_ADC10 — SMCVSNS_CPUCORE
SMC_ADC11 — SMCISNS_CPUCORE
SMC_ADC12 — SMCVSNS_CPUAXG
SMC_ADC13 — SMCISNS_CPUAXG
SMC_ADC14 — SMCVSNS_P5VS0_HDD
SMC_ADC15 — SMCISNS_P5VS0_HDD
SMC_ADC16 — SMCVSNS_P1V05S0_PCH
SMC_ADC17 — SMCISNS_P1V05S0_PCH
SMC_ADC18 — SMCISNS_P12VS0_HDD
SMC_ADC19 — SMCISNS_P3V3S4_AP
SMC_ADC20 — SMCVSNS_P3V3S0
SMC_ADC21 — SMCISNS_P3V3S0_SSD
SMC_ADC22 — SMCISNS_P12VS0_CPU_VCCSA
SMC_ADC23 — SMCISNS_P12VS0_CPU_P1V05
Project-specific Aliases
SMC_PH3 — BDV_BKL_PWM
SMC_PN5 — ACDC_BURST_EN_L
SMC_PJ3 — SMC_OOB2_TX_L
SMC_PJ2 — SMC_OOB2_RX_L
SMC_PP0 — SMC_ACDC_ID
SMC_PH2 — SMC_ASSERT_RTCRST
SMC_PN4 — SMC_BLC_FAULT
Unused Project-specific
radar://11033060 Remove USB hookup from SMC (not needed)
USB_SMC_P — NC_USB_SMC_P
USB_SMC_N — NC_USB_SMC_N
SMC_PN2 — NC_SMC_PN2
SMC_PN3 — NC_SMC_PN3
SMC_PN6 — NC_SMC_PN6
SMC_PN7 — NC_SMC_PN7
SMC_PP5 — NC_SMC_PP5
SMC_PP6 — NC_SMC_PP6
SMC_PP7 — NC_SMC_PP7
SMC_DP_HPD_L — NC_SMC_DP_HPD_L
SMC_PME_S4_DARK_L — NC_SMC_PME_S4_DARK_L
SMC_PH7 — TP_SMC_PH7
TP for access if ZPB re-instated
SMBUS_SMC_4_ASF_SCL — NC_SMBUS_SMC_4_ASF_SCL
SMBUS_SMC_4_ASF_SDA — NC_SMBUS_SMC_4_ASF_SDA
SMBUS_SMC_5_G3H_SCL — NC_SMBUS_SMC_5_G3H_SCL
SMBUS_SMC_5_G3H_SDA — NC_SMBUS_SMC_5_G3H_SDA
SMC_OOB1_TX_L — NC_SMB_OOB1_TX_L
Platform Thermal Control
Allow either GFX_OVERTEMP, SMC-driven THRMTRIP or
CPU-driven THRMTRIP to drive PCH PM_THRMTRIP
RDAR://10107203
R5023 51
Q5023
SSM6N15AFE
SMC_GFX_OVERTEMP
R5024 10K
R5028 3.3K
Q5027
MMDT3904-X-G
PM_THRMTRIP_L
R5025 1K
SMC_ROMBOOT
Note: Previously SMC_NMI. Matt card pulls low.
SMC samples on power on to enter recovery flasher mode.
SMC_THRMTRIP
R5026 10K
R5027 3.3K
CPU_THRMTRIP_L
CPU_THRMTRIP_R_L
CPU_THRMTRIP_3V3
SEE(RADAR://PROBLEM/11724870)
THIS CIRCUIT WILL NOT WORK
SECOND STAGE FET WILL NOT FIX THIS
S0 COLLAPSES BEFORE SIGNAL REACHES 3.3
SOLUTION WILL REQUIRE LATCHING OF TT
Connect BLC Serial through Mojo Mux
For a debug ability to communicate to BLC MCU through SMC
MOJO_TX_L
MOJO_RX_L
R5058 0
R5059 0
Q5024
SSM6N15AFE
BLC_EXT_BOOT
U5060
USB3740
DFN
C5060 0.01UF
SMC_TO_BLC_TX_L
SMC_TO_BLC_RX_L
SMC_BLC_MUX_TX_L
SMC_BLC_MUX_RX_L
BLC_EXT_BOOT
PCH and CPU PM signals to SMC
To let SMC log if a CATERR or SYS_PWROK abruptly occurs
R5048 0
PM_PCH_SYS_PWROK
SMC_PM_PCH_SYS_PWROK
R5049 0
CPU_CATERR_L
SMC_CPU_CATERR_L
SMC SPI Support
RDAR://11158919 D8:DETERMINE VALUE AND STUFF SERIES R FOR SPI BUS
R5050 24.9
SPI_SMC_MISO
SPI_MLB_MISO
R5051 15
SPI_SMC_MOSI
SPI_MLB_MOSI
R5052 15
SPI_SMC_CLK
SPI_MLB_CLK
R5053 15
SPI_SMC_CS_L
SPI_MLB_CS_L
SMC 32KHz Clock
R5060 22
PM_CLK32K_SUSCLK_R
PLACE_NEAR=U1800.BA47:6MM
SMC_CLK32K
SMC Crystal
SMC_EXTAL
R5066 1M
RDAR://10350663 SMC CRYSTAL SELECTION
Y5065
12.000MHZ-50PPM-8PF-1000HM
5X3.2X1.2-SM
197S0472
SMC_XTAL_R
R5065 0
SMC_XTAL
C5065 12PF
C5066 12PF
Arch Pull Up/Down
=PP3V3_S0_SMC
MEM_EVENT_L R5070 10K
PM_CLKRUN_L R5071 10K
SMC_BLC_FAULT R5072 10K
=PP3V3_G3H_SMC
ENET_ASF_GPIO R5075 10K
G3_POWERON_L R5076 10K
SMC_BATLOW_L R5077 100K
SMC_BC_ACOK R5078 100K
SMC_SYS_LED R5079 100K
SMS_INT_L R5080 100K
SMC_PME_S4_WAKE_L R5081 10K
=PP3V3_S4_AP_FET
AP_EVENT_L R5085 10K
SMC_S4_WAKESRC_EN R5017 100K
SMC_DELAYED_PWRGD R5086 100K
PM_DSW_PWRGD R5084 100K
SMC_PM_G2_EN R5087 100K
Note:
Pull-down needed for SMC SSI signals
Serial/JTAG Interface Pull-ups
=PP3V3_G3H_SMC
SMC_TX_L R5090 10K
SMC_RX_L R5091 100K
MOJO_TX_L R5092 10K
MOJO_RX_L R5093 100K
SMC_TCK R5095 10K
SMC_TDI R5096 10K
SMC_TDO R5097 10K
SMC_TMS R5098 10K
SYNC MASTER=D8 MLB
SYNC DATE=07/03/2013
PAGE TITLE
SMC Support
Apple Inc.
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SIZE D
REVISION 6.1.0
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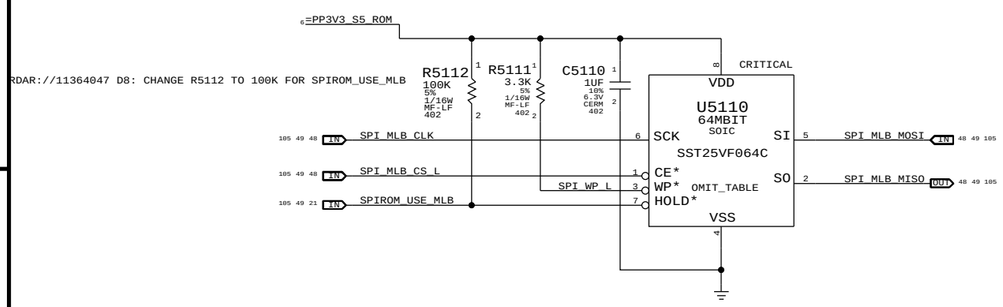
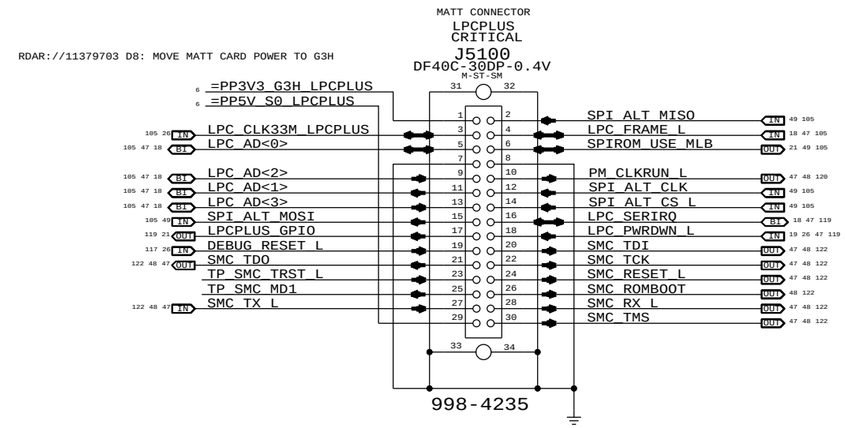
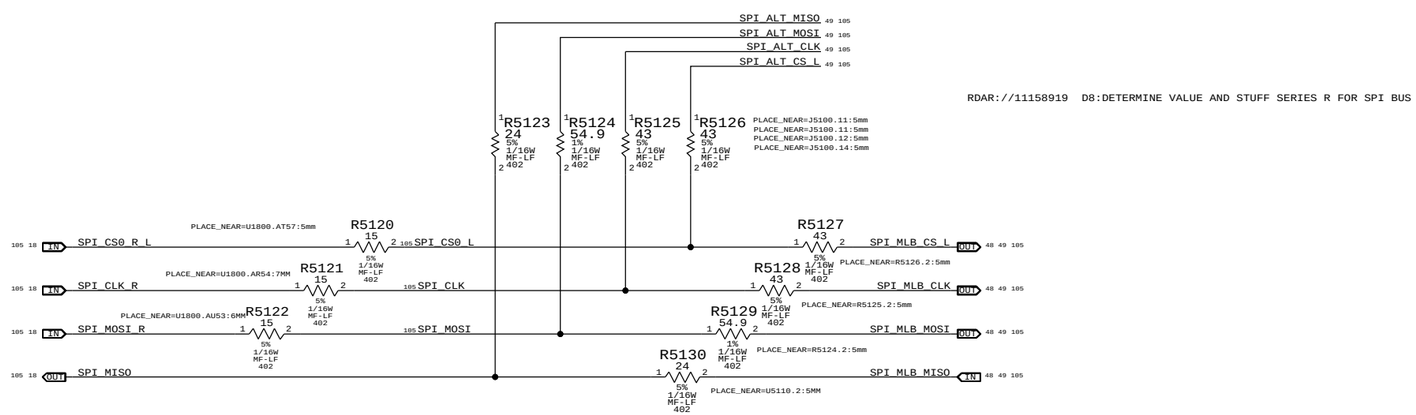
# SPI BootROM




# LPC+SPI Connector




# SPI Series Termination

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PAGE TITLE
SPI and Debug Connector

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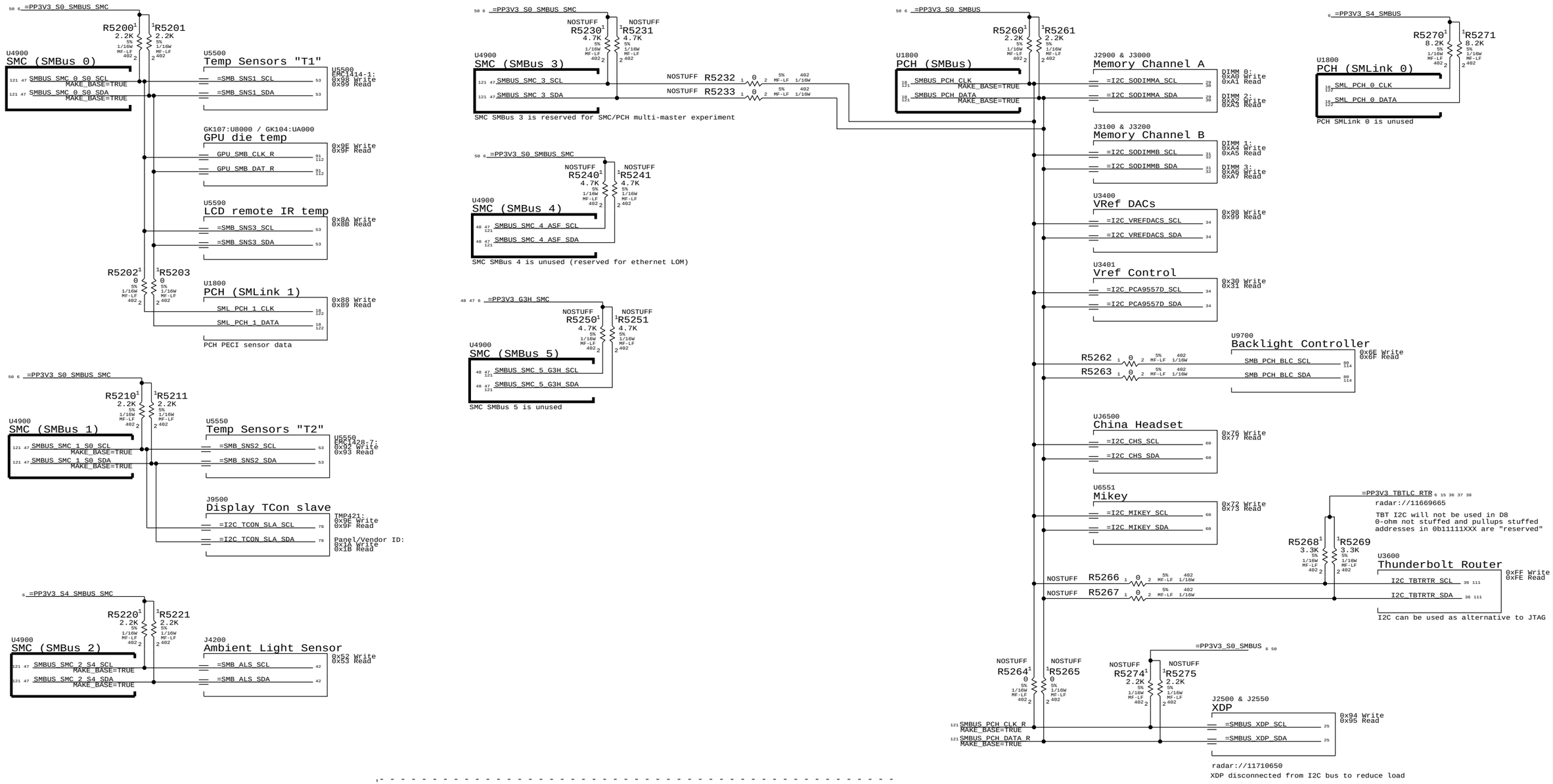


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# SMBus Connections

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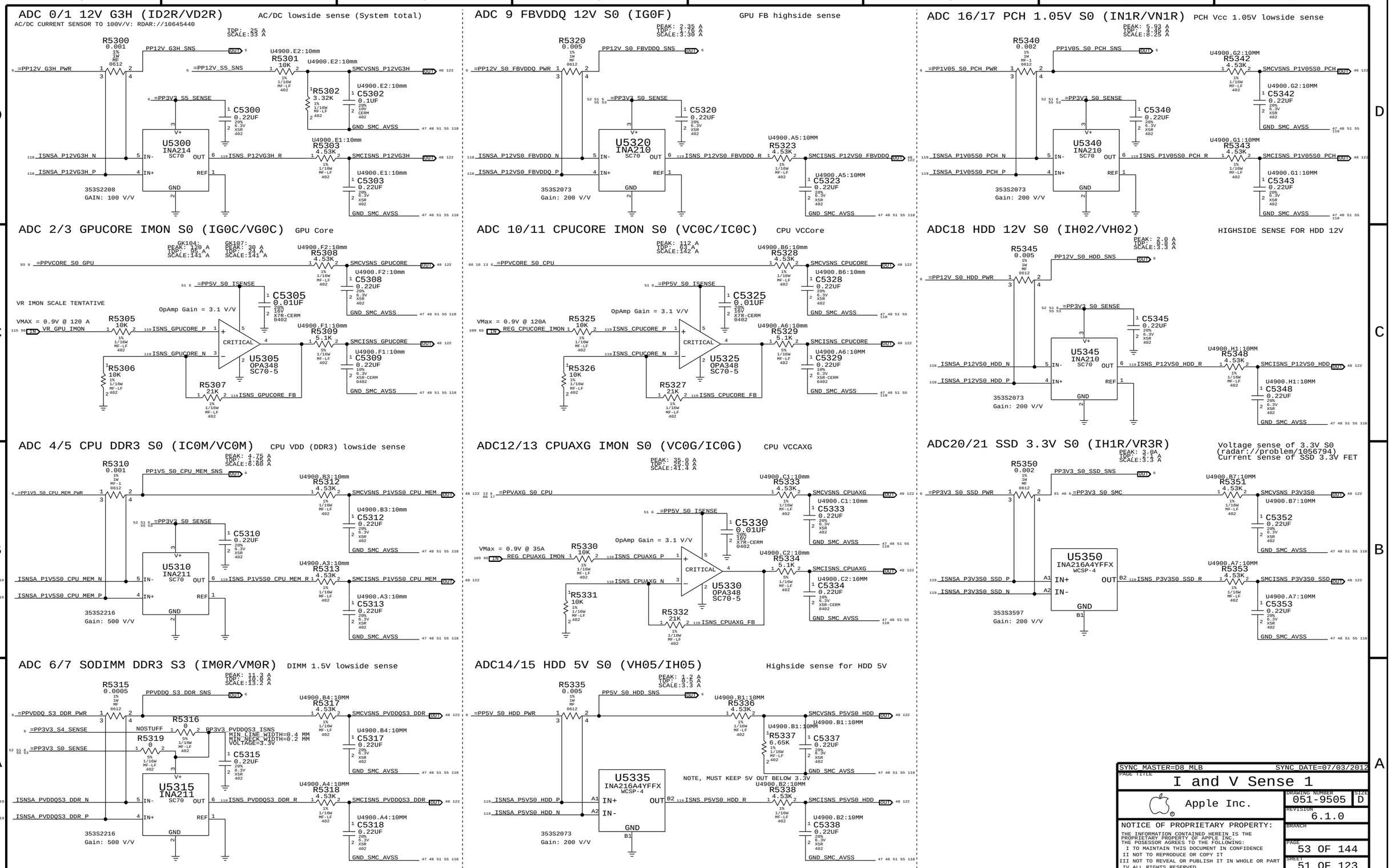
ADC 0/1 12V G3H (ID2R/VD2R)
AC/DC lowside sense (System total)
AC/DC CURRENT SENSOR TO 100V/V: RDAR://10645440
ADC 9 FBVDDQ 12V S0 (IG0F)
GPU FB highside sense
ADC 16/17 PCH 1.05V S0 (IN1R/VN1R)
PCH Vcc 1.05V lowside sense
ADC 2/3 GPUCORE IMON S0 (IG0C/VG0C)
GPU Core
VR IMON SCALE TENTATIVE
OpAmp Gain = 3.1 V/V
ADC 10/11 CPUCORE IMON S0 (VC0C/IC0C)
CPU VCCore
ADC18 HDD 12V S0 (IH02/VH02)
HIGHSIDE SENSE FOR HDD 12V
ADC 4/5 CPU DDR3 S0 (IC0M/VC0M)
CPU VDD (DDR3) lowside sense
ADC12/13 CPUAXG IMON S0 (VC0G/IC0G)
CPU VCCAXG
ADC20/21 SSD 3.3V S0 (IH1R/VR3R)
Voltage sense of 3.3V S0
(radar://problem/1056794)
Current sense of SSD 3.3V FET
ADC 6/7 SODIMM DDR3 S3 (IM0R/VM0R)
DIMM 1.5V lowside sense
ADC14/15 HDD 5V S0 (VH05/IH05)
Highside sense for HDD 5V
NOTE, MUST KEEP 5V OUT BELOW 3.3V
SYNC_MASTER=D8_MLB
SYNC_DATE=07/03/2012
PAGE TITLE
I and V Sense 1
Apple Inc.
DRAWING NUMBER
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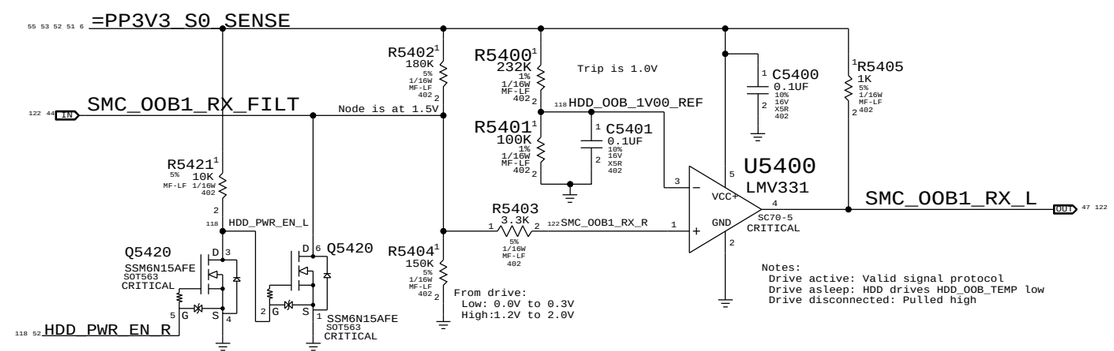
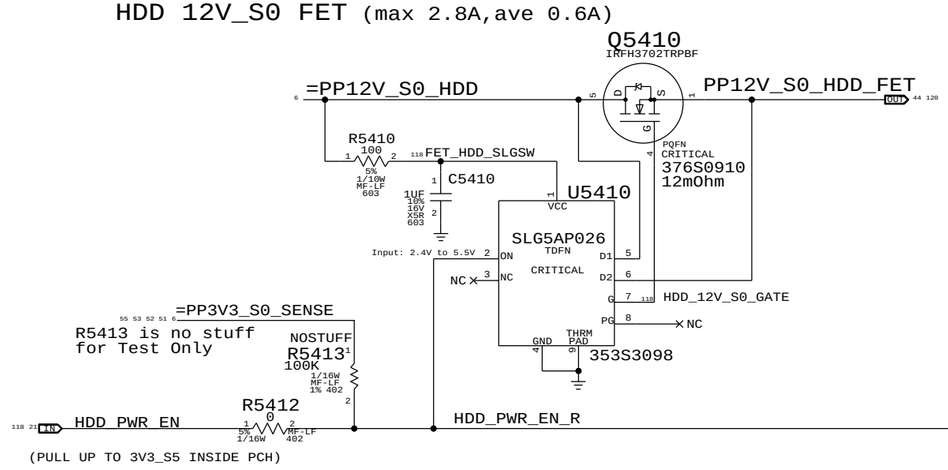
## HDD Out-of-Band Temp Sensing

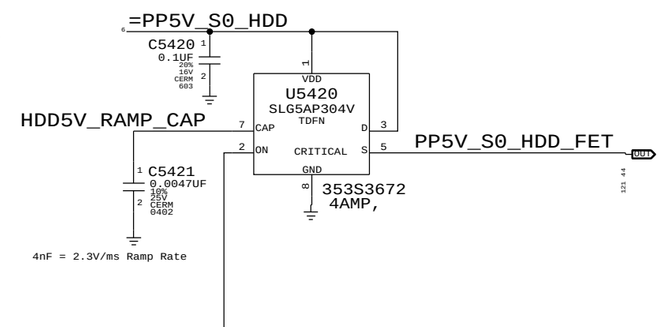
Temperature read from SATA power connecter pin 11




## HDD 12V_S0 FET (max 2.8A,ave 0.6A)




## HDD 5V_S0 FET (max 0.7A,ave 0.3A)




REMOVE R5413 AND SHORT R5412 AFTER HDD_PWR_EN WORKS

SYNC-MASTER=D8-MLB- - - - - - - - - - - - - - - - SYNC-DATE=07/03/2012

| | |
|---|---|
| PAGE TITLE | HDD/SSD Temp Sense |
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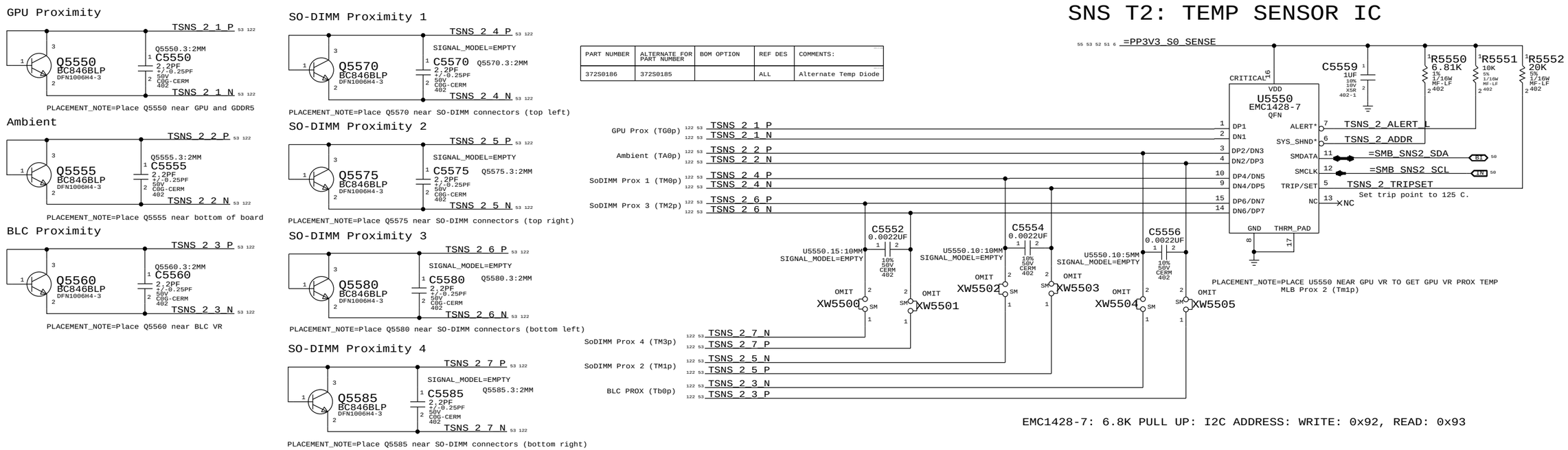
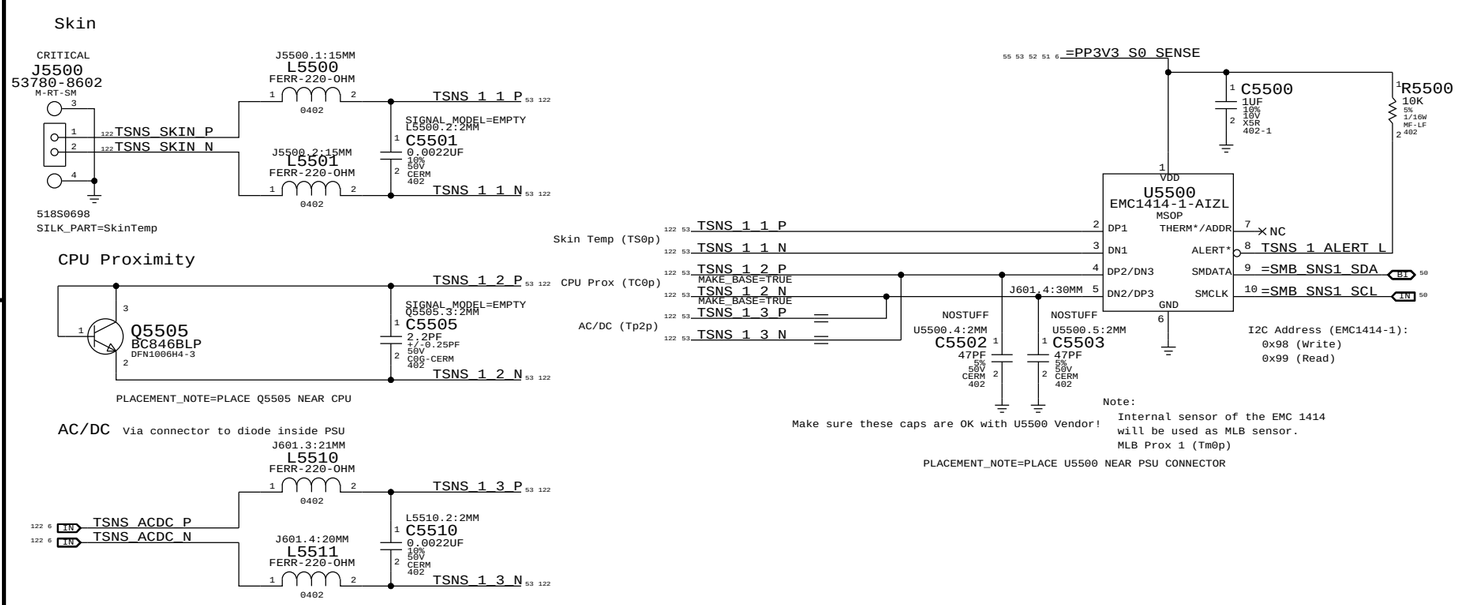
# Temperature Sensor T2 EMC1428: Near GPU VR



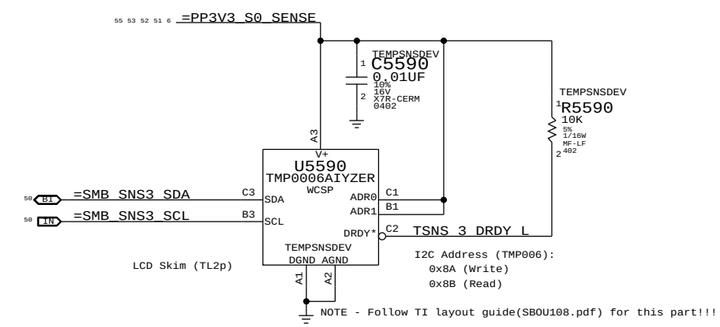

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 372S0186 | 372S0185 | | ALL | Alternate Temp Diode |

EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

# Temperature Sensor T1 EMC1414: Near PSU Conn




# Temperature Sensor T3: LCD Remote Sensor(Dev4Now)

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PAGE TITLE
# Temperature Sensors

Apple Inc.

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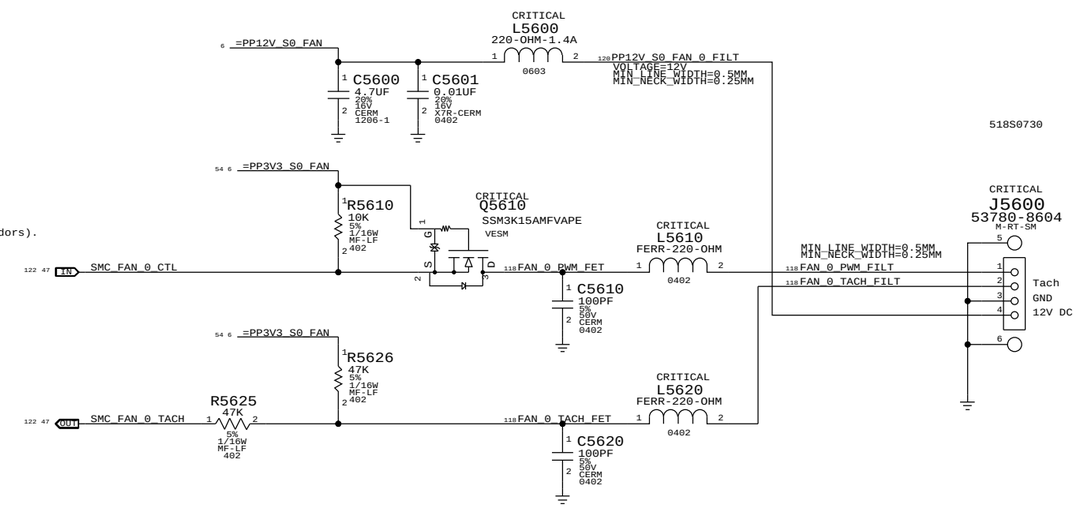
# SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q5610 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).




# SMC Fan 1 (Unused)

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PAGE TITLE
System Fan

Apple Inc.

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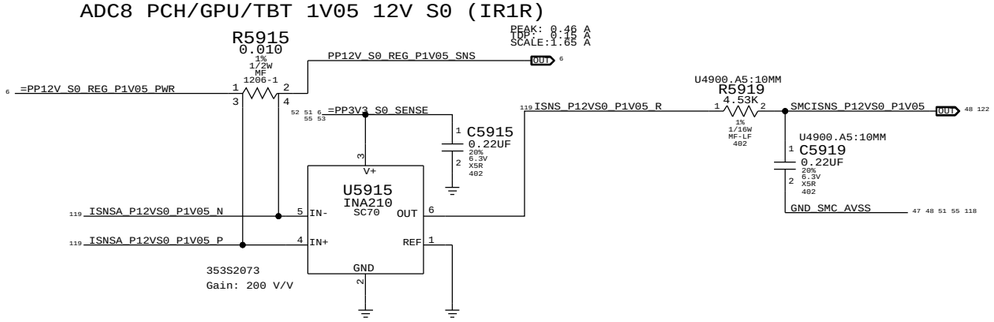
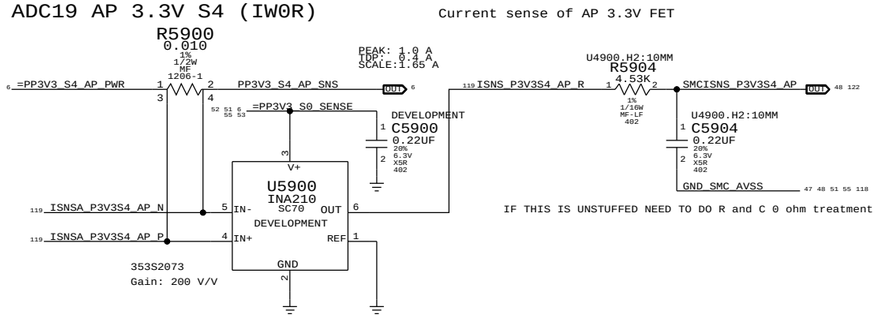
## ADC8 PCH/GPU/TBT 1V05 12V S0 (IR1R)



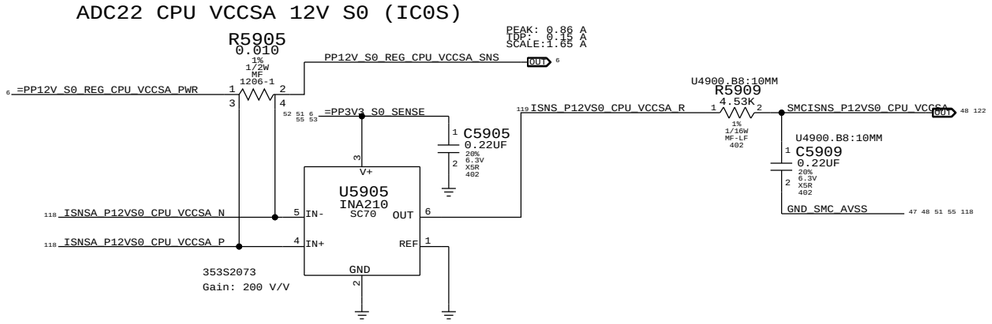

## ADC19 AP 3.3V S4 (IW0R)

Current sense of AP 3.3V FET

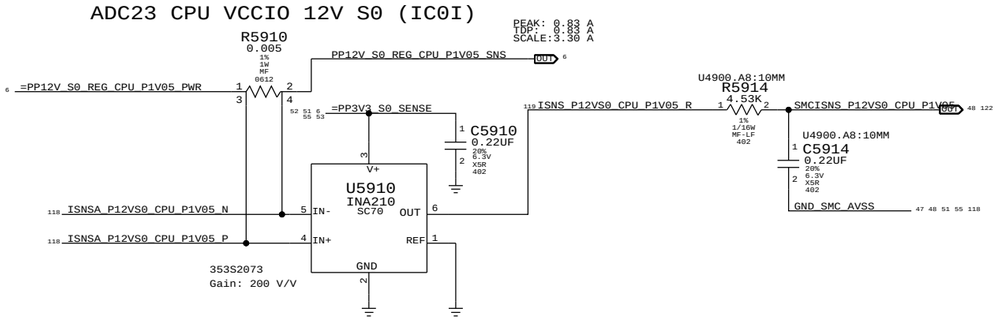



IF THIS IS UNSTUFFED NEED TO DO R and C 0 ohm treatment

## ADC22 CPU VCCSA 12V S0 (IC0S)




## ADC23 CPU VCCIO 12V S0 (IC0I)

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# I and V Sense 2

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# AUDIO CODEC

APPLE P/N 353S2592

PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5 S0 AUD DIG

C6101 4.7UF 20% 4V X5R-1 402

C6100 0.47UF 10% 10V X5R 0402

C6108 10UF 20% 16V POLY-TANT CASE-B2-SM

C6109 2.2UF 20% 6.3V CERM 402-LF

C6110 2.2UF 20% 6.3V CERM 402-LF

C6102 0.47UF 10% 10V X5R 0402

C6103 10UF 20% 16V POLY-TANT CASE-B2-SM

C6105 1UF 10% 10V X5R 402-1

C6104 0.47UF 10% 10V X5R 0402

C6106 0.47UF 10% 10V X5R 0402

CRITICAL C6107 10UF 20% 10V X5R-CERM 0402-1

PP5V AUDIO HPAMP (IN) 56 57 121

=PP3V3 S0 AUDIO (IN) 5 42 56 58 59 62

PP4V5 AUDIO ANALOG (IN) 56 60 62 121

63 62 60 56 GND AUDIO CODEC

121 62 60 56 (IN) PP4V5 AUDIO ANALOG

R6100 2.67K 1% 1/16W MF-LF 402

VBIAS_DAC

CS4206 FP

CS4206 FN

CRITICAL U6101 CS4206B QFN

VD VA_REF VA_HP VA

29 VBIAS_DAC

44 VHP_FILT+

41 VHP_FILT-

2 GPIO0/DMIC_SDA1

12 GPIO1/DMIC_SDA2 /SPDIF_OUT2

14 GPIO2

15 GPIO3

13 SENSE_A

45 FLYP

43 FLYC

42 FLYN

3 VL_HD

1 VL_IF

6 BITCLK

10 SYNC

8 SDI

5 SDO

11 RESET*

47 SPDIF_IN

48 SPDIF_OUT

DGND THRM PAD AGND

HPOUT_L 38 — MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM — TP_AUD_HP_L NC

HPOUT_R 40 — MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM — TP_AUD_HP_R NC

HPREF 39 — MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM — CS4206_HPREF

GND AUDIO CODEC (56 60 62 63) — R6105 0 5% 1/16W MF-LF 402

LINEOUT_L1+ 35 — AUD_LO1_L_P (OUT 57 58 63)

LINEOUT_L1- 34 — AUD_LO1_L_N (OUT 57 58 63)

LINEOUT_R1+ 36 — AUD_LO1_R_P (OUT 57 59 63)

LINEOUT_R1- 37 — AUD_LO1_R_N (OUT 57 59 63)

LINEOUT_L2+ 31 — AUD_LO2_L_P (OUT 58 63)

LINEOUT_L2- 30 — AUD_LO2_L_N (OUT 58 63)

LINEOUT_R2+ 32 — AUD_LO2_R_P (OUT 59 63)

LINEOUT_R2- 33 — AUD_LO2_R_N (OUT 59 63)

HP AMP/LINE OUT — RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT

TWEETERS

WOOFERS

MICBIAS 16 — AUD_CODEC_MICBIAS (OUT 56 58)

VCOM 28 — CS4206_VCOM — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

LINEIN_L+ 21 — NO_TEST=TRUE — NC_AUD_LI_P_L NC

LINEIN_C- 22 — NO_TEST=TRUE — NC_AUD_LI_COM NC

LINEIN_R+ 23 — NO_TEST=TRUE — NC_AUD_LI_P_R NC

MICIN_L+ 18 — AUD_MIC_INL_P (IN 60 63)

MICIN_L- 17 — AUD_MIC_INL_N (IN 60 63)

MICIN_R+ 19 — NO_TEST=TRUE — NC_AUD_MIC_INP_R NC

MICIN_R- 20 — NO_TEST=TRUE — NC_AUD_MIC_INN_R NC

VREF+_ADC 27 — CS4206_VREF_ADC NC — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

DMIC_SCL 4 — CS4206_DMIC_SCL — R6104 22 5% 1/16W MF-LF 402 — AUD_DMIC_CLK (OUT 42)

DMIC_SCL — R6103 100K 1% 1/10W MF-LF 402

DMIC_SDA1 — AUD_DMIC_SDA1 (OUT 42)

NC TP_AUD_GPIO_1

HP AMP CNTRL — AUD_GPIO_2 (OUT 57)

MAC SPKR AMP CNTRL — AUD_CODEC_MICBIAS (IN 58 56)

D6100 SOD-523 BAT54XV2T1

WIN SPKR AMP CNTRL — AUD_GPIO_3 (OUT 58) — AUD_SENSE_A (IN 63 62)

C6111 2.2UF 20% 6.3V CERM 402-LF

C6112 2.2UF 20% 6.3V CERM 402-LF

CS4206 FLYP

CS4206 FLYC

CS4206 FLYN

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK (IN 105 18)

HDA_SYNC (IN 105 18 15)

HDA_SDIN0 (OUT 105 18) — R6101 22 5% 1/16W MF-LF 402 — AUD_SDI_R (105)

HDA_SDOUT (IN 105 18)

HDA_RST_L (IN 105 18)

DP_INT_SPDIF_AUDIO (IN 111 78)

AUD_SPDIF_CHIP (105)

AUD_SPDIF_OUT (OUT 105 60) — R6102 22 5% 1/16W MF-LF 402

DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA

GND_AUDIO_DMIC (OUT 42) — MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=0V — XW6100 SM

GND AUDIO CODEC (63 62 60 56)

CRITICAL C6113 1UF 10% 20V TANT CASE-P3-HF

CRITICAL C6114 10UF 20% 16V POLY-TANT CASE-B2-SM

C6115 0.47UF 10% 10V X5R 0402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

Q6170 P S — DEVEL_AUDIO CRITICAL Q6170 DMC2400UV SOT563 — DEVEL_AUDIO R6170 0 5% 1/16W MF-LF 402 — Q6170 P G

P-CHN

NC

NC

DEVEL_AUDIO CRITICAL Q6170 DMC2400UV SOT563 — Q6170 N G — DEVEL_AUDIO R6171 0 5% 1/16W MF-LF 402 — Q6170 N S

Q6171 P S — DEVEL_AUDIO CRITICAL Q6171 DMC2400UV SOT563 — DEVEL_AUDIO R6172 0 5% 1/16W MF-LF 402 — Q6171 P G

P-CHN

NC

NC

DEVEL_AUDIO CRITICAL Q6171 DMC2400UV SOT563 — Q6171 N G — DEVEL_AUDIO R6173 0 5% 1/16W MF-LF 402 — Q6171 N S

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 127S0134 | 127S0111 | | C6113 | THAILAND ALTERNATE |

# APPLE P/N 353S2456
# 4.5V POWER SUPPLY FOR CODEC

L6111 FERR-220-OHM 0402 — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=5V — PP5V_AUDIO_HPAMP (OUT 56 57 121)

L6110 FERR-220-OHM 0402 — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=5V

63 6 (IN) =PP5V_S0_AUDIO

59 58 56 42 62 6 (IN) =PP3V3_S0_AUDIO — R6120 0 5% 1/16W MF-LF 402

VR6101 TPS71745 SON CRITICAL

IN OUT NR/FB EN GND NC

4V5_REG_IN

4V5_REG_EN (117)

4V5_NR

C6122 1UF 10% 10V X5R 402-1

C6123 0.1UF 10% 16V X7R-CERM 0402

XW6110 SM

PP4V5_AUDIO_ANALOG (OUT 56 60 62 121) — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.15MM VOLTAGE=4.5V

MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

C6124 1UF 10% 10V X5R 402-1

GND_AUDIO_CODEC (56 60 62 63) — MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

XW6111 SM

GND_AUDIO_HPAMP (57) — MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

SYNC_MASTER=D8_MLB — SYNC_DATE=07/03/2012

PAGE TITLE: AUDIO: CODEC/REGULATORS

Apple Inc.

DRAWING NUMBER: 051-9505 — SIZE: D

REVISION: 6.1.0

BRANCH:

PAGE: 61 OF 144

SHEET: 56 OF 123

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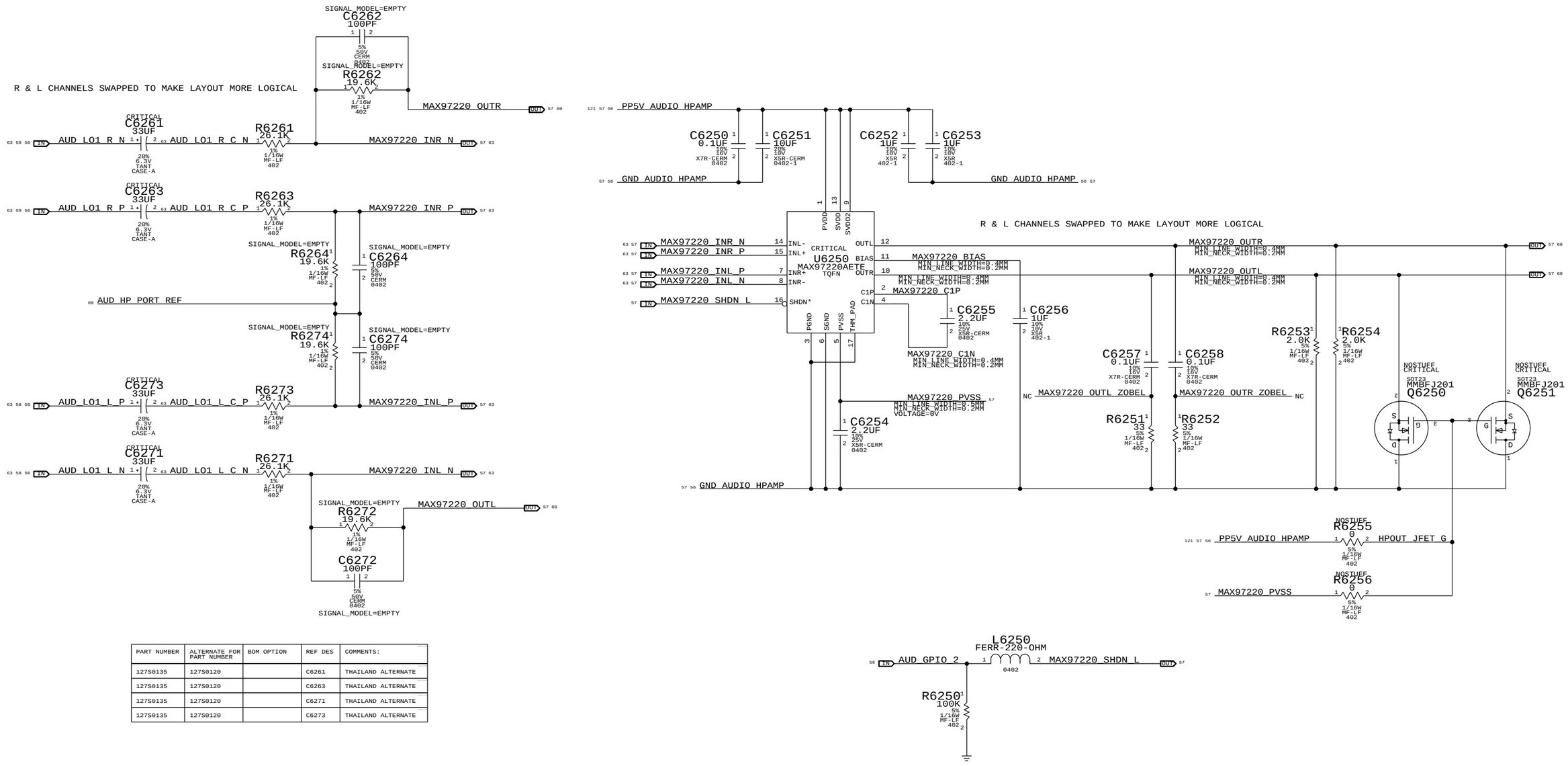


| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|---|---|---|---|---|
| 127S0135 | 127S0120 | | C6261 | THAILAND ALTERNATE |
| 127S0135 | 127S0120 | | C6263 | THAILAND ALTERNATE |
| 127S0135 | 127S0120 | | C6271 | THAILAND ALTERNATE |
| 127S0135 | 127S0120 | | C6273 | THAILAND ALTERNATE |

SYNC MASTER=D8_MLB SYNC DATE=07/03/2012

PAGE TITLE
# AUDIO: HEADPHONE AMP

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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PAGE 62 OF 144

SHEET 57 OF 123

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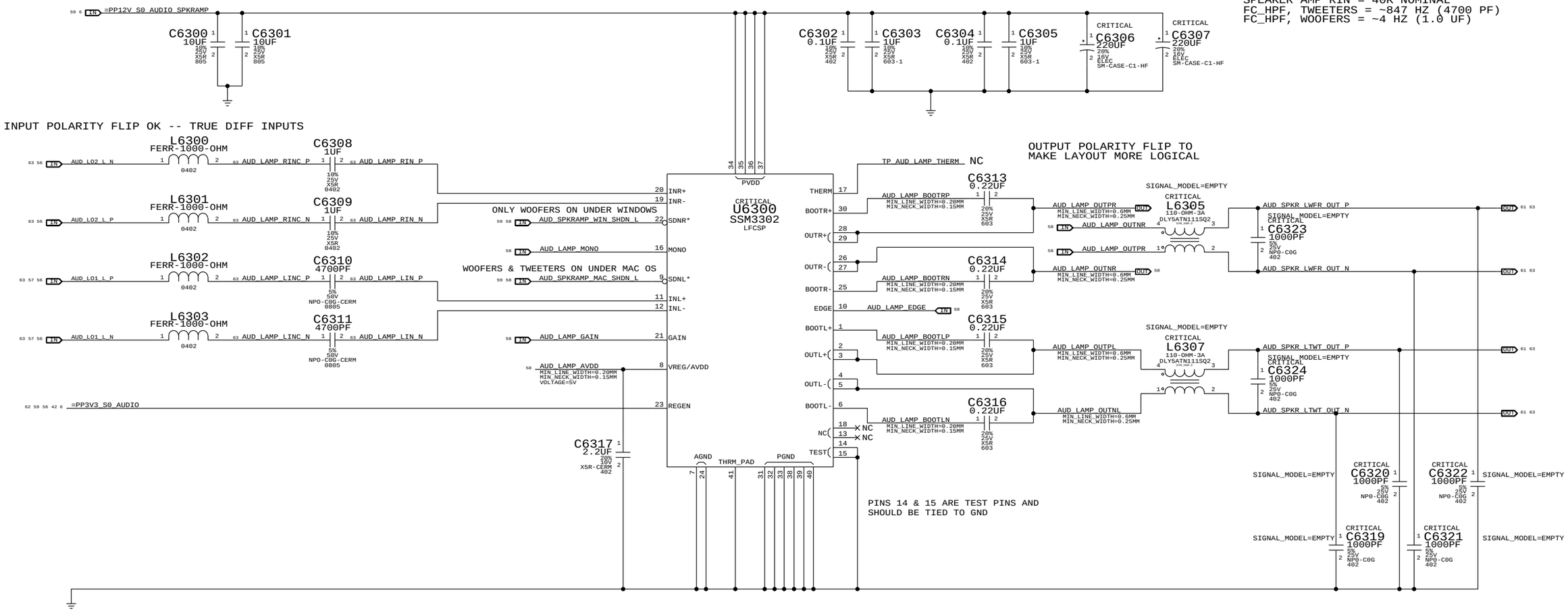
# LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

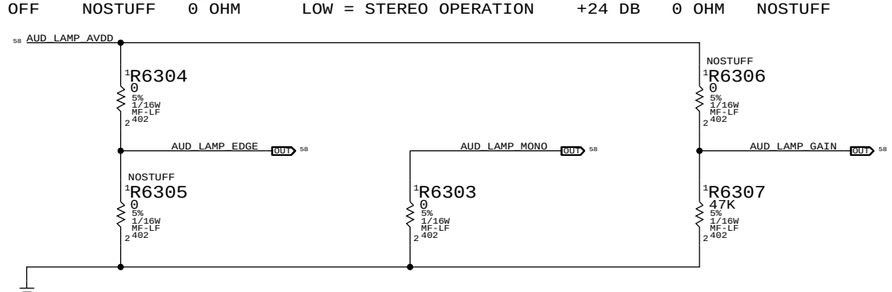



EDGE RATE CONTROL

| | R6304 | R6305 |
|---|---|---|
| ON | 0 OHM | NOSTUFF |
| OFF | NOSTUFF | 0 OHM |

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

| GAIN | R6306 | R6307 |
|---|---|---|
| +9 DB | NOSTUFF | 0 OHM |
| +12 DB | NOSTUFF | 47 KOHM |
| +15 DB | NOSTUFF | NOSTUFF |
| +18 DB | 47 KOHM | NOSTUFF |
| +24 DB | 0 OHM | NOSTUFF |




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
AUDIO: LEFT SPKR AMP

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D
REVISION 6.1.0
BRANCH
PAGE 63 OF 144
SHEET 58 OF 123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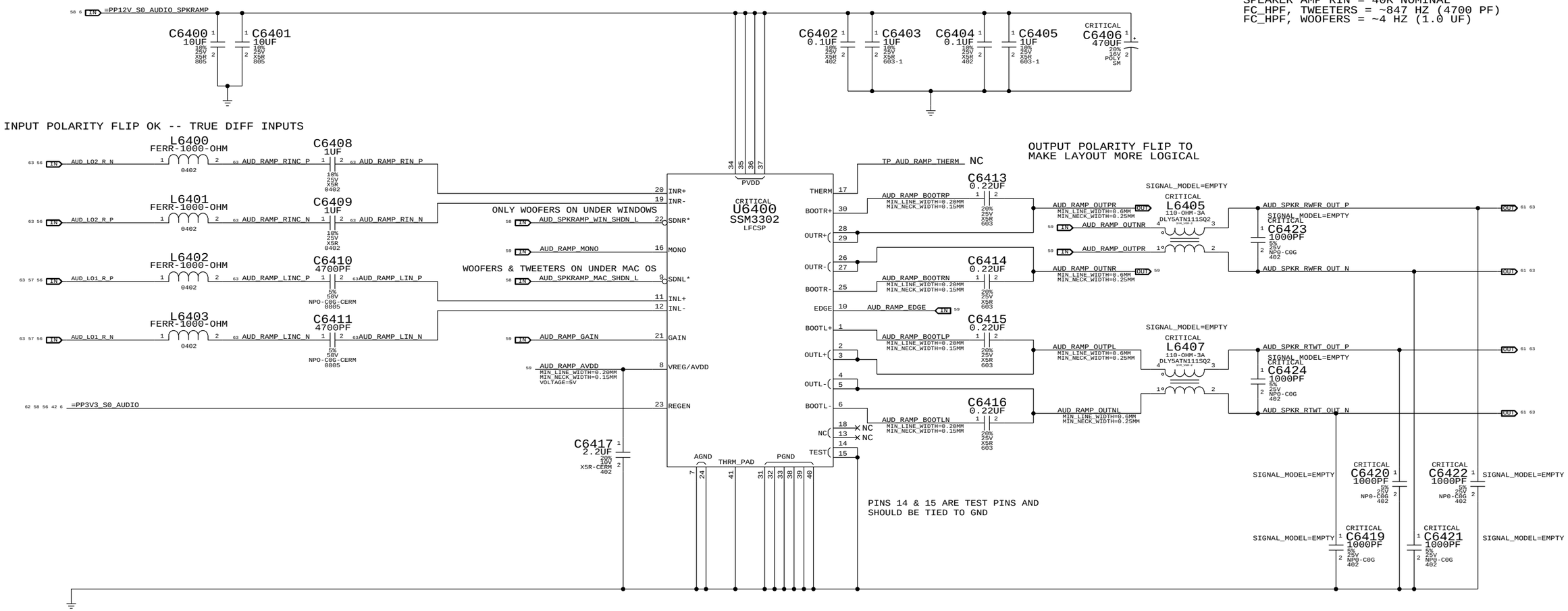
# RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

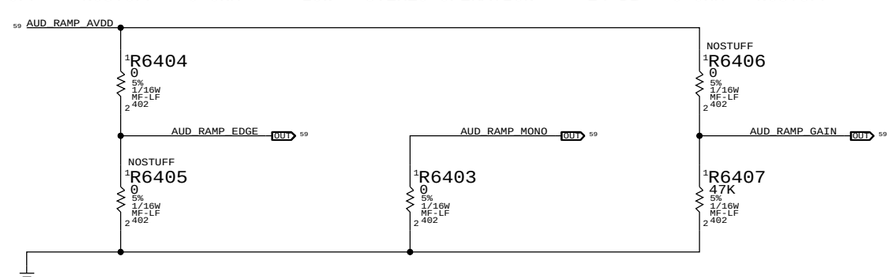



EDGE RATE CONTROL

| | R6404 | R6405 |
|---|---|---|
| ON | 0 OHM | NOSTUFF |
| OFF | NOSTUFF | 0 OHM |

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

| GAIN | R6406 | R6407 |
|---|---|---|
| +9 DB | NOSTUFF | 0 OHM |
| +12 DB | NOSTUFF | 47 KOHM |
| +15 DB | NOSTUFF | NOSTUFF |
| +18 DB | 47 KOHM | NOSTUFF |
| +24 DB | 0 OHM | NOSTUFF |




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
AUDIO: RIGHT SPKR AMP

Apple Inc.

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REVISION 6.1.0
BRANCH
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SHEET 59 OF 123

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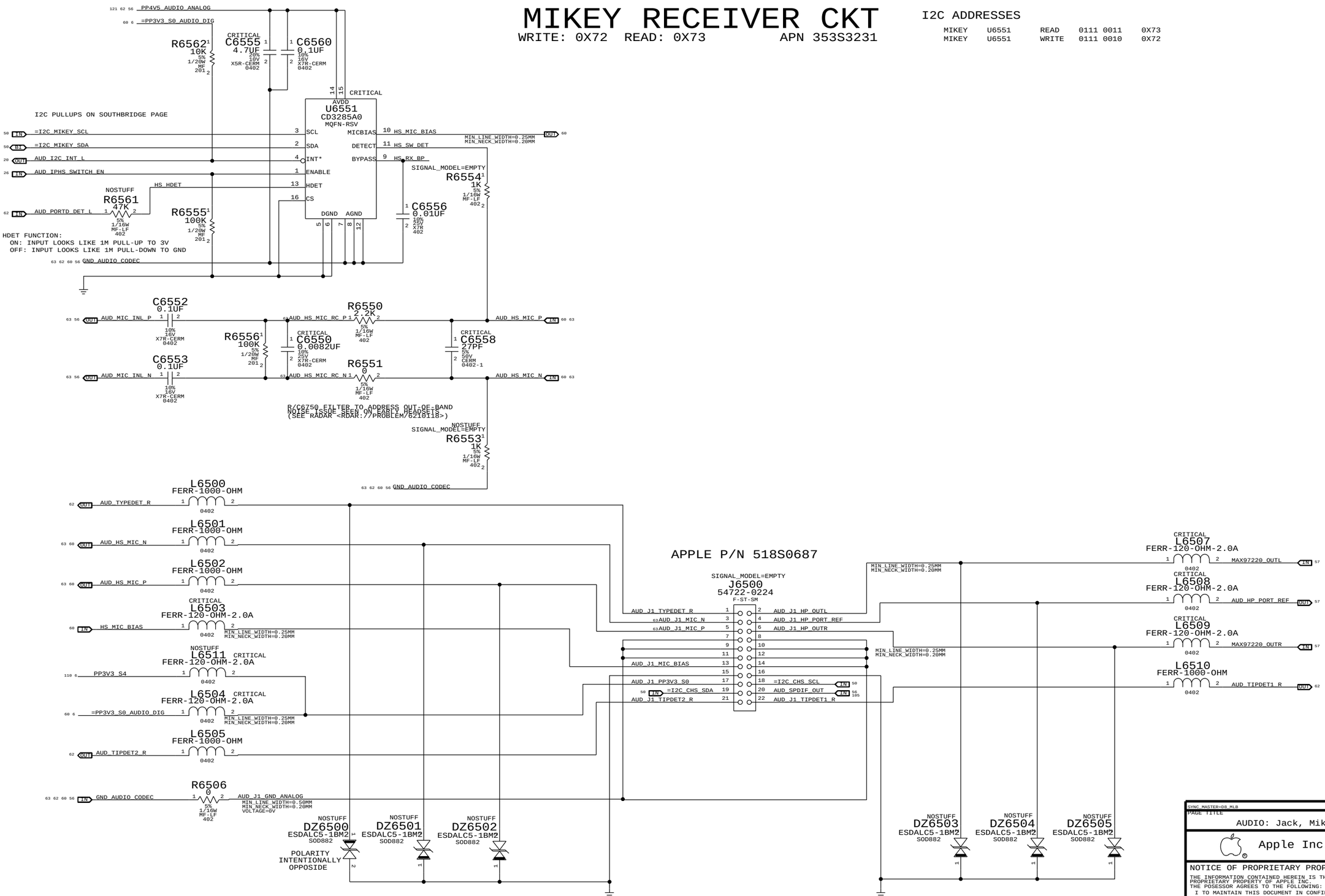
# MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

| | | | | |
|---|---|---|---|---|
| MIKEY | U6551 | READ | 0111 0011 | 0X73 |
| MIKEY | U6551 | WRITE | 0111 0010 | 0X72 |




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2013

PAGE TITLE: AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

REVISION: 6.1.0

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PAGE: 65 OF 144

SHEET: 60 OF 123

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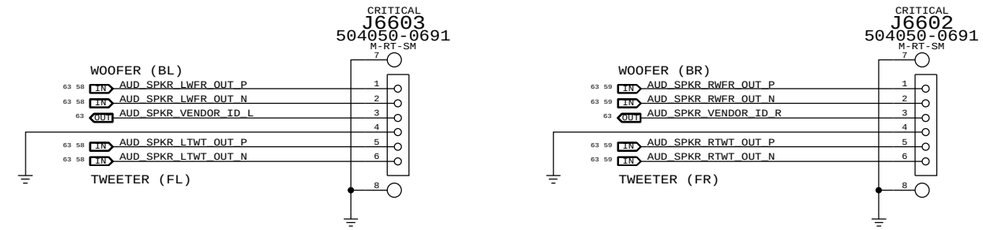
# SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
Audio: Spkr/Mic Conn.

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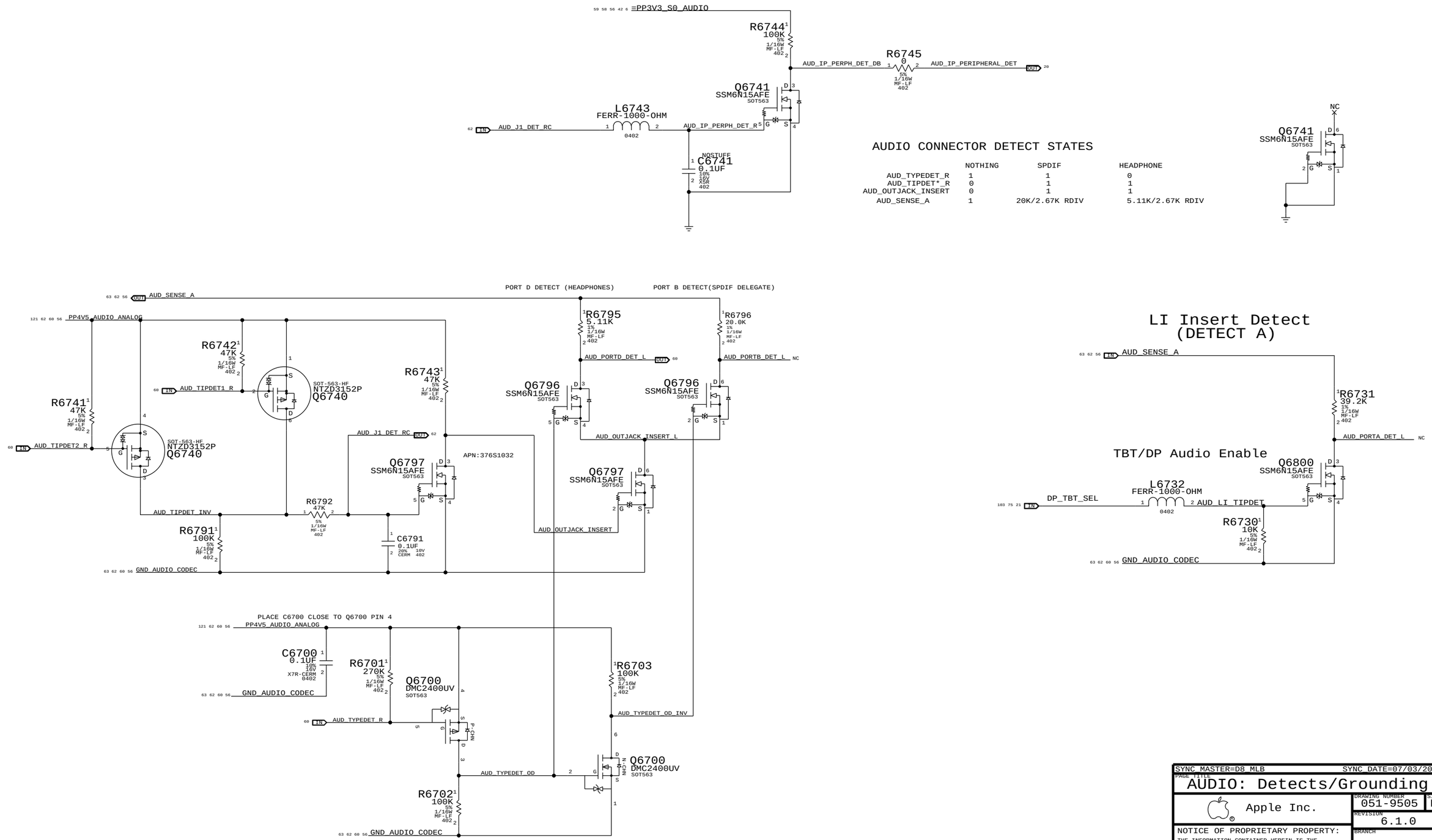
# IPHS HS Detect Debounce CKT




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
AUDIO: Detects/Grounding

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## CODEC OUTPUT SIGNAL PATHS

| FUNCTION | VOLUME/MUTE | CONVERTER | PIN COMPLEX | MAC SHDN | WIN SHDN | DET ASSIGNMENT |
|---|---|---|---|---|---|---|
| HP/LINE OUT | 0X03 (3) | 0X03 (3) | 0X0A (10,D) | GPIO_2 | GPIO_2 | 0X0A (DET D) |
| PRIMARY SPKRS (WFR) | 0X04 (4) | 0X04 (4) | 0X0B (11) | MICBIAS | GPIO_3 | N/A |
| SECONDARY SPKRS (TWT) | 0X03 (3) | 0X03 (3) | 0X0A (10,V24) | MICBIAS | N/A | N/A |
| SPDIF OUT | N/A | 0X08 (8) | 0x10 (16) | N/A | N/A | 0X0D (DET B) |

## CODEC INPUT SIGNAL PATHS

| FUNCTION | CONVERTER | PIN COMPLEX | ENABLE/CONTROL | DET ASSIGNMENT |
|---|---|---|---|---|
| SPDIF IN | 0X07 (7) | 0x0F (15) | N/A | 0X09 (DET A) |
| INTERNAL MIC ARRAY | 0X06 (6)<br>0X05 (5) | 0X0E (14,LEFT & RIGHT)<br>0X12 (18,LEFT) | N/A | N/A |
| EXTERNAL MIC | 0X06 (6) | 0X0D (13,V22,B,LEFT) | PANTHER POINT GPIO 16 | PANTHER POINT GPIO 5 (BCVR INT)<br>PANTHER POINT GPIO 3 (PERIPH DET) |

## OTHER DETECT

| FUNCTION | CONVERTER | PIN COMPLEX | ENABLE/CONTROL | DET ASSIGNMENT |
|---|---|---|---|---|
| MULTIPLE SPKR VENDORS | N/A | N/A | N/A | 0X0C (DET C) |

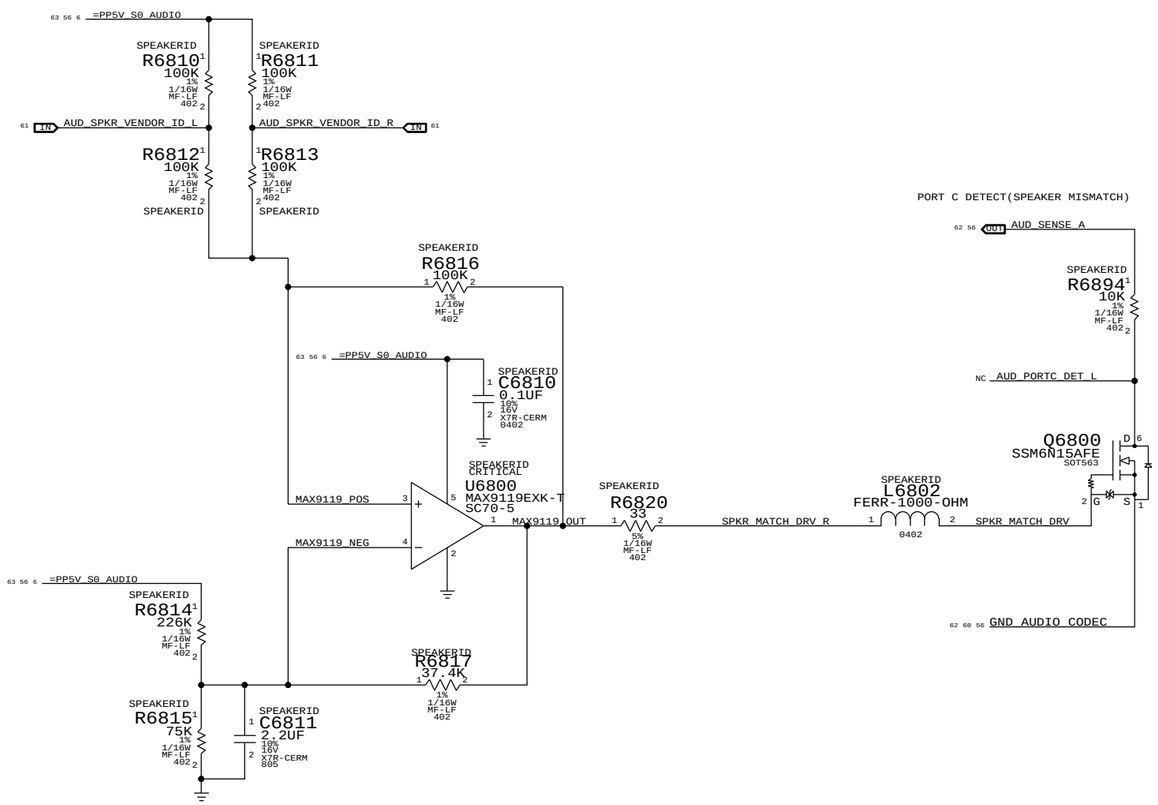
| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| AUDIO | * | 0.1 MM | ? |
| SPKROUT | * | 0.2 MM | ? |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| AUDIODIFF | * | AUDIODIFF |
| SPKROUTDIFF | * | SPKROUTDIFF |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| AUDIODIFF | * | Y | 0.1 MM | 0.1 MM | 10 MM | 0.1 MM | 0.1 MM |
| SPKROUTDIFF | * | Y | 0.6 MM | 0.25 MM | 10 MM | 0.2 MM | 0.2 MM |

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE: PHYSICAL | NET_TYPE: SPACING | | |
|---|---|---|---|---|
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_P | 56 57 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_N | 56 57 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_C_P | 57 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_L_C_N | 57 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_P | 56 57 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_N | 56 57 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_C_P | 57 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO1_R_C_N | 57 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_L_P | 56 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_L_N | 56 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_R_P | 56 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LO2_R_N | 56 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LINC_P | 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LINC_N | 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RINC_P | 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RINC_N | 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LIN_P | 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_LIN_N | 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RIN_P | 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_RAMP_RIN_N | 59 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LINC_P | 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LINC_N | 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RINC_P | 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RINC_N | 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LIN_P | 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_LIN_N | 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RIN_P | 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_LAMP_RIN_N | 58 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX97220_INL_P | 57 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX97220_INL_N | 57 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX97220_INR_P | 57 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | MAX97220_INR_N | 57 |
| SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RWFR_OUT_P | 59 61 |
| SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RWFR_OUT_N | 59 61 |
| SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RTWT_OUT_P | 59 61 |
| SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_RTWT_OUT_N | 59 61 |
| SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LWFR_OUT_P | 58 61 |
| SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LWFR_OUT_N | 58 61 |
| SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LTWT_OUT_P | 58 61 |
| SPKROUT_DIFFPAIR | SPKROUTDIFF | SPKROUT | AUD_SPKR_LTWT_OUT_N | 58 61 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC_INL_P | 56 60 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_MIC_INL_N | 56 60 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HS_MIC_RC_P | 60 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HS_MIC_RC_N | 60 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HS_MIC_P | 60 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_HS_MIC_N | 60 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_J1_MIC_P | 60 |
| AUDIO_DIFFPAIR | AUDIODIFF | AUDIO | AUD_J1_MIC_N | 60 |

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# AUDIO: Speaker ID

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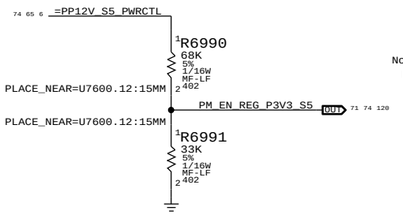
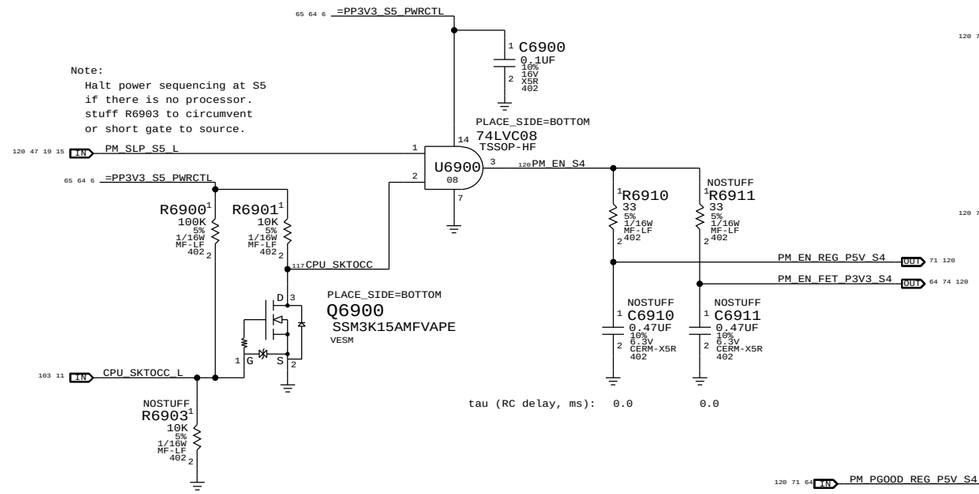
## S5 3V3 Soft Enable




Note:
Expected 3.9V +/- 0.4V EN signal

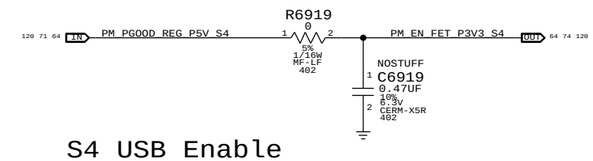
## S4 5V Enable



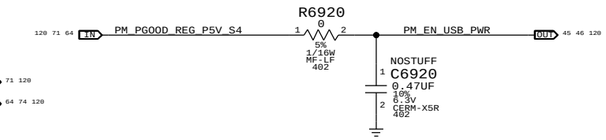

Note:
Halt power sequencing at S5
if there is no processor.
stuff R6903 to circumvent
or short gate to source.

tau (RC delay, ms): 0.0 0.0

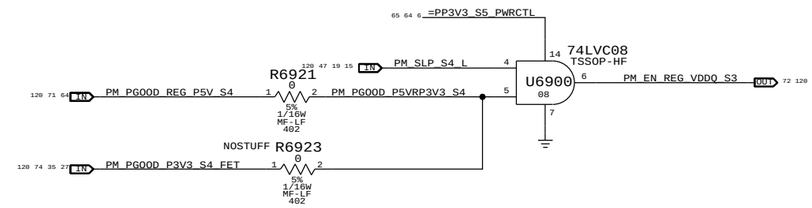
## S4 3V3 Enable



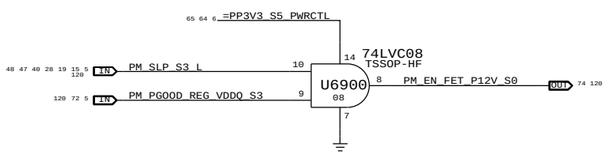

## S4 USB Enable




## S3 1V5 Reg (S0/S3) Enable

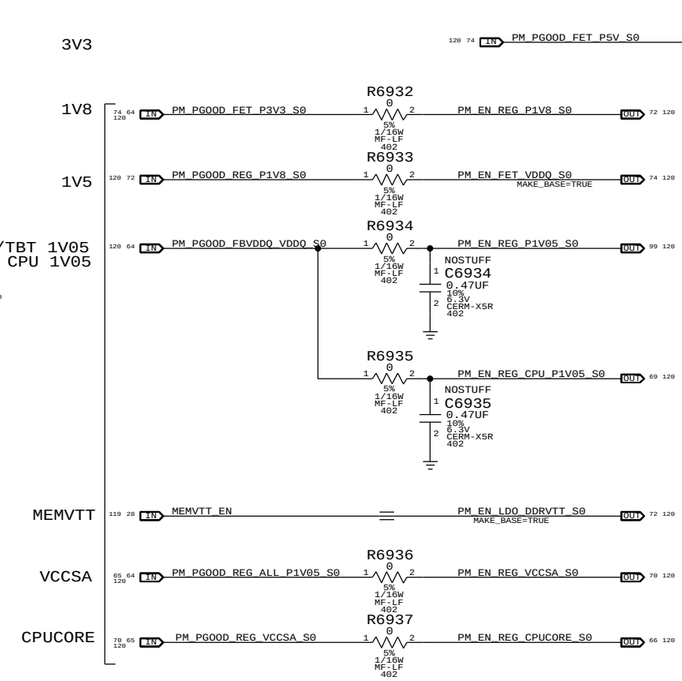



## S0 12V Enable

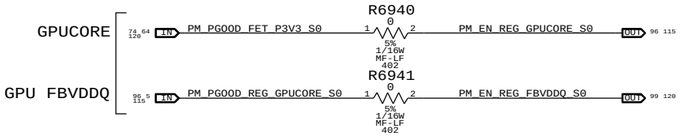



## S0 Platform Parallel Sequence Enable

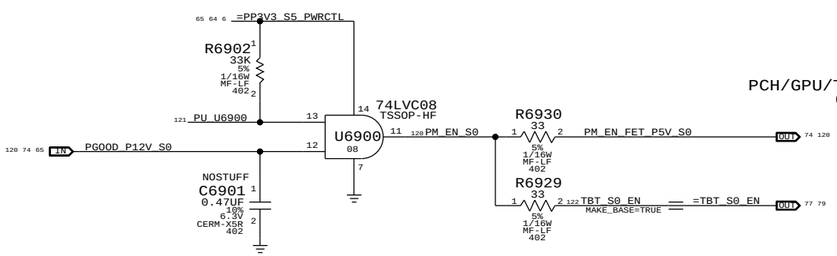
CPU/PCH Sequencing



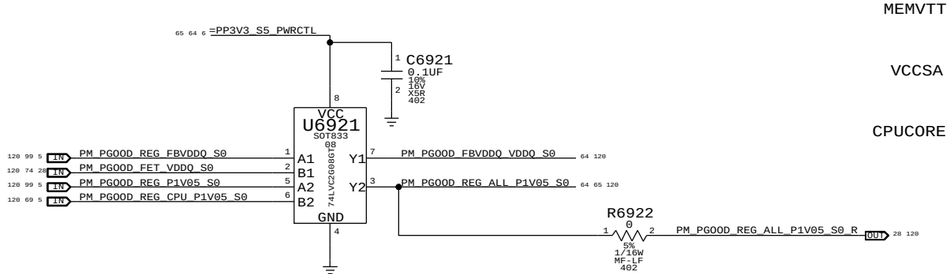

## GPU Sequencing




## S0 5V and TBT Enable




## Parallel Enable PGOOD combinator




### Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.8 V 1.5 V, PCH Core/PLL/VRM)
Uncore: VccSA, VDDQ, VccA (1.8 V), VccIO (VccSA, VccA, and VccIO must ramp within 50 ms of each other)

### Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. CPU VDDQ must ramp before MEMVTT and vice versa on power down. It has no relationship to any other rails.

NVIDIA GFX:
1. VDD33 (our 3V3_S0)
2. IFPA/B_IOVDD (1.8 V) with or after 3V3_S0 (unused in our implementation)
3. NVVDD (our GPUCORE) after IFPA/B_IOVDD
4. FBVDDQ (our GPU_VDDQ) after NVVDD
5. PEX_VDD (our GPU_1V05) after FBVDDQ
6. IFPC/D/E/F_IOVDD (1.05V) wit or after PEX_VDD
7. The ramp time for any rail must be more than 40 uS
8. All rails must be powered off within 10 ms from first rail powering off

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PAGE TITLE
# PM Regulator Enables

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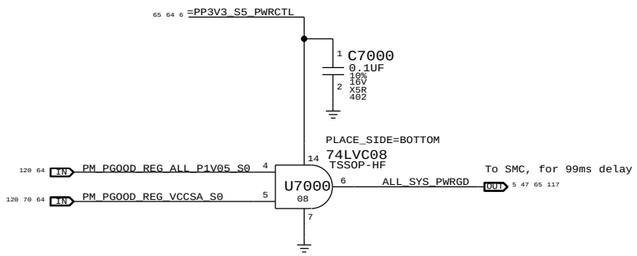
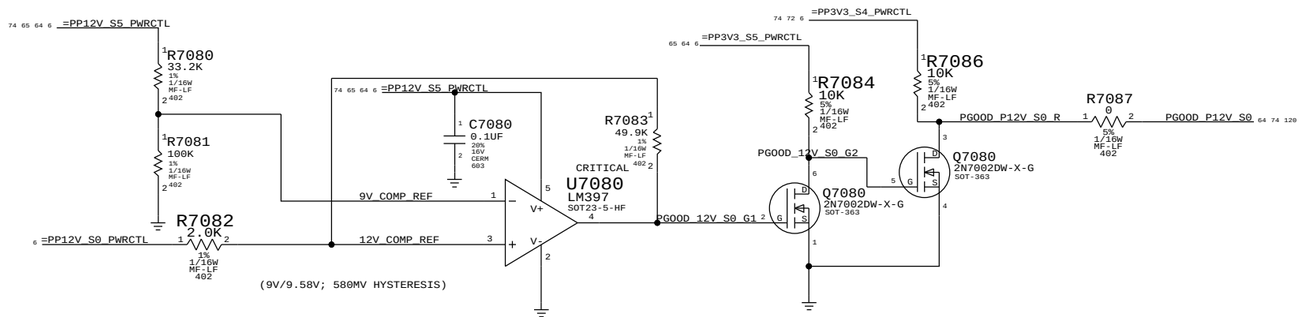
# Platform Power Good Derive SMC ALL_SYS_PWRGD

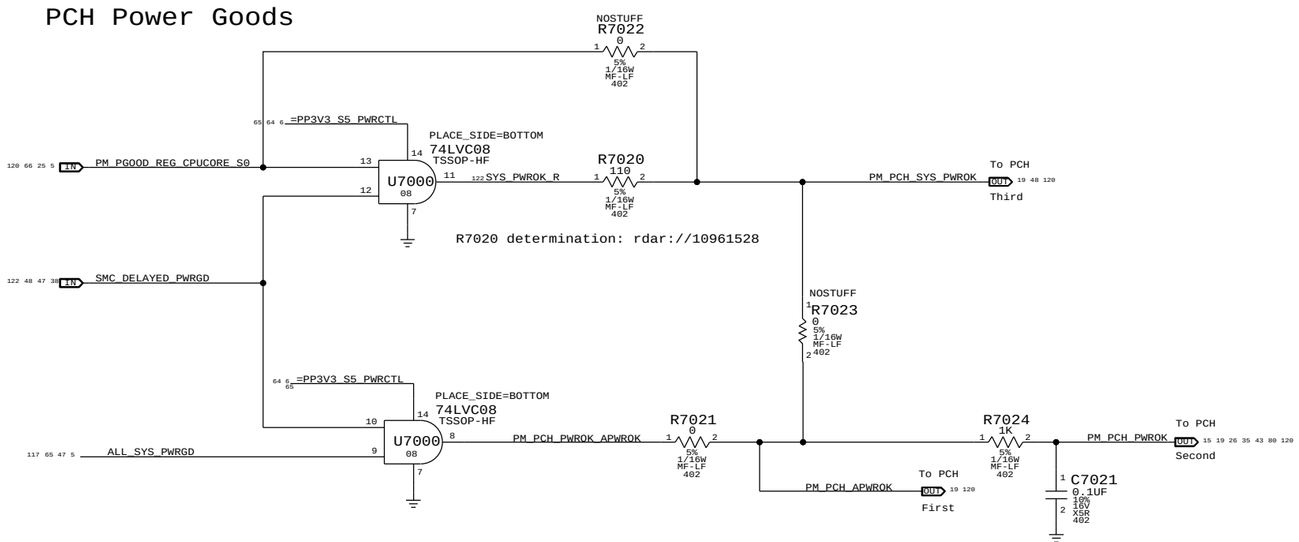
The end of the power sequence for S0 rails except CPU CORE.




## PGOOD COMPARATORS FOR PP12V_S0




## PCH Power Goods




radar://11043352 Need AND Gate to deassert PM_PCH_PWROK to PCH when unexpected power loss happens

# Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

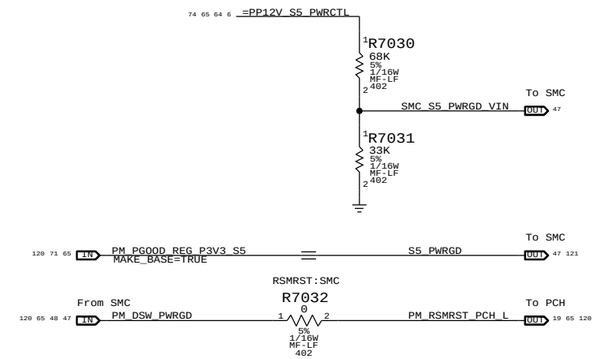
Note:
The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation.

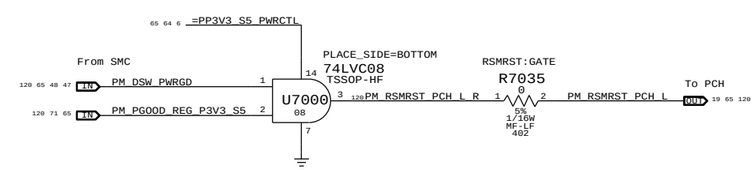
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and SMC_S5_PWRGD_VIN input is above comparator input level of 1.5 V.

SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.




Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.

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|---|---|
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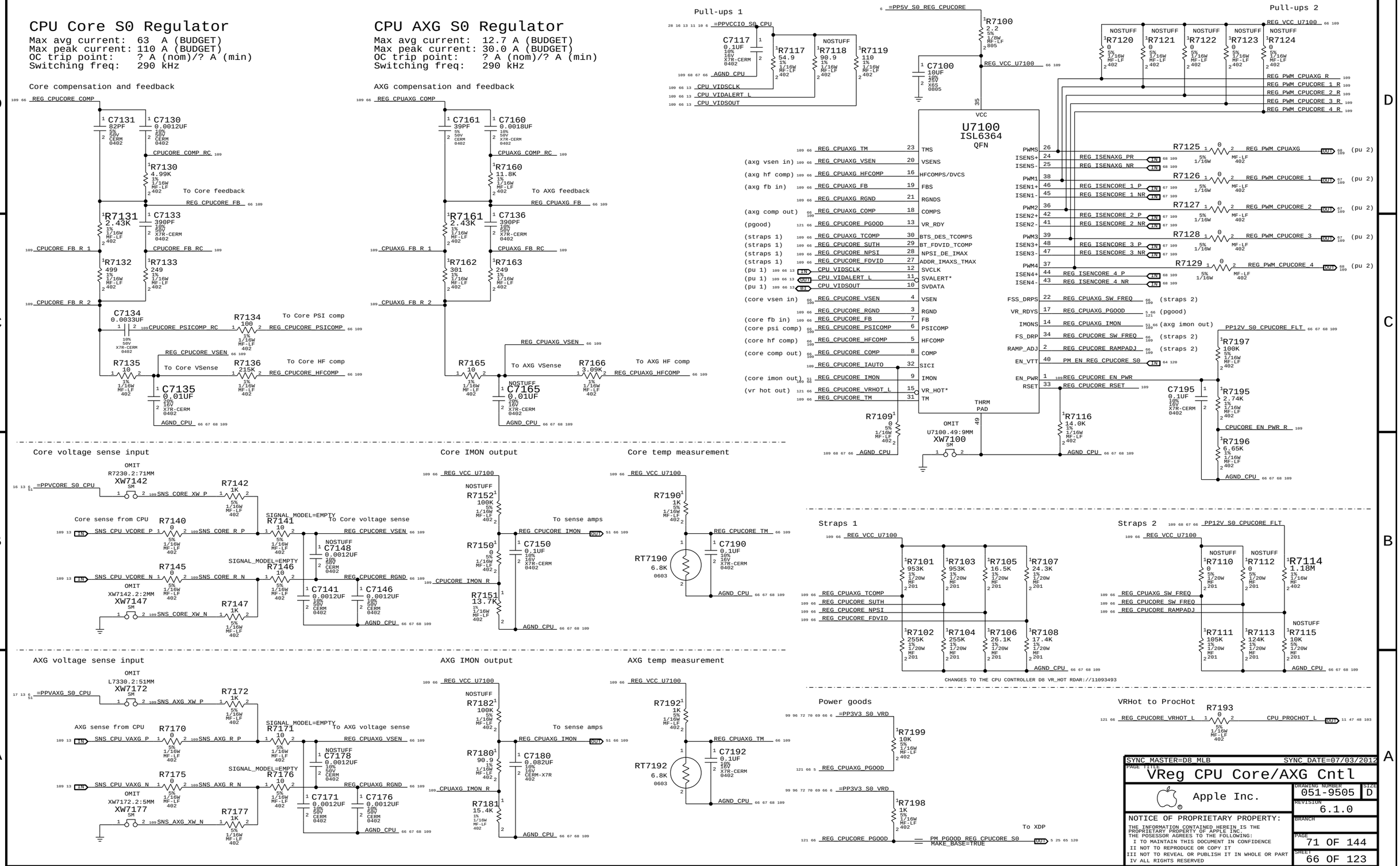
CPU Core S0 Regulator
Max avg current: 63 A (BUDGET)
Max peak current: 110 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz
CPU AXG S0 Regulator
Max avg current: 12.7 A (BUDGET)
Max peak current: 30.0 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz
Pull-ups 1
Pull-ups 2
U7100
ISL6364
QFN
Core compensation and feedback
AXG compensation and feedback
Core voltage sense input
Core IMON output
Core temp measurement
AXG voltage sense input
AXG IMON output
AXG temp measurement
Straps 1
Straps 2
Power goods
VRHot to ProcHot
CHANGES TO THE CPU CONTROLLER D8 VR_HOT RDAR://11093493
SYNC MASTER=D8_MLB
SYNC DATE=07/03/2012
PAGE TITLE
VReg CPU Core/AXG Cntl
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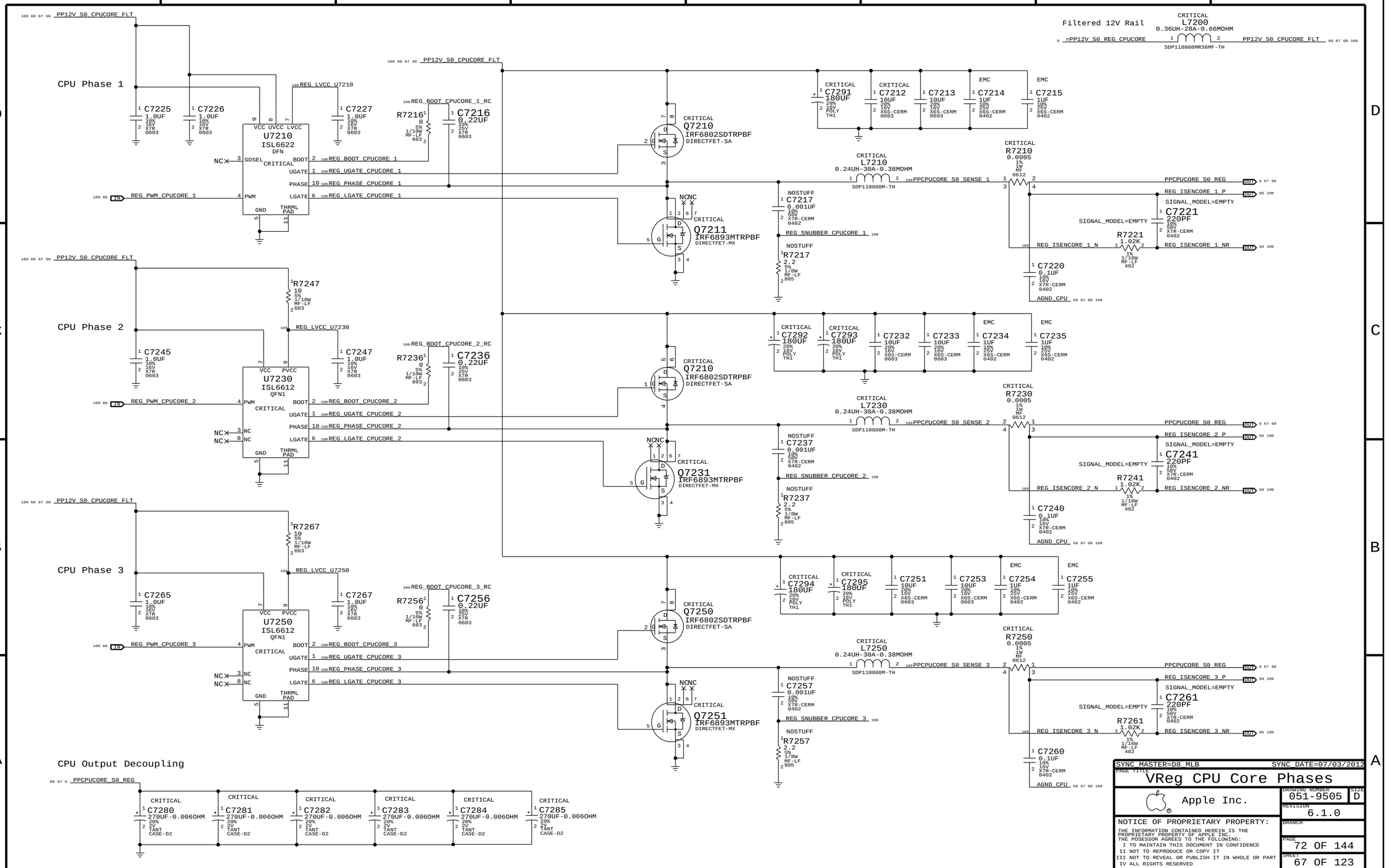


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PAGE TITLE
# VReg CPU Core Phases

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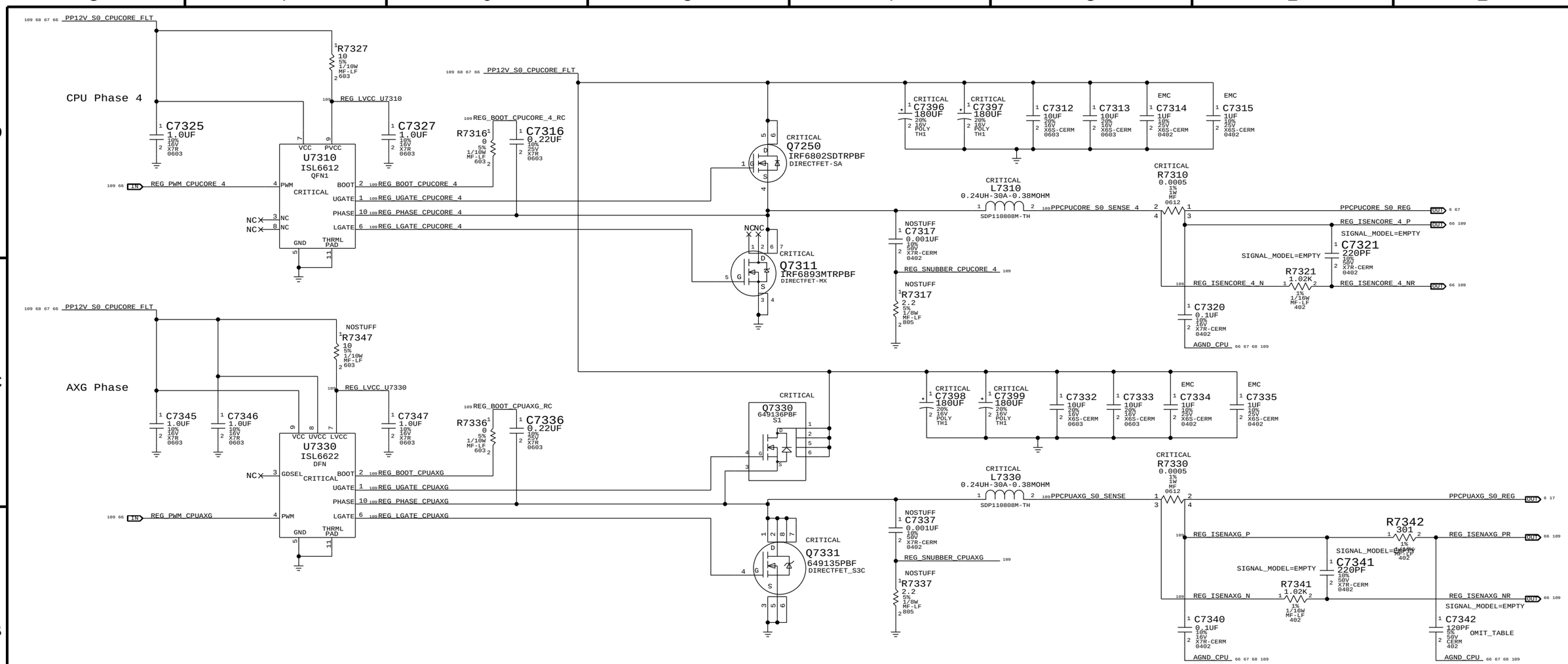


| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 131S0513 | 1 | 120PF,5%,50V,0402,SMD | C7342 | | |

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# VReg CPU AXG Phases

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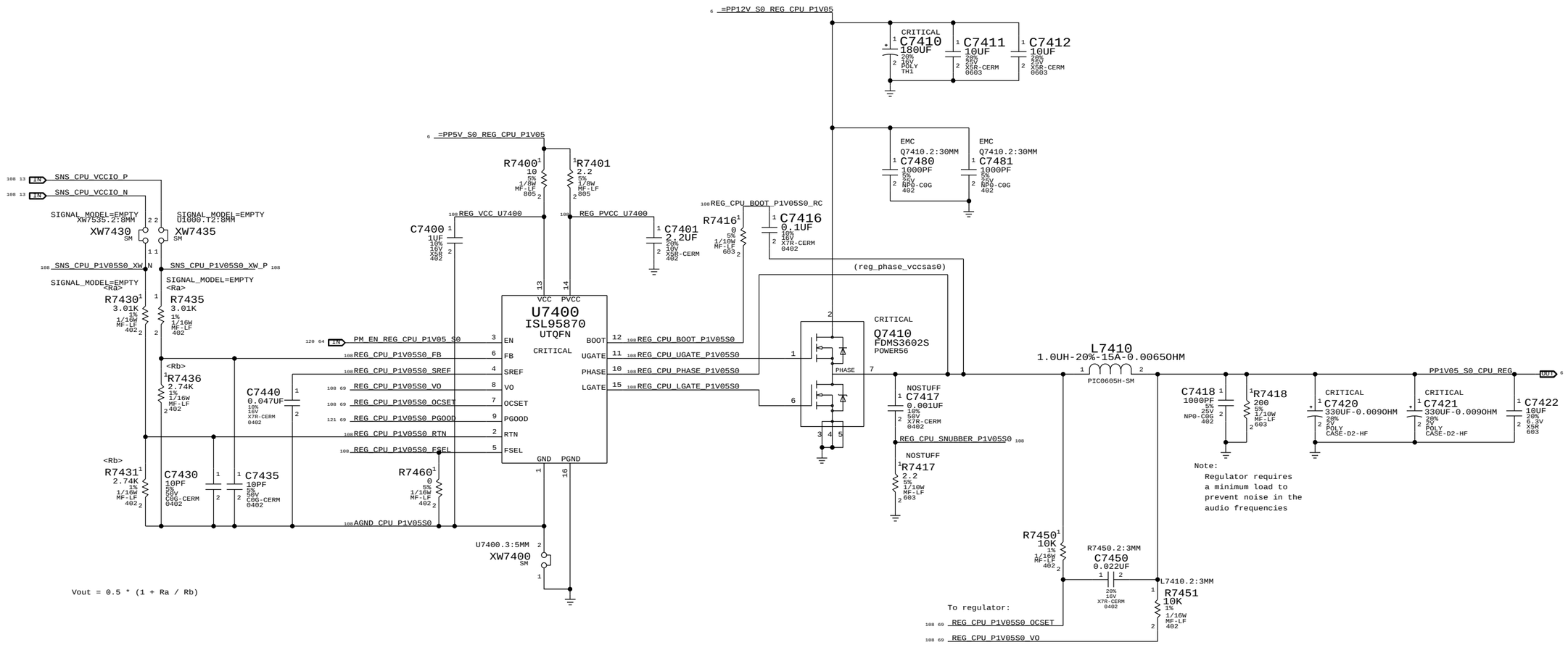
# CPU VccIO (1.05V) S0 Regulator

Max avg current: 8.10 A (BUDGET)
Max peak current: 8.50 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz

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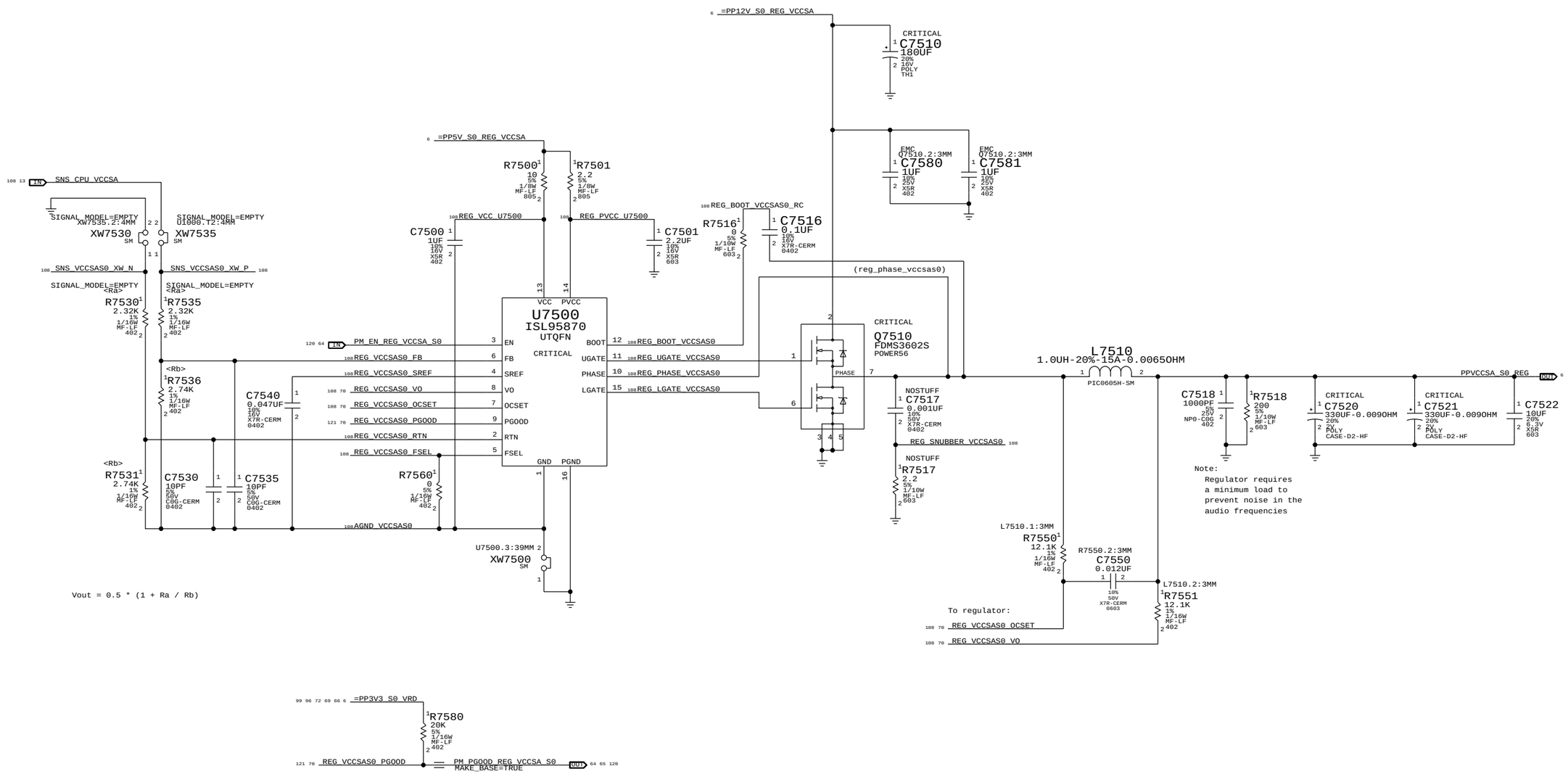
# CPU VccSA (0.925V) S0 Regulator

Max avg current: 12.07 A (BUDGET)
Max peak current: 30 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz

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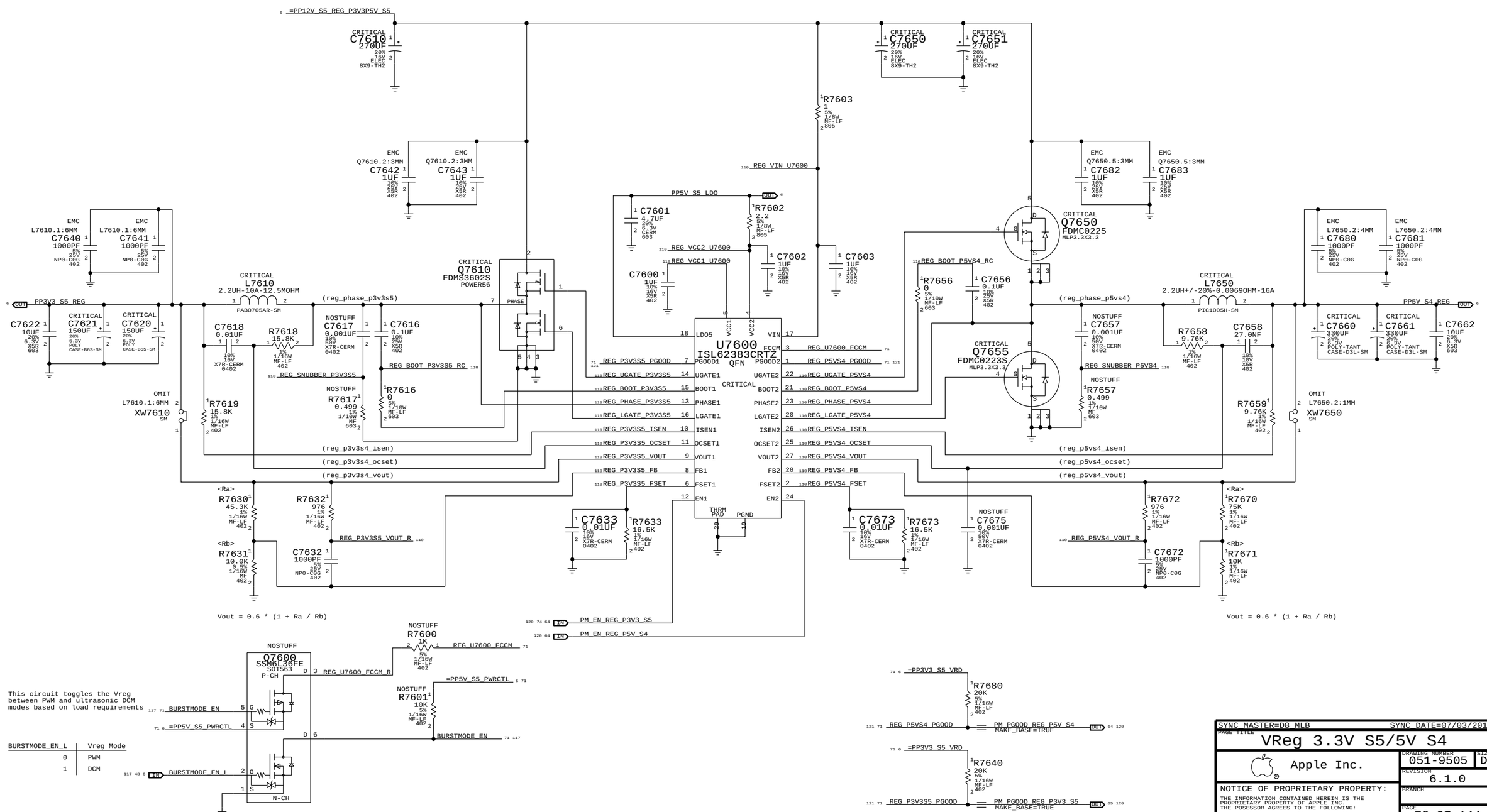
## 3.3V S5 Regulator

Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: ? A (design)/ 6.6 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

## 5V S4 Regulator

Max avg current: 10 A (design)/ 6.08 A (budget)
Max peak current: ? A (design)/ 6.9 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

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PAGE TITLE
VReg 3.3V S5/5V S4

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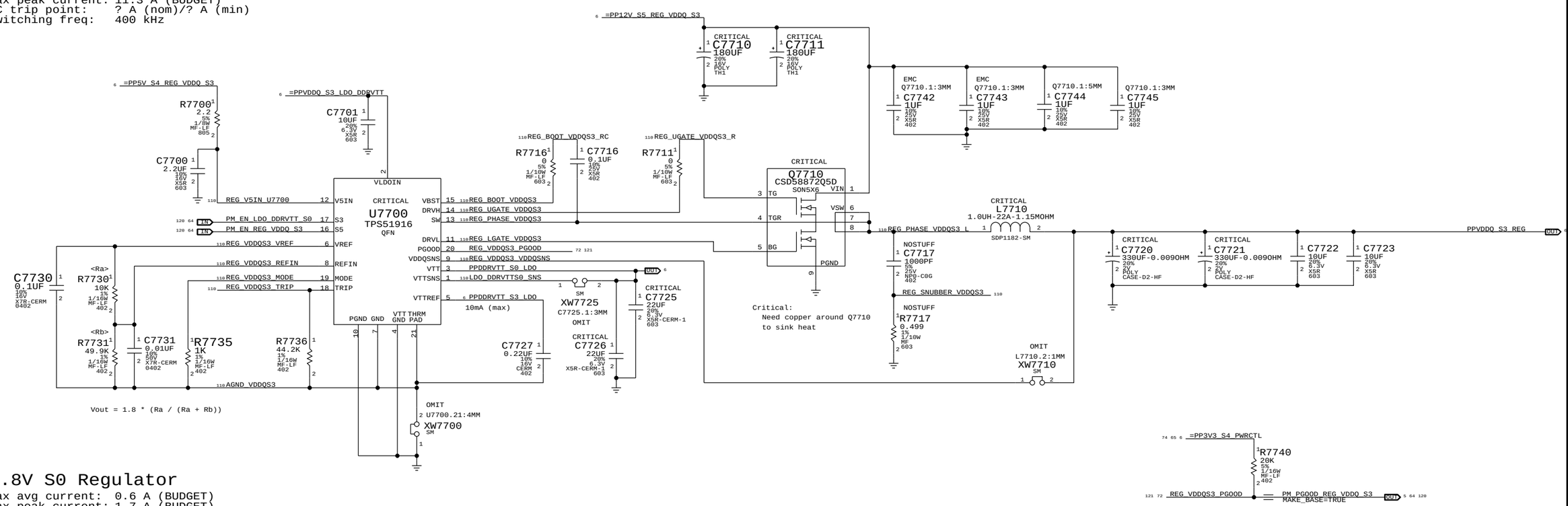
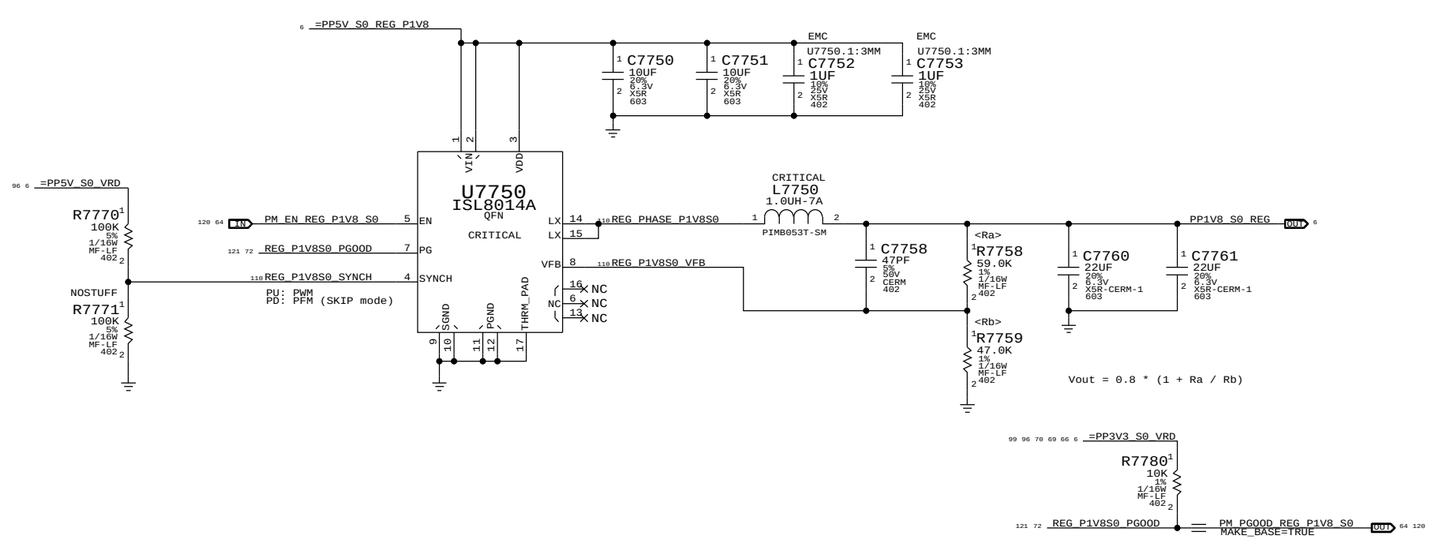
## VDDQ (1.5V) S3 Regulator

Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 400 kHz




## 1.8V S0 Regulator

Max avg current: 0.6 A (BUDGET)
Max peak current: 1.7 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz

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PAGE TITLE
# VReg VDDQ and 1.8V S0

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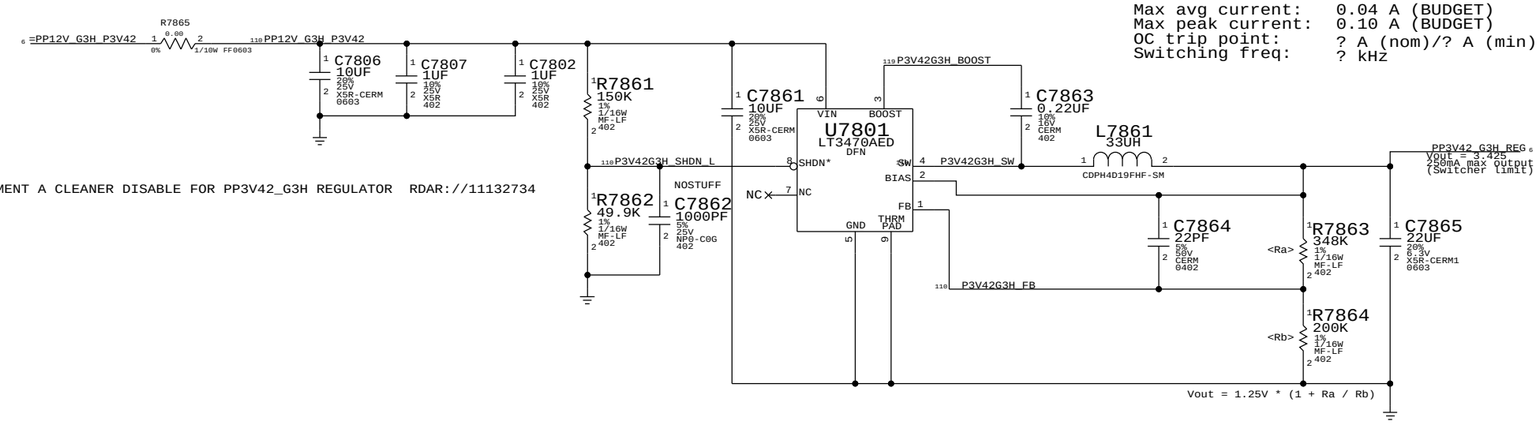
D8:CONTROLLER CHANGE FOR 3.42V SMC SUPPLY RDAR://11003901

D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42_G3H REGULATOR RDAR://11132734

## 3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz

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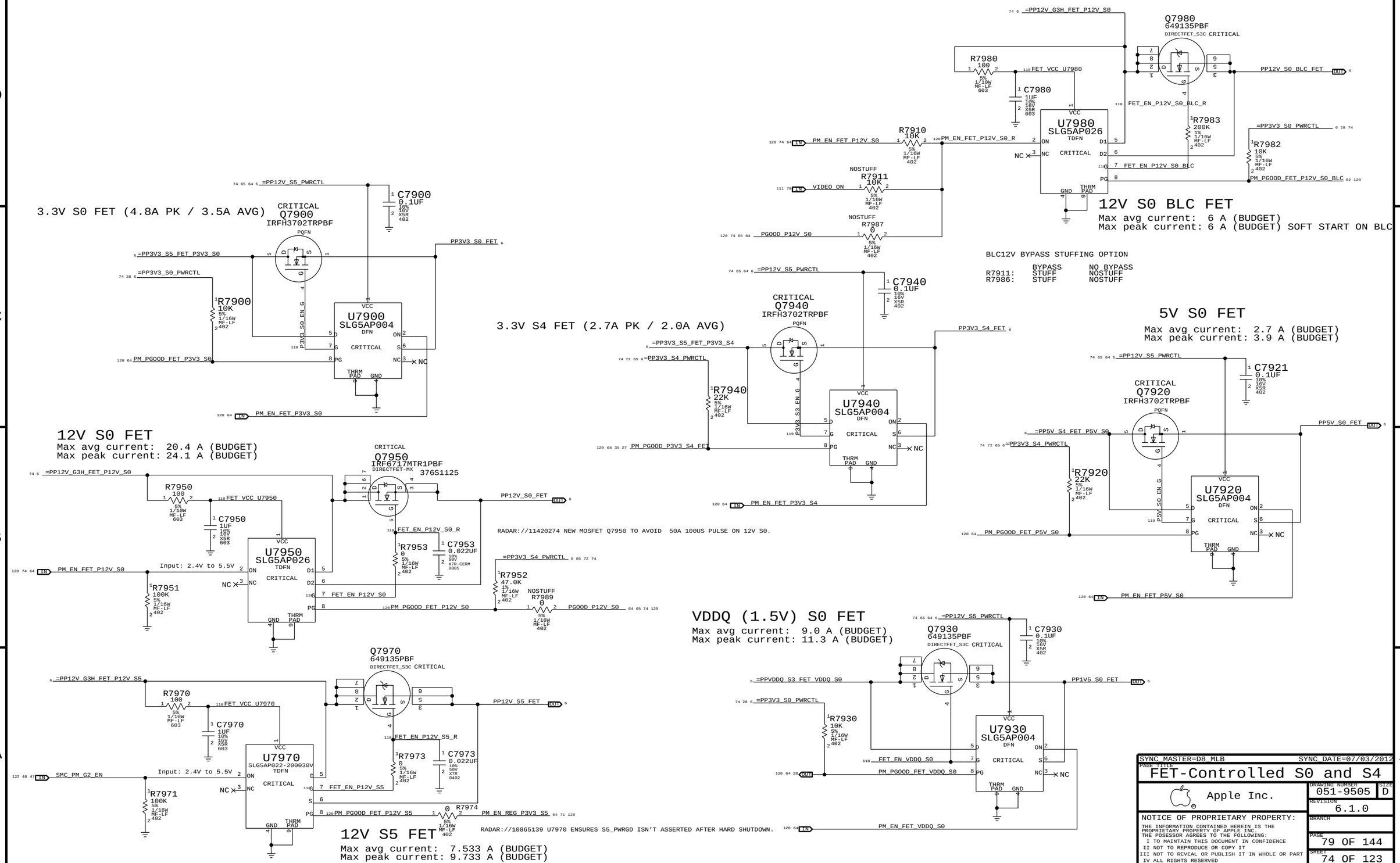
| | PAGE: 78 OF 144 |
| | SHEET: 73 OF 123 |




SYNC MASTER=D8_MLB SYNC DATE=07/03/2012

PAGE TITLE
# FET-Controlled S0 and S4

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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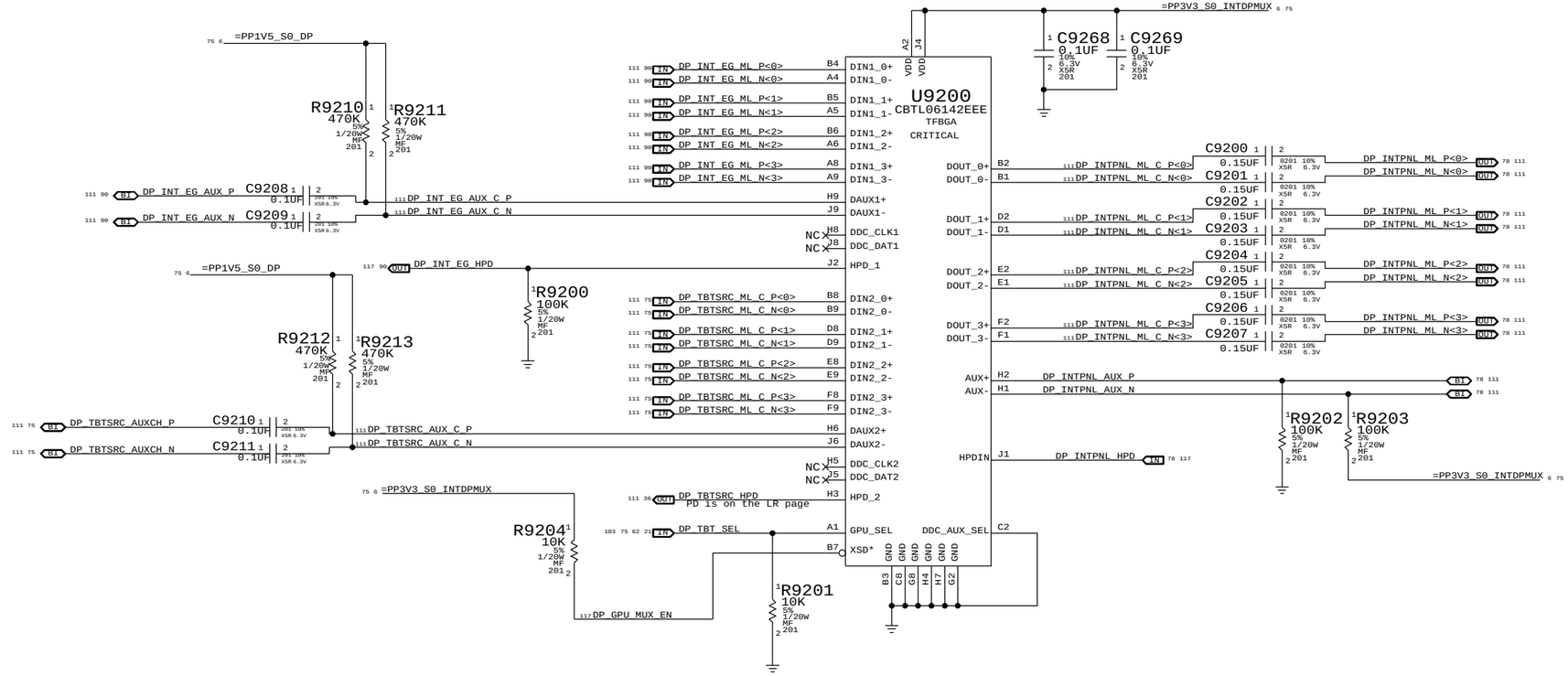
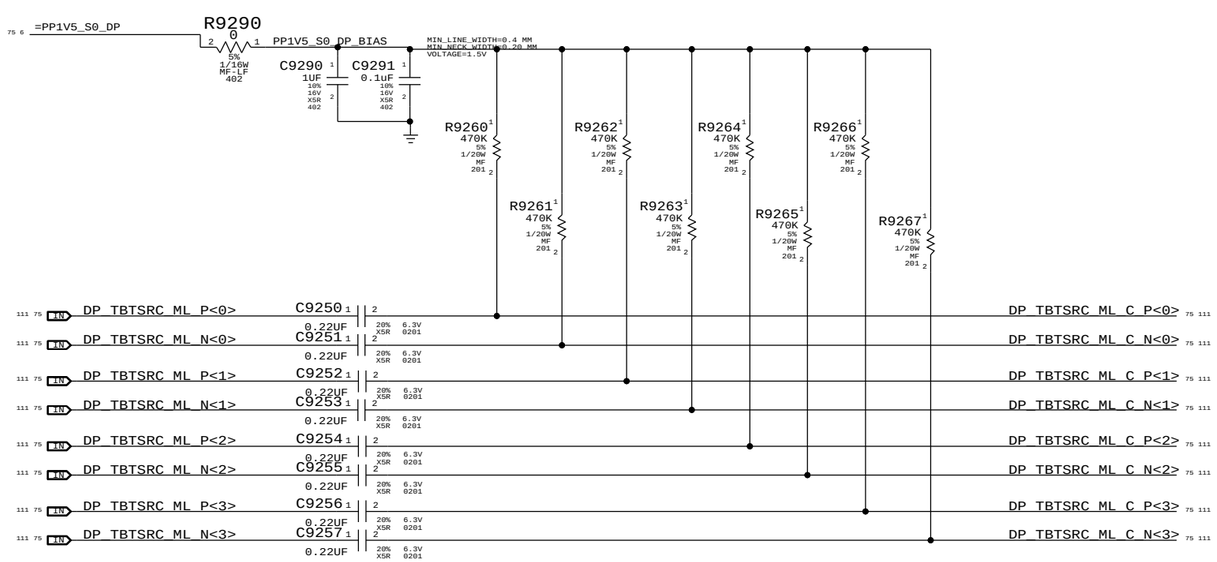
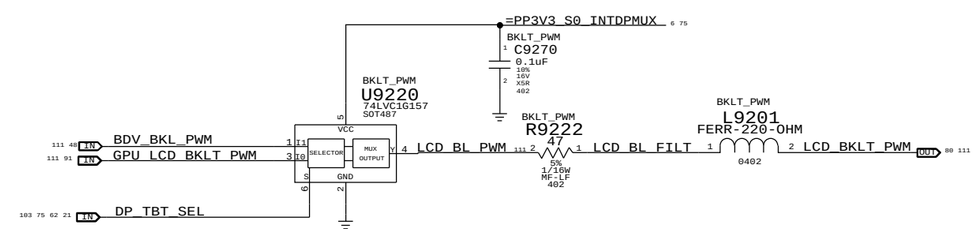
TP to DP aliases

| | | |
|---|---|---|
| TP_DP_TBTSRC_ML_CP<0> | DP_TBTSRC_ML_P<0> | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_ML_CN<0> | DP_TBTSRC_ML_N<0> | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_ML_CP<1> | DP_TBTSRC_ML_P<1> | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_ML_CN<1> | DP_TBTSRC_ML_N<1> | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_ML_CP<2> | DP_TBTSRC_ML_P<2> | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_ML_CN<2> | DP_TBTSRC_ML_N<2> | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_ML_CP<3> | DP_TBTSRC_ML_P<3> | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_ML_CN<3> | DP_TBTSRC_ML_N<3> | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_AUXCH_CP | DP_TBTSRC_AUXCH_P | MAKE_BASE=TRUE |
| TP_DP_TBTSRC_AUXCH_CN | DP_TBTSRC_AUXCH_N | MAKE_BASE=TRUE |

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| SYNC MASTER=D8 MLB | SYNC DATE=07/03/2012 |
| PAGE TITLE: Internal DP MUXing | |
| Apple Inc. | DRAWING NUMBER: 051-9505 SIZE: D |
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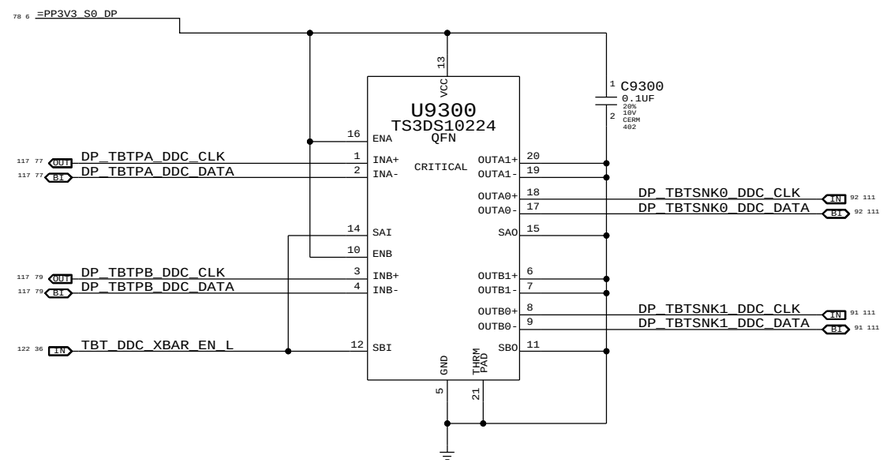
| | SHEET: 75 OF 123 |

# Dual-Port Host DDC Crossbar




SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE

## TBT DDC Crossbar

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

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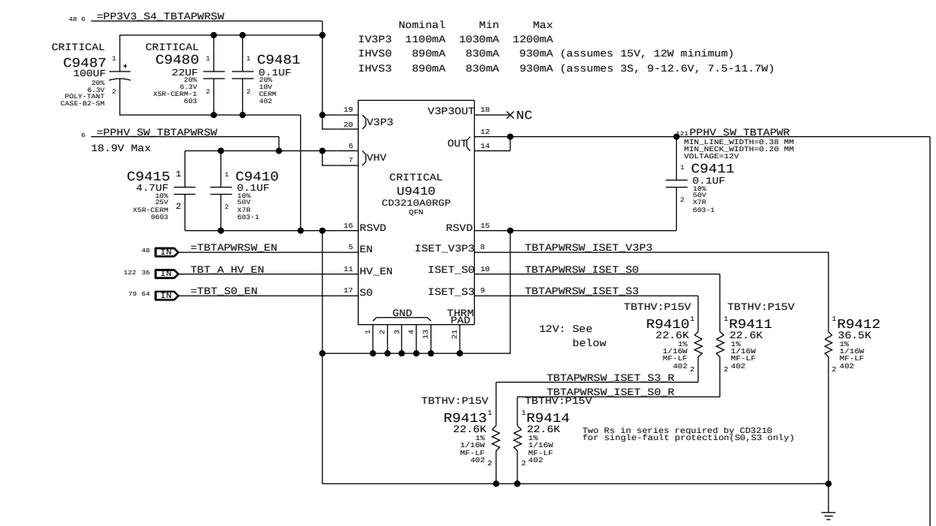
# 3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

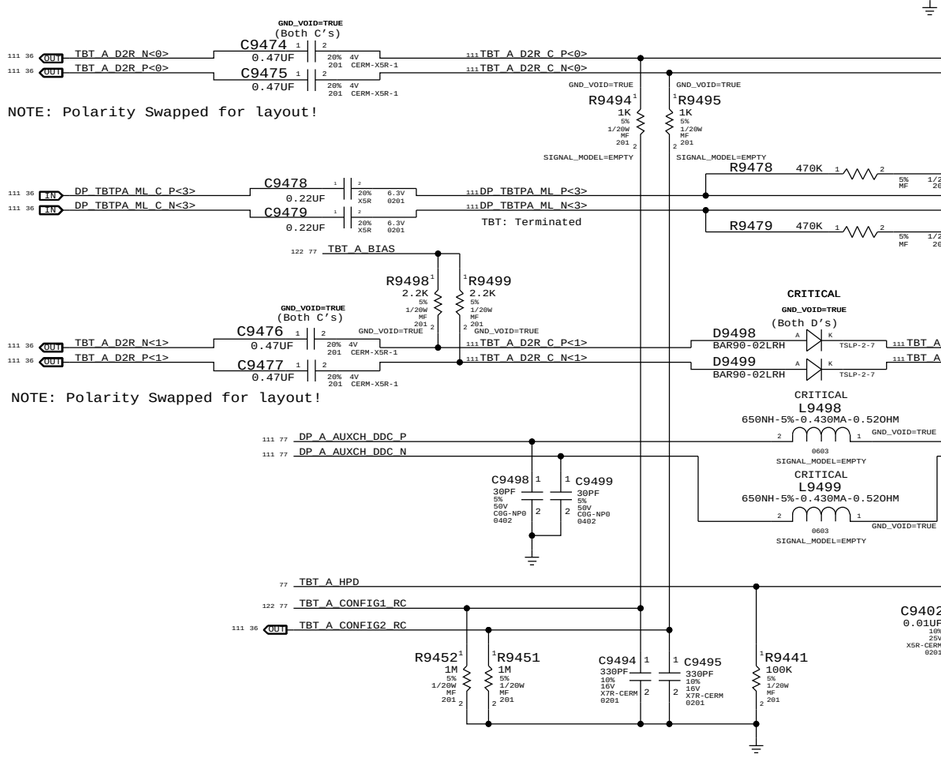
| | Nominal | Min | Max | |
|---|---|---|---|---|
| IV3P3 | 1100mA | 1030mA | 1200mA | |
| IHVS0 | 890mA | 830mA | 930mA | (assumes 15V, 12W minimum) |
| IHVS3 | 890mA | 830mA | 930mA | (assumes 3S, 9-12.6V, 7.5-11.7W) |

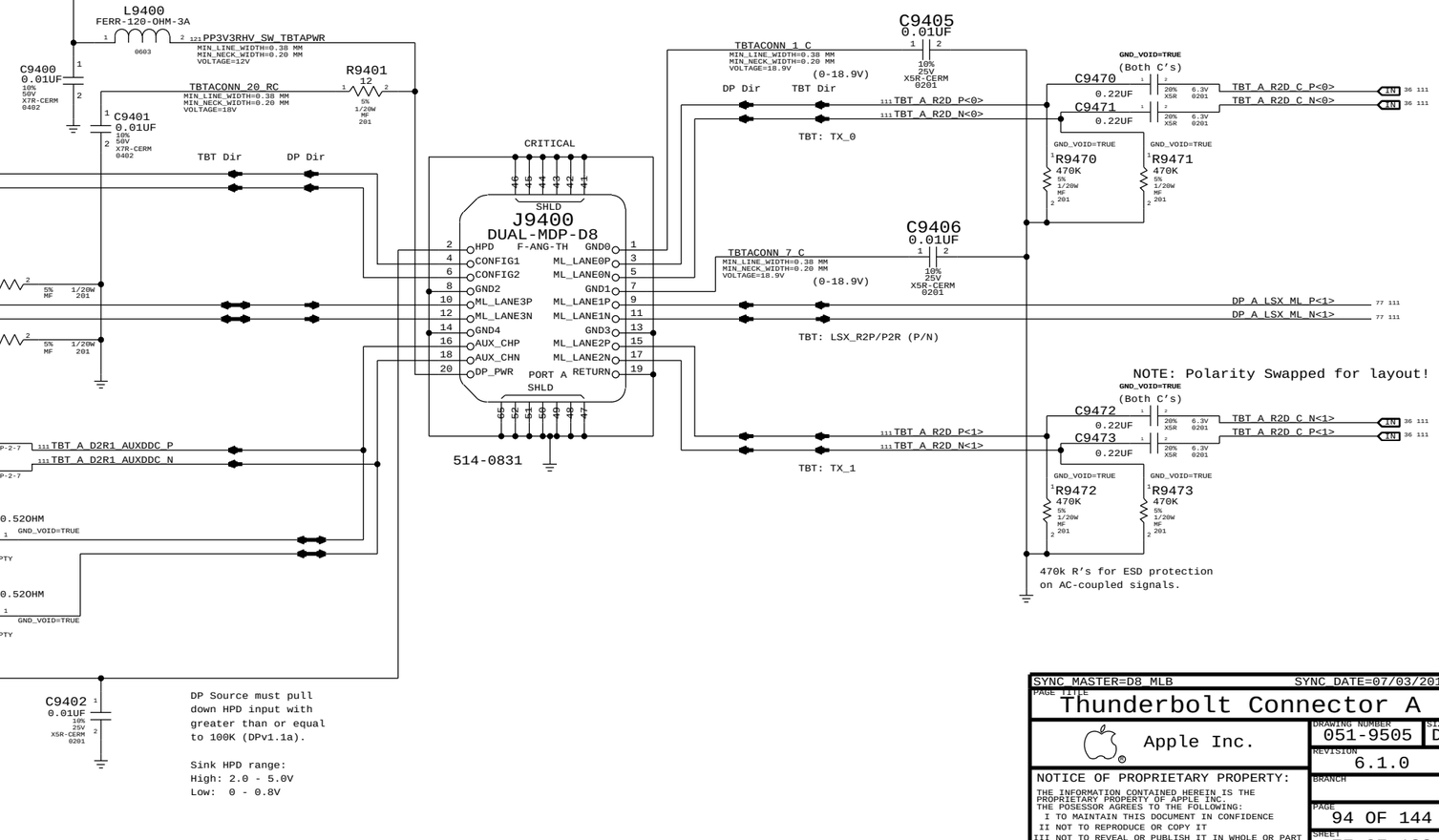



For 12V systems:

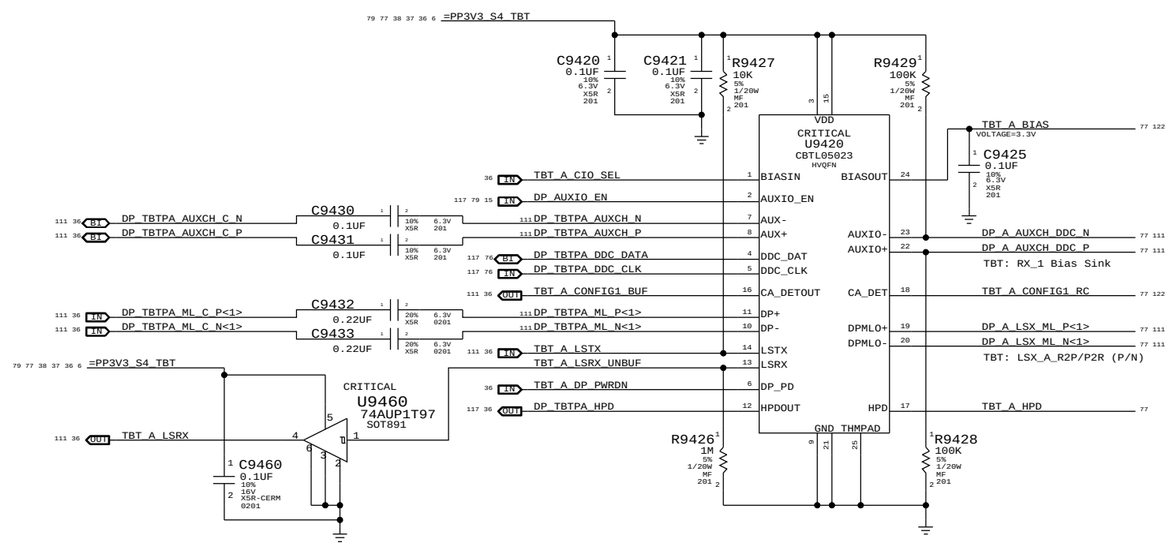
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 114S0338 | 2 | RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF | R9410,R9413 | | TBTHV:P12V |
| 114S0338 | 2 | RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF | R9411,R9414 | | TBTHV:P12V |

| | Nominal | Min | Max | |
|---|---|---|---|---|
| IHVS0/S3 | 1120mA | 1090mA | 1170mA | (12W minimum) |




# Thunderbolt Connector A

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| PAGE TITLE: Thunderbolt Connector A | |
| Apple Inc. | DRAWING NUMBER: 051-9505 SIZE: D |
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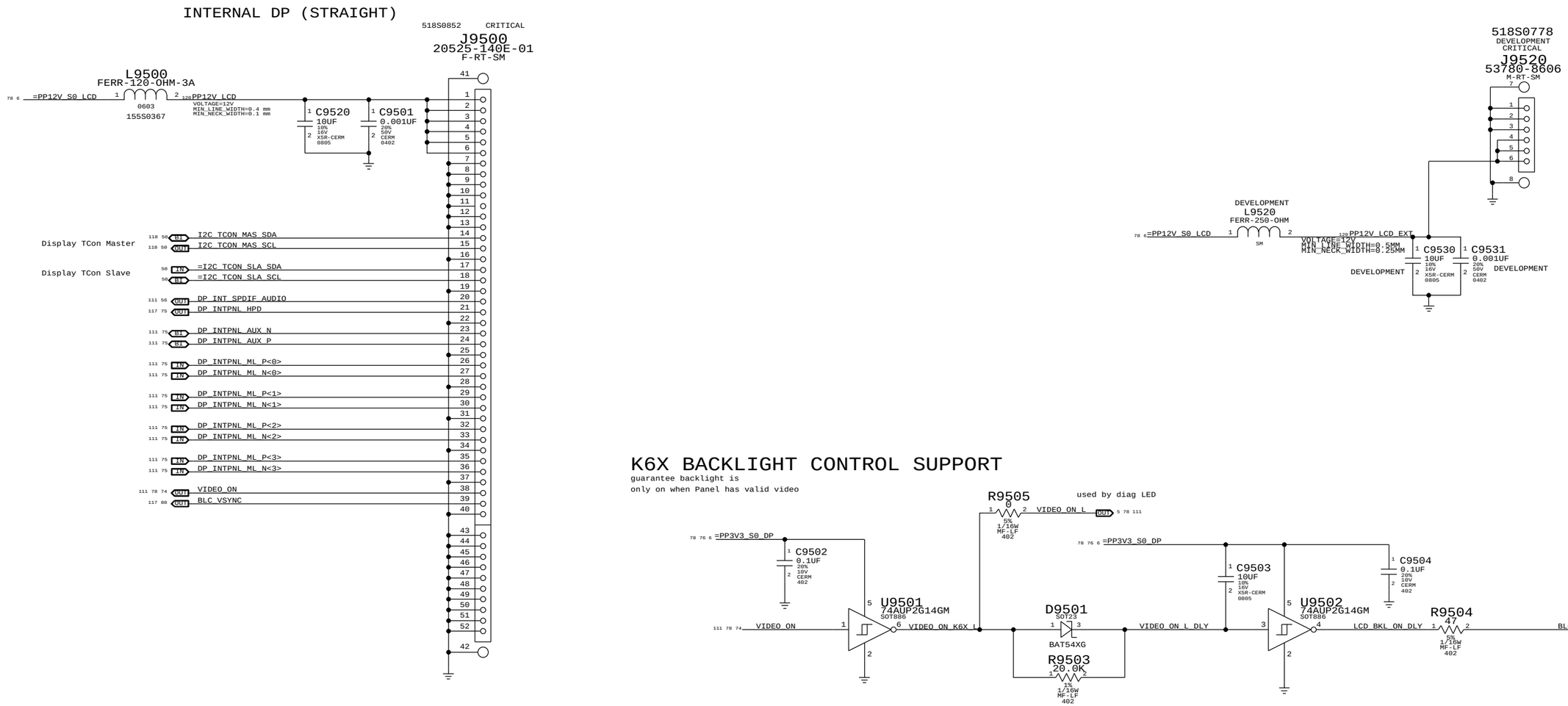
| | SHEET: 77 OF 123 |




| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 311S0566 | 1 | ONE BIT SELECTABLE DELAY | U9500 | Y | |

SYNC MASTER=D8_MLB SYNC DATE=07/03/2012

PAGE TITLE
# Internal DP Support

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

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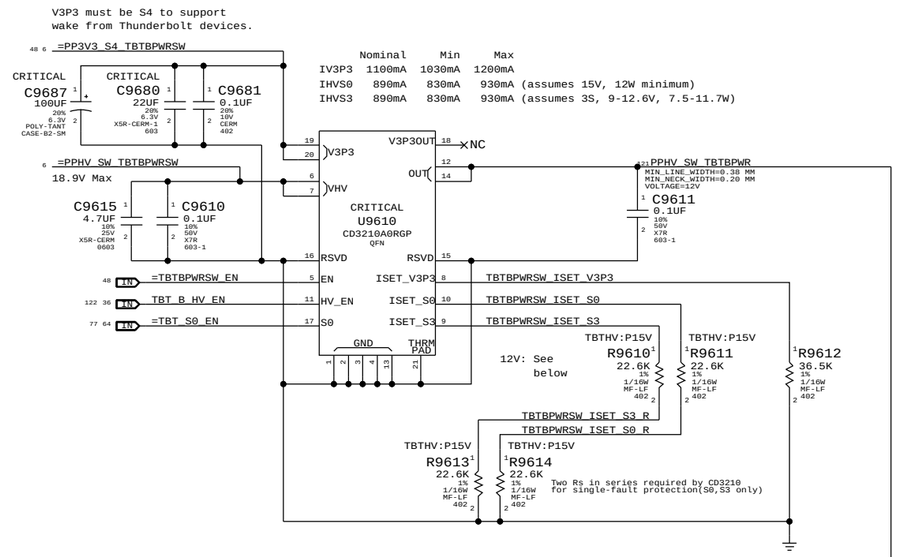
# 3.3V/HV Power MUX



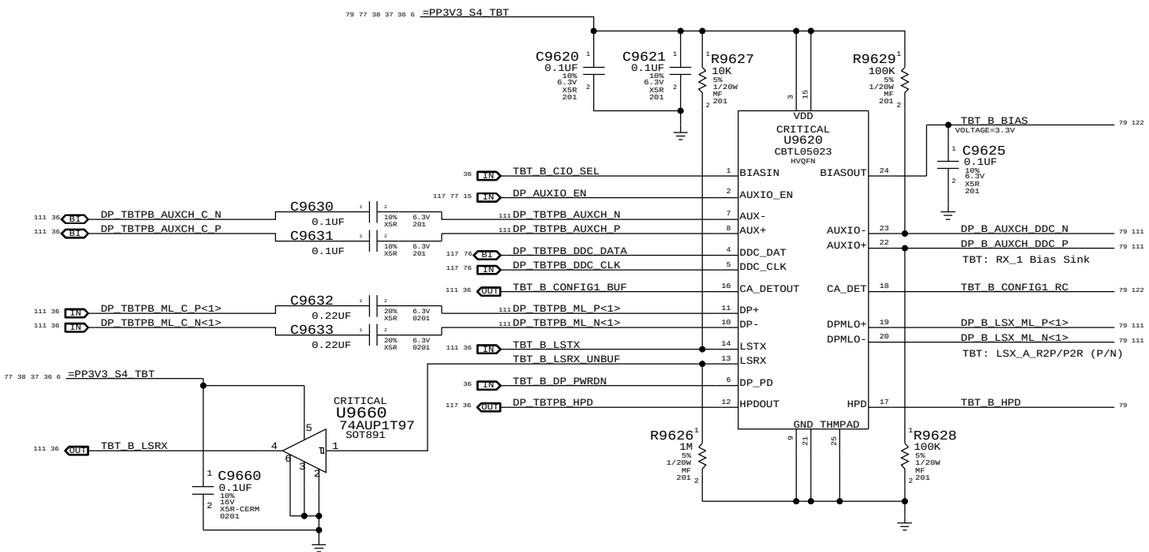

| | Nominal | Min | Max |
|---|---|---|---|
| IV3P3 | 1100mA | 1030mA | 1200mA |
| IHVS0 | 890mA | 830mA | 930mA (assumes 15V, 12W minimum) |
| IHVS3 | 890mA | 830mA | 930mA (assumes 3S, 9-12.6V, 7.5-11.7W) |

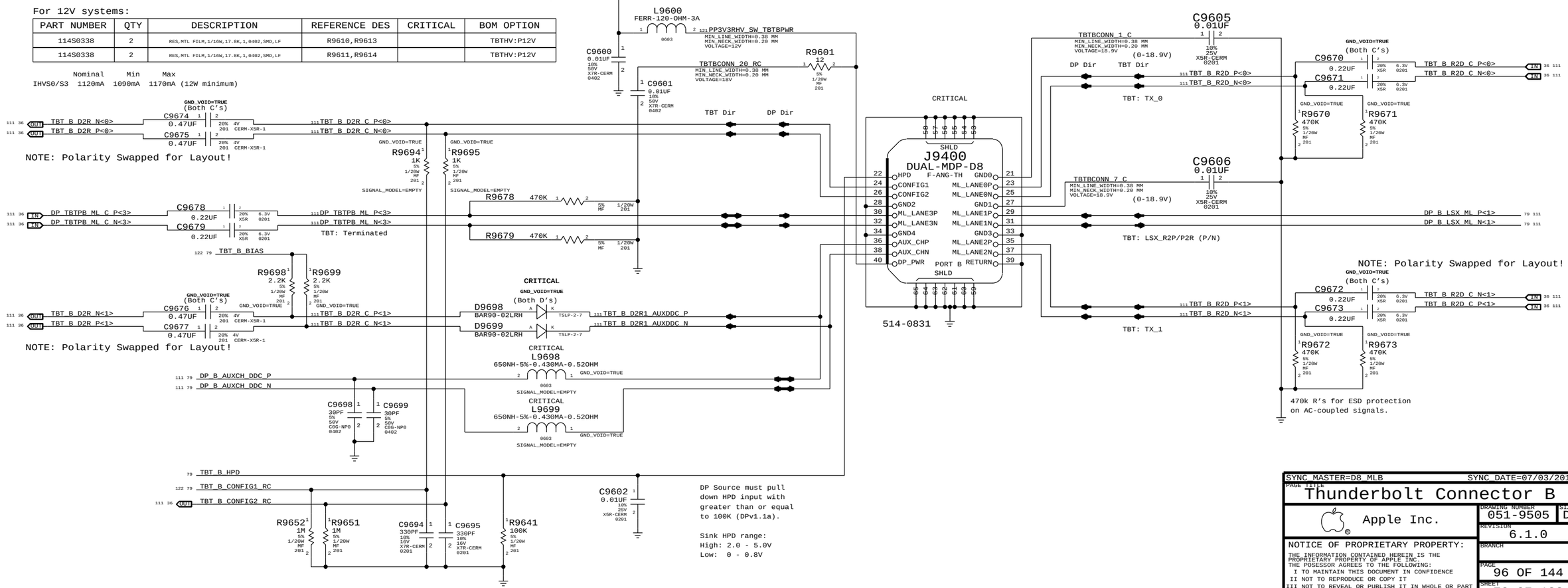
For 12V systems:

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 114S0338 | 2 | RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF | R9610,R9613 | | TBTHV:P12V |
| 114S0338 | 2 | RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF | R9611,R9614 | | TBTHV:P12V |

| | Nominal | Min | Max |
|---|---|---|---|
| IHVS0/S3 | 1120mA | 1090mA | 1170mA (12W minimum) |

# Thunderbolt Connector B

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| SYNC MASTER=D8_MLB | SYNC DATE=07/03/2012 |
| PAGE TITLE: Thunderbolt Connector B | |
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| | PAGE: 96 OF 144 |
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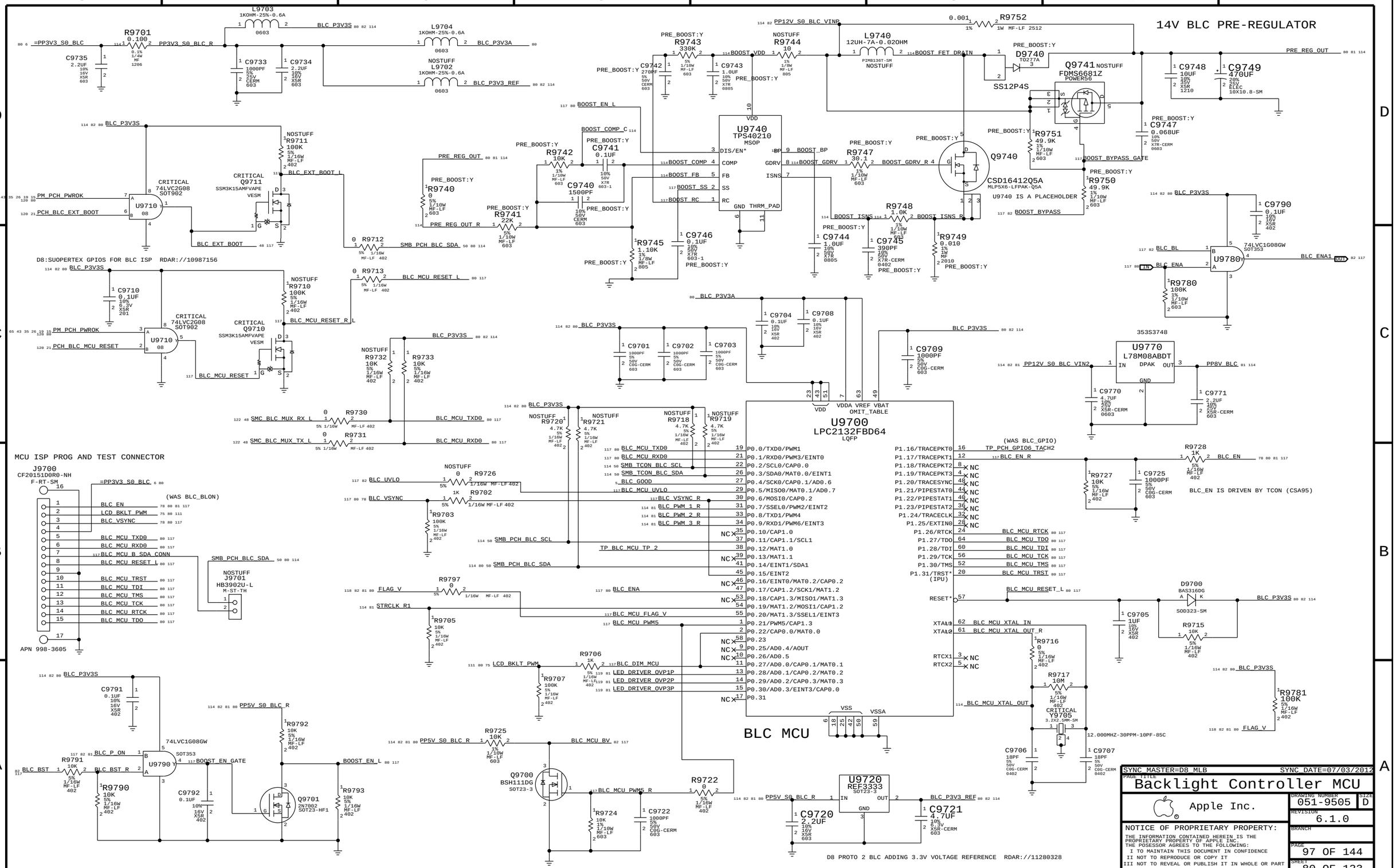


SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE

# Backlight Controller MCU

Apple Inc.

| DRAWING NUMBER | SIZE |
|---|---|
| 051-9505 | D |
| REVISION | |
| 6.1.0 | |
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| SHEET | |
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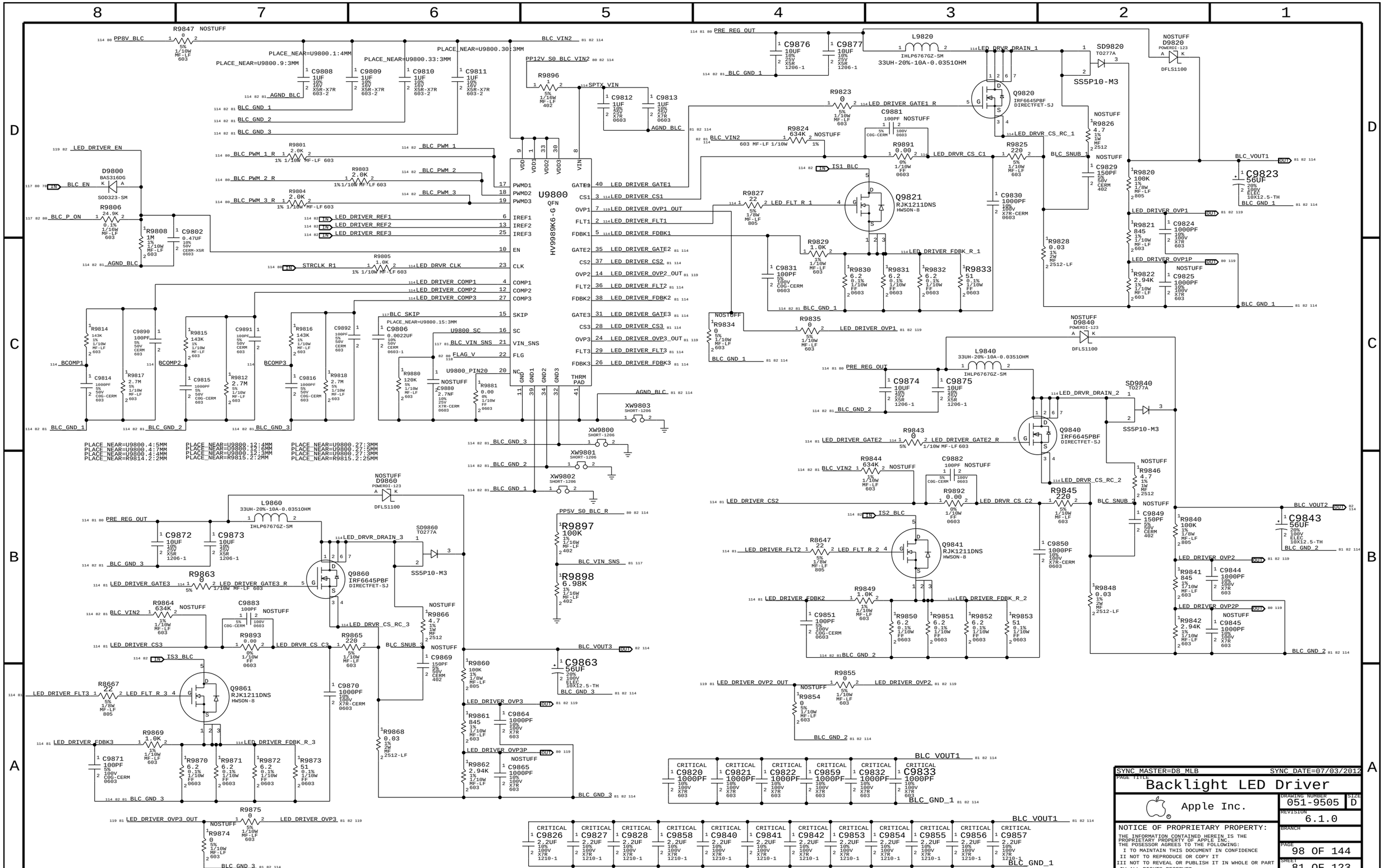
U9800
HV9989K6-G
QFN
Q9820
IRF6645PBF
DIRECTFET-SJ
Q9821
RJK1211DNS
HWSON-8
Q9840
IRF6645PBF
DIRECTFET-SJ
Q9841
RJK1211DNS
HWSON-8
Q9860
IRF6645PBF
DIRECTFET-SJ
Q9861
RJK1211DNS
HWSON-8
L9820
33UH-20%-10A-0.03510HM
IHLP6767GZ-SM
L9840
33UH-20%-10A-0.03510HM
IHLP6767GZ-SM
L9860
33UH-20%-10A-0.03510HM
IHLP6767GZ-SM
SD9820
TO277A
SS5P10-M3
SD9840
TO277A
SS5P10-M3
SD9860
TO277A
SS5P10-M3
D9800
BAS316DG
SOD323-SM
D9820
POWERDI-123
DFLS1100
D9840
POWERDI-123
DFLS1100
D9860
POWERDI-123
DFLS1100
PP8V_BLC
PP12V_S0_BLC_VIN2
PP5V_S0_BLC_R
PRE_REG_OUT
BLC_VIN2
BLC_VOUT1
BLC_VOUT2
BLC_VOUT3
BLC_GND_1
BLC_GND_2
BLC_GND_3
AGND_BLC
LED_DRIVER_EN
BLC_EN
BLC_P_ON
STRCLK_R1
IS1_BLC
IS2_BLC
IS3_BLC
LED_DRIVER_GATE1_R
LED_DRVR_DRAIN_1
LED_DRVR_CS_RC_1
LED_DRVR_CS_C1
LED_FLT_R_1
LED_DRIVER_FDBK_R_1
LED_DRIVER_OVP1
LED_DRIVER_OVP1P
LED_DRIVER_GATE2_R
LED_DRVR_DRAIN_2
LED_DRVR_CS_RC_2
LED_DRVR_CS_C2
LED_FLT_R_2
LED_DRIVER_FDBK_R_2
LED_DRIVER_OVP2
LED_DRIVER_OVP2P
LED_DRIVER_GATE3_R
LED_DRVR_DRAIN_3
LED_DRVR_CS_RC_3
LED_DRVR_CS_C3
LED_FLT_R_3
LED_DRIVER_FDBK_R_3
LED_DRIVER_OVP3
LED_DRIVER_OVP3P
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BLC_SNUB_2
BLC_SNUB_3
BLC_VIN_SNS
BCOMP1
BCOMP2
BCOMP3
SYNC_MASTER=D8_MLB
SYNC_DATE=07/03/2012
PAGE TITLE
Backlight LED Driver
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
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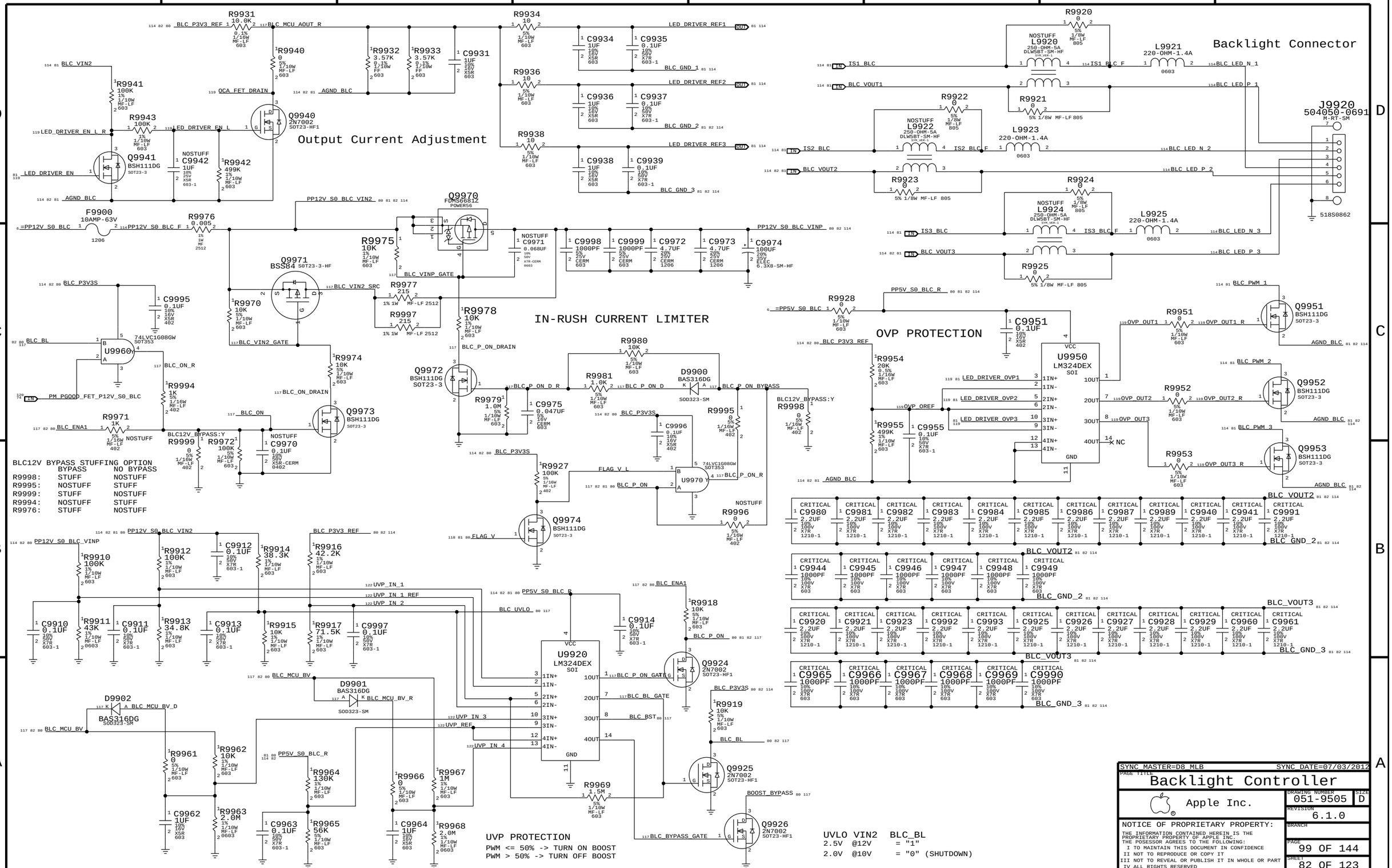
Output Current Adjustment
IN-RUSH CURRENT LIMITER
OVP PROTECTION
Backlight Connector
UVP PROTECTION
PWM <= 50% -> TURN ON BOOST
PWM > 50% -> TURN OFF BOOST
UVLO VIN2 BLC_BL
2.5V @12V = "1"
2.0V @10V = "0" (SHUTDOWN)
BLC12V BYPASS STUFFING OPTION
BYPASS NO BYPASS
R9998: STUFF NOSTUFF
R9995: NOSTUFF STUFF
R9999: STUFF NOSTUFF
R9994: NOSTUFF STUFF
R9976: STUFF NOSTUFF
SYNC_MASTER=D8_MLB
SYNC_DATE=07/03/2012
PAGE TITLE
Backlight Controller
Apple Inc.
DRAWING NUMBER 051-9505
SIZE D
REVISION 6.1.0
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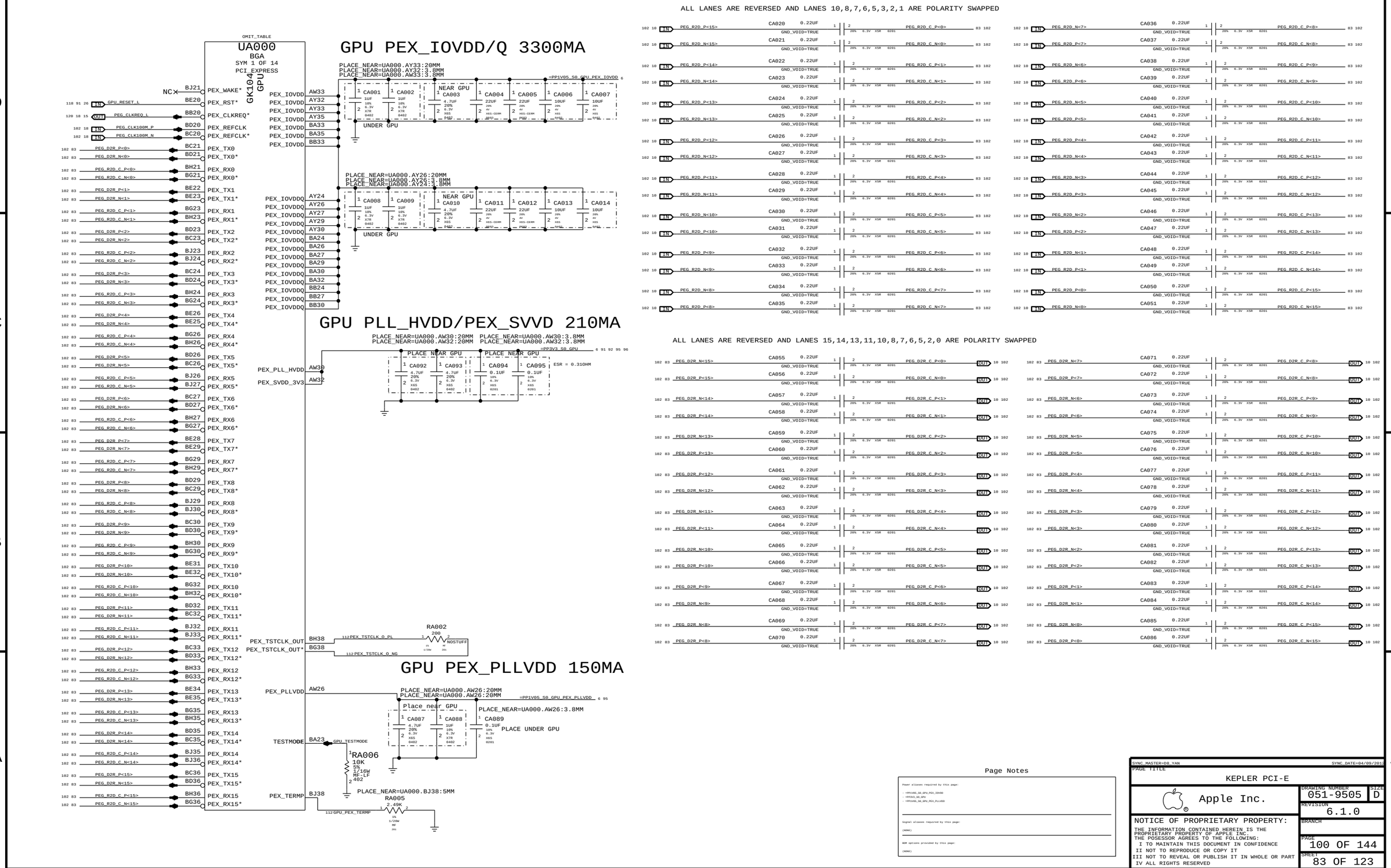
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ALL LANES ARE REVERSED AND LANES 15,14,13,11,10,8,7,6,5,2,0 ARE POLARITY SWAPPED
UA000
BGA
SYM 1 OF 14
PCI_EXPRESS
GK104 GPU
GPU PEX_IOVDD/Q 3300MA
PLACE_NEAR=UA000.AY33:20MM
PLACE_NEAR=UA000.AY32:3.8MM
PLACE_NEAR=UA000.AW33:3.8MM
=PP1V05_S0_GPU_PEX_IOVDD
NEAR GPU
UNDER GPU
PLACE_NEAR=UA000.AY26:20MM
PLACE_NEAR=UA000.AY26:3.8MM
PLACE_NEAR=UA000.AY24:3.8MM
GPU PLL_HVDD/PEX_SVVD 210MA
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PLACE_NEAR=UA000.AW32:20MM
PLACE_NEAR=UA000.AW30:3.8MM
PLACE_NEAR=UA000.AW32:3.8MM
=PP3V3_S0_GPU
PLACE NEAR GPU
ESR = 0.310HM
RA002
200
NOSTUFF
GPU PEX_PLLVDD 150MA
=PP1V05_S0_GPU_PEX_PLLVDD
Place near GPU
PLACE_NEAR=UA000.AW26:3.8MM
PLACE UNDER GPU
RA006
10K
5%
1/16W
MF-LF
402
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RA005
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SYNC_DATE=04/09/2013
PAGE TITLE
KEPLER PCI-E
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
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REVISION
6.1.0
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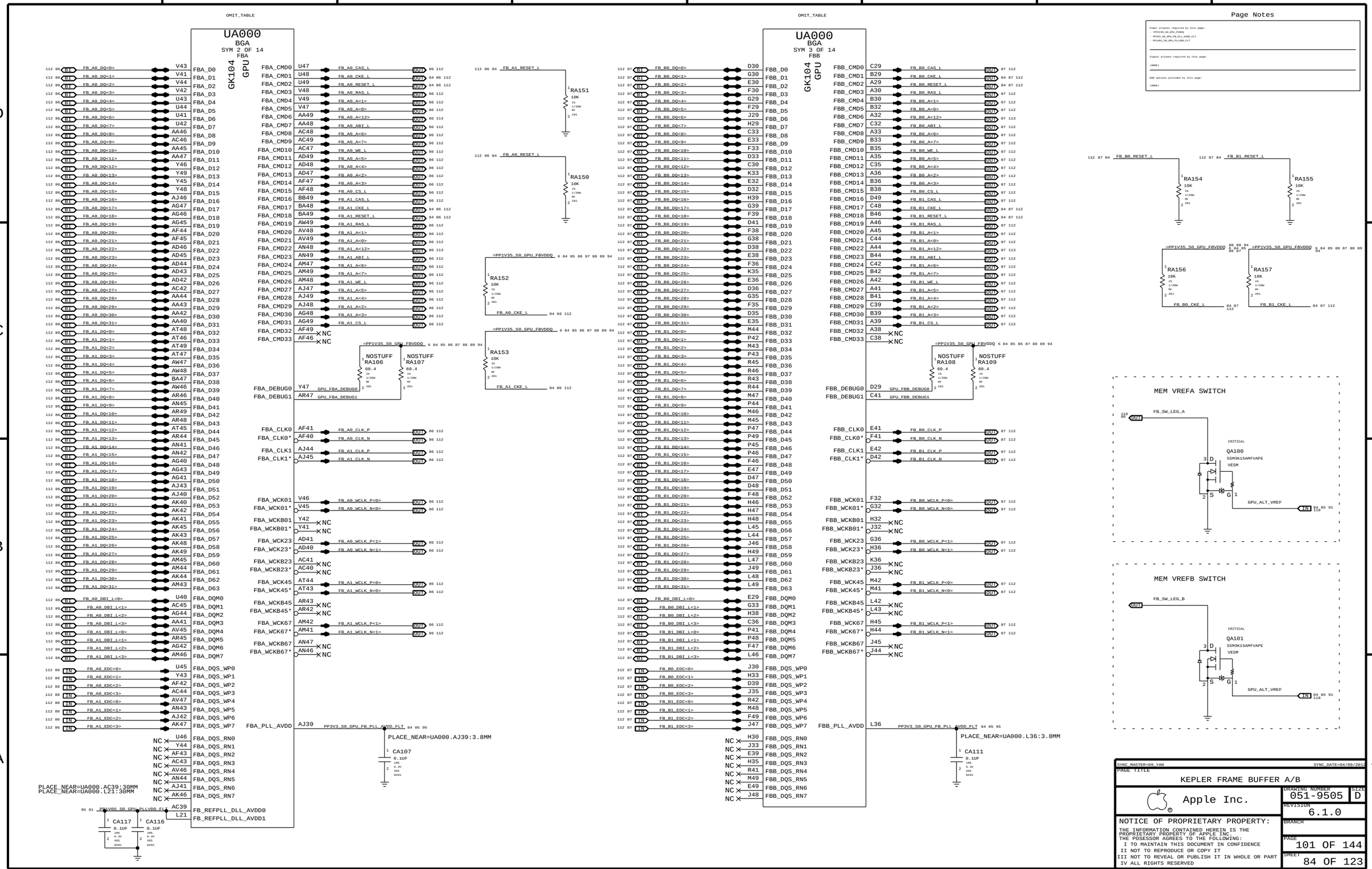
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BGA
SYM 2 OF 14
FBA
GK104 GPU
OMIT_TABLE
UA000
BGA
SYM 3 OF 14
FBB
GK104 GPU
OMIT_TABLE
Page Notes
MEM VREFA SWITCH
QA100
SSM3K15AMFVAPE
VESM
MEM VREFB SWITCH
QA101
SSM3K15AMFVAPE
VESM
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SYNC_MASTER=DB_YAN
SYNC_DATE=04/09/2012
PAGE TITLE
KEPLER FRAME BUFFER A/B
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
D
REVISION
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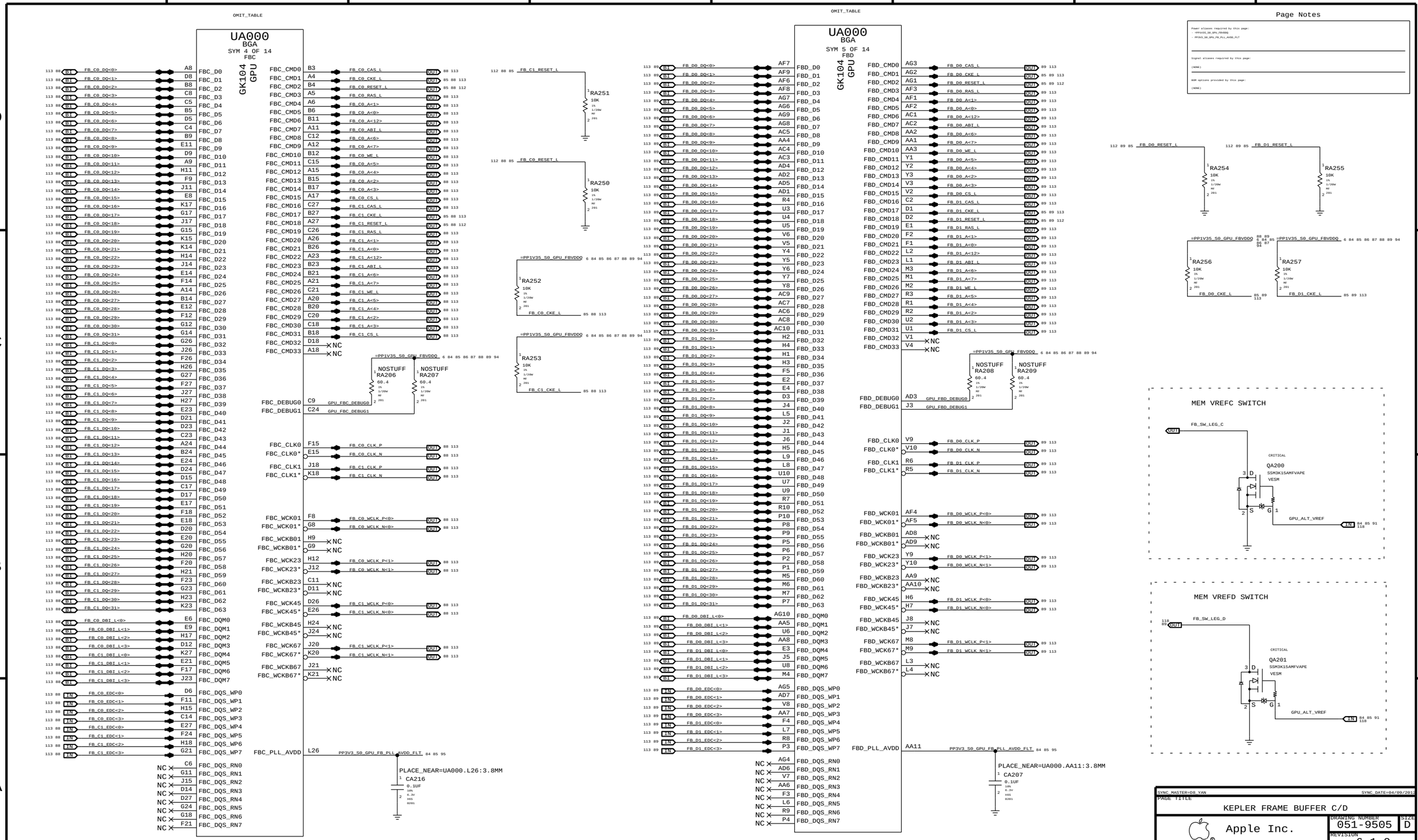


SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2013

PAGE TITLE

KEPLER FRAME BUFFER C/D

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DRAWING NUMBER 051-9505 SIZE D

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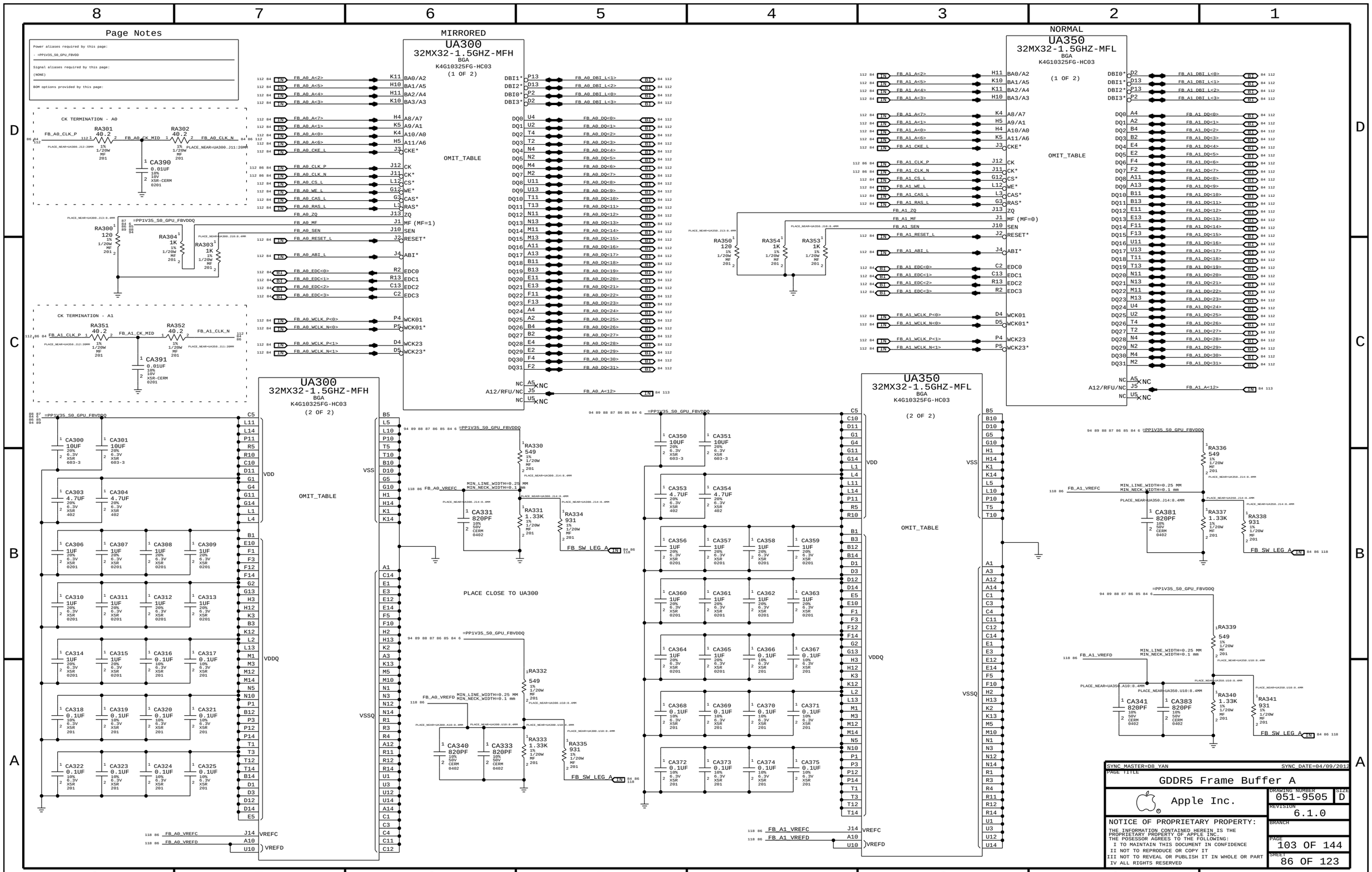
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Signal aliases required by this page:
(NONE)
BOM options provided by this page:
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UA300
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BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
NORMAL
UA350
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
CK TERMINATION - A0
CK TERMINATION - A1
UA300
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
PLACE CLOSE TO UA300
UA350
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2013
PAGE TITLE
GDDR5 Frame Buffer A
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
D
REVISION
6.1.0
BRANCH
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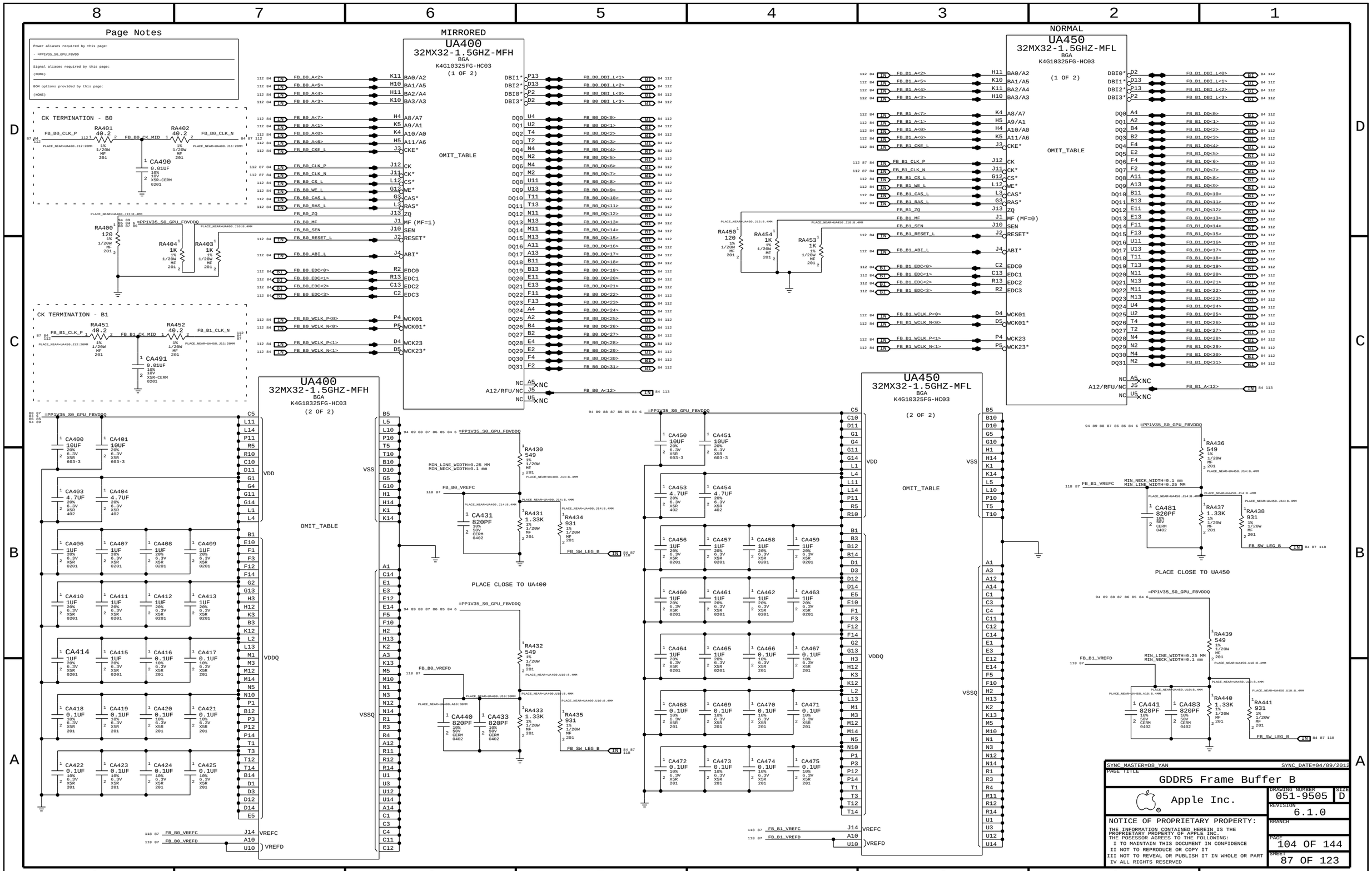
Page Notes
Power aliases required by this page:
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Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
MIRRORED
UA400
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
NORMAL
UA450
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
UA400
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
UA450
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
CK TERMINATION - B0
CK TERMINATION - B1
PLACE CLOSE TO UA400
PLACE CLOSE TO UA450
VDD
VDDQ
VSS
VSSQ
VREFC
VREFD
SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2013
PAGE TITLE
GDDR5 Frame Buffer B
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
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REVISION
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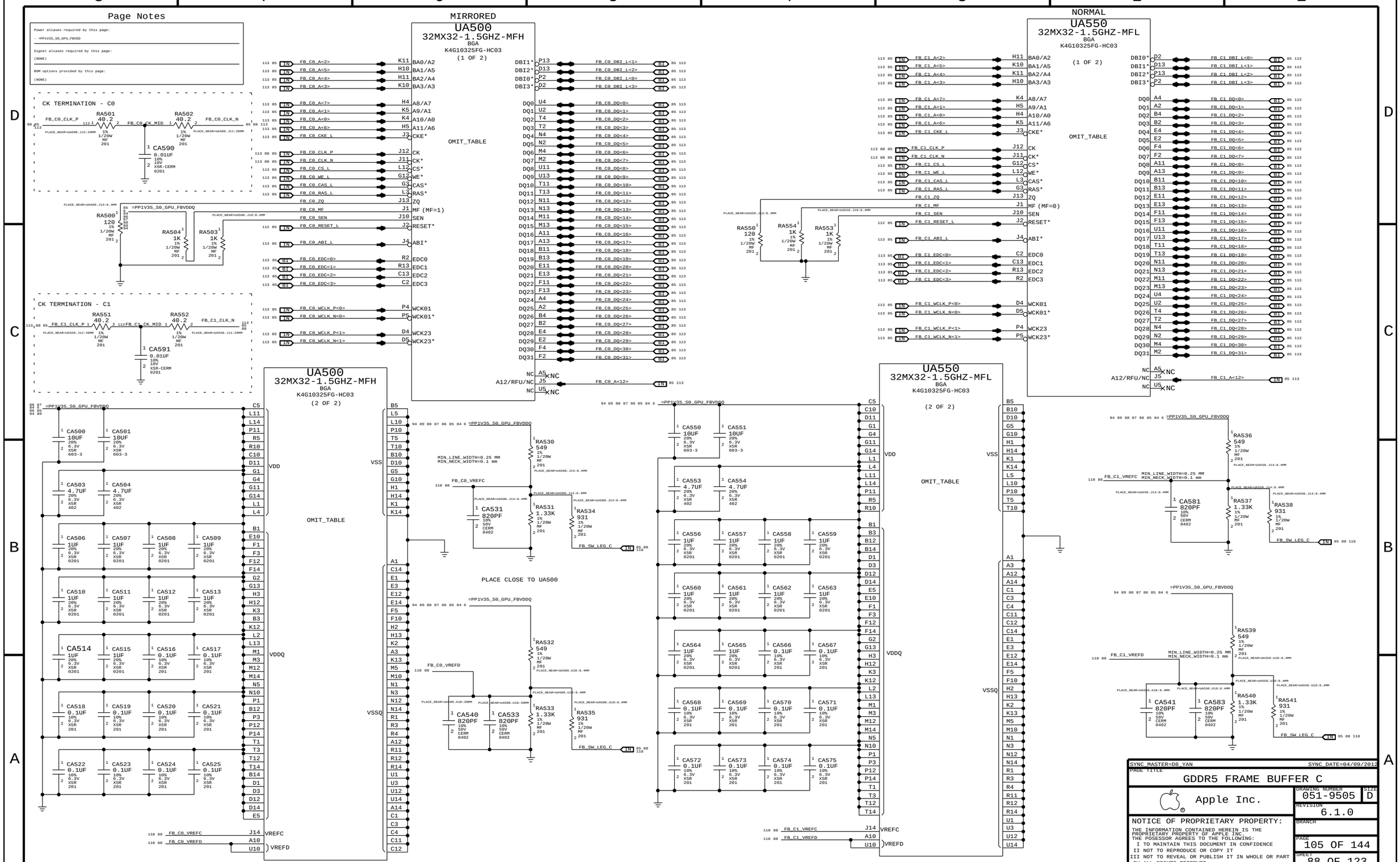
Page Notes
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Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
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UA500
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
NORMAL
UA550
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)
OMIT_TABLE
CK TERMINATION - C0
CK TERMINATION - C1
UA500
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
PLACE CLOSE TO UA500
UA550
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)
OMIT_TABLE
VDD
VDDQ
VSS
VSSQ
VREFC
VREFD
SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2013
PAGE TITLE
GDDR5 FRAME BUFFER C
Apple Inc.
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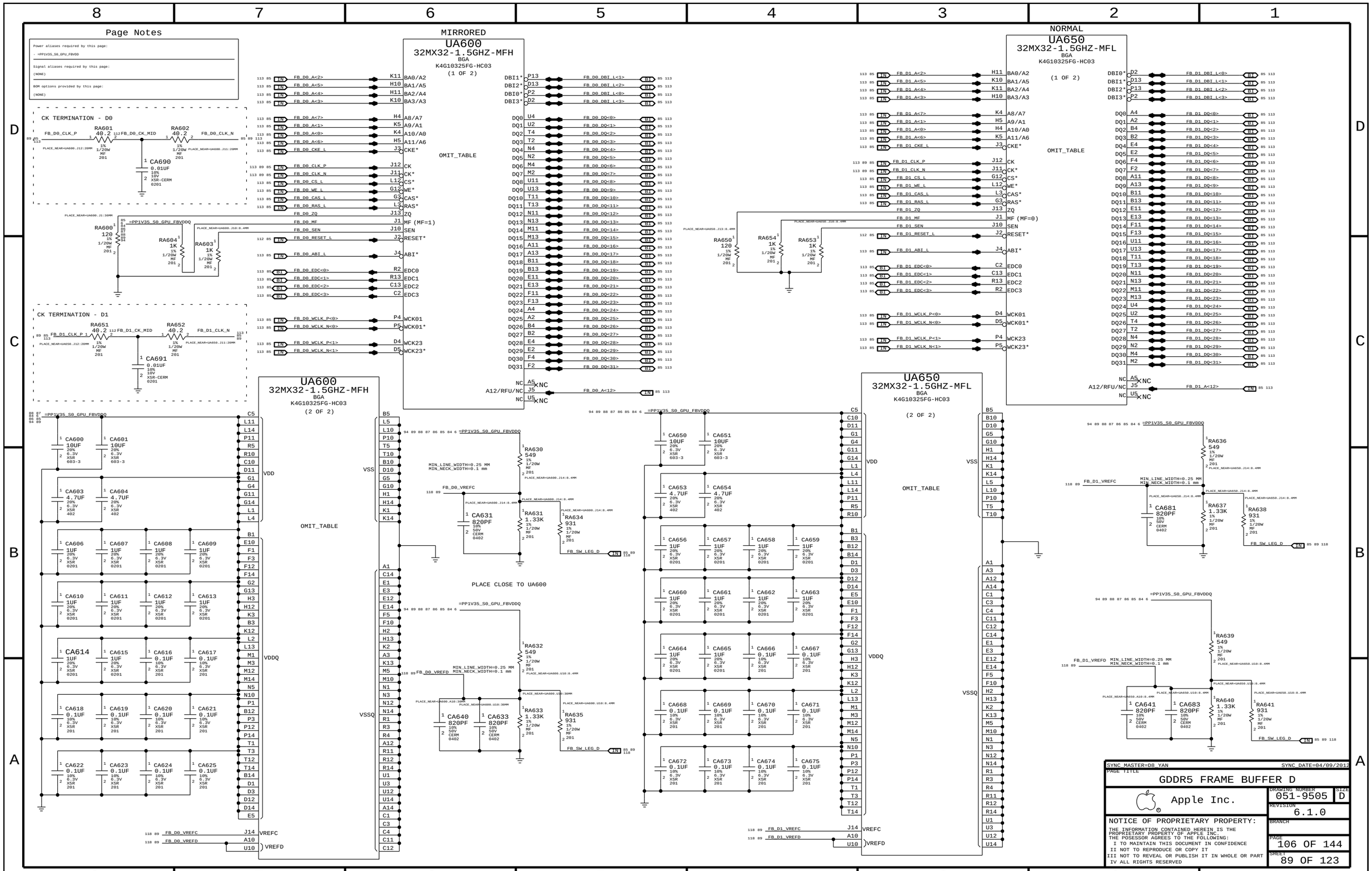
Page Notes
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- =PP1V35_S0_GPU_FBVDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)
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CK TERMINATION - D1
MIRRORED
UA600
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)
(2 OF 2)
OMIT_TABLE
NORMAL
UA650
32MX32-1.5GHZ-MFL
PLACE CLOSE TO UA600
VDD
VDDQ
VSS
VSSQ
VREFC
VREFD
SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2013
PAGE TITLE
GDDR5 FRAME BUFFER D
Apple Inc.
DRAWING NUMBER
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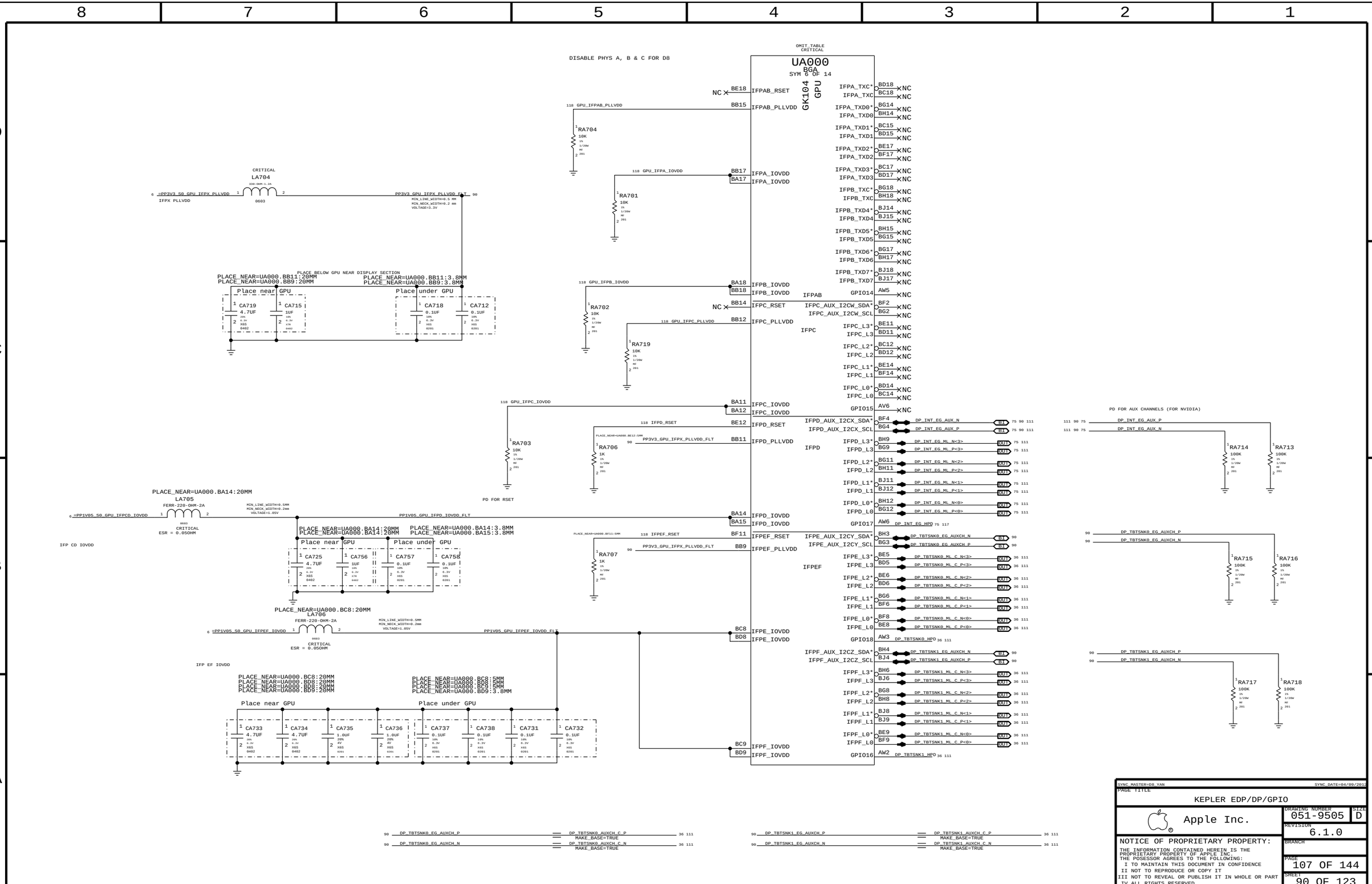


SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE

KEPLER EDP/DP/GPIO

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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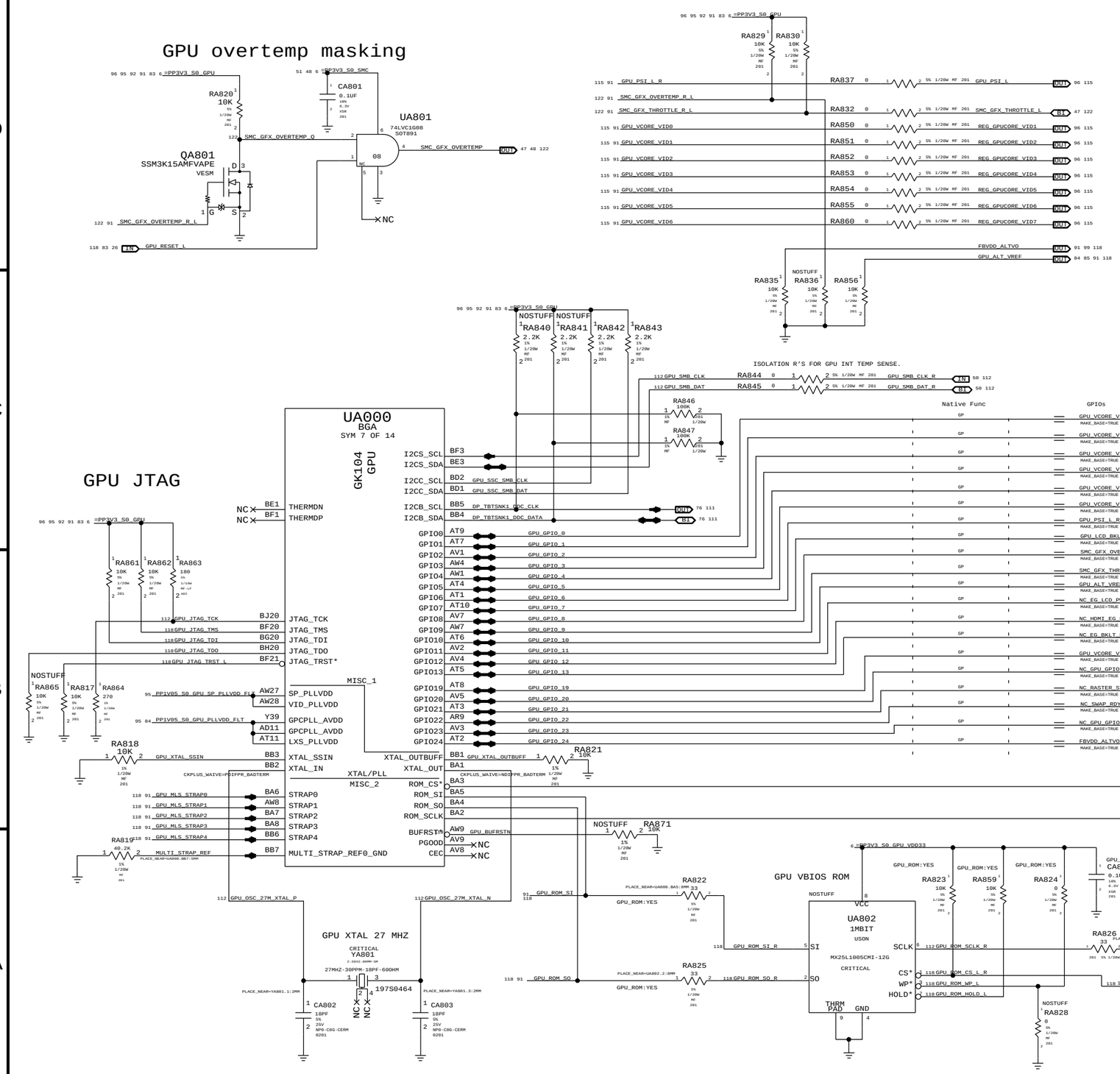
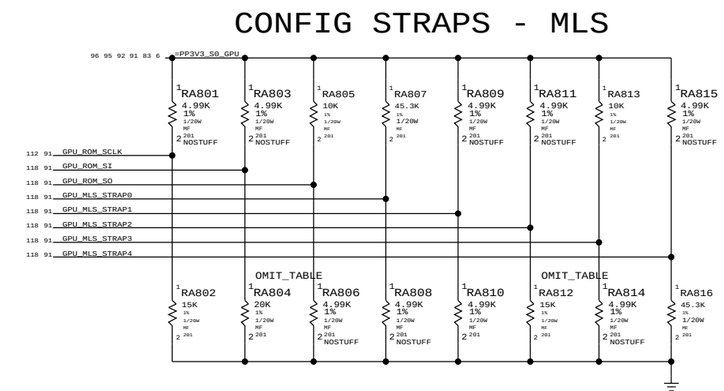



| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|---|---|---|---|---|---|
| 118S0175 | 1 | RES,MF,20KOHM,1,1/20W,0201 | RA804 | CRITICAL | FB:1G_SAMSUNG |
| 118S0105 | 1 | RES,MF,15KOHM,1,1/20W,0201 | RA804 | CRITICAL | FB:1G_HYNIX |
| 118S0385 | 1 | RES,MF,45.3KOHM,1,1/20W,0201 | RA804 | CRITICAL | FB:2G_SAMSUNG |
| 118S0315 | 1 | RES,MF,34.8KOHM,1,1/20W,0201 | RA804 | CRITICAL | FB:2G_HYNIX |
| 118S0175 | 1 | RES,MF,20KOHM,1,1/20W,0201 | RA812 | CRITICAL | GPU:104GTX |
| 118S0105 | 1 | RES,MF,15KOHM,1,1/20W,0201 | RA812 | CRITICAL | GPU:104GT |
| 118S0105 | 1 | RES,MF,15KOHM,1,1/20W,0201 | RA812 | CRITICAL | GPU:104GT2 |




SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2013

PAGE TITLE

KEPLER GPIO/STRAPPING

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

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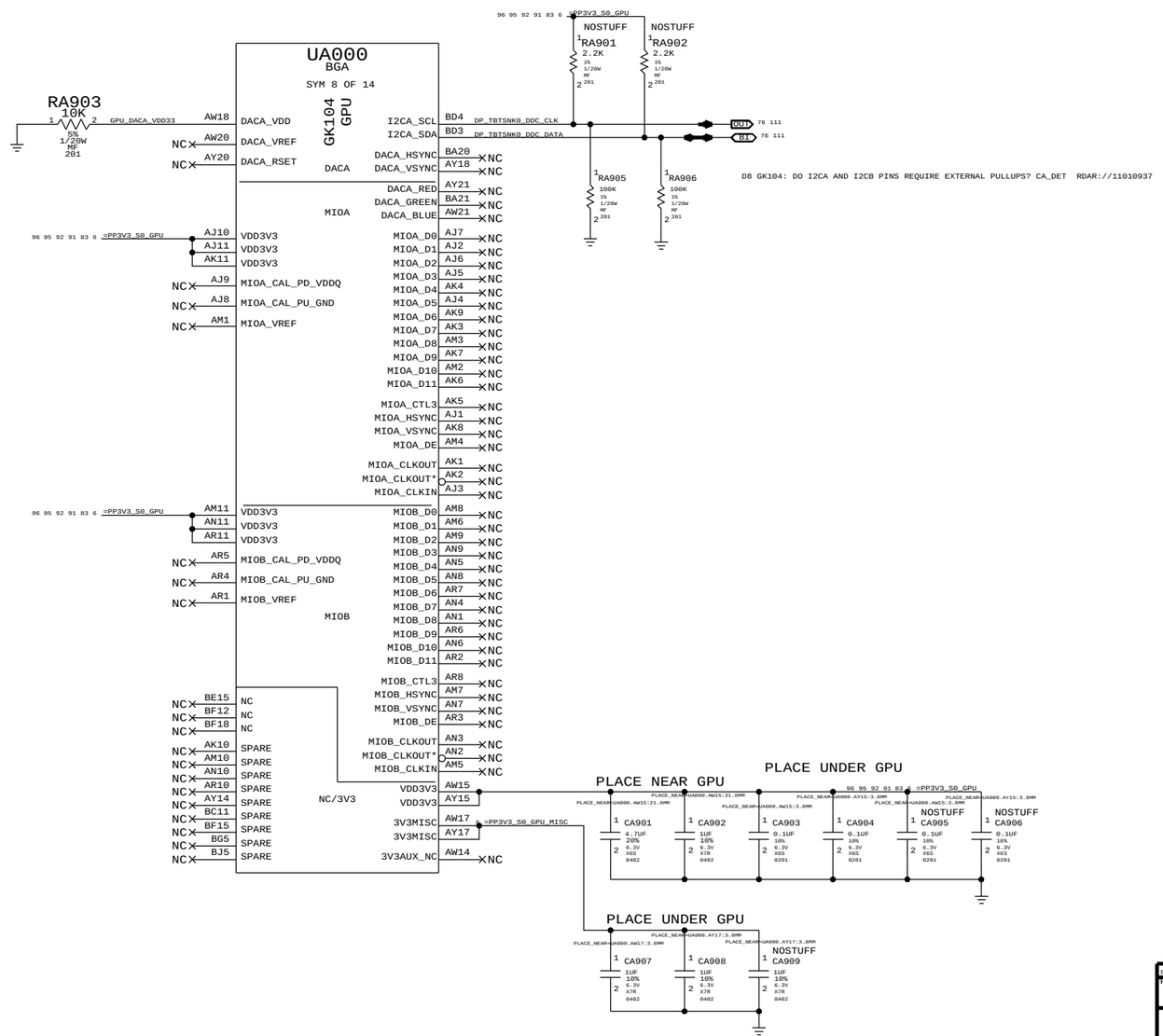


SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2013

PAGE TITLE

KEPLER MISC

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DRAWING NUMBER 051-9505

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# GPU NVVDD DECOUPLING I(EDP)=95A

Page Notes

Power aliases required by this page:

- =PPVCORE_S0_GPU

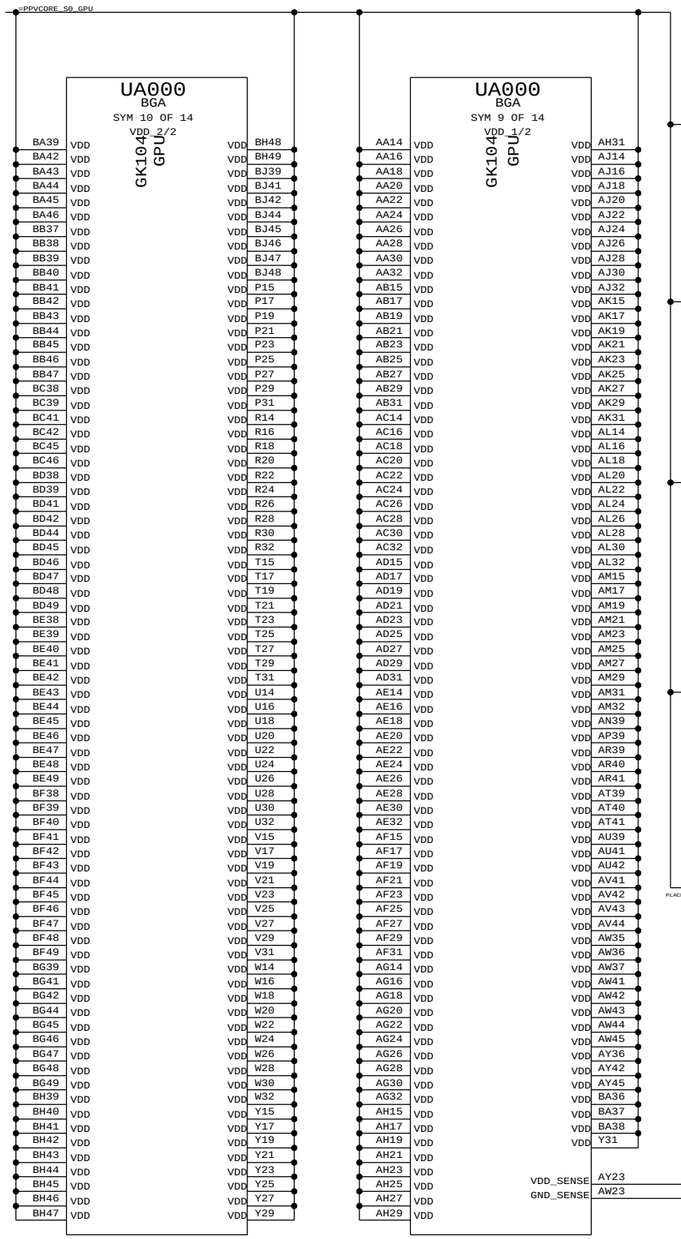
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

93 51 6 =PPVCORE_S0_GPU




## PLACE UNDER GPU

CB101 CB102 CB103 CB104 CB105 CB106 CB107 CB108 CB109 CB110 CB111 CB112 CB113 CB114 CB115 CB116 CB117 CB118 CB119 CB120
4.7UF 20% 6.3V X6S 0402

## PLACE UNDER GPU

CB121 CB122 CB123 CB124 CB125 CB126 CB127 CB128 CB129 CB130 CB131 CB132 CB133 CB134 CB135 CB136 CB137 CB138 CB139 CB140
4.7UF 20% 6.3V X6S 0402

## PLACE UNDER GPU

CB141 CB142 CB143 CB144 CB145 CB146 CB147 CB148 CB149 CB150 CB151 CB152 CB153 CB154 CB155 CB156 CB157 CB158 CB159 CB160
1.0UF 20% 4V X6S 0201

## PLACE UNDER GPU

CB161 CB162 CB163 CB164 CB171 CB172 CB173 CB174 CB175 CB176 CB177 CB178 CB179 CB180 CB181 CB191 CB192 CB193 CB194
10UF 20% 4V X6S 0402
18UF 20% 4V X6S 0402
22UF 20% 4V X6S-CERM 0603
47UF 20% 4V X6S 0805

## PLACE NEAR GPU W/ 35MM FROM GPU CENTER

PLACE_NEAR=UA000.AT40:35MM
CRITICAL
CB165
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:35MM
CRITICAL
CB166
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:42MM
CRITICAL
CB167
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:38MM
CRITICAL
CB168
330UF-0.006OHM 20% 2V POLY CASE-D2-SM

=PPVCORE_S0_GPU 6 51 93

NOSTUFF
RB101
100 5% 1/20W MF 201

MIN_LINE_WIDTH=0.41 MM
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=1.0V
VSNS_GPU_VDD → OUT 96 115

VSNS_GPU_VSS → OUT 96 115
MIN_LINE_WIDTH=0.41MM
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=0V

NOSTUFF
RB102
100 5% 1/20W MF 201

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE
KEPLER CORE POWER

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D
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# GPU FBVDD/Q DECOUPLING I(EDP PEAK)=26A

Page Notes

Power aliases required by this page:

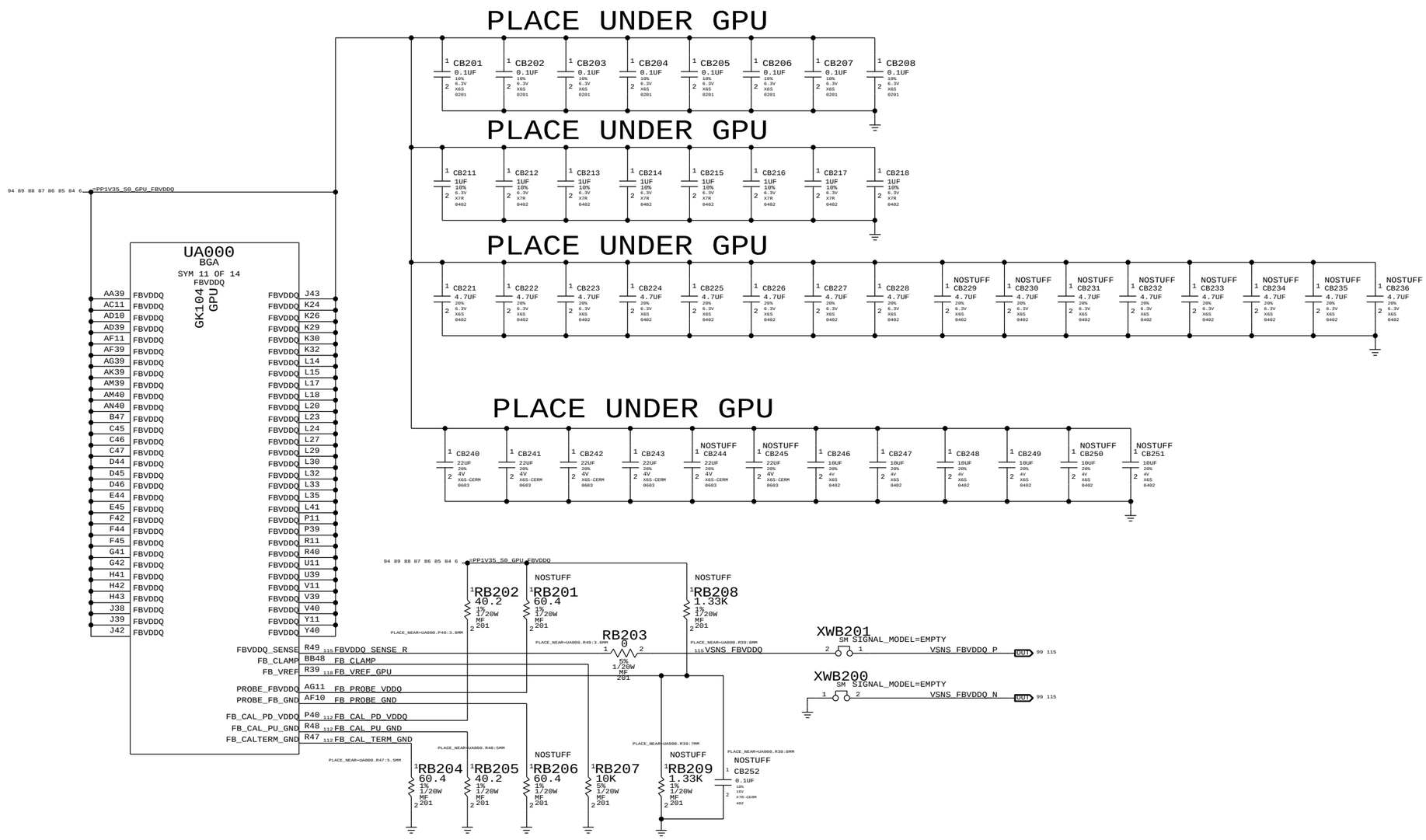
- +PP1V35_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)




SYNC_MASTER=DB_YAN SYNC_DATE=04/09/2013

PAGE TITLE

KEPLER FBVDD/Q POWER

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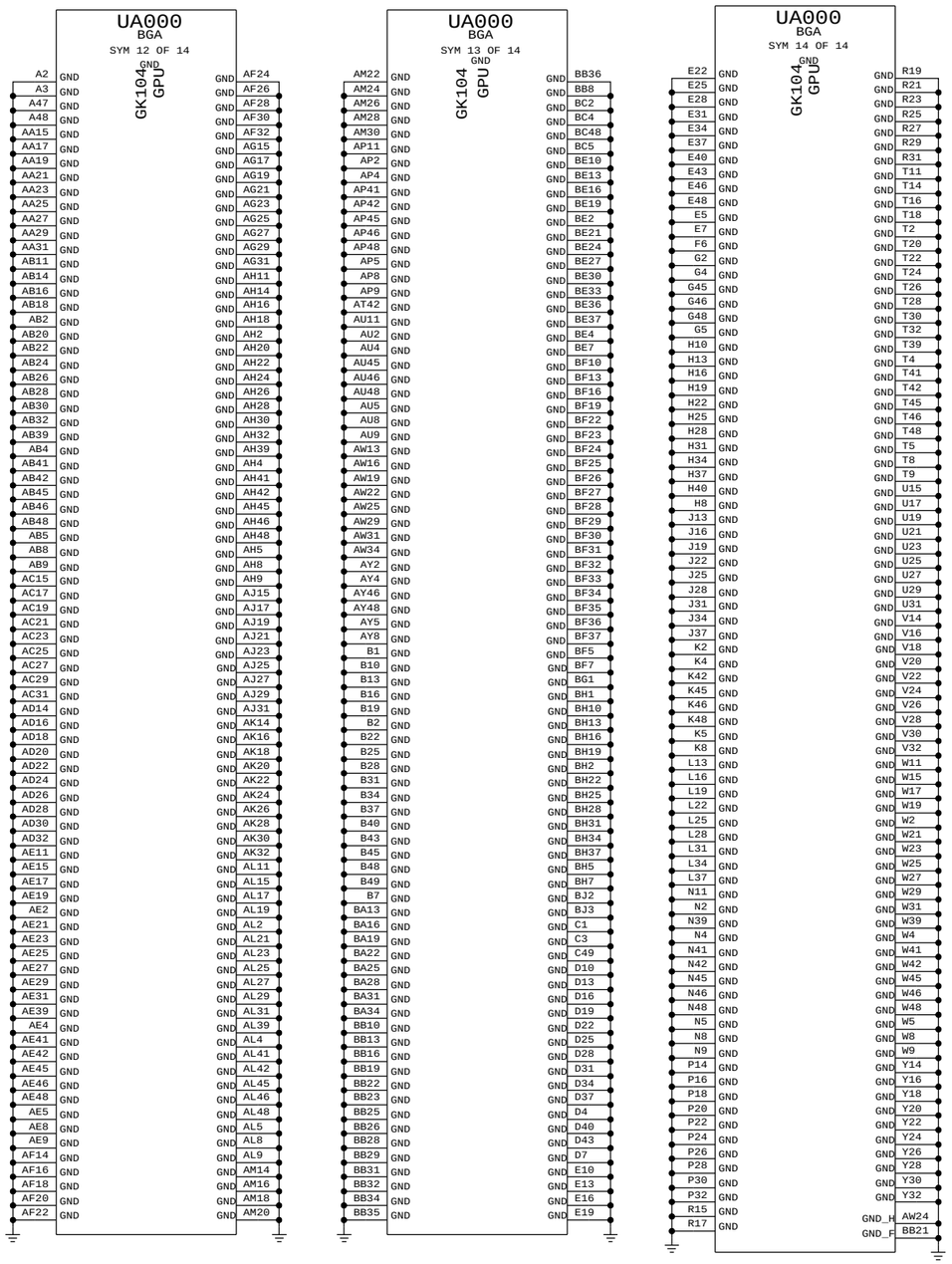



Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD

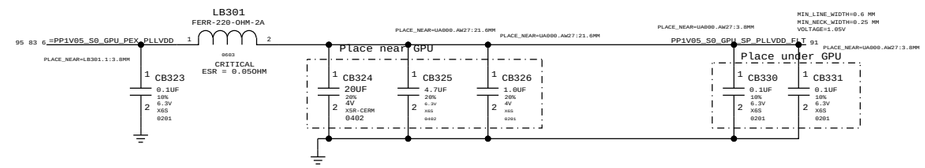
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

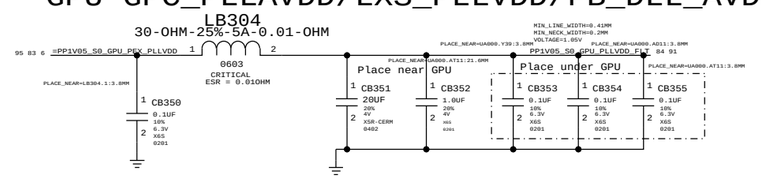
(NONE)

## GPU SP_PLLVDD/VID_PLLVDD 47MA+41MA

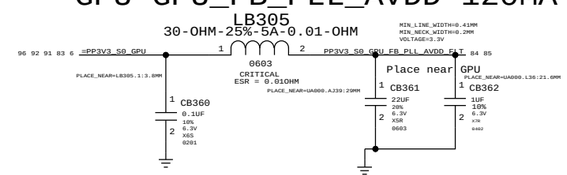



RDAR://11427653 D8: REPLACE 138S0682 WITH 138S0802

## GPU GPC_PLLAVDD/LXS_PLLVDD/FB_DLL_AVDD 52MA+39MA+50MA




## GPU GPU_FB_PLL_AVDD 120MA X 4 = 480MA




SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE

KEPLER PEX PWR/GNDS

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GPU CORE REG 1.1V/???A O/P= PPGPUCORE_S0_REG

GPU VCORE
VOUT = VCORE
PEAK = ???A
AVG = ???A

=PP5V_S0_VRD — RB418 2.2 5% 8W MF-LF 805 (MAX NECK LENGTH=3MM, MIN NECK WIDTH=0.3MM, MIN LINE WIDTH=0.6MM, VOLTAGE=5V)

PP5V_S0_GPU_VCORE_VCC — RB447, RB448, RB444, RB455 (NOSTUFF) 0 5% 1/10W MF-LF 402

VSNS_GPU_VDD — XWB420 (SM, OMIT) — VR_GPU_VSEN (VOLTAGE=1.1V, NET_PHYSICAL_TYPE=SNS_DIFF_PWR)

VSNS_GPU_VSS — XWB430 (SM, OMIT) — VR_GPU_RGND (VOLTAGE=0V, NET_PHYSICAL_TYPE=SNS_DIFF_PWR)

1.25 mOhm loadline

SIGNAL_MODEL=EMPTY

NOSTUFF CB401 0.0022UF 10% 50V CERM 402

CB402 0.0022UF 10% 50V CERM 402 — CB403 0.0022UF 10% 50V CERM 402 — AGND_GPU

CB404 47PF 5% 50V CERM 402 (VR_GPU_FB_R, VR_GPU_COMP_R)

RB401 8.06K 1% 1/16W MF-LF 402 — VR_GPU_COMP_RC — CB405 0.0047UF 10% 25V CERM 402

RB479 0 5% 1/16W MF-LF 402

RB402 1K 1% 1/16W MF-LF 402 — VR_VDF_R1 — RB403 287 1% 1/16W MF-LF 402

CB406 0.001UF 10% 50V X7R-CERM 0402 — VR_VDF_R2 — RB449 47.5 1% 1/16W MF-LF 402

NOSTUFF RB446 1M 5% 1/16W MF-LF 402 — RB404 0 5% 1/16W MF-LF 402

LOCAL 5V — CB407 1UF 10% 10V X6S-CERM 0402 — AGND_GPU

PP5V_S0_GPU_VCORE_VCC

VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.

RB400 1.02K 1% 1/10W MF-LF 402 — NOSTUFF RB405 20.0K 1% 1/10W MF-LF 402 — NOSTUFF RB498 0 5% 1/10W MF-LF 402 — RB477 100K 1% 1/10W MF-LF 402

LAYOUT: PLACE RTB401 NEAR HOT SPOT

RTB401 6.8K 0603 — CB480 0.1UF 10% 10V CERM 402

RB406 0 5% 1/10W MF-LF 402 — NOSTUFF RB407 21K 1% 1/10W MF-LF 402 — RB408 75K 1% 1/10W MF-LF 402 — NOSTUFF RB409 100K 1% 1/10W MF-LF 402

CB410 0.0033UF 10% 50V X7R-CERM 0402 — RB410 2.15K 1% 1/10W MF-LF 402 — AGND_GPU

=PP5V_S0_VRD — RB411 10K 0.1% 1/10W MF-LF 0402

PP5V_S0_GPU_VCORE_VCC

=PP3V3_S0_VRD

=PP3V3_S0_GPU — RB412 2.0K 5% 1/10W MF-LF 402

RB499 10K 0.1% 1/10W MF-LF 0402 — PM_PGOOD_REG_GPUCORE_S0

RB414 49.9K 1% 1/10W MF-LF 402 — RB415 49.9K 1% 1/10W MF-LF 402

GPU_PSI_L

VR_GPU_IMON — RB445 0 5% 1/10W MF-LF 402

RB417 10K 1% 1/10W MF-LF 402 — CB412 0.022UF 10% 16V X5R-X7R-CERM 0402 — RB416 0 5% 1/10W MF-LF 402 (VR_GPU_IOUT_PD)

DEFAULT: 0.9000V STEP: 12.5MV

=PP3V3_S0_GPU — NOSTUFF RB478 1K 1% 1/10W MF-LF 402 — NOSTUFF RB470 1K — NOSTUFF RB471 1K — NOSTUFF RB472 1K — NOSTUFF RB473 1K — RB474 1K — RB475 1K — NOSTUFF RB476 1K

REG_GPUCORE_VID7
REG_GPUCORE_VID6
REG_GPUCORE_VID5
REG_GPUCORE_VID4
REG_GPUCORE_VID3
REG_GPUCORE_VID2
REG_GPUCORE_VID1
REG_GPUCORE_VID0

NOSTUFF RB495 1K — RB496 1K — RB497 1K — NOSTUFF RB480 1K — NOSTUFF RB481 1K — NOSTUFF RB482 1K — RB485 1K — RB483 1K

NEED TO FIGURE OUT SEQUENCING FOR ENABLE

UB400 ISL6334D QFN (VCC CRITICAL SYM_VER_2)

| Pin | Signal |
|---|---|
| 13 | COMP |
| 14 | FB |
| 15 | VDIFF |
| 17 | VSEN |
| 16 | RGND |
| 18 | TCOMP |
| 9 | OFS |
| 34 | FS |
| 35 | SS |
| 11 | DAC |
| 12 | REF |
| 39 | TM |
| 33 | EN_VTT |
| 36 | VR_RDY |
| 7 | VID0 |
| 6 | VID1 |
| 5 | VID2 |
| 4 | VID3 |
| 3 | VID4 |
| 2 | VID5 |
| 1 | VID6 |
| 40 | VID7 |
| 8 | PSI* |
| 10 | IMON |
| 37 | H_CPURST_N |
| 38 | VR_HOT |
| 32 | EN_PWR |
| 41 | THRM PAD |
| 26 | PWM1 |
| 28 | ISEN1+ |
| 27 | ISEN1- |
| 20 | PWM2 |
| 22 | ISEN2+ |
| 21 | ISEN2- |
| 31 | PWM3 |
| 29 | ISEN3+ |
| 30 | ISEN3- |
| 25 | PWM4 |
| 23 | ISEN4+ |
| 24 | ISEN4- |
| 19 | |

VR_GPU_TCOMP, VR_GPU_OFS, VR_GPU_FS, VR_GPU_SS, VR_GPU_DAC, VR_GPU_REF, VR_GPU_TM, VR_GPU_EN_VTT, VR_GPU_IMON_R, VR_GPU_FAN, VR_GPU_VRDHOT, VR_GPU_VDIFF, VR_GPU_COMP, VR_GPU_FB

OMIT XWB401 SM — AGND_GPU (MAX NECK LENGTH=3MM, MIN NECK WIDTH=0.3MM, MIN LINE WIDTH=0.6MM, VOLTAGE=0V)

RB484 0 5% 1/10W MF-LF 402 — PM_EN_REG_GPUCORE_S0 — NOSTUFF CB409 0.01UF 10% 16V X7R-CERM 0402

VR_GPU_PWM1_R, VR_GPU_PWM2_R, VR_GPU_PWM3_R, VR_GPU_PWM4_R

RB434 0 5% 1/10W MF-LF 402 — REG_PWM_GPUCORE_1

RB431 178 1% 1/10W MF-LF 402 (VR_GPU_ISNS1_RR_2) — RB432 0 5% 1/10W MF-LF 402

NOSTUFF CB430 15PF 1% 50V C0G 402 — CB431 150PF 5% 50V CERM 402 — CB432 0.1UF 10% 16V X7R-CERM 0402 — CB433 220PF 5% 25V C0G-CERM 0402

REG_ISEN_GCORE_1_P — REG_ISEN_GCORE_1_N (DIFFERENTIAL_PAIR=REG_ISEN_GCORE_1)

RB433 1.02K 1% 1/10W MF-LF 402

VR_GPU_ISNS1_R_P, VR_GPU_ISNS1_R_N

RB440 0 5% 1/10W MF-LF 402 — REG_PWM_GPUCORE_2

RB441 178 1% 1/10W MF-LF 402 (VR_GPU_ISNS2_RR_2) — RB442 0 5% 1/10W MF-LF 402

NOSTUFF CB440 15PF 1% 50V C0G 402 — CB441 150PF 5% 50V CERM 402 — CB442 0.1UF 10% 16V X7R-CERM 0402 — CB443 220PF 5% 25V C0G-CERM 0402

REG_ISEN_GCORE_2_P — REG_ISEN_GCORE_2_N (DIFFERENTIAL_PAIR=REG_ISEN_GCORE_2)

RB443 1.02K 1% 1/10W MF-LF 402

VR_GPU_ISNS2_R_P, VR_GPU_ISNS2_R_N, VR_GPU_ISNS3_R_P, VR_GPU_ISNS3_R_N, VR_GPU_ISNS4_R_P, VR_GPU_ISNS4_R_N

RB450 0 5% 1/10W MF-LF 402 — REG_PWM_GPUCORE_3

RB451 178 1% 1/10W MF-LF 402 (VR_GPU_ISNS3_RR_2) — RB452 0 5% 1/10W MF-LF 402

NOSTUFF CB450 15PF 1% 50V C0G 402 — CB451 150PF 5% 50V CERM 402 — CB452 0.1UF 10% 16V X7R-CERM 0402 — CB453 220PF 5% 25V C0G-CERM 0402

REG_ISEN_GCORE_3_P — REG_ISEN_GCORE_3_N (DIFFERENTIAL_PAIR=REG_ISEN_GCORE_3)

RB453 1.02K 1% 1/10W MF-LF 402

RB438 0 5% 1/10W MF-LF 402 — REG_PWM_GPUCORE_4

RB439 178 1% 1/10W MF-LF 402 (VR_GPU_ISNS4_RR_2) — RB420 0 5% 1/10W MF-LF 402

NOSTUFF CB460 15PF 1% 50V C0G 402 — CB461 150PF 5% 50V CERM 402 — CB462 0.1UF 10% 16V X7R-CERM 0402 — CB463 220PF 5% 25V C0G-CERM 0402

REG_ISEN_GCORE_4_P — REG_ISEN_GCORE_4_N (DIFFERENTIAL_PAIR=REG_ISEN_GCORE_4)

RB421 1.02K 1% 1/10W MF-LF 402

AGND_GPU

=PP12V_S0_REG_GPUCORE (IMAX = 10.5A) — LB400 0.36UH-28A-0.66MOHM SDP110808MR36MF-TH 152-0110 — PP12V_S0_GPUCORE_FLT

GPU CORE INPUT Filtering

| | |
|---|---|
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| PAGE TITLE: VReg GPU Core Phases | |
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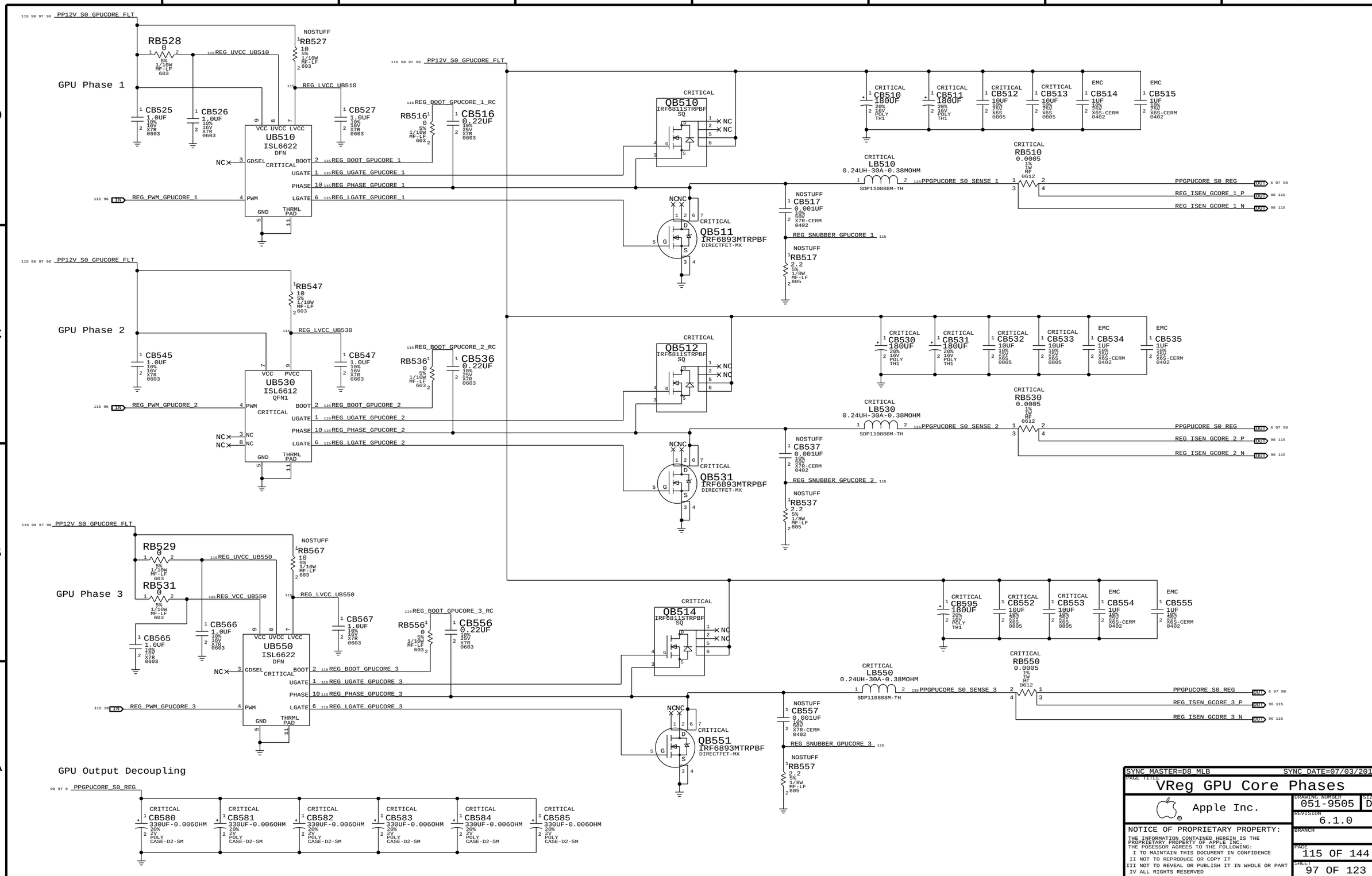


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# VReg GPU Core Phases

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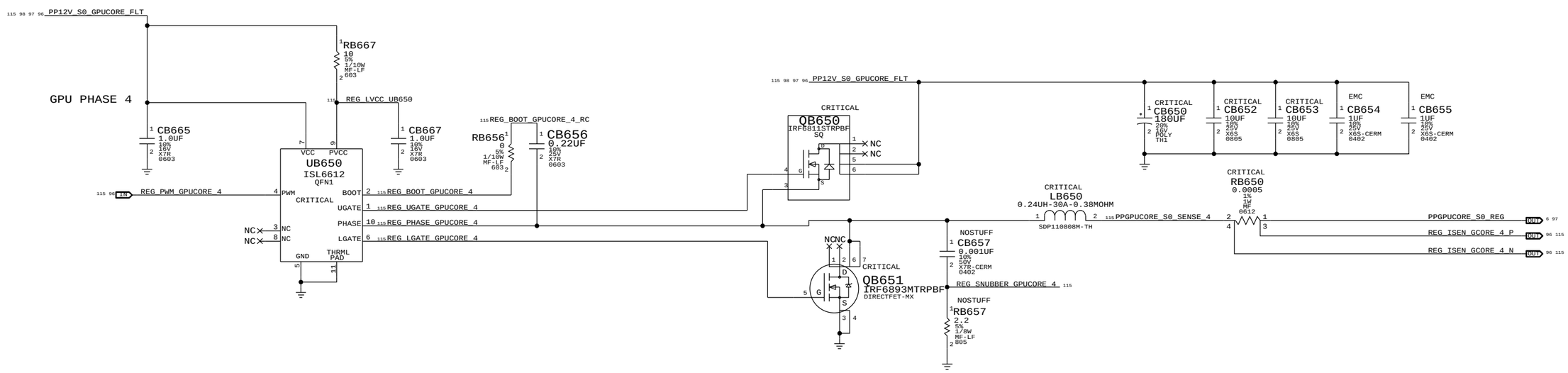


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# VREG GPU CORE PHASE 4

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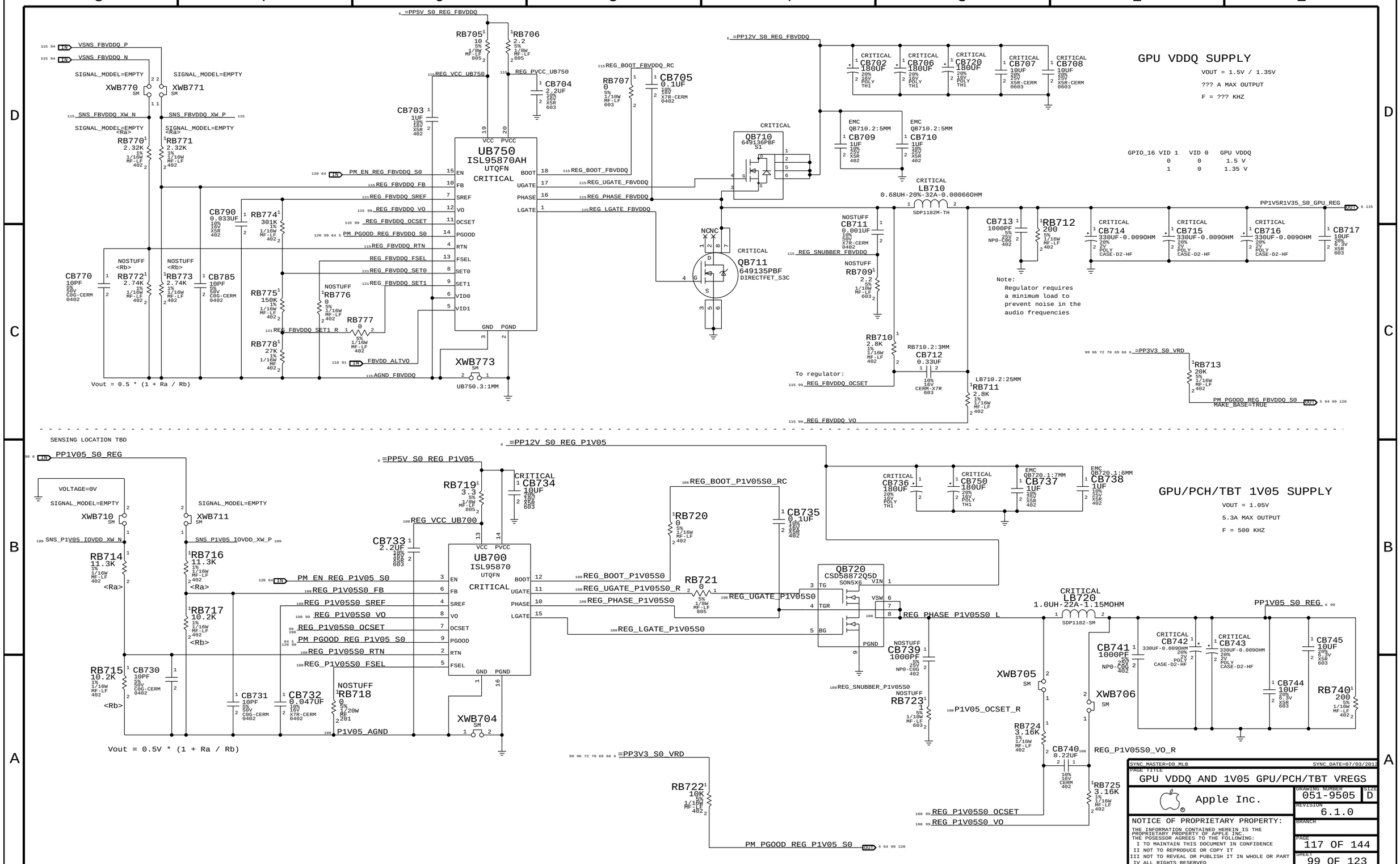
GPU VDDQ SUPPLY
VOUT = 1.5V / 1.35V
??? A MAX OUTPUT
F = ??? KHZ
GPIO_16 VID 1 VID 0 GPU VDDQ
0 0 1.5 V
1 0 1.35 V
UB750
ISL95870AH
UTQFN
CRITICAL
Vout = 0.5 * (1 + Ra / Rb)
Note:
Regulator requires
a minimum load to
prevent noise in the
audio frequencies
To regulator:
GPU/PCH/TBT 1V05 SUPPLY
VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ
UB700
ISL95870
UTQFN
CRITICAL
Vout = 0.5V * (1 + Ra / Rb)
SENSING LOCATION TBD
GPU VDDQ AND 1V05 GPU/PCH/TBT VREGS
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# D8 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

| BOARD LAYERS | BOARD AREAS | BOARD UNITS (MIL or MM) | ALLEGRO VERSION |
|---|---|---|---|
| TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM | NO_TYPE,BGA,BGA_TBT | MM | 16.2 |

## General Physical Rule Definitions

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DEFAULT | * | Y | 0.1 MM | =50_OHM_SE | 10 MM | 0 MM | 0 MM |
| STANDARD | * | Y | =DEFAULT | =DEFAULT | 10 MM | =DEFAULT | =DEFAULT |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 34_OHM_SE | * | Y | 0.185 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 34_OHM_SE | ISL5,ISL8 | Y | 0.205 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 34_OHM_SE | TOP,BOTTOM | Y | 0.220 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 39_OHM_SE | * | Y | 0.150 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 39_OHM_SE | ISL5,ISL8 | Y | 0.165 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 39_OHM_SE | TOP,BOTTOM | Y | 0.175 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 42_OHM_SE | * | Y | 0.130 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 42_OHM_SE | ISL5,ISL8 | Y | 0.145 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 42_OHM_SE | TOP,BOTTOM | Y | 0.155 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 45_OHM_SE | * | Y | 0.115 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 45_OHM_SE | ISL5,ISL8 | Y | 0.126 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 45_OHM_SE | TOP,BOTTOM | Y | 0.135 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 50_OHM_SE | * | Y | 0.090 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 50_OHM_SE | ISL5,ISL8 | Y | 0.100 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |
| 50_OHM_SE | TOP,BOTTOM | Y | 0.105 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 55_OHM_SE | * | Y | 0.075 MM | 0.075 MM | =STANDARD | =STANDARD | =STANDARD |
| 55_OHM_SE | ISL5,ISL8 | Y | 0.080 MM | 0.080 MM | =STANDARD | =STANDARD | =STANDARD |
| 55_OHM_SE | TOP,BOTTOM | Y | 0.085 MM | 0.085 MM | =STANDARD | =STANDARD | =STANDARD |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 68_OHM_DIFF | * | Y | 0.171 MM | 0.085 MM | =STANDARD | 0.130 MM | 0.1 MM |
| 68_OHM_DIFF | TOP,BOTTOM | Y | 0.185 MM | 0.085 MM | =STANDARD | 0.150 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 80_OHM_DIFF | * | Y | 0.136 MM | 0.085 MM | =STANDARD | 0.190 MM | 0.1 MM |
| 80_OHM_DIFF | TOP,BOTTOM | Y | 0.141 MM | 0.085 MM | =STANDARD | 0.185 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 85_OHM_DIFF | * | Y | 0.121 MM | 0.085 MM | =STANDARD | 0.190 MM | 0.1 MM |
| 85_OHM_DIFF | TOP,BOTTOM | Y | 0.125 MM | 0.085 MM | =STANDARD | 0.190 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 90_OHM_DIFF | * | Y | 0.109 MM | 0.085 MM | =STANDARD | 0.200 MM | 0.1 MM |
| 90_OHM_DIFF | TOP,BOTTOM | Y | 0.111 MM | 0.085 MM | =STANDARD | 0.200 MM | 0.1 MM |

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 100_OHM_DIFF | * | Y | 0.086 MM | 0.085 MM | =STANDARD | 0.200 MM | 0.1 MM |
| 100_OHM_DIFF | TOP,BOTTOM | Y | 0.090 MM | 0.085 MM | =STANDARD | 0.230 MM | 0.1 MM |

## Compensation Physical Rule Definition

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| COMP_SE | * | Y | 0.305 MM | 0.105 MM | 3 MM | =STANDARD | =STANDARD |

NOTE: line width based on 12 mil recommendation
NOTE: neck width based on 4 mil recommendation

## General Spacing Definitions

Default

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DEFAULT | * | 0.1 MM | ? |
| STANDARD | * | =DEFAULT | ? |

Fixed and Dielectric

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| 1:1_SPACING | * | 0.1 MM | ? |
| 1X_DIELECTRIC | TOP,BOTTOM | 0.071 MM | ? |
| 1X_DIELECTRIC | ISL3,ISL10 | 0.101 MM | ? |
| 1X_DIELECTRIC | * | 0.076 MM | ? |

## Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

| | | | |
|---|---|---|---|
| Top | Signal | 0.5 oz (Cu plated) |
| | Prepreg | 0.071 MM |
| 2 | Plane | 1 oz |
| | Core | 0.101 MM |
| 3 | Signal | 0.5 oz |
| | Prepreg | 0.115 MM |
| 4 | Plane | 1 oz |
| | Core | 0.076 MM |
| 5 | Signal | 0.5 oz |
| | Prepreg | 0.380 MM |
| 6 | Plane | 1 oz |
| | Core | 0.076 MM |
| 7 | Plane | 1 oz |
| | Prepreg | 0.380 MM |
| 8 | Signal | 0.5 oz |
| | Core | 0.076 MM |
| 9 | Plane | 1 oz |
| | Prepreg | 0.115 MM |
| 10 | Signal | 0.5 oz |
| | Core | 0.101 MM |
| 11 | Plane | 1 oz |
| | Prepreg | 0.071 MM |
| Btm | Signal | 0.5 oz (Cu plated) |

BGA

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| BGA_P1MM | * | =STANDARD | ? |

Power and Common

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GND_ISO | * | =STANDARD | 8000 |
| GND_P2MM | * | =2:1_SPACING | 1000 |
| PWR_P2MM | * | =2:1_SPACING | 1100 |

GENERIC

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GENERIC_ISO | * | =1:1_SPACING | ? |
| PM_ISO | * | =1:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| PM | * | * | PM_ISO |
| PM | GND | * | DEFAULT |

## BGA Area Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| * | * | BGA | BGA_P1MM |

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PAGE TITLE
# D8 RULE DEFINITIONS

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# DDR3

## DDR3-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DDR_34S | * | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | =STANDARD | =STANDARD |
| DDR_34S | BOTTOM | =34_OHM_SE | =34_OHM_SE | =34_OHM_SE | 2.0 MM | =STANDARD | =STANDARD |
| DDR_39S | * | =39_OHM_SE | =39_OHM_SE | =39_OHM_SE | =39_OHM_SE | =STANDARD | =STANDARD |
| DDR_42S | * | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =STANDARD | =STANDARD |
| DDR_42S | BOTTOM | =42_OHM_SE | =55_OHM_SE | =55_OHM_SE | 2.0 MM | =STANDARD | =STANDARD |
| DDR_42S | ISL5,ISL8 | =42_OHM_SE | =55_OHM_SE | =55_OHM_SE | 2.0 MM | =STANDARD | =STANDARD |
| DDR_42S_D | * | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | =42_OHM_SE | 0.1016 MM | 0.1016 MM |
| DDR_42S_D | BOTTOM | =42_OHM_SE | =55_OHM_SE | =55_OHM_SE | 2.0 MM | 0.1016 MM | 0.1016 MM |
| DDR_42S_D | ISL5,ISL8 | =42_OHM_SE | =55_OHM_SE | =55_OHM_SE | 2.0 MM | 0.1016 MM | 0.1016 MM |
| DDR_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| DDR_68D | * | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF | =68_OHM_DIFF |

Minimum diff spacing is 4 mil
Table 3-5, Intel Doc# 473718

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| POWER_DDR_P4MM | * | Y | 0.400 MM | 0.100 MM | 3.0 MM | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| POWER_DDR_PHY | * | POWER_DDR_P4MM |
| DDR_CLK_PHY | * | DDR_68D |
| DDR_CTRL_PHY | * | DDR_39S |
| DDR_CMD_PHY | * | DDR_34S |
| DDR_DQ_PHY | * | DDR_42S |
| DDR_DQS_PHY | * | DDR_42S_D |

## DDR3-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DDR_CLK_ISO | TOP,BOTTOM | =5.5X_DIELECTRIC | ? |
| DDR_CLK_ISO | ISL3,ISL10 | =4.9X_DIELECTRIC | ? |
| DDR_CLK_ISO | * | =6.5X_DIELECTRIC | ? |
| DDR_CTRL_ISO | TOP,BOTTOM | =4.5X_DIELECTRIC | ? |
| DDR_CTRL_ISO | ISL3,ISL10 | =4.0X_DIELECTRIC | ? |
| DDR_CTRL_ISO | * | =5.3X_DIELECTRIC | ? |
| DDR_CTRL2CTRL | TOP,BOTTOM | =3.0X_DIELECTRIC | ? |
| DDR_CTRL2CTRL | ISL3,ISL10 | =2.6X_DIELECTRIC | ? |
| DDR_CTRL2CTRL | * | =3.5X_DIELECTRIC | ? |
| DDR_CMD_ISO | TOP,BOTTOM | =4.5X_DIELECTRIC | ? |
| DDR_CMD_ISO | ISL3,ISL10 | =4.0X_DIELECTRIC | ? |
| DDR_CMD_ISO | * | =5.3X_DIELECTRIC | ? |
| DDR_CMD2CMD | TOP,BOTTOM | =2.3X_DIELECTRIC | ? |
| DDR_CMD2CMD | ISL3,ISL10 | =2.0X_DIELECTRIC | ? |
| DDR_CMD2CMD | * | =2.7X_DIELECTRIC | ? |
| DDR_DATA_ISO | TOP,BOTTOM | =4.5X_DIELECTRIC | ? |
| DDR_DATA_ISO | ISL3,ISL10 | =4.0X_DIELECTRIC | ? |
| DDR_DATA_ISO | * | =5.3X_DIELECTRIC | ? |
| DDR_DQ2DQ | TOP,BOTTOM | =3.2X_DIELECTRIC | 900 |
| DDR_DQ2DQ | ISL3,ISL10 | =2.8X_DIELECTRIC | 900 |
| DDR_DQ2DQ | * | =3.8X_DIELECTRIC | 900 |
| DDR_DQ2DQS | TOP,BOTTOM | =3.7X_DIELECTRIC | ? |
| DDR_DQ2DQS | ISL3,ISL10 | =3.3X_DIELECTRIC | ? |
| DDR_DQ2DQS | * | =4.4X_DIELECTRIC | ? |
| DDR_BL2BL | TOP,BOTTOM | =4.5X_DIELECTRIC | ? |
| DDR_BL2BL | ISL3,ISL10 | =4.0X_DIELECTRIC | ? |
| DDR_BL2BL | * | =5.3X_DIELECTRIC | ? |
| DDR_CH2CH | TOP,BOTTOM | =9.1X_DIELECTRIC | ? |
| DDR_CH2CH | ISL3,ISL10 | =8.2X_DIELECTRIC | ? |
| DDR_CH2CH | * | =10.9X_DIELECTRIC | ? |
| CMD2DATA_ISO | TOP,BOTTOM | =7X_DIELECTRIC | ? |
| CMD2DATA_ISO | ISL3,ISL10 | =5X_DIELECTRIC | ? |
| CMD2DATA_ISO | * | =5X_DIELECTRIC | ? |

## DDR3 Power-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| POWER_DDR_ISO | * | =4.3X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| POWER_DDR | * | * | POWER_DDR_ISO |

## Constraints

### Clocks: CK[3:0], CK#[3:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DDR_CLK | * | * | DDR_CLK_ISO |

### Control: CS#[3:0], CKE[3:0], ODT[3:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DDR_CTRL | * | * | DDR_CTRL_ISO |
| DDR_CTRL | DDR_CTRL | * | DDR_CTRL2CTRL |

### Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DDR_CMD | * | * | DDR_CMD_ISO |
| DDR_CMD | DDR_CMD | * | DDR_CMD2CMD |
| DDR_CMD | DDR_A_DQ_BYTE* | * | CMD2DATA_ISO |
| DDR_CMD | DDR_A_DQS* | * | CMD2DATA_ISO |
| DDR_CMD | DDR_B_DQ_BYTE* | * | CMD2DATA_ISO |
| DDR_CMD | DDR_B_DQS* | * | CMD2DATA_ISO |

### Data: DQS[7:0], DQS#[7:0], DQ[63:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET | |
|---|---|---|---|---|
| DDR_A_DQ_BYTE* | * | * | DDR_DATA_ISO | |
| DDR_A_DQS* | * | * | DDR_DATA_ISO | |
| DDR_B_DQ_BYTE* | * | * | DDR_DATA_ISO | |
| DDR_B_DQS* | * | * | DDR_DATA_ISO | |
| DDR_*_DQ_BYTE* | =SAME | * | DDR_DQ2DQ | See Note (3) |
| DDR_A_DQ_BYTE* | DDR_A_DQS* | * | DDR_DQ2DQS | See Note (1) |
| DDR_A_DQ_BYTE* | DDR_A_DQ_BYTE* | * | DDR_BL2BL | See Note (3) |
| DDR_B_DQ_BYTE* | DDR_B_DQS* | * | DDR_DQ2DQS | See Note (1) |
| DDR_B_DQ_BYTE* | DDR_B_DQ_BYTE* | * | DDR_BL2BL | |
| DDR_A_* | DDR_B_* | * | DDR_CH2CH | See Note (2) |

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

## DDR3

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| **Channel A** | | | | |
| I17 DDR_A_CLK0 | DDR_CLK_PHY | DDR_CLK | MEM_A_CLK_P<1..0> | 12 29 |
| I17 DDR_A_CLK0 | DDR_CLK_PHY | DDR_CLK | MEM_A_CLK_N<1..0> | 12 29 |
| I25 DDR_A_CLK1 | DDR_CLK_PHY | DDR_CLK | MEM_A_CLK_P<3..2> | 12 30 |
| I25 DDR_A_CLK1 | DDR_CLK_PHY | DDR_CLK | MEM_A_CLK_N<3..2> | 12 30 |
| I18 DDR_A_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_CKE<1..0> | 12 29 |
| I18 DDR_A_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_CS_L<1..0> | 12 29 |
| I18 DDR_A_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_ODT<1..0> | 12 29 |
| I24 DDR_A_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_CKE<3..2> | 12 30 |
| I24 DDR_A_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_CS_L<3..2> | 12 30 |
| I24 DDR_A_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_A_ODT<3..2> | 12 30 |
| I18 DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_A<15..0> | 12 29 30 |
| I18 DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_BA<2..0> | 12 29 30 |
| I18 DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_RAS_L | 12 29 30 |
| I18 DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_CAS_L | 12 29 30 |
| I18 DDR_A_CMD | DDR_CMD_PHY | DDR_CMD | MEM_A_WE_L | 12 29 30 |
| I19 DDR_A_DQ_BYTE0 | DDR_DQ_PHY | DDR_A_DQ_BYTE0 | MEM_A_DQ<7..0> | 12 33 |
| I16 DDR_A_DQ_BYTE1 | DDR_DQ_PHY | DDR_A_DQ_BYTE1 | MEM_A_DQ<15..8> | 12 33 |
| I19 DDR_A_DQ_BYTE2 | DDR_DQ_PHY | DDR_A_DQ_BYTE2 | MEM_A_DQ<23..16> | 12 33 |
| I19 DDR_A_DQ_BYTE3 | DDR_DQ_PHY | DDR_A_DQ_BYTE3 | MEM_A_DQ<31..24> | 12 33 |
| I19 DDR_A_DQ_BYTE4 | DDR_DQ_PHY | DDR_A_DQ_BYTE4 | MEM_A_DQ<39..32> | 12 33 |
| I19 DDR_A_DQ_BYTE5 | DDR_DQ_PHY | DDR_A_DQ_BYTE5 | MEM_A_DQ<47..40> | 12 33 |
| I19 DDR_A_DQ_BYTE6 | DDR_DQ_PHY | DDR_A_DQ_BYTE6 | MEM_A_DQ<55..48> | 12 33 |
| I19 DDR_A_DQ_BYTE7 | DDR_DQ_PHY | DDR_A_DQ_BYTE7 | MEM_A_DQ<63..56> | 12 33 |
| I19 DDR_A_DQS0 | DDR_DQS_PHY | DDR_A_DQS0 | MEM_A_DQS_P<0> | 12 33 |
| I19 DDR_A_DQS0 | DDR_DQS_PHY | DDR_A_DQS0 | MEM_A_DQS_N<0> | 12 33 |
| I19 DDR_A_DQS1 | DDR_DQS_PHY | DDR_A_DQS1 | MEM_A_DQS_P<1> | 12 33 |
| I19 DDR_A_DQS1 | DDR_DQS_PHY | DDR_A_DQS1 | MEM_A_DQS_N<1> | 12 33 |
| I20 DDR_A_DQS2 | DDR_DQS_PHY | DDR_A_DQS2 | MEM_A_DQS_P<2> | 12 33 |
| I20 DDR_A_DQS2 | DDR_DQS_PHY | DDR_A_DQS2 | MEM_A_DQS_N<2> | 12 33 |
| I20 DDR_A_DQS3 | DDR_DQS_PHY | DDR_A_DQS3 | MEM_A_DQS_P<3> | 12 33 |
| I20 DDR_A_DQS3 | DDR_DQS_PHY | DDR_A_DQS3 | MEM_A_DQS_N<3> | 12 33 |
| I20 DDR_A_DQS4 | DDR_DQS_PHY | DDR_A_DQS4 | MEM_A_DQS_P<4> | 12 33 |
| I20 DDR_A_DQS4 | DDR_DQS_PHY | DDR_A_DQS4 | MEM_A_DQS_N<4> | 12 33 |
| I20 DDR_A_DQS5 | DDR_DQS_PHY | DDR_A_DQS5 | MEM_A_DQS_P<5> | 12 33 |
| I20 DDR_A_DQS5 | DDR_DQS_PHY | DDR_A_DQS5 | MEM_A_DQS_N<5> | 12 33 |
| I20 DDR_A_DQS6 | DDR_DQS_PHY | DDR_A_DQS6 | MEM_A_DQS_P<6> | 12 33 |
| I20 DDR_A_DQS6 | DDR_DQS_PHY | DDR_A_DQS6 | MEM_A_DQS_N<6> | 12 33 |
| I21 DDR_A_DQS7 | DDR_DQS_PHY | DDR_A_DQS7 | MEM_A_DQS_P<7> | 12 33 |
| I21 DDR_A_DQS7 | DDR_DQS_PHY | DDR_A_DQS7 | MEM_A_DQS_N<7> | 12 33 |
| **Channel B** | | | | |
| I21 DDR_B_CLK0 | DDR_CLK_PHY | DDR_CLK | MEM_B_CLK_P<1..0> | 12 31 |
| I21 DDR_B_CLK0 | DDR_CLK_PHY | DDR_CLK | MEM_B_CLK_N<1..0> | 12 31 |
| I25 DDR_B_CLK1 | DDR_CLK_PHY | DDR_CLK | MEM_B_CLK_P<3..2> | 12 32 |
| I25 DDR_B_CLK1 | DDR_CLK_PHY | DDR_CLK | MEM_B_CLK_N<3..2> | 12 32 |
| I21 DDR_B_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_CKE<1..0> | 12 31 |
| I21 DDR_B_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_CS_L<1..0> | 12 31 |
| I21 DDR_B_CTRL0 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_ODT<1..0> | 12 31 |
| I25 DDR_B_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_CKE<3..2> | 12 32 |
| I25 DDR_B_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_CS_L<3..2> | 12 32 |
| I25 DDR_B_CTRL1 | DDR_CTRL_PHY | DDR_CTRL | MEM_B_ODT<3..2> | 12 32 |
| I21 DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_A<15..0> | 12 31 32 |
| I21 DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_BA<2..0> | 12 31 32 |
| I21 DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_RAS_L | 12 31 32 |
| I22 DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_CAS_L | 12 31 32 |
| I22 DDR_B_CMD | DDR_CMD_PHY | DDR_CMD | MEM_B_WE_L | 12 31 32 |
| I22 DDR_B_DQ_BYTE0 | DDR_DQ_PHY | DDR_B_DQ_BYTE0 | MEM_B_DQ<7..0> | 12 33 |
| I22 DDR_B_DQ_BYTE1 | DDR_DQ_PHY | DDR_B_DQ_BYTE1 | MEM_B_DQ<15..8> | 12 33 |
| I22 DDR_B_DQ_BYTE2 | DDR_DQ_PHY | DDR_B_DQ_BYTE2 | MEM_B_DQ<23..16> | 12 33 |
| I22 DDR_B_DQ_BYTE3 | DDR_DQ_PHY | DDR_B_DQ_BYTE3 | MEM_B_DQ<31..24> | 12 33 |
| I22 DDR_B_DQ_BYTE4 | DDR_DQ_PHY | DDR_B_DQ_BYTE4 | MEM_B_DQ<39..32> | 12 33 |
| I22 DDR_B_DQ_BYTE5 | DDR_DQ_PHY | DDR_B_DQ_BYTE5 | MEM_B_DQ<47..40> | 12 33 |
| I22 DDR_B_DQ_BYTE6 | DDR_DQ_PHY | DDR_B_DQ_BYTE6 | MEM_B_DQ<55..48> | 12 33 |
| I22 DDR_B_DQ_BYTE7 | DDR_DQ_PHY | DDR_B_DQ_BYTE7 | MEM_B_DQ<63..56> | 12 33 |
| I23 DDR_B_DQS0 | DDR_DQS_PHY | DDR_B_DQS0 | MEM_B_DQS_P<0> | 12 33 |
| I23 DDR_B_DQS0 | DDR_DQS_PHY | DDR_B_DQS0 | MEM_B_DQS_N<0> | 12 33 |
| I23 DDR_B_DQS1 | DDR_DQS_PHY | DDR_B_DQS1 | MEM_B_DQS_P<1> | 12 33 |
| I23 DDR_B_DQS1 | DDR_DQS_PHY | DDR_B_DQS1 | MEM_B_DQS_N<1> | 12 33 |
| I23 DDR_B_DQS2 | DDR_DQS_PHY | DDR_B_DQS2 | MEM_B_DQS_P<2> | 12 33 |
| I23 DDR_B_DQS2 | DDR_DQS_PHY | DDR_B_DQS2 | MEM_B_DQS_N<2> | 12 33 |
| I23 DDR_B_DQS3 | DDR_DQS_PHY | DDR_B_DQS3 | MEM_B_DQS_P<3> | 12 33 |
| I23 DDR_B_DQS3 | DDR_DQS_PHY | DDR_B_DQS3 | MEM_B_DQS_N<3> | 12 33 |
| I23 DDR_B_DQS4 | DDR_DQS_PHY | DDR_B_DQS4 | MEM_B_DQS_P<4> | 12 33 |
| I23 DDR_B_DQS4 | DDR_DQS_PHY | DDR_B_DQS4 | MEM_B_DQS_N<4> | 12 33 |
| I24 DDR_B_DQS5 | DDR_DQS_PHY | DDR_B_DQS5 | MEM_B_DQS_P<5> | 12 33 |
| I24 DDR_B_DQS5 | DDR_DQS_PHY | DDR_B_DQS5 | MEM_B_DQS_N<5> | 12 33 |
| I24 DDR_B_DQS6 | DDR_DQS_PHY | DDR_B_DQS6 | MEM_B_DQS_P<6> | 12 33 |
| I24 DDR_B_DQS6 | DDR_DQS_PHY | DDR_B_DQS6 | MEM_B_DQS_N<6> | 12 33 |
| I24 DDR_B_DQS7 | DDR_DQS_PHY | DDR_B_DQS7 | MEM_B_DQS_P<7> | 12 33 |
| I24 DDR_B_DQS7 | DDR_DQS_PHY | DDR_B_DQS7 | MEM_B_DQS_N<7> | 12 33 |
| **Reset** | | | | |
| I24 | DDR_50S | CPU | MEM_RESET_L | 28 29 30 31 32 |

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
DDR3 Constraints

Apple Inc.

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# PCI EXPRESS

## PCIe-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCIE_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| PCIE_80D | * | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF |
| PCIE_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| PCIE_PHY | * | PCIE_80D |
| CLK_PCIE_PHY | * | PCIE_90D |
| COMP_PCIE_PHY | * | COMP_SE |

## PCIe-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PCIE_ISO | TOP,BOTTOM | =5X_DIELECTRIC | ? |
| PCIE_ISO | * | =4X_DIELECTRIC | ? |
| CLK_PCIE_ISO | * | =5:1_SPACING | ? |
| COMP_PCIE_ISO | * | =4:1_SPACING | ? |

## PCIe Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

| Section | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 4.2.1 | 80 | 85 | 16 | 15.75 | PCIe Gen2, PCIe Gen3, DMI |

## PCIe and DMI Compensation Rules (mils)

| Table | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 4-5 | 50 | 50 | 15 | 15.75 | PCIe. Impedance inferred from Table 4-7. |
| 4-7 | 50 | 50 | 8 | 15.75 | DMI. Numbers based on Intel stack-up. |

## Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| PCIE | * | * | PCIE_ISO |
| CLK_PCIE | * | * | CLK_PCIE_ISO |
| COMP_PCIE | * | * | COMP_PCIE_ISO |

## PCIe (PCH)

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| x1 AirPort | | | | | |
| 1659 PCIE_GEN2_R2D_CONN_AP | PCIE_PHY | PCIE | PCIE_AP_R2D_P | NO_TEST=TRUE | 35 |
| 1660 PCIE_GEN2_R2D_CONN_AP | PCIE_PHY | PCIE | PCIE_AP_R2D_N | NO_TEST=TRUE | 35 |
| 1661 | PCIE_PHY | PCIE | PCIE_AP_R2D_C_P | NO_TEST=TRUE | 18 35 |
| 1662 | PCIE_PHY | PCIE | PCIE_AP_R2D_C_N | NO_TEST=TRUE | 18 35 |
| 1663 PCIE_GEN2_D2R_CONN_AP | PCIE_PHY | PCIE | PCIE_AP_D2R_P | NO_TEST=TRUE | 18 35 |
| 1664 PCIE_GEN2_D2R_CONN_AP | PCIE_PHY | PCIE | PCIE_AP_D2R_N | NO_TEST=TRUE | 18 35 |
| 1667 PCIE_REF_CLK_CONN | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_AP_P | | 18 35 |
| 1668 PCIE_REF_CLK_CONN | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_AP_N | | 18 35 |
| x1 Caesar IV | | | | | |
| 1637 PCIE_GEN2_R2D | PCIE_PHY | PCIE | PCIE_ENET_R2D_P | NO_TEST=TRUE | 39 |
| 1638 PCIE_GEN2_R2D | PCIE_PHY | PCIE | PCIE_ENET_R2D_N | NO_TEST=TRUE | 39 |
| 1639 | PCIE_PHY | PCIE | PCIE_ENET_R2D_C_P | NO_TEST=TRUE | 18 39 |
| 1640 | PCIE_PHY | PCIE | PCIE_ENET_R2D_C_N | NO_TEST=TRUE | 18 39 |
| 1633 PCIE_GEN2_D2R | PCIE_PHY | PCIE | PCIE_ENET_D2R_P | NO_TEST=TRUE | 18 39 |
| 1634 PCIE_GEN2_D2R | PCIE_PHY | PCIE | PCIE_ENET_D2R_N | NO_TEST=TRUE | 18 39 |
| 1635 | PCIE_PHY | PCIE | PCIE_ENET_D2R_C_P | NO_TEST=TRUE | 39 |
| 1636 | PCIE_PHY | PCIE | PCIE_ENET_D2R_C_N | NO_TEST=TRUE | 39 |
| 1631 PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_ENET_P | | 18 39 |
| 1632 PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_ENET_N | | 18 39 |

## PCIE (PCH - TBT)

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| x4 Thunderbolt | | | | | |
| 1677 PCIE_GEN2_R2D_PINV | PCIE_PHY | PCIE | PCIE_TBT_R2D_P<2..0> | NO_TEST=TRUE | 36 |
| 1678 PCIE_GEN2_R2D_PINV | PCIE_PHY | PCIE | PCIE_TBT_R2D_N<2..0> | NO_TEST=TRUE | 36 |
| 1679 PCIE_GEN2_R2D | PCIE_PHY | PCIE | PCIE_TBT_R2D_P<3> | NO_TEST=TRUE | 36 |
| 1680 PCIE_GEN2_R2D | PCIE_PHY | PCIE | PCIE_TBT_R2D_N<3> | NO_TEST=TRUE | 36 |
| 1673 | PCIE_PHY | PCIE | PCIE_TBT_R2D_C_P<3..0> | NO_TEST=TRUE | 18 36 |
| 1674 | PCIE_PHY | PCIE | PCIE_TBT_R2D_C_N<3..0> | NO_TEST=TRUE | 18 36 |
| 1675 | PCIE_PHY | PCIE | PCIE_TBT_D2R_P<3..0> | NO_TEST=TRUE | 18 36 |
| 1676 | PCIE_PHY | PCIE | PCIE_TBT_D2R_N<3..0> | NO_TEST=TRUE | 18 36 |
| 1677 PCIE_GEN2_D2R_PINV | PCIE_PHY | PCIE | PCIE_TBT_D2R_C_P<1..0> | NO_TEST=TRUE | 36 |
| 1678 PCIE_GEN2_D2R_PINV | PCIE_PHY | PCIE | PCIE_TBT_D2R_C_N<1..0> | NO_TEST=TRUE | 36 |
| 1679 PCIE_GEN2_D2R | PCIE_PHY | PCIE | PCIE_TBT_D2R_C_P<2> | NO_TEST=TRUE | 36 |
| 1680 PCIE_GEN2_D2R | PCIE_PHY | PCIE | PCIE_TBT_D2R_C_N<2> | NO_TEST=TRUE | 36 |
| 1673 PCIE_GEN2_D2R_PINV | PCIE_PHY | PCIE | PCIE_TBT_D2R_C_P<3> | NO_TEST=TRUE | 36 |
| 1674 PCIE_GEN2_D2R_PINV | PCIE_PHY | PCIE | PCIE_TBT_D2R_C_N<3> | NO_TEST=TRUE | 36 |
| 1671 PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_TBT_P | | 18 36 |
| 1672 PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PCIE_CLK100M_TBT_N | | 18 36 |

## PCIe (CPU)

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| x16 Graphics | | | | | |
| 1642 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_P<15> | NO_TEST=TRUE | 10 83 |
| 1643 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_N<15> | NO_TEST=TRUE | 10 83 |
| 1644 | PCIE_PHY | PCIE | PEG_R2D_C_P<15> | NO_TEST=TRUE | 83 |
| 1645 | PCIE_PHY | PCIE | PEG_R2D_C_N<15> | NO_TEST=TRUE | 83 |
| 1646 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<15> | NO_TEST=TRUE | 83 |
| 1647 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<15> | NO_TEST=TRUE | 83 |
| 1648 | PCIE_PHY | PCIE | PEG_D2R_C_P<15> | NO_TEST=TRUE | 10 83 |
| 1649 | PCIE_PHY | PCIE | PEG_D2R_C_N<15> | NO_TEST=TRUE | 10 83 |
| 1655 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_P<14> | NO_TEST=TRUE | 10 83 |
| 1656 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_N<14> | NO_TEST=TRUE | 10 83 |
| 1652 | PCIE_PHY | PCIE | PEG_R2D_C_P<14> | NO_TEST=TRUE | 83 |
| 1653 | PCIE_PHY | PCIE | PEG_R2D_C_N<14> | NO_TEST=TRUE | 83 |
| 1654 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<14> | NO_TEST=TRUE | 83 |
| 1655 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<14> | NO_TEST=TRUE | 83 |
| 1650 | PCIE_PHY | PCIE | PEG_D2R_C_P<14> | NO_TEST=TRUE | 10 83 |
| 1651 | PCIE_PHY | PCIE | PEG_D2R_C_N<14> | NO_TEST=TRUE | 10 83 |
| 1656 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_P<13> | NO_TEST=TRUE | 10 83 |
| 1657 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_N<13> | NO_TEST=TRUE | 10 83 |
| 1714 | PCIE_PHY | PCIE | PEG_R2D_C_P<13> | NO_TEST=TRUE | 83 |
| 1715 | PCIE_PHY | PCIE | PEG_R2D_C_N<13> | NO_TEST=TRUE | 83 |
| 1712 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<13> | NO_TEST=TRUE | 83 |
| 1713 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<13> | NO_TEST=TRUE | 83 |
| 1714 | PCIE_PHY | PCIE | PEG_D2R_C_P<13> | NO_TEST=TRUE | 10 83 |
| 1715 | PCIE_PHY | PCIE | PEG_D2R_C_N<13> | NO_TEST=TRUE | 10 83 |
| 1716 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_P<12> | NO_TEST=TRUE | 10 83 |
| 1717 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_N<12> | NO_TEST=TRUE | 10 83 |
| 1718 | PCIE_PHY | PCIE | PEG_R2D_C_P<12> | NO_TEST=TRUE | 83 |
| 1719 | PCIE_PHY | PCIE | PEG_R2D_C_N<12> | NO_TEST=TRUE | 83 |
| 1720 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_P<12> | NO_TEST=TRUE | 83 |
| 1721 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_N<12> | NO_TEST=TRUE | 83 |
| 1722 | PCIE_PHY | PCIE | PEG_D2R_C_P<12> | NO_TEST=TRUE | 10 83 |
| 1723 | PCIE_PHY | PCIE | PEG_D2R_C_N<12> | NO_TEST=TRUE | 10 83 |
| 1724 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_P<11> | NO_TEST=TRUE | 10 83 |
| 1725 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_N<11> | NO_TEST=TRUE | 10 83 |
| 1726 | PCIE_PHY | PCIE | PEG_R2D_C_P<11> | NO_TEST=TRUE | 83 |
| 1727 | PCIE_PHY | PCIE | PEG_R2D_C_N<11> | NO_TEST=TRUE | 83 |
| 1728 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<11> | NO_TEST=TRUE | 83 |
| 1729 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<11> | NO_TEST=TRUE | 83 |
| 1730 | PCIE_PHY | PCIE | PEG_D2R_C_P<11> | NO_TEST=TRUE | 10 83 |
| 1731 | PCIE_PHY | PCIE | PEG_D2R_C_N<11> | NO_TEST=TRUE | 10 83 |
| 1732 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_P<10> | NO_TEST=TRUE | 10 83 |
| 1733 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_N<10> | NO_TEST=TRUE | 10 83 |
| 1734 | PCIE_PHY | PCIE | PEG_R2D_C_P<10> | NO_TEST=TRUE | 83 |
| 1735 | PCIE_PHY | PCIE | PEG_R2D_C_N<10> | NO_TEST=TRUE | 83 |
| 1736 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<10> | NO_TEST=TRUE | 83 |
| 1737 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<10> | NO_TEST=TRUE | 83 |
| 1738 | PCIE_PHY | PCIE | PEG_D2R_C_P<10> | NO_TEST=TRUE | 10 83 |
| 1739 | PCIE_PHY | PCIE | PEG_D2R_C_N<10> | NO_TEST=TRUE | 10 83 |
| 1740 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_P<9> | NO_TEST=TRUE | 10 83 |
| 1741 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_N<9> | NO_TEST=TRUE | 10 83 |
| 1742 | PCIE_PHY | PCIE | PEG_R2D_C_P<9> | NO_TEST=TRUE | 83 |
| 1743 | PCIE_PHY | PCIE | PEG_R2D_C_N<9> | NO_TEST=TRUE | 83 |
| 1744 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_P<9> | NO_TEST=TRUE | 83 |
| 1745 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_N<9> | NO_TEST=TRUE | 83 |
| 1746 | PCIE_PHY | PCIE | PEG_D2R_C_P<9> | NO_TEST=TRUE | 10 83 |
| 1747 | PCIE_PHY | PCIE | PEG_D2R_C_N<9> | NO_TEST=TRUE | 10 83 |
| 1748 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_P<8> | NO_TEST=TRUE | 10 83 |
| 1749 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_N<8> | NO_TEST=TRUE | 10 83 |
| 1750 | PCIE_PHY | PCIE | PEG_R2D_C_P<8> | NO_TEST=TRUE | 83 |
| 1751 | PCIE_PHY | PCIE | PEG_R2D_C_N<8> | NO_TEST=TRUE | 83 |
| 1752 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<8> | NO_TEST=TRUE | 83 |
| 1753 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<8> | NO_TEST=TRUE | 83 |
| 1754 | PCIE_PHY | PCIE | PEG_D2R_C_P<8> | NO_TEST=TRUE | 10 83 |
| 1755 | PCIE_PHY | PCIE | PEG_D2R_C_N<8> | NO_TEST=TRUE | 10 83 |

## PCIe (CPU)

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| x16 Graphics | | | | | |
| 1620 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_P<7> | NO_TEST=TRUE | 10 83 |
| 1621 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_N<7> | NO_TEST=TRUE | 10 83 |
| 1622 | PCIE_PHY | PCIE | PEG_R2D_C_P<7> | NO_TEST=TRUE | 83 |
| 1623 | PCIE_PHY | PCIE | PEG_R2D_C_N<7> | NO_TEST=TRUE | 83 |
| 1624 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<7> | NO_TEST=TRUE | 83 |
| 1625 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<7> | NO_TEST=TRUE | 83 |
| 1626 | PCIE_PHY | PCIE | PEG_D2R_C_P<7> | NO_TEST=TRUE | 10 83 |
| 1627 | PCIE_PHY | PCIE | PEG_D2R_C_N<7> | NO_TEST=TRUE | 10 83 |
| 1638 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_P<6> | NO_TEST=TRUE | 10 83 |
| 1639 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_N<6> | NO_TEST=TRUE | 10 83 |
| 1630 | PCIE_PHY | PCIE | PEG_R2D_C_P<6> | NO_TEST=TRUE | 83 |
| 1631 | PCIE_PHY | PCIE | PEG_R2D_C_N<6> | NO_TEST=TRUE | 83 |
| 1632 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<6> | NO_TEST=TRUE | 83 |
| 1633 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<6> | NO_TEST=TRUE | 83 |
| 1634 | PCIE_PHY | PCIE | PEG_D2R_C_P<6> | NO_TEST=TRUE | 10 83 |
| 1635 | PCIE_PHY | PCIE | PEG_D2R_C_N<6> | NO_TEST=TRUE | 10 83 |
| 1636 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_P<5> | NO_TEST=TRUE | 10 83 |
| 1637 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_N<5> | NO_TEST=TRUE | 10 83 |
| 1638 | PCIE_PHY | PCIE | PEG_R2D_C_P<5> | NO_TEST=TRUE | 83 |
| 1639 | PCIE_PHY | PCIE | PEG_R2D_C_N<5> | NO_TEST=TRUE | 83 |
| 1640 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<5> | NO_TEST=TRUE | 83 |
| 1641 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<5> | NO_TEST=TRUE | 83 |
| 1642 | PCIE_PHY | PCIE | PEG_D2R_C_P<5> | NO_TEST=TRUE | 10 83 |
| 1643 | PCIE_PHY | PCIE | PEG_D2R_C_N<5> | NO_TEST=TRUE | 10 83 |
| 1644 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_P<4> | NO_TEST=TRUE | 10 83 |
| 1645 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_N<4> | NO_TEST=TRUE | 10 83 |
| 1646 | PCIE_PHY | PCIE | PEG_R2D_C_P<4> | NO_TEST=TRUE | 83 |
| 1647 | PCIE_PHY | PCIE | PEG_R2D_C_N<4> | NO_TEST=TRUE | 83 |
| 1648 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_P<4> | NO_TEST=TRUE | 83 |
| 1649 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_N<4> | NO_TEST=TRUE | 83 |
| 1650 | PCIE_PHY | PCIE | PEG_D2R_C_P<4> | NO_TEST=TRUE | 10 83 |
| 1651 | PCIE_PHY | PCIE | PEG_D2R_C_N<4> | NO_TEST=TRUE | 10 83 |
| 1652 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_P<3> | NO_TEST=TRUE | 10 83 |
| 1653 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_N<3> | NO_TEST=TRUE | 10 83 |
| 1654 | PCIE_PHY | PCIE | PEG_R2D_C_P<3> | NO_TEST=TRUE | 83 |
| 1655 | PCIE_PHY | PCIE | PEG_R2D_C_N<3> | NO_TEST=TRUE | 83 |
| 1656 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_P<3> | NO_TEST=TRUE | 83 |
| 1657 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_N<3> | NO_TEST=TRUE | 83 |
| 1658 | PCIE_PHY | PCIE | PEG_D2R_C_P<3> | NO_TEST=TRUE | 10 83 |
| 1659 | PCIE_PHY | PCIE | PEG_D2R_C_N<3> | NO_TEST=TRUE | 10 83 |
| 1660 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_P<2> | NO_TEST=TRUE | 10 83 |
| 1661 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_N<2> | NO_TEST=TRUE | 10 83 |
| 1662 | PCIE_PHY | PCIE | PEG_R2D_C_P<2> | NO_TEST=TRUE | 83 |
| 1663 | PCIE_PHY | PCIE | PEG_R2D_C_N<2> | NO_TEST=TRUE | 83 |
| 1664 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<2> | NO_TEST=TRUE | 83 |
| 1665 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<2> | NO_TEST=TRUE | 83 |
| 1666 | PCIE_PHY | PCIE | PEG_D2R_C_P<2> | NO_TEST=TRUE | 10 83 |
| 1667 | PCIE_PHY | PCIE | PEG_D2R_C_N<2> | NO_TEST=TRUE | 10 83 |
| 1668 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_P<1> | NO_TEST=TRUE | 10 83 |
| 1669 PCIE_GEN3_R2D_PINV | PCIE_PHY | PCIE | PEG_R2D_N<1> | NO_TEST=TRUE | 10 83 |
| 1670 | PCIE_PHY | PCIE | PEG_R2D_C_P<1> | NO_TEST=TRUE | 83 |
| 1671 | PCIE_PHY | PCIE | PEG_R2D_C_N<1> | NO_TEST=TRUE | 83 |
| 1672 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_P<1> | NO_TEST=TRUE | 83 |
| 1673 PCIE_GEN3_D2R | PCIE_PHY | PCIE | PEG_D2R_N<1> | NO_TEST=TRUE | 83 |
| 1674 | PCIE_PHY | PCIE | PEG_D2R_C_P<1> | NO_TEST=TRUE | 10 83 |
| 1675 | PCIE_PHY | PCIE | PEG_D2R_C_N<1> | NO_TEST=TRUE | 10 83 |
| 1676 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_P<0> | NO_TEST=TRUE | 10 83 |
| 1677 PCIE_GEN3_R2D | PCIE_PHY | PCIE | PEG_R2D_N<0> | NO_TEST=TRUE | 10 83 |
| 1678 | PCIE_PHY | PCIE | PEG_R2D_C_P<0> | NO_TEST=TRUE | 83 |
| 1679 | PCIE_PHY | PCIE | PEG_R2D_C_N<0> | NO_TEST=TRUE | 83 |
| 1680 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_P<0> | NO_TEST=TRUE | 83 |
| 1681 PCIE_GEN3_D2R_PINV | PCIE_PHY | PCIE | PEG_D2R_N<0> | NO_TEST=TRUE | 83 |
| 1682 | PCIE_PHY | PCIE | PEG_D2R_C_P<0> | NO_TEST=TRUE | 10 83 |
| 1683 | PCIE_PHY | PCIE | PEG_D2R_C_N<0> | NO_TEST=TRUE | 10 83 |
| CPU PCIe Clocks | | | | | |
| 1686 PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PEG_CLK100M_P | NO_TEST=TRUE | 10 83 |
| 1687 PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | PEG_CLK100M_N | NO_TEST=TRUE | 10 83 |
| CPU PCIe Compensation | | | | | |
| 1688 | COMP_PCIE_PHY | COMP_PCIE | CPU_PEG_COMP | | 10 |

SYNC_MASTER=D8_MLB SYNC_DATE=02/06/2012

PAGE TITLE
# CPU PCIe Constraints

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

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# DMI

## DMI-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DMI_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| DMI_PHY | * | DMI_85D |

# CPU Misc / FDI

## CPU-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CPU_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| COMP_FDI_SE | * | Y | 0.3 MM | 0.25 MM | 3 MM | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| CPU_PHY | * | CPU_50S |
| COMP_FDI_PHY | * | COMP_FDI_SE |

## CPU-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CPU_ISO | * | =3:1_SPACING | ? |
| COMP_FDI_ISO | * | =4:1_SPACING | ? |

## Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CPU | * | * | CPU_ISO |
| COMP_FDI | * | * | COMP_FDI_ISO |

FDI Compensation Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

| Table | Trace | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 6-4 | 10 | 11.81 | - | 15.75 | Using PCIe guidelines |

# XDP

## XDP-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| XDP_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| XDP_PHY | * | XDP_50S |

## XDP-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| XDP_ISO | * | =2:1_SPACING | ? |
| XDP_CLK_ISO | * | =4:1_SPACING | ? |

## Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| XDP | * | * | XDP_ISO |
| CLK_JTAG | * | * | XDP_CLK_ISO |
| OBS_STROBE | * | * | XDP_CLK_ISO |

Desktop Debug Design Guide (Intel Doc# 430883)

| Section | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 1.5 | 45-65 | 50 | - | 15.75 | Isolation is for JTAG clocks.<br>All signals default are 50 Ohm SE. |

## DMI

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| DMI | | | | | |
| 116 DMI_N2S | DMI_PHY | PCIE | DMI_N2S_P<3..0> | NO_TEST=TRUE | 10 19 |
| 116 DMI_N2S | DMI_PHY | PCIE | DMI_N2S_N<3..0> | NO_TEST=TRUE | 10 19 |
| 116 DMI_S2N | DMI_PHY | PCIE | DMI_S2N_P<3..0> | NO_TEST=TRUE | 10 19 |
| 116 DMI_S2N | DMI_PHY | PCIE | DMI_S2N_N<3..0> | NO_TEST=TRUE | 10 19 |
| 128 PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | DMI_CLK100M_CPU_P | | 11 18 |
| 128 PCIE_REF_CLK | CLK_PCIE_PHY | CLK_PCIE | DMI_CLK100M_CPU_N | | 11 18 |
| DMI Compensation | | | | | |
| 172 | COMP_PCIE_PHY | COMP_PCIE | PCH_DMI_COMP | | 19 |
| 122 | COMP_PCIE_PHY | COMP_PCIE | PCH_DMI2RBIAS | | 19 |

## CPU Misc.

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| CPU Misc. | | | | |
| 124 | CPU_PHY | CPU | CPU_SKTOCC_L | 11 64 |
| 124 | CPU_PHY | CPU | CPU_PROC_SEL | 11 19 |
| 125 | CPU_PHY | CPU | CPU_CATERR_L | 11 48 |
| 125 | CPU_PHY | CPU | CPU_PECI | 11 21 47 48 |
| 125 | CPU_PHY | CPU | CPU_PROCHOT_L | 11 47 48 66 |
| 126 | CPU_PHY | CPU | CPU_PROCHOT_R_L | 11 |
| 124 | CPU_PHY | CPU | CPU_THRMTRIP_L | 11 48 |
| 124 | CPU_PHY | CPU | CPU_RESET_L | 11 26 |
| 124 | CPU_PHY | CPU | PLT_RESET_LS1V05_L | 11 |
| 124 | CPU_PHY | CPU | PM_SYNC | 11 19 |
| 124 | CPU_PHY | CPU | CPU_PWRGD | 11 21 25 28 |
| 126 | CPU_PHY | CPU | PM_MEM_PWRGD | 11 19 28 |
| 125 | CPU_PHY | CPU | PM_MEM_PWRGD_R | 11 |
| 128 | CPU_PHY | CPU | CPU_MEM_RESET_L | 11 28 |

## FDI

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| FDI Compensation | | | | |
| 126 | COMP_FDI_PHY | COMP_FDI | CPU_FDI_COMPIO | 10 |

## XDP

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| XDP MISC. | | | | |
| 117 XDP_BPM_L | XDP_PHY | XDP | XDP_BPM_L<7..0> | 11 25 |
| 117 | XDP_PHY | XDP | CPU_CFG<17..16> | 10 25 |
| 125 | XDP_PHY | XDP | CPU_CFG<11..0> | 10 15 25 |
| 126 | XDP_PHY | XDP | XDP_DBRESET_L | 11 25 |
| 126 | XDP_PHY | XDP | XDP_CPU_PWRGD | 25 |
| 126 | XDP_PHY | XDP | XDP_CPU_PWRBTN_L | 25 |
| 124 | XDP_PHY | XDP | XDP_CPU_CFG<0> | 25 |
| 126 | XDP_PHY | XDP | XDP_VR_READY | 25 |
| 127 | XDP_PHY | XDP | XDP_CPU_PLTRST_L | 25 26 |
| 126 | XDP_PHY | XDP | XDP_PCH_PWRGD | 25 |
| 126 | XDP_PHY | XDP | XDP_PCH_PWRBTN_L | 25 |
| 127 | XDP_PHY | XDP | XDP_PCH_PLTRST_L | 25 26 |
| 117 | CLK_PCIE_PHY | CLK_PCIE | ITPCPU_CLK100M_P | 11 15 |
| 117 | CLK_PCIE_PHY | CLK_PCIE | ITPCPU_CLK100M_N | 11 15 |
| 117 TTP_CLK_CONN | CLK_PCIE_PHY | CLK_PCIE | ITPXDP_CLK100M_P | 15 18 25 |
| 118 TTP_CLK_CONN | CLK_PCIE_PHY | CLK_PCIE | ITPXDP_CLK100M_N | 15 18 25 |
| 117 | CLK_PCIE_PHY | CLK_PCIE | XDP_CPU_CLK100M_P | 25 |
| 118 | CLK_PCIE_PHY | CLK_PCIE | XDP_CPU_CLK100M_N | 25 |
| CPU JTAG | | | | |
| 118 | XDP_PHY | CLK_JTAG | XDP_CPU_TCK | 11 25 |
| 118 | XDP_PHY | XDP | XDP_CPU_TMS | 11 25 |
| 118 | XDP_PHY | XDP | XDP_CPU_TDI | 11 25 |
| 118 | XDP_PHY | XDP | XDP_CPU_TDO | 11 25 |
| 115 | XDP_PHY | XDP | XDP_CPU_TRST_L | 11 25 |
| 125 | XDP_PHY | XDP | XDP_CPU_PRDY_L | 11 25 |
| 125 | XDP_PHY | XDP | XDP_CPU_PREQ_L | 11 25 |
| PCH JTAG | | | | |
| 118 | XDP_PHY | CLK_JTAG | XDP_PCH_TCK | 18 25 |
| 118 | XDP_PHY | XDP | XDP_PCH_TMS | 18 25 |
| 118 | XDP_PHY | XDP | XDP_PCH_TDI | 18 25 |
| 118 | XDP_PHY | XDP | XDP_PCH_TDO | 18 25 |

## Chipset Test Interface

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| OBS PCH Side | | | | |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | USB_EXTA_OC_R_L | 20 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | USB_EXTB_OC_R_L | 20 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | USB_EXTC_OC_R_L | 20 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | USB_EXTD_OC_R_L | 20 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | USB_EXTB_OC_EHCI_R_L | 20 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | USB_EXTD_OC_EHCI_R_L | 20 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | AP_PWR_EN_R | 20 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | SDCONN_STATE_CHANGE_R | 20 25 |
| 150 XDP_PCH_OBS | XDP_PHY | OBS_STROBE | TBT_CIO_PLUG_EVENT_R | 21 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | ISOLATE_CPU_MEM_R_L | 21 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | GPU_GOOD_R | 21 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | DP_AUXCH_ISOL_R | 18 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | SATARDRVR_EN_R | 18 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | DP_TBT_SEL_R | 21 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | JTAG_TBT_TCK_R | 21 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | AUD_IPHS_SWITCH_EN_PCH_R | 21 25 |
| 150 XDP_PCH_OBS | XDP_PHY | XDP | ENET_LOW_PWR_PCH_R | 21 25 |
| 150 XDP_PCH_OBS_UNUSED | XDP_PHY | OBS_STROBE | XDP_PIN03 | 21 25 |
| OBS XDP Side | | | | |
| 150 | XDP_PHY | XDP | XDP_DA0_USB_EXTA_OC_L | 25 |
| 150 | XDP_PHY | XDP | XDP_DA1_USB_EXTB_OC_L | 25 |
| 151 | XDP_PHY | XDP | XDP_DA2_USB_EXTC_OC_L | 25 |
| 151 | XDP_PHY | XDP | XDP_DA3_USB_EXTD_OC_L | 25 |
| 151 | XDP_PHY | XDP | XDP_DB0_USB_EXTB_OC_EHCI_L | 25 |
| 151 | XDP_PHY | XDP | XDP_DB1_USB_EXTD_OC_EHCI_L | 25 |
| 151 | XDP_PHY | XDP | XDP_DB2_AP_PWR_EN | 25 |
| 151 | XDP_PHY | XDP | XDP_DB3_SDCONN_STATE_CHANGE | 25 |
| 151 | XDP_PHY | OBS_STROBE | XDP_FC1_TBT_CIO_PLUG_EVENT | 25 |
| 151 | XDP_PHY | XDP | XDP_DC0_ISOLATE_CPU_MEM_L | 25 |
| 151 | XDP_PHY | XDP | XDP_DC1_GPU_GOOD | 25 |
| 152 | XDP_PHY | XDP | XDP_DC2_DP_AUXCH_ISOL | 25 |
| 152 | XDP_PHY | XDP | XDP_DC3_SATARDRVR_EN | 25 |
| 152 | XDP_PHY | XDP | XDP_DD0_DP_TBT_SEL | 25 |
| 152 | XDP_PHY | XDP | XDP_DD1_JTAG_TBT_TCK | 25 |
| 152 | XDP_PHY | XDP | XDP_DD2_AUD_IPHS_SWITCH_EN_PCH | 25 |
| 152 | XDP_PHY | XDP | XDP_DD3_ENET_LOW_PWR_PCH | 25 |
| 152 | XDP_PHY | OBS_STROBE | XDP_FC0_PCH_GPIO15 | 25 |
| Standard usage branch off from OBS | | | | |
| 152 | XDP_PHY | XDP | USB_EXTA_OC_L | 15 20 45 |
| 152 | XDP_PHY | XDP | USB_EXTB_OC_L | 15 20 45 |
| 153 | XDP_PHY | XDP | USB_EXTC_OC_L | 15 20 46 |
| 152 | XDP_PHY | XDP | USB_EXTD_OC_L | 15 20 46 |
| 153 | XDP_PHY | XDP | USB_EXTB_OC_EHCI_L | 15 20 |
| 153 | XDP_PHY | XDP | USB_EXTD_OC_EHCI_L | 15 20 |
| 153 | XDP_PHY | XDP | AP_PWR_EN | 15 20 |
| 153 | XDP_PHY | XDP | SDCONN_STATE_CHANGE | 15 20 41 |
| 153 | XDP_PHY | OBS_STROBE | TBT_CIO_PLUG_EVENT | 15 21 |
| 154 | XDP_PHY | XDP | ISOLATE_CPU_MEM_L | 21 28 34 |
| 154 | XDP_PHY | XDP | GPU_GOOD | 5 21 |
| 154 | XDP_PHY | XDP | DP_AUXCH_ISOL | 15 18 |
| 154 | XDP_PHY | XDP | SATARDRVR_EN | 15 18 |
| 154 | XDP_PHY | XDP | DP_TBT_SEL | 21 62 75 |
| 154 | XDP_PHY | XDP | JTAG_TBT_TCK | 15 21 |
| 127 | XDP_PHY | XDP | JTAG_TBT_TCK_ISOL | 15 36 |
| 124 | XDP_PHY | XDP | AUD_IPHS_SWITCH_EN_PCH | 21 26 |
| 124 | XDP_PHY | XDP | ENET_LOW_PWR_PCH | 15 21 26 |
| 127 | XDP_PHY | XDP | DP_AUXCH_ISOL_EN | 15 |

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CPU MISC/DMI/FDI/XDP Constraints

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# SATA

## SATA-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SATA_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| SATA_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SATA_PHY | * | SATA_90D |
| COMP_SATA_PHY | * | SATA_50S |

## SATA-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SATA_ISO | * | =7.2X_DIELECTRIC | ? |
| COMP_SATA_ISO | * | =5.4X_DIELECTRIC | ? |

## Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SATA | * | * | SATA_ISO |
| COMP_SATA | * | * | COMP_SATA_ISO |

## SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

| Section | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 15.2.1 | 90 | 95 | 20 | 23.62 | SATA Gen2, SATA Gen3 |

## SATA Compensation Rules (mils)

| Table | Imp | Design | Iso | Design | Comments |
|---|---|---|---|---|---|
| 15-3 | 50 | 50 | 15 | 15.75 | SATA Gen2, SATA Gen3 |

## SATA

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| **PCH SATA Port 0 (HDD)** | | | | |
| 190 SATA_R2D | SATA_PHY | SATA | SATA_HDD_R2D_P | 44 |
| 192 SATA_R2D | SATA_PHY | SATA | SATA_HDD_R2D_N | 44 |
| 188 | SATA_PHY | SATA | SATA_HDD_R2D_C_P | 18 44 |
| 189 | SATA_PHY | SATA | SATA_HDD_R2D_C_N | 18 44 |
| 194 SATA_D2R | SATA_PHY | SATA | SATA_HDD_D2R_P | 18 44 |
| 195 SATA_D2R | SATA_PHY | SATA | SATA_HDD_D2R_N | 18 44 |
| 191 | SATA_PHY | SATA | SATA_HDD_D2R_C_P | 44 |
| 193 | SATA_PHY | SATA | SATA_HDD_D2R_C_N | 44 |
| **PCH SATA Port 1 (SSD)** | | | | |
| 197 SATA_R2D_MUX_SSD | SATA_PHY | SATA | SATA_SSD_R2D_P | 18 44 |
| 199 SATA_R2D_MUX_SSD | SATA_PHY | SATA | SATA_SSD_R2D_N | 18 44 |
| 196 SATA_D2R_MUX_SSD | SATA_PHY | SATA | SATA_SSD_D2R_P | 18 44 |
| 198 SATA_D2R_MUX_SSD | SATA_PHY | SATA | SATA_SSD_D2R_N | 18 44 |
| **PCH SATA Compensation** | | | | |
| 1400 | COMP_SATA_PHY | COMP_SATA | PCH_SATA1COMP | 18 |
| 1400 | COMP_SATA_PHY | COMP_SATA | PCH_SATA3COMP | 18 |
| 1400 | COMP_SATA_PHY | COMP_SATA | PCH_SATA3RBIAS | 18 |

## Unused

| Electrical Contraint Set | Physical | Spacing |
|---|---|---|
| | | |




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# PCH

## PCH-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCH_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| CLK_PCH_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## PCH-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_PCH_ISO | * | =6.5X_DIELECTRIC | ? |
| COMP_PCH_ISO | * | =2:1_SPACING | ? |
| PCH_ISO | * | =3:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CLK_PCH | * | * | CLK_PCH_ISO |
| COMP_PCH | * | * | COMP_PCH_ISO |
| PCH | * | * | PCH_ISO |

# PCI

## PCI-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| PCI_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| CLK_PCI_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## PCI-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_PCI_ISO | * | =3.6X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CLK_PCI | * | * | CLK_PCI_ISO |

# LPC

## LPC-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| LPC_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| CLK_LPC_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## LPC-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| LPC_ISO | * | =1.5:1_SPACING | ? |
| CLK_LPC_ISO | * | =3.6X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| LPC | * | * | LPC_ISO |
| CLK_LPC | * | * | CLK_LPC_ISO |

# HDA

## HDA-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| HDA_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## HDA-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| HDA_ISO | * | =2X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| HDA | * | * | HDA_ISO |

# Crystal

## Crystal-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CLK_XTAL | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |

## Crystal-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| XTAL_ISO | * | =4X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| XTAL | * | * | XTAL_ISO |

# SPI

## SPI-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SPI_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## SPI-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SPI_ISO | * | =2X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SPI | * | * | SPI_ISO |

# PCI

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| PCI Clock | | | | |
| 1833 | CLK_PCI_50S | CLK_PCI | PCH_CLK33M_PCIIN | 18 26 |
| 1832 | CLK_PCI_50S | CLK_PCI | PCH_CLK33M_PCIOUT | 20 26 |

# LPC

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| LPC | | | | |
| 1838 | LPC_50S | LPC | LPC_AD<3..0> | 18 47 49 |
| 1839 | LPC_50S | LPC | LPC_R_AD<3..0> | 18 |
| 1836 | LPC_50S | LPC | LPC_FRAME_L | 18 47 49 |
| 1837 | LPC_50S | LPC | LFRAME_L | 18 |
| LPC Clocks | | | | |
| 1835 | CLK_LPC_50S | CLK_LPC | LPC_CLK33M_LPCPLUS | 26 49 |
| 1845 | CLK_LPC_50S | CLK_LPC | LPC_CLK33M_LPCPLUS_R | 20 26 |
| 1843 | CLK_LPC_50S | CLK_LPC | LPC_CLK33M_SMC | 26 47 |
| 1844 | CLK_LPC_50S | CLK_LPC | LPC_CLK33M_SMC_R | 20 26 |

# PCH Clocks

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| PCH Reference Clock | | | | |
| 1188 | CLK_PCH_50S | CLK_PCH | SYSCLK_CLK25M_SB | 26 |
| 1189 | CLK_PCH_50S | CLK_PCH | PCH_CLK25M_XTALIN | 18 26 |
| PCH Ref Clock Comp | | | | |
| 1840 | PCH_50S | COMP_PCH | PCH_XCLK_RCOMP | 18 |
| PCH RTC 32K | | | | |
| 1841 | CLK_XTAL | XTAL | PCH_CLK32K_RTCX1 | 18 26 |
| 1842 | CLK_XTAL | XTAL | PCH_CLK32K_RTCX2 | 18 26 |
| 1852 | CLK_XTAL | XTAL | PCH_CLK32K_RTCX2_R | 26 |
| SMC 32K | | | | |
| 1846 | CLK_PCH_50S | CLK_PCH | PM_CLK32K_SUSCLK_R | 19 48 |
| 1858 | CLK_PCH_50S | CLK_PCH | SMC_CLK32K | 47 48 |

# 25 MHz Reference Clocks

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| 25M Reference Crystal | | | | |
| 1870 | CLK_XTAL | XTAL | SYSCLK_CLK25M_X1 | 26 |
| 1871 | CLK_XTAL | XTAL | SYSCLK_CLK25M_X2 | 26 |
| 1872 | CLK_XTAL | XTAL | SYSCLK_CLK25M_X2_R | 26 |
| 25M Reference Clocks | | | | |
| 1873 | CLK_PCH_50S | CLK_PCH | SYSCLK_CLK25M_ENET | 26 39 |
| 1874 | CLK_PCH_50S | CLK_PCH | SYSCLK_CLK25M_ENET_R | 26 |
| 1875 | CLK_PCH_50S | CLK_PCH | SYSCLK_CLK25M_TBT | 26 36 |
| 1876 | CLK_PCH_50S | CLK_PCH | SYSCLK_CLK25M_TBT_R | 36 |

# HDA

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| HDA | | | | |
| 1860 | HDA_50S | HDA | HDA_BIT_CLK | 18 56 |
| 1861 | HDA_50S | HDA | HDA_BIT_CLK_R | 18 |
| 1862 | HDA_50S | HDA | HDA_RST_L | 18 56 |
| 1863 | HDA_50S | HDA | HDA_RST_R_L | 18 |
| 1865 | HDA_50S | HDA | HDA_SDOUT | 18 56 |
| 1867 | HDA_50S | HDA | HDA_SDOUT_R | 15 18 |
| 1866 | HDA_50S | HDA | HDA_SYNC | 15 18 56 |
| 1868 | HDA_50S | HDA | HDA_SYNC_R | 18 |
| 1869 | HDA_50S | HDA | HDA_SDIN0 | 18 56 |
| 1864 | HDA_50S | HDA | AUD_SDI_R | 56 |
| 1814 | HDA_50S | HDA | SPI_DESCRIPTOR_OVERRIDE_R | 15 |
| SPDIF | | | | |
| 1870 | | HDA | AUD_SPDIF_CHIP | 56 |
| 1872 | | HDA | AUD_SPDIF_OUT | 56 60 |

# SPI Bootrom

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| SPI ROM | | | | |
| 1801 | SPI_50S | SPI | SPI_CLK_R | 18 49 |
| 1802 | SPI_50S | SPI | SPI_CLK | 49 |
| 1803 | SPI_50S | SPI | SPI_ALT_CLK | 49 |
| 1140 | SPI_50S | SPI | SPI_SMC_CLK | 47 48 |
| 1147 | SPI_50S | SPI | SPI_MLB_CLK | 48 49 |
| 1804 | SPI_50S | SPI | SPI_CS0_R_L | 18 49 |
| 1805 | SPI_50S | SPI | SPI_CS0_L | 49 |
| 1806 | SPI_50S | SPI | SPI_ALT_CS_L | 49 |
| 1148 | SPI_50S | SPI | SPI_SMC_CS_L | 47 48 |
| 1807 | SPI_50S | SPI | SPI_MLB_CS_L | 48 49 |
| 1808 | SPI_50S | SPI | SPI_MOSI_R | 18 49 |
| 1809 | SPI_50S | SPI | SPI_MOSI | 49 |
| 1149 | SPI_50S | SPI | SPI_ALT_MOSI | 49 |
| 1151 | SPI_50S | SPI | SPI_SMC_MOSI | 47 48 |
| 1181 | SPI_50S | SPI | SPI_MLB_MOSI | 48 49 |
| 1810 | SPI_50S | SPI | SPI_MISO | 18 49 |
| 1150 | SPI_50S | SPI | SPI_ALT_MISO | 49 |
| 1152 | SPI_50S | SPI | SPI_SMC_MISO | 47 48 |
| 1182 | SPI_50S | SPI | SPI_MLB_MISO | 48 49 |
| 1160 | SPI_50S | SPI | SPIROM_USE_MLB | 21 49 |

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# PCH and BR Constraints

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# USB

## USB-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| USB_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |
| USB_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF |
| USB_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| USB2_PHY | * | USB_90D |
| USB3_PHY | * | USB_85D |
| USB_HUB_PHY | * | USB_50S |

## USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

| Section | Imp | Design | Iso | Comments |
|---|---|---|---|---|
| 12.2.1 | 90 | 90 | 12/2.8 mils = 4.29:1 | USB 2.0 |
| 13.3.1 | 85 | 85 | 20/2.8 mils = 7.14:1 | USB 3.0 |
| | | | 50/2.8 mils = 17.9:1 | USB 2.0/3.0 |

SMSC Hub Application Note 15.17
Single-ended impedance range from 45-80 ohm is acceptable

## USB 2.0 Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| USB2_ISO | * | =4.4X_DIELECTRIC | ? |
| USB2_ISO | TOP,BOTTOM | =4.4X_DIELECTRIC | ? |
| USB2_CLK_ISO | * | =18X_DIELECTRIC | ? |
| USB2_CLK_ISO | TOP,BOTTOM | =18X_DIELECTRIC | ? |
| USB_HUB_ISO | * | =2:1_SPACING | ? |

## USB 3.0 Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| USB3_ISO | * | =7.3X_DIELECTRIC | ? |
| USB3_ISO | TOP,BOTTOM | =7.3X_DIELECTRIC | ? |
| USB3_CLK_ISO | * | =18X_DIELECTRIC | ? |
| USB3_CLK_ISO | TOP,BOTTOM | =18X_DIELECTRIC | ? |
| USB3_USB3_ISO | * | =7.3X_DIELECTRIC | ? |
| USB3_USB3_ISO | TOP,BOTTOM | =7.3X_DIELECTRIC | ? |
| USB3_USB3_ISO | ISL10 | =5X_DIELECTRIC | ? |

## USB 2.0 Spacing Rules

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| USB2 | * | * | USB2_ISO |
| USB2 | *CLK* | * | USB2_CLK_ISO |
| USB2 | DISPLAYPORT | * | USB2_CLK_ISO |
| USB2 | *TBT* | * | USB2_CLK_ISO |
| USB2 | *ENET* | * | USB2_CLK_ISO |
| USB2 | *SD* | * | USB2_CLK_ISO |
| USB3 | PCIE | * | USB3_CLK_ISO |
| USB3 | SATA | * | USB3_CLK_ISO |
| USB_HUB | * | * | USB_HUB_ISO |

## USB 3.0 Spacing Rules

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| USB3 | * | * | USB3_ISO |
| USB3 | *CLK* | * | USB3_CLK_ISO |
| USB3 | DISPLAYPORT | * | USB3_CLK_ISO |
| USB3 | *TBT* | * | USB3_CLK_ISO |
| USB3 | *ENET* | * | USB3_CLK_ISO |
| USB3 | *SD* | * | USB3_CLK_ISO |
| USB3 | PCIE | * | USB3_CLK_ISO |
| USB3 | SATA | * | USB3_CLK_ISO |
| USB3 | USB3 | * | USB3_USB3_ISO |

# CAMERA CONTROLLER

## Camera Controller's SMIA Interface & MISC. Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SMIA_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| CAM_SE | * | Y | 0.2 MM | 0.1 MM | =STANDARD | =STANDARD | =STANDARD |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SMIA_DIFF_PHY | * | SMIA_100D |
| CAM_PHY | * | CAM_SE |

## Camera Controller's SMIA Interface & MISC. Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SMIA_DIFF_ISO | * | =6:1_SPACING | ? |
| SMIA_DIFF2DIFF | * | =3:1_SPACING | ? |
| CAM_ISO | * | =2:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SMIA_DIFF | * | * | SMIA_DIFF_ISO |
| SMIA_DIFF | SMIA_DIFF | * | SMIA_DIFF2DIFF |
| CAM | * | * | CAM_ISO |

## USB 3.0 and USB 2.0 Trixies Muxing

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| External Port A (J4600) | | | | |
| J8700 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTA_RX_P | 45 |
| J8701 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTA_RX_N | 45 |
| J8692 | USB3_PHY | USB3 | USB3_EXTA_RX_F_P | 20 45 |
| J8692 | USB3_PHY | USB3 | USB3_EXTA_RX_F_N | 20 45 |
| J8610 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTA_TX_P | 20 45 |
| J8611 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTA_TX_N | 20 45 |
| J8612 | USB3_PHY | USB3 | USB3_EXTA_TX_F_P | 45 |
| J8612 | USB3_PHY | USB3 | USB3_EXTA_TX_F_N | 45 |
| J8612 | USB3_PHY | USB3 | USB3_EXTA_TX_C_P | 45 |
| J8612 | USB3_PHY | USB3 | USB3_EXTA_TX_C_N | 45 |
| J8617 USB2_MUXED_MOJO_CONN | USB2_PHY | USB2 | USB_PCH_0_P | 20 45 |
| J8618 USB2_MUXED_MOJO_CONN | USB2_PHY | USB2 | USB_PCH_0_N | 20 45 |
| J8619 | USB2_PHY | USB2 | USB2_EXTA_MUXED_P | 45 |
| J8620 | USB2_PHY | USB2 | USB2_EXTA_MUXED_N | 45 |
| J8622 | USB2_PHY | USB2 | USB2_EXTA_MUXED_F_P | 45 |
| J8622 | USB2_PHY | USB2 | USB2_EXTA_MUXED_F_N | 45 |
| External Port B (J4610) | | | | |
| J8637 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTB_RX_P | 45 |
| J8638 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTB_RX_N | 45 |
| J8639 | USB3_PHY | USB3 | USB3_EXTB_RX_F_P | 20 45 |
| J8639 | USB3_PHY | USB3 | USB3_EXTB_RX_F_N | 20 45 |
| J8646 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTB_TX_P | 20 45 |
| J8647 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTB_TX_N | 20 45 |
| J8648 | USB3_PHY | USB3 | USB3_EXTB_TX_F_P | 45 |
| J8648 | USB3_PHY | USB3 | USB3_EXTB_TX_F_N | 45 |
| J8648 | USB3_PHY | USB3 | USB3_EXTB_TX_C_P | 45 |
| J8648 | USB3_PHY | USB3 | USB3_EXTB_TX_C_N | 45 |
| J8430 USB2_MUXED_CONN | USB2_PHY | USB2 | USB_PCH_1_P | 20 45 |
| J8431 USB2_MUXED_CONN | USB2_PHY | USB2 | USB_PCH_1_N | 20 45 |
| J8432 | USB2_PHY | USB2 | USB_PCH_9_P | 20 45 |
| J8432 | USB2_PHY | USB2 | USB_PCH_9_N | 20 45 |
| J8437 | USB2_PHY | USB2 | USB2_EXTB_MUXED_P | 45 |
| J8438 | USB2_PHY | USB2 | USB2_EXTB_MUXED_N | 45 |
| J8439 | USB2_PHY | USB2 | USB2_EXTB_MUXED_F_P | 45 |
| J8439 | USB2_PHY | USB2 | USB2_EXTB_MUXED_F_N | 45 |
| External Port C (J4700) | | | | |
| J8437 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTC_RX_P | 46 |
| J8438 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTC_RX_N | 46 |
| J8439 | USB3_PHY | USB3 | USB3_EXTC_RX_F_P | 20 46 |
| J8439 | USB3_PHY | USB3 | USB3_EXTC_RX_F_N | 20 46 |
| J8441 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTC_TX_P | 20 46 |
| J8442 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTC_TX_N | 20 46 |
| J8443 | USB3_PHY | USB3 | USB3_EXTC_TX_F_P | 46 |
| J8443 | USB3_PHY | USB3 | USB3_EXTC_TX_F_N | 46 |
| J8443 | USB3_PHY | USB3 | USB3_EXTC_TX_C_P | 46 |
| J8443 | USB3_PHY | USB3 | USB3_EXTC_TX_C_N | 46 |
| J8446 USB2_CONN | USB2_PHY | USB2 | USB_PCH_2_P | 20 46 |
| J8447 USB2_CONN | USB2_PHY | USB2 | USB_PCH_2_N | 20 46 |
| J8448 | USB2_PHY | USB2 | USB2_EXTC_F_P | 46 |
| J8448 | USB2_PHY | USB2 | USB2_EXTC_F_N | 46 |
| External Port D (J4710) | | | | |
| J8455 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTD_RX_P | 46 |
| J8456 USB3_RX_CONN | USB3_PHY | USB3 | USB3_EXTD_RX_N | 46 |
| J8457 | USB3_PHY | USB3 | USB3_EXTD_RX_F_P | 20 46 |
| J8457 | USB3_PHY | USB3 | USB3_EXTD_RX_F_N | 20 46 |
| J8457 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTD_TX_P | 20 46 |
| J8458 USB3_TX_CONN | USB3_PHY | USB3 | USB3_EXTD_TX_N | 20 46 |
| J8460 | USB3_PHY | USB3 | USB3_EXTD_TX_F_P | 46 |
| J8460 | USB3_PHY | USB3 | USB3_EXTD_TX_F_N | 46 |
| J8460 | USB3_PHY | USB3 | USB3_EXTD_TX_C_P | 46 |
| J8460 | USB3_PHY | USB3 | USB3_EXTD_TX_C_N | 46 |
| J8452 USB2_MUXED_CONN | USB2_PHY | USB2 | USB_PCH_3_P | 20 46 |
| J8453 USB2_MUXED_CONN | USB2_PHY | USB2 | USB_PCH_3_N | 20 46 |
| J8454 | USB2_PHY | USB2 | USB_PCH_10_P | 20 46 |
| J8454 | USB2_PHY | USB2 | USB_PCH_10_N | 20 46 |
| J8456 | USB2_PHY | USB2 | USB2_EXTD_MUXED_P | 46 |
| J8457 | USB2_PHY | USB2 | USB2_EXTD_MUXED_N | 46 |
| J8458 | USB2_PHY | USB2 | USB2_EXTD_MUXED_F_P | 46 |
| J8458 | USB2_PHY | USB2 | USB2_EXTD_MUXED_F_N | 46 |
| Camera (U4200) | | | | |
| J8375 USB2_CONN_INT | USB2_PHY | USB2 | USB_CAMERA_P | 42 |
| J8376 USB2_CONN_INT | USB2_PHY | USB2 | USB_CAMERA_N | 42 |
| PCH USB Compensation | | | | |
| J8385 | PCH_50S | COMP_PCH | PCH_USB_RBIAS | 20 |

| Electrical Contraint Set | Physical | Spacing | Voltage | | |
|---|---|---|---|---|---|
| Camera Controller Local Ground | | | | | |
| J8972 | GND_PHY | GND | 0V | CAM_AGND | 42 |
| J8972 | GND_PHY | GND | 0V | CAM_PLLGND | 42 |

## USB Hub

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| USB 2.0 Hub | | | | |
| J4400 USB2_HUB_PCH | USB2_PHY | USB2 | USB_PCH_7_P | 20 27 |
| J4400 USB2_HUB_PCH | USB2_PHY | USB2 | USB_PCH_7_N | 20 27 |
| J4400 USB2_HUB_BT | USB2_PHY | USB2 | USB_BT_P | 27 35 |
| J4410 USB2_HUB_BT | USB2_PHY | USB2 | USB_BT_N | 27 35 |
| J4500 USB2_HUB_BT | USB2_PHY | USB2 | USB_BT_MUX_P | 35 |
| J4500 USB2_HUB_BT | USB2_PHY | USB2 | USB_BT_MUX_N | 35 |
| J4414 | USB_HUB_PHY | USB_HUB | USB_HUB_2P | 27 |
| J4412 | USB_HUB_PHY | USB_HUB | USB_HUB_2N | 27 |
| USB 2.0 Hub Misc. | | | | |
| J8510 | USB_HUB_PHY | USB_HUB | USB_HUB_RESET_L | 27 |
| J8520 | USB_HUB_PHY | USB_HUB | USB_HUB_VBUS_DET | 27 |
| J8511 | USB_HUB_PHY | USB_HUB | USB_HUB_NON_REM0 | 27 |
| J8521 | USB_HUB_PHY | USB_HUB | USB_HUB_NON_REM1 | 27 |
| J8517 | USB_HUB_PHY | USB_HUB | USB_HUB_HS_IND | 27 |
| USB 2.0 Hub Compensation | | | | |
| J4472 | PCH_50S | COMP_PCH | USB_HUB_RBIAS | 27 |
| USB 2.0 Hub Crystal | | | | |
| J4472 | CLK_XTAL | XTAL | USB_HUB_XTAL1 | 27 |
| J4474 | CLK_XTAL | XTAL | USB_HUB_XTAL2 | 27 |
| J8515 | CLK_XTAL | XTAL | USB_HUB_XTAL2_R | 27 |

## Camera Controller

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| SMIA | | | | |
| J8482 SMIA_DATA | SMIA_DIFF_PHY | SMIA_DIFF | SMIA_DATA_P | 42 |
| J8482 SMIA_DATA | SMIA_DIFF_PHY | SMIA_DIFF | SMIA_DATA_N | 42 |
| J8524 SMIA_CLK | SMIA_DIFF_PHY | SMIA_DIFF | SMIA_CLK_P | 42 |
| J8524 SMIA_CLK | SMIA_DIFF_PHY | SMIA_DIFF | SMIA_CLK_N | 42 |
| MISC | | | | |
| J8507 | SPI_50S | SPI | CAM_SF_CLK | 42 |
| J8508 | SPI_50S | SPI | CAM_SF_CLK_R | 42 |
| J8509 | SPI_50S | SPI | CAM_SF_DIN | 42 |
| J8510 | SPI_50S | SPI | CAM_SF_DIN_R | 42 |
| J8511 | SPI_50S | SPI | CAM_SF_CS_L | 42 |
| J8513 | SPI_50S | SPI | CAM_SF_WP_L | 42 |
| J8512 | SPI_50S | SPI | CAM_SF_DOUT | 42 |
| J8514 | SPI_50S | SPI | CAM_SF_DOUT_R | 42 |
| J8480 | SPI_50S | SPI | CAM_SF_HOLD_L | 42 |
| J8524 | CAM_PHY | CAM | CAM_USB_VRES | 42 |
| J8524 | CAM_PHY | CAM | MIPI_RESISTOR | 42 |
| J8530 | | PM | CAM_EXT_BOOT_L | 43 |
| J8531 | | PM | PCH_CAM_EXT_BOOT_R_L | 21 43 |
| J8537 | | PM | CAM_P1V2_RST_HOLDOFF | 43 |
| J8538 | | PM | CAM_P1V2_RST_HOLDOFF_L | 43 |
| I2C | | | | |
| J8534 | SMB_PHY | SMB | I2C_CAMSENSOR_SDA | 42 |
| J8535 | SMB_PHY | SMB | I2C_CAMSENSOR_SCL | 42 |
| J8532 | SMB_PHY | SMB | SMB_ALS_F_SDA | 42 |
| J8533 | SMB_PHY | SMB | SMB_ALS_F_SCL | 42 |
| Camera Controller Crystal | | | | |
| J8926 | CLK_XTAL | XTAL | CAM_XTAL_IN | 42 |
| J8926 | CLK_XTAL | XTAL | CAM_XTAL_OUT | 42 |
| J8927 | CLK_XTAL | XTAL | CAM_XTAL_OUT_R | 42 |

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USB/Camera Constraints

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## SMBus

### SMBus-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| SMB_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SMB_PHY | * | SMB_55S |

### SMBus-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SMB_ISO | * | =2x_DIELECTRIC | ? |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SMB | * | * | SMB_ISO |

## Sensor

### Sensor-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| 1:1_DIFFPAIR | * | Y | =STANDARD | =STANDARD | =STANDARD | 0.1 MM | 0.085 MM |
| SNS_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

### Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| SNS_DIFF_PHY | * | 1:1_DIFFPAIR |
| SNS_PHY | * | SNS_50S |

### Sensor-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SENSE_ISO | * | =4:1_SPACING | ? |

### Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SENSE | * | * | SENSE_ISO |
| SENSE | POWER | * | PWR_P2MM |
| SENSE | GND | * | GND_P2MM |




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# DC-DC

## Power-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| GND_P3MM | * | Y | 0.300 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |
| GND_P5MM | * | Y | 0.500 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |
| POWER_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| POWER_P3MM | * | Y | 0.300 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |
| POWER_P6MM | * | Y | 0.600 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |
| POWER_P5MM | * | Y | 0.500 MM | 0.200 MM | 3.0 MM | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| VR_CTL_PHY | * | POWER_P5MM |
| VR_CTL_PHY | BGA | STANDARD |
| VR_VID_PHY | * | POWER_50S |
| POWER_PHY | * | POWER_P6MM |
| GND_PHY | * | GND_P5MM |

## Constraints
## Power and Common

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| POWER | * | * | POWER_ISO |
| GND | * | * | GND_ISO |

## Power-specific Spacing Definitions
## Power and Common

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| POWER_ISO | * | =STANDARD | ? |

## DC-DC Baddies

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| VR_SWITCH | * | * | SWNODE_ISO |
| VR_SWITCH | * | BGA | BGA_P1MM |
| VR_SWITCH | VR_SWITCH | * | SWNODE_SW2SW |
| VR_SWITCH | POWER | * | SWNODE_SW2PWR |
| VR_SWITCH | GND | * | SWNODE_SW2GND |
| VR_LGATE | * | * | SWNODE_ISO |
| VR_LGATE | VR_SWITCH | * | SWNODE_LG2SW |

## DC-DC Baddies

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SWNODE_ISO | * | =8:1_SPACING | 1000 |
| SWNODE_SW2SW | * | =1:1_SPACING | ? |
| SWNODE_SW2PWR | * | =2:1_SPACING | ? |
| SWNODE_SW2GND | * | =2:1_SPACING | ? |
| SWNODE_LG2SW | * | =3:1_SPACING | ? |

## DC-DC Control

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| VR_CTL | * | * | VR_CTL_ISO |
| VR_VID | * | * | VR_VID_ISO |

## DC-DC Control

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| VR_CTL_ISO | * | =3:1_SPACING | ? |
| VR_VID_ISO | * | =4X_DIELECTRIC | ? |

## CPU VccSA

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| Input Bus | | | | | | | |
| I24 | POWER_PHY | POWER | 5V | | | REG_VCC_U7500 | 70 |
| I25 | POWER_PHY | POWER | 5V | | | REG_PVCC_U7500 | 70 |
| Local Ground | | | | | | | |
| I26 | GND_PHY | GND | 0V | | | AGND_VCCSAS0 | 70 |
| VCCIO | | | | | | | |
| I27 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_VCCSAS0 | 70 |
| I28 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_VCCSAS0 | 70 |
| I29 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_VCCSAS0_RC | 70 |
| I31 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_VCCSAS0 | 70 |
| I30 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_VCCSAS0 | 70 |
| I33 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_VCCSAS0 | 70 |
| I32 | VR_CTL_PHY | VR_CTL | | | | REG_VCCSAS0_OCSET | 70 |
| I35 | VR_CTL_PHY | VR_CTL | | | | REG_VCCSAS0_VO | 70 |
| I34 | | SENSE | | | | SNS_CPU_VCCSA | 13 70 |
| I37 VSNS_CPU_VCCSA | SNS_DIFF_PHY | SENSE | | | | SNS_VCCSAS0_XW_P | 70 |
| I36 VSNS_CPU_VCCSA | SNS_DIFF_PHY | SENSE | | | | SNS_VCCSAS0_XW_N | 70 |
| I38 | | SENSE | | | | REG_VCCSAS0_FB | 70 |
| I39 | | SENSE | | | | REG_VCCSAS0_RTN | 70 |
| I40 | VR_CTL_PHY | VR_CTL | | | | REG_VCCSAS0_SREF | 70 |
| I41 | VR_CTL_PHY | VR_CTL | | | | REG_VCCSAS0_FSEL | 70 |
| Output Bus | | | | | | | |
| I42 | POWER_PHY | POWER | 0.925V | | | PPVCCSA_S0 | 6 |

## CPU VccIO PCH 1.05V S0

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| Input Bus | | | | | | | |
| I1 | POWER_PHY | POWER | 5V | | | REG_VCC_U7400 | 69 |
| I2 | POWER_PHY | POWER | 5V | | | REG_PVCC_U7400 | 69 |
| Local Ground | | | | | | | |
| I3 | GND_PHY | GND | 0V | | | AGND_CPU_P1V05S0 | 69 |
| 1.05V S0 | | | | | | | |
| I5 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_CPU_PHASE_P1V05S0 | 69 |
| I7 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_CPU_BOOT_P1V05S0 | 69 |
| I6 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_CPU_BOOT_P1V05S0_RC | 69 |
| I8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_CPU_UGATE_P1V05S0 | 69 |
| I9 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_CPU_UGATE_P1V05S0_R | |
| I10 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_CPU_LGATE_P1V05S0 | 69 |
| I12 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_CPU_SNUBBER_P1V05S0 | 69 |
| I11 | VR_CTL_PHY | VR_CTL | | | | REG_CPU_P1V05S0_OCSET | 69 |
| I14 | VR_CTL_PHY | VR_CTL | | | | REG_CPU_P1V05S0_VO | 69 |
| I13 VSNS_CPU_VCCIO | SNS_DIFF_PHY | SENSE | | | | SNS_CPU_VCCIO_P | 13 69 |
| I15 VSNS_CPU_VCCIO | SNS_DIFF_PHY | SENSE | | | | SNS_CPU_VCCIO_N | 13 69 |
| I16 | SNS_DIFF_PHY | SENSE | | | | SNS_CPU_P1V05S0_XW_P | 69 |
| I17 | SNS_DIFF_PHY | SENSE | | | | SNS_CPU_P1V05S0_XW_N | 69 |
| I19 | | SENSE | | | | REG_CPU_P1V05S0_FB | 69 |
| I18 | | SENSE | | | | REG_CPU_P1V05S0_RTN | 69 |
| I21 | VR_CTL_PHY | VR_CTL | | | | REG_CPU_P1V05S0_SREF | 69 |
| I20 | VR_CTL_PHY | VR_CTL | | | | REG_CPU_P1V05S0_FSEL | 69 |
| Output Bus | | | | | | | |
| I22 | POWER_PHY | POWER | 1.05V | | | PP1V05_S0_CPU | 6 |

## PCH/GPU/TBT 1.05V S0

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| Input Bus | | | | | | | |
| I44 | POWER_PHY | POWER | 5V | | | REG_VCC_UB700 | 99 |
| Local Ground | | | | | | | |
| I46 | GND_PHY | GND | 0V | | | P1V05_AGND | 99 |
| 1.05V S0 | | | | | | | |
| I47 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_P1V05S0 | 99 |
| I48 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_P1V05S0_L | 99 |
| I49 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_P1V05S0 | 99 |
| I50 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_P1V05S0_RC | 99 |
| I51 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_P1V05S0 | 99 |
| I52 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_P1V05S0_R | 99 |
| I53 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_P1V05S0 | 99 |
| I54 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_P1V05S0 | 99 |
| I55 | VR_CTL_PHY | VR_CTL | | | | REG_P1V05S0_OCSET | 99 |
| I56 | VR_CTL_PHY | VR_CTL | | | | REG_P1V05S0_VO | 99 |
| I72 | POWER_PHY | VR_SWITCH | 12V | | | REG_P1V05S0_VO_R | 99 |
| I73 | POWER_PHY | VR_SWITCH | 12V | | | P1V05_OCSET_R | 99 |
| I61 | | SENSE | | | | REG_P1V05S0_FB | 99 |
| I62 | | SENSE | | | | REG_P1V05S0_RTN | 99 |
| I63 | VR_CTL_PHY | VR_CTL | | | | REG_P1V05S0_SREF | 99 |
| I64 | VR_CTL_PHY | VR_CTL | | | | REG_P1V05S0_FSEL | 99 |
| Output Bus | | | | | | | |
| I68 | POWER_PHY | POWER | 1.05V | | | PP1V05_S0_PCH | 6 |
| I69 | POWER_PHY | POWER | 1.05V | | | PP1V05_S0 | 6 |
| FET Switched | | | | | | | |
| I67 | POWER_PHY | POWER | 1.05V | | | PP1V05_TBTLC | 6 38 |
| I66 | POWER_PHY | POWER | 1.05V | | | PP1V05_TBTCIQ | 6 |

SYNC_MASTER=D8_MLB SYNC_DATE=07/03/2012

PAGE TITLE
# VReg Constraints

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

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## CPU Core Phases

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | | |
| 1G10 | POWER_PHY | POWER | 12V | | | PP12V_S0_CPUCORE_FLT | 66 67 68 |
| 1H10 | POWER_PHY | POWER | 5V | | | REG_VCC_U7100 | 66 |
| **Local Ground** | | | | | | | |
| 1H20 | GND_PHY | GND | 0V | | | AGND_CPU | 66 67 68 |
| **Phase 1** | | | | | | | |
| 1G8 | POWER_PHY | POWER | 12V | | | REG_LVCC_U7210 | 67 |
| 1G6 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUCORE_1 | 66 67 |
| 1G5 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUCORE_1_R | 66 |
| 1G7 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUCORE_1 | 67 |
| 1G8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_CPUCORE_1 | 67 |
| 1G8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_CPUCORE_1_RC | 67 |
| 1G8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_CPUCORE_1 | 67 |
| 1G8 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_CPUCORE_1 | 67 |
| 1G8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_CPUCORE_1 | 67 |
| 1G9 | POWER_PHY | POWER | 1.1V | | | PPCPUCORE_S0_SENSE_1 | 67 |
| 1G8 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENCORE_1_P | 66 67 |
| 1G8 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENCORE_1_N | 67 |
| 1G8 | | SENSE | | | | REG_ISENCORE_1_NR | 66 67 |
| **Phase 2** | | | | | | | |
| 1H8 | POWER_PHY | POWER | 12V | | | REG_LVCC_U7230 | 67 |
| 1H6 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUCORE_2 | 66 67 |
| 1H5 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUCORE_2_R | 66 |
| 1H7 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUCORE_2 | 67 |
| 1H8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_CPUCORE_2 | 67 |
| 1H8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_CPUCORE_2_RC | 67 |
| 1H8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_CPUCORE_2 | 67 |
| 1H8 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_CPUCORE_2 | 67 |
| 1H8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_CPUCORE_2 | 67 |
| 1H9 | POWER_PHY | POWER | 1.1V | | | PPCPUCORE_S0_SENSE_2 | 67 |
| 1H8 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENCORE_2_P | 66 67 |
| 1H8 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENCORE_2_N | 67 |
| 1H8 | | SENSE | | | | REG_ISENCORE_2_NR | 66 67 |
| **Phase 3** | | | | | | | |
| 1J8 | POWER_PHY | POWER | 12V | | | REG_LVCC_U7250 | 67 |
| 1J6 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUCORE_3 | 66 67 |
| 1J5 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUCORE_3_R | 66 |
| 1J7 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUCORE_3 | 67 |
| 1J8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_CPUCORE_3 | 67 |
| 1J8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_CPUCORE_3_RC | 67 |
| 1J8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_CPUCORE_3 | 67 |
| 1J8 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_CPUCORE_3 | 67 |
| 1J8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_CPUCORE_3 | 67 |
| 1J9 | POWER_PHY | POWER | 1.1V | | | PPCPUCORE_S0_SENSE_3 | 67 |
| 1J8 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENCORE_3_P | 66 67 |
| 1J8 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENCORE_3_N | 67 |
| 1J8 | | SENSE | | | | REG_ISENCORE_3_NR | 66 67 |
| **Phase 4** | | | | | | | |
| 1K8 | POWER_PHY | POWER | 12V | | | REG_LVCC_U7310 | 68 |
| 1K7 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUCORE_4 | 66 68 |
| 1K5 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUCORE_4_R | 66 |
| 1K7 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUCORE_4 | 68 |
| 1K8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_CPUCORE_4 | 68 |
| 1K8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_CPUCORE_4_RC | 68 |
| 1K8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_CPUCORE_4 | 68 |
| 1K8 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_CPUCORE_4 | 68 |
| 1K8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_CPUCORE_4 | 68 |
| 1K9 | POWER_PHY | POWER | 1.1V | | | PPCPUCORE_S0_SENSE_4 | 68 |
| 1K8 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENCORE_4_P | 66 68 |
| 1K8 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISENCORE_4_N | 68 |
| 1K8 | | SENSE | | | | REG_ISENCORE_4_NR | 66 68 |
| 1L20 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_CORE_XW_P | 66 |
| 1L20 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_CORE_XW_N | 66 |
| 1L20 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_CORE_R_P | 66 |
| 1L20 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_CORE_R_N | 66 |
| 1L22 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_CPU_VAXG_P | 13 66 |
| 1L22 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_CPU_VAXG_N | 13 66 |
| 1L22 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_CPU_VCORE_P | 13 66 |
| 1L22 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_CPU_VCORE_N | 13 66 |
| 1L22 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_P1V05_IOVDD_XW_P | 99 |
| 1L22 ISNS_CPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_P1V05_IOVDD_XW_N | 99 |

## CPU AXG Phase and Core Controller

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **AXG** | | | | | | | |
| 1E10 | POWER_PHY | POWER | 12V | | | REG_LVCC_U7330 | 68 |
| 1E8 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUAXG | 66 68 |
| 1E6 | VR_CTL_PHY | VR_CTL | | | | REG_PWM_CPUAXG_R | 66 |
| 1E7 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_CPUAXG | 68 |
| 1E8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_CPUAXG | 68 |
| 1E8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_CPUAXG_RC | 68 |
| 1E8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_CPUAXG | 68 |
| 1E8 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_CPUAXG | 68 |
| 1E8 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_CPUAXG | 68 |
| 1E9 | POWER_PHY | POWER | 1.1V | | | PPCPUAXG_S0_SENSE | 68 |
| 1E8 ISNS_CPU_AXG | SNS_DIFF_PHY | SENSE | | | | REG_ISENAXG_P | 68 |
| 1E8 ISNS_CPU_AXG | SNS_DIFF_PHY | SENSE | | | | REG_ISENAXG_N | 68 |
| 1E8 | | SENSE | | | | REG_ISENAXG_PR | 66 68 |
| 1E8 | | SENSE | | | | REG_ISENAXG_NR | 66 68 |
| 1E22 ISNS_CPU_AXG | SNS_DIFF_PHY | SENSE | | | | SNS_AXG_R_P | 66 |
| 1E22 ISNS_CPU_AXG | SNS_DIFF_PHY | SENSE | | | | SNS_AXG_R_N | 66 |
| 1E22 ISNS_CPU_AXG | SNS_DIFF_PHY | SENSE | | | | SNS_AXG_XW_P | 66 |
| 1E22 ISNS_CPU_AXG | SNS_DIFF_PHY | SENSE | | | | SNS_AXG_XW_N | 66 |
| **ISL6364** | | | | | | | |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_COMP | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUCORE_COMP_RC | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_FB | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUCORE_FB_RC | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUCORE_FB_R_1 | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUCORE_FB_R_2 | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUCORE_PSICOMP_RC | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_PSICOMP | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_HFCOMP | 66 |
| 1E10 | | SENSE | | | | REG_CPUCORE_VSEN | 66 |
| 1E10 | | SENSE | | | | REG_CPUCORE_RGND | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_IMON | 51 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUCORE_IMON_R | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_TM | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_SUTH | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_NPSI | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_FDVID | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_IAUTO | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_SW_FREQ | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_RAMPADJ | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_EN_PWR | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUCORE_EN_PWR_R | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUCORE_RSET | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUAXG_COMP | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUAXG_COMP_RC | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUAXG_FB | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUAXG_FB_RC | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUAXG_FB_R_1 | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUAXG_FB_R_2 | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUAXG_HFCOMP | 66 |
| 1E10 | | SENSE | | | | REG_CPUAXG_VSEN | 66 |
| 1E10 | | SENSE | | | | REG_CPUAXG_RGND | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUAXG_IMON | 51 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | CPUAXG_IMON_R | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUAXG_TM | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUAXG_TCOMP | 66 |
| 1E10 | VR_CTL_PHY | VR_CTL | | | | REG_CPUAXG_SW_FREQ | 66 |
| 1E10 | VR_VID_PHY | VR_VID | | | | CPU_VIDSCLK | 13 66 |
| 1E10 | VR_VID_PHY | VR_VID | | | | CPU_VIDSCLK_R | 13 |
| 1E10 | VR_VID_PHY | VR_VID | | | | CPU_VIDALERT_L | 13 66 |
| 1E10 | VR_VID_PHY | VR_VID | | | | CPU_VIDALERT_R_L | 13 |
| 1E10 | VR_VID_PHY | VR_VID | | | | CPU_VIDSOUT | 13 66 |
| 1E10 | VR_VID_PHY | VR_VID | | | | CPU_VIDSOUT_R | 13 |
| **Output Bus** | | | | | | | |
| 1E10 | POWER_PHY | POWER | 1.1V | | | PPVCORE_S0_CPU | 6 |
| 1E10 | POWER_PHY | POWER | 1.1V | | | PPVAXG_S0 | 6 |

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## 3.3V S5/5V S4

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | | |
| 1814 | POWER_PHY | POWER | 12V | | | REG_VIN_U7600 | 71 |
| 1812 | POWER_PHY | POWER | 5V | | | REG_VCC1_U7600 | 71 |
| 1812 | POWER_PHY | POWER | 5V | | | REG_VCC2_U7600 | 71 |
| **3.3V S5** | | | | | | | |
| 1810 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_P3V3S5 | 71 |
| 1814 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_P3V3S5 | 71 |
| 1814 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_P3V3S5_RC | 71 |
| 1810 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_P3V3S5 | 71 |
| 1810 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_P3V3S5 | 71 |
| 1810 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_P3V3S5 | 71 |
| 1814 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_ISEN | 71 |
| 1814 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_OCSET | 71 |
| 1814 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_FSET | 71 |
| 1814 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_VOUT | 71 |
| 1814 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_VOUT_R | 71 |
| 1814 | VR_CTL_PHY | VR_CTL | | | | REG_P3V3S5_FB | 71 |
| **5V S3** | | | | | | | |
| 1816 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_P5VS4 | 71 |
| 1816 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_P5VS4 | 71 |
| 1816 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_P5VS4_RC | 71 |
| 1816 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_P5VS4 | 71 |
| 1816 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_P5VS4 | 71 |
| 1816 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_P5VS4 | 71 |
| 1816 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_ISEN | 71 |
| 1816 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_OCSET | 71 |
| 1816 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_FSET | 71 |
| 1816 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_VOUT | 71 |
| 1816 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_VOUT_R | 71 |
| 1816 | VR_CTL_PHY | VR_CTL | | | | REG_P5VS4_FB | 71 |
| **Output Bus** | | | | | | | |
| 1816 | POWER_PHY | POWER | 5V | | | PP5V_S5 | 6 |
| 1816 | POWER_PHY | POWER | 5V | | | PP5V_S4 | 6 |
| 1816 | POWER_PHY | POWER | 3.3V | | | PP3V3_S5 | 6 |
| **FET Switched** | | | | | | | |
| 1818 | POWER_PHY | POWER | 5V | | | PP5V_S0 | 6 |
| 1818 | POWER_PHY | POWER | 3.3V | | | PP3V3_S4 | 6 60 |
| 1818 | POWER_PHY | POWER | 3.3V | | | PP3V3_S0 | 6 |
| 1818 | POWER_PHY | POWER | 3.3V | | | PP3V3_S4_ENET | 6 |
| 1818 | POWER_PHY | POWER | 3.3V | | | PP3V3_TBTLC | 6 |
| 1818 | POWER_PHY | POWER | 3.3V | | | PP3V3_S4_AP | 6 |
| 1818 | POWER_PHY | POWER | 3.3V | | | PP3V3_S0_SSD | 6 |

## VDDQ S3 (1.5V)/VTT S0

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | | |
| 1820 | POWER_PHY | POWER | 5V | | | REG_V5IN_U7700 | 72 |
| **Local Ground** | | | | | | | |
| 1822 | GND_PHY | GND | 0V | | | AGND_VDDQS3 | 72 |
| **VDDQ S3** | | | | | | | |
| 1826 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_VDDQS3 | 72 |
| 1826 | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_VDDQS3_L | 72 |
| 1826 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_VDDQS3 | 72 |
| 1826 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_VDDQS3_RC | 72 |
| 1826 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_VDDQS3 | 72 |
| 1826 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_VDDQS3_R | 72 |
| 1826 | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_VDDQS3 | 72 |
| 1826 | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_SNUBBER_VDDQS3 | 72 |
| 1828 | POWER_PHY | POWER | 1.5V | | | PPVDDQ_S3_SENSE | |
| 1826 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_VDDQSNS | 72 |
| 1826 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_VREF | 72 |
| 1826 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_REFIN | 72 |
| 1826 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_MODE | 72 |
| 1826 | VR_CTL_PHY | VR_CTL | | | | REG_VDDQS3_TRIP | 72 |
| 1826 | VR_CTL_PHY | VR_CTL | | | | LDO_DDRVTTS0_SNS | 72 |
| **Output Bus** | | | | | | | |
| 1828 | POWER_PHY | POWER | 1.5V | | | PPVDDQ_S3 | 6 |
| 1828 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | PPDDRVTT_S0 | 6 |
| **FET Switched** | | | | | | | |
| 1830 | POWER_PHY | POWER | 1.5V | | | PP1V5_S0 | 6 |
| **Sensed** | | | | | | | |
| 1830 | POWER_PHY | POWER | 1.5V | | | PPVDDQ_S3_DDR | 6 |
| 1830 | POWER_PHY | POWER | 1.5V | | | PP1V5_S0_CPU_MEM | 6 |
| 1830 | POWER_PHY | POWER | 1.5V | | | PPFBVDDQ_S0_GPU | 6 |

## DDR3 Vref

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **Memory Vref** | | | | | | | |
| 1838 | POWER_PHY | POWER | 3.3V | | | PP3V3_S4_VREFMRGN_DAC | 34 |
| 1838 | POWER_PHY | POWER | 3.3V | | | PP3V3_S4_VREFMRGN_CTRL | 34 |
| 1838 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | PPDDRVREF_DQ_MEM_A_S3 | 6 |
| 1838 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | PPDDRVREF_DQ_MEM_B_S3 | 6 |
| 1841 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | CPU_DIMM_VREF_DAC_A | 11 34 |
| 1841 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | CPU_DIMM_VREF_DAC_B | 11 34 |
| 1838 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | PPDDRVREF_CA_MEM_A_S3 | 6 |
| 1838 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | PPDDRVREF_CA_MEM_B_S3 | 6 |
| 1838 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | CPU_DDR_VREF | 11 |
| 1840 | POWER_DDR_PHY | POWER_DDR | 0.75V | | | PPDDRVTT_S3 | 6 |

## 1.8V S0

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **1.8V S0** | | | | | | | |
| 1110 | POWER_PHY | VR_SWITCH | 5V | TRUE | | REG_PHASE_P1V8S0 | 72 |
| 1110 | VR_CTL_PHY | VR_CTL | | | | REG_P1V8S0_VFB | 72 |
| 1110 | VR_CTL_PHY | VR_CTL | | | | REG_P1V8S0_SYNCH | 72 |
| **Output Bus** | | | | | | | |
| 1110 | POWER_PHY | POWER | 1.8V | | | PP1V8_S0 | 6 |

## HDD S0

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **HDD S0** | | | | | | | |
| 1830 | POWER_PHY | POWER | 5V | | | PP5V_S0_HDD | 6 |

## 12V S5

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | | |
| 1138 | POWER_PHY | POWER | 12V | | | PP12V_ACDC | 6 |
| **FET Switched** | | | | | | | |
| 1138 | POWER_PHY | POWER | 12V | | | PP12V_S0 | 6 |
| **Sensed** | | | | | | | |
| 1138 | POWER_PHY | POWER | 12V | | | PP12V_S5 | 6 |
| 1138 | POWER_PHY | POWER | 12V | | | PP12V_G3H | 6 |
| 1141 | POWER_PHY | POWER | 12V | | | PP12V_G3H_P3V42 | 73 |
| 1140 | POWER_PHY | POWER | 12V | | | PP12V_S0_FBVDDQ | 6 |
| 1140 | POWER_PHY | POWER | 12V | | | PP12V_S0_CPU_P1V05 | 6 |
| 1140 | POWER_PHY | POWER | 12V | | | PP12V_S0_VCCSA | 6 |
| 1140 | POWER_PHY | POWER | 12V | | | PP12V_S0_P1V05 | 6 |
| 1138 | POWER_PHY | POWER | 12V | | | PP12V_S0_HDD | 6 |
| 1140 | POWER_PHY | POWER | 12V | | | PP12V_S0_BLC | 6 |

## Ground/Common

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **Common** | | | | | | | |
| 1138 | GND_PHY | GND | 0V | | | GND | |

## 3V42 S0

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **3V42 S0** | | | | | | | |
| 1138 | POWER_PHY | VR_SWITCH | 5V | TRUE | | P3V42G3H_SW | 73 |
| 1138 | VR_CTL_PHY | VR_CTL | | | | P3V42G3H_FB | 73 |
| 1138 | VR_CTL_PHY | VR_CTL | | | | P3V42G3H_SHDN_L | 73 |
| 1138 | POWER_PHY | POWER | 3.3V | | | PP3V3_G3 | 6 |
| 1138 | POWER_PHY | POWER | 3.3V | | | PP3V42_G3H | 6 |

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PAGE TITLE
# Platform VReg Constraints

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# Thunderbolt

## Thunderbolt-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| TBT_I2C_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| TBT_SPI_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |
| TBTDP_90D | * | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | =90_OHM_DIFF | 0.075MM |
| TBT_GEN_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

## Thunderbolt-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| TBT_I2C_ISO | * | =2x_DIELECTRIC | ? |
| TBT_SPI_ISO | * | =2x_DIELECTRIC | ? |
| TBTDP_ISO | * | =5x_DIELECTRIC | ? |
| TBTDP_ISO | TOP,BOTTOM | =7x_DIELECTRIC | ? |
| TBT_GEN_ISO | * | =2X_DIELECTRIC | ? |
| BGA_TBT_AREA | * | 0.075MM | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| * | * | BGA_TBT | BGA_TBT_AREA |
| TBT_I2C | * | * | TBT_I2C_ISO |
| TBT_SPI | * | * | TBT_SPI_ISO |
| TBTDP | * | * | TBTDP_ISO |
| TBT_GEN | * | * | TBT_GEN_ISO |

SOURCE: Bill Cornelius's T29 Routing Notes

# DisplayPort

## DP-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| DP_85D | * | =85_OHM_DIFF | =85_OHM_DIFF | 0.08MM | =85_OHM_DIFF | =85_OHM_DIFF | =85_OHM_DIFF |

## DP-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| DP_ISO | * | =6.7X_DIELECTRIC | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| DISPLAYPORT | * | * | DP_ISO |

MAX LENGTH OF DISPLAYPORT TRACES: 6 INCHES

DISPLAYPORT INTRA-PAIR MATCHING SHOULD BE 1 PS. INTER-PAIR MATCHING SHOULD BE WITHIN 150 PS.
DISPLAYPORT AUX CHANNEL INTRA-PAIR MATCHING SHOULD BE 5 PS.

## TBT IC Net Properties

| Electrical Contraint Set | Physical | Spacing | | | | |
|---|---|---|---|---|---|---|
| 1631 | DP_85D | DISPLAYPORT | DP_TBTSNK0_ML_C_P<3..0> | NO_TEST=TRUE | 36 | 90 |
| 1632 | DP_85D | DISPLAYPORT | DP_TBTSNK0_ML_C_N<3..0> | NO_TEST=TRUE | 36 | 90 |
| 1633 DP_TBTSNK0_ML | DP_85D | DISPLAYPORT | DP_TBTSNK0_ML_P<3..0> | NO_TEST=TRUE | 36 | |
| 1634 DP_TBTSNK0_ML | DP_85D | DISPLAYPORT | DP_TBTSNK0_ML_N<3..0> | NO_TEST=TRUE | 36 | |
| 1635 | DP_85D | DISPLAYPORT | DP_TBTSNK0_AUXCH_C_P | | 36 | 90 |
| 1636 | DP_85D | DISPLAYPORT | DP_TBTSNK0_AUXCH_C_N | | 36 | 90 |
| 1637 DP_TBTSNK0_AUX | DP_85D | DISPLAYPORT | DP_TBTSNK0_AUXCH_P | | 36 | |
| 1638 DP_TBTSNK0_AUX | DP_85D | DISPLAYPORT | DP_TBTSNK0_AUXCH_N | | 36 | |
| 1639 | DP_85D | DISPLAYPORT | DP_TBTSNK1_ML_C_P<3..0> | NO_TEST=TRUE | 36 | 90 |
| 1640 | DP_85D | DISPLAYPORT | DP_TBTSNK1_ML_C_N<3..0> | NO_TEST=TRUE | 36 | 90 |
| 1641 DP_TBTSNK1_ML | DP_85D | DISPLAYPORT | DP_TBTSNK1_ML_P<3..0> | NO_TEST=TRUE | 36 | |
| 1642 DP_TBTSNK1_ML | DP_85D | DISPLAYPORT | DP_TBTSNK1_ML_N<3..0> | NO_TEST=TRUE | 36 | |
| 1643 | DP_85D | DISPLAYPORT | DP_TBTSNK1_AUXCH_C_P | | 36 | 90 |
| 1644 | DP_85D | DISPLAYPORT | DP_TBTSNK1_AUXCH_C_N | | 36 | 90 |
| 1645 DP_TBTSNK1_AUX | DP_85D | DISPLAYPORT | DP_TBTSNK1_AUXCH_P | | 36 | |
| 1646 DP_TBTSNK1_AUX | DP_85D | DISPLAYPORT | DP_TBTSNK1_AUXCH_N | | 36 | |
| 1680 DP_TNTPNL_TBT_ML_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_ML_P<3..0> | NO_TEST=TRUE | 75 | |
| 1681 DP_TNTPNL_TBT_ML_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_ML_N<3..0> | NO_TEST=TRUE | 75 | |
| 1686 DP_TNTPNL_TBT_ML_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_ML_C_P<3..0> | NO_TEST=TRUE | 75 | |
| 1687 DP_TNTPNL_TBT_ML_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_ML_C_N<3..0> | NO_TEST=TRUE | 75 | |
| 1682 DP_TNTPNL_TBT_AUX_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_AUXCH_P | | 75 | |
| 1683 DP_TNTPNL_TBT_AUX_MUX | DP_85D | DISPLAYPORT | DP_TBTSRC_AUXCH_N | | 75 | |
| 1688 | DP_85D | DISPLAYPORT | DP_TBTSRC_AUX_C_P | | 75 | |
| 1689 | DP_85D | DISPLAYPORT | DP_TBTSRC_AUX_C_N | | 75 | |
| 1631 | TBT_I2C_55S | TBT_I2C | I2C_TBTRTR_SCL | | 36 | 50 |
| 1632 | TBT_I2C_55S | TBT_I2C | I2C_TBTRTR_SDA | | 36 | 50 |
| 1633 TBT_SPI_CLK | TBT_I2C_55S | TBT_SPI | TBT_SPI_CLK | | 36 | |
| 1652 TBT_SPI_MOSI | TBT_I2C_55S | TBT_SPI | TBT_SPI_MOSI | | 36 | |
| 1634 TBT_SPI_MISO | TBT_I2C_55S | TBT_SPI | TBT_SPI_MISO | | 36 | |
| 1653 TBT_SPI_CS_L | TBT_I2C_55S | TBT_SPI | TBT_SPI_CS_L | | 36 | |
| 1688 | TBT_GEN_55S | TBT_GEN | TBT_A_CONFIG1_BUF | | 36 | 77 |
| 1689 | TBT_GEN_55S | TBT_GEN | TBT_A_CONFIG2_RC | | 36 | 77 |
| 1690 | TBT_GEN_55S | TBT_GEN | TBT_B_CONFIG1_BUF | | 36 | 79 |
| 1691 | TBT_GEN_55S | TBT_GEN | TBT_B_CONFIG2_RC | | 36 | 79 |
| 1692 | TBT_GEN_55S | TBT_GEN | TBT_A_LSTX | | 36 | 77 |
| 1693 | TBT_GEN_55S | TBT_GEN | TBT_A_LSRX | | 36 | 77 |
| 1694 | TBT_GEN_55S | TBT_GEN | TBT_B_LSTX | | 36 | 79 |
| 1695 | TBT_GEN_55S | TBT_GEN | TBT_B_LSRX | | 36 | 79 |
| 1696 | TBT_GEN_55S | TBT_GEN | DP_TBTSNK0_HPD | | 36 | 90 |
| 1697 | TBT_GEN_55S | TBT_GEN | DP_TBTSNK1_HPD | | 36 | 90 |
| 1698 | TBT_GEN_55S | TBT_GEN | DP_TBTSRC_HPD | | 36 | 75 |
| 1699 | TBT_GEN_55S | TBT_GEN | DP_TBTSNK0_DDC_CLK | | 76 | 92 |
| 1700 | TBT_GEN_55S | TBT_GEN | DP_TBTSNK0_DDC_DATA | | 76 | 92 |
| 1701 | TBT_GEN_55S | TBT_GEN | DP_TBTSNK1_DDC_CLK | | 76 | 91 |
| 1702 | TBT_GEN_55S | TBT_GEN | DP_TBTSNK1_DDC_DATA | | 76 | 91 |
| 1703 | TBT_GEN_55S | TBT_GEN | VIDEO_ON | | 74 | 78 |
| 1704 | TBT_GEN_55S | TBT_GEN | VIDEO_ON_L | | 5 | 78 |
| 1705 | TBT_GEN_55S | TBT_GEN | BDV_BKL_PWM | | 48 | 75 |
| 1706 | TBT_GEN_55S | TBT_GEN | GPU_LCD_BKLT_PWM | | 75 | 91 |
| 1707 | TBT_GEN_55S | TBT_GEN | LCD_BL_PWM | | 75 | |
| 1708 | TBT_GEN_55S | TBT_GEN | LCD_BL_FILT | | 75 | |
| 1709 | TBT_GEN_55S | TBT_GEN | LCD_BKLT_PWM | | 75 | 80 |

*: Only used on hosts supporting T29 video-in

## TBT/DP Net Properties

| Electrical Contraint Set | Physical | Spacing | | | | |
|---|---|---|---|---|---|---|
| Port A | | | | | | |
| 1641 TBT_A_R2D | TBTDP_90D | TBTDP | TBT_A_R2D_C_P<0> | NO_TEST=TRUE | 36 | 77 |
| 1642 TBT_A_R2D | TBTDP_90D | TBTDP | TBT_A_R2D_C_N<0> | NO_TEST=TRUE | 36 | 77 |
| 1729 TBT_A_R2D_PINV | TBTDP_90D | TBTDP | TBT_A_R2D_C_N<1> | NO_TEST=TRUE | 36 | 77 |
| 1730 TBT_A_R2D_PINV | TBTDP_90D | TBTDP | TBT_A_R2D_C_P<1> | NO_TEST=TRUE | 36 | 77 |
| 1643 | TBTDP_90D | TBTDP | TBT_A_R2D_P<1..0> | NO_TEST=TRUE | | 77 |
| 1644 | TBTDP_90D | TBTDP | TBT_A_R2D_N<1..0> | NO_TEST=TRUE | | 77 |
| 1646 DP_TBTPA_ML1 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_C_P<1> | NO_TEST=TRUE | 36 | 77 |
| 1645 DP_TBTPA_ML1 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_C_N<1> | NO_TEST=TRUE | 36 | 77 |
| 1648 DP_TBTPA_ML3 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_C_P<3> | NO_TEST=TRUE | 36 | 77 |
| 1647 DP_TBTPA_ML3 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_C_N<3> | NO_TEST=TRUE | 36 | 77 |
| 1649 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_P<1> | NO_TEST=TRUE | | 77 |
| 1647 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_N<1> | NO_TEST=TRUE | | 77 |
| 1650 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_P<3> | NO_TEST=TRUE | | 77 |
| 1650 | DP_85D | DISPLAYPORT | DP_TBTPA_ML_N<3> | NO_TEST=TRUE | | 77 |
| 1653 | DP_85D | DISPLAYPORT | DP_A_LSX_ML_P<1> | | | 77 |
| 1654 | DP_85D | DISPLAYPORT | DP_A_LSX_ML_N<1> | | | 77 |
| 1655 | TBTDP_90D | TBTDP | TBT_A_D2R_C_P<1..0> | NO_TEST=TRUE | | 77 |
| 1656 | TBTDP_90D | TBTDP | TBT_A_D2R_C_N<1..0> | NO_TEST=TRUE | | 77 |
| 1664 TBT_A_D2R1 | TBTDP_90D | TBTDP | TBT_A_D2R_P<1> | NO_TEST=TRUE | 36 | 77 |
| 1665 TBT_A_D2R1 | TBTDP_90D | TBTDP | TBT_A_D2R_N<1> | NO_TEST=TRUE | 36 | 77 |
| 1666 TBT_A_D2R0 | TBTDP_90D | TBTDP | TBT_A_D2R_P<0> | NO_TEST=TRUE | 36 | 77 |
| 1667 TBT_A_D2R0 | TBTDP_90D | TBTDP | TBT_A_D2R_N<0> | NO_TEST=TRUE | 36 | 77 |
| 1668 DP_TBT_A_AUXCH | DP_85D | DISPLAYPORT | DP_TBTPA_AUXCH_C_P | | 36 | 77 |
| 1669 DP_TBT_A_AUXCH | DP_85D | DISPLAYPORT | DP_TBTPA_AUXCH_C_N | | 36 | 77 |
| 1656 | DP_85D | DISPLAYPORT | DP_TBTPA_AUXCH_P | | | 77 |
| 1656 | DP_85D | DISPLAYPORT | DP_TBTPA_AUXCH_N | | | 77 |
| 1641 | DP_85D | DISPLAYPORT | DP_A_AUXCH_DDC_P | | | 77 |
| 1642 | DP_85D | DISPLAYPORT | DP_A_AUXCH_DDC_N | | | 77 |
| 1659 | TBTDP_90D | TBTDP | TBT_A_D2R1_AUXDDC_P | NO_TEST=TRUE | | 77 |
| 1661 | TBTDP_90D | TBTDP | TBT_A_D2R1_AUXDDC_N | NO_TEST=TRUE | | 77 |
| Port B | | | | | | |
| 1662 TBT_B_R2D | TBTDP_90D | TBTDP | TBT_B_R2D_C_P<1..0> | NO_TEST=TRUE | 36 | 79 |
| 1663 TBT_B_R2D | TBTDP_90D | TBTDP | TBT_B_R2D_C_N<1..0> | NO_TEST=TRUE | 36 | 79 |
| 1663 | TBTDP_90D | TBTDP | TBT_B_R2D_P<1..0> | NO_TEST=TRUE | | 79 |
| 1664 | TBTDP_90D | TBTDP | TBT_B_R2D_N<1..0> | NO_TEST=TRUE | | 79 |
| 1657 DP_TBTPB_ML1 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_C_P<1> | NO_TEST=TRUE | 36 | 79 |
| 1658 DP_TBTPB_ML1 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_C_N<1> | NO_TEST=TRUE | 36 | 79 |
| 1660 DP_TBTPB_ML3 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_C_P<3> | NO_TEST=TRUE | 36 | 79 |
| 1659 DP_TBTPB_ML3 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_C_N<3> | NO_TEST=TRUE | 36 | 79 |
| 1661 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_P<1> | NO_TEST=TRUE | | 79 |
| 1657 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_N<1> | NO_TEST=TRUE | | 79 |
| 1662 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_P<3> | NO_TEST=TRUE | | 79 |
| 1660 | DP_85D | DISPLAYPORT | DP_TBTPB_ML_N<3> | NO_TEST=TRUE | | 79 |
| 1658 | DP_85D | DISPLAYPORT | DP_B_LSX_ML_P<1> | NO_TEST=TRUE | | 79 |
| 1662 | DP_85D | DISPLAYPORT | DP_B_LSX_ML_N<1> | NO_TEST=TRUE | | 79 |
| 1671 | TBTDP_90D | TBTDP | TBT_B_D2R_C_P<1..0> | NO_TEST=TRUE | | 79 |
| 1672 | TBTDP_90D | TBTDP | TBT_B_D2R_C_N<1..0> | NO_TEST=TRUE | | 79 |
| 1673 TBT_B_D2R1 | TBTDP_90D | TBTDP | TBT_B_D2R_P<1> | NO_TEST=TRUE | 36 | 79 |
| 1674 TBT_B_D2R1 | TBTDP_90D | TBTDP | TBT_B_D2R_N<1> | NO_TEST=TRUE | 36 | 79 |
| 1675 TBT_B_D2R0 | TBTDP_90D | TBTDP | TBT_B_D2R_P<0> | NO_TEST=TRUE | 36 | 79 |
| 1677 TBT_B_D2R0 | TBTDP_90D | TBTDP | TBT_B_D2R_N<0> | NO_TEST=TRUE | 36 | 79 |
| 1668 DP_TBT_B_AUXCH | DP_85D | DISPLAYPORT | DP_TBTPB_AUXCH_C_P | | 36 | 79 |
| 1669 DP_TBT_B_AUXCH | DP_85D | DISPLAYPORT | DP_TBTPB_AUXCH_C_N | | 36 | 79 |
| 1656 | DP_85D | DISPLAYPORT | DP_TBTPB_AUXCH_P | | | 79 |
| 1670 | DP_85D | DISPLAYPORT | DP_TBTPB_AUXCH_N | | | 79 |
| 1668 | DP_85D | DISPLAYPORT | DP_B_AUXCH_DDC_P | | | 79 |
| 1672 | DP_85D | DISPLAYPORT | DP_B_AUXCH_DDC_N | | | 79 |
| 1674 | TBTDP_90D | TBTDP | TBT_B_D2R1_AUXDDC_P | NO_TEST=TRUE | | 79 |
| 1676 | TBTDP_90D | TBTDP | TBT_B_D2R1_AUXDDC_N | NO_TEST=TRUE | | 79 |

## DisplayPort

| Electrical Contraint Set | Physical | Spacing | | | | |
|---|---|---|---|---|---|---|
| Graphics Source | | | | | | |
| 1640 DP_INTPNL_EG_ML_MUX | DP_85D | DISPLAYPORT | DP_INT_EG_ML_P<3..0> | NO_TEST=TRUE | 75 | 90 |
| 1639 DP_INTPNL_EG_ML_MUX | DP_85D | DISPLAYPORT | DP_INT_EG_ML_N<3..0> | NO_TEST=TRUE | 75 | 90 |
| 1638 DP_INTPNL_EG_AUX_MUX | DP_85D | DISPLAYPORT | DP_INT_EG_AUX_P | NO_TEST=TRUE | 75 | 90 |
| 1637 DP_INTPNL_EG_AUX_MUX | DP_85D | DISPLAYPORT | DP_INT_EG_AUX_N | NO_TEST=TRUE | 75 | 90 |
| 1636 | DP_85D | DISPLAYPORT | DP_INT_EG_AUX_C_P | | 75 | |
| 1635 | DP_85D | DISPLAYPORT | DP_INT_EG_AUX_C_N | | 75 | |
| Internal Panel | | | | | | |
| 1690 | DP_85D | DISPLAYPORT | DP_INTPNL_ML_C_P<3..0> | NO_TEST=TRUE | 75 | |
| 1689 | DP_85D | DISPLAYPORT | DP_INTPNL_ML_C_N<3..0> | NO_TEST=TRUE | 75 | |
| 1687 DP_INTPNL_ML_CONN | DP_85D | DISPLAYPORT | DP_INTPNL_ML_P<3..0> | NO_TEST=TRUE | 75 | 78 |
| 1688 DP_INTPNL_ML_CONN | DP_85D | DISPLAYPORT | DP_INTPNL_ML_N<3..0> | NO_TEST=TRUE | 75 | 78 |
| 1690 DP_INTPNL_AUX_CONN | DP_85D | DISPLAYPORT | DP_INTPNL_AUX_P | | 75 | 78 |
| 1691 DP_INTPNL_AUX_CONN | DP_85D | DISPLAYPORT | DP_INTPNL_AUX_N | | 75 | 78 |
| Internal DP SPDIF | | | | | | |
| 1611 | | HDA | DP_INT_SPDIF_AUDIO | | 56 | 78 |

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# TBT/DP Constraints

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# GDDR5

## GDDR5-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| GDDR_45S | * | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =45_OHM_SE | =STANDARD | =STANDARD |
| GDDR_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | 12 MM | =STANDARD | =STANDARD |
| GDDR_80D | * | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF | =80_OHM_DIFF |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| GDDR_MA_PHY | * | GDDR_45S |
| GDDR_ADBI_PHY | * | GDDR_45S |
| GDDR_CTRL_PHY | * | GDDR_45S |
| GDDR_CLK_PHY | * | GDDR_80D |
| GDDR_DQ_PHY | * | GDDR_45S |
| GDDR_EDC_PHY | * | GDDR_45S |
| GDDR_DBI_PHY | * | GDDR_45S |
| GDDR_WCK_PHY | * | GDDR_80D |

## Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

| | Trace-to-Trace | | | | Isolation | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Table | Micro | Design | Strip | Design | Micro | Design | Strip | Design | Comments |
| 5-6/5-7 | 2:1 | 2:1 | 2:1 | 2:1 | 5:1 | 5:1 | 5:1 | 5:1 | Memory address (MA). Implented 4.5 Gbps or less rules for K70. |
| 5-6/5-7 | 2:1 | 2:1 | 2:1 | 2:1 | 5:1 | 5:1 | 5:1 | 5:1 | Address dynamic bus inversion (ADBI) |
| 5-6/5-7 | 2:1 | 2:1 | 2:1 | 2:1 | 5:1 | 5:1 | 5:1 | 5:1 | Control (CTRL) |
| 5-6/5-7 | 5:1 | 5:1 | 5:1 | 5:1 | 5:1 | 5:1 | 5:1 | 5:1 | Clock (CLK) |
| 5-6/5-7 | 3:1 | 3:1 | 3:1 | 3:1 | 5:1 | 5:1 | 5:1 | 5:1 | Data (DQ) |
| 5-6/5-7 | 7:1 | 7:1 | 7:1 | 7:1 | 7:1 | 7:1 | 7:1 | 7:1 | Error detection pins (EDC). Using larger isolation rules, |
| 5-6/5-7 | 3:1 | 3:1 | 3:1 | 3:1 | 5:1 | 5:1 | 5:1 | 5:1 | Data dynamic bus inversion (DBI) |
| 5-6/5-7 | 5:1 | 5:1 | 5:1 | 5:1 | 5:1 | 5:1 | 5:1 | 5:1 | Forwarded clock (WCK) |

## GDDR5-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GDDR_ISO | * | =3X_DIELECTRIC | ? |
| GDDR_ISO | TOP,BOTTOM | =5x_DIELECTRIC | ? |
| GDDR_MA2MA | * | =2x_DIELECTRIC | ? |
| GDDR_MA2MA | TOP,BOTTOM | =3X_DIELECTRIC | ? |
| GDDR_ADBI2ADBI | * | =2x_DIELECTRIC | ? |
| GDDR_ADBI2ADBI | TOP,BOTTOM | =2x_DIELECTRIC | ? |
| GDDR_CTRL2CTRL | * | =2x_DIELECTRIC | ? |
| GDDR_CTRL2CTRL | TOP,BOTTOM | =2x_DIELECTRIC | ? |
| GDDR_CLK2CLK | * | =3X_DIELECTRIC | ? |
| GDDR_CLK2CLK | TOP,BOTTOM | =5x_DIELECTRIC | ? |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| GDDR_DQ2DQ | * | =3x_DIELECTRIC | ? |
| GDDR_DQ2DQ | TOP,BOTTOM | =3x_DIELECTRIC | ? |
| GDDR_EDC_ISO | * | =3X_DIELECTRIC | ? |
| GDDR_EDC_ISO | TOP,BOTTOM | =5X_DIELECTRIC | ? |
| GDDR_EDC2EDC | * | =3X_DIELECTRIC | ? |
| GDDR_EDC2EDC | TOP,BOTTOM | =5X_DIELECTRIC | ? |
| GDDR_DBI2DBI | * | =3x_DIELECTRIC | ? |
| GDDR_DBI2DBI | TOP,BOTTOM | =3x_DIELECTRIC | ? |
| GDDR_WCK2WCK | * | =3X_DIELECTRIC | ? |
| GDDR_WCK2WCK | TOP,BOTTOM | =5x_DIELECTRIC | ? |

### Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GDDR_*_*_MA | * | * | GDDR_ISO |
| GDDR_*_*_MA | =SAME | * | GDDR_MA2MA |

Data: DQxy[31:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GDDR_*_*_DQ | * | * | GDDR_ISO |
| GDDR_*_*_DQ | =SAME | * | GDDR_DQ2DQ |

Address Dynamic Bus Inversion: ADBIxy

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GDDR_*_*_ADBI | * | * | GDDR_ISO |
| GDDR_*_*_ADBI | =SAME | * | GDDR_ADBI2ADBI |

Error Detection: EDCxy[3:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GDDR_*_*_EDC | * | * | GDDR_EDC_ISO |
| GDDR_*_*_EDC | =SAME | * | GDDR_EDC2EDC |

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GDDR_CTRL | * | * | GDDR_ISO |
| GDDR_*_*_CTRL | * | * | GDDR_ISO |
| GDDR_*_*_CTRL | =SAME | * | GDDR_CTRL2CTRL |

Data Dynamic Bus Inversion: DDBIxy[3:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GDDR_*_*_DBI | * | * | GDDR_ISO |
| GDDR_*_*_DBI | =SAME | * | GDDR_DBI2DBI |

Clock: CKxy

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GDDR_*_*_CLK | * | * | GDDR_ISO |
| GDDR_*_*_CLK | =SAME | * | GDDR_CLK2CLK |

Forwarded Clock: WCKxy[1:0]

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| GDDR_*_*_WCK | * | * | GDDR_ISO |
| GDDR_*_*_WCK | =SAME | * | GDDR_WCK2WCK |

# GPU

## GPU-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| CLK_GPU_55S | * | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =55_OHM_SE | =STANDARD | =STANDARD |

## GPU-specific Spacing Definitions

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| CLK_GPU_ISO | * | =4:1_SPACING | ? |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| CLK_GPU | * | * | CLK_GPU_ISO |

## GDDR5 Frame Buffer A

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| **Memory Address** | | | | | |
| 1642 GDDR_A0_MA | GDDR_MA_PHY | GDDR_A_0_MA | FB_A0_A<8..0> | NO_TEST=TRUE | 84 86 |
| 1643 GDDR_A1_MA | GDDR_MA_PHY | GDDR_A_1_MA | FB_A1_A<8..0> | NO_TEST=TRUE | 84 86 |
| **Address Dynamic Bus Inv** | | | | | |
| 1644 GDDR_A0_ADBI | GDDR_ADBI_PHY | GDDR_A_0_ADBI | FB_A0_ABI_L | NO_TEST=TRUE | 84 86 |
| 1645 GDDR_A1_ADBI | GDDR_ADBI_PHY | GDDR_A_1_ADBI | FB_A1_ABI_L | NO_TEST=TRUE | 84 86 |
| **Control** | | | | | |
| 1647 GDDR_A0_CKE | GDDR_CTRL_PHY | GDDR_A_0_CTRL | FB_A0_CKE_L | NO_TEST=TRUE | 84 86 |
| 1648 GDDR_A0_CTRL | GDDR_CTRL_PHY | GDDR_A_0_CTRL | FB_A0_CS_L | NO_TEST=TRUE | 84 86 |
| 1646 GDDR_A0_CTRL | GDDR_CTRL_PHY | GDDR_A_0_CTRL | FB_A0_WE_L | NO_TEST=TRUE | 84 86 |
| 1650 GDDR_A0_CTRL | GDDR_CTRL_PHY | GDDR_A_0_CTRL | FB_A0_CAS_L | NO_TEST=TRUE | 84 86 |
| 1651 GDDR_A0_CTRL | GDDR_CTRL_PHY | GDDR_A_0_CTRL | FB_A0_RAS_L | NO_TEST=TRUE | 84 86 |
| 1653 GDDR_A1_CKE | GDDR_CTRL_PHY | GDDR_A_1_CTRL | FB_A1_CKE_L | NO_TEST=TRUE | 84 86 |
| 1654 GDDR_A1_CTRL | GDDR_CTRL_PHY | GDDR_A_1_CTRL | FB_A1_CS_L | NO_TEST=TRUE | 84 86 |
| 1652 GDDR_A1_CTRL | GDDR_CTRL_PHY | GDDR_A_1_CTRL | FB_A1_WE_L | NO_TEST=TRUE | 84 86 |
| 1655 GDDR_A1_CTRL | GDDR_CTRL_PHY | GDDR_A_1_CTRL | FB_A1_CAS_L | NO_TEST=TRUE | 84 86 |
| 1656 GDDR_A1_CTRL | GDDR_CTRL_PHY | GDDR_A_1_CTRL | FB_A1_RAS_L | NO_TEST=TRUE | 84 86 |
| **Clock** | | | | | |
| 1652 GDDR_A0_CLK | GDDR_CLK_PHY | GDDR_A_0_CLK | FB_A0_CLK_P | NO_TEST=TRUE | 84 86 |
| 1653 GDDR_A0_CLK | GDDR_CLK_PHY | GDDR_A_0_CLK | FB_A0_CLK_N | NO_TEST=TRUE | 84 86 |
| 1655 GDDR_A1_CLK | GDDR_CLK_PHY | GDDR_A_1_CLK | FB_A1_CLK_P | NO_TEST=TRUE | 84 86 |
| 1656 GDDR_A1_CLK | GDDR_CLK_PHY | GDDR_A_1_CLK | FB_A1_CLK_N | NO_TEST=TRUE | 84 86 |
| **Data** | | | | | |
| 1665 GDDR_A0_DQ_BYTE0 | GDDR_DQ_PHY | GDDR_A_0_DQ | FB_A0_DQ<7..0> | NO_TEST=TRUE | 84 86 |
| 1666 GDDR_A0_DQ_BYTE1 | GDDR_DQ_PHY | GDDR_A_0_DQ | FB_A0_DQ<15..8> | NO_TEST=TRUE | 84 86 |
| 1662 GDDR_A0_DQ_BYTE2 | GDDR_DQ_PHY | GDDR_A_0_DQ | FB_A0_DQ<23..16> | NO_TEST=TRUE | 84 86 |
| 1663 GDDR_A0_DQ_BYTE3 | GDDR_DQ_PHY | GDDR_A_0_DQ | FB_A0_DQ<31..24> | NO_TEST=TRUE | 84 86 |
| 1664 GDDR_A1_DQ_BYTE0 | GDDR_DQ_PHY | GDDR_A_1_DQ | FB_A1_DQ<7..0> | NO_TEST=TRUE | 84 86 |
| 1660 GDDR_A1_DQ_BYTE1 | GDDR_DQ_PHY | GDDR_A_1_DQ | FB_A1_DQ<15..8> | NO_TEST=TRUE | 84 86 |
| 1661 GDDR_A1_DQ_BYTE2 | GDDR_DQ_PHY | GDDR_A_1_DQ | FB_A1_DQ<23..16> | NO_TEST=TRUE | 84 86 |
| 1658 GDDR_A1_DQ_BYTE3 | GDDR_DQ_PHY | GDDR_A_1_DQ | FB_A1_DQ<31..24> | NO_TEST=TRUE | 84 86 |
| **Error Detection** | | | | | |
| 1670 GDDR_A0_EDC0 | GDDR_EDC_PHY | GDDR_A_0_EDC | FB_A0_EDC<0> | NO_TEST=TRUE | 84 86 |
| 1669 GDDR_A0_EDC1 | GDDR_EDC_PHY | GDDR_A_0_EDC | FB_A0_EDC<1> | NO_TEST=TRUE | 84 86 |
| 1674 GDDR_A0_EDC2 | GDDR_EDC_PHY | GDDR_A_0_EDC | FB_A0_EDC<2> | NO_TEST=TRUE | 84 86 |
| 1672 GDDR_A0_EDC3 | GDDR_EDC_PHY | GDDR_A_0_EDC | FB_A0_EDC<3> | NO_TEST=TRUE | 84 86 |
| 1673 GDDR_A1_EDC0 | GDDR_EDC_PHY | GDDR_A_1_EDC | FB_A1_EDC<0> | NO_TEST=TRUE | 84 86 |
| 1671 GDDR_A1_EDC1 | GDDR_EDC_PHY | GDDR_A_1_EDC | FB_A1_EDC<1> | NO_TEST=TRUE | 84 86 |
| 1675 GDDR_A1_EDC2 | GDDR_EDC_PHY | GDDR_A_1_EDC | FB_A1_EDC<2> | NO_TEST=TRUE | 84 86 |
| 1677 GDDR_A1_EDC3 | GDDR_EDC_PHY | GDDR_A_1_EDC | FB_A1_EDC<3> | NO_TEST=TRUE | 84 86 |
| **Data Dynamic Bus Inv** | | | | | |
| 1677 GDDR_A0_DBI0 | GDDR_DBI_PHY | GDDR_A_0_DBI | FB_A0_DBI_L<0> | NO_TEST=TRUE | 84 86 |
| 1676 GDDR_A0_DBI1 | GDDR_DBI_PHY | GDDR_A_0_DBI | FB_A0_DBI_L<1> | NO_TEST=TRUE | 84 86 |
| 1680 GDDR_A0_DBI2 | GDDR_DBI_PHY | GDDR_A_0_DBI | FB_A0_DBI_L<2> | NO_TEST=TRUE | 84 86 |
| 1679 GDDR_A0_DBI3 | GDDR_DBI_PHY | GDDR_A_0_DBI | FB_A0_DBI_L<3> | NO_TEST=TRUE | 84 86 |
| 1689 GDDR_A1_DBI0 | GDDR_DBI_PHY | GDDR_A_1_DBI | FB_A1_DBI_L<0> | NO_TEST=TRUE | 84 86 |
| 1688 GDDR_A1_DBI1 | GDDR_DBI_PHY | GDDR_A_1_DBI | FB_A1_DBI_L<1> | NO_TEST=TRUE | 84 86 |
| 1686 GDDR_A1_DBI2 | GDDR_DBI_PHY | GDDR_A_1_DBI | FB_A1_DBI_L<2> | NO_TEST=TRUE | 84 86 |
| 1687 GDDR_A1_DBI3 | GDDR_DBI_PHY | GDDR_A_1_DBI | FB_A1_DBI_L<3> | NO_TEST=TRUE | 84 86 |
| **Forwarded Clock** | | | | | |
| 1685 GDDR_A0_WCK0 | GDDR_WCK_PHY | GDDR_A_0_WCK | FB_A0_WCLK_P<0> | NO_TEST=TRUE | 84 86 |
| 1683 GDDR_A0_WCK0 | GDDR_WCK_PHY | GDDR_A_0_WCK | FB_A0_WCLK_N<0> | NO_TEST=TRUE | 84 86 |
| 1684 GDDR_A0_WCK1 | GDDR_WCK_PHY | GDDR_A_0_WCK | FB_A0_WCLK_P<1> | NO_TEST=TRUE | 84 86 |
| 1682 GDDR_A0_WCK1 | GDDR_WCK_PHY | GDDR_A_0_WCK | FB_A0_WCLK_N<1> | NO_TEST=TRUE | 84 86 |
| 1690 GDDR_A1_WCK0 | GDDR_WCK_PHY | GDDR_A_1_WCK | FB_A1_WCLK_P<0> | NO_TEST=TRUE | 84 86 |
| 1696 GDDR_A1_WCK0 | GDDR_WCK_PHY | GDDR_A_1_WCK | FB_A1_WCLK_N<0> | NO_TEST=TRUE | 84 86 |
| 1692 GDDR_A1_WCK1 | GDDR_WCK_PHY | GDDR_A_1_WCK | FB_A1_WCLK_P<1> | NO_TEST=TRUE | 84 86 |
| 1691 GDDR_A1_WCK1 | GDDR_WCK_PHY | GDDR_A_1_WCK | FB_A1_WCLK_N<1> | NO_TEST=TRUE | 84 86 |

## GDDR5 Frame Buffer B

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| **Memory Address** | | | | | |
| 1698 GDDR_B0_MA | GDDR_MA_PHY | GDDR_B_0_MA | FB_B0_A<8..0> | NO_TEST=TRUE | 84 87 |
| 1699 GDDR_B1_MA | GDDR_MA_PHY | GDDR_B_1_MA | FB_B1_A<8..0> | NO_TEST=TRUE | 84 87 |
| **Address Dynamic Bus Inv** | | | | | |
| 1696 GDDR_B0_ADBI | GDDR_ADBI_PHY | GDDR_B_0_ADBI | FB_B0_ABI_L | NO_TEST=TRUE | 84 87 |
| 1697 GDDR_B1_ADBI | GDDR_ADBI_PHY | GDDR_B_1_ADBI | FB_B1_ABI_L | NO_TEST=TRUE | 84 87 |
| **Control** | | | | | |
| 1698 GDDR_B0_CKE | GDDR_CTRL_PHY | GDDR_B_0_CTRL | FB_B0_CKE_L | NO_TEST=TRUE | 84 87 |
| 1701 GDDR_B0_CTRL | GDDR_CTRL_PHY | GDDR_B_0_CTRL | FB_B0_CS_L | NO_TEST=TRUE | 84 87 |
| 1702 GDDR_B0_CTRL | GDDR_CTRL_PHY | GDDR_B_0_CTRL | FB_B0_WE_L | NO_TEST=TRUE | 84 87 |
| 1707 GDDR_B0_CTRL | GDDR_CTRL_PHY | GDDR_B_0_CTRL | FB_B0_CAS_L | NO_TEST=TRUE | 84 87 |
| 1708 GDDR_B0_CTRL | GDDR_CTRL_PHY | GDDR_B_0_CTRL | FB_B0_RAS_L | NO_TEST=TRUE | 84 87 |
| 1703 GDDR_B1_CKE | GDDR_CTRL_PHY | GDDR_B_1_CTRL | FB_B1_CKE_L | NO_TEST=TRUE | 84 87 |
| 1704 GDDR_B1_CTRL | GDDR_CTRL_PHY | GDDR_B_1_CTRL | FB_B1_CS_L | NO_TEST=TRUE | 84 87 |
| 1706 GDDR_B1_CTRL | GDDR_CTRL_PHY | GDDR_B_1_CTRL | FB_B1_WE_L | NO_TEST=TRUE | 84 87 |
| 1709 GDDR_B1_CTRL | GDDR_CTRL_PHY | GDDR_B_1_CTRL | FB_B1_CAS_L | NO_TEST=TRUE | 84 87 |
| 1707 GDDR_B1_CTRL | GDDR_CTRL_PHY | GDDR_B_1_CTRL | FB_B1_RAS_L | NO_TEST=TRUE | 84 87 |
| **Clock** | | | | | |
| 1699 GDDR_B0_CLK | GDDR_CLK_PHY | GDDR_B_0_CLK | FB_B0_CLK_P | NO_TEST=TRUE | 84 87 |
| 1701 GDDR_B0_CLK | GDDR_CLK_PHY | GDDR_B_0_CLK | FB_B0_CLK_N | NO_TEST=TRUE | 84 87 |
| 1707 GDDR_B1_CLK | GDDR_CLK_PHY | GDDR_B_1_CLK | FB_B1_CLK_P | NO_TEST=TRUE | 84 87 |
| 1711 GDDR_B1_CLK | GDDR_CLK_PHY | GDDR_B_1_CLK | FB_B1_CLK_N | NO_TEST=TRUE | 84 87 |
| **Data** | | | | | |
| 1715 GDDR_B0_DQ_BYTE0 | GDDR_DQ_PHY | GDDR_B_0_DQ | FB_B0_DQ<7..0> | NO_TEST=TRUE | 84 87 |
| 1714 GDDR_B0_DQ_BYTE1 | GDDR_DQ_PHY | GDDR_B_0_DQ | FB_B0_DQ<15..8> | NO_TEST=TRUE | 84 87 |
| 1712 GDDR_B0_DQ_BYTE2 | GDDR_DQ_PHY | GDDR_B_0_DQ | FB_B0_DQ<23..16> | NO_TEST=TRUE | 84 87 |
| 1713 GDDR_B0_DQ_BYTE3 | GDDR_DQ_PHY | GDDR_B_0_DQ | FB_B0_DQ<31..24> | NO_TEST=TRUE | 84 87 |
| 1718 GDDR_B1_DQ_BYTE0 | GDDR_DQ_PHY | GDDR_B_1_DQ | FB_B1_DQ<7..0> | NO_TEST=TRUE | 84 87 |
| 1716 GDDR_B1_DQ_BYTE1 | GDDR_DQ_PHY | GDDR_B_1_DQ | FB_B1_DQ<15..8> | NO_TEST=TRUE | 84 87 |
| 1717 GDDR_B1_DQ_BYTE2 | GDDR_DQ_PHY | GDDR_B_1_DQ | FB_B1_DQ<23..16> | NO_TEST=TRUE | 84 87 |
| 1719 GDDR_B1_DQ_BYTE3 | GDDR_DQ_PHY | GDDR_B_1_DQ | FB_B1_DQ<31..24> | NO_TEST=TRUE | 84 87 |
| **Error Detection** | | | | | |
| 1720 GDDR_B0_EDC0 | GDDR_EDC_PHY | GDDR_B_0_EDC | FB_B0_EDC<0> | NO_TEST=TRUE | 84 87 |
| 1721 GDDR_B0_EDC1 | GDDR_EDC_PHY | GDDR_B_0_EDC | FB_B0_EDC<1> | NO_TEST=TRUE | 84 87 |
| 1723 GDDR_B0_EDC2 | GDDR_EDC_PHY | GDDR_B_0_EDC | FB_B0_EDC<2> | NO_TEST=TRUE | 84 87 |
| 1722 GDDR_B0_EDC3 | GDDR_EDC_PHY | GDDR_B_0_EDC | FB_B0_EDC<3> | NO_TEST=TRUE | 84 87 |
| 1725 GDDR_B1_EDC0 | GDDR_EDC_PHY | GDDR_B_1_EDC | FB_B1_EDC<0> | NO_TEST=TRUE | 84 87 |
| 1724 GDDR_B1_EDC1 | GDDR_EDC_PHY | GDDR_B_1_EDC | FB_B1_EDC<1> | NO_TEST=TRUE | 84 87 |
| 1726 GDDR_B1_EDC2 | GDDR_EDC_PHY | GDDR_B_1_EDC | FB_B1_EDC<2> | NO_TEST=TRUE | 84 87 |
| 1727 GDDR_B1_EDC3 | GDDR_EDC_PHY | GDDR_B_1_EDC | FB_B1_EDC<3> | NO_TEST=TRUE | 84 87 |
| **Data Dynamic Bus Inv** | | | | | |
| 1729 GDDR_B0_DBI0 | GDDR_DBI_PHY | GDDR_B_0_DBI | FB_B0_DBI_L<0> | NO_TEST=TRUE | 84 87 |
| 1728 GDDR_B0_DBI1 | GDDR_DBI_PHY | GDDR_B_0_DBI | FB_B0_DBI_L<1> | NO_TEST=TRUE | 84 87 |
| 1730 GDDR_B0_DBI2 | GDDR_DBI_PHY | GDDR_B_0_DBI | FB_B0_DBI_L<2> | NO_TEST=TRUE | 84 87 |
| 1731 GDDR_B0_DBI3 | GDDR_DBI_PHY | GDDR_B_0_DBI | FB_B0_DBI_L<3> | NO_TEST=TRUE | 84 87 |
| 1732 GDDR_B1_DBI0 | GDDR_DBI_PHY | GDDR_B_1_DBI | FB_B1_DBI_L<0> | NO_TEST=TRUE | 84 87 |
| 1733 GDDR_B1_DBI1 | GDDR_DBI_PHY | GDDR_B_1_DBI | FB_B1_DBI_L<1> | NO_TEST=TRUE | 84 87 |
| 1734 GDDR_B1_DBI2 | GDDR_DBI_PHY | GDDR_B_1_DBI | FB_B1_DBI_L<2> | NO_TEST=TRUE | 84 87 |
| 1735 GDDR_B1_DBI3 | GDDR_DBI_PHY | GDDR_B_1_DBI | FB_B1_DBI_L<3> | NO_TEST=TRUE | 84 87 |
| **Forwarded Clock** | | | | | |
| 1736 GDDR_B0_WCK0 | GDDR_WCK_PHY | GDDR_B_0_WCK | FB_B0_WCLK_P<0> | NO_TEST=TRUE | 84 87 |
| 1737 GDDR_B0_WCK0 | GDDR_WCK_PHY | GDDR_B_0_WCK | FB_B0_WCLK_N<0> | NO_TEST=TRUE | 84 87 |
| 1738 GDDR_B0_WCK1 | GDDR_WCK_PHY | GDDR_B_0_WCK | FB_B0_WCLK_P<1> | NO_TEST=TRUE | 84 87 |
| 1739 GDDR_B0_WCK1 | GDDR_WCK_PHY | GDDR_B_0_WCK | FB_B0_WCLK_N<1> | NO_TEST=TRUE | 84 87 |
| 1740 GDDR_B1_WCK0 | GDDR_WCK_PHY | GDDR_B_1_WCK | FB_B1_WCLK_P<0> | NO_TEST=TRUE | 84 87 |
| 1741 GDDR_B1_WCK0 | GDDR_WCK_PHY | GDDR_B_1_WCK | FB_B1_WCLK_N<0> | NO_TEST=TRUE | 84 87 |
| 1743 GDDR_B1_WCK1 | GDDR_WCK_PHY | GDDR_B_1_WCK | FB_B1_WCLK_P<1> | NO_TEST=TRUE | 84 87 |
| 1742 GDDR_B1_WCK1 | GDDR_WCK_PHY | GDDR_B_1_WCK | FB_B1_WCLK_N<1> | NO_TEST=TRUE | 84 87 |

## GPU

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| **Clocks** | | | | | |
| 1747 | CLK_GPU_55S | CLK_GPU | PEX_TSTCLK_O_PL | | 83 |
| 1748 | CLK_GPU_55S | CLK_GPU | PEX_TSTCLK_O_NG | | 83 |
| 1749 | CLK_PCIE_PHY | CLK_PCIE | GPU_TESTMODE | | 83 |
| 1750 | CLK_PCIE_PHY | CLK_PCIE | GPU_PEX_TERMP | | 83 |
| 1751 | CLK_GPU_55S | CLK_GPU | FB_A0_CK_MID | NO_TEST=TRUE | 86 |
| 1752 | CLK_GPU_55S | CLK_GPU | FB_A1_CK_MID | NO_TEST=TRUE | 86 |
| 1753 | CLK_GPU_55S | CLK_GPU | FB_B0_CK_MID | NO_TEST=TRUE | 87 |
| 1754 | CLK_GPU_55S | CLK_GPU | FB_B1_CK_MID | NO_TEST=TRUE | 87 |
| 1755 | CLK_GPU_55S | CLK_GPU | FB_C0_CK_MID | NO_TEST=TRUE | 88 |
| 1756 | CLK_GPU_55S | CLK_GPU | FB_C1_CK_MID | NO_TEST=TRUE | 88 |
| 1757 | CLK_GPU_55S | CLK_GPU | FB_D0_CK_MID | NO_TEST=TRUE | 89 |
| 1758 | CLK_GPU_55S | CLK_GPU | FB_D1_CK_MID | NO_TEST=TRUE | 89 |
| 1771 | CLK_GPU_55S | CLK_GPU | GPU_JTAG_TCK | | 91 |
| 1772 | CLK_GPU_55S | CLK_GPU | GPU_ROM_SCLK | | 91 |
| 1773 | CLK_GPU_55S | CLK_GPU | GPU_ROM_SCLK_R | | 91 |
| 1774 | CLK_GPU_55S | CLK_GPU | GPU_OSC_27M_XTAL_P | | 91 |
| 1775 | CLK_GPU_55S | CLK_GPU | GPU_OSC_27M_XTAL_N | | 91 |
| **SMB** | | | | | |
| 1764 | SMB_PHY | SMB | GPU_SMB_CLK | | 91 |
| 1765 | SMB_PHY | SMB | GPU_SMB_DAT | | 91 |
| 1763 | SMB_PHY | SMB | GPU_SMB_CLK_R | | 50 91 |
| 1762 | SMB_PHY | SMB | GPU_SMB_DAT_R | | 50 91 |
| **PCIe Compensation** | | | | | |
| 1768 | PCIE_50S | COMP_PCIE | FB_CAL_PD_VDDQ | | 94 |
| 1769 | PCIE_50S | COMP_PCIE | FB_CAL_PU_GND | | 94 |
| 1767 | PCIE_50S | COMP_PCIE | FB_CAL_TERM_GND | | 94 |

## Frame Buffer Reset

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| **Reset** | | | | | |
| 1764 GDDR_A0_RESET | GDDR_50S | GDDR_CTRL | FB_A0_RESET_L | | 84 86 |
| 1765 GDDR_A1_RESET | GDDR_50S | GDDR_CTRL | FB_A1_RESET_L | | 84 86 |
| 1760 GDDR_B0_RESET | GDDR_50S | GDDR_CTRL | FB_B0_RESET_L | | 84 87 |
| 1761 GDDR_B1_RESET | GDDR_50S | GDDR_CTRL | FB_B1_RESET_L | | 84 87 |
| 1762 GDDR_C0_RESET | GDDR_50S | GDDR_CTRL | FB_C0_RESET_L | | 85 88 |
| 1763 GDDR_C1_RESET | GDDR_50S | GDDR_CTRL | FB_C1_RESET_L | | 85 88 |
| 1766 GDDR_D0_RESET | GDDR_50S | GDDR_CTRL | FB_D0_RESET_L | | 85 89 |
| 1767 GDDR_D1_RESET | GDDR_50S | GDDR_CTRL | FB_D1_RESET_L | | 85 89 |

SYNC_MASTER=D8_MLB SYNC_DATE=01/11/2012

PAGE TITLE
GDDR5/GPU Constraints

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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## GDDR5 FRAME BUFFER C

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| **Memory Address** | | | | | |
| 1642 GDDR_C0_MA | GDDR_MA_PHY | GDDR_C_0_MA | FB_C0_A<8..0> | NO_TEST=TRUE | 85 88 |
| 1643 GDDR_C1_MA | GDDR_MA_PHY | GDDR_C_1_MA | FB_C1_A<8..0> | NO_TEST=TRUE | 85 88 |
| **Address Dynamic Bus Inv** | | | | | |
| 1644 GDDR_C0_ADBI | GDDR_ADBI_PHY | GDDR_C_0_ADBI | FB_C0_ABI_L | NO_TEST=TRUE | 85 88 |
| 1645 GDDR_C1_ADBI | GDDR_ADBI_PHY | GDDR_C_1_ADBI | FB_C1_ABI_L | NO_TEST=TRUE | 85 88 |
| **Control** | | | | | |
| 1647 GDDR_C0_CKE | GDDR_CTRL_PHY | GDDR_C_0_CTRL | FB_C0_CKE_L | NO_TEST=TRUE | 85 88 |
| 1648 GDDR_C0_CTRL | GDDR_CTRL_PHY | GDDR_C_0_CTRL | FB_C0_CS_L | NO_TEST=TRUE | 85 88 |
| 1649 GDDR_C0_CTRL | GDDR_CTRL_PHY | GDDR_C_0_CTRL | FB_C0_WE_L | NO_TEST=TRUE | 85 88 |
| 1650 GDDR_C0_CTRL | GDDR_CTRL_PHY | GDDR_C_0_CTRL | FB_C0_CAS_L | NO_TEST=TRUE | 85 88 |
| 1651 GDDR_C0_CTRL | GDDR_CTRL_PHY | GDDR_C_0_CTRL | FB_C0_RAS_L | NO_TEST=TRUE | 85 88 |
| 1652 GDDR_C1_CKE | GDDR_CTRL_PHY | GDDR_C_1_CTRL | FB_C1_CKE_L | NO_TEST=TRUE | 85 88 |
| 1653 GDDR_C1_CTRL | GDDR_CTRL_PHY | GDDR_C_1_CTRL | FB_C1_CS_L | NO_TEST=TRUE | 85 88 |
| 1654 GDDR_C1_CTRL | GDDR_CTRL_PHY | GDDR_C_1_CTRL | FB_C1_WE_L | NO_TEST=TRUE | 85 88 |
| 1655 GDDR_C1_CTRL | GDDR_CTRL_PHY | GDDR_C_1_CTRL | FB_C1_CAS_L | NO_TEST=TRUE | 85 88 |
| 1656 GDDR_C1_CTRL | GDDR_CTRL_PHY | GDDR_C_1_CTRL | FB_C1_RAS_L | NO_TEST=TRUE | 85 88 |
| **Clock** | | | | | |
| 1657 GDDR_C0_CLK | GDDR_CLK_PHY | GDDR_C_0_CLK | FB_C0_CLK_P | NO_TEST=TRUE | 85 88 |
| 1658 GDDR_C0_CLK | GDDR_CLK_PHY | GDDR_C_0_CLK | FB_C0_CLK_N | NO_TEST=TRUE | 85 88 |
| 1659 GDDR_C1_CLK | GDDR_CLK_PHY | GDDR_C_1_CLK | FB_C1_CLK_P | NO_TEST=TRUE | 85 88 |
| 1660 GDDR_C1_CLK | GDDR_CLK_PHY | GDDR_C_1_CLK | FB_C1_CLK_N | NO_TEST=TRUE | 85 88 |
| **Data** | | | | | |
| 1661 GDDR_C0_DQ_BYTE0 | GDDR_DQ_PHY | GDDR_C_0_DQ | FB_C0_DQ<7..0> | NO_TEST=TRUE | 85 88 |
| 1662 GDDR_C0_DQ_BYTE1 | GDDR_DQ_PHY | GDDR_C_0_DQ | FB_C0_DQ<15..8> | NO_TEST=TRUE | 85 88 |
| 1663 GDDR_C0_DQ_BYTE2 | GDDR_DQ_PHY | GDDR_C_0_DQ | FB_C0_DQ<23..16> | NO_TEST=TRUE | 85 88 |
| 1664 GDDR_C0_DQ_BYTE3 | GDDR_DQ_PHY | GDDR_C_0_DQ | FB_C0_DQ<31..24> | NO_TEST=TRUE | 85 88 |
| 1665 GDDR_C1_DQ_BYTE0 | GDDR_DQ_PHY | GDDR_C_1_DQ | FB_C1_DQ<7..0> | NO_TEST=TRUE | 85 88 |
| 1666 GDDR_C1_DQ_BYTE1 | GDDR_DQ_PHY | GDDR_C_1_DQ | FB_C1_DQ<15..8> | NO_TEST=TRUE | 85 88 |
| 1667 GDDR_C1_DQ_BYTE2 | GDDR_DQ_PHY | GDDR_C_1_DQ | FB_C1_DQ<23..16> | NO_TEST=TRUE | 85 88 |
| 1668 GDDR_C1_DQ_BYTE3 | GDDR_DQ_PHY | GDDR_C_1_DQ | FB_C1_DQ<31..24> | NO_TEST=TRUE | 85 88 |
| **Error Detection** | | | | | |
| 1669 GDDR_C0_EDC0 | GDDR_EDC_PHY | GDDR_C_0_EDC | FB_C0_EDC<0> | NO_TEST=TRUE | 85 88 |
| 1668 GDDR_C0_EDC1 | GDDR_EDC_PHY | GDDR_C_0_EDC | FB_C0_EDC<1> | NO_TEST=TRUE | 85 88 |
| 1671 GDDR_C0_EDC2 | GDDR_EDC_PHY | GDDR_C_0_EDC | FB_C0_EDC<2> | NO_TEST=TRUE | 85 88 |
| 1672 GDDR_C0_EDC3 | GDDR_EDC_PHY | GDDR_C_0_EDC | FB_C0_EDC<3> | NO_TEST=TRUE | 85 88 |
| 1673 GDDR_C1_EDC0 | GDDR_EDC_PHY | GDDR_C_1_EDC | FB_C1_EDC<0> | NO_TEST=TRUE | 85 88 |
| 1674 GDDR_C1_EDC1 | GDDR_EDC_PHY | GDDR_C_1_EDC | FB_C1_EDC<1> | NO_TEST=TRUE | 85 88 |
| 1675 GDDR_C1_EDC2 | GDDR_EDC_PHY | GDDR_C_1_EDC | FB_C1_EDC<2> | NO_TEST=TRUE | 85 88 |
| 1676 GDDR_C1_EDC3 | GDDR_EDC_PHY | GDDR_C_1_EDC | FB_C1_EDC<3> | NO_TEST=TRUE | 85 88 |
| **Data Dynamic Bus Inv** | | | | | |
| 1677 GDDR_C0_DBI0 | GDDR_DBI_PHY | GDDR_C_0_DBI | FB_C0_DBI_L<0> | NO_TEST=TRUE | 85 88 |
| 1678 GDDR_C0_DBI1 | GDDR_DBI_PHY | GDDR_C_0_DBI | FB_C0_DBI_L<1> | NO_TEST=TRUE | 85 88 |
| 1679 GDDR_C0_DBI2 | GDDR_DBI_PHY | GDDR_C_0_DBI | FB_C0_DBI_L<2> | NO_TEST=TRUE | 85 88 |
| 1680 GDDR_C0_DBI3 | GDDR_DBI_PHY | GDDR_C_0_DBI | FB_C0_DBI_L<3> | NO_TEST=TRUE | 85 88 |
| 1681 GDDR_C1_DBI0 | GDDR_DBI_PHY | GDDR_C_1_DBI | FB_C1_DBI_L<0> | NO_TEST=TRUE | 85 88 |
| 1682 GDDR_C1_DBI1 | GDDR_DBI_PHY | GDDR_C_1_DBI | FB_C1_DBI_L<1> | NO_TEST=TRUE | 85 88 |
| 1683 GDDR_C1_DBI2 | GDDR_DBI_PHY | GDDR_C_1_DBI | FB_C1_DBI_L<2> | NO_TEST=TRUE | 85 88 |
| 1684 GDDR_C1_DBI3 | GDDR_DBI_PHY | GDDR_C_1_DBI | FB_C1_DBI_L<3> | NO_TEST=TRUE | 85 88 |
| **Forwarded Clock** | | | | | |
| 1685 GDDR_C0_WCK0 | GDDR_WCK_PHY | GDDR_C_0_WCK | FB_C0_WCLK_P<0> | NO_TEST=TRUE | 85 88 |
| 1686 GDDR_C0_WCK0 | GDDR_WCK_PHY | GDDR_C_0_WCK | FB_C0_WCLK_N<0> | NO_TEST=TRUE | 85 88 |
| 1687 GDDR_C0_WCK1 | GDDR_WCK_PHY | GDDR_C_0_WCK | FB_C0_WCLK_P<1> | NO_TEST=TRUE | 85 88 |
| 1688 GDDR_C0_WCK1 | GDDR_WCK_PHY | GDDR_C_0_WCK | FB_C0_WCLK_N<1> | NO_TEST=TRUE | 85 88 |
| 1689 GDDR_C1_WCK0 | GDDR_WCK_PHY | GDDR_C_1_WCK | FB_C1_WCLK_P<0> | NO_TEST=TRUE | 85 88 |
| 1690 GDDR_C1_WCK0 | GDDR_WCK_PHY | GDDR_C_1_WCK | FB_C1_WCLK_N<0> | NO_TEST=TRUE | 85 88 |
| 1691 GDDR_C1_WCK1 | GDDR_WCK_PHY | GDDR_C_1_WCK | FB_C1_WCLK_P<1> | NO_TEST=TRUE | 85 88 |
| 1692 GDDR_C1_WCK1 | GDDR_WCK_PHY | GDDR_C_1_WCK | FB_C1_WCLK_N<1> | NO_TEST=TRUE | 85 88 |
| **Memory Address** | | | | | |
| 1744 GDDR_A0_MA | GDDR_MA_PHY | GDDR_A_0_MA | FB_A0_A<12> | NO_TEST=TRUE | 84 86 |
| 1745 GDDR_A1_MA | GDDR_MA_PHY | GDDR_A_1_MA | FB_A1_A<12> | NO_TEST=TRUE | 84 86 |
| 1746 GDDR_B0_MA | GDDR_MA_PHY | GDDR_B_0_MA | FB_B0_A<12> | NO_TEST=TRUE | 84 87 |
| 1747 GDDR_B1_MA | GDDR_MA_PHY | GDDR_B_1_MA | FB_B1_A<12> | NO_TEST=TRUE | 84 87 |
| 1748 GDDR_C0_MA | GDDR_MA_PHY | GDDR_C_0_MA | FB_C0_A<12> | NO_TEST=TRUE | 85 88 |
| 1749 GDDR_C1_MA | GDDR_MA_PHY | GDDR_C_1_MA | FB_C1_A<12> | NO_TEST=TRUE | 85 88 |
| 1750 GDDR_D0_MA | GDDR_MA_PHY | GDDR_D_0_MA | FB_D0_A<12> | NO_TEST=TRUE | 85 89 |
| 1751 GDDR_D1_MA | GDDR_MA_PHY | GDDR_D_1_MA | FB_D1_A<12> | NO_TEST=TRUE | 85 89 |

## GDDR5 FRAME BUFFER D

| Electrical Contraint Set | Physical | Spacing | | | |
|---|---|---|---|---|---|
| **Memory Address** | | | | | |
| 1690 GDDR_D0_MA | GDDR_MA_PHY | GDDR_D_0_MA | FB_D0_A<8..0> | NO_TEST=TRUE | 85 89 |
| 1691 GDDR_D1_MA | GDDR_MA_PHY | GDDR_D_1_MA | FB_D1_A<8..0> | NO_TEST=TRUE | 85 89 |
| **Address Dynamic Bus Inv** | | | | | |
| 1696 GDDR_D0_ADBI | GDDR_ADBI_PHY | GDDR_D_0_ADBI | FB_D0_ABI_L | NO_TEST=TRUE | 85 89 |
| 1697 GDDR_D1_ADBI | GDDR_ADBI_PHY | GDDR_D_1_ADBI | FB_D1_ABI_L | NO_TEST=TRUE | 85 89 |
| **Control** | | | | | |
| 1698 GDDR_D0_CKE | GDDR_CTRL_PHY | GDDR_D_0_CTRL | FB_D0_CKE_L | NO_TEST=TRUE | 85 89 |
| 1699 GDDR_D0_CTRL | GDDR_CTRL_PHY | GDDR_D_0_CTRL | FB_D0_CS_L | NO_TEST=TRUE | 85 89 |
| 1700 GDDR_D0_CTRL | GDDR_CTRL_PHY | GDDR_D_0_CTRL | FB_D0_WE_L | NO_TEST=TRUE | 85 89 |
| 1701 GDDR_D0_CTRL | GDDR_CTRL_PHY | GDDR_D_0_CTRL | FB_D0_CAS_L | NO_TEST=TRUE | 85 89 |
| 1702 GDDR_D0_CTRL | GDDR_CTRL_PHY | GDDR_D_0_CTRL | FB_D0_RAS_L | NO_TEST=TRUE | 85 89 |
| 1703 GDDR_D1_CKE | GDDR_CTRL_PHY | GDDR_D_1_CTRL | FB_D1_CKE_L | NO_TEST=TRUE | 85 89 |
| 1704 GDDR_D1_CTRL | GDDR_CTRL_PHY | GDDR_D_1_CTRL | FB_D1_CS_L | NO_TEST=TRUE | 85 89 |
| 1705 GDDR_D1_CTRL | GDDR_CTRL_PHY | GDDR_D_1_CTRL | FB_D1_WE_L | NO_TEST=TRUE | 85 89 |
| 1706 GDDR_D1_CTRL | GDDR_CTRL_PHY | GDDR_D_1_CTRL | FB_D1_CAS_L | NO_TEST=TRUE | 85 89 |
| 1707 GDDR_D1_CTRL | GDDR_CTRL_PHY | GDDR_D_1_CTRL | FB_D1_RAS_L | NO_TEST=TRUE | 85 89 |
| **Clock** | | | | | |
| 1709 GDDR_D0_CLK | GDDR_CLK_PHY | GDDR_D_0_CLK | FB_D0_CLK_P | NO_TEST=TRUE | 85 89 |
| 1710 GDDR_D0_CLK | GDDR_CLK_PHY | GDDR_D_0_CLK | FB_D0_CLK_N | NO_TEST=TRUE | 85 89 |
| 1708 GDDR_D1_CLK | GDDR_CLK_PHY | GDDR_D_1_CLK | FB_D1_CLK_P | NO_TEST=TRUE | 85 89 |
| 1711 GDDR_D1_CLK | GDDR_CLK_PHY | GDDR_D_1_CLK | FB_D1_CLK_N | NO_TEST=TRUE | 85 89 |
| **Data** | | | | | |
| 1712 GDDR_D0_DQ_BYTE0 | GDDR_DQ_PHY | GDDR_D_0_DQ | FB_D0_DQ<7..0> | NO_TEST=TRUE | 85 89 |
| 1713 GDDR_D0_DQ_BYTE1 | GDDR_DQ_PHY | GDDR_D_0_DQ | FB_D0_DQ<15..8> | NO_TEST=TRUE | 85 89 |
| 1714 GDDR_D0_DQ_BYTE2 | GDDR_DQ_PHY | GDDR_D_0_DQ | FB_D0_DQ<23..16> | NO_TEST=TRUE | 85 89 |
| 1715 GDDR_D0_DQ_BYTE3 | GDDR_DQ_PHY | GDDR_D_0_DQ | FB_D0_DQ<31..24> | NO_TEST=TRUE | 85 89 |
| 1716 GDDR_D1_DQ_BYTE0 | GDDR_DQ_PHY | GDDR_D_1_DQ | FB_D1_DQ<7..0> | NO_TEST=TRUE | 85 89 |
| 1718 GDDR_D1_DQ_BYTE1 | GDDR_DQ_PHY | GDDR_D_1_DQ | FB_D1_DQ<15..8> | NO_TEST=TRUE | 85 89 |
| 1717 GDDR_D1_DQ_BYTE2 | GDDR_DQ_PHY | GDDR_D_1_DQ | FB_D1_DQ<23..16> | NO_TEST=TRUE | 85 89 |
| 1719 GDDR_D1_DQ_BYTE3 | GDDR_DQ_PHY | GDDR_D_1_DQ | FB_D1_DQ<31..24> | NO_TEST=TRUE | 85 89 |
| **Error Detection** | | | | | |
| 1720 GDDR_D0_EDC0 | GDDR_EDC_PHY | GDDR_D_0_EDC | FB_D0_EDC<0> | NO_TEST=TRUE | 85 89 |
| 1721 GDDR_D0_EDC1 | GDDR_EDC_PHY | GDDR_D_0_EDC | FB_D0_EDC<1> | NO_TEST=TRUE | 85 89 |
| 1723 GDDR_D0_EDC2 | GDDR_EDC_PHY | GDDR_D_0_EDC | FB_D0_EDC<2> | NO_TEST=TRUE | 85 89 |
| 1722 GDDR_D0_EDC3 | GDDR_EDC_PHY | GDDR_D_0_EDC | FB_D0_EDC<3> | NO_TEST=TRUE | 85 89 |
| 1725 GDDR_D1_EDC0 | GDDR_EDC_PHY | GDDR_D_1_EDC | FB_D1_EDC<0> | NO_TEST=TRUE | 85 89 |
| 1724 GDDR_D1_EDC1 | GDDR_EDC_PHY | GDDR_D_1_EDC | FB_D1_EDC<1> | NO_TEST=TRUE | 85 89 |
| 1726 GDDR_D1_EDC2 | GDDR_EDC_PHY | GDDR_D_1_EDC | FB_D1_EDC<2> | NO_TEST=TRUE | 85 89 |
| 1727 GDDR_D1_EDC3 | GDDR_EDC_PHY | GDDR_D_1_EDC | FB_D1_EDC<3> | NO_TEST=TRUE | 85 89 |
| **Data Dynamic Bus Inv** | | | | | |
| 1729 GDDR_D0_DBI0 | GDDR_DBI_PHY | GDDR_D_0_DBI | FB_D0_DBI_L<0> | NO_TEST=TRUE | 85 89 |
| 1730 GDDR_D0_DBI1 | GDDR_DBI_PHY | GDDR_D_0_DBI | FB_D0_DBI_L<1> | NO_TEST=TRUE | 85 89 |
| 1731 GDDR_D0_DBI2 | GDDR_DBI_PHY | GDDR_D_0_DBI | FB_D0_DBI_L<2> | NO_TEST=TRUE | 85 89 |
| 1732 GDDR_D0_DBI3 | GDDR_DBI_PHY | GDDR_D_0_DBI | FB_D0_DBI_L<3> | NO_TEST=TRUE | 85 89 |
| 1733 GDDR_D1_DBI0 | GDDR_DBI_PHY | GDDR_D_1_DBI | FB_D1_DBI_L<0> | NO_TEST=TRUE | 85 89 |
| 1734 GDDR_D1_DBI1 | GDDR_DBI_PHY | GDDR_D_1_DBI | FB_D1_DBI_L<1> | NO_TEST=TRUE | 85 89 |
| 1735 GDDR_D1_DBI2 | GDDR_DBI_PHY | GDDR_D_1_DBI | FB_D1_DBI_L<2> | NO_TEST=TRUE | 85 89 |
| 1736 GDDR_D1_DBI3 | GDDR_DBI_PHY | GDDR_D_1_DBI | FB_D1_DBI_L<3> | NO_TEST=TRUE | 85 89 |
| **Forwarded Clock** | | | | | |
| 1738 GDDR_D0_WCK0 | GDDR_WCK_PHY | GDDR_D_0_WCK | FB_D0_WCLK_P<0> | NO_TEST=TRUE | 85 89 |
| 1737 GDDR_D0_WCK0 | GDDR_WCK_PHY | GDDR_D_0_WCK | FB_D0_WCLK_N<0> | NO_TEST=TRUE | 85 89 |
| 1739 GDDR_D0_WCK1 | GDDR_WCK_PHY | GDDR_D_0_WCK | FB_D0_WCLK_P<1> | NO_TEST=TRUE | 85 89 |
| 1740 GDDR_D0_WCK1 | GDDR_WCK_PHY | GDDR_D_0_WCK | FB_D0_WCLK_N<1> | NO_TEST=TRUE | 85 89 |
| 1741 GDDR_D1_WCK0 | GDDR_WCK_PHY | GDDR_D_1_WCK | FB_D1_WCLK_P<0> | NO_TEST=TRUE | 85 89 |
| 1743 GDDR_D1_WCK0 | GDDR_WCK_PHY | GDDR_D_1_WCK | FB_D1_WCLK_N<0> | NO_TEST=TRUE | 85 89 |
| 1742 GDDR_D1_WCK1 | GDDR_WCK_PHY | GDDR_D_1_WCK | FB_D1_WCLK_P<1> | NO_TEST=TRUE | 85 89 |
| 1742 GDDR_D1_WCK1 | GDDR_WCK_PHY | GDDR_D_1_WCK | FB_D1_WCLK_N<1> | NO_TEST=TRUE | 85 89 |

SYNC_MASTER=D8_MLB SYNC_DATE=12/20/2011

PAGE TITLE
# GDDR5 FB C/D CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 6.1.0

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# Backlight Controller

## BLC-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| BLC_P6MM | * | Y | 0.600 MM | 0.100 MM | 3.0 MM | =STANDARD | =STANDARD |
| BLC_P3MM | * | Y | 0.300 MM | 0.100 MM | 3.0 MM | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| POWER_BLC | * | BLC_P6MM |
| POWER_BLC_RET | * | BLC_P3MM |
| BLC_CTL_PHY | * | BLC_P3MM |

## BLC-specific Spacing Definitions
## BLC High Voltage Output

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| BLC_HV_ISO | * | 1.00MM | 1000 |

## Constraints
## BLC High Voltage Output

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| BLC_HV | BLC_HV | * | BLC_CTL_ISO |
| BLC_HV | * | * | BLC_HV_ISO |

## BLC Baddies

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| PHASE_ISO | * | =8:1_SPACING | 2000 |
| PHASE_SW2SW | * | =1:1_SPACING | ? |
| PHASE_SW2PWR | * | =2:1_SPACING | ? |
| PHASE_SW2GND | * | =2:1_SPACING | ? |

## BLC Baddies

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| BLC_PHASE | * | * | PHASE_ISO |
| BLC_PHASE | BLC_PHASE | * | PHASE_SW2SW |
| BLC_PHASE | POWER | * | PHASE_SW2PWR |
| BLC_PHASE | GND | * | PHASE_SW2GND |

## BLC Control

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| BLC_CTL_ISO | * | =3:1_SPACING | ? |

## BLC Control

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| BLC_CTL | * | * | BLC_CTL_ISO |

## BKLT MISCELLANEOUS

| Electrical Contraint Set | Physical | Spacing | | |
|---|---|---|---|---|
| SPI | | | | |
| 1556 | SMB_PHY | SMB | SMB_PCH_BLC_SCL | 50 80 |
| 1557 | SMB_PHY | SMB | SMB_PCH_BLC_SDA | 50 80 |
| 1812 | SMB_PHY | SMB | SMB_TCON_BLC_SCL | 50 80 |
| 1811 | SMB_PHY | SMB | SMB_TCON_BLC_SDA | 50 80 |
| 12M REFERENCE CRYSTAL | | | | |
| 1844 | CLK_XTAL | XTAL | BLC_MCU_XTAL_IN | 80 |
| 1845 | CLK_XTAL | XTAL | BLC_MCU_XTAL_OUT | 80 |
| 1846 | CLK_XTAL | XTAL | BLC_MCU_XTAL_OUT_R | 80 |
| 250K REFERENCE CLOCKS | | | | |
| 1848 | CLK_PCH_50S | CLK_PCH | STRCLK_R1 | 80 81 |
| 1849 | CLK_PCH_50S | CLK_PCH | LED_DRVR_CLK | 81 |

| | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| Input Bus | | | | | | | |
| 1766 | POWER_PHY | POWER | 12V | | | PP12V_S0_BLC_VIN2 | 80 81 82 |
| 1772 | POWER_PHY | POWER | 12V | | | PP12V_S0_BLC_VINP | 80 82 |
| 1686 | POWER_PHY | POWER | 14V | | | PRE_REG_OUT | 80 81 |
| 1837 | POWER_PHY | POWER | 3.3V | | | BLC_P3V3S | 80 82 |
| 1857 | POWER_PHY | POWER | 3.3V | | | BLC_P3V3_REF | 80 82 |
| 1838 | POWER_PHY | POWER | 3.3V | | | BLC_P3V3 | |
| 1842 | POWER_PHY | POWER | 3.3V | | | PP3V3_S0_BLC_R | 80 |
| 1843 | POWER_PHY | POWER | 8V | | | SPTX_VIN | 81 |
| 1840 | POWER_PHY | POWER | 8V | | | PP8V_BLC | 80 81 |
| 1847 | POWER_PHY | POWER | 8V | | | BLC_VIN2 | 81 82 |
| 1692 | POWER_PHY | POWER | 14V | | | BOOST_FET_DRAIN | 80 |
| 1853 | POWER_PHY | POWER | 12V | | | BOOST_VDD | 80 |
| 1855 | POWER_PHY | POWER | 5V | | | PP5V_S0_BLC_R | 80 81 82 |
| 1856 | POWER_PHY | POWER | 12V | | | PP12V_S0_BLC_F | 82 |
| Local Ground | | | | | | | |
| 1750 | BLC_CTL_PHY | BLC_PHASE | 0V | | | BLC_GND_1 | 81 82 |
| 1804 | BLC_CTL_PHY | BLC_PHASE | 0V | | | BLC_GND_2 | 81 82 |
| 1805 | BLC_CTL_PHY | BLC_PHASE | 0V | | | BLC_GND_3 | 81 82 |
| 1810 | GND_PHY | GND | 0V | | | AGND_BLC | 81 82 |
| Backlight | | | | | | | |
| 1755 | BLC_CTL_PHY | BLC_PHASE | | | | LED_DRIVER_GATE1 | 81 |
| 1756 | BLC_CTL_PHY | BLC_PHASE | | | | LED_DRIVER_GATE1_R | 81 |
| 1796 | BLC_CTL_PHY | BLC_PHASE | | | | LED_DRIVER_GATE2 | 81 |
| 1797 | BLC_CTL_PHY | BLC_PHASE | | | | LED_DRIVER_GATE2_R | 81 |
| 1798 | BLC_CTL_PHY | BLC_PHASE | | | | LED_DRIVER_GATE3 | 81 |
| 1799 | BLC_CTL_PHY | BLC_PHASE | | | | LED_DRIVER_GATE3_R | 81 |
| 1795 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRVR_CS_RC_1 | 81 |
| 1775 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRVR_CS_RC_2 | 81 |
| 1776 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRVR_CS_RC_3 | 81 |
| 1803 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_CS1 | 81 |
| 1808 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_CS2 | 81 |
| 1809 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_CS3 | 81 |
| 1878 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRVR_CS_C1 | 81 |
| 1879 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRVR_CS_C2 | 81 |
| 1880 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRVR_CS_C3 | 81 |
| 1813 | BLC_CTL_PHY | BLC_HV | 80V | | | LED_DRIVER_FDBK_R_1 | 81 |
| 1814 | BLC_CTL_PHY | BLC_HV | 80V | | | LED_DRIVER_FDBK_R_2 | 81 |
| 1841 | BLC_CTL_PHY | BLC_HV | 80V | | | LED_DRIVER_FDBK_R_3 | 81 |
| 1818 | BLC_CTL_PHY | BLC_CTL | 80V | | | LED_DRIVER_FDBK1 | 81 |
| 1819 | BLC_CTL_PHY | BLC_CTL | 80V | | | LED_DRIVER_FDBK2 | 81 |
| 1820 | BLC_CTL_PHY | BLC_CTL | 80V | | | LED_DRIVER_FDBK3 | 81 |
| 1835 | BLC_CTL_PHY | BLC_CTL | | | | BLC_PWM_1_R | 80 81 |
| 1836 | BLC_CTL_PHY | BLC_CTL | | | | BLC_PWM_2_R | 80 81 |
| 1837 | BLC_CTL_PHY | BLC_CTL | | | | BLC_PWM_3_R | 80 81 |
| 1816 | BLC_CTL_PHY | BLC_CTL | | | | BLC_PWM_1 | 81 82 |
| 1817 | BLC_CTL_PHY | BLC_CTL | | | | BLC_PWM_2 | 81 82 |
| 1818 | BLC_CTL_PHY | BLC_CTL | | | | BLC_PWM_3 | 81 82 |
| 1816 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_REF1 | 81 82 |
| 1817 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_REF2 | 81 82 |
| 1818 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_REF3 | 81 82 |
| 1745 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_COMP1 | 81 |
| 1746 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_COMP2 | 81 |
| 1747 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_COMP3 | 81 |
| 1822 | BLC_CTL_PHY | BLC_CTL | | | | BCOMP1 | 81 |
| 1823 | BLC_CTL_PHY | BLC_CTL | | | | BCOMP2 | 81 |
| 1824 | BLC_CTL_PHY | BLC_CTL | | | | BCOMP3 | 81 |
| 1839 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_FLT1 | 81 |
| 1840 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_FLT2 | 81 |
| 1841 | BLC_CTL_PHY | BLC_CTL | | | | LED_DRIVER_FLT3 | 81 |
| 1862 | BLC_CTL_PHY | BLC_CTL | | | | LED_FLT_R_1 | 81 |
| 1863 | BLC_CTL_PHY | BLC_CTL | | | | LED_FLT_R_2 | 81 |
| 1864 | BLC_CTL_PHY | BLC_CTL | | | | LED_FLT_R_3 | 81 |
| 1866 | BLC_CTL_PHY | BLC_CTL | | | | PRE_REG_OUT_R | 80 |
| 1865 | BLC_CTL_PHY | BLC_CTL | | | | BOOST_FB | 80 |
| 1854 | BLC_CTL_PHY | BLC_CTL | | | | BOOST_COMP | 80 |
| 1857 | BLC_CTL_PHY | BLC_CTL | | | | BOOST_COMP_C | 80 |
| 1870 | BLC_CTL_PHY | BLC_CTL | | | TRUE | BOOST_GDRV | 80 |
| 1871 | BLC_CTL_PHY | BLC_CTL | | | TRUE | BOOST_GDRV_R | 80 |
| 1869 | BLC_CTL_PHY | BLC_CTL | | | | BOOST_ISNS | 80 |
| 1868 | BLC_CTL_PHY | BLC_CTL | | | | BOOST_ISNS_R | 80 |
| 1750 | BLC_CTL_PHY | BLC_HV | 80V | | | LED_DRVR_DRAIN_1 | 81 |
| 1750 | BLC_CTL_PHY | BLC_HV | 80V | | | LED_DRVR_DRAIN_2 | 81 |
| 1750 | BLC_CTL_PHY | BLC_HV | 80V | | | LED_DRVR_DRAIN_3 | 81 |
| OUTPUT BUS | | | | | | | |
| 1749 | POWER_BLC_RET | BLC_HV | 80V | | | IS1_BLC_F | 82 |
| 1749 | POWER_BLC_RET | BLC_HV | 80V | | | IS2_BLC_F | 82 |
| 1750 | POWER_BLC_RET | BLC_HV | 80V | | | IS3_BLC_F | 82 |
| 1751 | POWER_BLC_RET | BLC_HV | 80V | | | IS1_BLC | 81 82 |
| 1752 | POWER_BLC_RET | BLC_HV | 80V | | | IS2_BLC | 81 82 |
| 1753 | POWER_BLC_RET | BLC_HV | 80V | | | IS3_BLC | 81 82 |
| 1781 | POWER_BLC_RET | BLC_HV | 80V | | | BLC_LED_P_1 | 82 |
| 1782 | POWER_BLC_RET | BLC_HV | 80V | | | BLC_LED_N_1 | 82 |
| 1783 | POWER_BLC_RET | BLC_HV | 80V | | | BLC_LED_P_2 | 82 |
| 1785 | POWER_BLC_RET | BLC_HV | 80V | | | BLC_LED_N_2 | 82 |
| 1786 | POWER_BLC_RET | BLC_HV | 80V | | | BLC_LED_P_3 | 82 |
| 1787 | POWER_BLC_RET | BLC_HV | 80V | | | BLC_LED_N_3 | 82 |
| 1825 | POWER_BLC | BLC_HV | 80V | | | BLC_VOUT1 | 81 82 |
| 1825 | POWER_BLC | BLC_HV | 80V | | | BLC_VOUT2 | 81 82 |
| 1825 | POWER_BLC | BLC_HV | 80V | | | BLC_VOUT3 | 81 82 |

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PAGE TITLE
BLC Constraints

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## GPU CORE PHASES

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | | |
| | POWER_PHY | POWER | 12V | | | PP12V_S0_GPUCORE_FLT | 96 97 98 |
| | POWER_PHY | POWER | 5V | | | PP5V_S0_GPU_VCORE_VCC | 96 |
| **Local Ground** | | | | | | | |
| | GND_PHY | GND | 0V | | | AGND_GPU | 96 |
| **Phase 1** | | | | | | | |
| | POWER_PHY | POWER | 12V | | | REG_LVCC_UB510 | 97 |
| | POWER_PHY | POWER | 12V | | | REG_UVCC_UB510 | 97 |
| | VR_CTL_PHY | VR_CTL | | | | REG_PWM_GPUCORE_1 | 96 97 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_PWM1_R | 96 |
| | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_GPUCORE_1 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_GPUCORE_1 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_GPUCORE_1_RC | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_GPUCORE_1 | 97 |
| | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_GPUCORE_1 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_GPUCORE_1 | 97 |
| | POWER_PHY | POWER | 0.9V | | | PPGPUCORE_S0_SENSE_1 | 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISEN_GCORE_1_P | 96 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISEN_GCORE_1_N | 96 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VR_GPU_ISNS1_R_P | 96 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VR_GPU_ISNS1_R_N | 96 |
| ISNS_GPU_CORE | | SENSE | | | | VR_GPU_ISNS1_RR_2 | 96 |
| **Phase 2** | | | | | | | |
| | POWER_PHY | POWER | 12V | | | REG_LVCC_UB530 | 97 |
| | VR_CTL_PHY | VR_CTL | | | | REG_PWM_GPUCORE_2 | 96 97 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_PWM2_R | 96 |
| | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_GPUCORE_2 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_GPUCORE_2 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_GPUCORE_2_RC | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_GPUCORE_2 | 97 |
| | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_GPUCORE_2 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_GPUCORE_2 | 97 |
| | POWER_PHY | POWER | 0.9V | | | PPGPUCORE_S0_SENSE_2 | 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISEN_GCORE_2_P | 96 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISEN_GCORE_2_N | 96 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VR_GPU_ISNS2_R_P | 96 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VR_GPU_ISNS2_R_N | 96 |
| ISNS_GPU_CORE | | SENSE | | | | VR_GPU_ISNS2_RR_2 | 96 |
| **Phase 3** | | | | | | | |
| | POWER_PHY | POWER | 12V | | | REG_VCC_UB550 | 97 |
| | POWER_PHY | POWER | 12V | | | REG_UVCC_UB550 | 97 |
| | POWER_PHY | POWER | 12V | | | REG_LVCC_UB550 | 97 |
| | VR_CTL_PHY | VR_CTL | | | | REG_PWM_GPUCORE_3 | 96 97 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_PWM3_R | 96 |
| | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_GPUCORE_3 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_GPUCORE_3 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_GPUCORE_3_RC | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_GPUCORE_3 | 97 |
| | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_GPUCORE_3 | 97 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_GPUCORE_3 | 97 |
| | POWER_PHY | POWER | 0.9V | | | PPGPUCORE_S0_SENSE_3 | 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISEN_GCORE_3_P | 96 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISEN_GCORE_3_N | 96 97 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VR_GPU_ISNS3_R_P | 96 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VR_GPU_ISNS3_R_N | 96 |
| ISNS_GPU_CORE | | SENSE | | | | VR_GPU_ISNS3_RR_2 | 96 |
| **Phase 4** | | | | | | | |
| | POWER_PHY | POWER | 12V | | | REG_LVCC_UB650 | 98 |
| | VR_CTL_PHY | VR_CTL | | | | REG_PWM_GPUCORE_4 | 96 98 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_PWM4_R | 96 |
| | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_GPUCORE_4 | 98 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_GPUCORE_4 | 98 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_GPUCORE_4_RC | 98 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_GPUCORE_4 | 98 |
| | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_GPUCORE_4 | 98 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_GPUCORE_4 | 98 |
| | POWER_PHY | POWER | 0.9V | | | PPGPUCORE_S0_SENSE_4 | 98 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISEN_GCORE_4_P | 96 98 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | REG_ISEN_GCORE_4_N | 96 98 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VR_GPU_ISNS4_R_P | 96 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VR_GPU_ISNS4_R_N | 96 |
| ISNS_GPU_CORE | | SENSE | | | | VR_GPU_ISNS4_RR_2 | 96 |

## GPU CORE CONTROLLER

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **ISL6334** | | | | | | | |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_COMP | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_COMP_R | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_COMP_RC | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_FB | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_FB_R | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_VDIFF | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_VDF_R1 | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_VDF_R2 | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_TCOMP | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_OFS | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_FS | 96 |
| | | VR_CTL | | | | VR_GPU_EN_VTT | 96 |
| | | VR_CTL | | | | PM_EN_REG_GPUCORE_S0 | 64 96 |
| | | VR_CTL | | | | PM_PGOOD_REG_GPUCORE_S0 | 5 64 96 |
| | | VR_CTL | | | | GPU_PSI_L | 91 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_IOUT | |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_IMON | 51 96 115 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_FAN | 96 115 |
| | | VR_CTL | | | | VR_GPU_VRDHOT | 96 |
| | | VR_CTL | | | | VR_GPU_EN_PWR | |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_SS | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_DAC | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_REF | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_TM | 96 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_IMON | 51 96 115 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_FAN | 96 115 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_VRHOT | |
| | | VR_CTL | | | | GPU_PSI_R | |
| | | VR_CTL | | | | GPU_PSI_L_R | 91 |
| | VR_CTL_PHY | VR_CTL | | | | VR_GPU_IMON_R | 96 |
| VSNS_GPU_VDD | SNS_DIFF_PHY | SENSE | | | | VSNS_GPU_VDD | 93 96 |
| VSNS_GPU_VSS | SNS_DIFF_PHY | SENSE | | | | VSNS_GPU_VSS | 93 96 |
| | SNS_DIFF_PHY | SENSE | | | | VR_GPU_VSEN | 96 |
| | SNS_DIFF_PHY | SENSE | | | | VR_GPU_RGND | 96 |
| **GPU VIDS** | | | | | | | |
| | | VR_VID | | | | REG_GPUCORE_VID7 | 91 96 |
| | | VR_VID | | | | REG_GPUCORE_VID6 | 91 96 |
| | | VR_VID | | | | REG_GPUCORE_VID5 | 91 96 |
| | | VR_VID | | | | REG_GPUCORE_VID4 | 91 96 |
| | | VR_VID | | | | REG_GPUCORE_VID3 | 91 96 |
| | | VR_VID | | | | REG_GPUCORE_VID2 | 91 96 |
| | | VR_VID | | | | REG_GPUCORE_VID1 | 91 96 |
| | | VR_VID | | | | REG_GPUCORE_VID0 | 96 |
| | | VR_VID | | | | GPU_VCORE_VID6 | 91 |
| | | VR_VID | | | | GPU_VCORE_VID5 | 91 |
| | | VR_VID | | | | GPU_VCORE_VID4 | 91 |
| | | VR_VID | | | | GPU_VCORE_VID3 | 91 |
| | | VR_VID | | | | GPU_VCORE_VID2 | 91 |
| | | VR_VID | | | | GPU_VCORE_VID1 | 91 |
| | | VR_VID | | | | GPU_VCORE_VID0 | 91 |
| **Output Bus** | | | | | | | |
| | POWER_PHY | POWER | 0.9V | | | PPVCORE_S0_GPU | 6 |

## GPU FBVDDQ

| Electrical Contraint Set | Physical | Spacing | Voltage | DIDT | NO_TEST | | |
|---|---|---|---|---|---|---|---|
| **Input Bus** | | | | | | | |
| | POWER_PHY | POWER | 5V | | | REG_VCC_UB750 | 99 |
| | POWER_PHY | POWER | 5V | | | REG_PVCC_UB750 | 99 |
| **Local Ground** | | | | | | | |
| | GND_PHY | GND | 0V | | | AGND_FBVDDQ | 99 |
| **FBVDDQ** | | | | | | | |
| | POWER_PHY | VR_SWITCH | 12V | TRUE | | REG_PHASE_FBVDDQ | 99 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_BOOT_FBVDDQ | 99 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_BOOT_FBVDDQ_RC | 99 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_FBVDDQ | 99 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | | REG_UGATE_FBVDDQ_R | |
| | VR_CTL_PHY | VR_LGATE | 12V | TRUE | | REG_LGATE_FBVDDQ | 99 |
| | VR_CTL_PHY | VR_SWITCH | 12V | TRUE | TRUE | REG_SNUBBER_FBVDDQ | 99 |
| | | SENSE | | | | VSNS_FBVDDQ | 94 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VSNS_FBVDDQ_P | 94 99 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | VSNS_FBVDDQ_N | 94 99 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_FBVDDQ_XW_P | 99 |
| ISNS_GPU_CORE | SNS_DIFF_PHY | SENSE | | | | SNS_FBVDDQ_XW_N | 99 |
| | | SENSE | | | | FBVDDQ_SENSE_R | 94 |
| | VR_CTL_PHY | VR_CTL | | | | REG_FBVDDQ_OCSET | |
| | VR_CTL_PHY | VR_CTL | | | | REG_FBVDDQ_VO | 99 |
| | | SENSE | | | | REG_FBVDDQ_FB | 99 |
| | | SENSE | | | | REG_FBVDDQ_RTN | 99 |
| **Output Bus** | | | | | | | |
| | POWER_PHY | POWER | 1.5V | | | PP1V5R1V35_S0_GPU_REG | 6 99 |

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PAGE TITLE
# GPU VREG CONSTRAINTS

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# Caesar IV (Ethernet/SD)

## CIV-specific Physical Rules

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|---|---|---|---|---|---|---|---|
| ENET_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |
| ENET_100D | * | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF | =100_OHM_DIFF |
| SD_50S | * | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =50_OHM_SE | =STANDARD | =STANDARD |

## Physical Net Type to Rule Map

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|---|---|---|
| ENET_COMP_PHY | * | ENET_50S |
| ENET_DIFF_PHY | * | ENET_100D |
| SD_PHY | * | SD_50S |

## CIV-specific Spacing Definitions

Ethernet

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| ENET_DIFF_ISO | * | =6:1_SPACING | ? |
| ENET_DIFF2DIFF | * | =3:1_SPACING | ? |
| ENET_TRANS_ISO | * | 1.27 MM | ? |
| COMP_ENET_ISO | * | =4:1_SPACING | ? |

SD

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---|---|---|---|
| SD_ISO | * | =3:1_SPACING | ? |

## Constraints

Ethernet

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET | |
|---|---|---|---|---|
| ENET_DIFF | * | * | ENET_DIFF_ISO | |
| ENET_DIFF | ENET_DIFF | * | ENET_DIFF2DIFF | |
| ENET_TRANS | * | * | ENET_TRANS_ISO | 2 kV isolation |
| COMP_ENET | * | * | COMP_ENET_ISO | |
| ENET_TRANS | ENET_TRANS | * | ENET_DIFF2DIFF | |

SD

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|---|---|---|---|
| SD | * | * | SD_ISO |

## VENI, VIDI, VICI!

| Electrical Contraint Set | | Physical | Spacing | | | |
|---|---|---|---|---|---|---|
| Ethernet | | | | | | |
| 147G | ENET_MDI_NORM | ENET_DIFF_PHY | ENET_DIFF | ENETCONN_MDI_P<3..0> | | 39 40 |
| 147G | ENET_MDI_NORM | ENET_DIFF_PHY | ENET_DIFF | ENETCONN_MDI_N<3..0> | | 39 40 |
| 147G | | ENET_DIFF_PHY | ENET_TRANS | ENETCONN_MDI_T_P<3..0> | | 40 |
| 147G | | ENET_DIFF_PHY | ENET_TRANS | ENETCONN_MDI_T_N<3..0> | | 40 |
| 146G | | | ENET_TRANS | ENETCONN_MCT3 | | 40 |
| 146G | | | ENET_TRANS | ENETCONN_MCT2 | | 40 |
| 146G | | | ENET_TRANS | ENETCONN_MCT1 | | 40 |
| 146G | | | ENET_TRANS | ENETCONN_MCT0 | | 40 |
| 147G | | ENET_COMP_PHY | COMP_ENET | ENET_RDAC | | 39 |
| SD | | | | | | |
| 147G | SD_DATA | SD_PHY | SD | ENET_CR_DATA<7..0> | NO_TEST=TRUE | 39 |
| 148G | | SD_PHY | SD | SDCONN_DATA<7..0> | | 39 41 |
| 149G | | SD_PHY | SD | SDCONN_DATA_R<7..0> | NO_TEST=TRUE | 41 |
| 148G | SD_CMD | SD_PHY | SD | ENET_SD_CMD | NO_TEST=TRUE | 39 |
| 148G | | SD_PHY | SD | SDCONN_CMD | NO_TEST=TRUE | 39 41 |
| 149G | | SD_PHY | SD | SDCONN_CMD_R | NO_TEST=TRUE | 41 |
| 148G | SD_CLK | SD_PHY | SD | ENET_SD_CLK | NO_TEST=TRUE | 39 |
| 148G | | SD_PHY | SD | SDCONN_CLK | NO_TEST=TRUE | 39 41 |
| 149G | | SD_PHY | SD | SDCONN_CLK_R | NO_TEST=TRUE | 41 |
| 148G | | SD_PHY | SD | ENET_MEDIA_SENSE | | 15 18 39 |
| 148G | | SD_PHY | SD | ENET_SD_DETECT_L | | 39 41 |
| 148G | | SD_PHY | SD | SDCONN_WP | | 39 41 |
| CIV SPI | | | | | | |
| 149G | | SPI_50S | SPI | ENET_SCLK | | 39 |
| 149G | | SPI_50S | SPI | ENET_MISO | | 39 |
| 149G | | SPI_50S | SPI | ENET_MOSI | | 39 |
| 149G | | SPI_50S | SPI | ENET_CS_L | | 39 |

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# AUTO-CONSTRAINTS PG 1

## 4V5_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| H1 | | PM | 4V5_REG_EN | 56 |
| H2 | POWER_PHY | POWER | 4V5_REG_IN | 56 |

## ACDC_*

| | Spacing | Netname | |
|---|---|---|---|
| H3 | PM | ACDC_BURST_EN | 48 |
| H4 | PM | ACDC_BURST_EN_L | 48 |

## ALL_*

| | Spacing | Netname | |
|---|---|---|---|
| H5 | PM | ALL_SYS_PWRGD | 5 47 65 |

## AP_*

| | Spacing | Netname | |
|---|---|---|---|
| H6 | GENERIC_ISO | AP_CLKREQ_L | 15 21 |
| H7 | GENERIC_ISO | AP_CLKREQ_L_ISO | 15 35 |
| H8 | GENERIC_ISO | AP_CLKREQ_Q_L | 35 |
| H9 | GENERIC_ISO | AP_EVENT_L | 35 47 48 |
| H10 | GENERIC_ISO | AP_PWR_EN_ISO | 15 35 |
| H11 | PM | AP_RESET_CONN_L | 35 |
| H12 | PM | AP_RESET_L | 26 35 |
| H13 | PM | AP_WAKE_L | 35 |

## BLC12V_*

| | Spacing | Netname |
|---|---|---|
| H14 | PM | BLC12V_FAULT |
| H15 | PM | BLC12V_FAULT_L |
| H16 | PM | BLC12V_UVLO |
| H17 | PM | BLC12V_UVLO_OUT |
| H18 | PM | BLC12V_UVLO_REF |

## BLC_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| H19 | | GENERIC_ISO | | BLC_BL | 80 82 |
| H20 | | GENERIC_ISO | | BLC_BL_GATE | 82 |
| H21 | | GENERIC_ISO | | BLC_BST | 80 82 |
| H22 | | GENERIC_ISO | | BLC_BST_R | 80 |
| H23 | | GENERIC_ISO | | BLC_BYPASS_GATE | 82 |
| H24 | | GENERIC_ISO | | BLC_DIM_MCU | 80 |
| H25 | | PM | | BLC_EN | 78 80 81 |
| H26 | | GENERIC_ISO | | BLC_ENA | 80 |
| H27 | | GENERIC_ISO | | BLC_ENA1 | 80 82 |
| H28 | | PM | | BLC_EN_DELAY | 78 |
| H29 | | PM | | BLC_EN_R | 80 |

## BLC_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| H30 | | PM | | BLC_EXT_BOOT | 48 80 |
| H31 | | PM | | BLC_EXT_BOOT_L | 80 |
| H32 | BLC_CTL_PHY | BLC_CTL | 5V | BLC_MCU_AOUT_R | 82 |
| H33 | | GENERIC_ISO | | BLC_MCU_BV | 80 82 |
| H34 | | GENERIC_ISO | | BLC_MCU_BV_D | 82 |
| H35 | | GENERIC_ISO | | BLC_MCU_BV_R | 82 |
| H36 | SMB_PHY | SMB | | BLC_MCU_B_SDA_CONN | 80 |
| H37 | | GENERIC_ISO | | BLC_MCU_FLAG_V | 80 |
| H38 | | GENERIC_ISO | | BLC_MCU_PWM5 | 80 |
| H39 | | GENERIC_ISO | | BLC_MCU_PWM5_R | 80 |
| H40 | | PM | | BLC_MCU_RESET | 80 |
| H41 | | PM | | BLC_MCU_RESET_L | 80 |
| H42 | | PM | | BLC_MCU_RESET_R_L | 80 |
| H43 | XDP_PHY | CLK_JTAG | | BLC_MCU_RTCK | 80 |
| H44 | | GENERIC_ISO | | BLC_MCU_RXD0 | 80 |
| H45 | XDP_PHY | XDP | | BLC_MCU_TCK | 80 |
| H46 | XDP_PHY | XDP | | BLC_MCU_TDI | 80 |
| H47 | XDP_PHY | XDP | | BLC_MCU_TDO | 80 |
| H48 | XDP_PHY | XDP | | BLC_MCU_TMS | 80 |
| H49 | XDP_PHY | XDP | | BLC_MCU_TRST | 80 |
| H50 | XDP_PHY | XDP | | BLC_MCU_TXD0 | 80 |
| H51 | | GENERIC_ISO | | BLC_MCU_UVLO | 80 |
| H52 | | GENERIC_ISO | | BLC_ON | 82 |
| H53 | | GENERIC_ISO | | BLC_ON_DRAIN | 82 |
| H54 | | GENERIC_ISO | | BLC_ON_R | 82 |
| H55 | | GENERIC_ISO | | BLC_P_ON | 80 81 82 |
| H56 | | GENERIC_ISO | | BLC_P_ON_BYPASS | 82 |
| H57 | | GENERIC_ISO | | BLC_P_ON_D | 82 |
| H58 | | GENERIC_ISO | | BLC_P_ON_DRAIN | 82 |
| H59 | | GENERIC_ISO | | BLC_P_ON_D_R | 82 |
| H60 | | GENERIC_ISO | | BLC_P_ON_GATE | 82 |
| H61 | | GENERIC_ISO | | BLC_P_ON_R | 82 |
| H62 | | GENERIC_ISO | | BLC_SKIP | 81 |
| H63 | | GENERIC_ISO | | BLC_SNUB_1 | 81 |
| H64 | | GENERIC_ISO | | BLC_SNUB_2 | 81 |
| H65 | | GENERIC_ISO | | BLC_SNUB_3 | 81 |
| H66 | | GENERIC_ISO | | BLC_UVLO | 80 82 |
| H67 | | GENERIC_ISO | | BLC_VIN2_GATE | 82 |
| H68 | | GENERIC_ISO | | BLC_VIN2_SRC | 82 |
| H69 | | GENERIC_ISO | | BLC_VINP_GATE | 82 |
| H70 | | GENERIC_ISO | | BLC_VIN_SNS | 81 |
| H71 | | GENERIC_ISO | | BLC_VSYNC | 78 80 |
| H72 | | GENERIC_ISO | | BLC_VSYNC_R | 80 |

## BOOST_*

| | Spacing | Netname | |
|---|---|---|---|
| H73 | GENERIC_ISO | BOOST_BP | 80 |
| H74 | GENERIC_ISO | BOOST_BYPASS | 80 82 |
| H75 | GENERIC_ISO | BOOST_BYPASS_GATE | 80 |
| H76 | PM | BOOST_EN_GATE | 80 |
| H77 | PM | BOOST_EN_L | 80 |
| H78 | GENERIC_ISO | BOOST_RC | 80 |
| H79 | GENERIC_ISO | BOOST_SS | 80 |

## BT_*

| | Spacing | Netname | |
|---|---|---|---|
| H80 | PM | BT_PWR_EN | 35 |
| H81 | PM | BT_PWR_RST_L | 15 20 35 |
| H82 | PM | BT_PWR_RST_L_Q | 35 |

## BURSTMODE_*

| | Spacing | Netname | |
|---|---|---|---|
| H83 | PM | BURSTMODE_EN | 71 |
| H84 | PM | BURSTMODE_EN_L | 6 48 71 |

## CAM_*

| | Spacing | Netname | |
|---|---|---|---|
| H85 | PM | CAM_EXT_BOOT | 42 43 |
| H86 | PM | CAM_PROC_RESET | 43 |
| H87 | PM | CAM_PROC_RESET_L | 42 43 |

## CPU_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| H88 | | PM | CPU_PWRGD_1V05_R | 28 |
| H89 | | PM | CPU_PWRGD_3V3 | 28 |
| H90 | | PM | CPU_PWRGD_3V3_R | 28 |
| H91 | | GENERIC_ISO | CPU_SKTOCC | 64 |
| H92 | CPU_PHY | CPU | CPU_THRMTRIP_3V3 | 47 48 |
| H93 | CPU_PHY | CPU | CPU_THRMTRIP_R_L | 48 |

## DEBUG_*

| | Spacing | Netname | |
|---|---|---|---|
| H94 | PM | DEBUG_RESET_L | 26 49 |

## DP_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| H95 | | PM | DP_AUXIO_EN | 15 77 79 |
| H96 | | PM | DP_GPU_MUX_EN | 75 |
| H97 | | GENERIC_ISO | DP_INTPNL_HPD | 75 78 |
| H98 | | GENERIC_ISO | DP_INT_EG_HPD | 75 90 |
| H99 | TBT_GEN_55S | TBT_GEN | DP_TBTPA_DDC_CLK | 76 77 |
| H100 | TBT_GEN_55S | TBT_GEN | DP_TBTPA_DDC_DATA | 76 77 |
| H101 | | GENERIC_ISO | DP_TBTPA_HPD | 36 77 |
| H102 | TBT_GEN_55S | TBT_GEN | DP_TBTPB_DDC_CLK | 76 79 |
| H103 | TBT_GEN_55S | TBT_GEN | DP_TBTPB_DDC_DATA | 76 79 |
| H104 | | GENERIC_ISO | DP_TBTPB_HPD | 36 79 |

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# AUTO-CONSTRAINTS PG 2

## ENETCONN_*

| | Spacing | Netname | |
|---|---|---|---|
| 1 | GENERIC_ISO | ENETCONN_TCT | 40 |

## ENET_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 2 | | GENERIC_ISO | ENET_ACT | 40 |
| 3 | | GENERIC_ISO | ENET_ASF_GPIO | 47 48 |
| 4 | | GENERIC_ISO | ENET_CLKREQ_L | 15 18 40 |
| 5 | | PM | ENET_CLKREQ_L_Q | 39 40 |
| 6 | | PM | ENET_CR_1V8_EN | |
| 7 | | PM | ENET_CR_1V8_EN_R | |
| 8 | | PM | ENET_CR_3V3_EN_L | |
| 9 | | PM | ENET_CR_3V3_EN_L_R | |
| 10 | | PM | ENET_CR_PWREN | 39 41 |
| 11 | XDP_PHY | XDP | ENET_LOW_PWR | 26 39 41 |
| 12 | | PM | ENET_PWR_EN_L | 40 |
| 13 | | PM | ENET_PWR_EN_L_R | 40 |
| 14 | | PM | ENET_RESET_L | 39 41 |
| 15 | | PM | ENET_SD_RESET_L | 26 41 |
| 16 | | GENERIC_ISO | ENET_SR_DISABLE | 39 |
| 17 | | GENERIC_ISO | ENET_SR_LX | 39 40 |
| 18 | | PM | ENET_WAKE_L | 40 |

## FAN_*

| | Spacing | Netname | |
|---|---|---|---|
| 19 | GENERIC_ISO | FAN_0_PWM_FET | 54 |
| 20 | GENERIC_ISO | FAN_0_PWM_FILT | 54 |
| 21 | GENERIC_ISO | FAN_0_TACH_FET | 54 |
| 22 | GENERIC_ISO | FAN_0_TACH_FILT | 54 |

## FBVDD_*

| | Spacing | Netname | |
|---|---|---|---|
| 23 | GENERIC_ISO | FBVDD_ALTVO | 91 99 |

## FB_*

| | Spacing | Netname | |
|---|---|---|---|
| 24 | GENERIC_ISO | FB_A0_VREFC | 86 |
| 25 | GENERIC_ISO | FB_A0_VREFD | 86 |
| 26 | GENERIC_ISO | FB_A1_VREFC | 86 |
| 27 | GENERIC_ISO | FB_A1_VREFD | 86 |
| 28 | GENERIC_ISO | FB_B0_VREFC | 87 |
| 29 | GENERIC_ISO | FB_B0_VREFD | 87 |
| 30 | GENERIC_ISO | FB_B1_VREFC | 87 |
| 31 | GENERIC_ISO | FB_B1_VREFD | 87 |
| 32 | GENERIC_ISO | FB_C0_VREFC | 88 |
| 33 | GENERIC_ISO | FB_C0_VREFD | 88 |
| 34 | GENERIC_ISO | FB_C1_VREFC | 88 |
| 35 | GENERIC_ISO | FB_C1_VREFD | 88 |
| 36 | GENERIC_ISO | FB_D0_VREFC | 89 |
| 37 | GENERIC_ISO | FB_D0_VREFD | 89 |
| 38 | GENERIC_ISO | FB_D1_VREFC | 89 |
| 39 | GENERIC_ISO | FB_D1_VREFD | 89 |
| 40 | GENERIC_ISO | FB_SW_LEG_A | 84 86 |

## FB_*

| | Spacing | Netname | |
|---|---|---|---|
| 41 | GENERIC_ISO | FB_SW_LEG_B | 84 87 |
| 42 | GENERIC_ISO | FB_SW_LEG_C | 85 88 |
| 43 | GENERIC_ISO | FB_SW_LEG_D | 85 89 |
| 44 | GENERIC_ISO | FB_VREF_GPU | 94 |

## FET_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| 45 | | GENERIC_ISO | | FET_EN_P12V_S0 | 74 |
| 46 | | GENERIC_ISO | | FET_EN_P12V_S0_BLC | 74 |
| 47 | | GENERIC_ISO | | FET_EN_P12V_S0_BLC_R | 74 |
| 48 | | GENERIC_ISO | | FET_EN_P12V_S0_R | 74 |
| 49 | | GENERIC_ISO | | FET_EN_P12V_S5 | 74 |
| 50 | | GENERIC_ISO | | FET_EN_P12V_S5_R | 74 |
| 51 | | GENERIC_ISO | | FET_EN_VDDQ_S0 | 74 |
| 52 | | GENERIC_ISO | | FET_HDD_SLGSW | 52 |
| 53 | POWER_PHY | POWER | 12V | FET_VCC_U7950 | 74 |
| 54 | POWER_PHY | POWER | 12V | FET_VCC_U7970 | 74 |
| 55 | POWER_PHY | POWER | 12V | FET_VCC_U7980 | 74 |

## FLAG_*

| | Spacing | Netname | |
|---|---|---|---|
| 56 | GENERIC_ISO | FLAG_V | 80 81 82 |

## G3_*

| | Spacing | Netname | |
|---|---|---|---|
| 57 | GENERIC_ISO | G3_POWERON_L | 47 48 |

## GND_*

| | Spacing | Netname | |
|---|---|---|---|
| 58 | SENSE | GND_SMC_AVSS | 47 48 51 55 |

## GPU_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 59 | | GENERIC_ISO | GPU_ALT_VREF | 84 85 91 |
| 60 | | GENERIC_ISO | GPU_BUFRSTN | 91 |
| 61 | | GENERIC_ISO | GPU_IFPAB_PLLVDD | 90 |
| 62 | | GENERIC_ISO | GPU_IFPA_IOVDD | 90 |
| 63 | | GENERIC_ISO | GPU_IFPB_IOVDD | 90 |
| 64 | | GENERIC_ISO | GPU_IFPC_IOVDD | 90 |
| 65 | | GENERIC_ISO | GPU_IFPC_PLLVDD | 90 |
| 66 | XDP_PHY | XDP | GPU_JTAG_TDI | 91 |
| 67 | XDP_PHY | XDP | GPU_JTAG_TDO | 91 |
| 68 | XDP_PHY | XDP | GPU_JTAG_TMS | 91 |
| 69 | XDP_PHY | XDP | GPU_JTAG_TRST_L | 91 |
| 70 | | GENERIC_ISO | GPU_MLS_STRAP0 | 91 |
| 71 | | GENERIC_ISO | GPU_MLS_STRAP1 | 91 |

## GPU_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 72 | | GENERIC_ISO | GPU_MLS_STRAP2 | 91 |
| 73 | | GENERIC_ISO | GPU_MLS_STRAP3 | 91 |
| 74 | | GENERIC_ISO | GPU_MLS_STRAP4 | 91 |
| 75 | | GENERIC_ISO | GPU_RESET_L | 26 83 91 |
| 76 | SPI_50S | SPI | GPU_ROM_CS_L | 91 |
| 77 | SPI_50S | SPI | GPU_ROM_CS_L_R | 91 |
| 78 | | GENERIC_ISO | GPU_ROM_HOLD_L | 91 |
| 79 | SPI_50S | SPI | GPU_ROM_SI | 91 |
| 80 | SPI_50S | SPI | GPU_ROM_SI_R | 91 |
| 81 | SPI_50S | SPI | GPU_ROM_SO | 91 |
| 82 | SPI_50S | SPI | GPU_ROM_SO_R | 91 |
| 83 | SPI_50S | SPI | GPU_ROM_WP_L | 91 |

## HDD_*

| | Spacing | Netname | |
|---|---|---|---|
| 84 | GENERIC_ISO | HDD_12V_S0_GATE | 52 |
| 85 | GENERIC_ISO | HDD_OOB_1V00_REF | 52 |
| 86 | PM | HDD_PWR_EN | 21 52 |
| 87 | GENERIC_ISO | HDD_PWR_EN_L | 52 |
| 88 | GENERIC_ISO | HDD_PWR_EN_R | 52 |

## I2C_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 89 | SMB_PHY | SMB | I2C_TCON_MAS_SCL | 50 78 |
| 90 | SMB_PHY | SMB | I2C_TCON_MAS_SDA | 50 78 |

## IFPD_*

| | Spacing | Netname | |
|---|---|---|---|
| 91 | GENERIC_ISO | IFPD_RSET | 90 |

## IFPEF_*

| | Spacing | Netname | |
|---|---|---|---|
| 92 | GENERIC_ISO | IFPEF_RSET | 90 |

## ISNSA_*

| | Electrical | Physical | Spacing | Netname | |
|---|---|---|---|---|---|
| 93 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VG3H_N | 51 |
| 94 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VG3H_P | 51 |
| 95 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_CPU_P1V05_N | 55 |
| 96 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_CPU_P1V05_P | 55 |
| 97 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_CPU_VCCSA_N | 55 |
| 98 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_CPU_VCCSA_P | 55 |
| 99 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_FBVDDQ_N | 51 |
| 100 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_FBVDDQ_P | 51 |
| 101 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_HDD_N | 51 |
| 102 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_HDD_P | 51 |

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# AUTO-CONSTRAINTS PG 3

## ISNSA_*

| | Electrical | Physical | Spacing | Netname | |
|---|---|---|---|---|---|
| H1 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_P1V05_N | 55 |
| H2 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P12VS0_P1V05_P | 55 |
| H3 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P1V05S0_PCH_N | 51 |
| H4 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P1V05S0_PCH_P | 51 |
| H5 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P1V5S0_CPU_MEM_N | 51 |
| H6 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P1V5S0_CPU_MEM_P | 51 |
| H7 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P3V3S0_SSD_N | 51 |
| H8 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P3V3S0_SSD_P | 51 |
| H9 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P3V3S4_AP_N | 55 |
| H10 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P3V3S4_AP_P | 55 |
| H11 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P5VS0_HDD_N | 51 |
| H12 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_P5VS0_HDD_P | 51 |
| H13 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_PVDDQS3_DDR_N | 51 |
| H14 | SNS_CURRENT | SNS_DIFF_PHY | SENSE | ISNSA_PVDDQS3_DDR_P | 51 |

## ISNS_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| H15 | SNS_PHY | SENSE | ISNS_CPUAXG_FB | 51 |
| H16 | SNS_PHY | SENSE | ISNS_CPUAXG_N | 51 |
| H17 | SNS_PHY | SENSE | ISNS_CPUAXG_P | 51 |
| H18 | SNS_PHY | SENSE | ISNS_CPUCORE_FB | 51 |
| H19 | SNS_PHY | SENSE | ISNS_CPUCORE_N | 51 |
| H20 | SNS_PHY | SENSE | ISNS_CPUCORE_P | 51 |
| H21 | SNS_PHY | SENSE | ISNS_GPUCORE_FB | 51 |
| H22 | SNS_PHY | SENSE | ISNS_GPUCORE_N | 51 |
| H23 | SNS_PHY | SENSE | ISNS_GPUCORE_P | 51 |
| H24 | SNS_PHY | SENSE | ISNS_P12VG3H_R | 51 |
| H25 | SNS_PHY | SENSE | ISNS_P12VS0_CPU_P1V05_R | 55 |
| H26 | SNS_PHY | SENSE | ISNS_P12VS0_CPU_VCCSA_R | 55 |
| H27 | SNS_PHY | SENSE | ISNS_P12VS0_FBVDDQ_R | 51 |
| H28 | SNS_PHY | SENSE | ISNS_P12VS0_HDD_R | 51 |
| H29 | SNS_PHY | SENSE | ISNS_P12VS0_P1V05_R | 55 |
| H30 | SNS_PHY | SENSE | ISNS_P1V05S0_PCH_R | 51 |
| H31 | SNS_PHY | SENSE | ISNS_P1V5S0_CPU_MEM_R | 51 |
| H32 | SNS_PHY | SENSE | ISNS_P3V3S0_SSD_R | 51 |
| H33 | SNS_PHY | SENSE | ISNS_P3V3S4_AP_R | 55 |
| H34 | SNS_PHY | SENSE | ISNS_P5VS0_HDD_R | 51 |
| H35 | SNS_PHY | SENSE | ISNS_PVDDQS3_DDR_R | 51 |

## ISOLATE_*

| | Spacing | Netname | |
|---|---|---|---|
| H36 | PM | ISOLATE_CPU_MEM_5V | 28 |
| H37 | PM | ISOLATE_CPU_MEM_5V_L | 28 |

## JTAG_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| H38 | XDP_PHY | XDP | JTAG_GMUX_TMS | 20 |
| H39 | XDP_PHY | XDP | JTAG_TBT_TDI | 15 21 |
| H40 | XDP_PHY | XDP | JTAG_TBT_TDI_ISOL | 15 36 |
| H41 | XDP_PHY | XDP | JTAG_TBT_TDO | 15 21 |
| H42 | XDP_PHY | XDP | JTAG_TBT_TDO_ISOL | 15 36 |
| H43 | XDP_PHY | XDP | JTAG_TBT_TMS | 15 18 |
| H44 | XDP_PHY | XDP | JTAG_TBT_TMS_ISOL | 15 36 |

## LED_*

| | Spacing | Netname | |
|---|---|---|---|
| H45 | PM | LED_DRIVER_EN | 81 82 |
| H46 | PM | LED_DRIVER_EN_L | 82 |
| H47 | PM | LED_DRIVER_EN_L_R | 82 |
| H48 | GENERIC_ISO | LED_DRIVER_OVP1 | 81 82 |
| H49 | GENERIC_ISO | LED_DRIVER_OVP1P | 80 81 |
| H50 | GENERIC_ISO | LED_DRIVER_OVP1_OUT | 81 |
| H51 | GENERIC_ISO | LED_DRIVER_OVP2 | 81 82 |
| H52 | GENERIC_ISO | LED_DRIVER_OVP2P | 80 81 |
| H53 | GENERIC_ISO | LED_DRIVER_OVP2_OUT | 81 |
| H54 | GENERIC_ISO | LED_DRIVER_OVP3 | 81 82 |
| H55 | GENERIC_ISO | LED_DRIVER_OVP3P | 80 81 |
| H56 | GENERIC_ISO | LED_DRIVER_OVP3_OUT | 81 |

## LPCPLUS_*

| | Spacing | Netname | |
|---|---|---|---|
| H57 | GENERIC_ISO | LPCPLUS_GPIO | 21 49 |

## LPC_*

| | Spacing | Netname | |
|---|---|---|---|
| H58 | GENERIC_ISO | LPC_PWRDWN_L | 19 26 47 49 |
| H59 | GENERIC_ISO | LPC_SERIRQ | 18 47 49 |

## MEMVTT_*

| | Spacing | Netname | |
|---|---|---|---|
| H60 | PM | MEMVTT_EN | 28 64 |
| H61 | PM | MEMVTT_EN_L | 28 |

## MEM_*

| | Spacing | Netname | |
|---|---|---|---|
| H62 | GENERIC_ISO | MEM_EVENT_L | 29 30 31 32 47 48 |

## MOJO_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| H63 | XDP_PHY | XDP | MOJO_RX_L | 45 47 48 |
| H64 | XDP_PHY | XDP | MOJO_TX_L | 45 47 48 |

## OCA_*

| | Spacing | Netname | |
|---|---|---|---|
| H65 | GENERIC_ISO | OCA_FET_DRAIN | 82 |

## OVP_*

| | Spacing | Netname | |
|---|---|---|---|
| H66 | GENERIC_ISO | OVP_OREF | 82 |
| H67 | GENERIC_ISO | OVP_OUT1 | 82 |
| H68 | GENERIC_ISO | OVP_OUT1_R | 82 |
| H69 | GENERIC_ISO | OVP_OUT2 | 82 |
| H70 | GENERIC_ISO | OVP_OUT2_R | 82 |
| H71 | GENERIC_ISO | OVP_OUT3 | 82 |
| H72 | GENERIC_ISO | OVP_OUT3_R | 82 |

## P1V2_*

| | Spacing | Netname | |
|---|---|---|---|
| H73 | PM | P1V2_S4_EN | 43 |

## P1V8_*

| | Spacing | Netname | |
|---|---|---|---|
| H74 | PM | P1V8_S4_EN | 43 |

## P3V3AP_*

| | Spacing | Netname | |
|---|---|---|---|
| H75 | GENERIC_ISO | P3V3AP_VMON | 35 |

## P3V3_*

| | Spacing | Netname | |
|---|---|---|---|
| H76 | GENERIC_ISO | P3V3_S0_EN_G | 74 |
| H77 | GENERIC_ISO | P3V3_S3_EN_G | 74 |

## P3V42G3H_*

| | Spacing | Netname | |
|---|---|---|---|
| H78 | GENERIC_ISO | P3V42G3H_BOOST | 73 |

## P5V_*

| | Spacing | Netname | |
|---|---|---|---|
| H79 | GENERIC_ISO | P5V_S0_EN_G | 74 |

## PCA9557D_*

| | Spacing | Netname | |
|---|---|---|---|
| H80 | GENERIC_ISO | PCA9557D_RESET_L | 26 28 34 |

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## PCH_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| | | PM | PCH_BLC_EXT_BOOT | 21 80 |
| | | PM | PCH_BLC_EXT_BOOT_R | 15 21 |
| | | PM | PCH_BLC_MCU_RESET | 21 80 |
| | | PM | PCH_BLC_MCU_RESET_R | 15 21 |
| | | PM | PCH_CAM_RESET | 15 21 |
| | | PM | PCH_CAM_RESET_R | 21 43 |
| | | GENERIC_ISO | PCH_DSWVRMEN | 19 |
| | CPU_PHY | CPU | PCH_PECI | 21 |
| | CPU_PHY | CPU | PCH_PROCPWRGD | 21 |
| | | GENERIC_ISO | PCH_RCIN_L | 21 |
| | | GENERIC_ISO | PCH_RI_L | 19 |
| | | GENERIC_ISO | PCH_SMBALERT_L | 15 18 |
| | | GENERIC_ISO | PCH_SRTCRST_L | 18 |
| | | GENERIC_ISO | PCH_STRP_TOPBLK_SWP_L | 20 |
| | | GENERIC_ISO | PCH_SUSWARN_L | 15 19 |

## PCIE_*

| | Spacing | Netname | |
|---|---|---|---|
| | GENERIC_ISO | PCIE_CLKREQ5_GPIO44_L | 18 |
| | PM | PCIE_WAKE_L | 19 35 40 |

## PEG_*

| | Spacing | Netname | |
|---|---|---|---|
| | GENERIC_ISO | PEG_CLKREQ_L | 15 18 83 |

## PGOOD_*

| | Spacing | Netname | |
|---|---|---|---|
| | PM | PGOOD_P1V5_S0_DLY | 28 |

## PLT_*

| | Spacing | Netname | |
|---|---|---|---|
| | PCH | PLT_RESET_L | 20 26 |
| | PCH | PLT_RST_BUF_L | 26 |

## PM_*

| | Spacing | Netname | |
|---|---|---|---|
| | PM | PM_CLKRUN_L | 47 48 49 |
| | PM | PM_DSW_PWRGD | 47 48 65 |
| | PM | PM_EN_FET_P12V_S0 | 64 74 |
| | PM | PM_EN_FET_P12V_S0_R | 74 |
| | PM | PM_EN_FET_P3V3_S0 | 64 74 |
| | PM | PM_EN_FET_P3V3_S4 | 64 74 |
| | PM | PM_EN_FET_P5V_S0 | 64 74 |
| | PM | PM_EN_FET_VDDQ_S0 | 64 74 |
| | PM | PM_EN_LDO_DDRVTT_S0 | 64 72 |
| | PM | PM_EN_REG_CPUCORE_S0 | 64 66 |

## PM_*

| | Spacing | Netname | |
|---|---|---|---|
| | PM | PM_EN_REG_CPU_P1V05_S0 | 64 69 |
| | PM | PM_EN_REG_FBVDDQ_S0 | 64 99 |
| | PM | PM_EN_REG_GPUCORE_S0_R | 96 |
| | PM | PM_EN_REG_P1V05_S0 | 64 99 |
| | PM | PM_EN_REG_P1V8_S0 | 64 72 |
| | PM | PM_EN_REG_P3V3_S5 | 64 71 74 |
| | PM | PM_EN_REG_P5V_S4 | 64 71 |
| | PM | PM_EN_REG_VCCSA_S0 | 64 70 |
| | PM | PM_EN_REG_VDDQ_S3 | 64 72 |
| | PM | PM_EN_S0 | 64 |
| | PM | PM_EN_S4 | 64 |
| | PM | PM_EN_USB_PWR | 45 46 64 |
| | PM | PM_LED_A_ALL_SYS_PWRGD | 5 |
| | PM | PM_LED_A_BLC_GOOD | 5 |
| | PM | PM_LED_A_CPUAXG_PGOOD | 5 |
| | PM | PM_LED_A_GPU_GOOD | 5 |
| | PM | PM_LED_A_PGOOD_CPUCORE_S0 | 5 |
| | PM | PM_LED_A_PGOOD_CPU_P1V05_S0 | 5 |
| | PM | PM_LED_A_PGOOD_REG_FBVDDQ_S0 | 5 |
| | PM | PM_LED_A_PGOOD_REG_GPUCORE_S0 | 5 |
| | PM | PM_LED_A_PGOOD_REG_P1V05 | 5 |
| | PM | PM_LED_A_PGOOD_REG_VDDQ_S3 | 5 |
| | PM | PM_LED_A_S4 | 5 |
| | PM | PM_LED_A_S5 | 5 |
| | PM | PM_LED_A_SLP_S3 | 5 |
| | PM | PM_LED_A_VIDEO_ON | 5 |
| | PM | PM_LED_K_ALL_SYS_PWRGD | 5 |
| | PM | PM_LED_K_BLC_GOOD | 5 |
| | PM | PM_LED_K_CPUAXG_PGOOD | 5 |
| | PM | PM_LED_K_GPU_GOOD | 5 |
| | PM | PM_LED_K_PGOOD_CPUCORE_S0 | 5 |
| | PM | PM_LED_K_PGOOD_CPU_P1V05_S0 | 5 |
| | PM | PM_LED_K_PGOOD_REG_FBVDDQ_S0 | 5 |
| | PM | PM_LED_K_PGOOD_REG_GPUCORE_S0 | 5 |
| | PM | PM_LED_K_PGOOD_REG_P1V05 | 5 |
| | PM | PM_LED_K_PGOOD_REG_VDDQ_S3 | 5 |
| | PM | PM_LED_K_SLP_S3 | 5 |
| | PM | PM_MEM_PWRGD_L | 28 |
| | PM | PM_PCH_APWROK | 19 65 |
| | PM | PM_PCH_PWROK | 15 19 26 35 43 65 80 |
| | PM | PM_PCH_PWROK_APWROK | 65 |
| | PM | PM_PCH_SYS_PWROK | 19 48 65 |
| | PM | PM_PGOOD_FBVDDQ_VDDQ_S0 | 64 |
| | PM | PM_PGOOD_FET_P12V_S0 | 74 |
| | PM | PM_PGOOD_FET_P12V_S0_BLC | 74 82 |
| | PM | PM_PGOOD_FET_P12V_S5 | 74 |
| | PM | PM_PGOOD_FET_P3V3_S0 | 64 74 |
| | PM | PM_PGOOD_FET_P5V_S0 | 64 74 |
| | PM | PM_PGOOD_FET_VDDQ_S0 | 28 64 74 |
| | PM | PM_PGOOD_P3V3_S4_FET | 27 35 64 74 |
| | PM | PM_PGOOD_REG_ALL_P1V05_S0 | 64 65 |
| | PM | PM_PGOOD_REG_ALL_P1V05_S0_R | 28 64 |
| | PM | PM_PGOOD_REG_CPUCORE_S0 | 5 25 65 66 |
| | PM | PM_PGOOD_REG_CPU_P1V05_S0 | 5 64 69 |
| | PM | PM_PGOOD_REG_FBVDDQ_S0 | 5 64 99 |
| | PM | PM_PGOOD_REG_P1V05_S0 | 5 64 99 |
| | PM | PM_PGOOD_REG_P1V8_S0 | 64 72 |
| | PM | PM_PGOOD_REG_P3V3_S5 | 65 71 |
| | PM | PM_PGOOD_REG_P5V_S4 | 64 71 |
| | PM | PM_PGOOD_REG_VCCSA_S0 | 64 65 70 |
| | PM | PM_PGOOD_REG_VDDQ_S3 | 5 64 72 |
| | PM | PM_PWRBTN_L | 15 19 25 47 |
| | PM | PM_RSMRST_PCH_L | 19 65 |
| | PM | PM_RSMRST_PCH_L_R | 65 |
| | PM | PM_SLP_S3_L | 5 15 19 28 40 47 48 64 |
| | PM | PM_SLP_S4_L | 15 19 47 64 |
| | PM | PM_SLP_S5_L | 15 19 47 64 |
| | PCH | PM_SYSRST_L | 19 25 26 47 |
| | PCH | PM_THRMTRIP_L | 21 48 |
| | PM | PGOOD_P12V_S0_R | 65 |
| | PM | PGOOD_P12V_S0 | 64 65 74 |

## PP12V_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| | POWER_PHY | POWER | 12V | PP12V_LCD | 78 |
| | POWER_PHY | POWER | 12V | PP12V_LCD_EXT | 78 |
| | POWER_PHY | POWER | 12V | PP12V_S0_FAN_0_FILT | 54 |
| | POWER_PHY | POWER | 12V | PP12V_S0_HDD_FET | 44 52 |

## PP1V05_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| | POWER_PHY | POWER | 1.05V | PP1V05_S0_PCH_VCCADPLLA_F | 17 22 |
| | POWER_PHY | POWER | 1.05V | PP1V05_S0_PCH_VCCADPLLB_F | 17 22 |

## PP1V2_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| | POWER_PHY | POWER | 1.2V | PP1V2_ENET_INTREG | 40 |
| | POWER_PHY | POWER | 1.2V | PP1V2_G3H_SMC_VDDC | 47 |
| | POWER_PHY | POWER | 1.2V | PP1V2_S4_ENET_PHY_AVDDL | 39 |
| | POWER_PHY | POWER | 1.2V | PP1V2_S4_ENET_PHY_GPHYPLL | 39 |
| | POWER_PHY | POWER | 1.2V | PP1V2_S4_ENET_PHY_PCIEPLL | 39 |
| | POWER_PHY | POWER | 1.2V | PP1V2_USB_HUB_CRFILT | 27 |
| | POWER_PHY | POWER | 1.2V | PP1V2_USB_HUB_PLLFILT | 27 |

## PP1V5_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| | POWER_PHY | POWER | 1.5V | PP1V5_S0_DP_BIAS | 75 |

## PP1V8_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| | POWER_PHY | POWER | 1.8V | PP1V8_S0_PCH_VCCVRM_F | 22 24 |

## PP3V3R1V8_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| | POWER_PHY | POWER | PP3V3R1V8_ENET_LR_OUT_REG | 39 |

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## PP3V3RHV_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| I34 | POWER_PHY | POWER | 12V | PP3V3RHV_SW_TBTAPWR | 77 |
| I35 | POWER_PHY | POWER | 12V | PP3V3RHV_SW_TBTBPWR | 79 |

## PP3V3_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| I3 | POWER_PHY | POWER | 3.3V | PP3V3_DMIC_CONN | 42 |
| I4 | POWER_PHY | POWER | 3.3V | PP3V3_G3H_AVREF_SMC | 47 48 |
| I5 | POWER_PHY | POWER | 3.3V | PP3V3_G3H_BT_FET | 35 |
| I6 | POWER_PHY | POWER | 3.3V | PP3V3_G3H_BT_FLT | 35 |
| I7 | POWER_PHY | POWER | 3.3V | PP3V3_G3H_SMC_USBMUX_R | 45 |
| I8 | POWER_PHY | POWER | 3.3V | PP3V3_G3H_SMC_VDDA | 47 |
| I9 | POWER_PHY | POWER | 3.3V | PP3V3_G3_RTC | 6 26 |
| I10 | POWER_PHY | POWER | 3.3V | PP3V3_PVDDQS3_ISNS | 51 |
| I11 | POWER_PHY | POWER | 3.3V | PP3V3_S0_PCH_VCCA_DAC_F | 17 22 |
| I12 | POWER_PHY | POWER | 3.3V | PP3V3_S0_SSD_FLT | 44 |
| I13 | POWER_PHY | POWER | 3.3V | PP3V3_S0_SW_SD_PWR | 41 |
| I14 | POWER_PHY | POWER | 3.3V | PP3V3_S4_ALS_F | 42 |
| I15 | POWER_PHY | POWER | 3.3V | PP3V3_S4_AP_FET | 35 |
| I16 | POWER_PHY | POWER | 3.3V | PP3V3_S4_AP_FLT | 35 |
| I17 | POWER_PHY | POWER | 3.3V | PP3V3_S4_ENET_FET_AVDDH | 39 |
| I18 | POWER_PHY | POWER | 3.3V | PP3V3_S4_ENET_FET_BIASVDDH | 39 |
| I19 | POWER_PHY | POWER | 3.3V | PP3V3_S4_ENET_FET_SRVDD | 39 |
| I20 | POWER_PHY | POWER | 3.3V | PP3V3_S4_ENET_FET_XTALVDDH | 39 |
| I21 | POWER_PHY | POWER | 3.3V | PP3V3_S4_USB_HUB_VDD | 27 |
| I22 | POWER_PHY | POWER | 3.3V | PP3V3_S5_XDP_R | 25 |

## PP4V5_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| I23 | POWER_PHY | POWER | 4.5V | PP4V5_AUDIO_ANALOG | 56 60 62 |

## PP5V_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| I24 | POWER_PHY | POWER | 5V | PP5V_AUDIO_HPAMP | 56 57 |
| I25 | POWER_PHY | POWER | 5V | PP5V_S0_HDD_FET | 44 52 |
| I26 | POWER_PHY | POWER | 5V | PP5V_S0_PCH_V5REF | 24 |
| I27 | POWER_PHY | POWER | 5V | PP5V_S4_EXTA | 45 |
| I28 | POWER_PHY | POWER | 5V | PP5V_S4_EXTA_F | 45 |
| I29 | POWER_PHY | POWER | 5V | PP5V_S4_EXTB | 45 |
| I30 | POWER_PHY | POWER | 5V | PP5V_S4_EXTB_F | 45 |
| I31 | POWER_PHY | POWER | 5V | PP5V_S4_EXTC | 46 |
| I32 | POWER_PHY | POWER | 5V | PP5V_S4_EXTC_F | 46 |
| I33 | POWER_PHY | POWER | 5V | PP5V_S4_EXTD | 46 |
| I34 | POWER_PHY | POWER | 5V | PP5V_S4_EXTD_F | 46 |
| I35 | POWER_PHY | POWER | 5V | PP5V_S5_PCH_V5REFSUS | 24 |

## PPHV_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| I36 | POWER_PHY | POWER | 12V | PPHV_SW_TBTAPWR | 77 |
| I37 | POWER_PHY | POWER | 12V | PPHV_SW_TBTBPWR | 79 |

## PPVBATT_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| I38 | POWER_PHY | POWER | 3.3V | PPVBATT_G3_RTC | 26 |
| I39 | POWER_PHY | POWER | 3.3V | PPVBATT_G3_RTC_R | 26 |

## PU_*

| | Spacing | Netname | |
|---|---|---|---|
| I40 | GENERIC_ISO | PU_U6900 | 64 |

## PWR_*

| | Spacing | Netname | |
|---|---|---|---|
| I41 | PM | PWR_BTN | 6 48 |
| I42 | PM | PWR_BTN_R | 6 |

## REG_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| I43 | | PM | REG_CPUAXG_PGOOD | 5 66 |
| I44 | | PM | REG_CPUCORE_PGOOD | 66 |
| I45 | CPU_PHY | CPU | REG_CPUCORE_VRHOT_L | 66 |
| I46 | | PM | REG_CPU_P1V05S0_PGOOD | 69 |
| I47 | VR_CTL_PHY | VR_CTL | REG_FBVDDQ_SET0 | 99 |
| I48 | VR_CTL_PHY | VR_CTL | REG_FBVDDQ_SET1 | 99 |
| I49 | VR_CTL_PHY | VR_CTL | REG_FBVDDQ_SET1_R | 99 |
| I50 | VR_CTL_PHY | VR_CTL | REG_FBVDDQ_SREF | 99 |
| I51 | | PM | REG_P1V8S0_PGOOD | 72 |
| I52 | | PM | REG_P3V3S5_PGOOD | 71 |
| I53 | | PM | REG_P5VS4_PGOOD | 71 |
| I54 | | PM | REG_VCCSAS0_PGOOD | 70 |
| I55 | | PM | REG_VDDQS3_PGOOD | 72 |

## RTC_*

| | Spacing | Netname | |
|---|---|---|---|
| I56 | PM | RTC_RESET_L | 18 26 48 |
| I57 | PM | RTC_RESET_L_R | 48 |

## S5_*

| | Spacing | Netname | |
|---|---|---|---|
| I58 | PM | S5_PWRGD | 47 65 |

## SATALED_*

| | Spacing | Netname | |
|---|---|---|---|
| I59 | GENERIC_ISO | SATALED_L | 44 |

## SDCONN_*

| | Spacing | Netname | |
|---|---|---|---|
| I60 | GENERIC_ISO | SDCONN_DETECT | 41 |
| I61 | GENERIC_ISO | SDCONN_ILIM | 41 |
| I62 | GENERIC_ISO | SDCONN_OC_L | 41 |

## SD_*

| | Spacing | Netname | |
|---|---|---|---|
| I63 | GENERIC_ISO | SD_DETECT_LVL | 41 |

## SLG_*

| | Spacing | Netname | |
|---|---|---|---|
| I64 | PM | SLG_ENET_RESET_L | 41 |
| I65 | PM | SLG_ENET_RESET_R_L | 41 |

## SMBUS_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| I66 | SMB_PHY | SMB | SMBUS_PCH_CLK | 18 50 |
| I67 | SMB_PHY | SMB | SMBUS_PCH_CLK_R | 50 |
| I68 | SMB_PHY | SMB | SMBUS_PCH_DATA | 18 50 |
| I69 | SMB_PHY | SMB | SMBUS_PCH_DATA_R | 50 |
| I70 | SMB_PHY | SMB | SMBUS_SMC_0_S0_SCL | 47 50 |
| I71 | SMB_PHY | SMB | SMBUS_SMC_0_S0_SDA | 47 50 |
| I72 | SMB_PHY | SMB | SMBUS_SMC_1_S0_SCL | 47 50 |
| I73 | SMB_PHY | SMB | SMBUS_SMC_1_S0_SDA | 47 50 |
| I74 | SMB_PHY | SMB | SMBUS_SMC_2_S4_SCL | 47 50 |
| I75 | SMB_PHY | SMB | SMBUS_SMC_2_S4_SDA | 47 50 |
| I76 | SMB_PHY | SMB | SMBUS_SMC_3_SCL | 47 50 |
| I77 | SMB_PHY | SMB | SMBUS_SMC_3_SDA | 47 50 |
| I78 | SMB_PHY | SMB | SMBUS_SMC_4_ASF_SCL | 47 48 50 |
| I79 | SMB_PHY | SMB | SMBUS_SMC_4_ASF_SDA | 47 48 50 |
| I80 | SMB_PHY | SMB | SMBUS_SMC_5_G3H_SCL | 47 48 50 |
| I81 | SMB_PHY | SMB | SMBUS_SMC_5_G3H_SDA | 47 48 50 |

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# AUTO-CONSTRAINTS PG 6

## SMCISNS_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 1 | SNS_PHY | SENSE | SMCISNS_CPUAXG | 48 51 |
| 2 | SNS_PHY | SENSE | SMCISNS_CPUCORE | 48 51 |
| 3 | SNS_PHY | SENSE | SMCISNS_GPUCORE | 48 51 |
| 4 | SNS_PHY | SENSE | SMCISNS_P12VG3H | 48 51 |
| 5 | SNS_PHY | SENSE | SMCISNS_P12VS0_CPU_P1V05 | 48 55 |
| 6 | SNS_PHY | SENSE | SMCISNS_P12VS0_CPU_VCCSA | 48 55 |
| 7 | SNS_PHY | SENSE | SMCISNS_P12VS0_FBVDDQ | 48 51 |
| 8 | SNS_PHY | SENSE | SMCISNS_P12VS0_HDD | 48 51 |
| 9 | SNS_PHY | SENSE | SMCISNS_P12VS0_P1V05 | 48 55 |
| 10 | SNS_PHY | SENSE | SMCISNS_P1V05S0_PCH | 48 51 |
| 11 | SNS_PHY | SENSE | SMCISNS_P1V5S0_CPU_MEM | 48 51 |
| 12 | SNS_PHY | SENSE | SMCISNS_P3V3S0_SSD | 48 51 |
| 13 | SNS_PHY | SENSE | SMCISNS_P3V3S4_AP | 48 55 |
| 14 | SNS_PHY | SENSE | SMCISNS_P5VS0_HDD | 48 51 |
| 15 | SNS_PHY | SENSE | SMCISNS_PVDDQS3_DDR | 48 51 |

## SMCVSNS_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 16 | SNS_PHY | SENSE | SMCVSNS_CPUAXG | 48 51 |
| 17 | SNS_PHY | SENSE | SMCVSNS_CPUCORE | 48 51 |
| 18 | SNS_PHY | SENSE | SMCVSNS_GPUCORE | 48 51 |
| 19 | SNS_PHY | SENSE | SMCVSNS_P12VG3H | 48 51 |
| 20 | SNS_PHY | SENSE | SMCVSNS_P1V05S0_PCH | 48 51 |
| 21 | SNS_PHY | SENSE | SMCVSNS_P1V5S0_CPU_MEM | 48 51 |
| 22 | SNS_PHY | SENSE | SMCVSNS_P3V3S0 | 48 51 |
| 23 | SNS_PHY | SENSE | SMCVSNS_P5VS0_HDD | 48 51 |
| 24 | SNS_PHY | SENSE | SMCVSNS_PVDDQS3_DDR | 48 51 |

## SMC_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 25 | | GENERIC_ISO | SMC_ACDC_ID | 6 48 |
| 26 | | GENERIC_ISO | SMC_ACDC_ID_R | 6 |
| 27 | | PM | SMC_ASSERT_RTCRST | 48 |
| 28 | | GENERIC_ISO | SMC_BLC_MUX_RX_L | 48 80 |
| 29 | | GENERIC_ISO | SMC_BLC_MUX_TX_L | 48 80 |
| 30 | | GENERIC_ISO | SMC_CPU_CATERR_L | 47 48 |
| 31 | CPU_PHY | CPU | SMC_CPU_PECI | 48 |
| 32 | | PM | SMC_DELAYED_PWRGD | 38 47 48 65 |
| 33 | | GENERIC_ISO | SMC_DP_HPD_L | 47 48 |
| 34 | CLK_XTAL | XTAL | SMC_EXTAL | 47 48 |
| 35 | | GENERIC_ISO | SMC_FAN_0_CTL | 47 54 |
| 36 | | GENERIC_ISO | SMC_FAN_0_TACH | 47 54 |
| 37 | | GENERIC_ISO | SMC_GFX_OVERTEMP | 47 48 91 |
| 38 | | GENERIC_ISO | SMC_GFX_OVERTEMP_Q | 91 |
| 39 | | GENERIC_ISO | SMC_GFX_OVERTEMP_R_L | 91 |
| 40 | | PM | SMC_GFX_THROTTLE_L | 47 91 |
| 41 | | PM | SMC_GFX_THROTTLE_R_L | 91 |
| 42 | | PM | SMC_LRESET_L | 26 47 |
| 43 | | PM | SMC_MANUAL_RST_L | 48 |
| 44 | | PM | SMC_ONOFF_L | 47 48 |
| 45 | | SENSE | SMC_OOB1_RX_CN | 44 |
| 46 | | SENSE | SMC_OOB1_RX_FILT | 44 52 |
| 47 | | SENSE | SMC_OOB1_RX_L | 47 52 |
| 48 | | SENSE | SMC_OOB1_RX_R | 52 |
| 49 | | SENSE | SMC_OOB1_TX_L | 47 48 |
| 50 | | SENSE | SMC_OOB2_RX_L | 44 48 |
| 51 | | SENSE | SMC_OOB2_TX_L | 44 48 |
| 52 | CPU_PHY | CPU | SMC_PECI_L | 47 48 |
| 53 | CPU_PHY | CPU | SMC_PECI_L_R | 48 |
| 54 | | PM | SMC_PME_S4_WAKE_L | 35 47 48 |
| 55 | | GENERIC_ISO | SMC_PM_G2_EN | 47 48 74 |
| 56 | | PM | SMC_PM_PCH_SYS_PWROK | 47 48 |
| 57 | | CPU | SMC_PROCHOT | 47 48 |
| 58 | | PM | SMC_RESET_L | 47 48 49 |

## SMC_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 59 | | GENERIC_ISO | SMC_ROMBOOT | 48 49 |
| 60 | | GENERIC_ISO | SMC_RUNTIME_SCI_L | 15 21 47 |
| 61 | | GENERIC_ISO | SMC_RX_L | 47 48 49 |
| 62 | | PM | SMC_S4_WAKESRC_EN | 35 47 48 |
| 63 | | GENERIC_ISO | SMC_TCK | 47 48 49 |
| 64 | | GENERIC_ISO | SMC_TDI | 47 48 49 |
| 65 | | GENERIC_ISO | SMC_TDO | 47 48 49 |
| 66 | | PM | SMC_THRMTRIP | 47 48 |
| 67 | | GENERIC_ISO | SMC_TMS | 47 48 49 |
| 68 | | GENERIC_ISO | SMC_TO_BLC_RX_L | 48 |
| 69 | | GENERIC_ISO | SMC_TO_BLC_TX_L | 48 |
| 70 | | GENERIC_ISO | SMC_TX_L | 47 48 49 |
| 71 | | PM | SMC_WAKE_L | 47 |
| 72 | | GENERIC_ISO | SMC_WAKE_SCI_L | 15 21 47 |
| 73 | CLK_XTAL | XTAL | SMC_XTAL | 47 48 |
| 74 | CLK_XTAL | XTAL | SMC_XTAL_R | 48 |

## SML_*

| | Physical | Spacing | Netname | |
|---|---|---|---|---|
| 75 | SMB_PHY | SMB | SML_PCH_0_CLK | 18 50 |
| 76 | SMB_PHY | SMB | SML_PCH_0_DATA | 18 50 |
| 77 | SMB_PHY | SMB | SML_PCH_1_CLK | 18 50 |
| 78 | SMB_PHY | SMB | SML_PCH_1_DATA | 18 50 |

## SPI_*

| | Spacing | Netname | |
|---|---|---|---|
| 79 | GENERIC_ISO | SPI_DESCRIPTOR_OVERRIDE_L | 15 47 |

## SSD_*

| | Spacing | Netname | |
|---|---|---|---|
| 80 | GENERIC_ISO | SSD_CLKREQ_L | 15 18 |

## SYS_*

| | Spacing | Netname | |
|---|---|---|---|
| 81 | PM | SYS_PWROK_R | 65 |

## TBT_*

| | Physical | Spacing | Voltage | Netname | |
|---|---|---|---|---|---|
| 82 | | GENERIC_ISO | 3.3V | TBT_A_BIAS | 77 |
| 83 | TBT_GEN_55S | TBT_GEN | | TBT_A_CONFIG1_RC | 77 |
| 84 | | PM | | TBT_A_HV_EN | 36 77 |
| 85 | | GENERIC_ISO | 3.3V | TBT_B_BIAS | 79 |
| 86 | TBT_GEN_55S | TBT_GEN | | TBT_B_CONFIG1_RC | 79 |
| 87 | | PM | | TBT_B_HV_EN | 36 79 |
| 88 | | GENERIC_ISO | | TBT_CLKREQ_ISOL_L | 38 |
| 89 | | GENERIC_ISO | | TBT_CLKREQ_L | 15 38 |
| 90 | | GENERIC_ISO | | TBT_DDC_XBAR_EN_L | 36 76 |
| 91 | | GENERIC_ISO | | TBT_EN_CIO_PWR | 38 |
| 92 | | PM | | TBT_EN_CIO_PWR_L | 36 38 |
| 93 | | GENERIC_ISO | | TBT_EN_LC_ISOL | 38 |
| 94 | | GENERIC_ISO | | TBT_EN_LC_PWR | 36 38 |
| 95 | | GENERIC_ISO | | TBT_PCH_CLKREQ_L | 15 21 |
| 96 | | PM | | TBT_PWR_EN | 15 26 36 |
| 97 | | PM | | TBT_PWR_EN_PCH | 18 26 |
| 98 | | PM | | TBT_PWR_ON_POC_RST_L | 36 38 |
| 99 | | PM | | TBT_PWR_REQ_L | 15 20 36 |
| 100 | | PM | | TBT_S0_EN | 64 |
| 101 | | PM | | TBT_SW_RESET_L | 21 38 |

## TSNS_*

| | Electrical | Physical | Spacing | Netname | |
|---|---|---|---|---|---|
| 102 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_1_1_N | 53 |
| 103 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_1_1_P | 53 |
| 104 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_1_2_N | 53 |
| 105 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_1_2_P | 53 |
| 106 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_1_3_N | 53 |
| 107 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_1_3_P | 53 |
| 108 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_1_N | 53 |
| 109 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_1_P | 53 |
| 110 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_2_N | 53 |
| 111 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_2_P | 53 |
| 112 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_3_N | 53 |
| 113 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_3_P | 53 |
| 114 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_4_N | 53 |
| 115 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_4_P | 53 |
| 116 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_5_N | 53 |
| 117 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_5_P | 53 |
| 118 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_6_N | 53 |
| 119 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_6_P | 53 |
| 120 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_7_N | 53 |
| 121 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_2_7_P | 53 |
| 122 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_ACDC_N | 6 53 |
| 123 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_ACDC_P | 6 53 |
| 124 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_SKIN_N | 53 |
| 125 | SNS_TEMP | SNS_DIFF_PHY | SENSE | TSNS_SKIN_P | 53 |

## UVP_*

| | Spacing | Netname | |
|---|---|---|---|
| 126 | PM | UVP_IN_1 | 82 |
| 127 | PM | UVP_IN_1_REF | 82 |
| 128 | PM | UVP_IN_2 | 82 |
| 129 | PM | UVP_IN_3 | 82 |
| 130 | PM | UVP_IN_4 | 82 |
| 131 | PM | UVP_REF | 82 |

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# AUTO-CONSTRAINTS PG 7

## VREFMRGN_*

| Spacing | Netname | |
|---|---|---|
| GENERIC_ISO | VREFMRGN_CA_SODIMMA_EN | 34 |
| GENERIC_ISO | VREFMRGN_CA_SODIMMB_EN | 34 |

## VTTCLAMP_*

| Spacing | Netname | |
|---|---|---|
| GENERIC_ISO | VTTCLAMP_EN | 28 |
| GENERIC_ISO | VTTCLAMP_L | 28 |

## WOL_*

| Spacing | Netname | |
|---|---|---|
| GENERIC_ISO | WOL_EN | 15 21 40 |

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