1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
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J41 MLB SCHEMATIC 6.6.0
DVT
4/09/13

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45	64	Audio: Speaker Amp	J43_MLB	09/04/2012
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50	73	CPU VR12.5 VCC Power Stage	J43_MLB	09/21/2012
51	74	LPDDR3 Supply	J43_MLB	09/17/2012
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53	76	1.05V S0 Power Supply	J43_MLB	09/10/2012
54	77	LCD/KBD Backlight Driver	J43_MLB	09/13/2012
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58	83	Internal DisplayPort Connector	J43_MLB	09/11/2012
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69	115	Thunderbolt Constraints	CHINMAY_J41	09/07/2012
70	116	Camera Constraints	CHINMAY_J41	09/07/2012
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72	118	Project Specific Constraints	J43_MLB	09/13/2012
73	120	Reference	MASTER	MASTER

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9795	1	SCHEM,MLB,J41	SCH	CRITICAL	
820-3435	1	PCBF,MLB,J41	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Apr 9 19:41:45 2013

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS
MLB_MISC	PP5V5_DCIN:NO,TBTHV:P15V,EDP,CAM_XTAL:NO,CAM_WAKE:NO,APCLKRQ:ISOL,TPAD_INTWAKE:SHARED,USB_PWR:S3,SD_ON_MLB,VCORE_FETS
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	DEVEL_BOM,XDP,LPCPLUS
MLB_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,XDP,LPCPLUS,ISNS:PROD
MLB_DEBUG:PROD	BKLT:PROD,LPCPLUS,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,P1V05_ISNS:YES,AIRPORT_ISNS:YES,SSD_ISNS:YES,LCDBKLT_ISNS:YES,P3V3S5_ISNS:YES,3V3S0_ISNS:YES,OTHER_HS_ISNS:YES,CAM_ISNS:YES,CPUDDR_ISNS:YES,PANEL_ISNS:YES
ISNS:PROD	CPU_HS_ISNS:YES,CPUVR_ISNS:YES,DRAM_ISNS:YES,P1V05_ISNS:NO,AIRPORT_ISNS:NO,SSD_ISNS:YES,LCDBKLT_ISNS:NO,P3V3S5_ISNS:NO,3V3S0_ISNS:NO,OTHER_HS_ISNS:NO,CAM_ISNS:NO,CPUDDR_ISNS:NO,PANEL_ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Dale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	200uW Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
128S0394	128S0415		ALL	NEC alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sense R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S1180	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	EEPROM,256KBIT,SPI,5MHZ,1.8V,2X3QFN	U2890	CRITICAL	TBTROM:BLANK
341S3802	1	IC,EEPROM,C/R (V23.4) EVT,J41/J41	U2890	CRITICAL	TBTROM:PROG
338S1159	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9X9,157BGA	U5000	CRITICAL	SMC:BLANK
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH,8X6X0.8	U6100	CRITICAL	BOOTROM_NUM:BLANK
341S3809	1	IC,EFI ROM (V0071) DVT,J41/J43	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4525	1	HSW,SR16M,PRQ,C0,1.3,15W,2+3,1.0,3M,BGA	U0500	CRITICAL	CPU:1.3GHZ
337S4526	1	HSW,SR16L,PRQ,C0,1.4,15W,2+3,1.1,3M,BGA	U0500	CRITICAL	CPU:1.4GHZ
337S4528	1	HSW,SR16H,PRQ,C0,1.7,15W,2+3,1.1,4M,BGA	U0500	CRITICAL	CPU:1.7GHZ
338S1113	1	IC,TBT,CR-4C,B1,PRQ,CIO,288,12X12 FC-CSP	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CAMERA PROCESSOR	U3900	CRITICAL	
607-6811	1	ASSEMBLY,SUBASSY,PCBA,HALL EFFECT,K99	J6955	CRITICAL	J41_MLB
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		
376S0964	2	MOSFET,N-CH,25V,30A,9.6M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S1104	2	MOSFET,N-CH,25V,30A,6.1M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1173	2	MOSFET,N-CH,30V,15.3A,12M,8P 3.3X3.3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1174	2	MOSFET,N-CH,30V,22A,6.0M,8P 3.3X3.3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0681	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0676	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0680	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0678	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0666	4	IC,SDRAM,16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0679	4	IC,SDRAM,8Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	DRAM_TYPE:MICRON_4GB

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-4118	PCBA,MLB,BEST,HY 4GB,J41:	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_4GB
639-4274	PCBA,MLB,BEST,HY 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:HYNIX_8GB
639-4275	PCBA,MLB,BEST,EL 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_4GB
639-4276	PCBA,MLB,BEST,EL 8GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:ELPIDA_8GB
639-4702	PCBA,MLB,BEST,MI 4GB,J41	MLB_CMNPTS,CPU:1.7GHZ,DDR3:MICRON_4GB
639-4434	PCBA,MLB,BETTER,HY 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_4GB
639-4435	PCBA,MLB,BETTER,HY 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:HYNIX_8GB
639-4436	PCBA,MLB,BETTER,EL 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_4GB
639-4437	PCBA,MLB,BETTER,EL 8GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:ELPIDA_8GB
639-4703	PCBA,MLB,BETTER,MI 4GB,J41	MLB_CMNPTS,CPU:1.3GHZ,DDR3:MICRON_4GB
685-0024	CMN PTS,PCBA,MLB,J41	MLB_COMMON,J41_MLB
985-0017	J41 MLB DEVELOPMENT BOM	MLB_DEVEL:ENG
685-0062	VCORE FET,REN,J41	VCORE_FET:REN
685-0063	VCORE FET,VSHY,J41	VCORE_FET:VSHY

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S3757	1	IC,SMC-A3 SCPL,EXT,V22.12A18,PROTO 1,J41	U5000	CRITICAL	SMC:PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0062	685-0063		ALL	Renesas alt to Vishay
333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
985-0017	1	J41 MLB DEVELOPMENT BOM	DEVEL	CRITICAL	DEVEL_BOM
685-0024	1	CMN PTS,PCBA,MLB,J41	CMNPTS	CRITICAL	MLB_CMNPTS
685-0063	1	VCORE FET,VSHY,J41	VCOREFETS	CRITICAL	VCORE_FETS

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BOM Variants

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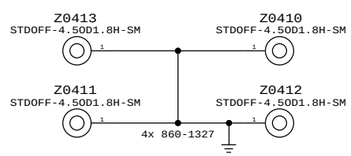
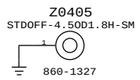
PD Module Parts

806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-5108	1	CAN,TOPSIDE,COVER,ALT,J41/J43	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

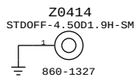
CPU Heat Sink Mounting Bosses



Fan Boss



X21 Boss



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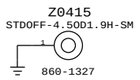
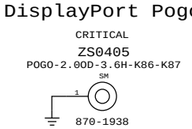
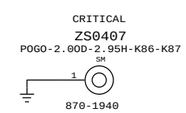


EMI I/O Pogo Pins

DisplayPort Pogo



USB/SD Card Pogo



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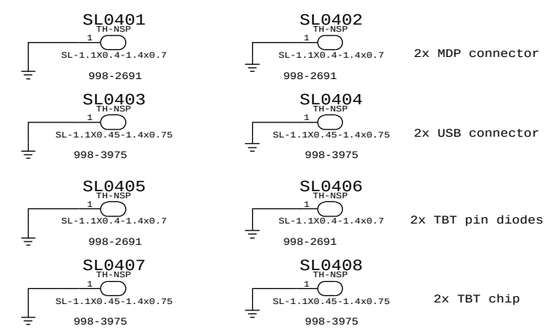

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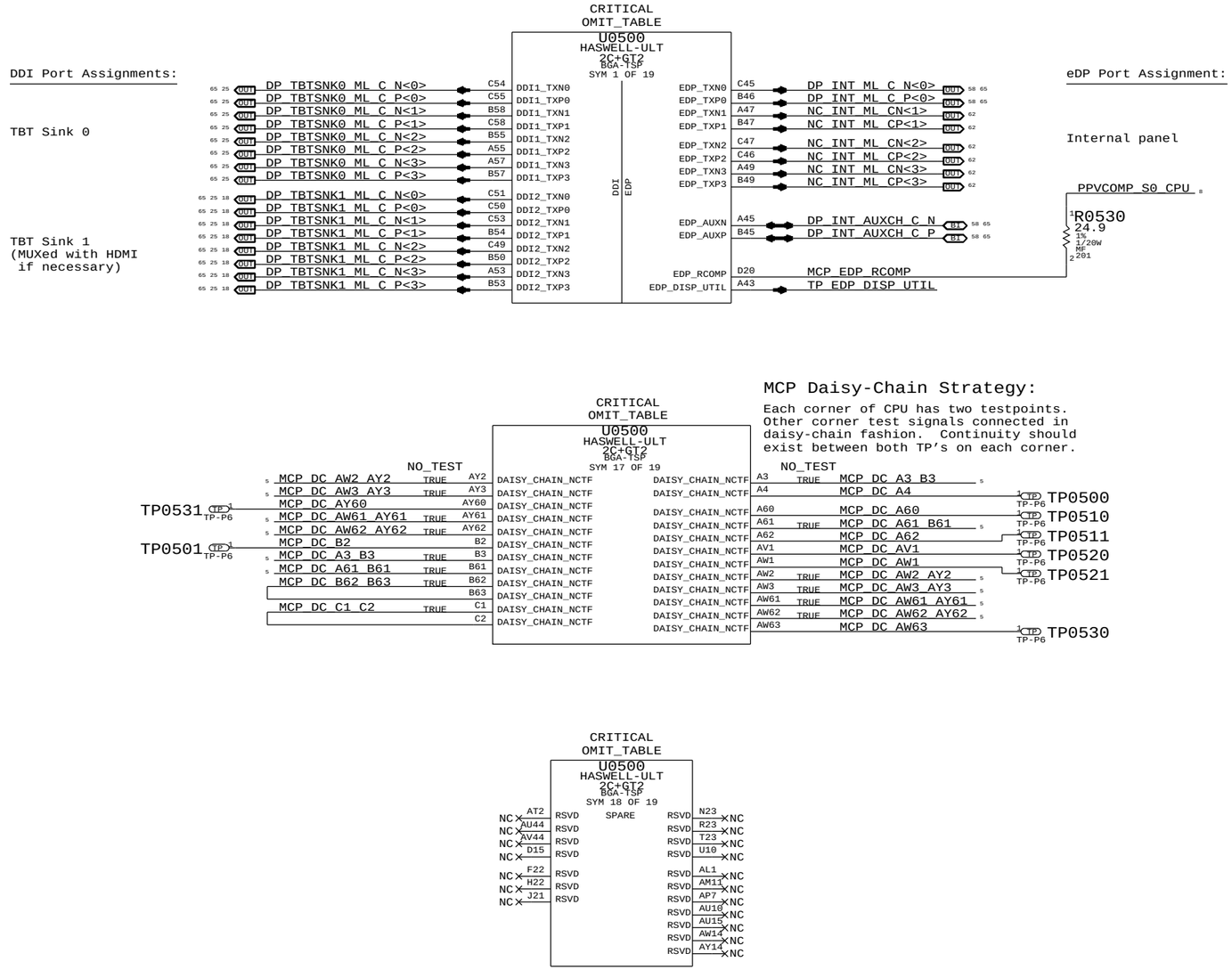

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.

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SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE: CPU GFX/NCTF/RSVD

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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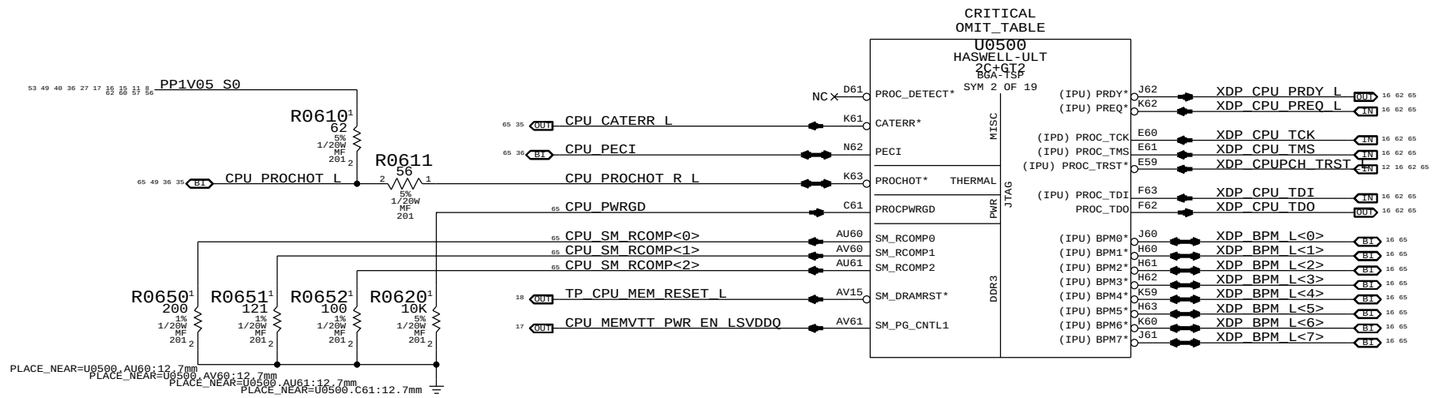
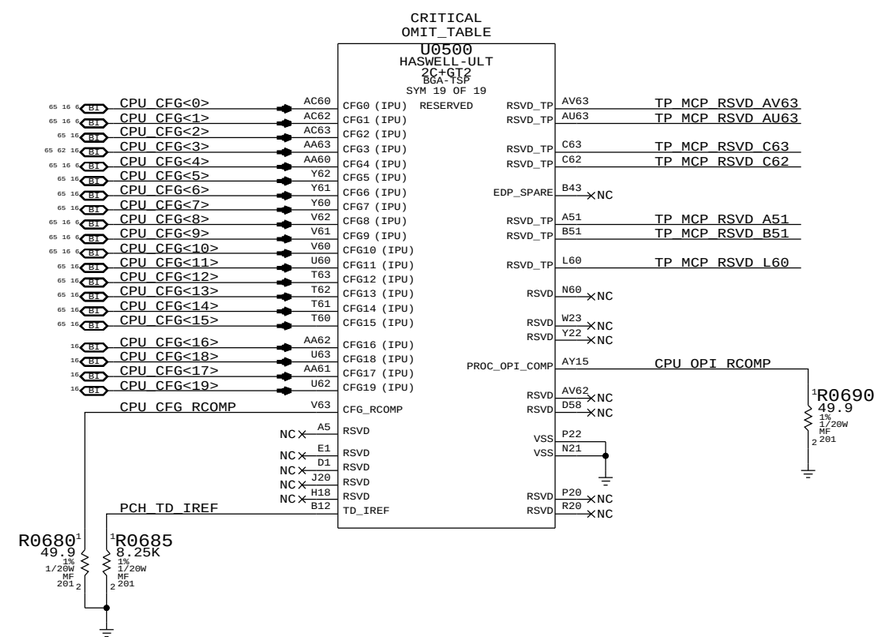
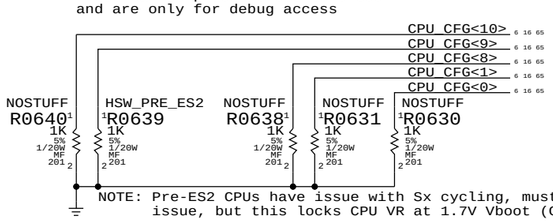


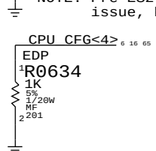


CFG<10>:	SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9>:	NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8>:	ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4>:	eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1>:	PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0>:	RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



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SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
CPU Misc/JTAG/CFG/RSVD

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BRANCH <BRANCH>
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CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
2C+GT2
BGA-TSP
SYM 3 OF 19

MEMORY CHANNEL A

MEM A DQ<0>	AH63	SA_DQ0	SA_CLK0*	AU37	MEM A CLK N<0>
MEM A DQ<1>	AH62	SA_DQ1	SA_CLK0	AV37	MEM A CLK P<0>
MEM A DQ<2>	AK63	SA_DQ2	SA_CLK1*	AW36	MEM A CLK N<1>
MEM A DQ<3>	AK62	SA_DQ3	SA_CLK1	AY36	MEM A CLK P<1>
MEM A DQ<4>	AH61	SA_DQ4			
MEM A DQ<5>	AH60	SA_DQ5	SA_CKE0	AU43	MEM A CKE<0>
MEM A DQ<6>	AK61	SA_DQ6	SA_CKE1	AW43	MEM A CKE<1>
MEM A DQ<7>	AK60	SA_DQ7	SA_CKE2	AY42	MEM A CKE<2>
MEM A DQ<8>	AM63	SA_DQ8	SA_CKE3	AY43	MEM A CKE<3>
MEM A DQ<9>	AM62	SA_DQ9			
MEM A DQ<10>	AP63	SA_DQ10	SA_CS0*	AP33	MEM A CS L<0>
MEM A DQ<11>	AP62	SA_DQ11	SA_CS1*	AR32	MEM A CS L<1>
MEM A DQ<12>	AM61	SA_DQ12			
MEM A DQ<13>	AM60	SA_DQ13	SA_ODT0	AP32	MEM A ODT<0>
MEM A DQ<14>	AP61	SA_DQ14	LPDDR3		
MEM A DQ<15>	AP60	SA_DQ15	CAB3 SA_RAS*	AY34	=MEM A RAS L
MEM A DQ<16>	AP58	SA_DQ16	CAB2 SA_WE*	AW34	=MEM A WE L
MEM A DQ<17>	AR58	SA_DQ17	CAB1 SA_CAS*	AU34	=MEM A CAS L
MEM A DQ<18>	AM57	SA_DQ18			
MEM A DQ<19>	AK57	SA_DQ19	CAB4 SA_BA0	AU35	=MEM A BA<0>
MEM A DQ<20>	AL58	SA_DQ20	CAB6 SA_BA1	AV35	MEM A CAB<6>
MEM A DQ<21>	AK58	SA_DQ21	CAA5 SA_BA2	AY41	=MEM A BA<2>
MEM A DQ<22>	AR57	SA_DQ22			
MEM A DQ<23>	AN57	SA_DQ23	CAB9 SA_MA0	AU36	=MEM A A<0>
MEM A DQ<24>	AP55	SA_DQ24	CAB8 SA_MA1	AY37	=MEM A A<1>
MEM A DQ<25>	AR55	SA_DQ25	CAB5 SA_MA2	AR38	=MEM A A<2>
MEM A DQ<26>	AM54	SA_DQ26	RSVD1 SA_MA3	AP36	TP_LPDDR3_RSVD1
MEM A DQ<27>	AK54	SA_DQ27	RSVD2 SA_MA4	AU39	TP_LPDDR3_RSVD2
MEM A DQ<28>	AL55	SA_DQ28	CAA0 SA_MA5	AR36	=MEM A A<5>
MEM A DQ<29>	AK55	SA_DQ29	CAA2 SA_MA6	AV40	=MEM A A<6>
MEM A DQ<30>	AR54	SA_DQ30	CAA4 SA_MA7	AW39	=MEM A A<7>
MEM A DQ<31>	AN54	SA_DQ31	CAA3 SA_MA8	AY39	=MEM A A<8>
MEM A DQ<32>	AY58	SA_DQ32	CAA1 SA_MA9	AU40	=MEM A A<9>
MEM A DQ<33>	AW58	SA_DQ33	CAB7 SA_MA10	AP35	=MEM A A<10>
MEM A DQ<34>	AY56	SA_DQ34	CAA7 SA_MA11	AW41	=MEM A A<11>
MEM A DQ<35>	AW56	SA_DQ35	CAA6 SA_MA12	AU41	MEM A CAA<6>
MEM A DQ<36>	AV58	SA_DQ36	CAB0 SA_MA13	AR35	=MEM A A<13>
MEM A DQ<37>	AU58	SA_DQ37	CAA9 SA_MA14	AV42	=MEM A A<14>
MEM A DQ<38>	AV56	SA_DQ38	CAA8 SA_MA15	AU42	=MEM A A<15>
MEM A DQ<39>	AU56	SA_DQ39			
MEM A DQ<40>	AY54	SA_DQ40	SA_DQSN0	AJ61	MEM A DQS N<0>
MEM A DQ<41>	AW54	SA_DQ41	SA_DQSN1	AN62	MEM A DQS N<1>
MEM A DQ<42>	AY52	SA_DQ42	SA_DQSN2	AM58	MEM A DQS N<2>
MEM A DQ<43>	AW52	SA_DQ43	SA_DQSN3	AM55	MEM A DQS N<3>
MEM A DQ<44>	AV54	SA_DQ44	SA_DQSN4	AV57	MEM A DQS N<4>
MEM A DQ<45>	AU54	SA_DQ45	SA_DQSN5	AV53	MEM A DQS N<5>
MEM A DQ<46>	AV52	SA_DQ46	SA_DQSN6	AL43	MEM A DQS N<6>
MEM A DQ<47>	AU52	SA_DQ47	SA_DQSN7	AL48	MEM A DQS N<7>
MEM A DQ<48>	AK40	SA_DQ48			
MEM A DQ<49>	AK42	SA_DQ49	SA_DQSP0	AJ62	MEM A DQS P<0>
MEM A DQ<50>	AM43	SA_DQ50	SA_DQSP1	AN61	MEM A DQS P<1>
MEM A DQ<51>	AM45	SA_DQ51	SA_DQSP2	AN58	MEM A DQS P<2>
MEM A DQ<52>	AK45	SA_DQ52	SA_DQSP3	AN55	MEM A DQS P<3>
MEM A DQ<53>	AK43	SA_DQ53	SA_DQSP4	AW57	MEM A DQS P<4>
MEM A DQ<54>	AM40	SA_DQ54	SA_DQSP5	AW53	MEM A DQS P<5>
MEM A DQ<55>	AM42	SA_DQ55	SA_DQSP6	AL42	MEM A DQS P<6>
MEM A DQ<56>	AM46	SA_DQ56	SA_DQSP7	AL49	MEM A DQS P<7>
MEM A DQ<57>	AK46	SA_DQ57			
MEM A DQ<58>	AM49	SA_DQ58			
MEM A DQ<59>	AK49	SA_DQ59			
MEM A DQ<60>	AM48	SA_DQ60	SM_VREF_CA	AP49	CPU_DIMM_VREFCA
MEM A DQ<61>	AK48	SA_DQ61	SM_VREF_DQ0	AR51	CPU_DIMMA_VREFDQ
MEM A DQ<62>	AM51	SA_DQ62	SM_VREF_DQ1	AP51	CPU_DIMMB_VREFDQ
MEM A DQ<63>	AK51	SA_DQ63			

CRITICAL
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MEMORY CHANNEL B

MEM B DQ<0>	AY31	SB_DQ0	SB_CK0*	AM38	MEM B CLK N<0>
MEM B DQ<1>	AW31	SB_DQ1	SB_CK0	AN38	MEM B CLK P<0>
MEM B DQ<2>	AY29	SB_DQ2	SB_CK1*	AK38	MEM B CLK N<1>
MEM B DQ<3>	AW29	SB_DQ3	SB_CK1	AL38	MEM B CLK P<1>
MEM B DQ<4>	AV31	SB_DQ4			
MEM B DQ<5>	AU31	SB_DQ5	SB_CKE0	AY49	MEM B CKE<0>
MEM B DQ<6>	AV29	SB_DQ6	SB_CKE1	AU50	MEM B CKE<1>
MEM B DQ<7>	AU29	SB_DQ7	SB_CKE2	AW49	MEM B CKE<2>
MEM B DQ<8>	AY27	SB_DQ8	SB_CKE3	AV50	MEM B CKE<3>
MEM B DQ<9>	AW27	SB_DQ9			
MEM B DQ<10>	AY25	SB_DQ10	SB_CS0*	AM32	MEM B CS L<0>
MEM B DQ<11>	AW25	SB_DQ11	SB_CS1*	AK32	MEM B CS L<1>
MEM B DQ<12>	AV27	SB_DQ12			
MEM B DQ<13>	AU27	SB_DQ13	SB_ODT0	AL32	MEM B ODT<0>
MEM B DQ<14>	AV25	SB_DQ14	LPDDR3		
MEM B DQ<15>	AU25	SB_DQ15	CAB3 SB_RAS*	AM35	=MEM B RAS L
MEM B DQ<16>	AM29	SB_DQ16	CAB2 SB_WE*	AK35	=MEM B WE L
MEM B DQ<17>	AK29	SB_DQ17	CAB1 SB_CAS*	AM33	=MEM B CAS L
MEM B DQ<18>	AL28	SB_DQ18			
MEM B DQ<19>	AK28	SB_DQ19	CAB4 SB_BA0	AL35	=MEM B BA<0>
MEM B DQ<20>	AR29	SB_DQ20	CAB6 SB_BA1	AM36	MEM B CAB<6>
MEM B DQ<21>	AN29	SB_DQ21	CAA5 SB_BA2	AU49	=MEM B BA<2>
MEM B DQ<22>	AR28	SB_DQ22			
MEM B DQ<23>	AP28	SB_DQ23	CAB9 SB_MA0	AP40	=MEM B A<0>
MEM B DQ<24>	AN26	SB_DQ24	CAB8 SB_MA1	AR40	=MEM B A<1>
MEM B DQ<25>	AR26	SB_DQ25	CAB5 SB_MA2	AP42	=MEM B A<2>
MEM B DQ<26>	AR25	SB_DQ26	RSVD3 SB_MA3	AR42	TP_LPDDR3_RSVD3
MEM B DQ<27>	AP25	SB_DQ27	RSVD4 SB_MA4	AR45	TP_LPDDR3_RSVD4
MEM B DQ<28>	AK26	SB_DQ28	CAA0 SB_MA5	AP45	=MEM B A<5>
MEM B DQ<29>	AM26	SB_DQ29	CAA2 SB_MA6	AW46	=MEM B A<6>
MEM B DQ<30>	AK25	SB_DQ30	CAA4 SB_MA7	AY46	=MEM B A<7>
MEM B DQ<31>	AL25	SB_DQ31	CAA3 SB_MA8	AY47	=MEM B A<8>
MEM B DQ<32>	AY23	SB_DQ32	CAA1 SB_MA9	AU46	=MEM B A<9>
MEM B DQ<33>	AW23	SB_DQ33	CAB7 SB_MA10	AK36	=MEM B A<10>
MEM B DQ<34>	AY21	SB_DQ34	CAA7 SB_MA11	AV47	=MEM B A<11>
MEM B DQ<35>	AW21	SB_DQ35	CAA6 SB_MA12	AU47	MEM B CAA<6>
MEM B DQ<36>	AV23	SB_DQ36	CAB0 SB_MA13	AK33	=MEM B A<13>
MEM B DQ<37>	AU23	SB_DQ37	CAA9 SB_MA14	AR46	=MEM B A<14>
MEM B DQ<38>	AV21	SB_DQ38	CAA8 SB_MA15	AP46	=MEM B A<15>
MEM B DQ<39>	AU21	SB_DQ39			
MEM B DQ<40>	AY19	SB_DQ40	SB_DQSN0	AW30	MEM B DQS N<0>
MEM B DQ<41>	AW19	SB_DQ41	SB_DQSN1	AV26	MEM B DQS N<1>
MEM B DQ<42>	AY17	SB_DQ42	SB_DQSN2	AN28	MEM B DQS N<2>
MEM B DQ<43>	AW17	SB_DQ43	SB_DQSN3	AN25	MEM B DQS N<3>
MEM B DQ<44>	AV19	SB_DQ44	SB_DQSN4	AW22	MEM B DQS N<4>
MEM B DQ<45>	AU19	SB_DQ45	SB_DQSN5	AV18	MEM B DQS N<5>
MEM B DQ<46>	AV17	SB_DQ46	SB_DQSN6	AN21	MEM B DQS N<6>
MEM B DQ<47>	AU17	SB_DQ47	SB_DQSN7	AN18	MEM B DQS N<7>
MEM B DQ<48>	AR21	SB_DQ48			
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MEM B DQ<51>	AM22	SB_DQ51	SB_DQSP2	AM28	MEM B DQS P<2>
MEM B DQ<52>	AN22	SB_DQ52	SB_DQSP3	AM25	MEM B DQS P<3>
MEM B DQ<53>	AP21	SB_DQ53	SB_DQSP4	AV22	MEM B DQS P<4>
MEM B DQ<54>	AK21	SB_DQ54	SB_DQSP5	AW18	MEM B DQS P<5>
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MEM B DQ<56>	AN20	SB_DQ56	SB_DQSP7	AM18	MEM B DQS P<7>
MEM B DQ<57>	AR20	SB_DQ57			
MEM B DQ<58>	AK18	SB_DQ58			
MEM B DQ<59>	AL18	SB_DQ59			
MEM B DQ<60>	AK20	SB_DQ60			
MEM B DQ<61>	AM20	SB_DQ61			
MEM B DQ<62>	AR18	SB_DQ62			
MEM B DQ<63>	AP18	SB_DQ63			

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
CPU DDR3/LPDDR3 Interfaces

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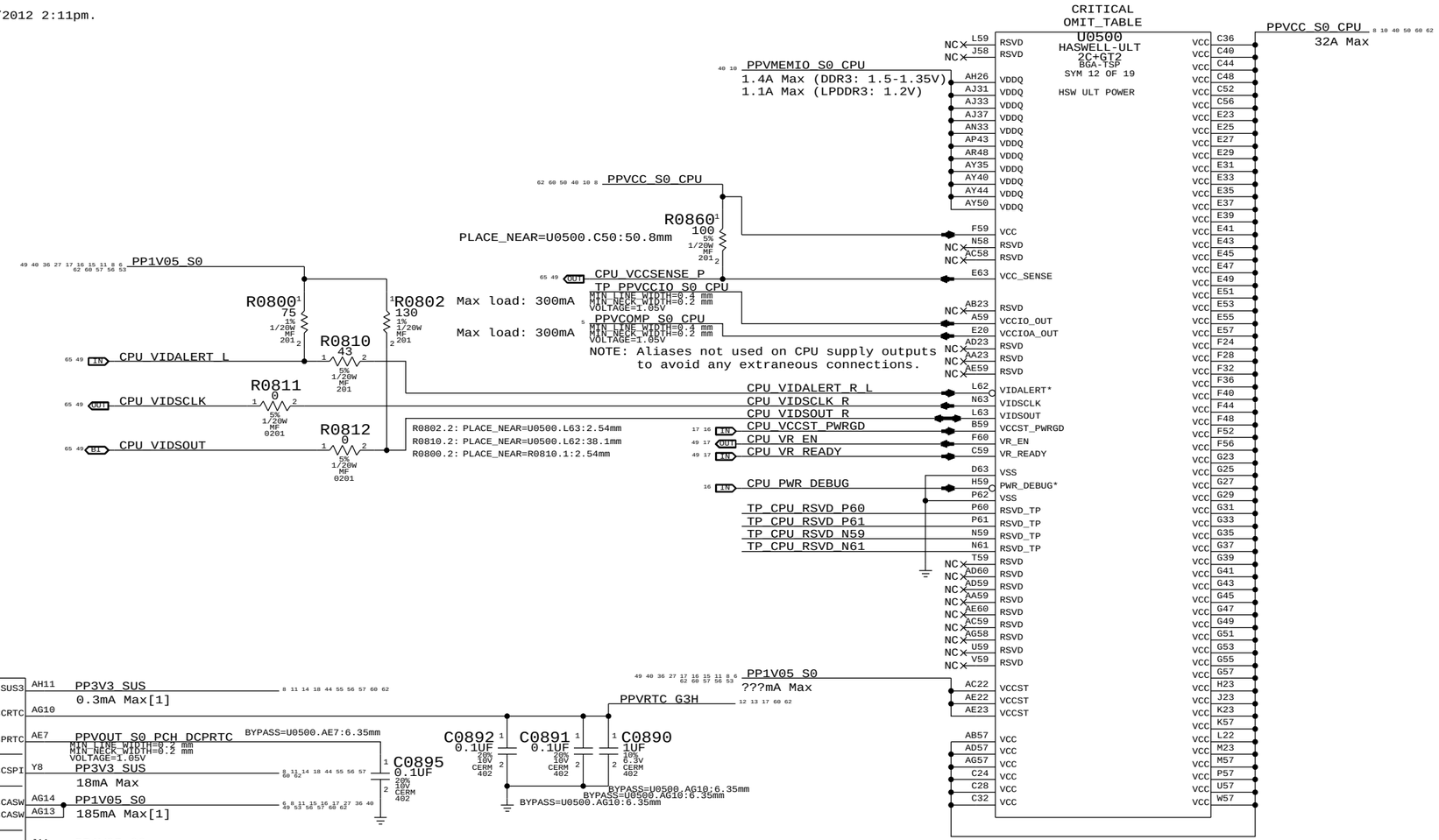
HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



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SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
CPU/PCH POWER

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CRITICAL
OMIT_TABLE

U0500
HASWELL-ULT
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A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN33
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
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AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
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D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS	VSS	V58
G5	VSS	VSS	AH46
G6	VSS	VSS	V23
G8	VSS	VSS	E62
H13	VSS	VSS	AH16

VSS_SENSE

CPU_VCCSENSE_N — OUT — 49 65

R0960
100
5%
1/20W
MF
201

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

62 60 50 40 8 PPVCC_S0_CPU

NO STUFF C1000 10UF 20% 4V X6S 0402
NO STUFF C1001 10UF 20% 4V X6S 0402
NO STUFF C1002 10UF 20% 4V X6S 0402
NO STUFF C1003 10UF 20% 4V X6S 0402
NO STUFF C1004 10UF 20% 4V X6S 0402
NO STUFF C1005 10UF 20% 4V X6S 0402
NO STUFF C1006 10UF 20% 4V X6S 0402
NO STUFF C1007 10UF 20% 4V X6S 0402
NO STUFF C1008 10UF 20% 4V X6S 0402
NO STUFF C1009 10UF 20% 4V X6S 0402
NO STUFF C1010 10UF 20% 4V X6S 0402
NO STUFF C1011 10UF 20% 4V X6S 0402
NO STUFF C1012 10UF 20% 4V X6S 0402
NO STUFF C1013 10UF 20% 4V X6S 0402
NO STUFF C1014 10UF 20% 4V X6S 0402
NO STUFF C105A 10UF 20% 4V X6S 0402
CRITICAL C105B 10UF 20% 4V X6S 0402
CRITICAL C105C 10UF 20% 4V X6S 0402
NO STUFF C105D 10UF 20% 4V X6S 0402
NO STUFF C105E 10UF 20% 4V X6S 0402
CRITICAL C105F 10UF 20% 4V X6S 0402

NO STUFF C1015 10UF 20% 4V X6S 0402
NO STUFF C1016 10UF 20% 4V X6S 0402
NO STUFF C1017 10UF 20% 4V X6S 0402
NO STUFF C1018 10UF 20% 4V X6S 0402
NO STUFF C1019 10UF 20% 4V X6S 0402
NO STUFF C1020 10UF 20% 4V X6S 0402
NO STUFF C1021 10UF 20% 4V X6S 0402
NO STUFF C1030 10UF 20% 4V X6S 0402
NO STUFF C104A 10UF 20% 4V X6S 0402
NO STUFF C104B 10UF 20% 4V X6S 0402
NO STUFF C104C 10UF 20% 4V X6S 0402
CRITICAL C104D 10UF 20% 4V X6S 0402
NO STUFF C104E 10UF 20% 4V X6S 0402
CRITICAL C104F 10UF 20% 4V X6S 0402
CRITICAL C106A 10UF 20% 4V X6S 0402
NO STUFF C106B 10UF 20% 4V X6S 0402
NO STUFF C106C 10UF 20% 4V X6S 0402
NO STUFF C106D 10UF 20% 4V X6S 0402
NO STUFF C106E 10UF 20% 4V X6S 0402

CRITICAL C1070 10UF 20% 4V X6S 0402
CRITICAL C1071 10UF 20% 4V X6S 0402
NO STUFF C1072 10UF 20% 4V X6S 0402
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NO STUFF C1074 10UF 20% 4V X6S 0402
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CRITICAL C1076 10UF 20% 4V X6S 0402
CRITICAL C1077 10UF 20% 4V X6S 0402
NO STUFF C1078 10UF 20% 4V X6S 0402
NO STUFF C1079 10UF 20% 4V X6S 0402
NO STUFF C1080 10UF 20% 4V X6S 0402
NO STUFF C1081 10UF 20% 4V X6S 0402
NO STUFF C1082 10UF 20% 4V X6S 0402
CRITICAL C1083 10UF 20% 4V X6S 0402
CRITICAL C1084 10UF 20% 4V X6S 0402

CRITICAL C1085 10UF 20% 4V X6S 0402
CRITICAL C1086 10UF 20% 4V X6S 0402
CRITICAL C1087 10UF 20% 4V X6S 0402
NO STUFF C1088 10UF 20% 4V X6S 0402
NO STUFF C1089 10UF 20% 4V X6S 0402
NO STUFF C1090 10UF 20% 4V X6S 0402
CRITICAL C1091 10UF 20% 4V X6S 0402
CRITICAL C1092 10UF 20% 4V X6S 0402
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CRITICAL C1097 10UF 20% 4V X6S 0402

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NO STUFF C1063 10UF 20% 4V X6S 0402
NO STUFF C1064 10UF 20% 4V X6S 0402
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NO STUFF C1098 10UF 20% 4V X6S 0402
NO STUFF C1099 10UF 20% 4V X6S 0402
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NO STUFF C109B 10UF 20% 4V X6S 0402
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NO STUFF C109D 10UF 20% 4V X6S 0402
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NO STUFF C109F 10UF 20% 4V X6S 0402
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NO STUFF C108E 10UF 20% 4V X6S 0402
NO STUFF C108F 10UF 20% 4V X6S 0402
NO STUFF C107A 10UF 20% 4V X6S 0402
NO STUFF C107B 10UF 20% 4V X6S 0402

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY-TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

40 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402-LF
C1041 2.2UF 20% 6.3V CERM 402-LF
C1042 2.2UF 20% 6.3V CERM 402-LF
C1043 2.2UF 20% 6.3V CERM 402-LF

C1050 10UF 20% 6.3V CERM-X5R 0402-1
C1051 10UF 20% 6.3V CERM-X5R 0402-1
C1052 10UF 20% 6.3V CERM-X5R 0402-1
C1053 10UF 20% 6.3V CERM-X5R 0402-1
C1054 10UF 20% 6.3V CERM-X5R 0402-1
C1055 10UF 20% 6.3V CERM-X5R 0402-1

C1060 270UF 20% 2V TANT CASE-B2-SM
NO STUFF C1061 270UF 20% 2V TANT CASE-B2-SM

2x Bulk nostuff per Harris Beach v1.0 schematic

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SYNC_MASTER=LABEL_J41 SYNC_DATE=01/11/2013
PAGE TITLE: CPU Decoupling
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REVISION: <E4LABEL>
BRANCH: <BRANCH>
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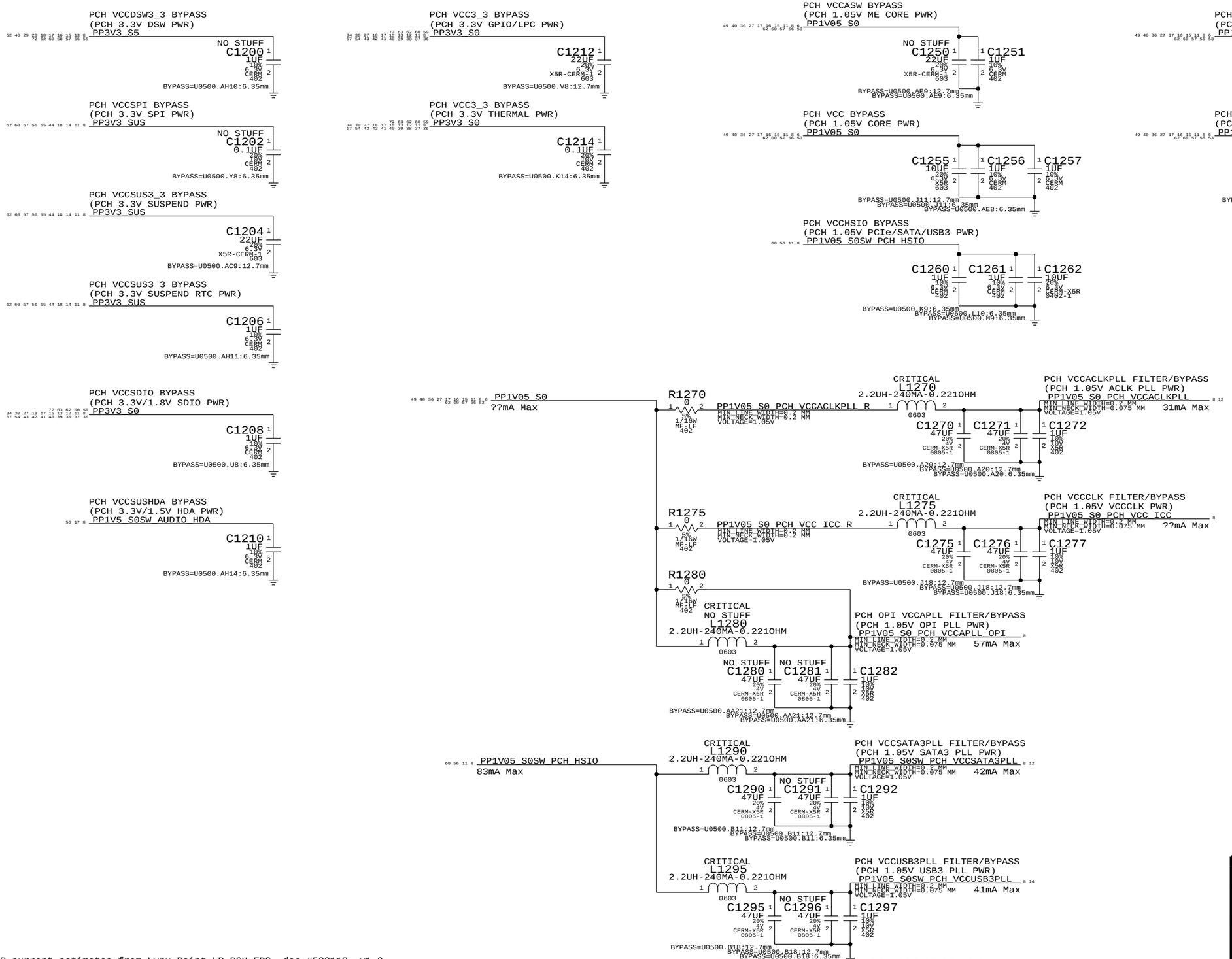

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

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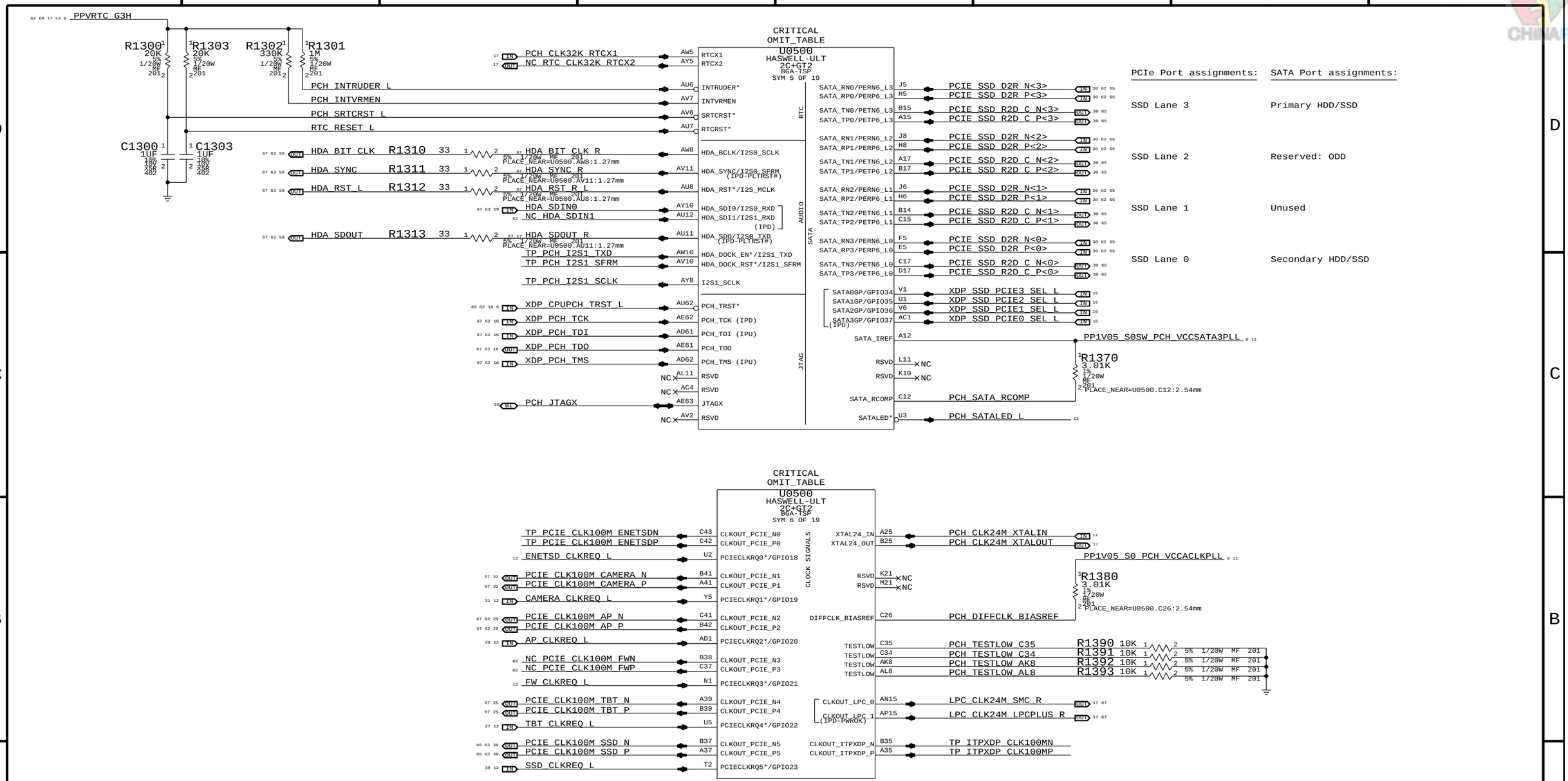

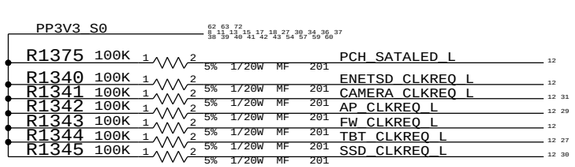

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PAGE TITLE: PCH Audio/JTAG/SATA/CLK

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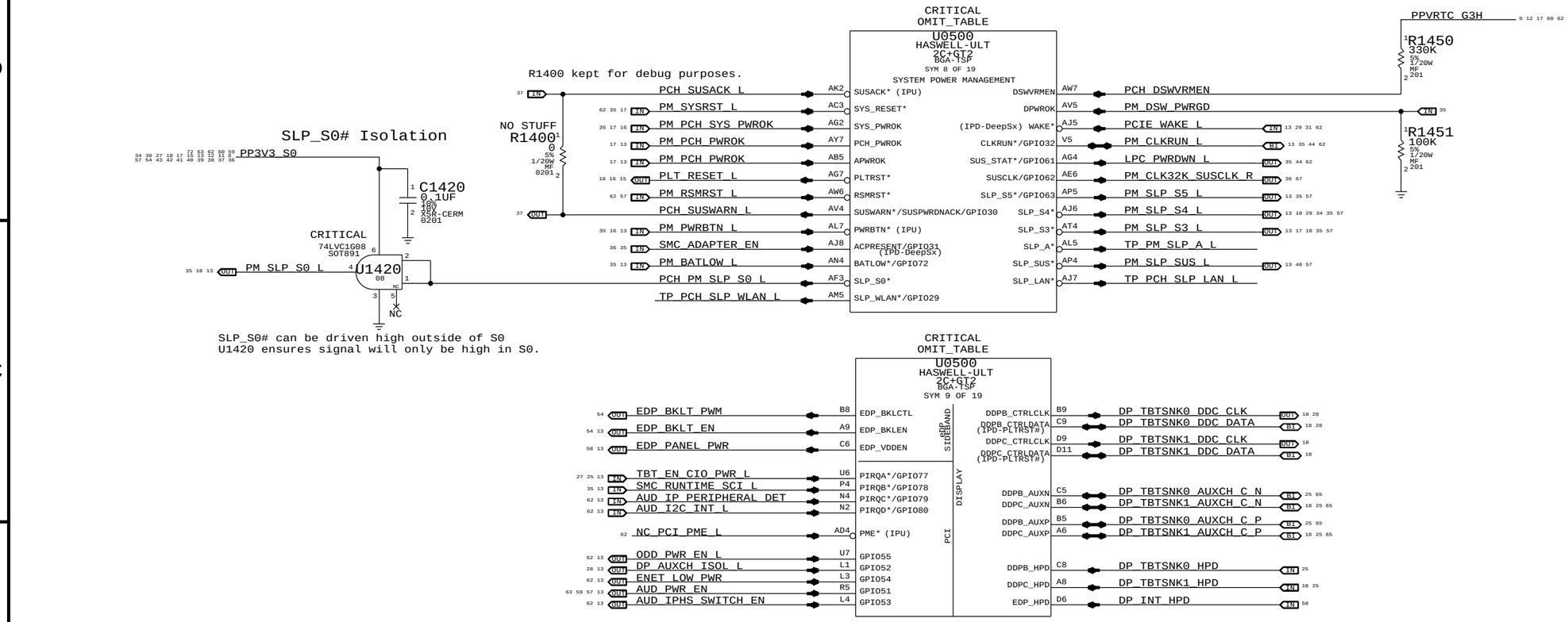

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PCH PM/PCI/GFX

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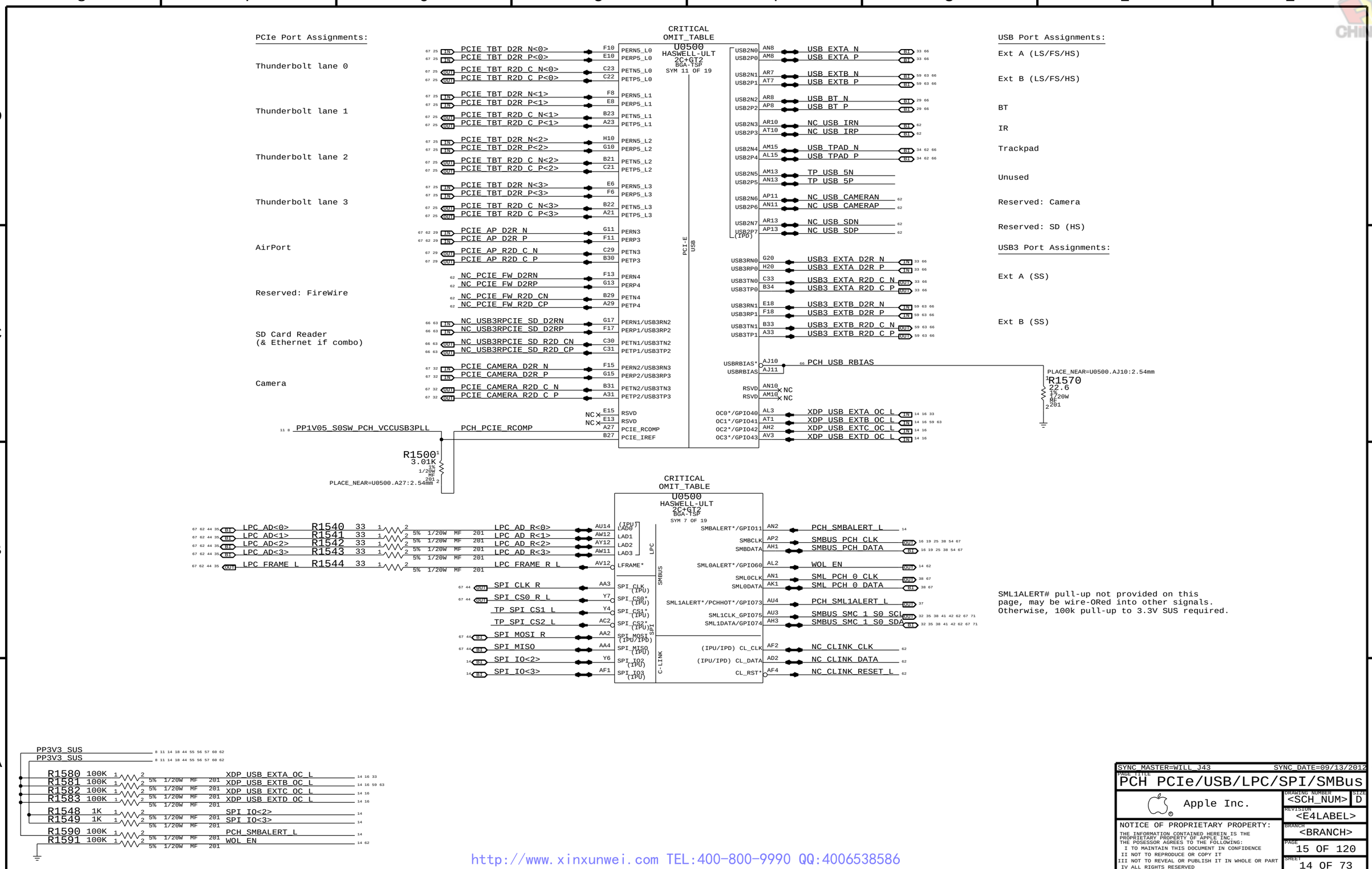

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PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

PP3V3_S0

RAMCFG3:H R1631 100K 5% 1/20W MF 201
RAMCFG2:H R1636 100K 5% 1/20W MF 201
RAMCFG1:H R1635 100K 5% 1/20W MF 201
RAMCFG0:H R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

PLT_RESET_L

R1621 100K 5% 1/20W MF 201

R1639 100K 5% 1/20W MF 201

NO STUFF
R1641 1K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE
U0500
HASWELL-ULT
2C+GT2
BGA-1168
SYM 10 OF 19

Signal	Pin	Net
BMBUSY*/GPIO76	P1	XDP_PCH_GPIO76
GPIO8	AU2	XDP_MLB_RAMCFG0
LAN_PHY_PWR_CTRL/GPIO12	AM7	TBT_GO2SX_BIDIR
GPIO15 (IPD-RSMRST#)	AD6	TP_MEM_VDD_SEL_1V5_L
GPIO16	Y1	XDP_LPCPLUS_GPIO
GPIO17	T3	XDP_PCH_GPIO17
GPIO24	AD5	SD_RESET_L
GPIO27 (IPD-DeepSx)	AN5	SMC_WAKE_SCI_L
GPIO28	AD7	TPAD_SPI_INT_L
GPIO26	AN3	TPAD_USB_IF_EN
GPIO56	AG6	SSD_PWR_EN
GPIO57	AP1	PCH_TBT_PCIE_RESET_L
GPIO58	AL4	HDD_PWR_EN
GPIO59	AT5	XDP_SDCONN_STATE_CHANGE_L
GPIO44	AK4	SD_PWR_EN
GPIO47	AB6	TBT_PWR_EN
GPIO48	U4	XDP_JTAG_ISP_TCK
GPIO49	Y3	XDP_JTAG_ISP_TDI
GPIO50	P3	JTAG_TBT_TMS
HSIOPC/GPIO71	Y2	PCH_HSIO_PWR_EN
GPIO13	AT3	TPAD_SPI_IF_EN
GPIO14	AH4	XDP_MLB_RAMCFG3
GPIO25	AM4	SPIROM_USE_MLB
GPIO45	AG5	CAMERA_PWR_EN_PCH
GPIO46	AG3	FW_PWR_EN
GPIO9	AM3	XDP_MLB_RAMCFG1
GPIO10	AM2	XDP_MLB_RAMCFG2
DEVSLP0*/GPIO33	P2	SSD_DEVSLP
SDIO_POWER_EN/GPIO70	C4	AP_S0IX_WAKE_SEL
DEVSLP1*/GPIO38	L2	SSD_RESET_L
DEVSLP2*/GPIO39	N5	FW_PME_L
SPKR/GPIO81 (IPD-PLTRST#)	V2	PCH_TCO_TIMER_DISABLE
THRMTRIP*	D60	PM_THRMTRIP_L
RCIN*/GPIO82	V4	TBT_CIO_PLUG_EVENT
SERIRQ	T4	LPC_SERIRQ
PCH_OPI_COMP	AW15	PCH_OPI_COMP
RSVD	AF20	NC
RSVD	AB21	NC
GSPI0_CS*/GPIO83	R6	PCH_GSPI0_CS_L
GSPI0_CLK/GPIO84	L6	PCH_GSPI0_CLK
GSPI0_MISO/GPIO85 (IPD)	N6	PCH_GSPI0_MISO
GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	L8	PCH_GSPI0_MOSI
GSPI1_CS*/GPIO87	R7	TPAD_SPI_CS_L
GSPI1_CLK/GPIO88	L5	TPAD_SPI_CLK
GSPI1_MISO/GPIO89 (IPD)	N7	TPAD_SPI_MISO
GSPI_MOSI/GPIO90	K2	TPAD_SPI_MOSI
UART0_RXD/GPIO91	J1	AP_S0IX_WAKE_L
UART0_TXD/GPIO92	K3	HDMITBTMUX_FLAG_L
UART0_RTS*/GPIO93	J2	JTAG_ISP_TDO
UART0_CTS*/GPIO94	G1	AP_RESET_L
UART1_RXD/GPIO0	K4	PCH_UART1_RXD
UART1_TXD/GPIO1	G2	PCH_UART1_TXD
UART1_RST*/GPIO2	J3	PCH_UART1_RTS_L
UART1_CTS*/GPIO3	J4	PCH_UART1_CTS_L
I2C0_SDA/GPIO4	F2	PCH_I2C0_SDA
I2C0_SCL/GPIO5	F3	PCH_I2C0_SCL
I2C1_SDA/GPIO6	G4	PCH_I2C1_SDA
I2C1_SCL/GPIO7	F1	PCH_I2C1_SCL
SDIO_CLK/GPIO64	E3	TBT_POC_RESET_L
SDIO_CMD/GPIO65	F4	BT_PWRRST_L
SDIO_D0/GPIO66 (IPD-PLTRST#)	D3	PCH_STRP_TOPBLK_SWP_L
SDIO_D1/GPIO67	E4	ENET_MEDIA_SENSE
SDIO_D2/GPIO68	C3	LCD_IRQ_L
SDIO_D3/GPIO69	E2	LCD_PSR_EN

CPU/MISC
GPIO
LPIO

PP1V05_S0

R1650 1K 5% 1/20W MF 201

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLACE_NEAR=U0500.AW15:2.54mm
R1655 49.9 1% 1/20W MF 201

PLT_RESET_L
R1671 100K 5% 1/20W MF 201

Pull-up on TBT page

Requires connection to SMC via 1K series R

PP3V3_S0

PP3V3_S5
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
PP3V3_TBTLC

TBTLC for CR, S0 for RR

Resistor	Value	Net
R1610	100K	XDP_PCH_GPIO76
R1614	100K	XDP_LPCPLUS_GPIO
R1615	100K	XDP_PCH_GPIO17
SD_ON_MLB		
R1616	100K	SD_RESET_L
R1617	100K	SMC_WAKE_SCI_L
R1618	100K	TPAD_SPI_INT_L
R1619	100K	TPAD_USB_IF_EN
R1620	100K	SSD_PWR_EN
R1622	100K	HDD_PWR_EN
R1623	100K	XDP_SDCONN_STATE_CHANGE_L
R1624	100K	SD_PWR_EN
R1625	100K	TBT_PWR_EN
R1626	100K	XDP_JTAG_ISP_TCK
R1627	100K	XDP_JTAG_ISP_TDI
R1628	100K	JTAG_TBT_TMS
R1629	100K	PCH_HSIO_PWR_EN
R1630	100K	TPAD_SPI_IF_EN
NO STUFF		
R1632	100K	SPIROM_USE_MLB
R1633	100K	CAMERA_PWR_EN_PCH
R1634	100K	FW_PWR_EN
R1637	100K	SSD_DEVSLP
R1638	100K	AP_S0IX_WAKE_SEL
R1640	100K	FW_PME_L
R1652	10K	LPC_SERIRQ
R1670	100K	JTAG_ISP_TDO
R1691	100K	BT_PWRRST_L
R1693	100K	ENET_MEDIA_SENSE
R1694	100K	LCD_IRQ_L
R1695	100K	LCD_PSR_EN

R1616 should also be stuffed if platform does not use SD card

PP3V3_S0

Net	Resistor	Value
PCH_GSPI0_CS_L	R1660	100K
PCH_GSPI0_CLK	R1661	100K
PCH_GSPI0_MISO	R1662	100K
PCH_GSPI0_MOSI	R1663	100K
TPAD_SPI_CS_L	R1664	47K
TPAD_SPI_CLK	R1665	47K
TPAD_SPI_MISO	R1666	47K
TPAD_SPI_MOSI	R1667	47K
AP_S0IX_WAKE_L	R1668	100K
HDMITBTMUX_FLAG_L	R1669	100K
PCH_UART1_RXD	R1672	100K
PCH_UART1_TXD	R1673	100K
PCH_UART1_RTS_L	R1674	100K
PCH_UART1_CTS_L	R1675	100K
PCH_I2C0_SDA	R1676	100K
PCH_I2C0_SCL	R1677	100K
PCH_I2C1_SDA	R1678	100K
PCH_I2C1_SCL	R1679	100K

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SYNC MASTER=WILL J43 SYNC DATE=01/14/2013

PAGE TITLE
PCH GPIO/MISC/LPIO

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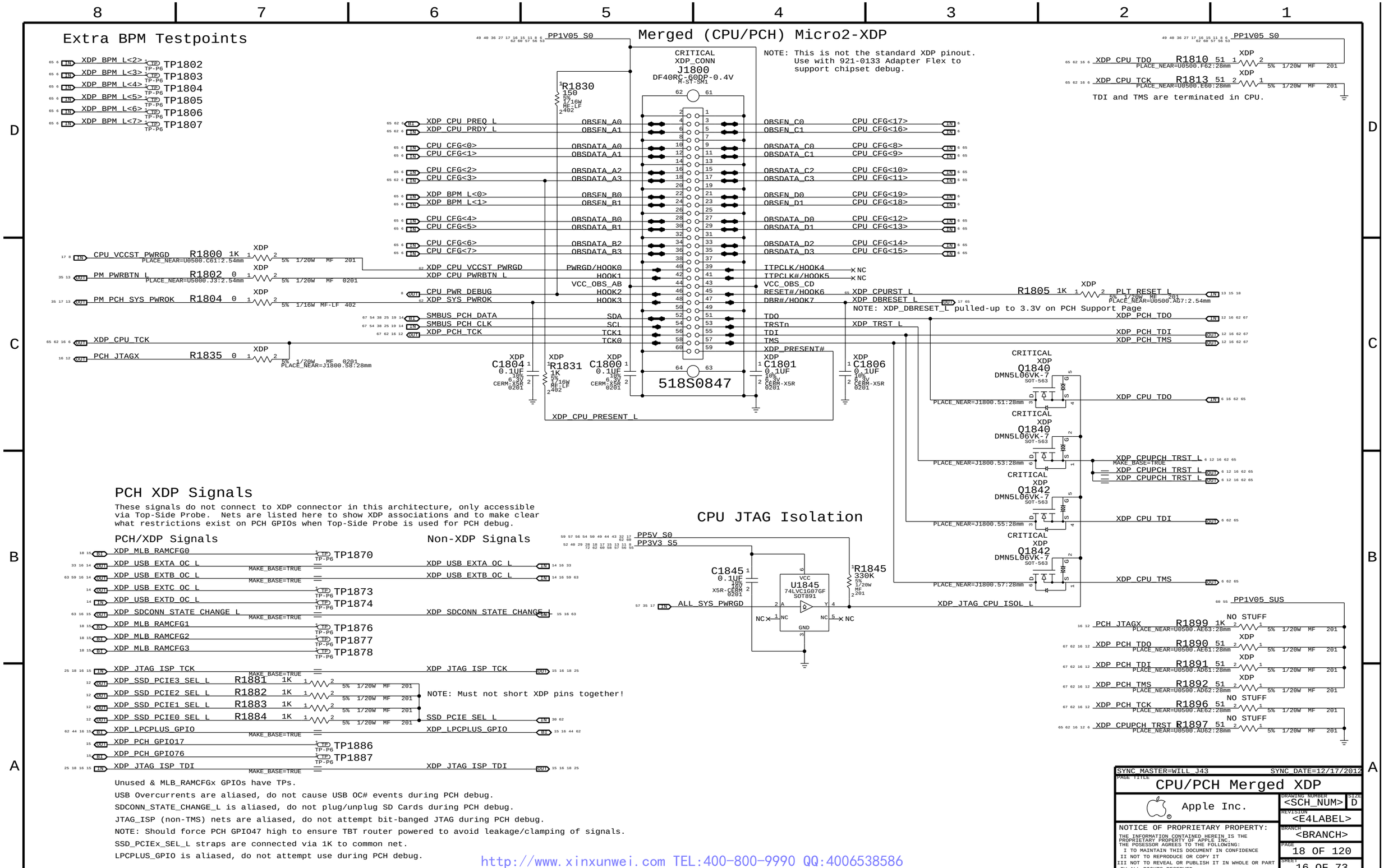

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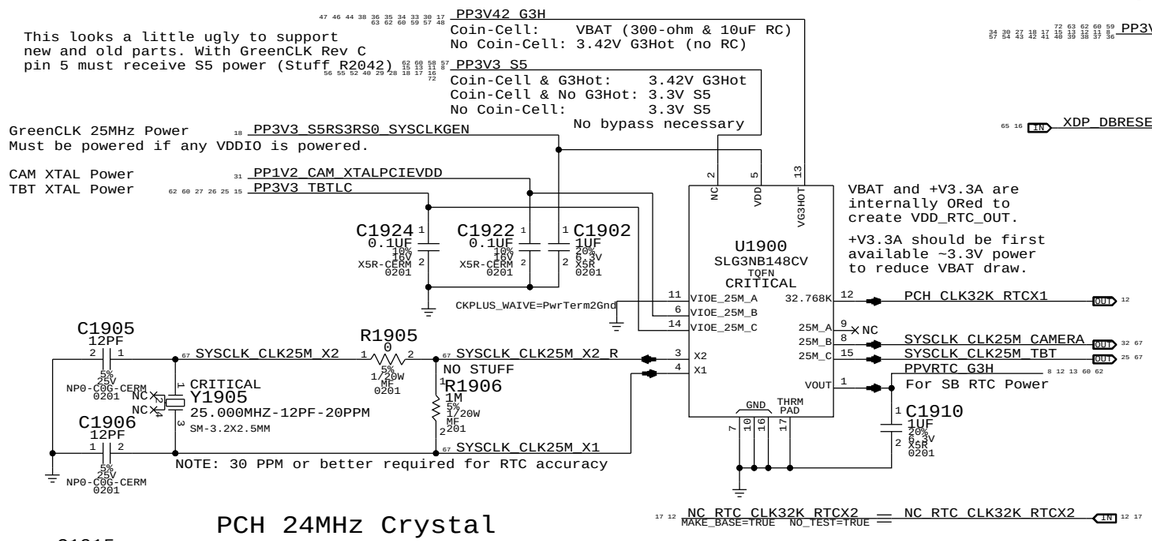
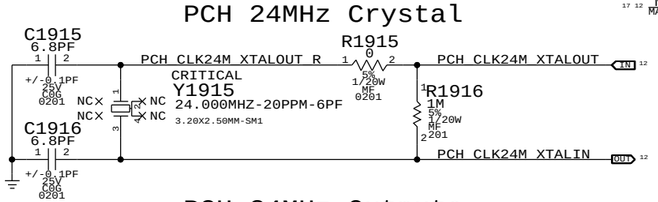
System RTC Power Source & 32kHz / 25MHz Clock Generator

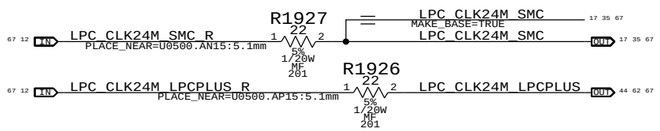
Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal



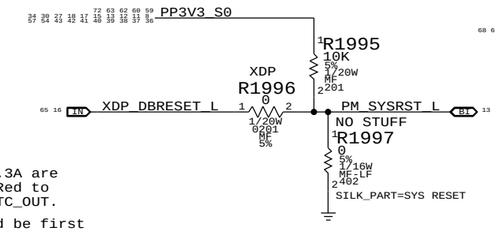
PCH 24MHz Crystal



PCH 24MHz Outputs

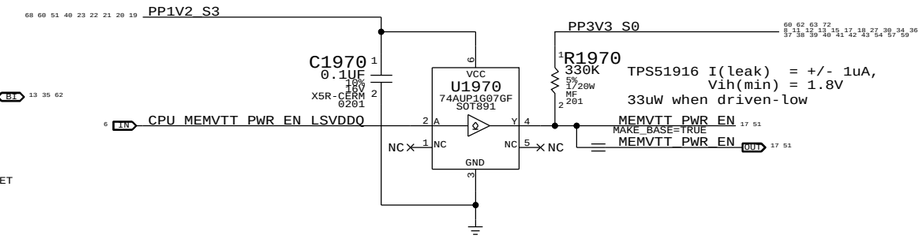


PCH Reset Button

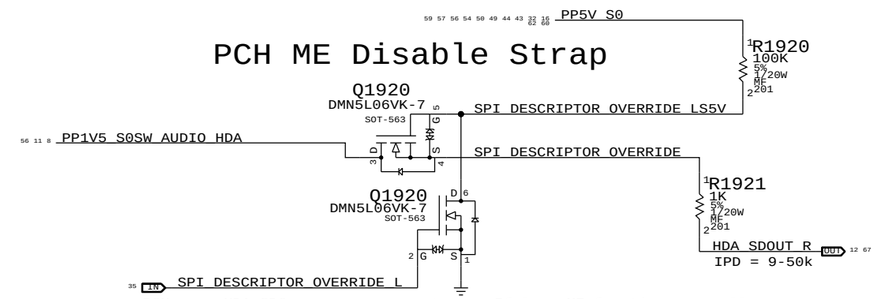


Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

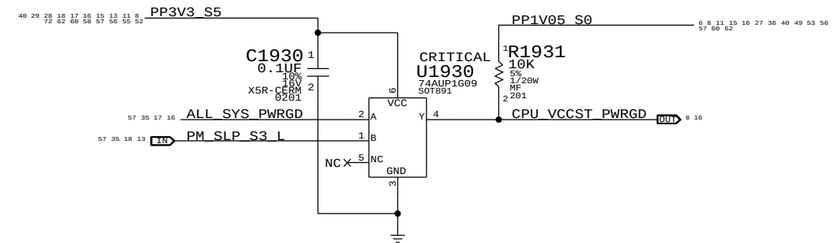


PCH ME Disable Strap

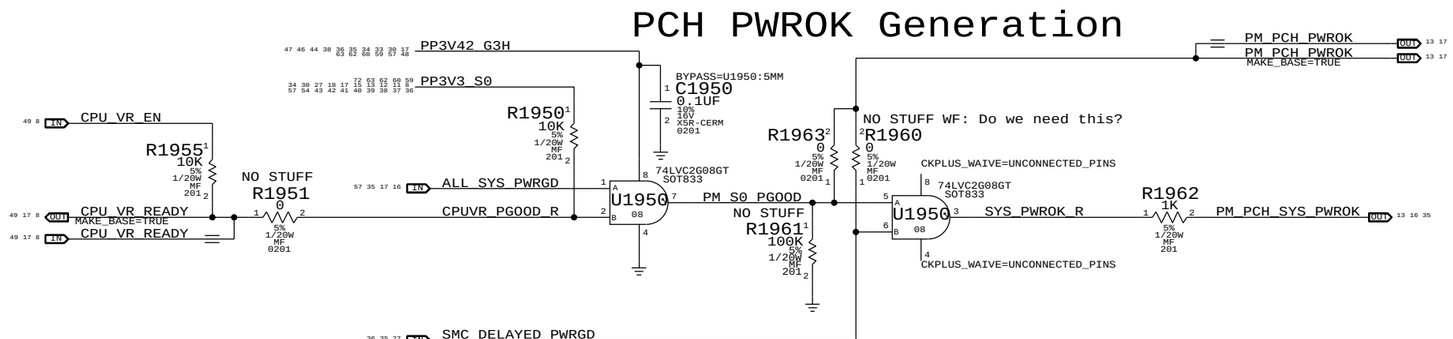


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

VCCST (1.05V S0) PWRGD



PCH PWROK Generation



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SYNC_MASTER=J43_MLB1 SYNC_DATE=01/09/2013

PAGE TITLE: Chipset Support

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Platform Reset Connections

Unbuffered

PLT_RESET_L → R2081 33 (5% 1/20W MF 201) → LPCPLUS_RESET_L
PLT_RESET_L → R2071 0 (5% 1/20W MF 0201) → PCA9557D_RESET_L

PP3V3_S0

Scrub for Layout Optimization

Buffered

CRITICAL
U2071 MC74VHC1G08 SC70-HF
C2071 0.1UF 10% 10V X5R-CERM 0201
R2070 100K 5% 1/20W MF 201

PLT_RST_BUF_L → R2072 0 (5% 1/20W MF 0201) → SMC_LRESET_L
PLT_RST_BUF_L → R2088 0 (5% 1/20W MF 0201) → BKLT_PLT_RST_L
PLT_RST_BUF_L → R2089 0 (5% 1/20W MF 0201) → CAM_PCIE_RESET_L

PCH_TBT_PCIE_RESET_L (MAKE_BASE=TRUE) = PCH_TBT_PCIE_RESET_L

GreenCLK 25MHz Power

PP3V3_S3 → NO STUFF R2040 0 (5% 1/20W MF 0201) → PP3V3_S5RS3RS0_SYSCLKGEN
PP3V3_S5RS3RS0_SYSCLKGEN (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3V, MAKE_BASE=TRUE)

PP3V3_S0 → NO STUFF R2041 0 (5% 1/20W MF 0201)

R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail

R2042 should be stuffed for GreenCLK C

PP3V3_S5 → R2042 0 (5% 1/20W MF 0201)

DDC Pull-Ups

2.2k pull-ups are required by PCH to indicate active display interface.

DP++ spec violation, should remove!

PP3V3_S0
NO STUFF R2020 2.2K (5% 1/20W MF 201)
R2021 2.2K (5% 1/20W MF 201)
NO STUFF R2022 2.2K (5% 1/20W MF 201)
R2023 2.2K (5% 1/20W MF 201)

DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA
DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA

TBTSNK1_DDC is pulled-up just to indicate that DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so DDC_CLK pull-ups are unstuffed.

Thunderbolt Pull-up/downs

Cactus Ridge GO2SX signal pulled-up to SUS rail

PP3V3_SUS
R2013 10K (5% 1/20W MF 201)

TBT_GO2SX_BIDIR (MAKE_BASE TRUE) = TBT_GO2SX_BIDIR

Cactus Ridge PLUG_EVENT is active-high, always driven (pull-down)

TBT_CIO_PLUG_EVENT (TRUE) = TBT_CIO_PLUG_EVENT

Required for unused second TBT port

TBT_B_CIO_SEL
DP_TBTPB_HPD
TBT_B_CONFIG2_RC
TBT_B_CONFIG1_BUF
TBT_B_LSRX

R2015 100K (5% 1/20W MF 201)
R2016 10K (5% 1/20W MF 201)
R2017 10K (5% 1/20W MF 201)
R2018 10K (5% 1/20W MF 201)
R2019 10K (5% 1/20W MF 201)
R2014 10K (5% 1/20W MF 201)

PP3V3_S5
NOSTUFF C2030 0.1UF 10% 10V X5R-CERM 0201 (BYPASS=U2030:3mm)

NOSTUFF CRITICAL
U2030 74LVC1G08 SOT891

PM_SLP_S4_L → U2030 → CAMERA_PWR_EN
CAMERA_PWR_EN_PCH → U2030
NC

R2030 0 (5% 1/20W MF 0201)

Power State Debug LEDs

(For development only)

PP3V3_S5 → R2094 0 (5% 1/10W MF-LF 402) (PLACE_SIDE=BOTTOM) → PP3V3_S5_DBGLED (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=3.3V)

DBGLED R2090 20K	DBGLED R2091 20K	DBGLED R2092 20K	DBGLED R2093 20K	DBGLED R2095 20K	(5% 1/20W MF 201)
DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0I3	DBGLED_S0	
DBGLED D2090	DBGLED D2091	DBGLED D2092	DBGLED D2093	DBGLED D2095	GREEN-56MCD-2MA-2.65V LTQH9G-SM PLACE_SIDE=BOTTOM SILK_PART=S5_ON / SILK_PART=S4BY_ON / SILK_PART=S3_ON / SILK_PART=S0I3_ON / SILK_PART=S0_ON
	DBGLED_S4_D	DBGLED_S3_D	DBGLED_S0I3_D	DBGLED_S0_D	
	DBGLED Q2090 DMN5L06VK-7 SOT-563	DBGLED Q2090 DMN5L06VK-7 SOT-563	DBGLED Q2091 DMN5L06VK-7 SOT-563	DBGLED Q2091 DMN5L06VK-7 SOT-563	

S4_PWR_EN
PM_SLP_S4_L
PM_SLP_S3_L
PM_SLP_S0_L

TBT Aliases

MAKE_BASE TRUE:
DP_TBTSNK0_DDC_CLK = DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA = DP_TBTSNK0_DDC_DATA

MAKE_BASE TRUE:
DP_TBTSNK1_HPD = DP_TBTSNK1_HPD
=DP_TBTSNK1_ML_C_P<3..0> = DP_TBTSNK1_ML_C_P<3..0>
=DP_TBTSNK1_ML_C_N<3..0> = DP_TBTSNK1_ML_C_N<3..0>
DP_TBTSNK1_AUXCH_C_P = DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N = DP_TBTSNK1_AUXCH_C_N
DP_TBTSNK1_DDC_CLK = DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA = DP_TBTSNK1_DDC_DATA

Single-port TBT implementation does not require DDC Crossbar

MAKE_BASE MAKE_BASE TRUE:
JTAG_ISP_TDO = JTAG_ISP_TDO
XDP_JTAG_ISP_TCK = XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDI = XDP_JTAG_ISP_TDI
JTAG_TBT_TMS = JTAG_TBT_TMS

No MAKE_BASE on TCK/TDI as these are provided on XDP page.

RAM Configuration Straps

Pull-downs for chip-down RAM systems

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

RAMCFG3:L	RAMCFG2:L	RAMCFG1:L	RAMCFG0:L
R2050 10K	R2051 10K	R2052 10K	R2053 10K

(5% 1/20W MF 201)

LPDDR3 Alias Support

TP_CPU_MEM_RESET_L = TP_CPU_MEM_RESET_L (MAKE_BASE=TRUE)
TP_MEM_VDD_SEL_1V5_L = TP_MEM_VDD_SEL_1V5_L (MAKE_BASE=TRUE)
PP0V6_S3_MEM_VREFDQ_A = PP0V6_S3_MEM_VREFDQ_A (MAKE_BASE=TRUE VOLTAGE=0.6V)
PP0V6_S3_MEM_VREFCA_A = PP0V6_S3_MEM_VREFCA_A (MAKE_BASE=TRUE VOLTAGE=0.6V)
PP0V6_S3_MEM_VREFDQ_B = PP0V6_S3_MEM_VREFDQ_B (MAKE_BASE=TRUE VOLTAGE=0.6V)
PP0V6_S3_MEM_VREFCA_B = PP0V6_S3_MEM_VREFCA_B (MAKE_BASE=TRUE VOLTAGE=0.6V)

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

CPU_DIMMA_VREFDQ — Q2220 DMN5L06VK-7 SOT-563

CPU_DIMMB_VREFDQ — Q2260 DMN5L06VK-7 SOT-563

CPU_DIMM_VREFCA — Q2220 DMN5L06VK-7 SOT-563; Q2260 DMN5L06VK-7 SOT-563

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN_CPU_EN is low to remove short due to CPU.

CPU MEM VREFDQ A ISOL — R2225 100K 5% 1/20W MF 201 — VREFMRGN_DQ_A_EN_RC — R2201 100K 5% 1/20W MF 201 — C2225 0.1UF 10% 6.3V CERM-X5R 0201 — Q2225 DMN5L06VK-7 SOT-563

CPU MEM VREFDQ B ISOL — R2245 100K 5% 1/20W MF 201 — VREFMRGN_DQ_B_EN_RC — R2202 100K 5% 1/20W MF 201 — C2245 0.1UF 10% 6.3V CERM-X5R 0201 — Q2265 DMN5L06VK-7 SOT-563

CPU MEM VREFCA A ISOL — R2265 100K 5% 1/20W MF 201 — VREFMRGN_CA_A_EN_RC — R2215 100K 5% 1/20W MF 201 — C2265 0.1UF 10% 6.3V CERM-X5R 0201 — Q2225 DMN5L06VK-7 SOT-563

CPU MEM VREFCA B ISOL — R2285 100K 5% 1/20W MF 201 — VREFMRGN_CA_B_EN_RC — R2207 100K 5% 1/20W MF 201 — C2285 0.1UF 10% 6.3V CERM-X5R 0201 — Q2265 DMN5L06VK-7 SOT-563

DDRVREF_DAC EN RC's to avoid drain glitches
May not be necessary due to C22x0

CRITICAL DDRVREF_DAC

Q2225 pin 6: PLACE_NEAR=Q2220.6:2.54mm

Q2265 pin 6: PLACE_NEAR=Q2260.6:2.54mm

R22x6 pin 2:
PLACE_NEAR=Q2225.1:2.54mm
PLACE_NEAR=Q2265.1:2.54mm
PLACE_NEAR=Q2225.4:2.54mm
PLACE_NEAR=Q2265.4:2.54mm

VRef Dividers

Always used, regardless of margining option.

R2223 10 1% 1/20W MF 201	PLACE_NEAR=Q2220.6:2mm	C2220 0.022UF 10% 6.3V X5R-CERM 0201	MEM_VREFDQ_A_RC	R2220 24.9 1% 1/20W MF 201
R2243 10 1% 1/20W MF 201	PLACE_NEAR=Q2260.6:2mm	C2240 0.022UF 10% 6.3V X5R-CERM 0201	MEM_VREFDQ_B_RC	R2240 24.9 1% 1/20W MF 201
R2263 10 1% 1/20W MF 201	PLACE_NEAR=Q2220.3:2mm	C2260 0.022UF 10% 6.3V X5R-CERM 0201	MEM_VREFCA_A_RC	R2260 24.9 1% 1/20W MF 201
R2283 10 1% 1/20W MF 201	PLACE_NEAR=Q2260.3:2mm	C2280 0.022UF 10% 6.3V X5R-CERM 0201	MEM_VREFCA_B_RC	R2280 24.9 1% 1/20W MF 201

R2221 8.2K 1% 1/20W MF 201	PLACE_NEAR=Q2220.6:3mm	PP0V6_S3_MEM_VREFDQ_A	MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm
R2222 8.2K 1% 1/20W MF 201	PLACE_NEAR=Q2221.2:1mm		
R2241 8.2K 1% 1/20W MF 201	PLACE_NEAR=Q2260.6:3mm	PP0V6_S3_MEM_VREFDQ_B	MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm
R2242 8.2K 1% 1/20W MF 201	PLACE_NEAR=Q2241.2:1mm		
R2261 8.2K 1% 1/20W MF 201	PLACE_NEAR=Q2220.3:3mm	PP0V6_S3_MEM_VREFCA_A	MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm
R2262 8.2K 1% 1/20W MF 201	PLACE_NEAR=Q2261.2:1mm		
R2281 8.2K 1% 1/20W MF 201	PLACE_NEAR=Q2260.3:3mm	PP0V6_S3_MEM_VREFCA_B	MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm
R2282 8.2K 1% 1/20W MF 201	PLACE_NEAR=Q2281.2:1mm		

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

PP3V3_S3 — OMIT R2218 SHORT NONE NONE NONE NONE 402 — PP3V3_S3_VREFMRGN_DAC (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V)

DDRVREF_DAC C2200 2.2UF 20% 6.3V CERM 402-LF — DDRVREF_DAC C2201 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC

U2200 DAC5574 MSOP — VDD, GND, SCL, SDA, A0, A1, VOUTA, VOUTB, VOUTC, VOUTD

SMBUS_PCH_CLK, SMBUS_PCH_DATA

Addr=0x98(WR)/0x99(RD)

VREFMRGN_DQ_A, VREFMRGN_DQ_B, VREFMRGN_CA_AB, VREFMRGN_MEMVREG

(All 4 R's) DDRVREF_DAC
R2226 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_A_RDIV
R2246 4.02K 1% 1/20W MF 201 — VREFMRGN_DQ_B_RDIV
R2266 4.02K 1% 1/20W MF 201 — VREFMRGN_CA_A_RDIV
R2286 4.02K 1% 1/20W MF 201 — VREFMRGN_CA_B_RDIV

NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!

DDRVREF_DAC C2202 0.1UF 10% 6.3V CERM-X5R 0201

CRITICAL DDRVREF_DAC

U2201 PCA9557 QFN (OD) — VCC, A0, A1, A2, SCL, SDA, P0, P1, P2, P3, P4, P5, P6, P7, RESET*, THRM PAD, GND

R2200 100K 5% 1/20W MF 201

VREFMRGN_CPU_EN, VREFMRGN_DQ_A_EN, VREFMRGN_DQ_B_EN, VREFMRGN_CA_A_EN, VREFMRGN_CA_B_EN, VREFMRGN_MEMVREG_EN, VREFMRGN_SPARE_EN, NC

Addr=0x30(WR)/0x31(RD)

SMBUS_PCH_CLK, SMBUS_PCH_DATA

RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PCA9557D_RESET_L

PP3V3_S3

DDRVREF_DAC C2205 0.1UF 10% 6.3V CERM-X5R 0201 — CRITICAL DDRVREF_DAC — U2204 MAX4253 UCSP — VREFMRGN_MEMVREG_BUF — DDRVREF_DAC R2214 38.3K 1% 1/20W MF 201 — DDRREG_FB — PLACE_NEAR=R7415.2:1mm

DDRVREF_DAC R2213 100K 5% 1/20W MF 201 — CRITICAL DDRVREF_DAC — U2204 MAX4253 UCSP — VREFMRGN_SPARE_BUF — DDRVREF_DAC R2217 1M 5% 1/20W MF 201

Pins B1 & B4: CKPLUS_WAIVE=unconnected_pins

DDRVREF_DAC R2212 100K 5% 1/20W MF 201

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	LPDDR3 (1.2V)		DDR3L (1.35V)		LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)		0.675V (DAC: 0x34)		1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)		0.337V - 1.013V (+/- 337.5mV)		0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)		+82uA - -82uA (- = sourced)		+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output		6.36mV / step @ output		4.28mV / step @ output	3.53mV / step @ output

SYNC_MASTER=WILL_J43 SYNC_DATE=02/04/2013

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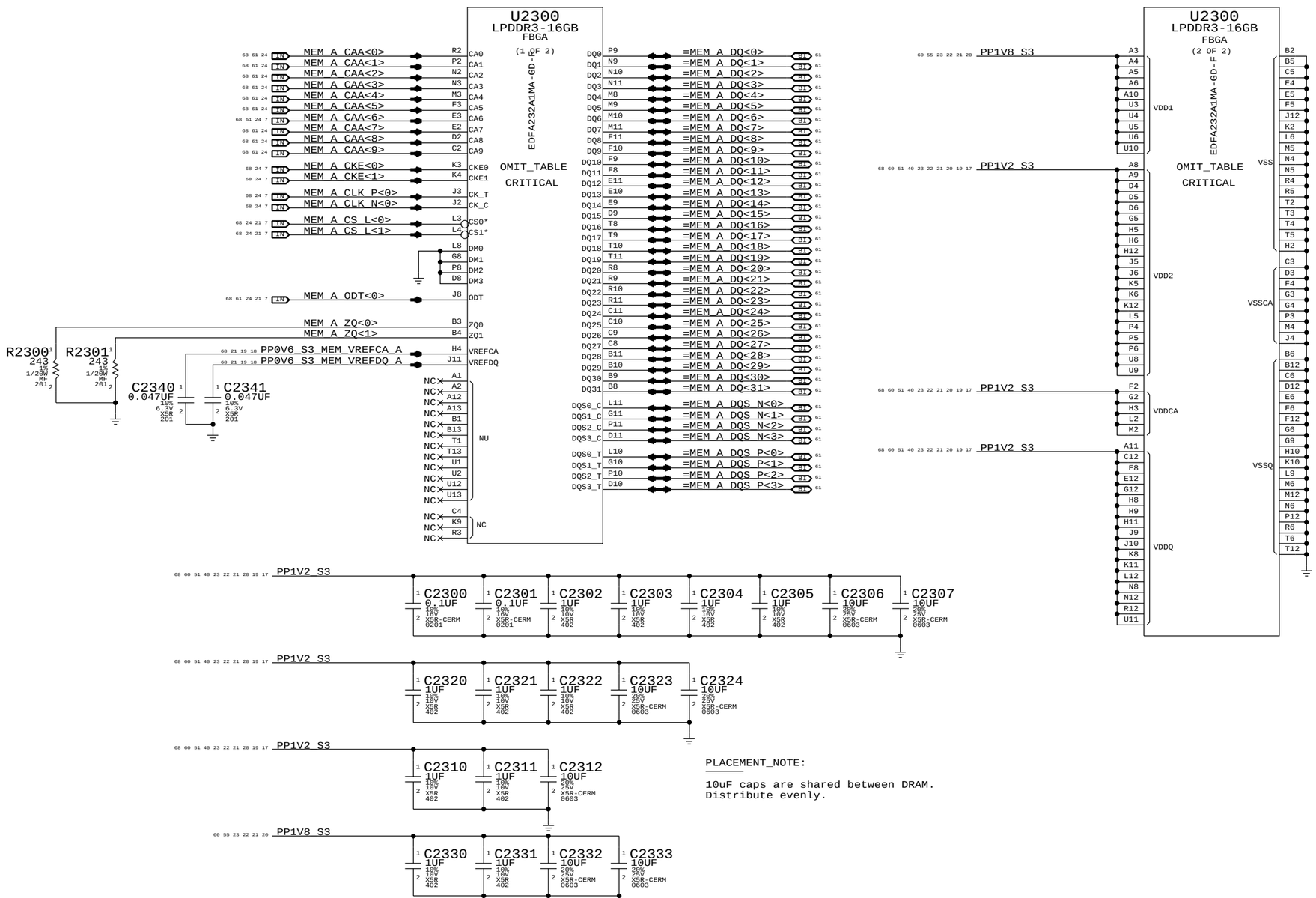
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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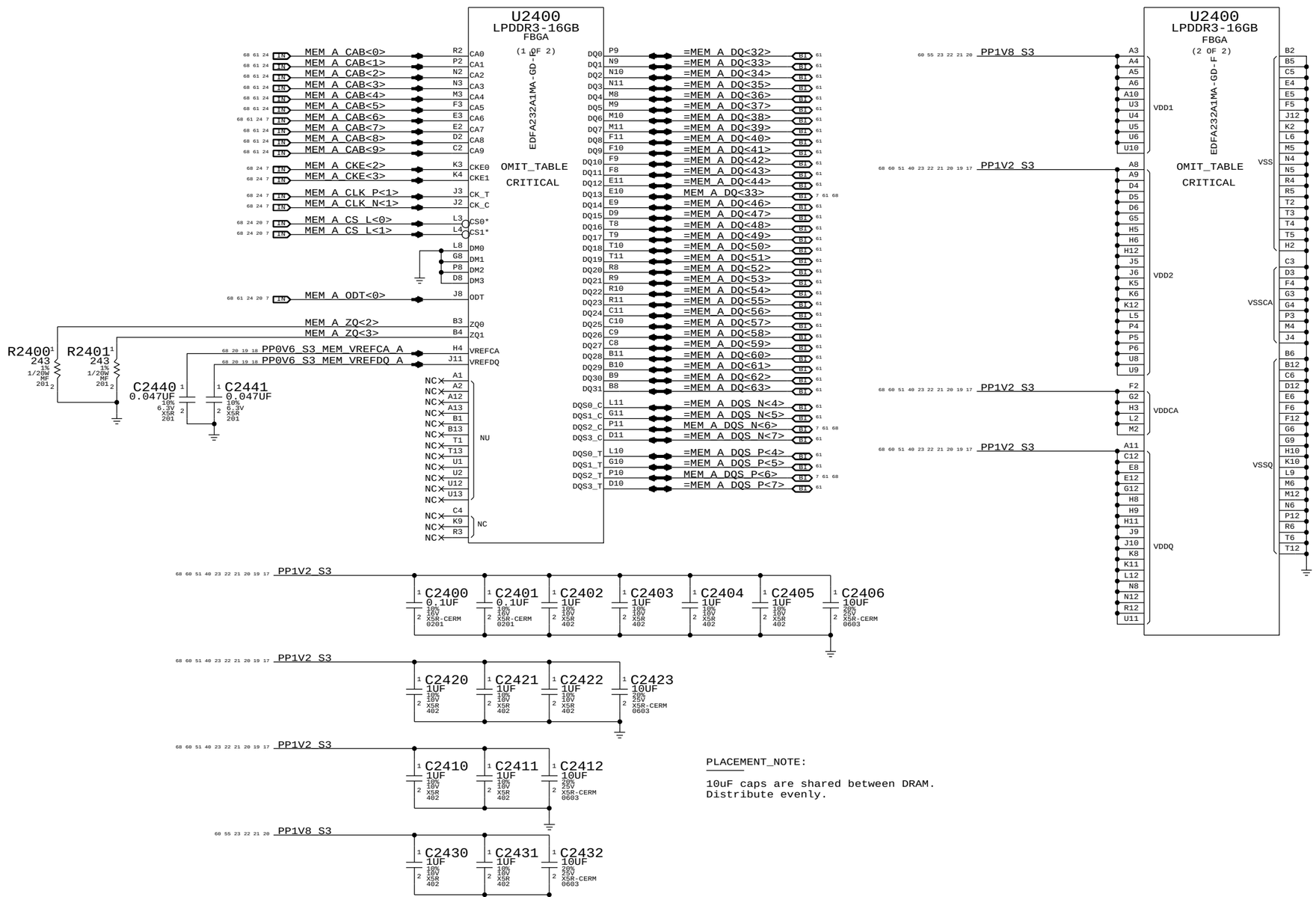
LPDDR3 CHANNEL A (32-63)



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PAGE TITLE
LPDDR3 DRAM Channel A (32-63)

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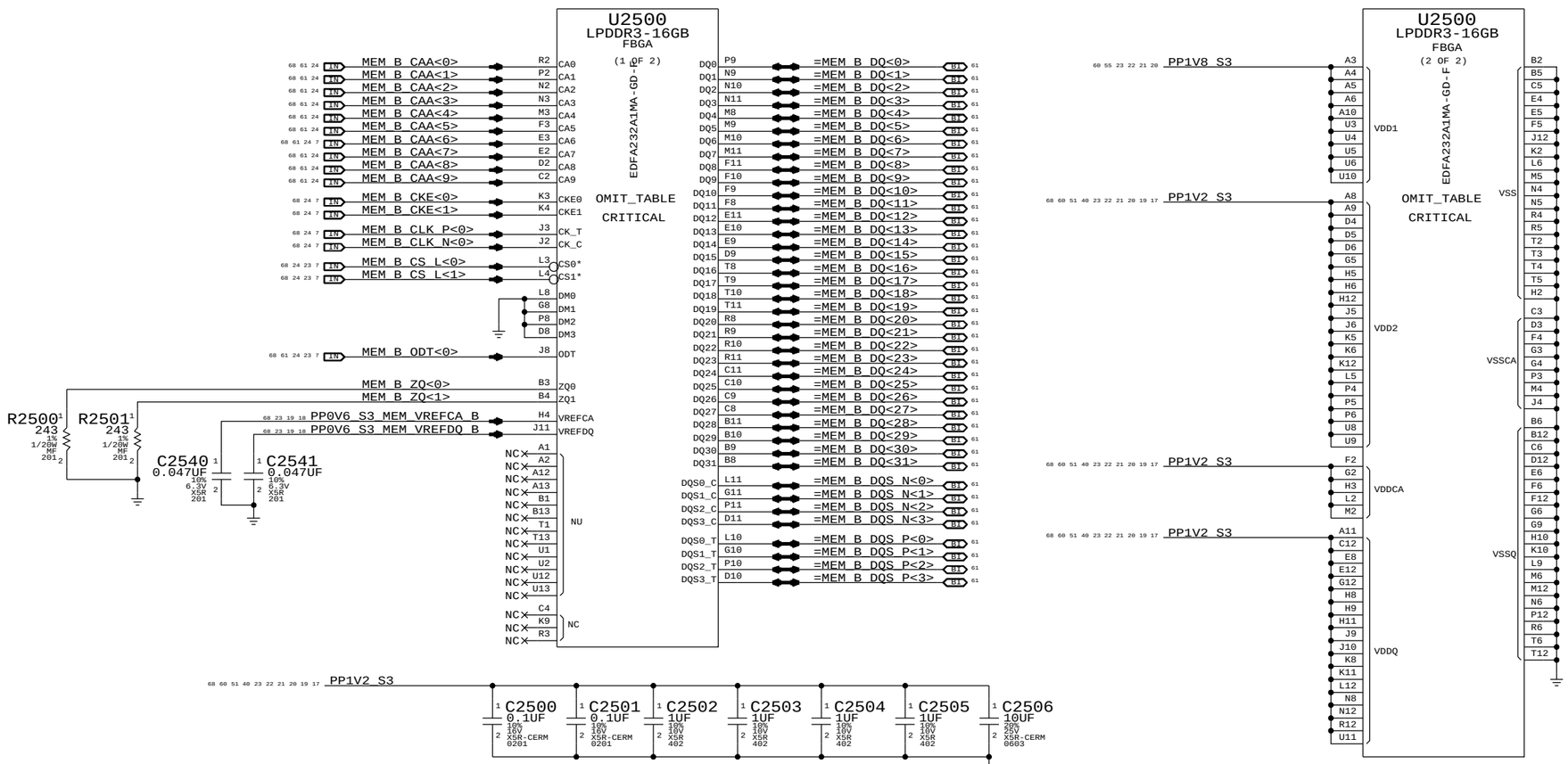
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

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Distribute evenly.

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PAGE TITLE
LPDDR3 DRAM Channel B (0-31)

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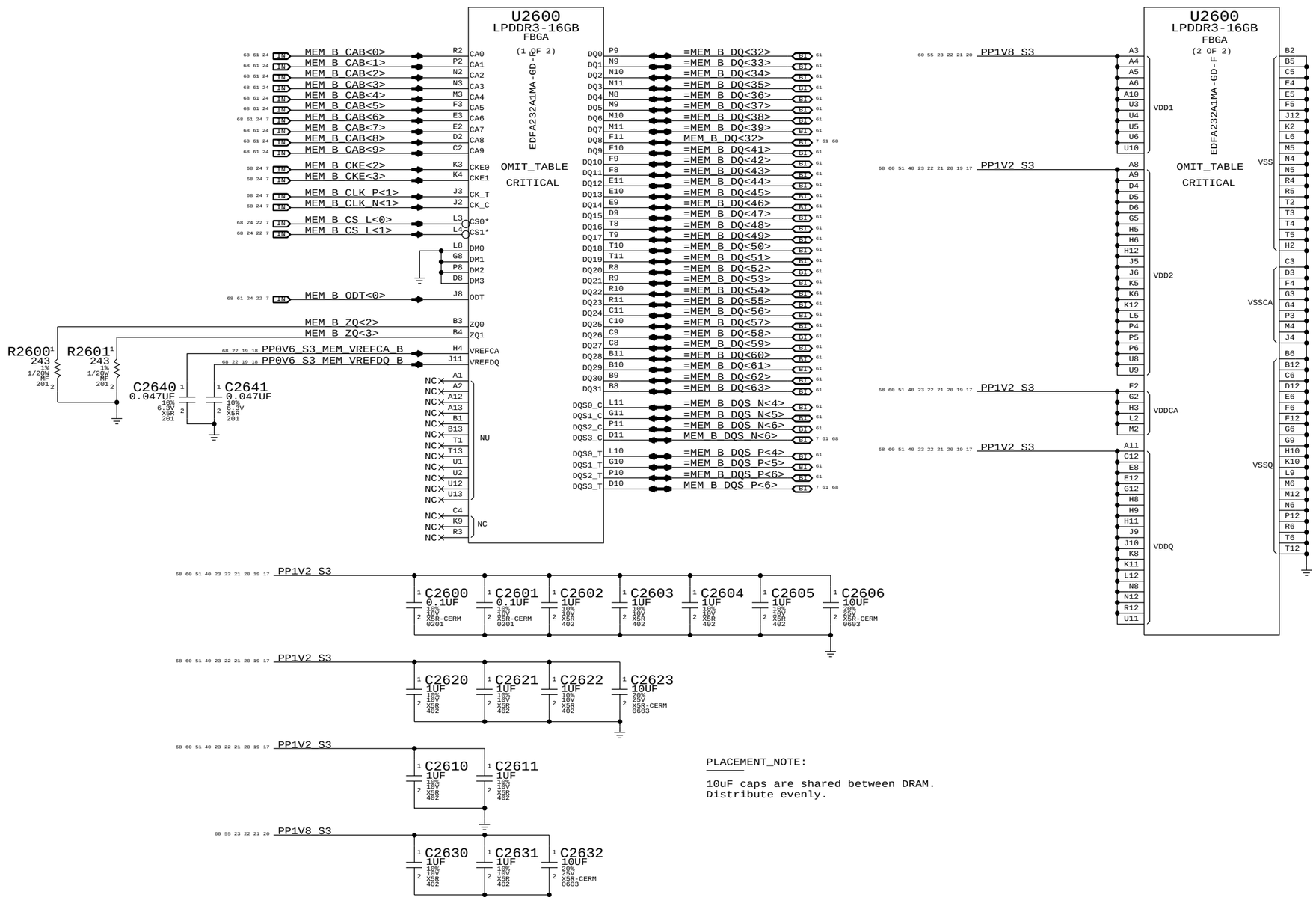
LPDDR3 CHANNEL B (32-63)



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PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

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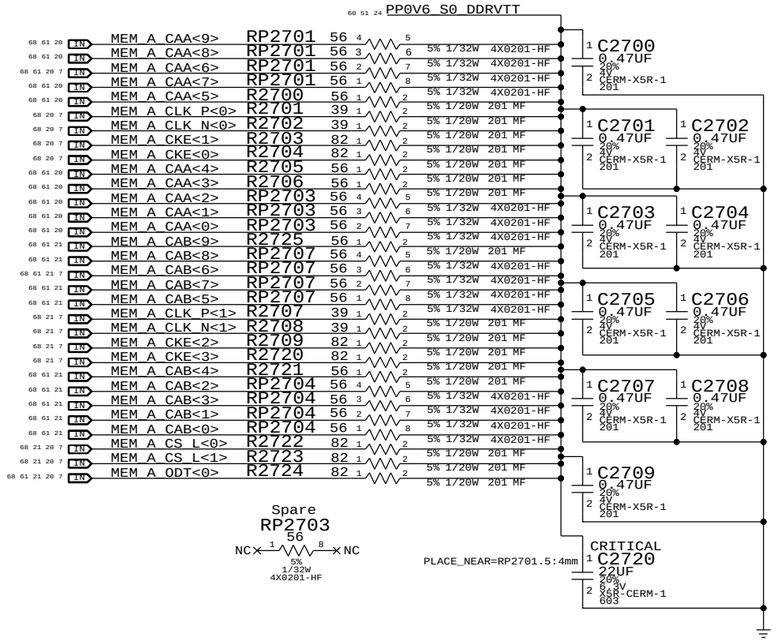
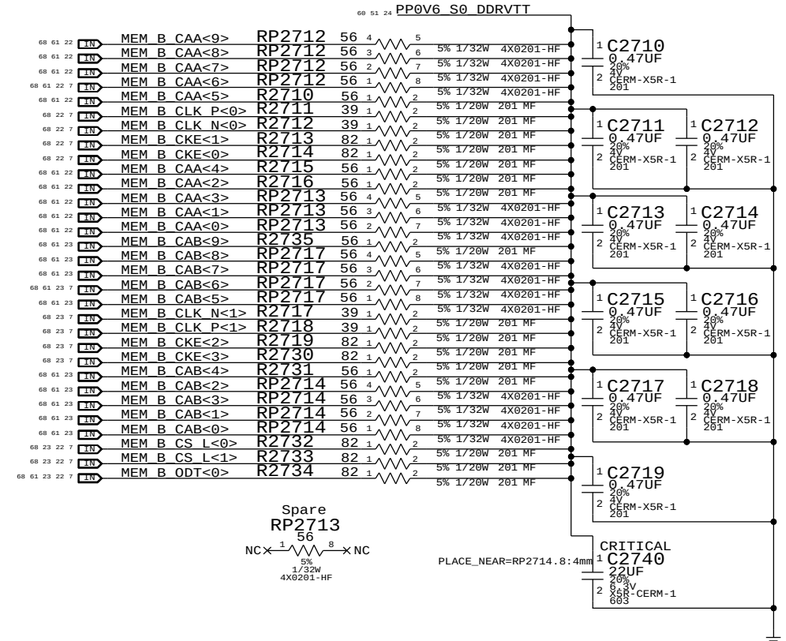
Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC_MASTER=J43_MLB SYNC_DATE=09/21/2012

PAGE TITLE
LPDDR3 DRAM Termination

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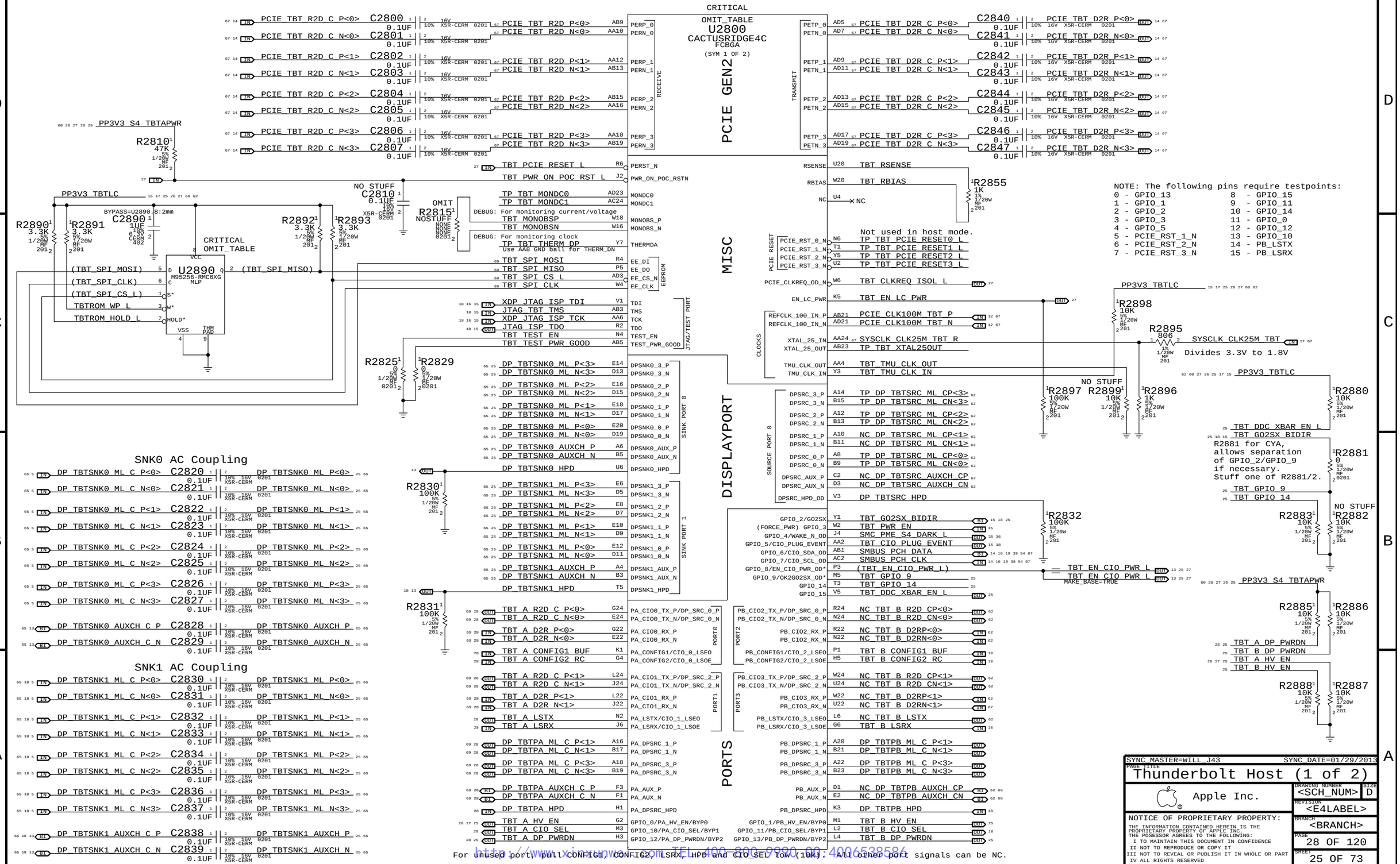

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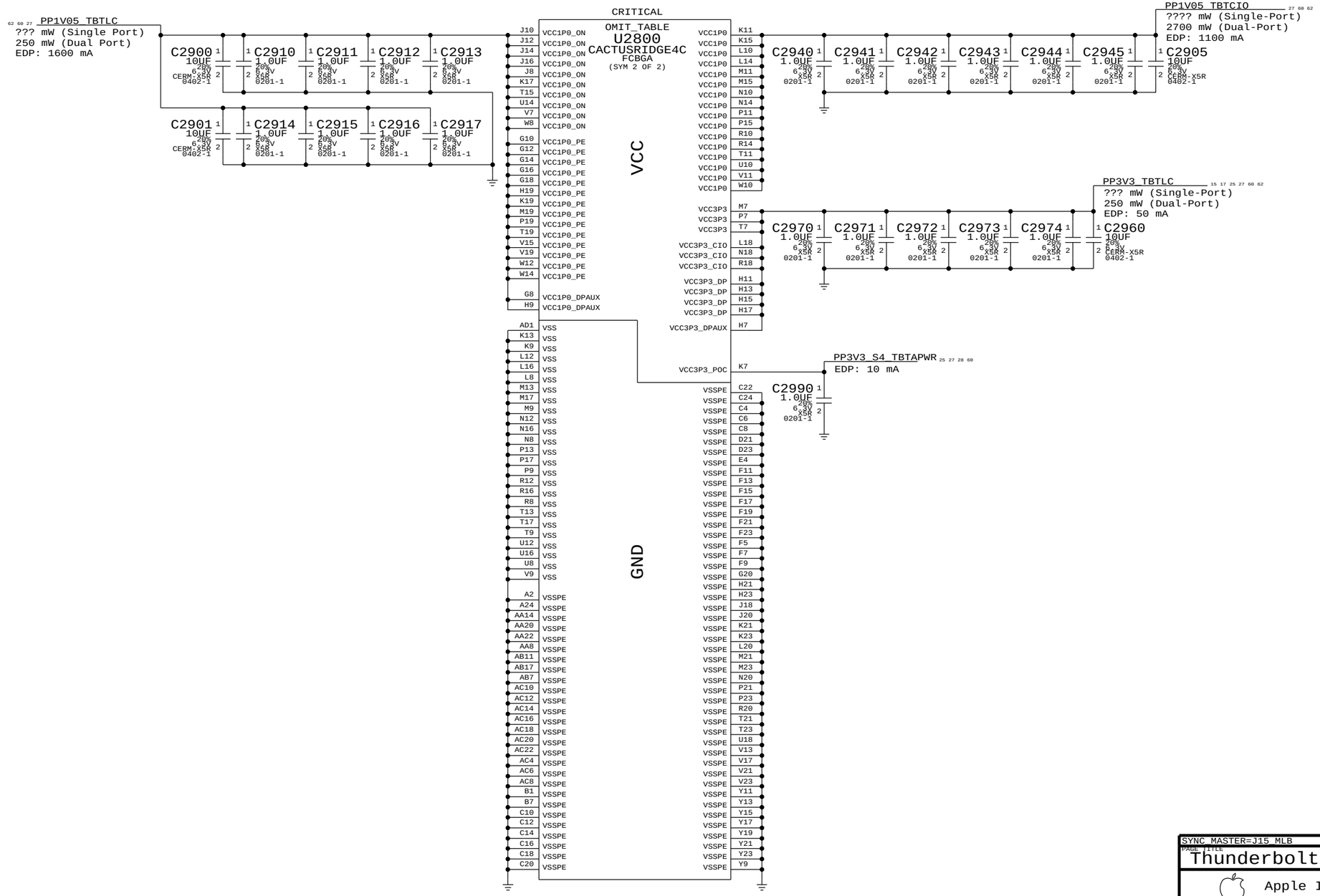

EDP numbers are from 12/22/2011 email from Haim Lustig (Intel) to Paul Baker (Apple)
Power consumption figures from CR DG v0.57, IBL doc #472455.

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SYNC_MASTER=J15_MLB SYNC_DATE=07/16/2012

PAGE TITLE: Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
(NONE)

TBT 15V Boost Regulator

PPBUS_G3H
8-13V Input
Changes required
for 2S.

R3080 470K 5% 1/20W MF 201
C3080 0.1UF 10% 16V X5R 402
R3081 150K 5% 1/20W MF 201
TBTBST_PWREN_DIV_L
TBTBST_PWREN_L
Q3005 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
TBT_A_HV_EN

CRITICAL Q3080 SI8409DB BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_S4SW_TBTBST_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here,
add property on another page.

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603
R3091 200K 1% 1/20W MF 201 <R1>

CRITICAL L3095 6.8UH-4.0A PIMB062D-SM

TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_MODE=TRUE
DIOT=TRUE

R3089 0 5% 1/20W MF 0201
TBTBST_SNS1
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TBTBST_SNS2
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

CRITICAL D3095 POWERDI-123 DFLS230L

PP15V_TBT
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

XW3095 SM
TBTBST_VSNS
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
PLACE_NEAR=C3095.1:2 mm

TBTBST_EN_UVLO
TBTBST_INTVCC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TBTBST_VC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

CRITICAL U3090 LT3957 QFN
VIN, SW, EN/UVLO, INTVCC, VC, RT, SS, SYNC, SNS1, SNS2, FBX, NC, SGND, GND

SGND shorted to
GND inside package,
no XW necessary.

C3081 2.2UF 20% 25V X5R-CERM 402
C3092 2.2UF 20% 25V X5R-CERM 402
C3087 47PF 5% 25V NP0-C0G-CERM 0201
R3093 10K 1% 1/20W MF 201
R3092 73.2K 1% 1/20W MF 201 <R2>
C3082 2.2UF 20% 25V X5R-CERM 402
C3093 3300PF 10% 10V X7R-CERM 0201
R3094 41.2K 1% 1/20W MF 201
C3094 0.33UF 10% 6.3V CERM-X5R 402

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

TBTBST_VSNS_RC
C3088 22PF 5% 50V CERM 0402
R3090 49.9K 1% 1/16W MF-LF 402
R3095 133K 1% 1/16W MF-LF 402 <Ra>
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>
NO STUFF C3089 100PF 5% 50V CERM 402

C3095 10UF 20% 25V X5R-CERM 0603
C3097 10UF 20% 25V X5R-CERM 0603
C3096 10UF 20% 25V X5R-CERM 0603
C3098 10UF 20% 25V X5R-CERM 0603
C3084 10UF 20% 25V X5R-CERM 0603
C309A 10UF 20% 25V X5R-CERM 0603
C3099 0.001UF 10% 50V X7R-CERM 0402
C3085 10UF 20% 25V X5R-CERM 0603
C309B 10UF 20% 25V X5R-CERM 0603

Vout = 1.6V * (1 + Ra / Rb)

Supervisor & CLKREQ# Isolation

PP3V3_S0

Q3040 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
R3040 10K 5% 1/20W MF 201
TBT_EN_LC_PWR
C3000 0.1UF 10% 16V X5R-CERM 0201

CRITICAL U3000 SLG4AP016V TDFN
VDD, SENSE 0.7V, DLY, RESET*, MR*, EN, OUT (OD), IN, GND, THRM PAD

PP3V3_TBTLC
R3007 100K 1% 1/20W MF 201
PP1V05_TBTLC
TBT_PCIE_RESET_L
DLY = 60 ms +/- 20%
PCH_TBT_PCIE_RESET_L
Platform (PCIe) Reset
TBT_CLKREQ_L
Pull-up provided by SB page.
TBT_CLKREQ_ISOL_L
TBT_CLKREQ_ISOL_L
MAKE_BASE=TRUE

Q3088 DMN5L06VK-7 SOT-563
Max Vgs: 10V
R3088 330K 5% 1/20W MF 201
TBTBST_SHDN_DIV
R3087 330K 5% 1/20W MF 201
Q3088 DMN5L06VK-7 SOT-563
SMC_DELAYED_PWRGD

TBT "POC" Power-up Reset

PP3V3_S4_TBTAPWR

CRITICAL U3030 TPS3808 QFN
VDD, SENSE, CT, RESET*, (IPU) MR*, GND, THRM PAD

Pull-up: R2810
TBT_PWR_ON_POC_RST_L
TBTPOCRST_CT
TBTPOCRST_MR_L
C3031 0.00047UF 10% 25V CERM 0402
C3030 0.1UF 10% 16V X5R-CERM 0201
TPS3808G25
Vt = 2.33V +/- 2%
Delay = 27.3ms
C3025 330PF 10% 16V X7R-CERM 0201
Q3025 DMN5L06VK-7 SOT-563
PP3V3_S0
R3030 100K 5% 1/20W MF 201
TBT_POC_RESET_L

3.3V TBT "LC" Switch

TBT_EN_LC_ISOL
R3011 36.5K 1% 1/20W MF 201
TBT_EN_LC_RC3V3
PP3V3_S0

U3010 TPS22924 CSP
A2, B2, VIN, C2, ON, A1, B1, VOUT, GND, C1
CRITICAL

PP3V3_TBTLC
Max Current = 2A (85C)

C3010 1.0UF 20% 6.3V X5R 0201-1
C3011 1.0UF 20% 6.3V X5R 0201-1

U3010	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

1.05V TBT "LC" Switch

R3016 0 5% 1/20W MF 0201
TBT_EN_LC_RC1V05
PP1V05_S0

U3015 TPS22920 CSP
A2, B2, C2, VIN, ON, D2, A1, B1, C1, VOUT, GND, D1
CRITICAL

PP1V05_TBTLC
Max Current = 4A (85C)

C3015 1.0UF 20% 6.3V X5R 0201-1
NO STUFF C3016 1.0UF 20% 6.3V X5R 0201-1

U3015	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	6.1 mOhm Typ 10.4 mOhm Max

1.05V TBT "CIO" Switch

PP1V05_S0
PP3V3_TBTLC
R3020 100K 5% 1/20W MF 201
TBT_EN_CIO_PWR
Q3025 DMN5L06VK-7 SOT-563
TBT_EN_CIO_PWR_L

U3020 TPS22920 CSP
A2, B2, C2, VIN, ON, D2, A1, B1, C1, VOUT, GND, D1
CRITICAL

PP1V05_TBTCIO
Max Current = 4A (85C)

C3020 1.0UF 20% 6.3V X5R 0201-1

U3020	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	6.1 mOhm Typ 10.4 mOhm Max

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SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: TBT Power Support

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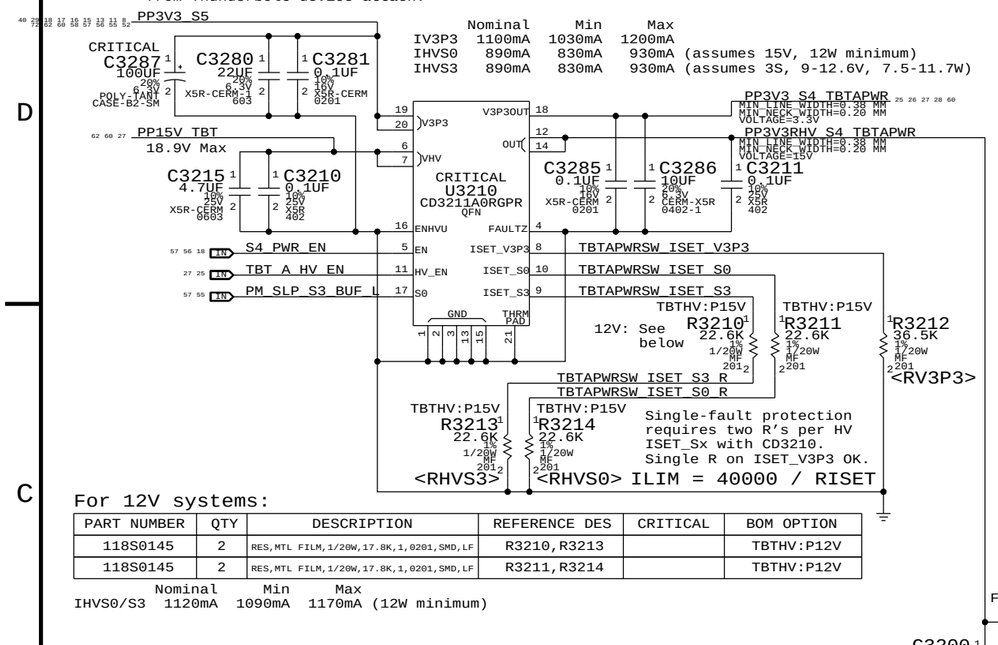
PAGE 30 OF 120
SHEET 27 OF 73

3.3V/HV Power MUX

V3P3 must be S4 to support wake
from Thunderbolt device attach.

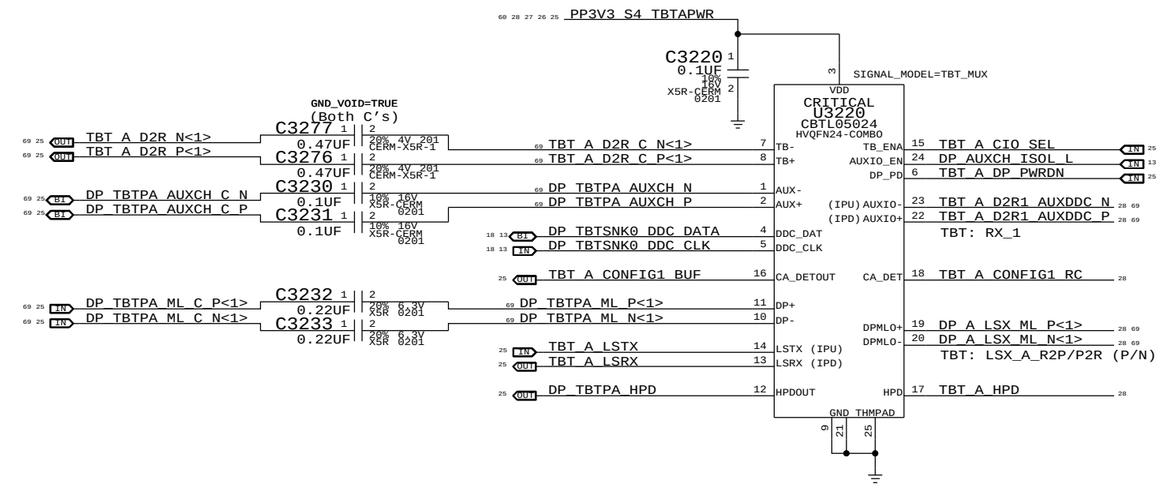
	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)



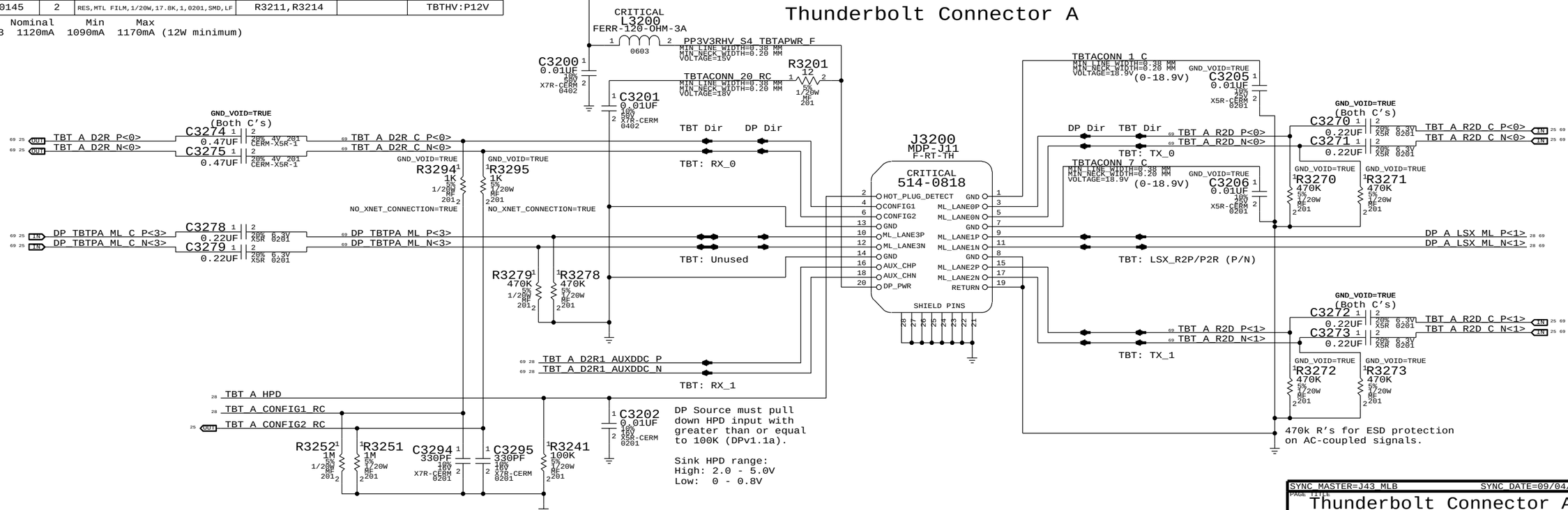
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)



Thunderbolt Connector A



SYNC MASTER=J43_MLB SYNC DATE=09/04/2012

PAGE TITLE: Thunderbolt Connector A

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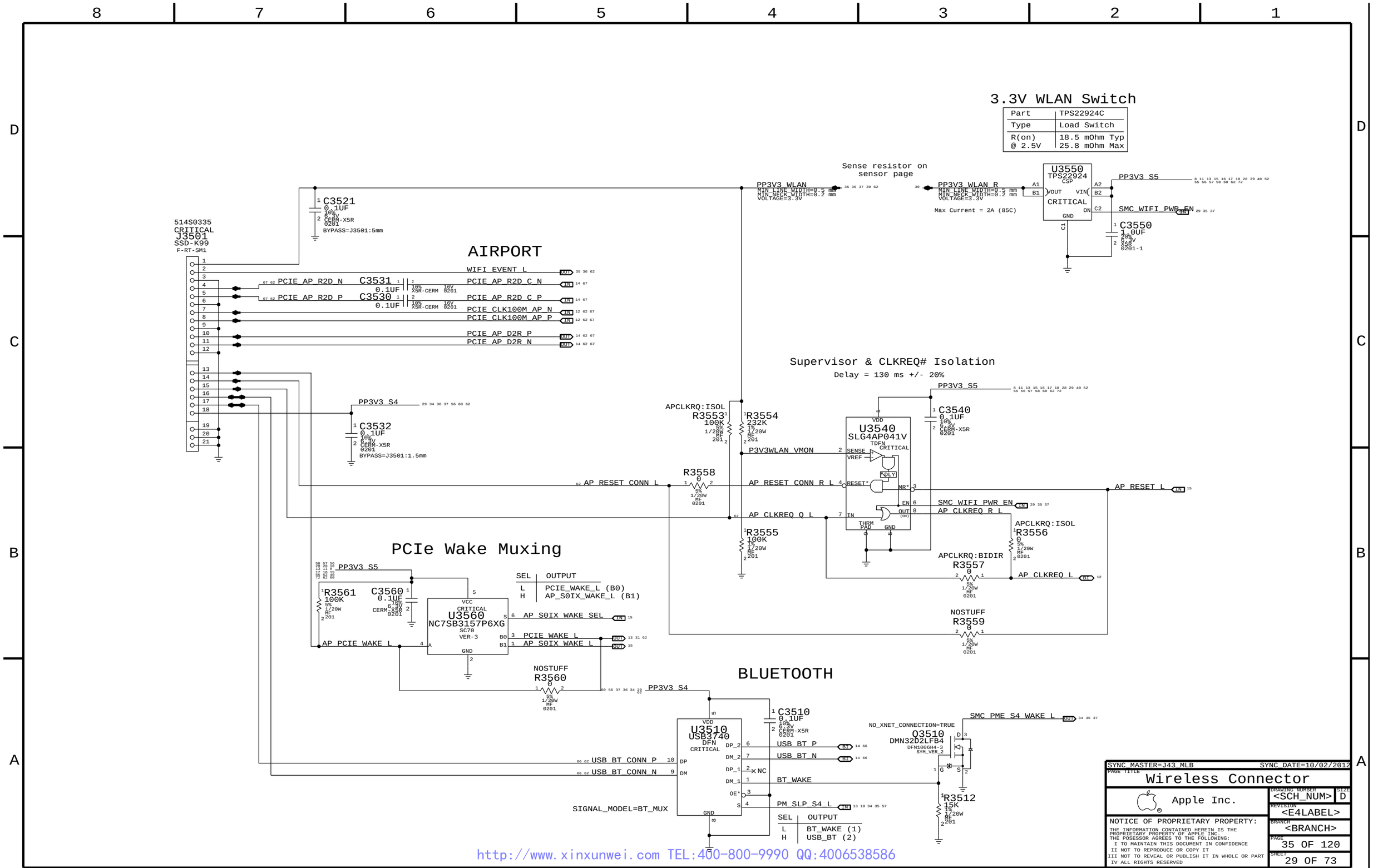

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE: Wireless Connector

Apple Inc.

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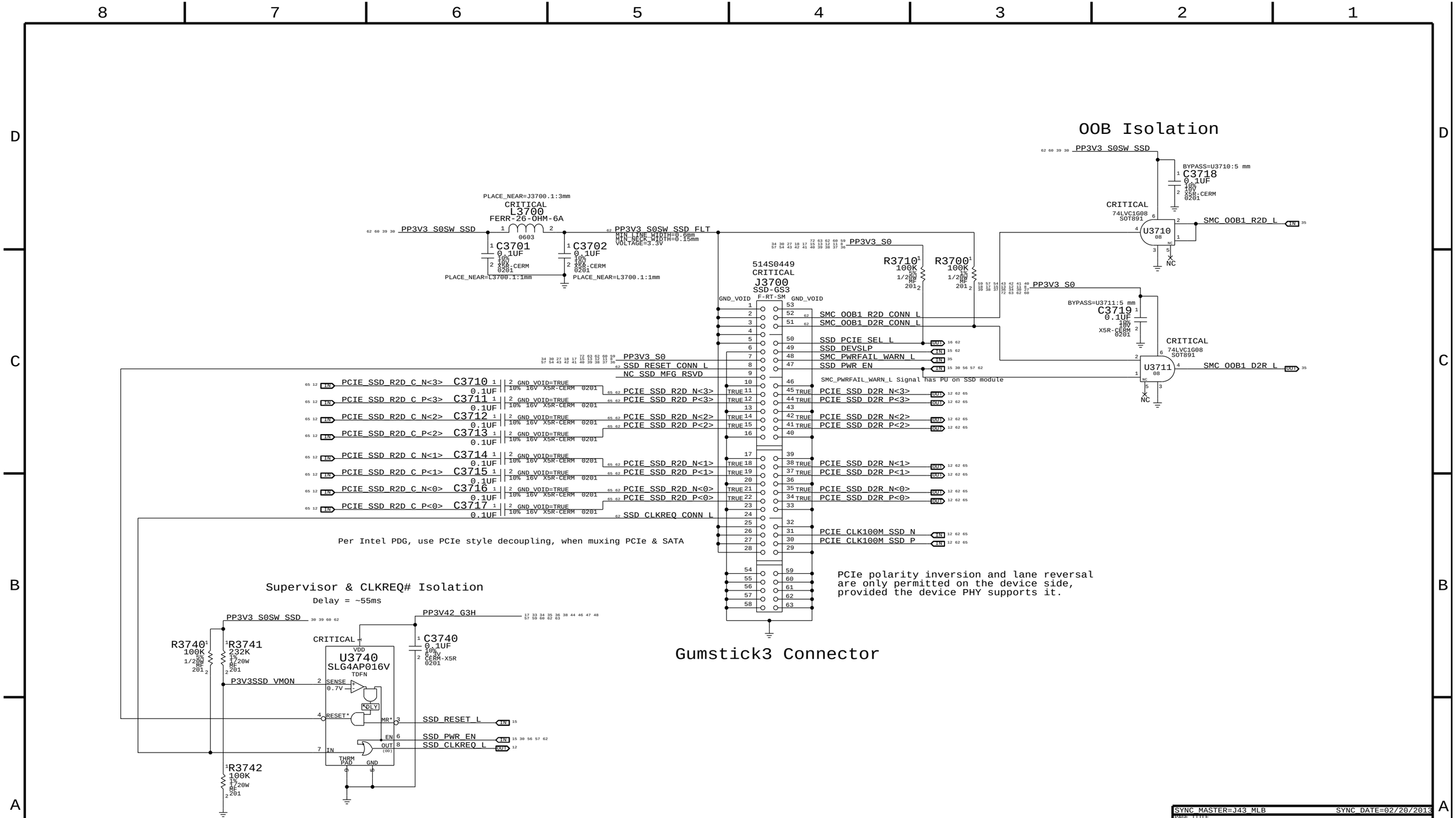

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE
SSD Connector

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DRAWING NUMBER <SCH_NUM> SIZE D

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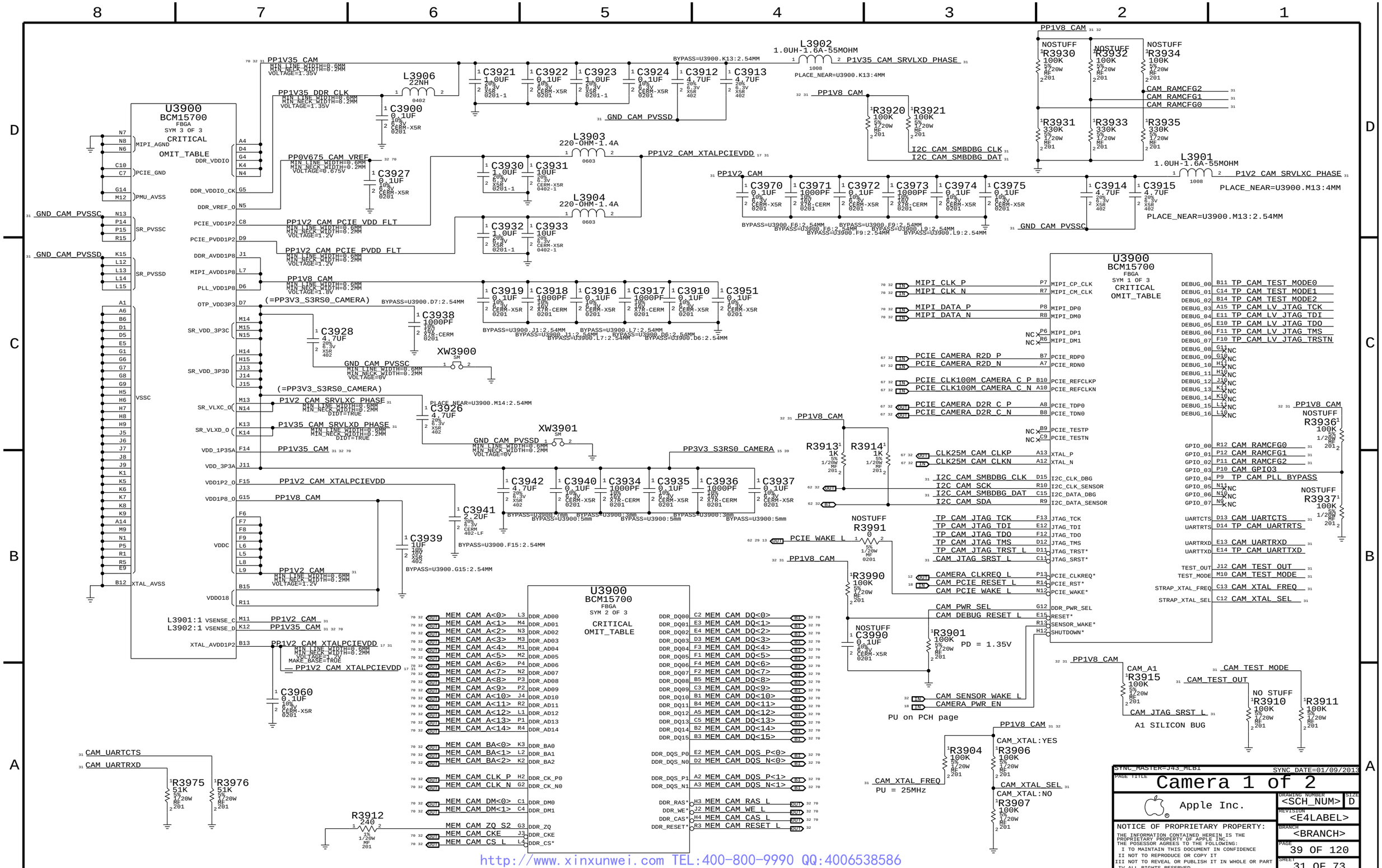
U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE
U3900
BCM15700
FBGA
SYM 2 OF 3
CRITICAL
OMIT_TABLE
L3902
1.0UH-1.6A-55MOHM
L3901
1.0UH-1.6A-55MOHM
L3906
22NH
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
PP1V35 CAM
PP1V35 DDR CLK
PP0V675 CAM VREF
PP1V2 CAM PCIE VDD FLT
PP1V2 CAM PCIE PVDD FLT
PP1V8 CAM
(=PP3V3_S3RS0_CAMERA)
P1V2 CAM SRVLXC PHASE
P1V35 CAM SRVLXD PHASE
PP1V2 CAM XTALPCIEVDD
PP3V3 S3RS0 CAMERA
GND CAM PVSSD
GND CAM PVSSC
XW3900
XW3901
PP1V8 CAM
NOSTUFF
R3930
R3932
R3934
R3931
R3933
R3935
CAM RAMCFG2
CAM RAMCFG1
CAM RAMCFG0
R3920
R3921
I2C CAM SMBDBG CLK
I2C CAM SMBDBG DAT
MIPI CLK P
MIPI CLK N
MIPI DATA P
MIPI DATA N
PCIE CAMERA R2D P
PCIE CAMERA R2D N
PCIE CLK100M CAMERA C P
PCIE CLK100M CAMERA C N
PCIE CAMERA D2R C P
PCIE CAMERA D2R C N
CLK25M CAM CLKP
CLK25M CAM CLKN
I2C CAM SMBDBG CLK
I2C CAM SCK
I2C CAM SMBDBG DAT
I2C CAM SDA
TP CAM JTAG TCK
TP CAM JTAG TDI
TP CAM JTAG TDO
TP CAM JTAG TMS
TP CAM JTAG TRST L
CAM JTAG SRST L
CAMERA CLKREQ L
CAM PCIE RESET L
CAM PCIE WAKE L
CAM PWR SEL
CAM DEBUG RESET L
CAM SENSOR WAKE L
CAMERA PWR EN
PCIE WAKE L
R3991
R3990
R3901
PD = 1.35V
PU on PCH page
R3913
R3914
R3936
R3937
CAM RAMCFG0
CAM RAMCFG1
CAM RAMCFG2
CAM GPIO3
TP CAM PLL BYPASS
CAM UARTCTS
TP CAM UARTRTS
CAM UARTRXD
TP CAM UARTTXD
CAM TEST OUT
CAM TEST MODE
CAM XTAL FREQ
CAM XTAL SEL
CAM_A1
R3915
CAM JTAG SRST L
A1 SILICON BUG
CAM TEST MODE
CAM TEST OUT
NO STUFF
R3910
R3911
CAM_XTAL:YES
R3904
R3906
CAM_XTAL:NO
R3907
CAM XTAL FREQ
PU = 25MHz
CAM UARTCTS
CAM UARTRXD
R3975
R3976
R3912
240
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MEM CAM A<1>
MEM CAM A<2>
MEM CAM A<3>
MEM CAM A<4>
MEM CAM A<5>
MEM CAM A<6>
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MEM CAM A<9>
MEM CAM A<10>
MEM CAM A<11>
MEM CAM A<12>
MEM CAM A<13>
MEM CAM A<14>
MEM CAM BA<0>
MEM CAM BA<1>
MEM CAM BA<2>
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MEM CAM CLK N
MEM CAM DM<0>
MEM CAM DM<1>
MEM CAM ZQ S2
MEM CAM CKE
MEM CAM CS L
MEM CAM DQ<0>
MEM CAM DQ<1>
MEM CAM DQ<2>
MEM CAM DQ<3>
MEM CAM DQ<4>
MEM CAM DQ<5>
MEM CAM DQ<6>
MEM CAM DQ<7>
MEM CAM DQ<8>
MEM CAM DQ<9>
MEM CAM DQ<10>
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MEM CAM DQ<12>
MEM CAM DQ<13>
MEM CAM DQ<14>
MEM CAM DQ<15>
MEM CAM DQS P<0>
MEM CAM DQS N<0>
MEM CAM DQS P<1>
MEM CAM DQS N<1>
MEM CAM RAS L
MEM CAM WE L
MEM CAM CAS L
MEM CAM RESET L
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SYNC_MASTER=J43_MLB1
SYNC DATE=01/09/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
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<SCH_NUM>
SIZE
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REVISION
<E4LABEL>
BRANCH
<BRANCH>
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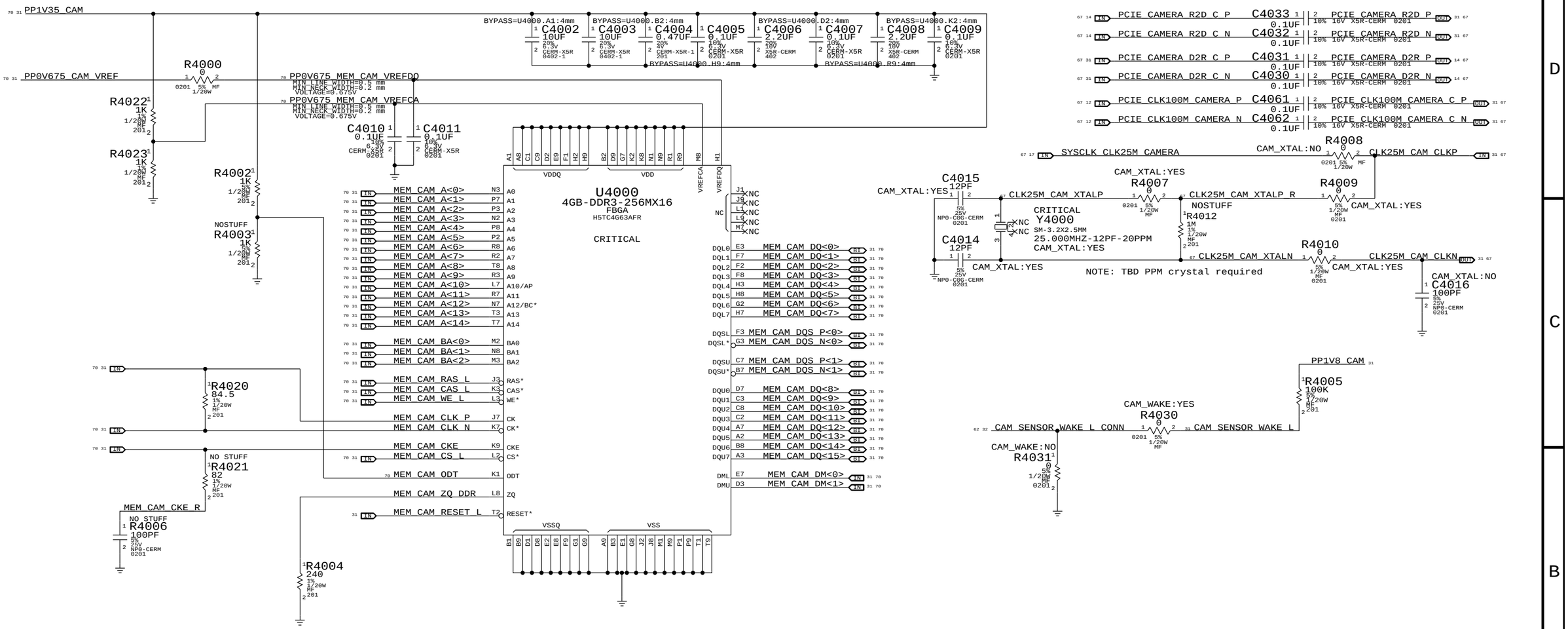

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PAGE TITLE: Camera 2 of 2

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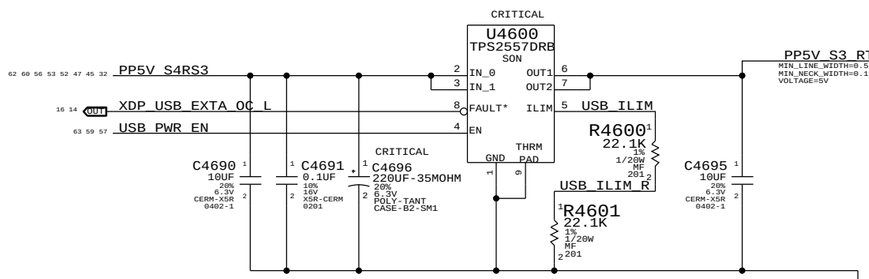
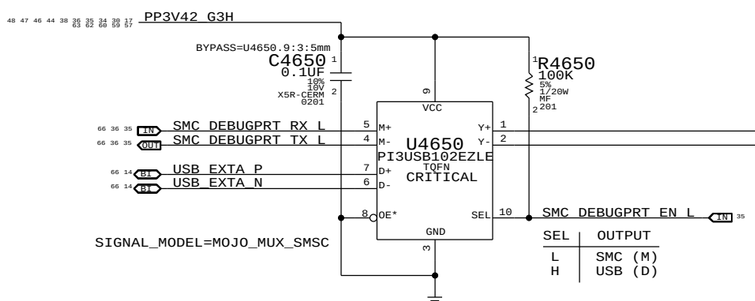
Right USB Port A

USB Port Power Switch

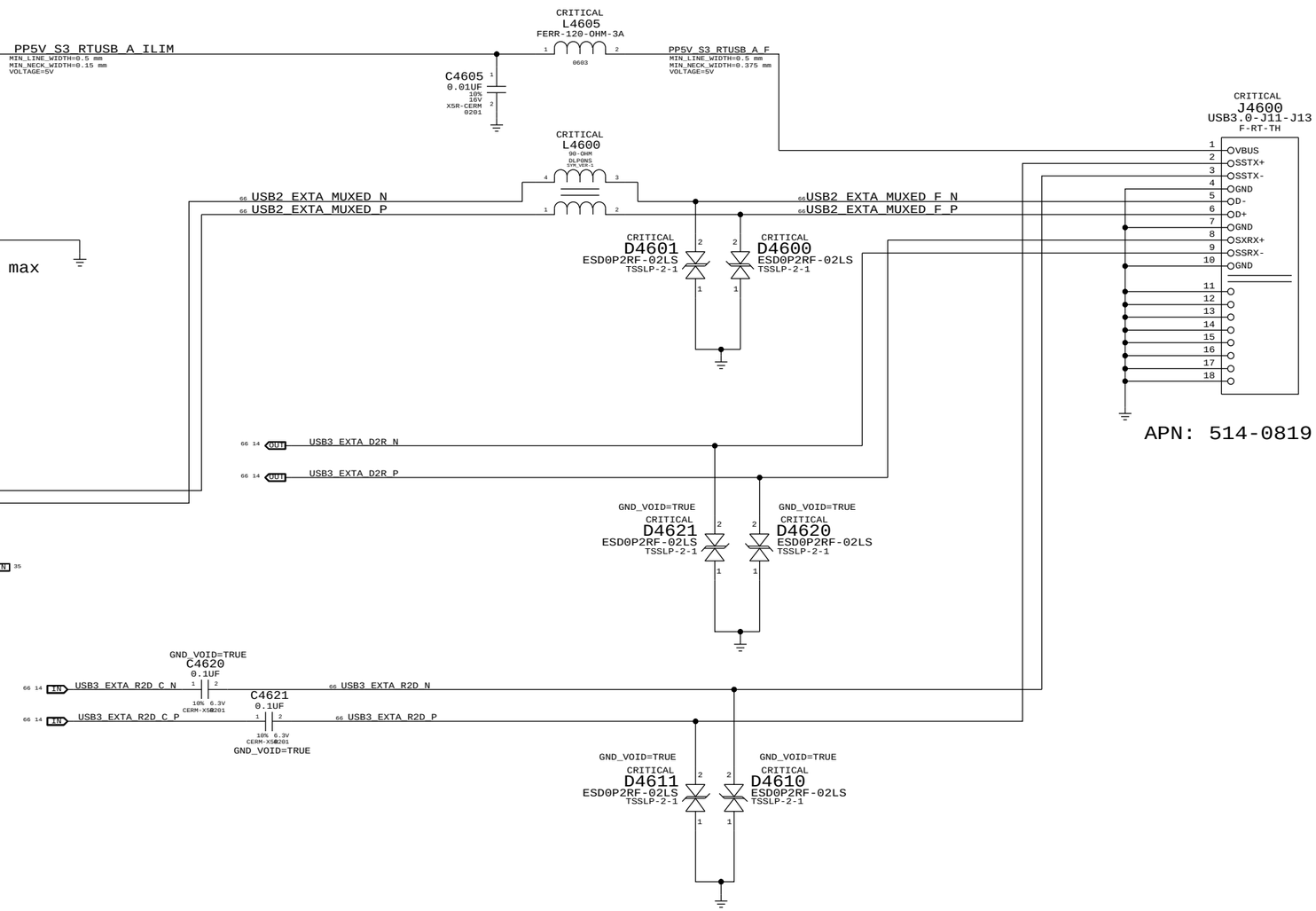


Current limit per port (R4600+R4601): 2.19A min / 2.76A max

Mojo SMC Debug Mux



SEL	OUTPUT
L	SMC (M)
H	USB (D)



APN: 514-0819

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PAGE TITLE
External A USB3 Connector

Apple Inc.

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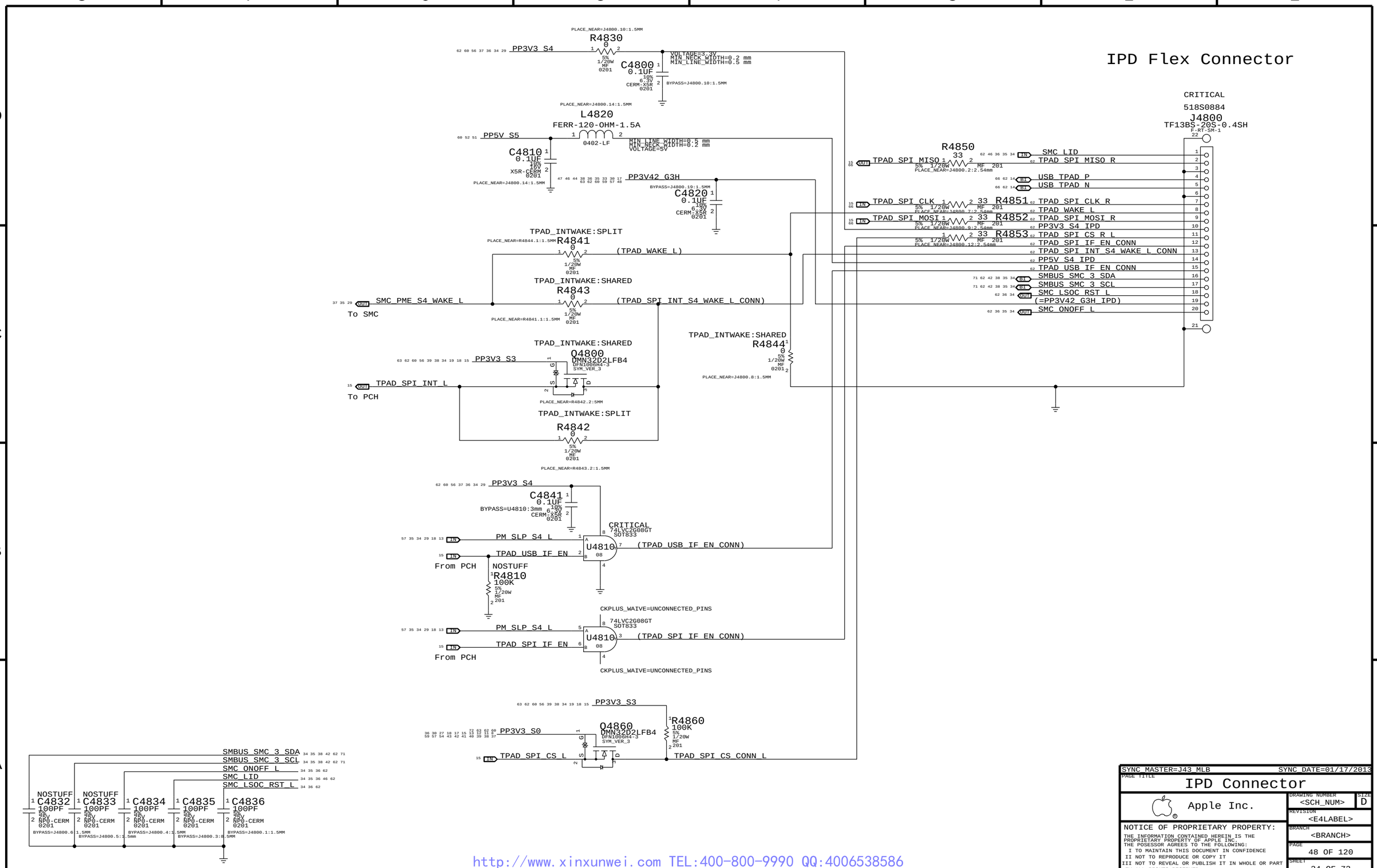

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PAGE TITLE
IPD Connector

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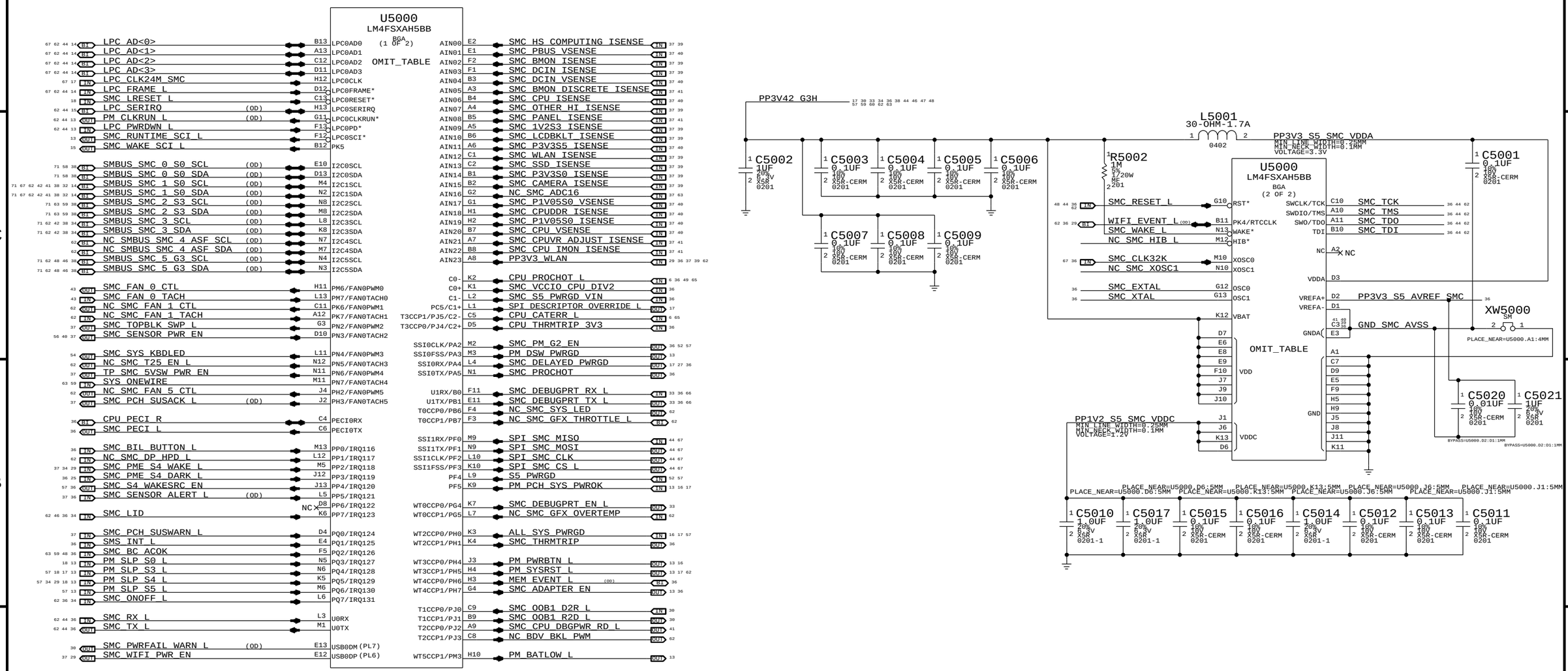

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE
SMC

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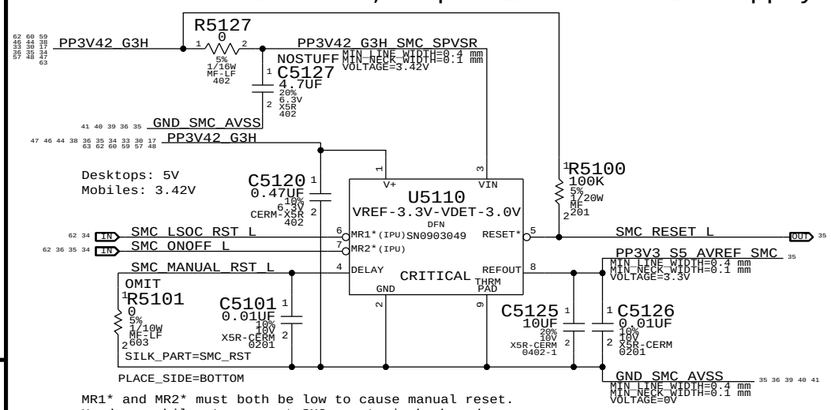
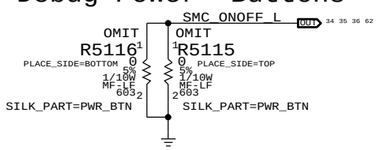
SMC Reset "Button", Supervisor & AVREF Supply



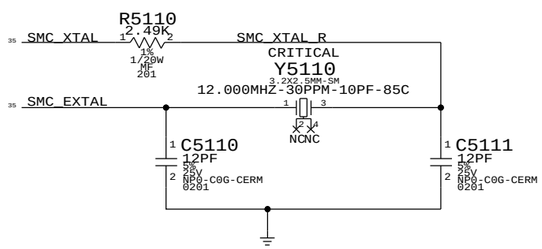
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

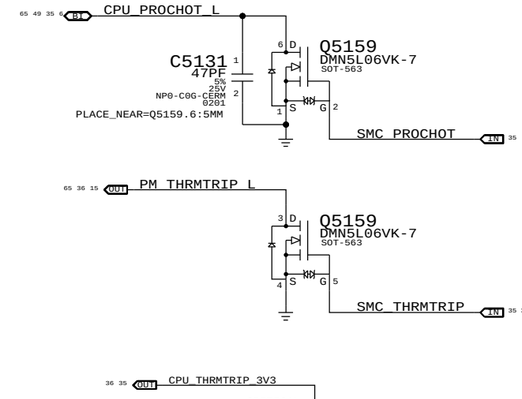
Debug Power "Buttons"



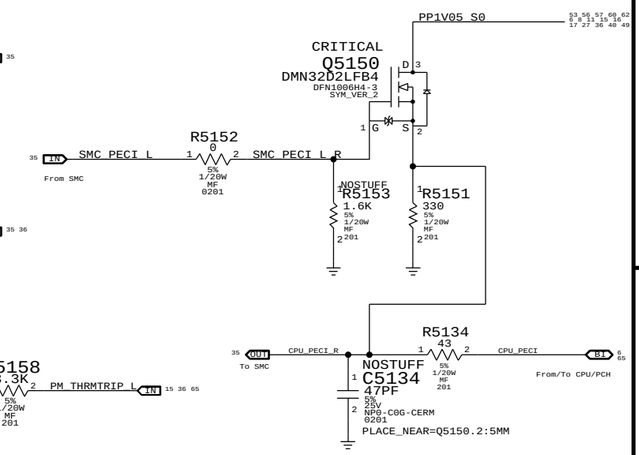
SMC Crystal Circuit

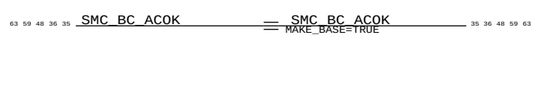
SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz

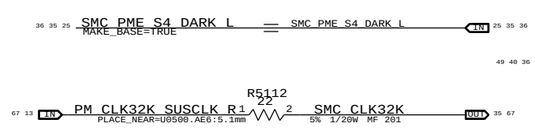


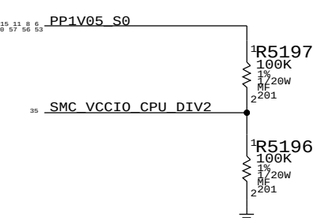


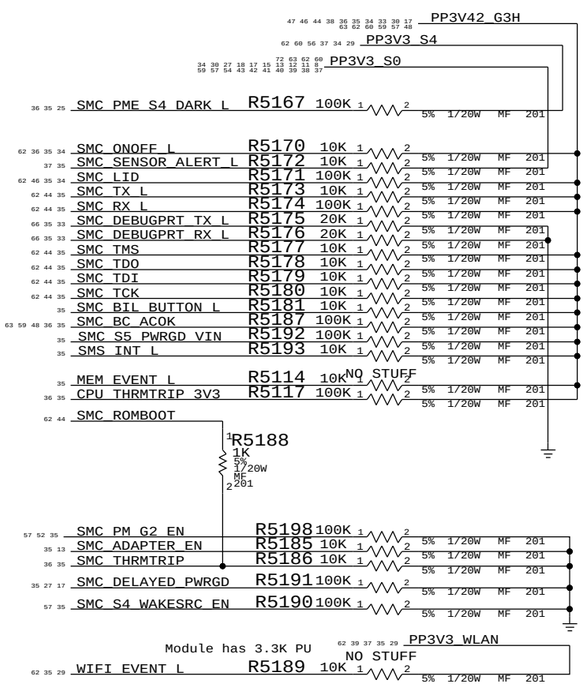
SMC12 PECI Support











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Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
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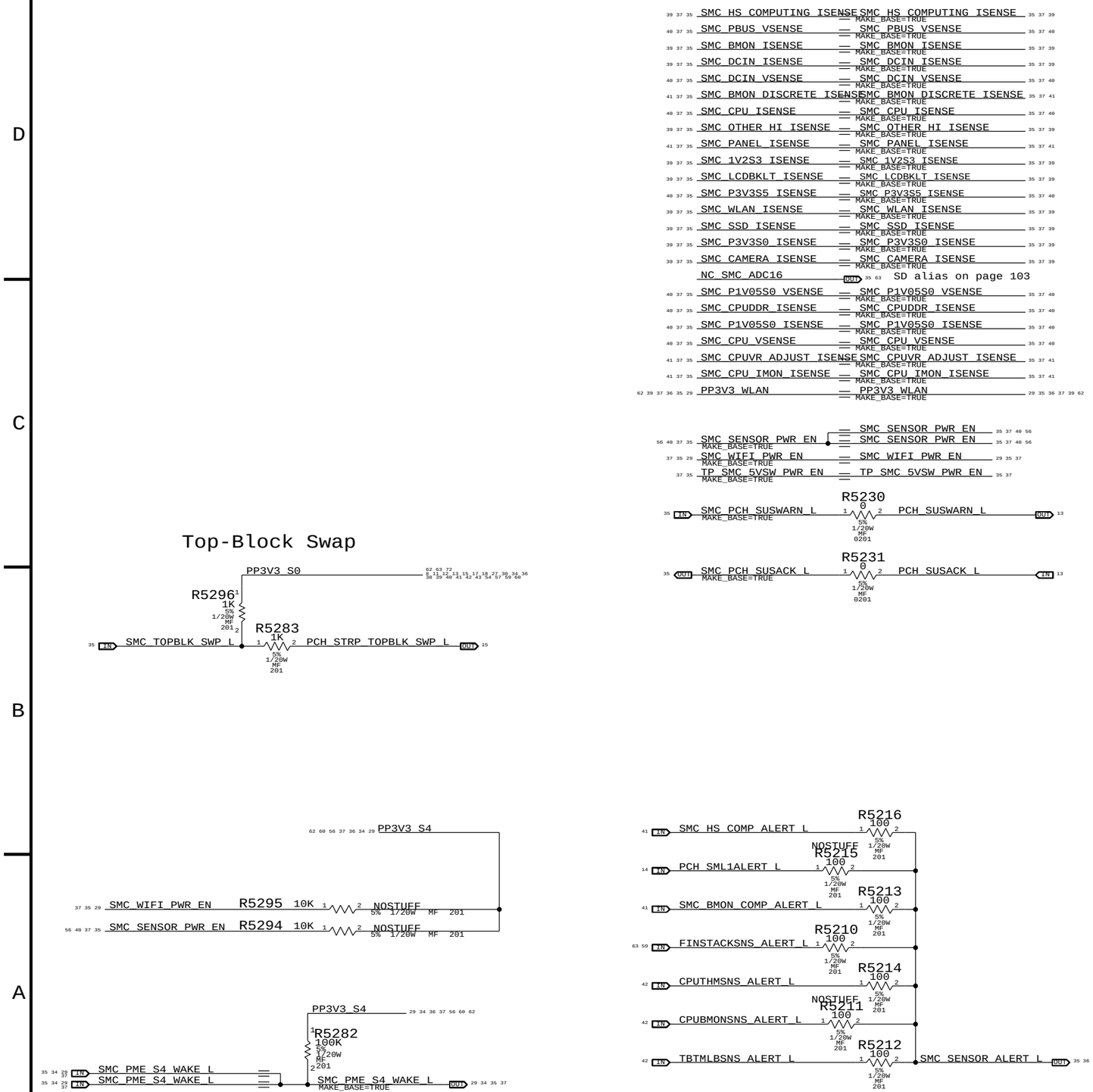

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PAGE TITLE
SMC Project Support

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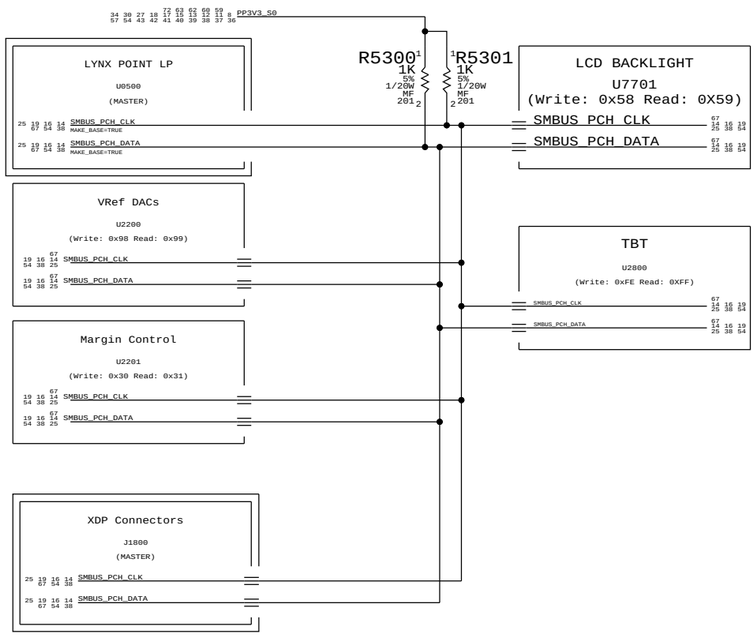
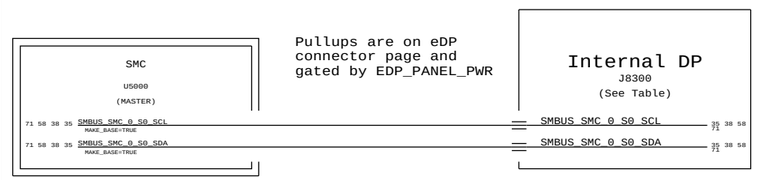
LYNX POINT LP S0 SMBus "0" Connections



SMC "0" SMBus S0 Connections



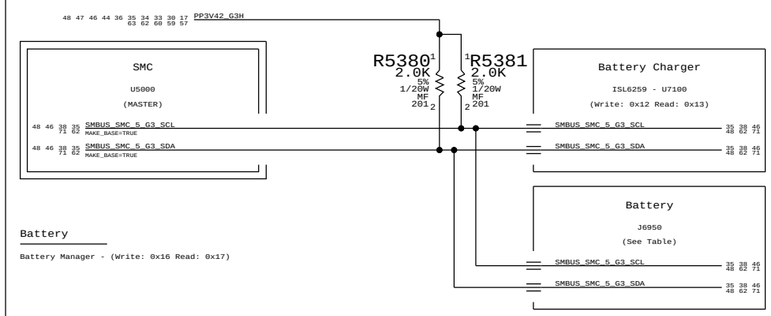
Pullups are on eDP connector page and gated by EDP_PANEL_PWR

(* = Multiple options)

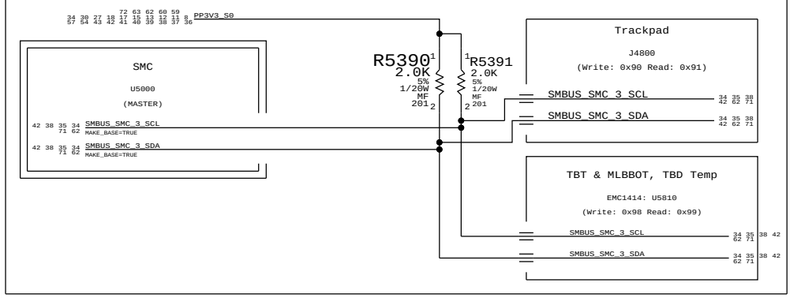
Internal DP

		J43		J41		
		Samsung	LGD	Samsung	LGD	AUO
Analogix T-con	- (Write: 0x7B/0x87 Read: 0x7C/0x88)	N	Y	*	Y	*
Parade T-con	- (0x10-0x1F or 0x30-0x3F)	Y	N	*	N	*
DVR	- (Write: 0x4E Read: 0x4F)	Y	Y	Y	Y	N

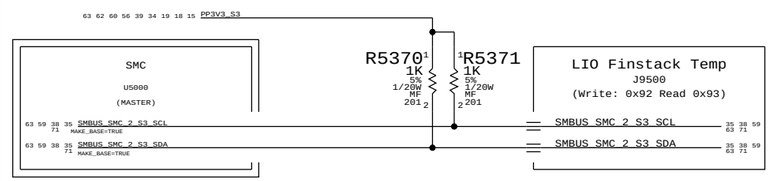
SMC "5" SMBus G3H Connections



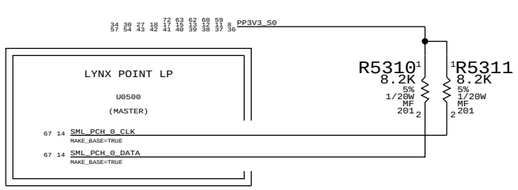
SMC "3" SMBus S0 Connections



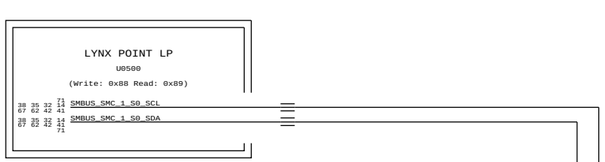
SMC "2" SMBus S3 Connections



LYNX POINT LP S0 "SMLink 0" Connections

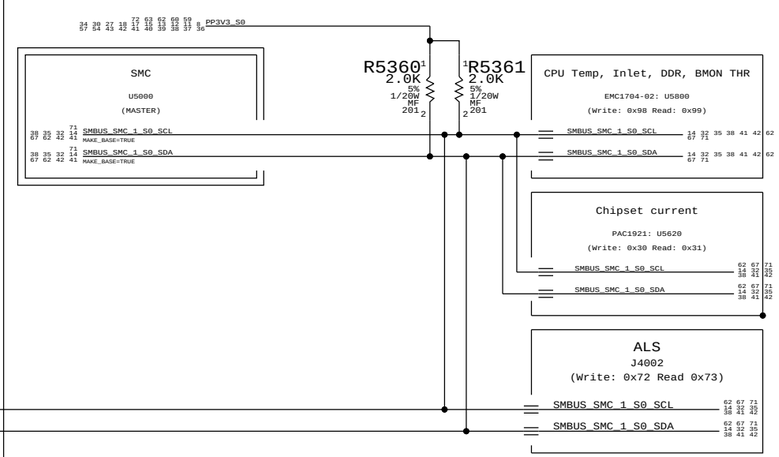


LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH

SMC S0 "1" SMBus Connections



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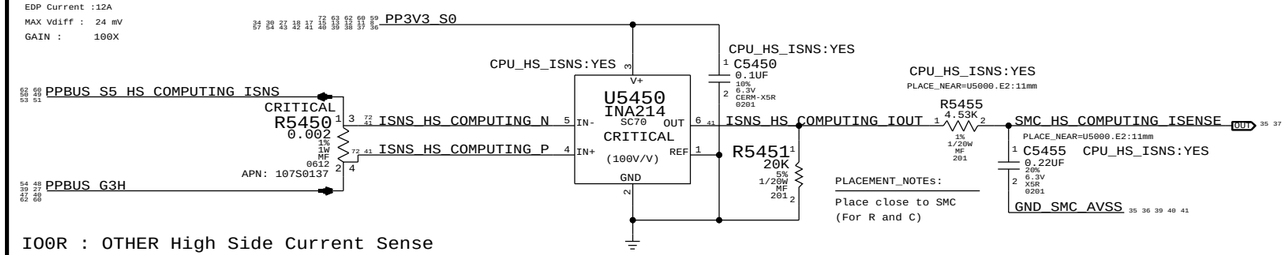
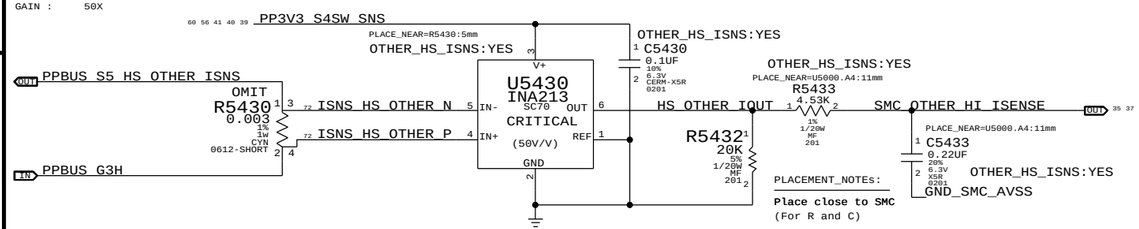
IC0R : COMPUTING High Side Current Sense

EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X



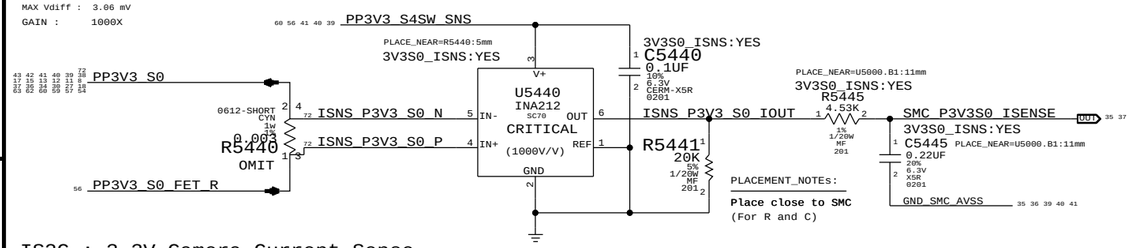
IO0R : OTHER High Side Current Sense

EDP Current :10.75A
MAX Vdiff : 53.75 mV
GAIN : 50X



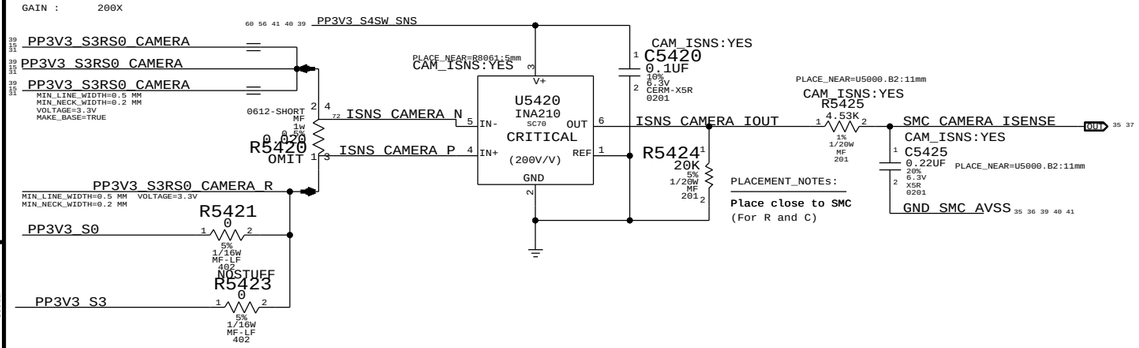
IR0C : 3.3V S0 FET Current Sense

EDP Current :1.02A
MAX Vdiff : 3.06 mV
GAIN : 1000X

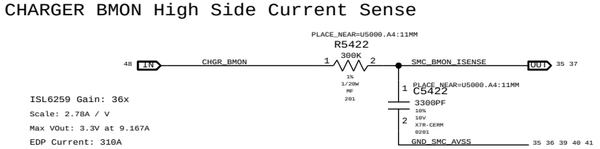


IS2C : 3.3V Camera Current Sense

EDP Current : 0.82A
MAX Vdiff : 16.36 mV
GAIN : 200X

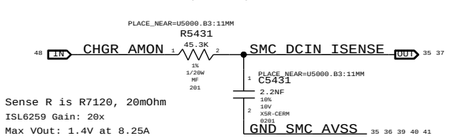


CHARGER BMON High Side Current Sense



ISL6259 Gain: 36X
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A
EDP Current: 310A

DC-IN (AMON) Current Sense

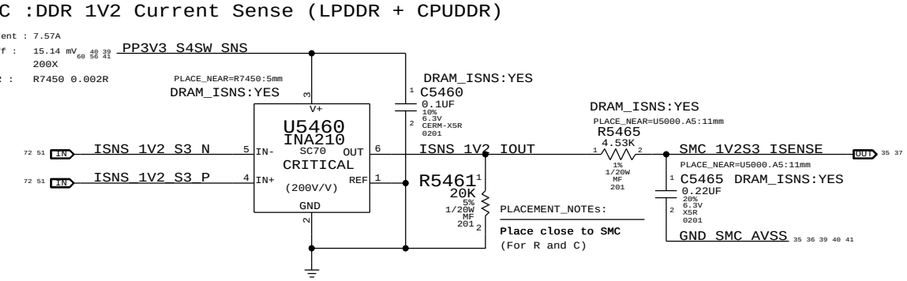


Sense R is R7120, 20mOhm
ISL6259 Gain: 20x
Max VOut: 1.4V at 8.25A
Scale: 2.5A / V
EDP Current: 3.5A

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES,SENSE,0.003OHM,1W,4-TERM,1%,0612,TFT	R5480	CRITICAL	

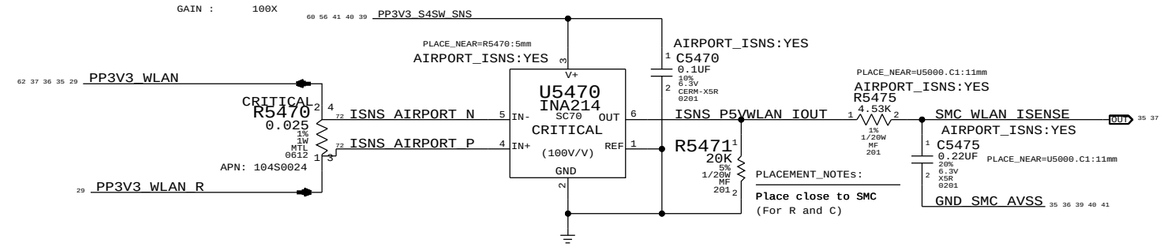
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)

EDP Current : 7.57A
MAX Vdiff : 15.14 mV
GAIN : 200X
SENSE R : R7450 0.002R



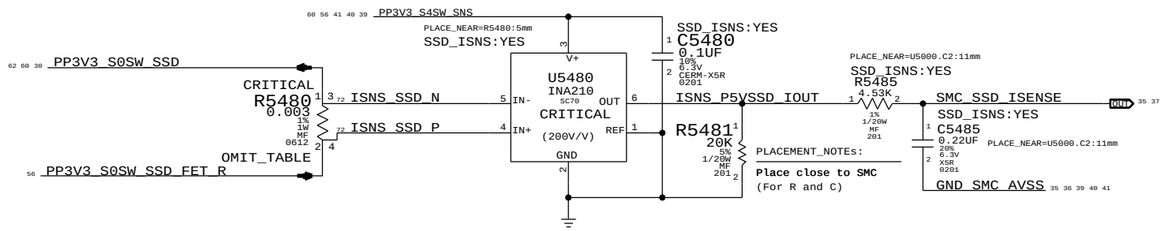
IAPC :AirPort Current Sense

EDP Current : 1.00A
MAX Vdiff : 25 mV
GAIN : 100X



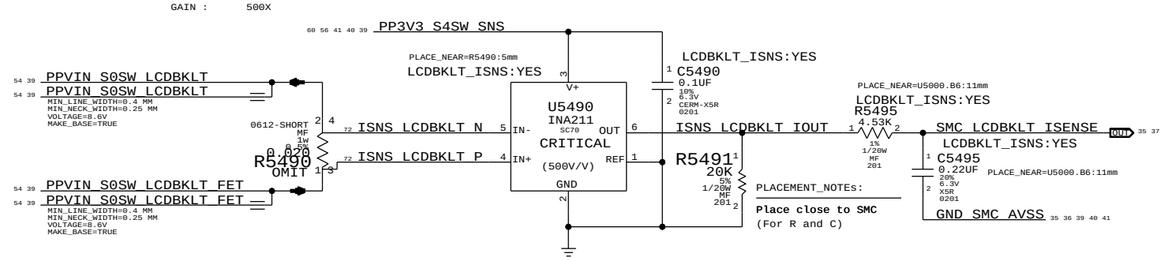
ISDC : SSD Current Sense

EDP Current : 3.00A
MAX Vdiff : 15 mV
GAIN : 200X



IBLC : LCD Backlight Driver Input Current Sense

EDP Current : 0.67A
MAX Vdiff : 0.06 mV
GAIN : 500X



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5455		CPU_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5465		DRAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5485		SSD_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLT_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5433		OTHER_HS_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5425		CAM_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5445		3V3S0_ISNS:NO

SYNC MASTER=SID_J41 SYNC DATE=02/26/2013

PAGE TITLE
High Side Current Sensing

Apple Inc.

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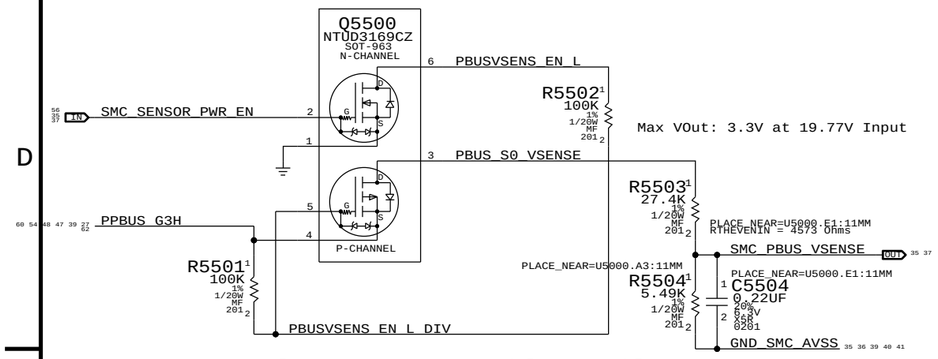
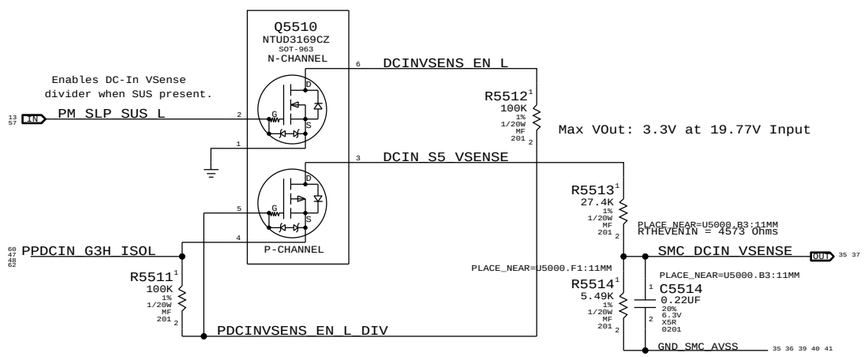
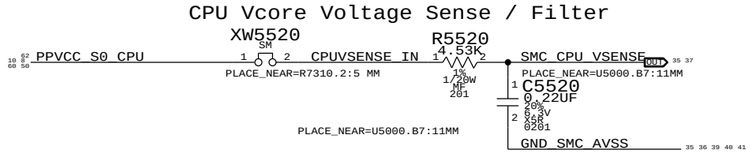
VP0R: PBUS Voltage Sense Enable & Filter



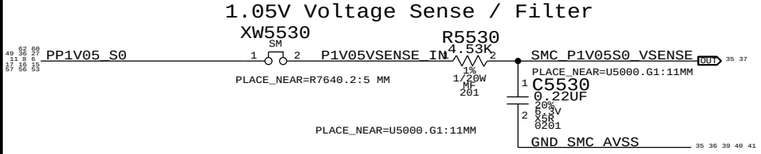
VD0R: DC-In Voltage Sense Enable & Filter



CPU Vcore Voltage Sense / Filter

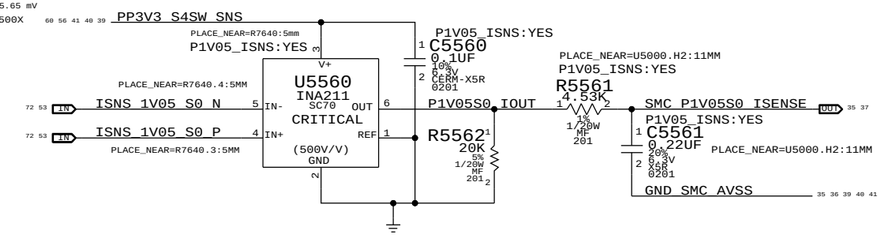


1.05V Voltage Sense / Filter

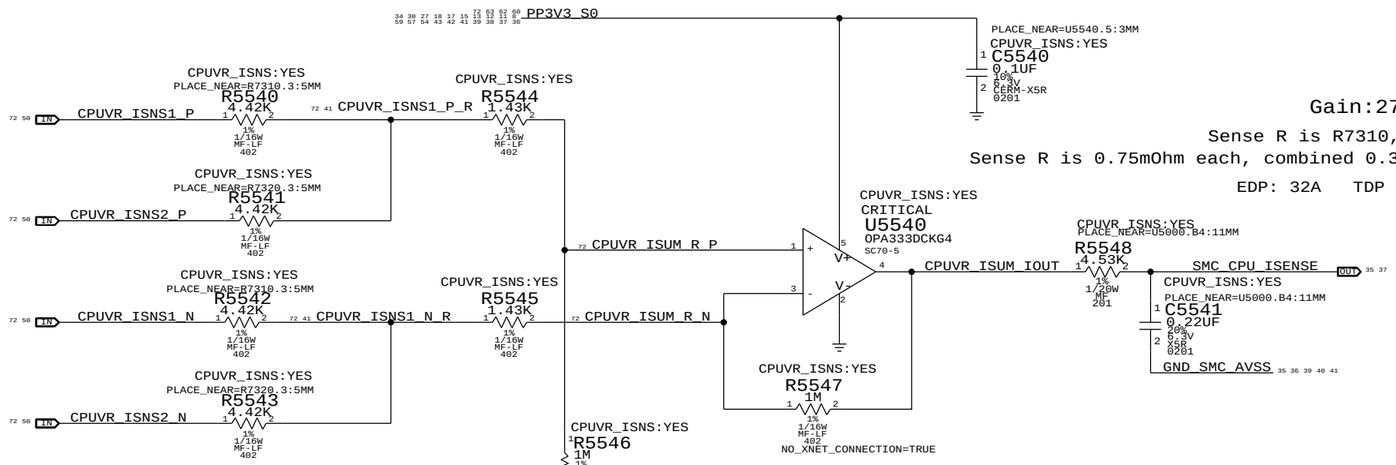


IC1C: 1.05V S0 CURRENT SENSE / FILTER

EDP Current : 1A
MAX Vdiff : 5.65 mV
GAIN : 500X



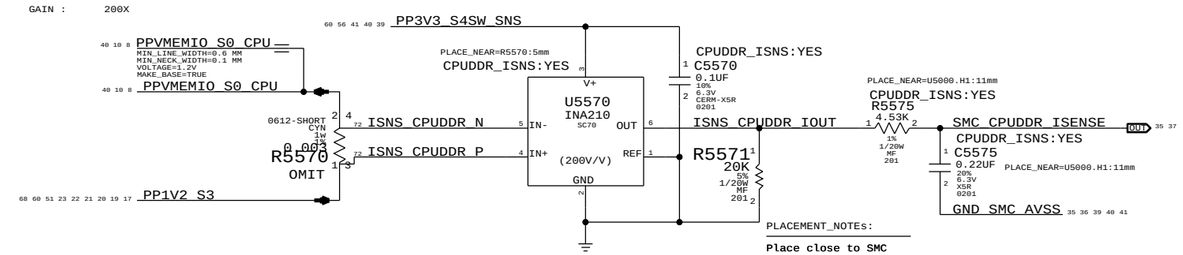
ICS0 : CPU VCore Load Side Current Sense



Gain:274.72x
Sense R is R7310, R7320
Sense R is 0.75mOhm each, combined 0.375mOhm
EDP: 32A TDP :28.05A

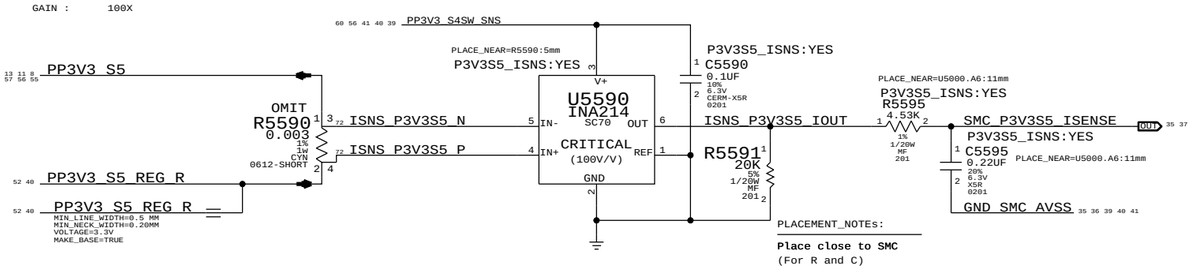
IM0C : CPU DDR Current Sense

EDP Current : 3.00A
MAX Vdiff : 12.60 mV
GAIN : 200X



IR5C :3.3 S5 REG Current Sense

EDP Current : 3.00A
MAX Vdiff : 30.00 mV
GAIN : 100X



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5541		CPUVR_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5561		P1V05_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5595		P3V3S5_ISNS:NO
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5575		CPUDDR_ISNS:NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

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Voltage & Load Side Current Sensing

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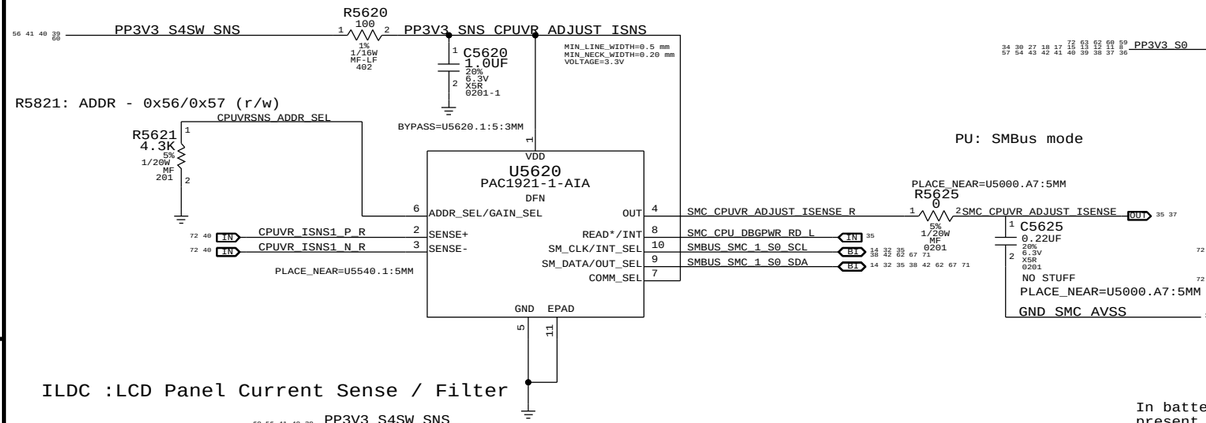
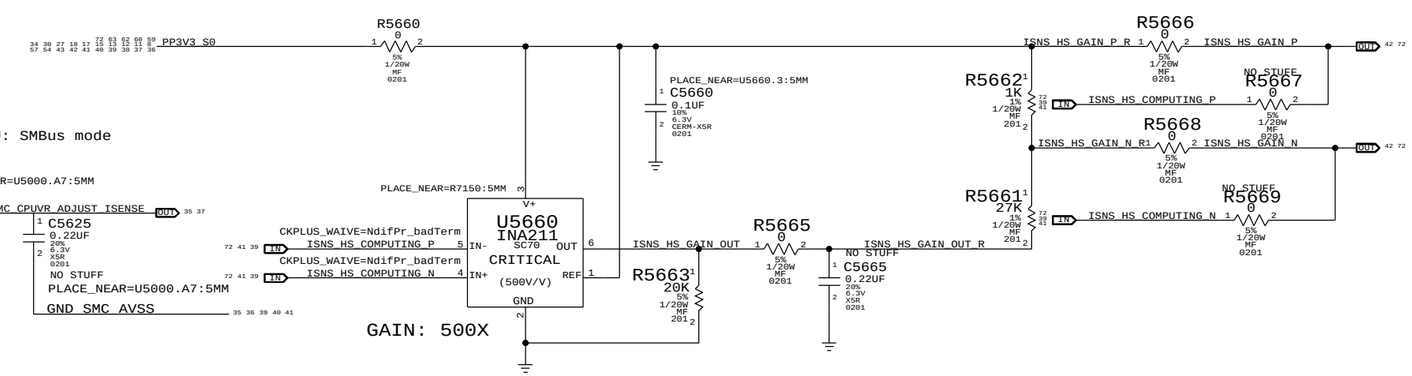
ICS3 : Adjustable Gain CPU VR Current



PU: SMBus mode

Sense Pins gain stage for U5800 (EMC1704)

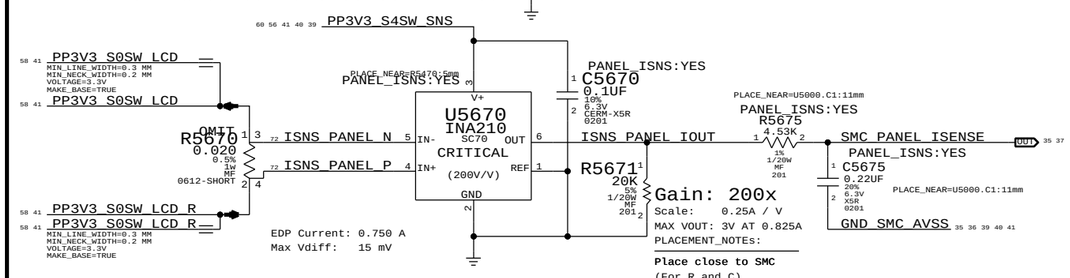


GAIN: 500X

In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

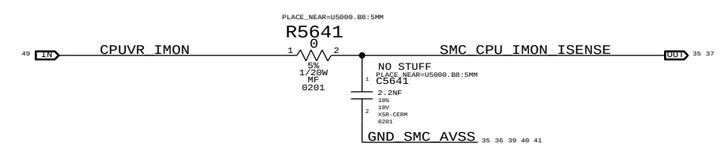
ILDC :LCD Panel Current Sense / Filter



EDP Current: 0.750 A
Max Vdiff: 15 mV

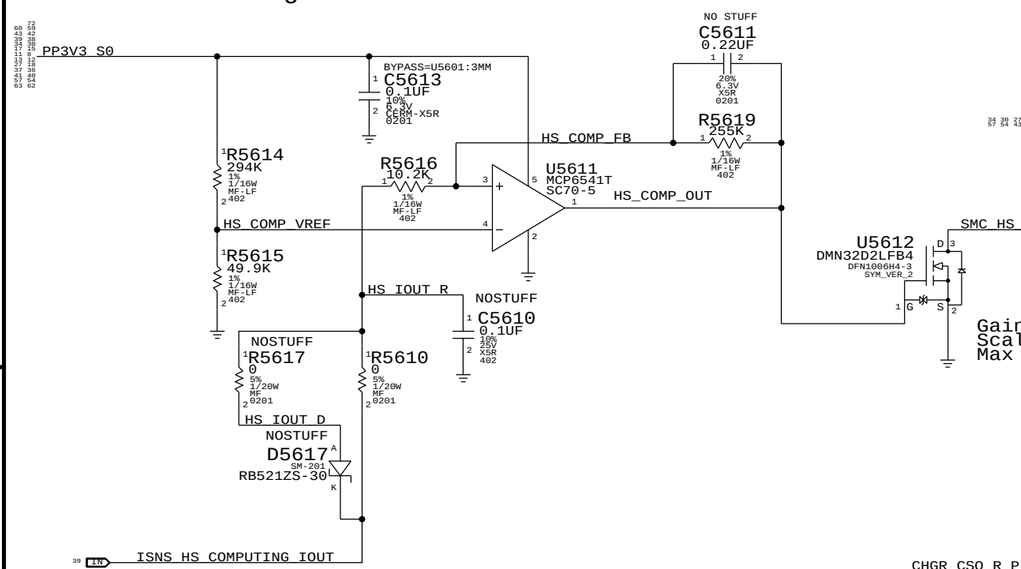
Gain: 200x
Scale: 0.25A / V
MAX VOUT: 3V AT 0.825A
PLACEMENT_NOTES:
Place close to SMC
(For R and C)

VR IMON Current Sense Filter



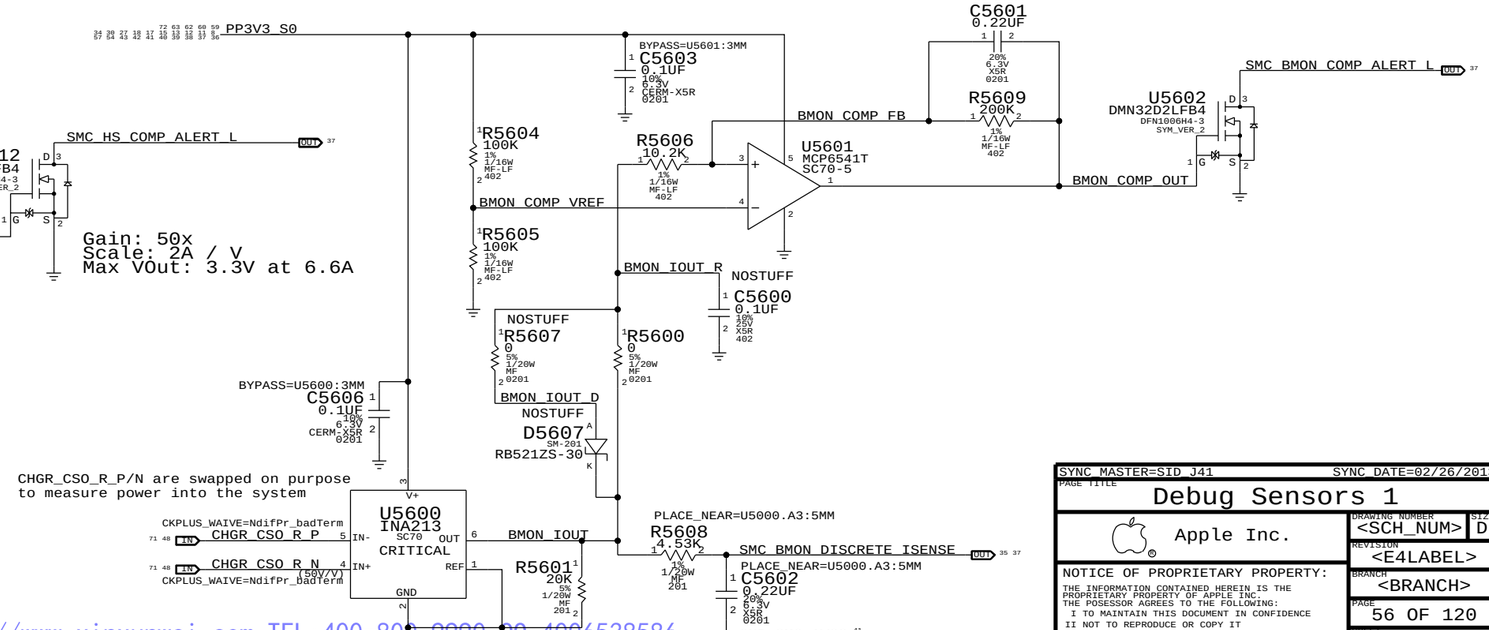
Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

Discrete High side Current threshold



Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

BMON : Discrete BMON Current Sense / Filter



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MF,1/20W,100K OHM,5,0201,SMD	C5675		PANEL_ISNS:NO

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PAGE TITLE
Debug Sensors 1

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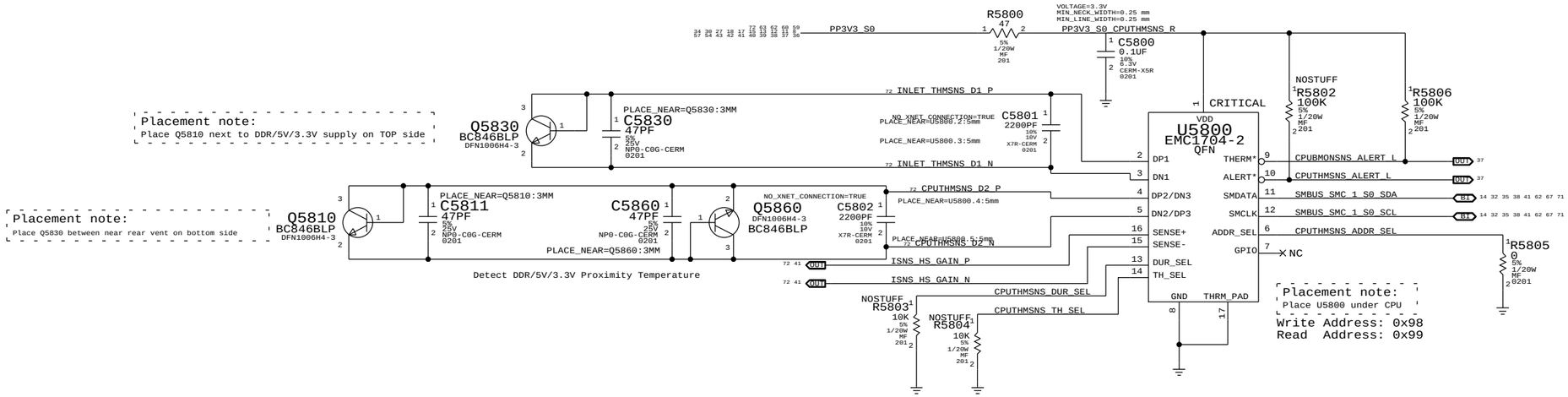
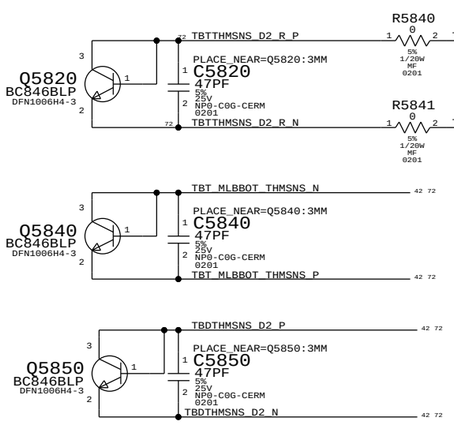
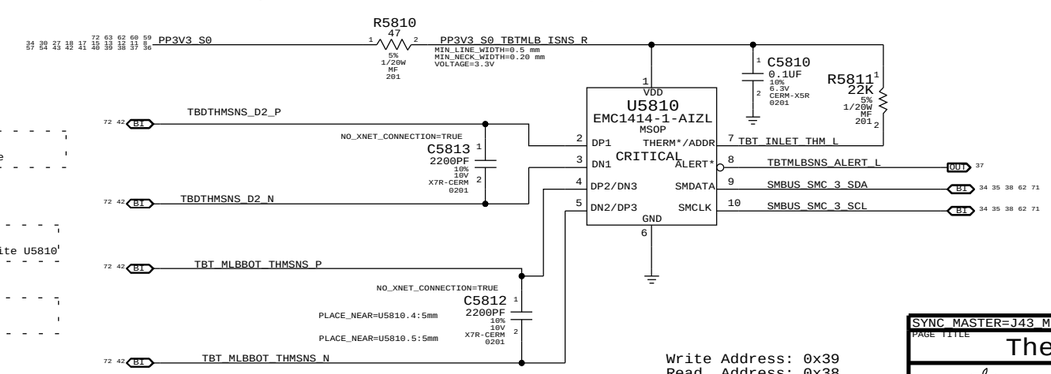
CPU Proximity, Inlet ,DDR and BMON THR Sensor

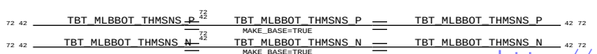


TBT,MLB Bottom Proximity Sensors



TBT, MLBBOT and TBD Temp Sensor





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SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE: Thermal Sensors

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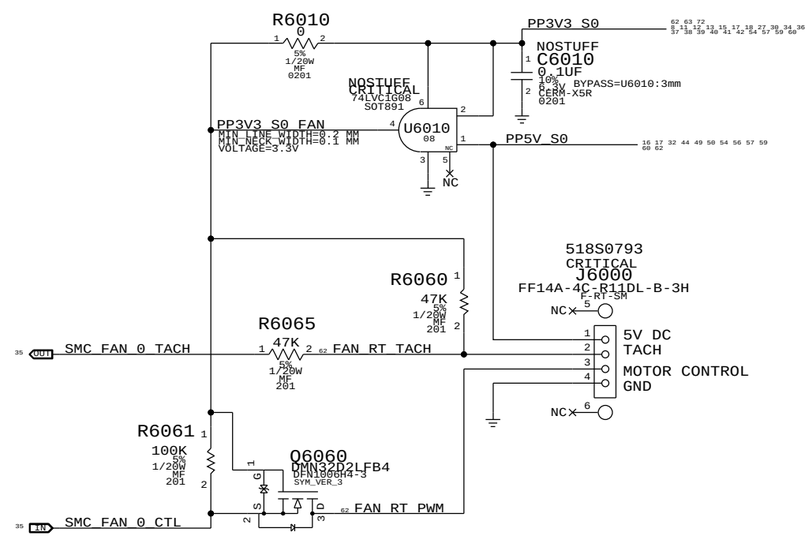
FAN CONNECTOR



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PAGE TITLE
Fan

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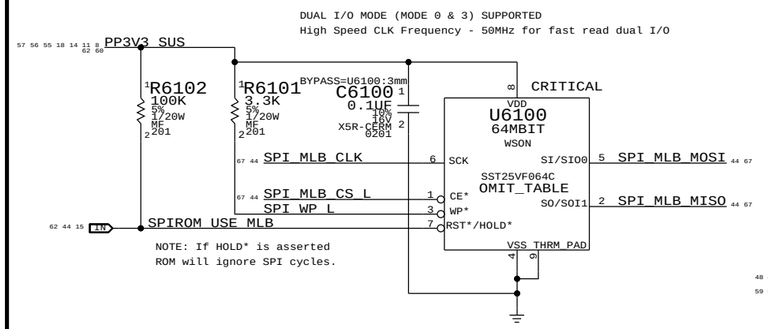
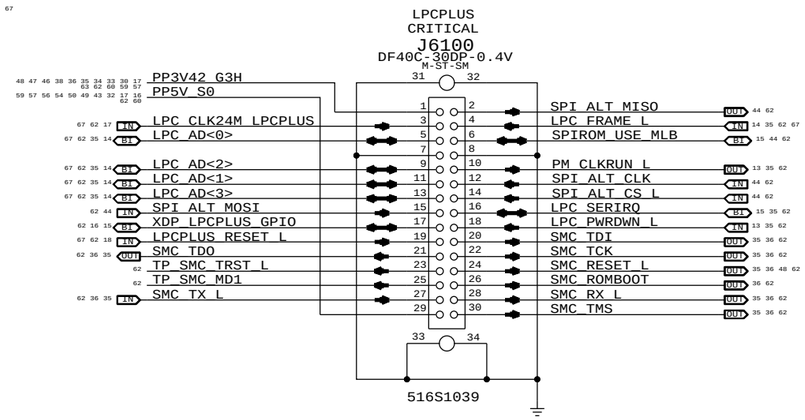
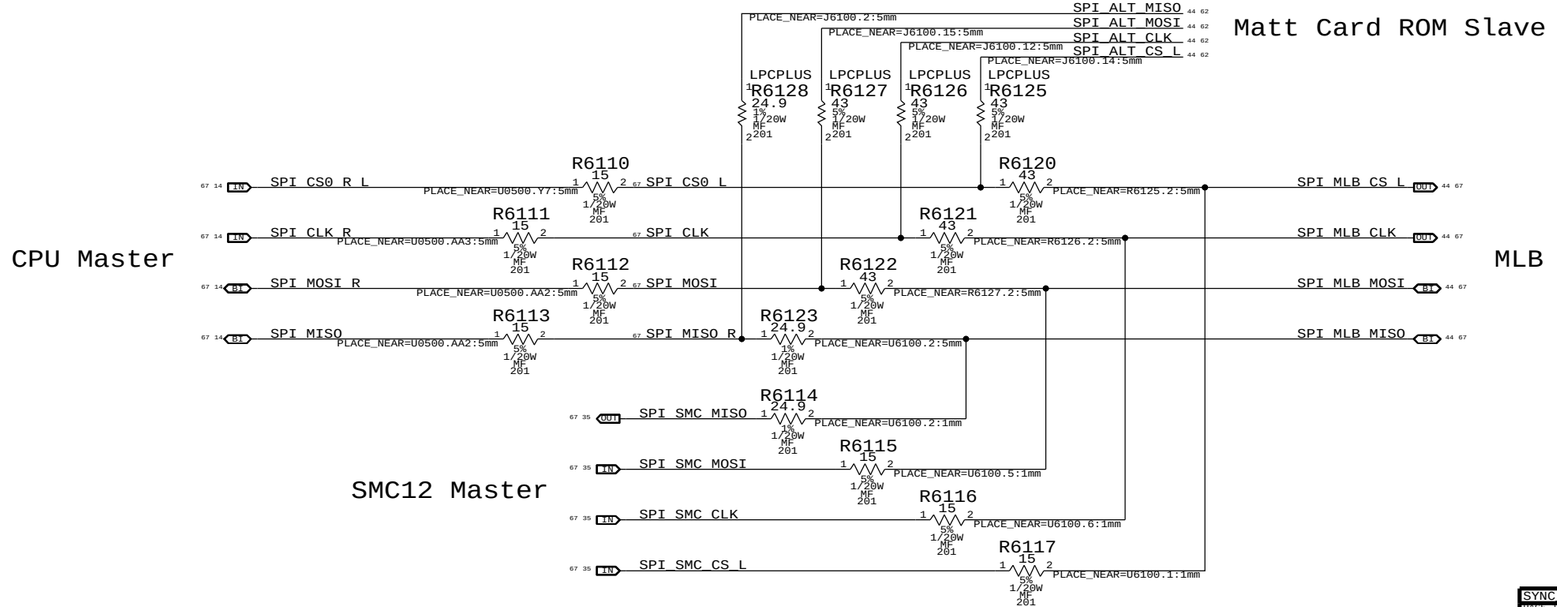


LPC+SPI Connector



SPI Bus Series Termination



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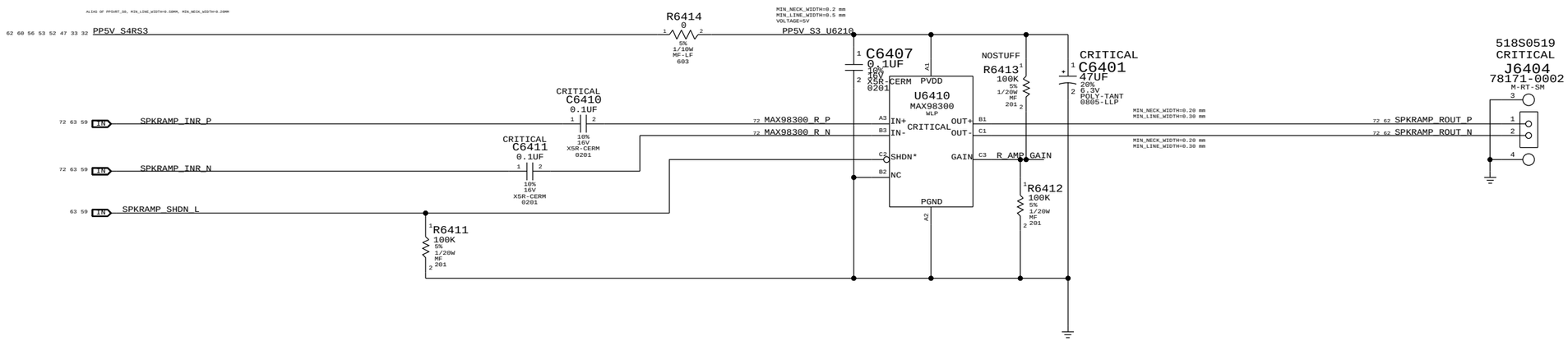
SPEAKER AMPLIFIERS

APN:353S2888

SPEAKER LOWPASS	80 HZ < FC < 132 HZ
GAIN	6DB

Right Speaker Connector



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SYNC_MASTER=J43_MLB SYNC_DATE=09/04/2012

PAGE TITLE
Audio: Speaker Amp

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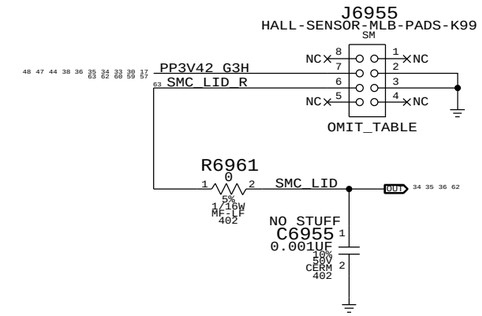
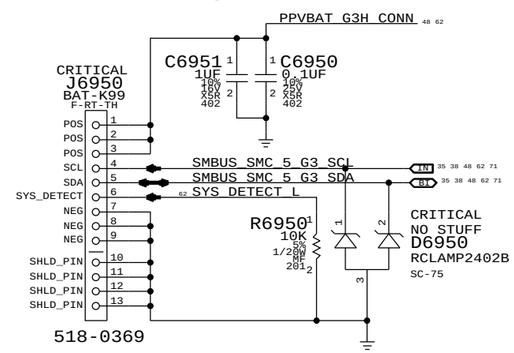
Hall Effect Sensor



11"-Specific Battery Connector



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SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Battery Connector & Hall Effect

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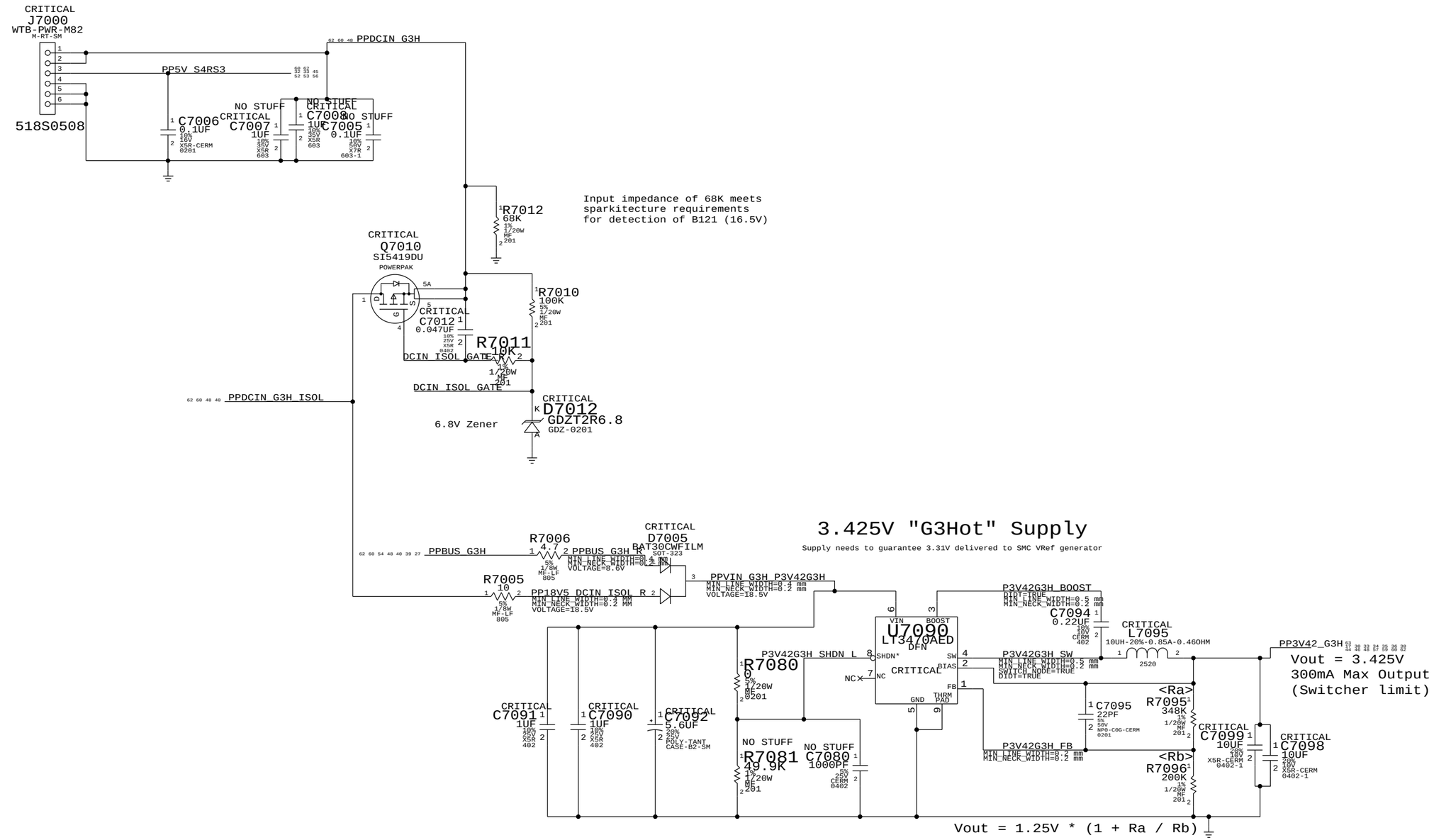
MLB to LIO Power Cable Connector



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SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE: DC-In & G3H Supply

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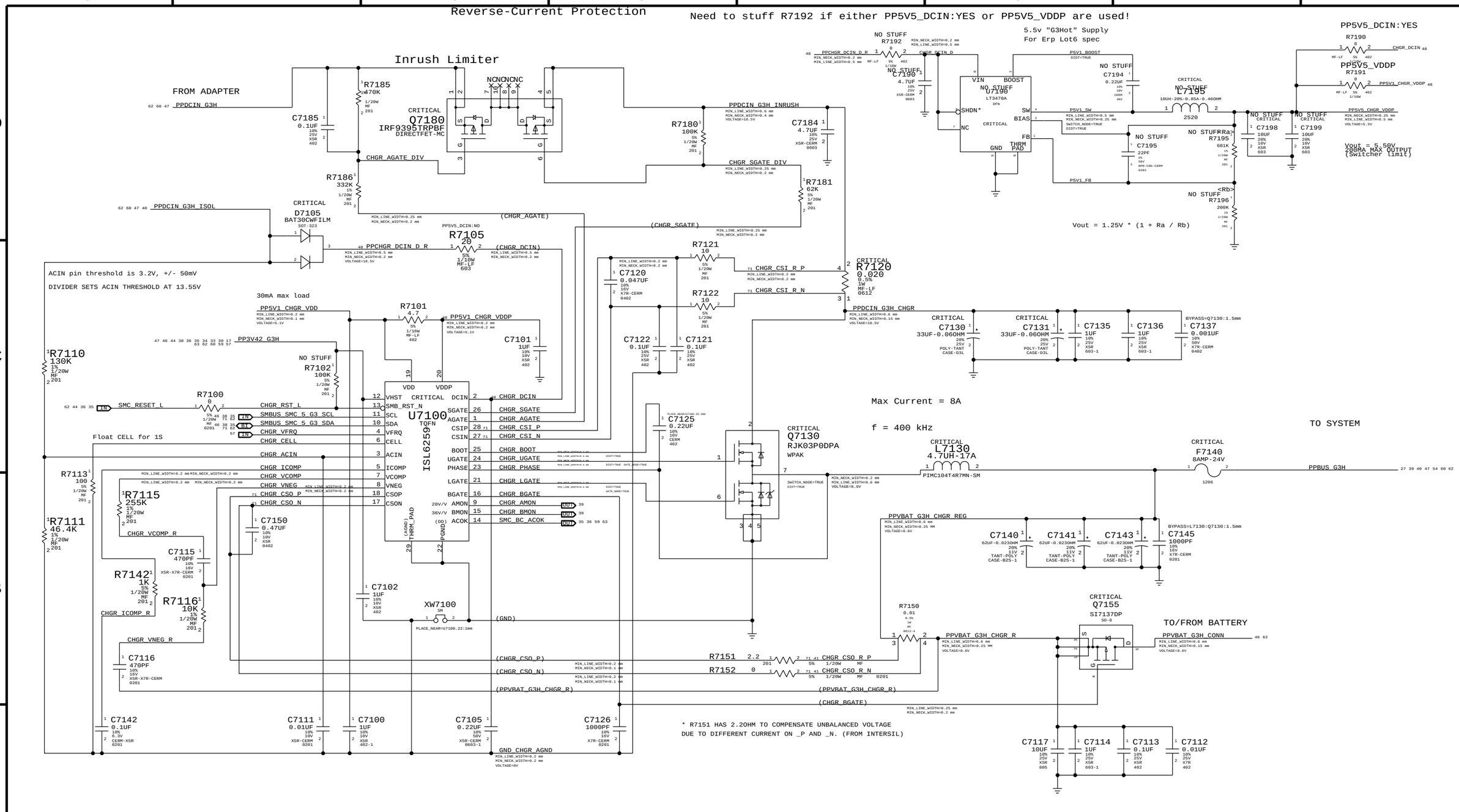

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

PAGE TITLE
PBus Supply & Battery Charger

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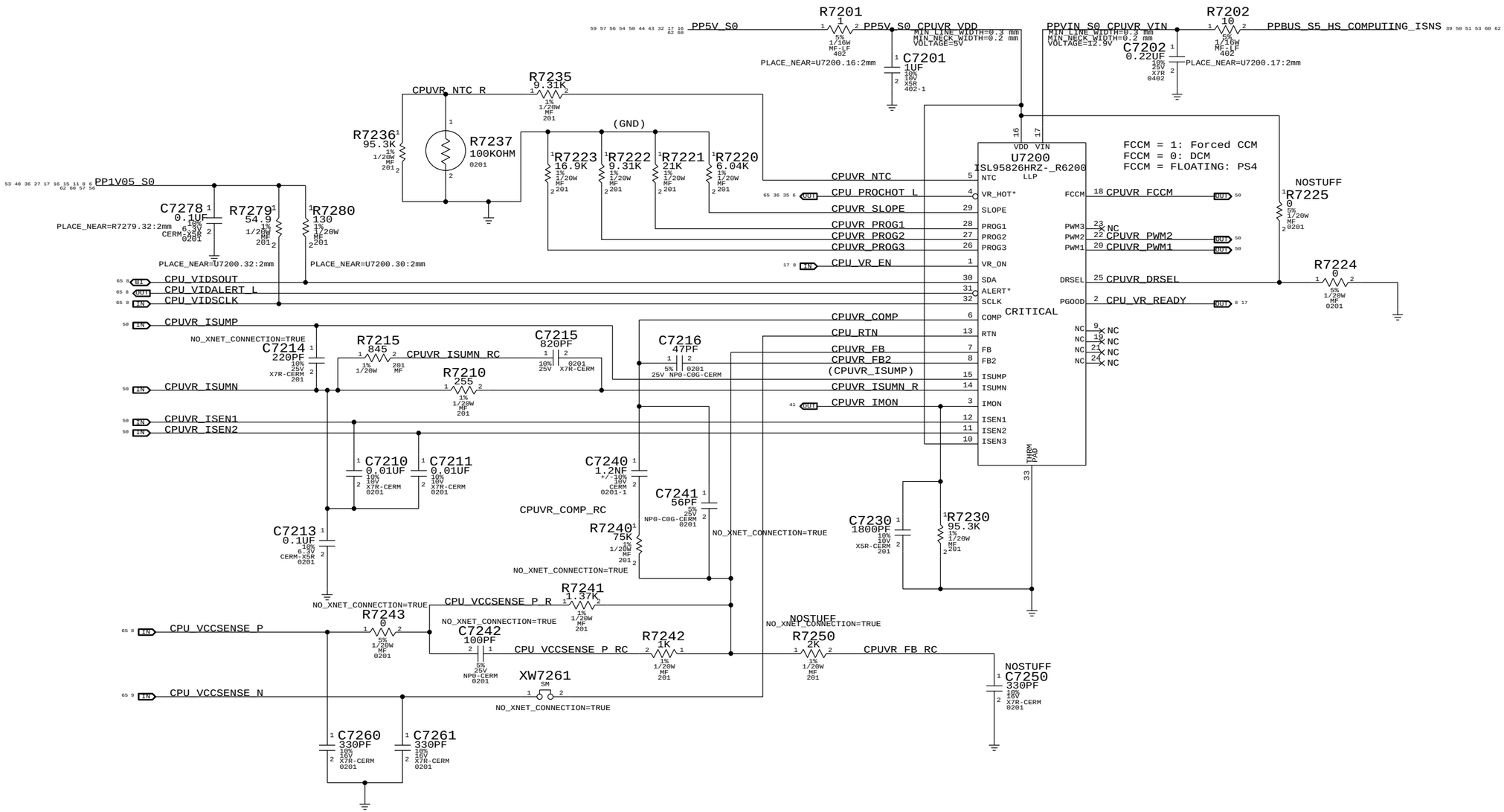

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Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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	PAGE: 72 OF 120
	SHEET: 49 OF 73

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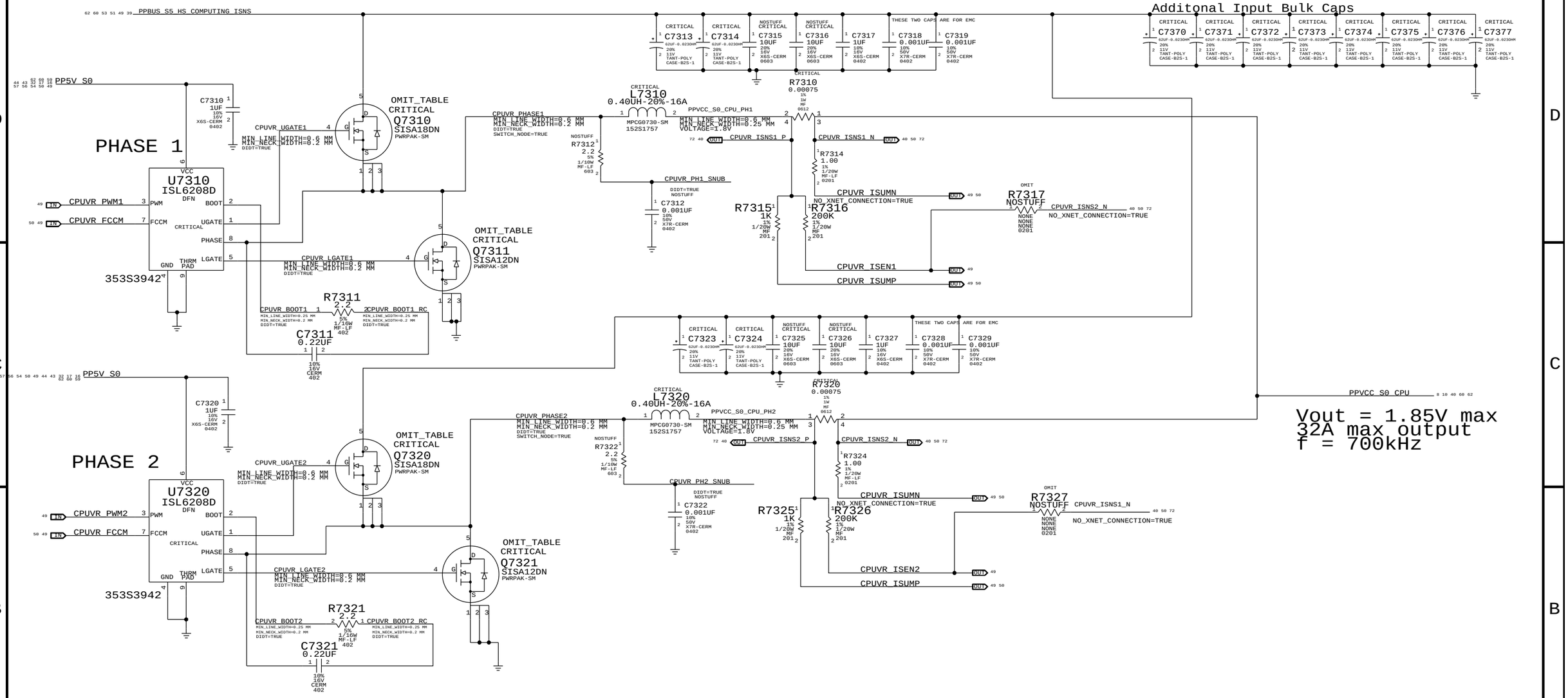

SYNC_MASTER=J43_MLB SYNC_DATE=09/21/2012

PAGE TITLE
CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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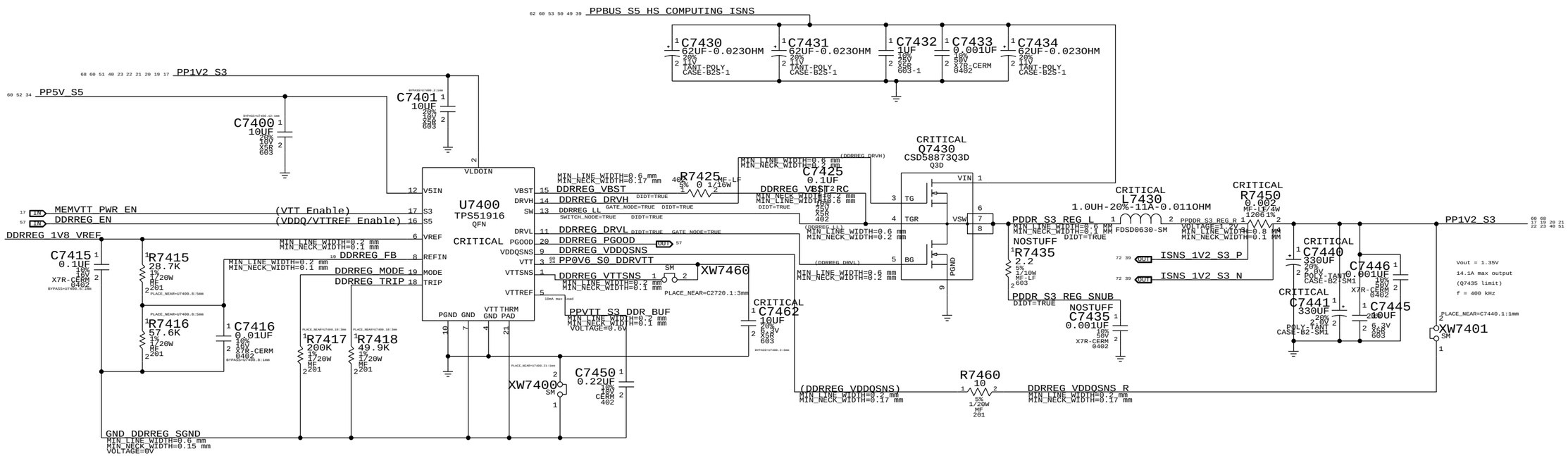

SYNC_MASTER=J43_MLB	SYNC_DATE=09/17/2012
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 74 OF 120
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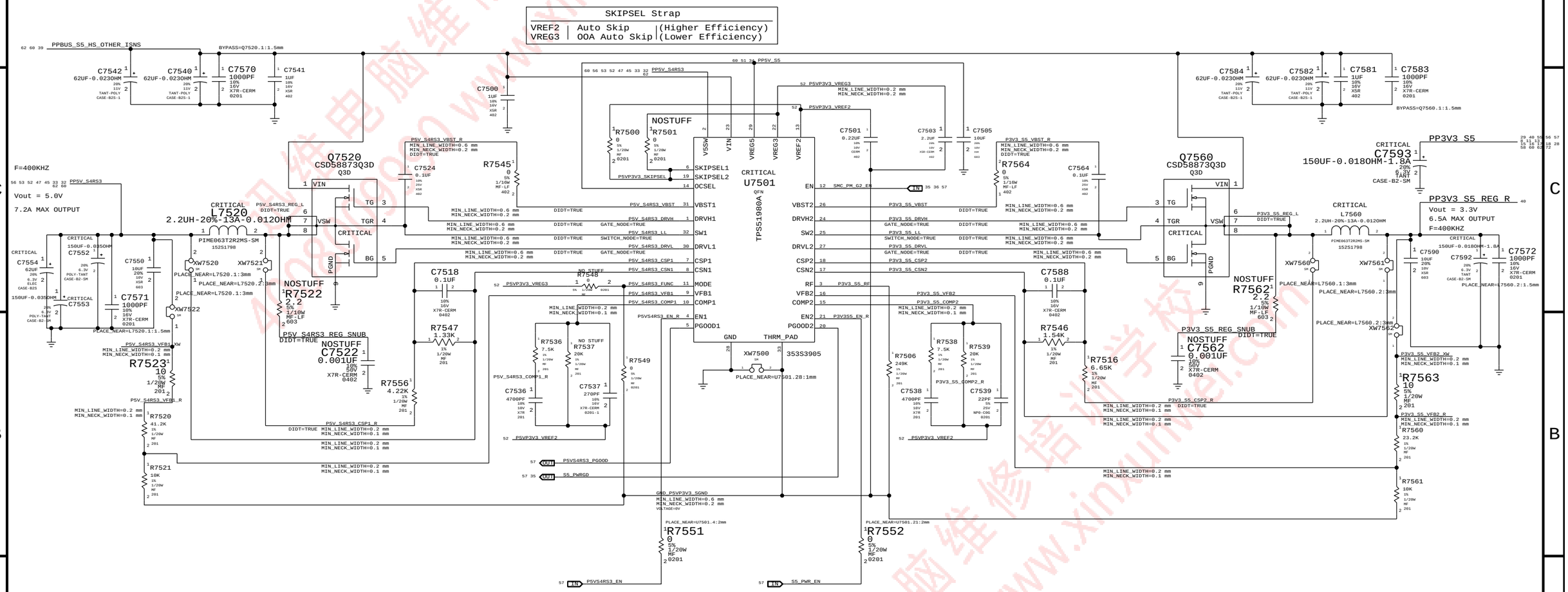

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SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
5V S4RS3 / 3.3V S5 Power Supply

Apple Inc.

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REVISION <E4LABEL>
BRANCH <BRANCH>
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SHEET 52 OF 73

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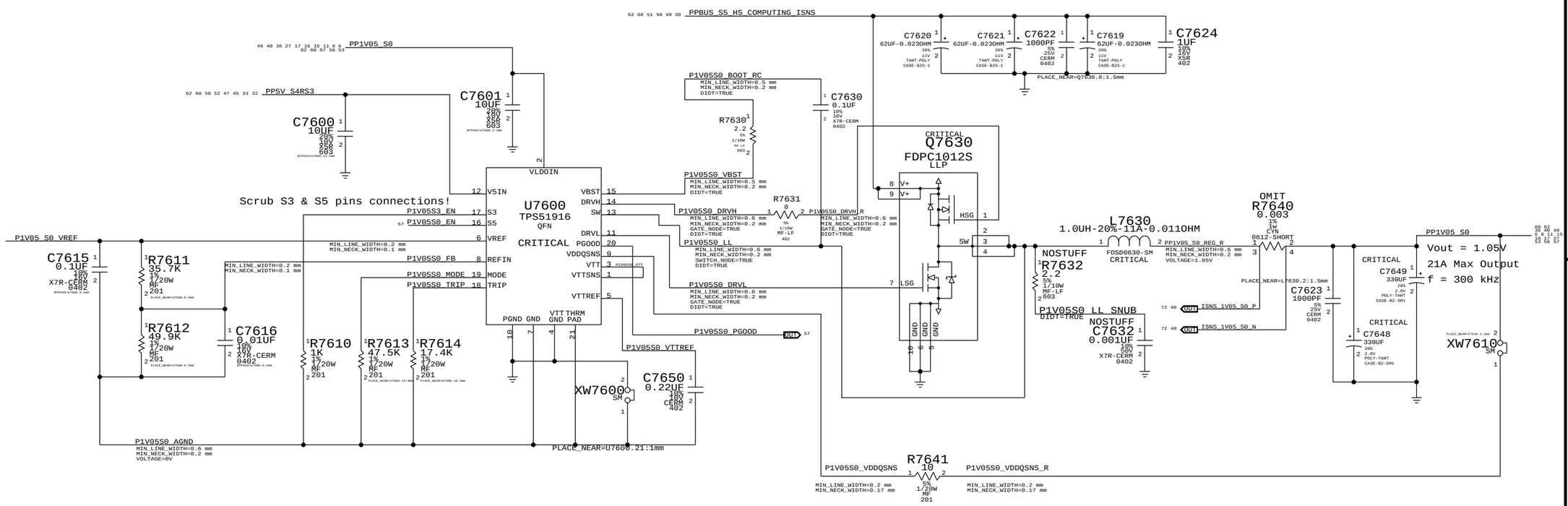
1.05V S0 Regulator



SYNC MASTER=J43_MLB	SYNC DATE=09/10/2012
PAGE TITLE: 1.05V S0 Power Supply	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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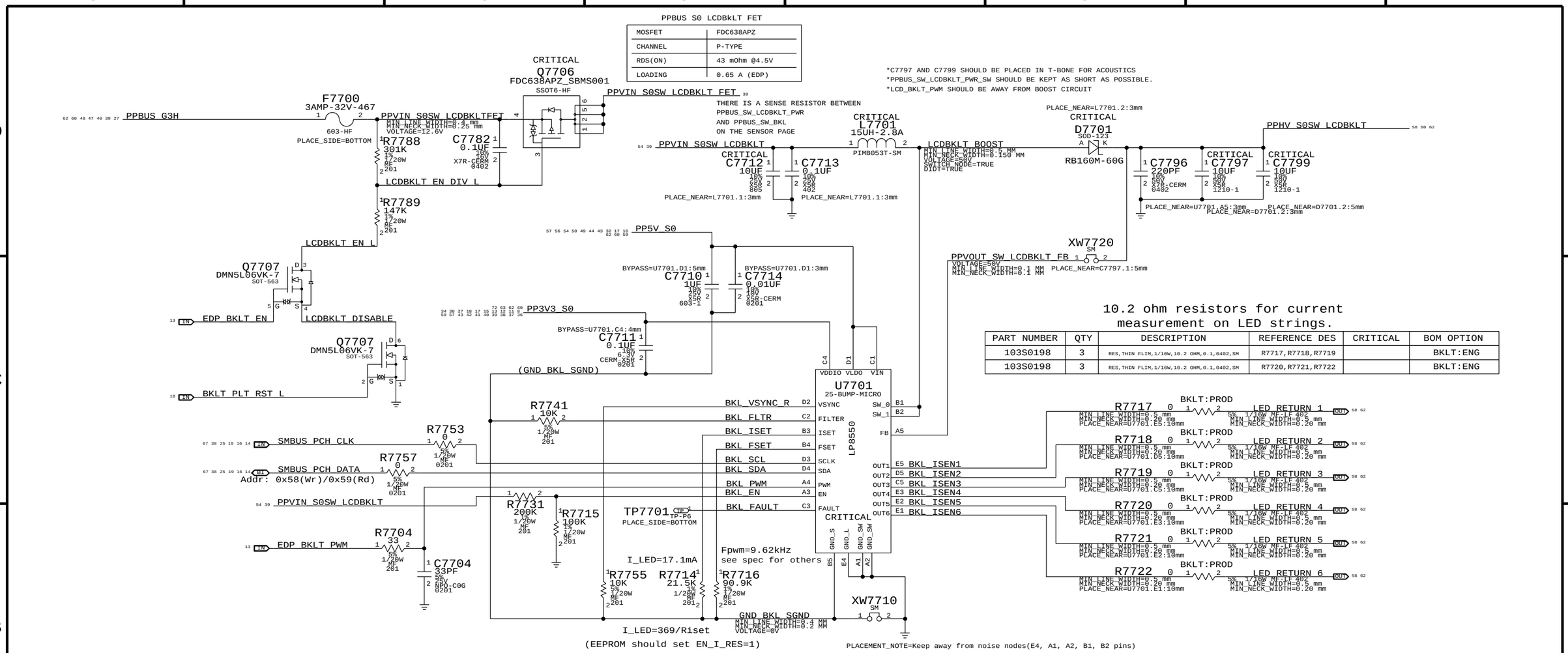

10.2 ohm resistors for current measurement on LED strings.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7717,R7718,R7719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R7720,R7721,R7722		BKLT:ENG

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SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE
LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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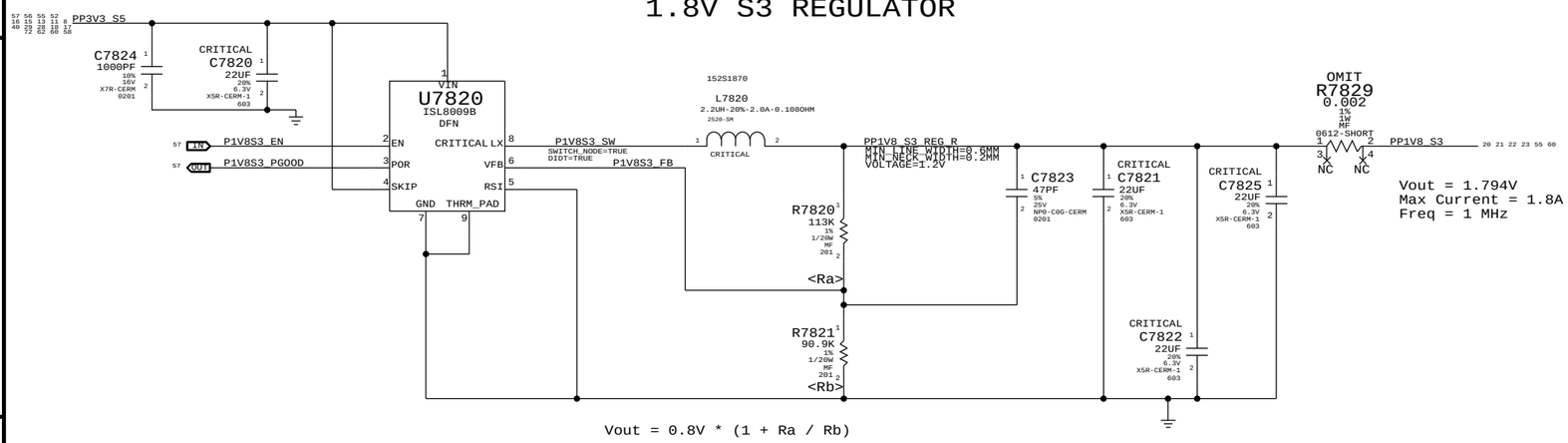
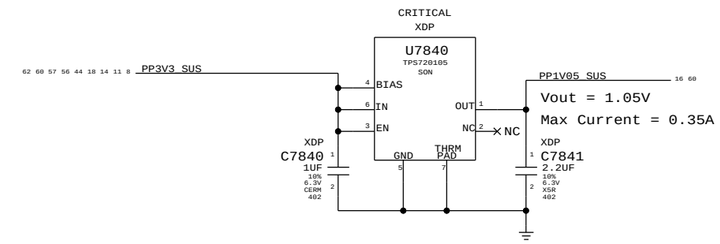
1.8V S3 REGULATOR

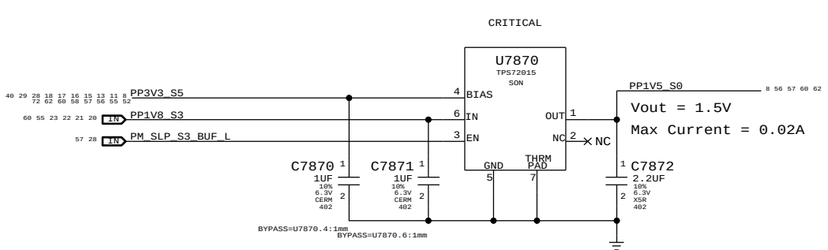


1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.



1.5V S0 LDO



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SYNC_MASTER=J43_MLB	SYNC_DATE=10/04/2012
PAGE TITLE: Misc Power Supplies	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
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	PAGE: 78 OF 120
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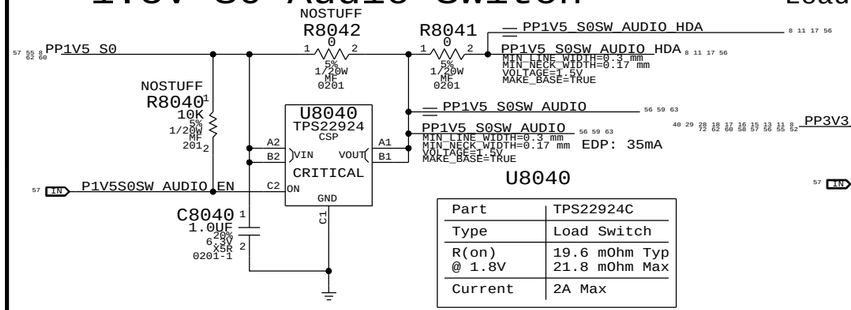
1.5V S0 Audio Switch

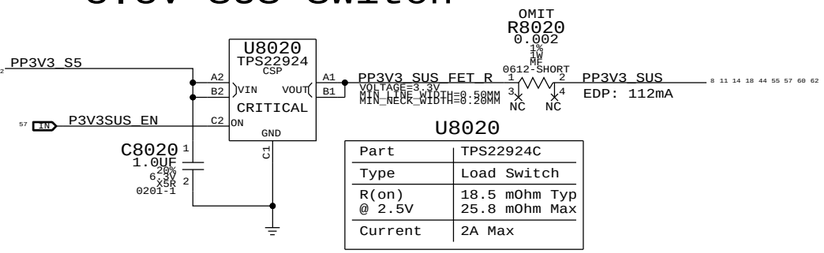
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

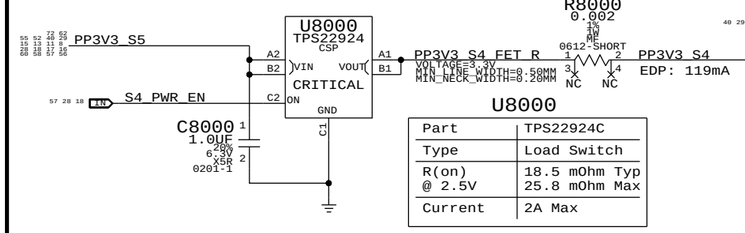
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

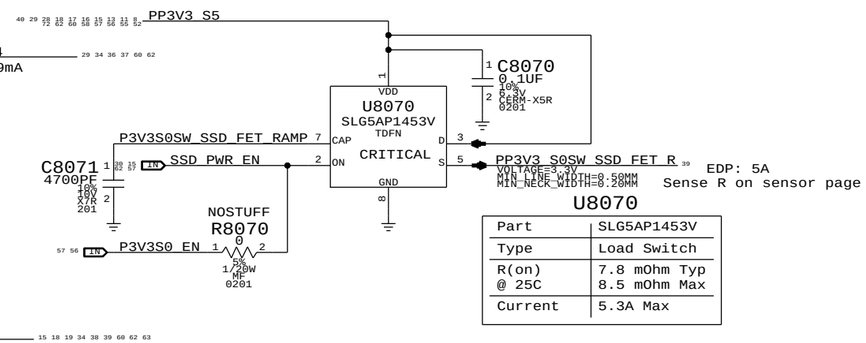
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

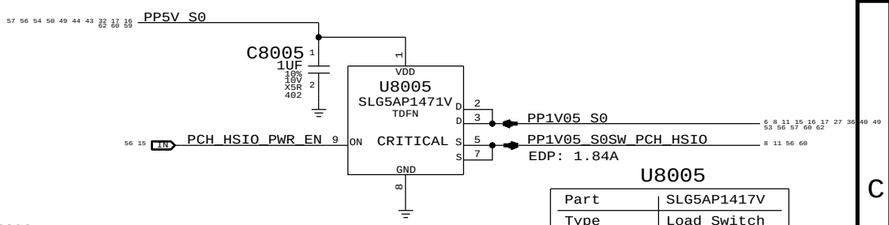
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

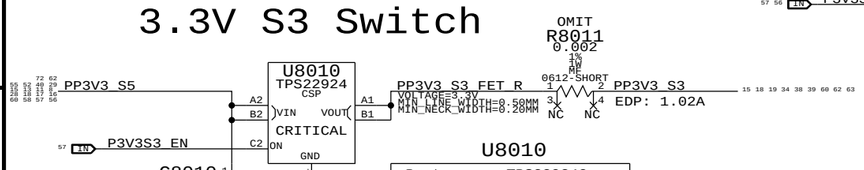


HSIO has turn-on requirement of <0.1V/uS ramp rate and <65uS from EN to 95% (1.05V)

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

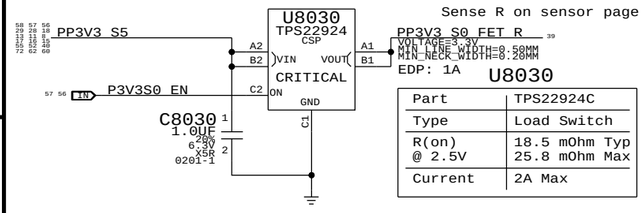
3.3V S3 Switch



U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

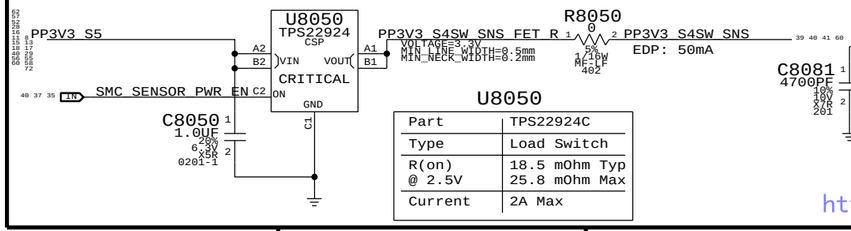
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

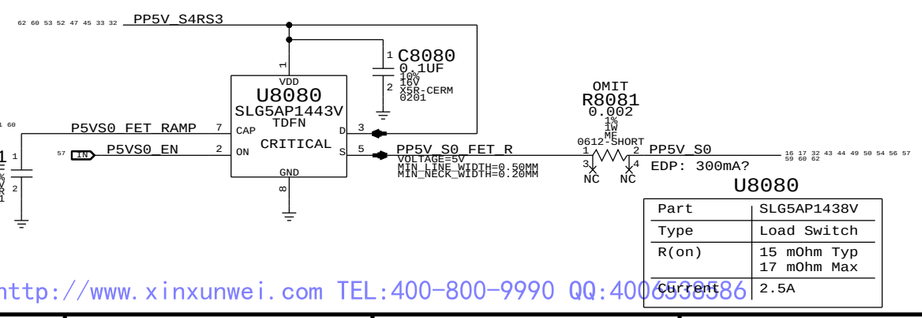
3.3V Sensor Switch



U8050

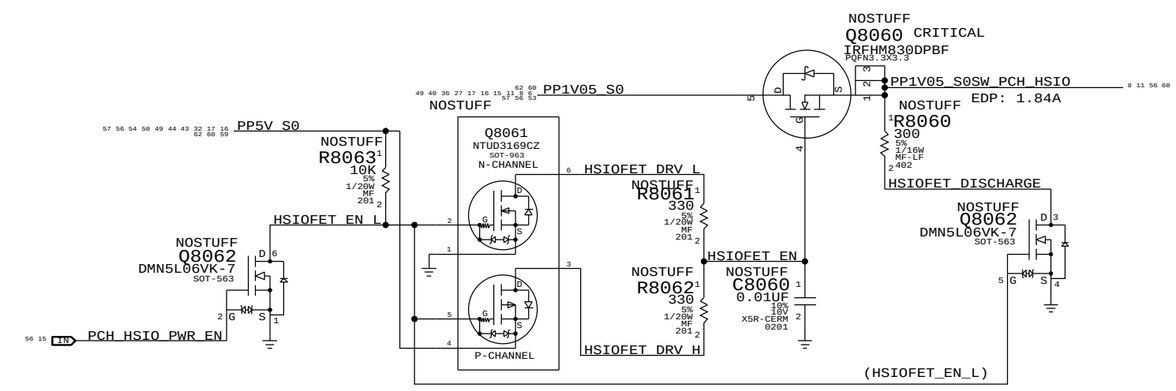
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A



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SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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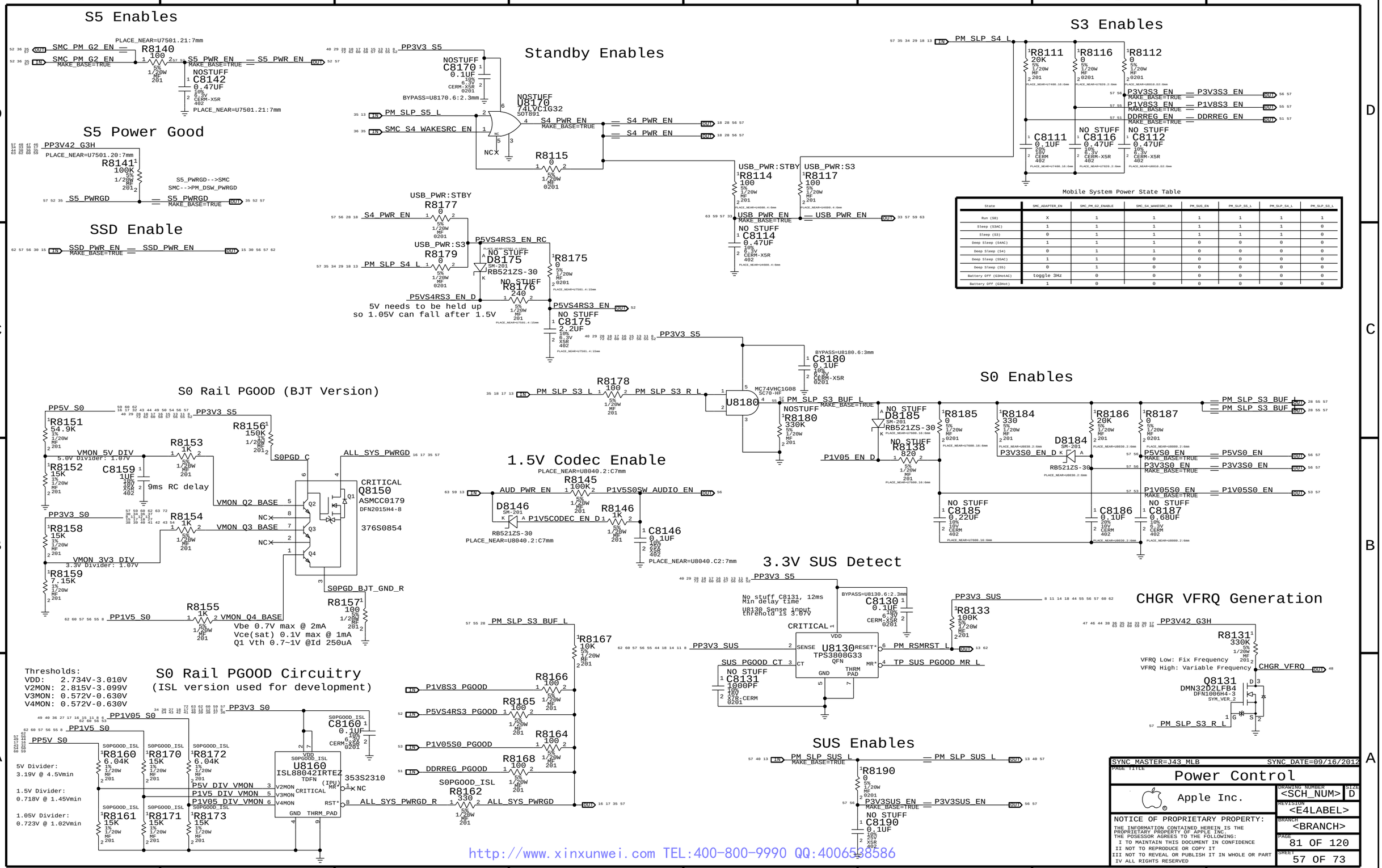

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

SYNC MASTER=J43_MLB SYNC DATE=09/16/2012

PAGE TITLE: Power Control

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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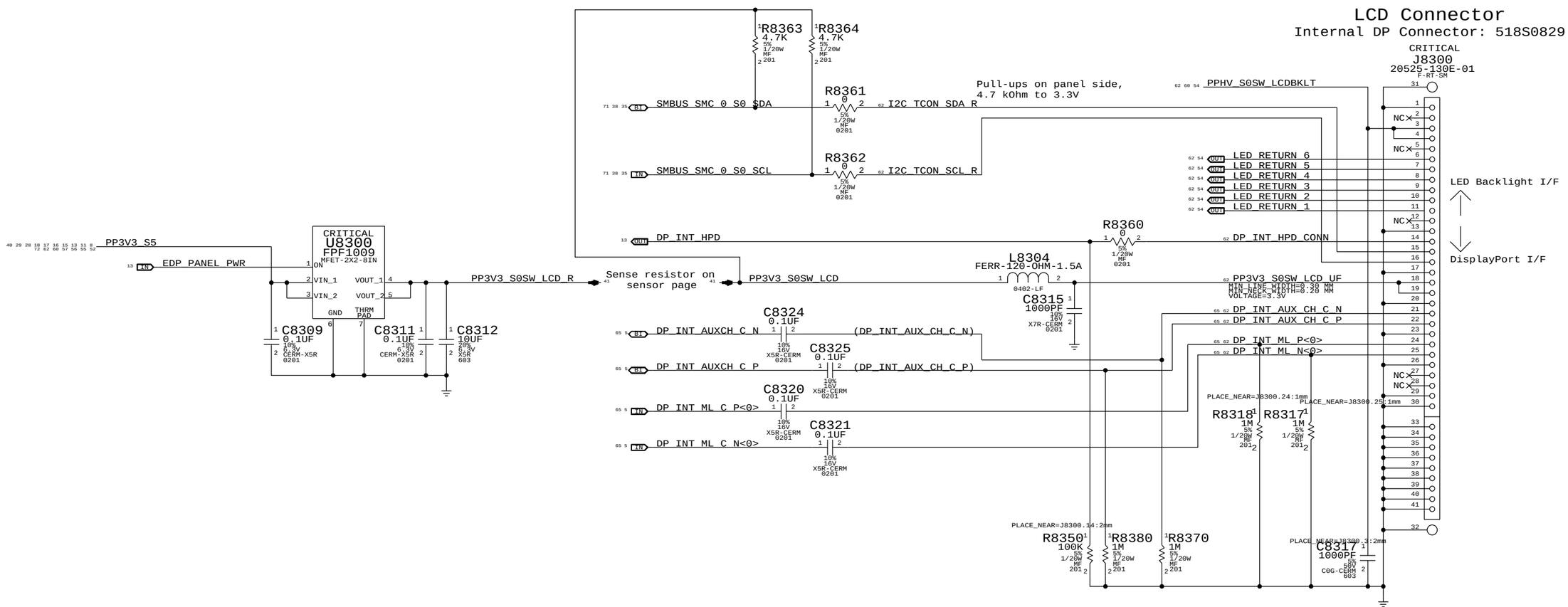

SYNC_MASTER=J43_MLB SYNC_DATE=09/11/2012

PAGE TITLE
Internal DisplayPort Connector

Apple Inc.

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REVISION <E4LABEL>

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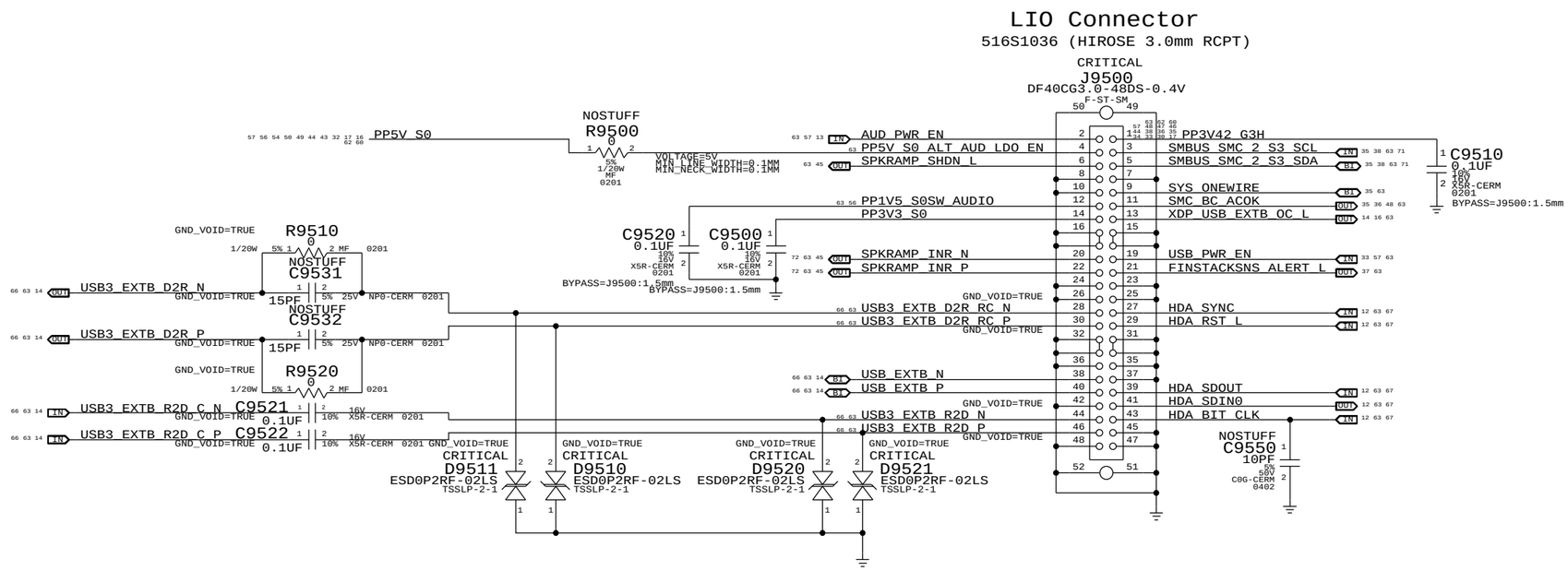

SYNC_MASTER=CLEAN_J41 SYNC_DATE=11/13/2012

PAGE TITLE
LIO Connector

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DRAWING NUMBER <SCH_NUM> SIZE D

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPBUS_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=8.6V
MAKE_BASE=TRUE

PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

PP3V42_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE

PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4RS3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

3.3V Rails

PP3V3_S5
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

PP3V3_S4
MIN_LINE_WIDTH=0.60MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE

PP3V3_SUS
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE

PP3V3_S3
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE

PP3V3_S0
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE

PP3V3_S4SW_SNS
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE

PP3V3_S0SW_SSD
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE

PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20 MM MAKE_BASE=TRUE

LCDBKLT Rail

PPHV_S0SW_LCDBKLT
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=50V
MAKE_BASE=TRUE

1.8V/1.5V/1.2V/1.05V Rails

PP1V8_S3
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

2A max supply

PP1V2_S3
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.2V
MAKE_BASE=TRUE

PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V5_S0
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

PP0V6_S0_DDRVTT
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

PP1V05_S0
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.175 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

? mA

PP1V05_S0SW_PCH_HSIO
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

1.84A

TBT Rails (off when no cable)

PP15V_TBT
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE

PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP1V05_TBTLC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PP1V05_TBTCIO
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVIN_S4SW_TBTBST_FET
VOLTAGE=8.6V

CPU "VCORE" RAILS

PPVCC_S0_CPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.075MM
MIN_LINE_WIDTH=0.6MM

SYNC MASTER=WILL J43 SYNC DATE=12/17/2012

PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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http://www.zhnxunwei.com TEL:400-800-9990 QQ:4006538586

LPDDR3 Command/Address

MAKE_BASE

7	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>	20 24 68	
7	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>	20 24 68	
7	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	20 24 68	
7	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	20 24 68	
7	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	20 24 68	
7	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	20 24 68	
68 61 24 20 7	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	7 20 24 61 68	
7	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	20 24 68	
7	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	20 24 68	
7	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	20 24 68	
7	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	21 24 68	
7	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	21 24 68	
7	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	21 24 68	
7	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	21 24 68	
7	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	21 24 68	
7	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	21 24 68	
68 61 24 21 7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	7 21 24 61 68	
7	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	21 24 68	
7	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	21 24 68	
7	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	21 24 68	
68 61 24 21 20 7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	7 20 21 24 61 68	
61 7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	7 61	
61 7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	7 61	
7	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	22 24 68	
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68 61 24 22 7	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	7 22 24 61 68	
7	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>	22 24 68	
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7	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	23 24 68	
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68 61 24 23 7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	7 23 24 61 68	
7	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	23 24 68	
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68 61 24 23 22 7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	7 22 23 24 61 68	
61 7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	7 61	
61 7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	7 61	

Memory Bit/Byte Swizzle

MAKE_BASE

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68 61 21 7	MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>	7 21 61 68	
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68 61 21 7	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	7 21 61 68	
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MAKE_BASE

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68 61 23 7	MEM_B_DQ<32>	TRUE	MEM_B_DQ<32>	7 23 61 68	
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68 61 23 7	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	7 23 61 68	
68 61 23 7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	7 23 61 68	

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
Signal Aliases

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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Functional Test Points

J3501: AirPort / BT Connector

FUNC_TEST

TRUE	PP3V3_WLAN	(Need 6 TPs)	29 35 36 37 39
TRUE	WIFI_EVENT_L		29 35 36
TRUE	PCIE_AP_R2D_N		29 67
TRUE	PCIE_AP_R2D_P		29 67
TRUE	PCIE_CLK100M_AP_N		12 29 67
TRUE	PCIE_CLK100M_AP_P		12 29 67
TRUE	PCIE_AP_D2R_P		14 29 67
TRUE	PCIE_AP_D2R_N		14 29 67
TRUE	PCIE_WAKE_L		13 29 31
TRUE	AP_RESET_CONN_L		29
TRUE	AP_CLKREQ_Q_L		29
TRUE	USB_BT_CONN_P		29 66
TRUE	USB_BT_CONN_N		29 66
TRUE	PP3V3_S4		29 34 36 37 56 60 62

(Need to add 8 GND TPs)

J3700: SSD Connector

FUNC_TEST

TRUE	PP3V3_S0SW_SSD_FLT	(Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>		30 65
TRUE	PCIE_SSD_R2D_P<3..0>		30 65
TRUE	PP3V3_S0		40 41 42 43 54 57 59 60 61 12 13 15 17 18 27 30 34 36 37 38 39 60 62 63 72
TRUE	SSD_RESET_CONN_L		30
TRUE	SSD_CLKREQ_CONN_L		30
TRUE	SMC_OOB1_R2D_CONN_L		30
TRUE	SMC_OOB1_D2R_CONN_L		30
TRUE	SSD_PCIE_SEL_L		16 30
TRUE	SSD_DEVSLP		15 30
TRUE	SSD_PWRFAIL_WARN_L		
TRUE	SSD_PWR_EN		15 30 56 57
TRUE	PCIE_SSD_D2R_N<3..0>		12 30 65
TRUE	PCIE_SSD_D2R_P<3..0>		12 30 65
TRUE	PCIE_CLK100M_SSD_N		12 30 65
TRUE	PCIE_CLK100M_SSD_P		12 30 65

(Need to add 6 GND TPs)

J4002: Camera Connector

FUNC_TEST

TRUE	MIPI_CLK_CONN_N		32 70
TRUE	MIPI_CLK_CONN_P		32 70
TRUE	CAM_SENSOR_WAKE_L_CONN		32
TRUE	MIPI_DATA_CONN_N		32 70
TRUE	MIPI_DATA_CONN_P		32 70
TRUE	SMBUS_SMC_1_S0_SDA		14 32 35 38 41 42 67 71
TRUE	SMBUS_SMC_1_S0_SCL		14 32 35 38 41 42 67 71
TRUE	I2C_CAM_SCK		31 32
TRUE	I2C_CAM_SDA		31 32
TRUE	PP5V_S3RS0_ALSCAM_F	(Need TBD TPs)	32

(Need to add TBD GND TPs)

J6100: LPC+SPI Connector

FUNC_TEST

TRUE	PP3V42_G3H		62 63 17 30 33 34 39 46 38 44 46 47 48 57 59 60
TRUE	PP5V_S0		16 17 32 43 44 49 54 54 56 57 59 60 62
TRUE	LPC_CLK24M_LPCPLUS		17 44 67
TRUE	LPC_AD<3..0>		14 35 44 67
TRUE	SPI_ALT_MOSI		44
TRUE	XDP_LPCPLUS_GPIO		15 16 44
TRUE	LPCPLUS_RESET_L		18 44 67
TRUE	SMC_TDO		35 36 44
TRUE	TP_SMC_TRST_L		44
TRUE	TP_SMC_MD1		44
TRUE	SMC_TX_L		35 36 44
TRUE	SPI_ALT_MISO		44
TRUE	LPC_FRAME_L		14 35 44 67
TRUE	SPIROM_USE_MLB		15 44
TRUE	PM_CLKRUN_L		13 35 44
TRUE	SPI_ALT_CLK		44
TRUE	SPI_ALT_CS_L		44
TRUE	LPC_SERIRQ		15 35 44
TRUE	LPC_PWRDWN_L		13 35 44
TRUE	SMC_TDI		35 36 44
TRUE	SMC_TCK		35 36 44
TRUE	SMC_RESET_L		35 36 44 48
TRUE	SMC_ROMBOOT		36 44
TRUE	SMC_RX_L		35 36 44
TRUE	SMC_TMS		35 36 44

(Need to add 6 GND TPs)

J6000: Fan Connector

FUNC_TEST

TRUE	PP5V_S0		16 17 32 43 44 49 50 54 56 57 59 60 62
TRUE	FAN_RT_TACH		43
TRUE	FAN_RT_PWM		43

(Need to add 1 GND TP)

J4800: IPD Flex Connector

FUNC_TEST

TRUE	SMC_LID		34 35 36 46
TRUE	TPAD_SPI_MISO_R		34
TRUE	USB_TPAD_P		14 34 66
TRUE	USB_TPAD_N		14 34 66
TRUE	TPAD_SPI_CLK_R		34
TRUE	TPAD_WAKE_L		34
TRUE	TPAD_SPI_MOSI_R		34
TRUE	PP3V3_S4_IPD		34
TRUE	TPAD_SPI_CS_R_L		34
TRUE	TPAD_SPI_IF_EN_CONN		34
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN		34
TRUE	PP5V_S4_IPD		34
TRUE	TPAD_USB_IF_EN_CONN		34
TRUE	SMBUS_SMC_3_SDA		34 35 38 42 71
TRUE	SMBUS_SMC_3_SCL		34 35 38 42 71
TRUE	SMC_LSOC_RST_L		34 36
TRUE	PP3V42_G3H		17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMC_ONOFF_L		34 35 36

(Need to add 5 GND TPs)

J7000: DC-In Connector

FUNC_TEST

TRUE	PPDCIN_G3H	(Need 4 TPs)	47 48 60 62
TRUE	PP5V_S4RS3	(Need 3 TPs)	32 33 45 47 52 53 56 60

(Need to add 5 GND TPs)

J6404: Speaker Connector

FUNC_TEST

TRUE	SPKRAMP_ROUT_P		45 72
TRUE	SPKRAMP_ROUT_N		45 72

(Need to add 3 GND TPs)

J6950: Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	(Need 4 TPs)	46 48
TRUE	SMBUS_SMC_5_G3_SCL		35 38 46 48 71
TRUE	SMBUS_SMC_5_G3_SDA		35 38 46 48 71
TRUE	SYS_DETECT_L		46

(Need to add 4 GND TPs near J7050 and 1 for shield)

J8300: Internal DP Connector

FUNC_TEST

TRUE	PPHV_S0SW_LCDBKLT	(Need 2 TPs)	54 58 60
TRUE	LED_RETURN_6		54 58
TRUE	LED_RETURN_5		54 58
TRUE	LED_RETURN_4		54 58
TRUE	LED_RETURN_3		54 58
TRUE	LED_RETURN_2		54 58
TRUE	LED_RETURN_1		54 58
TRUE	DP_INT_HPD_CONN		58
TRUE	I2C_TCON_SDA_R		58
TRUE	I2C_TCON_SCL_R		58
TRUE	PP3V3_S0SW_LCD_UF	(Need 2 TPs)	58
TRUE	DP_INT_AUX_CH_C_N		58 65
TRUE	DP_INT_AUX_CH_C_P		58 65
TRUE	DP_INT_ML_P<0>		58 65
TRUE	DP_INT_ML_N<0>		58 65

(Need to add 5 GND TPs)

J7715: KB BKLT Connector

FUNC_TEST

TRUE	KBDLED_ANODE		54
TRUE	KBDLED_FB		54

(Need to add 2 GND TPs)

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC_TEST

1776	TRUE	XDP_CPU_TCK	6 16 65
1777	TRUE	XDP_PCH_TCK	12 16 67
1778	TRUE	XDP_CPU_TDI	6 16 65
1779	TRUE	XDP_CPU_TDO	6 16 65
1780	TRUE	XDP_CPUPCH_TRST_L	6 12 16 65
1781	TRUE	XDP_CPU_TMS	6 16 65
1782	TRUE	XDP_PCH_TMS	12 16 67
1783	TRUE	XDP_PCH_TDI	12 16 67
1784	TRUE	XDP_PCH_TDO	12 16 67
1785	TRUE	XDP_CPU_PREQ_L	6 16 65
1786	TRUE	XDP_CPU_PRDY_L	6 16 65
1787	TRUE	XDP_CPU_VCCST_PWRGD	16
1788	TRUE	PM_RSMRST_L	13 57
1789	TRUE	XDP_SYS_PWROK	16
1790	TRUE	PM_SYSRST_L	13 17 35
1791	TRUE	CPU_CFG<3>	6 16 65
1792	TRUE	PP1V05_S0	6 8 11 15 16 17 27 36 40 49 53 56 57 60 62

(Need to add 2 GND TPs)

1793 TRUE GND

Misc Voltages & Control Signals

FUNC_TEST

TRUE	PPBUS_G3H		27 39 40 47 48 54 60
TRUE	PPVIN_S4SW_TBTBST_FET		27 60
TRUE	PPBUS_S5_HS_COMPUTING_ISNS		39 49 50 51 53 60
TRUE	PPDCIN_G3H		47 48 60 62
TRUE	PP3V42_G3H		17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	PPVRTC_G3H		8 12 13 17 60
TRUE	PP3V3_S5		8 11 13 15 16 17 18 28 29 40 52 56 58 57 58 60 72
TRUE	PP3V3_SUS		8 11 14 18 44 55 56 57 60
TRUE	PP3V3_S3		15 18 19 34 38 39 56 60 63 60 62 63 72
TRUE	PP3V3_S0		8 12 13 15 16 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	PP3V3_S0SW_SSD		30 39 60
TRUE	PP1V5_S0		8 55 56 57 60
TRUE	PP1V05_S0		6 8 11 15 16 17 27 36 40 49 53 56 57 60 62
TRUE	PP15V_TBT		27 28 60
TRUE	PP3V3_TBTLC		15 17 25 26 27 60
TRUE	PP1V05_TBTLC		26 27 60
TRUE	PPVCC_S0_CPU		8 10 40 50 60
TRUE	PP1V05_TBTCIO		26 27 60
TRUE	PPBUS_S5_HS_OTHER_ISNS		39 52 60
TRUE	PPDCIN_G3H_ISOL		40 47 48 60
TRUE	PP3V3_S4		29 34 36 37 56 60 62

(Need to add 27 GND TPs)

NO_TEST Nets

		NO_TEST	MAKE_BASE			
62	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	62	CPU/PCH
62	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	62	CPU/PCH
62 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 62	CPU/PCH
62 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 62	CPU/PCH
62 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14 62	CPU/PCH
62 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14 62	CPU/PCH
62 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14 62	CPU/PCH
62 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14 62	CPU/PCH
62 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 62	CPU/PCH
62 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 62	CPU/PCH
62 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 62	CPU/PCH
62 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 62	CPU/PCH
62 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 62	CPU/PCH
62 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 62	CPU/PCH
65	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	5	CPU/PCH
65	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	5	CPU/PCH
62 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 62	CPU/PCH
62 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 62	CPU/PCH
62 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 62	CPU/PCH
62 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 62	CPU/PCH
62 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 62	CPU/PCH
62 35	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	35 62	SMC
62	NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC	62	SMC
62	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	62	SMC
62	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	62	SMC
62 35	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	35 62	SMC
62 35	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	35 62	SMC
62 35	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	35 62	SMC
62 35	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	35 62	SMC
62 35	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	35 62	SMC
62	NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO	62	SMC
62	NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR	62	SMC
62	NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG	62	SMC
62 35	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	35 62	SMC
62 35	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	35 62	SMC
62 35	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	35 62	SMC
62 35	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	35 62	SMC
62 35	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	35 62	SMC
69	TBT_B_R2D_C_P<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CP<1..0>	25	TBT
69	TBT_B_R2D_C_N<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CN<1..0>	25	TBT
69	TBT_B_D2R_P<1..0>	TRUE	TRUE	NC_TBT_B_D2RP<1..0>	25	TBT
69	TBT_B_D2R_N<1..0>	TRUE	TRUE	NC_TBT_B_D2RN<1..0>	25	TBT
62 25	NC_TBT_B_LSTX	TRUE	TRUE	NC_TBT_B_LSTX	25 62	TBT
69 62	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	62 69	TBT
69 62	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	62 69	TBT
69 62 25	NC_DP_TBTPB_AUXCH_CP	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CP	25 62 69	TBT
69 62 25	NC_DP_TBTPB_AUXCH_CN	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CN	25 62 69	TBT
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3>		TBT
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3>		TBT
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<2>		TBT
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<2>		TBT
62 25	NC_DP_TBTSRC_ML_CP<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<1>	25 62	TBT
62 25	NC_DP_TBTSRC_ML_CN<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<1>	25 62	TBT
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<0>		TBT
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<0>		TBT
62 25	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	25 62	TBT
62 25	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	25 62	TBT

Unused nets with offpage

(Nets with offpages not used on this project)

HDD_PWR_EN	15
WOL_EN	14
BT_PWRRST_L	15
HDMITBTMUX_FLAG_L	15
FW_PWR_EN	15
FW_PME_L	15
ENET_MEDIA_SENSE	15
LCD_PSR_EN	15
LCD_IRQ_L	15
ODD_PWR_EN_L	13
ENET_LOW_PWR	13
AUD_IP_PERIPHERAL_DET	13
AUD_I2C_INT_L	13
AUD_IPHS_SWITCH_EN	13

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

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Functional Test Points

J9500: LIO Connector

FUNC_TEST			
TRUE	AUD_PWR_EN	13 57 59	
TRUE	PP5V_S0_ALT_AUD_LDO_EN	59	
TRUE	SPKRAMP_SHDN_L	45 59	
TRUE	PP1V5_S0SW_AUDIO	56 59	
TRUE	PP3V3_S0	60 62 72 5 11 12 13 15 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59	
TRUE	SPKRAMP_INR_N	45 59 72	
TRUE	SPKRAMP_INR_P	45 59 72	
TRUE	USB3_EXTB_D2R_RC_N	59 63 66	
TRUE	USB3_EXTB_D2R_RC_P	59 63 66	
TRUE	USB_EXTB_N	14 59 66	
TRUE	USB_EXTB_P	14 59 66	
TRUE	USB3_EXTB_R2D_N	59 63 66	
TRUE	USB3_EXTB_R2D_P	59 63 66	
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63	
TRUE	SMBUS_SMC_2_S3_SCL	35 38 59 71	
TRUE	SMBUS_SMC_2_S3_SDA	35 38 59 71	
TRUE	SYS_ONEWIRE	35 59	
TRUE	SMC_BC_ACOK	35 36 48 59	
TRUE	XDP_USB_EXTB_OC_L	14 16 59	
TRUE	USB_PWR_EN	33 57 59	
TRUE	FINSTACKSNS_ALERT_L	37 59	
TRUE	HDA_SYNC	12 59 67	
TRUE	HDA_RST_L	12 59 67	
TRUE	HDA_SDOUT	12 59 67	
TRUE	HDA_SDIN0	12 59 67	
TRUE	HDA_BIT_CLK	12 59 67	

(Need to add 5 GND TPs)

J6955: HALL EFFECT Connector

FUNC_TEST		
TRUE	SMC_LID_R	46
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63

Power Aliases

63 62 60 56 39 38 34 19 18 15 PP3V3_S3 = PP3V3_S3 15 18 19 34 38 39 56 60 62 63

NO_TEST Nets

		NO_TEST	MAKE_BASE			
66 63 14	NC_USB3RPCIE_SD_D2RP	=	TRUE	TRUE	NC_USB3RPCIE_SD_D2RP	14 63 66
66 63 14	NC_USB3RPCIE_SD_D2RN	=	TRUE	TRUE	NC_USB3RPCIE_SD_D2RN	14 63 66
66 63 14	NC_USB3RPCIE_SD_R2D_CP	=	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CP	14 63 66 CPU/PCH
66 63 14	NC_USB3RPCIE_SD_R2D_CN	=	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CN	14 63 66
63 37 35	NC_SMC_ADC16	=	TRUE	TRUE	NC_SMC_ADC16	35 63 37 SMC

Bead Probes

66 59 14	USB3_EXTB_D2R_N	1	SM	BEAD-PROBE BPA511
66 59 14	USB3_EXTB_D2R_P	1	SM	BEAD-PROBE BPA510
66 63 59	USB3_EXTB_D2R_RC_N	1	SM	BEAD-PROBE BPA520
66 63 59	USB3_EXTB_D2R_RC_P	1	SM	BEAD-PROBE BPA521
66 59 14	USB3_EXTB_R2D_C_N	1	SM	BEAD-PROBE BPA513
66 59 14	USB3_EXTB_R2D_C_P	1	SM	BEAD-PROBE BPA512
66 63 59	USB3_EXTB_R2D_N	1	SM	BEAD-PROBE BPA523
66 63 59	USB3_EXTB_R2D_P	1	SM	BEAD-PROBE BPA522

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L 15
XDP_SDCONN_STATE_CHANGE_L 15 16
SD_PWR_EN 15

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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Project FCT/NC/Aliases

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J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2,ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4,ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.110 MM	0.110 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL3,ISL10	Y	0.105 MM	0.105 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110MM		0.095 MM	0.095 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL3,ISL10	Y	0.070 MM	0.070 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL4,ISL9	Y	0.076 MM	0.076 MM		0.180 MM	0.180 MM
90_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL2,ISL11	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL3,ISL10	Y	0.106 MM	0.106 MM		0.150 MM	0.150 MM
73_OHM_DIFF	ISL4,ISL9	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM
73_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL3,ISL10	Y	0.078 MM	0.078 MM		0.160 MM	0.160 MM
85_OHM_DIFF	ISL4,ISL9	Y	0.082 MM	0.082 MM		0.140 MM	0.140 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

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PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 36
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_45S	CPU_TTP	XDP_DBRESET_L	16 17
	CPU_45S	CPU_TTP	XDP_CPU_PRDY_L	6 16 62
	CPU_45S	CPU_TTP	XDP_CPU_PREQ_L	6 16 62
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
	CPU_45S	CPU_TTP	CPU_CFG<11..0>	6 16 62
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 35
	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 35 36 49
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L	15 36
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_45S	CPU_TTP	XDP_CPU_TDI	6 16 62
XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO	6 16 62
XDP_TMS	CPU_45S	CPU_TTP	XDP_CPU_TMS	6 16 62
XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK	6 16 62
XDP_TRST_L	CPU_45S	CPU_TTP	XDP_CPUPCH_TRST_L	6 12 16 62
XDP_BPM_L	CPU_45S	CPU_TTP	XDP_BPM_L<1..0>	6 16
	CPU_45S	CPU_TTP	XDP_BPM_L<7..2>	6 16
	CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>	
	CPU_45S	CPU_TTP	CPU_CFG<15..12>	6 16
(FSB_CPURST_L)	CPU_45S	CPU_TTP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 49
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 49
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 49
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 49
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 49
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 62
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 62
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 62
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 62
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	58 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	58 62
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 58 62
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 58
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 58
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

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CPU Constraints

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING			
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP		
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P		USB Hucopyb nets
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N		
USB_BT	USB_80D	USB	USB_BT_P	14 29	
USB_BT	USB_80D	USB	USB_BT_N	14 29	
	USB_80D	USB	USB_BT_CONN_P	29 62	
	USB_80D	USB	USB_BT_CONN_N	29 62	
	USB_80D	USB	USB_BT_WAKE_P		
	USB_80D	USB	USB_BT_WAKE_N		
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 34 62	
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 34 62	
	USB_80D	USB	USB_TPAD_CONN_P		
	USB_80D	USB	USB_TPAD_CONN_N		
	USB_80D	USB	TPAD_SPI_MOSI_USB_P		
	USB_80D	USB	TPAD_SPI_MISO_USB_N		
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P		
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N		
USB_SDCARD	USB_80D	USB	USB_SDCARD_P		
USB_SDCARD	USB_80D	USB	USB_SDCARD_N		
	SPI_45S	SPI	TPAD_SPI_MOSI	15 34	TP SPI nets
	SPI_45S	SPI	TPAD_SPI_MISO	15 34	
	SPI_45S	SPI	TPAD_SPI_CLK	15 34	
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 33	USB EXTA nets (Right USB port)
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 33	
	UART_45S	UART	SMC_DEBUGPRT_TX_L	33 35 36	
	UART_45S	UART	SMC_DEBUGPRT_RX_L	33 35 36	
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	33	
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	33	
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	33	
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	33	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 33	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 33	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	33	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	33	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P		
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N		
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P		
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N		
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 33	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 33	
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 59 63	USB EXTB nets (Left USB port)
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 59 63	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 59 63	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 59 63	
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	59 63	
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	59 63	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	59 63	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	59 63	
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 59 63	
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 59 63	
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RP	14 63	
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RN	14 63	
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CP	14 63	
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CN	14 63	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P		
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N		
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P		
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N		
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14	
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P		
PCH_DIFFCLK_UNUSED_	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N		
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK		

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC AD<3..0>	14 35 44 62
LPC_FRAME_L	LPC_45S	LPC	LPC FRAME L	14 35 44 62
	LPC_45S	LPC	LPCPLUS RESET L	18 44 62
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK24M SMC	17 35
	CLK_LPC_45S	CLK_LPC	LPC CLK24M SMC R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK24M LPCPLUS	17 44 62
	CLK_LPC_45S	CLK_LPC	LPC CLK24M LPCPLUS R	12 17
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS PCH CLK	14 16 19 25 38 54
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS PCH DATA	14 16 19 25 38 54
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML PCH 0 CLK	14 38
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML PCH 0 DATA	14 38
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS SMC 1 S0 SCL	14 32 35 38 41 42 62
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS SMC 1 S0 SDA	14 32 35 38 41 42 62 71
HDA_BIT_CLK	HDA_45S	HDA	HDA BIT CLK	12 59 63
	HDA_45S	HDA	HDA BIT CLK R	12
HDA_SYNC	HDA_45S	HDA	HDA SYNC	12 59 63
	HDA_45S	HDA	HDA SYNC R	12
HDA_RST_L	HDA_45S	HDA	HDA RST R L	12
	HDA_45S	HDA	HDA RST L	12 59 63
HDA_SDIN0	HDA_45S	HDA	HDA SDIN0	12 59 63
HDA_SDOUT	HDA_45S	HDA	HDA SDOUT	12 59 63
	HDA_45S	HDA	HDA SDOUT R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM CLK32K SUSCLK R	13 36
	CLK_SLOW_45S	CLK_SLOW	SMC CLK32K	35 36
SPI_CLK	SPI_45S	SPI	SPI CLK R	14 44
	SPI_45S	SPI	SPI CLK	44
SPI_MOSI	SPI_45S	SPI	SPI MOSI R	14 44
	SPI_45S	SPI	SPI MOSI	44
SPI_MISO	SPI_45S	SPI	SPI MISO	14 44
	SPI_45S	SPI	SPI MISO R	44
SPI_CS0	SPI_45S	SPI	SPI CS0 R L	14 44
	SPI_45S	SPI	SPI CS0 L	44
	SPI_45S	SPI	SPI SMC CLK	35 44
	SPI_45S	SPI	SPI SMC MOSI	35 44
	SPI_45S	SPI	SPI SMC MISO	35 44
	SPI_45S	SPI	SPI SMC CS L	35 44
	SPI_45S	SPI	SPI MLB CLK	44
	SPI_45S	SPI	SPI MLB MOSI	44
	SPI_45S	SPI	SPI MLB MISO	44
	SPI_45S	SPI	SPI MLB CS L	44
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D P	29 62
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D N	29 62
	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C P	14 29
	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C N	14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R P	14 29 62
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R N	14 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP P	12 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP N	12 29 62
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D P<3..0>	25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D N<3..0>	25
	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C P<3..0>	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C N<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R P<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R N<3..0>	14 25
	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C P<3..0>	25
	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C N<3..0>	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M TBT P	12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M TBT N	12 25
	CLK_PCIE_80D	CLK_PCIE	PEG CLK100M P	
	CLK_PCIE_80D	CLK_PCIE	PEG CLK100M N	
XDP_TDI	PCH_45S	PCH_ITP	XDP PCH TDI	12 16 62
XDP_TDO	PCH_45S	PCH_ITP	XDP PCH TDO	12 16 62
XDP_TMS	PCH_45S	PCH_ITP	XDP PCH TMS	12 16 62
XDP_TCK	PCH_45S	PCH_ITP	XDP PCH TCK	12 16 62
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE CAMERA R2D P	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE CAMERA R2D N	31 32
	PCIE_80D	PCIE_PCH_TX	PCIE CAMERA R2D C P	14 32
	PCIE_80D	PCIE_PCH_TX	PCIE CAMERA R2D C N	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE CAMERA D2R P	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE CAMERA D2R N	14 32
	PCIE_80D	PCIE_PCH_RX	PCIE CAMERA D2R C P	31 32
	PCIE_80D	PCIE_PCH_RX	PCIE CAMERA D2R C N	31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M CAMERA P	12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M CAMERA N	12 32
	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M CAMERA C P	31 32
	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M CAMERA C N	31 32

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK CLK32K RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK CLK25M CAMERA	17 32
	CLK_25M_45S	CLK_25M	CLK25M CAM CLKP	31 32
	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP R	32
	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP	32
	CLK_25M_45S	CLK_25M	CLK25M CAM XTALN	32
	CLK_25M_45S	CLK_25M	CLK25M CAM CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT	17 25
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT R	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X1	17
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2	17
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2 R	17
	CLK_25M_45S	CLK_25M	SDCLK CLK25M X2	
	CLK_25M_45S	CLK_25M	SDCLK CLK25M X2 R	
	CLK_25M_45S	CLK_25M	SDSCLK CLK25M X1	

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 20 21 24 61
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	7 20 24 61
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	7 21 24 61
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 61
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 61
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 61
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 61
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 21 61
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 61
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 61
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 21 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 21 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 61
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 22 23 24 61
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	7 22 24 61
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	7 23 24 61
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 61
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 61
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 61
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 61
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 23 61
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 61
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 61
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 23 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 23 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 61
		MEM_PWR	PP1V2_S3	
		MEM_PWR	PP0V6_S3_MEM_VREFCA_A	17 19 20 21 22 23 40 51 60
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_A	18 19 20 21
		MEM_PWR	PP0V6_S3_MEM_VREFCA_B	18 19 20 21
		MEM_PWR	PP0V6_S3_MEM_VREFDQ_B	18 19 22 23
		MEM_PWR		18 19 22 23

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Memory Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_TX	TBTDP_TX	*	TBTDP_TX2TX
TBTDP_RX	TBTDP_RX	*	TBTDP_RX2RX
TBTDP_TX	TBTDP_RX	*	TBTDP_TX2RX
TBTDP_RX	TBTDP_TX	*	TBTDP_TX2RX
TBTDP_TX	*_TX	*	TBTDP_2OTHERHS
TBTDP_RX	*_TX	*	TBTDP_2OTHERHS
TBTDP_TX	*_RX	*	TBTDP_2OTHERHS
TBTDP_RX	*_RX	*	TBTDP_2OTHERHS
TBTDP_TX	*	*	TBTDP_2OTHER
TBTDP_RX	*	*	TBTDP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_RX2RX	TOP,BOTTOM	=6x_DIELECTRIC	?
TBTDP_TX2RX	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHERHS	TOP,BOTTOM	=10x_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_TX2TX	*	=4x_DIELECTRIC	?
TBTDP_RX2RX	*	=4x_DIELECTRIC	?
TBTDP_TX2RX	*	=6x_DIELECTRIC	?
TBTDP_2OTHERHS	*	=6x_DIELECTRIC	?
TBTDP_2OTHER	*	=4x_DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	62
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	62
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2>	62
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2>	62
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	62
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP	25 62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN	25 62
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	25

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
F10A	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
F10Z		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
F10X	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
F10W	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
F10N	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
F10P	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
F10Q	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
F10R	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
F10S	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
F10T	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
F12V	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
F12W	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
F12X		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 62
F12Y		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 62
F13A	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
F13B	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
F13Z		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 62
F13Y		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 62
F14D			S2_MEM_PWR	PP1V35_CAM	31 32
F14E			S2_MEM_PWR	PP0V675_CAM_VREF	31 32
F14F			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
F14G			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	0.1 MM	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	35 38 58
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	35 38 58
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 62 67
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 62 67
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SCL	35 38 59 63
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_S3_SDA	35 38 59 63
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	34 35 38 42 62
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	34 35 38 42 62
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	35 38 46 48 62
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	35 38 46 48 62

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR			CHGR_CSI_P	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N	48
	2TO1_DIFFPAIR		CHGR_CSI_R_P	48
	2TO1_DIFFPAIR		CHGR_CSI_R_N	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N	48
	2TO1_DIFFPAIR		CHGR_CSO_R_P	41 48
	2TO1_DIFFPAIR		CHGR_CSO_R_N	41 48

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.300 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

J11/J13 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_N	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N	40 50
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P_R	40 41
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N_R	40 41
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_P	40
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_N	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_P	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_P	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_P	39
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_P	40 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_N	40 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_N	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_P	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_P	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N	41 42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P	41 42
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	45 59 63
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	45 59 63
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P	45
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N	45
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	45 62
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	45 62
		SB_POWER	PP3V3_S5	8 11 13 15 16 17 18 28 29 40 52 56 56 57 58 60 62
		SB_POWER	PP3V3_S0	8 11 12 13 15 17 18 27 30 34 36 37 38 39 40 41 42 43 54 57 59
	GND		GND	

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<rdar://component/512995> J41 HW EE Schematic | Pre Proto 1
<rdar://component/508412> J41 HW EE Schematic | Proto 1
<rdar://component/508413> J41 HW EE Schematic | EVT
<rdar://component/508414> J41 HW EE Schematic | DVT

Kismet:

afp://kismet.apple.com/Kismet-Projects/J41-J43

Useful Wiki Links:

Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:

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<rdar://component/497587> MobileMac HW | Schematic
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