1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
1	0006782329	ENGINEERING RELEASED	2016-08-10

DESIGN: X502/MLB_CATZ

LAST CHANGE: Tue Aug 9 17:02:57 2016

LAST_MODIFICATION=Tue Aug 9 17:03:06 2016

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49	63	JACK CODEC	AHAAGE	09/22/2015
50	64	SPEAKER AMP	AHAAGE	03/23/2016
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55	72	CPU IMVP VCC & VCCSA		
56	73	IMVP VCCSA		
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59	77	VR - OPC (EDRAM)		
60	78	PMIC IC & Power Control		
61	79	PMIC VCCPCH VCCIO 1.8V		
62	80	PMIC 1.2V 1.0V 0.6V		
63	81	RAIL DESENSE CAPS		
64	82	Power FETs		
65	84	LCD Backlight Driver		
66	85	eDP Display Connector	X362	06/23/2015
67	86	SSD MODULE	PAULM	06/15/2015
68	99	DEVELOPMENT ONLY	PAULM	06/15/2015
69	100	Power Aliases	X502-EXP	12/03/2015
70	102	NC_ AND NO_TEST SIGNALS	PAULM	06/15/2015
71	103	Memory Signal Swaps	X502-EXP	12/03/2015
72	104	FCT, ICT PROPERTIES	PAULM	06/15/2015
73	500	=LAST SCHEMATIC PAGE=	MICHKLEE	06/23/2015

DOCUMENTS / BOARDS / ASSEMBLIES

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-02265	1	SCHEM,MLB_CATZ,X502	SCH		
820-00875	1	PCBF,MLB_CATZ,X502	MLB	CRITICAL	

639-03266 PCBA,MLB_CATZ,XXXXX,X502

685-00125	1	COMMON PARTS,MLB_CATZ,X502	CBOM		CMN_PARTS_BOM
985-00239	1	DEV PARTS,MLB_CATZ,X502	DEV1		DEVELOPMENT_LIST

BOM_COST_GROUP=NO COST ITEMS

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Major ICs

CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-00235	1	IC,CPU,SKL-ULT,2+3E,42X24MM,BGA1356	U0500	CRITICAL	CPU_SKL:BASE
998-04195	1	INTERPOSER,VTT ADAPTER,SKL-U,BGA1356	U0500	CRITICAL	CPU_SKL:VTT_INTERPOSER
337S00168	1	CPU,SKYU,QJ8N,D0,QS,2/2,2.3,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_2_QS_2.3
337S00170	1	CPU,SKYU,QJ8K,D0,QS,2/2,2.6,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_2_QS_2.6
337S00149	1	CPU,SKYU,QJ57,J0,ES0,2/3,1.6,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_ES0_GD
337S00150	1	CPU,SKYU,QJ58,J0,ES0,2/3,1.6,28W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_ES0_BT
337S00219	1	CPU,SKYU,QK2T,K1,SQS,1.8,15W,.95,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_1G8
337S00220	1	CPU,SKYU,QKBY,K1,SQS,2.2,15W,1.05,BG1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G2
337S00222	1	CPU,SKYU,QK33,K1,SQS,2.0,15W,1.0,BG1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G0
337S00233	1	CPU,SKYU,QK32,K1,SQS,2.4,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_SQS_2G4
337S00232	1	CPU,SKY,SR2JC,K1,PRQ,1.8,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_1G8
337S00239	1	CPU,SKY,SR2JM,K1,PRQ,2.0,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_2G0
337S00234	1	CPU,SKYU,SR2JL,K1,PRQ,2.4,15W,BGA1356	U0500	CRITICAL	CPU_SKL:2_3_PRQ_2G4

ACE

353S00422	2	IC,CD3215,USB PWR SWITCH,A0,6X6MM,BGA96	U3100,U3200	CRITICAL	ACE:A0	
353S00660	2	IC,CD3215,ACE,A1,USB PWR SWITCH,BGA96	U3100,U3200	CRITICAL	ACE:A1	
353S00807	2	IC,CD3215,ACE,B0,USB PWR SWITCH,BGA96	U3100,U3200	CRITICAL	ACE:B0	
353S00887	2	IC,CD3215,ACE,B0,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:B0_B	(BOOT CODE: 0002.08.07)
353S00888	2	IC,CD3215,ACE,B0,USB PWR SW,OTP=2,BGA96	U3100,U3200	CRITICAL	ACE:B0_2	(BOOT CODE: 0002.08.07)
353S00926	2	IC,CD3215,ACE,B03,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:B0_3	(BOOT CODE: 0002.08.08)
353S00961	2	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200	CRITICAL	ACE:C0	

TBT ALPINE RIDGE

338S00160	1	IC,TBT,ALPINE RIDGE DP,QSJV,B1,6X6MM,BGA96	U2800	CRITICAL	TBT_AR:B1_QS
998-04160	1	IC,TBT,ALP-RIDGE DP,SLL44-TRAY,B1,CSP337	U2800	CRITICAL	TBT_AR:B1_PRQ_TRAY
338S00176	1	IC,TBT,ALPN-RIDGE DP,SLL43-T&R,B1,CSP337	U2800	CRITICAL	TBT_AR:B1_PRQ
338S00229	1	IC,TBT,ALPINE RIDGE,QSTY,QS,C0,CSP337	U2800	CRITICAL	TBT_AR:C0_QS
338S00249	1	IC,TBT,ALPINE RIDGE,QT5S,QS,C1,CSP337	U2800	CRITICAL	TBT_AR:C1_QS
338S00254	1	IC,TBT,ALPINE RIDGE,SLLSM,PRQ,C1,CSP337	U2800	CRITICAL	TBT_AR:C1_PRQ

WIRELESS MODULE

339S0250	1	MODULE,WIFI/BT,STELLA CIDRE,MUR,LGA80	U3700	CRITICAL	WIRELESS:MURATA
339S0251	1	MODULE,WIFI/BT,STELLA CIDRE,USI,LGA80	U3700	CRITICAL	WIRELESS:USI

Programmables (All Builds)

SMC

338S1231	1	IC,SMC12,40MHZ/50DMIPS MCU,7X7,168BBGA	U5000	CRITICAL	SMC:BLANK
341S00334	1	IC,SMC-B1,EXT (V2.31A18) POC,X502	U5000	CRITICAL	SMC:POC
341S00429	1	IC,SMC-B1,EXT (V2.35A4) PROTO 1,X502	U5000	CRITICAL	SMC:PROTO1
341S00517	1	IC,SMC-B1,EXT (V2.35A51) PROTO 2,X502	U5000	CRITICAL	SMC:PROTO2
341S00562	1	IC,SMC-B1,EXT (V2.36A2) EVT,X502	U5000	CRITICAL	SMC:EVT
341S00611	1	IC,SMC-B1,EXT (V2.36A33) PRE-DVT,X502	U5000	CRITICAL	SMC:PREDVT
341S00633	1	IC,SMC-B1,EXT (V2.36A48) DVT,X502	U5000	CRITICAL	SMC:DVT
341S00662	1	IC,SMC-B1,EXT (V2.36F58) PVT,X502	U5000	CRITICAL	SMC:PVT

EFI ROM

335S0959	1	IC,SPI SERIAL FLASH,64M BITS,3V,CSP,QE=1	U6100	CRITICAL	BOOTROM:BLANK	MICRON	
335S00006	335S0959	ALT_CMN	ALL	MACRONIX			
341S00389	1	IC,EFI (V0072) PROTO 0,X502	U6100	CRITICAL	BOOTROM:PROTO0		
341S00452	1	IC,EFI (V0093) PROTO 0,X502	U6100	CRITICAL	BOOTROM:PROTO1		
341S00513	1	IC,EFI (V0114) PROTO 2,X502	U6100	CRITICAL	BOOTROM:PROTO2		
341S00543	1	IC,EFI (V0130) PROTO 2.2,X502	U6100	CRITICAL	BOOTROM:PROTO2_2		
341S00573	1	IC,EFI (V0143) EVT,X502	U6100	CRITICAL	BOOTROM:EVT		
341S00673	1	IC,EFI (V0173) PVT,X502	U6100	CRITICAL	BOOTROM:PVT		

BT ROM

335S00024	1	IC,FLASH,USON8,512KBIT,75MHZ	U3770	CRITICAL	BT_ROM:BLANK
335S0837	335S00024	ALT_CMN	ALL	ALTERNATE	
341S00196	1	IC,BT ROM (V53) DVT,X261	U3770	CRITICAL	BT_ROM:X261
341S00397	1	IC,BT ROM (V53) PROTO0,X502	U3770	CRITICAL	BT_ROM:PROTO0
341S00397	1	IC,BT ROM (V53) PROTO0,X502	U3770	CRITICAL	BT_ROM:PVT

WIFI ROM

335S0956	1	IC,MEMORY,EEPROM,4K,1.7V-5.5V,UDFN8	U3780	CRITICAL	WIFI-ROM:BLANK
335S00145	335S0956	ALT_CMN	ALL	ALTERNATE	
341S00607	1	WIFI ROM (P175) PRE-DVT,WW1,X502	U3780	CRITICAL	WIFI-ROM:MURATA-FCC
341S00608	1	WIFI ROM (P175) PRE-DVT,WW2,X502	U3780	CRITICAL	WIFI-ROM:MURATA-ETSI
341S00609	1	WIFI ROM (P175) PRE-DVT,WW3,X502	U3780	CRITICAL	WIFI-ROM:MURATA-APAC
341S00610	1	WIFI ROM (P175) PRE-DVT,IND,X502	U3780	CRITICAL	WIFI-ROM:MURATA-IND
341S00636	1	WIFI ROM (P177) USI-WW1,X502	U3780	CRITICAL	WIFI-ROM:USI-FCC
341S00637	1	WIFI ROM (P177) USI-WW2,X502	U3780	CRITICAL	WIFI-ROM:USI-ETSI
341S00638	1	WIFI ROM (P177) USI-WW3,X502	U3780	CRITICAL	WIFI-ROM:USI-APAC
341S00639	1	WIFI ROM (P177) USI-IND,X502	U3780	CRITICAL	WIFI-ROM:USI-IND

TBT ROM

335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U2890	CRITICAL	AR_ROM:BLANK
341S00451	1	IC,NVM / AR (V0.8.15.E1) PROTO 1,X502	U2890	CRITICAL	AR_ROM:PROTO1
341S00512	1	IC,NVM (VB1-10.11-E2.6.3) PROTO 2,X502	U2890	CRITICAL	AR_ROM:PROTO2
341S00559	1	IC,NVM (V16.8) EVT,X502	U2890	CRITICAL	AR_ROM:EVT
341S00606	1	IC,NVM (V1.5) PRE-DVT,X502	U2890	CRITICAL	AR_ROM:PREDVT
341S00628	1	IC, NVM (V3.8), DVT, X502	U2890	CRITICAL	AR_ROM:DVT
341S00661	1	IC, NVM (VTBD), PVT, X502	U2890	CRITICAL	AR_ROM:PVT

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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BOM Configuration

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Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00101	4	IC,LPDDR3-1866,16GB,512MX32,25NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HYNIX_8GB_1866
333S0784	4	IC,LPDDR3-1866,32GBIT,25NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:HYNIX_16GB_1866
333S00097	4	IC,LPDDR3-1866,16GB,512MX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MICRON_8GB_1866
333S00098	4	IC,LPDDR3-1866,32GB,1GX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:MICRON_16GB_1866
333S00099	4	IC,LPDDR3-1866,16GB,512MX32,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SAMSUNG_8GB_1866
333S00049	4	IC,SDRAM,LPDDR3-1866,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	DRAM:SAMSUNG_16GB_1866

Main DRAM SPD Straps

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

	RAMCFG1	RAMCFG0
HYNIX	0 (STUFF R)	0 (STUFF R)
MICRON	0 (STUFF R)	1 (OPEN)
SAMSUNG	1 (OPEN)	0 (STUFF R)
-RESERVED-	1 (OPEN)	1 (OPEN)

	RAMCFG2
8GB	0 (STUFF R)
16GB	1 (OPEN)

	RAMCFG3
2133	0 (STUFF R)
1867	1 (OPEN)

	RAMCFG4
DIE A	0 (STUFF R)
DIE B	1 (OPEN)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0006	4	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1331,R1332,R1334		DRAM:HYNIX_8GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1331,R1334		DRAM:HYNIX_16GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1331,R1332,R1334		DRAM:MICRON_8GB_1866
117S0006	2	RES,MF,1/20W,1K OHM,5,0201,SMD	R1331,R1334		DRAM:MICRON_16GB_1866
117S0006	3	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1332,R1334		DRAM:SAMSUNG_8GB_1866
117S0006	2	RES,MF,1/20W,1K OHM,5,0201,SMD	R1330,R1334		DRAM:SAMSUNG_16GB_1866

MLB VERSION ID STRAPS

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE	INVERT TO VALUE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:POC	<11111>	<00000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:PROTO0	<11110>	<00001>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:PRE_PROTO1	<11101>	<00010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:PROTO1	<11100>	<00011>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:PROTO2	<11011>	<00100>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:PROTO2_2	<11010>	<00101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:EVT	<11001>	<00110>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:PREDVT	<11000>	<00111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:DVT	<10111>	<01000>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:DVT3	<10110>	<01001>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:PVT	<10101>	<01010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:PRQ1	<10100>	<01011>

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
107S00015	107S00011	ALT_CMN	ALL		TFT
107S00087	107S00029	ALT_CMN	ALL		YAGEO
107S00033	107S00034	ALT_CMN	ALL		TFT
107S00071	107S00053	ALT_CMN	ALL		YAGEO
107S00044	107S00076	ALT_CMN	ALL		CYNTEC
107S00070	107S0085	ALT_CMN	ALL		TDK
107S0248	107S0250	ALT_CMN	ALL		TFT
107S0249	107S0251	ALT_CMN	ALL		TFT
128S00009	128S00015	ALT_CMN	ALL		KEMET
128S00070	128S00015	ALT_CMN	ALL		PANASONIC
128S00010	128S00011	ALT_CMN	ALL		PANASONIC
128S00026	128S00011	ALT_CMN	ALL		NEC
128S00031	128S00011	ALT_CMN	ALL		ROHM
128S00058	128S00018	ALT_CMN	ALL		ROHM
128S00069	128S00067	ALT_CMN	ALL		ROHM
128S00062	128S00067	ALT_CMN	ALL		NEC
128S0364	128S0264	ALT_CMN	ALL		SANYO 2ND FACTORY
128S0311	128S0329	ALT_CMN	ALL		NEC ALT TO SANYO
128S0325	128S0397	ALT_CMN	ALL		PANASONIC
131S00134	131S00041	ALT_CMN	ALL		TAIYO YUDEN
132S00064	132S0409	ALT_CMN	ALL		MURATA
138S00077	138S00035	ALT_CMN	ALL		TAIYO YUDEN
138S00093	138S00035	ALT_CMN	ALL		KYOCERA
138S00084	138S00060	ALT_CMN	ALL		TAIYO YUDEN
138S0703	138S0648	ALT_CMN	ALL		MURATA
138S0700	138S0641	ALT_CMN	ALL		MURATA
138S0689	138S0701	ALT_CMN	ALL		MURATA
138S0864	138S0709	ALT_CMN	ALL		MULTIPLE
138S1103	138S0719	ALT_CMN	ALL		TAIYO YUDEN
138S0706	138S0739	ALT_CMN	ALL		MURATA
138S00106	138S0754	ALT_CMN	ALL		KYOCERA
138S00015	138S0777	ALT_CMN	ALL		MULTIPLE
138S0846	138S0811	ALT_CMN	ALL		SAMSUNG
138S00032	138S0831	ALT_CMN	ALL		TAIYO YUDEN
138S00049	138S0831	ALT_CMN	ALL		KYOCERA
138S0775	138S0860	ALT_CMN	ALL		SAMSUNG
138S00086	138S0884	ALT_CMN	ALL		TAIYO YUDEN
138S0738	138S1101	ALT_CMN	ALL		SAMSUNG
152S00381	152S1129	ALT_CMN	ALL		CHILISIN
152S00343	152S1682	ALT_CMN	ALL		MURATA
152S00363	152S00048	ALT_CMN	ALL		NEC
152S00358	152S00208	ALT_CMN	ALL		CHILISIN
152S00367	152S00266	ALT_CMN	ALL		NEC
152S00403	152S00322	ALT_CMN	ALL		CHILISIN
152S1872	152S00361	ALT_CMN	ALL		MURATA
155S0659	155S0382	ALT_CMN	ALL		MURATA
155S0694	155S0387	ALT_CMN	ALL		MURATA
155S00155	155S0441	ALT_CMN	ALL		TDK
155S0660	155S0513	ALT_CMN	ALL		MURATA
155S00007	155S0667	ALT_CMN	ALL		TAIYO YUDEN
155S00034	155S0706	ALT_CMN	ALL		MURATA
155S00203	155S0894	ALT_CMN	ALL		TAIYO YUDEN
155S00115	155S00114	ALT_CMN	ALL		MURATA

More Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
197S00046	197S00036	ALT_CMN	ALL		EPSON
197S00047	197S00036	ALT_CMN	ALL		KYOCERA
197S00048	197S00036	ALT_CMN	ALL		MURATA
197S00053	197S00050	ALT_CMN	ALL		KYOCERA
197S00054	197S00050	ALT_CMN	ALL		NDK
197S00055	197S00050	ALT_CMN	ALL		MURATA
311S00008	311S0271	ALT_CMN	ALL		DIODES INC
311S00060	311S0273	ALT_CMN	ALL		DIODES INC
311S00004	311S0370	ALT_CMN	ALL		ON SEMI
311S00013	311S0508	ALT_CMN	ALL		DIODES INC
311S00122	311S0543	ALT_CMN	ALL		DIODES INC
311S0596	311S0593	ALT_CMN	ALL		TI
311S00097	311S00036	ALT_CMN	ALL		DIODES INC
353S00711	353S2073	ALT_CMN	ALL		ON SEMI
353S00712	353S2216	ALT_CMN	ALL		ON SEMI
353S00107	353S3239	ALT_CMN	ALL		ON SEMI
353S00854	353S4342	ALT_CMN	ALL		ST MICRO
353S00769	353S4398	ALT_CMN	ALL		DIODES INC
353S00525	353S4471	ALT_CMN	ALL		VISHAY
371S0713	371S0558	ALT_CMN	ALL		DIODES INC
371S00074	371S0602	ALT_CMN	ALL		INFINEON
371S0704	371S00077	ALT_CMN	ALL		NXP
371S00089	371S00085	ALT_CMN	ALL		DIODES INC
372S0186	372S0185	ALT_CMN	ALL		NXP
372S00016	372S00015	ALT_CMN	ALL		DIODES INC
376S1053	376S0604	ALT_CMN	ALL		DIODES INC
376S1106	376S0678	ALT_CMN	ALL		FAIRCHILD
376S00014	376S0761	ALT_CMN	ALL		TOSHIBA
376S00086	376S0761	ALT_CMN	ALL		DIODES INC.
376S1080	376S0820	ALT_CMN	ALL		DIODES INC
376S00074	376S0855	ALT_CMN	ALL		TOSHIBA
376S00146	376S1061	ALT_CMN	ALL		ROHM
376S1089	376S1128	ALT_CMN	ALL		NXP
377S00031	377S0178	ALT_CMN	ALL		ON SEMI
377S00048	377S00017	ALT_CMN	ALL		ST MICRO
377S0155	377S00011	ALT_CMN	ALL		ON SEMI
740S0144	740S0118	ALT_CMN	ALL		LITTELFUSE
740S00028	740S0118	ALT_CMN	ALL		BUSSMANN
740S00003	740S0135	ALT_CMN	ALL		AEM, INC.
740S00027	740S0159	ALT_CMN	ALL		BOURNS
740S00033	740S00002	ALT_CMN	ALL		THINKING
740S00007	740S00019	ALT_CMN	ALL		BOURNS

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
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BOM Configuration

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MOUNTING HOLES

998-03850

SH0400
4.0R3.6-NSP

SH0401
4.0R3.6-NSP

FAN MOUNTING HOLE

998-03850

SH0410
TH-NSP
SL-2.6X2.0-4.7X4.1

PLATED HOLES

SH0420
TH-NSP
LARGER SLOT, NEAR ANTENNA
SL-3.38X2.1-5.88X4.6
998-06494

SH0421
TH-NSP
SL-3.36X2.1-5.86X4.6
998-03823

SH0425
TH-NSP
SL-3.36X2.1-5.86X4.6

SH0426
TH-NSP
SL-3.36X2.1-5.86X4.6
998-03823

POGO PINS

870-01680

SH0430
POGO-2.30D-4.1H-SM

SH0431
POGO-2.30D-4.1H-SM

SH0437
POGO-2.30D-4.1H-SM

870-02068

SH0432
POGO-2.00D-2.95H-SM-1

SH0434
POGO-2.30D-4.1H-SM

SH0435
POGO-2.30D-4.1H-SM

SH0436
POGO-2.30D-4.1H-SM

SH0433
POGO-2.00D-2.95H-SM-1

TOP STANDOFFS

860-00385

SH0450
2.8OD1.2ID-1.44H-SM

SH0451
2.8OD1.2ID-1.44H-SM

SH0452
2.8OD1.2ID-1.44H-SM

SH0453
2.8OD1.2ID-1.44H-SM

SH0455
2.8OD1.2ID-1.44H-SM

SH0457
2.8OD1.2ID-1.44H-SM

BOTTOM STANDOFFS

860-00468

SH0460
2.8OD1.2ID-3.0H-SM

SH0461
2.8OD1.2ID-3.0H-SM

SHIELD CANS

MEMORY CAN - TOP

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07887	1	SHIELD CAN FENCE,DRAM,MN,X520	SHLD4	CRITICAL	SHIELD_CAN_MEMORY_TOP

MEMORY CAN - BOTTOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-08894	1	SHIELD FENCE,BOT DRAM,SUS,PRE-MN,X520	SHLD1	CRITICAL	SHIELD_CAN_MEMORY_BOT

WIRELESS CAN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07886	1	SHIELD CAN,EMI,WIFI,SYM,MN,TALL,X520	SHLD2	CRITICAL	SHIELD_CAN_WIFI

USB-C CAN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-07885	1	SHIELD CAN,AR,USB-C,THRU,X520	SHLD3	CRITICAL	SHIELD_CAN_USBC

BOM_COST_GROUP=MECHANICALS

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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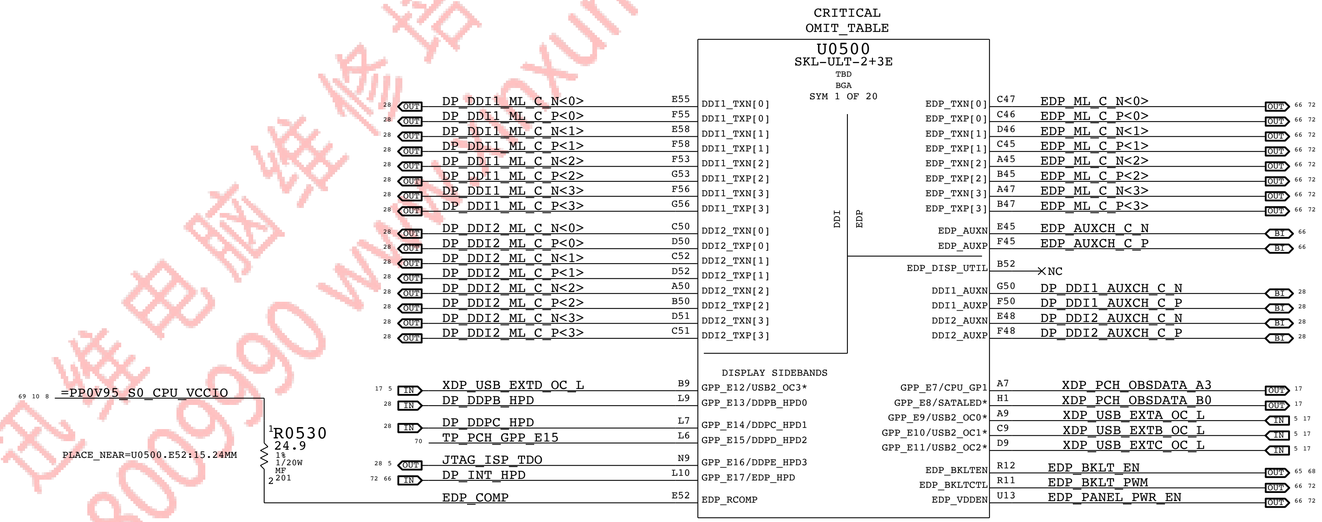

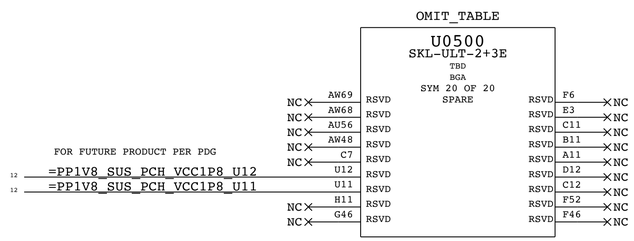

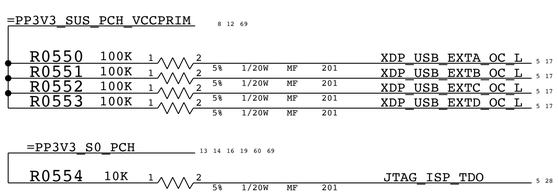

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
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CPU GFX

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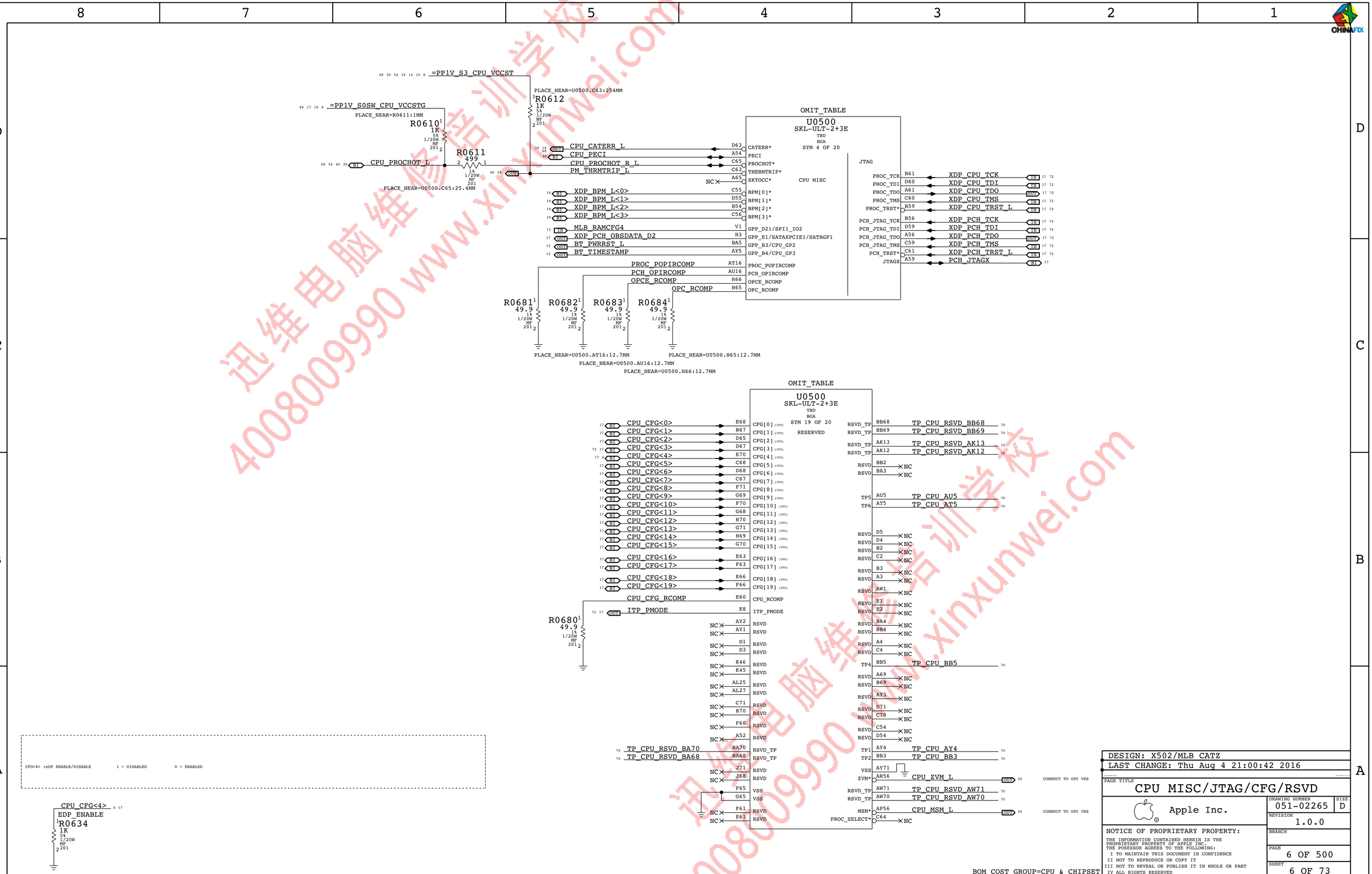

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OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 2 OF 20

LPDDR3 NON-INTERLEAVED0

Signal	Pin	Net
MEM_A_DQ<0>	AL71	DDR0_DQ[0]
MEM_A_DQ<1>	AL68	DDR0_DQ[1]
MEM_A_DQ<2>	AN68	DDR0_DQ[2]
MEM_A_DQ<3>	AN69	DDR0_DQ[3]
MEM_A_DQ<4>	AL70	DDR0_DQ[4]
MEM_A_DQ<5>	AL69	DDR0_DQ[5]
MEM_A_DQ<6>	AN70	DDR0_DQ[6]
MEM_A_DQ<7>	AN71	DDR0_DQ[7]
MEM_A_DQ<8>	AR70	DDR0_DQ[8]
MEM_A_DQ<9>	AR68	DDR0_DQ[9]
MEM_A_DQ<10>	AU71	DDR0_DQ[10]
MEM_A_DQ<11>	AU68	DDR0_DQ[11]
MEM_A_DQ<12>	AR71	DDR0_DQ[12]
MEM_A_DQ<13>	AR69	DDR0_DQ[13]
MEM_A_DQ<14>	AU70	DDR0_DQ[14]
MEM_A_DQ<15>	AU69	DDR0_DQ[15]
MEM_A_DQ<16>	AF65	DDR0_DQ[16]
MEM_A_DQ<17>	AF64	DDR0_DQ[17]
MEM_A_DQ<18>	AK65	DDR0_DQ[18]
MEM_A_DQ<19>	AK64	DDR0_DQ[19]
MEM_A_DQ<20>	AF66	DDR0_DQ[20]
MEM_A_DQ<21>	AF67	DDR0_DQ[21]
MEM_A_DQ<22>	AK67	DDR0_DQ[22]
MEM_A_DQ<23>	AK66	DDR0_DQ[23]
MEM_A_DQ<24>	AF70	DDR0_DQ[24]
MEM_A_DQ<25>	AF68	DDR0_DQ[25]
MEM_A_DQ<26>	AH71	DDR0_DQ[26]
MEM_A_DQ<27>	AH68	DDR0_DQ[27]
MEM_A_DQ<28>	AF71	DDR0_DQ[28]
MEM_A_DQ<29>	AF69	DDR0_DQ[29]
MEM_A_DQ<30>	AH70	DDR0_DQ[30]
MEM_A_DQ<31>	AH69	DDR0_DQ[31]
MEM_A_DQ<32>	BB65	DDR0_DQ[32]
MEM_A_DQ<33>	AW65	DDR0_DQ[33]
MEM_A_DQ<34>	AW63	DDR0_DQ[34]
MEM_A_DQ<35>	AY63	DDR0_DQ[35]
MEM_A_DQ<36>	BA65	DDR0_DQ[36]
MEM_A_DQ<37>	AY65	DDR0_DQ[37]
MEM_A_DQ<38>	BA63	DDR0_DQ[38]
MEM_A_DQ<39>	BB63	DDR0_DQ[39]
MEM_A_DQ<40>	BA61	DDR0_DQ[40]
MEM_A_DQ<41>	AW61	DDR0_DQ[41]
MEM_A_DQ<42>	BB59	DDR0_DQ[42]
MEM_A_DQ<43>	AW59	DDR0_DQ[43]
MEM_A_DQ<44>	BB61	DDR0_DQ[44]
MEM_A_DQ<45>	AY61	DDR0_DQ[45]
MEM_A_DQ<46>	BA59	DDR0_DQ[46]
MEM_A_DQ<47>	AY59	DDR0_DQ[47]
MEM_A_DQ<48>	AT66	DDR0_DQ[48]
MEM_A_DQ<49>	AU66	DDR0_DQ[49]
MEM_A_DQ<50>	AP65	DDR0_DQ[50]
MEM_A_DQ<51>	AN65	DDR0_DQ[51]
MEM_A_DQ<52>	AN66	DDR0_DQ[52]
MEM_A_DQ<53>	AP66	DDR0_DQ[53]
MEM_A_DQ<54>	AT65	DDR0_DQ[54]
MEM_A_DQ<55>	AU65	DDR0_DQ[55]
MEM_A_DQ<56>	AT61	DDR0_DQ[56]
MEM_A_DQ<57>	AU61	DDR0_DQ[57]
MEM_A_DQ<58>	AP60	DDR0_DQ[58]
MEM_A_DQ<59>	AN60	DDR0_DQ[59]
MEM_A_DQ<60>	AN61	DDR0_DQ[60]
MEM_A_DQ<61>	AP61	DDR0_DQ[61]
MEM_A_DQ<62>	AT60	DDR0_DQ[62]
MEM_A_DQ<63>	AU60	DDR0_DQ[63]

Signal	Pin	Net
DDR0_CKP[0]	AT53	MEM_A_CLK_P<0>
DDR0_CKN[0]	AU53	MEM_A_CLK_N<0>
DDR0_CKP[1]	AT55	MEM_A_CLK_P<1>
DDR0_CKN[1]	AU55	MEM_A_CLK_N<1>
DDR0_CKE[0]	BA56	MEM_A_CKE<0>
DDR0_CKE[1]	BB56	MEM_A_CKE<1>
DDR0_CKE[2]	AW56	MEM_A_CKE<2>
DDR0_CKE[3]	AY56	MEM_A_CKE<3>
DDR0_CS[0]*	AU45	MEM_A_CS_L<0>
DDR0_CS[1]*	AU43	MEM_A_CS_L<1>
DDR0_ODT[0]	AT45	MEM_A_ODT<0>
DDR0_ODT[1]	AT43	NC
DDR0_CAA[0]	BA51	MEM_A_CAA<0>
DDR0_CAA[1]	BB54	MEM_A_CAA<1>
DDR0_CAA[2]	BA52	MEM_A_CAA<2>
DDR0_CAA[3]	AY52	MEM_A_CAA<3>
DDR0_CAA[4]	AW52	MEM_A_CAA<4>
DDR0_CAA[5]	AY55	MEM_A_CAA<5>
DDR0_CAA[6]	AW54	MEM_A_CAA<6>
DDR0_CAA[7]	BA54	MEM_A_CAA<7>
DDR0_CAA[8]	BA55	MEM_A_CAA<8>
DDR0_CAA[9]	AY54	MEM_A_CAA<9>
DDR0_CAB[0]	AU46	MEM_A_CAB<0>
DDR0_CAB[1]	AU48	MEM_A_CAB<1>
DDR0_CAB[2]	AT46	MEM_A_CAB<2>
DDR0_CAB[3]	AU50	MEM_A_CAB<3>
DDR0_CAB[4]	AU52	MEM_A_CAB<4>
DDR0_CAB[5]	AY51	MEM_A_CAB<5>
DDR0_CAB[6]	AT48	MEM_A_CAB<6>
DDR0_CAB[7]	AT50	MEM_A_CAB<7>
DDR0_CAB[8]	BB50	MEM_A_CAB<8>
DDR0_CAB[9]	AY50	MEM_A_CAB<9>
DDR0_DQSN[0]	AM70	MEM_A_DQS_N<0>
DDR0_DQSN[1]	AT69	MEM_A_DQS_N<1>
DDR0_DQSN[2]	AH66	MEM_A_DQS_N<2>
DDR0_DQSN[3]	AG69	MEM_A_DQS_N<3>
DDR0_DQSN[4]	BA64	MEM_A_DQS_N<4>
DDR0_DQSN[5]	AY60	MEM_A_DQS_N<5>
DDR0_DQSN[6]	AR66	MEM_A_DQS_N<6>
DDR0_DQSN[7]	AR61	MEM_A_DQS_N<7>
DDR0_DQSP[0]	AM69	MEM_A_DQS_P<0>
DDR0_DQSP[1]	AT70	MEM_A_DQS_P<1>
DDR0_DQSP[2]	AH65	MEM_A_DQS_P<2>
DDR0_DQSP[3]	AG70	MEM_A_DQS_P<3>
DDR0_DQSP[4]	AY64	MEM_A_DQS_P<4>
DDR0_DQSP[5]	BA60	MEM_A_DQS_P<5>
DDR0_DQSP[6]	AR65	MEM_A_DQS_P<6>
DDR0_DQSP[7]	AR60	MEM_A_DQS_P<7>
DDR0_ALERT*	AW50	
DDR0_PAR	AT52	NC
DDR0_MA[3]	BA50	NC
DDR0_MA[4]	BB52	NC
DDR_VREF_CA	AY67	CPU_DIMM_VREFCA
DDR0_VREF_DQ	AY68	CPU_DIMMA_VREFDQ
DDR1_VREF_DQ	BA67	CPU_DIMMB_VREFDQ
DDR_VTT_CNTL	AW67	PM_MEMVTT_EN

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LPDDR3 NON-INTERLEAVED

Signal	Pin	Net
MEM_B_DQ<0>	AY39	DDR1_DQ[0]
MEM_B_DQ<1>	AW39	DDR1_DQ[1]
MEM_B_DQ<2>	AY37	DDR1_DQ[2]
MEM_B_DQ<3>	AW37	DDR1_DQ[3]
MEM_B_DQ<4>	BB39	DDR1_DQ[4]
MEM_B_DQ<5>	BA39	DDR1_DQ[5]
MEM_B_DQ<6>	BA37	DDR1_DQ[6]
MEM_B_DQ<7>	BB37	DDR1_DQ[7]
MEM_B_DQ<8>	AY35	DDR1_DQ[8]
MEM_B_DQ<9>	AW35	DDR1_DQ[9]
MEM_B_DQ<10>	AY33	DDR1_DQ[10]
MEM_B_DQ<11>	AW33	DDR1_DQ[11]
MEM_B_DQ<12>	BB35	DDR1_DQ[12]
MEM_B_DQ<13>	BA35	DDR1_DQ[13]
MEM_B_DQ<14>	BA33	DDR1_DQ[14]
MEM_B_DQ<15>	BB33	DDR1_DQ[15]
MEM_B_DQ<16>	AU40	DDR1_DQ[16]
MEM_B_DQ<17>	AT40	DDR1_DQ[17]
MEM_B_DQ<18>	AT37	DDR1_DQ[18]
MEM_B_DQ<19>	AU37	DDR1_DQ[19]
MEM_B_DQ<20>	AR40	DDR1_DQ[20]
MEM_B_DQ<21>	AP40	DDR1_DQ[21]
MEM_B_DQ<22>	AP37	DDR1_DQ[22]
MEM_B_DQ<23>	AR37	DDR1_DQ[23]
MEM_B_DQ<24>	AT33	DDR1_DQ[24]
MEM_B_DQ<25>	AU33	DDR1_DQ[25]
MEM_B_DQ<26>	AU30	DDR1_DQ[26]
MEM_B_DQ<27>	AT30	DDR1_DQ[27]
MEM_B_DQ<28>	AR33	DDR1_DQ[28]
MEM_B_DQ<29>	AP33	DDR1_DQ[29]
MEM_B_DQ<30>	AR30	DDR1_DQ[30]
MEM_B_DQ<31>	AP30	DDR1_DQ[31]
MEM_B_DQ<32>	AY31	DDR1_DQ[32]
MEM_B_DQ<33>	AW31	DDR1_DQ[33]
MEM_B_DQ<34>	AY29	DDR1_DQ[34]
MEM_B_DQ<35>	AW29	DDR1_DQ[35]
MEM_B_DQ<36>	BB31	DDR1_DQ[36]
MEM_B_DQ<37>	BA31	DDR1_DQ[37]
MEM_B_DQ<38>	BA29	DDR1_DQ[38]
MEM_B_DQ<39>	BB29	DDR1_DQ[39]
MEM_B_DQ<40>	AY27	DDR1_DQ[40]
MEM_B_DQ<41>	AW27	DDR1_DQ[41]
MEM_B_DQ<42>	AY25	DDR1_DQ[42]
MEM_B_DQ<43>	AW25	DDR1_DQ[43]
MEM_B_DQ<44>	BB27	DDR1_DQ[44]
MEM_B_DQ<45>	BA27	DDR1_DQ[45]
MEM_B_DQ<46>	BA25	DDR1_DQ[46]
MEM_B_DQ<47>	BB25	DDR1_DQ[47]
MEM_B_DQ<48>	AU27	DDR1_DQ[48]
MEM_B_DQ<49>	AT27	DDR1_DQ[49]
MEM_B_DQ<50>	AT25	DDR1_DQ[50]
MEM_B_DQ<51>	AU25	DDR1_DQ[51]
MEM_B_DQ<52>	AP27	DDR1_DQ[52]
MEM_B_DQ<53>	AN27	DDR1_DQ[53]
MEM_B_DQ<54>	AN25	DDR1_DQ[54]
MEM_B_DQ<55>	AP25	DDR1_DQ[55]
MEM_B_DQ<56>	AT22	DDR1_DQ[56]
MEM_B_DQ<57>	AU22	DDR1_DQ[57]
MEM_B_DQ<58>	AU21	DDR1_DQ[58]
MEM_B_DQ<59>	AT21	DDR1_DQ[59]
MEM_B_DQ<60>	AN22	DDR1_DQ[60]
MEM_B_DQ<61>	AP22	DDR1_DQ[61]
MEM_B_DQ<62>	AP21	DDR1_DQ[62]
MEM_B_DQ<63>	AN21	DDR1_DQ[63]

Signal	Pin	Net
DDR1_CKP[0]	AP45	MEM_B_CLK_P<0>
DDR1_CKN[0]	AN45	MEM_B_CLK_N<0>
DDR1_CKP[1]	AP46	MEM_B_CLK_P<1>
DDR1_CKN[1]	AN46	MEM_B_CLK_N<1>
DDR1_CKE[0]	AN56	MEM_B_CKE<0>
DDR1_CKE[1]	AP55	MEM_B_CKE<1>
DDR1_CKE[2]	AN55	MEM_B_CKE<2>
DDR1_CKE[3]	AP53	MEM_B_CKE<3>
DDR1_CS[0]*	BB42	MEM_B_CS_L<0>
DDR1_CS[1]*	AY42	MEM_B_CS_L<1>
DDR1_ODT[0]	BA42	MEM_B_ODT<0>
DDR1_ODT[1]	AW42	NC
DDR1_CAA[0]	AY48	MEM_B_CAA<0>
DDR1_CAA[1]	AP50	MEM_B_CAA<1>
DDR1_CAA[2]	BA48	MEM_B_CAA<2>
DDR1_CAA[3]	BB48	MEM_B_CAA<3>
DDR1_CAA[4]	AP48	MEM_B_CAA<4>
DDR1_CAA[5]	AP52	MEM_B_CAA<5>
DDR1_CAA[6]	AN50	MEM_B_CAA<6>
DDR1_CAA[7]	AN48	MEM_B_CAA<7>
DDR1_CAA[8]	AN53	MEM_B_CAA<8>
DDR1_CAA[9]	AN52	MEM_B_CAA<9>
DDR1_CAB[0]	BA43	MEM_B_CAB<0>
DDR1_CAB[1]	AY43	MEM_B_CAB<1>
DDR1_CAB[2]	AY44	MEM_B_CAB<2>
DDR1_CAB[3]	AW44	MEM_B_CAB<3>
DDR1_CAB[4]	BB44	MEM_B_CAB<4>
DDR1_CAB[5]	AY47	MEM_B_CAB<5>
DDR1_CAB[6]	BA44	MEM_B_CAB<6>
DDR1_CAB[7]	AW46	MEM_B_CAB<7>
DDR1_CAB[8]	AY46	MEM_B_CAB<8>
DDR1_CAB[9]	BA46	MEM_B_CAB<9>
DDR1_DQSN[0]	BA38	MEM_B_DQS_N<0>
DDR1_DQSN[1]	AY34	MEM_B_DQS_N<1>
DDR1_DQSN[2]	AT38	MEM_B_DQS_N<2>
DDR1_DQSN[3]	AT32	MEM_B_DQS_N<3>
DDR1_DQSN[4]	BA30	MEM_B_DQS_N<4>
DDR1_DQSN[5]	AY26	MEM_B_DQS_N<5>
DDR1_DQSN[6]	AR25	MEM_B_DQS_N<6>
DDR1_DQSN[7]	AR22	MEM_B_DQS_N<7>
DDR1_DQSP[0]	AY38	MEM_B_DQS_P<0>
DDR1_DQSP[1]	BA34	MEM_B_DQS_P<1>
DDR1_DQSP[2]	AR38	MEM_B_DQS_P<2>
DDR1_DQSP[3]	AR32	MEM_B_DQS_P<3>
DDR1_DQSP[4]	AY30	MEM_B_DQS_P<4>
DDR1_DQSP[5]	BA26	MEM_B_DQS_P<5>
DDR1_DQSP[6]	AR27	MEM_B_DQS_P<6>
DDR1_DQSP[7]	AR21	MEM_B_DQS_P<7>
DDR1_ALERT*	AN43	
DDR1_PAR	AP43	NC
DDR1_MA[3]	BB46	NC
DDR1_MA[4]	BA43	NC
DRAM_RESET*	AT13	NC
DDR_RCOMP[0]	AR18	CPU_DDR_RCOMP<0>
DDR_RCOMP[1]	AT18	CPU_DDR_RCOMP<1>
DDR_RCOMP[2]	AU18	CPU_DDR_RCOMP<2>

R0700
162
1%
1/20W
MF
201

R0701
80.6
1%
1/20W
MF
201

R0702
200
1%
1/20W
MF
201

PLACE_NEAR=U0500.AU18:6MM

PLACE_NEAR=U0500.AT18:6MM

PLACE_NEAR=U0500.AR18:6MM

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE

CPU LPDDR3 Interface

Apple Inc.

DRAWING NUMBER 051-02265

SIZE D

REVISION 1.0.0

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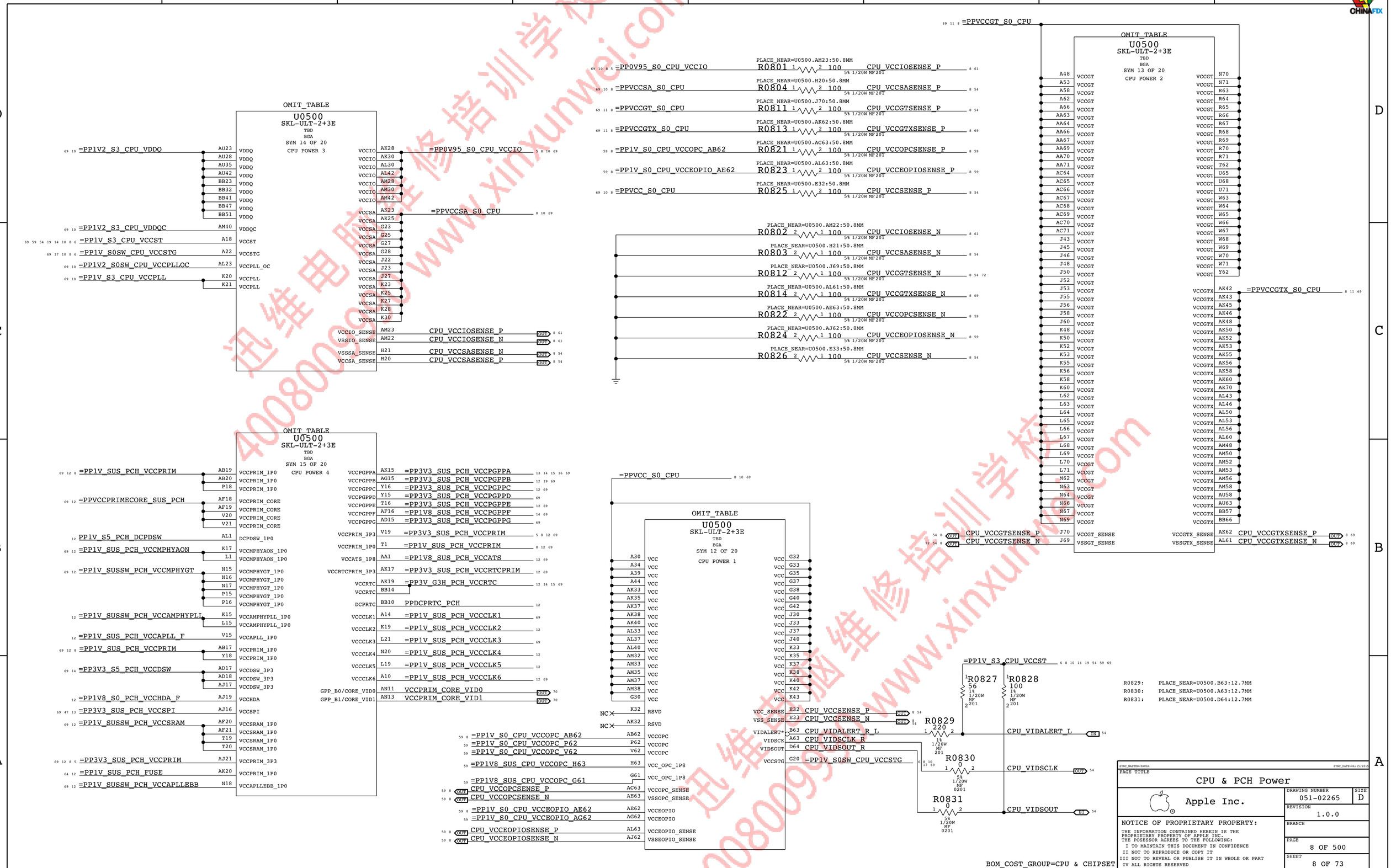
OMIT_TABLE
U0500
SKL-ULT-2+3E
TBD
BGA
SYM 14 OF 20
CPU POWER 3
=PP1V2_S3_CPU_VDDQ
=PP1V2_S3_CPU_VDDQC
=PP1V_S3_CPU_VCCST
=PP1V_S0SW_CPU_VCCSTG
=PP1V2_S0SW_CPU_VCCPLLOC
=PP1V_S3_CPU_VCCPLL
=PP0V95_S0_CPU_VCCIO
=PPVCCSA_S0_CPU
CPU_VCCIOSENSE_P
CPU_VCCIOSENSE_N
CPU_VCCSASENSE_N
CPU_VCCSASENSE_P
OMIT_TABLE
U0500
SKL-ULT-2+3E
TBD
BGA
SYM 15 OF 20
CPU POWER 4
=PP1V_SUS_PCH_VCCPRIM
=PPVCCPRIMECORE_SUS_PCH
PP1V_S5_PCH_DCPDSW
=PP1V_SUS_PCH_VCCMPHYAON
=PP1V_SUSSW_PCH_VCCMPHYGT
=PP1V_SUSSW_PCH_VCCAMPHYPLL
=PP1V_SUS_PCH_VCCAPLL_F
=PP1V_SUS_PCH_VCCPRIM
=PP3V3_S5_PCH_VCCDSW
=PP1V8_S0_PCH_VCCHDA_F
=PP3V3_SUS_PCH_VCCSPI
=PP1V_SUSSW_PCH_VCCSRAM
=PP3V3_SUS_PCH_VCCPRIM
=PP1V_SUS_PCH_FUSE
=PP1V_SUSSW_PCH_VCCAPLLEBB
=PP3V3_SUS_PCH_VCCPGPPA
=PP3V3_SUS_PCH_VCCPGPPB
=PP3V3_SUS_PCH_VCCPGPPC
=PP3V3_SUS_PCH_VCCPGPPD
=PP3V3_SUS_PCH_VCCPGPPE
=PP1V8_SUS_PCH_VCCPGPPF
=PP3V3_SUS_PCH_VCCPGPPG
=PP3V3_SUS_PCH_VCCPRIM
=PP1V_SUS_PCH_VCCPRIM
=PP1V8_SUS_PCH_VCCATS
=PP3V3_SUS_PCH_VCCRTCPRIM
=PP3V_G3H_PCH_VCCRTC
PPDCPRTC_PCH
=PP1V_SUS_PCH_VCCCLK1
=PP1V_SUS_PCH_VCCCLK2
=PP1V_SUS_PCH_VCCCLK3
=PP1V_SUS_PCH_VCCCLK4
=PP1V_SUS_PCH_VCCCLK5
=PP1V_SUS_PCH_VCCCLK6
VCCPRIM_CORE_VID0
VCCPRIM_CORE_VID1
=PPVCC_S0_CPU
OMIT_TABLE
U0500
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BGA
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CPU POWER 1
=PP1V_S0_CPU_VCCOPC_AB62
=PP1V_S0_CPU_VCCOPC_P62
=PP1V_S0_CPU_VCCOPC_V62
=PP1V8_SUS_CPU_VCCOPC_H63
=PP1V8_SUS_CPU_VCCOPC_G61
CPU_VCCOPCSENSE_P
CPU_VCCOPCSENSE_N
=PP1V_S0_CPU_VCCEOPIO_AE62
=PP1V_S0_CPU_VCCEOPIO_AG62
CPU_VCCEOPIOSENSE_P
CPU_VCCEOPIOSENSE_N
=PPVCCGT_S0_CPU
OMIT_TABLE
U0500
SKL-ULT-2+3E
TBD
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SYM 13 OF 20
CPU POWER 2
=PPVCCGTX_S0_CPU
CPU_VCCGTSENSE_P
CPU_VCCGTSENSE_N
CPU_VCCGTXSENSE_P
CPU_VCCGTXSENSE_N
=PP0V95_S0_CPU_VCCIO
=PPVCCSA_S0_CPU
=PPVCCGT_S0_CPU
=PPVCCGTX_S0_CPU
=PPVCC_S0_CPU
R0801 100 5% 1/20W MF 201
R0804 100 5% 1/20W MF 201
R0811 100 5% 1/20W MF 201
R0813 100 5% 1/20W MF 201
R0821 100 5% 1/20W MF 201
R0823 100 5% 1/20W MF 201
R0825 100 5% 1/20W MF 201
R0802 100 5% 1/20W MF 201
R0803 100 5% 1/20W MF 201
R0812 100 5% 1/20W MF 201
R0814 100 5% 1/20W MF 201
R0822 100 5% 1/20W MF 201
R0824 100 5% 1/20W MF 201
R0826 100 5% 1/20W MF 201
PLACE_NEAR=U0500.AM23:50.8MM
PLACE_NEAR=U0500.H20:50.8MM
PLACE_NEAR=U0500.J70:50.8MM
PLACE_NEAR=U0500.AK62:50.8MM
PLACE_NEAR=U0500.AC63:50.8MM
PLACE_NEAR=U0500.AL63:50.8MM
PLACE_NEAR=U0500.E32:50.8MM
PLACE_NEAR=U0500.AM22:50.8MM
PLACE_NEAR=U0500.H21:50.8MM
PLACE_NEAR=U0500.J69:50.8MM
PLACE_NEAR=U0500.AL61:50.8MM
PLACE_NEAR=U0500.AE63:50.8MM
PLACE_NEAR=U0500.AJ62:50.8MM
PLACE_NEAR=U0500.E33:50.8MM
=PP1V_S3_CPU_VCCST
R0827 56 1% 1/20W MF 201
R0828 100 1% 1/20W MF 201
R0829 220 1% 1/20W MF 201
R0830 0 5% 1/20W MF 0201
R0831 0 5% 1/20W MF 0201
CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
=PP1V_S0SW_CPU_VCCSTG
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
R0829: PLACE_NEAR=U0500.B63:12.7MM
R0830: PLACE_NEAR=U0500.A63:12.7MM
R0831: PLACE_NEAR=U0500.D64:12.7MM
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
CPU & PCH Power
Apple Inc.
DRAWING NUMBER 051-02265
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U0500
SKL-ULT-2+3E
TBD
BGA
SYM 16 OF 20
GND1

70 TP_CPU_NCTFVSS_A5	A5 VSS	VSS AL65	
	A67 VSS	VSS AL66	
70 TP_CPU_NCTFVSS_A70	A70 VSS	VSS AM13	
	AA2 VSS	VSS AM21	
	AA4 VSS	VSS AM25	
	AA65 VSS	VSS AM27	
	AA68 VSS	VSS AM43	
	AB15 VSS	VSS AM45	
	AB16 VSS	VSS AM46	
	AB18 VSS	VSS AM55	
	AB21 VSS	VSS AM60	
	AB8 VSS	VSS AM61	
	AD13 VSS	VSS AM68	
	AD16 VSS	VSS AM71	
	AD19 VSS	VSS AM8	
	AD20 VSS	VSS AN20	
	AD21 VSS	VSS AN23	
	AD62 VSS	VSS AN28	
	AD8 VSS	VSS AN30	
	AE64 VSS	VSS AN32	
	AE65 VSS	VSS AN33	
	AE66 VSS	VSS AN35	
	AE67 VSS	VSS AN37	
	AE68 VSS	VSS AN38	
	AE69 VSS	VSS AN40	
	AF1 VSS	VSS AN42	
	AF10 VSS	VSS AN58	
	AF15 VSS	VSS AN63	
	AF17 VSS	VSS AP10	
	AF2 VSS	VSS AP18	
	AF4 VSS	VSS AP20	
	AF63 VSS	VSS AP23	
	AG16 VSS	VSS AP28	
	AG17 VSS	VSS AP32	
	AG18 VSS	VSS AP35	
	AG19 VSS	VSS AP38	
	AG20 VSS	VSS AP42	
	AG21 VSS	VSS AP58	
	AG71 VSS	VSS AP63	
	AH13 VSS	VSS AP68	
	AH6 VSS	VSS AP70	
	AH63 VSS	VSS AR11	
	AH64 VSS	VSS AR15	
	AH67 VSS	VSS AR16	
	AJ15 VSS	VSS AR20	
	AJ18 VSS	VSS AR23	
	AJ20 VSS	VSS AR28	
	AJ4 VSS	VSS AR35	
	AK11 VSS	VSS AR42	
	AK16 VSS	VSS AR43	
	AK18 VSS	VSS AR45	
	AK21 VSS	VSS AR46	
	AK22 VSS	VSS AR48	
	AK27 VSS	VSS AR5	
	AK63 VSS	VSS AR50	
	AK68 VSS	VSS AR52	
	AK69 VSS	VSS AR53	
	AK8 VSS	VSS AR55	
	AL2 VSS	VSS AR58	
	AL28 VSS	VSS AR63	
	AL32 VSS	VSS AR8	
	AL35 VSS	VSS AT2	
	AL38 VSS	VSS AT20	
	AL4 VSS	VSS AT23	
	AL45 VSS	VSS AT28	
	AL48 VSS	VSS AT35	
	AL52 VSS	VSS AT4	
	AL55 VSS	VSS AT42	
	AL58 VSS	VSS AT56	
	AL64 VSS	VSS AT58	

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	AT63 VSS	VSS BA49	
	AT68 VSS	VSS BA53	
	AT71 VSS	VSS BA57	
	AU10 VSS	VSS BA6	
	AU15 VSS	VSS BA62	
	AU20 VSS	VSS BA66	
	AU32 VSS	VSS BA71	TP_CPU_NCTFVSS_BA71 70
	AU38 VSS	VSS BB18	
70 TP_CPU_NCTFVSS_AV1	AV1	VSS BB26	
	AV68 VSS	VSS BB30	
	AV69 VSS	VSS BB34	
	AV70 VSS	VSS BB38	
	AV71 VSS	VSS BB43	
	AW10 VSS	VSS BB55	
	AW12 VSS	VSS BB6	
	AW14 VSS	VSS BB60	
	AW16 VSS	VSS BB64	
	AW18 VSS	VSS BB67	
	AW21 VSS	VSS BB70	TP_CPU_NCTFVSS_BB70 70
	AW23 VSS	VSS C1	TP_CPU_NCTFVSS_C1 70
	AW26 VSS	VSS C25	
	AW28 VSS	VSS C5	
	AW30 VSS	VSS D10	
	AW32 VSS	VSS D11	
	AW34 VSS	VSS D14	
	AW36 VSS	VSS D18	
	AW38 VSS	VSS D22	
	AW41 VSS	VSS D25	
	AW43 VSS	VSS D26	
	AW45 VSS	VSS D30	
	AW47 VSS	VSS D34	
	AW49 VSS	VSS D39	
	AW51 VSS	VSS D44	
	AW53 VSS	VSS D45	
	AW55 VSS	VSS D47	
	AW57 VSS	VSS D48	
	AW6 VSS	VSS D53	
	AW60 VSS	VSS D58	
	AW62 VSS	VSS D6	
	AW64 VSS	VSS D62	
	AW66 VSS	VSS D66	
	AW8 VSS	VSS D69	
	AY66 VSS	VSS E11	
	B10 VSS	VSS E15	
	B14 VSS	VSS E18	
	B18 VSS	VSS E21	
	B22 VSS	VSS E46	
	B30 VSS	VSS E50	
	B34 VSS	VSS E53	
	B39 VSS	VSS E56	
	B44 VSS	VSS E6	
	B48 VSS	VSS E65	
	B53 VSS	VSS E71	
	B58 VSS	VSS F1	
	B62 VSS	VSS F13	
	B66 VSS	VSS F2	
70 TP_CPU_NCTFVSS_B71	B71	VSS F22	
70 TP_CPU_NCTFVSS_BA1	BA1	VSS F23	
	BA10 VSS	VSS F27	
	BA14 VSS	VSS F28	
	BA18 VSS	VSS F32	
	BA2 VSS	VSS F33	
	BA23 VSS	VSS F35	
	BA28 VSS	VSS F37	
	BA32 VSS	VSS F38	
	BA36 VSS	VSS F4	
	F68 VSS	VSS F40	
	BA45 VSS	VSS F42	
		VSS BA41	

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SKL-ULT-2+3E
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F8 VSS	VSS L18	
G10 VSS	VSS L2	
G22 VSS	VSS L20	
G43 VSS	VSS L4	
G45 VSS	VSS L8	
G48 VSS	VSS N10	
G5 VSS	VSS N13	
G52 VSS	VSS N19	
G55 VSS	VSS N21	
G58 VSS	VSS N6	
G6 VSS	VSS N65	
G60 VSS	VSS N68	
G63 VSS	VSS P17	
G66 VSS	VSS P19	
H15 VSS	VSS P20	
H18 VSS	VSS P21	
H71 VSS	VSS R13	
J11 VSS	VSS R6	
J13 VSS	VSS T15	
J25 VSS	VSS T17	
J28 VSS	VSS T18	
J32 VSS	VSS T2	
J35 VSS	VSS T21	
J38 VSS	VSS T4	
J42 VSS	VSS U10	
J8 VSS	VSS U63	
K16 VSS	VSS U64	
K18 VSS	VSS U66	
K22 VSS	VSS U67	
K61 VSS	VSS U69	
K63 VSS	VSS U70	
K64 VSS	VSS V16	
K65 VSS	VSS V17	
K66 VSS	VSS V18	
K67 VSS	VSS W13	
K68 VSS	VSS W6	
K70 VSS	VSS W9	
K71 VSS	VSS Y17	
L11 VSS	VSS Y19	
L16 VSS	VSS Y20	
L17 VSS	VSS Y21	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE
CPU & PCH Grounds

Apple Inc.

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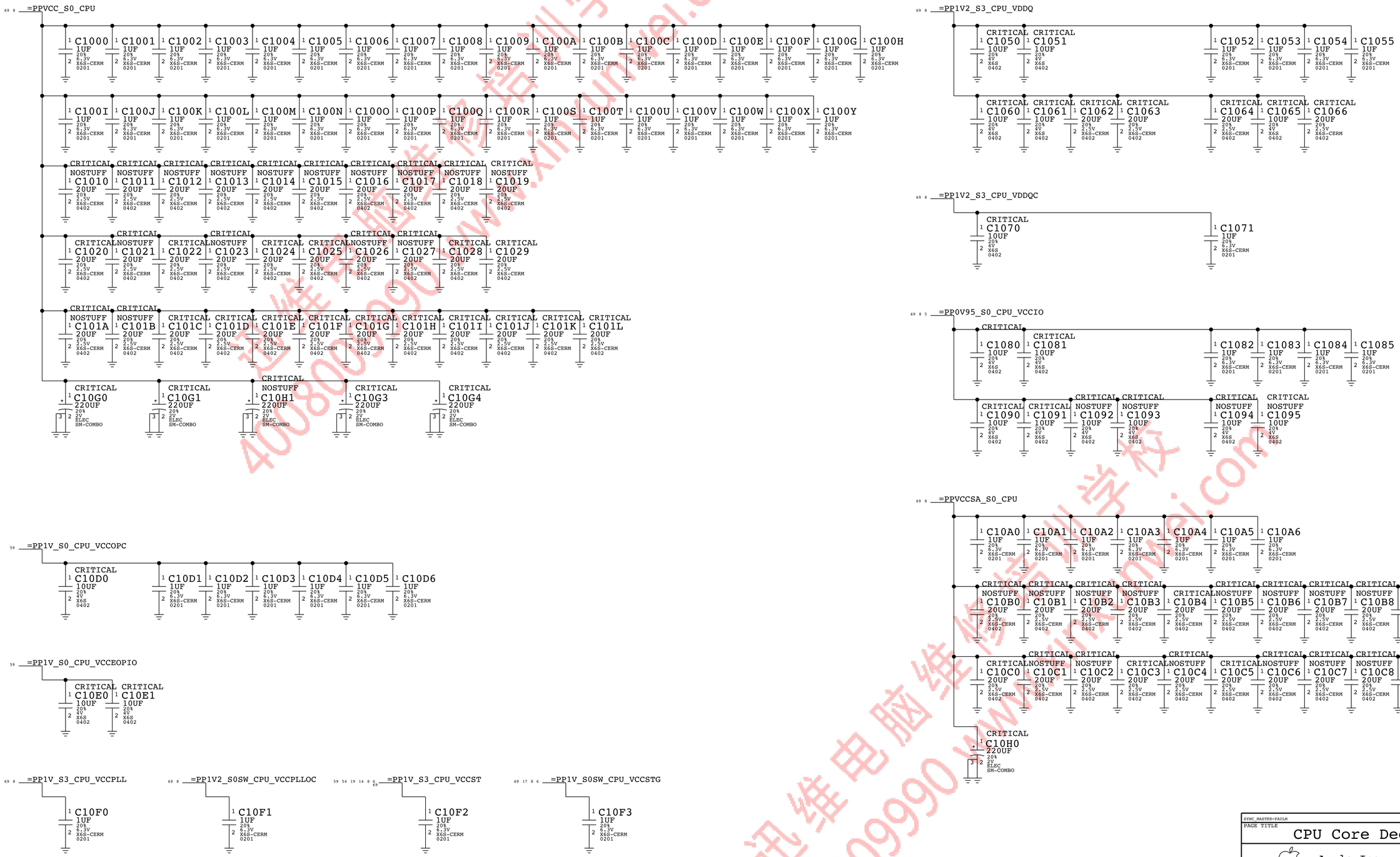

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE

CPU Core Decoupling

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D

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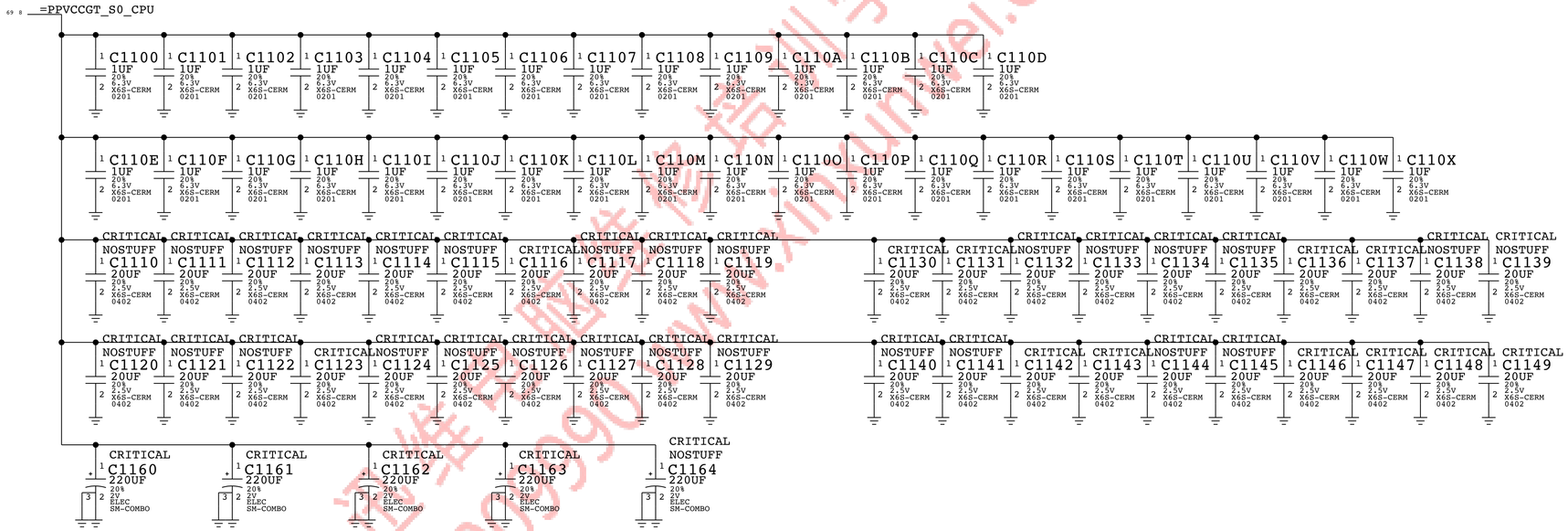

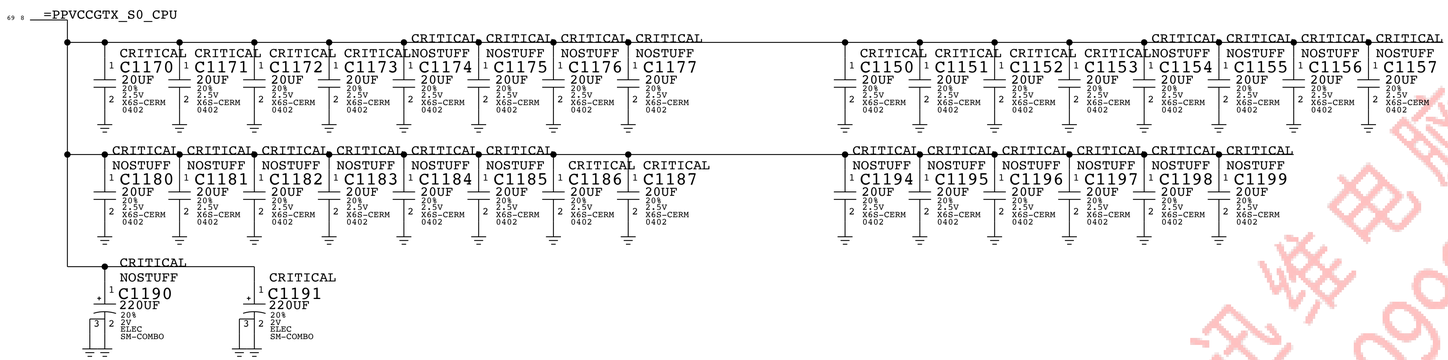

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU GT Decoupling

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DRAWING NUMBER: 051-02265 SIZE: D

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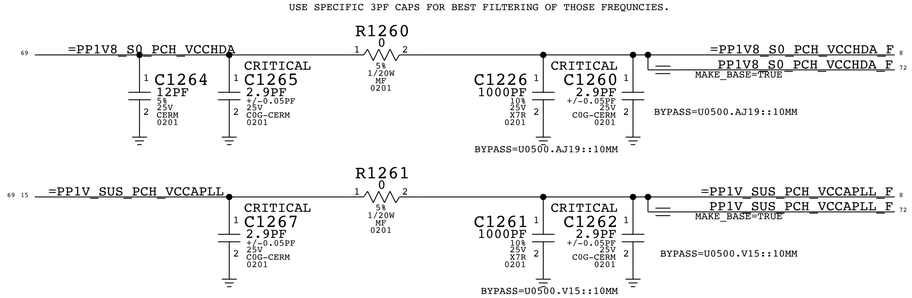
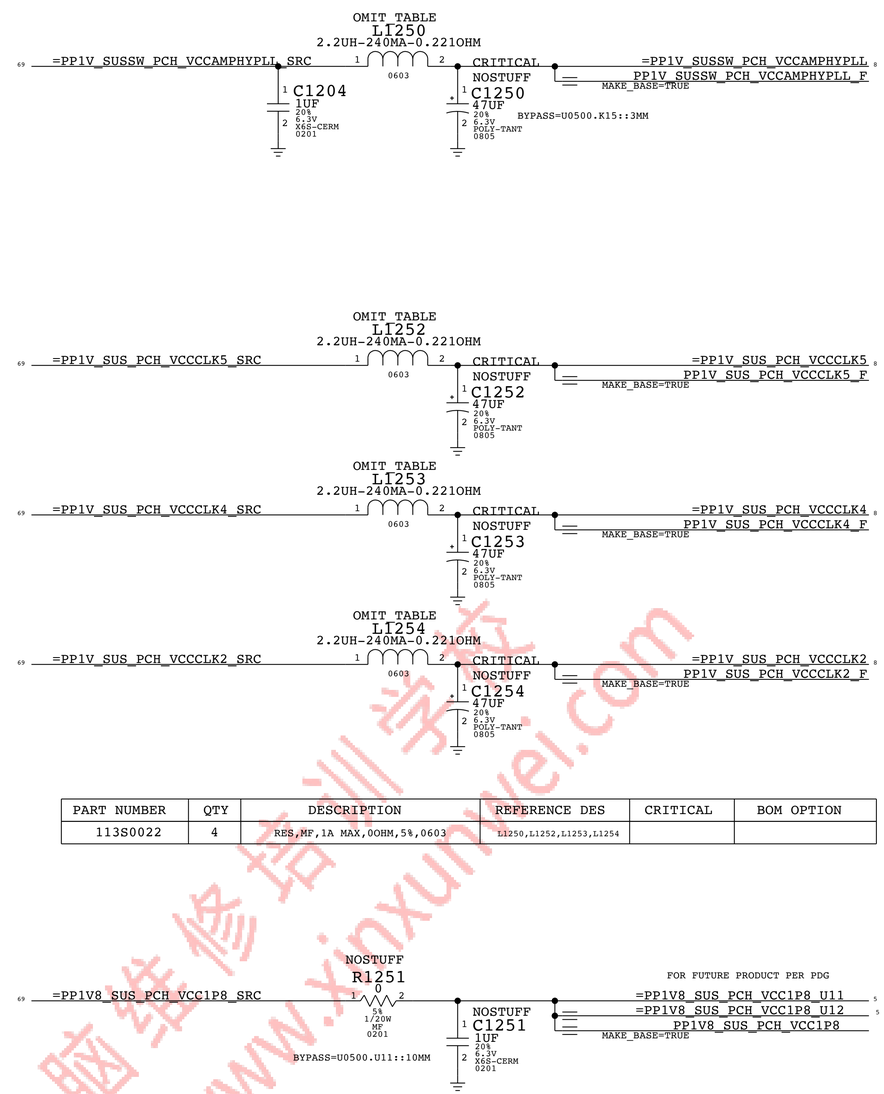
CPU CIRCUITS GENERATE NOISE AT WIFI BAND FREQUENCIES.
USE SPECIFIC 3PF CAPS FOR BEST FILTERING OF THOSE FREQUNCIES.



FILTER PLACEHOLDERS ONLY

RAIL SIDE PCH SIDE



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	4	RES,MF,1A MAX,0OHM,5%,0603	L1250,L1252,L1253,L1254		

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH Decoupling

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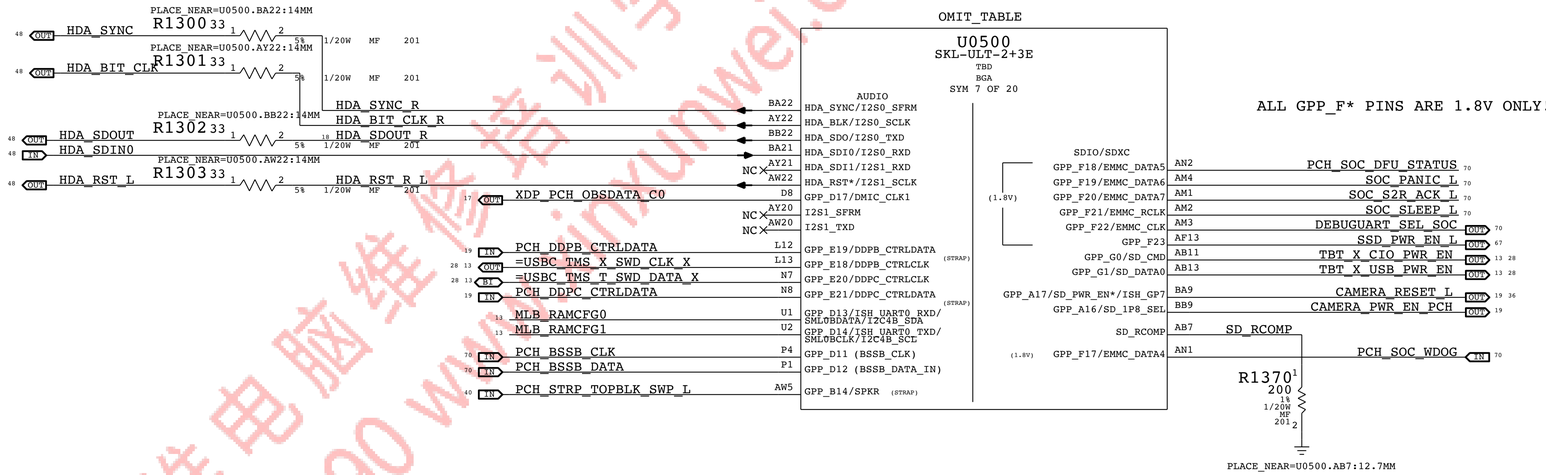
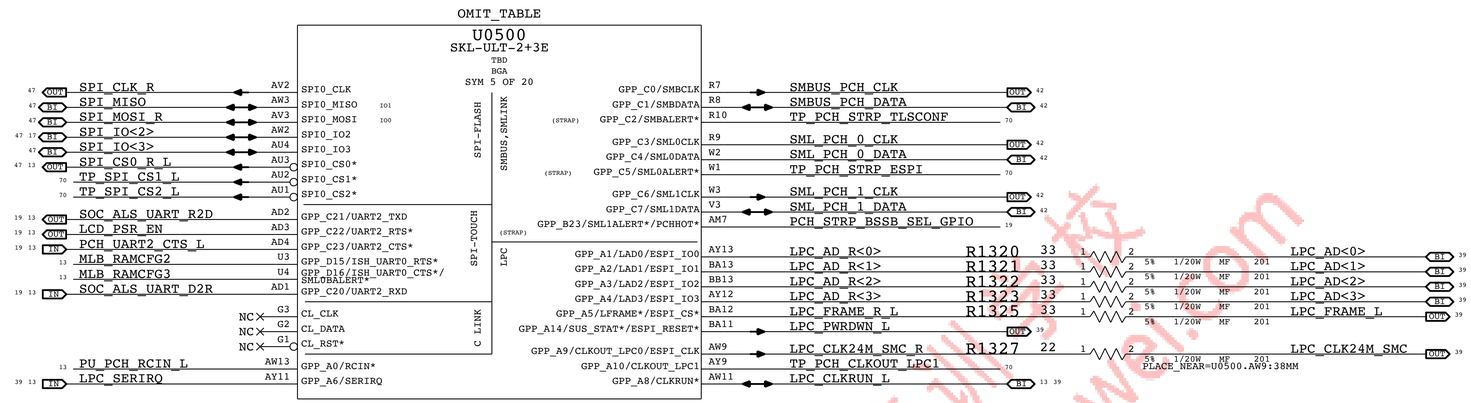
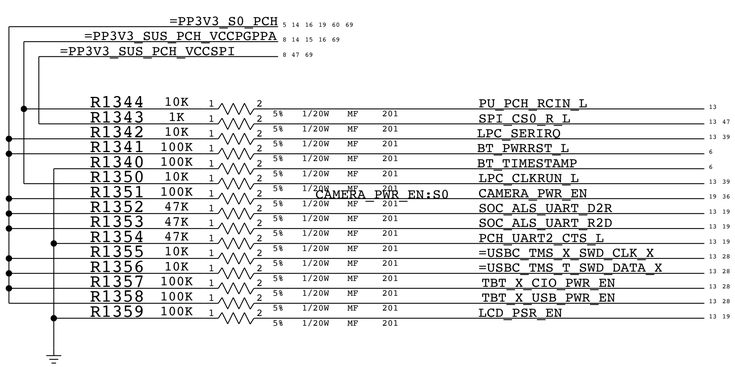
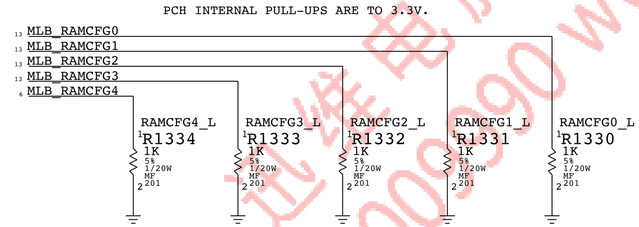






MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH Audio/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
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PCH Reset Button

=PP3V3_SUS_PCH_VCCPGPPA
=PP3V3_S0_PCH
=PP1V_S3_CPU_VCCST

R1405 1K 5% 1/20W MF 201
NOSTUFF R1407 2.2K 5% 1/20W MF 201
R1408 2.2K 5% 1/20W MF 201

PM_SYSRST_L
CPU_VCCST_PWRGD
VCCST_PWRGD 1V TOLERANT
PM_DSW_PWRGD

R1406 60.4k 1% 1/20W MF 201
PLACE_NEAR=U0500.B65:38mm

R1403 100K 5% 1/20W MF 201

NO STUFF
R1400 0 5% 1/20W MF 0201

R1400 kept for debug purposes.

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 11 OF 20
SYSTEM POWER MANAGEMENT

Signal	Pin	Signal	Pin	Net
PLT_RST_L	AN10	GPP_B13/PLTRST*		
	B5	SYS_RESET*		
PM_RSMRST_L	AY17	RSMRST*		
TP_CPU_PWRGD	A68	PROCPWRGD		
CPU_VCCST_PWRGD_R	B65	VCCST_PWRGD (1V ONLY)		
PM_PCH_SYS_PWROK	B6	SYS_PWROK		
PM_PCH_PWROK	BA20	PCH_PWROK		
	BB20	DSW_PWROK		
PCH_SUSWARN_L	AR13	GPP_A13/SUSWARN*/SUSPWRDNACK		
PCH_SUSACK_L	AP11	GPP_A15/SUSACK*		
PCIE_WAKE_L	BB15	WAKE*		
SMC_WAKE_SCI_L	AM15	GPD2/LAN_WAKE*		
TP_PCH_LANPHYPC	AW17	GPD11/LANPHYPC		
TP_PCH_GPD7	AT15	GPD7/RSVD		
	AT11	GPP_B12/SLP_S0*	PM_SLP_S0_L	
	AP15	GPD4/SLP_S3*	PM_SLP_S3_L	
	BA16	GPD5/SLP_S4*	PM_SLP_S4_L	
	AY16	GPD10/SLP_S5*	PM_SLP_S5_L	
	AN15	SLP_SUS*	PM_SLP_SUS_L	
	AW15	SLP_LAN*	NC	
	BB17	GPD9/SLP_WLAN*	TP_PCH_SLP_WLAN_L	
	AN16	GPD6/SLP_A*	TP_PCH_SLP_A_L	
	BA15	GPD3/PWRBTN*	PCH_PWRBTN_L	
	AY15	GPD1/ACPRESENT	SSD_SR_EN_L	
	AU13	GPD0/BATLOW*	PM_BATLOW_L	
	AU11	GPP_A11/PME*	TP_PCH_PME_L	
	AP16	INTRUDER*	PCH_INTRUDER_L	
	AM10	GPP_B11/EXT_PWR_GATE*	PCH_HSIO_PWR_EN	
	AM11	GPP_B2/VRALERT*	BT_LOW_PWR_L	

=PP3V_G3H_PCH_VCCRTC
R1401 1M 5% 1/20W MF 201

=PP1V8_SUS_PCH_VCCPGPPF
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S4_PCH
=PP3V3_S0_PCH

R1446	100K	PCH_SWD_CLK	
R1445	100K	PCH_SWD_IO	
R1444	100K	PCH_SWD_MUX_SEL	
NOSTUFF R1443	100K	SOC_S2R_L	
R1442	100K	SSD_BOOT_L	
R1441	10K	BT_LOW_PWR_L	
R1440	100K	SSD_SR_EN_L	
R1450	1K	PCH_PWRBTN_L	
R1451	10K	PM_BATLOW_L	
R1452	10K	PCIE_WAKE_L	
R1453	100K	SMC_WAKE_SCI_L	
R1454	100K	PM_SLP_S5_L	
R1455	100K	PM_SLP_S4_L	
R1456	100K	PM_SLP_S3_L	
R1457	220K	PM_SLP_S0_L	
R1458	100K	PM_SLP_SUS_L	

NOTE: PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 9 OF 20

CSI-2

Pin	Signal	Pin	Signal
A36	CSI2_DN0	C37	CSI2_CLKN0
B36	CSI2_DP0	D37	CSI2_CLKP0
C38	CSI2_DN1	C32	CSI2_CLKN1
D38	CSI2_DP1	D32	CSI2_CLKP1
C36	CSI2_DN2	C29	CSI2_CLKN2
D36	CSI2_DP2	D29	CSI2_CLKP2
A38	CSI2_DN3	B26	CSI2_CLKN3
B38	CSI2_DP3	A26	CSI2_CLKP3
C31	CSI2_DN4	E13	CSI2_COMP
D31	CSI2_DP4	M1	GPP_D0/SPI1_CS*
C33	CSI2_DN5		
D33	CSI2_DP5		
A31	CSI2_DN6	AH12	GPP_F7/I2C3_SCL
B31	CSI2_DP6	AF11	GPP_F8/I2C4_SDA
A33	CSI2_DN7	AF12	GPP_F9/I2C4_SCL
B33	CSI2_DP7	AD11	GPP_F10/I2C5_SDA/ISH_I2C2_SDA
		AD12	GPP_F11/I2C5_SCL/ISH_I2C2_SCL
A29	CSI2_DN8	AP4	GPP_F12/EMMC_CMD
B29	CSI2_DP8	AP2	GPP_F13/EMMC_DATA0
C28	CSI2_DN9	AP1	GPP_F14/EMMC_DATA1
D28	CSI2_DP9	AP3	GPP_F15/EMMC_DATA2
A27	CSI2_DN10	AN3	GPP_F16/EMMC_DATA3
B27	CSI2_DP10	AH11	GPP_F6/I2C3_SDA
C27	CSI2_DN11		
D27	CSI2_DP11	AT1	EMMC_RCOMP

EMMC (1.8V)

CSI2_COMP
R1480 100 1% 1/20W MF 201
PLACE_NEAR=U0500.E13:12.7MM

ALL GPP_F* PINS ARE 1.8V ONLY!

Signal	Net
	TP_PCH_GPP_D0
	SSD_BOOT_L
	TP_PCH_GPP_F8
	TP_PCH_GPP_F9
	TP_PCH_GPP_F10
	PCH_BT_ROM_BOOT
	PCH_SWD_CLK
	PCH_SWD_IO
	PCH_SWD_MUX_SEL
	SOC_S2R_L
	PCH_SOC_FORCE_DFU
	UPC_I2C_INT_L

EMMC_RCOMP
R1481 200 1% 1/20W MF 201
PLACE_NEAR=U0500.AT1:12.7MM

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH Power Management

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PCIe Port Assignments:

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 8 OF 20

Signal	Pin	Dir	Lane
PCIE_SSD_D2R_N<0>	H13	IN	SSD LANE 0
PCIE_SSD_D2R_P<0>	G13	IN	SSD LANE 0
PCIE_SSD_R2D_C_N<0>	B17	OUT	SSD LANE 0
PCIE_SSD_R2D_C_P<0>	A17	OUT	SSD LANE 0
PCIE_SSD_D2R_N<1>	G11	IN	SSD LANE 1
PCIE_SSD_D2R_P<1>	F11	IN	SSD LANE 1
PCIE_SSD_R2D_C_N<1>	D16	OUT	SSD LANE 1
PCIE_SSD_R2D_C_P<1>	C16	OUT	SSD LANE 1
PCIE_SSD_D2R_N<2>	H16	IN	SSD LANE 2
PCIE_SSD_D2R_P<2>	G16	IN	SSD LANE 2
PCIE_SSD_R2D_C_N<2>	D17	OUT	SSD LANE 2
PCIE_SSD_R2D_C_P<2>	C17	OUT	SSD LANE 2
PCIE_SSD_D2R_N<3>	G15	IN	SSD LANE 3
PCIE_SSD_D2R_P<3>	F15	IN	SSD LANE 3
PCIE_SSD_R2D_C_N<3>	B19	OUT	SSD LANE 3
PCIE_SSD_R2D_C_P<3>	A19	OUT	SSD LANE 3
PCIE_TBT_X_D2R_N<0>	F16	IN	Thunderbolt X lane 0
PCIE_TBT_X_D2R_P<0>	E16	IN	Thunderbolt X lane 0
PCIE_TBT_X_R2D_C_N<0>	C19	OUT	Thunderbolt X lane 0
PCIE_TBT_X_R2D_C_P<0>	D19	OUT	Thunderbolt X lane 0
PCIE_TBT_X_D2R_N<1>	G18	IN	Thunderbolt X lane 1
PCIE_TBT_X_D2R_P<1>	F18	IN	Thunderbolt X lane 1
PCIE_TBT_X_R2D_C_N<1>	D20	OUT	Thunderbolt X lane 1
PCIE_TBT_X_R2D_C_P<1>	C20	OUT	Thunderbolt X lane 1
PCIE_TBT_X_D2R_N<2>	F20	IN	Thunderbolt X lane 2
PCIE_TBT_X_D2R_P<2>	E20	IN	Thunderbolt X lane 2
PCIE_TBT_X_R2D_C_N<2>	B21	OUT	Thunderbolt X lane 2
PCIE_TBT_X_R2D_C_P<2>	A21	OUT	Thunderbolt X lane 2
PCIE_TBT_X_D2R_N<3>	G21	IN	Thunderbolt X lane 3
PCIE_TBT_X_D2R_P<3>	F21	IN	Thunderbolt X lane 3
PCIE_TBT_X_R2D_C_N<3>	D21	OUT	Thunderbolt X lane 3
PCIE_TBT_X_R2D_C_P<3>	C21	OUT	Thunderbolt X lane 3
PCIE_AP_D2R_N	E22	IN	AirPort
PCIE_AP_D2R_P	E23	IN	AirPort
PCIE_AP_R2D_C_N	B23	OUT	AirPort
PCIE_AP_R2D_C_P	A23	OUT	AirPort
PCIE_CAMERA_D2R_N	F25	IN	CAMERA
PCIE_CAMERA_D2R_P	E25	IN	CAMERA
PCIE_CAMERA_R2D_C_N	D23	OUT	CAMERA
PCIE_CAMERA_R2D_C_P	C23	OUT	CAMERA
PCH_PCIE_RCOMP_N	F5		
PCH_PCIE_RCOMP_P	E5		
XDP_CPU_PRDY_L	D56	OUT	
XDP_CPU_PREQ_L	D61	IN	
SMC_RUNTIME_SCI_L	BB11	IN	
PCIE_TBT_T_D2R_N<0>	E28	IN	Thunderbolt T lane 0
PCIE_TBT_T_D2R_P<0>	E27	IN	Thunderbolt T lane 0
PCIE_TBT_T_R2D_C_N<0>	D24	OUT	Thunderbolt T lane 0
PCIE_TBT_T_R2D_C_P<0>	C24	OUT	Thunderbolt T lane 0
PCIE_TBT_T_D2R_N<1>	E30	IN	Thunderbolt T lane 1
PCIE_TBT_T_D2R_P<1>	F30	IN	Thunderbolt T lane 1
PCIE_TBT_T_R2D_C_N<1>	A25	OUT	Thunderbolt T lane 1
PCIE_TBT_T_R2D_C_P<1>	B25	OUT	Thunderbolt T lane 1

PCIE/USB3/SATA

R1504 100 1% 1/20W MF 201 (PLACE_NEAR=U0500.F5:12.7mm)

Signal	Pin	Dir
USB3_1_RXN	H8	IN
USB3_1_RXP	G8	IN
USB3_1_TXN	C13	OUT
USB3_1_TXP	D13	OUT
USB3_2_RXN/SSIC_RXN	J6	IN
USB3_2_RXP/SSIC_RXP	H6	IN
USB3_2_TXN/SSIC_TXN	B13	OUT
USB3_2_TXP/SSIC_TXP	A13	OUT
USB3_3_RXN	J10	
USB3_3_RXP	H10	
USB3_3_TXN	B15	
USB3_3_TXP	A15	
USB3_4_RXN	E10	
USB3_4_RXP	F10	
USB3_4_TXN	C15	
USB3_4_TXP	D15	
USB2N_1	AB9	
USB2P_1	AB10	
USB2N_2	AD6	
USB2P_2	AD7	
USB2N_3	AH3	
USB2P_3	AJ3	
USB2N_4	AD9	
USB2P_4	AD10	
USB2N_5	AJ1	
USB2P_5	AJ2	
USB2N_6	AF6	
USB2P_6	AF7	
USB2N_7	AH1	
USB2P_7	AH2	
USB2N_8	AF8	
USB2P_8	AF9	
USB2N_9	AG1	
USB2P_9	AG2	
USB2N_10	AH7	
USB2P_10	AH8	
USB2_COMP	AB6	
USB2_ID	AG3	
USB2_VBUSSENSE	AG4	
GPP_E3/CPU_GP0	A6	
GPP_E4/DEVSLP0	J1	
GPP_E5/DEVSLP1	J2	
GPP_E6/DEVSLP2	J3	
GPP_D22/SPI1_IO3	V2	
GPP_D23/I2S_MCLK	J5	
GPP_E0/SATAXPCIE0/SATAGP0	H2	
GPP_D18/DMIC_DATA1	C8	
GPP_D19/DMIC_CLK0	H5	
GPP_D20/DMIC_DATA0	D7	
GPP_E2/SATAXPCIE2/SATAGP2	G4	

USB3 (SSIC/USB3): USB3_EXTA_D2R_N, USB3_EXTA_D2R_P, USB3_EXTA_R2D_C_N, USB3_EXTA_R2D_C_P — EXT A (SS,DCI)

USB3: USB3_EXTB_D2R_N, USB3_EXTB_D2R_P, USB3_EXTB_R2D_C_N, USB3_EXTB_R2D_C_P — EXT B (SS)

USB3: TP_USB3_03_D2RN, TP_USB3_03_D2RP, TP_USB3_03_R2DN, TP_USB3_03_R2DP

USB3: TP_USB3_04_D2RN, TP_USB3_04_D2RP, TP_USB3_04_R2DN, TP_USB3_04_R2DP

USB2: USB_EXTA_N, USB_EXTA_P — EXT A (LS/FS/HS)

USB2: USB_EXTB_N, USB_EXTB_P — EXT B (LS/FS/HS)

USB2: USB_CAMERA_DFR_N, USB_CAMERA_DFR_P

USB2: TP_USB_TESTERN, TP_USB_TESTERP

USB2: NC_USB2_05N, NC_USB2_05P

USB2: NC_USB2_06N, NC_USB2_06P

USB2: NC_USB2_07N, NC_USB2_07P

USB2: NC_USB2_08N, NC_USB2_08P

USB2: NC_USB2_09N, NC_USB2_09P

USB2: NC_USB2_10N, NC_USB2_10P

USB2: PCH_USB2_COMP

USB2: PCH_USB2_VBUSSENSE — GROUNDED PER SKYLAKE MOW 2015WW10.

R1501 113 1% 1/20W MF 201 (PLACE_NEAR=U0500.AB6:12.7MM)

R1503 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.AG4:12.7MM)

JTAG: XDP_PCH_OBSFN_C1, XDP_JTAG_ISP_TCK, XDP_JTAG_ISP_TDI, XDP_PCH_OBSDATA_A2

SPI: SPKR_ID0, XDP_PCH_OBSDATA_D0, XDP_PCH_OBSDATA_D1

DMIC: XDP_PCH_OBSDATA_C1, XDP_PCH_OBSDATA_C2, XDP_PCH_OBSDATA_C3, XDP_PCH_OBSDATA_D3

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 10 OF 20

CLOCK SIGNALS

ANY CLKREQ CAN MAP TO ANY CLK.
ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
PER SKYLAKE PDG, SKYLAKE PCH EDS.

Signal	Pin	Dir
PCIE_CLK100M_SSD_N	D42	OUT
PCIE_CLK100M_SSD_P	C42	OUT
=SSD_CLKREQ_L	AR10	IN
PCIE_CLK100M_TBT_X_N	B42	OUT
PCIE_CLK100M_TBT_X_P	A42	OUT
=TBT_X_CLKREQ_L	AT7	IN
PCIE_CLK100M_TBT_T_N	D41	OUT
PCIE_CLK100M_TBT_T_P	C41	OUT
=TBT_T_CLKREQ_L	AT8	IN
PCIE_CLK100M_AP_N	D40	OUT
PCIE_CLK100M_AP_P	C40	OUT
=AP_CLKREQ_L	AT10	IN
PCIE_CLK100M_CAMERA_N	B40	OUT
PCIE_CLK100M_CAMERA_P	A40	OUT
=CAMERA_CLKREQ_L	AU8	IN
TP_PCIE_CLK100M5N	E40	
TP_PCIE_CLK100M5P	E38	
TP_PCH_CLKREQ5_L	AU7	
CLKOUT_ITPXDP_N	F43	
CLKOUT_ITPXDP_P	E43	
GPD8/SUSCLK	BA17	OUT
XTAL24_IN	E37	IN
XTAL24_OUT	E35	OUT
XCLK_BIASREF	E42	
RTCX1	AM18	IN
RTCX2	AM20	OUT
SRTCRST*	AN18	
RTCRST*	AM16	

CLOCK SIGNALS: CLKOUT_PCIE_N0, CLKOUT_PCIE_P0, GPP_B5/SRCCLKREQ0*, CLKOUT_PCIE_N1, CLKOUT_PCIE_P1, GPP_B6/SRCCLKREQ1*, CLKOUT_PCIE_N2, CLKOUT_PCIE_P2, GPP_B7/SRCCLKREQ2*, CLKOUT_PCIE_N3, CLKOUT_PCIE_P3, GPP_B8/SRCCLKREQ3*, CLKOUT_PCIE_N4, CLKOUT_PCIE_P4, GPP_B9/SRCCLKREQ4*, CLKOUT_PCIE_N5, CLKOUT_PCIE_P5, GPP_B10/SRCCLKREQ5*

=PP1V_SUS_PCH_VCCAPLL — R1520 2.7K 1% 1/20W MF 201 (PLACE_NEAR=U0500.E42:2.54mm)

=PP3V_G3H_PCH_VCCRTC — R1530 20K 1% 1/20W MF 201, R1531 20K 1% 1/20W MF 201

C1530 1UF 20% 6.3V X6S-CERM 0201, C1531 1UF 20% 6.3V X6S-CERM 0201

=PP3V3_SUS_PCH_VCCPGPPA — R1550 100K 5% 1/20W MF 201 — SMC_RUNTIME_SCI_L

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH PCIE/USB/CLKS

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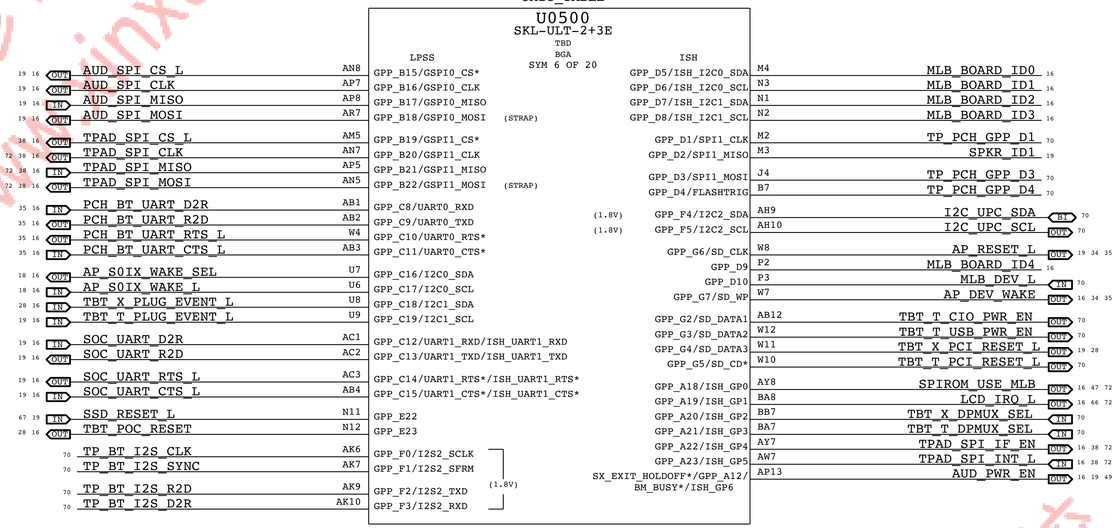
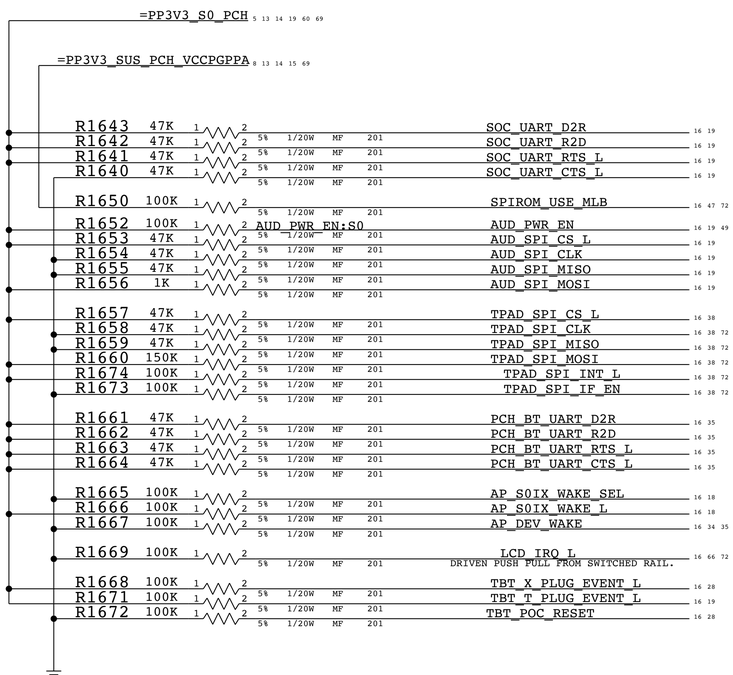
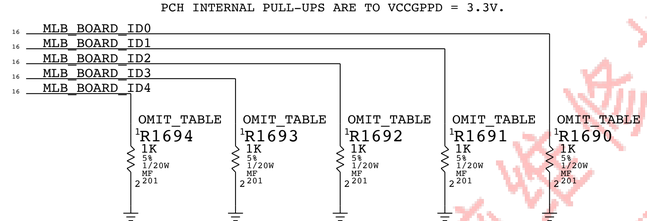
ALL GPP_F* PINS ARE 1.8V ONLY!
OMIT_TABLE





MLB ID STRAPS.

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:0	<11111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:1	<11110>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:5	<11010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:6	<11001>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:9	<10110>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:10	<10101>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:11	<10100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1694	BOARD_ID:16	<01111>

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PCH SPI/UART/GPIO

Apple Inc.

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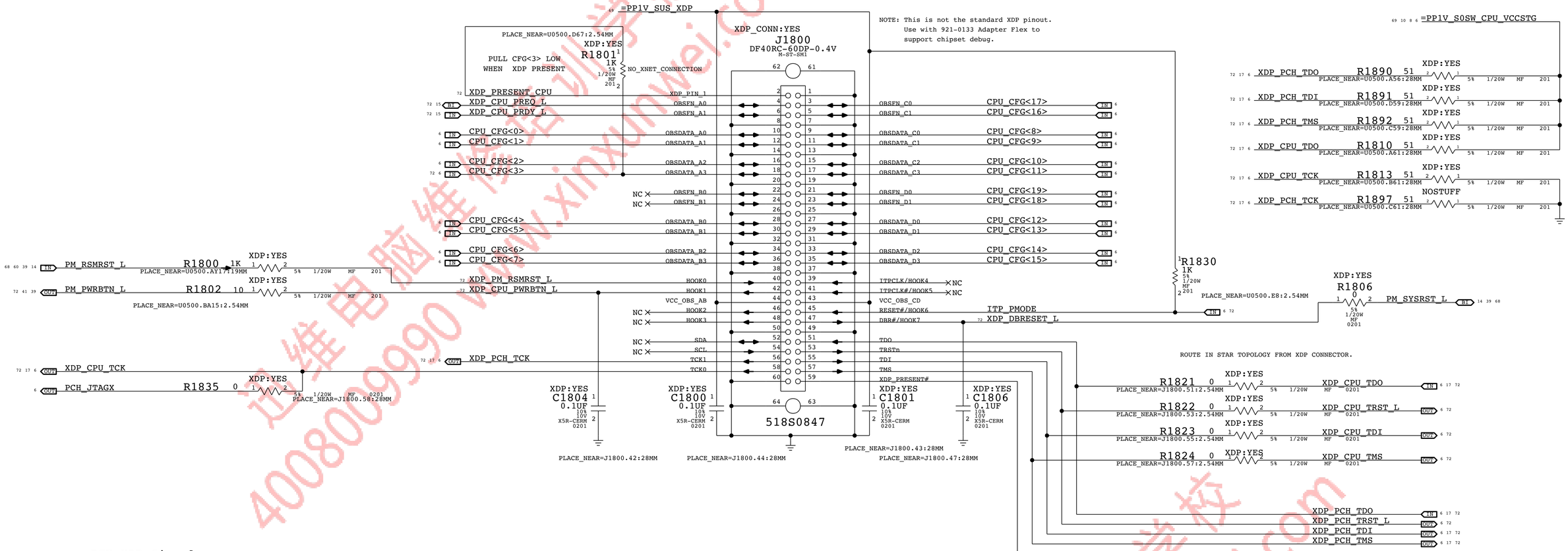
Primary / Merged (CPU/PCH) Micro2-XDP



PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals			Non-XDP Signals
XDP_JTAG_ISP_TCK	MAKE_BASE=TRUE		JTAG_ISP_TCK
XDP_JTAG_ISP_TDI	MAKE_BASE=TRUE		JTAG_ISP_TDI
XDP_PCH_OBSDATA_A2		TP1870	
XDP_PCH_OBSDATA_A3		TP1871	
XDP_PCH_OBSDATA_B0		TP1872	
XDP_PCH_OBSDATA_C0		TP1873	
XDP_PCH_OBSDATA_C1		TP1874	
XDP_PCH_OBSDATA_C2		TP1875	
XDP_PCH_OBSDATA_C3		TP1876	
XDP_PCH_OBSDATA_D0		TP1877	
XDP_PCH_OBSDATA_D1		TP1878	
XDP_PCH_OBSDATA_D2		TP1879	
XDP_PCH_OBSDATA_D3		TP1880	
XDP_PCH_OBSFN_C1		TP1881	
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE		USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE		USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	MAKE_BASE=TRUE		USB_EXTC_OC_L
XDP_USB_EXTD_OC_L	MAKE_BASE=TRUE		USB_EXTD_OC_L

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE: CPU/PCH Merged XDP

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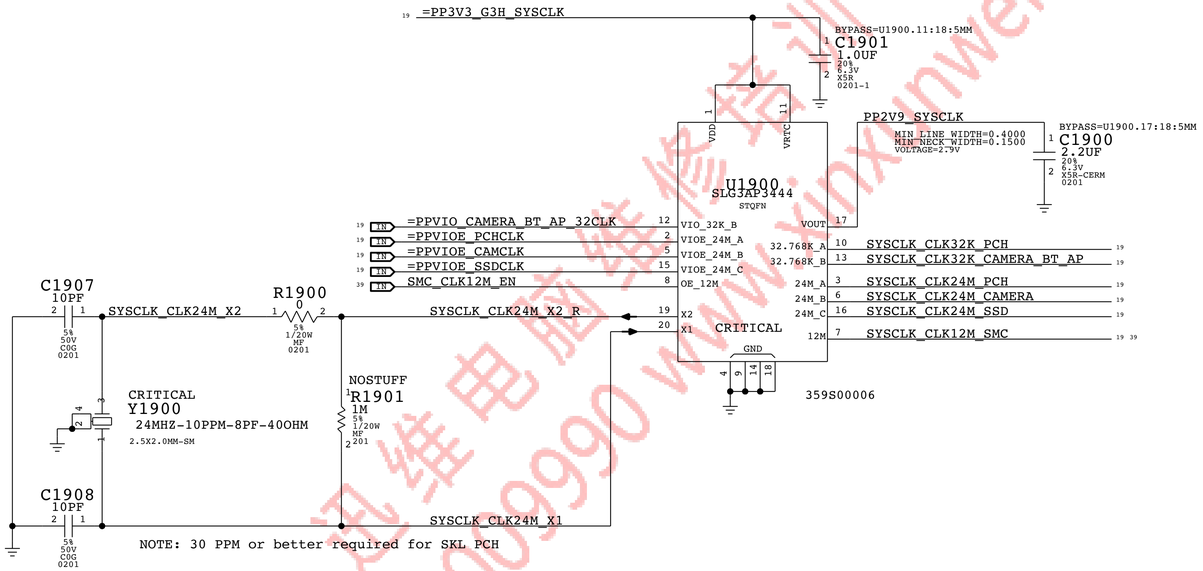
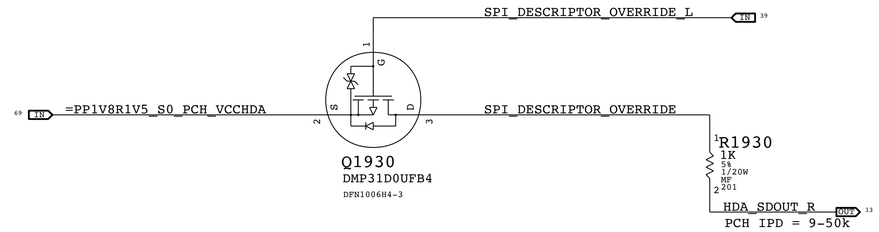
System 32kHz / 12MHz / 24MHz Clock Generator

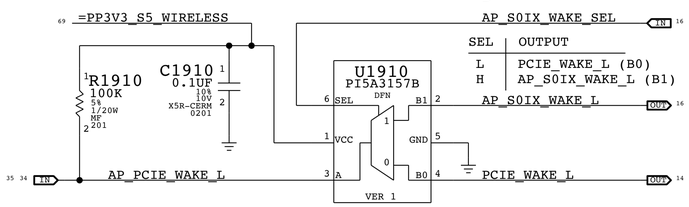


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

BOM_COST_GROUP=CPU & CHIPSET

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OPTION STRAPS

PROJECT DEPENDANT

STUFF PULL-UPS TO ENABLE INTERNAL GPU DP PORTS.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWNS TO DISABLE.

=PP3V3_S0_PCH

R2020 2.2K 5% 1/20W MF 201 — IG_DDI1_EN — (STRAP-OPTION) — PCH_DDPB_CTRLDATA
R2021 2.2K 5% 1/20W MF 201 — IG_DDI2_EN — (STRAP-OPTION) — PCH_DDPC_CTRLDATA

=PP3V3_SUS_PCH_VCCPGPPB

STUFF PULL-UP TO ENABLE BSSB (DCI) CLK/DI ON GPP_D11, _D12.
NOSTUFF / DELETE TO ALLOW INTERNAL PULL-DOWN FOR BSSB ON USB-SS.

R2022 1K 5% 1/20W MF 201 — BSSB_ON_GPIOS — (STRAP-OPTION) — PCH_STRP_BSSB_SEL_GPIO

GREENCLK CLOCK CONNECTIONS.

=PP3V3_G3H_SYSCLK — PP3V3_G3H

BT_CLK32K:YES
R2030 0 5% 1/20W MF 0201

=PPVIO_CAMERA_BT_AP_32CLK — PPVIO_BT_AP_32CLK (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800) — =PP3V3_S4_WLAN

BT_CLK32K:NO
R2031 100K 5% 1/20W MF 201

=PPVIOE_SSDCLK — PD_PPVIOE_SSDCLK (MAKE_BASE=TRUE)

XW2000 SM

=PPVIOE_CAMCLK — PPVIOE_CAMCLK (MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800) — =PPVDDIO_S0_CAMCLK

XW2002 SM

PCH 24MHz VIOE Options

XW2065 SM

PP1V_S5G — PP1V_S5G_PCHCLK (VOLTAGE=1V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800)

PCH24M:SUS
R2065 0 5% 1/20W MF 0201 — =PPVIOE_PCHCLK
PP1V_SUSRS0SW_PCHCLK (VOLTAGE=1V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800, MAKE_BASE=TRUE)

PCH24M:S0SW
R2066 0 5% 1/20W MF 0201 — PP1V_S0SW_PCHCLK (VOLTAGE=1V, MIN_LINE_WIDTH=0.1000, MIN_NECK_WIDTH=0.0800)

Q2065 CRITICAL
DMN32D2LFB4 (SYM VER 3, DFN1006H4-3)
PM_SLP_S0S3_L

=PPVIO_CAMERA_BT_AP_32CLK
=PPVIOE_PCHCLK
=PPVIOE_CAMCLK

BYPASS=U1900.12:18:5MM
BYPASS=U1900.02:18:5MM
BYPASS=U1900.05:18:5MM

C2004 0.1UF 10% 10V X5R-CERM 0201
C2005 0.1UF 10% 10V X5R-CERM 0201
C2006 0.1UF 10% 10V X5R-CERM 0201

SYSCLK_CLK32K_PCH — PCH_CLK32K_RTCX1
TP_PCH_CLK32K_RTCX2 — PCH_CLK32K_RTCX2

BT_CLK32K:YES
R2032 0 5% 1/20W MF 0201

SYSCLK_CLK32K_CAMERA_BT_AP — SYSCLK_CLK32K_BT_AP
SYSCLK_CLK32K_BT_AP_R (MAKE_BASE=TRUE)

SYSCLK_CLK24M_PCH — PCH_CLK24M_XTALIN
TP_PCH_CLK24M_XTALOUT — PCH_CLK24M_XTALOUT

SYSCLK_CLK24M_SSD — TP_SYSCLK_CLK24M_SSD

SYSCLK_CLK24M_CAMERA — CLK25M_CAM_CLKP

SYSCLK_CLK12M_SMC

=PP3V3_S0_PCH

R2071 47K 5% 1/20W MF 201 — SSD_CLKREQ_L
R2072 47K 5% 1/20W MF 201 — TBT_X_CLKREQ_L
R2074 47K 5% 1/20W MF 201 — AP_CLKREQ_L
R2075 47K 5% 1/20W MF 201 — CAMERA_CLKREQ_L

SERIES R FOR VOLTAGE DIVIDER WHEN PCH IS DRIVING IN L1 SUB-STATE.

=SSD_CLKREQ_L — SSD_CLKREQ_R_L (MAKE_BASE=TRUE) — R2001 1K 1/20W 5% 201 MF — SSD_CLKREQ_L
=AP_CLKREQ_L — AP_CLKREQ_R_L (MAKE_BASE=TRUE) — R2002 1K 1/20W 5% 201 MF — AP_CLKREQ_L
=CAMERA_CLKREQ_L — CAMERA_CLKREQ_R_L (MAKE_BASE=TRUE) — R2003 1K 1/20W 5% 201 MF — CAMERA_CLKREQ_L
=TBT_X_CLKREQ_L — TBT_X_CLKREQ_R_L (MAKE_BASE=TRUE) — R2004 1K 1/20W 5% 201 MF — TBT_X_CLKREQ_L

UNUSED PCH XDP SIGNALS NEED TEST POINTS.

JTAG_ISP_TCK — TP2070
JTAG_ISP_TDI — TP2071
USB_EXTD_OC_L — TP2072
USB_EXTC_OC_L — TP2073

EXTRA BPM TESTPOINTS

XDP_BPM_L<1> — TP_XDP_BPM_L<1>
XDP_BPM_L<2> — TP_XDP_BPM_L<2>
XDP_BPM_L<3> — TP_XDP_BPM_L<3>

IFDIM TRIGGERS USING R2055 & R2056 PADS
ASK DC/DC GROUP FOR DETAILS.

XDP_BPM_L<0> — R2055 100K 5% 1/16W MF-LF 402 — NOSTUFF
TP_CPU_RSVD_AK13 — CPU_RSVD_AK13 — R2056 100K 5% 1/16W MF-LF 402 — NOSTUFF

UNUSED GPIO SIGNALS

SOC_UART_D2R — PU_SOC_UART_D2R
SOC_UART_R2D — PU_SOC_UART_R2D
SOC_UART_RTS_L — PU_SOC_UART_RTS_L
SOC_UART_CTS_L — PD_SOC_UART_CTS_L
TBT_T_PLUG_EVENT_L — PU_TBT_T_PLUG_EVENT_L
PCH_SWD_CLK — PU_PCH_SWD_CLK
PCH_SWD_IO — PU_PCH_SWD_IO
PCH_SWD_MUX_SEL — PD_PCH_SWD_MUX_SEL
LCD_PSR_EN — PD_LCD_PSR_EN
AUD_SPI_CS_L — PU_AUD_SPI_CS_L
AUD_SPI_CLK — PD_AUD_SPI_CLK
AUD_SPI_MISO — PD_AUD_SPI_MISO
AUD_SPI_MOSI — PU_AUD_SPI_MOSI
SPKR_ID0 — TP_SPKR_ID0
SPKR_ID1 — TP_SPKR_ID1

CAMERA_PWR_EN_PCH — R2060 0 5% 1/20W MF 0201 — CAMERA_PWR_EN

=PP3V3_S0_PCH — C2040 0.1UF 10% 10V X5R-CERM 0201

=PP1V_S3_CPU_VCCST — R2061 51 5% 1/20W MF 201 — CPU_CATERR_L

CRITICAL
U2040 74LVC1G08 SOT891

PM_PCH_PWROK — PM_PCH_PWROK_BUF

R2040 100K 5% 1/20W MF 201 — CAMERA_PWR_EN
R2041 100K 5% 1/20W MF 201 — AUD_PWR_EN

SOC_S2R_L — SOC_WAKE_L

BOM_COST_GROUP=CPU & CHIPSET

RESETS

PLT_RST_L

R2014 470K 5% 1/20W MF 201

R2010 100K 5% 1/20W MF 201 — CAMERA_RESET_L
R2011 100K 5% 1/20W MF 201 — AP_RESET_L
R2012 100K 5% 1/20W MF 201 — SSD_RESET_L
R2013 100K 5% 1/20W MF 201 — TBT_X_PCI_RESET_L
R2015 33 5% 1/20W MF 201 — SMC_LRESET_L

PM_PLT_RST_TBT_X_L — TBT_X_PCI_RESET_L (MAKE_BASE=TRUE)

S3X SSD CONTROL

PCH — S3X SSD DOWN

SSD_PWR_REQ — STORAGE_LATCH (MAKE_BASE=TRUE)

UNUSED GPIO SIGNALS

SOC_ALS_UART_R2D — PU_SSD_UART_R2D
SOC_ALS_UART_D2R — PU_SSD_UART_D2R
PCH_UART2_CTS_L — PD_SSD_UART_CTS_L

PROBE POINTS

PCIE_TBT_X_R2D_C_P<0>
PCIE_TBT_X_R2D_C_N<0>

NO_XNET_CONNECTION=1
NOSTUFF
PLACE_NEAR=C3040.1:1MM
C2090 0.22UF 20% 6.3V X5R 0201 — TBTXR2DP0 (PLACE_NEAR=C2090.2:1MM) — R2090 51 5% 1/20W MF 201 — NOSTUFF
C2091 0.22UF 20% 6.3V X5R 0201 — TBTXR2DN0 (PLACE_NEAR=C3040.1:1MM) — R2091 51 5% 1/20W MF 201 — NOSTUFF

DP_X_SNK1_ML_C_P<0>
DP_X_SNK1_ML_C_N<0>

NO_XNET_CONNECTION=1
NOSTUFF
PLACE_NEAR=C3040.1:1MM
C2092 0.1UF 10% 16V X5R-CERM 0201 — DPX1P0 (PLACE_NEAR=C2090.2:6MM) — R2092 51 5% 1/20W MF 201 — NOSTUFF
C2093 0.1UF 10% 16V X5R-CERM 0201 — DPX1N0 (PLACE_NEAR=C2090.2:5MM) — R2093 51 5% 1/20W MF 201 — NOSTUFF

DESIGN: X502/MLB CATZ
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Chipset Support 2

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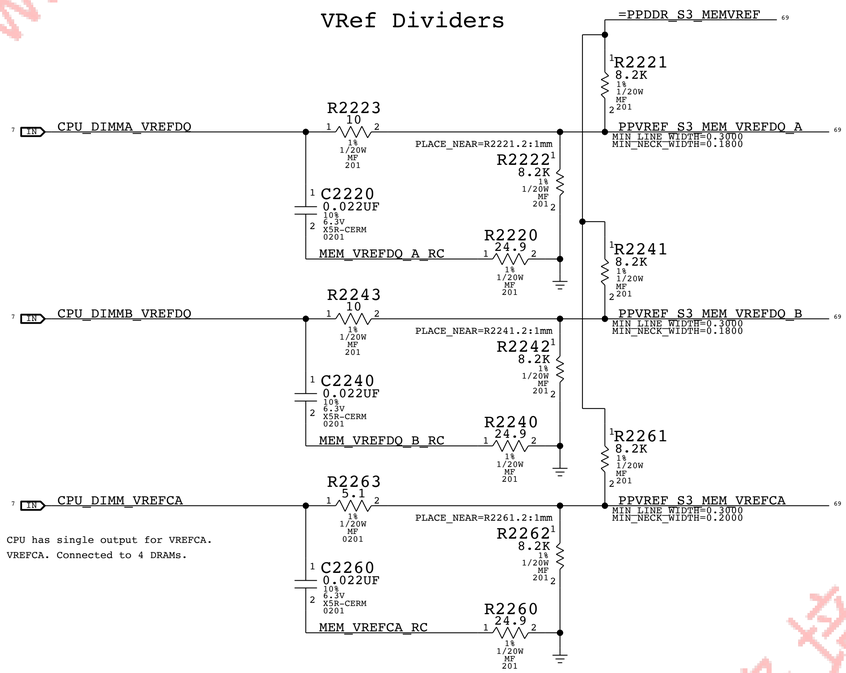
CPU-Based Margining

VRef Dividers



NOTE: CPU has single output for VREFCA.
VREFCA. Connected to 4 DRAMs.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 VREF Margining

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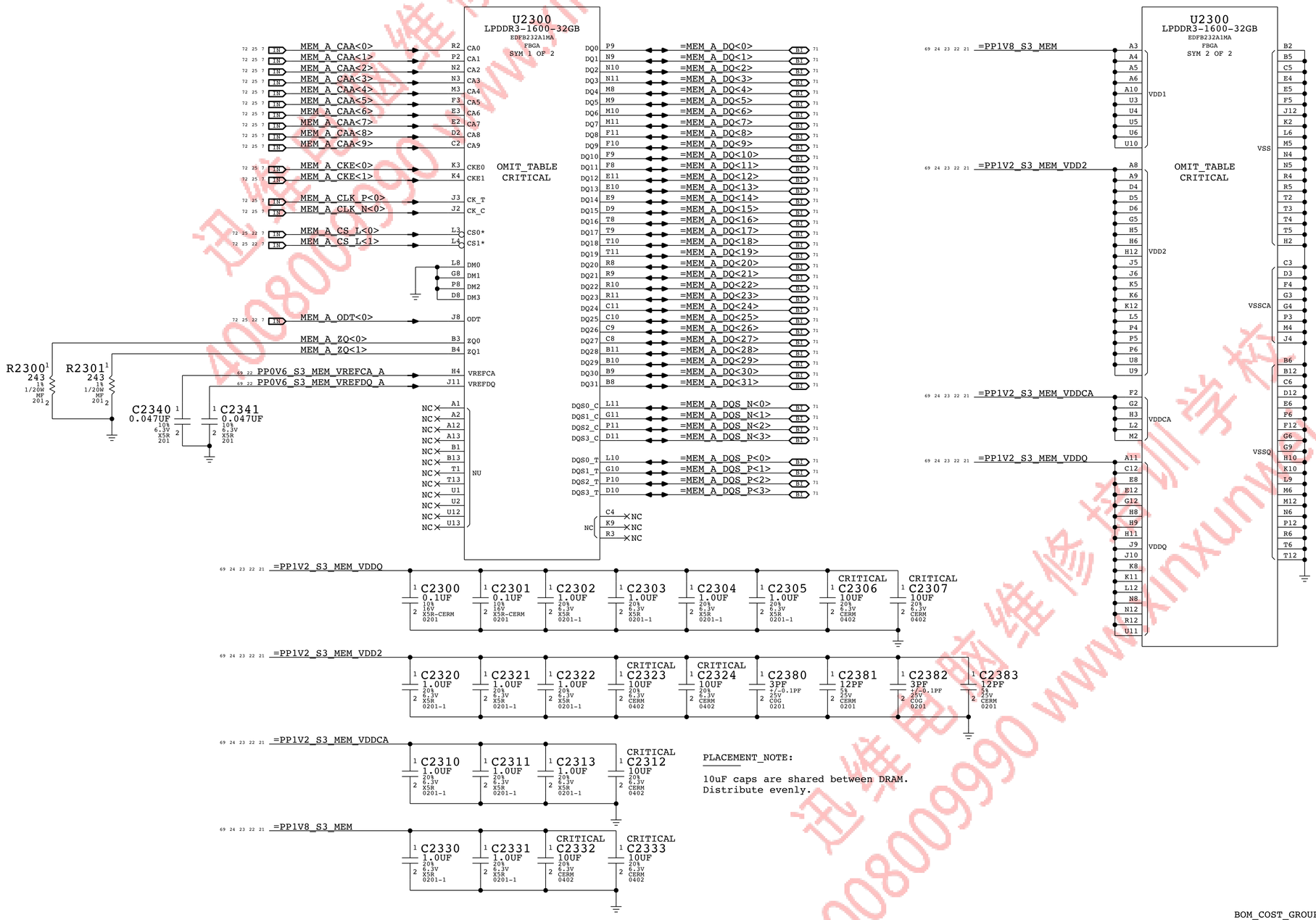
LPDDR3 CHANNEL A (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
PAGE TITLE	LPDDR3 DRAM Channel A (00-31)
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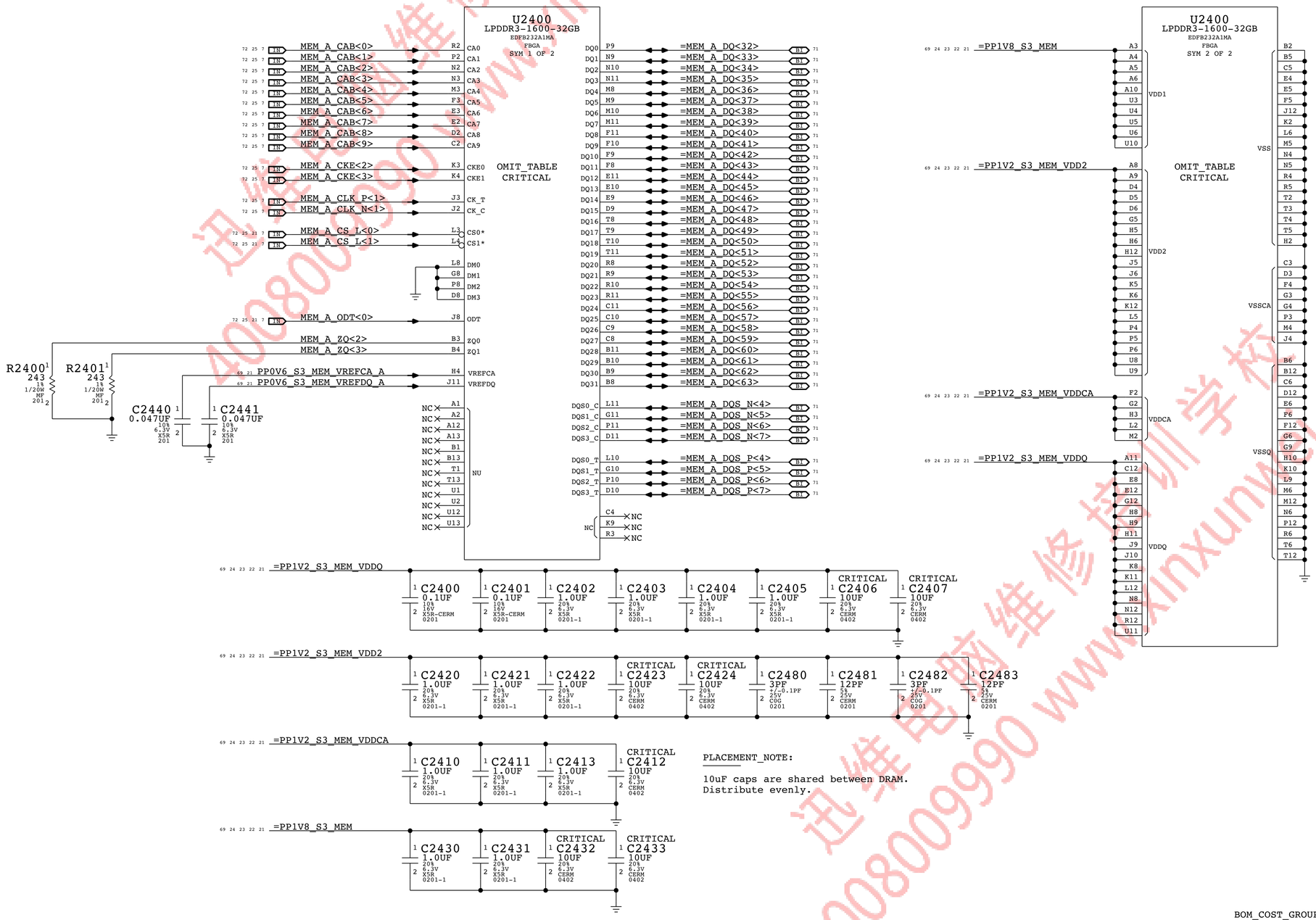
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
PAGE TITLE	LPDDR3 DRAM Channel A (32-63)
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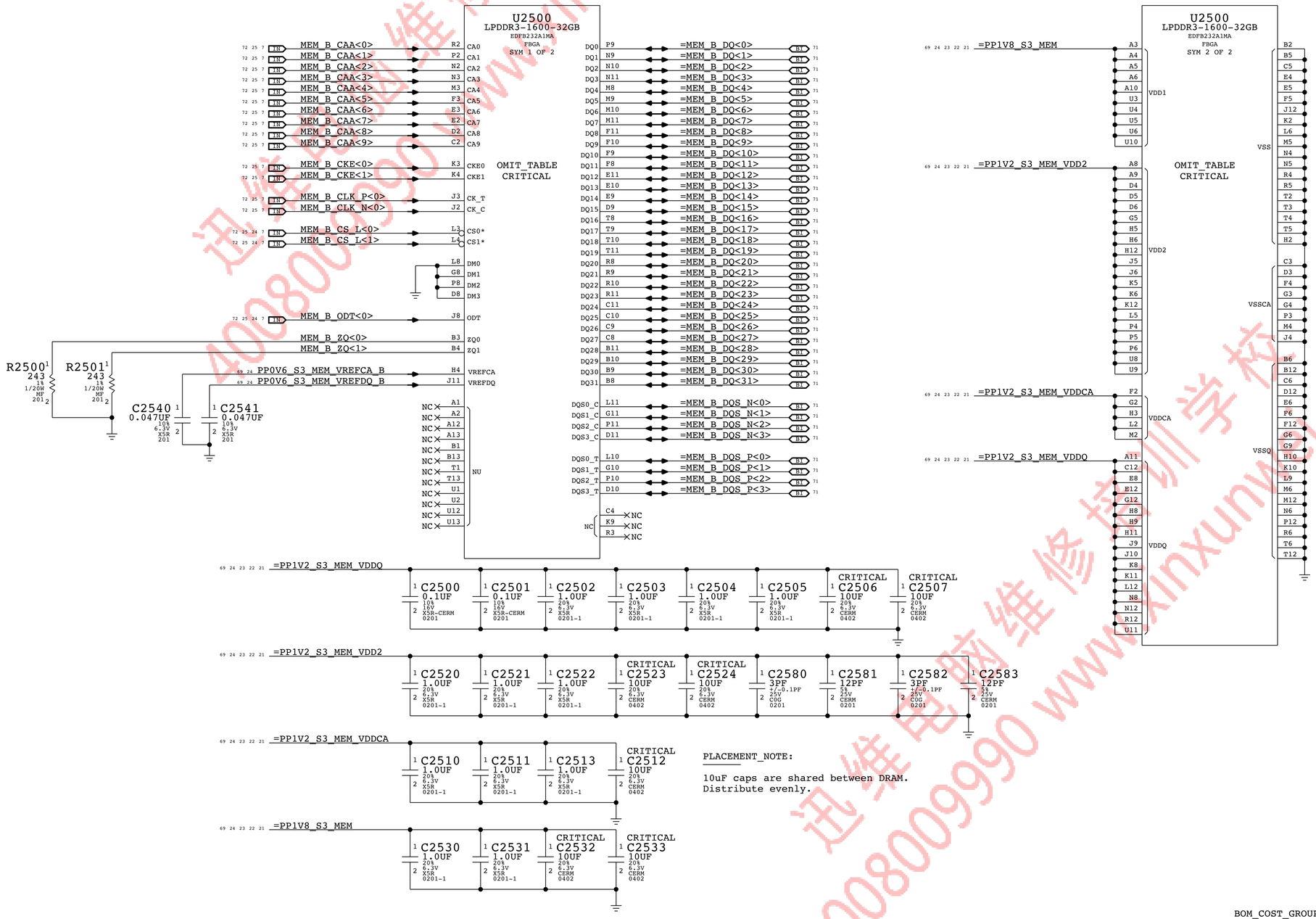
LPDDR3 CHANNEL B (0-31)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE
LPDDR3 DRAM Channel B (00-31)

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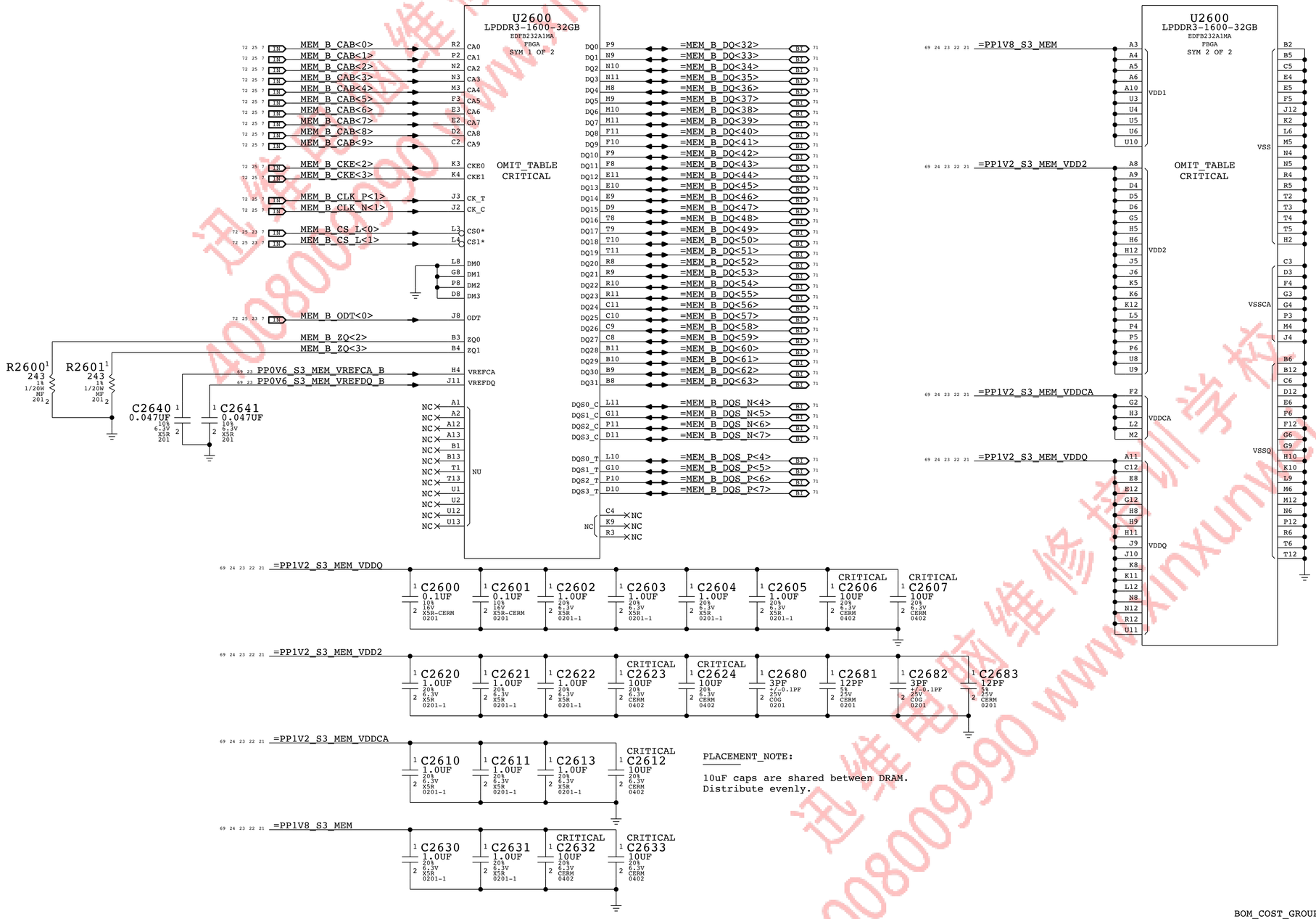
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP	SYNC_DATE=12/03/2015
PAGE TITLE	LPDDR3 DRAM Channel B (32-63)
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Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

69 =PP0V6_S0_MEM_VTT_A

72 21 7	IN	MEM_A_CAA<9>	R2700	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<8>	R2701	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<6>	R2702	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<7>	R2703	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<5>	R2704	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CLK_P<0>	R2705	39	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CLK_N<0>	R2706	39	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CKE<1>	R2707	82	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CKE<0>	R2708	82	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<4>	R2709	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<3>	R2710	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<2>	R2711	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<1>	R2712	68	1%	1/20W	201	MF	
72 21 7	IN	MEM_A_CAA<0>	R2713	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<9>	R2714	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<8>	R2715	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<6>	R2716	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<7>	R2717	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<5>	R2718	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CLK_P<1>	R2719	39	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CLK_N<1>	R2720	39	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CKE<2>	R2721	82	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CKE<3>	R2722	82	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<4>	R2723	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<2>	R2724	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<3>	R2725	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<1>	R2726	68	1%	1/20W	201	MF	
72 22 7	IN	MEM_A_CAB<0>	R2727	68	1%	1/20W	201	MF	
72 22 21 7	IN	MEM_A_CS_L<0>	R2728	82	1%	1/20W	201	MF	
72 22 21 7	IN	MEM_A_CS_L<1>	R2729	82	1%	1/20W	201	MF	
72 22 21 7	IN	MEM_A_ODT<0>	R2730	82	1%	1/20W	201	MF	

C2700	0.47UF 20% 4V CERM-X5R-1 201	
C2730	12PF 5% 25V CERM 0201	
C2701	0.47UF 20% 4V CERM-X5R-1 201	
C2702	0.47UF 20% 4V CERM-X5R-1 201	
C2703	0.47UF 20% 4V CERM-X5R-1 201	
C2704	0.47UF 20% 4V CERM-X5R-1 201	
C2705	0.47UF 20% 4V CERM-X5R-1 201	
C2706	0.47UF 20% 4V CERM-X5R-1 201	
C2707	0.47UF 20% 4V CERM-X5R-1 201	
C2708	0.47UF 20% 4V CERM-X5R-1 201	
C2709	0.47UF 20% 4V CERM-X5R-1 201	
C2722	3PF +/-0.1PF 25V C0G 0201	
C2720	20UF 20% 6.3V CERM-X5R 0402	CRITICAL
C2721	20UF 20% 6.3V CERM-X5R 0402	NOSTUFF CRITICAL

69 =PP0V6_S0_MEM_VTT_B

72 23 7	IN	MEM_B_CAA<9>	R2740	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<8>	R2741	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<7>	R2742	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<6>	R2743	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<5>	R2744	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CLK_P<0>	R2745	39	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CLK_N<0>	R2746	39	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CKE<1>	R2747	82	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CKE<0>	R2748	82	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<4>	R2749	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<2>	R2750	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<3>	R2751	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<1>	R2752	68	1%	1/20W	201	MF	
72 23 7	IN	MEM_B_CAA<0>	R2753	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<9>	R2754	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<8>	R2755	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<7>	R2756	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<6>	R2757	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<5>	R2758	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CLK_N<1>	R2759	39	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CLK_P<1>	R2760	39	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CKE<2>	R2761	82	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CKE<3>	R2762	82	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<4>	R2763	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<2>	R2764	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<3>	R2765	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<1>	R2766	68	1%	1/20W	201	MF	
72 24 7	IN	MEM_B_CAB<0>	R2767	68	1%	1/20W	201	MF	
72 24 23 7	IN	MEM_B_CS_L<0>	R2768	82	1%	1/20W	201	MF	
72 24 23 7	IN	MEM_B_CS_L<1>	R2769	82	1%	1/20W	201	MF	
72 24 23 7	IN	MEM_B_ODT<0>	R2770	82	1%	1/20W	201	MF	

C2710	0.47UF 20% 4V CERM-X5R-1 201	
C2731	12PF 5% 25V CERM 0201	
C2711	0.47UF 20% 4V CERM-X5R-1 201	
C2712	0.47UF 20% 4V CERM-X5R-1 201	
C2713	0.47UF 20% 4V CERM-X5R-1 201	
C2714	0.47UF 20% 4V CERM-X5R-1 201	
C2715	0.47UF 20% 4V CERM-X5R-1 201	
C2716	0.47UF 20% 4V CERM-X5R-1 201	
C2717	0.47UF 20% 4V CERM-X5R-1 201	
C2718	0.47UF 20% 4V CERM-X5R-1 201	
C2719	0.47UF 20% 4V CERM-X5R-1 201	
C2742	3PF +/-0.1PF 25V C0G 0201	
C2740	20UF 20% 6.3V CERM-X5R 0402	CRITICAL
C2741	20UF 20% 6.3V CERM-X5R 0402	NOSTUFF CRITICAL

BOM_COST_GROUP=DRAM

SYNC_MASTER=X502-EXP SYNC_DATE=12/03/2015

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D

REVISION 1.0.0

BRANCH

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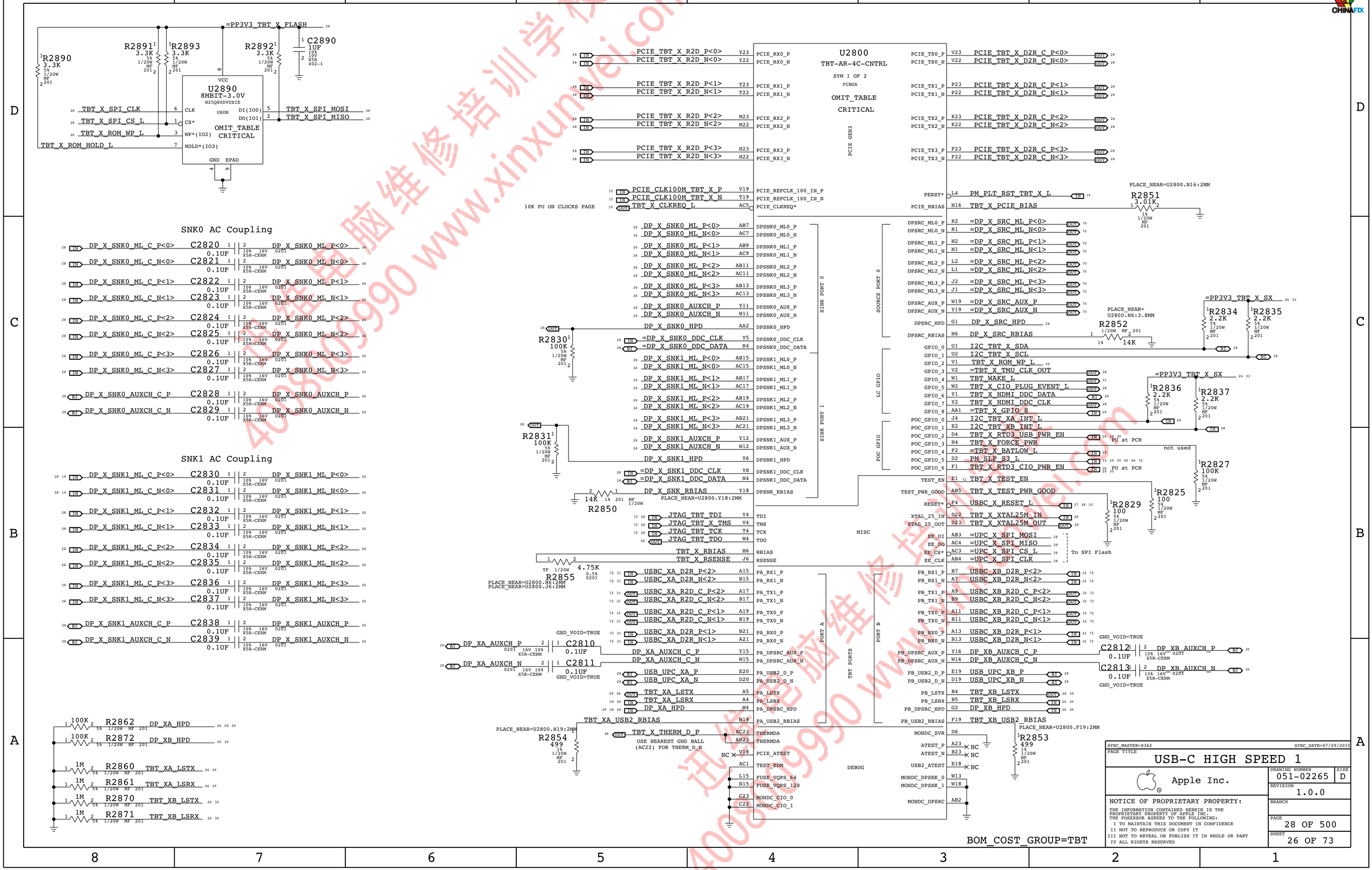
=PP3V3_TBT_X_FLASH
R2890 3.3K 5% 1/20W MF 201
R2891 3.3K 5% 1/20W MF 201
R2893 3.3K 5% 1/20W MF 201
R2892 3.3K 5% 1/20W MF 201
C2890 1UF 10% 10V X5R 402-1
U2890 8MBIT-3.0V W25Q80DVUXIE USON
OMIT_TABLE CRITICAL
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_ROM_WP_L
TBT_X_ROM_HOLD_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
U2800 TBT-AR-4C-CNTRL SYM 1 OF 2 FCBGA
OMIT_TABLE CRITICAL
PCIE GEN3
10K PU ON CLOCKS PAGE
PLACE_NEAR=U2800.N16:2MM
R2851 3.01K 1% 1/20W MF 201
PLACE_NEAR=U2800.N6:3.8MM
R2852 14K 1% 1/20W MF 201
R2830 100K 5% 1/20W MF 201
R2831 100K 5% 1/20W MF 201
R2850 14K 1% 1/20W MF 201
PLACE_NEAR=U2800.Y18:2MM
R2855 4.75K 0.5% 0201
PLACE_NEAR=U2800.H6:2MM
PLACE_NEAR=U2800.J6:2MM
R2854 499 1% 1/20W MF 201
USE NEAREST GND BALL (AC22) FOR THERM_D_N
R2853 499 1% 1/20W MF 201
PLACE_NEAR=U2800.F19:2MM
R2834 2.2K 5% 1/20W MF 201
R2835 2.2K 5% 1/20W MF 201
R2836 2.2K 5% 1/20W MF 201
R2837 2.2K 5% 1/20W MF 201
R2827 100K 5% 1/20W MF 201
R2829 100 5% 1/20W MF 201
R2825 100 5% 1/20W MF 201
PU at PCH
not used
To SPI Flash
SNK0 AC Coupling
SNK1 AC Coupling
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
LC GPIO
POC GPIO
MISC
TBT PORTS
PORT A
PORT B
DEBUG
R2862 100K DP_XA_HPD
R2872 100K DP_XB_HPD
R2860 1M TBT_XA_LSTX
R2861 1M TBT_XA_LSRX
R2870 1M TBT_XB_LSTX
R2871 1M TBT_XB_LSRX
BOM_COST_GROUP=TBT
SYNC_MASTER=X362
SYNC_DATE=07/29/2015
PAGE TITLE
USB-C HIGH SPEED 1
Apple Inc.
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REVISION 1.0.0
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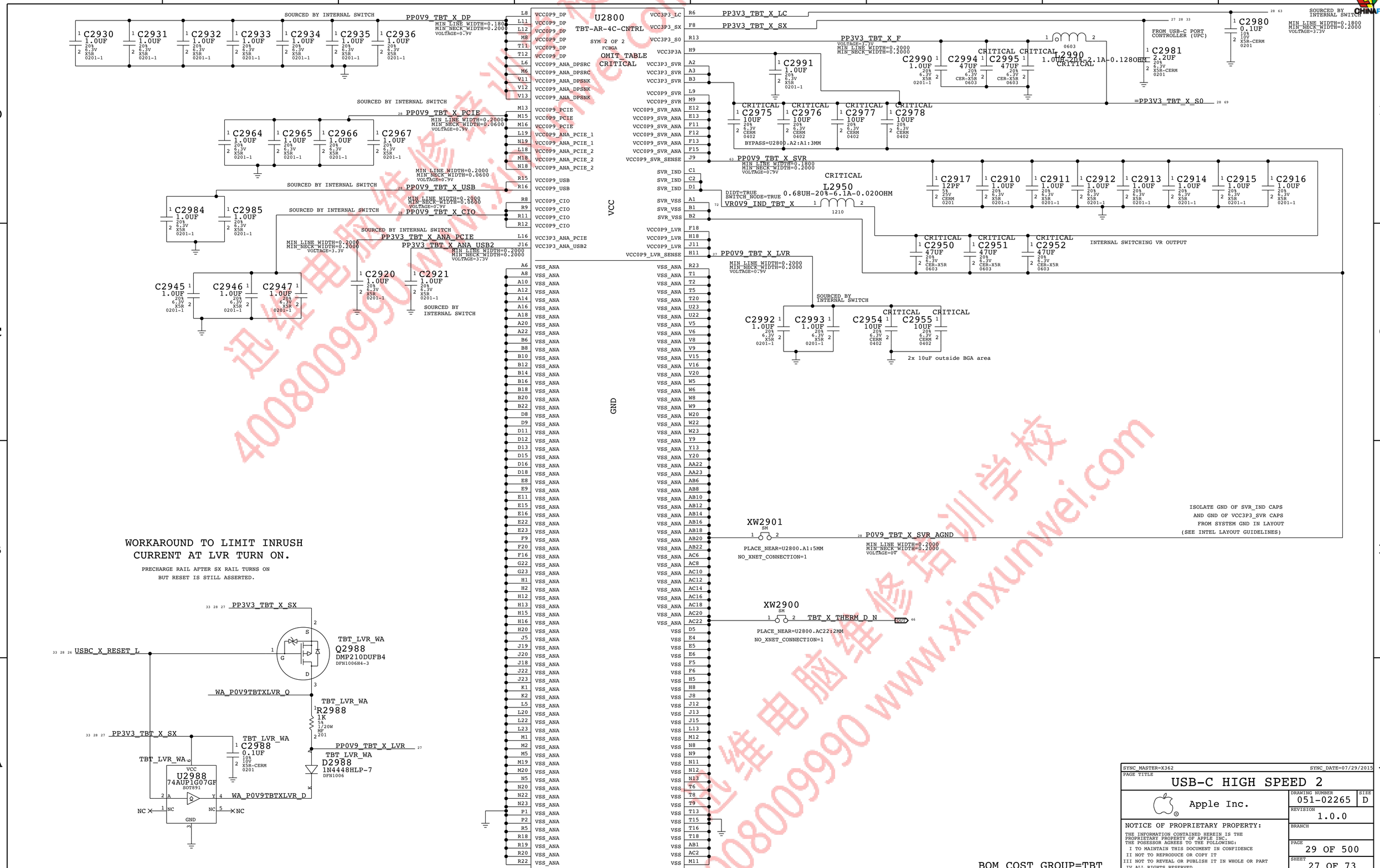

SYNC_MASTER=X362 SYNC_DATE=07/29/2015

PAGE TITLE

USB-C HIGH SPEED 2

Apple Inc.

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RIDGE AC COUPLING

R2D

PCIE_TBT_X_R2D_C_P<0>	C3040	0.22UF	PCIE_TBT_X_R2D_P<0>	
PCIE_TBT_X_R2D_C_N<0>	C3041	0.22UF	PCIE_TBT_X_R2D_N<0>	
PCIE_TBT_X_R2D_C_P<1>	C3042	0.22UF	PCIE_TBT_X_R2D_P<1>	
PCIE_TBT_X_R2D_C_N<1>	C3043	0.22UF	PCIE_TBT_X_R2D_N<1>	
PCIE_TBT_X_R2D_C_P<2>	C3044	0.22UF	PCIE_TBT_X_R2D_P<2>	TBT_PCIE_4LANES
PCIE_TBT_X_R2D_C_N<2>	C3045	0.22UF	PCIE_TBT_X_R2D_N<2>	TBT_PCIE_4LANES
PCIE_TBT_X_R2D_C_P<3>	C3046	0.22UF	PCIE_TBT_X_R2D_P<3>	TBT_PCIE_4LANES
PCIE_TBT_X_R2D_C_N<3>	C3047	0.22UF	PCIE_TBT_X_R2D_N<3>	TBT_PCIE_4LANES

D2R

PCIE_TBT_X_D2R_C_P<0>	C3050	0.22UF	PCIE_TBT_X_D2R_P<0>	
PCIE_TBT_X_D2R_C_N<0>	C3051	0.22UF	PCIE_TBT_X_D2R_N<0>	
PCIE_TBT_X_D2R_C_P<1>	C3052	0.22UF	PCIE_TBT_X_D2R_P<1>	
PCIE_TBT_X_D2R_C_N<1>	C3053	0.22UF	PCIE_TBT_X_D2R_N<1>	
PCIE_TBT_X_D2R_C_P<2>	C3055	0.22UF	PCIE_TBT_X_D2R_P<2>	TBT_PCIE_4LANES
PCIE_TBT_X_D2R_C_N<2>	C3056	0.22UF	PCIE_TBT_X_D2R_N<2>	TBT_PCIE_4LANES
PCIE_TBT_X_D2R_C_P<3>	C3057	0.22UF	PCIE_TBT_X_D2R_P<3>	TBT_PCIE_4LANES
PCIE_TBT_X_D2R_C_N<3>	C3054	0.22UF	PCIE_TBT_X_D2R_N<3>	TBT_PCIE_4LANES

ACE RPD STRAPPING

CONNECT G1/G2 TO CC1/CC2 TO RECEIVE POWER UNDER DB CASE
CONNECT G1/G2 TO GND TO NOT RECEIVE POWER UNDER DB CASE

USBC_XA_RPD_G1	R3026	0	USBC_XA_CC1
USBC_XA_RPD_G2	R3022	0	USBC_XA_CC2
USBC_XB_RPD_G1	R3011	0	USBC_XB_CC1
USBC_XB_RPD_G2	R3024	0	USBC_XB_CC2

ACE BUSPOWERZ STRAPPING

R3017	0	UPC_XA_BUSPOWERZ
R3019	0	UPC_XB_BUSPOWERZ

PU BUSPOWERZ TO LDO_3V3 TO NOT PASS VBUS TO SYS UNDER DB CASE

PU BUSPOWERZ TO 1V8D TO PASS VBUS TO SYS UNDER DB CASE USES INT POWER PATH

GND BUSPOWERZ TO PASS VBUS TO SYS UNDER DB CASE USES EXT POWER PATH

RIDGE DEBUG CONN

J3099 505070-1220 M-ST-SM UPC_DBG_HDR

TBT_X_CIO_PLUG_EVENT_L	1	2	TBT_X_PCI_RESET_L
DP_X_SNK0_HPD	3	4	USBC_X_RESET_L
ARKANOID_P5	5	6	PP3V3_TBT_X_SX
ARKANOID_P7	7	8	PP0V9_TBT_X_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_X_USB
PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO
	15	16	

516S00115

ACE DEBUG CONN

J3098 505070-1220 M-ST-SM UPC_DBG_HDR

I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L
=I2C_UPC_XA_SCL2	3	4	I2C_TBT_X_SDA
=I2C_UPC_XA_SDA2	5	6	I2C_TBT_X_SCL
SMC_USBC_INT_L	7	8	I2C_UPC_XA_DBG_CTL_SDA
TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_TX	11	12	UPC_XA_UART_RX
	15	16	

516S00115

DP_X_SNK1_HPD	ARKANOID:HPD	R3080	ARKANOID_P5
SMC_DEBUGPRT_RX_L	ARKANOID:MOJO	R3081	
DP_XA_HPD	ARKANOID:HPD	R3082	ARKANOID_P7
SMC_DEBUGPRT_TX_L	ARKANOID:MOJO	R3083	

F3000 CRITICAL 6AMP-32V-0.0095OHM 0603
=PP20V_USBC_XA_VBUS — PP20V_USBC_XA_VBUS_F

F3010 CRITICAL 6AMP-32V-0.0095OHM 0603
=PP20V_USBC_XB_VBUS — PP20V_USBC_XB_VBUS_F

POWER ALIASES

=PP3V3_G3H_UPC_XA	PP3V3_G3H_UPC_XA	R3000 0	PP3V3_G3H
=PP3V3_G3H_UPC_XB	PP3V3_G3H_UPC_XB	R3001 0	PP3V3_G3H

MAKE_BASE=TRUE; 5% 1/20W MF 0201

=PP20V_USBC_XA_VBUS	MAKE_BASE=TRUE	PP20V_USBC_XA_VBUS
=PP20V_USBC_XB_VBUS	MAKE_BASE=TRUE	PP20V_USBC_XB_VBUS
=UPC_XA_I2C_STRAP	MAKE_BASE=TRUE	PP3V3_UPC_XA_LDO
=PP3V3R1V8_UPC_XA		
=UPC_XB_I2C_STRAP	MAKE_BASE=TRUE	PP3V3_UPC_XB_LDO
=PP3V3_TBT_X_FLASH		
=PP3V3R1V8_UPC_XB		
=PP3V3_TBT_X_S0	MAKE_BASE=TRUE	PP3V3_TBT_X_S0
=PPHV_INT_G3H		

MISC ALIASES

=UPC_X_SPI_CLK	MAKE_BASE=TRUE	UPC_X_SPI_CLK
=UPC_X_SPI_CS_L	MAKE_BASE=TRUE	UPC_X_SPI_CS_L
=UPC_X_SPI_MOSI	MAKE_BASE=TRUE	UPC_X_SPI_MOSI
=UPC_X_SPI_MISO	MAKE_BASE=TRUE	UPC_X_SPI_MISO
USBC_X_POC_RESET	MAKE_BASE=TRUE	TBT_POC_RESET
TBT_X_RTD3_CIO_PWR_EN	MAKE_BASE=TRUE	TBT_X_CIO_PWR_EN
TBT_X_RTD3_USB_PWR_EN	MAKE_BASE=TRUE	TBT_X_USB_PWR_EN
TBT_X_PLUG_EVENT_L	MAKE_BASE=TRUE	TBT_X_CIO_PLUG_EVENT_L
=TBT_X_BATLOW_L	MAKE_BASE=TRUE	PM_BATLOW_L
=USBC_TMS_X_SWD_CLK_X	MAKE_BASE=TRUE	JTAG_TBT_X_TMS
=USBC_TMS_T_SWD_DATA_X	MAKE_BASE=TRUE	PU_USBC_TMS_T_SWD_DATA_X
JTAG_TBT_TDO	MAKE_BASE=TRUE	JTAG_ISP_TDO
=USBC_XA_RESET_L	MAKE_BASE=TRUE	TP_USBC_XA_RESET_L
UPC_XA_SPI_CLK	MAKE_BASE=TRUE	
UPC_XA_SPI_CS_L		
UPC_XA_SPI_MISO		
UPC_XA_SPI_MOSI		
UPC_XA_RESET		
UPC_XB_RESET		

XW3001 SM
PLACE_NEAR=U2800.A1:5MM NO_XNET_CONNECTION=1
P0V9_TBT_X_SVR_AGND — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=0V

I2C_TBT_X_SDA		=I2C_UPC_XA_SDA1
I2C_TBT_X_SCL	UPC XA - U3100	=I2C_UPC_XA_SCL1
I2C_TBT_XA_INT_L	(WRITE: 0X70 READ: 0X71)	=I2C_UPC_XA_INT1_L
I2C_TBT_XB_INT_L		=I2C_UPC_XB_SDA1
TBT - MASTER	UPC XB - U3200	=I2C_UPC_XB_SCL1
ALPINE RIDGE - U2800	(WRITE: 0X7E READ: 0X7F)	=I2C_UPC_XB_INT1_L

TBT_X_SPI_CLK	R3098 100	TBT_X_SPI_CLK_DBG	
TBT_X_SPI_CS_L	R3090 15	UPC_XB_SPI_CLK	
TBT_X_SPI_MOSI	R3091 15	UPC_XB_SPI_CS_L	
TBT_X_SPI_MISO	R3092 15	UPC_XB_SPI_MOSI	
	R3093 15	UPC_XB_SPI_MISO	
	R3094 15	=UPC_X_SPI_CLK	
	R3095 15	=UPC_X_SPI_CS_L	
	R3096 15	=UPC_X_SPI_MOSI	
	R3097 15	=UPC_X_SPI_MISO	

5% 1/20W MF 201

TBT_X_XTAL25M_OUT — NOSTUFF R3006 1M 5% 1/20W MF 201 — TBT_X_XTAL25M_IN
CRITICAL Y3000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
C3002 20PF 5% 25V C0G 0201
C3003 20PF 5% 25V C0G 0201

USB3_EXTA_R2D_C_P	C3020 0.1UF 0201 X5R-CERM 10% 16V	USB3_EXTA_R2D_P	TP3091
USB3_EXTA_R2D_C_N	C3021 0.1UF 0201 X5R-CERM 10% 16V	USB3_EXTA_R2D_N	TP3092
USB3_EXTA_D2R_P			TP3093
USB3_EXTA_D2R_N			TP3094

SM-TPP3

USBC_XA_USB_TOP_P	MAKE_BASE=TRUE	USBC_XA_USB_DBG_TOP_P
USBC_XA_USB_TOP_N	MAKE_BASE=TRUE	USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_BOT_P	MAKE_BASE=TRUE	USBC_XA_USB_DBG_BOT_P
USBC_XA_USB_BOT_N	MAKE_BASE=TRUE	USBC_XA_USB_DBG_BOT_N

CRITICAL L3000 90-OHM-0.1A EXCX4CE 100.1MHz
=USB_UPC_XA_P — USB_UPC_XA_F_P — =USB_UPC_XA_F_P
=USB_UPC_XA_N — USB_UPC_XA_F_N — =USB_UPC_XA_F_N
MAKE_BASE=TRUE; PLACE_NEAR=U3100.L5:5MM

TP_UPC_XB_SWD_CLK — TSP_UPC_XB_SWD_CLK — TP3090

DP / USB SOURCE ALIASES

DP_DDI1_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_P<3..0>
DP_DDI1_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_X_SNK1_ML_C_N<3..0>
DP_DDI1_AUXCH_C_P	MAKE_BASE=TRUE	DP_X_SNK1_AUXCH_C_P
DP_DDI1_AUXCH_C_N	MAKE_BASE=TRUE	DP_X_SNK1_AUXCH_C_N
DP_DDPB_HPD	MAKE_BASE=TRUE	DP_X_SNK1_HPD
DP_DDI2_ML_C_P<3..0>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_P<3..0>
DP_DDI2_ML_C_N<3..0>	MAKE_BASE=TRUE	DP_X_SNK0_ML_C_N<3..0>
DP_DDI2_AUXCH_C_P	MAKE_BASE=TRUE	DP_X_SNK0_AUXCH_C_P
DP_DDI2_AUXCH_C_N	MAKE_BASE=TRUE	DP_X_SNK0_AUXCH_C_N
DP_DDPC_HPD	MAKE_BASE=TRUE	DP_X_SNK0_HPD

USB_EXTB_P	MAKE_BASE=TRUE	USB_UPC_PCH_XA_P	=USB_UPC_XA_P
USB_EXTB_N	MAKE_BASE=TRUE	USB_UPC_PCH_XA_N	=USB_UPC_XA_N
USB_UPC_XA_P	R3012 0		
USB_UPC_XA_N	R3013 0		
UPC_XA_FAULT_L	R3008 0	USB_EXTA_OC_L	
NC_USB2_08P	MAKE_BASE=TRUE	USB_UPC_PCH_XB_P	=USB_UPC_XB_P
NC_USB2_08N	MAKE_BASE=TRUE	USB_UPC_PCH_XB_N	=USB_UPC_XB_N
USB_UPC_XB_P	R3014 0		
USB_UPC_XB_N	R3015 0		
UPC_XB_FAULT_L	R3018 0	USB_EXTB_OC_L	

5% 1/20W MF 0201

PP3V3_TBT_X_LC

R3071 100K	TBT_X_HDMI_DDC_CLK		
R3035 100K	JTAG_TBT_TCK	R3033 0	JTAG_ISP_TCK
R3036 100K	JTAG_TBT_TDI	R3034 0	JTAG_ISP_TDI
R3073 100K	UPC_XA_DBG3		
R3074 100K	UPC_XA_DBG4		
R3072 100K	TBT_X_HDMI_DDC_DATA		
R3066 100K	DP_X_SNK0_DDC_DATA		=DP_X_SNK0_DDC_DATA
R3067 100K	DP_X_SNK0_DDC_CLK		=DP_X_SNK0_DDC_CLK
R3069 100K	DP_X_SNK1_DDC_CLK		=DP_X_SNK1_DDC_CLK
R3070 100K	DP_X_SNK1_DDC_DATA		=DP_X_SNK1_DDC_DATA
R3040 100K	PD_UPC_XA_GPIO5		UPC_XA_HPD_RX
R3041 100K	PD_UPC_XB_GPIO5		UPC_XB_HPD_RX
R3042 100K	PD_UPC_XA_GPIO6		UPC_XA_5V_EN
R3043 100K	PD_UPC_XB_GPIO6		UPC_XB_5V_EN
R3049 100K	PD_TBT_X_TMU_CLK_OUT		=TBT_X_TMU_CLK_OUT
R3050 100K	PD_TBT_X_GPIO_8		=TBT_X_GPIO_8
R3020 1M	DP_X_SRC_HPD		

5% 1/20W MF 201

XPD JTAG ISOLATION

LOCAL BULK CAP

=PP5V_USBC
CRITICAL C3000 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

PD WHEN NOT USED

UPC_XA_DBG1	MAKE_BASE=TRUE	SMC_TCK	
UPC_XA_DBG2	MAKE_BASE=TRUE	SMC_TMS	
UPC_XB_DBG1	MAKE_BASE=TRUE	SSD_JTAG_TCK	
UPC_XB_DBG2	MAKE_BASE=TRUE	SSD_JTAG_TMS	
UPC_XB_DBG3	MAKE_BASE=TRUE	SMC_DEBUGPRT_TX_L	
UPC_XB_DBG4	MAKE_BASE=TRUE	SMC_DEBUGPRT_RX_L	

BOM_COST_GROUP=USB-C

DESIGN: X502/MLB CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016

PAGE TITLE: USB-C SUPPORT

Apple Inc.

DRAWING NUMBER: 051-02265 SIZE: D
REVISION: 1.0.0
BRANCH
PAGE: 30 OF 500
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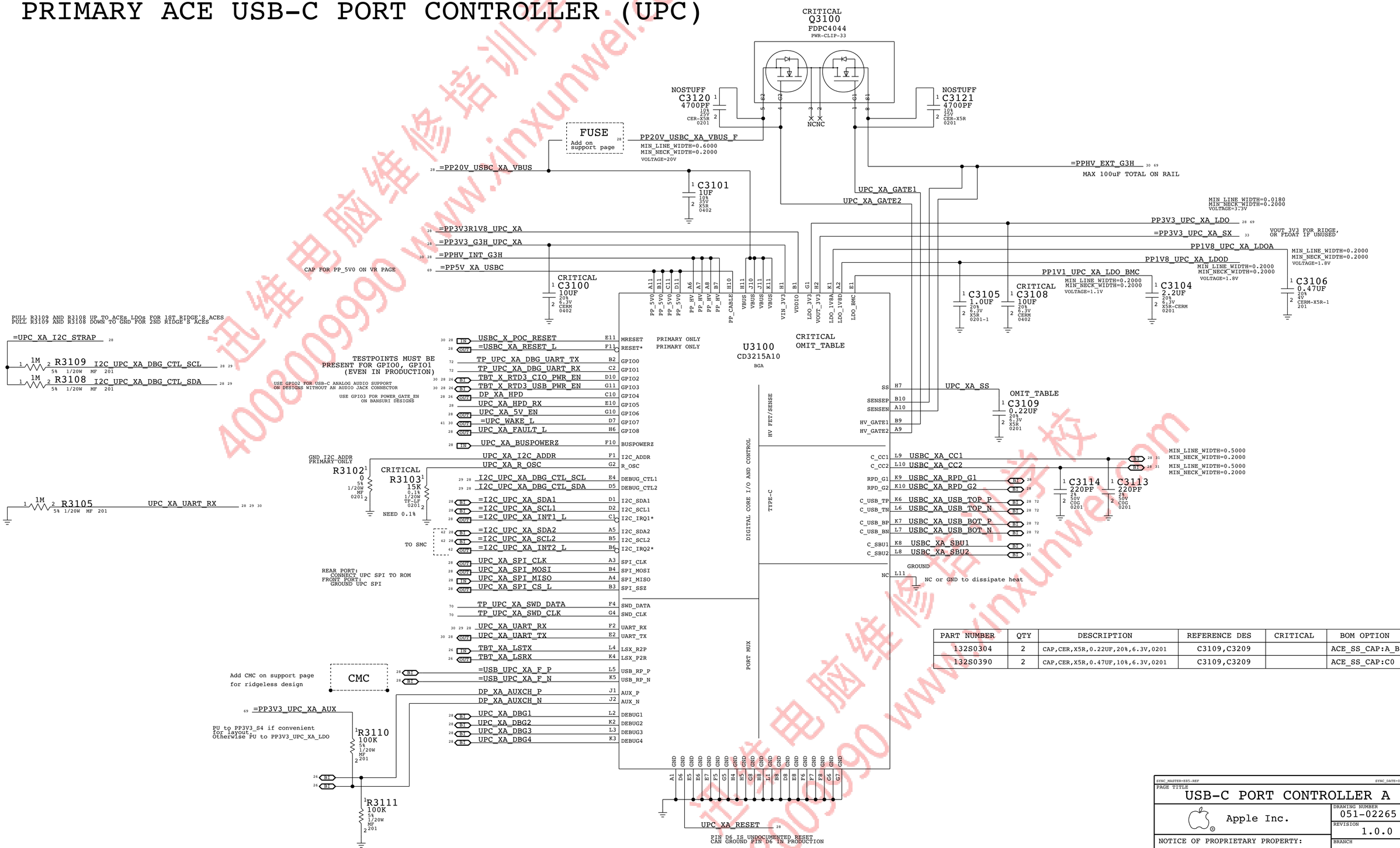
PRIMARY ACE USB-C PORT CONTROLLER (UPC)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0304	2	CAP,CER,X5R,0.22UF,20%,6.3V,0201	C3109,C3209		ACE_SS_CAP:A_B
132S0390	2	CAP,CER,X5R,0.47UF,10%,6.3V,0201	C3109,C3209		ACE_SS_CAP:C0

BOM_COST_GROUP=USB-C

SYNC_MASTER=E85-REF SYNC_DATE=06/17/2015

PAGE TITLE
USB-C PORT CONTROLLER A

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DRAWING NUMBER 051-02265 SIZE D
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PAGE 31 OF 500
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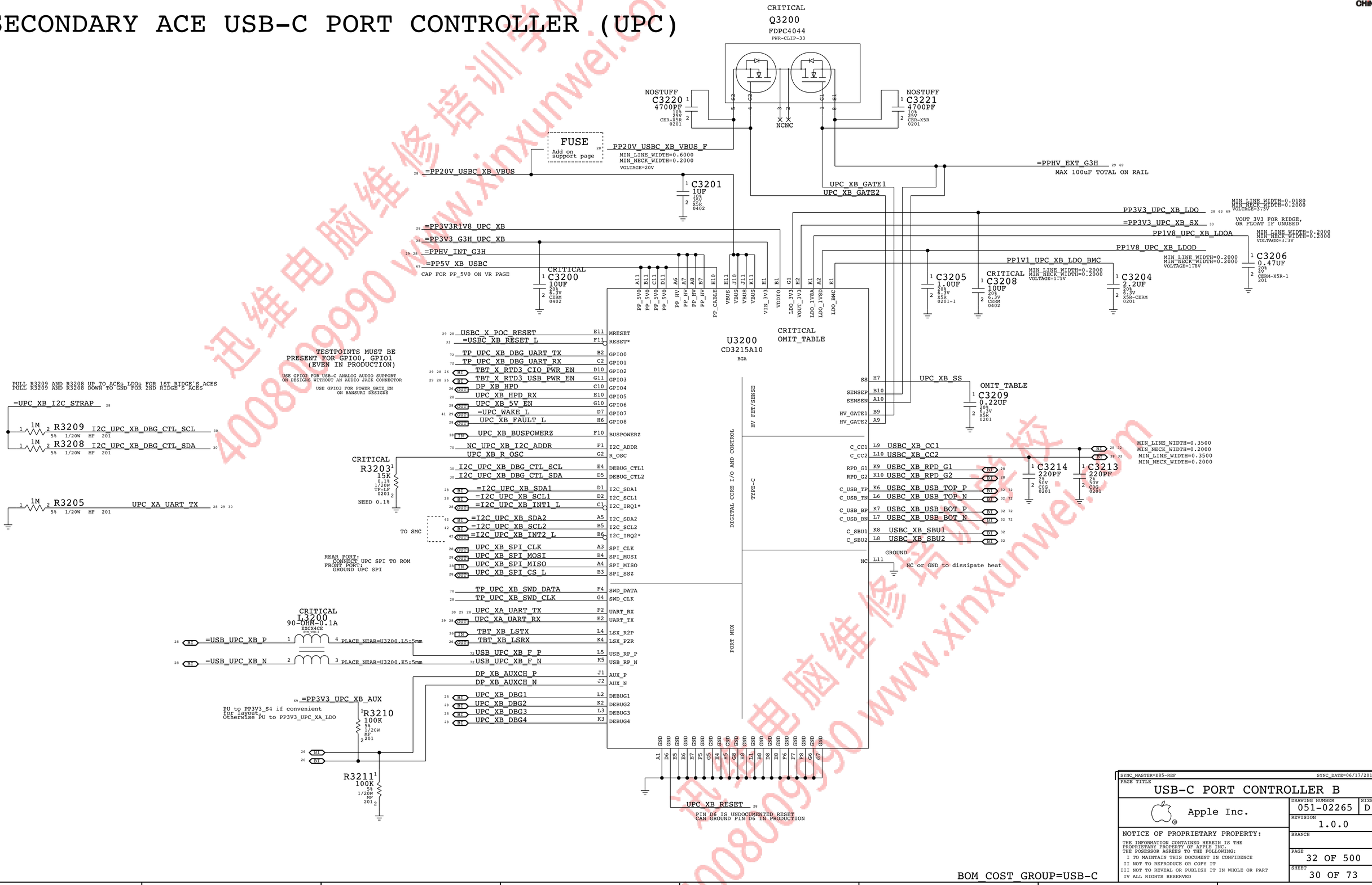
SECONDARY ACE USB-C PORT CONTROLLER (UPC)



BOM_COST_GROUP=USB-C

SYNC_MASTER=E85-REF SYNC_DATE=06/17/2015

PAGE TITLE
USB-C PORT CONTROLLER B

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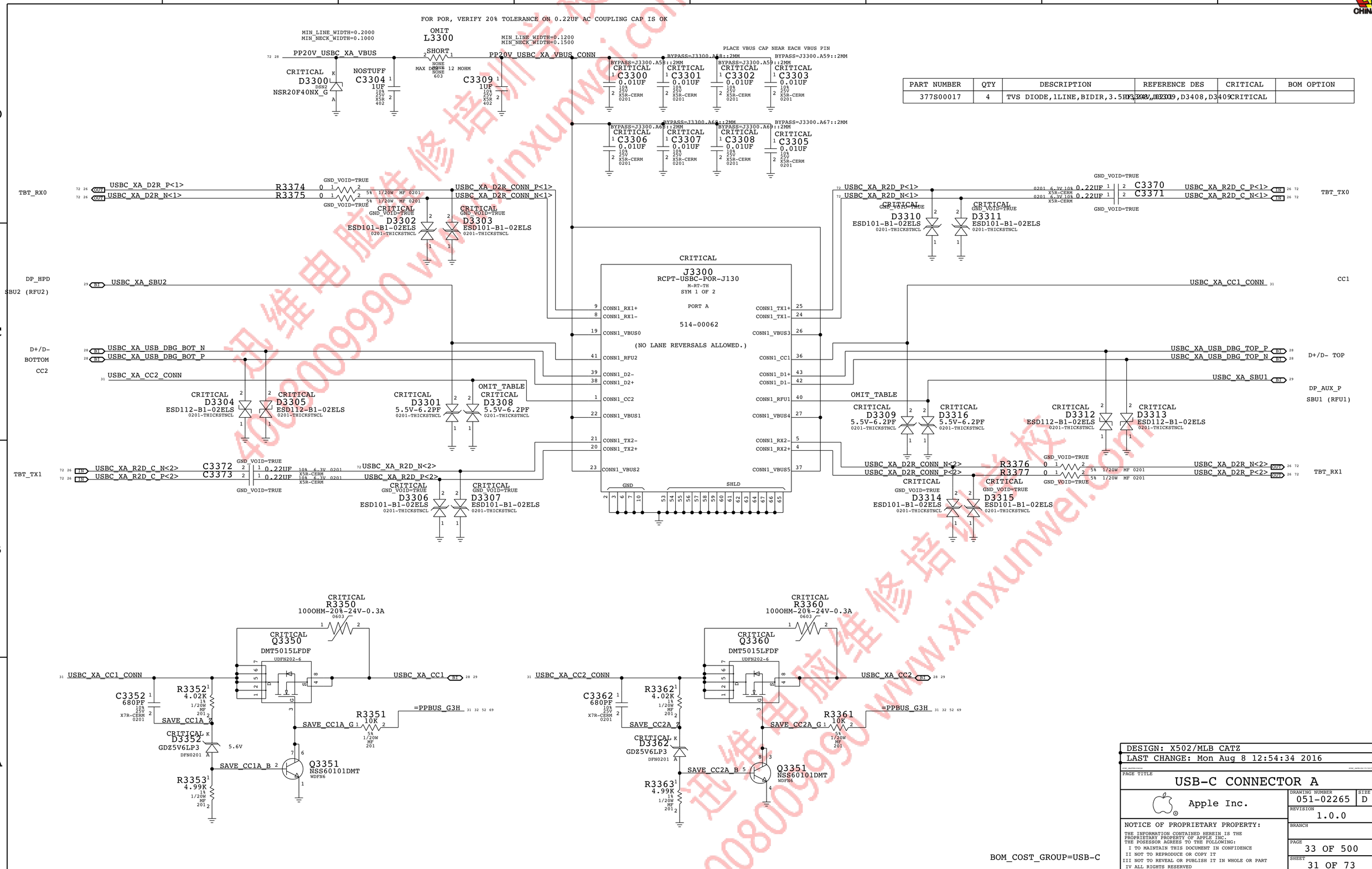

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
377S00017	4	TVS DIODE,1LINE,BIDIR,3.5HF,3.0V,0.2PF	D3300,D3301,D3302,D3303,D3304,D3305,D3306,D3307,D3308,D3309,D3310,D3311,D3312,D3313,D3314,D3315,D3316	CRITICAL	

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
USB-C CONNECTOR A

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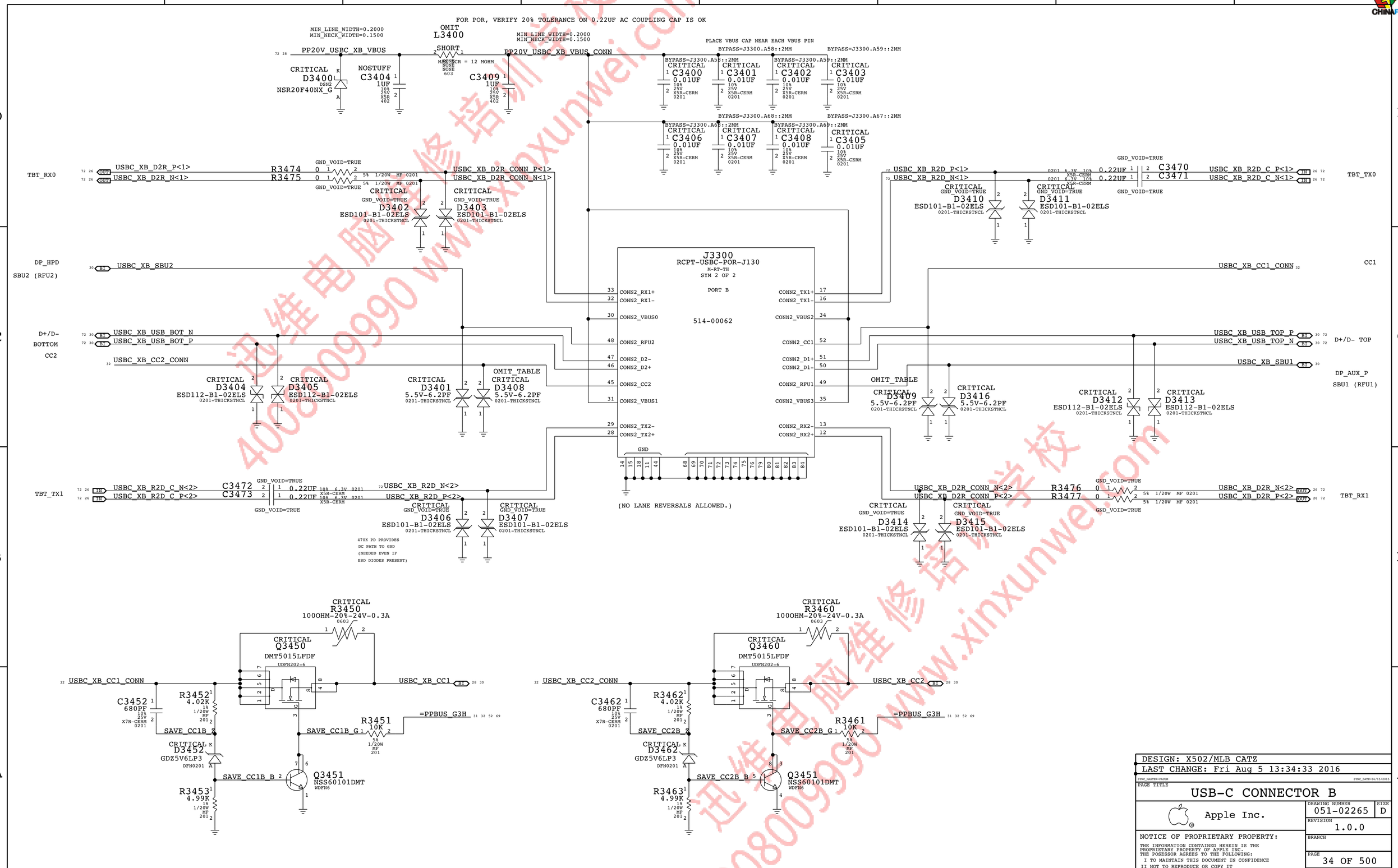
FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1500
OMIT
L3400
SHORT
PP20V_USBC_XB_VBUS
PP20V_USBC_XB_VBUS_CONN
CRITICAL
D3400
NSR20F40NX_G
NOSTUFF
C3404
1UF
C3409
1UF
PLACE VBUS CAP NEAR EACH VBUS PIN
BYPASS=J3300.A58::2MM
BYPASS=J3300.A59::2MM
BYPASS=J3300.A68::2MM
BYPASS=J3300.A67::2MM
C3400
C3401
C3402
C3403
C3406
C3407
C3408
C3405
0.01UF
X5R-CERM
0201
TBT_RX0
USBC_XB_D2R_P<1>
USBC_XB_D2R_N<1>
R3474
R3475
GND_VOID=TRUE
USBC_XB_D2R_CONN_P<1>
USBC_XB_D2R_CONN_N<1>
D3402
D3403
ESD101-B1-02ELS
0201-THICKSTNCL
USBC_XB_R2D_P<1>
USBC_XB_R2D_N<1>
C3470
C3471
0.22UF
USBC_XB_R2D_C_P<1>
USBC_XB_R2D_C_N<1>
TBT_TX0
D3410
D3411
DP_HPD
SBU2 (RFU2)
USBC_XB_SBU2
J3300
RCPT-USBC-POR-J130
M-RT-TH
SYM 2 OF 2
PORT B
514-00062
CONN2_RX1+
CONN2_RX1-
CONN2_VBUS0
CONN2_RFU2
CONN2_D2-
CONN2_D2+
CONN2_CC2
CONN2_VBUS1
CONN2_TX2-
CONN2_TX2+
CONN2_TX1+
CONN2_TX1-
CONN2_VBUS2
CONN2_CC1
CONN2_D1+
CONN2_D1-
CONN2_RFU1
CONN2_VBUS3
CONN2_RX2-
CONN2_RX2+
GND
USBC_XB_CC1_CONN
CC1
D+/D-
BOTTOM
CC2
USBC_XB_USB_BOT_N
USBC_XB_USB_BOT_P
USBC_XB_CC2_CONN
USBC_XB_USB_TOP_P
USBC_XB_USB_TOP_N
D+/D- TOP
USBC_XB_SBU1
DP_AUX_P
SBU1 (RFU1)
D3404
D3405
ESD112-B1-02ELS
D3401
D3408
5.5V-6.2PF
OMIT_TABLE
D3409
D3416
D3412
D3413
TBT_TX1
USBC_XB_R2D_C_N<2>
USBC_XB_R2D_C_P<2>
C3472
C3473
USBC_XB_R2D_N<2>
USBC_XB_R2D_P<2>
D3406
D3407
470K PD PROVIDES
DC PATH TO GND
(NEEDED EVEN IF
ESD DIODES PRESENT)
(NO LANE REVERSALS ALLOWED.)
USBC_XB_D2R_CONN_N<2>
USBC_XB_D2R_CONN_P<2>
R3476
R3477
USBC_XB_D2R_N<2>
USBC_XB_D2R_P<2>
TBT_RX1
D3414
D3415
R3450
100OHM-20%-24V-0.3A
0603
Q3450
DMT5015LFDF
UDFN202-6
USBC_XB_CC1_CONN
USBC_XB_CC1
C3452
680PF
R3452
4.02K
R3451
10K
=PPBUS_G3H
SAVE_CC1B_Z
SAVE_CC1B_G
D3452
GDZ5V6LP3
SAVE_CC1B_B
Q3451
NSS60101DMT
WDFN6
R3453
4.99K
R3460
Q3460
USBC_XB_CC2_CONN
USBC_XB_CC2
C3462
R3462
R3461
SAVE_CC2B_Z
SAVE_CC2B_G
D3462
SAVE_CC2B_B
R3463
BOM_COST_GROUP=USB-C
DESIGN: X502/MLB CATZ
LAST CHANGE: Fri Aug 5 13:34:33 2016
PAGE TITLE
USB-C CONNECTOR B
Apple Inc.
DRAWING NUMBER
051-02265
SIZE
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REVISION
1.0.0
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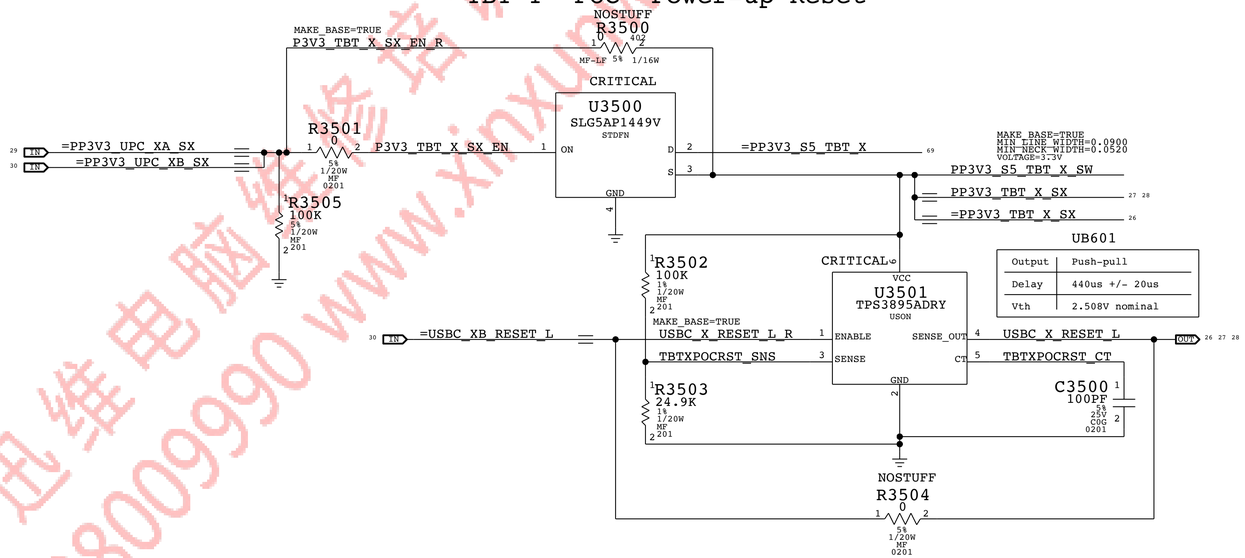
TBT T "POC" Power-up Reset



BOM_COST_GROUP=USB-C

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
USB-C SUPPORT 2

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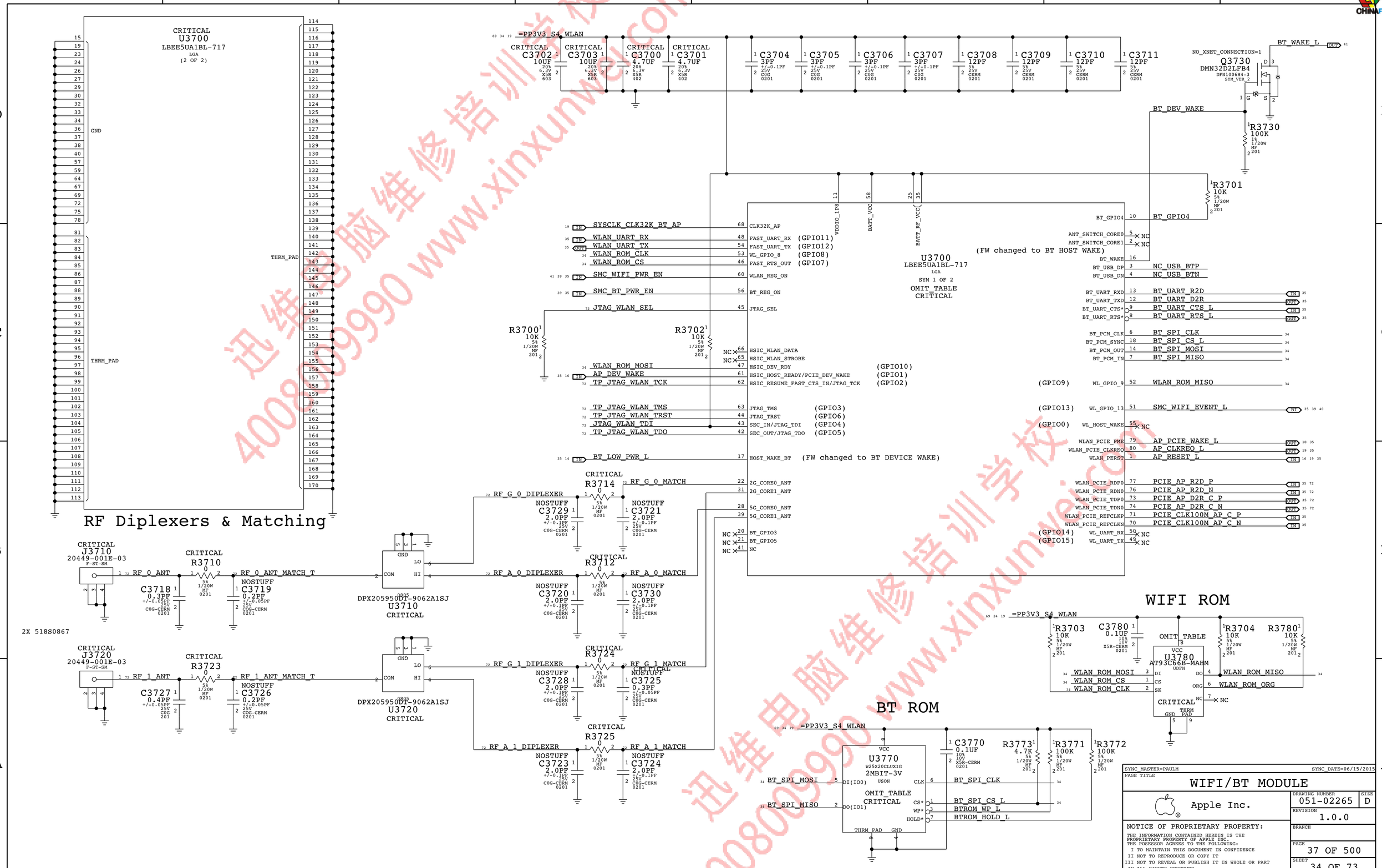
CRITICAL
U3700
LBEE5UA1BL-717
LGA
(2 OF 2)
GND
THRM_PAD
=PP3V3_S4_WLAN
C3702 10UF
C3703 10UF
C3700 4.7UF
C3701 4.7UF
C3704 3PF
C3705 3PF
C3706 3PF
C3707 3PF
C3708 12PF
C3709 12PF
C3710 12PF
C3711 12PF
NO_XNET_CONNECTION=1
Q3730
DMN32D2LFB4
BT_WAKE_L
BT_DEV_WAKE
R3730 100K
R3701 10K
U3700
LBEE5UA1BL-717
LGA
SYM 1 OF 2
OMIT_TABLE
CRITICAL
(FW changed to BT HOST WAKE)
SYSCLK_CLK32K_BT_AP
WLAN_UART_RX
WLAN_UART_TX
WLAN_ROM_CLK
WLAN_ROM_CS
SMC_WIFI_PWR_EN
SMC_BT_PWR_EN
JTAG_WLAN_SEL
R3700 10K
R3702 10K
WLAN_ROM_MOSI
AP_DEV_WAKE
TP_JTAG_WLAN_TCK
TP_JTAG_WLAN_TMS
TP_JTAG_WLAN_TRST
JTAG_WLAN_TDI
TP_JTAG_WLAN_TDO
BT_LOW_PWR_L
(FW changed to BT DEVICE WAKE)
BT_GPIO4
NC_USB_BTP
NC_USB_BTN
BT_UART_R2D
BT_UART_D2R
BT_UART_CTS_L
BT_UART_RTS_L
BT_SPI_CLK
BT_SPI_CS_L
BT_SPI_MOSI
BT_SPI_MISO
WLAN_ROM_MISO
SMC_WIFI_EVENT_L
AP_PCIE_WAKE_L
AP_CLKREQ_L
AP_RESET_L
PCIE_AP_R2D_P
PCIE_AP_R2D_N
PCIE_AP_D2R_C_P
PCIE_AP_D2R_C_N
PCIE_CLK100M_AP_C_P
PCIE_CLK100M_AP_C_N
RF Diplexers & Matching
CRITICAL
J3710
20449-001E-03
F-ST-SM
RF_0_ANT
R3710 0
C3718 0.3PF
RF_0_ANT_MATCH_T
C3719 0.2PF
DPX205950DT-9062A1SJ
U3710
CRITICAL
2X 518S0867
J3720
20449-001E-03
RF_1_ANT
R3723 0
C3727 0.4PF
RF_1_ANT_MATCH_T
C3726 0.2PF
U3720
RF_G_0_DIPLEXER
R3714 0
C3729 2.0PF
C3721 2.0PF
RF_A_0_DIPLEXER
R3712 0
C3720 2.0PF
C3730 2.0PF
RF_G_1_DIPLEXER
R3724 0
C3728 2.0PF
C3725 0.3PF
RF_A_1_DIPLEXER
R3725 0
C3723 2.0PF
C3724 2.0PF
WIFI ROM
R3703 10K
C3780 0.1UF
OMIT_TABLE
R3704 10K
R3780 10K
U3780
AT93C66B-MAHM
BT ROM
U3770
W25X20CLUXIG
2MBIT-3V
C3770 0.1UF
R3773 4.7K
R3771 100K
R3772 100K
BT_SPI_MOSI
BT_SPI_MISO
BTROM_WP_L
BTROM_HOLD_L
SYNC_MASTER=PAULM
SYNC_DATE=06/15/2015
PAGE TITLE
WIFI/BT MODULE
Apple Inc.
DRAWING NUMBER 051-02265
SIZE D
REVISION 1.0.0
BRANCH
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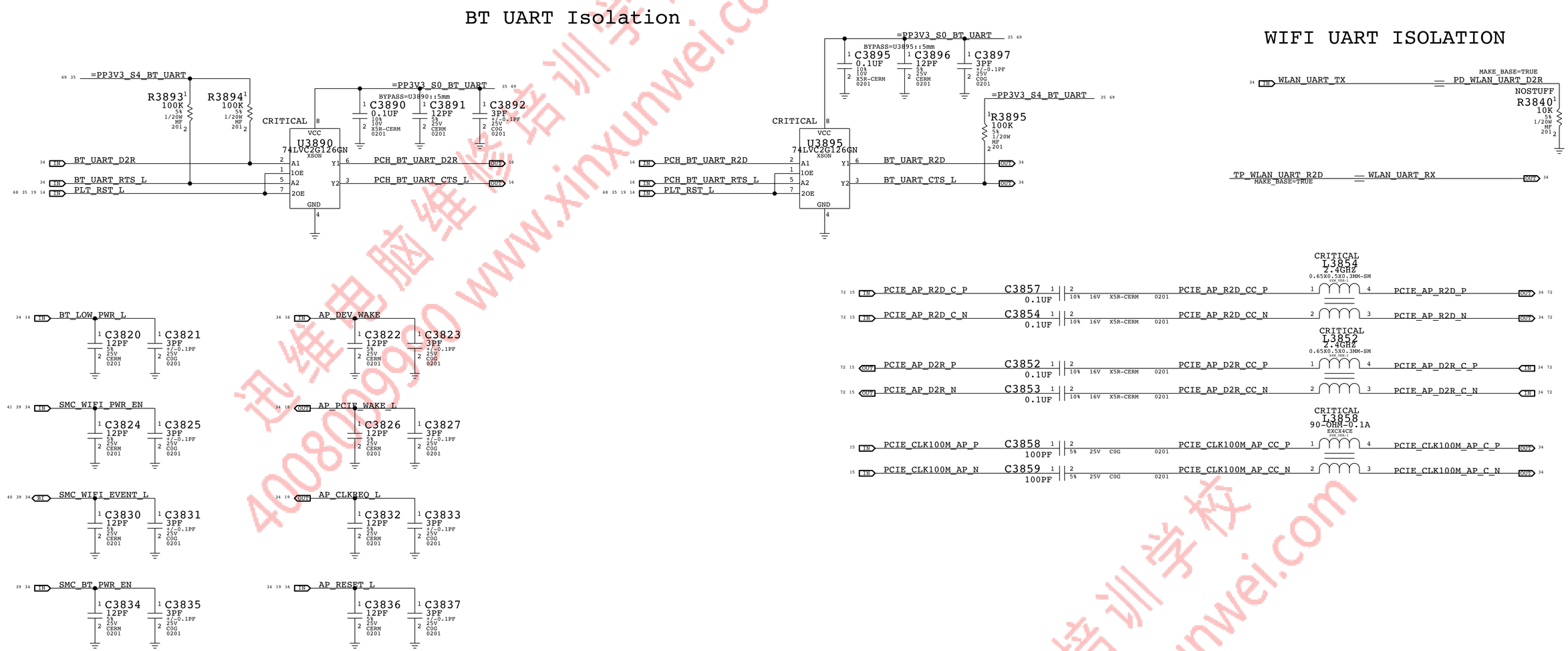

PAGE TITLE

WIFI/BT Module Support

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D

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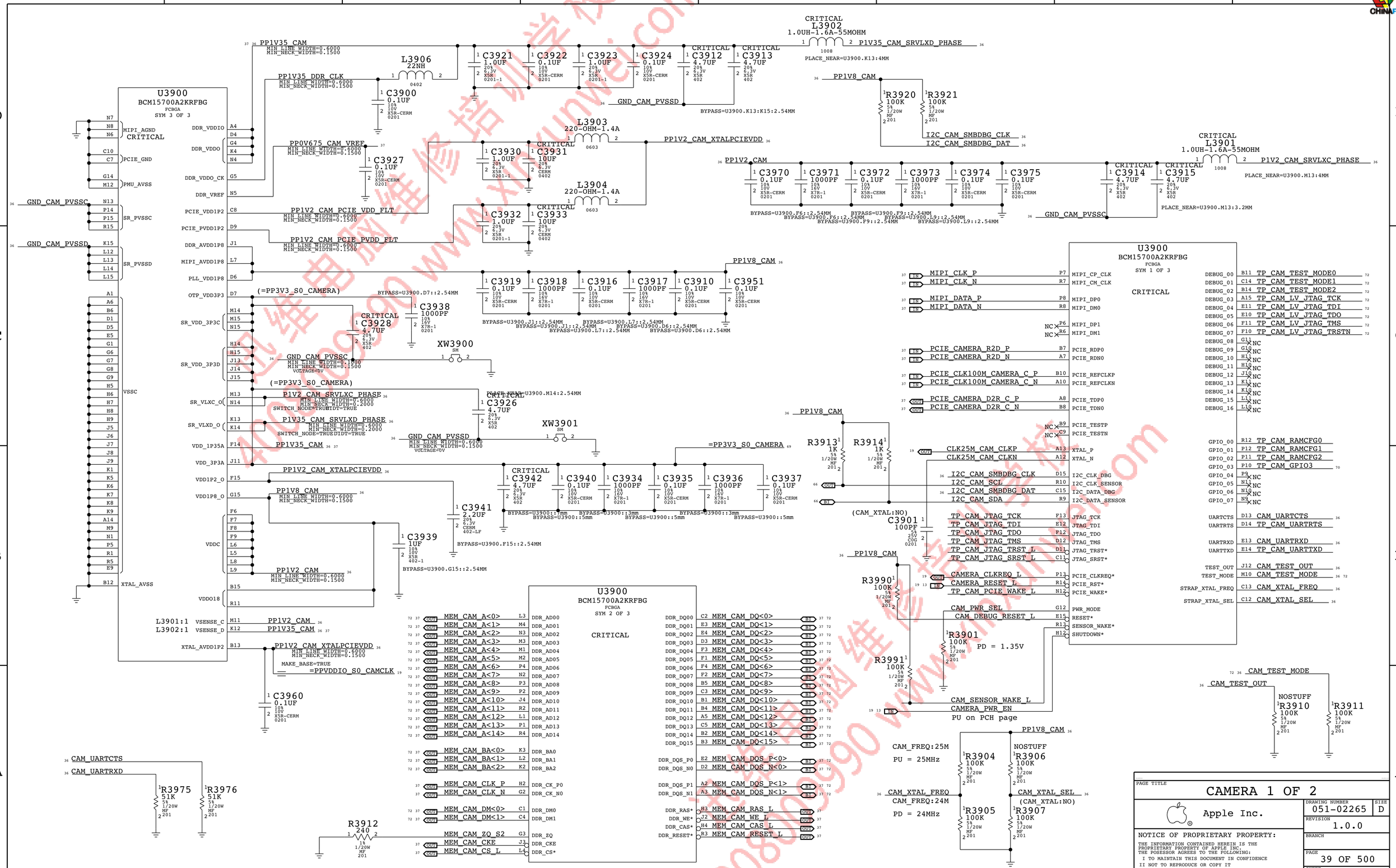

PAGE TITLE

CAMERA 1 OF 2

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DRAWING NUMBER 051-02265 SIZE D

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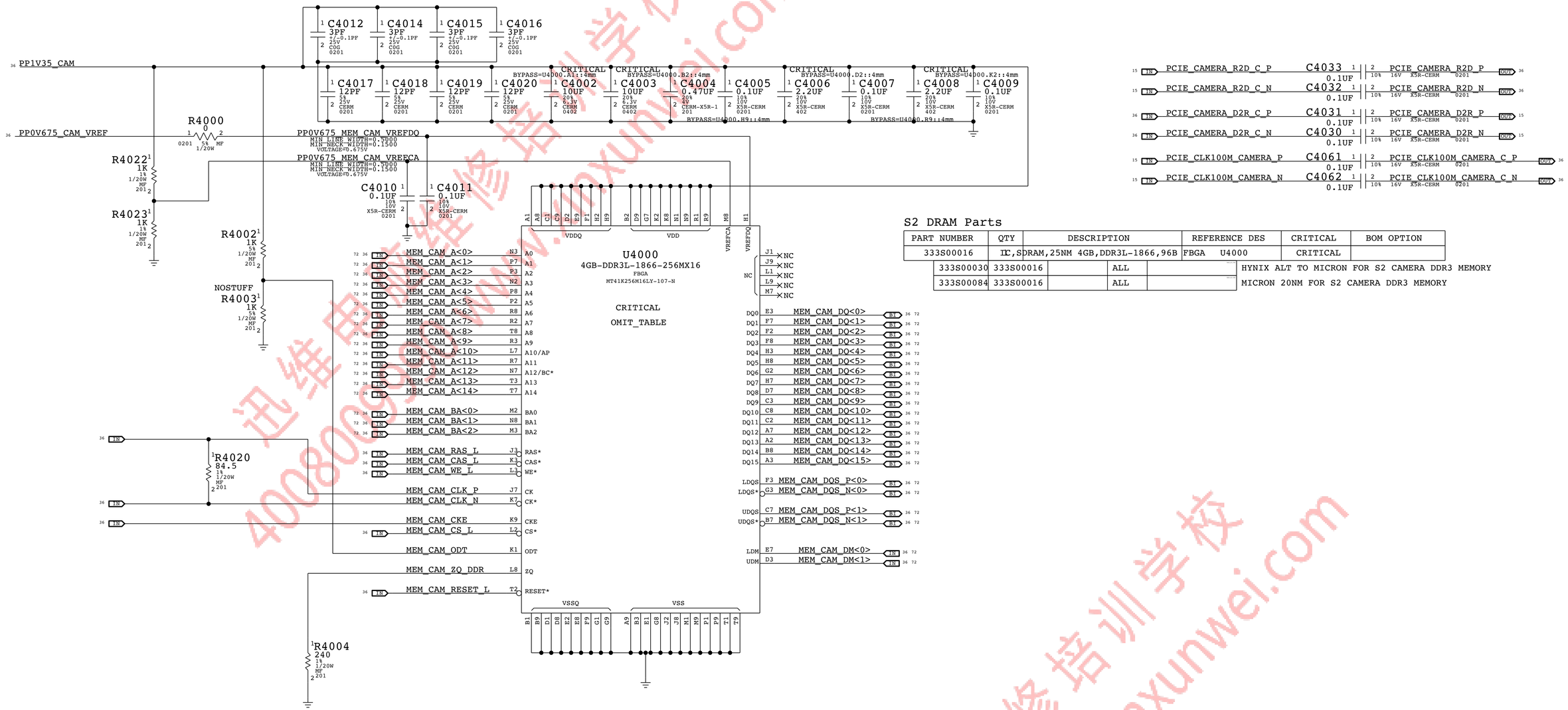
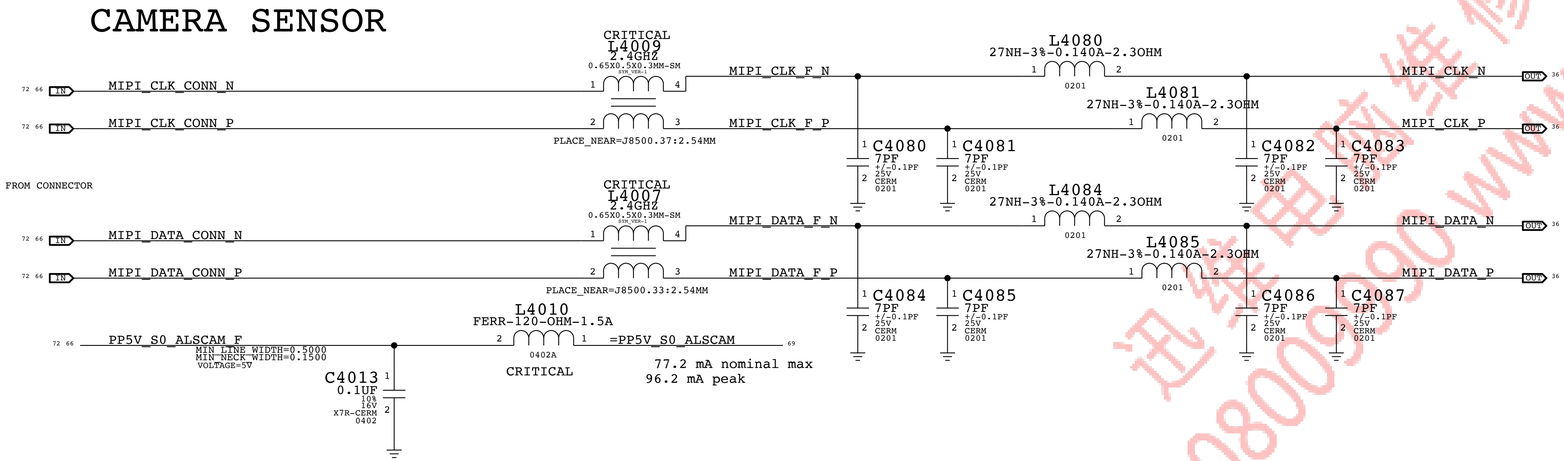


S2 DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00016	IC,SDRAM,25NM 4GB,DDR3L-1866,96B		FBGA U4000	CRITICAL	
333S00030	333S00016	ALL			HYNIX ALT TO MICRON FOR S2 CAMERA DDR3 MEMORY
333S00084	333S00016	ALL			MICRON 20NM FOR S2 CAMERA DDR3 MEMORY

CAMERA SENSOR



BOM_COST_GROUP=CAMERA

PAGE TITLE	CAMERA 2 OF 2
Apple Inc.	DRAWING NUMBER 051-02265 SIZE D
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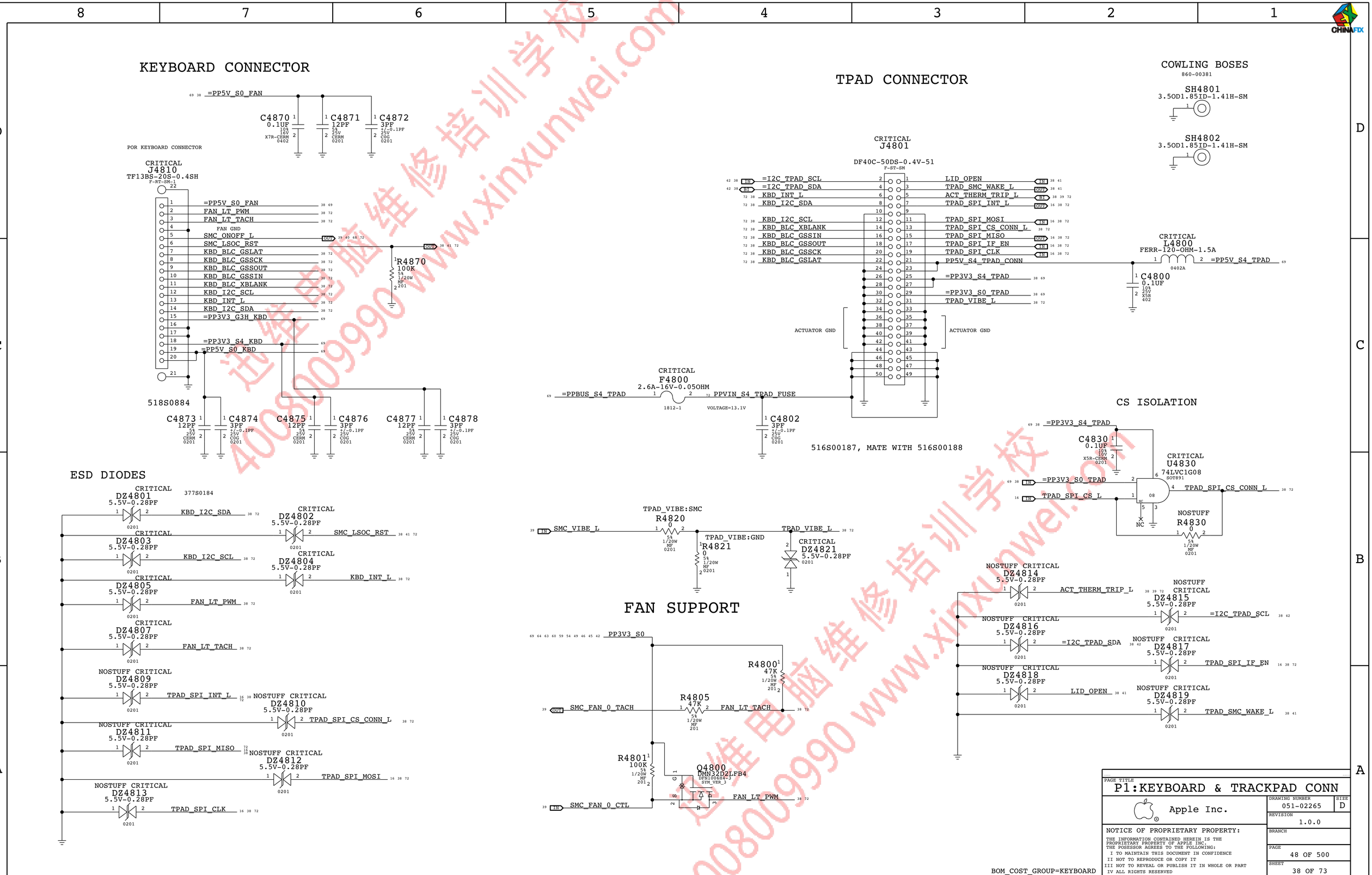
KEYBOARD CONNECTOR
=PP5V_S0_FAN
C4870 0.1UF 10% 16V X7R-CERM 0402
C4871 12PF 5% 25V CERM 0201
C4872 3PF +/-0.1PF 25V C0G 0201
POR KEYBOARD CONNECTOR
CRITICAL
J4810
TF13BS-20S-0.4SH
F-RT-SM-1
=PP5V_S0_FAN
FAN_LT_PWM
FAN_LT_TACH
FAN GND
SMC_ONOFF_L
SMC_LSOC_RST
KBD_BLC_GSLAT
KBD_BLC_GSSCK
KBD_BLC_GSSOUT
KBD_BLC_GSSIN
KBD_BLC_XBLANK
KBD_I2C_SCL
KBD_INT_L
KBD_I2C_SDA
=PP3V3_G3H_KBD
=PP3V3_S4_KBD
=PP5V_S0_KBD
R4870 100K 5% 1/20W MF 201
518S0884
C4873 12PF 5% 25V CERM 0201
C4874 3PF +/-0.1PF 25V C0G 0201
C4875 12PF 5% 25V CERM 0201
C4876 3PF +/-0.1PF 25V C0G 0201
C4877 12PF 5% 25V CERM 0201
C4878 3PF +/-0.1PF 25V C0G 0201
ESD DIODES
377S0184
CRITICAL
DZ4801 5.5V-0.28PF
KBD_I2C_SDA
DZ4802 5.5V-0.28PF
SMC_LSOC_RST
DZ4803 5.5V-0.28PF
KBD_I2C_SCL
DZ4804 5.5V-0.28PF
KBD_INT_L
DZ4805 5.5V-0.28PF
FAN_LT_PWM
DZ4807 5.5V-0.28PF
FAN_LT_TACH
NOSTUFF CRITICAL
DZ4809 5.5V-0.28PF
TPAD_SPI_INT_L
DZ4810 5.5V-0.28PF
TPAD_SPI_CS_CONN_L
DZ4811 5.5V-0.28PF
TPAD_SPI_MISO
DZ4812 5.5V-0.28PF
TPAD_SPI_MOSI
DZ4813 5.5V-0.28PF
TPAD_SPI_CLK
TPAD CONNECTOR
CRITICAL
J4801
DF40C-50DS-0.4V-51
F-ST-SM
=I2C_TPAD_SCL
=I2C_TPAD_SDA
KBD_INT_L
KBD_I2C_SDA
KBD_I2C_SCL
KBD_BLC_XBLANK
KBD_BLC_GSSIN
KBD_BLC_GSSOUT
KBD_BLC_GSSCK
KBD_BLC_GSLAT
LID_OPEN
TPAD_SMC_WAKE_L
ACT_THERM_TRIP_L
TPAD_SPI_INT_L
TPAD_SPI_MOSI
TPAD_SPI_CS_CONN_L
TPAD_SPI_MISO
TPAD_SPI_IF_EN
TPAD_SPI_CLK
PP5V_S4_TPAD_CONN
=PP3V3_S4_TPAD
=PP3V3_S0_TPAD
TPAD_VIBE_L
ACTUATOR GND
ACTUATOR GND
CRITICAL
L4800
FERR-120-OHM-1.5A
0402A
=PP5V_S4_TPAD
C4800 0.1UF 10% 25V X5R 402
CRITICAL
F4800
2.6A-16V-0.05OHM
1812-1
=PPBUS_S4_TPAD
PPVIN_S4_TPAD_FUSE
VOLTAGE=13.1V
C4802 3PF +/-0.1PF 25V C0G 0201
516S00187, MATE WITH 516S00188
COWLING BOSES
860-00381
SH4801 3.5OD1.85ID-1.41H-SM
SH4802 3.5OD1.85ID-1.41H-SM
CS ISOLATION
=PP3V3_S4_TPAD
C4830 0.1UF 10% 10V X5R-CERM 0201
CRITICAL
U4830
74LVC1G08
SOT891
=PP3V3_S0_TPAD
TPAD_SPI_CS_L
TPAD_SPI_CS_CONN_L
NC
NOSTUFF
R4830 0 5% 1/20W MF 0201
NOSTUFF CRITICAL
DZ4814 5.5V-0.28PF
ACT_THERM_TRIP_L
DZ4815 5.5V-0.28PF
=I2C_TPAD_SCL
DZ4816 5.5V-0.28PF
=I2C_TPAD_SDA
DZ4817 5.5V-0.28PF
TPAD_SPI_IF_EN
DZ4818 5.5V-0.28PF
LID_OPEN
DZ4819 5.5V-0.28PF
TPAD_SMC_WAKE_L
TPAD_VIBE:SMC
R4820 0 5% 1/20W MF 0201
SMC_VIBE_L
TPAD_VIBE:GND
R4821 0 5% 1/20W MF 0201
TPAD_VIBE_L
CRITICAL
DZ4821 5.5V-0.28PF
FAN SUPPORT
PP3V3_S0
R4800 47K 5% 1/20W MF 201
R4805 47K 5% 1/20W MF 201
SMC_FAN_0_TACH
FAN_LT_TACH
R4801 100K 5% 1/20W MF 201
Q4800
DMN32D2LFB4
DFN1006H4-3
SYM_VER_3
SMC_FAN_0_CTL
FAN_LT_PWM
BOM_COST_GROUP=KEYBOARD
PAGE TITLE
P1:KEYBOARD & TRACKPAD CONN
Apple Inc.
DRAWING NUMBER
051-02265
SIZE
D
REVISION
1.0.0
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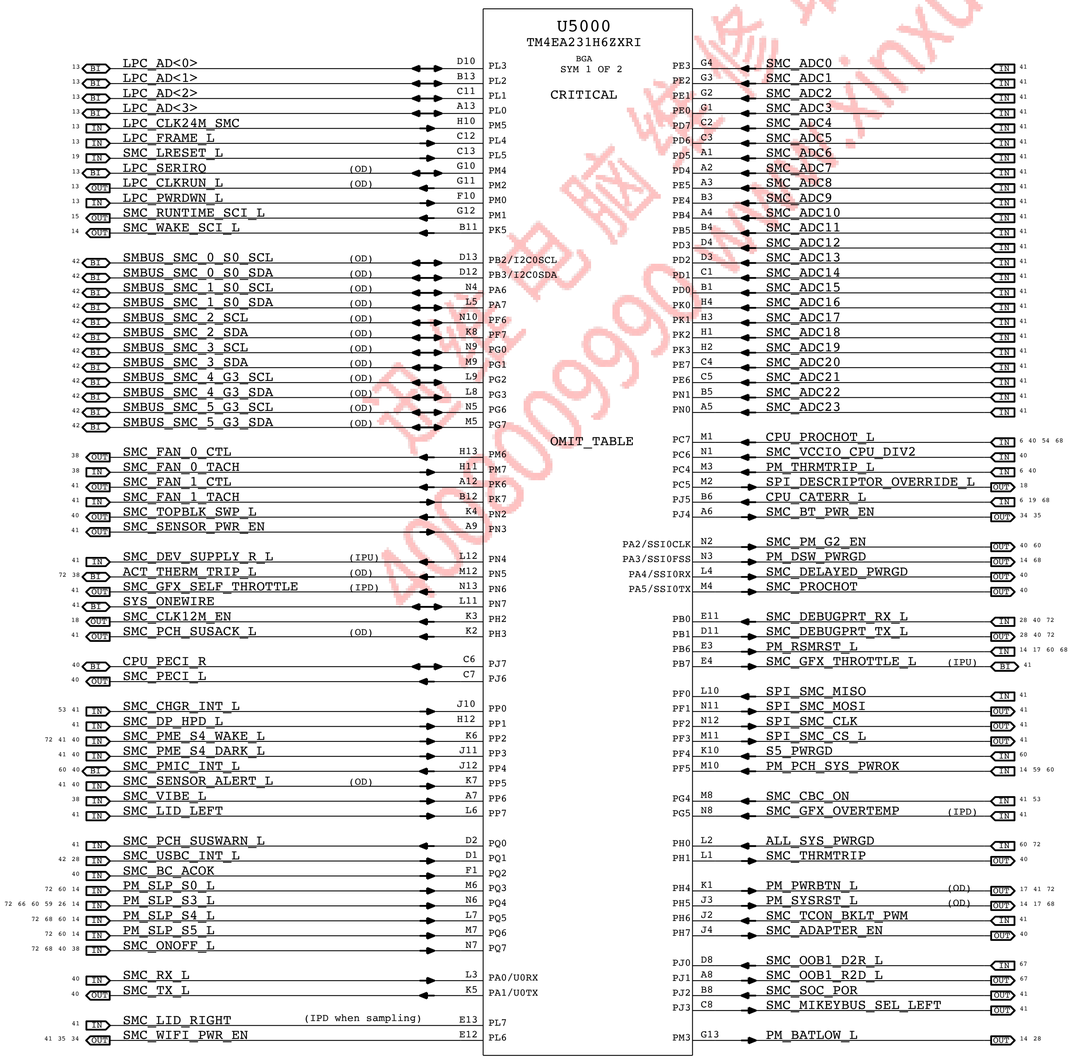
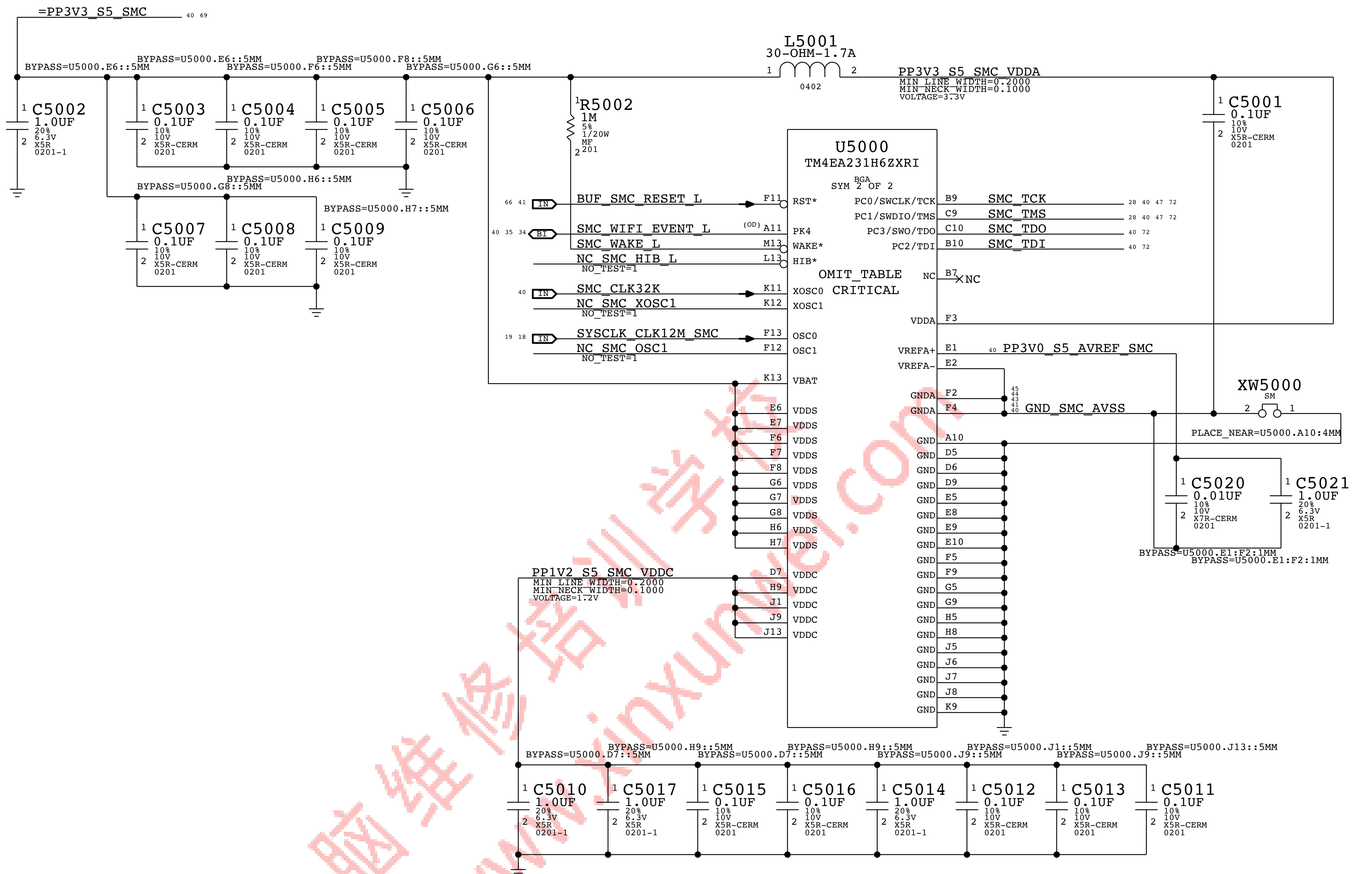


NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.



SYNC_MASTER=PAULM SYNC_DATE=06/15/2015

PAGE TITLE

SMC

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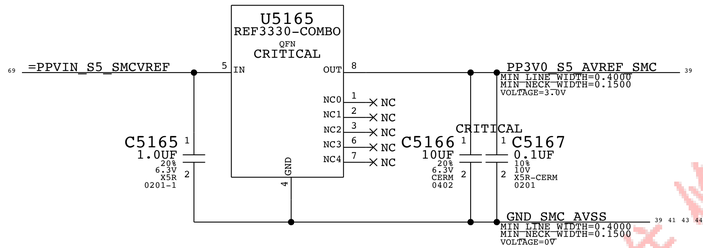
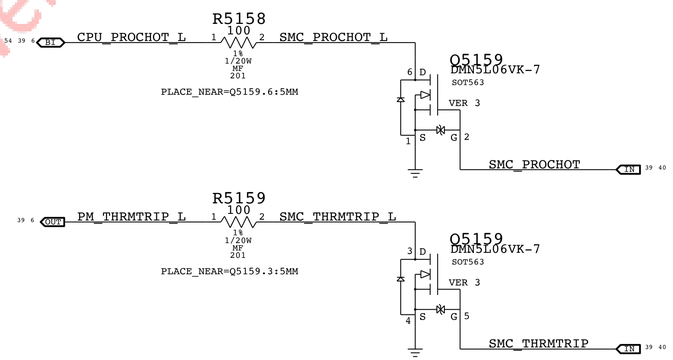
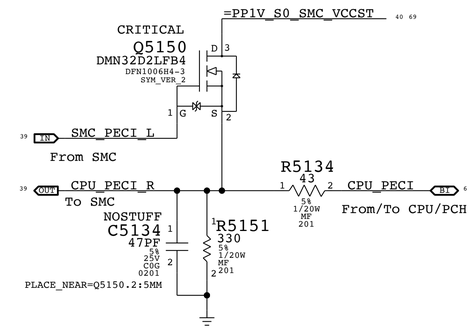
SMC AVREF Supply



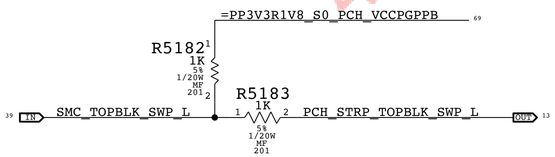
PROCHOT/THRMTRIP Support

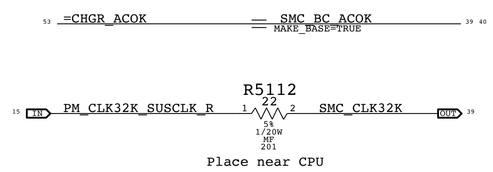


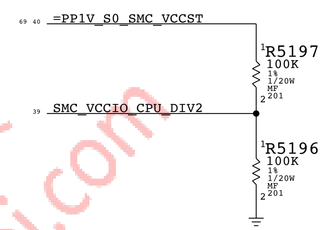
PECI Support

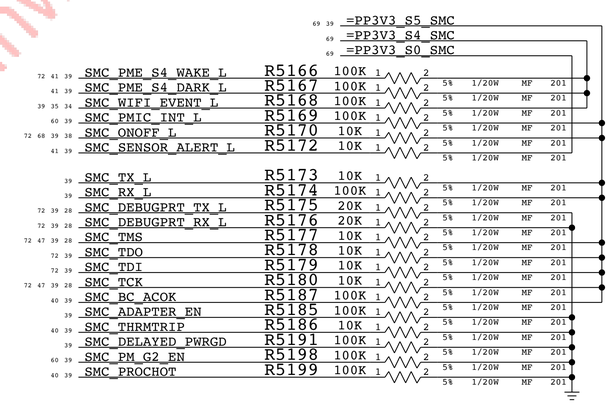


Top-Block Swap









BOM_COST_GROUP=SMC

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SMC Shared Support

Apple Inc.

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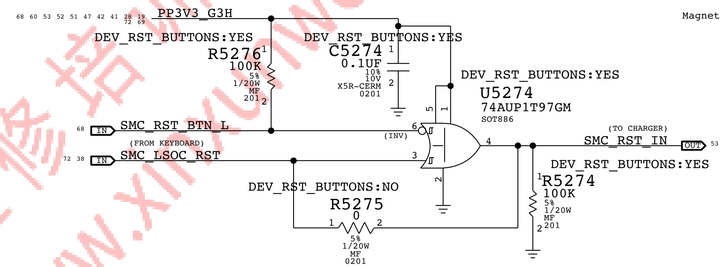
SMC ANALOG INPUTS

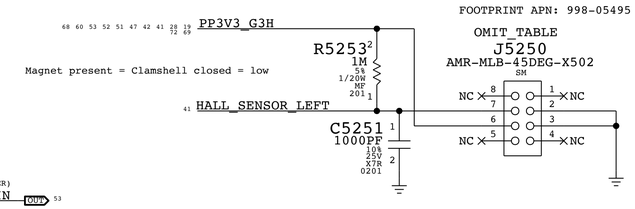
SMC_ADC0	MAKE_BASE=TRUE	SMC_DCIN_VSENSE	
SMC_ADC1	MAKE_BASE=TRUE	SMC_DCIN_ISENSE	
SMC_ADC2	MAKE_BASE=TRUE	SMC_PBUS_VSENSE	
SMC_ADC3	MAKE_BASE=TRUE	SMC_BMON_ISENSE	
SMC_ADC4	MAKE_BASE=TRUE	SMC_TPAD_ISENSE	
SMC_ADC5	MAKE_BASE=TRUE	SMC_CPU_HI_ISENSE	
SMC_ADC6	MAKE_BASE=TRUE	SMC_CPU_VSENSE	
SMC_ADC7	MAKE_BASE=TRUE	SMC_CPU_ISENSE	
SMC_ADC8	MAKE_BASE=TRUE	SMC_GT_VSENSE	
SMC_ADC9	MAKE_BASE=TRUE	SMC_GT_ISENSE	
SMC_ADC10	MAKE_BASE=TRUE	SMC_SA_ISENSE	
SMC_ADC11	MAKE_BASE=TRUE	SMC_1V5S_ISENSE	
SMC_ADC12	MAKE_BASE=TRUE	SMC_SSD_ISENSE	
SMC_ADC13	MAKE_BASE=TRUE	SMC_3V3SSD_ISENSE	
SMC_ADC14	MAKE_BASE=TRUE	SMC_1V2S3_ISENSE	
SMC_ADC15	MAKE_BASE=TRUE	SMC_CPU_IMON_ISENSE	
SMC_ADC16	MAKE_BASE=TRUE	SMC_GT_IMON_ISENSE	
SMC_ADC17	MAKE_BASE=TRUE	SMC_3V3LCD_ISENSE	
SMC_ADC18	MAKE_BASE=TRUE	SMC_3V3WLS_ISENSE	
SMC_ADC19	MAKE_BASE=TRUE	SMC_LCDBKLT_ISENSE	
SMC_ADC20	MAKE_BASE=TRUE	SMC_SA_IMON_ISENSE	
SMC_ADC21	MAKE_BASE=TRUE	SMC_5VS4_ISENSE	
SMC_ADC22	MAKE_BASE=TRUE	SMC_3V3S5_ISENSE	
SMC_ADC23	MAKE_BASE=TRUE	SMC_TBT_ISENSE	

SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_THROTTLE_L
SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_OVERTEMP
SMC_FAN_1_CTL	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_1_CTL
SMC_FAN_1_TACH	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_1_TACH
SMC_SOC_POR	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_SOC_POR
SMC_GFX_SELF_THROTTLE	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GFX_SELF_THROTTLE
SPI_SMC_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_CLK
SPI_SMC_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_CS_L
SPI_SMC_MISO	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_MISO
SPI_SMC_MOSI	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_SMC_MOSI
SMC_MIKEYBUS_SEL_LEFT	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_MIKEYBUS_SEL_LEFT
SYS_ONEWIRE	MAKE_BASE=TRUE	NO_TEST=1	NC_SYS_ONEWIRE

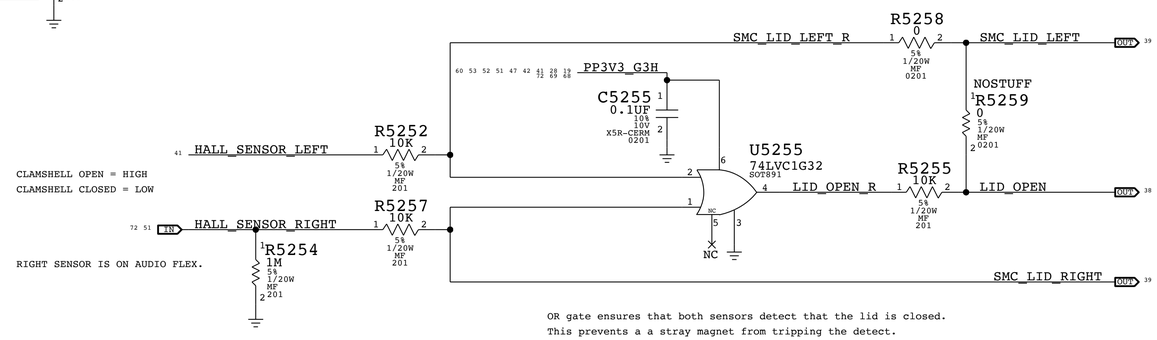


AMR SENSOR PADS

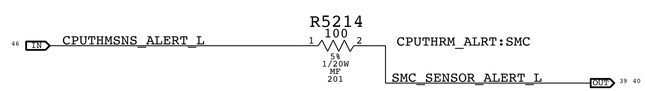
FOOTPRINT APN: 998-05495

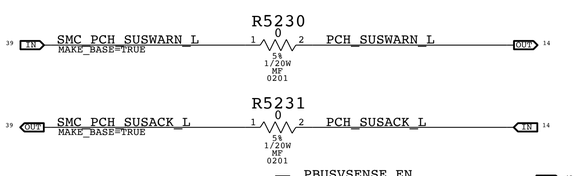


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-05143	1	SUBASSY (T&R) PCBA,HES INTERPOSER 45,X502	J5250	CRITICAL	

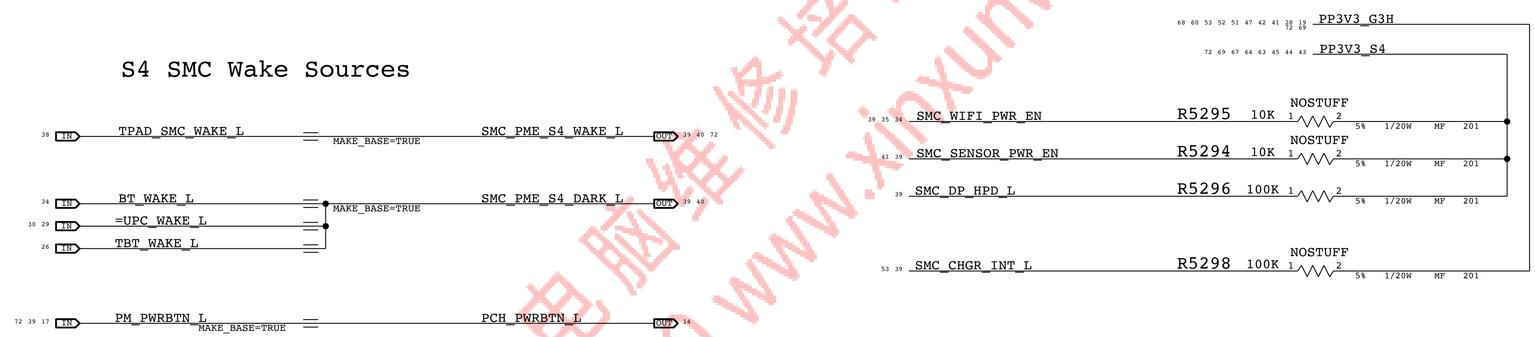


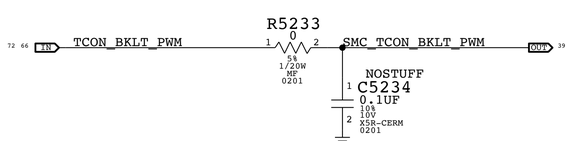
Thermal Alerts

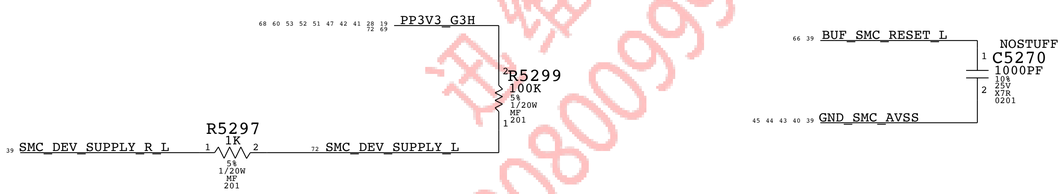




S4 SMC Wake Sources







BOM_COST_GROUP=SMC

DESIGN: X502/MLB CATZ
SYNC MASTER=PAULM

PAGE TITLE
SMC Project Support

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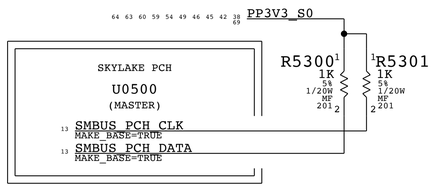
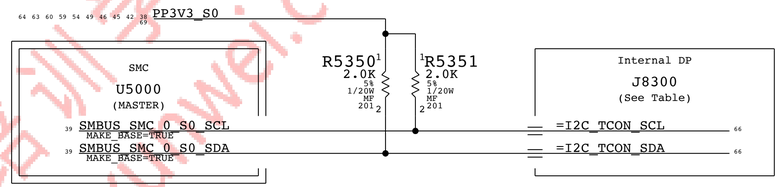
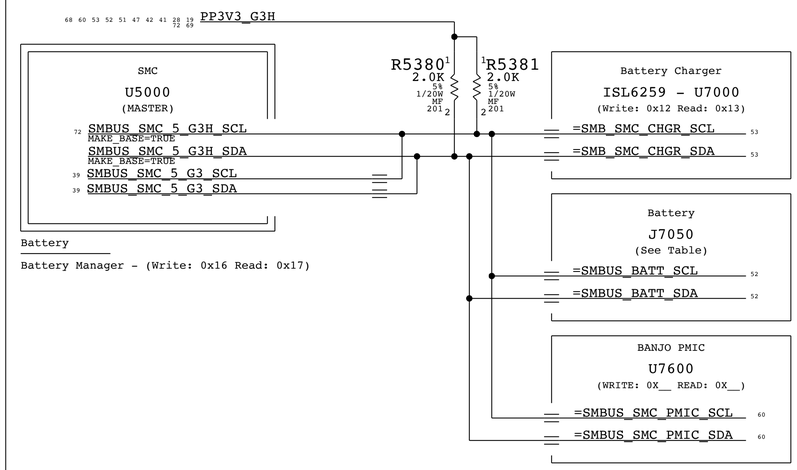
SKYLAKE PCH S0 "SMBUS 0" CONNECTIONS



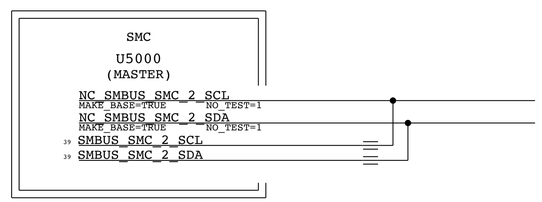
SMC SMBus "0" S0 Connections



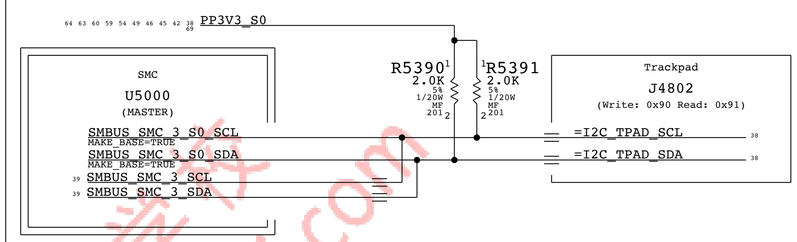
SMC SMBus "5" G3H Connections



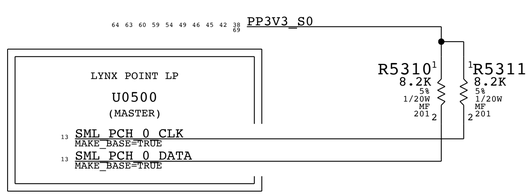
SMC SMBus "2" S3 Connections



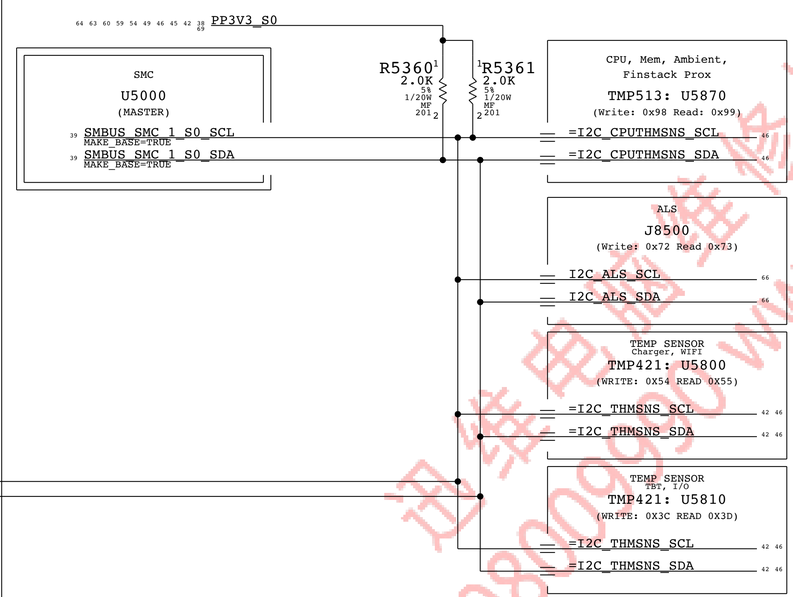
SMC SMBus "3" S0 Connections



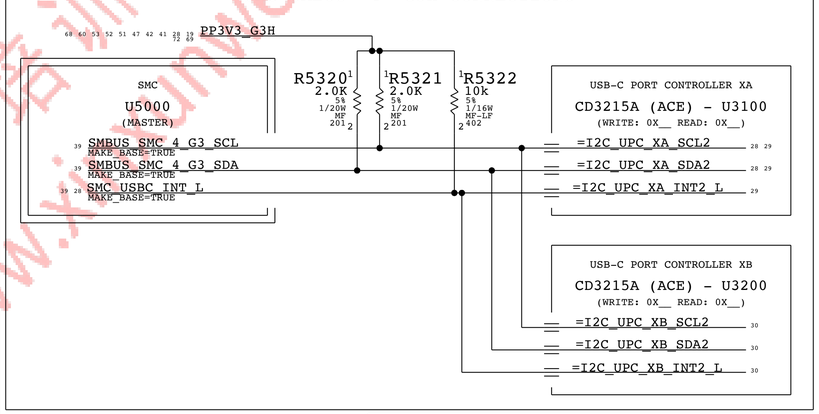
LYNX POINT LP S0 "SMLink 0" Connections



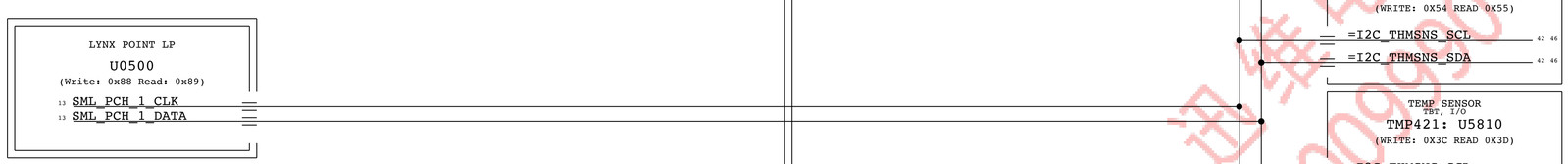
SMC SMBus "1" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to access PCH.

BOM_COST_GROUP=SMC

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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SMBus Connections

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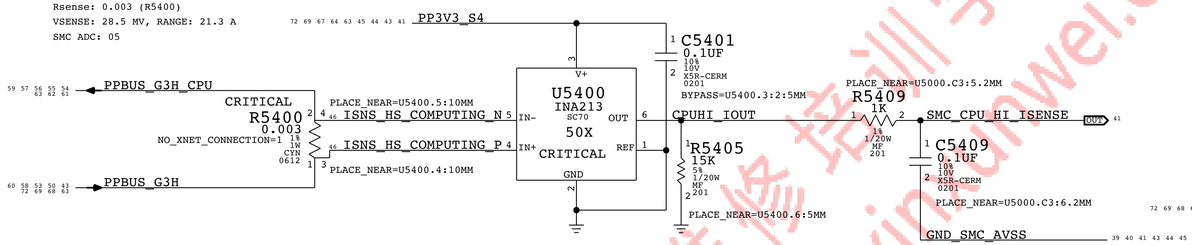
INA21X PARTS HAVE MINOR LEAKAGE PATH FROM INPUTS TO OUTPUT WHEN UNPOWERED.
PULL-DOWN RESISTERS ON INA OUTPUTS BLEED OFF THE LEAKAGE CURRENT TO PREVENT
SIGNAL PUMP-UP.

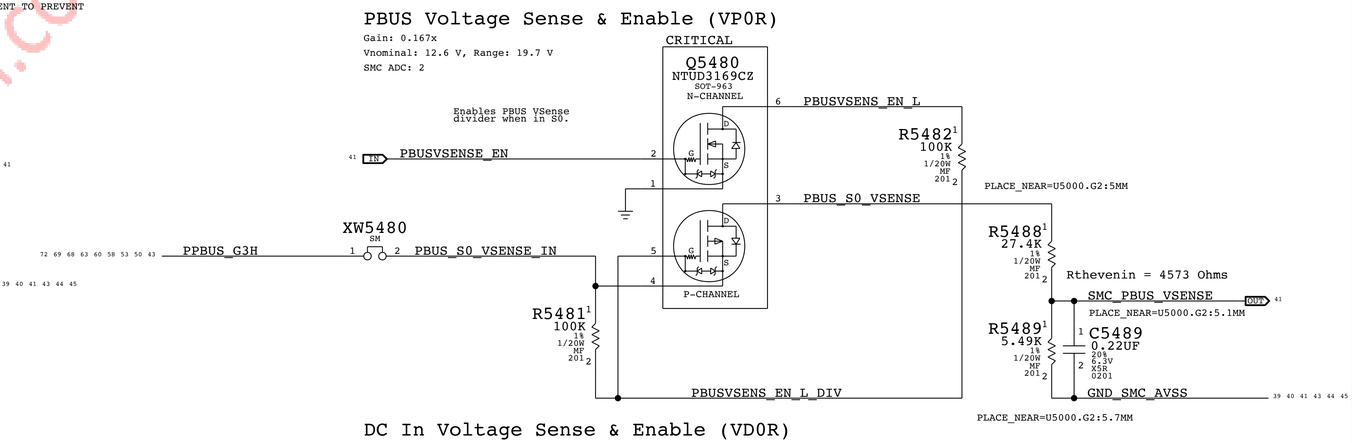
CPU High Side Current Sense (IC0R)

GAIN: 50X, EDP: 9.5 A
Rsense: 0.003 (R5400)
VSENSE: 28.5 MV, RANGE: 21.3 A
SMC ADC: 05



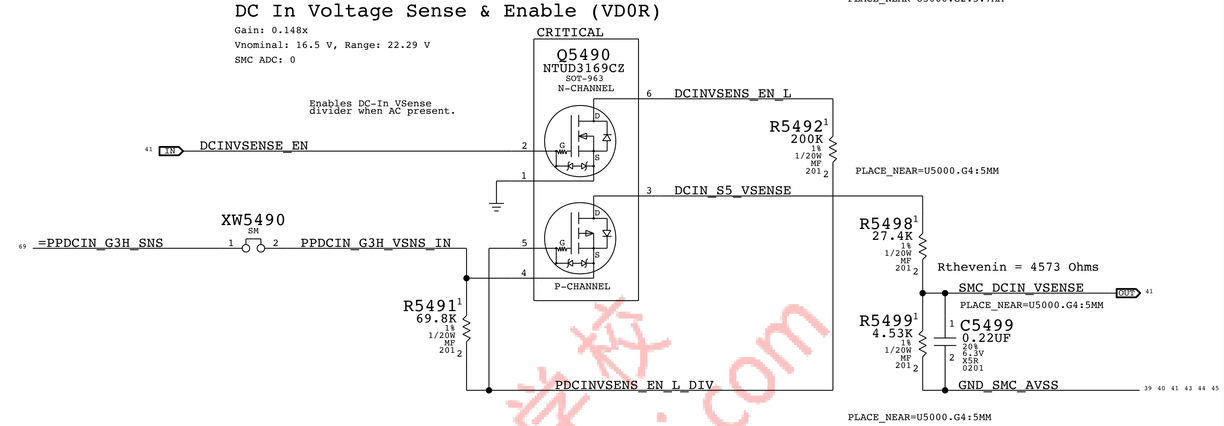
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 19.7 V
SMC ADC: 2



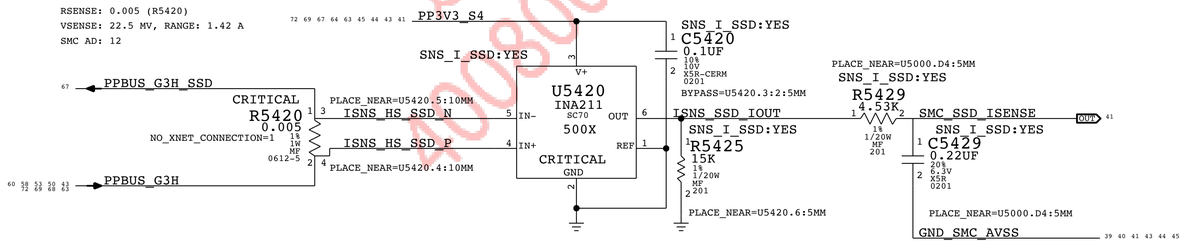
DC In Voltage Sense & Enable (VD0R)

Gain: 0.148x
Vnominal: 16.5 V, Range: 22.29 V
SMC ADC: 0



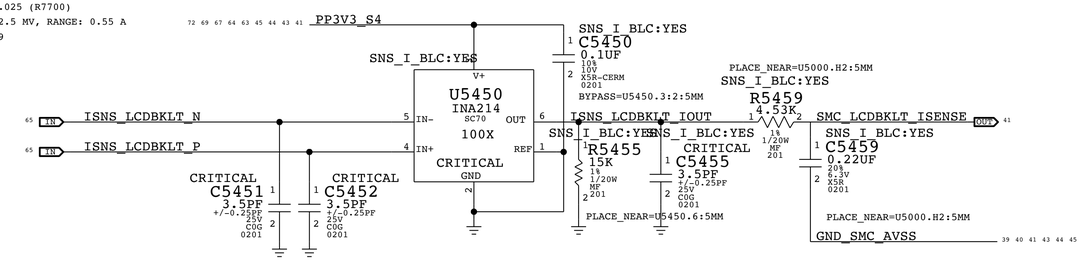
SSD NAND CURRENT SENSE (IHNC)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R5420)
VSENSE: 22.5 MV, RANGE: 1.42 A
SMC AD: 12



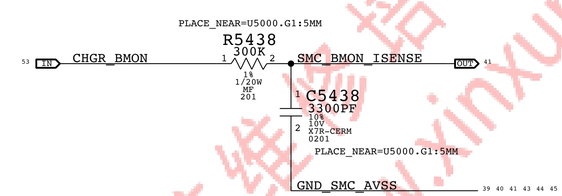
LCD BACKLIGHT CURRENT SENSE (IBLR)

GAIN: 100X. EDP: 0.9 A
Rsense: 0.025 (R7700)
VSENSE: 22.5 MV, RANGE: 0.55 A
SMC AD: 19



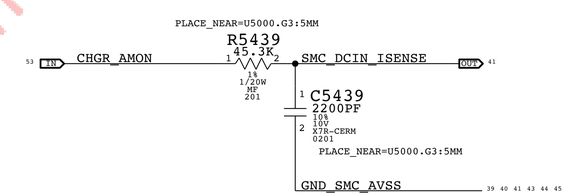
Charger (BMON) Current Sense (IPBR)

Charger Gain: 36x, EDP: 8 A
RSENSE: 0.005 (R7160)
SMC ADC: 03



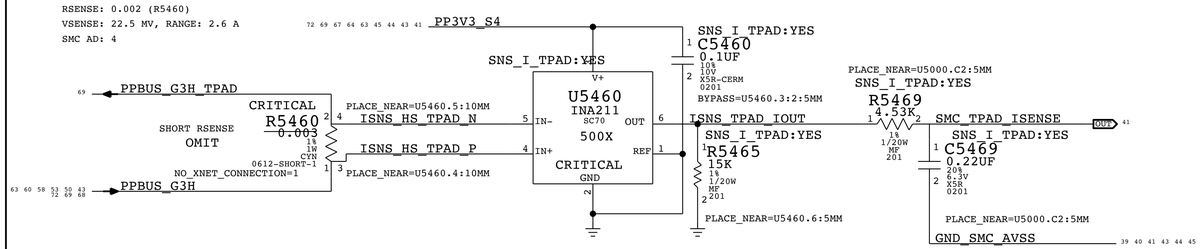
DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
RSENSE: 0.010 (R7120)
SMC ADC: 01



TRACKPAD ACTUATOR X239 CURRENT SENSE (ITAR)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R5460)
VSENSE: 22.5 MV, RANGE: 2.6 A
SMC AD: 4



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5429		SNS_I_SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		SNS_I_BLC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		SNS_I_TPAD:NO

BOM_COST_GROUP=SENSORS

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016
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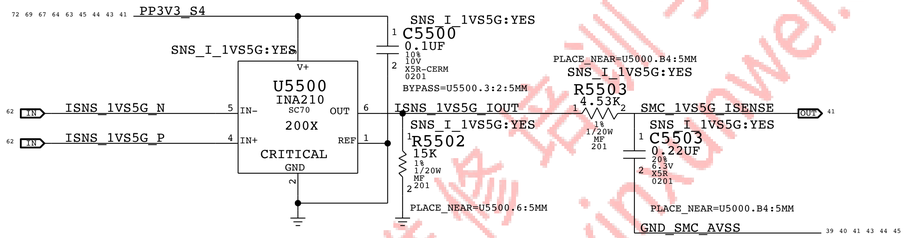
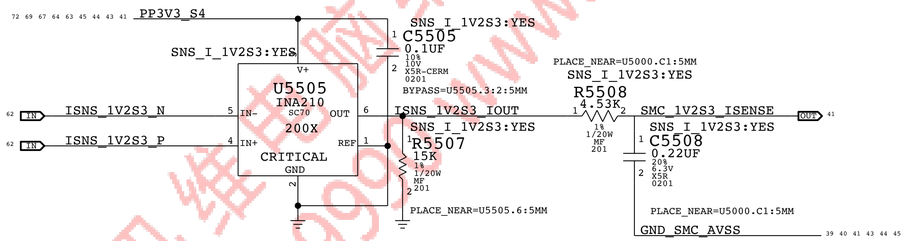
1V_S5G CURRENT SENSE (ISIC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7700)
VSENSE: 22.5 MV, RANGE: 3.0 A
SMC AD: 11



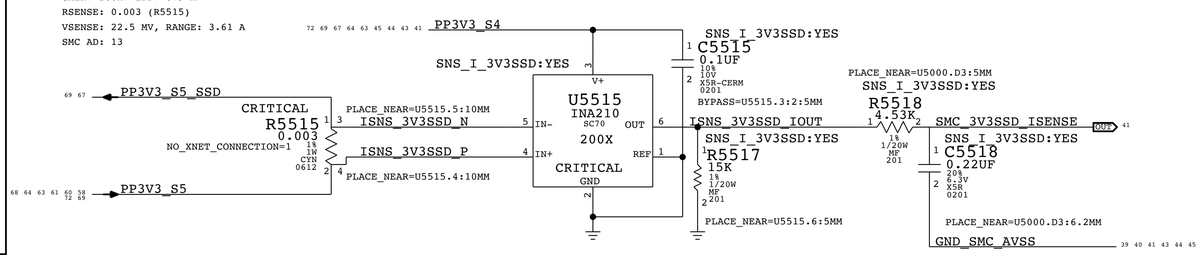
1V2_S3 CURRENT SENSE (IM0C)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 14



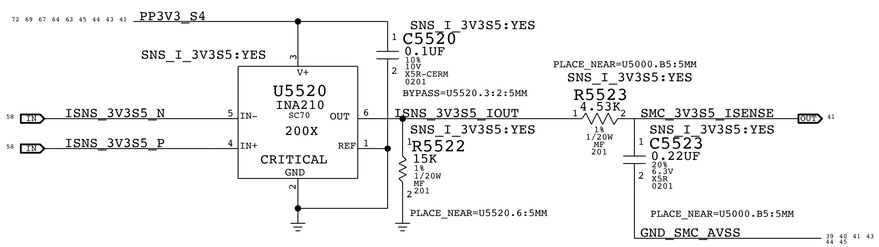
3V3_SSD CURRENT SENSE (IHCC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R5515)
VSENSE: 22.5 MV, RANGE: 3.61 A
SMC AD: 13



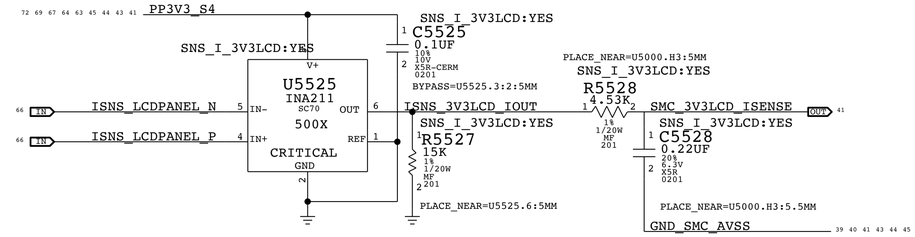
3V3_S5 CURRENT SENSE (IO3R) (HIGH-SIDE)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.003 (R7710)
VSENSE: 22.5 MV ?, RANGE: 4 A
SMC AD: 22



3V3_S0 LCD CURRENT SENSE (ILDC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R5525)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

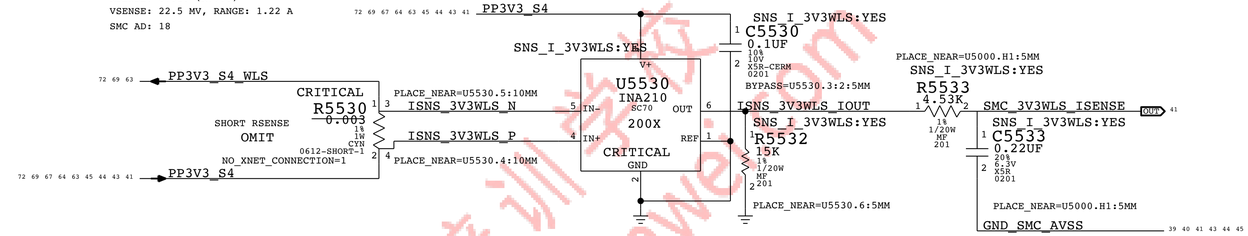


5V_S0 LCD CURRENT SENSE (I___)

GAIN: 500X. EDP: 0.9 A
RSENSE: 0.005 (R8520)
VSENSE: 22.5 MV, RANGE: 1.6 A
SMC AD: 17

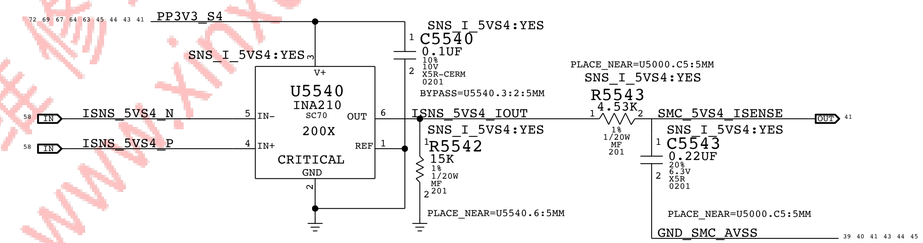
3V3_S4 WIRELESS CURRENT SENSE (IAPC)

GAIN: 200X. EDP: 0.9 A
RSENSE: 0.010 (R7700)
VSENSE: 22.5 MV, RANGE: 1.22 A
SMC AD: 18



5V_S4 CURRENT SENSE (IO5R) (HIGH-SIDE)

GAIN: 200X. EDP: ?? A
RSENSE: 0.003 (R7900)
VSENSE: 22.5 MV ?, RANGE: 6.8 A
SMC AD: 21



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5503		SNS_I_1VS5G:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5508		SNS_I_1V2S3:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5518		SNS_I_3V3SSD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5523		SNS_I_3V3S5:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5528		SNS_I_3V3LCD:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5533		SNS_I_3V3WLS:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5543		SNS_I_5VS4:NO

BOM_COST_GROUP=SENSORS

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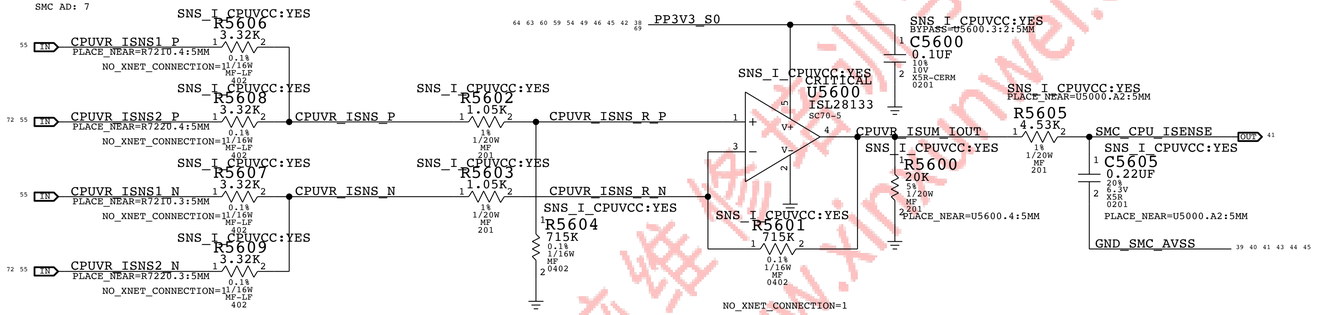
CPU VCC CURRENT SENSE (ICAC)

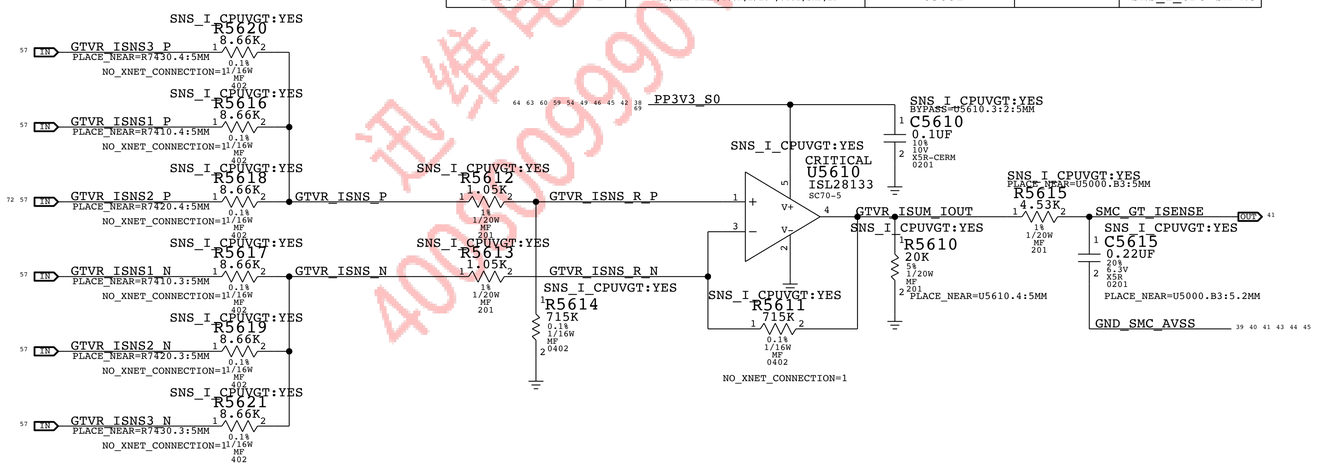
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 7



CPU GT CURRENT SENSE (ICGC)

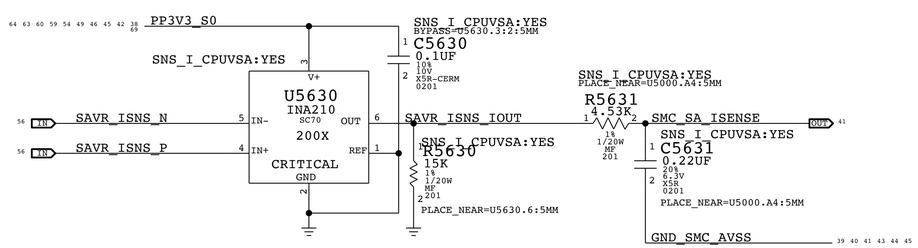
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.005 (R7700)
VSENSE: 22.5 MV, RANGE: 2.27 A
SMC AD: 9

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5605		SNS_I_CPUVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5615		SNS_I_CPUVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5631		SNS_I_CPUVSA:NO



CPU SA CURRENT SENSE (ICSC)

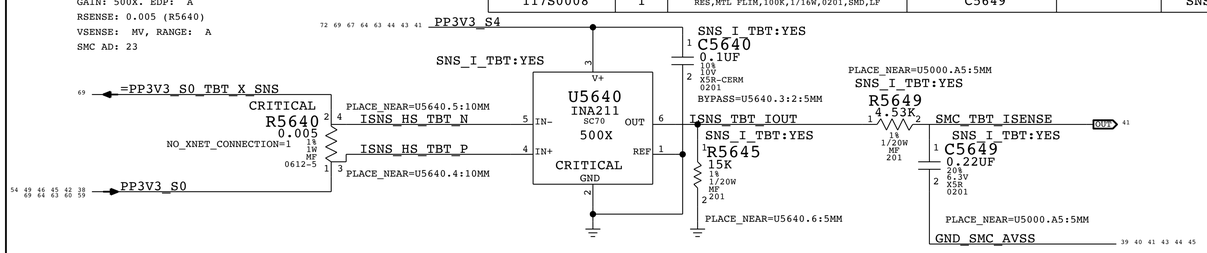
GAIN: 200X. EDP: 0.9 A
RSENSE: 0.002 (R7700)
VSENSE: 22.5 MV, RANGE: 7.67 A
SMC AD: 10



TBT CURRENT SENSE (IULC)

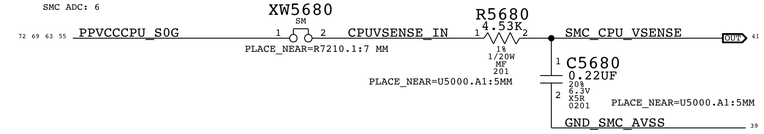
GAIN: 500X. EDP: A
RSENSE: 0.005 (R5640)
VSENSE: MV, RANGE: A
SMC AD: 23

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5649		SNS_I_TBT:NO



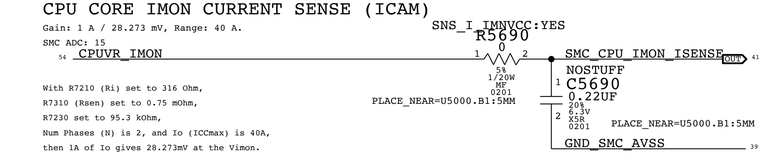
CPU CORE VOLTAGE SENSE (VCAC)

SMC ADC: 6



CPU CORE IMON CURRENT SENSE (ICAM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 15

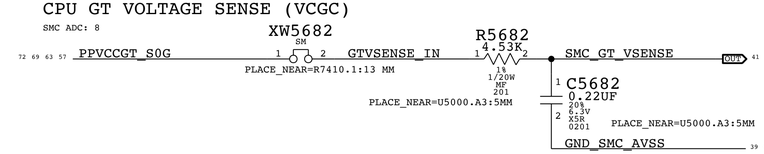


With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5690		SNS_I_IMNVCC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5692		SNS_I_IMNVGT:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5691		SNS_I_IMNVSA:NO

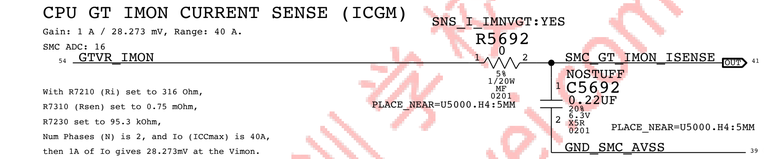
CPU GT VOLTAGE SENSE (VCGC)

SMC ADC: 8



CPU GT IMON CURRENT SENSE (ICGM)

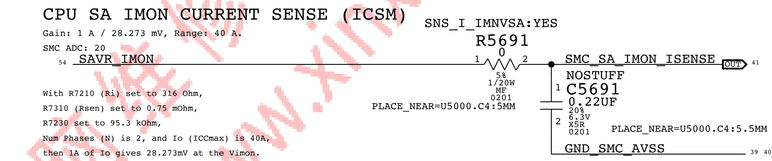
Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 16



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

CPU SA IMON CURRENT SENSE (ICSM)

Gain: 1 A / 28.273 mV, Range: 40 A.
SMC ADC: 20



With R7210 (Ri) set to 316 Ohm,
R7310 (Rsen) set to 0.75 mOhm,
R7230 set to 95.3 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 40A,
then 1A of Io gives 28.273mV at the Vimon.

BOM_COST_GROUP=SENSORS

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Power Sensors Extended

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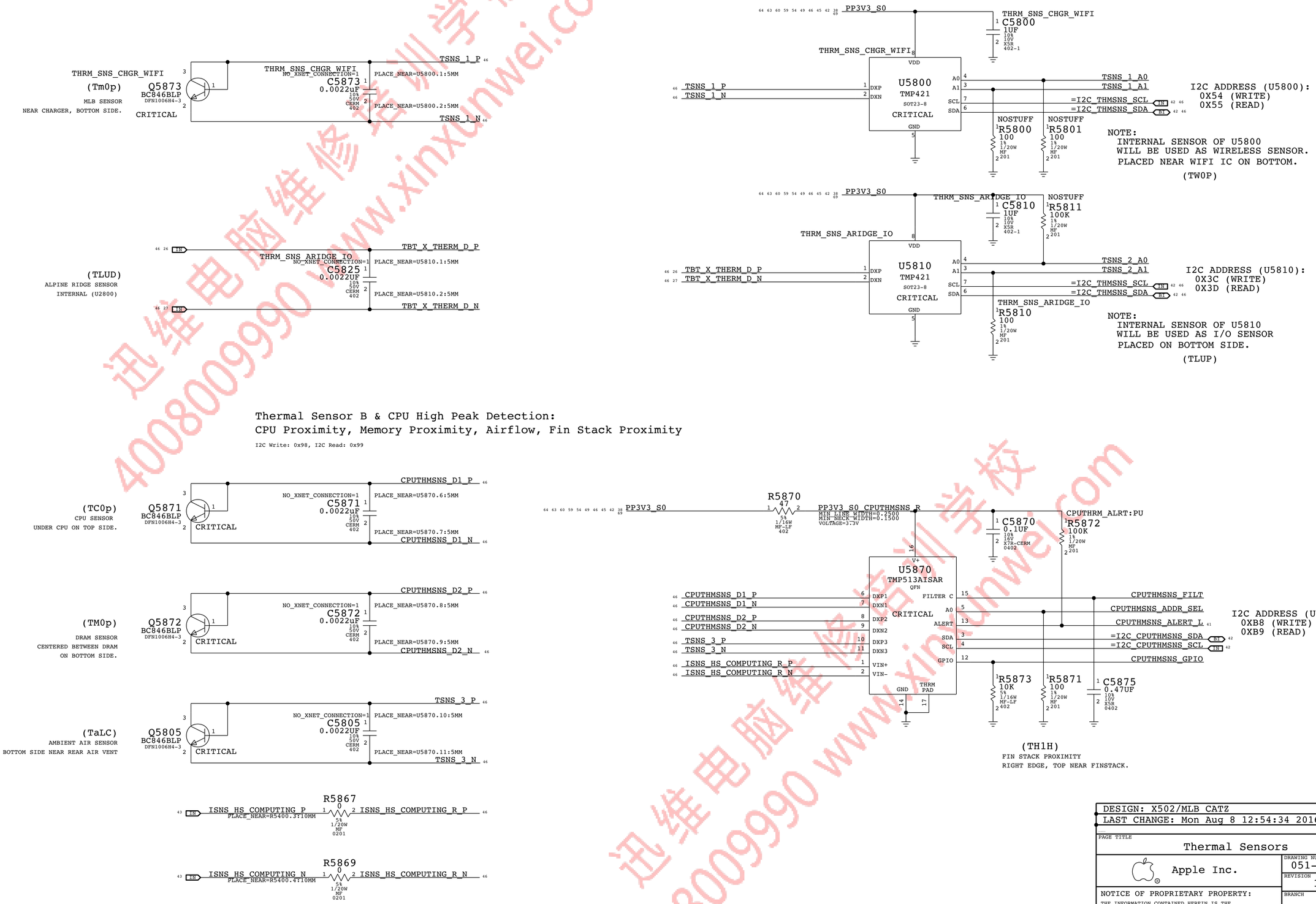

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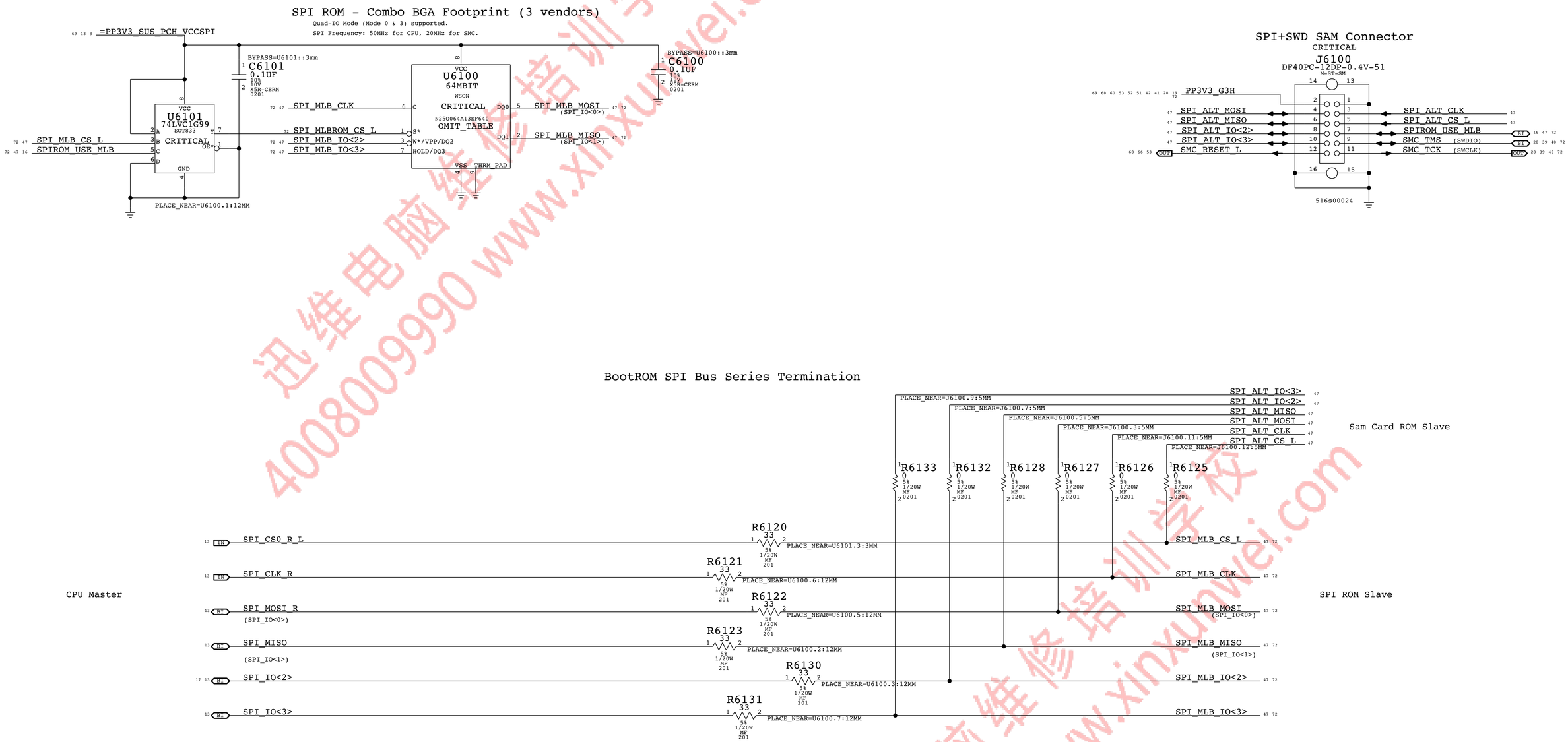

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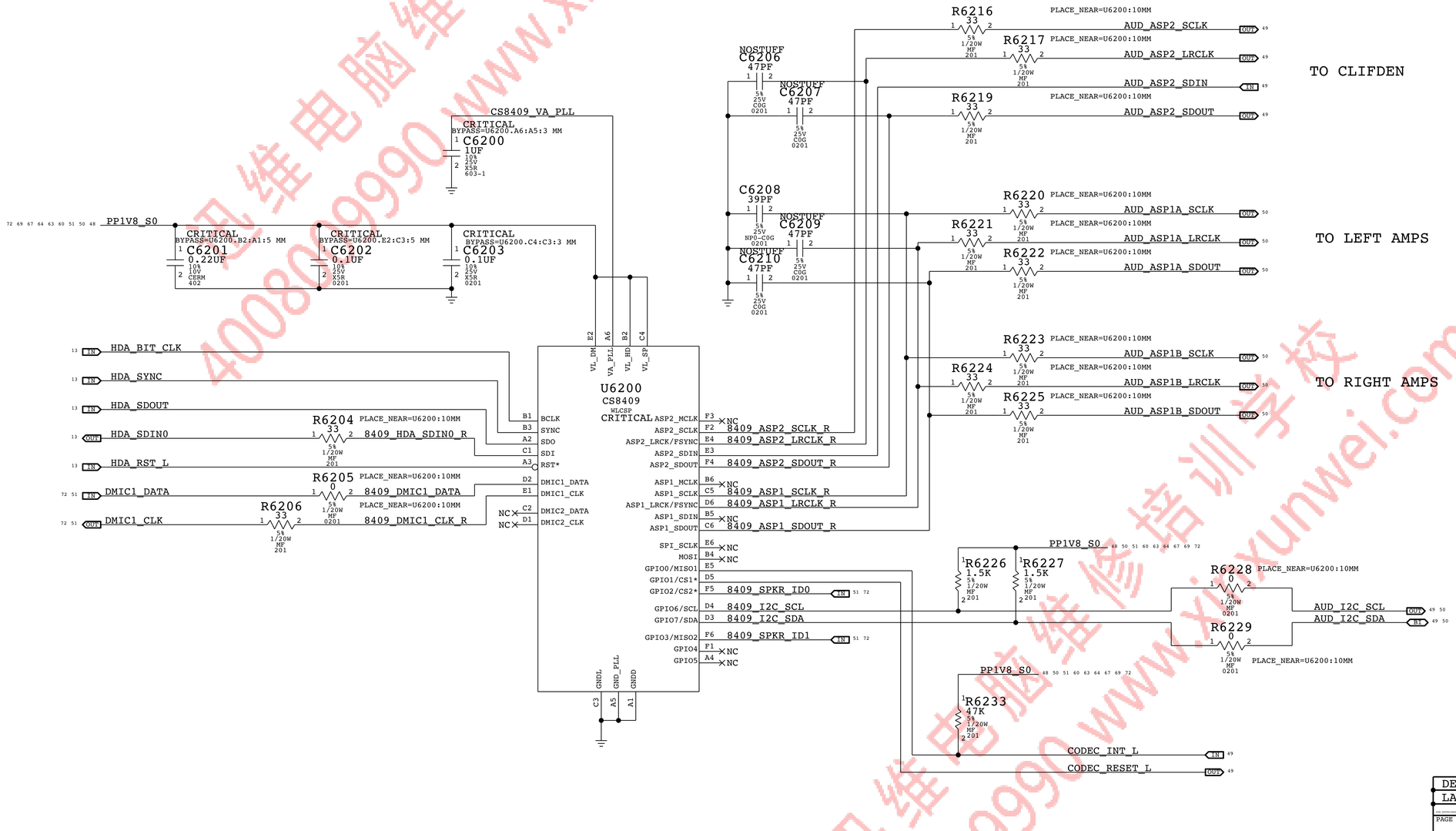

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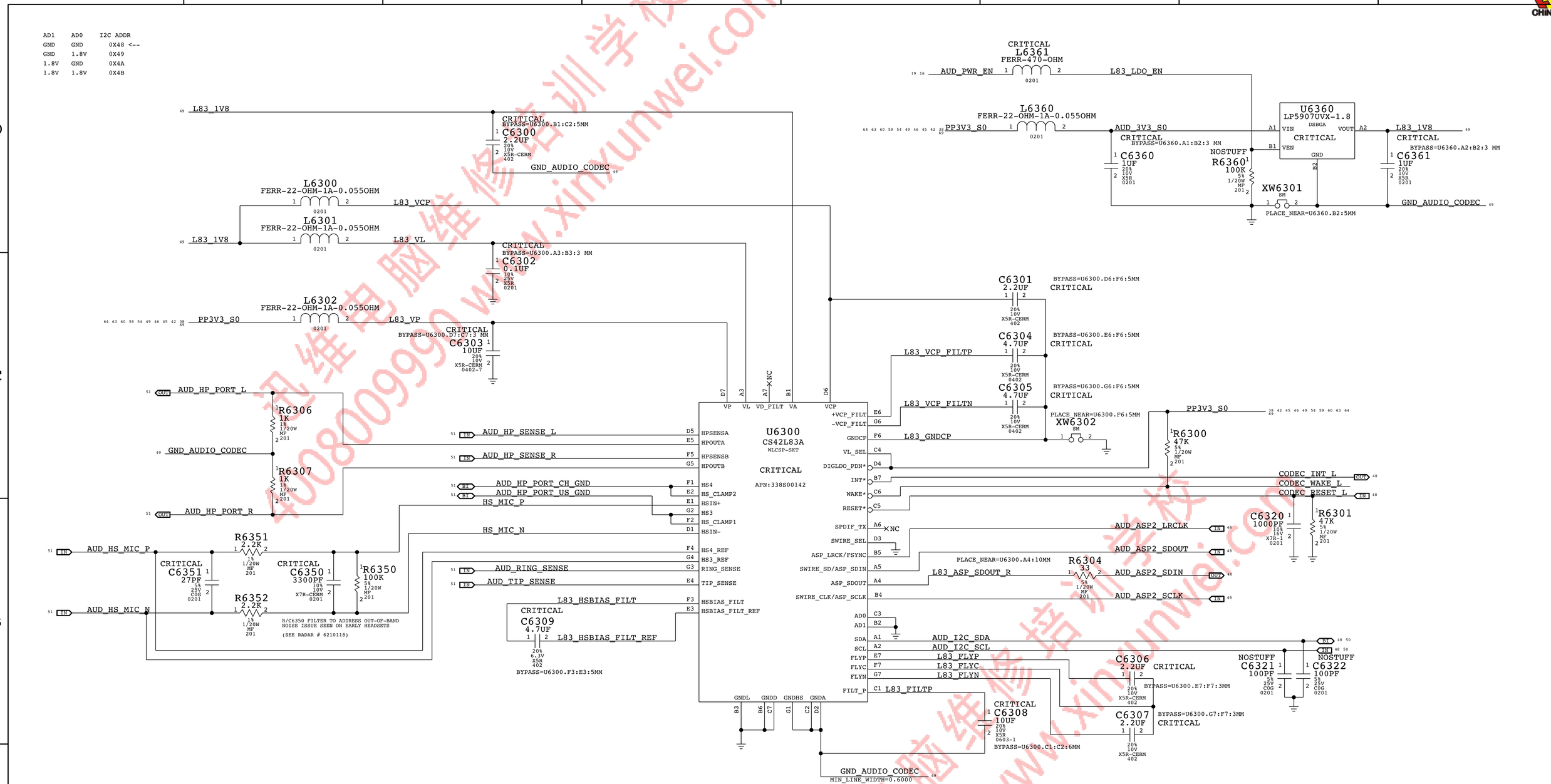

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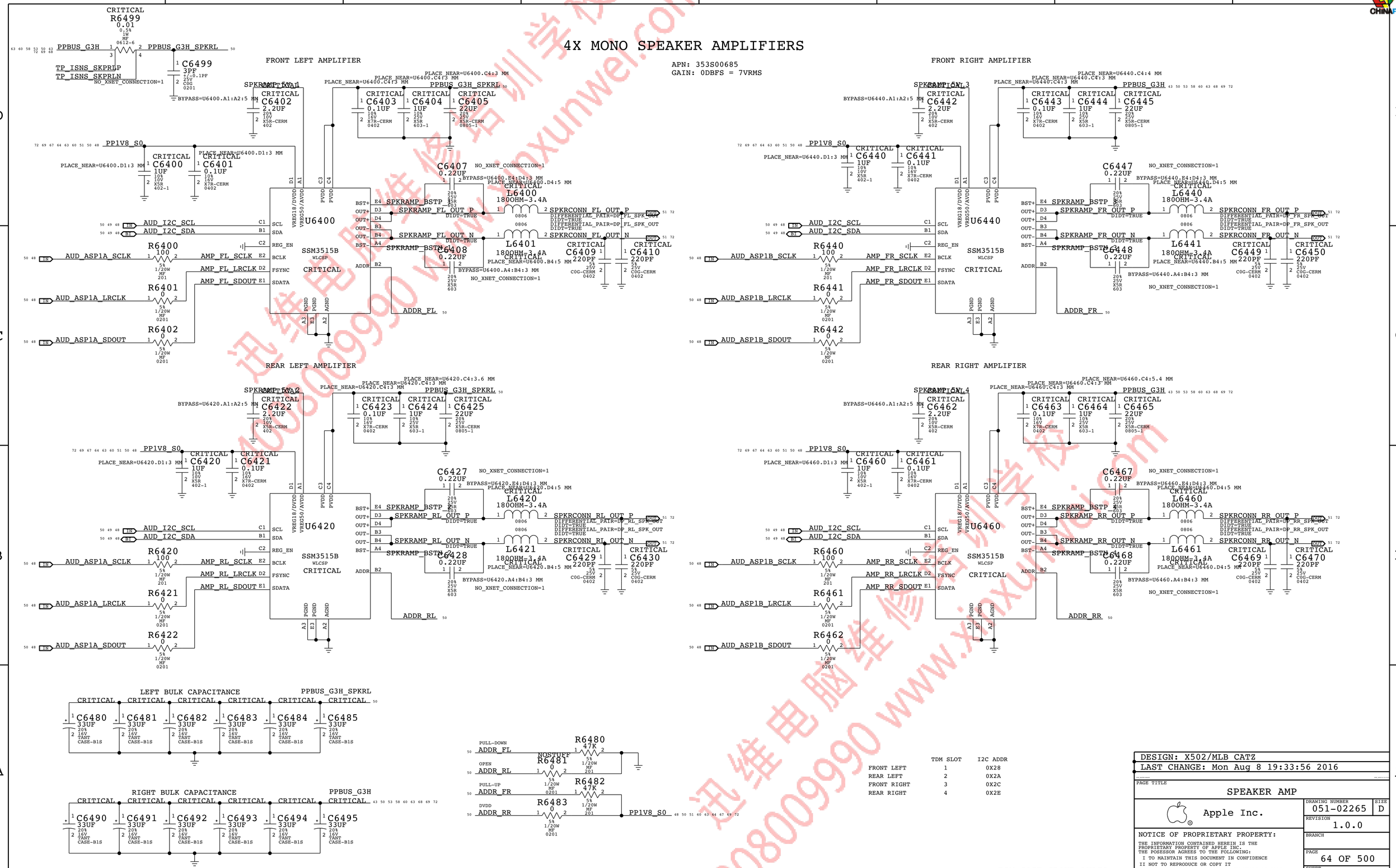
4X MONO SPEAKER AMPLIFIERS

APN: 353S00685
GAIN: 0DBFS = 7VRMS



	TDM SLOT	I2C ADDR
FRONT LEFT	1	0X28
REAR LEFT	2	0X2A
FRONT RIGHT	3	0X2C
REAR RIGHT	4	0X2E

BOM_COST_GROUP=AUDIO

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 19:33:56 2016

PAGE TITLE
SPEAKER AMP

Apple Inc.

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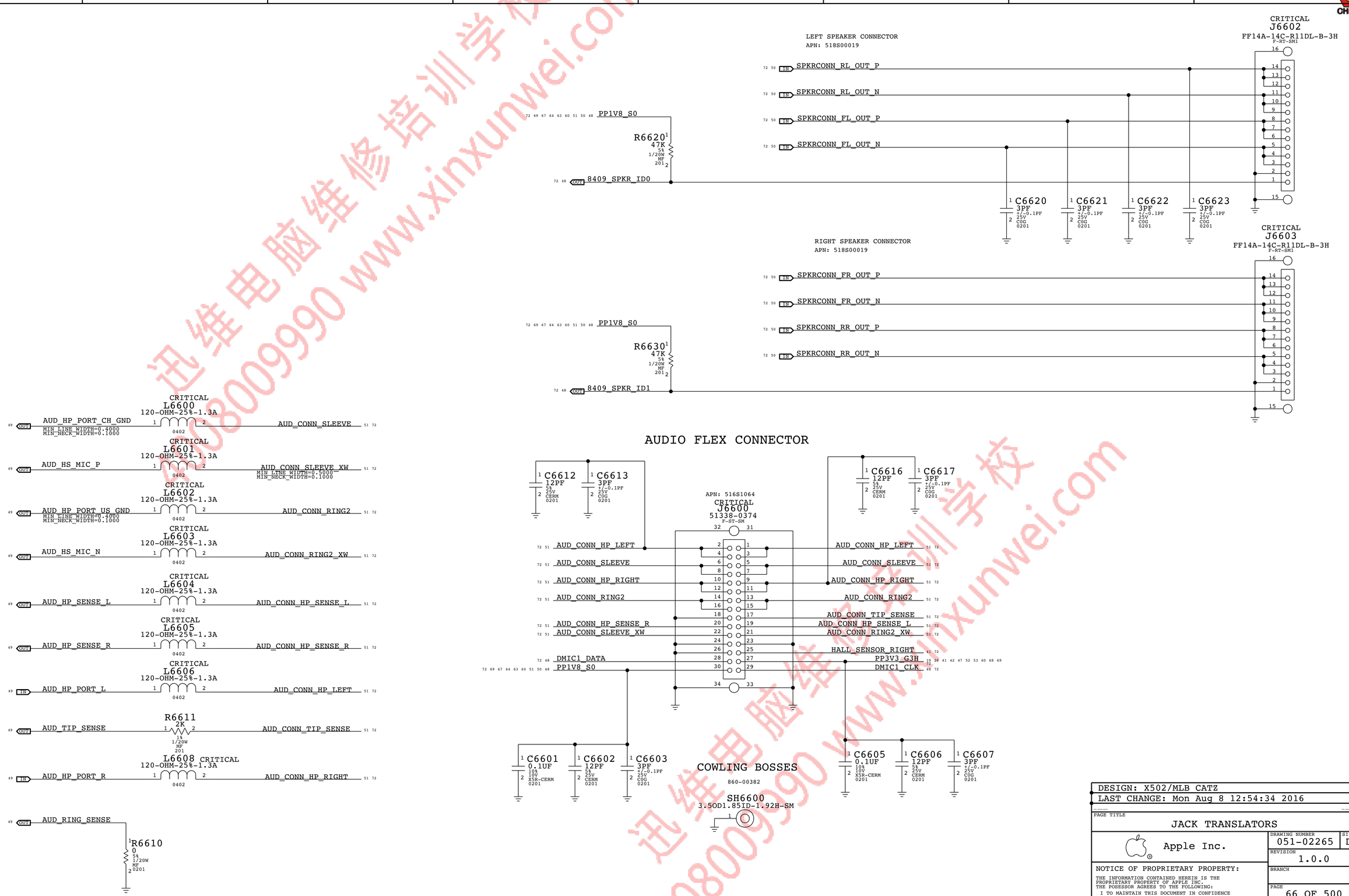

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
JACK TRANSLATORS

Apple Inc.

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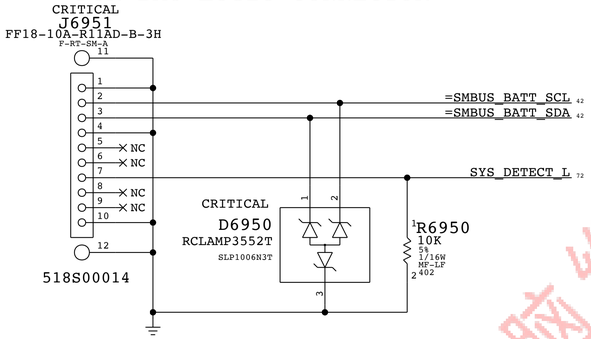
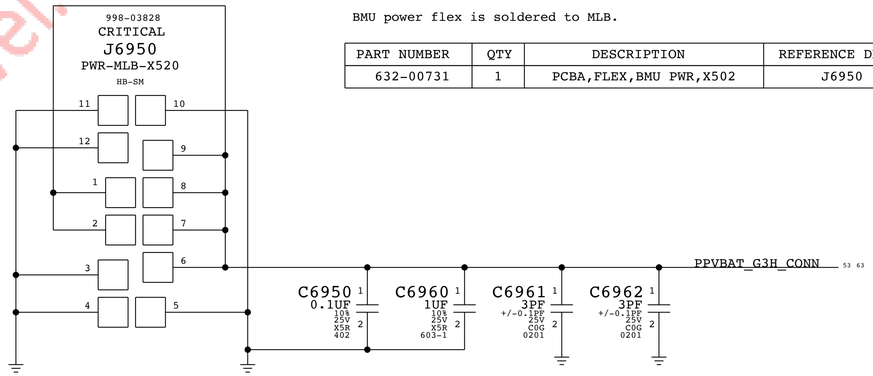
POR BMU LOGIC CONNECTOR



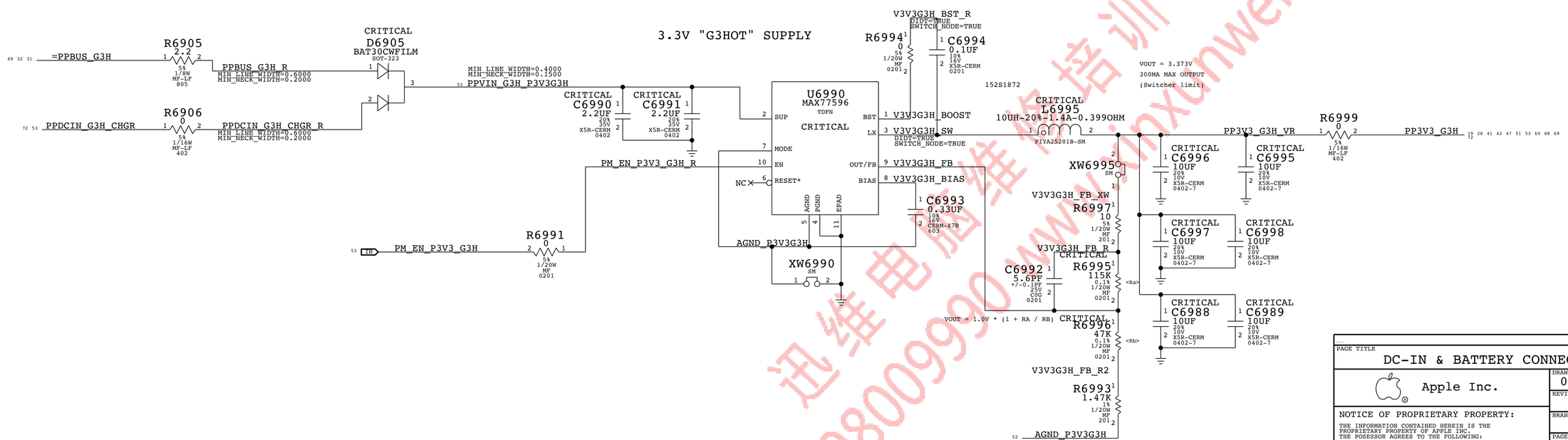
POR BATTERY (BMU) FLEX SOLDER PADS.



BMU power flex is soldered to MLB.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00731	1	PCBA,FLEX,BMU PWR,X502	J6950	CRITICAL	

3.3V "G3HOT" SUPPLY



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
DC-IN & BATTERY CONNECTORS

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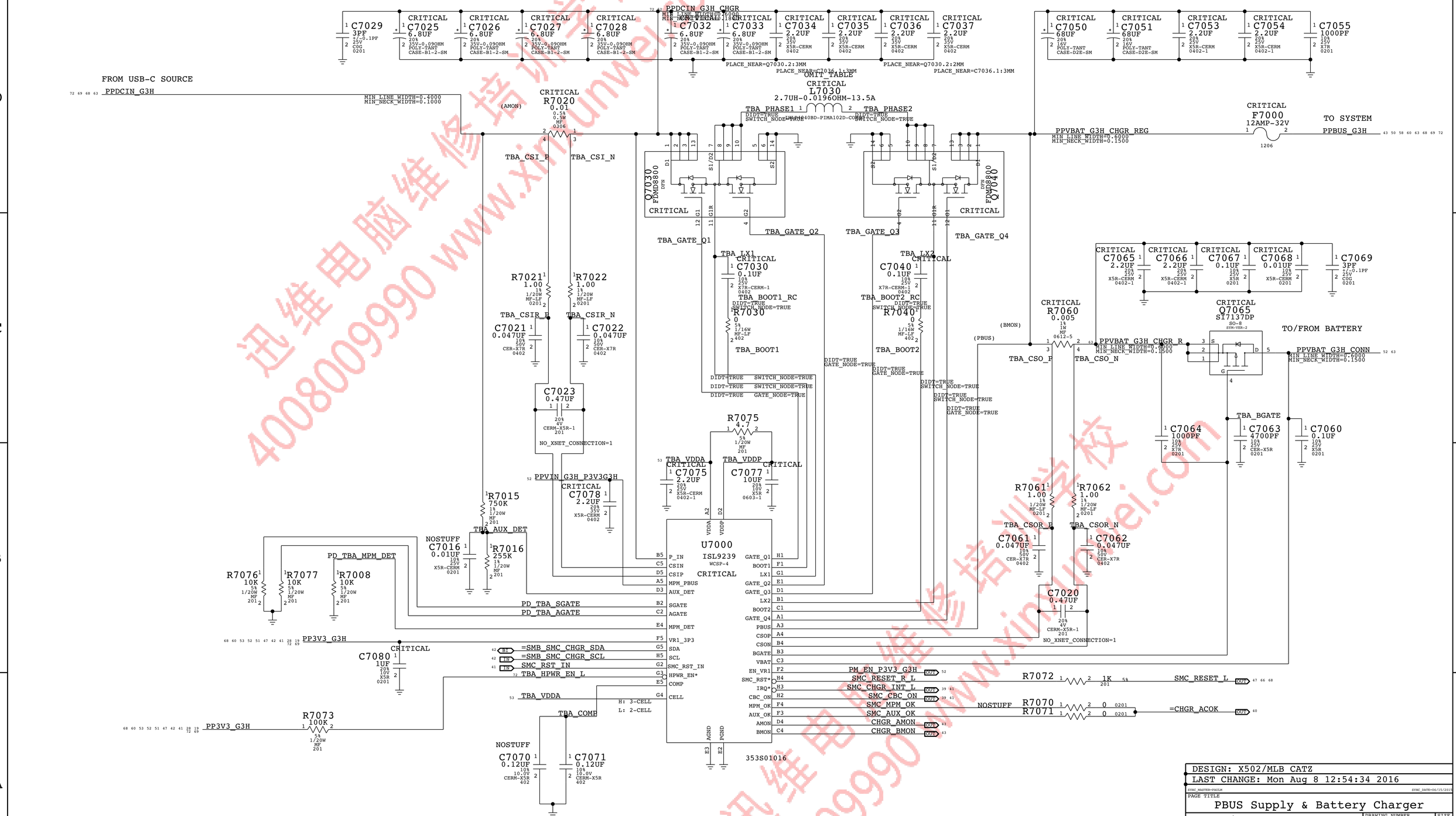

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

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PAGE TITLE
PBUS Supply & Battery Charger

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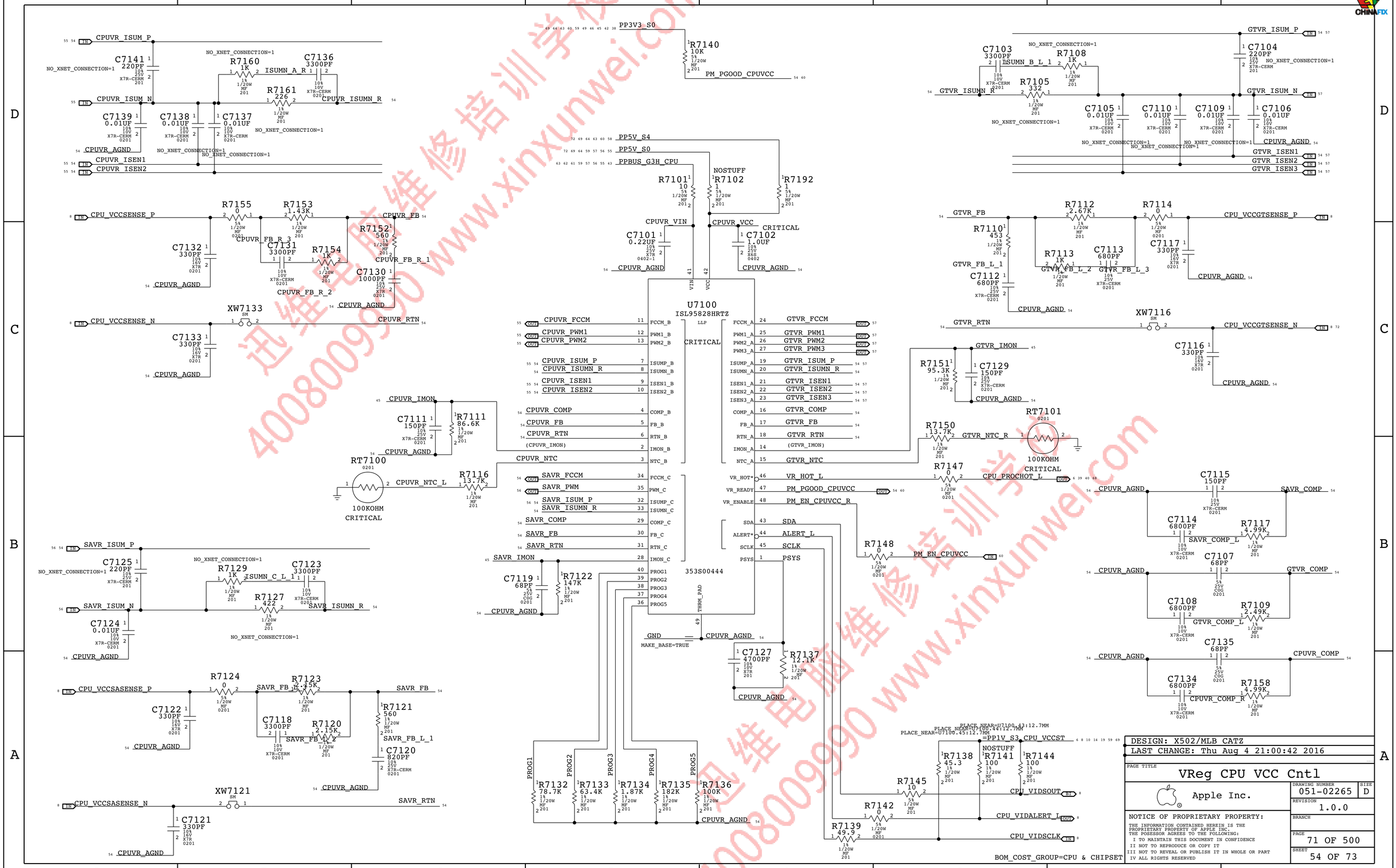

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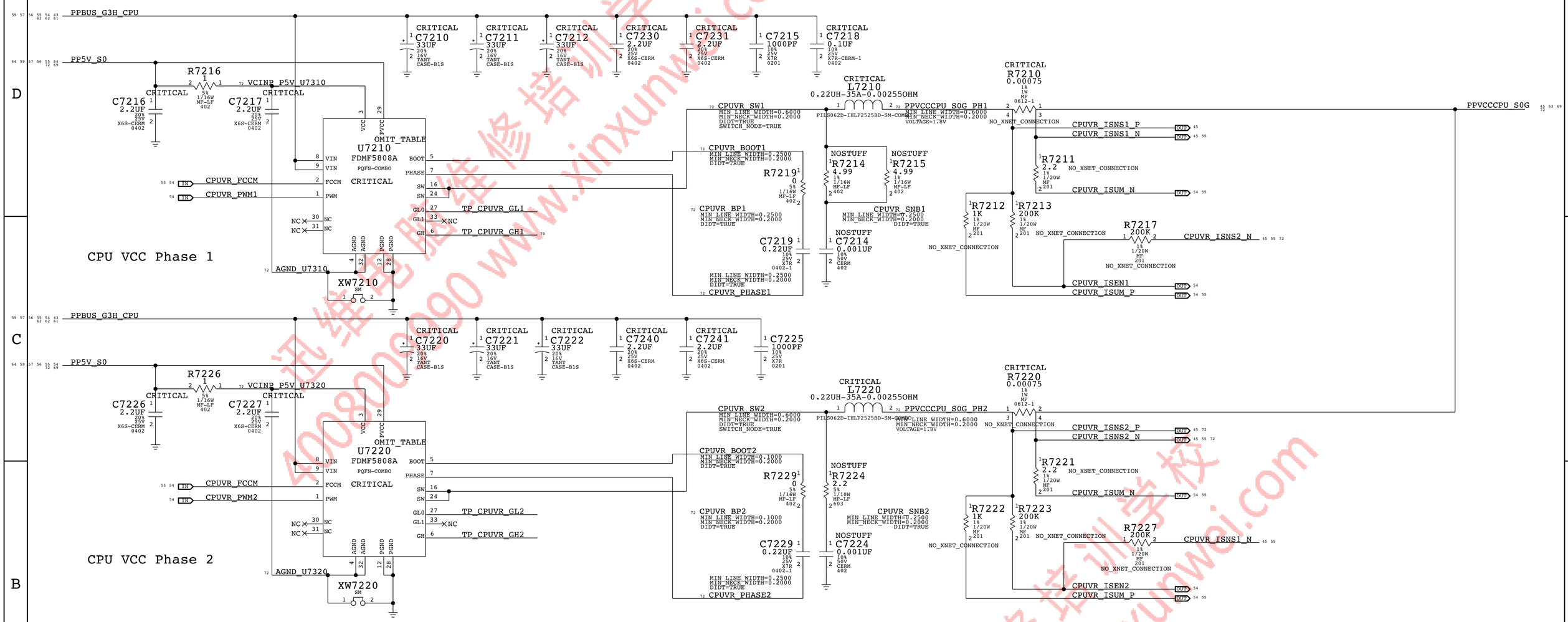

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	5	IC,SIC635,DR MOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7410,U7420,U7430	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
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PAGE TITLE
CPU IMVP VCC & VCCSA

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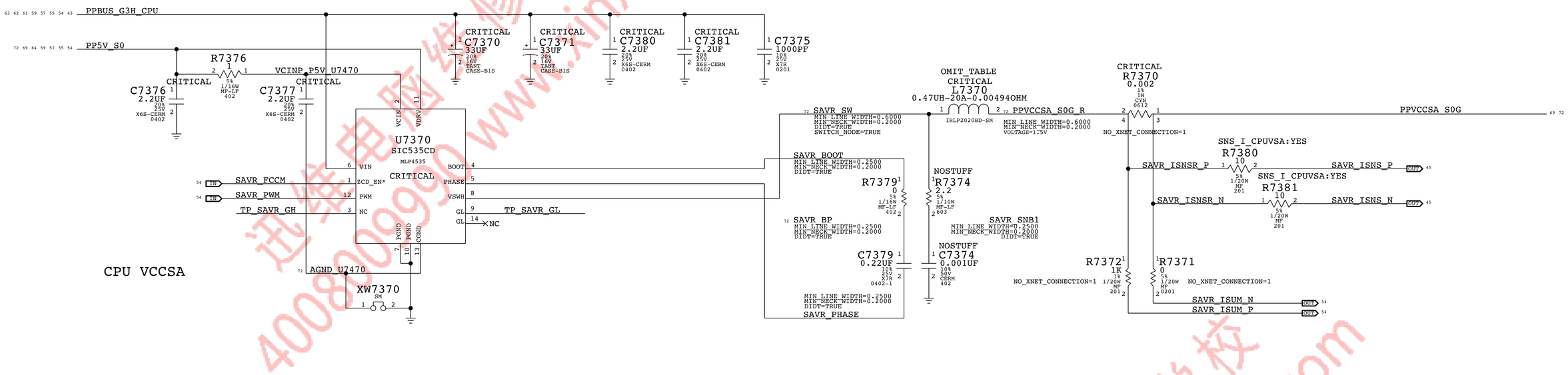
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00241	1	IND,MLD,0.47UH,4.9MO,17.5A,5.4X5.2X2.4MM	L7370	CRITICAL	



BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB CATZ
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PAGE TITLE
IMVP VCCSA

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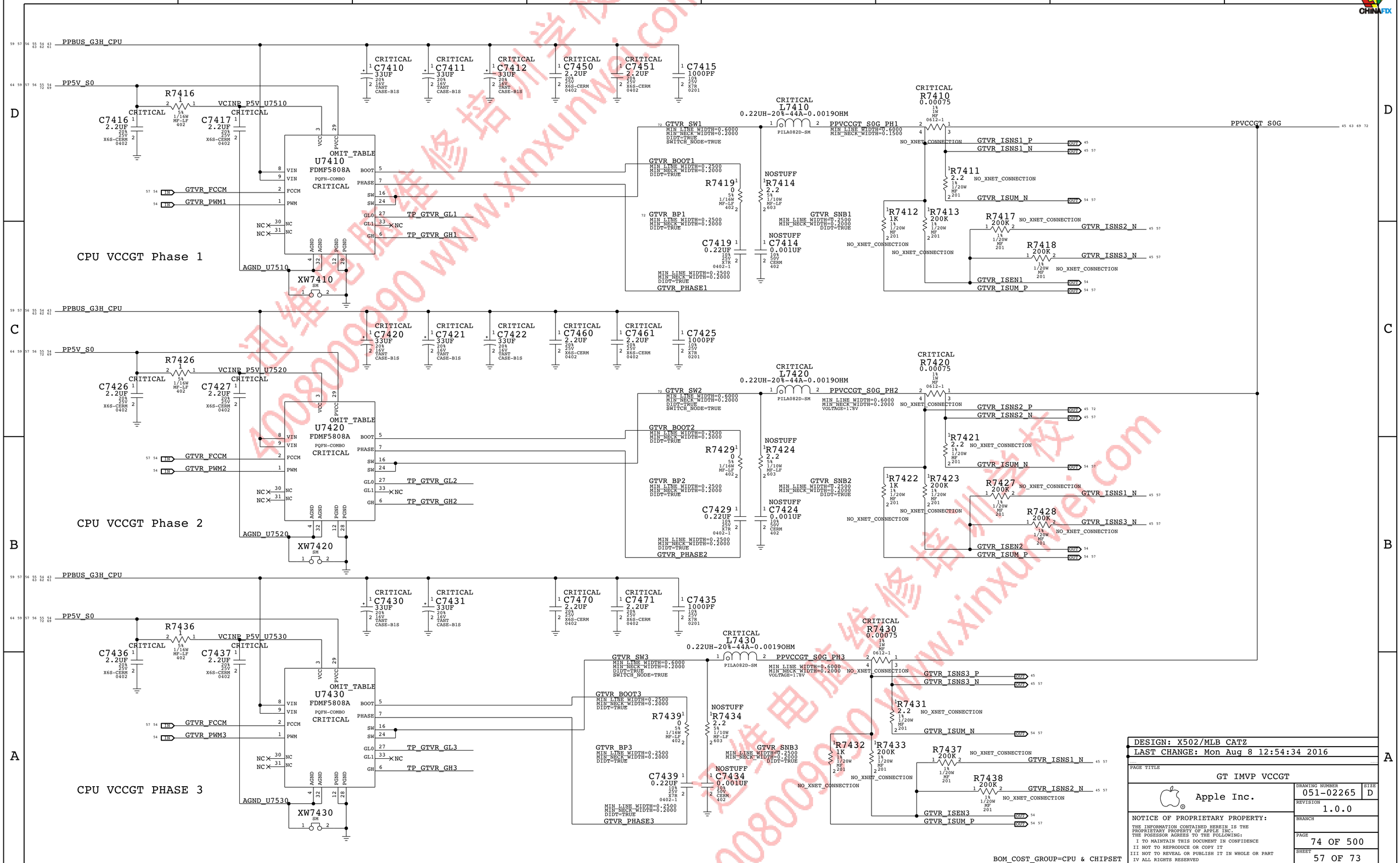
PPBUS_G3H_CPU
PP5V_S0
R7416 1 5% 1/16W MF-LF 402
VCINR_P5V_U7510
C7416 2.2UF 20% 25V X6S-CERM 0402
C7417 2.2UF 20% 25V X6S-CERM 0402
CRITICAL
C7410 33UF 20% 16V TANT CASE-B1S
C7411 33UF 20% 16V TANT CASE-B1S
C7412 33UF 20% 16V TANT CASE-B1S
C7450 2.2UF 20% 25V X6S-CERM 0402
C7451 2.2UF 20% 25V X6S-CERM 0402
C7415 1000PF 10% 25V X7R 0201
U7410
FDMF5808A
PQFN-COMBO
OMIT_TABLE
GTVR_FCCM
GTVR_PWM1
TP_GTVR_GL1
TP_GTVR_GH1
CPU VCCGT Phase 1
AGND_U7510
XW7410
L7410 0.22UH-20%-44A-0.0019OHM PILA082D-SM
PPVCCGT_S0G_PH1
GTVR_SW1
GTVR_BOOT1
GTVR_BP1
GTVR_PHASE1
R7419 0 5% 1/16W MF-LF 402
R7414 2.2 5% 1/10W MF-LF 603
NOSTUFF
C7419 0.22UF 10% 25V X7R 0402-1
C7414 0.001UF 10% 50V CERM 402
GTVR_SNB1
R7410 0.00075 1% 1W MF 0612-1
PPVCCGT_S0G
GTVR_ISNS1_P
GTVR_ISNS1_N
R7411 2.2 1% 1/20W MF 201
GTVR_ISUM_N
R7412 1K 1% 1/20W MF 201
R7413 200K 1% 1/20W MF 201
R7417 200K 1% 1/20W MF 201
GTVR_ISNS2_N
R7418 200K 1% 1/20W MF 201
GTVR_ISNS3_N
GTVR_ISEN1
GTVR_ISUM_P
NO_XNET_CONNECTION
PPBUS_G3H_CPU
PP5V_S0
R7426 1 5% 1/16W MF-LF 402
VCINR_P5V_U7520
C7426 2.2UF 20% 25V X6S-CERM 0402
C7427 2.2UF 20% 25V X6S-CERM 0402
C7420 33UF 20% 16V TANT CASE-B1S
C7421 33UF 20% 16V TANT CASE-B1S
C7422 33UF 20% 16V TANT CASE-B1S
C7460 2.2UF 20% 25V X6S-CERM 0402
C7461 2.2UF 20% 25V X6S-CERM 0402
C7425 1000PF 10% 25V X7R 0201
U7420
FDMF5808A
PQFN-COMBO
OMIT_TABLE
GTVR_FCCM
GTVR_PWM2
TP_GTVR_GL2
TP_GTVR_GH2
CPU VCCGT Phase 2
AGND_U7520
XW7420
L7420 0.22UH-20%-44A-0.0019OHM PILA082D-SM
PPVCCGT_S0G_PH2
GTVR_SW2
GTVR_BOOT2
GTVR_BP2
GTVR_PHASE2
R7429 0 5% 1/16W MF-LF 402
R7424 2.2 5% 1/10W MF-LF 603
NOSTUFF
C7429 0.22UF 10% 25V X7R 0402-1
C7424 0.001UF 10% 50V CERM 402
GTVR_SNB2
R7420 0.00075 1% 1W MF 0612-1
GTVR_ISNS2_P
GTVR_ISNS2_N
R7421 2.2 1% 1/20W MF 201
GTVR_ISUM_N
R7422 1K 1% 1/20W MF 201
R7423 200K 1% 1/20W MF 201
R7427 200K 1% 1/20W MF 201
GTVR_ISNS1_N
R7428 200K 1% 1/20W MF 201
GTVR_ISNS3_N
GTVR_ISEN2
GTVR_ISUM_P
PPBUS_G3H_CPU
PP5V_S0
R7436 1 5% 1/16W MF-LF 402
VCINR_P5V_U7530
C7436 2.2UF 20% 25V X6S-CERM 0402
C7437 2.2UF 20% 25V X6S-CERM 0402
C7430 33UF 20% 16V TANT CASE-B1S
C7431 33UF 20% 16V TANT CASE-B1S
C7470 2.2UF 20% 25V X6S-CERM 0402
C7471 2.2UF 20% 25V X6S-CERM 0402
C7435 1000PF 10% 25V X7R 0201
U7430
FDMF5808A
PQFN-COMBO
OMIT_TABLE
GTVR_FCCM
GTVR_PWM3
TP_GTVR_GL3
TP_GTVR_GH3
CPU VCCGT PHASE 3
AGND_U7530
XW7430
L7430 0.22UH-20%-44A-0.0019OHM PILA082D-SM
PPVCCGT_S0G_PH3
GTVR_SW3
GTVR_BOOT3
GTVR_BP3
GTVR_PHASE3
R7439 0 5% 1/16W MF-LF 402
R7434 2.2 5% 1/10W MF-LF 603
C7439 0.22UF 10% 25V X7R 0402-1
C7434 0.001UF 10% 50V CERM 402
GTVR_SNB3
R7430 0.00075 1% 1W MF 0612-1
GTVR_ISNS3_P
GTVR_ISNS3_N
R7431 2.2 1% 1/20W MF 201
GTVR_ISUM_N
R7432 1K 1% 1/20W MF 201
R7433 200K 1% 1/20W MF 201
R7437 200K 1% 1/20W MF 201
GTVR_ISNS1_N
R7438 200K 1% 1/20W MF 201
GTVR_ISNS2_N
GTVR_ISEN3
GTVR_ISUM_P
BOM_COST_GROUP=CPU & CHIPSET
DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016
PAGE TITLE
GT IMVP VCCGT
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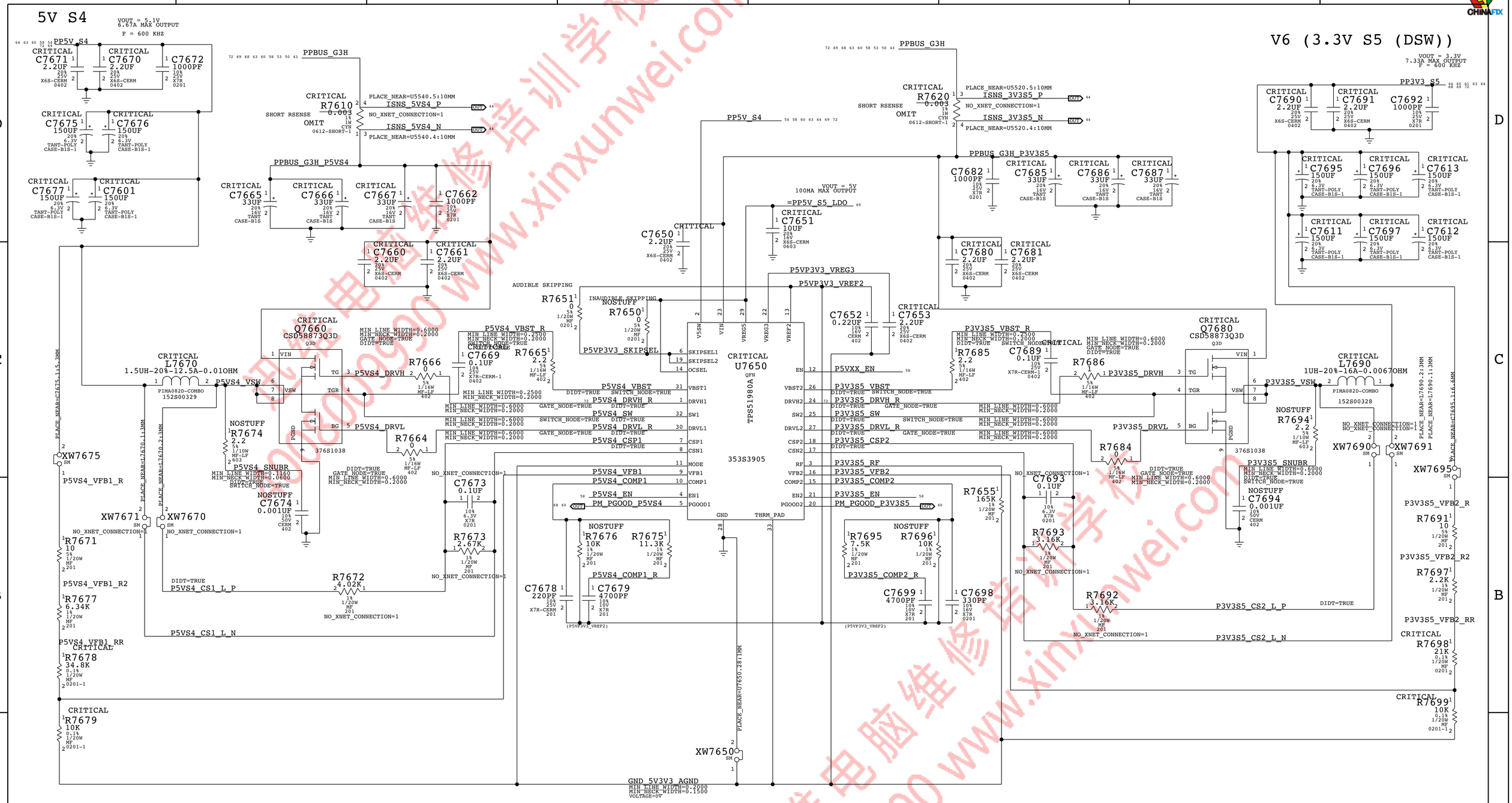

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LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
VR - 5V S4, 3.3V S5

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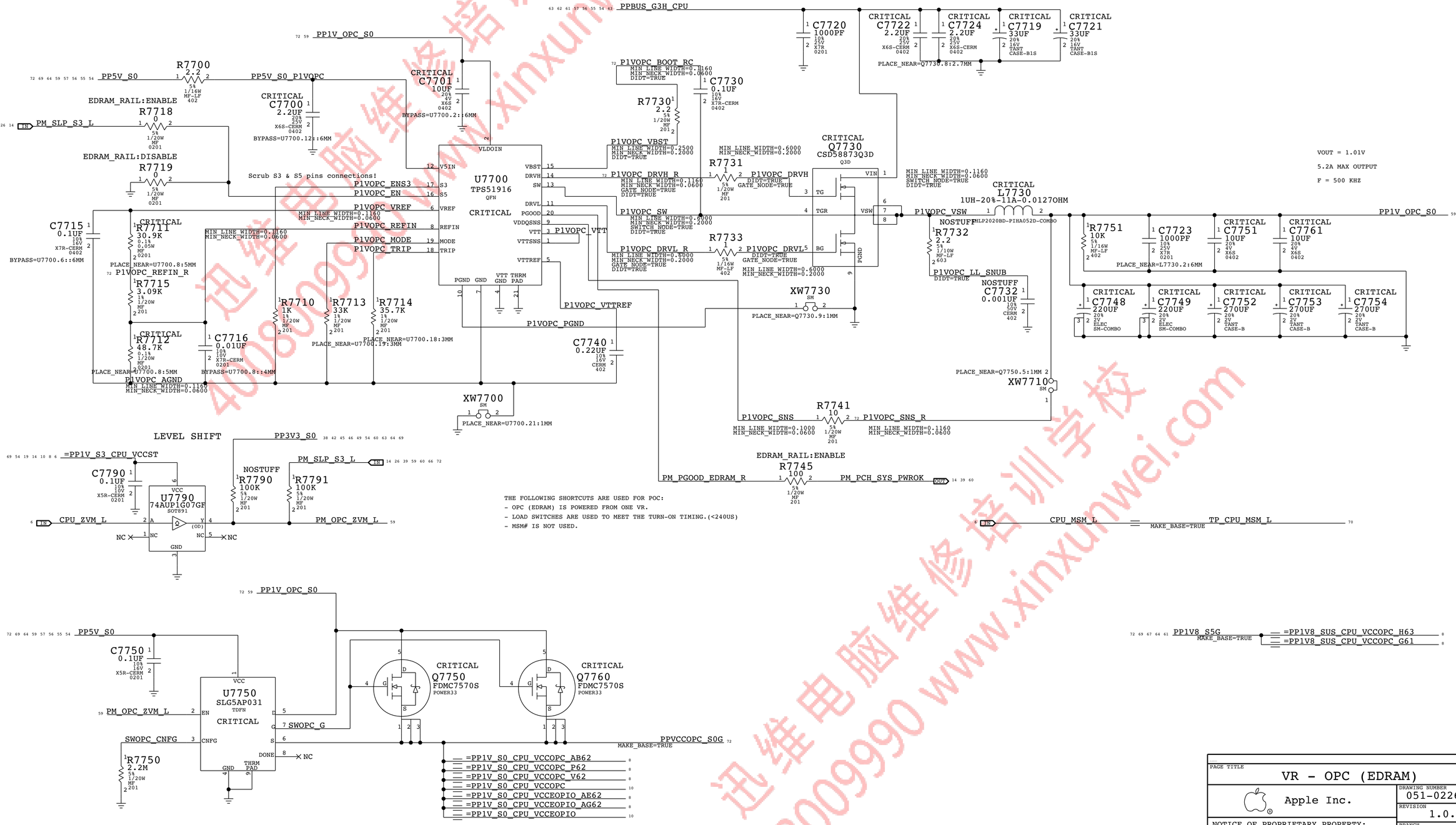
1V S0 REGULATOR FOR EDRAM (ON-PACKAGE CACHE)



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: VR - OPC (EDRAM)

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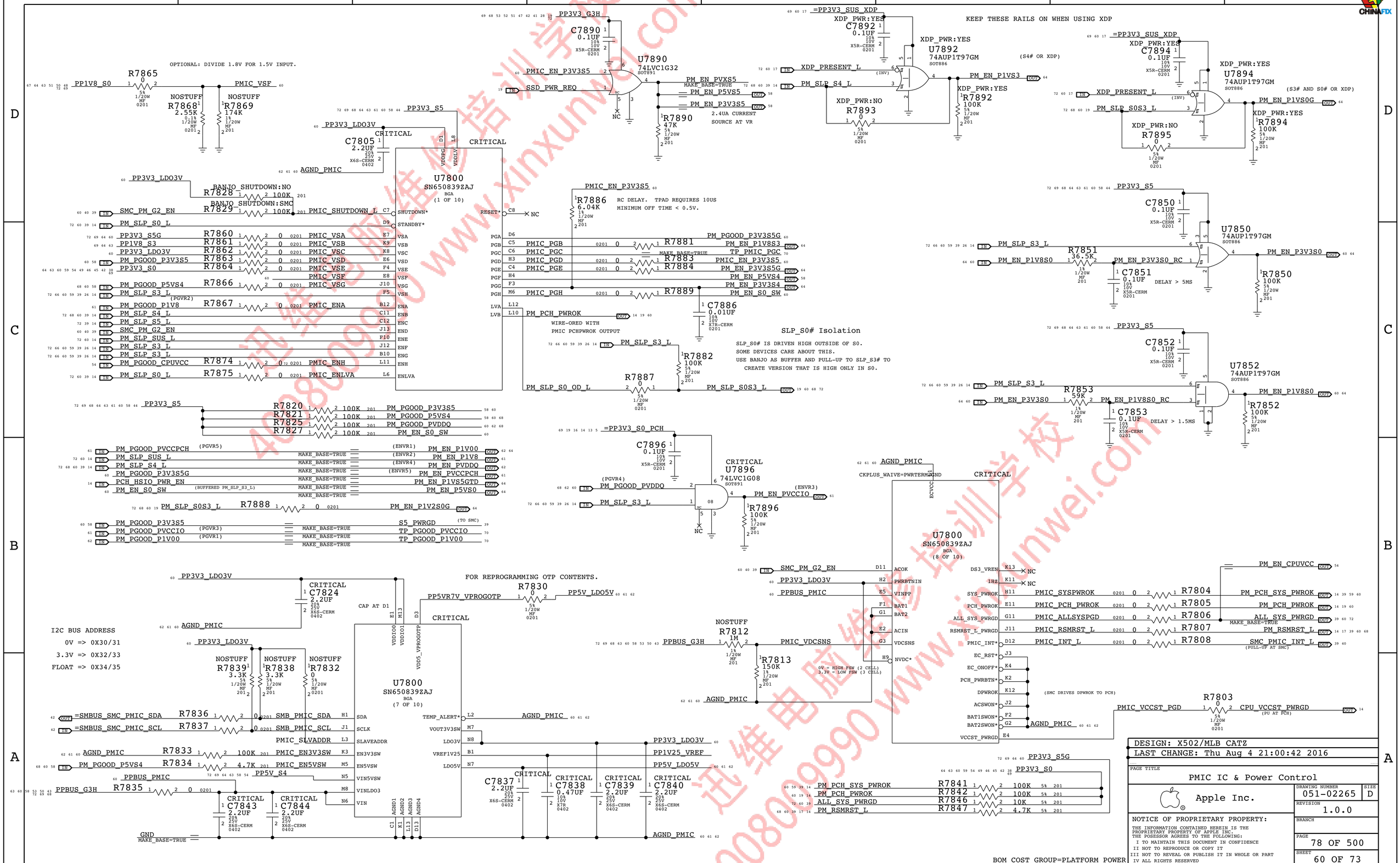

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
PMIC IC & Power Control

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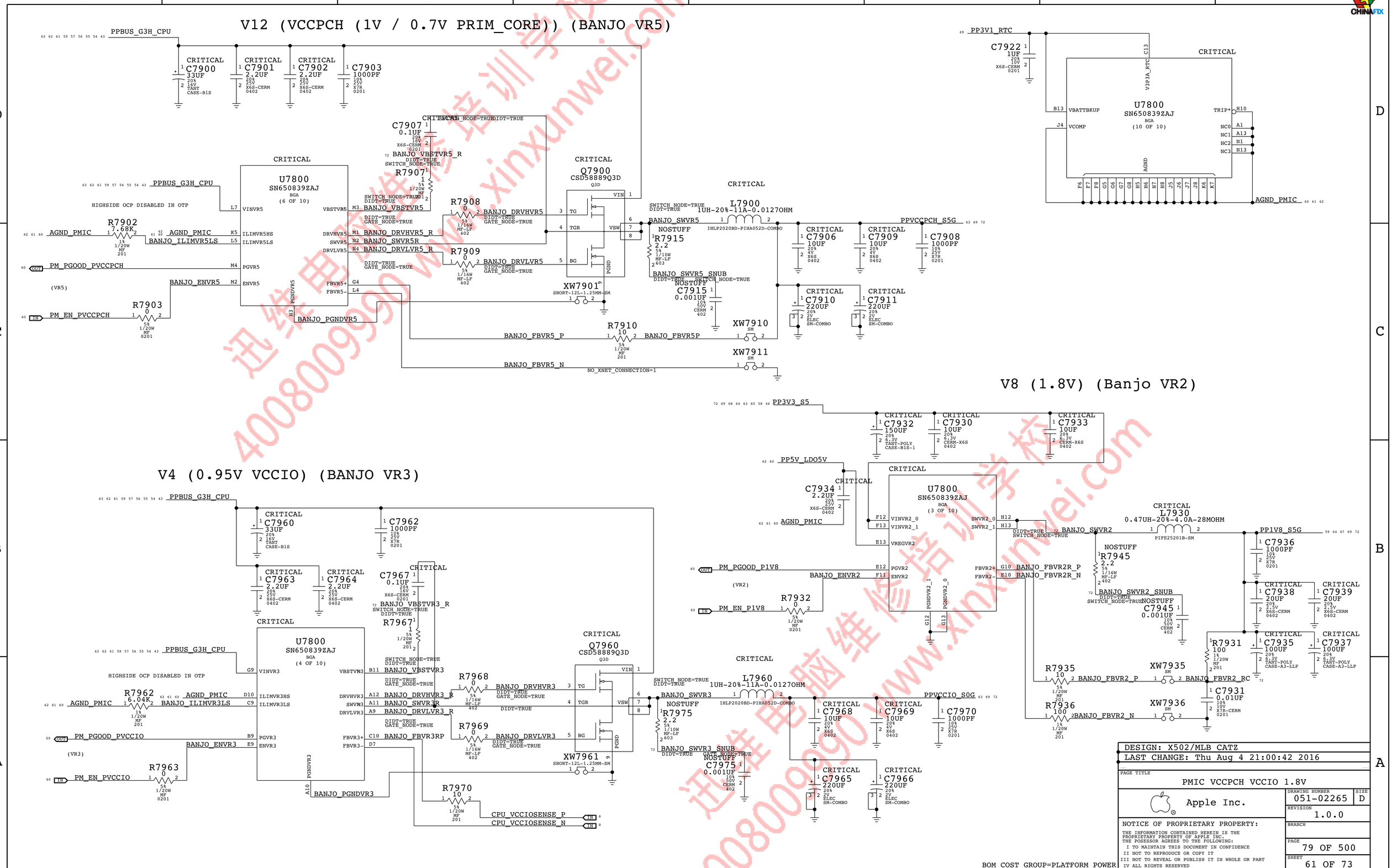

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PAGE TITLE
PMIC VCCPCH VCCIO 1.8V

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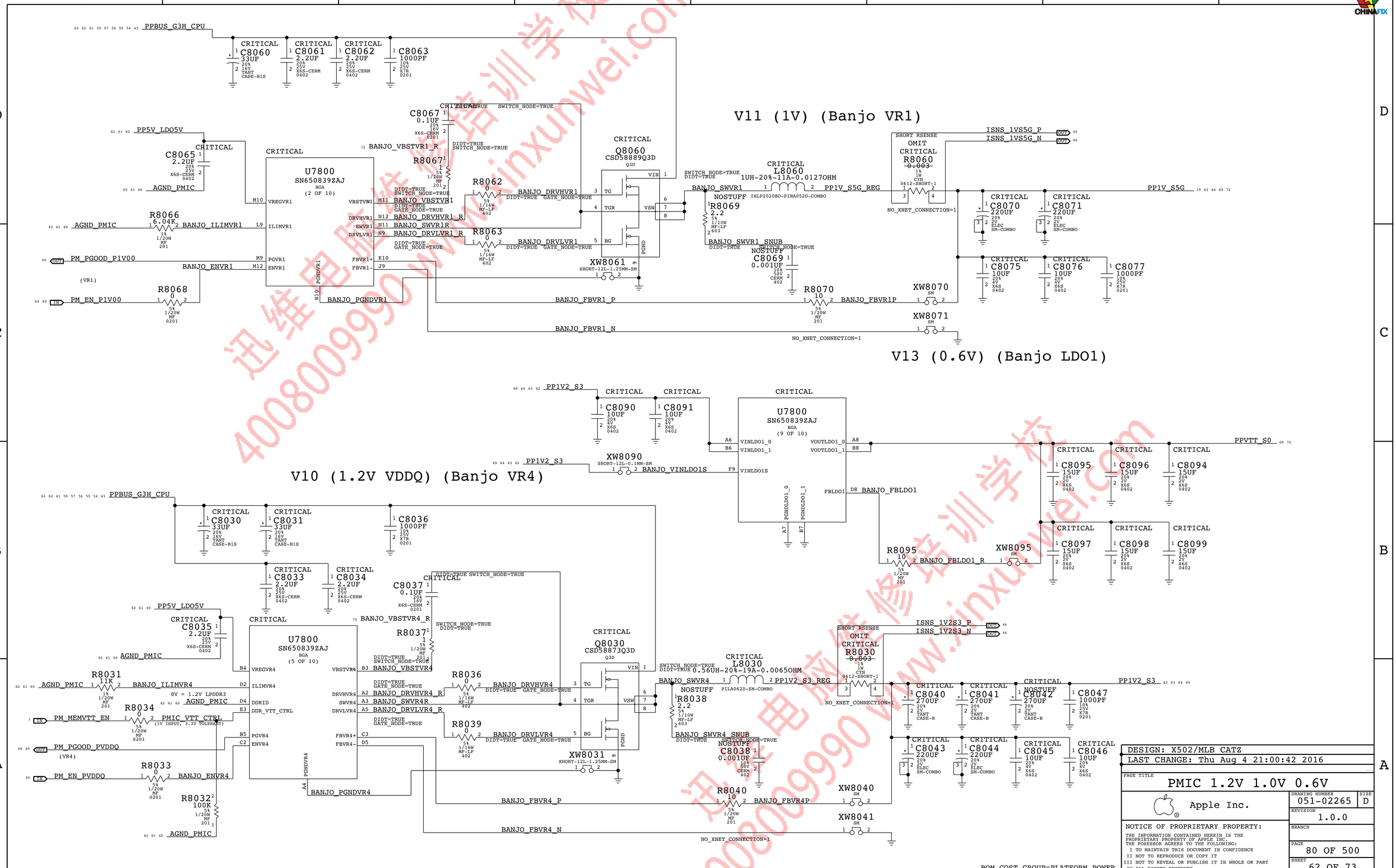

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PAGE TITLE
PMIC 1.2V 1.0V 0.6V

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69 64 63 62 PP1V2_S3	C8100 12PF 5% 25V CERM 0201	CRITICAL	C8101 3PF +/-0.1PF 25V C0G 0201	CRITICAL			
69 64 63 62 PP1V2_S3	C8102 3PF +/-0.1PF 25V C0G 0201		C8103 3PF +/-0.1PF 25V C0G 0201				
69 64 63 62 PP1V2_S3	C8104 3PF +/-0.1PF 25V C0G 0201		C8105 3PF +/-0.1PF 25V C0G 0201				
69 64 63 60 PP1V8_S3	C8106 3PF +/-0.1PF 25V C0G 0201		C8107 3PF +/-0.1PF 25V C0G 0201				
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8108 3PF +/-0.1PF 25V C0G 0201		C8109 3.5PF +/-0.25PF 25V C0G 0201				
72 69 68 64 63 61 60 58 44 PP3V3_S5	C8110 12PF 5% 25V CERM 0201		C8111 3PF +/-0.1PF 25V C0G 0201				
72 69 64 63 60 58 54 PP5V_S4	C8112 12PF 5% 25V CERM 0201		C8113 3.5PF +/-0.25PF 25V C0G 0201				
72 69 64 63 60 58 54 PP5V_S4	C8114 3.5PF +/-0.25PF 25V C0G 0201		C8115 3.5PF +/-0.25PF 25V C0G 0201				
72 69 64 63 60 58 54 PP5V_S4	C8116 12PF 5% 25V CERM 0201		C8117 3PF +/-0.1PF 25V C0G 0201				
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8118 3PF +/-0.1PF 25V C0G 0201		C8119 3PF +/-0.1PF 25V C0G 0201				
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8120 3PF +/-0.1PF 25V C0G 0201		C8121 3.5PF +/-0.25PF 25V C0G 0201				
72 69 68 53 PPDCIN_G3H	C8122 12PF 5% 25V CERM 0201		C8123 3PF +/-0.1PF 25V C0G 0201				
63 53 PPVBAT_G3H_CHGR_R	C8124 3PF +/-0.1PF 25V C0G 0201		C8125 3PF +/-0.1PF 25V C0G 0201				
63 53 PPVBAT_G3H_CHGR_R	C8126 3PF +/-0.1PF 25V C0G 0201		C8127 3PF +/-0.1PF 25V C0G 0201				
63 53 52 PPVBAT_G3H_CONN	C8128 12PF 5% 25V CERM 0201		C8129 3PF +/-0.1PF 25V C0G 0201				
63 53 52 PPVBAT_G3H_CONN	C8130 3PF +/-0.1PF 25V C0G 0201		C8131 3PF +/-0.1PF 25V C0G 0201				
72 69 55 45 PPVCCCPU_S0G	C8132 3PF +/-0.1PF 25V C0G 0201		C8133 3PF +/-0.1PF 25V C0G 0201				
72 69 67 64 63 60 51 50 48 PP1V8_S0	C8134 12PF 5% 25V CERM 0201	FREQUENCY SPECIFIC	C8135 3.0PF +/-0.1PF 25V NP0-C0G 0201	CRITICAL			
72 69 64 63 62 19 PP1V_S5G	C8137 3PF +/-0.1PF 25V C0G 0201						
72 69 64 63 62 19 PP1V_S5G	C8138 3PF +/-0.1PF 25V C0G 0201				NOSTUFF		
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8136 3PF +/-0.1PF 25V C0G 0201						
67 64 63 45 44 43 41 72 69 PP3V3_S4	C8139 3PF +/-0.1PF 25V C0G 0201				NOSTUFF		
69 64 63 62 PP1V2_S3	C8140 12PF 5% 25V CERM 0201	NOSTUFF	C8141 3PF +/-0.1PF 25V C0G 0201				
69 64 63 62 PP1V2_S3	C8142 12PF 5% 25V CERM 0201	NOSTUFF	C8143 3PF +/-0.1PF 25V C0G 0201				
69 64 63 62 PP1V2_S3	C8144 12PF 5% 25V CERM 0201	NOSTUFF	C8145 3PF +/-0.1PF 25V C0G 0201				
69 64 63 62 PP1V2_S3	C8146 12PF 5% 25V CERM 0201	NOSTUFF	C8147 3PF +/-0.1PF 25V C0G 0201				
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8148 12PF 5% 25V CERM 0201		C8149 3PF +/-0.1PF 25V C0G 0201				
69 64 63 60 PP1V8_S3	C8150 12PF 5% 25V CERM 0201	NOSTUFF	C8151 3PF +/-0.1PF 25V C0G 0201				
69 64 63 62 PP1V2_S3	C8152 3PF +/-0.1PF 25V C0G 0201		C8153 3PF +/-0.1PF 25V C0G 0201				
69 64 63 60 PP1V8_S3	C8155 3PF +/-0.1PF 25V C0G 0201						
67 PPBUS_SSD_FLT	C8157 3.5PF +/-0.25PF 25V C0G 0201						
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8158 3PF +/-0.1PF 25V C0G 0201		C8159 3PF +/-0.1PF 25V C0G 0201				
69 64 63 PP5V_S5	C8154 3PF +/-0.1PF 25V C0G 0201						
69 64 63 PP5V_S5	C8156 3PF +/-0.1PF 25V C0G 0201						
63 28 27 PP3V3_TBT_X_LC	C8160 12PF 5% 25V CERM 0201		C8161 3PF +/-0.1PF 25V C0G 0201				
63 28 27 PP3V3_TBT_X_LC	C8162 12PF 5% 25V CERM 0201		C8163 3PF +/-0.1PF 25V C0G 0201				
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8164 3PF +/-0.1PF 25V C0G 0201		C8165 3PF +/-0.1PF 25V C0G 0201				
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8166 12PF 5% 25V CERM 0201		C8167 3PF +/-0.1PF 25V C0G 0201				
28 PP3V3_TBT_X_S0	C8168 12PF 5% 25V CERM 0201		C8169 3PF +/-0.1PF 25V C0G 0201				
72 69 61 PPVCCPCH_S5G	C8170 3PF +/-0.1PF 25V C0G 0201		C8171 3PF +/-0.1PF 25V C0G 0201				
72 69 63 57 45 PPVCCGT_S0G	C8172 3PF +/-0.1PF 25V C0G 0201		C8173 3PF +/-0.1PF 25V C0G 0201				
72 69 61 PPVCCIO_S0G	C8175 3PF +/-0.1PF 25V C0G 0201						
69 30 28 PP3V3_UPC_XB_LDO	C8176 12PF 5% 25V CERM 0201		C8177 3PF +/-0.1PF 25V C0G 0201				
72 69 68 64 63 61 60 58 44 PP3V3_S5	C8178 12PF 5% 25V CERM 0201		C8179 3PF +/-0.1PF 25V C0G 0201				
69 PP3V3_S5_SSD_SNS	C8174 3.5PF +/-0.25PF 25V C0G 0201						
72 69 63 57 45 PPVCCGT_S0G	C8181 3PF +/-0.1PF 25V C0G 0201						
72 69 67 64 63 45 44 43 41 PP3V3_S4	C8182 3PF +/-0.1PF 25V C0G 0201		C8183 3PF +/-0.1PF 25V C0G 0201				
69 64 63 62 PP1V2_S3	C8185 3PF +/-0.1PF 25V C0G 0201						
72 69 68 60 58 53 50 43 PPBUS_G3H	C8187 3PF +/-0.1PF 25V C0G 0201						
27 PP0V9_TBT_X_SVR	C8188 12PF 5% 25V CERM 0201		C8189 3PF +/-0.1PF 25V C0G 0201				
72 69 68 64 63 61 60 58 44 PP3V3_S5	C8180 3PF +/-0.1PF 25V C0G 0201						
63 62 61 59 57 56 55 54 43 PPBUS_G3H_CPU	C8191 3PF +/-0.1PF 25V C0G 0201						
72 69 64 63 60 58 54 PP5V_S4	C8192 12PF 5% 25V CERM 0201		C8193 3PF +/-0.1PF 25V C0G 0201				
72 69 64 63 60 58 54 PP5V_S4	C8194 12PF 5% 25V CERM 0201		C8195 3PF +/-0.1PF 25V C0G 0201				
72 69 64 63 60 58 54 PP5V_S4	C8197 3PF +/-0.1PF 25V C0G 0201						
69 64 63 PP5V_S5	C8199 3PF +/-0.1PF 25V C0G 0201						
72 69 64 63 60 58 54 PP5V_S4	C8196 12PF 5% 25V CERM 0201		C8198 3PF +/-0.1PF 25V C0G 0201				
72 69 67 64 63 60 51 50 48 PP1V8_S0	C81A0 2.9PF +/-0.05PF 25V C0G-CERM 0201	CRITICAL	C81A1 2.9PF +/-0.05PF 25V C0G-CERM 0201	CRITICAL			
72 69 67 64 63 60 51 50 48 PP1V8_S0	C81A3 2.9PF +/-0.05PF 25V C0G-CERM 0201						
72 69 67 64 63 45 44 43 41 PP3V3_S4	C81A5 3.5PF +/-0.25PF 25V C0G 0201						
72 69 44 PP3V3_S4_WLS	C81A7 3PF +/-0.1PF 25V C0G 0201						
69 64 60 59 54 49 46 45 42 38 PP3V3_S0	C81A8 3PF +/-0.1PF 25V C0G 0201	NOSTUFF	C81A9 3PF +/-0.1PF 25V C0G 0201	NOSTUFF			

BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

PAGE TITLE
RAIL DESENSE CAPS

Apple Inc.

DRAWING NUMBER 051-02265 SIZE D
REVISION 1.0.0
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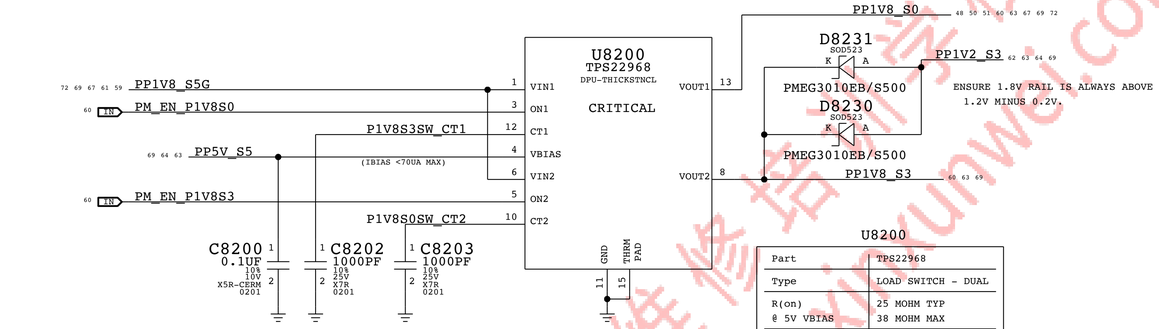
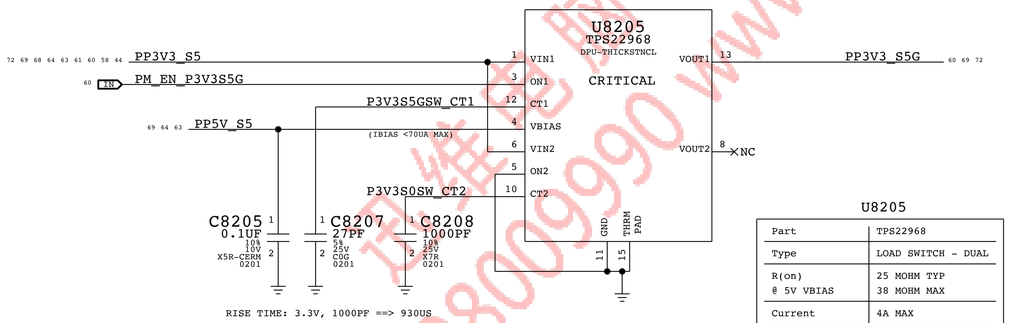
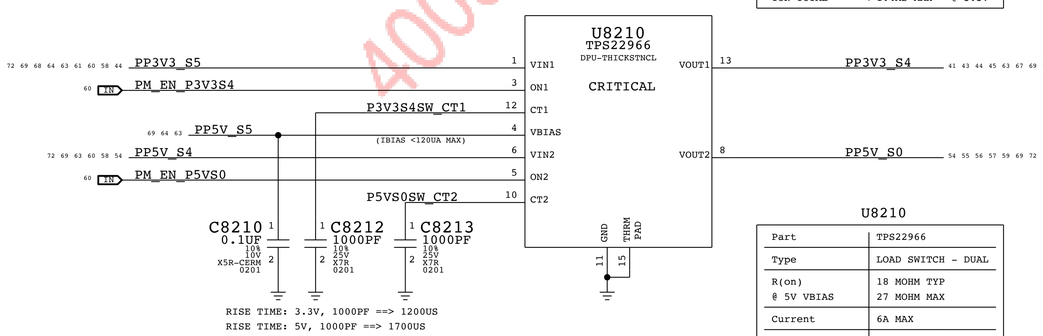


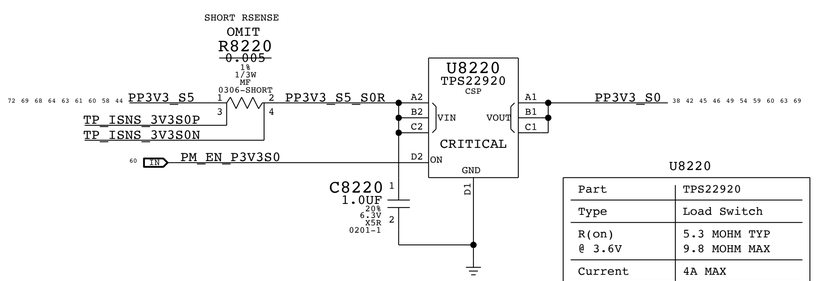
U8200	
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1MS MAX @ 1.8V



U8205	
Part	TPS22968
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	25 MOHM TYP 38 MOHM MAX
Current	4A MAX
TON-TOTAL	1.4MS MAX @ 3.3V

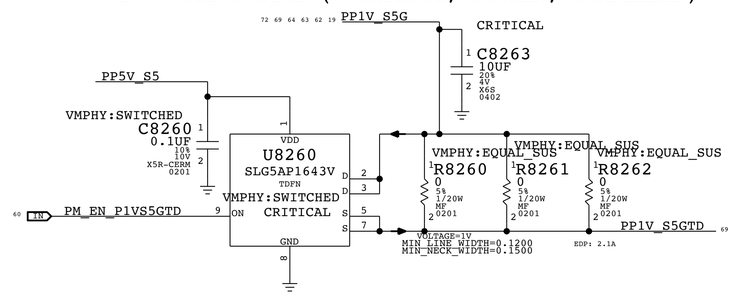


U8210	
Part	TPS22966
Type	LOAD SWITCH - DUAL
R(on) @ 5V VBIAS	18 MOHM TYP 27 MOHM MAX
Current	6A MAX
TON-TOTAL	1.7MS MAX @ 3,3V 2.4MS MAX @ 5V



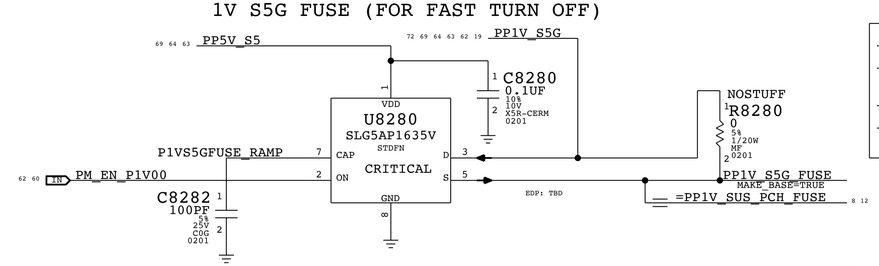
U8220	
Part	TPS22920
Type	Load Switch
R(on) @ 3.6V	5.3 MOHM TYP 9.8 MOHM MAX
Current	4A MAX
TON-TOTAL	1.3MS MAX @ 3.6V

1V S5GTD SWITCH (VCCMPHYGT,VCCSRAM,VCCAPLLEBB)



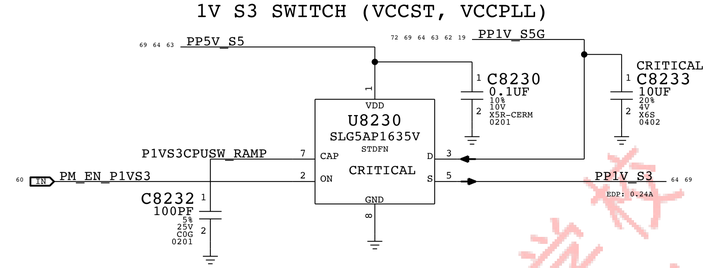
U8260	
Part	SLG5AP1643V
Type	Load Switch
R(on) @ 25C R(on) @ 70C	7.4 MOHM TYP 10.6 MOHM MAX
Current	6A MAX
TON-TOTAL	65US MAX @ 1V

1V S5G FUSE (FOR FAST TURN OFF)



U8230	
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

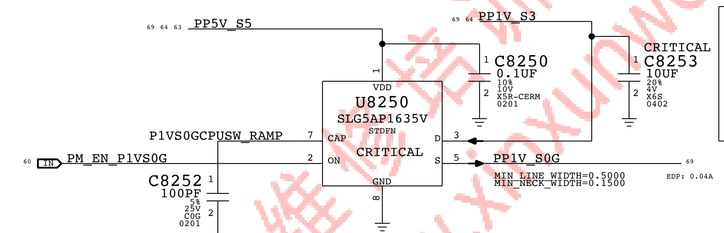
1V S3 SWITCH (VCCST, VCCPLL)



U8230	
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

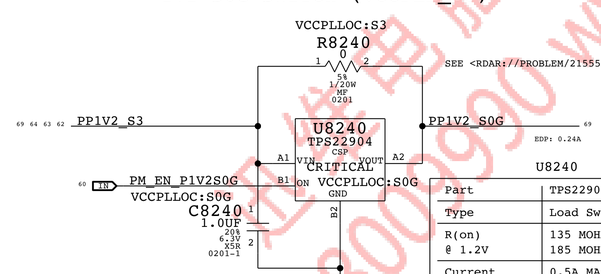
1V S0G CPU SWITCH (VCCSTG)

FAST TURN ON: < 64US



U8250	
Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 MOHM TYP 28 MOHM MAX
Current	2.5A MAX
TON-TOTAL	39US MAX @ 1V

1V2 S0G SWITCH (VCCPLL_OC)



U8240	
Part	TPS22904
Type	Load Switch
R(on) @ 1.2V	135 MOHM TYP 185 MOHM MAX
Current	0.5A MAX
TON-TOTAL	20US MAX @ 1.2V

BOM_COST_GROUP=PLATFORM POWER

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 12:54:34 2016

PAGE TITLE
Power FETs

Apple Inc.

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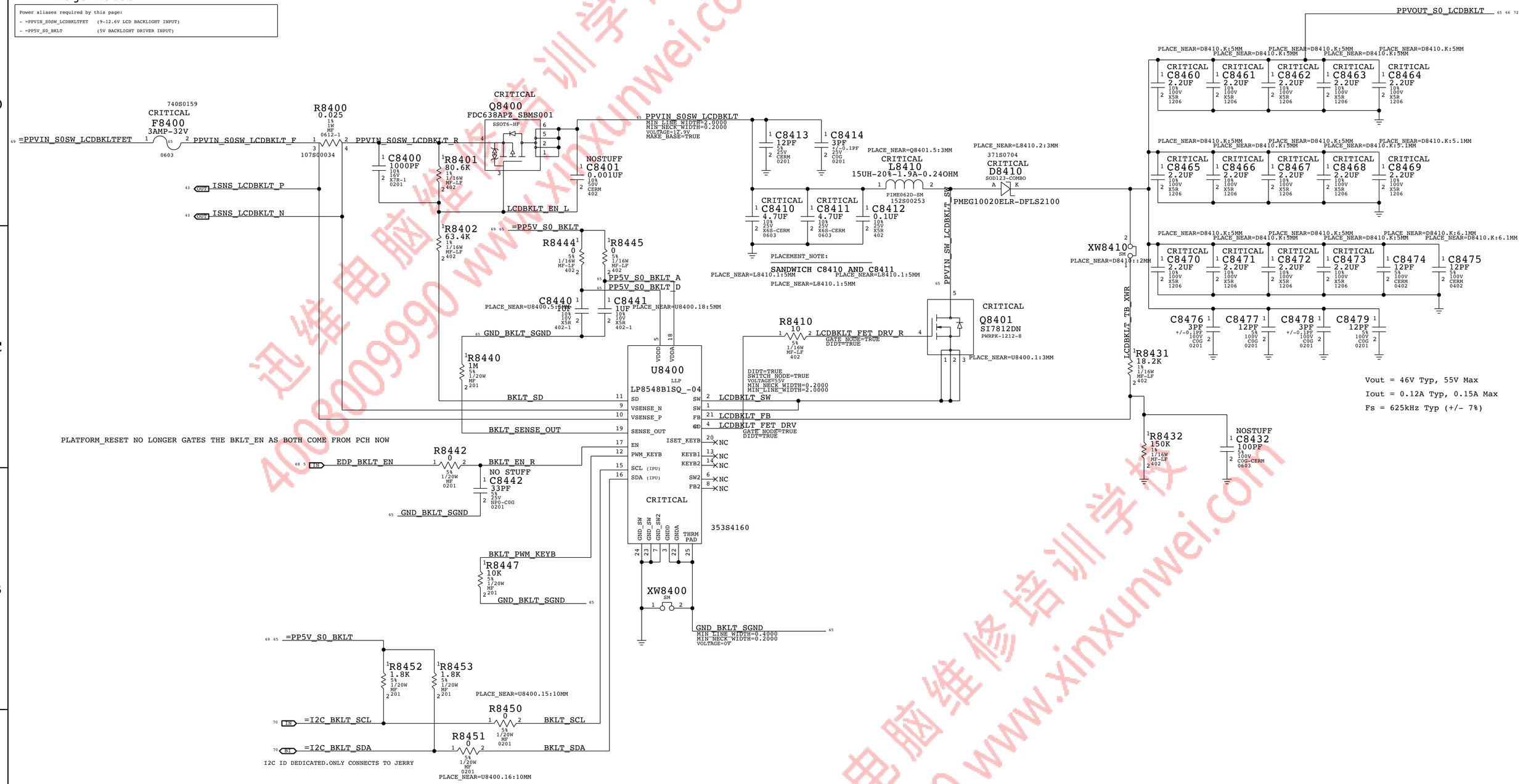
Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)



LINE WIDTHS

PP5V_S0_BKLT_A
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

PP5V_S0_BKLT_D
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V

PBUS LINE WIDTHS

PPVIN_S0SW_LCDBKLT_F
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT_R
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

PPVIN_S0SW_LCDBKLT
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V

LCD BKLT LINE WIDTHS

LCDBKLT_FET_DRV
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
GATE_NODE=TRUE DIDT=TRUE

PPVIN_SW_LCDBKLT_SW
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V
SWITCH_NODE=TRUE DIDT=TRUE

PPVOUT_S0_LCDBKLT
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.2000
VOLTAGE=55V

BOM_COST_GROUP=DISPLAY

PAGE TITLE	LCD Backlight Driver
	Apple Inc.
DRAWING NUMBER	051-02265
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REVISION	1.0.0
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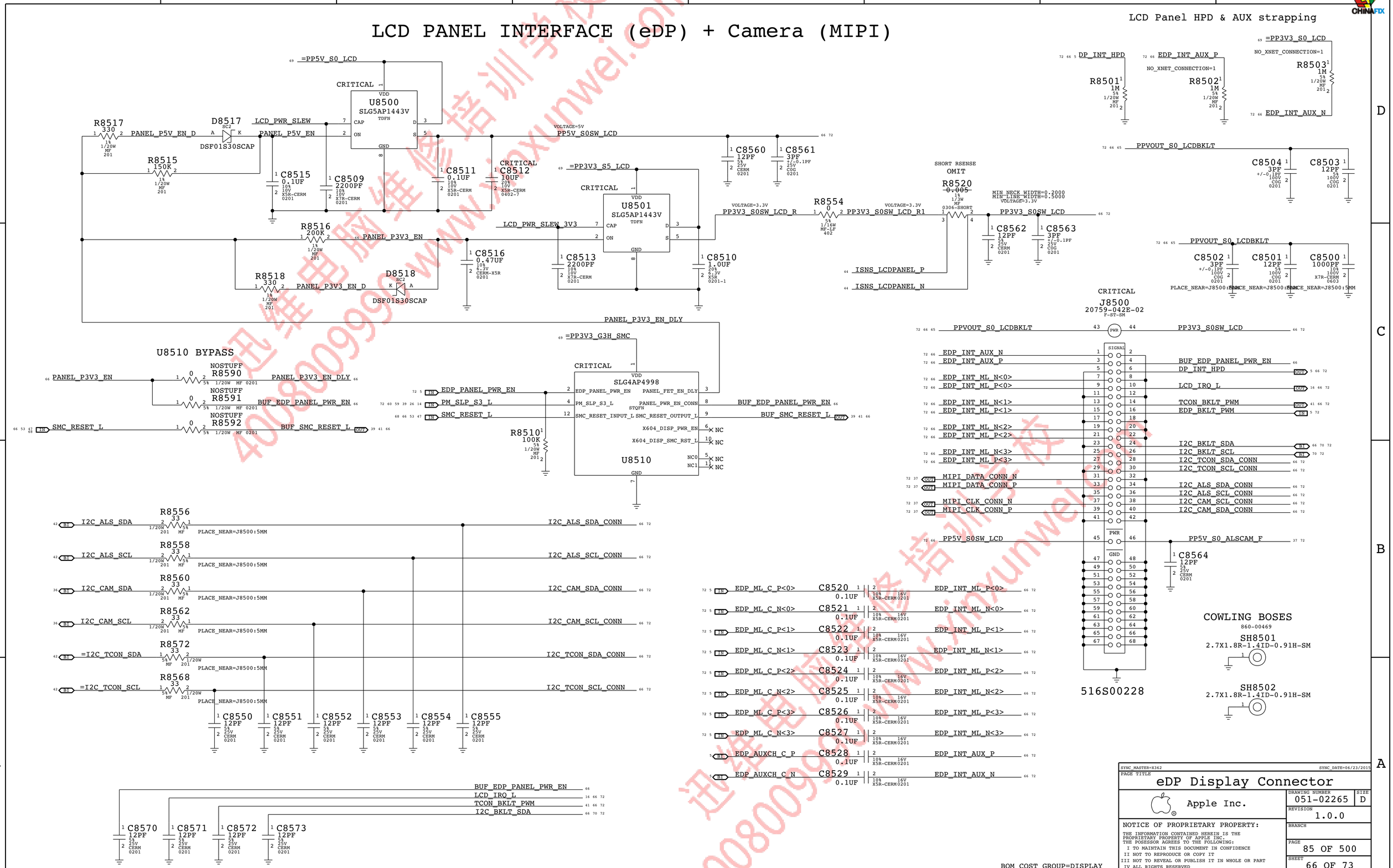
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



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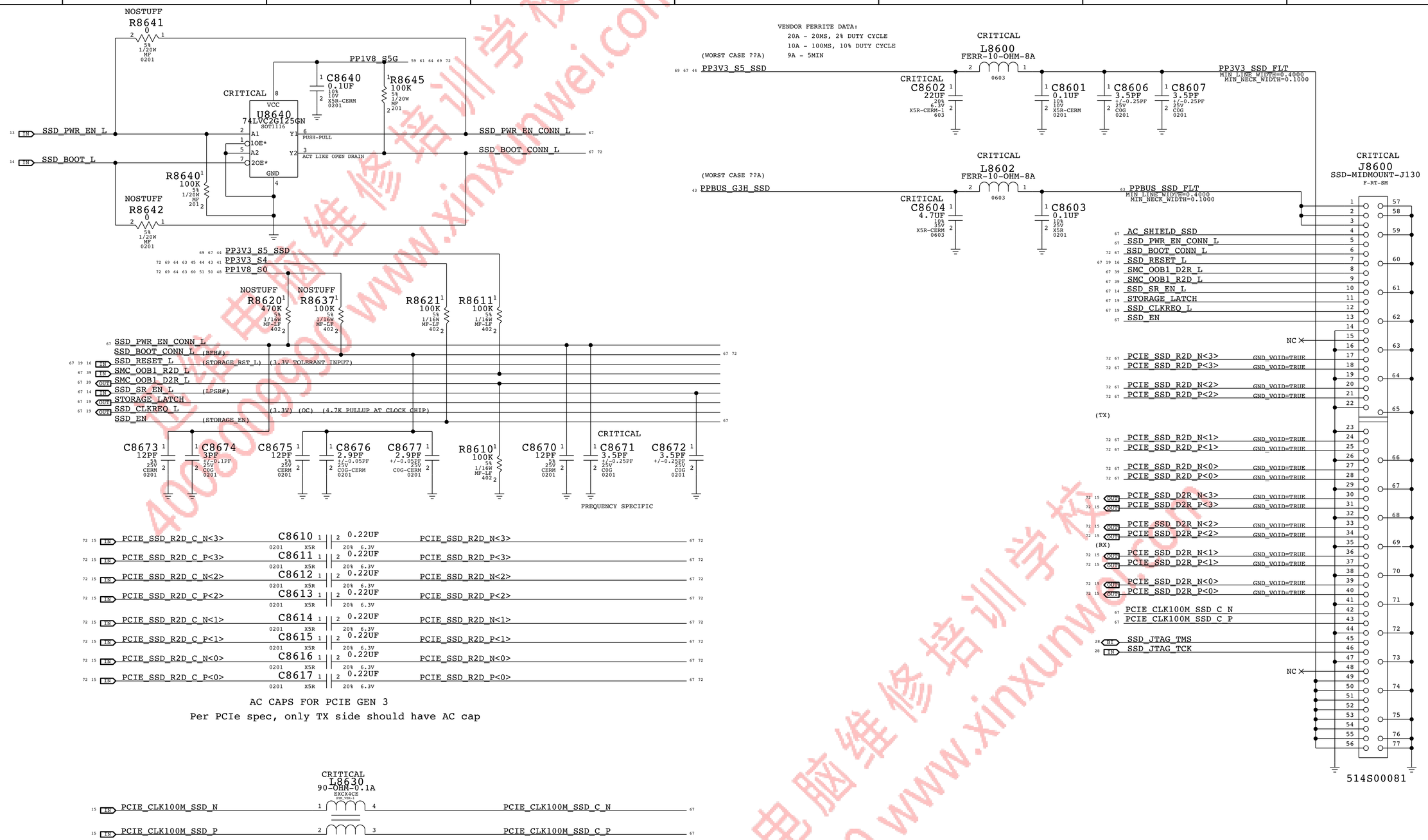
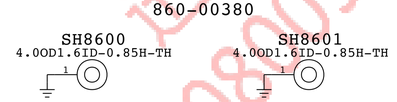


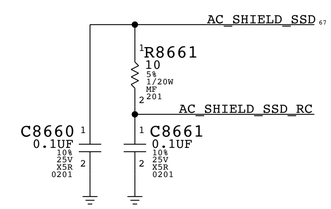
NOTES:

1. POWER-ON TO PERST_L DE-ASSERTION = 10MS MINIMUM
2. PP3V3_EN: PROVIDE 10MS EARLY WARNING TO SSD THAT POWER WILL BE OFF. (PIN 47, PP3V3_EN, IS NOT USED BY SAMSUNG UAX AND SANDISK SSD.)
3. PCIE CLK100M ARE 2.5V SIGNALS.
4. OOB SIGNALS: UART 3.3V, 115.2 KBAUD, 8B, NO PARITY, 1 STOP BIT.

SSD STANDOFFS

860-00380





BOM_COST_GROUP=SSD

DESIGN: X502/MLB CATZ	
LAST CHANGE: Thu Aug 4 21:00:42 2016	
PAGE TITLE: SSD MODULE	
Apple Inc.	DRAWING NUMBER 051-02265 / SIZE D
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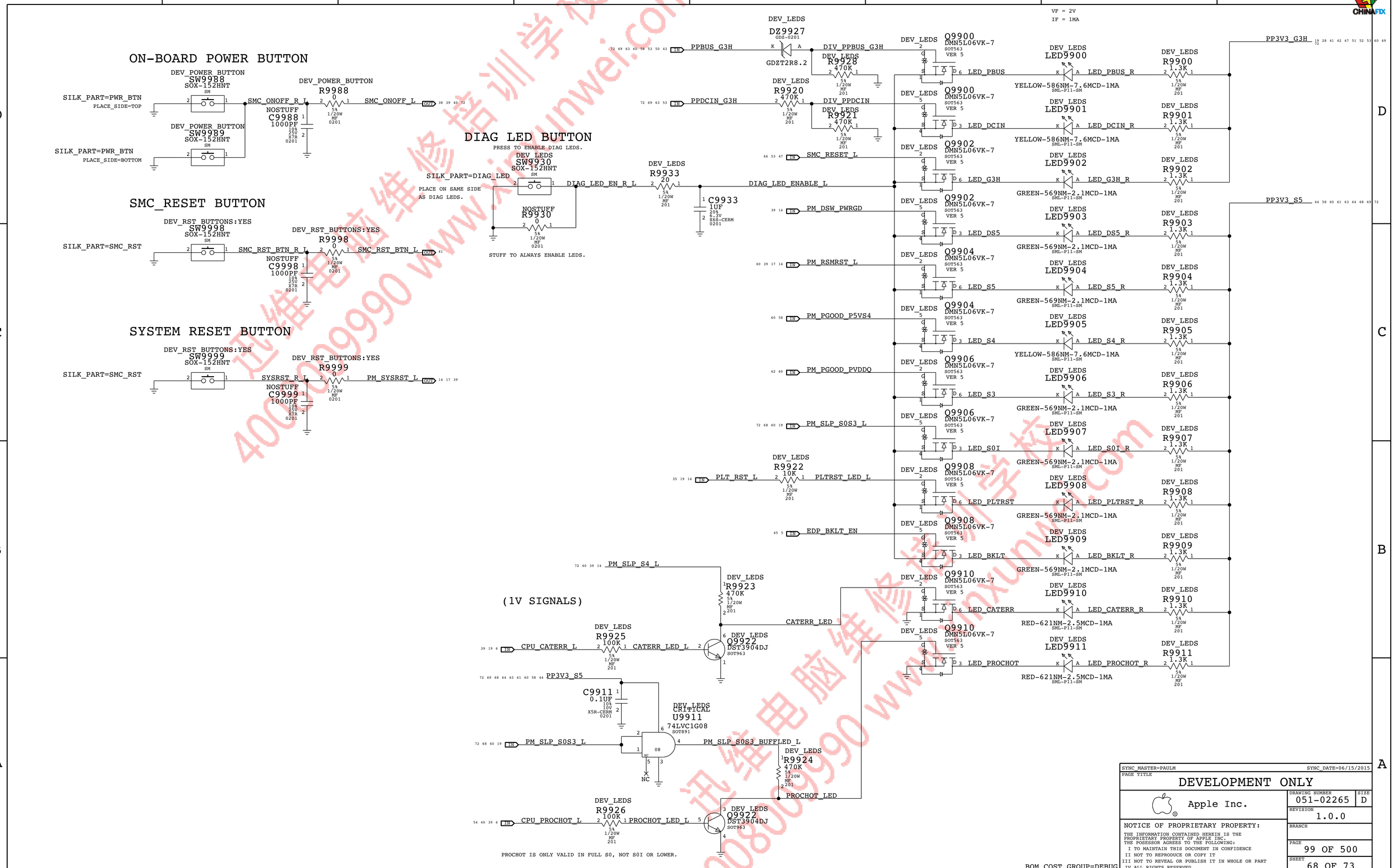
ON-BOARD POWER BUTTON
DEV_POWER_BUTTON SW9988 SOX-152HNT
SILK_PART=PWR_BTN PLACE_SIDE=TOP
DEV_POWER_BUTTON SW9989 SOX-152HNT
SILK_PART=PWR_BTN PLACE_SIDE=BOTTOM
SMC_ONOFF_R_L
DEV_POWER_BUTTON R9988 0
NOSTUFF C9988 1000PF
SMC_ONOFF_L
SMC_RESET BUTTON
DEV_RST_BUTTONS:YES SW9998 SOX-152HNT
SILK_PART=SMC_RST
SMC_RST_BTN_R_L
DEV_RST_BUTTONS:YES R9998 0
NOSTUFF C9998 1000PF
SMC_RST_BTN_L
SYSTEM RESET BUTTON
DEV_RST_BUTTONS:YES SW9999 SOX-152HNT
SILK_PART=SMC_RST
SYSRST_R_L
DEV_RST_BUTTONS:YES R9999 0
NOSTUFF C9999 1000PF
PM_SYSRST_L
DIAG LED BUTTON
PRESS TO ENABLE DIAG LEDS.
DEV_LEDS SW9930 SOX-152HNT
SILK_PART=DIAG_LED
PLACE ON SAME SIDE AS DIAG LEDS.
DIAG_LED_EN_R_L
NOSTUFF R9930 0
STUFF TO ALWAYS ENABLE LEDS.
DEV_LEDS R9933 20
C9933 1UF
DIAG_LED_ENABLE_L
PPBUS_G3H
DEV_LEDS DZ9927 GDZ-0201
GDZT2R8.2
DIV_PPBUS_G3H
DEV_LEDS R9928 470K
DEV_LEDS R9920 470K
PPDCIN_G3H
DIV_PPDCIN
DEV_LEDS R9921 470K
SMC_RESET_L
PM_DSW_PWRGD
PM_RSMRST_L
PM_PGOOD_P5VS4
PM_PGOOD_PVDDQ
PM_SLP_S0S3_L
DEV_LEDS R9922 10K
PLT_RST_L
PLTRST_LED_L
EDP_BKLT_EN
DEV_LEDS Q9900 DMN5L06VK-7 SOT563 VER 5
LED_PBUS
LED_DCIN
LED_G3H
LED_DS5
LED_S5
LED_S4
LED_S3
LED_S0I
LED_PLTRST
LED_BKLT
LED_CATERR
LED_PROCHOT
VF = 2V
IF = 1MA
DEV_LEDS LED9900 YELLOW-586NM-7.6MCD-1MA SML-P11-SM
LED_PBUS_R
DEV_LEDS LED9901 YELLOW-586NM-7.6MCD-1MA
LED_DCIN_R
DEV_LEDS LED9902 GREEN-569NM-2.1MCD-1MA
LED_G3H_R
DEV_LEDS LED9903 GREEN-569NM-2.1MCD-1MA
LED_DS5_R
DEV_LEDS LED9904 GREEN-569NM-2.1MCD-1MA
LED_S5_R
DEV_LEDS LED9905 YELLOW-586NM-7.6MCD-1MA
LED_S4_R
DEV_LEDS LED9906 GREEN-569NM-2.1MCD-1MA
LED_S3_R
DEV_LEDS LED9907 GREEN-569NM-2.1MCD-1MA
LED_S0I_R
DEV_LEDS LED9908 GREEN-569NM-2.1MCD-1MA
LED_PLTRST_R
DEV_LEDS LED9909 GREEN-569NM-2.1MCD-1MA
LED_BKLT_R
DEV_LEDS LED9910 RED-621NM-2.5MCD-1MA
LED_CATERR_R
DEV_LEDS LED9911 RED-621NM-2.5MCD-1MA
LED_PROCHOT_R
DEV_LEDS R9900 1.3K
DEV_LEDS R9901 1.3K
DEV_LEDS R9902 1.3K
DEV_LEDS R9903 1.3K
DEV_LEDS R9904 1.3K
DEV_LEDS R9905 1.3K
DEV_LEDS R9906 1.3K
DEV_LEDS R9907 1.3K
DEV_LEDS R9908 1.3K
DEV_LEDS R9909 1.3K
DEV_LEDS R9910 1.3K
DEV_LEDS R9911 1.3K
PP3V3_G3H
PP3V3_S5
(1V SIGNALS)
PM_SLP_S4_L
DEV_LEDS R9923 470K
CATERR_LED
DEV_LEDS R9925 100K
CPU_CATERR_L
CATERR_LED_L
DEV_LEDS Q9922 DST3904DJ SOT963
PP3V3_S5
C9911 0.1UF
DEV_LEDS CRITICAL U9911 74LVC1G08 SOT891
PM_SLP_S0S3_L
PM_SLP_S0S3_BUFFLED_L
DEV_LEDS R9924 470K
PROCHOT_LED
DEV_LEDS R9926 100K
CPU_PROCHOT_L
PROCHOT_LED_L
DEV_LEDS Q9922 DST3904DJ SOT963
PROCHOT IS ONLY VALID IN FULL S0, NOT S0I OR LOWER.
BOM_COST_GROUP=DEBUG
SYNC_MASTER=PAULM
SYNC_DATE=06/15/2015
PAGE TITLE
DEVELOPMENT ONLY
Apple Inc.
DRAWING NUMBER 051-02265
SIZE D
REVISION 1.0.0
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=PPBUS_G3H	MAKE_BASE=TRUE	PPBUS_G3H	43 50 53 58 60 63 68 69 72
=PPDCIN_G3H_SNS	MAKE_BASE=TRUE	PPDCIN_G3H	53 63 68 69 72
=PP5V_S5_LDO	MAKE_BASE=TRUE	PP5V_S5	63 64
=PP3V3_G3H_SMC	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
=PP3V3_S5_SMC	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
=PP3V3_S4_SMC	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP3V3_S0_SMC	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PPVIN_S5_SMCVREF	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
=PP1V8_S3_MEM	MAKE_BASE=TRUE	PP1V8_S3	60 63 64
=PP1V2_S3_MEM_VDD2	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PP1V2_S3_MEM_VDDCA	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PP1V2_S3_MEM_VDDQ	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PPDDR_S3_MEMVREF	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PP0V6_S0_MEM_VTT_A	MAKE_BASE=TRUE	PPVTT_S0	62 69 72
=PP0V6_S0_MEM_VTT_B	MAKE_BASE=TRUE	PPVTT_S0	62 69 72
PPVREF_S3_MEM_VREFDQ_A	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFDQ_A	21 22
PPVREF_S3_MEM_VREFCA	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFCA_A	21 22
PPVREF_S3_MEM_VREFDQ_B	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFDQ_B	23 24
PPVREF_S3_MEM_VREFCA	MAKE_BASE=TRUE	PP0V6_S3_MEM_VREFCA_B	23 24

CPU RAILS

=PPVCC_S0_CPU	MAKE_BASE=TRUE	PPVCCCPU_S0G	45 55 63 72
=PPVCCSA_S0_CPU	MAKE_BASE=TRUE	PPVCCSA_S0G	56 72
=PPVCCGT_S0_CPU	MAKE_BASE=TRUE	PPVCCGT_S0G	45 57 63 69 72
=PPVCCGTX_S0_CPU	MAKE_BASE=TRUE	PPVCCGT_S0G	45 57 63 69 72
=PP1V2_S3_CPU_VDDQ	MAKE_BASE=TRUE	PP1V2_S3	62 63 64 69
=PP1V2_S3_CPU_VDDOC	MAKE_BASE=TRUE	=PP1V2_S3_CPU_VDDQ	8 10 69
=PP0V95_S0_CPU_VCCIO	MAKE_BASE=TRUE	PPVCCIO_S0G	61 63 72
=PP1V_S3_CPU_VCCST	MAKE_BASE=TRUE	PP1V_S3	64 69
=PP1V_S0_SMC_VCCST	MAKE_BASE=TRUE		
=PP1V_S0SW_CPU_VCCSTG	MAKE_BASE=TRUE	PP1V_S0G	64
=PP1V_S3_CPU_VCCPLL	MAKE_BASE=TRUE	PP1V_S3	64 69
=PP1V2_S0SW_CPU_VCCPLLOC	MAKE_BASE=TRUE	PP1V2_S0G	64

PCH RAILS

=PP3V_G3H_PCH_VCCRTC	MAKE_BASE=TRUE	PP3V1_RTC	61
=PP3V3_S5_PCH_VCCDSW	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
=PP3V3_SUS_PCH_VCCPGPPA	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPB	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPC	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPD	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPE	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPGPPG	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCPRIM	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCSPI	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP3V3_SUS_PCH_VCCRTCPRIM	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP1V_SUS_PCH_VCCPRIM	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCMPHYAON	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK1	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK2_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK3	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK4_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK5_SRC	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCCLK6	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V_SUS_PCH_VCCAPLL	MAKE_BASE=TRUE	PP1V_S5G	19 62 63 64 69 72
=PP1V8_SUS_PCH_VCCPGPPF	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
=PP1V8_SUS_PCH_VCCATS	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
=PP1V8_SUS_PCH_VCC1P8_SRC	MAKE_BASE=TRUE	PP1V8_S5G	59 61 64 67 69 72
=PPVCCPRIMECORE_SUS_PCH	MAKE_BASE=TRUE	PPVCCPCH_S5G	61 63 72
=PP1V_SUSSW_PCH_VCCAMPHYPLL_SRC	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
=PP1V_SUSSW_PCH_VCCMPHYGT	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
=PP1V_SUSSW_PCH_VCCSRAM	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
=PP1V_SUSSW_PCH_VCCAPLLEBB	MAKE_BASE=TRUE	PP1V_S5GTD	64 69
=PP1V8_S0_PCH_VCCHDA	MAKE_BASE=TRUE	PP1V8_S0	48 50 51 60 63 64 67 72
=PP1V8R1V5_S0_PCH_VCCHDA			
=PP3V3_S0_PCH	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP3V3_S4_PCH	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP3V3R1V8_S0_PCH_VCCPGPPB	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69

SSD RAILS

PP3V3_S5_SSD	MAKE_BASE=TRUE	PP3V3_S5_SSD_SNS	63
=PP3V3_S0_TBT_X_SNS		=PP3V3_TBT_X_S0	27 28

CPU_VCCGTXSENSE_P	MAKE_BASE=TRUE	PU_VSNS_CPU_VCCGTX_TP	
CPU_VCCGTXSENSE_N	MAKE_BASE=TRUE	PD_VSNS_CPU_VCCGTX_TN	
=PP3V3_S0_CAMERA	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP5V_S0_ALSCAM	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
=PP3V3_S0_LCD	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP3V3_S5_LCD	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
=PP5V_S0_LCD	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
=PP3V3_S0_BT_UART	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP3V3_S4_BT_UART	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP3V3_G3H_KBD	MAKE_BASE=TRUE	PP3V3_G3H	19 28 41 42 47 51 52 53 60 68 69 72
=PP3V3_S4_KBD	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP5V_S0_KBD	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
=PP3V3_S4_WLAN	MAKE_BASE=TRUE	PP3V3_S4_WLS	44 63 72
=PP3V3_S5_WIRELESS	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
=PP3V3_S0_TPAD	MAKE_BASE=TRUE	PP3V3_S0	38 42 45 46 49 54 59 60 63 64 69
=PP3V3_S4_TPAD	MAKE_BASE=TRUE	PP3V3_S4	41 43 44 45 63 64 67 69 72
=PP5V_S4_TPAD	MAKE_BASE=TRUE	PP5V_S4	54 58 60 63 64 69 72
=PPBUS_S4_TPAD	MAKE_BASE=TRUE	PPBUS_G3H_TPAD	43
=PP1V_SUS_XDP		=PP1V_SUS_PCH_VCCPRIM	8 12 69
=PP3V3_SUS_XDP	MAKE_BASE=TRUE	PP3V3_S5G	60 64 69 72
=PP5V_S0_BKLT	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72
=PPVIN_S0SW_LCDBKLTFET	MAKE_BASE=TRUE	PPBUS_G3H	43 50 53 58 60 63 68 69 72
=PP5V_S0_FAN	MAKE_BASE=TRUE	PP5V_S0	54 55 56 57 59 64 69 72

Digital Ground

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.0850
MIN_LINE_WIDTH=0.3000

USB-C GLOBAL POWER ALIASES

=PP3V3_UPC_XA_AUX	MAKE_BASE=TRUE	PP3V3_UPC_XA_LDO	28 29
=PP3V3_UPC_XB_AUX	MAKE_BASE=TRUE	PP3V3_UPC_XB_LDO	28 30 63
=PP3V3_S5_TBT_X	MAKE_BASE=TRUE	PP3V3_S5	44 58 60 61 63 64 68 69 72
=PP5V_XA_USBC	MAKE_BASE=TRUE	PP5V_S4	54 58 60 63 64 69 72
=PP5V_XB_USBC			
=PP5V_USBC			
=PPHV_EXT_G3H	MAKE_BASE=TRUE	PPDCIN_G3H	53 63 68 69 72

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
LAST CHANGE: Mon Aug 8 19:33:56 2016

PAGE TITLE
Power Aliases

Apple Inc.

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UNUSED GPIOS, HSIO

8	IN	VCCPRIM_CORE_VID0	MAKE_BASE=TRUE	NO_TEST=1	NC_VCCPRIM_CORE_VID0
8	IN	VCCPRIM_CORE_VID1	MAKE_BASE=TRUE	NO_TEST=1	NC_VCCPRIM_CORE_VID1
16	IN	MLB_DEV_L	MAKE_BASE=TRUE	NO_TEST=1	NC_MLB_DEV_L
16	IN	I2C_UPC_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_UPC_SDA
16	IN	I2C_UPC_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_UPC_SCL
13	IN	PCH_BSSB_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_BSSB_CLK
13	IN	PCH_BSSB_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_BSSB_DATA
16	IN	TBT_X_DPMUX_SEL	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_X_DPMUX_SEL
16	IN	TBT_T_CIO_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_CIO_PWR_EN
16	IN	TBT_T_USB_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_USB_PWR_EN
16	IN	TBT_T_PCI_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_PCI_RESET_L
16	IN	TBT_T_DPMUX_SEL	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_DPMUX_SEL
15	OUT	=TBT_T_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TBT_T_CLKREQ_L
15	IN	PCIE_CLK100M_TBT_T_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_TBT_TN
15	IN	PCIE_CLK100M_TBT_T_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_TBT_TP
15	OUT	PCIE_TBT_T_D2R_N<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RN0
15	OUT	PCIE_TBT_T_D2R_P<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RP0
15	IN	PCIE_TBT_T_R2D_C_N<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CN0
15	IN	PCIE_TBT_T_R2D_C_P<0>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CP0
15	OUT	PCIE_TBT_T_D2R_N<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RN1
15	OUT	PCIE_TBT_T_D2R_P<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_D2RP1
15	IN	PCIE_TBT_T_R2D_C_N<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CN1
15	IN	PCIE_TBT_T_R2D_C_P<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_TBT_T_R2D_CP1
15	BI	USB_CAMERA_DFR_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_03N
15	BI	USB_CAMERA_DFR_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_03P
13	IN	DEBUGUART_SEL_SOC	MAKE_BASE=TRUE	NO_TEST=1	NC_DEBUGUART_SEL_SOC
15	BI	USB3_EXTB_D2R_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RN
15	BI	USB3_EXTB_D2R_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_D2RP
15	BI	USB3_EXTB_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCN
15	BI	USB3_EXTB_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_EXTB_R2DCP
26	BI	=DP_X_SRC_ML_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_ML_CP<3..0>
26	BI	=DP_X_SRC_ML_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_ML_CN<3..0>
26	BI	=DP_X_SRC_AUX_P	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_AUXCHP
26	BI	=DP_X_SRC_AUX_N	MAKE_BASE=TRUE	NO_TEST=1	NC_DP_X_SRC_AUXCHN
15	BI	USB_EXTA_N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_01N
15	BI	USB_EXTA_P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB2_01P

15	BI	NC_USB2_05N	NO_TEST=1
15	BI	NC_USB2_05P	NO_TEST=1
15	BI	NC_USB2_06N	NO_TEST=1
15	BI	NC_USB2_06P	NO_TEST=1
15	BI	NC_USB2_07N	NO_TEST=1
15	BI	NC_USB2_07P	NO_TEST=1
15	BI	NC_USB2_09N	NO_TEST=1
15	BI	NC_USB2_09P	NO_TEST=1
15	BI	NC_USB2_10N	NO_TEST=1
15	BI	NC_USB2_10P	NO_TEST=1

30	BI	NC_UPC_XB_I2C_ADDR	NO_TEST=1

GND
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.0850
VOLTAGE=0V

Digital Ground

65	BI	=I2C_BKLT_SCL	MAKE_BASE TRUE	I2C_BKLT_SCL	BI	66 72
65	BI	=I2C_BKLT_SDA	TRUE	I2C_BKLT_SDA	BI	66 72

16	IN	TP_BT_I2S_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_CLK
16	IN	TP_BT_I2S_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_D2R
16	IN	TP_BT_I2S_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_R2D
16	IN	TP_BT_I2S_SYNC	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_I2S_SYNC
26	IN	TP_CAM_GPIO3	MAKE_BASE=TRUE	NO_TEST=1	NC_CAM_GPIO3
6	IN	TP_CPU_AT5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AT5
6	IN	TP_CPU_AU5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AU5
6	IN	TP_CPU_AY4	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_AY4
6	IN	TP_CPU_BB3	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_BB3
6	IN	TP_CPU_BB5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_BB5
59	IN	TP_CPU_MSM_L	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_MSM_L
9	IN	TP_CPU_NCTFVSS_A5	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_A5
9	IN	TP_CPU_NCTFVSS_A70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_A70
9	IN	TP_CPU_NCTFVSS_AV1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_AV1
9	IN	TP_CPU_NCTFVSS_B71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_B71
9	IN	TP_CPU_NCTFVSS_BA1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BA1
9	IN	TP_CPU_NCTFVSS_BA71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BA71
9	IN	TP_CPU_NCTFVSS_BB70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_BB70
9	IN	TP_CPU_NCTFVSS_C1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_NCTFVSS_C1
13	IN	TP_PCH_CLKOUT_LPC1	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLKOUT_LPC1
14	IN	TP_PCH_GPD7	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPD7
14	IN	TP_PCH_GPP_D0	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D0
16	IN	TP_PCH_GPP_D1	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D1
16	IN	TP_PCH_GPP_D3	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D3
16	IN	TP_PCH_GPP_D4	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_D4
5	IN	TP_PCH_GPP_E15	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_E15
14	IN	TP_PCH_GPP_F8	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F8
14	IN	TP_PCH_GPP_F9	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F9
14	IN	TP_PCH_GPP_F10	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F10
14	IN	PCH_BT_ROM_BOOT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F11
13	IN	PCH_SOC_DFU_STATUS	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F18
13	IN	SOC_PANIC_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F19
13	IN	SOC_S2R_ACK_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F20
13	IN	SOC_SLEEP_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_GPP_F21
14	IN	TP_PCH_LANPHYPC	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_LANPHYPC
14	IN	TP_PCH_PME_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_PME_L
14	IN	TP_PCH_SLP_WLAN_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SLP_WLAN_L
13	IN	TP_PCH_STRP_ESPI	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_STRP_ESPI
13	IN	TP_PCH_STRP_TLSCONF	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_STRP_TLSCONF
60	IN	TP_PMIC_PGC	MAKE_BASE=TRUE	NO_TEST=1	NC_PMIC_PGC
13	IN	TP_SPI_CS1_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_CS1_L
13	IN	TP_SPI_CS2_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_CS2_L
19	IN	TP_SYSCLK_CLK24M_SSD	MAKE_BASE=TRUE	NO_TEST=1	NC_SYSCLK_CLK24M_SSD
15	IN	TP_USB3_03_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_D2RN
15	IN	TP_USB3_03_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_D2RP
15	IN	TP_USB3_03_R2DN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_R2DN
15	IN	TP_USB3_03_R2DP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_03_R2DP
15	IN	TP_USB3_04_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_D2RN
15	IN	TP_USB3_04_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_D2RP
15	IN	TP_USB3_04_R2DN	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_R2DN
15	IN	TP_USB3_04_R2DP	MAKE_BASE=TRUE	NO_TEST=1	NC_USB3_04_R2DP
14	IN	PCH_SOC_FORCE_DFU	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SOC_FORCE_DFU
13	OUT	PCH_SOC_WDOG	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_SOC_WDOG
14	OUT	UPC_I2C_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_I2C_INT_L
30	IN	TP_UPC_XB_SWD_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XB_SWD_DATA
29	IN	TP_UPC_XA_SWD_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XA_SWD_DATA
29	IN	TP_UPC_XA_SWD_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_UPC_XA_SWD_CLK
15	IN	TP_PCIE_CLK100M5P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M5P
15	IN	TP_PCIE_CLK100M5N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M5N
15	IN	TP_PCH_CLKREQ5_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLKREQ5_L
15	IN	TP_ITPXDP_CLK100MP	MAKE_BASE=TRUE	NO_TEST=1	NC_ITPXDP_CLK100MP
15	IN	TP_ITPXDP_CLK100MN	MAKE_BASE=TRUE	NO_TEST=1	NC_ITPXDP_CLK100MN
55	IN	TP_CPUVR_GH1	MAKE_BASE=TRUE	NO_TEST=1	NC_CPUVR_GH1
6	IN	TP_CPU_RSVD_BB69	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BB69
6	IN	TP_CPU_RSVD_BB68	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BB68
6	IN	TP_CPU_RSVD_BA70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BA70
6	IN	TP_CPU_RSVD_BA68	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_BA68
6	IN	TP_CPU_RSVD_AW71	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AW71
6	IN	TP_CPU_RSVD_AW70	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AW70
6	IN	TP_CPU_RSVD_AK12	MAKE_BASE=TRUE	NO_TEST=1	NC_CPU_RSVD_AK12
19	IN	TP_SPKR_ID0	MAKE_BASE=TRUE	NO_TEST=1	NC_SPKR_ID0
60	IN	TP_PGOOD_PVCCIO	MAKE_BASE=TRUE	NO_TEST=1	NC_PGOOD_PVCCIO
60	IN	TP_PGOOD_P1V00	MAKE_BASE=TRUE	NO_TEST=1	NC_PGOOD_P1V00
19	IN	TP_PCH_CLK32K_RTCX2	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLK32K_RTCX2
19	IN	TP_PCH_CLK24M_XTALOUT	MAKE_BASE=TRUE	NO_TEST=1	NC_PCH_CLK24M_XTALOUT
19	IN	TP_XDP_BPM_L<3>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<3>
19	IN	TP_XDP_BPM_L<2>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<2>
19	IN	TP_XDP_BPM_L<1>	MAKE_BASE=TRUE	NO_TEST=1	NC_XDP_BPM_L<1>

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
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NC_ AND NO_TEST SIGNALS

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Memory Bit/Byte Swizzle

CPU	MAKE_BASE	DRAM
MEM_A_DQ<0>	TRUE	=MEM_A_DQ<16>
MEM_A_DQ<1>	TRUE	=MEM_A_DQ<17>
MEM_A_DQ<2>	TRUE	=MEM_A_DQ<23>
MEM_A_DQ<3>	TRUE	=MEM_A_DQ<19>
MEM_A_DQ<4>	TRUE	=MEM_A_DQ<20>
MEM_A_DQ<5>	TRUE	=MEM_A_DQ<21>
MEM_A_DQ<6>	TRUE	=MEM_A_DQ<22>
MEM_A_DQ<7>	TRUE	=MEM_A_DQ<18>
MEM_A_DQ<8>	TRUE	=MEM_A_DQ<2>
MEM_A_DQ<9>	TRUE	=MEM_A_DQ<7>
MEM_A_DQ<10>	TRUE	=MEM_A_DQ<6>
MEM_A_DQ<11>	TRUE	=MEM_A_DQ<4>
MEM_A_DQ<12>	TRUE	=MEM_A_DQ<0>
MEM_A_DQ<13>	TRUE	=MEM_A_DQ<3>
MEM_A_DQ<14>	TRUE	=MEM_A_DQ<1>
MEM_A_DQ<15>	TRUE	=MEM_A_DQ<5>
MEM_A_DQ<16>	TRUE	=MEM_A_DQ<46>
MEM_A_DQ<17>	TRUE	=MEM_A_DQ<47>
MEM_A_DQ<18>	TRUE	=MEM_A_DQ<42>
MEM_A_DQ<19>	TRUE	=MEM_A_DQ<43>
MEM_A_DQ<20>	TRUE	=MEM_A_DQ<44>
MEM_A_DQ<21>	TRUE	=MEM_A_DQ<45>
MEM_A_DQ<22>	TRUE	=MEM_A_DQ<40>
MEM_A_DQ<23>	TRUE	=MEM_A_DQ<41>
MEM_A_DQ<24>	TRUE	=MEM_A_DQ<63>
MEM_A_DQ<25>	TRUE	=MEM_A_DQ<59>
MEM_A_DQ<26>	TRUE	=MEM_A_DQ<61>
MEM_A_DQ<27>	TRUE	=MEM_A_DQ<56>
MEM_A_DQ<28>	TRUE	=MEM_A_DQ<62>
MEM_A_DQ<29>	TRUE	=MEM_A_DQ<58>
MEM_A_DQ<30>	TRUE	=MEM_A_DQ<60>
MEM_A_DQ<31>	TRUE	=MEM_A_DQ<57>
MEM_A_DQ<32>	TRUE	=MEM_A_DQ<8>
MEM_A_DQ<33>	TRUE	=MEM_A_DQ<11>
MEM_A_DQ<34>	TRUE	=MEM_A_DQ<10>
MEM_A_DQ<35>	TRUE	=MEM_A_DQ<13>
MEM_A_DQ<36>	TRUE	=MEM_A_DQ<12>
MEM_A_DQ<37>	TRUE	=MEM_A_DQ<9>
MEM_A_DQ<38>	TRUE	=MEM_A_DQ<14>
MEM_A_DQ<39>	TRUE	=MEM_A_DQ<15>
MEM_A_DQ<40>	TRUE	=MEM_A_DQ<24>
MEM_A_DQ<41>	TRUE	=MEM_A_DQ<25>
MEM_A_DQ<42>	TRUE	=MEM_A_DQ<27>
MEM_A_DQ<43>	TRUE	=MEM_A_DQ<30>
MEM_A_DQ<44>	TRUE	=MEM_A_DQ<28>
MEM_A_DQ<45>	TRUE	=MEM_A_DQ<29>
MEM_A_DQ<46>	TRUE	=MEM_A_DQ<31>
MEM_A_DQ<47>	TRUE	=MEM_A_DQ<26>
MEM_A_DQ<48>	TRUE	=MEM_A_DQ<39>
MEM_A_DQ<49>	TRUE	=MEM_A_DQ<33>
MEM_A_DQ<50>	TRUE	=MEM_A_DQ<34>
MEM_A_DQ<51>	TRUE	=MEM_A_DQ<35>
MEM_A_DQ<52>	TRUE	=MEM_A_DQ<36>
MEM_A_DQ<53>	TRUE	=MEM_A_DQ<37>
MEM_A_DQ<54>	TRUE	=MEM_A_DQ<38>
MEM_A_DQ<55>	TRUE	=MEM_A_DQ<32>
MEM_A_DQ<56>	TRUE	=MEM_A_DQ<55>
MEM_A_DQ<57>	TRUE	=MEM_A_DQ<51>
MEM_A_DQ<58>	TRUE	=MEM_A_DQ<49>
MEM_A_DQ<59>	TRUE	=MEM_A_DQ<52>
MEM_A_DQ<60>	TRUE	=MEM_A_DQ<48>
MEM_A_DQ<61>	TRUE	=MEM_A_DQ<53>
MEM_A_DQ<62>	TRUE	=MEM_A_DQ<54>
MEM_A_DQ<63>	TRUE	=MEM_A_DQ<50>
MEM_A_DQS_P<0>	TRUE	=MEM_A_DQS_P<2>
MEM_A_DQS_N<0>	TRUE	=MEM_A_DQS_N<2>
MEM_A_DQS_P<1>	TRUE	=MEM_A_DQS_P<0>
MEM_A_DQS_N<1>	TRUE	=MEM_A_DQS_N<0>
MEM_A_DQS_P<2>	TRUE	=MEM_A_DQS_P<5>
MEM_A_DQS_N<2>	TRUE	=MEM_A_DQS_N<5>
MEM_A_DQS_P<3>	TRUE	=MEM_A_DQS_P<7>
MEM_A_DQS_N<3>	TRUE	=MEM_A_DQS_N<7>
MEM_A_DQS_P<4>	TRUE	=MEM_A_DQS_P<1>
MEM_A_DQS_N<4>	TRUE	=MEM_A_DQS_N<1>
MEM_A_DQS_P<5>	TRUE	=MEM_A_DQS_P<3>
MEM_A_DQS_N<5>	TRUE	=MEM_A_DQS_N<3>
MEM_A_DQS_P<6>	TRUE	=MEM_A_DQS_P<4>
MEM_A_DQS_N<6>	TRUE	=MEM_A_DQS_N<4>
MEM_A_DQS_P<7>	TRUE	=MEM_A_DQS_P<6>
MEM_A_DQS_N<7>	TRUE	=MEM_A_DQS_N<6>

CPU	MAKE_BASE	DRAM
MEM_B_DQ<0>	TRUE	=MEM_B_DQ<6>
MEM_B_DQ<1>	TRUE	=MEM_B_DQ<7>
MEM_B_DQ<2>	TRUE	=MEM_B_DQ<1>
MEM_B_DQ<3>	TRUE	=MEM_B_DQ<3>
MEM_B_DQ<4>	TRUE	=MEM_B_DQ<4>
MEM_B_DQ<5>	TRUE	=MEM_B_DQ<5>
MEM_B_DQ<6>	TRUE	=MEM_B_DQ<2>
MEM_B_DQ<7>	TRUE	=MEM_B_DQ<0>
MEM_B_DQ<8>	TRUE	=MEM_B_DQ<16>
MEM_B_DQ<9>	TRUE	=MEM_B_DQ<20>
MEM_B_DQ<10>	TRUE	=MEM_B_DQ<19>
MEM_B_DQ<11>	TRUE	=MEM_B_DQ<23>
MEM_B_DQ<12>	TRUE	=MEM_B_DQ<21>
MEM_B_DQ<13>	TRUE	=MEM_B_DQ<17>
MEM_B_DQ<14>	TRUE	=MEM_B_DQ<22>
MEM_B_DQ<15>	TRUE	=MEM_B_DQ<18>
MEM_B_DQ<16>	TRUE	=MEM_B_DQ<40>
MEM_B_DQ<17>	TRUE	=MEM_B_DQ<41>
MEM_B_DQ<18>	TRUE	=MEM_B_DQ<45>
MEM_B_DQ<19>	TRUE	=MEM_B_DQ<46>
MEM_B_DQ<20>	TRUE	=MEM_B_DQ<42>
MEM_B_DQ<21>	TRUE	=MEM_B_DQ<43>
MEM_B_DQ<22>	TRUE	=MEM_B_DQ<44>
MEM_B_DQ<23>	TRUE	=MEM_B_DQ<47>
MEM_B_DQ<24>	TRUE	=MEM_B_DQ<63>
MEM_B_DQ<25>	TRUE	=MEM_B_DQ<59>
MEM_B_DQ<26>	TRUE	=MEM_B_DQ<57>
MEM_B_DQ<27>	TRUE	=MEM_B_DQ<61>
MEM_B_DQ<28>	TRUE	=MEM_B_DQ<58>
MEM_B_DQ<29>	TRUE	=MEM_B_DQ<62>
MEM_B_DQ<30>	TRUE	=MEM_B_DQ<60>
MEM_B_DQ<31>	TRUE	=MEM_B_DQ<56>
MEM_B_DQ<32>	TRUE	=MEM_B_DQ<10>
MEM_B_DQ<33>	TRUE	=MEM_B_DQ<9>
MEM_B_DQ<34>	TRUE	=MEM_B_DQ<12>
MEM_B_DQ<35>	TRUE	=MEM_B_DQ<13>
MEM_B_DQ<36>	TRUE	=MEM_B_DQ<11>
MEM_B_DQ<37>	TRUE	=MEM_B_DQ<15>
MEM_B_DQ<38>	TRUE	=MEM_B_DQ<14>
MEM_B_DQ<39>	TRUE	=MEM_B_DQ<8>
MEM_B_DQ<40>	TRUE	=MEM_B_DQ<24>
MEM_B_DQ<41>	TRUE	=MEM_B_DQ<31>
MEM_B_DQ<42>	TRUE	=MEM_B_DQ<26>
MEM_B_DQ<43>	TRUE	=MEM_B_DQ<27>
MEM_B_DQ<44>	TRUE	=MEM_B_DQ<25>
MEM_B_DQ<45>	TRUE	=MEM_B_DQ<28>
MEM_B_DQ<46>	TRUE	=MEM_B_DQ<30>
MEM_B_DQ<47>	TRUE	=MEM_B_DQ<29>
MEM_B_DQ<48>	TRUE	=MEM_B_DQ<32>
MEM_B_DQ<49>	TRUE	=MEM_B_DQ<33>
MEM_B_DQ<50>	TRUE	=MEM_B_DQ<34>
MEM_B_DQ<51>	TRUE	=MEM_B_DQ<38>
MEM_B_DQ<52>	TRUE	=MEM_B_DQ<36>
MEM_B_DQ<53>	TRUE	=MEM_B_DQ<37>
MEM_B_DQ<54>	TRUE	=MEM_B_DQ<35>
MEM_B_DQ<55>	TRUE	=MEM_B_DQ<39>
MEM_B_DQ<56>	TRUE	=MEM_B_DQ<55>
MEM_B_DQ<57>	TRUE	=MEM_B_DQ<54>
MEM_B_DQ<58>	TRUE	=MEM_B_DQ<50>
MEM_B_DQ<59>	TRUE	=MEM_B_DQ<51>
MEM_B_DQ<60>	TRUE	=MEM_B_DQ<52>
MEM_B_DQ<61>	TRUE	=MEM_B_DQ<53>
MEM_B_DQ<62>	TRUE	=MEM_B_DQ<49>
MEM_B_DQ<63>	TRUE	=MEM_B_DQ<48>
MEM_B_DQS_P<0>	TRUE	=MEM_B_DQS_P<0>
MEM_B_DQS_N<0>	TRUE	=MEM_B_DQS_N<0>
MEM_B_DQS_P<1>	TRUE	=MEM_B_DQS_P<2>
MEM_B_DQS_N<1>	TRUE	=MEM_B_DQS_N<2>
MEM_B_DQS_P<2>	TRUE	=MEM_B_DQS_P<5>
MEM_B_DQS_N<2>	TRUE	=MEM_B_DQS_N<5>
MEM_B_DQS_P<3>	TRUE	=MEM_B_DQS_P<7>
MEM_B_DQS_N<3>	TRUE	=MEM_B_DQS_N<7>
MEM_B_DQS_P<4>	TRUE	=MEM_B_DQS_P<1>
MEM_B_DQS_N<4>	TRUE	=MEM_B_DQS_N<1>
MEM_B_DQS_P<5>	TRUE	=MEM_B_DQS_P<3>
MEM_B_DQS_N<5>	TRUE	=MEM_B_DQS_N<3>
MEM_B_DQS_P<6>	TRUE	=MEM_B_DQS_P<4>
MEM_B_DQS_N<6>	TRUE	=MEM_B_DQS_N<4>
MEM_B_DQS_P<7>	TRUE	=MEM_B_DQS_P<6>
MEM_B_DQS_N<7>	TRUE	=MEM_B_DQS_N<6>

BOM_COST_GROUP=NO COST ITEMS

DESIGN: X502/MLB CATZ
LAST CHANGE: Thu Aug 4 21:00:42 2016

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XDP

CPU_CFG<3>	FUNC_TEST=TRUE	
ITP_PMODE	FUNC_TEST=TRUE	
XDP_CPU_PRDY_L	FUNC_TEST=TRUE	
XDP_CPU_PREQ_L	FUNC_TEST=TRUE	
XDP_CPU_PWRBTN_L	FUNC_TEST=TRUE	
XDP_CPU_TCK	FUNC_TEST=TRUE	
XDP_CPU_TDI	FUNC_TEST=TRUE	
XDP_CPU_TDO	FUNC_TEST=TRUE	
XDP_CPU_TMS	FUNC_TEST=TRUE	
XDP_CPU_TRST_L	FUNC_TEST=TRUE	
XDP_DBRESET_L	FUNC_TEST=TRUE	
XDP_PCH_TCK	FUNC_TEST=TRUE	
XDP_PCH_TDI	FUNC_TEST=TRUE	
XDP_PCH_TDO	FUNC_TEST=TRUE	
XDP_PCH_TMS	FUNC_TEST=TRUE	
XDP_PCH_TRST_L	FUNC_TEST=TRUE	
XDP_PM_RSMRST_L	FUNC_TEST=TRUE	
XDP_PRESENT_CPU	FUNC_TEST=TRUE	
XDP_PRESENT_L	FUNC_TEST=TRUE	
PP1V_S5G	FUNC_TEST=TRUE	
GND	FUNC_TEST=TRUE	

AUDIO FLEX

AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
AUD_CONN_RING2	FUNC_TEST=TRUE
AUD_CONN_RING2_XW	FUNC_TEST=TRUE
AUD_CONN_SLEEVE	FUNC_TEST=TRUE
AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
DMIC1_CLK	FUNC_TEST=TRUE
DMIC1_DATA	FUNC_TEST=TRUE
HALL_SENSOR_RIGHT	FUNC_TEST=TRUE
PP1V8_S0	FUNC_TEST=TRUE
PP3V3_G3H	FUNC_TEST=TRUE
GND	FUNC_TEST=TRUE

LEFT SPEAKERS

8409_SPKR_ID0	FUNC_TEST=TRUE
SPKRCONN_FL_OUT_N	FUNC_TEST=TRUE
SPKRCONN_FL_OUT_P	FUNC_TEST=TRUE
SPKRCONN_RL_OUT_N	FUNC_TEST=TRUE
SPKRCONN_RL_OUT_P	FUNC_TEST=TRUE
GND	FUNC_TEST=TRUE

RIGHT SPEAKERS

8409_SPKR_ID1	FUNC_TEST=TRUE
SPKRCONN_FR_OUT_N	FUNC_TEST=TRUE
SPKRCONN_FR_OUT_P	FUNC_TEST=TRUE
SPKRCONN_RR_OUT_N	FUNC_TEST=TRUE
SPKRCONN_RR_OUT_P	FUNC_TEST=TRUE
GND	FUNC_TEST=TRUE

BATTERY

SYS_DETECT_L	FUNC_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	FUNC_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	FUNC_TEST=TRUE

SMC

SMC_TCK	FUNC_TEST=TRUE
SMC_TDI	FUNC_TEST=TRUE
SMC_TDO	FUNC_TEST=TRUE
SMC_TMS	FUNC_TEST=TRUE
SMC_DEV_SUPPLY_L	FUNC_TEST=TRUE

BOOTROM

SPIROM_USE_MLB	FUNC_TEST=TRUE
SPI_MLBROM_CS_L	FUNC_TEST=TRUE
SPI_MLB_CLK	FUNC_TEST=TRUE
SPI_MLB_CS_L	FUNC_TEST=TRUE
SPI_MLB_IO<2>	FUNC_TEST=TRUE
SPI_MLB_IO<3>	FUNC_TEST=TRUE
SPI_MLB_MISO	FUNC_TEST=TRUE
SPI_MLB_MOSI	FUNC_TEST=TRUE

USB2 FIXTURE PORT

TP_USB_TESTERN	FUNC_TEST=TRUE
TP_USB_TESTERP	FUNC_TEST=TRUE
PP5V_S4	FUNC_TEST=TRUE
GND	FUNC_TEST=TRUE

MAKE_BASE=TRUE, FUNC_TEST=TRUE — USB_TESTER_N — TPA410 (TP-P6)

MAKE_BASE=TRUE, FUNC_TEST=TRUE — USB_TESTER_P — TPA411 (TP-P6)

DA410 ESD112-B1-02ELS 0201-THICKSTNCL — CRITICAL

DA411 ESD112-B1-02ELS 0201-THICKSTNCL — CRITICAL

CAP POWER DISCHARGE

PPBUS_G3H	FUNC_TEST=TRUE
PPDCIN_G3H	FUNC_TEST=TRUE
PPDCIN_G3H_CHGR	FUNC_TEST=TRUE
PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE

SYSTEM STATE

PM_SLP_S0S3_L	FUNC_TEST=TRUE
PM_SLP_S0_L	FUNC_TEST=TRUE
PM_SLP_S3_L	FUNC_TEST=TRUE
PM_SLP_S4_L	FUNC_TEST=TRUE
PM_SLP_S5_L	FUNC_TEST=TRUE
PM_SLP_SUS_L	FUNC_TEST=TRUE
PM_PWRBTN_L	FUNC_TEST=TRUE
ALL_SYS_PWRGD	FUNC_TEST=TRUE

MOJO PORT

SMC_DEBUGPRT_TX_L	FUNC_TEST=TRUE
SMC_DEBUGPRT_RX_L	FUNC_TEST=TRUE

MISC

SSD_BOOT_CONN_L	FUNC_TEST=TRUE
TP_PCH_SLP_A_L	FUNC_TEST=TRUE

CAMERA

CAM_TEST_MODE	FUNC_TEST=TRUE
TP_CAM_LV_JTAG_TCK	FUNC_TEST=TRUE
TP_CAM_LV_JTAG_TDI	FUNC_TEST=TRUE
TP_CAM_LV_JTAG_TDO	FUNC_TEST=TRUE
TP_CAM_LV_JTAG_TMS	FUNC_TEST=TRUE
TP_CAM_LV_JTAG_TRSTN	FUNC_TEST=TRUE
TP_CAM_TEST_MODE0	FUNC_TEST=TRUE
TP_CAM_TEST_MODE1	FUNC_TEST=TRUE
TP_CAM_TEST_MODE2	FUNC_TEST=TRUE

DISPLAY

DP_INT_HPD	FUNC_TEST=TRUE
EDP_BKLT_PWM	FUNC_TEST=TRUE
EDP_INT_AUX_N	FUNC_TEST=TRUE
EDP_INT_AUX_P	FUNC_TEST=TRUE
EDP_PANEL_PWR_EN	FUNC_TEST=TRUE
I2C_ALS_SCL_CONN	FUNC_TEST=TRUE
I2C_ALS_SDA_CONN	FUNC_TEST=TRUE
I2C_BKLT_SCL	FUNC_TEST=TRUE
I2C_BKLT_SDA	FUNC_TEST=TRUE
I2C_CAM_SCL_CONN	FUNC_TEST=TRUE
I2C_CAM_SDA_CONN	FUNC_TEST=TRUE
I2C_TCON_SCL_CONN	FUNC_TEST=TRUE
I2C_TCON_SDA_CONN	FUNC_TEST=TRUE
LCD_IRQ_L	FUNC_TEST=TRUE
MIPI_CLK_CONN_N	FUNC_TEST=TRUE
MIPI_CLK_CONN_P	FUNC_TEST=TRUE
MIPI_DATA_CONN_N	FUNC_TEST=TRUE
MIPI_DATA_CONN_P	FUNC_TEST=TRUE
TCON_BKLT_PWM	FUNC_TEST=TRUE
PP3V3_S0SW_LCD	FUNC_TEST=TRUE
PP5V_S0SW_LCD	FUNC_TEST=TRUE
PP5V_S0_ALSCAM_F	FUNC_TEST=TRUE
PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE
GND	FUNC_TEST=TRUE

USBC/TBT

JTAG_TBT_TCK	FUNC_TEST=TRUE
JTAG_TBT_TDI	FUNC_TEST=TRUE
JTAG_TBT_X_TMS	FUNC_TEST=TRUE
TBT_X_TEST_EN	FUNC_TEST=TRUE
PP20V_USBC_XA_VBUS	FUNC_TEST=TRUE
PP20V_USBC_XB_VBUS	FUNC_TEST=TRUE

POWER

PP1V8_S5G	FUNC_TEST=TRUE
PP1V_OPC_S0	FUNC_TEST=TRUE
PP3V3_S4_WLS	FUNC_TEST=TRUE
PP3V3_S5	FUNC_TEST=TRUE
PP3V3_S5G	FUNC_TEST=TRUE
PPVCCCPU_S0G	FUNC_TEST=TRUE
PPVCCGT_S0G	FUNC_TEST=TRUE
PPVCCIO_S0G	FUNC_TEST=TRUE
PPVCCOPC_S0G	FUNC_TEST=TRUE
PPVCCPCH_S5G	FUNC_TEST=TRUE
PPVCCSA_S0G	FUNC_TEST=TRUE
PPVTT_S0	FUNC_TEST=TRUE

WIRELESS

JTAG_WLAN_SEL	FUNC_TEST=TRUE
TP_JTAG_WLAN_TCK	FUNC_TEST=TRUE
JTAG_WLAN_TDI	FUNC_TEST=TRUE
TP_JTAG_WLAN_TDO	FUNC_TEST=TRUE
TP_JTAG_WLAN_TMS	FUNC_TEST=TRUE
TP_JTAG_WLAN_TRST	FUNC_TEST=TRUE

TRACKPAD AND KEYBOARD

ACT_THERM_TRIP_L	FUNC_TEST=TRUE
FAN_LT_PWM	FUNC_TEST=TRUE
FAN_LT_TACH	FUNC_TEST=TRUE
KBD_BLC_GSLAT	FUNC_TEST=TRUE
KBD_BLC_GSSCK	FUNC_TEST=TRUE
KBD_BLC_GSSIN	FUNC_TEST=TRUE
KBD_BLC_GSSOUT	FUNC_TEST=TRUE
KBD_BLC_XBLANK	FUNC_TEST=TRUE
KBD_I2C_SCL	FUNC_TEST=TRUE
KBD_I2C_SDA	FUNC_TEST=TRUE
KBD_INT_L	FUNC_TEST=TRUE
TPAD_SPI_MOSI	FUNC_TEST=TRUE
TPAD_SPI_INT_L	FUNC_TEST=TRUE
TPAD_SPI_CS_CONN_L	FUNC_TEST=TRUE
TPAD_SPI_MISO	FUNC_TEST=TRUE
TPAD_SPI_IF_EN	FUNC_TEST=TRUE
TPAD_SPI_CLK	FUNC_TEST=TRUE
TPAD_VIBE_L	FUNC_TEST=TRUE
SMC_LSOC_RST	FUNC_TEST=TRUE
SMC_ONOFF_L	FUNC_TEST=TRUE
SMC_PME_S4_WAKE_L	FUNC_TEST=TRUE
PP3V3_G3H	FUNC_TEST=TRUE
PP3V3_S4	FUNC_TEST=TRUE
PP5V_S0	FUNC_TEST=TRUE
PP5V_S4_TPAD_CONN	FUNC_TEST=TRUE
PPVIN_S4_TPAD_FUSE	FUNC_TEST=TRUE
GND	FUNC_TEST=TRUE

EDP_ML_C_N<0..3>	NO_TEST=1
EDP_ML_C_P<0..3>	NO_TEST=1
EDP_INT_ML_N<0..3>	NO_TEST=1
EDP_INT_ML_P<0..3>	NO_TEST=1
PCIE_AP_D2R_C_N	NO_TEST=1
PCIE_AP_D2R_C_P	NO_TEST=1
PCIE_AP_D2R_N	NO_TEST=1
PCIE_AP_D2R_P	NO_TEST=1
PCIE_AP_R2D_C_N	NO_TEST=1
PCIE_AP_R2D_C_P	NO_TEST=1
PCIE_AP_R2D_N	NO_TEST=1
PCIE_AP_R2D_P	NO_TEST=1
PCIE_SSD_D2R_N<0..3>	NO_TEST=1
PCIE_SSD_D2R_P<0..3>	NO_TEST=1
PCIE_SSD_R2D_C_N<0..3>	NO_TEST=1
PCIE_SSD_R2D_C_P<0..3>	NO_TEST=1
PCIE_SSD_R2D_N<0..3>	NO_TEST=1
PCIE_SSD_R2D_P<0..3>	NO_TEST=1
USB_UPC_XB_F_N	NO_TEST=1
USB_UPC_XB_F_P	NO_TEST=1
USBC_XA_D2R_N<1..2>	NO_TEST=1
USBC_XA_D2R_P<1..2>	NO_TEST=1
USBC_XA_R2D_C_N<1..2>	NO_TEST=1
USBC_XA_R2D_C_P<1..2>	NO_TEST=1
USBC_XA_R2D_N<1..2>	NO_TEST=1
USBC_XA_R2D_P<1..2>	NO_TEST=1
USBC_XA_USB_BOT_N	NO_TEST=1
USBC_XA_USB_BOT_P	NO_TEST=1
USBC_XA_USB_TOP_N	NO_TEST=1
USBC_XA_USB_TOP_P	NO_TEST=1
USBC_XB_D2R_N<1..2>	NO_TEST=1
USBC_XB_D2R_P<1..2>	NO_TEST=1
USBC_XB_R2D_C_N<1..2>	NO_TEST=1
USBC_XB_R2D_C_P<1..2>	NO_TEST=1
USBC_XB_R2D_N<1..2>	NO_TEST=1
USBC_XB_R2D_P<1..2>	NO_TEST=1
USBC_XB_USB_BOT_N	NO_TEST=1
USBC_XB_USB_BOT_P	NO_TEST=1
USBC_XB_USB_TOP_N	NO_TEST=1
USBC_XB_USB_TOP_P	NO_TEST=1
AGND_U7320	NO_TEST=1
BANJO_VBSTVR1	NO_TEST=1
BANJO_VBSTVR3	NO_TEST=1
BANJO_VBSTVR4	NO_TEST=1
BANJO_VBSTVR5	NO_TEST=1
CPUVR_BP2	NO_TEST=1
CPUVR_PHASE2	
CPUVR_SNB1	NO_TEST=1
CPUVR_SNB2	NO_TEST=1
PD_VSNS_CPU_VCCEOPIO_TN	NO_TEST=1
PD_VSNS_CPU_VCCOPC_TN	NO_TEST=1
PPVCCCPU_S0G_PH1	NO_TEST=1
PPVCCCPU_S0G_PH2	NO_TEST=1
PPVCCSA_S0G_R	NO_TEST=1
PU_VSNS_CPU_VCCEOPIO_TP	NO_TEST=1
PU_VSNS_CPU_VCCOPC_TP	NO_TEST=1
VR0V9_IND_TBT_X	NO_TEST=1
PP1V_SUS_PCH_VCCAPLL_F	NO_TEST=1
PP1V8_S0_PCH_VCCHDA_F	NO_TEST=1

FOR DC/DC

TBA_HPWR_EN_L	FUNC_TEST=TRUE
PD_TBA_MPM_DET	FUNC_TEST=TRUE

FOR DEBUG

TP_UPC_XA_DBG_UART_TX	FUNC_TEST=TRUE
TP_UPC_XA_DBG_UART_RX	FUNC_TEST=TRUE
TP_UPC_XB_DBG_UART_TX	FUNC_TEST=TRUE
TP_UPC_XB_DBG_UART_RX	FUNC_TEST=TRUE

BOM_COST_GROUP=NO COST ITEMS

MEM_A_CAA<0..9>	NO_TEST=1
MEM_A_CAB<0..9>	NO_TEST=1
MEM_A_CKE<0..3>	NO_TEST=1
MEM_A_CLK_N<0..1>	NO_TEST=1
MEM_A_CLK_P<0..1>	NO_TEST=1
MEM_A_CS_L<0..1>	NO_TEST=1
MEM_A_DQ<0..63>	NO_TEST=1
MEM_A_DQS_N<0..7>	NO_TEST=1
MEM_A_DQS_P<0..7>	NO_TEST=1
MEM_A_ODT<0>	NO_TEST=1
MEM_B_CAA<0..9>	NO_TEST=1
MEM_B_CAB<0..9>	NO_TEST=1
MEM_B_CKE<0..3>	NO_TEST=1
MEM_B_CLK_N<0..1>	NO_TEST=1
MEM_B_CLK_P<0..1>	NO_TEST=1
MEM_B_CS_L<0..1>	NO_TEST=1
MEM_B_DQ<0..63>	NO_TEST=1
MEM_B_DQS_N<0..7>	NO_TEST=1
MEM_B_DQS_P<0..7>	NO_TEST=1
MEM_B_ODT<0>	NO_TEST=1
MEM_CAM_A<0..14>	NO_TEST=1
MEM_CAM_BA<0..2>	NO_TEST=1
MEM_CAM_DM<0..1>	NO_TEST=1
MEM_CAM_DQ<0..15>	NO_TEST=1
MEM_CAM_DQS_N<0..1>	NO_TEST=1
MEM_CAM_DQS_P<0..1>	NO_TEST=1
RF_0_ANT	NO_TEST=1
RF_0_ANT_MATCH_T	NO_TEST=1
RF_1_ANT	NO_TEST=1
RF_1_ANT_MATCH_T	NO_TEST=1
RF_A_0_DIPLEXER	NO_TEST=1
RF_A_0_MATCH	NO_TEST=1
RF_A_1_DIPLEXER	NO_TEST=1
RF_A_1_MATCH	NO_TEST=1
RF_G_0_DIPLEXER	NO_TEST=1
RF_G_0_MATCH	NO_TEST=1
RF_G_1_DIPLEXER	NO_TEST=1
RF_G_1_MATCH	NO_TEST=1
AGND_U7310	NO_TEST=1
BANJO_FBVR2_N	NO_TEST=1
BANJO_FBVR2_RC	NO_TEST=1
BANJO_SWVR2	NO_TEST=1
BANJO_SWVR2_SNUB	NO_TEST=1
BANJO_SWVR3R	NO_TEST=1
BANJO_SWVR3_SNUB	NO_TEST=1
BANJO_VBSTVR1_R	NO_TEST=1
BANJO_VBSTVR3_R	NO_TEST=1
BANJO_VBSTVR4_R	NO_TEST=1
BANJO_VBSTVR5_R	NO_TEST=1
CPUVR_BOOT1	NO_TEST=1
CPUVR_BP1	NO_TEST=1
CPUVR_ISNS2_N	NO_TEST=1
CPUVR_ISNS2_P	NO_TEST=1
CPUVR_PHASE1	NO_TEST=1
CPUVR_SW1	NO_TEST=1
CPU_PROCHOT_R_L	NO_TEST=1
CPU_VCCGTSENSE_N	NO_TEST=1
CPU_VCCST_PWRGD_R	NO_TEST=1
GTVR_BP1	
GTVR_ISNS2_P	NO_TEST=1
GTVR_SNB1	NO_TEST=1
GTVR_SNB2	NO_TEST=1
GTVR_SNB3	NO_TEST=1
GTVR_SW1	NO_TEST=1
GTVR_SW2	NO_TEST=1
P1VOPC_BOOT_RC	NO_TEST=1
P1VOPC_DRVH_R	NO_TEST=1
P1VOPC_REFIN_R	NO_TEST=1
P1VOPC_SNS_R	NO_TEST=1
P3V3S5_DRVH_R	NO_TEST=1
P5VS4_DRVH_R	NO_TEST=1
SAVR_BP	NO_TEST=1
SAVR_SNB1	NO_TEST=1
SAVR_SW	NO_TEST=1
VCINP_P5V_U7310	NO_TEST=1
AGND_U7470	NO_TEST=1
VCINP_P5V_U7310	NO_TEST=1
VCINP_P5V_U7320	NO_TEST=1
TBA_PHASE1	NO_TEST=1
PMIC_ENH	NO_TEST=1

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