1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X665 MLB DVT

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6			2017-08-14

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	DESCRIPTION	SCHEMATIC	BOARD	MCO	PANEL
MLB	POR FORM FACTOR MLB	051-01649	820-00967	056-04348	057-00903
DEV_MLB	ACRYLIC ONLY DEVELOPMENT MLB	951-04366	920-03304	056-04350	N/A
FLEX_PWR_BTN	FOR POR PWR BUTTON	051-02379	821-01249	056-04296	N/A
GS5_REDHEAD	SSD	051-02311	820-00899	056-04271	057-00906
FLEX_CAMERA_IA	CAMERA MODULE FLEX	051-01861	821-00978	056-04578	N/A
FLEX_INTERCONNECT_CAM_MIC	HUB FLEX	051-02325	821-01216	056-04194	N/A
FLEX_CG_MIC_LEFT	FLEX FROM HUB TO LEFT CG MIC	051-02369	821-01245	056-04245	N/A
FLEX_CG_MIC_RIGHT	FLEX FROM HUB TO RIGHT CG MIC	051-02370	821-01216	056-04246	N/A
FAN FLEX LEFT	FLEX FROM L FAN MODULE TO MLB	N/A	N/A	099-09233	N/A
FAN FLEX RIGHT	FLEX FROM R FAN MODULE TO MLB	N/A	N/A	099-09234	N/A

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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SYSTEM PCB SUMMARY

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PROGRAMMABLES

TBT T ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,U8ON8	U2890	CRITICAL	TBT_T_ROM:BLANK
341S00738	1	IC,T29,A81,VT8D,P0 DEV,X665	U2890	CRITICAL	TBT_T_ROM:POC
341S00795	1	IC,T29,A8,V15.4,PROTO 0,X665	U2890	CRITICAL	TBT_T_ROM:P0_V15P4
341S00846	1	IC,T29,A81-T,V15.10,PROTO1,X665	U2890	CRITICAL	TBT_T_ROM:P1A_V15P10
341S00902	1	IC,T29,A81-T,V15.10,EVT,X665	U2890	CRITICAL	TBT_T_ROM:EVT_V15P10

TBT X ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,U8ON8	U3490	CRITICAL	TBT_X_ROM:BLANK
341S00738	1	IC,T29,A81,VT8D,P0 DEV,X665	U3490	CRITICAL	TBT_X_ROM:POC
341S00795	1	IC,T29,A8,V15.4,PROTO 0,X665	U3490	CRITICAL	TBT_X_ROM:P0_V15P4
341S00847	1	IC,T290,A82-X,V15.10,PROTO1,X665	U3490	CRITICAL	TBT_X_ROM:P1A_V15P10
341S00903	1	IC,T29,A82-X,V15.10,EVT,X665	U3490	CRITICAL	TBT_X_ROM:EVT_V15P10

SD READER ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00024	1	IC,SERIAL FLASH,2MBIT,3V,8-USON,2X3X,6MM	U6230	CRITICAL	SD_ROM:BLANK_WINBOUND
335S00282	1	IC,SERIAL FLASH,2MBIT,3V,8-USON,2X3X,6MM	U6230	CRITICAL	SD_ROM:BLANK_MACRONIX
341S00733	1	IC,ROM,SDCARD CTLR GL3227A,V001,POC,X665	U6230	CRITICAL	SD_ROM:POC
341S00783	1	FW,SDCARD CTRL GL3227A,V002,POC,X665	U6230	CRITICAL	SD_ROM:P0_V002
341S00897	1	IC,ROM,SDCARD CTL GL3227A,VAP03,EVT,X665	U6230	CRITICAL	SD_ROM:EVT_VAP03

ETHERNET ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00269	1	IC,SPI SERIAL FLASH,32MBIT,3V,SOIC8	U6090	CRITICAL	ETHERNET_ROM:BLANK_ADESTO
341S00751	1	IC,ETHERNET,VT8D,PROTO 0,X665	U6090	CRITICAL	ETHERNET_ROM:POC
341S00793	1	IC,ETHERNET,VT8D,PROTO 0,X665	U6090	CRITICAL	ETHERNET_ROM:P0
341S00817	1	IC,ETHERNET,V2.5.24,PROTO1,X665	U6090	CRITICAL	ETHERNET_ROM:P1_V2P9P24
341S00864	1	IC,ETHERNET,V2.7.36,MDI NORMAL,P1B,X665	U6090	CRITICAL	ETHERNET_ROM:P1B_MDI_NORMAL
341S00901	1	IC,ETHERNET,V2.7.64,MDI NORMAL,EVT,X665	U6090	CRITICAL	ETHERNET_ROM:EVT_MDI_NORMAL

BT SERIAL FLASH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00255	1	IC,SPI SERIAL FLASH,2MBIT,1.8V,DFN8	UG450	CRITICAL	BT_FLASH:BLANK_ADESTO
335S00256	1	IC,SPI SERIAL FLASH,2MBIT,1.8V,DFN8	UG450	CRITICAL	BT_FLASH:BLANK_WINBOUND
341S00726	1	IC,BT,VT8D,POC,X665	UG450	CRITICAL	BT_FLASH:POC
341S00844	1	IC,BT,VT8D,POC,X665	UG450	CRITICAL	BT_FLASH:P1B
341S00892	1	IC,BT SFLASH,VT8D,EVT,X665	UG450	CRITICAL	BT_FLASH:EVT

WLAN SERIAL EEPROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00214	1	IC,EEPROM,EEP,UWIRE,16K,1.8V,DFN8	UG410	CRITICAL	WLAN_EEPROM:BLANK_ONSEMI
335S00216	1	IC,EEPROM,EEP,UWIRE,16K BITS,1.7V,DFN8	UG410	CRITICAL	WLAN_EEPROM:BLANK_ROHM
341S00725	1	IC,WIFI ROM,VT8D,POC,X665	UG410	CRITICAL	WLAN_EEPROM:POC

GPU BOOT ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0399	1	IC,FLASH,SERIAL,SPI,1M X 8,3.3V,MLP8,LF	UA920	CRITICAL	GPU_BOOT_ROM:BLANK
341S00729	1	VBIOS,ROM,VEGA10 GPU,V001,POC,X665	UA920	CRITICAL	GPU_BOOT_ROM:POC
341S00792	1	IC,VBIOS,ROM,VEGA10 GPU,V002,P0,X665	UA920	CRITICAL	GPU_BOOT_ROM:P0_V002
341S00863	1	IC,VBIOS,ROM,VEGA10 A0-XLA GPU,P1B,X665	UA920	CRITICAL	GPU_BOOT_ROM:P1B_A0_XLA
341S00862	1	IC,VBIOS,ROM,VEGA10 A0-XTA GPU,P1B,X665	UA920	CRITICAL	GPU_BOOT_ROM:P1B_A0_XTA
341S00888	1	IC,VBIOS,ROM,VEGA10 XLA GPU,A1,P1C,X665	UA920	CRITICAL	GPU_BOOT_ROM:P1C_A1_XLA
341S00887	1	IC,VBIOS,ROM,VEGA10 XTA GPU,A1,P1C,X665	UA920	CRITICAL	GPU_BOOT_ROM:P1C_A1_XTA
341S00899	1	IC,VBIOS,ROM,VEGA10 XLA GPU,A1,EVT,X665	UA920	CRITICAL	GPU_BOOT_ROM:EVT_A1_XLA
341S00898	1	IC,VBIOS,ROM,VEGA10 XTA GPU,A1,EVT,X665	UA920	CRITICAL	GPU_BOOT_ROM:EVT_A1_XTA
341S00943	1	IC,VBIOS,ROM,VEGA10,XTA GPU(V15)DVT,X665	UA920	CRITICAL	GPU_BOOT_ROM:DVT_A1_XTA
341S00944	1	IC,VBIOS,ROM,VEGA10,XLA GPU(V15)DVT,X665	UA920	CRITICAL	GPU_BOOT_ROM:DVT_A1_XLA

SILICON

CPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00415	1	CPU,SKYW,AM9S,L0,ESP,2.4,8C,130W,LGA2066	CPU	CRITICAL	CPU_X86:08C_EVT1
337S00360	1	CPU,SKYW,QLRX,L0,ES,2.4,10C,140W,LGA2066	CPU	CRITICAL	CPU_X86:10C_EVT1
337S00435	1	CPU,SKYW,QMVZ,Q8,8C,3.2,120W,BGA2066	CPU	CRITICAL	CPU_X86:08C_3P2GHZ_QMVZ
337S00434	1	CPU,SKYW,QN57,Q8,10C,3.0,120W,BGA2066	CPU	CRITICAL	CPU_X86:10C_3P0GHZ_QN57
337S00453	1	CPU,SKYW,QNH8,Q8,2.3,18C,140W,LGA2066	CPU	CRITICAL	CPU_X86:18C_2P3GHZ_QNH8

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-06198	1	CONN,CPU,SOCKET,R4,LGA2066,SKYLAKE W	U1000	CRITICAL	CPU_SOCKET:POC
511S00004	1	CONN,SOCKET R4 LGA2066	U1000	CRITICAL	CPU_SOCKET:POR_P0

PCH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00359	1	IC,PCH-H,KBL,SSKU02,QLL9,ES2,A0	U7000	CRITICAL	PCH:ES2_MAF_QLL9
337S00390	1	IC,PCH-H,KBL,SSKU02,QM36,SAF,ES2,A0	U7000	CRITICAL	PCH:ES2_SAF_QM36
337S00436	1	IC,PCH-H,KBL,SSKU02,QML1,SAF,Q8,BGA885	U7000	CRITICAL	PCH:QS_SAF_QML1

GPU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-11669	1	VEGA10 SDLE ADAPTER (VDDC)	UA000	CRITICAL	GPU:SDLE_VDDC
998-11670	1	VEGA10 SDLE ADAPTER (VDDCI/MVDD)	UA000	CRITICAL	GPU:SDLE_VDDCI_MVDD
337S00452	1	IC,GPU,AMD,VEGA10,XLA,A1,LF,PS,BGA2013	UA000	CRITICAL	GPU:XLA_08_SEC
337S00451	1	IC,GPU,AMD,VEGA10,XTA,A1,LF,PS,BGA2013	UA000	CRITICAL	GPU:XTA_16_SEC

TBT X,T

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00254	2	IC,TBT,ALPINE RIDGE,8LLSM,FBQ,C1,CSP337	U2800,U3400	CRITICAL	TBT_AR:C1

ACE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S00961	4	IC,CD3215,ACE,C00,USB PWR SW,8LNK,BGA96	U3100,U3200,U3700,U3800	CRITICAL	ACE:C0

SOC VR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00268	1	IC,PMU,CALPE,D2249A0,OTP-BG,CSP324	U7800	CRITICAL	PMU:A0_B

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00372	1	POP,SOC,GIBRALTAR+2G 20NM,M,B0,CSP1406	U3900	CRITICAL	SOC:B0_2G_MI_SCK

SILICON

SD CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-07938	1	IC,GL3227A,USB3 3.0 TO SD CARD READER 4.0	U6200	CRITICAL	SD:POC
338S00312	1	IC,GL3227A,USB3 3.0 TO SD CARD READER,QFN48	U6200	CRITICAL	SD:P0_A2

ETHERNET CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-08198	1	ETHERNET,10GBASE-T,PCIE,MAC+PHY	U5800	CRITICAL	ENET:A0
998-09963	1	IC,ETHERNET CONTROLLER,AQC107,B0,BGA224	U5800	CRITICAL	ENET:B0
338S00332	1	IC,ETHERNET CONTROLLER,AQC107,B1,BGA224	U5800	CRITICAL	ENET:B1

CPU CORE VR CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01192	1	IC,PXE1610-PM001,5+1,CTRL,QFN48	U9000	CRITICAL	VR_CPU_CORE:PM001
353S01239	1	IC,PXE1610-PM002,5+1,CTRL,QFN48	U9000	CRITICAL	VR_CPU_CORE:PM002
353S01376	1	IC,PXE1610-PM003,5+1,CTRL,QFN48	U9000	CRITICAL	VR_CPU_CORE:PM003

CPU VCCIO VR CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01193	1	IC,PXE1110-PMA001,1+0,VCCIO,CTRL,QFN40	U9400	CRITICAL	VR_CPU_VCCIO:PMA001
353S01240	1	IC,PXE1110-PMA002,1+0,VCCIO,CTRL,QFN40	U9400	CRITICAL	VR_CPU_VCCIO:PMA002
353S01377	1	IC,PXE1110-PMA003,1+0,VCCIO,CTRL,QFN40	U9400	CRITICAL	VR_CPU_VCCIO:PMA003

CPU VDDQ 01 VR CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01194	1	IC,PXE1110-PMB001,1+0,VDDQ_01,CTRL,QFN40	U9800	CRITICAL	VR_CPU_VDDQ01:PMB001
353S01241	1	IC,PXE1110-PMB002,1+0,VDDQ_01,CTRL,QFN40	U9800	CRITICAL	VR_CPU_VDDQ01:PMB002
353S01309	1	IC,PXE1110-PMB003,1+0,VDDQ_01,CTRL,QFN40	U9800	CRITICAL	VR_CPU_VDDQ01:PMB003
353S01378	1	IC,PXE1110-PMB004,1+0,VDDQ_01,CTRL,QFN40	U9800	CRITICAL	VR_CPU_VDDQ01:PMB004

CPU VDDQ 23 VR CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01195	1	IC,PXE1110-PMC001,1+0,VDDQ_23,CTRL,QFN40	U9900	CRITICAL	VR_CPU_VDDQ23:PMC001
353S01242	1	IC,PXE1110-PMC002,1+0,VDDQ_23,CTRL,QFN40	U9900	CRITICAL	VR_CPU_VDDQ23:PMC002
353S01310	1	IC,PXE1110-PMC003,1+0,VDDQ_23,CTRL,QFN40	U9900	CRITICAL	VR_CPU_VDDQ23:PMC003
353S01379	1	IC,PXE1110-PMC004,1+0,VDDQ_23,CTRL,QFN40	U9900	CRITICAL	VR_CPU_VDDQ23:PMC004

GPU CORE VR CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S00997	1	IC,IR35217-4199,BUCK CTRL,QFN56,7X7MM	UD000	CRITICAL	GPU_VR:P0_V4199
353S01246	1	IC,IR35217-4207,BUCK CTRL,QFN56,7X7MM	UD000	CRITICAL	GPU_VR:P1C_V4207
353S01380	1	IC,IR35217-4210,BUCK CTRL,QFN56,7X7MM	UD000	CRITICAL	GPU_VR:EVT_V4210
353S01469	1	IC,IR35217-3078,BUCK CTRL,QFN56,7X7MM	UD000	CRITICAL	GPU_VR:DVT_V3078

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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BOM CONFIGURATION

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BOM VARIANTS

BOM NUMBER	BOM NAME	BOM OPTIONS	
685-00136	COMMON PARTS,MLB,X665	X665_COMMON_PARTS	
639-04744	PCBA,MLB,08SS,08C,X665	X665_COMMON,X665_XLA_08_SEC,X665_08C	DVT
639-04745	PCBA,MLB,08SS,10C,X665	X665_COMMON,X665_XLA_08_SEC,X665_10C	DVT
639-05079	PCBA,MLB,08SS,18C,X665	X665_COMMON,X665_XLA_08_SEC,X665_18C	DVT
639-04746	PCBA,MLB,16SS,08C,X665	X665_COMMON,X665_XTA_16_SEC,X665_08C	DVT
639-04747	PCBA,MLB,16SS,10C,X665	X665_COMMON,X665_XTA_16_SEC,X665_10C	DVT
639-05080	PCBA,MLB,16SS,18C,X665	X665_COMMON,X665_XTA_16_SEC,X665_18C	DVT
939-05214	DEV,PCBA,MLB,16SS,18C,X665	X665_COMMON,X665_XTA_16_SEC,X665_08C,X665_DBG_EE	DVT DEV
939-04922	DEV,PCBA,MLB,GFX VDDC	X665_COMMON,X665_ADAPT_VDDC,X665_00C	DVT DEV
939-04923	DEV,PCBA,MLB,GFX VDDCI MVDD	X665_COMMON,X665_ADAPT_OTHR,X665_00C	DVT DEV

SYSTEM PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-01649	1	SCH,MLB,X665	SCH	CRITICAL	
820-00967	1	PCBF,MLB,X665	MLB	CRITICAL	
685-00136	1	COMMON PARTS,MLB,X665	CBOM	CRITICAL	X665_COMMON

COMMON BOM GROUPS

BOM GROUP	BOM OPTIONS
X665_COMMON_PARTS	COMMON,ALTERNATE:PART,ALT_CMN,X665_USBC,X665_NETWORK,X665_T290,X665_PWR,X665_SD,X665_X86_SUPPORT,X665_GPU,X665_DBG_MP
X665_USBC	ACE:C0,TBT_AR:C1,TBT_T_ROM:EVT_V15P10,TBT_X_ROM:EVT_V15P10
X665_NETWORK	BT_FLASH:EVT,WLAN_EEPROM:POC,ENET:B1,ETHERNET_ROM:EVT_MDI_NORMAL,ENET_REFCLK:OSC
X665_T290	PMU:A0_B,SOC:B0_2G_MI_SCK
X665_PWR	PWR_SEQUENCE:SMC,VR_CPU_CORE:PM003,VR_CPU_VCCIO:PMA003,VR_CPU_VDDQ01:PMB004,VR_CPU_VDDQ23:PMC004,GPU_VR:DVT_V3078
X665_SD	SD:P0_A2,SD_ROM:EVT_VAP03
X665_X86_SUPPORT	PCH:QS_SAF_QML1,CPU_SOCKET:POR_P0
X665_GPU	GPUCLK:XTAL
X665_DBG_MP	XDP,XDP_CONNECTOR,ESPI_DBG,DBG_FANTACH

GRAPHICS BOM GROUPS

BOM GROUP	BOM OPTIONS
X665_ADAPT_VDDC	GPU:SDLE_VDDC,GPU_BOOT_ROM:EVT_A1_XLA
X665_ADAPT_OTHR	GPU:SDLE_VDDCI_MVDD,GPU_BOOT_ROM:EVT_A1_XLA
X665_XLA_08_SEC	GPU:XLA_08_SEC,GPU_BOOT_ROM:DVT_A1_XLA
X665_XTA_16_SEC	GPU:XTA_16_SEC,GPU_BOOT_ROM:DVT_A1_XTA

CPU BOM GROUPS

BOM GROUP	BOM OPTIONS
X665_00C	CPU_X86:OFF
X665_08C	CPU_X86:08C_3P2GHZ_QMVZ
X665_10C	CPU_X86:10C_3P0GHZ_QN57
X665_18C	CPU_X86:18C_2P3GHZ_QNH8

EE ONLY DEBUG

BOM GROUP	BOM OPTIONS
X665_DBG_EE	DEBUG_UART,DEBUG_LEDS,DEBUG_LEDS_GFX

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COMPONENT ALTERNATES TRACKED IN <RDAR://24198640>

SYSTEM EE

197S0588	197S0591	ALT_CMN	ALL	J135 <RDAR://30128206>	XTAL,24.000MHZ,20PPM,9.5PF,60OHM,1.6X1.2
353S4376	353S3384	ALT_CMN	ALL	J135 <RDAR://30128375>	IC.LMV331,COMP,OPEN COL,2.7V,60UA,1SC70
376S0972	376S00075	ALT_CMN	ALL	J135 <RDAR://30128436>	MOSFET,N-CH,30V,100MA,13.0OHM,VMT3,HF
107S00112	107S00006	ALT_CMN	ALL	J135 <RDAR://30128488>	THERMISTOR,NTC,47K OHM,1%,4073K,0603
311S00112	311S0437	ALT_CMN	ALL	DAVID <RDAR://30156705>	IC,74LVC2G126,DUAL,3-STATE BUFFER,DFN8
353S00711	353S2073	ALT_CMN	ALL	DAVID <RDAR://30174231>	IC,NCS210,CURRENT SENSE,200V/V,SC70-6
371S00089	371S00085	ALT_CMN	ALL	DAVID <RDAR://30174773>	DIODE,SCHOTTKY,40V,2A,LOW VF,0603
371S0684	371S0495	ALT_CMN	ALL	DAVID <RDAR://30174773>	DIODE,DUAL SCHOTTKY,30V,200MA,SOT-363
372S0186	372S0185	ALT_CMN	ALL	DAVID <RDAR://30174982>	XSTR,NPN,65V,100MA,3P SOT883B
376S00015	376S0610	ALT_CMN	ALL	DAVID <RDAR://30195640>	XSTR,FET,DUAL N-CH,60V,3.3OHM,SOT-363
376S00001	376S0659	ALT_CMN	ALL	DAVID <RDAR://30196068>	MOSFET,P-CH,20V,4.2A,60MOHM@4.5V,SOT23
376S00146	376S1061	ALT_CMN	ALL	DAVID <RDAR://30197441>	FET,P-CH,20V,0.1A,3.8MOHM,DFN1006
311S00116	311S0324	ALT_CMN	ALL	DAVID <RDAR://30244248>	IC,74LVC2G34,DUAL BUFFER GATE,DFN6
311S00133	311S00130	ALT_CMN	ALL	DAVID <RDAR://30273650>	IC,74AVC1T45,XCVR,DL SUPPLY,1BIT,DFN-6
353S01041	353S01042	ALT_CMN	ALL	DAVID <RDAR://30275632>	IC,TS3312,V-REF,1.25V,0.15%,5MA,QFN8
371S00095	371S0567	ALT_CMN	ALL	DAVID <RDAR://30318051>	DIODE,SWITCH,100V,500MA,SOD323,2P
372S00008	372S0173	ALT_CMN	ALL	DAVID <RDAR://30352970>	XSTR,PNP,50V,100MA,100MVW,HFE=200,CST3
376S00224	376S1128	ALT_CMN	ALL	DAVID <RDAR://30430125>	NFET,30V,590MA,670MOHM,SOT883B
311S00141	311S0653	ALT_CMN	ALL	LEE <RDAR://30054342>	IC,PI6ULS5V9,I2C LEVEL TRANSLATOR,DFN-8
138S00013	138S0772	ALT_CMN	ALL	DAVID <RDAR://30703933>	CAP,CER,2.2UF,20%,10V,X6S,0402
311S0649	311S0541	ALT_CMN	ALL	DAVID <RDAR://30735093>	IC,SINGLE,2-INPUT AND GATE, 5P SOT553
138S0714	138S0713	ALT_CMN	ALL	DAVID <RDAR://30812224>	CAP,CER,10UF,6.3V,X5R0.7MM,0402,SAMSUNG
152S0098	155S0137	ALT_CMN	ALL	DAVID <RDAR://30812705>	IND,CHIP EMIFIL,1000OHM,200MA,10HM DCR
116S00007	116S00006	ALT_CMN	ALL	DAVID <RDAR://30812830>	RES,MTL FILM,0 OHM,TIGHT TOL,3A,0402
311S0426	311S00007	ALT_CMN	ALL	DAVID <RDAR://30904120>	IC,74LVC1G07,SNGL BUFFER W/OD OUT,SOT891
107S00015	107S00011	ALT_CMN	ALL	DAVID <RDAR://31047426>	RES,MTL FLM,0.000750HM,1%,4-L,0612,BLK
107S00101	107S00005	ALT_CMN	ALL	DAVID <RDAR://31047611>	RES,SENSE,0.005 OHM,1/3W,1%,100PPM,0306
107S0250	107S0248	ALT_CMN	ALL	DAVID <RDAR://31047727>	RES,SENSE,0.003OHM,1W,4-TERM,1%,0612,CYN
107S0240	107S0255	ALT_CMN	ALL	DAVID <RDAR://31048025>	RES,MTL FLM,.001OHM,1%,1W,0612,4-TERM
107S00041	107S00039	ALT_CMN	ALL	DAVID <RDAR://31048140>	RES,MF,.0005 OHM,1%,200PPM,1W,0612-4T
132S00064	132S0409	ALT_CMN	ALL	DAVID <RDAR://31048516>	CAP,X6S,0.1UF,20%,16V,0201
138S00006	138S0835	ALT_CMN	ALL	DAVID <RDAR://31048596>	CAP,CER,3-TERM,4.3UF,20%,4V,X5R,0402
138S00084	138S00060	ALT_CMN	ALL	DAVID <RDAR://31050082>	CAP,X5R,47UF,20%,6.3V,0603
138S0641	138S0700	ALT_CMN	ALL	DAVID <RDAR://31073310>	CAP,CER,X5R,2.2UF,20%,10V,0402
138S0703	138S0648	ALT_CMN	ALL	DAVID <RDAR://31073310>	CAP,CER,X5R,4.7UF,20%,6.3V,H=0.6MM,0402
138S0759	138S0762	ALT_CMN	ALL	DAVID <RDAR://31073517>	CAP,CER,1UF,20%,4V,X6S,0201
138S0739	138S0706	ALT_CMN	ALL	DAVID <RDAR://31077229>	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S0945	138S0706	ALT_CMN	ALL	DAVID <RDAR://31077229>	CAP,CER,1UF,20%,10V,X5R,0201
138S0831	138S00049	ALT_CMN	ALL	DAVID <RDAR://32926922>	CAP,CER,X5R,2.2UF,20%,6.3V,0201
155S0588	155S0367	ALT_CMN	ALL	DAVID <RDAR://31153563>	FLTR,EMI BEAD,120OHM,25%,3A,0603
155S00155	155S0441	ALT_CMN	ALL	DAVID <RDAR://31153579>	FERR BD,220 OHM,25%,1.5A,0.1 OHM,0603
155S00007	155S0667	ALT_CMN	ALL	DAVID <RDAR://31153776>	FLTR,COMMON MODE,90 OHM,100 MA,0202
197S00048	197S00036	ALT_CMN	ALL	DAVID <RDAR://31153886>	XTAL,25MHZ,30PPM,20PF,50OHM,500UW,2016
740S00035	740S0115	ALT_CMN	ALL	DAVID <RDAR://31183655>	FUSE,FAST-ACTING,2A,35V,26MOHM,0603
128S00042	128S0329	ALT_CMN	ALL	DAVID <RDAR://31203639>	CAP,TA,POLY,220UF,20%,6.3V,25MO,1.8A,B2
155S0731	155S0699	ALT_CMN	ALL	DAVID <RDAR://31824320>	FERR BD,120 OHM,25%,1.8A,60MOHM DCR,0402
311S0489	311S00118	ALT_CMN	ALL	DAVID <RDAR://32143855>	IC,SNGL,2-INPUT AND GATE, 5P SOT353-1
131S00246	131S0741	ALT_CMN	ALL	DAVID <RDAR://32169407>	CAP,COG,270PF,2%,50V,0402
152S00358	152S00208	ALT_CMN	ALL	DAVID <RDAR://31205760>	IND,MLD,1.0UH,20%,2.0A,120 MOHM,1608
152S00552	152S00002	ALT_CMN	ALL	DAVID <RDAR://31225584>	IND,PWR,2.2UH,20%,3.3A,82MOHM,2520
152S0835	152S00203	ALT_CMN	ALL	DAVID <RDAR://31226192>	IND,WW,2.2UH,20%,240MA,0.221 OHM,0603
152S1499	152S0864	ALT_CMN	ALL	DAVID <RDAR://31227799>	IND,47NH,2%,0.58OHM,0402,LF,HF
155S0830	155S0316	ALT_CMN	ALL	DAVID <RDAR://31244976>	FLTR,EMI,FER BD,600 OHM,100MH
197S0481	197S0343	ALT_CMN	ALL	DAVID <RDAR://31249918>	XTAL,25MHZ,20PPM,12PF,3.2X2.5X.6MM,85C
132S00153	132S0198	ALT_CMN	ALL	DAVID <RDAR://31284382>	CAP,X7R,1000PF,5%,2KV,1206
197S00096	197S00104	ALT_CMN	ALL	DAVID <RDAR://31249998>	XTAL,50MHZ,10PPM,8PF,40OHM,2016

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377S00103	377S0057	ALT_CMN	ALL	DAVID <RDAR://31309975>	SUPPR,TRANS,VARISTOR,6.8V,100PF,0402
377S00104	377S0068	ALT_CMN	ALL	DAVID <RDAR://31312281>	SUPPR,TRANS,VARISTOR,27V,47PF,0402
371S00127	371S00096	ALT_CMN	ALL	DAVID <RDAR://30359683>	DIODE,ZENER,3.0V,5%,250MW,SOD882-2
353S00636	353S4037	ALT_CMN	ALL	DAVID <RDAR://30432514>	IC,NX3DV42,DIFF USB SW,DPDT,QFN10,0.33MM
311S00138	311S0436	ALT_CMN	ALL	DAVID <RDAR://30474733>	IC,74AVC4T245,XCVR,4BIT,DUALSPPLY,QFN16
378S00074	378S00072	ALT_CMN	ALL	DAVID <RDAR://31561515>	LED,GREEN,568NM,4.3MCD@1MA,0402
378S00073	378S00067	ALT_CMN	ALL	DAVID <RDAR://31561520>	LED,RED,621NM,2.5MCD@1MA,1X0.6X0.25MM
311S0595	311S00155	ALT_CMN	ALL	DAVID <RDAR://31204779>	IX,XCVR,DL-BIT/DL-SUPPLY,2ST-OUT-QFN-10
371S00046	371S00082	ALT_CMN	ALL	DAVID <RDAR://31824517>	DIODE SCHOTTKY,30V,2A,LOW VF,0603
155S00067	155S0581	ALT_CMN	ALL	DAVID <RDAR://31230560>	FERR BD,240 OHM,25%,420MA,0.31 DCR,0201
311S0596	311S0593	ALT_CMN	ALL	DAVID <RDAR://32226608>	IC,VOLT-LEVEL TRANS,W/CONFIG GATE,SOT886
377S0178	377S00031	ALT_CMN	ALL	DAVID <RDAR://30735965>	SUPPR,TRANS,BIDIR,5.5V,0.2PF,0201
197S00129	197S00130	ALT_CMN	ALL	DAVID <RDAR://32196224>	OSC,XTAL,50MHZ,50PPM,3.3V,5032
376S00246	376S0865	ALT_CMN	ALL	LEWIS <RDAR://32512513>	NFET,20V,4A,0.038OHM,SOT23
197S00118	197S00120	ALT_CMN	ALL	LEWIS <RDAR://32818477>	XTAL,24MHZ,30PPM,9.5PF,60 OHM MAX,1612
155S00363	155S00367	ALT_CMN	ALL	JOHN <RDAR//32896387>	CHOKE,COMMONE MODE,67OHM,20%,400MA,0805-4
155S00364	155S00367	ALT_CMN	ALL	JOHN <RDAR//32896387>	CHOKE,COMMONE MODE,90OHM,50%,300MA,0805-4
157S00024	157S00026	ALT_CMN	ALL	JOHN <RDAR//32886430>	XFMR,LAN,10G,1CH,120UH,4532-8
197S00143	197S00142	ALT_CMN	ALL	ALAN <RDAR//33418271>	XTAL,27MHZ,10PPM,12PF,40OHM,2520
102S0880	102S0879	ALT_CMN	ALL	DAVID <RDAR//33305301>	RES,0.0100HM,1%,100PPM,1/2W,1206,BLK,CYN

DC-DC

152S00573	152S1778	ALT_CMN	ALL	SURESH <RDAR://29604818>	IND,0.105UH,20%,46A,0.35MOHM,6.8X6.8X5MM
152S00685	152S1778	ALT_CMN	ALL	LEWIS <RDAR//30977597>	IND,0.105UH,20%,46A,0.35MOHM,6.7X6.5X5MM
152S1684	152S1870	ALT_CMN	ALL	SURESH <RDAR//29190171>	IND,PWR,MOLD,2.2UH,20%,105MO,2.0A,2520
152S00408	152S00329	ALT_CMN	ALL	SURESH <RDAR//29078048>	IND,MLD,1.5UH,20%,13A,10.45MO,8.44X8X2.4
128S0364	128S0264	ALT_CMN	ALL	VINCENT MARKUP 03/20/2017	CAP,TANT,POLY,68UF,20%,16V,50MOHM,D2E,BLK
138S0775	138S0860	ALT_CMN	ALL	SURESH EMAIL 09/20/16	CAP,CER,X6S,1UF,10%,25V,0402
152S00398	152S00204	ALT_CMN	ALL	SURESH <RDAR//29078168>	IND,PWR,0.22UF,20%,6.7A,23MOHM,2012
152S00741	152S00699	ALT_CMN	ALL	LEWIS <RDAR//30499425>	IND,MLD,0.15UH,20%,90A,0.65MO,11.2X10X4
128S0444	128S0323	ALT_CMN	ALL	LEWIS <RDAR//29189353>	CAP,TANT,POLY,330UF,6.3V,25MOHM,2.4A,D2E
152S00747	152S00691	ALT_CMN	ALL	LEWIS <RDAR//30637603>	IND,MLD,1UH,20%,13.5A,6.6MOHM,7X6MOHM,7X6.6X3MM
152S00744	152S00692	ALT_CMN	ALL	LEWIS <RDAR//30638664>	IND,MLD,1.5UH,20%,9.5MOHM,12A,7.0X6.6X3
152S00743	152S00694	ALT_CMN	ALL	LEWIS <RDAR//30567068>	IND,MLD,3.3UH,20%,5A,32MOHM,4.85MOHM,4.85X4.7X3MM
152S00738	152S1685	ALT_CMN	ALL	LEWIS <RDAR//30568036>	IND,MLD,0.1UH,20%,21A,6MOHM,4.4X4.2X1.2
152S00748	152S00697	ALT_CMN	ALL	LEWIS <RDAR//30645234>	IND,MLD,0.36UH,20%,40A,0.8MOHM,11.2X10X4
128S0412	128S0237	ALT_CMN	ALL	LEWIS <RDAR//33154336>	CAP,TANT,PLY,BK,330UF,20%,6.3V,9MOHM,D3L
152S00608	152S00696	ALT_CMN	ALL	LEWIS <RDAR//29077951>	IND,MLD,0.22UH,65A,0.64MOHM,11.15X10.1X4
152S00774	152S00692	ALT_CMN	ALL	LEWIS <RDAR//31693715>	IND,MLD,1.5UH,20%,8.6MOHM,12A,7.0X6.6X3
353S01283	353S01013	ALT_CMN	ALL	LEWIS <RDAR//32001361>	IC,IR3575-4206,DR MOS,60A,PQFN31,6X6MM
138S00047	138S00073	ALT_CMN	ALL	LEWIS <RDAR//32229710>	CAP,CER,10UF,20%,6.3V,X6S,HRETL,TY,0402
152S00802	152S00698	ALT_CMN	ALL	LEWIS <RDAR//32231069>	IND,MLD,4.7UH,20%,8A,40MOHM,7X6.6X3MM
152S00803	152S00693	ALT_CMN	ALL	LEWIS <RDAR//32233571>	IND,MLD,2.2UH,20%,8A,35MOHM,5.0X4.7X3MM
152S00801	152S00695	ALT_CMN	ALL	LEWIS <RDAR//32229959>	IND,MLD,1UH,20%,23A,2.9MOHM,11.2X10X3.5
128S00038	128S00039	ALT_CMN	ALL	LEWIS <RDAR//32254335>	CAP,TA,POLY,150UF,20%,6.3V,18MO,2A,B2
128S00050	128S0351	ALT_CMN	ALL	LEWIS <RDAR//32261377>	CAP,TA,POLY,330UF,20%,2.5V,13MOHM,2A,B2
128S00008	128S0380	ALT_CMN	ALL	LEWIS <RDAR//32678648>	CAP,TA,POLY,220UF,20%,0.009 OHM,2.5V,B2
128S0631	128S0352	ALT_CMN	ALL	LEWIS <RDAR//32678456>	CAP,TANT,POLY,330UF,2.5V,9MOHM,B2
128S0375	128S0378	ALT_CMN	ALL	LEWIS <RDAR//32678872>	CAP,AL POLY,39UF,16V,27MOHM,2.35A,BLK

BLC

126-00012	126-0306	ALT_CMN	ALL	LINDA KAMAS 02/08/2017 EMAIL	CAP,AL EL,100UF,20%,35V,0.3A,6.3X11,BLK
152S00740	152S1668	ALT_CMN	ALL	LINDA KAMAS 02/08/2017 EMAIL	IND,MOD,33UH,9.4A TYP,39MOHM,17X17X7MM
138S1078	138S0810	ALT_CMN	ALL	LINDA KAMAS 02/08/2017 EMAIL	CAP,CER,2.2UF,10%,100V,X7R,1206,SFT,MRTA
124-00003	126-00013	ALT_CMN	ALL	BLC OUTPUT CAPS	CAP,AL-PLY,180UF,20,100V,105C,3A,10X13,BK
371S0748	371S0731	ALT_CMN	ALL	BLC INPUT DIODE	DIODE,SCHOTTKY,30V,1A,SOD-323
371S0782	371S0783	ALT_CMN	ALL	BLC OUTPUT DIODE	DIODE,RECT,STPS8H100G,100V,8A,TO263
376S0845	376S1067	ALT_CMN	ALL	BLC POWER FET + 12V POWER FET	MOSFET,P-CH,30V,9.4MOHM,23.7A,5X6 DFN
376S1204	376S1106	ALT_CMN	ALL	BLC LED SINK FET	MOSFET,NCH,100V,12.5A,24MOHM,3X3 DFN
740S0145	740S0146	ALT_CMN	ALL	BLC FUSE	FUSE 6A 32V SMD 0603
107S0359	107S0229	ALT_CMN	ALL	BLC BOOST SENSE RES	RES,FILM,2W,.03 OHM,1%,2512,SMD
376S1184	376S1183	ALT_CMN	ALL	BLC BOOST FET	MOSFET,NCH,100V,30A,31.5MOHM,3X3 MLP
376S1256	376S1073	ALT_CMN	ALL	BLC SHORT PROTECTION FETS	XSTR,FET,N-CH,150V,1.4A,425MOHM,SSOT-6L
155S0831	155S0797	ALT_CMN	ALL	BLC FERRITE BEADS	FLTR,EMI,FER BD,600 OHM,100MHZ,0603
138S0805	138S0834	ALT_CMN	ALL	LINDA KAMAS 02/24/2017 EMAIL	CAP,CER,10UF,10%,25V,X7R,1206,SOFT

N&V

138S00077	138S00035	ALT_CMN	ALL	AAASH BUILD MATRIX REV 3.0	CAP,X6S,20UF,20%,2.5V,HETL,TY,0402
138S00169	138S00168	ALT_CMN	ALL	AAASH BUILD MATRIX REV 3.0	CAP,X6S,43UF,20%,2.5V,NU,0603
138S00111	138S00036	ALT_CMN	ALL	AAASH BUILD MATRIX REV 3.0	CAP,X6S,20UF,20%,2.5V,NU,0402
138S00188	138S00043	ALT_CMN	ALL	DAVID <RDAR//31632406>	CAP,X6S,10UF,20%,6.3V,0402,NU

WIRELESS

339S00411	339S00404	ALT_CMN	ALL	METE EMAIL ON 05/16/2017	MODULE,WIFI/BT,HARPOON,USI,ES7.1,LGA324
339S00425	339S00404	ALT_CMN	ALL	METE EMAIL ON 05/16/2017	MODULE,WIFI/BT,HARPOON,M,ES7.3,LGA385
339S00427	339S00404	ALT_CMN	ALL	METE EMAIL ON 05/16/2017	MODULE,WIFI/BT,HARPOON,USI,ES7.3,LGA385
339S00426	339S00404	ALT_CMN	ALL	METE EMAIL ON 05/16/2017	MODULE,WIFI/BT,HARPOON,M,ES7.5,LGA385
339S00428	339S00404	ALT_CMN	ALL	METE EMAIL ON 05/16/2017	MODULE,WIFI/BT/HARPOON/USI/ES7.5,LGA385

SOC

339S00373	339S00372	ALT_CMN	ALL	LYNN 03/21/17 SILICON SYNC	POP,SOC,GIBRALTAR+2G 21NM,H,B0,CSP1406
339S00377	339S00372	ALT_CMN	ALL	LYNN 03/21/17 SILICON SYNC	POP,GIBRALTAR+2G 20NM,M,B0,ATK,CSP1406
339S00378	339S00372	ALT_CMN	ALL	LYNN 03/21/17 SILICON SYNC	POP,GIBRALTAR+2G 21NM,H,B0,ATK,CSP1406

AUDIO

155S0660	155S0513	ALT_CMN	ALL	DAVID<RDAR://31153630>	FERR BD,220OHM,25%,1.8A,40MOHM DCR,0201
138S1103	138S0719	ALT_CMN	ALL	DAVID<RDAR://31153099>	CAP,CER,4.7UF,20%,10V,X5R,0402
155S00034	155S0706	ALT_CMN	ALL	DAVID<RDAR://31153821>	FERR BD,120 OHM,25%,1.3A,0.09 OHM,0402
138S0841	138S0638	ALT_CMN	ALL	DAVID <RDAR://31205208>	CAP,CER,10UF,10%,25V,X5R,0805,MURATA
155S00203	155S0894	ALT_CMN	ALL	DAVID <RDAR//31153858>	FLTR,MLD,180 OHM,3.4A,0.025OHM,2016
353S01341	353S00920	ALT_CMN	ALL	DAVID <RDAR//30173238>	IC,LDO REG,1.8V,250MA,LOW NOISE,STO23-5

PD

099-09276	870-3024	ALT_CMN	ALL	JANET H IN 05/18/2017 EMAIL	SPRING FINGER,P5S-20X30X31,J28
099-09277	870-1415	ALT_CMN	ALL	JANET H IN 05/18/2017 EMAIL	SPRING FINGER,3.2 X 1.2 X 0.8MM,SMD

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SOLDERED PARTS

SHIELD FENCE AR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-11526	1	SHIELD FENCE,MLB,AR,X664	SHIELD_FENCE_AR	CRITICAL	

SHIELD CAN RJ45

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-10607	1	SHIELD,CAN,RJ45,X664	SHIELD_CAN_RJ45	CRITICAL	

SHIELD CAN HARPOON

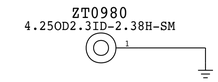
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-10608	1	SHIELD CAN,HARPOON,X664	SHIELD_HPN_CAN	CRITICAL	

SHIELD FENCE HARPOON

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-12956	1	SHIELD,FENCE,WIFI,X664	SHIELD_HPN_FENCE	CRITICAL	

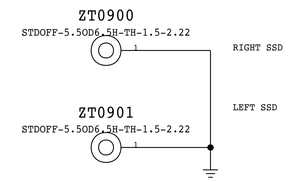
AUDIO BOSS

(860-00773)



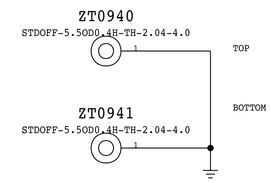
GS5 SSD STANDOFF

2.35MM HOLE, 5.8MM PAD, WITH BOSS INCLUDED (860-00739)



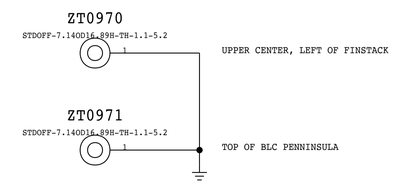
WIRELESS STRAIN RELIEF STANDOFFS

4.11MM HOLE, 6.00MM PAD, WITH BOSS INCLUDED (860-00713)



MLB STANDOFFS

5.38MM HOLE, 8.5MM PAD, WITH BOSS INCLUDED (860-00708)



BOM_COST_GROUP=MECHANICALS

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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OMIT_TABLE

U1000
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SYM 2 OF 16
CRITICAL

MEM_0_DQ<63..0>			
DD52	DDR0_DQ[63]	DDR0_DQS_DP[17]	DD18
DE51	DDR0_DQ[62]	DDR0_DQS_DP[16]	DD50
DB48	DDR0_DQ[61]	DDR0_DQS_DP[15]	CU47
DD48	DDR0_DQ[60]	DDR0_DQS_DP[14]	DD44
DA51	DDR0_DQ[59]	DDR0_DQS_DP[13]	DD38
DB52	DDR0_DQ[58]	DDR0_DQS_DP[12]	CY14
DA49	DDR0_DQ[57]	DDR0_DQS_DP[11]	CY8
DE49	DDR0_DQ[56]	DDR0_DQS_DP[10]	CR3
CP48	DDR0_DQ[55]	DDR0_DQS_DP[9]	CR4
CV48	DDR0_DQ[54]	DDR0_DQS_DP[8]	DB20
CR45	DDR0_DQ[53]	DDR0_DQS_DP[7]	CY50
CP46	DDR0_DQ[52]	DDR0_DQS_DP[6]	CR47
CR49	DDR0_DQ[51]	DDR0_DQS_DP[5]	CY44
CU49	DDR0_DQ[50]	DDR0_DQS_DP[4]	DB38
CV46	DDR0_DQ[49]	DDR0_DQS_DP[3]	DD14
CU45	DDR0_DQ[48]	DDR0_DQS_DP[2]	DF8
DD46	DDR0_DQ[47]	DDR0_DQS_DP[1]	CU5
DE45	DDR0_DQ[46]	DDR0_DQS_DP[0]	CR4
DB42	DDR0_DQ[45]		
DD42	DDR0_DQ[44]	DDR0_DQS_DN[17]	DC19
DA45	DDR0_DQ[43]	DDR0_DQS_DN[16]	DF50
DB46	DDR0_DQ[42]	DDR0_DQS_DN[15]	CW47
DE43	DDR0_DQ[41]	DDR0_DQS_DN[14]	DF44
DA43	DDR0_DQ[40]	DDR0_DQS_DN[13]	DF38
DA39	DDR0_DQ[39]	DDR0_DQS_DN[12]	DB14
DE39	DDR0_DQ[38]	DDR0_DQS_DN[11]	DB8
DD36	DDR0_DQ[37]	DDR0_DQS_DN[10]	CP2
DB36	DDR0_DQ[36]	DDR0_DQS_DN[9]	CD4
DB40	DDR0_DQ[35]	DDR0_DQS_DN[8]	DA21
DD40	DDR0_DQ[34]	DDR0_DQS_DN[7]	DB50
DE37	DDR0_DQ[33]	DDR0_DQS_DN[6]	CW47
DA37	DDR0_DQ[32]	DDR0_DQS_DN[5]	DB44
DA15	DDR0_DQ[31]	DDR0_DQS_DN[4]	CY38
DE15	DDR0_DQ[30]	DDR0_DQS_DN[3]	DF14
DB12	DDR0_DQ[29]	DDR0_DQS_DN[2]	DD8
DA13	DDR0_DQ[28]	DDR0_DQS_DN[1]	CT4
DD16	DDR0_DQ[27]	DDR0_DQS_DN[0]	CF4
DB16	DDR0_DQ[26]		
DE13	DDR0_DQ[25]	DDR0_MA[17]	CU33
DD12	DDR0_DQ[24]	DDR0_MA[16]	DB30
DE9	DDR0_DQ[23]	DDR0_MA[15]	CT30
DA9	DDR0_DQ[22]	DDR0_MA[14]	DC31
DD6	DDR0_DQ[21]	DDR0_MA[13]	CW31
DB6	DDR0_DQ[20]	DDR0_MA[12]	DF24
DD10	DDR0_DQ[19]	DDR0_MA[11]	CY24
DB10	DDR0_DQ[18]	DDR0_MA[10]	CW29
DE7	DDR0_DQ[17]	DDR0_MA[9]	DC25
DA7	DDR0_DQ[16]	DDR0_MA[8]	DE25
CV2	DDR0_DQ[15]	DDR0_MA[7]	CP22
CT2	DDR0_DQ[14]	DDR0_MA[6]	CY26
CN5	DDR0_DQ[13]	DDR0_MA[5]	CW25
CM4	DDR0_DQ[12]	DDR0_MA[4]	DB26
CW3	DDR0_DQ[11]	DDR0_MA[3]	CU25
CV4	DDR0_DQ[10]	DDR0_MA[2]	CT26
CN3	DDR0_DQ[9]	DDR0_MA[1]	DC27
CR5	DDR0_DQ[8]	DDR0_MA[0]	CT28
CJ3	DDR0_DQ[7]		
CG3	DDR0_DQ[6]	DDR0_ECC[7]	DE19
CC5	DDR0_DQ[5]	DDR0_ECC[6]	DC21
CA5	DDR0_DQ[4]	DDR0_ECC[5]	DB18
CJ5	DDR0_DQ[3]	DDR0_ECC[4]	CY18
CG5	DDR0_DQ[2]	DDR0_ECC[3]	DF20
CC3	DDR0_DQ[1]	DDR0_ECC[2]	DE21
CA3	DDR0_DQ[0]	DDR0_ECC[1]	CY20
		DDR0_ECC[0]	CW19
		DDR0_CKE[3]	DC23
		DDR0_CKE[2]	DE23
NC	DE30 DDR0_CS_7*	DDR0_CKE[1]	CU21
NC	DB30 DDR0_CS_6*	DDR0_CKE[0]	CT22
NC	CT30 DDR0_CS_5*		
NC	DE30 DDR0_CS_4*		
MEM_0_CS_L<3>	CT30 DDR0_CS_3*	DDR0_BA[1]	DC29
MEM_0_CS_L<2>	CY30 DDR0_CS_2*	DDR0_BA[0]	CU29
MEM_0_CS_L<1>	CY30 DDR0_CS_1*		
MEM_0_CS_L<0>	CY30 DDR0_CS_0*	DDR0_BG[1]	DB24
		DDR0_BG[0]	CT24
NC	DE26 DDR0_CLK_DP[3]		
NC	DB28 DDR0_CLK_DP[2]	DDR0_ODT[3]	DE33
MEM_0_CLK_P<1>	CP24 DDR0_CLK_DP[1]	DDR0_ODT[2]	DB32
MEM_0_CLK_P<0>	CW27 DDR0_CLK_DP[0]	DDR0_ODT[1]	CW33
		DDR0_ODT[0]	CU31
NC	DE27 DDR0_CLK_DN[3]		
NC	CY28 DDR0_CLK_DN[2]	DDR0_CID_2	DC33
MEM_0_CLK_N<1>	CN25 DDR0_CLK_DN[1]	DDR0_PAR	DE29
MEM_0_CLK_N<0>	CU27 DDR0_CLK_DN[0]	DDR0_ACT*	CU23
		DDR0_ALERT*	CW23
		DDR0_CAVREF	CD20

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MEM_0_ECC<7..0>	
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MEM_0_CKE<1>	
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MEM_0_BG<0>	
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MEM_0_ODT<1>	
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MEM_0_ALERT_L	
PPVREFCA_MEM_0_CPU	22

BOM_COST_GROUP=CPU & CHIPSET

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OMIT_TABLE

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CRITICAL

MEM_1_DQ<63..0>	CE49	DDR1_DQ[63]	DDR1_DQS_DP[17]	CP18	MEM_1_DQS_P<17..0>
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	CM50	DDR1_DQ[60]	DDR1_DQS_DP[14]	CU41	
	CF48	DDR1_DQ[59]	DDR1_DQS_DP[13]	CK38	
	CH48	DDR1_DQ[58]	DDR1_DQS_DP[12]	CD14	
	CJ51	DDR1_DQ[57]	DDR1_DQS_DP[11]	CM14	
	CL51	DDR1_DQ[56]	DDR1_DQS_DP[10]	CM8	
	CK46	DDR1_DQ[55]	DDR1_DQS_DP[9]	CD8	
	CL45	DDR1_DQ[54]	DDR1_DQS_DP[8]	CM18	
	CG43	DDR1_DQ[53]	DDR1_DQS_DP[7]	CH50	
	CH42	DDR1_DQ[52]	DDR1_DQS_DP[6]	CH44	
	CG45	DDR1_DQ[51]	DDR1_DQS_DP[5]	CR41	
	CH46	DDR1_DQ[50]	DDR1_DQS_DP[4]	CF38	
	CL43	DDR1_DQ[49]	DDR1_DQS_DP[3]	BY14	
	CK42	DDR1_DQ[48]	DDR1_DQS_DP[2]	CN13	
	CU43	DDR1_DQ[47]	DDR1_DQS_DP[1]	CP8	
	CV42	DDR1_DQ[46]	DDR1_DQS_DP[0]	CB10	
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	CR39	DDR1_DQ[44]	DDR1_DQS_DN[17]	CT18	MEM_1_DQS_N<17..0>
	CR43	DDR1_DQ[43]	DDR1_DQS_DN[16]	CK48	
	CP42	DDR1_DQ[42]	DDR1_DQS_DN[15]	CM44	
	CV40	DDR1_DQ[41]	DDR1_DQS_DN[14]	CW41	
	CU39	DDR1_DQ[40]	DDR1_DQS_DN[13]	CM38	
	CK40	DDR1_DQ[39]	DDR1_DQS_DN[12]	CF14	
	CL39	DDR1_DQ[38]	DDR1_DQS_DN[11]	CL15	
	CG37	DDR1_DQ[37]	DDR1_DQS_DN[10]	CK8	
	CH36	DDR1_DQ[36]	DDR1_DQS_DN[9]	CE7	
	CH40	DDR1_DQ[35]	DDR1_DQS_DN[8]	CK18	
	CG39	DDR1_DQ[34]	DDR1_DQS_DN[7]	CC51	
	CL37	DDR1_DQ[33]	DDR1_DQS_DN[6]	CF44	
	CK36	DDR1_DQ[32]	DDR1_DQS_DN[5]	CN41	
	CD16	DDR1_DQ[31]	DDR1_DQS_DN[4]	CH38	
	CE15	DDR1_DQ[30]	DDR1_DQS_DN[3]	CB14	
	CA13	DDR1_DQ[29]	DDR1_DQS_DN[2]	CP12	
	CB12	DDR1_DQ[28]	DDR1_DQS_DN[1]	CT8	
	CB16	DDR1_DQ[27]	DDR1_DQS_DN[0]	CC9	
	CA15	DDR1_DQ[26]			
	CE13	DDR1_DQ[25]	DDR1_MA[17]	CD32	MEM_1_MA<17..0>
	CD12	DDR1_DQ[24]	DDR1_MA[16]	CN29	
	CT14	DDR1_DQ[23]	DDR1_MA[15]	CL31	
	CR13	DDR1_DQ[22]	DDR1_MA[14]	CP30	
	CK14	DDR1_DQ[21]	DDR1_MA[13]	CP32	
	CJ13	DDR1_DQ[20]	DDR1_MA[12]	CP26	
	CR15	DDR1_DQ[19]	DDR1_MA[11]	CL25	
	CN15	DDR1_DQ[18]	DDR1_MA[10]	CD30	
	CM12	DDR1_DQ[17]	DDR1_MA[9]	CN23	
	CK12	DDR1_DQ[16]	DDR1_MA[8]	CL23	
	CP10	DDR1_DQ[15]	DDR1_MA[7]	CD26	
	CR9	DDR1_DQ[14]	DDR1_MA[6]	CK24	
	CL7	DDR1_DQ[13]	DDR1_MA[5]	CR27	
	CJ7	DDR1_DQ[12]	DDR1_MA[4]	CH24	
	CM10	DDR1_DQ[11]	DDR1_MA[3]	CD28	
	CL9	DDR1_DQ[10]	DDR1_MA[2]	CE29	
	CU7	DDR1_DQ[9]	DDR1_MA[1]	CG25	
	CR7	DDR1_DQ[8]	DDR1_MA[0]	CP28	
	CG9	DDR1_DQ[7]			MEM_1_ECC<7..0>
	CP8	DDR1_DQ[6]	DDR1_ECC[7]	CP20	
	BY8	DDR1_DQ[5]	DDR1_ECC[6]	CR19	
	CA9	DDR1_DQ[4]	DDR1_ECC[5]	CL17	
	CP10	DDR1_DQ[3]	DDR1_ECC[4]	CJ17	
	CD10	DDR1_DQ[2]	DDR1_ECC[3]	CM20	
	CC7	DDR1_DQ[1]	DDR1_ECC[2]	CL19	
	CA7	DDR1_DQ[0]	DDR1_ECC[1]	CU17	
			DDR1_ECC[0]	CR17	
			DDR1_CKE[3]	CE21	NC
			DDR1_CKE[2]	CJ21	NC
			DDR1_CKE[1]	CG23	MEM_1_CKE<1>
			DDR1_CKE[0]	CE23	MEM_1_CKE<0>
NC	CP34	DDR1_CS_7*			
NC	CN33	DDR1_CS_6*			
NC	CK32	DDR1_CS_5*			
NC	CK30	DDR1_CS_4*			
MEM_1_CS_L<3>	CE33	DDR1_CS_3*	DDR1_BA[1]	CK28	MEM_1_BA<1>
MEM_1_CS_L<2>	CD34	DDR1_CS_2*	DDR1_BA[0]	CL29	MEM_1_BA<0>
MEM_1_CS_L<1>	CG33	DDR1_CS_1*			
MEM_1_CS_L<0>	CE31	DDR1_CS_0*	DDR1_BG[1]	CE25	MEM_1_BG<1>
			DDR1_BG[0]	CD24	MEM_1_BG<0>
NC	CK26	DDR1_CLK_DP[3]			
NC	CH26	DDR1_CLK_DP[2]			
MEM_1_CLK_P<1>	CH30	DDR1_CLK_DP[1]	DDR1_ODT[3]	CL33	NC
MEM_1_CLK_P<0>	CH28	DDR1_CLK_DP[0]	DDR1_ODT[2]	CN31	NC
			DDR1_ODT[1]	CH34	MEM_1_ODT<1>
			DDR1_ODT[0]	CH32	MEM_1_ODT<0>
NC	CL27	DDR1_CLK_DN[3]			
NC	CG27	DDR1_CLK_DN[2]	DDR1_CID[2]	CK34	TP_MEM_1_CID_2
MEM_1_CLK_N<1>	CG31	DDR1_CLK_DN[1]	DDR1_PAR	CN27	MEM_1_PARITY
MEM_1_CLK_N<0>	CG29	DDR1_CLK_DN[0]	DDR1_ACT*	CH22	MEM_1_ACT_L
			DDR1_ALERT*	CK22	MEM_1_ALERT_L
			DDR1_CAVREF	CH20	PPVREFCA_MEM_1_CPU

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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CPU MEMORY CHANNEL 1

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CRITICAL

Signal	Pin	Net
DDR3_DQ[63]	N47	MEM_2_DQ<63..0>
DDR3_DQ[62]	M48	
DDR3_DQ[61]	J45	
DDR3_DQ[60]	K44	
DDR3_DQ[59]	J47	
DDR3_DQ[58]	K48	
DDR3_DQ[57]	N45	
DDR3_DQ[56]	M44	
DDR3_DQ[55]	C51	
DDR3_DQ[54]	B50	
DDR3_DQ[53]	E47	
DDR3_DQ[52]	C47	
DDR3_DQ[51]	F50	
DDR3_DQ[50]	E51	
DDR3_DQ[49]	B48	
DDR3_DQ[48]	F48	
DDR3_DQ[47]	F44	
DDR3_DQ[46]	B44	
DDR3_DQ[45]	F42	
DDR3_DQ[44]	E41	
DDR3_DQ[43]	C45	
DDR3_DQ[42]	E45	
DDR3_DQ[41]	B42	
DDR3_DQ[40]	C41	
DDR3_DQ[39]	C39	
DDR3_DQ[38]	B38	
DDR3_DQ[37]	E35	
DDR3_DQ[36]	C35	
DDR3_DQ[35]	F38	
DDR3_DQ[34]	E39	
DDR3_DQ[33]	B36	
DDR3_DQ[32]	F36	
DDR3_DQ[31]	C15	
DDR3_DQ[30]	B14	
DDR3_DQ[29]	E12	
DDR3_DQ[28]	E11	
DDR3_DQ[27]	E15	
DDR3_DQ[26]	F14	
DDR3_DQ[25]	B12	
DDR3_DQ[24]	C11	
DDR3_DQ[23]	F8	
DDR3_DQ[22]	B8	
DDR3_DQ[21]	E5	
DDR3_DQ[20]	F6	
DDR3_DQ[19]	C9	
DDR3_DQ[18]	E9	
DDR3_DQ[17]	B6	
DDR3_DQ[16]	C5	
DDR3_DQ[15]	H2	
DDR3_DQ[14]	K2	
DDR3_DQ[13]	T4	
DDR3_DQ[12]	V4	
DDR3_DQ[11]	H4	
DDR3_DQ[10]	K4	
DDR3_DQ[9]	T2	
DDR3_DQ[8]	V2	
DDR3_DQ[7]	AB4	
DDR3_DQ[6]	AA1	
DDR3_DQ[5]	AG3	
DDR3_DQ[4]	AH2	
DDR3_DQ[3]	AA3	
DDR3_DQ[2]	AB2	
DDR3_DQ[1]	AE1	
DDR3_DQ[0]	AG1	
DDR3_DQS_DP[17]	G19	MEM_2_DQS_P<17..0>
DDR3_DQS_DP[16]	H46	
DDR3_DQS_DP[15]	C49	
DDR3_DQS_DP[14]	G43	
DDR3_DQS_DP[13]	C37	
DDR3_DQS_DP[12]	G13	
DDR3_DQS_DP[11]	G7	
DDR3_DQS_DP[10]	R3	
DDR3_DQS_DP[9]	AP4	
DDR3_DQS_DP[8]	C19	
DDR3_DQS_DP[7]	P46	
DDR3_DQS_DP[6]	G49	
DDR3_DQS_DP[5]	C43	
DDR3_DQS_DP[4]	G37	
DDR3_DQS_DP[3]	C13	
DDR3_DQS_DP[2]	C7	
DDR3_DQS_DP[1]	L3	
DDR3_DQS_DP[0]	AC3	
DDR3_DQS_DN[17]	E19	MEM_2_DQS_N<17..0>
DDR3_DQS_DN[16]	K46	
DDR3_DQS_DN[15]	A49	
DDR3_DQS_DN[14]	E43	
DDR3_DQS_DN[13]	A37	
DDR3_DQS_DN[12]	E13	
DDR3_DQS_DN[11]	E7	
DDR3_DQS_DN[10]	P4	
DDR3_DQS_DN[9]	AR3	
DDR3_DQS_DN[8]	A19	
DDR3_DQS_DN[7]	M46	
DDR3_DQS_DN[6]	E49	
DDR3_DQS_DN[5]	A43	
DDR3_DQS_DN[4]	E37	
DDR3_DQS_DN[3]	A13	
DDR3_DQS_DN[2]	A7	
DDR3_DQS_DN[1]	M4	
DDR3_DQS_DN[0]	AD4	
DDR3_MA[17]	G33	MEM_2_MA<17..0>
DDR3_MA[16]	E31	
DDR3_MA[15]	D32	
DDR3_MA[14]	G31	
DDR3_MA[13]	K32	
DDR3_MA[12]	G23	
DDR3_MA[11]	B24	
DDR3_MA[10]	K30	
DDR3_MA[9]	A23	
DDR3_MA[8]	D24	
DDR3_MA[7]	E23	
DDR3_MA[6]	A25	
DDR3_MA[5]	B26	
DDR3_MA[4]	L25	
DDR3_MA[3]	K26	
DDR3_MA[2]	G27	
DDR3_MA[1]	H26	
DDR3_MA[0]	B30	
DDR3_ECC[7]	E20	MEM_2_ECC<7..0>
DDR3_ECC[6]	B20	
DDR3_ECC[5]	E17	
DDR3_ECC[4]	F18	
DDR3_ECC[3]	C21	
DDR3_ECC[2]	E21	
DDR3_ECC[1]	B18	
DDR3_ECC[0]	C17	
DDR3_CKE[3]	L21	NC
DDR3_CKE[2]	K22	NC
DDR3_CKE[1]	H22	MEM_2_CKE<1>
DDR3_CKE[0]	L23	MEM_2_CKE<0>
DDR3_BA[1]	L29	MEM_2_BA<1>
DDR3_BA[0]	D30	MEM_2_BA<0>
DDR3_BG[1]	H24	MEM_2_BG<1>
DDR3_BG[0]	G25	MEM_2_BG<0>
DDR3_ODT[3]	B34	NC
DDR3_ODT[2]	B33	NC
DDR3_ODT[1]	K34	MEM_2_ODT<1>
DDR3_ODT[0]	L31	MEM_2_ODT<0>
DDR3_CID[2]	L33	TP_MEM_2_CID_2
DDR3_PAR	E29	MEM_2_PARITY
DDR3_ACT*	K24	MEM_2_ACT_L
DDR3_ALERT*	E25	MEM_2_ALERT_L
DDR3_CAVREF	R21	PPVREFCA_MEM_2_CPU
DDR3_CS_7*	E36	NC
DDR3_CS_6*	H36	NC
DDR3_CS_5*	A36	NC
DDR3_CS_4*	B36	NC
DDR3_CS_3*	P36	MEM_2_CS_L<3>
DDR3_CS_2*	N36	MEM_2_CS_L<2>
DDR3_CS_1*	H36	MEM_2_CS_L<1>
DDR3_CS_0*	H36	MEM_2_CS_L<0>
DDR3_CLK_DP[3]	B28	NC
DDR3_CLK_DP[2]	D26	NC
DDR3_CLK_DP[1]	H28	MEM_2_CLK_P<1>
DDR3_CLK_DP[0]	L27	MEM_2_CLK_P<0>
DDR3_CLK_DN[3]	D28	NC
DDR3_CLK_DN[2]	E27	NC
DDR3_CLK_DN[1]	G29	MEM_2_CLK_N<1>
DDR3_CLK_DN[0]	K28	MEM_2_CLK_N<0>

BOM_COST_GROUP=CPU & CHIPSET

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CPU MEMORY CHANNEL 2

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OMIT_TABLE

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CRITICAL

MEM_3_DQ<63..0>					
	T48	DDR4_DQ[63]	DDR4_DQS_DP[17]	P16	MEM_3_DQS_P<17..0>
	U47	DDR4_DQ[62]	DDR4_DQS_DP[16]	AA49	
	AB48	DDR4_DQ[61]	DDR4_DQS_DP[15]	W43	
	AC47	DDR4_DQ[60]	DDR4_DQS_DP[14]	K40	
	U49	DDR4_DQ[59]	DDR4_DQS_DP[13]	Y36	
	W49	DDR4_DQ[58]	DDR4_DQS_DP[12]	AB18	
	Y46	DDR4_DQ[57]	DDR4_DQS_DP[11]	N13	
	AB46	DDR4_DQ[56]	DDR4_DQS_DP[10]	N7	
	AB42	DDR4_DQ[55]	DDR4_DQS_DP[9]	AC7	
	AA43	DDR4_DQ[54]	DDR4_DQS_DP[8]	M18	
	T42	DDR4_DQ[53]	DDR4_DQS_DP[7]	W47	
	R43	DDR4_DQ[52]	DDR4_DQS_DP[6]	U41	
	AA41	DDR4_DQ[51]	DDR4_DQS_DP[5]	P40	
	W41	DDR4_DQ[50]	DDR4_DQS_DP[4]	U39	
	T44	DDR4_DQ[49]	DDR4_DQS_DP[3]	W19	
	V44	DDR4_DQ[48]	DDR4_DQS_DP[2]	P12	
	K42	DDR4_DQ[47]	DDR4_DQS_DP[1]	T8	
	J41	DDR4_DQ[46]	DDR4_DQS_DP[0]	AD8	
	N39	DDR4_DQ[45]			
	M38	DDR4_DQ[44]	DDR4_DQS_DN[17]	N17	MEM_3_DQS_N<17..0>
	N41	DDR4_DQ[43]	DDR4_DQS_DN[16]	Y48	
	M42	DDR4_DQ[42]	DDR4_DQS_DN[15]	Y44	
	J39	DDR4_DQ[41]	DDR4_DQS_DN[14]	H40	
	K38	DDR4_DQ[40]	DDR4_DQS_DN[13]	W37	
	AA39	DDR4_DQ[39]	DDR4_DQS_DN[12]	AC19	
	W39	DDR4_DQ[38]	DDR4_DQS_DN[11]	M14	
	T36	DDR4_DQ[37]	DDR4_DQS_DN[10]	L7	
	V36	DDR4_DQ[36]	DDR4_DQS_DN[9]	AB6	
	AB38	DDR4_DQ[35]	DDR4_DQS_DN[8]	L19	
	AA37	DDR4_DQ[34]	DDR4_DQS_DN[7]	V46	
	R37	DDR4_DQ[33]	DDR4_DQS_DN[6]	V42	
	P36	DDR4_DQ[32]	DDR4_DQS_DN[5]	M40	
	AA21	DDR4_DQ[31]	DDR4_DQS_DN[4]	V38	
	AB20	DDR4_DQ[30]	DDR4_DQS_DN[3]	AA19	
	V16	DDR4_DQ[29]	DDR4_DQS_DN[2]	R11	
	W15	DDR4_DQ[28]	DDR4_DQS_DN[1]	P8	
	W21	DDR4_DQ[27]	DDR4_DQS_DN[0]	AE9	
	V20	DDR4_DQ[26]			
	W17	DDR4_DQ[25]	DDR4_MA[17]	U33	MEM_3_MA<17..0>
	AA17	DDR4_DQ[24]	DDR4_MA[16]	T30	
	L11	DDR4_DQ[23]	DDR4_MA[15]	P32	
	N11	DDR4_DQ[22]	DDR4_MA[14]	AB30	
	P14	DDR4_DQ[21]	DDR4_MA[13]	Y32	
	T14	DDR4_DQ[20]	DDR4_MA[12]	T24	
	K12	DDR4_DQ[19]	DDR4_MA[11]	P26	
	L13	DDR4_DQ[18]	DDR4_MA[10]	Y30	
	T12	DDR4_DQ[17]	DDR4_MA[9]	U25	
	U13	DDR4_DQ[16]	DDR4_MA[8]	Y24	
	L9	DDR4_DQ[15]	DDR4_MA[7]	N27	
	K8	DDR4_DQ[14]	DDR4_MA[6]	AB24	
	U7	DDR4_DQ[13]	DDR4_MA[5]	T26	
	T6	DDR4_DQ[12]	DDR4_MA[4]	AC25	
	R9	DDR4_DQ[11]	DDR4_MA[3]	W25	
	N9	DDR4_DQ[10]	DDR4_MA[2]	U27	
	M6	DDR4_DQ[9]	DDR4_MA[1]	Y26	
	P6	DDR4_DQ[8]	DDR4_MA[0]	AB28	
	Y8	DDR4_DQ[7]			MEM_3_ECC<7..0>
	AA7	DDR4_DQ[6]	DDR4_ECC[7]	R19	
	AG7	DDR4_DQ[5]	DDR4_ECC[6]	N19	
	AF8	DDR4_DQ[4]	DDR4_ECC[5]	M16	
	AA9	DDR4_DQ[3]	DDR4_ECC[4]	K16	
	AC9	DDR4_DQ[2]	DDR4_ECC[3]	T18	
	AD6	DDR4_DQ[1]	DDR4_ECC[2]	R17	
	AF6	DDR4_DQ[0]	DDR4_ECC[1]	K18	
			DDR4_ECC[0]	J17	
			DDR4_CKE[3]	N21	NC
			DDR4_CKE[2]	P22	NC
NC	V2	DDR4_CS_7*	DDR4_CKE[1]	W23	MEM_3_CKE<1>
NC	Y2	DDR4_CS_6*	DDR4_CKE[0]	N23	MEM_3_CKE<0>
NC	T2	DDR4_CS_5*			
NC	N2	DDR4_CS_4*			
MEM_3_CS_L<3>	AB2	DDR4_CS_3*	DDR4_BA[1]	W29	MEM_3_BA<1>
MEM_3_CS_L<2>	AC2	DDR4_CS_2*	DDR4_BA[0]	P30	MEM_3_BA<0>
MEM_3_CS_L<1>	W2	DDR4_CS_1*			
MEM_3_CS_L<0>	AC2	DDR4_CS_0*	DDR4_BG[1]	P24	MEM_3_BG<1>
			DDR4_BG[0]	U23	MEM_3_BG<0>
NC	T28	DDR4_CLK_DP[3]			
NC	P28	DDR4_CLK_DP[2]	DDR4_ODT[3]	T34	NC
MEM_3_CLK_P<1>	W27	DDR4_CLK_DP[1]	DDR4_ODT[2]	U31	NC
MEM_3_CLK_P<0>	AB26	DDR4_CLK_DP[0]	DDR4_ODT[1]	AC33	MEM_3_ODT<1>
			DDR4_ODT[0]	AC31	MEM_3_ODT<0>
NC	U29	DDR4_CLK_DN[3]			
NC	N29	DDR4_CLK_DN[2]	DDR4_CID[2]	AB32	TP_MEM_3_CID_2
MEM_3_CLK_N<1>	Y28	DDR4_CLK_DN[1]	DDR4_PAR	W31	MEM_3_PARITY
MEM_3_CLK_N<0>	AC27	DDR4_CLK_DN[0]	DDR4_ACT*	E22	MEM_3_ACT_L
			DDR4_ALERT*	N25	MEM_3_ALERT_L
			DDR4_CAVREF	AA23	PPVREFCA_MEM_3_CPU

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CPU MEMORY CHANNEL 3

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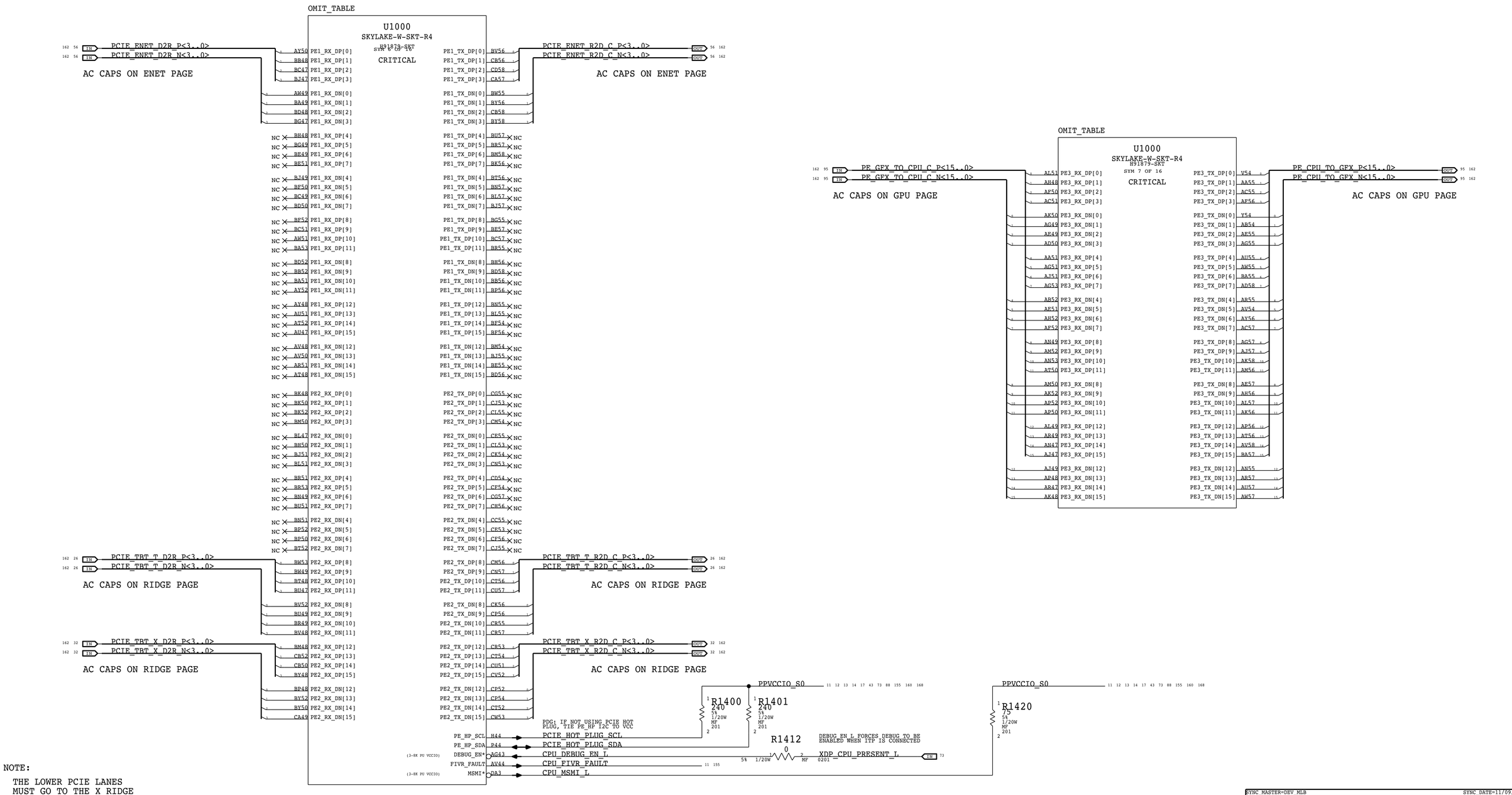

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CPU PCIE

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OMIT_TABLE

U1000
SKYLAKE-W-SKT-R4
SYMB_8x_OF_16
BGA1879-SKT
CRITICAL

PER PEDG 12.1.4, BPM
BPM NETS CAN BE NC IF NOT USED

TP_CPU_BPM_L<7>	AE46	BPM_7*	(IPU VCC)
TP_CPU_BPM_L<6>	AH46	BPM_6*	(IPU VCC)
TP_CPU_BPM_L<5>	AL46	BPM_5*	(IPU VCC)
TP_CPU_BPM_L<4>	AM46	BPM_4*	(IPU VCC)
TP_CPU_BPM_L<3>	AG46	BPM_3*	(IPU VCC)
TP_CPU_BPM_L<2>	AF46	BPM_2*	(IPU VCC)
TP_CPU_BPM_L<1>	AF44	BPM_1*	(IPU VCC)
TP_CPU_BPM_L<0>	AH44	BPM_0*	(IPU VCC)

DMI_SB_TO_CPU_C_P<3>	K50	DMI_RX_DP[3]	
DMI_SB_TO_CPU_C_P<2>	M52	DMI_RX_DP[2]	
DMI_SB_TO_CPU_C_P<1>	K52	DMI_RX_DP[1]	
DMI_SB_TO_CPU_C_P<0>	H54	DMI_RX_DP[0]	
DMI_SB_TO_CPU_C_N<3>	J51	DMI_RX_DN[3]	
DMI_SB_TO_CPU_C_N<2>	L51	DMI_RX_DN[2]	
DMI_SB_TO_CPU_C_N<1>	H52	DMI_RX_DN[1]	
DMI_SB_TO_CPU_C_N<0>	J53	DMI_RX_DN[0]	
DMI_CPU_TO_SB_C_P<3>	J57	DMI_TX_DP[3]	
DMI_CPU_TO_SB_C_P<2>	N55	DMI_TX_DP[2]	
DMI_CPU_TO_SB_C_P<1>	M56	DMI_TX_DP[1]	
DMI_CPU_TO_SB_C_P<0>	U55	DMI_TX_DP[0]	
DMI_CPU_TO_SB_C_N<3>	K56	DMI_TX_DN[3]	
DMI_CPU_TO_SB_C_N<2>	R55	DMI_TX_DN[2]	
DMI_CPU_TO_SB_C_N<1>	L55	DMI_TX_DN[1]	
DMI_CPU_TO_SB_C_N<0>	T54	DMI_TX_DN[0]	

BOOT MODE CONFIGURATION

CPU_DMIMODE_OVERRIDE	BA45	DMIMODE_OVERRIDE	(3-8K PU VCCIO)

PM_FAST_WAKE ENABLES QUICK C3-C6
EXITS OF ALL SOCKETS

PM_FAST_WAKE_L	CR4	PM_FAST_WAKE*	(3-8K PU VCCIO)
PM_SYNC_CLK_R	AR45	PMSYNC_CLK	
PROCID_0	N57	PROC_ID[0]	
PROCID_1	L57	PROC_ID[1]	
TP_CPU_PROCDIS_L	CR36	PROCDIS*	(3-8K PU VCCIO)
XDP_CPU_PWR_DEBUG_L	CA14	PWR_DEBUG*	(IPU VCC)
CPU_RFID_VCC2P5	DA55	RFID_VCC2P5	

RFID_VDD2P5 TIED TO VPP ON REF SCHEM

TEST_15	BT46	CPU_TEST_15	
TEST_14	A29	PD_CPU_TEST14_DDR4TEST	
TEST_13	A31	PD_CPU_TEST13_DDR4TEST	
TEST_12	BD44	CPU_TEST_12	
TEST_11	AW45	CPU_TEST_11	
TEST_10	AY46	CPU_TEST_10	
TEST_9	AU43	CPU_TEST_09	
TEST_8	BM46	CPU_TEST_08	
TEST_7	BF46	CPU_TEST_07	
TEST_6	CH10	CPU_TEST_06	
TEST_5	CE43	CPU_TEST_05	
TEST_4	CM42	CPU_TEST_04	
TEST_3	CN39	CPU_TEST_03	
TEST_2	DP30	PD_CPU_TEST2_DDR4TEST	
TEST_1	DP32	PD_CPU_TEST1_DDR4TEST	
DDR012_DRAM_PWR_OK	CG19	VDDQ_AB_PWRGD_BUFFER	IN
DDR012_RESET*	CP20	DDR_RESET_CPU_CAB_L	OUT
DDR012_SPDSCL	CG15	CPU_DDR_SCL_CAB	OUT
DDR012_SPDSDA	CJ15	CPU_DDR_SDA_CAB	BT
DDR345_DRAM_PWR_OK	L35	VDDQ_CD_PWRGD_BUFFER	IN
DDR345_RESET*	AC23	DDR_RESET_CPU_CCD_L	OUT
DDR345_SPDSCL	K14	CPU_DDR_SCL_CCD	OUT
DDR345_SPDSDA	H14	CPU_DDR_SDA_CCD	BT
ERROR_2*	CM6	CPU_ERROR_L<2>	OUT
ERROR_1*	CV6	CPU_ERROR_L<1>	OUT
ERROR_0*	DB4	CPU_ERROR_L<0>	OUT

DDR[01/23]_DRAM_PWR_OK
FOR BASIN FALLS, PCH NO LONGER DRIVES DRAM PWR OK.
IT IS OPEN DRAIN AND REQUIRES PU, AS WELL AS BUFFER

DRAM_RESET_L
PER PDG 6.17.5, ACTIVE LOW, ASYNCHRONOUS
RESET OUTPUT FROM PROCESSOR TO DIMM

SPD SMBUS
USED FOR INTERFACING DIMM SERIAL PRESENCE DETECT
CAN BE LEFT UNCONNECTED

66 IN PM_SYNC_CLK — R1596 0 0% 1/16W MTL-FILM0402

PROCID[0,1] ARE PACKAGE SIGNALS ONLY

168 161 90 19 18 17 PPVPP01_S3 — R1597 0 0% 1/16W MTL-FILM0402

OMIT_TABLE

U1000
SKYLAKE-W-SKT-R4
SYMB_8x_OF_16
BGA1879-SKT
CRITICAL

NC	A5	RSVD	CF12	NC
NC	A53		CH12	NC
NC	AA57		CM58	NC
NC	AB44		CN35	NC
NC	AE47		CP36	NC
NC	AH6		CR37	NC
NC	AH8		CT36	NC
NC	AL53		CU37	NC
NC	AM54		CV10	NC
NC	AP58		CV36	NC
NC	AR43		CW35	NC
NC	AR53		CY56	NC
NC	AU53		CY58	NC
NC	AW43		D56	NC
NC	AW47		DB2	NC
NC	B4		DB56	NC
NC	B54		DB58	NC
NC	BG45		DC55	NC
NC	BH44		DD4	NC
NC	BH46		DD54	NC
NC	BJ45		DE55	NC
NC	BK44		E1	NC
NC	BT2		E3	NC
NC	BU1		E57	NC
NC	BU11		F16	NC
NC	BU13		F58	NC
NC	BU5		G1	NC
NC	BU7		H16	NC
NC	BU9		H18	NC
NC	BV10		H58	NC
NC	BV12		H8	NC
NC	BV4		J35	NC
NC	BV54		J5	NC
NC	BV6		K36	NC
NC	C3		K58	NC
NC	C55		K6	NC
NC	CC1		R57	NC
NC	CC39		V56	NC
NC	CC51		W1	NC
NC	CD40		W5	NC

R2D DMI3 CAPS

DMI_CPU_TO_SB_C_N<0>	C1540	DMI_CPU_TO_SB_N<0>	0.22UF 020t X5R 6.3V 20%
DMI_CPU_TO_SB_C_P<0>	C1541	DMI_CPU_TO_SB_P<0>	0.22UF 020t X5R 6.3V 20%
DMI_CPU_TO_SB_C_N<1>	C1542	DMI_CPU_TO_SB_N<1>	0.22UF 020t X5R 6.3V 20%
DMI_CPU_TO_SB_C_P<1>	C1543	DMI_CPU_TO_SB_P<1>	0.22UF 020t X5R 6.3V 20%
DMI_CPU_TO_SB_C_N<2>	C1544	DMI_CPU_TO_SB_N<2>	0.22UF 020t X5R 6.3V 20%
DMI_CPU_TO_SB_C_P<2>	C1545	DMI_CPU_TO_SB_P<2>	0.22UF 020t X5R 6.3V 20%
DMI_CPU_TO_SB_C_N<3>	C1546	DMI_CPU_TO_SB_N<3>	0.22UF 020t X5R 6.3V 20%
DMI_CPU_TO_SB_C_P<3>	C1547	DMI_CPU_TO_SB_P<3>	0.22UF 020t X5R 6.3V 20%

D2R DMI3 CAPS

DMI_SB_TO_CPU_C_N<0>	C1550	DMI_SB_TO_CPU_N<0>	0.22UF 020t X5R 6.3V 20%
DMI_SB_TO_CPU_C_P<0>	C1551	DMI_SB_TO_CPU_P<0>	0.22UF 020t X5R 6.3V 20%
DMI_SB_TO_CPU_C_N<1>	C1552	DMI_SB_TO_CPU_N<1>	0.22UF 020t X5R 6.3V 20%
DMI_SB_TO_CPU_C_P<1>	C1553	DMI_SB_TO_CPU_P<1>	0.22UF 020t X5R 6.3V 20%
DMI_SB_TO_CPU_C_N<2>	C1554	DMI_SB_TO_CPU_N<2>	0.22UF 020t X5R 6.3V 20%
DMI_SB_TO_CPU_C_P<2>	C1555	DMI_SB_TO_CPU_P<2>	0.22UF 020t X5R 6.3V 20%
DMI_SB_TO_CPU_C_N<3>	C1556	DMI_SB_TO_CPU_N<3>	0.22UF 020t X5R 6.3V 20%
DMI_SB_TO_CPU_C_P<3>	C1557	DMI_SB_TO_CPU_P<3>	0.22UF 020t X5R 6.3V 20%

PULL UPS

PPVCCIO_S0 — 11 12 13 14 17 43 73 88 155 160 168

R1507	75	PM_FAST_WAKE_L	1% 1/16W MF-LF 402
R1508	75	CPU_ERROR_L<2>	1% 1/16W MF-LF 402
R1509	75	CPU_ERROR_L<1>	1% 1/16W MF-LF 402
R1510	75	CPU_ERROR_L<0>	1% 1/16W MF-LF 402

PP3V3_S0 — 117 118 119 120 143 148 151 153 155 156 46 67 49 65 66 68 69 70 78 84 85 88 94 97 98 99 103 105 106 107 108 109 111 112 116 159

R1518	10K	PROCID_0	5% 1/20W MF 201
R1519	10K	PROCID_1	5% 1/20W MF 201

PULL DOWNS

R1565	NOSTUFF 0	PROCID_0	5% 1/20W MF 201
R1564	NOSTUFF 0	PROCID_1	5% 1/20W MF 201
R1563	49.9	PD_CPU_TEST1_DDR4TEST	1% 1/16W MF-LF 402
R1562	49.9	PD_CPU_TEST2_DDR4TEST	1% 1/16W MF-LF 402
R1561	49.9	PD_CPU_TEST13_DDR4TEST	1% 1/16W MF-LF 402
R1560	49.9	PD_CPU_TEST14_DDR4TEST	1% 1/16W MF-LF 402
R1570	49.9	CPU_TEST_15	1% 1/16W MF-LF 402
R1573	49.9	CPU_TEST_12	1% 1/16W MF-LF 402
R1574	NOSTUFF 49.9	CPU_TEST_11	1% 1/16W MF-LF 402
R1575	NOSTUFF 49.9	CPU_TEST_10	1% 1/16W MF-LF 402
R1576	NOSTUFF 49.9	CPU_TEST_09	1% 1/16W MF-LF 402
R1577	NOSTUFF 49.9	CPU_TEST_08	1% 1/16W MF-LF 402
R1578	NOSTUFF 49.9	CPU_TEST_07	1% 1/16W MF-LF 402
R1579	NOSTUFF 49.9	CPU_TEST_06	1% 1/16W MF-LF 402
R1580	NOSTUFF 49.9	CPU_TEST_05	1% 1/16W MF-LF 402
R1581	NOSTUFF 49.9	CPU_TEST_04	1% 1/16W MF-LF 402
R1582	NOSTUFF 49.9	CPU_TEST_03	1% 1/16W MF-LF 402

DMI OVERRIDE STRAP

PPVCCIO_S0 — 11 12 13 14 17 43 73 88 155 160 168

R1599 240 5% 1/16W MF-LF 402

CPU_DMIMODE_OVERRIDE — 12

NOSTUFF

R1598 240 5% 1/16W MF-LF 402

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB — SYNC_DATE=11/06/2016

PAGE TITLE
CPU DMI, MISC

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DRAWING NUMBER	051-01649
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OMIT_TABLE

U1000
SKYLAKE-W-SKT-R4
H91879-SKT
SYM 1 OF 16
CRITICAL

CLK100M_CPU_BCLK_0_P	CD46 BCLK0_DP		
CLK100M_CPU_BCLK_0_N	CC47 BCLK0_DN		
CLK100M_CPU_BCLK_1_P	C53 BCLK1_DP		
CLK100M_CPU_BCLK_1_N	E53 BCLK1_DN		
CLK100M_CPU_BCLK_2_P	E56 BCLK2_DP		
CLK100M_CPU_BCLK_2_N	E55 BCLK2_DN		
CPU_TXT_PLTEN	BN47 TXT_PLTEN	(3-8K PU VCCIO)	
CPU_MCI_FRMAGENT	BB46 FRMAGENT	(3-8K PD VSS)	(3-8K PD VSS)
CPU_TXT_AGENT	BD46 TXT_AGENT	(3-8K PD VSS)	
CPU_BIST_ENABLE	BB44 BIST_ENABLE	(3-8K PU VCCIO)	
CPU_SKTOCC_L	CD28 SKTOCC*		
CPU_CATERR_L	R43 CATERR*		
CPU_SAFE_MODE_BOOT	AV46 SAFE_MODE_BOOT	(3-8K PD VSS)	
XDP_CPU_TDI	AL45 TDI	(3-8K PU VCCIO)	
XDP_CPU_TCK	AD44 TCK	(3-8K PD VSS)	
XDP_CPU_TMS	AJ45 TMS	(3-8K PU VCCIO)	
XDP_CPU_TRST_L	DF18 TRST*	(3-8K PU VCCIO)	
XDP_CPU_TDO	AE43 TDO		
XDP_CPU_PRDY_L	AN43 PRDY*		
XDP_CPU_PREQ_L	AN45 PREQ*		
NC	BE43 KBLX_CFG[0]		
NC	CC45 KBLX_CFG[1]		
NC	BF44 KBLX_CFG[2]		
NC	BC45 KBLX_CFG[3]		
NC	BG43 KBLX_CFG[4]		
NC	CA45 KBLX_CFG[5]		
NC	BL45 KBLX_CFG[6]		
NC	BW45 KBLX_CFG[7]		
NC	BC43 KBLX_CFG[8]		
NC	AY44 KBLX_CFG[9]		
NC	BU45 KBLX_CFG[10]		
NC	BA43 KBLX_CFG[11]		
NC	BN45 KBLX_CFG[12]		
NC	BJ43 KBLX_CFG[13]		
NC	BP46 KBLX_CFG[14]		
	CH16 MEM_HOT_C0123*		
	N15 MEM_HOT_DDR345*		
	CL3 THERMTRIP*		
	DP48 PROCHOT*		
	BY40 SOCKET_ID[1]	(3-8K PD VSS)	
	CB40 SOCKET_ID[0]	(3-8K PD VSS)	
	DC47 PECI		
	CF18 SVIDCLK[0]		
	CD18 SVIDDATA[0]		
	CE19 SVIDALERT_0*		
	H10 SVIDCLK[1]		
	F10 SVIDDATA[1]		
	H12 SVIDALERT_1*		
	BY46 PMSYNC		
	AM44 PWRGOOD		
	AK42 EAR*	(3-8K PU VCCIO)	
	CW11 RESET*		
	AT44 KBLX_CLK24*		NC
	AL43 KBLX_PM_DOWN		
	AK44 KBLX_PROC_TRIGIN		NC
	AJ43 KBLX_PROC_TRIGOUT		NC
	CU11 KBLX_THERMADA0		NC
	V10 KBLX_THERMADA1		NC
	CV12 KBLX_THERMADC0		NC
	W11 KBLX_THERMADC1		NC
	R51 KBLX_VCCPLL		NC
	V52 KBLX_VCCPLL_OC		NC
	T52 KBLX_VCCST		NC
	U51 KBLX_VCCST		NC
	P50 KBLX_VCCST_PWRGD		NC

SKTOCC INDICATES A PROCESSOR IS PRESENT
PULLED TO GND ON PROCESSOR PACKAGE

INDICATES CATASTROPHIC ERROR
AND MACHINE CANNOT CONTINUE TO OPERATE

KBLX SIGNALS ARE NOT DOCUMENTED IN BASIN FALLS PDG 0.7 / EDS 1.5
BUT PER SRINI EMAIL ON 09/28/16, ARE NC FOR SKL-W

MEM HOT CAN BE INPUT OR OUTPUT
WE WILL USE AS INPUT. CRB TIES THEM TOGETHER

BDIRECTIONAL PROCHOT RESPONSE IS 3MS
FAST PROCHOT (CPU INPUT ONLY) IS 80 MS
WE ARE USING FAST PROCHOT

PER PDG 0.7 SECTION 5.9.1, THESE SERIES SVID TERMS NEED TO BE WITHIN 4.5 INCHES OF CPU PIN
HERE IT'S SET TO 1 INCH (25MM) FOR ALL OF THEM

PM DOWN INDICATES PROCESSOR WAKE EVENT TO PCH
INTEL RECOMMENDED WE CONNECT IT <RDAR://30876611>

CPU_THERMTRIP_SKL_CL3_L	PLACE_NEAR=U1000.CL3:5MM	R1679	0	5%	1/16W	MF-LF	402	CPU_THERMTRIP_SKL_L	OUT 13 45
CPU_PROCHOT_SKL_L	PLACE_NEAR=U1000.DP48:5MM	R1613	51	5%	1/20W	MF	201	CPU_PROCHOT_L	IN 13 76 85 155
REG_CPU_SVID_CLK_SKL	PLACE_NEAR=U1000.CF18:25MM	R1672	0	5%	1/16W	MF-LF	402	REG_CPU_SVID_CLK	OUT 13 85 88
REG_CPU_SVID_DATA_SKL	PLACE_NEAR=U1000.CD18:25MM	R1674	0	5%	1/16W	MF-LF	402	REG_CPU_SVID_DATA	BI 13 85 88
REG_CPU_SVID_ALERT_SKL_L	PLACE_NEAR=U1000.CE19:25MM	R1670	220	5%	1/20W	MF	201	REG_CPU_SVID_ALERT_L	IN 13 85 88
REG_CPU_VDDQ_SVID_CLK_SKL	PLACE_NEAR=U1000.H10:25MM	R1673	0	5%	1/16W	MF-LF	402	REG_CPU_VDDQ_SVID_CLK	OUT 13 92 93
REG_CPU_VDDQ_SVID_DATA_SKL	PLACE_NEAR=U1000.F10:25MM	R1675	0	5%	1/16W	MF-LF	402	REG_CPU_VDDQ_SVID_DATA	BI 13 92 93
REG_CPU_VDDQ_SVID_ALERT_SKL_L	PLACE_NEAR=U1000.H12:25MM	R1671	220	5%	1/20W	MF	201	REG_CPU_VDDQ_SVID_ALERT_L	IN 13 92 93

NOSTUFF
R1698 33 5% 1/20W MF 201

NOSTUFF
R1699 1K 5% 1/20W MF 201

PPVCCIO PIN STRAPS

PPVCCIO_S0 11 12 13 14 17 43 73 88 155 160 168

R1600	240	1/16W 1% MF 0402	
R1601	240	1/16W 1% MF 0402	NOSTUFF
R1602	240	1/16W 1% MF 0402	
R1603	240	1/16W 1% MF 0402	NOSTUFF
R1604	240	1/16W 1% MF 0402	
R1605	240	1/16W 1% MF 0402	
R1606	240	1/16W 1% MF 0402	NOSTUFF
R1620	240	1/16W 1% MF 0402	NOSTUFF — CPU_TXT_PLTEN
R1621	240	1/16W 1% MF 0402	CPU_MCI_FRMAGENT
R1622	240	1/16W 1% MF 0402	NOSTUFF — CPU_TXT_AGENT
R1623	240	1/16W 1% MF 0402	CPU_BIST_ENABLE
R1624	240	1/16W 1% MF 0402	NOSTUFF — SOCKET_ID_1
R1625	240	1/16W 1% MF 0402	NOSTUFF — SOCKET_ID_0
R1626	240	1/16W 1% MF 0402	CPU_EAR_L

TXT_PLTEN
0: PLATFORM IS NOT INTEL TXT ENABLED
1: PLATFORM IS INTEL TXT ENABLED

FRMAGENT
USED WITH SOCKET ID TO DETERMINTE
LEGACY SOCKET STATUS, BOOT FLASH PRESENCE, DMI3 MODE

TXT_AGENT
0: TXT
1: INDICATES INTEL TXT FOR SERVERS IS ENABLED ON THE PLATFORM

BIST_ENABLE
0: CPU WILL NOT EXECTURE LLC AND MLC BIST
1: CPU WILL EXECUTE LLC AND MLC BIST

SOCKET_ID_1	SOCKET_ID_0	PECI ADDRESS
GND	GND	0X30
GND	VTT	0X31
VTT	GND	0X32
VTT	VTT	0X33

EAR* IS USED TO BRING UP THE PROCESSOR IN A DETERMINISTIC STATE

PP3V3_S5	11 43 54 67 68 70 72 73 76 77 78 105 145 153 156 159							
R1653	10K	5% 1/20W MF 201	CPU_SKTOCC_L	13 17				
PP1V0_S0	45 74 76 159							
R1652	75	1% 1/16W MF-LF 402	CPU_PROCHOT_L	13 76 85 155				
PPVCCIO_S0	11 12 13 14 17 43 73 88 155 160 168							
R1650	150	5% 1/16W MF-LF 402	MEM_HOT_ABCD_L	13 18 19 20 21				
R1651	75	1% 1/16W MF-LF 402	NOSTUFF	CPU_THERMTRIP_SKL_L	13 45			
R1654	10K	5% 1/20W MF 201	CPU_RESET_L	13 67				
R1655	51	5% 1/20W MF 201	PLACE_NEAR=R1670.2:5.08MM	REG_CPU_SVID_ALERT_L	13 85 88			
R1656	51	5% 1/20W MF 201	PLACE_NEAR=R1671.2:5.08MM	REG_CPU_VDDQ_SVID_ALERT_L	13 92 93			
R1657	51	5% 1/20W MF 201	PLACE_NEAR=R9414.2:5.08MM	REG_CPU_SVID_CLK	13 85 88			
R1658	51	5% 1/20W MF 201	PLACE_NEAR=R9814.2:5.08MM	REG_CPU_VDDQ_SVID_CLK	13 92 93			
R1659	100	5% 1/20W MF 201	PLACE_NEAR=R1674.2:5.08MM	REG_CPU_SVID_DATA	13 85 88			
R1660	100	5% 1/20W MF 201	PLACE_NEAR=R9415.2:5.08MM	REG_CPU_SVID_DATA	13 85 88			
R1661	100	5% 1/20W MF 201	PLACE_NEAR=R1675.2:25.4MM	REG_CPU_VDDQ_SVID_DATA	13 92 93			
R1662	100	5% 1/20W MF 201	PLACE_NEAR=R9815.2:25.4MM	REG_CPU_VDDQ_SVID_DATA	13 92 93			

PER PDG 0.7 SECTION 5.9.1, THESE PULL UPS SHOULD BE WITHIN 0.2 OR 1 INCH OF THE RELEVANT SERIES TERM
HERE IT'S SET 0.2 INCH (0.508MM) FOR ALL OF THEM

SVID PULL UP BYPASS CAPS

PPVCCIO_S0 11 12 13 14 17 43 73 88 155 160 168

C1680	PLACE_NEAR=R1672:5MM	0.1UF 10% 6.3V X6S 0201
C1681	PLACE_NEAR=C1680:5MM	10UF 20% 6.3V CERM-X6S 0402
C1684	PLACE_NEAR=R9414:5MM	0.1UF 10% 6.3V X6S 0201
C1685	PLACE_NEAR=C1684:5MM	10UF 20% 6.3V CERM-X6S 0402
C1690	PLACE_NEAR=R1673:5MM	0.1UF 10% 6.3V X6S 0201
C1691	PLACE_NEAR=C1690:5MM	10UF 20% 6.3V CERM-X6S 0402
C1692	PLACE_NEAR=R9814:5MM	0.1UF 10% 6.3V X6S 0201
C1693	PLACE_NEAR=C1692:5MM	10UF 20% 6.3V CERM-X6S 0402

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB SYNC_DATE=11/07/2016

PAGE TITLE
CPU SVID, BCLK, JTAG

Apple Inc.

DRAWING NUMBER 051-01649 SIZE D
REVISION 6.21.0
BRANCH
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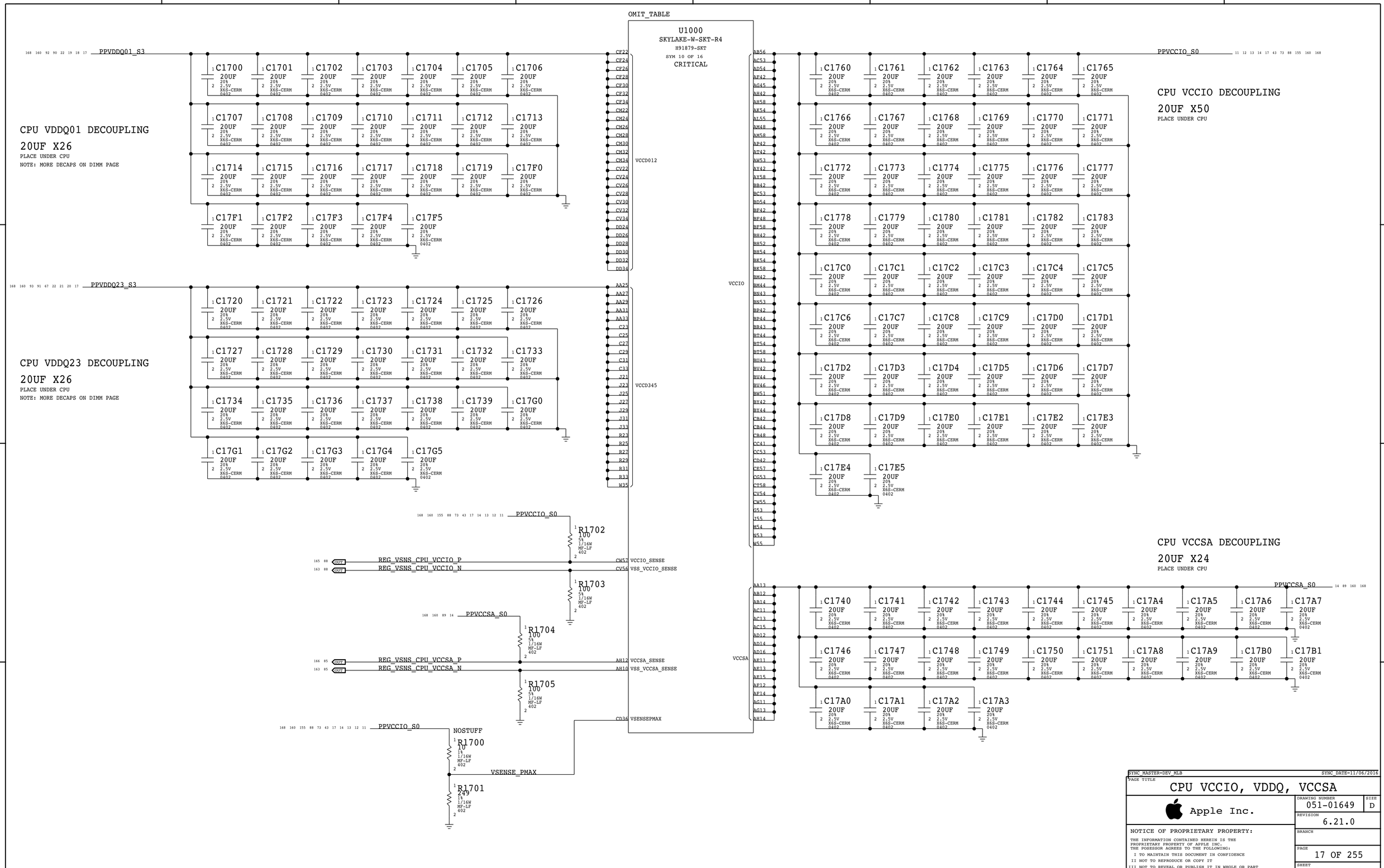

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE
CPU VCCIO, VDDQ, VCCSA

Apple Inc.

DRAWING NUMBER 051-01649 SIZE D

REVISION 6.21.0

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CPU VCORE DECOUPLING

20UF X130

PLACE UNDER CPU

PPVCCIN_S0 15 86 87 151 159 161 168

C1800 C1801 C1802 C1803 C1804 C1805 C1806 C1807 C1808 C1809
C1810 C1811 C1812 C1813 C1814 C1815 C1816 C1817 C1818 C1819
C1820 C1821 C1822 C1823 C1824 C1825 C1826 C1827 C1828 C1829
C1830 C1831 C1832 C1833 C1834 C1835 C1836 C1837 C1838 C1839
C1840 C1841 C1842 C1843 C1844 C1845 C1846 C1847 C1848 C1849
C1850 C1851 C1852 C1853 C1854 C1855 C1856 C1857 C1858 C1859
C1860 C1861 C1862 C1863 C1864 C1865 C1866 C1867 C1868 C1869
C1870 C1871 C1872 C1873 C1874 C1875 C1876 C1877 C1878 C1879
C1880 C1881 C1882 C1883 C1884 C1885 C1886 C1887 C1888 C1889
C1890 C1891 C1892 C1893 C1894 C1895 C1896 C1897 C1898 C1899
C18A0 C18A1 C18A2 C18A3 C18A4 C18A5 C18A6 C18A7 C18A8 C18A9
C18B0 C18B1 C18B2 C18B3 C18B4 C18B5 C18B6 C18B7 C18B8 C18B9
C18C0 C18C1 C18C2 C18C3 C18C4 C18C5 C18C6 C18C7 C18C8 C18C9

20% 2.5V X6S-CERM 0402

OMIT_TABLE

U1000
SKYLAKE-W-SKT-R4
SYM 11 OF 16
H91879-SKT
CRITICAL

VCCIN

OMIT_TABLE

U1000
SKYLAKE-W-SKT-R4
SYM 12 OF 16
H91879-SKT
CRITICAL

VCCIN

VCCIN_SENSE BP2 — REG_VSNS_CPU_VCCIN_P — IN 85 165
VSS_VCCIN_SENSE BR1 — REG_VSNS_CPU_VCCIN_N — IN 85 163
VCCINPMAX BW1 BA1 — VCCINPMAX

PPVCCIN_S0 15 86 87 151 159 161 168

R1802 100K 5% 1/16W MF-LF 402

R1800 1U0 5% 1/16W MF-LP 402

R1801 1U0 5% 1/16W MF-LP 402

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

CPU VCCIN

Apple Inc.

DRAWING NUMBER 051-01649 SIZE D

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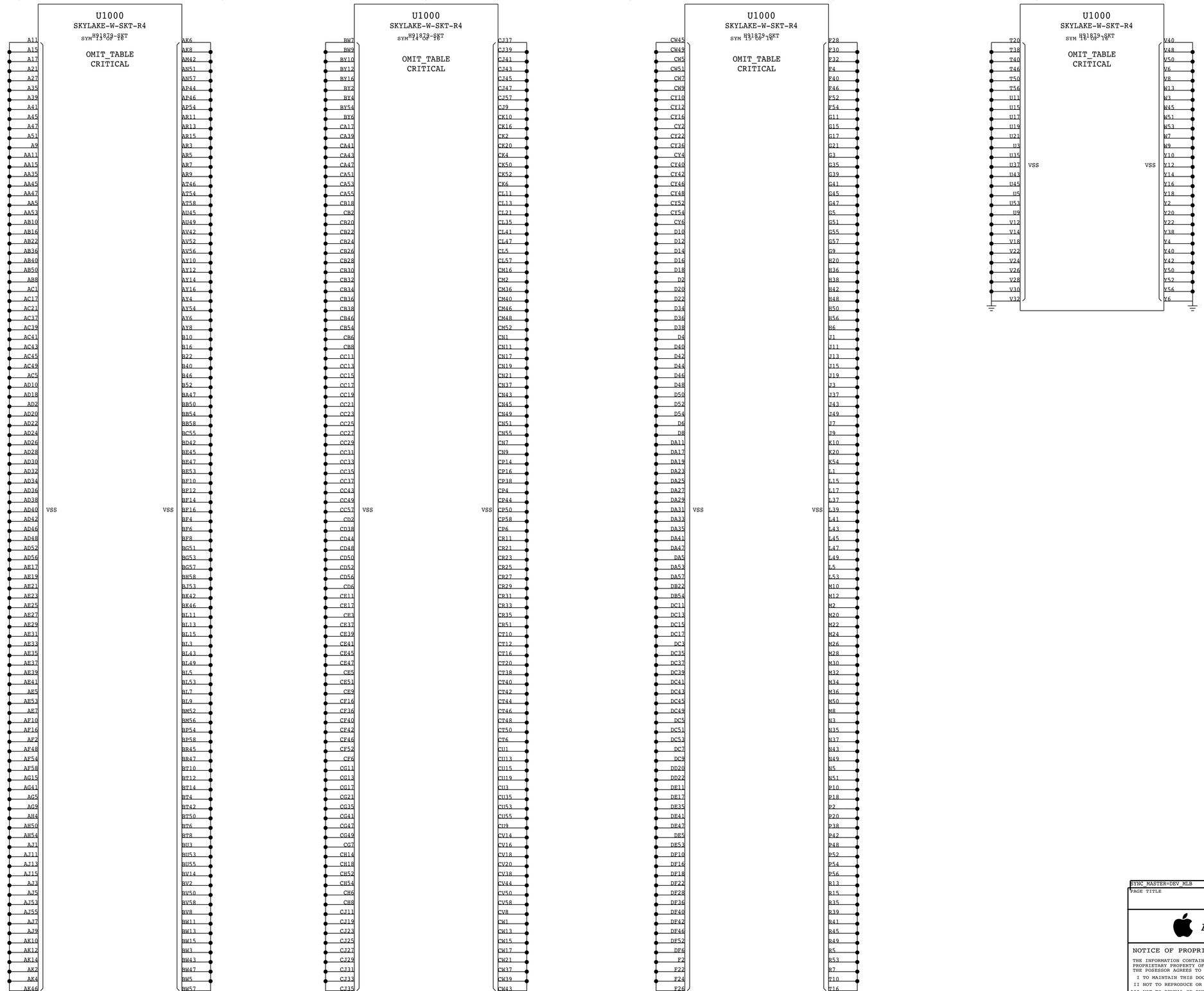

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

CPU GND

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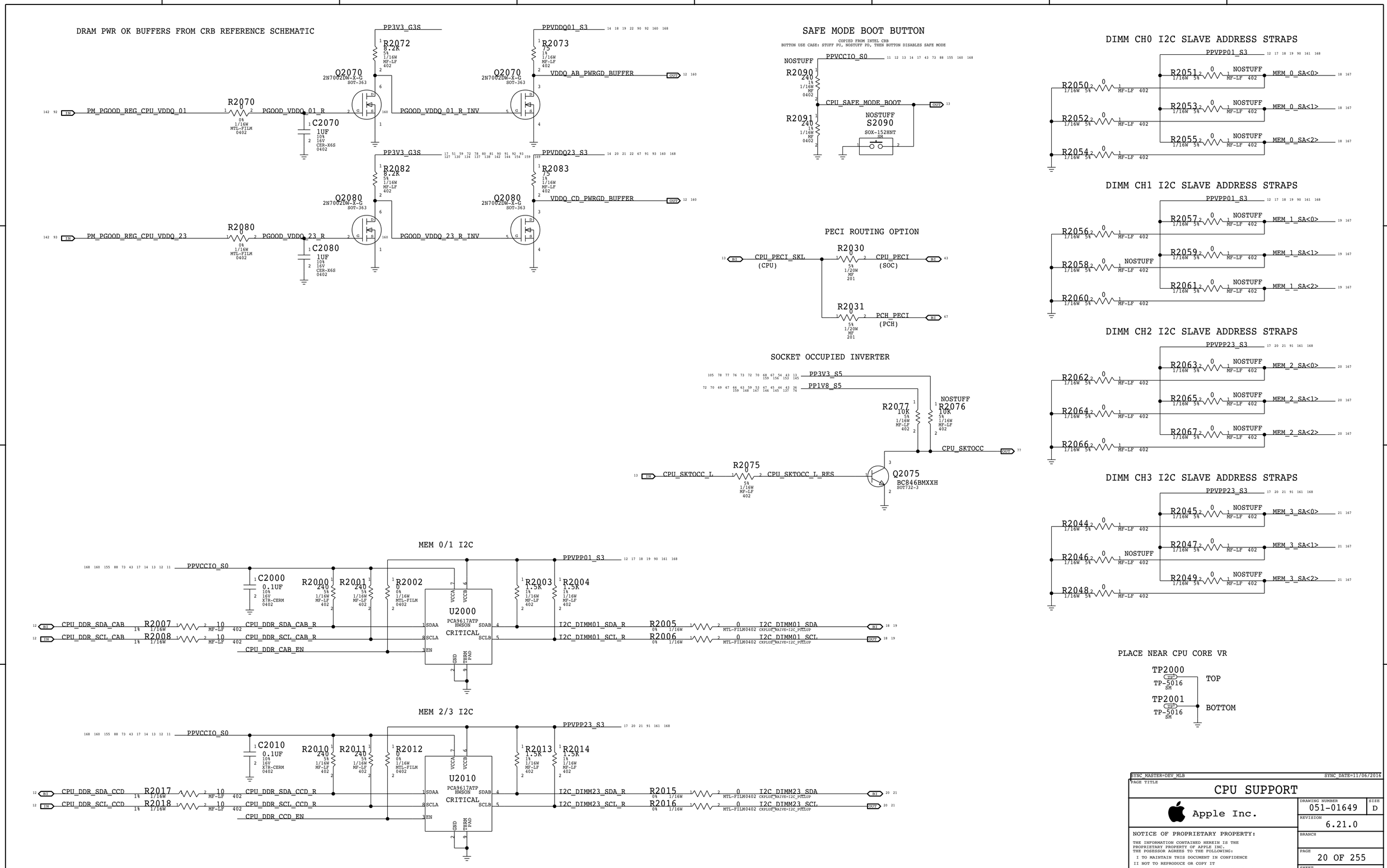
DRAM PWR OK BUFFERS FROM CRB REFERENCE SCHEMATIC
PP3V3_G3S
PPVDDQ01_S3
R2072 8.2K 5% 1/16W MF-LF 402
R2073 75 1% 1/16W MF-LF 402
Q2070 2N7002DW-X-G SOT-363
VDDQ_AB_PWRGD_BUFFER
PM_PGOOD_REG_CPU_VDDQ_01
R2070 0 1/16W MTL-FILM 0402
PGOOD_VDDQ_01_R
C2070 1UF 10% 16V CER-X6S 0402
PGOOD_VDDQ_01_R_INV
PP3V3_G3S
PPVDDQ23_S3
R2082 8.2K 5% 1/16W MF-LF 402
R2083 75 1% 1/16W MF-LF 402
Q2080 2N7002DW-X-G SOT-363
VDDQ_CD_PWRGD_BUFFER
PM_PGOOD_REG_CPU_VDDQ_23
R2080 0 1/16W MTL-FILM 0402
PGOOD_VDDQ_23_R
C2080 1UF 10% 16V CER-X6S 0402
PGOOD_VDDQ_23_R_INV
SAFE MODE BOOT BUTTON
COPIED FROM INTEL CRB
BUTTON USE CASE: STUFF PU, NOSTUFF PD, THEN BUTTON DISABLES SAFE MODE
NOSTUFF
PPVCCIO_S0
R2090 240 1% 1/16W MF 0402
CPU_SAFE_MODE_BOOT
R2091 240 1% 1/16W MF 0402
NOSTUFF
S2090 SOX-152HNT SM
PECI ROUTING OPTION
CPU_PECI_SKL (CPU)
R2030 0 5% 1/20W MF 201
CPU_PECI (SOC)
R2031 0 5% 1/20W MF 201
PCH_PECI (PCH)
SOCKET OCCUPIED INVERTER
PP3V3_S5
PP1V8_S5
R2077 10K 5% 1/16W MF-LF 402
NOSTUFF
R2076 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
CPU_SKTOCC_L
R2075 0 5% 1/16W MF-LF 402
CPU_SKTOCC_L_RES
Q2075 BC846BMXXH SOT732-3
MEM 0/1 I2C
PPVCCIO_S0
C2000 0.1UF 10% 16V X7R-CERM 0402
R2000 240 5% 1/16W MF-LF 402
R2001 240 5% 1/16W MF-LF 402
R2002 0 0% 1/16W MTL-FILM 0402
PPVPP01_S3
R2003 1.5K 1% 1/16W MF-LF 402
R2004 1.5K 1% 1/16W MF-LF 402
U2000 PCA9617ATP HWSON CRITICAL
CPU_DDR_SDA_CAB
R2007 10 1% 1/16W MF-LF 402
CPU_DDR_SDA_CAB_R
CPU_DDR_SCL_CAB
R2008 10 1% 1/16W MF-LF 402
CPU_DDR_SCL_CAB_R
CPU_DDR_CAB_EN
I2C_DIMM01_SDA_R
R2005 0 0% 1/16W MTL-FILM0402 CKPLUS_WAIVE=I2C_PULLUP
I2C_DIMM01_SDA
I2C_DIMM01_SCL_R
R2006 0 0% 1/16W MTL-FILM0402 CKPLUS_WAIVE=I2C_PULLUP
I2C_DIMM01_SCL
MEM 2/3 I2C
PPVCCIO_S0
C2010 0.1UF 10% 16V X7R-CERM 0402
R2010 240 5% 1/16W MF-LF 402
R2011 240 5% 1/16W MF-LF 402
R2012 0 0% 1/16W MTL-FILM 0402
PPVPP23_S3
R2013 1.5K 1% 1/16W MF-LF 402
R2014 1.5K 1% 1/16W MF-LF 402
U2010 PCA9617ATP HWSON CRITICAL
CPU_DDR_SDA_CCD
R2017 10 1% 1/16W MF-LF 402
CPU_DDR_SDA_CCD_R
CPU_DDR_SCL_CCD
R2018 10 1% 1/16W MF-LF 402
CPU_DDR_SCL_CCD_R
CPU_DDR_CCD_EN
I2C_DIMM23_SDA_R
R2015 0 0% 1/16W MTL-FILM0402 CKPLUS_WAIVE=I2C_PULLUP
I2C_DIMM23_SDA
I2C_DIMM23_SCL_R
R2016 0 0% 1/16W MTL-FILM0402 CKPLUS_WAIVE=I2C_PULLUP
I2C_DIMM23_SCL
DIMM CH0 I2C SLAVE ADDRESS STRAPS
PPVPP01_S3
R2050 0 1/16W 5% MF-LF 402
R2051 0 1/16W 5% MF-LF 402
NOSTUFF
MEM_0_SA<0>
R2052 0 1/16W 5% MF-LF 402
R2053 0 1/16W 5% MF-LF 402
MEM_0_SA<1>
R2054 0 1/16W 5% MF-LF 402
R2055 0 1/16W 5% MF-LF 402
MEM_0_SA<2>
DIMM CH1 I2C SLAVE ADDRESS STRAPS
PPVPP01_S3
R2056 0 1/16W 5% MF-LF 402
R2057 0 1/16W 5% MF-LF 402
NOSTUFF
MEM_1_SA<0>
R2058 0 1/16W 5% MF-LF 402
R2059 0 1/16W 5% MF-LF 402
MEM_1_SA<1>
R2060 0 1/16W 5% MF-LF 402
R2061 0 1/16W 5% MF-LF 402
MEM_1_SA<2>
DIMM CH2 I2C SLAVE ADDRESS STRAPS
PPVPP23_S3
R2062 0 1/16W 5% MF-LF 402
R2063 0 1/16W 5% MF-LF 402
NOSTUFF
MEM_2_SA<0>
R2064 0 1/16W 5% MF-LF 402
R2065 0 1/16W 5% MF-LF 402
MEM_2_SA<1>
R2066 0 1/16W 5% MF-LF 402
R2067 0 1/16W 5% MF-LF 402
MEM_2_SA<2>
DIMM CH3 I2C SLAVE ADDRESS STRAPS
PPVPP23_S3
R2044 0 1/16W 5% MF-LF 402
R2045 0 1/16W 5% MF-LF 402
NOSTUFF
MEM_3_SA<0>
R2046 0 1/16W 5% MF-LF 402
R2047 0 1/16W 5% MF-LF 402
MEM_3_SA<1>
R2048 0 1/16W 5% MF-LF 402
R2049 0 1/16W 5% MF-LF 402
MEM_3_SA<2>
PLACE NEAR CPU CORE VR
TP2000 TP-5016 SM
TOP
TP2001 TP-5016 SM
BOTTOM
BOM_COST_GROUP=CPU & CHIPSET
SYNC_MASTER=DEV_MLB
SYNC_DATE=11/06/2016
PAGE TITLE
CPU SUPPORT
Apple Inc.
DRAWING NUMBER 051-01649
SIZE D
REVISION 6.21.0
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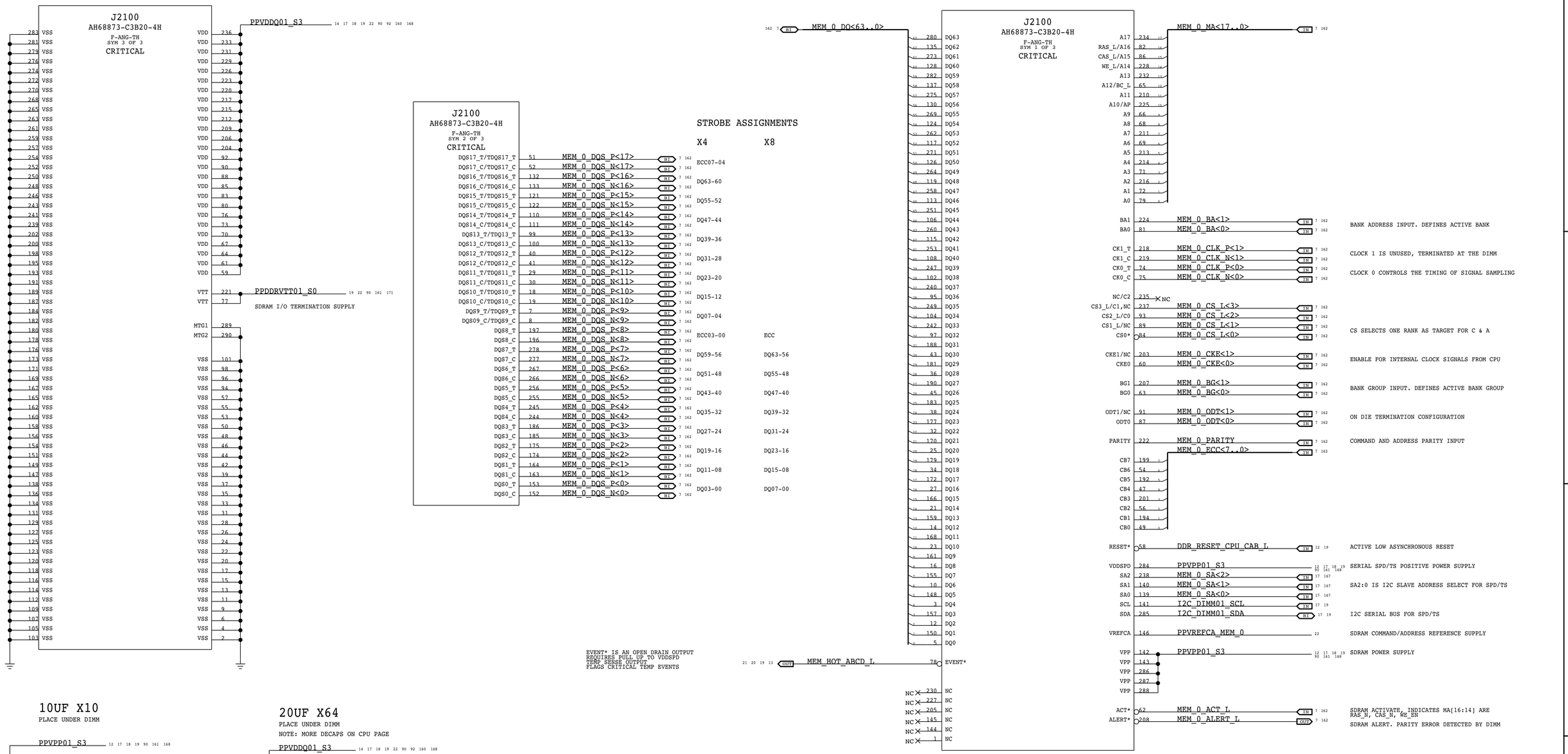

BOM_COST_GROUP=DRAM

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

DDR4 DIMM CONN CH0

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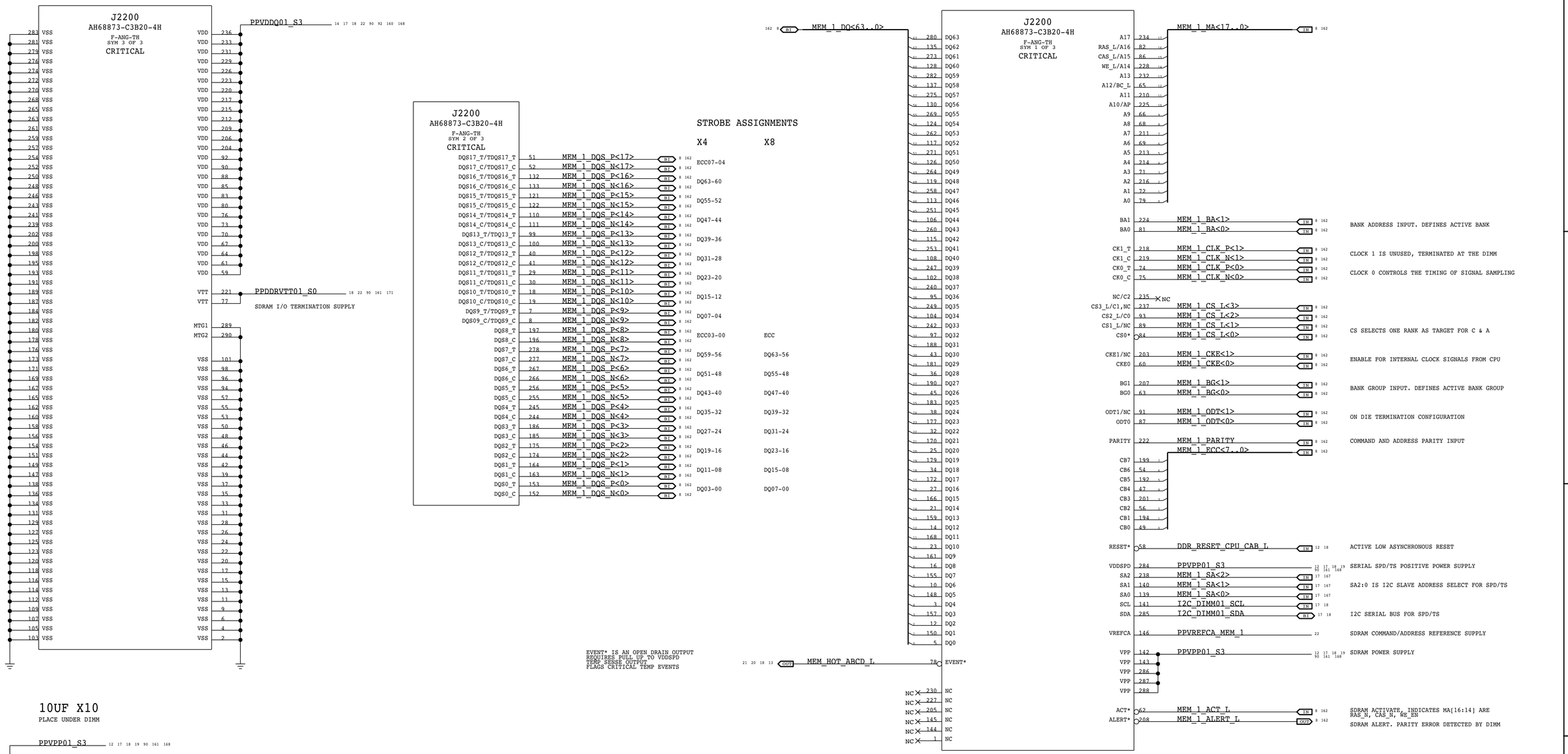

BOM_COST_GROUP=DRAM

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PAGE TITLE

DDR4 DIMM CONN CH1

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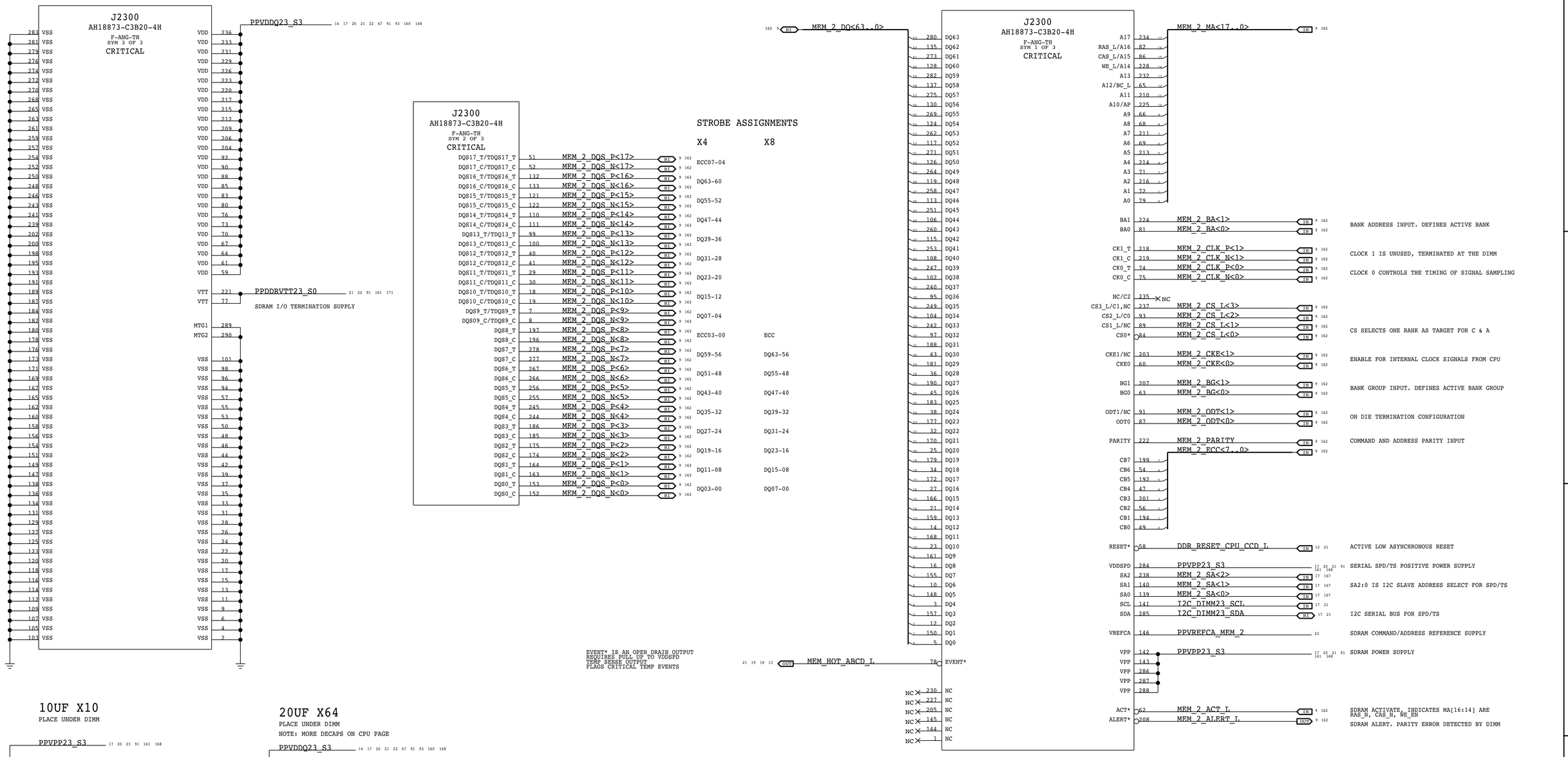

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SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

DDR4 DIMM CONN CH2

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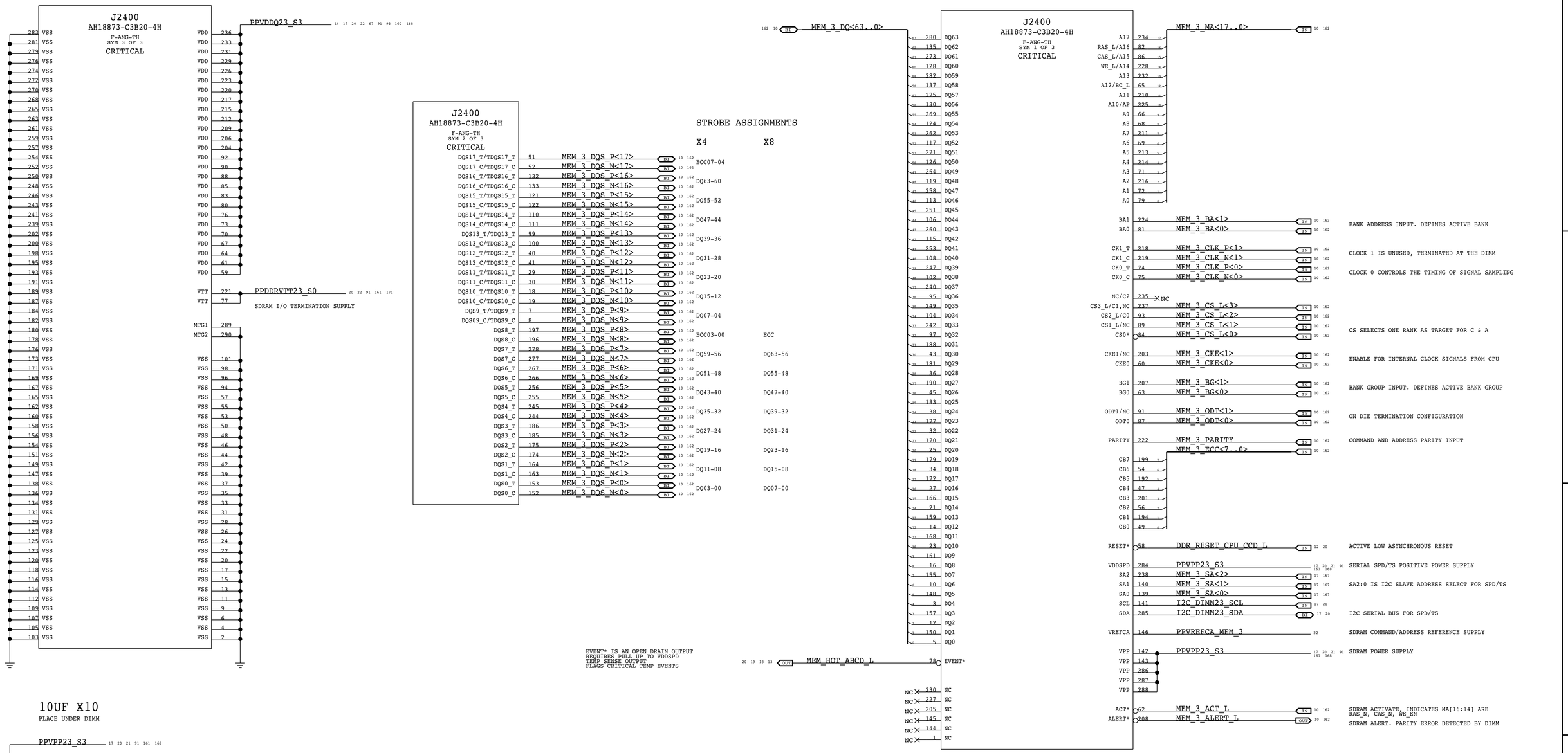

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SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

DDR4 DIMM CONN CH3

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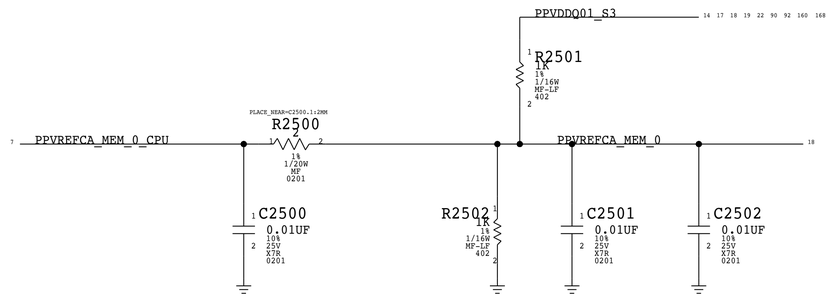
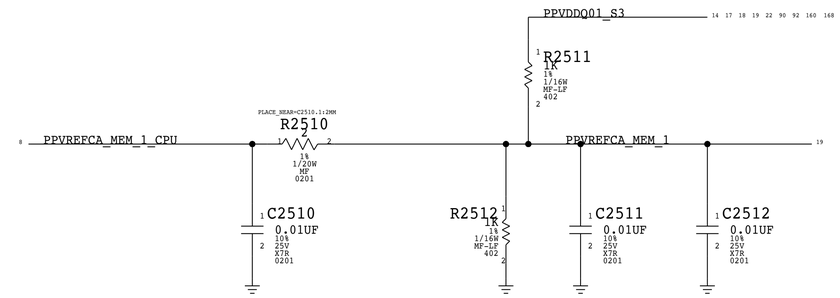
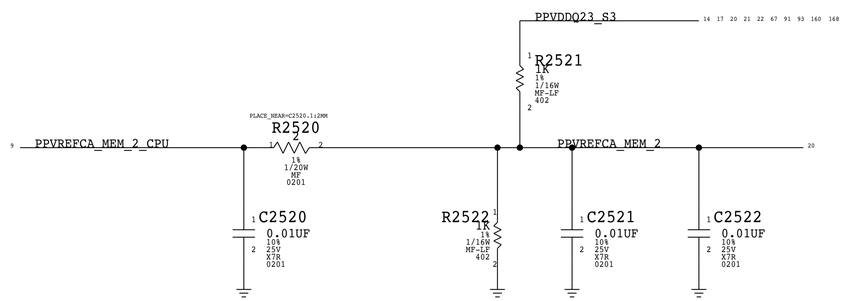
MEM 0 COMMAND AND ADDRESS VREF DIVIDER



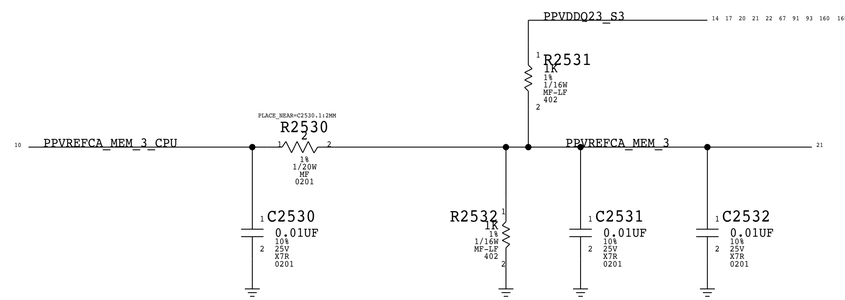
MEM 1 COMMAND AND ADDRESS VREF DIVIDER

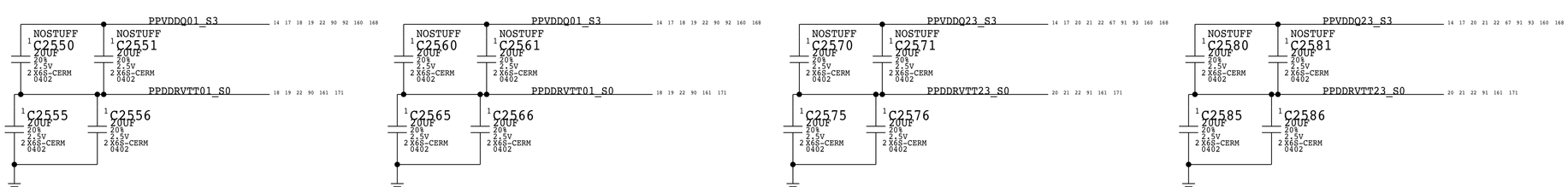


MEM 2 COMMAND AND ADDRESS VREF DIVIDER



MEM 3 COMMAND AND ADDRESS VREF DIVIDER





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SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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DDR4 CA VREF, VTT

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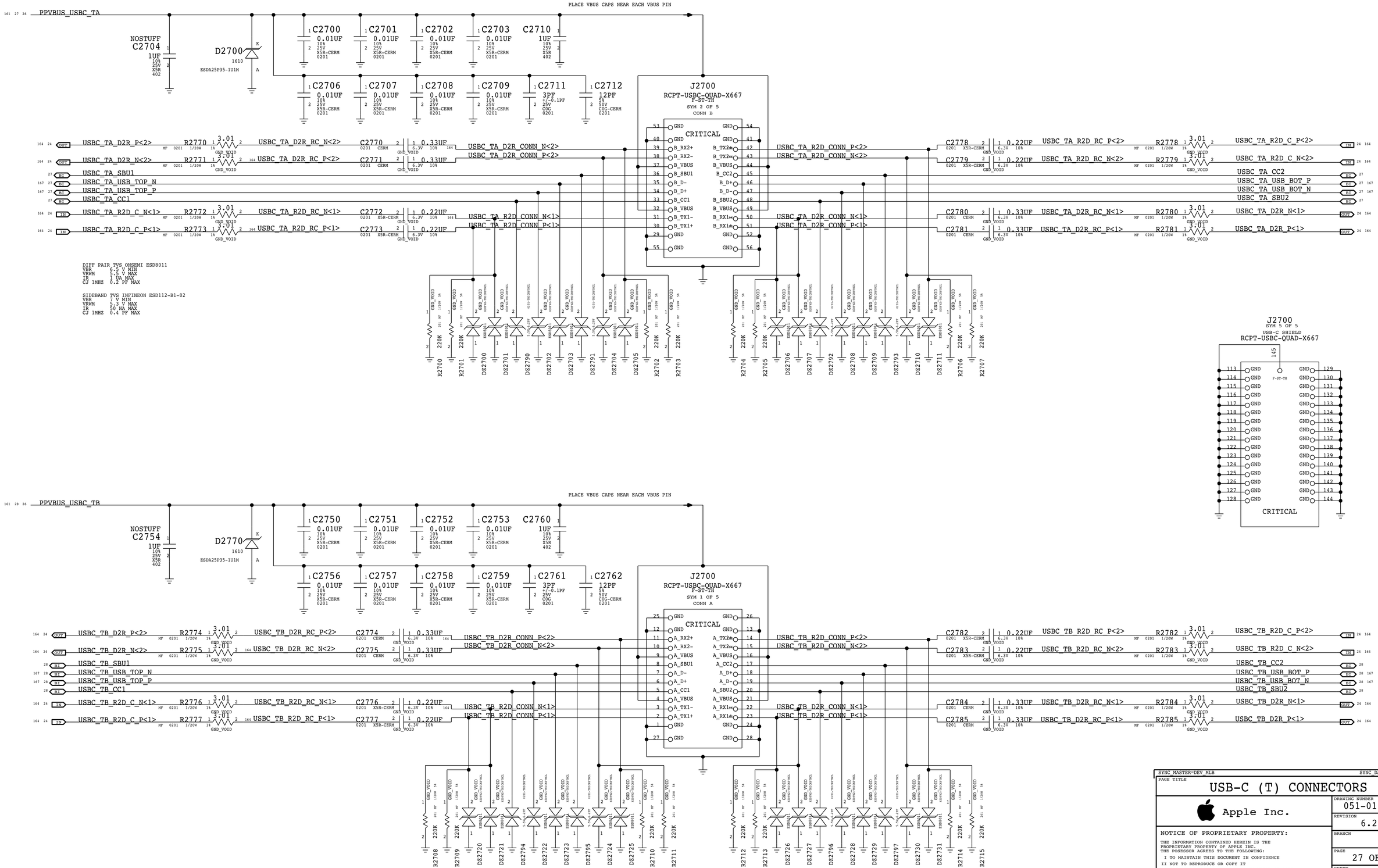
J137 SUPPORTS 5V @ 3A
J137 HAS A QUAD-PACK USB-C CONNECTOR



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PAGE TITLE
USB-C (T) CONNECTORS

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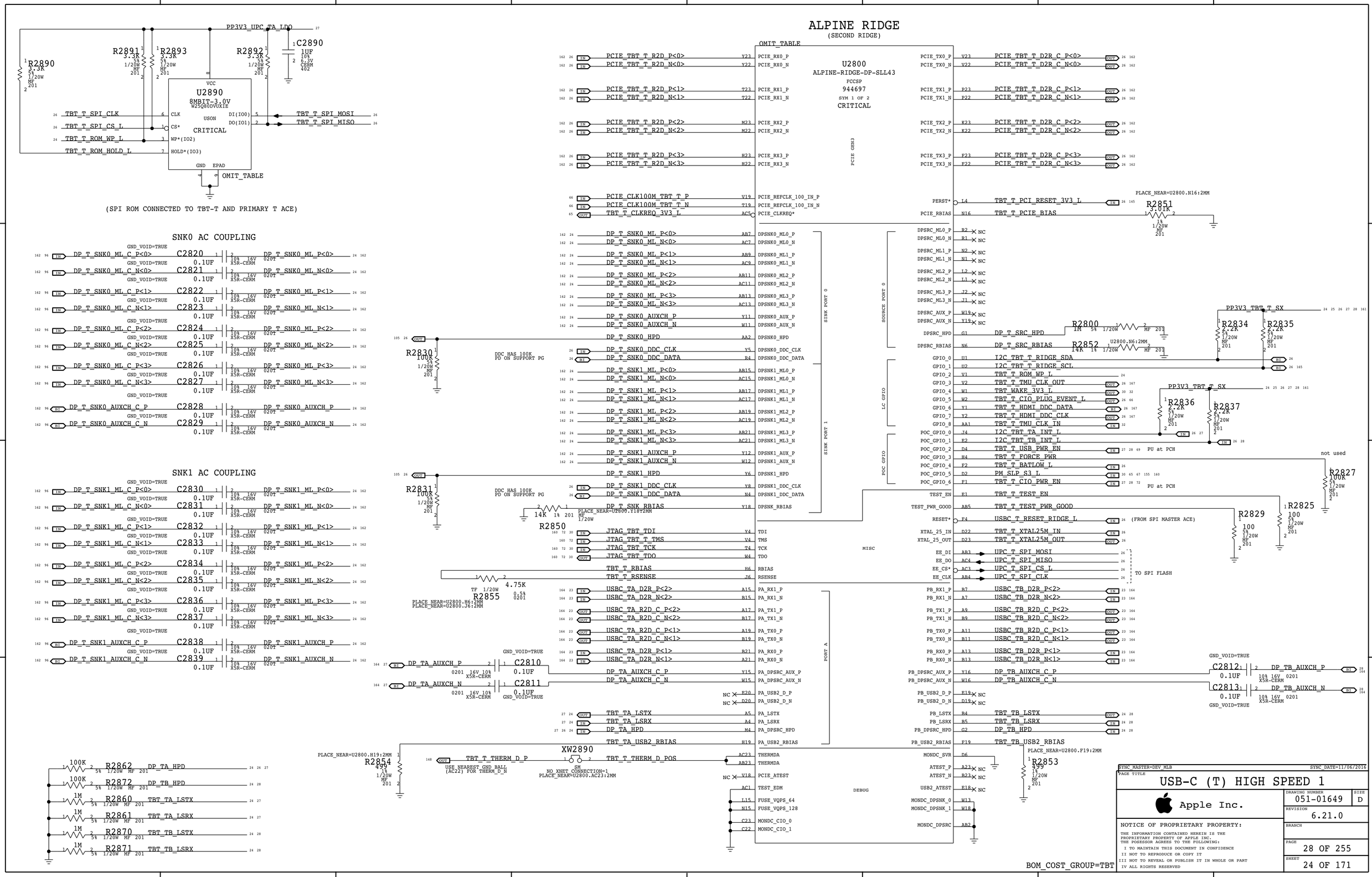
ALPINE RIDGE
(SECOND RIDGE)
U2800
ALPINE-RIDGE-DP-SLL43
FCCSP
944697
SYM 1 OF 2
CRITICAL
OMIT_TABLE
PCIE GEN3
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
LC GPIO
POC GPIO
MISC
PORT A
DEBUG
U2890
8MBIT-3.0V
W25Q80DVUXIE
USON
CRITICAL
VCC
GND EPAD
PP3V3_UPC_TA_LDO
(SPI ROM CONNECTED TO TBT-T AND PRIMARY T ACE)
SNK0 AC COUPLING
SNK1 AC COUPLING
DDC HAS 100K
PD ON SUPPORT PG
PLACE_NEAR=U2800.N16:2MM
PLACE_NEAR=U2800.H6:2MM
PLACE_NEAR=U2800.J6:2MM
PLACE_NEAR=U2800.H19:2MM
PLACE_NEAR=U2800.F19:2MM
PU at PCH
not used
(FROM SPI MASTER ACE)
TO SPI FLASH
USE NEAREST GND BALL
(AC22) FOR THERM_D_N
NO XNET CONNECTION=1
PLACE_NEAR=U2800.AC23:2MM
BOM_COST_GROUP=TBT
SYNC_MASTER=DEV_MLB
SYNC_DATE=11/06/2016
PAGE TITLE
USB-C (T) HIGH SPEED 1
Apple Inc.
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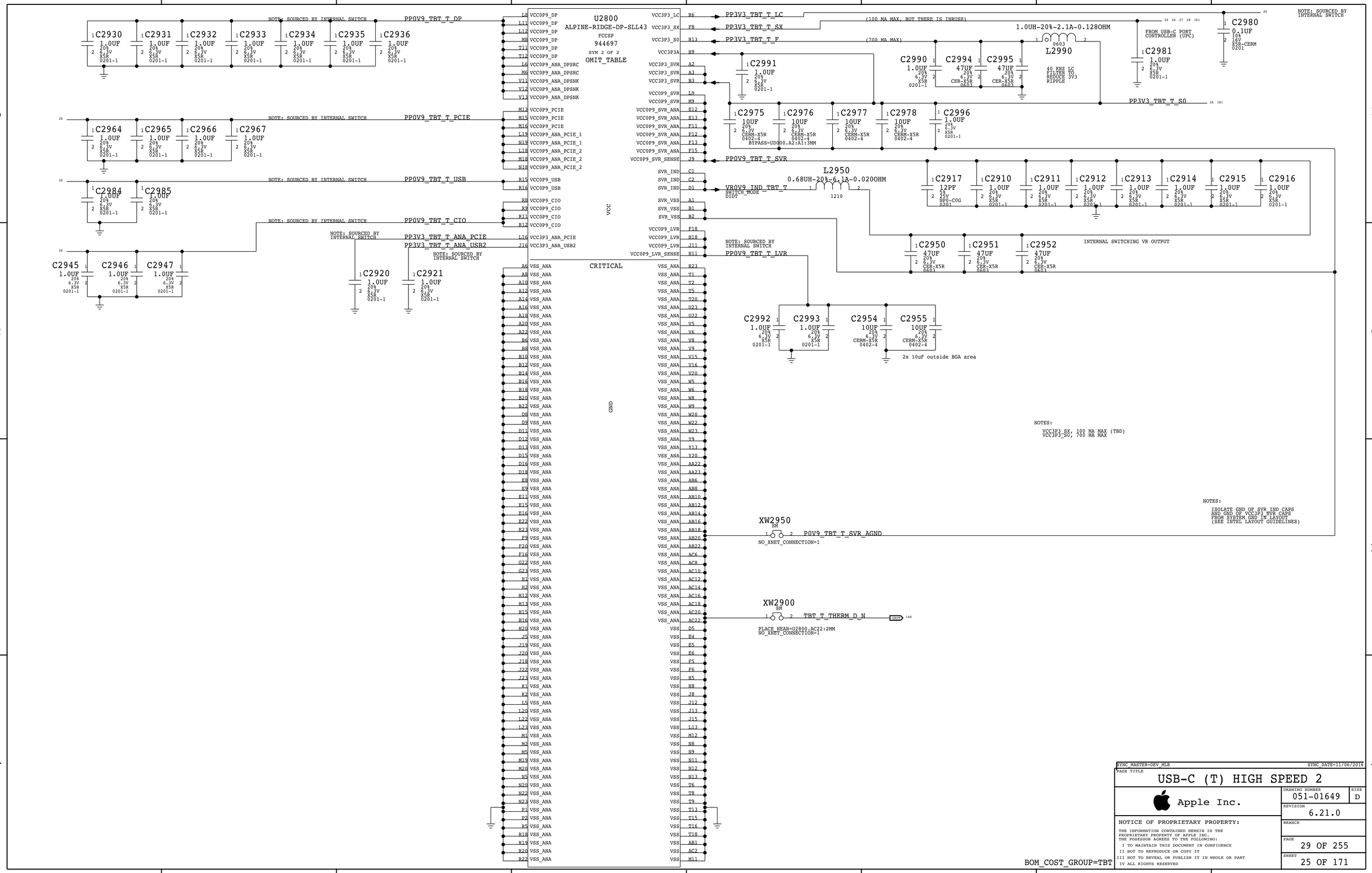

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

USB-C (T) HIGH SPEED 2

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RIDGE TMU CLKS

TO SYNC BETWEEN X AND T RIDGES - NOT USED

NOSTUFF R3000 15 1/20W 5% MF 201

167 24 IN TBT_T_TMU_CLK_OUT — R3000 — TBT_X_TMU_CLK_IN OUT 30

R3071 100K 5% 1/20W MF 201

R3072 100K 5% 1/20W MF 201

RIDGE PULL DOWNS

24	DP_T_SNK0_DDC_CLK	R3067 100K 5% 1/20W MF 201
24	DP_T_SNK0_DDC_DATA	R3068 100K 5% 1/20W MF 201
24	DP_T_SNK1_DDC_CLK	R3069 100K 5% 1/20W MF 201
24	DP_T_SNK1_DDC_DATA	R3070 100K 5% 1/20W MF 201
167 24	TBT_T_HDMI_DDC_DATA	R3076 100K 5% 1/20W MF 201

RIDGE PULL UPS

R3075 100K 201 5% 1/20W MF

24 TBT_T_BATLOW_L — R3075 — PP3V3_TBT_T_SX 24 25 26 27 28 161

R3074 100K 1/20W 201 MF 5%

167 24 TBT_T_HDMI_DDC_CLK — R3074 — PP3V3_TBT_T_LC 25 26

SERIES R FOR RESET

24 OUT USBC_T_RESET_RIDGE_L — R3066 10K 5% 1/20W MF 201 — USBC_T_RESET_L IN 26 27

AR/ACE SPI BUS SERIES R'S

24	TBT_T_SPI_CLK	R3094 1K	TBT_T_SPI_CLK_DBG	26
24	TBT_T_SPI_CS_L	R3095 15	UPC_TA_SPI_CLK	IN 27
24	TBT_T_SPI_MOSI	R3096 15	UPC_TA_SPI_CS_L	IN 27
24	TBT_T_SPI_MISO	R3097 15	UPC_TA_SPI_MOSI	IN 27
		R3098 15	UPC_TA_SPI_MISO	OUT 27
		R3090 15	UPC_T_SPI_CLK	IN 24
		R3091 15	UPC_T_SPI_CS_L	IN 24
		R3092 15	UPC_T_SPI_MOSI	IN 24
		R3093 15	UPC_T_SPI_MISO	OUT 24

Ace

ROM

AR

RIDGE DEBUG CONNECTOR OPTION

105 24 IN DP_T_SNK1_HPD — R3082 0 MF 0201 — ARKANOID_T_P5 26 167

27 26 SMC_DEBUGPRT_USB_RX — R3083 0 MF 0201 — ARKANOID_T_P5

NOSTUFF 5% 1/20W

(IMAC)

27 24 IN DP_TA_HPD — R3084 0 MF 0201 — ARKANOID_T_P7 26 167

27 26 SMC_DEBUGPRT_USB_TX — R3085 0 MF 0201 — ARKANOID_T_P7

NOSTUFF 5% 1/20W

(IMAC)

ALPINE RIDGE ARKANOID DEBUG CONN

PLACE ON BOTTOM
BOM OPTION REMOVED
NO STUFF AT PVT

J3099 516S0115 505070-1220 M-ST-SM

66 24 OUT	TBT_T_CIO_PLUG_EVENT_L	TBT_T_PCI_RESET_3V3_L	24 145
105 24 BI	DP_T_SNK0_HPD	USBC_T_RESET_L BI	24 27
167 26	ARKANOID_T_P5	PP3V3_TBT_T_SX	24 25 26 27 28 161
167 26	ARKANOID_T_P7	PP0V9_TBT_T_PCIE	25
69 34 33 32 28 27 BI	TBT_POC_RESET	PP0V9_TBT_T_USB	25
26 25 IN	PP3V3_TBT_T_LC	PP0V9_TBT_T_CIO	25

ACE ARKANOID DEBUG CONN

PLACE ON BOTTOM
BOM OPTION REMOVED
NO STUFF AT PVT

J3000 516S0115 505070-1220 M-ST-SM

SMBUS 4

28 26 24	I2C_TBT_TB_INT_L	I2C_TBT_TA_INT_L	24 26 27
47 28 27 26	I2C_UPC_T_SCL2	I2C_TBT_T_SDA	26 27 28
47 28 27 26	I2C_UPC_T_SDA2	I2C_TBT_T_SCL	26 27 28
47 36 34 33 32 28 27	UPC_I2C_INT_L	UPC_TA_SWD_DATA	27 166
26	TBT_T_SPI_CLK_DBG	UPC_TA_SWD_CLK	27 166
28 27	UPC_TA_UART_TX	UPC_TA_UART_RX	27 28

RIDGE POWER SENSE RESISTOR

NOTE: FROM LOAD SWITCH BY TBT_PWR_EN
NOTE: THESE 3 CAPS SUPPORT BOTH RIDGES

161 78 69 32 PP3V3_S0_TBT — XW3078 SM — PP3V3_TBT_T_S0 (TO RIDGE T) 25 161

C3080 47UF 20% 6.3V CER-X5R 0603

C3081 47UF 20% 6.3V CER-X5R 0603

C3082 47UF 20% 6.3V CER-X5R 0603

25MHZ XTAL

24 IN TBT_T_XTAL25M_OUT — R3007 0 5% 1/20W MF 201 — TBT_T_XTAL25M_OUT_R PLACE_NEAR=Y3000.3:2MM — C3002 20PF 5% 25V COG 0201 PLACE_NEAR=Y3000.3:2MM

NOSTUFF R3006 1M 5% 1/20W MF 201

TO/FROM RIDGE

Y3000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM

24 OUT TBT_T_XTAL25M_IN — C3003 20PF 5% 25V COG 0201 PLACE_NEAR=Y3000.1:2MM

TA ACE TEST POINTS

TP3020 A	1 TP-P5	SMC_DEBUGPRT_USB_TX	26 27
TP3021 A	1 TP-P5	SMC_DEBUGPRT_USB_RX	26 27

ACE XA AND XB OTP TPS

TP3030 A	1 TP-P5	PPVBUS_USBC_TA	23 27 161
TP3031 A	1 TP-P5	PPVBUS_USBC_TB	23 28 161
TP3032 A	1 TP-P5	I2C_UPC_T_SDA2	26 27 28 47
TP3033 A	1 TP-P5	I2C_UPC_T_SCL2	26 27 28 47

ACE DEBUG SUPPORT (FOR TP)

NOSTUFF R3089 NONE NONE NONE NONE 402

UPC_TA_DEBUGUART_TX 27 166

UPC_TA_GPIO1 27 166

NOSTUFF R3088 NONE NONE NONE NONE 402

UPC_TB_DEBUGUART_TX 28 166

UPC_TB_GPIO1 28 166

TBT TO ACE I2C

TBT-T
RIDGE U2800
MASTER

165 24 IN	I2C_TBT_T_RIDGE_SCL	R3086 33 MF 201 5% 1/20W	I2C_TBT_T_SCL OUT
24 BI	I2C_TBT_T_RIDGE_SDA	R3087 33 MF 201 5% 1/20W	I2C_TBT_T_SDA BI
27 26 24 OUT	I2C_TBT_TA_INT_L		IN (ACE TA I2C_IRQ1_L)
28 26 24 OUT	I2C_TBT_TB_INT_L		(ACE TB I2C_IRQ1_L)

PRI ACE
U3100
WRITE: 0X70 READ: 0X71

SEC ACE
U3200
WRITE: 0X7E READ: 0X7F

OUT 26 27 28
BI 26 27
IN 26 27

BULK CAP FOR BOTH ACES

PP5V_G3S_USBC 27 28 32 33 34 79 159

C3089 220UF-35MOHM 20% 6.3V POLY-TANT CASE-B2-SM1

SOC SMC TO ACE I2C

SEE CSA 51

R2D RIDGE PCIE CAPS

162 11 IN	PCIE_TBT_T_R2D_C_P<0>	C3040 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_R2D_P<0> OUT 24 162
162 11 IN	PCIE_TBT_T_R2D_C_N<0>	C3041 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_R2D_N<0> OUT 24 162
162 11 IN	PCIE_TBT_T_R2D_C_P<1>	C3042 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_R2D_P<1> OUT 24 162
162 11 IN	PCIE_TBT_T_R2D_C_N<1>	C3043 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_R2D_N<1> OUT 24 162
162 11 IN	PCIE_TBT_T_R2D_C_P<2>	C3044 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_R2D_P<2> OUT 24 162
162 11 IN	PCIE_TBT_T_R2D_C_N<2>	C3045 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_R2D_N<2> OUT 24 162
162 11 IN	PCIE_TBT_T_R2D_C_P<3>	C3046 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_R2D_P<3> OUT 24 162
162 11 IN	PCIE_TBT_T_R2D_C_N<3>	C3047 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_R2D_N<3> OUT 24 162

D2R RIDGE PCIE CAPS

162 24 IN	PCIE_TBT_T_D2R_C_P<0>	C3050 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_P<0> OUT 11 162
162 24 IN	PCIE_TBT_T_D2R_C_N<0>	C3051 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_N<0> OUT 11 162
162 24 IN	PCIE_TBT_T_D2R_C_P<1>	C3052 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_P<1> OUT 11 162
162 24 IN	PCIE_TBT_T_D2R_C_N<1>	C3053 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_N<1> OUT 11 162
162 24 IN	PCIE_TBT_T_D2R_C_P<2>	C3054 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_P<2> OUT 11 162
162 24 IN	PCIE_TBT_T_D2R_C_N<2>	C3055 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_N<2> OUT 11 162
162 24 IN	PCIE_TBT_T_D2R_C_P<3>	C3056 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_P<3> OUT 11 162
162 24 IN	PCIE_TBT_T_D2R_C_N<3>	C3057 0.22UF 0201 X5R 6.3V 20%	PCIE_TBT_T_D2R_N<3> OUT 11 162

SMC DEBUG UART ISOLATION

159 123 36 OUT SMC_DEBUGPRT_RX — R3035 0 MF 0201 5% 1/20W PLACE_NEAR=UE560:10MM — SMC_DEBUGPRT_USB_RX IN 26 27

159 123 36 IN SMC_DEBUGPRT_TX — R3036 0 MF 0201 5% 1/20W PLACE_NEAR=UE560:10MM — SMC_DEBUGPRT_USB_TX OUT 26 27

(SMC) (ACE)

BOM_COST_GROUP=USB-C

SYNC_MASTER=DEV_MLB SYNC_DATE=11/07/2016

PAGE TITLE: USB-C (T) SUPPORT

Apple Inc.

DRAWING NUMBER	051-01649
SIZE	D
REVISION	6.21.0
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PAGE	30 OF 255
SHEET	26 OF 171

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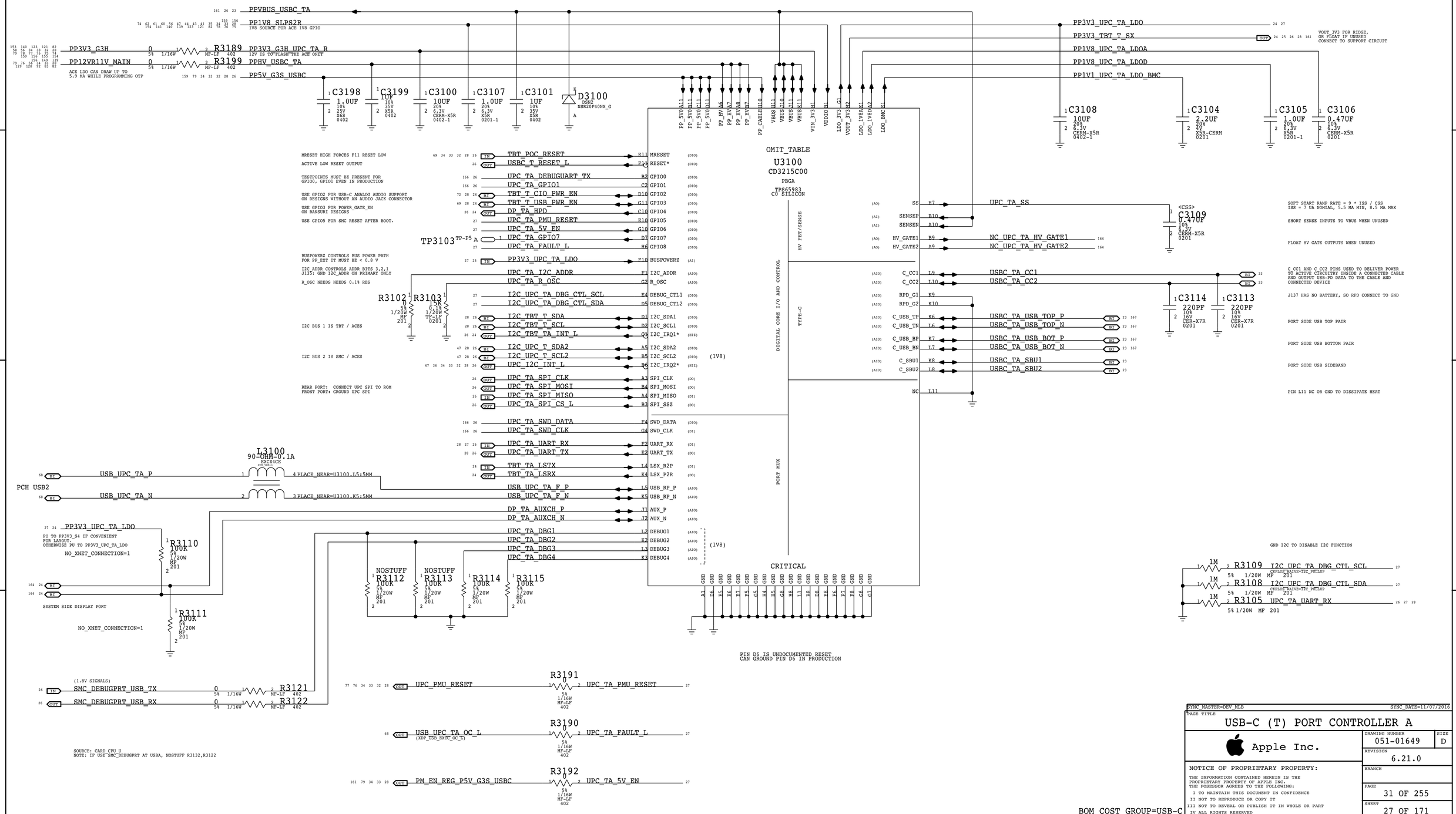
T PRIMARY ACE USB-C PORT CONTROLLER (UPC)



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PAGE TITLE

USB-C (T) PORT CONTROLLER A

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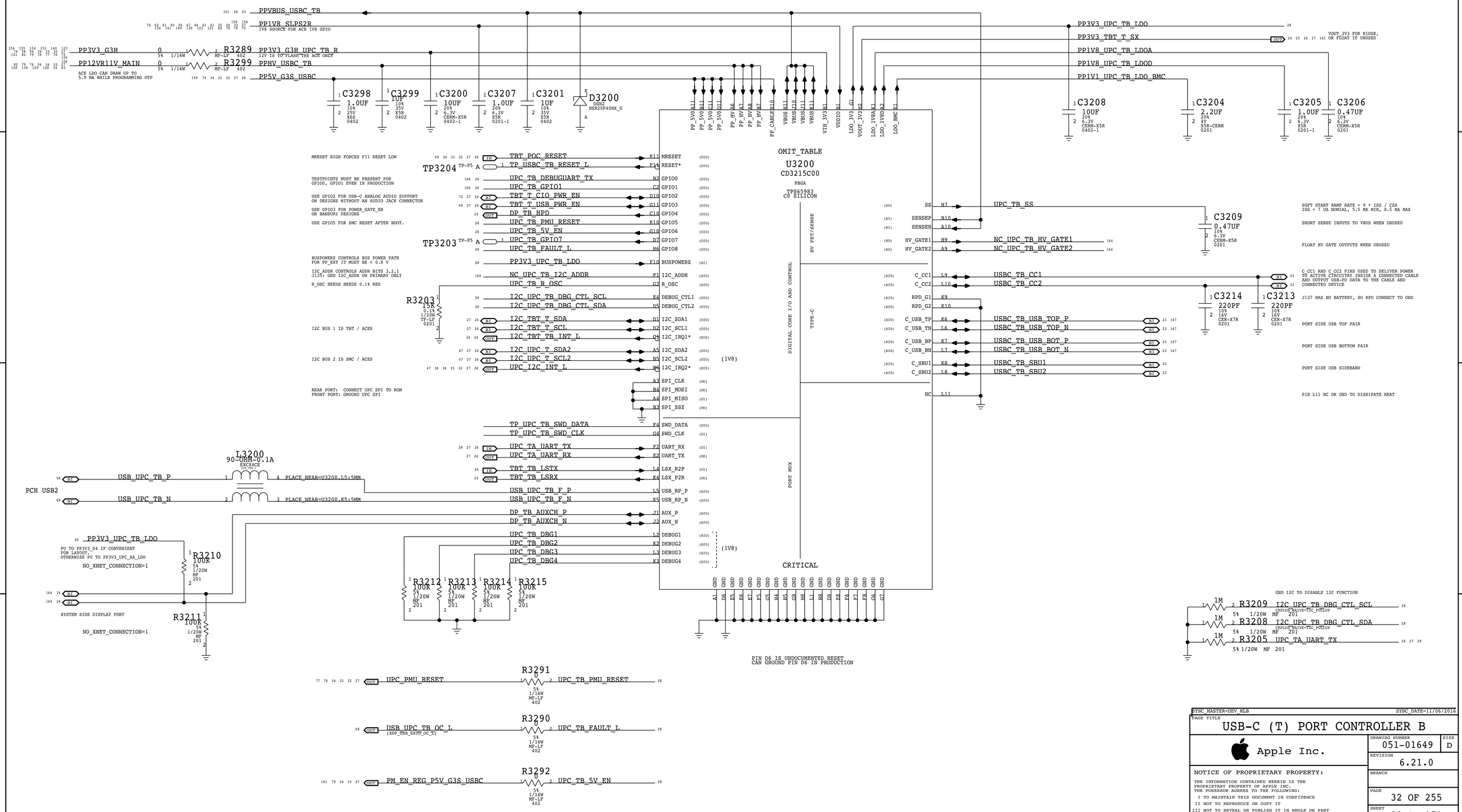
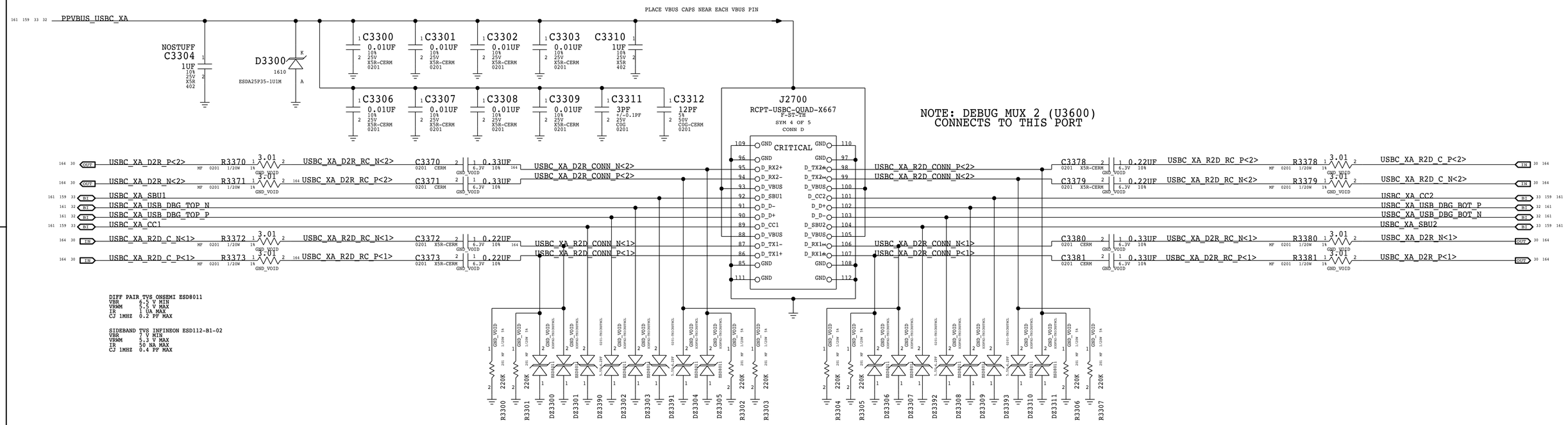
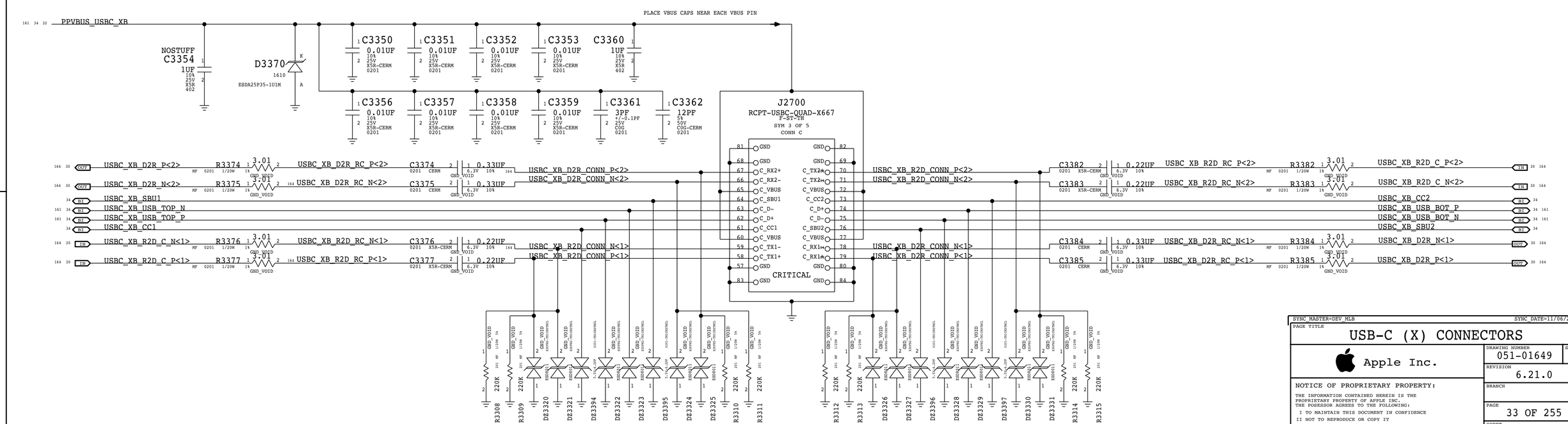
T SECONDARY ACE USB-C PORT CONTROLLER (UPC)



J137 SUPPORTS 5V @ 3A
J137 HAS A QUAD-PACK USB-C CONNECTOR





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USB-C (X) CONNECTORS

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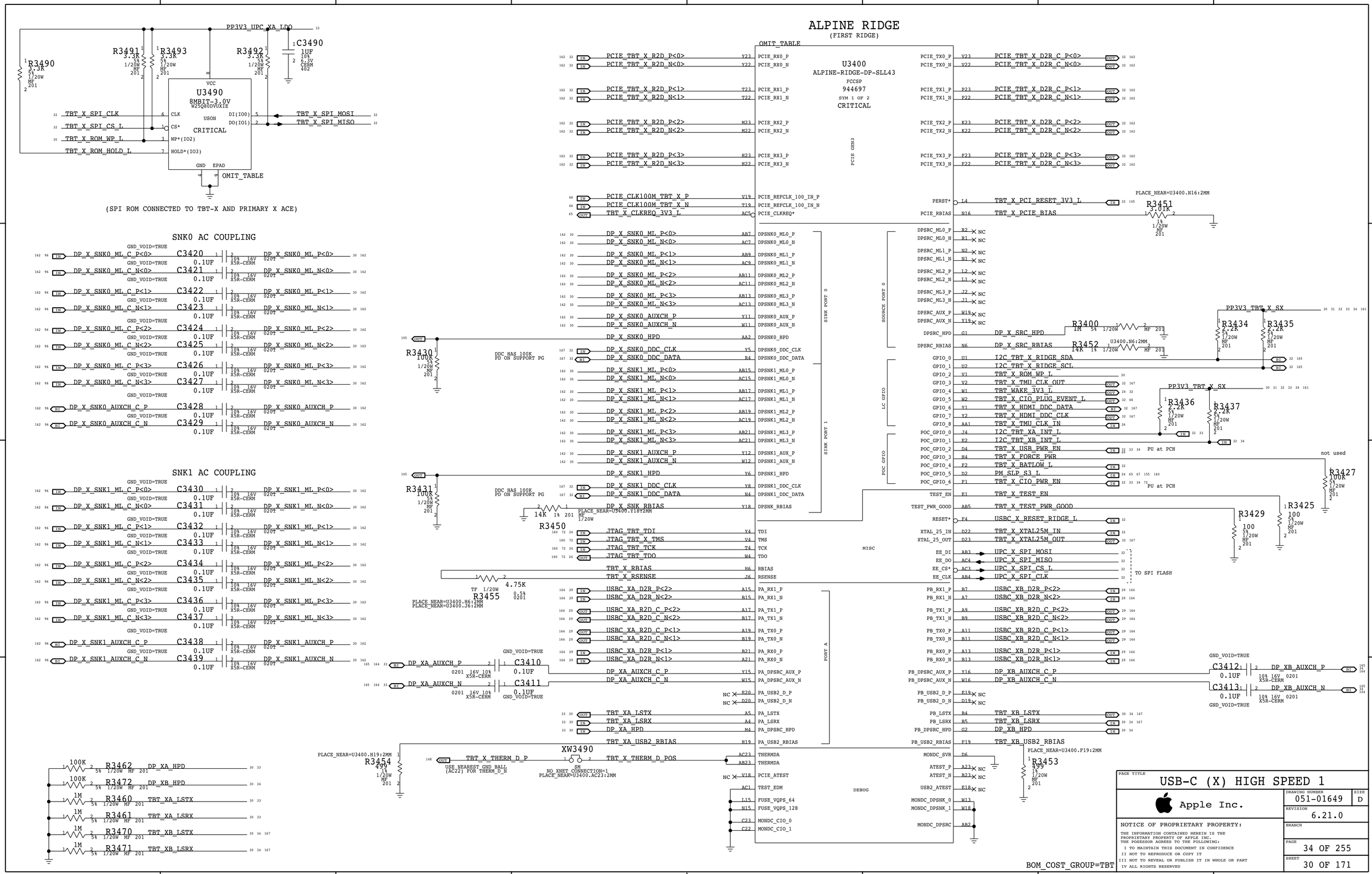
ALPINE RIDGE
(FIRST RIDGE)
U3400
ALPINE-RIDGE-DP-SLL43
FCCSP
944697
SYM 1 OF 2
CRITICAL
OMIT_TABLE
PCIE GEN3
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
LC GPIO
POC GPIO
MISC
PORT A
DEBUG
U3490
8MBIT-3.0V
W25Q80DVUXIE
USON
CRITICAL
VCC
GND EPAD
PP3V3_UPC_XA_LDO
(SPI ROM CONNECTED TO TBT-X AND PRIMARY X ACE)
SNK0 AC COUPLING
SNK1 AC COUPLING
DDC HAS 100K
PD ON SUPPORT PG
PLACE_NEAR=U3400.N16:2MM
PU at PCH
not used
TO SPI FLASH
PLACE_NEAR=U3400.H19:2MM
USE NEAREST GND BALL
(AC22) FOR THERM_D_N
NO XNET CONNECTION=1
PLACE_NEAR=U3400.AC23:2MM
BOM_COST_GROUP=TBT
PAGE TITLE
USB-C (X) HIGH SPEED 1
Apple Inc.
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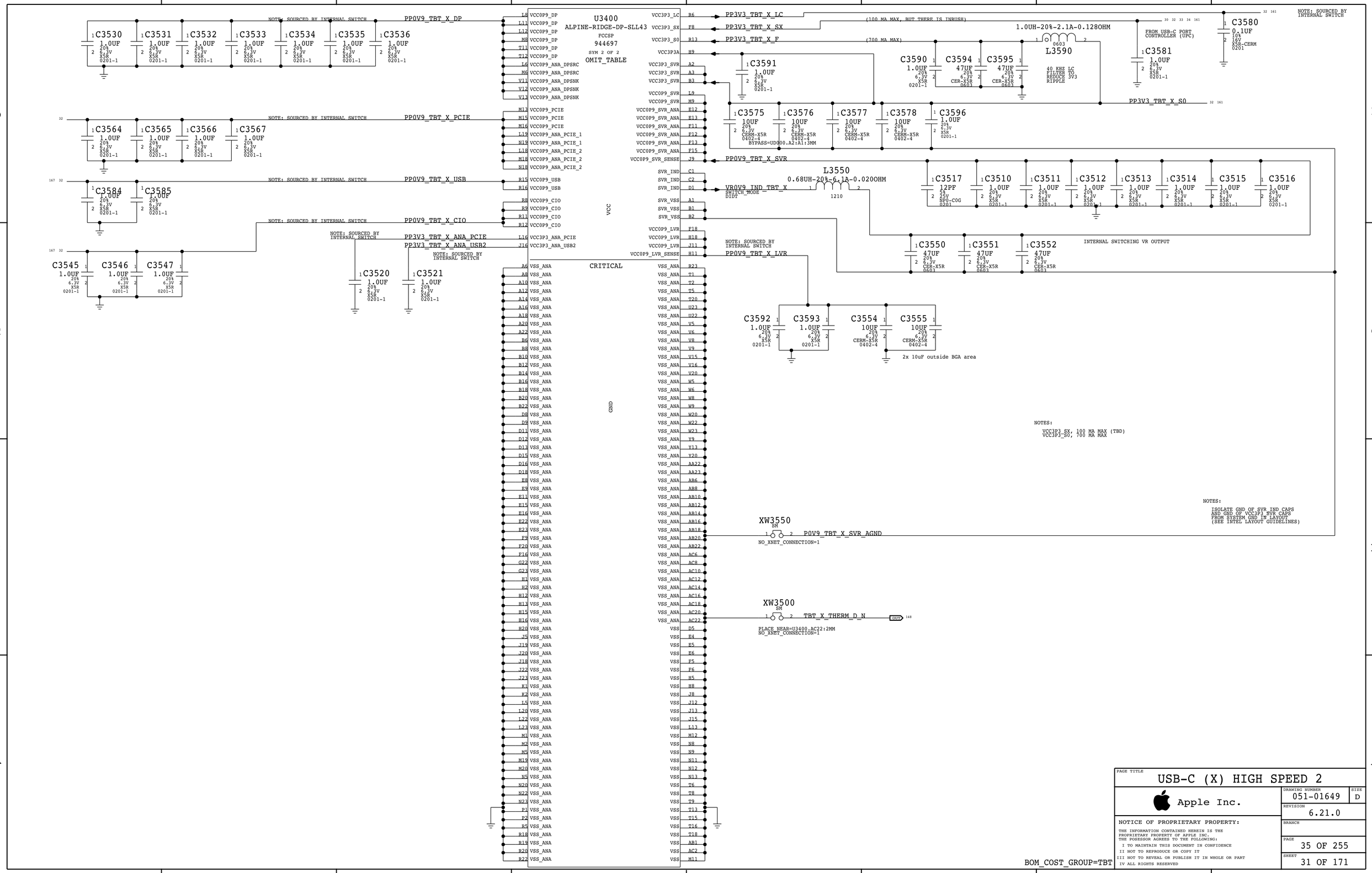

PAGE TITLE
USB-C (X) HIGH SPEED 2

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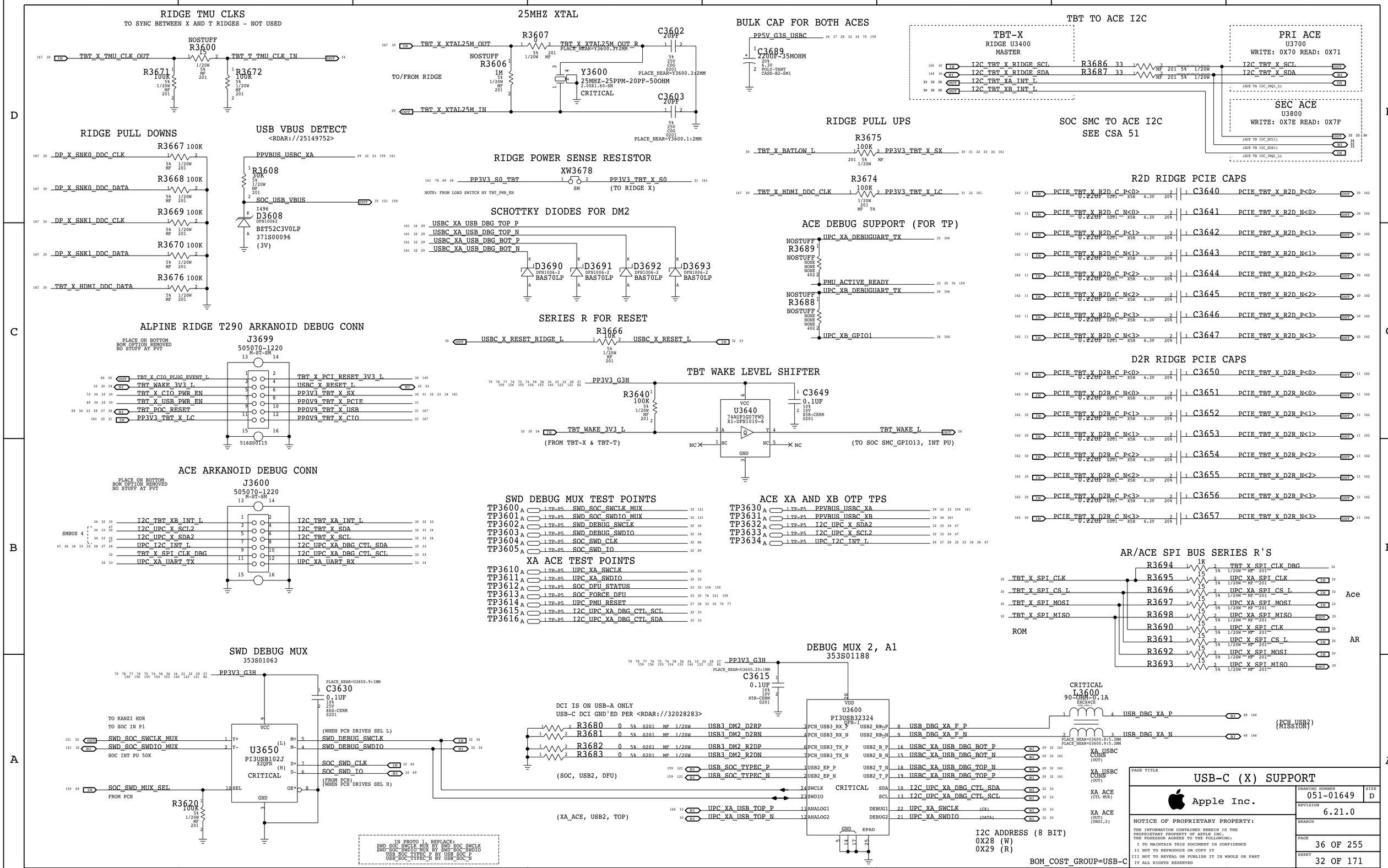
RIDGE TMU CLKS
TO SYNC BETWEEN X AND T RIDGES - NOT USED
TBT_X_TMU_CLK_OUT
NOSTUFF R3600 15
TBT_T_TMU_CLK_IN
R3671 100K
R3672 100K
25MHZ XTAL
TBT_X_XTAL25M_OUT
R3607 0
TBT_X_XTAL25M_OUT_R
PLACE_NEAR=Y3600.3:2MM
NOSTUFF R3606 1M
TO/FROM RIDGE
Y3600 25MHZ-25PPM-20PF-500HM 2.0X1.60-SM CRITICAL
C3602 20PF
PLACE_NEAR=Y3600.3:2MM
C3603 20PF
PLACE_NEAR=Y3600.1:2MM
TBT_X_XTAL25M_IN
BULK CAP FOR BOTH ACES
PP5V_G3S_USBC
C3689 220UF-35MOHM POLY-TANT CASE-B2-SM1
TBT TO ACE I2C
TBT-X
RIDGE U3400
MASTER
I2C_TBT_X_RIDGE_SCL
I2C_TBT_X_RIDGE_SDA
I2C_TBT_XA_INT_L
I2C_TBT_XB_INT_L
R3686 33
R3687 33
PRI ACE
U3700
WRITE: 0X70 READ: 0X71
I2C_TBT_X_SCL
I2C_TBT_X_SDA
SEC ACE
U3800
WRITE: 0X7E READ: 0X7F
(ACE TB I2C_SCL1)
(ACE TB I2C_SDA1)
(ACE TB I2C_IRQ1_L)
RIDGE PULL DOWNS
R3667 100K DP_X_SNK0_DDC_CLK
R3668 100K DP_X_SNK0_DDC_DATA
R3669 100K DP_X_SNK1_DDC_CLK
R3670 100K DP_X_SNK1_DDC_DATA
R3676 100K TBT_X_HDMI_DDC_DATA
USB VBUS DETECT
<RDAR://25149752>
PPVBUS_USBC_XA
R3608 30K
SOC_USB_VBUS
D3608 BZT52C3V0LP 371S00096 (3V)
RIDGE POWER SENSE RESISTOR
XW3678
PP3V3_S0_TBT
PP3V3_TBT_X_S0
(TO RIDGE X)
NOTE: FROM LOAD SWITCH BY TBT_PWR_EN
SCHOTTKY DIODES FOR DM2
USBC_XA_USB_DBG_TOP_P
USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_DBG_BOT_P
USBC_XA_USB_DBG_BOT_N
D3690 BAS70LP
D3691 BAS70LP
D3692 BAS70LP
D3693 BAS70LP
RIDGE PULL UPS
R3675 100K
TBT_X_BATLOW_L
PP3V3_TBT_X_SX
R3674 100K
TBT_X_HDMI_DDC_CLK
PP3V3_TBT_X_LC
SOC SMC TO ACE I2C
SEE CSA 51
ACE DEBUG SUPPORT (FOR TP)
UPC_XA_DEBUGUART_TX
R3689
PMU_ACTIVE_READY
UPC_XB_DEBUGUART_TX
R3688
UPC_XB_GPIO1
R2D RIDGE PCIE CAPS
PCIE_TBT_X_R2D_C_P<0> C3640 PCIE_TBT_X_R2D_P<0>
PCIE_TBT_X_R2D_C_N<0> C3641 PCIE_TBT_X_R2D_N<0>
PCIE_TBT_X_R2D_C_P<1> C3642 PCIE_TBT_X_R2D_P<1>
PCIE_TBT_X_R2D_C_N<1> C3643 PCIE_TBT_X_R2D_N<1>
PCIE_TBT_X_R2D_C_P<2> C3644 PCIE_TBT_X_R2D_P<2>
PCIE_TBT_X_R2D_C_N<2> C3645 PCIE_TBT_X_R2D_N<2>
PCIE_TBT_X_R2D_C_P<3> C3646 PCIE_TBT_X_R2D_P<3>
PCIE_TBT_X_R2D_C_N<3> C3647 PCIE_TBT_X_R2D_N<3>
D2R RIDGE PCIE CAPS
PCIE_TBT_X_D2R_C_P<0> C3650 PCIE_TBT_X_D2R_P<0>
PCIE_TBT_X_D2R_C_N<0> C3651 PCIE_TBT_X_D2R_N<0>
PCIE_TBT_X_D2R_C_P<1> C3652 PCIE_TBT_X_D2R_P<1>
PCIE_TBT_X_D2R_C_N<1> C3653 PCIE_TBT_X_D2R_N<1>
PCIE_TBT_X_D2R_C_P<2> C3654 PCIE_TBT_X_D2R_P<2>
PCIE_TBT_X_D2R_C_N<2> C3655 PCIE_TBT_X_D2R_N<2>
PCIE_TBT_X_D2R_C_P<3> C3656 PCIE_TBT_X_D2R_P<3>
PCIE_TBT_X_D2R_C_N<3> C3657 PCIE_TBT_X_D2R_N<3>
ALPINE RIDGE T290 ARKANOID DEBUG CONN
PLACE ON BOTTOM
BOM OPTION REMOVED
NO STUFF AT PVT
J3699
505070-1220
M-ST-SM
TBT_X_CIO_PLUG_EVENT_L
TBT_WAKE_3V3_L
TBT_X_CIO_PWR_EN
TBT_X_USB_PWR_EN
TBT_POC_RESET
PP3V3_TBT_X_LC
TBT_X_PCI_RESET_3V3_L
USBC_X_RESET_L
PP3V3_TBT_X_SX
PP0V9_TBT_X_PCIE
PP0V9_TBT_X_USB
PP0V9_TBT_X_CIO
516S00115
SERIES R FOR RESET
R3666 10K
USBC_X_RESET_RIDGE_L
USBC_X_RESET_L
TBT WAKE LEVEL SHIFTER
PP3V3_G3H
R3640 100K
C3649 0.1UF
U3640 74AUP1G07FW5 X1-DFN1010-6
TBT_WAKE_3V3_L
(FROM TBT-X & TBT-T)
TBT_WAKE_L
(TO SOC SMC_GPIO13, INT PU)
ACE ARKANOID DEBUG CONN
PLACE ON BOTTOM
BOM OPTION REMOVED
NO STUFF AT PVT
J3600
505070-1220
M-ST-SM
SMBUS 4
I2C_TBT_XB_INT_L
I2C_UPC_X_SCL2
I2C_UPC_X_SDA2
UPC_I2C_INT_L
TBT_X_SPI_CLK_DBG
UPC_XA_UART_TX
I2C_TBT_XA_INT_L
I2C_TBT_X_SDA
I2C_TBT_X_SCL
I2C_UPC_XA_DBG_CTL_SDA
I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_RX
SWD DEBUG MUX TEST POINTS
TP3600 SWD_SOC_SWCLK_MUX
TP3601 SWD_SOC_SWDIO_MUX
TP3602 SWD_DEBUG_SWCLK
TP3603 SWD_DEBUG_SWDIO
TP3604 SOC_SWD_CLK
TP3605 SOC_SWD_IO
XA ACE TEST POINTS
TP3610 UPC_XA_SWCLK
TP3611 UPC_XA_SWDIO
TP3612 SOC_DFU_STATUS
TP3613 SOC_FORCE_DFU
TP3614 UPC_PMU_RESET
TP3615 I2C_UPC_XA_DBG_CTL_SCL
TP3616 I2C_UPC_XA_DBG_CTL_SDA
ACE XA AND XB OTP TPS
TP3630 PPVBUS_USBC_XA
TP3631 PPVBUS_USBC_XB
TP3632 I2C_UPC_X_SDA2
TP3633 I2C_UPC_X_SCL2
TP3634 UPC_I2C_INT_L
AR/ACE SPI BUS SERIES R'S
TBT_X_SPI_CLK
TBT_X_SPI_CS_L
TBT_X_SPI_MOSI
TBT_X_SPI_MISO
ROM
R3694 1K TBT_X_SPI_CLK_DBG
R3695 15 UPC_XA_SPI_CLK
R3696 15 UPC_XA_SPI_CS_L
R3697 15 UPC_XA_SPI_MOSI
R3698 15 UPC_XA_SPI_MISO
R3690 15 UPC_X_SPI_CLK
R3691 15 UPC_X_SPI_CS_L
R3692 15 UPC_X_SPI_MOSI
R3693 15 UPC_X_SPI_MISO
Ace
AR
SWD DEBUG MUX
353S01063
PP3V3_G3H
C3630 0.1UF
TO KANZI HDR
TO SOC IN P1
U3650 PI3USB102J
CRITICAL
SWD_SOC_SWCLK_MUX
SWD_SOC_SWDIO_MUX
SOC INT PU 50K
(WHEN PCH DRIVES SEL L)
SWD_DEBUG_SWCLK
SWD_DEBUG_SWDIO
SOC_SWD_CLK
SOC_SWD_IO
(FROM PCH)
(WHEN PCH DRIVES SEL H)
SOC_SWD_MUX_SEL
FROM PCH
R3620 100K
IN PROTO 1, REPLACE:
SWD_SOC_SWCLK_MUX BY SWD_SOC_SWCLK
SWD_SOC_SWDIO_MUX BY SWD_SOC_SWDIO
USB_SOC_TYPEC_P BY USB_SOC_P
USB_SOC_TYPEC_N BY USB_SOC_N
DEBUG MUX 2, A1
353S01188
PP3V3_G3H
C3615 0.1UF
DCI IS ON USB-A ONLY
USB-C DCI GND'ED PER <RDAR://32028283>
U3600 PI3USB32324
R3680
R3681
R3682
R3683
USB3_DM2_D2RP
USB3_DM2_D2RN
USB3_DM2_R2DP
USB3_DM2_R2DN
USB_SOC_TYPEC_P
USB_SOC_TYPEC_N
(SOC, USB2, DFU)
UPC_XA_USB_TOP_P
UPC_XA_USB_TOP_N
(XA_ACE, USB2, TOP)
USB_DBG_XA_F_P
USB_DBG_XA_F_N
USBC_XA_USB_DBG_BOT_P
USBC_XA_USB_DBG_BOT_N
USBC_XA_USB_DBG_TOP_N
USBC_XA_USB_DBG_TOP_P
I2C_UPC_XA_DBG_CTL_SDA
I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_SWCLK
UPC_XA_SWDIO
CRITICAL
I3600 90-OHM-0.1A
USB_DBG_XA_P
USB_DBG_XA_N
(PCH_USB2) (MISSION)
XA_USBC CONN (OUT)
XA_ACE (CTL MUX)
XA_ACE (OUT) (DBG1,2)
I2C ADDRESS (8 BIT)
0X28 (W)
0X29 (R)
BOM_COST_GROUP=USB-C
PAGE TITLE
USB-C (X) SUPPORT
Apple Inc.
DRAWING NUMBER 051-01649
SIZE D
REVISION 6.21.0
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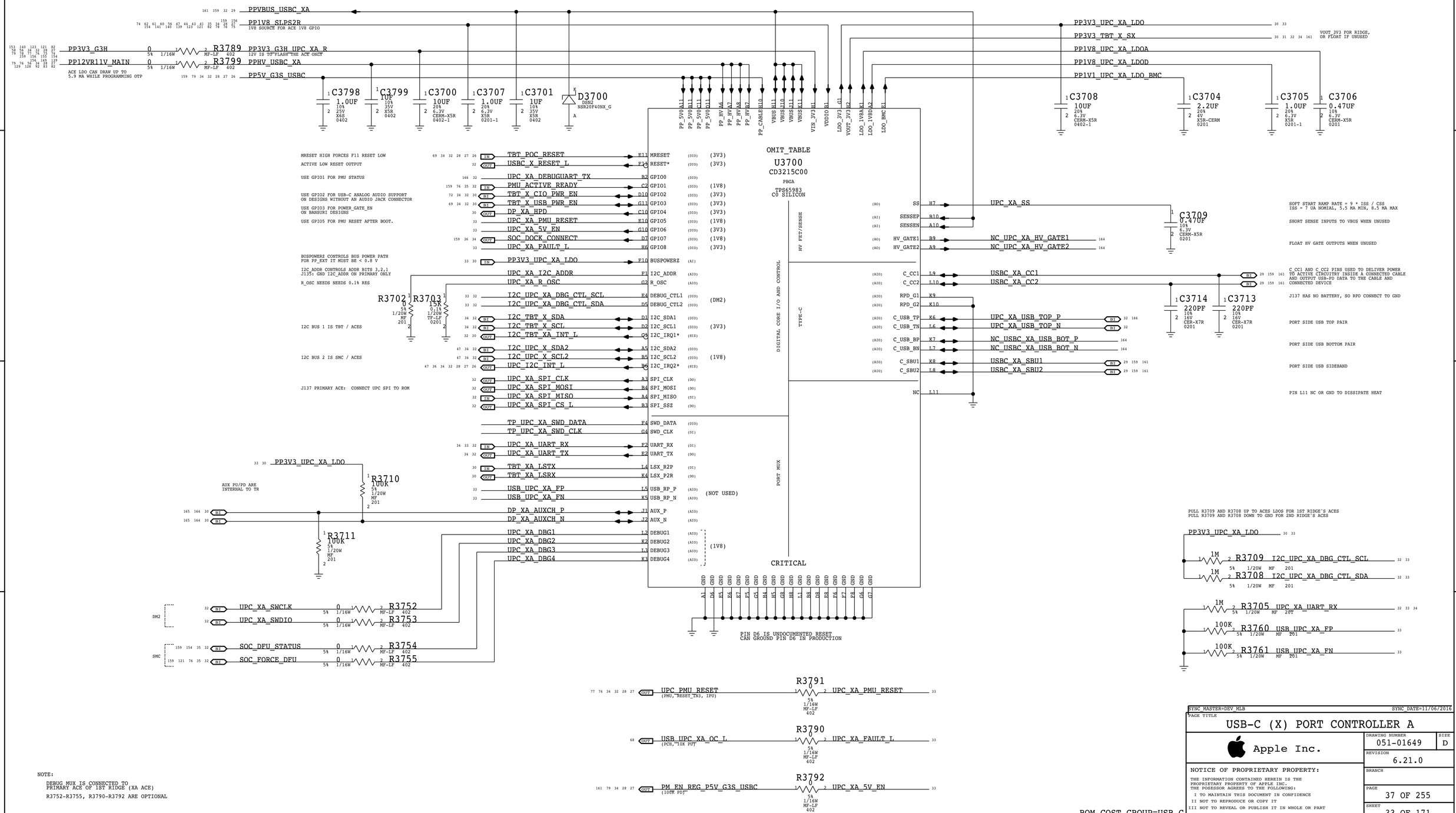
X PRIMARY ACE USB-C PORT CONTROLLER (UPC)

J137 USBC SUPPORTS 5V @ 3A
PP12V IS FOR PROGRAMMING ACE ONLY



NOTE:

DEBUG MUX IS CONNECTED TO PRIMARY ACE OF 1ST RIDGE (XA ACE)

R3752-R3755, R3790-R3792 ARE OPTIONAL

BOM_COST_GROUP=USB-C

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE
USB-C (X) PORT CONTROLLER A

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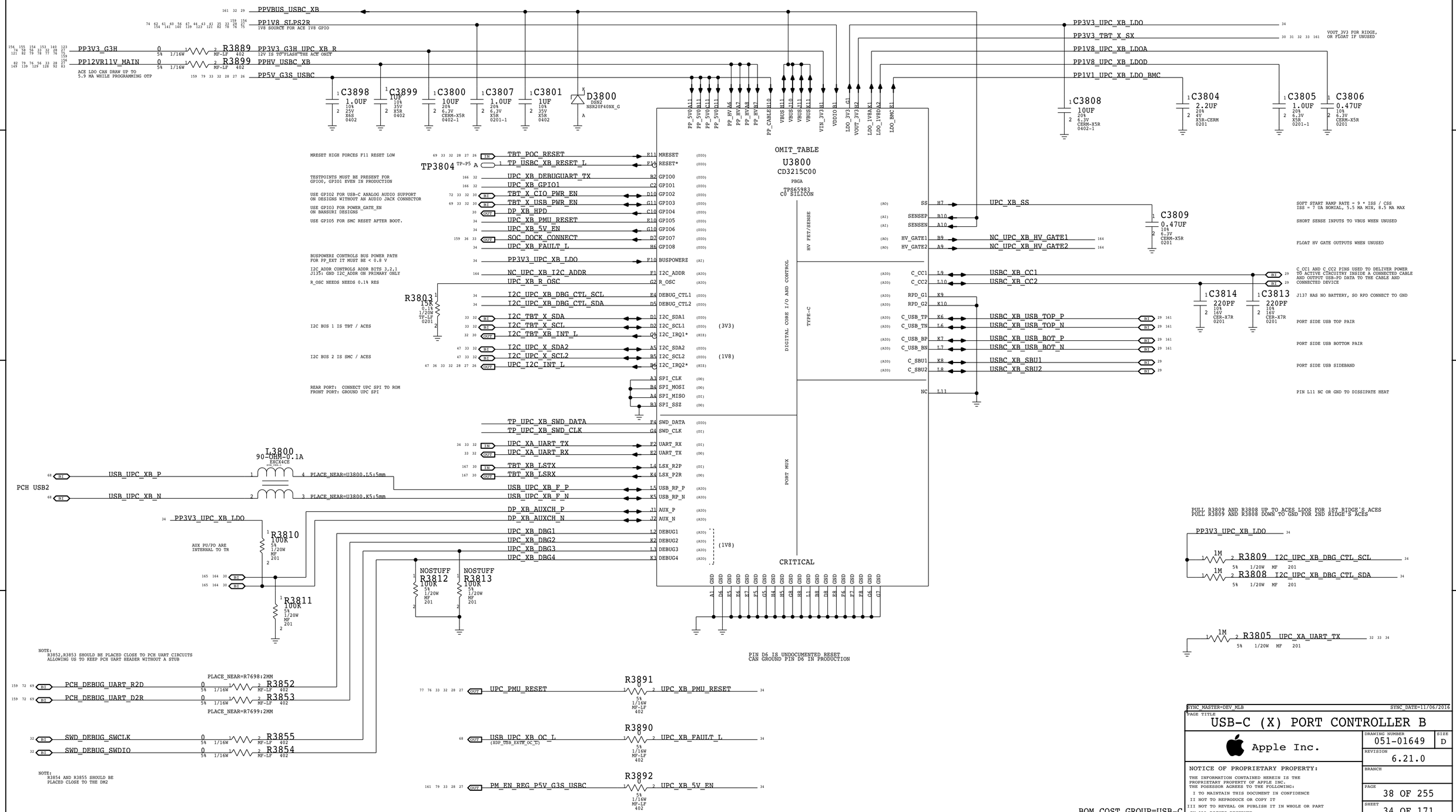
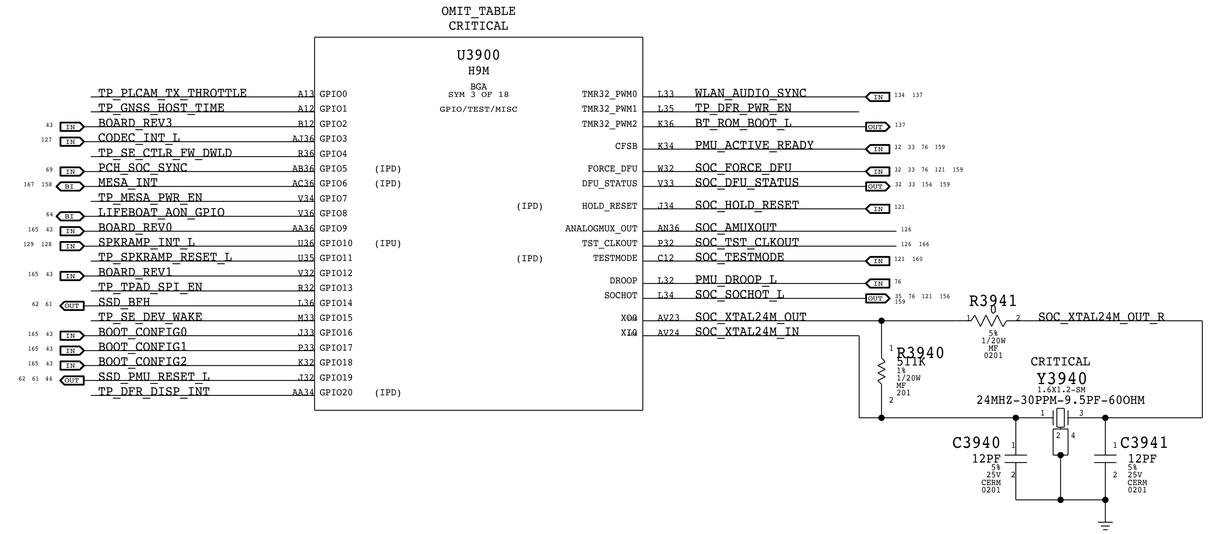
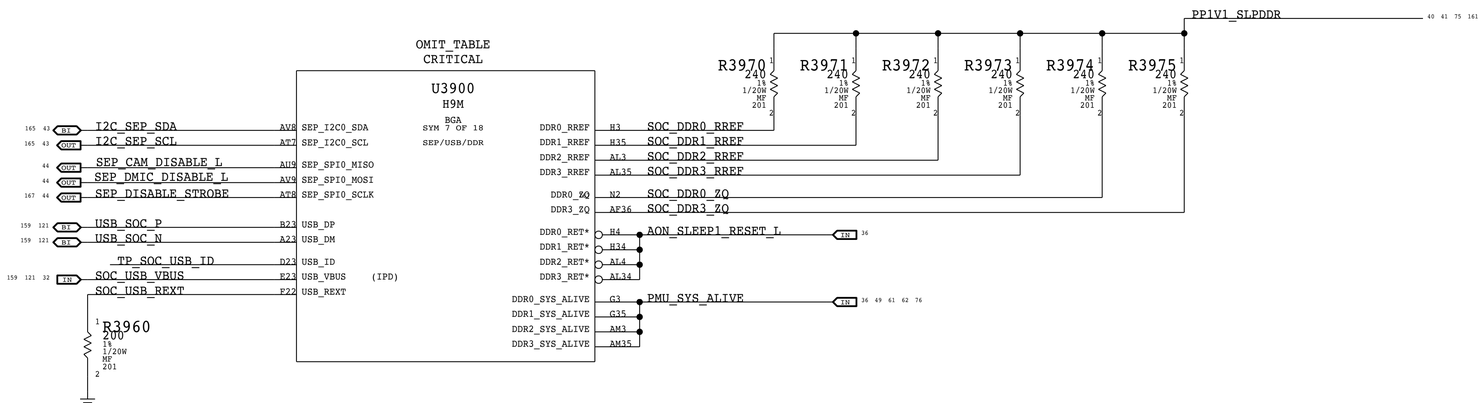
X SECONDARY ACE USB-C PORT CONTROLLER (UPC)



Note 1) IPU represents SW configured state, not HW default
Note 2) Internal and external pulls are preliminary assumptions. To be verified.





PP1V8_SLPS2R
R3939 47K 5% 1/20W MF 201 SOC_SOCHOT_L

BOM_COST_GROUP=SOC

PAGE TITLE
SOC GPIO/SEP/USB/DDR/TEST

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OMIT_TABLE
CRITICAL

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123	AOP_UART_TX_FUNC_0	D3	AOP_FUNC[0]		AOP_PDM_CLK0	P6	PDM_DMIC_CLK0_R	OUT 44 165
123	AOP_UART_RX_FUNC_1	F4	AOP_FUNC[1]		AOP_PDM_CLK1	K2	PDM_DMIC_CLK1_R	OUT 44 165
	TP_GYRO_INT1	M6	AOP_FUNC[2] (IPD)	(IPU)	AOP_PDM_CLK2	J6	TP_SMC_DEV_SUPPLY_L	
64 BI	LIFEBOAT_AOP_GPIO	D4	AOP_FUNC[3] (IPD)	(IPU)	AOP_PDM_CLK3	L6	TP_PLCAM_PROX_INT_L	
138 OUT	BTUARTMUX_SEL_PCH	F3	AOP_FUNC[4]		AOP_PDM_CLK4	L5	NC_SOC_AOP_PDM_CLK4	167
145 67 IN	SOC_PERST_L	K6	AOP_FUNC[5]					
147	NC_ALTIMETER_INT	E4	AOP_FUNC[6] (IPD)	(IPD)	AOP_PDM_DATA0	J5	PDM_DMIC_DATA0	IN 51
	TP_SPI_GYRO_CS_L	J3	AOP_FUNC[7]	(IPD)	AOP_PDM_DATA1	K4	PDM_DMIC_DATA1	IN 131
	TP_SPI_ALTIMETER_CS_L	H6	AOP_FUNC[8]		AOP_SPI_MOSI	D2	TP_SPI_AOP_SENSOR_MOSI_R	
	TP_I2C_AOP_SCL	N6	AOP_I2C0_SCL		AOP_SPI_SCLK	F2	TP_SPI_AOP_SENSOR_CLK_R	
	TP_I2C_AOP_SDA	G5	AOP_I2C0_SDA		AOP_SPI_MISO	E2	TP_SPI_AOP_SENSOR_MISO	

OMIT_TABLE
CRITICAL

U3900
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SYM 5 OF 18

167	NC_DFR_TOUCH_INT_L	AL6	AON_GPIO0	(IPU)	JTAG_TCK	AK6	SWD_SOC_SWCLK	AIN 121 167
167 158 45 IN	CPU_SMC_THRMTRIP_L	AE6	AON_GPIO1 (IPU)	(IPU)	JTAG_TMS	AN5	SWD_SOC_SWDIO	BI 121 167
103 IN	SMC_GFX_SELF_THROTTLE	AT5	AON_GPIO2 (IPD)	(IPU)	JTAG_TDI	AH6	JTAG_SOC_TDI	AIN 121 160
45 IN	GPU_SMC_THRMTRIP	AN4	AON_GPIO3 (IPD)		JTAG_TDO	AP4	JTAG_SOC_TDO	OUT 121 160
73 IN	XDP_PRESENT_L	AK4	AON_GPIO4	(IPD)	JTAG_TRST*	AJ6	TP_JTAG_SOC_TRST_L	160
127 OUT	CODEC_RESET_L	AV5	AON_GPIO5		JTAG_SEL	AC6	SOC_JTAG_SEL (DAP=0, TAP=1)	36 160
138 OUT	SOC_BT_DEV_WAKE	AR3	AON_GPIO6		DOCK_CONNECT	AN2	SOC_DOCK_CONNECT	AIN 33 34 36 159
56 IN	PCIEDN_WAKE_L	AG6	AON_GPIO7 (IPU)					
167 158 BI	ENET_LOW_PWR	AU5	AON_GPIO8		AON_SWD0_TMS	AJ4	SWD_WLAN_SWDIO	BI 134 137 160
141 IN	ACDC_ID	AP2	AON_GPIO9 (IPU)	(IPU)	AON_SWD1_TMS	AH4	MESA_MENUKEY_L	BI 158 167
59 IN	SDCONN_STATE_CHANGE_L	AR4	AON_GPIO10		AON_SWD01_TCK	AJ2	SWD_WLAN_SWCLK	OUT 134 137 160
56 IN	ENET_MEDIA_SENSE	AN3	AON_GPIO11 (IPD)		WDOG	AJ5	SOC_WDOG	OUT 76
165 76 IN	PMU_INT_L	AT6	AON_GPIO12 (IPU)		AON_SLEEP1_RESET*	AF6	AON_SLEEP1_RESET_L	OUT 35

PCIEDN_WAKE_L is needed for ENET PCIE wake purposes

SDCONN_STATE_CHANGE_L IPU removed per <RDAR://30976274>

PLACE_NEAR=U3900.AD6:5MM
PLACE_NEAR=U7800.R7:5MM

76 OUT	SPMI_CLK	R4036	20	5%	1/20W	MF	201	SPMI_CLK_R — AD6 AON_SPMI_SCLK
74 BI	SPMI_DATA	R4037	20	5%	1/20W	MF	201	SPMI_DATA_R — AR2 AON_SPMI_SDATA

76 IN	PMU_CLK32K_SOC	AR5	RT_CLK32768					
166	SOC_COLD_RESET_L	AK2	COLD_RESET*					
	R4039 1 2 4.7K 5% 201 MF 1/20W	AK3	CFSB_AON					
160 121 76 44 IN	PMU_COLD_RESET_L							

OMIT_TABLE
CRITICAL

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SMC

PLACE_NEAR=U3900.U2:5MM
PLACE_NEAR=U3900.V2:5MM
PLACE_NEAR=U3900.U3:5MM
PLACE_NEAR=U3900.V4:5MM

124 67 36 BI	ESPI_IO<0>	R4050	20	5%	1/20W	MF	201	ESPI_IO_R<0> — V2 SMC_ESPI_IO0
124 67 36 BI	ESPI_IO<1>	R4051	20	5%	1/20W	MF	201	ESPI_IO_R<1> — U3 SMC_ESPI_IO1
124 67 36 BI	ESPI_IO<2>	R4052	20	5%	1/20W	MF	201	ESPI_IO_R<2> — U4 SMC_ESPI_IO2
124 67 36 BI	ESPI_IO<3>	R4053	20	5%	1/20W	MF	201	ESPI_IO_R<3> — V8 SMC_ESPI_IO3

165 124 66 IN	ESPI_CLK	U2	SMC_ESPI_CLK	(IPD)	SMC_GPIO0	Y4	CODEC_WAKE_L	IN 127
124 67 36 IN	ESPI_CS_L	V3	SMC_ESPI_CS*	(IPD)	SMC_GPIO1	Y8	BT_HOST_WAKE	IN 134 137
124 67 IN	ESPI_RESET_L	V6	SMC_ESPI_RESET* (IPD)	(IPD)	SMC_GPIO2	Y5	WLAN_HOST_WAKE	IN 138
43 IN	SMC_PECI_RX	M5	SMC_PECI_IN (IPD)		SMC_GPIO3	AA2	SMC_GFX_THROTTLE_L	OUT 103
43 OUT	SMC_PECI_TX	T6	SMC_PECI_OUT		SMC_GPIO4	Y7	NC_LIDINT_L_UARTHDD_D2R	167
160 43 OUT	SMC_PCH_PWROK	W7	PCH_PWROK	(IPD)	SMC_GPIO5	Y6	PCC_EVENT	IN 107
160 43 OUT	SMC_PCH_SYS_PWROK	W8	SYS_PWROK		SMC_GPIO6	AB2	LIFEBOAT_SMC_GPIO	BI 64
43 OUT	SMC_RSMRST_L	W6	RSMRST*		SMC_GPIO7	AD5	PSU11VOC_WAKE_L	IN 140
160 43 OUT	SMC_SYSRST_L	W4	SYS_RESET*		SMC_GPIO8	AD2	PSU12VPGOOD	IN 52 53 140 161
160 76 72 IN	PM_SLP_S0_L	AA4	SLP_S0B		SMC_GPIO9	AB4	SPI_DESCRIPTOR_OVERRIDE_L	OUT 46
156 76 BI	SMC_PROCHOT_L	B5	PROCHOT*	(IPU)	SMC_GPIO10	AC2	DISP_GCON_INT_L	IN 49
76 62 61 49 35 IN	PMU_SYS_ALIVE	AA6	SYS_ALIVE		SMC_GPIO11	AC3	PCH_GCON_INT_L	OUT 69
47 OUT	I2C_UPC_SCL	M3	SMC_I2C0_SCL		SMC_GPIO12	AA8	PSU_P12V_EN_SMC_L	OUT 141
47 BI	I2C_UPC_SDA	J4	SMC_I2C0_SDA	(IPU)	SMC_GPIO13	AB3	TBT_WAKE_L	IN 32
162 47 OUT	I2C_SNS0_S0_SCL	N4	SMC_I2C1_SCL	(IPU)	SMC_GPIO14	AE2	UPC_I2C_INT_L	IN 26 27 28 32 33 34 47
47 BI	I2C_SNS0_S0_SDA	P4	SMC_I2C1_SDA		SMC_GPIO15	L4	NC_GNSS_HOST_WAKE	167
47 OUT	I2C_MLBSNS_SCL	U5	SMC_I2C2_SCL		SMC_ADC0	AG2	SMC_P12V_MAIN_ISENSE	IN 149 161
47 BI	I2C_MLBSNS_SDA	M2	SMC_I2C2_SDA		SMC_ADC1	AC4	SMC_P12V_GPU_ISENSE	IN 149 161
47 44 OUT	I2C_DISP_SCL	U6	SMC_I2C3_SCL		SMC_ADC2	AH3	SMC_CPU_VDDQ_01_S3_ISENSE	IN 151
47 44 BI	I2C_DISP_SDA	R4	SMC_I2C3_SDA		SMC_ADC3	AD4	SMC_P12V_MAIN_AUX_GPU_ISENSE	IN 149
122 47 OUT	I2C_PWR_SCL	P3	SMC_I2C4_SCL		SMC_ADC4	AB6	SMC_P12V_MAIN_CPU_HS_ISENSE	IN 149
122 47 BI	I2C_PWR_SDA	T4	SMC_I2C4_SDA		SMC_ADC5	AH2	SMC_P12V_MAIN_VSENSE	IN 149
	TP_I2C_IOSNS_SCL	R2	SMC_I2C5_SCL		SMC_ADC6	AG4	SMC_CPU_VDDQ_23_S3_ISENSE	IN 151
	TP_I2C_IOSNS_SDA	P2	SMC_I2C5_SDA		SMC_ADC7	AC5	SMC_P12V_GPU_VSENSE	IN 149
47 OUT	I2C_SSD_SCL	R3	SMC_I2C6_SCL		REFP_ADC	AF4	PP1V25_SLPS2R_SMC_AVREF	43
47 BI	I2C_SSD_SDA	T2	SMC_I2C6_SDA		REFM_ADC	AG3	GND_SMC_AVSS	43 149 151 152 167
					SMC_PWM0	J2	SMC_FAN_0_PWM	OUT 60 167
					SMC_TACH0	L3	SMC_FAN_0_TACH	IN 60 159
					SMC_PWM1	R6	SMC_FAN_1_PWM	OUT 60
					SMC_TACH1	L2	SMC_FAN_1_TACH	IN 60 159
					SMC_PWM2	M4	TP_SMC_LED_ONEWIRE	
				(IPU)	SMC_UART0_RXD	V4	SMC_DEBUGPRT_RX	IN 26 123 159
					SMC_UART0_TXD	V5	SMC_DEBUGPRT_TX	OUT 26 123 159
					SWD_OUT0_TCK	AE3	SSD0_SWCLK_UART_R2D	OUT 61
					SWD_OUT0_TMS	AA5	SSD0_SWDIO_UART_D2R	BI 61
					SWD_OUT1_TCK	AF2	SSD1_SWCLK_UART_R2D	OUT 62 146
					SWD_OUT1_TMS	AA7	SSD1_SWDIO_UART_D2R	BI 62

SPI_DESCRIPTOR_OVERRIDE_L is only used in MAF systems

XW4089
SM
PLACE_NEAR=U3900.AG3:4MM
2 1

PP1V8_S5
17 43 44 45 47 53 59 63 66 67 69 70 72 74
137 145 146 147 148 159

R4046	10K	5%	1/20W	MF	201	SOC_JTAG_SEL	36 160
R4047	100K	5%	1/20W	MF	201	SOC_DOCK_CONNECT	33 34 36 159
R4054	100K	5%	1/20W	MF	201	ESPI_IO<0>	36 67 124
R4055	100K	5%	1/20W	MF	201	ESPI_IO<1>	36 67 124
R4056	100K	5%	1/20W	MF	201	ESPI_IO<2>	36 67 124
R4057	100K	5%	1/20W	MF	201	ESPI_IO<3>	36 67 124
R4059	100K	5%	1/20W	MF	201	ESPI_CS_L	36 67 124

BOM_COST_GROUP=SOC

PAGE TITLE
SOC AOP/AON/SMC

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CRITICAL

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ISP

165 51	IN	MIPI_FTCAM_DATA_P<0>	B27	MIPI0C_DATA0_P			
165 51	IN	MIPI_FTCAM_DATA_N<0>	A27	MIPI0C_DATA0_N			
165 51	IN	MIPI_FTCAM_DATA_P<1>	B25	MIPI0C_DATA1_P			
165 51	IN	MIPI_FTCAM_DATA_N<1>	A25	MIPI0C_DATA1_N			
165 51	IN	MIPI_FTCAM_CLK_P	B26	MIPI0C_CLK_P			
165 51	IN	MIPI_FTCAM_CLK_N	A26	MIPI0C_CLK_N			
162		NC_MIPI_PLCAM_DATA_P<0>	B28	MIPI1C_DATA0_P			
162		NC_MIPI_PLCAM_DATA_N<0>	A28	MIPI1C_DATA0_N			
162		NC_MIPI_PLCAM_DATA_P<1>	B30	MIPI1C_DATA1_P			
162		NC_MIPI_PLCAM_DATA_N<1>	A30	MIPI1C_DATA1_N			
162		NC_MIPI_PLCAM_CLK_P	B29	MIPI1C_CLK_P			
162		NC_MIPI_PLCAM_CLK_N	A29	MIPI1C_CLK_N			
162		NC_MIPI_DFR_DATA_P	B33	MIPID_DATA0_P			
162		NC_MIPI_DFR_DATA_N	A33	MIPID_DATA0_N			
162		NC_MIPI_DFR_CLK_P	B32	MIPID_CLK_P			
162		NC_MIPI_DFR_CLK_N	A32	MIPID_CLK_N			
		SOC_MIPI0C_REXT	F23	MIPI0C_REXT			
		SOC_MIPI1C_REXT	F26	MIPI1C_REXT			
166		SOC_MIPID_REXT	F27	MIPID_REXT			
		ISP_I2C0_SDA	AF32	I2C_FTCAM_SDA		BI	48 51
		ISP_I2C0_SCL	AH36	I2C_FTCAM_SCL		OUT	48 51
		ISP_I2C1_SDA	AB32	TP_I2C_PLCAM_SDA			
		ISP_I2C1_SCL	AG32	TP_I2C_PLCAM_SCL			
		SENSOR0_CLK	AK35	TP_FTCAM_CLK12M_R			
		SENSOR0_RST	AK34	TP_FTCAM_RESET_L			
		SENSOR0_ISTRB	AJ33	TP_DFR_TOUCH_RESET_L			
		SENSOR1_CLK	AD33	TP_PLCAM_RX_CLK12M_R			
		SENSOR1_RST	AC32	TP_PLCAM_RX_RESET_L			
		SENSOR1_ISTRB	AC34	DFR_DISP_RESET_L		BI	158 167
		SENSOR2_CLK	AD32	TP_PLCAM_TX_CLK12M_R			
		SENSOR2_RST	AJ32	TP_PLCAM_TX_RESET_L			
	(IPD)	SENSOR_INT	AA33	TP_PLCAM_TX_INT			
	(IPD)	DISP_TE	H32	TP_DFR_DISP_TE			
		DISP_VSYNC	T36	BOARD_REV2		IN	43 165
		CLK32K_OUT	AK33	TP_DFR_TOUCH_CLK32K_RESET_L			

R4101 and R4102 can potentially be no-stuff since MIPI "C" and "D" are unused

R4100 4.02K 1% 1/20W MF 201
R4101 4.02K 1% 1/20W MF 201
R4102 4.02K 1% 1/20W MF 201

OMIT_TABLE
CRITICAL

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I2C/UART/SPI/I2S

128 48	BI	I2C_SPKRAMP_L_SDA	AE35	I2C0_SDA			
128 48	OUT	I2C_SPKRAMP_L_SCL	AD35	I2C0_SCL			
129 48	BI	I2C_SPKRAMP_R_SDA	AF34	I2C1_SDA			
129 48	OUT	I2C_SPKRAMP_R_SCL	AG35	I2C1_SCL			
127 48	BI	I2C_CODEC_SDA	M34	I2C2_SDA			
127 48	OUT	I2C_CODEC_SCL	R33	I2C2_SCL			
51 48	BI	I2C_ALS_SDA	Y32	I2C3_SDA			
51 48	OUT	I2C_ALS_SCL	AE34	I2C3_SCL			
		TP_I2C_DFR_SDA	T34	I2C4_SDA			
		TP_I2C_DFR_SCL	U32	I2C4_SCL			
48	BI	I2C_SOC_5_SDA	R35	I2C5_SDA			
48	OUT	I2C_SOC_5_SCL	U33	I2C5_SCL			
161 129	IN	SPKR_ID1	P34	I2C6_SDA	(IPU)		
161 128	IN	SPKR_ID0	R34	I2C6_SCL	(IPU)		
159 123	IN	SOC_DEBUGPRT_RX	Y33	UART0_RXD	(IPU)		
159 123	OUT	SOC_DEBUGPRT_TX	Y34	UART0_TXD			
		TP_UART_SE_D2R	B15	UART1_RXD			
		TP_UART_SE_R2D	A15	UART1_TXD			
		TP_UART_SE_D2R_CTS_L	C15	UART1_CTS*			
		TP_UART_SE_R2D_RTS_L	D15	UART1_RTS*			
166 138	IN	UART_BT_SOC_D2R	J36	UART2_RXD			
166 138	OUT	UART_BT_SOC_R2D	J35	UART2_TXD			
138	IN	UART_BT_SOC_D2R_CTS_L	N38	UART2_CTS*			
138	OUT	UART_BT_SOC_R2D_RTS_L	M38	UART2_RTS*			
134	IN	UART_BT_SOC_LH_D2R	M36	UART3_RXD			
134	OUT	UART_BT_SOC_LH_R2D	N36	UART3_TXD			
		TP_UART_GNSS_D2R_CTS_L	M35	UART3_CTS*			
		TP_UART_GNSS_R2D_RTS_L	N34	UART3_RTS*			
		TP_UART_WLAN_D2R	B14	UART4_RXD			
		TP_UART_WLAN_R2D	A14	UART4_TXD			
		TP_UART_WLAN_D2R_CTS_L	C14	UART4_CTS*			
		TP_UART_WLAN_R2D_RTS_L	C13	UART4_RTS*			
		SPI0_MISO	AR9	SPI_SOCROM_MISO		IN	43
		SPI0_MOSI	AR7	SPI_SOCROM_MOSI_R			
		SPI0_SCLK	AU7	SPI_SOCROM_CLK_R			
		SPI0_SSIN	AT9	SPI_SOCROM_CS_L		OUT	43
	(IPU)	SPI1_MISO	P36	SPI_TPAD_MISO		IN	43 166
		SPI1_MOSI	N34	SPI_TPAD_MOSI		OUT	43 166
		SPI1_SCLK	P35	SPI_TPAD_CLK		OUT	43 166
		SPI1_SSIN	T32	TP_SPI_TPAD_CS_L			
		SPI2_MISO	A19	TP_SPI_MESA_MISO			
		SPI2_MOSI	A20	TP_SPI_MESA_MOSI_R			
		SPI2_SCLK	C19	TP_SPI_MESA_CLK_R			
		SPI2_SSIN	A18	WLAN_THROTTLE		OUT	134 137 160
		SPI3_MISO	C17	TP_SPI_DFR_MISO			
		SPI3_MOSI	C18	TP_SPI_DFR_MOSI_R			
		SPI3_SCLK	B18	TP_SPI_DFR_CLK_R			
		SPI3_SSIN	A17	TP_SPI_DFR_CS_L			
	(IPD)	I2S0_DIN	AC33	TP_I2S_SPKRAMP_L_D2R			
		I2S0_DOUT	AG34	I2S_SPKRAMP_L_R2D_R		OUT	44 165
		I2S0_BCLK	AA32	I2S_SPKRAMP_L_BCLK_R		OUT	44 165
		I2S0_LRCK	AG33	I2S_SPKRAMP_L_LRCLK_R		OUT	44 167
		I2S0_MCK	AB35	NC			
	(IPD)	I2S1_DIN	B20	TP_I2S_SPKRAMP_R_D2R			
		I2S1_DOUT	C20	I2S_SPKRAMP_R_R2D_R		OUT	44 165
		I2S1_BCLK	C21	I2S_SPKRAMP_R_BCLK_R		OUT	44 165
		I2S1_LRCK	A21	I2S_SPKRAMP_R_LRCLK_R		OUT	44 167
		I2S1_MCK	D21	TP_PCHROM_SW_EN			
	(IPD)	I2S2_DIN	AH34	I2S_CODEC_D2R		IN	127
		I2S2_DOUT	AB34	I2S_CODEC_R2D_R		OUT	44 165
		I2S2_BCLK	AF33	I2S_CODEC_BCLK_R		OUT	44 165
		I2S2_LRCK	AH35	I2S_CODEC_LRCLK_R		OUT	44 167
		I2S2_MCK	AB33	I2S_SPKRAMP_L_MCLK_R		OUT	44 165
	(IPD)	I2S3_DIN	AD36	TP_I2S_HAWKING_D2R			
		I2S3_DOUT	AB35	I2S_CODEC1_R2D_R		BI	158 167
		I2S3_BCLK	AE36	NC_I2S_HAWKING_BCLK_R	167		
		I2S3_LRCK	W34	TP_I2S_HAWKING_LRCLK			
		I2S3_MCK	AG36	I2S_SPKRAMP_R_MCLK_R		OUT	44

PLACE_NEAR=U3900.AR7:5MM
PLACE_NEAR=U3900.AU7:5MM

R4171 20 1 2 5% 1/20W MF 201 SPI_SOCROM_MOSI OUT 43
R4172 20 1 2 5% 1/20W MF 201 SPI_SOCROM_CLK OUT 43

TPAD signals are used for board ID

BOM_COST_GROUP=SOC

PAGE TITLE
SOC ISP/I2C/UART/SPI/I2S

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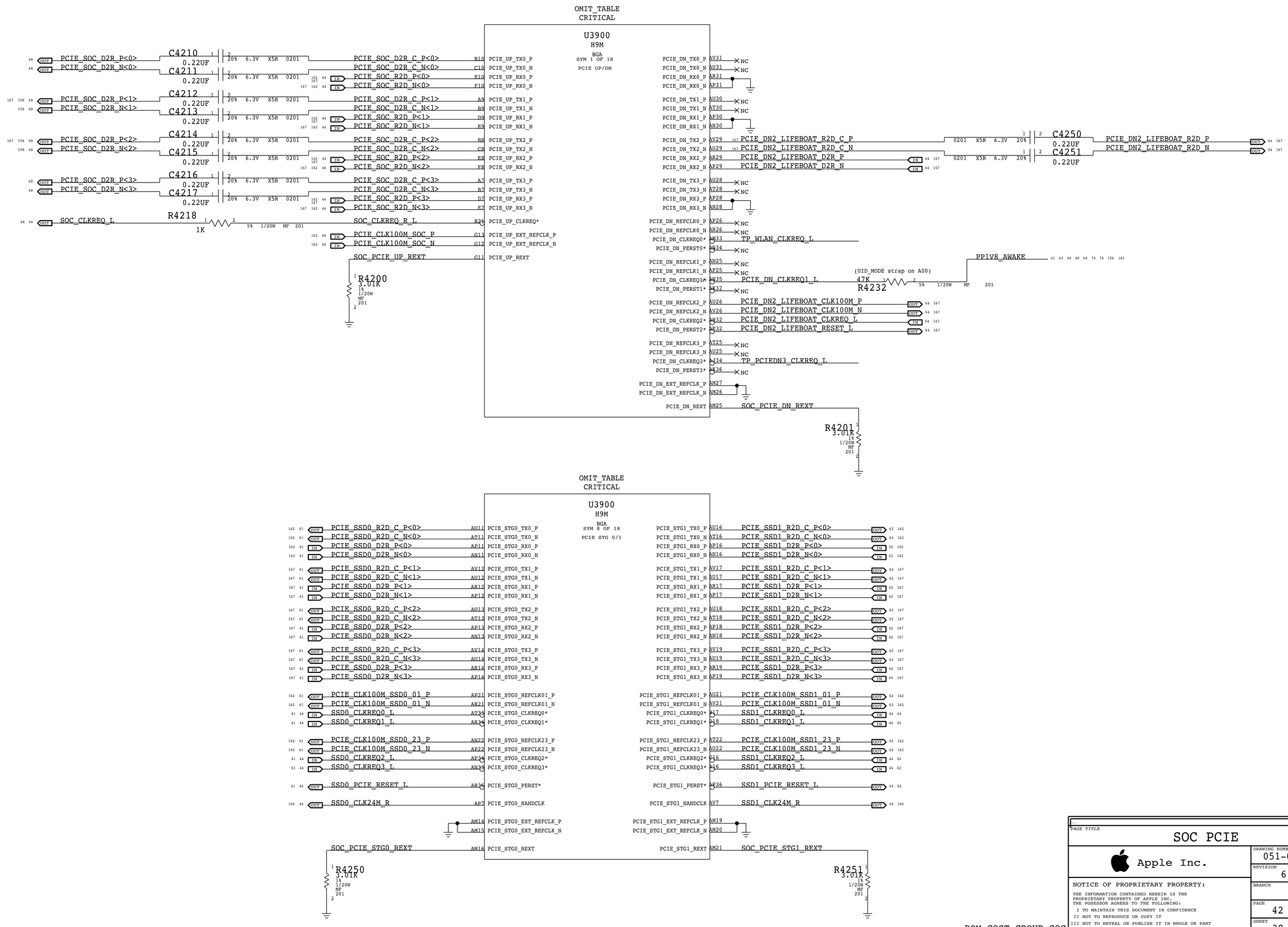

BOM_COST_GROUP=SOC

PAGE TITLE
SOC PCIE

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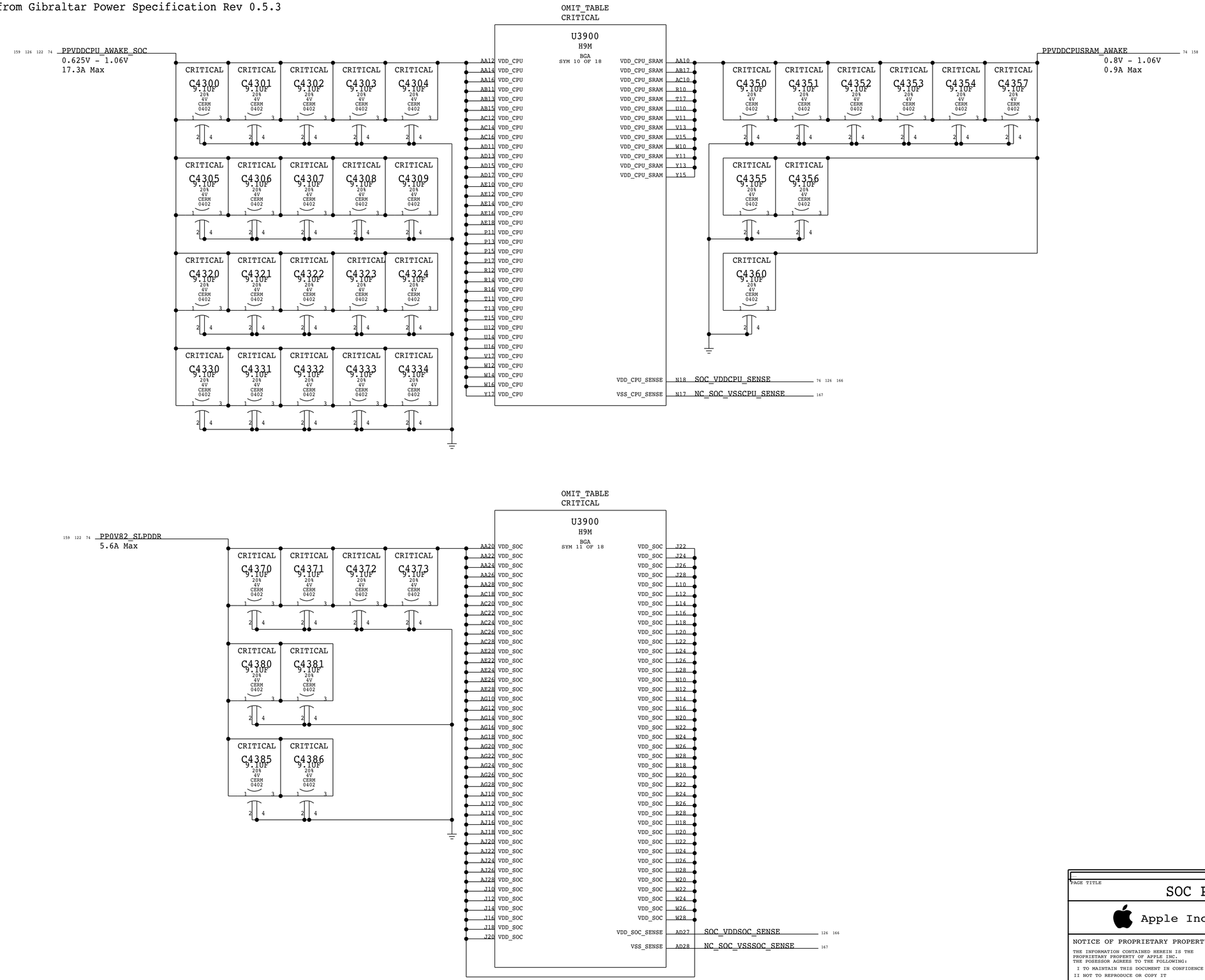
Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



BOM_COST_GROUP=SOC

PAGE TITLE
SOC POWER 1

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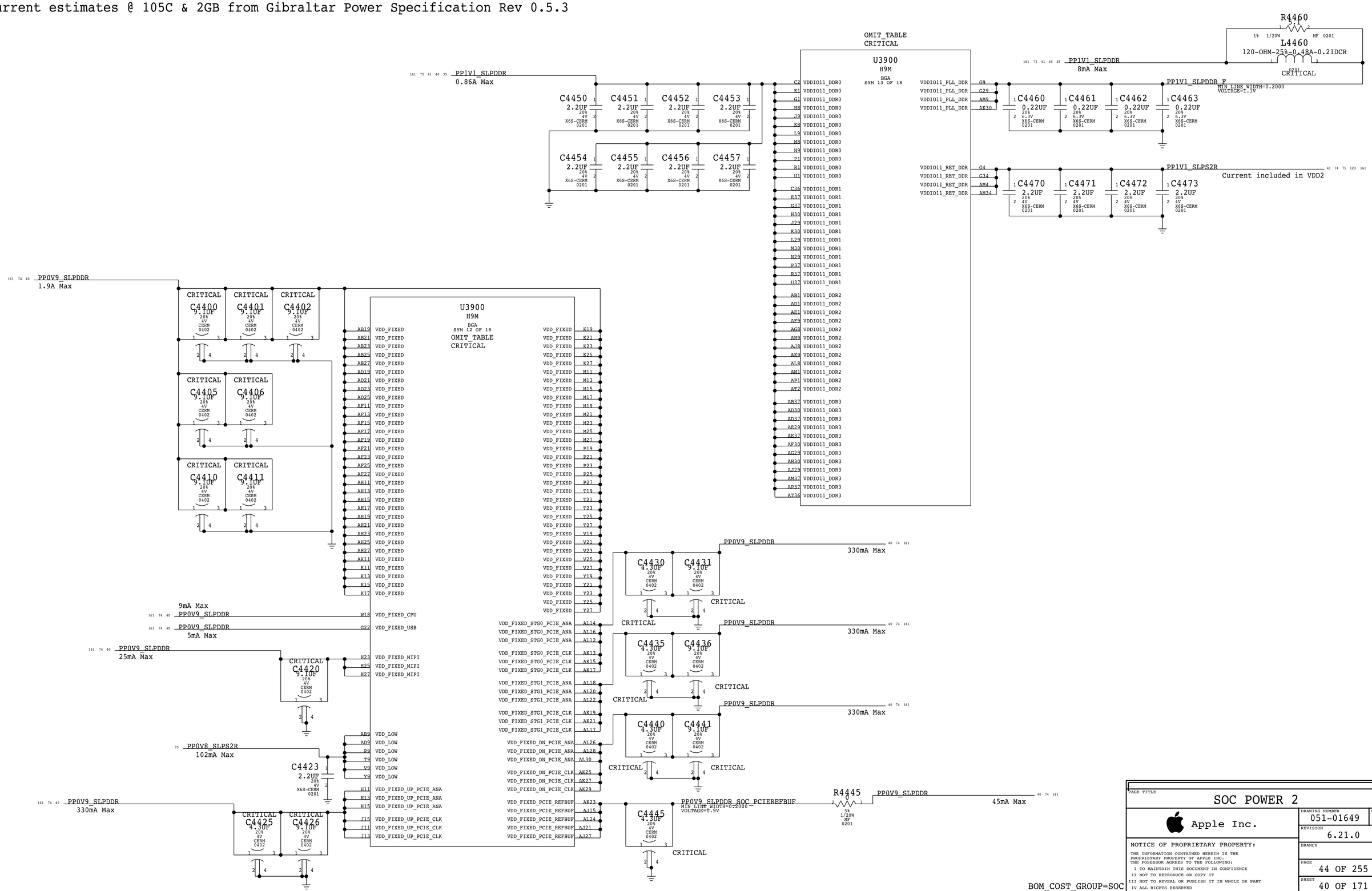

PAGE TITLE

SOC POWER 2

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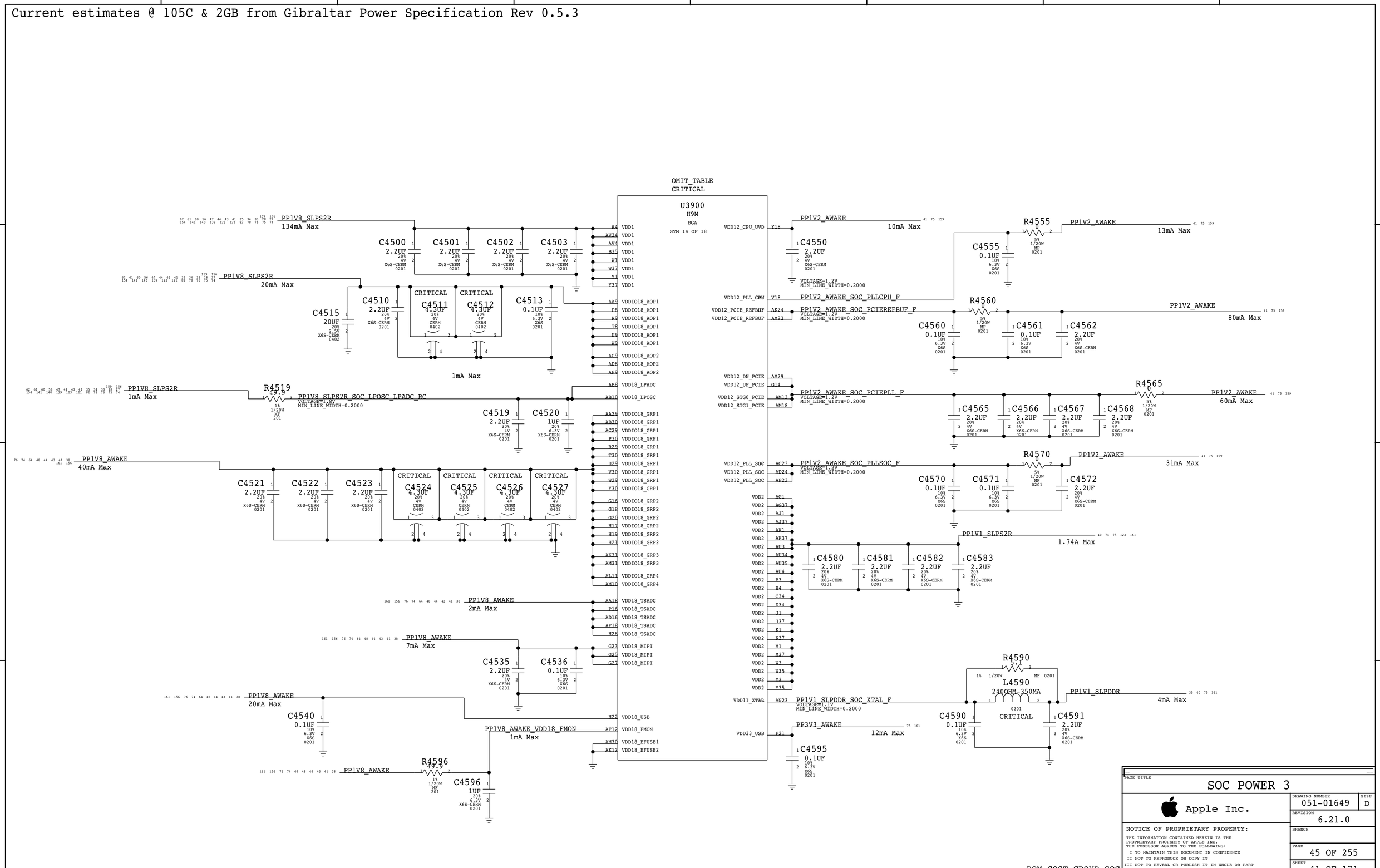

PAGE TITLE

SOC POWER 3

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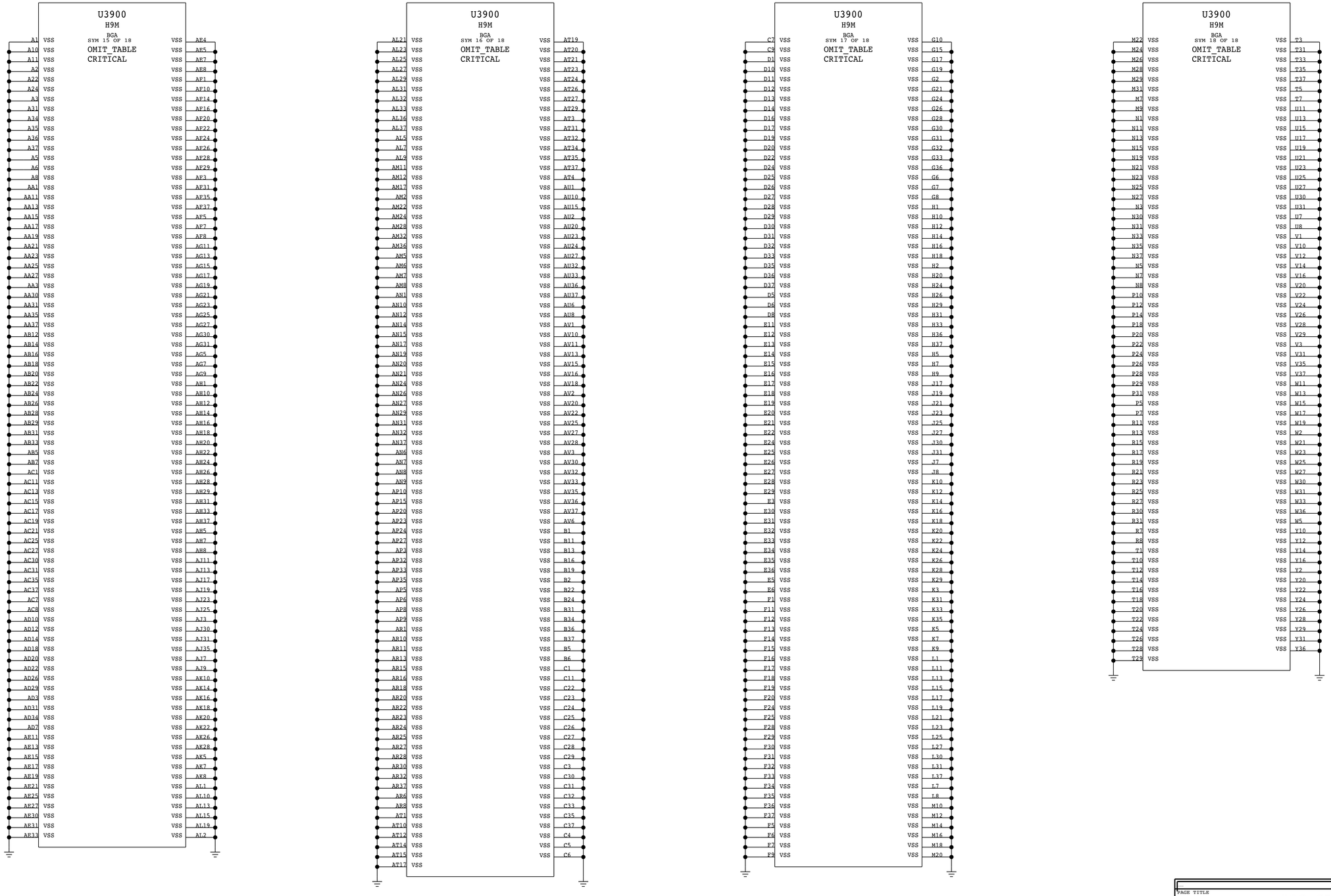

BOM_COST_GROUP=SOC

PAGE TITLE

SOC GROUND

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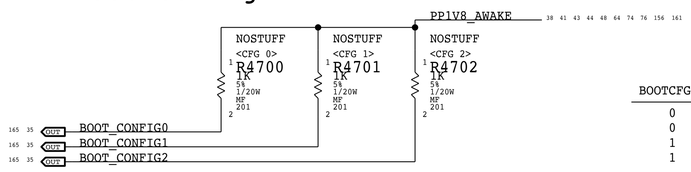
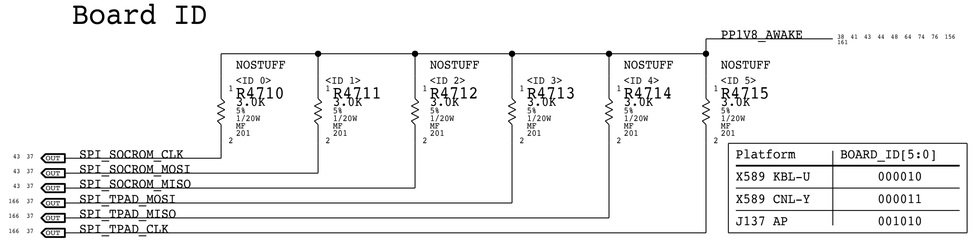
Boot Config



BOOTCFG0	Test Mode
0	Disabled
1	Enabled

BOOTCFG2	BOOTCFG1	Frequency
0	0	40 MHz
0	1	6 MHz
1	0	24 MHz
1	1	Invalid

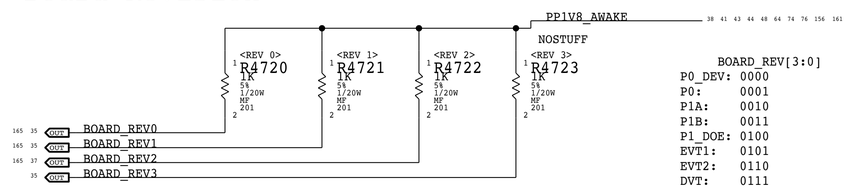
Board ID



Platform	BOARD_ID[5:0]
X589 KBL-U	000010
X589 CNL-Y	000011
J137 AP	001010

SEE <RDAR://PROBLEM/28088184> FOR PROJECT ASSIGNMENTS

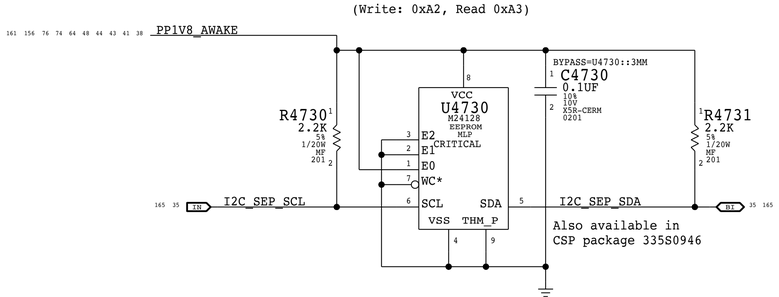
Board Revision



BOARD_REV[3:0]	
P0_DEV:	0000
P0:	0001
P1A:	0010
P1B:	0011
P1_DOE:	0100
EVT1:	0101
EVT2:	0110
DVT:	0111

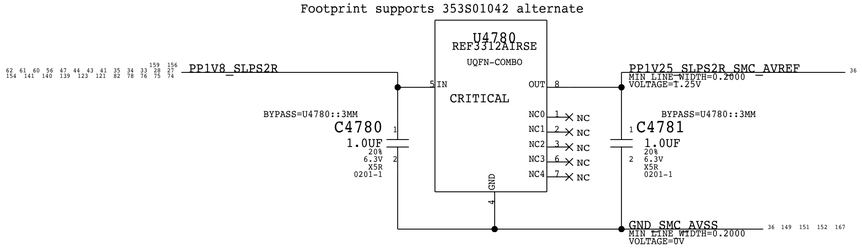
SEP EEPROM

(Write: 0xA2, Read 0xA3)

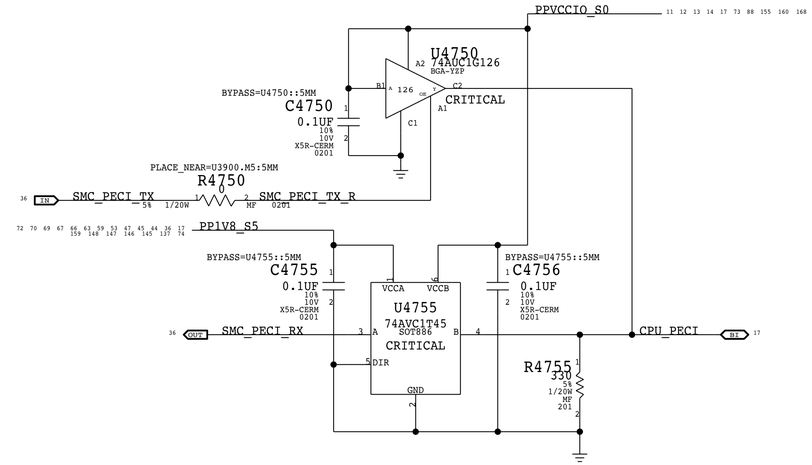


SMC AVREF Supply

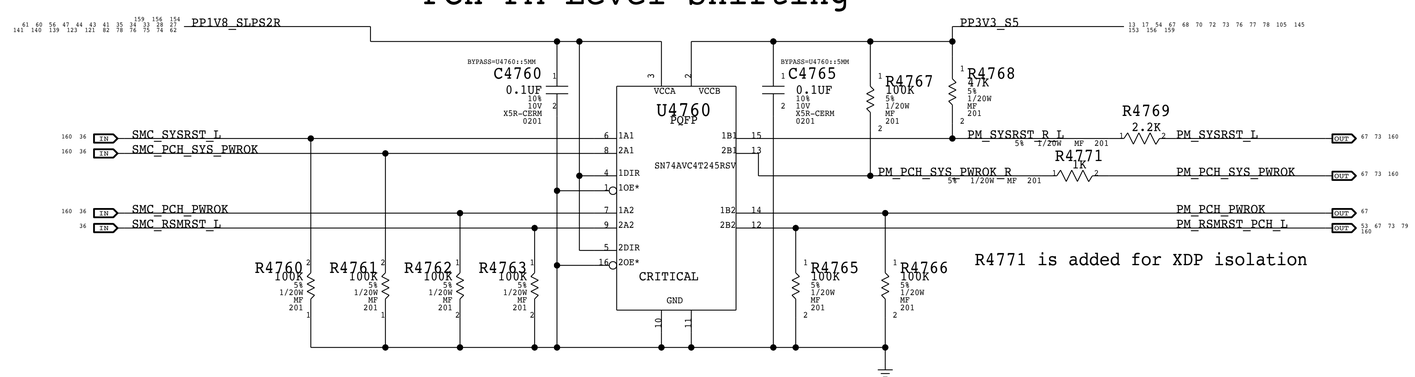
Footprint supports 353S01042 alternate



PECI Level Shifting

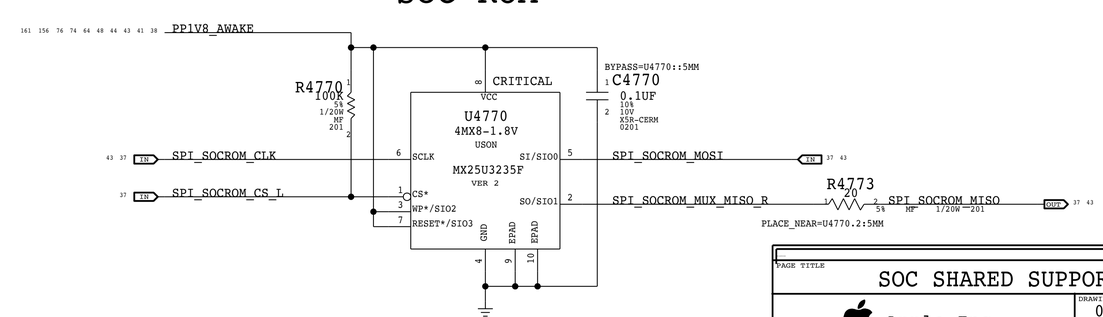


PCH PM Level Shifting



R4771 is added for XDP isolation

SoC ROM



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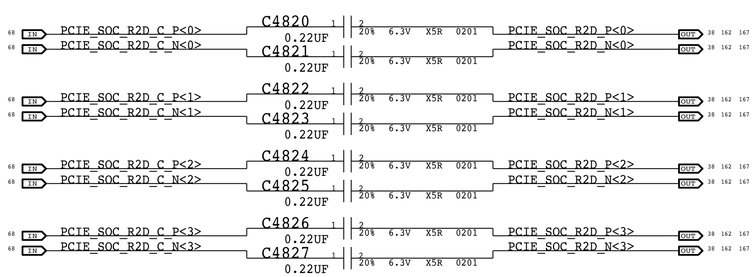
SMC ADC Assignments

Desktop Assignments

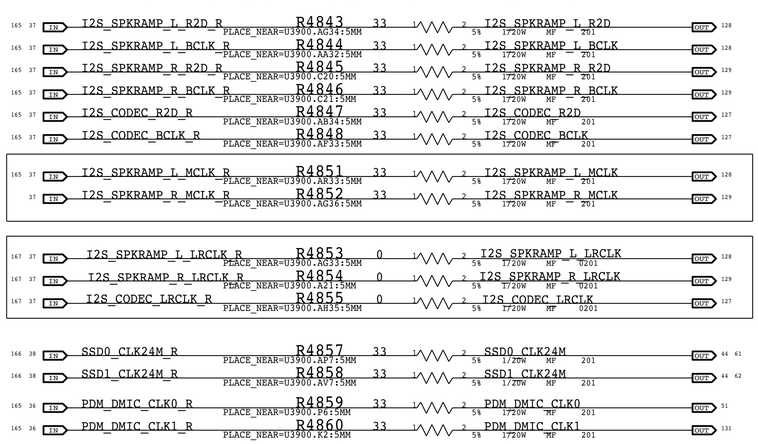
GPU_AUX	ADC0
GPU_CORE	ADC1
12V VSNS	ADC2
12V ISNS	ADC3
Same	ADC4-7

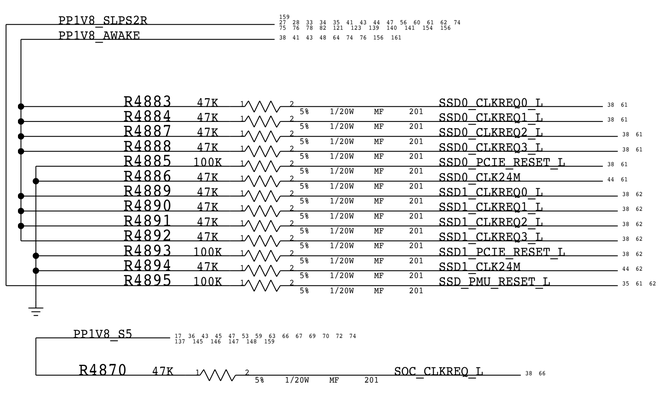
PCIe Up R2D AC Caps

(All Caps)



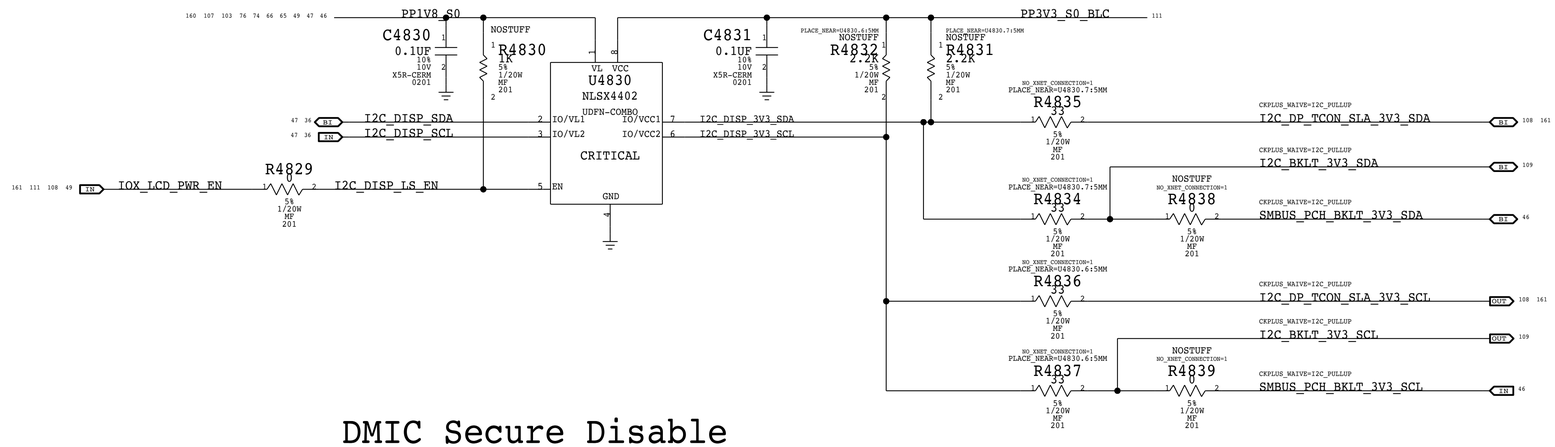
GPIO Source Termination



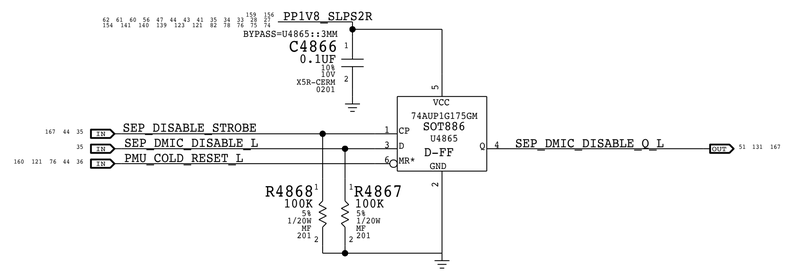


SMC I2C "3" LEVEL SHIFTING

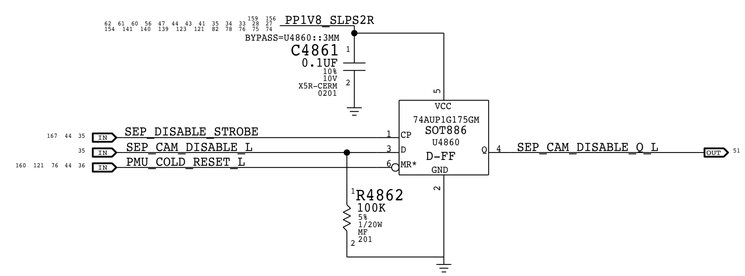
NOTE: LEVEL SHIFTER CONNECTIONS NEED TO BE FIXED PENDING ON-SEMI'S REPLY
Added options to connect PCH to BLC



DMIC Secure Disable



FTCAM Secure Disable



BOM_COST_GROUP=SOC

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SOC PROJECT SUPPORT 1

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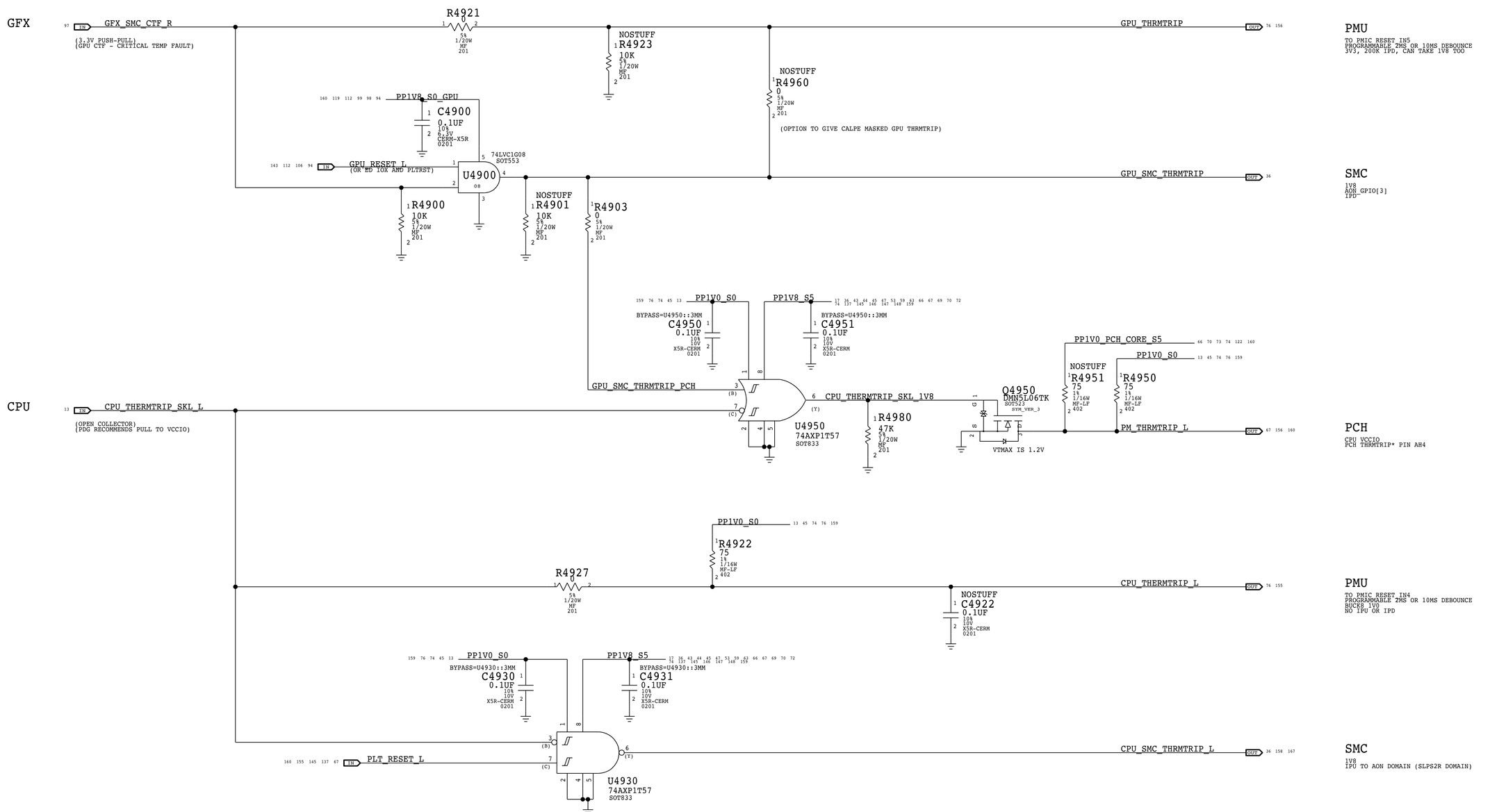
PLATFORM THERMTRIP SUPPORT

INTENTION IS PMU GETS CPU/GPU THERMTRIP SO THAT IN THE CASE SMC HAS ISSUES, CALPE CAN STILL BRING DOWN THE SYSTEM GRACEFULLY

CALPE HAS AN INTERNAL DEBOUNCE, SMC DOESN'T, SO SMC VERSIONS OF THERMTRIP ARE MASKED

PCH GETS A COMBINED CPU/GPU THERMTRIP, SO IF EITHER ASSERTS, PCH SHOULD BRING DOWN THE SYSTEM GRACEFULLY



BOM_COST_GROUP=PLATFORM POWER

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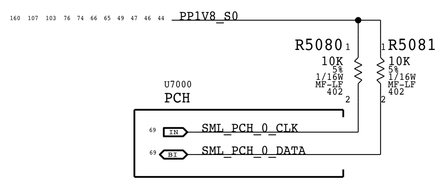
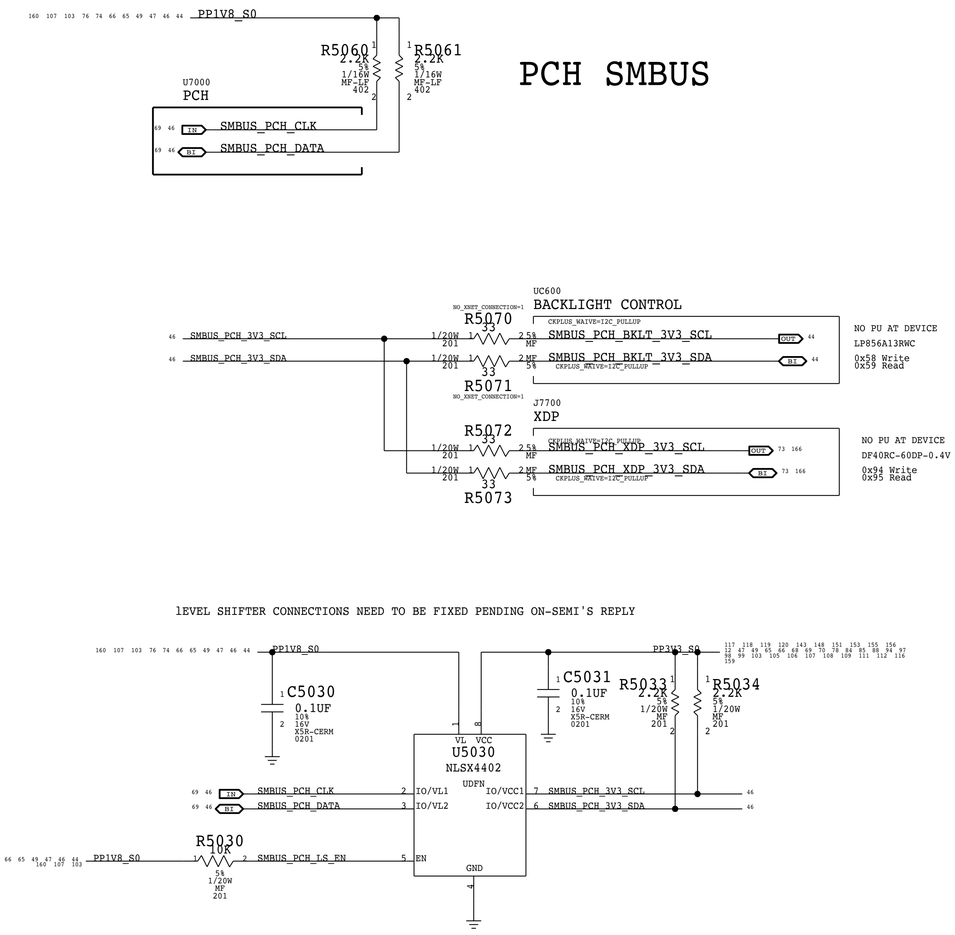
PCH SML 0



PCH SMBUS



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

I2C PCH

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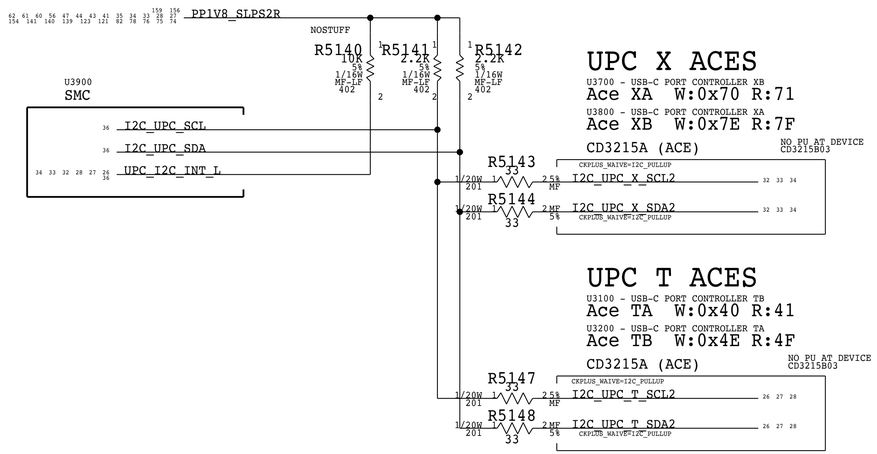
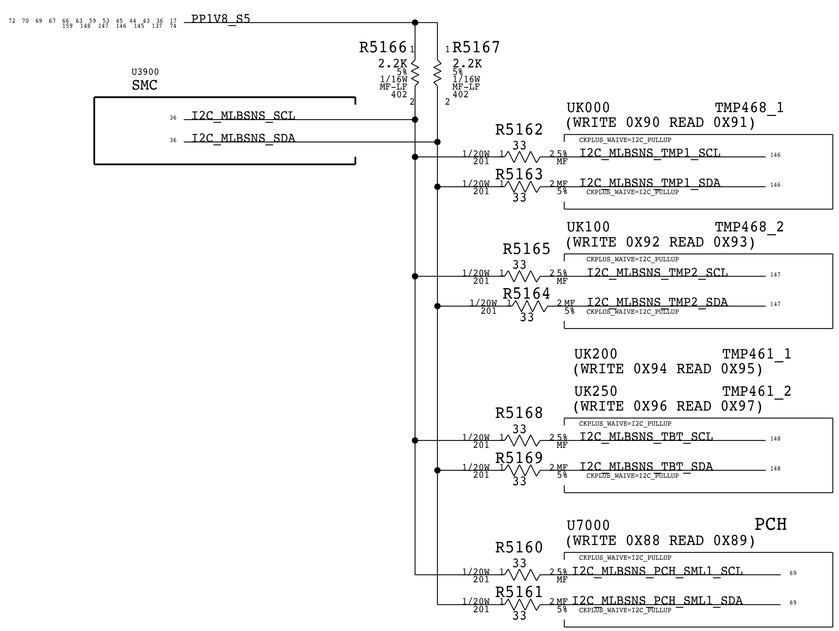
FOLLOW UP: NEED LEVEL SHIFTER

SMC I2C "0" CONNECTIONS

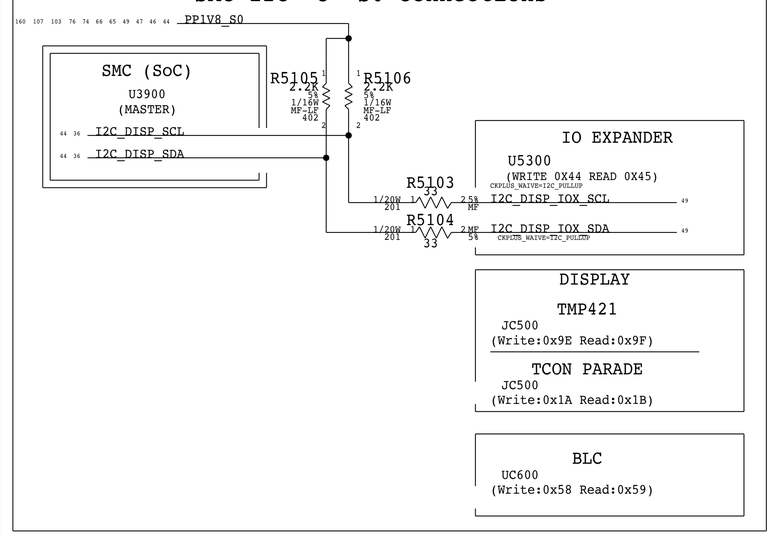


I2C traces need to be routed through the ACEs with no branches

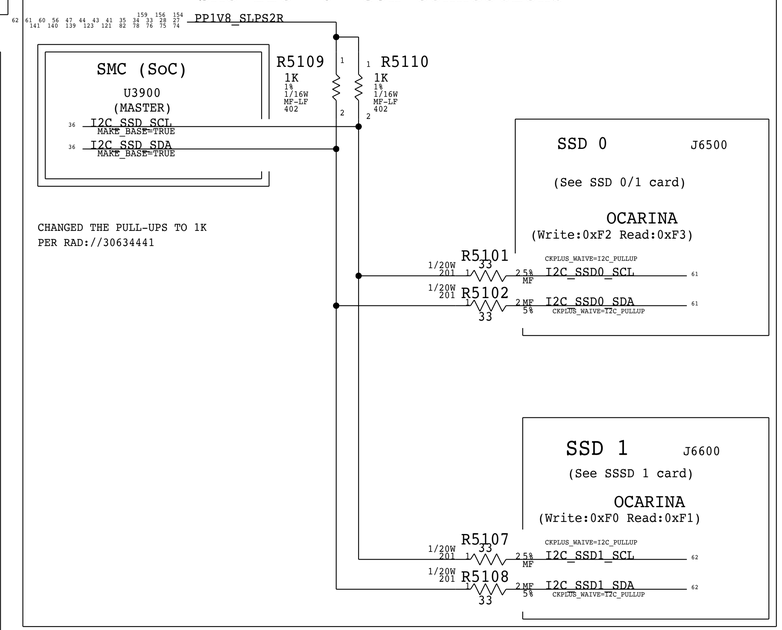
SMC I2C "2" CONNECTIONS



SMC I2C "3" S0 Connections

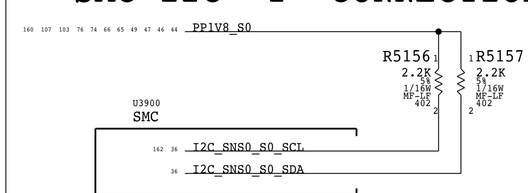


SMC I2C "6" G3H Connections

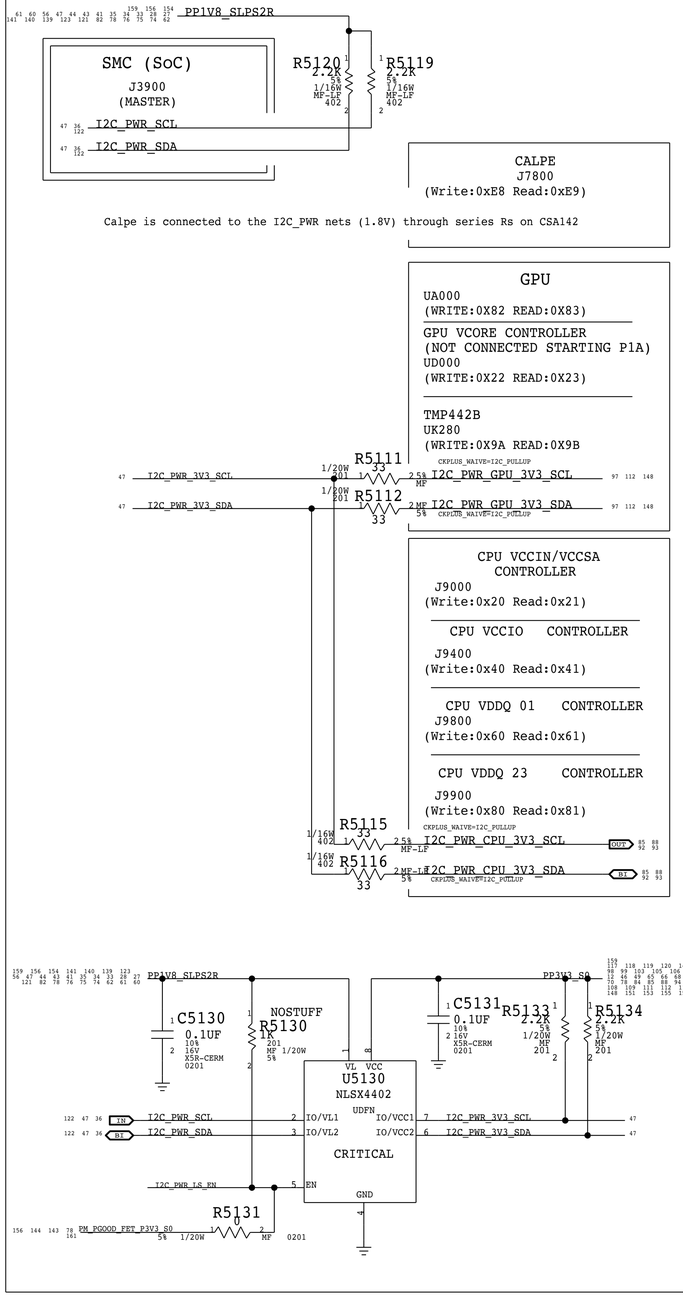


CHANGED THE PULL-UPS TO 1K
PER RAD://30634441

SMC I2C "1" CONNECTIONS



SMC I2C "4" G3H Connections



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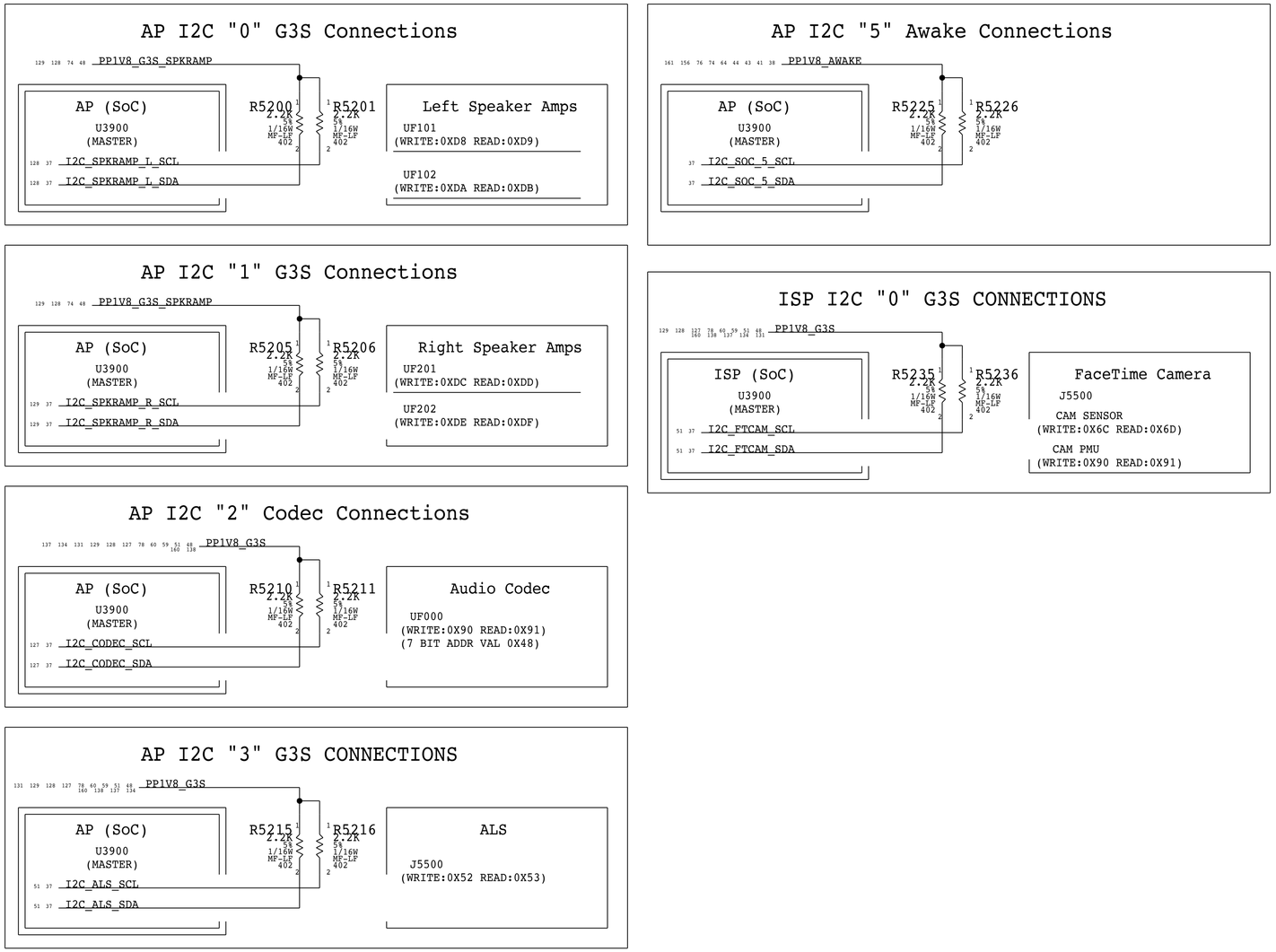

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PAGE TITLE

I2C SOC 2

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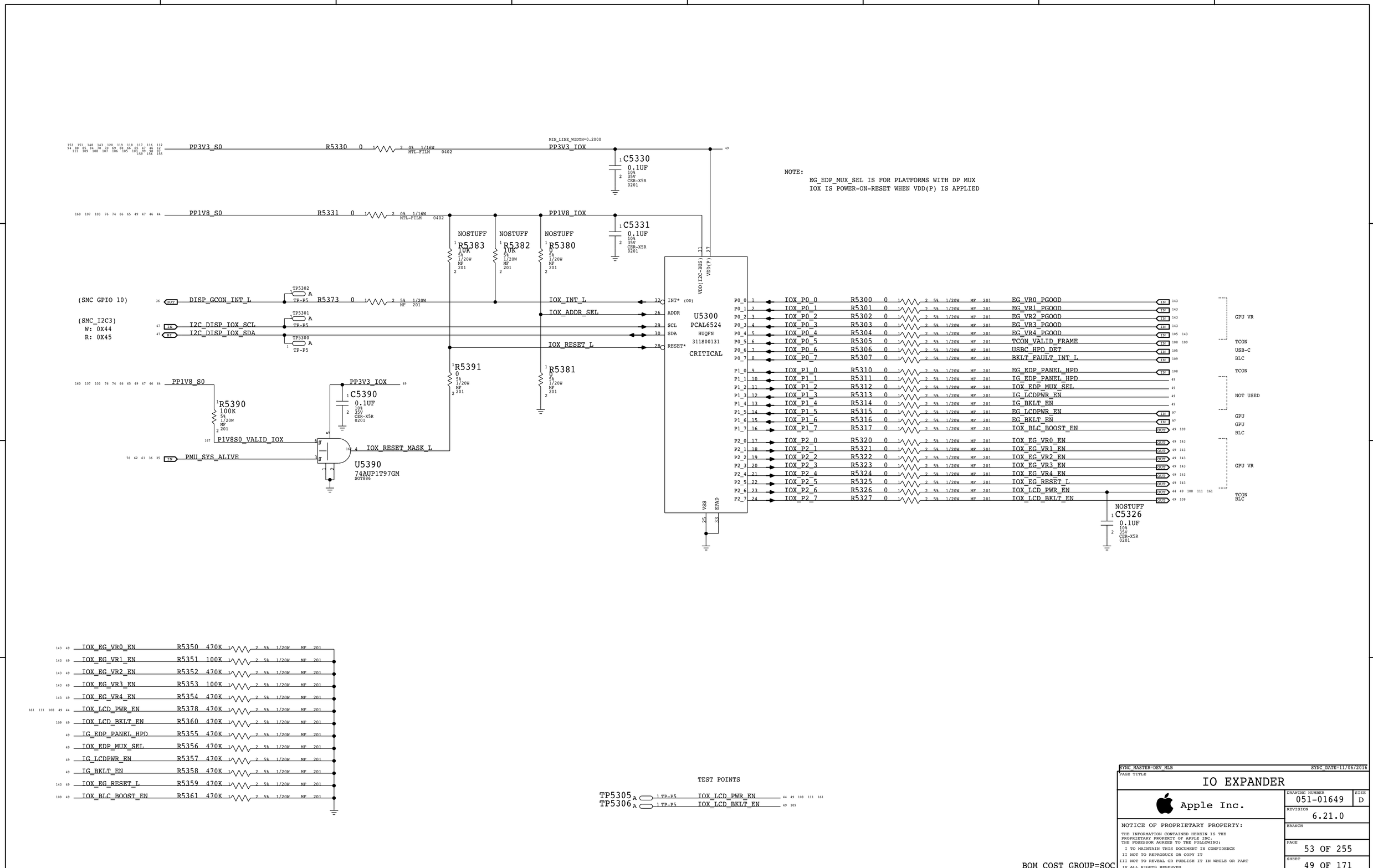
PP3V3_S0
R5330 0
MIN_LINE_WIDTH=0.2000
PP3V3_IOX
C5330 0.1UF
PP1V8_S0
R5331 0
PP1V8_IOX
C5331 0.1UF
NOSTUFF
R5383 1UK
R5382 1UK
R5380 0
(SMC GPIO 10)
DISP_GCON_INT_L
R5373 0
IOX_INT_L
IOX_ADDR_SEL
(SMC_I2C3)
W: 0X44
R: 0X45
I2C_DISP_IOX_SCL
I2C_DISP_IOX_SDA
IOX_RESET_L
R5391 0
R5381 0
R5390 100K
C5390 0.1UF
P1V8S0_VALID_IOX
PMU_SYS_ALIVE
IOX_RESET_MASK_L
U5390
74AUP1T97GM
SOT886
U5300
PCAL6524
HUQFN
311S00131
CRITICAL
INT* (OD)
ADDR
SCL
SDA
RESET*
VDD(I2C-BUS)
VDD(P)
VSS
EPAD
NOTE:
EG_EDP_MUX_SEL IS FOR PLATFORMS WITH DP MUX
IOX IS POWER-ON-RESET WHEN VDD(P) IS APPLIED
IOX_P0_0 R5300 EG_VR0_PGOOD
IOX_P0_1 R5301 EG_VR1_PGOOD
IOX_P0_2 R5302 EG_VR2_PGOOD
IOX_P0_3 R5303 EG_VR3_PGOOD
IOX_P0_4 R5304 EG_VR4_PGOOD
IOX_P0_5 R5305 TCON_VALID_FRAME
IOX_P0_6 R5306 USBC_HPD_DET
IOX_P0_7 R5307 BKLT_FAULT_INT_L
IOX_P1_0 R5310 EG_EDP_PANEL_HPD
IOX_P1_1 R5311 IG_EDP_PANEL_HPD
IOX_P1_2 R5312 IOX_EDP_MUX_SEL
IOX_P1_3 R5313 IG_LCDPWR_EN
IOX_P1_4 R5314 IG_BKLT_EN
IOX_P1_5 R5315 EG_LCDPWR_EN
IOX_P1_6 R5316 EG_BKLT_EN
IOX_P1_7 R5317 IOX_BLC_BOOST_EN
IOX_P2_0 R5320 IOX_EG_VR0_EN
IOX_P2_1 R5321 IOX_EG_VR1_EN
IOX_P2_2 R5322 IOX_EG_VR2_EN
IOX_P2_3 R5323 IOX_EG_VR3_EN
IOX_P2_4 R5324 IOX_EG_VR4_EN
IOX_P2_5 R5325 IOX_EG_RESET_L
IOX_P2_6 R5326 IOX_LCD_PWR_EN
IOX_P2_7 R5327 IOX_LCD_BKLT_EN
NOSTUFF
C5326 0.1UF
GPU VR
TCON
USB-C
BLC
TCON
NOT USED
GPU
GPU
BLC
GPU VR
TCON
BLC
IOX_EG_VR0_EN R5350 470K
IOX_EG_VR1_EN R5351 100K
IOX_EG_VR2_EN R5352 470K
IOX_EG_VR3_EN R5353 100K
IOX_EG_VR4_EN R5354 470K
IOX_LCD_PWR_EN R5378 470K
IOX_LCD_BKLT_EN R5360 470K
IG_EDP_PANEL_HPD R5355 470K
IOX_EDP_MUX_SEL R5356 470K
IG_LCDPWR_EN R5357 470K
IG_BKLT_EN R5358 470K
IOX_EG_RESET_L R5359 470K
IOX_BLC_BOOST_EN R5361 470K
TEST POINTS
TP5305 IOX_LCD_PWR_EN
TP5306 IOX_LCD_BKLT_EN
BOM_COST_GROUP=SOC
SYNC_MASTER=DEV_MLB
SYNC_DATE=11/06/2016
PAGE TITLE
IO EXPANDER
Apple Inc.
DRAWING NUMBER 051-01649
SIZE D
REVISION 6.21.0
BRANCH
PAGE 53 OF 255
SHEET 49 OF 171
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PAGE TITLE

IO EXPANDER SUPPORT

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BOM_COST_GROUP=SOC

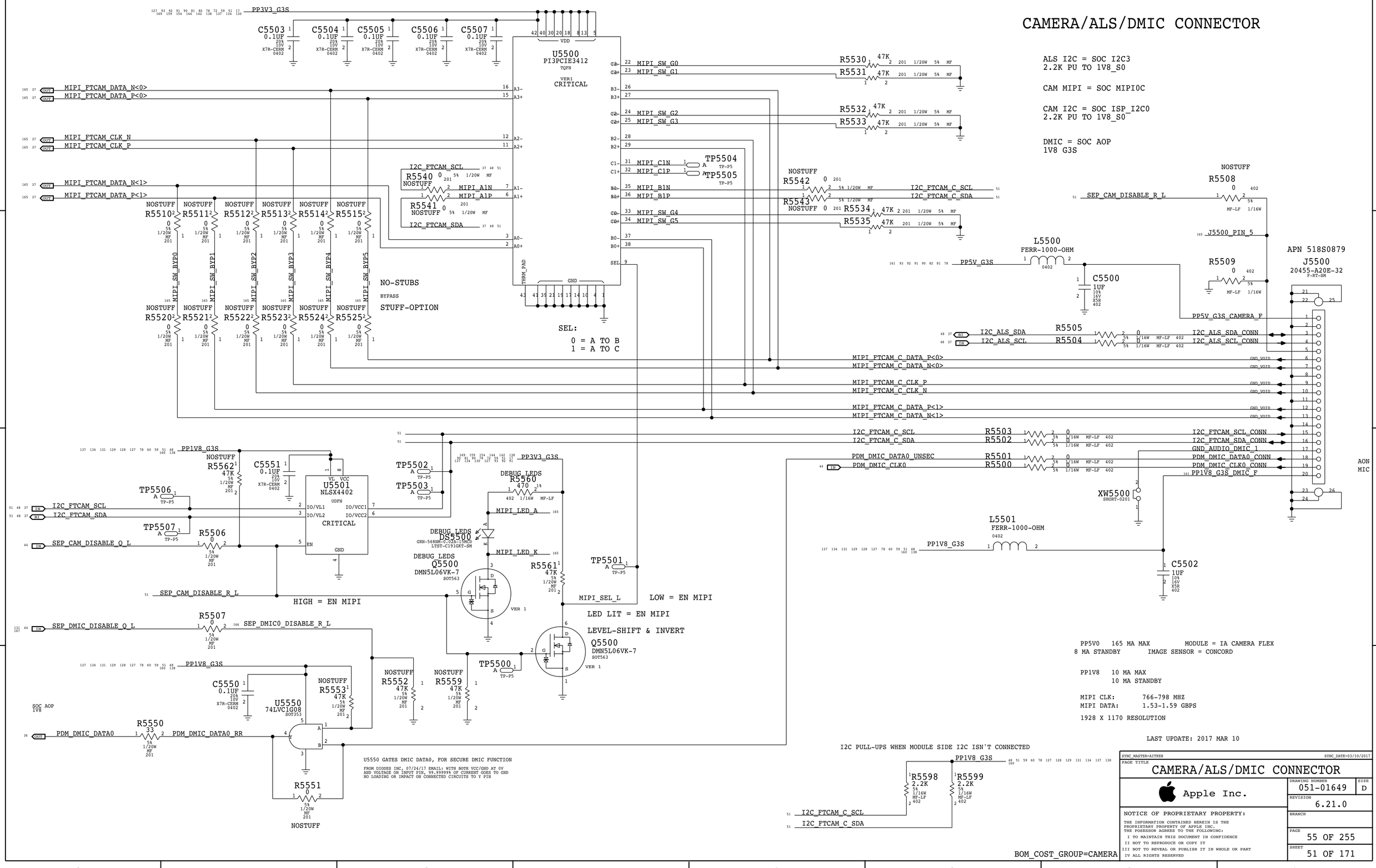
CAMERA/ALS/DMIC CONNECTOR

ALS I2C = SOC I2C3
2.2K PU TO 1V8_S0

CAM MIPI = SOC MIPI0C

CAM I2C = SOC ISP_I2C0
2.2K PU TO 1V8_S0

DMIC = SOC AOP
1V8 G3S



PP5V0 165 MA MAX MODULE = IA CAMERA FLEX
8 MA STANDBY IMAGE SENSOR = CONCORD

PP1V8 10 MA MAX
10 MA STANDBY

MIPI CLK: 766-798 MHZ
MIPI DATA: 1.53-1.59 GBPS

1928 X 1170 RESOLUTION

LAST UPDATE: 2017 MAR 10

SYNC_MASTER=AITKEN SYNC_DATE=03/10/2017

PAGE TITLE
CAMERA/ALS/DMIC CONNECTOR

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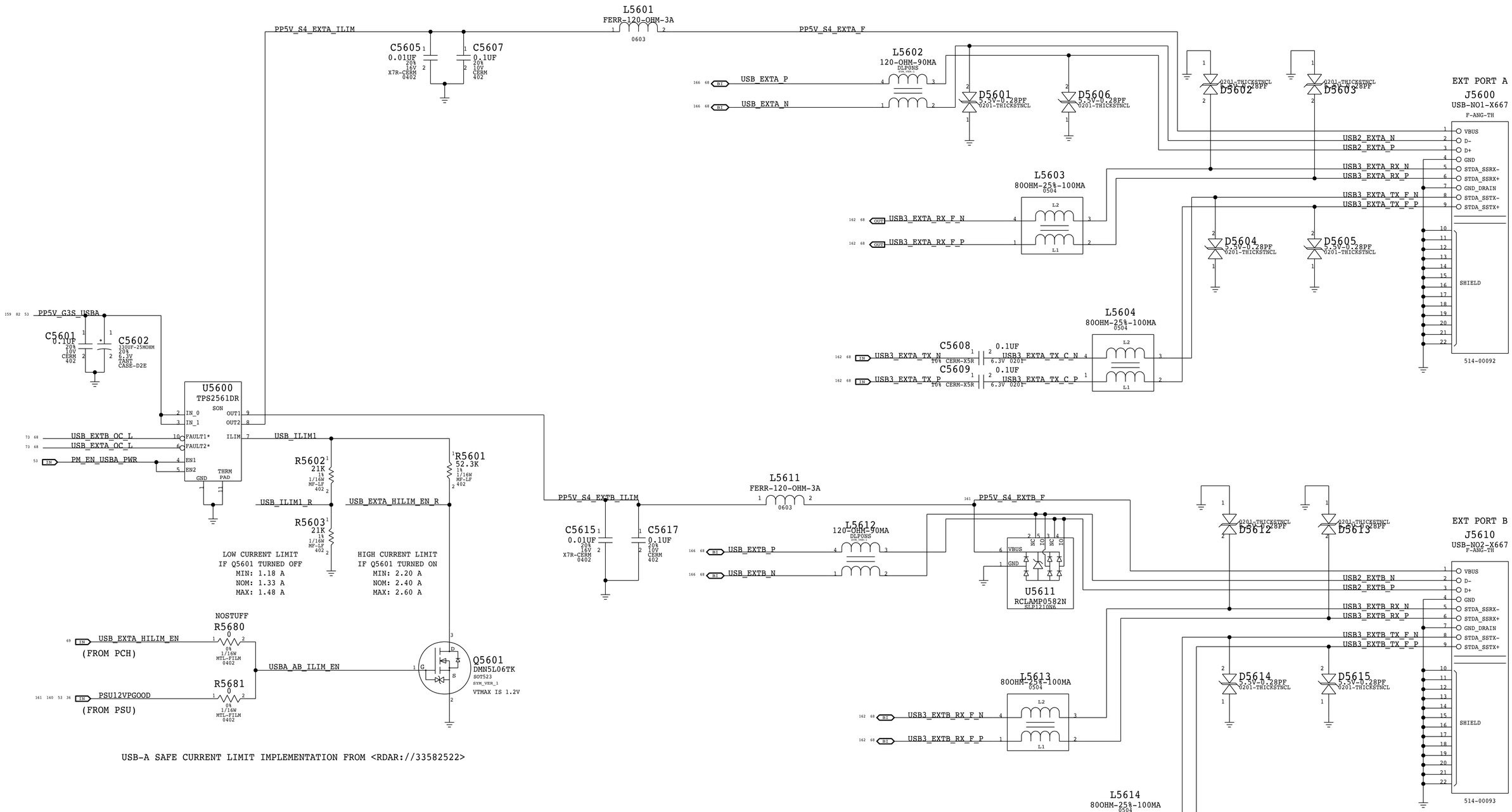

BOM_COST_GROUP=USB-A

SYNC_MASTER=ANDRES SYNC_DATE=02/13/2017

PAGE TITLE

USB-A EXTERNAL USB PORTS A & B

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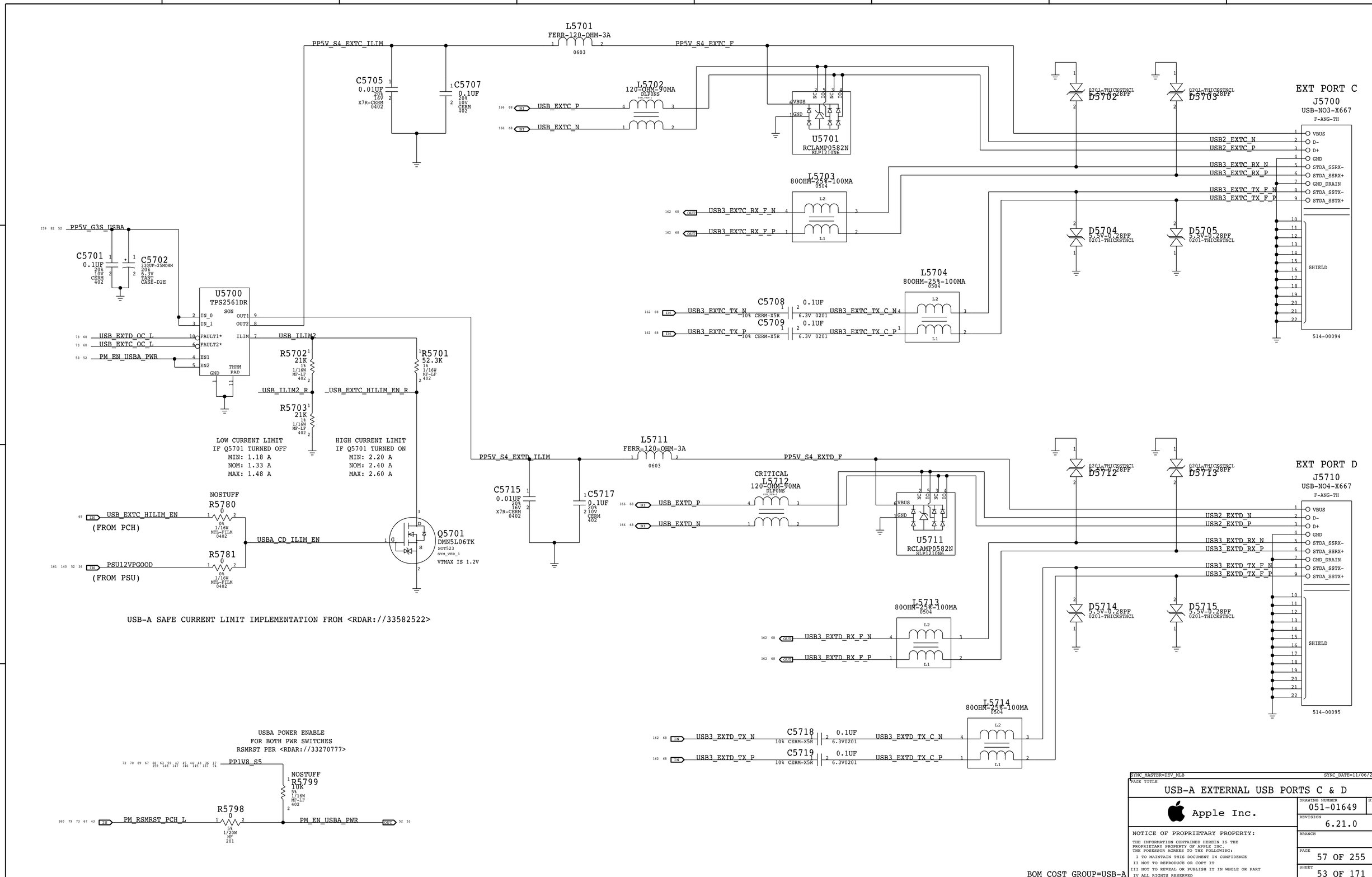
L5701
FERR-120-OHM-3A
0603
PP5V_S4_EXTC_ILIM
PP5V_S4_EXTC_F
C5705
0.01UF
20%
16V
X7R-CERM
0402
C5707
0.1UF
20%
10V
CERM
402
L5702
120-OHM-90MA
DLP0NS
USB_EXTC_P
USB_EXTC_N
U5701
RCLAMP0582N
SLP1210N6
D5702
D5703
0201-THICKSTNCL
5.5V-0.28PF
EXT PORT C
J5700
USB-NO3-X667
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
514-00094
USB2_EXTC_N
USB2_EXTC_P
USB3_EXTC_RX_N
USB3_EXTC_RX_P
USB3_EXTC_TX_F_N
USB3_EXTC_TX_F_P
L5703
80OHM-25%-100MA
0504
USB3_EXTC_RX_F_N
USB3_EXTC_RX_F_P
D5704
D5705
PP5V_G3S_USBA
C5701
0.1UF
20%
10V
CERM
402
C5702
330UF-25MOHM
20%
6.3V
TANT
CASE-D2E
U5700
TPS2561DR
SON
IN_0
IN_1
FAULT1*
FAULT2*
EN1
EN2
OUT1
OUT2
ILIM
GND
THRM PAD
USB_EXTD_OC_L
USB_EXTC_OC_L
PM_EN_USBA_PWR
USB_ILIM2
R5702
21K
1%
1/16W
MF-LF
402
R5701
52.3K
USB_ILIM2_R
USB_EXTC_HILIM_EN_R
R5703
LOW CURRENT LIMIT
IF Q5701 TURNED OFF
MIN: 1.18 A
NOM: 1.33 A
MAX: 1.48 A
HIGH CURRENT LIMIT
IF Q5701 TURNED ON
MIN: 2.20 A
NOM: 2.40 A
MAX: 2.60 A
L5704
80OHM-25%-100MA
0504
C5708
0.1UF
10% CERM-X5R
6.3V 0201
C5709
USB3_EXTC_TX_N
USB3_EXTC_TX_P
USB3_EXTC_TX_C_N
USB3_EXTC_TX_C_P
L5711
FERR-120-OHM-3A
0603
PP5V_S4_EXTD_ILIM
PP5V_S4_EXTD_F
C5715
0.01UF
20%
16V
X7R-CERM
0402
C5717
0.1UF
20%
10V
CERM
402
CRITICAL
L5712
120-OHM-90MA
DLP0NS
USB_EXTD_P
USB_EXTD_N
U5711
RCLAMP0582N
SLP1210N6
D5712
D5713
EXT PORT D
J5710
USB-NO4-X667
F-ANG-TH
USB2_EXTD_N
USB2_EXTD_P
USB3_EXTD_RX_N
USB3_EXTD_RX_P
USB3_EXTD_TX_F_N
USB3_EXTD_TX_F_P
514-00095
L5713
80OHM-25%-100MA
0504
USB3_EXTD_RX_F_N
USB3_EXTD_RX_F_P
D5714
D5715
L5714
80OHM-25%-100MA
0504
C5718
0.1UF
10% CERM-X5R
6.3V0201
C5719
USB3_EXTD_TX_N
USB3_EXTD_TX_P
USB3_EXTD_TX_C_N
USB3_EXTD_TX_C_P
NOSTUFF
R5780
0
0%
1/16W
MTL-FILM
0402
USB_EXTC_HILIM_EN
(FROM PCH)
R5781
PSU12VPGOOD
(FROM PSU)
USBA_CD_ILIM_EN
Q5701
DMN5L06TK
SOT523
SYM_VER_1
VTMAX IS 1.2V
USB-A SAFE CURRENT LIMIT IMPLEMENTATION FROM <RDAR://33582522>
USBA POWER ENABLE
FOR BOTH PWR SWITCHES
RSMRST PER <RDAR://33270777>
PP1V8_S5
NOSTUFF
R5799
10K
5%
1/16W
MF-LF
402
R5798
5%
1/20W
MF
201
PM_RSMRST_PCH_L
PM_EN_USBA_PWR
BOM_COST_GROUP=USB-A
SYNC_MASTER=DEV_MLB
SYNC_DATE=11/06/2016
PAGE TITLE
USB-A EXTERNAL USB PORTS C & D
Apple Inc.
DRAWING NUMBER
051-01649
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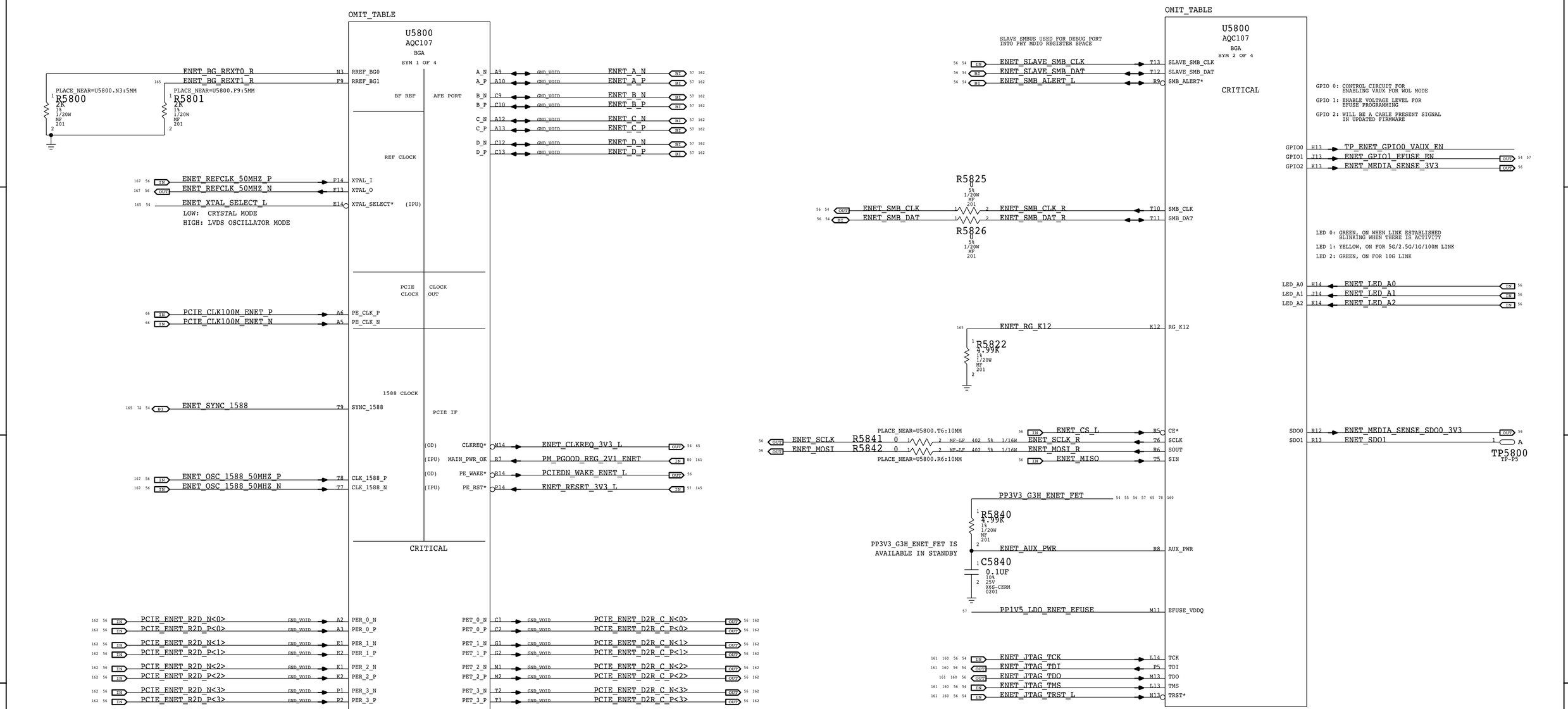
OMIT_TABLE
U5800
AQC107
BGA
SYM 1 OF 4
ENET_BG_REXT0_R
ENET_BG_REXT1_R
PLACE_NEAR=U5800.N3:5MM
PLACE_NEAR=U5800.F9:5MM
R5800
2K
1%
1/20W
MF
201
R5801
2K
1%
1/20W
MF
201
RREF_BG0
RREF_BG1
BF REF
AFE PORT
A_N
A_P
B_N
B_P
C_N
C_P
D_N
D_P
ENET_A_N
ENET_A_P
ENET_B_N
ENET_B_P
ENET_C_N
ENET_C_P
ENET_D_N
ENET_D_P
REF CLOCK
ENET_REFCLK_50MHZ_P
ENET_REFCLK_50MHZ_N
XTAL_I
XTAL_O
ENET_XTAL_SELECT_L
XTAL_SELECT* (IPU)
LOW: CRYSTAL MODE
HIGH: LVDS OSCILLATOR MODE
PCIE CLOCK
CLOCK OUT
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
PE_CLK_P
PE_CLK_N
1588 CLOCK
ENET_SYNC_1588
SYNC_1588
PCIE IF
CLKREQ*
MAIN_PWR_OK
PE_WAKE*
PE_RST*
ENET_CLKREQ_3V3_L
PM_PGOOD_REG_2V1_ENET
PCIEDN_WAKE_ENET_L
ENET_RESET_3V3_L
ENET_OSC_1588_50MHZ_P
ENET_OSC_1588_50MHZ_N
CLK_1588_P
CLK_1588_N
CRITICAL
PCIE_ENET_R2D_N<0>
PCIE_ENET_R2D_P<0>
PCIE_ENET_R2D_N<1>
PCIE_ENET_R2D_P<1>
PCIE_ENET_R2D_N<2>
PCIE_ENET_R2D_P<2>
PCIE_ENET_R2D_N<3>
PCIE_ENET_R2D_P<3>
PER_0_N
PER_0_P
PER_1_N
PER_1_P
PER_2_N
PER_2_P
PER_3_N
PER_3_P
PET_0_N
PET_0_P
PET_1_N
PET_1_P
PET_2_N
PET_2_P
PET_3_N
PET_3_P
PCIE_ENET_D2R_C_N<0>
PCIE_ENET_D2R_C_P<0>
PCIE_ENET_D2R_C_N<1>
PCIE_ENET_D2R_C_P<1>
PCIE_ENET_D2R_C_N<2>
PCIE_ENET_D2R_C_P<2>
PCIE_ENET_D2R_C_N<3>
PCIE_ENET_D2R_C_P<3>
OMIT_TABLE
U5800
AQC107
BGA
SYM 2 OF 4
SLAVE SMBUS USED FOR DEBUG PORT
INTO PHY MDIO REGISTER SPACE
ENET_SLAVE_SMB_CLK
ENET_SLAVE_SMB_DAT
ENET_SMB_ALERT_L
SLAVE_SMB_CLK
SLAVE_SMB_DAT
SMB_ALERT*
CRITICAL
GPIO 0: CONTROL CIRCUIT FOR
ENABLING VAUX FOR WOL MODE
GPIO 1: ENABLE VOLTAGE LEVEL FOR
EFUSE PROGRAMMING
GPIO 2: WILL BE A CABLE PRESENT SIGNAL
IN UPDATED FIRMWARE
GPIO0
GPIO1
GPIO2
TP_ENET_GPIO0_VAUX_EN
ENET_GPIO1_EFUSE_EN
ENET_MEDIA_SENSE_3V3
R5825
0
5%
1/20W
MF
201
R5826
0
5%
1/20W
MF
201
ENET_SMB_CLK
ENET_SMB_DAT
ENET_SMB_CLK_R
ENET_SMB_DAT_R
SMB_CLK
SMB_DAT
LED 0: GREEN, ON WHEN LINK ESTABLISHED
BLINKING WHEN THERE IS ACTIVITY
LED 1: YELLOW, ON FOR 5G/2.5G/1G/100M LINK
LED 2: GREEN, ON FOR 10G LINK
LED_A0
LED_A1
LED_A2
ENET_LED_A0
ENET_LED_A1
ENET_LED_A2
ENET_RG_K12
RG_K12
R5822
4.99K
1%
1/20W
MF
201
PLACE_NEAR=U5800.T6:10MM
PLACE_NEAR=U5800.R6:10MM
ENET_SCLK
ENET_MOSI
R5841
R5842
0
MF-LF
402
5%
1/16W
ENET_CS_L
ENET_SCLK_R
ENET_MOSI_R
ENET_MISO
CE*
SCLK
SOUT
SIN
SDO0
SDO1
ENET_MEDIA_SENSE_SDO0_3V3
ENET_SDO1
TP5800
TF-P5
PP3V3_G3H_ENET_FET
R5840
4.99K
1%
1/20W
MF
201
PP3V3_G3H_ENET_FET IS
AVAILABLE IN STANDBY
ENET_AUX_PWR
AUX_PWR
C5840
0.1UF
10%
25V
X6S-CERM
0201
PP1V5_LDO_ENET_EFUSE
EFUSE_VDDQ
ENET_JTAG_TCK
ENET_JTAG_TDI
ENET_JTAG_TDO
ENET_JTAG_TMS
ENET_JTAG_TRST_L
TCK
TDI
TDO
TMS
TRST*
PULL UPS
PP3V3_G3H_ENET_FET
R5889 4.99K 1% 1/16W MF-LF 402 ENET_CLKREQ_3V3_L
R5890 4.99K 1% 1/16W MF-LF 402 ENET_SMB_CLK
R5891 4.99K 1% 1/16W MF-LF 402 ENET_SMB_DAT
R5892 4.99K NOSTUFF 1% 1/16W MF-LF 402 ENET_SLAVE_SMB_CLK
R5893 4.99K NOSTUFF 1% 1/16W MF-LF 402 ENET_SLAVE_SMB_DAT
R5894 1K NOSTUFF 5% 1/16W MF-LF 402 ENET_JTAG_TMS
R5895 1K NOSTUFF 5% 1/16W MF-LF 402 ENET_JTAG_TDI
PP3V3_S5
R5886 4.99K NOSTUFF 1% 1/16W MF-LF 402 ENET_SYNC_1588
PULL UP / DOWNS
PP3V3_G3H_ENET_FET
R5899 4.99K NOSTUFF 1% 1/16W MF-LF 402 ENET_SMB_ALERT_L
R5898 4.99K NOSTUFF 1% 1/16W MF-LF 402
R5812 4.99K ENET_REFCLK:OSC 1% 1/16W MF-LF 402 ENET_XTAL_SELECT_L
R5810 0 ENET_REFCLK:CRYSTAL 5% 1/20W MF 201
R5814 4.99K NOSTUFF 1% 1/16W MF-LF 402 ENET_GPIO1_EFUSE_EN
R5813 10K 5% 1/16W MF-LF 402
PULL DOWNS
R5897 1K NOSTUFF 5% 1/16W MF-LF 402 ENET_JTAG_TCK
R5888 4.99K NOSTUFF 1% 1/16W MF-LF 402 ENET_JTAG_TRST_L
R5811 0 NOSTUFF 5% 1/20W MF 201 ENET_SYNC_1588
BOM_COST_GROUP=ETHERNET
SYNC_MASTER=BOYLE
SYNC_DATE=03/01/2017
PAGE TITLE
ETHERNET CONTROLLER 1
Apple Inc.
DRAWING NUMBER
051-01649
SIZE
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REVISION
6.21.0
BRANCH
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54 OF 171
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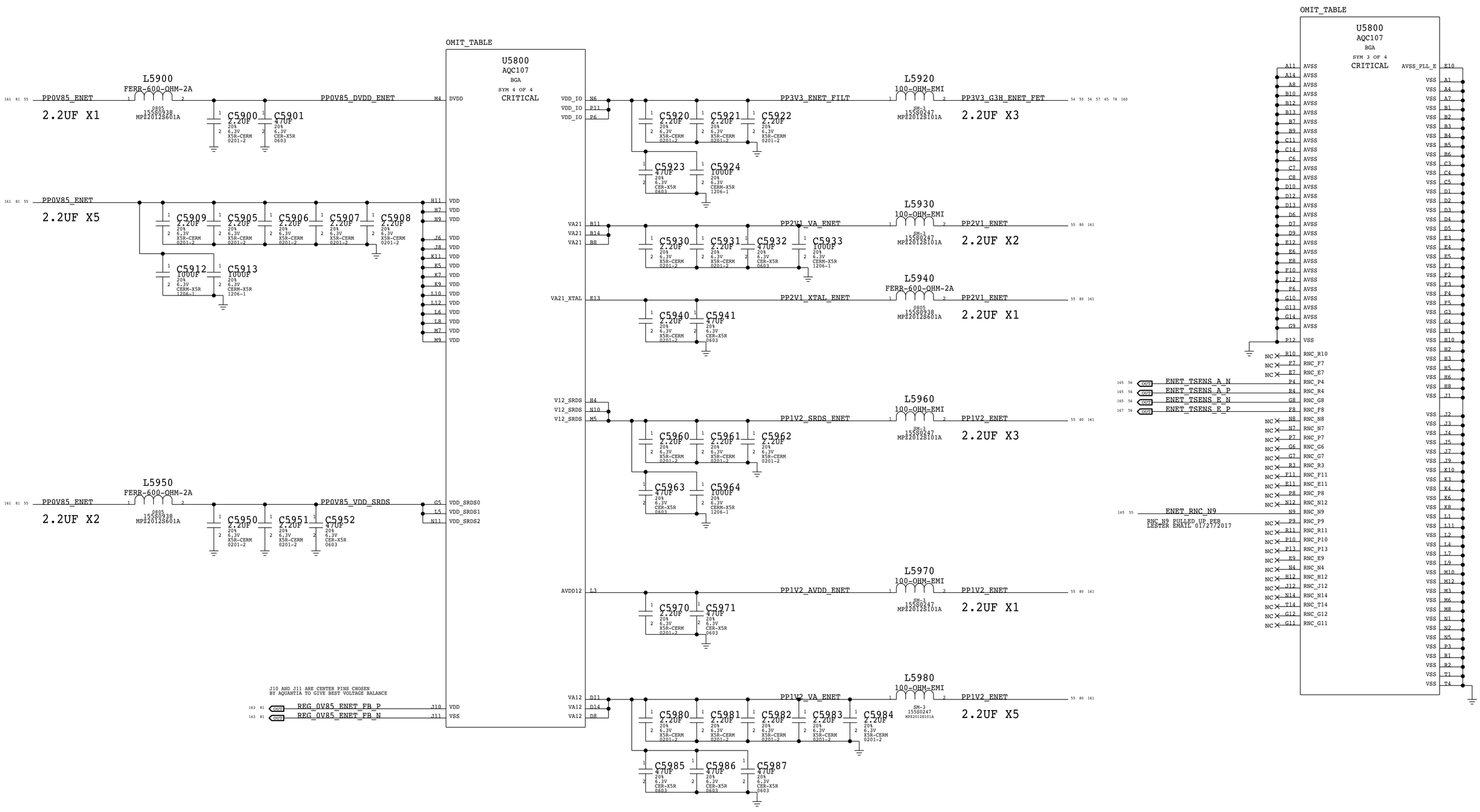

BOM_COST_GROUP=ETHERNET

SYNC_MASTER=BOYLE SYNC_DATE=03/01/2017

PAGE TITLE

ETHERNET CONTROLLER 2

Apple Inc.

DRAWING NUMBER 051-01649 SIZE D

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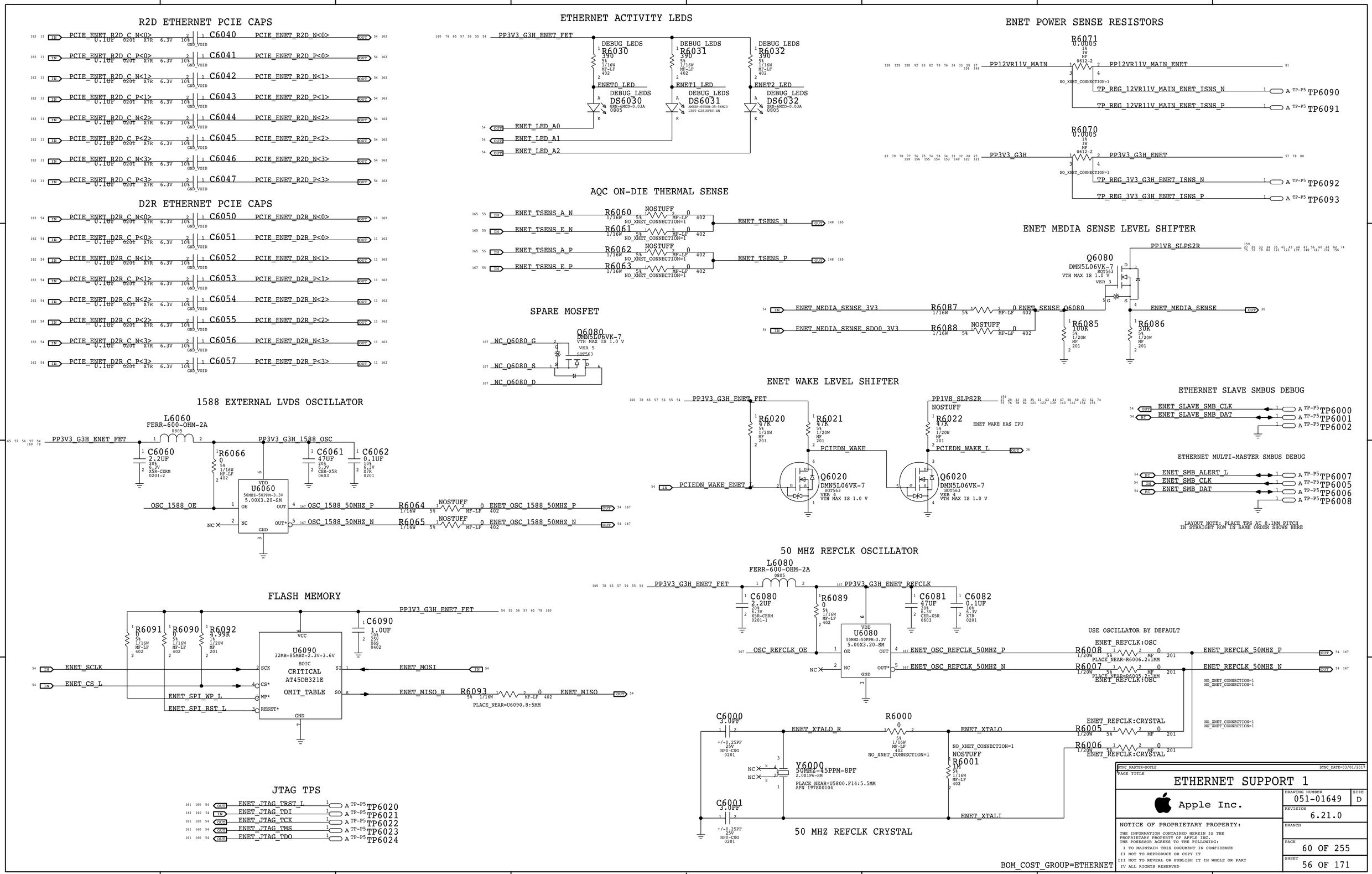
R2D ETHERNET PCIE CAPS
D2R ETHERNET PCIE CAPS
ETHERNET ACTIVITY LEDS
ENET POWER SENSE RESISTORS
AQC ON-DIE THERMAL SENSE
ENET MEDIA SENSE LEVEL SHIFTER
SPARE MOSFET
ENET WAKE LEVEL SHIFTER
ETHERNET SLAVE SMBUS DEBUG
ETHERNET MULTI-MASTER SMBUS DEBUG
1588 EXTERNAL LVDS OSCILLATOR
50 MHZ REFCLK OSCILLATOR
FLASH MEMORY
JTAG TPS
50 MHZ REFCLK CRYSTAL
USE OSCILLATOR BY DEFAULT
BOM_COST_GROUP=ETHERNET
ETHERNET SUPPORT 1
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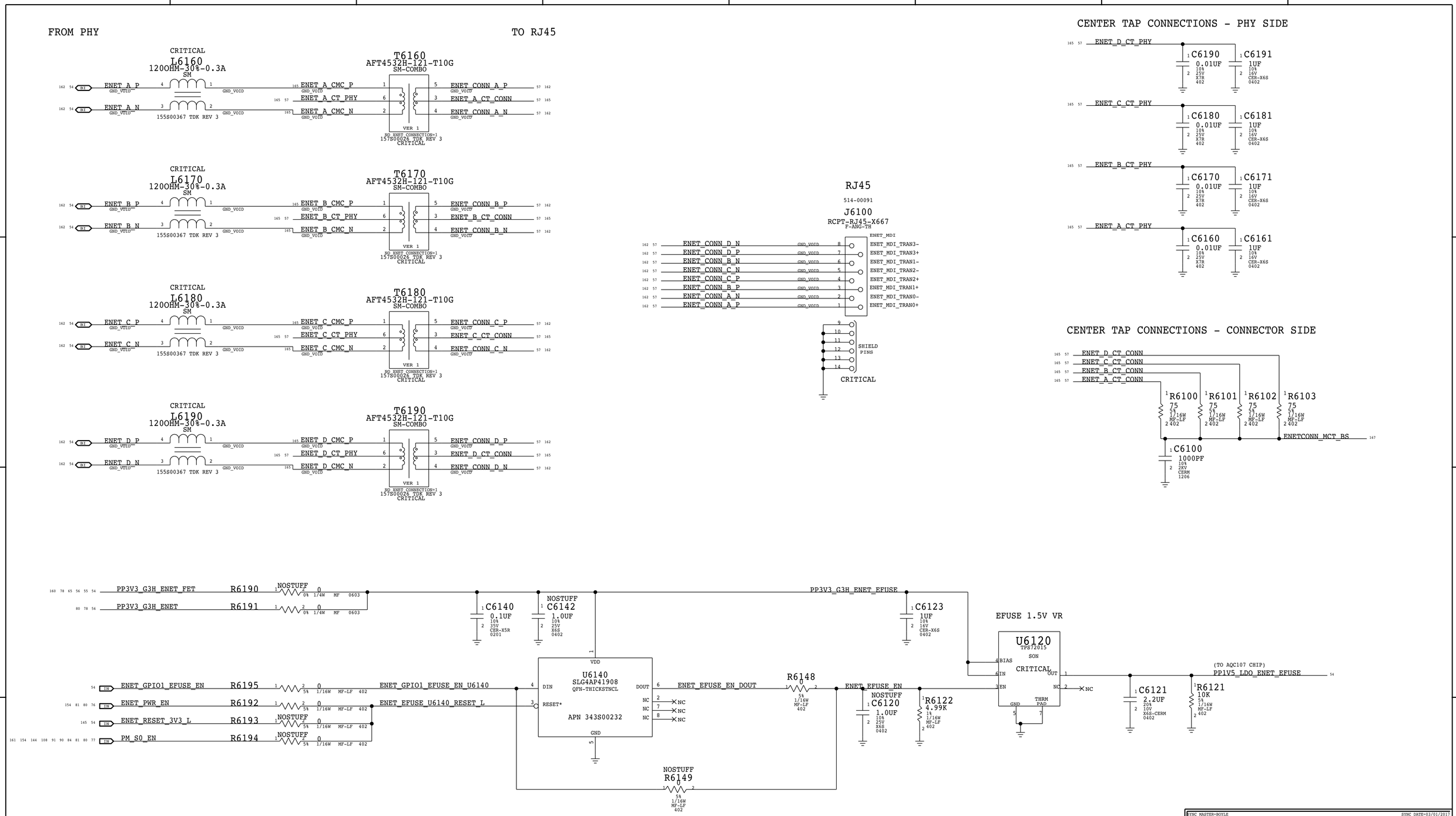

SYNC_MASTER=BOYLE SYNC_DATE=03/01/2017

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ETHERNET SUPPORT 2

Apple Inc.

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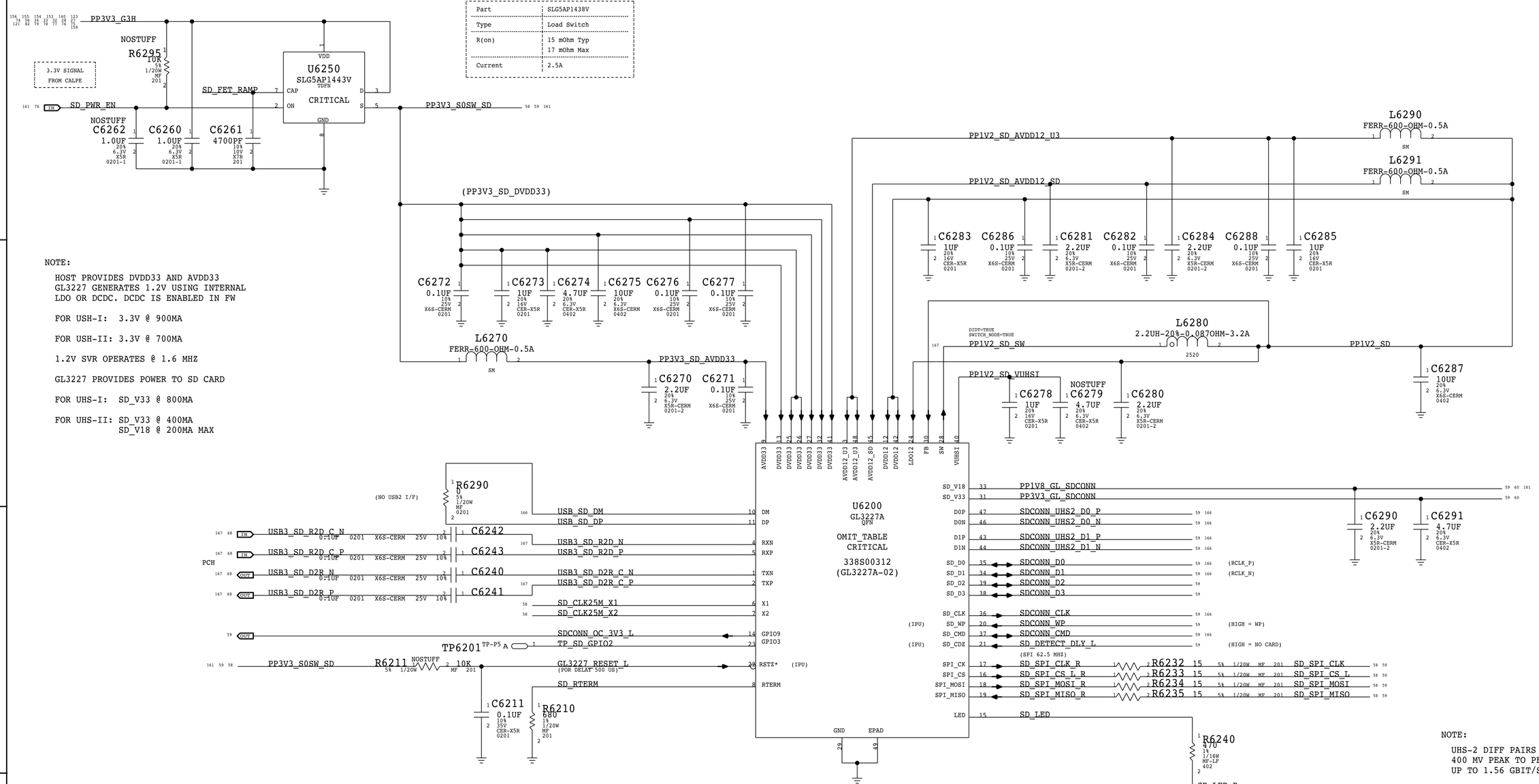
3.3V SD CARD LOAD SWITCH

U6250	EDP: 1.05A
Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A



NOTE:

HOST PROVIDES DVDD33 AND AVDD33
GL3227 GENERATES 1.2V USING INTERNAL
LDO OR DCDC. DCDC IS ENABLED IN FW

FOR USH-I: 3.3V @ 900MA

FOR USH-II: 3.3V @ 700MA

1.2V SVR OPERATES @ 1.6 MHZ

GL3227 PROVIDES POWER TO SD CARD

FOR UHS-I: SD_V33 @ 800MA

FOR UHS-II: SD_V33 @ 400MA
SD_V18 @ 200MA MAX

PIN 29 IS SVR GND
DO NOT CONNECT PIN 29 TO EPAD DIRECTLY
CONNECT PIN 29 TO PIN 27 CAP FIRST
THEN TO MAIN GND

NOTE:

UHS-2 DIFF PAIRS 100 OHM
400 MV PEAK TO PEAK
UP TO 1.56 GBIT/S

UHS-2 DIFF CLK UP TO 52 MHZ

USH-1 SE SIGNALS 50-OHM

SD_CLK MAX FREQ IS 208 MHZ
AT SDR104 MODE

LED IS ON WHEN POWER ON
BLINKING DURING R/W OPERATIONS

BOM_COST_GROUP=SD CARD

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

SD CONTROLLER UHS-II

Apple Inc.

DRAWING NUMBER	051-01649
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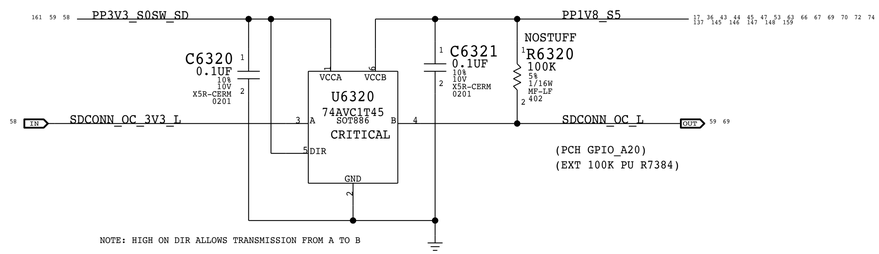
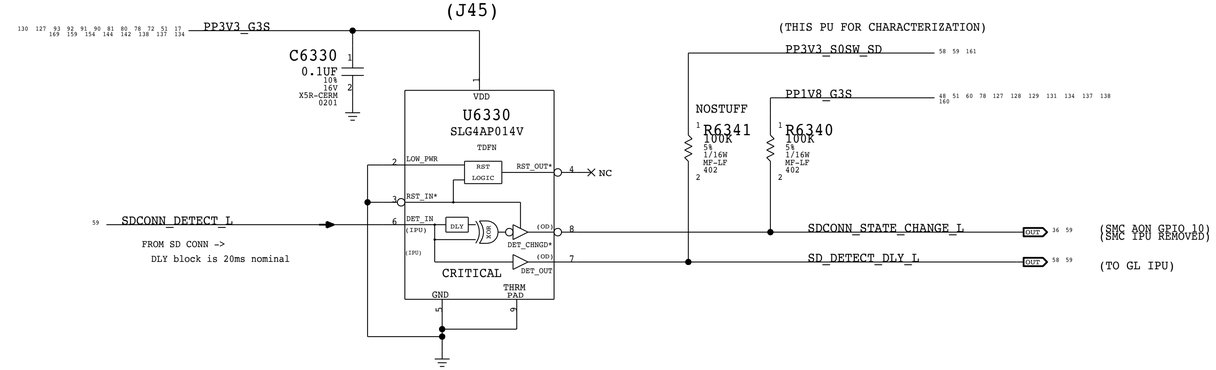
NOTE: CHANGE THIS POWER RAIL FOR P1 TO 1V8_S5

OC LEVEL SHIFTER

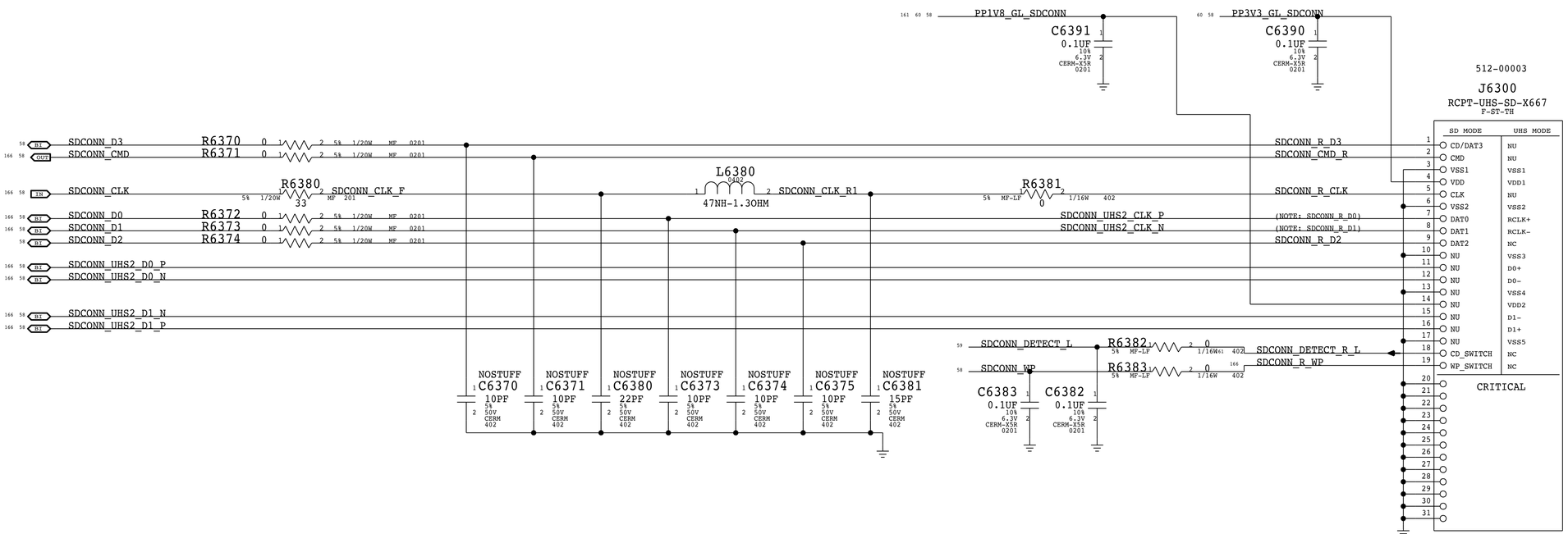


SDCONN STATE CHANGE AND DEBOUNCE

343S0527
(J45)



SD UHS-II CARD CONNECTOR



TP6330 SD_SPI_CLK
TP6331 SD_SPI_CS_L
TP6332 SD_SPI_MOSI
TP6333 SD_SPI_MISO
TP6340 SDCONN_OC_L
TP6341 SDCONN_DETECT_L
TP6342 SDCONN_STATE_CHANGE_L
TP6343 SD_DETECT_DLY_L

BOM_COST_GROUP=SD CARD

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE
SD CONNECTOR UHS-II

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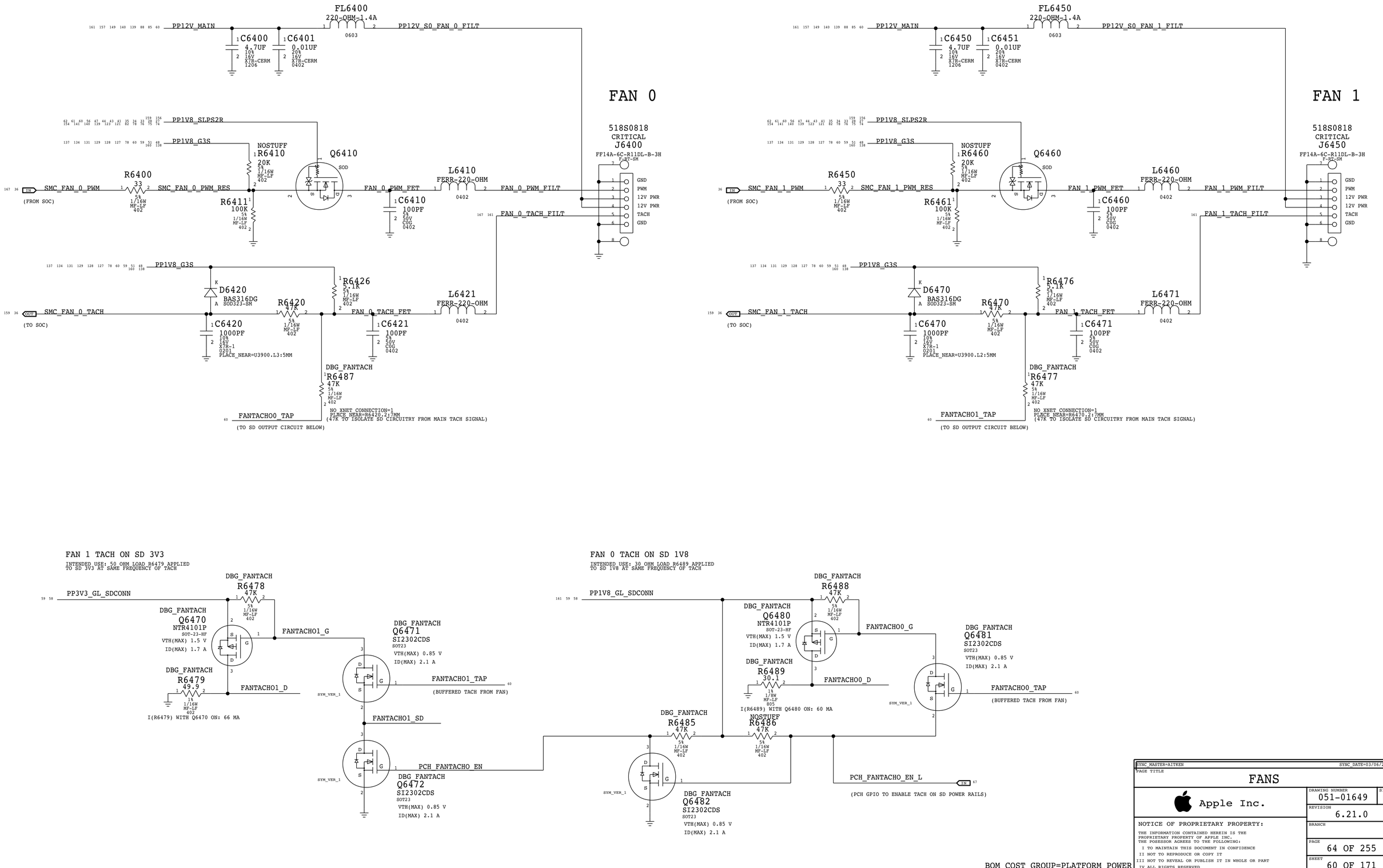
FAN 0
FL6400
220-OHM-1.4A
0603
PP12V_MAIN
PP12V_S0_FAN_0_FILT
C6400
4.7UF
10%
16V
X7R-CERM
1206
C6401
0.01UF
20%
16V
X7R-CERM
0402
PP1V8_SLPS2R
PP1V8_G3S
NOSTUFF
R6410
20K
5%
1/16W
MF-LF
402
Q6410
SOD
518S0818
CRITICAL
J6400
FF14A-6C-R11DL-B-3H
F-ST-SM
GND
PWM
12V PWR
12V PWR
TACH
GND
R6400
33
SMC_FAN_0_PWM
SMC_FAN_0_PWM_RES
(FROM SOC)
R6411
100K
FAN_0_PWM_FET
C6410
100PF
L6410
FERR-220-OHM
FAN_0_PWM_FILT
FAN_0_TACH_FILT
D6420
BAS316DG
SOD323-SM
R6426
5.1K
SMC_FAN_0_TACH
(TO SOC)
R6420
47K
FAN_0_TACH_FET
L6421
C6420
1000PF
10%
16V
X7R-1
0201
PLACE_NEAR=U3900.L3:5MM
C6421
100PF
DBG_FANTACH
R6487
47K
FANTACHO0_TAP
(TO SD OUTPUT CIRCUIT BELOW)
NO_XNET_CONNECTION=1
PLACE_NEAR=R6420.2:7MM
(47K TO ISOLATE SD CIRCUITRY FROM MAIN TACH SIGNAL)
FAN 1
FL6450
220-OHM-1.4A
PP12V_S0_FAN_1_FILT
C6450
C6451
PP1V8_SLPS2R
PP1V8_G3S
NOSTUFF
R6460
20K
Q6460
518S0818
CRITICAL
J6450
FF14A-6C-R11DL-B-3H
F-ST-SM
R6450
33
SMC_FAN_1_PWM
SMC_FAN_1_PWM_RES
(FROM SOC)
R6461
100K
FAN_1_PWM_FET
C6460
100PF
L6460
FERR-220-OHM
FAN_1_PWM_FILT
FAN_1_TACH_FILT
D6470
BAS316DG
SOD323-SM
R6476
5.1K
SMC_FAN_1_TACH
(TO SOC)
R6470
47K
FAN_1_TACH_FET
L6471
C6470
1000PF
PLACE_NEAR=U3900.L2:5MM
C6471
100PF
DBG_FANTACH
R6477
47K
FANTACHO1_TAP
(TO SD OUTPUT CIRCUIT BELOW)
NO_XNET_CONNECTION=1
PLACE_NEAR=R6470.2:7MM
(47K TO ISOLATE SD CIRCUITRY FROM MAIN TACH SIGNAL)
FAN 1 TACH ON SD 3V3
INTENDED USE: 50 OHM LOAD R6479 APPLIED
TO SD 3V3 AT SAME FREQUENCY OF TACH
PP3V3_GL_SDCONN
DBG_FANTACH
R6478
47K
Q6470
NTR4101P
SOT-23-HF
VTH(MAX) 1.5 V
ID(MAX) 1.7 A
FANTACHO1_G
R6479
49.9
1%
1/16W
MF-LF
402
FANTACHO1_D
I(R6479) WITH Q6470 ON: 66 MA
Q6471
SI2302CDS
SOT23
VTH(MAX) 0.85 V
ID(MAX) 2.1 A
FANTACHO1_TAP
(BUFFERED TACH FROM FAN)
FANTACHO1_SD
PCH_FANTACHO_EN
Q6472
SI2302CDS
FAN 0 TACH ON SD 1V8
INTENDED USE: 30 OHM LOAD R6489 APPLIED
TO SD 1V8 AT SAME FREQUENCY OF TACH
PP1V8_GL_SDCONN
R6488
47K
Q6480
NTR4101P
SOT-23-HF
VTH(MAX) 1.5 V
ID(MAX) 1.7 A
FANTACHO0_G
R6489
30.1
1%
1/8W
MF-LF
805
I(R6489) WITH Q6480 ON: 60 MA
FANTACHO0_D
Q6481
SI2302CDS
SOT23
VTH(MAX) 0.85 V
ID(MAX) 2.1 A
FANTACHO0_TAP
(BUFFERED TACH FROM FAN)
R6485
47K
NOSTUFF
R6486
47K
PCH_FANTACHO_EN_L
(PCH GPIO TO ENABLE TACH ON SD POWER RAILS)
Q6482
SI2302CDS
SOT23
VTH(MAX) 0.85 V
ID(MAX) 2.1 A
BOM_COST_GROUP=PLATFORM POWER
SYNC_MASTER=AITKEN
SYNC_DATE=03/06/2017
PAGE TITLE
FANS
Apple Inc.
DRAWING NUMBER
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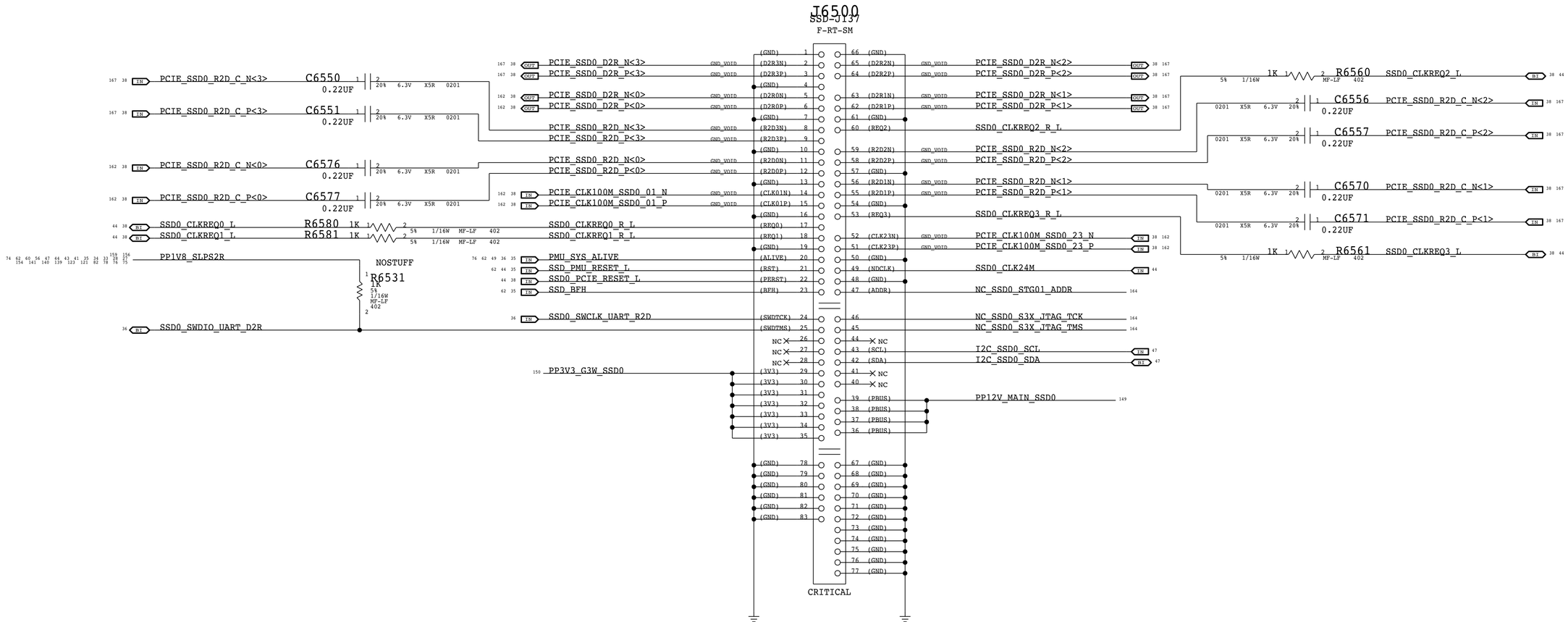
SSD GS5 CONNECTOR A

APN:514S00120



BOM_COST_GROUP=SSD

PAGE TITLE
SSD CONN A

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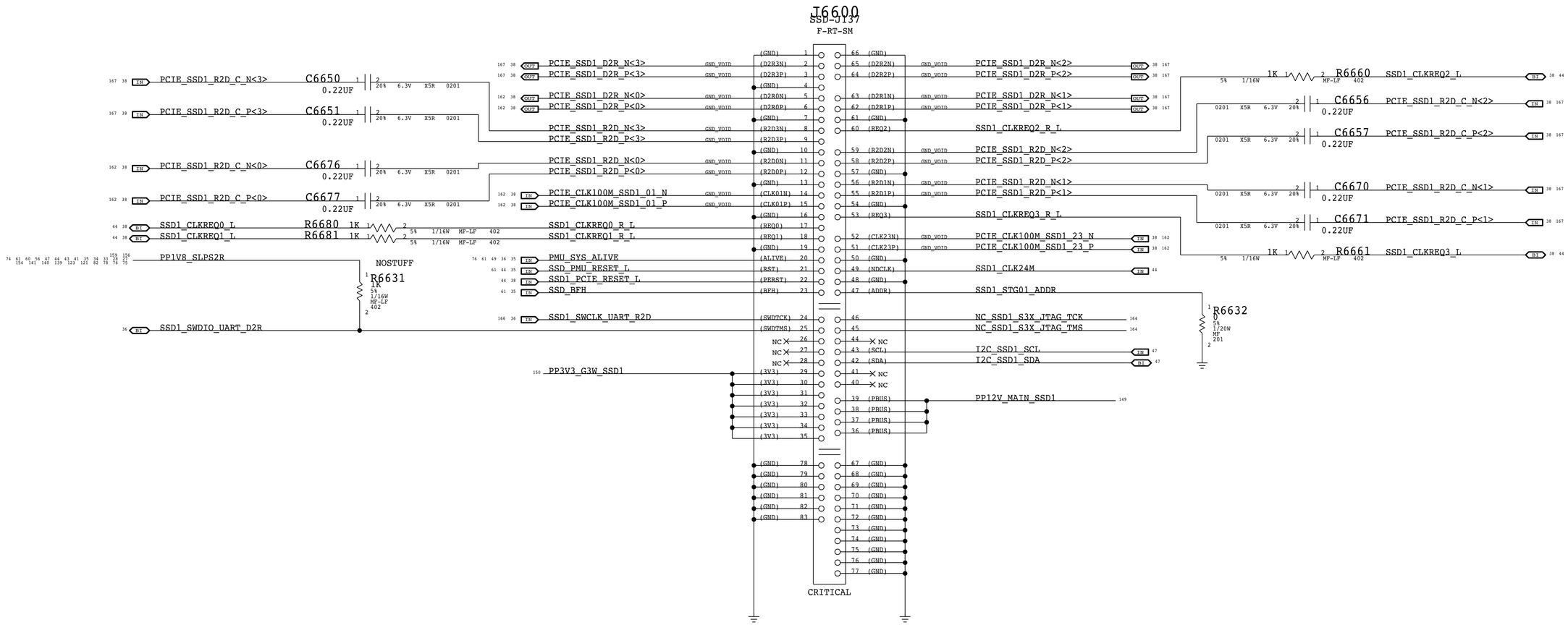
SSD GS5 CONNECTOR B

APN:514S00120



BOM_COST_GROUP=SSD

PAGE TITLE
SSD CONN B

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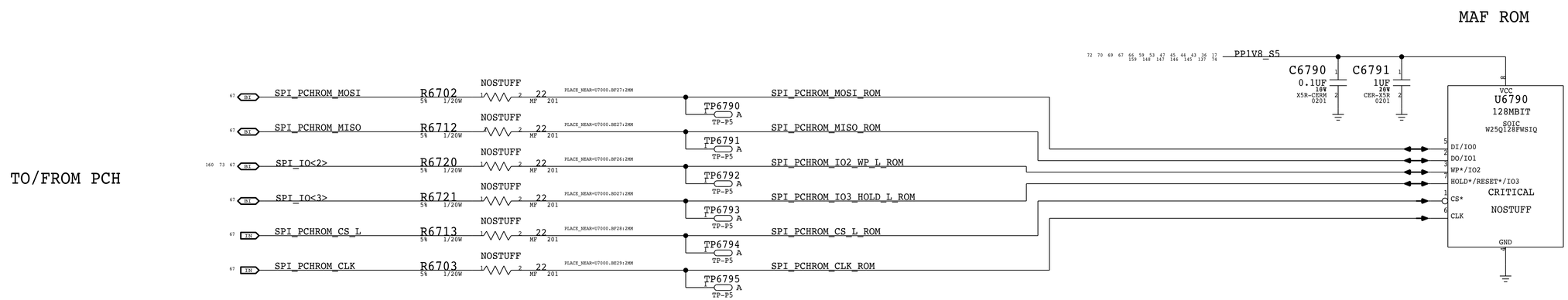

SPI ROM

Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 40MHz for SMC.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and Dual-IO modes.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE: SPI ROM

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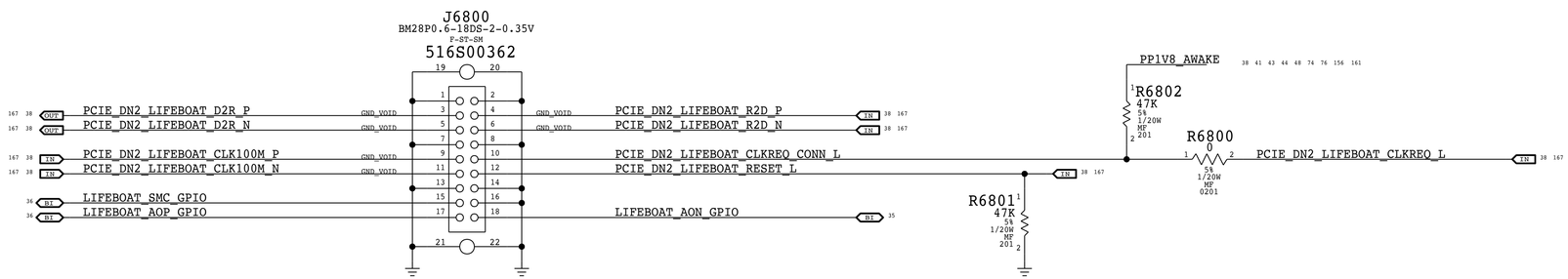

LIFEBOAT GPIOS ASSIGNED PER <RDAR://33517854>

BOM_COST_GROUP=SSD

SYNC_MASTER=AMAN SYNC_DATE=07/25/2017

PAGE TITLE

LIFEBOAT

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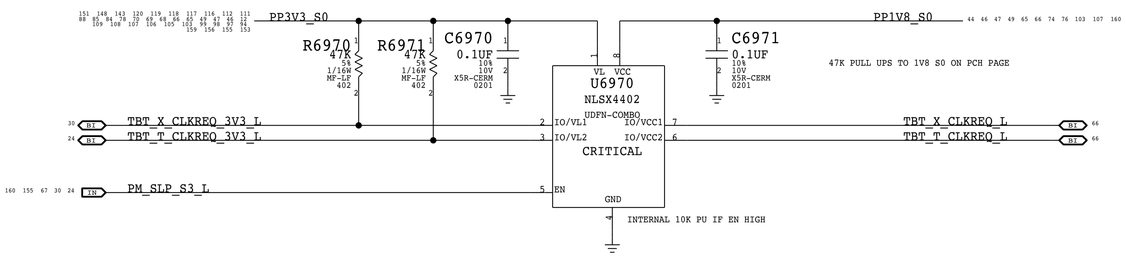
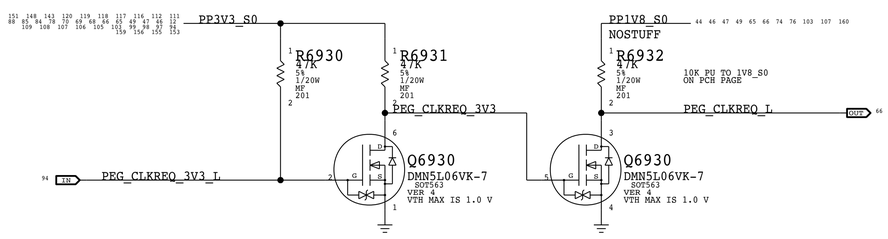
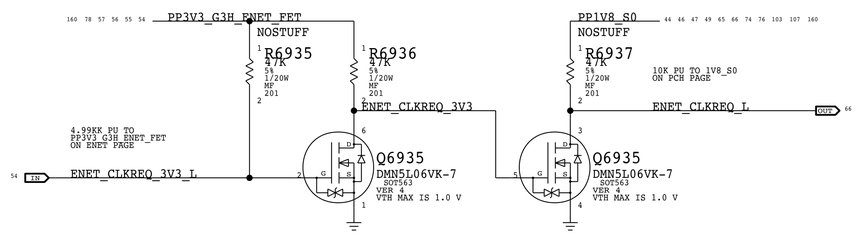
CLKREQ LEVEL SHIFTERS







BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

PCH LEVEL SHIFTERS

Apple Inc.

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NOTE: 1V8 BANKS ARE A,B,C,H

OMIT_TABLE

U7000
KBL-PCH-H
951678
FCBGA
SYM 2 OF 12
CRITICAL

PCIE REF CLKS

PCIE_CLK100M_WLAN_N	P5	CLKOUT_PCIE_N0
PCIE_CLK100M_WLAN_P	P7	CLKOUT_PCIE_P0
PCIE_CLK100M_ENET_N	M7	CLKOUT_PCIE_N1
PCIE_CLK100M_ENET_P	M5	CLKOUT_PCIE_P1
PCIE_CLK100M_SOC_N	H7	CLKOUT_PCIE_N2
PCIE_CLK100M_SOC_P	G7	CLKOUT_PCIE_P2
PCIE_CLK100M_TBT_X_N	K7	CLKOUT_PCIE_N3
PCIE_CLK100M_TBT_X_P	K5	CLKOUT_PCIE_P3
PCIE_CLK100M_TBT_T_N	E3	CLKOUT_PCIE_N4
PCIE_CLK100M_TBT_T_P	E4	CLKOUT_PCIE_P4
PEG_CLK100M_N	C5	CLKOUT_PCIE_N5
PEG_CLK100M_P	C6	CLKOUT_PCIE_P5
NC	T8	CLKOUT_PCIE_N6
NC	T7	CLKOUT_PCIE_P6
PCIE_CLK100M_ANALYZER_N	V5	CLKOUT_PCIE_N7
PCIE_CLK100M_ANALYZER_P	V7	CLKOUT_PCIE_P7
NC	Y10	CLKOUT_PCIE_N8
NC	Y11	CLKOUT_PCIE_P8
NC	M2	CLKOUT_PCIE_N9
NC	M1	CLKOUT_PCIE_P9
NC	P3	CLKOUT_PCIE_N10
NC	P2	CLKOUT_PCIE_P10
NC	T2	CLKOUT_PCIE_N11
NC	T3	CLKOUT_PCIE_P11
NC	U1	CLKOUT_PCIE_N12
NC	U2	CLKOUT_PCIE_P12
NC	Y7	CLKOUT_PCIE_N13
NC	AA5	CLKOUT_PCIE_P13
NC	R3	CLKOUT_PCIE_N14
NC	R2	CLKOUT_PCIE_P14
NC	T13	CLKOUT_PCIE_N15
NC	T11	CLKOUT_PCIE_P15

CLOCK SIGNALS

PCI EXPRESS
CLOCKS & CONTROL

XTAL24_IN	E1	PCH_XTAL24_IN
XTAL24_OUT	A5	PCH_XTAL24_OUT
XCLK_BIASREF	F1	PCH_DIFFCLK_BIASREF
GPP_A9/CLKOUT_LPC0 /ESPI_CLK	BE15	ESPI_CLK60M_R
GPP_A10/CLKOUT_LPC1	AY17	TP_GPP_A10
GPP_A16/CLKOUT_48	BC17	SOC_SWD_CLK
CLKOUT_ITPXDP_N	L2	CLK100M_CPU_BCLK_2_N
CLKOUT_ITPXDP_P	L3	CLK100M_CPU_BCLK_2_P
CLKOUT_CPUBCLK_N	H2	CLK100M_CPU_BCLK_0_N
CLKOUT_CPUBCLK_P	H1	CLK100M_CPU_BCLK_0_P
CLKOUT_CPUNSSC_N	G1	TP_KBLX_CLK24M
CLKOUT_CPUNSSC_P	G2	PM_SYNC_CLK
CLKOUT_CPUPCIBCLK_N	J3	CLK100M_CPU_BCLK_1_N
CLKOUT_CPUPCIBCLK_P	J2	CLK100M_CPU_BCLK_1_P

R7018 0 5% 1/20W MF 0201 — PCH_XTAL24_IN_R
R7002 1M 5% 1/20W MF 201
R7019 0 5% 1/20W MF 0201 — PCH_XTAL24_OUT_R
CRITICAL Y7001 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM
C7001 10PF 5% 50V COG 0201
C7002 10PF 5% 50V COG 0201

R7015 2.7K 0.1% 1/16W MF 0402 — PP1V0_PCH_CORE_S5

R7020 33 5% 1/16W MF-LF 402 — ESPI_CLK

DIRECT 100MHZ CLOCK DIF CORE REF CLOCK FROM PCH TO PROCESSOR

DIRECT 24MHZ DIFF CRYSTAL REF CLOCK FROM PCH TO PROCESSOR
SPLIT INTO TWO SINGLE ENDED CLOCKS PER CRB REF SCHEMATIC

CLKREQS

GPP_B5/SRCCLKREQ0*	BE22	WLAN_CLKREQ_PCH_L	R7016 0	WLAN_CLKREQ_L
GPP_B6/SRCCLKREQ1*	BA24	ENET_CLKREQ_PCH_L	R7094 0	ENET_CLKREQ_L
GPP_B7/SRCCLKREQ2*	BA19	SOC_CLKREQ_PCH_L	R7058 0	SOC_CLKREQ_L
GPP_B8/SRCCLKREQ3*	BE23	TBT_X_CLKREQ_PCH_L	R7055 0	TBT_X_CLKREQ_L
GPP_B9/SRCCLKREQ4*	BD22	TBT_T_CLKREQ_PCH_L	R7056 0	TBT_T_CLKREQ_L
GPP_B10/SRCCLKREQ5*	BF23	PEG_CLKREQ_PCH_L	R7057 0	PEG_CLKREQ_L
GPP_H0/SRCCLKREQ6*	AR29	NC		
GPP_H1/SRCCLKREQ7*	AU27	PU_CLKREQ_ANA_PCH_L	R7059 0	PU_CLKREQ_ANALYZER_L
GPP_H2/SRCCLKREQ8*	BG30	NC		
GPP_H3/SRCCLKREQ9*	BF30	NC		
GPP_H4/SRCCLKREQ10*	BD29	TP_PCH_GPP_H4		
GPP_H5/SRCCLKREQ11*	BE31	TP_PCH_GPP_H5		
GPP_H6/SRCCLKREQ12*	AY29	NC		
GPP_H7/SRCCLKREQ13*	AV29	TP_PCH_GPP_H7		
GPP_H8/SRCCLKREQ14*	BD31	TP_PCH_GPP_H8		
GPP_H9/SRCCLKREQ15*	BF31	NC		

PP1V8_S5 — R7088 100K 5% 1/16W MF-LF 402 — SOC_SWD_CLK

PP1V8_S0 — R7004 47K 5% 1/20W MF 201 — TBT_X_CLKREQ_L
R7034 47K 5% 1/20W MF 201 — TBT_T_CLKREQ_L
R7001 47K 5% 1/20W MF 201 — ENET_CLKREQ_L
R7013 47K 5% 1/20W MF 201 — WLAN_CLKREQ_L

PP3V3_S0 — R7084 100K 5% 1/16W MF-LF 402 — TBT_X_CIO_PLUG_EVENT_L
R7085 100K 5% 1/16W MF-LF 402 — TBT_T_CIO_PLUG_EVENT_L

PP1V8_S0
R7091 10K 1/16W 5% MF-LF 402 — PU_CLKREQ_ANALYZER_L
R7090 10K 1/16W 5% MF-LF 402 NOSTUFF
R7093 10K 1/16W 5% MF-LF 402 — PEG_CLKREQ_L
R7092 10K 1/16W 5% MF-LF 402 NOSTUFF

R7074 1.1K 5% 1/16W MF-LF 402 NOSTUFF — TP_GPP_A10
R7070 100K 5% 1/16W MF-LF 402 — BT_I2S_CLK_R_3V3
R7071 100K 5% 1/16W MF-LF 402 — BT_I2S_D2R_R_3V3
R7072 100K 5% 1/16W MF-LF 402 — BT_I2S_R2D_R_3V3
R7073 100K 5% 1/16W MF-LF 402 — BT_I2S_WC_R_3V3
R7006 1K 5% 1/20W MF 201 — PCH_JTAGX
PLACE_NEAR=U7000.AP3:8MM

OMIT_TABLE

U7000
KBL-PCH-H
951678
FCBGA
SYM 1 OF 12
CRITICAL

AUDIO TEAM REQUESTS TPS ON ALL HDA SIGNALS

NC	AC13	RSVD
NC	AF17	RSVD
NC	AG17	RSVD
NC	AH14	RSVD
NC	AH16	RSVD
NC	AP29	RSVD
NC	AU22	RSVD
NC	BF1	RSVD
NC	BG2	RSVD
NC	H33	RSVD
NC	N29	RSVD
NC	N33	RSVD
NC	P24	RSVD
NC	P27	RSVD
NC	P29	RSVD
NC	T24	RSVD
NC	T27	RSVD
NC	T33	RSVD
NC	T35	RSVD
NC	V11	RSVD
NC	V13	RSVD
TP_FPF_MON	AP17	TP1
TP_FPF_VREF	AU19	TP2
PCH_ITP_PMODE	AR2	ITP_PMODE
XDP_PCH_TCK	AN1	JTAG_TCK
XDP_PCH_TDI	AP2	JTAG_TDI
XDP_PCH_TDO	AN3	JTAG_TDO
XDP_PCH_TMS	AP4	JTAG_TMS
PCH_JTAGX	AP3	JTAGX

RSVD & TP PINS

HDA_BCLK	BB3	TP_HDA_BCLK
HDA_SYNC	BG6	TP_HDA_SYNC
HDA_SDIO	BA2	TP_HDA_SDIO
HDA_SDI1	BB1	TP_HDA_SDI1
HDA_SDO	BC3	HDA_SDOUT
HDA_RST*	BC1	TP_HDA_RST_L
DISPA_BCLK	AM2	NC
DISPA_SDI	AN2	NC
DISPA_SDO	AM3	NC
GPP_D5/I2S0_SFRM	AP36	BT_I2S_WC_R_3V3
GPP_D6/I2S0_TXD	AU43	BT_I2S_R2D_R_3V3
GPP_D7/I2S0_RXD	AV44	BT_I2S_D2R_R_3V3
GPP_D8/I2S0_SCLK	AU42	BT_I2S_CLK_R_3V3
GPP_D17/DMIC_CLK1	AP42	TBT_X_CIO_PLUG_EVENT_L
GPP_D18/DMIC_DATA1	AN43	TBT_T_CIO_PLUG_EVENT_L
GPP_D19/DMIC_CLK0	AP38	NC
GPP_D20/DMIC_DATA0	AM43	NC

AUDIO

JTAG

SPI_DESCRIPTOR_OVERRIDE — R7060 330 5% 1/20W MF 201 — HDA_SDOUT
330 OHM USED HERE TO MATCH J135
14K-26K IPD
330 BRINGS MIN VH TO 1.76V
PORTABLES HAVE HIGHER IPD AND USE 1K

Q7060
DFN1006H4-3
DMP31D0UFB4
PP1V8_S5

PCH USES HDA_SDO AS A POWER-UP STRAP. IF LOW, ME FUNCTIONS NORMALLY.
IF HIGH, ME IS DISABLED. THIS ALLOWS FOR FULL RE-FLASHING OF SPI ROM.
SMC CONTROLS STRAP ENABLE TO ALLOW IN-FIELD CONTROL OF STRAP SETTING.

SPI_DESCRIPTOR_OVERRIDE_L

TP_FPF_MON
TP_FPF_VREF
PCH_ITP_PMODE
XDP_PCH_TCK
XDP_PCH_TDI
XDP_PCH_TDO
XDP_PCH_TMS
XDP_CPU_TCK — R7017 0 5% 1/20W MF 0201 — PCH_JTAGX
PLACE_NEAR=U7000.AP3:10MM

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=AITKEN SYNC_DATE=03/06/2017

PAGE TITLE
PCH CLOCKS, JTAG

Apple Inc.

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REVISION 6.21.0
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NOTE: 1V8 BANKS ARE A,B,C,H

NOTE: PER EDS #564464, RSMRST, PCH_PWROK, INTRUDER, DSW PWROK, SRTCRST ARE INPUTS IN RTC WELL WITH VIH MIN 0.65 * VRTC AND VIL MAX 0.30 * VRTC

NOTE: RTCRST HAS A DIFFERENT VIH/VIL VIH MIN IS 0.75 * VRTC VIL MAX IS 0.40 * VRTC

OMIT_TABLE

U7000 KBL-PCH-H 951678 FCBGA SYM 4 OF 12 SYSTEM POWER MANAGEMENT CRITICAL

PCH_SUSACK_L	BD17	GPP_A15/SUS_ACK*	
PM_SYSRST_L	AV3	SYS_RESET*	
PM_PCH_SYS_PWROK	AW3	SYS_PWROK	
PM_PCH_PWROK	BE4	PCH PWROK (VCCRTC)	
PLT_RESET_L	BD24	GPP_B13/PLTRST*	
PM_RSMRST_PCH_L	BG5	RSMRST*	
PCH_SUSWARN_L	BF17	GPP_A13/SUSWARN* /SUSPWRDNACK	
PM_PWRBTN_L	BC5	GPD3/PWRBTN*	
SPIROM_USE_MLB	BD13	GPD1/ACPRESENT	
PCH_GPD_0	BF11	GPD0/BATLOW*	
PCH_PM_SLP_S0_L	BB24	GPP_B12/SLP_S0*	
TP_PCH_GPD9	BA9	GPD9/SLP_WLAN*	
NC	BF15	GPP_A11/PME*	
NC	BD15	GPP_A12/BMBUSY*/ISH_GP6 /SX_EXIT_HOLDOFF*	
DRAM_RESET*	BD10		PCH_MEM_RESET_L
DSW PWROK (VCCRTC)	BD4		PM_RSMRST_PCH_L
WAKE*	BF9		PCIE_WAKE_L
GPP_A8/CLKRUN*	BA15	NC	
GPP_A14/SUS_STAT*/ESPI_RESET*	BF16		ESPI_RESET_L
GPD8/SUSCLK	AV13		TP_PCH_GPD8
GPD10/SLP_S5*	BB7		PM_SLP_S5_L
GPD5/SLP_S4*	BF13		PM_SLP_S4_L
GPD4/SLP_S3*	BA11		PM_SLP_S3_L
GPD6/SLP_A*	BE13		TP_PM_SLP_A_L
SLP_SUS*	BF10		PM_SLP_SUS_L
SLP_LAN*	AV11		TP_PCH_SLP_LAN_L
GPD2/LAN_WAKE*	BE10		TP_PCH_LAN_WAKE_L
GPD11/LANPHYPC	BC11		TP_PCH_GPD11
GPP_B2/VRALERT*	BG21		TP_PCH_GPP_B2
PCH_CLK32K_RTCX1_R	BF7	RTCX1	
PCH_CLK32K_RTCX2_R	BG7	RTCX2	
PCH_INTRUDER_L	BF9	INTRUDER* (VCCRTC)	
PCH_SRTCRST_L	BF8	SRTCRST* (VCCRTC)	
RTC_RESET_L	BE8	RTCRST* (VCCRTC)	
GPP_A0/RCIN*/ESPI_ALERT1*	AU15		PU_PCH_GPP_A0
GPP_A1/LAD0/ESPI_IO0	AR15		ESPI_IO<0>
GPP_A2/LAD1/ESPI_IO1	AY15		ESPI_IO<1>
GPP_A3/LAD2/ESPI_IO2	AV17		ESPI_IO<2>
GPP_A4/LAD3/ESPI_IO3	BE14		ESPI_IO<3>
GPP_A5/LFRAME*/ESPI_CS0*	BE14		ESPI_CS_L
GPP_A6/SERIRQ/ESPI_CS1*	BC13		TP_PCH_GPP_A6
GPP_A7/PIRQA*/ESPI_ALERT0*	AY13		PU_PCH_GPP_A7
GPD7/RSVD	BG11		TP_PCH_GPD7

RTC ESPI/LPC

NOSTUFF R7186 0 5% 1/20W MF 0201

NOTE: NOSTUFF ACCORDING TO WILL EFI HANDLES THIS

R7171 0 5% 1/20W MF 0201

R7163 1K 5% 1/16W MF-LF 402

PPVDDQ23_S3

TP_PCH_MEM_RESET_L

NOSTUFF C7161 0.1UF 10% 16V X7R-CERM 0402

PPVRTC_G3H

R7102 20K 5% 1/20W MF 201

R7101 20K 5% 1/20W MF 201

R7100 1M 5% 1/20W MF 201

C7101 1UF 10% 10V X5R 402-1

C7100 1UF 10% 10V X5R 402-1

R7103 0 5% 402 1/16W MF-LF

R7104 0 5% 402 1/16W MF-LF

LEGACY RTC RESET

R7105 0 NOSTUFF 5% 402 1/16W MF-LF

R7106 0 NOSTUFF 5% 402 1/16W MF-LF

RTC RESET FROM CALPE

OMIT_TABLE

U7000 KBL-PCH-H 951678 FCBGA SYM 5 OF 12 CRITICAL

DMI_SB_TO_CPU_N<0>	D27	DMI_TXN0	
DMI_SB_TO_CPU_P<0>	C27	DMI_TXP0	
DMI_SB_TO_CPU_N<1>	B27	DMI_TXN1	
DMI_SB_TO_CPU_P<1>	A28	DMI_TXP1	
DMI_SB_TO_CPU_N<2>	B28	DMI_TXN2	
DMI_SB_TO_CPU_P<2>	C28	DMI_TXP2	
DMI_SB_TO_CPU_N<3>	C29	DMI_TXN3	
DMI_SB_TO_CPU_P<3>	B29	DMI_TXP3	
DMI_CPU_TO_SB_N<0>	L27	DMI_RXN0	
DMI_CPU_TO_SB_P<0>	N27	DMI_RXP0	
DMI_CPU_TO_SB_N<1>	E24	DMI_RXN1	
DMI_CPU_TO_SB_P<1>	G24	DMI_RXP1	
DMI_CPU_TO_SB_N<2>	G27	DMI_RXN2	
DMI_CPU_TO_SB_P<2>	E26	DMI_RXP2	
DMI_CPU_TO_SB_N<3>	L29	DMI_RXN3	
DMI_CPU_TO_SB_P<3>	K29	DMI_RXP3	
PROCPWRGD	AL2		PCH_PROCPWRGD
THRMTRIP*	AH4		PM_THRMTRIP_L
PECI	AK4		PCH_PECI
GPP_B3/CPU_GP2	BF21		WLAN_PERST_L
GPP_B4/CPU_GP3	BF22		WLAN_DEV_WAKE
GPP_E3/CPU_GP0	AP41		XDP_OBSDATA_A_2
GPP_E7/CPU_GP1	AK43		XDP_OBSDATA_B_2
GPP_B23/SML1ALERT*/PCHHOT*	BA22		TP_PCH_GPP_B23
CPU_TRST*	AV2		XDP_PCH_TRST_L
PLTRST_PROC*	AK3		CPU_RESET_L
PRDY*	AR1		XDP_PCH_PRDY_L
PREQ*	AU3		XDP_PCH_PREQ_L
PCH_TRIGIN	AJ2		TP_CPU_2_PCH_TRIGGER
PCH_TRIGOUT	AL1		TP_PCH_2_CPU_TRIGGER
PM_DOWN	AH2		PCH_PM_DOWN
PM_SYNC	AH3		PM_PCH_SYNC

DMI CPU/MISC

R7187 33 1% 1/20W MF 201 PLACE_NEAR=U7000.AL2:10MM — CPU_PWRGD

INTERNAL PULL ON HARPOON

KBLX SIGNAL ON CPU

KBLX SIGNAL ON CPU

R7129 33 1% 1/20W MF 201 PLACE_NEAR=U7000.AH3:5MM — PM_CPU_SYNC

PP1V8_S5

R7138	100K	PU_PCH_GPP_A7	
R7139	100K	PU_PCH_GPP_A0	
R7183	1K	PCH_STRP_NOREBOOT	
R7160	47K	ENET_RESET_L	
R7161	47K	TBT_T_PCI_RESET_PCH_L	
R7162	47K	TBT_X_PCI_RESET_PCH_L	
R7169	1K	SPI_PCHROM_CS_L	
R7184	10K	NOSTUFF PCH_STRP_BOOT_LPC	
R7185	1K	NOSTUFF TP_PCH_GPP_B23	
R7189	10K	PCH_FANTACHO_EN_L	

PP3V3_S5

R7110	1K	PCIE_WAKE_L	
R7159	100K	TP_PCH_LAN_WAKE_L	
R7157	100K	SPIROM_USE_MLB	
R7158	1K	PCH_GPD_0	
R7148	100K	NOSTUFF PLT_RESET_L	
R7144	100K	WLAN_DEV_WAKE	
R7116	100K	PCH_PM_SLP_S0_L	
R7188	1K	NOSTUFF PCH_PECI	
R7112	100K	PM_SLP_S3_L	
R7113	100K	PM_SLP_S4_L	
R7114	100K	PM_SLP_S5_L	
R7115	100K	NOSTUFF PM_SLP_SUS_L	

OMIT_TABLE

U7000 KBL-PCH-H 951678 FCBGA SYM 3 OF 12 CRITICAL

SPI_PCHROM_CLK	BE29	SPI0_CLK	
SPI_PCHROM_CS_L	BE28	SPI0_CS0*	
NC	BA27	SPI0_CS1*	
NC	AY27	SPI0_CS2*	
SPI_PCHROM_MOSI	BE27	SPI0_MOSI	
SPI_PCHROM_MISO	BE27	SPI0_MISO	
SPI_IO<2>	BE26	SPI0_IO2	
SPI_IO<3>	BD27	SPI0_IO3	
GPP_B15/GSPI0_CS*	AV22		ENET_RESET_L
GPP_B16/GSPI0_CLK	AY24		TBT_X_PCI_RESET_PCH_L
GPP_B17/GSPI0_MISO	BG25		TBT_T_PCI_RESET_PCH_L
GPP_B18/GSPI0_MOSI	BE26		PCH_STRP_NOREBOOT
GPP_B19/GSPI1_CS*	BF25		TP_PCH_GPP_B19
GPP_B20/GSPI1_CLK	BF24		PCH_FANTACHO_EN_L
GPP_B21/GSPI1_MISO	AP24		SOC_PERST_L
GPP_B22/GSPI1_MOSI	AR24		PCH_STRP_BOOT_LPC
CL_CLK	AU2		TP_CLINK_CLK
CL_DATA	AU4		TP_CLINK_DATA
CL_RST*	AW2		TP_CLINK_RESET_L

SPI GSPI C-LINK

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=AITKEN SYNC_DATE=03/10/2017

PAGE TITLE

PCH DMI, PM, MISC

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NOTE: 1V8 BANKS ARE A,B,C,H

OMIT_TABLE

U7000
KBL-PCH-H
951678
FCBGA
SYM 7 OF 12
CRITICAL

NC	B7 USB3_1_RXN	USB2N_1 AH5	NC
NC	A7 USB3_1_RXP	USB2P_1 AH7	NC
NC	D13 USB3_1_TXN	USB2N_2 AE5	USB_EXTC_N
NC	C13 USB3_1_TXP	USB2P_2 AE7	USB_EXTC_P
162 53 IN USB3_EXTD_RX_F_N	C8 USB3_2_RXN	USB2N_3 AH8	USB_EXTB_N
162 53 IN USB3_EXTD_RX_F_P	B8 USB3_2_RXP	USB2P_3 AH10	USB_EXTB_P
162 53 OUT USB3_EXTD_TX_N	B13 USB3_2_TXN	USB2N_4 AE2	USB_EXTD_N
162 53 OUT USB3_EXTD_TX_P	A14 USB3_2_TXP	USB2P_4 AE3	USB_EXTD_P
162 52 IN USB3_EXTA_RX_F_N	B9 USB3_3_RXN	USB2N_5 AC2	USB_DBG_XA_N
162 52 IN USB3_EXTA_RX_F_P	A9 USB3_3_RXP	USB2P_5 AC3	USB_DBG_XA_P
162 52 OUT USB3_EXTA_TX_N	B14 USB3_3_TXN	USB2N_6 AF2	USB_UPC_XB_N
162 52 OUT USB3_EXTA_TX_P	C14 USB3_3_TXP	USB2P_6 AF1	USB_UPC_XB_P
167 58 IN USB3_SD_D2R_N	E11 USB3_4_RXN	USB2N_7 AB2	USB_UPC_TA_N
167 58 IN USB3_SD_D2R_P	G11 USB3_4_RXP	USB2P_7 AB1	USB_UPC_TA_P
SD 167 58 OUT USB3_SD_R2D_C_N	B15 USB3_4_TXN	USB2N_8 AM8	USB_UPC_TB_N
167 58 OUT USB3_SD_R2D_C_P	C15 USB3_4_TXP	USB2P_8 AM7	USB_UPC_TB_P
162 52 IN USB3_EXTB_RX_F_N	E13 USB3_5_RXN	USB2N_9 Y3	NC
162 52 IN USB3_EXTB_RX_F_P	G13 USB3_5_RXP	USB2P_9 Y2	NC
162 52 OUT USB3_EXTB_TX_N	A16 USB3_5_TXN	USB2N_10 AK8	USB_EXTA_N
162 52 OUT USB3_EXTB_TX_P	B16 USB3_5_TXP	USB2P_10 AK7	USB_EXTA_P
162 53 IN USB3_EXTC_RX_F_N	H15 USB3_6_RXN	USB2N_11 W2	NC
162 53 IN USB3_EXTC_RX_F_P	K15 USB3_6_RXP	USB2P_11 W1	NC
162 53 OUT USB3_EXTC_TX_N	C17 USB3_6_TXN	USB2N_12 AD3	USB2_SWDL_N
162 53 OUT USB3_EXTC_TX_P	D17 USB3_6_TXP	USB2P_12 AD2	USB2_SWDL_P
		USB2N_13 V3	USB2_ENET_ADAPTER_N
		USB2P_13 V2	USB2_ENET_ADAPTER_P
		USB2N_14 AK11	NC
		USB2P_14 AK13	NC
		GPP_E9/USB_OC0* AJ43	USB_EXTA_OC_L
		GPP_E10/USB_OC1* AH44	USB_EXTB_OC_L
		GPP_E11/USB_OC2* AM39	USB_EXTC_OC_L
		GPP_E12/USB_OC3* AK42	USB_EXTD_OC_L
		GPP_F15/USB_OC4* AD43	USB_UPC_XA_OC_L
		GPP_F16/USB_OC5* AC44	USB_UPC_XB_OC_L
		GPP_F17/USB_OC6* AH42	USB_UPC_TA_OC_L
		GPP_F18/USB_OC7* AC43	USB_UPC_TB_OC_L
		USB2_COMP AG3	PCH_USB_RBIAS
		USB2_ID AG2	PCH_USB_ID
		USB2_VBUSSENSE AE10	PCH_USB_VBUSSENSE

USB3 USB2

GPP_E[9-12] SERVE DUAL ROLE
AS USB OC AND/OR XDP OBSDATA_C[0-3]

PLACE_NEAR=U7000.AG3:11.4MM

R7201 1K 5% 1/16W MF-LF 402
R7218 0 5% 1/16W MF-LF 402
R7214 113 1% 1/20W MF 201

TODO: ASK INTEL WHAT TO DO WITH VBUSSENSE

OMIT_TABLE

U7000
KBL-PCH-H
951678
FCBGA
SYM 8 OF 12
PCIE/SATA/USB3
CRITICAL

38 IN PCIE_SOC_D2R_N<0>	K19 PCIE5_RXN	PCIE9_RXN/SATA0A_RXN	G31 NC
38 IN PCIE_SOC_D2R_P<0>	L19 PCIE5_RXP	PCIE9_RXP/SATA0A_RXP	H31 NC
44 OUT PCIE_SOC_R2D_C_N<0>	D22 PCIE5_TXN	PCIE9_TXN/SATA0A_TXN	D31 NC
44 OUT PCIE_SOC_R2D_C_P<0>	C22 PCIE5_TXP	PCIE9_TXP/SATA0A_TXP	C31 NC
158 38 IN PCIE_SOC_D2R_N<1>	G22 PCIE6_RXN	PCIE10_RXN/SATA1A_RXN	G29 NC
167 158 38 IN PCIE_SOC_D2R_P<1>	E22 PCIE6_RXP	PCIE10_RXP/SATA1A_RXP	E29 NC
44 OUT PCIE_SOC_R2D_C_N<1>	B22 PCIE6_TXN	PCIE10_TXN/SATA1A_TXN	B31 NC
44 OUT PCIE_SOC_R2D_C_P<1>	A23 PCIE6_TXP	PCIE10_TXP/SATA1A_TXP	A32 NC
158 38 IN PCIE_SOC_D2R_N<2>	L22 PCIE7_RXN	PCIE13_RXN/SATA0B_RXN	G35 NC
167 158 38 IN PCIE_SOC_D2R_P<2>	K22 PCIE7_RXP	PCIE13_RXP/SATA0B_RXP	E35 NC
44 OUT PCIE_SOC_R2D_C_N<2>	C23 PCIE7_TXN	PCIE13_TXN/SATA0B_TXN	C36 NC
44 OUT PCIE_SOC_R2D_C_P<2>	B23 PCIE7_TXP	PCIE13_TXP/SATA0B_TXP	B36 NC
38 IN PCIE_SOC_D2R_N<3>	K24 PCIE8_RXN	PCIE14_RXN/SATA1B_RXN	E37 NC
38 IN PCIE_SOC_D2R_P<3>	L24 PCIE8_RXP	PCIE14_RXP/SATA1B_RXP	G37 NC
44 OUT PCIE_SOC_R2D_C_N<3>	C24 PCIE8_TXN	PCIE14_TXN/SATA1B_TXN	A37 NC
44 OUT PCIE_SOC_R2D_C_P<3>	B24 PCIE8_TXP	PCIE14_TXP/SATA1B_TXP	B37 NC
NC	L31 PCIE11_RXN	PCIE15_RXN/SATA2_RXN	E41 NC
NC	K31 PCIE11_RXP	PCIE15_RXP/SATA2_RXP	C42 NC
NC	C32 PCIE11_TXN	PCIE15_TXN/SATA2_TXN	C38 NC
NC	B32 PCIE11_TXP	PCIE15_TXP/SATA2_TXP	B38 NC
NC	E33 PCIE12_RXN	PCIE16_RXN/SATA3_RXN	D42 NC
NC	G33 PCIE12_RXP	PCIE16_RXP/SATA3_RXP	E43 NC
NC	C33 PCIE12_TXN	PCIE16_TXN/SATA3_TXN	B39 NC
NC	B33 PCIE12_TXP	PCIE16_TXP/SATA3_TXP	A39 NC
167 134 IN PCIE_WLAN_D2R_N	T39 PCIE_21_RXN	PCIE17_RXN/SATA4_RXN	J41 NC
167 134 IN PCIE_WLAN_D2R_P	T41 PCIE_21_RXP	PCIE17_RXP/SATA4_RXP	K39 NC
167 134 OUT PCIE_WLAN_R2D_C_N	K43 PCIE_21_TXN	PCIE17_TXN/SATA4_TXN	F45 NC
167 134 OUT PCIE_WLAN_R2D_C_P	K44 PCIE_21_TXP	PCIE17_TXP/SATA4_TXP	F45 NC
NC	V35 PCIE_22_RXN	PCIE18_RXN/SATA5_RXN	M39 NC
NC	V36 PCIE_22_RXP	PCIE18_RXP/SATA5_RXP	M41 NC
NC	L43 PCIE_22_TXN	PCIE18_TXN/SATA5_TXN	G45 NC
NC	L44 PCIE_22_TXP	PCIE18_TXP/SATA5_TXP	G44 NC
NC	V39 PCIE_23_RXN	PCIE19_RXN/SATA6_RXN	P39 NC
NC	V41 PCIE_23_RXP	PCIE19_RXP/SATA6_RXP	P41 NC
NC	N44 PCIE_23_TXN	PCIE19_TXN/SATA6_TXN	H44 NC
NC	N45 PCIE_23_TXP	PCIE19_TXP/SATA6_TXP	H45 NC
NC	Y39 PCIE_24_RXN	PCIE20_RXN/SATA7_RXN	P38 NC
NC	Y41 PCIE_24_RXP	PCIE20_RXP/SATA7_RXP	P36 NC
NC	P43 PCIE_24_TXN	PCIE20_TXN/SATA7_TXN	J43 NC
NC	P44 PCIE_24_TXP	PCIE20_TXP/SATA7_TXP	J44 NC
NC	G15 PCIE1_RXN/USB3_7_RXN		
NC	E15 PCIE1_RXP/USB3_7_RXP		
NC	A18 PCIE1_TXN/USB3_7_TXN	GPP_E4/DEVSLP0 AL44	XDP_OBSDATA_A_3 73 167
NC	B18 PCIE1_TXP/USB3_7_TXP	GPP_E5/DEVSLP1 AL45	XDP_OBSDATA_B_0 73 167
		GPP_E6/DEVSLP2 AK44	XDP_OBSDATA_B_1 73 167
NC	E17 PCIE2_RXN/USB3_8_RXN	GPP_F5/DEVSLP3 AF44	MEM_OK OUT 68 153
NC	G17 PCIE2_RXP/USB3_8_RXP	GPP_F6/DEVSLP4 AG41	NC
NC	B19 PCIE2_TXN/USB3_8_TXN	GPP_F7/DEVSLP5 AH39	TBT_PLUG_EVENT_L 68
NC	C19 PCIE2_TXP/USB3_8_TXP	GPP_F8/DEVSLP6 AH36	TP_PCH_GPP_F8 72
		GPP_F9/DEVSLP7 AF45	TP_PCH_GPP_F9 72
159 IN USB3_SWDL_D2R_N	L17 PCIE3_RXN/USB3_9_RXN	GPP_E8/SATALED* AJ44	XDP_OBSDATA_B_3 73 167
159 IN USB3_SWDL_D2R_P	K17 PCIE3_RXP/USB3_9_RXP		
159 OUT USB3_SWDL_R2D_N	B20 PCIE3_TXN/USB3_9_TXN		
159 OUT USB3_SWDL_R2D_P	C20 PCIE3_TXP/USB3_9_TXP		
159 IN USB3_ENET_ADAPTER_D2R_N	E19 PCIE4_RXN/USB3_10_RXN		
159 IN USB3_ENET_ADAPTER_D2R_P	G19 PCIE4_RXP/USB3_10_RXP		
159 OUT USB3_ENET_ADAPTER_R2D_N	B21 PCIE4_TXN/USB3_10_TXN		
159 OUT USB3_ENET_ADAPTER_R2D_P	A21 PCIE4_TXP/USB3_10_TXP		
167 73 BI XDP_OBSFN_C_0	AM36 GPP_E0/SATAXPCIE0/SATAGP0		
167 73 BI XDP_OBSDATA_A_0	AM35 GPP_E1/SATAXPCIE1/SATAGP1		
167 73 BI XDP_OBSDATA_A_1	AM38 GPP_E2/SATAXPCIE2/SATAGP2		
167 73 BI XDP_OBSDATA_D_0	AK36 GPP_F0/SATAXPCIE3/SATAGP3		
167 73 BI XDP_OBSDATA_D_1	AK33 GPP_F1/SATAXPCIE4/SATAGP4		
167 73 BI XDP_OBSDATA_D_2	AK38 GPP_F2/SATAXPCIE5/SATAGP5		
167 73 BI XDP_OBSDATA_D_3	AH43 GPP_F3/SATAXPCIE6/SATAGP6		
73 72 69 BI JTAG_ISP_TDO	AE42 GPP_F4/SATAXPCIE7/SATAGP7		
72 TP_PCH_GPP_F10	AE30 GPP_F10/SCLOCK		
72 TP_PCH_GPP_F11	AH35 GPP_F11/SLOAD		
72 TP_PCH_GPP_F12	AE44 GPP_F12/SDATAOUT1		
165 72 OUT ENET_SYNC_1588_OUT	AE43 GPP_F13/SDATAOUT0		
167 PCIE_RCOMPP	C10 PCIE_RCOMPP		
167 PCIE_RCOMPN	B10 PCIE_RCOMPN		

AWAITING RESPONSE FROM SRINI
WHAT DO WE DO WITH UNUSED SATA?

PLACE_NEAR=U7000.C10:10MM
R7215 100 1% 1/20W MF 201

NOTE:
GPP_F4 CAN BE USED AS
XDP_OBSDEN_C_1 BY
STUFFING R7799

PP3V3_S0 117 118 119 120 143 148 151 153 155 156 12 46 47 49 65 66 69 76 78 84 85 88 94 97 98 99 103 105 106 107 108 109 111 112 116 159

R7286 100K 5% 1/20W MF 201 — TBT_PLUG_EVENT_L 68

PP3V3_S5 13 17 43 54 67 70 72 73 76 77 78 105 145 153 156 159

R7203	10K	5% 1/20W MF 201	USB_EXTA_OC_L 52 68 73
R7204	10K	5% 1/20W MF 201	USB_EXTC_OC_L 53 68 73
R7207	10K	5% 1/20W MF 201	USB_EXTB_OC_L 52 68 73
R7208	10K	5% 1/20W MF 201	USB_EXTD_OC_L 53 68 73
R7240	10K	5% 1/20W MF 201	USB_UPC_XA_OC_L 33 68
R7241	10K	5% 1/20W MF 201	USB_UPC_XB_OC_L 34 68
R7242	10K	5% 1/20W MF 201	USB_UPC_TA_OC_L 27 68
R7243	10K	5% 1/20W MF 201	USB_UPC_TB_OC_L 28 68
R7298	100K	5% 1/20W MF 201	MEM_OK 68 153

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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PCH PCIE, USB

Apple Inc.

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TOP-BLOCK SWAP

PP1V8_S5 — 17 36 43 44 45 47 53 59 63 66 67 69 70 72 74 137 145 146 147 148 159

R7399 1K 5% 1/20W MF 201

TP_SMC_TOPBLK_SWP_L — R7398 1K 5% 1/20W MF 201 — PCH_STRP_TOPBLK_SWP_L 69

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GPPA/INTEGRATED SENSOR

69 32 BI	SOC_SWD_IO	BE17	GPP_A17/ISH_GP7
159 32 OUT	SOC_SWD_MUX_SEL	BD19	GPP_A18/ISH_GP0
69 36 IN	PCH_GCON_INT_L	BE18	GPP_A19/ISH_GP1
69 59 IN	SDCONN_OC_L	BE19	GPP_A20/ISH_GP2
137 IN	PCH_WIFI_AUDIO_TIMESYNC	BF18	GPP_A21/ISH_GP3
72 69	TP_PCH_GPP_A22	BG16	GPP_A22/ISH_GP4
138 69 OUT	PCH_BT_DEV_WAKE	BE19	GPP_A23/ISH_GP5

GPPB

NC		AY22	GPP_B0
137 OUT	PCH_BT_ROM_BOOT_L	AV19	GPP_B1
35 OUT	PCH_SOC_SYNC	AR17	GPP_B11
69	PCH_STRP_TOPBLK_SWP_L	AU24	GPP_B14/SPKR

GPPC/SMLINK/I2C/UART

GPPD/INTEGRATED SENSOR/UART/I2C

72 69 OUT	JTAG_TBT_X_TMS_PCH	AV41	GPP_D0
72 69 OUT	JTAG_TBT_T_TMS_PCH	AY39	GPP_D1
NC		BB44	GPP_D2
72 69 IN	JTAG_ISP_TDI	AV43	GPP_D3
72	TP_PCH_GPP_D9	AT45	GPP_D9
72	TP_PCH_GPP_D10	AV39	GPP_D10
NC		AT38	GPP_D11
NC		AT41	GPP_D12
72 69 OUT	TBT_X_PWR_EN_PCH	AP44	GPP_D13/ISH_UART0_RXD/I2C2_SDA
69 34 33 32 30 OUT	TBT_X_USB_PWR_EN	AP43	GPP_D14/ISH_UART0_TXD/I2C2_SCL
72 69 OUT	TBT_T_PWR_EN_PCH	AT44	GPP_D15/ISH_UART0_RTS*
69 28 27 24 OUT	TBT_T_USB_PWR_EN	AT39	GPP_D16/ISH_UART0_CTS*
NC		AM44	GPP_D21
69 34 33 32 28 27 26 OUT	TBT_POC_RESET	AM42	GPP_D22
72 69 IN	JTAG_ISP_TCK	AU44	GPP_D4/ISH_I2C2_SDA/ISH_I2C3_SDA
NC		AN44	GPP_D23/ISH_I2C2_SCL/ISH_I2C3_SCL

CRITICAL

GPP_C0/SMBCLK	BF38	SMBUS_PCH_CLK	OUT 46
GPP_C1/SMBDATA	BC42	SMBUS_PCH_DATA	BI 46
GPP_C2/SMBALERT*	BF41	PCH_STRP_TLSCONF	69
GPP_C3/SML0CLK	BE37	SML_PCH_0_CLK	OUT 46
GPP_C4/SML0DATA	BC33	SML_PCH_0_DATA	BI 46
GPP_C5/SML0ALERT*	BC35	PCH_STRP_ESPI	69
GPP_C6/SML1CLK	BC43	I2C_MLBSNS_PCH_SML1_SCL	IN 47
GPP_C7/SML1DATA	BF38	I2C_MLBSNS_PCH_SML1_SDA	BI 47
GPP_C8/UART0_RXD	BA39	BT_UART_D2R	IN 137
GPP_C9/UART0_TXD	BC39	BT_UART_R2D	OUT 137
GPP_C10/UART0_RTS*	BF39	BT_UART_RTS_L	OUT 137
GPP_C11/UART0_CTS*	BC45	BT_UART_CTS_L	IN 137
GPP_C12/UART1_RXD/ISH_UART1_RXD	BB45	WLAN_UART_D2R	IN 137
GPP_C13/UART1_TXD/ISH_UART1_TXD	BA44	WLAN_UART_R2D	OUT 137
GPP_C14/UART1_RTS*/ISH_UART1_RTS*	BA45	WLAN_UART_RTS_L	OUT 137
GPP_C15/UART1_CTS*/ISH_UART1_CTS*	BA35	WLAN_UART_CTS_L	IN 137
GPP_C16/I2C0_SDA	AY45	NC	
GPP_C17/I2C0_SCL	AY33	NC	
GPP_C18/I2C1_SDA	AY35	NC	
GPP_C19/I2C1_SCL	AW44	NC	
GPP_C20/UART2_RXD	AY44	PCH_DEBUG_UART_D2R	IN 34 69 72 159
GPP_C21/UART2_TXD	BA33	PCH_DEBUG_UART_R2D	OUT 34 69 72 159
GPP_C22/UART2_RTS*	AW43	TP_GPP_C22	
GPP_C23/UART2_CTS*	AW42	PCH_UART2_CTS_L	69 165

PP1V8_S5 — 17 36 43 44 45 47 53 59 63 66 67 69 70 72 74 137 145 146 147 148 159

R7355	47K	5% 1/20W MF 201	PCH_DEBUG_UART_R2D	34 69 72 159
R7356	47K	5% 1/20W MF 201	PCH_DEBUG_UART_D2R	34 69 72 159
R7313	1K	5% 1/16W MF-LF 402	PCH_STRP_ESPI	69
R7304	10K	NOSTUFF 5% 1/20W MF 201	PCH_STRP_TLSCONF	69
R7383	1K	5% 1/16W MF-LF 402	PCH_STRP_SPIROM_SAF	69 167
R7384	100K	5% 1/20W MF 201	SDCONN_OC_L	59 69
R7387	100K	5% 1/20W MF 201	SOC_SWD_IO	32 69
R7388	100K	5% 1/20W MF 201	PCH_GCON_INT_L	36 69

PP3V3_S0 — 116 117 118 119 120 143 148 151 153 155 12 46 47 53 65 66 68 70 75 78 84 95 88 94 97 98 99 103 105 106 107 108 109 111 112 156 159

R7325	100K	5% 1/20W MF 201	TCON_RESET_R_L	69
R7315	10K	5% 1/20W MF 201	JTAG_ISP_TDO	68 72 73
R7381	10K	5% 1/20W MF 201	JTAG_TBT_X_TMS_PCH	69 72
R7382	10K	5% 1/20W MF 201	JTAG_TBT_T_TMS_PCH	69 72
R7379	100K	NOSTUFF 5% 1/20W MF 201	TCON_RESET_L	69 108

PP3V3_S0_TBT — 26 32 78 161

R7353	100K	5% 1/20W MF 201	TBT_X_PWR_EN_PCH	69 72
R7350	100K	5% 1/20W MF 201	TBT_T_PWR_EN_PCH	69 72
R7351	100K	5% 1/20W MF 201	TBT_X_USB_PWR_EN	30 32 33 34 69
R7352	100K	5% 1/20W MF 201	TBT_T_USB_PWR_EN	24 27 28 69

PP3V3_S0 — 116 117 118 119 120 143 148 151 153 155 12 46 47 53 65 66 68 70 75 78 84 95 88 94 97 98 99 103 105 106 107 108 109 111 112 156 159

R7316	100K	NOSTUFF 5% 1/20W MF 201	JTAG_ISP_TDI	69 72
R7318	100K	5% 1/20W MF 201		

R7361	100K	5% 1/20W MF 201	TP_PCH_GPP_A22	69 72
R7360	100K	5% 1/20W MF 201	PCH_BT_DEV_WAKE	69 138
R7371	100K	5% 1/20W MF 201	PD_PCH_GPP_I4	69 165
R7375	47K	5% 1/20W MF 201	PCH_UART2_CTS_L	69 165
R7385	100K	5% 1/20W MF 201	USB_EXTA_HILIM_EN	52 69
R7386	100K	5% 1/20W MF 201	USB_EXTC_HILIM_EN	53 69
R7392	100K	5% 1/20W MF 201	TBT_POC_RESET	24 27 28 32 33 34 69
R7314	10K	5% 1/20W MF 201	JTAG_ISP_TCK	69 72
R7372	100K	5% 1/20W MF 201	PD_PCH_GPP_I0	69 165
R7373	100K	5% 1/20W MF 201	PD_PCH_GPP_I1	69 165
R7374	100K	5% 1/20W MF 201	PD_PCH_GPP_I2	69 165

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CRITICAL

108 69 OUT TCON_RESET_L — R7305 33 5% 1/20W MF 201 — TCON_RESET_R_L 69

165 72 IN	ENET_SYNC_1588_IN	AD44	GPP_F14
NC		AC42	GPP_F19/EDP_VDDEN
NC		AE35	GPP_F20/EDP_BKLTEN
NC		AE36	GPP_F21/EDP_BKLTCTL
	TCON_RESET_R_L	AB45	GPP_F22
72	TP_PCH_GPP_F23	AE39	GPP_F23

GPPF/BACKLIGHT

165 69	PD_PCH_GPP_I0	AP7	GPP_I0/DDPB_HPD0
165 69	PD_PCH_GPP_I1	AT8	GPP_I1/DDPC_HPD1
165 69	PD_PCH_GPP_I2	AP8	GPP_I2/DDPD_HPD2
NC		AT7	GPP_I3/DDPE_HPD3
165 69	PD_PCH_GPP_I4	BA1	GPP_I4/EDP_HPD
NC		AW5	GPP_I5/DDPB_CTRLCLK
NC		AV7	GPP_I6/DDPB_CTRLDATA
NC		AT5	GPP_I7/DDPC_CTRLCLK
NC		BA6	GPP_I8/DDPC_CTRLDATA
NC		AY1	GPP_I9/DDPD_CTRLCLK
NC		AY2	GPP_I10/DDPD_CTRLDATA

GPPI/DISPLAY

GPPG

72	TP_PCH_GPP_H10	BF32	GPP_H10/SML2CLK
72	TP_PCH_GPP_H11	AU31	GPP_H11/SML2DATA
167 69	PCH_STRP_SPIROM_SAF	BF33	GPP_H12/SML2ALERT* (IPD)
72	TP_PCH_GPP_H13	BE33	GPP_H13/SML3CLK
72	TP_PCH_GPP_H14	AV31	GPP_H14/SML3DATA
NC		BD33	GPP_H15/SML3ALERT*
NC		BD36	GPP_H16/SML4CLK
NC		BF32	GPP_H17/SML4DATA
NC		BF34	GPP_H18/SML4ALERT*
72	TP_PCH_GPP_H19	AY31	GPP_H19/ISH_I2C0_SDA
72	TP_PCH_GPP_H20	BE36	GPP_H20/ISH_I2C0_SCL
NC		BF37	GPP_H21/ISH_I2C1_SDA
NC		BF36	GPP_H22/ISH_I2C1_SCL
NC		BG34	GPP_H23

GPPH/I2C/INTEGRATED SENSOR/SMLINK

H12 IS READ ON DF-ASSERTION EDGE OF RESUME RESET
LOW (DEFAULT) IS MAF, HIGH WILL FORCE SAF

GPP_G0	AA43	USB_EXTA_HILIM_EN	OUT 52 69
GPP_G1	AB44	NC	
GPP_G2	AC36	USB_EXTC_HILIM_EN	OUT 53 69
GPP_G3	T44	NC	
GPP_G4	AC33	NC	
GPP_G5	V43	NC	
GPP_G6	Y42	NC	
GPP_G7	AA44	NC	
GPP_G8	W44	NC	
GPP_G9	Y44	NC	
GPP_G10	AC35	NC	
GPP_G11	AC41	NC	
GPP_G12/GSXDOUT	AC39	NC	
GPP_G13/GSXSLOAD	Y36	NC	
GPP_G14/GSXDIN	Y43	NC	
GPP_G15/GSXRESET*	U44	NC	
GPP_G16/GSXCLK	T43	NC	
GPP_G17/ADR_COMPLETE	V42	NC	
GPP_G18/NMI*	U45	NC	
GPP_G19/SMI*	R43	NC	
GPP_G20	Y35	NC	
GPP_G21	AC30	NC	
GPP_G22	R45	NC	
GPP_G23	R44	NC	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=AITKEN — SYNC_DATE=03/10/2017

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PCH GPIO

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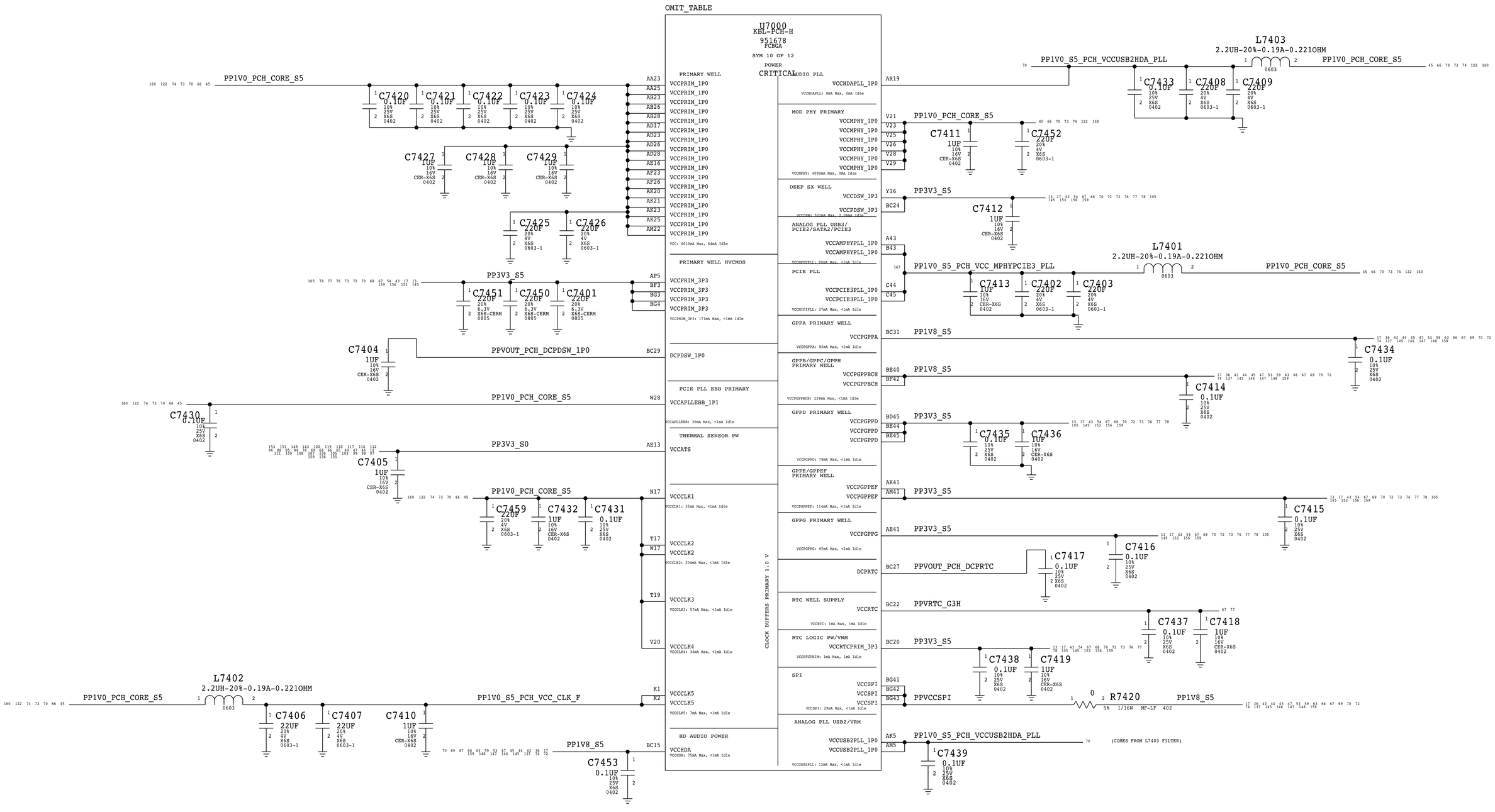

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SYNC_MASTER=AITKEN SYNC_DATE=03/08/2017

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PCH POWER, DECOUPLING

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OMIT_TABLE

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A12	VSS	VSS	AK10
A2	VSS	VSS	AK14
A25	VSS	VSS	AK16
A3	VSS	VSS	AK17
A30	VSS	VSS	AK18
A35	VSS	VSS	AK26
A4	VSS	VSS	AK28
A40	VSS	VSS	AK29
A41	VSS	VSS	AK30
A42	VSS	VSS	AK32
A44	VSS	VSS	AK35
A6	VSS	VSS	AK39
AA17	VSS	VSS	AL4
AA18	VSS	VSS	AL42
AA20	VSS	VSS	AM10
AA21	VSS	VSS	AM11
AA26	VSS	VSS	AM13
AA28	VSS	VSS	AM14
AA29	VSS	VSS	AM17
AB17	VSS	VSS	AM19
AB18	VSS	VSS	AM24
AB20	VSS	VSS	AM27
AB21	VSS	VSS	AM29
AB25	VSS	VSS	AM32
AB29	VSS	VSS	AM33
AB4	VSS	VSS	AM4
AB42	VSS	VSS	AN14
AC10	VSS	VSS	AN45
AC11	VSS	VSS	AP10
AC14	VSS	VSS	AP11
AC16	VSS	VSS	AP13
AC32	VSS	VSS	AP15
AC38	VSS	VSS	AP19
AC4	VSS	VSS	AP22
AC5	VSS	VSS	AP27
AC7	VSS	VSS	AP31
AC8	VSS	VSS	AP33
AD1	VSS	VSS	AP34
AD18	VSS	VSS	AP39
AD20	VSS	VSS	AR13
AD21	VSS	VSS	AR22
AD25	VSS	VSS	AR27
AD29	VSS	VSS	AR31
AD45	VSS	VSS	AR33
AE11	VSS	VSS	AR4
AE14	VSS	VSS	AT10
AE32	VSS	VSS	AT13
AE33	VSS	VSS	AT35
AE38	VSS	VSS	AT37
AE4	VSS	VSS	AT42
AE8	VSS	VSS	AU11
AF18	VSS	VSS	AU17
AF20	VSS	VSS	AU29
AF21	VSS	VSS	AU33
AF25	VSS	VSS	AV1
AF28	VSS	VSS	AV10
AF29	VSS	VSS	AV15
AF4	VSS	VSS	AV24
AF42	VSS	VSS	AV27
AG18	VSS	VSS	AV33
AG20	VSS	VSS	AV35
AG21	VSS	VSS	AV38
AG23	VSS	VSS	AV45
AG25	VSS	VSS	AV8
AG26	VSS	VSS	AY11
AG28	VSS	VSS	AY19
AG29	VSS	VSS	AY37
AH11	VSS	VSS	AY4
AH13	VSS	VSS	AY42
AH30	VSS	VSS	AY8
AH32	VSS	VSS	B1
AH33	VSS	VSS	B12
AH38	VSS	VSS	B2
AJ1	VSS	VSS	B25
AJ17	VSS	VSS	B3
AJ18	VSS	VSS	B30
AJ20	VSS	VSS	B35
AJ21	VSS	VSS	B4
AJ23	VSS	VSS	B41
AJ25	VSS	VSS	B44
AJ26	VSS	VSS	B45
AJ28	VSS	VSS	BA13
AJ29	VSS	VSS	BA17
AJ45	VSS	VSS	BA29

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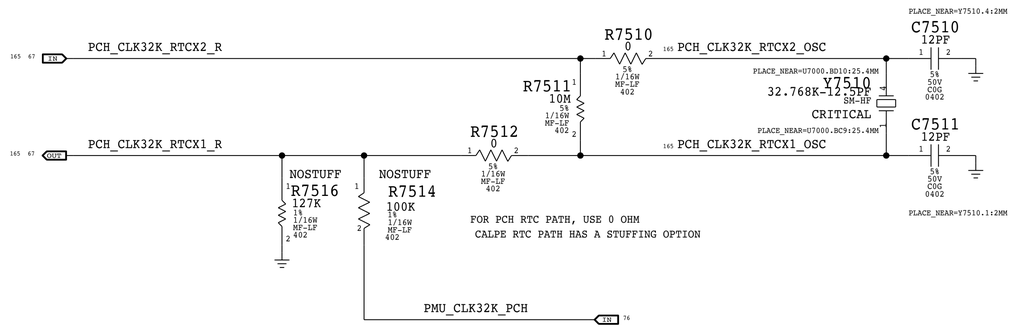
BA31	VSS	VSS	K13
BA37	VSS	VSS	K27
BA4	VSS	VSS	K3
BA42	VSS	VSS	K33
BB40	VSS	VSS	K35
BC38	VSS	VSS	K36
BC40	VSS	VSS	K38
BC9	VSS	VSS	K45
BD1	VSS	VSS	K8
BD11	VSS	VSS	L13
BD16	VSS	VSS	L15
BD2	VSS	VSS	L35
BD21	VSS	VSS	L4
BD25	VSS	VSS	L42
BD30	VSS	VSS	M11
BD34	VSS	VSS	M36
BD39	VSS	VSS	M38
BD7	VSS	VSS	M4
BE1	VSS	VSS	M8
BE2	VSS	VSS	M9
BF2	VSS	VSS	N13
BF43	VSS	VSS	N15
BF44	VSS	VSS	N19
BF45	VSS	VSS	N22
BF5	VSS	VSS	N24
BG14	VSS	VSS	N31
BG18	VSS	VSS	N42
BG23	VSS	VSS	P10
BG28	VSS	VSS	P12
BG32	VSS	VSS	P13
BG37	VSS	VSS	P15
BG40	VSS	VSS	P17
BG44	VSS	VSS	P19
BG9	VSS	VSS	P22
C1	VSS	VSS	P31
C2	VSS	VSS	P33
C37	VSS	VSS	P35
C9	VSS	VSS	P4
D1	VSS	VSS	P42
D10	VSS	VSS	P8
D12	VSS	VSS	R1
D15	VSS	VSS	R32
D16	VSS	VSS	T10
D19	VSS	VSS	T14
D21	VSS	VSS	T22
D24	VSS	VSS	T29
D25	VSS	VSS	T32
D29	VSS	VSS	T36
D30	VSS	VSS	T38
D33	VSS	VSS	T4
D35	VSS	VSS	T42
D36	VSS	VSS	T5
D39	VSS	VSS	U4
D44	VSS	VSS	U42
D45	VSS	VSS	V10
D7	VSS	VSS	V14
E31	VSS	VSS	V16
E6	VSS	VSS	V17
E8	VSS	VSS	V18
F2	VSS	VSS	V30
F39	VSS	VSS	V32
F43	VSS	VSS	V33
F6	VSS	VSS	V38
G4	VSS	VSS	V4
G40	VSS	VSS	V8
G42	VSS	VSS	W18
G9	VSS	VSS	W20
H11	VSS	VSS	W21
H13	VSS	VSS	W23
H17	VSS	VSS	W25
H19	VSS	VSS	W26
H22	VSS	VSS	W29
H24	VSS	VSS	W3
H27	VSS	VSS	W45
H29	VSS	VSS	Y13
H33	VSS	VSS	Y14
H35	VSS	VSS	Y30
H38	VSS	VSS	Y32
H4	VSS	VSS	Y33
H42	VSS	VSS	Y38
H9	VSS	VSS	Y4
J4	VSS	VSS	Y8
K11	VSS		

PCH RTC Crystal



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=AITKEN SYNC_DATE=02/07/2017

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PCH GND, RTC, ME

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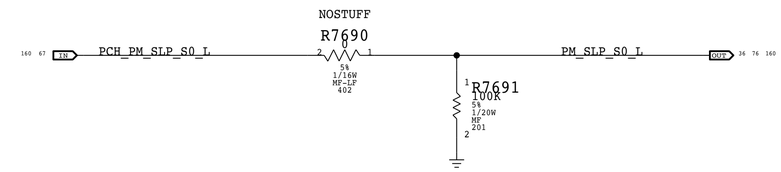
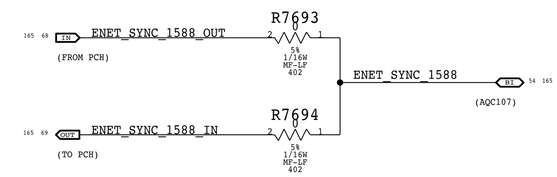
TP7616	TP-P5	TP_HDA_SDI1	66
TP7617	TP-P5	TP_HDA_BCLK	66
TP7618	TP-P5	TP_HDA_SDIO	66
TP7619	TP-P5	TP_PCH_GPD9	67
TP7620	TP-P5	TP_GPP_A10	66
TP7621	TP-P5	TP_PCH_GPP_H19	69
TP7622	TP-P5	TP_PCH_GPP_D10	69
TP7623	TP-P5	TP_PCH_GPP_H14	69
TP7624	TP-P5	TP_PCH_GPP_H7	66
TP7625	TP-P5	TP_PCH_GPD8	67
TP7626	TP-P5	TP_PCH_SLP_LAN_L	67
TP7627	TP-P5	TP_CLINK_RESET_L	67
TP7628	TP-P5	TP_CLINK_CLK	67
TP7629	TP-P5	TP_CLINK_DATA	67
TP7630	TP-P5	TP_FPF_VREF	66
TP7631	TP-P5	TP_PCH_GPP_H11	69
TP7632	TP-P5	TP_PCH_GPP_D9	69
TP7634	TP-P5	TP_FPF_MON	66
TP7635	TP-P5	TP_PCH_2_CPU_TRIGGER	67
TP7636	TP-P5	TP_CPU_2_PCH_TRIGGER	67
TP7637	TP-P5	PCH_PM_DOWN	13 67 160
TP7638	TP-P5	TP_PCH_GPP_F11	68
TP7639	TP-P5	TP_PCH_GPP_F8	68
TP7640	TP-P5	TP_PCH_GPP_F9	68
TP7641	TP-P5	TP_PCH_GPP_F12	68
TP7644	TP-P5	TP_PCH_GPP_F23	69
TP7645	TP-P5	TP_PCH_GPP_F10	68
TP7646	TP-P5	TP_KBLX_CLK24M	66
TP7648	TP-P5	TP_PCH_GPP_A22	69
TP7649	TP-P5	TP_PCH_GPP_B23	67

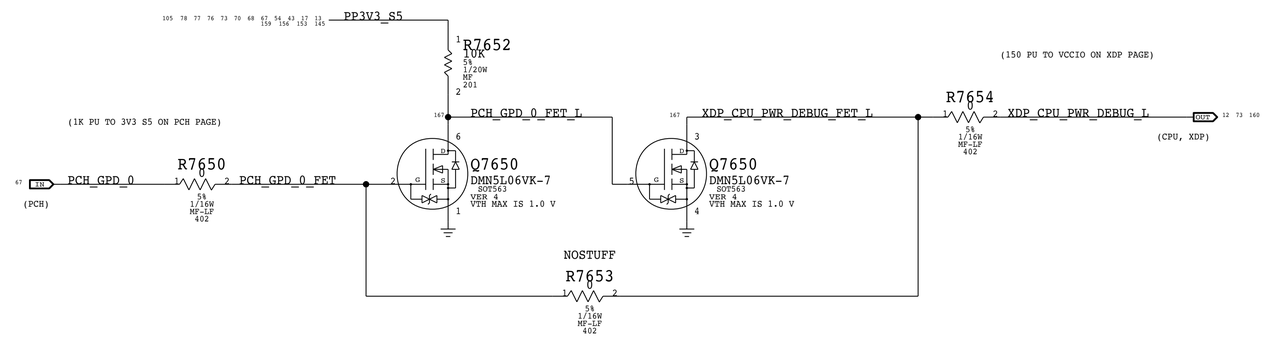
PM_SLP_S0_L OPTION



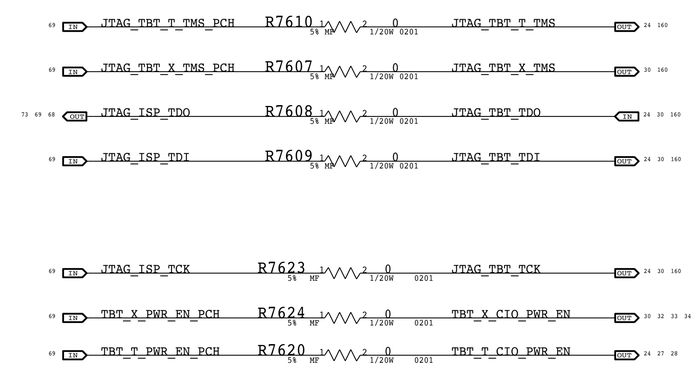
ETHERNET TIMESYNC



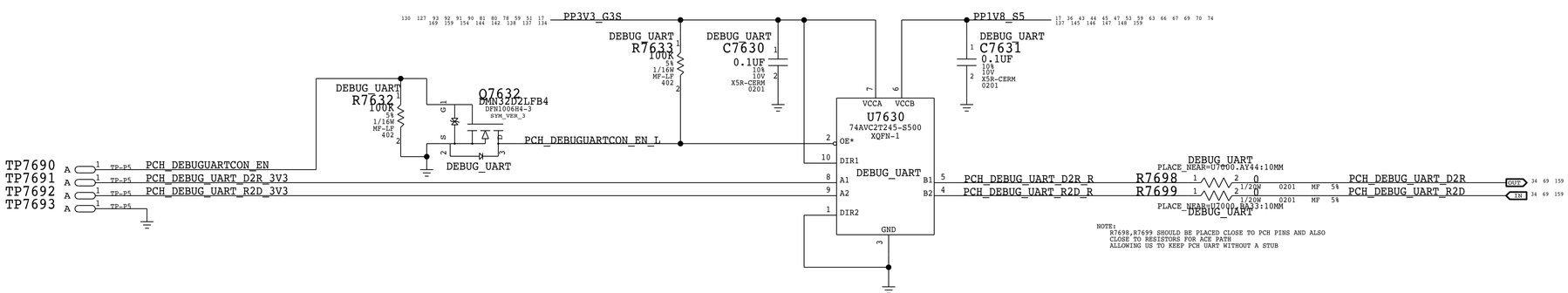
XDP HOOK[2] LEVEL SHIFTER



RIDGE JTAG ISOLATION



PCH DEBUG UART HEADER



NOTE:
R7698,R7699 SHOULD BE PLACED CLOSE TO PCH PINS AND ALSO CLOSE TO RESISTORS FOR ACE PATH
ALLOWING US TO KEEP PCH UART WITHOUT A STUB

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=AITKEN SYNC_DATE=03/10/2017

PAGE TITLE

PCH SUPPORT

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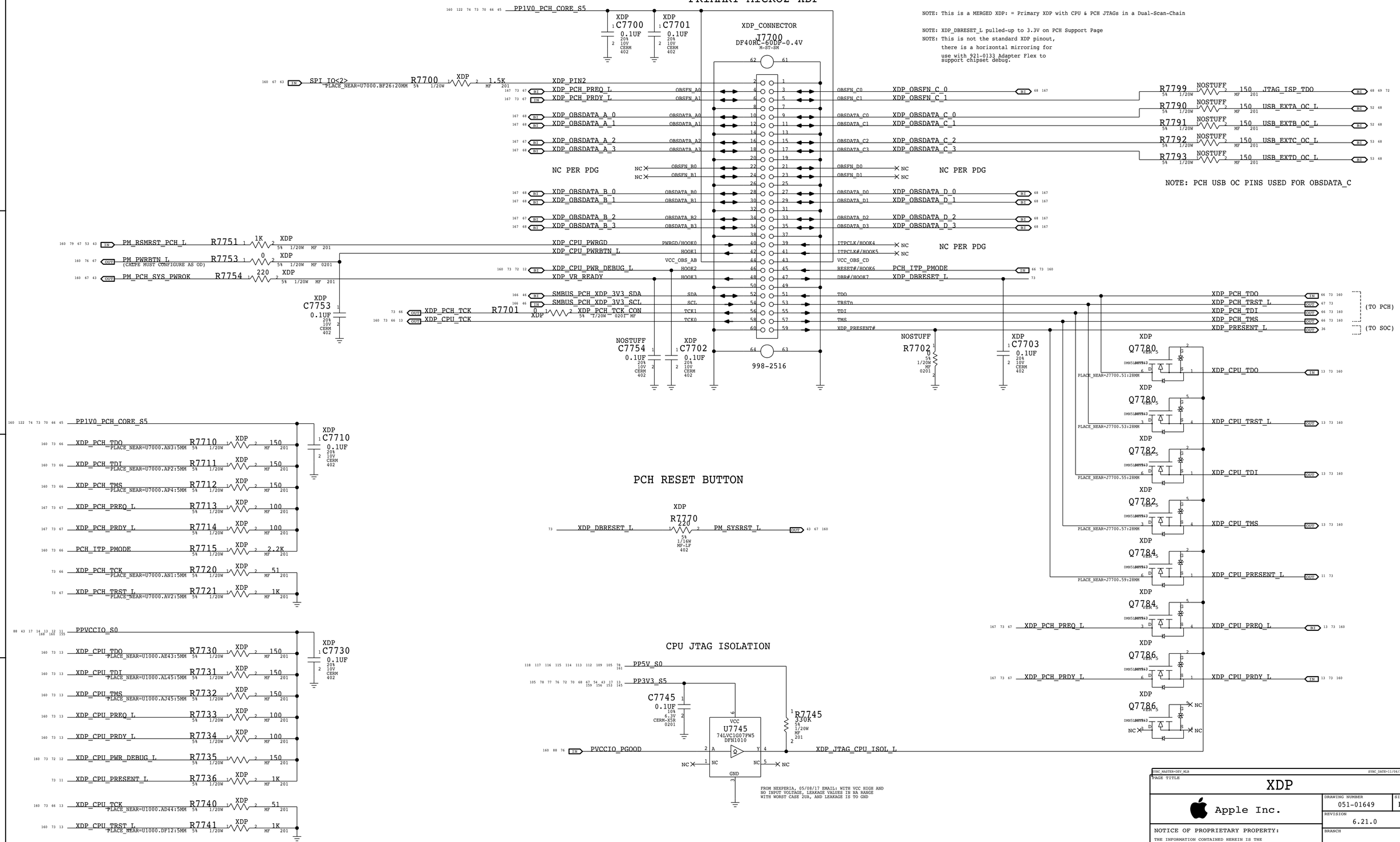
PRIMARY MICRO2-XDP

NOTE: This is a MERGED XDP: = Primary XDP with CPU & PCH JTAGs in a Dual-Scan-Chain

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

NOTE: This is not the standard XDP pinout, there is a horizontal mirroring for use with 921-0133 Adapter Flex to support chipset debug.



NOTE: JTAG PINS CAN BE LEFT FLOATING ON PCH AND CPU

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=DEV_MLB	SYNC_DATE=11/06/2016
PAGE TITLE	XDP
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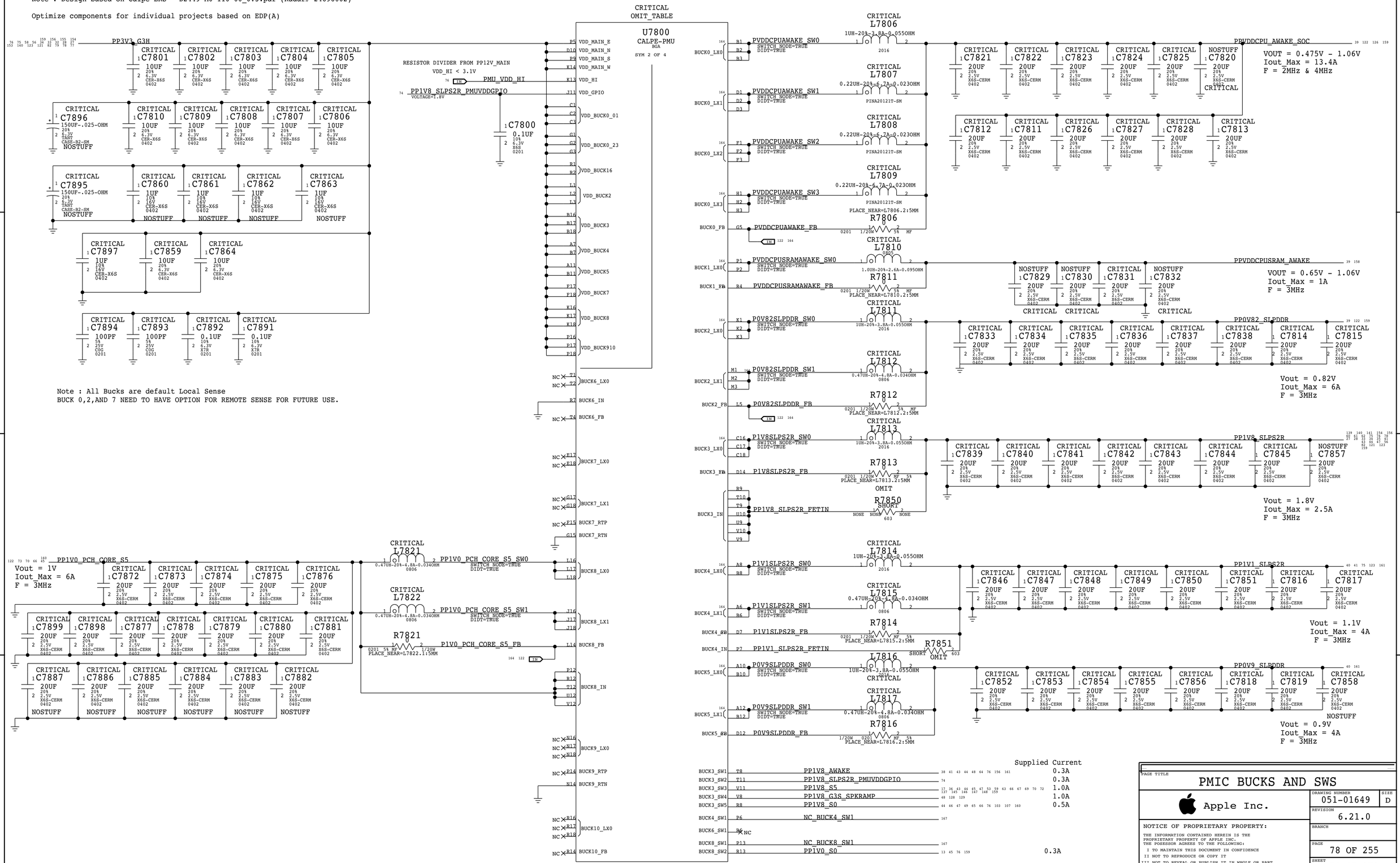
Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)

Optimize components for individual projects based on EDP(A)



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PMIC BUCKS AND SWS

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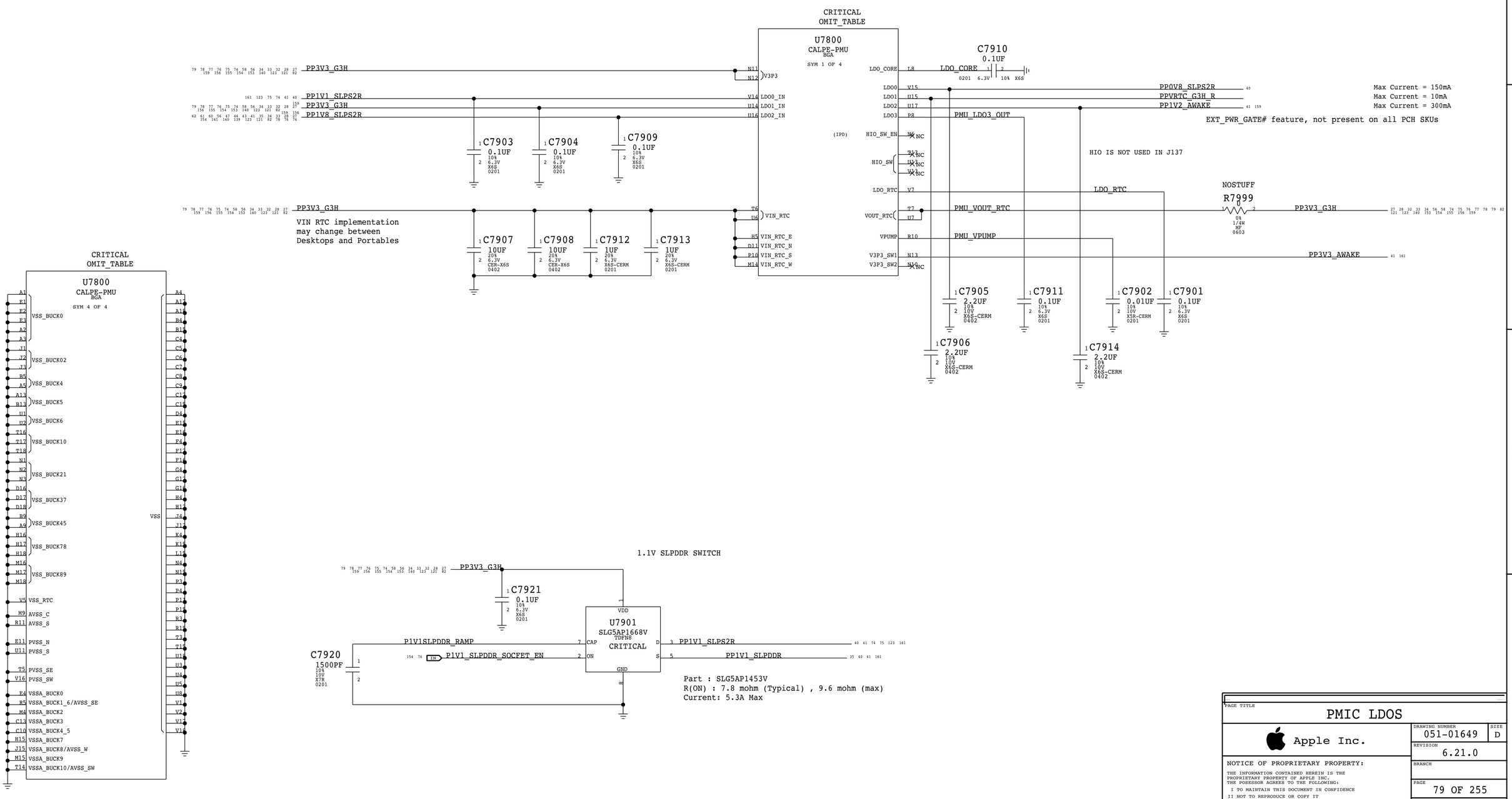

BOM_COST_GROUP=SOC

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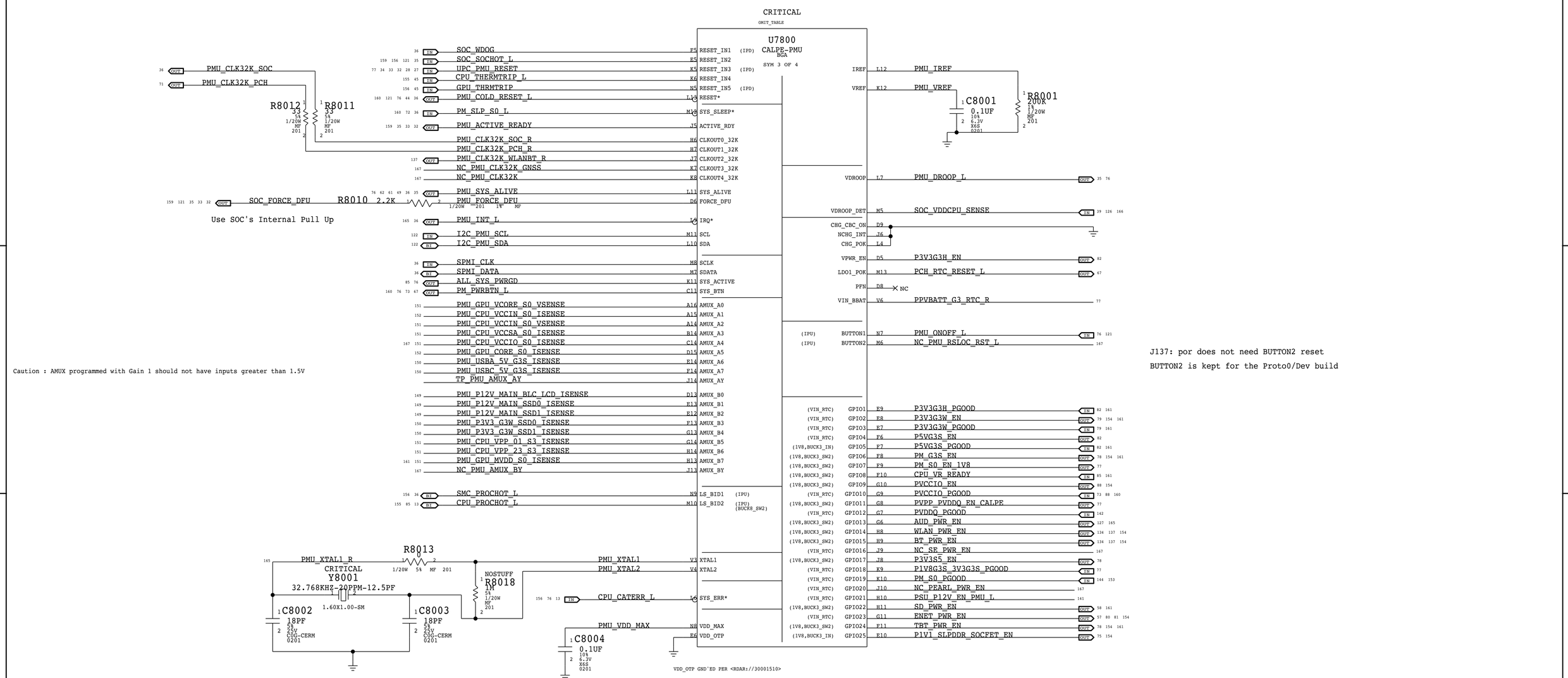
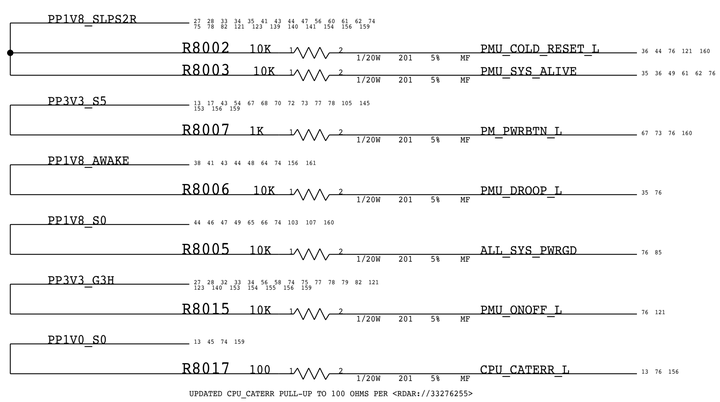


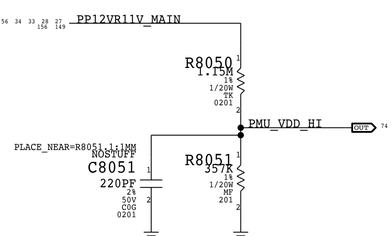
Caution : AMUX programmed with Gain 1 should not have inputs greater than 1.5V

J137: por does not need BUTTON2 reset

BUTTON2 is kept for the Proto0/Dev build



VDD_HI THRESHOLD



PBUS	Rising Vth	Falling Vth
12V	9.076V	8.443V

BOM_COST_GROUP=SOC

PAGE TITLE
PMIC GPIOS & CONTROL

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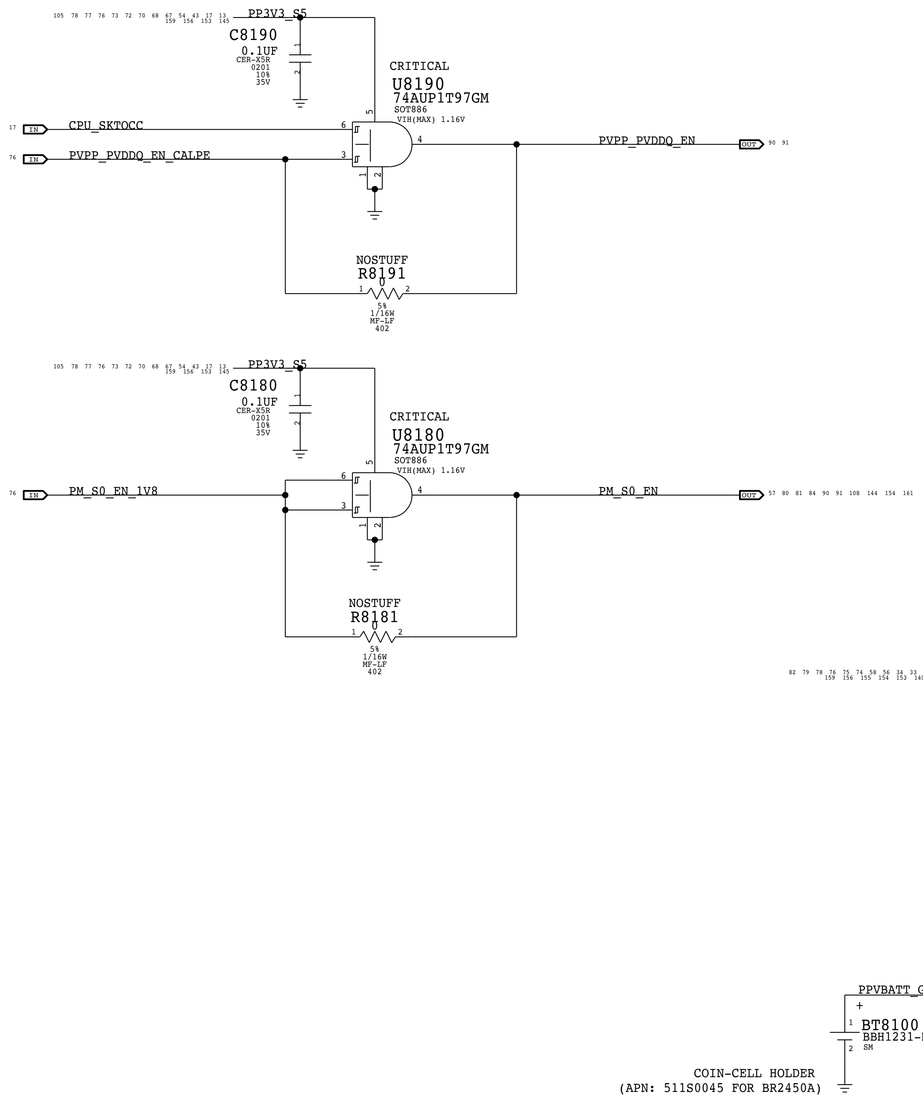
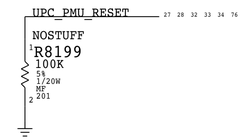
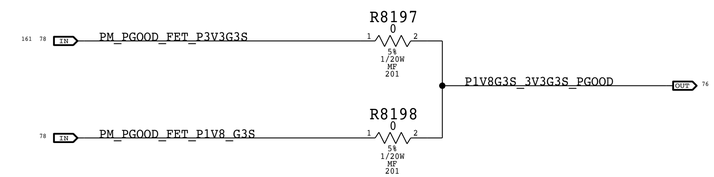
GATE S3 BY SOCKET OCCUPIED



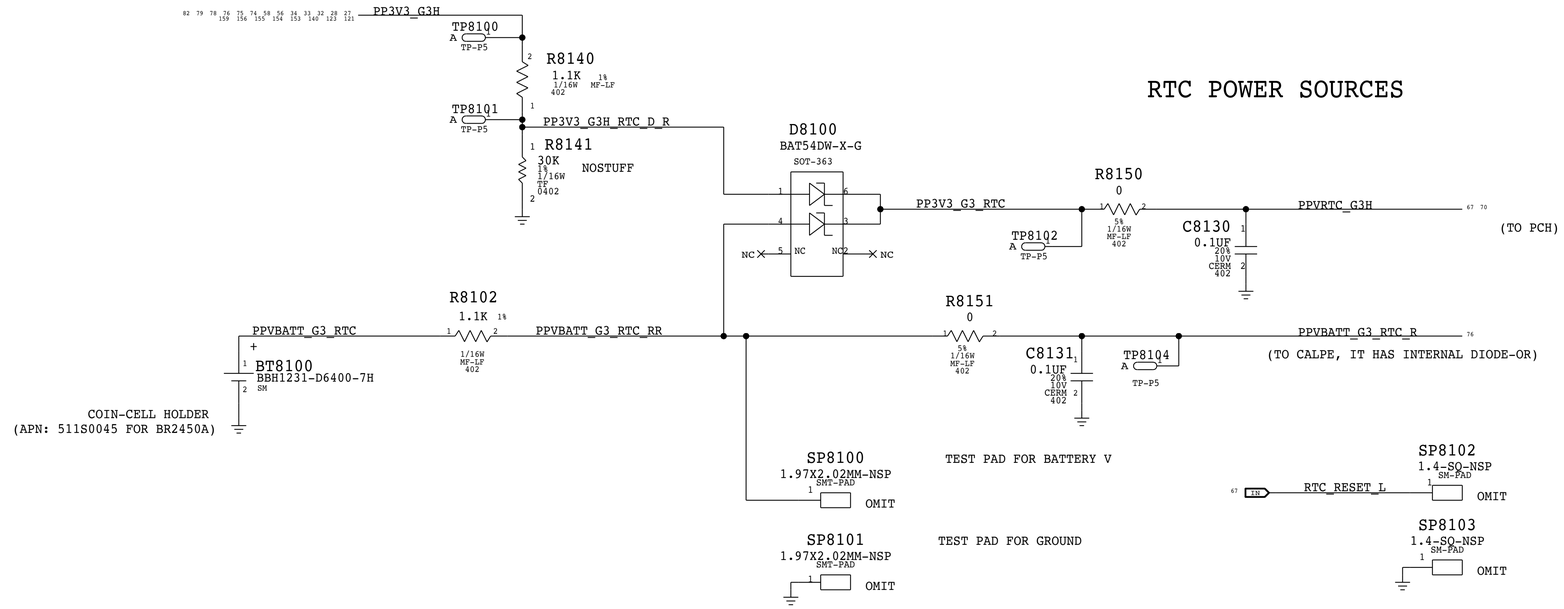
OPTION FOR EXTERNAL PD



CREATE A SINGLE G3S POWER GOOD



RTC POWER SOURCES



BOM_COST_GROUP=SOC

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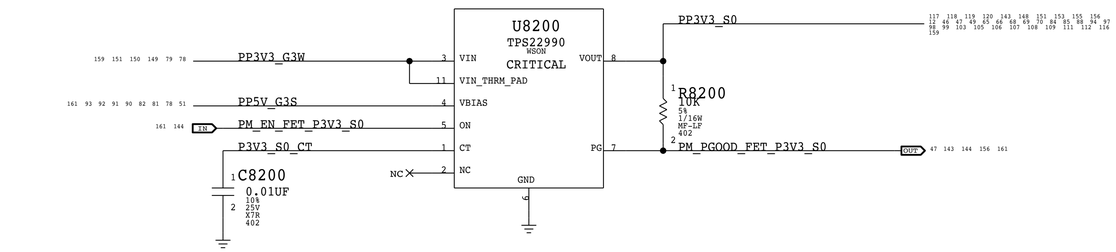
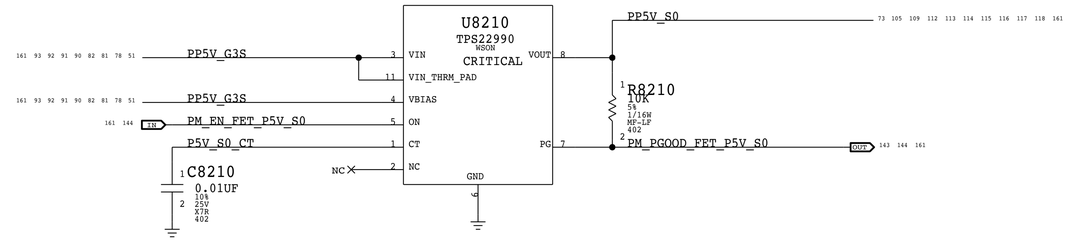
3.3V S0 FET

4.8 A 4 US PEAK
3.5 A AVG



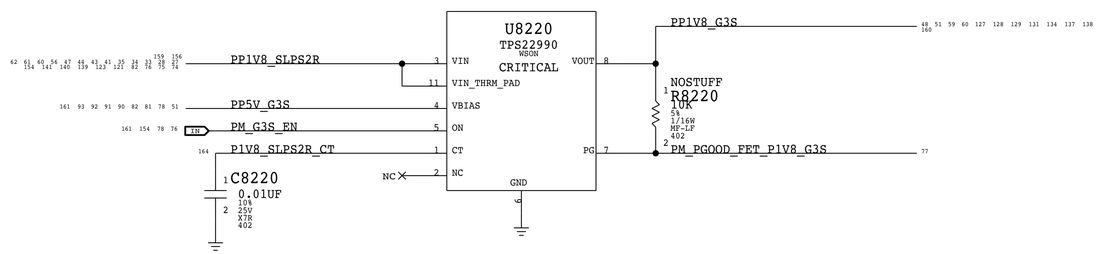
5V S0 FET

2.7 A 4 US PEAK
3.9 A AVG

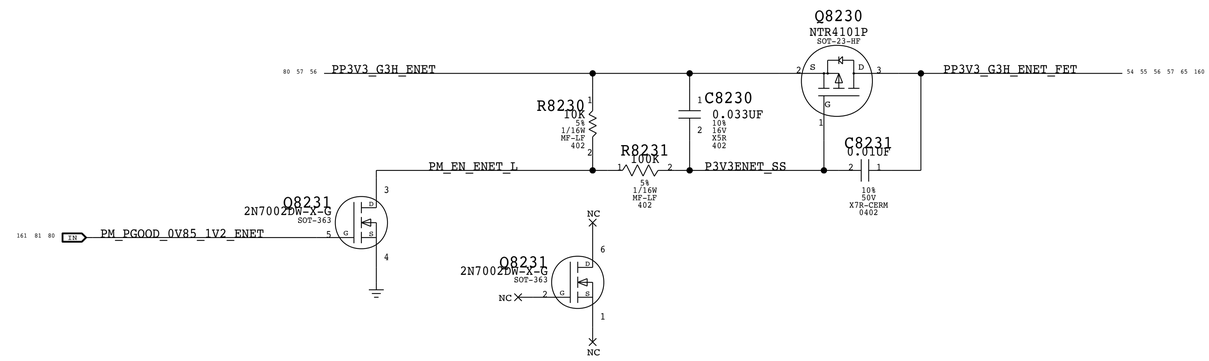


1V8 G3S FET

2.7 A 4 US PEAK
3.9 A AVG

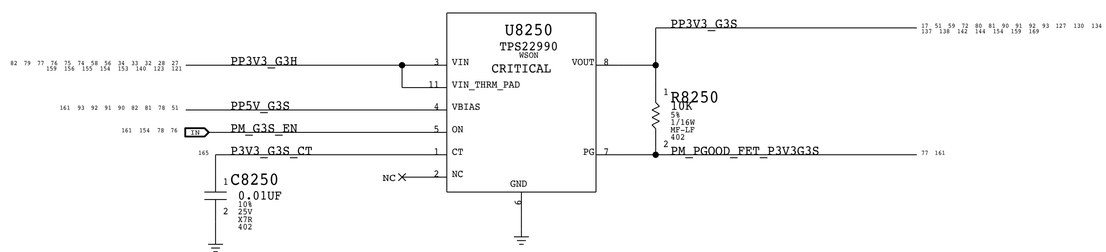


3.3V ENET FET



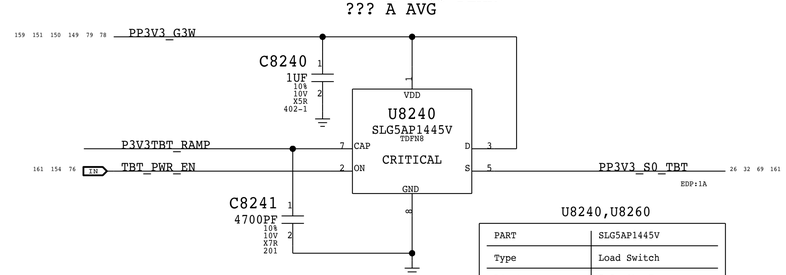
3.3V G3S FET

??? A 4 US PEAK
??? A AVG



TBT S0 FET

??? A 4 US PEAK
??? A AVG

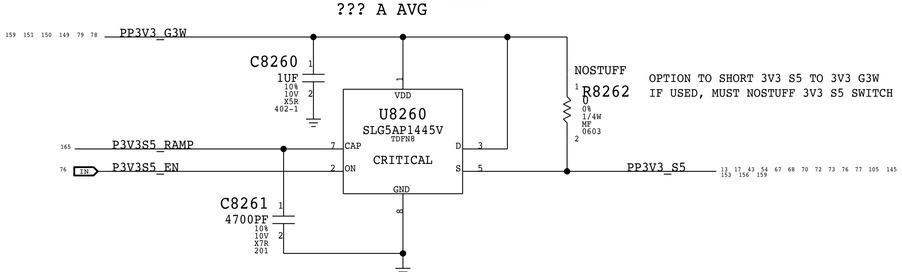


U8240,U8260

PART	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

3V3 S5 FET

??? A 4 US PEAK
??? A AVG



OPTION TO SHORT 3V3 S5 TO 3V3 G3W
IF USED, MUST NOSTUFF 3V3 S5 SWITCH

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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POWER FETS

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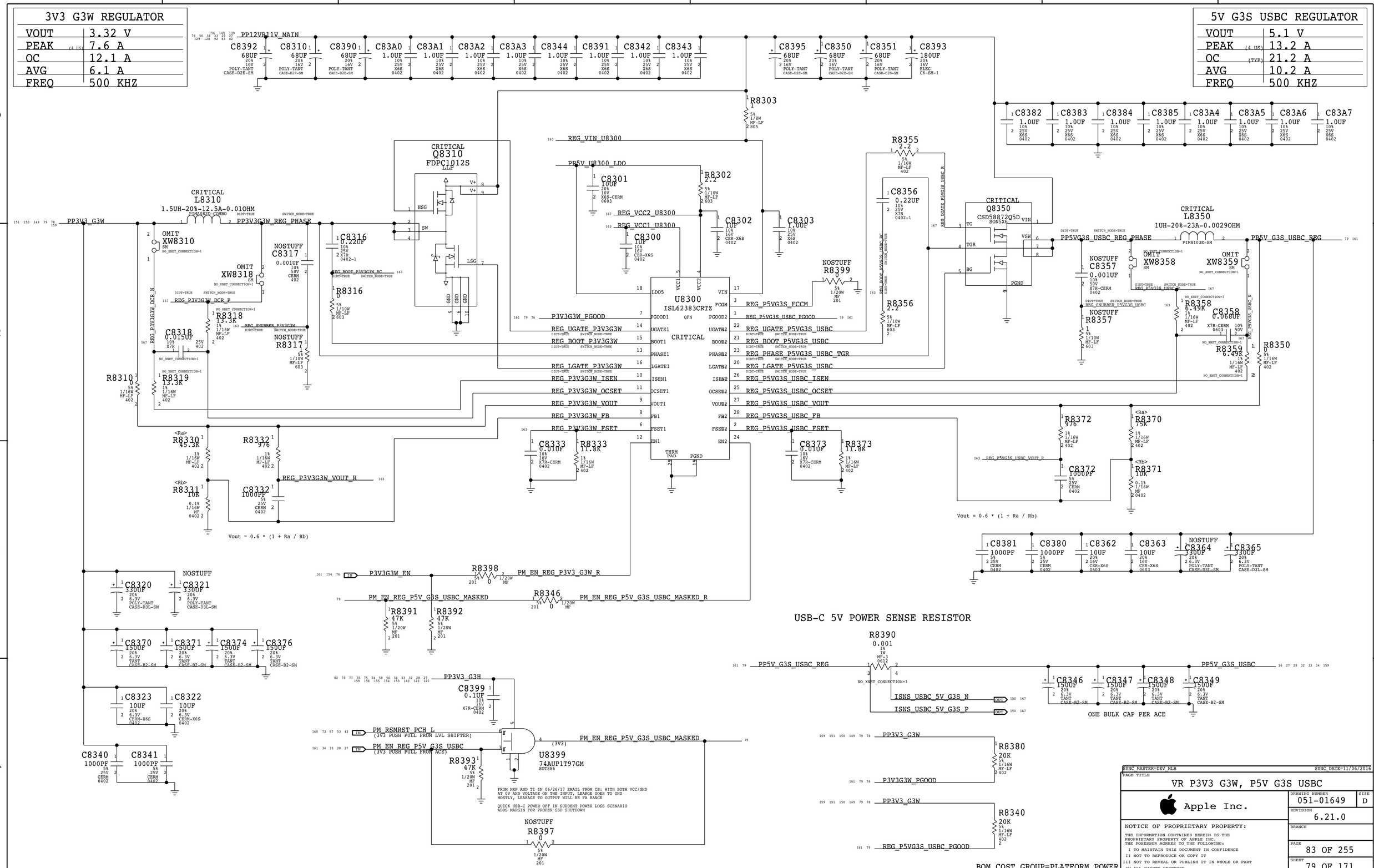
3V3 G3W REGULATOR	
VOUT	3.32 V
PEAK (4 US)	7.6 A
OC	12.1 A
AVG	6.1 A
FREQ	500 KHZ

5V G3S USBC REGULATOR	
VOUT	5.1 V
PEAK (4 US)	13.2 A
OC (TYP)	21.2 A
AVG	10.2 A
FREQ	500 KHZ



SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

VR P3V3 G3W, P5V G3S USBC

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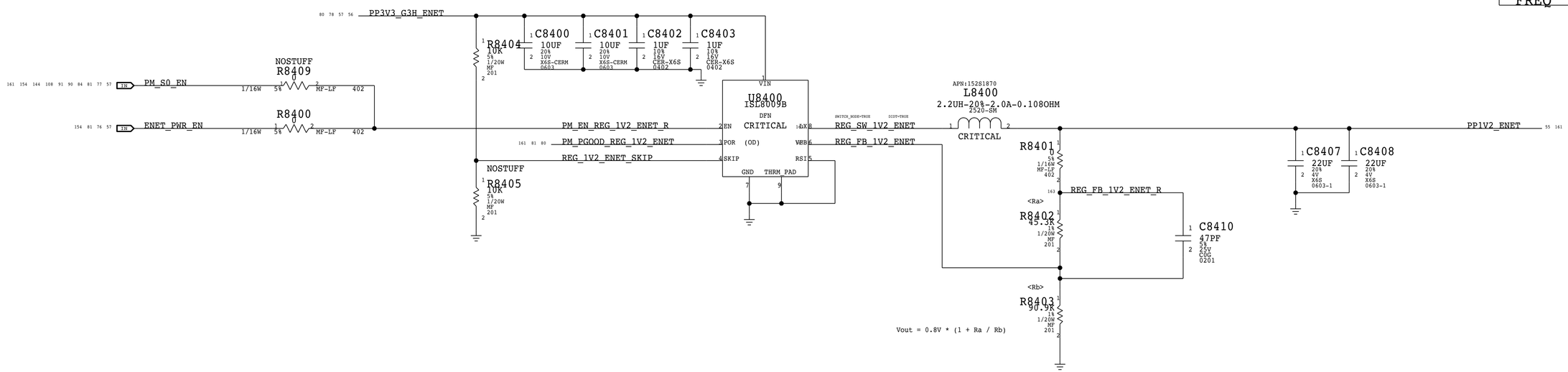
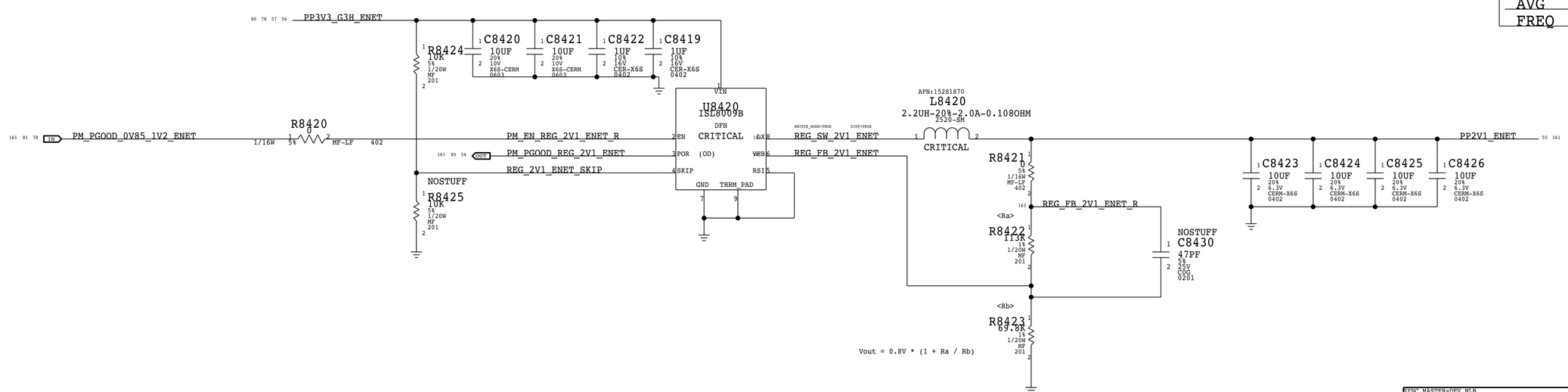
ENET 1V2 REGULATOR	
VOUT	1.20 V
PEAK (4 US)	0.9 A
OC (TYP)	2.2 A
AVG	0.8 A
FREQ	1.6 MHZ

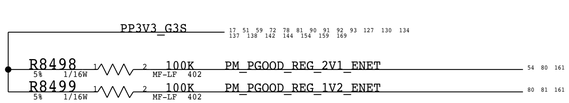
1.2V ENET REGULATOR



ENET 2V1 REGULATOR	
VOUT	2.10 V
PEAK (4 US)	0.5 A
OC (TYP)	2.2 A
AVG	0.5 A
FREQ	1.6 MHZ

2.1V ENET REGULATOR





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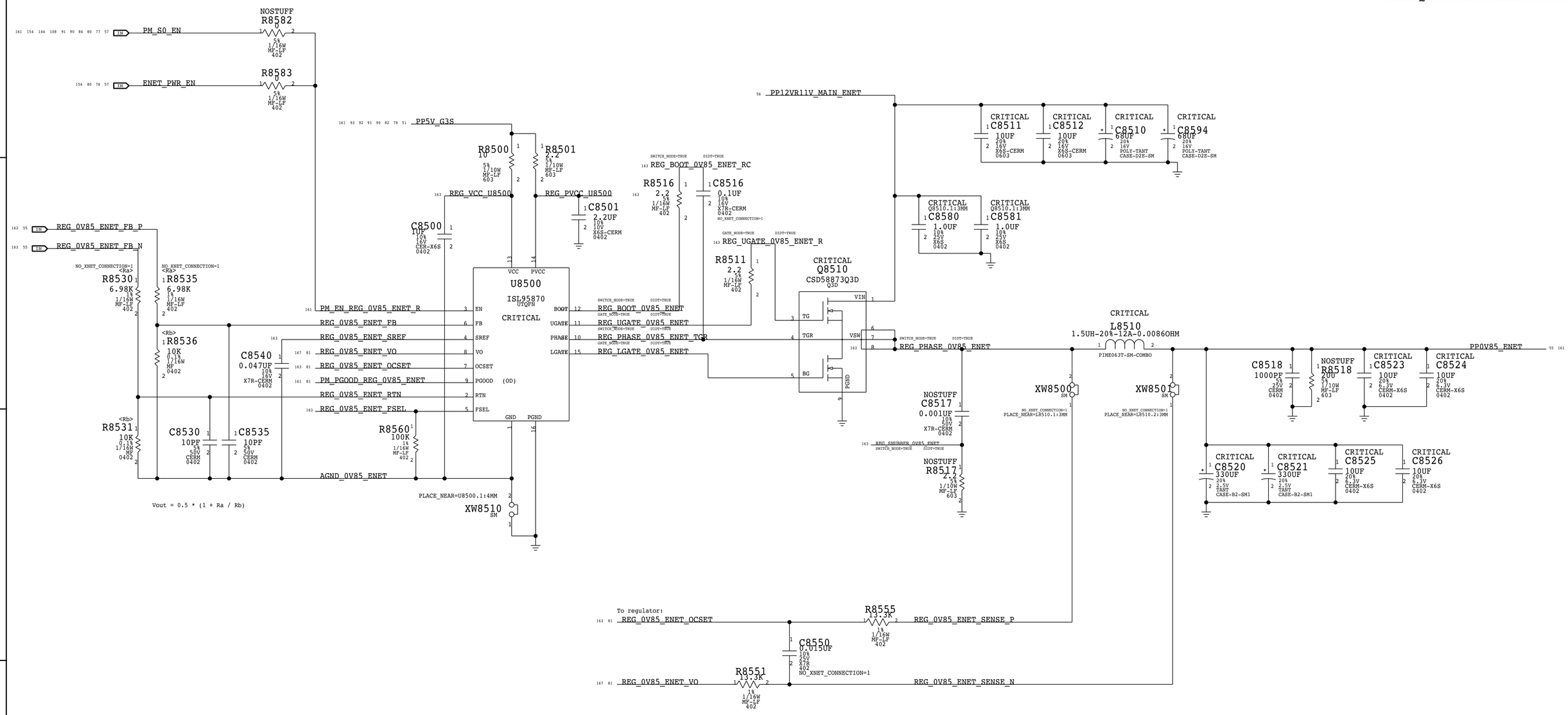
ENET 0V85 REGULATOR	
VOUT	0.85 V
PEAK (4 US)	6.5 A
OC (TYP)	12 A
AVG	6.5 A
FREQ	600 KHZ



FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE: VR ENET 0V85

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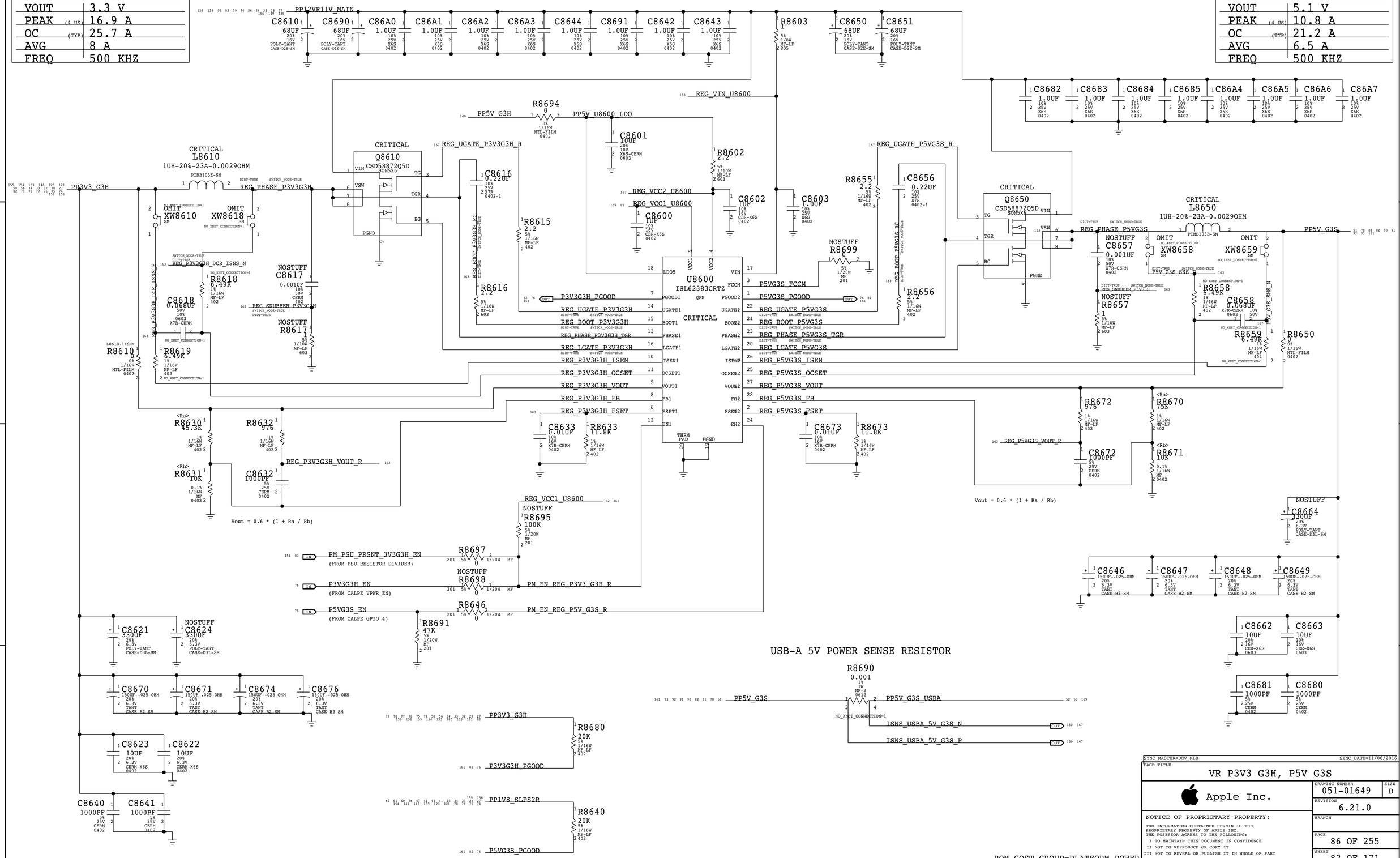
3V3 G3H REGULATOR	
VOUT	3.3 V
PEAK (4 US)	16.9 A
OC (TYP)	25.7 A
AVG	8 A
FREQ	500 KHZ

5V G3S REGULATOR	
VOUT	5.1 V
PEAK (4 US)	10.8 A
OC (TYP)	21.2 A
AVG	6.5 A
FREQ	500 KHZ



SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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VR P3V3 G3H, P5V G3S

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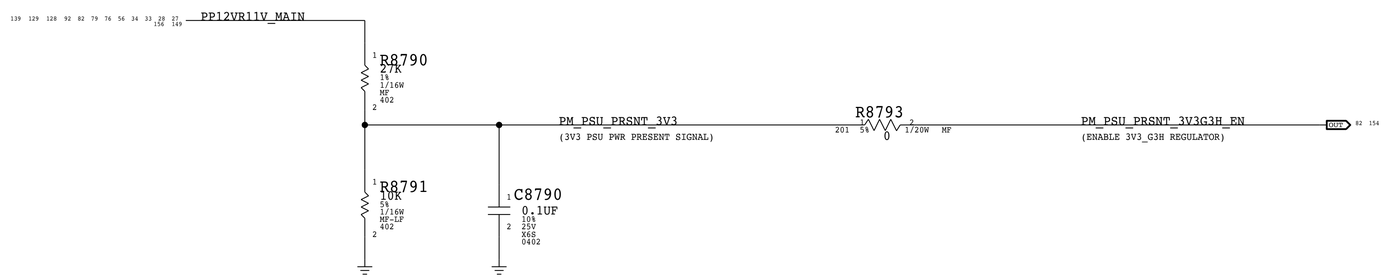

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

PSU PRESENCE G3H ENABLE

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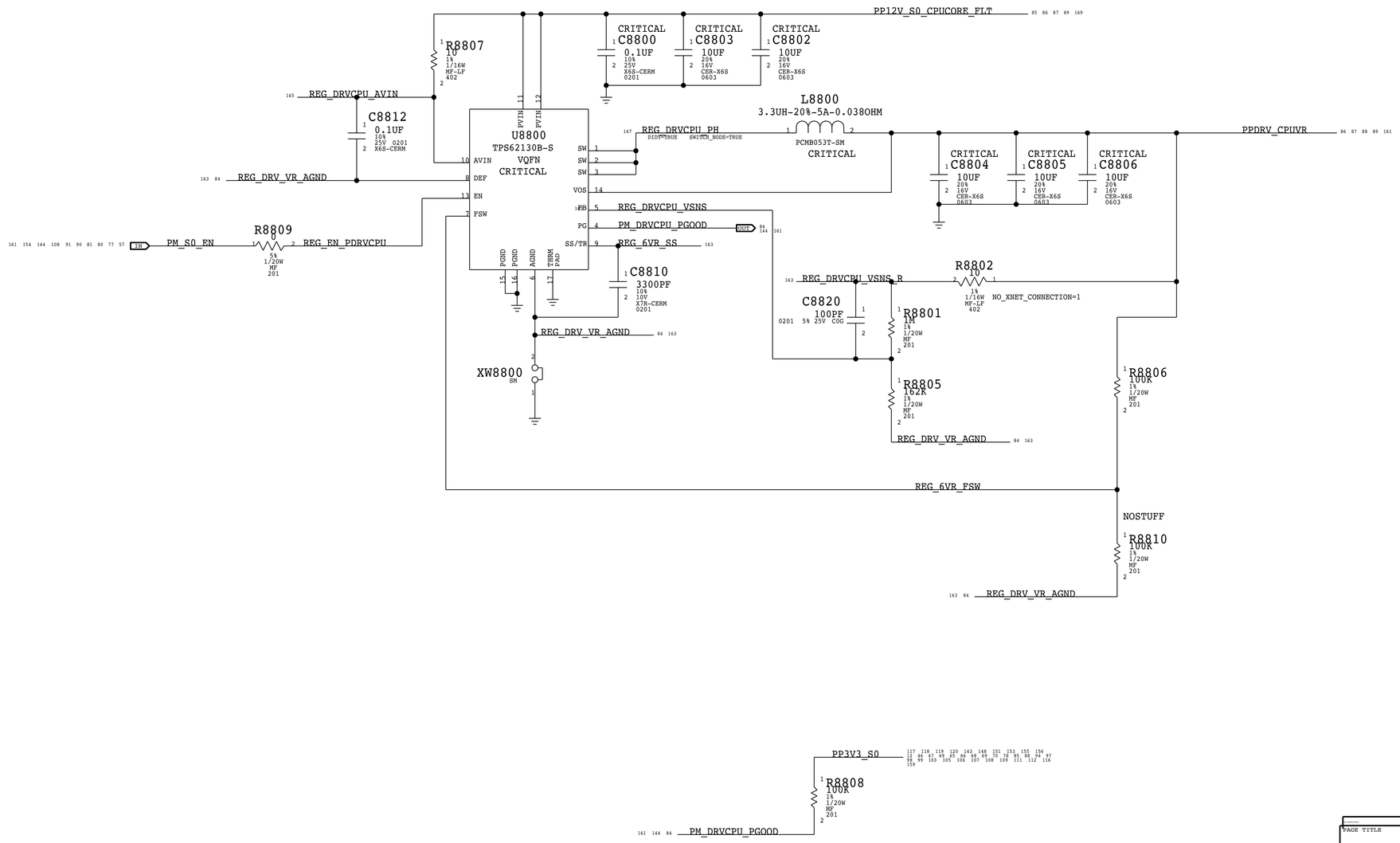
CPU DRV S0 REGULATOR	
VOUT	5.75 V
PEAK	0.5 A
OC (TYP)	4.2 A
AVG	0.5 A
FREQ	1.25 MHZ



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE

VR 5.75V CPUVR

Apple Inc.

DRAWING NUMBER 051-01649 SIZE D

REVISION 6.21.0

BRANCH

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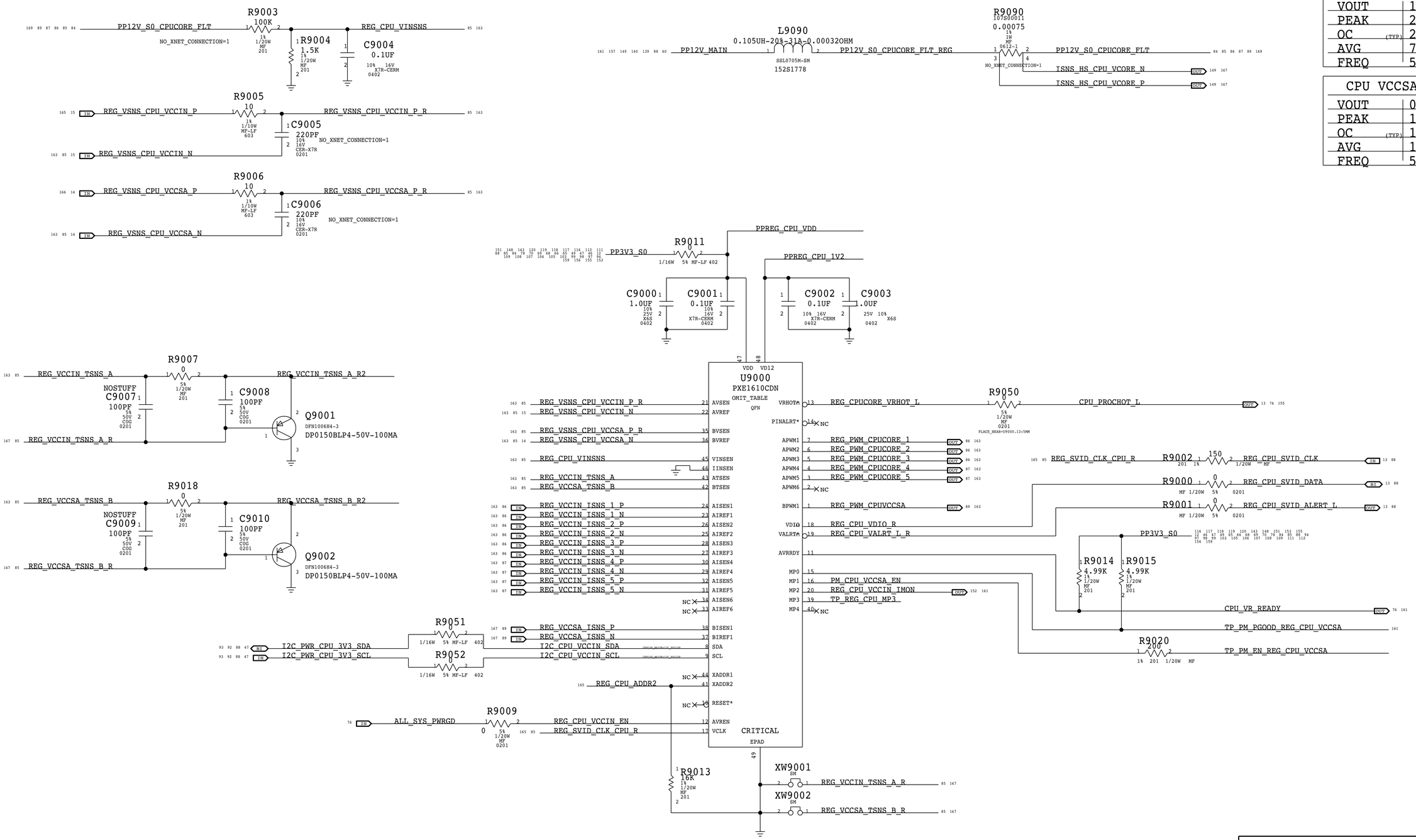
CPU VCCIN REGULATOR	
VOUT	1.8 V
PEAK	200 A
OC (TYP)	240 A
AVG	77 A
FREQ	500 KHZ

CPU VCCSA REGULATOR	
VOUT	0.85 V
PEAK	15 A
OC (TYP)	18 A
AVG	14 A
FREQ	500 KHZ



ACCESS POINT FOR I2C
DEBUG HOOKUP
PLACE GND TP NEARBY

SMBUS ADDR: 0XA0/A1 (I2C) 0X80/81 (PMBUS1) 0X82/83 (PMBUS2)

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: VR CPU CORE & VCCSA CTRL

Apple Inc.

DRAWING NUMBER: 051-01649 SIZE: D
REVISION: 6.21.0
BRANCH
PAGE: 90 OF 255
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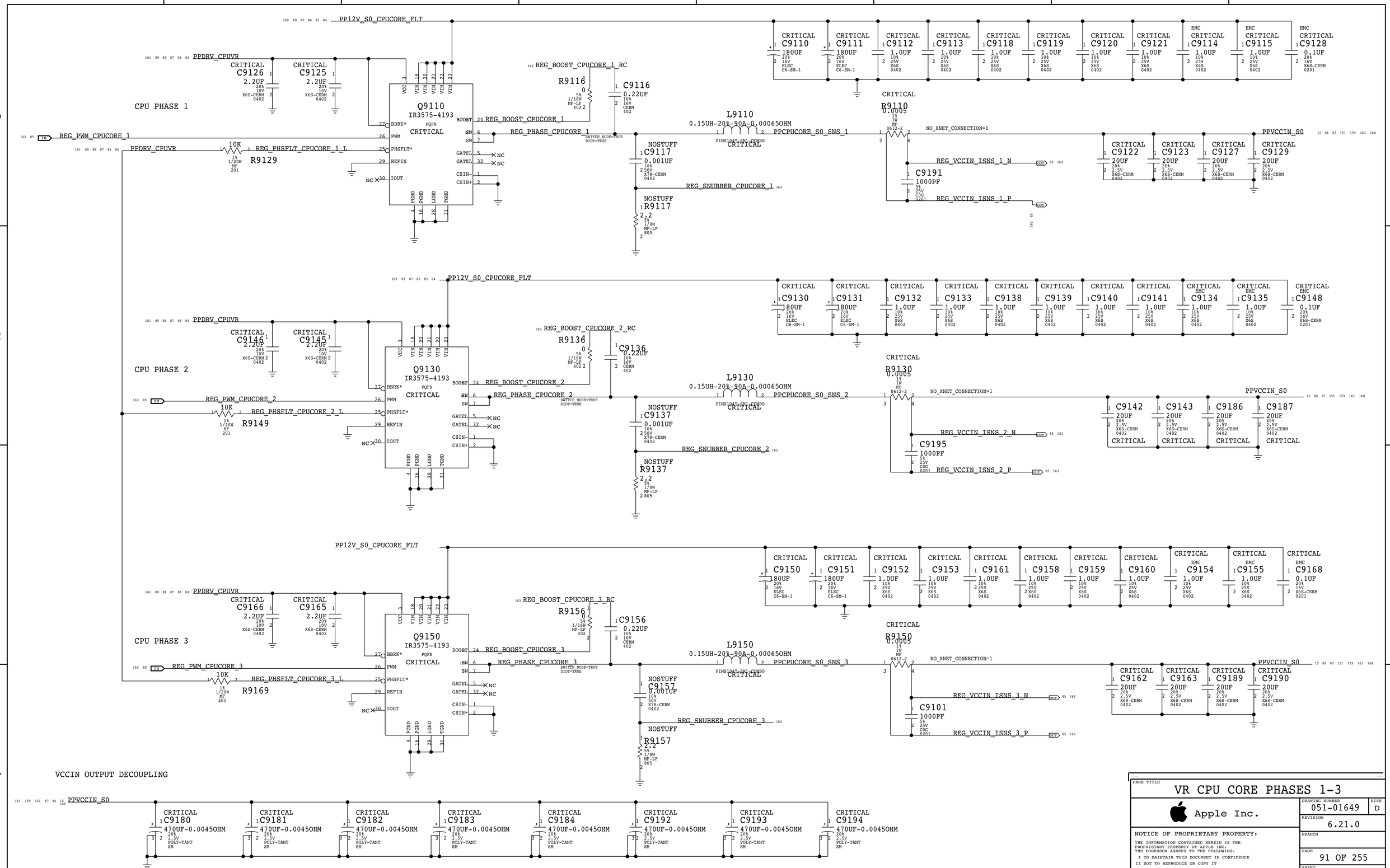

PAGE TITLE

VR CPU CORE PHASES 1-3

Apple Inc.

DRAWING NUMBER 051-01649

SIZE D

REVISION 6.21.0

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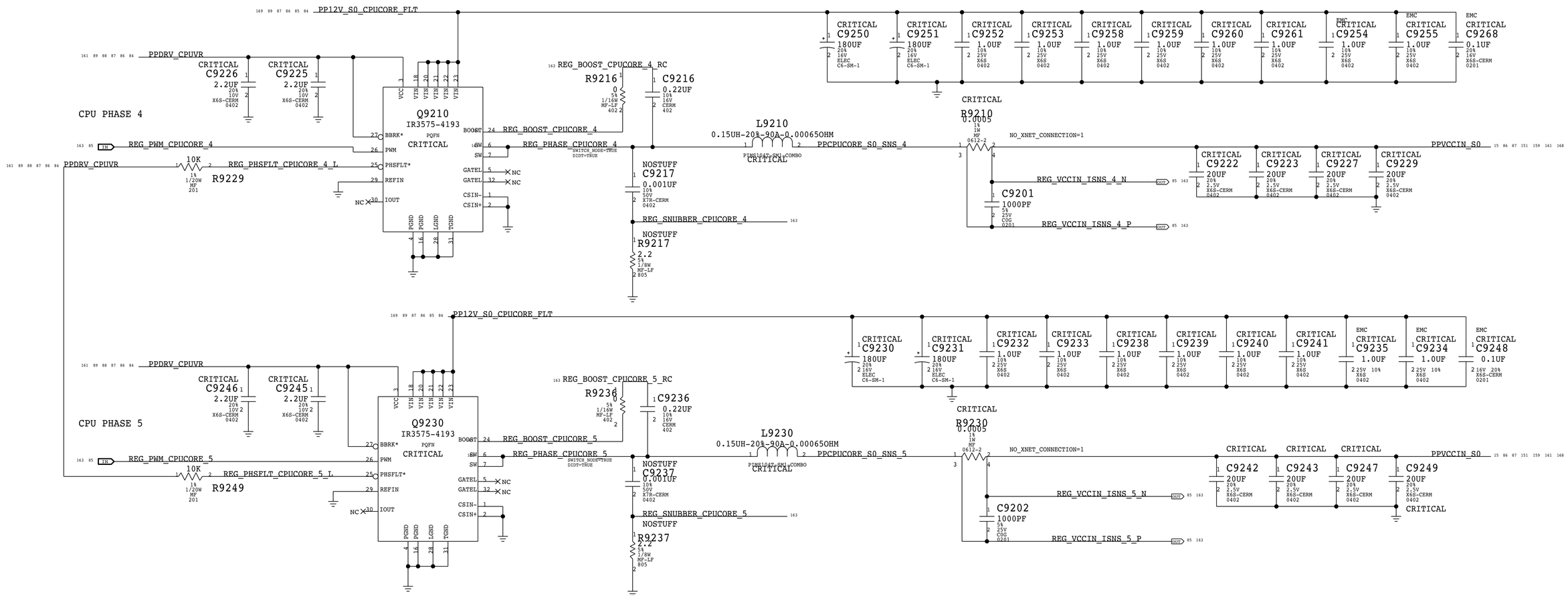

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	VR CPU CORE PHASES 4-5
Apple Inc.	DRAWING NUMBER 051-01649 SIZE D
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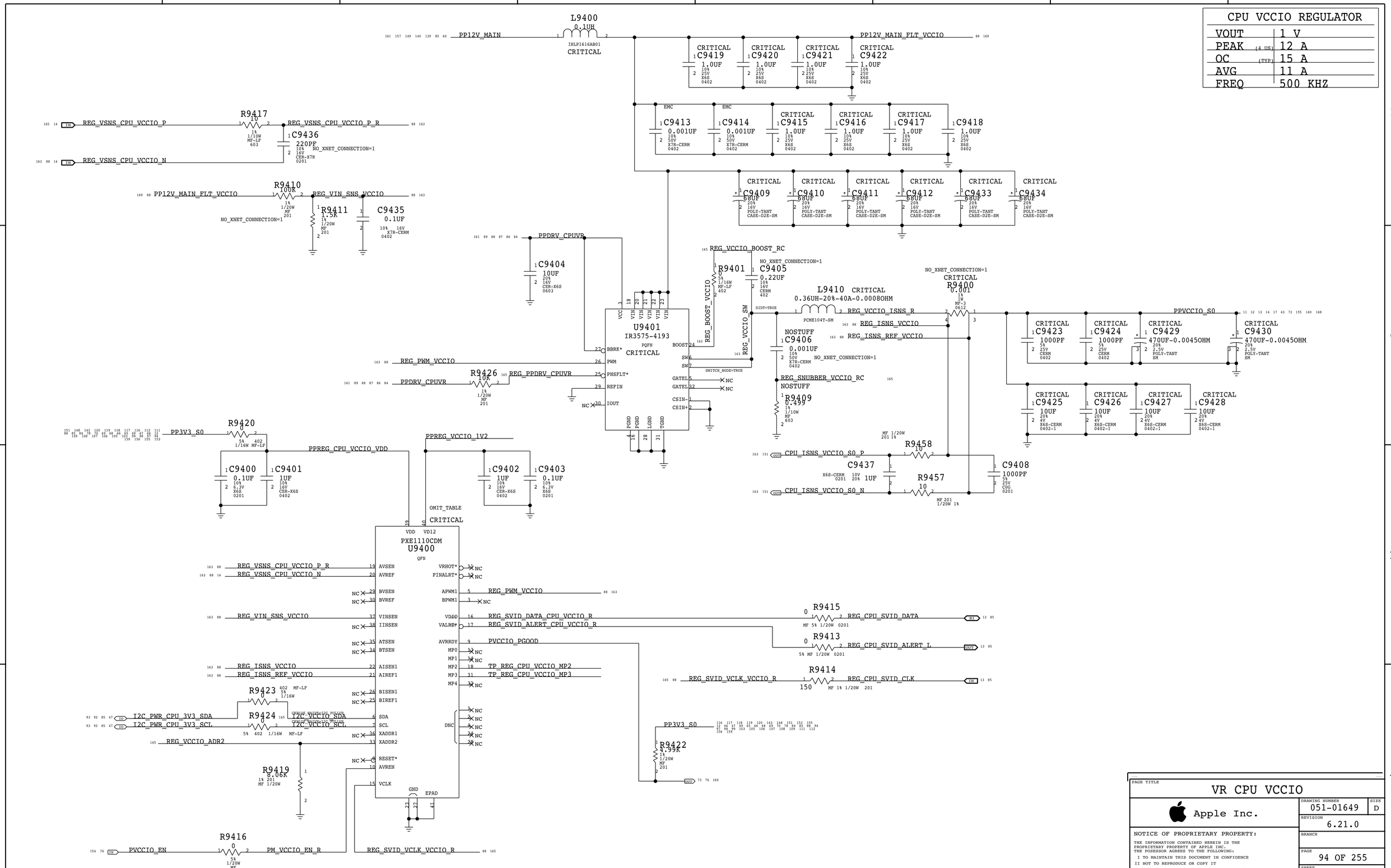
CPU VCCIO REGULATOR
VOUT 1 V
PEAK (4 US) 12 A
OC (TYP) 15 A
AVG 11 A
FREQ 500 KHZ
L9400 0.1UH IHLP1616AB01 CRITICAL
PP12V_MAIN
PP12V_MAIN_FLT_VCCIO
C9419 C9420 C9421 C9422 1.0UF 10% 25V X6S 0402
C9413 0.001UF 10% 50V X7R-CERM 0402
C9414 0.001UF 10% 50V X7R-CERM 0402
C9415 C9416 C9417 C9418 1.0UF 10% 25V X6S 0402
C9409 C9410 C9411 C9412 C9433 C9434 680UF 20% 16V POLY-TANT CASE-D2E-SM
REG_VSNS_CPU_VCCIO_P
REG_VSNS_CPU_VCCIO_N
R9417 10 1% 1/10W MF-LF 603
REG_VSNS_CPU_VCCIO_P_R
C9436 220PF 10% 16V CER-X7R 0201 NO_XNET_CONNECTION=1
R9410 100K 1% 1/20W MF 201
REG_VIN_SNS_VCCIO
R9411 1.5K 1% 1/20W MF 201
C9435 0.1UF 10% 16V X7R-CERM 0402
PPDRV_CPUVR
C9404 10UF 20% 16V CER-X6S 0603
REG_VCCIO_BOOST_RC
R9401 0 5% 1/16W MF-LF 402
C9405 0.22UF 10% 16V CERM 402
REG_BOOST_VCCIO
REG_VCCIO_SW
L9410 CRITICAL 0.36UH-20%-40A-0.0008OHM PCME104T-SM
REG_VCCIO_ISNS_R
REG_ISNS_VCCIO
REG_ISNS_REF_VCCIO
NOSTUFF C9406 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_VCCIO_RC
NOSTUFF R9409 0.499 1% 1/10W MF 603
R9400 0.001 1% 1W MF-3 0612
PPVCCIO_S0
C9423 1000PF 5% 25V CERM 0402
C9424 1000PF 5% 25V CERM 0402
C9429 470UF-0.0045OHM 20% 2.5V POLY-TANT SM
C9430 470UF-0.0045OHM 20% 2.5V POLY-TANT SM
C9425 C9426 C9427 C9428 10UF 20% 4V X6S-CERM 0402-1
U9401 IR3575-4193 PQFN CRITICAL
VCC VIN BBRK* PWM PHSFLT* REFIN IOUT BOOST SW6 SW7 GATEL GATEL CSIN- CSIN+ PGND LGND TGND
REG_PWM_VCCIO
R9426 10K 1% 1/20W MF 201
REG_PPDRV_CPUVR
R9420 0 5% 1/16W MF-LF 402
PP3V3_S0
PPREG_CPU_VCCIO_VDD
PPREG_VCCIO_1V2
C9400 0.1UF 10% 6.3V X6S 0201
C9401 1UF 10% 16V CER-X6S 0402
C9402 1UF 10% 16V CER-X6S 0402
C9403 0.1UF 10% 6.3V X6S 0201
OMIT_TABLE
CRITICAL
PXE1110CDM U9400 QFN
VDD VD12 AVSEN AVREF BVSEN BVREF VINSEN IINSEN ATSEN BTSEN AISEN1 AIREF1 BISEN1 BIREF1 SDA SCL XADDR1 XADDR2 RESET* AVREN VCLK VRHOT* PINALRT* APWM1 BPWM1 VDIO VALRT* AVRRDY MP0 MP1 MP2 MP3 MP4 DNC GND EPAD
REG_VSNS_CPU_VCCIO_P_R
REG_VSNS_CPU_VCCIO_N
REG_PWM_VCCIO
REG_VIN_SNS_VCCIO
REG_SVID_DATA_CPU_VCCIO_R
REG_SVID_ALERT_CPU_VCCIO_R
PVCCIO_PGOOD
REG_ISNS_VCCIO
REG_ISNS_REF_VCCIO
TP_REG_CPU_VCCIO_MP2
TP_REG_CPU_VCCIO_MP3
R9423 0 5% 1/16W 402 MF-LF
R9424 0 5% 1/16W 402 MF-LF
I2C_PWR_CPU_3V3_SDA
I2C_PWR_CPU_3V3_SCL
I2C_VCCIO_SDA
I2C_VCCIO_SCL
REG_VCCIO_ADR2
R9419 8.06K 1% 1/20W MF 201
R9415 0 5% MF 1/20W 0201
REG_CPU_SVID_DATA
R9413 0 5% MF 1/20W 0201
REG_CPU_SVID_ALERT_L
R9414 150 1% MF 1/20W 201
REG_SVID_VCLK_VCCIO_R
REG_CPU_SVID_CLK
R9422 4.99K 1% 1/20W MF 201
R9458 10 MF 1/20W 201 1%
R9457 10 MF 201 1/20W 1%
CPU_ISNS_VCCIO_S0_P
CPU_ISNS_VCCIO_S0_N
C9437 1UF 10V 20% X6S-CERM 0201
C9408 1000PF 5% 25V C0G 0201
R9416 0 5% 1/20W MF 0201
PVCCIO_EN
PM_VCCIO_EN_R
REG_SVID_VCLK_VCCIO_R
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE
VR CPU VCCIO
Apple Inc.
DRAWING NUMBER 051-01649
SIZE D
REVISION 6.21.0
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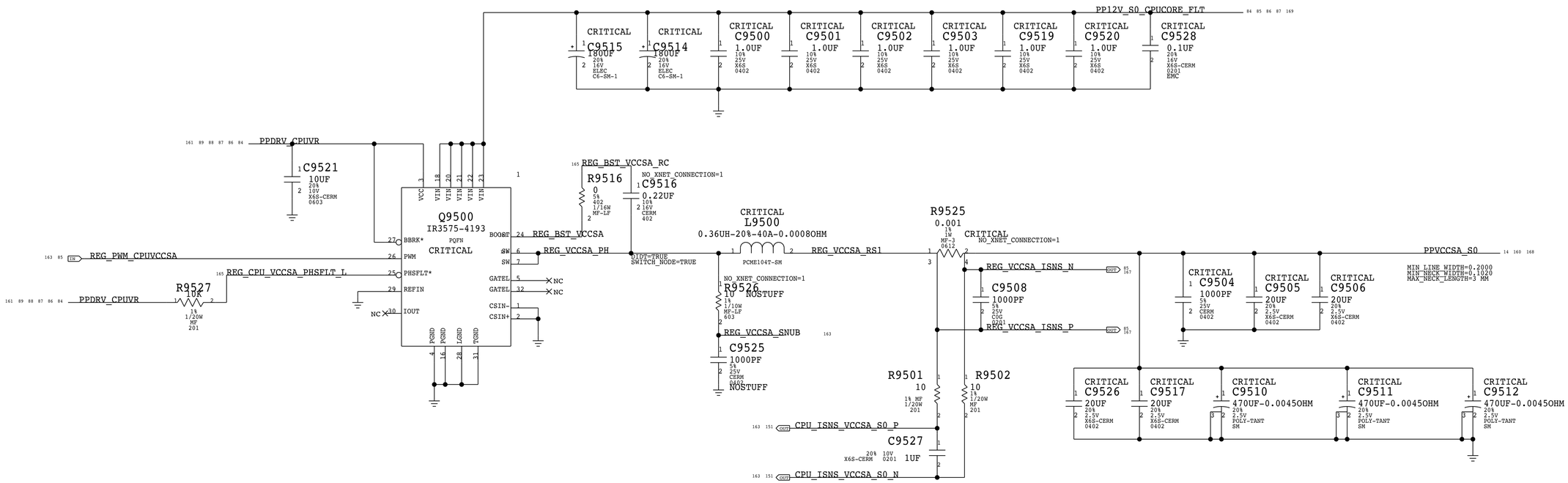

CPU VCCSA REGULATOR
SHARES CONTROLLER ON CSA90

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	VR CPU VCCSA
Apple Inc.	DRAWING NUMBER 051-01649 SIZE D
	REVISION 6.21.0
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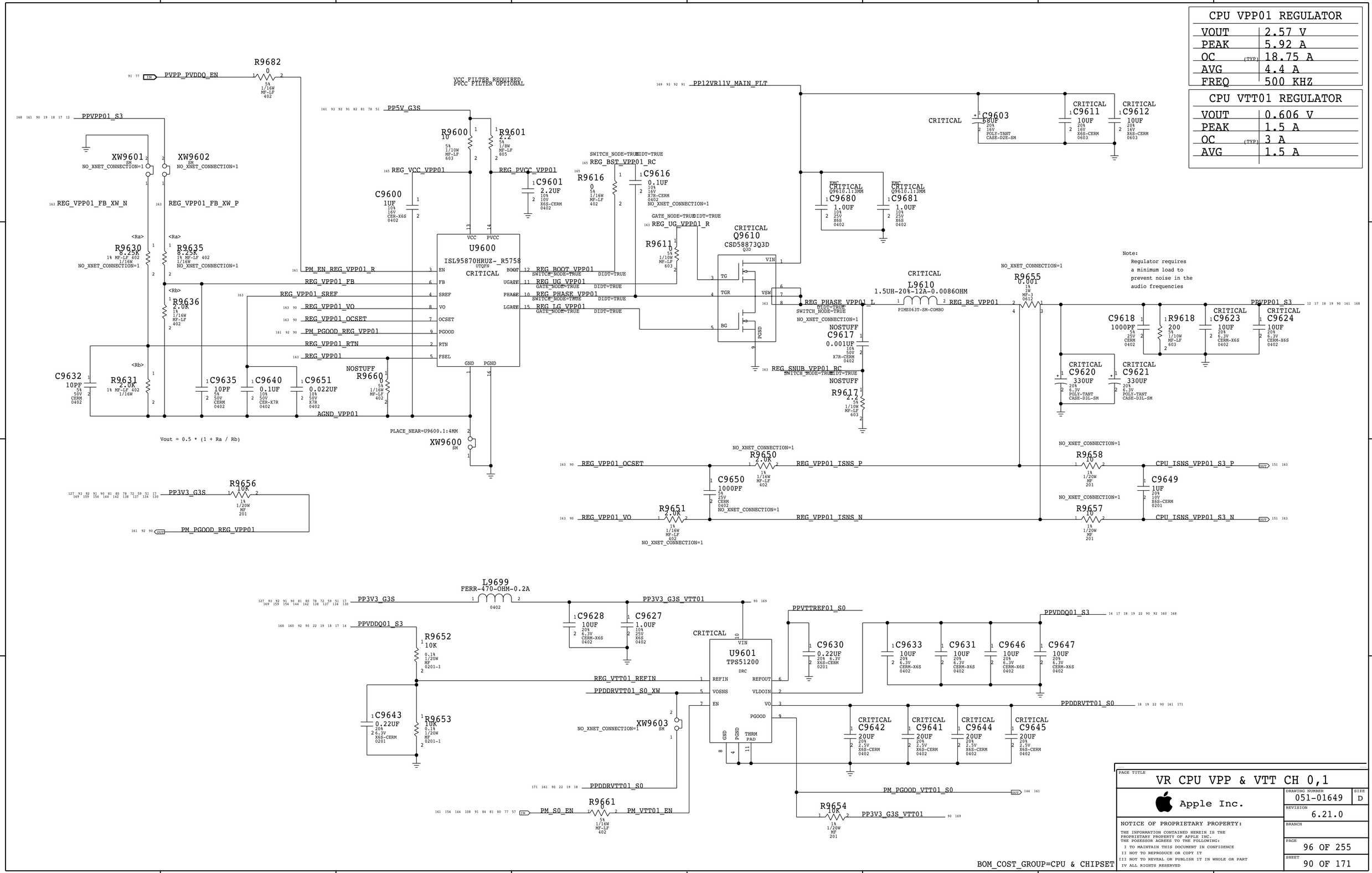
CPU VPP01 REGULATOR	
VOUT	2.57 V
PEAK	5.92 A
OC (TYP)	18.75 A
AVG	4.4 A
FREQ	500 KHZ

CPU VTT01 REGULATOR	
VOUT	0.606 V
PEAK	1.5 A
OC (TYP)	3 A
AVG	1.5 A



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	VR CPU VPP & VTT CH 0,1
	Apple Inc.
DRAWING NUMBER	051-01649
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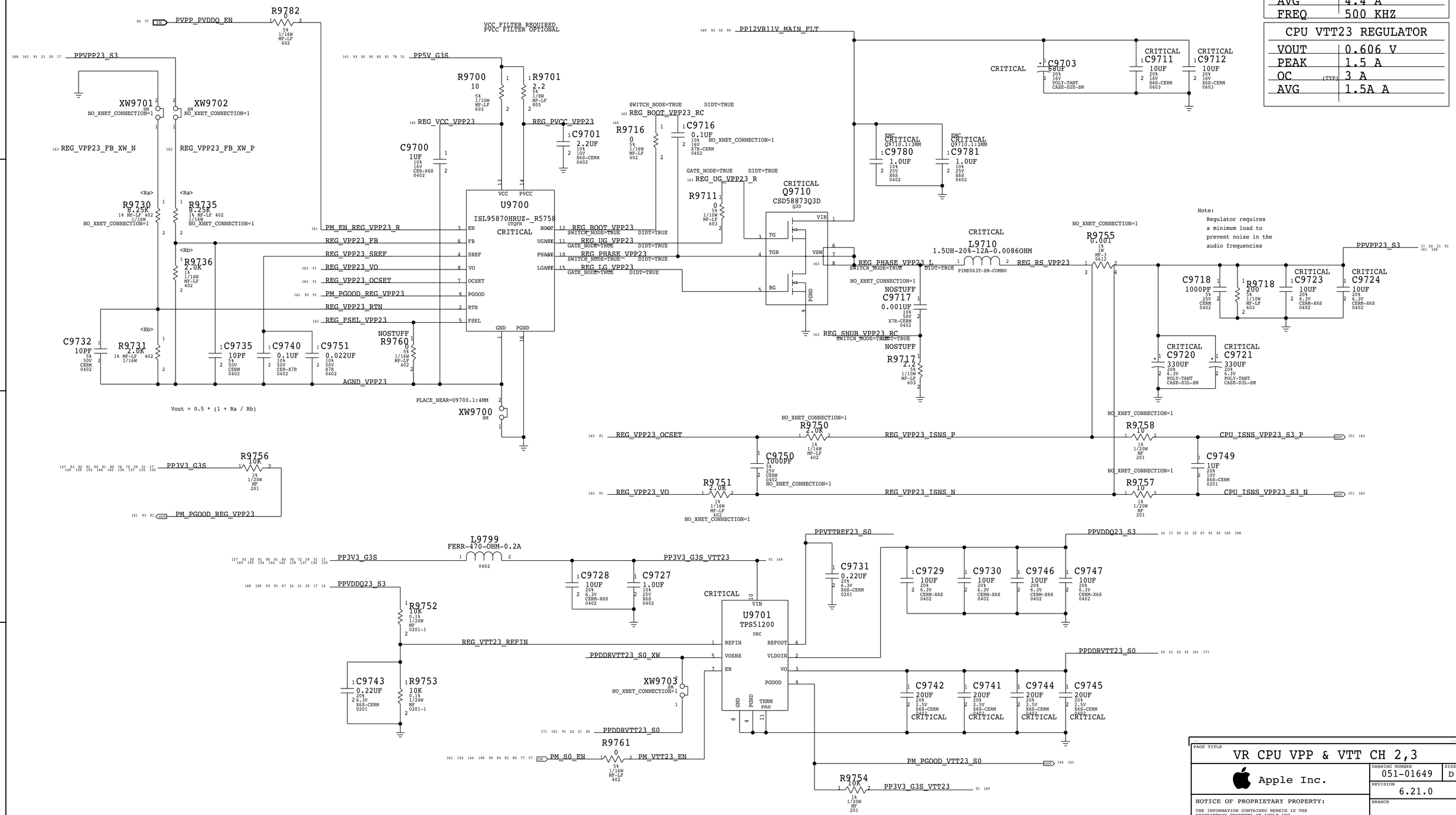
CPU VPP23 REGULATOR	
VOUT	2.57 V
PEAK	5.92 A
OC (TYP)	18.75 A
AVG	4.4 A
FREQ	500 KHZ

CPU VTT23 REGULATOR	
VOUT	0.606 V
PEAK	1.5 A
OC (TYP)	3 A
AVG	1.5A A



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	VR CPU VPP & VTT CH 2,3
	Apple Inc.
DRAWING NUMBER	051-01649
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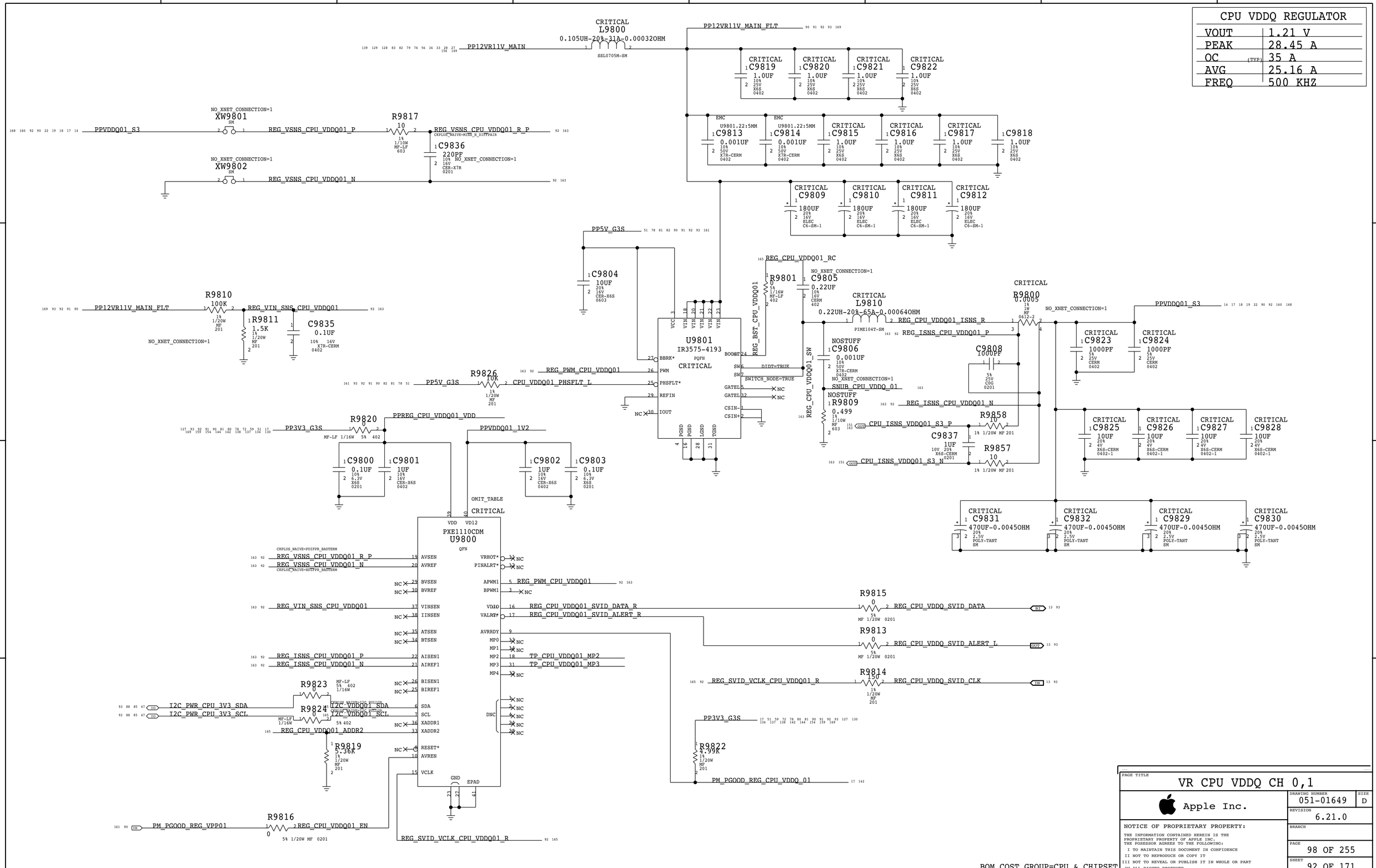
CPU VDDQ REGULATOR
VOUT 1.21 V
PEAK 28.45 A
OC (TYP) 35 A
AVG 25.16 A
FREQ 500 KHZ
CRITICAL L9800 0.105UH-20%-31A-0.00032OHM
PP12VR11V_MAIN
PP12VR11V_MAIN_FLT
CRITICAL C9819 1.0UF
CRITICAL C9820 1.0UF
CRITICAL C9821 1.0UF
CRITICAL C9822 1.0UF
EMC C9813 0.001UF
EMC C9814 0.001UF
CRITICAL C9815 1.0UF
CRITICAL C9816 1.0UF
CRITICAL C9817 1.0UF
C9818 1.0UF
CRITICAL C9809 180UF
CRITICAL C9810 180UF
CRITICAL C9811 180UF
CRITICAL C9812 180UF
NO_XNET_CONNECTION=1 XW9801
NO_XNET_CONNECTION=1 XW9802
PPVDDQ01_S3
REG_VSNS_CPU_VDDQ01_P
REG_VSNS_CPU_VDDQ01_N
R9817 10
REG_VSNS_CPU_VDDQ01_R_P
C9836 220PF
PP5V_G3S
C9804 10UF
REG_CPU_VDDQ01_RC
R9801 0
NO_XNET_CONNECTION=1 C9805 0.22UF
CRITICAL L9810 0.22UH-20%-65A-0.000640HM
REG_CPU_VDDQ01_ISNS_R
REG_ISNS_CPU_VDDQ01_P
CRITICAL R9800 0.0005
PPVDDQ01_S3
CRITICAL C9823 1000PF
CRITICAL C9824 1000PF
R9810 100K
PP12VR11V_MAIN_FLT
REG_VIN_SNS_CPU_VDDQ01
R9811 1.5K
C9835 0.1UF
NO_XNET_CONNECTION=1
U9801 IR3575-4193 PQFN CRITICAL
REG_BST_CPU_VDDQ01
REG_CPU_VDDQ01_SW
NOSTUFF C9806 0.001UF
C9808 1000PF
REG_PWM_CPU_VDDQ01
R9826 10K
PP5V_G3S
CPU_VDDQ01_PHSFLT_L
DIDT=TRUE
SWITCH_NODE=TRUE
SNUB_CPU_VDDQ_01
NOSTUFF R9809 0.499
REG_ISNS_CPU_VDDQ01_N
CPU_ISNS_VDDQ01_S3_P
CPU_ISNS_VDDQ01_S3_N
R9858 10
C9837 1UF
R9857 10
CRITICAL C9825 10UF
CRITICAL C9826 10UF
CRITICAL C9827 10UF
CRITICAL C9828 10UF
PP3V3_G3S
R9820 0
PPREG_CPU_VDDQ01_VDD
PPVDDQ01_1V2
C9800 0.1UF
C9801 1UF
C9802 1UF
C9803 0.1UF
OMIT_TABLE
CRITICAL
PXE1110CDM U9800 QFN
REG_VSNS_CPU_VDDQ01_R_P
REG_VSNS_CPU_VDDQ01_N
REG_PWM_CPU_VDDQ01
REG_VIN_SNS_CPU_VDDQ01
REG_CPU_VDDQ01_SVID_DATA_R
REG_CPU_VDDQ01_SVID_ALERT_R
TP_CPU_VDDQ01_MP2
TP_CPU_VDDQ01_MP3
REG_ISNS_CPU_VDDQ01_P
REG_ISNS_CPU_VDDQ01_N
CRITICAL C9831 470UF-0.0045OHM
CRITICAL C9832 470UF-0.0045OHM
CRITICAL C9829 470UF-0.0045OHM
CRITICAL C9830 470UF-0.0045OHM
R9815 0 REG_CPU_VDDQ_SVID_DATA
R9813 0 REG_CPU_VDDQ_SVID_ALERT_L
R9814 150 REG_CPU_VDDQ_SVID_CLK
REG_SVID_VCLK_CPU_VDDQ01_R
R9823 0
R9824 0
I2C_PWR_CPU_3V3_SDA
I2C_PWR_CPU_3V3_SCL
I2C_VDDQ01_SDA
I2C_VDDQ01_SCL
REG_CPU_VDDQ01_ADDR2
R9819 5.36K
PP3V3_G3S
R9822 4.99K
PM_PGOOD_REG_CPU_VDDQ_01
R9816 0
PM_PGOOD_REG_VPP01
REG_CPU_VDDQ01_EN
REG_SVID_VCLK_CPU_VDDQ01_R
BOM_COST_GROUP=CPU & CHIPSET
PAGE TITLE VR CPU VDDQ CH 0,1
Apple Inc.
DRAWING NUMBER 051-01649
SIZE D
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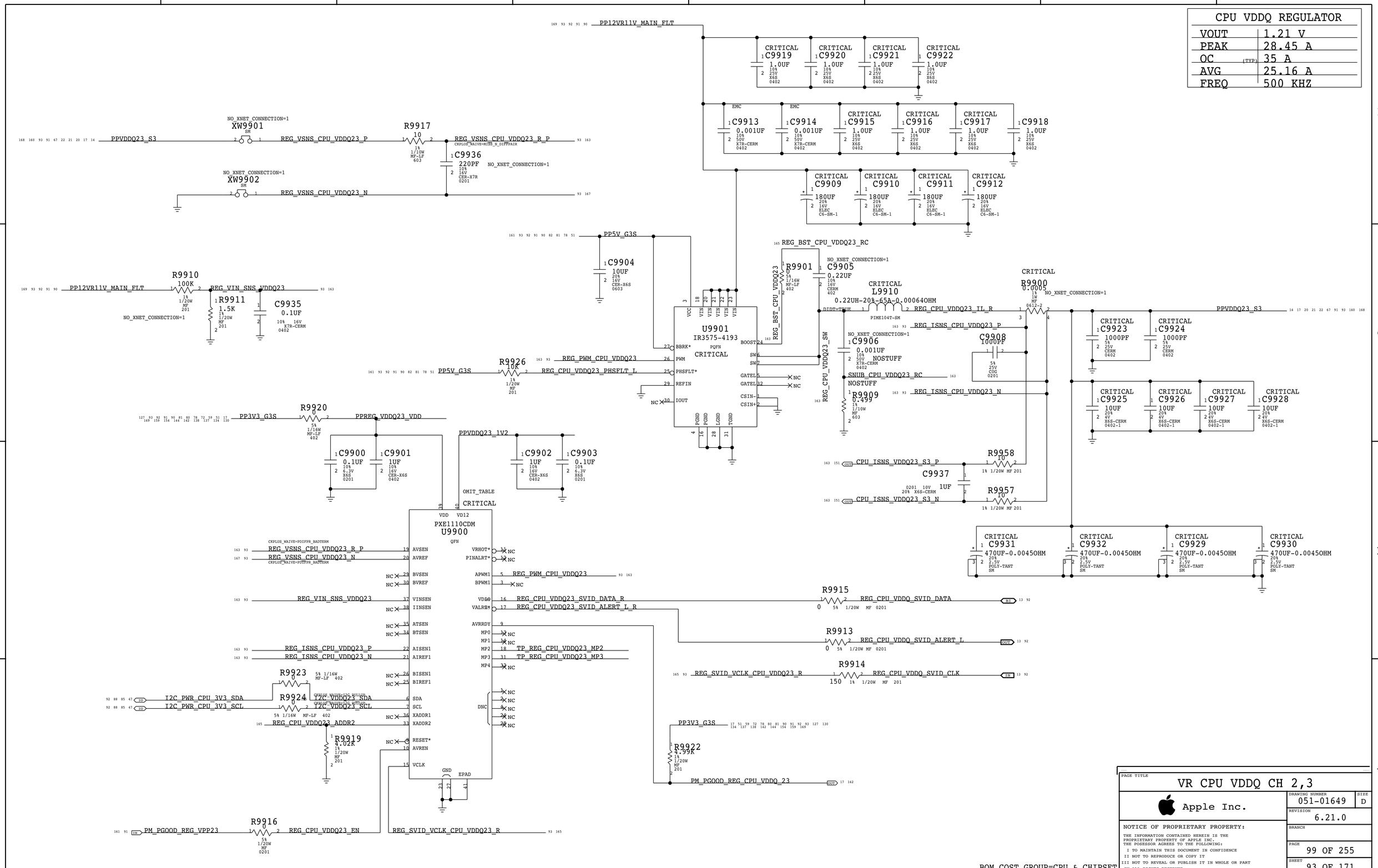
CPU VDDQ REGULATOR	
VOUT	1.21 V
PEAK	28.45 A
OC (TYP)	35 A
AVG	25.16 A
FREQ	500 KHZ



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	VR CPU VDDQ CH 2,3
Apple Inc.	DRAWING NUMBER 051-01649 SIZE D
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PCIE / REF CLOCK

OMIT_TABLE

UA000
VEGA10-T7
TBD
BGA
SYM 1 OF 16
PCIEXPRESS
CRITICAL

PE_CPU_TO_GFX_C_P<0>	BC5 PCIE_RX0P	PCIE_TX0P BB6	PE_GFX_TO_CPU_P<0>	OUT	95 162
PE_CPU_TO_GFX_C_N<0>	BC6 PCIE_RX0N	PCIE_TX0N BB7	PE_GFX_TO_CPU_N<0>	OUT	95 162
PE_CPU_TO_GFX_C_P<1>	BE6 PCIE_RX1P	PCIE_TX1P BA7	PE_GFX_TO_CPU_P<1>	OUT	95 162
PE_CPU_TO_GFX_C_N<1>	BE7 PCIE_RX1N	PCIE_TX1N BA8	PE_GFX_TO_CPU_N<1>	OUT	95 162
PE_CPU_TO_GFX_C_P<2>	BD7 PCIE_RX2P	PCIE_TX2P AY8	PE_GFX_TO_CPU_P<2>	OUT	95 162
PE_CPU_TO_GFX_C_N<2>	BD8 PCIE_RX2N	PCIE_TX2N AY9	PE_GFX_TO_CPU_N<2>	OUT	95 162
PE_CPU_TO_GFX_C_P<3>	BC8 PCIE_RX3P	PCIE_TX3P BB9	PE_GFX_TO_CPU_P<3>	OUT	95 162
PE_CPU_TO_GFX_C_N<3>	BC9 PCIE_RX3N	PCIE_TX3N BB10	PE_GFX_TO_CPU_N<3>	OUT	95 162
PE_CPU_TO_GFX_C_P<4>	BE9 PCIE_RX4P	PCIE_TX4P BA10	PE_GFX_TO_CPU_P<4>	OUT	95 162
PE_CPU_TO_GFX_C_N<4>	BE10 PCIE_RX4N	PCIE_TX4N BA11	PE_GFX_TO_CPU_N<4>	OUT	95 162
PE_CPU_TO_GFX_C_P<5>	BD10 PCIE_RX5P	PCIE_TX5P AY11	PE_GFX_TO_CPU_P<5>	OUT	95 162
PE_CPU_TO_GFX_C_N<5>	BD11 PCIE_RX5N	PCIE_TX5N AY12	PE_GFX_TO_CPU_N<5>	OUT	95 162
PE_CPU_TO_GFX_C_P<6>	BC11 PCIE_RX6P	PCIE_TX6P BB12	PE_GFX_TO_CPU_P<6>	OUT	95 162
PE_CPU_TO_GFX_C_N<6>	BC12 PCIE_RX6N	PCIE_TX6N BB13	PE_GFX_TO_CPU_N<6>	OUT	95 162
PE_CPU_TO_GFX_C_P<7>	BE12 PCIE_RX7P	PCIE_TX7P BA13	PE_GFX_TO_CPU_P<7>	OUT	95 162
PE_CPU_TO_GFX_C_N<7>	BE13 PCIE_RX7N	PCIE_TX7N BA14	PE_GFX_TO_CPU_N<7>	OUT	95 162
PE_CPU_TO_GFX_C_P<8>	BD13 PCIE_RX8P	PCIE_TX8P AY14	PE_GFX_TO_CPU_P<8>	OUT	95 162
PE_CPU_TO_GFX_C_N<8>	BD14 PCIE_RX8N	PCIE_TX8N AY15	PE_GFX_TO_CPU_N<8>	OUT	95 162
PE_CPU_TO_GFX_C_P<9>	BC14 PCIE_RX9P	PCIE_TX9P BB15	PE_GFX_TO_CPU_P<9>	OUT	95 162
PE_CPU_TO_GFX_C_N<9>	BC15 PCIE_RX9N	PCIE_TX9N BB16	PE_GFX_TO_CPU_N<9>	OUT	95 162
PE_CPU_TO_GFX_C_P<10>	BE15 PCIE_RX10P	PCIE_TX10P BA16	PE_GFX_TO_CPU_P<10>	OUT	95 162
PE_CPU_TO_GFX_C_N<10>	BE16 PCIE_RX10N	PCIE_TX10N BA17	PE_GFX_TO_CPU_N<10>	OUT	95 162
PE_CPU_TO_GFX_C_P<11>	BD16 PCIE_RX11P	PCIE_TX11P AY17	PE_GFX_TO_CPU_P<11>	OUT	95 162
PE_CPU_TO_GFX_C_N<11>	BD17 PCIE_RX11N	PCIE_TX11N AY18	PE_GFX_TO_CPU_N<11>	OUT	95 162
PE_CPU_TO_GFX_C_P<12>	BC17 PCIE_RX12P	PCIE_TX12P BB18	PE_GFX_TO_CPU_P<12>	OUT	95 162
PE_CPU_TO_GFX_C_N<12>	BC18 PCIE_RX12N	PCIE_TX12N BB19	PE_GFX_TO_CPU_N<12>	OUT	95 162
PE_CPU_TO_GFX_C_P<13>	BE18 PCIE_RX13P	PCIE_TX13P BA19	PE_GFX_TO_CPU_P<13>	OUT	95 162
PE_CPU_TO_GFX_C_N<13>	BE19 PCIE_RX13N	PCIE_TX13N BA20	PE_GFX_TO_CPU_N<13>	OUT	95 162
PE_CPU_TO_GFX_C_P<14>	BD19 PCIE_RX14P	PCIE_TX14P AY20	PE_GFX_TO_CPU_P<14>	OUT	95 162
PE_CPU_TO_GFX_C_N<14>	BD20 PCIE_RX14N	PCIE_TX14N AY21	PE_GFX_TO_CPU_N<14>	OUT	95 162
PE_CPU_TO_GFX_C_P<15>	BC20 PCIE_RX15P	PCIE_TX15P BB21	PE_GFX_TO_CPU_P<15>	OUT	95 162
PE_CPU_TO_GFX_C_N<15>	BC21 PCIE_RX15N	PCIE_TX15N BB22	PE_GFX_TO_CPU_N<15>	OUT	95 162

PEG_CLK100M_P (TPA090, TP-P5)	AY5 PCIE_REFCLKP			
PEG_CLK100M_N (TPA091, TP-P5)	AY6 PCIE_REFCLKN			
GPU_RESET_L	BD3 PERST*	CLKREQ* BE3	PEG_CLKREQ_3V3_R_L — RA076 0 1/20W 5% MF 201 — PEG_CLKREQ_3V3_L	OUT 65
NC	BD8 WAKE* (RSVD)	(IPD) PX_EN AU16	BACO_EN	94

NOTE:
PEG CLKREQ L
HAS PU AT PCH

NOTE:
POWER XPRESS / BACO
OFF BY INTERNAL PD

NOTE:
VEGA10 SUPPORTS X16 LANE REVERSAL
AND POLARITY INVERSION
BOTH FEATURES NOT USED IN J137

NOTE:
POLARITY SWAP NOT SUPPORTED BY SKYLAKE
LANE REVERSAL IS SUPPORTED BUT NOT USED IN J137

DEBUG PINS

INTERNAL PU/PD AT GPIO PAD IS APPROX 40K

OMIT_TABLE

UA000
VEGA10-T7
TBD
BGA
SYM 3 OF 16
CRITICAL

GPU_PINSTRAP_0	BB3 PINSTRAP_0	(IPU)
GPU_PINSTRAP_1	BB2 PINSTRAP_1	(IPD)
GPU_PINSTRAP_2	BB1 PINSTRAP_2	(IPU)
GPU_PINSTRAP_3	BA3 PINSTRAP_3	(IPD)
GPU_PINSTRAP_4	BA2 PINSTRAP_4	(IPD)
GPU_PINSTRAP_5	AY3 PINSTRAP_5	(IPD)
GPU_PINSTRAP_6	AY2 PINSTRAP_6	(IPD)
GPU_PINSTRAP_7	AY1 PINSTRAP_7	(IPD)
GPU_OSX_GAN0	AP1 OSC_GAIN0	
GPU_OSX_GAN1	AP2 OSC_GAIN1	
GPU_OSX_GAN2	AP3 OSC_GAIN2	
GPU_REF_CLK100M_P	BE22 REFCLKP	
GPU_REF_CLK100M_N	BE23 REFCLKN	
NC	BE33 PUMPIN	
NC	BD33 PUMPOUT	
NC	BE29 FANIN	
NC	BD29 FANOUT	
NC	AT12 MACO_EN	(RSVD)
TPA050 (TP-P5)	TP_GPU_MTESTA	AM15 MTESTA
TPA051 (TP-P5)	TP_GPU_MTESTB	AN37 MTESTB
GPU_BP_0	AR1 BP_0	
GPU_BP_1	AR2 BP_1	
GPU_BP_2	AT2 BP_2	
GPU_BP_3	AT1 BP_3	

(PHY CALIBRATION PINS)

PP0V8_S0_GPU	RA033 200 1/20W MF 201	
DP_ZVDD_08 AH6	GPU_DP_ZVDD_08	
DP_ZVSS AG6	GPU_DP_ZVSS	
AUX_ZVSS P5	GPU_AUX_ZVSS	
PCIE_ZVSS AK5	GPU_PCIE_ZVSS	RA030 200, RA031 150, RA032 200 1/20W MF 201
TEST6 T37	GPU_DIECRACKMON	RA092 0 5% 1/20W MF 0201
CRACKMON		
INTCRACKMONDA AE18	NC	
INTCRACKMONDB AU35	NC	
INTCRACKMONGLL V10	NC	
INTCRACKMONGLR Y10	NC	
INTCRACKMONGUL V37	NC	
INTCRACKMONGUR Y37	NC	
INTCRACKMONP BC43	NC	
INTCRACKMONPDG BC43	NC	
TEST_PG AJ11	GPU_TEST_PG	RA090 1K, RA091 1K 5% 1/20W MF 201 (PP1V8_S0_GPU)
TEST_PG_BACO AV15	GPU_TEST_PG_BACO	
DBREQ* AM9	GPU_DBREQ_L	94
JTAG		
TDO AB8	GPU_JTAG_TDO	94 160
TDI AB9	GPU_JTAG_TDI	94 160
TMS AC7	GPU_JTAG_TMS	94 160
TCK AC8	GPU_JTAG_TCK	94 160
TESTEN AD8	GPU_JTAG_TESTEN	94 160
TRST* AA8	GPU_JTAG_TRST_L	94 160

PP3V3_S0 — RA061 10K, RA062 10K (NOSTUFF), RA063 10K, RA064 10K (NOSTUFF), RA065 10K (NOSTUFF), RA066 10K 5% 1/20W MF 201

PP1V8_S0_GPU — RA070, RA071, RA072, RA073 10K 5% 1/20W MF 201

PP1V8 PIN STRAPS

PP1V8_S0_GPU 45 94 98 99 112 119 160

RA000 10K 1/20W 5% MF 201 (NOSTUFF)	RA010 10K (NOSTUFF)	GPU_PINSTRAP_0	TPA000 (TP-P5)
RA001 10K	RA011 10K (NOSTUFF)	GPU_PINSTRAP_1	TPA001 (TP-P5)
RA002 10K (NOSTUFF)	RA012 10K	GPU_PINSTRAP_2	TPA002 (TP-P5)
RA003 10K	RA013 10K (NOSTUFF)	GPU_PINSTRAP_3	TPA003 (TP-P5)
RA004 10K	RA014 10K (NOSTUFF)	GPU_PINSTRAP_4	TPA004 (TP-P5)
RA005 10K	RA015 10K (NOSTUFF)	GPU_PINSTRAP_5	TPA005 (TP-P5)
RA006 10K	RA016 10K (NOSTUFF)	GPU_PINSTRAP_6	TPA006 (TP-P5)
RA007 10K (NOSTUFF)	RA017 10K	GPU_PINSTRAP_7	TPA007 (TP-P5)

ROM_CONFIG[2:0] = 101
FOR EXTERNAL ROM

AUD_PORT_CONFIG[2:0] = 000
ALL ENDPOINTS CONNECTED

BIF_GEN3_DIS_A = 0
PCIE GEN 3 SUPPORTED

CLK_PM_EN=1
CLKREQ PM CAPABILITY IS ENABLED

PP1V8_S0_GPU

GPU_JTAG_TCK	TPA020	RA045 1K (NOSTUFF), RA046 1K (NOSTUFF), RA043 1K (NOSTUFF), RA047 1K (NOSTUFF), RA050 1K
GPU_JTAG_TMS	TPA021	
GPU_JTAG_TDI	TPA022	
GPU_JTAG_TDO	TPA023	
GPU_JTAG_TRST_L	TPA024	RA052 33 5% 1/20W MF 201 — HDA_TRST_L
GPU_JTAG_TESTEN	TPA025	
GPU_DBREQ_L	TPA026	RA053 33 5% 1/20W MF 201 — HDA_DBREQ_L

RA044 1K (NOSTUFF), CA044 0.01UF 10% 25V X5R-CERM 0201, RA051 1K 5% 1/20W MF 201, CA045 0.01UF 10% 25V X5R-CERM 0201

SUPPORTS AMD
2 X 10 HEADER

PULL UPS

PP3V3_S0 — RA075 10K 5% 1/16W MF-LF 402 (NOSTUFF) — BACO_EN 94

BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE: GPU PCIE, STRAPS, JTAG

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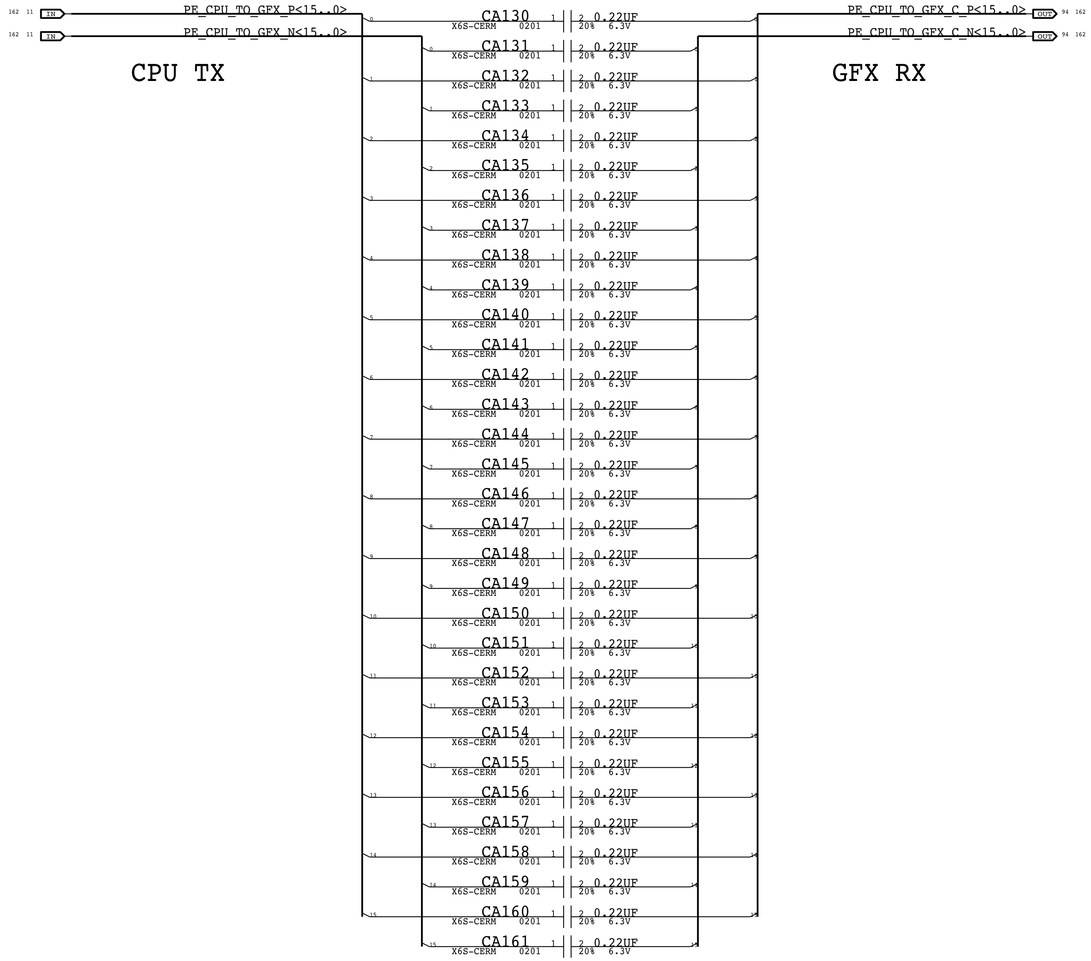
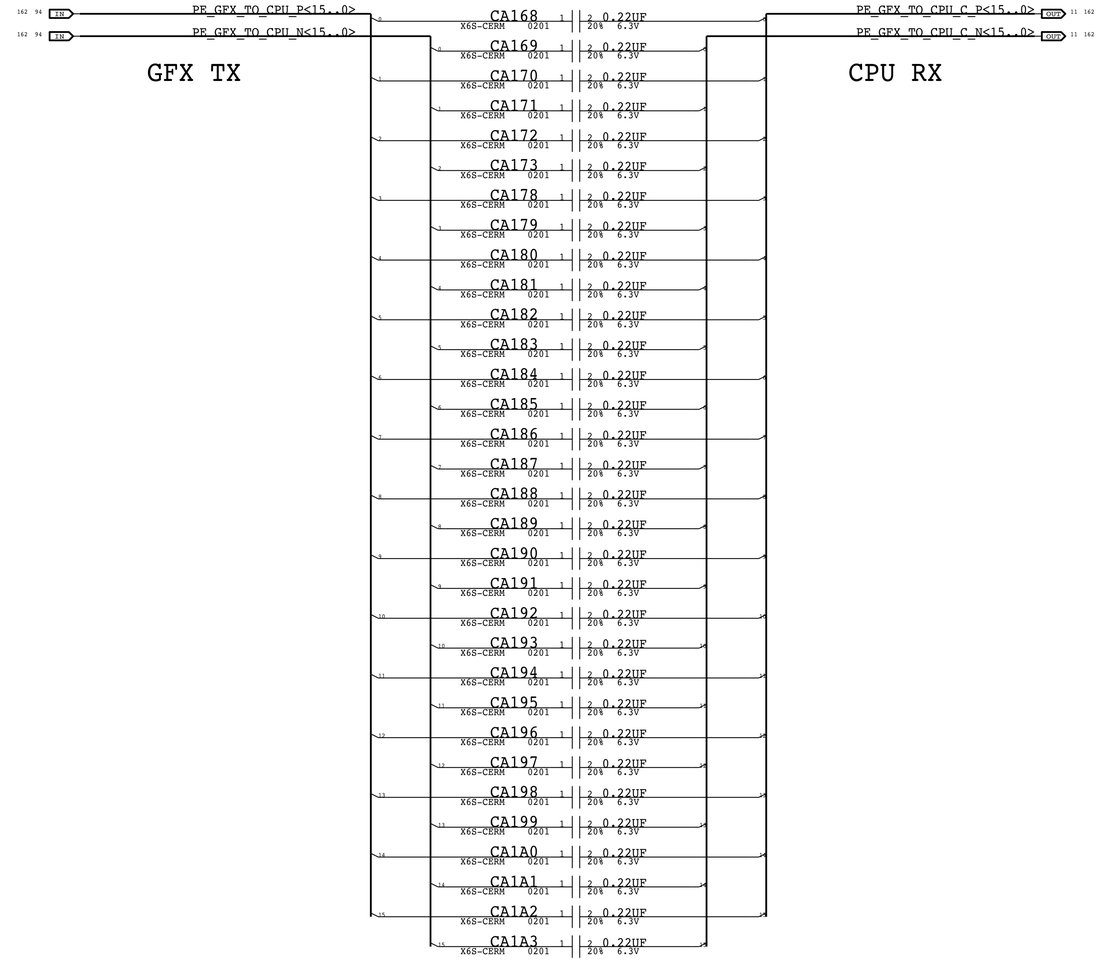
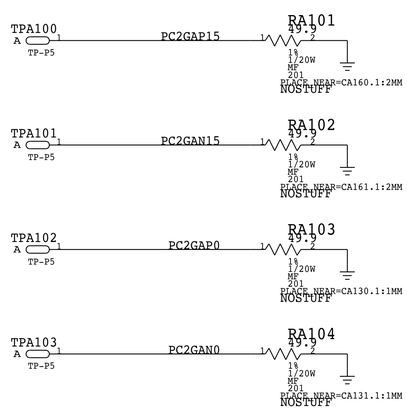
PCIE AC COUPLING CAPS CPU TO GFX
PLACE NEAR GFX



PCIE AC COUPLING CAPS GFX TO CPU
PLACE NEAR CPU





FOR PCIE MEASUREMENT

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GPU PCIE AC CAPS

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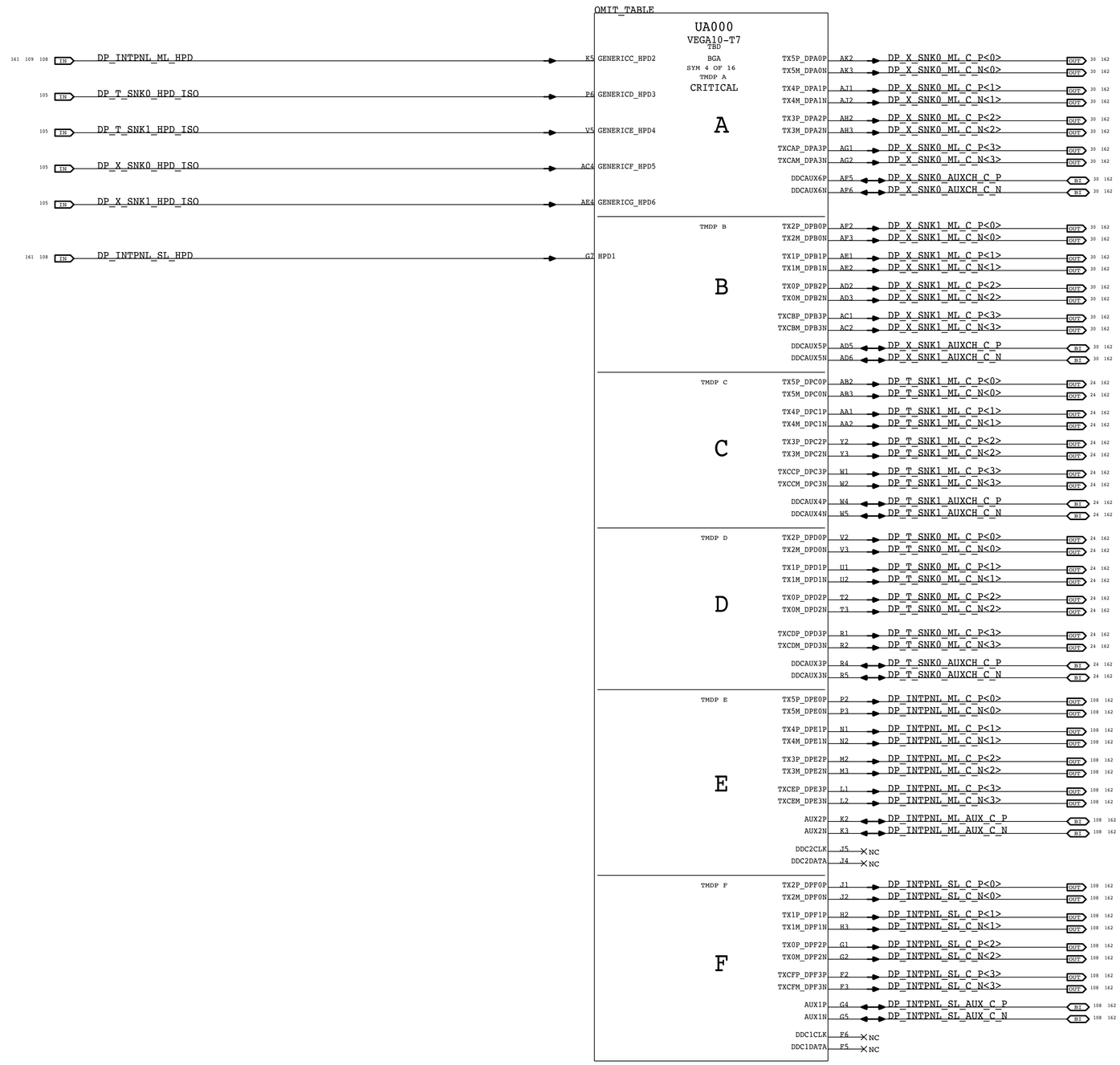

AC CAPS ON RIDGE PAGES

AC CAPS ON PANEL CONNECTOR PAGE

NOTE:

USB-C DOES NOTE SUPPORT DP++
VIDEO PORTS ARE CONFIG TO DP IN VBIOS

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PAGE TITLE
GPU DISPLAYPORT

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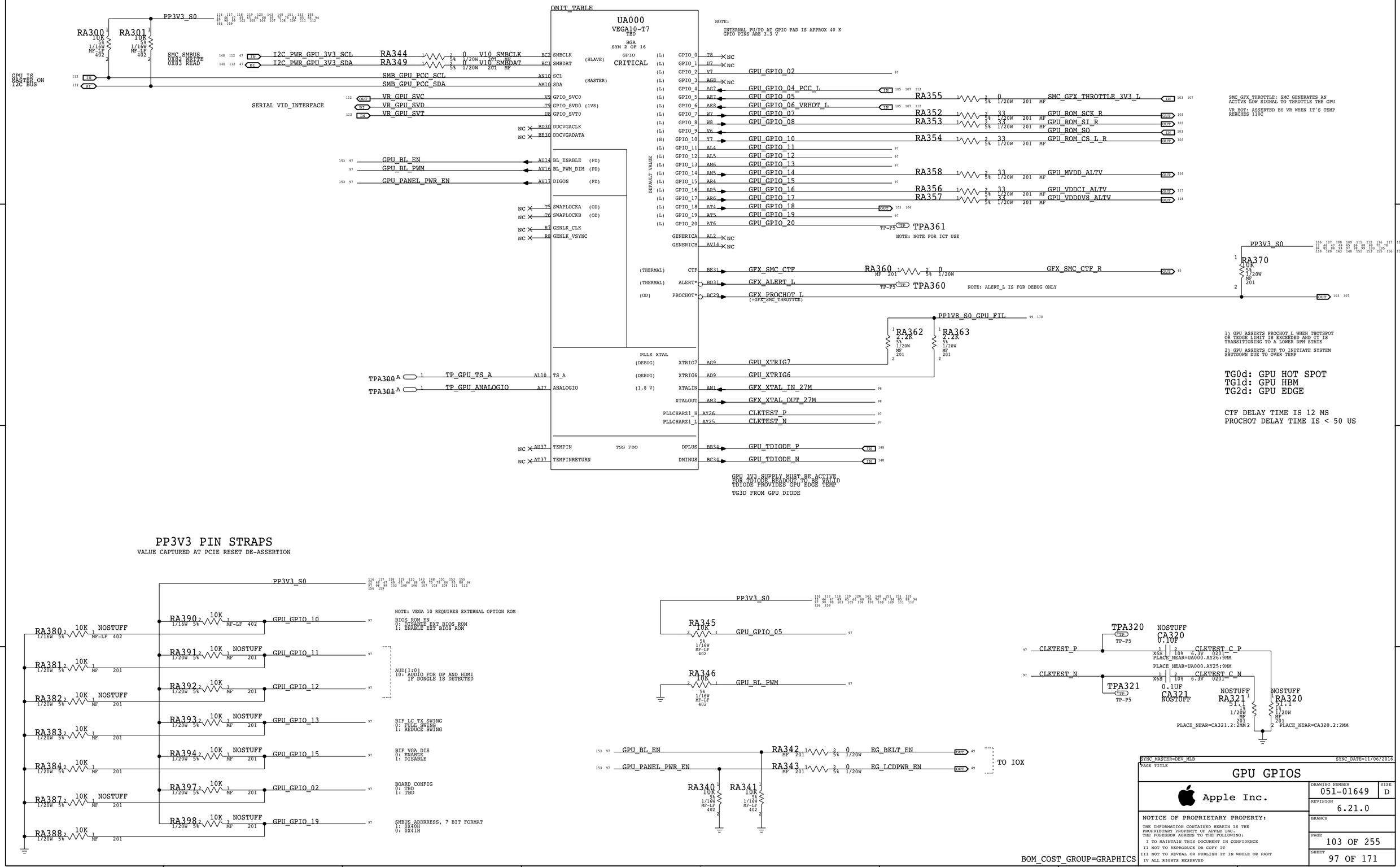
OMIT_TABLE
UA000
VEGA10-T7
TBD
BGA
SYM 2 OF 16
GPIO
CRITICAL
PP3V3_S0
RA300 10K 5% 1/16W MF-LF 402
RA301 10K 5% 1/16W MF-LF 402
SMC SMBUS
0x84 WRITE
0x85 READ
GPU IS MASTER ON I2C BUS
I2C_PWR_GPU_3V3_SCL
I2C_PWR_GPU_3V3_SDA
RA344 0 5% 1/20W 201 MF
RA349 0 5% 1/20W 201 MF
V10_SMBCLK
V10_SMBDAT
SMB_GPU_PCC_SCL
SMB_GPU_PCC_SDA
SERIAL VID_INTERFACE
VR_GPU_SVC
VR_GPU_SVD
VR_GPU_SVT
GPU_BL_EN
GPU_BL_PWM
GPU_PANEL_PWR_EN
TPA300 TP_GPU_TS_A
TPA301 TP_GPU_ANALOGIO
NOTE:
INTERNAL PU/PD AT GPIO PAD IS APPROX 40 K
GPIO PINS ARE 3.3 V
GPU_GPIO_02
GPU_GPIO_04_PCC_L
GPU_GPIO_05
GPU_GPIO_06_VRHOT_L
GPU_GPIO_07
GPU_GPIO_08
GPU_GPIO_10
GPU_GPIO_11
GPU_GPIO_12
GPU_GPIO_13
GPU_GPIO_14
GPU_GPIO_15
GPU_GPIO_16
GPU_GPIO_17
GPU_GPIO_18
GPU_GPIO_19
GPU_GPIO_20
RA355 0 5% 1/20W 201 MF SMC_GFX_THROTTLE_3V3_L
RA352 33 5% 1/20W 201 MF GPU_ROM_SCK_R
RA353 33 5% 1/20W 201 MF GPU_ROM_SI_R
GPU_ROM_SO
RA354 33 5% 1/20W 201 MF GPU_ROM_CS_L_R
RA358 33 5% 1/20W 201 MF GPU_MVDD_ALTV
RA356 33 5% 1/20W 201 MF GPU_VDDCI_ALTV
RA357 33 5% 1/20W 201 MF GPU_VDD0V8_ALTV
TPA361
NOTE: NOTE FOR ICT USE
SMC GFX THROTTLE: SMC GENERATES AN ACTIVE LOW SIGNAL TO THROTTLE THE GPU
VR HOT: ASSERTED BY VR WHEN IT'S TEMP REACHES 110C
PP3V3_S0
RA370 10K 5% 1/20W MF 201
RA360 0 5% 1/20W MF 201
GFX_SMC_CTF_R
TPA360
NOTE: ALERT_L IS FOR DEBUG ONLY
GFX_SMC_CTF
GFX_ALERT_L
GFX_PROCHOT_L
(=GFX_SMC_THROTTLE)
PP1V8_S0_GPU_FIL
RA362 2.2K 5% 1/20W MF 201
RA363 2.2K 5% 1/20W MF 201
GPU_XTRIG7
GPU_XTRIG6
GFX_XTAL_IN_27M
GFX_XTAL_OUT_27M
CLKTEST_P
CLKTEST_N
GPU_TDIODE_P
GPU_TDIODE_N
1) GPU ASSERTS PROCHOT L WHEN THOTSPOT OR TEDGE LIMIT IS EXCEEDED AND IT IS TRANSITIONING TO A LOWER DPM STATE
2) GPU ASSERTS CTF TO INITIATE SYSTEM SBUTDOWN DUE TO OVER TEMP
TG0d: GPU HOT SPOT
TG1d: GPU HBM
TG2d: GPU EDGE
CTF DELAY TIME IS 12 MS
PROCHOT DELAY TIME IS < 50 US
GPU 3V3 SUPPLY MUST BE ACTIVE FOR TDIODE READOUT TO BE VALID
TDIODE PROVIDES GPU EDGE TEMP
TG3D FROM GPU DIODE
PP3V3 PIN STRAPS
VALUE CAPTURED AT PCIE RESET DE-ASSERTION
RA380 10K 5% 1/16W MF-LF 402 NOSTUFF
RA381 10K 5% 1/20W MF 201
RA382 10K 5% 1/20W MF 201 NOSTUFF
RA383 10K 5% 1/20W MF 201
RA384 10K 5% 1/20W MF 201
RA387 10K 5% 1/20W MF 201 NOSTUFF
RA388 10K 5% 1/20W MF 201
RA390 10K 5% 1/16W MF-LF 402 GPU_GPIO_10
RA391 10K 5% 1/20W MF 201 NOSTUFF GPU_GPIO_11
RA392 10K 5% 1/20W MF 201 GPU_GPIO_12
RA393 10K 5% 1/20W MF 201 NOSTUFF GPU_GPIO_13
RA394 10K 5% 1/20W MF 201 NOSTUFF GPU_GPIO_15
RA397 10K 5% 1/20W MF 201 GPU_GPIO_02
RA398 10K 5% 1/20W MF 201 NOSTUFF GPU_GPIO_19
NOTE: VEGA 10 REQUIRES EXTERNAL OPTION ROM
BIOS_ROM_EN
0: DISABLE EXT BIOS ROM
1: ENABLE EXT BIOS ROM
AUD[1:0]
10: AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED
BIF_LC_TX_SWING
0: FULL SWING
1: REDUCE SWING
BIF_VGA_DIS
0: ENABLE
1: DISABLE
BOARD_CONFIG
0: TBD
1: TBD
SMBUS_ADDRRESS, 7 BIT FORMAT
1: 0X40H
0: 0X41H
RA345 10K 5% 1/16W MF-LF 402 GPU_GPIO_05
RA346 10K 5% 1/16W MF-LF 402 GPU_BL_PWM
TPA320 TP-P5
CA320 0.1UF 10% 6.3V 0201
PLACE_NEAR=UA000.AY26:9MM
PLACE_NEAR=UA000.AY25:9MM
TPA321 TP-P5
CA321 0.1UF 10% 6.3V 0201 NOSTUFF
RA321 51.1 1% 1/20W MF 201 NOSTUFF
RA320 51.1 1% 1/20W MF 201 NOSTUFF
PLACE_NEAR=CA321.2:2MM
PLACE_NEAR=CA320.2:2MM
RA342 0 5% 1/20W MF 201 EG_BKLT_EN
RA343 0 5% 1/20W MF 201 EG_LCDPWR_EN
TO IOX
RA340 10K 5% 1/16W MF-LF 402
RA341 10K 5% 1/16W MF-LF 402
BOM_COST_GROUP=GRAPHICS
SYNC_MASTER=DEV_MLB
SYNC_DATE=11/06/2016
PAGE TITLE
GPU GPIOS
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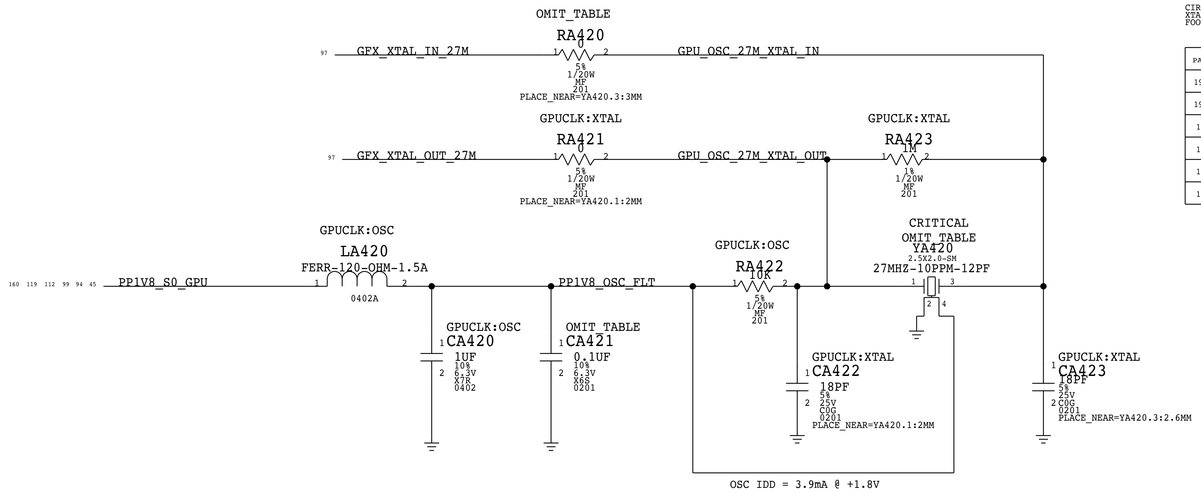
GPU 27 MHZ CLK

PIN	OSC	XTAL
1	OE/ST*	XTAL PIN 1
2	GND	NC
3	VOUT	XTAL PIN 2
4	VDD	NC

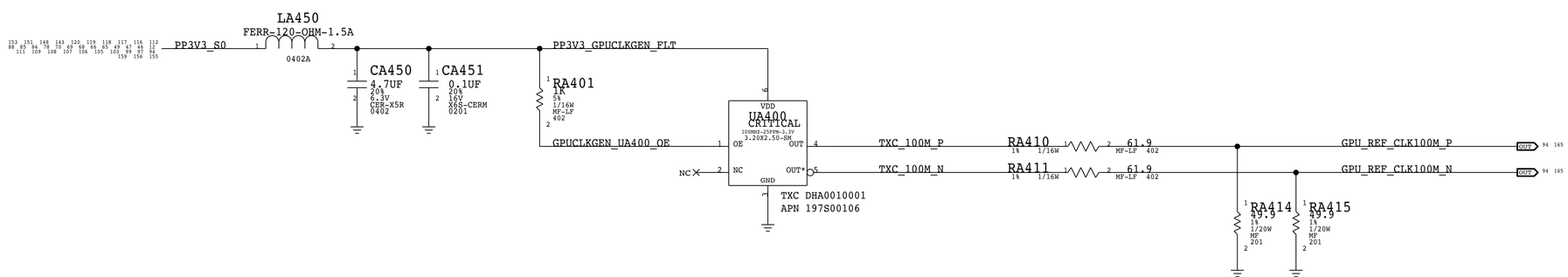
CIRCUIT FOR EITHER OSC OR XTAL, BOTH SHARE SAME THE FOOTPRINT

XTALIN IS 1.8V LEVEL
CLK GEN: 100 MHZ, NON SPREAD SPECTRUM, 1.8V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
197S00056	1	OSC,MEMS,100MHZ,+/-20%,1V8,2520	YA420	GPUCLK:OSC
197S00142	1	XTAL,27MHZ,10PPM,12PF,40OHM,2520	YA420	GPUCLK:XTAL
117S0080	1	RES,33OHM,5%,0201	RA420	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA420	GPUCLK:XTAL
117S0201	1	RES,0 OHM,5%,0201	CA421	GPUCLK:XTAL
132S0395	1	CAP,0.1UF,10%,0201	CA421	GPUCLK:OSC



GPU 100 MHZ CLK
(NO SPREAD)



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GPU CLK GEN

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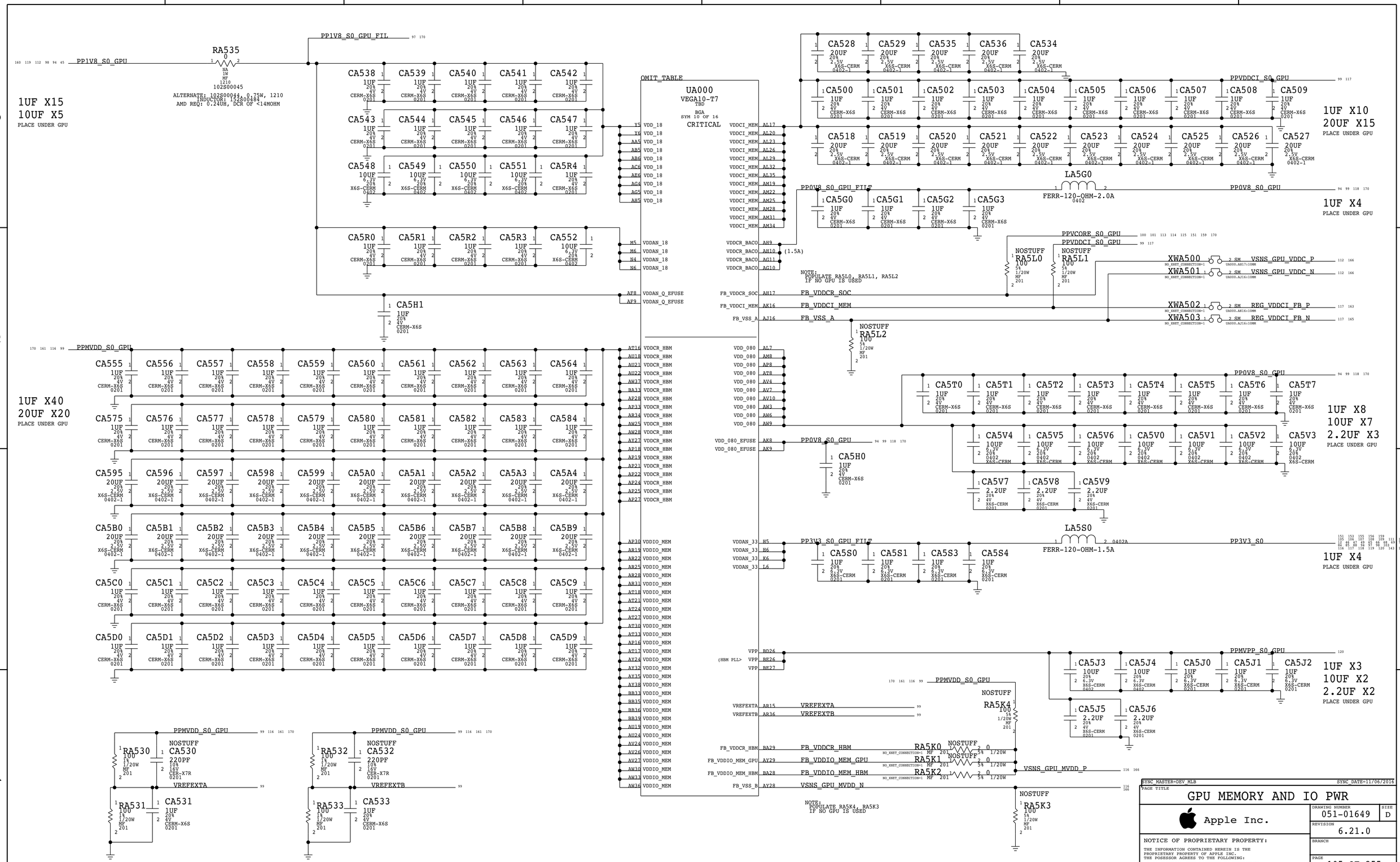
PP1V8_S0_GPU
RA535
0
NA
1W
MF
1210
102S00045
ALTERNATE: 102S00044, 0.75W, 1210
INDUCTOR: 152S00484
AMD REQ: 0.24UH, DCR OF <14MOHM
PP1V8_S0_GPU_FIL
1UF X15
10UF X5
PLACE UNDER GPU
OMIT_TABLE
UA000
VEGA10-T7
TBD
BGA
SYM 10 OF 16
CRITICAL
PPVDDCI_S0_GPU
1UF X10
20UF X15
PLACE UNDER GPU
LA5G0
FERR-120-OHM-2.0A
PP0V8_S0_GPU_FILT
PP0V8_S0_GPU
1UF X4
PLACE UNDER GPU
PPVCORE_S0_GPU
PPVDDCI_S0_GPU
NOSTUFF
RA5L0
RA5L1
XWA500
XWA501
XWA502
XWA503
VSNS_GPU_VDDC_P
VSNS_GPU_VDDC_N
REG_VDDCI_FB_P
REG_VDDCI_FB_N
NOTE:
POPULATE RA5L0, RA5L1, RA5L2
IF NO GPU IS USED
FB_VDDCR_SOC
FB_VDDCI_MEM
FB_VSS_A
RA5L2
PPMVDD_S0_GPU
1UF X40
20UF X20
PLACE UNDER GPU
PP0V8_S0_GPU
1UF X8
10UF X7
2.2UF X3
PLACE UNDER GPU
PP3V3_S0_GPU_FILT
LA5S0
FERR-120-OHM-1.5A
PP3V3_S0
1UF X4
PLACE UNDER GPU
PPVPP_S0_GPU
1UF X3
10UF X2
2.2UF X2
PLACE UNDER GPU
RA5K4
RA5K0
RA5K1
RA5K2
RA5K3
VSNS_GPU_MVDD_P
VSNS_GPU_MVDD_N
NOTE:
POPULATE RA5K4, RA5K3
IF NO GPU IS USED
RA530
CA530
220PF
VREFEXTA
RA531
CA531
RA532
CA532
VREFEXTB
RA533
CA533
BOM_COST_GROUP=GRAPHICS
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SYNC_DATE=11/06/2016
PAGE TITLE
GPU MEMORY AND IO PWR
Apple Inc.
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170 159 151 115 114 113 101 99 PPVCORE_S0_GPU

OMIT_TABLE

UA000
VEGA10-T7
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CRITICAL

A10	VDDCR_SOC	VDDCR_SOC	AC27
A11	VDDCR_SOC	VDDCR_SOC	AC28
A12	VDDCR_SOC	VDDCR_SOC	AC29
A13	VDDCR_SOC	VDDCR_SOC	AC30
A14	VDDCR_SOC	VDDCR_SOC	AC31
A15	VDDCR_SOC	VDDCR_SOC	AC32
A16	VDDCR_SOC	VDDCR_SOC	AC33
A17	VDDCR_SOC	VDDCR_SOC	AC34
A18	VDDCR_SOC	VDDCR_SOC	AC35
A19	VDDCR_SOC	VDDCR_SOC	AC36
A2	VDDCR_SOC	VDDCR_SOC	AC37
A20	VDDCR_SOC	VDDCR_SOC	AC41
A21	VDDCR_SOC	VDDCR_SOC	AC45
A22	VDDCR_SOC	VDDCR_SOC	AD13
A23	VDDCR_SOC	VDDCR_SOC	AD14
A24	VDDCR_SOC	VDDCR_SOC	AD17
A25	VDDCR_SOC	VDDCR_SOC	AD18
A26	VDDCR_SOC	VDDCR_SOC	AD21
A27	VDDCR_SOC	VDDCR_SOC	AD22
A28	VDDCR_SOC	VDDCR_SOC	AD23
A29	VDDCR_SOC	VDDCR_SOC	AD24
A3	VDDCR_SOC	VDDCR_SOC	AD25
A30	VDDCR_SOC	VDDCR_SOC	AD26
A31	VDDCR_SOC	VDDCR_SOC	AD27
A32	VDDCR_SOC	VDDCR_SOC	AD28
A33	VDDCR_SOC	VDDCR_SOC	AD29
A34	VDDCR_SOC	VDDCR_SOC	AD30
A35	VDDCR_SOC	VDDCR_SOC	AD31
A36	VDDCR_SOC	VDDCR_SOC	AD32
A37	VDDCR_SOC	VDDCR_SOC	AD33
A38	VDDCR_SOC	VDDCR_SOC	AD34
A39	VDDCR_SOC	VDDCR_SOC	AD35
A4	VDDCR_SOC	VDDCR_SOC	AD36
A40	VDDCR_SOC	VDDCR_SOC	AD39
A42	VDDCR_SOC	VDDCR_SOC	AD43
A43	VDDCR_SOC	VDDCR_SOC	AD45
A44	VDDCR_SOC	VDDCR_SOC	AE13
A6	VDDCR_SOC	VDDCR_SOC	AE14
A7	VDDCR_SOC	VDDCR_SOC	AE17
A8	VDDCR_SOC	VDDCR_SOC	AE18
A9	VDDCR_SOC	VDDCR_SOC	AE45
AA13	VDDCR_SOC	VDDCR_SOC	AF17
AA14	VDDCR_SOC	VDDCR_SOC	AF18
AA17	VDDCR_SOC	VDDCR_SOC	AF45
AA18	VDDCR_SOC	VDDCR_SOC	AG17
AA21	VDDCR_SOC	VDDCR_SOC	AG18
AA22	VDDCR_SOC	VDDCR_SOC	AG19
AA45	VDDCR_SOC	VDDCR_SOC	AG20
AB13	VDDCR_SOC	VDDCR_SOC	AG21
AB14	VDDCR_SOC	VDDCR_SOC	AG22
AB17	VDDCR_SOC	VDDCR_SOC	AG23
AB18	VDDCR_SOC	VDDCR_SOC	AG24
AB21	VDDCR_SOC	VDDCR_SOC	AG25
AB22	VDDCR_SOC	VDDCR_SOC	AG26
AB45	VDDCR_SOC	VDDCR_SOC	AG27
AC13	VDDCR_SOC	VDDCR_SOC	AG28
AC14	VDDCR_SOC	VDDCR_SOC	AG29
AC17	VDDCR_SOC	VDDCR_SOC	AG30
AC18	VDDCR_SOC	VDDCR_SOC	AG31
AC21	VDDCR_SOC	VDDCR_SOC	AG32
AC22	VDDCR_SOC	VDDCR_SOC	AG33
AC23	VDDCR_SOC	VDDCR_SOC	AG34
AC24	VDDCR_SOC	VDDCR_SOC	AG35
AC25	VDDCR_SOC	VDDCR_SOC	AG36
AC26	VDDCR_SOC	VDDCR_SOC	AG37

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AG41	VDDCR_SOC	VDDCR_SOC	D35
AG45	VDDCR_SOC	VDDCR_SOC	D45
AH18	VDDCR_SOC	VDDCR_SOC	P15
AH19	VDDCR_SOC	VDDCR_SOC	P19
AH20	VDDCR_SOC	VDDCR_SOC	P23
AH21	VDDCR_SOC	VDDCR_SOC	P27
AH22	VDDCR_SOC	VDDCR_SOC	P31
AH23	VDDCR_SOC	VDDCR_SOC	P35
AH24	VDDCR_SOC	VDDCR_SOC	P45
AH25	VDDCR_SOC	VDDCR_SOC	G45
AH26	VDDCR_SOC	VDDCR_SOC	H15
AH27	VDDCR_SOC	VDDCR_SOC	H19
AH28	VDDCR_SOC	VDDCR_SOC	H23
AH29	VDDCR_SOC	VDDCR_SOC	H27
AH30	VDDCR_SOC	VDDCR_SOC	H31
AH31	VDDCR_SOC	VDDCR_SOC	H35
AH32	VDDCR_SOC	VDDCR_SOC	H39
AH33	VDDCR_SOC	VDDCR_SOC	H43
AH34	VDDCR_SOC	VDDCR_SOC	H45
AH35	VDDCR_SOC	VDDCR_SOC	J13
AH36	VDDCR_SOC	VDDCR_SOC	J17
AH39	VDDCR_SOC	VDDCR_SOC	J21
AH43	VDDCR_SOC	VDDCR_SOC	J25
AH45	VDDCR_SOC	VDDCR_SOC	J29
AJ45	VDDCR_SOC	VDDCR_SOC	J33
AK45	VDDCR_SOC	VDDCR_SOC	J45
AL41	VDDCR_SOC	VDDCR_SOC	K13
AL45	VDDCR_SOC	VDDCR_SOC	K14
AM39	VDDCR_SOC	VDDCR_SOC	K17
AM43	VDDCR_SOC	VDDCR_SOC	K18
AM44	VDDCR_SOC	VDDCR_SOC	K21
AM45	VDDCR_SOC	VDDCR_SOC	K22
AN43	VDDCR_SOC	VDDCR_SOC	K25
AN44	VDDCR_SOC	VDDCR_SOC	K26
AN45	VDDCR_SOC	VDDCR_SOC	K29
AP42	VDDCR_SOC	VDDCR_SOC	K30
AP43	VDDCR_SOC	VDDCR_SOC	K33
AP44	VDDCR_SOC	VDDCR_SOC	K34
AP45	VDDCR_SOC	VDDCR_SOC	K39
AR41	VDDCR_SOC	VDDCR_SOC	K43
AR42	VDDCR_SOC	VDDCR_SOC	K45
AR43	VDDCR_SOC	VDDCR_SOC	L13
AR44	VDDCR_SOC	VDDCR_SOC	L14
AT39	VDDCR_SOC	VDDCR_SOC	L17
AT40	VDDCR_SOC	VDDCR_SOC	L18
AT41	VDDCR_SOC	VDDCR_SOC	L21
AT42	VDDCR_SOC	VDDCR_SOC	L22
AU38	VDDCR_SOC	VDDCR_SOC	L25
AU39	VDDCR_SOC	VDDCR_SOC	L26
AU40	VDDCR_SOC	VDDCR_SOC	L29
AU41	VDDCR_SOC	VDDCR_SOC	L30
B10	VDDCR_SOC	VDDCR_SOC	L33
B15	VDDCR_SOC	VDDCR_SOC	L34
B19	VDDCR_SOC	VDDCR_SOC	L35
B23	VDDCR_SOC	VDDCR_SOC	L36
B27	VDDCR_SOC	VDDCR_SOC	L37
B31	VDDCR_SOC	VDDCR_SOC	L41
B35	VDDCR_SOC	VDDCR_SOC	L45
B45	VDDCR_SOC	VDDCR_SOC	M13
C45	VDDCR_SOC	VDDCR_SOC	M14
D15	VDDCR_SOC	VDDCR_SOC	M17
D19	VDDCR_SOC	VDDCR_SOC	M18
D23	VDDCR_SOC	VDDCR_SOC	M21
D27	VDDCR_SOC	VDDCR_SOC	M22
D31	VDDCR_SOC	VDDCR_SOC	M25

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M26	VDDCR_SOC	VDDCR_SOC	T35
M29	VDDCR_SOC	VDDCR_SOC	T36
M30	VDDCR_SOC	VDDCR_SOC	T39
M33	VDDCR_SOC	VDDCR_SOC	T43
M34	VDDCR_SOC	VDDCR_SOC	T45
M35	VDDCR_SOC	VDDCR_SOC	U13
M36	VDDCR_SOC	VDDCR_SOC	U14
M39	VDDCR_SOC	VDDCR_SOC	U17
M43	VDDCR_SOC	VDDCR_SOC	U18
M45	VDDCR_SOC	VDDCR_SOC	U21
N13	VDDCR_SOC	VDDCR_SOC	U22
N14	VDDCR_SOC	VDDCR_SOC	U25
N17	VDDCR_SOC	VDDCR_SOC	U26
N18	VDDCR_SOC	VDDCR_SOC	U45
N21	VDDCR_SOC	VDDCR_SOC	V13
N22	VDDCR_SOC	VDDCR_SOC	V14
N25	VDDCR_SOC	VDDCR_SOC	V17
N26	VDDCR_SOC	VDDCR_SOC	V18
N29	VDDCR_SOC	VDDCR_SOC	V21
N30	VDDCR_SOC	VDDCR_SOC	V22
N45	VDDCR_SOC	VDDCR_SOC	V25
P13	VDDCR_SOC	VDDCR_SOC	V26
P14	VDDCR_SOC	VDDCR_SOC	V45
P17	VDDCR_SOC	VDDCR_SOC	W13
P18	VDDCR_SOC	VDDCR_SOC	W14
P21	VDDCR_SOC	VDDCR_SOC	W17
P22	VDDCR_SOC	VDDCR_SOC	W18
P25	VDDCR_SOC	VDDCR_SOC	W21
P26	VDDCR_SOC	VDDCR_SOC	W22
P29	VDDCR_SOC	VDDCR_SOC	W25
P30	VDDCR_SOC	VDDCR_SOC	W26
P45	VDDCR_SOC	VDDCR_SOC	W27
R13	VDDCR_SOC	VDDCR_SOC	W28
R14	VDDCR_SOC	VDDCR_SOC	W29
R17	VDDCR_SOC	VDDCR_SOC	W30
R18	VDDCR_SOC	VDDCR_SOC	W31
R21	VDDCR_SOC	VDDCR_SOC	W32
R22	VDDCR_SOC	VDDCR_SOC	W33
R25	VDDCR_SOC	VDDCR_SOC	W34
R26	VDDCR_SOC	VDDCR_SOC	W35
R29	VDDCR_SOC	VDDCR_SOC	W36
R30	VDDCR_SOC	VDDCR_SOC	W37
R31	VDDCR_SOC	VDDCR_SOC	W41
R32	VDDCR_SOC	VDDCR_SOC	W45
R33	VDDCR_SOC	VDDCR_SOC	Y13
R34	VDDCR_SOC	VDDCR_SOC	Y14
R35	VDDCR_SOC	VDDCR_SOC	Y17
R36	VDDCR_SOC	VDDCR_SOC	Y18
R37	VDDCR_SOC	VDDCR_SOC	Y21
R41	VDDCR_SOC	VDDCR_SOC	Y22
R45	VDDCR_SOC	VDDCR_SOC	Y25
T13	VDDCR_SOC	VDDCR_SOC	Y26
T14	VDDCR_SOC	VDDCR_SOC	Y27
T17	VDDCR_SOC	VDDCR_SOC	Y28
T18	VDDCR_SOC	VDDCR_SOC	Y29
T21	VDDCR_SOC	VDDCR_SOC	Y30
T22	VDDCR_SOC	VDDCR_SOC	Y31
T25	VDDCR_SOC	VDDCR_SOC	Y32
T26	VDDCR_SOC	VDDCR_SOC	Y33
T29	VDDCR_SOC	VDDCR_SOC	Y34
T30	VDDCR_SOC	VDDCR_SOC	Y35
T31	VDDCR_SOC	VDDCR_SOC	Y36
T32	VDDCR_SOC	VDDCR_SOC	Y39
T33	VDDCR_SOC	VDDCR_SOC	Y43
T34	VDDCR_SOC	VDDCR_SOC	Y45

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CA700	CA701	CA702	CA703	CA704	CA705	CA706	CA707	CA708	CA709	CA710	CA711	CA712	CA713	CA714	CA7S0	CA7S1	CA7S2	CA7S3	CA7S4
CA715	CA716	CA717	CA718	CA719	CA720	CA721	CA722	CA723	CA724	CA725	CA726	CA727	CA728	CA729	CA7S5	CA7S6	CA7S7	CA7S8	CA7S9
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CA745	CA746	CA747	CA748	CA749	CA750	CA751	CA752	CA753	CA754	CA755	CA756	CA757	CA758	CA759					
CA760	CA761	CA762	CA763	CA764	CA765	CA766	CA767	CA768	CA769	CA770	CA771	CA772	CA773	CA774	CA7B5	CA7B6	CA7B7	CA7B8	CA7B9
CA775	CA776	CA777	CA778	CA779	CA780	CA781	CA782	CA783	CA784	CA785	CA786	CA787	CA788	CA789	CA7B0	CA7B1	CA7B2	CA7B3	CA7B4
CA790	CA791	CA792	CA793	CA794	CA795	CA796	CA797	CA798	CA799	CA7A0	CA7A1	CA7A2	CA7A3	CA7A4	CA7A5	CA7A6	CA7A7	CA7A8	CA7A9
CA7P0	CA7P1	CA7P2	CA7P3	CA7P4	CA7P5	CA7P6	CA7P7	CA7P8	CA7P9	CA7Q0	CA7Q1	CA7Q2	CA7Q3	CA7Q4	CA7U0	CA7U1	CA7U2	CA7U3	CA7U4
CA7C0	CA7C1	CA7C2	CA7C3	CA7C4	CA7C5	CA7C6	CA7C7	CA7C8	CA7C9	CA7D0	CA7D1	CA7D2	CA7D3	CA7D4	CA7U5	CA7U6	CA7U7	CA7U8	CA7U9
CA7D5	CA7D6	CA7D7	CA7D8	CA7D9	CA7E0	CA7E1	CA7E2	CA7E3	CA7E4	CA7E5	CA7E6	CA7E7	CA7E8	CA7E9	CA7V0	CA7V1	CA7V2	CA7V3	CA7V4
CA7G5	CA7J0	CA7K5	CA7M0	CA7K6	CA7J1	CA7K7	CA7K8	CA7M3	CA7J5	CA7M5	CA7K9	CA7J6	CA7J7	CA7L2	CA7M8	CA7J9	CA7L3	CA7L5	CA7L6
CA7H4	NOSTUFF CA7H9	NOSTUFF CA7K0	CA7K1	CA7K4	CA7N4	CA7N2	CA7N1	NOSTUFF CA7L7	CA7J3	CA7BA	NOSTUFF CA7BB	NOSTUFF CA7BC	CA7BD	CA7BK	NOSTUFF CA7BE	CA7BF	CA7BG	CA7BH	CA7BJ
CA7J2	CA7G6	NOSTUFF CA7G7	CA7G8	CA7G9	CA7H0	CA7H1	CA7H2	CA7H3	NOSTUFF CA7L4	CA7H5	CA7H6	CA7H7	CA7H8	CA7N3	CA7V5	CA7V6	CA7V7	CA7V8	CA7V9
CA7L9	CA7M1	NOSTUFF CA7M2	CA7M4	CA7J4	CA7L0	CA7L1	CA7M6	CA7J8	CA7M7	CA7M9	CA7N0	CA7K2	CA7K3	CA7L8	NOSTUFF CA7W0	NOSTUFF CA7W1	CA7W2	CA7W3	CA7W4
CA7W5	NOSTUFF CA7W6	CA7W7	CA7W8	CA7W9	CA7Y0	NOSTUFF CA7Y1	CA7Y2	CA7Y3	CA7Y4	CA7AA	CA7AB	NOSTUFF CA7AC	NOSTUFF CA7AD	CA7AE					

1UF 20% 4V CERM-X6S 0201

20UF 20% 2.5V X6S-CERM 0402-1

43UF 20% 2.5V X6S 0603

GPU VDDC DECOUPLING
PLACE ALL CAPS UNDER GPU

1UF X130 138S0775
20UF X80 138S00036
43UF X60 138S00168
43UF X15 138S00168 NOSTUFF

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AA15	VSS	VSS	AP13
AA16	VSS	VSS	AP14
AA19	VSS	VSS	AP15
AA20	VSS	VSS	AP16
AA23	VSS	VSS	AP19
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AA27	VSS	VSS	AP23
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AA3	VSS	VSS	AP26
AA30	VSS	VSS	AP27
AA31	VSS	VSS	AP28
AA32	VSS	VSS	AP29
AA33	VSS	VSS	AP30
AA34	VSS	VSS	AP31
AA35	VSS	VSS	AP32
AA36	VSS	VSS	AP33
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AA41	VSS	VSS	AP35
AA6	VSS	VSS	AP36
AA9	VSS	VSS	AP39
AB1	VSS	VSS	AP4
AB11	VSS	VSS	AP43
AB12	VSS	VSS	AP7
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AB19	VSS	VSS	AG14
AB20	VSS	VSS	AG15
AB23	VSS	VSS	AG16
AB24	VSS	VSS	AG3
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AB27	VSS	VSS	AH12
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AB31	VSS	VSS	AH16
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AC16	VSS	VSS	AJ34
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AD7	VSS	VSS	AK33
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AF1	VSS	VSS	AN33
AF11	VSS	VSS	AN36

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AP35	VSS	VSS	BC25
AP7	VSS	VSS	BC30
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AR13	VSS	VSS	BC35
AR16	VSS	VSS	BC38
AR3	VSS	VSS	BC4
AR7	VSS	VSS	BC41
AR9	VSS	VSS	BC44
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AU29	VSS	VSS	BD44
AU32	VSS	VSS	BD45
AU35	VSS	VSS	BD5
AU45	VSS	VSS	BD6
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AV28	VSS	VSS	BE14
AV31	VSS	VSS	BE17
AV34	VSS	VSS	BE2
AV37	VSS	VSS	BE20
AV43	VSS	VSS	BE21
AV5	VSS	VSS	BE25
AV6	VSS	VSS	BE28
AV9	VSS	VSS	BE34
AW11	VSS	VSS	BE37
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AW41	VSS	VSS	C21
AW45	VSS	VSS	C25
AW5	VSS	VSS	C29
AW8	VSS	VSS	C33
AY10	VSS	VSS	C37
AY13	VSS	VSS	C41
AY16	VSS	VSS	C5
AY19	VSS	VSS	C9
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BA22	VSS	VSS	E5
BA27	VSS	VSS	E9
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BA34	VSS	VSS	F11
BA37	VSS	VSS	F39
BA41	VSS	VSS	F4
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G6	VSS	VSS	P4
G9	VSS	VSS	P43
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H7	VSS	VSS	R16
J3	VSS	VSS	R19
J37	VSS	VSS	R20
J41	VSS	VSS	R23
J6	VSS	VSS	R24
J9	VSS	VSS	R27
K1	VSS	VSS	R28
K11	VSS	VSS	R3
K12	VSS	VSS	R6
K15	VSS	VSS	R9
K16	VSS	VSS	T1
K19	VSS	VSS	T11
K20	VSS	VSS	T12
K23	VSS	VSS	T15
K24	VSS	VSS	T16
K27	VSS	VSS	T19
K28	VSS	VSS	T20
K31	VSS	VSS	T23
K32	VSS	VSS	T24
K35	VSS	VSS	T27
K36	VSS	VSS	T28
K4	VSS	VSS	T4
K7	VSS	VSS	T7
L12	VSS	VSS	U12
L15	VSS	VSS	U15
L16	VSS	VSS	U16
L19	VSS	VSS	U19
L20	VSS	VSS	U20
L23	VSS	VSS	U23
L24	VSS	VSS	U24
L27	VSS	VSS	U27
L28	VSS	VSS	U28
L3	VSS	VSS	U29
L31	VSS	VSS	U3
L32	VSS	VSS	U30
L5	VSS	VSS	U31
L9	VSS	VSS	U32
M1	VSS	VSS	U33
M11	VSS	VSS	U34
M12	VSS	VSS	U35
M15	VSS	VSS	U36
M16	VSS	VSS	U37
M19	VSS	VSS	U41
M20	VSS	VSS	U6
M23	VSS	VSS	U9
M24	VSS	VSS	V1
M27	VSS	VSS	V11
M28	VSS	VSS	V12
M31	VSS	VSS	V15
M32	VSS	VSS	V16
M4	VSS	VSS	V19
M7	VSS	VSS	V20
N12	VSS	VSS	V23
N15	VSS	VSS	V24
N16	VSS	VSS	V27
N19	VSS	VSS	V28
N20	VSS	VSS	V29
N23	VSS	VSS	V30
N24	VSS	VSS	V31
N27	VSS	VSS	V32
N28	VSS	VSS	V33
N3	VSS	VSS	V34
N31	VSS	VSS	V35
N32	VSS	VSS	V36
N33	VSS	VSS	V39
N34	VSS	VSS	V4
N35	VSS	VSS	V43
N36	VSS	VSS	V8
N37	VSS	VSS	W12
N41	VSS	VSS	W15
N5	VSS	VSS	W16
N9	VSS	VSS	W19
P1	VSS	VSS	W20
P11	VSS	VSS	W23
P12	VSS	VSS	W24
P15	VSS	VSS	W3
P16	VSS	VSS	W6
P19	VSS	VSS	W9
P20	VSS	VSS	Y1
P23	VSS	VSS	Y11
P24	VSS	VSS	Y12
P27	VSS	VSS	Y15
P28	VSS	VSS	Y16
P31	VSS	VSS	Y19
P32	VSS	VSS	Y20
P33	VSS	VSS	Y23
P34	VSS	VSS	Y24
P35	VSS	VSS	Y4
P36	VSS	VSS	Y8

BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

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GPU GND

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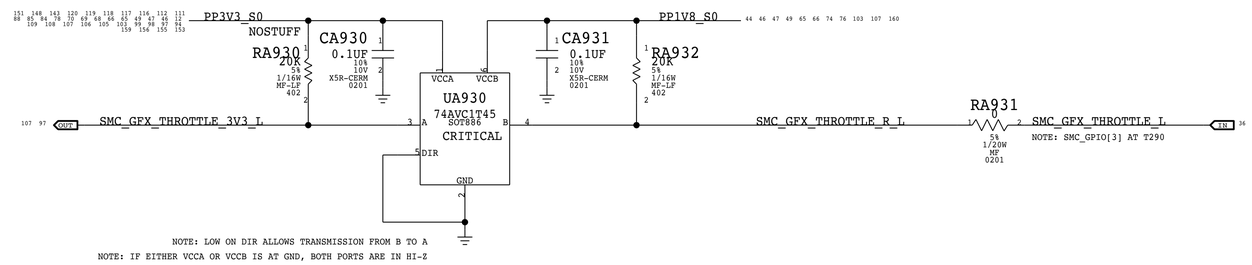
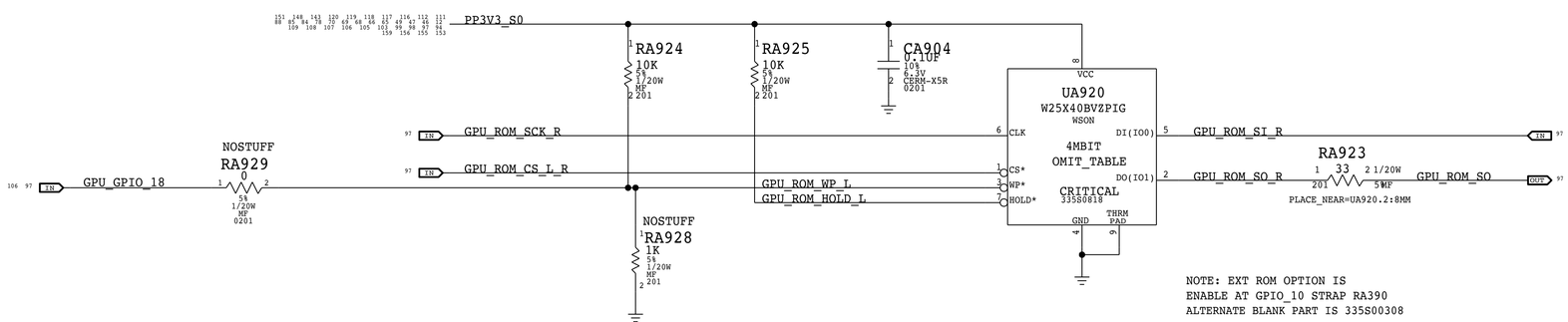
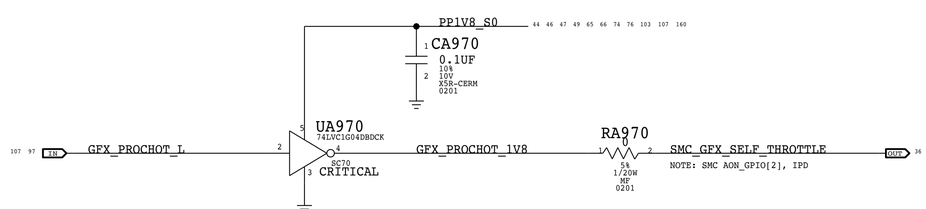
GFX THROTTLE LEVEL SHIFTING



GPU BOOT ROM



PROCHOT INVERTER AND LEVEL SHIFTER



BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

GPU ROM, TEMP, LVL SHIFT

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DFTIO

OMIT_TABLE

UA000
VEGA10-T7
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SYM 5 OF 16
CRITICAL

NC	J7	DFTIO_0	DFTIO_96	C18	NC
NC	L11	DFTIO_1	DFTIO_97	B16	NC
NC	E4	DFTIO_2	DFTIO_98	G20	NC
NC	L8	DFTIO_3	DFTIO_99	J20	NC
NC	M10	DFTIO_4	DFTIO_100	J19	NC
NC	E3	DFTIO_5	DFTIO_101	D17	NC
NC	M9	DFTIO_6	DFTIO_102	C19	NC
NC	L7	DFTIO_7	DFTIO_103	F18	NC
NC	N8	DFTIO_8	DFTIO_104	C20	NC
NC	C2	DFTIO_9	DFTIO_105	D18	NC
NC	N10	DFTIO_10	DFTIO_106	E22	NC
NC	M8	DFTIO_11	DFTIO_107	B17	NC
NC	E6	DFTIO_12	DFTIO_108	D20	NC
NC	D4	DFTIO_13	DFTIO_109	B18	NC
NC	K9	DFTIO_14	DFTIO_110	D21	NC
NC	P9	DFTIO_15	DFTIO_111	E19	NC
NC	E7	DFTIO_16	DFTIO_112	B20	NC
NC	C1	DFTIO_17	DFTIO_113	H26	NC
NC	D2	DFTIO_18	DFTIO_114	G23	NC
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NC	C3	DFTIO_21	DFTIO_117	E20	NC
NC	C4	DFTIO_22	DFTIO_118	C26	NC
NC	K8	DFTIO_23	DFTIO_119	C23	NC
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NC	F8	DFTIO_25	DFTIO_121	B22	NC
NC	J8	DFTIO_26	DFTIO_122	F22	NC
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NC	D5	DFTIO_33	DFTIO_129	C24	NC
NC	E8	DFTIO_34	DFTIO_130	G28	NC
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NC	J12	DFTIO_41	DFTIO_137	D28	NC
NC	G10	DFTIO_42	DFTIO_138	F21	NC
NC	H9	DFTIO_43	DFTIO_139	C28	NC
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NC	D9	DFTIO_47	DFTIO_143	B26	NC
NC	B6	DFTIO_48	DFTIO_144	G27	NC
NC	C7	DFTIO_49	DFTIO_145	F24	NC
NC	F13	DFTIO_50	DFTIO_146	D26	NC
NC	J16	DFTIO_51	DFTIO_147	C32	NC
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NC	C11	DFTIO_87	DFTIO_183	F29	NC
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NC	F17	DFTIO_95	DFTIO_191	H29	NC

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CRITICAL

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NC	J30	DFTIO_197	DFTIO_293	W40	NC
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NC	E43	DFTIO_199	DFTIO_295	P37	NC
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NC	H37	DFTIO_207	DFTIO_303	T40	NC
NC	E34	DFTIO_208	DFTIO_304	W42	NC
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NC	H42	DFTIO_226	DFTIO_322	T38	NC
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NC	J44	DFTIO_231	DFTIO_327	AD41	NC
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NC	F37	DFTIO_243	DFTIO_339	AN42	NC
NC	G40	DFTIO_244	DFTIO_340	AT44	NC
NC	G39	DFTIO_245	DFTIO_341	AR45	NC
NC	K40	DFTIO_246	DFTIO_342	AJ40	NC
NC	J34	DFTIO_247	DFTIO_343	AY45	NC
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NC	P44	DFTIO_258	DFTIO_354	BA40	NC
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NC	N42	DFTIO_260	DFTIO_356	AY44	NC
NC	M41	DFTIO_261	DFTIO_357	AU42	NC
NC	R43	DFTIO_262	DFTIO_358	AU43	NC
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NC	P42	DFTIO_267	DFTIO_363	AN39	NC
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NC	H38	DFTIO_269	DFTIO_365	AR40	NC
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NC	H33	DFTIO_281	DFTIO_377	AK41	NC
NC	M40	DFTIO_282	DFTIO_378	AJ39	NC
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NC	K38	DFTIO_286	DFTIO_382	AL39	NC
NC	N40	DFTIO_287	DFTIO_383	AJ38	NC

HBM_DAP

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CRITICAL

NC	AJ27	HBMA_DAP_0	HBMB_DAP_0	AL37	NC
NC	AK26	HBMA_DAP_1	HBMB_DAP_1	AJ36	NC
NC	AR27	HBMA_DAP_2	HBMB_DAP_2	AP36	NC
NC	AM27	HBMA_DAP_3	HBMB_DAP_3	AM36	NC
NC	AM26	HBMA_DAP_4	HBMB_DAP_4	AM35	NC
NC	AL27	HBMA_DAP_5	HBMB_DAP_5	AP37	NC
NC	AJ26	HBMA_DAP_6	HBMB_DAP_6	AN35	NC
NC	AJ21	HBMA_DAP_7	HBMB_DAP_7	AL36	NC
NC	AJ24	HBMA_DAP_8	HBMB_DAP_8	AT35	NC
NC	AK25	HBMA_DAP_9	HBMB_DAP_9	AR35	NC
NC	AN26	HBMA_DAP_10	HBMB_DAP_10	AK35	NC
NC	AL22	HBMA_DAP_11	HBMB_DAP_11	AJ35	NC
NC	AJ20	HBMA_DAP_12	HBMB_DAP_12	AU34	NC
NC	AL21	HBMA_DAP_13	HBMB_DAP_13	AM35	NC
NC	AK22	HBMA_DAP_14	HBMB_DAP_14	AK34	NC
NC	AN22	HBMA_DAP_15	HBMB_DAP_15	AV35	NC
NC	AL25	HBMA_DAP_16	HBMB_DAP_16	AN34	NC
NC	AJ23	HBMA_DAP_17	HBMB_DAP_17	AL34	NC
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NC	AK23	HBMA_DAP_19	HBMB_DAP_19	AY33	NC
NC	AL24	HBMA_DAP_20	HBMB_DAP_20	AW34	NC
NC	AK20	HBMA_DAP_21	HBMB_DAP_21	AL33	NC
NC	AM21	HBMA_DAP_22	HBMB_DAP_22	AP34	NC
NC	AK19	HBMA_DAP_23	HBMB_DAP_23	AM33	NC
NC	AT26	HBMA_DAP_24	HBMB_DAP_24	AJ33	NC
NC	AR26	HBMA_DAP_25	HBMB_DAP_25	AU33	NC
NC	AL18	HBMA_DAP_26	HBMB_DAP_26	AT32	NC
NC	AM20	HBMA_DAP_27	HBMB_DAP_27	AM32	NC
NC	AJ18	HBMA_DAP_28	HBMB_DAP_28	AR33	NC
NC	AM24	HBMA_DAP_29	HBMB_DAP_29	AW32	NC
NC	AR24	HBMA_DAP_30	HBMB_DAP_30	AT32	NC
NC	AR20	HBMA_DAP_31	HBMB_DAP_31	AK32	NC
NC	AJ17	HBMA_DAP_32	HBMB_DAP_32	AR32	NC
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NC	AN20	HBMA_DAP_34	HBMB_DAP_34	AV32	NC
NC	AM23	HBMA_DAP_35	HBMB_DAP_35	AW31	NC
NC	AR23	HBMA_DAP_36	HBMB_DAP_36	AU31	NC
NC	AT23	HBMA_DAP_37	HBMB_DAP_37	AP31	NC
NC	AK17	HBMA_DAP_38	HBMB_DAP_38	AN31	NC
NC	AM17	HBMA_DAP_39	HBMB_DAP_39	AL31	NC
NC	AM18	HBMA_DAP_40	HBMB_DAP_40	AV30	NC
NC	AL19	HBMA_DAP_41	HBMB_DAP_41	AJ30	NC
NC	AN23	HBMA_DAP_42	HBMB_DAP_42	AR30	NC
NC	AR17	HBMA_DAP_43	HBMB_DAP_43	AT31	NC
NC	AR21	HBMA_DAP_44	HBMB_DAP_44	AK31	NC
NC	AT22	HBMA_DAP_45	HBMB_DAP_45	AM30	NC
NC	AK15	HBMA_DAP_46	HBMB_DAP_46	AU30	NC
NC	AT20	HBMA_DAP_47	HBMB_DAP_47	AJ29	NC
NC	AT19	HBMA_DAP_48	HBMB_DAP_48	AM29	NC
NC	AJ15	HBMA_DAP_49	HBMB_DAP_49	AR29	NC
NC	AN19	HBMA_DAP_50	HBMB_DAP_50	AL30	NC
NC	AN17	HBMA_DAP_51	HBMB_DAP_51	AV29	NC
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NC	AP14	HBMA_DAP_53	HBMB_DAP_53	AN29	NC
NC	AR18	HBMA_DAP_54	HBMB_DAP_54	AU28	NC
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NC	AP15	HBMA_DAP_56	HBMB_DAP_56	AU28	NC
NC	AR14	HBMA_DAP_57	HBMB_DAP_57	AT28	NC
NC	AL14	HBMA_DAP_58	HBMB_DAP_58	AL28	NC
NC	AK14	HBMA_DAP_59	HBMB_DAP_59	AK28	NC

NOTE:

AJ18 AND AR33 ARE NC FOR HBM2
HBM2 DOES NOT NEED THE CONNECTION
TO GND FOR NORMAL OPERATION
HBM2 USES A MRS SETTING TO LOCK OUT
THE DIRECT ACCESS (DA) BUS

OMIT_TABLE

UA000
VEGA10-T7
TBD
BGA
SYM 8 OF 16
CRITICAL

NC	P8	RSVD	RSVD	AV45	NC
NC	N7	RSVD	RSVD	AW1	NC
NC	AD37	RSVD	RSVD	AW2	NC
NC	AD38	RSVD	RSVD	AW7	NC
NC	AD40	RSVD	RSVD	AW10	NC
NC	AD44	RSVD	RSVD	AW12	NC
NC	AE38	RSVD	RSVD	AW13	NC
NC	AE39	RSVD	RSVD	AW15	NC
NC	AE40	RSVD	RSVD	AW16	NC
NC	AE42	RSVD	RSVD	AW23	NC
NC	AE44	RSVD	RSVD	AW24	NC
NC	AF37	RSVD	RSVD	AW26	NC
NC	AF38	RSVD	RSVD	AW27	NC
NC	D12	RSVD	RSVD	AW29	NC
NC	C12	RSVD	RSVD	AW38	NC
NC	B12	RSVD	RSVD	AY23	NC
NC	AP38	RSVD	RSVD	AY30	NC
NC	AR8	RSVD	RSVD	AY31	NC
NC	AR10	RSVD	RSVD	AY33	NC
NC	AR11	RSVD	RSVD	AY34	NC
NC	AR38	RSVD	RSVD	AY36	NC
NC	AT9	RSVD	RSVD	AY37	NC
NC	AT10	RSVD	RSVD	BA4	NC
NC	AU1	RSVD	RSVD	BA23	NC
NC	AU2	RSVD	RSVD	BA24	NC
NC	AU3	RSVD	RSVD	BA25	NC
NC	AU4	RSVD	RSVD	BA26	NC
NC	AU5	RSVD	RSVD	BA30	NC
NC	AU6	RSVD	RSVD	BA32	NC
NC	AU7	RSVD	RSVD	BA35	NC
NC	AU8	RSVD	RSVD	BA36	NC
NC	AU9	RSVD	RSVD	BA38	NC
NC	AU11	RSVD	RSVD	BA39	NC
NC	AU15	RSVD	RSVD	BB24	NC
NC	AU25	RSVD	RSVD	BB25	NC
NC	AU27	RSVD	RSVD	BB26	NC
NC	AV1	RSVD	RSVD	BB27	NC
NC	AV2	RSVD	RSVD	BB31	NC
NC	AV3	RSVD	RSVD	BB32	NC
NC	AV8	RSVD	RSVD	BB37	NC
NC	AV12	RSVD	RSVD	BB38	NC
NC	AV13	RSVD	RSVD	BB40	NC
NC	AV18	RSVD	RSVD	BB41	NC
NC	AV19	RSVD	RSVD	BB43	NC
NC	AV20	RSVD	RSVD	BC3	NC
NC	AV21	RSVD	RSVD	BC23	NC
NC	AV22	RSVD	RSVD	BC24	NC
NC	AV23	RSVD	RSVD	BC26	NC
NC	AV36	RSVD	RSVD	BC27	NC
NC	AV38	RSVD	RSVD	BC28	NC
NC	AV39	RSVD	RSVD	BC31	NC

OMIT_TABLE

UA000
VEGA10-T7
TBD
BGA
SYM 9 OF 16
CRITICAL

NC	BC33	RSVD	RSVD	AG42	NC
NC	BC36	RSVD	RSVD	AG43	NC
NC	BC37	RSVD	RSVD	AG44	NC
NC	BC39	RSVD	RSVD	AH38	NC
NC	BC40	RSVD	RSVD	AH40	NC
NC	BD4	RSVD	RSVD	AH41	NC
NC	BD22	RSVD	RSVD	AH42	NC
NC	BD24	RSVD	RSVD	AH44	NC
NC	BD27	RSVD	RSVD	AJ4	NC
NC	BD28	RSVD	RSVD	AJ5	NC
NC	BD32	RSVD	RSVD	AJ8	NC
NC	BD36	RSVD	RSVD	AJ10	NC
NC	BD38	RSVD	RSVD	AJ14	NC
NC	BD39	RSVD	RSVD	AJ42	NC
NC	BD41	RSVD	RSVD	AJ44	NC
NC	BD42	RSVD	RSVD	AK7	NC
NC	L4	RSVD	RSVD	AK10	NC
NC	BE24	RSVD	RSVD	AK38	NC
NC	BE32	RSVD	RSVD	AK40	NC
NC	BE38	RSVD	RSVD	AL6	NC
NC	BE40	RSVD	RSVD	AL8	NC
NC	N11	RSVD	RSVD	AL11	NC
NC	P10	RSVD	RSVD	AL15	NC
NC	R10	RSVD	RSVD	AL38	NC
NC	R11	RSVD	RSVD	AM14	NC
NC	T10	RSVD	RSVD	AM37	NC
NC	U4	RSVD	RSVD	AM38	NC
NC	U5	RSVD	RSVD	AN1	NC
NC	U10	RSVD	RSVD	AN2	NC
NC	U11	RSVD	RSVD	AN3	NC
NC	W10	RSVD	RSVD	AN4	NC
NC	W11	RSVD	RSVD	AN5	NC
NC	Y9	RSVD	RSVD	AN6	NC
NC	AA4	RSVD	RSVD	AN8	NC
NC	AA7	RSVD	RSVD	AN11	NC
NC	AA10	RSVD	RSVD	AN12	NC
NC	AA11	RSVD	RSVD	AN14	NC
NC	AB10	RSVD	RSVD	AN38	NC
NC	AC10	RSVD	RSVD	AP4	NC
NC	AC11	RSVD	RSVD	AP5	NC
NC	AD10	RSVD	RSVD	AP6	NC
NC	AE11	RSVD	RSVD	AP9	NC
NC	AE43	RSVD	RSVD	AP10	NC
NC	AF10	RSVD	RSVD	AR37	NC
NC	AF40	RSVD	RSVD	AT36	NC
NC	AF41	RSVD	RSVD	AW39	NC
NC	AF42	RSVD	RSVD	BD35	NC
NC	AF44	RSVD	RSVD	BE35	NC
NC	AG38	RSVD	RSVD	BE36	NC
NC	AG39	RSVD	RSVD	B1	NC
NC	AG40	RSVD			

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SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE
GPU DA, DFTIO

Apple Inc.

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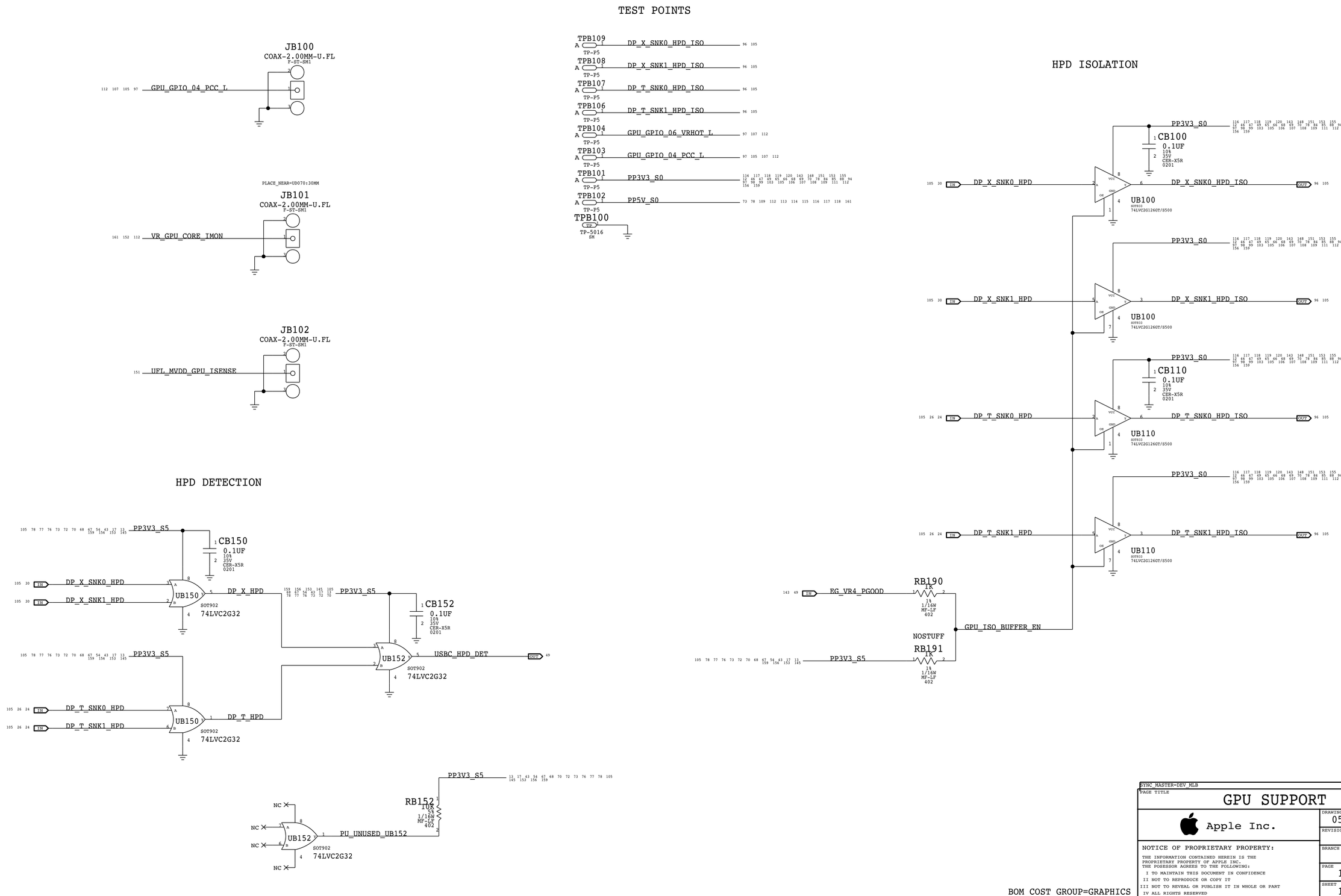

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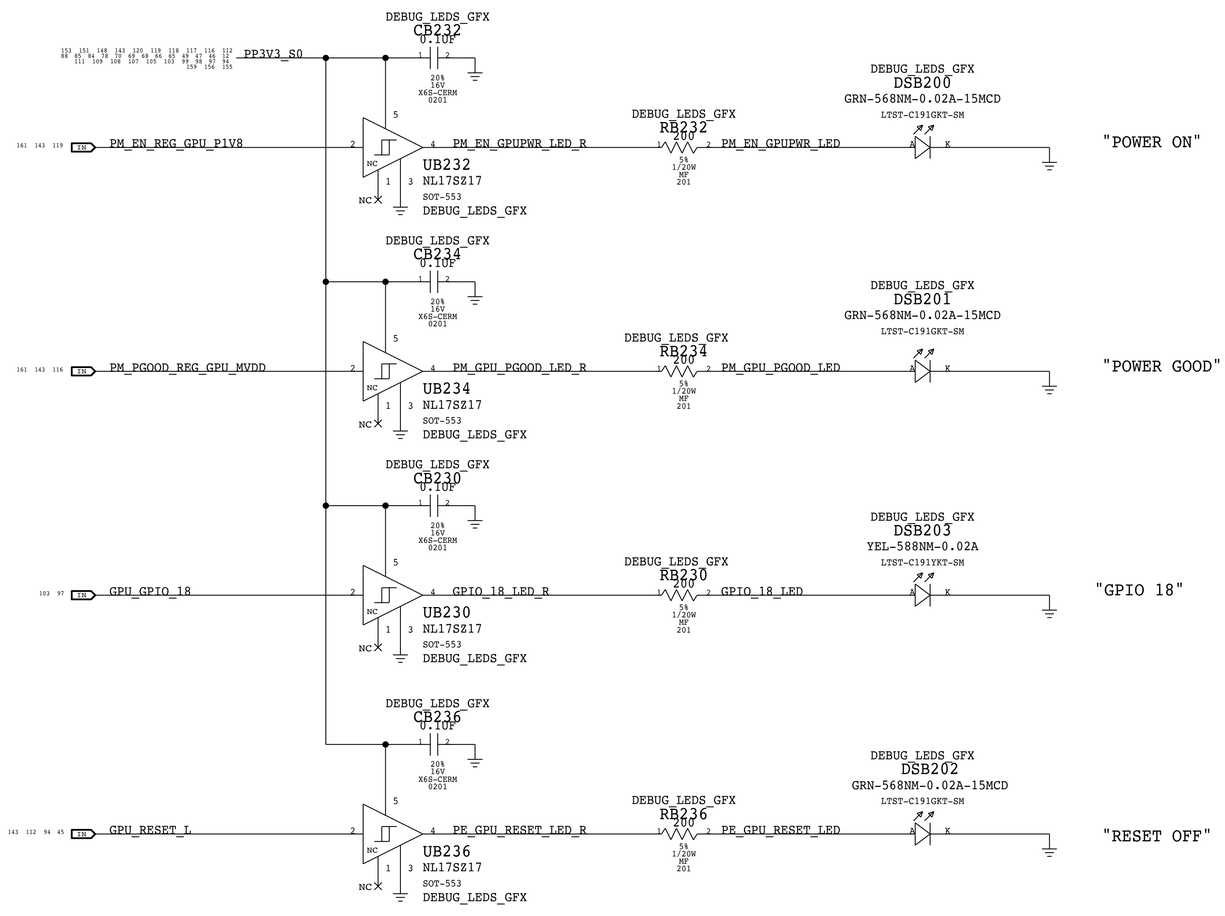
GPU DEBUG LEDS



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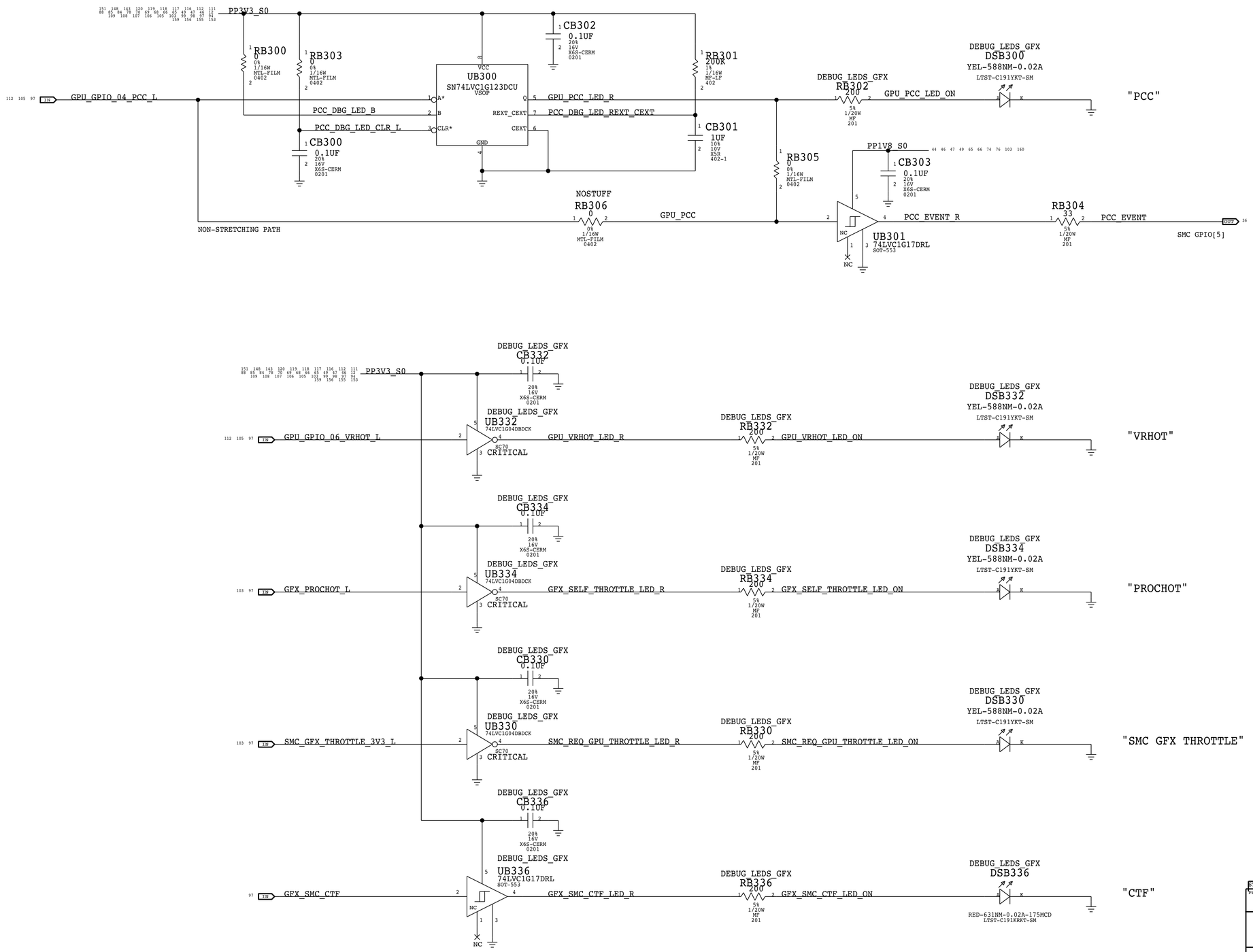
GPU POWER MANAGEMENT LEDS



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PAGE TITLE: GPU POWER MGMT LEDS

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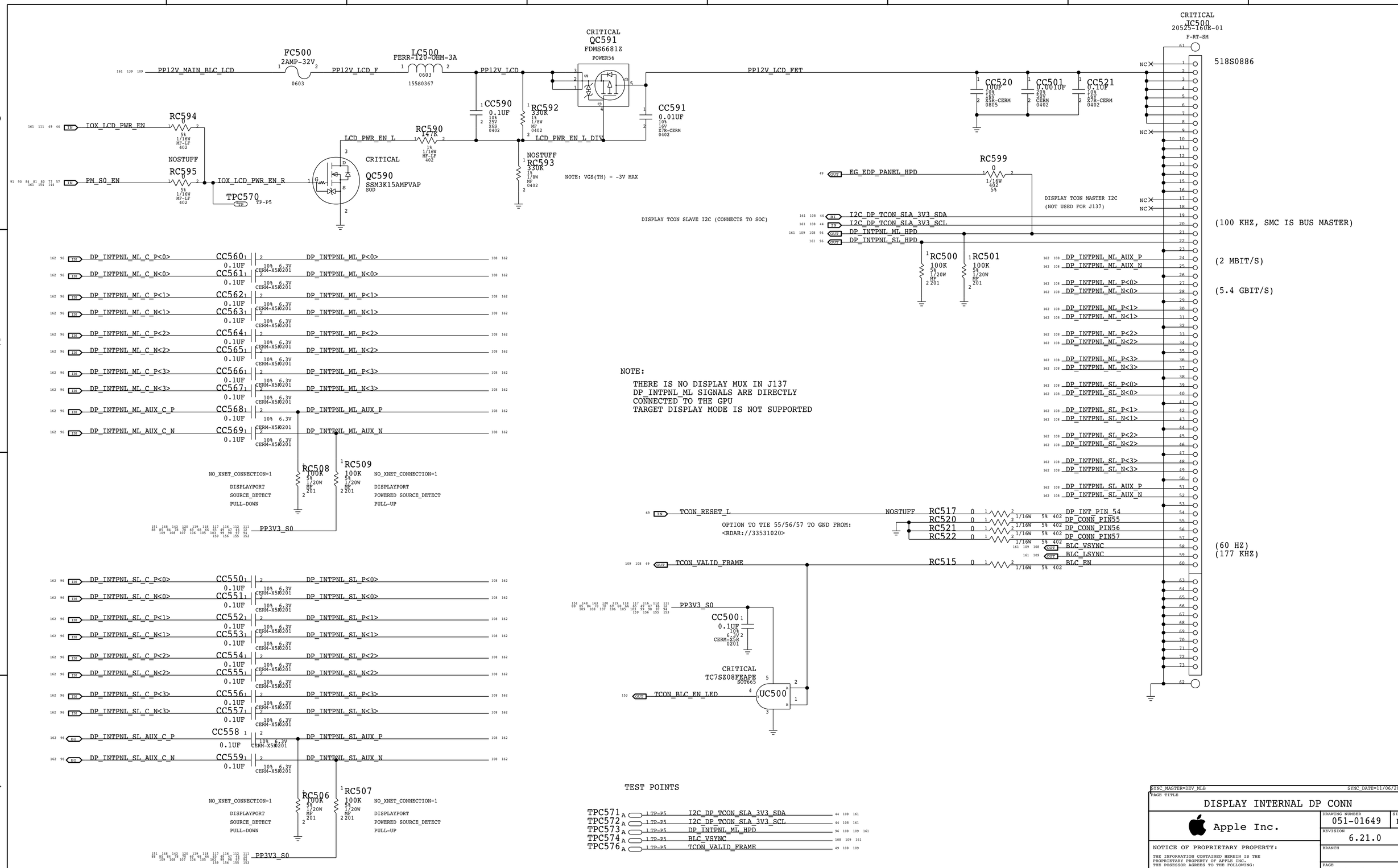

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DISPLAY INTERNAL DP CONN

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NOTE:
POWER RAILS REQUIRED BY BACKLIGHT DRIVER
PP12V_S0_BKLT
PP5V_S0_BKLT
PP3V3_S0_BKLT

PP12V_BKLT_PWR — DC603 SBR130S3 (SOD-323) — CC640 1000PF 5% 25V CERM 0402 — CC641 1000PF 5% 25V CERM 0402 — CRITICAL CC602 10UF 10% 25V X7R-CERM 1206-4 — CRITICAL CC603 10UF 10% 25V X7R-CERM 1206-4 — CRITICAL CC614 100UF 20% 35V ELEC 6.3X11-TH

PLACE CC614 NEAR HIGHER FREQUENCY CAPS

CRITICAL LC601 33UH-20%-10A-0.0355OHM (PIMB177T-SM 152S1668) — PPBKLT_PHASE — NOSTUFF RC623 2.7 5% 1/10W MF-LF 603 — BKLT_SNUBBER — NOSTUFF CC613 100PF 5% 100V C0G-CERM 0603

CRITICAL DC601 VS-8TQ100SPBF (TO263) — NC

PPBKLT_BOOST — CC619 100PF 5% 100V C0G-CERM 0603 — CC606 2.2UF 10% 100V X7S-CERM 1206 — CC690 1UF 10% 100V X7S-CERM 0805 — CC691 1UF 10% 100V X7S-CERM 0805 — CC608 2.2UF 10% 100V X7S-CERM 1206 — CRITICAL 126-00013 CC609 18UF 20% 100V AL-EL 10X12.5-TH — CRITICAL 126-00013 CC618 18UF 20% 100V AL-EL 10X12.5-TH — CC620 100PF 5% 100V C0G-CERM 0603

NOTE:
QC620 IS APN 376S1183 WITH PWRPK OPTION

BLC I2C ADDR
WRITE: 0X58
READ: 0X59

TPC670 TP-P5 I2C_BKLT_3V3_SDA
TPC671 TP-P5 I2C_BKLT_3V3_SCL
TPC672 TP-P5 BKLT_SHUTDOWN

PP5V_S0_BKLT_VDDA
PP5V_S0_BKLT_VDDD
PP3V3_S0_BKLT_VDDIO
PP12V_BKLT_FILT

BKLT_GATE_R — RC619 30.1 1% 1/8W MF-LF 805 — QC620 FDMC86102LZ MLP-3.3X3.3-PWRPK-12128-COMBO CRITICAL — BKLT_SNSP_R — RC602 0.03 1% 2W MF 2512-LF — BKLT_SNSN_R

RC614 20 5% 1/8W MF-LF 805 — BKLT_BST_FB_R — RC613 887K 1% 1/16W MF-LF 402 — RC612 330K 1% 1/8W MF 0402 — CC610 1000PF 10% 100V X7R-CERM 0603 — XWC609 (SHORT-1206) — BKLT_SNSN_R — RC604 887K 1% 1/16W MF-LF 402 — RC603 330K 1% 1/8W MF 0402 — CC611 1000PF 10% 100V X7R-CERM 0603

BKLT_PLL_FILT — RC611 270K 5% 1/16W MF-LF 402 — NOSTUFF DC602 (SOD-523) BAT54XV2T1 — CC615 330PF 5% 50V NPO-C0G-CERM 0402 — BKLT_PLL_FILT_R — CC616 4700PF 10% 50V X7R-CERM 0402 — BKLT_GNDA

UC600 LP8565A13RWC WQFN-THICKSTNCL CRITICAL 353S00079

Pin	Net	Dir
36	BKLT_GATE	
34	BKLT_SNSP	
33	BKLT_SNSN	
31	BKLT_BST_FB	
30	BKLT_BST_SHORT_FB	
14	BKLT_VSEN1	IN
15	BKLT_GD1	OUT
16	BKLT_ISEN1_Q	IN
17	BKLT_VSEN2	IN
18	BKLT_GD2	OUT
19	BKLT_ISEN2_Q	IN
20	BKLT_VSEN3	IN
21	BKLT_GD3	OUT
22	BKLT_ISEN3_Q	IN
24	BKLT_VSEN4	IN
25	BKLT_GD4	OUT
26	BKLT_ISEN4_Q	IN
29	BKLT_VSEN5	IN
27	BKLT_GD5	OUT
28	BKLT_ISEN5_Q	IN
44	BKLT_VSEN6	IN
45	BKLT_GD6	OUT
46	BKLT_ISEN6_Q	IN
47	BKLT_VSEN7	IN
48	BKLT_GD7	OUT
49	BKLT_ISEN7_Q	IN
51	BKLT_VSEN8	IN
52	BKLT_GD8	OUT
53	BKLT_ISEN8_Q	IN
54	BKLT_VSEN9	IN
55	BKLT_GD9	OUT
56	BKLT_ISEN9_Q	IN
39	SD	
40	UVLO_OVP	
9	SDA	IN
8	SCL	IN
2	HPD	
3	BL_EN	
12	INT	
10	BRT_SYNC	
7	PWM	
11	SYNC	
43	FILTER	
32	ANALOG_TEST	
1	DIGITAL_TEST	
38	VING	
37	BST_GD_RAIL	
13	NC	
4	VDDIO	
5	VDDD	
42	VDDA	
41	GNDA	
6	GNDD	
23	LED_GND1	
50	LED_GND2	
35	GND_BST_GD	
57	THRM PAD	

(GATE DR VOLTAGE)

BKLT_GD_RAIL — CC645 0.1UF 10% 25V X6S 0402 — CC617 0.1UF 10% 25V X6S 0402 — NOSTUFF — BKLT_GND_BST_GD

RC640 0 5% 1/16W MF-LF 402 — NOSTUFF — BKLT_GD_RAIL

PP12V_BKLT_PWR — RC638 1 5% 1/16W MF-LF 402 — PP12V_BKLT_PWR_R

MIN_NECK_WIDTH=0.1020
MIN_LINE_WIDTH=0.2000

CC642 1UF 10% 25V X7R 0603 — CC643 0.01UF 10% 16V X7R-CERM 0402 — CC644 0.1UF 10% 16V X7R-CERM 0402 — BKLT_GND_BST_GD

XWC605 (SM) — BKLT_GNDA
XWC606 (SM) — BKLT_GNDD
XWC608 (SM) — BKLT_GND_BST_GD

PPBKLT_BOOST — CC621 470PF 5% 100V CER-C0G 0603 — CC622 470PF 5% 100V CER-C0G 0603 — CC623 470PF 5% 100V CER-C0G 0603 — CC624 470PF 5% 100V CER-C0G 0603 — CC625 470PF 5% 100V CER-C0G 0603 — CC626 470PF 5% 100V CER-C0G 0603 — CC627 470PF 5% 100V CER-C0G 0603 — CC628 470PF 5% 100V CER-C0G 0603 — CC629 470PF 5% 100V CER-C0G 0603

LED_RETURN_1_FB
LED_RETURN_2_FB
LED_RETURN_3_FB
LED_RETURN_4_FB
LED_RETURN_5_FB
LED_RETURN_6_FB
LED_RETURN_7_FB
LED_RETURN_8_FB
LED_RETURN_9_FB

BKLT_SNSP — RC625 0 5% 1/16W MF-LF 402 — BKLT_SNSP_R
CC630 1000PF 10% 100V X7R 603 NOSTUFF
BKLT_SNSN — RC691 0 5% 1/16W MF-LF 402 — BKLT_SNSN_R

PP5V_S0 — RC637 1 5% 1/16W MF-LF 402 — PP5V_S0_BKLT_VDDA — CC637 22UF 20% 10V X5R-CERM 0603 — CC638 0.01UF 10% 16V X7R-CERM 0402 — CC639 0.1UF 10% 16V X7R-CERM 0402 — BKLT_GNDA

RC631 1 5% 1/16W MF-LF 402 — PP5V_S0_BKLT_VDDD — CC631 22UF 20% 10V X5R-CERM 0603 — CC632 0.01UF 10% 16V X7R-CERM 0402 — CC633 0.1UF 10% 16V X7R-CERM 0402 — BKLT_GNDD

PP3V3_S0 — RC634 1 5% 1/16W MF-LF 402 — PP3V3_S0_BKLT_VDDIO — CC634 1UF 10% 25V X7R 0603 — CC635 0.01UF 10% 16V X7R-CERM 0402 — CC636 0.1UF 10% 16V X7R-CERM 0402 — BKLT_GNDD

BLC_VSYNC_R — NOSTUFF RC670 0 5% 1/16W MF-LF 402 — BLC_VSYNC (IN)
NOSTUFF RC639 0 5% 1/16W MF-LF 402
BLC_LSYNC_R — RC671 0 5% 1/16W MF-LF 402 — BLC_LSYNC (IN)

RC606 200K 1% — BKLT_HPD
RC605 100K 5% — BKLT_BL_EN
RC607 10K 5% — BKLT_PWM_IN
RC621 10K 5% — BLC_VSYNC_R
RC620 10K 5% — BLC_LSYNC_R
RC681 10K 5% — BKLT_DIG_TEST
BKLT_GNDD

RC680 10K 5% — BKLT_ANG_TEST
RC682 10K 5% — BKLT_NC_TEST
BKLT_GNDA

PP3V3_S0 — RC624 4.7K 5% — RC672 0 5% 1/16W MF-LF 402 — BKLT_FAULT_INT_R_L — BKLT_FAULT_INT_L (OUT) (TO SMC)

FC600 6AMP-32V (0603-1) — PP12V_MAIN_BLC_LCD — PP12V_BKLT_FUSED — CRITICAL RC632 0.005 1% 1/8W MF 1206-1 — PP12V_BKLT_SNS — CRITICAL LC600 16U-OHM-6A (1206) — PP12V_BKLT_FILT — CRITICAL 376S1067 QC619 FDMS6681Z POWER56 — PP12V_BKLT_PWR

NOSTUFF CC671 0.1UF 10% 25V X6S 0402 — NOSTUFF RC601 330K 1% 1/8W MF 0402 — BKLT_EN_DIV — CC601 0.01UF 10% 16V X7R-CERM 0402

NOSTUFF RC633 147K 1% 1/16W MF-LF 402 — BKLT_EN_L — CRITICAL NOSTUFF QC601 SSM3K15AMFVAP (SOD) — RC622 0 5% 1/16W MF-LF 402 — BKLT_SHUTDOWN

TCON_VALID_FRAME (IN)

(OPTION TO CONTROL BLC BY SMC)

BKLT_HPD — RC673 0 5% 1/16W MF-LF 402 — NOSTUFF — DP_INTPNL_ML_HPD (IN)
RC674 0 5% 1/16W MF-LF 402 — IOX_BLC_BOOST_EN (IN)
BKLT_BL_EN — RC675 0 5% 1/16W MF-LF 402 — NOSTUFF — TCON_VALID_FRAME (IN)
RC676 0 5% 1/16W MF-LF 402 — IOX_LCD_BKLT_EN (IN)

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE: DISPLAY BACKLIGHT DRIVER

Apple Inc.

DRAWING NUMBER: 051-01649 SIZE: D
REVISION: 6.21.0
BRANCH:
PAGE: 126 OF 255
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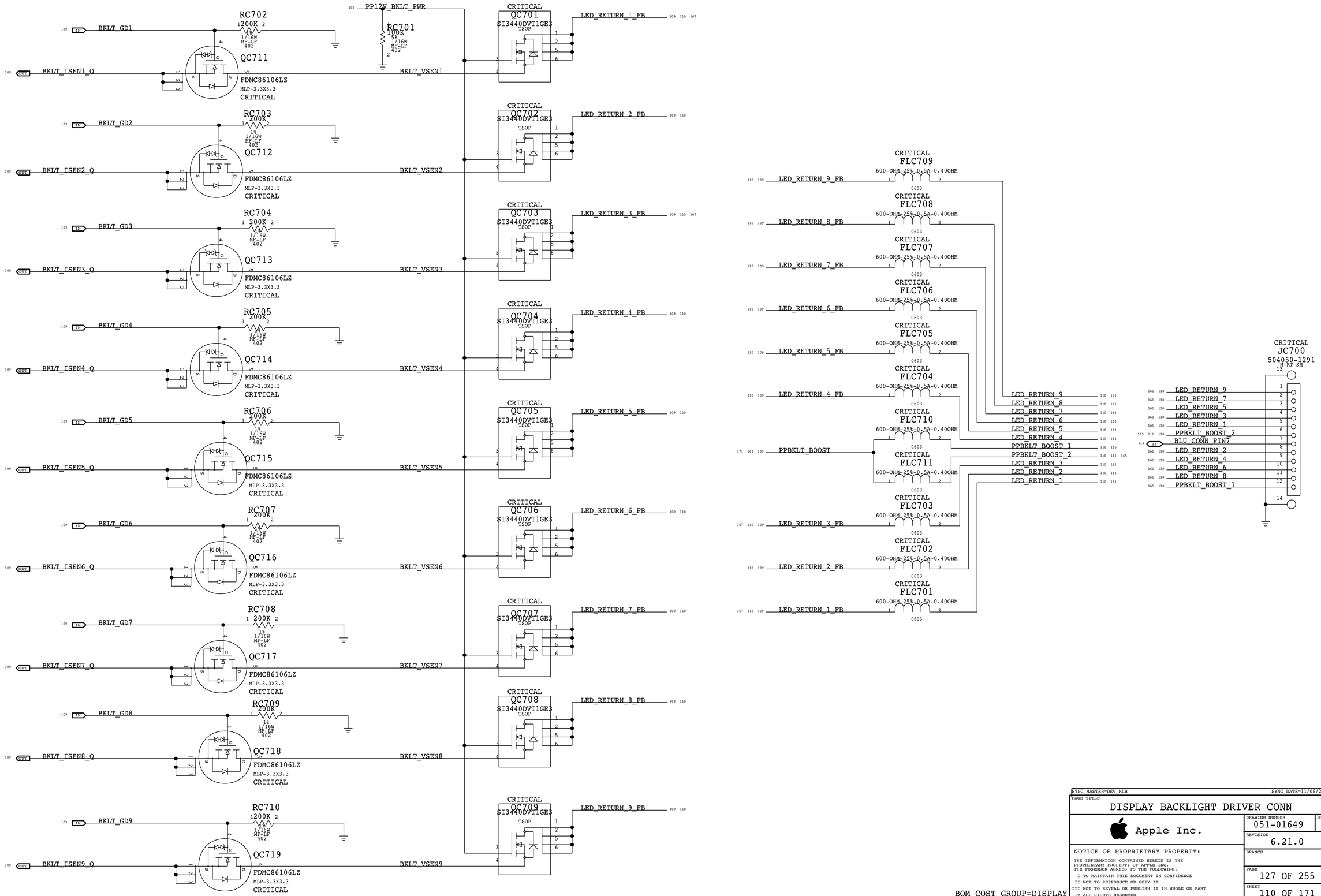

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PAGE TITLE

DISPLAY BACKLIGHT DRIVER CONN

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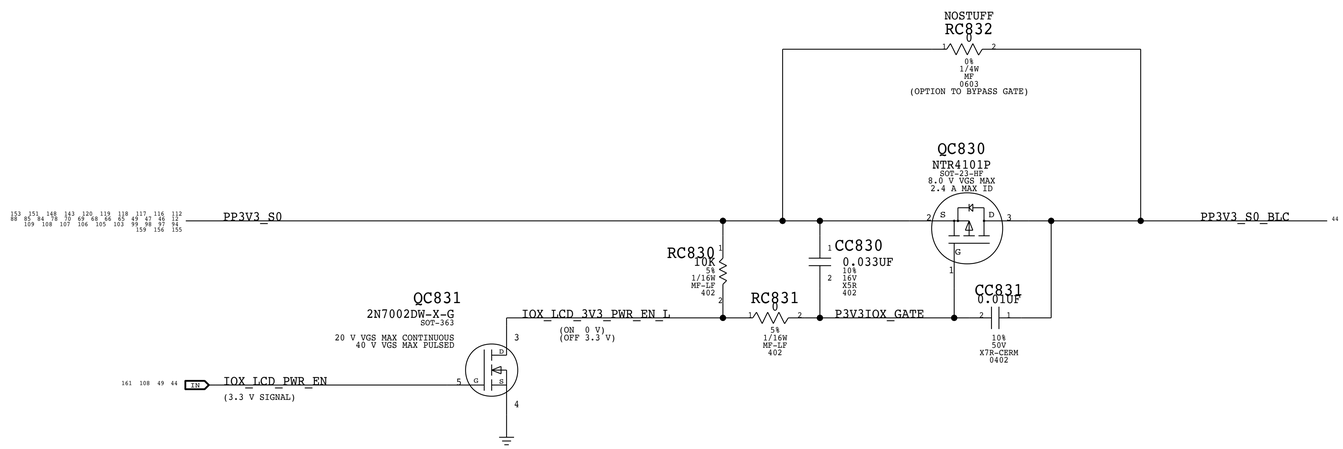
DISPLAY 3V3 FET

GATED POWER BECAUSE THE DISPLAY AND 3V3 S0 MAY NOT ALWAYS BE ON TOGETHER



OPTION TO TIE BLUE CONN PIN 7 TO PIN 6 FROM:
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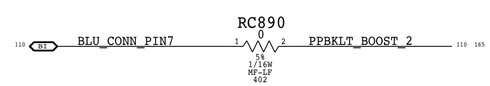

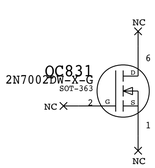

BOM_COST_GROUP=DISPLAY

PAGE TITLE	DISPLAY BACKLIGHT SUPPORT
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	REVISION 6.21.0
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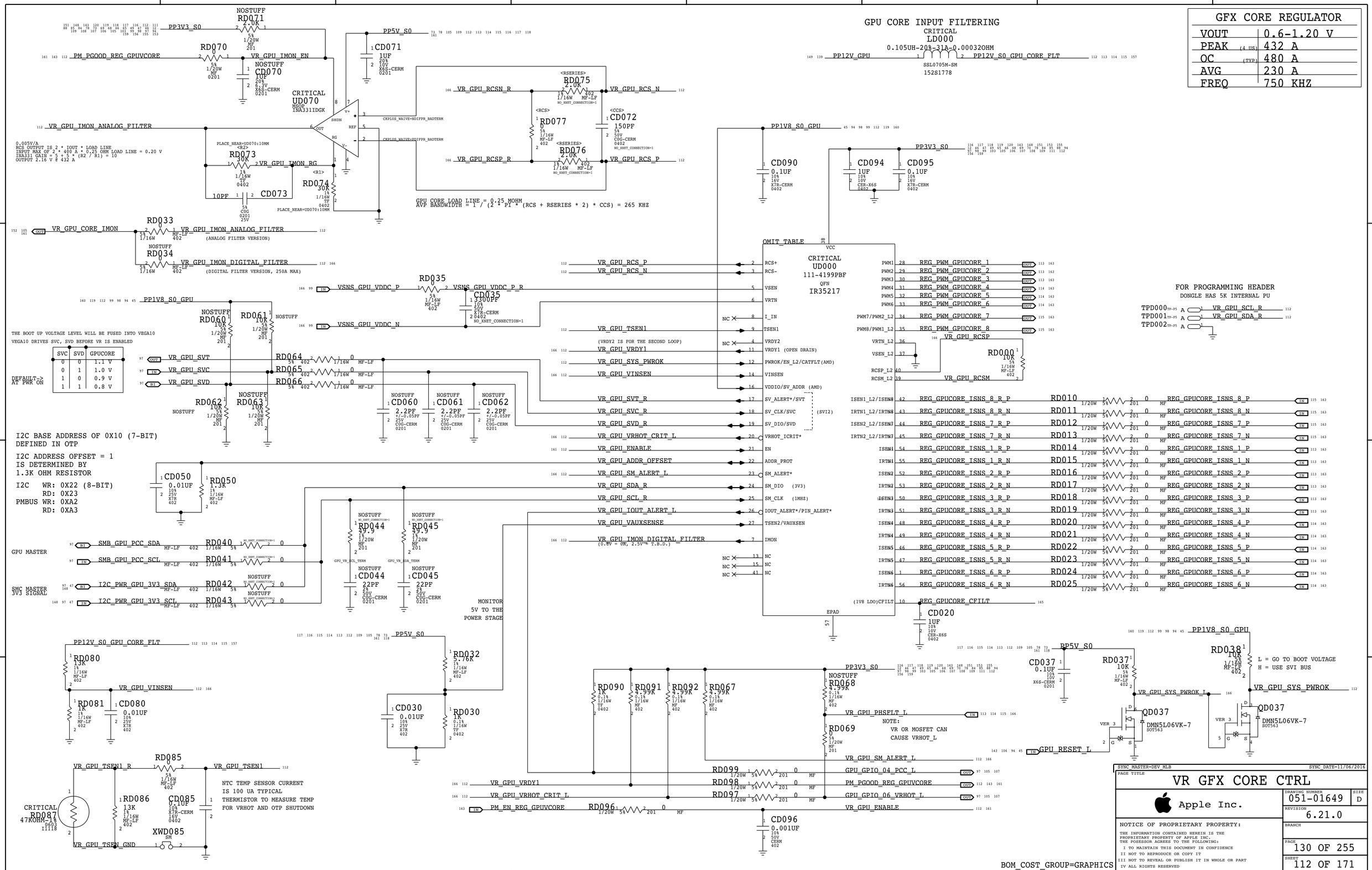
GFX CORE REGULATOR
VOUT 0.6-1.20 V
PEAK (4 US) 432 A
OC (TYP) 480 A
AVG 230 A
FREQ 750 KHZ
GPU CORE INPUT FILTERING
CRITICAL
LD000
0.105UH-20%-31A-0.00032OHM
SSL0705M-SM
152S1778
PP12V_GPU
PP12V_S0_GPU_CORE_FLT
CRITICAL
UD070
MSOP
INA331IDGK
0.005V/A
RCS OUTPUT IS 2 * IOUT * LOAD LINE
INPUT MAX OF 2 * 400 A * 0.25 OHM LOAD LINE = 0.20 V
INA331 GAIN = 5 + 5 * (R2 / R1) = 10
OUTPUT 2.16 V @ 432 A
GPU CORE LOAD LINE = 0.25 MOHM
AVP BANDWIDTH = 1 / (2 * PI * (RCS + RSERIES * 2) * CCS) = 265 KHZ
OMIT_TABLE
CRITICAL
UD000
111-4199PBF
QFN
IR35217
THE BOOT UP VOLTAGE LEVEL WILL BE FUSED INTO VEGA10
VEGA10 DRIVES SVC, SVD BEFORE VR IS ENABLED
SVC SVD GPUCORE
0 0 1.1 V
0 1 1.0 V
1 0 0.9 V
1 1 0.8 V
DEFAULT-> AT PWR ON
I2C BASE ADDRESS OF 0X10 (7-BIT)
DEFINED IN OTP
I2C ADDRESS OFFSET = 1
IS DETERMINED BY
1.3K OHM RESISTOR
I2C WR: 0X22 (8-BIT)
RD: 0X23
PMBUS WR: 0XA2
RD: 0XA3
GPU MASTER
SMC MASTER 3V3 SIGNAL
MONITOR 5V TO THE POWER STAGE
FOR PROGRAMMING HEADER
DONGLE HAS 5K INTERNAL PU
NOTE: VR OR MOSFET CAN CAUSE VRHOT_L
L = GO TO BOOT VOLTAGE
H = USE SVI BUS
NTC TEMP SENSOR CURRENT IS 100 UA TYPICAL
THERMISTOR TO MEASURE TEMP FOR VRHOT AND OTP SHUTDOWN
BOM_COST_GROUP=GRAPHICS
SYNC_MASTER=DEV_MLB
SYNC_DATE=11/06/2016
PAGE TITLE
VR GFX CORE CTRL
Apple Inc.
DRAWING NUMBER 051-01649
SIZE D
REVISION 6.21.0
BRANCH
PAGE 130 OF 255
SHEET 112 OF 171
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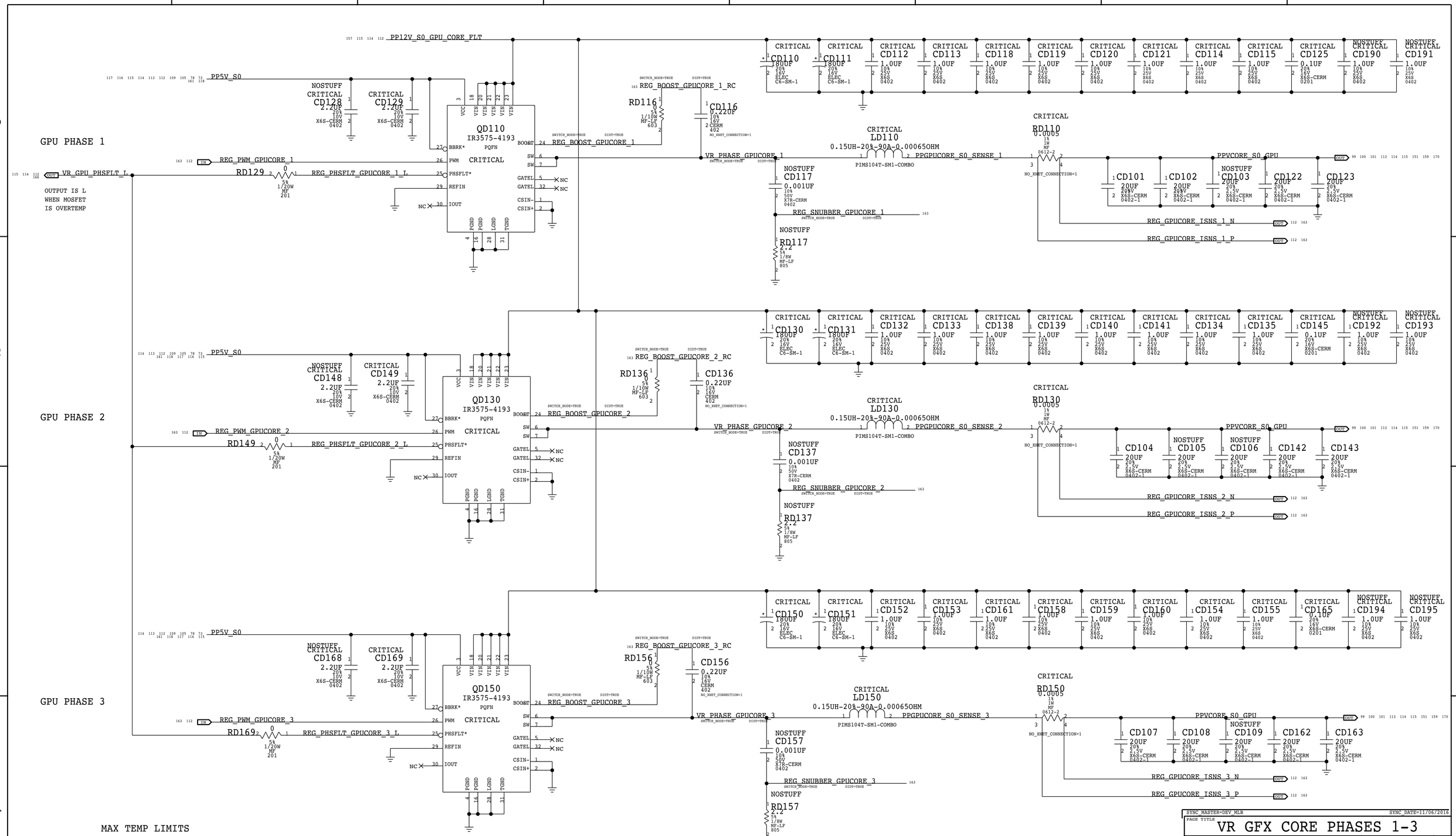

MAX TEMP LIMITS

IR3575M	125 C (TJ)	353S4458
470 UF	95 C	128S0381
0.15 UH	125 C	152S00302

BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE: VR GFX CORE PHASES 1-3

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DRAWING NUMBER: 051-01649 SIZE: D

REVISION: 6.21.0

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PAGE: 131 OF 255

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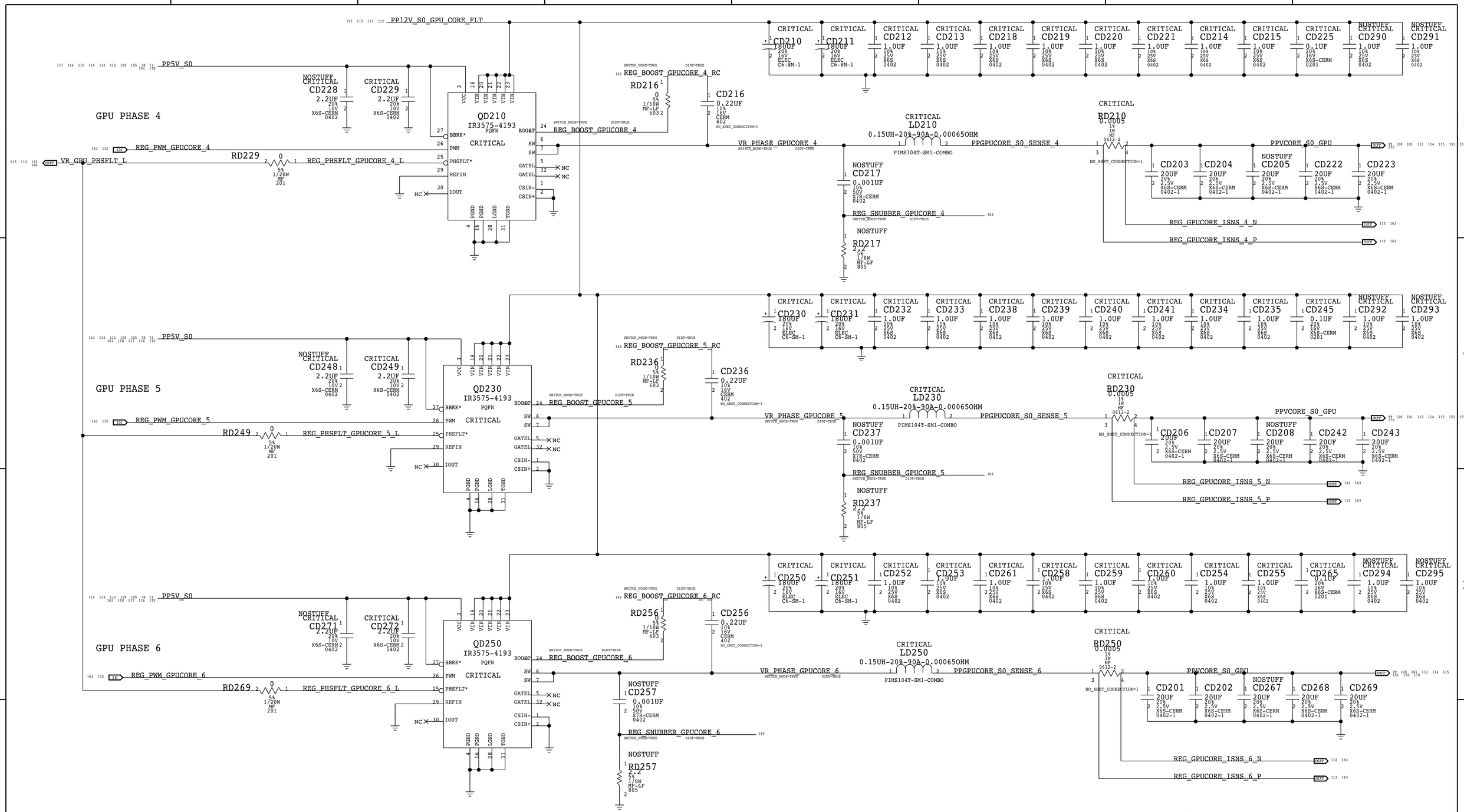

BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE
VR GFX CORE PHASES 4-6

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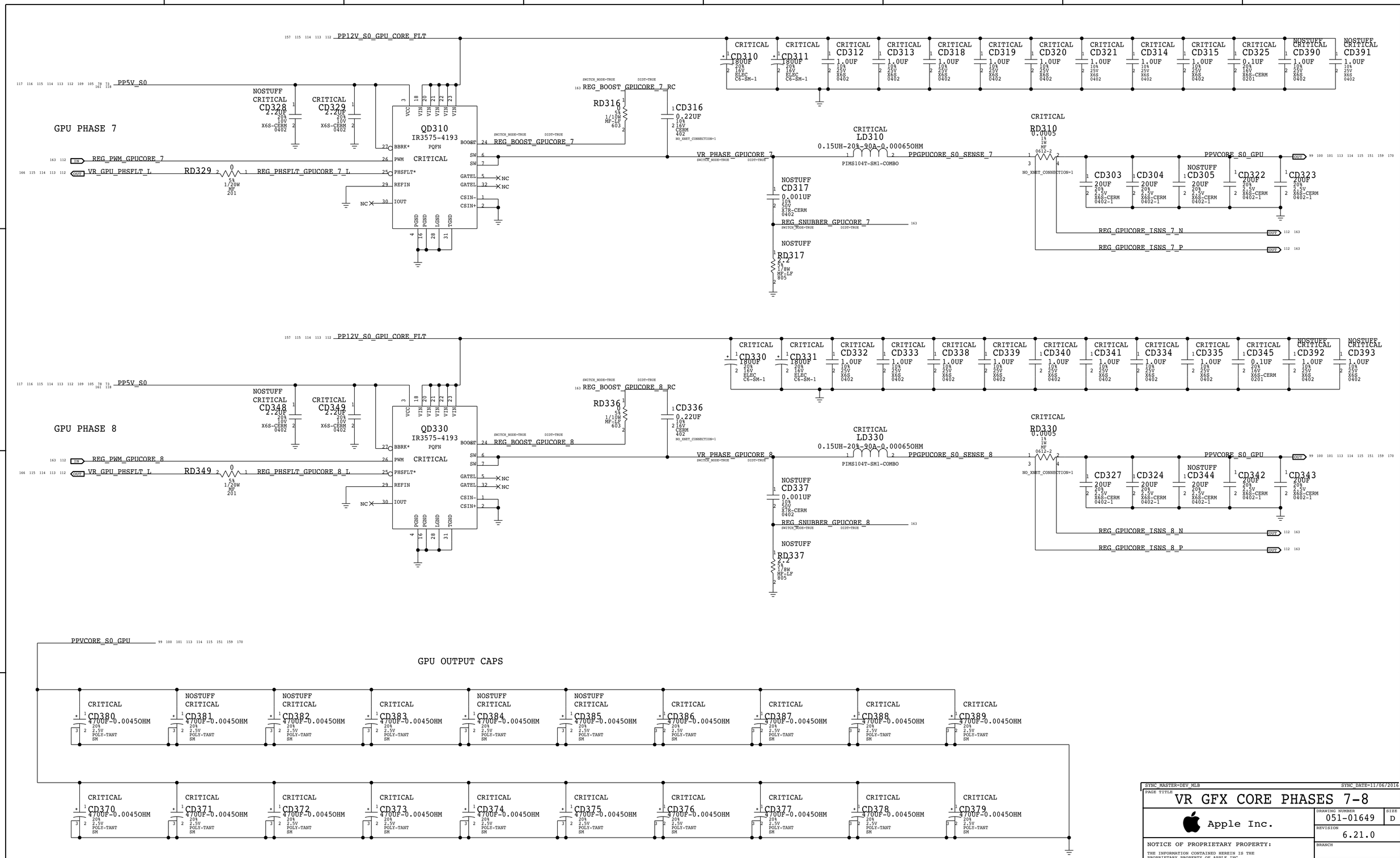

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE: VR GFX CORE PHASES 7-8

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DRAWING NUMBER: 051-01649 SIZE: D

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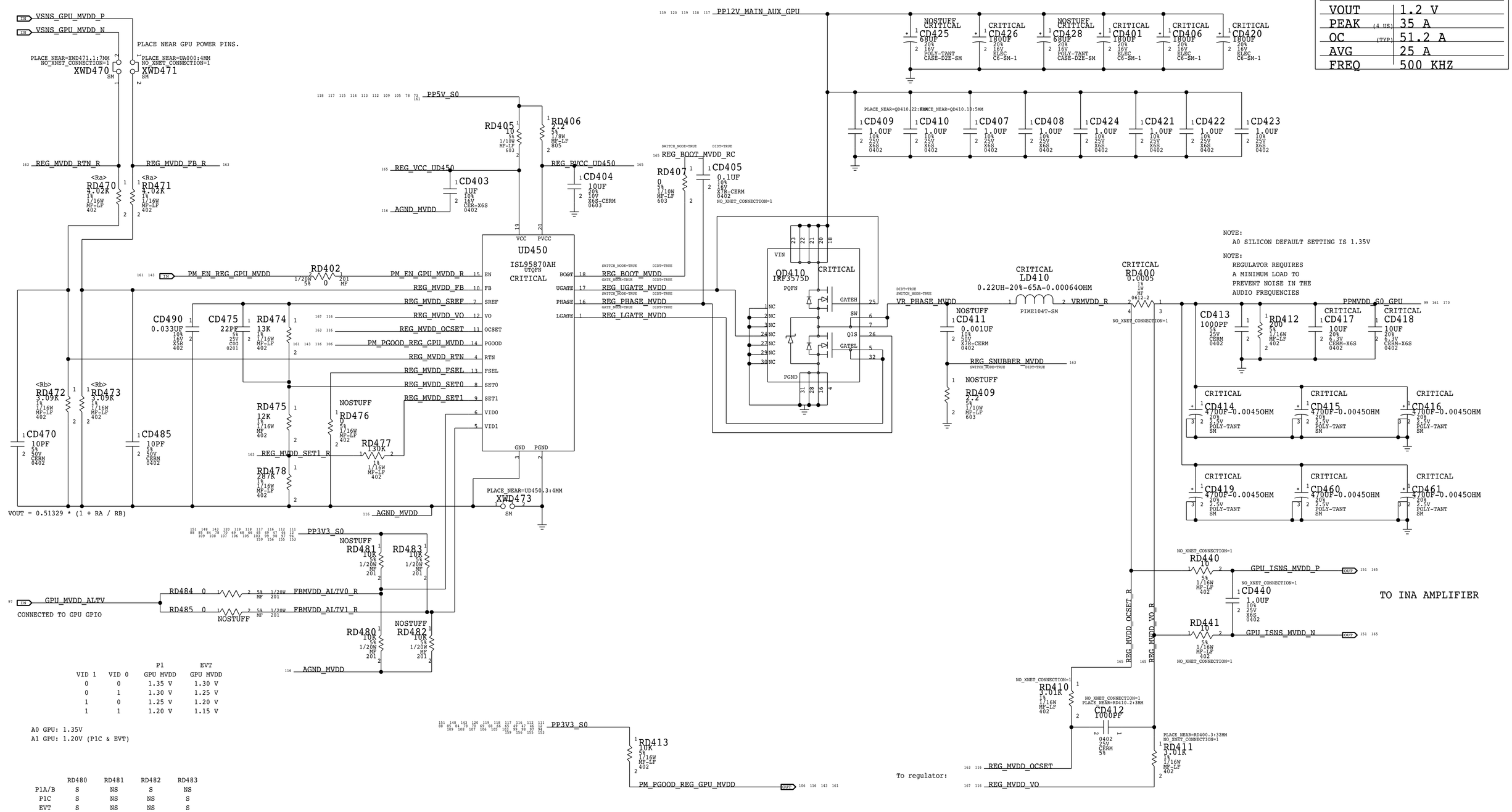
GFX MVDD REGULATOR	
VOUT	1.2 V
PEAK (4 US)	35 A
OC (TYP)	51.2 A
AVG	25 A
FREQ	500 KHZ



NOTE:
A0 SILICON DEFAULT SETTING IS 1.35V

NOTE:
REGULATOR REQUIRES
A MINIMUM LOAD TO
PREVENT NOISE IN THE
AUDIO FREQUENCIES

VID 1	VID 0	P1 GPU MVDD	EVT GPU MVDD
0	0	1.35 V	1.30 V
0	1	1.30 V	1.25 V
1	0	1.25 V	1.20 V
1	1	1.20 V	1.15 V

A0 GPU: 1.35V
A1 GPU: 1.20V (P1C & EVT)

	RD480	RD481	RD482	RD483
P1A/B	S	NS	S	NS
P1C	S	NS	NS	S
EVT	S	NS	NS	S

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PAGE TITLE
VR GFX MVDD

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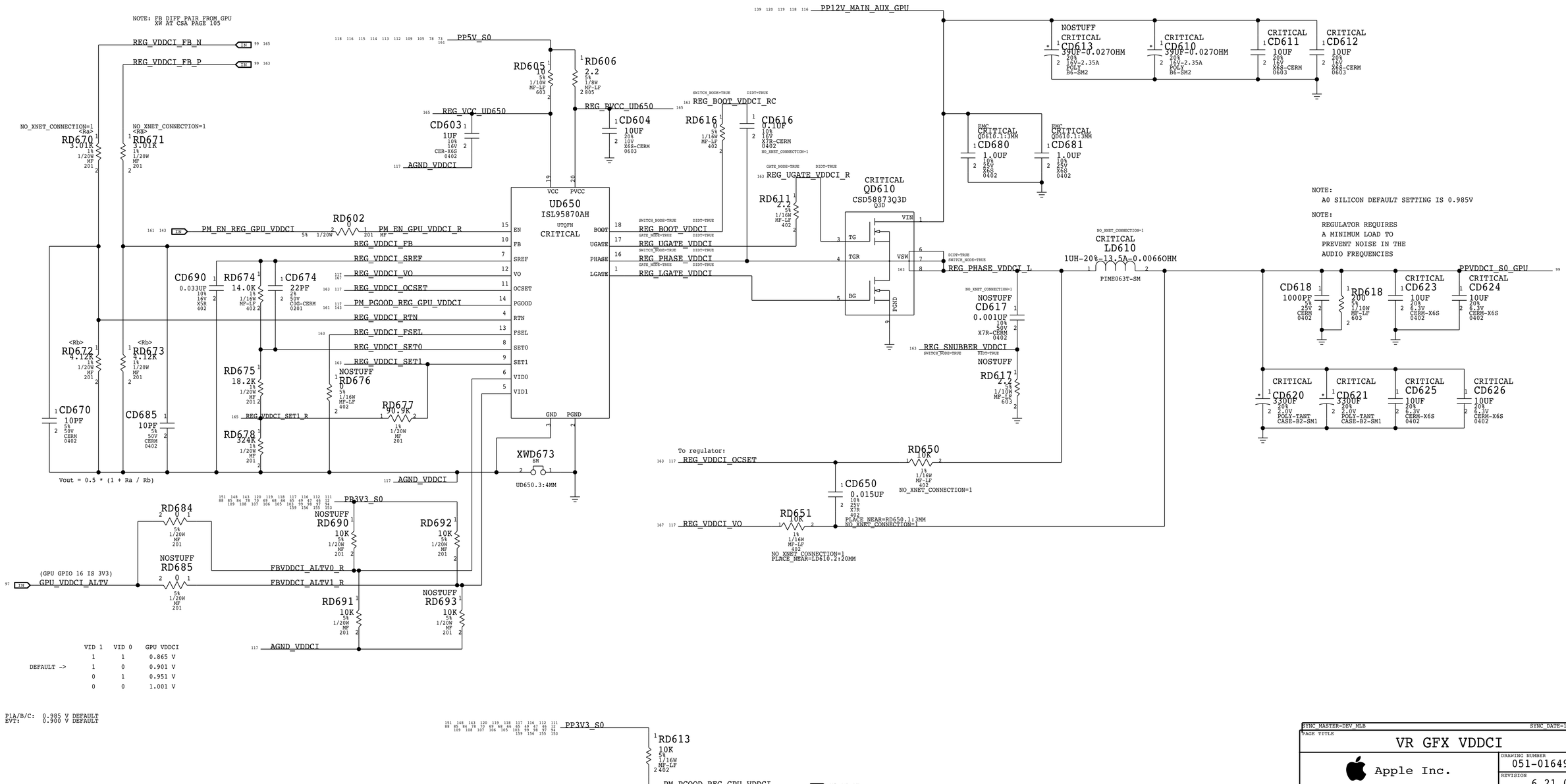
GFX VDDCI REGULATOR	
VOUT	0.900 V
PEAK (4 US)	6 A
OC (TYP)	12.7 A
AVG	4 A
FREQ	500 KHZ



VID 1	VID 0	GPU VDDCI
1	1	0.865 V
DEFAULT -> 1	0	0.901 V
0	1	0.951 V
0	0	1.001 V

P1A/B/C: 0.985 V DEFAULT
EVT: 0.900 V DEFAULT

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PAGE TITLE: VR GFX VDDCI

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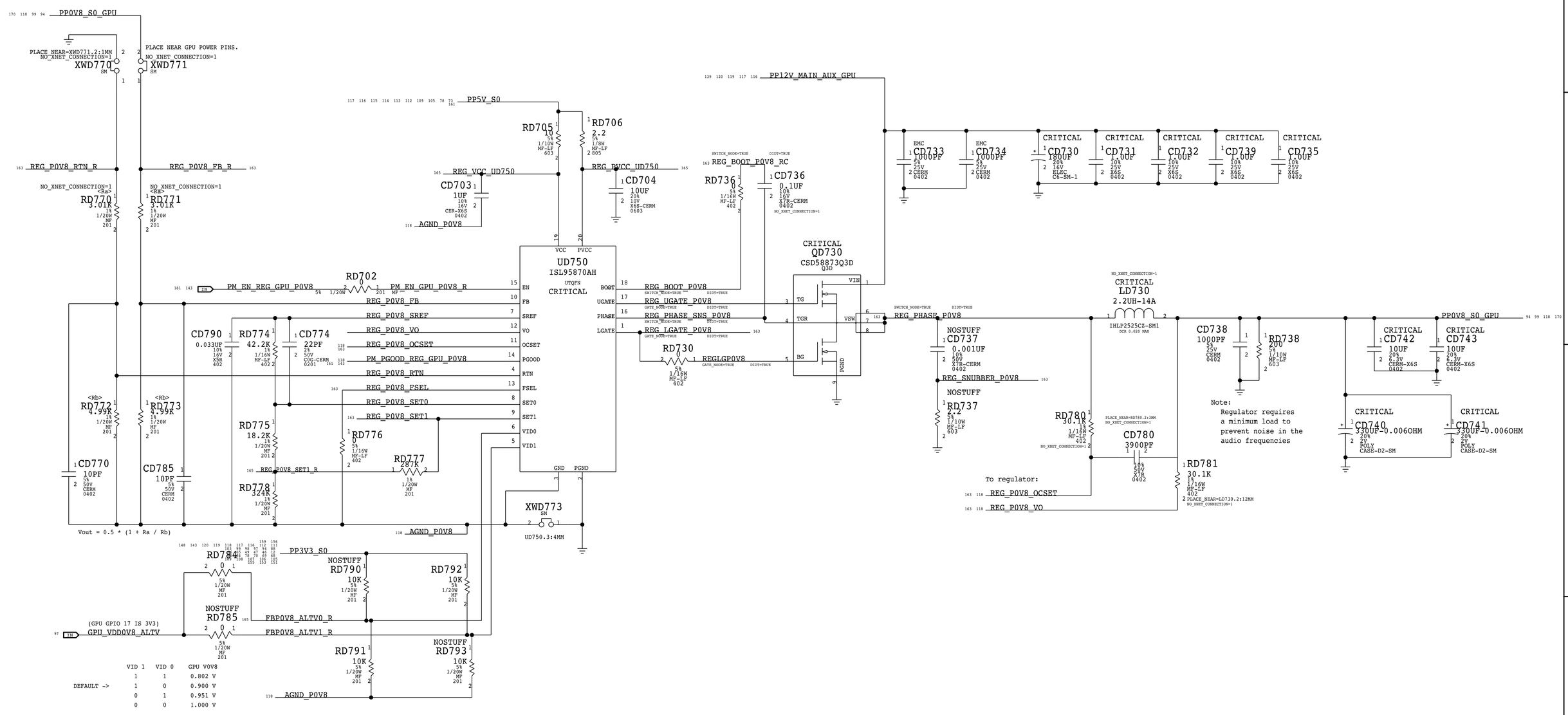
GFX 0V8 REGULATOR	
VOUT	0.9 V
PEAK (4 US)	5 A
OC (TYP)	14.2 A
AVG	4.5 A
FREQ	300 KHZ



VID 1	VID 0	GPU V0V8
1	1	0.802 V
DEFAULT -> 1	0	0.900 V
0	1	0.951 V
0	0	1.000 V

BOM_COST_GROUP=GRAPHICS

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VR GFX 0V8

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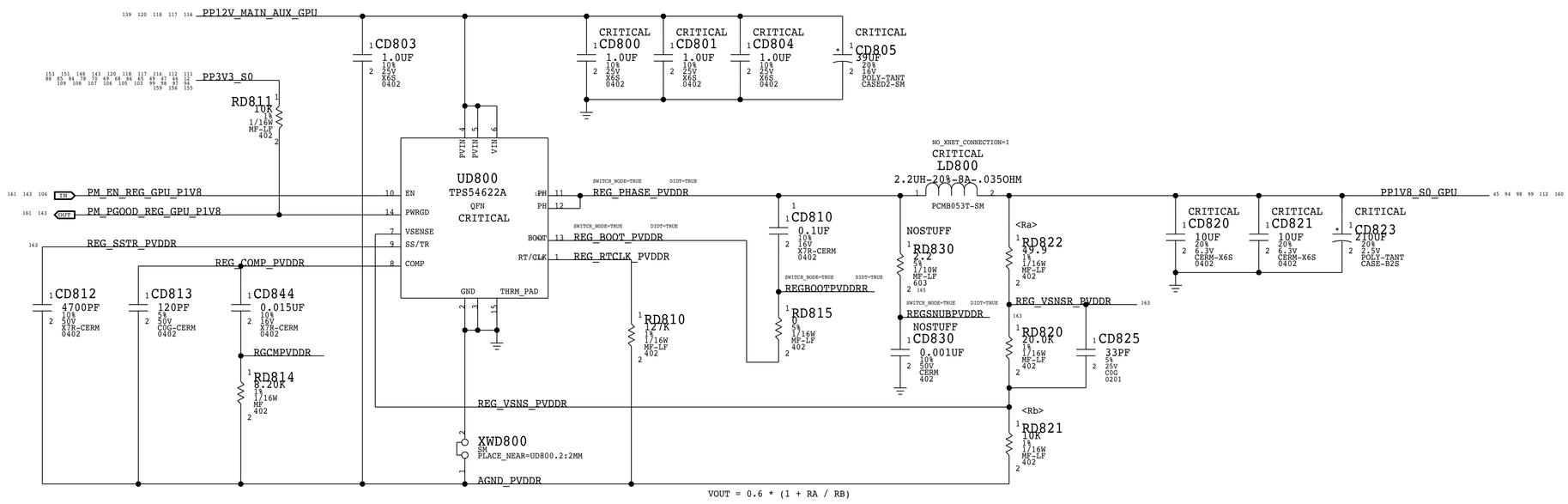
GFX 1V8 REGULATOR	
VOUT	1.803 V
PEAK (4 US)	4 A
OC (TYP)	11 A
AVG	3.2 A
FREQ	379 KHZ



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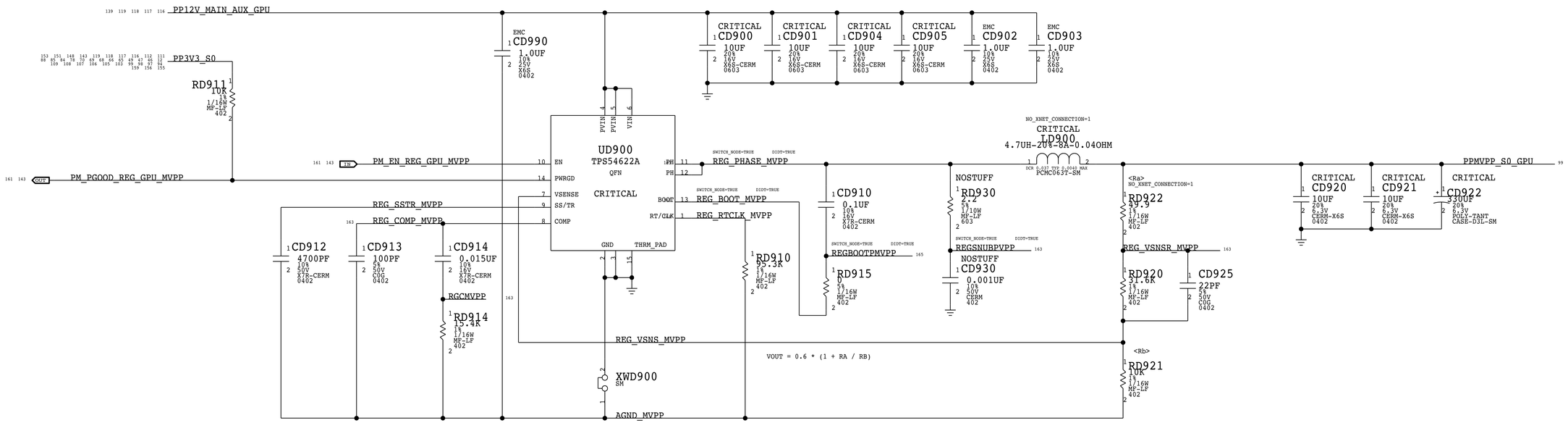
GFX MVPP REGULATOR	
VOUT	2.499 V
PEAK (4 US)	2 A
OC (TYP)	11 A
AVG	1.5 A
FREQ	500 KHZ



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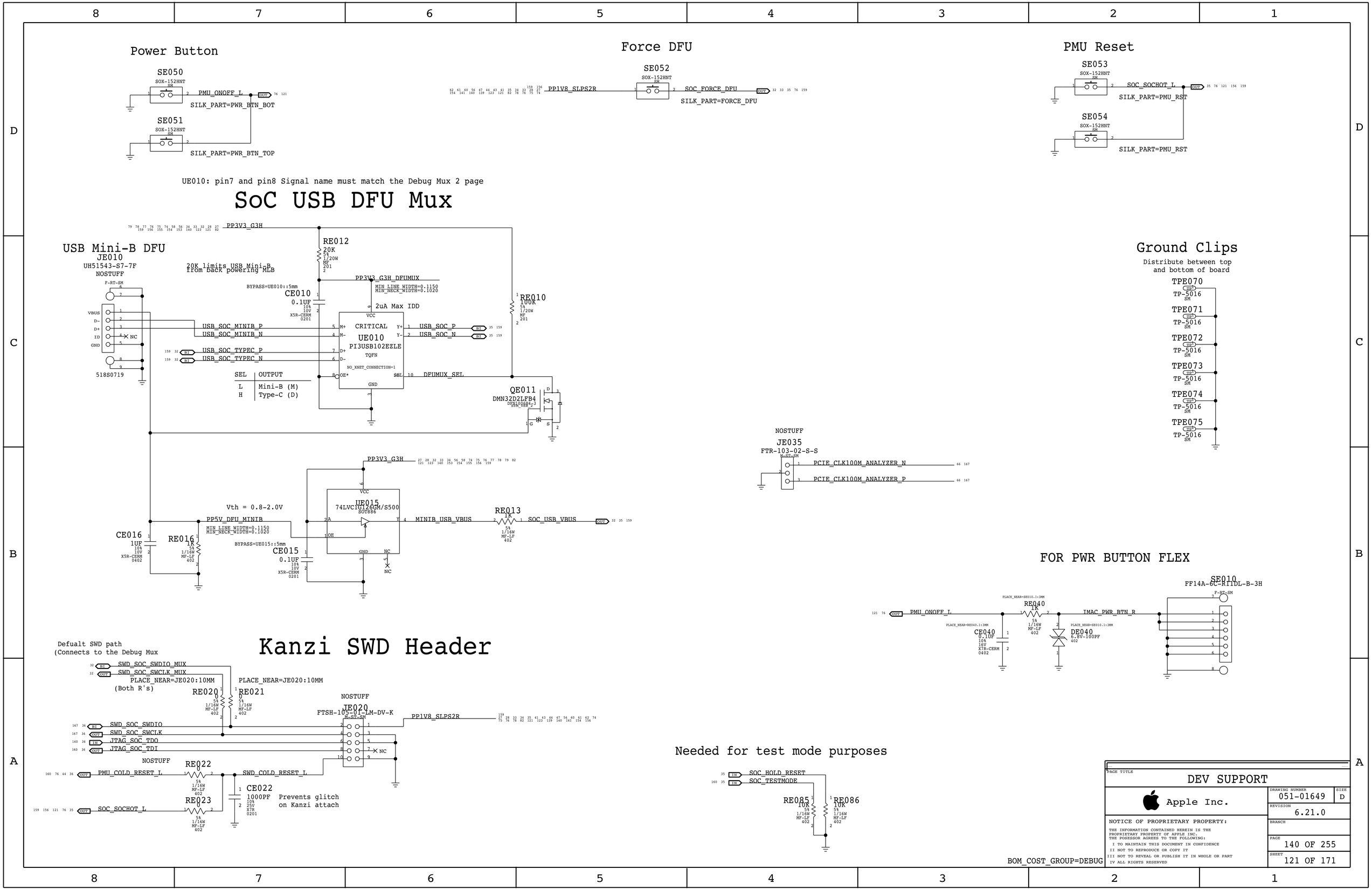
Power Button
SE050
SOX-152HNT
SM
PMU_ONOFF_L
SILK_PART=PWR_BTN_BOT
SE051
SOX-152HNT
SM
SILK_PART=PWR_BTN_TOP
Force DFU
SE052
SOX-152HNT
SM
PP1V8_SLPS2R
SOC_FORCE_DFU
SILK_PART=FORCE_DFU
PMU Reset
SE053
SOX-152HNT
SM
SOC_SOCHOT_L
SILK_PART=PMU_RST
SE054
SOX-152HNT
SM
SILK_PART=PMU_RST
UE010: pin7 and pin8 Signal name must match the Debug Mux 2 page
SoC USB DFU Mux
PP3V3_G3H
USB Mini-B DFU
JE010
UH51543-S7-7F
NOSTUFF
F-RT-SM
VBUS
D-
D+
ID
GND
NC
518S0719
20K limits USB Mini-B
from back powering MLB
RE012
20K
5%
1/20W
MF
201
PP3V3_G3H_DFUMUX
BYPASS=UE010::5mm
CE010
0.1UF
10%
10V
X5R-CERM
0201
MIN_LINE_WIDTH=0.1150
MIN_NECK_WIDTH=0.1020
2uA Max IDD
RE010
100K
5%
1/20W
MF
201
VCC
CRITICAL
UE010
PI3USB102EZLE
TQFN
NO_XNET_CONNECTION=1
GND
USB_SOC_MINIB_P
USB_SOC_MINIB_N
USB_SOC_TYPEC_P
USB_SOC_TYPEC_N
USB_SOC_P
USB_SOC_N
DFUMUX_SEL
SEL | OUTPUT
L | Mini-B (M)
H | Type-C (D)
QE011
DMN32D2LFB4
DFN1006H4-3
STN_VER=2
Ground Clips
Distribute between top
and bottom of board
TPE070
TPE071
TPE072
TPE073
TPE074
TPE075
TP-5016
SM
NOSTUFF
JE035
FTR-103-02-S-S
M-ST-SM
PCIE_CLK100M_ANALYZER_N
PCIE_CLK100M_ANALYZER_P
Vth = 0.8-2.0V
PP5V_DFU_MINIB
MIN_LINE_WIDTH=0.1150
MIN_NECK_WIDTH=0.1020
BYPASS=UE015::5mm
CE016
1UF
10%
10V
X5R-CERM
0402
RE016
1K
5%
1/16W
MF-LF
402
CE015
0.1UF
10%
10V
X5R-CERM
0201
UE015
74LVC1G126GM/S500
SOT886
MINIB_USB_VBUS
RE013
1K
5%
1/16W
MF-LF
402
SOC_USB_VBUS
FOR PWR BUTTON FLEX
SE010
FF14A-6C-R1IDL-B-3H
F-RT-SM
PMU_ONOFF_L
RE040
1K
5%
1/16W
MF-LF
402
IMAC_PWR_BTN_R
CE040
0.1UF
10%
16V
X7R-CERM
0402
DE040
6.8V-100PF
402
Kanzi SWD Header
Default SWD path
(Connects to the Debug Mux
(Both R's)
SWD_SOC_SWDIO_MUX
SWD_SOC_SWCLK_MUX
PLACE_NEAR=JE020:10MM
RE020
0
5%
1/16W
MF-LF
402
RE021
0
5%
1/16W
MF-LF
402
NOSTUFF
JE020
FTSH-105-01-L-DV-K
M-ST-SM
PP1V8_SLPS2R
SWD_SOC_SWDIO
SWD_SOC_SWCLK
JTAG_SOC_TDO
JTAG_SOC_TDI
NC
NOSTUFF
RE022
0
5%
1/16W
MF-LF
402
PMU_COLD_RESET_L
SWD_COLD_RESET_L
CE022
1000PF
10%
25V
X7R
0201
Prevents glitch
on Kanzi attach
RE023
0
5%
1/16W
MF-LF
402
SOC_SOCHOT_L
Needed for test mode purposes
SOC_HOLD_RESET
SOC_TESTMODE
RE085
10K
5%
1/16W
MF-LF
402
RE086
10K
5%
1/16W
MF-LF
402
BOM_COST_GROUP=DEBUG
PAGE TITLE
DEV SUPPORT
Apple Inc.
DRAWING NUMBER
051-01649
SIZE
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REVISION
6.21.0
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140 OF 255
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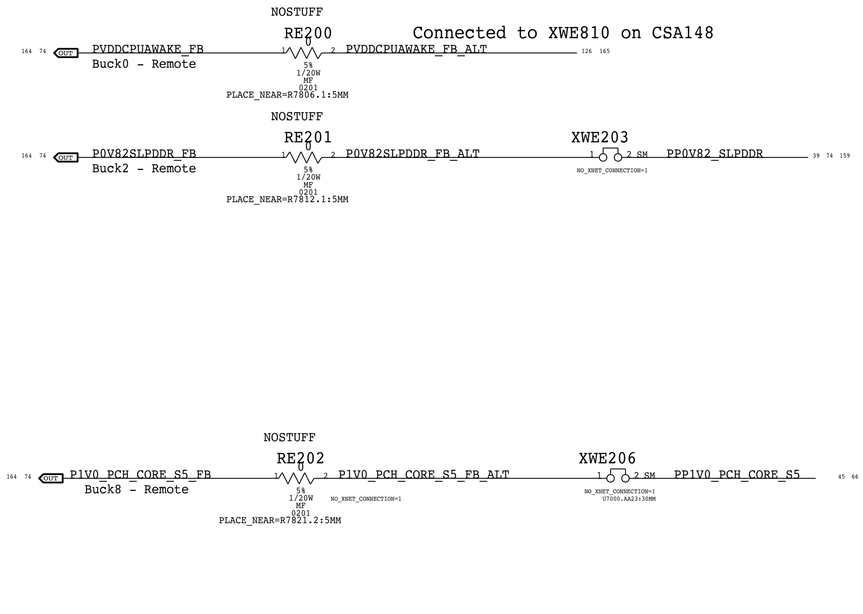
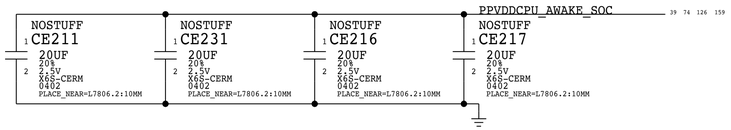
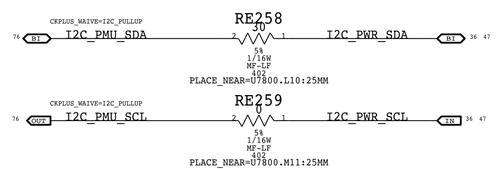
Alternate Feedback Sense





Undershoot damping rdar://26173471



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DRAWING NUMBER 051-01649
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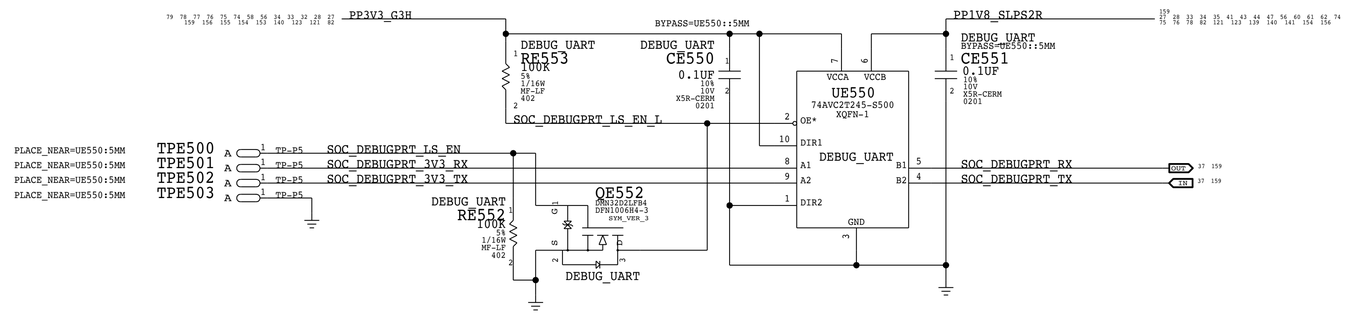
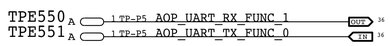
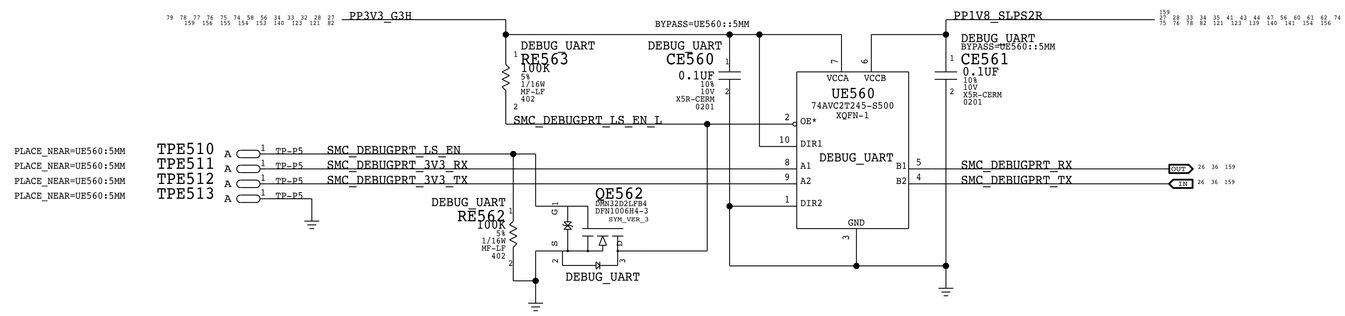
SOC UART0 Header

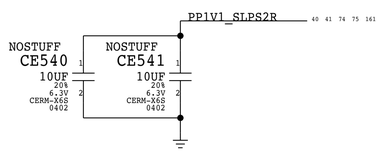


Debug header for SOC AOP UART



SMC UART0 Header





XDP_PRESENT and PCIE_UP_CLKREQ PU are moved to their pages

BOM_COST_GROUP=DEBUG

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SOC DEV SUPPORT

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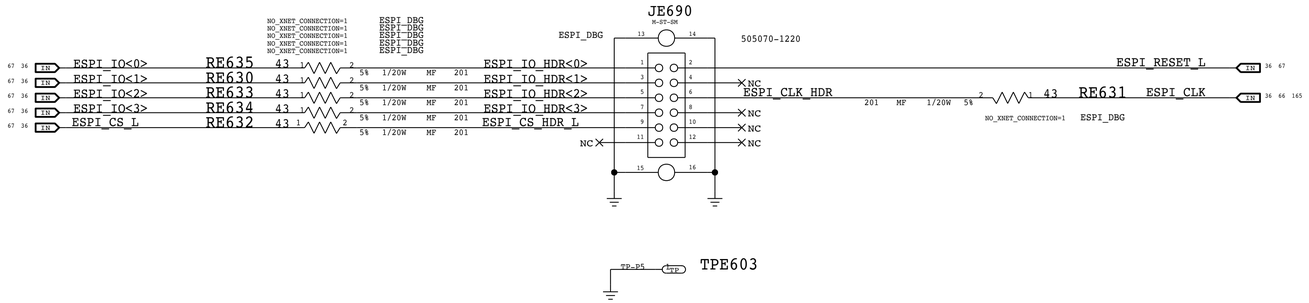
eSPI Analyzer

Placement study first



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DEBUG HEADERS 1

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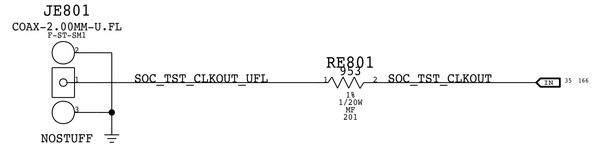
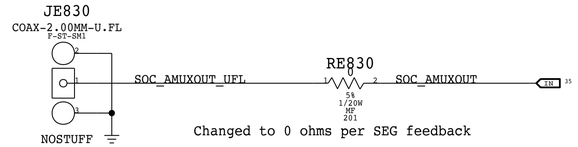
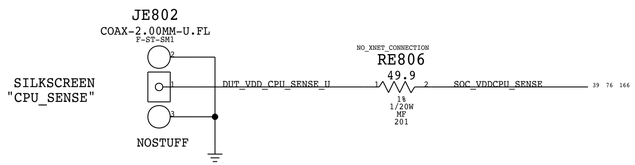
U.FL CONNECTOR FOR SOC CLOCKS

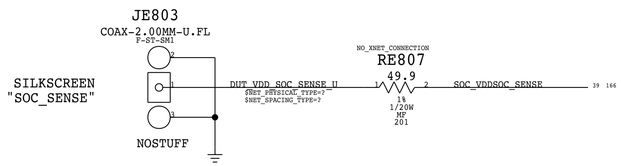


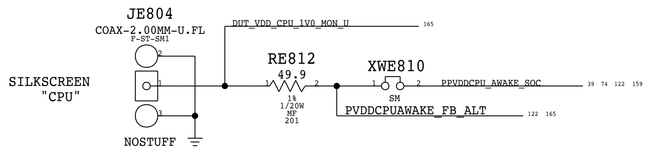


Changed to 0 ohms per SEG feedback

U.FL CONNECTOR FOR SOC POWER







BOM_COST_GROUP=DEBUG

PAGE TITLE
DEBUG SOC U.FL CONNECTORS

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DRAWING NUMBER 051-01649
SIZE D
REVISION 6.21.0
BRANCH
PAGE 148 OF 255
SHEET 126 OF 171

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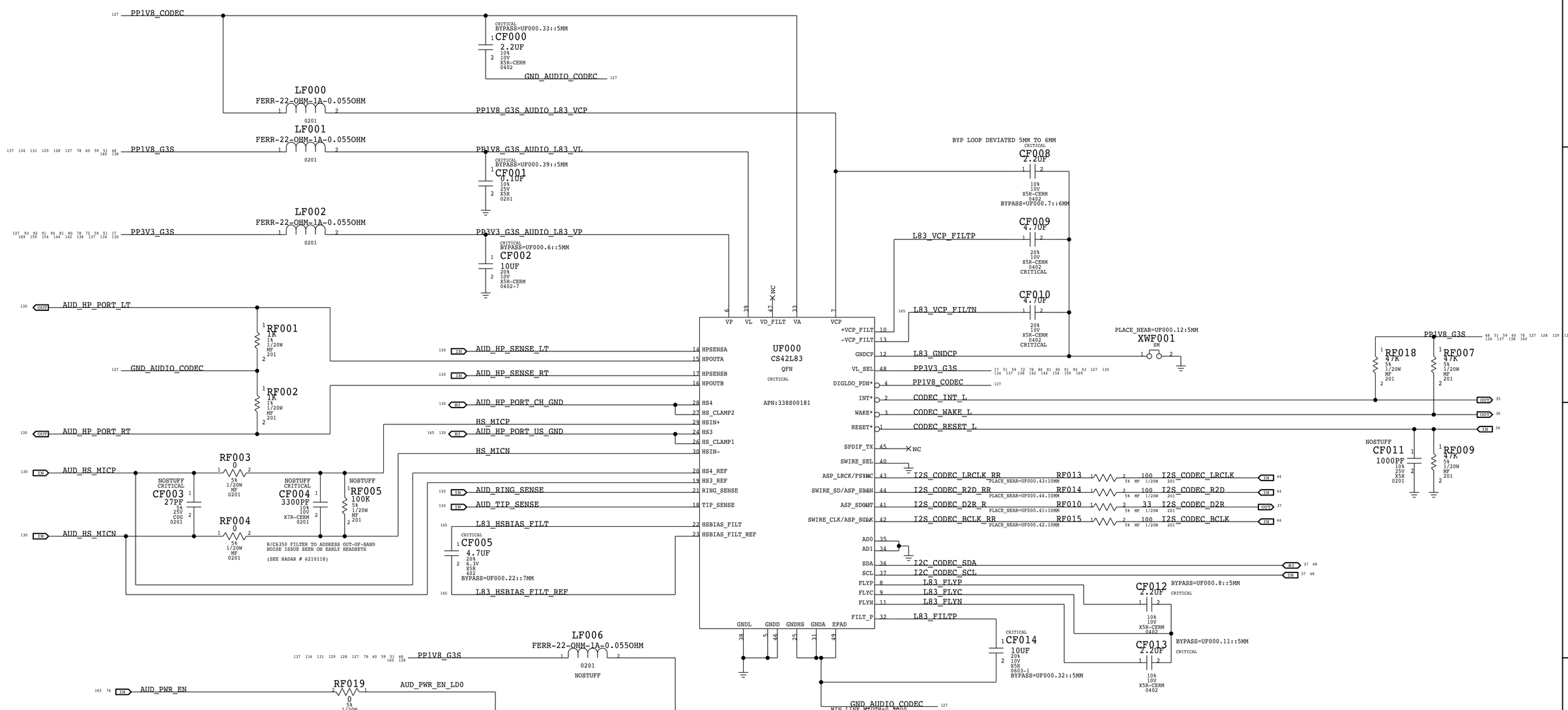
AD1	AD0	I2C ADDR
GND	GND	0X48 <--
GND	1.8V	0X49
1.8V	GND	0X4A
1.8V	1.8V	0X4B



PAGE TITLE

AUDIO JACK CODEC

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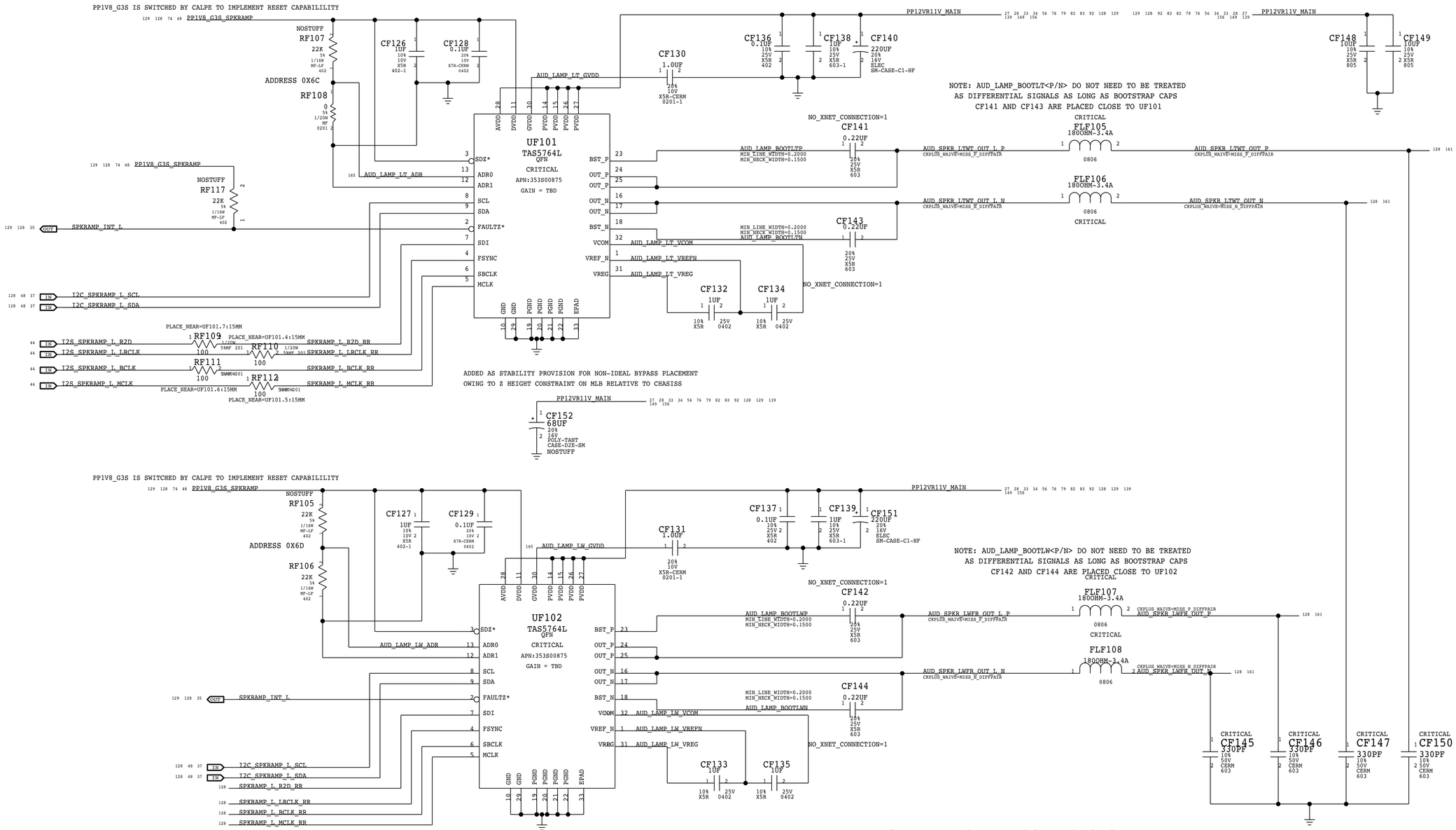
SPEAKER AMPLIFIERS - LEFT CHANNEL

2X MONO SPEAKER AMPLIFIERS (TAS5764L)



BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO LEFT SPKR AMP

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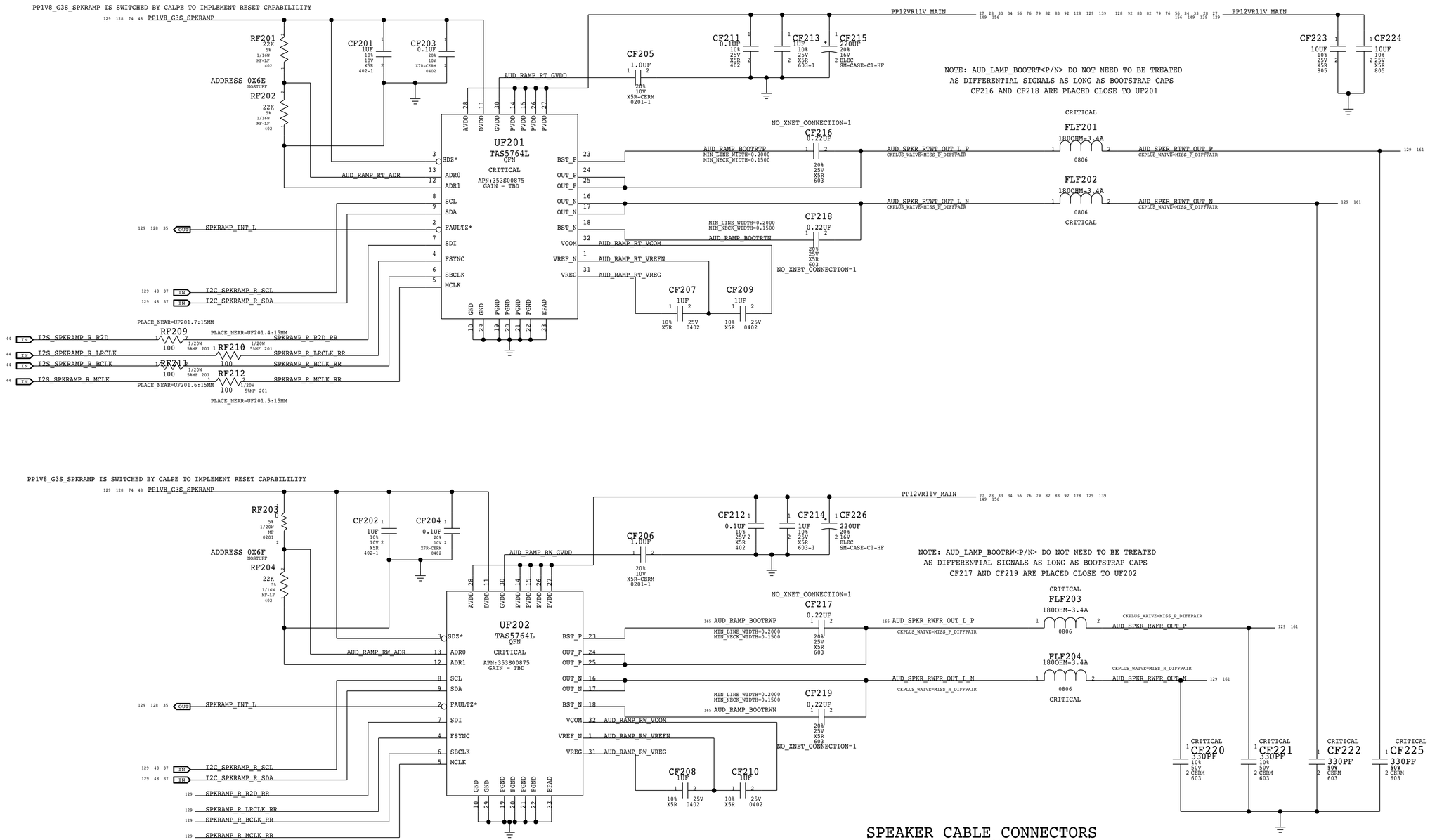

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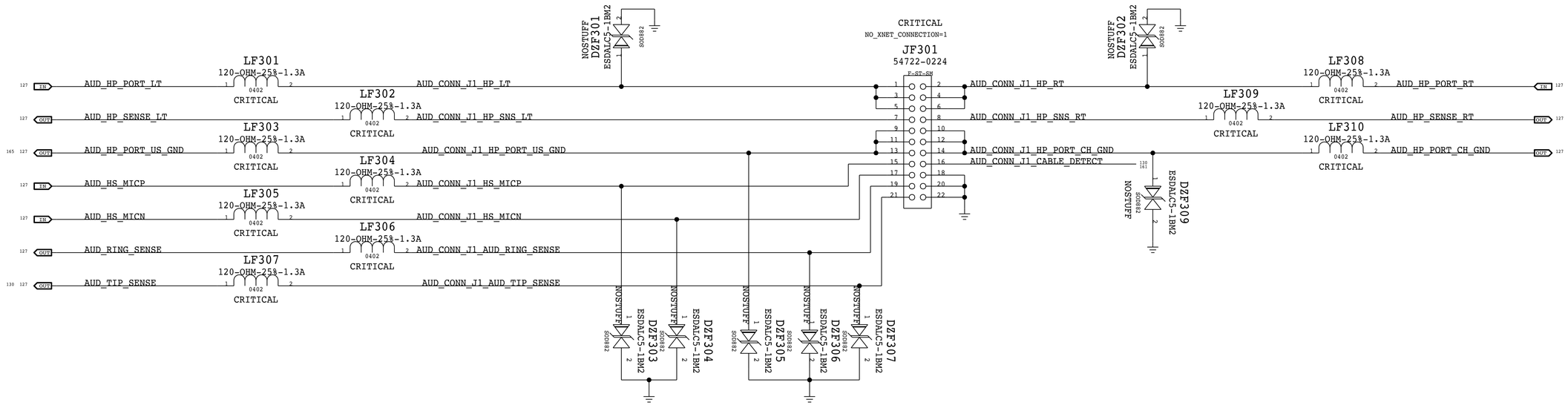
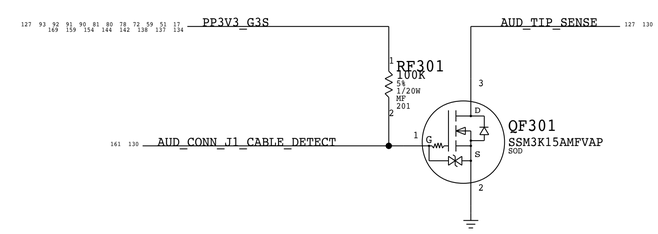


AUDIO JACK FLEX MISSING CABLE DETECT

FORCES SYSTEM TO INTERNAL SPEAKERS IF CABLE REMOVED



BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO JACK CONNECTOR

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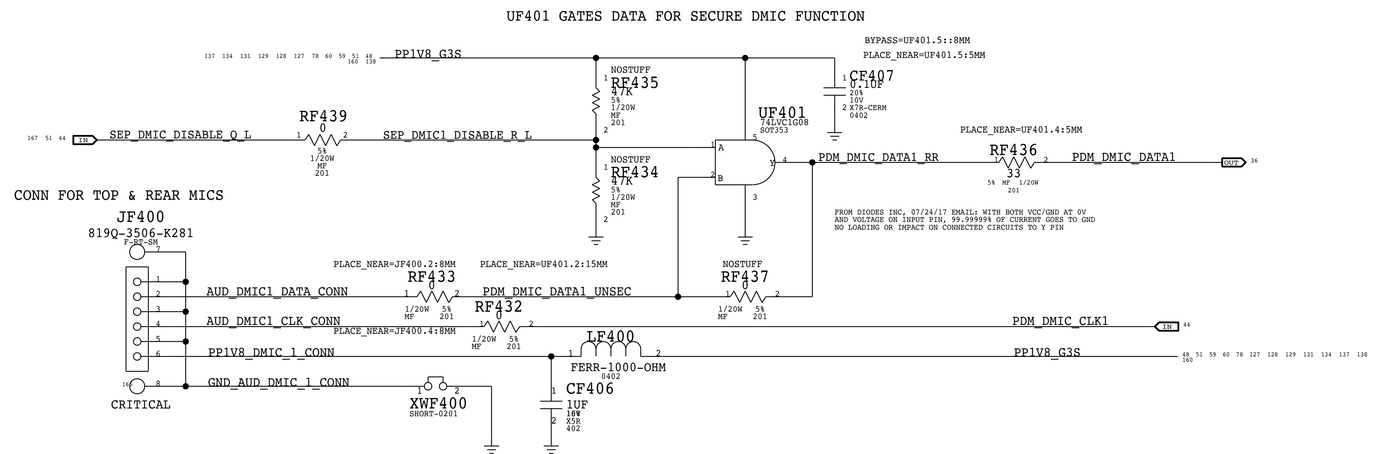

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AUDIO MIC CONNECTOR

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LAYOUT NOTE: ALL PCIE SIGNALS REQUIRE EASY ACCESS TPS
FOR X1 LANE P/N AND REFCLK - TPS AT EACH RECEIVER END
FOR CLKREQ, WAKE, RESET - TPS AT HARDPOOL END

PP3V3_G3S

CG071 3.0PF ±/-0.1PF 25V NPO-C0G 0201
CG072 3.0PF ±/-0.1PF 25V NPO-C0G 0201
CG061 3.0PF ±/-0.1PF 25V NPO-C0G 0201
CG062 3.0PF ±/-0.1PF 25V NPO-C0G 0201
CG063 3.0PF ±/-0.1PF 25V NPO-C0G 0201
CG073 3.0PF ±/-0.1PF 25V NPO-C0G 0201
CG092 3.0PF ±/-0.1PF 25V NPO-C0G 0201
CG081 3.0PF ±/-0.1PF 25V NPO-C0G 0201

CG040 12PF 5% 25V NPO-C0G 0201
CG041 12PF 5% 25V NPO-C0G 0201
CG042 12PF 5% 25V NPO-C0G 0201
CG043 12PF 5% 25V NPO-C0G 0201
CG044 12PF 5% 25V NPO-C0G 0201
CG074 12PF 5% 25V NPO-C0G 0201
CG077 12PF 5% 25V NPO-C0G 0201
CG078 12PF 5% 25V NPO-C0G 0201

CG070 10UF 20% 6.3V CERM-X5R 0402-4
CG036 10UF 20% 6.3V CERM-X5R 0402-4
CG037 10UF 20% 6.3V CERM-X5R 0402-4
CG038 10UF 20% 6.3V CERM-X5R 0402-4
CG075 10UF 20% 6.3V CERM-X5R 0402-4

CG080 0.1UF 10% 35V CER-X5R 0201
CG076 0.1UF 10% 35V CER-X5R 0201

PP1V8_G3S

CG082 0.1UF 10% 35V CER-X5R 0201
CG093 12PF 5% 25V NPO-C0G 0201
CG079 3.0PF ±/-0.1PF 25V NPO-C0G 0201

UG000
LBEE5ZZ1HP-049
LGA
SYM 1 OF 3
339S00404
CRITICAL

Pin	Signal	Net	Notes
91	2G_ANT_CORE0	50_G_0_MATCH	
87	5G_ANT_CORE0	50_A_0_MATCH	
76	2G_ANT_CORE1	50_G_1_MATCH	
72	5G_ANT_CORE1	50_A_1_MATCH	
49	2G_ANT_CORE2	50_G_2_MATCH	
65	5G_ANT_CORE2	50_A_2_MATCH	
44	BT_ONLY_ANT	BT_ONLY_ANT	
1	WL_JTAG_SEL	WLAN_JTAG_SEL	
81	WL_JTAG_TCK	SWD_WLAN_SWCLK	(GPIO2, 100K IPU VDDIO)
82	WL_JTAG_TDI	WLAN_THROTTLE	(GPIO4, IPD)
83	WL_JTAG_TMS	SWD_WLAN_SWDIO	(GPIO3, 100K IPU VDDIO)
84	WL_JTAG_TRST	WLAN_JTAG_TRST_L	(GPIO6, ACTIVE LOW)
85	WL_JTAG_TDO	WLAN_JTAG_TDO	(GPIO5)
93	WL_UART_RX	HPN_WLAN_UART_R2D	(100K IPU VDDIO)
94	WL_UART_TX	HPN_WLAN_UART_D2R	(EXT PU NEEDED)
95	WL_UART_RTS	HPN_WLAN_UART_RTS_L	(ACTIVE LOW, EXT PU NEEDED)
96	WL_UART_CTS	HPN_WLAN_UART_CTS_L	(ACTIVE LOW, 100K IPU VDDIO)
67	WL_SPROM_MO	WLAN_SPROM_MOSI	
68	WL_SPROM_MI	WLAN_SPROM_MISO	
69	WL_SPROM_CLK	WLAN_SPROM_CLK	
70	WL_SPROM_CS	WLAN_SPROM_CS	(ACTIVE HIGH)
97	WL_GPIO_13	NC	(MOTION CONTEXT A)
100	WL_GPIO_21	NC	(MOTION CONTEXT B)
99	WL_GPIO_20	WLAN_AUDIO_SYNC	(WIFI TIME SYNC, EXT PD NEEDED)
98	WL_GPIO_17	PD_WLAN_GPIO_17	(ACTIVE LOW SROM PRESENCE)
159	WL_PMU_TEST_O	WLAN_PMU_TEST_O	(NOTE DEFINED)
161	WL_GPIO_14	NC_SECI_OUT_D2R	(SECI OUT)
163	WL_GPIO_12	NC_SECI_IN_R2D	(SECI IN)
78	WL_HOST_WAKE	WLAN_HOST_WAKE_HPN	(EXT PULL NEEDED)
79	WL_DEV_WAKE	WLAN_DEV_WAKE	(IPD)
19	WL_REG_ON	WLAN_PWR_EN	(ACTIVE HIGH)
20	BT_REG_ON	BT_PWR_EN	(ACTIVE HIGH)
6	PCIE_REFCLK_P	PCIE_CLK100M_WLAN_P	
5	PCIE_REFCLK_N	PCIE_CLK100M_WLAN_N	
9	PCIE_TX0P	PCIE_WLAN_D2R_C_P	
8	PCIE_TX0N	PCIE_WLAN_D2R_C_N	
12	PCIE_RX0P	PCIE_WLAN_R2D_P	
11	PCIE_RX0N	PCIE_WLAN_R2D_N	
14	PCIE_CLKREQ*	WLAN_CLKREQ_L	(EXT PU NEEDED)
15	PCIE_WAKE*	WLAN_WAKE_L	
16	PERST*	WLAN_PERST_L	(EXT PU NEEDED)
54	BT_UART_RX	HPN_BT_UART_R2D	(IPU VDDIO)
55	BT_UART_TX	HPN_BT_UART_D2R	(EXT PU NEEDED)
56	BT_UART_CTS	HPN_BT_UART_CTS_L	(ACTIVE LOW, IPU VDDIO)
57	BT_UART_RTS	HPN_BT_UART_RTS_L	(ACTIVE LOW, EXT PU NEEDED)
53	BT_GPIO_2/BT_SF_STRAP	BT_ROM_BOOT_HPN_L	(40K IPD)
60	BT_JTAG_STRAP	TP_BT_JTAG_STRAP	(NOT DEFINED)
36	BT_SF_CS	BT_SF_CS_L	(ACTIVE LOW)
37	BT_SF_CLK	BT_SF_CLK	
38	BT_SF_MISO	BT_SF_MISO	
39	BT_SF_MOSI	BT_SF_MOSI	
40	BT_I2S_WS	UART_BT_SOC_LH_R_R2D	(I2S:IPD, UART:IPU)
41	BT_I2S_DO	TP_BT_I2S_D2R	(I2S:EXT PD NEEDED, UART:NONE?)
123	BT_I2S_CLK	UART_BT_SOC_LH_R_D2R	(I2S:IPD, UART:NONE)
124	BT_I2S_DI	TP_BT_I2S_R2D	(I2S:IPD, UART:NONE)
59	BT_GPIO_3	NC	(BT TIME STAMP)
58	BT_GPIO_4	NC	(BT TIME SYNC)
			(RSVD)
61	BT_DEV_WAKE	BT_DEV_WAKE	(IPD)
62	BT_HOST_WAKE	BT_HOST_WAKE	(EXT PULL NEEDED)
29	VDDBAT_HP		
30	VDDBAT_LP		
28	VDD3P3_BT		
42	VDD3P3_PAD		
35	VDD3P3_FEM_CORE0		
89	VDD3P3_FEM_CORE1		
74	VDD3P3_FEM_CORE2		
63	VDDIO_RFSW		
2	VDDIO_PMU		
18	VDD3P3_SDAOTP		
17	VDDIO_DIG		
3	VDD1P5_1X1		
21	SR1P4_VLX		
22	SR1P8_VLX		
23	VIN_RFLDO		
24	SR1P2_VLX		
34	VDD1P2_3X3		
25	CLK32K		
26			
32			
33			
52			

CG032 0.1UF 10% 25V X6S-CERM 0201 PLACE_NEAR=UG000.9:2MM — PCIE_WLAN_D2R_P (OUT 68 167)
CG033 0.1UF 10% 25V X6S-CERM 0201 PLACE_NEAR=UG000.8:2MM — PCIE_WLAN_D2R_N (OUT 68 167)
CG031 0.1UF 10% 25V X6S-CERM 0201 PLACE_NEAR=U7000.K44:5MM — PCIE_WLAN_R2D_C_P (IN 68 167)
CG030 0.1UF 10% 25V X6S-CERM 0201 PLACE_NEAR=U7000.K43:5MM — PCIE_WLAN_R2D_C_N (IN 68 167)

RG070 0 5% 1/20W MF 201 — UART_BT_SOC_LH_R_R2D (IN 37)
RG071 0 5% 1/20W MF 201 — UART_BT_SOC_LH_D2R (OUT 37 134)

WLAN_CLK32K_HPN (IN 137)

WLAN_HOST WAKE ASSERTS WHEN A WLAN TRIGGER INTENDS TO WAKE THE SYSTEM FOR EXAMPLE, A REMOTE LOGIN SHOULD WAKE THE SYSTEM VIA WLAN_HOST_WAKE

WLAN_DEV_WAKE WAS HISTORICALLY USED TO WAKE WLAN WITHOUT HAVING TO WAIT FOR A PCIE RESPONSE COMING FROM AN ASLEEP WLAN DEVICE. THE PCIE RESPONSE TOOK A LONG TIME SO WLAN_DEV WAKE USED INSTEAD. BUT NOW SW IS WORKING ON ANOTHER WAY, SENDING A PCIE MESSAGE THAT DOESN'T REQUIRE A RESPONSE FROM THE WLAN DEVICE. SO THIS SIGNAL MAY BE GOING AWAY SOON

BT_DEV_WAKE IS ACTIVE HIGH AND IS ANALAGOUS TO BT_LOW_PWR_L
IF PULLED LOW, HOST ALLOWS BT CONTROLLER TO GO TO LOW POWER STATE

BT_HOST_WAKE WILL ASSERT ANYTIME THERE IS BT DEVICE ACTIVITY

PP1V8_G3S

RG088 47K 5% 1/20W MF 201 — UART_BT_SOC_LH_D2R (37 134)
RG089 10K NOSTUFF 5% 1/20W MF 201 — WLAN_WAKE_L (134 137 138)

PP1V8_G3S

RG082 2.4K 1/16W 1% MF 402-1 — BT_ROM_BOOT_HPN_L (134 137) 0: BOOT FROM INTERNAL ROM 1: BOOT FROM SPLASH
RG081 10K NOSTUFF 1/16W 5% MF-LF 402
RG083 10K NOSTUFF 1/20W 5% MF 201 — WLAN_JTAG_SEL (134 137 160) 0: SOME JTAG ARE GPIOS 1: JTAG ENABLED
RG084 10K 1/20W 5% MF 201

RG087 10K 5% 1/20W MF 201 — WLAN_SPROM_CS (134 137)
RG085 10K NOSTUFF 5% 1/20W MF 201 — BT_HOST_WAKE (36 134 137)
RG086 10K NOSTUFF 5% 1/20W MF 201 — WLAN_HOST_WAKE_HPN (134 137 138)
RG080 10K 5% 1/20W MF 201 — PD_WLAN_GPIO_17 (134) 0: SROM IS PRESENT 1: SROM ABSENT

VDD1P2
CG003 7.5UF 20% 4V CERM 0402
LG003 1UH-20%-4.1A-0.048OHM 2520-1
SR1P2_VLX — VDD1P2_C

VDD1P5
CG001 7.5UF 20% 4V CERM 0402
LG001 2.2UH-1.2A 0806
VDD1P5_C — SR1P4_VLX

VIN_RFLDO
CG002 7.5UF 20% 4V CERM 0402
LG002 2.2UH-1.2A 0806
SR1P8_VLX — VIN_RFLDO_C

BOM_COST_GROUP=WIRELESS

SYNC_DATE=NETS — SYNC_DATE=05/04/2017
PAGE TITLE: WIFI/BT MODULE 1

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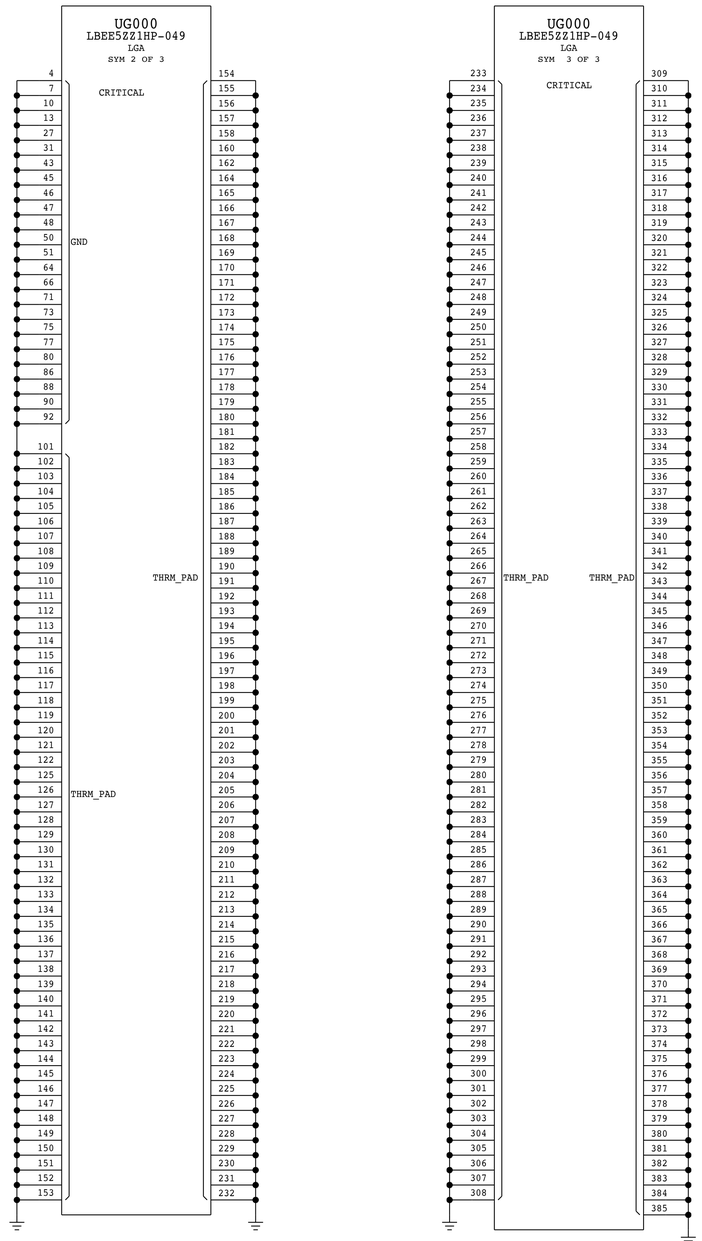

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SYNC_MASTER=METE SYNC_DATE=05/04/2017

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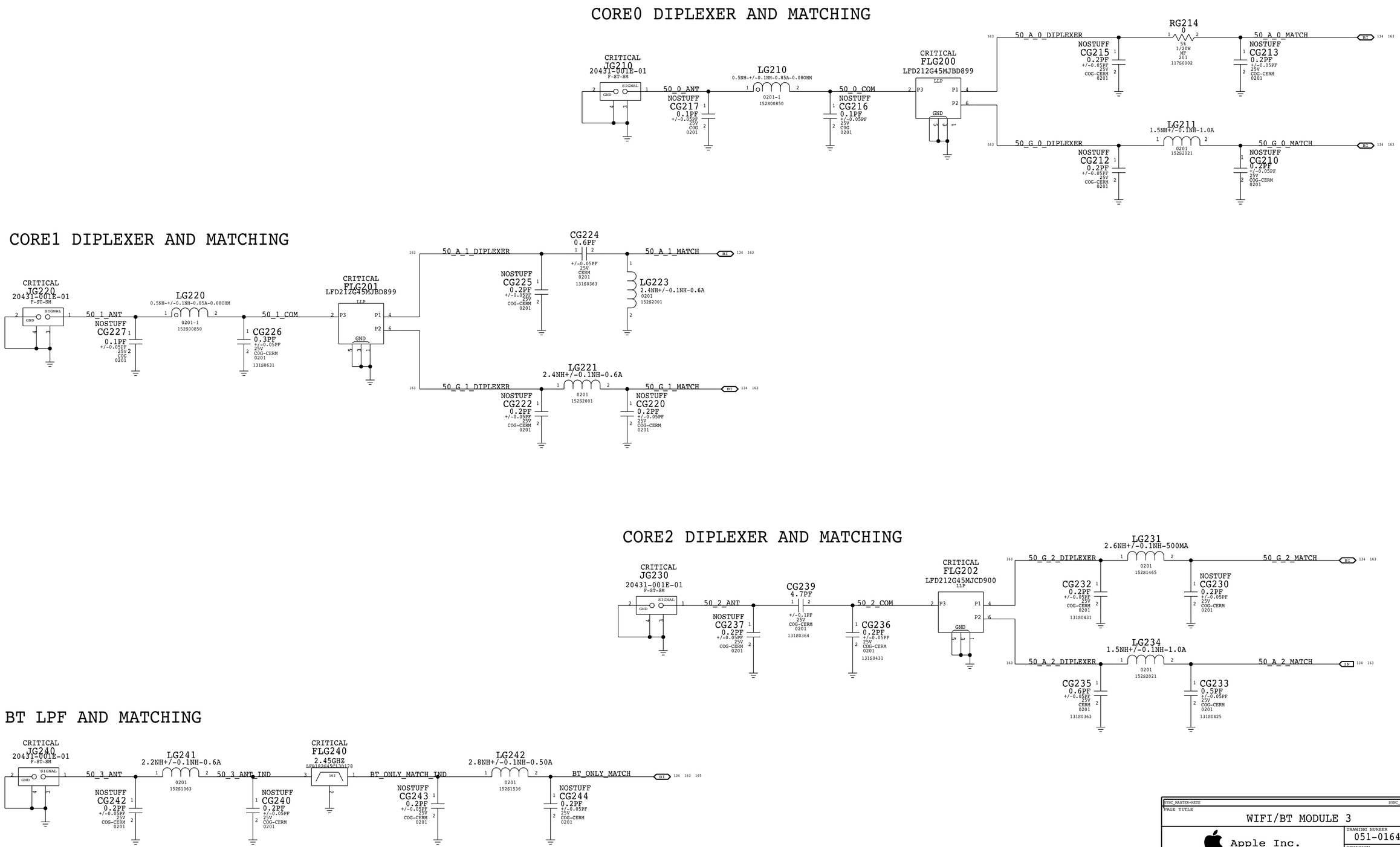

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SYNC_MASTER=METE SYNC_DATE=05/04/2017

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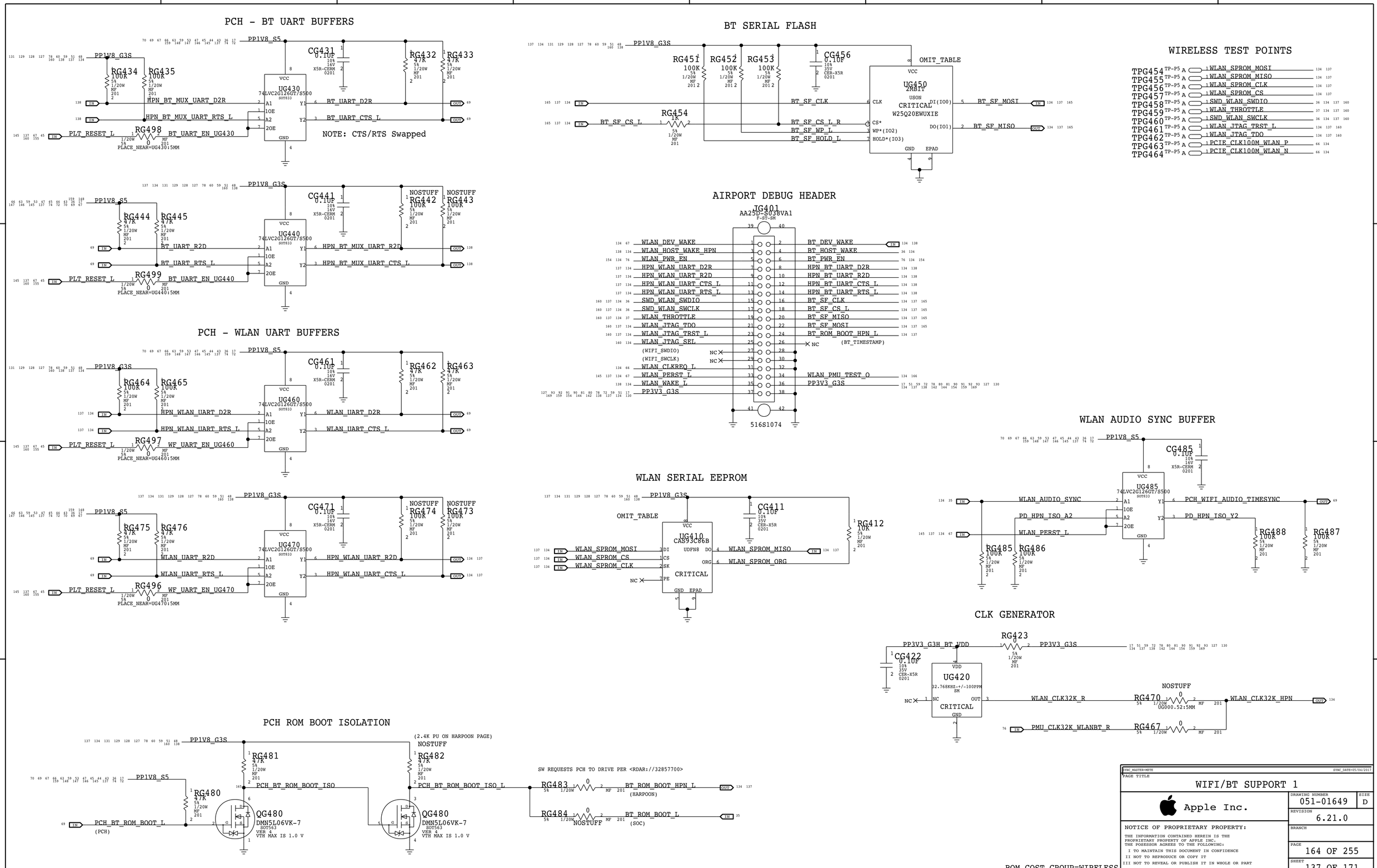
PCH - BT UART BUFFERS
NOTE: CTS/RTS Swapped
BT SERIAL FLASH
WIRELESS TEST POINTS
AIRPORT DEBUG HEADER
PCH - WLAN UART BUFFERS
WLAN AUDIO SYNC BUFFER
WLAN SERIAL EEPROM
CLK GENERATOR
PCH ROM BOOT ISOLATION
SW REQUESTS PCH TO DRIVE PER <RDAR://32857700>
BOM_COST_GROUP=WIRELESS
WIFI/BT SUPPORT 1
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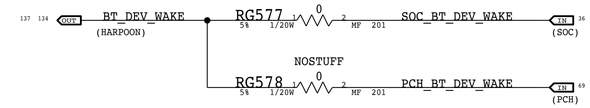
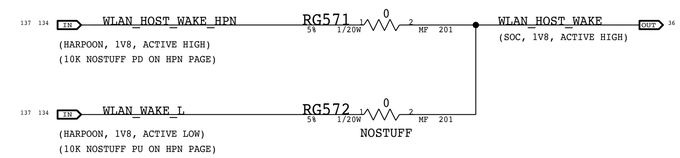
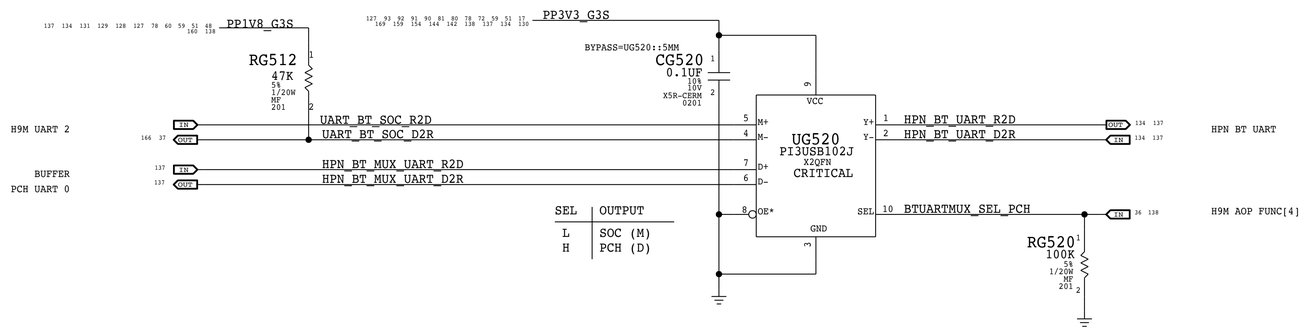
Software	I2S_SEL	UART_SEL	I2S I/F	UART I/F
Gen1 (macOS)	0	1	UART (PCH)	UART (PCH)
Gen1 (Bootcamp)	1	1	I2S (PCH)	UART (PCH)
Gen2	X	0	X	UART (SOC)

BT DEV WAKE ROUTING OPTION
<RDAR://33783520>

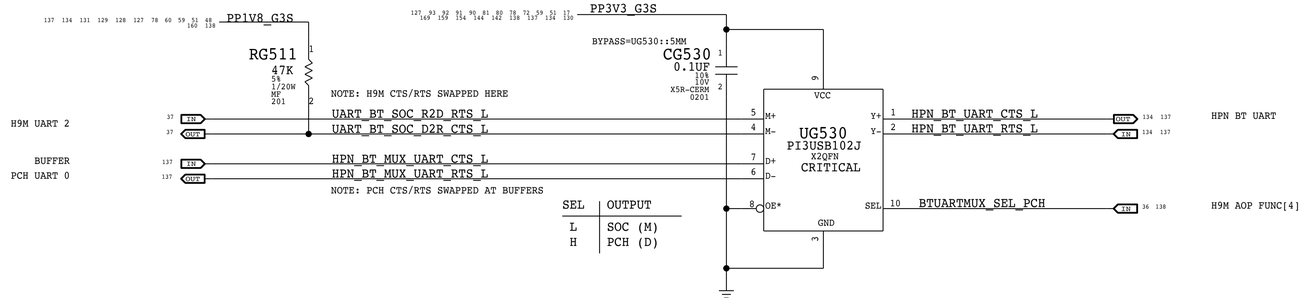


WIRELESS WAKE ROUTING OPTIONS





SEL	OUTPUT
L	SOC (M)
H	PCH (D)



SEL	OUTPUT
L	SOC (M)
H	PCH (D)

BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT SUPPORT 2

Apple Inc.

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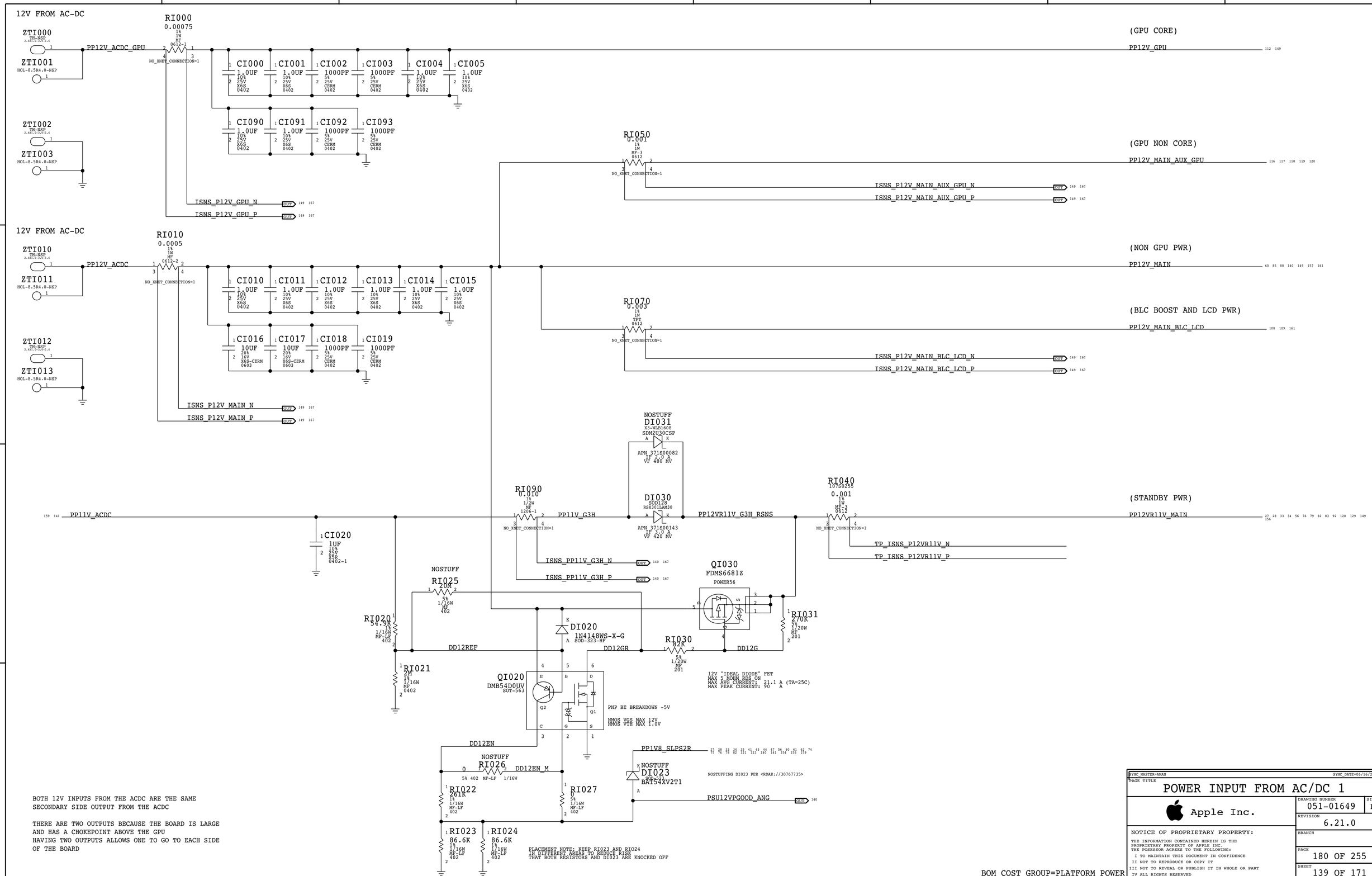
12V FROM AC-DC
ZTI000
ZTI001
ZTI002
ZTI003
PP12V_ACDC_GPU
RI000
0.00075
CI000 CI001 CI002 CI003 CI004 CI005
CI090 CI091 CI092 CI093
ISNS_P12V_GPU_N
ISNS_P12V_GPU_P
(GPU CORE)
PP12V_GPU
RI050
0.001
(GPU NON CORE)
PP12V_MAIN_AUX_GPU
ISNS_P12V_MAIN_AUX_GPU_N
ISNS_P12V_MAIN_AUX_GPU_P
12V FROM AC-DC
ZTI010
ZTI011
ZTI012
ZTI013
PP12V_ACDC
RI010
0.0005
CI010 CI011 CI012 CI013 CI014 CI015
CI016 CI017 CI018 CI019
ISNS_P12V_MAIN_N
ISNS_P12V_MAIN_P
(NON GPU PWR)
PP12V_MAIN
RI070
0.003
(BLC BOOST AND LCD PWR)
PP12V_MAIN_BLC_LCD
ISNS_P12V_MAIN_BLC_LCD_N
ISNS_P12V_MAIN_BLC_LCD_P
NOSTUFF
DI031
X3-WLB1608
SDM2U30CSP
APN 371S00082
IF 2.0 A
VF 480 MV
RI090
0.010
DI030
SOD128
RSX301LAM30
APN 371S00143
IF 3.0 A
VF 420 MV
RI040
107S0255
0.001
(STANDBY PWR)
PP12VR11V_MAIN
PP11V_ACDC
PP11V_G3H
PP12VR11V_G3H_RSNS
TP_ISNS_P12VR11V_N
TP_ISNS_P12VR11V_P
CI020
1UF
ISNS_PP11V_G3H_N
ISNS_PP11V_G3H_P
NOSTUFF
RI025
20K
QI030
FDMS6681Z
POWER56
RI020
54.9K
DI020
1N4148WS-X-G
SOD-323-HF
RI031
270K
RI030
82K
DD12REF
DD12GR
DD12G
RI021
2M
QI020
DMB54D0UV
SOT-563
12V "IDEAL DIODE" FET
MAX 5 MOHM RDS ON
MAX AVG CURRENT: 21.1 A (TA=25C)
MAX PEAK CURRENT: 90 A
PNP BE BREAKDOWN -5V
NMOS VGS MAX 12V
NMOS VTH MAX 1.0V
DD12EN
NOSTUFF
RI026
DD12EN_M
PP1V8_SLPS2R
NOSTUFF
DI023
BAT54XV2T1
NOSTUFFING DI023 PER <RDAR://30767735>
PSU12VPGOOD_ANG
RI022
261K
RI027
0
RI023
86.6K
RI024
86.6K
PLACEMENT NOTE: KEEP RI023 AND RI024
IN DIFFERENT AREAS TO REDUCE RISK
THAT BOTH RESISTORS AND DI023 ARE KNOCKED OFF
BOTH 12V INPUTS FROM THE ACDC ARE THE SAME
SECONDARY SIDE OUTPUT FROM THE ACDC
THERE ARE TWO OUTPUTS BECAUSE THE BOARD IS LARGE
AND HAS A CHOKEPOINT ABOVE THE GPU
HAVING TWO OUTPUTS ALLOWS ONE TO GO TO EACH SIDE
OF THE BOARD
BOM_COST_GROUP=PLATFORM POWER
SYNC_MASTER=AMAN
SYNC_DATE=06/16/2017
PAGE TITLE
POWER INPUT FROM AC/DC 1
Apple Inc.
DRAWING NUMBER
051-01649
SIZE
D
REVISION
6.21.0
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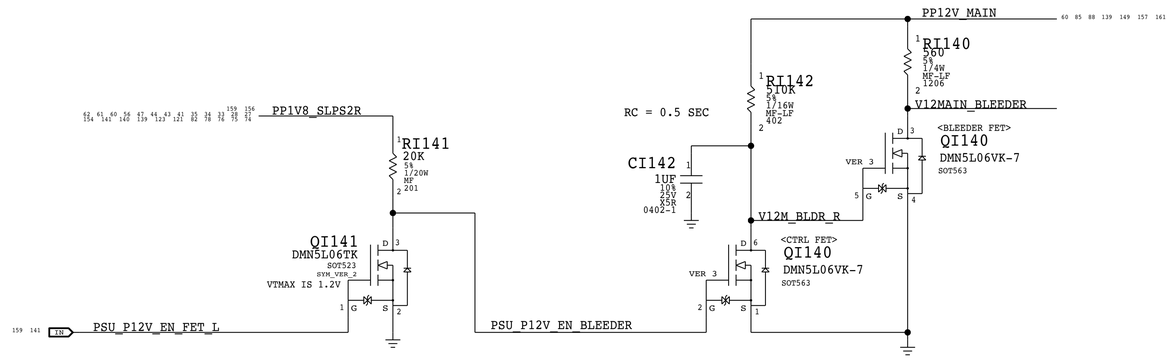
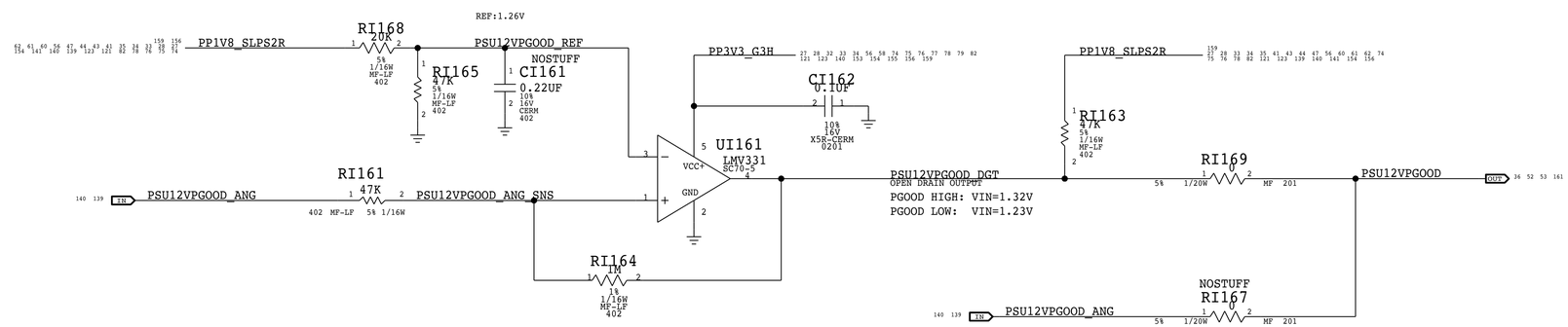
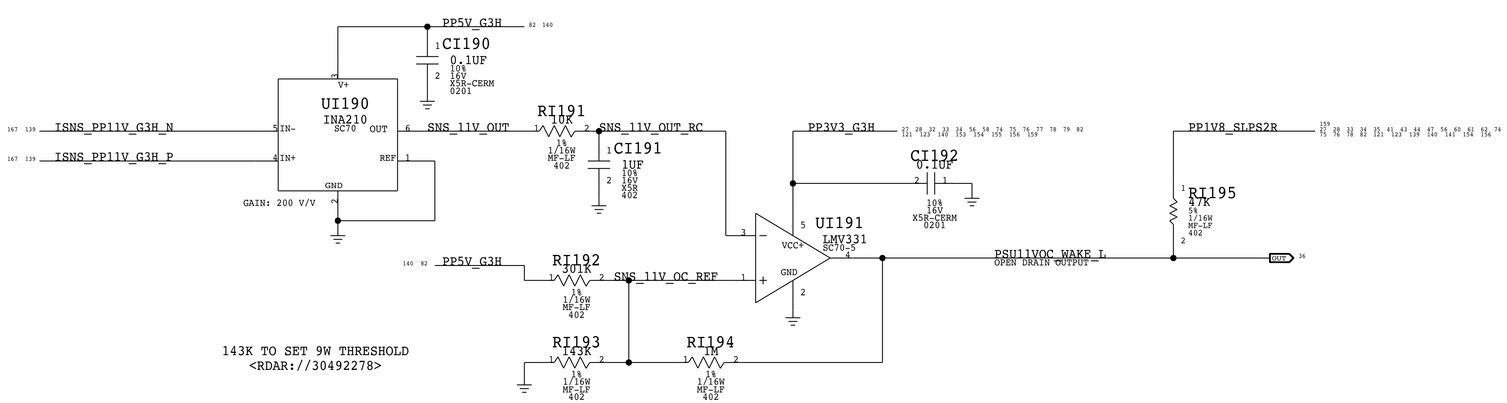
PP12_MAIN BLEEDER CIRCUIT





PP11V_STBY OVERCURRENT DETECTION



143K TO SET 9W THRESHOLD
<RDAR://30492278>

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=AMAN SYNC_DATE=06/16/2017

PAGE TITLE
POWER INPUT FROM AC/DC 2

Apple Inc.

DRAWING NUMBER 051-01649 SIZE D

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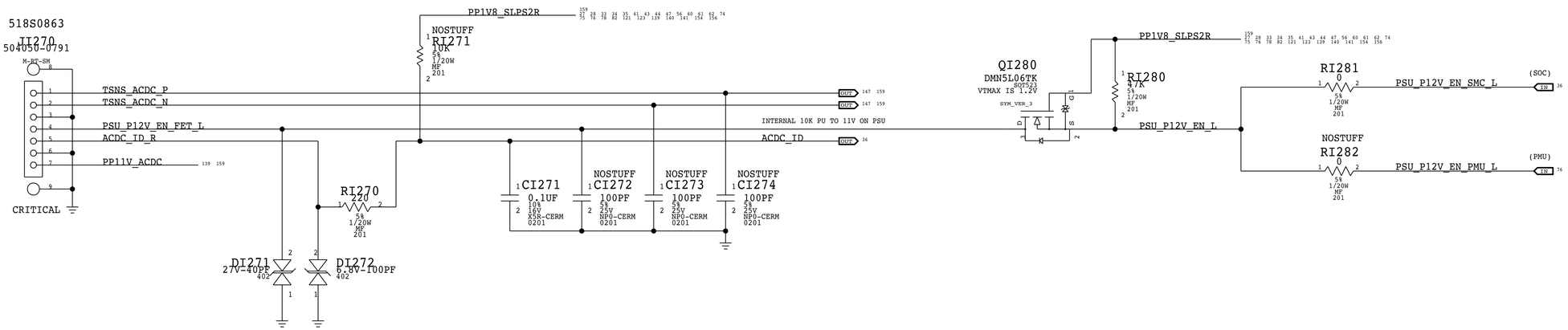
POR: 7 PIN SIGNAL + AUX POWER CONNECTOR



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=AMAN SYNC_DATE=06/22/2017

PAGE TITLE

POWER INPUT FROM AC/DC 3

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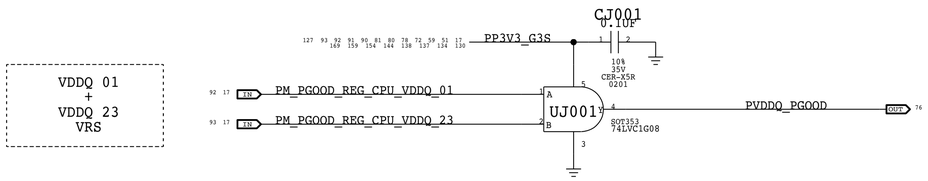
MEMORY POWER PGOOD



Power Sequencing requirements

System:

1. 12V_ACDC -> 3V42G3H -> 12V_S5/12V_S5_SSD -> 3V3_S5 -> 1V0_S5 -> 5V_S4/3V3_S4 -> 1V0_S3

Intel CPU:

2. 1V0_S3 -> 2V5_S3 -> VDDQ_S3 -> 12V_S0 -> 5V_S0 -> 3V3_S0 -> GPU Rails -> VCCIO_S0-> VCC_CPU_S0 (VCCGT & VCCSA)

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

POWER SEQUENCING S3

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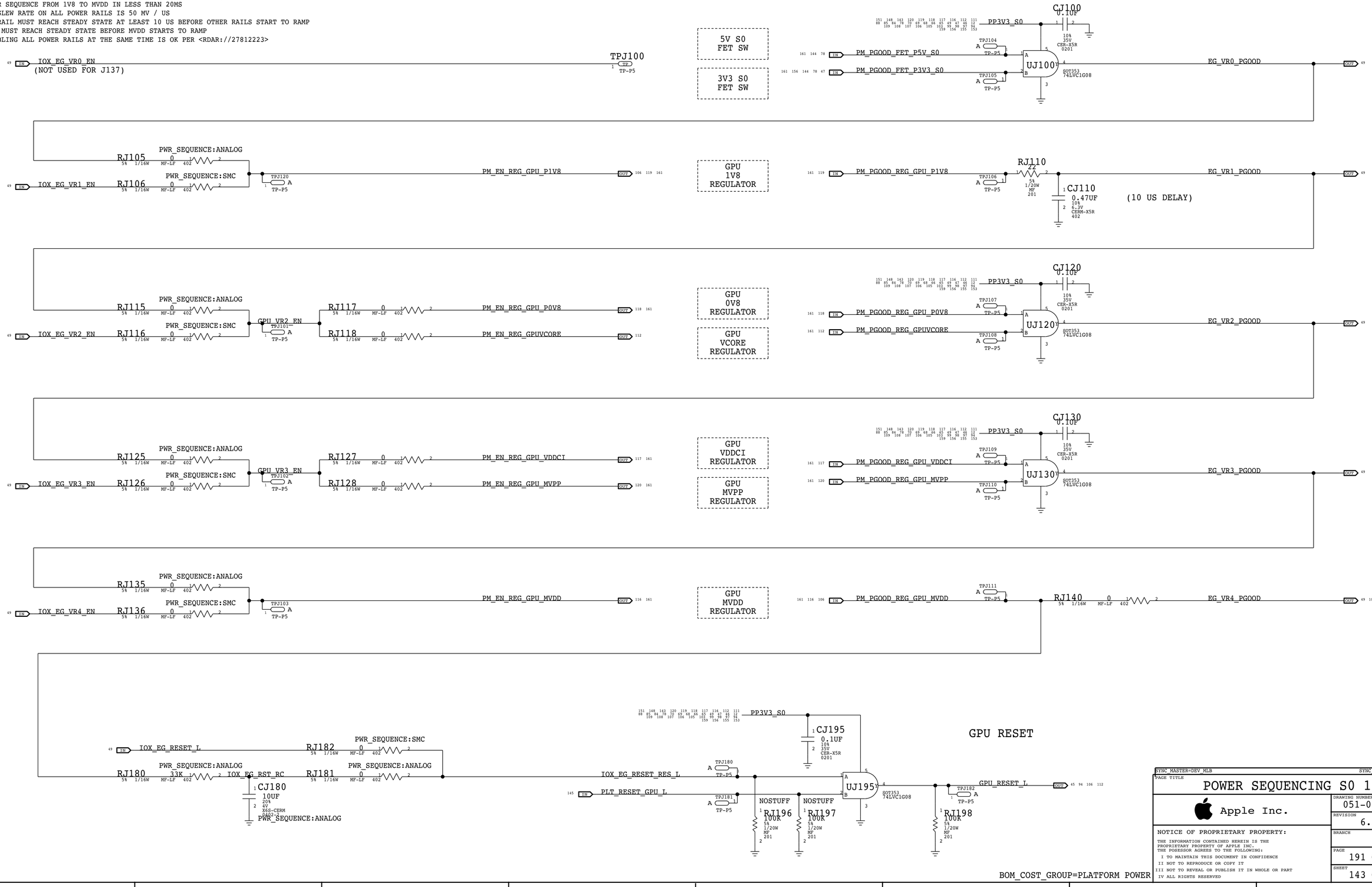
ALL POWER ENABLE AND POWER GOOD SIGNALS ARE 3V3 SIGNALS
POWER SEQUENCING REQUIREMENTS
AMD GPU:
12V_S0 -> 5V_S0 ->3V3_S0 -> 1V8(VDD_CT) -> 0V8 -> GPUCORE (VDDC) -> VDDCI -> MVPP -> MVDD
POWER SEQUENCE FROM 1V8 TO MVDD IN LESS THAN 20MS
MAX SLEW RATE ON ALL POWER RAILS IS 50 MV / US
1V8 RAIL MUST REACH STEADY STATE AT LEAST 10 US BEFORE OTHER RAILS START TO RAMP
MVPP MUST REACH STEADY STATE BEFORE MVDD STARTS TO RAMP
DISABLING ALL POWER RAILS AT THE SAME TIME IS OK PER <RDAR://27812223>



SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE
POWER SEQUENCING S0 1

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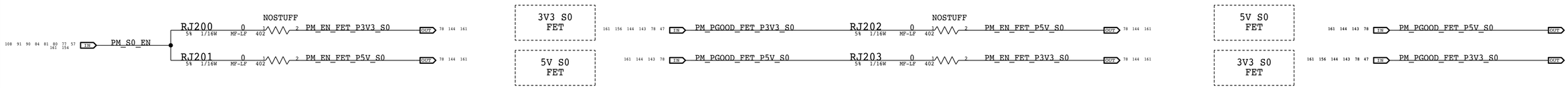
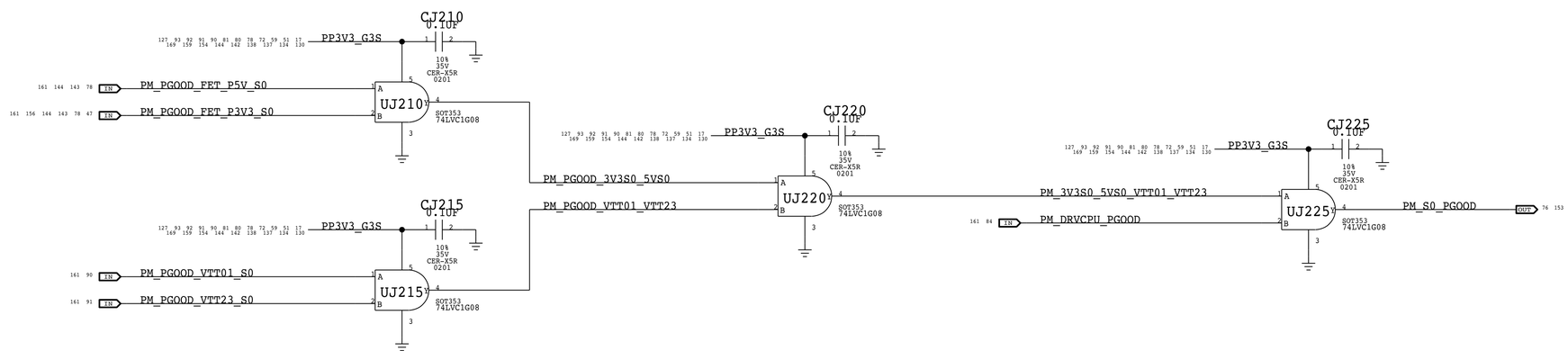
3V3 AND 5V S0



S0 PGOOD GENERATION



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

POWER SEQUENCING S0 2

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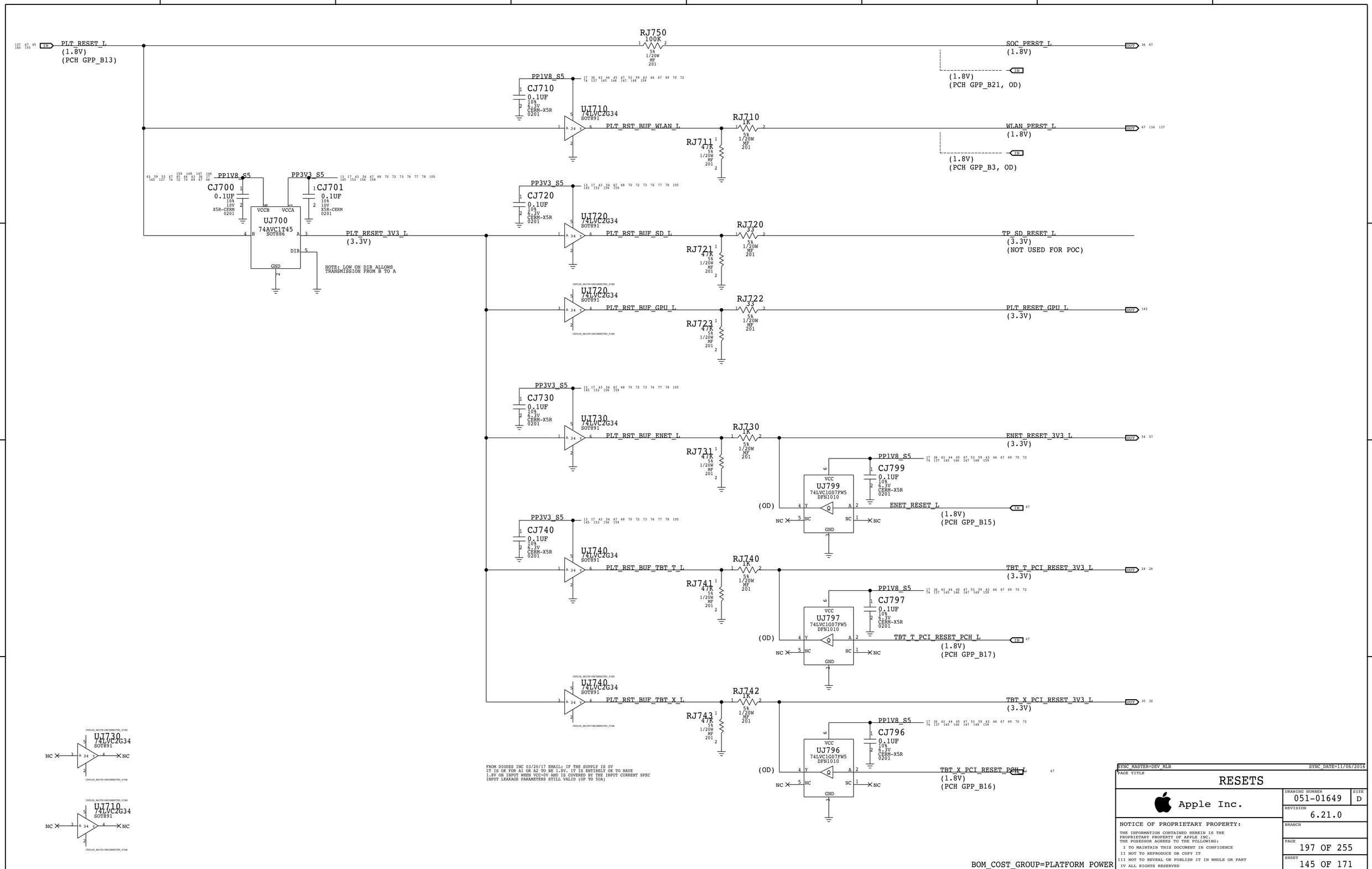
PLT_RESET_L
(1.8V)
(PCH GPP_B13)
RJ750
100K
SOC_PERST_L
(1.8V)
(1.8V)
(PCH GPP_B21, OD)
PP1V8_S5
CJ710
0.1UF
UJ710
74LVC2G34
SOT891
PLT_RST_BUF_WLAN_L
RJ710
1K
RJ711
47K
WLAN_PERST_L
(1.8V)
(1.8V)
(PCH GPP_B3, OD)
PP1V8_S5
CJ700
0.1UF
PP3V3_S5
CJ701
0.1UF
UJ700
74AVC1T45
SOT886
VCCB
VCCA
DIR
GND
PLT_RESET_3V3_L
(3.3V)
NOTE: LOW ON DIR ALLOWS
TRANSMISSION FROM B TO A
PP3V3_S5
CJ720
0.1UF
UJ720
74LVC2G34
SOT891
PLT_RST_BUF_SD_L
RJ720
33
RJ721
47K
TP_SD_RESET_L
(3.3V)
(NOT USED FOR POC)
UJ720
74LVC2G34
SOT891
PLT_RST_BUF_GPU_L
RJ722
33
RJ723
47K
PLT_RESET_GPU_L
(3.3V)
PP3V3_S5
CJ730
0.1UF
UJ730
74LVC2G34
SOT891
PLT_RST_BUF_ENET_L
RJ730
1K
RJ731
47K
ENET_RESET_3V3_L
(3.3V)
PP1V8_S5
CJ799
0.1UF
UJ799
74LVC1G07FW5
DFN1010
VCC
GND
(OD)
NC
ENET_RESET_L
(1.8V)
(PCH GPP_B15)
PP3V3_S5
CJ740
0.1UF
UJ740
74LVC2G34
SOT891
PLT_RST_BUF_TBT_T_L
RJ740
1K
RJ741
47K
TBT_T_PCI_RESET_3V3_L
(3.3V)
PP1V8_S5
CJ797
0.1UF
UJ797
74LVC1G07FW5
DFN1010
TBT_T_PCI_RESET_PCH_L
(1.8V)
(PCH GPP_B17)
UJ740
74LVC2G34
SOT891
PLT_RST_BUF_TBT_X_L
RJ742
1K
RJ743
47K
TBT_X_PCI_RESET_3V3_L
(3.3V)
PP1V8_S5
CJ796
0.1UF
UJ796
74LVC1G07FW5
DFN1010
TBT_X_PCI_RESET_PCH_L
(1.8V)
(PCH GPP_B16)
UJ730
74LVC2G34
SOT891
UJ710
74LVC2G34
SOT891
FROM DIODES INC 03/20/17 EMAIL: IF THE SUPPLY IS 0V
IT IS OK FOR A1 OR A2 TO BE 1.8V. IT IS ENTIRELY OK TO HAVE
1.8V ON INPUT WHEN VCC=0V AND IS COVERED BY THE INPUT CURRENT SPEC
INPUT LEAKAGE PARAMETERS STILL VALID (UP TO 5UA)
BOM_COST_GROUP=PLATFORM POWER
SYNC_MASTER=DEV_MLB
SYNC_DATE=11/06/2016
PAGE TITLE
RESETS
Apple Inc.
DRAWING NUMBER
051-01649
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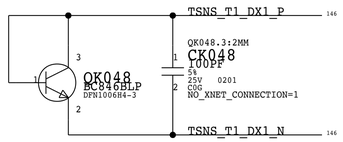
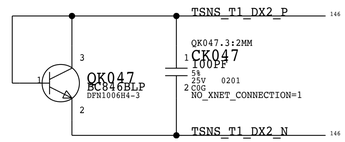
THERMAL DIODE: CPU PROX (KEY TC0P)

Placement Note:
Place QK048 under the CPU



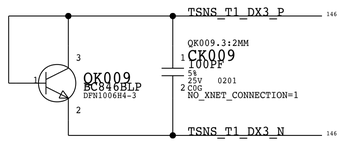
THERMAL DIODE: CPU VR PROX 1 (KEY TC1P)

Placement Note:
Place QK047 near CPU Core VR input hot spot



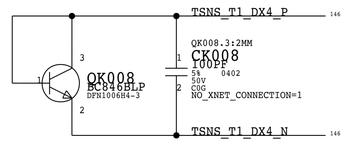
THERMAL DIODE: CPU VR PROX 2 (KEY TC2P)

Placement Note:
Place QK009 near CPU Core VR output hot spot



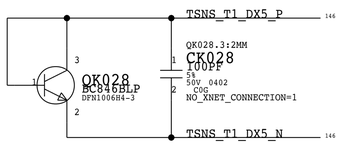
THERMAL DIODE: DIMM CONN 0 (KEY TM0P)

Place QK008 near DIMM CONN CH0 (J2100)



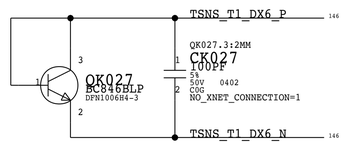
THERMAL DIODE: DIMM CONN 1 (KEY TM1P)

Place QK028 near DIMM CONN CH1 (J2200)



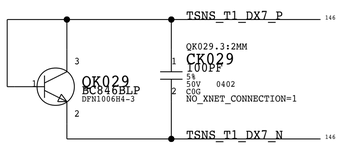
THERMAL DIODE: DIMM CONN 2 (KEY TM2P)

Place QK027 near DIMM CONN CH2 (J2300)



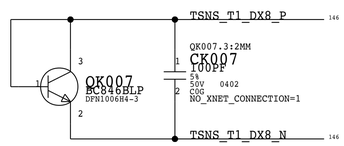
THERMAL DIODE: DIMM CONN 3 (KEY TM3P)

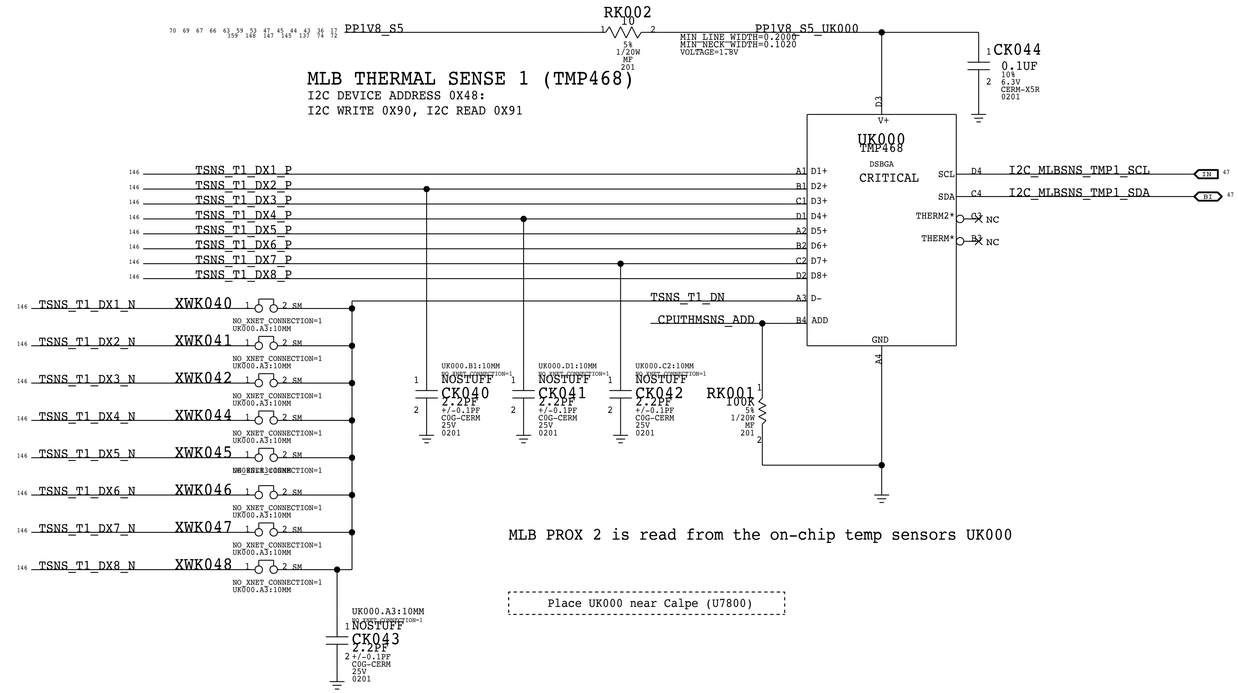
Place QK029 near DIMM CONN CH3 (J2400)



THERMAL DIODE: MLB PROX 1 - AC/DC PLUG (KEY TA0P)

Place QK007 near AC/DC PLUG





MLB PROX 2 is read from the on-chip temp sensors UK000

Place UK000 near Calpe (U7800)

J135 SCHEMATC SAYS NEED DIFFERENT APN 353S2908??

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS THERMAL 1

Apple Inc.

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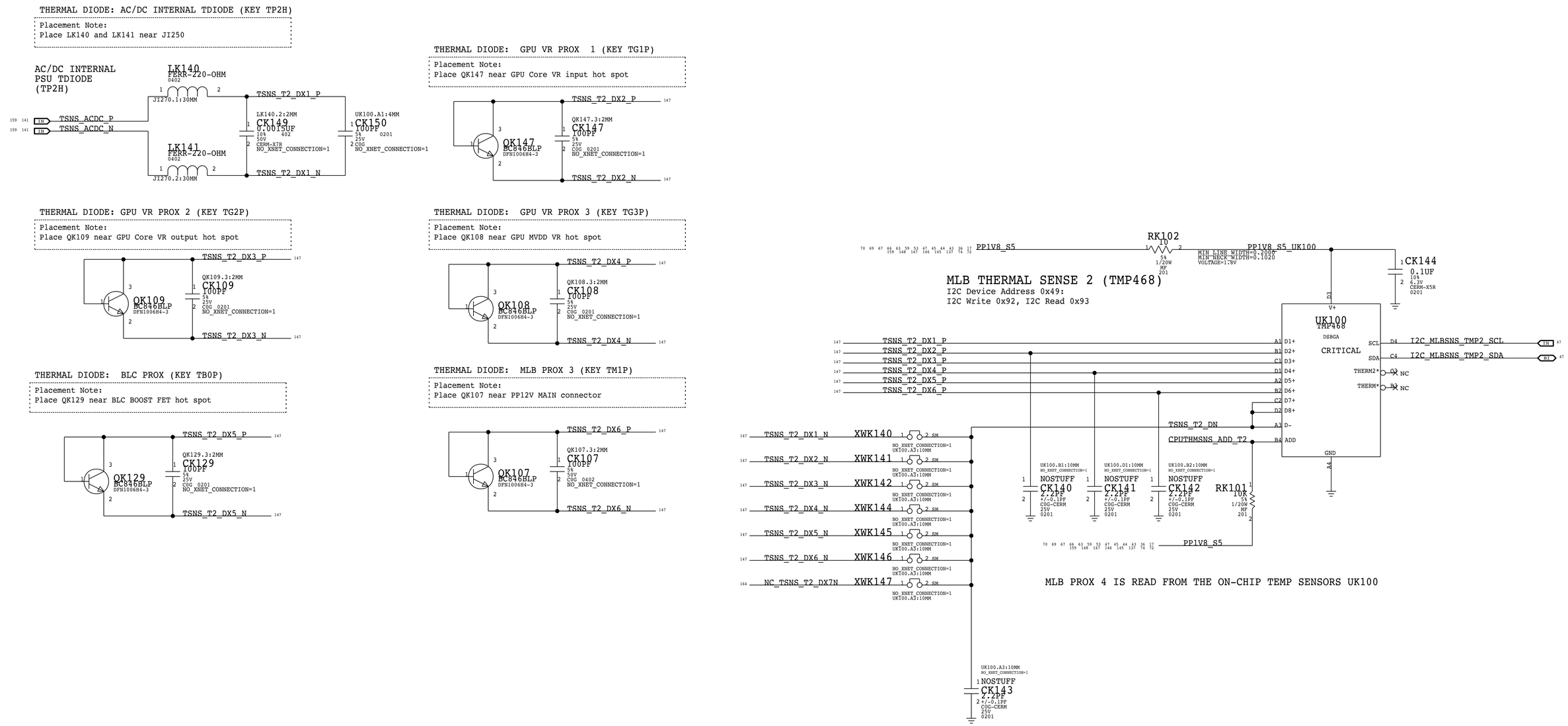

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS THERMAL 2

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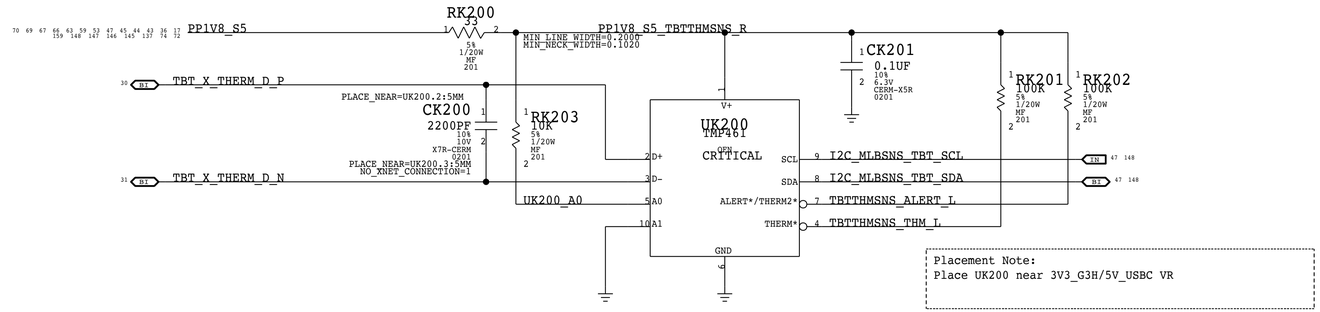
Thermal Sensor A: Thunderbolt Die

I2C Write: 0xD8, I2C Read: 0xD9

THERMAL DIODE: TBT DIE (TBT1 - KEY TI0D)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to TitanRidge pin V9.

I2C Device (UK200) Address 0X4A:
I2C Write 0x94, I2C Read 0x95



Placement Note:
Place UK200 near 3V3_G3H/5V_USBC VR

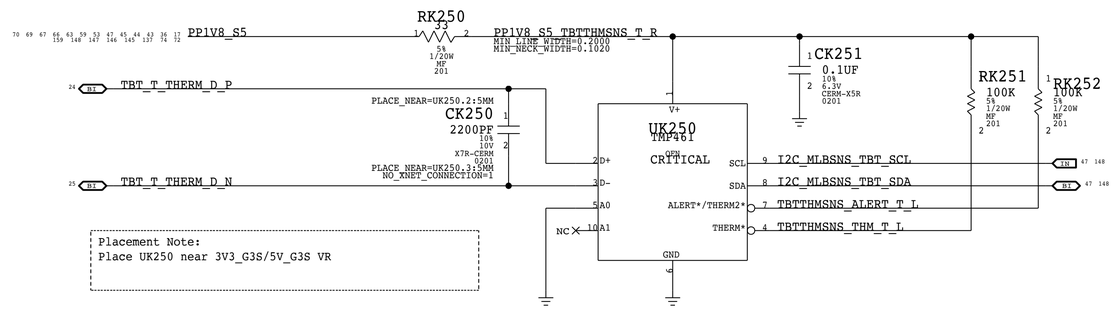
Thermal Sensor B: Thunderbolt Die

I2C Write: 0xB8, I2C Read: 0xB9

THERMAL DIODE: TBT DIE (TBT2 - KEY TI1D)

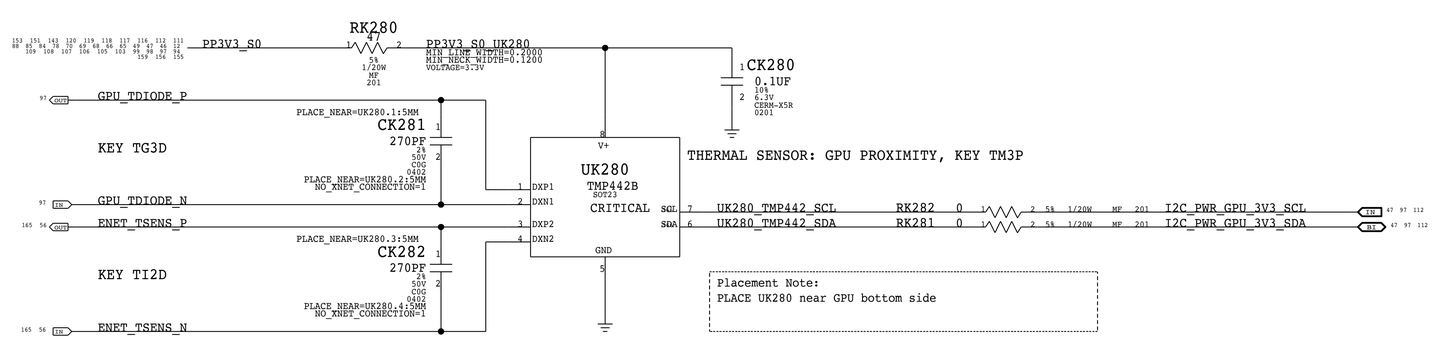
Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.

I2C Device (UK250) Address 0x4B:
I2C Write 0x96, I2C Read 0x97



Placement Note:
Place UK250 near 3V3_G3S/5V_G3S VR

GPU THERMAL - KEY TM3P



THERMAL SENSOR: GPU PROXIMITY, KEY TM3P

Placement Note:
PLACE UK280 near GPU bottom side

I2C WRITE: 0X9A, I2C READ: 0X9B
I2C DEVICE (UK280) ADDRESS 0X4D

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SENSORS THERMAL 3

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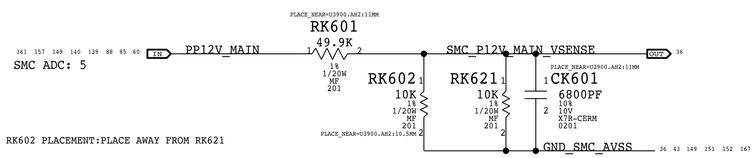
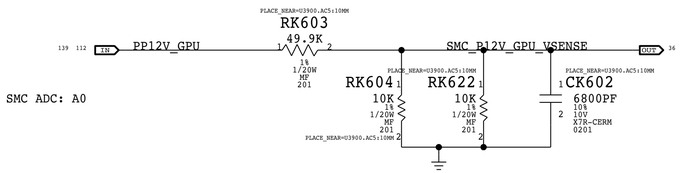
AC/DC 12V MAIN LOW SIDE VOLTAGE SENSE (KEY VD2R)

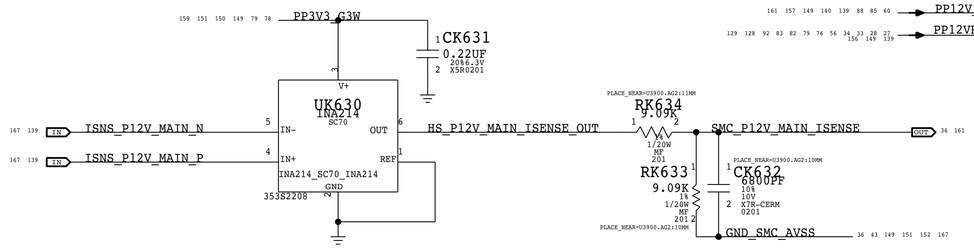


AC/DC 12V GPU HIGH SIDE VOLTAGE SENSE (KEY VG2R)



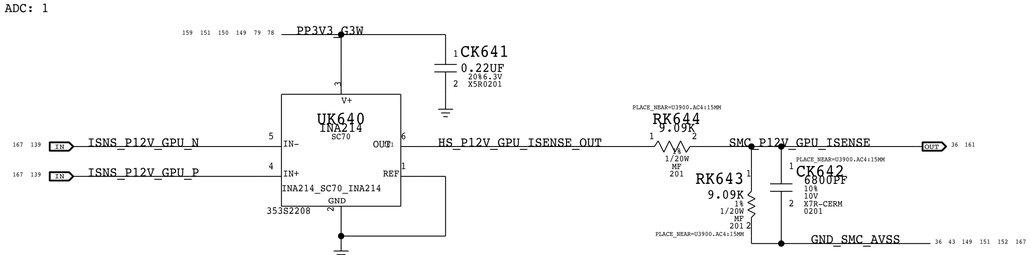
PP12V MAIN HIGH SIDE CURRENT SENSE (KEY ID2M)

GAIN: 100X, EDP: 30 A
RSENSE: 0.00075 (RI010) OR RSENSE SHORT
VSENSE: 25 MV, RANGE: 33.33 A
SMC ADC: 0



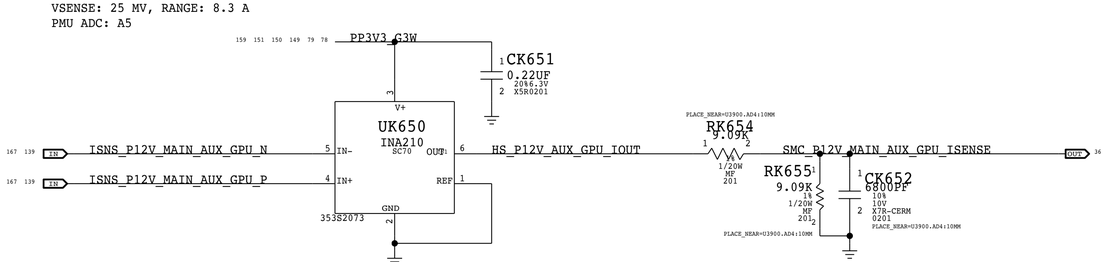
PP12V GPU HIGH SIDE CURRENT SENSE (KEY IG2R)

GAIN: 100X, EDP: 30 A
RSENSE: 0.00075 (RI000) OR RSENSE SHORT
VSENSE: 25 MV, RANGE: 33.33 A
SMC ADC: 1



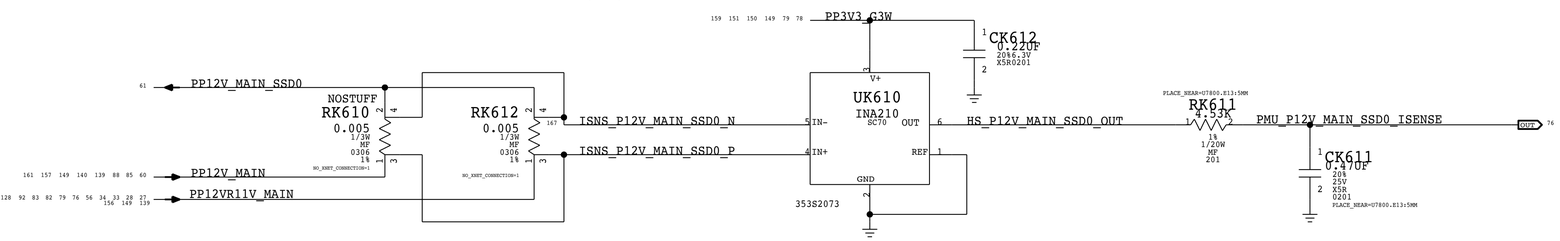
PP12V MAIN AUXILIARY GPU RAIL HIGH SIDE CURRENT SENSE (KEY IG2A)

GAIN: 100X, EDP: 6 A
RSENSE: 0.003 (RI050) OR RSENSE SHORT
VSENSE: 25 MV, RANGE: 8.3 A
PMU ADC: A5



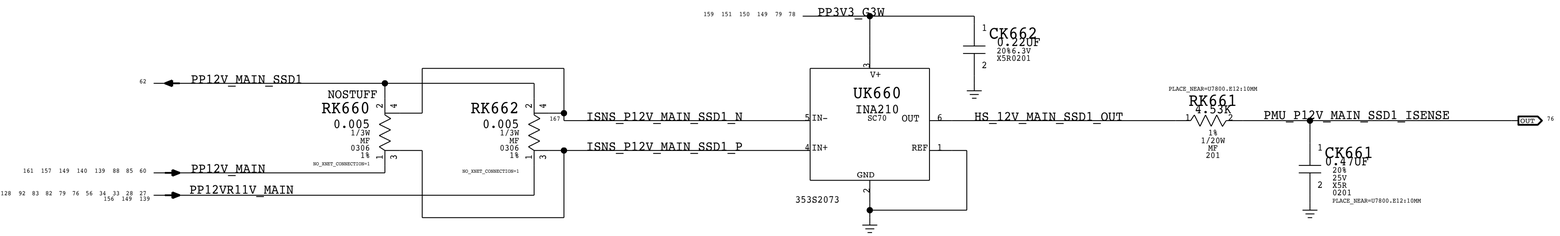
PP12V SSD0 HIGH SIDE CURRENT SENSE (KEY IH02)

GAIN: 200X, EDP: 0.5 A
RSENSE: 0.005 (RK610) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
PMU ADC: B1



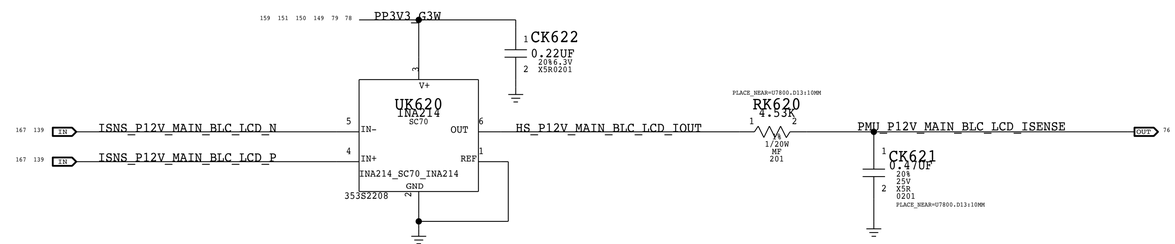
PP12V SSD1 HIGH SIDE CURRENT SENSE (KEY IH12)

GAIN: 200X, EDP: 0.5 A
RSENSE: 0.005 (RK660) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
PMU ADC: B2



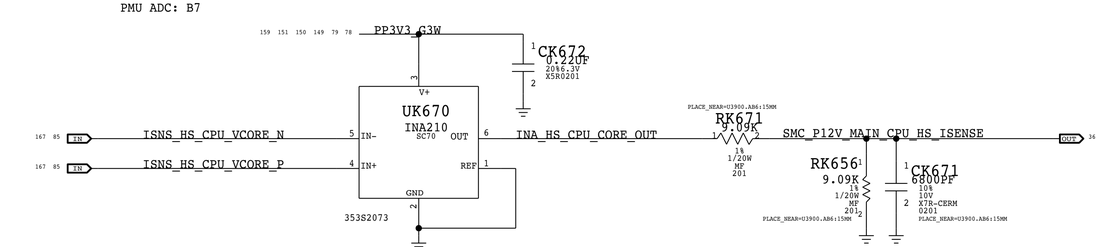
PP12V BACKLIGHT AND LCD HIGH SIDE CURRENT SENSE (KEY IB2R)

GAIN: 100X, EDP: 6 A
RSENSE: 0.003 (RI070) OR RSENSE SHORT
VSENSE: 25 MV, RANGE: 8.3 A
PMU ADC: B0



PP12V MAIN CPU HIGH SIDE CURRENT SENSE (KEY IC2R)

GAIN: 100X, EDP: 15 A
RSENSE: 0.005 (R9090) OR RSENSE SHORT
VSENSE: 25 MV, RANGE: 25 A
PMU ADC: B7



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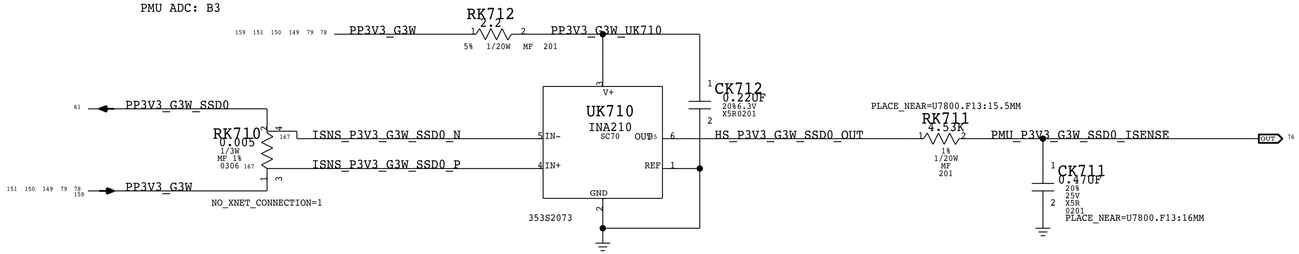
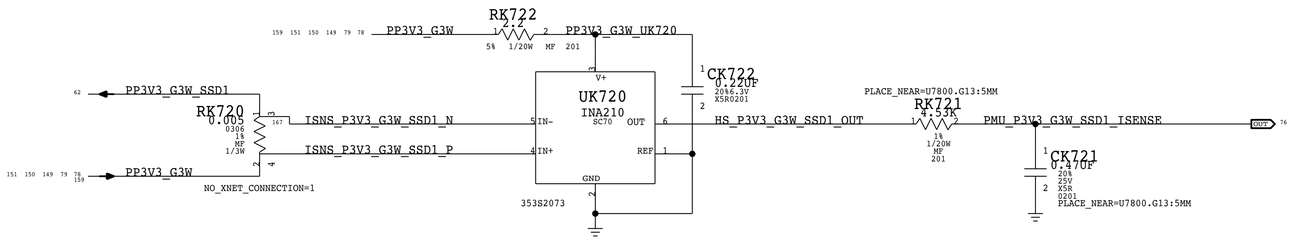
PP3V3_G3W_SSD0 HIGH SIDE CURRENT SENSE (KEY IH0R)

GAIN: 200X, EDP: 1.1 A
RSENSE: 0.005 (RK710) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
PMU ADC: B3



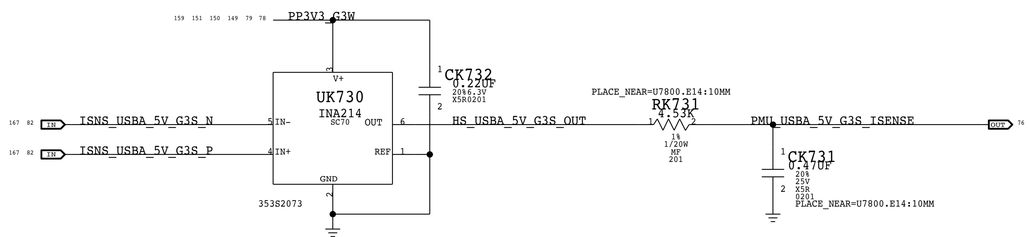
PP3V3_G3W_SSD1 HIGH SIDE CURRENT SENSE (KEY IH1R)

GAIN: 200X, EDP: 1.1 A
RSENSE: 0.005 (RK760) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
PMU ADC: B4



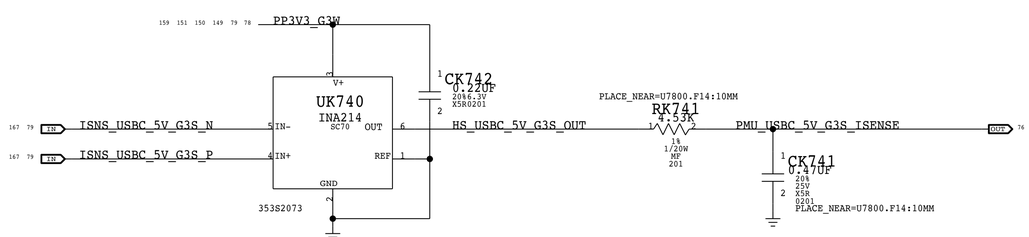
PP5V_G3S_USBA HIGH SIDE CURRENT SENSE (KEY II0R)

GAIN: 100X, EDP: 5.5 A
RSENSE: 0.003 (R8690) OR RSENSE SHORT
VSENSE: 25 MV, RANGE: 8.3 A
PMU ADC: A6



PP5V_G3S_USBC HIGH SIDE CURRENT SENSE (KEY II1R)

GAIN: 100X, EDP: 13 A
RSENSE: 0.001 (R8390) OR RSENSE SHORT
VSENSE: 25 MV, RANGE: 25 A
PMU ADC: A7



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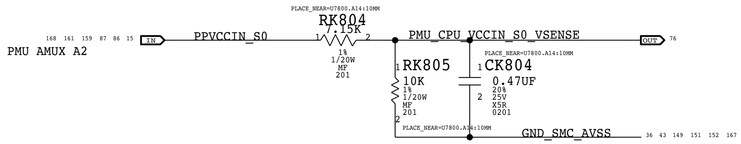
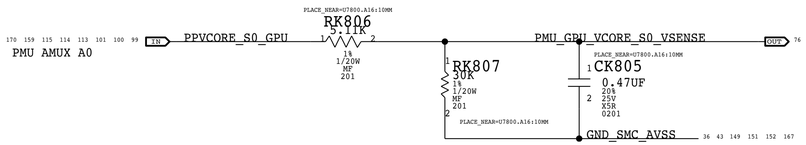
PPVCCIN CPU CORE VOLTAGE SENSE (KEY VC0C)

PPVCCIN RANGE: 1.5V - 2V



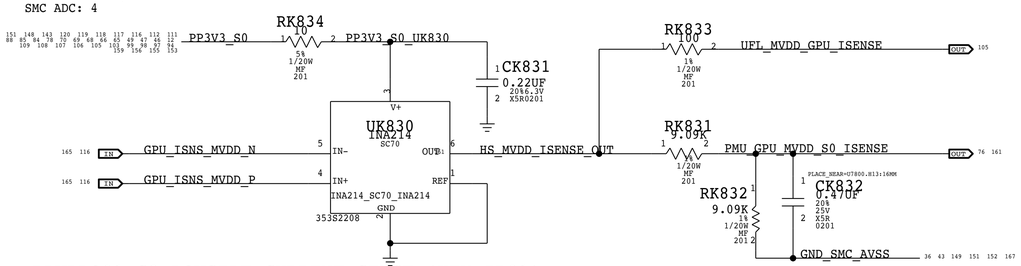
PPVCORE S0 GPU CORE VOLTAGE SENSE (KEY VG0C)

PPVCORE S0 GPU RANGE: 0.6V - 1.2V



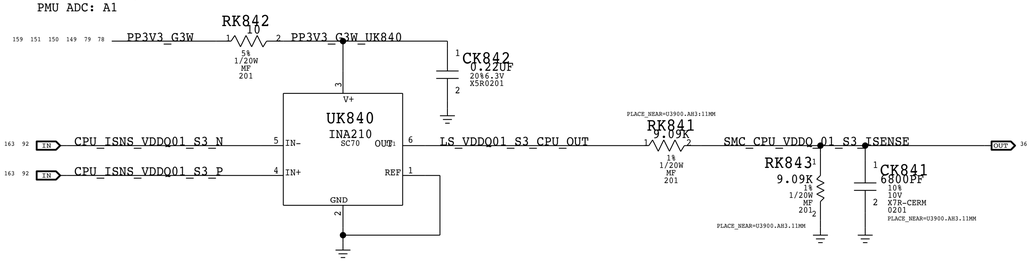
MVDD GPU LOWSIDE CURRENT SENSE (KEY IG0M)

GAIN: 100X, EDP: 30 A
RSENSE: 0.0005 (RD400) OR RSENSE SHORT
VSENSE: 25 MV, RANGE: 50 A
SMC ADC: 4



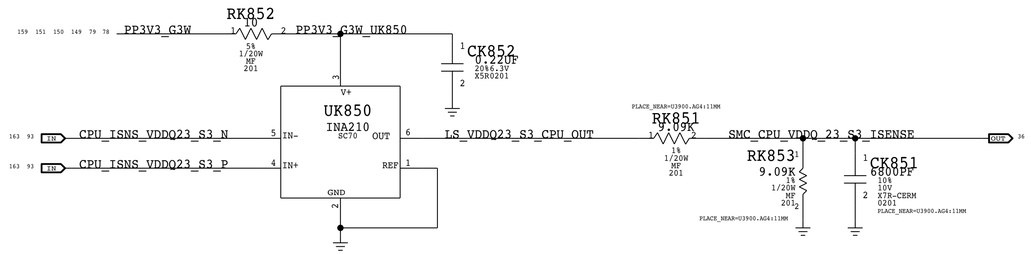
PPVDDQ01_S3 LOWSIDE CURRENT SENSE (KEY IR01)

GAIN: 100X, EDP: 25 A
RSENSE: 0.0005 (R9800) OR RSENSE SHORT
VSENSE: 25 MV, RANGE:50 A
PMU ADC: A1



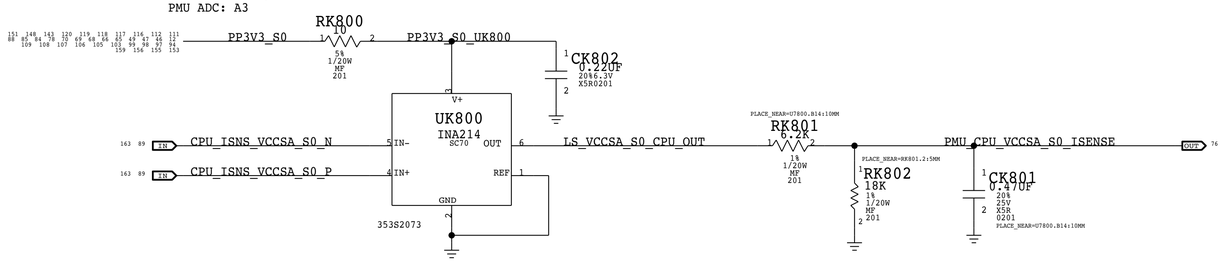
PPVDDQ23_S3 LOWSIDE CURRENT SENSE (KEY IC23)

GAIN: 100X, EDP: 25 A
RSENSE: 0.0005 (R9900) OR RSENSE SHORT
VSENSE: 25 MV, RANGE:50 A
PMU ADC: A2



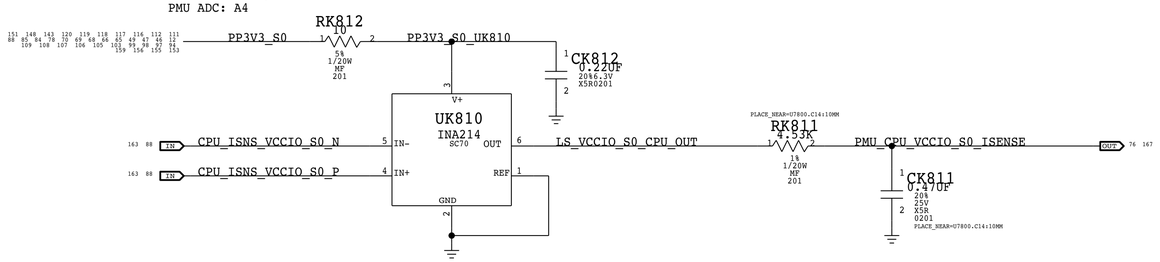
PPVCCSA_S0 LOWSIDE CURRENT SENSE (KEY IC0S)

GAIN: 100X, EDP: 15 A
RSENSE: 0.001 (R9525) OR RSENSE SHORT
VSENSE: 25 MV, RANGE:25 A
PMU ADC: A3



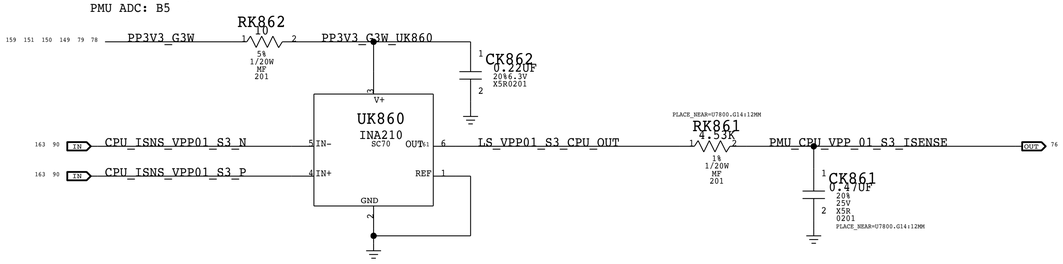
PPVCCIO_S0 LOWSIDE CURRENT SENSE (KEY IC0I)

GAIN: 200X, EDP: 12 A
RSENSE: 0.001 (R9400) OR RSENSE SHORT
VSENSE: 13 MV, RANGE:12.5 A
PMU ADC: A4



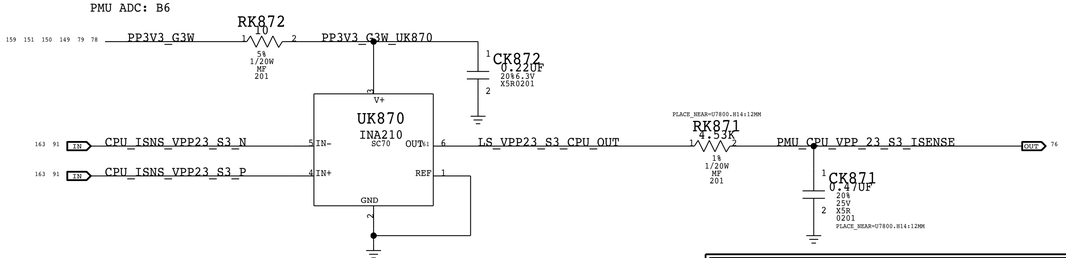
PPVPP01_S3 LOWSIDE CURRENT SENSE (KEY IM0P)

GAIN: 200X, EDP: 4 A
RSENSE: 0.001 (R9610) OR RSENSE SHORT
VSENSE: 13 MV, RANGE:12.5 A
PMU ADC: B5



PPVPP23_S3 LOWSIDE CURRENT SENSE (KEY IM1P)

GAIN: 200X, EDP: 4 A
RSENSE: 0.001 (R9710) OR RSENSE SHORT
VSENSE: 13 MV, RANGE:12.5 A
PMU ADC: B6



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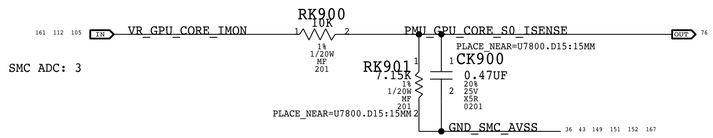
GPU CORE CURRENT SENSE VIA IMON (KEY IG0C)

CPU CORE CURRENT RANGE: 432A

VOLTAGE RANGE: INPUT 2.16V/432A - OUTPUT 2.16 *7.15/(10+7.15) = 2.2mV

VSENSE: 2.2mV/A

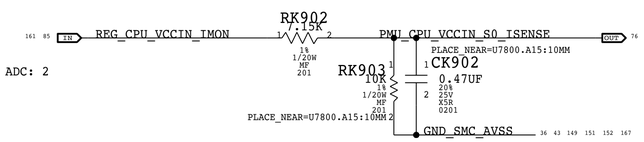


SMC ADC: 3

CPU CORE CURRENT SENSE VIA IMON (KEY IC0C)

CPU CORE CURRENT RANGE: 200A

VSENSE: 1.25 MV/A



SMC ADC: 2

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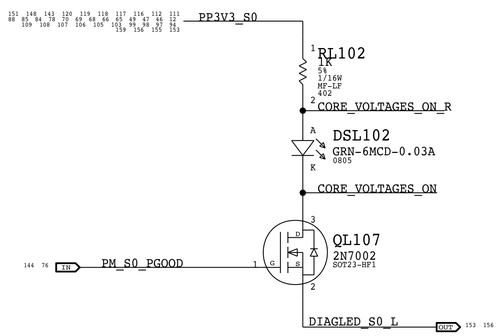
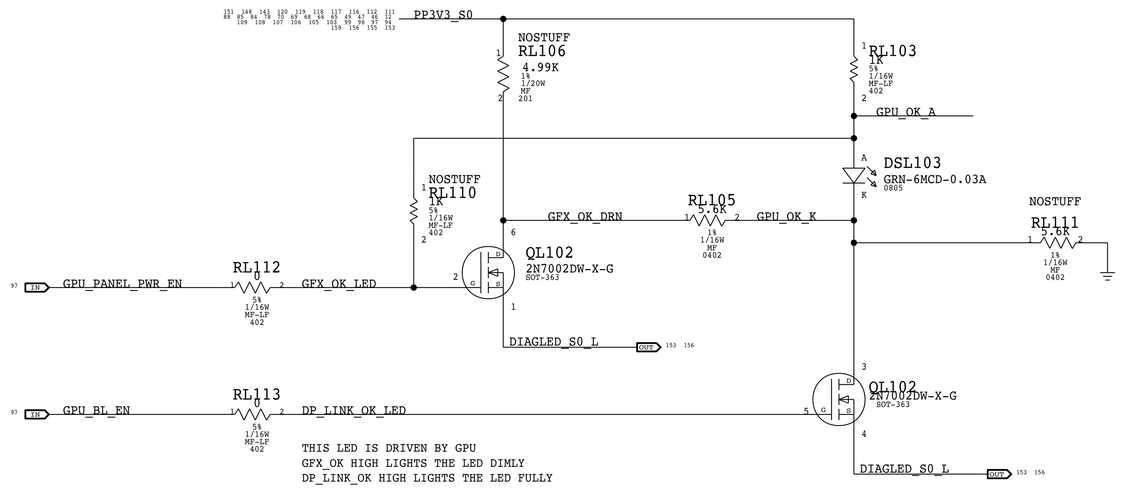
POR LED LIST TRACKED AT <RDAR://30685511>
NOTE, NONE OF THESE WILL TURN ON BY DEFAULT UNLESS SWITCH SL550 IS PUSHED

S0 PGOOD LED

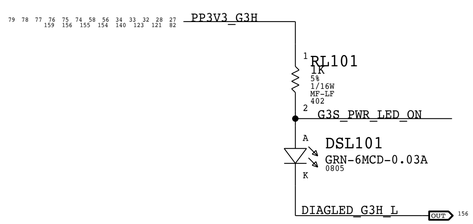


GPU OK LED

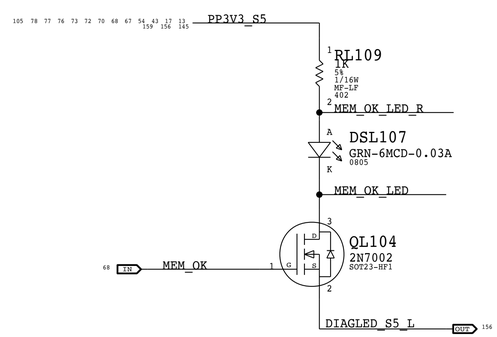


THIS LED IS DRIVEN BY GPU
GFX_OK HIGH LIGHTS THE LED DIMLY
DP_LINK_OK HIGH LIGHTS THE LED FULLY

G3H PWR LED

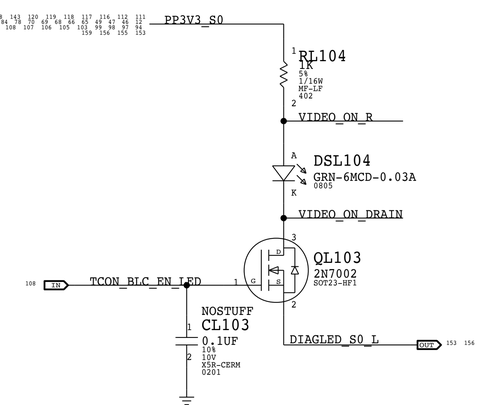


MEM_OK LED



THIS LED IS LIT WHEN THE MEMORY TEST COMPLETES OK

TCON OK LED



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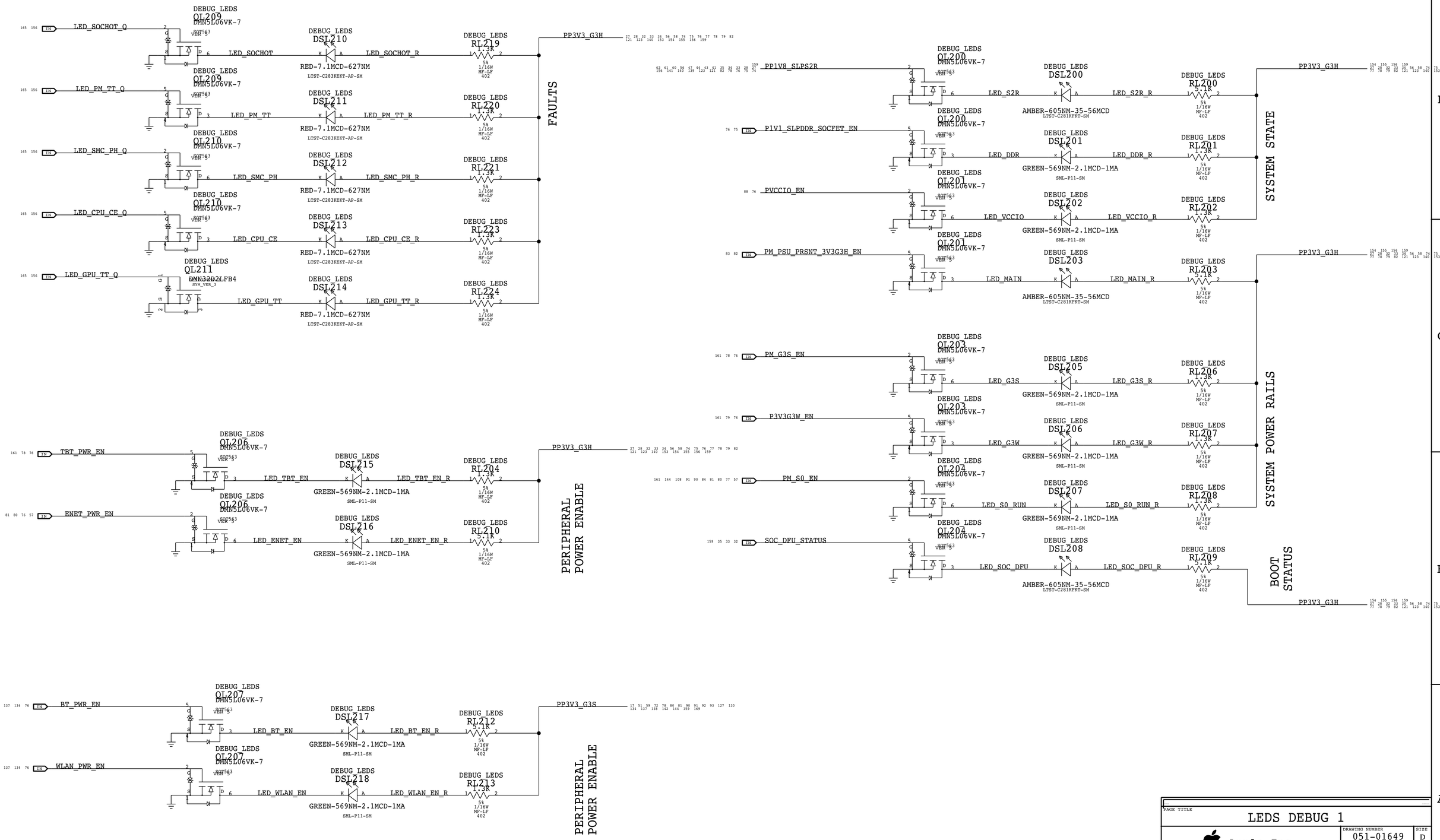

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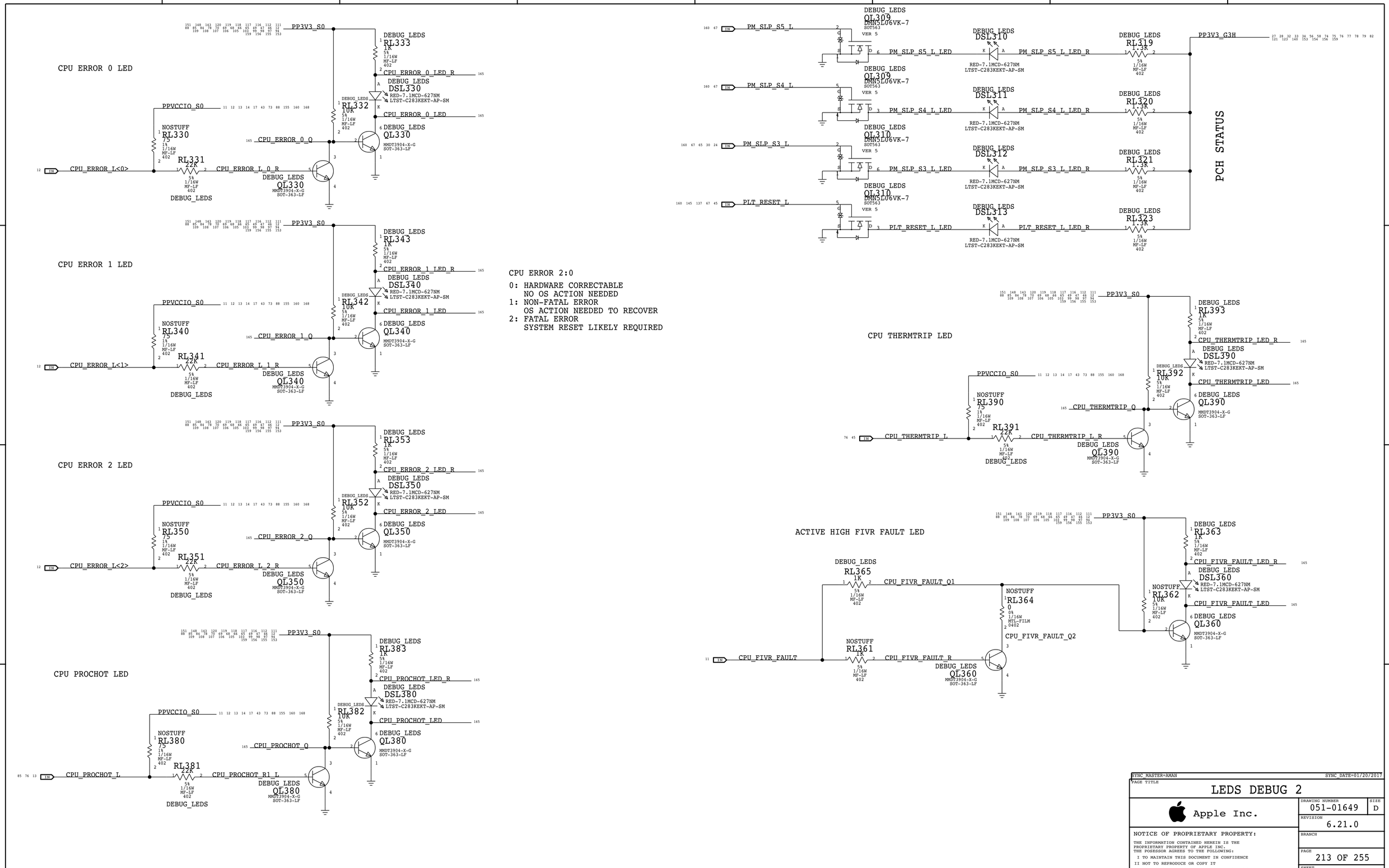

SYNC_MASTER=AMAN SYNC_DATE=01/20/2017

PAGE TITLE

LEDS DEBUG 2

Apple Inc.

DRAWING NUMBER 051-01649 SIZE D

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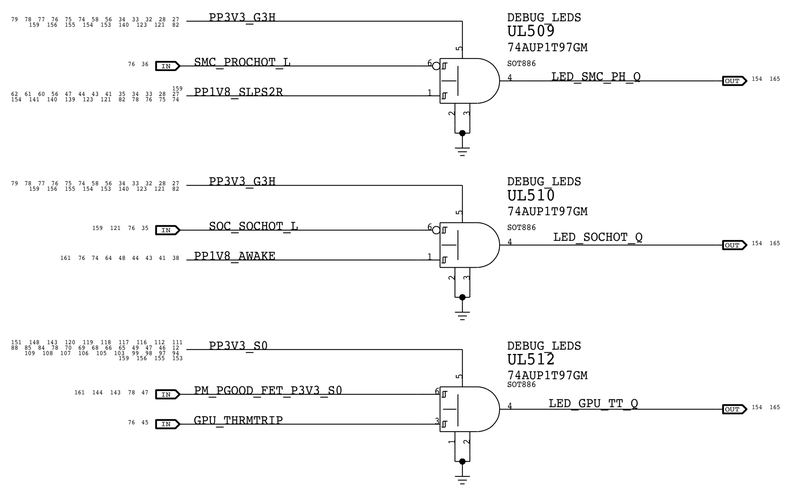
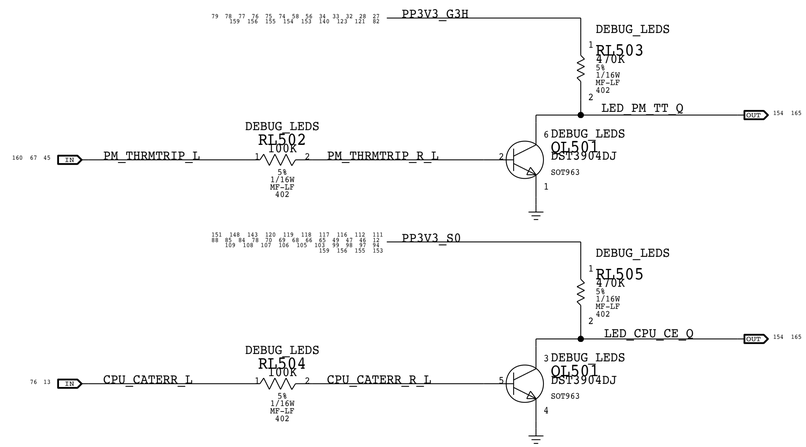
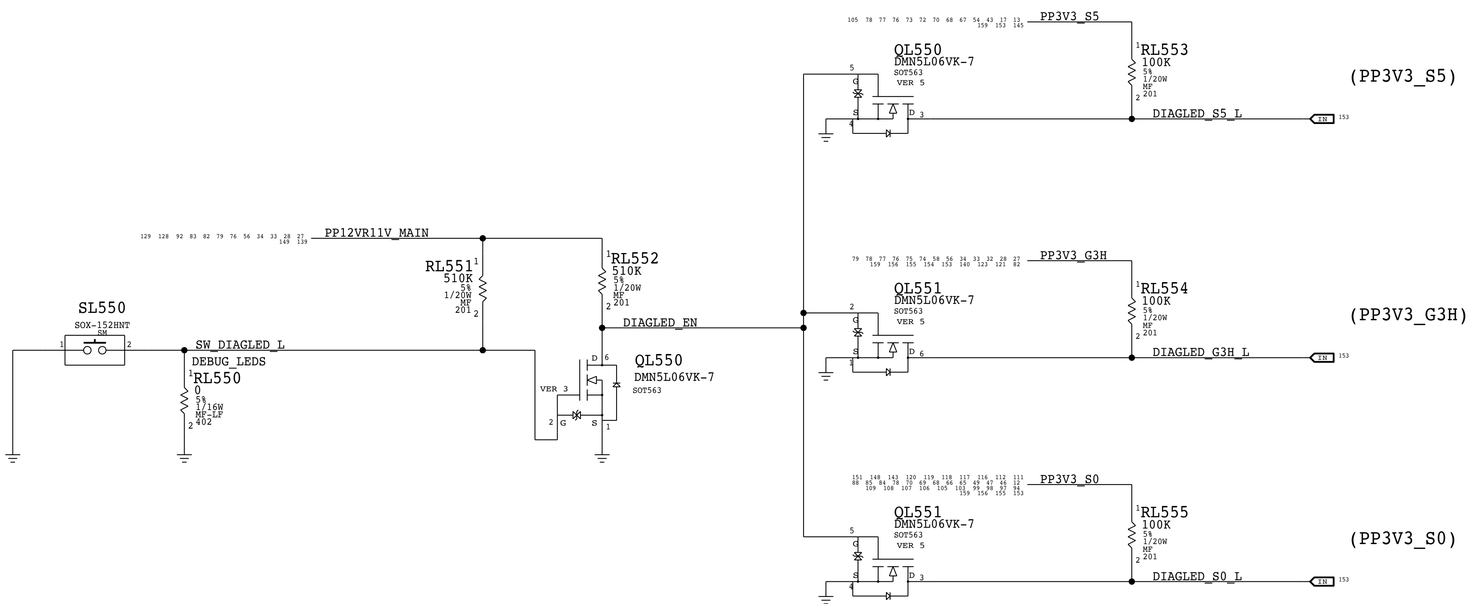




LED ENABLE SWITCH FOR POR LEDS



BOM_COST_GROUP=DEBUG

PAGE TITLE
LEDS SUPPORT

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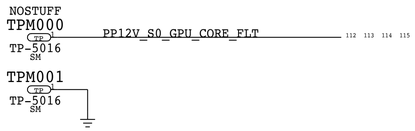

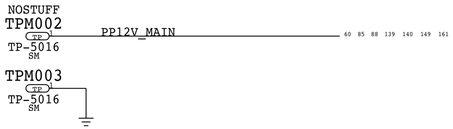

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
PSU RESISTANCE MEASUREMENT

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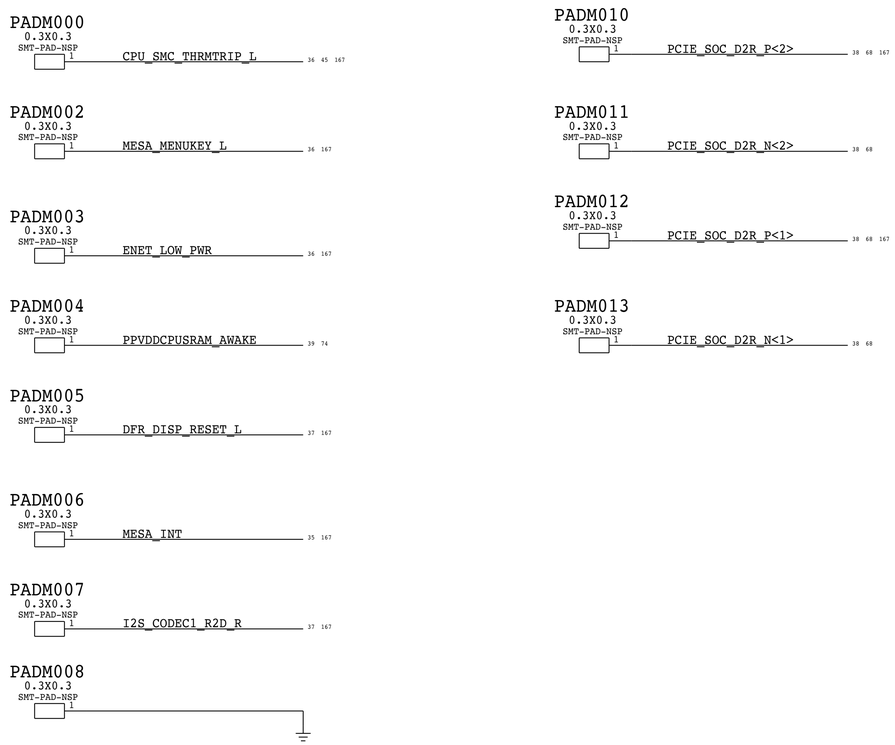
SMALL PADS TO EXPOSE NETS IN SOC AREA WHERE TP WON'T FIT



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
TEST PADS FOR SOC AREA

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DFU TEST POINTS <RDAR://30758642>

POWER SEQUENCE

TPN070	1 TP-P5	PP3V3_G3H	27 28 32 33 34 56 58 74 75 76 77 78 79 82 121 123 140 153 154 155 156
TPN071	1 TP-P5	PP3V3_G3W	78 79 149 150 151
TPN072	1 TP-P5	PP3V3_G3S	17 51 59 72 78 80 81 90 91 92 93 127 130 134 137 138 142 144 154 169
TPN073	1 TP-P5	PP1V8_SLPS2R	27 28 33 34 35 41 43 44 47 56 60 61 62 74 75 76 78 82 121 123 139 140 141 154 156
TPN074	1 TP-P5	PP0V8Z_SLPDDR	39 74 122
TPN075	1 TP-P5	PP1V2_AWAKE	41 75
TPN076	1 TP-P5	PPVDDCPU_AWAKE_SOC	39 74 122 126
TPN077	1 TP-P5	PP1V8_S5	17 36 43 44 45 47 53 59 63 66 67 69 70 72 74 137 145 146 147 148
TPN078	1 TP-P5	PP1V0_S0	13 45 74 76
TPN079	1 TP-P5	PP3V3_S0	116 117 118 119 120 143 168 151 153 155 17 46 47 49 65 66 68 69 70 78 84 85 86 94 97 98 99 102 105 106 107 108 109 111 112
TPN090	1 TP-P5	PPVCCIN_S0	15 86 87 151 161 168 156
TPN091	1 TP-P5	PPVCORE_S0_GPU	99 100 101 113 114 115 151 170

POWER

TPN030	1 TP-P5	PP12V_ACDC_GPU	139
TPN031	1 TP-P5		
TPN032	1 TP-P5	PP12V_ACDC	139
TPN033	1 TP-P5		
TPN034	1 TP-P5	PP11V_ACDC	139 141
TPN035	1 TP-P5	TSNS_ACDC_P	141 147
TPN036	1 TP-P5	TSNS_ACDC_N	141 147
TPN037	1 TP-P5	PSU_P12V_EN_FET_L	140 141
TPN038	1 TP-P5	ACDC_ID_R	141
TPN039	1 TP-P5		
TPN080	1 TP-P5	IMAC_PWR_BTN_R	121
TPN081	1 TP-P5	PP5V_G3S_USBC	26 27 28 32 33 34 79
TPN082	1 TP-P5	PP5V_G3S_USBA	52 53 82
TPN024	1 TP-P5	PP3V3_S5	13 17 43 54 67 68 70 72 73 76 77 78 105 145 153 156

DEBUG MOJO

TPN040	1 TP-P5	SMC_DEBUGPRT_RX	26 36 123
TPN041	1 TP-P5	SMC_DEBUGPRT_TX	26 36 123
TPN042	1 TP-P5	PCH_DEBUG_UART_R2D	34 69 72
TPN043	1 TP-P5	PCH_DEBUG_UART_D2R	34 69 72
TPN044	1 TP-P5		

DFU

TPN045	1 TP-P5	SOC_USB_VBUS	32 35 121
TPN046	1 TP-P5	USB_SOC_N	35 121
TPN047	1 TP-P5	USB_SOC_P	35 121
TPN049	1 TP-P5	PMU_ACTIVE_READY	32 33 35 76
TPN050	1 TP-P5	SOC_FORCE_DFU	32 33 35 76 121
TPN051	1 TP-P5	SOC_DFU_STATUS	32 33 35 154
TPN054	1 TP-P5	SOC_DOCK_CONNECT	33 34 36
TPN055	1 TP-P5	SOC_DEBUGPRT_TX	37 123
TPN056	1 TP-P5	SOC_DEBUGPRT_RX	37 123
TPN057	1 TP-P5		
TPN062	1 TP-P5	USBC_XA_SBU1	29 33 161
TPN063	1 TP-P5	USBC_XA_SBU2	29 33 161
TPN064	1 TP-P5	USBC_XA_CC1	29 33 161
TPN065	1 TP-P5	USBC_XA_CC2	29 33 161
TPN066	1 TP-P5	PPVBUS_USBC_XA	29 32 33 161
TPN067	1 TP-P5		
TPN068	1 TP-P5		
TPN093	1 TP-P5	SOC_SWD_MUX_SEL	32 69
TPN069	1 TP-P5	SOC_SOCHOT_L	35 76 121 156
TPN083	1 TP-P5	DFUMUX_SEL	121

ICT TEST VIAS DUE TO PACKAGE KEEPOUT CONSTRAINTS AT USB-C AREA

(USBC_XA_USB_DBG_TOP_P)
(USBC_XA_USB_DBG_TOP_N)
(USBC_XA_USB_DBG_BOT_P)
(USBC_XA_USB_DBG_BOT_N)
(USBC_XB_USB_TOP_P)
(USBC_XB_USB_TOP_N)
(USBC_XB_USB_BOT_P)
(USBC_XB_USB_BOT_N)

FAN

TPN099	1 TP-P5	SMC_FAN_0_PWM_RES	60
TPN098	1 TP-P5	SMC_FAN_0_TACH	36 60
TPN0A0	1 TP-P5	SMC_FAN_1_PWM_RES	60
TPN0A1	1 TP-P5	SMC_FAN_1_TACH	36 60
TPN097	1 TP-P5	PP12V_S0_FAN_0_FILT	60 161
TPN096	1 TP-P5	PP12V_S0_FAN_1_FILT	60 161
TPN095	1 TP-P5		
TPN094	1 TP-P5		

MISC / BACK UP

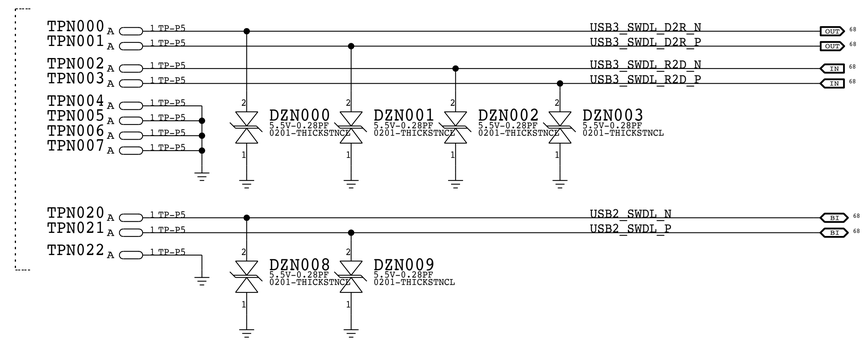
TPN060	1 TP-P5	USB_SOC_TYPEC_P	32 121
TPN061	1 TP-P5	USB_SOC_TYPEC_N	32 121
TPN052	1 TP-P5	UPC_XB_DBG3	34
TPN053	1 TP-P5	UPC_XB_DBG4	34

PLACED ON TOP

SWDL

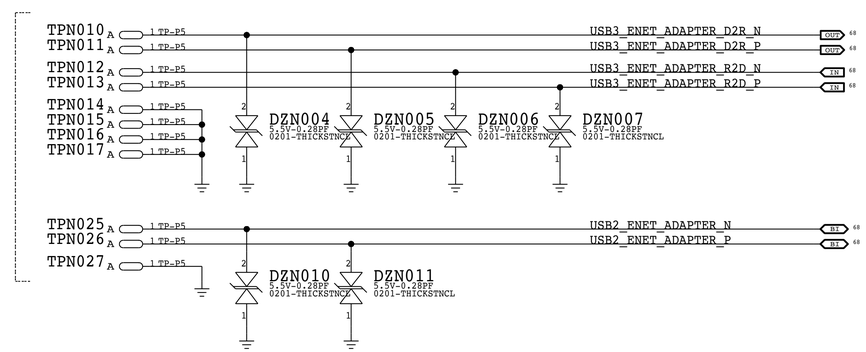
PLACE IN ACCESSIBLE BOARD AREA

NON-CUSTOMER-FACING USB PORTS



ENET ADAPTER

PLACE IN ACCESSIBLE BOARD AREA



BOM_COST_GROUP=PCB

SYNC_MASTER=ANDRES SYNC_DATE=02/13/2017

PAGE TITLE
DFU TEST POINTS

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SVT TEST POINTS <RDAR://30758642>

ITP-XDP

73 13	BI	XDP_CPU_PREQ_L	FUNC_TEST=TRUE
73 13	BI	XDP_CPU_PRDY_L	FUNC_TEST=TRUE
73 66 13	BI	XDP_CPU_TCK	FUNC_TEST=TRUE
73 13	BI	XDP_CPU_TDI	FUNC_TEST=TRUE
73 13	BI	XDP_CPU_TDO	FUNC_TEST=TRUE
73 13	BI	XDP_CPU_TMS	FUNC_TEST=TRUE
73 66	BI	PCH_ITP_PMODE	FUNC_TEST=TRUE
74 73 70 66 45 122	BI	PP1V0_PCH_CORE_S5	FUNC_TEST=TRUE
73 13	BI	XDP_CPU_TRST_L	FUNC_TEST=TRUE
79 73 67 53 43	BI	PM_RSMRST_PCH_L	FUNC_TEST=TRUE
76 73 67	BI	PM_PWRBTN_L	FUNC_TEST=TRUE
73 67 63	BI	SPI_IO<2>	FUNC_TEST=TRUE
73 67 43	BI	PM_PCH_SYS_PWROK	FUNC_TEST=TRUE
73 72 13	BI	XDP_CPU_PWR_DEBUG_L	FUNC_TEST=TRUE
73 67 43	BI	PM_SYSRST_L	FUNC_TEST=TRUE
13	BI	CPU_DEBUG_EN_L	FUNC_TEST=TRUE

BSCAN

73 66	BI	XDP_PCH_TMS	FUNC_TEST=TRUE
73 66	BI	XDP_PCH_TDI	FUNC_TEST=TRUE
73 66	BI	XDP_PCH_TDO	FUNC_TEST=TRUE
73	BI	XDP_JTAG_CPU_ISOL_L	FUNC_TEST=TRUE
72 30 24	BI	JTAG_TBT_TDI	FUNC_TEST=TRUE
72 30 24	BI	JTAG_TBT_TDO	FUNC_TEST=TRUE
72 30 24	BI	JTAG_TBT_TCK	FUNC_TEST=TRUE
72 24	BI	JTAG_TBT_T_TMS	FUNC_TEST=TRUE
72 30	BI	JTAG_TBT_X_TMS	FUNC_TEST=TRUE
121 36	BI	JTAG_SOC_TDO	FUNC_TEST=TRUE
121 36	BI	JTAG_SOC_TDI	FUNC_TEST=TRUE
36	BI	TP_JTAG_SOC_TRST_L	FUNC_TEST=TRUE
94	BI	GPU_JTAG_TCK	FUNC_TEST=TRUE
94	BI	GPU_JTAG_TDI	FUNC_TEST=TRUE
94	BI	GPU_JTAG_TDO	FUNC_TEST=TRUE
94	BI	GPU_JTAG_TMS	FUNC_TEST=TRUE
94	BI	GPU_JTAG_TRST_L	FUNC_TEST=TRUE
161 56 54	BI	ENET_JTAG_TCK	FUNC_TEST=TRUE
161 56 54	BI	ENET_JTAG_TDI	FUNC_TEST=TRUE
161 56 54	BI	ENET_JTAG_TDO	FUNC_TEST=TRUE
161 56 54	BI	ENET_JTAG_TMS	FUNC_TEST=TRUE
161 56 54	BI	ENET_JTAG_TRST_L	FUNC_TEST=TRUE
137 134 36	BI	SWD_WLAN_SWDIO	FUNC_TEST=TRUE
137 134 36	BI	SWD_WLAN_SWCLK	FUNC_TEST=TRUE
137 134 37	BI	WLAN_THROTTLE	FUNC_TEST=TRUE
137 134	BI	WLAN_JTAG_TDO	FUNC_TEST=TRUE
137 134	BI	WLAN_JTAG_TRST_L	FUNC_TEST=TRUE

BSCAN COMPLIANCE

67	BI	PM_SLP_SUS_L	FUNC_TEST=TRUE
76 72 36	BI	PM_SLP_S0_L	FUNC_TEST=TRUE
155 67 65 30 24	BI	PM_SLP_S3_L	FUNC_TEST=TRUE
155 67	BI	PM_SLP_S4_L	FUNC_TEST=TRUE
155 67	BI	PM_SLP_S5_L	FUNC_TEST=TRUE
72 67	BI	PCH_PM_SLP_S0_L	FUNC_TEST=TRUE
156 67 45	BI	PM_THRMTRIP_L	FUNC_TEST=TRUE
155 145 137 67 45	BI	PLT_RESET_L	FUNC_TEST=TRUE
43 36	BI	SMC_PCH_SYS_PWROK	FUNC_TEST=TRUE
43 36	BI	SMC_PCH_PWROK	FUNC_TEST=TRUE
43 36	BI	SMC_SYSRST_L	FUNC_TEST=TRUE
72 67 13	BI	PCH_PM_DOWN	FUNC_TEST=TRUE
67	BI	PCH_SRTCRST_PCH_L	FUNC_TEST=TRUE
67	BI	PCH_PROCPWRGD	FUNC_TEST=TRUE
17 12	BI	VDDQ_AB_PWRGD_BUFFER	FUNC_TEST=TRUE
17 12	BI	VDDQ_CD_PWRGD_BUFFER	FUNC_TEST=TRUE
17	BI	PGOOD_VDDQ_01_R_INV	FUNC_TEST=TRUE
17	BI	PGOOD_VDDQ_23_R_INV	FUNC_TEST=TRUE
67 13	BI	CPU_PWRGD	FUNC_TEST=TRUE
121 76 44 36	BI	PMU_COLD_RESET_L	FUNC_TEST=TRUE
36	BI	SOC_JTAG_SEL	FUNC_TEST=TRUE
121 35	BI	SOC_TESTMODE	FUNC_TEST=TRUE
94	BI	GPU_JTAG_TESTEN	FUNC_TEST=TRUE
137 134	BI	WLAN_JTAG_SEL	FUNC_TEST=TRUE
24	BI	TBT_T_TEST_EN	FUNC_TEST=TRUE
30	BI	TBT_X_TEST_EN	FUNC_TEST=TRUE

VOLTAGE MONITORING

88 76 73	BI	PVCCIO_PGOOD	FUNC_TEST=TRUE
168 89 34	BI	PPVCCSA_S0	FUNC_TEST=TRUE
107 103 76 74 66 65 49 47 46 44	BI	PP1V8_S0	FUNC_TEST=TRUE
168 92 90 22 19 18 17 14	BI	PPVDDQ01_S3	FUNC_TEST=TRUE
168 93 91 67 22 21 20 17 14	BI	PPVDDQ23_S3	FUNC_TEST=TRUE
119 112 99 98 94 45	BI	PP1V8_S0_GPU	FUNC_TEST=TRUE
78 65 57 56 55 54	BI	PP3V3_G3H_ENET_FET	FUNC_TEST=TRUE
168 155 88 73 43 17 14 13 12 11	BI	PPVCCIO_S0	FUNC_TEST=TRUE
137 134 131 129 128 127 78 60 59 51 48 128	BI	PP1V8_G3S	FUNC_TEST=TRUE

BOM_COST_GROUP=PCB

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

SVT TEST PROPERTIES

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FCT TEST POINTS <RDAR://30758642>

VOLTAGE MONITORING

59 58	BI	PP3V3_S0SW_SD	FUNC_TEST=TRUE
58	BI	PP1V2_SD	FUNC_TEST=TRUE
78 69 32 24	BI	PP3V3_S0_TBT	FUNC_TEST=TRUE
113 112 109 105 78 73 118 117 106 115 114	BI	PP5V_S0	FUNC_TEST=TRUE
59	BI	PP5V_G3S_USBC_REG	FUNC_TEST=TRUE
80 55	BI	PP1V2_ENET	FUNC_TEST=TRUE
80 55	BI	PP2V1_ENET	FUNC_TEST=TRUE
81 55	BI	PP0V85_ENET	FUNC_TEST=TRUE
92 91 90 82 81 78 51 54	BI	PP5V_G3S	FUNC_TEST=TRUE
89 88 87 86 84	BI	PPDRV_CPUVR	FUNC_TEST=TRUE
171 90 22 19 18	BI	PPDDRVTT01_S0	FUNC_TEST=TRUE
171 91 22 21 20	BI	PPDDRVTT23_S0	FUNC_TEST=TRUE
168 90 19 18 17 12	BI	PPVPP01_S3	FUNC_TEST=TRUE
168 91 21 20 17	BI	PPVPP23_S3	FUNC_TEST=TRUE
108	BI	PP12V_LCD_FET	FUNC_TEST=TRUE
171 110 109	BI	PPBKLT_BOOST	FUNC_TEST=TRUE
170 116 99	BI	PPMVDD_S0_GPU	FUNC_TEST=TRUE
149 140 139 88 85 49 157	BI	PP12V_MAIN	FUNC_TEST=TRUE
139 109 108	BI	PP12V_MAIN_BLC_LCD	FUNC_TEST=TRUE
25	BI	PP0V9_TBT_T_SVR	FUNC_TEST=TRUE
26 25	BI	PP3V3_TBT_T_S0	FUNC_TEST=TRUE
25	BI	PP3V3_TBT_T_F	FUNC_TEST=TRUE
28 27 26 25 24	BI	PP3V3_TBT_T_SX	FUNC_TEST=TRUE
31	BI	PP0V9_TBT_X_SVR	FUNC_TEST=TRUE
31	BI	PP0V9_TBT_X_LVR	FUNC_TEST=TRUE
32 31	BI	PP3V3_TBT_X_S0	FUNC_TEST=TRUE
34 33 32 31 30	BI	PP3V3_TBT_X_SX	FUNC_TEST=TRUE
32 31	BI	PP3V3_TBT_X_LC	FUNC_TEST=TRUE
75 41 40 35	BI	PP1V1_SLPDDR	FUNC_TEST=TRUE
74 40	BI	PP0V9_SLPDDR	FUNC_TEST=TRUE
74 64 48 44 43 41 38 156 76	BI	PP1V8_AWAKE	FUNC_TEST=TRUE
123 75 74 41 40	BI	PP1V1_SLPS2R	FUNC_TEST=TRUE
75 41	BI	PP3V3_AWAKE	FUNC_TEST=TRUE

MIKEY

130	BI	AUD_CONN_J1_HP_LT	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_HP_RT	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_HP_SNS_LT	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_HP_SNS_RT	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_HP_PORT_US_GND	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_HP_PORT_CH_GND	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_HS_MICP	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_CABLE_DETECT	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_HS_MICN	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_AUD_RING_SENSE	FUNC_TEST=TRUE
130	BI	AUD_CONN_J1_AUD_TIP_SENSE	FUNC_TEST=TRUE

WIFI AND BT

134	BI	VDD1P5	FUNC_TEST=TRUE
134	BI	VIN_RFLDO	FUNC_TEST=TRUE
134	BI	VDD1P2	FUNC_TEST=TRUE

SD

60 59 58	BI	PP1V8_GL_SDCONN	FUNC_TEST=TRUE
59	BI	SDCONN_R_D3	FUNC_TEST=TRUE
59	BI	SDCONN_CMD_R	FUNC_TEST=TRUE
59	BI	SDCONN_R_CLK	FUNC_TEST=TRUE
59	BI	SDCONN_R_D2	FUNC_TEST=TRUE
59	BI	SDCONN_DETECT_R_L	FUNC_TEST=TRUE

POWER ENABLES AND PGOODS

76 58	BI	SD_PWR_EN	FUNC_TEST=TRUE
144 78	BI	PM_EN_FET_P3V3_S0	FUNC_TEST=TRUE
154 78 76	BI	PM_G3S_EN	FUNC_TEST=TRUE
154 78 76	BI	TBT_PWR_EN	FUNC_TEST=TRUE
81 80 78	BI	PM_PGOOD_0V85_1V2_ENET	FUNC_TEST=TRUE
144 78	BI	PM_EN_FET_P5V_S0	FUNC_TEST=TRUE
154 79 76	BI	P3V3G3W_EN	FUNC_TEST=TRUE
79 34 33 28 27	BI	PM_EN_REG_P5V_G3S_USBC	FUNC_TEST=TRUE
80	BI	PM_EN_REG_1V2_ENET_R	FUNC_TEST=TRUE
80	BI	PM_EN_REG_2V1_ENET_R	FUNC_TEST=TRUE
81	BI	PM_EN_REG_0V85_ENET_R	FUNC_TEST=TRUE
82	BI	PM_EN_REG_P3V3_G3H_R	FUNC_TEST=TRUE
82	BI	PM_EN_REG_P5V_G3S_R	FUNC_TEST=TRUE
154 144 108 91 90 84 81 80 77 57	BI	PM_S0_EN	FUNC_TEST=TRUE
85	BI	REG_CPU_VCCIN_EN	FUNC_TEST=TRUE
88	BI	PM_VCCIO_EN_R	FUNC_TEST=TRUE
93	BI	REG_CPU_VDDQ23_EN	FUNC_TEST=TRUE
92	BI	REG_CPU_VDDQ01_EN	FUNC_TEST=TRUE
90	BI	PM_EN_REG_VPP01_R	FUNC_TEST=TRUE
93	BI	PM_EN_REG_VPP23_R	FUNC_TEST=TRUE
111 108 49 44	BI	IOX_LCD_PWR_EN	FUNC_TEST=TRUE
109	BI	BKLT_BL_EN	FUNC_TEST=TRUE
112	BI	VR_GPU_ENABLE	FUNC_TEST=TRUE
143 116	BI	PM_EN_REG_GPU_MVDD	FUNC_TEST=TRUE
143 117	BI	PM_EN_REG_GPU_VDDCI	FUNC_TEST=TRUE
143 118	BI	PM_EN_REG_GPU_P0V8	FUNC_TEST=TRUE
143 119 106	BI	PM_EN_REG_GPU_P1V8	FUNC_TEST=TRUE
143 120	BI	PM_EN_REG_GPU_MVPP	FUNC_TEST=TRUE
156 144 143 78 47	BI	PM_PGOOD_FET_P3V3_S0	FUNC_TEST=TRUE
78 77	BI	PM_PGOOD_FET_P3V3G3S	FUNC_TEST=TRUE
144 143 78	BI	PM_PGOOD_FET_P5V_S0	FUNC_TEST=TRUE
79 76	BI	P3V3G3W_PGOOD	FUNC_TEST=TRUE
79	BI	REG_P5VG3S_USBC_PGOOD	FUNC_TEST=TRUE
81 80	BI	PM_PGOOD_REG_1V2_ENET	FUNC_TEST=TRUE
80 54	BI	PM_PGOOD_REG_2V1_ENET	FUNC_TEST=TRUE
81	BI	PM_PGOOD_REG_0V85_ENET	FUNC_TEST=TRUE
82 76	BI	P3V3G3H_PGOOD	FUNC_TEST=TRUE
82 76	BI	P5VG3S_PGOOD	FUNC_TEST=TRUE
144 84	BI	PM_DRVCPU_PGOOD	FUNC_TEST=TRUE
85 76	BI	CPU_VR_READY	FUNC_TEST=TRUE
85	BI	TP_PM_PGOOD_REG_CPU_VCCSA	FUNC_TEST=TRUE
144 90	BI	PM_PGOOD_VTT01_S0	FUNC_TEST=TRUE
144 93	BI	PM_PGOOD_VTT23_S0	FUNC_TEST=TRUE
92 90	BI	PM_PGOOD_REG_VPP01	FUNC_TEST=TRUE
93 93	BI	PM_PGOOD_REG_VPP23	FUNC_TEST=TRUE
143 112	BI	PM_PGOOD_REG_GPUVCORE	FUNC_TEST=TRUE
143 116 106	BI	PM_PGOOD_REG_GPU_MVDD	FUNC_TEST=TRUE
143 117	BI	PM_PGOOD_REG_GPU_VDDCI	FUNC_TEST=TRUE
143 118	BI	PM_PGOOD_REG_GPU_P0V8	FUNC_TEST=TRUE
143 119	BI	PM_PGOOD_REG_GPU_P1V8	FUNC_TEST=TRUE
143 120	BI	PM_PGOOD_REG_GPU_MVPP	FUNC_TEST=TRUE
140 53 52 36	BI	PSU12VPGOOD	FUNC_TEST=TRUE
141	BI	PSU_P12V_EN_L	FUNC_TEST=TRUE

FAN

69	BI	FAN_1_PWM_FILT	FUNC_TEST=TRUE
69	BI	FAN_1_TACH_FILT	FUNC_TEST=TRUE
159 69	BI	PP12V_S0_FAN_1_FILT	FUNC_TEST=TRUE
68	BI	FAN_0_PWM_FILT	FUNC_TEST=TRUE
167 68	BI	FAN_0_TACH_FILT	FUNC_TEST=TRUE
159 68	BI	PP12V_S0_FAN_0_FILT	FUNC_TEST=TRUE

USB-A

52	BI	PP5V_S4_EXTA_F	FUNC_TEST=TRUE
52	BI	PP5V_S4_EXTB_F	FUNC_TEST=TRUE
53	BI	PP5V_S4_EXTC_F	FUNC_TEST=TRUE
53	BI	PP5V_S4_EXTD_F	FUNC_TEST=TRUE

SENSE RESISTOR MEASUREMENTS

51	BI	GND_AUDIO_DMIC_1	FUNC_TEST=TRUE
51	BI	PDM_DMIC_DATA0_CONN	FUNC_TEST=TRUE
51	BI	PDM_DMIC_CLK0_CONN	FUNC_TEST=TRUE
128	BI	AUD_SPKR_LWFR_OUT_N	FUNC_TEST=TRUE
128	BI	AUD_SPKR_LWFR_OUT_P	FUNC_TEST=TRUE
128 37	BI	SPKR_ID0	FUNC_TEST=TRUE
128	BI	AUD_SPKR_LTWT_OUT_N	FUNC_TEST=TRUE
128	BI	AUD_SPKR_LTWT_OUT_P	FUNC_TEST=TRUE
129	BI	AUD_SPKR_RWFR_OUT_N	FUNC_TEST=TRUE
129	BI	AUD_SPKR_RWFR_OUT_P	FUNC_TEST=TRUE
129 37	BI	SPKR_ID1	FUNC_TEST=TRUE
129	BI	AUD_SPKR_RTWT_OUT_N	FUNC_TEST=TRUE
129	BI	AUD_SPKR_RTWT_OUT_P	FUNC_TEST=TRUE

USB-C

27 26 29	BI	PPVBUS_USBC_TA	FUNC_TEST=TRUE
28 26 29	BI	PPVBUS_USBC_TB	FUNC_TEST=TRUE
159 33 32 29	BI	PPVBUS_USBC_XA	FUNC_TEST=TRUE
159 33 29	BI	USBC_XA_SBU1	FUNC_TEST=TRUE
159 33 29	BI	USBC_XA_CC1	FUNC_TEST=TRUE
159 33 29	BI	USBC_XA_CC2	FUNC_TEST=TRUE
159 33 29	BI	USBC_XA_SBU2	FUNC_TEST=TRUE
32 29	BI	USBC_XA_USB_DBG_BOT_P	FUNC_TEST=TRUE
32 29	BI	USBC_XA_USB_DBG_BOT_N	FUNC_TEST=TRUE
32 29	BI	USBC_XA_USB_DBG_TOP_P	FUNC_TEST=TRUE
32 29	BI	USBC_XA_USB_DBG_TOP_N	FUNC_TEST=TRUE
34 29	BI	USBC_XB_USB_BOT_P	FUNC_TEST=TRUE
34 29	BI	USBC_XB_USB_BOT_N	FUNC_TEST=TRUE
34 29	BI	USBC_XB_USB_TOP_P	FUNC_TEST=TRUE
34 29	BI	USBC_XB_USB_TOP_N	FUNC_TEST=TRUE
34 32 29	BI	PPVBUS_USBC_XB	FUNC_TEST=TRUE

MAC-1 DISPLAY

161 109 108 96	BI	DP_INTPNL_ML_HPD	FUNC_TEST=TRUE
161 108 96	BI	DP_INTPNL_SL_HPD	FUNC_TEST=TRUE

ADCS

149 36	BI	SMC_P12V_MAIN_ISENSE	FUNC_TEST=TRUE
149 36	BI	SMC_P12V_GPU_ISENSE	FUNC_TEST=TRUE
152 85	BI	REG_CPU_VCCIN_IMON	FUNC_TEST=TRUE
152 112 105	BI	VR_GPU_CORE_IMON	FUNC_TEST=TRUE
151	BI	HS_MVDD_ISENSE_OUT	FUNC_TEST=TRUE
149	BI	HS_P12V_GPU_ISENSE_OUT	FUNC_TEST=TRUE
149	BI	HS_P12V_AUX_GPU_IOUT	FUNC_TEST=TRUE
151	BI	LS_VDDQ01_S3_CPU_OUT	FUNC_TEST=TRUE
168 159 151 87 86 15	BI	PPVCCIN_S0	FUNC_TEST=TRUE
151	BI	LS_VPP01_S3_CPU_OUT	FUNC_TEST=TRUE
151	BI	LS_VPP23_S3_CPU_OUT	FUNC_TEST=TRUE
151 76	BI	PMU_GPU_MVDD_S0_ISENSE	FUNC_TEST=TRUE

DISPLAY

108 44	BI	I2C_DP_TCON_SLA_3V3_SDA	FUNC_TEST=TRUE
108 44	BI	I2C_DP_TCON_SLA_3V3_SCL	FUNC_TEST=TRUE
161 109 108 96	BI	DP_INTPNL_ML_HPD	FUNC_TEST=TRUE
161 108 96	BI	DP_INTPNL_SL_HPD	FUNC_TEST=TRUE
108	BI	DP_INT_PIN_54	FUNC_TEST=TRUE
109 108	BI	BLC_VSYNC	FUNC_TEST=TRUE
161 109 108	BI	BLC_LSYNC	FUNC_TEST=TRUE
108	BI	BLC_EN	FUNC_TEST=TRUE

BACKLIGHT TEST

110	BI	LED_RETURN_9	FUNC_TEST=TRUE
110	BI	LED_RETURN_7	FUNC_TEST=TRUE
110	BI	LED_RETURN_5	FUNC_TEST=TRUE
110	BI	LED_RETURN_3	FUNC_TEST=TRUE
110	BI	LED_RETURN_1	FUNC_TEST=TRUE
110	BI	LED_RETURN_2	FUNC_TEST=TRUE
110	BI	LED_RETURN_4	FUNC_TEST=TRUE
110	BI	LED_RETURN_6	FUNC_TEST=TRUE
110	BI	LED_RETURN_8	FUNC_TEST=TRUE
161 109 108	BI	BLC_LSYNC	FUNC_TEST=TRUE
109	BI	PP12V_BKLT_FUSED	FUNC_TEST=TRUE
109	BI	PP12V_BKLT_SNS	FUNC_TEST=TRUE

CAMERA

51	BI	I2C_FTCAM_SCL_CONN	FUNC_TEST=TRUE
51	BI	I2C_FTCAM_SDA_CONN	FUNC_TEST=TRUE
51	BI	PP1V8_G3S_DMIC_F	FUNC_TEST=TRUE

ALS

51	BI	I2C_ALS_SDA_CONN	FUNC_TEST=TRUE
51	BI	I2C_ALS_SCL_CONN	FUNC_TEST=TRUE

ETHERNET

160 56 54	BI	ENET_JTAG_TRST_L	FUNC_TEST=TRUE
160 56 54	BI	ENET_JTAG_TDI	FUNC_TEST=TRUE
160 56 54	BI	ENET_JTAG_TCK	FUNC_TEST=TRUE
160 56 54	BI	ENET_JTAG_TMS	FUNC_TEST=TRUE
160 56 54	BI	ENET_JTAG_TDO	FUNC_TEST=TRUE

BOM_COST_GROUP=PCB

SYNC_MASTER=DEV_MLB SYNC_DATE=11/06/2016

PAGE TITLE

FCT TEST PROPERTIES

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REVISION 6.21.0

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ICT NO TEST <RDAR://30758642>

MEMORY

18 7	BI	MEM_0_DQ<63..0>	NO_TEST=1
18 7	BI	MEM_0_CS_L<3..0>	NO_TEST=1
18 7	BI	MEM_0_CLK_P<1..0>	NO_TEST=1
18	BI	MEM_0_CLK_N<1..0>	NO_TEST=1
18	BI	MEM_0_DQS_P<17..0>	NO_TEST=1
18	BI	MEM_0_DQS_N<17..0>	NO_TEST=1
18 7	BI	MEM_0_MA<17..0>	NO_TEST=1
18 7	BI	MEM_0_ECC<7..0>	NO_TEST=1
18 7	BI	MEM_0_CKE<1..0>	NO_TEST=1
18 7	BI	MEM_0_BA<1..0>	NO_TEST=1
18 7	BI	MEM_0_BG<1..0>	NO_TEST=1
18 7	BI	MEM_0_ODT<1..0>	NO_TEST=1
18 7	BI	MEM_0_PARITY	NO_TEST=1
18 7	BI	MEM_0_ACT_L	NO_TEST=1
18 7	BI	MEM_0_ALERT_L	NO_TEST=1
19 8	BI	MEM_1_DQ<63..0>	NO_TEST=1
19 8	BI	MEM_1_CS_L<3..0>	NO_TEST=1
19 9	BI	MEM_1_CLK_P<1..0>	NO_TEST=1
19 9	BI	MEM_1_CLK_N<1..0>	NO_TEST=1
19	BI	MEM_1_DQS_P<17..0>	NO_TEST=1
19 9	BI	MEM_1_DQS_N<17..0>	NO_TEST=1
19 8	BI	MEM_1_MA<17..0>	NO_TEST=1
19 8	BI	MEM_1_ECC<7..0>	NO_TEST=1
19 8	BI	MEM_1_CKE<1..0>	NO_TEST=1
19 8	BI	MEM_1_BA<1..0>	NO_TEST=1
19 8	BI	MEM_1_BG<1..0>	NO_TEST=1
19 8	BI	MEM_1_ODT<1..0>	NO_TEST=1
19 8	BI	MEM_1_PARITY	NO_TEST=1
19 8	BI	MEM_1_ACT_L	NO_TEST=1
19 8	BI	MEM_1_ALERT_L	NO_TEST=1
20 9	BI	MEM_2_DQ<63..0>	NO_TEST=1
20 9	BI	MEM_2_CS_L<3..0>	NO_TEST=1
20 9	BI	MEM_2_CLK_P<1..0>	NO_TEST=1
20 9	BI	MEM_2_CLK_N<1..0>	NO_TEST=1
20	BI	MEM_2_DQS_P<17..0>	NO_TEST=1
20 9	BI	MEM_2_DQS_N<17..0>	NO_TEST=1
20 9	BI	MEM_2_MA<17..0>	NO_TEST=1
20 9	BI	MEM_2_ECC<7..0>	NO_TEST=1
20 9	BI	MEM_2_CKE<1..0>	NO_TEST=1
20 9	BI	MEM_2_BA<1..0>	NO_TEST=1
20 9	BI	MEM_2_BG<1..0>	NO_TEST=1
20 9	BI	MEM_2_ODT<1..0>	NO_TEST=1
20 9	BI	MEM_2_PARITY	NO_TEST=1
20 9	BI	MEM_2_ACT_L	NO_TEST=1
20 9	BI	MEM_2_ALERT_L	NO_TEST=1
21 10	BI	MEM_3_DQ<63..0>	NO_TEST=1
21 10	BI	MEM_3_CS_L<3..0>	NO_TEST=1
21 10	BI	MEM_3_CLK_P<1..0>	NO_TEST=1
21 10	BI	MEM_3_CLK_N<1..0>	NO_TEST=1
21 10	BI	MEM_3_DQS_P<17..0>	NO_TEST=1
21 10	BI	MEM_3_DQS_N<17..0>	NO_TEST=1
21 10	BI	MEM_3_MA<17..0>	NO_TEST=1
21 10	BI	MEM_3_ECC<7..0>	NO_TEST=1
21 10	BI	MEM_3_CKE<1..0>	NO_TEST=1
21 10	BI	MEM_3_BA<1..0>	NO_TEST=1
21 10	BI	MEM_3_BG<1..0>	NO_TEST=1
21 10	BI	MEM_3_ODT<1..0>	NO_TEST=1
21 10	BI	MEM_3_PARITY	NO_TEST=1
21 10	BI	MEM_3_ACT_L	NO_TEST=1
21 10	BI	MEM_3_ALERT_L	NO_TEST=1

PCIE

56 11	BI	PCIE_ENET_D2R_P<3..0>	NO_TEST=1
56 11	BI	PCIE_ENET_D2R_N<3..0>	NO_TEST=1
56 54	BI	PCIE_ENET_R2D_P<3..0>	NO_TEST=1
56 54	BI	PCIE_ENET_R2D_N<3..0>	NO_TEST=1
56 54	BI	PCIE_ENET_D2R_C_P<3..0>	NO_TEST=1
56 54	BI	PCIE_ENET_D2R_C_N<3..0>	NO_TEST=1
56 11	BI	PCIE_ENET_R2D_C_P<3..0>	NO_TEST=1
56 11	BI	PCIE_ENET_R2D_C_N<3..0>	NO_TEST=1
26 11	BI	PCIE_TBT_T_D2R_P<3..0>	NO_TEST=1
26 11	BI	PCIE_TBT_T_D2R_N<3..0>	NO_TEST=1
26 24	BI	PCIE_TBT_T_R2D_P<3..0>	NO_TEST=1
26 24	BI	PCIE_TBT_T_R2D_N<3..0>	NO_TEST=1
26 24	BI	PCIE_TBT_T_D2R_C_P<3..0>	NO_TEST=1
26 24	BI	PCIE_TBT_T_D2R_C_N<3..0>	NO_TEST=1
26 11	BI	PCIE_TBT_T_R2D_C_P<3..0>	NO_TEST=1
26 11	BI	PCIE_TBT_T_R2D_C_N<3..0>	NO_TEST=1
32 11	BI	PCIE_TBT_X_D2R_P<3..0>	NO_TEST=1
32 11	BI	PCIE_TBT_X_D2R_N<3..0>	NO_TEST=1
32 30	BI	PCIE_TBT_X_R2D_P<3..0>	NO_TEST=1
32 30	BI	PCIE_TBT_X_R2D_N<3..0>	NO_TEST=1
32 30	BI	PCIE_TBT_X_D2R_C_P<3..0>	NO_TEST=1
32 30	BI	PCIE_TBT_X_D2R_C_N<3..0>	NO_TEST=1
32 11	BI	PCIE_TBT_X_R2D_C_P<3..0>	NO_TEST=1
32 11	BI	PCIE_TBT_X_R2D_C_N<3..0>	NO_TEST=1
95 94	BI	PE_GFX_TO_CPU_P<15..0>	NO_TEST=1
95 94	BI	PE_GFX_TO_CPU_N<15..0>	NO_TEST=1
95 11	BI	PE_CPU_TO_GFX_P<15..0>	NO_TEST=1
95 11	BI	PE_CPU_TO_GFX_N<15..0>	NO_TEST=1
95 11	BI	PE_GFX_TO_CPU_C_P<15..0>	NO_TEST=1
95 11	BI	PE_GFX_TO_CPU_C_N<15..0>	NO_TEST=1
95 94	BI	PE_CPU_TO_GFX_C_P<15..0>	NO_TEST=1
95 94	BI	PE_CPU_TO_GFX_C_N<15..0>	NO_TEST=1
67 12	BI	DMI_SB_TO_CPU_P<3..0>	NO_TEST=1
67 12	BI	DMI_SB_TO_CPU_N<3..0>	NO_TEST=1
67 12	BI	DMI_CPU_TO_SB_P<3..0>	NO_TEST=1
67 12	BI	DMI_CPU_TO_SB_N<3..0>	NO_TEST=1
12	BI	DMI_SB_TO_CPU_C_P<3..0>	NO_TEST=1
12	BI	DMI_SB_TO_CPU_C_N<3..0>	NO_TEST=1
12	BI	DMI_CPU_TO_SB_C_P<3..0>	NO_TEST=1
12	BI	DMI_CPU_TO_SB_C_N<3..0>	NO_TEST=1
167 44 38	BI	PCIE_SOC_R2D_P<3..0>	NO_TEST=1
167 44 38	BI	PCIE_SOC_R2D_N<3..0>	NO_TEST=1
38	BI	PCIE_SOC_D2R_C_P<3..0>	NO_TEST=1
38	BI	PCIE_SOC_D2R_C_N<3..0>	NO_TEST=1
66 38	BI	PCIE_CLK100M_SOC_P	NO_TEST=1
66 38	BI	PCIE_CLK100M_SOC_N	NO_TEST=1
61	BI	PCIE_SSD0_R2D_P<0>	NO_TEST=1
61	BI	PCIE_SSD0_R2D_N<0>	NO_TEST=1
61 38	BI	PCIE_SSD0_R2D_C_P<0>	NO_TEST=1
61 38	BI	PCIE_SSD0_R2D_C_N<0>	NO_TEST=1
61 38	BI	PCIE_SSD0_D2R_P<0>	NO_TEST=1
61 38	BI	PCIE_SSD0_D2R_N<0>	NO_TEST=1
61 38	BI	PCIE_CLK100M_SSD0_01_P	NO_TEST=1
61 38	BI	PCIE_CLK100M_SSD0_01_N	NO_TEST=1
61 38	BI	PCIE_CLK100M_SSD0_23_P	NO_TEST=1
61 38	BI	PCIE_CLK100M_SSD0_23_N	NO_TEST=1
62	BI	PCIE_SSD1_R2D_P<0>	NO_TEST=1
62	BI	PCIE_SSD1_R2D_N<0>	NO_TEST=1
62 38	BI	PCIE_SSD1_R2D_C_P<0>	NO_TEST=1
62 38	BI	PCIE_SSD1_R2D_C_N<0>	NO_TEST=1
62 38	BI	PCIE_SSD1_D2R_P<0>	NO_TEST=1
62 38	BI	PCIE_SSD1_D2R_N<0>	NO_TEST=1
62 38	BI	PCIE_CLK100M_SSD1_01_P	NO_TEST=1
62 38	BI	PCIE_CLK100M_SSD1_01_N	NO_TEST=1
62 38	BI	PCIE_CLK100M_SSD1_23_P	NO_TEST=1
62 38	BI	PCIE_CLK100M_SSD1_23_N	NO_TEST=1

DISPLAY PORT

96 30	BI	DP_X_SNK0_ML_C_P<3..0>	NO_TEST=1
96 30	BI	DP_X_SNK0_ML_C_N<3..0>	NO_TEST=1
96 30	BI	DP_X_SNK0_AUXCH_C_P	NO_TEST=1
96 30	BI	DP_X_SNK0_AUXCH_C_N	NO_TEST=1
30	BI	DP_X_SNK0_ML_P<3..0>	NO_TEST=1
30	BI	DP_X_SNK0_ML_N<3..0>	NO_TEST=1
30	BI	DP_X_SNK0_AUXCH_P	NO_TEST=1
30	BI	DP_X_SNK0_AUXCH_N	NO_TEST=1
96 30	BI	DP_X_SNK1_ML_C_P<3..0>	NO_TEST=1
96 30	BI	DP_X_SNK1_ML_C_N<3..0>	NO_TEST=1
96 30	BI	DP_X_SNK1_AUXCH_C_P	NO_TEST=1
96 30	BI	DP_X_SNK1_AUXCH_C_N	NO_TEST=1
30	BI	DP_X_SNK1_ML_P<3..0>	NO_TEST=1
30	BI	DP_X_SNK1_ML_N<3..0>	NO_TEST=1
30	BI	DP_X_SNK1_AUXCH_P	NO_TEST=1
30	BI	DP_X_SNK1_AUXCH_N	NO_TEST=1
96 24	BI	DP_T_SNK0_ML_C_P<3..0>	NO_TEST=1
96 24	BI	DP_T_SNK0_ML_C_N<3..0>	NO_TEST=1
96 24	BI	DP_T_SNK0_AUXCH_C_P	NO_TEST=1
96 24	BI	DP_T_SNK0_AUXCH_C_N	NO_TEST=1
24	BI	DP_T_SNK0_ML_P<3..0>	NO_TEST=1
24	BI	DP_T_SNK0_ML_N<3..0>	NO_TEST=1
24	BI	DP_T_SNK0_AUXCH_P	NO_TEST=1
24	BI	DP_T_SNK0_AUXCH_N	NO_TEST=1
96 24	BI	DP_T_SNK1_ML_C_P<3..0>	NO_TEST=1
96 24	BI	DP_T_SNK1_ML_C_N<3..0>	NO_TEST=1
96 24	BI	DP_T_SNK1_AUXCH_C_P	NO_TEST=1
96 24	BI	DP_T_SNK1_AUXCH_C_N	NO_TEST=1
24	BI	DP_T_SNK1_ML_P<3..0>	NO_TEST=1
24	BI	DP_T_SNK1_ML_N<3..0>	NO_TEST=1
24	BI	DP_T_SNK1_AUXCH_P	NO_TEST=1
24	BI	DP_T_SNK1_AUXCH_N	NO_TEST=1
108 96	BI	DP_INTPNL_ML_C_P<3..0>	NO_TEST=1
108 96	BI	DP_INTPNL_ML_C_N<3..0>	NO_TEST=1
108 96	BI	DP_INTPNL_ML_AUX_C_P	NO_TEST=1
108 96	BI	DP_INTPNL_ML_AUX_C_N	NO_TEST=1
108	BI	DP_INTPNL_ML_P<3..0>	NO_TEST=1
108	BI	DP_INTPNL_ML_N<3..0>	NO_TEST=1
108	BI	DP_INTPNL_ML_AUX_P	NO_TEST=1
108	BI	DP_INTPNL_ML_AUX_N	NO_TEST=1
108 96	BI	DP_INTPNL_SL_C_P<3..0>	NO_TEST=1
108 96	BI	DP_INTPNL_SL_C_N<3..0>	NO_TEST=1
108 96	BI	DP_INTPNL_SL_AUX_C_P	NO_TEST=1
108 96	BI	DP_INTPNL_SL_AUX_C_N	NO_TEST=1
108	BI	DP_INTPNL_SL_P<3..0>	NO_TEST=1
108	BI	DP_INTPNL_SL_N<3..0>	NO_TEST=1
108	BI	DP_INTPNL_SL_AUX_P	NO_TEST=1
108	BI	DP_INTPNL_SL_AUX_N	NO_TEST=1

ETHERNET

57	BI	ENET_CONN_A_P	NO_TEST=1
57	BI	ENET_CONN_A_N	NO_TEST=1
57	BI	ENET_CONN_B_P	NO_TEST=1
57	BI	ENET_CONN_B_N	NO_TEST=1
57	BI	ENET_CONN_C_P	NO_TEST=1
57	BI	ENET_CONN_C_N	NO_TEST=1
57	BI	ENET_CONN_D_P	NO_TEST=1
57	BI	ENET_CONN_D_N	NO_TEST=1
57 54	BI	ENET_A_P	NO_TEST=1
57 54	BI	ENET_A_N	NO_TEST=1
57 54	BI	ENET_B_P	NO_TEST=1
57 54	BI	ENET_B_N	NO_TEST=1
57 54	BI	ENET_C_P	NO_TEST=1
57 54	BI	ENET_C_N	NO_TEST=1
57 54	BI	ENET_D_P	NO_TEST=1
57 54	BI	ENET_D_N	NO_TEST=1

MIPI

37	BI	NC_MIPI_PLCAM_DATA_P<0>	NO_TEST=1
37	BI	NC_MIPI_PLCAM_DATA_N<0>	NO_TEST=1
37	BI	NC_MIPI_PLCAM_DATA_P<1>	NO_TEST=1
37	BI	NC_MIPI_PLCAM_DATA_N<1>	NO_TEST=1
37	BI	NC_MIPI_PLCAM_CLK_P	NO_TEST=1
37	BI	NC_MIPI_PLCAM_CLK_N	NO_TEST=1
37	BI	NC_MIPI_DFR_DATA_P	NO_TEST=1
37	BI	NC_MIPI_DFR_DATA_N	NO_TEST=1
37	BI	NC_MIPI_DFR_CLK_P	NO_TEST=1
37	BI	NC_MIPI_DFR_CLK_N	NO_TEST=1

I2C

47 36	BI	I2C_SNS0_S0_SCL	NO_TEST=1

USB-A 3.0

68 53	BI	USB3_EXTD_RX_F_P	NO_TEST=1
68 53	BI	USB3_EXTD_RX_F_N	NO_TEST=1
53	BI	USB3_EXTD_RX_P	NO_TEST=1
53	BI	USB3_EXTD_RX_N	NO_TEST=1
68 53	BI	USB3_EXTD_TX_P	NO_TEST=1
68 53	BI	USB3_EXTD_TX_N	NO_TEST=1
53	BI	USB3_EXTD_TX_C_P	NO_TEST=1
53	BI	USB3_EXTD_TX_C_N	NO_TEST=1
53	BI	USB3_EXTD_TX_F_P	NO_TEST=1
53	BI	USB3_EXTD_TX_F_N	NO_TEST=1
68 53	BI	USB3_EXTC_RX_F_P	NO_TEST=1
68 53	BI	USB3_EXTC_RX_F_N	NO_TEST=1
53	BI	USB3_EXTC_RX_P	NO_TEST=1
53	BI	USB3_EXTC_RX_N	NO_TEST=1
68 53	BI	USB3_EXTC_TX_P	NO_TEST=1
68 53	BI	USB3_EXTC_TX_N	NO_TEST=1
53	BI	USB3_EXTC_TX_C_P	NO_TEST=1
53	BI	USB3_EXTC_TX_C_N	NO_TEST=1
53	BI	USB3_EXTC_TX_F_P	NO_TEST=1
53	BI	USB3_EXTC_TX_F_N	NO_TEST=1
68 52	BI	USB3_EXTB_RX_F_P	NO_TEST=1
68 52	BI	USB3_EXTB_RX_F_N	NO_TEST=1
52	BI	USB3_EXTB_RX_P	NO_TEST=1
52	BI	USB3_EXTB_RX_N	NO_TEST=1
68 52	BI	USB3_EXTB_TX_P	NO_TEST=1
68 52	BI	USB3_EXTB_TX_N	NO_TEST=1
52	BI	USB3_EXTB_TX_C_P	NO_TEST=1
52	BI	USB3_EXTB_TX_C_N	NO_TEST=1
52	BI	USB3_EXTB_TX_F_P	NO_TEST=1
52	BI	USB3_EXTB_TX_F_N	NO_TEST=1
68 52	BI	USB3_EXTA_RX_F_P	NO_TEST=1
68 52	BI	USB3_EXTA_RX_F_N	NO_TEST=1
52	BI	USB3_EXTA_RX_P	NO_TEST=1
52	BI	USB3_EXTA_RX_N	NO_TEST=1
68 52	BI	USB3_EXTA_TX_P	NO_TEST=1
68 52	BI	USB3_EXTA_TX_N	NO_TEST=1
52	BI	USB3_EXTA_TX_C_P	NO_TEST=1
52	BI	USB3_EXTA_TX_C_N	NO_TEST=1
52	BI	USB3_EXTA_TX_F_P	NO_TEST=1
52	BI	USB3_EXTA_TX_F_N	NO_TEST=1

BOM_COST_GROUP=PCB

PAGE TITLE
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Apple Inc.

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GRAPHICS VOLTAGE REGULATORS

113	113	B1	REG_BOOST_GPUCORE_1	NO_TEST=1
113	113	B1	REG_BOOST_GPUCORE_1_RC	NO_TEST=1
113	113	B1	REG_BOOST_GPUCORE_2	NO_TEST=1
112	112	B1	REG_BOOST_GPUCORE_2_RC	NO_TEST=1
113	113	B1	REG_BOOST_GPUCORE_3	NO_TEST=1
113	113	B1	REG_BOOST_GPUCORE_3_RC	NO_TEST=1
114	114	B1	REG_BOOST_GPUCORE_4	NO_TEST=1
114	114	B1	REG_BOOST_GPUCORE_4_RC	NO_TEST=1
114	114	B1	REG_BOOST_GPUCORE_5	NO_TEST=1
114	114	B1	REG_BOOST_GPUCORE_5_RC	NO_TEST=1
114	114	B1	REG_BOOST_GPUCORE_6	NO_TEST=1
114	114	B1	REG_BOOST_GPUCORE_6_RC	NO_TEST=1
115	115	B1	REG_BOOST_GPUCORE_7	NO_TEST=1
115	115	B1	REG_BOOST_GPUCORE_7_RC	NO_TEST=1
115	115	B1	REG_BOOST_GPUCORE_8	NO_TEST=1
115	115	B1	REG_BOOST_GPUCORE_8_RC	NO_TEST=1
163	113	B1	VR_PHASE_GPUCORE_1	NO_TEST=1
163	113	B1	VR_PHASE_GPUCORE_2	NO_TEST=1
163	112	B1	VR_PHASE_GPUCORE_3	NO_TEST=1
163	114	B1	VR_PHASE_GPUCORE_4	NO_TEST=1
163	114	B1	VR_PHASE_GPUCORE_5	NO_TEST=1
163	115	B1	VR_PHASE_GPUCORE_6	NO_TEST=1
163	115	B1	VR_PHASE_GPUCORE_7	NO_TEST=1
163	115	B1	VR_PHASE_GPUCORE_8	NO_TEST=1
118		B1	REGLGP0V8	NO_TEST=1
163	119	B1	REGSNUBPVDDR	NO_TEST=1
163	120	B1	REGSNUBPVPP	NO_TEST=1
116		B1	REG_BOOT_MVDD	NO_TEST=1
120		B1	REG_BOOT_MVPP	NO_TEST=1
118		B1	REG_BOOT_P0V8	NO_TEST=1
118		B1	REG_BOOT_P0V8_RC	NO_TEST=1
163	126	B1	REG_COMP_MVPP	NO_TEST=1
119		B1	REG_COMP_PVDDR	NO_TEST=1
113	112	B1	REG_GPUCORE_ISNS_1_N	NO_TEST=1
113	112	B1	REG_GPUCORE_ISNS_1_P	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_1_R_N	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_1_R_P	NO_TEST=1
113	112	B1	REG_GPUCORE_ISNS_2_N	NO_TEST=1
113	112	B1	REG_GPUCORE_ISNS_2_P	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_2_R_N	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_2_R_P	NO_TEST=1
113	112	B1	REG_GPUCORE_ISNS_3_N	NO_TEST=1
113	112	B1	REG_GPUCORE_ISNS_3_P	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_3_R_N	NO_TEST=1
165	112	B1	REG_GPUCORE_ISNS_3_R_P	NO_TEST=1
114	112	B1	REG_GPUCORE_ISNS_4_N	NO_TEST=1
114	112	B1	REG_GPUCORE_ISNS_4_P	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_4_R_N	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_4_R_P	NO_TEST=1
114	112	B1	REG_GPUCORE_ISNS_5_N	NO_TEST=1
114	112	B1	REG_GPUCORE_ISNS_5_P	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_5_R_N	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_5_R_P	NO_TEST=1
114	112	B1	REG_GPUCORE_ISNS_6_N	NO_TEST=1
114	112	B1	REG_GPUCORE_ISNS_6_P	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_6_R_N	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_6_R_P	NO_TEST=1
115	112	B1	REG_GPUCORE_ISNS_7_N	NO_TEST=1
115	112	B1	REG_GPUCORE_ISNS_7_P	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_7_R_N	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_7_R_P	NO_TEST=1
115	112	B1	REG_GPUCORE_ISNS_8_N	NO_TEST=1
115	112	B1	REG_GPUCORE_ISNS_8_P	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_8_R_N	NO_TEST=1
112		B1	REG_GPUCORE_ISNS_8_R_P	NO_TEST=1
116		B1	REG_LGATE_MVDD	NO_TEST=1
118		B1	REG_LGATE_P0V8	NO_TEST=1
116		B1	REG_MVDD_FB	NO_TEST=1
116		B1	REG_MVDD_FB_R	NO_TEST=1
116		B1	REG_MVDD_FSEL	NO_TEST=1
116		B1	REG_MVDD_OCSET	NO_TEST=1
116		B1	REG_MVDD_RTN	NO_TEST=1
116		B1	REG_MVDD_RTN_R	NO_TEST=1
116		B1	REG_MVDD_SET0	NO_TEST=1
116		B1	REG_MVDD_SET1	NO_TEST=1
116		B1	REG_MVDD_SET1_R	NO_TEST=1
116		B1	REG_MVDD_SREF	NO_TEST=1

GRAPHICS VOLTAGE REGULATORS

118		B1	REG_P0V8_FB	NO_TEST=1
118		B1	REG_P0V8_FB_R	NO_TEST=1
118		B1	REG_P0V8_FSEL	NO_TEST=1
118		B1	REG_P0V8_OCSET	NO_TEST=1
118		B1	REG_P0V8_RTN	NO_TEST=1
118		B1	REG_P0V8_RTN_R	NO_TEST=1
118		B1	REG_P0V8_SET0	NO_TEST=1
118		B1	REG_P0V8_SET1	NO_TEST=1
118		B1	REG_P0V8_SREF	NO_TEST=1
118		B1	REG_P0V8_VO	NO_TEST=1
116		B1	REG_PHASE_MVDD	NO_TEST=1
120		B1	REG_PHASE_MVPP	NO_TEST=1
118		B1	REG_PHASE_P0V8	NO_TEST=1
118		B1	REG_PHASE_SNS_P0V8	NO_TEST=1
113	112	B1	REG_PWM_GPUCORE_1	NO_TEST=1
113	112	B1	REG_PWM_GPUCORE_2	NO_TEST=1
113	112	B1	REG_PWM_GPUCORE_3	NO_TEST=1
114	112	B1	REG_PWM_GPUCORE_4	NO_TEST=1
114	112	B1	REG_PWM_GPUCORE_5	NO_TEST=1
114	112	B1	REG_PWM_GPUCORE_6	NO_TEST=1
115	112	B1	REG_PWM_GPUCORE_7	NO_TEST=1
115	112	B1	REG_PWM_GPUCORE_8	NO_TEST=1
120		B1	REG_RTCLK_MVPP	NO_TEST=1
113		B1	REG_SNUBBER_GPUCORE_1	NO_TEST=1
113		B1	REG_SNUBBER_GPUCORE_2	NO_TEST=1
113		B1	REG_SNUBBER_GPUCORE_3	NO_TEST=1
114		B1	REG_SNUBBER_GPUCORE_4	NO_TEST=1
114		B1	REG_SNUBBER_GPUCORE_5	NO_TEST=1
114		B1	REG_SNUBBER_GPUCORE_6	NO_TEST=1
115		B1	REG_SNUBBER_GPUCORE_7	NO_TEST=1
115		B1	REG_SNUBBER_GPUCORE_8	NO_TEST=1
116		B1	REG_SNUBBER_MVDD	NO_TEST=1
118		B1	REG_SNUBBER_P0V8	NO_TEST=1
120		B1	REG_SSTR_MVPP	NO_TEST=1
116		B1	REG_UGATE_MVDD	NO_TEST=1
120		B1	REG_VSNSR_MVPP	NO_TEST=1
120		B1	REG_VSNS_MVPP	NO_TEST=1
163	120	B1	REG_COMP_MVPP	NO_TEST=1
120		B1	RGCMVPP	NO_TEST=1
163	113	B1	VR_PHASE_GPUCORE_1	NO_TEST=1
163	113	B1	VR_PHASE_GPUCORE_2	NO_TEST=1
163	113	B1	VR_PHASE_GPUCORE_3	NO_TEST=1
163	114	B1	VR_PHASE_GPUCORE_4	NO_TEST=1
163	114	B1	VR_PHASE_GPUCORE_5	NO_TEST=1
163	114	B1	VR_PHASE_GPUCORE_6	NO_TEST=1
163	115	B1	VR_PHASE_GPUCORE_7	NO_TEST=1
163	115	B1	VR_PHASE_GPUCORE_8	NO_TEST=1
116		B1	VR_PHASE_MVDD	NO_TEST=1

ETHERNET VOLTAGE REGULATORS

78		B1	P3V3ENET_SS	NO_TEST=1
163	81	B1	REG_0V85_ENET_FB	NO_TEST=1
163	81	B1	REG_0V85_ENET_OCSET	NO_TEST=1
163	81	B1	REG_0V85_ENET_RTN	NO_TEST=1
163	81	B1	REG_0V85_ENET_FB	NO_TEST=1
81	55	B1	REG_0V85_ENET_FB_N	NO_TEST=1
81	55	B1	REG_0V85_ENET_FB_P	NO_TEST=1
81		B1	REG_0V85_ENET_FSEL	NO_TEST=1
163	81	B1	REG_0V85_ENET_OCSET	NO_TEST=1
163	81	B1	REG_0V85_ENET_RTN	NO_TEST=1
81		B1	REG_0V85_ENET_SENSE_N	NO_TEST=1
81		B1	REG_0V85_ENET_SENSE_P	NO_TEST=1
81		B1	REG_0V85_ENET_SREF	NO_TEST=1
81		B1	REG_BOOT_0V85_ENET	NO_TEST=1
81		B1	REG_BOOT_0V85_ENET_RC	NO_TEST=1
81		B1	REG_LGATE_0V85_ENET	NO_TEST=1
81		B1	REG_PHASE_0V85_ENET	NO_TEST=1
81		B1	REG_PHASE_0V85_ENET_TGR	NO_TEST=1
81		B1	REG_PVCC_U8500	NO_TEST=1
81		B1	REG_SNUBBER_0V85_ENET	NO_TEST=1
81		B1	REG_UGATE_0V85_ENET	NO_TEST=1
81		B1	REG_UGATE_0V85_ENET_R	NO_TEST=1
81		B1	REG_VCC_U8500	NO_TEST=1
80		B1	REG_FB_1V2_ENET	NO_TEST=1
80		B1	REG_FB_1V2_ENET_R	NO_TEST=1
80		B1	REG_FB_2V1_ENET	NO_TEST=1
80		B1	REG_FB_2V1_ENET_R	NO_TEST=1

CPU VOLTAGE REGULATORS

86		B1	REG_BOOST_CPUCORE_1	NO_TEST=1
86		B1	REG_BOOST_CPUCORE_1_RC	NO_TEST=1
86		B1	REG_BOOST_CPUCORE_2	NO_TEST=1
86		B1	REG_BOOST_CPUCORE_2_RC	NO_TEST=1
86		B1	REG_BOOST_CPUCORE_3	NO_TEST=1
86		B1	REG_BOOST_CPUCORE_3_RC	NO_TEST=1
87		B1	REG_BOOST_CPUCORE_4	NO_TEST=1
87		B1	REG_BOOST_CPUCORE_4_RC	NO_TEST=1
87		B1	REG_BOOST_CPUCORE_5	NO_TEST=1
87		B1	REG_BOOST_CPUCORE_5_RC	NO_TEST=1
163	119	B1	REGSNUBPVDDR	NO_TEST=1
163	120	B1	REGSNUBPVPP	NO_TEST=1
163	84	B1	REG_6VR_FSW	NO_TEST=1
163	84	B1	REG_6VR_SS	NO_TEST=1
151	88	B1	CPU_ISNS_VCCIO_S0_N	NO_TEST=1
151	88	B1	CPU_ISNS_VCCIO_S0_P	NO_TEST=1
151	89	B1	CPU_ISNS_VCCSA_S0_N	NO_TEST=1
151	89	B1	CPU_ISNS_VCCSA_S0_P	NO_TEST=1
151	92	B1	CPU_ISNS_VDDQ01_S3_N	NO_TEST=1
151	92	B1	CPU_ISNS_VDDQ01_S3_P	NO_TEST=1
151	93	B1	CPU_ISNS_VDDQ23_S3_N	NO_TEST=1
151	93	B1	CPU_ISNS_VDDQ23_S3_P	NO_TEST=1
151	90	B1	CPU_ISNS_VPP01_S3_N	NO_TEST=1
151	90	B1	CPU_ISNS_VPP01_S3_P	NO_TEST=1
151	91	B1	CPU_ISNS_VPP23_S3_N	NO_TEST=1
151	91	B1	CPU_ISNS_VPP23_S3_P	NO_TEST=1
163	84	B1	REG_6VR_FSW	NO_TEST=1
163	84	B1	REG_6VR_SS	NO_TEST=1
88		B1	REG_BOOST_VCCIO	NO_TEST=1
119		B1	REG_BOOT_PVDDR	NO_TEST=1
117		B1	REG_BOOT_VDDCI	NO_TEST=1
117		B1	REG_BOOT_VDDCI_RC	NO_TEST=1
90		B1	REG_BOOT_VPP01	NO_TEST=1
91		B1	REG_BOOT_VPP23	NO_TEST=1
92		B1	REG_BST_CPU_VDDQ01	NO_TEST=1
93		B1	REG_BST_CPU_VDDQ23	NO_TEST=1
89		B1	REG_BST_VCCSA	NO_TEST=1
92		B1	REG_CPU_VDDQ01_SW	NO_TEST=1
93		B1	REG_CPU_VDDQ23_SW	NO_TEST=1
85		B1	REG_CPU_VINSNS	NO_TEST=1
84		B1	REG_DRVCPU_VSNS	NO_TEST=1
84		B1	REG_DRVCPU_VSNS_R	NO_TEST=1
84		B1	REG_DRV_VR_AGND	NO_TEST=1
91		B1	REG_FSEL_VPP23	NO_TEST=1
92		B1	REG_ISNS_CPU_VDDQ01_N	NO_TEST=1
92		B1	REG_ISNS_CPU_VDDQ01_P	NO_TEST=1
93		B1	REG_ISNS_CPU_VDDQ23_N	NO_TEST=1
93		B1	REG_ISNS_CPU_VDDQ23_P	NO_TEST=1
88		B1	REG_ISNS_REF_VCCIO	NO_TEST=1
88		B1	REG_ISNS_VCCIO	NO_TEST=1
117		B1	REG_LGATE_VDDCI	NO_TEST=1
90		B1	REG_LG_VPP01	NO_TEST=1
91		B1	REG_LG_VPP23	NO_TEST=1
86		B1	REG_PHASE_CPUCORE_1	NO_TEST=1
86		B1	REG_PHASE_CPUCORE_2	NO_TEST=1
86		B1	REG_PHASE_CPUCORE_3	NO_TEST=1
87		B1	REG_PHASE_CPUCORE_4	NO_TEST=1
87		B1	REG_PHASE_CPUCORE_5	NO_TEST=1
119		B1	REG_PHASE_PVDDR	NO_TEST=1
117		B1	REG_PHASE_VDDCI	NO_TEST=1
117		B1	REG_PHASE_VDDCI_L	NO_TEST=1
90		B1	REG_PHASE_VPP01	NO_TEST=1
90		B1	REG_PHASE_VPP01_L	NO_TEST=1
91		B1	REG_PHASE_VPP23	NO_TEST=1
91		B1	REG_PHASE_VPP23_L	NO_TEST=1
86	85	B1	REG_PWM_CPUCORE_1	NO_TEST=1
86	85	B1	REG_PWM_CPUCORE_2	NO_TEST=1
86	85	B1	REG_PWM_CPUCORE_3	NO_TEST=1
87	85	B1	REG_PWM_CPUCORE_4	NO_TEST=1
87	85	B1	REG_PWM_CPUCORE_5	NO_TEST=1
89	85	B1	REG_PWM_CPUVCCSA	NO_TEST=1
92		B1	REG_PWM_CPU_VDDQ01	NO_TEST=1
93		B1	REG_PWM_CPU_VDDQ23	NO_TEST=1
88		B1	REG_PWM_VCCIO	NO_TEST=1
119		B1	REG_RTCLK_PVDDR	NO_TEST=1
86		B1	REG_SNUBBER_CPUCORE_1	NO_TEST=1
86		B1	REG_SNUBBER_CPUCORE_2	NO_TEST=1
86		B1	REG_SNUBBER_CPUCORE_3	NO_TEST=1
87		B1	REG_SNUBBER_CPUCORE_4	NO_TEST=1
87		B1	REG_SNUBBER_CPUCORE_5	NO_TEST=1
117		B1	REG_SNUBBER_VDDCI	NO_TEST=1
90		B1	REG_SNUB_VPP01_RC	NO_TEST=1
91		B1	REG_SNUB_VPP23_RC	NO_TEST=1
119		B1	REG_SSTR_PVDDR	NO_TEST=1

CPU VOLTAGE REGULATORS

117		B1	REG_UGATE_VDDCI	NO_TEST=1
117		B1	REG_UGATE_VDDCI_R	NO_TEST=1
90		B1	REG_UG_VPP01	NO_TEST=1
90		B1	REG_UG_VPP01_R	NO_TEST=1
91		B1	REG_UG_VPP23	NO_TEST=1
91		B1	REG_UG_VPP23_R	NO_TEST=1
86	85	B1	REG_VCCIN_ISNS_1_N	NO_TEST=1
86	85	B1	REG_VCCIN_ISNS_1_P	NO_TEST=1
86	85	B1	REG_VCCIN_ISNS_2_N	NO_TEST=1
86	85	B1	REG_VCCIN_ISNS_2_P	NO_TEST=1
86	85	B1	REG_VCCIN_ISNS_3_N	NO_TEST=1
86	85	B1	REG_VCCIN_ISNS_3_P	NO_TEST=1
87	85	B1	REG_VCCIN_ISNS_4_N	NO_TEST=1
87	85	B1	REG_VCCIN_ISNS_4_P	NO_TEST=1
87	85	B1	REG_VCCIN_ISNS_5_N	NO_TEST=1
87	85	B1	REG_VCCIN_ISNS_5_P	NO_TEST=1
85		B1	REG_VCCIN_TSNS_A	NO_TEST=1
88		B1	REG_VCCIO_SW	NO_TEST=1
163	89	B1	REG_VCCSA_PH	NO_TEST=1
163	89	B1	REG_VCCSA_PH	NO_TEST=1
89		B1	REG_VCCSA_SNUB	NO_TEST=1
85		B1	REG_VCCSA_TSNS_B	NO_TEST=1
117		B1	REG_VDDCI_FB	NO_TEST=1
117	99	B1	REG_VDDCI_FB_P	NO_TEST=1
117		B1	REG_VDDCI_FSEL	NO_TEST=1
117		B1	REG_VDDCI_OCSET	NO_TEST=1
117		B1	REG_VDDCI_RTN	NO_TEST=1
117		B1	REG_VDDCI_SET0	NO_TEST=1
117		B1	REG_VDDCI_SET1	NO_TEST=1
117		B1	REG_VDDCI_SREF	NO_TEST=1
92		B1	REG_VIN_SNS_CPU_VDDQ01	NO_TEST=1
88		B1	REG_VIN_SNS_VCCIO	NO_TEST=1
163	93	B1	REG_VIN_SNS_VDDQ23	NO_TEST=1
163	93	B1	REG_VIN_SNS_VDDQ23	NO_TEST=1
90		B1	REG_VPP01	NO_TEST=1
90		B1	REG_VPP01_FB	NO_TEST=1
90		B1	REG_VPP01_FB_XW_N	NO_TEST=1
90		B1	REG_VPP01_FB_XW_P	NO_TEST=1
90		B1	REG_VPP01_OCSET	NO_TEST=1
90		B1	REG_VPP01_RTN	NO_TEST=1
90		B1	REG_VPP01_SREF	NO_TEST=1
90		B1	REG_VPP01_VO	NO_TEST=1
91		B1	REG_VPP23_FB	NO_TEST=1
91		B1	REG_VPP23_FB_XW_N	NO_TEST=1
91		B1	REG_VPP23_FB_XW_P	NO_TEST=1
91		B1	REG_VPP23_OCSET	NO_TEST=1
91		B1	REG_VPP23_RTN	NO_TEST=1
91		B1	REG_VPP23_SREF	NO_TEST=1
91		B1	REG_VPP23_VO	NO_TEST=1
119		B1	REG_VSNSR_PVDDR	NO_TEST=1
85	15	B1	REG_VSNS_CPU_VCCIN_N	NO_TEST=1
85		B1	REG_VSNS_CPU_VCCIN_P_R	NO_TEST=1
88	14	B1	REG_VSNS_CPU_VCCIO_N	NO_TEST=1
88		B1	REG_VSNS_CPU_VCCIO_P_R	NO_TEST=1
85	14	B1	REG_VSNS_CPU_VCCSA_N	NO_TEST=1
85		B1	REG_VSNS_CPU_VCCSA_P_R	NO_TEST=1
92		B1	REG_VSNS_CPU_VDDQ01_N	NO_TEST=1
92		B1	REG_VSNS_CPU_VDDQ01_R_P	NO_TEST=1
93		B1	REG_VSNS_CPU_VDDQ23_R_P	NO_TEST=1
119		B1	REG_VSNS_PVDDR	NO_TEST=1
90		B1	REG_VTT01_REFIN	NO_TEST=1
91		B1	REG_VTT23_REFIN	NO_TEST=1
93		B1	SNUB_CPU_VDDQ23_RC	
92		B1	SNUB_CPU_VDDQ_01	

WIRELESS ANTENNAS

136		B1	50_0_ANT	NO_TEST=1
136		B1	50_0_COM	NO_TEST=1
136		B1	50_A_0_DIPLEXER	NO_TEST=1
136		B1	50_G_0_DIPLEXER	NO_TEST=1
136	134	B1	50_A_0_MATCH	NO_TEST=1
136	134	B1	50_G_0_MATCH	NO_TEST=1
136		B1	50_1_ANT	NO_TEST=1
136		B1	50_1_COM	NO_TEST=1
136		B1	50_A_1_DIPLEXER	NO_TEST=1
136		B1	50_G_1_DIPLEXER	NO_TEST=1
136	134	B1	50_A_1_MATCH	NO_TEST=1
136	134	B1	50_G_1_MATCH	NO_TEST=1
136		B1	50_2_ANT	NO_TEST=1
136		B1	50_2_COM	NO_TEST=1
136		B1	50_A_2_DIPLEXER	NO_TEST=1
136		B1	50_G_2_DIPLEXER	NO_TEST=1
136	134	B1	50_A_2_MATCH	NO_TEST=1
136	134	B1	50_G_2_MATCH	NO_TEST=1
136		B1	50_3_ANT	NO_TEST=1
136		B1	50_3_ANT_IND	NO_TEST=1
136		B1	BT_ONLY_MATCH_IND	NO_TEST=1
165	136	134	B1	BT_ONLY_MATCH	NO_TEST=1

SYSTEM VOLTAGE REGULATORS

82		B1	P5V_G3S_SNS_P	NO_TEST=1
82		B1	REG_BOOT_P3V3G3H	NO_TEST=1
82		B1	REG_BOOT_P3V3G3H_RC	NO_TEST=1
82		B1	REG_BOOT_P5VG3S	NO_TEST=1
82		B1	REG_BOOT_P5VG3S_RC	NO_TEST=1
82		B1	REG_LGATE_P3V3G3H	NO_TEST=1
82		B1	REG_LGATE_P5VG3S	NO_TEST=1
82		B1	REG_P3V3G3H_DCR_ISNS_N	NO_TEST=1
82		B1	REG_P3V3G3H_DCR_ISNS_P	NO_TEST=1
82		B1	REG_P3V3G3H_FSET	NO_TEST=1
82		B1	REG_P3V3G3H_ISEN	NO_TEST=1
82		B1	REG_P3V3G3H_OCSET	NO_TEST=1
82		B1	REG_P3V3G3H_VOUT	NO_TEST=1
82		B1	REG_P3V3G3H_VOUT_R	NO_TEST=1
82		B1	REG_P5VG3S_FB	NO_TEST=1
82		B1	REG_P5VG3S_FSET	NO_TEST=1
82		B1	REG_P5VG3S_ISEN	NO_TEST=1
82		B1	REG_P5VG3S_OCSET	NO_TEST=1
82		B1	REG_P5VG3S_VOUT_R	NO_TEST=1
82		B1	REG_PHASE_P3V3G3H	NO_TEST=1
82		B1	REG_PHASE_P3V3G3H_TGR	NO_TEST=1
82		B1	REG_PHASE_P5VG3S	NO_TEST=1
82		B1	REG_SNUBBER_P3V3G3H	NO_TEST=1
82		B1	REG_SNUBBER_P5VG3S	NO_TEST=1
82		B1	REG_UGATE_P3V3G3H	NO_TEST=1
82		B1	REG_UGATE_P5VG3S	NO_TEST=1
82		B1	REG_VIN_U8600	NO_TEST=1
79		B1	REG_SNUBBER_P3V3G3W	NO_TEST=1
79		B1	REG_P3V3G3W_VOUT_R	NO_TEST=1
79		B1	REG_VIN_U8300	NO_TEST=1
79		B1	REG_VCCI_U8300	NO_TEST=1
79		B1	REG_UGATE_P3V3G3W	NO_TEST=1
79		B1	REG_LGATE_P3V3G3W	NO_TEST=1
79		B1	REG_BOOT_P3V3G3W	NO_TEST=1
79		B1	REG_P3V3G3W_ISEN	NO_TEST=1
163	79	B1	REG_P3V3G3W_VOUT	NO_TEST=1
79		B1	REG_P3V3G3W_FSET	NO_TEST=1
163	79	B1	REG_P3V3G3W_VOUT	NO_TEST=1
79		B1	REG_P5VG3S_FCCM	NO_TEST=1
79		B1	REG_UGATE_P5VG3S_USBC	NO_TEST=1
79		B1	REG_BOOT_P5VG3S_USBC	NO_TEST=1
79		B1	REG_PHASE_P5VG3S_USBC_TGR	NO_TEST=1
79		B1	REG_LGATE_P5VG3S_USBC	NO_TEST=1
79		B1	REG_P5VG3S_USBC_ISEN	NO_TEST=1
79		B1	REG_P5VG3S_USBC_OCSET	NO_TEST=1
79		B1	REG_P5VG3S_USBC_VOUT	NO_TEST=1
79		B1	REG_P5VG3S_USBC_FSET	NO_TEST=1
79		B1	REG_P5VG3S_USBC_FB	NO_TEST=1
79		B1	REG_BOOT_P5VG3S_USBC_RC	NO_TEST=1
79		B1	REG_P5VG3S_USBC_VOUT_R	NO_TEST=1
79		B1	REG_SNUBBER_P5VG3S_USBC	NO_TEST=1

BOM_COST_GROUP=PCB

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ICT NO TEST <RDAR://30758642>

USB-C

27	24	BI	DP_TA_AUXCH_P	NO_TEST=1
27	24	BI	DP_TA_AUXCH_N	NO_TEST=1
	24	BI	DP_TA_AUXCH_C_P	NO_TEST=1
	24	BI	DP_TA_AUXCH_C_N	NO_TEST=1
28	24	BI	DP_TB_AUXCH_P	NO_TEST=1
28	24	BI	DP_TB_AUXCH_N	NO_TEST=1
	24	BI	DP_TB_AUXCH_C_P	NO_TEST=1
	24	BI	DP_TB_AUXCH_C_N	NO_TEST=1
165	33	30	BI	DP_XA_AUXCH_P	NO_TEST=1
165	33	30	BI	DP_XA_AUXCH_N	NO_TEST=1
165		30	BI	DP_XA_AUXCH_C_P	NO_TEST=1
165		30	BI	DP_XA_AUXCH_C_N	NO_TEST=1
165	34	30	BI	DP_XB_AUXCH_P	NO_TEST=1
165	34	30	BI	DP_XB_AUXCH_N	NO_TEST=1
165		30	BI	DP_XB_AUXCH_C_P	NO_TEST=1
165		30	BI	DP_XB_AUXCH_C_N	NO_TEST=1
24	23	BI	USBC_TA_D2R_P<2..1>	NO_TEST=1
24	23	BI	USBC_TA_D2R_N<2..1>	NO_TEST=1
	23	BI	USBC_TA_D2R_CONN_P<2..1>	NO_TEST=1
	23	BI	USBC_TA_D2R_CONN_N<2..1>	NO_TEST=1
24	23	BI	USBC_TA_R2D_C_P<2..1>	NO_TEST=1
24	23	BI	USBC_TA_R2D_C_N<2..1>	NO_TEST=1
24	23	BI	USBC_TB_D2R_P<2..1>	NO_TEST=1
24	23	BI	USBC_TB_D2R_N<2..1>	NO_TEST=1
	23	BI	USBC_TB_D2R_CONN_P<2..1>	NO_TEST=1
	23	BI	USBC_TB_D2R_CONN_N<2..1>	NO_TEST=1
24	23	BI	USBC_TB_R2D_C_P<2..1>	NO_TEST=1
24	23	BI	USBC_TB_R2D_C_N<2..1>	NO_TEST=1
30	29	BI	USBC_XA_D2R_P<2..1>	NO_TEST=1
30	29	BI	USBC_XA_D2R_N<2..1>	NO_TEST=1
	29	BI	USBC_XA_D2R_CONN_P<2..1>	NO_TEST=1
	29	BI	USBC_XA_D2R_CONN_N<2..1>	NO_TEST=1
30	29	BI	USBC_XA_R2D_C_P<2..1>	NO_TEST=1
30	29	BI	USBC_XA_R2D_C_N<2..1>	NO_TEST=1
30	29	BI	USBC_XB_D2R_P<2..1>	NO_TEST=1
30	29	BI	USBC_XB_D2R_N<2..1>	NO_TEST=1
	29	BI	USBC_XB_D2R_CONN_P<2..1>	NO_TEST=1
	29	BI	USBC_XB_D2R_CONN_N<2..1>	NO_TEST=1
30	29	BI	USBC_XB_R2D_C_P<2..1>	NO_TEST=1
30	29	BI	USBC_XB_R2D_C_N<2..1>	NO_TEST=1
	23	BI	USBC_TA_D2R_RC_N<2>	NO_TEST=1
	23	BI	USBC_TA_D2R_RC_P<2>	NO_TEST=1
	23	BI	USBC_TA_D2R_RC_N<1>	NO_TEST=1
	23	BI	USBC_TA_D2R_RC_P<1>	NO_TEST=1
	23	BI	USBC_TA_R2D_CONN_N<1>	NO_TEST=1
	23	BI	USBC_TA_R2D_CONN_N<2>	NO_TEST=1
	23	BI	USBC_TA_R2D_CONN_P<1>	NO_TEST=1
	23	BI	USBC_TA_R2D_CONN_P<2>	NO_TEST=1
	23	BI	USBC_TA_R2D_RC_N<1>	NO_TEST=1
	23	BI	USBC_TA_R2D_RC_P<1>	NO_TEST=1
	23	BI	USBC_TA_R2D_RC_N<2>	NO_TEST=1
	23	BI	USBC_TA_R2D_RC_P<2>	NO_TEST=1
	23	BI	USBC_TB_D2R_RC_N<2>	NO_TEST=1
	23	BI	USBC_TB_D2R_RC_P<2>	NO_TEST=1
	23	BI	USBC_TB_D2R_RC_N<1>	NO_TEST=1
	23	BI	USBC_TB_D2R_RC_P<1>	NO_TEST=1
	23	BI	USBC_TB_R2D_CONN_N<1>	NO_TEST=1
	23	BI	USBC_TB_R2D_CONN_N<2>	NO_TEST=1
	23	BI	USBC_TB_R2D_CONN_P<1>	NO_TEST=1
	23	BI	USBC_TB_R2D_CONN_P<2>	NO_TEST=1
	23	BI	USBC_TB_R2D_RC_N<1>	NO_TEST=1
	23	BI	USBC_TB_R2D_RC_P<1>	NO_TEST=1
	23	BI	USBC_TB_R2D_RC_N<2>	NO_TEST=1
	23	BI	USBC_TB_R2D_RC_P<2>	NO_TEST=1
	29	BI	USBC_XA_D2R_RC_N<2>	NO_TEST=1
	29	BI	USBC_XA_D2R_RC_P<2>	NO_TEST=1
	29	BI	USBC_XA_D2R_RC_N<1>	NO_TEST=1
	29	BI	USBC_XA_D2R_RC_P<1>	NO_TEST=1
	29	BI	USBC_XA_R2D_CONN_N<1>	NO_TEST=1
	29	BI	USBC_XA_R2D_CONN_N<2>	NO_TEST=1
	29	BI	USBC_XA_R2D_CONN_P<1>	NO_TEST=1
	29	BI	USBC_XA_R2D_CONN_P<2>	NO_TEST=1
	29	BI	USBC_XA_R2D_RC_N<1>	NO_TEST=1
	29	BI	USBC_XA_R2D_RC_P<1>	NO_TEST=1
	29	BI	USBC_XA_R2D_RC_N<2>	NO_TEST=1
	29	BI	USBC_XA_R2D_RC_P<2>	NO_TEST=1
	29	BI	USBC_XB_D2R_RC_N<2>	NO_TEST=1
	29	BI	USBC_XB_D2R_RC_P<2>	NO_TEST=1
	29	BI	USBC_XB_D2R_RC_N<1>	NO_TEST=1
	29	BI	USBC_XB_D2R_RC_P<1>	NO_TEST=1
	29	BI	USBC_XB_R2D_CONN_N<1>	NO_TEST=1
	29	BI	USBC_XB_R2D_CONN_N<2>	NO_TEST=1
	29	BI	USBC_XB_R2D_CONN_P<1>	NO_TEST=1
	29	BI	USBC_XB_R2D_CONN_P<2>	NO_TEST=1
	29	BI	USBC_XB_R2D_RC_N<1>	NO_TEST=1
	29	BI	USBC_XB_R2D_RC_P<1>	NO_TEST=1
	29	BI	USBC_XB_R2D_RC_N<2>	NO_TEST=1
	29	BI	USBC_XB_R2D_RC_P<2>	NO_TEST=1

NO CONNECTS

27	BI	NC_UPC_TA_HV_GATE1	NO_TEST=1
27	BI	NC_UPC_TA_HV_GATE2	NO_TEST=1
28	BI	NC_UPC_TB_HV_GATE1	NO_TEST=1
28	BI	NC_UPC_TB_HV_GATE2	NO_TEST=1
28	BI	NC_UPC_TB_I2C_ADDR	NO_TEST=1
33	BI	NC_UPC_XA_HV_GATE1	NO_TEST=1
33	BI	NC_UPC_XA_HV_GATE2	NO_TEST=1
33	BI	NC_USBC_XA_USB_BOT_P	NO_TEST=1
33	BI	NC_USBC_XA_USB_BOT_N	NO_TEST=1
34	BI	NC_UPC_XB_HV_GATE1	NO_TEST=1
34	BI	NC_UPC_XB_HV_GATE2	NO_TEST=1
34	BI	NC_UPC_XB_I2C_ADDR	NO_TEST=1
61	BI	NC_SSD0_S3X_JTAG_TCK	NO_TEST=1
61	BI	NC_SSD0_S3X_JTAG_TMS	NO_TEST=1
61	BI	NC_SSD0_STG01_ADDR	NO_TEST=1
62	BI	NC_SSD1_S3X_JTAG_TCK	NO_TEST=1
62	BI	NC_SSD1_S3X_JTAG_TMS	NO_TEST=1
147	BI	NC_TSNS_T2_DX7N	NO_TEST=1

PMIC VOLTAGE REGULATORS

	74	BI	P0V9SLPDDR_FB	NO_TEST=1
	74	BI	P0V9SLPDDR_SW0	NO_TEST=1
	74	BI	P0V9SLPDDR_SW1	NO_TEST=1
	74	BI	P1V1SLPS2R_FB	NO_TEST=1
	74	BI	P1V1SLPS2R_SW0	NO_TEST=1
	74	BI	P1V1SLPS2R_SW1	NO_TEST=1
	74	BI	P1V8SLPS2R_FB	NO_TEST=1
	74	BI	P1V8SLPS2R_SW0	NO_TEST=1
	78	BI	P1V8_SLPS2R_CT	NO_TEST=1
122	74	BI	P1V0_PCH_CORE_S5_FB	NO_TEST=1
122	74	BI	P0V82SLPDDR_FB	NO_TEST=1
	74	BI	P0V82SLPDDR_SW0	NO_TEST=1
	74	BI	P0V82SLPDDR_SW1	NO_TEST=1
122	74	BI	PVDDCPUAWAKE_FB	NO_TEST=1
	74	BI	PVDDCPUAWAKE_SW0	NO_TEST=1
	74	BI	PVDDCPUAWAKE_SW1	NO_TEST=1
	74	BI	PVDDCPUAWAKE_SW2	NO_TEST=1
	74	BI	PVDDCPUAWAKE_SW3	NO_TEST=1
	74	BI	PVDDCPUSRAMAWAKE_FB	NO_TEST=1
	74	BI	PVDDCPUSRAMAWAKE_SW0	NO_TEST=1

BLC VOLTAGE REGULATORS

109	BI	BKLT_SNUBBER	NO_TEST=1
109	BI	BKLT_BST_FB	NO_TEST=1
109	BI	BKLT_BST_FB_R	NO_TEST=1

BOM_COST_GROUP=PCB

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130 127	BI	AUD_HP_PORT_US_GND	NO_TEST=1
128	BI	AUD_LAMP_BOOTLTN	NO_TEST=1
128	BI	AUD_LAMP_BOOTLTP	NO_TEST=1
128	BI	AUD_LAMP_BOOTLWN	NO_TEST=1
128	BI	AUD_LAMP_BOOTLWP	NO_TEST=1
128	BI	AUD_LAMP_LT_ADR	NO_TEST=1
128	BI	AUD_LAMP_LW_GVDD	NO_TEST=1
128	BI	AUD_LAMP_LW_VCOM	NO_TEST=1
128	BI	AUD_LAMP_LW_VREG	NO_TEST=1
127 76	BI	AUD_PWR_EN	NO_TEST=1
129	BI	AUD_RAMP_BOOTRTN	NO_TEST=1
129	BI	AUD_RAMP_BOOTRTP	NO_TEST=1
129	BI	AUD_RAMP_BOOTRWN	NO_TEST=1
129	BI	AUD_RAMP_BOOTRWP	NO_TEST=1
129	BI	AUD_SPKR_RTWT_OUT_L_N	NO_TEST=1
129	BI	AUD_SPKR_RTWT_OUT_L_P	NO_TEST=1
129	BI	AUD_SPKR_RWFR_OUT_L_N	NO_TEST=1
129	BI	AUD_SPKR_RWFR_OUT_L_P	NO_TEST=1
109	BI	BKLT_SNSN	NO_TEST=1
109	BI	BKLT_SNSP	NO_TEST=1
43 35	BI	BOARD_REV0	NO_TEST=1
43 35	BI	BOARD_REV1	NO_TEST=1
43 37	BI	BOARD_REV2	NO_TEST=1
43 35	BI	BOOT_CONFIG0	NO_TEST=1
43 35	BI	BOOT_CONFIG1	NO_TEST=1
43 35	BI	BOOT_CONFIG2	NO_TEST=1
163 136 134	BI	BT_ONLY_MATCH	NO_TEST=1
137 134	BI	BT_SF_CLK	NO_TEST=1
137 134	BI	BT_SF_CS_L	NO_TEST=1
137	BI	BT_SF_CS_L_R	NO_TEST=1
137	BI	BT_SF_HOLD_L	NO_TEST=1
137 134	BI	BT_SF_MISO	NO_TEST=1
137 134	BI	BT_SF_MOSI	NO_TEST=1
137	BI	BT_SF_WP_L	NO_TEST=1
156	BI	CPU_CATERR_R_L	NO_TEST=1
155	BI	CPU_ERROR_0_LED	NO_TEST=1
155	BI	CPU_ERROR_0_LED_R	NO_TEST=1
155	BI	CPU_ERROR_0_Q	NO_TEST=1
155	BI	CPU_ERROR_1_LED	NO_TEST=1
155	BI	CPU_ERROR_1_LED_R	NO_TEST=1
155	BI	CPU_ERROR_1_Q	NO_TEST=1
155	BI	CPU_ERROR_2_LED	NO_TEST=1
155	BI	CPU_ERROR_2_LED_R	NO_TEST=1
155	BI	CPU_ERROR_2_Q	NO_TEST=1
155	BI	CPU_ERROR_L_0_R	NO_TEST=1
155	BI	CPU_ERROR_L_1_R	NO_TEST=1
155	BI	CPU_ERROR_L_2_R	NO_TEST=1
155	BI	CPU_FIVR_FAULT_LED	NO_TEST=1
155	BI	CPU_FIVR_FAULT_LED_R	NO_TEST=1
155	BI	CPU_FIVR_FAULT_R	NO_TEST=1
155	BI	CPU_PROCHOT_LED	NO_TEST=1
155	BI	CPU_PROCHOT_LED_R	NO_TEST=1
155	BI	CPU_PROCHOT_Q	NO_TEST=1
155	BI	CPU_PROCHOT_R1_L	NO_TEST=1
155	BI	CPU_THERMTRIP_LED	NO_TEST=1
155	BI	CPU_THERMTRIP_LED_R	NO_TEST=1
155	BI	CPU_THERMTRIP_L_R	NO_TEST=1
155	BI	CPU_THERMTRIP_Q	NO_TEST=1
164 30	BI	DP_XA_AUXCH_C_N	NO_TEST=1
164 30	BI	DP_XA_AUXCH_C_P	NO_TEST=1
164 33 30	BI	DP_XA_AUXCH_N	NO_TEST=1
164 33 30	BI	DP_XA_AUXCH_P	NO_TEST=1
164 30	BI	DP_XB_AUXCH_C_N	NO_TEST=1
164 30	BI	DP_XB_AUXCH_C_P	NO_TEST=1
164 34 30	BI	DP_XB_AUXCH_N	NO_TEST=1
164 34 30	BI	DP_XB_AUXCH_P	NO_TEST=1
30	BI	DP_X_SNK_RBIAS	NO_TEST=1
126	BI	DUT_VDD_CPU_1V0_MON_U	NO_TEST=1
126	BI	DUT_VDD_CPU_SENSE_U	NO_TEST=1
126	BI	DUT_VDD_SOC_SENSE_U	NO_TEST=1
57	BI	ENET_A_CMC_N	NO_TEST=1

57	BI	ENET_A_CMC_P	NO_TEST=1
57	BI	ENET_A_CT_CONN	NO_TEST=1
57	BI	ENET_A_CT_PHY	NO_TEST=1
54	BI	ENET_BG_REXT1_R	NO_TEST=1
57	BI	ENET_B_CMC_N	NO_TEST=1
57	BI	ENET_B_CMC_P	NO_TEST=1
57	BI	ENET_B_CT_CONN	NO_TEST=1
57	BI	ENET_B_CT_PHY	NO_TEST=1
66	BI	ENET_CLKREQ_PCH_L	NO_TEST=1
57	BI	ENET_C_CMC_N	NO_TEST=1
57	BI	ENET_C_CMC_P	NO_TEST=1
57	BI	ENET_C_CT_CONN	NO_TEST=1
57	BI	ENET_C_CT_PHY	NO_TEST=1
57	BI	ENET_D_CMC_N	NO_TEST=1
57	BI	ENET_D_CMC_P	NO_TEST=1
57	BI	ENET_D_CT_CONN	NO_TEST=1
57	BI	ENET_D_CT_PHY	NO_TEST=1
57	BI	ENET_EFUSE_EN	NO_TEST=1
56	BI	ENET_MISO_R	NO_TEST=1
54	BI	ENET_RG_K12	NO_TEST=1
55	BI	ENET_RNC_N9	NO_TEST=1
54	BI	ENET_SMB_CLK_R	NO_TEST=1
54	BI	ENET_SMB_DAT_R	NO_TEST=1
72 54	BI	ENET_SYNC_1588	NO_TEST=1
72 69	BI	ENET_SYNC_1588_IN	NO_TEST=1
72 68	BI	ENET_SYNC_1588_OUT	NO_TEST=1
56 55	BI	ENET_TSENS_A_N	NO_TEST=1
56 55	BI	ENET_TSENS_A_P	NO_TEST=1
56 55	BI	ENET_TSENS_E_N	NO_TEST=1
148 56	BI	ENET_TSENS_N	NO_TEST=1
148 56	BI	ENET_TSENS_P	NO_TEST=1
56	BI	ENET_XTAL1	NO_TEST=1
56	BI	ENET_XTAL0	NO_TEST=1
56	BI	ENET_XTAL0_R	NO_TEST=1
54	BI	ENET_XTAL_SELECT_L	NO_TEST=1
124 66 36	BI	ESPI_CLK	NO_TEST=1
66	BI	ESPI_CLK60M_R	NO_TEST=1
124	BI	ESPI_IO_HDR<0>	NO_TEST=1
124	BI	ESPI_IO_HDR<1>	NO_TEST=1
124	BI	ESPI_IO_HDR<2>	NO_TEST=1
124	BI	ESPI_IO_HDR<3>	NO_TEST=1
36	BI	ESPI_IO_R<0>	NO_TEST=1
36	BI	ESPI_IO_R<1>	NO_TEST=1
36	BI	ESPI_IO_R<2>	NO_TEST=1
36	BI	ESPI_IO_R<3>	NO_TEST=1
116	BI	FBMVDD_ALTV0_R	NO_TEST=1
116	BI	FBMVDD_ALTV1_R	NO_TEST=1
118	BI	FBP0V8_ALTV0_R	NO_TEST=1
118	BI	FBP0V8_ALTV1_R	NO_TEST=1
117	BI	FBVDDCI_ALTV0_R	NO_TEST=1
117	BI	FBVDDCI_ALTV1_R	NO_TEST=1
99	BI	FB_VDDCI_MEM	NO_TEST=1
99	BI	FB_VDDCR_HBM	NO_TEST=1
99	BI	FB_VDDCR_SOC	NO_TEST=1
99	BI	FB_VDDIO_MEM_GPU	NO_TEST=1
99	BI	FB_VDDIO_MEM_HBM	NO_TEST=1
99	BI	FB_VSS_A	NO_TEST=1
131	BI	GND_AUD_DMIC_1_CONN	NO_TEST=1
97	BI	GPU_GPIO_14	NO_TEST=1
151 116	BI	GPU_ISNS_MVDD_N	NO_TEST=1
151 116	BI	GPU_ISNS_MVDD_P	NO_TEST=1
98 94	BI	GPU_REF_CLK100M_N	NO_TEST=1
98 94	BI	GPU_REF_CLK100M_P	NO_TEST=1
127	BI	HS_MICN	NO_TEST=1
127	BI	HS_MICP	NO_TEST=1
150	BI	HS_P3V3_G3W_SSD0_OUT	NO_TEST=1
85	BI	I2C_CPU_VCCIN_SCL	NO_TEST=1
85	BI	I2C_CPU_VCCIN_SDA	NO_TEST=1
43 35	BI	I2C_SEP_SCL	NO_TEST=1
43 35	BI	I2C_SEP_SDA	NO_TEST=1
26 24	BI	I2C_TBT_T_RIDGE_SCL	NO_TEST=1
32 30	BI	I2C_TBT_X_RIDGE_SCL	NO_TEST=1
32 30	BI	I2C_TBT_X_RIDGE_SDA	NO_TEST=1
88	BI	I2C_VCCIO_SCL	NO_TEST=1
88	BI	I2C_VCCIO_SDA	NO_TEST=1
92	BI	I2C_VDDQ01_SCL	NO_TEST=1
92	BI	I2C_VDDQ01_SDA	NO_TEST=1
93	BI	I2C_VDDQ23_SCL	NO_TEST=1
93	BI	I2C_VDDQ23_SDA	NO_TEST=1

44 37	BI	I2S_CODEC_BCLK_R	NO_TEST=1
127	BI	I2S_CODEC_BCLK_RR	NO_TEST=1
127	BI	I2S_CODEC_D2R_R	NO_TEST=1
127	BI	I2S_CODEC_LRCLK_RR	NO_TEST=1
44 37	BI	I2S_CODEC_R2D_R	NO_TEST=1
127	BI	I2S_CODEC_R2D_RR	NO_TEST=1
44 37	BI	I2S_SPKRAMP_L_BCLK_R	NO_TEST=1
44 37	BI	I2S_SPKRAMP_L_MCLK_R	NO_TEST=1
44 37	BI	I2S_SPKRAMP_L_R2D_R	NO_TEST=1
44 37	BI	I2S_SPKRAMP_R_BCLK_R	NO_TEST=1
44 37	BI	I2S_SPKRAMP_R_R2D_R	NO_TEST=1
51	BI	J5500_PIN_5	NO_TEST=1
127	BI	L83_FLYC	NO_TEST=1
127	BI	L83_FLYN	NO_TEST=1
127	BI	L83_FLYP	NO_TEST=1
127	BI	L83_HSBIAS_FILT	NO_TEST=1
127	BI	L83_HSBIAS_FILT_REF	NO_TEST=1
127	BI	L83_VCP_FILTN	NO_TEST=1
75	BI	LDO_CORE	NO_TEST=1
75	BI	LDO_RTC	NO_TEST=1
154	BI	LED_CPU_CE	NO_TEST=1
156 154	BI	LED_CPU_CE_Q	NO_TEST=1
154	BI	LED_CPU_CE_R	NO_TEST=1
154	BI	LED_DDR	NO_TEST=1
154	BI	LED_DDR_R	NO_TEST=1
154	BI	LED_ENET_EN_R	NO_TEST=1
154	BI	LED_G3S	NO_TEST=1
154	BI	LED_G3S_R	NO_TEST=1
154	BI	LED_G3W	NO_TEST=1
154	BI	LED_G3W_R	NO_TEST=1
154	BI	LED_GPU_TT	NO_TEST=1
156 154	BI	LED_GPU_TT_Q	NO_TEST=1
154	BI	LED_GPU_TT_R	NO_TEST=1
154	BI	LED_MAIN	NO_TEST=1
154	BI	LED_MAIN_R	NO_TEST=1
154	BI	LED_PM_TT	NO_TEST=1
156 154	BI	LED_PM_TT_Q	NO_TEST=1
154	BI	LED_PM_TT_R	NO_TEST=1
154	BI	LED_S0_RUN	NO_TEST=1
154	BI	LED_S0_RUN_R	NO_TEST=1
154	BI	LED_S2R	NO_TEST=1
154	BI	LED_S2R_R	NO_TEST=1
154	BI	LED_SMC_PH	NO_TEST=1
156 154	BI	LED_SMC_PH_Q	NO_TEST=1
154	BI	LED_SMC_PH_R	NO_TEST=1
154	BI	LED_SOCHOT	NO_TEST=1
156 154	BI	LED_SOCHOT_Q	NO_TEST=1
154	BI	LED_SOCHOT_R	NO_TEST=1
154	BI	LED_SOC_DFU	NO_TEST=1
154	BI	LED_SOC_DFU_R	NO_TEST=1
154	BI	LED_TBT_EN_R	NO_TEST=1
154	BI	LED_VCCIO	NO_TEST=1
154	BI	LED_VCCIO_R	NO_TEST=1
51	BI	MIPI_A1N	NO_TEST=1
51	BI	MIPI_A1P	NO_TEST=1
51	BI	MIPI_B1N	NO_TEST=1
51	BI	MIPI_B1P	NO_TEST=1
51 37	BI	MIPI_FTCAM_CLK_N	NO_TEST=1
51 37	BI	MIPI_FTCAM_CLK_P	NO_TEST=1
51	BI	MIPI_FTCAM_C_CLK_N	NO_TEST=1
51	BI	MIPI_FTCAM_C_CLK_P	NO_TEST=1
51	BI	MIPI_FTCAM_C_DATA_N<0>	NO_TEST=1
51	BI	MIPI_FTCAM_C_DATA_N<1>	NO_TEST=1
51	BI	MIPI_FTCAM_C_DATA_P<0>	NO_TEST=1
51	BI	MIPI_FTCAM_C_DATA_P<1>	NO_TEST=1
51 37	BI	MIPI_FTCAM_DATA_N<0>	NO_TEST=1
51 37	BI	MIPI_FTCAM_DATA_N<1>	NO_TEST=1
51 37	BI	MIPI_FTCAM_DATA_P<0>	NO_TEST=1
51 37	BI	MIPI_FTCAM_DATA_P<1>	NO_TEST=1
51	BI	MIPI_LED_A	NO_TEST=1
51	BI	MIPI_LED_K	NO_TEST=1
51	BI	MIPI_SW_BYP0	NO_TEST=1
51	BI	MIPI_SW_BYP1	NO_TEST=1
51	BI	MIPI_SW_BYP2	NO_TEST=1
51	BI	MIPI_SW_BYP3	NO_TEST=1
51	BI	MIPI_SW_BYP4	NO_TEST=1
51	BI	MIPI_SW_BYP5	NO_TEST=1
51	BI	MIPI_SW_G0	NO_TEST=1
51	BI	MIPI_SW_G1	NO_TEST=1

51	BI	MIPI_SW_G2	NO_TEST=1
51	BI	MIPI_SW_G3	NO_TEST=1
51	BI	MIPI_SW_G4	NO_TEST=1
51	BI	MIPI_SW_G5	NO_TEST=1
122	BI	P0V82SLPDDR_FB_ALT	NO_TEST=1
122	BI	P1V0_PCH_CORE_S5_FB_ALT	NO_TEST=1
75	BI	P1V1SLPDDR_RAMP	NO_TEST=1
78	BI	P3V3S5_RAMP	NO_TEST=1
78	BI	P3V3_G3S_CT	NO_TEST=1
137	BI	PCH_BT_ROM_BOOT_ISO	NO_TEST=1
71	BI	PCH_CLK32K_RTCX1_OSC	NO_TEST=1
71 67	BI	PCH_CLK32K_RTCX1_R	NO_TEST=1
71	BI	PCH_CLK32K_RTCX2_OSC	NO_TEST=1
71 67	BI	PCH_CLK32K_RTCX2_R	NO_TEST=1
66	BI	PCH_DIFFCLK_BIASREF	NO_TEST=1
72	BI	PCH_GPD_0_FET	NO_TEST=1
67	BI	PCH_INTRUDER_L	NO_TEST=1
67	BI	PCH_SUSACK_L	NO_TEST=1
69	BI	PCH_UART2_CTS_L	NO_TEST=1
68	BI	PCH_USB2_TD	NO_TEST=1
68	BI	PCH_USB_VBUSSENSE	NO_TEST=1
66	BI	PCH_XTAL24_IN	NO_TEST=1
66	BI	PCH_XTAL24_IN_R	NO_TEST=1
66	BI	PCH_XTAL24_OUT	NO_TEST=1
66	BI	PCH_XTAL24_OUT_R	NO_TEST=1
44 36	BI	PDM_DMIC_CLK0_R	NO_TEST=1
44 36	BI	PDM_DMIC_CLK1_R	NO_TEST=1
69	BI	PD_PCH_GPP_I0	NO_TEST=1
69	BI	PD_PCH_GPP_I1	NO_TEST=1
69	BI	PD_PCH_GPP_I2	NO_TEST=1
69	BI	PD_PCH_GPP_I4	NO_TEST=1
66	BI	PEG_CLKREQ_PCH_L	NO_TEST=1
155	BI	PLT_RESET_L_LED	NO_TEST=1
155	BI	PLT_RESET_L_LED_R	NO_TEST=1
145	BI	PLT_RST_BUF_ENET_L	NO_TEST=1
145	BI	PLT_RST_BUF_GPU_L	NO_TEST=1
145	BI	PLT_RST_BUF_SD_L	NO_TEST=1
145	BI	PLT_RST_BUF_TBT_T_L	NO_TEST=1
145	BI	PLT_RST_BUF_TBT_X_L	NO_TEST=1
145	BI	PLT_RST_BUF_WLAN_L	NO_TEST=1
76	BI	PMU_CLK32K_PCH_R	NO_TEST=1
76	BI	PMU_CLK32K_SOC_R	NO_TEST=1
76 36	BI	PMU_INT_L	NO_TEST=1
76	BI	PMU_IREF	NO_TEST=1
75	BI	PMU_LDO3_OUT	NO_TEST=1
75	BI	PMU_VOUT_RTC	NO_TEST=1
75	BI	PMU_VPUMP	NO_TEST=1
76	BI	PMU_VREF	NO_TEST=1
76	BI	PMU_XTAL1	NO_TEST=1
76	BI	PMU_XTAL1_R	NO_TEST=1
76	BI	PMU_XTAL2	NO_TEST=1
155	BI	PM_SLP_S3_L_LED	NO_TEST=1
155	BI	PM_SLP_S3_L_LED_R	NO_TEST=1
155	BI	PM_SLP_S4_L_LED	NO_TEST=1
155	BI	PM_SLP_S4_L_LED_R	NO_TEST=1
155	BI	PM_SLP_S5_L_LED	NO_TEST=1
155	BI	PM_SLP_S5_L_LED_R	NO_TEST=1
156	BI	PM_THRMTRIP_R_L	NO_TEST=1
90	BI	PM_VTT01_EN	NO_TEST=1
91	BI	PM_VTT23_EN	NO_TEST=1
131	BI	PP1V8_DMIC_1_CONN	NO_TEST=1
57	BI	PP3V3_G3H_ENET_EFUSE	NO_TEST=1
110	BI	PPBKLT_BOOST_1	NO_TEST=1
111 110	BI	PPBKLT_BOOST_2	NO_TEST=1
46	BI	PU_CLKREQ_ANALYZER_L	NO_TEST=1
46	BI	PU_CLKREQ_ANA_PCH_L	NO_TEST=1
126 122	BI	PVDDCPUAWAKE_FB_ALT	NO_TEST=1
120	BI	REGBOOTPMVPP	NO_TEST=1
119	BI	REGBOOTPVDDRR	NO_TEST=1

80	BI	REG_1V2_ENET_SKIP	NO_TEST=1
80	BI	REG_2V1_ENET_SKIP	NO_TEST=1
116	BI	REG_BOOT_MVDD_RC	NO_TEST=1
91	BI	REG_BOOT_VPP23_RC	NO_TEST=1
93	BI	REG_BST_CPU_VDDQ23_RC	NO_TEST=1
89	BI	REG_BST_VCCSA_RC	NO_TEST=1
90	BI	REG_BST_VPP01_RC	NO_TEST=1
85	BI	REG_CPUCORE_VRHOT_L	NO_TEST=1
85	BI	REG_CPU_ADDR2	NO_TEST=1
13	BI	REG_CPU_SVID_ALERT_SKL_L	NO_TEST=1
13	BI	REG_CPU_SVID_CLK_SKL	NO_TEST=1
13	BI	REG_CPU_SVID_DATA_SKL	NO_TEST=1
85	BI	REG_CPU_VALRT_L_R	NO_TEST=1
89	BI	REG_CPU_VCCSA_PHSFLT_L	NO_TEST=1
92	BI	REG_CPU_VDDQ01_ADDR2	NO_TEST=1
92	BI	REG_CPU_VDDQ01_ISNS_R	NO_TEST=1
92	BI	REG_CPU_VDDQ01_RC	NO_TEST=1
92	BI	REG_CPU_VDDQ01_SVID_ALERT_R	NO_TEST=1
92	BI	REG_CPU_VDDQ01_SVID_DATA_R	NO_TEST=1
93	BI	REG_CPU_VDDQ23_ADDR2	NO_TEST=1
93	BI	REG_CPU_VDDQ23_IL_R	NO_TEST=1
93	BI	REG_CPU_VDDQ23_PHSFLT_L	NO_TEST=1
93	BI	REG_CPU_VDDQ23_SVID_ALERT_L_R	NO_TEST=1
93	BI	REG_CPU_VDDQ23_SVID_DATA_R	NO_TEST=1
13	BI	REG_CPU_VDDQ_SVID_ALERT_SKL_L	NO_TEST=1
13	BI	REG_CPU_VDDQ_SVID_CLK_SKL	NO_TEST=1
13	BI	REG_CPU_VDDQ_SVID_DATA_SKL	NO_TEST=1
85	BI	REG_CPU_VDIO_R	NO_TEST=1
84	BI	REG_DRVCPU_AVIN	NO_TEST=1
112	BI	REG_GPUCORE_CFILT	NO_TEST=1
163 112	BI	REG_GPUCORE_ISNS_3_R_P	NO_TEST=1
116	BI	REG_MVDD_OCSET_R	NO_TEST=1
116	BI	REG_MVDD_VO_R	NO_TEST=1
118	BI	REG_P0V8_SET1_R	NO_TEST=1
82	BI	REG_P3V3G3H_FB	NO_TEST=1
79	BI	REG_P3V3G3W_FB	NO_TEST=1
79	BI	REG_P3V3G3W_OCSET	NO_TEST=1
113	BI	REG_PHSFLT_GPUCORE_1_L	NO_TEST=1
113	BI	REG_PHSFLT_GPUCORE_2_L	NO_TEST=1
113	BI	REG_PHSFLT_GPUCORE_3_L	NO_TEST=1
114	BI	REG_PHSFLT_GPUCORE_4_L	NO_TEST=1
114	BI	REG_PHSFLT_GPUCORE_5_L	NO_TEST=1
114	BI	REG_PHSFLT_GPUCORE_6_L	NO_TEST=1
115	BI	REG_PHSFLT_GPUCORE_7_L	NO_TEST=1
115	BI	REG_PHSFLT_GPUCORE_8_L	NO_TEST=1
88	BI	REG_PPDRV_CPUVR	NO_TEST=1
116	BI	REG_PVCC_UD450	NO_TEST=1
117	BI	REG_PVCC_UD650	NO_TEST=1
118	BI	REG_PVCC_UD750	NO_TEST=1
90	BI	REG_PVCC_VPP01	NO_TEST=1
91	BI	REG_PVCC_VPP23	NO_TEST=1
90	BI	REG_RS_VPP01	NO_TEST=1
91	BI	REG_RS_VPP23	NO_TEST=1
88	BI	REG_SNUBBER_VCCIO_RC	NO_TEST=1
88	BI	REG_SVID_ALERT_CPU_VCCIO_R	NO_TEST=1
85	BI	REG_SVID_CLK_CPU_R	NO_TEST=1
88	BI	REG_SVID_DATA_CPU_VCCIO_R	NO_TEST=1
92	BI	REG_SVID_VCLK_CPU_VDDQ01_R	NO_TEST=1
93	BI	REG_SVID_VCLK_CPU_VDDQ23_R	NO_TEST=1
88	BI	REG_SVID_VCLK_VCCIO_R	NO_TEST=1
82	BI	REG_VCC1_U8600	NO_TEST=1
88	BI	REG_VCCIO_ADR2	NO_TEST=1
88	BI	REG_VCCIO_BOOST_RC	NO_TEST=1
88	BI	REG_VCCIO_ISNS_R	NO_TEST=1
89	BI	REG_VCCSA_RS1	NO_TEST=1
116	BI	REG_VCC_UD450	NO_TEST=1
117	BI	REG_VCC_UD650	NO_TEST=1
118	BI	REG_VCC_UD750	NO_TEST=1
90	BI	REG_VCC_VPP01	NO_TEST=1
91	BI	REG_VCC_VPP23	NO_TEST=1
117 99	BI	REG_VDDCI_FB_N	NO_TEST=1
117	BI	REG_VDDCI_SET1_R	NO_TEST=1
90	BI	REG_VPP01_ISNS_N	NO_TEST=1
90	BI	REG_VPP01_ISNS_P	NO_TEST=1
91	BI	REG_VPP23_ISNS_N	NO_TEST=1
91	BI	REG_VPP23_ISNS_P	NO_TEST=1
85 15	BI	REG_VSNS_CPU_VCCIN_P	NO_TEST=1
88 14	BI	REG_VSNS_CPU_VCCIO_P	NO_TEST=1

BOM_COST_GROUP=PCB

PAGE TITLE
ICT NO TEST 4

Apple Inc.

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85	14	BI	REG_VSNS_CPU_VCCSA_P	NO_TEST=1	
59	58	BI	SDCONN_CLK	NO_TEST=1	
59	58	BI	SDCONN_CMD	NO_TEST=1	
59	58	BI	SDCONN_D0	NO_TEST=1	
59	58	BI	SDCONN_D1	NO_TEST=1	
	59	BI	SDCONN_R_WP	NO_TEST=1	
	59	BI	SDCONN_UHS2_CLK_P	NO_TEST=1	
59	58	BI	SDCONN_UHS2_D0_N	NO_TEST=1	
59	58	BI	SDCONN_UHS2_D0_P	NO_TEST=1	
59	58	BI	SDCONN_UHS2_D1_N	NO_TEST=1	
59	58	BI	SDCONN_UHS2_D1_P	NO_TEST=1	
	58	BI	SD_SPI_CLK_R	NO_TEST=1	
	58	BI	SD_SPI_CS_L_R	NO_TEST=1	
	58	BI	SD_SPI_HOLD	NO_TEST=1	
	58	BI	SD_SPI_MISO_R	NO_TEST=1	
	58	BI	SD_SPI_MOSI_R	NO_TEST=1	
	51	BI	SEP_DMIC0_DISABLE_R_L	NO_TEST=1	
	131	BI	SEP_DMIC1_DISABLE_R_L	NO_TEST=1	
73	46	BI	SMBUS_PCH_XDP_3V3_SCL	NO_TEST=1	
73	46	BI	SMBUS_PCH_XDP_3V3_SDA	NO_TEST=1	
	126	BI	SOC_AMUXOUT_UFL	NO_TEST=1	
	66	BI	SOC_CLKREQ_PCH_L	NO_TEST=1	
	36	BI	SOC_COLD_RESET_L	NO_TEST=1	
	37	BI	SOC_MIPI0C_REXT	NO_TEST=1	
	37	BI	SOC_MIPI1C_REXT	NO_TEST=1	
	37	BI	SOC_MIPID_REXT	NO_TEST=1	
126	35	BI	SOC_TST_CLKOUT	NO_TEST=1	
	126	BI	SOC_TST_CLKOUT_UFL	NO_TEST=1	
126	76	39	BI	SOC_VDDCPU_SENSE	NO_TEST=1
126	39	BI	SOC_VDDSOC_SENSE	NO_TEST=1	
	35	BI	SOC_XTAL24M_IN	NO_TEST=1	
	35	BI	SOC_XTAL24M_OUT	NO_TEST=1	
	35	BI	SOC_XTAL24M_OUT_R	NO_TEST=1	
	37	BI	SPI_SOCROM_CLK_R	NO_TEST=1	115 114 113
	37	BI	SPI_SOCROM_MOSI_R	NO_TEST=1	
43	37	BI	SPI_TPAD_CLK	NO_TEST=1	
43	37	BI	SPI_TPAD_MISO	NO_TEST=1	
43	37	BI	SPI_TPAD_MOSI	NO_TEST=1	
	134	BI	SR1P2_VLX	NO_TEST=1	
	134	BI	SR1P4_VLX	NO_TEST=1	
	134	BI	SR1P8_VLX	NO_TEST=1	
44	38	BI	SSD0_CLK24M_R	NO_TEST=1	
	61	BI	SSD0_CLKREQ0_R_L	NO_TEST=1	
	61	BI	SSD0_CLKREQ1_R_L	NO_TEST=1	
44	38	BI	SSD1_CLK24M_R	NO_TEST=1	
	62	BI	SSD1_CLKREQ0_R_L	NO_TEST=1	
	62	BI	SSD1_CLKREQ1_R_L	NO_TEST=1	
62	36	BI	SSD1_SWCLK_UART_R2D	NO_TEST=1	
	30	BI	TBT_X_RSENSE	NO_TEST=1	
	98	BI	TXC_100M_N	NO_TEST=1	
	98	BI	TXC_100M_P	NO_TEST=1	
138	37	BI	UART_BT_SOC_D2R	NO_TEST=1	
138	37	BI	UART_BT_SOC_R2D	NO_TEST=1	
	148	BI	UK280_TMP442_SCL	NO_TEST=1	
	148	BI	UK280_TMP442_SDA	NO_TEST=1	
	33	BI	UPC_XA_R_OSC	NO_TEST=1	
33	32	BI	UPC_XA_USB_TOP_P	NO_TEST=1	
	52	BI	USB2_EXTA_N	NO_TEST=1	
	52	BI	USB2_EXTA_P	NO_TEST=1	
	52	BI	USB2_EXTB_N	NO_TEST=1	
	52	BI	USB2_EXTB_P	NO_TEST=1	
	41	BI	PP1V1_SLPDDR_SOC_XTAL_F	NO_TEST=1	

	53	BI	USB2_EXTC_N	NO_TEST=1	
	53	BI	USB2_EXTC_P	NO_TEST=1	
	53	BI	USB2_EXTD_N	NO_TEST=1	
	53	BI	USB2_EXTD_P	NO_TEST=1	
	32	BI	USB_DBG_XA_F_N	NO_TEST=1	
	32	BI	USB_DBG_XA_F_P	NO_TEST=1	
68	32	BI	USB_DBG_XA_N	NO_TEST=1	
68	32	BI	USB_DBG_XA_P	NO_TEST=1	
68	52	BI	USB_EXTA_N	NO_TEST=1	
68	52	BI	USB_EXTA_P	NO_TEST=1	
68	52	BI	USB_EXTB_N	NO_TEST=1	
68	52	BI	USB_EXTB_P	NO_TEST=1	
68	53	BI	USB_EXTC_N	NO_TEST=1	
68	53	BI	USB_EXTC_P	NO_TEST=1	
68	53	BI	USB_EXTD_N	NO_TEST=1	
68	53	BI	USB_EXTD_P	NO_TEST=1	
	58	BI	USB_SD_DM	NO_TEST=1	
	58	BI	USB_SD_DP	NO_TEST=1	
	27	BI	USB_UPC_TA_F_N	NO_TEST=1	
	27	BI	USB_UPC_TA_F_P	NO_TEST=1	
	28	BI	USB_UPC_TB_F_N	NO_TEST=1	
	28	BI	USB_UPC_TB_F_P	NO_TEST=1	
	34	BI	USB_UPC_XB_F_N	NO_TEST=1	
	34	BI	USB_UPC_XB_F_P	NO_TEST=1	
	97	BI	V10_SMBCLK	NO_TEST=1	
	97	BI	V10_SMBDAT	NO_TEST=1	
	134	BI	VDD1P2_C	NO_TEST=1	
	134	BI	VDD1P5_C	NO_TEST=1	
	112	BI	VR_GPU_ADDR_OFFSET	NO_TEST=1	
	112	BI	VR_GPU_IMON_DIGITAL_FILTER	NO_TEST=1	
	112	BI	VR_GPU_IMON_EN	NO_TEST=1	
	112	BI	VR_GPU_IMON_RG	NO_TEST=1	
	112	BI	VR_GPU_IOUT_ALERT_L	NO_TEST=1	
	112	BI	VR_GPU_PHSFLT_L	NO_TEST=1	
	112	BI	VR_GPU_RCSM	NO_TEST=1	
	112	BI	VR_GPU_RCSN_R	NO_TEST=1	
	112	BI	VR_GPU_RCSP	NO_TEST=1	
	112	BI	VR_GPU_RCSP_R	NO_TEST=1	
	112	BI	VR_GPU_SM_ALERT_L	NO_TEST=1	
	112	BI	VR_GPU_SVC_R	NO_TEST=1	
	112	BI	VR_GPU_SVD_R	NO_TEST=1	
	112	BI	VR_GPU_SVT_R	NO_TEST=1	
	112	BI	VR_GPU_SYS_PWROK_L	NO_TEST=1	
	112	BI	VR_GPU_VAUXSENSE	NO_TEST=1	
166	112	BI	VR_GPU_VINSEN	NO_TEST=1	
166	112	BI	VR_GPU_VINSEN	NO_TEST=1	
	112	BI	VR_GPU_VRDY1	NO_TEST=1	
	112	BI	VR_GPU_VRHOT_CRIT_L	NO_TEST=1	
	14	BI	VSENSE_PMAX	NO_TEST=1	
116	99	BI	VSNS_GPU_MVDD_N	NO_TEST=1	
116	99	BI	VSNS_GPU_MVDD_P	NO_TEST=1	
112	99	BI	VSNS_GPU_VDDC_N	NO_TEST=1	
112	99	BI	VSNS_GPU_VDDC_P	NO_TEST=1	
	112	BI	VSNS_GPU_VDDC_P_R	NO_TEST=1	
137	134	BI	WLAN_PMU_TEST_O	NO_TEST=1	
	73	BI	XDP_CPU_PWRBTN_L	NO_TEST=1	
27	26	BI	UPC_TA_DEBUGUART_TX	NO_TEST=1	
27	26	BI	UPC_TA_GPIO1	NO_TEST=1	
27	26	BI	UPC_TA_SWD_CLK	NO_TEST=1	
27	26	BI	UPC_TA_SWD_DATA	NO_TEST=1	
28	26	BI	UPC_TB_DEBUGUART_TX	NO_TEST=1	
28	26	BI	UPC_TB_GPIO1	NO_TEST=1	
33	32	BI	UPC_XA_DEBUGUART_TX	NO_TEST=1	
34	32	BI	UPC_XB_DEBUGUART_TX	NO_TEST=1	
34	32	BI	UPC_XB_GPIO1	NO_TEST=1	

BOM_COST_GROUP=PCB

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30	B7	TBT_X_RBIAS	NO_TEST=1	
30	B7	TBT_X_PCIE_BIAS	NO_TEST=1	
27 23	B7	USBC_TA_USB_TOP_N	NO_TEST=1	
27 23	B7	USBC_TA_USB_TOP_P	NO_TEST=1	
28 23	B7	USBC_TB_USB_BOT_N	NO_TEST=1	
28 23	B7	USBC_TB_USB_BOT_P	NO_TEST=1	
28 23	B7	USBC_TB_USB_TOP_N	NO_TEST=1	
28 23	B7	USBC_TB_USB_TOP_P	NO_TEST=1	
97	B7	CLKTEST_C_N	NO_TEST=1	
97	B7	CLKTEST_C_P	NO_TEST=1	
24	B7	DP_T_SNK_RBIAS	NO_TEST=1	
24	B7	DP_T_SRC_RBIAS	NO_TEST=1	
24	B7	TBT_TA_USB2_RBIAS	NO_TEST=1	
24	B7	TBT_TB_USB2_RBIAS	NO_TEST=1	
26 24	B7	TBT_T_HDMI_DDC_CLK	NO_TEST=1	
26 24	B7	TBT_T_HDMI_DDC_DATA	NO_TEST=1	
24	B7	TBT_T_PCIE_BIAS	NO_TEST=1	
24	B7	TBT_T_RBIAS	NO_TEST=1	
26	B7	TBT_T_XTAL25M_OUT_R	NO_TEST=1	
110 109	B7	LED_RETURN_1_FB	NO_TEST=1	
110 109	B7	LED_RETURN_3_FB	NO_TEST=1	
68 58	B7	USB3_SD_D2R_N	NO_TEST=1	
68 58	B7	USB3_SD_D2R_P	NO_TEST=1	
58	B7	USB3_SD_D2R_C_N	NO_TEST=1	
58	B7	USB3_SD_D2R_C_P	NO_TEST=1	
58	B7	USB3_SD_R2D_N	NO_TEST=1	
58	B7	USB3_SD_R2D_P	NO_TEST=1	
86	B7	REG_PHSFLT_CPUCORE_1_L	NO_TEST=1	
86	B7	REG_PHSFLT_CPUCORE_2_L	NO_TEST=1	
86	B7	REG_PHSFLT_CPUCORE_3_L	NO_TEST=1	
87	B7	REG_PHSFLT_CPUCORE_4_L	NO_TEST=1	
87	B7	REG_PHSFLT_CPUCORE_5_L	NO_TEST=1	
66	B7	WLAN_CLKREQ_PCH_L	NO_TEST=1	
67	B7	PCH_SUSWARN_L	NO_TEST=1	
68	B7	PCH_USB_RBIAS	NO_TEST=1	
70	B7	PP1V0_S5_PCH_VCC_MPHYPCIE3_PLL	NO_TEST=1	
134 68	B7	PCIE_WLAN_R2D_C_N	NO_TEST=1	
134 68	B7	PCIE_WLAN_R2D_C_P	NO_TEST=1	
68	B7	PCIE_RCOMPN	NO_TEST=1	
68	B7	PCIE_RCOMPP	NO_TEST=1	
73	B7	XDP_VR_READY	NO_TEST=1	
32 30	B7	TBT_X_TMU_CLK_OUT	NO_TEST=1	
26 24	B7	TBT_T_TMU_CLK_OUT	NO_TEST=1	
82	B7	P5V_G3S_SNS_N	NO_TEST=1	
116	B7	REG_MVDD_VO	NO_TEST=1	
82	B7	REG_P5VG3S_VOUT	NO_TEST=1	
82	B7	REG_VCC2_U8600	NO_TEST=1	
117	B7	REG_VDDCI_VO	NO_TEST=1	
26	B7	ARKANOID_T_P5	NO_TEST=1	
26	B7	ARKANOID_T_P7	NO_TEST=1	
161 60	B7	FAN_0_TACH_FILT		
134	B7	PCIE_WLAN_R2D_N	NO_TEST=1	
134	B7	PCIE_WLAN_R2D_P	NO_TEST=1	
18 17	B7	MEM_0_SA<0>	NO_TEST=1	
18 17	B7	MEM_0_SA<1>	NO_TEST=1	
18 17	B7	MEM_0_SA<2>	NO_TEST=1	
19 17	B7	MEM_1_SA<0>	NO_TEST=1	
19 17	B7	MEM_1_SA<1>	NO_TEST=1	
19 17	B7	MEM_1_SA<2>	NO_TEST=1	
20 17	B7	MEM_2_SA<0>	NO_TEST=1	
20 17	B7	MEM_2_SA<1>	NO_TEST=1	
20 17	B7	MEM_2_SA<2>	NO_TEST=1	
21 17	B7	MEM_3_SA<0>	NO_TEST=1	
21 17	B7	MEM_3_SA<1>	NO_TEST=1	
21 17	B7	MEM_3_SA<2>	NO_TEST=1	
140 139	B7	ISNS_PP11V_G3H_N	NO_TEST=1	
140 139	B7	ISNS_PP11V_G3H_P	NO_TEST=1	
152 151 149 43 36	B7	GND_SMC_AVSS	NO_TEST=1	
64 38	B7	PCIE_DN2_LIFEBOAT_D2R_P	NO_TEST=1	
64 38	B7	PCIE_DN2_LIFEBOAT_D2R_N	NO_TEST=1	
64 38	B7	PCIE_DN2_LIFEBOAT_R2D_P	NO_TEST=1	
64 38	B7	PCIE_DN2_LIFEBOAT_R2D_N	NO_TEST=1	
64 38	B7	PCIE_DN2_LIFEBOAT_CLK100M_P	NO_TEST=1	
64 38	B7	PCIE_DN2_LIFEBOAT_CLK100M_N	NO_TEST=1	
64 38	B7	PCIE_DN2_LIFEBOAT_CLKREQ_L	NO_TEST=1	
64 38	B7	PCIE_DN2_LIFEBOAT_RESET_L	NO_TEST=1	
38	B7	PCIE_DN2_LIFEBOAT_R2D_C_P	NO_TEST=1	
38	B7	PCIE_DN2_LIFEBOAT_R2D_C_N	NO_TEST=1	

74	B7	PP1V0_PCH_CORE_S5_SW0	NO_TEST=1	
74	B7	PP1V0_PCH_CORE_S5_SW1	NO_TEST=1	
61 38	B7	PCIE_SSD0_D2R_N<1>	NO_TEST=1	
61 38	B7	PCIE_SSD0_D2R_N<2>	NO_TEST=1	
61 38	B7	PCIE_SSD0_D2R_N<3>	NO_TEST=1	
61 38	B7	PCIE_SSD0_D2R_P<1>	NO_TEST=1	
61 38	B7	PCIE_SSD0_D2R_P<2>	NO_TEST=1	
61 38	B7	PCIE_SSD0_D2R_P<3>	NO_TEST=1	
61 38	B7	PCIE_SSD0_R2D_C_N<1>	NO_TEST=1	
61 38	B7	PCIE_SSD0_R2D_C_N<2>	NO_TEST=1	
61 38	B7	PCIE_SSD0_R2D_C_N<3>	NO_TEST=1	
61 38	B7	PCIE_SSD0_R2D_C_P<1>	NO_TEST=1	
61 38	B7	PCIE_SSD0_R2D_C_P<2>	NO_TEST=1	
61 38	B7	PCIE_SSD0_R2D_C_P<3>	NO_TEST=1	
63	B7	PCIE_SSD0_R2D_N<1>	NO_TEST=1	
63	B7	PCIE_SSD0_R2D_N<2>	NO_TEST=1	
63	B7	PCIE_SSD0_R2D_N<3>	NO_TEST=1	
63	B7	PCIE_SSD0_R2D_P<1>	NO_TEST=1	
63	B7	PCIE_SSD0_R2D_P<2>	NO_TEST=1	
63	B7	PCIE_SSD0_R2D_P<3>	NO_TEST=1	
62 38	B7	PCIE_SSD1_D2R_N<1>	NO_TEST=1	
62 38	B7	PCIE_SSD1_D2R_N<2>	NO_TEST=1	
62 38	B7	PCIE_SSD1_D2R_N<3>	NO_TEST=1	
62 38	B7	PCIE_SSD1_D2R_P<1>	NO_TEST=1	
62 38	B7	PCIE_SSD1_D2R_P<2>	NO_TEST=1	
62 38	B7	PCIE_SSD1_D2R_P<3>	NO_TEST=1	
62 38	B7	PCIE_SSD1_R2D_C_N<1>	NO_TEST=1	
62 38	B7	PCIE_SSD1_R2D_C_N<2>	NO_TEST=1	
62 38	B7	PCIE_SSD1_R2D_C_N<3>	NO_TEST=1	
62 38	B7	PCIE_SSD1_R2D_C_P<1>	NO_TEST=1	
62 38	B7	PCIE_SSD1_R2D_C_P<2>	NO_TEST=1	
62 38	B7	PCIE_SSD1_R2D_C_P<3>	NO_TEST=1	
62	B7	PCIE_SSD1_R2D_N<1>	NO_TEST=1	
62	B7	PCIE_SSD1_R2D_N<2>	NO_TEST=1	
62	B7	PCIE_SSD1_R2D_N<3>	NO_TEST=1	
62	B7	PCIE_SSD1_R2D_P<1>	NO_TEST=1	
62	B7	PCIE_SSD1_R2D_P<2>	NO_TEST=1	
62	B7	PCIE_SSD1_R2D_P<3>	NO_TEST=1	
40	B7	PP0V9_SLPDDR_SOC_PCIEREFBUF	NO_TEST=1	
41	B7	PP1V2_AWAKE_SOC_PCIEREFBUF_F	NO_TEST=1	
41	B7	PP1V2_AWAKE_SOC_PLLCPU_F	NO_TEST=1	
41	B7	PP1V2_AWAKE_SOC_PLLSOC_F	NO_TEST=1	
60 36	B7	SMC_FAN_0_PWM	NO_TEST=1	
43	B7	SMC_PECI_TX_R	NO_TEST=1	
36	B7	SPMI_CLK_R	NO_TEST=1	
36	B7	SPMI_DATA_R	NO_TEST=1	
151 76	B7	PMU_CPU_VCCIO_S0_ISENSE	NO_TEST=1	
30	B7	TBT_XA_USB2_RBIAS	NO_TEST=1	
30	B7	TBT_XB_USB2_RBIAS	NO_TEST=1	
68 58	B7	USB3_SD_R2D_C_N	NO_TEST=1	
68 58	B7	USB3_SD_R2D_C_P	NO_TEST=1	
34	B7	PPHV_USBC_XB	NO_TEST=1	
27 23	B7	USBC_TA_USB_BOT_N	NO_TEST=1	
27 23	B7	USBC_TA_USB_BOT_P	NO_TEST=1	
81	B7	REG_0V85_ENET_VO	NO_TEST=1	
59	B7	SDCONN_CLK_F	NO_TEST=1	
79	B7	REG_P5VG3S_USBC_N	NO_TEST=1	
76	B7	NC_PMU_RSLOC_RST_L	NO_TEST=1	
79	B7	REG_BOOT_P3V3G3W_RC	NO_TEST=1	
79	B7	REG_P3V3G3W_DCR_P	NO_TEST=1	
79	B7	REG_P5VG3S_USBC_P	NO_TEST=1	
79	B7	REG_VCC2_U8300	NO_TEST=1	
79	B7	REG_P3V3G3W_DCR_N	NO_TEST=1	
50	B7	PP1V2_SD_SW	NO_TEST=1	
80	B7	REG_SW_1V2_ENET	NO_TEST=1	
80	B7	REG_SW_2V1_ENET	NO_TEST=1	
118	B7	REG_UGATE_P0V8	NO_TEST=1	
89 85	B7	REG_VCCSA_ISNS_N	NO_TEST=1	
89 85	B7	REG_VCCSA_ISNS_P	NO_TEST=1	
134 68	B7	PCIE_WLAN_D2R_P	NO_TEST=1	
134 68	B7	PCIE_WLAN_D2R_N	NO_TEST=1	
92	B7	REG_VSNS_CPU_VDDQ23_N	NO_TEST=1	
13	B7	PCIE_HOT_PLUG_SCL	NO_TEST=1	

11	B7	PCIE_HOT_PLUG_SDA	NO_TEST=1	
82	B7	REG_PHASE_P5VG3S_TGR	NO_TEST=1	
38	B7	PCIE_DN_CLKREQ1_L	NO_TEST=1	
149	B7	ISNS_P12V_MAIN_SSD0_N	NO_TEST=1	
149	B7	ISNS_P12V_MAIN_SSD0_P	NO_TEST=1	
149	B7	ISNS_P12V_MAIN_SSD1_N	NO_TEST=1	
149	B7	ISNS_P12V_MAIN_SSD1_P	NO_TEST=1	
84	B7	REG_DRVCPU_PH	NO_TEST=1	
149 85	B7	ISNS_HS_CPU_VCORE_N	NO_TEST=1	
149 85	B7	ISNS_HS_CPU_VCORE_P	NO_TEST=1	
150 82	B7	ISNS_USBA_5V_G3S_N	NO_TEST=1	
150 82	B7	ISNS_USBA_5V_G3S_P	NO_TEST=1	
150 79	B7	ISNS_USBC_5V_G3S_N	NO_TEST=1	
150 79	B7	ISNS_USBC_5V_G3S_P	NO_TEST=1	
121 66	B7	PCIE_CLK100M_ANALYZER_N	NO_TEST=1	
121 66	B7	PCIE_CLK100M_ANALYZER_P	NO_TEST=1	
73 68	B7	XDP_OBSFN_C_0	NO_TEST=1	
73	B7	XDP_OBSFN_C_1	NO_TEST=1	
149 139	B7	ISNS_P12V_GPU_N	NO_TEST=1	
149 139	B7	ISNS_P12V_GPU_P	NO_TEST=1	
149 139	B7	ISNS_P12V_MAIN_AUX_GPU_N	NO_TEST=1	
149 139	B7	ISNS_P12V_MAIN_AUX_GPU_P	NO_TEST=1	
149 139	B7	ISNS_P12V_MAIN_BLC_LCD_N	NO_TEST=1	
149 139	B7	ISNS_P12V_MAIN_BLC_LCD_P	NO_TEST=1	
149 139	B7	ISNS_P12V_MAIN_N	NO_TEST=1	
149 139	B7	ISNS_P12V_MAIN_P	NO_TEST=1	
150	B7	ISNS_P3V3_G3W_SSD0_N	NO_TEST=1	
150	B7	ISNS_P3V3_G3W_SSD0_P	NO_TEST=1	
150	B7	ISNS_P3V3_G3W_SSD1_N	NO_TEST=1	
150	B7	ISNS_P3V3_G3W_SSD1_P	NO_TEST=1	
92	B7	REG_VSNS_CPU_VDDQ01_P	NO_TEST=1	
93	B7	REG_VSNS_CPU_VDDQ23_P	NO_TEST=1	
73 67	B7	XDP_PCH_PRDY_L	NO_TEST=1	
73 67	B7	XDP_PCH_PREQ_L	NO_TEST=1	
85	B7	REG_VCCIN_TSNS_A_R	NO_TEST=1	
85	B7	REG_VCCSA_TSNS_B_R	NO_TEST=1	
73 68	B7	XDP_OBSDATA_A_0	NO_TEST=1	
73 68	B7	XDP_OBSDATA_A_1	NO_TEST=1	
73 67	B7	XDP_OBSDATA_A_2	NO_TEST=1	
73 68	B7	XDP_OBSDATA_A_3	NO_TEST=1	
73 68	B7	XDP_OBSDATA_B_0	NO_TEST=1	
73 68	B7	XDP_OBSDATA_B_1	NO_TEST=1	
73 67	B7	XDP_OBSDATA_B_2	NO_TEST=1	
73 68	B7	XDP_OBSDATA_B_3	NO_TEST=1	
73	B7	XDP_OBSDATA_C_0	NO_TEST=1	
73	B7	XDP_OBSDATA_C_1	NO_TEST=1	
73	B7	XDP_OBSDATA_C_2	NO_TEST=1	
73	B7	XDP_OBSDATA_C_3	NO_TEST=1	
73 68	B7	XDP_OBSDATA_D_0	NO_TEST=1	
73 68	B7	XDP_OBSDATA_D_1	NO_TEST=1	
73 68	B7	XDP_OBSDATA_D_2	NO_TEST=1	
73 68	B7	XDP_OBSDATA_D_3	NO_TEST=1	
73	B7	XDP_PCH_TCK_CON	NO_TEST=1	
73	B7	XDP_PIN2	NO_TEST=1	
134	B7	PCIE_WLAN_D2R_C_N	NO_TEST=1	
134	B7	PCIE_WLAN_D2R_C_P	NO_TEST=1	
72	B7	PCH_GPD_0_FET_L	NO_TEST=1	
72	B7	XDP_CPU_PWR_DEBUG_FET_L	NO_TEST=1	
49	B7	IOX_RESET_MASK_L	NO_TEST=1	
49	B7	P1V8S0_VALID_IOX	NO_TEST=1	
57	B7	ENETCONN_MCT_BS	NO_TEST=1	
69	B7	PCH_STRP_SPIROM_SAF	NO_TEST=1	
69	B7	CLK100M_CPU_BCLK_0_P	NO_TEST=1	
69	B7	CLK100M_CPU_BCLK_0_N	NO_TEST=1	
69	B7	CLK100M_CPU_BCLK_1_P	NO_TEST=1	
69	B7	CLK100M_CPU_BCLK_1_N	NO_TEST=1	
69	B7	CLK100M_CPU_BCLK_2_P	NO_TEST=1	
69	B7	CLK100M_CPU_BCLK_2_N	NO_TEST=1	

32 30	B8	DP_X_SNK0_DDC_CLK	NO_TEST=1	
32 30	B8	DP_X_SNK0_DDC_DATA	NO_TEST=1	
32 30	B8	DP_X_SNK1_DDC_CLK	NO_TEST=1	
32 30	B8	DP_X_SNK1_DDC_DATA	NO_TEST=1	
30	B8	DP_X_SRC_RBIAS	NO_TEST=1	
32 31	B8	PP0V9_TBT_X_CIO	NO_TEST=1	
31	B8	PP0V9_TBT_X_DP	NO_TEST=1	
32 31	B8	PP0V9_TBT_X_USB	NO_TEST=1	
34 30	B8	TBT_XB_LSRX	NO_TEST=1	
34 30	B8	TBT_XB_LSTX	NO_TEST=1	
32 30	B8	TBT_X_HDMI_DDC_CLK	NO_TEST=1	
32 30	B8	TBT_X_HDMI_DDC_DATA	NO_TEST=1	
30	B8	TBT_X_THERM_D_POS	NO_TEST=1	
56 55	B8	ENET_TSENS_E_P	NO_TEST=1	
44 35	B8	SEP_DISABLE_STROBE	NO_TEST=1	
131 51 44	B8	SEP_DMIC_DISABLE_Q_L	NO_TEST=1	
36	B8	NC_DFR_TOUCH_INT_L	NO_TEST=1	
56	B8	NC_Q6080_S	NO_TEST=1	
56	B8	NC_Q6080_G	NO_TEST=1	
56	B8	NC_Q6080_D	NO_TEST=1	
134	B8	NC_SECI_OUT_D2R	NO_TEST=1	
134	B8	NC_SECI_IN_R2D	NO_TEST=1	
44 37	B8	I2S_SPKRAMP_L_LRCLK_R	NO_TEST=1	
44 37	B8	I2S_SPKRAMP_R_LRCLK_R	NO_TEST=1	
44 37	B8	I2S_CODEC_LRCLK_R	NO_TEST=1	
37	B8	NC_I2S_HAWKING_BCLK_R	NO_TEST=1	
39	B8	NC_SOC_VSSSOC_SENSE	NO_TEST=1	
39	B8	NC_SOC_VSSCPU_SENSE	NO_TEST=1	
36	B8	NC_SOC_AOP_PDM_CLK4	NO_TEST=1	
76	B8	NC_SE_PWR_EN	NO_TEST=1	
76	B8	NC_PMU_CLK32K_GNSS	NO_TEST=1	
76	B8	NC_PMU_CLK32K	NO_TEST=1	
76	B8	NC_PMU_AMUX_BY	NO_TEST=1	
76	B8	NC_PEARL_PWR_EN	NO_TEST=1	
36	B8	NC_LIDINT_L_UARTHDD_D2R	NO_TEST=1	
36	B8	NC_GNSS_HOST_WAKE	NO_TEST=1	
74	B8	NC_BUCK8_SW1	NO_TEST=1	
74	B8	NC_BUCK4_SW1	NO_TEST=1	
36	B8	NC_ALTIMETER_INT	NO_TEST=1	
158 45 36	B8	CPU_SMC_THRMTRIP_L	NO_TEST=1	
158 36	B8	MESA_MENUKEY_L	NO_TEST=1	
158 36	B8	ENET_LOW_PWR	NO_TEST=1	
158 37	B8	DFR_DISP_RESET_L	NO_TEST=1	
158 35	B8	MESA_INT	NO_TEST=1	
158 37	B8	I2S_CODEC1_R2D_R	NO_TEST=1	
32 30	B8	TBT_X_XTAL25M_OUT	NO_TEST=1	
35	B8	SOC_DDR0_ZQ	NO_TEST=1	
121 36	B8	SWD_SOC_SWCLK	NO_TEST=1	
121 36	B8	SWD_SOC_SWDIO	NO_TEST=1	
13	B8	KBLX_PM_DOWN	NO_TEST=1	
162 44 38	B8	PCIE_SOC_R2D_P<3..0>	NO_TEST=1	
162 44 38	B8	PCIE_SOC_R2D_N<3..0>	NO_TEST=1	
158 68 38	B8	PCIE_SOC_D2R_P<2>	NO_TEST=1	
158 68 38	B8	PCIE_SOC_D2R_P<1>	NO_TEST=1	
32	B8	USB3_DM2_D2RP	NO_TEST=1	
32	B8	USB3_DM2_D2RN	NO_TEST=1	
32	B8	USB3_DM2_R2DP	NO_TEST=1	
32	B8	USB3_DM2_R2DN	NO_TEST=1	
56	B8	OSC_1588_50MHZ_P	NO_TEST=1	
56	B8	OSC_1588_50MHZ_N	NO_TEST=1	
56 54	B8	ENET_OSC_1588_50MHZ_P	NO_TEST=1	
56 54	B8	ENET_OSC_1588_50MHZ_N	NO_TEST=1	
82	B8	REG_UGATE_P3V3G3H_R	NO_TEST=1	
82	B8	REG_UGATE_P5VG3S_R	NO_TEST=1	
79	B8	REG_UGATE_P5VG3S_USBC_R	NO_TEST=1	
56	B8	ENET_OSC_REFCLK_50MHZ_N	NO_TEST=1	
56	B8	ENET_OSC_REFCLK_50MHZ_P	NO_TEST=1	
56 54	B8	ENET_REFCLK_50MHZ_N	NO_TEST=1	
56 54	B8	ENET_REFCLK_50MHZ_P	NO_TEST=1	
56	B8	OSC_REFCLK_OE	NO_TEST=1	
56	B8	PP3V3_G3H_ENET_REFCLK	NO_TEST=1	

BOM_COST_GROUP=PCB

PAGE TITLE
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CAPS FOR DESENSE MITIGATION

CPU CORE VR

PPVCCIN_S0

CP003 12PF 5% 25V NP0-C0G 0201	CP004 12PF 5% 25V NP0-C0G 0201	CP005 12PF 5% 25V NP0-C0G 0201	CP006 12PF 5% 25V NP0-C0G 0201	CP007 12PF 5% 25V NP0-C0G 0201	CP008 12PF 5% 25V NP0-C0G 0201	CP009 12PF 5% 25V NP0-C0G 0201	CP019 12PF 5% 25V NP0-C0G 0201
CP011 12PF 5% 25V NP0-C0G 0201	CP012 12PF 5% 25V NP0-C0G 0201	CP013 12PF 5% 25V NP0-C0G 0201	CP014 12PF 5% 25V NP0-C0G 0201	CP015 12PF 5% 25V NP0-C0G 0201	CP016 12PF 5% 25V NP0-C0G 0201	CP017 12PF 5% 25V NP0-C0G 0201	CP018 12PF 5% 25V NP0-C0G 0201
CP020 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP021 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP022 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP023 3.0PF +/-0.1PF 25V NP0-C0G 0201				

CPU VDDQ 01 VR

PPVDDQ01_S3

CP030 12PF 5% 25V NP0-C0G 0201	CP031 12PF 5% 25V NP0-C0G 0201	CP032 12PF 5% 25V NP0-C0G 0201	CP033 12PF 5% 25V NP0-C0G 0201	CP034 12PF 5% 25V NP0-C0G 0201	CP035 12PF 5% 25V NP0-C0G 0201	CP036 12PF 5% 25V NP0-C0G 0201
CP040 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP041 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP042 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP043 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP044 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP045 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP046 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VDDQ 23 VR

PPVDDQ23_S3

CP050 12PF 5% 25V NP0-C0G 0201	CP051 12PF 5% 25V NP0-C0G 0201	CP052 12PF 5% 25V NP0-C0G 0201	CP053 12PF 5% 25V NP0-C0G 0201	CP054 12PF 5% 25V NP0-C0G 0201	CP055 12PF 5% 25V NP0-C0G 0201	CP056 12PF 5% 25V NP0-C0G 0201
CP060 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP061 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP062 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP063 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP064 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP065 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP066 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VCCSA VR

PPVCCSA_S0

CP0F0 12PF 5% 25V NP0-C0G 0201	CP0F1 12PF 5% 25V NP0-C0G 0201	CP0F2 12PF 5% 25V NP0-C0G 0201	CP0F3 12PF 5% 25V NP0-C0G 0201
CP0G0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0G1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0G2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0G3 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VCCIO VR

PPVCCIO_S0

CP0H0 12PF 5% 25V NP0-C0G 0201	CP0H1 12PF 5% 25V NP0-C0G 0201	CP0H2 12PF 5% 25V NP0-C0G 0201	CP0H3 12PF 5% 25V NP0-C0G 0201
CP0J0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0J1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0J2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0J3 3.0PF +/-0.1PF 25V NP0-C0G 0201

DIMM CH 0

PPVDDQ01_S3

CP070 12PF 5% 25V NP0-C0G 0201	CP071 12PF 5% 25V NP0-C0G 0201	CP072 12PF 5% 25V NP0-C0G 0201	CP073 12PF 5% 25V NP0-C0G 0201
CP080 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP081 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP082 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP083 3.0PF +/-0.1PF 25V NP0-C0G 0201

DIMM CH 1

PPVDDQ01_S3

CP090 12PF 5% 25V NP0-C0G 0201	CP091 12PF 5% 25V NP0-C0G 0201	CP092 12PF 5% 25V NP0-C0G 0201	CP093 12PF 5% 25V NP0-C0G 0201
CP0A0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0A1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0A2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0A3 3.0PF +/-0.1PF 25V NP0-C0G 0201

DIMM CH 2

PPVDDQ23_S3

CP0B0 12PF 5% 25V NP0-C0G 0201	CP0B1 12PF 5% 25V NP0-C0G 0201	CP0B2 12PF 5% 25V NP0-C0G 0201	CP0B3 12PF 5% 25V NP0-C0G 0201
CP0C0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0C1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0C2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0C3 3.0PF +/-0.1PF 25V NP0-C0G 0201

DIMM CH 3

PPVDDQ23_S3

CP0D0 12PF 5% 25V NP0-C0G 0201	CP0D1 12PF 5% 25V NP0-C0G 0201	CP0D2 12PF 5% 25V NP0-C0G 0201	CP0D3 12PF 5% 25V NP0-C0G 0201
CP0E0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0E1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0E2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0E3 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VPP 01 VR

PPVPP01_S3

CP0K0 12PF 5% 25V NP0-C0G 0201	CP0K1 12PF 5% 25V NP0-C0G 0201	CP0K2 12PF 5% 25V NP0-C0G 0201	CP0K3 12PF 5% 25V NP0-C0G 0201
CP0L0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0L1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0L2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0L3 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VPP 23 VR

PPVPP23_S3

CP0M0 12PF 5% 25V NP0-C0G 0201	CP0M1 12PF 5% 25V NP0-C0G 0201	CP0M2 12PF 5% 25V NP0-C0G 0201	CP0M3 12PF 5% 25V NP0-C0G 0201
CP0N0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0N1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0N2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP0N3 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=DESENSE

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CAPS FOR DESENSE MITIGATION

CPU VDDQ 01 12V INPUT

169 93 92 91 90 PP12VR11V_MAIN_FLT

CP170 12PF 5% 25V NP0-C0G 0201	CP171 12PF 5% 25V NP0-C0G 0201	CP172 12PF 5% 25V NP0-C0G 0201	CP173 12PF 5% 25V NP0-C0G 0201
CP180 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP181 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP182 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP183 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VDDQ 23 12V INPUT

169 93 92 91 90 PP12VR11V_MAIN_FLT

CP190 12PF 5% 25V NP0-C0G 0201	CP191 12PF 5% 25V NP0-C0G 0201	CP192 12PF 5% 25V NP0-C0G 0201	CP193 12PF 5% 25V NP0-C0G 0201
CP1A0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1A1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1A2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1A3 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VPP 01 12V INPUT

169 93 92 91 90 PP12VR11V_MAIN_FLT

CP1B0 12PF 5% 25V NP0-C0G 0201	CP1B1 12PF 5% 25V NP0-C0G 0201	CP1B2 12PF 5% 25V NP0-C0G 0201	CP1B3 12PF 5% 25V NP0-C0G 0201
CP1C0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1C1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1C2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1C3 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VPP 23 12V INPUT

169 93 92 91 90 PP12VR11V_MAIN_FLT

CP1D0 12PF 5% 25V NP0-C0G 0201	CP1D1 12PF 5% 25V NP0-C0G 0201	CP1D2 12PF 5% 25V NP0-C0G 0201	CP1D3 12PF 5% 25V NP0-C0G 0201
CP1E0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1E1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1E2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1E3 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU CORE, VSA 12V INPUT

89 87 86 85 84 PP12V_S0_CPUCORE_FLT

CP1K0 12PF 5% 25V NP0-C0G 0201	CP1K1 12PF 5% 25V NP0-C0G 0201	CP1K2 12PF 5% 25V NP0-C0G 0201	CP1K3 12PF 5% 25V NP0-C0G 0201	CP1K4 12PF 5% 25V NP0-C0G 0201	CP1K5 12PF 5% 25V NP0-C0G 0201	CP1K6 12PF 5% 25V NP0-C0G 0201	CP1K7 12PF 5% 25V NP0-C0G 0201	CP1K8 12PF 5% 25V NP0-C0G 0201	CP1K9 12PF 5% 25V NP0-C0G 0201	CP1L4 12PF 5% 25V NP0-C0G 0201	CP1L5 12PF 5% 25V NP0-C0G 0201
CP1L0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1L1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1L2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1L3 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1L6 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1L7 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1L8 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1L9 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1T0 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1T1 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1T2 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP1T3 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VCCIO 12V INPUT

88 PP12V_MAIN_FLT_VCCIO

CP100 12PF 5% 25V NP0-C0G 0201	CP101 12PF 5% 25V NP0-C0G 0201	CP102 12PF 5% 25V NP0-C0G 0201	CP103 12PF 5% 25V NP0-C0G 0201
CP110 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP111 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP112 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP113 3.0PF +/-0.1PF 25V NP0-C0G 0201

CPU VTT 01 3V3 G3S

90 PP3V3_G3S_VTT01

CP120 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP121 12PF 5% 25V NP0-C0G 0201

CPU VTT 23 3V3 G3S

91 PP3V3_G3S_VTT23

CP130 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP131 12PF 5% 25V NP0-C0G 0201

CAMERA 3V3 G3S

127 93 92 91 90 85 81 80 78 75 59 51 13 159 154 144 142 138 137 124 120 PP3V3_G3S

CP140 12PF 5% 25V NP0-C0G 0201	CP141 12PF 5% 25V NP0-C0G 0201
CP142 3.0PF +/-0.1PF 25V NP0-C0G 0201	CP143 3.0PF +/-0.1PF 25V NP0-C0G 0201

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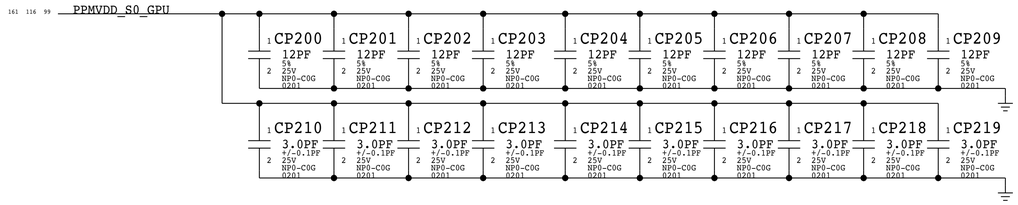
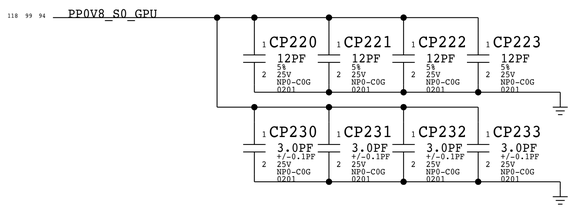
CAPS FOR DESENSE MITIGATION

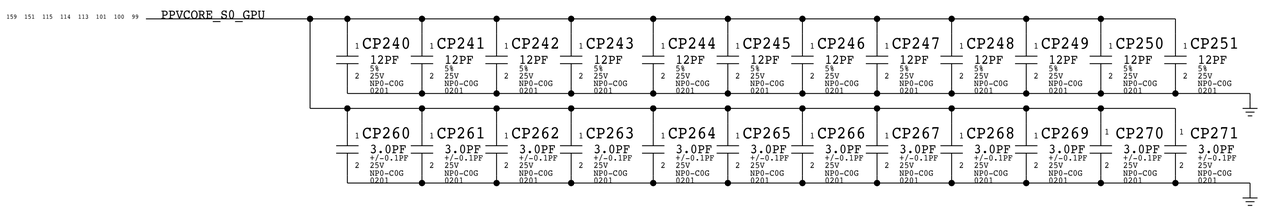
GPU MEMORY



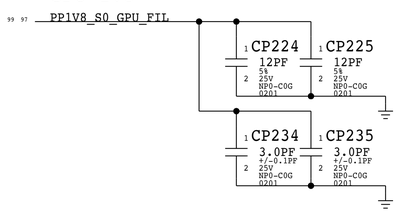
GPU 0V8



GPU CORE



GPU 1V8



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PPDDRVTT01 ISL1 STITCHING CAPS

171 161 90 22 19 18 PPDDRVTT01_S0

CP500	CP501	CP502	CP503	CP504	CP505	CP506
1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201

PPDDRVTT01 ISL14 STITCHING CAPS

171 161 90 22 19 18 PPDDRVTT01_S0

CP510	CP511	CP512	CP513	CP514	CP515	CP516
1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201

PPDDRVTT23 ISL1 STITCHING CAPS

171 161 91 22 21 20 PPDDRVTT23_S0

CP520	CP521	NOSTUFF CP522	CP523	CP524	CP525	CP526
1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201

PPDDRVTT23 ISL14 STITCHING CAPS

171 161 91 22 21 20 PPDDRVTT23_S0

CP530	CP531	CP532	CP533	CP534	CP535	CP536
1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201	1UF 20% 6.3V X6S-CERM 0201

PPBKLT_BOOST CAPS

161 110 109 PPBKLT_BOOST

CP540	CP541
1000PF 10% 100V X7R-CERM 0603	1000PF 10% 100V X7R-CERM 0603

CPU SPRINGS

1.5X2MM PAD, SPRING INCLUDED (870-3024)

SPP575 SPRING-PSE-2E030X031 CLIP-SM	NOSTUFF
SPP576 SPRING-PSE-2E030X031 CLIP-SM	NOSTUFF
SPP577 SPRING-PSE-2E030X031 CLIP-SM	
SPP578 SPRING-PSE-2E030X031 CLIP-SM	
SPP579 SPRING-PSE-2E030X031 CLIP-SM	
SPP580 SPRING-PSE-2E030X031 CLIP-SM	NOSTUFF
SPP581 SPRING-PSE-2E030X031 CLIP-SM	NOSTUFF
SPP582 SPRING-PSE-2E030X031 CLIP-SM	NOSTUFF
SPP583 SPRING-PSE-2E030X031 CLIP-SM	NOSTUFF
SPP584 SPRING-PSE-2E030X031 CLIP-SM	

GPU SPRINGS

2.5X1.2MM PAD, SPRING INCLUDED (870-1415)

SPP585 EMI-SPRING TNM-0008A	
SPP586 EMI-SPRING TNM-0008A	
SPP587 EMI-SPRING TNM-0008A	
SPP588 EMI-SPRING TNM-0008A	
SPP589 EMI-SPRING TNM-0008A	NOSTUFF
SPP590 EMI-SPRING TNM-0008A	NOSTUFF
SPP591 EMI-SPRING TNM-0008A	
SPP592 EMI-SPRING TNM-0008A	
SPP593 EMI-SPRING TNM-0008A	
SPP594 EMI-SPRING TNM-0008A	NOSTUFF
SPP595 EMI-SPRING TNM-0008A	
SPP596 EMI-SPRING TNM-0008A	NOSTUFF

BOM_COST_GROUP=EMC

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