Analog to Digital (A / D) Converters

Topics

- A / D Process
- Signal Conditioning
- Type of A / D Converters
- Errors in A / D Converters
- Aliasing

Course Goals

- We use A / D converters in the laboratory as a general purpose instrument for measuring analog signals (the mixed signal oscilloscope is a digital instrument)

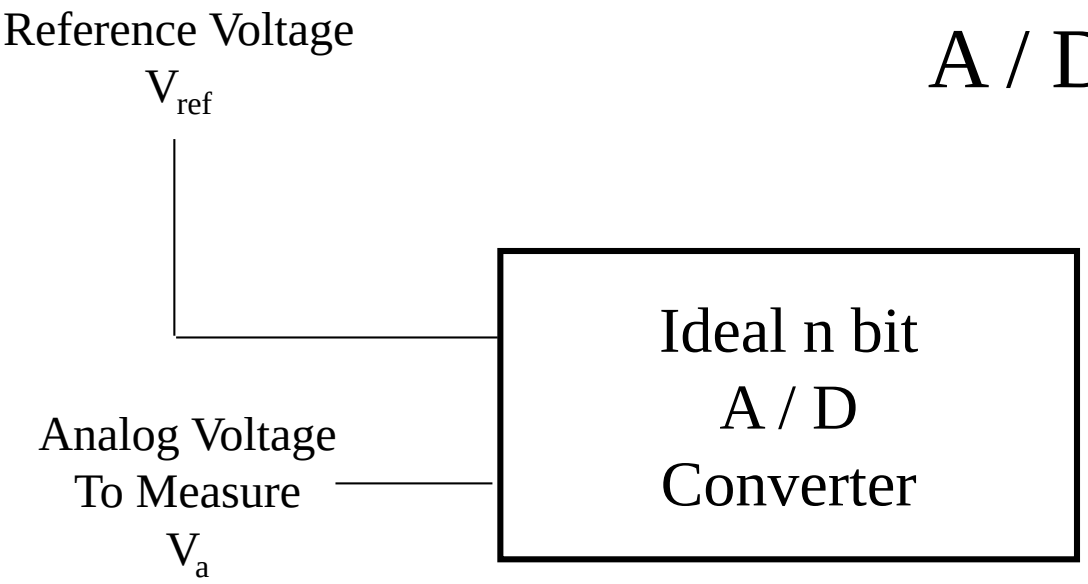
- We use an A / D converter as the primary mechanism for bringing analog signals into a microcomputer for digital signal processing and control purposes
  - In previous case study, we have used an A / D converter to measure the analog voltage from a potentiometer.
  - In the DC motor case study, an A / D converter will measure the analog velocity of the motor using a tachometer.

A / D Converter Process

An Analog to Digital converter (A / D) accepts an analog (continuous in time) electrical signal (a voltage or a current) and converts it to a digital value by:

- Sampling the signal in time
- Quantizing the signal in amplitude

A / D Code

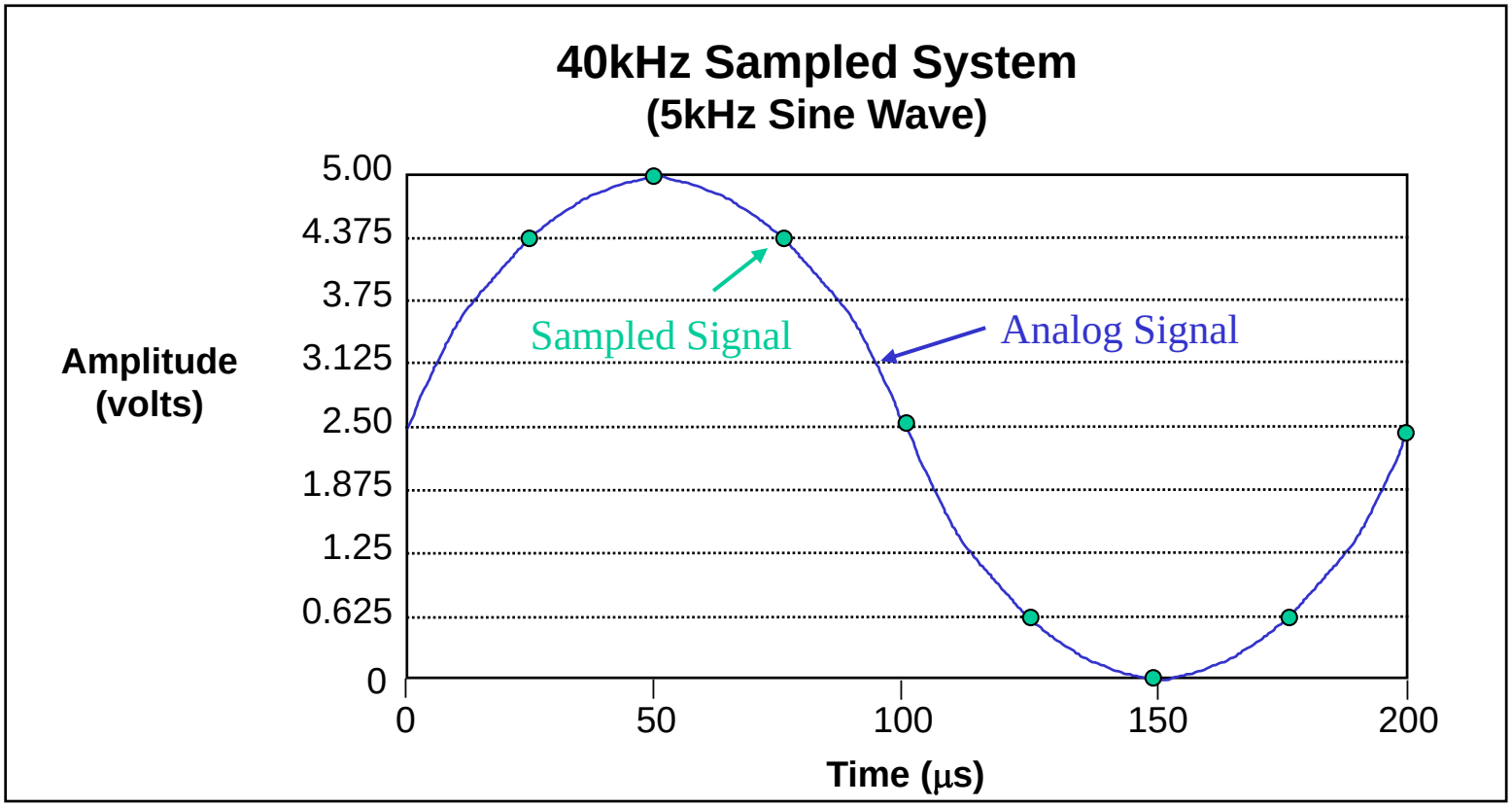


$$\text{Digital Code} = \left(2^n - 1\right)\frac{V_a}{V_{ref}}$$

$$\text{Digital Code (10 bits)} = 1023\ \frac{V_a}{V_{ref}}$$

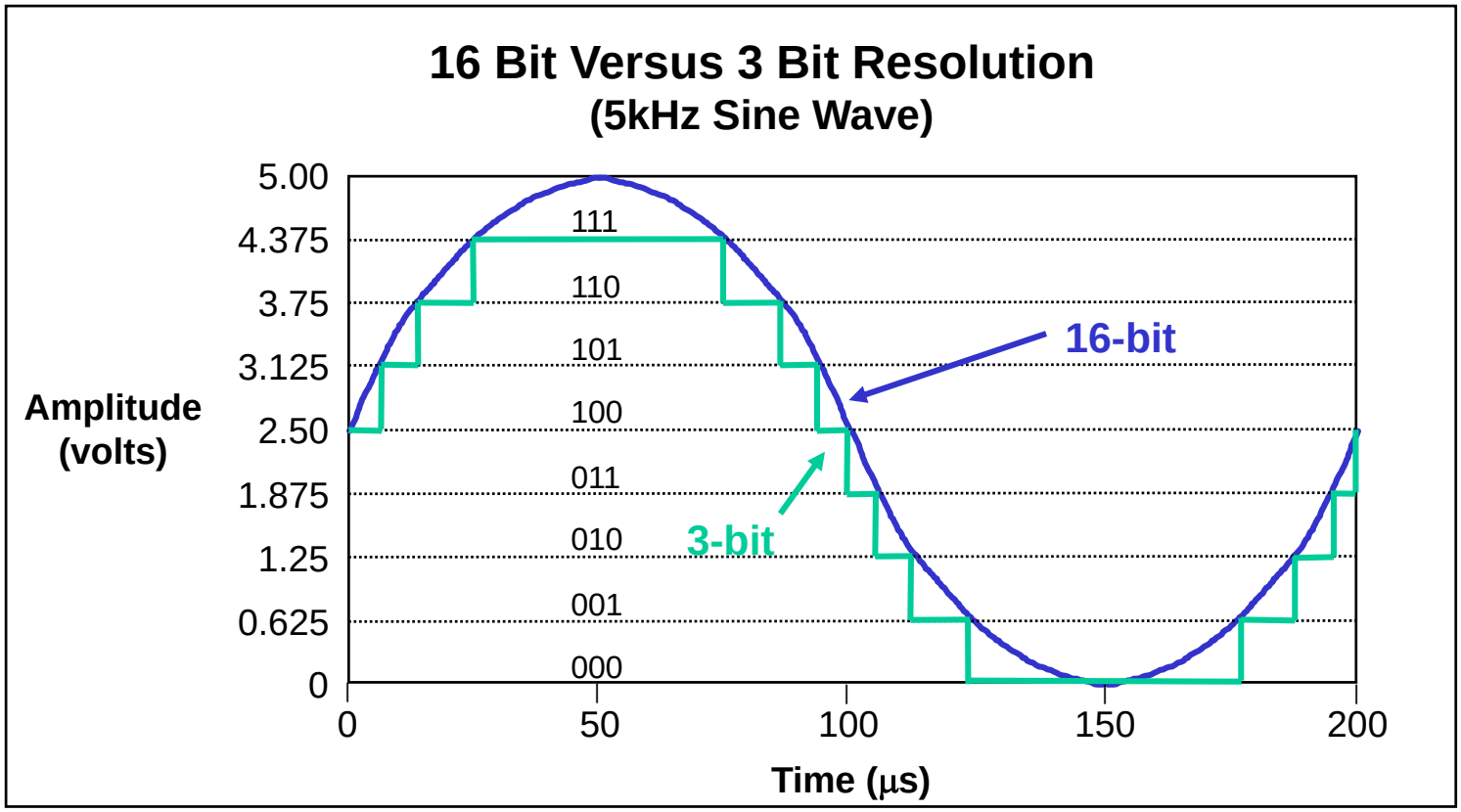
$$\text{Digital Code (8 bits)} = 255\ \frac{V_a}{V_{ref}}$$

Sampling in Time



As sampling frequency increases, the digital signal better approximates the analog signal.

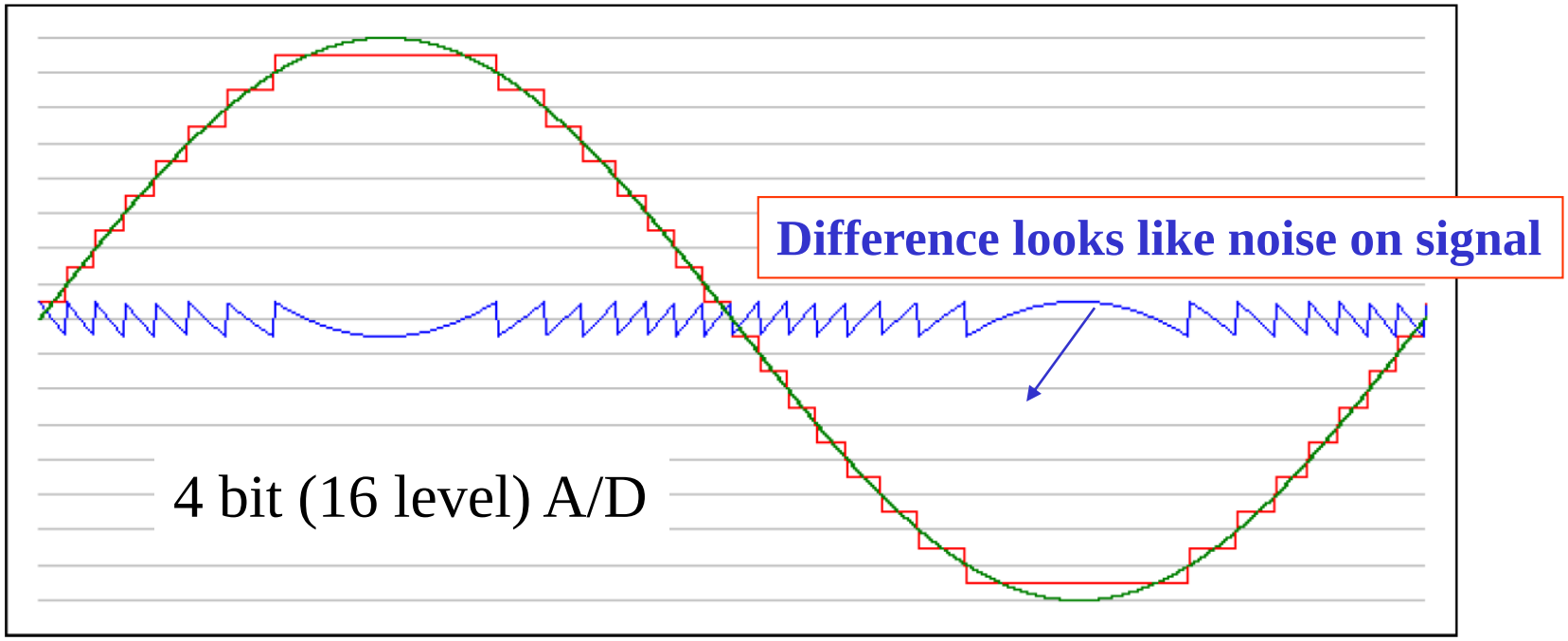
Quantization in Amplitude



As resolution increases, the digital signal better approximates the analog signal.

The maximum quantization error is ½ the increment size.

Quantization Noise

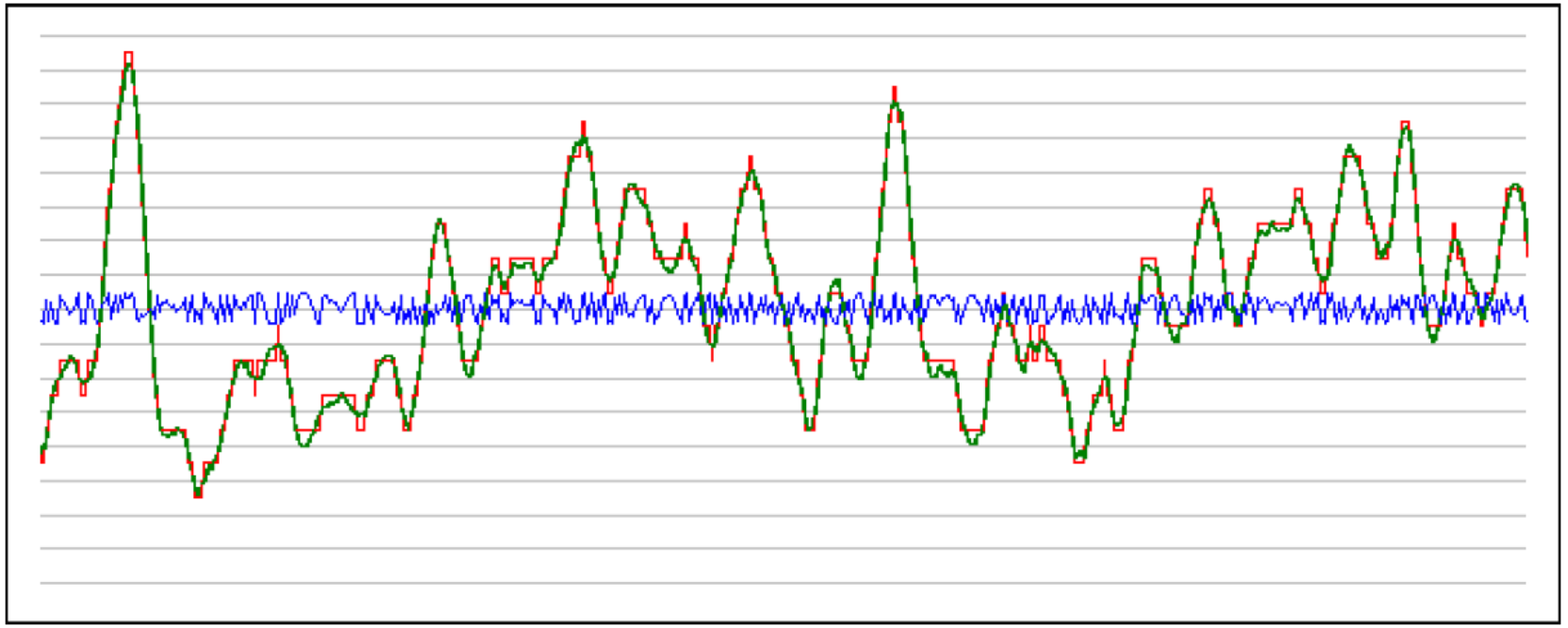


If you assume that the noise is uniformly distributed & uncorrelated with the signal then the rms (root mean square) value of the noise is

$$\frac{1}{\sqrt{12}}\ \text{LSB}$$

(that is, the standard deviation of the uniform distribution)

Quantization Noise 16 bit Converter



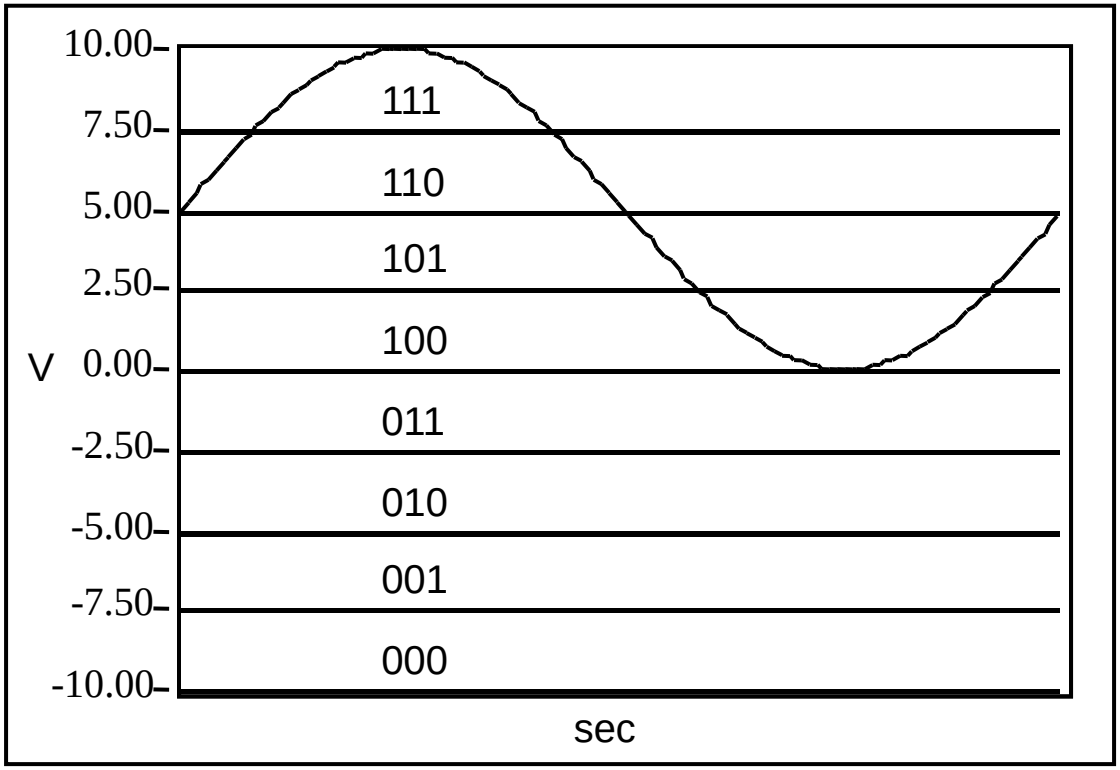
Green – analog signal
Red – sampled A / D output
Blue – noise (difference)

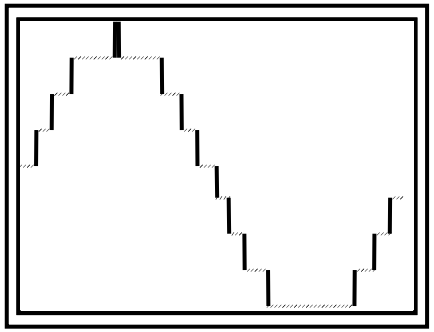
Digital Signals

Digital signals are **both** sampled in time and quantized in amplitude.

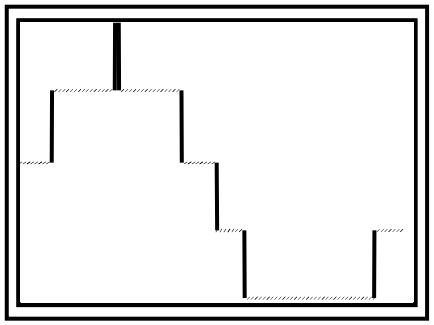
- Sampling in Time Issues
  - Uniform vs. Non-Uniform sampling
  - Sampling frequency
  - Sample time accuracy
- Quantization in amplitude issues
  - Resolution
  - Conversion time
  - Conversion method

The optimal resolution depends on the range of signal being measured.





Range = 0 V to 10 V

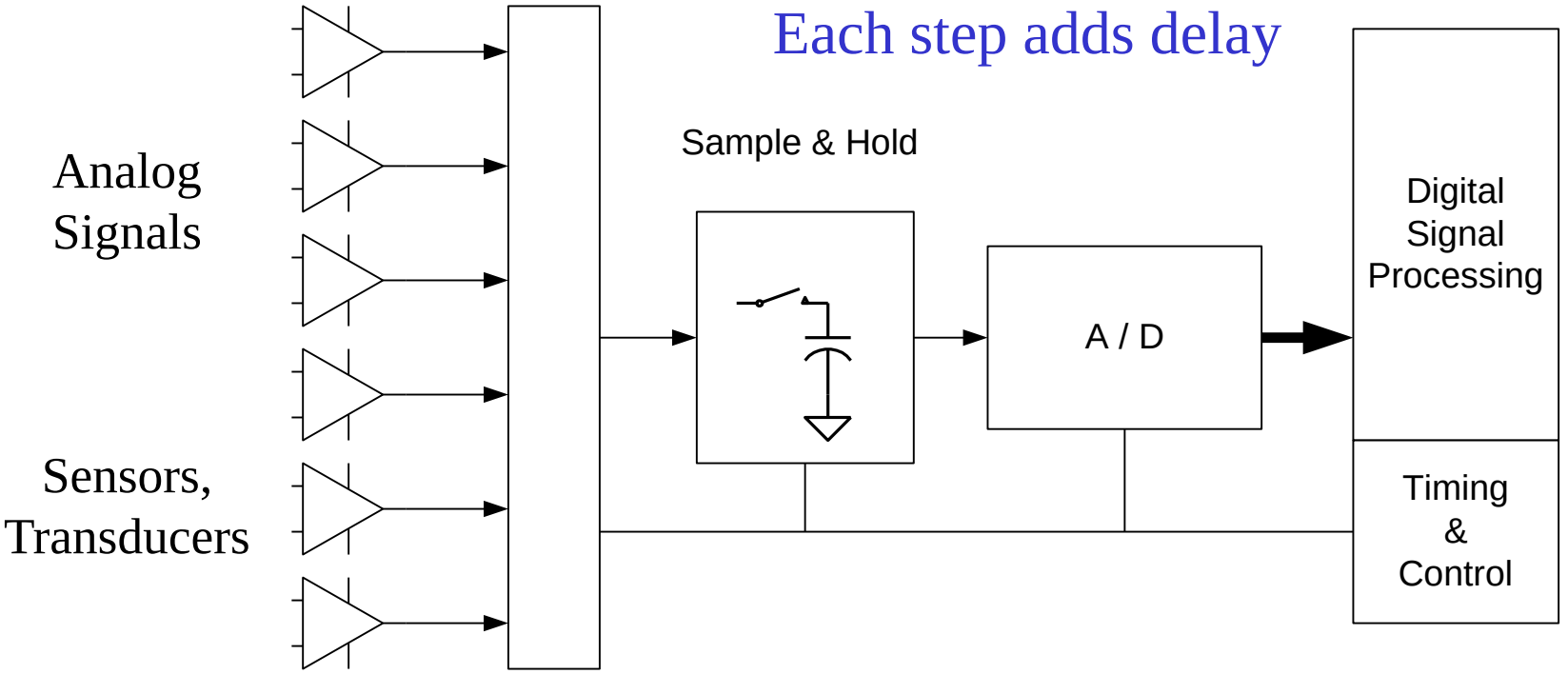


Range = -10 V to +10 V

For Instruments & DAQ boards, the A / D determines the resolution. In Microcontrollers, it may be determined by the data word size but can be different (MicroChip has parts with 10 or 12 bit A/D and an 8 bit word).

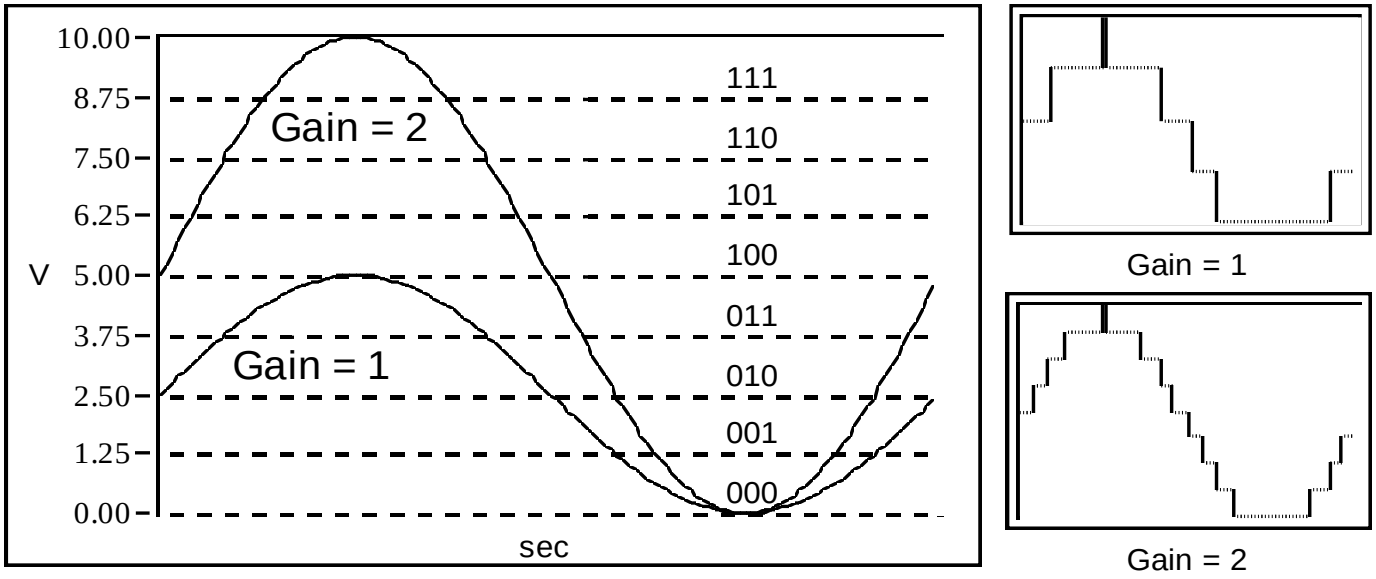
Analog World

Digital World



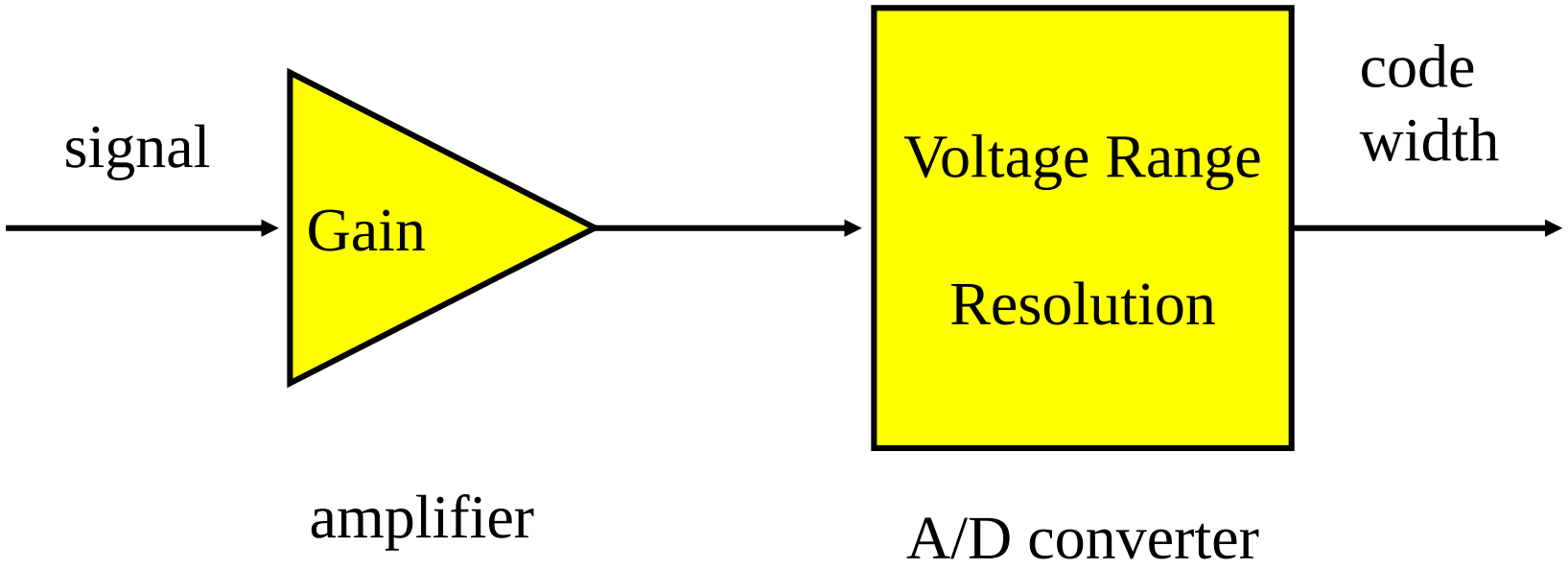
Acquisition time is the time required to charge & discharge the holding capacitor. It depends on the internal impedance of the multiplexor & the output impedance of the analog source.

Amplification (or attenuation) sets the range of the analog signal.



From a design perspective, you want to set the analog range to coincide with the range of the A / D.
Too small -> limited detectable range.
Too large -> clipping.

Code Width Determination



How much does the signal have to change to produce a 1 bit change in the output of the A/D converter?

Detectable limit (code width) with respect to range, gain and resolution

- Resolution, range, and gain determine the smallest detectable change in signal voltage (code width).

$$\text{code width} = \frac{\text{converter range}}{\text{gain} * 2^{\text{resolution}}}$$

- Example: 10-bit converter, range = 0 to 5V, gain = 1

$$\frac{\text{converter range}}{\text{gain} * 2^{\text{resolution}}} = \frac{5}{1 * 2^{10}} = 4.88 \text{ mV}$$

Increase range: $\frac{10}{1 * 2^{10}} = 9.76 \text{ mV}$

Increase gain: $\frac{5}{2 * 2^{10}} = 2.44 \text{ mV}$

Detectable limit (code width) of Microchip Microcomputer (assuming 8 bits used)

$$\text{code width} = \frac{\text{converter range}}{\text{gain} * 2^{\text{resolution}}}$$

- Example: 8-bit board, range = 0 to 5V, gain = 1

$$\frac{\text{converter range}}{\text{gain} * 2^{\text{resolution}}} = \frac{5}{1 * 2^8} = 19.5 \text{ mV}$$

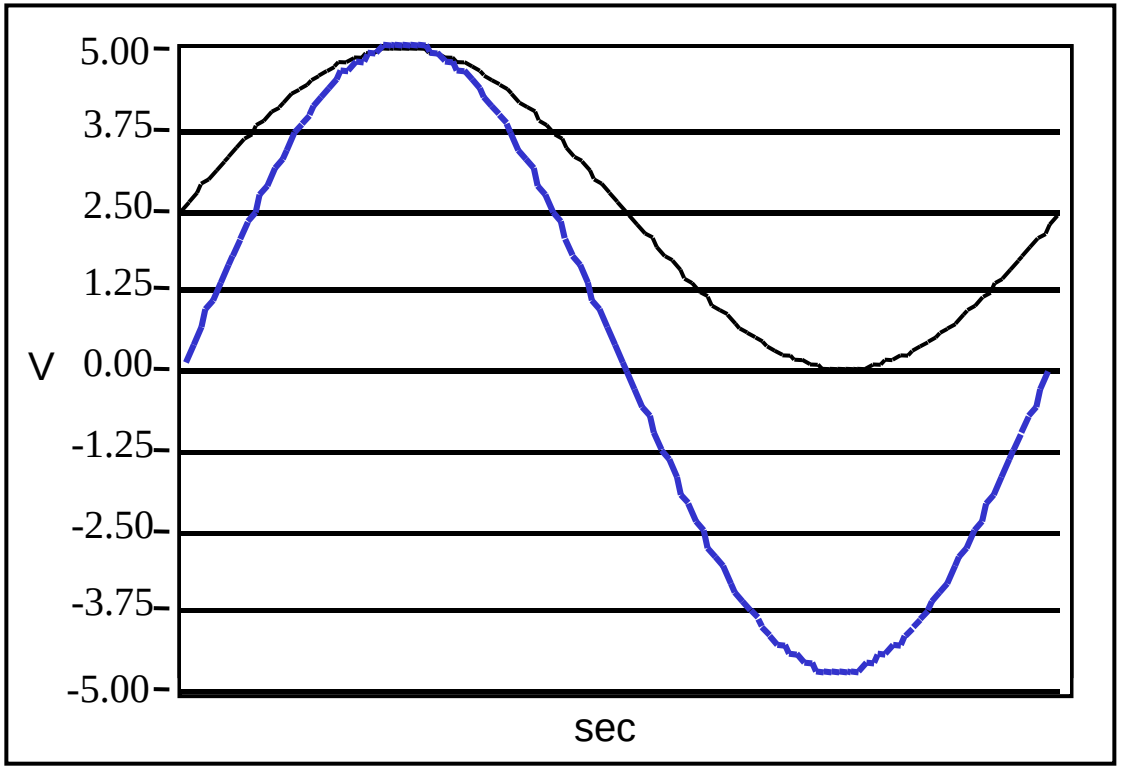
Increase range is not possible (cannot read 10 V)

Increase gain: $\frac{5}{2 * 2^8} = 9.8 \text{ mV}$

Signal Conditioning

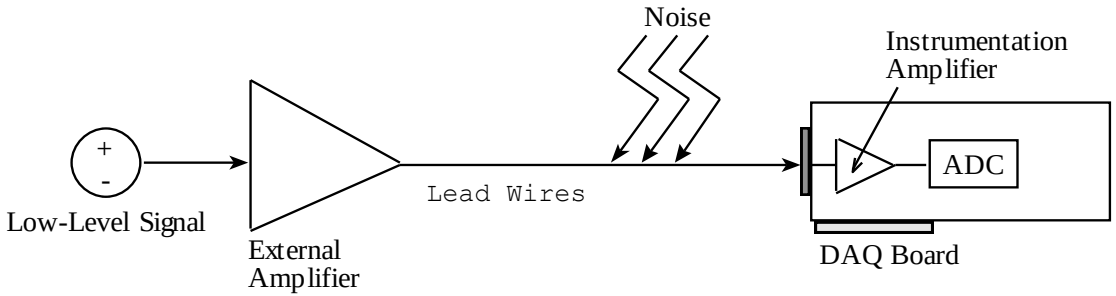
- Transducer Excitation
  - External voltage or current applied to transducer
  - Provided by signal conditioning hardware
- Linearization
  - Most transducers are not linear
  - Can be done in hardware or software
- Amplification
  - Amplification or Attenuation to span input range
  - Level shifting
- Filtering
  - Remove noise or unwanted signals
  - Remove 60 Hz AC noise from slowly sampled signals
  - Antialiasing filters

Unipolar or Bipolar



Microcontroller A / Ds are typically unipolar (0 to 5 Volts) and require level shifting and attenuation of bipolar signals.

Amplification increases accuracy and improves signal to noise ratio (SNR).

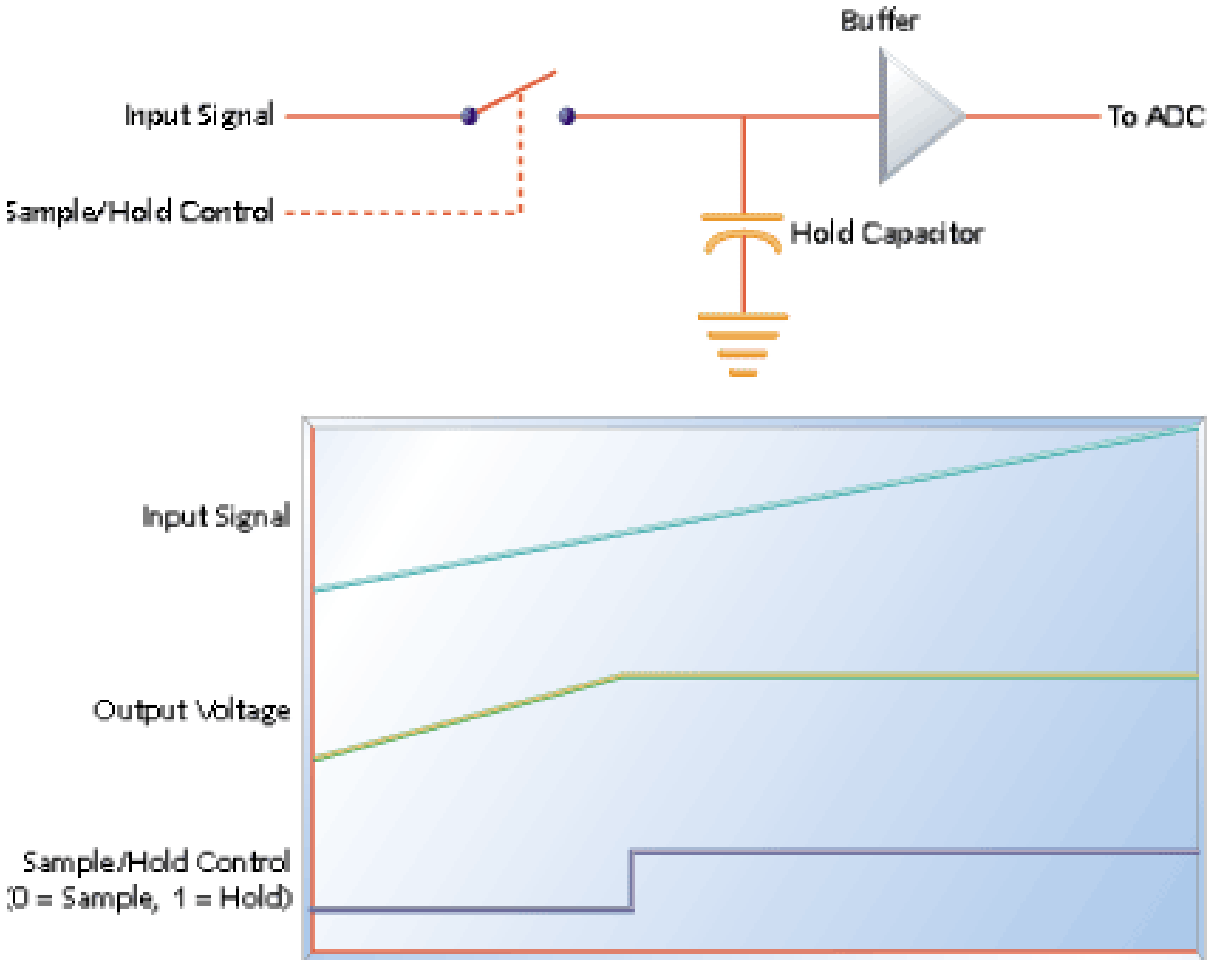


	Signal Voltage	External Amplification	Noise in Lead Wires	DAQ Board Amplification	Digitized Voltage	**SNR**
Amplify only at DAQ Board	.01 V	None	.001 V	x100	1.1 V	**10**
Amplify Externally and DAQ Board	.01 V	x10	.001 V	x10	1.01 V	**100**
Amplify only Externally	.01 V	x100	.001 V	None	1.001 V	**1000**

Sample and Hold

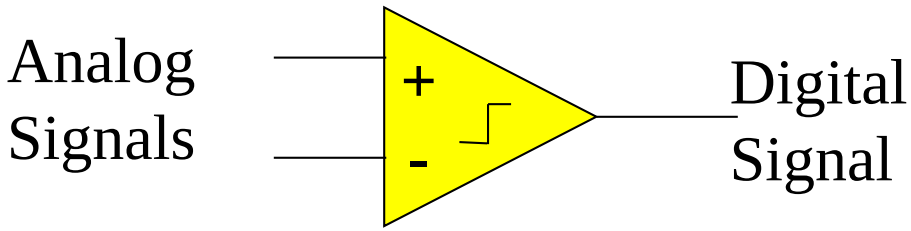
- Analog signal is held at a fixed value during the data conversion
- Can be thought of as charging a capacitor
- Sample and Hold (S /H)
  - Sample analog value and charge capacitor to this value
- Track and Hold (T/H)
  - Attach analog signal to capacitor and hold for conversion

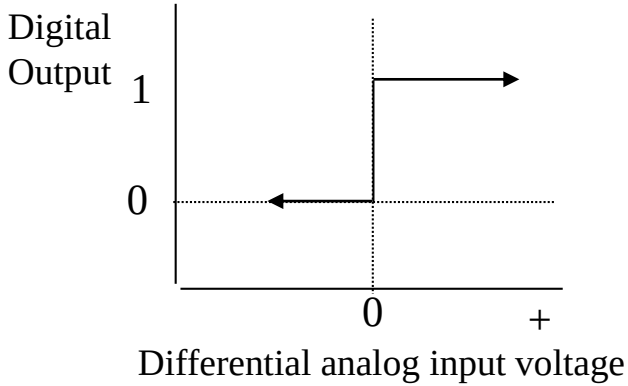
Sample and Hold Control



A / D Converters

- A fundamental building block of any A/D is a comparator.
- The comparator is really a 1 bit A/D
- It has 2 analog inputs and 1 digital output
- The comparator compares 2 analog signals
  - If the voltage of the + input is greater than the voltage at the – input, the digital output is 1.
  - If the voltage of the - input is greater than the voltage at the + input, the digital output is 0.



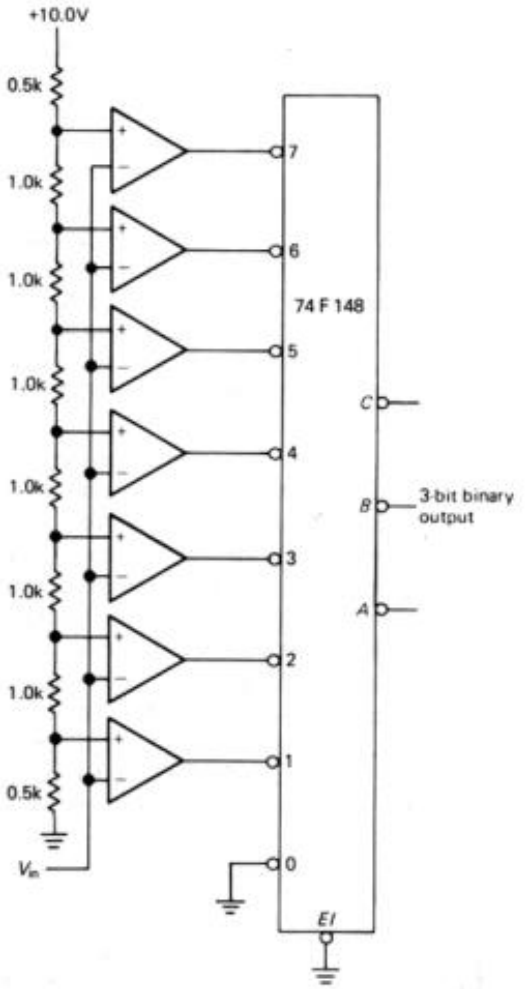


Types of A/D Converters

- Flash
- Successive – Approximation Register
- Multistage
- Integrating
- Sigma - Delta

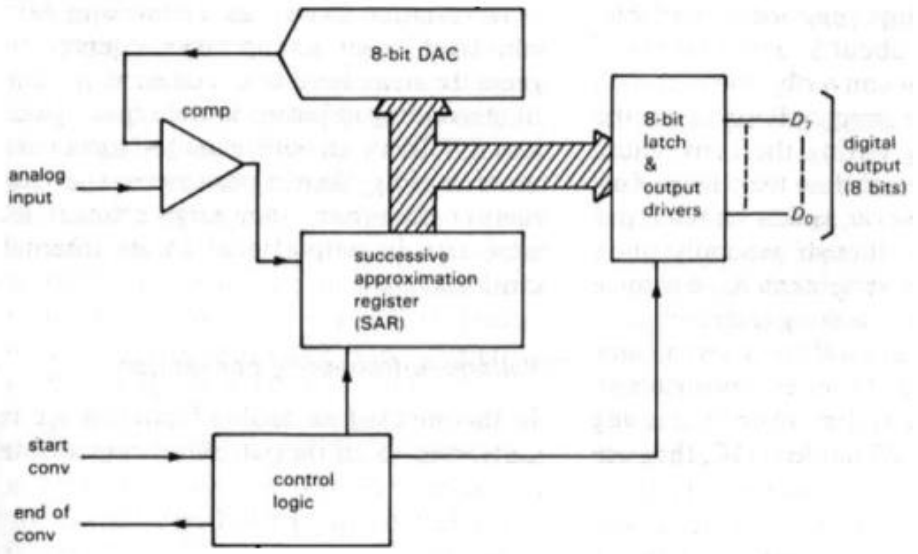
Flash Converters

- Simultaneous conversion
- Does not require S/H
- Video application
- Very fast
- N bits of resolution requires $2^n - 1$ comparators
- Accuracy requires precision resistors
- Comparator output called "thermometer code"
- Logic converts thermometer code to normal n-bit binary numbers



Successive Approximation Register (SAR) Converters

- Contains a D/A
- Most common electronic A/D
- Low cost
- Good linearity
- SAR sequences the D/A through a series on n guesses of the analog value which are compared in the comparator

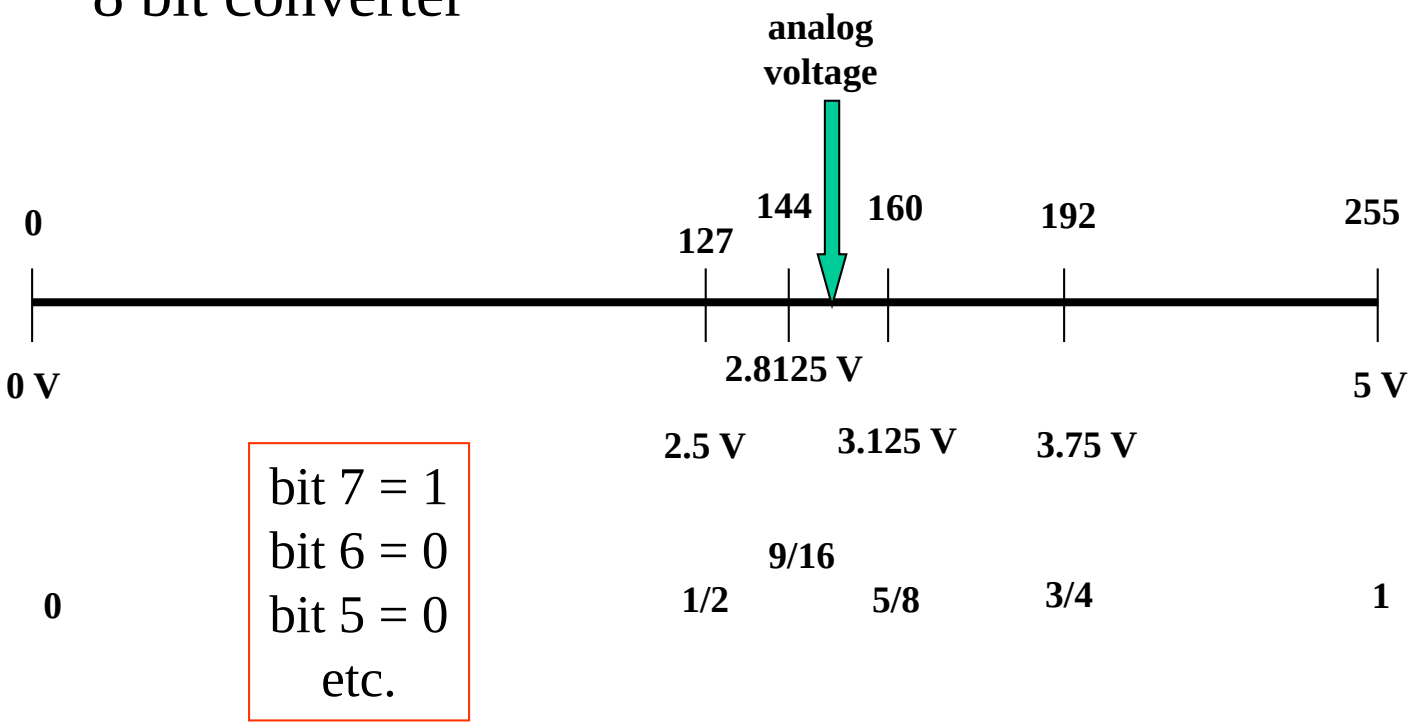


D/A in feedback loop

A/D on MicroChip PIC16F74 is a SAR A/D

Successive Approximation Concept

8 bit converter



bit 7 = 1
bit 6 = 0
bit 5 = 0
etc.

Each bit requires one A/D clock cycle (must meet minimum time).
Two to three additional cycles required for settling.
Final result must be written to register (requiring time).

A / D Conversion Steps

- Select the Channel to Convert
- Configure and Enable the A/D
- Wait the Acquisition Time
- Initiate the Conversion
- Wait for the Conversion to Complete (or Enable Interrupt)
- Read the Result

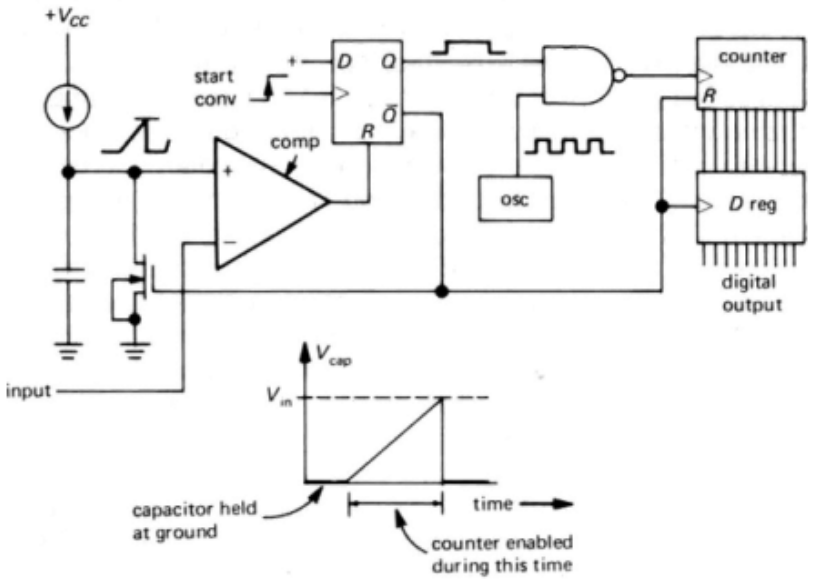
Timing is still required in C.

Multistage

- Higher sample rates at higher resolutions than SAR converters
- Replace comparator with low resolution (4 to 8 bit) flash converter
- Convert upper range and lower range of analog signal in stages
- Adding a S/H or T/H at the input will allow converter to process signals in a pipeline
- Also called a subranging or multipass A/D converter

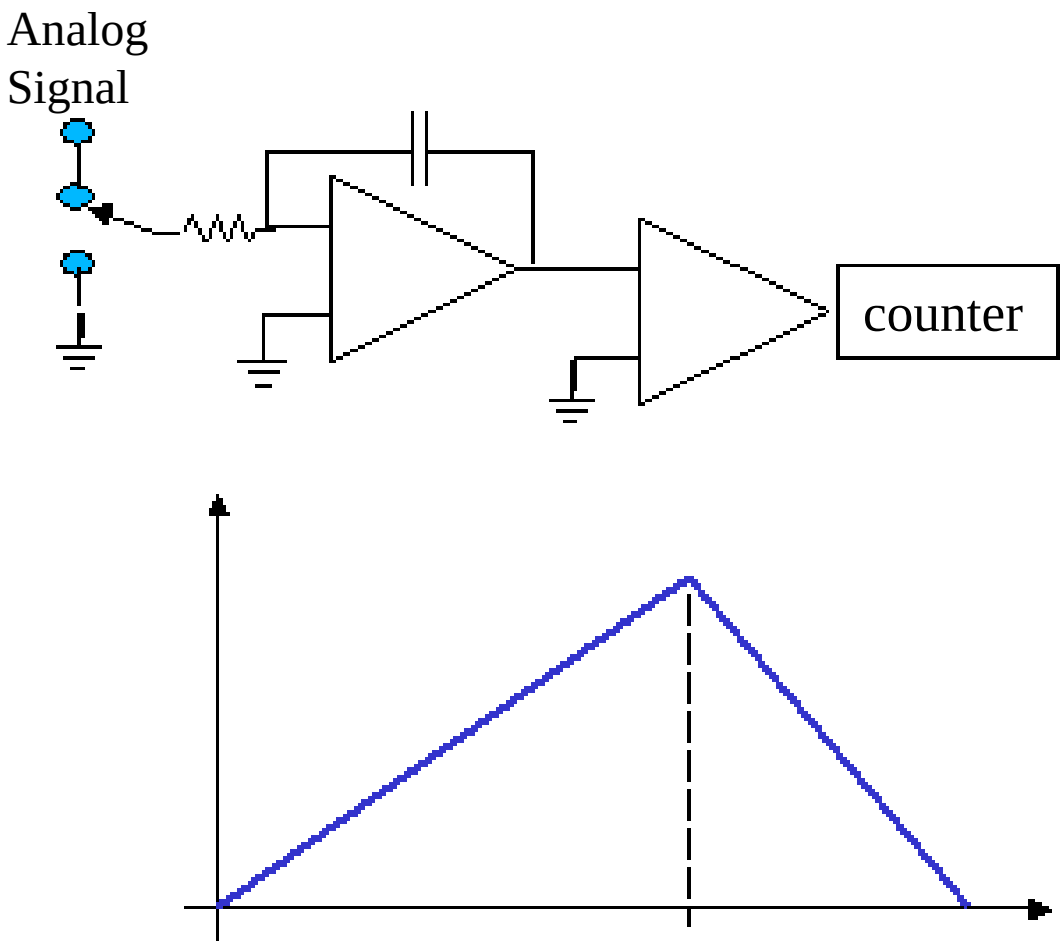
Integrating

- Low speed
- High resolution
- Voltmeters
- Integrate analog signal until it reaches a certain value
- Record the time required (count pulses)

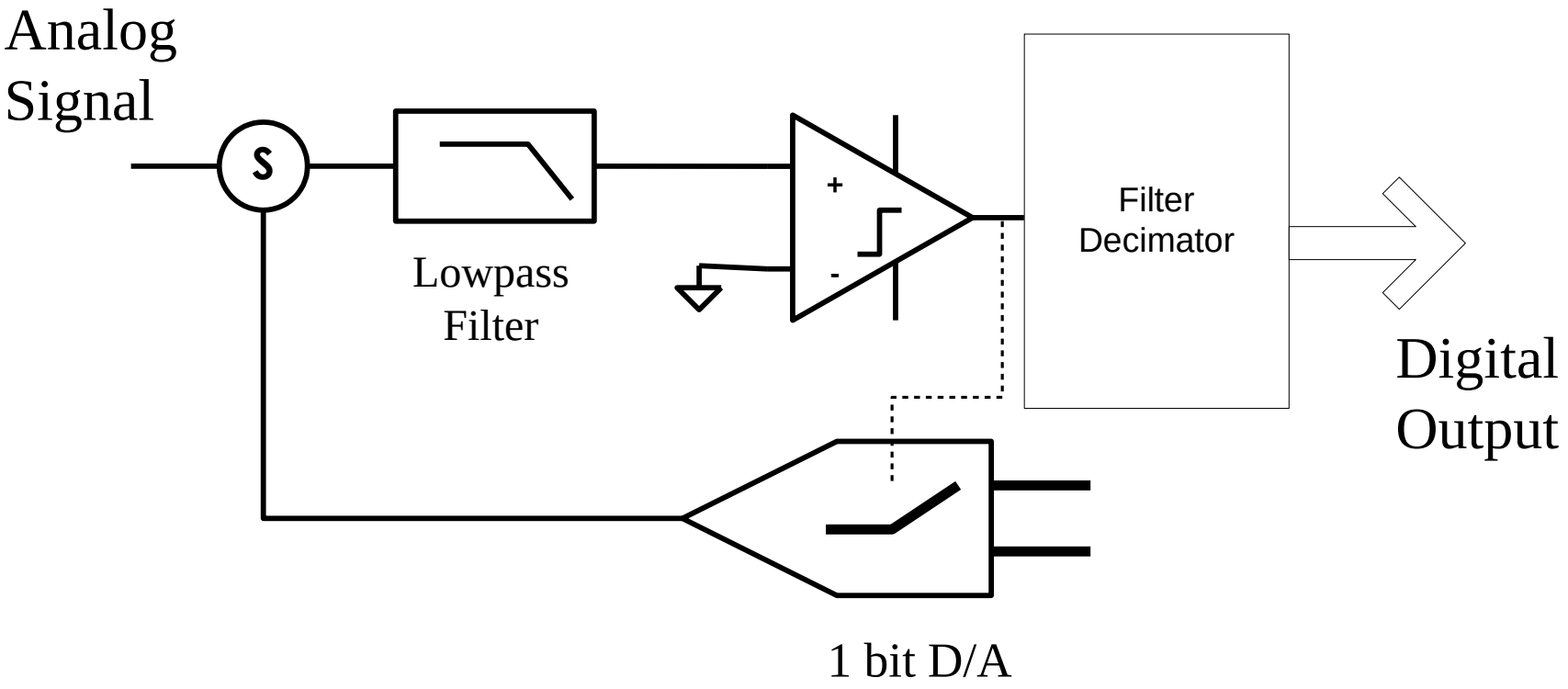


Dual Slope Integrating

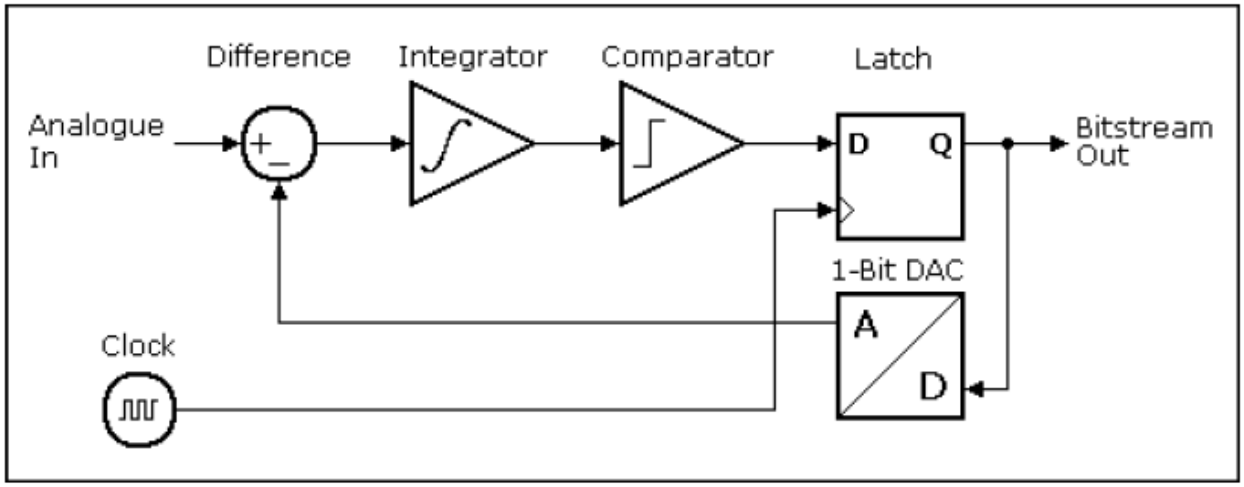
- Time required to integrate in positive and negative direction



Sigma Delta Converter



First Order Sigma Delta Operation



Pulse Proportion Modulation (PPM) as opposed to Pulse Code Modulation (PCM) for other A/Ds

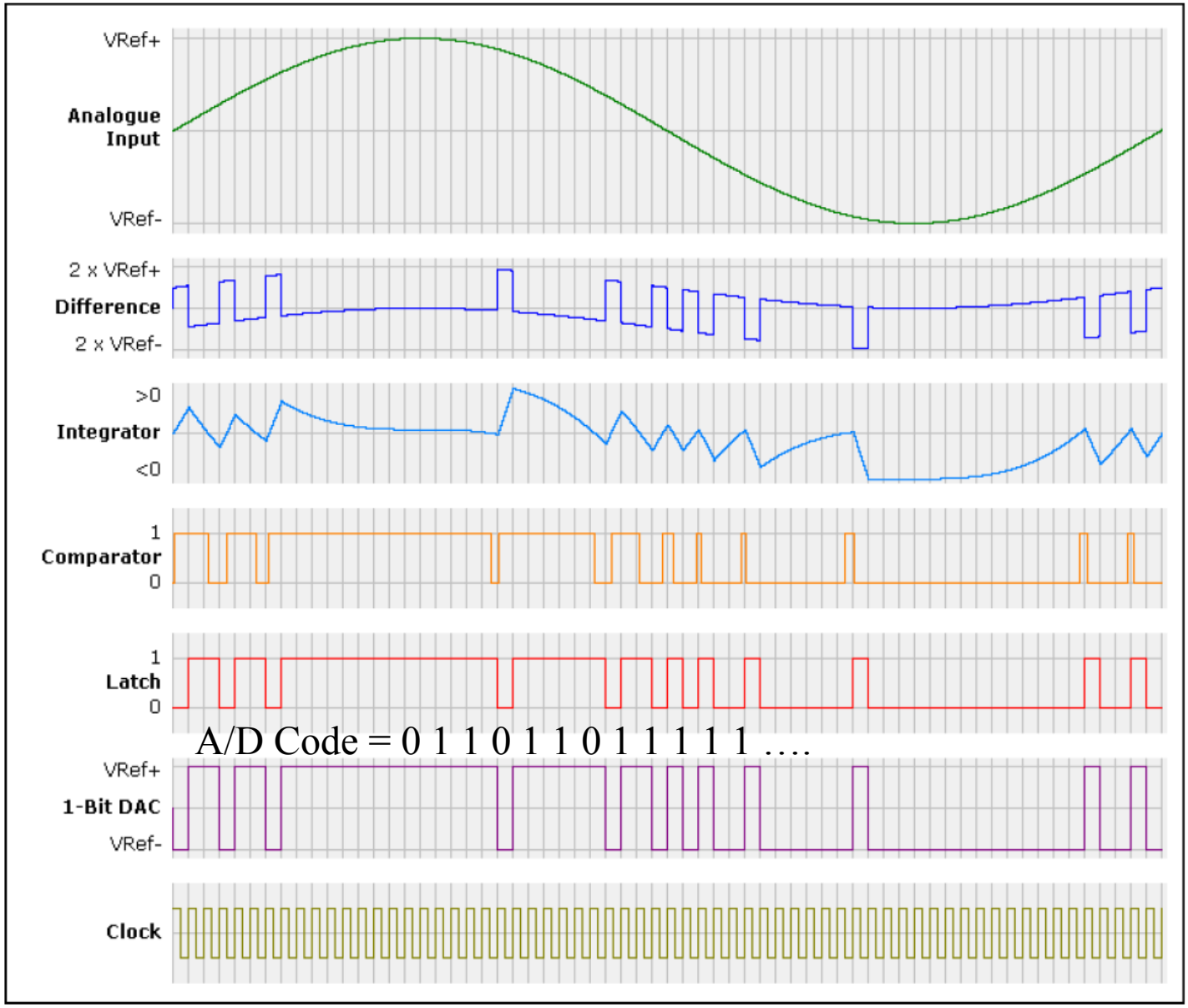
Comparator outputs digital 0 when input < 0
digital 1 when input > 0

1-bit DAC produces voltage $V_{ref}+$ when input = 1
voltage $V_{ref}-$ when input = 0

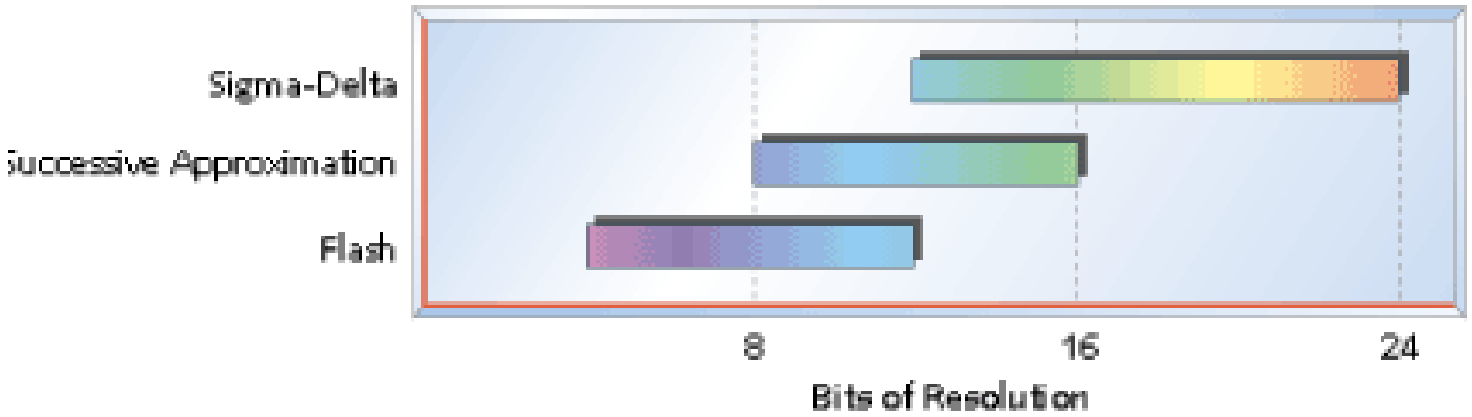
Sigma Delta A/D Signals

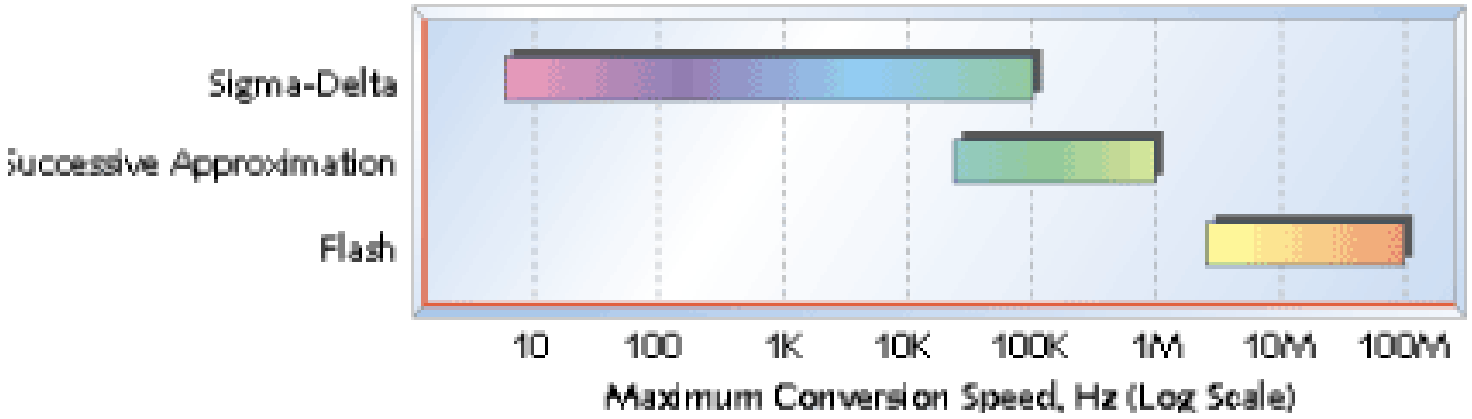
clock rate shown is 64x analog frequency

If you want to "oversample" a 20 kHz bandwidth audio signal at 48 kHz you want clock rate 48 x 64 kHz = 3.07 MHz



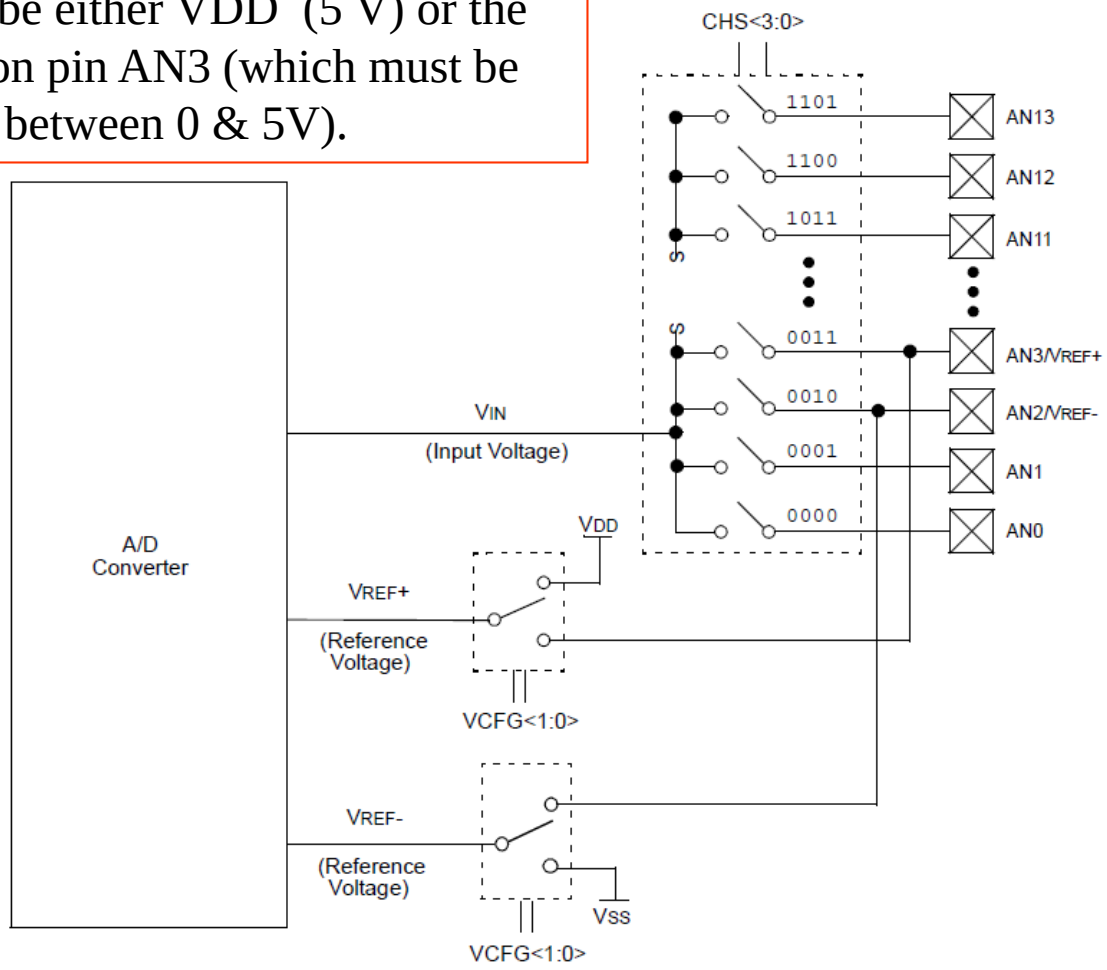
A/D Comparison





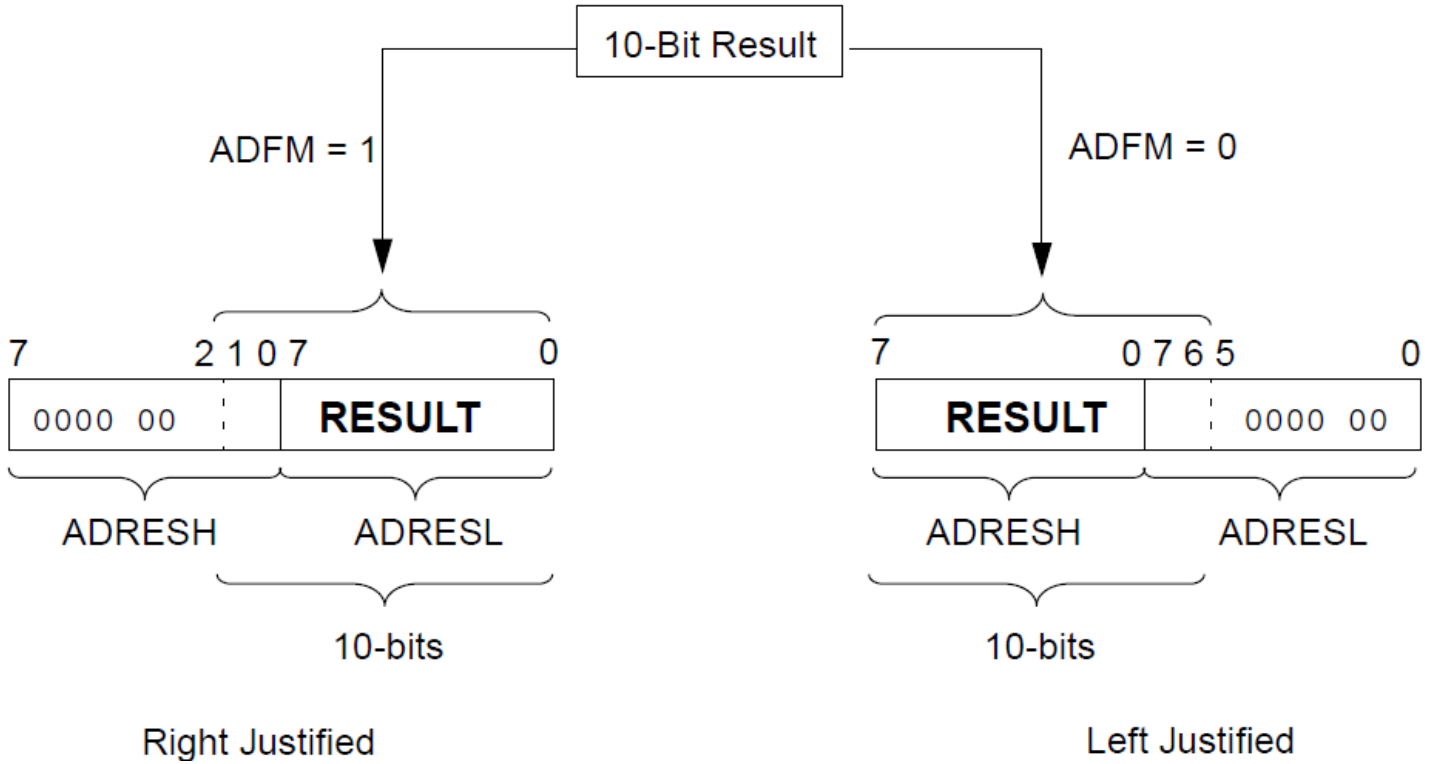
PIC16F747 A/D Block Diagram

The reference voltage for the A / D can be set to be either VDD (5 V) or the voltage on pin AN3 (which must be between 0 & 5V).

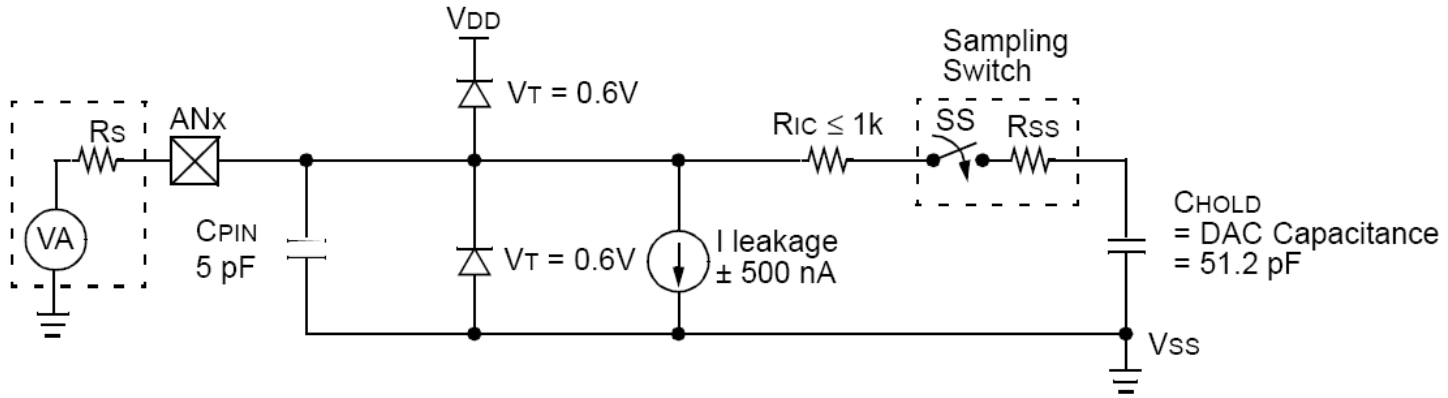


PIC16F747 A/D Result

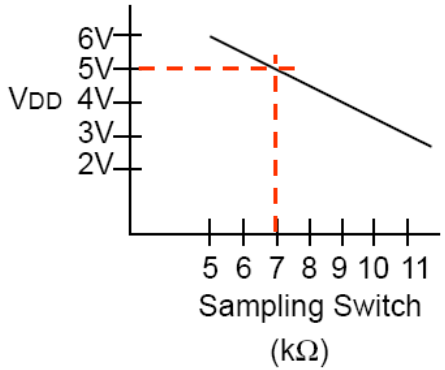
The result for the A / D can be either right or left justified depending on the ADFM bit in ADCON1. Should use ADFM == 0 for these case studies.



PIC16F747 Analog Input Model



Legend		
	C_{PIN}	= input capacitance
	V_T	= threshold voltage
	I leakage	= leakage current at the pin due to various junctions
	R_{IC}	= interconnect resistance
	SS	= sampling switch
	C_{HOLD}	= sample/hold capacitance (from DAC)



NOTE: F_{osc} is frequency of the microcomputer oscillator (e.g. 4 MHz)
T_{osc} is period of the microcomputer oscillator = 1 / F_{osc} (e.g. 250 nsec)
T_{ins} is the instruction cycle period = 4 x T_{osc} (e.g. 1 μsec)

T_{ACQ} = Amplifier Settling Time +
Holding Capacitor Charging Time +
Temperature Coefficient Time
= $T_{AMP} + T_C + T_{COFF}$

TAMP + TC + TCOFF

2 μs + TC + [(Temperature – 25°C)(0.05 μs/°C)]

CHOLD (RIC + RSS + RS) In(1/2047)

-120 pF (1 kΩ + 7 kΩ + 10 kΩ) In(0.0004885)

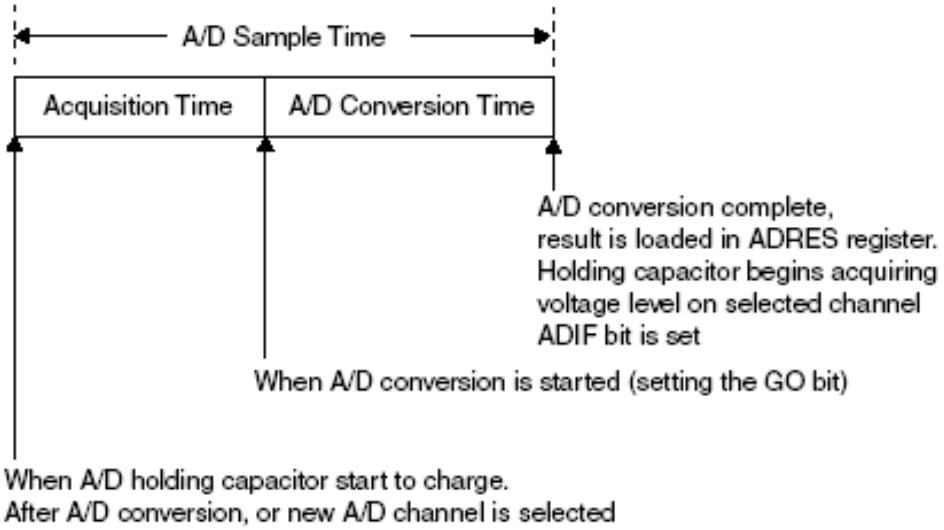
16.47 μs

2 μs + 16.47 μs + [(50°C – 25°C)(0.05 μs/°C)

19.72 μs

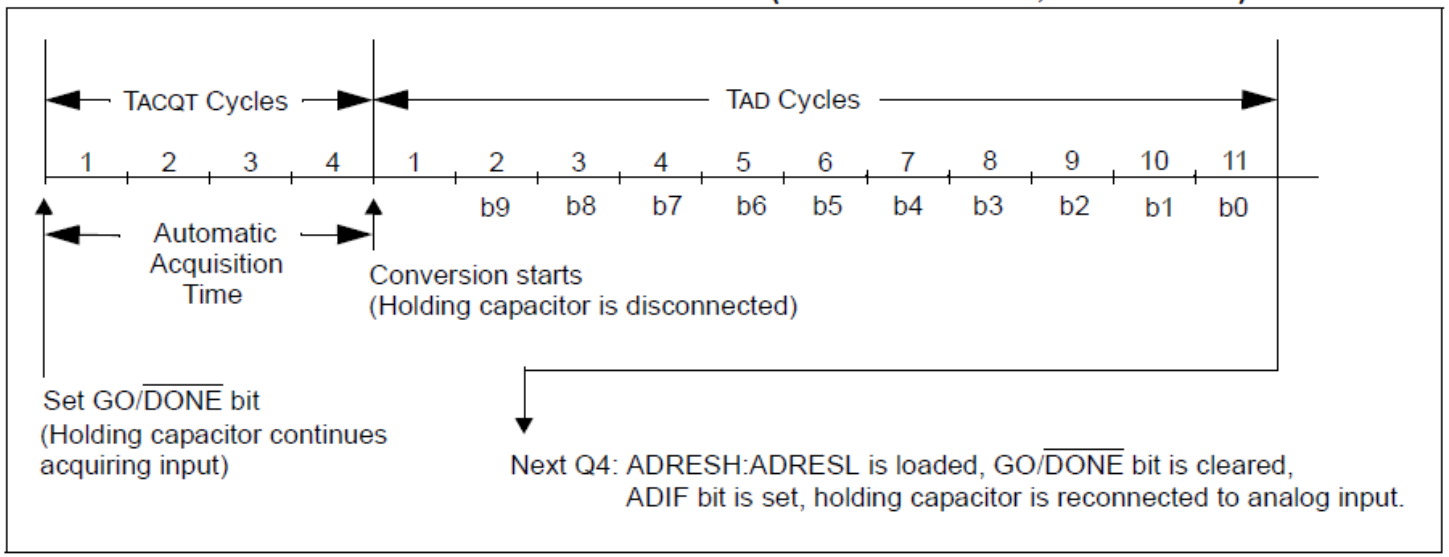
A/D Acquisition Time

A/D Sample Time



A / D Conversion Time

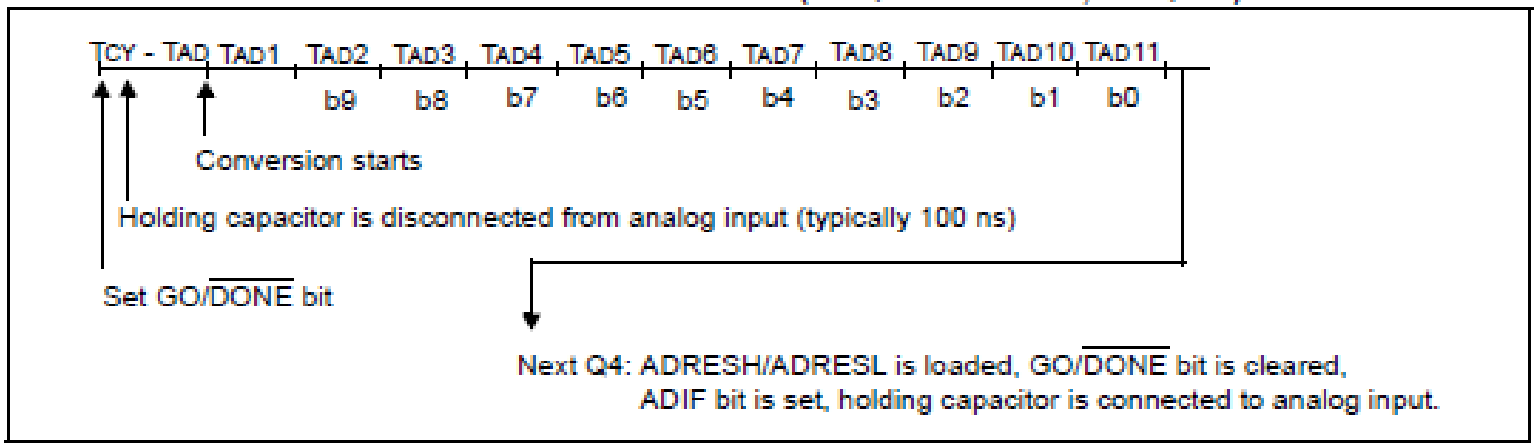
FIGURE 12-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



A/D Sample Time

A / D Conversion Time
Single Channel

FIGURE 12-3: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)



A/D Sample Time

A / D operates slower than the CPU

TABLE 12-1: TAD vs. MAXIMUM DEVICE OPERATING FREQUENCIES (STANDARD DEVICES (F))

AD Clock Source (TAD)		Maximum Device Frequency
Operation	ADCS2:ADCS1:ADCS0	
2 TOSC	000	1.25 MHz
4 TOSC	100	2.5 MHz
8 TOSC	001	5 MHz
16 TOSC	101	10 MHz
32 TOSC	010	20 MHz
64 TOSC	110	20 MHz
RC(1,2,3)	x11	**(Note 1)**

Setting A/D Conrol Registers

ADCON0

bit 7-6 **ADCS1:ADCS0**: A/D Conversion Clock Select bits

If ADCS2 = 0:
000 = Fosc/2
001 = Fosc/8
010 = Fosc/32
011 = FRC (clock derived from an RC oscillation)

If ADCS2 = 1:
00 = Fosc/4
01 = Fosc/16
10 = Fosc/64
11 = FRC (clock derived from an RC oscillation)

bit 7							bit 0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	CHS3	ADON
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

bit 5-3 **CHS<2:0>**: Analog Channel Select bits

0000 = Channel 00 (AN0)
0001 = Channel 01 (AN1)
0010 = Channel 02 (AN2)
0011 = Channel 03 (AN3)
0100 = Channel 04 (AN4)
0101 = Channel 05 (AN5)(1)
0110 = Channel 06 (AN6)(1)
0111 = Channel 07 (AN7)(1)
1000 = Channel 08 (AN8)
1001 = Channel 09 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12)
1101 = Channel 13 (AN13)
111x = Unused

Note 1: Selecting AN5 through AN7 on the 28-pin product variant (PIC16F737 and PIC16F767) will result in a full-scale conversion as unimplemented channels are connected to VDD.

bit 2 **GO/$\overline{\text{DONE}}$**: A/D Conversion Status bit

1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle. This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress

bit 1 **CHS<3>**: Analog Channel Select bit (see bit 5-3 for bit settings)

bit 0 **ADON**: A/D Conversion Status bit

1 = A/D converter module is operating
0 = A/D converter is shut-off and consumes no operating current

Setting A/D Conrol Registers

ADCON1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM**: A/D Result Format Select bit

1 = Right justified. Six Most Significant bits of ADRESH are read as '0'.
0 = Left justified. Six Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2**: A/D Clock Divide by 2 Select bit

1 = A/D clock source is divided by two when system clock is used
0 = Disabled

bit 5 **VCFG1**: Voltage Reference Configuration bit 1

0 = VREF- is connected to VSS
1 = VREF- is connected to external VREF- (RA2)

bit 4 **VCFG0**: Voltage Reference Configuration bit 0

0 = VREF+ is connected to VDD
1 = VREF+ is connected to external VREF+ (RA3)

bit 3-0 **PCFG<3:0>**: A/D Port Configuration bits

	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
0000	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	D	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	D	A	A	A	A	A	A	A	A	A
0111	D	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Legend: A = Analog input, D = Digital I/O

Setting A/D Conrol Registers

ADCON2

U-0	U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
—	—	ACQT2	ACQT1	ACQT0	—	—	—
bit 7							bit 0

bit 7-6 **Unimplemented**: Read as '0'

bit 5-3 **ACQT<2:0>**: A/D Acquisition Time Select bits

000 = 0(1)
001 = 2 TAD
010 = 4 TAD
011 = 6 TAD
100 = 8 TAD
101 = 12TAD
110 = 16 TAD
111 = 20 TAD

Note 1: If the A/D clock source is selected as RC, a time of TCY is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

bit 2-0 **Unimplemented**: Read as '0'

Conversion to Binary

2's complement

	+	6	5	4	3	2	1	0
127	0	1	1	1	1	1	1	1
126	0	1	1	1	1	1	1	0
2	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	1	1	1
-2	1	1	1	1	1	1	1	0
-3	1	1	1	1	1	1	0	0
-126	1	0	0	0	0	0	1	0
-127	1	0	0	0	0	0	0	1
-128	1	0	0	0	0	0	0	0

Adding an Offset for Monotonic Progression

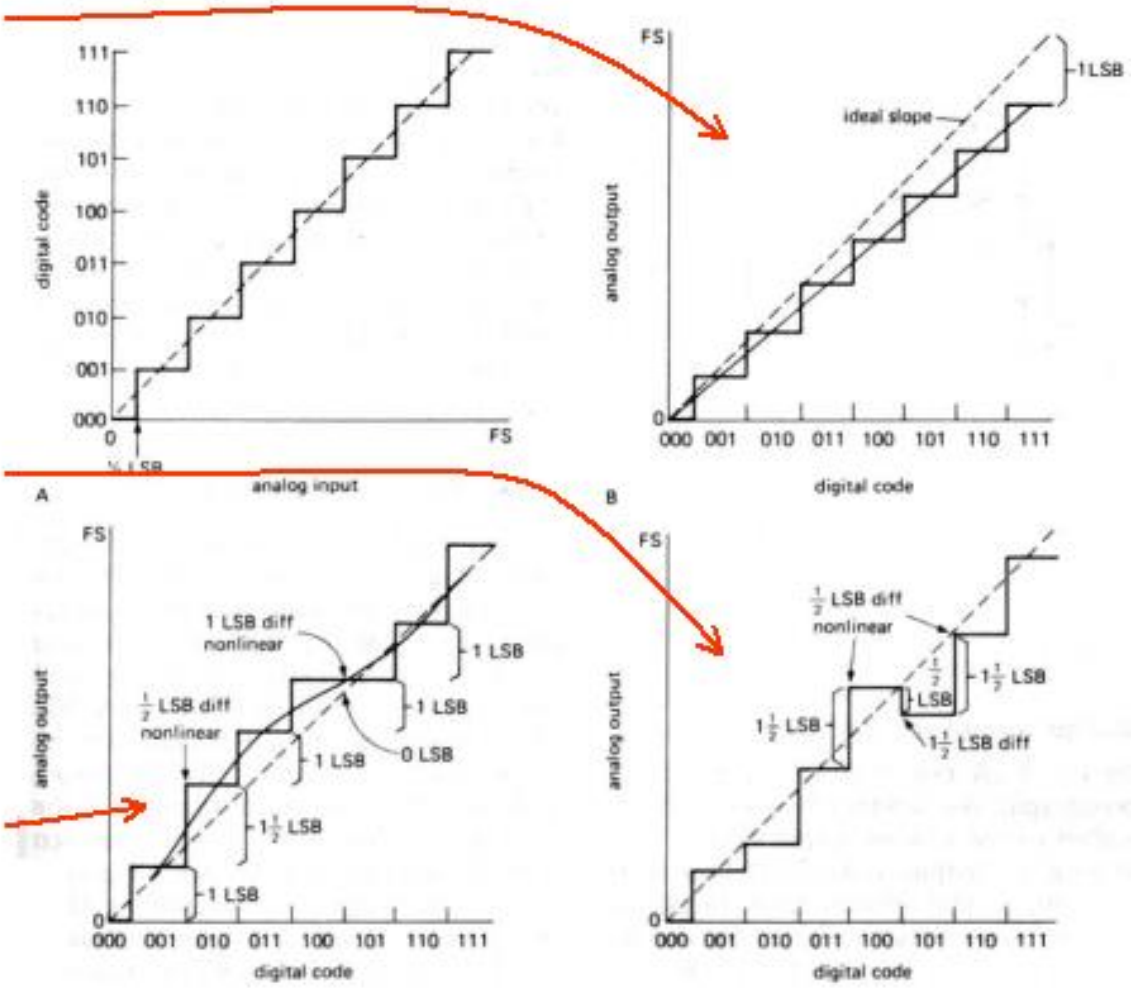
	+	6	5	4	3	2	1	0
127	1	1	1	1	1	1	1	1
126	1	1	1	1	1	1	1	0
2	1	0	0	0	0	0	1	0
1	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0
-1	0	1	1	1	1	1	1	1
-2	0	1	1	1	1	1	1	0
-3	0	1	1	1	1	1	0	0
-126	0	0	0	0	0	0	1	0
-127	0	0	0	0	0	0	0	1
-128	0	0	0	0	0	0	0	0

Errors in Conversion

Linearity (slope) errors

Non-monotonic errors

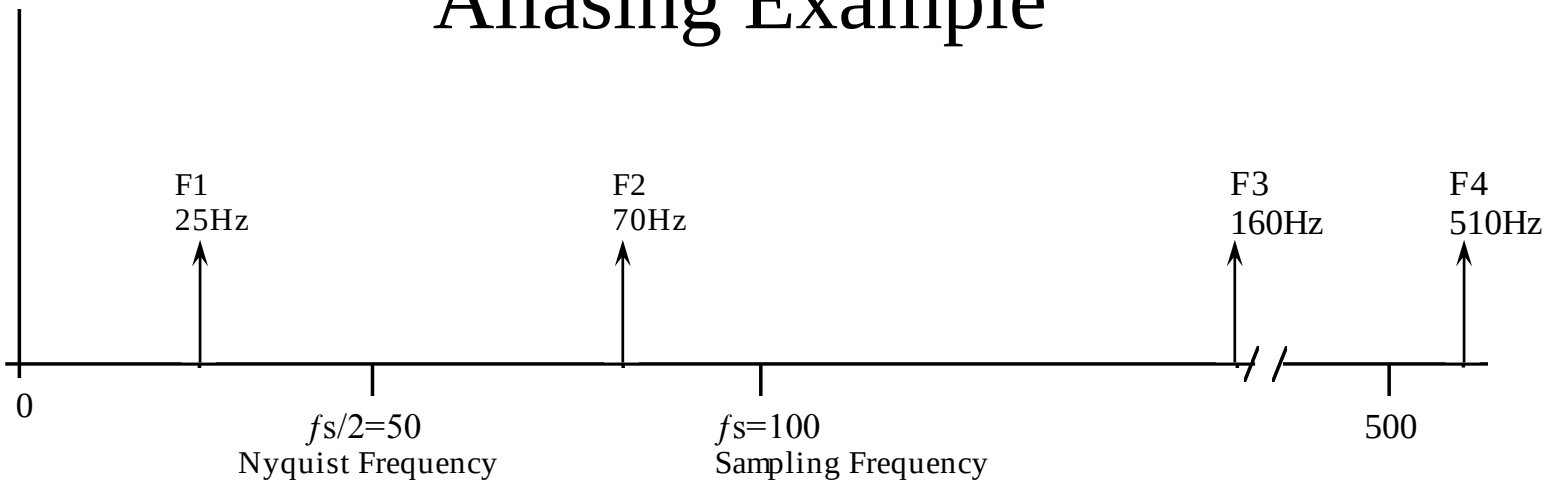
Nonlinear errors



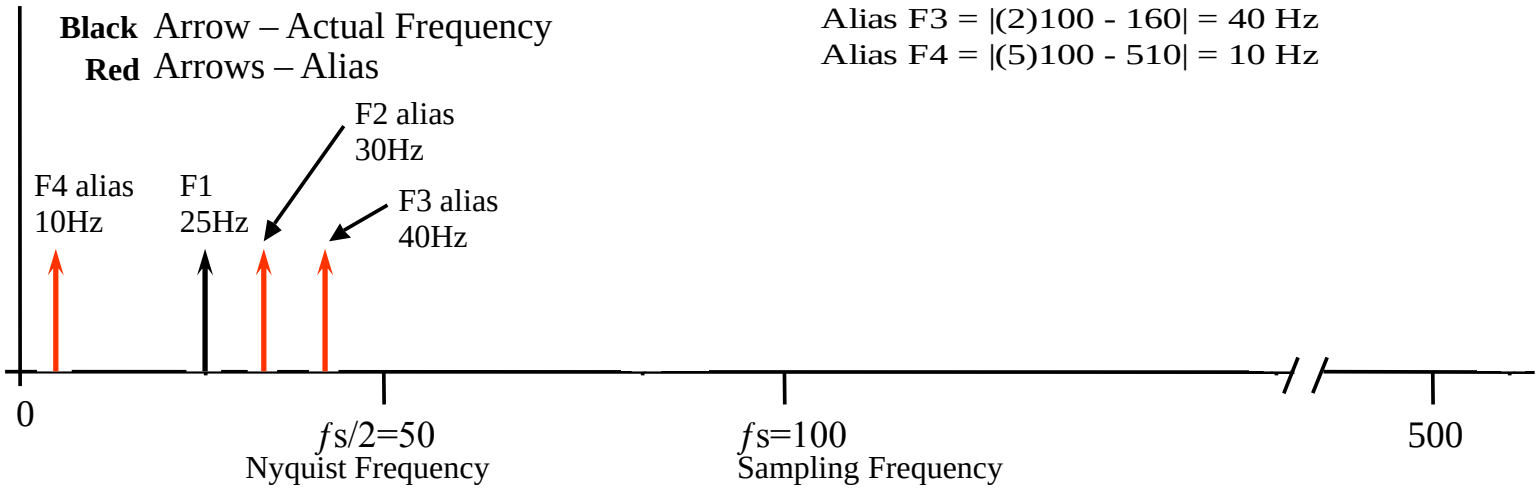
Aliasing

- Nyquist Theorem – sample at greater than twice the rate of the maximum frequency component in the input signal
- Nyquist frequency – half the sampling frequency
- Only possible to recover frequencies at or below Nyquist
- Frequencies above Nyquist will “alias” between DC and Nyquist
- Alias frequency = Absolute Value (closest integer multiple of sampling frequency - input frequency)

Aliasing Example

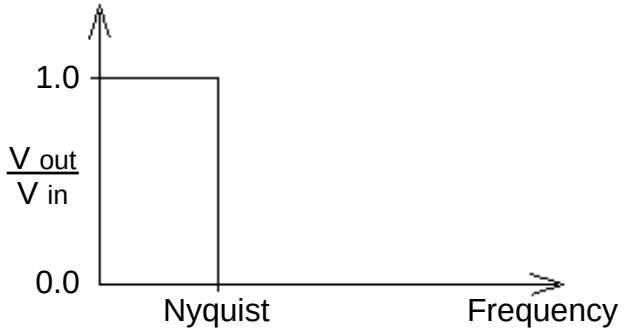


Alias F2 = |100 - 70| = 30 Hz
Alias F3 = |(2)100 - 160| = 40 Hz
Alias F4 = |(5)100 - 510| = 10 Hz

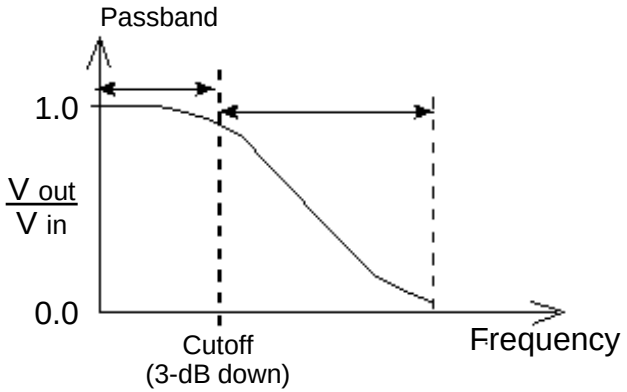


Preventing Aliasing

- Oversampling
- Use filters designed to eliminate frequencies over Nyquist frequency
- Use combination of both because real-world filters exhibit some roll-off
- Use special antialiasing filters that have sharp roll-off



Ideal Filter



Real-World Filter