Mechatronics & Embedded Microcomputer Control ME E4058 Spring 2017

Case Study #2: Introduction to Analog Electronics

The true power of a mechatronic design comes from the application of electronics to mechanical design. For the most part, the last several years have seen the pervasive use of microcomputers in industrial products. Microcomputers provide the control and user interface. Low cost microcomputers are the primary electronic component of a mechatronics design.

Although the microcomputer is ubiquitous, analog electronics, components that produce an electronic signal continuous in both time and amplitude, provide many necessary functions. Analog signal conditioning is necessary to interface sensors to microcomputers. Analog processing of digital signals provide the drive for actuators. Analog electronics provide amplification and filtering, two important system aspects. Analog electronics can compensate for system delay and system phase lag and thus enable feedback control.

While the components in the field of analog electronics are changing very rapidly, the fundamental laws describing the operation of these electronic devices and the methods of analysis used to understand electronic circuits change only slowly, if at all, and so the emphasis for this case study is an understanding of the fundamentals and the basic vocabulary used in analog electronics. A good working knowledge of electronics has four distinct elements:

- knowledge of the basic physical laws that apply to the operation of electronic devices, including basic device laws
- knowledge of circuit analysis techniques, i.e., the mathematical techniques used to understand the operation of circuits (Kirchoff's Voltage and Current Law)
- knowledge of the state of the art in electronic components in order to decide how to proceed with a particular design and what parts to use
- mastery of the vocabulary of electronics which is essential for reading the electronics literature

Of these four, only the third element changes very rapidly.

The goal in the second case study is to provide an understanding of these elements of analog electronics as they relate to mechatronic system design.

The case study is divided into three sections:

- > Part 1 deals with passive components and the concept of impedance.
- > Part 2 involves the primary active analog electronic component the opamp.
- > Part 3 involves the use of analog electronics to control a fundamentally unstable system magnetic levitation.

Part 1: Resistors, Capacitors, Inductors, DC / AC Circuits, RC (Filter) Circuits, Impedance, Loading Effects

Introduction:

This case study is a review of the three most fundamental passive electronic components, the resistor, capacitor and inductor together comprising the essential building blocks of both analog and digital circuitry. Kirchoff's laws provide the means of analyzing and constructing analog circuits using these components. You will examine some basic circuits: voltage dividers, RC filters and RLC filters (2nd order filters) in this case study. You will learn about input / output impedance and loading effects, two important concepts for any mechatronics engineer to know. You will also begin to learn, through analysis and experimentation, the relationship between the time domain (exemplified by differential equations) and the frequency domain (exemplified by transfer functions and Bode plots). Obviously, much of this is a review in the basics of circuits that nearly all of you have, at one point or another, already seen. Yet it is precisely for this reason that it is so important that you master these basics, particularly from a design point of view. Voltage dividers and RC filters are elementary circuit fragments. They are also, in fact, two of the most useful and applicable circuit fragments to know as a mechatronics engineer, since a host of common electronic devices are based on them and they are often used in conjunction with microcomputer systems to perform basic functions.

Laboratory Procedure:

General procedure:

- Assume nothing
- Using the multimeter, measure all resistors and capacitors. Note values. Note tolerances.
- You can also use the multimeter to check + 15 V and -15 V on the power supply. Remember that all the power supply voltages are relative to the one reference terminal labeled **COM**.
- Using the multimeter, check the connectivity on the protoboard.

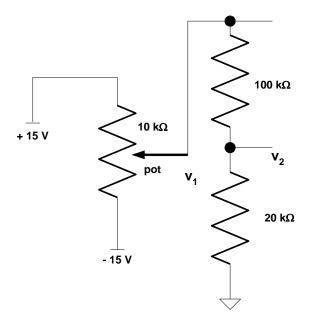
1. Voltage Divider

This circuit illustrates Kirchoff's current and voltage laws.

You do not have to construct the circuit shown. If you want, you can construct the circuit on the protoboard to check your answers.

Note the polarity of the power supplies. The laboratory power supply has to be adjusted to output 15 Volts on the high voltage terminals. Recall that if the **Tracking** knob is switched all the way to the right, the negative terminal will track the voltage on the positive terminal. If the multimeter measures the point at which the –15 V attaches to the pot (potentiometer) relative to circuit ground (the **COM** terminal), it should read –15 V.

You will need to select a point for the ground. The most convenient point is the **COM** terminal on the power supply. As in the digital logic case study, you would typically choose one or more of the long column connections on the protoboard to serve as a ground strip. In this way, any wire inserted in that column would be connected to ground. (If this is not clear, please ask.) You would also use other long columns for each of the +15V and -15V power signals.



When you vary the position of the wiper on the pot (with the screw terminal) and note the voltage measured at v1, you should be able to measure any voltage between +15V and -15V (approximately).

a) If the voltage at the point v_1 is -10V, what should be the voltage at the point v_2 ? (Hint: assume that there is a -10V power supply attached to v_1 and use Kirchoff's voltage law to get the current in the fixed resistors and the resistor element law to get the voltage across the 20 k Ω resistor.) What is your prediction using the resistor values shown in the figure. If you measure v_2 to verify your prediction, would you expect to get what you predicted? If not, why not? (Hint: what if you measure the resistor values with the multimeter.)

- b) Repeat part a with the voltage at v_1 set to +6V.
- c) Power is dissipated in the resistors. Where does the power go?

2. RC Low Pass Filter Circuit

The circuit illustrates a first order passive electronic system.

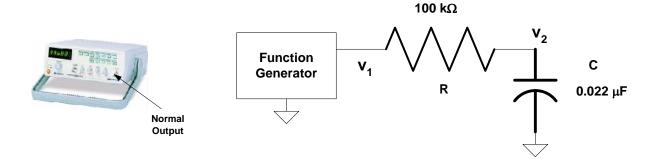
For this part of the case study, you will use the laboratory function generator and the oscilloscope.

Use the laboratory function generator to apply a signal. NOTE: in this case, you will be using the normal output ($Output\ 50\Omega$) from the function generator rather than the TTL output that was used in the digital logic case study. You will set the amplitude of the function generator using the oscilloscope. Recall that you can use the $Output\ Meas$ ($Output\ Meas$ ($Output\ Meas$) feature of the oscilloscope to measure amplitude of a signal. With the softkey and the entry knob, you can select which measurement you want and which channel you are measuring.

IMPORTANT NOTE: When you select phase using the **Quick Meas** menu, you will measure phase with channel 2 as the reference. For this reading (part e), you will want to measure v1 using channel 2 and v2 using channel 1. Otherwise, your reading will not be correct and inconsistent with MATLAB. Negative numbers indicate phase lag; positive numbers, phase lead.. The measurement should read **Phase** (1->2) indicating the phase of channel 1 relative to channel 2.

Construct the circuit shown.

Note that you will again need to select a point for the ground. At this ground point, you will connect the reference for the function generator, the reference for the oscilloscope and the ground point of the circuit. If this is not clear, please ask.

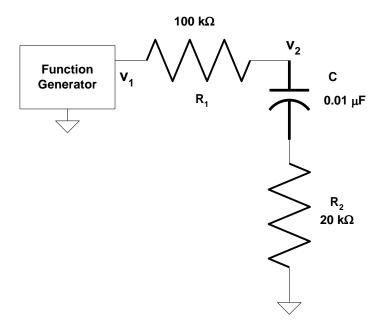


- a) Derive the transfer function for the system assuming that the voltage v₁ is the input and the voltage v₂ is the output. Express the transfer function in terms of R and C and then substitute the values shown and express the transfer function with numerical values.
- b) Derive the differential equation for the system again assuming that the voltage v_1 is the input and the voltage v_2 is the output. From the differential equation, predict the response of the system (the output v_2 as a function of time) for a unit step change in v_1 (i.e. for a change in v_1 between 0 volt and 1 volt). Sketch the response (approximately). What does this response represent?
- c) Set the function generator to output a low frequency square wave (amplitude \pm 0.5V, frequency 10 Hz, i.e. the signal should go from -0.5 V to + 0.5 V at a frequency of 10 Hz). Connect the signals v_1 and v_2 to the oscilloscope. Measure v_2 . Sketch the response and compare it to the prediction in part b (in words). (Note: this square wave is slow enough so that it essentially looks like a series of steps. You want to set the time base on the oscilloscope so that the time near the transition in the square wave is displayed.)
- d) Derive the frequency response for the system (i.e. take the transfer function that you derived in part a and set $s = j\omega$). What is the magnitude and phase of the frequency response at $\omega = 100$ rad/sec? At $\omega = 1000$ rad/sec? What is the magnitude and phase at a frequency of 100 Hz? (Note: ω in rad/sec = 2 π f in Hz) (Hint: use the *bode* command in MATLAB.)
- e) Plot the complete Bode plot for frequencies between 10 rad/sec and 10000 rad/sec. Save plot and attach it to the answer sheet.
- f) Change the function generator to output a \pm 0.5V sine wave at 100 Hz (i.e. a sine wave which is 1 V peak-to-peak). Verify the signal amplitude with the oscilloscope. Measure the amplitude and phase of v2 (see IMPORTANT NOTE above). Does this agree with your prediction? Measure the magnitude and phase at 1 kHz. What is this value?
- g) From the frequency response (Bode plot), why would you call this a low pass filter? Sweep the frequency from the function generator and note how the voltage v2 changes. Describe the response in words.
- h) What is the input impedance of this circuit as a function of ω (use the values for the resistor and capacitor)? The input impedance is the circuit impedance looking out the terminal of the function generator (i.e. looking into the resistor at the terminal marked v1). What is the output impedance? The output impedance is the circuit impedance looking into the terminal marked v2. (Note: the definition for output impedance is the impedance looking into the output terminal with all voltage and current sources dead. Since the function generator is a voltage source, for this analysis, you would replace it with a zero voltage source (or short circuit). In other words, you would analyze the impedance of the circuit with the terminal labeled v1 connected to ground.)

3. Passive Lag Circuit

Construct the circuit shown.

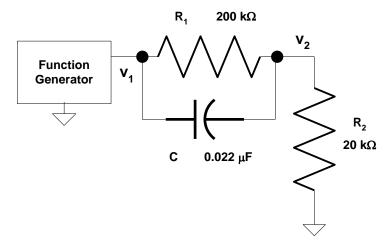
- a) Derive the transfer function for the system assuming that the voltage v1 is the input and the voltage v2 is the output. Express the transfer function in terms of R₁, R₂ and C and then substitute the values shown and express the transfer function with numerical values.
- b) Derive the differential equation for the system again assuming that the voltage v1 is the input and the voltage v2 is the output. How does this differ from the circuit in part 2 above?
- c) Set the function generator to output a low frequency square wave (amplitude \pm 0.5V, frequency 10 Hz). Connect the signals v1 and v2 to the oscilloscope. Measure v2 as a function of time. Sketch the result and compare it to the result in part 2 above.
- d) Derive the frequency response for the system. What is the magnitude and phase of the frequency response at $\omega = 100$ rad/sec? At $\omega = 1000$ rad/sec? What is the magnitude and phase at a frequency of 100 Hz?
- e) Plot the complete Bode plot for frequencies between 10 rad/sec and 10000 rad/sec. Save plot and attach it to the answer sheet.
- f) Change the function generator to output a 1V peak-to-peak sine wave at 100 Hz. Verify the signal amplitude with the oscilloscope. Measure the amplitude and phase of v2. Does this agree with your prediction? Measure the magnitude and phase at 1 kHz. What is this value? How is this response different from part 2 (in words)?



- g) What is the input impedance of this circuit (as a function of ω)? What is the output impedance?
- h) This circuit is called a lag circuit. It is a popular form of compensator in control systems. Sweep the frequency from the function generator and note how the voltage v2 changes. Describe the response in words. Pay particular attention to the phase.

4. Passive Lead Circuit

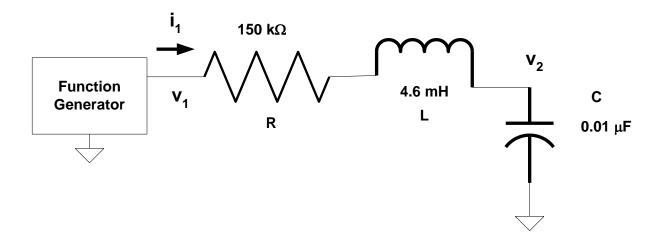
Construct the circuit shown.



- a) Derive the transfer function for the system assuming that the voltage v1 is the input and the voltage v2 is the output. Express the transfer function in terms of R₁, R₂ and C and then substitute the values shown and express the transfer function with numerical values.
- b) Derive the differential equation for the system again assuming that the voltage v1 is the input and the voltage v2 is the output. How does this differ from the circuit in part 3 above?
- c) Set the function generator to output a low frequency square wave (amplitude \pm 0.5 V, frequency 10 Hz). Connect the signals v1 and v2 to the oscilloscope. Measure v2 as a function of time. Sketch the response and compare it to the result in part 3.
- d) Derive the frequency response for the system. What is the magnitude and phase of the frequency response at $\omega=100~\text{rad/sec}$? At $\omega=1000~\text{rad/sec}$? What is the magnitude and phase at a frequency of 100 Hz?
- e) Plot the complete Bode plot for frequencies between 10 rad/sec and 10000 rad/sec. Save plot and attach it to the answer sheet.
- f) Change the function generator to output a 1V peak-to-peak sine wave at 100 Hz. Verify the signal amplitude with the oscilloscope. Measure the amplitude and phase of v2. Does this agree with your prediction? Measure the magnitude and phase at 1 kHz. What is this value? How is the response different from part 3?
- g) What is the input impedance of this circuit (as a function of ω)? What is the output impedance?
- h) This circuit is called a lead circuit. It is another popular form of compensator in control systems. Sweep the frequency from the function generator and note how the voltage v2 changes. Describe the response in words. Pay particular attention to the phase.

5. LRC Filter Circuit

Answer the following questions but you will not construct the circuit. (We do not have the inductor.)



- a) Derive the transfer function for the system assuming that the voltage v1 is the input and the voltage v2 is the output. Express the transfer function in terms of R, L and C and then substitute the values shown and express the transfer function with numerical values.
- b) Derive the differential equation for the system assuming that the voltage v1 is the input and the voltage v2 is the output.
- c) Derive the frequency response for the system. What is the magnitude and phase of the frequency response at $\omega=100$ rad/sec? At $\omega=1000$ rad/sec? What is the magnitude and phase at a frequency of 100 Hz?
- d) Plot the complete Bode plot for frequencies between 10 rad/sec and 10000 rad/sec. Save plot and attach it to the answer sheet.
- e) Derive the transfer function for the system assuming that the voltage v1 is the input and the current i₁ is the output. Express the transfer function in terms of R, L and C and then substitute the values shown.
- f) What is the input impedance of this circuit (as a function of ω)? (Hint use part d above.) What is the output impedance?
- g) For what purpose would you use this circuit? (Hint: look at the Bode plot.)

Part 2: Active Analog Electronics. Operational Amplifiers (OpAmps), Active Lead and Lag Circuits, Analog Filters and Buffers.

Introduction:

This part of the case study is an introduction to the most versatile analog integrated circuit (IC), the operational amplifier (OpAmp). OpAmps are used as a basic building block for a wide variety of analog signal processing applications. In control applications, OpAmps are used as compensators for the feedback loop. During this case study, you will become familiar with active electronic circuits used for controllers and active filters. In part 1, you built and tested a passive low-pass RC filter. In this part, you will construct active lead and lag controllers and compare the performance to the passive lead and lag controllers you built and analyzed in part 1. You will construct active high-pass and low-pass filters and compare their performance to the passive versions.

Laboratory Procedure:

General procedure:

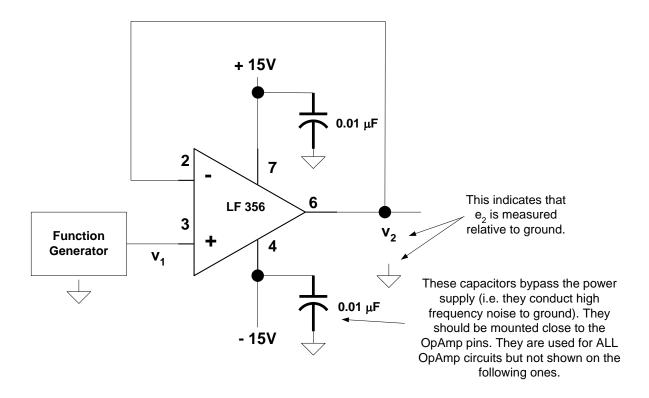
- Connect the + 15V, 15 V and ground (COM) from the power supply to the protoboard. Add a 0.1 μF polyester capacitor and a 10.0 μF electrolytic capacitor close to the where the power supply voltage is connected to the Protoboard at each of the supply voltages. NOTE: for the 15 V supply, the electrolytic capacitor should be connected so that the flow of positive current is INTO the 15 V terminal. If this is not clear, please ask. The capacitor can explode if connected improperly.
- The LF 356 OpAmp 8 pin package is numbered as shown in the figure below.



6. OpAmp Buffer

Construct the following OpAmp circuit.

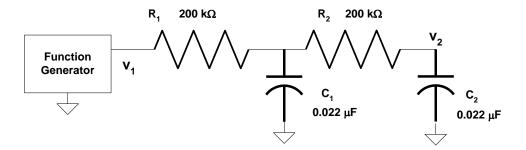
(**Note:** in the following exercises, different passive components will be connected to the inputs (pins 2 and 3) and output (pin 6) of the OpAmp. In each case, the function generator will be used as an input signal and the power supplies will be connected as shown below (pins 4 and 7). If you plan your protoboard layout with this circuit and route wires so that the power supply and function generator leads are out of your way, the remaining exercises will proceed more efficiently.)



- a) Examine the transfer function for the circuit assuming that the voltage v1 is the input and the voltage v2 is the output and the OpAmp is ideal. Express this transfer function using time constants (if needed) rather than circuit elements. (Note: There are two characteristics of OpAmps that define its bandwidth (i.e. the magnitude of its frequency response at high frequencies). For small amplitude inputs, it is simply the frequency response of the OpAmp. For large amplitude inputs, it is the slew rate (i.e. the ability of the OpAmp to produce large voltages versus time.))
- b) What is the input and output impedance for this circuit? (Hint: look at the data sheet for the LF356 OpAmp. The input impedance is listed; the output impedance is in a graph for which you need the results of part a.)

(Aside) Loading Effects in RC Circuits

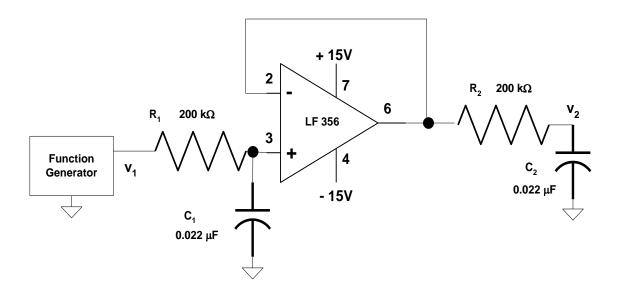
Consider the circuit shown. You do not have to construct this circuit. It is meant to illustrate the use of the OpAmp circuit that you constructed above.



Note that this is the two of the circuits that you constructed in exercise 2 cascaded.

If you derive the transfer function for the system assuming that the voltage v1 is the input and the voltage v2 is the output, it is a complicated expression of the 4 circuit elements R_1 , R_2 , C_1 and C_2 . If you wanted to construct a circuit that produced the square of the transfer function derived in exercise 2, this circuit would not be correct. This circuit looks like the cascade of two of the exercise 2 circuits but the transfer function is different from the square of the exercise 2 circuit. This is an example of loading effects in electronic circuits. The addition of R_2 and C_2 "loads" the response of R_1 and C_1 .

Next consider the following circuit.

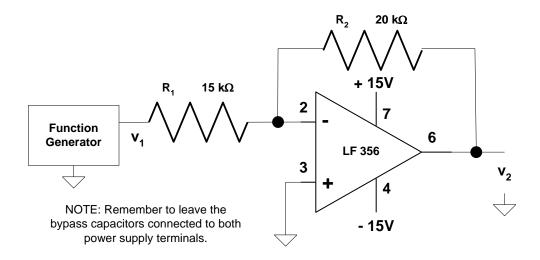


Note that the buffer amplifier has been placed between the two RC circuits. This circuit does produce the square of the transfer function derived in exercise 2. The buffer amplifier in the center of the circuit prevents the second resistor and capacitor from loading the first. This is

therefore a second order low pass filter. Buffer amplifiers are often used to prevent loading effects.

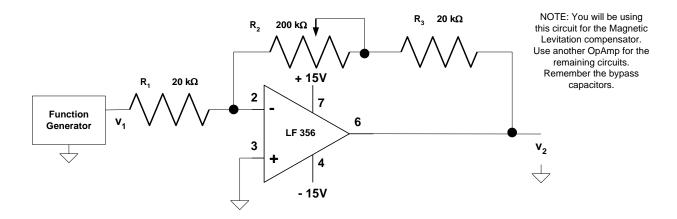
7. Basic Inverting Amplifier

Construct the circuit shown.



- a) Derive the transfer function for the system assuming that the voltage v1 is the input and the voltage v0 is the output. Express the transfer function in terms of R_1 and R_2 and then substitute the values shown and express the transfer function with numerical values. (Be careful of the sign of the output.)
- b) What is the frequency response of this circuit assuming that the OpAmp is ideal? What is the frequency response that you would expect from the data sheet? (Note: the gainbandwidth product for an opamp specifies the bandwidth that you should expect for a given gain.) Measure the response at several frequencies and verify your prediction. Did the measurements match prediction? Buffers (part 6) and amplifiers (part 7) are often used to condition transducer signals prior to bringing them into a microcontroller for control. (NOTE: the OpAmp cannot produce a voltage larger than the power supply voltages. You have to set the level of the input from the function generator so that the OpAmp does not saturate.)
- c) If you interchange the positions of the two resistors, how would you change the transfer function?

Replace the fixed $200~k\Omega$ resistor with a potentiometer and a fixed resistor connected as shown. In this arrangement, you are using the potentiometer as a variable resistor. Replace the 100~K input resistor with a 10~K resistor. The added $10~k\Omega$ resistor (R₃) insures that the gain never goes below unity.



d) With a fixed frequency sine wave from the function generator, note the response of the circuit as the wiper on the potentiometer is varied. Describe the response in words. This circuit is often used to adjust transducer signals and is often called a "trimming" circuit.

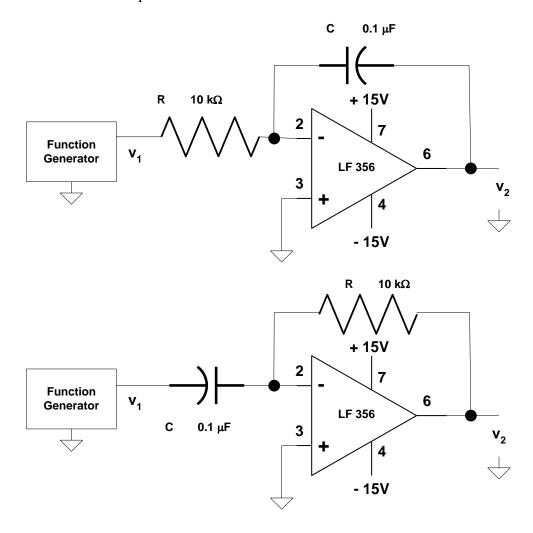
NOTE: This circuit will be used in the compensator of the Magnetic Levitation system. Use another OpAmp to construct the remaining circuits. Remember the bypass capacitors.

8. Active Differentiator (High Pass Filter) and Active Integrator (Low Pass Filter)

These two circuits have been constructed on a circuit board. You will use the circuit board to measure the properties of these circuits.

- a) Derive the transfer function for the two circuits assuming that the voltage v1 is the input and the voltage v0 is the output. Express the transfer functions in terms of R and C and then substitute the values shown and express the transfer function with numerical values.
- b) Derive the differential equations for the circuits again assuming that the voltage v1 is the input and the voltage v0 is the output. What do these differential equations represent (in words)?
- c) Set the function generator to output a low frequency square wave (amplitude \pm 0.5V, frequency 1 Hz). What would you expect the response to be? Sketch the expected response (approximately). Connect the function generator to the BNC terminal on the circuit board. Measure the input voltage signal v1 and the two output voltage signals v0 (at different times) on the oscilloscope. Sketch these responses and compare each measured v0 to your predicted sketch. Save a copy of the traces from the oscilloscope on a floppy disk so that you can print them. Please use the TIFF or BMP format so it can be read on a PC. Print out the traces and turn in the plots to the instructor with the answer sheet. (Note: the circuit response occurs very close to the transition in the square wave. Use the function generator signal to trigger the oscilloscope and set the time base

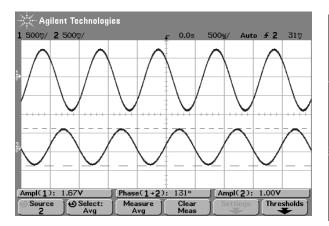
- appropriately. If you press *Autoscale*, the oscilloscope triggers on channel 2 by default. This may not be what you want.)
- d) Derive the frequency responses for the circuits What is the magnitude and phase of the frequency response at $\omega = 100$ rad/sec? At $\omega = 1000$ rad/sec? What is the magnitude and phase at a frequency of 100 Hz?
- e) Plot the complete Bode plot for each circuit for frequencies between 10 rad/sec and 10000 rad/sec. Save plot and attach it to the answer sheet.

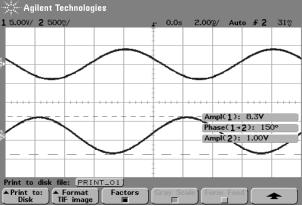


f) Change the function generator to output a ± 0.5V sine wave at 100 Hz. Verify the signal with the oscilloscope. Measure the magnitude and the phase of each v0. Does this agree with your prediction? Measure the magnitude and phase at 1 kHz. What is this value? Save a copy of the traces from the oscilloscope (along with the **Quick Meas** measurements) on a digital camera so that you can print them. (Important Note: for the upper circuit, the signal v0 may saturate. If you do not get signals like shown in the trace

below, try pulling out and adjusting the offset on the function generator so that the output signal is not at the + 15 V or -15 V rail.)

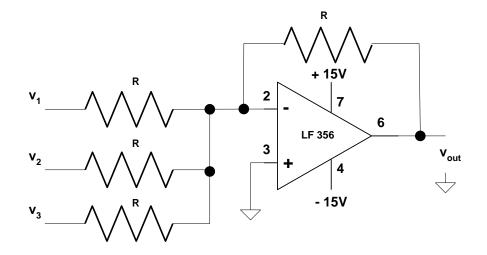
This is illustrated in the following (not for these circuits):

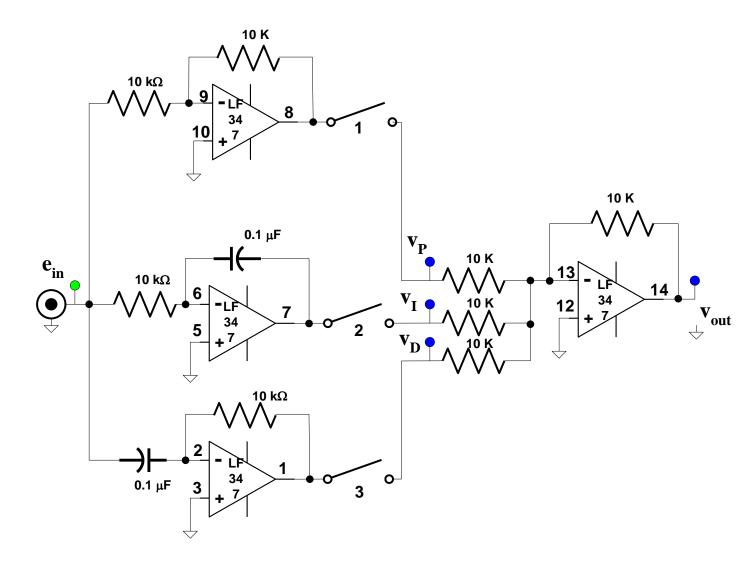




g) From the frequency response (Bode plot), why would you call these circuits an integrator and differentiator, respectively? Why would you call them a low pass filter and high pass filter? Sweep the frequency from the function generator and note how the voltage v0 changes. Describe the response in words.

The circuit on the circuit board contains the circuit from part 7 and these two circuits. Thus it is a circuit with three outputs: one proportional to the input signal, one the derivative of the signal and the third, the integral of the signal? (Note: This is a classic control compensator circuit called a PID (proportional – integral – derivative) compensator. It is often used for analog control purposes. To complete the PID circuit, these three circuits were connected to an adder circuit (which was discussed in lecture and shown below) so that one signal proportional to the sum of these three signals could be produced. (i.e. if all four resistors in the circuit shown are the same value then $\mathbf{e}_{out} = -(\mathbf{v1} + \mathbf{v2} + \mathbf{v_3})$) The complete circuit on the circuit board is shown below.

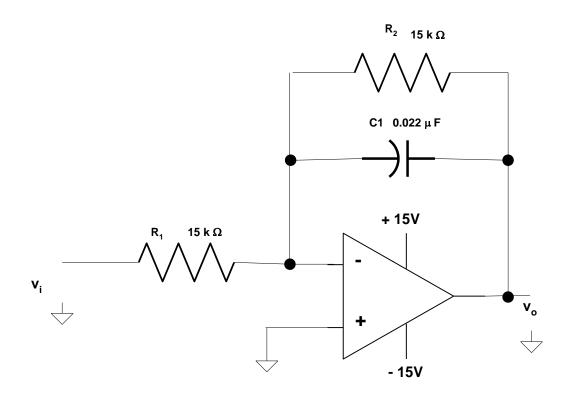




9. First Order Low Pass Filter

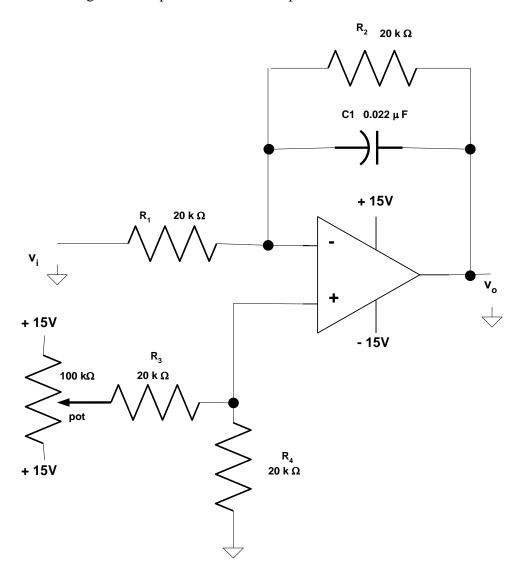
Construct the circuit shown.

- a) Derive the transfer function for the system assuming that the voltage v1 is the input and the voltage v0 is the output. Express the transfer function in terms of R_1 , R_2 and C_1 and then substitute the values shown and express the transfer function with numerical values.
- b) What is the frequency response of this circuit assuming that the OpAmp is ideal? Derive the frequency responses for the circuits What is the magnitude and phase of the frequency response at $\omega = 100$ rad/sec? At $\omega = 1000$ rad/sec? What is the magnitude and phase at a frequency of 100 Hz and 1000 Hz?
- c) Plot the complete Bode plot for the circuit for frequencies between 10 rad/sec and 10000 rad/sec. Save plot and attach it to the answer sheet.
- d) Change the function generator to output a \pm 0.5V sine wave at 100 Hz. Verify the signal with the oscilloscope. Measure the magnitude and the phase of each v0. Does this agree with your prediction? Measure the magnitude and phase at 1 kHz. What is this value?
- e) This circuit is often used as a simple filter. From your frequency response, at what frequency would you expect the filtering action to begin. Verify this frequency using the function generator and oscilloscope.
- f) Comment on the amount of filtering and the phase shift of this circuit as opposed to the one in Part 2. Why do you think that this circuit would be preferred over the one in Part 2? Why would the one in Part 2 be preferred?



Add resistors R_3 , R_4 and the potentiometer to construct the circuit shown.

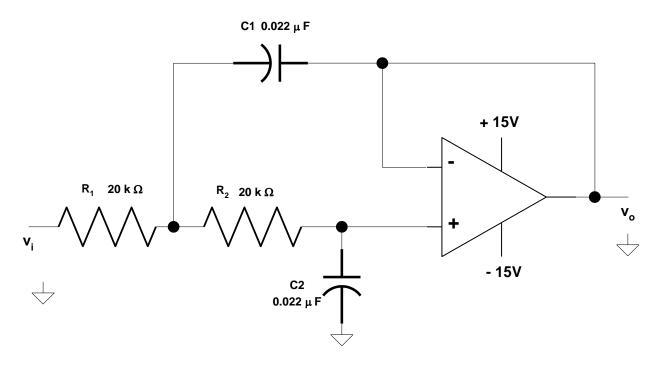
g) With a fixed frequency sine wave from the function generator, note the response of the circuit as the wiper on the potentiometer is varied. (Hint: make sure that the amplifier on the Oscilloscope is DC coupled.) Describe the response in words. This circuit is often used to offset transducer signals for input into a microcomputer.



10. Sallen – Key Filter

Construct the circuit shown.

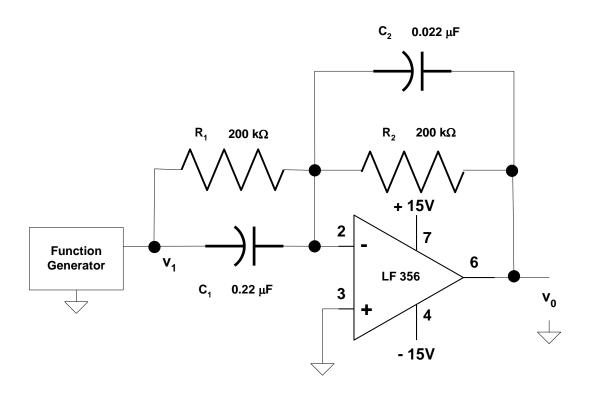
- a) Derive the transfer function for the system assuming that the voltage v1 is the input and the voltage v0 is the output. Express the transfer function in terms of R₁, R₂, C₁ and C₂ and then substitute the values shown and express the transfer function with numerical values. (Hint: assume the OpAmp is ideal. In this case, the output impedance is zero.)
- b) What is the frequency response of this circuit assuming that the OpAmp is ideal? Derive the frequency responses for the circuits What is the magnitude and phase of the frequency response at $\omega = 100$ rad/sec? At $\omega = 1000$ rad/sec? What is the magnitude and phase at a frequency of 100 Hz and 1000 Hz?
- c) Plot the complete Bode plot for the circuit for frequencies between 10 rad/sec and 10000 rad/sec. Save plot and attach it to the answer sheet.
- d) Change the function generator to output a \pm 0.5V sine wave at 100 Hz. Verify the signal with the oscilloscope. Measure the magnitude and the phase of each v0. Does this agree with your prediction? Measure the magnitude and phase at 1 kHz. What is this value?
- e) This circuit is often used as a filter because it produces a large filtering effect with one OpAmp. From your frequency response, at what frequency would you expect the filtering action to begin. Verify this frequency using the function generator and oscilloscope.
- f) Comment on the amount of filtering and the phase shift of this circuit as opposed to the one in Part 9.



11. Lead-Lag Active Circuit

Construct the circuit shown.

- a) Derive the transfer function for the system assuming that the voltage v1 is the input and the voltage v0 is the output. Express the transfer function in terms of R_1 , R_2 , C_1 and C_2 and then substitute the values shown and express the transfer function with numerical values. Compare the transfer function to those derived in parts 3 and 4. Discuss in words how it is the same and how it differs.
- b) What is the frequency response of this circuit assuming that the OpAmp is ideal? Measure and record the response at several frequencies and verify your prediction. Over what range of frequencies should you vary the frequency to see the characteristics of the circuit? You should realize that you could construct a circuit which would produce a similar response using the circuits from parts 3 and 4 and the buffer amplifier from part 6.
- c) This circuit is often used as a control compensator when it is desired to get phase lead at certain frequencies (i.e. to have the output v0 lead the input v1 in phase). Phase lead is often required to make a system stable. From your frequency response, at what frequency would you expect the maximum phase lead to occur? (i.e. at what frequency would you expect the phase of the output v0 lead the input v1 by the greatest amount?) Verify this frequency using the function generator and oscilloscope.



NOTE: This circuit will be used as the Magnetic Levitation compensator.

Part 3: Electromagnetic Levitation (Mag Lev)

Introduction:

In this part of the case study you will use two of the OpAmp circuits from the previous part to form the control compensator for an electromagnetic levitation (Mag Lev) system. OpAmps are an effective means of providing continuous feedback control for mechatronic systems. While most mechatronic systems would use a microcomputer for digital control of systems, continuous (or analog) control often has many advantages. Modern OpAmps are low cost and have many control system performance advantages which cannot be achieved with microcomputers.

The design of the compensator will be discussed in lecture. Your task will be to construct the compensator on the protoboard and demonstrate its operation with the Mag Lev system. If you are able to float the Mag Lev ball below the electromagnet, the task is completed. You should however attempt to reduce the error in ball location by investigating the effect of compensator feedback gain.

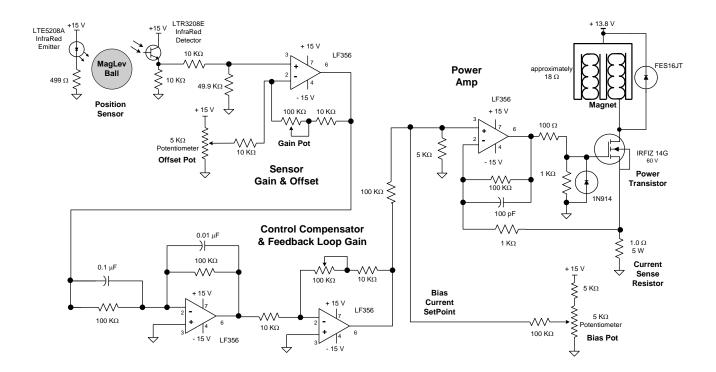
Control of electromagnetic levitation is not simple and you should not be surprised if the system requires several adjustments before levitation is achieved. The system dynamics are both nonlinear and unstable. Levitation cannot be achieved with only permanent magnets; it requires active feedback control. The compensator circuit that you will construct provides both phase lead and feedback gain to make the active feedback control stable. While both phase lead and gain can be provided with one OpAmp (you should think about the circuits in part 2 to see how this can be done), two OpAmps are used to allow for independent adjustment of the gain.

Laboratory Procedure:

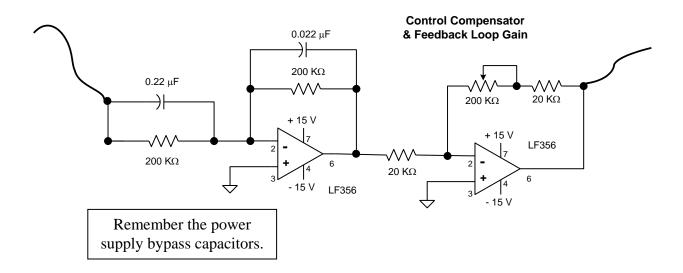
The Mag Lev circuit (shown below) consists of three parts:

- 1. A sensor circuit on the breadboard mounted with the system
- 2. A control compensator that you will build on the protoboard
- 3. A driver (amplifier) on the breadboard mounted with the system

While you do not have to construct either the sensor or driver (to save time), you will have to calibrate them for your system. The sensor circuit has to be calibrated for both zero position and sensitivity. Zero position is the location at which the ball will levitate. Sensitivity is the voltage that the sensor circuit will output for a displacement of the ball away from its zero position (i.e. volts per mm of displacement). The driver circuit has to be calibrated to give the proper bias. Bias is the amount of current which will flow in the electromagnet when the ball is at its zero position. For the Mag Lev system, bias accomplishes two purposes. It provides a force to overcome gravity without requiring a feedback error in the ball position. It also linearizes the system so that linear control theory can be used to design the control compensator. The reasons for calibrating the sensor and driver were discussed in lecture.



The portion of the above circuit that must be constructed on the protoboard is shown below.

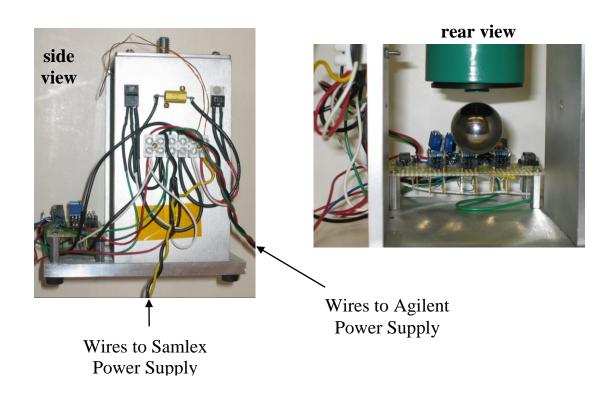


Power must be applied to the Mag Lev system from both the Agilent E3630A DC power supply and the MPJA Higher Current power supply. In the schematic, it should be noted that the power supply is only connected to the Mag Lev coil. Set the voltage to 12 V.

The power supply connections (twisted wires) are as follows:

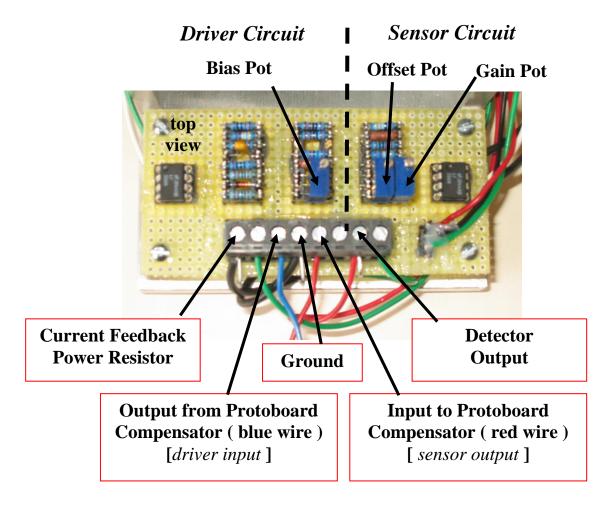
Yellow wire => + terminal of MPJA power supply set to 12 V Black wire => - terminal of MPJA power supply set to 12 V

Red wire => + 15 V Agilent power supply
Green wire => - 15 V Agilent power supply
Black wire => COM Agilent power supply



The sensor and driver electronics are shown below.

Connector Block									
Terminal Description									
1	Current Feedback Power Resistor								
2	Gate of Power Transistor								
3	Output of Protoboard Compensator (blue wire) [driver circuit input]								
4	Ground								
5	Input to Protoboard Compensator (red wire) [sensor circuit output]								
6									
7	InfraRed Detector Output								
8	InfraRed Emitter Input								

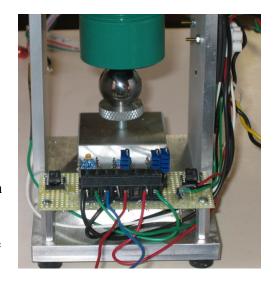


The procedure for levitating the ball is as follows:

- 1. Adjust Agilent Power Supply for 15 V (and tracking). Connect the red-green-black twisted wires and turn on the supply. Remember that the Agilent Power Supply + 15 V must also be connected to your circuit on the protoboard.
- 2. Without the ball present, measure the detector output (terminal 7 on the connector block) using either the oscilloscope or multimeter. It should be in the range of +3 V to +10 V. (Note: a test point (terminal 4 on the connector block) is connected to ground for easier measurement.) Block the emitter or detector with your hand. The voltage should go to ground (0 V). This indicates that the sensor is working.
- 3. Using the calibration test stand, set the ball to approximately 3/8 inch below the electromagnet. You want the ball to be approximately centered under the electromagnet core. If you monitor the detector output (terminal 7), the ball will be approximately centered in the forward-reverse direction when the voltage is a minimum.



- 4. Set the output of the sensor for 0 V. This is done by measuring the sensor output (red wire - terminal 5) and adjusting the sensor offset pot. This will be the position at which the ball will levitate. It is the zero position of the feedback system.
- 5. Move the ball up by turning the screw ½ turn counterclockwise. This will move the ball up approximately ½ mm (actually 1/56 of an inch since it is a ¼ 28 screw). Adjust the sensor gain pot so that the sensor output is between -0.5 and -1.0 V. If you change the pot by several turns, you should recheck zero in step 4 (by turning the screw ½ turn clockwise to return to zero) and then redo step 5.



- 6. Move the ball down ½ mm from zero by turning the screw ½ turn clockwise. Check that the sensor output is between +1.0 and +2.0 V. (It is best if the sensor is symmetric about 0 V. If you have difficulty levitating the ball, you should return to these steps perhaps selecting a different zero position below the electromagnet in step 3.)
- 7. The sensor has a very limited linear range. Most of the difficulties with levitating the ball are due to an improperly adjusted sensor.
- 8. Remove the ball from the system. Connect the yellow-black twisted wires to the Samlex fixed 13.8 V power supply. Ground the blue wire (the driver input - terminal3). You can do this by connecting it to ground on the protoboard or with a clip lead to the COM of the power supply. Turn on the power supply.
- 9. Set the driver bias for 0.3 to 0.4 Amps. This is done by measuring the voltage across the 1.0Ω current sense resistor (terminal 1) and adjusting the driver bias pot. Since the resistor is 1.0Ω , 0.3 to 0.4 Amps corresponds to 0.3 to 0.4 V measured at terminal 1. This will be the current that is applied to the electromagnet when the position sensor is at zero.
- 10. Connect the red and blue wires to the appropriate terminals of the compensator circuit on your protoboard. With the feedback loop gain pot set to approximately $50~k\Omega$, the ball should levitate but some adjustment may be necessary. When you try to position the ball under the electromagnet, put it in the palm of your hand and make sure that your fingers do not block the sensor. If it does not appear to have enough force, you can set the bias current higher by repeating step 8.

- 11. Good luck. When all else fails, return to step 3 remembering to first disconnect the compensator circuit on the protoboard.
- 12. Once the ball is levitated, you can improve the operation of the system by increasing the feedback gain. Measure the sensor output (red wire - terminal 5). It is probably not 0 V. This voltage is therefore the feedback error. If you increase the feedback loop gain by increasing the resistance of the pot in your compensator circuit, you should reduce this error. If you increase the gain too much, the loop will oscillate and the ball will either fall or stick to the electromagnet. It should not be possible to reduce the error to zero.
- 13. Demonstrate levitation to the instructor. Welcome to the world of analog feedback control.



LF155/LF156/LF256/LF257/LF355/LF356/LF357 JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Features

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers

Logarithmic amplifiers

- Photocell amplifiers
- Sample and Hold circuits

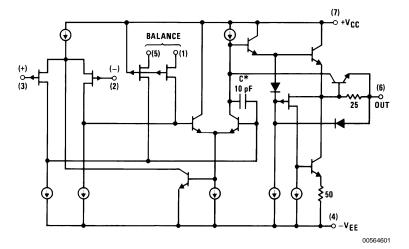
Common Features

- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: $10^{12}\Omega$
- Low input noise current: $0.01 \text{ pA}/\sqrt{\text{Hz}}$
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

		LF155/ LF355	LF156/ LF256/ LF356	LF257/ LF357 (A _V =5)	Units
	Extremely fast settling time to 0.01%	4	1.5	1.5	μs
	Fast slew rate	5	12	50	V/µs
•	Wide gain bandwidth	2.5	5	20	MHz
	Low input noise voltage	20	12	12	nV/√Hz

Simplified Schematic



*3pF in LF357 series.

BI-FET™, BI-FET II™ are trademarks of National Semiconductor Corporation

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF155/6	LF256/7/LF356B	LF355/6/7
Supply Voltage	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
T_{JMAX}			
H-Package	150°C	115°C	115°C
N-Package		100°C	100°C
M-Package		100°C	100°C
Power Dissipation at T _A = 25°C (Notes			
1, 8)			
H-Package (Still Air)	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1000 mW	1000 mW
N-Package		670 mW	670 mW
M-Package		380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}			
H-Package (Still Air)	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W
N-Package		130°C/W	130°C/W
M-Package		195°C/W	195°C/W
(Typical) θ_{JC}			
H-Package	23°C/W	23°C/W	23°C/W
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Soldering Information (Lead Temp.)			
Metal Can Package			
Soldering (10 sec.)	300°C	300°C	300°C
Dual-In-Line Package			
Soldering (10 sec.)	260°C	260°C	260°C
Small Outline Package			
Vapor Phase (60 sec.)		215°C	215°C
Infrared (15 sec.)		220°C	220°C
See AN-450 "Surface Mounting Methods	and Their Effect on P	Product Reliability" for	other methods of
soldering surface mount devices.			
ECD telement			

ESD tolerance

(100 pF discharged through 1.5k Ω) 1000V 1000V 1000V

DC Electrical Characteristics

(Note 3)

Symbol	Parameter	Conditions	LF155/6 LF256/7 LF356B				LF355/6/7			Units		
			Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	1
Vos	Input Offset Voltage	$R_S=50\Omega$, $T_A=25^{\circ}C$		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S=50\Omega$		5			5			5		μV/°C
ΔTC/ΔV _{OS}	Change in Average TC with V _{OS} Adjust	$R_S=50\Omega$, (Note 4)		0.5			0.5			0.5		μV/°C per mV
I _{os}	Input Offset Current	T _J =25°C, (Notes 3, 5)		3	20		3	20		3	50	рА
		T _J ≤T _{HIGH}			20			1			2	nA

DC Electrical Characteristics (Continued)

(Note 3)

Symbol	Parameter	Conditions		LF155/6	6	LF256/7 LF356B			LF355/6/7			Units
			Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
I _B	Input Bias Current	T _J =25°C, (Notes 3, 5)		30	100		30	100		30	200	pА
		T _J ≤T _{HIGH}			50			5			8	nA
R _{IN}	Input Resistance	T _J =25°C		10 ¹²			10 ¹²			10 ¹²		Ω
A _{VOL}	Large Signal Voltage	V _S =±15V, T _A =25°C	50	200		50	200		25	200		V/mV
	Gain	$V_O = \pm 10V$, $R_L = 2k$										
		Over Temperature	25			25			15			V/mV
Vo	Output Voltage Swing	$V_S=\pm 15V, R_L=10k$	±12	±13		±12	±13		±12	±13		V
		$V_S=\pm 15V, R_L=2k$	±10	±12		±10	±12		±10	±12		V
V _{CM}	Input Common-Mode	V _S =±15V	±11	+15.1		±11	±15.1		+10	+15.1		V
	Voltage Range		-	-12		- 1	-12		+10	-12		V
CMRR	Common-Mode		85	100		85	100		80	100		dB
	Rejection Ratio		00	100		65	100		60	100		ub
PSRR	Supply Voltage	(Note 6)	85	100		85	100		80	100		dB
	Rejection Ratio			100			1.00					QD

DC Electrical Characteristics

 $T_A = T_J = 25^{\circ}C, V_S = \pm 15V$

Parameter	LF'	155	LF	355	LF156/256	/257/356B	LF:	356	LF357		Units
	Тур	Max	Тур	Max	Тур	Max	Тур	Max	Тур	Max	Units
Supply Current	2	4	2	4	5	7	5	10	5	10	mA

AC Electrical Characteristics

 $T_A = T_J = 25^{\circ}C, V_S = \pm 15V$

			LF155/355	LF156/256/	LF156/256/356/	LF257/357	
Symbol	Parameter	Conditions		356B	LF356B		Units
			Тур	Min	Тур	Тур	
SR	Slew Rate	LF155/6:	5	7.5	12		V/µs
		A _V =1,					
		LF357: A _V =5				50	V/µs
GBW	Gain Bandwidth Product		2.5		5	20	MHz
t _s	Settling Time to 0.01%	(Note 7)	4		1.5	1.5	μs
e _n	Equivalent Input Noise	R _S =100Ω					
	Voltage	f=100 Hz	25		15	15	nV/√Hz
		f=1000 Hz	20		12	12	nV/√Hz
i _n	Equivalent Input Current	f=100 Hz	0.01		0.01	0.01	pA/√Hz
	Noise	f=1000 Hz	0.01		0.01	0.01	pA/√Hz
C _{IN}	Input Capacitance		3		3	3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum available power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the 25°C P_{dMAX} , whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

Notes for Electrical Characteristics (Continued)

	LF155/156	LF256/257	LF356B	LF355/6/7
Supply Voltage, V _S	±15V ≤ V _S ≤ ±20V	$\pm 15 \text{V} \le \text{V}_{\text{S}} \le \pm 20 \text{V}$	±15V ≤ V _S ±20V	V _S = ±15V
T_A	–55°C ≤ T _A ≤ +125°C	$-25^{\circ}\text{C} \le \text{T}_{\text{A}} \le +85^{\circ}\text{C}$	$0^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +70^{\circ}\text{C}$	$0^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +70^{\circ}\text{C}$
T_{HIGH}	+125°C	+85°C	+70°C	+70°C

and V_{OS} , I_B and I_{OS} are measured at V_{CM} = 0.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

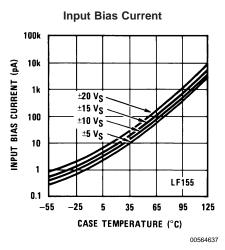
Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

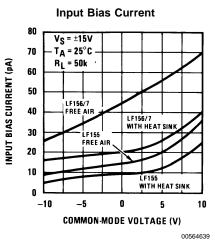
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

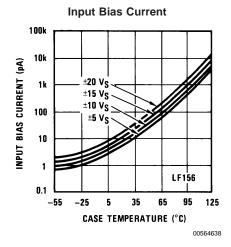
Note 7: Settling time is defined here, for a unity gain inverter connection using $2 k\Omega$ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, $A_V = -5$, the feedback resistor from output to input is $2k\Omega$ and the output step is 10V (See Settling Time Test Circuit).

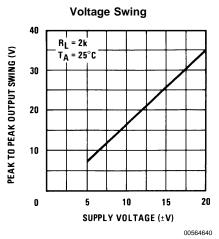
Note 8: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside quaranteed limits

Typical DC Performance Characteristics Curves are for LF155 and LF156 unless otherwise specified.



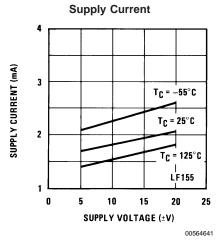




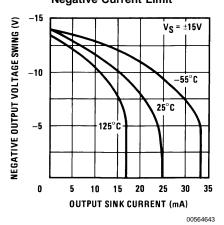


Typical DC Performance Characteristics Curves are for LF155 and LF156 unless otherwise

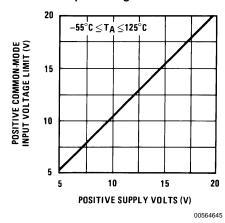
specified. (Continued)



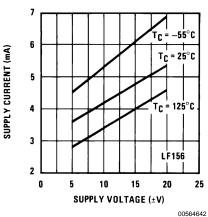
Negative Current Limit



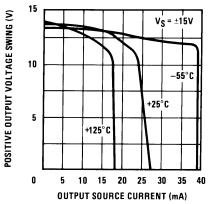
Positive Common-Mode Input Voltage Limit



Supply Current

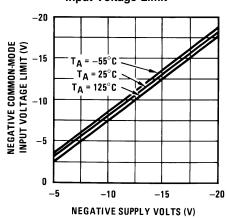


Positive Current Limit



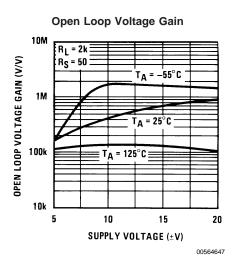
00564644

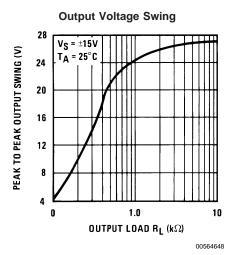
Negative Common-Mode Input Voltage Limit



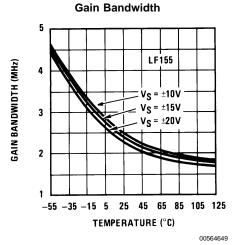
00564646

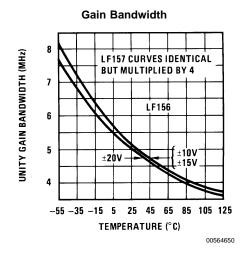
Typical DC Performance Characteristics Curves are for LF155 and LF156 unless otherwise specified. (Continued)

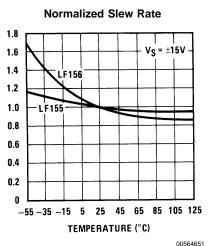


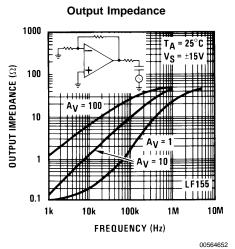


Typical AC Performance Characteristics



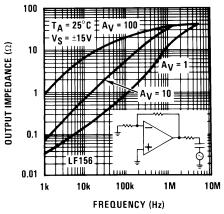






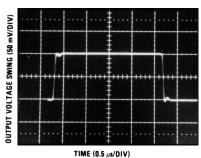
Typical AC Performance Characteristics (Continued)





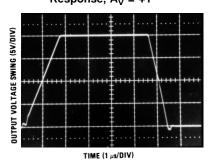
00564653

LF156 Small Signal Pulse Response, $A_V = +1$



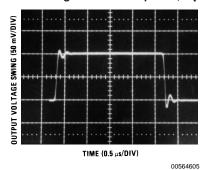
00564606

LF156 Large Signal Puls Response, $A_V = +1$

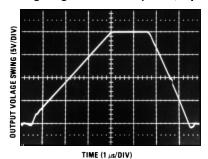


00564609

LF155 Small Signal Pulse Response, $A_V = +1$

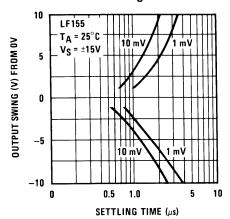


LF155 Large Signal Pulse Response, A_V = +1



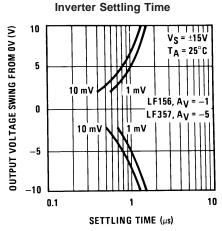
00564608

Inverter Settling Time

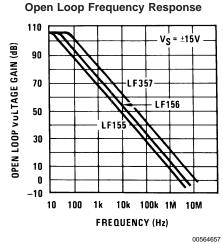


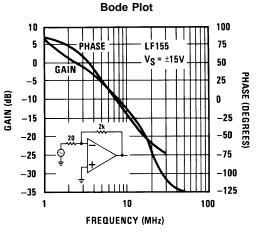
00564655

Typical AC Performance Characteristics (Continued)

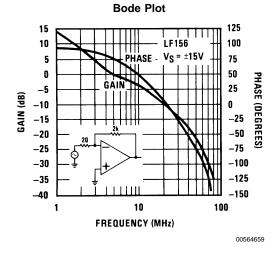


00564656

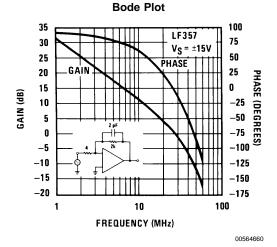


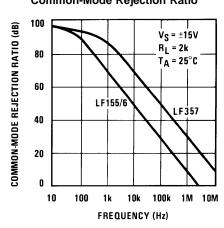


00564658



Common-Mode Rejection Ratio

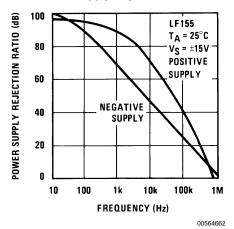




00564661

Typical AC Performance Characteristics (Continued)

Power Supply Rejection Ratio



POWER SUPPLY REJECTION RATIO (dB) 100 1k 100k 1M



FREQUENCY (Hz)

Power Supply Rejection Ratio

T_A = 25°C

V_S = ±15V

10M

POSITIVE SUPPLY

LF156/7

120

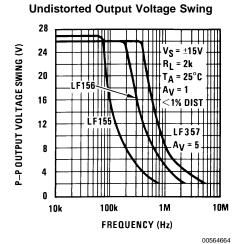
100

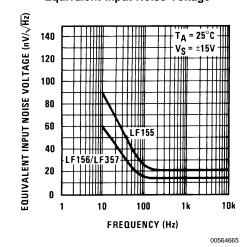
80

60

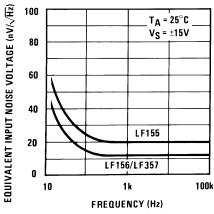
40

20



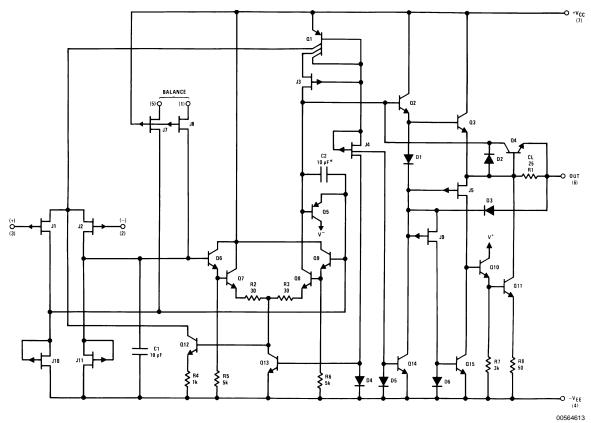


Equivalent Input Noise Voltage (Expanded Scale)



00564666

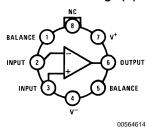
Detailed Schematic



*C = 3pF in LF357 series.

Connection Diagrams (Top Views)

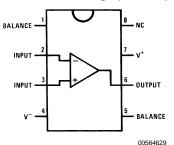
Metal Can Package (H)



Order Number LF155H, LF156H, LF256H, LF257H, LF356BH, LF356H, or LF357H See NS Package Number H08C

*Available per JM38510/11401 or JM38510/11402

Dual-In-Line Package (M and N)



Order Number LF356M, LF356MX, LF355N, or LF356N See NS Package Number M08A or N08E

Application Hints

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a

Application Hints (Continued)

reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

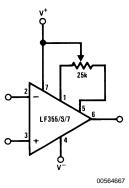
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

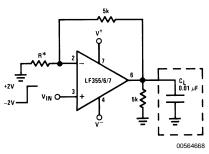
Typical Circuit Connections

Vos Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V⁺
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is $\approx 0.5 \mu V/$ °C/mV of adjustment
- Typical overall drift: 5µV/°C ±(0.5µV/°C/mV of adj.)

Driving Capacitive Loads



* LF155/6 R = 5k

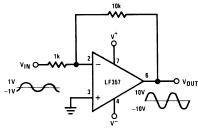
LF357 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \simeq 0.01 \mu F$.

Overshoot ≤ 20%

Settling time $(t_s) \approx 5 \mu s$

LF357. A Large Power BW Amplifier

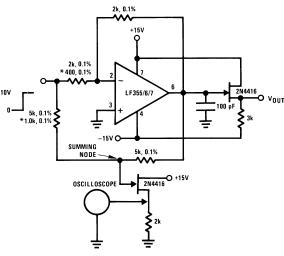


00564615

For distortion \leq 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500kHz.

Typical Applications

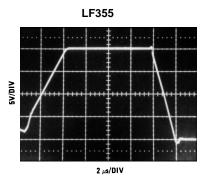
Settling Time Test Circuit



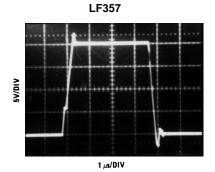
00564616

- Settling time is tested with the LF155/6 connected as unity gain inverter and LF357 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF357

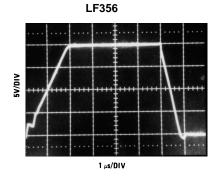
Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



00564617

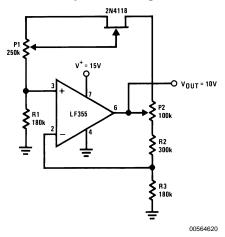


00564619



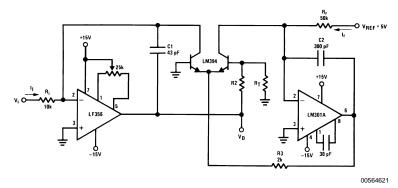
00564618

Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%$ °C
- · All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- · Use LF155 for
 - Low I_B
 - Low drift
 - Low supply current

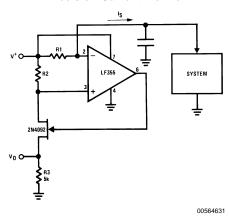
Fast Logarithmic Converter



- Dynamic range: $100\mu\text{A} \le I_i \le 1\text{mA}$ (5 decades), $|V_O| = 1\text{V/decade}$
- Transient response: $3\mu s$ for $\Delta l_i = 1$ decade
- · C1, C2, R2, R3: added dynamic compensation
- \bullet $\,$ $\,$ $\,$ $\,$ $\,$ $\,$ V $_{OS}$ adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

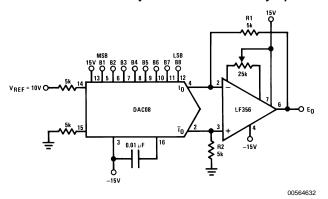
$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF~Ri}}\right] = log~V_i~\frac{1}{R_i I_r}~R2 = 15.7k,~R_T = 1k,~0.3\%/°C~(for~temperature~compensation)$$

Precision Current Monitor



- $V_O = 5 R1/R2 (V/mA of I_S)$
- R1, R2, R3: 0.1% resistors
- Use LF155 for
 - Common-mode range to supply range
 - Low I_B
 - Low V_{OS}
 - Low Supply Current

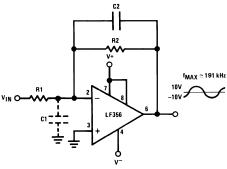
8-Bit D/A Converter with Symmetrical Offset Binary Operation



- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3µs

Eo	В1	B2	В3	В4	B5	В6	В7	В8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
-0.040	0	1	1	1	1	1	1	1	(-) Zero-Scale
-9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

Wide BW Low Noise, Low Drift Amplifier

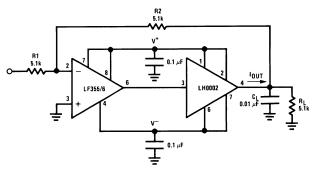


00564670

• Power BW:
$$f_{MAX} = \frac{S_r}{2\pi V_p} \cong 191 \text{ kHz}$$

• Parasitic input capacitance C1 = (3pF for LF155, LF156 and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 = R1 C1.

Boosting the LF156 with a Current Amplifier



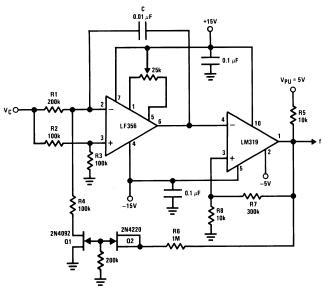
00564673

• $I_{OUT(MAX)} \approx 150 mA$ (will drive $R_L \ge 100 \Omega$)

•
$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}} \text{ V/} \mu \text{s (with C}_{L} \text{ shown)}$$

· No additional phase shift added by the current amplifier

3 Decades VCO

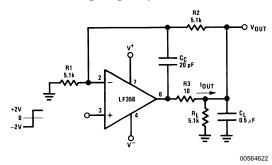


00564624

$$f = \frac{V_{C} (R8 + R7)}{(8 V_{PU} R8 R1) C'} 0 \le V_{C} \le 30V, 10 Hz \le f \le 10 kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

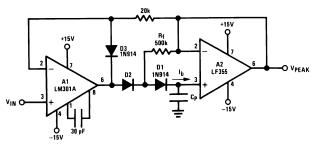
Isolating Large Capacitive Loads



- Overshoot 6%
- t_s 10µs
- When driving large C_L , the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{\rm OUT}}{\Delta T} \,=\, \frac{I_{\rm OUT}}{C_{\rm L}} \,\cong\,\, \frac{0.02}{0.5} \, {\rm V}/\mu {\rm s} \,=\, 0.04 \, {\rm V}/\mu {\rm s} \,\, ({\rm with} \,\, C_{\rm L} \,\, {\rm shown})$$

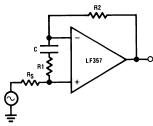
Low Drift Peak Detector



00564623

- By adding D1 and R_f, V_{D1}=0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN}-V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<<1/2\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157



00564675

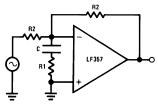
$$R1C \ge \frac{1}{(2\pi) (5 \text{ MHz})}$$

$$R1 = \frac{R2 + R_S}{4}$$

$$A_{V(DC)} = 1$$

$$f_{-3 \text{ dB}} \approx 5 \text{ MHz}$$

Inverting Unity Gain for LF157

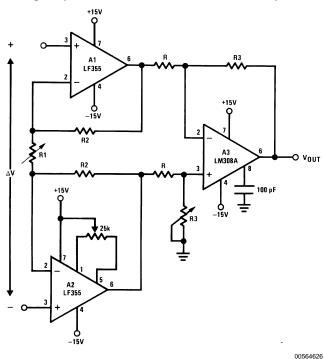


$$R1C \ge \frac{1}{(2\pi) (5 \text{ MHz})}$$

$$R1 = \frac{R2}{4}$$

$$f_{-3 dB} \approx 5 MHz$$

High Impedance, Low Drift Instrumentation Amplifier



•
$$V_{OUT} = \frac{R3}{R} \left[\frac{2R2}{R1} + 1 \right] \Delta V$$
, $V^- + 2V \le V_{IN}$ common-mode $\le V^+$

- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Fast Sample and Hold +15V 2cc pF R1 100k JFET SWITCHES SW2 A1 LF356 LF356 VOUT

0564633

- · Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

$$T_{A} \cong \left[\frac{2R_{ON}, V_{IN}, C_{h}}{S_{r}}\right] \frac{1}{2} \text{ provided that:}$$

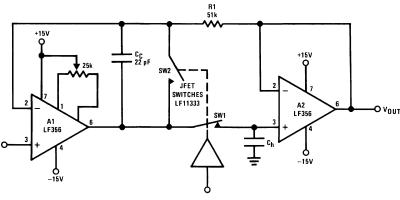
$$V_{IN}C_{h}$$

$$V_{IN}$$
 < $2\pi S_r R_{ON} C_h$ and T_A > $\frac{V_{IN} C_h}{I_{OUT(MAX)}}$, R_{ON} is of SW1

If inequality not satisfied:
$$T_A \simeq \frac{V_{IN}C_h}{20 \text{ mA}}$$

- LF156 develops full S_r output capability for $V_{IN} \ge 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

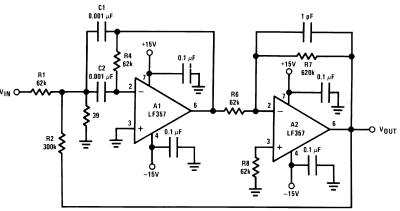
High Accuracy Sample and Hold



00564627

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1.
 No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- · Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
 - Fast settling time
 - Low V_{os}

High Q Band Pass Filter



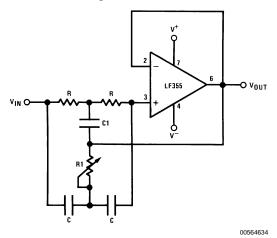
0056462

- By adding positive feedback (R2)
- Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{\overline{Q}}$$

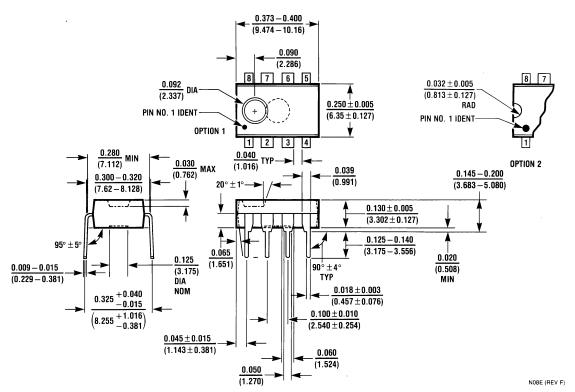
- Clean layout recommended
- Response to a 1Vp-p tone burst: 300µs

High Q Notch Filter



- $2R1 = R = 10M\Omega$ 2C = C1 = 300pF
- · Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120 \text{ Hz}, \text{ notch} = -55 \text{ dB}, Q > 100$
- Use LF155 for
 - Low I_B
 - Low supply current

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N) Order Number LF356N NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Europe

Fax: +49 (0) 180-530 85 86 Email: europe.support@nsc.com Deutsch Tel: +49 (0) 69 9508 6208 English Tel: +44 (0) 870 24 0 2171

English Tel: +44 (0) 870 24 0 2171 Français Tel: +33 (0) 1 41 91 8790 National Semiconductor Asia Pacific Customer Response Group Tel: 65-2544466 Fax: 65-2504466 Email: ap.support@nsc.com National Semiconductor Japan Ltd. Tel: 81-3-5639-7560 Fax: 81-3-5639-7507



LF147/LF347

Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

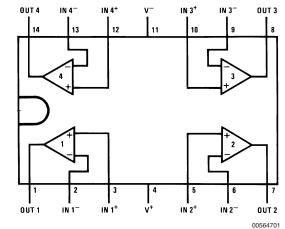
Internally trimmed offset voltage:Low input bias current:	5 mV max 50 pA
■ Low input noise current:	0.01 pA/√Hz
Wide gain bandwidth:High slew rate:	4 MHz 13 V/μs
Low supply current:High input impedance:	7.2 mA 10 ¹² Ω
■ Low total harmonic distortion:	≤0.02%
Low 1/f noise corner:Fast settling time to 0.01%:	50 Hz 2 μs

Simplified Schematic

VCC O VO VO INTERNALLY TRIMMED TRIMMED O0564713

Connection Diagram

Dual-In-Line Package



Note 1: LF147 available as per JM38510/11906.

Top View

Order Number LF147J, LF147J-SMD, LF347M, LF347BN, LF347N, LF147J/883, or JL147 BCA (Note 1)
See NS Package Number J14A, M14A or N14A

BI-FET II™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range	±19V	±15V
(Note 3)		
Output Short Circuit	Continuous	Continuous
Duration (Note 4)		
Power Dissipation	900 mW	1000 mW
(Notes 5, 11)		
T _j max	150°C	150°C
θ_{jA}		
Ceramic DIP (J) Package		70°C/W
Plastic DIP (N) Package		75°C/W
Surface Mount Narrow (M)		100°C/W
Surface Mount Wide (WM)		85°C/W

	LF147	LF347B/LF347
Operating Temperature	(Note 6)	(Note 6)

Range

Storage Temperature

Range $-65^{\circ}\text{C} \le \text{T}_{A} \le 150^{\circ}\text{C}$

Lead Temperature

(Soldering, 10 sec.) 260°C 260°C

Soldering Information

Dual-In-Line Package

Soldering (10 seconds) 260°C

Small Outline Package

Vapor Phase (60 seconds) 215°C Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering

surface mount devices.

ESD Tolerance (Note 12) 900V

DC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions		LF147			LF347E	3		LF347		Units
			Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
V _{os}	Input Offset Voltage	R _S =10 kΩ, T _A =25°C		1	5		3	5		5	10	mV
		Over Temperature			8			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset	R _S =10 kΩ		10			10			10		μV/°C
	Voltage											
I _{os}	Input Offset Current	T _j =25°C, (Notes 7, 8)		25	100		25	100		25	100	pА
		Over Temperature			25			4			4	nA
I _B	Input Bias Current	T _j =25°C, (Notes 7, 8)		50	200		50	200		50	200	pА
		Over Temperature			50			8			8	nA
R _{IN}	Input Resistance	T _j =25°C		10 ¹²			10 ¹²			10 ¹²		Ω
A _{VOL}	Large Signal Voltage Gain	V _S =±15V, T _A =25°C	50	100		50	100		25	100		V/mV
		$V_O=\pm 10V$, $R_L=2 k\Omega$										
		Over Temperature	25			25			15			V/mV
Vo	Output Voltage Swing	$V_S=\pm 15V$, $R_L=10 \text{ k}\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
V _{CM}	Input Common-Mode Voltage	V _S =±15V	±11	+15		±11	+15		±11	+15		V
	Range			-12			-12			-12		V
CMRR	Common-Mode Rejection Ratio	R _S ≤10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 9)	80	100		80	100		70	100		dB
Is	Supply Current			7.2	11		7.2	11		7.2	11	mA

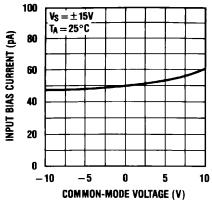
AC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions		LF147	,	ı	LF347E	3		LF347		Units
			Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
	Amplifier to Amplifier Coupling	T _A =25°C,		-120			-120			-120		dB
		f=1 Hz-20 kHz										
		(Input Referred)										
SR	Slew Rate	V _S =±15V, T _A =25°C	8	13		8	13		8	13		V/µs
GBW	Gain-Bandwidth Product	V _S =±15V, T _A =25°C	2.2	4		2.2	4		2.2	4		MHz
e _n	Equivalent Input Noise Voltage	$T_A=25$ °C, $R_S=100\Omega$,		20			20			20		nV/√ Hz
		f=1000 Hz										
i _n	Equivalent Input Noise Current	T _j =25°C, f=1000 Hz		0.01			0.01			0.01		pA/√ Hz
THD	Total Harmonic Distortion	A _V =+10, R _L =10k,		<0.02			<0.02			<0.02		%
		V _O =20 Vp-p, BW=20 Hz-20 kHz										

- Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.
- Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
- **Note 4:** Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
- Note 5: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA} .
- Note 6: The LF147 is available in the military temperature range $-55^{\circ}C \le T_{A} \le 125^{\circ}C$, while the LF347B and the LF347 are available in the commercial temperature range $0^{\circ}C \le T_{A} \le 70^{\circ}C$. Junction temperature can rise to T_{i} max = 150°C.
- Note 7: Unless otherwise specified the specifications apply over the full temperature range and for $V_S=\pm20V$ for the LF147 and for $V_S=\pm15V$ for the LF347B/LF347. V_{OS} , I_B , and I_{OS} are measured at $V_{CM}=0$.
- Note 8: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_j = T_A + \theta_{jA}$ P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
- Note 9: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5V$ to $\pm 15V$ for the LF347 and LF347B and from $V_S = \pm 20V$ to $\pm 5V$ for the LF147.
- Note 10: Refer to RETS147X for LF147D and LF147J military specifications.
- Note 11: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.
- Note 12: Human body model, 1.5 k Ω in series with 100 pF.

Typical Performance Characteristics





TEMPERATURE (°C)

0 25 50 75

Input Bias Current

100k

10k

1k

100

10

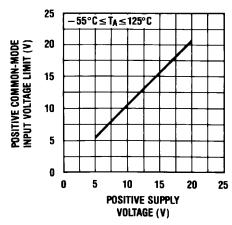
-50 - 25

INPUT BIAS CURRENT (pA)

 $V_{CM} = 0$

 $V_S = \pm 15V$

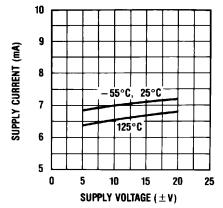




00564717

100 125

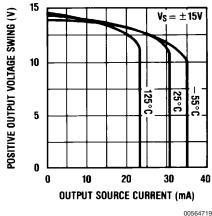
00564715



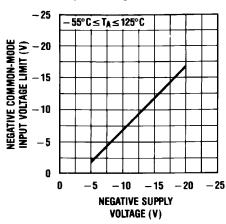
Supply Current

00564716

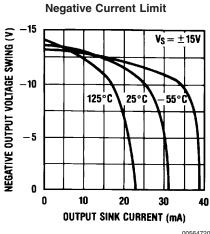
Positive Current Limit

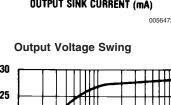


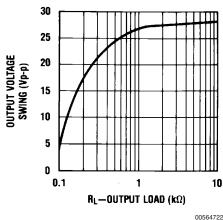


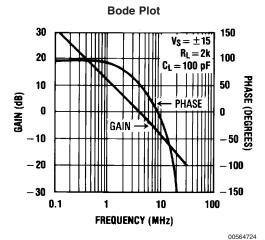


Typical Performance Characteristics (Continued)

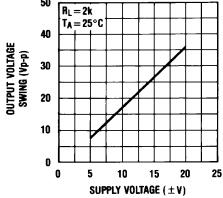






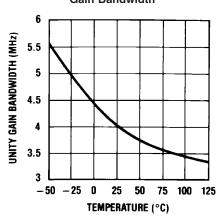


Output Voltage Swing RL=2k



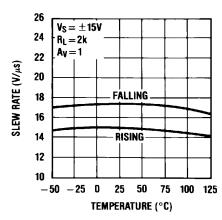
00564721

Gain Bandwidth

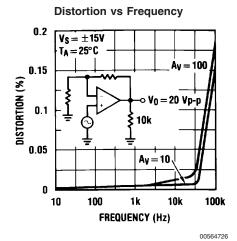


00564723

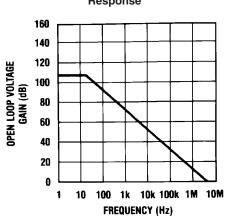
Slew Rate



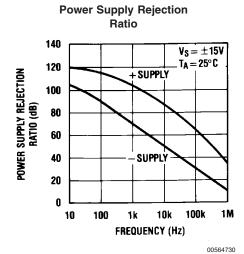
Typical Performance Characteristics (Continued)



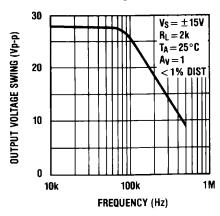
Open Loop Frequency Response



00564728

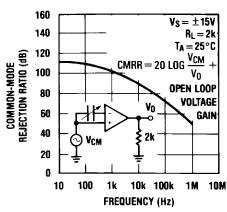


Undistorted Output Voltage Swing



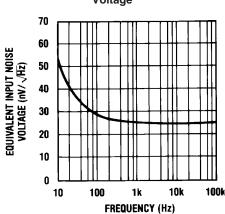
00564727

Common-Mode Rejection



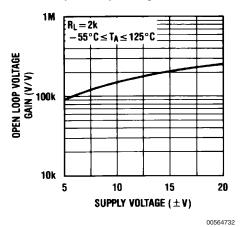
00564729

Equivalent Input Noise Voltage

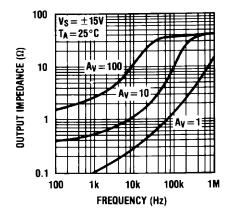


Typical Performance Characteristics (Continued)

Open Loop Voltage Gain

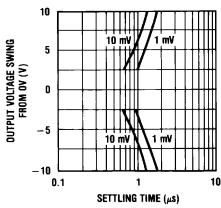


Output Impedance



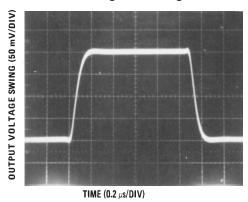
00564733

Inverter Settling Time

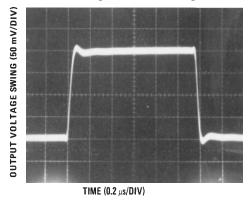


Pulse Response $R_L=2 \text{ k}\Omega, C_L=10 \text{ pF}$

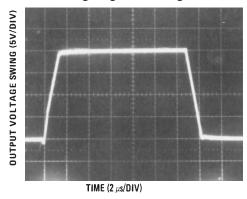
Small Signal Inverting



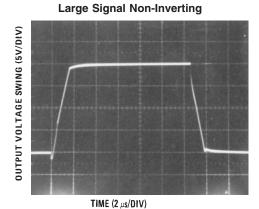
Small Signal Non-Inverting



Large Signal Inverting

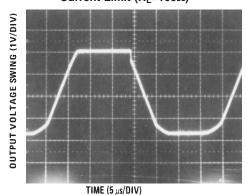


005647



0056470

Current Limit (R_L=100Ω)



0056470

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages

should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 4.5 \text{V}$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

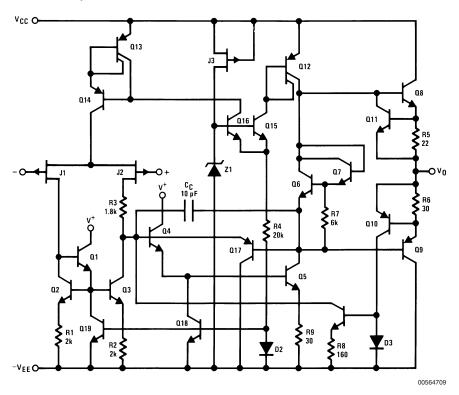
The LF147 will drive a 2 k Ω load resistance to $\pm 10V$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

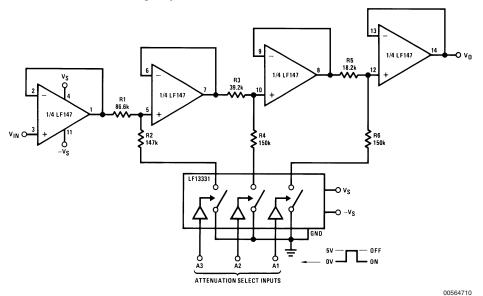
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

Digitally Selectable Precision Attenuator

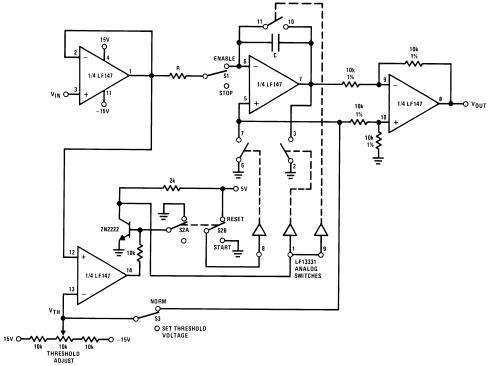


All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
 No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

A 1	A2	А3	Vo
			Attenuation
0	0	0	0
0	0	1	–1 dB
0	1	0	–2 dB
0	1	1	-3 dB
1	0	0	-4 dB
1	0	1	–5 dB
1	1	0	−6 dB
1	1	1	–7 dB

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



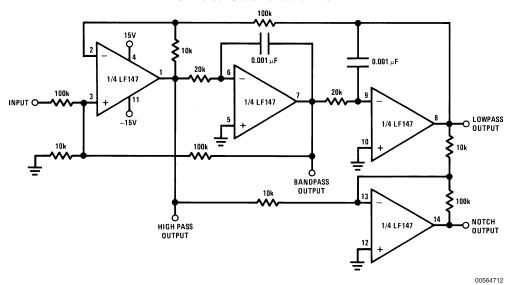
0564711

 \bullet V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC} \int_0^t (V_{IN} - V_{TH}) dt$$

- Output starts when V_{IN}≥V_{TH}
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Universal State Variable Filter



For circuit shown:

 $f_0=3$ kHz, $f_{NOTCH}=9.5$ kHz

 $\Omega = 3.4$

Passband gain:

Highpass — 0.1

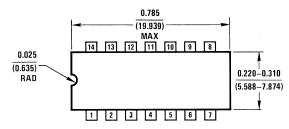
Bandpass — 1

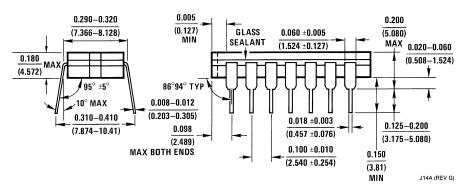
Lowpass — 1

Notch — 10

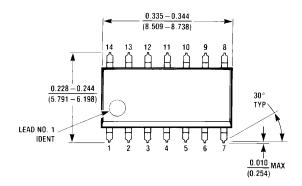
- f_oxQ≤200 kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

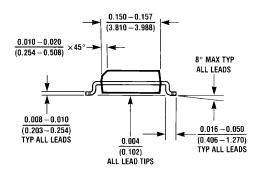
Physical Dimensions inches (millimeters) unless otherwise noted

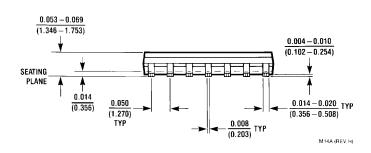




Ceramic Dual-In-Line Package (J)
Order Number LF147J, LM147J-SMD or LF147J/883
NS Package Number J14A

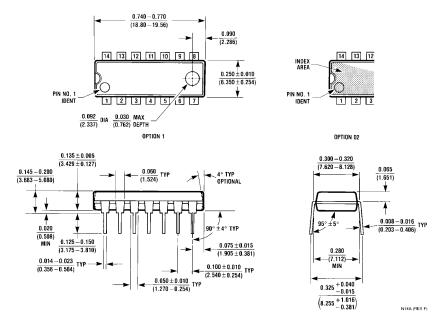






S.O. Package (M)
Order Number LF347M or LF347MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N) Order Number LF347BN or LF347N NS Package Number N14A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



National Semiconductor Americas Customer Support Center

Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor Europe Customer Support Center Fax: +49 (0) 180-530 85 86

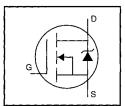
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center Email: ap.support@nsc.com National Semiconductor Japan Customer Support Center Fax: 81-3-5639-7507 Email: jpn.feedback@nsc.com Tel: 81-3-5639-7560



HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- 175°C Operating Temperature
- Dynamic dv/dt Rating
- Low Thermal Resistance

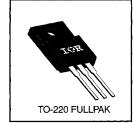


 $V_{DSS} = 60V$ $R_{DS(on)} = 0.20\Omega$ $I_{D} = 8.0A$

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



Absolute Maximum Ratings

	Parameter	Max.	Units
lp @ T _C ≈ 25°C	Continuous Drain Current, VGS @ 10 V	8.0	
I _D @ T _C = 100°C	Continuous Drain Current, VGS @ 10 V	5.7	Α
[DM	Pulsed Drain Current ①	32	
P _D @ T _C = 25°C	Power Dissipation	27	W
	Linear Derating Factor	0.18	W/°C
V _{GS}	Gate-to-Source Voltage	±20	V
Eas	Single Pulse Avalanche Energy ②	47	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
TJ	Operating Junction and	-55 to +175	
T _{STG}	Storage Temperature Range		∘c
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Тур.	Max.	Units
Rыc	Junction-to-Case			5.5	°C/W
Bala	Junction-to-Ambient		_	65	-0/00



Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	60	_	_	V	V _{GS} =0V, I _D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	_	0.63	_	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	_	_	0.20	Ω	V _{GS} =10V, I _D =4.8A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	_	4.0	٧	V _{DS} =V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	2.2	_	_	S	V _{DS} =25V, I _D =4.8A ⊕
Ipss	Drain-to-Source Leakage Current	_		25	μΑ	V _{DS} =60V, V _{GS} =0V
SSUI	Dialif-to-Cource Leakage Outrent			250	μΛ	V _{DS} =48V, V _{GS} =0V, T _J =150°C
I _{GSS}	Gate-to-Source Forward Leakage			100	nA	V _{GS} =20V
IGSS	Gate-to-Source Reverse Leakage			-100		V _{GS} =-20V
Qg	Total Gate Charge		_	11		I _D =10A
Q _{gs}	Gate-to-Source Charge			3.1	nC	V _{DS} =48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	<u> </u>	_	5.8		V _{GS} =10V See Fig. 6 and 13 ®
t _{d(on)}	Turn-On Delay Time	<u></u>	10			V _{DD} =30V
t _r	Rise Time		50		ns	I _D =10A
t _{d(off)}	Turn-Off Delay Time	<u> </u>	13		110	$R_{G}=24\Omega$
tf	Fall Time		19	_		R _D =2.7Ω See Figure 10 @
L _D	Internal Drain Inductance	_	4.5		nН	Between lead, 6 mm (0.25in.)
Ls	Internal Source Inductance	_	7.5	_	''''	from package and center of die contact
Ciss	Input Capacitance		300	_		V _{GS} =0V
Coss	Output Capacitance		160		рF	V _{DS} = 25V
Crss	Reverse Transfer Capacitance	_	29			f=1.0MHz See Figure 5
С	Drain to Sink Capacitance	_	12		рF	f=1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Тур.	Max.	Units	Test Conditions
ls	Continuous Source Current (Body Diode)	_	_	8.0		MOSFET symbol showing the
Ism	Pulsed Source Current (Body Diode) ①		_	32	A	integral reverse p-n junction diode.
V _{SD}	Diode Forward Voltage	_ _	_	1.6	V	T _J =25°C, I _S =8.0A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time		70	140	ns	T _J =25°C, I _F =10A
Qrr	Reverse Recovery Charge	_	0.20	0.40	μC	di/dt=100A/μs ④
ton	Forward Turn-On Time	Intrinsi	turn-or	time is	neglegib	le (turn-on is dominated by Ls+LD)

Notes:

- Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ③ I_{SD} ≤10A, di/dt≤90A/ μ s, V_{DD} ≤ $V_{(BR)DSS}$, T_{J} ≤175°C
- \$ t=60s, f=60Hz

- $V_{DD}=25V$, starting T_J=25°C, L=856μH R_G=25Ω, I_{AS}=8.0A (See Figure 12)
- 4 Pulse width \leq 300 μ s; duty cycle \leq 2%.

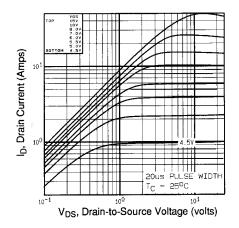


Fig 1. Typical Output Characteristics, T_C=25°C

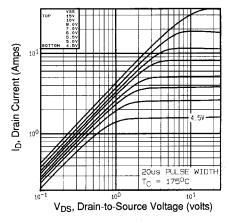


Fig 2. Typical Output Characteristics, T_C=175°C

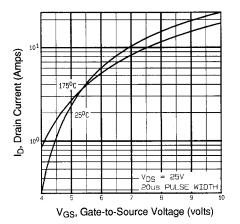


Fig 3. Typical Transfer Characteristics

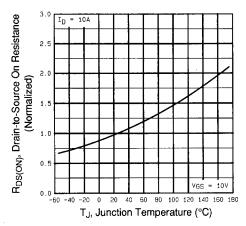


Fig 4. Normalized On-Resistance Vs. Temperature

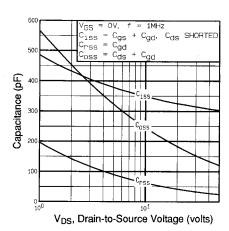


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

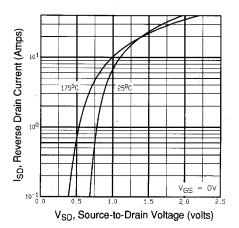


Fig 7. Typical Source-Drain Diode Forward Voltage

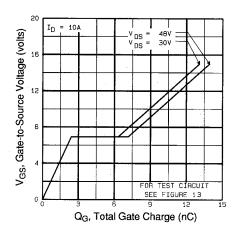


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

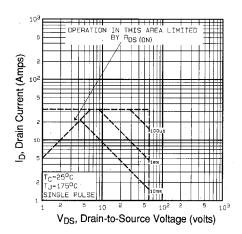


Fig 8. Maximum Safe Operating Area

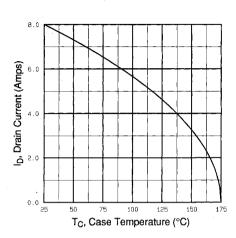


Fig 9. Maximum Drain Current Vs. Case Temperature

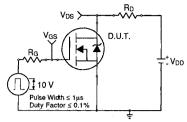


Fig 10a. Switching Time Test Circuit

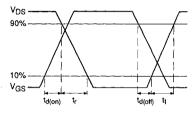


Fig 10b. Switching Time Waveforms

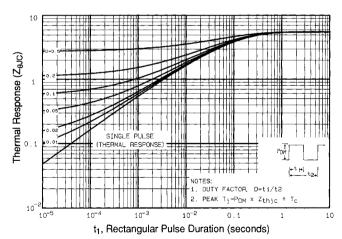


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

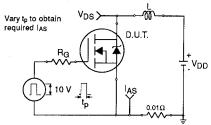


Fig 12a. Unclamped Inductive Test Circuit

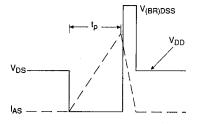


Fig 12b. Unclamped Inductive Waveforms

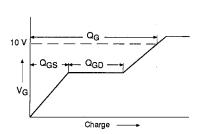


Fig 13a. Basic Gate Charge Waveform

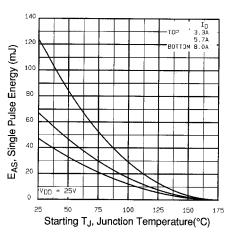


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

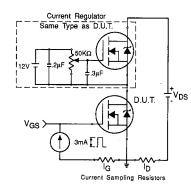


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit - See page 1505

Appendix B: Package Outline Mechanical Drawing - See page 1510

Appendix C: Part Marking Information – See page 1517



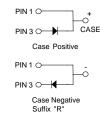


FES16AT - FES16JT

Features

- Low forward voltage drop.
- High surge current capacity.
- High current capability.
- High reliability.





Fast Rectifiers (Glass Passivated)

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value								Units
		16AT	16BT	16CT	16DT	16FT	16GT	16HT	16JT	
V_{RRM}	Maximum Repetitive Reverse Voltage	50	100	150	200	300	400	500	600	V
I _{F(AV)}	Average Rectified Forward Current, .375 " lead length @ T _A = 100°C		16							Α
I _{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave		250							
T _{sta}	Storage Temperature Range		-65 to +150							V
T _J	Operating Junction Temperature				-65 to	+150				pF

^{*}These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_{D}	Power Dissipation	7.81	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	16	°C/W
$R_{\theta JL}$	Thermal Resistance, Junction to Lead	1.2	°C/W

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Device							Units	
		16AT	16BT	16CT	16DT	16FT	16GT	16HT	16JT	1
V_{F}	Forward Voltage @ 8.0A	0.95				1.3		1.5		V
t _{rr}	Reverse Recovery Time	35				50				
	$I_F = 0.5 \text{ A}, I_R = 1.0 \text{ A}, I_{RR} = 0.25 \text{ A}$									ns
I _R	Reverse Current @ rated V _R									
	T _A = 25°C	10 500						μΑ		
	T _A = 100°C							μΑ		
Ст	Total Capacitance	170				170 145		15	pF	
	$V_R = 4.0. f = 1.0 MHz$							+0		

Typical Characteristics

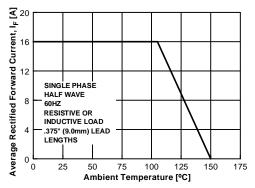


Figure 1. Forward Current Derating Curve

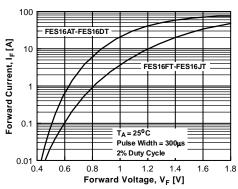


Figure 3. Forward Voltage Characteristics

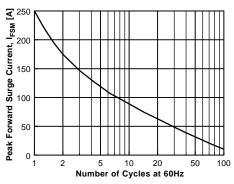


Figure 2. Non-Repetitive Surge Current

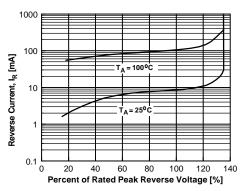


Figure 4. Reverse Current vs Reverse Voltage

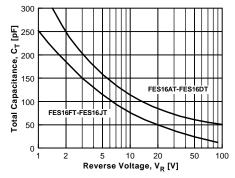
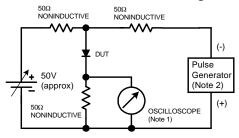
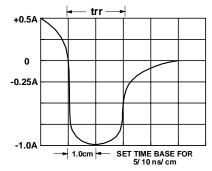


Figure 5. Total Capacitance





Reverse Recovery Time Characterstic and Test Circuit Diagram