National Semiconductor

December 2001

LF155/LF156/LF256/LF257/LF355/LF356/LF357 JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Features

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance — very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

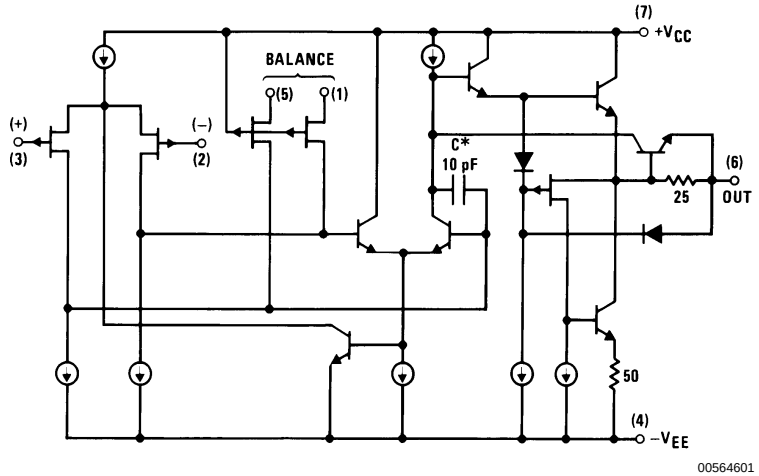
Common Features

- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: $10^{12}\Omega$
- Low input noise current: $0.01\ pA/\sqrt{Hz}$
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

	LF155/ LF355	LF156/ LF256/ LF356	LF257/ LF357 (A_V=5)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	µs
■ Fast slew rate	5	12	50	V/µs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

Simplified Schematic



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*3pF in LF357 series.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF155/6	LF256/7/LF356B	LF355/6/7
Supply Voltage	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
T_{JMAX}			
H-Package	150˚C	115˚C	115˚C
N-Package		100˚C	100˚C
M-Package		100˚C	100˚C
Power Dissipation at T_A = 25˚C (Notes 1, 8)			
H-Package (Still Air)	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1000 mW	1000 mW
N-Package		670 mW	670 mW
M-Package		380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}			
H-Package (Still Air)	160˚C/W	160˚C/W	160˚C/W
H-Package (400 LF/Min Air Flow)	65˚C/W	65˚C/W	65˚C/W
N-Package		130˚C/W	130˚C/W
M-Package		195˚C/W	195˚C/W
(Typical) θ_{JC}			
H-Package	23˚C/W	23˚C/W	23˚C/W
Storage Temperature Range	−65˚C to +150˚C	−65˚C to +150˚C	−65˚C to +150˚C
Soldering Information (Lead Temp.)			
Metal Can Package			
Soldering (10 sec.)	300˚C	300˚C	300˚C
Dual-In-Line Package			
Soldering (10 sec.)	260˚C	260˚C	260˚C
Small Outline Package			
Vapor Phase (60 sec.)		215˚C	215˚C
Infrared (15 sec.)		220˚C	220˚C
See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.			
ESD tolerance			
(100 pF discharged through 1.5kΩ)	1000V	1000V	1000V

DC Electrical Characteristics

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25˚C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		5			5			5		µV/˚C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (Note 4)		0.5			0.5			0.5		µV/˚C per mV
I_{OS}	Input Offset Current	T_J=25˚C, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_J \leq T_{HIGH}$			20			1			2	nA

DC Electrical Characteristics (Continued)

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_B	Input Bias Current	T_J=25˚C, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	T_J=25˚C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25˚C	50	200		50	200		25	200		V/mV
		V_O=±10V, R_L=2k										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k	±12	±13		±12	±13		±12	±13		V
		V_S=±15V, R_L=2k	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics

$T_A = T_J = 25˚C$, $V_S = ±15V$

Parameter	LF155		LF355		LF156/256/257/356B		LF356		LF357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	10	mA

AC Electrical Characteristics

$T_A = T_J = 25˚C$, $V_S = ±15V$

Symbol	Parameter	Conditions	LF155/355	LF156/256/ 356B	LF156/256/356/ LF356B	LF257/357	Units
			Typ	Min	Typ	Typ	
SR	Slew Rate	LF155/6: A_V=1,	5	7.5	12		V/µs
		LF357: A_V=5				50	V/µs
GBW	Gain Bandwidth Product		2.5		5	20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5	1.5	µs
e_n	Equivalent Input Noise Voltage	R_S=100Ω					
		f=100 Hz	25		15	15	$nV/\sqrt{Hz}$
		f=1000 Hz	20		12	12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f=100 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
		f=1000 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3	3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{JMAX}-T_A)/\theta_{JA}$ or the 25˚C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

Notes for Electrical Characteristics (Continued)

	LF155/156	LF256/257	LF356B	LF355/6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55^\circ C \le T_A \le +125^\circ C$	$-25^\circ C \le T_A \le +85^\circ C$	$0^\circ C \le T_A \le +70^\circ C$	$0^\circ C \le T_A \le +70^\circ C$
T_{HIGH}	$+125^\circ C$	$+85^\circ C$	$+70^\circ C$	$+70^\circ C$

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5µV/˚C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

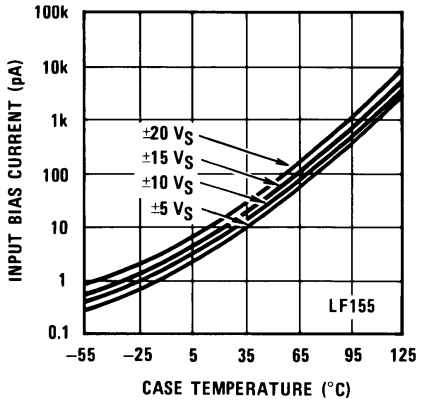
Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

Note 8: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical DC Performance Characteristics

Curves are for LF155 and LF156 unless otherwise specified.

Input Bias Current



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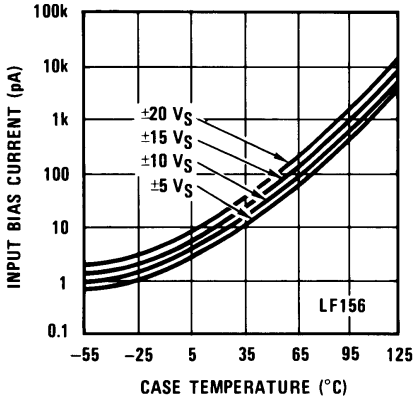
Input Bias Current



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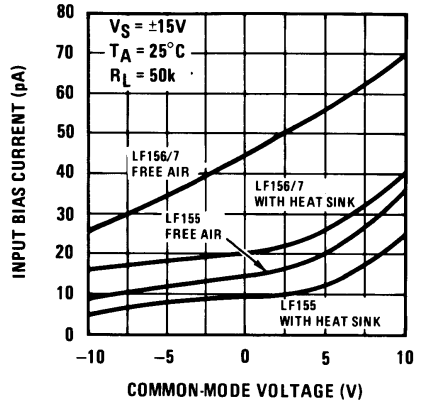
Input Bias Current



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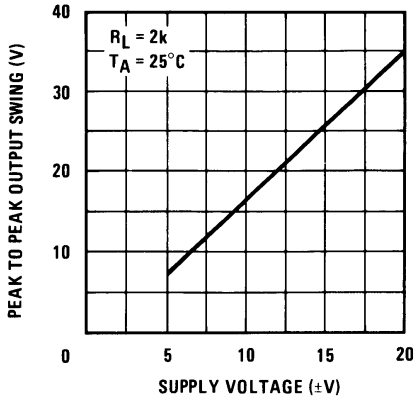
Voltage Swing



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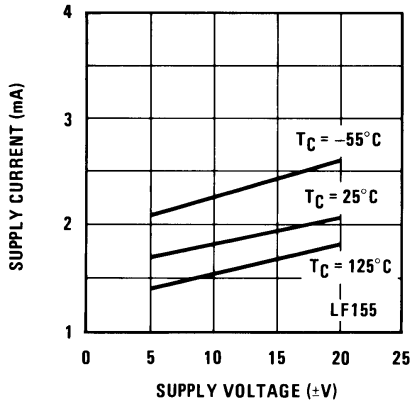
Typical DC Performance Characteristics

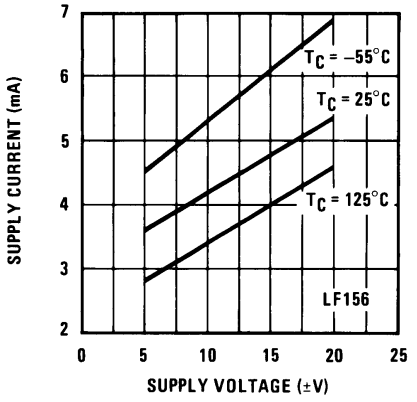
Curves are for LF155 and LF156 unless otherwise specified. (Continued)

Supply Current



00564641

Supply Current



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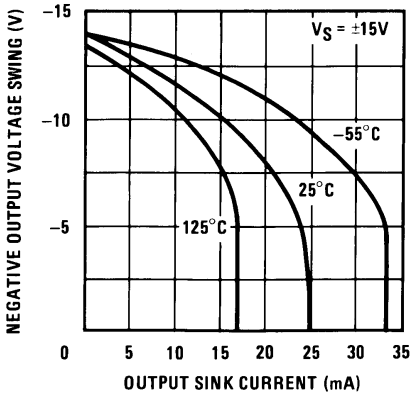
Negative Current Limit



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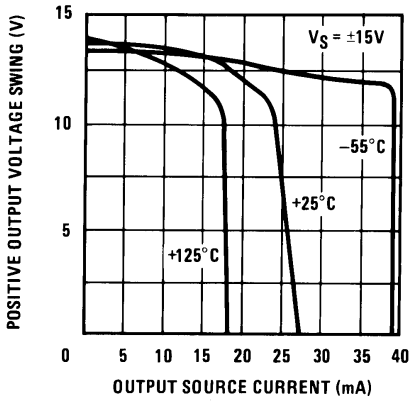
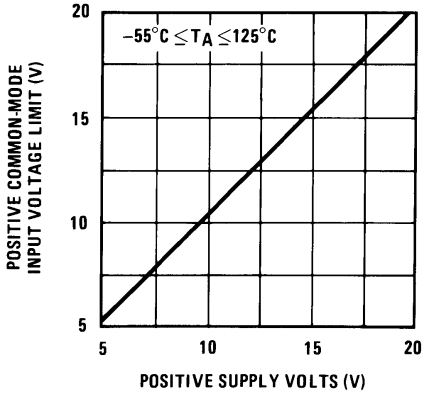
Positive Current Limit



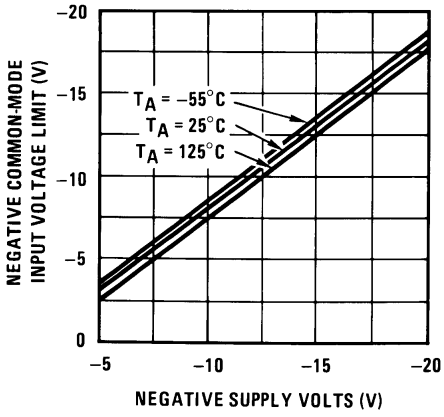
00564644

Positive Common-Mode Input Voltage Limit



00564645

Negative Common-Mode Input Voltage Limit



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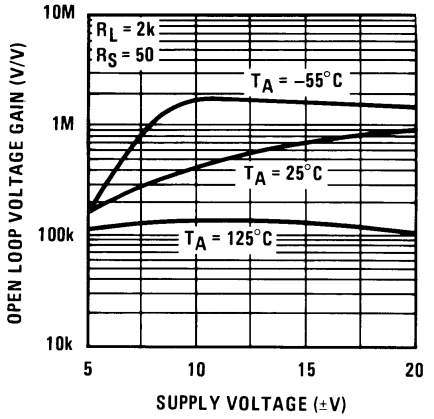
Typical DC Performance Characteristics

Curves are for LF155 and LF156 unless otherwise specified. (Continued)

Open Loop Voltage Gain



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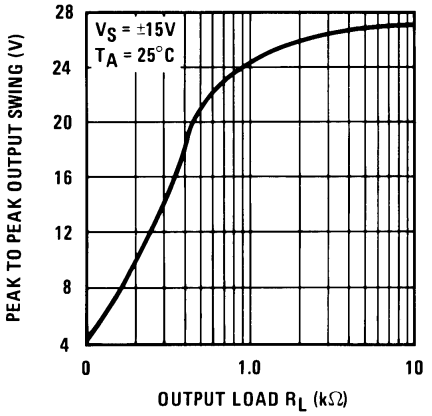
Output Voltage Swing



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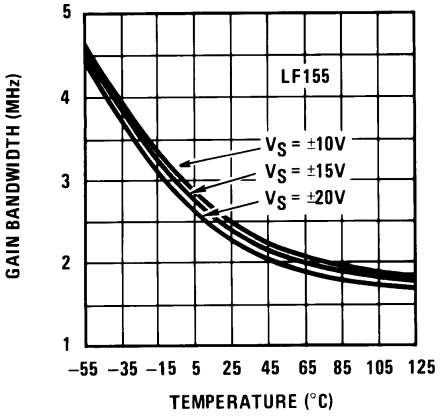
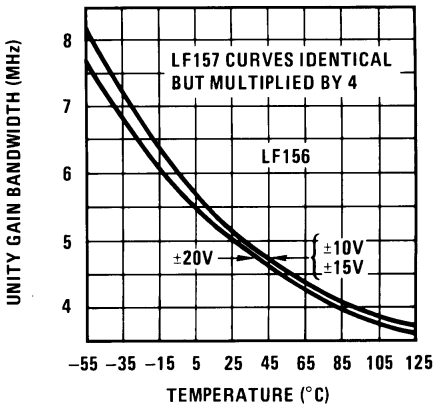
Typical AC Performance Characteristics

Gain Bandwidth



00564649

Gain Bandwidth



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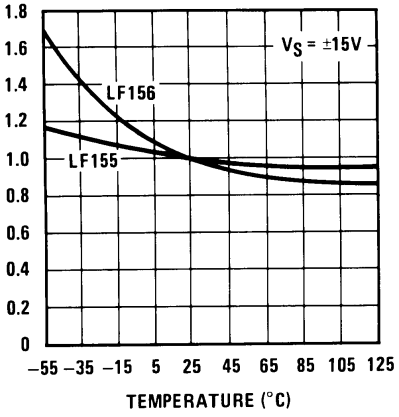
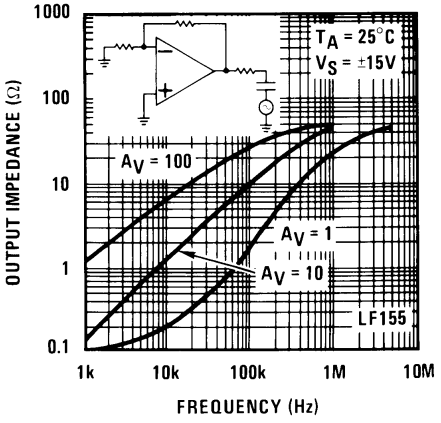
Normalized Slew Rate



00564651

Output Impedance



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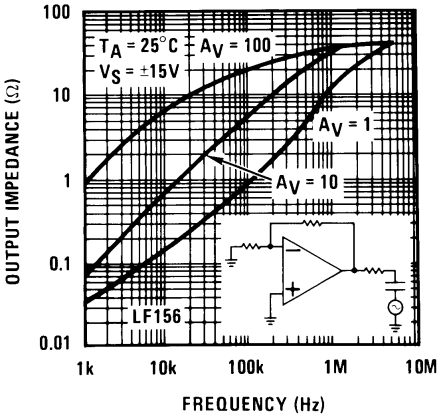
Typical AC Performance Characteristics (Continued)

Output Impedance



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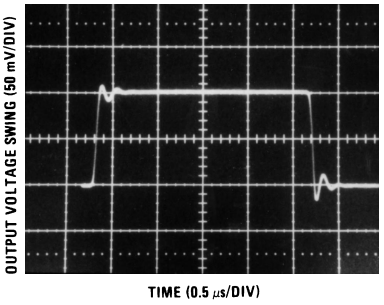
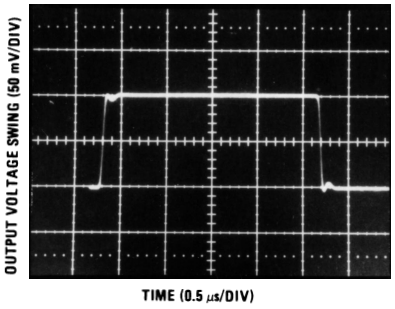
LF155 Small Signal Pulse Response, A_V = +1



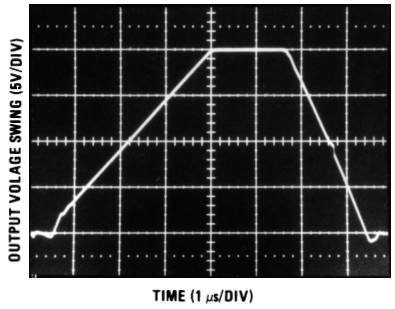
00564605

LF156 Small Signal Pulse Response, A_V = +1



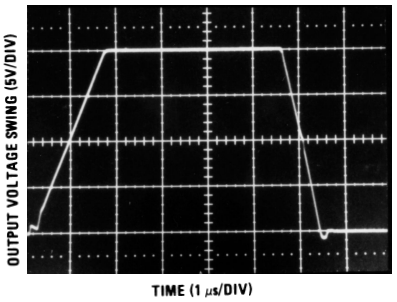
00564606

LF155 Large Signal Pulse Response, A_V = +1



00564608

LF156 Large Signal Puls Response, A_V = +1



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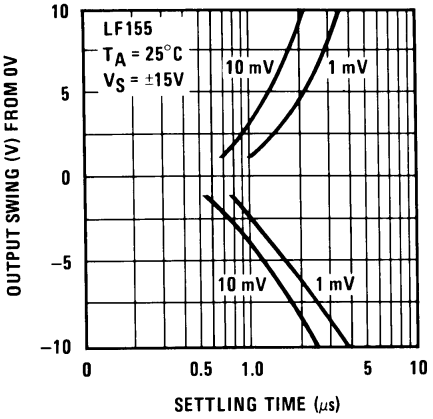
Inverter Settling Time



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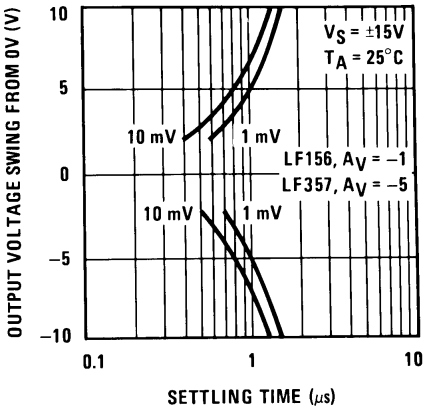
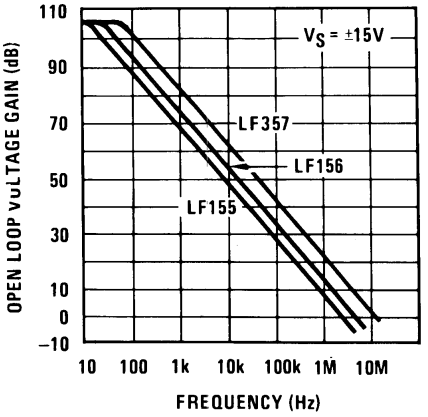
Typical AC Performance Characteristics (Continued)

Inverter Settling Time



00564656

Open Loop Frequency Response



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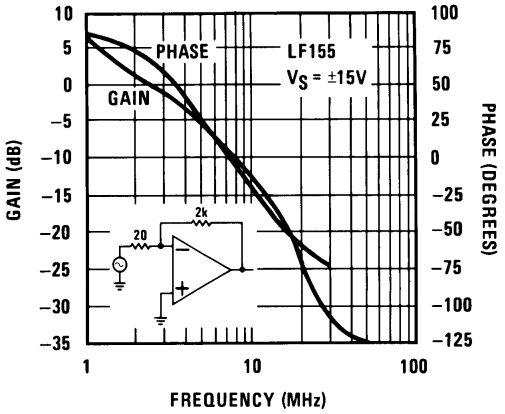
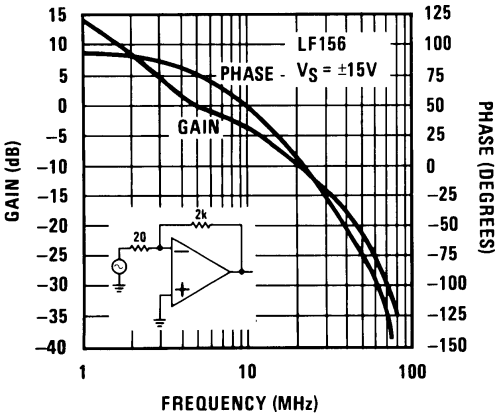
Bode Plot



00564658

Bode Plot



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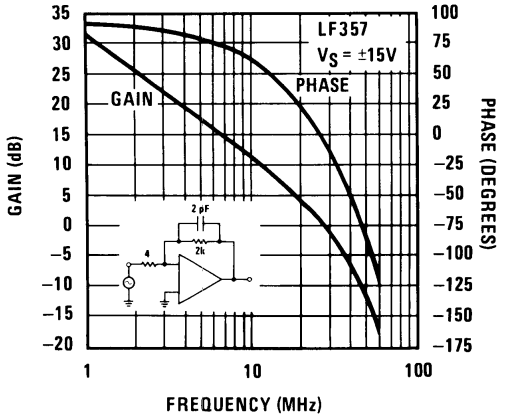
Bode Plot



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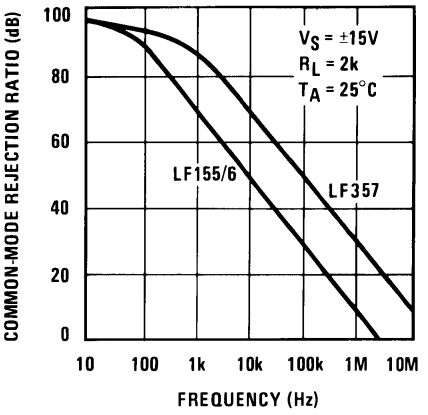
Common-Mode Rejection Ratio



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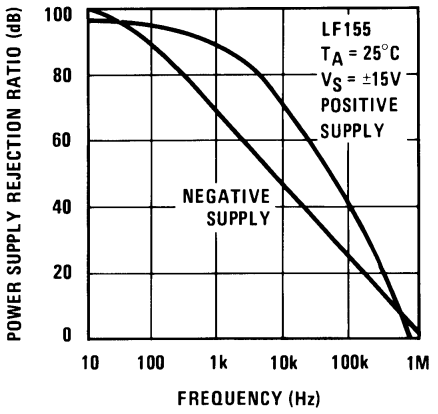
Typical AC Performance Characteristics (Continued)

Power Supply Rejection Ratio



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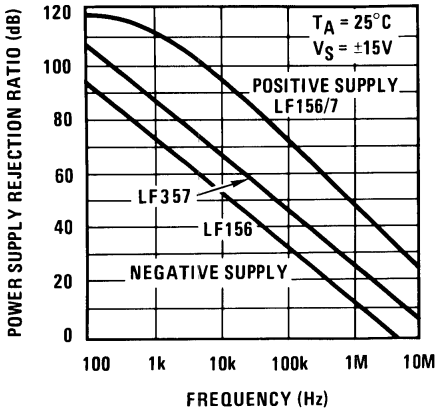
Power Supply Rejection Ratio



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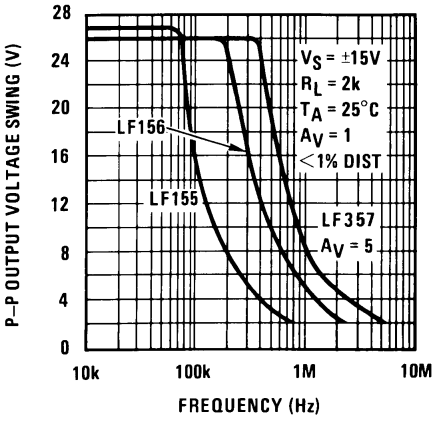
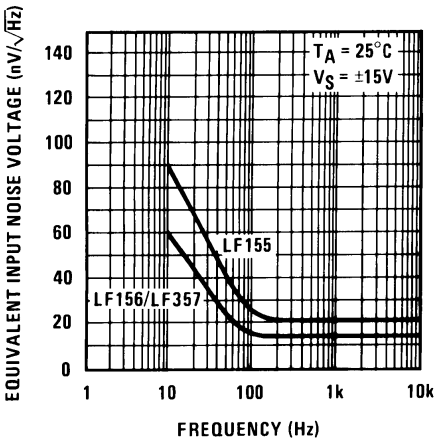
Undistorted Output Voltage Swing



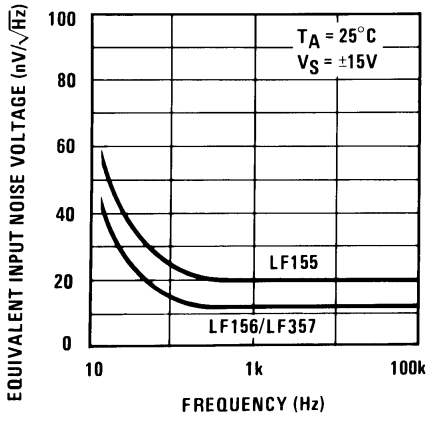
00564664

Equivalent Input Noise Voltage



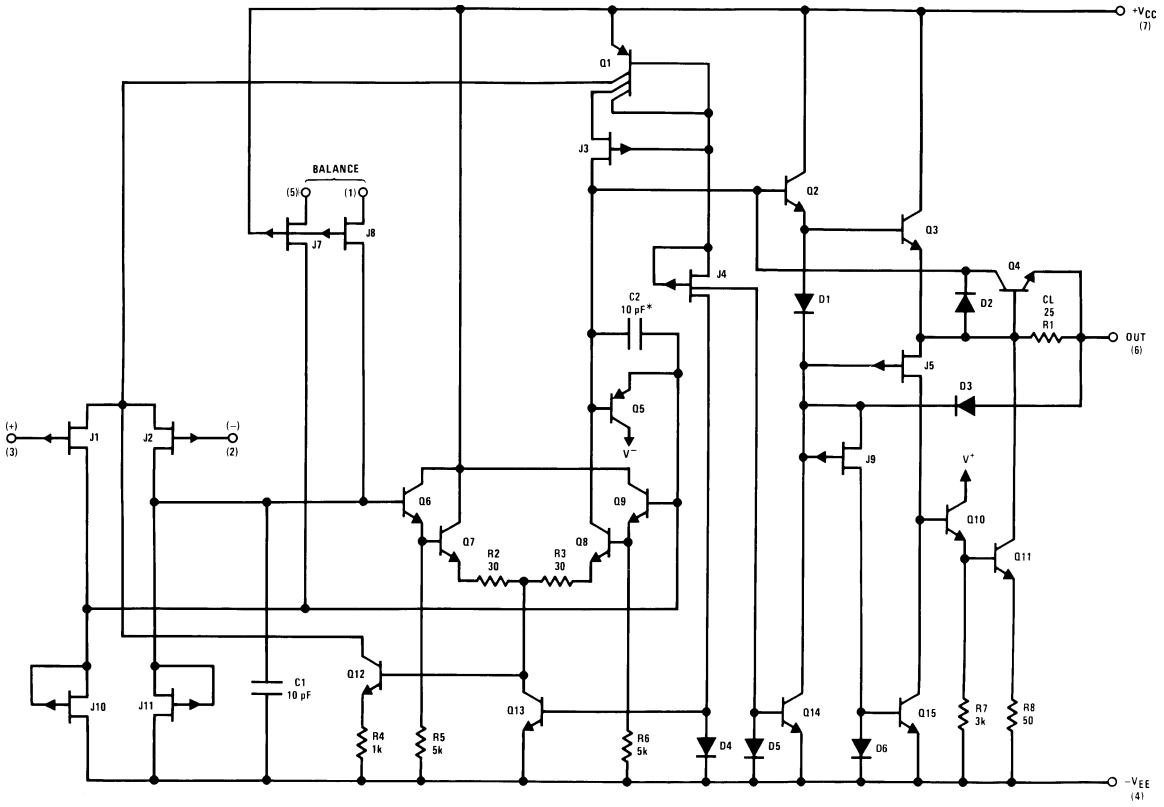
00564665

Equivalent Input Noise Voltage (Expanded Scale)



00564666

Detailed Schematic

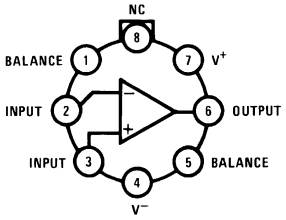


00564613

*C = 3pF in LF357 series.

Connection Diagrams (Top Views)

Metal Can Package (H)

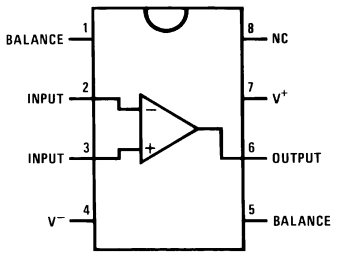


00564614

Order Number LF155H, LF156H, LF256H, LF257H, LF356BH, LF356H, or LF357H
See NS Package Number H08C

*Available per JM38510/11401 or JM38510/11402

Dual-In-Line Package (M and N)



00564629

Order Number LF356M, LF356MX, LF355N, or LF356N
See NS Package Number M08A or N08E

Application Hints

These are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a

Application Hints (Continued)

reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

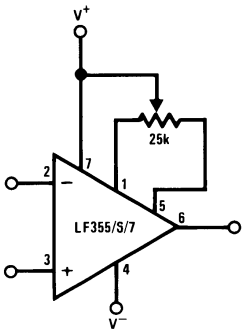
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pickup” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Circuit Connections

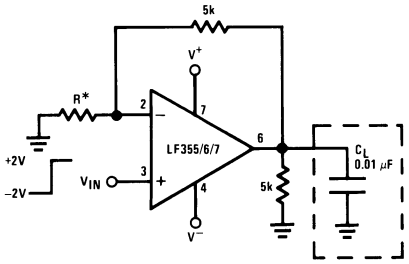
V_{OS} Adjustment



00564667

- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5µV/°C/mV of adjustment
- Typical overall drift: 5µV/°C ±(0.5µV/°C/mV of adj.)

Driving Capacitive Loads



00564668

* LF155/6 R = 5k

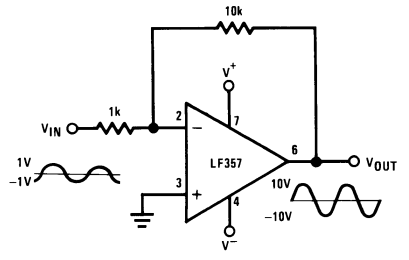
LF357 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \simeq 0.01\mu F$.

Overshoot ≤ 20%

Settling time (t_s) ≃ 5µs

LF357. A Large Power BW Amplifier

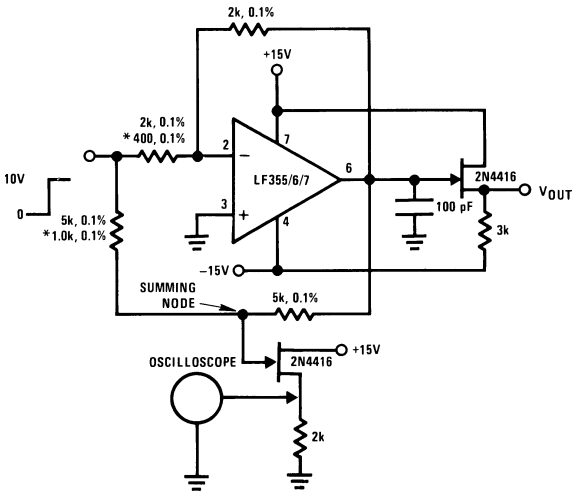


00564615

For distortion ≤ 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500kHz.

Typical Applications

Settling Time Test Circuit

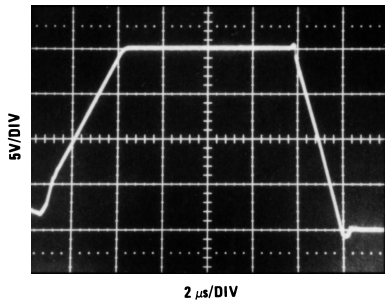


00564616

- Settling time is tested with the LF155/6 connected as unity gain inverter and LF357 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_V = -5$ for LF357

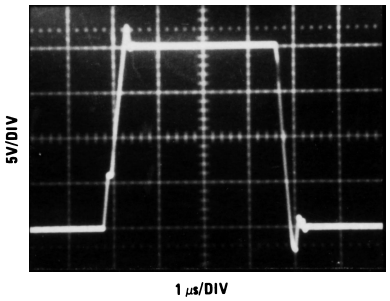
Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

LF355



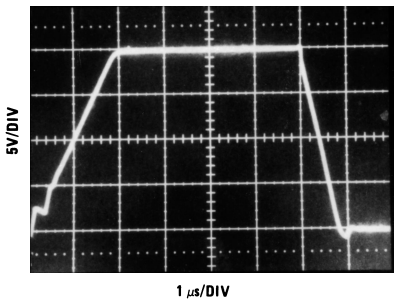
00564617

LF357



00564619

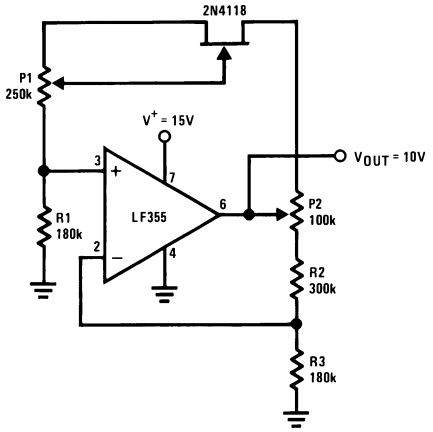
LF356



00564618

Typical Applications (Continued)

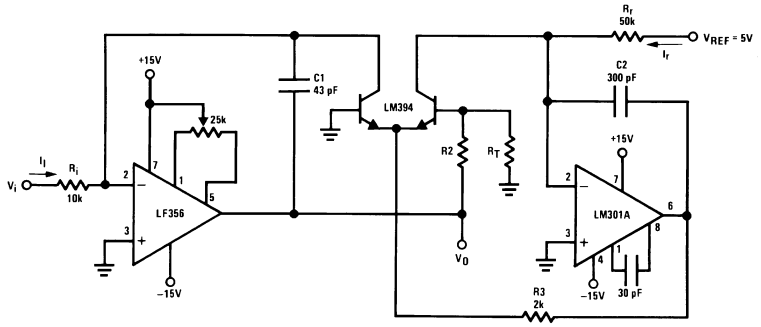
Low Drift Adjustable Voltage Reference



00564620

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{\circ}C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

Fast Logarithmic Converter



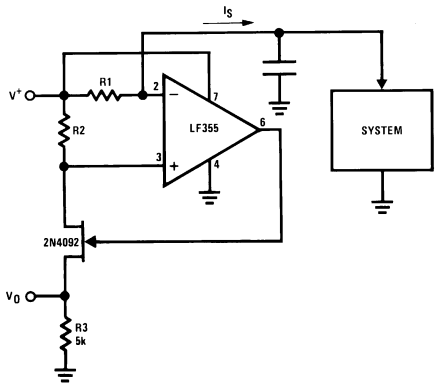
00564621

- Dynamic range: $100\mu A \leq I_i \leq 1mA$ (5 decades), $|V_O| = 1V$/decade
- Transient response: $3\mu s$ for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \text{ in } V_i \left[\frac{R_r}{V_{REF}\, Ri}\right] = \log V_i \frac{1}{R_i I_r} \quad R2 = 15.7k,\ R_T = 1k,\ 0.3\%/^{\circ}C \text{ (for temperature compensation)}$$

Typical Applications (Continued)

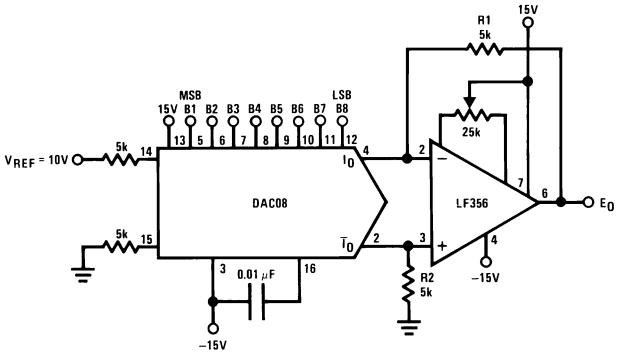
Precision Current Monitor



00564631

- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - ■ Common-mode range to supply range
  - ■ Low I_B
  - ■ Low V_{OS}
  - ■ Low Supply Current

8-Bit D/A Converter with Symmetrical Offset Binary Operation



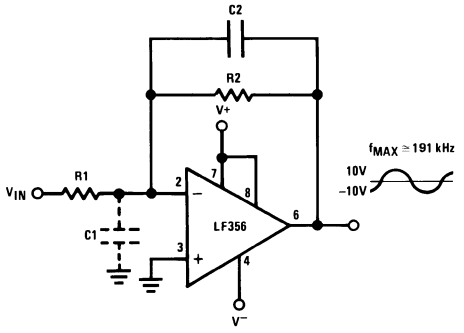
00564632

- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	Comments
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier

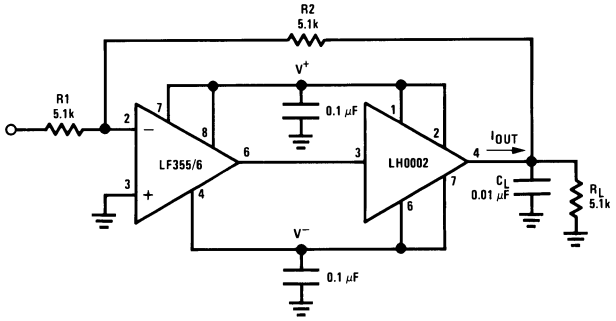


00564670

- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 191\,kHz$

- Parasitic input capacitance C1 ≃ (3pF for LF155, LF156 and LF357 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2 C2 ≃ R1 C1.

Boosting the LF156 with a Current Amplifier



00564673

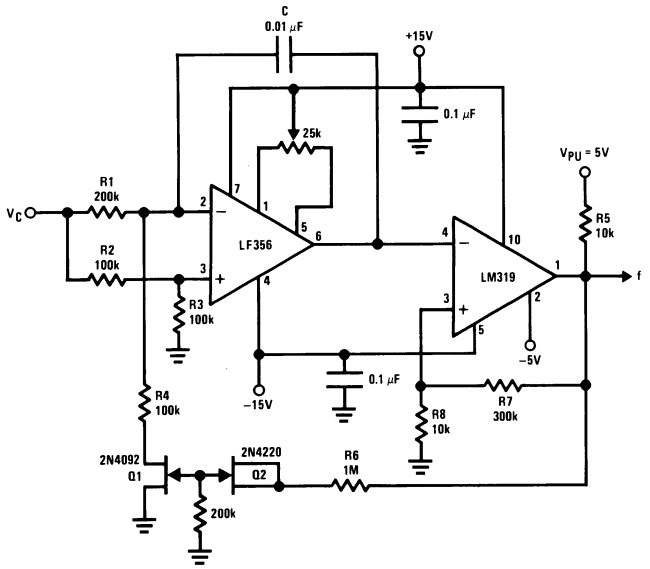
- $I_{OUT(MAX)} \simeq 150mA$ (will drive $R_L \geq 100\Omega$)

- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}\ V/\mu s$ (with C_L shown)

- No additional phase shift added by the current amplifier

Typical Applications (Continued)

3 Decades VCO

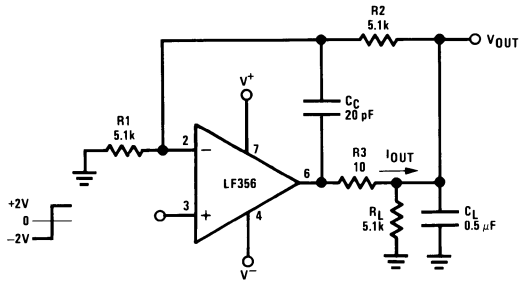


00564624

$$f = \frac{V_C\,(R8 + R7)}{(8\ V_{PU}\ R8\ R1)\ C'} \quad 0 \le V_C \le 30V,\ 10\,Hz \le f \le 10\,kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

Isolating Large Capacitive Loads



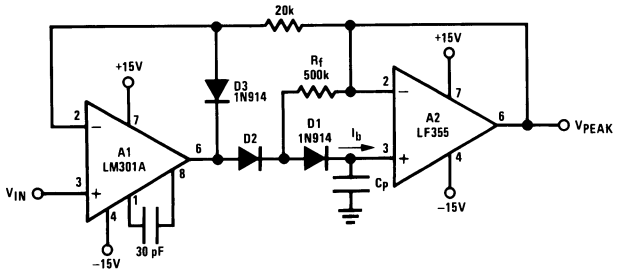
00564622

- Overshoot 6%
- t_s 10µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5}\ V/\mu s = 0.04\ V/\mu s \text{ (with } C_L \text{ shown)}$$

Typical Applications (Continued)

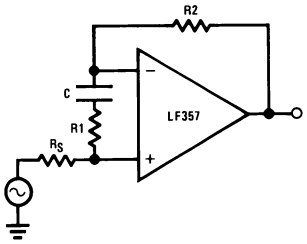
Low Drift Peak Detector



00564623

- By adding D1 and R_f, V_{D1}=0 during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of Cp.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN}-V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< \frac{1}{2}\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

Non-Inverting Unity Gain Operation for LF157



00564675

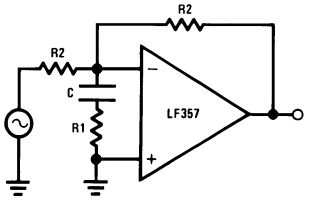
$$R1C \geq \frac{1}{(2\pi)\ (5\ MHz)}$$

$$R1 = \frac{R2 + R_S}{4}$$

$$A_{V(DC)} = 1$$

$$f_{-3\,dB} \approx 5\ MHz$$

Inverting Unity Gain for LF157



00564625

$$R1C \geq \frac{1}{(2\pi)\ (5\ MHz)}$$

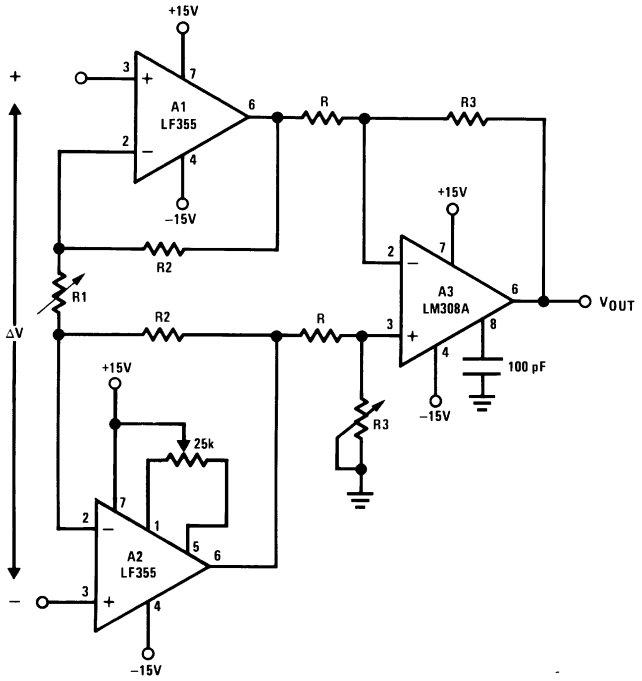
$$R1 = \frac{R2}{4}$$

$$A_{V(DC)} = -1$$

$$f_{-3\,dB} \approx 5\ MHz$$

Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



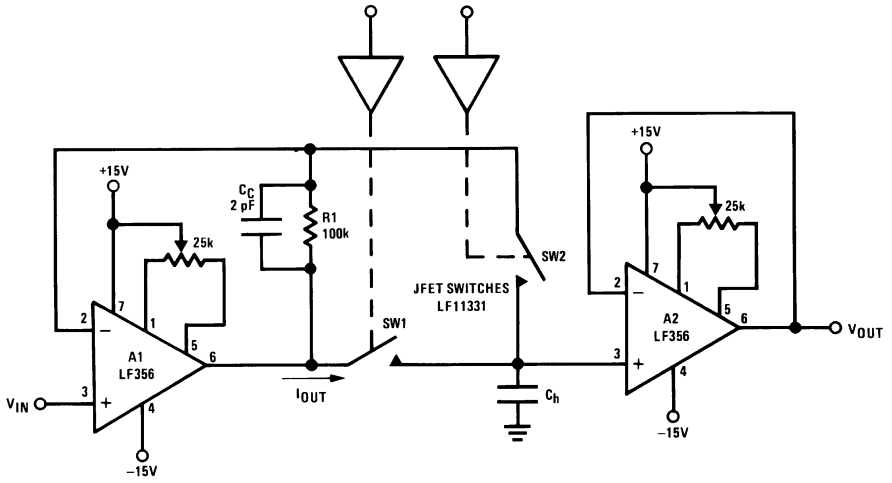
00564626

$$\bullet\ V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]\Delta V,\ V^- + 2V \leq V_{IN}\ \text{common-mode} \leq V^+$$

- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift

Typical Applications (Continued)

Fast Sample and Hold



00564633

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON},\ V_{IN},\ C_h}{S_r}\right] 1/2 \text{ provided that:}$$

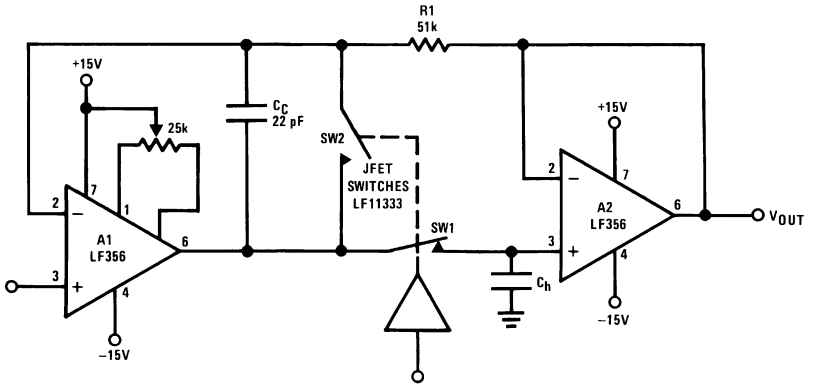
$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}},\ R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \cong \frac{V_{IN} C_h}{20\ mA}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

Typical Applications (Continued)

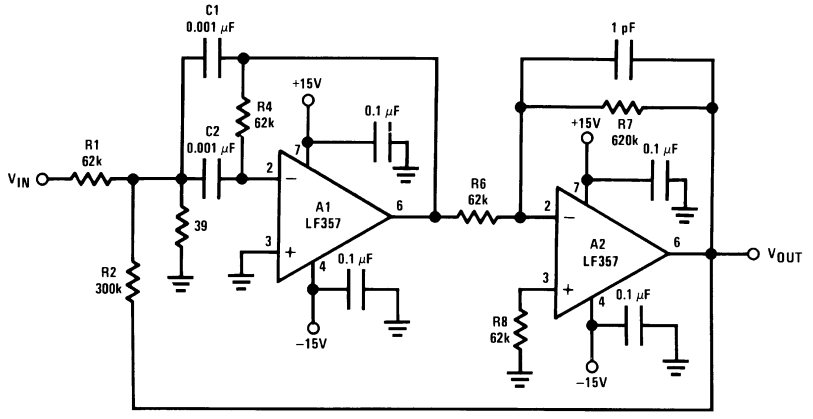
High Accuracy Sample and Hold



00564627

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - ■ Fast settling time
  - ■ Low V_{OS}

High Q Band Pass Filter



00564628

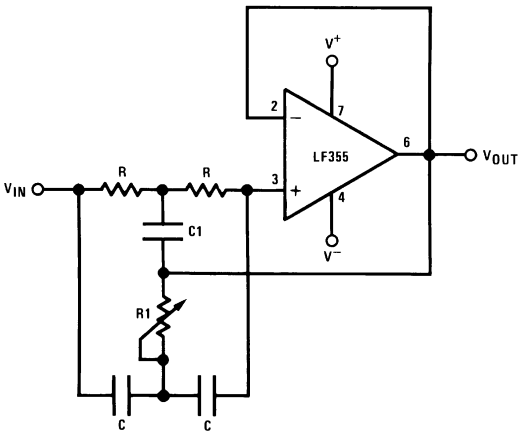
- By adding positive feedback (R2)
- Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1Vp-p tone burst: 300μs

Typical Applications (Continued)

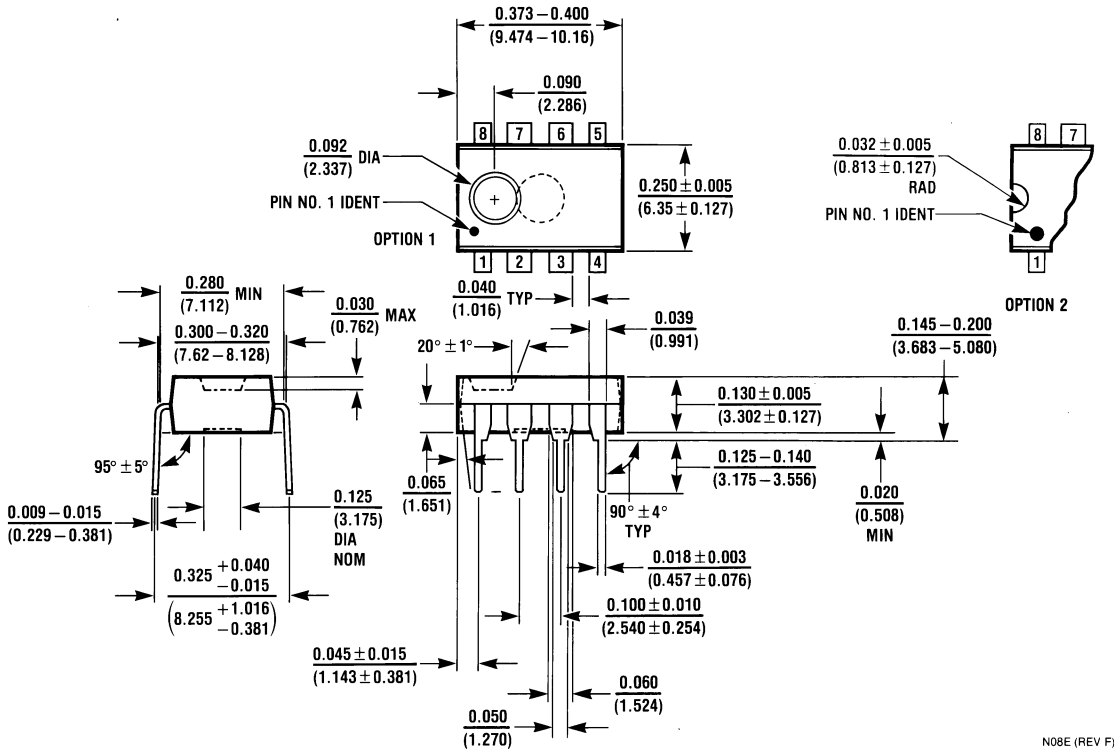
High Q Notch Filter



00564634

- 2R1 = R = 10MΩ
  2C = C1 = 300pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - ■ Low I_B
  - ■ Low supply current

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LF356N
NS Package Number N08E

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August 2000

LF147/LF347
Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

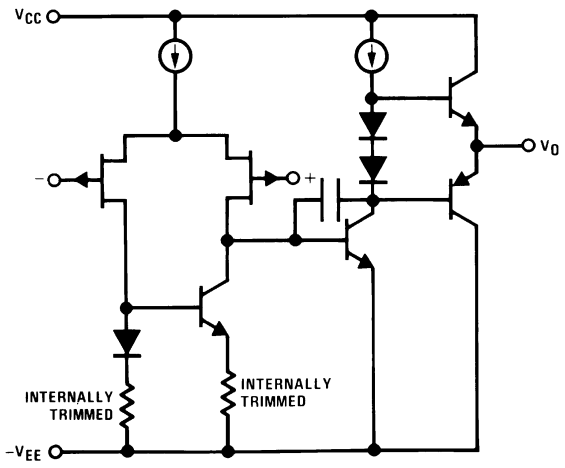
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 5 mV max
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/µs
- Low supply current: 7.2 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion: ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

Simplified Schematic

¼ Quad



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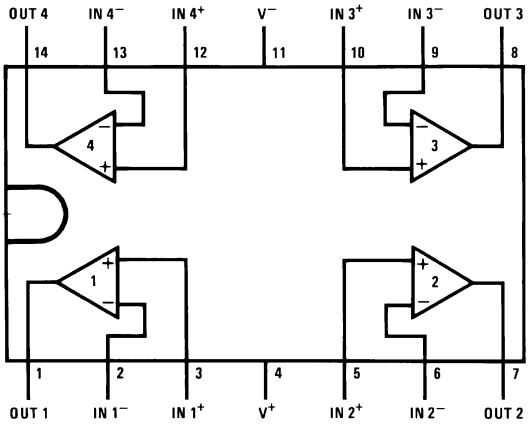
Connection Diagram

Dual-In-Line Package



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Note 1: LF147 available as per JM38510/11906.

Top View
Order Number LF147J, LF147J-SMD, LF347M, LF347BN, LF347N, LF147J/883, or JL147 BCA (Note 1)
See NS Package Number J14A, M14A or N14A

BI-FET II™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 3)	±19V	±15V
Output Short Circuit Duration (Note 4)	Continuous	Continuous
Power Dissipation (Notes 5, 11)	900 mW	1000 mW
T_j max	150˚C	150˚C
θ_{jA}		
Ceramic DIP (J) Package		70˚C/W
Plastic DIP (N) Package		75˚C/W
Surface Mount Narrow (M)		100˚C/W
Surface Mount Wide (WM)		85˚C/W

	LF147	LF347B/LF347
Operating Temperature Range	(Note 6)	(Note 6)
Storage Temperature Range	$-65˚C \le T_A \le 150˚C$	
Lead Temperature (Soldering, 10 sec.)	260˚C	260˚C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)		260˚C
Small Outline Package		
Vapor Phase (60 seconds)		215˚C
Infrared (15 seconds)		220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

ESD Tolerance (Note 12) 900V

DC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25˚C		1	5		3	5		5	10	mV
		Over Temperature			8			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10			10			10		µV/˚C
I_{OS}	Input Offset Current	T_j=25˚C, (Notes 7, 8)		25	100		25	100		25	100	pA
		Over Temperature			25			4			4	nA
I_B	Input Bias Current	T_j=25˚C, (Notes 7, 8)		50	200		50	200		50	200	pA
		Over Temperature			50			8			8	nA
R_{IN}	Input Resistance	T_j=25˚C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25˚C	50	100		50	100		25	100		V/mV
		V_O=±10V, R_L=2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \le 10$ kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 9)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25˚C, f=1 Hz–20 kHz (Input Referred)		–120			–120			–120		dB
SR	Slew Rate	V_S=±15V, T_A=25˚C	8	13		8	13		8	13		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25˚C	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25˚C, R_S=100Ω, f=1000 Hz		20			20			20		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j=25˚C, f=1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	A_V=+10, R_L=10k, V_O=20 Vp-p, BW=20 Hz–20 kHz		<0.02			<0.02			<0.02		%

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 5: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 6: The LF147 is available in the military temperature range –55˚C≤T_A≤125˚C, while the LF347B and the LF347 are available in the commercial temperature range 0˚C≤T_A≤70˚C. Junction temperature can rise to T_j max = 150˚C.

Note 7: Unless otherwise specified the specifications apply over the full temperature range and for V_S=±20V for the LF147 and for V_S=±15V for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

Note 8: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 9: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ± 5V to ±15V for the LF347 and LF347B and from V_S = ±20V to ±5V for the LF147.

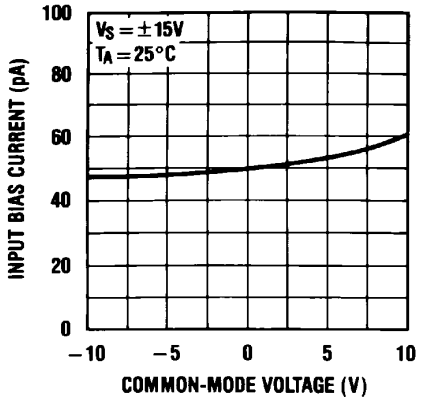
Note 10: Refer to RETS147X for LF147D and LF147J military specifications.

Note 11: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 12: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

Input Bias Current



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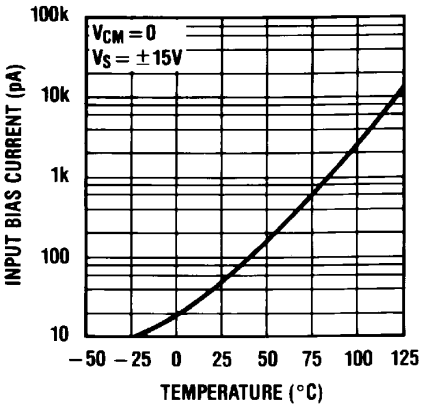
Input Bias Current



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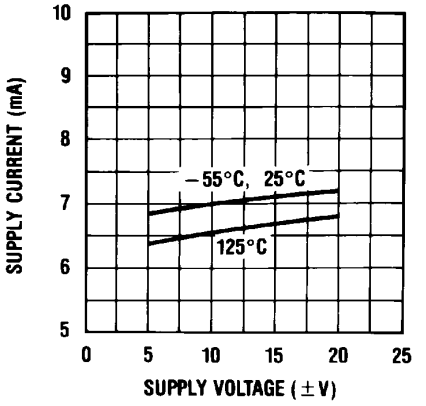
Supply Current



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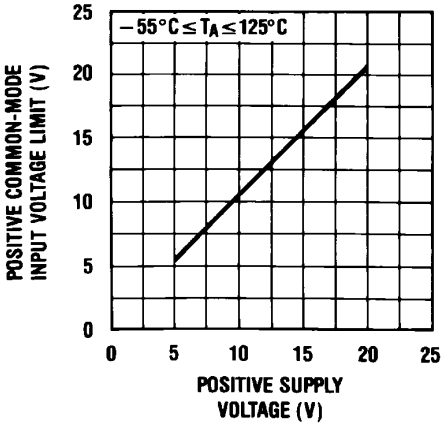
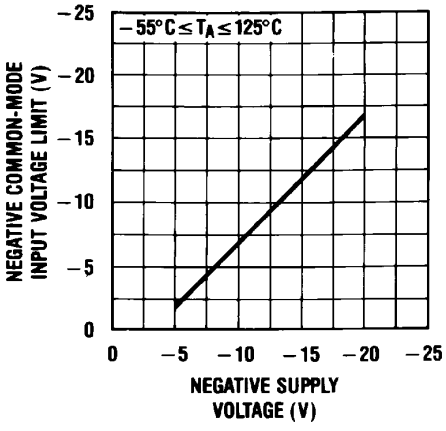
Positive Common-Mode Input Voltage Limit



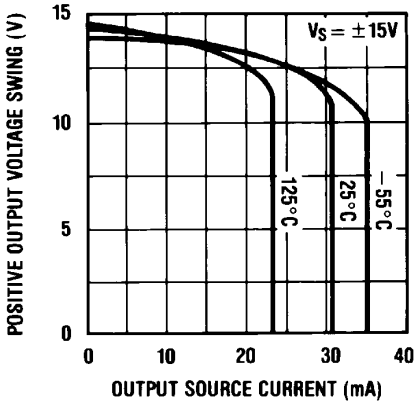
00564717

Negative Common-Mode Input Voltage Limit



00564718

Positive Current Limit



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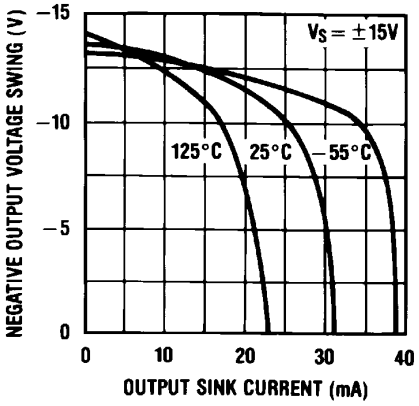
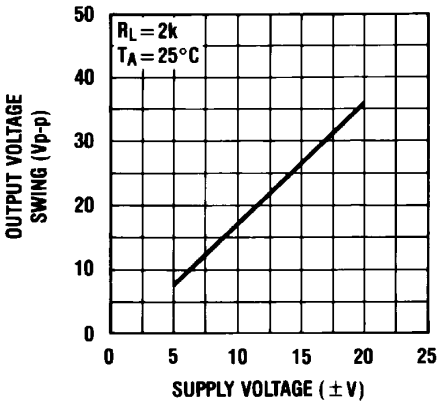
Typical Performance Characteristics (Continued)

Negative Current Limit



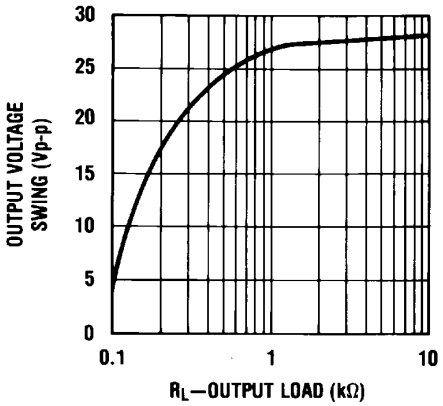
00564720

Output Voltage Swing



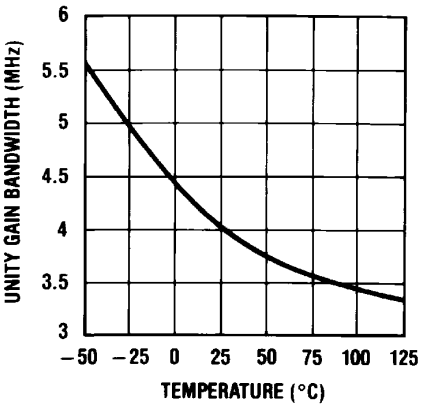
00564721

Output Voltage Swing



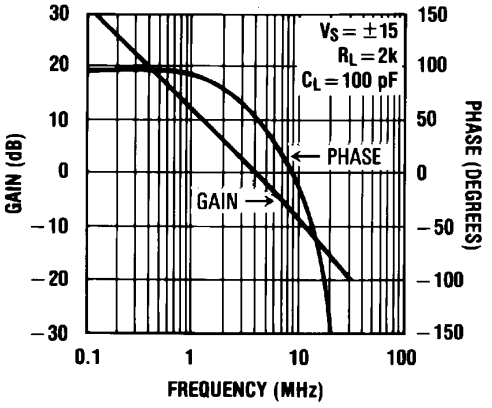
00564722

Gain Bandwidth



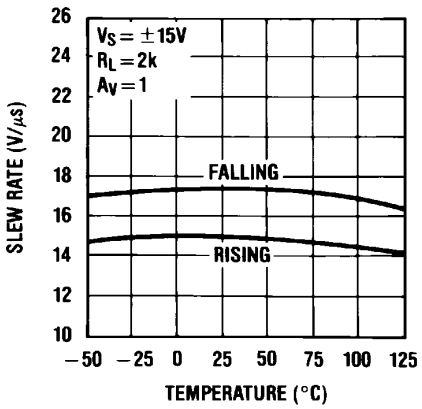
00564723

Bode Plot



00564724

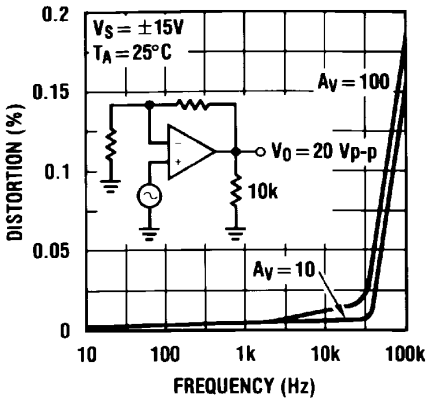
Slew Rate



00564725

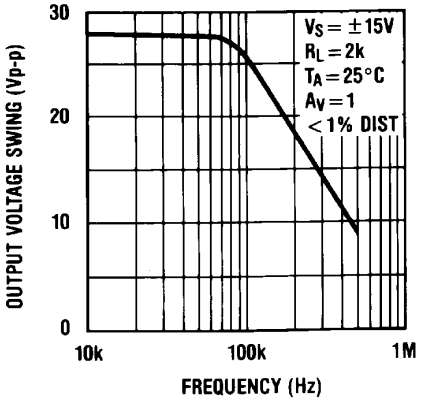
Typical Performance Characteristics (Continued)

Distortion vs Frequency



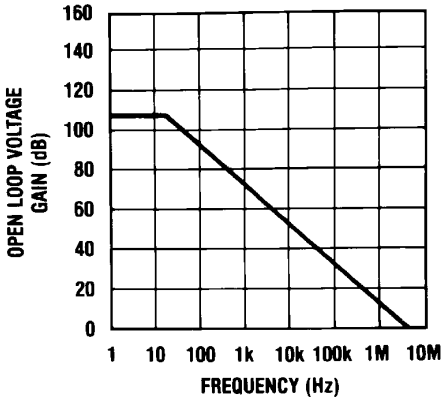
00564726

Undistorted Output Voltage Swing



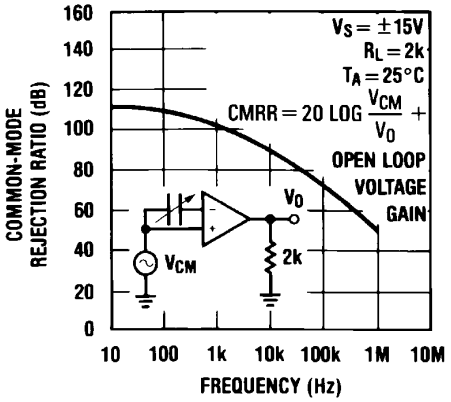
00564727

Open Loop Frequency Response



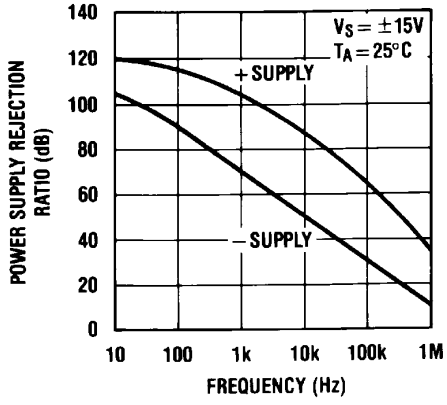
00564728

Common-Mode Rejection Ratio



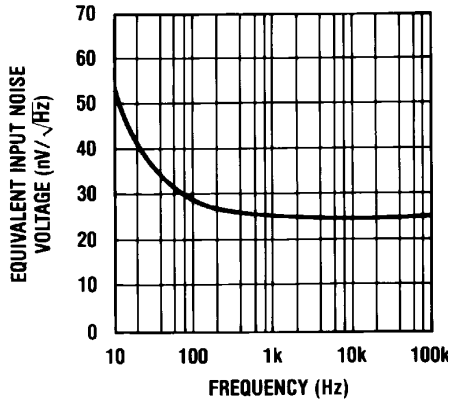
00564729

Power Supply Rejection Ratio



00564730

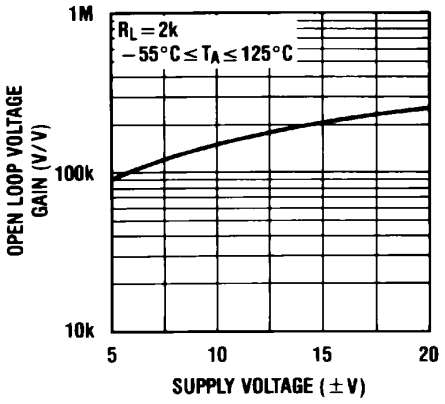
Equivalent Input Noise Voltage



00564731

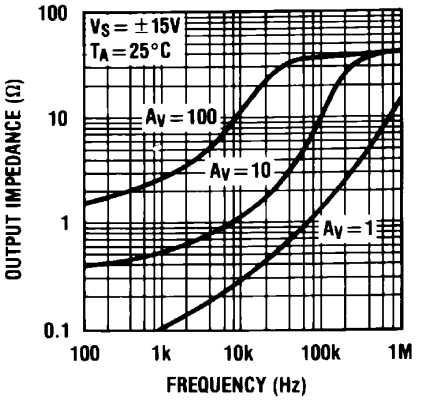
Typical Performance Characteristics (Continued)

Open Loop Voltage Gain



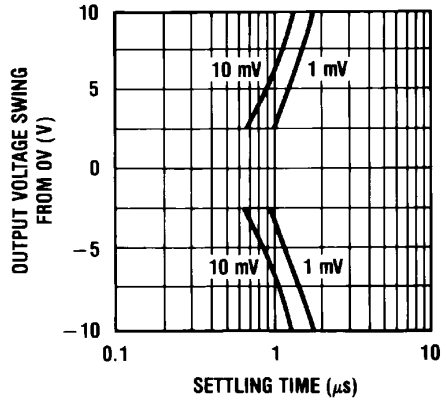
00564732

Output Impedance



00564733

Inverter Settling Time



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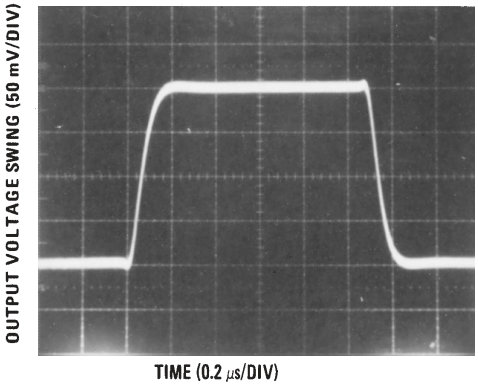
Pulse Response R_L=2 kΩ, C_L=10 pF

Small Signal Inverting



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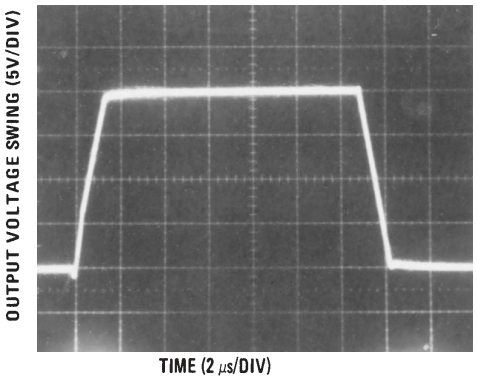
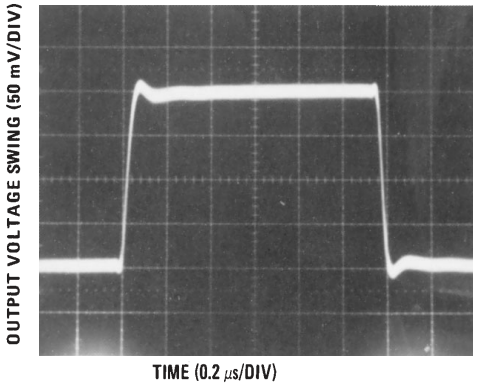
Large Signal Inverting



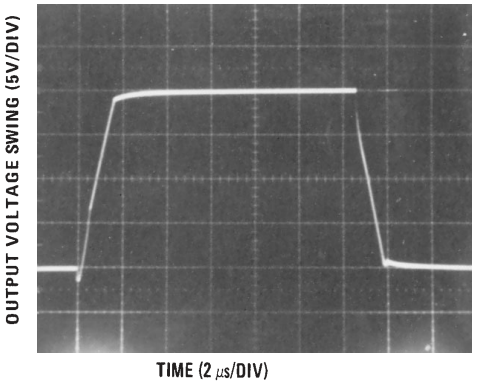
00564706

Small Signal Non-Inverting



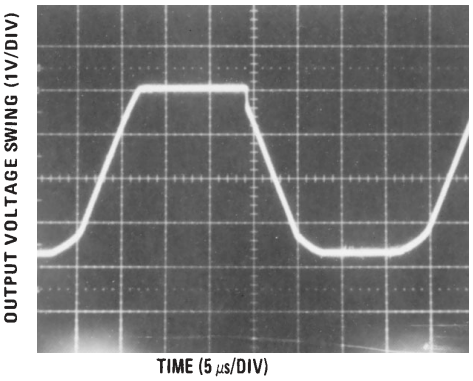
00564705

Large Signal Non-Inverting



00564707

Current Limit (R_L=100Ω)



00564708

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

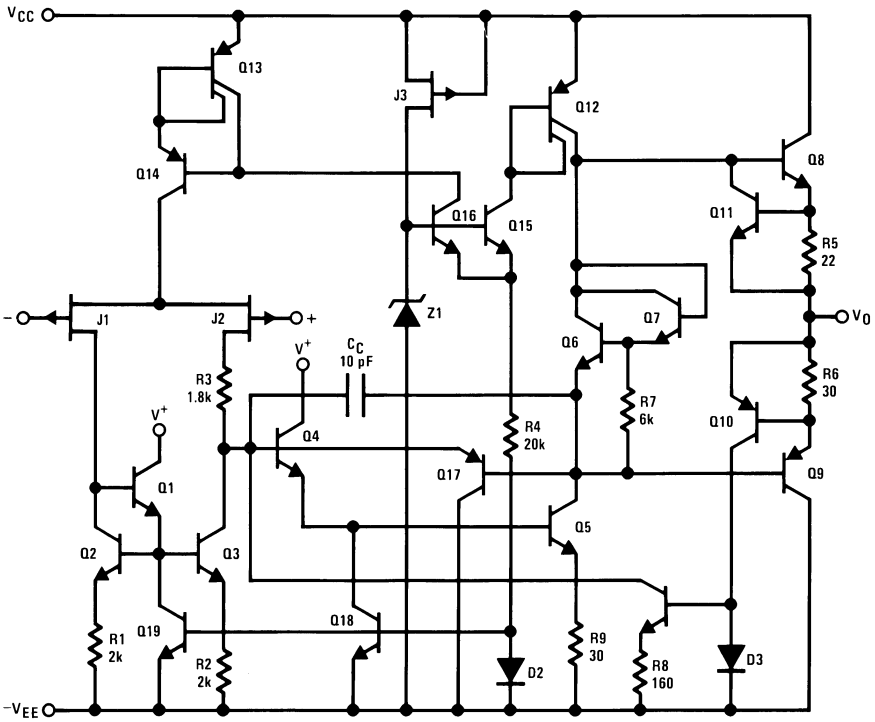
The LF147 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

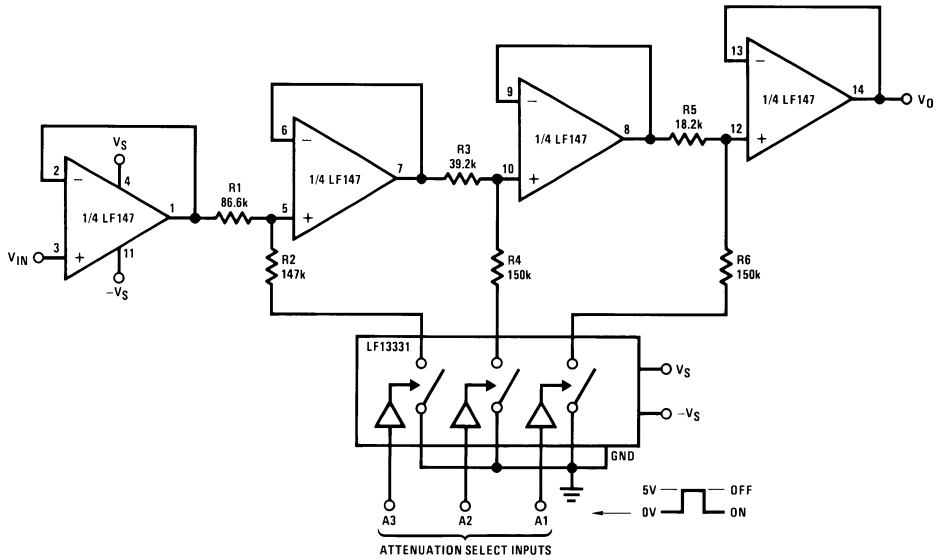
Detailed Schematic



00564709

Typical Applications

Digitally Selectable Precision Attenuator



00564710

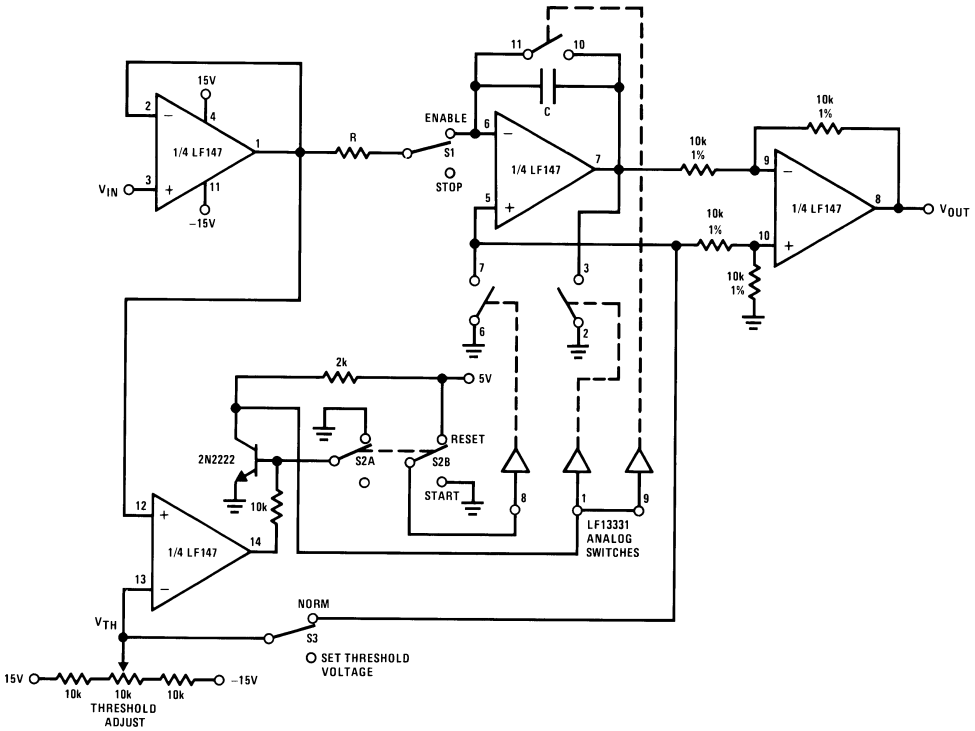
All resistors 1% tolerance

- Accuracy of better than 0.4% with standard 1% value resistors
  No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

A1	A2	A3	V_O Attenuation
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

Typical Applications (Continued)

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



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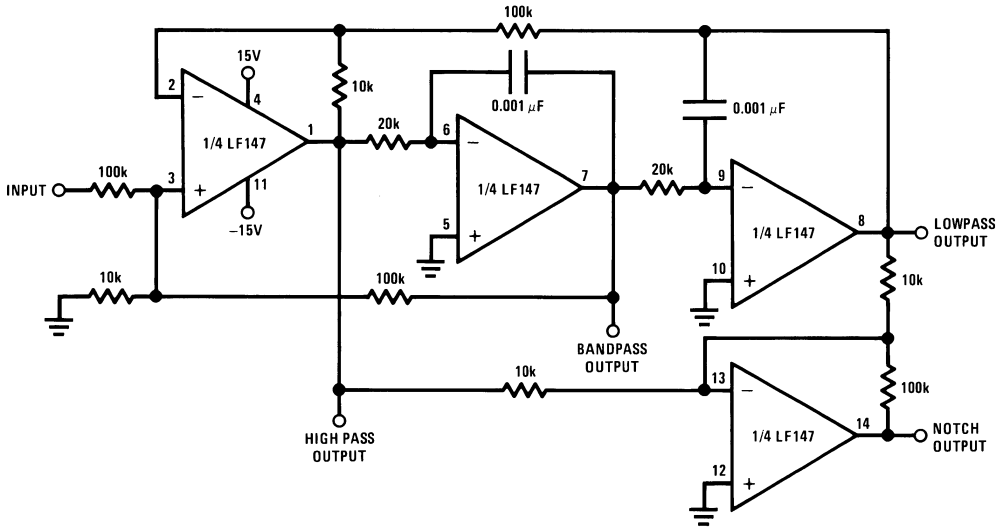
- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter



00564712

For circuit shown:

f_o=3 kHz, f_{NOTCH}=9.5 kHz

Q=3.4

Passband gain:

Highpass — 0.1

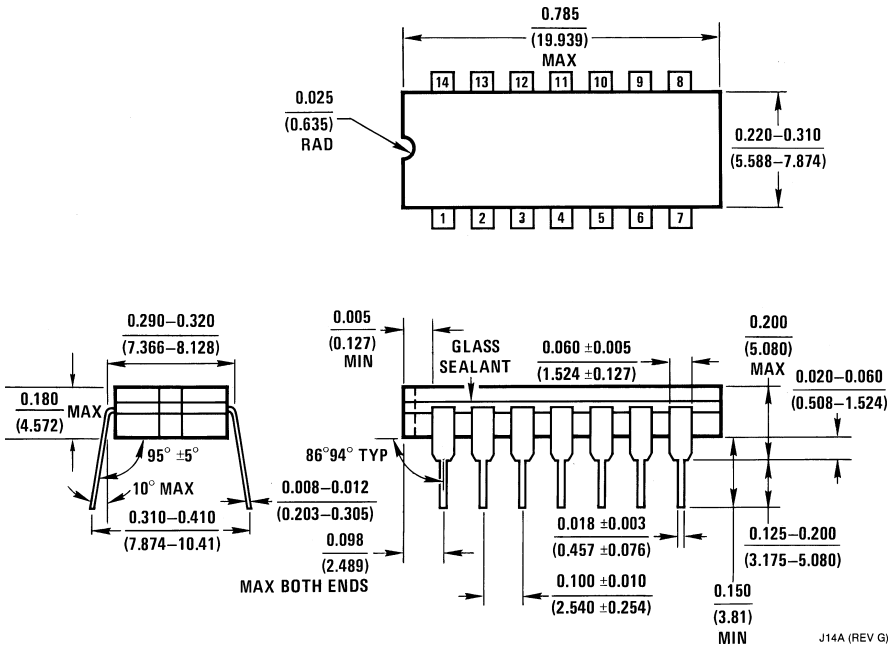
Bandpass — 1

Lowpass — 1

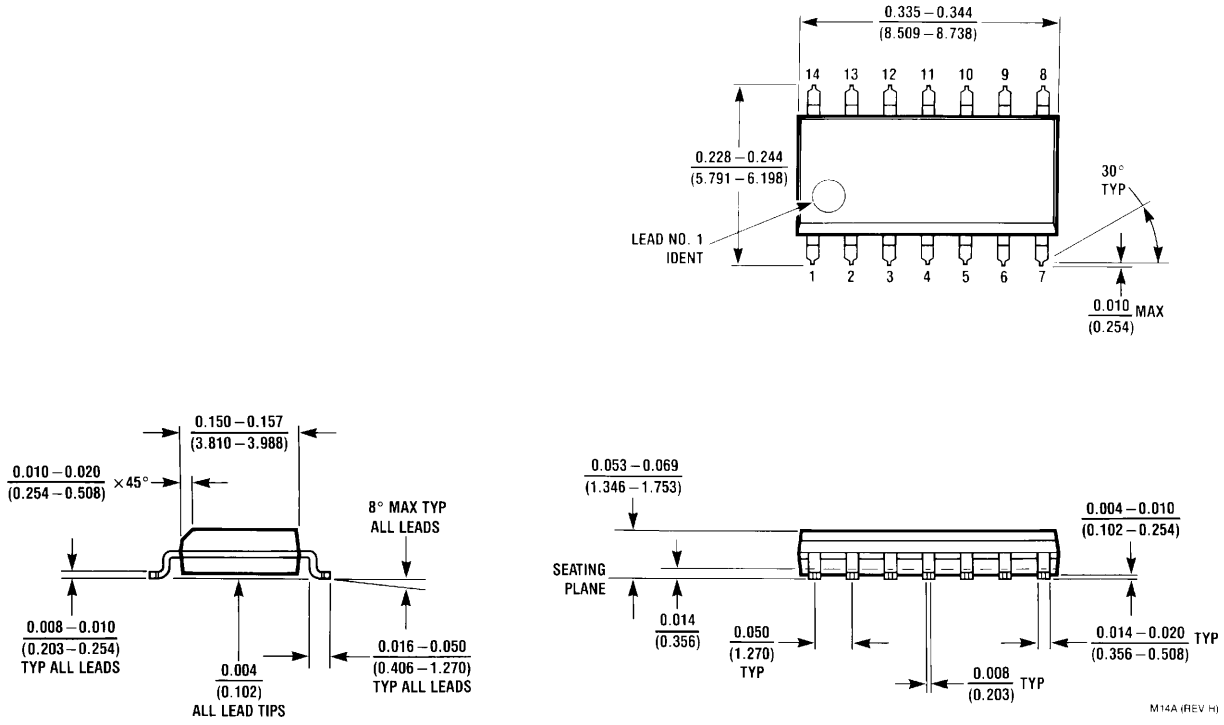
Notch — 10

- f_oxQ≤200 kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

Physical Dimensions inches (millimeters) unless otherwise noted

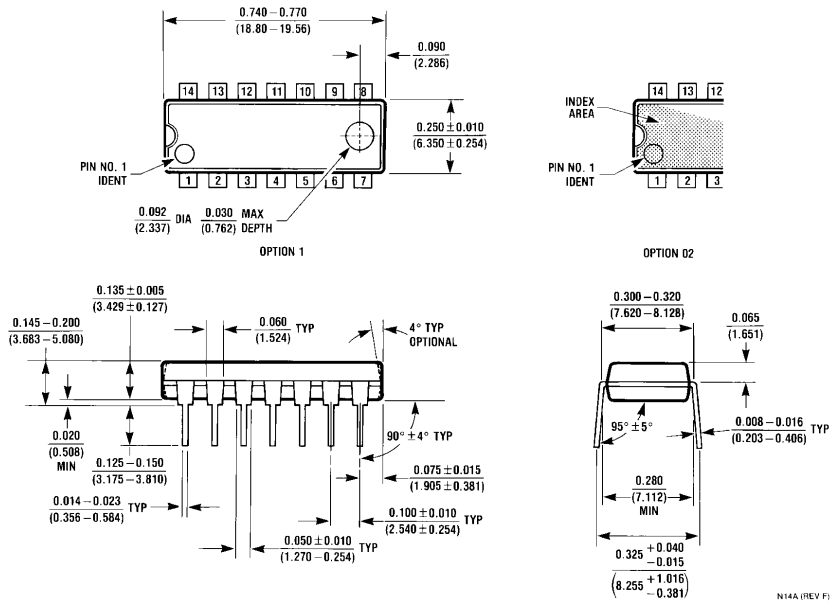


Ceramic Dual-In-Line Package (J)
Order Number LF147J, LM147J-SMD or LF147J/883
NS Package Number J14A



S.O. Package (M)
Order Number LF347M or LF347MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number LF347BN or LF347N
NS Package Number N14A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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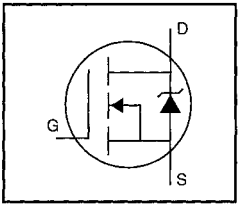
Tel: 81-3-5639-7560

PD-9.859

IRFIZ14G

HEXFET® Power MOSFET

- Isolated Package
- High Voltage Isolation= 2.5KVRMS ⑤
- Sink to Lead Creepage Dist.= 4.8mm
- 175°C Operating Temperature
- Dynamic dv/dt Rating
- Low Thermal Resistance



V_{DSS} = 60V

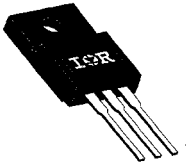
$R_{DS(on)}$ = 0.20Ω

I_D = 8.0A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 Fullpak eliminates the need for additional insulating hardware in commercial-industrial applications. The moulding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. This isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The Fullpak is mounted to a heatsink using a single clip or by a single screw fixing.



TO-220 FULLPAK

DATA SHEETS

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	5.7	
I_{DM}	Pulsed Drain Current ①	32	
P_D @ T_C = 25°C	Power Dissipation	27	W
	Linear Derating Factor	0.18	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	47	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	5.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	65	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.63	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	V_{GS}=10V, I_D=4.8A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	2.2	—	—	S	V_{DS}=25V, I_D=4.8A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=60V, V_{GS}=0V
		—	—	250		V_{DS}=48V, V_{GS}=0V, T_J=150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	11	nC	I_D=10A
Q_{gs}	Gate-to-Source Charge	—	—	3.1		V_{DS}=48V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	5.8		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	V_{DD}=30V
t_r	Rise Time	—	50	—		I_D=10A
$t_{d(off)}$	Turn-Off Delay Time	—	13	—		R_G=24Ω
t_f	Fall Time	—	19	—		R_D=2.7Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	300	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	160	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	29	—		f=1.0MHz See Figure 5
C	Drain to Sink Capacitance	—	12	—	pF	f=1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	32		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	T_J=25°C, I_S=8.0A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	70	140	ns	T_J=25°C, I_F=10A
Q_{rr}	Reverse Recovery Charge	—	0.20	0.40	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=25V, starting T_J=25°C, L=856μH R_G=25Ω, I_{AS}=8.0A (See Figure 12)

③ I_{SD}≤10A, di/dt≤90A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤175°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

⑤ t=60s, f=60Hz

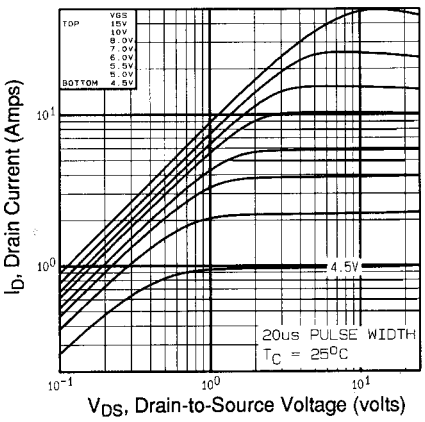


Fig 1. Typical Output Characteristics, T_C=25°C

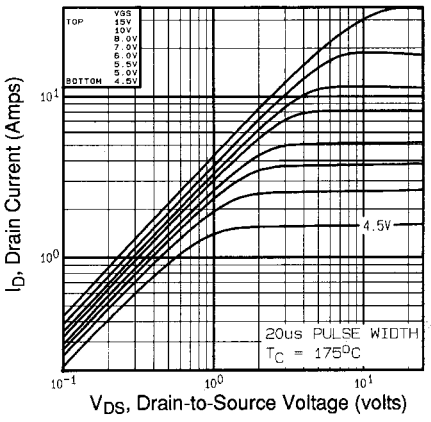


Fig 2. Typical Output Characteristics, T_C=175°C

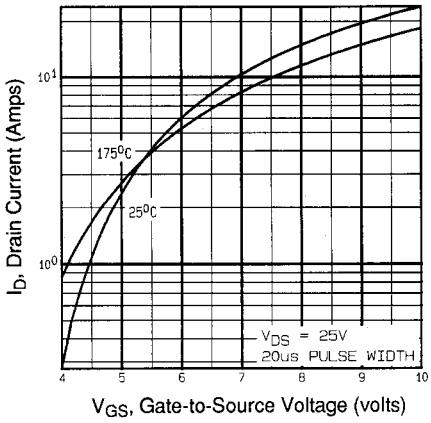


Fig 3. Typical Transfer Characteristics

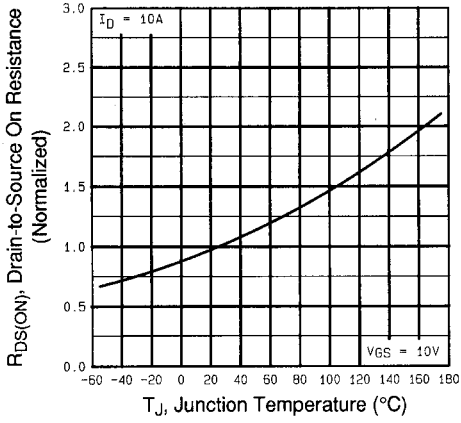


Fig 4. Normalized On-Resistance Vs. Temperature

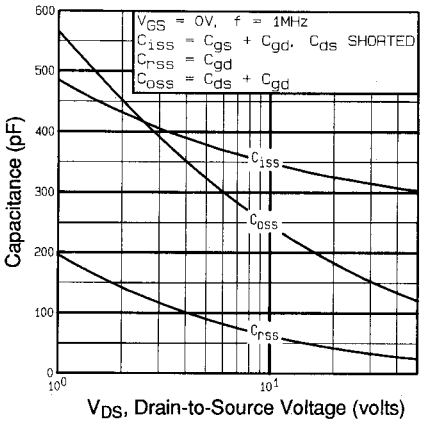


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

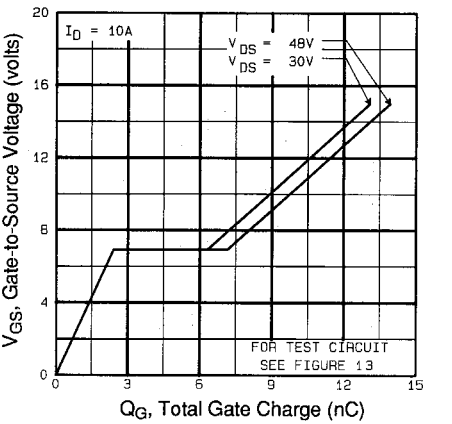


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

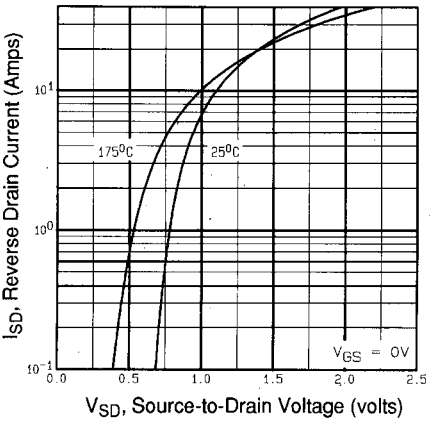


Fig 7. Typical Source-Drain Diode Forward Voltage

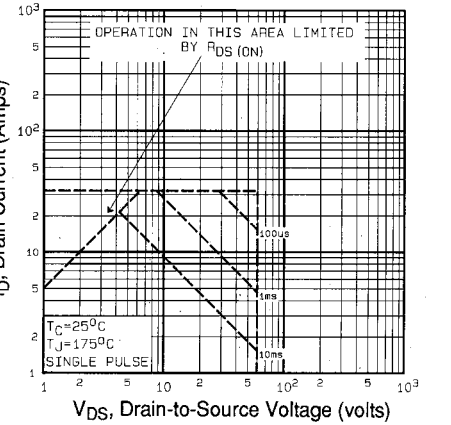


Fig 8. Maximum Safe Operating Area

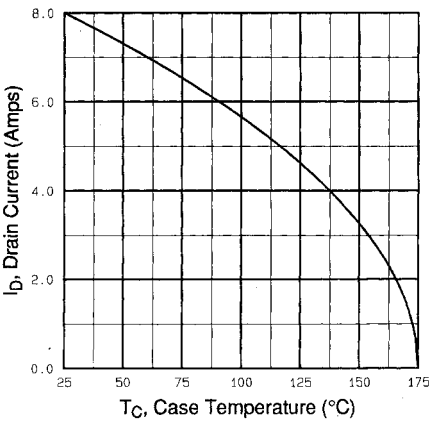


Fig 9. Maximum Drain Current Vs. Case Temperature

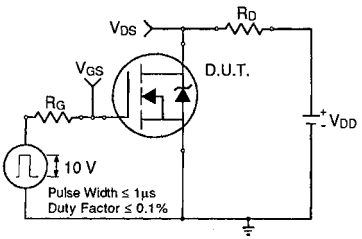


Fig 10a. Switching Time Test Circuit

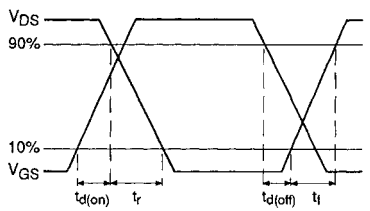


Fig 10b. Switching Time Waveforms

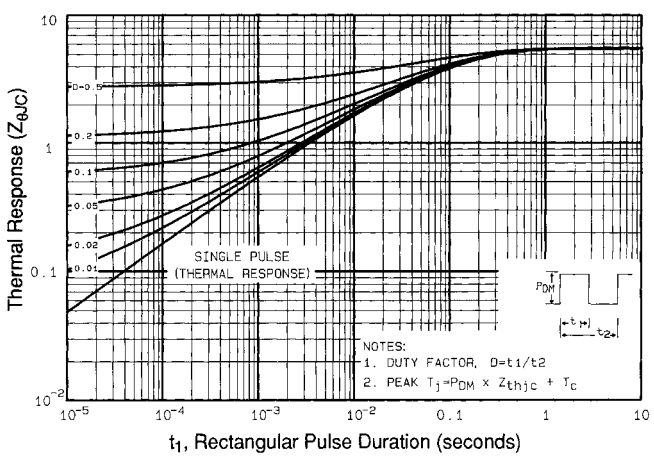


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

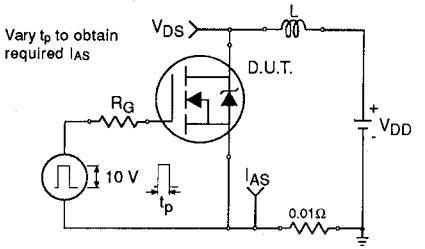


Fig 12a. Unclamped Inductive Test Circuit

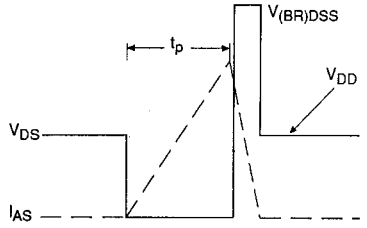


Fig 12b. Unclamped Inductive Waveforms

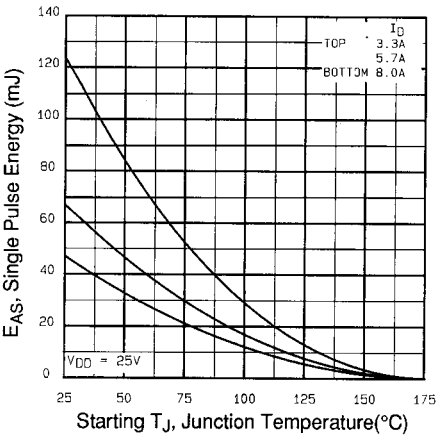


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

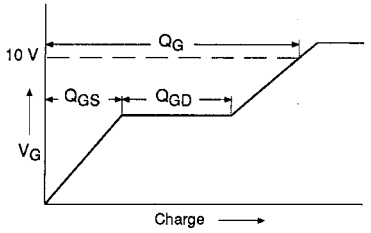


Fig 13a. Basic Gate Charge Waveform

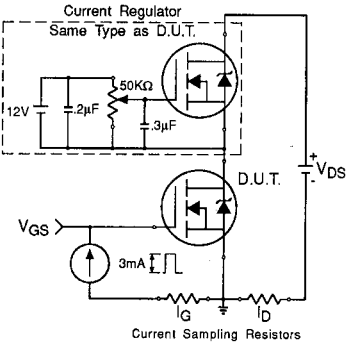


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

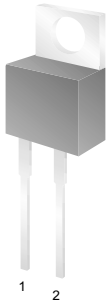
Appendix B: Package Outline Mechanical Drawing – See page 1510

Appendix C: Part Marking Information – See page 1517

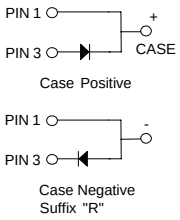
International
IOR Rectifier

FAIRCHILD
SEMICONDUCTOR®

FES16AT - FES16JT



TO-220AC



Features

- Low forward voltage drop.
- High surge current capacity.
- High current capability.
- High reliability.

Fast Rectifiers (Glass Passivated)

Absolute Maximum Ratings*

T_A = 25°C unless otherwise noted

Symbol	Parameter	Value								Units
		16AT	16BT	16CT	16DT	16FT	16GT	16HT	16JT	
V_{RRM}	Maximum Repetitive Reverse Voltage	50	100	150	200	300	400	500	600	V
$I_{F(AV)}$	Average Rectified Forward Current, .375 " lead length @ T_A = 100°C	16								A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	250								A
T_{stg}	Storage Temperature Range	-65 to +150								V
T_J	Operating Junction Temperature	-65 to +150								pF

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	7.81	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	16	°C/W
$R_{\theta JL}$	Thermal Resistance, Junction to Lead	1.2	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Device								Units
		16AT	16BT	16CT	16DT	16FT	16GT	16HT	16JT	
V_F	Forward Voltage @ 8.0A	0.95				1.3		1.5		V
t_{rr}	Reverse Recovery Time I_F = 0.5 A, I_R = 1.0 A, I_{RR} = 0.25 A	35				50				ns
I_R	Reverse Current @ rated V_R T_A = 25°C T_A = 100°C	10 500								µA µA
C_T	Total Capacitance V_R = 4.0. f = 1.0 MHz	170						145		pF

Typical Characteristics

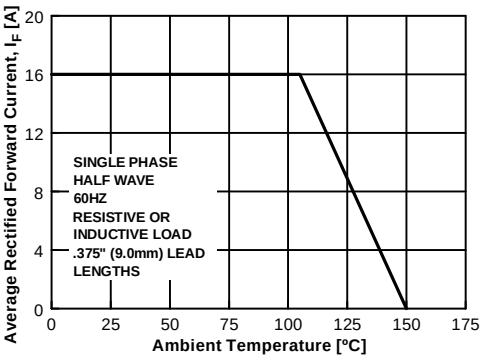


Figure 1. Forward Current Derating Curve

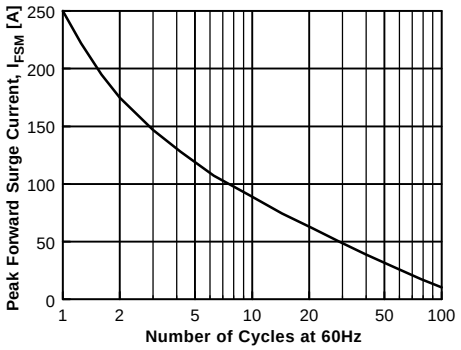


Figure 2. Non-Repetitive Surge Current

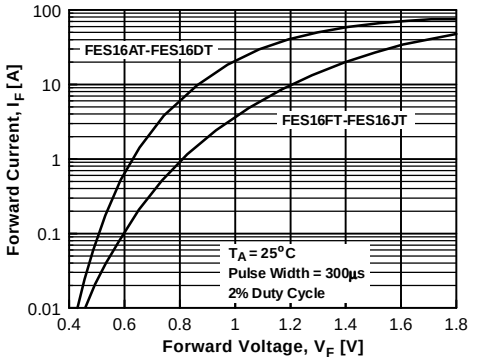


Figure 3. Forward Voltage Characteristics

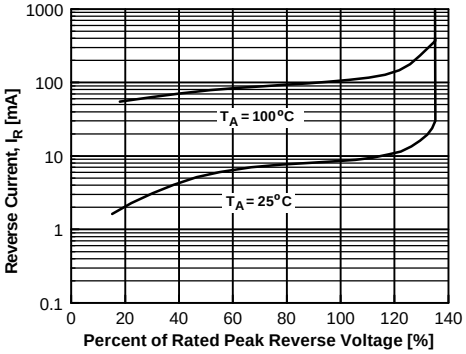


Figure 4. Reverse Current vs Reverse Voltage

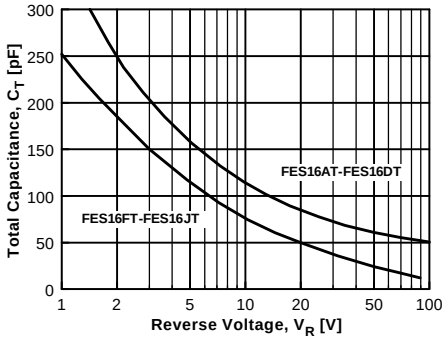
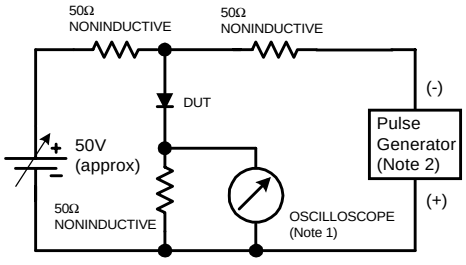
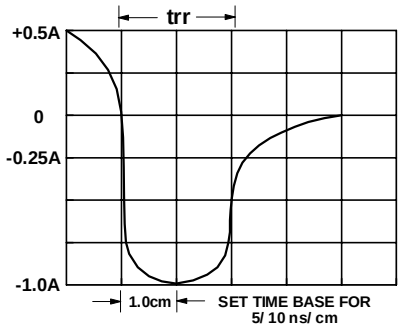


Figure 5. Total Capacitance





Reverse Recovery Time Characterstic and Test Circuit Diagram