Biresh Kumar Joardar

Computing Innovation Fellow (Postdoctoral researcher) at Duke University

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EDUCATION

Computing Innovation Fellow (Postdoc), Sept. 2020 - Present
Duke University, Durham, NC, US
Mentor: Krishnendu Chakrabarty

Ph. D. in Electrical and Computer Engineering, Aug. 2016 – Aug 2020
Washington State University**,** Pullman**,** WA, US
Advisors: Dr. Partha Pratim Pande and Dr. Janardhan Rao Doppa
Major: Computer Engineering
Relevant Coursework: VLSI Design, Machine Learning, Structured Prediction, Computer Architecture
GPA: 4/4

Bachelor of Engineering in Electronics and Telecommunications, Aug. 2012 - May. 2016
Jadavpur University, Kolkata, India
CGPA: 9.1/10 (First Class Honors)

AWARDS and ACHIEVEMENTS

- Selected for the DAAD AInet Fellowship, Awarded by DAAD, 2021
- Received the CI-Fellowship for Post-doctoral research, Awarded by CRA and CCC, 2020
- Best Paper Award Nomination, DATE 2020 and DATE 2021
- Won the Best Paper Award, NOCS 2019
- Outstanding Graduate Student Researcher award, Voiland College of Engineering and Architecture, Washington State University, 2019
- Harold and Dianna Frank Electrical Engineering Fellowship, Washington State University, 2018

PROFESSIONAL SERVICE

Tutorials, Lectures and Special Sessions:

- Overcoming Moore's Law via Technology and Machine Learning-driven Manycore Systems at ESWEEK 2021 (with Dr. Janardhan Rao Doppa)

Program Committee Member:

- International Green and Sustainable Computing Conference (IGSC), 2021
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2021

Reviewer:

- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large-Scale Integrated Circuits and Systems (TVLSI)
- IEEE/ACM Transactions on Computational Biology and Bioinformatics (TCBB)
- IEEE Design & Test (D&T)
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
- IEEE Transactions on Automation Science and Engineering (TASE)
- IEEE Transactions on Circuits and Systems II (TCAS)
- ACM Journal on Emerging Technologies in Computing Systems (JETC)
- ACM Transactions on Architecture and Code Optimization (TACO)

MENTORSHIP and TEACHING

- Mentored students (four PhD and one Masters) at Duke University and Washington State University
- Instructor for ECE 590-7061 course, titled "Machine Learning-based hardware design methodologies", in Fall 2021 at Duke University

PUBLICATIONS (Google Scholar)

Journal Publications:

1. **B. K. Joardar**, A. Deshwal, J. R. Doppa, P. P. Pande and K. Chakrabarty, "High-Throughput Training of Deep CNNs on ReRAM-based Heterogeneous Architectures via Optimized Normalization Layers," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021 (*currently under review*)
2. A. I. Arka, **B. K. Joardar**, R. G. Kim, D. H. Kim, J. R. Doppa, and P. P. Pande, "HeM3D: Heterogeneous Manycore Architecture Based on Monolithic 3D Vertical Integration," in Transactions on Design Automation of Electronic Systems, 2020
3. **B. K. Joardar**, J. R. Doppa, P. P. Pande, H. Li and K. Chakrabarty, "AccuReD: High Accuracy Training of CNNs on ReRAM/GPU Heterogeneous 3D Architecture," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and 5Systems, 2020
4. A. Deshwal, N. K. Jayakodi, **B. K. Joardar**, J. R. Doppa, and P. P. Pande, "MOOS: A Multi-Objective Design Space Exploration and Optimization Framework for NoC Enabled Manycore Systems," in ACM Trans. Embed. Comput. Syst. 18, 5s, Article 77, 2019
5. **B. K. Joardar**, R. G. Kim, J. R. Doppa, P. P. Pande, D. Marculescu and R. Marculescu, "Learning-based Application-Agnostic 3D NoC Design for Heterogeneous Manycore Systems," in IEEE Transactions on Computers, vol. 68, no. 6, pp. 852-866, 2019

Conference Publications:

6. **B. K. Joardar**, J. R. Doppa, H. Li, K. Chakrabarty and P. P. Pande, "Learning to Train CNNs on Faulty ReRAM-based Manycore Accelerators," in International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), 2021.
7. A. I. Arka, **B. K. Joardar**, J. R. Doppa, P. P. Pande and K. Chakrabarty, "DARe: DropLayer-Aware Manycore ReRAM Architecture for Training Graph Neural Networks," in International Conference on Computer Aided Design (ICCAD), 2021.
8. X. Yang, S. Belakaria, **B. K. Joardar**, H. Yang, J. R. Doppa, P. P. Pande, K. Chakrabarty and H. Li, "Multi-Objective Optimization of ReRAM Crossbars for Robust DNN Inferencing under Stochastic Noise," in International Conference on Computer Aided Design (ICCAD), 2021.
9. **B. K. Joardar**, A. I. Arka, J. R. Doppa and P. P. Pande, "3D++: Unlocking the Next Generation of High-Performance and Energy-Efficient Architectures using M3D Integration," in Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 2021
10. A. I. Arka, **B. K. Joardar**, J. R. Doppa, P. P. Pande and K. Chakrabarty, "ReGraphX: NoC-enabled 3D Heterogeneous ReRAM Architecture for Training Graph Neural Networks," in Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 2021 (**Best Paper Award Nomination**).
11. **B. K. Joardar**, N. K. Jayakodi, J. R. Doppa, H. Li, P. P. Pande and K. Chakrabarty, "GRAMARCH: A GPU-ReRAM based Heterogeneous Architecture for Neural Image Segmentation," in Proceedings of 23rd IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition (DATE), 2020 (**Best Paper Award Nomination**)
12. **B. K. Joardar**, P. Ghosh, P. P. Pande, A. Kalyanaraman and S. Krishnamoorthy, "NoC-enabled Software/Hardware Co-Design Framework for Accelerating k-mer Counting," International Symposium on Networks-on-Chip (NOCS '19), New York, NY, USA, 2019 (**Best Paper Award**)
13. P. Bogdan, F. Chen, A. Deshwal, J. R. Doppa, **B. K. Joardar**, H. Li, S. Nazarian, L. Song, and Y. Xiao, "Taming extreme heterogeneity via machine learning based design of autonomous manycore systems," in Proceedings of the International Conf. on Hardware/Software Codesign and System Synthesis Companion (CODES/ISSS), 2019

14. **B. K. Joardar**, A. Deshwal, J. R. Doppa and P. P. Pande, "A Machine Learning Framework for Multi-Objective Design Space Exploration and Optimization of Manycore Systems," 2019 ACM/IEEE 1st Workshop on Machine Learning for CAD (MLCAD), Canmore, AB, Canada, 2019, pp. 1-6
15. **B. K. Joardar**, R. G. Kim, J. R. Doppa, P. P. Pande, "Design and Optimization of Heterogeneous Manycore Systems enabled by Emerging Interconnect Technologies: Promises and Challenges," Proceedings of 22nd IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019
16. **B. K. Joardar**, B. Li, J. R. Doppa, H. Li, P. P. Pande and K. Chakrabarty, "REGENT: A Heterogeneous ReRAM/GPU-based Architecture Enabled by NoC for Training CNNs," Proceedings of 22nd IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019
17. **B. K. Joardar**, J. R. Doppa, P. P. Pande, D. Marculescu and R. Marculescu, "Hybrid On-Chip Communication Architectures for Heterogeneous Manycore Systems," Proceedings of 37th IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2018.
18. **B. K. Joardar**, K. Duraisamy and P. P. Pande, "High performance collective communication-aware 3D Network-on-Chip architectures," 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, 2018
19. **B. K. Joardar**, W. Choi, R. G. Kim, J. R. Doppa, P. P. Pande, D. Marculescu and R. Marculescu, "3D NoC-enabled heterogeneous manycore architectures for accelerating CNN training: Performance and thermal trade-offs," 2017 Eleventh IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Seoul, 2017

EXPERIENCE

Internship May 2019 – Aug. 2019

Cadence Design Systems, San Jose, CA

- Machine Learning-based netlist optimization for faster RTL synthesis

Graduate Research Assistant Aug. 2016 – Aug 2020

School of EECS, Washington State University, Pullman, WA.

- Machine Learning enabled multi-objective design space exploration and optimization algorithms
- Software/Hardware Co-Design solutions for Deep Learning applications
- Heterogeneous architectures with CPUs, GPUs, and Non-volatile memory for Machine Learning
- Novel Hardware design like Processing-in-memory using 3D integration and new interconnect paradigms

PROJECTS

- Machine Learning
  - Accelerating Graph Neural Networks for graph property prediction.
  - Mixed precision Convolutional Neural Network training for faster image recognition.
  - Implemented complex search/optimization techniques like Dagger, Bayesian Optimization, etc.
  - Worked with a wide variety of learning algorithms including reinforcement learning, imitation learning, structured prediction based online learning with complex datasets.
- Novel hardware design
  - Reliable in-memory computing architecture design
  - Novel designs considering domain- and application-specific requirements and trade-offs
  - Heterogeneous architecture design with new interconnect and integration methodologies

OTHERS

- Presented my research at multiple conferences including DATE (2018, 2019, 2020), NOCS (2019).
- Presented a poster on Machine Learning-based netlist optimization at Cadence.