Biresh Kumar Joardar

Assistant Professor at University of Houston

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PROFESSIONAL EXPERIENCE

Assistant Professor, Sept. 2022 – Present
University of Houston, Houston, TX, US

NSF Computing Innovation (Postdoctoral) Fellow, Sept. 2020 – Aug 2022
Duke University, Durham, NC, US
Mentor: Krishnendu Chakrabarty

Internship May 2019 – Aug. 2019
Cadence Design Systems, San Jose, CA
Project: Machine Learning-based netlist optimization for faster RTL synthesis

EDUCATION

Ph. D. in Electrical and Computer Engineering, Aug. 2016 – Aug 2020
Washington State University**,** Pullman**,** WA, US
Advisors: Dr. Partha Pratim Pande and Dr. Janardhan Rao Doppa
Major: Computer Engineering, GPA: 4/4

Bachelor of Engineering, Aug. 2012 - May. 2016
Jadavpur University, Kolkata, India
Major: Electronics and Telecommunications, GPA: 9.1/10 (First Class Honors)

PROFESSIONAL SERVICE

Journal Associate Editor:

- ACM TODAES Special Issue on Embedded System Software/Tools, 2023-2024

Competition organizing:

- Co-chair of Embedded System Software Competition (ESSC) at ESWEEK 2023, 2024

Program Committee Member and Track/Session chair duties:

- International Conference on VLSI Design (VLSID), 2024 (Track chair)
- International Symposium on Smart Electronic Systems (iSES), 2024 (SRF chair)
- The AAAI conference on Artificial Intelligence Student Abstract, 2024
- Embedded Systems Week conference (ESWEEK), 2024, (*Track Chair*)
- Design Automation Conference (DAC), 2022, 2023 (*TPC and Session chair*), 2024
- International Symposium on Hardware Oriented Security and Trust (HOST), 2022, 2023 and 2024
- The AAAI conference on Artificial Intelligence, 2023, 2024
- International Reliability Physics Symposium (IRPS), 2024
- International Green and Sustainable Computing Conference (IGSC), 2021, 2022 and 2023
- Network-On-Chip symposium (NOCS), 2022
- International Conference on Computer-Aided Design (ICCAD), 2022 (*Session chair*)
- International Conference on Networking, Architecture, and Storage (NAS), 2022
- Jury member for Student Research Competition at ICCAD, 2021
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2021

Reviewer (Web of Science profile):

- IEEE Transactions on Very Large-Scale Integration (VLSI) Systems (22)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (14)

- IEEE Design & Test (12)
- IEEE Transactions on Computers (11)
- ACM Journal on Emerging Technologies in Computing Systems (9)
- IEEE Embedded Systems Letters (7)
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (4)
- IEEE Transactions on Parallel and Distributed Systems (4)
- IEEE Micro (3)
- IEEE Transactions on Automation Science and Engineering (3)
- IEEE Transactions on Emerging Topics in Computational Intelligence (2)
- IEEE/ACM Transactions on Computational Biology and Bioinformatics (2)
- Transactions on Architecture and Code Optimization (2)
- IEEE Transactions on Emerging Topics in Computing (1)
- IEEE Transactions on Information Forensics and Security (1)
- IEEE Transactions on Circuits and Systems I: Regular Papers (1)
- Electronics Letters (1)
- ACM Transactions on Intelligent Systems and Technology (1)
- Transactions on Embedded Computing Systems (1)
- IEEE Transactions on Circuits and Systems II: Express Briefs (1)

Tutorials and Special Sessions:

- Special session at DCAS 2024, ICCAD 2021
- Processing-in-Memory enabled Manycore Systems Design for Deep Learning Workloads at ESWEEK 2022
- Overcoming Moore's Law via Technology and Machine Learning-driven Manycore Systems at ESWEEK 2021

MENTORSHIP and TEACHING

- Two PhD students and three masters students.
- Mentored seven school students at various grades.
- Participated as judge at regional and state-level school science fairs in Houston, Texas.
- Instructor for ECE 5346/6346 (VLSI) course at UH, Spring and Fall 2023, Spring and Fall 2024
    - Average class size: ~40, Faculty evaluation (average): 4.74/5
- Instructor for ECE 590-7061 course, titled “Machine Learning-based hardware design methodologies”, in Fall 2021 at Duke University.
- Mentored five students (four PhD and one Masters) at Duke University and Washington State University.

PUBLICATIONS (Google Scholar)

Book Chapters:

1. **B.K. Joardar**, J. R. Doppa, P. P. Pande, “Machine Learning for Heterogeneous Manycore Design, “Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing,” In: Pasricha, S., Shafique, M. (eds), Springer, Cham
2. Y. Ma, **B. K. Joardar**, P. P. Pande, A. Joshi, “Interconnect and Integration Technology,” In: Aly, M.M.S., Chattopadhyay, A. (eds) Emerging Computing: From Devices to Systems. Computer Architecture and Design Methodologies. Springer, Singapore

Journal Publications:

3. **P. Edara**, S. Banerjee, **B. K. Joardar**, “Localization of Data Compromised by Hardware Attacks in Machine Learning enabled Cyber-Physical Edge Devices,” in IEEE ACM Transactions on Cyber-Physical Systems, 2024, (under review)
4. C. Ogbogu, **B. K. Joardar**, K. Chakrabarty, J. R. Doppa, and P. P. Pande. 2024. Data Pruning-enabled High Performance and Reliable Graph Neural Network Training on ReRAM-based Processing-in-Memory Accelerators. ACM Trans. Des. Autom. Electron. Syst. 29, 5, Article 72 (September 2024), 29 pages. https://doi.org/10.1145/3656171, **Highlight paper** (IF: 2.22)
5. A. Jaiswal, K. C. S. Shahana, **S. Ravichandran**, K. Adarsh, H. B. Bhat, **B. K. Joardar**, S. K. Mandal, "HALO: Communication-aware Heterogeneous 2.5D System for Energy-efficient LLM Execution at Edge," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, doi: 10.1109/JETCAS.2024.3427421, **Spotlight paper**, (IF: 4.34)

6. C. -Y. Chen, **B. K. Joardar**, J. R. Doppa, P. P. Pande and K. Chakrabarty, "Mitigating Slow-to-Write Errors in Memristor-Mapped Graph Neural Networks Induced by Adversarial Attacks," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2024, doi: 10.1109/TCAD.2024.3372444, (IF: 2.8)
7. **B. K. Joardar,** T. K. Bletsch and K. Chakrabarty, "Machine Learning-Based Rowhammer Mitigation," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 42, no. 5, pp. 1393-1405, May 2023, doi: 10.1109/TCAD.2022.3206729, (IF: 2.8)
8. **B. K. Joardar,** J. R. Doppa, H. Li, K. Chakrabarty and P. P. Pande, "ReaLPrune: ReRAM Crossbar-Aware Lottery Ticket Pruning for CNNs," in IEEE Transactions on Emerging Topics in Computing, vol. 11, no. 2, pp. 303-317, 1 April-June 2023, doi: 10.1109/TETC.2022.3223630, (IF: 5.1)
9. C. Ogbogu, A. I. Arka, L. Pfromm, **B. K. Joardar**, J. R. Doppa, H. Li, K. Chakrabarty, P. P. Pande, "Accelerating Graph Neural Network Training on ReRAM-based PIM Architectures via Graph and Model Pruning," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 42, no. 8, pp. 2703-2716, Aug. 2023, doi: 10.1109/TCAD.2022.3227879 (IF: 2.8)
10. C. Ogbogu, A. I. Arka, **B. K. Joardar**, J. R. Doppa, H. Li, K. Chakrabarty, P. P. Pande, "Accelerating Large-Scale Graph Neural Network Training on Crossbar Diet," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 41, no. 11, pp. 3626-3637, Nov. 2022, doi: 10.1109/TCAD.2022.3197342 (IF: 2.8)
11. **B. K. Joardar**, J. R. Doppa, H. Li, K. Chakrabarty and P. P. Pande, "Learning to Train CNNs on Faulty ReRAM-based Manycore Accelerators," in ACM Trans. Embed. Comput. Syst., 20, 5s, Article 55, August 2021, 23 pages, (as part of ESWEEK 2021), https://doi.org/10.1145/3476986, (IF: 2.8)
12. **B. K. Joardar,** A. Deshwal, J. R. Doppa, P. P. Pande and K. Chakrabarty, "High-Throughput Training of Deep CNNs on ReRAM-Based Heterogeneous Architectures via Optimized Normalization Layers," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 41, no. 5, pp. 1537-1549, May 2022, doi: 10.1109/TCAD.2021.3083684, (IF: 2.8).
13. **B. K. Joardar**, J. R. Doppa, P. P. Pande, H. Li and K. Chakrabarty, "AccuReD: High Accuracy Training of CNNs on ReRAM/GPU Heterogeneous 3-D Architecture," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 40, no. 5, pp. 971-984, 2021, doi: 10.1109/TCAD.2020.3013194 (IF: 2.8).
14. A. I. Arka, **B. K. Joardar**, R. G. Kim, D. H. Kim, J. R. Doppa, and P. P. Pande, "HeM3D: Heterogeneous Manycore Architecture Based on Monolithic 3D Vertical Integration," in Transactions on Design Automation of Electronic Systems, 26, 2, Article 16, 2021, https://doi.org/10.1145/3424239 (IF: 2.22).
15. A. I. Arka, **B. K. Joardar**, J. R. Doppa, P. P. Pande and K. Chakrabarty, "Performance and Accuracy Trade-offs for Training Graph Neural Networks on ReRAM-based Architectures," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 29, no. 10, pp. 1743-1756, Oct. 2021, doi: 10.1109/TVLSI.2021.3110721 (IF: 3.2)
16. **B. K. Joardar**, R. G. Kim, J. R. Doppa, P. P. Pande, D. Marculescu and R. Marculescu, "Learning-based Application-Agnostic 3D NoC Design for Heterogeneous Manycore Systems," in IEEE Transactions on Computers, vol. 68, no. 6, pp. 852-866, 2019 (IF: 3.7)
17. A. Deshwal, N. K. Jayakodi, **B. K. Joardar**, J. R. Doppa, and P. P. Pande, "MOOS: A Multi-Objective Design Space Exploration and Optimization Framework for NoC Enabled Manycore Systems," in ACM Trans. Embed. Comput. Syst. 18, 5s, Article 77, 2019 (IF: 2.8)

Conference Publications:

17. **P. Edara**, L. Wang, **S. Duttala, B.K. Joardar**, *Name not disclosed due to double blind requirements*, in IEEE 2025 Design, Automation & Test in Europe Conference & Exhibition (DATE), (under review)
18. **M. Heidary, B. K. Joardar**, *Name not disclosed due to double blind requirements*, in International Symposium on Quality Electronic Design (ISQED), (under review)
19. **M. Heidary** and **B. K. Joardar**, "Hardware Attacks on ReRAM-Based AI Accelerators," 2024 IEEE 17th Dallas Circuits and Systems Conference (DCAS), TX, USA, 2024, pp. 1-4, doi: 10.1109/DCAS61159.2024.10539864
20. P. Dhingra, C. Ogbogu, **B. K. Joardar**, J. R. Doppa, A. Kalyanaraman and P. P. Pande, "FARe: Fault-Aware GNN Training on ReRAM-Based PIM Accelerators," *2024 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Valencia, Spain, 2024, pp. 1-6, doi: 10.23919/DATE58400.2024.10546762
21. C. Ogbogu,M. Soumen, **B. K. Joardar**, J. R. Doppa, D. Heo, K. Chakrabarty, P. P. Pande, "Energy-Efficient ReRAM-Based ML Training via Mixed Pruning and Reconfigurable ADC," 2023 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), Vienna, Austria, 2023, pp. 1-6
22. E. Ortega, T. Bletsch, **B. Joardar**, J. Talukdar, W. Paik and K. Chakrabarty, "Simply-Track-and-Refresh: Efficient and Scalable Rowhammer Mitigation," 2023 IEEE International Test Conference (ITC), CA, USA, 2023, pp. 340-349

23. **B. K. Joardar**, and K. Chakrabarty, “Attacking ReRAM-based Architectures using Repeated Writes,” in Design, Automation & Test in Europe Conference & Exhibition (DATE), 2023
24. C. H. Tung, **B. K. Joardar**, P. P. Pande, J. R. Doppa, H. Li, K. Chakrabarty, “Dynamic Task Remapping for Reliable CNN Training on ReRAM Crossbars,” in Design, Automation & Test in Europe Conference & Exhibition (DATE), 2023
25. C. Y. Chen, **B. K. Joardar**, J. R. Doppa, P. P. Pande, K. Chakrabarty, “Attacking Memristor-mapped Graph Neural Network by Inducing Slow-to-Write Errors,” in European Test Symposium (ETS), 2023
26. B. K. Joardar, a. I. Arka, J. R. Doppa, and P. P. Pande, “Fault-Tolerant Deep Learning Using Regularization,” in Proceedings of the 41st IEEE/ACM International Conference on Computer-Aided Design (ICCAD '22), New York, NY, USA, Article 159, 1–6, 2022.
27. **B. K. Joardar**, T. K. Bletsch and K. Chakrabarty, "Learning to Mitigate Rowhammer Attacks," in Design, Automation & Test in Europe Conference & Exhibition (DATE), 2022, pp. 564-567.
28. **B. K. Joardar**, J. Rao Doppa, P. P. Pande and K. Chakrabarty, "NoC-enabled 3D Heterogeneous Manycore Systems for Big-Data Applications," in 23rd International Symposium on Quality Electronic Design (ISQED), 2022, pp. 1-6.
29. **B. K. Joardar**, A. I. Arka, J. R. Doppa, P. P. Pande, H. Li, and K. Chakrabarty, “Processing-in-Memory enabled Heterogeneous Manycore Architectures for Deep Learning: From CNNs to GNNs”, in International Conference on Computer Aided Design (ICCAD), 2021
30. A. I. Arka, **B. K. Joardar**, J. R. Doppa, P. P. Pande and K. Chakrabarty, “DARe: DropLayer-Aware Manycore ReRAM Architecture for Training Graph Neural Networks,” in International Conference on Computer Aided Design (ICCAD), 2021.
31. X. Yang, S. Belakaria, **B. K. Joardar**, H. Yang, J. R. Doppa, P. P. Pande, K. Chakrabarty and H. Li, “Multi-Objective Optimization of ReRAM Crossbars for Robust DNN Inferencing under Stochastic Noise,” in International Conference on Computer Aided Design (ICCAD), 2021.
32. **B. K. Joardar**, A. I. Arka, J. R. Doppa and P. P. Pande, “3D++: Unlocking the Next Generation of High-Performance and Energy-Efficient Architectures using M3D Integration,” in Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 2021
33. A. I. Arka, **B. K. Joardar**, J. R. Doppa, P. P. Pande and K. Chakrabarty, “ReGraphX: NoC-enabled 3D Heterogeneous ReRAM Architecture for Training Graph Neural Networks,” in Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 2021 (**Best Paper Award Nomination**).
34. **B. K. Joardar**, N. K. Jayakodi, J. R. Doppa, H. Li, P. P. Pande and K. Chakrabarty, “GRAMARCH: A GPU-ReRAM based Heterogeneous Architecture for Neural Image Segmentation,” in Proceedings of 23rd IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition (DATE), 2020 (**Best Paper Award Nomination**)
35. **B. K. Joardar**, P. Ghosh, P. P. Pande, A. Kalyanaraman and S. Krishnamoorthy, “NoC-enabled Software/Hardware Co-Design Framework for Accelerating k-mer Counting,” International Symposium on Networks-on-Chip (NOCS '19), New York, NY, USA, 2019 (**Best Paper Award**)
36. P. Bogdan, F. Chen, A. Deshwal, J. R. Doppa, **B. K. Joardar**, H. Li, S. Nazarian, L. Song, and Y. Xiao, “Taming extreme heterogeneity via machine learning based design of autonomous manycore systems,” in Proceedings of the International Conf. on Hardware/Software Codesign and System Synthesis Companion (CODES/ISSS), 2019
37. **B. K. Joardar**, A. Deshwal, J. R. Doppa and P. P. Pande, "A Machine Learning Framework for Multi-Objective Design Space Exploration and Optimization of Manycore Systems," 2019 ACM/IEEE 1st Workshop on Machine Learning for CAD (MLCAD), Canmore, AB, Canada, 2019, pp. 1-6
38. **B. K. Joardar**, R. G. Kim, J. R. Doppa, P. P. Pande, “Design and Optimization of Heterogeneous Manycore Systems enabled by Emerging Interconnect Technologies: Promises and Challenges,” Proceedings of 22nd IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019
39. **B. K. Joardar**, B. Li, J. R. Doppa, H. Li, P. P. Pande and K. Chakrabarty, “REGENT: A Heterogeneous ReRAM/GPU-based Architecture Enabled by NoC for Training CNNs,” Proceedings of 22nd IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, 2019
40. **B. K. Joardar**, J. R. Doppa, P. P. Pande, D. Marculescu and R. Marculescu, “Hybrid On-Chip Communication Architectures for Heterogeneous Manycore Systems,” Proceedings of 37th IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2018.
41. **B. K. Joardar**, K. Duraisamy and P. P. Pande, "High performance collective communication-aware 3D Network-on-Chip architectures," 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, 2018

42. **B. K. Joardar**, W. Choi, R. G. Kim, J. R. Doppa, P. P. Pande, D. Marculescu and R. Marculescu, "3D NoC-enabled heterogeneous manycore architectures for accelerating CNN training: Performance and thermal trade-offs," 2017 Eleventh IEEE/ACM International Symposium on Networks-on-Chip (NOCS), Seoul, 2017

PRESENTATIONS/POSTERS AND INVITED TALKS

- Invited talks at NCSU, UC Irvine, UT Dallas, UC Riverside, Boston University, Iowa State University
- Poster presentation at SRC annual event (2021, 2022).
- Presented my research at multiple conferences including DATE (2018, 2019, 2020, 2022, 2023), ICCAD (2022), NOCS (2019), DCAS 2024.
- Presented poster at Cadence Design Systems (2019).

AWARDS and ACCOMPLISHMENTS

- Selected for the DAAD AInet Fellowship, Awarded by DAAD, 2021
- Best Paper Award Nomination, DATE 2020 and DATE 2021
- Received the CI-Fellowship for Postdoctoral research, Awarded by CRA and CCC, 2020
- Won the Best Paper Award, NOCS 2019
- Outstanding Graduate Student Researcher award, Voiland College of Engineering and Architecture, Washington State University, 2019
- Harold and Dianna Frank Electrical Engineering Fellowship, Washington State University, 2018