

Extending the reach of RISC-V with Renode & Zephyr, on Earth and beyond

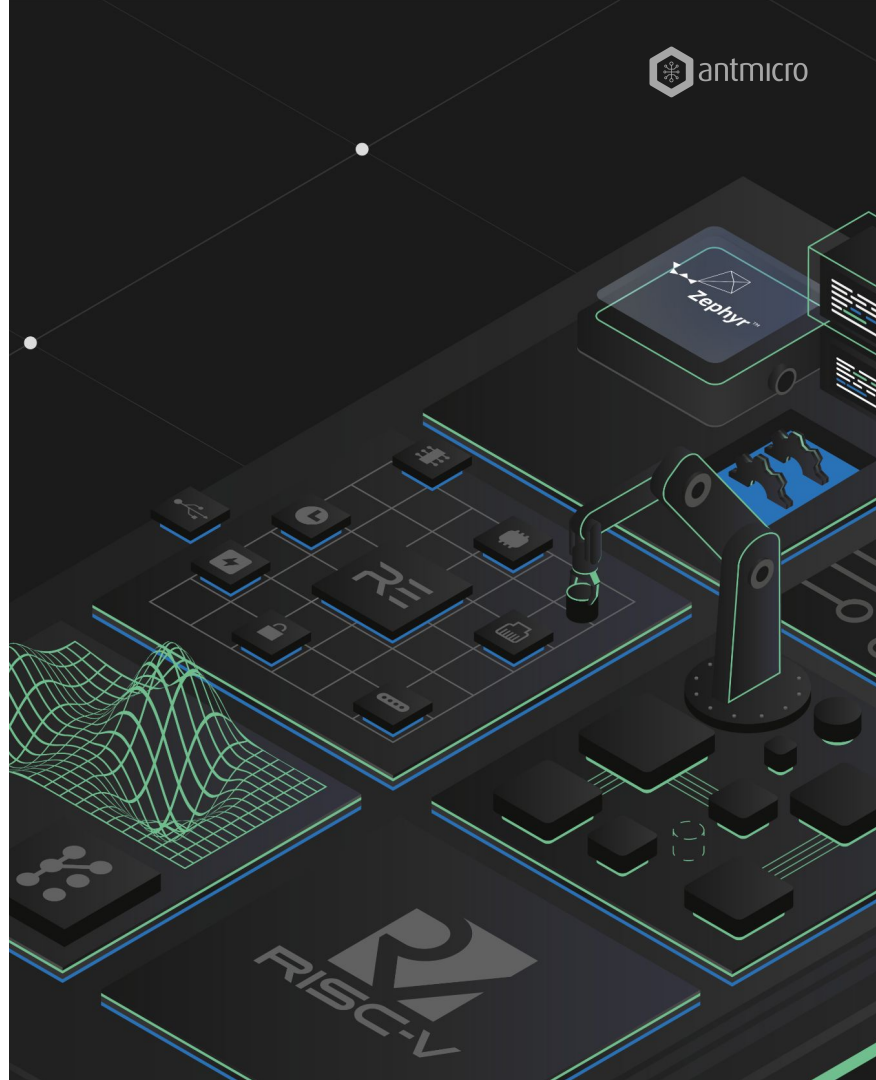
Göteborg RISC-V Meetup #3, 2024-02-20

Michael Gielda, mgielda@antmicro.com



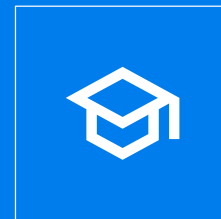
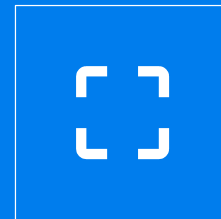
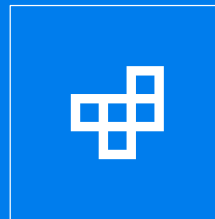
ANTMICRO

- Founded in 2009, dedicated to open source in a pragmatic and commercial approach
- Around 130 people (now also in Gothenburg - Citygate), SW-driven company with extensive HW know-how - developing complete systems
- We provide end-to-end engineering services, advanced tooling and platform development and strategic R&D for high-tech products
- Heavily involved in RISC-V, Zephyr, open source hardware/FPGA/ASIC - members of CHIPS Alliance, RISC-V International, Zephyr project



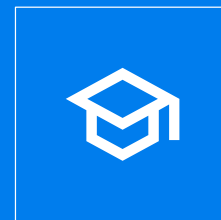
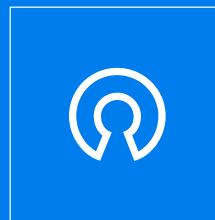
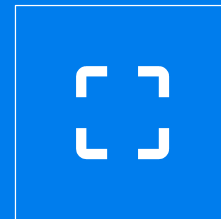
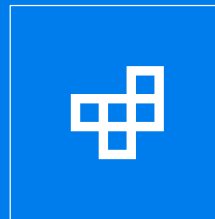
WHY DO PEOPLE PICK RISC-V?

- Customizability and flexibility - can be freely adapted, versatile framework/ecosystem rather than just a “technology”
- Scalability - start with small cores, scale to any use case, including very complex ones
- Openness - share everything freely, no licensing restrictions
- Lack of barrier to entry - experiment without up front investment, meshes well with academia and research, industrial R&D



WHY DO PEOPLE PICK RISC-V, RENODE AND ZEPHYR

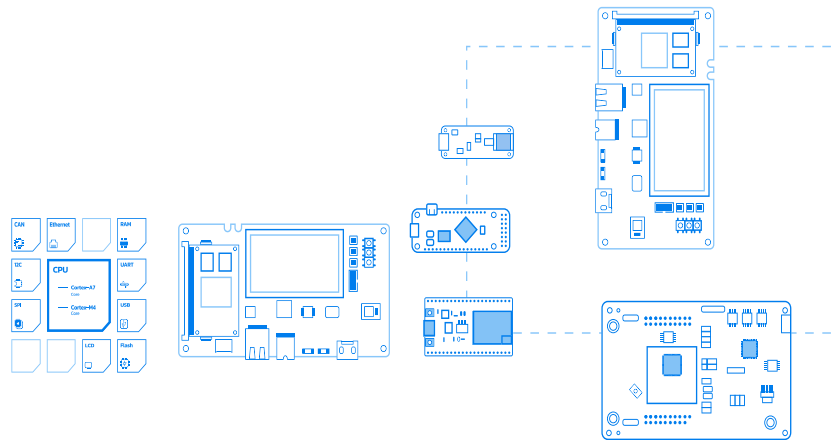
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- **As RISC-V, Renode and Zephyr share those qualities, they go along very well!**



SO WHAT IS RENODE?

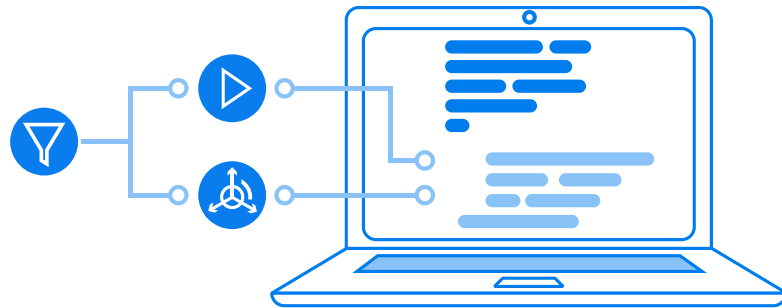
- **Renode** is our flagship open-source system development framework featuring software/hardware/FPGA/ASIC co-simulation capability for the flexible and rapid design of heterogeneous systems
- It supports various CPU and I/O IP, sensor, network building blocks — you can quickly build and simulate entire SoCs/systems before actually implementing them
- We offer commercial support and engineering services around Renode and integrating it into various interactive and CI workflows

RENODE™



SUPPORTS COMPLEX, MULTI-NODE ENVIRONMENTS

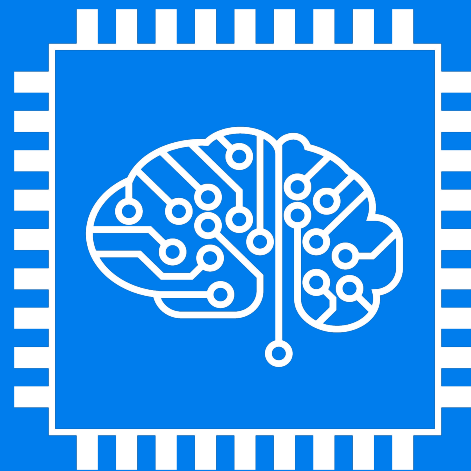
- Renode allows to design and test sophisticated **multi-node environments**, heterogeneous, multi-ISA; complete products
- Full-system, binary-compatible simulation, software agnostic - but meshes best with open source like Zephyr!
- Full inspection of SW behaviour and robust event **tracing mechanisms**
- **Lets you debug simulated applications with GDB**, also for multiple nodes at the same time



RENODE FOR CUSTOMIZED RISC-V DEVELOPMENT

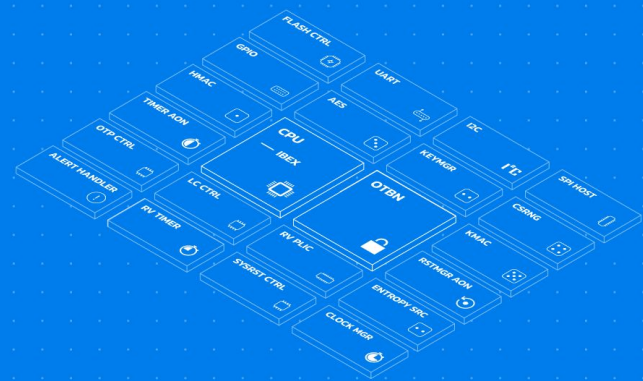
- Renode helps develop end products but also e.g. SoCs, security IP or ML solutions, especially based on RISC-V
- Supports [RISC-V Vector extensions](#)
- Many ways of adding RISC-V Custom Instructions - including Python one-liners - and [Custom Function Units](#) for HW/SW ML co-development
- Renode together with [Kenning](#) enables [co-development of RISC-V AI accelerators and testing of ML flows](#) in a fully automated, reproducible and consistent manner - Kenning now **includes Zephyr runtime with TVM!**

 RISC-V



RENODE IN RISC-V PROJECTS

- Prominently supports Microchips PolarFire SoC - with Zephyr and complete FPGA co-development flow - see our talk at EOSS/ZDS in Seattle in April (right before LatchUp in Boston)! <https://sched.co/1aBFb>
- Very good support for SiFive platforms
- Great support for [OpenTitan](#)
 - and, as a consequence, [Open Se Cura](#)
- (we're also working with Caliptra, which is Microsoft+Google+AMD+NVIDIA, the core is called VeeR, and we [just added PMP to it](#))



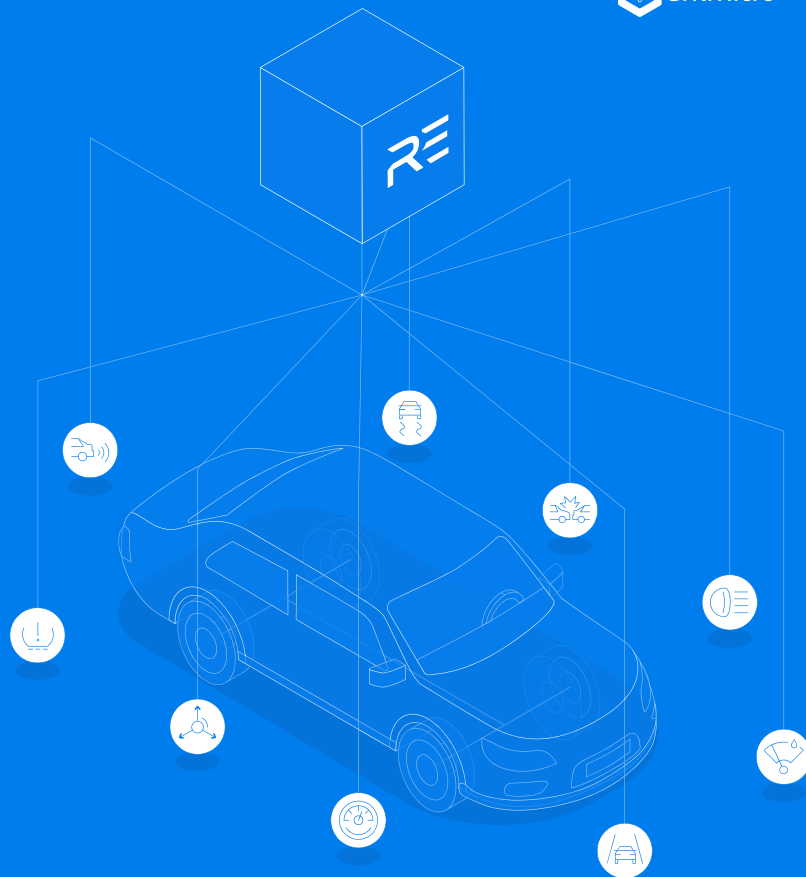
RENODE FOR PROTOTYPING AND HARDWARE DEVELOPMENT

- Renode can **co-simulate with Verilator**, including **simulating CPUs directly from RTL**, as well as to emulate with physical peripherals
- **Supports DPI** to integrate with simulators such as Verilator, Questa, Vivado or VCS
- Despite being an ISS, Renode also **supports trace-based augmentation of execution data**, useful for pre-silicon HW/SW co-design and performance evaluation
- Broad support for RISC-V but also ARM and other popular platforms



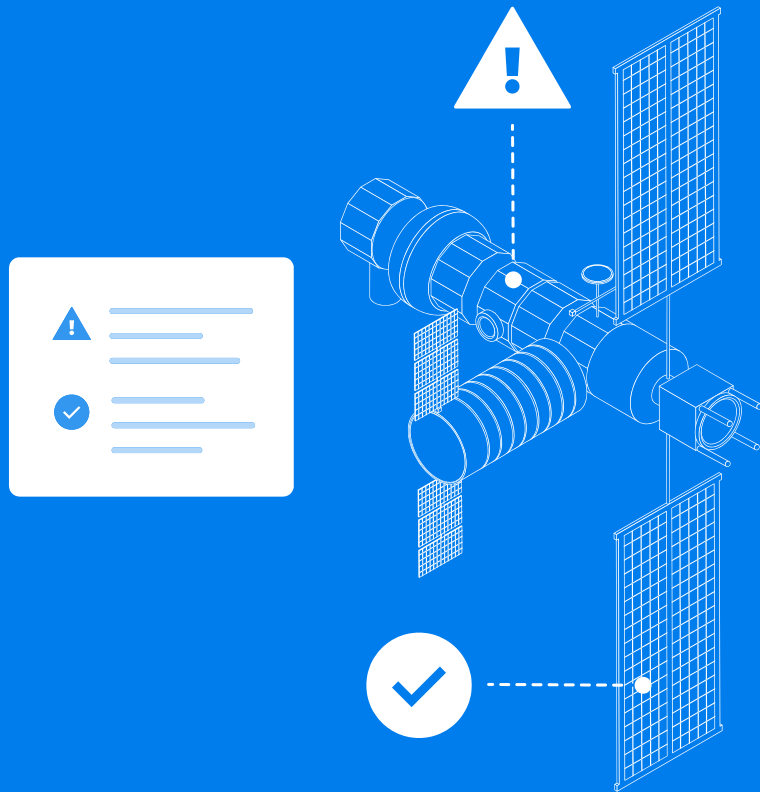
AGENT OF CHANGE: RENODE FOR AUTOMOTIVE

- Renode is gaining traction in new automotive applications, software driven and electric cars
- Key features: ability to mix architectures, simulate multi-node systems, debugging features
- Also agent for Zephyr / open source OS adoption
- Helping build new, tailored silicon devices, evaluate choice of CPUs for specific algorithms
- Used as demonstrator for capabilities of RISC-V product portfolios
- Dedicated blog note:
<https://antmicro.com/blog/2023/12/multi-node-development-in-renode-for-automotive-use-cases/>



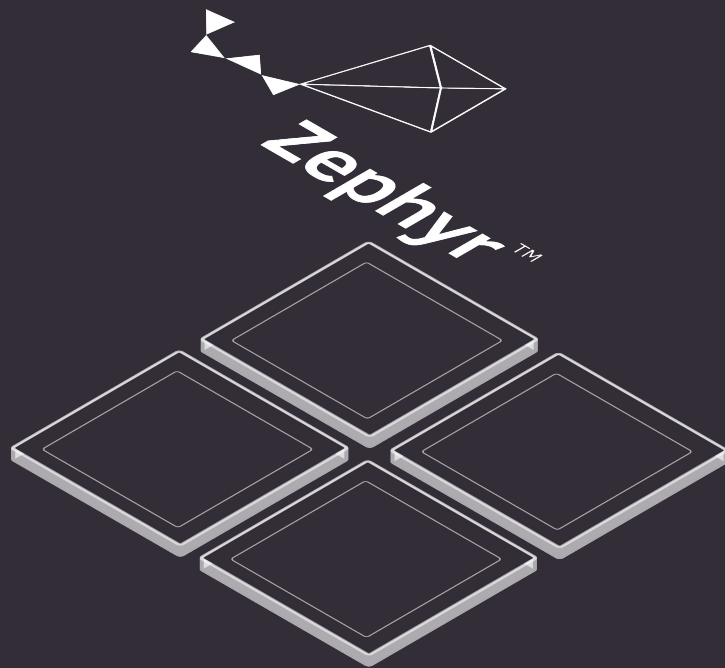
AGENT OF CHANGE: RENODE FOR SPACE

- Renode is also seeing incredible adoption in space
- Good match: multiple ISAs, FPGA co-simulation, multi-node systems, lot of testing!
- RISC-V is a rising star there as well, and Renode is helping establish its footprint
 - ARC, Microblaze, LEON and other proprietary options slowly fading away, replaced with RISC-V
- Seeing a lot of space ROS, looking forward to more Zephyr adoption
- Dedicated blog note:
<https://antmicro.com/blog/2024/02/developing-and-testing-space-systems-with-renode/>



ZEPHYR

- For those of you that don't know...
- ... where have you been hiding?
- Zephyr RTOS is the world's fastest growing RTOS, most commits, developers, boards...
- Focused on security, standardization, portability
- Pushing for Zephyr to be the “de-facto” standard for RISC-V (alongside Linux)



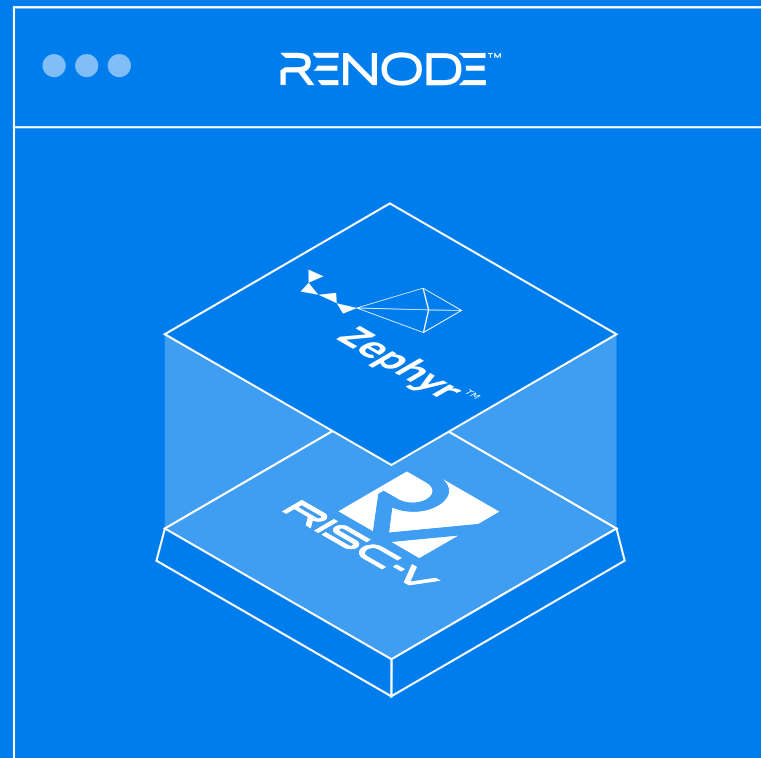
ZEPHYR AND RISC-V

- Antmicro maintains the RISC-V ISA in Zephyr
 - your contributions to SoCs and arch port will likely go through our review
- We're working on improving the ease of use
 - ISA modularity
 - soft CPUs, soft SoCs
- Helping test Zephyr with Renode
 - helps ensure stability and fitness of platforms and drivers (not only cores!)
 - default testing platform for many Zephyr platforms, especially RISC-V



RENODE HELPS RISC-V IN ZEPHYR

- Co-developing support for RISC-V both in Zephyr and Renode
 - ISA strings added as part of DTS for all RISC-V platforms in Zephyr
 - improved platform descriptions for better consistency and analyzability
 - improved a range of peripheral models
- Renode-specific virtual target contributed by Meta, for increased ease of use and modularity comparing to other simulators



ZEPHYR + RENODE = DASHBOARD

- A great example of the power of Zephyr and Renode used together for testing at scale:
- zephyr-dashboard.renode.io
- Presents auto-generated Zephyr examples and tests passing on >430 platforms in Renode
- Visualizes the data in a matrix view and allows for easy local reproduction
- Leverages device trees used in Zephyr to describe build targets
- Helps improve RISC-V HW descriptions in Zephyr!

Search...	435 PASSED	408 PASSED	360 PASSED	425
BOARD NAME	HELLO WORLD	PHILOSOPHERS	SHELL MODULE	TENSO
RISCV64 (4) ▼				
Beagleboard BeagleV-Fire	PASSED	PASSED	PASSED	P
Microchip PolarFire ICICLE kit	PASSED	PASSED	PASSED	P
SiFive HiFive Unleashed	PASSED	PASSED	PASSED	P
SiFive HiFive Unmatched	PASSED	PASSED	PASSED	P
RISCV32 (27) ▼				
Andes ADP-XC7K AE350	PASSED	GENERATED	PASSED	P
ESP32-C3	BUILT	BUILT	BUILT	
ESP32C3 LuatOS Core	BUILT	BUILT	BUILT	
ESP32C3 LuatOS Core USB	BUILT	BUILT	BUILT	
GigaDevice GD32VF103C-STARTER	GENERATED	GENERATED	GENERATED	GE
GigaDevice GD32VF103V-EVAL	GENERATED	GENERATED	GENERATED	GE
ICE-V Wireless	BUILT	BUILT	BUILT	
INTEL FPGA Nios V/g general purpose processor	PASSED	GENERATED	GENERATED	P
INTEL FPGA niosv_m	PASSED	GENERATED	GENERATED	P
ITE IT82XX2 EVB	BUILT	BUILT	BUILT	

UBOOT DASHBOARD

- Similarly to the Zephyr Dashboard, the U-Boot Dashboard applies this concept for boards supported in U-Boot
- u-boot-dashboard.renode.io
- Great source of extra data, especially for boards that are also supported in Zephyr
- Proves the approach is generic and can be expanded to other types of software

Search...

148 PASSED

BOARD NAME

U-BOOT

RISCV (21)

SiFive HiFive Unleashed A00

PASSED

Microchip PolarFire-SoC Icicle Kit

BUILT

openpiton_riscv64--openpiton-riscv64

BUILT

openpiton_riscv64_spl--openpiton-riscv64

BUILT

qemu-riscv64--qemu-virt64

BUILT

qemu-riscv64_smode--qemu-virt64

BUILT

qemu-riscv64_spl--qemu-virt64

BUILT

SiFive HiFive Unmatched A00

BUILT

Sipeed Lichee Pi 4A

BUILT

starfive_visionfive2--jh7110-starfive-visionfive-2

BUILT

ae350_rv32--ae350_32

NOT BUILT

ae350_rv32_spl--ae350_32

NOT BUILT

ae350_rv32_spl_xip--ae350_32

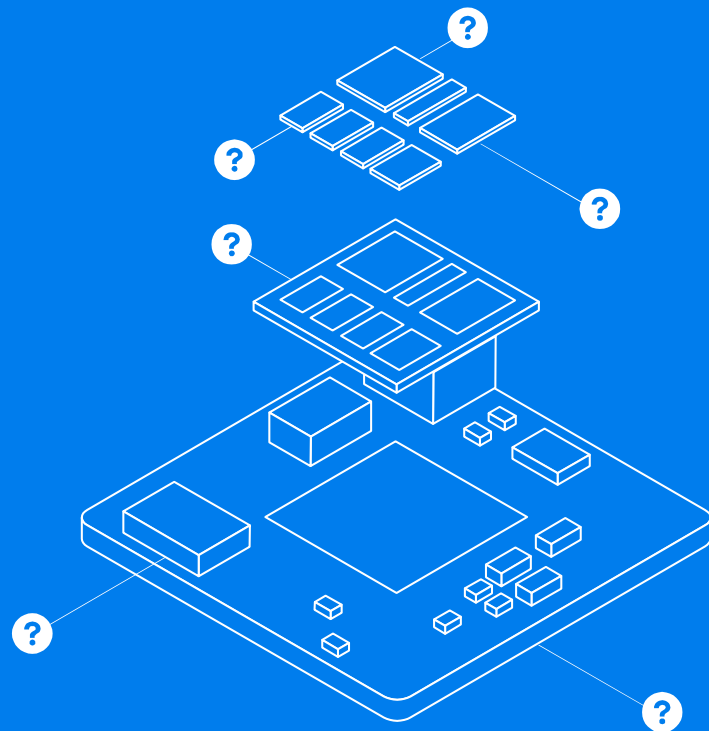
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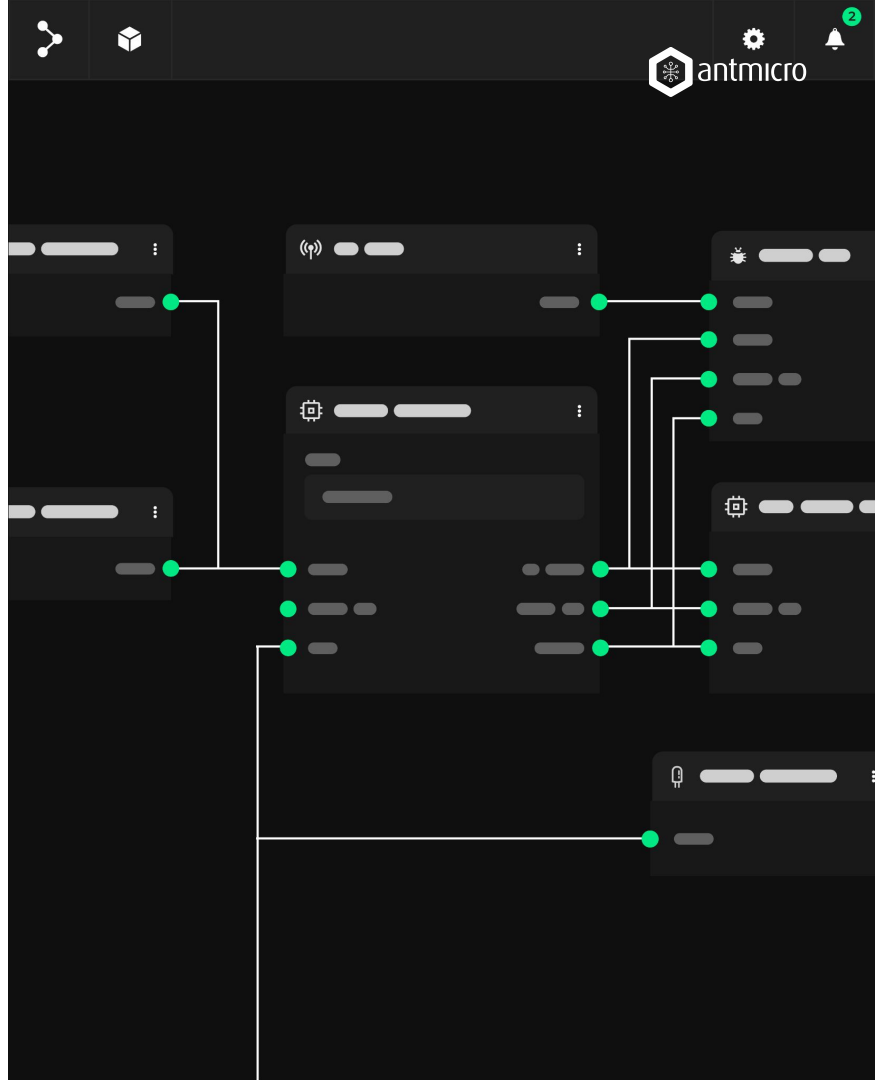
RENODEPEDIA

- [Renodepedia](#) - Antmicro's encyclopedia of hardware - SoCs, boards, IP blocks
- Cataloging HW ecosystem, exposing structure - especially great for open source hardware and RISC-V ecosystem
- Based on automated data e.g. device trees from our [Zephyr Dashboard CI](#):
 - Discover connections between components
 - Navigate dependencies
 - Show commonalities and SW payloads
 - Simulate in Renode



VISUAL SYSTEM DESIGNER

- An open source tool, based on Antmicro's open source component and platform database, using [Pipeline Manager](#), [visual diagramming tool for AI](#)
- [Visual System Designer](#) enables a visual, formalized way to build embedded systems from defined building blocks - and generating Zephyr firmware and tests from the system description!
- Design hardware block diagrams that use a unified specification file containing different component types
- Co-develop hardware and software for Machine Learning scenarios with RISC-V features



PREDICTING THE FUTURE

- Always a bad idea but I'll try anyway
- Systems will converge around Zephyr (and Linux) and other open options (of course will never get close to 100% adoption, diversity is good)
- RISC-V will continue to grow rapidly, alongside ARM for the foreseeable future, custom architectures will go away except extreme niches
- More software-driven chips!
- Hoping for even more Renode adoption - start using it today (and talk to me tonight)!





**THANK YOU
FOR YOUR ATTENTION!**

