3

Metal-Oxide-Semiconductor System

3.1 Introduction

The metal-oxide-semiconductor (MOS) structure, commonly referred to as the MOS capacitor, is a two-terminal device with one electrode connected to the metal and the other electrode connected to the semiconductor, forming a voltage-dependent capacitor. The acronym MOS is used even if the top electrode is not a metal and the insulator is not an oxide. An MOS capacitor is a very useful device both for evaluating the MOS integrated circuit (IC)–fabrication process and for predicting the MOS transistor performance. Therefore, MOS capacitors are included in the test chip for IC process and device characterization.

The MOS capacitor systems have been the subject of numerous investigations and the detailed description of the early development can be found in the literature [1]. The major objective of this chapter is to build the foundation for the development of MOS transistor theory and models that will be used in Chapters 4, 5, and 9. In order to achieve our objective, we first discuss the behavior of an MOS capacitor system and then develop the charge-voltage (Q–V) and capacitance-voltage (C–V) relationships, which will be used later in the development of MOS transistor model.

3.2 MOS Capacitor at Equilibrium

In order to describe the basic performance of MOS capacitor system, let us consider the two-dimensional (2D) cross section of an ideal MOS capacitor shown in Figure 3.1. The structure includes a p- or n-type semiconductor substrate such as silicon, a dielectric layer such as silicon dioxide (SiO_2), a metal or polysilicon gate, a gate electrode (G), and a body (back or bulk) electrode (B) for operating the MOS capacitor system at the intended applied bias V_g and V_b. Typically, the SiO_2 layer is thermally grown on silicon substrate with a typical thickness between 10 and 100 nm. The gate

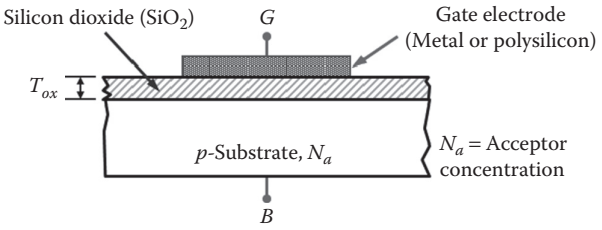

FIGURE 3.1
2D cross section of an ideal MOS capacitor structure fabricated on a uniformly doped *p*-type substrate with doping concentration, N_a; here *G* and *B* denote the gate and body electrodes for applied biases to the gate and substrate, respectively.

metal or degenerately doped polysilicon or a combination of polysilicon and silicide (e.g., $TiSi_2$, $CoSi_2$) is formed on the top of the gate dielectric by masking, photolithography, and annealing processes. The body electrode is obtained by deposited metal to achieve an ohmic contact. If the substrate conducts sufficiently to support the displacement currents, the structure in Figure 3.1 forms a parallel-plate capacitor with *G* as one electrode, *B* as the second electrode, and SiO_2 as the dielectric. This is referred to as the MOS capacitor system. This system is in thermal equilibrium with applied DC bias, and if the change in voltage is sufficiently slow, it is approximated to be a constant. Thus, from the parallel-plate capacitance formulation, we can write the oxide capacitance (C_{ox}) per unit area between the metal and silicon surface as:

$$C_{ox} = \frac{\varepsilon_0 K_{ox}}{T_{ox}} \tag{3.1}$$

where:
ε_0 is the permittivity of free space or vacuum
K_{ox} is the dielectric constant of oxide
T_{ox} is the gate oxide thickness

In order to study the behavior of MOS capacitor system, let us consider the metal, oxide, and semiconductor (*p*-type silicon) as three separate materials, that is, materials before brought into contact. The energy band diagram of each material is shown separately in Figure 3.2. In Figure 3.2, E_0 denotes a convenient reference potential energy level, which is the vacuum or free electron energy level. In reality, E_0 is the level at which the Coulombic potential of an isolated positive charge becomes zero. It is to be noted that the reported value of bandgap energy for SiO_2 layer is in the range of 8.0–9.0 eV [1–3]. In Figure 3.2, we have used 8.0 eV as the bandgap energy for SiO_2 to discuss the behavior of MOS capacitor. The other characteristic parameters of the three materials in Figure 3.2 are defined in the next subsection.

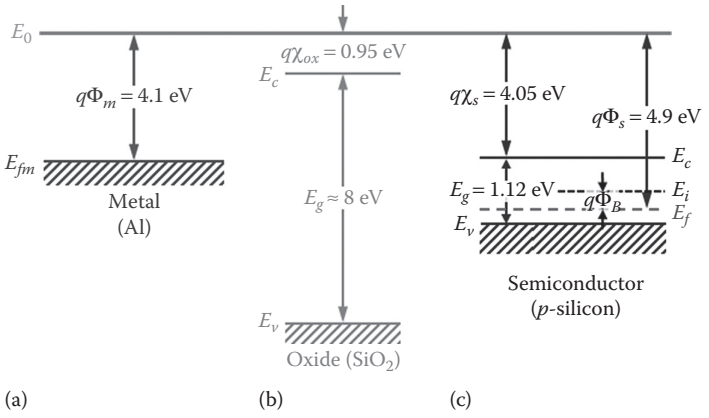

FIGURE 3.2
The energy band diagram of three separate materials that form an MOS capacitor system: (a) aluminum, (b) thermally grown SiO_2, and (c) *p*-type silicon substrate with $N_a = 1 \times 10^{15}\,cm^{-3}$; here, E_0 = vacuum energy level (reference energy), E_c = bottom edge of conduction band, E_v = top-edge of valence band, E_f = Fermi level, E_g = forbidden energy (energy gap), E_i = Intrinsic energy level, $E_{fm} = E_c$ = Fermi level in metal; Φ_m = metal work function, χ_s = electron affinity in silicon, χ_{ox} = electron affinity in oxide, Φ_s = semiconductor work function, and q = electronic charge.

3.2.1 Work Function

Figure 3.2 shows the energy band diagrams of the metal, oxide, and semiconductor materials relative to vacuum level, E_0. In Figure 3.2a, Φ_m is defined as the metal work function in units of volts or ($q\Phi_m$) in units of energy. Φ_m is the energy required to take an electron across the surface energy barrier of metal at the Fermi level E_{fm} to E_0. However, for a metal, the Fermi level E_{fm} is at E_c. Thus, Φ_m is the energy difference between E_0 and E_{fm}, that is $\left(q\Phi_m = E_0 - E_{fm}\right)$. For pure metals without impurities and contamination, the value of Φ_m depends only on the charge distribution of the atomic core or the type of atom involved. For aluminum metal shown in Figure 3.2a, the value of $\Phi_m = 4.10\,V$.

In semiconductors and insulators, the height of the surface energy barrier is defined by electron affinity, χ_s and χ_{ox} as shown in Figure 3.2c and b, respectively. As shown in Figure 3.2b and c, χ is the energy difference between the vacuum level E_0 and the bottom of the conduction band edge E_c at the surface, and for a semiconductor material, $q\chi_s = \left(E_0 - E_c\right)$. And, χ defines the basic property of a material independent of the presence of impurities or imperfections and only varies from one atomic type to another or is changed by alloy composition. Unlike metals, the Fermi level, E_f, is not a constant in semiconductors and depends on the doping concentration of impurities. Since the work function is the energy required to take an electron from E_f to E_0, the electron affinity χ_s is used to define the work function Φ_s in semiconductors. Thus, for a *p*-type semiconductor, the work function is given by

$$q\Phi_{sp} = q\chi_s + \frac{E_g}{2} + q\phi_{Bp} \quad (p\text{-type semiconductor}) \tag{3.2}$$

where:
E_g is the bandgap energy
ϕ_{Bp} is the bulk or Fermi potential for a p-type semiconductor

Similarly, the work function for an n-type semiconductor is given by

$$q\Phi_{sn} = q\chi_s + \frac{E_g}{2} - q\phi_{Bn} \quad (n\text{-type semiconductor}) \tag{3.3}$$

where:
ϕ_{Bn} is the bulk or Fermi potential for an n-type semiconductor

If the doping concentration for both the n-type and p-type semiconductors is the same, then $|\phi_{Bp}| = |\phi_{Bn}| \equiv \phi_B$ and is given by Equation 2.70 as

$$\phi_B = v_{kT} \ln\left(\frac{N_b}{n_i}\right) \tag{3.4}$$

where:
$v_{kT}\,(= kT/q)$ is the *thermal voltage* at the ambient temperature T
n_i is the intrinsic carrier concentration

In v_{kT}, the parameters k and q represent the Boltzmann constant and electronic charge, respectively. In order to calculate the value of the semiconductor work function, Φ_s, the magnitude of ϕ_B is calculated from Equation 3.4 as shown in the following example.

Let us consider a p-type silicon with $N_b = N_a = 1 \times 10^{15}\,\text{cm}^{-3}$ at room temperature 300 K so that $v_{kT} \cong 0.0259$ V. Then using $n_i = 1.45 \times 10^{10}\,\text{cm}^{-3}$, we can show from Equation 3.4 that the value of $\phi_B \cong 0.29$ V. Now, considering $q\chi_s = 4.05$ eV and $E_g = 1.12$ eV for silicon, we get from Equation 3.2, $q\Phi_{sp} \equiv q\Phi_s \cong 4.90$ eV. For aluminum, $q\Phi_m = 4.1$ eV; therefore, for a p-type silicon, $\Phi_m < \Phi_s$, that is, the energy required to free an electron from the p-type silicon is higher than the energy required to free an electron from aluminum.

In order to calculate Φ_s for polysilicon gate, it is assumed that the polysilicon is degenerately doped so that the Fermi energy lies at the band edges, that is, E_f is at E_c for an n-type polysilicon and E_f is at E_v for a p-type polysilicon. For nanoscale CMOS (complementary metal-oxide-semiconductor) technology, work function engineering is used to achieve the target value of metal gate work function [4]. The work functions of commonly used gate material for IC technology are shown in Table 3.1 [5,6].

Now, let us consider the energy bands of three materials shown in Figure 3.2a–c are brought in contact to form an MOS capacitor system. It can be shown that when different materials are in contact with each other, the work

TABLE 3.1

Work Function of Different Materials Used as Gate Materials

Material	Work Function (eV)
Al	4.10
Au	5.27
$MoSi_2$	4.73
$TiSi_2$	3.95
n-type degenerately doped polysilicon	4.05
p-type degenerately doped polysilicon	5.17

function between the two ends of the composite system of materials depends only on the first and the last materials [7]. Thus, for an MOS system, the work function difference between the metal and the semiconductor defines the behavior of the system. The work function difference between two materials in contact can be visualized as the contact potential between them. For an MOS capacitor system, the work function difference between the metal and semiconductor (Φ_m–Φ_s) causes distortion in the band structure of the system as shown in Figure 3.3a. This is because when *three* materials are in contact, E_f is constant at equilibrium and E_0 is continuous; *holes* flow from *p*-type semiconductor to metal and *electrons* flow from metal to *p*-type semiconductor on contact until a potential is built up to counterbalance the difference in work function. However, the currents through SiO_2 are very small. Thus, there is a variation in electrostatic potential from one region to another, causing band

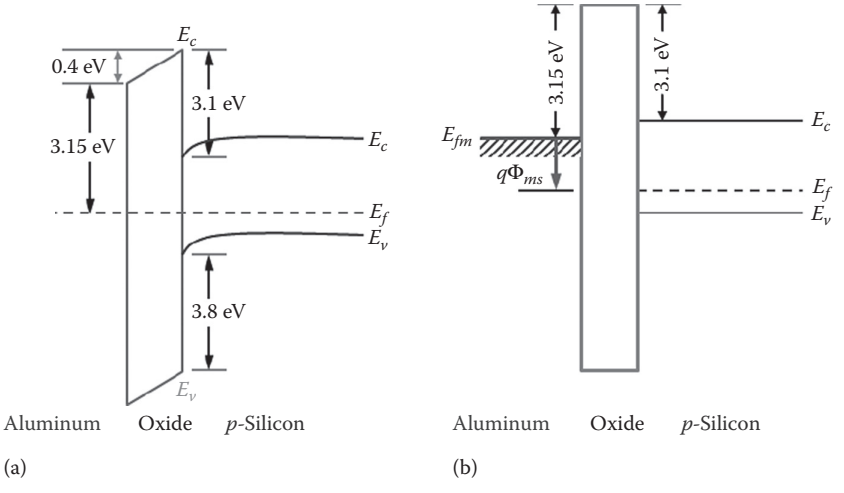

FIGURE 3.3

MOS capacitor system at applied gate voltage, $V_g = 0$, showing (a) band bending at the surface due to Φ_{ms} between aluminum metal and *p*-type semiconductor and (b) flat band condition for structure shown in (a); oxide is assumed to be free of any charges.

bending in the oxide and silicon. Since metal is an equipotential region, there is no band bending in metal.

For *p*-type silicon and aluminum metal MOS capacitor (Al-SiO_2-Si) system, $\Phi_m < \Phi_s$, therefore, energy bands bend downward in the oxide and silicon near the surface as shown in Figure 3.3a. And, there is an abrupt transition in E_c and E_v levels at the material interfaces. The metal and semiconductor work function difference (Φ_m–Φ_s) causes a potential drop in oxide and near the silicon surface due to band bending. A typical potential drop in oxide is about 0.4 V. This potential drop depends on the doping level in silicon and can be supported since no current flows through oxide. The values shown in Figure 3.3a for the band bending in the oxide and silicon are obtained by assuming that the oxide is an ideal insulator without any charges. We can compensate for this band bending by applying an external voltage $V_{fb} = (\Phi_m - \Phi_s)$, which caused the band bending in the first place. V_{fb} is referred to as the *flat band voltage* and the band structure for an MOS capacitor at flat band condition is shown in Figure 3.3b.

Thus, the condition for flat band voltage at the Si/SiO_2 interface is given by

$$V_{fb} = \Phi_m - \Phi_s \equiv \Phi_{ms} \tag{3.5}$$

where:

Φ_{ms} is the work function difference between the gate electrode and bulk silicon (in units of volts)

Then for an Al-SiO_2-*p*Si system,

$$q\Phi_{ms} = q\Phi_m - q\Phi_{sp} = q\Phi_m - \left(q\chi_s + \frac{E_g}{2} + q\phi_B\right) \tag{3.6}$$

Considering the values shown in Figure 3.2a–c, we get

$$\Phi_{ms} = -\left(0.51 + \phi_B\right) \quad \text{for } p\text{-type silicon} \tag{3.7}$$

Since $\phi_B \cong 0.29\,\text{V}$ for substrate concentration $N_b = 1 \times 10^{15}\ \text{cm}^{-3}$; therefore, Φ_{ms} is a negative number. Similarly, for an Al-SiO_2-*n*Si system,

$$q\Phi_{ms} = q\Phi_m - q\Phi_{sn} = q\Phi_m - \left(q\chi_s + \frac{E_g}{2} - q\phi_B\right) \tag{3.8}$$

$$\Phi_{ms} = -\left(0.51 - \phi_B\right) \quad \text{for } n\text{-type silicon} \tag{3.9}$$

Equation 3.9 shows that Φ_{ms} for MOS capacitors with an *n*-type silicon is also a negative number for $N_b < 1 \times 10^{18}\ \text{cm}^{-3}$. Since in advanced CMOS technologies, the channel is undoped or lightly doped, Φ_{ms} is always negative. This work function difference causes band bending when the materials are brought in contact.

For degenerately doped polysilicon gate electrode, the band structure for an MOS capacitor system is shown in Figure 3.4.

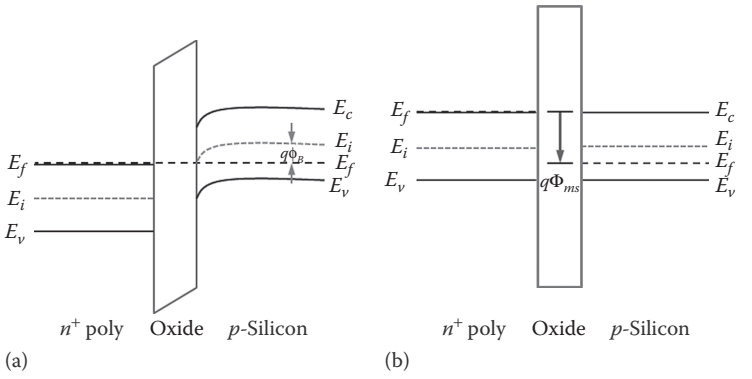

FIGURE 3.4
MOS capacitor system with degenerately doped n+ polysilicon gate electrode and p-type silicon (a) band bending at the surface due work function difference, Φ_{ms}, (b) flat band condition; oxide is assumed to be free of any charges.

Thus, with reference to Figure 3.4, Φ_{ms} for an n+ polysilicon gate on a p-type substrate MOS capacitor system is

$$q\Phi_{ms} = q\chi_s - \left(q\chi_s + \frac{E_g}{2} + q\phi_B\right) = -\left(0.56 + \phi_B\right), \quad \text{for } p\text{-type silicon} \tag{3.10}$$

Similarly, it can be shown that Φ_{ms} for p+ polysilicon gate and n-type substrate MOS capacitor system is

$$q\Phi_{ms} = \left(q\chi_s + E_g\right) - \left(q\chi_s + \frac{E_g}{2} - q\phi_B\right) = \left(0.56 + \phi_B\right), \quad \text{for } n\text{-type silicon} \tag{3.11}$$

Equation 3.10 shows that even for an n+ polysilicon gate with p-type silicon MOS capacitor system, Φ_{ms} is still negative. On the other hand, Equation 3.11 shows that for a p+ polysilicon gate with n-type substrate, Φ_{ms} is a positive quantity. The value of Φ_{ms} for polysilicon gate is found to be dependent on polysilicon doping concentration and grain structure [8,9].

3.2.2 Oxide Charges

During oxide growth process or subsequent IC fabrication processing steps, some impurities or defects are inadvertently incorporated into the oxide. As a result, the oxide is contaminated with various types of charges and traps. Typically, four different types of charge have been identified in thermally grown oxide on a silicon surface as shown in Figure 3.5 [10]. These charges are (1) interface-trapped charge Q_{it}, (2) fixed-oxide charge Q_f, (3) oxide-trapped charge Q_{ot}, and (4) mobile ionic charge Q_m. All of these charges are dependent on IC fabrication processing steps. The detailed description of the origin and techniques of measurements of different oxide charges are available in the literature [1,11]. In the following subsection, the basic properties of these charges are described.

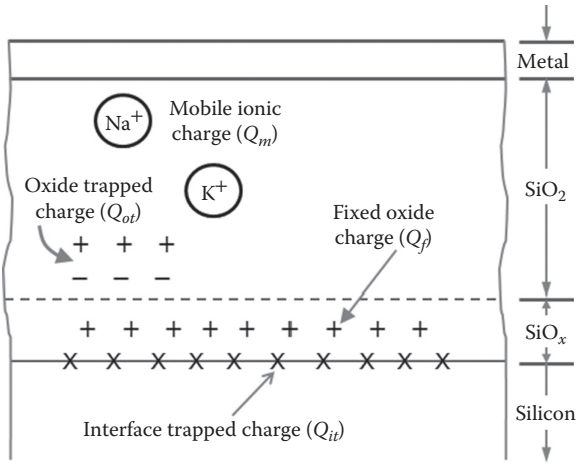

FIGURE 3.5
Types and location of the charges associated with thermally grown SiO_2 on silicon.

3.2.2.1 Interface-Trapped Charge

The interface-trapped charge density, Q_{it}, also referred to as the *surface states*, *fast states*, or *interface states*, exists at the Si/SiO_2 interface as shown in Figure 3.5. It is caused by defects at that interface which gives rise to charge *traps* or *electronic energy levels* with energy states (E_s) in the silicon bandgap that can capture or emit mobile carriers. These electronic states are due to lattice mismatch at the interface, dangling bonds, the adsorption of foreign impurity atoms at the silicon surface, and other defects caused by radiation or any bond-breaking process. Q_{it} is the most important type of charge because of its wide-ranging and degrading effect on device characteristics. Under the equilibrium condition, the occupancy of the interface states or traps depends on the position of the Fermi level.

Typically, the interface trap levels with density, D_{it} (traps cm^{-2} eV^{-1}), are distributed over energies within the silicon energy gap [1–3,5]. D_{it} varies significantly from process to process and is dependent on crystal orientation. In thermally grown SiO_2 on silicon, the most of the interface-trapped charge is neutralized by low temperature (≤500°C) hydrogen annealing. D_{it} correlates with the density of available bonds at the surface. Therefore, in <100> orientation with lower density of silicon atoms (available bonds) at the surface, D_{it} is about an order of magnitude lower than that in <111> oriented silicon with higher available bonds at the surface. The value of D_{it} at mid-gap for <100> oriented silicon in modern MOS VLSI (very-large-scale-integrated) process can be as low as 5×10^9 cm^{-2} eV^{-1}. *Higher values of* D_{it} *cause instabilities in the MOS transistor behavior.*

3.2.2.2 Fixed-Oxide Charge

The fixed charge density, Q_f, is the immobile charge always present and located within 1 nm transition layer of nonstoichiometric silicon oxide

(SiO_x) at the boundary between the silicon and SiO_x layer as shown in Figure 3.5. Generally, Q_f is positive and appears to arise from incomplete silicon-to-silicon bonds and depends on the oxidation ambient, temperature and annealing conditions, and silicon orientation. Since the density of atoms at the surface of a silicon crystal depends on the crystal orientation, Q_f is higher in <111> silicon than in <100> wafers. However, it is independent of the doping type and concentration in the silicon, oxide thickness, and oxidation time. Q_f can be minimized by annealing the oxide in an inert ambient, such as Argon at a temperature in excess of 900°C. A typical value of Q_f for a carefully treated Si/SiO_2 system is about 1×10^{10} cm^{-2} for the <100> surface. Because of the low values of Q_{it} and Q_f, the <100> orientation is preferred for silicon MOSFETs (metal-oxide-semiconductor field-effect transistors).

3.2.2.3 Oxide-Trapped Charge

The oxide-trapped charge density, Q_{ot}, is associated with defects in SiO_2. Q_{ot} is located in traps distributed throughout the oxide layer. The oxide traps are usually electrically neutral and are charged by introducing electrons and holes into the oxide through ionizing radiation such as implanted ions, X-rays, and electron beams. The magnitude of Q_{ot} depends on the amount of radiation dose and energy and the field across the oxide during irradiation. Like Q_{it}, these charges could be positive (trapped holes) or negative (trapped electrons). Q_{ot} resembles Q_f in that its magnitude is not a function of silicon surface potential and there is no capacitance associated with it.

3.2.2.4 Mobile Ionic Charge

The mobile ionic charge density, Q_m, is due to sodium (Na^+) or other alkali ions that get into the oxide during cleaning, processing, and handling of MOS devices. These ions move very slowly within the oxide; their transport depends strongly on the applied electric field (~1 MV cm^{-1}) and temperature (30°C–400°C). Positive voltages push the ions toward the Si/SiO_2 interface while the negative voltages draw them toward the gate. A current is observed in the external circuit during ion drift. The drift of ions changes the centroid of charge within the oxide layer, resulting *in a shift of the flat band voltage of MOS capacitor system and may cause an unexpected device failure*. Different approaches are used to reduce mobile ion contamination in gate oxide and mitigate the risk of mobile ionic induced device failure [1,5].

The earlier described oxide charges cause an additional band bending at the silicon surface of an MOS capacitor system and shift the value of V_{fb} caused by Φ_{ms} as described in the following section.

3.2.3 Flat Band Voltage

In order to determine the total shift in the flat band voltage (ΔV_{fb}) by various oxide charges, let us consider $\rho(x)$ as the charge density per unit volume within the oxide. Then from Gauss's law (Equation 2.61), we can show

$$\Delta V_{fb} = -\frac{1}{K_{ox}\varepsilon_0}\int_0^{T_{ox}} x\rho(x)dx = -\frac{1}{C_{ox}}\int_0^{T_{ox}} \frac{x}{T_{ox}}\rho(x)dx \tag{3.12}$$

where $\rho(x)$ includes the charge densities due to Q_{it}, Q_f, Q_{ot}, and Q_m. Q_f and Q_{it} are located at or near the Si/SiO_2 interface (i.e., $x = T_{ox}$) whereas Q_{ot} and Q_m are distributed throughout the oxide. Therefore, we only integrate Q_{ot} and Q_m that are distributed throughout the oxide to get

$$\Delta V_{fb} = -\frac{Q_{it}+Q_f}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{T_{ox}} \frac{x}{T_{ox}}\left[Q_{ot}(x)+Q_m(x)\right]dx \tag{3.13}$$

In compact modeling for circuit simulation, Equation 3.13 is expressed as

$$\Delta V_{fb} = -\frac{Q_o}{C_{ox}}(V) \tag{3.14}$$

where:

Q_o is the *equivalent interface charge* located at the Si/SiO_2 interface and causes the same effect as that of the actual charges of unknown distribution

Q_o is always positive for both *p*- and *n*-type substrates. ΔV_{fb} is the gate voltage that is needed to cause Q_o to be imaged in the gate electrode so that none is induced in the silicon. However, when gate "floats" or the gate electrode is absent, the oxide charges will seek all their image charges in the silicon.

In Figure 3.3a, we have shown the band bending of an MOS capacitor system due to work function difference between the metal and semiconductor. The corresponding flat band voltage is given by Equation 3.5. Now, the shift in work function due to band bending by oxide charges is given by Equations 3.13 and 3.14. Thus, combining Equations 3.5 and 3.14, the total V_{fb} due to Φ_{ms} and Q_o is given by

$$V_{fb} = \Phi_{ms} - \frac{Q_o}{C_{ox}} \tag{3.15}$$

Typically, Q_o/C_{ox} is much smaller than Φ_{ms} in Equation 3.15. Therefore, for an MOS capacitor with *p*-substrate and *n*+ polysilicon gate, V_{fb} is a negative number since Φ_{ms} is negative from Equation 3.10. On the other hand, for MOS capacitor with *n*-substrate and *p*+ polysilicon gate, V_{fb} is positive since Φ_{ms} is positive from Equation 3.11.

3.2.4 Effect of Band Bending on the Semiconductor Surface

Let us now consider an Al-SiO_2-Si MOS capacitor system on a *p*-type substrate to discuss the effect of band bending at the silicon surface on the surface behavior of MOS capacitors. We know that the concentration of holes in a *p*-type substrate is given by (Equation 2.63),

$$p = n_i \exp\left(\frac{E_i - E_f}{kT}\right) \tag{3.16}$$

The band structure of the system is shown in Figure 3.6. It is seen from Figure 3.6 that as the bands bend downward, the energy difference (E_i–E_f) gradually decreases as we approach the silicon surface at $x = 0$ from the bulk at ($x = \infty$). Then from Equation 3.16, the decrease in (E_i–E_f) results in a decrease in the hole concentration *p*. This implies that the holes are depleted at the surface, giving rise to a space charge region. On the other hand, if the bands bend upward, as in the case of an MOS capacitor system with ($\Phi_m > \Phi_s$), the value of (E_i–E_f) increases at the surface, resulting in an increase in the hole concentration (accumulation) at the surface. Thus, even without an applied external voltage to an MOS capacitor, the carrier concentration at the surface differs from that in the bulk due to Φ_{ms} and Q_o. This change in the concentration sets up an electric field at the surface and hence a voltage difference between the silicon surface and bulk. This voltage difference is referred to as the *surface potential* ϕ_s and represents the electrostatic potential at the surface measured from the bulk intrinsic level E_i. Thus, ϕ_s is the difference between $E_i(x = 0)$ at the surface and $E_i(x = \infty)$ at a point deep into the substrate. As shown in Figure 3.6, ϕ_s is a measure of the amount of total band bending at the silicon surface. And, at a depth *x* into the surface, the potential is given by $\phi(x)$.

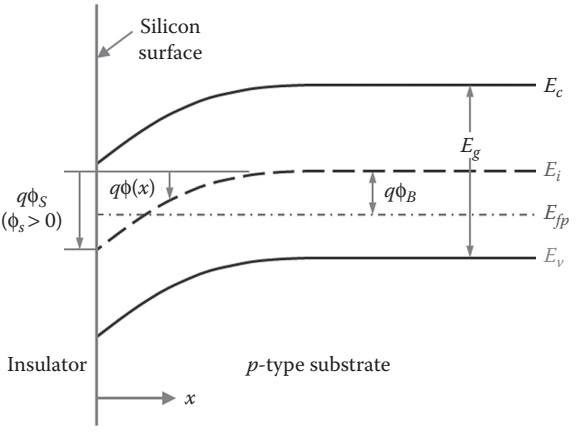

FIGURE 3.6
MOS capacitor system: Band bending showing the surface potential ϕ_s at the surface of a *p*-type silicon; here *x* is the distance from the insulator/substrate interface into the substrate with $x = 0$ at the surface.

The band bending described earlier can be compensated by applying an external gate voltage given by Equation 3.15. The condition to achieve the flat bands at the surface is called the *flat band condition* and the corresponding gate voltage required to achieve the flat band condition is called the *flat band voltage*, V_{fb}. Thus, V_{fb} *is the applied gate voltage to have zero surface potential with flat energy bands over the entire semiconductor surface*. The flat band condition is often used as a reference state along with V_{fb} as a reference voltage and, thus, can be considered as an important figure of merit for an MOS capacitor system.

3.3 MOS Capacitor under Applied Bias

In the previous section, we described the behavior of an MOS capacitor system without the application of any external bias. Now, let us discuss the behavior of the system under the applied gate bias V_g as shown in Figure 3.7. The applied V_g is shared between the voltage across the oxide V_{ox}, surface potential ϕ_s, and the work function Φ_{ms} between the metal and the semiconductor to achieve flat band condition. Thus,

$$\begin{aligned} V_g &= V_{ox} + \phi_s + \Phi_{ms} \\ &= V_{ox} + \phi_s + V_{fb} \end{aligned} \tag{3.17}$$

With reference to charges, an MOS capacitor consists of three different charges under the applied V_g such as: (1) gate charge Q_g due to the applied V_g to the gate, (2) effective interface charge Q_o at the Si/SiO_2 interface for

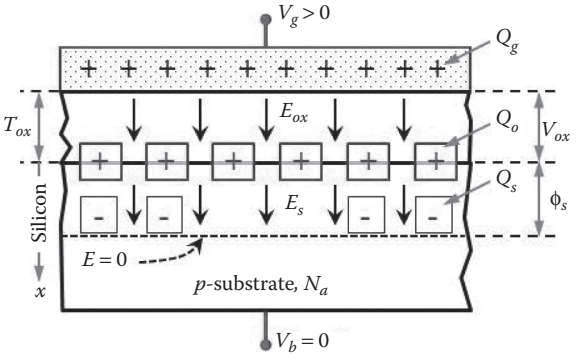

FIGURE 3.7
An MOS capacitor system under the applied gate bias V_g showing various charges, electric fields, and potentials. E_{ox} is the electric field in oxide; E_s is the electric field in substrate.

nonideal insulator as discussed in Section 3.2.2, and (3) the induced charge Q_s in the silicon underneath the gate oxide. Then from the charge neutrality condition we get

$$Q_g + Q_o + Q_s = 0 \tag{3.18}$$

If the applied voltage V_g is positive, then the electric field E_s is directed into the silicon surface at the interface and will induce a charge Q_s in the silicon. The density of the induced charge Q_s per unit area can be calculated by applying Gauss's law at the Si/SiO_2 interface. Thus, Q_s per unit area is given by

$$Q_s = -\varepsilon_0 K_{si} E_s \tag{3.19}$$

where:
K_{si} is the permittivity of silicon
ε_0 is the permittivity of vacuum

Similarly, applying Gauss's law at the metal-oxide interface gives

$$Q_g = \varepsilon_0 K_{ox} E_{ox} \equiv V_{ox} C_{ox} \tag{3.20}$$

where:
$E_{ox} = V_{ox}/T_{ox}$ is the electric field in the oxide

The field E_{ox} and E_s are related by Equation 3.18. For an ideal oxide, $Q_o = 0$, and we have from Equation 3.18, $Q_g = -Q_s$; then from Equations 3.19 and 3.20, we get

$$\varepsilon_0 K_{si} E_s = \varepsilon_0 K_{ox} E_{ox}$$

or

$$E_s = \frac{K_{ox} E_{ox}}{K_{si}} \tag{3.21}$$

Now, substituting for E_s from Equation 3.21 in Equation 3.19 we get

$$Q_s = -\varepsilon_0 K_{si}\left(\frac{K_{ox} E_{ox}}{K_{si}}\right) = -\varepsilon_0 K_{ox} E_{ox} = -V_{ox} C_{ox}$$

$$\therefore V_{ox} = -\frac{Q_s}{C_{ox}} \tag{3.22}$$

Now, substituting for V_{ox} from Equation 3.22 in Equation 3.17, we get

$$V_g = V_{fb} + \phi_s - \frac{Q_s}{C_{ox}} \tag{3.23}$$

Equation 3.23 relates the applied bias V_g and the surface potential ϕ_s. At the flat band condition, $\phi_s = 0$ and $Q_s = 0$; therefore, from Equation 3.23, $V_g = V_{fb}$. Within the range $0 > V_g > 0$, different surface conditions result in an MOS capacitor system as discussed in Sections 3.3.1 through 3.3.3.

3.3.1 Accumulation

To continue our discussion on Al/SiO_2/*p*-silicon MOS capacitor system, let us apply a negative gate voltage V_g with body grounded such that $V_g < V_{fb}$. The negative voltage at the gate creates an upward electric field E_{ox} from the substrate to metal as shown in Figure 3.8. Since the applied negative voltage depresses the electrostatic potential of the metal relative to the substrate, electron energies are raised in the metal relative to the substrate. As a result, the Fermi level E_{fm} for the metal moves up above its equilibrium position by qV_g. Since Φ_m and Φ_s do not change with V_g, moving E_{fm} up in energy relative to E_f causes the oxide conduction band to bend upward, consistent with the direction of the field E_{ox} causing gradient in the energy bands [2,12].

With reference to charge, the negative voltage at the gate results in a negative charge ($Q_g < 0$) on the gate. This in turn induces an equal amount of positive charge Q_s at the silicon surface. This amount of positive charge in the *p*-type silicon means excess hole concentration is created at the surface as shown in Figure 3.8. These holes are accumulated at the surface and known as the *accumulation* charges. We know from Equation 3.16 that, as the hole concentration increases at the surface, $(E_i – E_f)$ increases, resulting in the bands bending upward as shown in Figure 3.9. Thus, in accumulation for *p*-type silicon we have

$$\text{Accumulation} \begin{cases} V_g < V_{fb} \\ \phi_s < 0 \\ Q_s > 0 \end{cases} \tag{3.24}$$

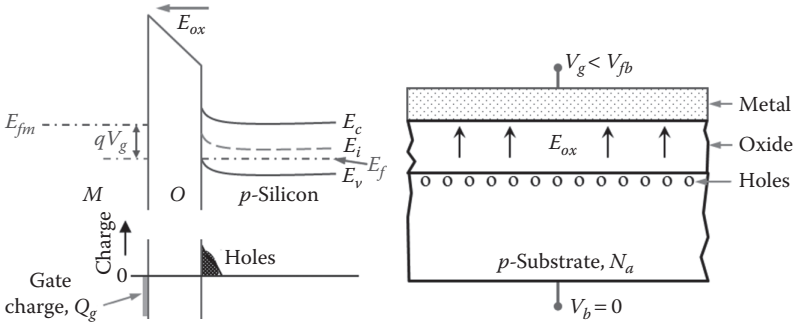

FIGURE 3.8
Effect of applied voltage, $V_g < V_{fb}$ on a *p*-type MOS capacitor system: the applied negative bias $V_g < V_{fb}$ causes hole accumulation at the silicon surface.

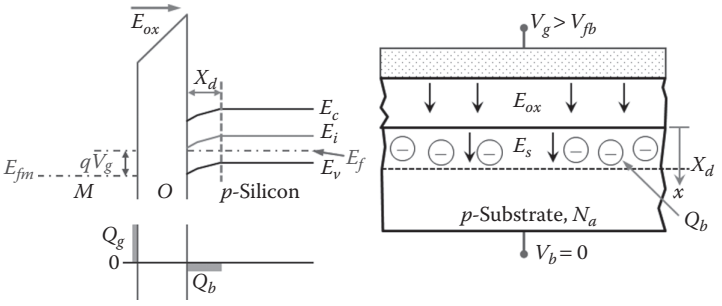

FIGURE 3.9
Effect of applied voltage, $V_g > V_{fb}$ on a *p*-type MOS capacitor system: the applied positive bias $V_{go} = (V_g - V_{fb})$ depletes the holes from the silicon surface. Q_b is the depletion or bulk charge; Q_g is the gate charge; X_d is the depletion region width.

This bias condition (Equation 3.24) is useful in the characterization of MOS capacitor system.

3.3.2 Depletion

Now, let us apply a positive gate voltage $V_g > V_{fb}$ with body grounded. This positive V_g will create a downward electric field E_{ox} from the gate into the substrate as shown in Figure 3.9. A positive gate voltage raises the potential of the gate, lowering the Fermi level E_{fm} by qV_g. Moving E_{fm} down in energy relative to E_f causes band bending downward in the oxide conduction band in accordance to the direction of E_{ox}.

Again, with reference to charge, a positive voltage at the gate deposits positive charge ($Q_g > 0$) on it. Due to $V_g > 0$, the holes are repulsed away from the silicon surface, leaving behind negatively charged acceptor ions. Thus, a positive charge on the gate induces a negative charge Q_s at the surface due to the depletion of holes creating a depletion region of width X_d. This is known as the *depletion* condition. Since the hole concentration decreases at the surface, then from Equation 3.16, $(E_i - E_f)$ must decrease. As a result, E_i slowly approaches to E_f thereby bending the bands downward near the surface as shown in Figure 3.9. Thus, the depletion condition is given by

$$\text{Depletion} \begin{cases} V_g > V_{fb} \\ \phi_s > 0 \\ Q_s < 0 \end{cases} \tag{3.25}$$

3.3.3 Inversion

If we further increase the positive gate voltage, the downward band bending will further increase. At a sufficiently large $V_g >> V_{fb}$, the band bending may pull down the mid-gap energy level E_i below the constant E_f at the silicon

surface, that is, $E_f > E_i$. At this condition, the surface behaves like an *n*-type material with an electron concentration given by (Equation 2.62)

$$n = n_i \exp\left(\frac{E_f - E_i}{kT}\right) \tag{3.26}$$

Thus, the *n*-surface is formed by inversion of the *p*-type substrate due to the applied gate voltage. This is known as the *inversion* condition as shown in Figure 3.10. In inversion, the total charge, Q_s, in the semiconductor consists of depletion charge, Q_b, and the inversion charge, Q_i. The inversion condition for MOS capacitor with *p*-type substrate is defined by

$$\text{Inversion} \quad \begin{cases} V_g >> V_{fb} \\ \phi_s > 0 \\ Q_s < 0 \end{cases} \tag{3.27}$$

Under the applied $V_g >> V_{fb}$, the *p*-type surface is inverted as soon as E_i is pulled below E_f. However, for small $(E_f - E_i)$, the electron concentration remains very small and the inversion is *weak*. This is referred to as the *weak inversion regime*. If we increase V_g such that $(E_f - E_i)$ at the surface equals $(E_i - E_f)$ at the *p*-type bulk, the concentration of electrons at the surface will be equal to that of holes in the bulk. This is called the *strong inversion* regime. On further increase of V_g, the electron concentration will exceed the concentration of the holes in the inversion region. Under the inversion condition, the depth of the inversion region (X_{inv}) into the substrate can be defined at $E_f = E_i$ and is about 3 nm [2].

Now, let us discuss how the inversion layer is formed in the substrate. At the onset of inversion, the minority carrier electrons in the *p*-type substrate of

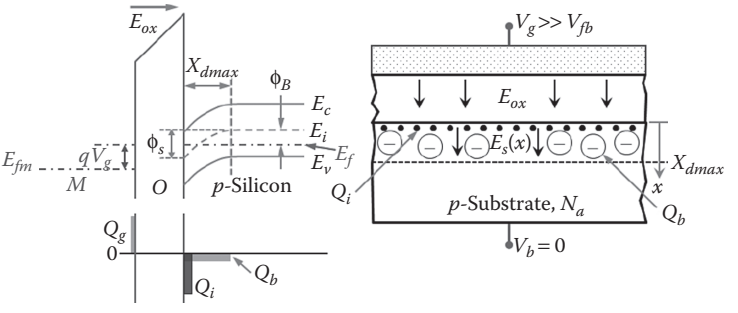

FIGURE 3.10
Effect of an applied voltage, $V_g >> V_{fb}$ on a *p*-type MOS capacitor system: a large positive bias $V_g >> V_{fb}$ causes inversion of the *p*-type surface forming an *n*-type layer. The gate charge is compensated by the depletion charge Q_b and the inversion charge Q_i in the semiconductor. Q_b is the depletion or bulk charge; Q_g is the gate charge; Q_i is the inversion charge; X_{dmax} is the maximum depletion width.

an MOS capacitor system originate from thermally generated electron–hole pairs within the depletion region. The rate of thermal generation depends upon the minority carrier lifetime, which is of the order of microseconds. It is found that the time required to form an inversion layer at the surface is about 0.2 sec [3]. Thus, the *formation of the inversion layer is a relatively slow process compared to the time required for the holes (majority carriers) to flow from or to the silicon surface*, which is of the order of picoseconds. Once the inversion layer is formed, it shields the underneath depletion layer, thus limiting the maximum width, X_{dmax}, of the depletion layer.

So far, we have presented a qualitative overview of the basic operation of an MOS capacitor system. In the following section, we will develop MOS capacitor theory that can be extended to develop the operational theory of MOSFET devices in Chapters 4, 5, and 9.

3.4 MOS Capacitor Theory

Now, let us derive the relation between the surface potential (ϕ_s), electric field (E_s), and charge (Q_s) by solving Poisson's equation for potential (ϕ) near the surface region of the silicon substrate of an MOS capacitor system. The Poisson's equation (Equation 2.58) is given by

$$\frac{d^2\phi}{dx^2} = -\frac{1}{K_{si}\varepsilon_0}\rho(x) \tag{3.28}$$

where:

$\rho(x)$ is the charge density at any point x along the depth of the substrate and is given by

$$\rho(x) = q\left[p(x) - n(x) + N_d^+(x) - N_a^-(x)\right] \tag{3.29}$$

where:

$p(x)$ is the hole concentration
$n(x)$ is the electron concentration
$N_d^+(x)$ is the ionized donor concentration in the semiconductor substrate
$N_a^-(x)$ is the ionized acceptor concentration in the semiconductor substrate

Thus, combining Equations 3.28 and 3.29 we get

$$\frac{d^2\phi}{dx^2} = -\frac{q}{K_{si}\varepsilon_0}\left[p(x) - n(x) + N_d^+(x) - N_a^-(x)\right] \tag{3.30}$$

Before solving Equation 3.30 for $\phi(x)$ at any point x of the surface, let us review the relevant semiconductor equations in the following subsection.

3.4.1 Formulation of Poisson's Equation in Terms of Band-Bending Potential

In order to solve Poisson's Equation 3.30 for $\phi(x)$ at any point x near the surface of an MOS capacitor system, we express carrier density $\rho(x)$ in terms of potentials ϕ_i, ϕ_f, and $\phi(x)$. In an n-type semiconductor with doping concentration, N_d, the majority carrier *electron* concentration n is given by (Equations 2.62 and 2.64)

$$n \cong \begin{cases} n_i \exp\left(\dfrac{E_f - E_i}{kT}\right) = n_i \exp\left[\dfrac{q\left(\phi_i - \phi_f\right)}{kT}\right] \\ N_d^+ \end{cases} \tag{3.31}$$

In Equation 3.31, $\phi_f = -E_f / q$ is the Fermi potential and $\phi_i = -E_i / q$ is the intrinsic potential; then the minority carrier concentration p_n in an n-type semiconductor is given by (Equation 2.66)

$$p_n \cong \frac{n_i^2}{N_d^+} \tag{3.32}$$

Similarly, the majority carrier concentration in a p-type semiconductor with doping concentration N_a is given by (Equations 2.63 and 2.65)

$$p \cong \begin{cases} n_i \exp\left(\dfrac{E_i - E_f}{kT}\right) = n_i \exp\left[\dfrac{q(\phi_f - \phi_i)}{kT}\right] \\ N_a^- \end{cases} \tag{3.33}$$

And, the minority carrier concentration n_p in a p-type semiconductor is given by (Equation 2.67)

$$n_p \cong \frac{n_i^2}{N_a^-} \tag{3.34}$$

In order to develop a generalized expression for both n-type and p-type substrates, we define, N_b as the substrate concentration. Then from Equations 3.31 and 3.33, we can show that the bulk (Fermi) potential is

$$\phi_B = \left|\phi_f - \phi_i\right| = v_{kT} \ln\left(\frac{N_b}{n_i}\right) \tag{3.35}$$

In Equation 3.35, N_b represents the donor-type doping concentration for an n-type substrate and acceptor-type doping concentration for a p-type substrate; v_{kT} is the thermal voltage.

Now, in order to express $\rho(x)$ in terms of band bending $\phi(x)$ at any point x near the surface of a semiconductor, we consider the band structure of an Al/SiO_2/p-silicon MOS capacitor system as shown in Figure 3.11.

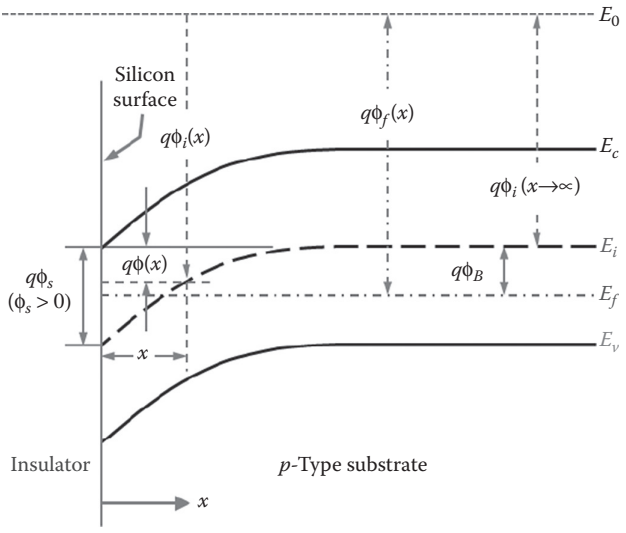

FIGURE 3.11
Equilibrium band structure of a *p*-type MOS capacitor system showing band bending in the substrate; here, $x = 0$ at the Si/SiO_2 interface and increases with the depth into the substrate; ϕ_s is the surface potential representing the total band bending at the surface.

From Figure 3.11, the amount of band bending at any point x near the silicon surface with reference to E_0 is given by

$$\phi(x) = \phi_i(x) - \phi_i(x \to \infty) \tag{3.36}$$

where $\phi(x = 0) = \phi_s$ = surface potential; $\phi_i(x \to \infty) = \phi_i$ is the intrinsic potential. Also, from Figure 3.11, the bulk-potential $\phi_B = (\phi_f - \phi_i)$. It is seen from Figure 3.11 that $\phi_i(x) > \phi_i$ when bands bend downward at the interface, resulting in $\phi(x) > 0$. Thus, it is clear that $\phi(x) > 0$ when bands bend downward in the *depletion* and *inversion* conditions and $\phi(x) < 0$ when bands bend upward in the *accumulation* condition.

Now, let us express $p(x)$, $n(x)$, $N_d^+(x)$, and $N_a^-(x)$ in Poisson's Equation 3.30 in terms of potential $\phi(x)$ and solve for ϕ_s and E_s at the surface of the MOS system. For a *p*-type silicon substrate, we can express the majority carrier concentration given in Equation 3.33 at any point x by substituting for $\phi_i(x)$ from Equation 3.36 so that

$$p(x) = n_i \exp\left\{\frac{\left[\phi_f - \phi_i(x)\right]}{v_{kT}}\right\} = n_i \exp\left\{\frac{\phi_f - \left[\phi_i(x \to \infty) + \phi(x)\right]}{v_{kT}}\right\} \tag{3.37}$$

Since $\left[\phi_f - \phi_i(x \to \infty)\right] = \left(\phi_f - \phi_i\right) = \phi_B$; then we can express (3.37) as

$$p(x) = n_i \exp\left[\frac{\left(\phi_f - \phi_i\right) - \phi(x)}{v_{kT}}\right] = n_i \exp\left(\frac{\phi_f - \phi_i}{v_{kT}}\right)\exp\left(-\frac{\phi(x)}{v_{kT}}\right) \tag{3.38}$$

Now, using Equation 3.33 in Equation 3.38, we get for the majority carrier concentration at any point x in a p-type substrate from

$$p(x) = N_a \exp\left(-\frac{\phi(x)}{v_{kT}}\right) \tag{3.39}$$

Then from Equation 3.34, the minority carrier electron concentration at any point x near the surface of a p-type substrate is given by

$$n(x) \cong \frac{n_i^2}{p(x)} = \frac{n_i^2}{N_a} \exp\left(\frac{\phi(x)}{v_{kT}}\right) \tag{3.40}$$

Again, from Equations 3.34 and 3.35, we can show that for a p-type substrate

$$\frac{n_i^2}{N_a} = \begin{cases} n_i \exp\left(-\dfrac{\phi_B}{v_{kT}}\right) \\ N_a \exp\left(-\dfrac{2\phi_B}{v_{kT}}\right) \end{cases} \tag{3.41}$$

Then the minority carrier concentration given by Equation 3.40 can also be written as

$$n(x) = \begin{cases} n_i \exp\left[\dfrac{\phi(x) - \phi_B}{v_{kT}}\right] \\ N_a \exp\left[\dfrac{\phi(x) - 2\phi_B}{v_{kT}}\right] \end{cases} \tag{3.42}$$

Substituting the expressions for $p(x)$ and $n(x)$ from Equations 3.39 and 3.40, respectively, in Equation 3.29 we get

$$\rho(x) = q\left\{N_a e^{-\left[\phi(x)/v_{kT}\right]} - \frac{n_i^2}{N_a} e^{\phi(x)/v_{kT}} + N_d^+(x) - N_a^-(x)\right\} \tag{3.43}$$

Again, assuming complete ionization of acceptor atoms, for a p-type substrate we get from Equations 3.34 and 3.35, $p \cong N_a^- \equiv N_a$ and $n \cong N_d^+ = n_i^2/N_a$. Therefore, for a uniformly doped p- substrate, we can write

$$N_d^+(x) - N_a^-(x) = \frac{n_i^2}{N_a} - N_a \tag{3.44}$$

Then combining Equations 3.43 and 3.44, the charge density in the substrate (assuming complete ionization of dopant atoms in silicon) is given by

$$\rho(x) = q\left[N_a\left(e^{-\left[\phi(x)/v_{kT}\right]} - 1\right) - \frac{n_i^2}{N_a}\left(e^{\left[\phi(x)/v_{kT}\right]} - 1\right)\right] \tag{3.45}$$

It is to be noted that the first term in Equation 3.45 represents the charge density in the *p*-type substrate due to the majority carrier concentration and the second term represents the charge density due to minority carrier concentration. Now, substituting Equation 3.45 in Equation 3.30, we get Poisson's equation in terms of band-bending potential $\phi(x)$ at a depth x near the surface of a *p*-type substrate as

$$\frac{d^2\phi(x)}{dx^2} = -\frac{q}{\varepsilon_0 K_{si}}\left[N_a\left(e^{-\left[\phi(x)/v_{kT}\right]}-1\right)-\frac{n_i^2}{N_a}\left(e^{\left[\phi(x)/v_{kT}\right]}-1\right)\right] \tag{3.46}$$

We will solve Equation 3.46 for $\phi(x)$ to obtain MOS capacitor behavior under different operating conditions. Again, we notice from Equation 3.46 that the first term inside the square bracket is due to the majority carrier charge density whereas the second term is due to minority carriers in a *p*-type semiconductor substrate.

3.4.2 Electrostatic Potentials and Charge Distribution

In order to solve Equation 3.46 for potential distribution in silicon, we use the mathematical identity

$$\frac{d}{dx}\left(\frac{d\phi}{dx}\right)^2 = 2\frac{d\phi}{dx}\frac{d^2\phi}{dx^2} \tag{3.47}$$

Then multiplying both sides of Equation 3.46 by $2\left[d\phi(x)/dx\right]$, we get

$$2\frac{d\phi(x)}{dx}\frac{d^2\phi(x)}{dx^2} = -\frac{2q}{\varepsilon_0 K_{si}}\left[N_a\left(e^{-\left[\phi(x)/v_{kT}\right]}-1\right)-\frac{n_i^2}{N_a}\left(e^{\left[\phi(x)/v_{kT}\right]}-1\right)\right]\frac{d\phi(x)}{dx} \tag{3.48}$$

Now, using Equation 3.47 in the left-hand side of Equation 3.48, we can show that

$$\frac{d}{dx}\left(\frac{d\phi(x)}{dx}\right)^2 = -\frac{2q}{\varepsilon_0 K_{si}}\left[N_a\left(e^{-\left[\phi(x)/v_{kT}\right]}-1\right)-\frac{n_i^2}{N_a}\left(e^{\left[\phi(x)/v_{kT}\right]}-1\right)\right]\frac{d\phi(x)}{dx} \tag{3.49}$$

We integrate Equation 3.49 from the bulk $\left(\phi(x)=0, d\phi(x)/dx=0\right)$ toward the surface at any point x $\left(\phi(x), d\phi(x)/dx\right)$ near the surface shown in Figure 3.11 so that

$$\int_0^{d\phi(x)/dx} d\left(\frac{d\phi(x)}{dx}\right)^2 = -\frac{2q}{\varepsilon_0 K_{si}}\int_0^{\phi(x)}\left[N_a\left(e^{-\left[\phi(x)/v_{kT}\right]}-1\right)-\frac{n_i^2}{N_a}\left(e^{\left[\phi(x)/v_{kT}\right]}-1\right)\right]d\phi(x) \tag{3.50}$$

We know that the electric field at any point x near the silicon surface is given by $E(x) = -\left[d\phi(x)/dx\right]$; therefore, after integration and simplification of Equation 3.50, we can show

$$\left(\frac{d\phi(x)}{dx}\right)^2 = \frac{2qN_a v_{kT}}{\varepsilon_0 K_{si}}\left[\left(e^{-\left[\phi(x)/v_{kT}\right]} + \frac{\phi(x)}{v_{kT}} - 1\right) + \frac{n_i^2}{N_a^2}\left(e^{\left[\phi(x)/v_{kT}\right]} - \frac{\phi(x)}{v_{kT}} - 1\right)\right] \tag{3.51}$$

$$= E_s^2(x)$$

In silicon substrate at the Si/SiO_2 interface, $x = 0$, $\phi(x) = \phi_s$, and $E(x) = E_s$; then from Gauss's law, the total charge per unit area induced in silicon (equal and opposite to the charge on the metal gate) is given by $Q_s = -\varepsilon_0 K_{si} E_s$. Then from Equation 3.51, we can show that the charge per unit area at the surface of the substrate is given by

$$Q_s = \pm\sqrt{2qK_{si}\varepsilon_0 N_a v_{kT}}\left[\left(e^{-(\phi_s/v_{kT})} + \frac{\phi_s}{v_{kT}} - 1\right) + \frac{n_i^2}{N_a^2}\left(e^{(\phi_s/v_{kT})} - \frac{\phi_s}{v_{kT}} - 1\right)\right]^{1/2} \tag{3.52}$$

The expression (Equation 3.52) is valid for all regions of MOS capacitor operations: accumulation, depletion, and inversion. The positive sign indicates the induced charge is positive for accumulation and negative sign represents that for depletion and inversion in a *p*-type substrate. Equation 3.52 can also be expressed as

$$Q_s = \pm\frac{\sqrt{2}v_{kT}K_{si}\varepsilon_0}{L_d}\left[\left(e^{-(\phi_s/v_{kT})} + \frac{\phi_s}{v_{kT}} - 1\right) + \frac{n_{po}}{p_{po}}\left(e^{(\phi_s/v_{kT})} - \frac{\phi_s}{v_{kT}} - 1\right)\right]^{1/2} \tag{3.53}$$

where n_i^2/N_a^2 is expressed in terms of the equilibrium majority and minority carrier concentrations p_{po} and n_{po} in a *p*-type substrate, respectively, such that $n_i^2/N_a^2 = \left(n_i^2/N_a\right).\left(1/N_a\right) = n_{po}/p_{po}$ and is related to ϕ_B by Equation 3.41, whereas L_d is the Debye length defined by

$$L_d = \sqrt{\frac{\varepsilon_0 K_{si} kT}{q^2 N_a}} \tag{3.54}$$

Again, in Equations 3.52 and 3.53, the first term within parenthesis is the majority carrier charge in *p*-type substrate whereas the second term is due to the minority carrier electrons.

The variation of the induced charge Q_s as a function of ϕ_s using Equation 3.52 for *p*-type substrate is illustrated in Figure 3.12, which clearly shows all three regimes of MOS capacitor operation.

From Figure 3.12, the different regimes of MOS capacitor operation are easily identified. Let us use Equation 3.52 to analyze different regions of MOS capacitor operation.

1. When $\phi_s < 0$, the MOS structure is in the accumulation mode and the inversion carrier term is negligible. Then the dominant term in Equation 3.52 is $\exp\left(-\phi_s / v_{kT}\right)$. Thus, Q_s varies with ϕ_s as

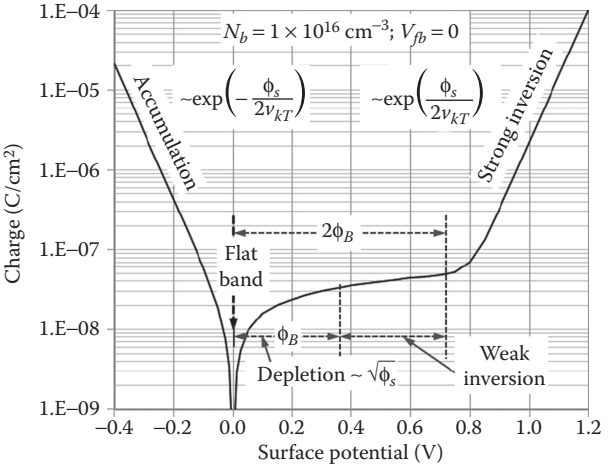

FIGURE 3.12
Variation of the induced charge density Q_s in a *p*-type silicon as a function of surface potential ϕ_s in all regimes of MOS capacitor operation; plot is obtained by Equation 3.52 using $N_a = 1 \times 10^{16}$ cm^{-3}, and $V_{fb} = 0$.

$$Q_s \approx \exp\left(-\frac{\phi_s}{2v_{kT}}\right) \quad \text{(accumulation)} \tag{3.55}$$

2. When $\phi_s > 0$ such that $0 < \phi_s < 2\phi_B$, the MOS capacitor structure is in the depletion and weak inversion regime. In this case, the term that dominates in Equation 3.52 is $\sqrt{\phi_s}$ and therefore Q_s varies with ϕ_s as

$$Q_s \approx \sqrt{\phi_s} \quad \text{(depletion and weak inversion)} \tag{3.56}$$

3. When $\phi_s > 2\phi_B$, the MOS capacitor structure is in the strong inversion regime, and to a first approximation, the majority carrier term in Equation 3.52 can be neglected. Then Q_s varies with ϕ_s as

$$Q_s \approx \exp\left(\frac{\phi_s}{2v_{kT}}\right) \quad \text{(strong inversion)} \tag{3.57}$$

The accumulation, depletion, and inversion conditions described by Equations 3.55, 3.56, and 3.57, respectively, are for *p*-type substrates. For *n*-type substrates, these conditions will be reversed.

3.4.2.1 MOS Capacitor at Depletion: Depletion Approximation

In the depletion region, $0 < \phi_s < 2\phi_B$ and the induced charge Q_s within the space charge region near the surface of the substrate is obtained by solving Poisson's equation. This induced charge in the depletion region is the depletion or *bulk charge* denoted by Q_b. For the simplicity of calculation, we use

depletion approximation; that is, we assume that the depletion region is free of minority carriers. Therefore, neglecting minority carrier term and recognizing $\phi(x) > 0$, we can approximate Equation 3.51 in the depletion region as

$$\frac{d\phi}{dx} \cong -\sqrt{\frac{2qN_a\phi}{K_{si}\varepsilon_0}} \tag{3.58}$$

or

$$\frac{1}{\sqrt{\phi}}\frac{d\phi}{dx} = -\sqrt{\frac{2qN_a}{K_{si}\varepsilon_0}} \tag{3.59}$$

We integrate Equation 3.59 from the surface ($x = 0$, $\phi(x) = \phi_s$) to a point (x, $\phi(x)$) in the depletion region of the substrate so that

$$\int_{\phi_s}^{\phi(x)} \frac{d\phi}{\sqrt{\phi}} = -\int_0^x \sqrt{\frac{2qN_a}{K_{si}\varepsilon_0}}\,dx \tag{3.60}$$

Integrating Equation 3.60 and after simplification, we can show

$$\phi(x) = \phi_s\left(1 - \sqrt{\frac{qN_a}{2K_{si}\varepsilon_0\phi_s}}x\right)^2 \tag{3.61}$$

If we define

$$X_d = \sqrt{\frac{2K_{si}\varepsilon_0\phi_s}{qN_a}} \tag{3.62}$$

Then we can express Equation 3.61 as

$$\phi(x) = \phi_s\left(1 - \frac{x}{X_d}\right)^2 \tag{3.63}$$

Equation 3.63 is parabolic with the vertex at $\phi(x) = 0$, $x = X_d$. Thus, X_d is the distance to which band bending extends and is the width of the depletion region as shown in Figure 3.13. Then using Equation 3.62 for X_d, the depletion layer (bulk) charge density is given by

$$Q_b = -qN_aX_d = -\sqrt{2qK_{si}\varepsilon_0N_a\phi_s} \tag{3.64}$$

Equation 3.64 also easily follows from Equation 3.52, using depletion approximation. In an MOS capacitor system, the onset of strong inversion is defined by

$$\phi_s = 2\phi_B = 2v_{kT}\ln\left(\frac{N_a}{n_i}\right) \tag{3.65}$$

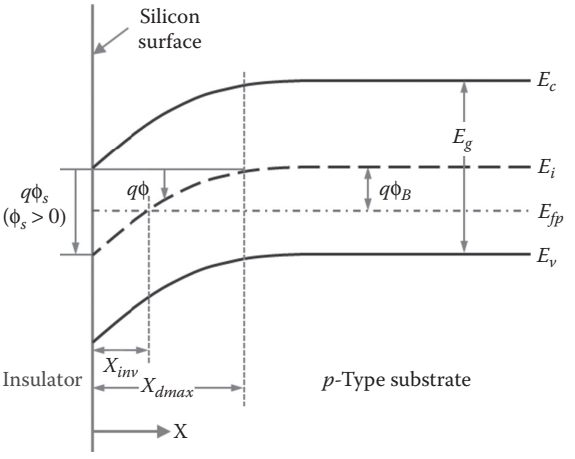

FIGURE 3.13
Variation of band-bending potential $\phi(x)$ along the depth of a p-type substrate showing the maximum width, X_{dmax}, of the depletion region at strong inversion and the width of the inversion layer, X_{inv}.

where ϕ_B is given by Equation 3.35. At strong inversion, X_d reaches a maximum, X_{dmax}, when $\phi_s = 2\phi_B$. This is because at strong inversion, the inversion layer shields the depletion charge so that the surface below can no longer respond to the applied V_g. Therefore, from Equations 3.62 and 3.65, the maximum width of the depletion layer is given by

$$X_{dmax} = \sqrt{\frac{4K_{si}\varepsilon_0 v_{kT}}{qN_a}\ln\left(\frac{N_a}{n_i}\right)} \tag{3.66}$$

3.4.2.2 MOS Capacitor at Inversion

In Section 3.3.3 we discussed that a sufficiently high gate voltage can cause enough band bending to pull the mid-gap energy E_i below the constant Fermi level E_f, that is, $E_i > E_f$. Under this condition, the surface of the p-type semiconductor is inverted and behaves like an n-type material with an electron concentration, n, given by Equation 3.42. In the inversion region $\phi_B < \phi_s < 2\phi_B$, the inversion layer charge Q_i can be calculated by considering the electron concentration (second term) from the general solution of Poisson's equation in Equation 3.52. In Equation 3.52, we observe that for $\phi_s > 0$, $\exp(-\phi_s/v_{kT})$ is negligibly small, the term "–1" is negligibly small since $\exp(\phi_s/v_{kT}) >> -1$ in strong inversion, and the term $(-\phi_s/v_{kT})$ is negligibly small in weak inversion. Therefore, from Equation 3.52, the induced charge in the semiconductor under the inversion condition is given by

$$Q_s \cong -\sqrt{2qK_{si}\varepsilon_0 N_a v_{kT}}\left[\frac{\phi_s}{v_{kT}} + \frac{n_i^2}{N_a^2}e^{(\phi_s/v_{kT})}\right]^{1/2} \tag{3.67}$$

Using the relation $n_i^2 / N_a^2 = \exp\left(-2\phi_B / v_{kT}\right)$ from Equation 3.41 in Equation 3.67, we get for the total induced charge density in the semiconductor as

$$Q_s = -\sqrt{2qK_{si}\varepsilon_0 N_a v_{kT}}\left[\frac{\phi_s}{v_{kT}} + e^{(\phi_s - 2\phi_B)/v_{kT}}\right]^{1/2} \tag{3.68}$$

Note that the induced charge represented by Equation 3.68 is the sum of the inversion charge Q_i and the depletion charge Q_b, that is,

$$Q_s = Q_i + Q_b \tag{3.69}$$

Using the expressions for $Q_b = -\sqrt{2qK_{si}\varepsilon_0 N_a \phi_s}$ from Equation 3.64 and Q_s from Equation 3.68 in Equation 3.69, we get the inversion charge per unit area as

$$Q_i = -\sqrt{2qK_{si}\varepsilon_0 N_a}\left[\left(\phi_s + v_{kT}e^{(\phi_s - 2\phi_B)/v_{kT}}\right)^{1/2} - \sqrt{\phi_s}\right] \tag{3.70}$$

Equation 3.70 shows the relation between the inversion charge density Q_i and surface potential ϕ_s for an MOS capacitor system. Figure 3.14 shows the dependence of Q_i, Q_b, and Q_s on ϕ_s. It is observed from Figure 3.14 that Q_b does not vary significantly. On the other hand, Q_i and Q_s clearly show two distinct regions of operation depending on the value of ϕ_s. These regions become more apparent on $\log(Q_i)$ versus ϕ_s plot as shown in Figure 3.15. These regions are (1) weak inversion for lower values of ϕ_s and (2) strong inversion at higher values of ϕ_s. Classically, the condition separating the

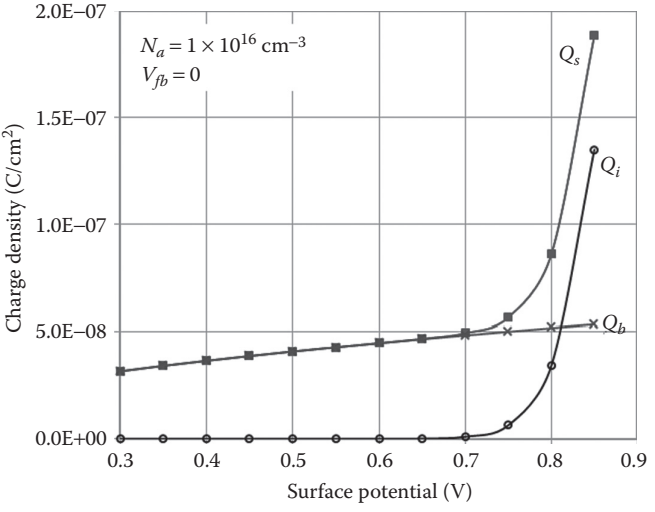

FIGURE 3.14
Variation of Q_b, Q_s, and Q_i as a function of ϕ_s obtained by Equations 3.64, 3.68, and 3.70, respectively, for an MOS capacitor system on a *p*-type substrate with $N_a = 1 \times 10^{16}$ cm^{-3}.

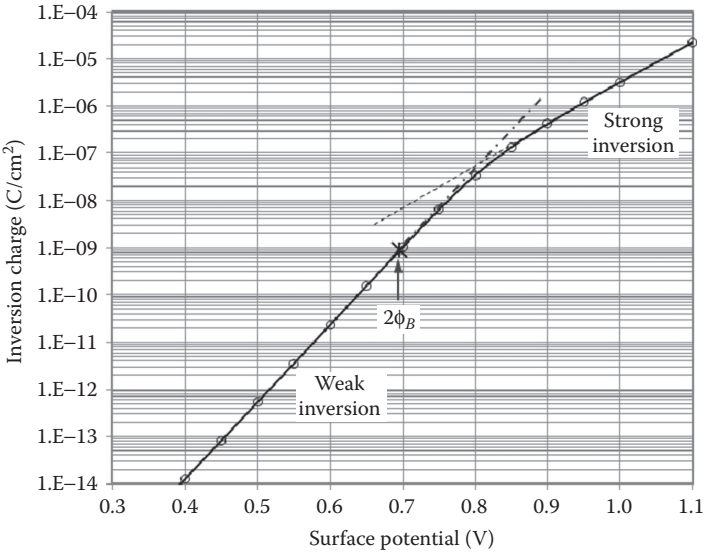

FIGURE 3.15
Variation of Q_i as function of ϕ_s for an MOS capacitor with p-type silicon substrate obtained by Equation 3.70; the plot shows the weak and strong inversion regions; here $N_a = 1 \times 10^{16}$ cm^{-3} and $V_{fb} = 0$.

weak and strong inversion regions is defined by $\phi_s = 2\phi_B$; that is, the inversion carrier concentration becomes equal to that of the majority carrier at the surface.

In order to distinguish the transition region between the weak and strong inversions, the inversion regime is divided into three regions. The third region that lies between the weak and strong inversion is called the moderate inversion region, which lies between $2\phi_B$ and $(2\phi_B + 6v_{kT})$ as shown in Figure 3.16. According to this convention, the region beyond $(2\phi_B + 6v_{kT})$ is the strong inversion region [7].

From the general expression of Q_i Equation 3.70, we can derive the regional expressions for Q_i at weak and strong inversions.

Weak inversion sets in when the band bending at the surface exceeds ϕ_B and extends to $2\phi_B$, that is, $\phi_B < \phi_s < 2\phi_B$. Within this region, the inversion charge Q_i is small compared to the depletion layer charge Q_b, that is,

$$|Q_i| << |Q_b| \quad \text{(weak inversion)} \tag{3.71}$$

For a small ϕ_s, Equation 3.70 can be simplified to obtain Q_i at weak inversion as

$$Q_i = -\sqrt{2qK_{si}\varepsilon_0 N_a v_{kT}}\, e^{(\phi_s - 2\phi_B)/2v_{kT}} \quad \text{(weak inversion)} \tag{3.72}$$

Equation 3.72 implies that in the weak inversion regime Q_i is essentially an exponential function of the surface potential ϕ_s as shown in Figure 3.15.

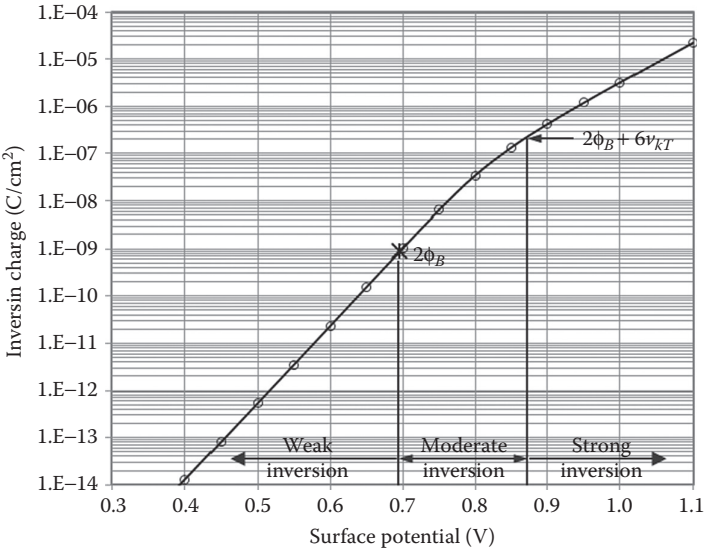

FIGURE 3.16
Variation of Q_i as function of ϕ_s for an MOS capacitor with p-type silicon substrate showing the weak, moderate, and strong inversion regions; Q_i is obtained by Equation 3.70; here $N_b = 1 \times 10^{16}$ cm^{-3} and $V_{fb} = 0$.

Strong inversion is defined when the band bending at the surface is such that $\phi_s >> 2\phi_B$ so that the inversion charge Q_i is large compared to the depletion region charge Q_b, that is,

$$|Q_i| >> |Q_b| \quad (\text{strong inversion}) \tag{3.73}$$

In this case, the exponential term in Equation 3.70 is large compared to ϕ_s and $\phi_s >> 2\phi_B$. Thus, at strong inversion we get

$$Q_i \cong -\sqrt{2qK_{si}\varepsilon_0 N_a v_{kT}}\, e^{(\phi_s/2v_{kT})} \quad (\text{strong inversion}) \tag{3.74}$$

Thus, the inversion charge is an exponential function of the surface potential. Therefore, *a small increment of the surface potential induces a large change in the inversion layer charge*.

Let us now find out the relation between the gate voltage V_g and surface potential ϕ_s. From Equation 3.23 we get

$$V_g = V_{fb} + \phi_s - \frac{Q_s}{C_{ox}} \tag{3.75}$$

Now, substituting for Q_s from Equation 3.68 in Equation 3.23, we get

$$V_g = V_{fb} + \phi_s + \frac{\sqrt{2qK_{si}\varepsilon_0 N_a v_{kT}}}{C_{ox}} \left[\frac{\phi_s}{v_{kT}} + e^{(\phi_s - 2\phi_B)/v_{kT}} \right]^{1/2} \tag{3.76}$$

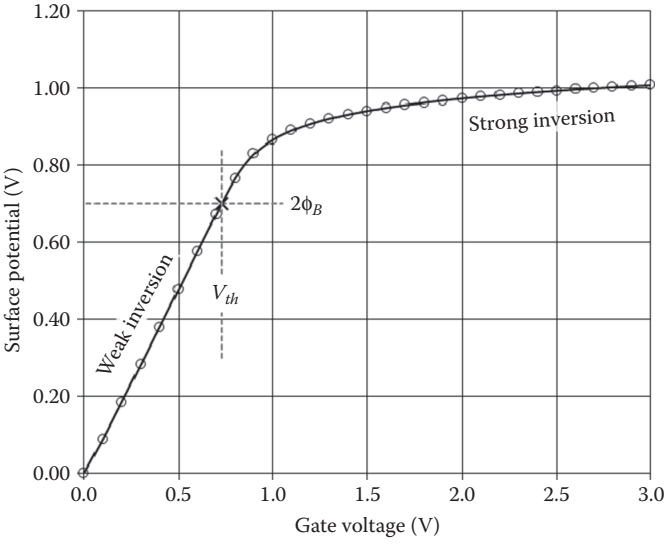

FIGURE 3.17
Surface potential versus gate voltage for a typical MOS capacitor system with *p*-type substrate obtained by numerical solution of Equation 3.76; the condition for strong inversion, at $\phi_s = 2\phi_B$, is also shown on the plot; the parameters used to compute surface potential are: $T_{ox} = 1.5$ nm, $N_a = 1 \times 10^{16}$ cm^{-3}, and $V_{fb} = 0$.

Equation 3.76 is an implicit relation in ϕ_s and must be solved numerically. Figure 3.17 shows the results of ϕ_s versus V_g characteristics obtained by numerical simulation. At low V_g ($>V_{fb}$), ϕ_s and X_d increase reasonably rapidly with V_g. This regime corresponds to the depletion and weak inversion regions of device operation. At larger gate biases, ϕ_s is almost constant and is pinned. This pinning occurs at the onset of strong inversion and the classical condition for pinning is $\phi_s = 2\phi_B$. This condition is referred to as the condition for *threshold* and the corresponding gate voltage is called the *threshold voltage*, V_{th}. Thus, at the onset of inversion, $\phi_s = 2\phi_B$ and $V_g = V_{th}$; then from (3.76), we get

$$\begin{aligned} V_{th} &= V_{fb} + 2\phi_B + \frac{\sqrt{2qK_{si}\varepsilon_0 N_a\left(2\phi_B\right)}}{C_{ox}} \\ &= V_{fb} + 2\phi_B + \gamma\sqrt{2\phi_B} \end{aligned} \tag{3.77}$$

where:

$\gamma \equiv \sqrt{2qK_{si}\varepsilon_0 N_a}\,/\,C_{ox}$ is called the *body effect coefficient* and is dependent on the substrate doping and gate oxide thickness.

V_{th} is one of the most important parameters for MOSFET devices and will be discussed in Chapter 4

Beyond the strong inversion, the concentration of the inversion charge $n(x)$ becomes significant. Therefore, from Equation 3.51 we get

$$\frac{d\phi(x)}{dx} = -\sqrt{\frac{2qN_a v_{kT}}{K_{si}\varepsilon_0}\left[\frac{\phi(x)}{v_{kT}} + \frac{n_i^2}{N_a^2}e^{\phi(x)/v_{kT}}\right]} \tag{3.78}$$

Equation 3.78 must be solved numerically with boundary condition, $\phi(x) = \phi_s$ at $x = 0$. From the solution of $\phi(x)$, the inversion carriers, $n(x)$, can be calculated from Equation 3.42. The numerically calculated $n(x)$ versus depth plot is shown in Figure 3.18. It is seen that the inversion charge distribution is extremely close to the surface with an inversion layer width < 5 nm.

From the previous mathematical formulation, let us find a simple analytical expression for *inversion layer thickness*. We have shown earlier that the general expression for inversion carrier charge is given by $Q_i = -\sqrt{2qK_{si}\varepsilon_0 N_a v_{kT}}\, e^{(\phi_s - 2\phi_B)/2v_{kT}}$. And, from the expression (Equation 3.42), we can show that the minority carrier concentration at the surface $x = 0$ is

$$\sqrt{n(0)} = \sqrt{N_a}\, e^{(\phi_s - 2\phi_B)/2v_{kT}} \tag{3.79}$$

Thus, combining Equations 3.72 and 3.79, we get

$$Q_i = -\sqrt{2qK_{si}\varepsilon_0 v_{kT} n(0)} \tag{3.80}$$

Again, if the inversion layer thickness is X_{inv}, then $Q_i = qn(0)X_{inv}$; then from Equation 3.80 we can show that the classical inversion charge thickness is given by

$$X_{inv} = \frac{Q_i}{qn(0)} = \frac{2K_{si}\varepsilon_0 v_{kT}}{Q_i} \tag{3.81}$$

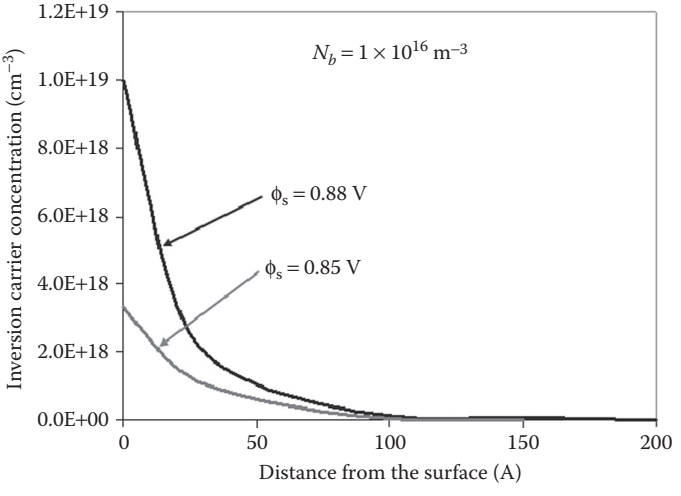

FIGURE 3.18
Calculated minority carrier electron distribution in a *p*-type silicon substrate of an MOS capacitor system for different ϕ_s.

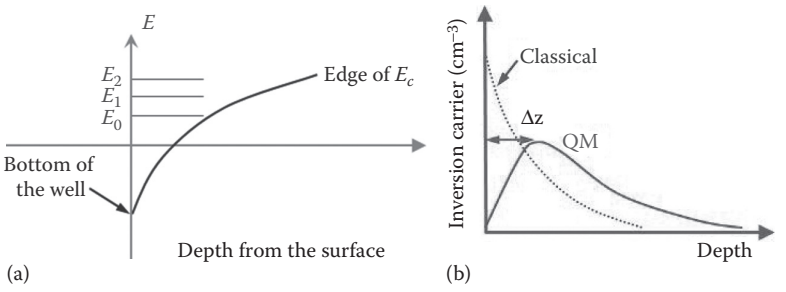

FIGURE 3.19
Inversion layer quantization: (a) minority carrier electron in a potential well of an MOS capacitor system on a *p*-type silicon substrate; the potential well is bounded by potential barrier at the Si/SiO_2 interface and conduction band bending due to high V_g to achieve $\phi_s \geq 2\phi_B$; (b) typical minority carrier electron concentration in silicon surface as a function of silicon depth for classical and QM model; Δz is the shift in the centroid of inversion charge due to quantization.

It is also observed from Equation 3.79 that at the onset of strong inversion defined by $\phi_s = 2\phi_B$, the inversion layer concentration at the surface becomes equal to the majority carrier concentration in the surface, that is, $n(0) = N_b$.

Generally, inversion carriers must be treated quantum-mechanically as a 2D gas molecules. According to quantum mechanical (QM) model, the inversion layer carriers occupy discrete energy bands as shown in Figure 3.19a and the peak distribution is about 1–3 nm away from the surface as shown in Figure 3.19b. Thus, near the silicon surface, the inversion layer charges are confined to a potential well bounded by (1) oxide barrier height at the Si/SiO_2 interface and (2) bend silicon conduction band at the surface due to sufficiently high gate voltage V_g as shown in Figure 3.19a.

Due to QM confinement of inversion layer electrons in the *p*-type silicon surface, the *electron* energy levels are grouped in discrete sub-bands of energy, E_j, where $j = 0, 1, 2, \ldots$ quantized states as shown in Figure 3.19a. Each E_j corresponds to a quantized level for electron motion in the normal direction. The net result of QM effect is that the inversion layer density peaks below the SiO_2/Si interface with about zero value at the surface contrary to the classical inversion carrier distribution as shown in Figure 3.19b. Therefore, for accurate computation of inversion carrier distribution at the silicon surface, we have to solve both Schrödinger and Poisson equations self-consistently with boundary conditions: $\phi(x) = 0$ for $x < 0$ in the oxide; and $\phi(x) = 0$ @ $x = \propto$ deep into the silicon substrate.

As observed from Figure 3.19b, the silicon surface is depleted of mobile carriers due to inversion layer quantization. This depletion region in silicon can be considered as an insulating layer of silicon increasing the effective gate oxide thickness. This increase in the effective gate thickness is given by

$$\Delta T_{ox} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \Delta z \tag{3.82}$$

where:

Δz is the shift in the centroid of inversion charge

Since the peak of the inversion charge is away from the surface due to QM effect, a higher V_g overdrive is required to produce the same level of inversion charge density predicted by classical theory. In other words, QM effect can be considered to reduce the net inversion charge density. Thus, the inversion layer quantization can be modeled as *bandgap widening* due to an increase in the effective bandgap energy, E_g, by an amount ΔE_g [13]. Then from Equation 2.14 relating E_g and the intrinsic carrier concentration, we can show that the intrinsic carrier concentration n_i^{QM} due to QM effect is given by

$$n_i^{QM} = n_i^{CL} \exp\left(-\frac{\Delta E_g}{2kT}\right) \tag{3.83}$$

where:

$\Delta E_g = \left(E_g^{QM} - E_g^{CL}\right)$ is the increase in the apparent value of E_g due to QM effect; here, E_g^{QM} is the energy gap due to QM effect and E_g^{CL} and n_i^{CL} are the energy gap and intrinsic carrier concentration, respectively, without the QM effect denoting the classical expression

Equation 3.83 shows that the inversion layer quantization decreases the intrinsic concentration compared to the classical value. We know from Equation 3.72, Q_i is proportional to n_i through the term $\exp(-2\phi_B/v_{KT})$. Thus, Q_i decreases due to QM effect. This decrease in Q_i due to QM effect has severe consequences on MOS transistor device performance as we will discuss in Chapter 9.

3.5 Capacitance of MOS Structure

In the previous section, we developed the mathematical foundation of MOS capacitor system relating the charge and potential under different gate biasing conditions. In this section, we will discuss the basic characteristics of MOS capacitor system under an applied bias. We know that the capacitance of any system is the ratio of the variation in charge due to the corresponding variation in the small signal voltage. Thus, the total capacitance (C) of an MOS structure in equilibrium is given by

$$C = \frac{d\left(-Q_s\right)}{dV_g} \tag{3.84}$$

From Equation 3.17, the applied bias of an MOS system is $V_g = V_{fb} + V_{ox} + \phi_s$; since V_{fb} is a constant, we can write

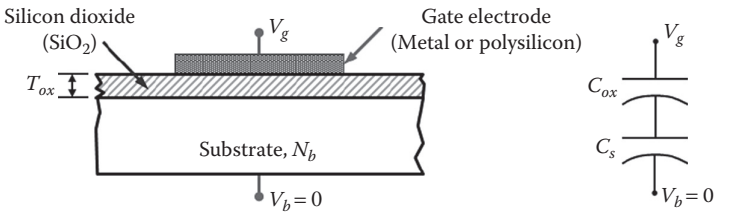

FIGURE 3.20
The individual component of the total MOS capacitor system; C_{ox} and C_s are the capacitance per unit area of the gate oxide capacitance and substrate capacitance, respectively. *Nb* is the substrate concentration.

$$dV_g = dV_{ox} + d\phi_s \tag{3.85}$$

From Equations 3.84 and 3.85, we can show that

$$\frac{dV_g}{d(-Q_s)} = \frac{dV_{ox}}{d(-Q_s)} + \frac{d\phi_s}{d(-Q_s)}$$
$$\therefore \quad \frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{3.86}$$

Thus, the total capacitance of an MOS structure equals the oxide capacitance C_{ox} and the substrate capacitance C_s connected in series as shown in Figure 3.20. Here, C_s is the capacitance per unit area of the space charge region in the silicon.

Equation 3.86 along with Equation 3.53 for Q_s is used to calculate *C–V* characteristics for the target range of operation of MOS capacitor systems. In order to generate *C–V* plot, first of all, we calculate the general expression for the space charge region capacitance C_s in the semiconductor from the total charge Q_s given by Equation 3.53. Then we select an appropriate value of ϕ_s for each mode of operation of an MOS capacitor system to obtain the corresponding *C–V* characteristics.

3.5.1 Low Frequency *C–V* Characteristics

In order to obtain the low frequency (LF) *C–V* characteristics of MOS capacitors, we can show from Equation 3.53

$$C_s = \frac{d(-Q_s)}{d\phi_s} = -\frac{\sqrt{2}K_{si}\varepsilon_0}{L_d} \frac{\left[1 - e^{-(\phi_s/v_{kT})} + \left(n_{p0}/p_{p0}\right)\left(e^{\phi_s/v_{kT}} - 1\right)\right]}{2\left[\left(e^{-(\phi_s/v_{kT})} + \left(\phi_s/v_{kT}\right) - 1\right) + \left(n_{p0}/p_{p0}\right)\left(e^{(\phi_s/v_{kT})} - \left(\phi_s/v_{kT}\right) - 1\right)\right]^{1/2}} \tag{3.87}$$

Equation 3.87 is the general expression for C_s in an MOS capacitor system that we will apply to analyze *C–V* characteristics in the different operational regions of the system discussed in Section 3.3.

3.5.1.1 Accumulation

In strong accumulation, $\phi_s << 0$; then considering the majority carrier term only in Equation 3.87 and recognizing that $\exp(-\phi_s / v_{kT}) >> 1$ and $\exp(-\phi_s / v_{kT}) >> (\phi_s / v_{kT})$, we can show after simplification

$$C_s = \frac{K_{si}\varepsilon_0}{\sqrt{2}L_d} e^{-(\phi_s/2v_{kT})} \tag{3.88}$$

Since $\phi_s << 0$, for large ϕ_s, C_s becomes very large; therefore, from Equation 3.86, we get

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \cong \frac{1}{C_{ox}} \tag{3.89}$$

Thus, in accumulation region

$$C \cong C_{ox}\,(\text{accumulation}) \tag{3.90}$$

3.5.1.2 Flat Band

At flat band condition, $\phi_s = 0$, the inversion charge term (i.e., term containing n_{po}/p_{po}) in Equation 3.87 can be neglected to get

$$C_s = \frac{d(-Q_s)}{d\phi_s} = -\frac{\sqrt{2}K_{si}\varepsilon_0}{L_d} \frac{\left[1 - e^{-(\phi_s/v_t)}\right]}{2\left[\left(e^{-(\phi_s/v_t)} + (\phi_s/v_t) - 1\right)\right]^{1/2}} \tag{3.91}$$

Since the direct substitution of $\phi_s = 0$ in Equation 3.91 results in indeterminate, we simplify Equation 3.91 by series expansion using $e^x = 1 + (x/1!) + (x^2/2!) + (x^3/3!) + \cdots, -\infty < x < \infty$, where $x \equiv -\phi_s/v_{kT}$, then

$$C_s \cong -\frac{\sqrt{2}K_{si}\varepsilon_0}{L_d} \frac{\left(1 - \left\{1 - (\phi_s/v_{kT}) + (1/2)\left[-(\phi_s/v_{kT})\right]^2 + (1/6)\left[-(\phi_s/v_{kT})\right]^3 + \cdots\right\}\right)}{2\left(\left\{1 - (\phi_s/v_{kT}) + (1/2)\left[-(\phi_s/v_{kT})\right]^2 + (1/6)\left[-(\phi_s/v_{kT})\right]^3 + \cdots\right\} + (\phi_s/v_{kT}) - 1\right)^{1/2}}$$

$$= -\frac{\sqrt{2}K_{si}\varepsilon_0}{L_d} \frac{\left[-(\phi_s/v_{kT}) + (1/2)(\phi_s/v_{kT})^2 - (1/6)(\phi_s/v_{kT})^3 + \cdots\right]}{2\left[(1/2)(\phi_s/v_{kT})^2 - (1/6)(\phi_s/v_{kT})^3 + \cdots\right]^{1/2}}$$

$$= -\frac{\sqrt{2}K_{si}\varepsilon_0}{L_d} \frac{\left[-(\phi_s/v_{kT})\right]\left[1 - (1/2)(\phi_s/v_{kT}) - (1/6)(\phi_s/v_{kT})^2 + \cdots\right]}{\sqrt{2}(\phi_s/v_{kT})\left[1 - (1/6)(\phi_s/v_{kT}) + \cdots\right]^{1/2}}$$

$$= \frac{K_{si}\varepsilon_0}{L_d} \frac{\left[1 - (1/2)(\phi_s/v_{kT}) - (1/6)(\phi_s/v_{kT})^2 + \cdots\right]}{\left[1 - (1/6)(\phi_s/v_{kT}) + \cdots\right]^{1/2}}$$

Now we substitute for $\phi_s = 0$ to get

$$C_s(\text{flat band}) \cong \frac{K_{si}\varepsilon_0}{L_d} \frac{\left[1-(1/2)(\phi_s/v_{kT})-(1/6)(\phi_s/v_{kT})^2+\cdots\right]}{\left[1-(1/6)(\phi_s/v_{kT})+\cdots\right]^{1/2}} = \frac{K_{si}\varepsilon_0}{L_d} \tag{3.92}$$

Then from Equation 3.86, the total capacitance of an MOS structure at flat band condition is given by

$$C \equiv C_{fb} = \left(\frac{1}{C_{ox}} + \frac{L_d}{K_{si}\varepsilon_0}\right)^{-1} \quad (\text{flat band}) \tag{3.93}$$

Since $(L_d/K_{si}\varepsilon_0)$ is a finite number, Equation 3.93 shows that C_{fb} is somewhat less than C_{ox}.

3.5.1.3 Depletion

In the depletion regime ($0 < \phi_s < 2\phi_B$), the general expression for C_d is given by Equation 3.87. However, we can derive an approximate expression from depletion approximation discussed in Section 3.4.2.1. We know that at the depletion condition $Q_s \cong Q_b$, then substituting for $Q_s = Q_b$ in Equation 3.23, we get

$$V_g = V_{fb} + \phi_s - \frac{Q_b}{C_{ox}} \tag{3.94}$$

Again, from Equation 3.64 we get:

$$Q_b = -\sqrt{2qK_{si}\varepsilon_0 N_b \phi_s} \quad \text{or} \quad \phi_s = \frac{Q_b^2}{2qK_{si}\varepsilon_0 N_b} \tag{3.95}$$

Then substituting for ϕ_s from Equation 3.95 to Equation 3.94, we can show after simplification

$$V_g - V_{fb} = \frac{Q_b^2}{2qK_{si}\varepsilon_0 N_b} - \frac{Q_b}{C_{ox}} \quad \text{or} \quad Q_b^2 - \left(\frac{2qK_{si}\varepsilon_0 N_b}{C_{ox}}\right)Q_b - 2qK_{si}\varepsilon_0 N_b\left(V_g - V_{fb}\right) = 0 \tag{3.96}$$

Equation 3.96 is a quadratic equation in Q_b with solution given by

$$Q_b = \frac{qK_{si}\varepsilon_0 N_b}{C_{ox}} \pm \sqrt{\left(\frac{qK_{si}\varepsilon_0 N_b}{C_{ox}}\right)^2 + 2qK_{si}\varepsilon_0 N_b\left(V_g - V_{fb}\right)} \tag{3.97}$$

Then from Equation 3.97 we can show that the depletion capacitance is given by

$$C = \frac{dQ_b}{dV_g} = \frac{C_{ox}}{\sqrt{1+\left[2C_{ox}^2\left(V_g - V_{fb}\right)/qK_{si}\varepsilon_0 N_b\right]}} \quad \text{(depletion)} \tag{3.98}$$

From Equation 3.98 we observe that the depletion capacitance C decreases with the increase in V_g. It is clear from Equation 3.98 that for a given voltage (V_g–V_{fb}), the capacitance in the depletion region will be higher for higher N_b as well as lower C_{ox} or thicker T_{ox}. It is also seen from Equation 3.98 that at $V_g = V_{fb}$, $C = C_{ox}$; this is because Equation 3.98 is derived assuming depletion approximation; that is, the transition between the accumulation and depletion region is abrupt.

3.5.1.4 Inversion

In strong inversion, $\phi_s >> 0$; considering only the minority carrier term in Equation 3.87 and recognizing that $\exp(\phi_s / v_{kT}) >> 1$ and $\exp(\phi_s / v_{kT}) >> (\phi_s / v_{kT})$, we can show after simplification

$$C_s \cong -\frac{\sqrt{2}K_{si}\varepsilon_0}{L_d}\frac{\left(n_{p0}/p_{p0}\right)e^{\phi_s/v_{kT}}}{2\sqrt{n_{p0}/p_{p0}}e^{\phi_s/2v_{kT}}} = -\frac{K_{si}\varepsilon_0}{\sqrt{2}L_d}\frac{n_i}{N_b}e^{\phi_s/2v_{kT}} \tag{3.99}$$

where we have used $N_b = p_{po} = N_a$ and $n_{po} = n_i^2 / N_a$. In Equation 3.99, the negative sign indicates that the charge has changed sign. Since $\phi_s >> 0$, for large value of ϕ_s, C_s becomes very large. Therefore, from Equation 3.86, the total capacitance of an MOS capacitor system at strong inversion is given by

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \approx \frac{1}{C_{ox}} \tag{3.100}$$

In a MOS capacitor system, the inversion layer is formed by thermally generated minority carriers (electrons for p-type substrate). The concentration of minority carriers can change only as fast as carriers can be generated within the depletion region near the surface. As a result, the MOS capacitance at inversion is a function of the frequency of the AC signal used to measure the capacitance. If the AC signal is sufficiently low (typically, 10 Hz), the inversion layer charge can respond to the AC bias and the DC sweeping voltage, generating LF C–V plot. In this condition, Equation 3.99 is valid and therefore

$$C \cong C_{ox} \quad \text{(inversion at LF signal)} \tag{3.101}$$

However, if the frequency of the AC voltage signal is too high (typically, above 1×10^5 Hz), the inversion charge cannot respond to the changes in AC voltage. As a result, the measured *C–V* curve, called the high frequency (HF) *C–V* plot is significantly different from the LF *C–V* plot. Also, we derived Equation 3.87 assuming that all charges in the depletion region of an MOS capacitor follow the variation of ϕ_s. Thus, Equation 3.87 is valid for LF *C–V* curve. On the other hand, the HF capacitance of an MOS system can be obtained by considering only the depletion charge, Q_b, at the surface and the effective depth, X_d, of the depletion region at inversion condition using parallel plate capacitance formula, $C = K_{si}\varepsilon_0 / X_d$.

In the accumulation and depletion regions of an MOS capacitor system, the minority carrier charge is negligibly small compared to the bulk charge and the total charge at the surface is primarily due to the majority carriers. As a result, MOS capacitance in these regions is independent of frequency at all range of operational frequency.

3.5.2 Intermediate and High Frequency *C–V* Characteristics

We discussed in the previous section that there are plenty of majority carriers in the substrate that can respond to the AC signal. However, the minority carriers are scarce and have to originate by diffusion from the bulk substrate, by generation in the depletion region, or by external sources (e.g., *n*+ diffusion region in MOS transistors). Thus, the inversion charge cannot respond to the applied AC signal higher than 100 Hz. Therefore, at any HF-applied signal to V_g, the inversion charge Q_i is assumed to be a constant, and therefore $Q_b = Q_s$. Thus, at any HF-applied signal to V_g, only Q_b will vary with the signal around its maximum value Q_{bmax}, and X_d will vary with the signal around its maximum value X_{dmax}. Thus, the HF capacitance is given by:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{X_{dmax}}{K_{si}\varepsilon_0} \equiv \frac{1}{C_{min}} \quad \text{(inversion at HF)} \tag{3.102}$$

Now, substituting for X_{dmax} from Equation 3.66 to Equation 3.100, we can show

$$\frac{1}{C_{min}} = \frac{1}{C_{ox}} + \sqrt{\frac{4v_{kT}}{qK_{si}\varepsilon_0 N_b}\ln\left(\frac{N_b}{n_i}\right)} \quad \text{(inversion at HF)} \tag{3.103}$$

3.5.3 Deep Depletion *C–V* Characteristics

We discussed in the previous section that the inversion layer is formed by thermal generation of carriers in the substrate of an MOS capacitor. However, if an MOS capacitor is swept from the accumulation to the inversion regions at a relatively fast rate (e.g., 10 V sec^{-1} and higher) so that there is not enough time for the thermal generation of the minority carriers, the capacitance will continue to fall with increasing magnitude of V_g along the depletion curve.

This is a nonequilibrium condition under which the depletion width continues to widen beyond its maximum value, X_{dmax}, in order to balance the increased gate charge and C does not reach a minimum. This expansion of the depletion region deep into the substrate is referred to as the *deep depletion*. From Equation 3.98, the capacitance in the deep depletion mode is given by

$$C = \frac{K_{si}\varepsilon_0}{X_d} = \frac{C_{ox}}{\sqrt{1+\left[2C_{ox}^2\left(V_g - V_{fb}\right)/qK_{si}\varepsilon_0 N_b\right]}} \quad \text{(deep depletion)} \tag{3.104}$$

The capacitance in the deep depletion is obtained when the rate of DC voltage sweep is high, independent of the frequency of the AC signal voltage (HF) and no inversion charge can form. *The easiest way to obtain deep depletion is to sweep the DC voltage by either applying a voltage step or using a fast voltage ramp on the gate.*

Thus, from the previous mathematical analysis, we find that, depending on the frequency of the AC signal and measurement conditions, three types of *C–V* plots are obtained as shown in Figure 3.21. *It should be pointed out that the frequency dependence of capacitance in inversion is true only for MOS capacitor*

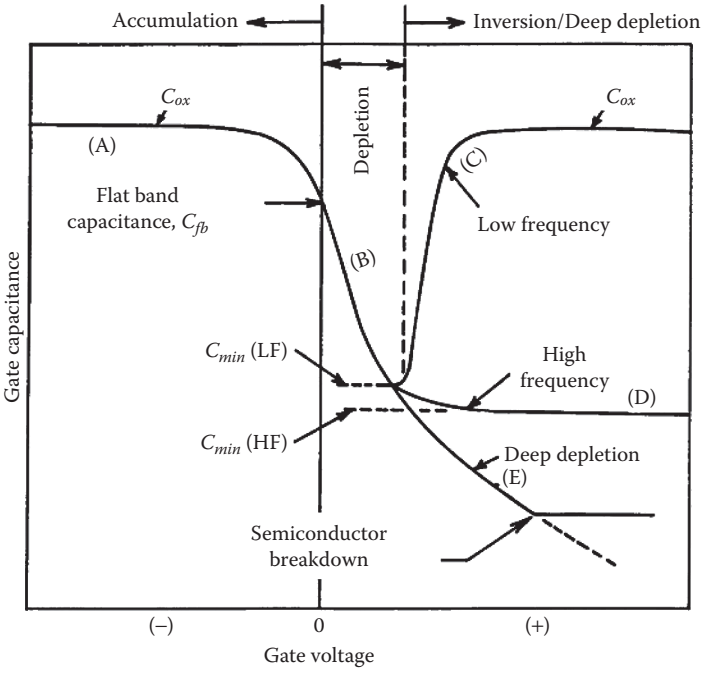

FIGURE 3.21
C–V characteristics of an ideal MOS capacitor system from accumulation to inversion regimes: regions A and B represent the accumulation and depletion, respectively; regions C and D represent the LF and HF inversion capacitances, respectively; and plot E shows deep depletion.

and not for MOS transistors. In the case of MOS transistors, the source and drain diffusions can supply minority carriers to the inversion layer almost instantaneously.

3.5.4 Deviation from Ideal *C–V* Curves

The ideal MOS capacitance plots shown in Figure 3.21 are obtained by assuming that the gate oxide is a perfect insulator free of charges ($Q_0 = 0$) and $\Phi_{ms} = 0$, so that $V_{fb} = 0$. However, due to the nonideal nature of the MOS structures, experimental LF and HF *C–V* plots deviate from the ideal behavior by one or more of the following parameters: (1) nonzero Φ_{ms}, (2) interface traps, (3) mobile ions in the oxide, (4) fixed charge, and (5) nonuniform substrate doping. The detailed description of the nonideal behavior of MOS capacitor system is available in the literature [2].

3.5.5 Polysilicon Depletion Effect on *C–V* Curves

In our discussions so far we assumed that the polysilicon gate is degenerately doped with concentration in excess of 5×10^{19} cm^{-3}. However, if the gate is nondegenerately doped, it can no longer be treated as an equipotential area like metal gate. In this case, the capacitance given by Equation 3.86 for a MOS capacitor system must be modified to include the capacitance C_{poly} due to polysilicon depletion at the polysilicon-gate/gate-dielectric interface. For polysilicon gate MOS capacitor, the capacitance, C, of the system is a series combination of: (1) polysilicon depletion capacitance, C_{poly}; (2) oxide capacitance, C_{ox}; and (3) substrate capacitance, C_s, as shown in Figure 3.22b. Then the resulting gate capacitance at strong inversion is given by [14]

$$\frac{1}{C} = \frac{1}{C_{poly}} + \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{3.105}$$

Typical MOS *C–V* characteristics due to polysilicon gate depletion effect is shown in Figure 3.23. It is observed from Figure 3.23 that as V_g increases in the inversion regime, C_{poly} decreases due to the increase in the depletion width, $X_{poly\text{-}depletion}$ of polysilicon gate causing a decrease in the total capacitance C and thereby C/C_{ox}. Therefore, LF *C–V* plots show a local maximum at a certain V_g.

The *C–V* behavior shown in Figure 3.23 is attributed to the deviation from the nondegenerate doping of the polysilicon gate [14–19]. The result of the nondegenerate polysilicon doping is that the LF capacitance in inversion ($C_{g,inv}$) is much smaller than that of accumulation, and $C_{g,inv}$ decreases slightly with gate bias. However, at gate bias larger than a certain voltage $C_{g,inv}$ recovers to C_{ox} rather abruptly [14–19].

The decrease in capacitance due to polysilicon depletion effect can be expressed as an increase in the effective gate oxide thickness. The increase in

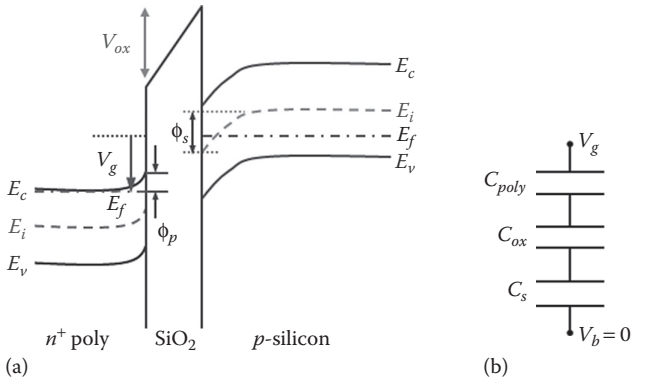

FIGURE 3.22
Polysilicon depletion effect in a polysilicon/SiO_2/p-type silicon substrate MOS capacitance system: plot shows (a) the band bending at strong inversion along with (b) the components of the associated capacitance with the structure.

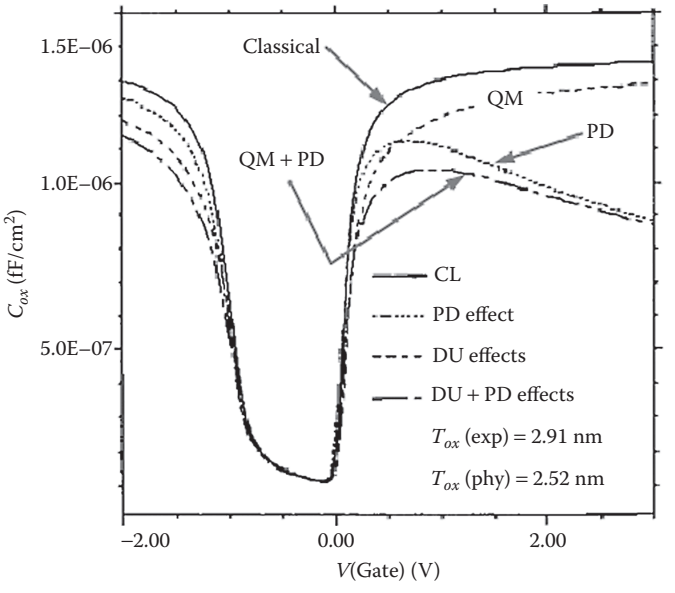

FIGURE 3.23
Low frequency *C–V* characteristics of polysilicon gate MOS capacitor system showing the impact of QM and poly-depletion (PD) effects on MOS capacitance system. (Data from S. Saha et al., *Mater. Res. Soc. Symp. Proc.*, 567, 275–282, 1999.)

effective SiO_2 gate oxide thickness can be shown to be ΔT_{ox}(poly-depletion) = $(K_{ox}/(K_{si})(X_{d,PD})$, where $X_{d,PD}$ is the width of the depletion region in the polysilicon at the polysilicon/SiO_2 interface. The total increase in the physical gate oxide thickness is the sum of the effective SiO_2 thickness due to QM effect expressed in Equation 3.82 and polysilicon depletion effect and is given by

$$\Delta T_{ox} = \frac{K_{ox}}{K_{si}}\left(\Delta z + X_{d,PD}\right) \tag{3.106}$$

where:

Δz and $X_{d,PD}$ are the centroid of inversion charge and width of the polysilicon depletion region, respectively

The increase in the effective gate oxide thickness due to polysilicon depletion and QM effects is about 0.5–0.7 nm and depends on the gate voltage and polysilicon doping density [18–19].

3.6 Summary

This chapter presented the basic structure and operation of an MOS capacitor system to build the foundation for developing MOS transistor compact models. We have discussed the basic MOS structure by considering the energy band model of metal, oxide, and semiconductors. The basic operation of an MOS capacitor system is discussed at equilibrium and under biasing conditions. The important parameter of the MOS structure is the flat band voltage V_{fb}. The significance of V_{fb} and the work function difference between the metal and semiconductor for MOS operation is clearly discussed using the energy band diagram. Analytical model of MOS capacitor system is developed to discuss the accumulation, depletion, and inversion mode operations of MOS capacitor structures. Finally, the analytical expressions to understand the *C–V* characteristics of MOS structures at different operation regimes are also presented.

Exercises

3.1 Consider an MOS capacitor system on a uniformly doped *p*-type substrate with doping concentration $N_a = 1 \times 10^{17}$ cm^{-3}. Calculate the flat band voltage. Assume that Si/SiO_2 interface charge is negligibly small. *Clearly state any assumptions you make.*

3.2 Consider an MOS capacitor system on a uniformly doped *p*-type substrate with doping concentration $N_a = 1 \times 10^{17}$ cm^{-3} operating in the accumulation region.

a. Sketch the band diagram into the substrate and clearly explain and label all relevant parameters such as:
   i. Surface potential
   ii. Fermi potential
   iii. Energy levels with reference to Si/SiO_2 interface.

b. Write one-dimensional Poisson equation that you will solve to obtain the surface potential in the accumulation region.

c. Derive an expression for the accumulation charge.

d. Derive an expression for surface potential.

Clearly state any assumption you make.

3.3 In Equation 3.40, we find that the inversion carrier density, $n(x)$ in a p-type substrate increases exponentially as $exp(\phi(x)/v_{kT})$ as x approaches to the surface at $x = 0$. In other words, we can consider, $n(x)$ decreases away from the surface as $\exp(-\phi(x)/v_{kT})$ and approaches to a minimum value at $x = X_{inv}$, defined as the inversion layer thickness. Thus, all the minority carrier electrons are confined in a region bounded by the depth X_{inv}, where the intrinsic band energy, E_i intersects the Fermi level, E_f. Here, $\phi(x)$ is the potential at any point x from the surface and v_{kT} is the thermal voltage at the ambient temperature T. If an MOS capacitor system on a uniformly doped p-type substrate with doping concentration $N_a = 1 \times 10^{17}$ cm^{-3} operating in the inversion region,

a. Calculate the maximum width of the depletion layer into the silicon (x-direction).

b. Considering the inversion carrier concentration, $n_{inv} \propto \exp(-\phi/v_{kT})$ along x-direction into the silicon and $n_{inv} \sim 0$ @ $x = X_{inv}$ whereas $n_{inv} = n_{surf}$ and $\phi = \phi_s$ @ $x = 0$:

   i. Calculate the potential drop $\Delta\phi$ @ $x = X_{inv}$.

   ii. Now assume that the device is in *weak inversion* ($\phi_B < \phi_s < 2\phi_B$) so that $Q_b >> Q_{inv}$, then use Gauss's law and $\Delta\phi$ expression from part (b)(i) to show:

$$X_{inv} = v_{kT}\sqrt{\frac{K_{si}\varepsilon_0}{2qN_a\phi_s}}$$

   where:

   ϕ is the potential at any point in silicon

   K_{si} is the dielectric constant of silicon

   ε_0 is the permittivity of free space

   ϕ_s is the surface potential

c. Calculate the thickness of the inversion layer, X_{inv} in silicon.

d. Sketch the band diagram into the substrate and clearly explain and label the following parameters with reference to Si/SiO_2 interface:

   i. Surface potential, ϕ_s

   ii. Bulk potential, ϕ_B

iii. Energy levels (E_c, E_i, E_f, E_v, E_g)
iv. Width of the depletion layer, X_d
v. Width of the inversion layer, X_{inv}

Clearly state any assumptions you make.

3.4 Use Equation 3.52 to calculate and plot the total charge (Q_s) in semiconductor as a function of surface potential ϕ_s of an MOS capacitor system for $-0.4\ \text{V} \leq \phi_s \leq 1.4\ \text{V}$. Label all the operating regions of the MOS capacitor system. Assume that the MOS capacitor is fabricated on a uniformly doped *p*-type substrate with doping concentration $N_a = 1 \times 10^{17}\ \text{cm}^{-3}$. *Clearly state any assumptions you make.*

3.5 Consider an MOS capacitor system with uniformly doped *p*-type substrate with doping concentration, N_a, to show the following:

a. $n_i^2 / N_a^2 = \exp(-2\phi_B / v_{kT})$, where n_i, ϕ_B, and v_{kT} are the intrinsic carrier concentration, bulk potential, and thermal voltage, respectively.

b. Complete the mathematical steps to express Equations 3.52 to 3.53 in terms of Debye length L_d given by Equation 3.54.

3.6 Consider a double gate MOS capacitor system shown in Figure E3.1 fabricated on a lightly doped, $N_a = 5 \times 10^{15}\ \text{cm}^{-3}$, *p*-type substrate with $t_{si} = 30$ nm, $L_g = 45$ nm, and $T_{ox} = 1.5$ nm as shown in Figure E3.1, and gates connected together. *Clearly state any assumptions you make* to answer the following questions.

a. Calculate the total width of the depletion region in silicon at strong inversion, if $t_{si} \rightarrow \propto$.

b. Calculate the total width of the inversion layer at strong inversion. Assume that the inversion layer thickness by a single gate is given by

$$X_{inv} = \frac{kT}{q}\sqrt{\frac{K_s\varepsilon_0}{2qN_a\phi_s}}$$

where:

k is the Boltzmann constant
T is the temperature
q is the electronic charge
K_{si} is the dielectric constant in silicon
ε_0 is the permittivity of free space
N_a is the channel doping concentration
ϕ_s is the surface potential

c. Use the values of the parameters in parts (a) and (b) to sketch the band diagram into silicon from $x = 0$ at the top gate Si/SiO_2

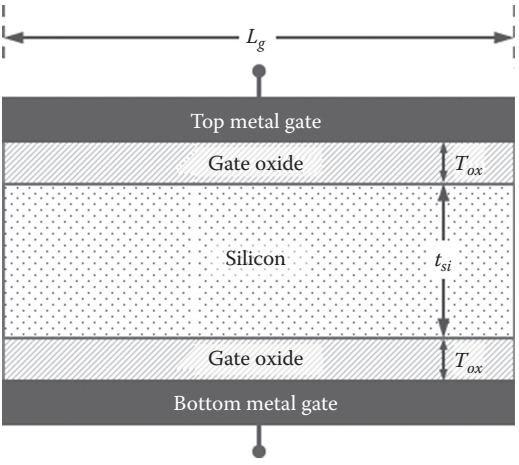

FIGURE E3.1
An ideal double gate MOS capacitance structure.

interface to $x = t_{si} = 30$ nm at the bottom gate Si/SiO_2 interface. Clearly define and label all relevant data points such as

i. Surface potential
ii. Fermi potential
iii. Depletion width
iv. Inversion layer thickness
v. Energy levels.

d. Calculate and plot the potential into the silicon from the top gate to the bottom gate at strong inversion for the top gate only. Repeat the calculation for the bottom gate only and plot on the same *X*–*Y* graph. Show the overall potential distribution from the top gate to the bottom gate when both gates are considered. Clearly define and label all relevant data points. Explain.

3.7 FinFETs with intrinsic or very lightly doped channel doping shown in Figure E3.2 are the most realistic double gate MOSFETs. Consider a simple FinFET capacitor fabricated on a lightly doped *p*-type substrate with $N_a = 3 \times 10^{15}$ cm^{-3}, $T_{fin} = 20$ nm, $H_{fin} = 50$ nm, $L_g = 50$ nm, $T_{ox} = 15$ nm, and gates connected together, as shown in Figure E3.2. (Ignore the effect of Source/Drain on the MOS capacitor system).

a. Calculate the depletion width of silicon at strong inversion.

b. Calculate the width of the inversion layer at strong inversion. Assume that the inversion layer thickness for a single gate is given by

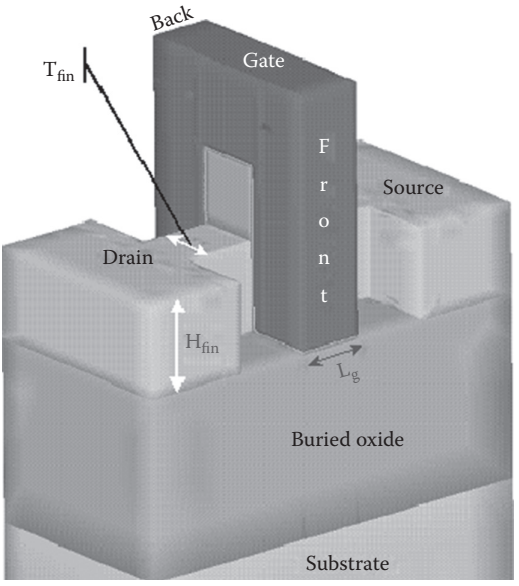

FIGURE E3.2
FinFET MOS device structure.

$$X_{inv} = \frac{kT}{q}\sqrt{\frac{K_s\varepsilon_0}{2qN_a\phi_s}}$$

c. Use the values of the parameters in parts (a) and (b) to sketch the band diagram into the silicon fin from $x = 0$ at the front-gate Si/SiO_2 interface to $x = T_{fin}$ at the back-gate Si/SiO_2 interface. Clearly define and label all relevant data points such as:
   i. Surface potential
   ii. Fermi potential
   iii. Depletion width
   iv. Inversion layer thickness
   v. Energy levels.

d. Calculate and plot the potential into the silicon fin from the front gate to the back gate at weak inversion ($\phi_s = 1.5\phi_B$) and strong inversion on the same *X–Y* graph. Clearly define and label all relevant data points. Explain.

3.8 A *p*-type MOS capacitor with $N_a = 1 \times 10^{18}\ cm^{-3}$ and $T_{ox} = 3$ nm is fabricated to characterize the van Dort's analytical bandgap widening QM model. Due to the inversion layer quantization, the increase in the effective bandgap $\Delta E_g = E_g^{QM} - E_g^{CL} = 104\,mV$. Here, E_g^{QM} and E_g^{CL}

represent the QM and classical (CL) values of bandgap (E_g), respectively. Assume $Q_o = 0$, $V_{sub} = 0$, and n+ poly gate.

a. Show that the intrinsic carrier concentration due to QM effect is given by

$$n_i^{QM} = n_i^{CL} \exp\left(-\frac{\Delta E_g}{2kT}\right)$$

b. Calculate the value of n_i^{QM} at the ambient temperature $T = 300^oK$.

c. If the shift in the centroid of inversion charge, $\Delta z \cong 1$ nm due to the QM effect in the p-substrate, estimate the value of T_{ox}(eff) at strong inversion due to QM effect of the metal gate capacitor.

d. Estimate the ratio of C/C_{ox} at strong inversion for metal gate capacitor in part (c). Here, C = bias-dependent capacitance of MOS system at strong inversion and C_{ox} = gate oxide capacitance. What is your conclusion on (C/C_{ox}) at strong inversion?

e. If the capacitor is fabricated using n+ polysilicon gate with doping concentration 1×10^{19} cm^{-3}, calculate the value of T_{ox}(eff) at strong inversion. Assume that the depletion width of silicon and polysilicon is given by the same expression.

f. Estimate the ratio of C/C_{ox} at strong inversion for polysilicon gate capacitor in part (e). Here, C = bias-dependent capacitance of MOS system at strong inversion and C_{ox} = gate oxide capacitance. What is your conclusion on (C/C_{ox}) at strong inversion?

3.9 An MOS capacitor is built with the structure shown in Figure E3.3. Both the n-type and p-type silicon regions are uniformly doped with concentration 1×10^{17} cm^{-3} and the areas of both the capacitors over the n-type and p-type regions are the same and T_{ox} = 200 nm. The threshold voltages for the n- and p-substrates are –1 V and +1 V, respectively. Sketch the shape of the HF (1 MHz) C–V curve that you would expect to measure for this structure. Calculate the maximum and minimum values of the composite capacitor per unit area. Label as many points as possible and explain.

3.10 Consider an MOS capacitor system on a uniformly doped p-type silicon substrate with doping concentration $N_a = 1 \times 10^{16}$ cm^{-3} at room temperature. Assume $V_{fb} = 0$ and wherever necessary $T_{ox} = 20$ nm.

a. Calculate and plot the inversion, bulk, and total charge Q_i, Q_b, and Q_s, respectively, in the substrate of the capacitor on the same plot. Clearly label all relevant parameters and explain.

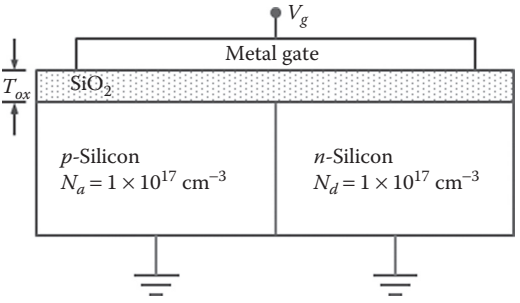

FIGURE E3.3
An MOS capacitor system.

b. Calculate and plot $\log(Q_i)$ versus surface potential ϕ_s for $\phi_s = 0.3$ to 1.1. Clearly, label different operating regimes of the MOS capacitor system and explain.

c. Calculate and plot ϕ_s versus gate voltage V_{gs} for $V_{gs} = 0$ to 3.0 V. Clearly label different operating regimes of the MOS capacitor system and explain.

3.11 Consider an MOS capacitor system on a uniformly doped *p*-type silicon substrate. In Section 3.4, MB probability distribution function is used to solve Poisson's equation in obtaining the surface charge Q_s in the semiconductor of the MOS capacitor system as a function of surface potential. Use the same procedure as in Section 3.4 and FD probability distribution function to obtain an expression similar to Equation 3.52 for Q_s as a function of surface potential in the semiconductor of the same MOS-capacitor system. Plot Q_s versus surface potential and compare with the plot in Figure 3.12.