CprE 381 – Computer Organization and Assembly-Level Programming

Lab-03 Report

Student Name _____Ben Pierre_____

Section / Lab Time _____10_____

Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-03 instructions for the context of the following questions.

a. [Prelab] At the end of Chapter 5, answer question 5. At the end of Chapter 7, answer exercise 2.

b. [Prelab] In your Lab #3 report PDF, provide the Canvas group name for your project team, and a listing of its members. On a scale of 1-10, how comfortable with VHDL does each team member currently feel?

Section 10 – group (1-10)
Ben 5
Tommy 4.99

c. [Part 1 (a)] Draw the interface description for the MIPS register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?

```
-- 32bit 32reg file--
entity Mips_Reg is
        port(clk, ,reset,ctrl : in std_logic;
                rd : in std_logic_vector(31 Downto 0);
                rt : out std_logic_vector(31 downto 0);
                rs : out std_logic_vector(31 downto 0);
                wloc, rloca, rlocb : in std_logic_vector(4 downto 0));
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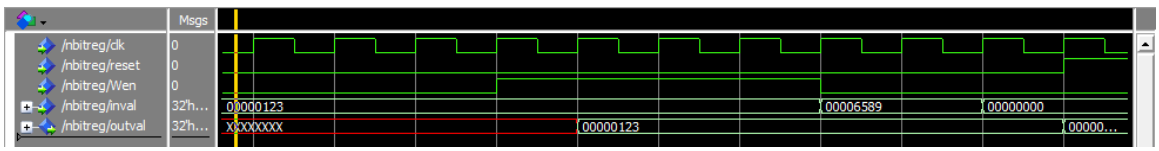
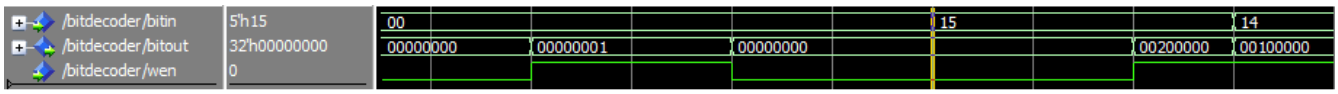
d. [Part 1 (b)] Create an N-bit register using this flip-flop as your basis.

e. [Part 1 (c)] Waveform.



f. [Part 1 (d)] What type of decoder would be required by the MIPS register file and why?
5bit to 32bit

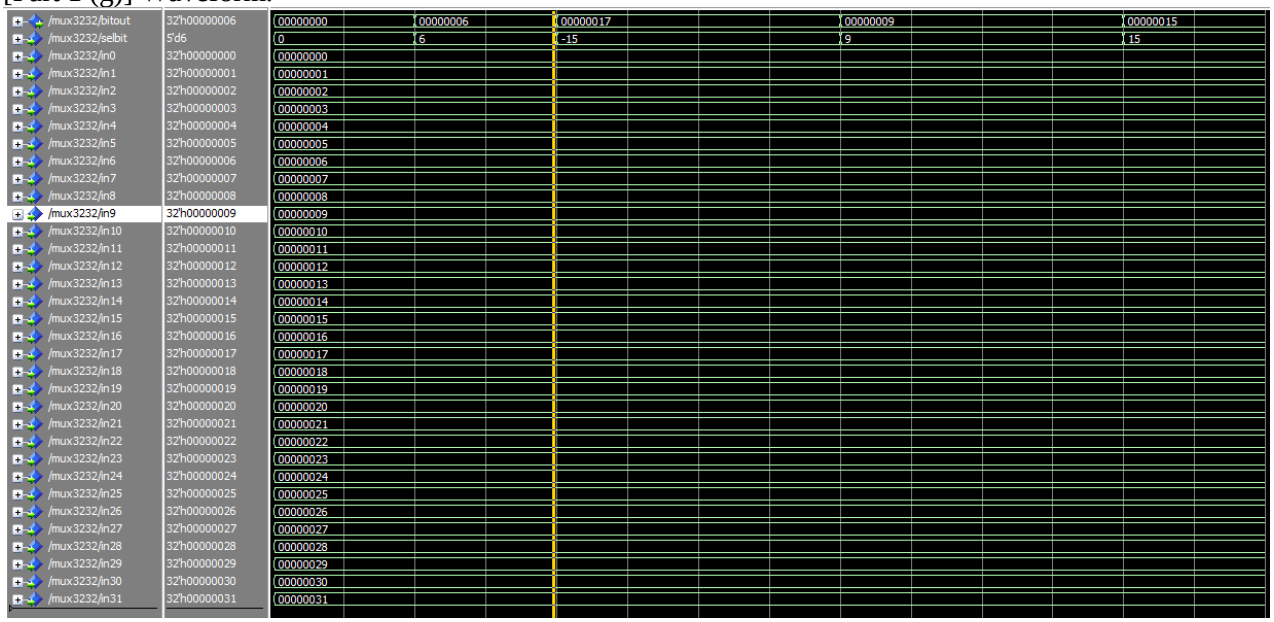
g. [Part 1 (e)] Waveform.



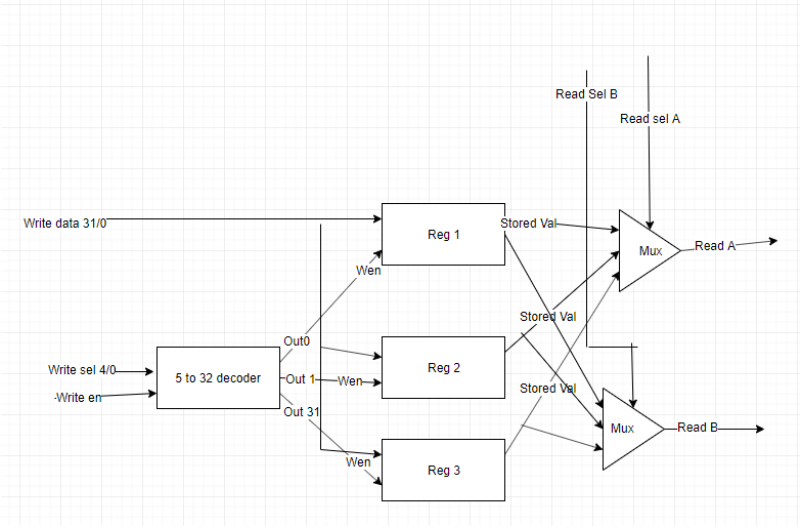
h. [Part 1 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.

I plan on implementing 32 multiplexers that are each 32-1, this will allow us to have a 32bit 32 to one multiplexer. This would be difficult to implement in Verilog so I intend to replicate it with a case statement.

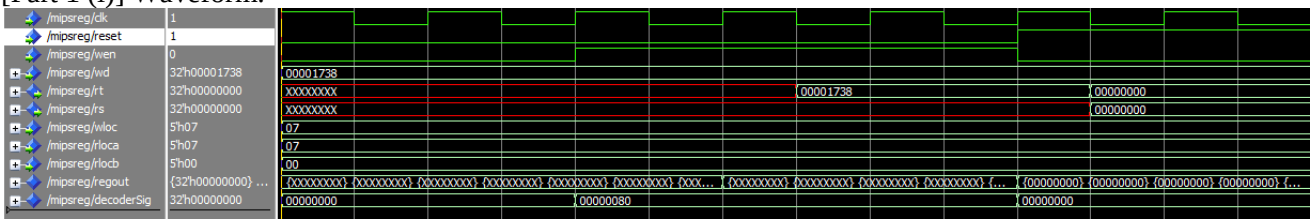
i. [Part 1 (g)] Waveform.



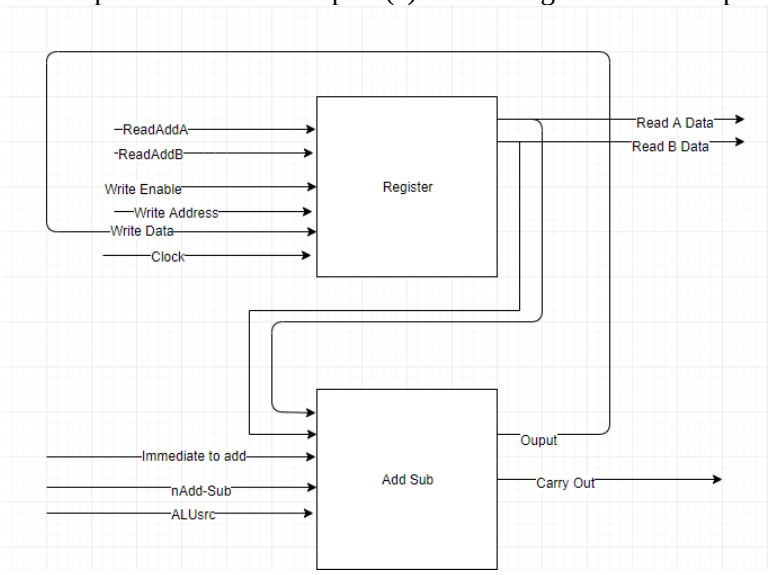
j. [Part 1 (h)] Draw a (simplified) schematic for the MIPS register file, using the same top-level interface ports as in your solution for part a), and using only the VHDL components you have created in parts (b), (e), and (g).



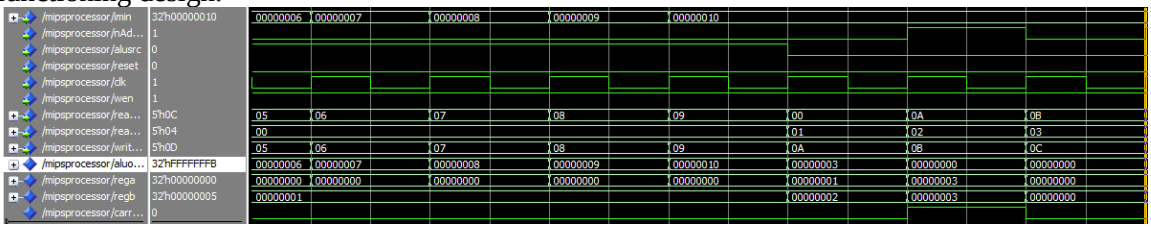
k. [Part 1 (i)] Waveform.



l. [Part 2 (b)] Draw a schematic of the simplified MIPS processor datapath consisting only of the component described in part (a) and the register file from problem (1).



m. [Part 2 (c)] Include in your report waveform screenshots that demonstrate your properly functioning design.



n. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	0	0
Pencil/paper design	0	0
VHDL design	1.5	4.5
Assembly coding	0	
Simulation	.5	.5

Debugging	0	0
Report writing	0	0
Other:	0	0
Total	2	5

ii. If you could change one thing about the lab experience, what would it be? Why?

It would be nice to have a testing program that we could just run, instead of slowly translating machine code, also it would be nice to actually learn some of this stuff in an instruction form instead of just figuring it out ourselves, for example arrays and running batches of commands.

iii. What was the most interesting part of the lab?

I just made a dang cpu dude. That's cool.