CprE 381 – Computer Organization and Assembly-Level Programming

Lab-04 Report

Student Name _____Ben Pierre_____

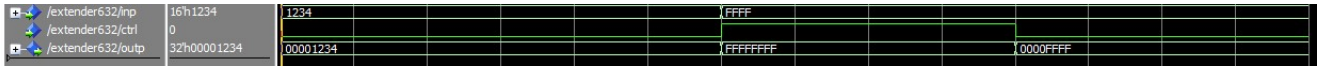
Section / Lab Time _____2_____

Submit a typeset pdf version of this on Canvas by the due date. Refer to the highlighted language in the Lab-04 instructions for the context of the following questions.

a. [Prelab] Based on the waveforms, provide a description in your own words of how this component operates. This can be in the form of a textual description, flow chart, or state machine

b. [Part 1 (a)] What are the MIPS instructions that require some value to be sign extended? What are the MIPS instructions that require some value to be zero extended?
Addi, addiu, lbu, ll,sltiu.
Andi, ori

c. [Part 1 (b)] what are the different 16-bit to 32-bit "extender" components that would be required by a MIPS processor implementation?
8-16 sign extend, 8-16 zero extend, 16 to 32 sign extend, 16 to 32 zero extend



d. [Part 2 (b)] Provide a 2-3 sentence description of each of the individual ports (both generic and regular). The mem file uses DATA_WIDTH and ADDR_WIDTH which define the width of the data busses. These numbers are natural which means they must be above zero but below 2147483647, allowing for less memory usage.
Clk is a constantly toggling port. As it toggles the registers in the file will change values.
Addr : defines where we are writing to. The register at this point will have the data on data stored to it. This also shows where to read from.
Data : The data to be written. This data will be stored at the register defined by addr.
We : enables the writing of values to the memory. This is hardcoded to 1.
Q : the data at the current address. This is valid all the time.

e. [Part 2 (c)] Waveform.

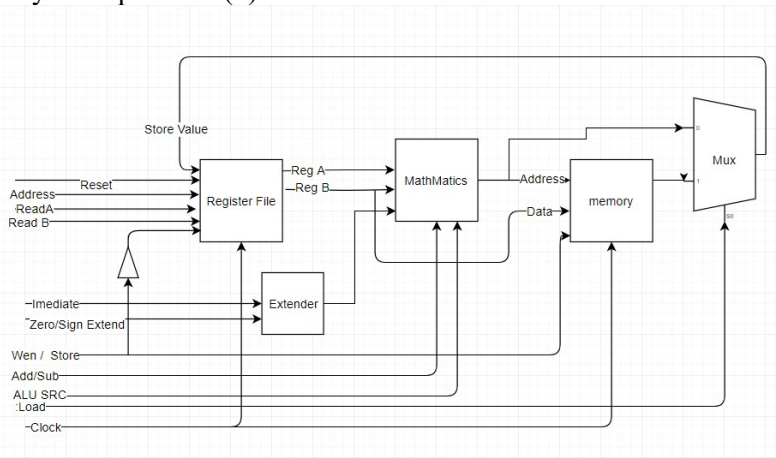
f. [Part 2 (d)] Briefly describe how the waveforms for this mem.vhd module differ from those that you analyzed as part of the pre-lab.

We only have a waveform for one memory location, and don't have a byteena. If we were able to see all five memory blocks like in the prelab as well byteena to write to different portions of memory we would see very similar results.

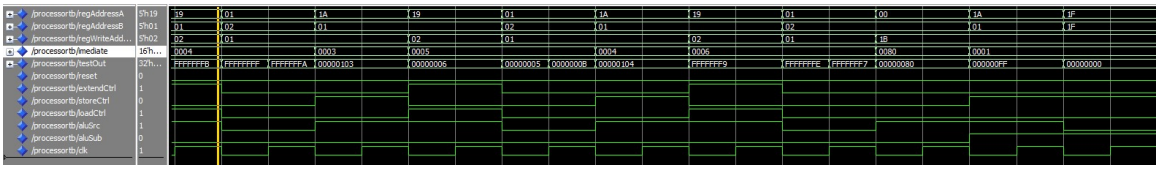
g. [Part 3 (a)] what control signals will need to be added to the simple processor from Lab #3? How do these control signals correspond to the ports on the mem.vhd component analyzed in problem 2)?

We need to add a control signal to decide if we want to write to memory or a register. We also need a control signal to decide if we want to read from memory or a register. And finally we need to be able to choose between using an extended number and a raw number.

h. [Part 3 (b)] Draw a schematic of a simplified MIPS processor consisting only of the base components used in Lab #3, the extender component described in problem (1), and the data memory from problem (2).



i. [Part 3 (c)] Waveform.

j. 

31	0	0	0	0	128
26	256	0	0	0	0
21	0	0	0	0	0
16	0	0	0	0	0
11	0	0	0	0	0
6	0	0	0	0	-7
1	-2	0			
-4					

273	X	X	X	X	X
268	X	X	X	5	-1
263	4	-3	3	-2	X
258	X	X	X	X	X
253	X	X	X	X	X
248	X	X	X	X	X
243	X	X	X	X	X
238	X	X	X	X	X
233	X	X	X	X	X
228	X	X	X	X	X
223	X	X	X	X	X
218	X	X	X	X	X
213	X	X	X	X	X
208	X	X	X	X	X
203	X	X	X	X	X
198	X	X	X	X	X
193	X	X	X	X	X
188	X	X	X	X	X
183	X	X	X	X	X
178	X	X	X	X	X
173	X	X	X	X	X
168	X	X	X	X	X
163	X	X	X	X	X
158	X	X	X	X	X
153	X	X	X	X	X
148	X	X	X	X	X
143	X	X	X	X	X
138	X	X	X	X	X
133	X	X	X	X	X
128	X	X	X	X	X
123	X	X	X	X	X
118	X	X	X	X	X
113	X	X	X	X	X
108	X	X	X	X	X
103	X	X	X	X	X
98	X	X	X	X	X
93	X	X	X	X	X
88	X	X	X	X	X
83	X	X	X	X	X
78	X	X	X	X	X
73	X	X	X	X	X
68	X	X	X	X	X
63	X	X	X	X	X
58	X	X	X	X	X
53	X	X	X	X	X
48	X	X	X	X	X
43	X	X	X	X	X
38	X	X	X	X	X
33	X	X	X	X	X
28	X	45056	40960	X	X
23	X	X	X	X	X
18	X	X	X	X	10
13	-9	8	-7	6	-5
8	4	-3	2	0	
3					

k. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	0	0
Pencil/paper design	0	0
VHDL design	2	2
Assembly coding	0	1
Simulation	1	1
Debugging	1	1.5
Report writing	0	0
Other:	0	0
Total	4	5.5

ii. If you could change one thing about the lab experience, what would it be? Why?

I didn't understand a good chunk of it and I'm not really confident in my answers, a way to check it would be nice.

iii. What was the most interesting part of the lab?
    i. I got some Cheetos during the lab, loved that, also writing to ram was admittedly very cool.