

CprE 381 – Computer Organization and Assembly-Level Programming

Lab-02 Report

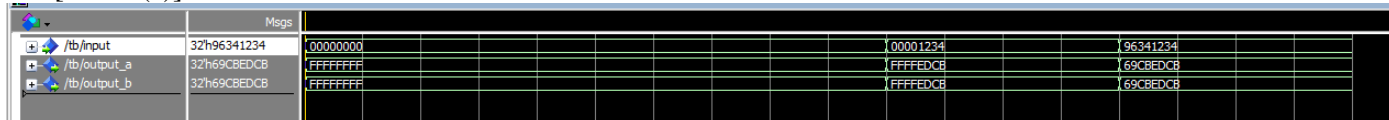
Student Name ____Ben Pierre____

Section / Lab Time ____10____

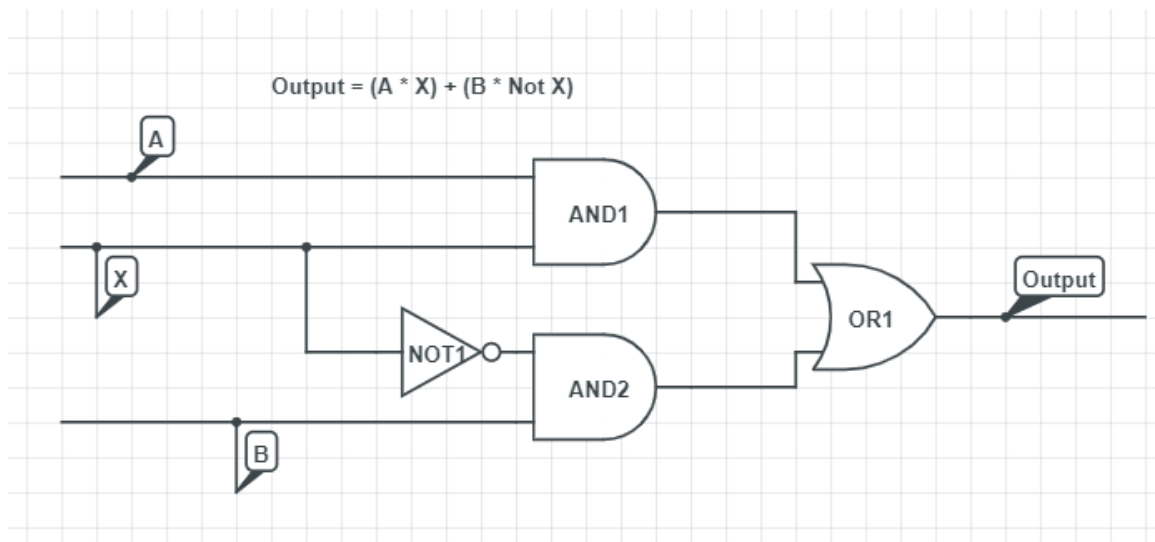
Submit a typeset pdf version of this on Canvas by the due date (i.e., the start of your next lab section). Refer to the highlighted language in the Lab-02 instructions for the context of the following questions.

a. [Prelab] At the end of Chapter 3, answer questions 4b), 5a), and 6.

b. [Part 1 (c)] Waveform.

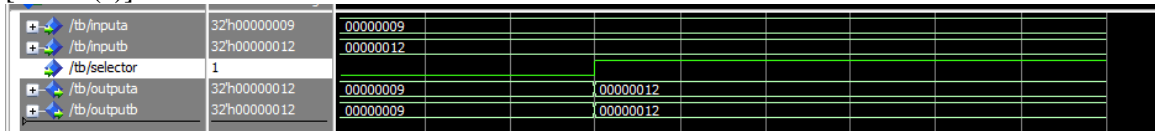


c. [Part 2 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a 2:1 mux.



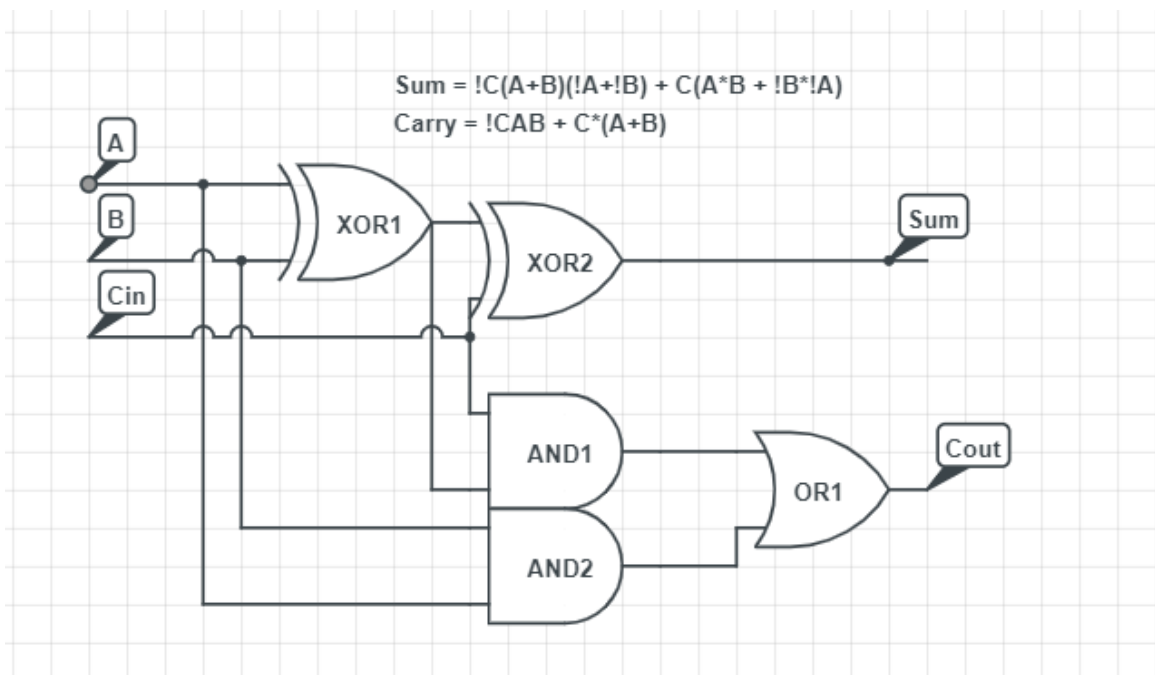
A	B	X	Output	
0	0	0	0	
0	1	0	0	
1	0	1	1	
1	1	1	1	

d. [Part 2 (e)] Waveform.

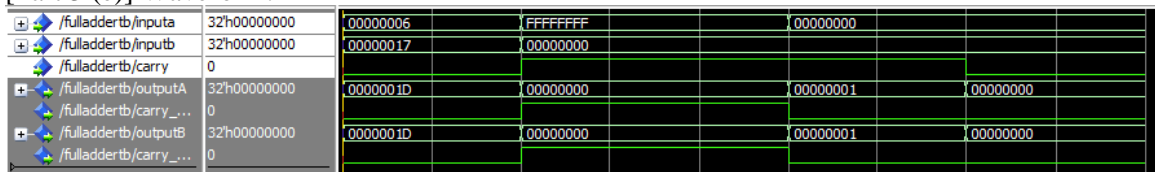


e. [Part 3 (a)] Draw the truth table, Boolean equation, and Boolean circuit equivalent (using only two-input gates) that implements a full adder.

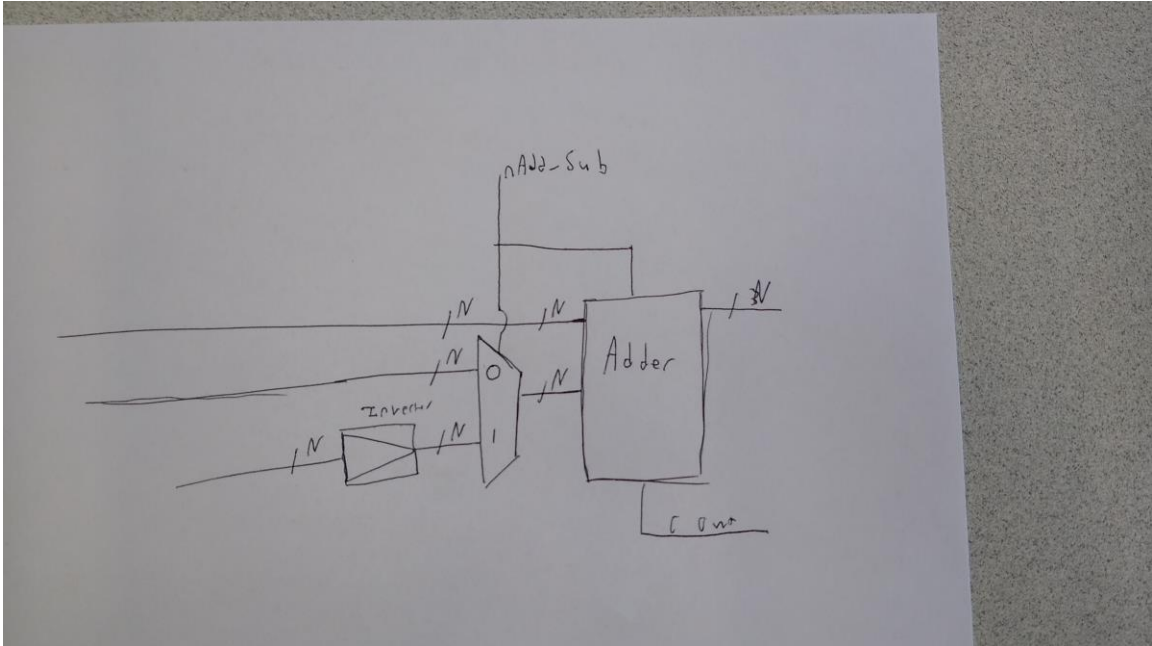
A	B	Cin	Sum	C out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



f. [Part 3 (e)] Waveform.



g. [Part 4 (a)] Draw a schematic (don't use a schematic capture tool) showing how an N-bit adder/subtractor with control can be implemented using only the three main components



designed in problems 1), 2), and 3) (the N-bit inverter, N-bit 2:1 mux, and N-bit adder). How is the 'nAdd_Sub' bit used?

That bit is used to control both the multiplexer and as the carry bit to the adder

- h. [Part 4 (c)] Provide multiple waveform screenshots in your write-up to confirm that this component is working correctly. What test-cases did you include and why?

Here I did basic adding and subtracting to make sure that the core functions of my block

+	/fulladdsub/ina	32'h00000006	00000006		
+	/fulladdsub/inb	32'h00000002	00000002		
	/fulladdsub/nAdd_Sub	1			
+	/fulladdsub/outp	32'h00000004	00000008	00000004	
worked.	/fulladdsub/carry_out	1			

FFFFFFFF		
00000001		
00000000		

Here I added one to FFFFFFFF to make sure that the carry works

Here I subtracted 8 from 6 to ensure that I do get a negative

00000006		
00000008		
0000000E	FFFFFFFE	

number

- i. [Feedback] You must complete this section for your lab to be graded. Write down the first response you think of; I expect it to take roughly 5 minutes (do not take more than 10 minutes).

- i. How many hours did you spend on this lab?

Task	During lab time	Outside of lab time
Reading lab	0	0
Pencil/paper design	.5	.5
VHDL design	1	2
Assembly coding	.5	2
Simulation	0	1
Debugging	0	.5
Report writing	0	0
Other:	0	0
Total	2	5

- ii. If you could change one thing about the lab experience, what would it be? Why?
- I get why we made everything from scratch however everyone I talked to got to around the 2:1 MUX in their lab time, so the two times the document mentioned talking to a TA for details we were unable to due to being outside of a lab section / we would have had to allocate even more time to finding a TA and talking to them
- iii. What was the most interesting part of the lab?
- I actually enjoyed seeing just how much easier dataflow is verse structural coding.