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Digital Chip Back-end Design Based on Script Mode

Lida Xu

Institute of Computing Technology, Chinese Academy of Sciences

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Preparation for tape-out

- Modify the RTL code in accordance with the **tape-out preparation document** and conduct tests and submissions (It will be provided separately later)
- The following steps such as using iverilog for netlist simulation will also be introduced in the tape-out preparation document
- The following 2 timing analysis, and 3 Place & Route operations are designed to help understand the process of digital back-end design and are not mandatory operations for tape-out, but the **1 logical synthesis is necessary**

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Modify the RTL

- ysyx_2025 is a RISC-V 32 processor, modifying the top-level port of the CPU designed by yourself to keep it consistent

```
2   module ysyx_2025(
3       input clock,
4       input reset,
5
6       output io_ifu_reqValid,
7       output [31:0]io_ifu_addr,
8       input io_ifu_respValid,
9       input [31:0]io_ifu_rdata,
10      output io_lsu_reqValid,
11      output [31:0]io_lsu_addr,
12      output [1:0]io_lsu_size,
13      output io_lsu_wen,
14      output [31:0]io_lsu_wdata,
15      output [3:0]io_lsu_wmask,
16      input io_lsu_respValid,
17      input [31:0]io_lsu_rdata
18  );
```

Modify the RTL

- Remove DPIC-related content from the RTL code

```
import "DPI-C" function void ebreak(input bit is_ebreak);
```

Modify the RTL

- Do not use latches，Check if the RTL code is
  - Complete conditional assignment

```
always @(posedge clk) begin
    if (enable)
        q = data;
    else
        q = 1'b0;
end
```

Modify the RTL

- Do not use latches，Check if the RTL code is
  - Complete case statement

```
always @(posedge clk) begin
   case(sel)
      2'b00: y = a;
      2'b01: y = b;
      2'b10: y = c;
      2'b11: y = d;
      default: y = 1'b0;
   endcase
end
```

Project Download

- Synthesize the RTL code using the open-source RTL synthesizer Yosys, and map the synthesis results to a 55nm open-source PDK ICsprout55

```
git clone https://github.com/OSCPU/yosys-sta.git
```

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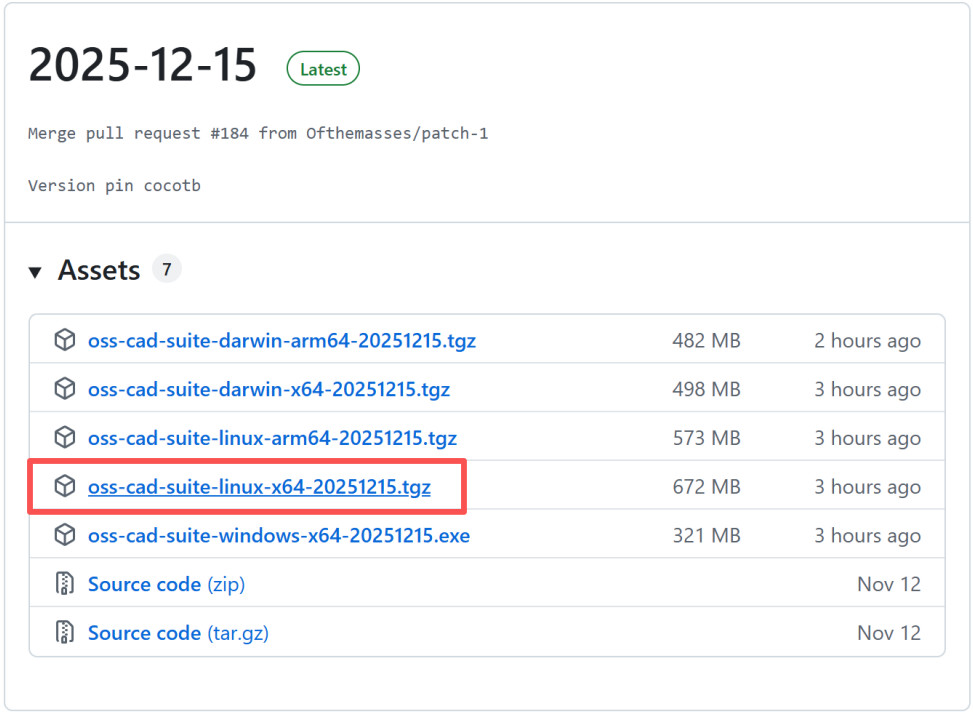
Install dependencies

- To install Yosys, it is recommended to download the corresponding package from https://github.com/YosysHQ/oss-cad-suite-build/releases



Install dependencies

- File uncompress

```
tar -xzvf oss-cad-suite-linux-x64-20251215.tgz
```

Install dependencies

- After uncompressing, add `path-to-oss-cad-suite/bin` to the environment variable `PATH` to call yosys from the toolkit

```
export PATH="/home/xxx/yosys/oss-cad-suite/bin:$PATH
```

- Install other dependencies and download components

```
apt install libunwind-dev liblzma-dev # iEDA's dependency libraries
# or
yum install libunwind liblzma
make init # Download the iEDA and icsprout55 process libraries
```

Install dependencies

- After completion, test whether iEDA can run

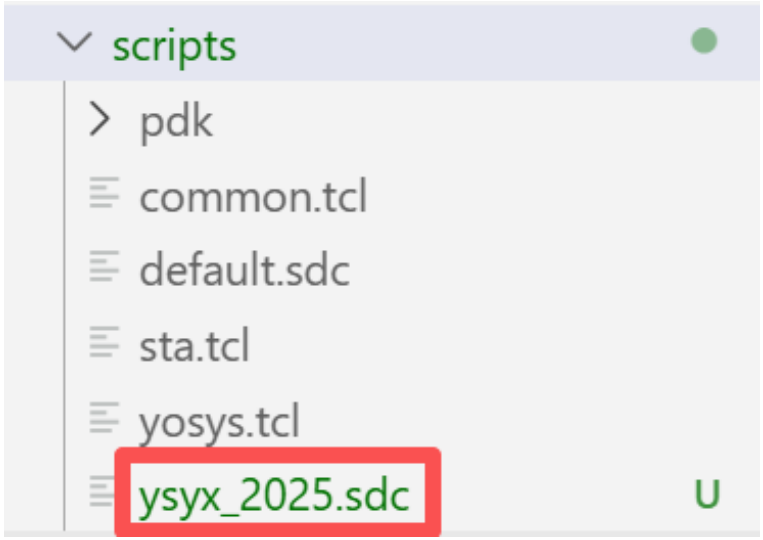
```
echo exit | ./bin/iEDA -v  # If it runs successfully, the terminal
will display the version number of iEDA.
```

Design Practice

- Add the RTL designs that need to be synthesied under the example directory, such as ysyx_2025.v

Design Practice

- Add the sdc constraint file in the scripts directory, such as ysyx_2025.sdc. The clock port name in the sdc file need to match the name in the design file



Design Practice

- Modify DESIGN, SDC_FILE, RTL_FILE, CLK_FREQ_MHZ, and CLK_PORT_NAME in the Makefile

Makefile

```
1   PROJ_PATH = $(shell pwd)
2   SHELL := /bin/bash
3
4   O ?= $(PROJ_PATH)/result
5   DESIGN ?= ysyx_2025
6   SDC_FILE ?= $(PROJ_PATH)/scripts/ysyx_2025.sdc
7   RTL_FILES ?= $(shell find $(PROJ_PATH)/example -name "ysyx_2025.v")
8   export CLK_FREQ_MHZ ?= 100
9   export CLK_PORT_NAME ?= clock
10  PDK = icsprout55
```

Design Practice

- In the /yosys-sta/ directory, execute the following commands in sequence to perform synthesis

```
make init # Required the first time it is executed
make syn
```

Design Practice

- Generate the synthesized report in the result/ysyx_2025-100MHz/ directory. Some file descriptions are as follows

```
* ` ysyx_2025.netlist.v` - Netlist file synthesized by Yosys
* ` ysyx_2025.netlist.v.sim` - Used for netlist simulation
* `synth_stat.txt` - Area report of Yosys synthesis
* `synth_check.txt` - Yosys synthesis check report
* `yosys.log` - Yosys synthesis log
```

Design Practice

- Shows a comparison between the ysyx_2025.netlist.v netlist and the ysyx_2025.netlist.v.sim netlist used for simulation

result > ysyx_2025-100MHz > ysyx_2025.netlist.v

```
1  /* Generated by Yosys 0.59+117 (git sha1 33a49452d, clang++ 1
2
3  module ysyx_2025(clock, reset, io_ifu_reqValid, io_ifu_addr_0
4  , io_ifu_addr_18_, io_ifu_addr_19_, io_ifu_addr_20_, io_ifu_a
5  , io_ifu_rdata_6_, io_ifu_rdata_7_, io_ifu_rdata_8_, io_ifu_r
6  , io_ifu_rdata_27_, io_ifu_rdata_28_, io_ifu_rdata_29_, io_if
7  , io_lsu_addr_15_, io_lsu_addr_16_, io_lsu_addr_17_, io_lsu_a
8  , io_lsu_wdata_1_, io_lsu_wdata_2_, io_lsu_wdata_3_, io_lsu_w
9  , io_lsu_wdata_22_, io_lsu_wdata_23_, io_lsu_wdata_24_, io_ls
10 , io_lsu_rdata_6_, io_lsu_rdata_7_, io_lsu_rdata_8_, io_lsu_r
11 , io_lsu_rdata_27_, io_lsu_rdata_28_, io_lsu_rdata_29_, io_ls
12   input clock;
13   wire clock;
14   input reset;
15   wire reset;
16   output io_ifu_reqValid;
17   wire io_ifu_reqValid;
18   output io_ifu_addr_0_;
19   wire io_ifu_addr_0_;
20   output io_ifu_addr_1_;
21   wire io_ifu_addr_1_;
22   output io_ifu_addr_2_;
23   wire io_ifu_addr_2_;
24   output io_ifu_addr_3_;
25   wire io_ifu_addr_3_;
26   output io_ifu_addr_4_;
27   wire io_ifu_addr_4_;
28   output io_ifu_addr_5_;
29   wire io_ifu_addr_5_;
30   output io_ifu_addr_6_;
31   wire io_ifu_addr_6_;
32   output io_ifu_addr_7_;
```

result > ysyx_2025-100MHz > ysyx_2025.netlist.v.sim

```
1  /* Generated by Yosys 0.59+117 (git sha1 33a49452d, clang++ 1
2
3  module ysyx_2025(clock, reset, io_ifu_reqValid, io_ifu_addr,
4    input clock;
5    wire clock;
6    input reset;
7    wire reset;
8    output io_ifu_reqValid;
9    wire io_ifu_reqValid;
10   output [31:0] io_ifu_addr;
11   wire [31:0] io_ifu_addr;
12   input io_ifu_respValid;
13   wire io_ifu_respValid;
14   input [31:0] io_ifu_rdata;
15   wire [31:0] io_ifu_rdata;
16   output io_lsu_reqValid;
17   wire io_lsu_reqValid;
18   output [31:0] io_lsu_addr;
19   wire [31:0] io_lsu_addr;
20   output [1:0] io_lsu_size;
21   wire [1:0] io_lsu_size;
22   output io_lsu_wen;
23   wire io_lsu_wen;
24   output [31:0] io_lsu_wdata;
25   wire [31:0] io_lsu_wdata;
26   output [3:0] io_lsu_wmask;
27   wire [3:0] io_lsu_wmask;
28   input io_lsu_respValid;
29   wire io_lsu_respValid;
30   input [31:0] io_lsu_rdata;
31   wire [31:0] io_lsu_rdata;
32   wire \io_ifu_addr[0]_reg_p_CK ;
```

Design Practice

- The area report after synthesis, showing the number of cells used and the area of each type of cell

result > ysyx_2025-100MHz > synth_stat.txt

```
4    === ysyx_2025 ===
15         6362 1.58E+04 cells
224         296    414.4   OAI21X0P5H7L
277          77    215.6   XNOR2X0P5H7L
279           4     11.2   XNOR2X1H7L
280          12     33.6   XNOR2X1P4H7L
281           2     6.72   XNOR2X3H7L
282           1     3.64   XNOR2X4H7L
283          60      168   XOR2X0P5H7L
284           2      5.6   XOR2X0P7H7L
285           1      2.8   XOR2X1H7L
286          10       28   XOR2X1P4H7L
287           4    13.44   XOR2X3H7L
288
289      Chip area for module '\ysyx_2025': 15839.320000
290        of which used for sequential elements: 5796.560000 (36.60%)
```

TASK1

- Synthesize the processor's RTL code and check the synthesized processor area.

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CONTENTS

Design Practice

- In the /yosys-sta/ directory, execute the following commands to perform static timing analysis

```
make sta
```

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Design Practice

- Generate the timing analysis report in the result/ysyx_2025-100MHz/ directory. Some of the files are described as follows

```
* `ysyx_2025.rpt` - iSTA Timing Analysis Report
* `ysyx_2025.cap` - iSTA Capacitance Violation Report
* `ysyx_2025.fanout` - iSTA Fanout Violation Report
* `ysyx_2025.trans` - iSTA Transition Time Violation Report
* `ysyx_2025_hold.skew` - iSTA Clock Skew Report in Hold Mode
* `ysyx_2025_setup.skew` - iSTA Clock Skew Report in Setup Mode
* `ysyx_2025.pwr` - STA Overall Power Report
* `ysyx_2025_instance.pwr` - iSTA Standard Cell Level Power Report
* `ysyx_2025_instance.csv` - CSV Format
* `sta.log` - iSTA Log
```

Design Practice

- Timing report. From the report, it can be seen that the timing margins (Slack) for all paths are positive

result > ysyx_2025-100MHz > ysyx_2025.rpt

Generate the report at 2025-12-17T15:47:19, GitVersion: aa25008b3778a76ae1975c839d4cc459f7f7b3b7.

Endpoint	Clock Group	Delay Type	Path Delay	Path Required	CPPR	Slack	Freq(MHz)
ysyx_2025_gpr.rf[8]_18__reg_p:D	core_clock	max	1.772f	9.951	0.000	8.179	549.245
ysyx_2025_gpr.rf[4]_18__reg_p:D	core_clock	max	1.772f	9.954	0.000	8.183	550.210
ysyx_2025_gpr.rf[12]_18__reg_p:D	core_clock	max	1.772f	9.954	0.000	8.183	550.210
ysyx_2025_gpr.rf[7]_18__reg_p:D	core_clock	max	1.772f	9.954	0.000	8.183	550.210
ysyx_2025_gpr.rf[15]_18__reg_p:D	core_clock	max	1.772f	9.954	0.000	8.183	550.210
mtvec_0__reg_p_CK_ICGX0P5H7L_ECK:E	**clock_gating_default**	max	1.347r	9.946	0.000	8.599	NA
ysyx_2025_my_csr.csr[4]_0__reg_p_CK_ICGX0P5H7L_ECK:E	**clock_gating_default**	max	1.325r	9.946	0.000	8.621	NA
ysyx_2025_my_csr.csr[1]_0__reg_p_CK_ICGX0P5H7L_ECK:E	**clock_gating_default**	max	1.294f	9.963	0.000	8.669	NA
ysyx_2025_my_csr.csr[4]_0__reg_p_CK_ICGX0P5H7L_ECK:E	**clock_gating_default**	max	1.290f	9.959	0.000	8.669	NA
mtvec_0__reg_p_CK_ICGX0P5H7L_ECK:E	**clock_gating_default**	max	1.293f	9.963	0.000	8.670	NA
ysyx_2025_my_lsu.en_flash_1__reg_p:D	core_clock	min	0.064f	-0.008	0.000	0.072	NA
io_ifu_reqValid_reg_p:D	core_clock	min	0.081r	-0.018	0.000	0.099	NA
ysyx_2025_my_lsu.is_been_alloc_reg_p:D	core_clock	min	0.091f	-0.009	0.000	0.100	NA
ysyx_2025_my_lsu.is_been_alloc_reg_p:D	core_clock	min	0.084r	-0.018	0.000	0.102	NA
ysyx_2025_my_lsu.en_flash_1__reg_p:D	core_clock	min	0.085r	-0.018	0.000	0.103	NA
io_lsu_reqValid_ICGX0P5H7L_E:E	**clock_gating_default**	min	0.059f	-0.006	0.000	0.065	NA
io_lsu_reqValid_ICGX0P5H7L_E:E	**clock_gating_default**	min	0.080r	-0.012	0.000	0.092	NA
io_ifu_respValid_AND2X1H7L_B_Y_ICGX0P5H7L_E:E	**clock_gating_default**	min	0.099f	-0.002	0.000	0.101	NA
mcycle_31__AND4X0P5H7L_C_Y_ICGX0P5H7L_E:E	**clock_gating_default**	min	0.117f	-0.004	0.000	0.121	NA
pc_valid_ICGX0P5H7L_E:E	**clock_gating_default**	min	0.129f	-0.008	0.000	0.136	NA

Clock	Delay Type	TNS
core_clock	max	0.000
core_clock	min	0.000

Design Practice

- Shows a path timing analysis for the setup time Tsetup. Slack = Tr - Ta = 9.951 - 1.772 = 8.179 > 0, no timing violations

Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Incr	Path
clock (port)		0.097	0.000	0.000		0.000	0.000r
clock (clock net)	72				NA		
ysyx_2025_my_ifu.curr_state_1__reg_p:CK (DFFQX1H7L)		0.001	0.000	0.000		0.000	0.000r
clock core_clock (rise edge)						0	0
clock network delay (ideal)						0.000	0.000
ysyx_2025_my_ifu.curr_state_1__reg_p:CK (DFFQX1H7L)		0.001	0.000	0.000		0.000	0.000r
ysyx_2025_my_ifu.curr_state_1__reg_p:Q (DFFQX1H7L)		0.002	0.000	0.032		0.089	0.089r
ysyx_2025_my_ifu.curr_state_1_ (net)	1				0.000		
ysyx_2025_my_ifu.curr_state_1__BUFX8H7L_A:A (BUFX8H7L)		0.002	0.000	0.032		0.000	0.089r
ysyx_2025_my_ifu.curr_state_1__BUFX8H7L_A:Y (BUFX8H7L)		0.022	0.000	0.056		0.054	0.144r
mepc_7__INVX0P5H7L_A_Y_MUX2X0P5H7L_A_B_AOI21X0P5H7L_Y_A0_NOR2BX1P4H7L_Z_AN (net)	10				0.000		
.....							
ysyx_2025_gpr.rf[8]_18__reg_p_D_NOR2BX8H7L_Z:AN (NOR2BX8H7L)		0.002	0.000	0.029		0.000	1.738f
ysyx_2025_gpr.rf[8]_18__reg_p_D_NOR2BX8H7L_Z:Z (NOR2BX8H7L)		0.001	0.000	0.046		0.034	1.772f
ysyx_2025_gpr.rf[8]_18__reg_p_D (net)	1				0.000		
ysyx_2025_gpr.rf[8]_18__reg_p:D (DFFQX1H7L)		0.001	0.000	0.046		0.000	1.772f
clock (port)		0.072	0.000	0.000		0.000	0.000r
clock (clock net)	72				NA		
ysyx_2025_gpr.rf[8]_0__reg_p_CK_ICGX0P5H7L_ECK:CK (ICGX0P5H7L)		0.002	0.000	0.000		0.000	0.000r
ysyx_2025_gpr.rf[8]_0__reg_p_CK_ICGX0P5H7L_ECK:ECK (ICGX0P5H7L)		0.025	0.000	0.000		0.000	0.000r
ysyx_2025_gpr.rf[8]_0__reg_p_CK (clock net)	32				NA		
ysyx_2025_gpr.rf[8]_18__reg_p:CK (DFFQX1H7L)		0.001	0.000	0.000		0.000	0.000r
clock core_clock (rise edge)						10	10
clock network delay (ideal)						0.000	10.000
ysyx_2025_gpr.rf[8]_18__reg_p:CK (DFFQX1H7L)							10.000r
library setup time						-0.049	9.951
clock reconvergence pessimism						0.000	9.951
path cell delay							1.772(100.000%)
path net delay							0.000(0.000%)
data require time							9.951
data arrival time							1.772
slack (MET)							8.179

Design Practice

- Timing analysis path with hold time Thold. The slack = Ta - Tr = 0.064 - (-0.008) = 0.072 > 0, indicating no timing violations

Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Incr	Path
clock (port)		0.072	0.000	0.000		0.000	0.000r
clock (clock net)	72				NA		
ysyx_2025_my_lsu.en_flash_0__reg_p:CK (DFFQX1H7L)		0.001	0.000	0.000		0.000	0.000r
clock core_clock (rise edge)						0	0
clock network delay (ideal)						0.000	0.000
ysyx_2025_my_lsu.en_flash_0__reg_p:CK (DFFQX1H7L)		0.001	0.000	0.000		0.000	0.000r
ysyx_2025_my_lsu.en_flash_0__reg_p:Q (DFFQX1H7L)		0.001	0.000	0.027		0.064	0.064f
ysyx_2025_my_lsu.en_flash_0_ (net)	2				0.000		
ysyx_2025_my_lsu.en_flash_1__reg_p:D (DFFQX1H7L)		0.001	0.000	0.027		0.000	0.064f
clock (port)		0.097	0.000	0.000		0.000	0.000r
clock (clock net)	72				NA		
ysyx_2025_my_lsu.en_flash_1__reg_p:CK (DFFQX1H7L)		0.001	0.000	0.000		0.000	0.000r
clock core_clock (rise edge)						0	0
clock network delay (ideal)						0.000	0.000
ysyx_2025_my_lsu.en_flash_1__reg_p:CK (DFFQX1H7L)							0.000r
library hold time						-0.008	-0.008
clock reconvergence pessimism						-0.000	-0.008
path cell delay							0.064(100.000%)
path net delay							0.000(0.000%)
data require time							-0.008
data arrival time							0.064
slack (MET)							0.072

Design Practice

- Power analysis report. The sequential logic power consumption: 7.726e-04 W. The combinational logic power consumption: 1.012e+01 W. The static power consumption: 1.282e-05 W, and the dynamic power consumption: 1.012e+01 W

result > ysyx_2025-100MHz > ysyx_2025.pwr

```
Generate the report at 2025-12-17T15:47:24
Report : Averaged Power
 +---------------+---------------+--------------+---------------+-------------+-----------+
| Power Group    | Internal Power | Switch Power | Leakage Power | Total Power | (%)       |
+---------------+---------------+--------------+---------------+-------------+-----------+
| combinational | 1.012e+01      | 0.000e+00    | 6.536e-06     | 1.012e+01   | (99.992%) |
| sequential    | 7.663e-04      | 0.000e+00    | 6.286e-06     | 7.726e-04   | (0.008%)  |
+---------------+---------------+--------------+---------------+-------------+-----------+
Net Switch Power   ==    0.000e+00 (0.000%)
Cell Internal Power   ==    1.012e+01 (100.000%)
Cell Leakage Power   ==    1.282e-05 (0.000%)
Total Power   ==  1.012e+01 W
```

TASK2

- Execute STA to check the processor's highest frequency, static power consumption, and dynamic power consumption

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Project Download

- Chip place and route design using iEDA tools

```
git clone --recursive https://github.com/OSCC-Project/iEDA.git iEDA && cd iEDA
```

Project Download

- Installing build dependencies via apt requires root privileges

```
sudo bash build.sh -i apt
```

- Compiling iEDA

```
bash build.sh
```

- If "Hello iEDA!" is output, then the compilation is successful

```
./bin/iEDA -script scripts/hello.tcl
```

Design Practice

- Copy the generated Netlist file to the iEDA/scripts/design/ics55_gcd/result/ verilog directory

Design Practice

- Enter the /iEDA/scripts/foundry/ directory and download the ICsprout55 PDK

```
git clone https://github.com/openecos-projects/icsprout55-pdk.git
cd icsprout55-pdk
make unzip
```

Design Practice

ICsprout55nm open source PDK directory

```
├── IP
│   ├── IO
│   │   └── ICsprout_55LLULP1233_IO_251013   # Specific IO library
│   │       ├── cdl       # Transistor-level circuit netlist
│   │       ├── cell_list # Cell list
│   │       ├── lef       # Layout Exchange Format
│   │       ├── liberty    # Timing and power consumption libraries
│   │       └── verilog    # Functional simulation model
│   └── STD_cell                            # Standard cell library
│       └── ics55_LLSC_H7C_V1p10C100        # 55nm LLSC H7C
standard cell library version 1.10
│           ├── ics55_LLSC_H7CH             # HVT standard cells
│           │   ├── cdl
│           │   ├── cell_list
│           │   ├── doc
│           │   ├── lef
│           │   ├── liberty
│           │   └── verilog
└── prtech                                  # Place & Route
technology files
    └── techLEF  # 技术 LEF 文件
```

Design Practice

- Modify the TOP_NAME, CLK_PORT_NAME, PDK_DIR, and default.sdc files in /iEDA/scripts/design/ics55_gcd/run_iEDA.sh

scripts > design > ics55_gcd > $ run_iEDA.sh

```
1  #!/bin/bash
2  set -e
3
4  TOP_NAME="ysyx_2025"
5  CLK_PORT_NAME="clock"
6  PDK_DIR=/home/xulida05/iEDA/scripts/foundry/icsprout55-pdk
7  export USE_FIXED_BBOX=False
```

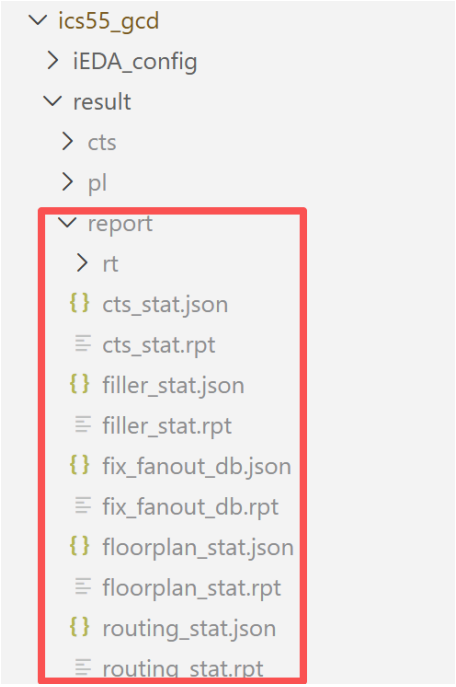
Design Practice

- Execute the following command in the /iEDA/scripts/design/ics55_gcd/ directory to perform place and route

```
./run_iEDA.sh
```

Design Practice

- Generate the backend design report in the /iEDA/scripts/design/ics55_gcd/result/ report directory



Design Practice

- Taking routing_stat.rpt as an example, which is a report after routing, you can see the area and utilization rate of DIE and CORE

Summary

Module	Value
DIE Area (um^2)	90853.413561 = 301.419000 * 301.419000
DIE Usage	0.180577
CORE Area (um^2)	79185.960000 = 281.400000 * 281.400000
CORE Usage	0.207183

Design Practice

- And routing resource information

Number - Site	3
Number - Row	201
Number - Track	14
Number - Layer	20
Number - Routing Layer	7
Number - Cut Layer	7
Number - GCell Grid	6
Number - Cell Master	1570
Number - Via Rule	48

Design Practice

Physical realization information

Number - IO Pin	177
Number - Instance	9163
Number - Blockage	0
Number - Filler	0
Number - Net	6829
Number - Special Net	4

Design Practice

Number and area of instances used

Summary - Instance

Type	Number	Number Ratio	Area	Area Ratio
All Instances	9163	1	17751.7	1
Netlist	6761	0.737859	16406.6	0.924226
Physical	2402	0.262141	1345.12	0.0757741
Timing	0	0	0	0
Core	9163	1	17751.7	1
Core - logic	6761	0.737859	16406.6	0.924226
Pad	0	0	0	0
Block	0	0	0	0
Endcap	0	0	0	0
Cover	0	0	0	0
Ring	0	0	0	0

Design Practice

Net usage

Summary - Net

Net Type	Number	Number Ratio	Length	Length Ratio
All Nets	6829	1	198764113	1
Signal	6824	0.999268	197815353	0.995227
Clock	5	0.000732172	948760	0.0047733
Power & Ground	0	0	0	0

Design Practice

Layer related information

Summary - Layer

Layer	Net - Wire Length	Net - Wire Length Ratio	Net - Wire Number	Net - Via Number	Net - Patch Number
OVERLAP	0	0	0	0	0
ACT	0	0	0	0	0
NP	0	0	0	0	0
PP	0	0	0	0	0
NW1	0	0	0	0	0
POLY	0	0	0	0	0
CT	0	0	0	0	0
MET1	0	0	0	0	0
VIA1	0	0	0	0	0
MET2	45950736	0.231182	38325	0	174
VIA2	0	0	0	27059	0
MET3	59464094	0.299169	27264	0	2467
VIA3	0	0	0	12698	0
MET4	54016345	0.271761	10770	0	1324
VIA4	0	0	0	5234	0
MET5	39332938	0.197888	4868	0	4
T4V2	0	0	0	0	0
T4M2	0	0	0	0	0
RV	0	0	0	0	0
RDL	0	0	0	0	0

TASK3

- Design the processor back-end layout using iEDA

Thanks!