Overview of the Back-End Design of Digital Chips

Lida Xu

Institute of Computing Technology, Chinese Academy of Sciences

2025.12.27

CONTENTS

1. Overview of the Back-end

2. Logical synthesis

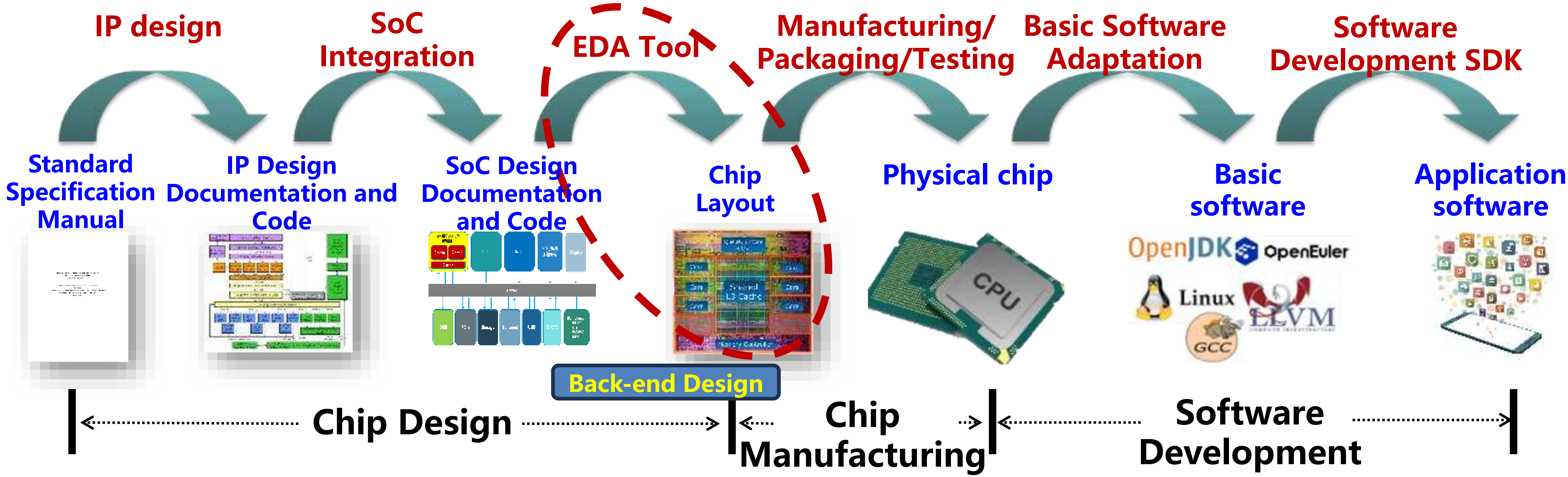
3. Timing analysis

4. Place & Route

5. Physical verification

1. Overview of the Back-end

- **Digital chip design**： Translating functional requirements into manufacturable silicon chip circuits
  - Front-end design: Design and verification of RTL
  - Back-end design: From RTL (Netlist) to the generation of GDS



IP design

SoC Integration

EDA Tool

Manufacturing/ Packaging/Testing

Basic Software Adaptation

Software Development SDK

Standard Specification Manual

IP Design Documentation and Code

SoC Design Documentation and Code

Chip Layout

Physical chip

Basic software

Application software

Back-end Design

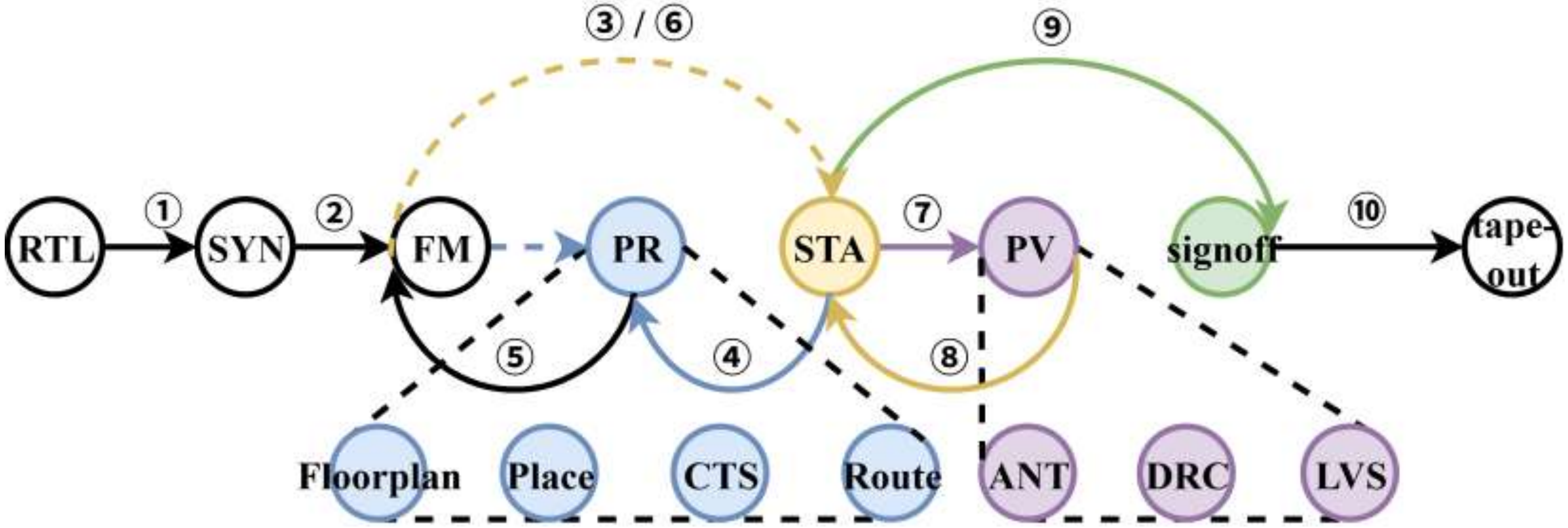
Chip Design

Chip Manufacturing

Software Development

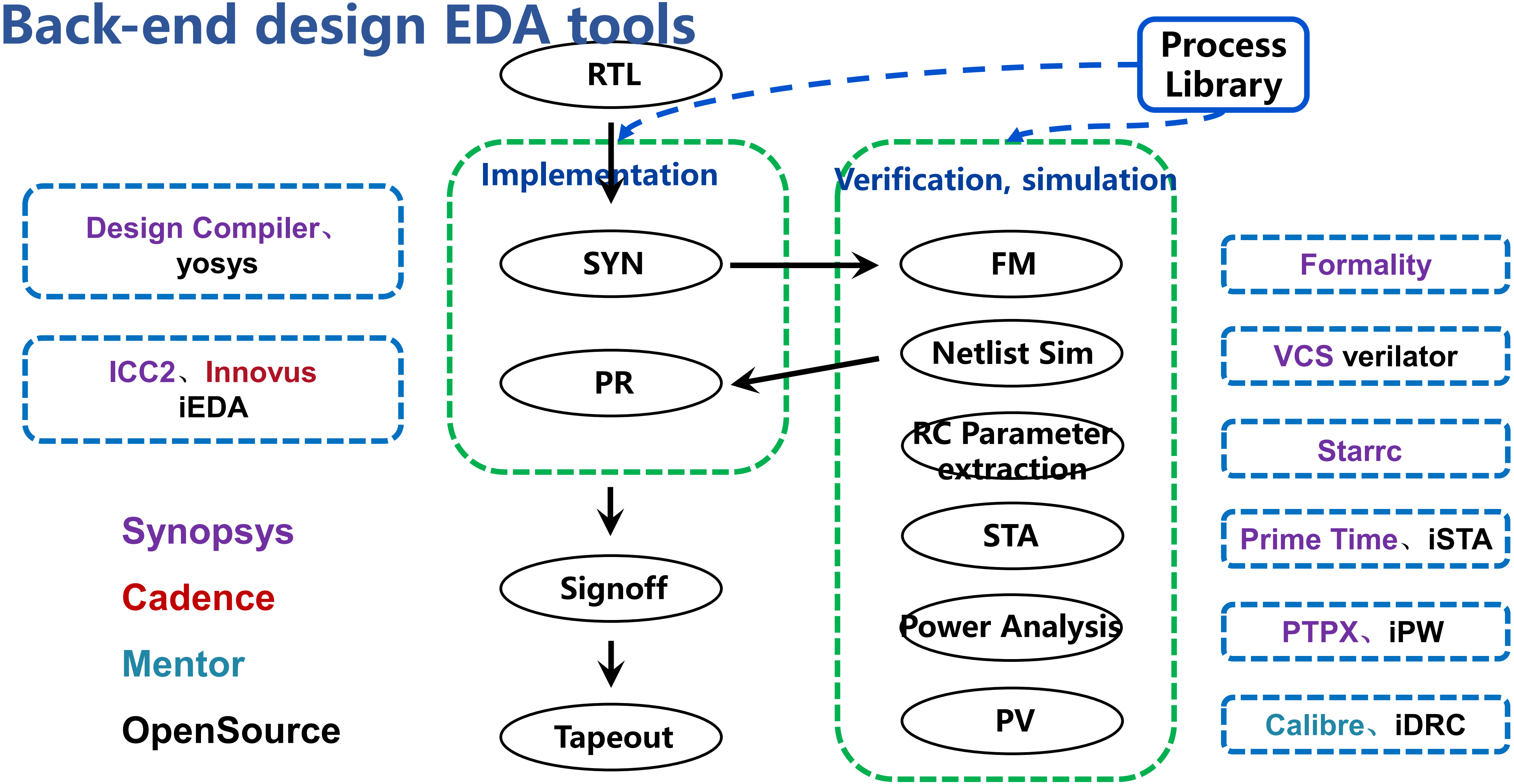
Back-end design process

- Logical synthesis (SYN)
- Place & Route (PR)
  - Floorplan
  - Place
  - CTS
  - Route
- Formal verification (FM)
- Physical verification (PV)
  - ERC
  - DRC
  - LVS
- Static timing analysis (STA)
- Signoff
- Tape out



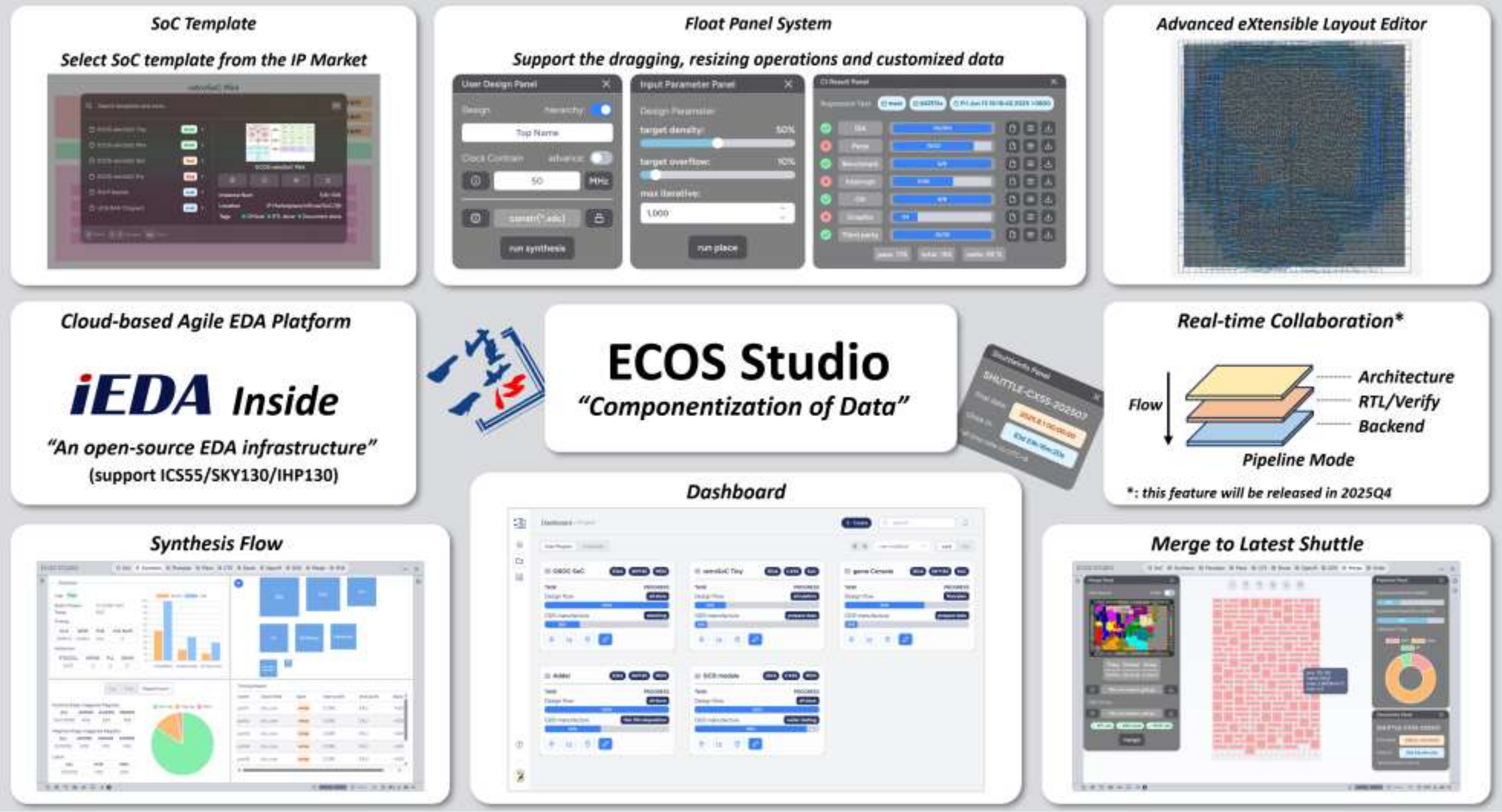
1. Overview of the Backend

Back-end design EDA tools



1. Overview of the Backend

■ ECOS (EDA、Chip、One-Student-One-Chip、System)



SoC Template

Select SoC template from the IP Market

Float Panel System

Support the dragging, resizing operations and customized data

Advanced eXtensible Layout Editor

Cloud-based Agile EDA Platform

iEDA Inside

"An open-source EDA infrastructure"

(support ICS55/SKY130/IHP130)

ECOS Studio

"Componentization of Data"

Real-time Collaboration*

Pipeline Mode

*: this feature will be released in 2025Q4

Dashboard

Synthesis Flow

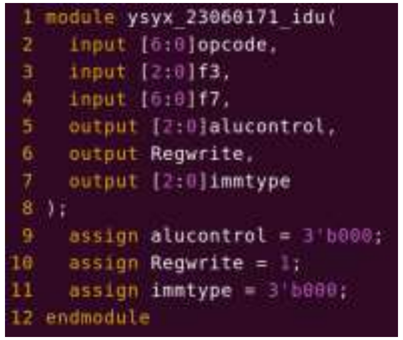
Merge to Latest Shuttle

1. Overview of the Backend

- **Supports one-stop RISC-V processor SoC chip design and tape-out using open-source EDA tools, open-source IP, and open-source PDK**

Submit Design

（Processor core/IP/…）

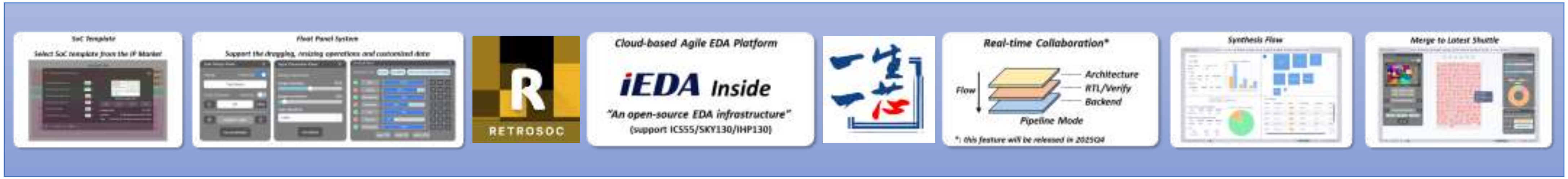


```
module ysyx_23060171_idu(
  input [6:0]opcode,
  input [2:0]f3,
  input [6:0]f7,
  output [2:0]alucontrol,
  output Regwrite,
  output [2:0]immtype
);
  assign alucontrol = 3'b000;
  assign Regwrite = 1;
  assign immtype = 3'b000;
endmodule
```

ECOS Studio

Home delivery

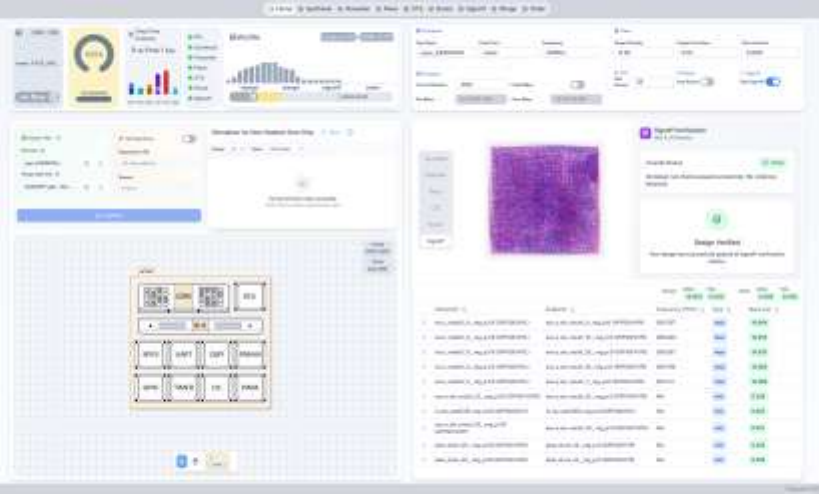
（Chip + Board）


SoC Template
Select SoC template from the IP Market
Float Panel System
Support the dragging, resizing operations and customized data
RETROSOC
Cloud-based Agile EDA Platform
iEDA Inside
"An open-source EDA infrastructure"
(support ICS55/SKY130/IHP130)
一生一芯
Real-time Collaboration*
Flow
Architecture
RTL/Verify
Backend
Pipeline Mode
*: this feature will be released in 2025Q4
Synthesis Flow
Merge to Latest Shuttle

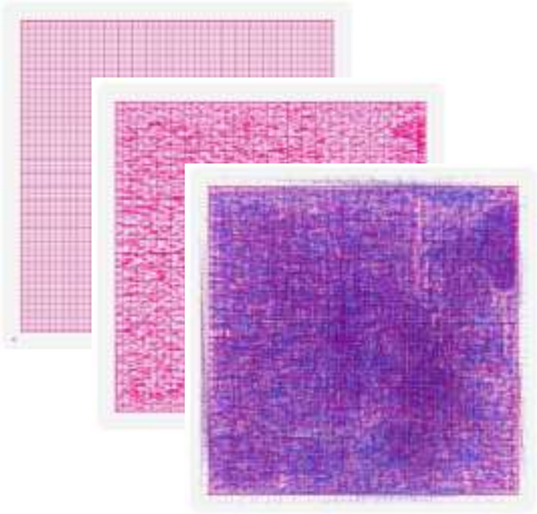
1. Overview of the Backend

中国科学院 CHINESE ACADEMY OF SCIENCES

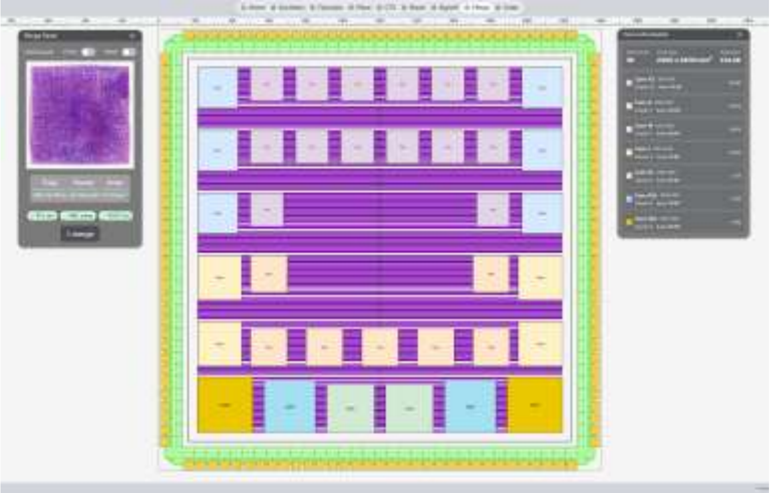
■ Supports end-to-end layout design of 100,000 instances of chips from RTL to GDSII on ICsprout 55nm process



Home interface



Layout render effect

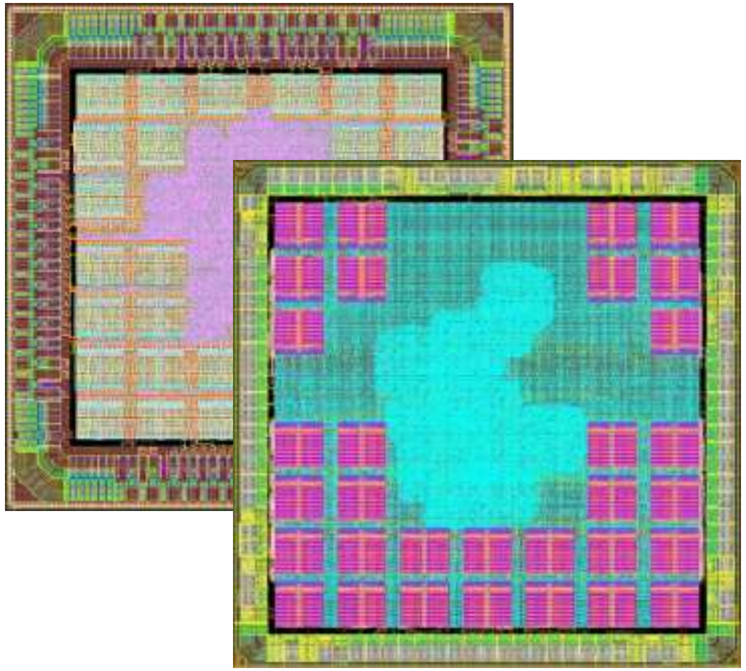


Merge interface

SoC Template
Select SoC template from the IP Market
Float Panel System
Support the dragging, resizing operations and customized data
R
RETROSOC
Cloud-based Agile EDA Platform
iEDA Inside
"An open-source EDA infrastructure"
(support ICS55/SKY130/IHP130)
一生一芯
Real-time Collaboration*
Flow
Architecture
RTL/Verify
Backend
Pipeline Mode
*: this feature will be released in 2025Q4
Synthesis Flow
Merge to Latest Shuttle

1. Overview of the Backend

- **Two chips designed based on ICsprout 55nm process have been fabricated and are running successfully**



Design: A RV32IMAC SoC(PSRAM, QSPI, UART, I2C, PWM, TIMER, RNG).
Size: 4mm^2(128KB OCM, no PLL)

Freq: 100MHz(external clock bypass)
Gates: 1.517M(73,009 cells) Power: 115.4mW(dynamic) 0.42mW(static)

中国科学院
CHINESE ACADEMY OF SCIENCES

CONTENTS

1. Overview of the Back-end

2. Logical synthesis

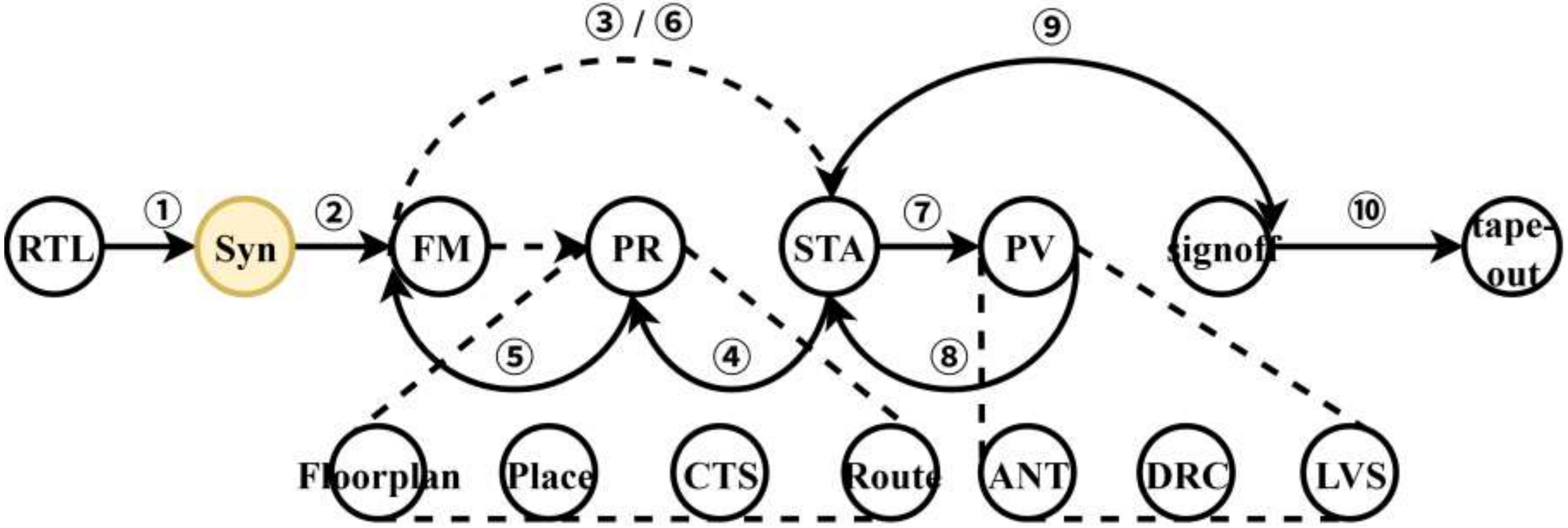
3. Timing analysis

4. Place & Route

5. Physical verification

Synthesis（Syn)

- Synthesis involves mapping the front-end RTL code to a specific process library, adding constraint information, and logically optimizing the RTL code to generate a gate-level netlist. It is the process from **RTL** to **Gate-Level Netlist**

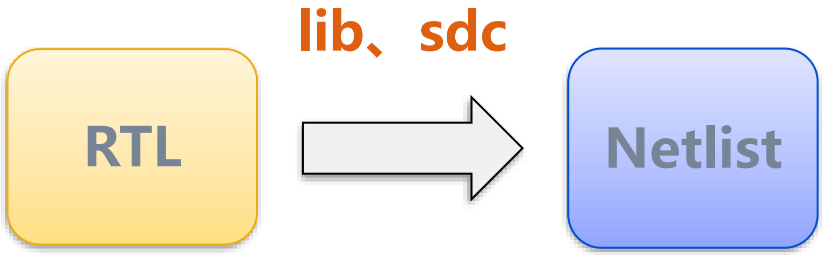


2. Synthesis

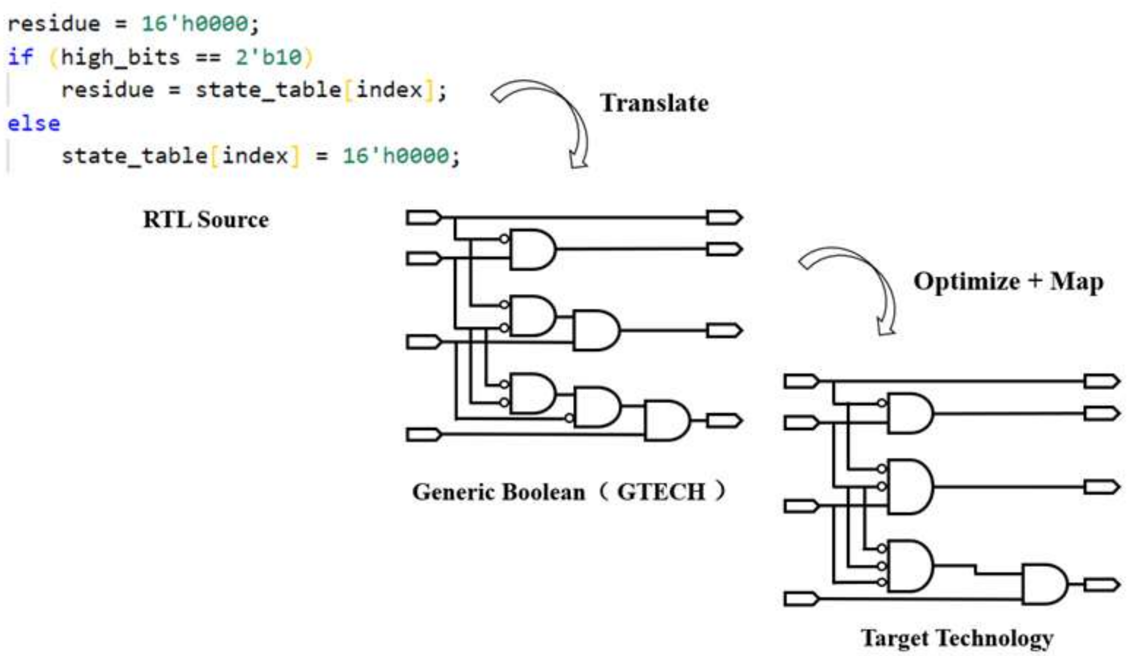
■ Synthesis： **RTL** to **Gate-level Netlist** generation

■ Input file:

- ■ RTL Code（Verilog、VHDL)
- ■ Library files（.lib/.db)
- ■ Constraint files （.sdc)



Synthesis = Translation + Optimization + Mapping



```
residue = 16'h0000;
if (high_bits == 2'b10)
    residue = state_table[index];
else
    state_table[index] = 16'h0000;
```

Translation

- **RTL translate to GTECH**

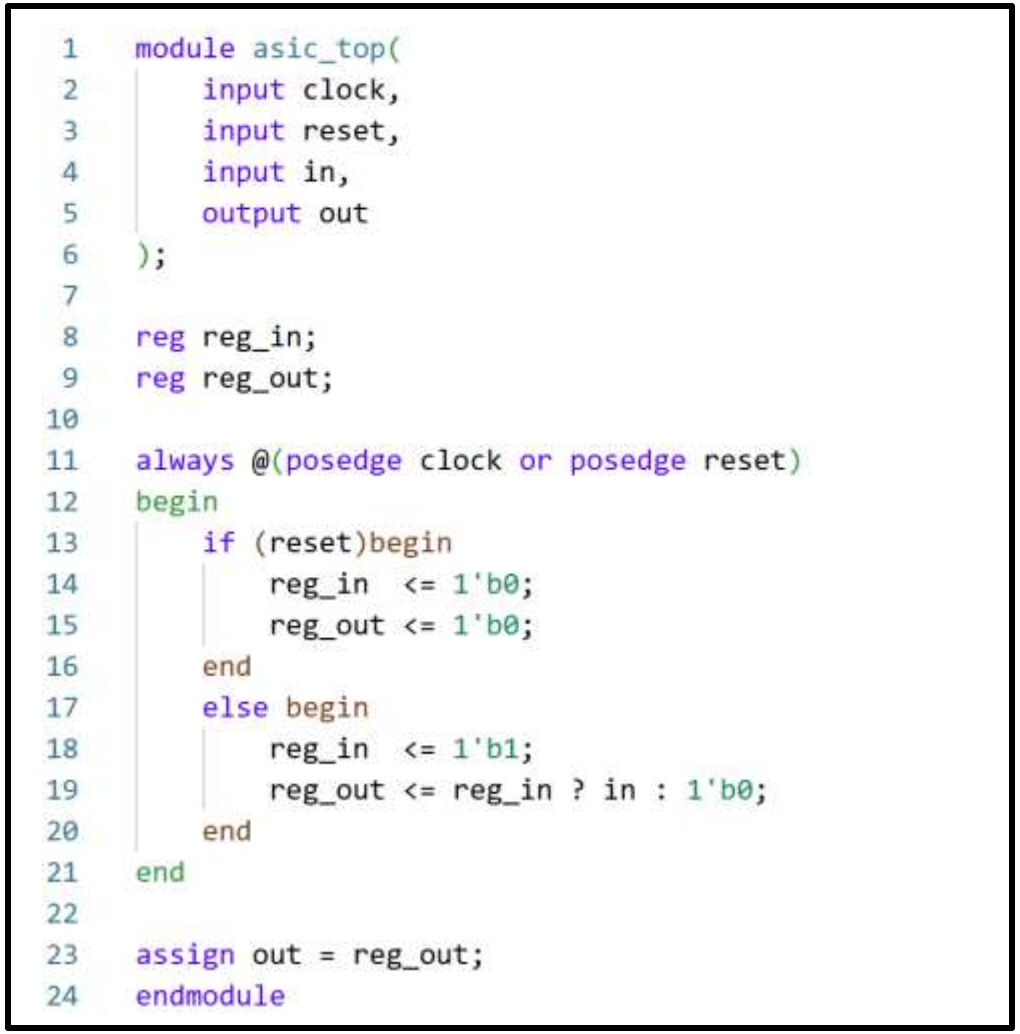
Optimization

- **Structural optimization**
- **Logic optimization**

Mapping

- **Optimized after mapping**

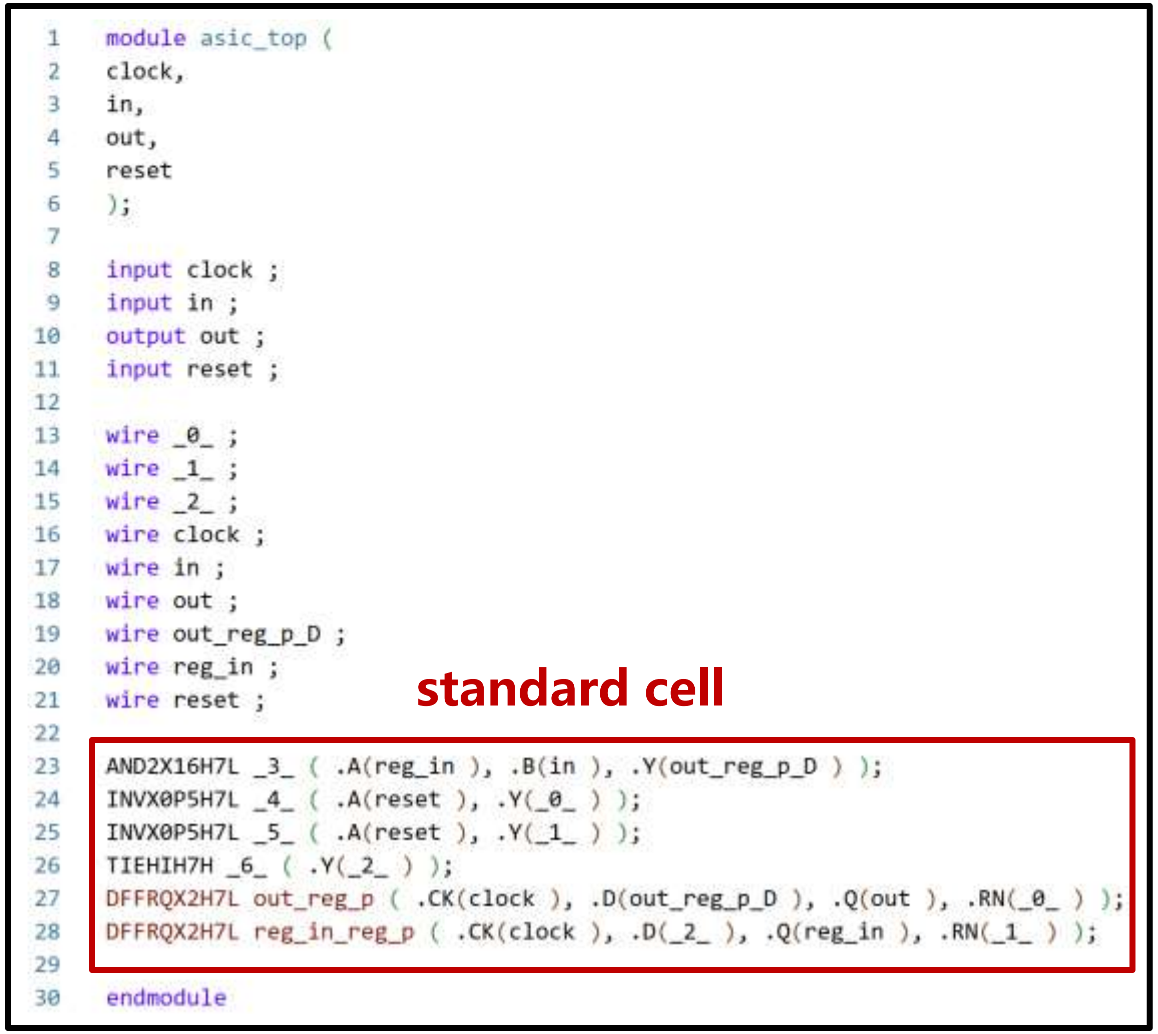
■ Comparison of the RTL and Netlist files



```
module asic_top(
    input clock,
    input reset,
    input in,
    output out
);

reg reg_in;
reg reg_out;

always @(posedge clock or posedge reset)
begin
    if (reset)begin
        reg_in  <= 1'b0;
        reg_out <= 1'b0;
    end
    else begin
        reg_in  <= 1'b1;
        reg_out <= reg_in ? in : 1'b0;
    end
end

assign out = reg_out;
endmodule
```

RTL

vs



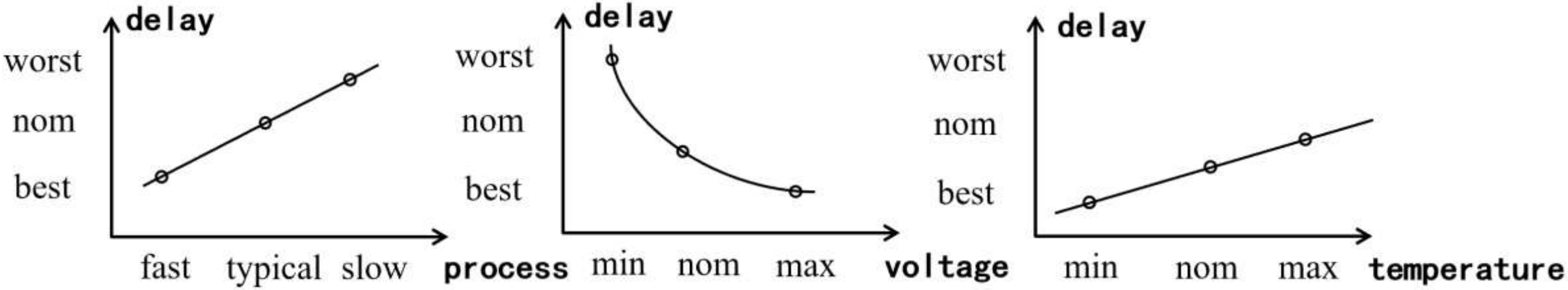
```
module asic_top (
clock,
in,
out,
reset
);

input clock ;
input in ;
output out ;
input reset ;

wire _0_ ;
wire _1_ ;
wire _2_ ;
wire clock ;
wire in ;
wire out ;
wire out_reg_p_D ;
wire reg_in ;
wire reset ;

AND2X16H7L _3_ ( .A(reg_in ), .B(in ), .Y(out_reg_p_D ) );
INVX0P5H7L _4_ ( .A(reset ), .Y(_0_ ) );
INVX0P5H7L _5_ ( .A(reset ), .Y(_1_ ) );
TIEHIH7H _6_ ( .Y(_2_ ) );
DFFRQX2H7L out_reg_p ( .CK(clock ), .D(out_reg_p_D ), .Q(out ), .RN(_0_ ) );
DFFRQX2H7L reg_in_reg_p ( .CK(clock ), .D(_2_ ), .Q(reg_in ), .RN(_1_ ) );

endmodule
```

standard cell

netlist

PVT (Process, Voltage,Temperature)

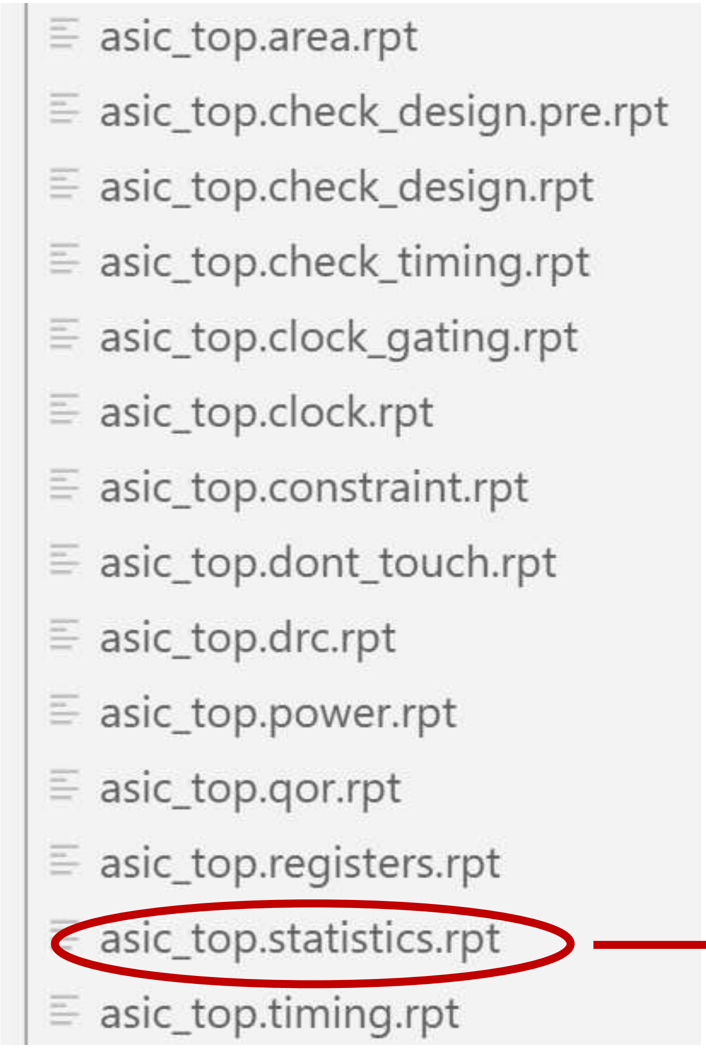
- The speed of the process Corner, voltage level and temperature level will all affect the timing analysis results



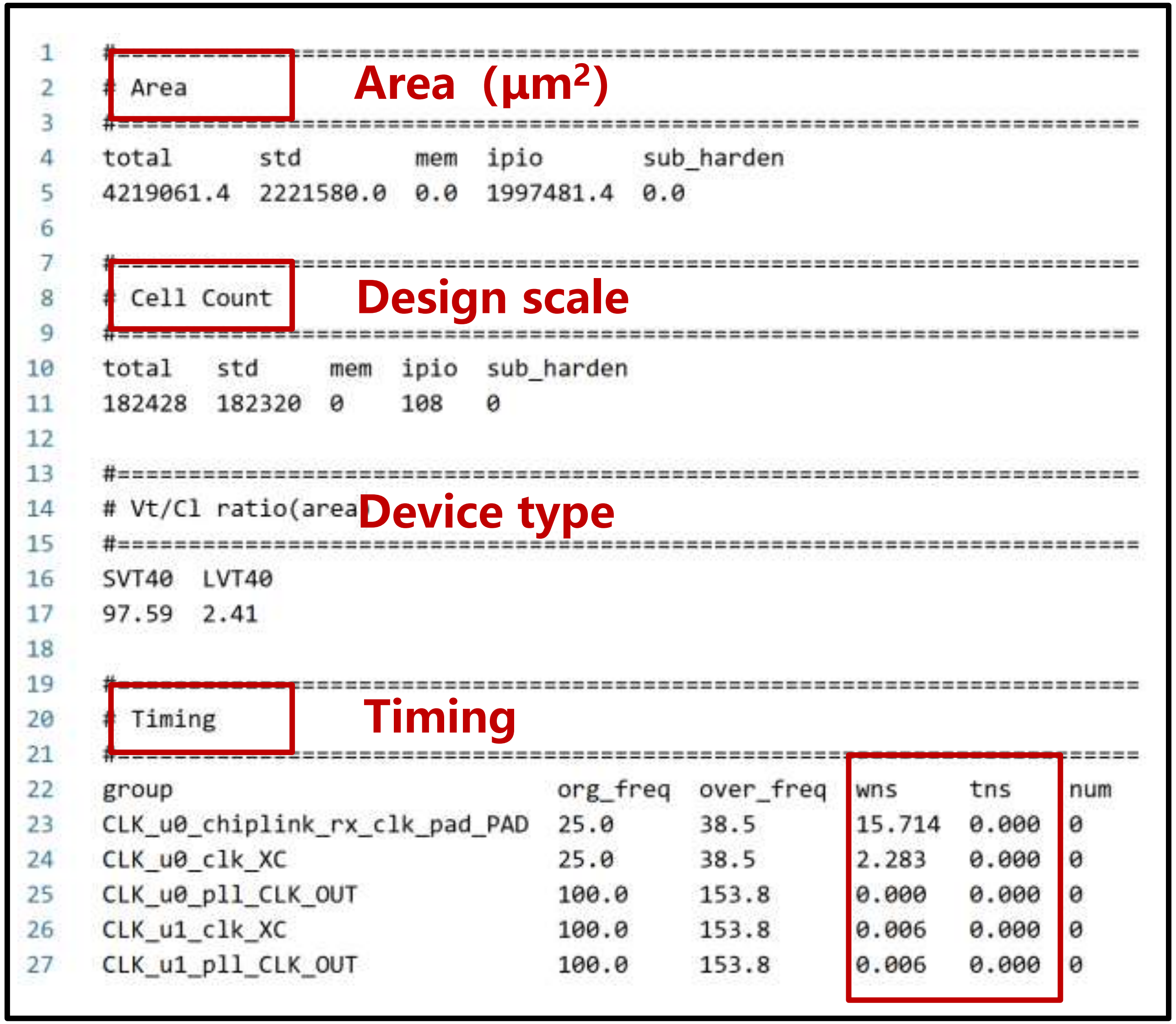
- **BC**：ff_0p88v_m40c：
  - fast process
  - high power voltage
  - low temperature
- **Typical**：typical_0p8v_25c：
  - typical process
  - normal power voltage
  - normal temperature
- **WC**：ss_0p72v_125c：
  - slow process
  - low power voltage
  - high temperature

2. Synthesis

■ Synthesis report



- asic_top.area.rpt
- asic_top.check_design.pre.rpt
- asic_top.check_design.rpt
- asic_top.check_timing.rpt
- asic_top.clock_gating.rpt
- asic_top.clock.rpt
- asic_top.constraint.rpt
- asic_top.dont_touch.rpt
- asic_top.drc.rpt
- asic_top.power.rpt
- asic_top.qor.rpt
- asic_top.registers.rpt
- asic_top.statistics.rpt
- asic_top.timing.rpt



```
#==========================================================================
# Area
#==========================================================================
total      std        mem  ipio       sub_harden
4219061.4  2221580.0  0.0  1997481.4  0.0

#==========================================================================
# Cell Count
#==========================================================================
total   std     mem  ipio  sub_harden
182428  182320  0    108   0

#==========================================================================
# Vt/Cl ratio(area
#==========================================================================
SVT40  LVT40
97.59  2.41

#==========================================================================
# Timing
#==========================================================================
group                           org_freq  over_freq  wns     tns    num
CLK_u0_chiplink_rx_clk_pad_PAD  25.0      38.5       15.714  0.000  0
CLK_u0_clk_XC                   25.0      38.5       2.283   0.000  0
CLK_u0_pll_CLK_OUT              100.0     153.8      0.000   0.000  0
CLK_u1_clk_XC                   100.0     153.8      0.006   0.000  0
CLK_u1_pll_CLK_OUT              100.0     153.8      0.006   0.000  0
```

Area (μm²)

Design scale

Device type

Timing

CONTENTS

1. Overview of the Back-end

2. Logical synthesis

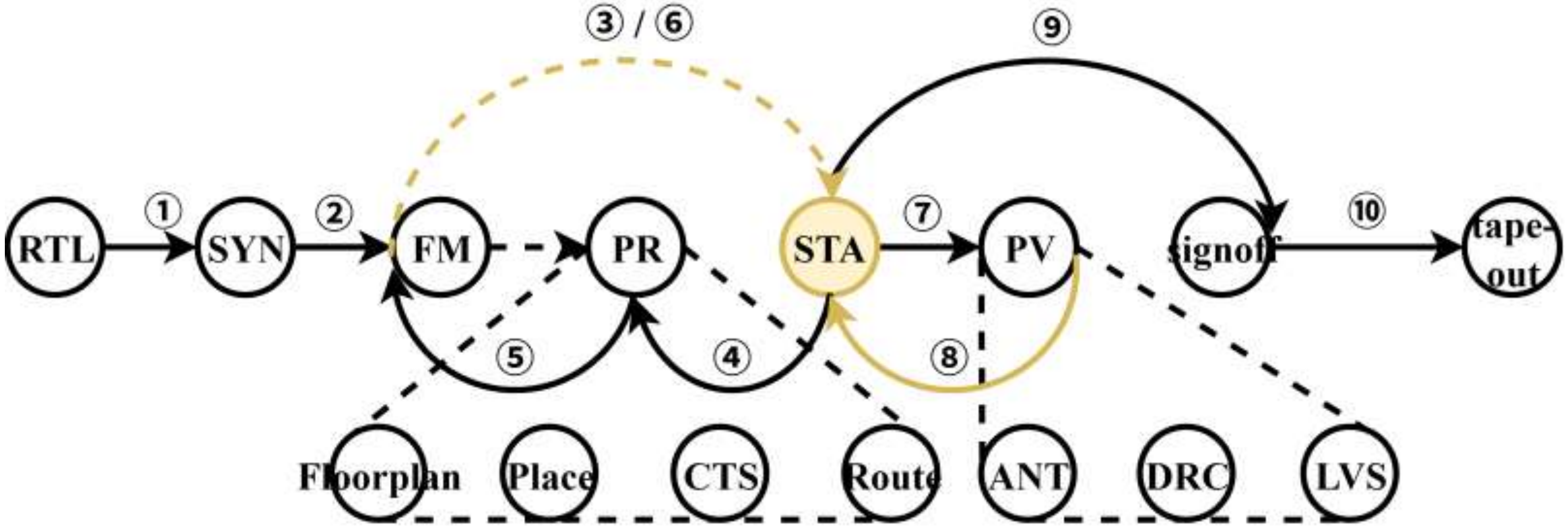
3. Timing analysis

4. Place & Route

5. Physical verification

Static Timing Analysis (STA)

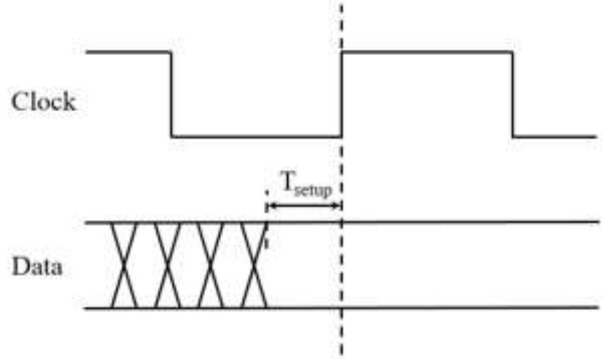
- **STA is the method for verifying the circuit timing by checking the timing information of all paths**
  - ➢ Divide the design into several paths
  - ➢ Calculate the delay of each path respectively
  - ➢ Check whether the delay of each path meets the design constraints

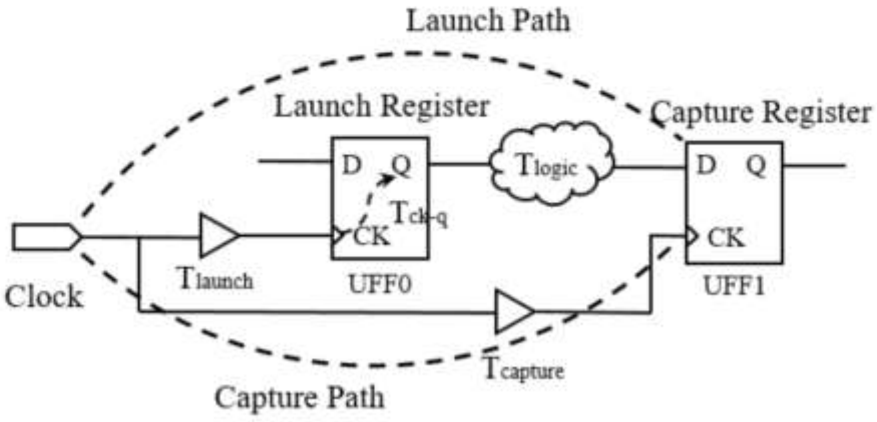


3. Timing Analysis

Setup Time（T_{setup})

- T_{setup} is the time when the data remains stable before the rising edge of the clock arrives





（1）The time when the data reaches the D end of UFF1(arrival time)：

$$T_a = T_{launch} + T_{ck\text{-}q} + T_{logic}$$

（2）Meet the maximum time allowed by setup (required time)：

$$T_r = T_{capture} + T_{clk} - T_{setup}$$

（3）According to the setup time requirements，$T_r - T_a = T_{margin} \geq 0$

$$T_{capture} + T_{clk} - T_{setup} - T_{launch} - T_{ck\text{-}q} - T_{logic} \geq 0$$

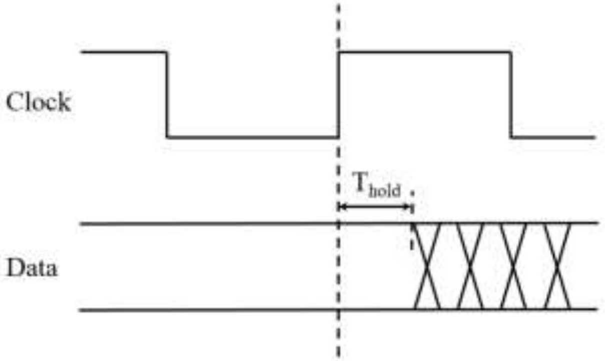
（4）Let $T_{capture} - T_{launch} = T_{skew}$， and we get：

$$T_{skew} + T_{clk} \geq T_{setup} + T_{ck\text{-}q} + T_{logic}$$

3. Timing Analysis

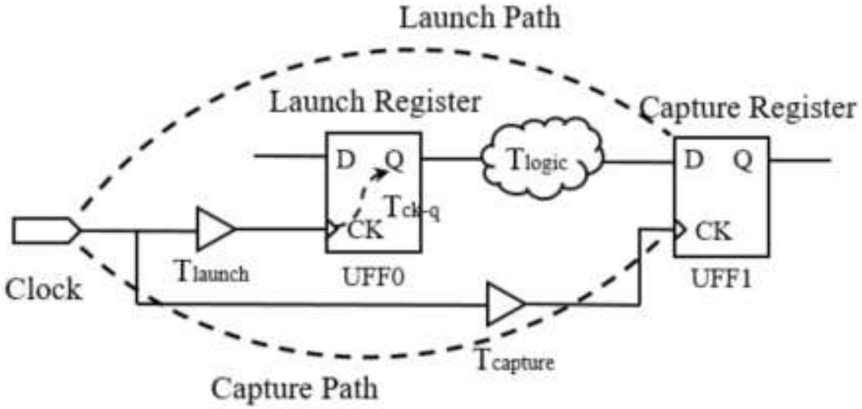
■ Hold Time （T_{hold}）

- ■ T_{hold} is the time when the data remains stable after the rising edge of the clock arrives



（1） The time when the data reaches the D end of UFF1(arrival time)：

$$T_a = T_{launch} + T_{ck\text{-}q} + T_{logic}$$



2）Meet the maximum time allowed by hold (required time)：

$$T_r = T_{capture} + T_{hold}$$

3） According to the hold time requirements， $T_a - T_r = T_{margin} \geq 0$

$$T_{launch} + T_{ck\text{-}q} + T_{logic} - T_{capture} - T_{hold} \geq 0$$

（4）Let $T_{capture} - T_{launch} = T_{skew}$， and we get：

$$T_{skew} + T_{hold} \leq T_{ck\text{-}q} + T_{logic}$$

Timing violation repair

- Method for fixing $\mathbf{T_{setup}}$ timing violations:

$$T_{skew} + T_{clk} \ge T_{setup} + T_{ck\text{-}q} + T_{logic}$$

（1）Increase T_{clk}： Reduce frequency

（2）Reduce T_{logic}： Optimize combinatorial logic, divide the pipeline, and reduce the load on the critical path

（3）Reduce $T_{ck\text{-}q}$： Switch to faster logic units, such as HVT->LVT

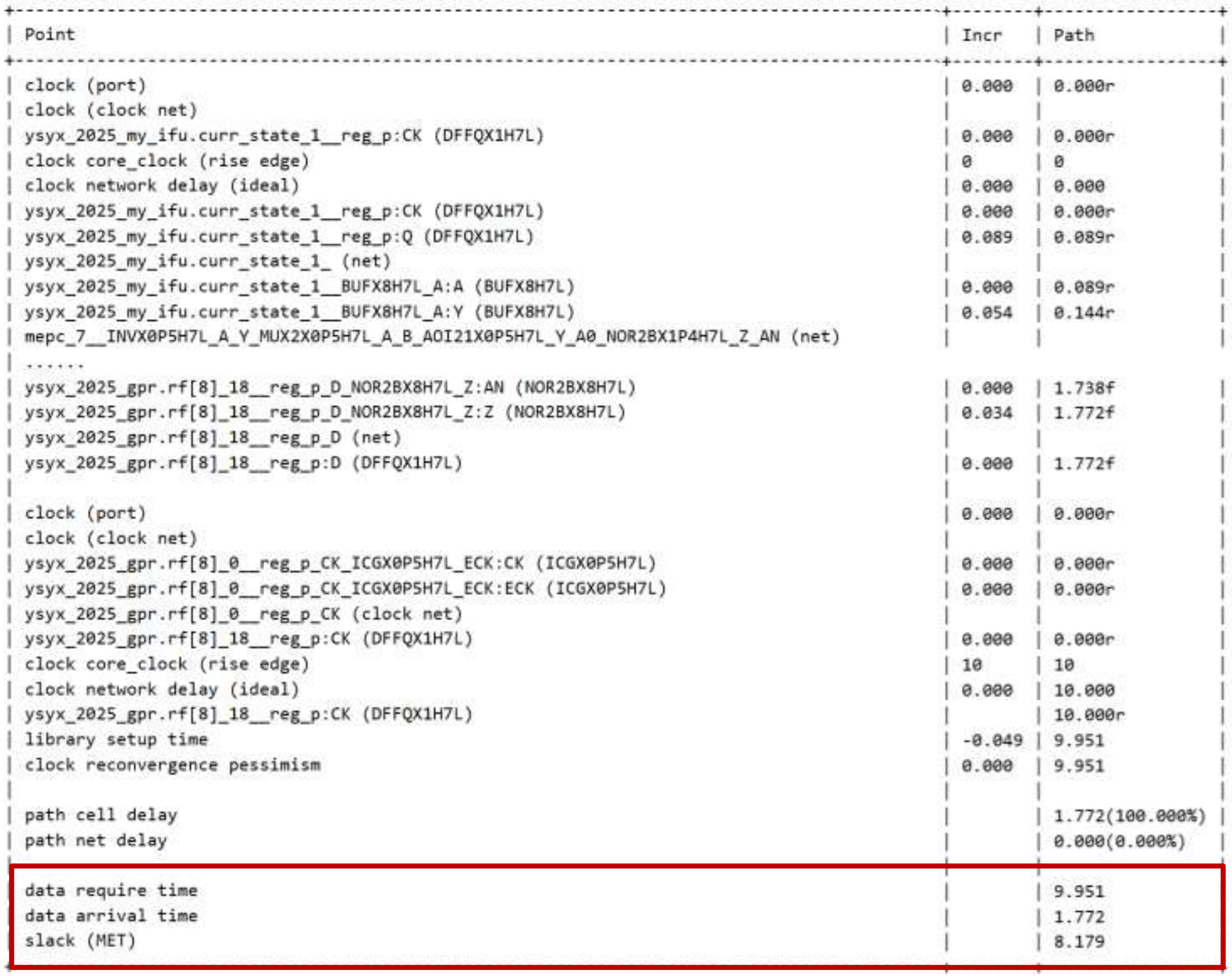
- Method for fixing $\mathbf{T_{hold}}$ timing violations:

$$T_{skew} + T_{hold} \le T_{ck\text{-}q} + T_{logic}$$

（1） Increase T_{logic}： Increase the delay of the combined path and insert the buffer

（2）Reduce T_{skew}： Even adopt a negative skew.

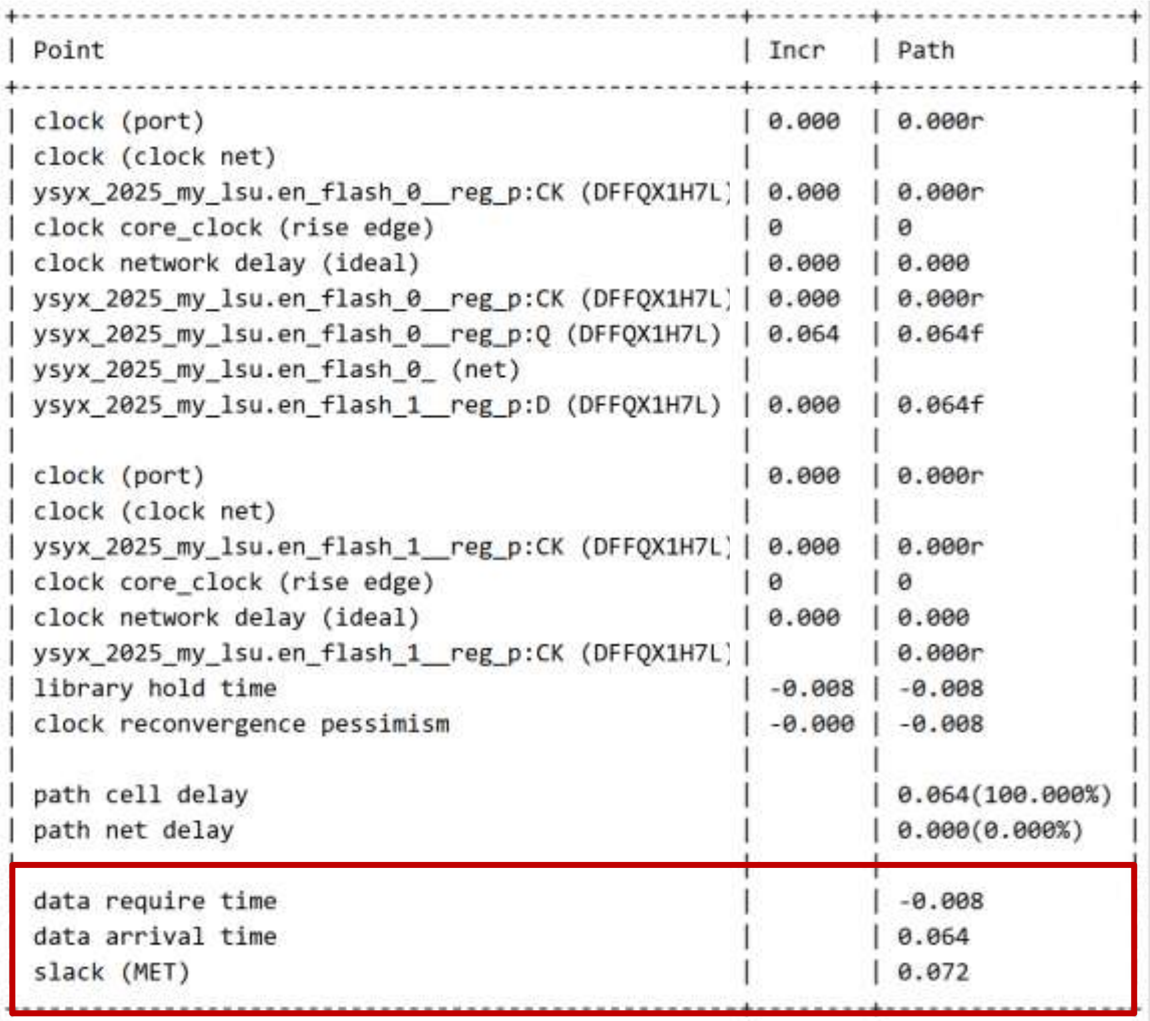
3.Timing Analysis（T_{setup}）



```
+------------------------------------------------------------------------------------+---------+------------------+
| Point                                                                              | Incr    | Path             |
+------------------------------------------------------------------------------------+---------+------------------+
| clock (port)                                                                       | 0.000   | 0.000r           |
| clock (clock net)                                                                  |         |                  |
| ysyx_2025_my_ifu.curr_state_1__reg_p:CK (DFFQX1H7L)                                | 0.000   | 0.000r           |
| clock core_clock (rise edge)                                                       | 0       | 0                |
| clock network delay (ideal)                                                        | 0.000   | 0.000            |
| ysyx_2025_my_ifu.curr_state_1__reg_p:CK (DFFQX1H7L)                                | 0.000   | 0.000r           |
| ysyx_2025_my_ifu.curr_state_1__reg_p:Q (DFFQX1H7L)                                 | 0.089   | 0.089r           |
| ysyx_2025_my_ifu.curr_state_1_ (net)                                               |         |                  |
| ysyx_2025_my_ifu.curr_state_1__BUFX8H7L_A:A (BUFX8H7L)                             | 0.000   | 0.089r           |
| ysyx_2025_my_ifu.curr_state_1__BUFX8H7L_A:Y (BUFX8H7L)                             | 0.054   | 0.144r           |
| mepc_7__INVX0P5H7L_A_Y_MUX2X0P5H7L_A_B_AOI21X0P5H7L_Y_A0_NOR2BX1P4H7L_Z_AN (net)   |         |                  |
| ......
| ysyx_2025_gpr.rf[8]_18__reg_p_D_NOR2BX8H7L_Z:AN (NOR2BX8H7L)                       | 0.000   | 1.738f           |
| ysyx_2025_gpr.rf[8]_18__reg_p_D_NOR2BX8H7L_Z:Z (NOR2BX8H7L)                        | 0.034   | 1.772f           |
| ysyx_2025_gpr.rf[8]_18__reg_p_D (net)                                              |         |                  |
| ysyx_2025_gpr.rf[8]_18__reg_p:D (DFFQX1H7L)                                        | 0.000   | 1.772f           |
|                                                                                    |         |                  |
| clock (port)                                                                       | 0.000   | 0.000r           |
| clock (clock net)                                                                  |         |                  |
| ysyx_2025_gpr.rf[8]_0__reg_p_CK_ICGX0P5H7L_ECK:CK (ICGX0P5H7L)                     | 0.000   | 0.000r           |
| ysyx_2025_gpr.rf[8]_0__reg_p_CK_ICGX0P5H7L_ECK:ECK (ICGX0P5H7L)                    | 0.000   | 0.000r           |
| ysyx_2025_gpr.rf[8]_0__reg_p_CK (clock net)                                        |         |                  |
| ysyx_2025_gpr.rf[8]_18__reg_p:CK (DFFQX1H7L)                                       | 0.000   | 0.000r           |
| clock core_clock (rise edge)                                                       | 10      | 10               |
| clock network delay (ideal)                                                        | 0.000   | 10.000           |
| ysyx_2025_gpr.rf[8]_18__reg_p:CK (DFFQX1H7L)                                       |         | 10.000r          |
| library setup time                                                                 | -0.049  | 9.951            |
| clock reconvergence pessimism                                                      | 0.000   | 9.951            |
|                                                                                    |         |                  |
| path cell delay                                                                    |         | 1.772(100.000%)  |
| path net delay                                                                     |         | 0.000(0.000%)    |
+------------------------------------------------------------------------------------+---------+------------------+
| data require time                                                                  |         | 9.951            |
| data arrival time                                                                  |         | 1.772            |
| slack (MET)                                                                        |         | 8.179            |
+------------------------------------------------------------------------------------+---------+------------------+
```

slack = T_r - T_a =9.951-1.772=8.179>0，The timing meets the requirements.

3. Timing Analysis（ T_{hold}）



```
+-----------------------------------------------------------+---------+-----------------+
| Point                                                     | Incr    | Path            |
+-----------------------------------------------------------+---------+-----------------+
| clock (port)                                              | 0.000   | 0.000r          |
| clock (clock net)                                         |         |                 |
| ysyx_2025_my_lsu.en_flash_0__reg_p:CK (DFFQX1H7L)         | 0.000   | 0.000r          |
| clock core_clock (rise edge)                              | 0       | 0               |
| clock network delay (ideal)                               | 0.000   | 0.000           |
| ysyx_2025_my_lsu.en_flash_0__reg_p:CK (DFFQX1H7L)         | 0.000   | 0.000r          |
| ysyx_2025_my_lsu.en_flash_0__reg_p:Q (DFFQX1H7L)          | 0.064   | 0.064f          |
| ysyx_2025_my_lsu.en_flash_0_ (net)                        |         |                 |
| ysyx_2025_my_lsu.en_flash_1__reg_p:D (DFFQX1H7L)          | 0.000   | 0.064f          |
|                                                           |         |                 |
| clock (port)                                              | 0.000   | 0.000r          |
| clock (clock net)                                         |         |                 |
| ysyx_2025_my_lsu.en_flash_1__reg_p:CK (DFFQX1H7L)         | 0.000   | 0.000r          |
| clock core_clock (rise edge)                              | 0       | 0               |
| clock network delay (ideal)                               | 0.000   | 0.000           |
| ysyx_2025_my_lsu.en_flash_1__reg_p:CK (DFFQX1H7L)         |         | 0.000r          |
| library hold time                                         | -0.008  | -0.008          |
| clock reconvergence pessimism                             | -0.000  | -0.008          |
|                                                           |         |                 |
| path cell delay                                           |         | 0.064(100.000%) |
| path net delay                                            |         | 0.000(0.000%)   |
+-----------------------------------------------------------+---------+-----------------+
  data require time                                         |         | -0.008
  data arrival time                                         |         | 0.064
  slack (MET)                                               |         | 0.072
+-----------------------------------------------------------+---------+-----------------+
```

slack = T_a- T_r =0.064-(-0.008)=0.072>0， The timing meets the requirements.

CONTENTS

1. Overview of the Back-end

2. Logical synthesis

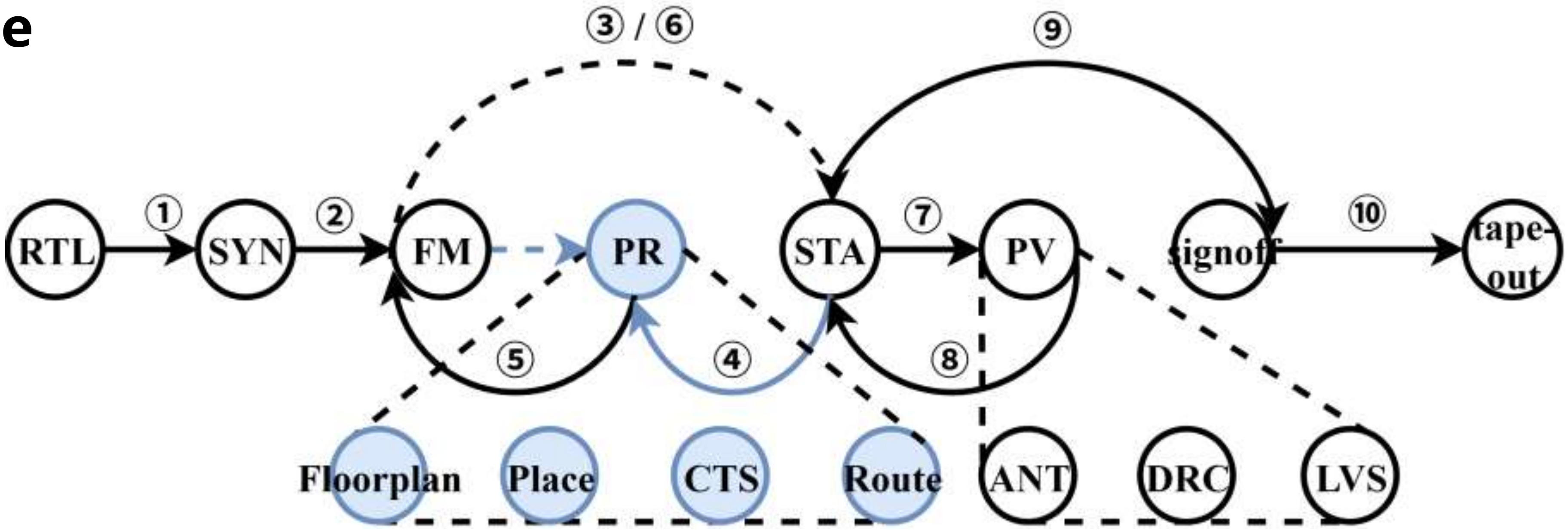
3. Timing analysis

4. Place & Route

5. Physical verification

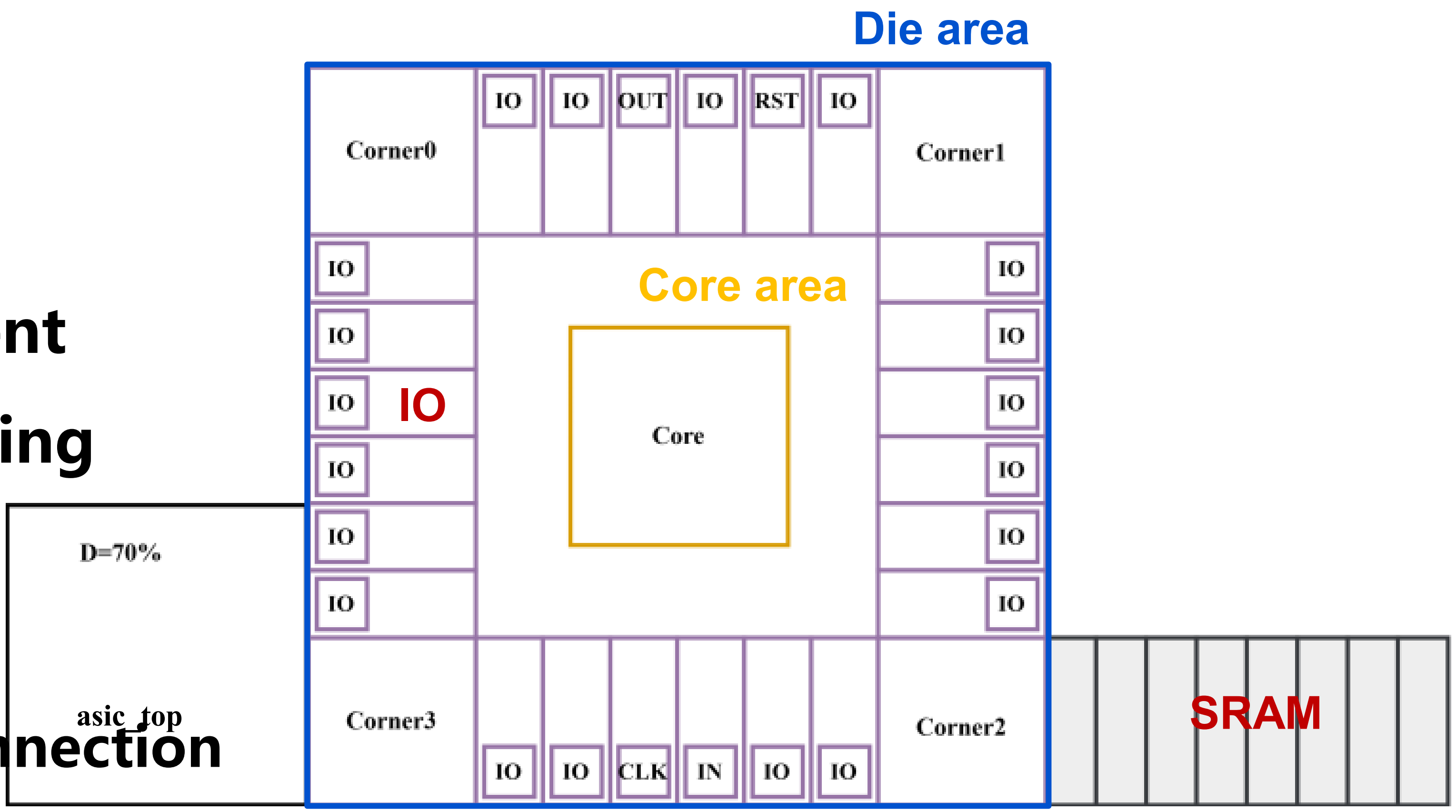
Place & Route(PR)

- Floorplan
- Place
- Clock Tree Synthesis(CTS)
- Route



4. Place & Route

- init & Floorplan
  - Chip design input
  - Chip I/O planning
  - Macro unit placement
  - Power supply planning
    - Power ring design
    - Power grid design
    - Power network connection

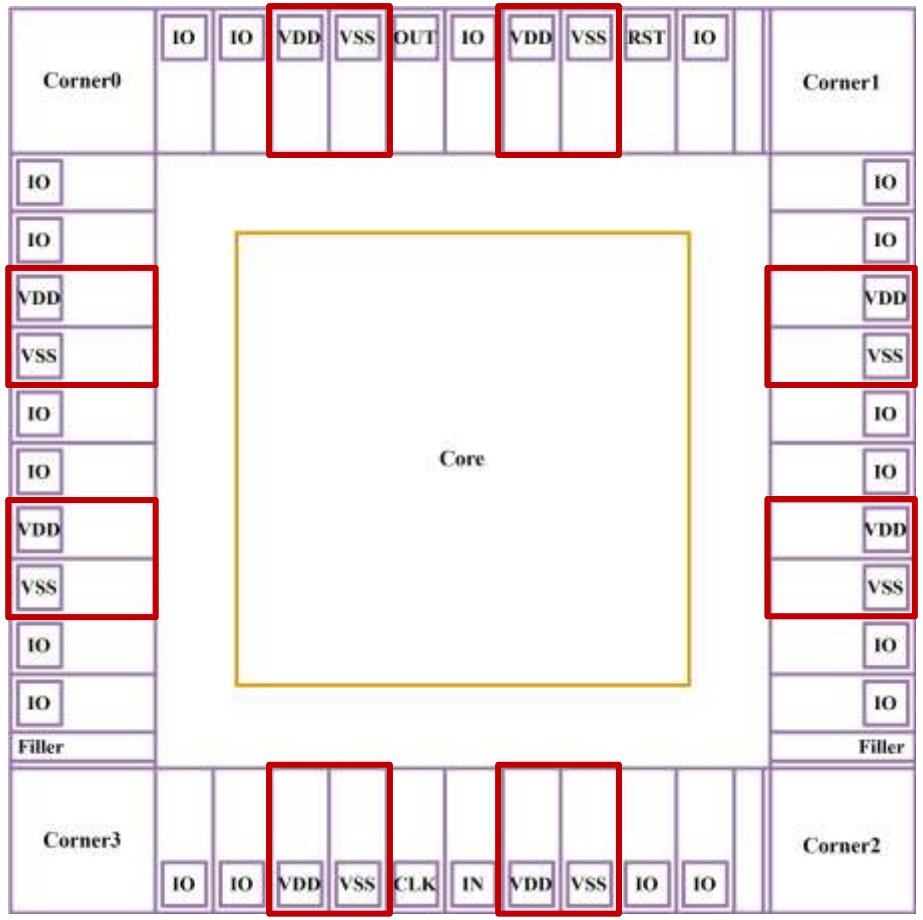


Chip utilization rate D=(Total area of standard units)/(Core area - SRAM)

4. Place & Route

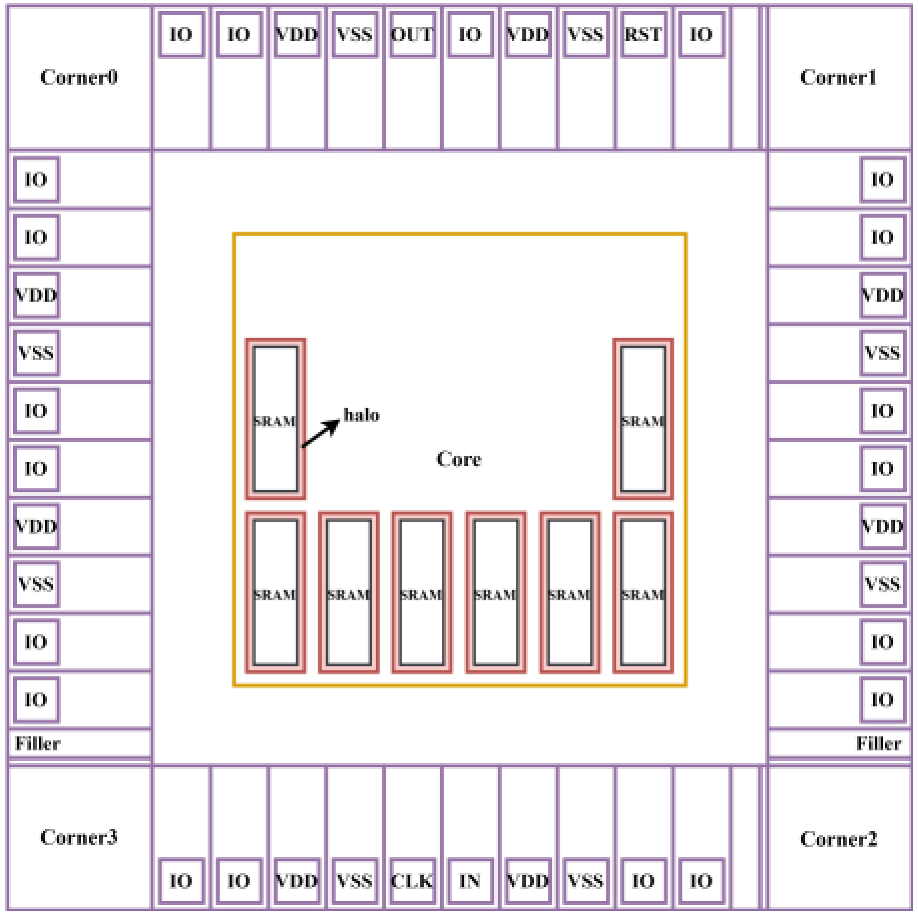
- init & Floorplan
  - Chip design input
  - Chip I/O planning
  - Macro unit placement
  - Power supply planning
    - ➢ Power ring design
    - ➢ Power grid design
    - ➢ Power network connection

VDD/VSS



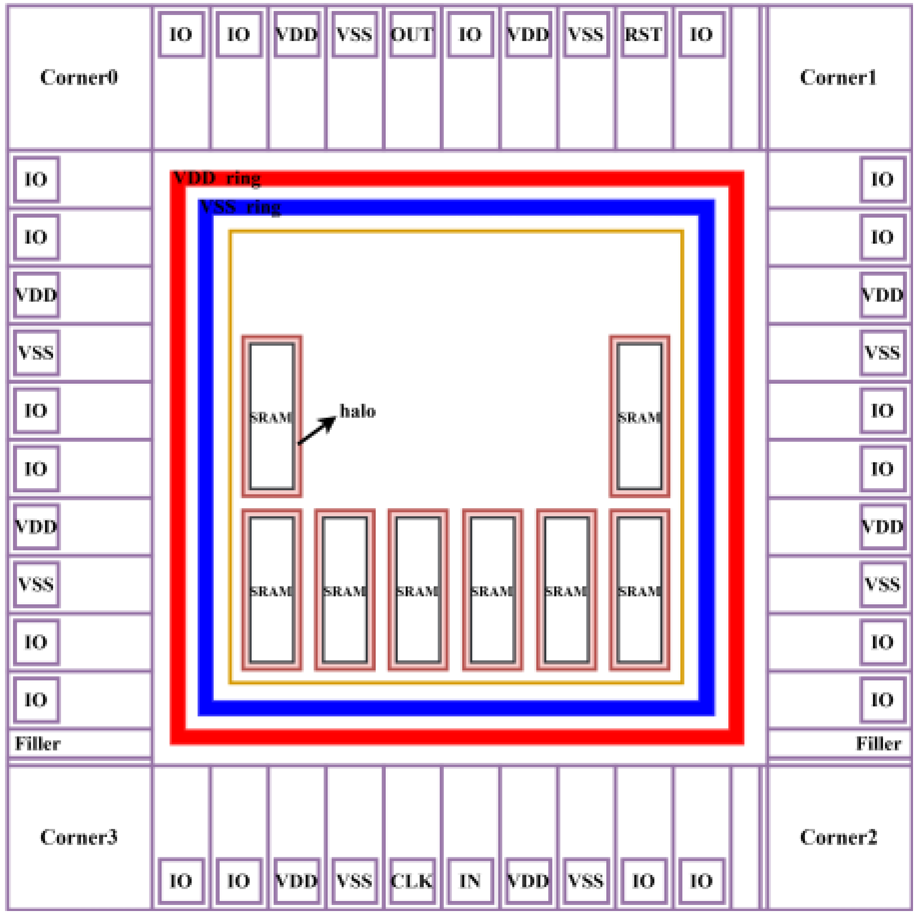
4. Place & Route

- init & Floorplan
  - Chip design input
  - Chip I/O planning
  - Macro unit placement
  - Power supply planning
    - ➢ Power ring design
    - ➢ Power grid design
    - ➢ Power network connection



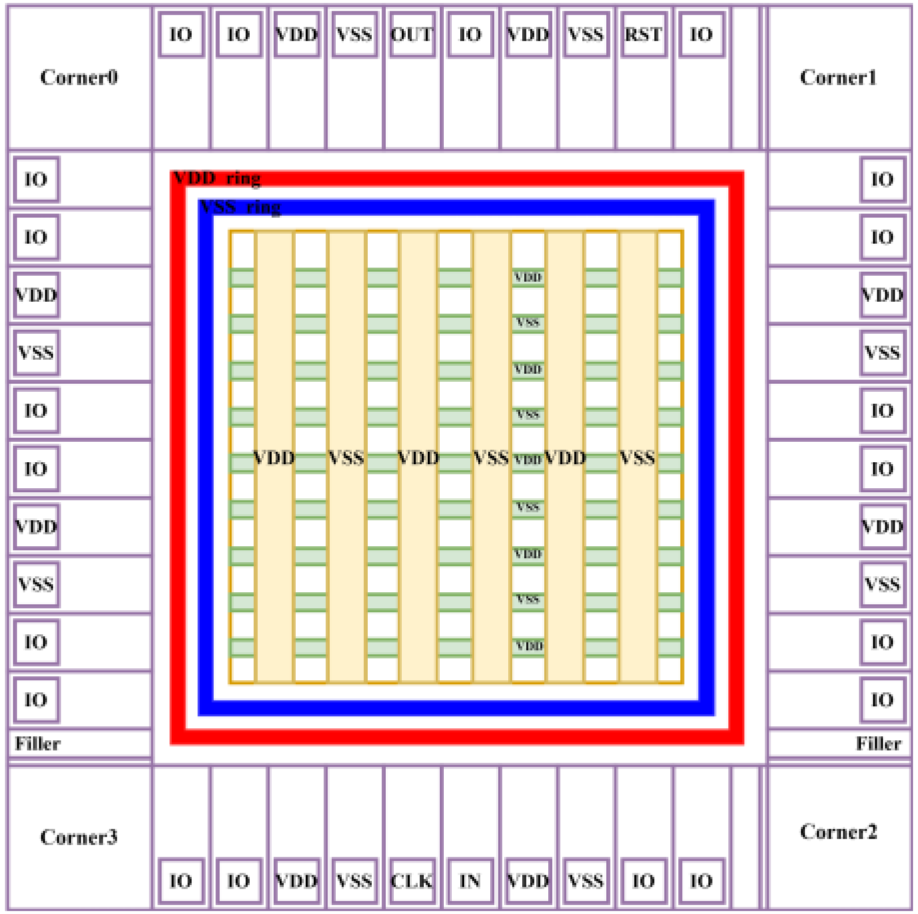
4. Place & Route

- init & Floorplan
  - Chip design input
  - Chip I/O planning
  - Macro unit placement
  - Power supply planning
    - ➢ Power ring design
    - ➢ Power grid design
    - ➢ Power network connection



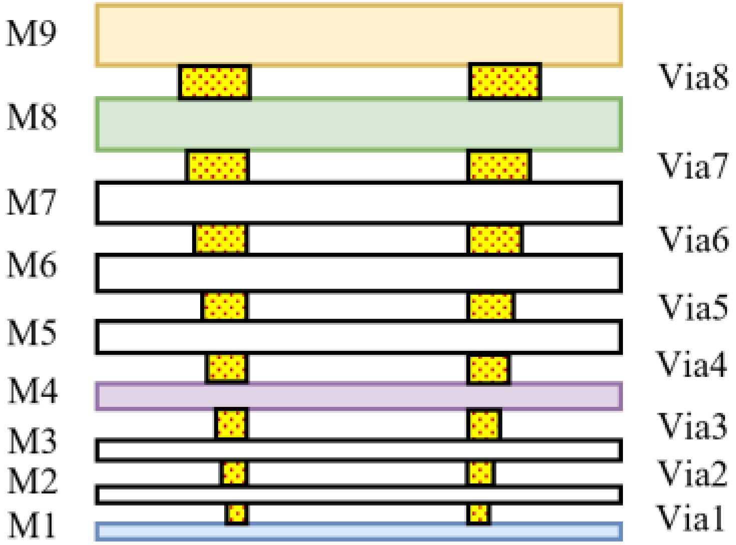
4. Place & Route

- init & Floorplan
  - Chip design input
  - Chip I/O planning
  - Macro unit placement
  - Power supply planning
    - Power ring design
    - Power grid design
    - Power network connection

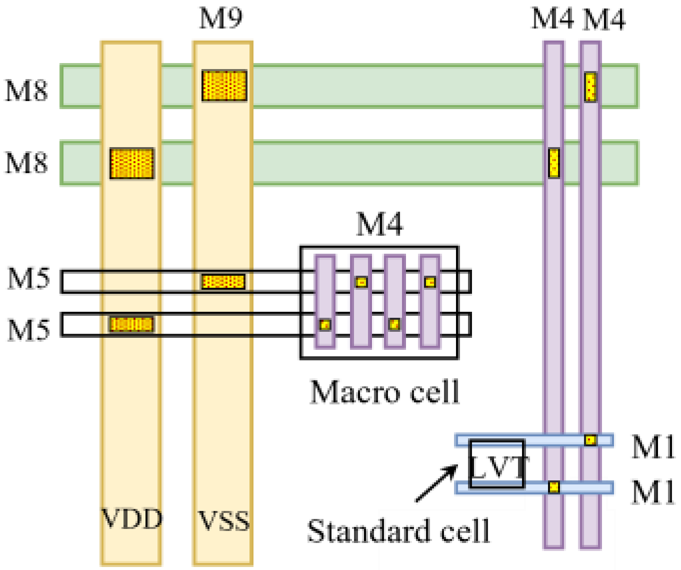


4. Place & Route

- **init & Floorplan**
  - **Chip design input**
  - **Chip I/O planning**
  - **Macro unit placement**
  - **Power supply planning**
    - ➢ **Power ring design**
    - ➢ **Power grid design**
    - ➢ **Power network connection**



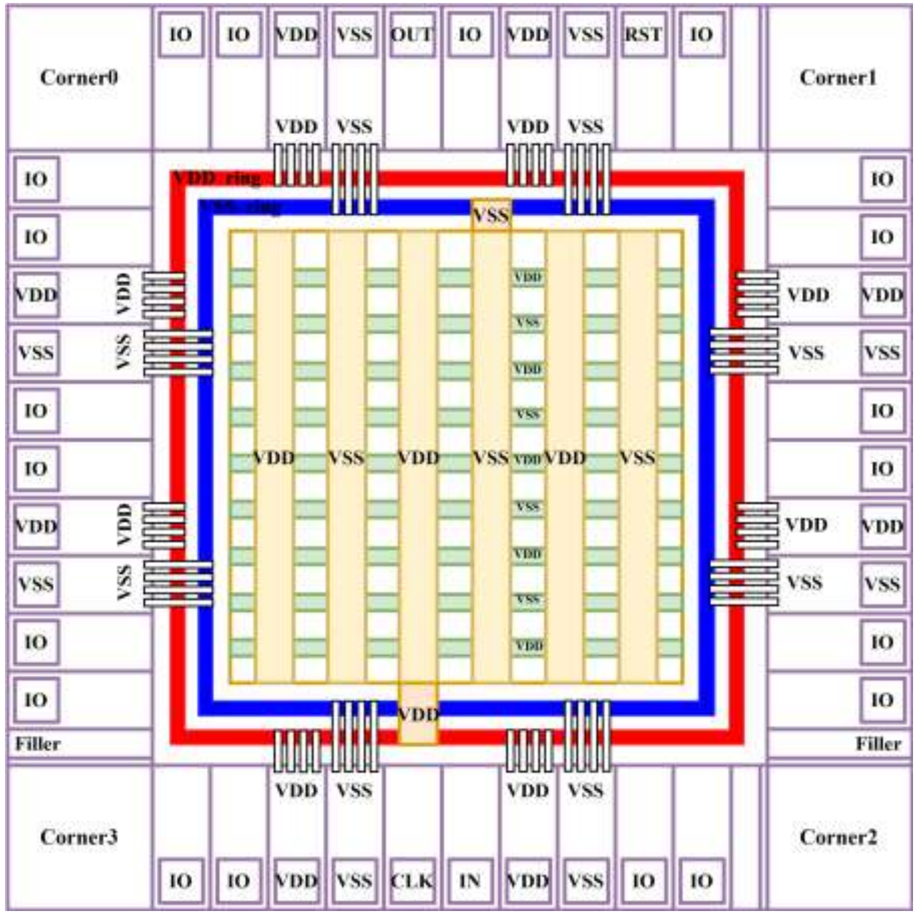
Routing metal layer



Power grid

4. Place & Route

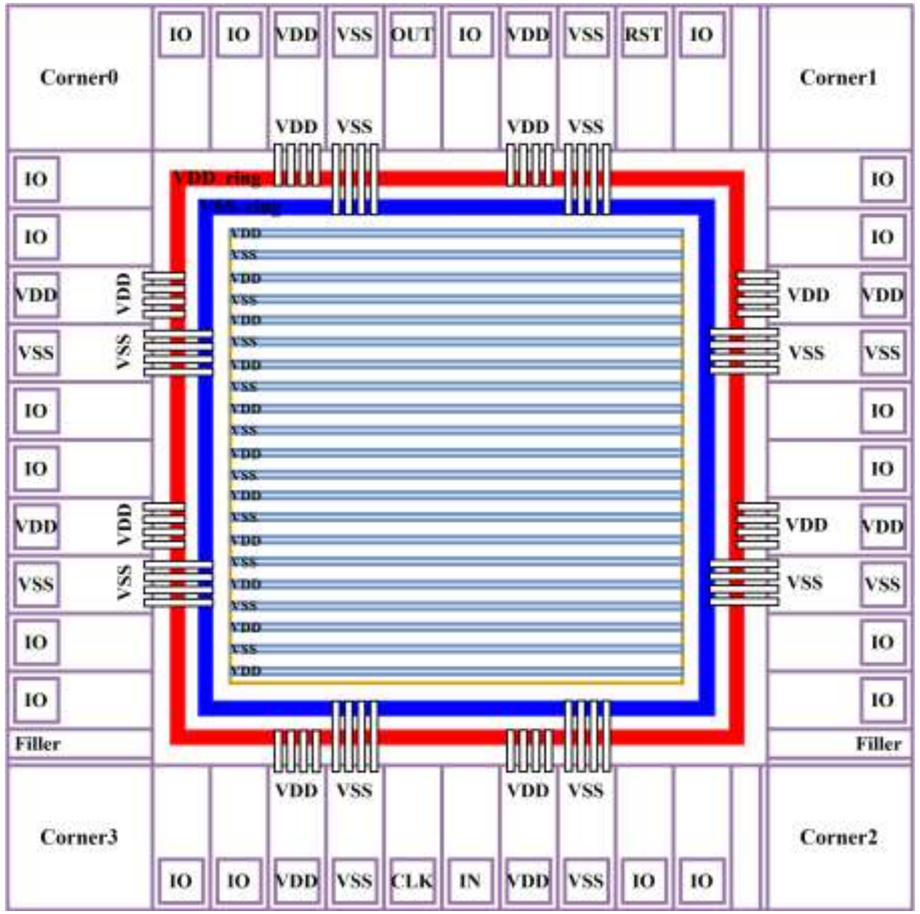
- init & Floorplan
  - Chip design input
  - Chip I/O planning
  - Macro unit placement
  - Power supply planning
    - Power ring design
    - Power grid design
    - Power network connection



4. Place & Route

■ Place

- ■ The placement of standard units
  - ➢ Global place
  - ➢ Detail place
- ■ Optimization of standard units
  - ➢ Whether it meets the timing sequence
  - ➢ Whether it has sufficient resources

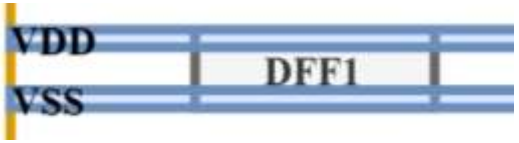


Before Place

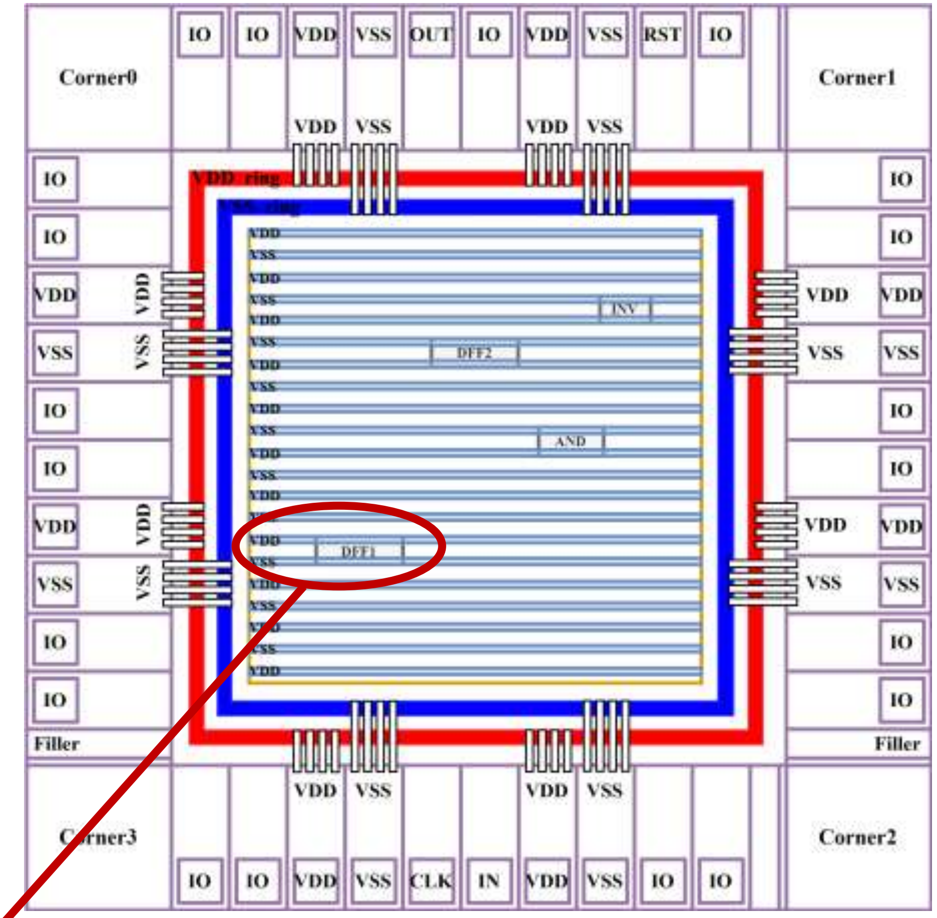
4. Place & Route

■ Place

- ■ The placement of standard units
  - ➢ Global place
  - ➢ Detail place
- ■ Optimization of standard units
  - ➢ Whether it meets the timing sequence
  - ➢ Whether it has sufficient resources



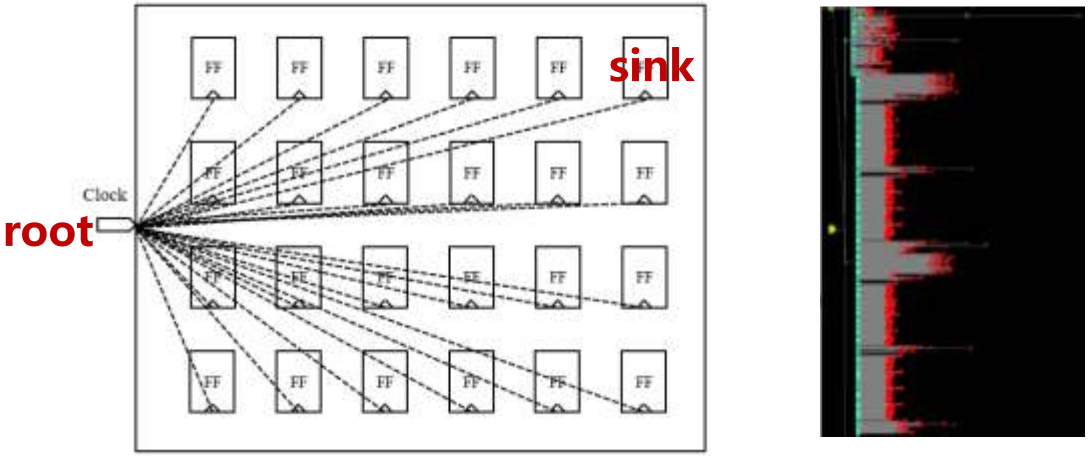
Standard Cell



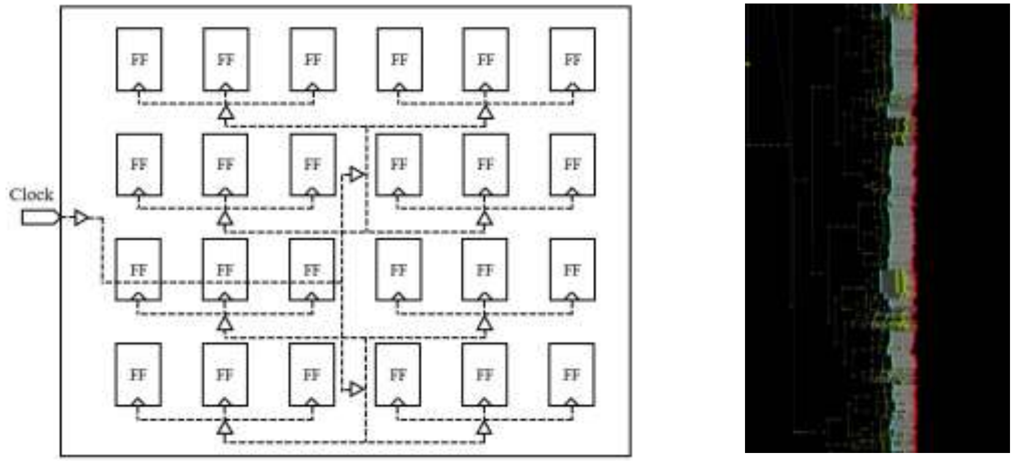
After Place

4. Place & Route

- **CTS**
  - **Growing clock tree**
    - ➢ The clock grows from the root point to each sink point
    - ➢ The time skew of the clock reaching the clock terminals of each register should be as small as possible
  - **Clock tree routing**
  - **Optimize the timing**

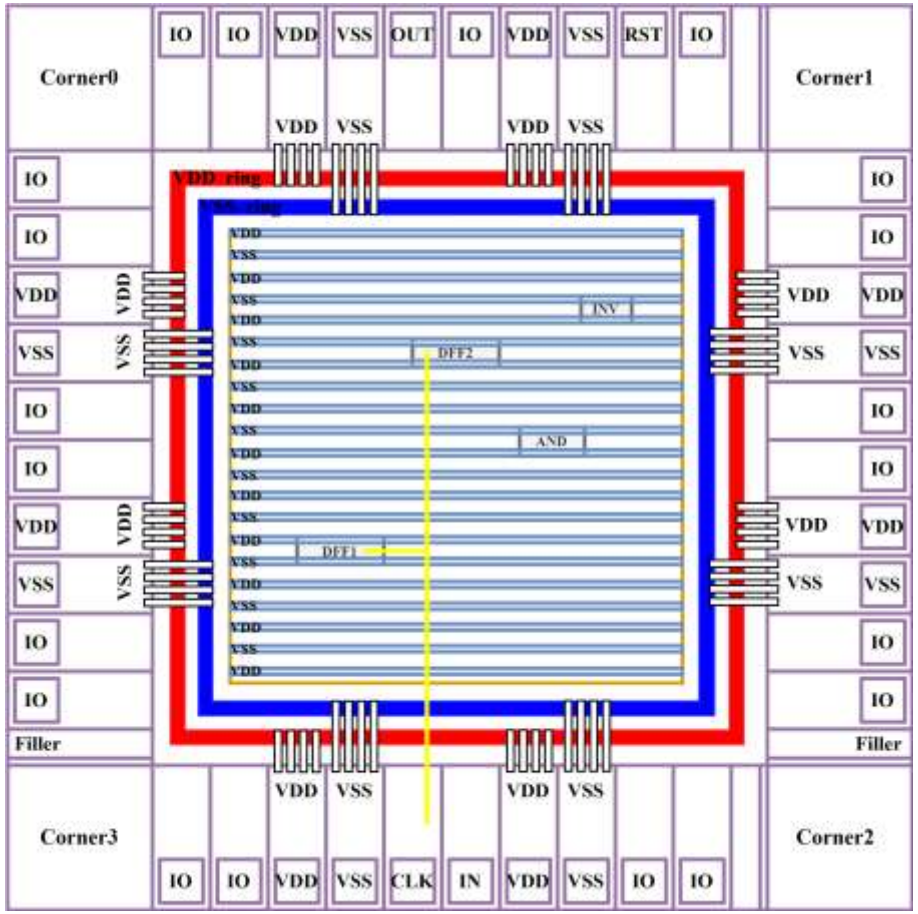


Before CTS



After CTS

- **CTS**
  - **Growing clock tree**
    - The clock grows from the root point to each sink point
    - The time skew of the clock reaching the clock terminals of each register should be as small as possible
  - **Clock tree routing**
  - **Optimize the timing**



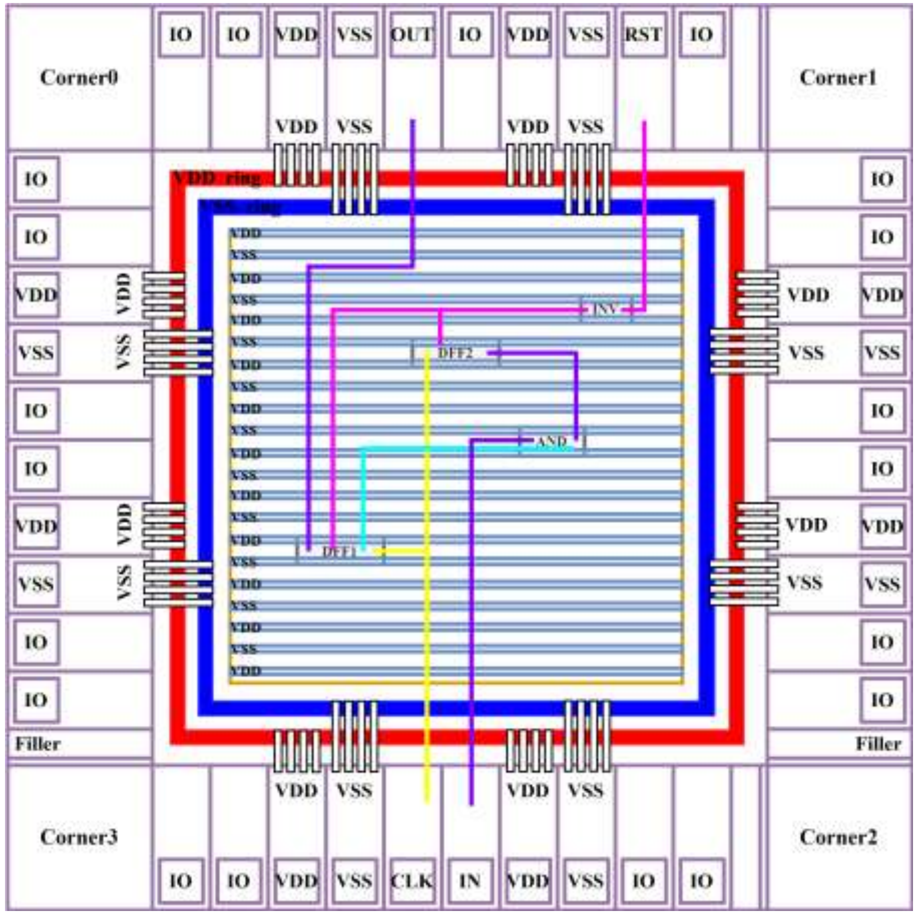
4. Place & Route

Route

- Global routing
  - ➢ Plan the signal path and allocate wiring resources
- Detail routing
  - ➢ Implement the physical path to satisfy DRC
- Search and repair
  - ➢ Fix the violations after routing

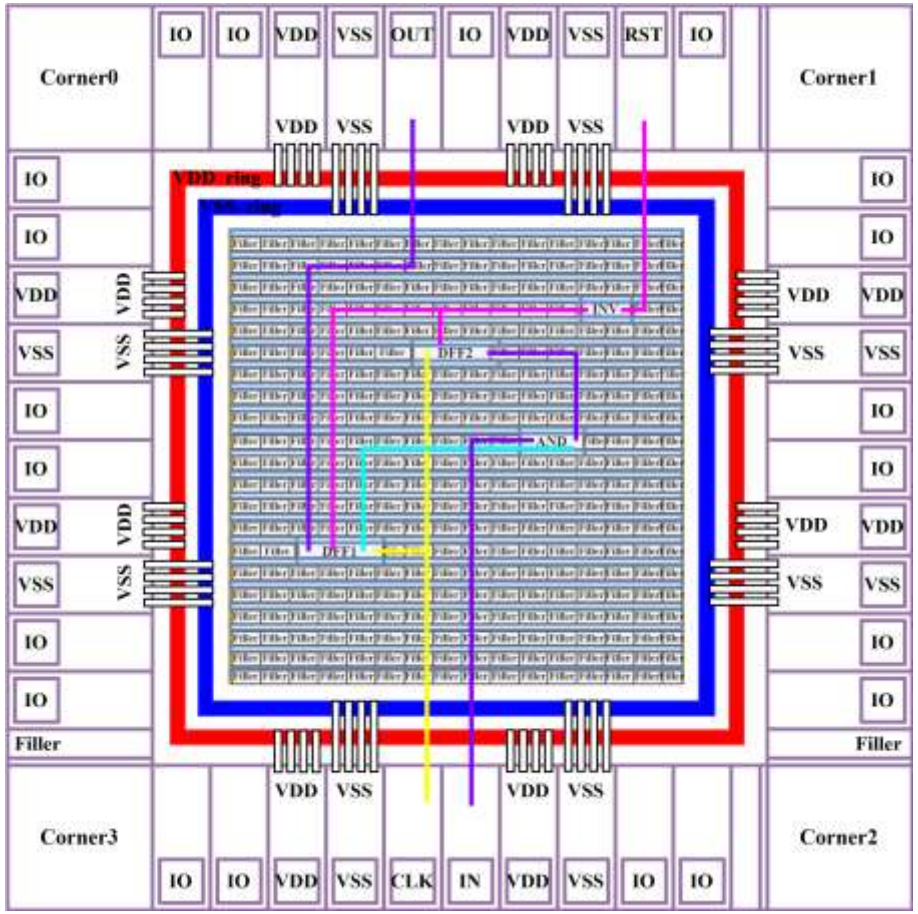
Filler insert

- Insert the standard Filler cell
  - ➢ Connect the diffusion layer to form the power ground track



4. Place & Route

- Route
  - Global routing
    - ➢ Plan the signal path and allocate wiring resources
  - Detail routing
    - ➢ Implement the physical path to satisfy DRC
  - Search and repair
    - ➢ Fix the violations after routing
- Filler insert
  - Insert the standard Filler cell
    - ➢ Connect the diffusion layer to form the power ground track



中国科学院
CHINESE ACADEMY OF SCIENCES

CONTENTS

1. Overview of the Back-end

2. Logical synthesis

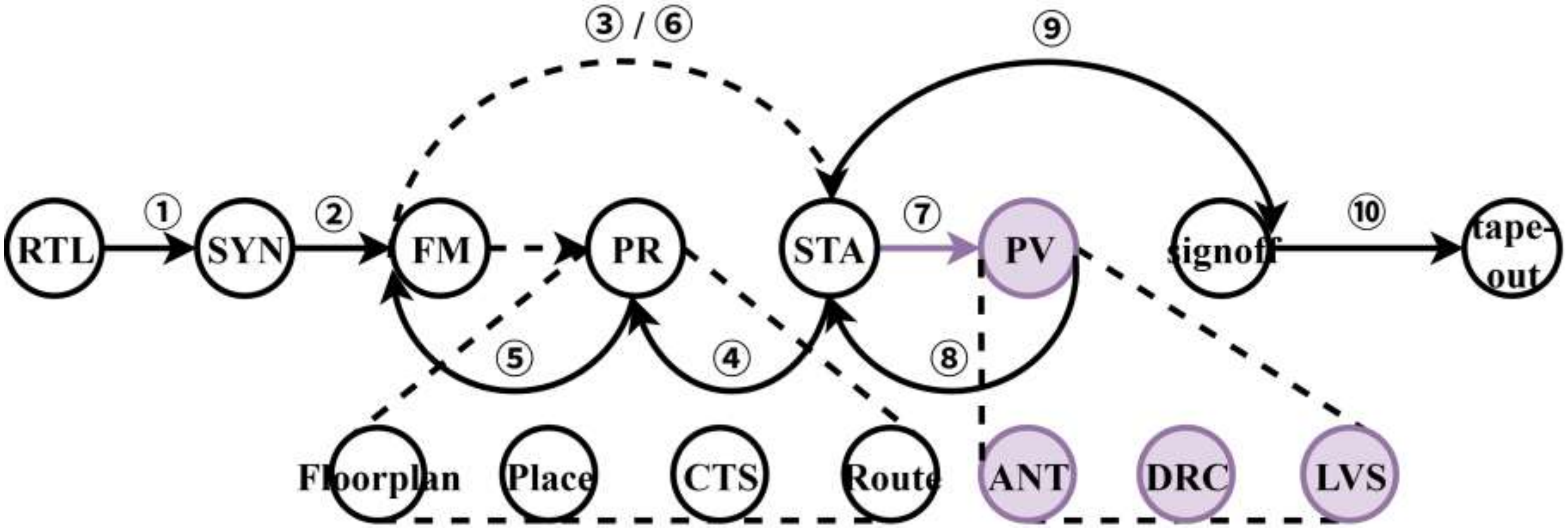
3. Timing analysis

4. Place & Route

5. Physical verification

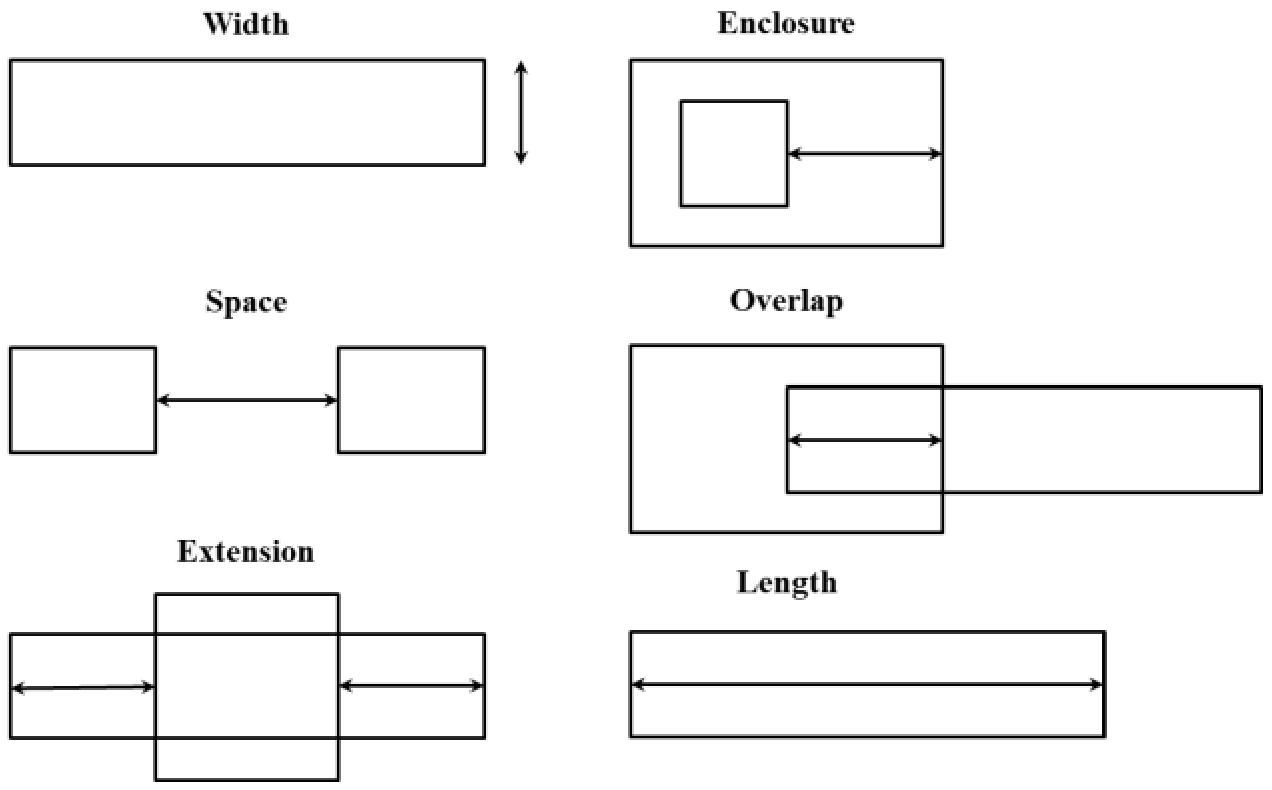
Physical Verification (PV)

- Electrical Rule Check (ERC)
- Design Rule Check (DRC)
- Layout Versus Schematic (LVS)



■ Design Rule Check（DRC)

- Ensure that the design of the chip layout complies with the design rules provided by the wafer fab (whether it can be manufactured)



Design Rules

Thanks!