PSpice Libraries for p-Channel Power Transistors

Models provided by Infineon are not warranted by Infineon as fully representing all the specifications and operating characteristics of the semiconductor product to which the model relates. The models describe the characteristics of typical devices. In all cases, the current data sheet information for a given device is the final design guideline and the only actual performance specification.

Although models can be a useful tool in evaluating device performance, they cannot model exact device performance under all conditions, nor are they intended to replace breadboarding for final verification. Infineon therefore does not assume any liability arising from their use.

Infineon reserves the right to change models without prior notice.

1 Installation

The downloaded modelling package consists of the following files relevant to the PSpice simulator:

- ***.lib file(s) comprising the PSpice code
- ***.slb file(s) providing symbols for the models required by the graphic user interface (GUI) 'Schematics'. (In order to be usable in evaluation versions of the PSpice/Schematics system, each symbol library does not contain more than twenty symbols.)
- ***.olb file(s) comprising symbols for the graphical user interface 'Capture'

If 'Schematics' is used as GUI, the ***.lib files must be installed via the 'Analysis → Library and Include Files' menu. Permanent installation via 'Add Library*' is recommended. The ***.slb files need to be installed via the menu 'Options → Editor Configuration → Library Settings'.

The installation in 'Capture' is similar. The ***.lib files must be included via the 'PSpice → Edit (New) Simulation Profile → Libraries' menu. Using the 'Add as Global' button will provide the models permanently. The symbol libraries (***.olb files) need to be included via 'Place → Part → Add Library'.

2 Definition of Modelling Levels

Infineon provides up to four different types of models for MOSFET devices. Three of them are based on a physical temperature-dependent model of the MOSFET structure and the package (so-called 'Level 1' till 'Level 3'). The fourth is a more empirical model that is less accurate, but faster and suitable for other Spice variants or simulators that can import Spice-like models ('Level 0')

Whereas Level 1 models assume a constant device temperature for the entire circuit and during a transient simulation (the temperature is to be given in the Analysis Setup), Level 2 models enable the user to define different temperatures for individual parts in the circuit. These temperatures can be changed dynamically during transient computations by connecting a voltage source to the Tj (junction temperature) pin. The voltage is converted into degree Celsius. If the Tj pin is not connected, a default temperature of 27 °C is used for the computation.

In order to be able to compute the self-heating dynamically, the electrical model is coupled with a thermal model of the device in Level 3 models. To do this, the current power dissipation in the transistor is determined permanently, and a current proportional to this power is fed into the thermal equivalent network. The voltage at the Tj node then contains the information about the time-dependent junction temperature which in turn acts directly on the temperature-dependent electrical model.

Level 3 models of single devices (one chip per package) have two external thermal nodes: First, there is Tj, where the user can monitor the junction temperature easily. Usually, this node should not be connected. However, when the computation should start with a device junction temperature different to the thermal equilibrium, connecting Tj with a small capacitor (typically 1pF) to ground and stating an initial value (parameter IC) for the initial potential difference (which is used as a measure for the initial temperature in °C) enables these types of simulations. The second thermal pin is Tcase (in TO packages), Tsolder_joint (in small signal packages like SO, SOT) or Tpad (in die models). This pin has to be connected. An external resistor-capacitor-network can be added between the Tcase pin and ground. The right-hand-side terminal of the heatsink RC-network has to be connected to a voltage source which represents the ambient temperature. (Fig. 1). On the other hand, connecting the ambient temperature source directly to the Tcase pin leads to a network where optimum heat transfer is modelled. (Fig. 2)

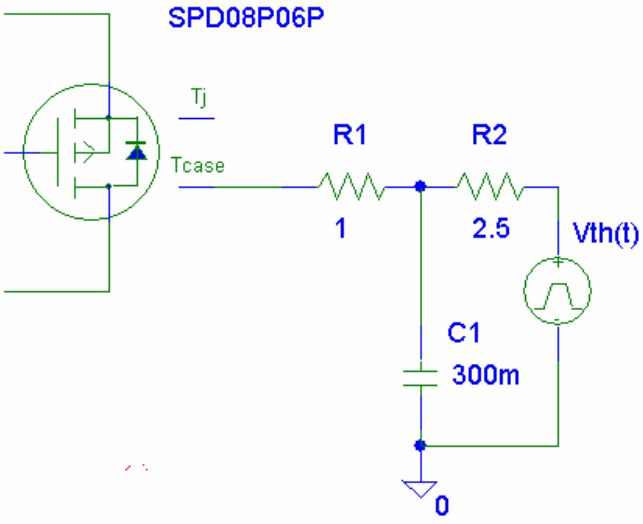

Fig. 1 Connecting a heat sink model to the device model

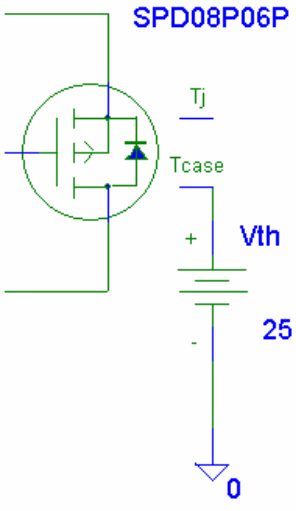

Fig. 2 Modelling of an ideal heat sink

Level 3 models for dual devices (ie devices comprising two dice) have a coupled thermal network which allows to compute the temperature rise in both chips for any switching state. Typically, these models have two pins for the junction temperatures (Tj1, Tj2) and the pins Tsolder_joint1 and Tsolder_joint2. Since often the thermal coupling between the two MOSFET subsystems is not restricted to internal heat flow, the external RC-networks should be connected in these cases as well. For example, if the drain pins of both MOSFETs are connected electrically directly at the device, the external coupling is considerable and, as a good approximation, the thermal pins Tsolder_joint1 and Tsolder_joint2 can be shorted.

The part names of Level 3 models are similar to the device names. For example, the Level 3 model of the SPD30P06P has the part name SPD30P06P. Level 1 and Level 2 models can be accessed using the suffixes L1 and L2, respectively. Hence, the models of the product above are named SPD30P06P_L1 and SPD30P06P_L2. For more details on the naming convention see the section 'Type Numbering System' given in the data book.

If the simulation focus is more on speed and not on accuracy, also simplified models are provided. These models can also be used in other Spice-like simulators that do not work with PSpice specific sytax like function statements. The model name of the SPD30P06P is SPD30P06P_L0, ie the suffix _L0 is used.

3 Optional Parameters for MOSFET Models

Model parameters are chosen to give the behaviour of a typical device. However, in order to enable worst-case and sensitivity analyses, models provide several important parameters to the user.

Generally, the deviations are scaled to the range [-1;1] where a value of –1 refers to the minimum value, 0 is the typical value (default) and 1 accounts for the maximum value of the model parameter. Note that the parameters have different priorities, such that not all combinations are possible.

Variations of the transconductance are modelled with the parameter `dgfs` which has a range of [-1;0].

The next parameter is `dRdson`, which enables the user to consider the maximum on-state resistance of the device. The allowed range is [0;1]. If `dRdson`≠0, entries in `dgfs` are overwritten.

Models have the attribute `dVth` to model threshold voltage deviations from the typical value. The allowed range is [-1;1]. If `dVth`≠0, entries in `dgfs` and `dRdson` are set to zero.

Variations in the capacitances are considered by assigning a value to `dC`, where values in the range [0;1] are possible.

Furthermore, level 3 models also have the parameter `dZth`, where values in the range [0;1] are allowed to vary between typical and guaranteed thermal performance.

The parameters of dual devices are accessible individually and named `dVth1`, `dVth2`, `dgfs1`, `dgf2`, etc.

The modelling of device performance deviations is a complex task since typically there is no one-to-one relation between a deviation in the manufacturing process and the variation in a particular device parameter. The use of the given optional parameters does therefore not account for all cases and might in special cases even result in performance that does not fulfil the specifications guaranteed by Infineon.

4 Typical Simulation Parameters

As PSpice was originally not designed for power electronics and highly non-linear components, the standard simulation parameters (Simulation Setup/Options) are often not suitable. In common, the following typical values facilitate convergence:

ABSTOL=	1nA	(maximum current accuracy)
CHGTOL=	1pC	(maximum charge accuracy)
ITL1=	150	(maximum number of iterations for DC analyses without initial conditions)
ITL2=	150	(maximum number of iterations for DC analyses with initial conditions)
ITL4=	500	(maximum number of iterations for transient analyses time steps)
RELTOL=	0.01	(relative accuracy of voltages and currents)

In many cases it is necessary to limit the step size for transient analyses. The circuit system contains many different time scales, where the automatic step control of the PSpice simulator sometimes disregards essential fast-time-scale information which eventually leads to convergence problems.

5 Modelling Contact Address

If you have further questions, feel free to contact us via our local sales offices, the internet (http://www.infineon.com) or email to simulate@infineon.com.