CSE 261: Digital Logic Design

Course Calendar: SPRING 2013

Note: Subject to Change

Week	Date	Topic
1	14 January	**Chapter 1** • Introduction to Course • Number-base systems ***HW1 Given Out***
	16 January	**Chapter 1** • Number-base systems
	18 January	**Chapter 1** • Number Base systems
2	21 January	**No class: Martin Luther King Day** ***HW2 Given Out***
	23 January	**Chapter 1** • Complements and Signed Binary numbers • Binary codes ***HW1 Due***
	25 January	**Chapter 2 – Boolean Algebra and Logic gates** • Basic Definitions • Theorems and properties
3	28 January	**Chapter 2 – Boolean Algebra and Logic gates** • Basic Definitions • Theorems and properties ***HW3 Given Out***
	30 January	**Chapter 2 – Boolean Algebra and Logic gates** • Boolean functions • SOP and POS forms ***HW2 Due***
	1 February	**Chapter 2 – Boolean Algebra and Logic gates** • Other Logic operations • Logic Gates
4	4 February	**Chapter 3 – Gate-level Minimization** • Map method • Two, three variable K-Maps ***HW4 Given Out***
	6 February	**Chapter 3 – Gate-level Minimization** • Three, Four variable K-Maps • POS form

		HW3 Due
	8 February	**Chapter 3 – Gate-level Minimization** • Five variable K-Maps • Handling Don't Care
5	11 February	***Exam 1: Chapters 1 and 2*** ***HW5 Given Out***
	13 February	**Chapter 3 – Gate-level Minimization** • NAND, NOR Implementations • Exclusive-OR Functions ***HW4 Due***
	15 February	**Chapter 3 – Gate-level Minimization** • Review
6	18 February	**Chapter 4 – Combinational Logic Analysis and Design** • Introduction • Analysis procedure • Example ***HW6 Given Out***
	20 February	**Chapter 4 – Combinational Logic Analysis and Design** • Design Procedure • Example ***HW5 Due***
	22 February	**Chapter 4 – Combinational Logic Analysis and Design** • Binary Adder • Subtractor
7	25 February	**Chapter 4 – Combinational Logic Analysis and Design** • Decimal Adder ***HW7 Given Out***
	27 February	**Chapter 4 – Combinational Logic Analysis and Design** • Comparators ***HW6 Due***
	1 March	**Chapter 4 – Combinational Logic Analysis and Design** • Decoders • Encoders
8	4 March	**Chapter 4 – Combinational Logic Analysis and Design** • Multiplexers • Multiplexer based Design ***HW8 Given Out***
	6 March	**Chapter 4 – Combinational Logic Analysis and Design** • Multiplexers • Multiplexer based Design ***HW7 Due***

	8 March	***Exam 2 – Chapters 3 and 4***
		SPRING BREAK, NO CLASSES
9	18 March	**Chapter 5 – Sequential Logic Analysis and Design** • Introduction • Storage Elements ***HW9 Given out***
	20 March	**Chapter 5 – Sequential Logic Analysis and Design** • Introduction • Storage Elements ***HW8 Due***
	22 March	**Chapter 5 – Sequential Logic Analysis and Design** • Analysis of Clocked Sequential Circuits
10	25 March	**Chapter 5 – Sequential Logic Analysis and Design** • Analysis of Clocked Sequential circuits ***HW10 Given Out***
	27 March	**Chapter 5 – Sequential Logic Analysis and Design** • Analysis of Clocked Sequential circuits ***HW9 Due***
	29 March	**Chapter 5 – Sequential Logic Analysis and Design** • Sequential System Design
11	1 April	**Chapter 5 – Sequential Logic Analysis and Design** • Sequential System Design ***HW11 Given Out***
	3 April	**Chapter 5 – Sequential Logic Analysis and Design** • Sequential System Design ***HW10 Due***
	5 April	**Design of a Central Processing Unit: Data path & control path** • Excerpts from Chapters 6, 7, and 8
12	8 April	**Design of a Central Processing Unit: Data path & control path** • Excerpts from Chapters 6, 7, and 8 ***HW12 Given Out***
	10 April	**Design of a Central Processing Unit: Data path & control path** • Excerpts from Chapters 6, 7, and 8 ***HW11 Due***
	12 April	**Design of a Central Processing Unit: Data path & control path** • Excerpts from Chapters 6, 7, and 8
13	15 April	***Exam 3 – Sequential Logic Analysis and Design*** ***HW13 Given Out***
	17 April	**Design of a Central Processing Unit: Data path & control path**

		• Excerpts from Chapters 6, 7, and 8 ***HW12 Due***
	19 April	**Design of a Central Processing Unit: Data path & control path** • Excerpts from Chapters 6, 7, and 8
14	22 April	**Design of a Central Processing Unit: Data path & control path** • Excerpts from Chapters 6, 7, and 8
	24 April	**Design of a Central Processing Unit: Data path & control path** • Excerpts from Chapters 6, 7, and 8 ***HW13 Due***
	26 April	**Design of a Central Processing Unit: Data path & control path** • Excerpts from Chapters 6, 7, and 8
15	29 April	***Last Class: Course Review***
	3 May	***Final Exam: 12:45-2:45 pm 111 Bowne Hall***