参考資料

計算の重さ

- 演算量
  - 一般的には浮動小数点演算（四則演算）を意味する
  - 四則演算の処理負荷（ハードウエア処理サイクル）は、演算の種類で異なる
  - 同じ計算式を実行する場合でも、ハードウエア（CPU）、ソフトウエア（コンパイラ）の選択やオプションにより演算量が異なる
    - 例えばFX10のあるオプション評価では．．．

      +, −, x　：　1 flop

      ÷　：　8 flops（単精度），13 flops（倍精度）

      abs()　：　1 flops
  - ユーザ申告モードではユーザ独自に計算の「重さ」を考慮した計算量を申告することも可能
    - 四則演算以外の複雑な演算を一つの計算単位として計上

HWPC

- プロセッサ固有のハードウエアパフォーマンスカウンタ（HWPC)について
- 京のHWPCとPAPIインタフェイス
- Intel XeonのHWPCとPAPIインタフェイス
- PAPI 高水準インタフェイスと低水準インタフェイス

ハードウエアカウンタについて

- 京・FX10 preset event

Available events and hardware information.

Vendor string and code : Sun (7)
Model string and code : Fujitsu SPARC64 IXfx (141)
CPU Revision : 0.000000
CPU Megahertz : 1650.000000
CPU Clock Megahertz : 1650
CPU's in this Node : 16
Nodes in this System : 1
Total CPU's : 16
Number Hardware Counters : 8
Max Multiplex Counters : 512

Name	Code	Deriv	Description (Note)
PAPI_L1_DCM	0x80000000	No	Level 1 data cache misses
PAPI_L1_ICM	0x80000001	No	Level 1 instruction cache misses
PAPI_L1_TCM	0x80000006	Yes	Level 1 cache misses
PAPI_L2_TCM	0x80000007	Yes	Level 2 cache misses
PAPI_CA_INV	0x8000000c	No	Requests for cache line invalidation
PAPI_CA_ITV	0x8000000d	No	Requests for cache line intervention
PAPI_TLB_DM	0x80000014	No	Data translation lookaside buffer misses
PAPI_TLB_IM	0x80000015	No	Instruction translation lookaside buffer misses
PAPI_TLB_TL	0x80000016	Yes	Total translation lookaside buffer misses
PAPI_MEM_SCY	0x80000022	No	Cycles Stalled Waiting for memory accesses
PAPI_STL_ICY	0x80000025	No	Cycles with no instruction issue
PAPI_FUL_ICY	0x80000026	No	Cycles with maximum instruction issue
PAPI_STL_CCY	0x80000027	Yes	Cycles with no instructions completed
PAPI_FUL_CCY	0x80000028	Yes	Cycles with maximum instructions completed
PAPI_HW_INT	0x80000029	No	Hardware interrupts
PAPI_BR_MSP	0x8000002e	No	Conditional branch instructions mispredicted
PAPI_BR_PRC	0x8000002f	Yes	Conditional branch instructions correctly predicted
PAPI_FMA_INS	0x80000030	Yes	FMA instructions completed
PAPI_TOT_IIS	0x80000031	Yes	Instructions issued
PAPI_TOT_INS	0x80000032	No	Instructions completed
PAPI_FP_INS	0x80000034	Yes	Floating point instructions
PAPI_LD_INS	0x80000035	Yes	Load instructions
PAPI_SR_INS	0x80000036	Yes	Store instructions
PAPI_BR_INS	0x80000037	No	Branch instructions
PAPI_VEC_INS	0x80000038	Yes	Vector/SIMD instructions
PAPI_TOT_CYC	0x8000003b	No	Total cycles
PAPI_LST_INS	0x8000003c	No	Load/store instructions completed
PAPI_L2_TCH	0x80000056	Yes	Level 2 total cache hits
PAPI_L2_TCA	0x80000059	Yes	Level 2 total cache accesses
PAPI_FP_OPS	0x80000066	Yes	Floating point operations

ハードウエアカウンタについて

- Intel Xeon E5 preset event

Hdw Threads per core : 1
Cores per Socket : 8
Sockets : 2
NUMA Nodes : 2
CPUs per Node : 8
Total CPUs : 16
Running in a VM : no
Number Hardware Counters : 11
Max Multiplex Counters : 32

Name Code Deriv Description (Note)
PAPI_L1_DCM 0x80000000 No Level 1 data cache misses
PAPI_L1_ICM 0x80000001 No Level 1 instruction cache misses
PAPI_L2_DCM 0x80000002 Yes Level 2 data cache misses
PAPI_L2_ICM 0x80000003 No Level 2 instruction cache misses
PAPI_L1_TCM 0x80000006 Yes Level 1 cache misses
PAPI_L2_TCM 0x80000007 No Level 2 cache misses
PAPI_L3_TCM 0x80000008 No Level 3 cache misses
PAPI_TLB_DM 0x80000014 Yes Data translation lookaside buffer misses
PAPI_TLB_IM 0x80000015 No Instruction TLBmisses
PAPI_L1_LDM 0x80000017 No Level 1 load misses
PAPI_L1_STM 0x80000018 No Level 1 store misses
PAPI_L2_STM 0x8000001a No Level 2 store misses
PAPI_STL_ICY 0x80000025 No Cycles with no instruction issue
PAPI_BR_UCN 0x8000002a Yes Unconditional branch instructions
PAPI_BR_CN 0x8000002b No Conditional branch instructions
PAPI_BR_TKN 0x8000002c Yes Conditional branch taken
PAPI_BR_NTK 0x8000002d No Conditional branch not taken
PAPI_BR_MSP 0x8000002e No Conditional branch mispredicted
PAPI_BR_PRC 0x8000002f Yes Conditional branch correctly predicted
PAPI_TOT_INS 0x80000032 No Instructions completed
PAPI_FP_INS 0x80000034 Yes Floating point instructions
PAPI_LD_INS 0x80000035 No Load instructions
PAPI_SR_INS 0x80000036 No Store instructions
PAPI_BR_INS 0x80000037 No Branch instructions
PAPI_TOT_CYC 0x8000003b No Total cycles
PAPI_L2_DCH 0x8000003f Yes Level 2 data cache hits
PAPI_L2_DCA 0x80000041 No Level 2 data cache accesses
PAPI_L3_DCA 0x80000042 Yes Level 3 data cache accesses
PAPI_L2_DCR 0x80000044 No Level 2 data cache reads
PAPI_L3_DCR 0x80000045 No Level 3 data cache reads
PAPI_L2_DCW 0x80000047 No Level 2 data cache writes
PAPI_L3_DCW 0x80000048 No Level 3 data cache writes
PAPI_L2_ICH 0x8000004a No Level 2 instruction cache hits
PAPI_L2_ICA 0x8000004d No Level 2 instruction cache accesses
PAPI_L3_ICA 0x8000004e No Level 3 instruction cache accesses
PAPI_L2_ICR 0x80000050 No Level 2 instruction cache reads
PAPI_L3_ICR 0x80000051 No Level 3 instruction cache reads
PAPI_L2_TCA 0x80000059 Yes Level 2 total cache accesses
PAPI_L3_TCA 0x8000005a No Level 3 total cache accesses
PAPI_L2_TCR 0x8000005c Yes Level 2 total cache reads
PAPI_L3_TCR 0x8000005d Yes Level 3 total cache reads
PAPI_L2_TCW 0x8000005f No Level 2 total cache writes
PAPI_L3_TCW 0x80000060 No Level 3 total cache writes
PAPI_FDV_INS 0x80000063 No Floating point divide instructions
PAPI_FP_OPS 0x80000066 Yes Floating point operations
PAPI_SP_OPS 0x80000067 Yes Floating point operations; optimized to count scaled single precision vector operations
PAPI_DP_OPS 0x80000068 Yes Floating point operations; optimized to count scaled double precision vector operations
PAPI_VEC_SP 0x80000069 Yes Single precision vector/SIMD instructions
PAPI_VEC_DP 0x8000006a Yes Double precision vector/SIMD instructions
PAPI_REF_CYC 0x8000006b No Reference clock cycles

ハードウエアカウンタ Xeon E5 preset とnative

Intel Xeon E5ではPAPI_FP_OPSとPAPI_FP_INSは同じ内容を表示

```
Event name:                    PAPI_FP_OPS
Event Code:                    0x80000066
Number of Native Events:       2
Short Description:            |FP instructions|
Long Description:             |Floating point instructions|
Developer's Notes:            ||
Derived Type:                 |DERIVED_ADD|
Postfix Processing String:    ||
 Native Code[0]: 0x4000001c |FP_COMP_OPS_EXE:SSE_SCALAR_DOUBLE|
 Native Event Description: |Counts number of floating point events, masks:Number of SSE double precision FP scalar uops executed|

 Native Code[1]: 0x4000001d |FP_COMP_OPS_EXE:SSE_FP_SCALAR_SINGLE|
 Native Event Description: |Counts number of floating point events, masks:Number of SSE single precision FP scalar uops executed|


$ papi_avail -e  PAPI_DP_OPS
Event name:                    PAPI_DP_OPS
Event Code:                    0x80000068
Number of Native Events:       3
Short Description:            |DP operations|
Long Description:             |Floating point operations; optimized to count scaled double precision vector operations|

 Native Code[0]: 0x4000001c |FP_COMP_OPS_EXE:SSE_SCALAR_DOUBLE|
 Native Event Description: |Counts number of floating point events, masks:Number of SSE double precision FP scalar uops executed|

 Native Code[1]: 0x40000020 |FP_COMP_OPS_EXE:SSE_FP_PACKED_DOUBLE|
 Native Event Description: |Counts number of floating point events, masks:Number of SSE double precision FP packed uops executed|

 Native Code[2]: 0x40000021 |SIMD_FP_256:PACKED_DOUBLE|
 Native Event Description: |Counts 256-bit packed floating point instructions, masks:Counts 256-bit packed double-precision|


$ papi_avail -e  PAPI_VEC_DP
Event name:                    PAPI_VEC_DP
Event Code:                    0x8000006a
Number of Native Events:       2
Short Description:            |DP Vector/SIMD instr|
Long Description:             |Double precision vector/SIMD instructions|

 Native Code[0]: 0x40000020 |FP_COMP_OPS_EXE:SSE_FP_PACKED_DOUBLE|
 Native Code[1]: 0x40000021 |SIMD_FP_256:PACKED_DOUBLE|
```

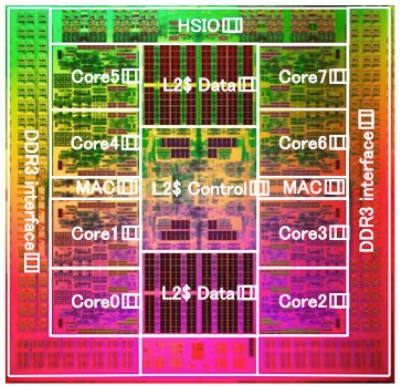
ハードウエアカウンタ SPARC64 VIIIfx preset とnative

```
$ papi_avail -e PAPI_FP_OPS

Event name:                   PAPI_FP_OPS
Number of Native Events:      4
Short Description:           |FP operations|
Long Description:            |Floating point operations|
Derived Type:                |DERIVED_POSTFIX|

 Native Code[0]: 0x40000010  |FLOATING_INSTRUCTIONS|
 Native Event Description:   |Counts the number of committed floating-point operation instructions.|

 Native Code[1]: 0x40000011  |FMA_INSTRUCTIONS|
 Native Event Description:   |Counts the number of committed floating-point Multiply-and-Add operation instructions.|

 Native Code[2]: 0x40000008  |SIMD_FLOATING_INSTRUCTIONS|
 Native Event Description:   |Counts the number of committed floating-point SIMD instructions of one operation in SIMD.|

 Native Code[3]: 0x40000009  |SIMD_FMA_INSTRUCTIONS|
 Native Event Description:   |Counts the number of committed floating-point SIMD instructions of two operation in SIMD.|
```

「京」コンピュータプロセッサ ・ノード

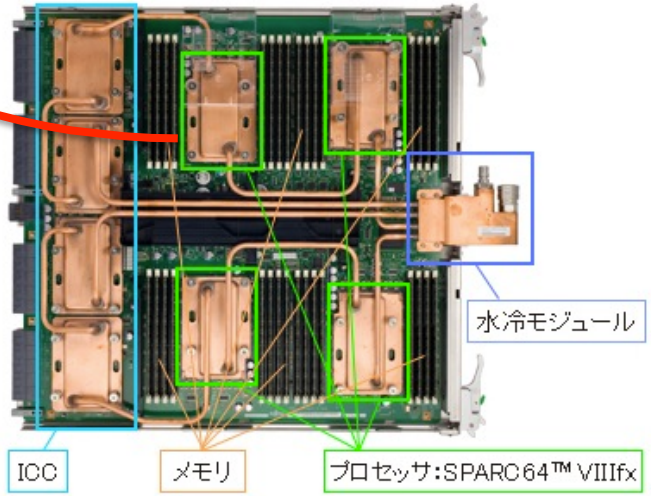
CPU : SPARC64 VIIIfxプロセッサ

SPARC64™VIIIfx



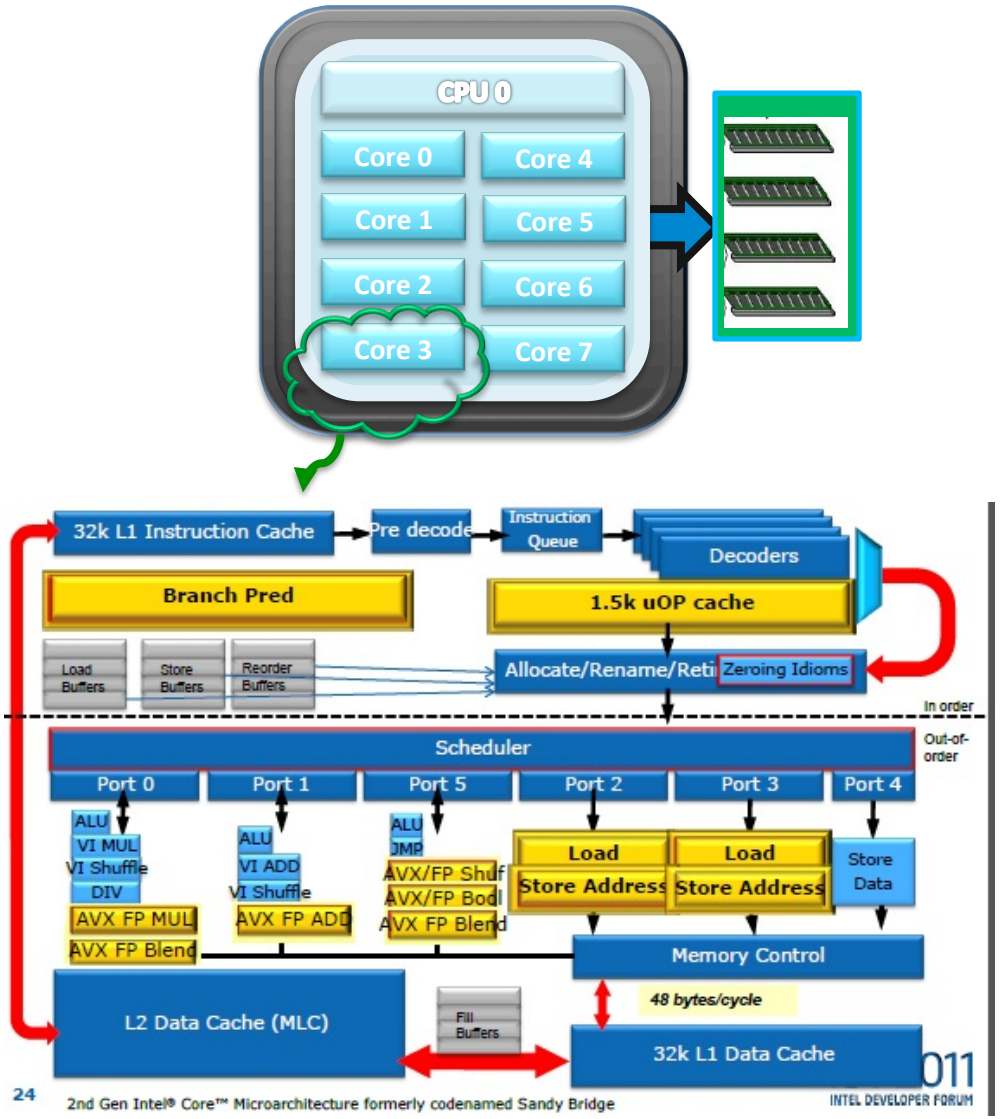
- **Specification**
  - 8 Cores
  - 6 MB Shared L2 Cache
  - FMA × 4 (2 SIMD)/core
  - 256 (64bit) DP Reg. /core
  - 2GHz
- **Peak Performance**
  - FP Performance 128GFlop/s
  - Memory Bandwidth 64GB/s
- **Power Consumption**
  - 58W (LINPACK Max)

Node : SPARC64 VIIIfx x 1
4 nodes/ board



Intel Xeon E5プロセッサ・ノード

CPU : Xeon E5-2670



node: E5-2670 x 2, QPI, PCIe, …