Class:	CPE-300L	Semester:	Spring 2020

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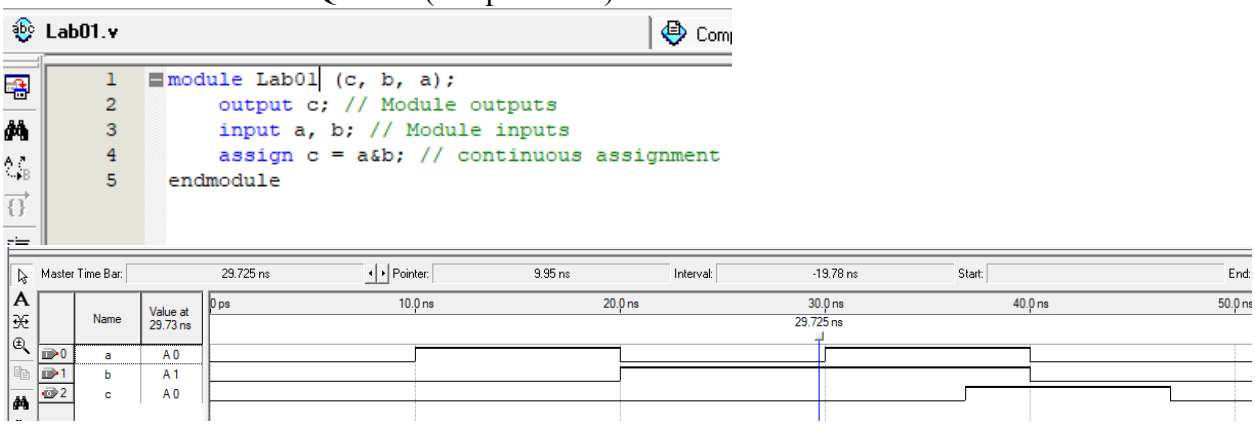
Instructor's comments:

1. Introduction / Theory of Operation

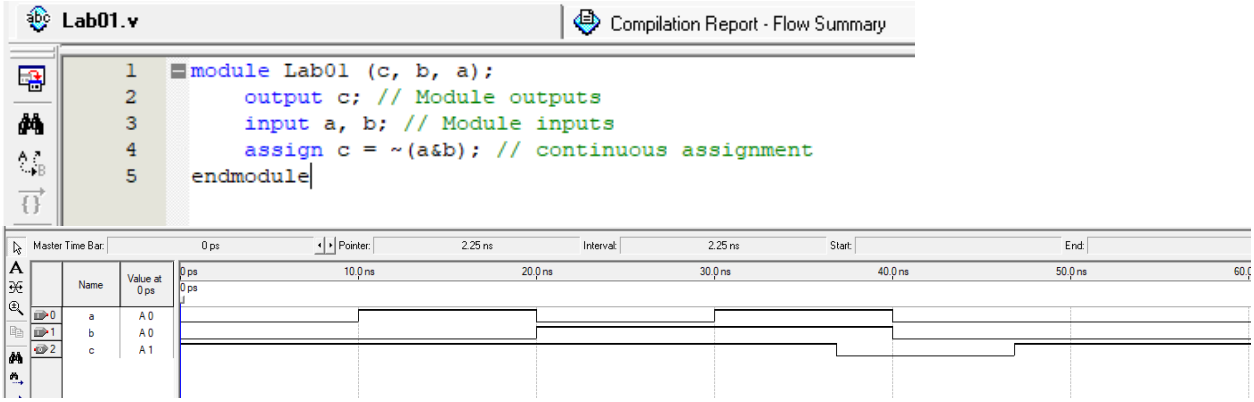
- Hardware Description Language (HDL) is a computer language for the creator/user to describe and understand the structure and functionalities of hardware and electronic circuits. 2 types of HDL that are used are Verilog and VHDL.

2. Experiments Results

1. Waveform from Quartus (2-input AND)



2. Verilog Code and Waveform (2-input AND w/Inverting Output)



Questions

1. What is Register Transfer Level (RTL)?
   - Register Transfer Level is a circuit design which models the flow of data between hardware registers and logical operations on the data.

2. What is the difference between HDL and general purposes languages(C/C++)?
   - HDL is a hardware description language which is used to implement only on hardware circuitry, while C/C++ is a mix of high-level language and assembly language. C uses only logical/algorithmic thinking while HDL uses hardware circuit knowledge.

3. Encountered Problems

- Problems that occurred was that the software Quartus II 7.1 (64-bit) kept on crashing. In order to solve the encountered problem was to change to Quartus II 7.1 (32-bit) which allowed us to finish experiment-1 without any problems.

4. Summary

- Within this lab we used the software Quartus II 7.1 (32-bit). We were instructed to create 2 modules in Verilog HDL code, one of them being a 2 input AND gate and the other being a 2 input AND gate with inverting output. We simulated the Verilog HDL code and created waveforms in order to show proof of completion.

5. Conclusions

- To conclude experiment-1, we learned about what Hardware Description Language is and the basic syntax of Verilog HDL. We learned how to create modules to perform gate-logical operations (AND gate), and how to simulate and create waveforms to verify our Verilog HDL code.