CPE 300L
DIGITAL SYSTEM ARCHITECTURE AND DESIGN LABORATORY

LABORATORY 6
DESIGN, SIMULATION AND TESTING OF THE SUMMATION ALGORITHM ON THE GENERAL DATAPATH I

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OBJECTIVE

Learn on implementing the general datapath: implement the datapath and its component.

INTRODUCTION

Simple computer architecture can be decomposed into a) datapath for executing operations b) control unit for controlling datapath operations. A datapath is specified by a set of its components, i.e., combinational components for performing microoperations and moving data to and from registers, where data on which operations are performed are stored. For a large number of registers, the latter can be organized into a register file with shared ports of access for reading and writing. The datapath is to be supplied with a conditional logic for implementing conditional statements. Generally, the datapath can contain also on-board memory and interface logic.

SUMMATION CIRCUIT

Summation Algorithm:

```
1 sum = 0
2 INPUT n
3 WHILE (n ≠ 0) {
4     sum = sum + n
5     n = n - 1
6 }
7 OUTPUT sum
```

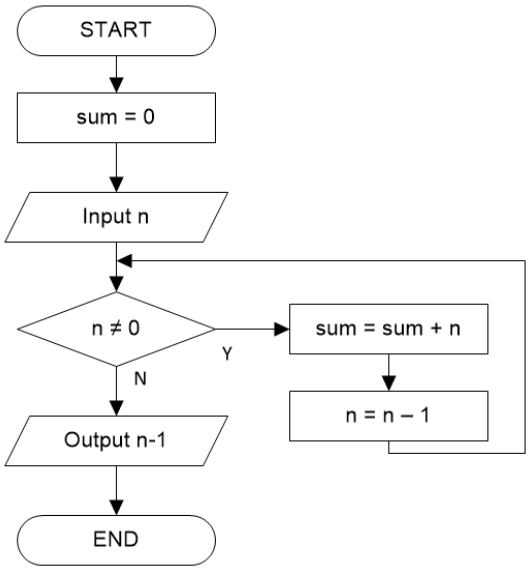
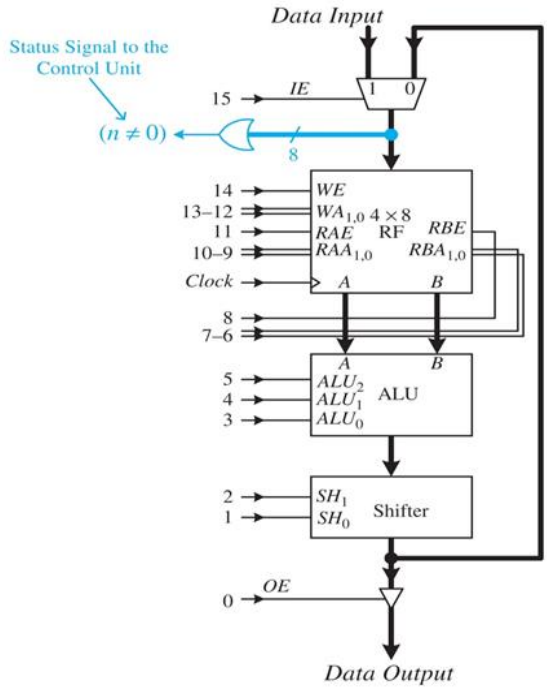


Fig. 1. Summation algorithm



ALU_2	ALU_1	ALU_0	Operation
0	0	0	Pass through A
0	0	1	A AND B
0	1	0	A OR B
0	1	1	NOT A
1	0	0	$A + B$
1	0	1	$A - B$
1	1	0	$A + 1$
1	1	1	$A - 1$

(b)

SH_1	SH_0	Operation
0	0	Pass through
0	1	Shift left and fill with 0
1	0	Shift right and fill with 0
1	1	Rotate right

Fig. 2. Datapath with ALU

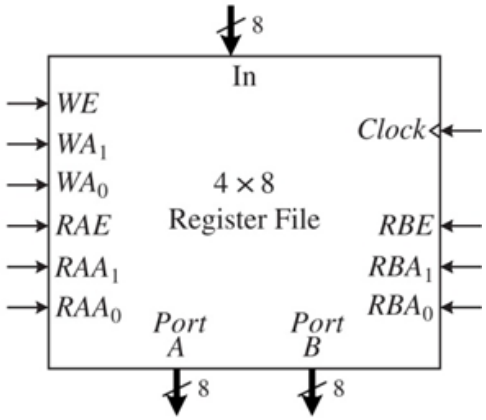


Fig. 3. Register file 4x8

LAB DELIVERIES

PRELAB DELIVERIES

1. Understand the objective of the summation algorithm and explain how the algorithm works.
2. Identify the components in the general datapath from Fig 2 and explain the use of each component with respect to the summation algorithm?
3. What are all the input and output signals shown in Fig 2 associated with each block, explain all of them.
4. Write a Verilog code for the ALU described in Fig 2b and verify using the Modelsim.

LAB EXPERIMENTS

Demonstrate all the experiments to TA.

1. Implementation of the Datapath I

Write a Verilog code for all the components identified from prelab 2. Verify the operation of each component in Modelsim.

2. Implementation of the Datapath II

Create a module called DP with all the signal and stich the components verified in experiment 1 as a complete datapath module.

POSTLAB REPORT

Include the following elements in your postlab report:

<table>
<tr><th>Section</th><th colspan="2">Element</th></tr>
<tr><td>1</td><td colspan="2">Theory of operation
Include a brief description of every element and phenomenon that appears during the experiments.
a. Describe how the digital circuit design can be tested
b. What is the datapath in general? Provide an example.</td></tr>
<tr><td>2</td><td colspan="2">Prelab report</td></tr>
<tr><td rowspan="4">3</td><td colspan="2">Results of the experiments</td></tr>
<tr><td>Experiment</td><td>Experiment Results</td></tr>
<tr><td>1</td><td>Verilog code, testbenches and waveforms</td></tr>
<tr><td>2</td><td>Verilog Code</td></tr>
<tr><td rowspan="3">4</td><td colspan="2">Answer the questions</td></tr>
<tr><td>Question no.</td><td>Question</td></tr>
<tr><td>1</td><td>What are the control words for the datapath?</td></tr>
<tr><td>5</td><td colspan="2">Conclusions
Write down your conclusions, things learned, problems encountered during the lab and how they were solved, etc.</td></tr>
</table>