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Points		Document author:	Brysen Kokubun
		Author's email:	Brysenkokubun96@gmail.com
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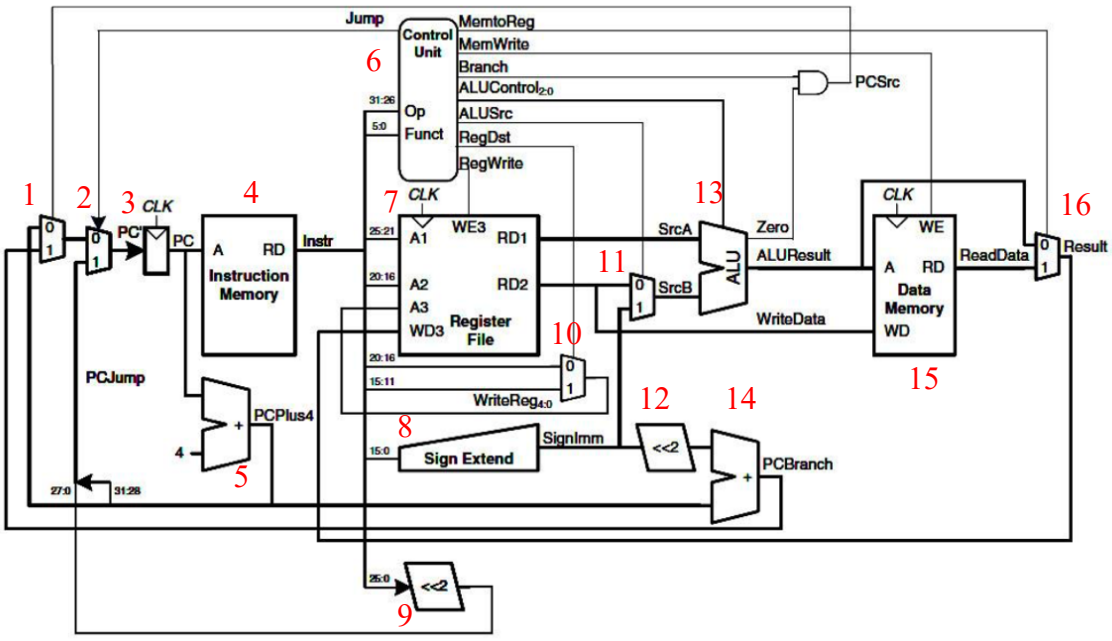
Instructor's comments:

Introduction / Theory of operation

- For this lab experiment we will be learning on how to design a CPU by implementing a single cycle implementation of limited subset of MIPS instructions.

Prelab main content

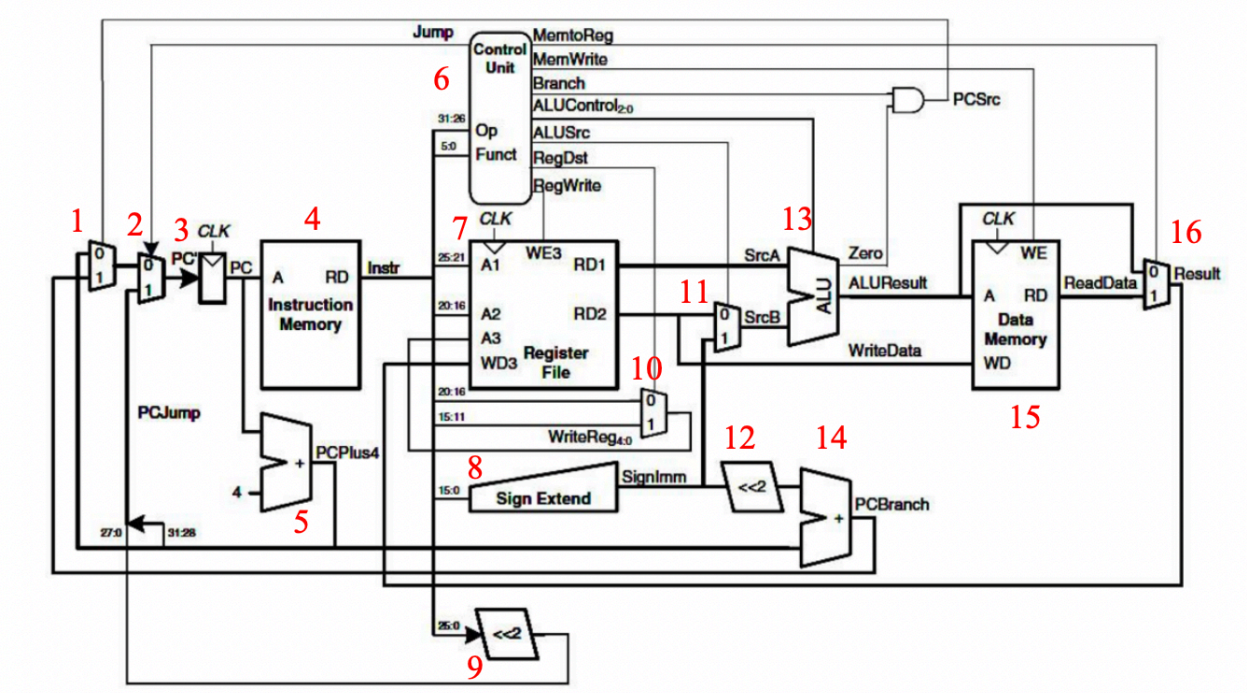
1. Describe, what is the function of each block (there are 16 blocks) in Fig.1?



1) Mux_1: Mux selection from PCSrc output for Mux_2
2) Mux_2: Mux selection from Jump output for PC'
3) Flip_flop: Program counter
4) Instruction memory: for Register destination of Program counter
5) Adder: Program counter + 4
6) Control Unit: Controls the operations of the other components
7) Register file: Addresses/write destinations/write enable/read destinations
8) Sign Extend: Address offset for I-type, destination/shift amount/function for R-type
9) Shifter: shifts 2 bits left
10) Mux_3: Mux selection from RegDst output for register file A3
11) Mux_4: Mux selection from ALUSrc output for ALU input SrcB

12) Shifter: shifts 2 bits left
13) ALU: performs arithmetic operations
14) Adder: (PC+4) + (Sign extend shifted 2 bits left)
15) Data Memory: write data/aluResult to Read data or pass through to Mux_5
16) Mux_5: Mux selection from memtoReg output for register file WD3

2. Study the given code and write the name of module that generates each block (there are 16 blocks) in Fig.1.



1) Module mux2.v
2) Module mux2.v
3) Module flopr.v
4) Module imem.v
5) Module adder.v
6) Module controller.v
7) Module regfile.v
8) Module signext.v
9) Module sl2.v
10) Module mux2.v
11) Module mux2.v
12) Module sl2.v
13) Module alu.v
14) Module adder.v
15) Module dmem.v
16) Module mux2.v