Class:	CPE-300L	Semester:	Spring 2020

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		Document topic:	Prelab 5

Instructor's comments:

Introduction / Theory of operation

- For this lab experiment we will be learning about Finite State Machines. There are two types of machines that we will be implementing, Mealy and Moore machines. Mealy machines outputs are dependent on present inputs, and current state while Moore machines outputs are dependent only on machines current state. This lab will teach us about FSM components, design and how to implement those designs as waveforms and on DE2 boards.

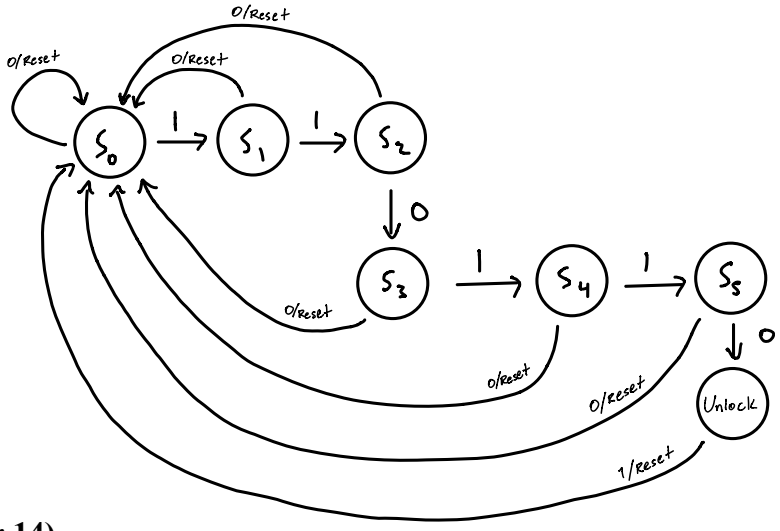
Prelab main content

1. What is a Finite State Machine? What are the components in a FSM?

- A Finite State Machine is a computation model (software/hardware) that is used to simulate sequential logic. Also, the FSM can only be in one state at any given time. The components in a FSM are sets of states, transitions between states, and actions associated with each transition (entering, exiting or remaining in a state).

2. Digital lock design

Unlock = "110110"



3. Read modeling FSM (Chapter 14)

Introduction to FSM

State machine or FSM are the heart of any digital design, of course counter is a simple form of FSM. When I was learning Verilog, I use to wonder "How do I code FSM in Verilog" and "What is the best way to code it". I will try to answer the first part of the question below and second part of the question could be found in the tidbits section.