CPE 300L
Digital System Architecture and Design Laboratory

Laboratory 5
Finite State Machine Design

Department of Electrical and Computer Engineering
University of Nevada, Las Vegas

Objective

Learn on various implementations of FSM design and implementation.

Introduction

In this lab we will design a finite state machine. Following are the example:

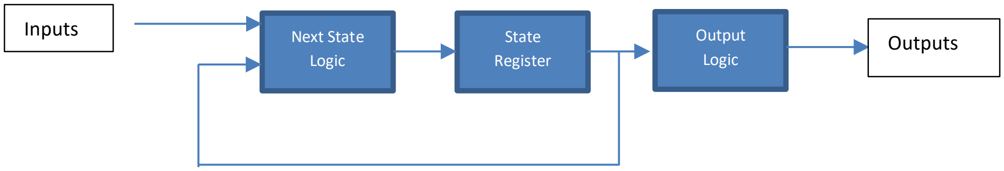


Fig1. Moore Machine

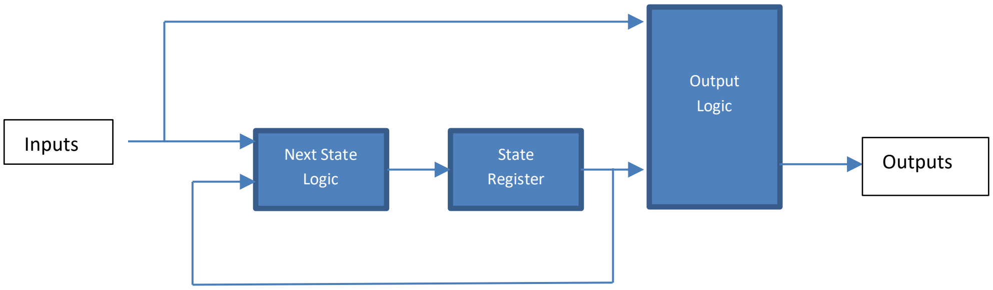


Fig2. Mealy Machine

Modeling in Verilog includes finding a way to model or encode each state, way to keep track of the current state, way for transitioning state to state, way to generate output based on the current state.

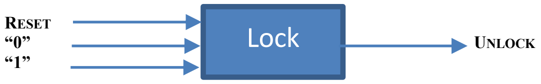
There are multiple ways of modeling a FSM, the one kind that we will discuss in this lab is two always block style with combinational outputs. In fig 1 and fig 2, next state logic is used in one always block with combinational logic while the state registers and output logic will be defined in another always block with sequential logic.

```
/*
Skeleton Verilog module for a FSM
*/

module module_name(input clock, input reset, input input_data, output reg output_data);

reg [1:0]state;   //adjust the width of state variable as needed
//declare any additional signals here like nextstate

//use non blocking assignment (<=) in synchronous always block; this is a sequential part
always @ (posedge CLK) begin

end

//use blocking assignment. (=) in next state and output logic block; this is a combinational part
always @ (*) begin

end

endmodule
```

LAB DELIVERIES

PRELAB

1. What is a Finite State Machine? What are the components in a FSM?
2. Our objective: To design a digital lock



Assume the lock code is "110110", if entered correctly the lock will unlock else the lock will stay locked.

Design a state transition diagram for the digital lock described above. Overlapping sequence is not allowed.

3. Read modeling FSM (chapter 14) in the link given below:
http://eelabs.faculty.unlv.edu/docs/guides/Verilog_Tutorial.pdf

Lab Experiments

1. Write a FSM code for the digital lock and upload your design to the DE2 board and verify the operation. 7 seg display should show “L” or “U” for locked and unlock status. You may have a clock, input button for 0, input button for 1, enter button, reset button, led status for lock (red) and unlock (green) and a status in 7 seg.

2. Model the FSM machine defined as follows:

PS	NS		Z	
	X=0	X=1	X=0	X=1
S_0	S_1	S_2	1	0
S_1	S_3	S_4	1	0
S_2	S_4	S_4	0	1
S_3	S_5	S_5	0	1
S_4	S_5	S_6	1	0
S_5	S_0	S_0	0	1
S_6	S_0	–	1	–

Use **always** block to represent the combinational part of the circuit and generate the next state information and output. Use another **always** block to model the state register. Verify your design in a Modelsim with a testbench.

3. Design a serial parity detector. Parity indicates whether the number of “1”s is odd or even. Eg: The output “1” can indicate odd parity and “0” can indicate even parity. Here, input is serial and we get continuous stream of input. Output is also a stream and generates parity continuously. Your design will have a input , clk , reset and output.

Design and verify with the testbench using Modelsim.

Postlab Report:

Include the following elements in your postlab report:

<table>
<tr><th>Section</th><th colspan="2">Element</th></tr>
<tr><td>1</td><td colspan="2">Theory of operation
<i>Include a brief description of every element and phenomenon that appears during the experiments.</i>
<i>a. What are two types of FSMs? Explain in detail.</i>
<i>b. Write few sentences: explain how you approach designing a FSMs.</i></td></tr>
<tr><td>2</td><td colspan="2">Prelab report</td></tr>
<tr><td rowspan="5">3</td><td colspan="2">Results of the experiments</td></tr>
<tr><th>Experiment</th><th>Experiment Results</th></tr>
<tr><td>1</td><td>Verilog code and a picture of DE2 board</td></tr>
<tr><td>2</td><td>Verilog code , testbench and waveform</td></tr>
<tr><td>3</td><td>Verilog code , testbench and waveform</td></tr>
<tr><td>4</td><td colspan="2">Answer the questions</td></tr>
</table>

	Question no.	**Question**
	1	What is the difference between mealy and moore machine?
	2	What is encoding style in a FSM?
	3	What is a combinational section and sequential section in a FSM design used for?
5	Conclusions *Write down your conclusions, things learned, problems encountered during the lab and how they were solved, etc.*	