CPE 300L
DIGITAL SYSTEM ARCHITECTURE AND DESIGN LABORATORY

LABORATORY 7
DESIGN, SIMULATION AND TESTING OF THE SUMMATION ALGORITHM ON THE GENERAL DATAPATH II

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
UNIVERSITY OF NEVADA, LAS VEGAS

OBJECTIVE

Learn on implementing the general datapath: design a control unit for implementing a given algorithm. Design the testbench and use it to test and debug the circuit.

INTRODUCTION

Simple computer architecture can be decomposed into a) datapath for executing operations b) control unit for controlling datapath operations. A datapath is specified by a set of its components, i.e., combinational components for performing microoperations and moving data to and from registers, where data on which operations are performed are stored. For a large number of registers, the latter can be organized into a register file with shared ports of access for reading and writing. The datapath is to be supplied with a conditional logic for implementing conditional statements. Generally, the datapath can contain also on-board memory and interface logic.

SUMMATION CIRCUIT

Summation Algorithm:

```
1 sum = 0
2 INPUT n
3 WHILE (n ≠ 0) {
4     sum = sum + n
5     n = n - 1
6 }
7 OUTPUT sum
```

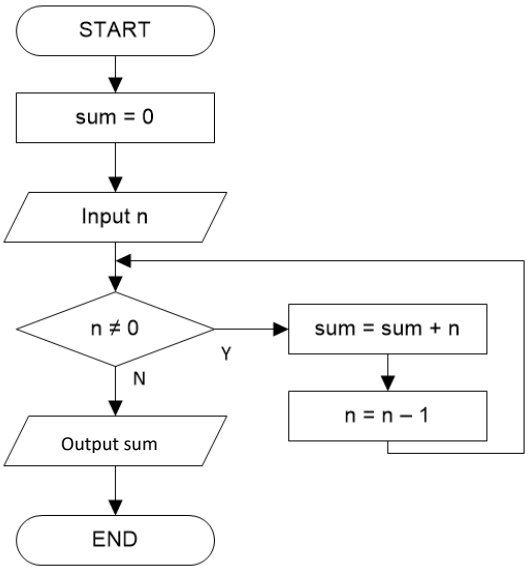
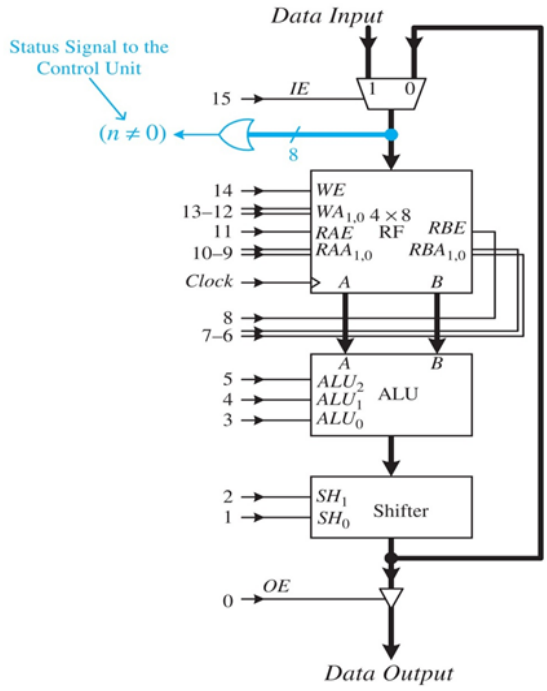


Fig. 2. Summation algorithm



ALU_2	ALU_1	ALU_0	Operation
0	0	0	Pass through A
0	0	1	A AND B
0	1	0	A OR B
0	1	1	NOT A
1	0	0	$A + B$
1	0	1	$A - B$
1	1	0	$A + 1$
1	1	1	$A - 1$

(b)

SH_1	SH_0	Operation
0	0	Pass through
0	1	Shift left and fill with 0
1	0	Shift right and fill with 0
1	1	Rotate right

Fig. 3. Datapath with ALU

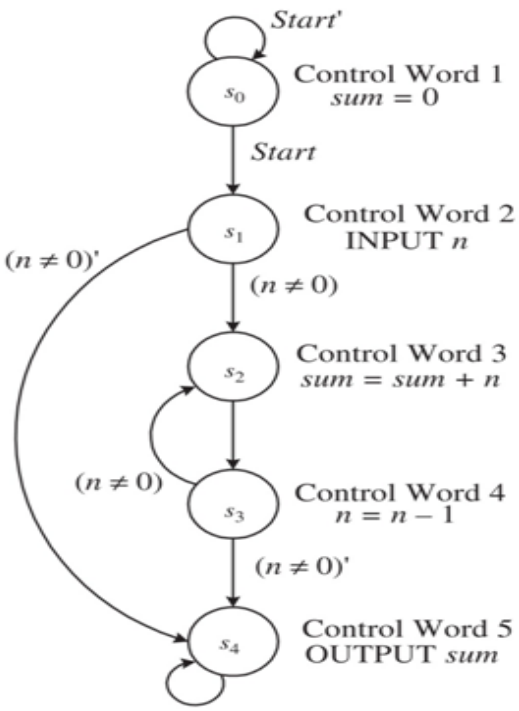


Fig. 4. State graph of the control unit

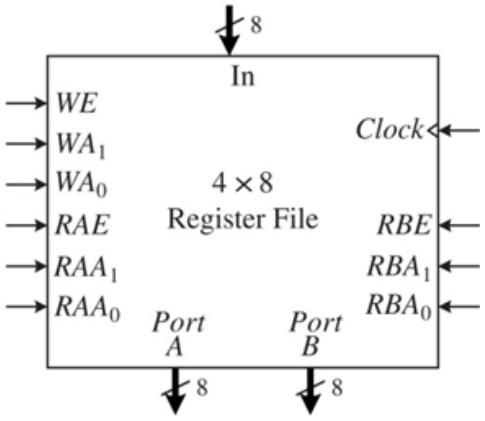


Fig. 5. Register file 4x8

Control words to generate and sum the numbers from n down to 1

Control Word	Instruction	IE 15	WE 14	$WA_{1,0}$ 13–12	RAE 11	$RAA_{1,0}$ 10–9	RBE 8	$RBA_{1,0}$ 7–6	$ALU_{2,1,0}$ 5–3	$SH_{1,0}$ 2–1	OE 0
1	$sum = 0$	0	1	00	1	00	1	00	101 (subtract)	00	0
2	INPUT n	1	1	01	0	××	0	××	× × ×	××	0
3	$sum = sum + n$	0	1	00	1	00	1	01	100 (add)	00	0
4	$n = n - 1$	0	1	01	1	01	0	××	111 (decrement)	00	0
5	OUTPUT sum	×	0	××	1	00	0	××	000 (pass)	00	1

Fig. 6. Control words

Control Unit Design:

Control Unit design is basically an FSM implementation of a state graph shown in Fig. 4. You can have a CLK, START, RESTART and any other signal like (**n ≠ 0)** as an input signal and all the signals shown in Fig. 2 in datapath are the output signals generated from the CU.

In this problem (Summation Algorithm), **n ≠ 0** is an important signal which is extensively used in the state graph, this is a signal that is used in a control unit. This signal (**n ≠ 0)** should be generated in a datapath module using the output of the mux which is shown in blue color in Fig. 4. The signal (**n ≠ 0)** is used as an input to a control unit module and an output from a datapath module. Similarly, any other application specific signal can be generated using any component from the datapath like the signal **n ≠ 0** in this example.

The important step in designing the CU is to work with state graph and control words together. Each state in a state graph from Fig. 4 is associated with the control word from Fig 6. Remember the two always block from FSM lab, one is sequential which will assign the next state to a present state and another combinational that will generate the next state based on the input signals (START, RESTART and n ≠ 0). All the control signals shown in Fig. 2 in datapath which is an output signals from the CU can be modeled using the continuous assignment statement. For example:

assign IE = (PresentState == S1);

if you look at signal ***IE***, it is ***1'b1*** only on control word 2 i.e., ***INPUT n*** (Fig. 6) which is executed in state ***S1*** from state graph (Fig. 4).

Similarly, generate all the necessary output control signal from the control unit module.

You can use parameter for making your code easy to read e.g.

parameter S0 = 3'b000;

parameter S1 = 3'b001;

LAB DELIVERIES

PRELAB

1. Implement a state graph for the summation algorithm and verify it with fig 4. Is it possible to have a different state graph than the one mentioned in fig 4?

2. Implement the control words for the state graph that you created in 1 and verify it with fig 6. Is it possible to have a different control words than the one mentioned in fig 6?

LAB EXPERIMENTS

Demonstrate all the experiments to TA.

1. Implementation of control unit for a general datapath

Implement the Verilog code for the control unit with the help of fig 4 and fig 6. Remember: Control unit is an FSM.

2. Top-level module

Create a top-level module and use the datapath code from lab 6 and control unit code from experiment 1 to create a complete datapath code.

3. Testbench

Write a testbench to check the correctness of your design and verify using Modelsim. Your testbench should test the summation algorithm for a given input N.

4. Datapath on DE2

Upload your design in DE2 board and verify the operation. Result of the summation algorithm should be displayed using the 7 segment display.

POSTLAB REPORT

Include the following elements in your postlab report:

<table>
<tr><th>Section</th><th colspan="2">Element</th></tr>
<tr><td>1</td><td colspan="2">Theory of operation
Include a brief description of every element and phenomenon that appears during the experiments.
a. Describe how the control unit is designed.
b. Explain all the control signal that you encountered.</td></tr>
<tr><td>2</td><td colspan="2">Prelab report</td></tr>
<tr><td rowspan="5">3</td><td colspan="2">Results of the experiments</td></tr>
<tr><td>Experiment</td><td>Experiment Results</td></tr>
<tr><td>1</td><td>Verilog code</td></tr>
<tr><td>2</td><td>Verilog code</td></tr>
<tr><td>3</td><td>Testbench Code
Testbench Result: waveform</td></tr>
<tr><td>4</td><td>Picture of DE2 with design implemented</td></tr>
<tr><td rowspan="3">4</td><td colspan="2">Answer the questions</td></tr>
<tr><td>Question no.</td><td>Question</td></tr>
<tr><td>1</td><td>What is a control unit and what role does it play in the implementation of the summation algorithm?</td></tr>
<tr><td>5</td><td colspan="2">Conclusions
Write down your conclusions, things learned, problems encountered during the lab and how they were solved, etc.</td></tr>
</table>