CPE 300L
DIGITAL SYSTEM ARCHITECTURE AND DESIGN LABORATORY

LABORATORY 8
GENERAL DATAPATH III
TIMEQUEST AND MEMORY INITIALIZATION

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
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OBJECTIVE

Implement a general datapath for a given algorithm.

Gain experience in setting up the timing constraints and obtain timing information for a logic circuit.

Algorithm:

Following algorithm calculates the greatest common divisor (GCD) of two natural numbers a and b. GCD of a and b is the largest natural number that divides both a and b with a zero remainder.

```
input a,b
while a ≠ b
      if a > b
            a = a - b
      else
            b = b - a
output a
```

LAB DELIVERIES

PRELAB

1. TimeQuest

Complete the TimeQuest analyzer tutorial:
https://faculty.unlv.edu/eelabs/docs/guides/Altera_Timequest.pdf

2. Memory initialization in Quartus II

Create the .mif file using the following tutorial:
https://faculty.unlv.edu/eelabs/docs/guides/Memory_initialization_tutorial.pdf

3. Graphs

Create a flowchart, state graph and control words for the GCD algorithm given above to implement in the general datapath.

PRELAB DELIVERABLES:

1. Screenshot of the timing report before and after setting up timing constraints.
3. Flowchart, state graph and control words for the algorithm.

LAB EXPERIMENTS

Demonstrate each experiment to TA.

1. General datapath

Implement the general datapath design for the GCD algorithm shown above, you can use the general datapath code from lab 7. Implement the testbench and verify in Modelsim before testing on the DE2. Result should be displayed on the 7 segment display.

2. Timequest analysis

Perform the time quest analysis on experiment 1 and obtain the report on the cycle time.

POSTLAB REPORT

Include the following elements in your postlab report:

<table>
<tr><th>Section</th><th colspan="2">Element</th></tr>
<tr><td>1</td><td colspan="2">Theory of operation
Include a brief description of every element and phenomenon that appears during the experiments.
a. What is a slack in time quest analysis?
b. Why is it important to consider timing analysis in a digital circuit?</td></tr>
<tr><td>2</td><td colspan="2">Prelab report</td></tr>
<tr><td rowspan="3">3</td><td colspan="2">Results of the experiments</td></tr>
<tr><td>Experiment</td><td>Experiment Results</td></tr>
<tr><td>1</td><td>Verilog Code, Testbench, Waveform, Picture of DE2</td></tr>
<tr><td rowspan="3">4</td><td>2</td><td>Screenshots of the timing analysis</td></tr>
<tr><td colspan="2">Answer the questions</td></tr>
<tr><td>Question no.</td><td>Question</td></tr>
<tr><td></td><td>1</td><td>Find out the information about the TimeQuest analyzer. Write 2 paragraphs about this tool.</td></tr>
<tr><td></td><td>2</td><td>List the purposes of initializing the memory in Quartus II</td></tr>
<tr><td>5</td><td colspan="2">Conclusions
Write down your conclusions, things learned, problems encountered during the lab and how they were solved, etc.</td></tr>
</table>

REFERENCES

1. *Memory Initialization tutorial:*
https://faculty.unlv.edu/eelabs/docs/guides/Memory_initialization_tutorial.pdf

2. *Using TimeQuest Timing Analyzer*, Altera.
https://faculty.unlv.edu/eelabs/docs/guides/Altera_Timequest.pdf