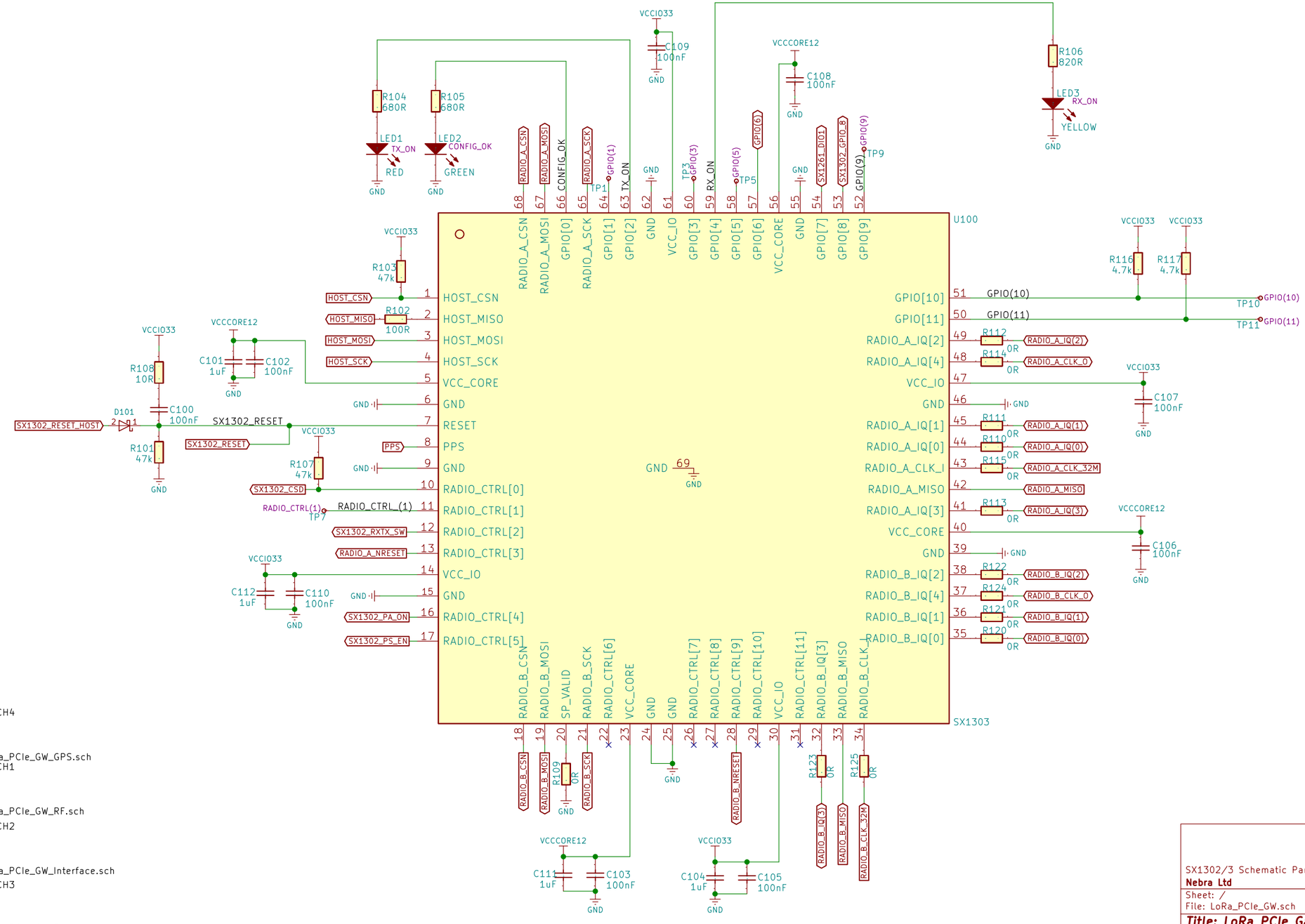
LoRa PCIe Gateway – Main part with SX1302/3 Lora Digital Baseband Chip



Sheet: SCH4

File: LoRa_PCIe_GW_GPS.sch

Sheet: SCH1

File: LoRa_PCIe_GW_RF.sch

Sheet: SCH2

File: LoRa_PCIe_GW_Interface.sch

Sheet: SCH3

File: LoRa_PCIe_GW_Power.sch

SX1302/3 Schematic Part

Nebra Ltd

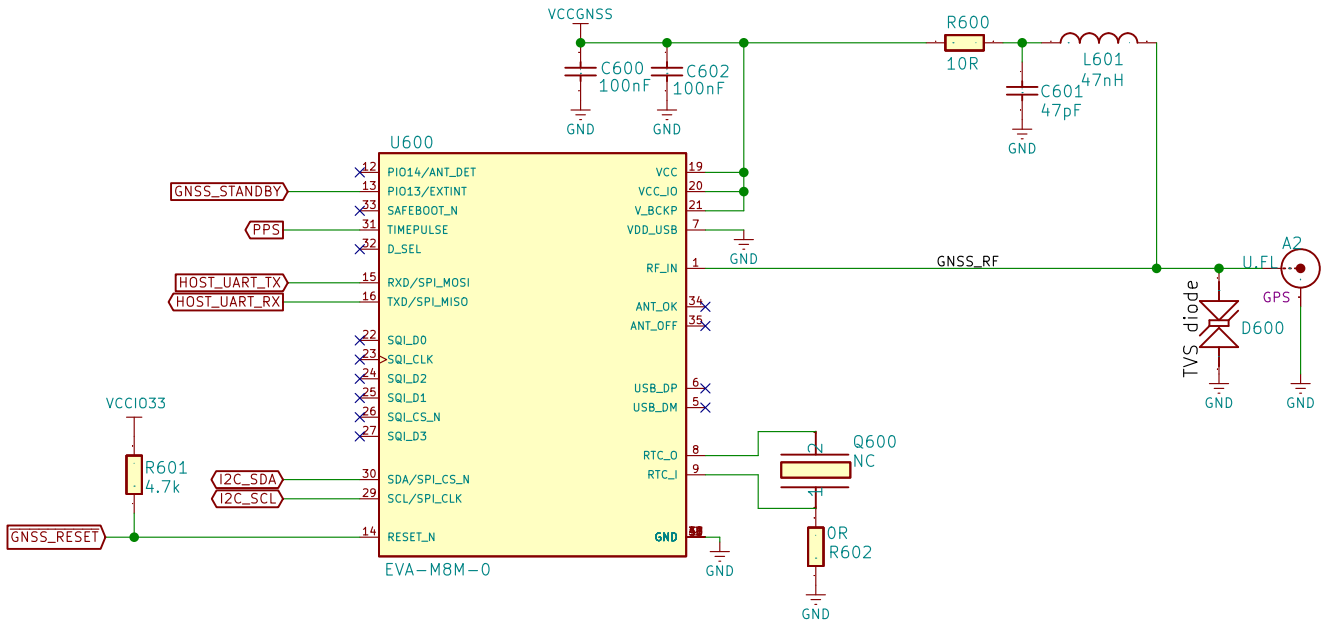
Sheet: /

File: LoRa_PCIe_GW.sch

Title: LoRa PCIe Gateway Main

Size: B	Date: 2022-01-18	**Rev: 1.2**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/5

LoRa PCIe Gateway – GNSS part with EVA-M8M SIP



GNSS Schematic part with EVA-M8M SIP

Nebra Ltd

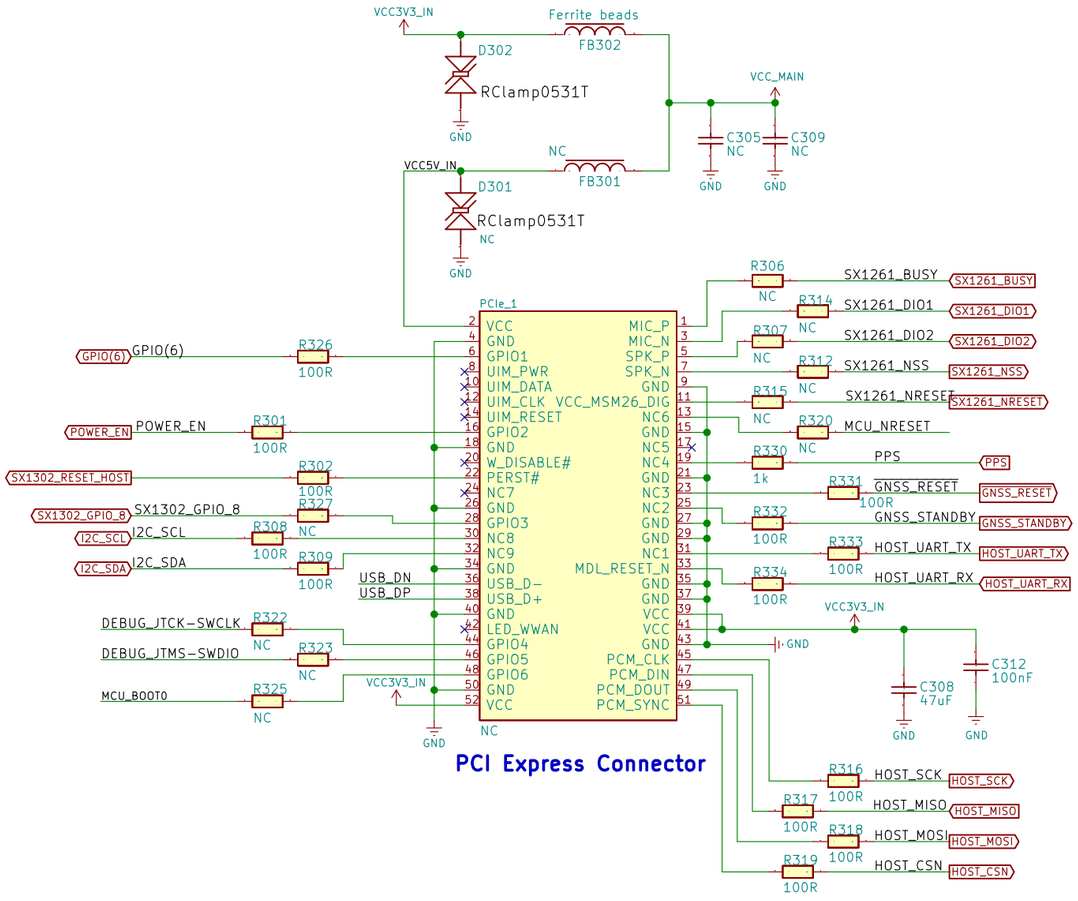
Sheet: /SCH4/

File: LoRa_PCIe_GW_GPS.sch

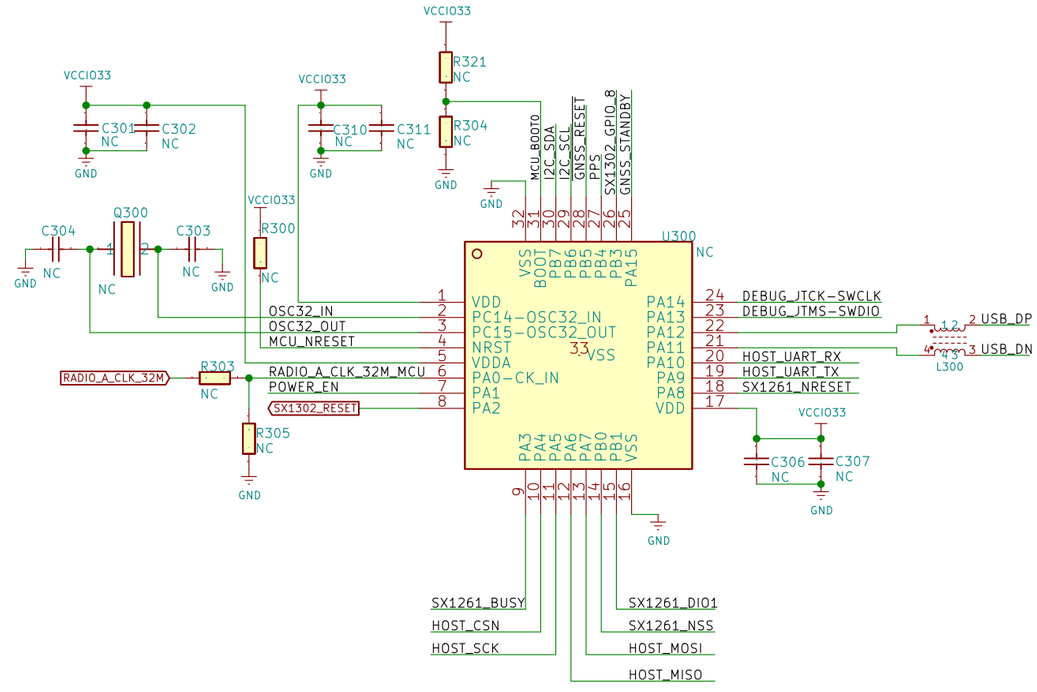
Title: LoRa PCIe Gateway – GNSS

Size: A	Date: 2022-01-18	**Rev: 1.2**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/5

LoRa PCIe Gateway Interface – mini-PCIe Interface Connector & MCU USB Bridge



PCI Express Connector



Series 0 ohm resistors = DNP when MCU/USB is used

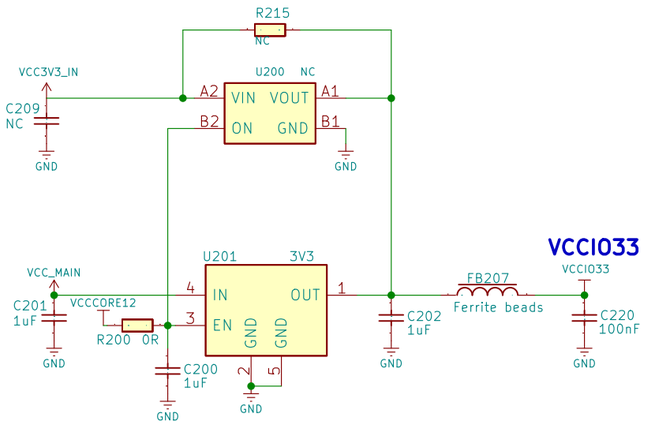
MCU = DNP when Lora Gateway odule is used through SPI Interface over PCIe connector

SWCLK, SWDIO, and MCU_NRESET are connected to mini-PCIe

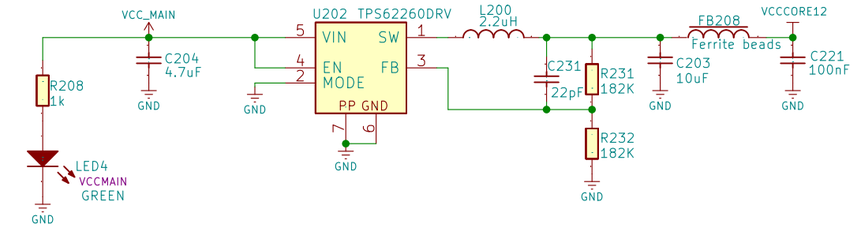
VCC_MAIN comes from 5V or 3.3V

mini-PCIe Interface Connector & MCU USB Bridge	
Nebra Ltd	
Sheet: /SCH2/	
File: LoRa_PCIe_GW_Interface.sch	
Title: LoRa PCIe Gateway Interface	
Size: B	Date: 2022-01-18
KiCad E.D.A. kicad (5.1.5)-3	Id: 3/5
	Rev: 1.2

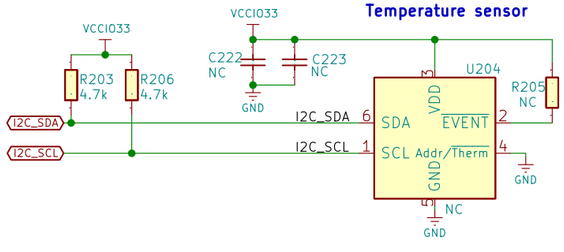
LoRa PCIe Gateway – Power Management



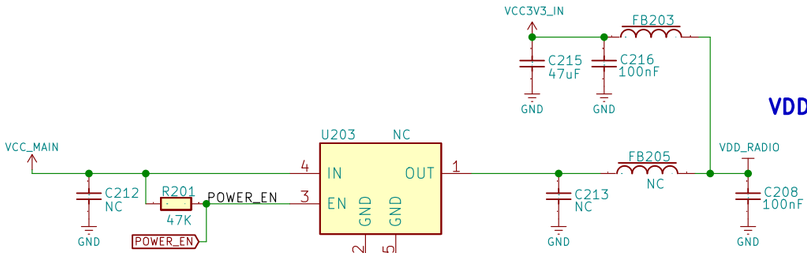
VCCIO33 : 3.3V



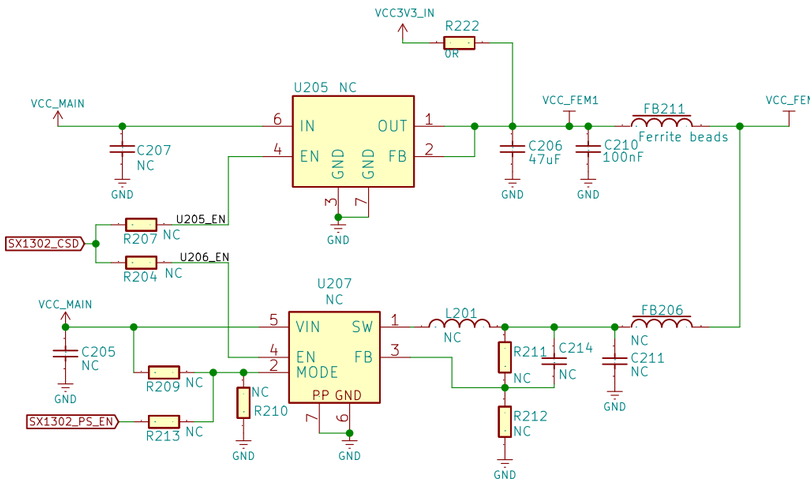
VCCCORE: 1.2V



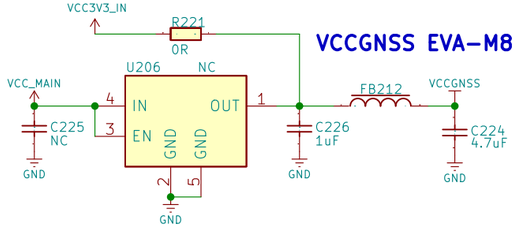
Temperature sensor



VDD_RF SX1250 & SX1261 : 3.3V



VCC_FEM : 3.3V



VCCGNSS EVA-M8 : 3.3V

Nebra logos + Fiducial_Marks:

Logo1 Logo Recycling
Logo2 Logo ESD
Logo3 Logo LoRa
Logo4 Logo KiCad
Logo5 Logo Nebra
Logo6 Open Source

Fiducial Mark
Fiducial1

MountingHole_Pad
H1
GND
H2
GND

PWR_FLAG
GND

Power Management Schematic Part
Nebra Ltd

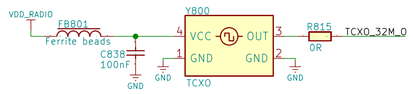
Sheet: /SCH3/
File: LoRa_PCIe_GW_Power.sch

Title: LoRa PCIe Gateway Power

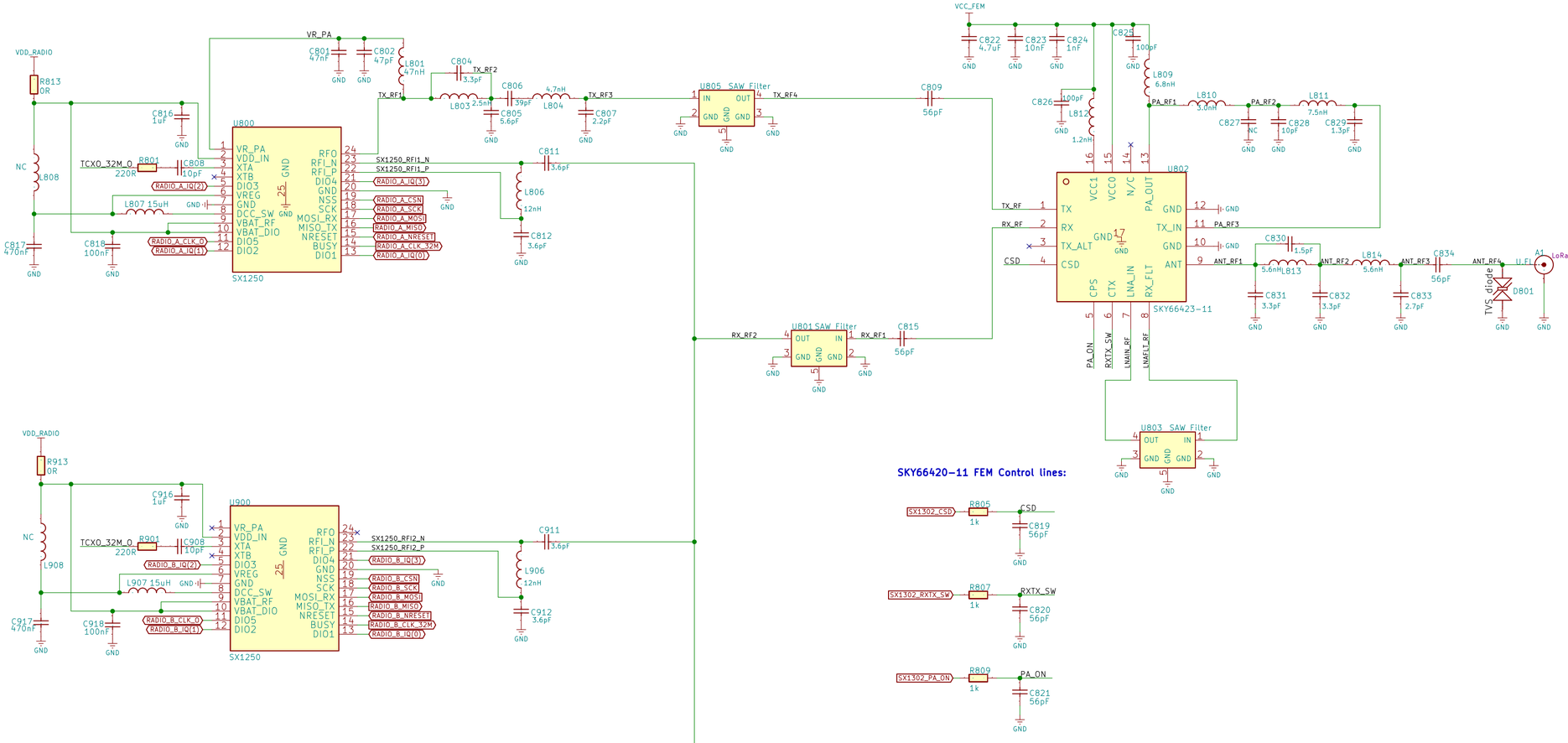
Size: B	Date: 2022-01-18	**Rev: 1.2**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/5

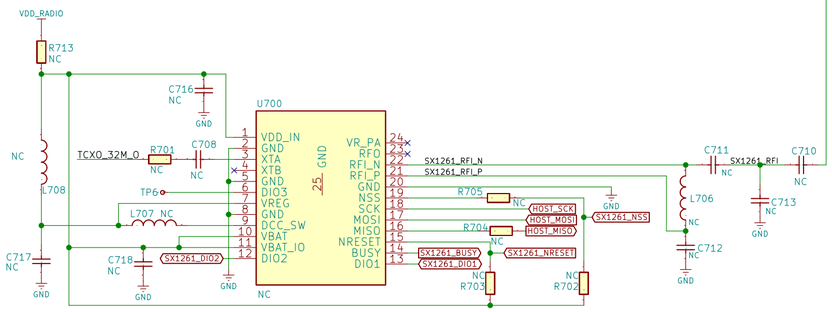
LoRa PCIe Gateway – RF Part with 2x SX1250 RF Front-Ends:

32MHz TCXO – Clipped Sinewave Output



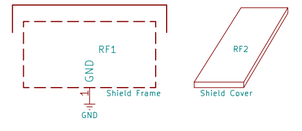
See LoRa_Reference_Clock_Selection_V1.1 for recommended osc





SKY66420-11 FEM Control lines:

Part	868M	915M
U801,U805	B4377	B4344
U803	B4377	B2625
C805	5.6pF	10pF
C711	1.8pF	2.4pF
C829	1.3pF	2.4pF
C832	3.3pF	1.8pF
C804, C831	3.3pF	NC
C833	2.7pF	NC
C807	2.2pF	2.7pF
C825	100pF	33pF
C826	100pF	120pF
C710	2.2pF	2.1pF
C830	1.5pF	2.1pF
L814	5.6nH	4.7nH
L810	3nH	2.7nH
L813	5.6nH	3.3nH



RF Front End Schematic Part

Nebra Ltd

Sheet: /SCH1/

File: LoRa_PCIe_GW_RF.sch

Title: LoRa PCIe Gateway Rf Part

Size: A2	Date: 2022-01-18	**Rev: 1.2**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/5