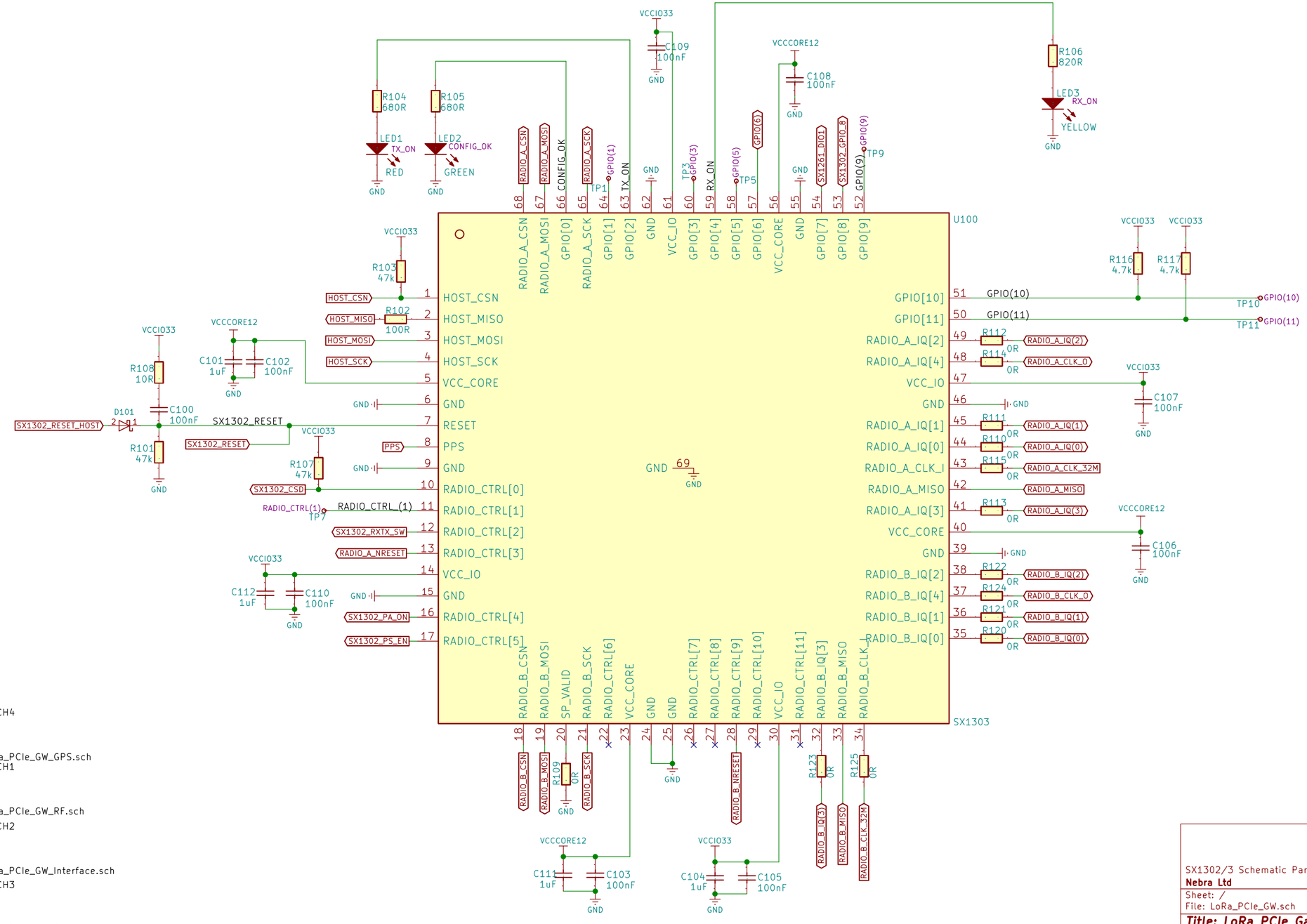
LoRa PCIe Gateway – Main part with SX1302/3 Lora Digital Baseband Chip



Sheet: SCH4

File: LoRa_PCIe_GW_GPS.sch

Sheet: SCH1

File: LoRa_PCIe_GW_RF.sch

Sheet: SCH2

File: LoRa_PCIe_GW_Interface.sch

Sheet: SCH3

File: LoRa_PCIe_GW_Power.sch

SX1302/3 Schematic Part

Nebra Ltd

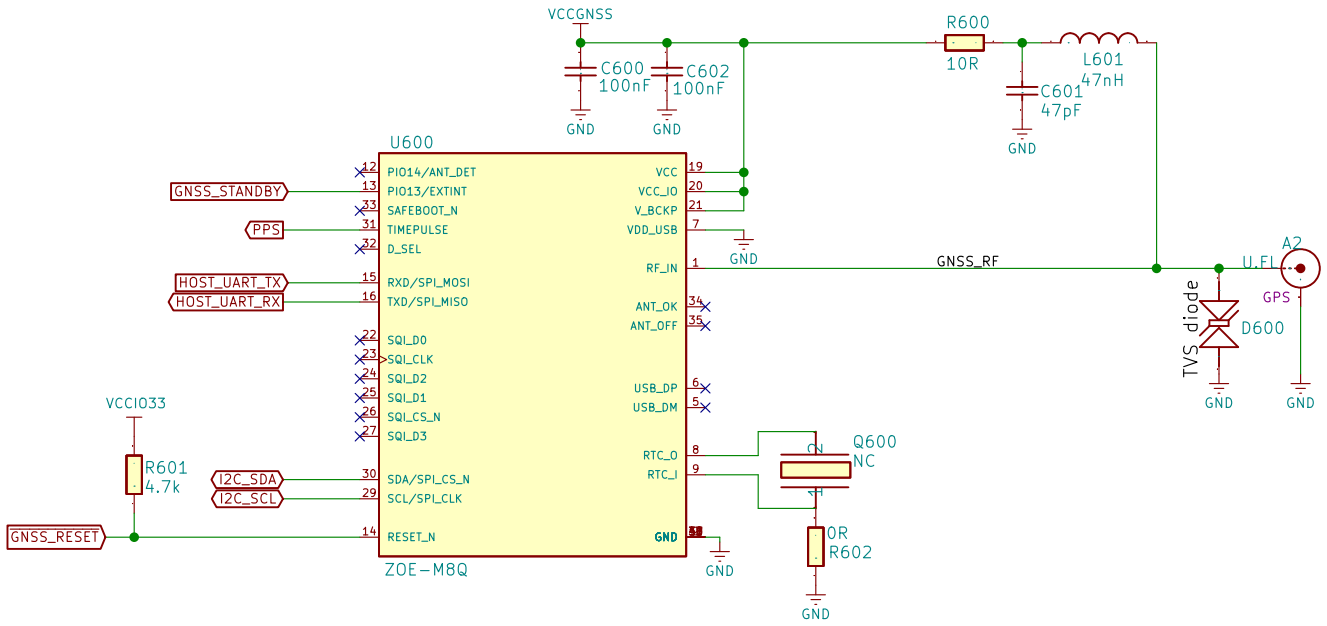
Sheet: /

File: LoRa_PCIe_GW.sch

Title: LoRa PCIe Gateway Main

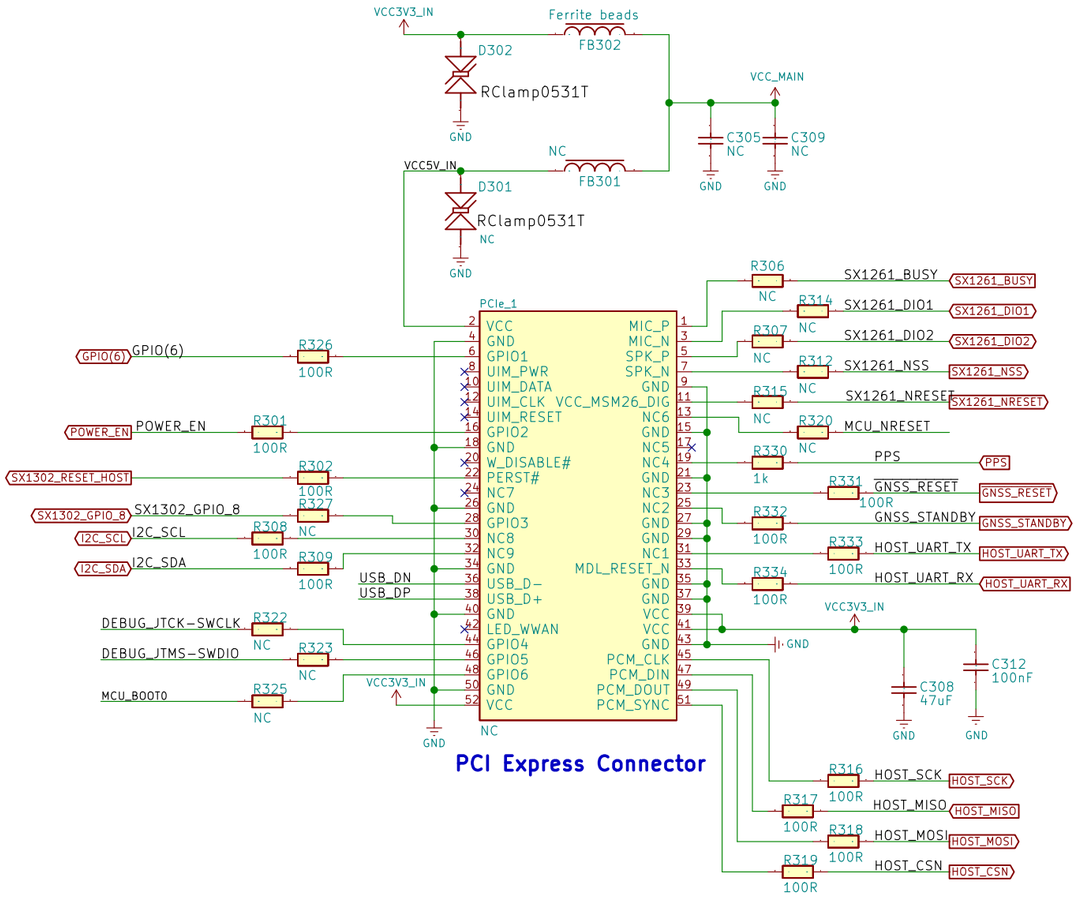
Size: B	Date: 2021-04-13	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 1/5

LoRa PCIe Gateway – GNSS part with EVA-M8M SIP

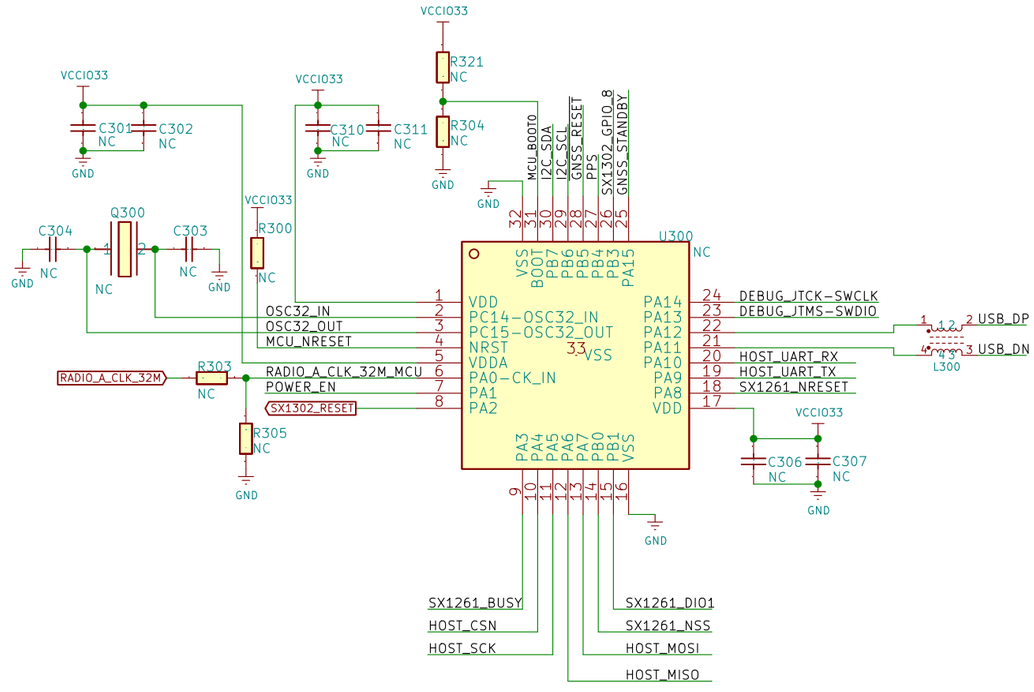


GNSS Schematic part with EVA-M8M SIP		
Nebra Ltd		
Sheet: /SCH4/		
File: LoRa_PCIe_GW_GPS.sch		
Title: LoRa PCIe Gateway – GNSS		
Size: A	Date: 2021-04-13	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 2/5

LoRa PCIe Gateway Interface – mini-PCIe Interface Connector & MCU USB Bridge



PCI Express Connector



Series 0 ohm resistors = DNP when MCU/USB is used

MCU = DNP when Lora Gateway odule is used through SPI Interface over PCIe connector

SWCLK, SWDIO, and MCU_NRESET are connected to mini-PCIe

VCC_MAIN comes from 5V or 3.3V

mini-PCIe Interface Connector & MCU USB Bridge

Nebra Ltd

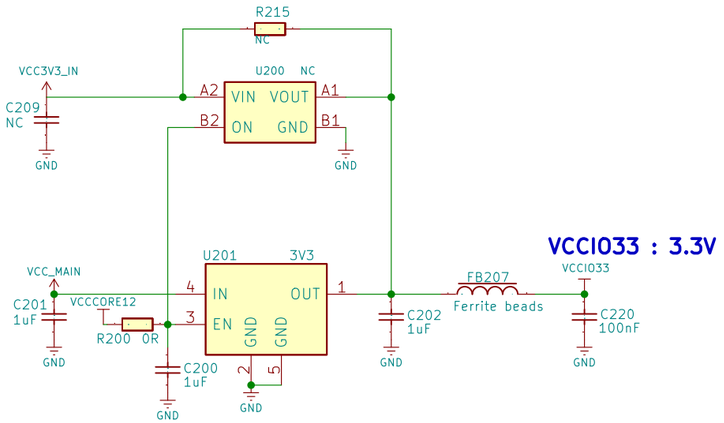
Sheet: /SCH2/

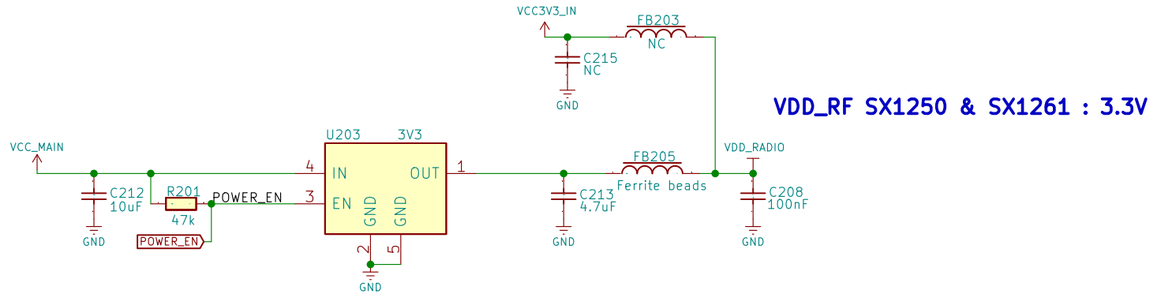
File: LoRa_PCIe_GW_Interface.sch

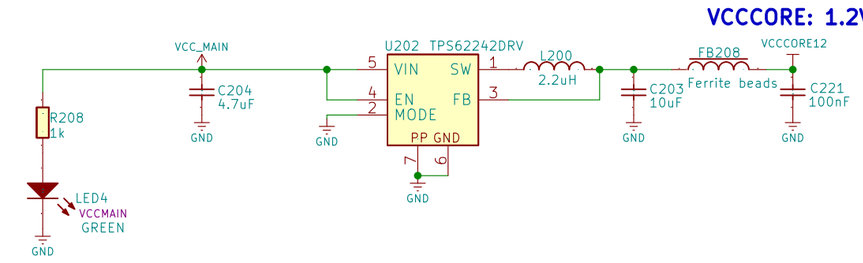
Title: LoRa PCIe Gateway Interface

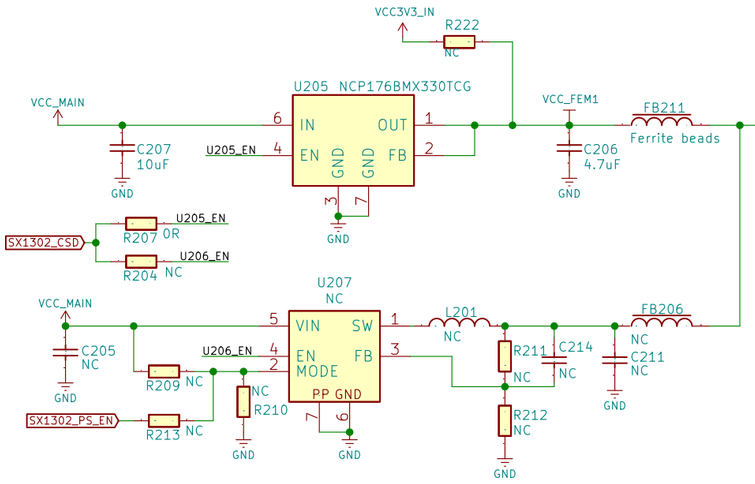
Size: B	Date: 2021-04-13	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 3/5

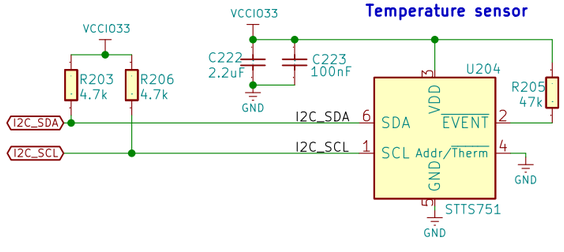
LoRa PCIe Gateway – Power Management

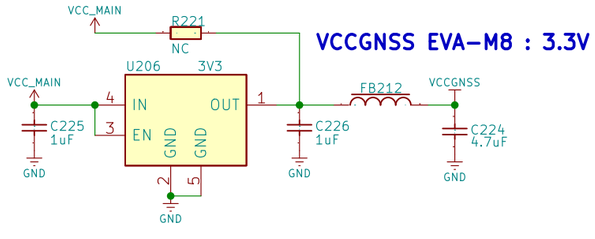












Nebra logos + Fiducial_Marks:

Logo1 Logo Recycling
Logo2 Logo ESD
Logo3 Logo LoRa
Logo4 Logo KiCad
Logo5 Logo Nebra
Logo6 Open Source

Fiducial Mark
Fiducial1

MountingHole_Pad
H1
H2
GND
GND

PWR_FLAG
GND

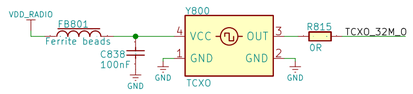
Power Management Schematic Part
Nebra Ltd
Sheet: /SCH3/
File: LoRa_PCIe_GW_Power.sch

Title: LoRa PCIe Gateway Power

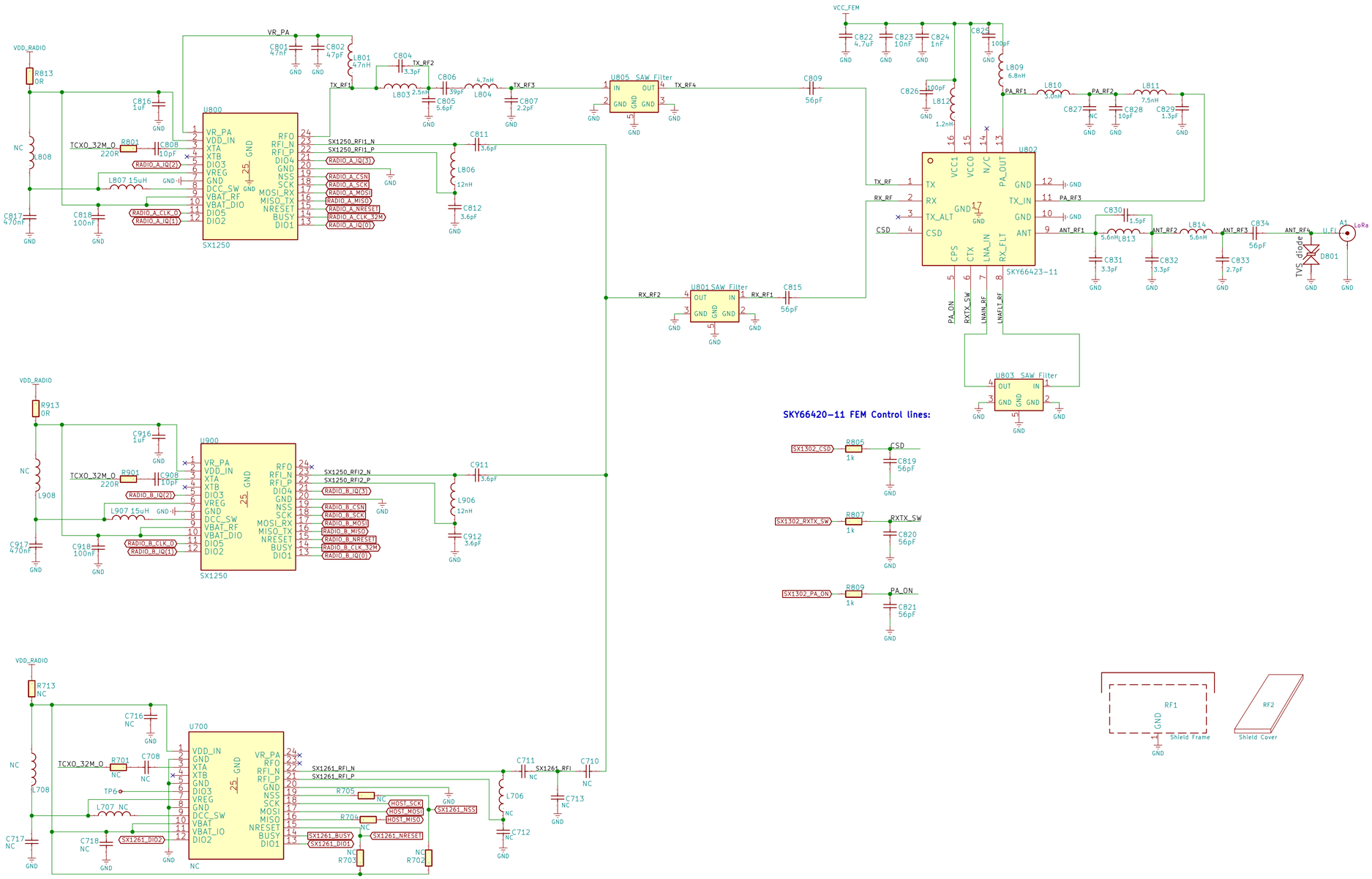
Size: B	Date: 2021-04-13	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 4/5

LoRa PCIe Gateway – RF Part with 2x SX1250 RF Front-Ends:

32MHz TCXO – Clipped Sinewave Output



See LoRa_Reference_Clock_Selection_V1.1 for recommended osc



SKY66420-11 FEM Control lines:

RF Front End Schematic Part

Nebra Ltd

Sheet: /SCH1/

File: LoRa_PCIe_GW_RF.sch

Title: LoRa PCIe Gateway Rf Part

Size: A2	Date: 2021-04-13	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.5)-3		Id: 5/5