THANTHAI PERIYAR GOVERNMENT INSTITUTE OF TECHNOLOGY, VELLORE - 632 002

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ENERGY EFFICIENT IN-MEMORY COMPUTING ARCHITECTURE WITH ENHANCED POLYMORPHIC CIRCUIT

PROJECT GUIDE

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ABSTRACT

To accomplish In-Memory Computing (IMC) by implementing all fundamental two-input Boolean functions, a hybrid memory architecture based on a novel array of SRAM and Resistive Random-Access Memory (RRAM) cells is proposed. The Proposed architecture can be utilized as an SRAM array to store data for high-performance applications. It can also be set up to read data from RRAMs and carry out In-memory computations as a sense amplifier (SA-SRAM). In addition, to address security concerns, the proposed polymorphic circuit primitive to prevent reverse engineering or integrated circuit (IC) counterfeiting. Furthermore, the energy consumption of our design in application areas like image processing is significantly less than the well-known comparative in-memory architecture solution.

INTRODUCTION

- With the increasing need for high-performance processing in applications such as artificial intelligence, neural networks, search engines, biological systems, and image processing, the von Neumann architecture faces a critical challenge known as the memory wall.

- In this case, transferring a large amount of data back and forth between a separate processor and memory leads to severe energy consumption, high latency, and I/O congestion.

- Therefore, one of the most promising approaches for alleviating these challenges is in-memory computing (IMC), which provides computing capability inside memory.

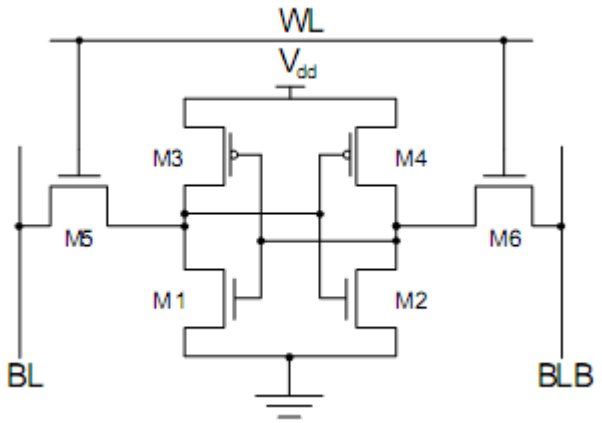
- IMC can perform simple computational tasks to reduce memory-processor data transfers.

LITERATURE SURVEY

S.NO	YEAR	TITLE	METHODOLOGY	LIMITATIONS
1.	May 2016	Functional polymorphism for intellectual property protection	DRAM/MRAM	Lag of Fast read/write and low power consumption.
2.	FEB 2020	Hybrid Spin CMOS Polymorphic logic gate	MTJ/CMOS Logic gates	Delay in performing Boolean computation is higher
3.	MAY 2020	IMC with double word lines and 3 read ports for 4 operands	8T SRAM Cell	Area overhead and Volatility are critical bottlenecks of this design
4.	NOV 2022	Short term long term compute-in-memory architecture with intrinsic consolidation	Hybrid Spin/CMOS approach	Unsuitable for complex computations.

EXISTING METHODS

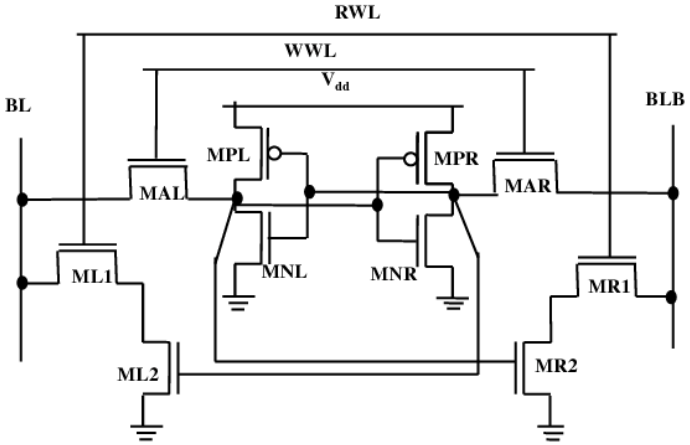
6T STANDARD SRAM CELL:



LIMITATIONS:

- High static power consumption
- Read and write disturbances can also compromise data integrity, requiring additional circuitry for mitigation.

10T SRAM CELL:

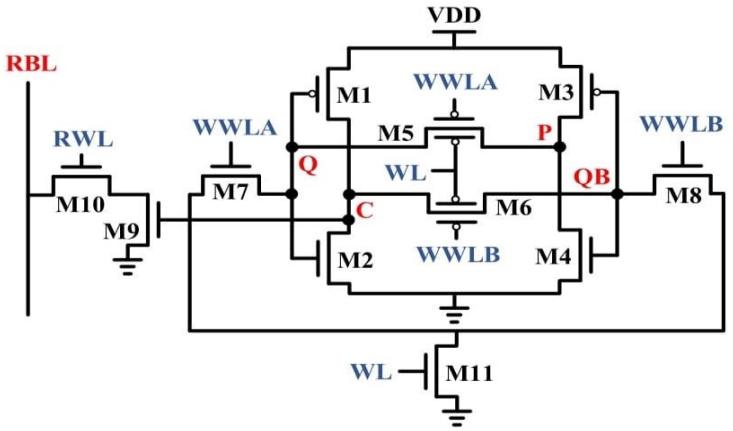


LIMITATIONS:

- Larger cell size and higher fabrication complexity.
- Practical implementation may be constrained in applications.

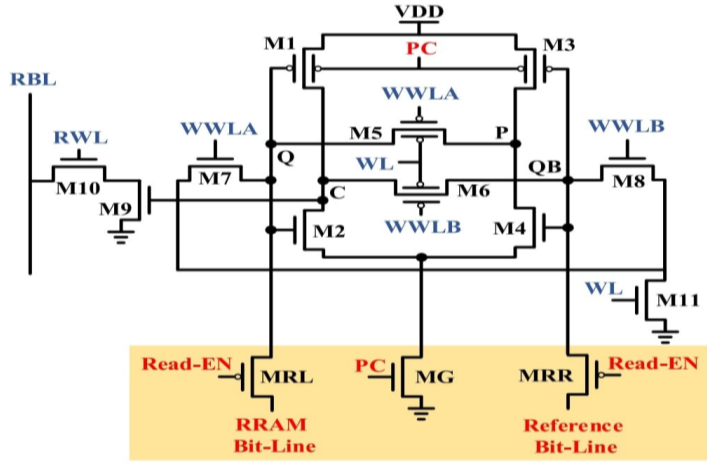
PROPOSED METHOD

Half select 11T SRAM Cell



- 11TSRAM cell provides greater read power and write power compared to 6TSRAM cell.
- To avoid unwanted writing in the neighbouring cell of the cell in reading and writing process, known as the HALF SELECT.
- This issue entirely addressed in our proposed cell.

Reconfigurable Half select 11T (HF11T) Cell



- To store and read data from a non-volatile memory or volatile memory.
- This Proposed cell can be configured as fast memory elements SRAM Mode in real time applications.
- Improved read stability and reliability can be achieved in this design.

IN-MEMORY ARCHITECTURE

- It includes an RRAM-based main memory array (MMA), a reconfigurable SRAM array (SA-SRAM), and polymorphic logic units (PMU).

A.MMA MEMORY MODE

- In MMA, the data stored in a memory cell is represented by the resistance of RRAM. To write a bit into a memory cell, the corresponding source line (SL) and bit-line (BL) are connected to the respective voltages to modify the stored data.

B.MMA COMPUTING MODE

- The data on both cells are ‘‘00’’ (low-low), ‘‘01’’ or ‘‘10’’ (low-high), or ‘‘11’’ (high high), the voltage on BL will be low (LV), medium (MV), or high (HV), respectively.

C.SA-SRAM MEMORY MODE

- SA-SRAM operates in the SRAM mode by disabling the active-low PC signal (PC=‘1’).
- The write operation is accomplished by selecting the required signals (WWLA, WWLB and WL) for the desired cell, activated by the SRD and SCD decoders.

D.SA-SRAM COMPUTING MODE

- The SA-SRAM cell provides in-memory computations in the SRAM mode, benefitting from the isolated read path due to the decoupled read ports.
- The isolated read mechanism makes it possible to perform the OR/NOR, AND/NAND, and XOR/XNOR functions within the SA-SRAM array.

POLYMORPHIC UNIT [PMU]:

Uses of Polymorphic Ciruit

1.Flexibility in implementing multiple processes,

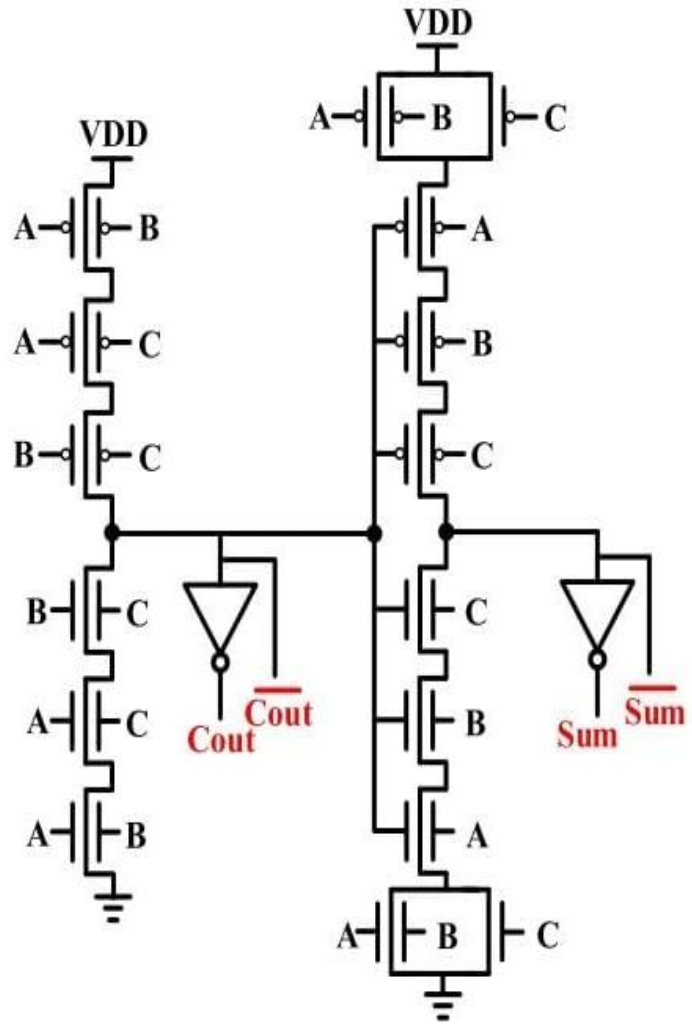
2.preventing security risks such as penetration,

3.reverse engineering.

- This structure can be configured as a dual-purpose design that can perform different functions:

  i) simple logic functions (logic mode)

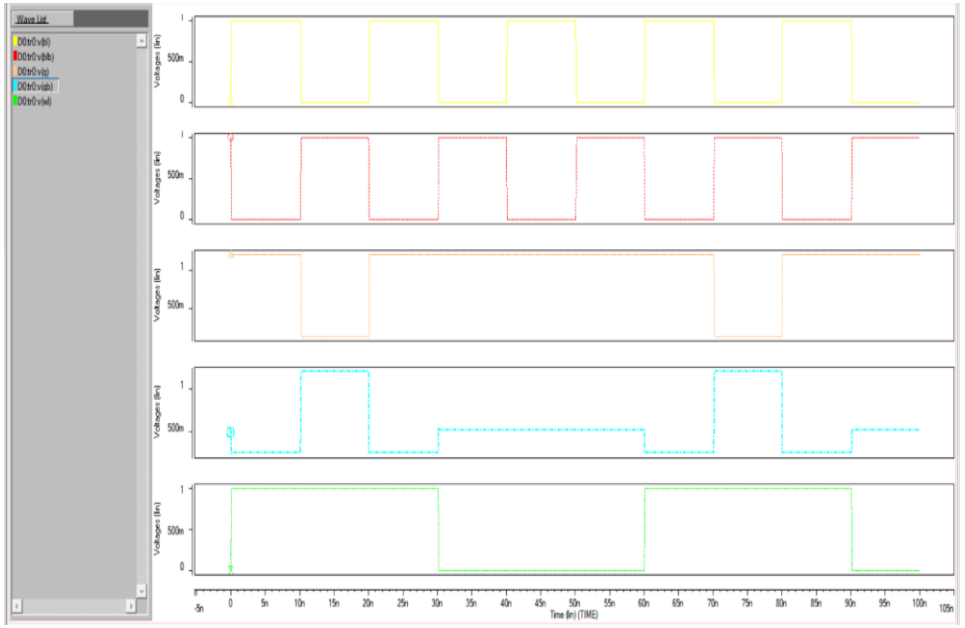
  ii) full-adder (full-adder mode)



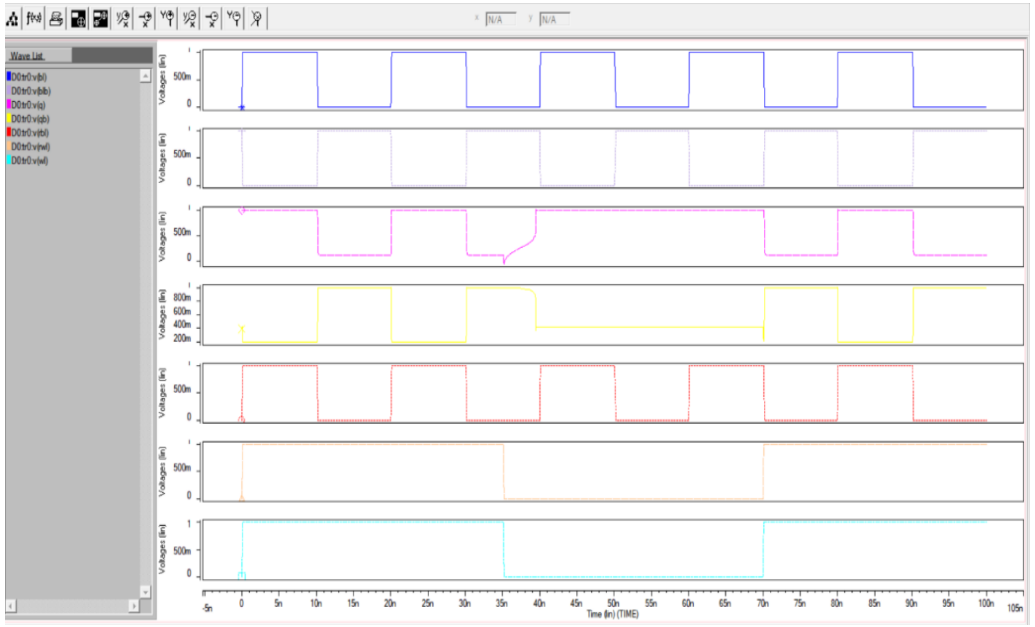
RESULTS AND DISCUSSIONS

A Timing diagram for an Half select 11T SRAM cell, Reconfigurable Half select SRAM cell and Polymorphic logic design, HSPICE simulations are performed ,which illustrates the various signals and their timing relationships during read and write operations

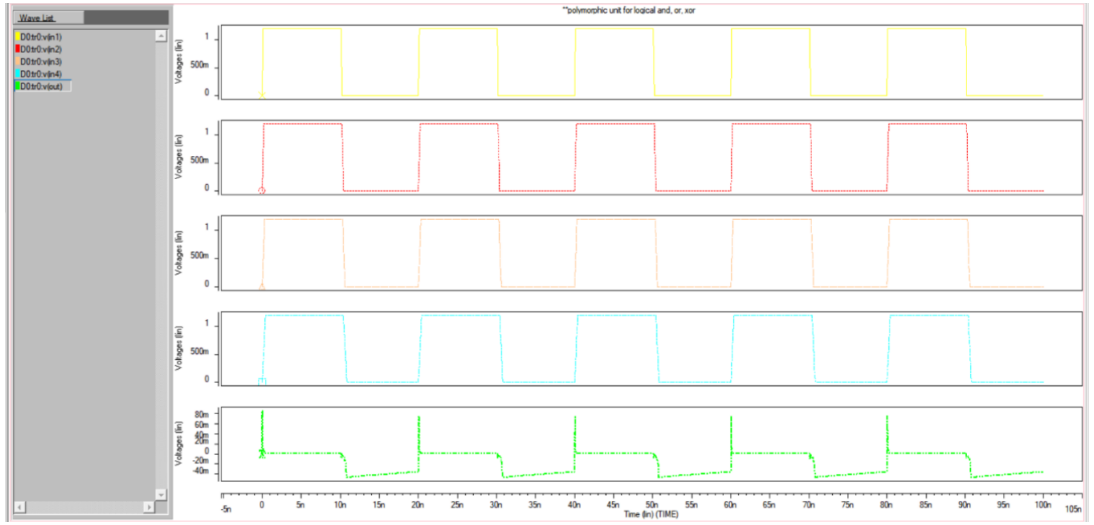
Transient waveform of Half Select 11T SRAM Cell



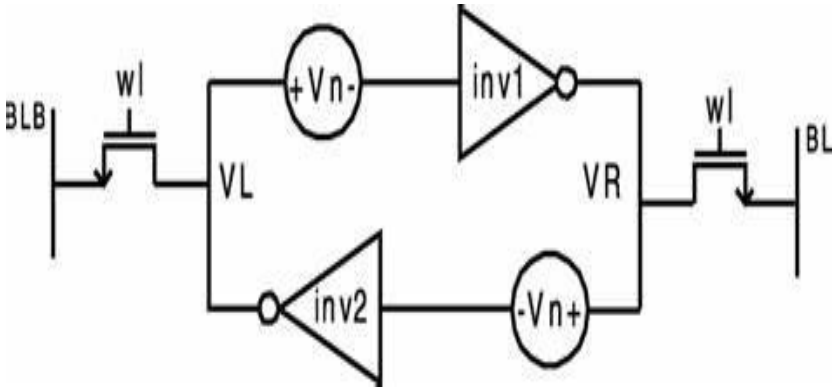
Transient waveform of Reconfigurable Half Select 11T SRAM Cell



Transient waveform of Polymorphic logic design



Measurement setup for Static Noise Margin



STATIC NOISE MARGIN (SNM)

- The static noise margin (SNM) of an SRAM (Static Random-Access Memory) cell refers to its tolerance to noise in maintaining stored data reliably. It is a critical parameter for the stability and reliability of SRAM operations.
- The read margin determines how much voltage can be dropped on the bit-lines before a read operation fails.
- The write margin refers to the voltage difference between the values of the bit-lines that are necessary to successfully write data into the cell. It's essentially the difference in voltage between the bit-line and the sensing voltage necessary for correct read operation.

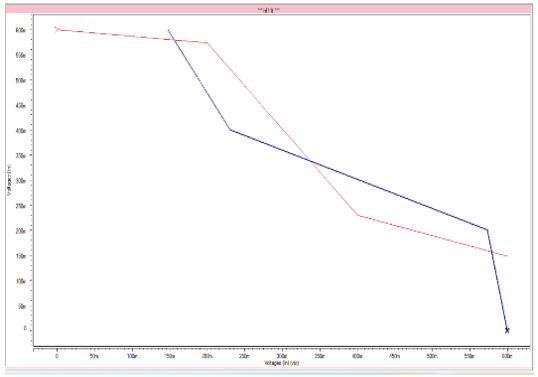
COMPARISON OF VARIOUS SRAM CELLS IN THE 7NM FINFET TECHNOLOGY

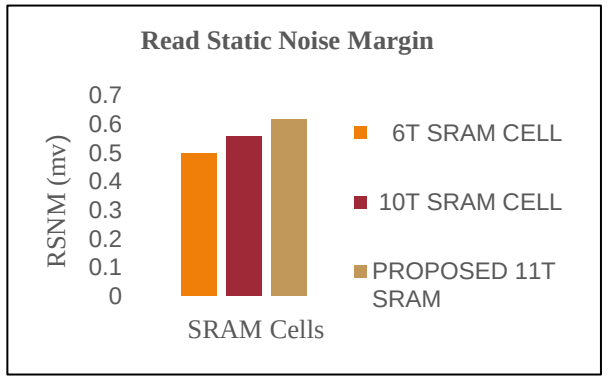
PARAMETERS	6T SRAM CELL	10T SRAM CELL	PROPOSED 11T SRAM
RSNM (mv)	0.498	0.558	0.616
HSNM (mv)	0.082	0.091	0.112
WSNM (mv)	0.498	0.521	0.545
READ POWER (uw)	695.9	558.5	426.2
WRITE POWER (uw)	0.0183	0.521	1.67
HOLD POWER (nw)	0.303	0.294	0.277
WRITE PDP(m)	0.481	0.733	0.881
READ PDP(m)	0.859	0.975	1.328

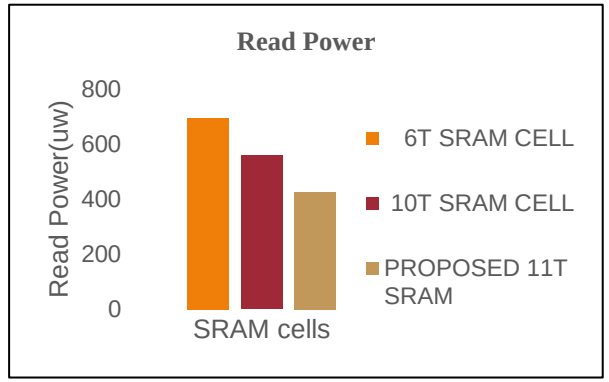
SIMULATION RESULTS

DC Waveforms

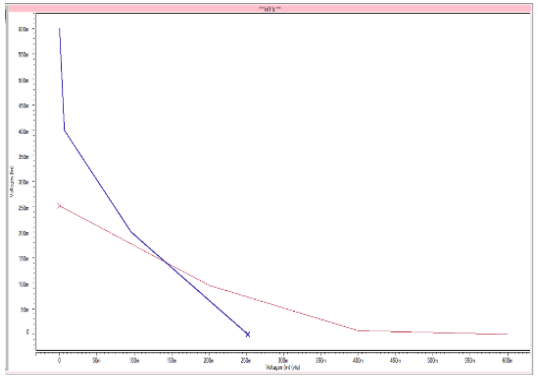
a) Read Static Noise Margin

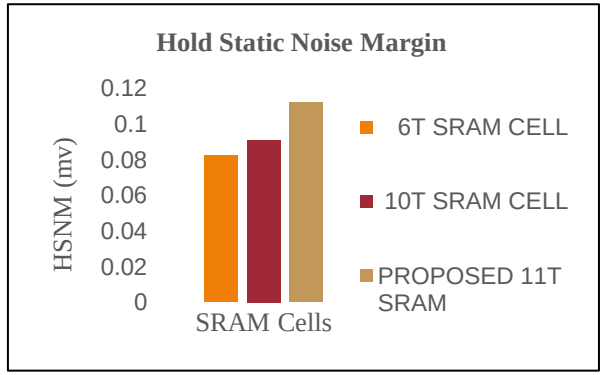


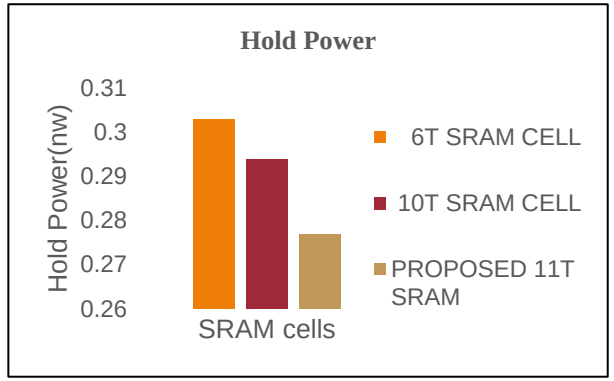




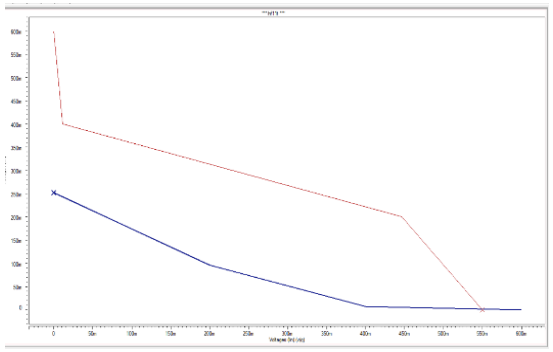
b) Hold Static Noise Margin

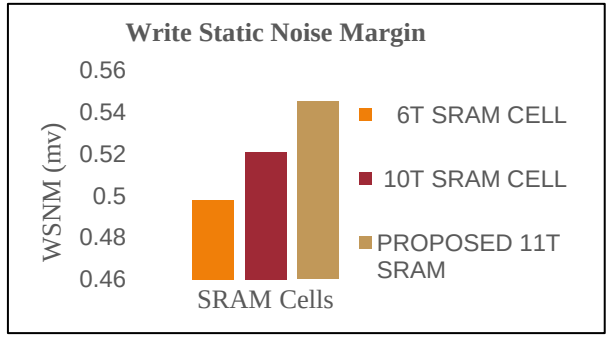


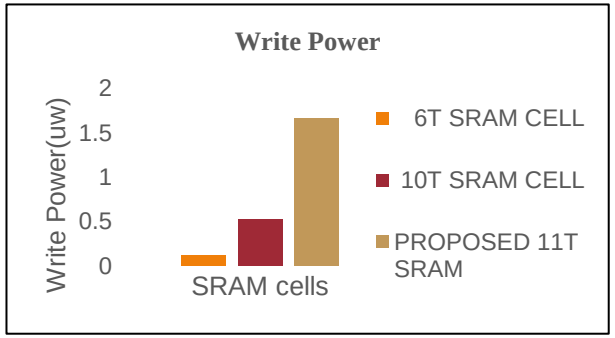




c) Write Static Noise Margin







CONCLUSION

- In-memory processing is a promising paradigm that improves the throughput and energy consumption, especially in data intensive applications.
- The Proposed reconfigurable SRAM cell has a high static noise margin and a free half-select issue which is essential for memory design adding the sense amplifier feature to the proposed SRAM cell.
- Moreover, by benefiting from the combination of SRAM and RRAM cells in the proposed architecture, the energy consumption of our design in application areas, such as image processing, is much lower than the well-known compared in-memory architecture designs.

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