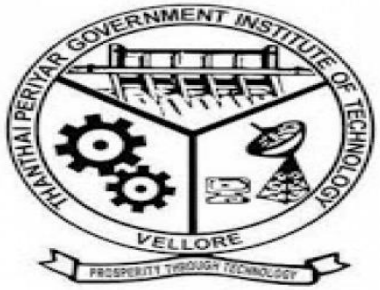


THANTHAI PERIYAR GOVT. INSTITUTE
OF TECHNOLOGY, VELLORE
DEPARTMENT OF ECE

AN ENERGY-EFFICIENT HYBRID SRAM BASED IN-MEMORY COMPUTING ARCHITECTURE WITH INDEPENDENT GATE FINFETS

PROJECT GUIDE:

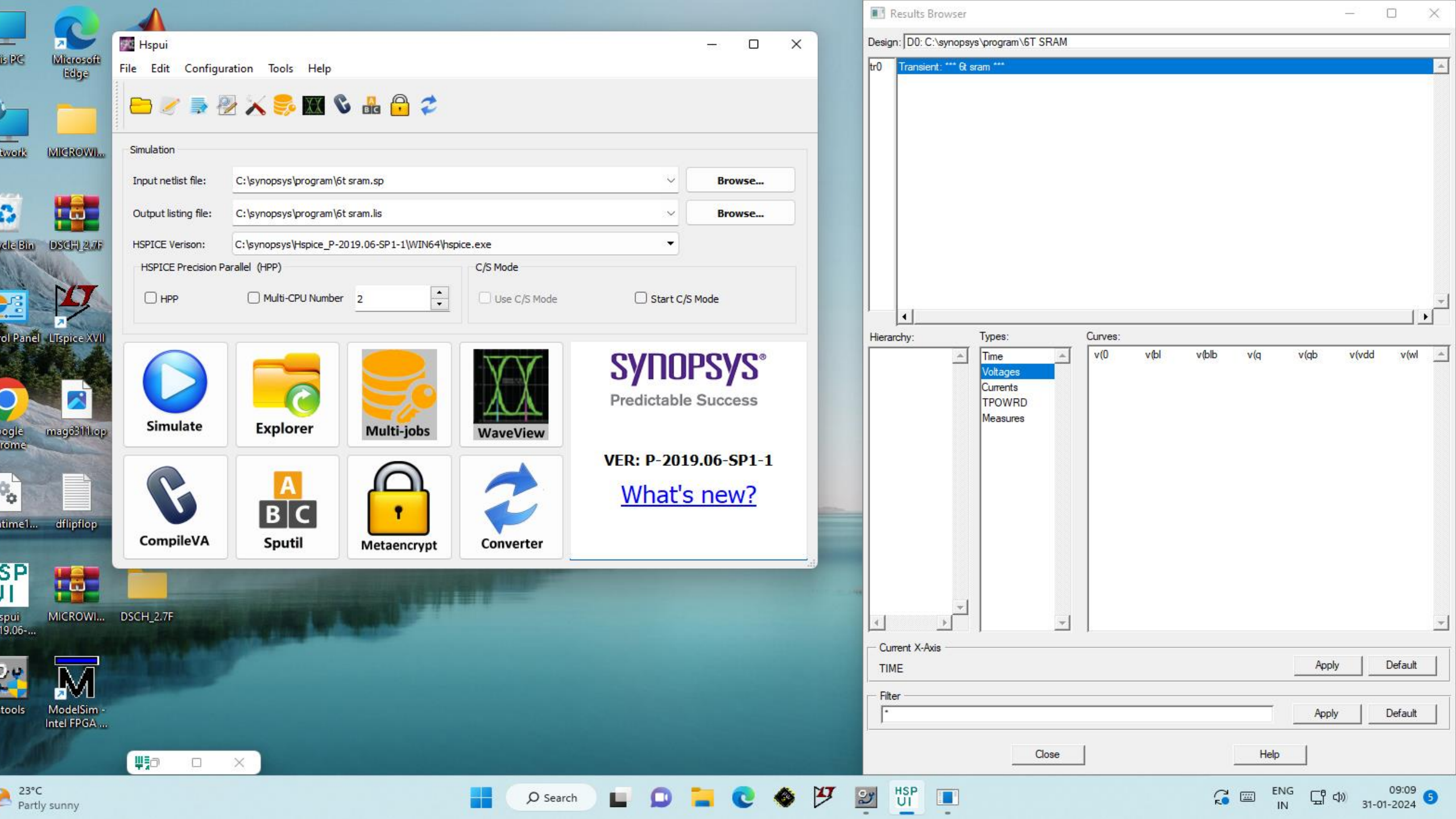
Mrs. M.JANANI, M.E., Assistant Professor

TEAM MEMBERS:

1) VINITHA K (513120106095)
2) PAVITHRA B(513120106063)
3) SHRUTHI B K (513120106078)

PROBLEM STATEMENT AND TECHNOLOGY PROPOSED

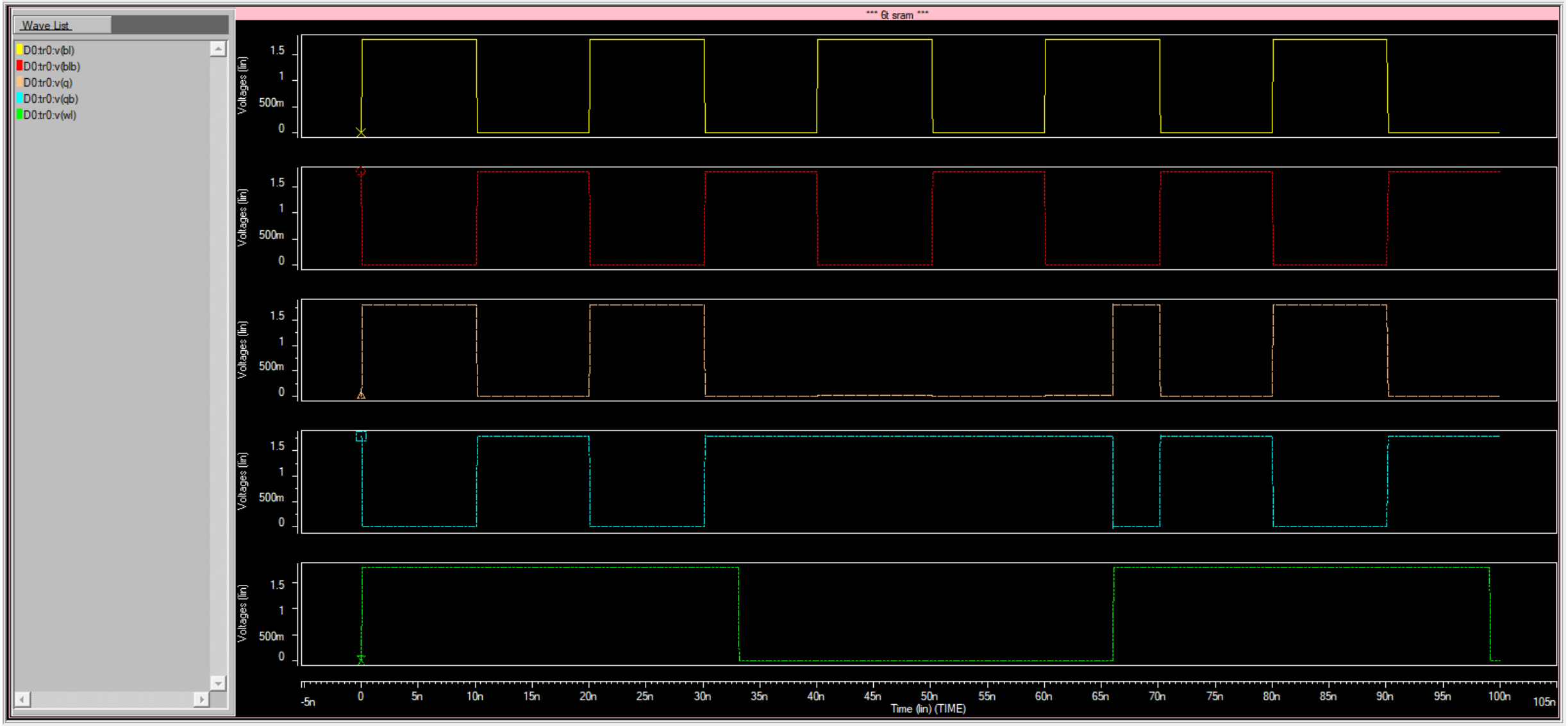
- The Hybrid SRAM/RRAM In-Memory Computing Architecture revolves around enhancing Energy efficiency and computational performance in memory centric tasks. The challenge lies in optimizing the integration of SRAM and RRAM technologies to enhance overall performance.
- The goal is to develop a flexible and efficient solution to implement all Boolean functions and also to overcome memory wall.
- Therefore, one of the most promising approaches for alleviating these challenges, **In-Memory Computing (IMC)** is proposed.
- **SOFTWARE TOOL**: SYNOPSYS HSPICE


Hspui
File
Edit
Configuration
Tools
Help
Simulation
Input netlist file:
C:\synopsys\program\6t sram.sp
Browse...
Output listing file:
C:\synopsys\program\6t sram.lis
Browse...
HSPICE Verison:
C:\synopsys\Hspice_P-2019.06-SP1-1\WIN64\hspice.exe
HSPICE Precision Parallel (HPP)
HPP
Multi-CPU Number
2
C/S Mode
Use C/S Mode
Start C/S Mode
Simulate
Explorer
Multi-jobs
WaveView
CompileVA
Sputil
Metaencrypt
Converter
SYNOPSYS®
Predictable Success
VER: P-2019.06-SP1-1
What's new?
Results Browser
Design:
D0: C:\synopsys\program\6T SRAM
tr0
Transient: *** 6t sram ***
Hierarchy:
Types:
Time
Voltages
Currents
TPOWRD
Measures
Curves:
v(0
v(bl
v(blb
v(q
v(qb
v(vdd
v(wl
Current X-Axis
TIME
Apply
Default
Filter
*
Apply
Default
Close
Help
Microsoft Edge
MICROWI...
DSCH_2.7F
LTspice XVII
mag6311.op
dflipflop
ModelSim - Intel FPGA ...
23°C
Partly sunny
Search
ENG
IN
09:09
31-01-2024

AvanWaves B-2008.09-SP1 (20081124)

Design Panels Window Measure Configuration Tools Help

x N/A y N/A



28°C Haze

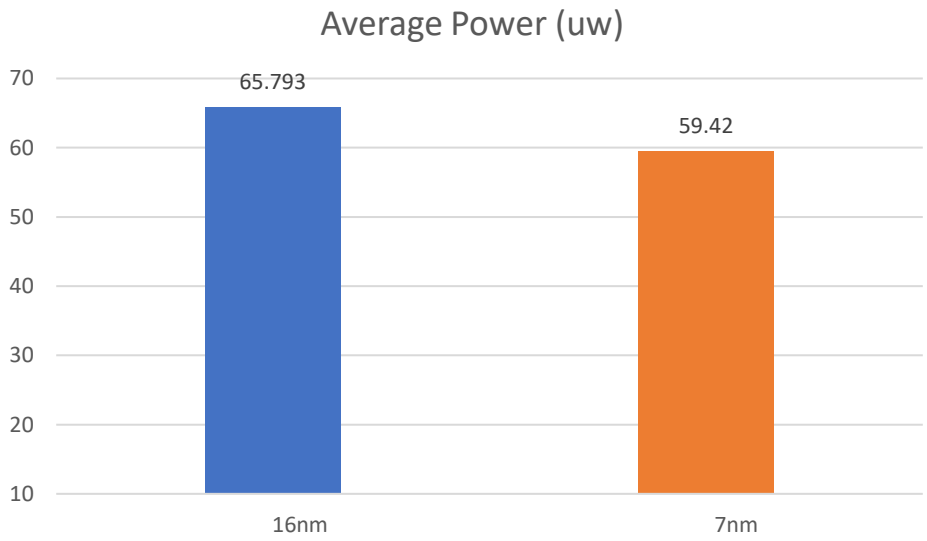
Search

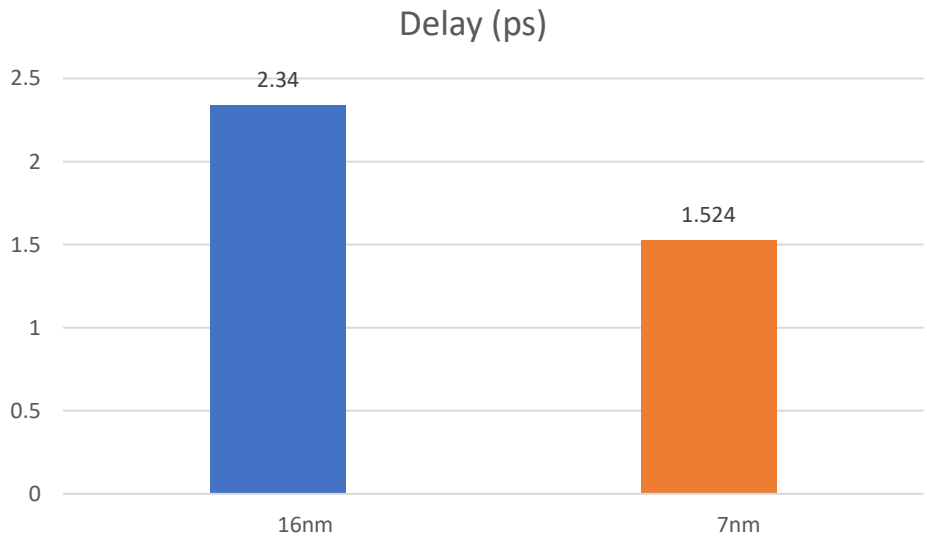
ENG IN

12:50 30-01-2024

PERFORMANCE ANALYSIS:

FINFET Technology	Average Power (uw)	Delay (ps)	Temperature (°C)
16nm	65.793	2.340	25
7nm	59.42	1.524	25





WORK DONE:

Date	Work Planned	Review Date	STATUS
01.01.24 – 07.01.24	Define Problem Statement & find feasible solution.	10.01.24	✓
08.01.24 – 14.01.24	Analysis of SRAM cell and reviewing different SRAM cells	18.01.24	✓
15.01.24 – 21.01.24	Installation of SYNOPSYS HSPICE & understanding of design process in the tool	23.01.24	✓
22.01.24 – 28.01.24	Implementation of standard Memory cell in the SPICE tool.	30.01.24	✓
29.01.24 – 04.02.24	Implementation of Half-select free 11T SRAM cell(HFT11T)	06.02.24	
05.02.24 – 11.02.24	Determining Power Consumption, Read /Write Static Noise Margin & other Metrics	13.02.24	
12.02.24 -18.02.24	Explore the reconfigurable SRAM sense amplifier(SA-SRAM)	20.02.24	
19.02.24 – 25.02.24	Simulate the design of RRAM cell	27.02.24	
26.02.24 – 03.03.24	Design of SA-SRAM in COMPUTING MODE	05.03.24	
04.03.24 – 10.03.24	Design the circuit of Polymorphic unit(PMU)	12.03.24	
11.03.24 – 17.03.24	Integrate RRAM, SA-SRAM, PMU cells using HSPICE Simulation	19.03.24	
18.03.24 – 24.03.24	Performance Evaluation in terms of SNM, Power, Delay	26.03.24	
25.03.24 – 31.03.24	Report and Documentation	02.04.24	