THANTHAI PERIYAR GOVT. INSTITUTE
OF TECHNOLOGY, VELLORE
DEPARTMENT OF ECE

AN ENERGY-EFFICIENT HYBRID SRAM BASED IN-MEMORY COMPUTING ARCHITECTURE WITH INDEPENDENT GATE FINFETS

PROJECT GUIDE:

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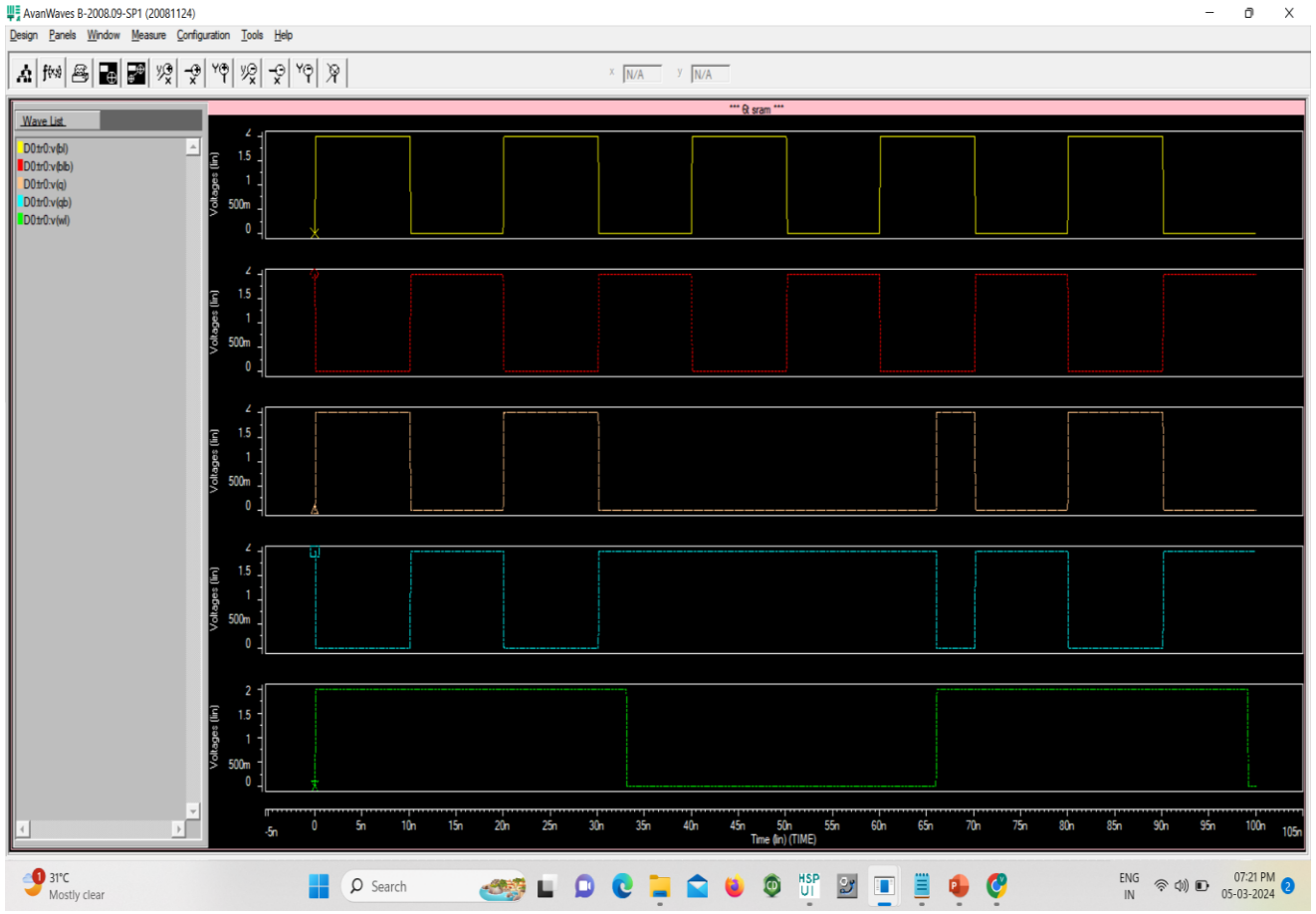
PROBLEM STATEMENT AND TECHNOLOGY PROPOSED

- The Hybrid SRAM/RRAM In-Memory Computing Architecture revolves around enhancing Energy efficiency and computational performance in memory centric tasks. The challenge lies in optimizing the integration of SRAM and RRAM technologies to enhance overall performance.
- The goal is to develop a flexible and efficient solution to implement all Boolean functions and also to overcome memory wall.
- Therefore, one of the most promising approaches for alleviating these challenges, **In-Memory Computing (IMC)** is proposed.
- **SOFTWARE TOOL**: SYNOPSYS HSPICE

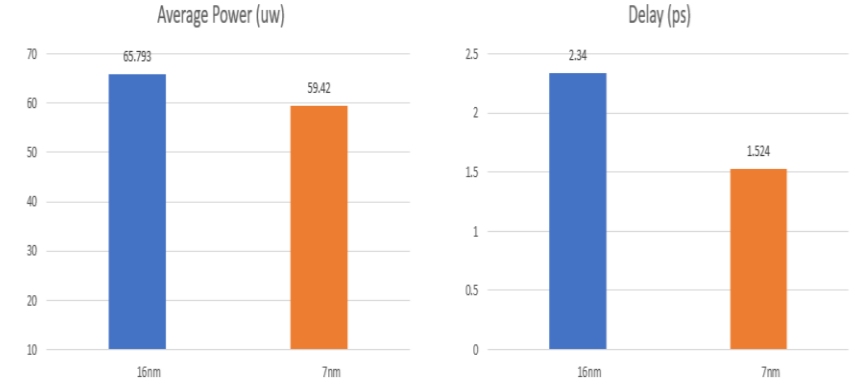
Results upto First Review

Implementation of 6T SRAM:

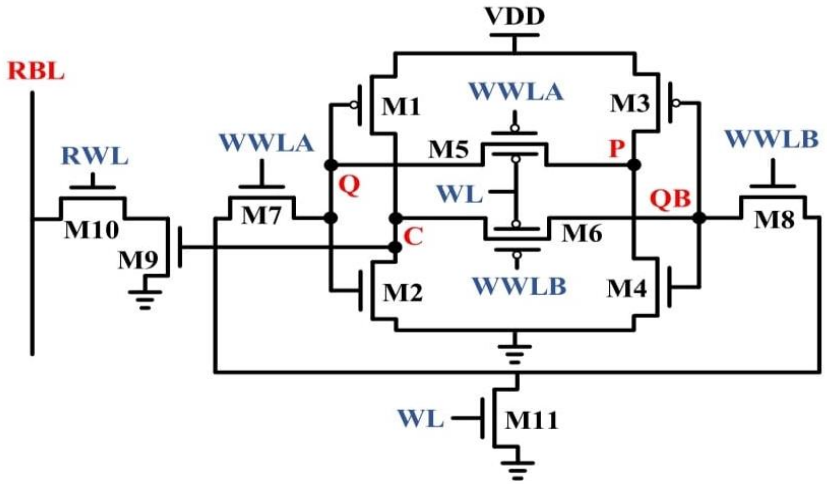


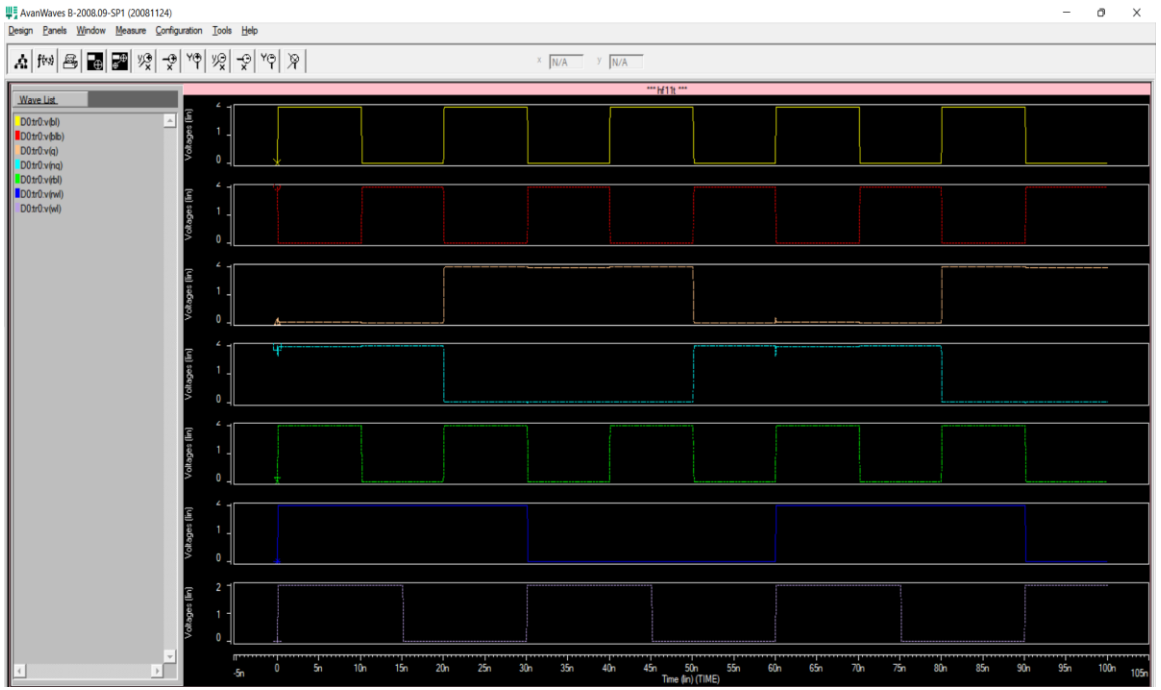
PERFORMANCE ANALYSIS:

FINFET Technology	Average Power (uw)	Delay (ps)	Temperature (°C)
16nm	65.793	2.340	25
7nm	59.42	1.524	25

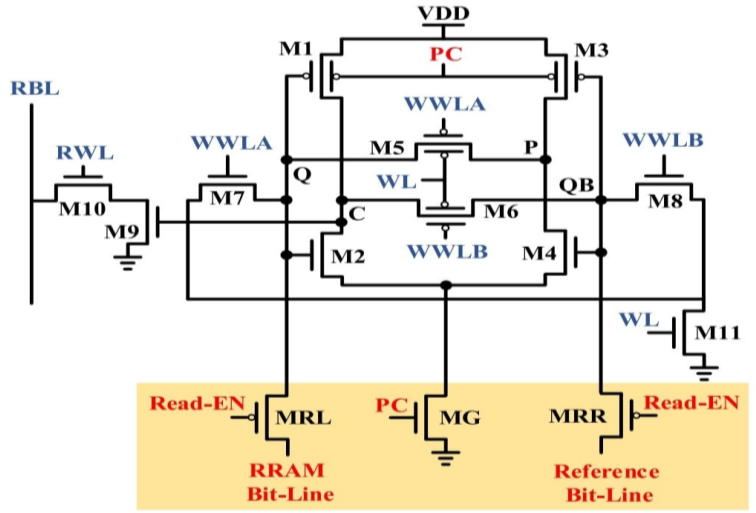


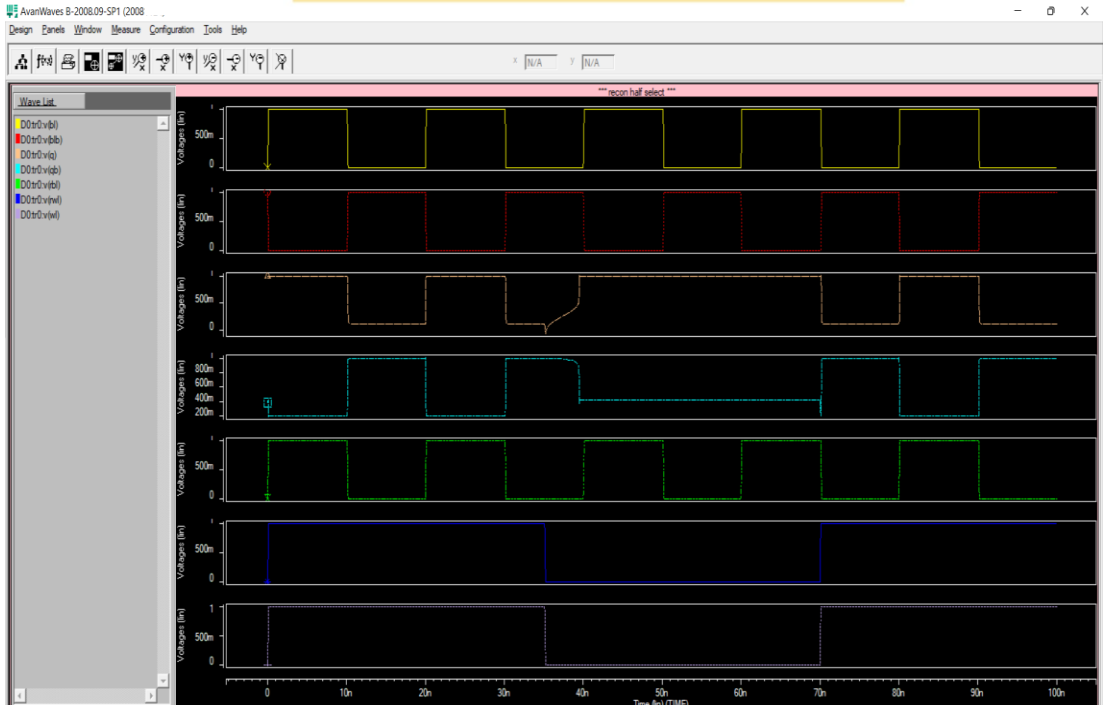
Half select 11T SRAM Cell:





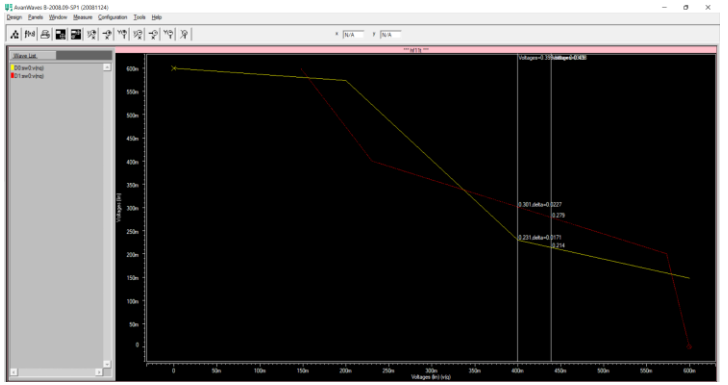
Reconfigurable Half select 11T (HF11T):

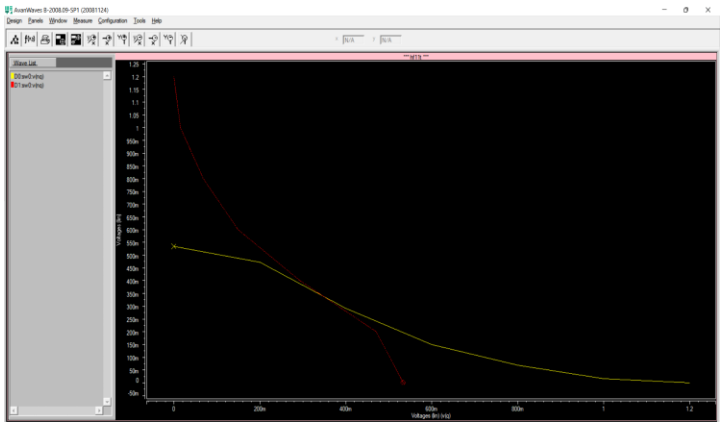


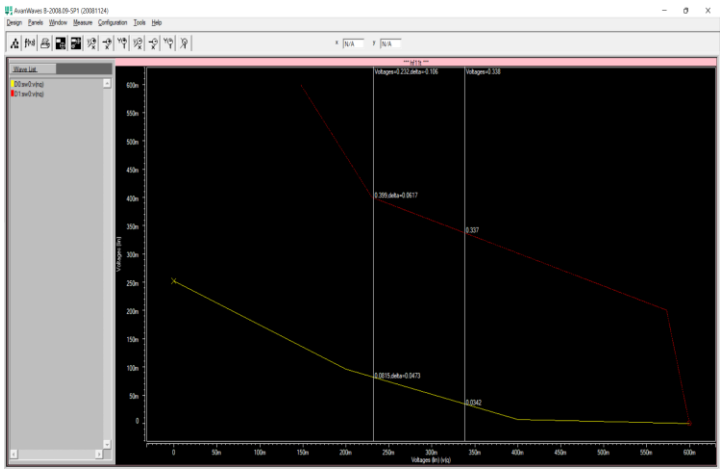


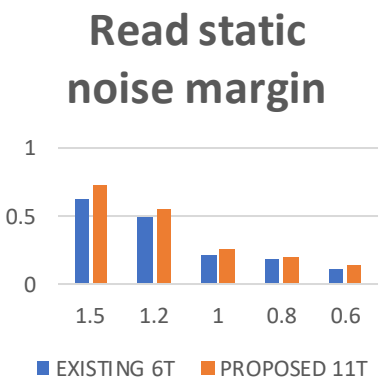
SNM Comparison of 6T and 11T SRAM for various supply voltage:

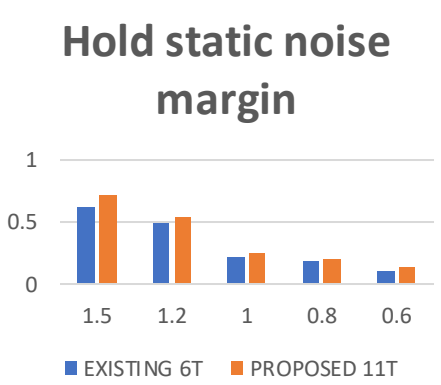
VOLTAGE(V)	RSNM(V)		HSNM(V)		WSNM(V)	
	6T SRAM	11T SRAM	6T SRAM	11T SRAM	6T SRAM	11T SRAM
1.5	0.5245	0.6169	0.0915	0.2169	0.6245	0.7224
1.2	0.4981	0.5361	0.0825	0.1123	0.4981	0.5451
1	0.2173	0.2214	0.0691	0.0742	0.2173	0.2518
0.8	0.1935	0.2048	0.0342	0.0518	0.1854	0.2948
0.6	0.1088	0.1263	0.0226	0.0299	0.1088	0.1381

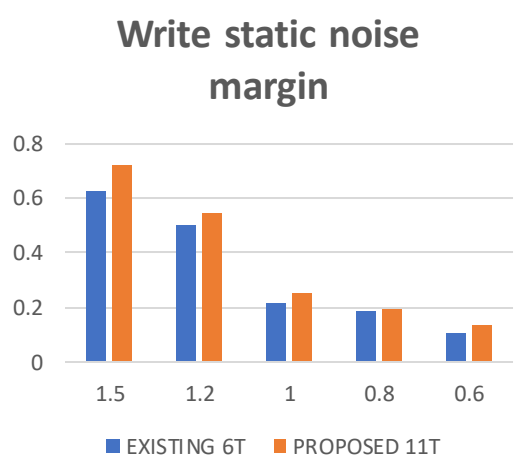












Results upto Second Review

Power Comparison on Various SRAM Cells:

Power supply(v)	Read static power(mw)		Hold static power(mw)		Write static power(mw)	
	6T SRAM	11T SRAM	6T SRAM	11T SRAM	6T SRAM	11T SRAM
1.2	1.734	0.568	1.321	0.780	0.4525	0.350
2	2.059	1.2248	2.7978	2.4306	1.9262	1.4549

Design of logic mode in polymorphic unit [PMU]: