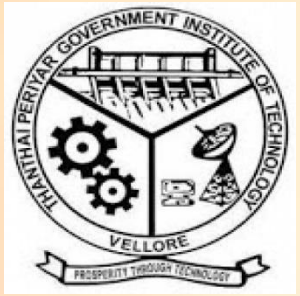


THANTHAI PERIYAR GOVERNMENT INSTITUTE
OF TECHNOLOGY,VELLORE.
DEPARTMENT OF ECE

AN ENERGY-EFFICIENT HYBRID SRAM/RRAM IN-MEMORY COMPUTING ARCHITECTURE WITH INDEPENDENT GATE FINFETs AND SECURITY ENHANCED POLYMORPHIC CIRCUITS

Project Guide: Mrs.M.Janani

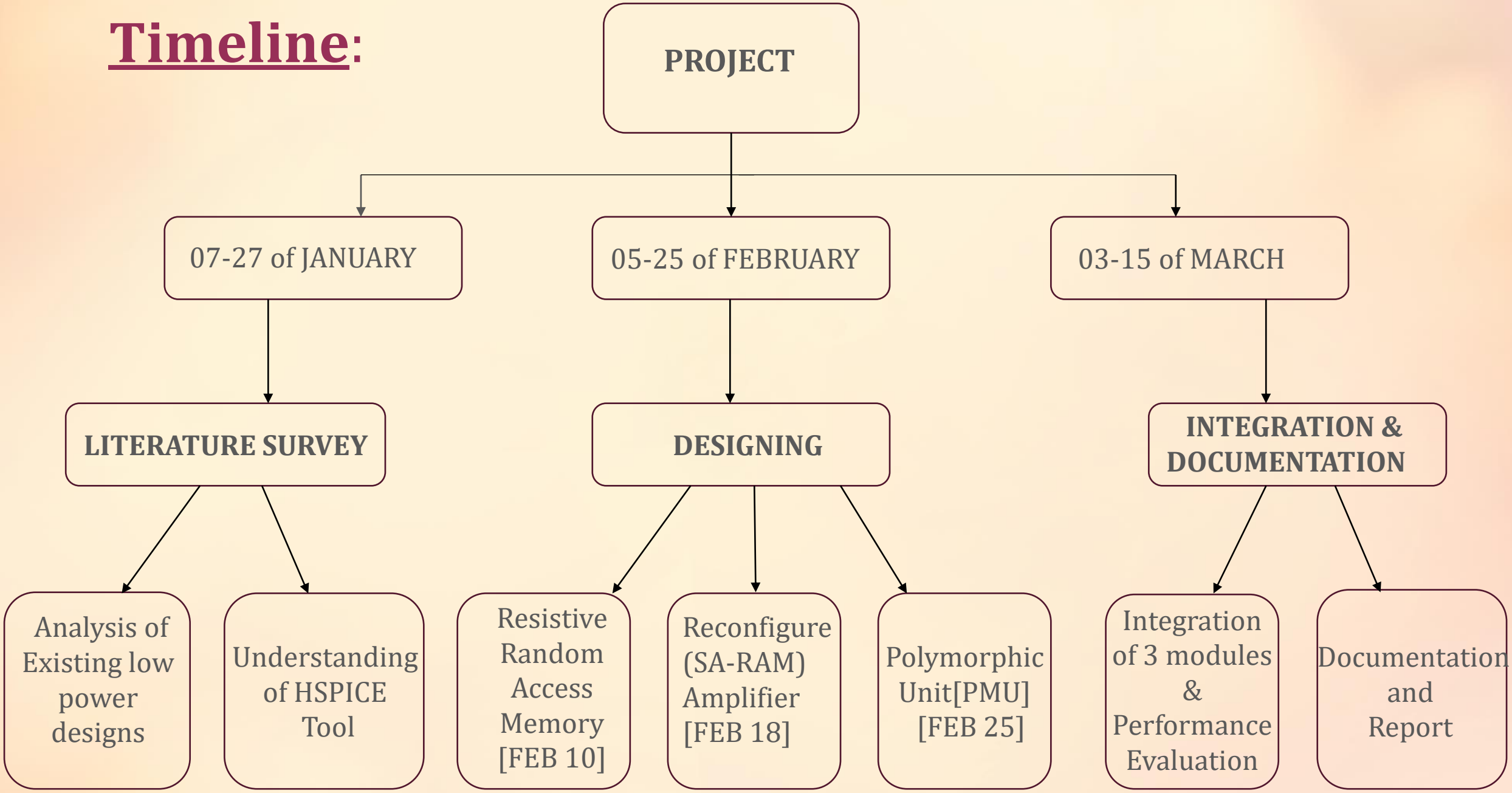
TEAM MEMBERS

- **TEAM MEMBER 1**: K.Vinitha (513120106095)
- **TEAM MEMBER 2**: B.Pavithra (513120106063)
- **TEAM MEMBER 3**: B.K.Shruthi (513120106078)

PROBLEM STATEMENT AND TECHNOLOGY PROPOSED

- The Hybrid SRAM/RRAM In-Memory Computing Architecture revolves around enhancing Energy efficiency and computational performance in memory centric tasks. The challenge lies in optimizing the integration of SRAM and RRAM technologies to enhance overall performance.
- The goal is to develop a flexible and efficient solution to implement all Boolean functions and also to overcome memory wall.
- Therefore, one of the most promising approaches for alleviating these challenges, In-memory computing (IMC) is proposed.
- **SOFTWARE TOOL**: SYNOPSIS HSPICE

Timeline:


PROJECT
07-27 of JANUARY
05-25 of FEBRUARY
03-15 of MARCH
LITERATURE SURVEY
DESIGNING
INTEGRATION & DOCUMENTATION
Analysis of Existing low power designs
Understanding of HSPICE Tool
Resistive Random Access Memory [FEB 10]
Reconfigure (SA-RAM) Amplifier [FEB 18]
Polymorphic Unit[PMU] [FEB 25]
Integration of 3 modules & Performance Evaluation
Documentation and Report

IMPLEMENTATION STEPS

MODULE 1:

1. **Analysis of Existing Designs:** Clearly articulate the challenges and goals for integrating Hybrid SRAM/RRAM in-memory computing architecture.

2. **Understanding of HSPICE Tool:** Acquire proficiency in HSPICE for accurate and detailed circuit simulations during the design phase.

MODULE 2:

3. **RRAM Designing:** Develop the Resistive Random Access Memory (RRAM) component of the hybrid architecture, considering performance and Power efficiency.

4. **Reconfiguring SA (SRAM):** Modify and optimize the Sense Amplifier (SA) in Static Random Access Memory (SRAM) for seamless integration with RRAM, ensuring adaptability.

5. **Polymorphic Circuit:** Explore and implement polymorphic circuit techniques to enhance flexibility and adaptability in the memory architecture.

MODULE 3:

6. **Integrate & Simulate:** Combine the designed components, integrating SRAM and RRAM, and simulate the entire architecture to validate functionality and performance.

7. **Performance Evaluation:** Systematically assess the hybrid SRAM/RRAM architecture's performance metrics, including speed, power consumption, and reliability.

8. **Documentation and Report:** Present conclusive results and insights from the performance evaluation, showcasing the advantages of the proposed hybrid memory architecture for in-memory computing.