## Intro:-

ELM stands for Embedded Linux Mezzanine, which is a small device based on Ultrascale+ ZYNQ FPGA. The main purpose of ELM is to serve as an on board control interface for ATCA modules. These test suites are being developed to automate/semi-automate the bring up tests of the ELM.

This manual includes the ZYNQ-DDR interface testing steps from HW configuration to SDK project building and actual testing on ELM. The DDR tests have to be done by a software program which already exists. The testing software should write various data patterns into the memory and then read back, thus we can check if the signal conditions of the PS-DDR interface are good enough or not. The DDR4 memory on the board is MT40A1G16KNR-075:E is a main RAM for the CPU having a total range of 4GB.

## Requirements-

* Vivado Design Suite (V2019.1) + SDK installed
* Board connected to the system with JTAG and USB-UART connection.

## Launching Vivado

----Steps to launch vivado on madorsky-d2---

* run this script, shown relative to the home directory:

>>> ~/bin/viv191.sh

## 

## 

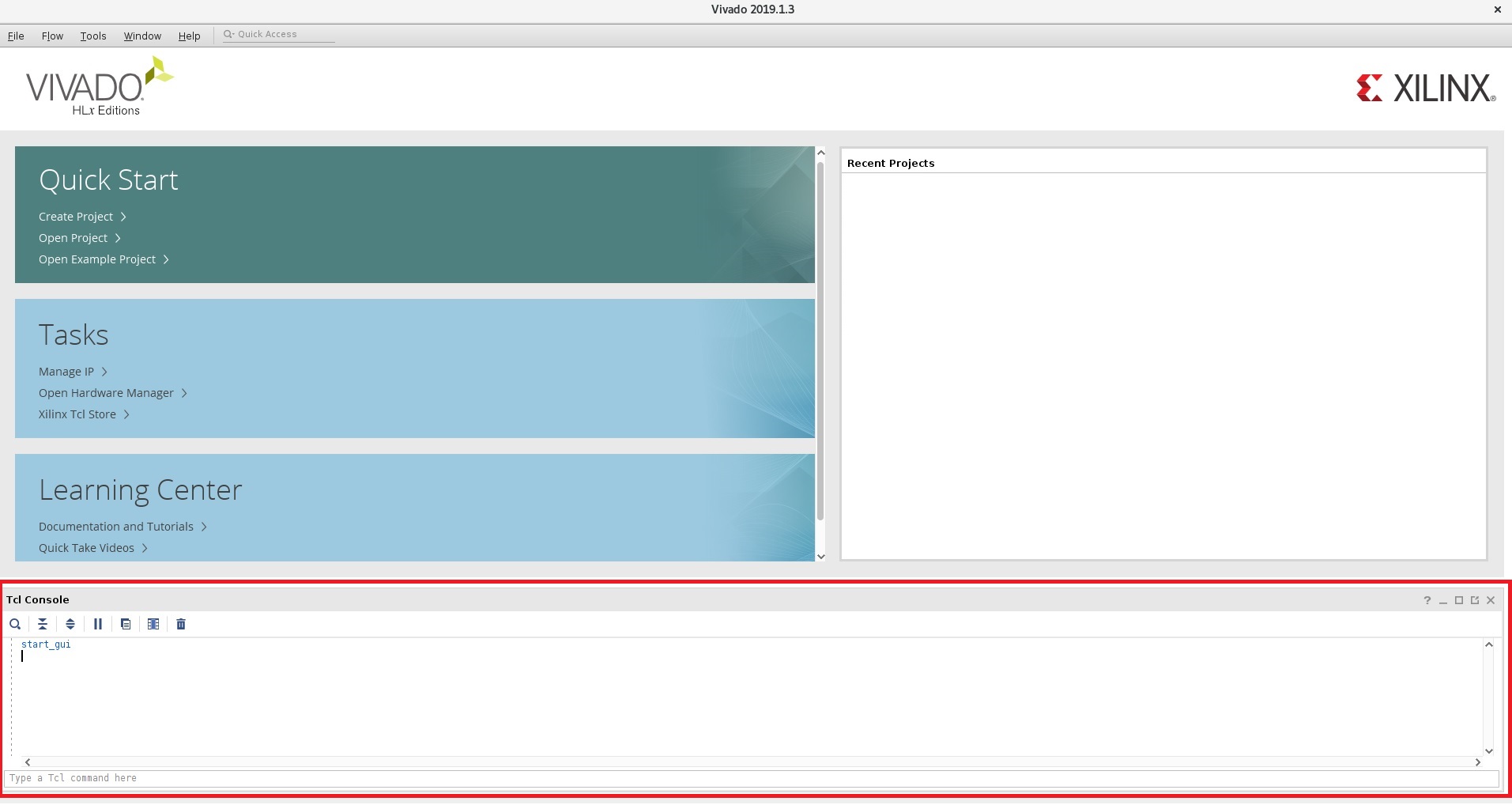
## Hardware (HW) configuration in Vivado-

### PS-DDR interface in vivado-

The HW configuration is done using Vivado Design Automation and IP integrator for simplicity. To automate the process of HW configuration, a tcl script is developed.

#### Running the TCL script-

1. After launching the Vivado,There are 2 options available to run the tcl script
   1. Using tcl console - Highlighted in Red below



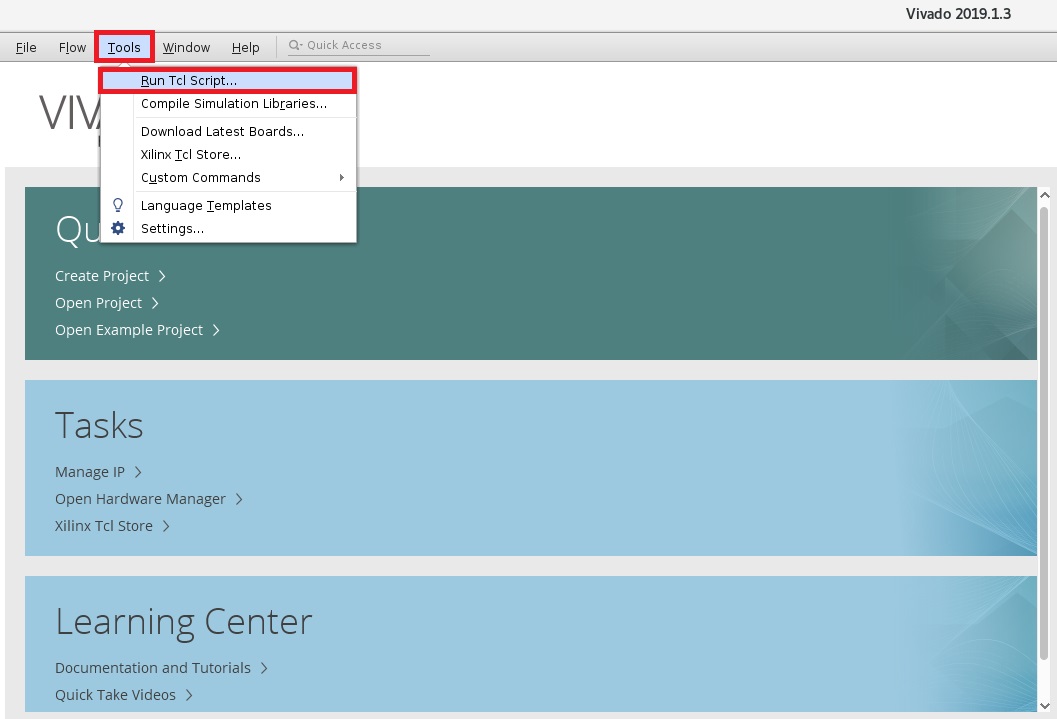
Run the following commands-

> cd <your project dir>

> source psddr.tcl

* 1. In Vivado GUI, Use option Tools-> Run Tcl Script

#### Here, the Tcl file is sourced by using GUI instead of using command line.



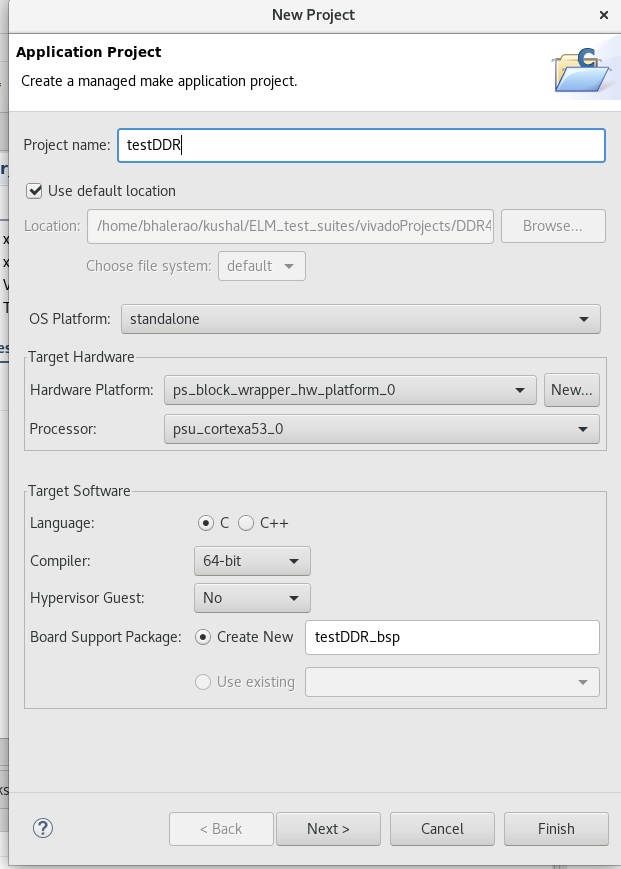
#### Both approaches do the same job.

#### The TCL script does the following tasks-

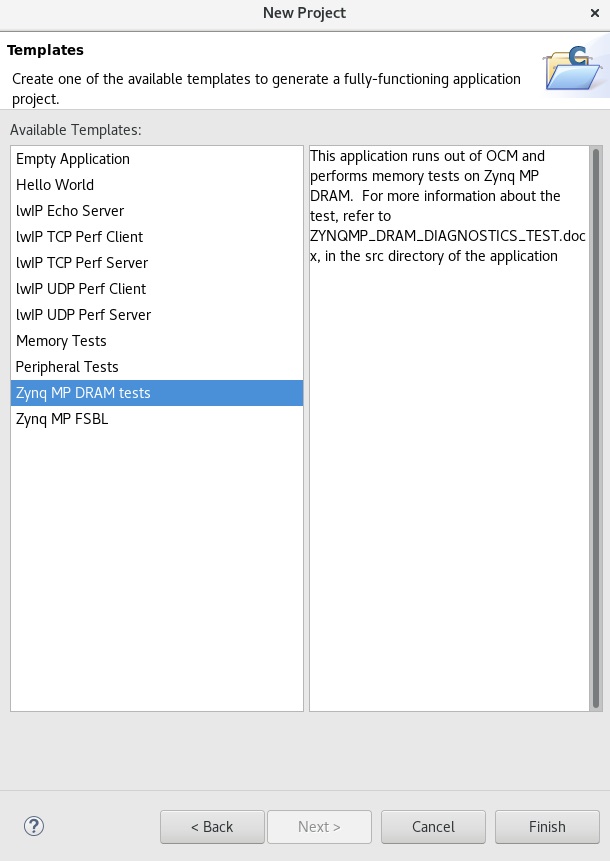
* Checks if the script is running the correct version (2019.1).
* Creates the new vivado project at current working directory (where the tcl is sourced) with the device as- xczu4cg-sfvc784-1-e
* Creates the block design in IP integrator with name ‘ps\_block’
* Configures ZYNQ UL+ IP with required parameters.
  + DDR
  + Clocks
  + PSU banks(0-3) IO standards
  + UART (MIO 5...9)
* Validates and saves the design
* Generate the HDL wrapper in target language and add it to the source file as a top module.
* Generates the Output products
* Export the hardware files to SDK
* Launch the Xlinx’s Software Development Kit (SDK)

## Xilinx’s Software Development Kit (SDK)

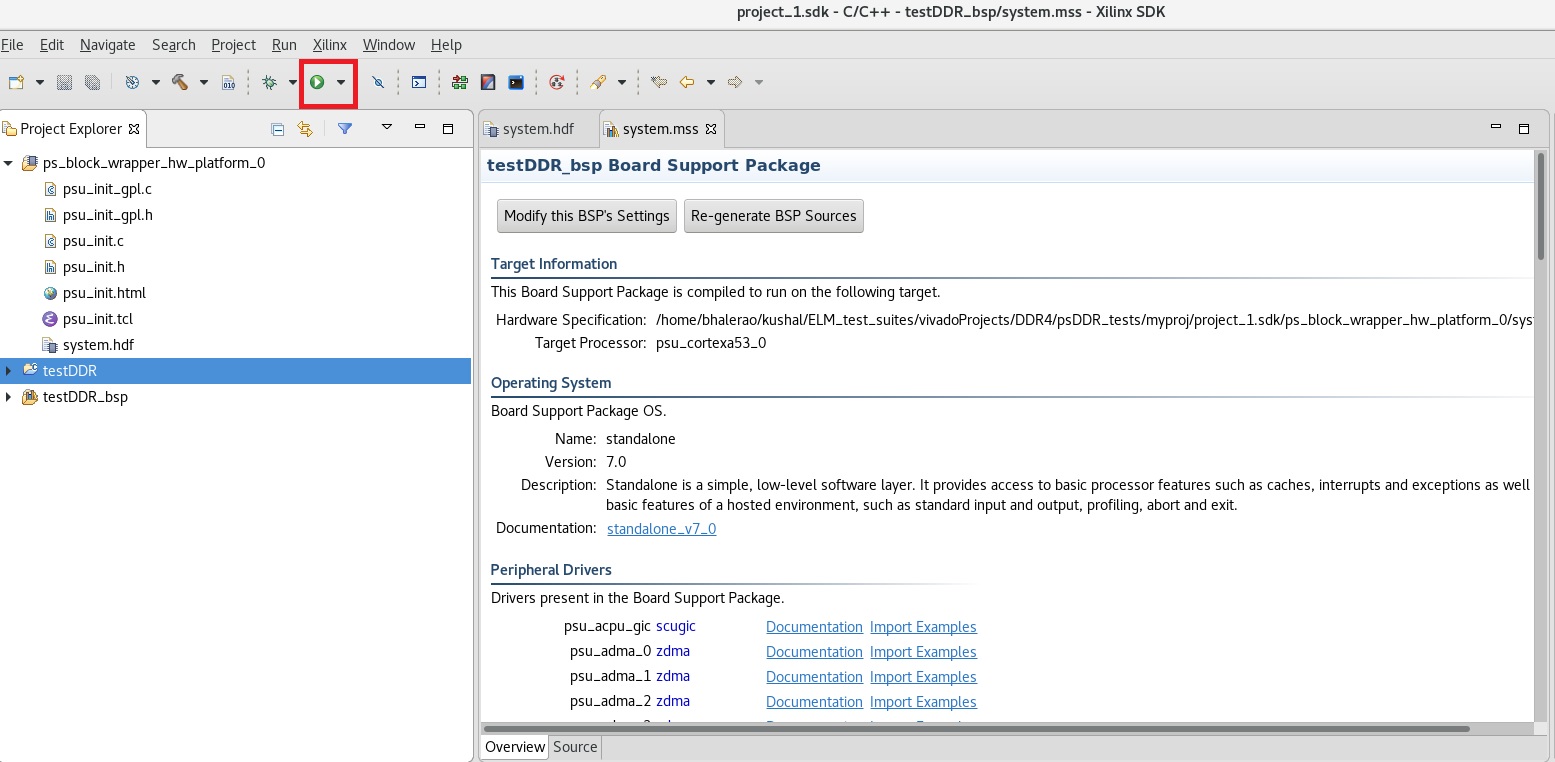
1. Once the SDK is launched, in the project explorer tab, select the ps\_block\_wrapper\_hw\_platform\_0 and File->New->Application Project. In the new project window, give the project name , and follow the settings below and click next.



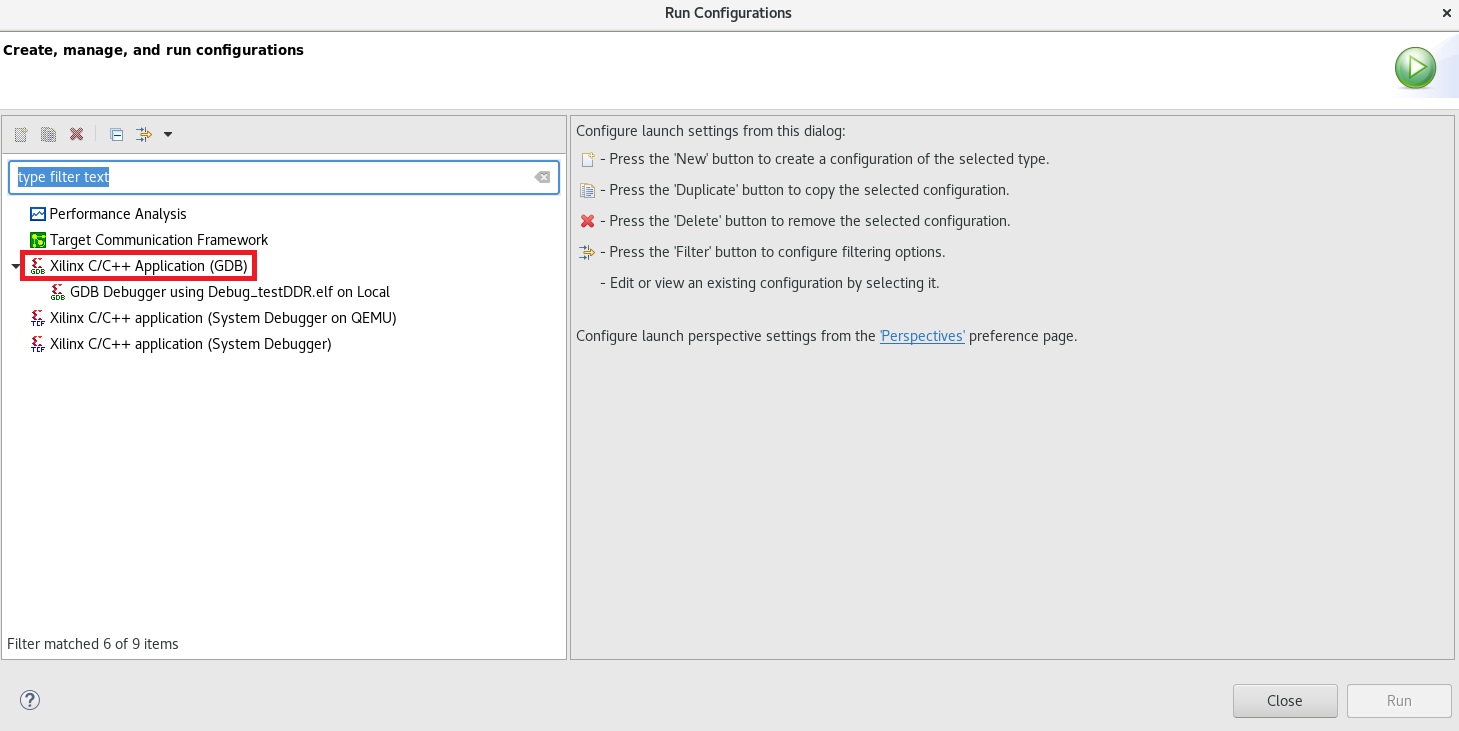
1. Next window would show the example templates available from Xilinx. The application template used for this testing is ‘ZYNQ DRAM tests’. Click Finish.



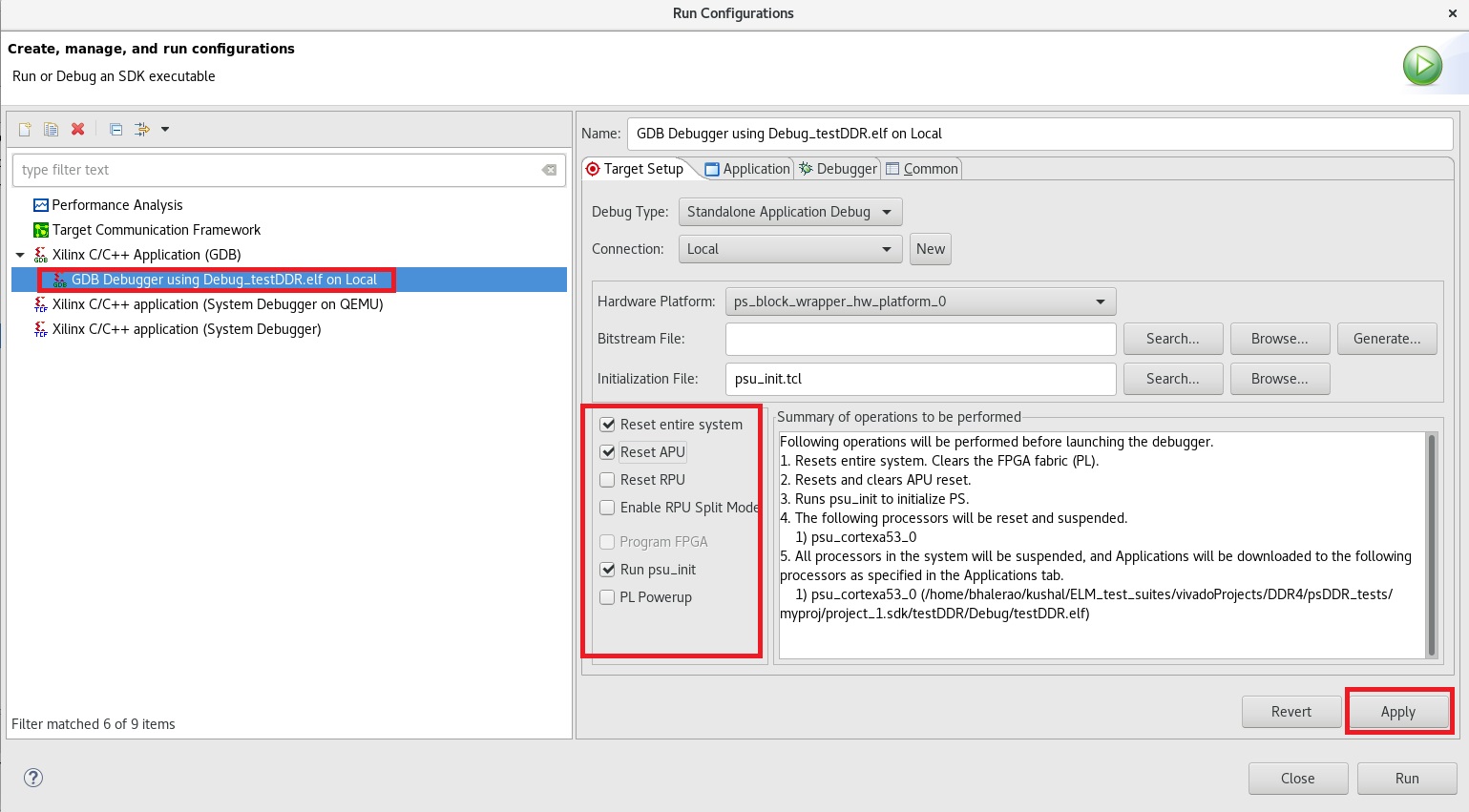
1. SDK adds this project to the Project Explorer window with its required bsp automatically generated. Once added, SDK automatically builds the project. Wait till the ‘Build Finished’ message prints on the console.Once Project is built successfully, select the application in Project Explorer window, locate the green button ‘Run’ tab and select ‘Run Configuration’.



1. In the Run configuration window, double click, Xilinx C/C++ Application (GDB).

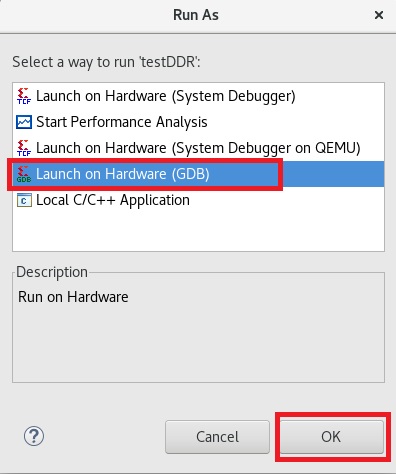
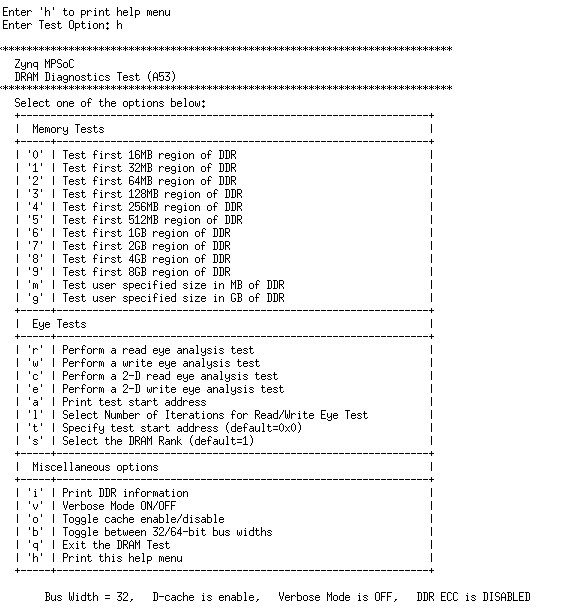


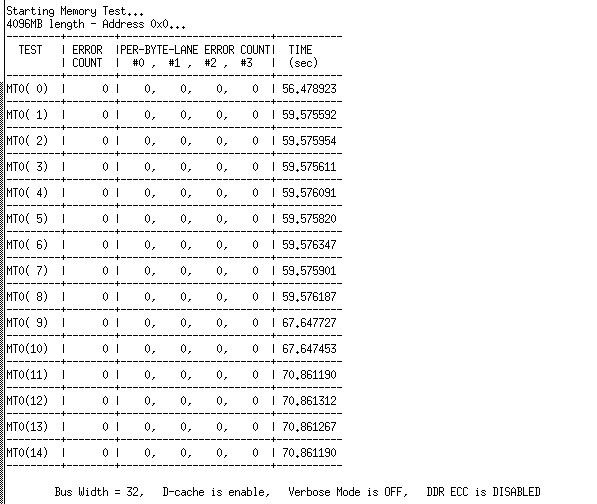
1. Then select the GDB Debugger using Debug\_testDDR.elf on local and follow the settings from the figure below and Click ‘Apply’



1. Before hitting ‘Run’, make sure the JTAG and USB-UART connection is done on the board and board is powered ON.
2. Verify the USB port by command- dmesg | grep ttyUSB. In case of madorsky-d2 machine, USB-UART bridge is connected to /dev/ttyUSB2
3. Open up a terminal/xterm and do- screen /dev/ttyUSB2 115200.



1. Now, hit the ‘Run’ button in the SDK. A pop- up window named ‘Run-As’ would appear, select Launch on Hardware (GDB).
2. If run is successful, below window would be appeared on the serial console.
3. The DDR test application is an interactive test, where the user can test the DDR for various memory ranges by selecting the appropriate command shown above.
4. The total range till which we can test is 4GB. So press‘8’ and hit <Enter>, it will start testing the selected range (4GB) with 15 different data patterns, starting from the logical address ‘0x0000000000000000’.



1. In the ‘src’ tab, a document named ‘ZYNQMP\_DRAM\_DIAGNOSTICS\_TEST.doc’ would be available, which briefs about the test patterns being used.