

VMEM VMEM C1 628128 A012 A111 A1 Q0 13D0 0.1uF Q1 14 D1 A210 A2 Q2 15D2 GND Q3 17D3 Q4 18D4 Q5 19 D5 A6 6 A6 20D6 Q7 21 D7 A926 A9 CS1 22 CS1 CS2 30 CS2 OE 24 OE WE 29 WE A1023 A10 A1125 A11 A12 4 A12 A1328 A13 A143 A1531 A15 A16 2 A16 GND

different SRAM parts standby current: R1LP0108E - 0.6 uA AS6C1008 - 1 uA CY62128ELL - 4 uA IS62C1024AL - 5 uA

The original board has three banks of four 8k by 8 SRAM ICs.

Each of the 3 $\overline{\text{CS1}}$ bank lines went to the enable of a decoder for each bank. The decoder selected $\overline{\text{CS1}}$ of an SRAM IC based on A13/A14.

In this <u>design</u>, a single 128k by 8 SRAM is used. An encoder combines the 3 $\overline{\text{CS1}}$ bank lines into two address lines, leaving one 32k bank of the SRAM unused.

It may be possible to use three 32k by 8 SRAMS and directly route a CS1 bank line to each. However that would not be entirely consistent with the original RAM module: In the original, when logic power is cut (but SRAM power is still present), the CS1 bank lines can no longer drive the SRAM CS1 lines. This circuit maintains that behavior by having the CS1 bank lines connect through the 74HC148.—ils

Originally based on Model600Sram_v1.1 by Jayeson Lee-Steer

LICENSE: CC-BY-SA 4.0

Brian K. White — b.kenyon.w@gmail.com

Sheet: /

File: TANDY_600_96K_SRAM.kicad_sch

Size: USLetter	Date: 2022-09-08		Rev: 007	
KiCad E.D.A. kid	ad 6.0.7-f9a2dced07~116	~ubuntu22.04.1	ld: 1/1	