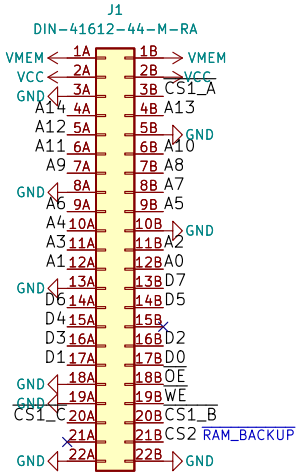


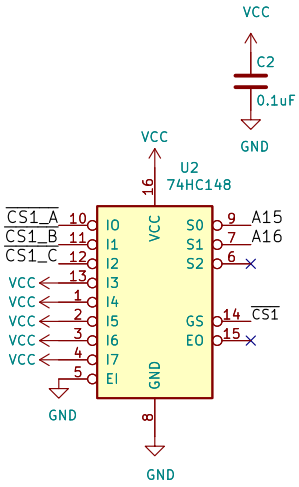


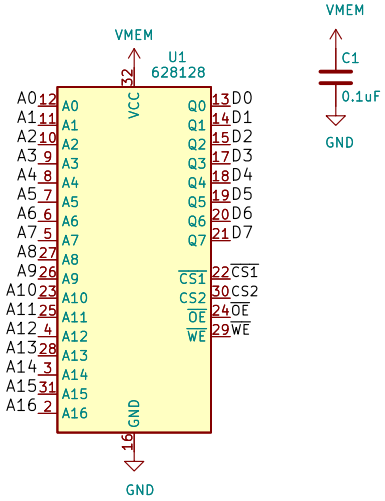


different SRAM parts standby current:
R1LP0108E – 0.6 uA
AS6C1008 – 1 uA
CY62128ELL – 4 uA
IS62C1024AL – 5 uA

The original board has three banks of four 8k by 8 SRAM ICs.

Each of the 3 $\overline{CS1}$ bank lines went to the enable of a decoder for each bank. The decoder selected $\overline{CS1}$ of an SRAM IC based on A13/A14.

In this design, a single 128k by 8 SRAM is used. An encoder combines the 3 $\overline{CS1}$ bank lines into two address lines, leaving one 32k bank of the SRAM unused.

It may be possible to use three 32k by 8 SRAMS and directly route a $\overline{CS1}$ bank line to each. However that would not be entirely consistent with the original RAM module: In the original, when logic power is cut (but SRAM power is still present), the $\overline{CS1}$ bank lines can no longer drive the SRAM $\overline{CS1}$ lines. This circuit maintains that behavior by having the $\overline{CS1}$ bank lines connect through the 74HC148.
–jls


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**Title: TANDY Model 600 96K SRAM Module**

| Size: USLetter | Date: 2022-09-08 | **Rev: 007** |
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